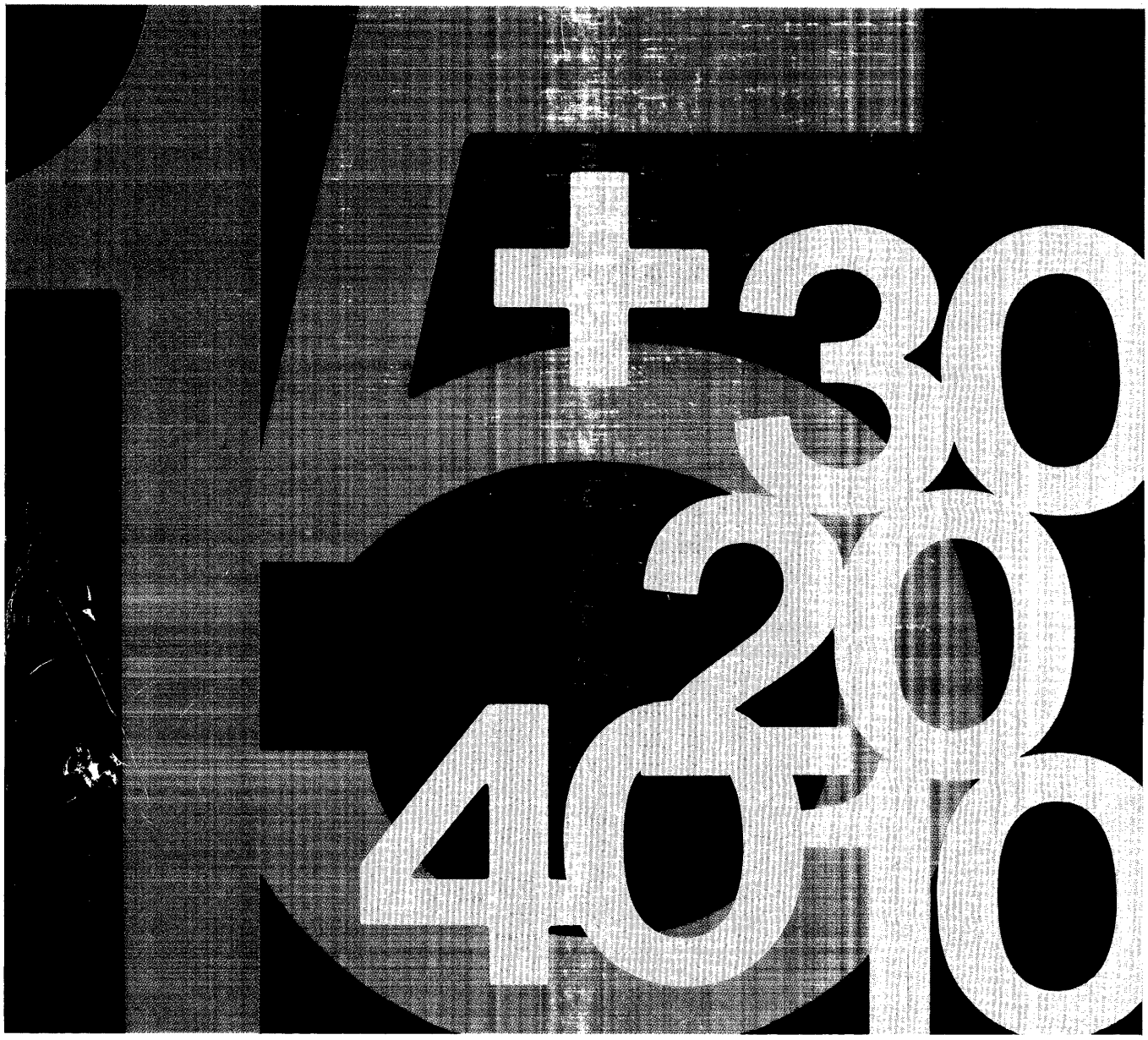
Digital Equipment Corporation
Maynard, Massachusetts

digital

PDP-15 Systems
Maintenance Manual
Volume 1

RP15 Disk Pack Control



DEC-15-H3GB-D

PDP-15 SYSTEMS
RP15 DISK PACK CONTROL MAINTENANCE MANUAL VOLUME 1

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

First Printing January 1971
2nd Printing (rev) October 1971

CONTENTS

CONTENTS (Cont)

CONTENTS (Cont)

CONTENTS (Cont)

ILLUSTRATIONS

ILLUSTRATIONS (Cont)

ILLUSTRATIONS (Cont)

ILLUSTRATIONS (Cont)

ILLUSTRATIONS (Cont)

ILLUSTRATIONS (Cont)

TABLES

CHAPTER 1
SYSTEM DESCRIPTION

1.1 GENERAL

This chapter describes the RP15 System in general terms and presents some characteristics of memory storage systems. An overall description is provided of the RP02 Disk Pack System as it interfaces with the PDP-15 Computer System. The remainder of the chapter defines certain controller parameters as they relate to overall system performance.

1.2 RP15 CONTROL

The RP15 Disk Pack Controller interfaces from one to eight RP02 Disk Pack Drives to the PDP-15 Computer (see Figure 1-1). Each RP02, when equipped with an RP02P Disk Pack, provides the PDP-15 Central Processor with an additional 10.24×10^6 18-bit words of memory storage at an average data acquisition time of 50 ms (positional) and 12.5 ms (rotational). Data are transferred through the PDP-15 single-cycle data channel provided by the I/O bus. Transfers are double buffered to produce a transfer rate of 14.8 μs for every two words and a latency time of 14.8 μs.

1.3 DISK SYSTEM CHARACTERISTICS

Modern computer systems use many methods to store information; each method has inherent advantages and disadvantages. Flip-flops and delay schemes are used for short-term data storage; magnetic devices are used for relatively long-term storage of data and instruction because once a magnetic state is established in the medium, it will remain, even after power is removed, until the state is modified or erased.

Core memories provide relatively small storage capacity (4K to 32K words) in minimal space, and offer the advantage of almost instantaneous retrieval. Because of this fact, core memories are used to store data in various computation stages, as well as with instructions of the main operating program.

However, rotating memories, such as magnetic tapes, provide greater capacity (150K to 8M words), but retrieval involves a search phase in a serial fashion by one fixed scanning device. For this reason, tapes are used for the storage of data that requires less frequent retrieval.

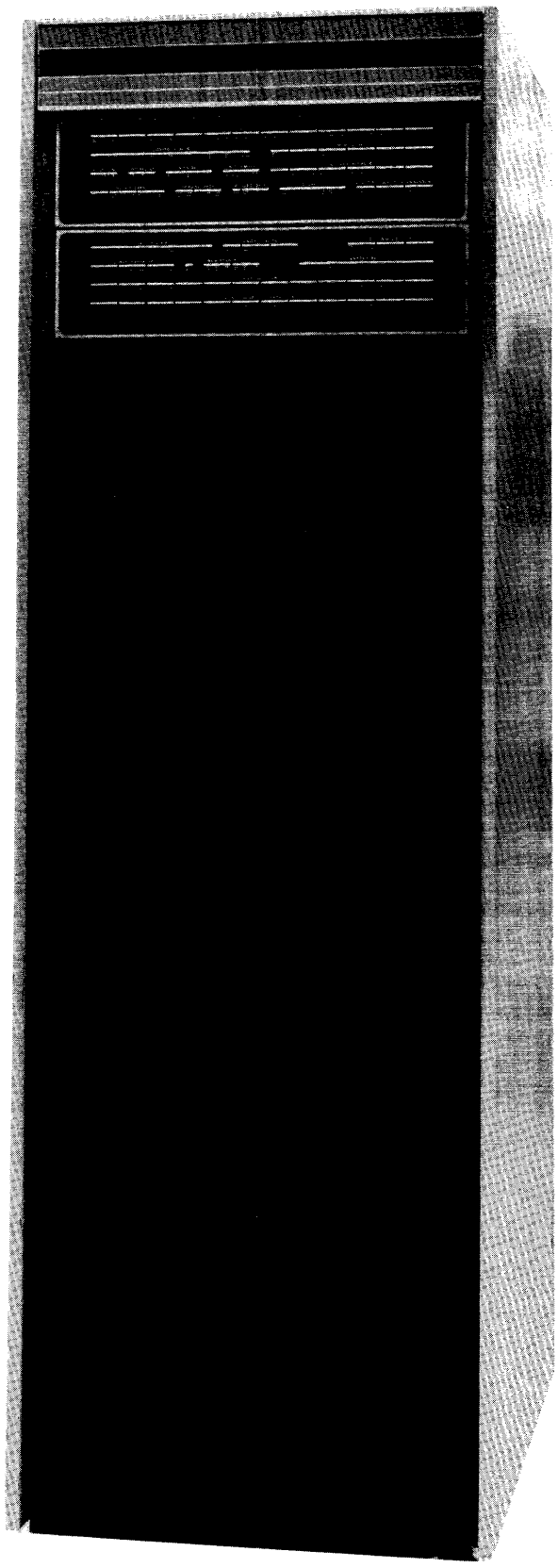


Figure 1-1 RP15 Disk Pack Controller

1.3.1 Disk vs Drum

The larger rotating memories (drum and disk) provide massive storage capability but retain the disadvantage of search; access times are orders of magnitude better than for tape. As with tapes, these memories require a synchronizing or clocking scheme that serves as a constant indication of instantaneous scan speed, so that synchronization with the operating system may be achieved.

Rotating memories serve a "scratch pad" or "swapping" function in the overall scheme of the computer; and provide short-term storage of routines, subroutines, or blocks of data in some intermediate state of computation. These memories are also used for long-term storage of tabular functions, catalogues, dictionaries, and other reference material. In time-shared systems, rotating memories serve as temporary repositories of partially completed operations, thereby freeing the other storage mediums to service a higher priority request.

The drum is usually a non-removable device in which a set of fixed flying heads write the data in a particular format across the outside surface of the cylinder. It has particular application in vibrational environments or in installations where atmospheric conditions are not stringently controlled. The drum has a constant diameter and presents a fixed frequency response characteristic to the data being recorded. The response of the disk is directly proportional to its diameter, and the bit density of the innermost track is much greater than for the outermost track. This disadvantage can be overcome easily and is a small consideration compared to the advantage of increased data capacity.

1.3.2 Disk Pack Effects on the Drive

The use of a removable media device, such as a disk pack, places some constraints on the design of the drive. Basically, the head design is affected because a movable head arrangement must be used so that the heads may be retracted while removing the pack. This requirement dictates that a set of single heads be held in vertical alignment by a common head tower which, in turn, must be actuated hydraulically, pneumatically, or by an electric positioning motor. Positioning means that extra logic must be provided for positioning comparators and servo control of head motion during these operations. The disadvantage of additional machinery and logic is minimal, however, when compared to the unlimited storage capacity provided by being able to remove and store many packs per drive.

1.4 RP02 SYSTEM CHARACTERISTICS

1.4.1 RP02P Disk Pack

The RP02P Disk Pack, shown in Figure 1-2, is the recording medium used with the RP15 Controller, and it is designed for mounting on an RP02 Disk Pack Drive. The RP02P is comprised of 11 aluminum

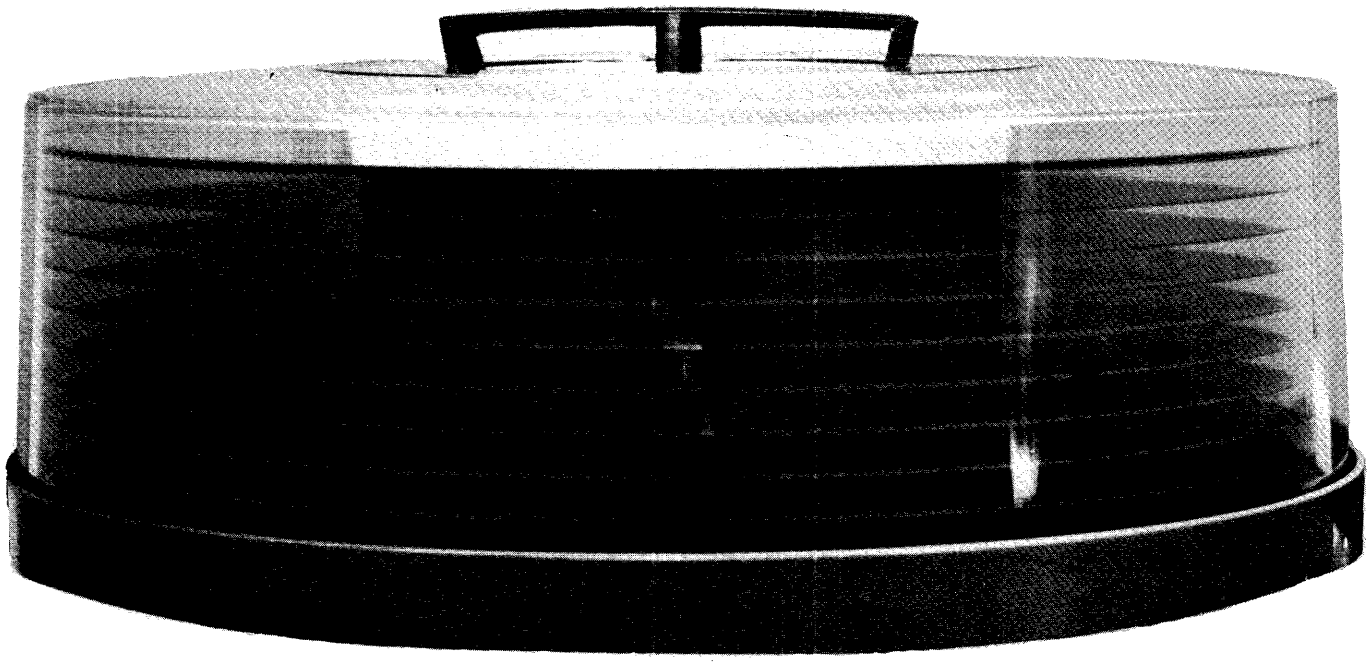


Figure 1-2 RP02P Disk Pack

disks coated with magnetic oxide and mounted 1/2-in. apart on a common hub. Information is recorded on the 20 inner surfaces.

The bottom disk is not used for recording and is notched to produce timing pulses for synchronization with the controller (see Figure 1-3). The disk contains 20 evenly spaced notches and a 21st notch called the index. The drive is equipped with a reluctance type pickup that senses these notches and sends a signal to the controller where the pulses are frequency divided to produce 10 sector indicators. An additional circuit then separates the index pulse. Note that the sectors are numbered octally.

1.4.2 RP02 Disk Pack Drive

The RP02 Disk Pack Drive is the mechanism controlled by the RP15 Controller (see Figure 1-4). It comprises two major subassemblies:

a. The spindle driving mechanism and
b. The head positioning system.

The spindle driving mechanism is made up of an ac motor, mounted below the baseplate that transmits a rotation of 2400 rpm to the disk pack by driving a conical spindle through a drive pulley and belt loop. The spindle secures the pack with a locking shaft within the spindle and washers below the spindle pulley. A mechanical lock is actuated by raising the cover. A pack-on switch disables spindle-drive motor power until a pack is installed.

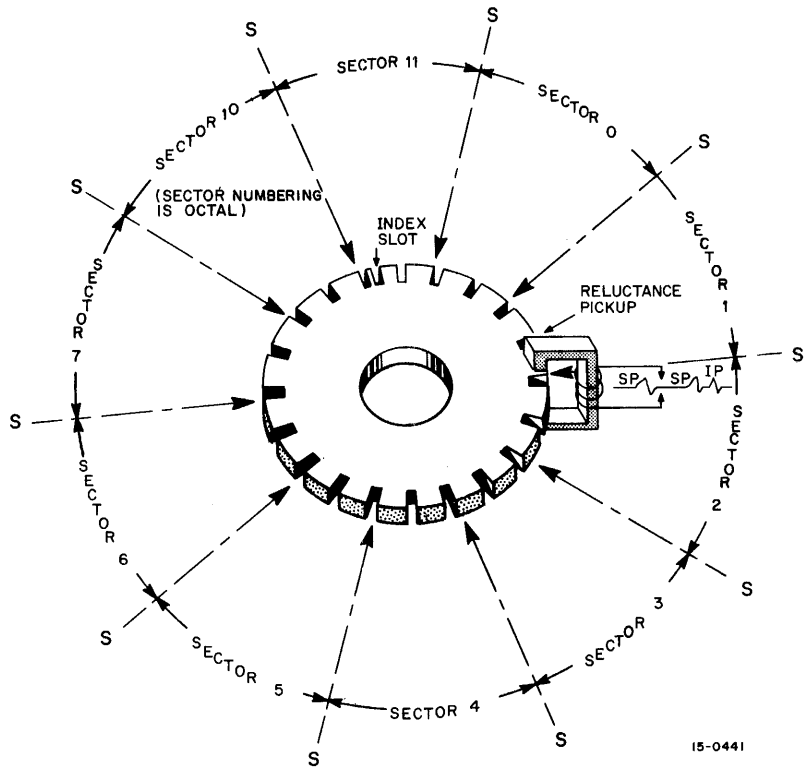


Figure 1-3 RP02P Disk Pack Sector and Index Pulse Generation

The head positioning system consists of a linear positioning motor that moves a T-bar tower along a horizontal carriage, either toward or away from the center of drive motor rotation. When the T-bar is fully retracted, it is sensed by a microswitch and braking power is applied. The disk pack may then be removed. The T-bar is used to mount 20 back-to-back head assemblies that are unloaded by camming action when the linear motor is fully retracted. A detenting mechanism stops the head assembly over any cylinder position.

The drive provides a means to monitor head position, drive speed, and rotational position. A cylinder transducer, made up of a 145 kHz excited sensing transformer and a toothed rack that rides with the head assembly and passes the sensing transformer while heads are in motion, produces a modulated signal that is an indication of head position. This signal is fed to an up/down counter in the RP02 logic. Drive speed and rotational position are monitored by a dc reluctance pickup that senses slots in the bottom disk of the pack (see Figure 1-3). This signal is sent back to the controller, to indicate disk position, and to a flip-flop rate sampler within the drive logic to generate an up-to-speed indication to the controller whenever the drive reaches 70 percent of rated speed.

Dynamic braking of the drive motor is accomplished by replacing ac power with dc power for approximately 12 seconds, whenever the STOP switch is depressed. Dynamic braking also occurs whenever the cabinet cover is lifted.

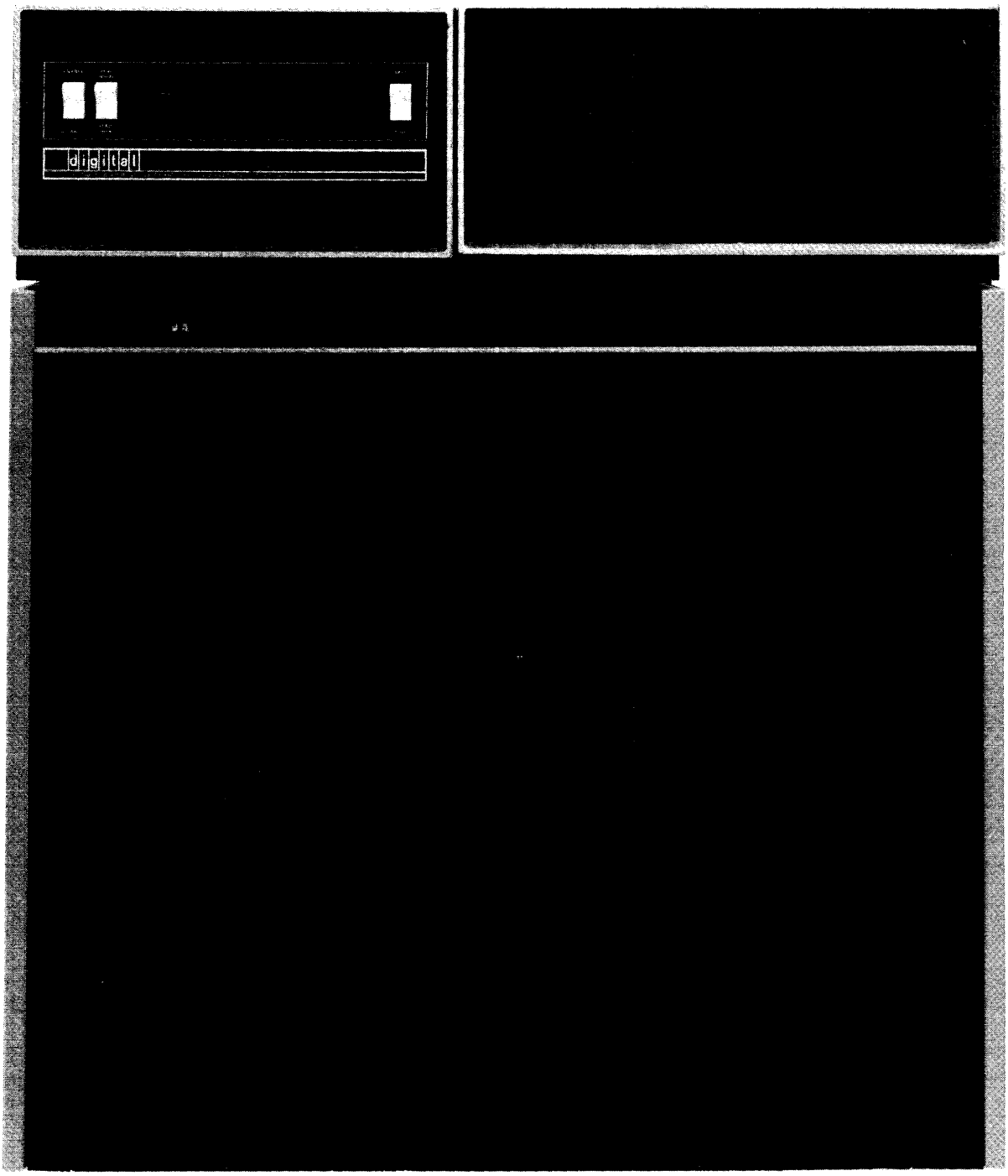


Figure 1-4 RP02 Disk Pack Drive

The read/write heads contain two center-tapped coils (one for the read/write gap and one for the erase pole). Diode switching is used to place ground on the center tap of the selected head. The heads are

gimbal-mounted in the horizontal plane and leaf-spring loaded in the vertical plane; when the disk is up to speed, the heads fly on a cushion of air over the surface of the disk.

There are four basic operations performed by the drive under controller command. They are:

Seek
Write
Read
Recalibrate

The Seek operation is initiated by the receipt of a cylinder address from the controller. The drive logic compares this address with its present address and determines the direction in which the heads must move. Head motion is then accomplished and monitored by a difference count within the drive and is detented in position when the count reaches zero. The time required to locate the next cylinder address is limited to 100 ms by a time delay actuated at the start of the Seek. Failure to re-detent during this time results in a SEEK INCOMPLETE to the controller. When the new address is reached, and after a 3.0-ms damping delay, the drive indicates to the controller its readiness to Read or Write.

When Write is commanded, the controller supplies data to the write-selected head as a double-frequency non-return-to-zero pulse train, together with clock pulses for synchronization. The data and clock information are recorded as reversals in magnetic flux on a side-trimmed 0.006-in. wide track.

When Read is commanded, the same head is read-selected to sense the previously recorded flux changes, producing current reversals in the head windings. This signal, which contains both data and clock pulses, is sent to the controller for processing.

When Recalibrate is commanded, the heads are moved by a forced forward seek that sends the carriage to the forward stop. When the carriage reaches the stop, it executes a normal reverse seek to home position (cylinder 000). The drive signals the controller 3 ms after detent that it is ready for instructions.

NOTE

The sequence just described occurs as a "first seek" whenever the drive START switch is depressed and after the motor has reached 70 percent of rated speed.

There are several safety circuits in the RP02 drive. These circuits protect data from being destroyed in the event of component failure. With the exception of ac/dc voltage failure, all conditions will issue a FILE UNSAFE indication to the controller; will deselect heads and terminate Read, Write, or Erase operations; will drop ready; and will light FILE UNSAFE on the panel. The FILE UNSAFE indication can be reset by switching START/STOP to the STOP position. Loss of primary power will remove all dc voltages from the machine. This automatically prevents Write current. If any dc logic voltage is

lost, heads are deselected to prevent writing. If an unsafe condition is present when a drive is turned on, an indication of FILE UNSAFE is given immediately. If the heads are extended when primary ac power fails, STOP is depressed, or the disk compartment door is opened before depressing STOP; the heads will automatically retract.

1.5 PDP-15 COMPUTER SYSTEM CHARACTERISTICS

The PDP-15 Computer System consists of three asynchronous subsystems:

a. Central Processor (CPU)
b. Memory
c. I/O Processor (I/O PU).

The PDP-15 is an 18-bit word length machine with a memory cycle time of 800 ns. Optional features include core memory expansion out to 131,072 words and a memory-protect system.

The CPU conducts bidirectional communication with both the memory and the I/O PU. It performs all required arithmetic and logical operations while controlling and executing stored programs. The core memory is the primary storage area for instructions and data. It is organized into pages and banks, with two pages comprising one bank. A page is capable of storing 4096 18-bit words. The I/O PU provides the timing, control, and data lines between either the memory or the CPU, and the peripheral devices. In addition, it can contain a real-time clock and an automatic priority interrupt system. The I/O PU handles all peripheral data transfers. These transfers are accomplished in three possible I/O modes as follows:

a. Single-cycle block (up to a million words/second)
b. Multicycle block (250,000 words/second input and 188,000 words/second output)
c. Program-controlled (single word to/from CP Accumulator).

The three subsystems operate together under console control. The console provides manual initiation of programs, monitoring of CPU and I/O PU registers, and manual examination and modification of memory contents.

The RP15 interfaces with memory through a single-cycle data channel break. The minimum PDP-15 configuration required for use with the RP15 Disk Pack Controller is the PDP-15/10 augmented by 8K of memory, and a PC15 High-Speed Paper Tape Reader/Punch. This is the first level system. The configuration is expandable due to pre-wired facilities that allow additional memory and peripherals to be plugged in at any time.

1.6 SINGLE-CYCLE INTERFACE AND I/O BUS

The RP15 transfers data to and from the PDP-15 via the single-cycle data channel. During a single-cycle transfer, the RP15 keeps track of its own word count (WC Register) and specifies the absolute address from or to which it wishes to transfer (CA Register).

The PDP-15 Permits two modes of single-cycle operation termed "Normal" and "Burst". The Burst mode is used when the device can transfer a word every microsecond.

In the RP15, all transfers are made in the Burst (or back-to-back) mode unless an odd number of words is to be transferred, in which case the last word is transferred in the Normal mode. Such transfers are made possible by a double-buffering scheme that allows assembly of two 18-bit words within the controller before they are transferred. This is done to achieve an economy of demand on the I/O bus that allows other devices access to the bus during RP15 assembly time (see Figure 1-5).

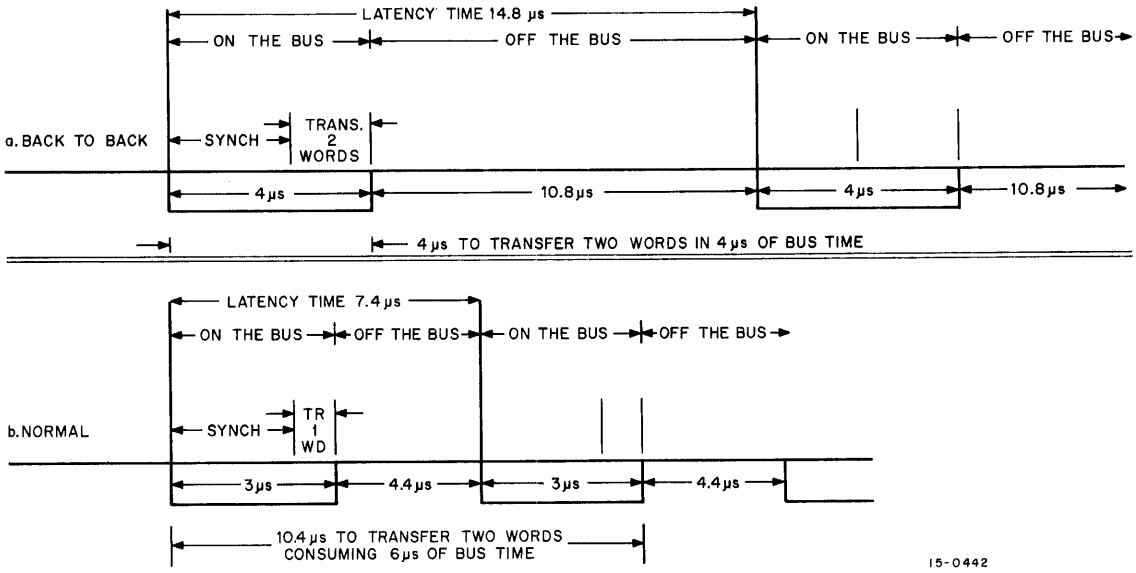


Figure 1-5 Latency vs Transfer Time in Normal and Back-To-Back Modes

Because of the rotational speed of the RP02, the latency time for double-buffered transfers is 14.8 μs, i.e., in this mode the RP15 must have access to the I/O bus every 14.8 μs, as long as it is transferring data on a two-word-per-break basis. If access is not granted in that time, a timing error will be raised.

As shown in Figure 1-5a, the first two words use 4 μs of I/O bus time (2 μs fixed synchronization + 1 μs/word). This leaves 10.8 μs of bus time during which other devices may have access to the bus (provided, of course, their latency times are compatible). Figure 1-5b shows the transfer characteristics

for a single word transfer (last word in an odd number of words) in which the latency time is 7.4 μs. Note that what is termed the Normal mode of operation is the uncommon mode of operation for the RP15. If single buffering had been used in the RP15, all words would have been transferred on this one-word-at-a-time basis, and only 4.4 μs of bus time would have been available for interlacing devices. In addition, 2 μs of fixed synchronization time would have been wasted on every second word transferred.

1.7 REFERENCE DOCUMENTS

The following documents contain information which supplements that contained in this manual:

PDP-15 Interface Manual (DEC-15-HOAB-D)
PDP-15 Systems Reference Manual (DEC-15-BRZA-D)
PDP-15 Installation Manual (DEC-15-H2AB-D)
PDP-15 Operator's Guide (DEC-15-H2CA-D)
PDP-15 Module Manual (DEC-15-H2EA-D)

CHAPTER 2
CONTROLS AND OPERATIONS

2.1 GENERAL

This chapter contains information required to operate the RP15 Controller. Controls and indicators are also identified.

2.2 CONTROLS AND INDICATORS

The RP15 indicators are located on the top front of the unit and are defined in Table 2-1. The controls are located on a logic panel inside the front door (refer to Table 2-2). The RP02 indicators and controls are located on its console panel and are explained in Tables 2-3 and 2-4, respectively. The controls and indicators for both units are shown in Figure 2-1. Power controls and indicators for the RP15 are found on the Type 841B Power Control located inside the RP15 cabinet. These are not included in Tables 2-1 through 2-4, but are shown in Chapter 8.

Table 2-1
RP15 Indicators

Index No.	Name	Function
1	BUFFER REGISTER	Thirty-six indicators that light on binary 1s to show the contents of the Buffer Register's two PDP-15 words.
2	CONTROL STATUS comprising:	Nine indicators that show controller status as follows:
	DED	One lamp that lights when the DONE and ERROR flags are disabled from the Program Interrupt (PI) and the Automatic Priority Interrupt (API) system.
	ATD	One lamp that lights when the ATTENTION flag has been disabled from the PI and API system.
	GO	One lamp that lights when bit 08 of Status Register A is set, enabling the Function Register to be executed.

Table 2-1 (Cont)
RP15 Indicators

Index No.	Name	Function
2 (cont)	DISK FLG	One lamp that lights when any error, attention, or job done flags have been raised.
	JOB DONE	One lamp that lights when a function is complete. (Exceptions are Idle, Recalibrate, and Seek.)
	ATT FLG	One lamp that lights on an attention flag which is raised whenever any unit attention is raised (OR of UA00-07).
	ERR FLG	One lamp that lights when any error condition occurs (OR of all errors).
	BK RQ	One lamp that lights when a request is made to access memory.
	BUSY	One lamp that lights when the controller is busy (other than Idle).
3	WORD COUNT Register comprising:	Sixteen indicators that show the following:
	WC OVFLO	One lamp that lights when a word count overflow has occurred, i.e., when the desired number of word transfers are complete.
	WC 03-17	Fifteen lamps that show the 2's complement of the number of 18-bit words yet to be transferred from or to memory.
4	FUNCTION Register FR00-02	Three indicators that light on binary 1s in bits 03, 04, and 05 of Status Register A to show a 3-bit octal number corresponding to one of eight functions to be performed. 0 = Idle 1 = Read 2 = Write 3 = Recalibrate 4 = Seek 5 = Read All 6 = Write All 7 = Write Check
5	UNIT SELECT Register UR00-02	Three indicators that light on binary 1s in bits 00, 01, and 02 of Status Register A to show a 3-bit octal number corresponding to the unit (one of eight) selected. 0 = Unit 0 1 = Unit 1, etc.
6	UNIT STATUS Register comprising:	Five indicators that show the status of the unit selected as follows:

Table 2-1 (Cont)
RP15 Indicators

Index No.	Name	Function
6 (cont)	SUOL	One lamp that lights when the selected unit has power and is placed on line by a switch on that unit console.
	SU RDY	One lamp that lights when the selected unit is ready for data transfer.
	SUSU	One lamp that lights when a seek is underway on the unit selected.
	SURO	One lamp that lights when the selected unit is in READ ONLY mode as selected by a switch on that unit console.
	SULO	One lamp that lights when the selected unit is locked out, i.e., LOCKOUT switch in LOCK-OUT position, the Unit Select register is equal to the Lock-out register, and the CAR $\leq$ LOA.
7	SWITCH MODE Register comprising:	Three indicators that show the status of the control switches on the RP15 logic as follows:
	FMT	One lamp that lights when the FORMAT/ NORMAL switch is in the FORMAT position.
	NORM	One lamp which lights when the FORMAT/ NORMAL switch is in the NORMAL position.
	LOCKOUT	One lamp that lights when the LOCKOUT switch is in the LOCKOUT position indicating that the LO and LOA switches are enabled.
8	CURRENT ADDRESS Register CA01-17	Seventeen indicators that show bits 1-17 of the current memory address.
9	CYLINDER ADDRESS Register CAR00-07	Eight indicators that light on binary 1s showing the contents of the Cylinder Address register in the RP15.
10	HEAD ADDRESS Register (Surface Address) HAR00-04	Five indicators that light on binary 1s to show the current head address.
11	SECTOR ADDRESS Register SAR00-03	Four indicators that light on binary 1s to show the current sector address.
12	LOCKOUT Register comprising:	Six indicators that light on binary 1s as follows:
	LO00-02	Three Lockout Unit Lamps that indicate the unit number (0-7) on which writing cannot take place in or below the cylinder address indicated by the Lockout Address Indicators if the LOCK-OUT switch is set.
	LOA00-02	Three Lockout Address Lamps that indicate the cylinder address (in octal) in or below which

Table 2-1 (Cont)
RP15 Indicators

Index No.	Name	Function
12 (cont)		writing cannot take place on that unit displayed by the Lockout Unit Indicators if the LOCKOUT switch is set.
13	SELECTED UNIT CYLINDER ADDRESS Register SUCA00-07	Eight indicators that light on binary 1s from the Cylinder Address Register in the selected RP02, showing the address in that unit at which the heads are presently positioned.
14	CONTROL STATE Register comprising:	Seven indicators that show the current state of the controller as follows:
	READ	One lamp that lights when the control is in Read state.
	WRITE	One lamp that lights when the control is in Write state.
	SEEK	One lamp that lights when the control begins a Seek.
	CLR HEAD	One lamp that lights when the control is in Clear Head state, i.e., head select register is cleared in RP02 Drive.
	INC HEAD	One lamp that lights when the control is in Increment Head state, i.e., when the current head is being disabled and the next head selected in the RP02 Drive.
	RECAL	One lamp that lights when the control begins a Recalibrate.
	IDLE	One lamp that lights when the control is in Idle (non-busy state).
15	UNIT ATTENTION Register UA00-07	Eight indicators that light on binary 1s showing the unit (0-7) from which ATTENTION has been raised as a result of a successfully completed SEEK command.
16	SECTOR WORD COUNT Register comprising:	Eight indicator lamps that indicate the following:
	SWC OVFLO	One lamp that indicates that the sector word counter has overflowed, signaling that the required number of 36-bit words have been transferred to or from the disk.
	SWC00-06	Seven lamps that show the number of 36-bit words read or written in a single sector.
17	FORMAT GENERATOR Register FMT GEN00-08	Nine indicators that light on binary 1s showing the state of the format generator.

Table 2-1 (Cont)
RP15 Indicators

Index No.	Name	Function
17 (cont)		This register controls formatting during WRITE, WRITE ALL, and FORMAT instructions.
18	MAINTENANCE Register comprising:	Seven indicators that show the following:
	MNT	One indicator that lights when the controller is in the maintenance mode.
	MR00-05	Six indicators that show the binary contents of the Maintenance Register.
19	ERROR STATUS comprising:	Fourteen indicators that show that an error has occurred as follows:
	FE	One lamp that indicates a Format Error has occurred due to a parity error in a header word.
	WE	One lamp that indicates a Word Error has occurred due to a parity error in a data word.
	LE	One lamp that indicates a Longitudinal Error has occurred due to a parity error in a bit position of a single sector.
	WCE	One lamp that indicates a Write Check Error has occurred due to no comparison between two 18-bit words read from memory and a paired data word read from the disk.
	TE	One lamp that indicates a Timing Error has occurred due to a missed transfer of a data word to or from processor memory.
	PE	One lamp that indicates a Programming Error has occurred due to an illegal series of RP15 instructions.
	HNF	One lamp that indicates a Header Not Found error has occurred due to the traversing of a complete revolution of the disk while searching unsuccessfully for a header word (unique sector address).
	WPE	One lamp that indicates a Write Protect Error has occurred due to a violation of either of two Write Protect functions.
	NEC	One lamp that indicates a Non-Existent Cylinder address has been commanded. This bit is present as long as an illegal cylinder address resides in the CAR.
	NEH	One lamp that indicates a Non-Existent Head (surface) address has been commanded. This bit is present as long as an illegal head address resides in the HAR.

Table 2-1 (Cont)
RP15 Indicators

Index No.	Name	Function
19 (cont)	NES	One lamp that indicates a Non-Existent Sector address has been commanded. This bit is present as long as an illegal sector address resides in the SAR.
	EOP	One lamp that indicates the End Of Pack point has been reached before the word count is complete.
	SUSI	One lamp that indicates a Selected Unit Seek Incomplete error has occurred due to 100 ms passing while unsuccessfully seeking a particular cylinder address.
	SUFU	One lamp that indicates a Selected Unit File Unsafe signal has been received from the selected RP02.
20	SHIFT REGISTER SR00-35	Thirty-six indicators that light on binary 1's showing the contents of the Shift Register in the RP15. This register assembles serial data from the disk or serializes the data being transferred to the disk.
21	LONGITUDINAL PARITY REGISTER LPR00-35	Thirty-six indicators that light on binary 1s showing the contents of the LPR in the RP15. This register accumulates bit position odd parity for each sector.

Table 2-2
RP15 Controls

Index No.	Name	Function
22	FORMAT/NORMAL Switch	One two-position rocker switch that, in FORMAT position, enables the controller for formatting operations and, in NORMAL position, enables the controller for normal operations.
23	FORMAT/NORMAL Lamp	One lamp that lights Clear when the FORMAT/NORMAL switch is in FORMAT position.
24	LOCKOUT Switch	One two-position rocker switch that, in LOCKOUT position, enables the controller to write protect disk addresses as selected by the LO and LOA toggle switches. The unmarked position is normal for "no lockout" condition.
25	LOCKOUT Lamp	One lamp that lights Red when the LOCKOUT switch is in LOCKOUT position.
26	LOA 00-02 Switches	Three toggle switches that determine the cylinder address (in octal) in or below which writing may not occur on the unit designated by the LO switches.

Table 2-2 (Cont)
RP15 Controls

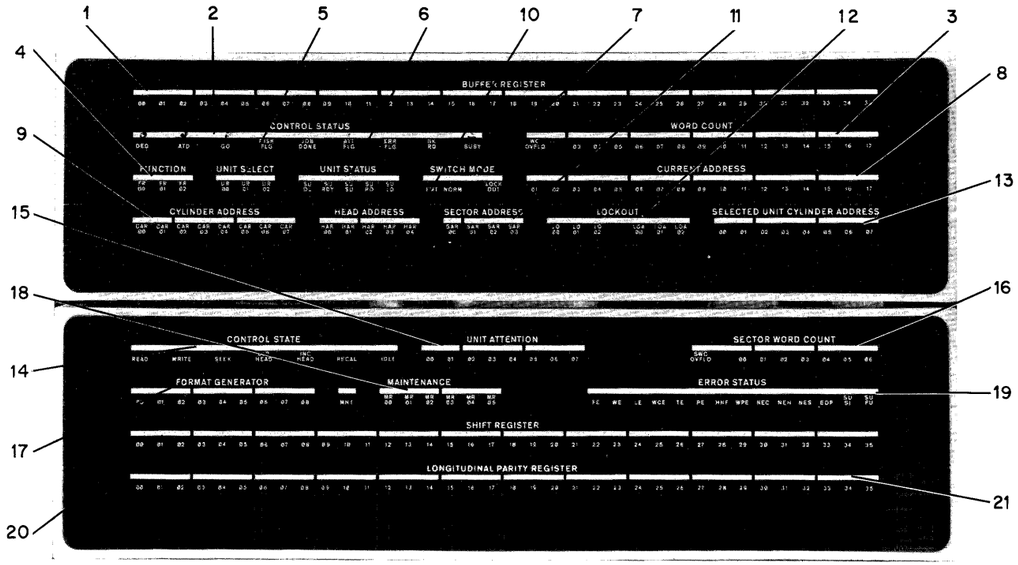
Index No.	Name	Function
27	LO 00-02 Switches	Three toggle switches that determine the unit (0-7) on which the LOA switches are applicable.

Table 2-3
RP02 Indicators

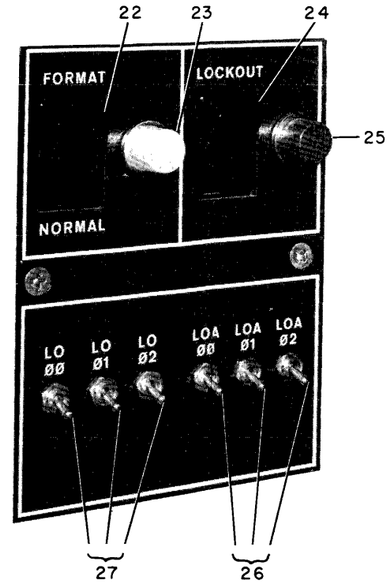
Index No.	Name	Function
28	Unit Number/Ready Indicator 0-7	One static indicator that shows the unit address of the disk pack which has been determined by its position on the bus. The number displayed can be manually changed within the unit. This indicator lights Green when the drive has reached operational speed and the heads are positioned to track 000 on the initial load operation. The indicator goes off when the STOP switch is depressed or when system power is removed.
29	128, 64, 32, 16, 8, 4, 2, 1 (Access Position)	Eight indicators that show the cylinder to which the heads have been positioned.
30	FILE UNSAFE Indicator	One indicator that lights Red when an unsafe condition exists in the RP02 Drive. Manual intervention is required to clear the condition. Placing the START/STOP switch in the STOP position resets the indicator.
31	READ ONLY Indicator	One indicator that lights Clear when the READ WRITE/READ ONLY switch is in the READ ONLY position and extinguishes when the switch is in the READ WRITE position. NOTE This light only indicates the position of the switch and is not necessarily an indication of whether or not the drive is write protected. (Refer to Table 2-4 under READ WRITE/READ ONLY switch.)

Table 2-4
RP02 Controls

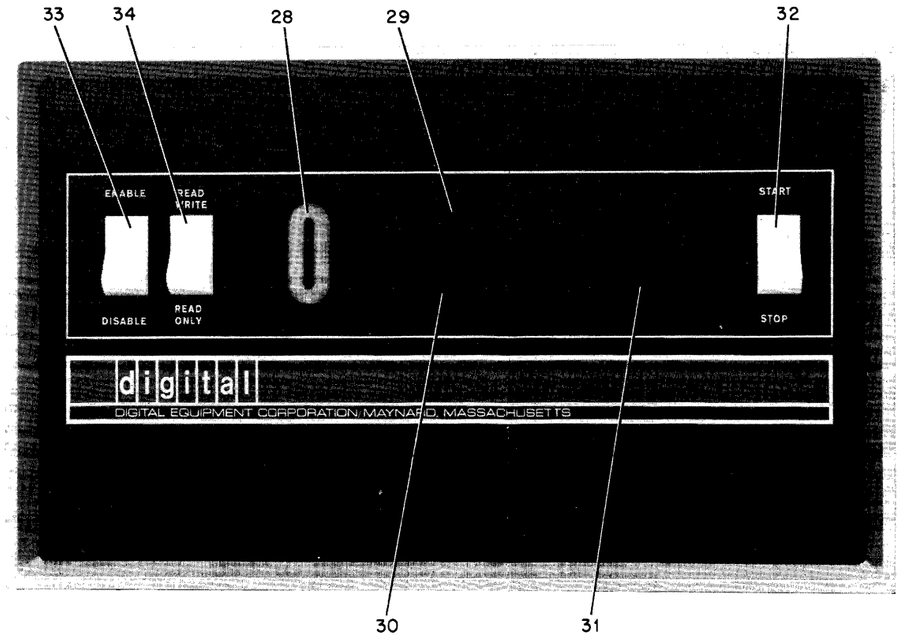
Index No.	Name	Function
32	START/STOP Switch	One two-position rocker switch that in START position applies power to the drive motor if the main power switch to the unit is on, a pack has been loaded, and the cover is closed. When the disk pack speed is greater than 1700 rpm, and the pack stabilization delay of 60 seconds has expired, it loads the heads and positions them to cylinder 000. In STOP position, power is removed from the drive, the heads are retracted, and dynamic braking stops the spindle within 12 seconds.
33	ENABLE/DISABLE Switch	One two-position rocker switch that in the ENABLE position places the RP02 on-line. When in the DISABLE position, the RP02 is still on-line until the unit has been deselected by the RP15. When the RP02 has been deselected with the switch in the DISABLE position, the unit is off-line and will remain off-line (even if reselected) until the switch is placed in the ENABLE position.
34	READ WRITE/READ ONLY Switch	One two-position rocker switch whose mechanical position enables initialization of two possible modes, when that unit is selected by the RP15, but has no control over changing the mode until that unit is once again deselected by the RP15. NOTE Because of the above, the switch could be in the READ ONLY position with the READ ONLY indicator on, but if the unit had not been deselected from a Read/Write mode, it would still be Read/Write enabled and vice versa.



a. RP15 Panel Indicators



b. RP15 Switch Panel



c. RP02 Panel

Figure 2-1 RP15/02 Controls and Indicators

2.3 OPERATING PROCEDURES

In Normal operation, the FORMAT/NORMAL switch on the RP15 switch panel is put in the NORMAL position (see Figure 2-1). In the RP02, the ENABLE/DISABLE switch is put in the ENABLE position, the READ WRITE/READ ONLY switch is put in the READ WRITE position, and the START/STOP switch is set to START (see Figure 2-1).

NOTE

The RP02 START/STOP switch should be left in STOP position until an RP02P disk pack is loaded and the cover closed.

2.3.1 Loading

To load an RP02P Disk Pack on the RP02 Disk Pack Drive, proceed as follows:

Step	Procedure
1	Put the START/STOP switch in the STOP position.
2	Hold the disk pack, enclosed in its plastic container, by the top handle; rotate the bottom cover latch and remove.
	NOTE The disk pack will remain attached to top cover.
3	Raise the cover on the drive and lower the pack, with its cover attached, into the well provided, until the pack sits on its conical hub.
4	Rotate the top cover latch clockwise until the pack is properly seated and secure.
	CAUTION Do not overtighten; merely make it snug.
5	Rotate the top cover latch in the opposite direction, while lifting the plastic cover out of the well.
6	Return top and bottom covers to storage.
7	Close the lid on the drive and place the START/STOP switch in the START position.

2.3.2 Unloading

To unload an RP02P Disk Pack from the RP02 Disk Pack Drive, proceed as follows:

Step	Procedure
1	Put the START/STOP switch in the STOP position.
2	Wait for the automatic brakes to stop the drive. When stopped, raise the lid on the drive.
	NOTE If the lid is opened when the drive is powered, power is automatically removed and braking action is applied.
3	Remove the plastic top cover from the bottom cover and lower the top cover into the well over the disk pack.
4	Once it is seated, rotate the top cover latch counterclockwise until a clicking sound occurs.
5	Lift the pack out of the well.
6	Holding the bottom cover ready on the palm of the left hand, place the cover and pack assembly firmly on its bottom cover.
7	Rotate the bottom cover latch until snug and return the encased disk pack to storage.
8	Close the cover on the disk pack drive.

2.3.3 Storage

Store the RP02P Disk Pack in its plastic container in the same ambient conditions as prevail at the drive.

2.4 SPECIAL OPERATING PROCEDURES

The RP15 can be operated under special conditions as described below.

2.4.1 Write Protection

To write protect any disk pack, proceed as follows:

Step	Procedure
1	To read only from an entire disk pack, place the READ WRITE/ READ ONLY switch on the disk pack drive in READ ONLY position.

(continued on Page 2-13)

Step	Procedure
2	To write protect only a certain block of addresses, set the READ WRITE/READ ONLY switch on the disk pack drive to READ WRITE position. On the RP15 switch panel, place the LOCKOUT switch in LOCKOUT position, set the LO toggle switches to the octal equivalent of the RP02 unit number, and set the LOA toggle switches to correspond to the upper cylinder address limit desired.

2.4.2 Formatting a Disk

To format a new disk pack, refer to the Formatter Program (MAINDEC-15-D5FA-D) supplied with each system.

CHAPTER 3
PROGRAMMING

3.1 GENERAL

Programming the RP15 is predicated upon the requirements imposed by the RP02 Disk Pack. A brief summary of the file is given as an introduction to programming considerations (see Figures 3-1 and 3-2).

3.1.1 RP02 Disk Pack Structure

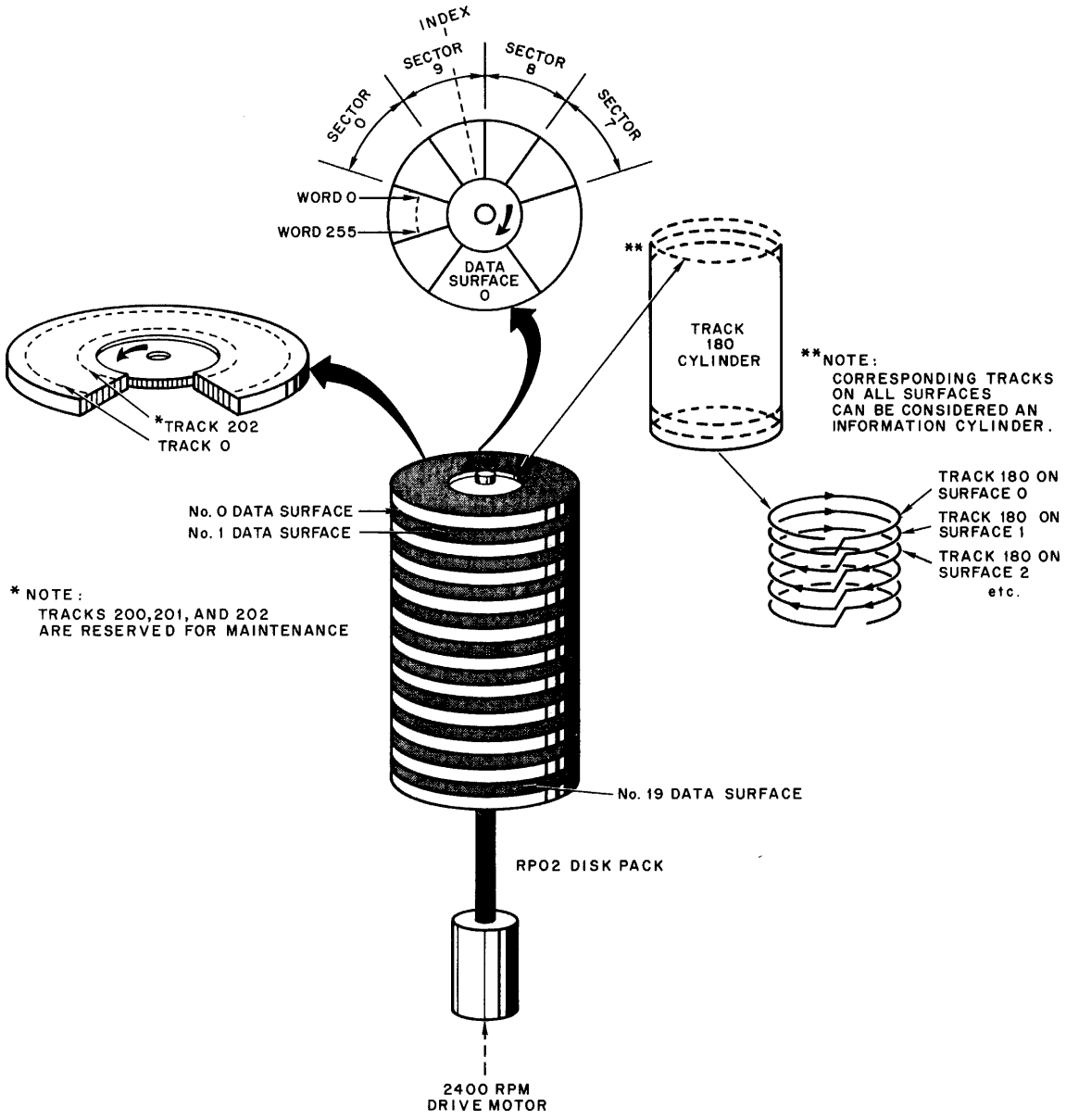
The total capacity of the RP02 Disk Pack is 232,000,000 bits, which is equivalent to 12,900,000 18-bit words. In actual practice, the two outside surfaces are not used; on all surfaces, tracks 200, 201, and 202 are reserved for maintenance. When these conditions are recognized, along with the data required for two synchronization areas, word and longitudinal parity, and a header word for each sector, the relative characteristics (as called out in the Summary on Figure 3-1) yield a total data word capacity of 10,240,000 18-bit words.

In the RP02, each disk contains 203 cylinders. Movable heads, connected to a common positioning actuator, access one cylinder at a time. Track-to-track, average, and maximum positioning times are 20, 50, and 80 ms, respectively. Rotation speed is 2400 rpm (or a rotational time of 25 ms), providing average and maximum latency times of 12.5 and 25 ms, respectively. Data are recorded by a double frequency, non-return-to-zero technique. Data are formatted into 128 36-bit word sectors that are individually addressable; each word provides storage space for two 18-bit PDP-15 words.

The RP02 has 20 read/write heads that record data at 2.5M bps. Recording densities are 1530 bpi for track 000 and 2228 bpi for track 202. Each RP02 track contains 10 sectors. Word transfer rate is 14.8 μs for each 36-bit word or 7.4 μs for each 18-bit PDP-15 processor word.

Data formats for information recorded on the disks are arranged as shown in Figure 3-2. These consist of a 30-word "preamble", a one-word header, a four-word data sync area, a data field of 128 36-bit words, followed by a two-word tail or "postamble".

The preamble or VFO sync area comprises 1109_{10} "zeros". This area is written by the control during Write All Format mode and provides the time necessary for the VFO circuit to determine the nominal



SUMMARY

11 DISKS
20 DATA SURFACES
4000 TRACKS
40,000 SECTORS
10,240,000 18-BIT WORDS

WORDS PER SECTOR	X	SECTORS PER TRACK	=	WORDS PER TRACK	X	TRACKS PER SURFACE	=	WORDS PER SURFACE	X	SURFACES PER PACK	=	WORDS PER PACK
256		10		2560		200		512,000		20		10,240,000

09-0343

Figure 3-1 RP02 Disk Pack Structure

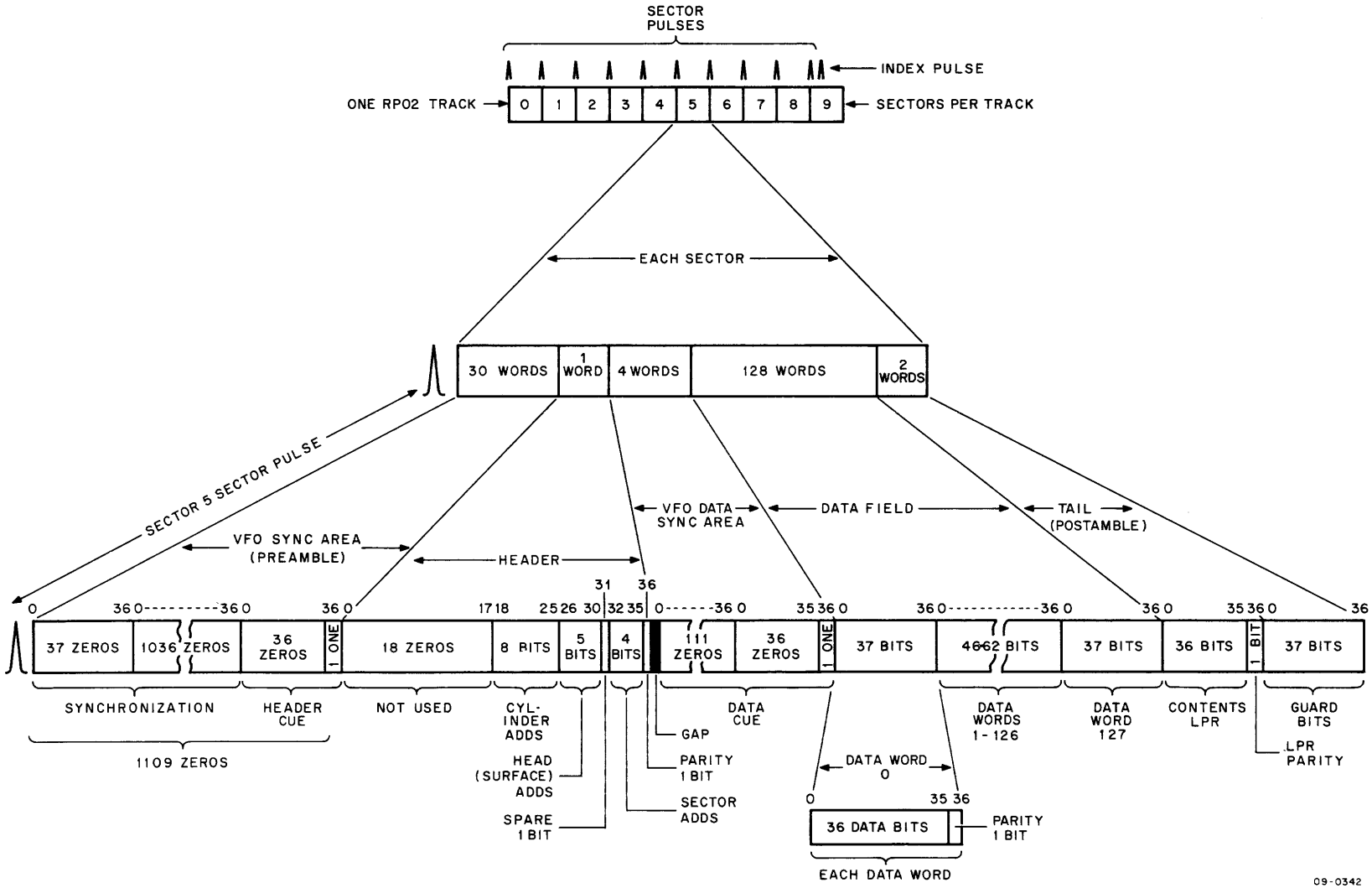


Figure 3-2 RP02 Format for RP15 Controller

disk pack density (frequency) during Read functions and to lock in on that frequency. The preamble area is followed by a 1 bit that cues the controller that the header word follows.

The header is a one-word field. In the RP15 system, the first 18 bits are not used but are filled in with zeros. The second half is used for addressing; bits 18-25 contain the cylinder address to which the heads are to be slewed, bits 26-30 designate the head to be enabled (surface address), and bits 32-35 provide the sector address. Bit 36 is a parity bit generated by the control at format time; bit 31 is wired as a spare for possible address expansion. The purpose of the header is to locate the desired sector by comparing the cylinder, head, and sector address, as read from the header on the disk, with the cylinder, head, and sector address deposited in their respective registers within the control.

The header field is followed by a gap provided for turning off the Read function and turning on the Write function. This area is ignored by the controller since its contents are indeterminate.

The third field is the VFO Data Sync Area that contains four words of zeros, with the last bit of the fourth word set to a 1. This area cues the control that the data field follows and also gives the VFO time to re-sync after the gap.

The fourth (data) field contains 128 36-bit words, with each word followed by an odd parity bit (word parity).

NOTE

Each 36-bit word transferred between controller and disk comprises two 18-bit words (256) when transferred between processor and controller. This controller only checks 36-bit word parity.

The fifth and last field, called the tail or "postamble", contains two 37-bit words. The first word contains 36 bits of odd longitudinal parity, accumulated for each significant bit of the data field, followed by its own word parity. The second word contains 37 indeterminate guard bits that serve to disable write current, without destroying the longitudinal parity word.

3.1.2 IOT Selection

A device selection code (63 or 64) from the PDP-15 provides the basic activating signal to the RP15 Disk Pack Controller's logic. Sensing of the device selection code by the logic circuits enables the receipt of IOP pulses from which the IOT pulses are internally generated to control operation of the disk pack. The functions of the IOT pulses are listed in Table 3-1.

NOTE

In systems requiring more than one RP15 Controller, the system is easily modified by wiring changes to accommodate the second controller with two other available Device Select Codes.

Table 3-1
Disk Pack IOT Instructions

Mnemonic Symbol	Octal Code	Operation Executed
DPSF	706301	Skip on DISK flag. Skip the following instruction if either the JOB DONE, ATTENTION, or ERROR flags are set.
DPOSA	706302	OR Status Register A into the AC.
DPRSA	706312	Read Status Register A into the AC.
DPLA	706304	Load the Cylinder Address Register from AC 0-7 (000_8 through 312_8 are legal). Load the Head Address Register from AC 8-12 (00_8 through 23_8 are legal). Load the Sector Address Register from AC 14-17 (0_8 through 11_8 are legal).
DPSA	706321	Skip on ATTENTION flag.
DPOSB	706322	OR Status Register B into the AC.
DPRSB	706332	Read Status Register B into the AC.
DPCS	706324	Clear the Status bits for Format Error, Word Parity Error, Longitudinal Parity Error, Write Check Error, Timing Error, Programming Error, Header Not Found, and End of Pack.
DPSJ	706341	Skip the following instruction if the JOB DONE flag is set.
DPOM	706342	OR the Maintenance Register into the AC.
DPRM	706352	Read the Maintenance Register into AC 0-5. Clear AC 6-17.
DPCA	706344	Load the Current Address Register from AC0-17.
DPSE	706361	Skip the following instruction if an error condition is present.
DPWC	706364	Load the 2's complement of the word count, contained in the AC, into the Word Count Register.
DPEM	706401	Execute the maintenance instructions as defined by AC 9-17 (refer to Table 3-2).
DPLM	706411	Clear the AC and leave maintenance mode.
DPOU	706402	OR the Selected Unit Cylinder Address Register into the AC 10-17.
DPRU	706412	Read the Selected Unit Cylinder Address Register into the AC 10-17.
DPCF †	706404	Clear the Function Register. Select Unit 0. Set Idle mode. Disable all interrupts. Set control to power clear state.

†After these instructions, another RP15 instruction should not occur for a minimum of 4 μs.

Table 3-1 (Cont)
Disk Pack IOT Instructions

Mnemonic Symbol	Octal Code	Operation Executed
DPSN	706421	Skip the following instruction if FORMAT/NORMAL switch is in NORMAL position.
DPOA	706422	OR the Cylinder, Head, and Sector Address Registers into the AC.
DPRA	706432	Read the Cylinder, Head, and Sector Address Registers into the AC.
DPLZ†	706424	Load the Accumulator zeros into Status Register A and execute bits 0-8 if GO bit is set (see Table 3-3).††
DPOC	706442	OR the Current Address Register into the AC.
DPRC	706452	Read the Current Address Register into the AC.
DPLO†	706444	Load the Accumulator 1's into Status Register A and execute bits 0-8 if GO bit is set (see Table 3-3††).
DPCN†	706454	Equivalent to a continue command. Clear the AC. Execute the Function Register. The FR is unchanged.††
DPOW	706462	OR the Word Count Register into the AC.
DPRW	706472	Read the Word Count Register into the AC.
DPLF†	706464	Load Status Register A from AC 0-8. Execute the new contents if the GO bit is set at completion of DPLF.

†After these instructions, another RP15 instruction should not occur for a minimum of 4 μs.

††When a DPLZ is issued with accumulator bits 0-8 equal to ones, the effect is the same as DPCN, with the exception that the accumulator is unchanged. Also, when a DPLO is issued, with accumulator bits 0-8 equal to zeros, the effect is the same as DPCN, with the exception that the accumulator is unchanged (refer to Table 3-3).

Table 3-2
AC Bit Assignment when Included in DPEM

Bit	Description
09	Load the Maintenance Register from AC bits 12-17 of this word. AC bits 10 and 11 are ineffective when bit 09 is set. AC bits 12-17 are interpreted as data to be loaded into the six bit Maintenance Register.
10	Enter maintenance mode and interpret AC bits 11-17 as follows: (effective only when AC bit 09 is cleared).
11	Issue a maintenance Selected Unit Index Pulse.

Table 3-2 (Cont)
AC Bit Assignment when Included in DPEM

Bit	Description
12	Issue a maintenance Selected Unit Sector Pulse.
13	Maintenance set JOB DONE.
14	Increment the Current Address Register.
15	Increment the Word Count Register.
16	Increment the Sector Address Register (overflow of SAR increments HAR, overflow of HAR increments CAR).
17	In a Read operation, one bit of data is transferred from the Maintenance Register to the Shift Register. In a Write operation, one bit of data is transferred from the Shift Register to the Maintenance Register. This instruction simulates one bit cell of data transfer through the same logic paths as normal data.

Table 3-3 explains the operation of the DPLO and DPLZ instructions in Truth Table form.

Table 3-3
DPLO and DPLZ Truth Tables

DPLO					DPLZ				
AC 0-8	1 V	SRA 0-8		SRA 0-8	AC 0-8	0 V	SRA 0-8		SRA 0-8
0	+	0	=	0	0	+	0	=	0
0	+	1	=	1	0	+	1	=	0
1	+	0	=	1	1	+	0	=	0
1	+	1	=	1	1	+	1	=	1

Note: SRA = Status Register A.

3.1.3 RP15 Status Facility

The RP15 DISK flag appears on bit 12 of the PDP-15 IORS Register. Status conditions may be checked readily by observing certain lights on the RP15 indicator board. While operating the RP15, the interaction of the various conditions which raise these flags should be kept in mind, so that no confusion will result as to what caused the flags to be raised.

In the RP15, there are two status registers designated Status Register A and Status Register B (see Figures 3-3 and 3-4, respectively). Table 3-4 relates bit position for each Status Register to the type of status indicated.

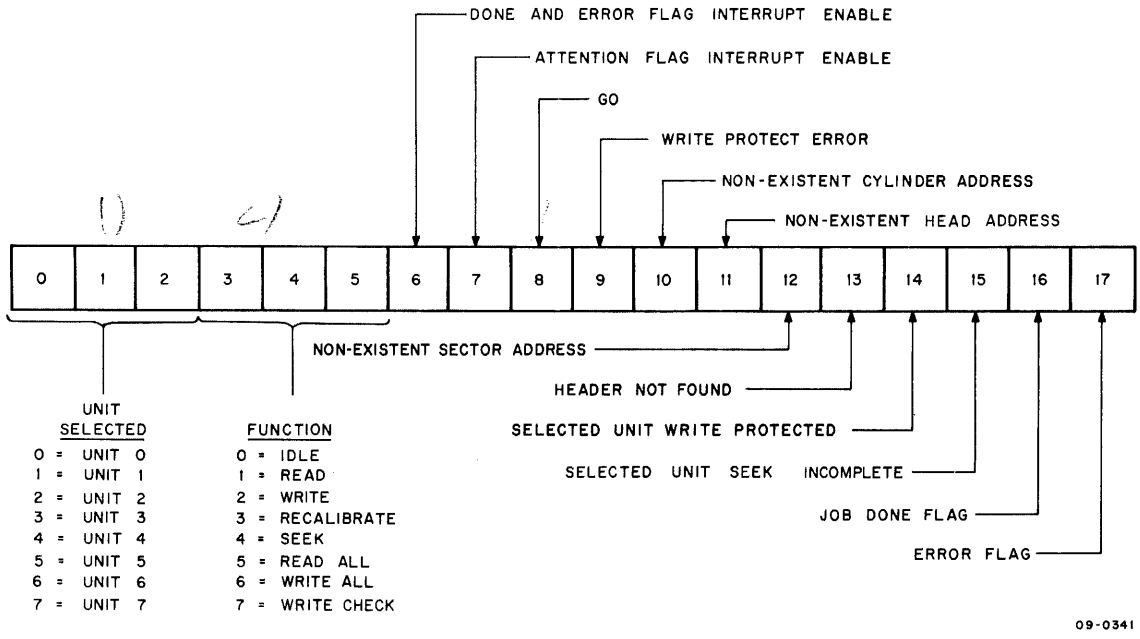


Figure 3-3 RP15 Status Register A Bit Assignment

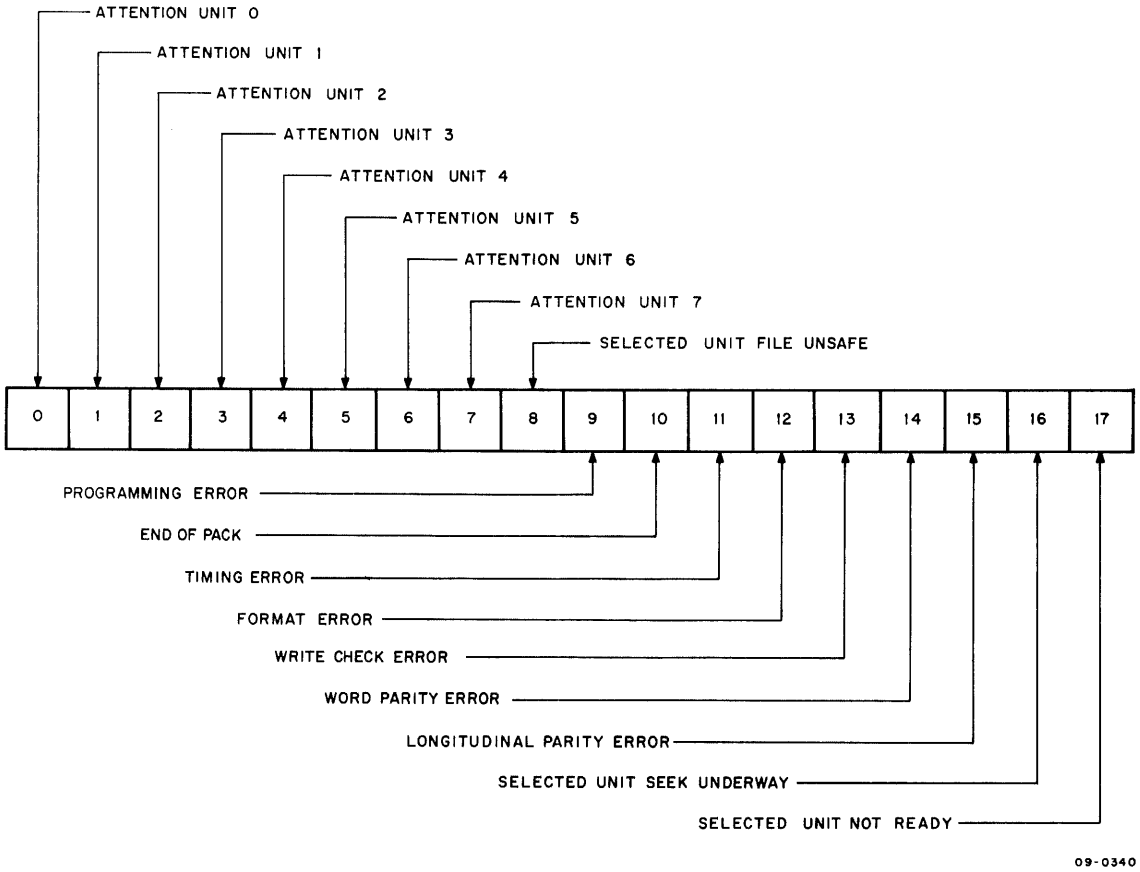


Figure 3-4 RP15 Status Register B Bit Assignment

Table 3-4
Status Register Bit Assignments

Bits Assigned	Status Reg.		Status Type					ORed for Disk Flg
	A	B	Error	Sel. Unit	Attn.	Int.	Func.	
0	x			x				
1	x			x				
2	x			x				
3	x						x	
4	x						x	
5	x						x	
6	x					x		
7	x					x		
8	x						x	
9	x		x					x
10	x		x					x
11	x		x					x
12	x		x					x
13	x		x					x
14	x			x				
15	x		x	x	x			x
16	x					x		x
17	x		x			x		x
0		x			x			x
1		x			x			x
2		x			x			x
3		x			x			x
4		x			x			x
5		x			x			x
6		x			x			x
7		x			x			x
8		x	x	x				x
9		x	x					x
10		x	x					x
11		x	x					x
12		x	x					x
13		x	x					x
14		x	x					x

Table 3-4 (Cont)
Status Register Bit Assignments

Bits Assigned	Status Reg.		Status Type					ORed for Disk Flg.
	A	B	Error	Sel. Unit	Attn.	Int.	Func.	
15		x	x					x
16		x		x				
17		x		x	x			

There are five status categories:

a. Error Status

b. Selected Unit Status

c. Attention Status

d. Interrupt Status

e. Function Status.

The fourteen types of Error Status are:

a. Format Error (Bit 12 of Register B) - The header word in each sector is parity checked when read. A parity error in the header word raises the format error status bit. Bit 17 of Register A is also raised.

b. Word Parity Error (Bit 14 of Register B) - Each word in the data field is parity checked while reading. A word parity error raises the word error status bit. Bit 17 of Register A is also raised.

c. Longitudinal Parity Error (Bit 15 of Register B) - Longitudinal parity is computed for each bit position of the data field. Errors that occur in longitudinal parity, while reading the data field, result in a longitudinal error status bit. Bit 17 of Register A is also raised.

d. Write Check Error (Bit 13 of Register B) - Errors that occur in the comparison of data words during a write check function result in a write check error status bit. Bit 17 of Register A is also raised.

e. Timing Error (Bit 11 of Register B) - Timing error status bit results from a missed data transfer between the PDP-15 and the RP15. The RP15 should be placed physically first on the positive I/O bus string to avoid this condition.

f. Programming Error (Bit 09 of Register B) - There are three programming conditions that must be avoided in the RP15. When the RP15 is BUSY, the following instructions are illegal:

DPLZ	DPCN (or any instruction which simulates continue)
DPWC	DPCA
DPLO	DPLF
DPLA	DPCS

BUSY is defined either as 1. the time from the completion of a DPLZ, DPLO, DPCN, or a DPLF and 4 μs later, if the function is an initiate type, i.e., Idle, Recalibrate, or Seek; or 2. the time from the completion of a DPLZ, DPLO, DPCN, or DPLF until the JOB DONE flag is raised, if the function is an execute type, i.e., Read, Write, Read All, Write All, or Write Check. A violation of these conditions results in a programming

error, the illegal instructions are not executed, and Bit 17 of Register A is raised. There is a third programming condition that does not raise a programming error and therefore should be avoided. Following a DPLF, DPLZ, DPLO, DPCN (or any instruction which simulates a continue), or DPCF, another RP15 instruction should not occur for a minimum of 4 μs (RP15 instructions are those with device code 63 or 64).

g. Header Not Found Error (Bit 13 of Register A) - The Header Not Found is a status bit that is raised when the disk has made a minimum of one revolution while searching for a header word and has been unsuccessful in finding that word. Bit 17 of Register A is also raised.

h. Write Protect Error (Bit 9 of Register A) - Write Protect Error is a status bit that is raised when a Write function is requested whose target is either in a Selected Unit Read Only mode or has been Selected Unit Lockout designated. Bit 17 of Register A is also raised.

i. Non-Existent Cylinder Address Error (Bit 10 of Register A) - This status bit is raised when the Cylinder Address Register is loaded with an illegal address (313_8 through 377_8). It remains set until the illegal address is cleared. Bit 17 of Register A is also set.

j. Non-Existent Head Address Error (Bit 11 of Register A) - This status bit is raised when the Head Address Register is loaded with an illegal address (24_8 through 37_8). It remains set until the illegal address is cleared. Bit 17 of Register A is also raised.

k. Non-Existent Sector Address Error (Bit 12 of Register A) - This status bit is raised when the Sector Address Register is loaded with an illegal address (12_8 through 17_8). It remains set until the illegal address is cleared. Bit 17 of Register A is also set.

l. End of Pack Error (Bit 10 of Register B) - To the controller, each disk pack (or unit) appears as a continuous chain of sectors starting with cylinder 000_8, head 00_8, and sector 00_8; continuing to cylinder 312_8, head 23_8, and sector 11_8. When a data transfer exceeds the upper limit before the word count has reached overflow, the JOB DONE flag (bit 16 of Register A) is set and the END OF PACK flag is raised. Bit 17 of Register A is also raised.

m. Selected Unit Seek Incomplete Error (Bit 15 of Register A) - Selected Unit Seek Incomplete is a status bit that is raised when 100 ms have passed since a Seek was issued and the desired cylinder has not been found. Also, Bit 17 of Register A and the appropriate attention bit in Status Register B are raised.

n. Selected Unit File Unsafe Error (Bit 8 of Register B) - Selected Unit File Unsafe is a status bit that is raised to indicate that a hardware failure has occurred in the selected unit. Bit 17 of Register A is also raised.

The five types of Selected Unit Status are:

a. Selected Unit Cylinder Address Status - An 8-bit register called Selected Unit Cylinder Address, which can be read into the accumulator, indicates the current position of the heads in the unit presently selected. This is allowed only when the RP15 is not busy and the unit being interrogated is not presently executing a previously given command. This is feasible when more than one RP02 is controlled by the same RP15.

b. Selected Unit On-Line Status - This bit indicates that power has been applied to the unit selected and that the heads are loaded. This bit can only be read from the indicator panel.

c. Selected Unit Not Ready Status (Bit 17 of Register B) - SELECTED UNIT READY is raised when the selected unit has successfully completed a Seek. The "not-ready" condition, however, raises the status bit.

d. Selected Unit Seek Underway Status (Bit 16 of Register B) - This bit indicates that the selected unit is in the process of seeking.

e. Selected Unit Write Protected (Bit 14 of Register A) - This bit indicates that the selected unit is "read-only" protected, or that the Unit Register is equal to the Lockout Register (UR = LO), the lockout switch is in the LOCKOUT position, and the Cylinder Address Register is equal to or less than the LOA register (CAR $\leq$ LOA).

The two types of Attention Status, indicated by bits 0-7 of Register B, designate the selected unit which raised the ATTENTION flag. They are indicated by the following:

a. Bit 17 of Register B, cleared when the unit has successfully completed a Seek, indicating selected unit ready.

b. Bit 15 of Register A, raised when the unit has unsuccessfully completed a seek, indicating selected unit seek incomplete.

For Interrupt Status, the RP15 provides one flag that raises program or automatic priority interrupt requests (PI or API Interrupt Facility). This flag is called the DISK flag. The DISK flag operates on API level 1 and port address 64. It is conditioned by the OR of the three sub-flags (JOB DONE, ERROR, and ATTENTION) and their interrupt enables (ATTENTION INTERRUPT, and JOB DONE/ ERROR INTERRUPT). These are described as follows:

a. Job Done Flag Status (Bit 16 of Register A) - The JOB DONE flag is raised when

   (1) an execute type function has been successfully completed or

   (2) an execute type function has been aborted as a result of an error condition.

b. Error Flag Status (Bit 17 of Register A) - The ERROR flag is an OR condition of all the error status conditions previously described.

c. Attention Flag Status (Bits 0-7 of Register B) - The ATTENTION flag is an OR condition of attention bits 0 through 7 in Status Register B.

d. Attention Interrupt Enable Status (Bit 7 of Register A) - Attention Interrupt Enable is a status bit that can be loaded with a DPLO, or DPLF instruction. When this bit is set, the ATTENTION flag is enabled for the interrupt system.

e. Job Done and Error Interrupt Enable Status (Bit 6 of Register A) - The Job Done and Error Interrupt Enable status bit can be loaded with a DPLO, or DPLF instruction. When this bit is set, the JOB DONE flag and the ERROR flag are enabled for the interrupt system.

3.2 SEQUENCE OF OPERATION

3.2.1 Write Function

To transfer data from the PDP-15 Memory to the RP02 Disk Pack, a Write function must be executed (see Figure 3-5). This is done by loading the RP15 Word Count Register with the 2's complement of the number of words to be written on the disk; then loading the RP15 Cylinder, Head, and Sector Address Registers with the location of the disk at which it is to be written. Next, the initial address in memory of the data to be transferred is loaded in the Current Address Register. The ATTENTION INTERRUPT ENABLE and JOB DONE/ERROR INTERRUPT ENABLE are also set, depending on the type

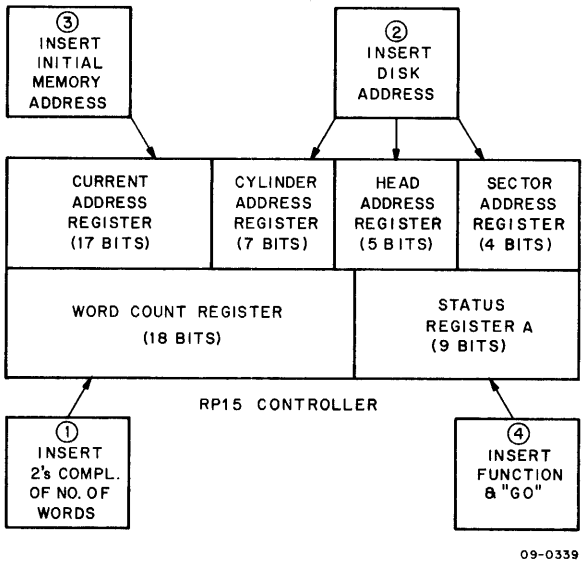


Figure 3-5 Insert and Execute Phase

of interrupt service desired. Finally, the 3-bit octal code of the unit to be used, the 3-bit code of the function to be performed (Write), and the GO bit are set in Status Register A bits 0-8. This provides the GO signal to the RP15, instructing the controller to:

a. Write the number of words, specified by the Word Count, from memory, starting with the initial memory address, which is specified by the Current Address Register, onto the disk at the location specified by the Cylinder, Head, and Sector Address Registers.

b. When it is accomplished, raise the JOB DONE flag.

c. If any errors are encountered in the process, raise the appropriate error flag and shut down.

NOTE

When loading the function and unit registers with a DPLF, if it is desired to inspect the selected unit status before the function is executed, the GO bit (bit 8 of Status Register A) may be left unset. Then, when ready, the GO bit can be set by the DPLO instruction, at whict time the RP15 will begin executing the instruction.

When the function is loaded and the GO bit set, an 18-bit word is taken from memory and parallel-transferred through the I/O bus to the RP15 Buffer Register, where it enters bits 18-35 (see Figure 3-6). This is designated the "B" half of the Buffer Register. A request is issued for another 18-bit word, while the first word is shifted to Buffer Register "A" (bits 0-17), and the second word is loaded into bits 18-35. Each 18-bit word transferred from memory into Buffer Register "B" increments the Word Count and Current Address Registers.

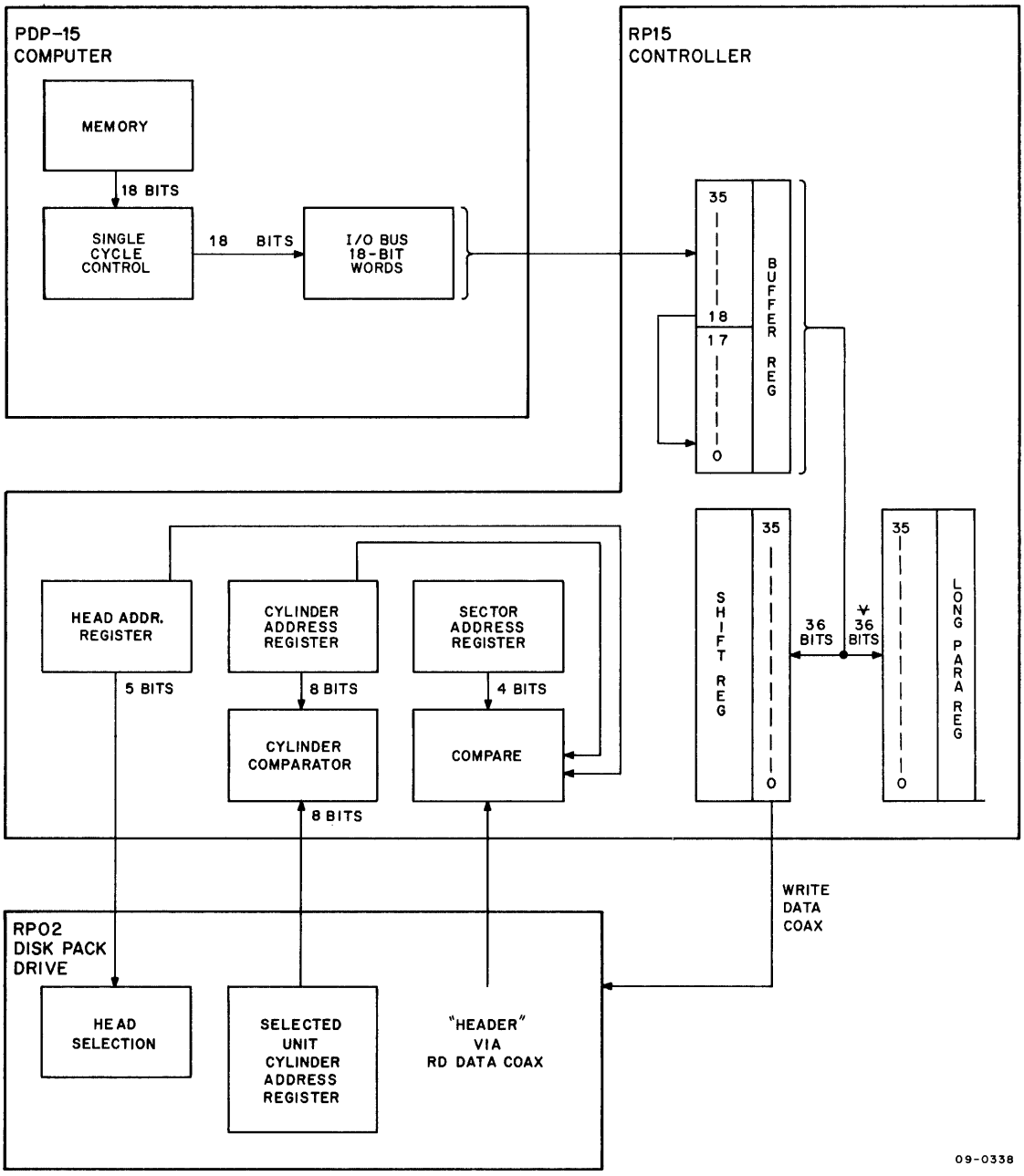


Figure 3-6 WRITE Function, SEEK State

During the time that data are being assembled from memory, a disk address comparison is made to determine if the heads require moving to another cylinder. A cylinder comparator within the RP15 looks at the Selected Unit Cylinder Address Register and checks it against its own Cylinder Address Register to determine if a change is required and in what direction. If they do not compare, a Seek function is performed until comparison is reached, at which time the RP02 sends back an "attention" signal indicating that the heads are now positioned in the proper cylinder.

On receipt of "attention", the proper head is selected by the Head Address Register, into which the desired address was previously loaded. This enables the head to begin reading header words from the disk.

NOTE

Although a Write function is being executed, the Read state must be enabled to find the proper sector.

The proper sector is found by sensing sector pulses that come from a notched arrangement on the bottom of each disk pack. These pulses are the only means of timing sent back from the disk. When the sector pulse is received, the controller reads the preamble synchronization field of zeros which is used to lock in a phase-locked VFO within the RP15. This is followed by a "cue" bit (1) to signal the beginning of the header. As the header is read, it is compared with the desired address previously inserted in the RP15. If it does not compare, the process repeats on succeeding sector pulses until comparison is found, at which time the controller readies itself to begin writing following the header word.

When the header is read, and during the gap period, the Read winding in the head is disabled and the Write winding is enabled. The controller then writes the post-header sync area consisting of 147_{10} bits of zeros followed by a 1 bit. At this time, the 36 bits assembled in the Buffer Register are parallel-transferred into the Shift Register and then XORed into the Longitudinal Parity Register (LPR) from the Shift Register (see Figure 3-7). The 36 bits are then serially shifted (from bit 36 to bit 0) out onto the disk.

As these bits are shifted out, each 1 bit complements a parity generator. As the last bit is shifted out, the resultant odd parity bit for that word is put on the disk in the 37th bit position and the cycle repeats.

The next two data words, already loaded in the Buffer Register, load the Shift Register in two 18-bit bytes, are XORed into the LPR, and are also shifted out onto the disk in a steady flow of 128 36-bit words. At that time, the odd parity contents of the LPR (accumulated XOR of all 128 36-bit words, bit-for-bit) are transferred into the Shift Register and then out onto the disk as the 129th word, passing through the Bit Generator that generates odd parity for that parity word.

If the Word Count has not as yet overflowed (more than one sector required for the entire transfer), the previous process repeats as the controller goes back into Read state, the next sequential header is compared, and the next two 18-bit data words fetched from memory are transferred. If the Word Count has overflowed, the operation is terminated and the controller is shut down.

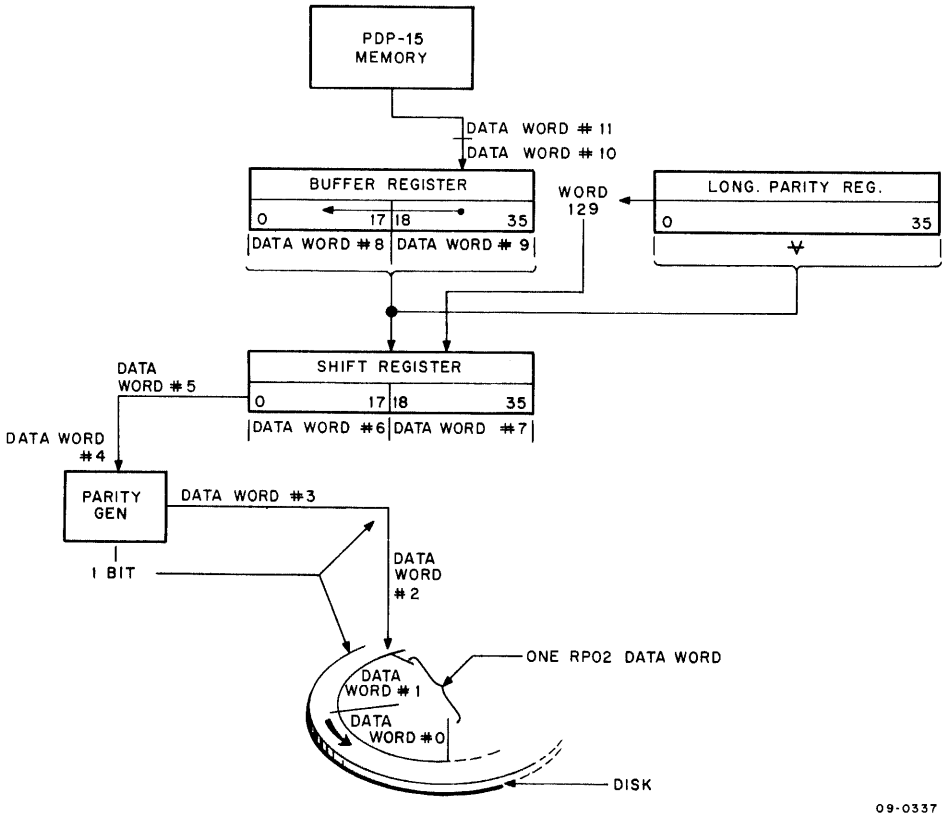


Figure 3-7 WRITE Function, Transfer/Write States

3.2.2 Read Function

To transfer data from the RP02 Disk Pack to memory, a Read function must be executed (see Figure 3-5). This is done by loading the RP15 Word Count Register with the 2's complement of the number of words to be read from disk, then loading the RP15 Cylinder, Head, and Sector Address Registers with the location on disk at which it is to be found. Next, the initial address in memory to which that data are to be transferred is loaded in the Current Address Register. The ATTENTION INTERRUPT ENABLE and JOB DONE/ERROR INTERRUPT ENABLE are also set, depending on the type of interrupt service desired. Finally, the 3-bit octal code of the unit to be used, the 3-bit octal code of the function to be performed (Read), and the GO bit are set in Status Register A bits 0-8. This provides the GO signal to the RP15, instructing the controller to

a. Read the number of words, specified by the Word Count, into memory starting with the initial memory address, which is specified by the Current Address Register, from the disk beginning at the location specified by the Cylinder, Head, and Sector Address Registers.

b. When this is done, raise the JOB DONE flag.

c. If any errors are encountered in the process, raise the appropriate error flag and shut down.

At this point, a disk address comparison is made, as described under the Write transfer sequence in Paragraph 3.2.1. Once comparison is found, the read head ignores the indeterminate information in the gap area, and is reenabled to read the data following the data "cue" bit at the end of the VFO Data Sync Area (see Figure 3-2). A 36-bit word is then read from disk, serially assembled in the Shift Register (see Figure 3-8), parallel-transferred to the Buffer Register, and XORed into the LPR to check longitudinal parity. Each 36-bit word transferred from the Shift Register to the Buffer Register increments the Sector Word Count. When memory time is granted, the word is transferred to memory as two 18-bit bytes; for each 18-bit word transferred to memory, the Word Count and Current Address Registers are incremented. Parity, Sector Word Count, and Word Count are checked in the same manner as in Write (see Paragraph 3.2.1). When Word Count overflows, the transfer is understood to be complete and the controller shuts down. Any error along the way is flagged.

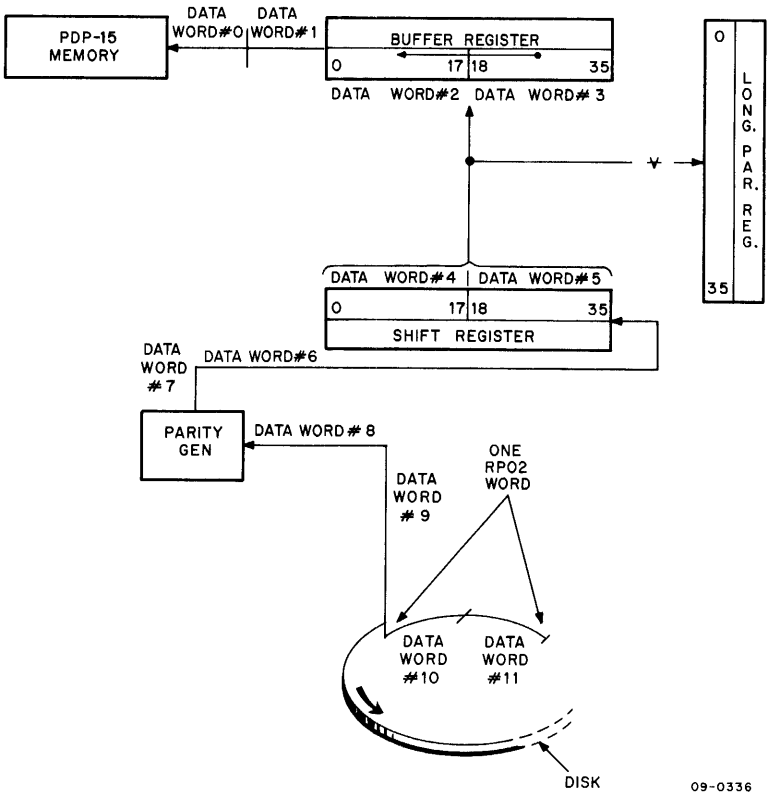


Figure 3-8 READ Function, Read/Transfer States

3.2.3 Read All Function

A Read All function is executed by first loading the RP15 Word Count Register with the 2's complement of the words to be read from the disk. In Read All, header words are read and transferred; they must be included in the word count calculation. Next, the Cylinder, Head, and Sector Address Registers of

the RP15 are loaded with one sector less than the true location on the disk at which the data are to be found. The initial address in memory to which these data are to be transferred is loaded in the RP15 Current Address Register. ATTENTION INTERRUPT ENABLE and JOB DONE/ERROR INTERRUPT ENABLE are also set, depending on the type of interrupt service desired. Finally, the 3-bit octal code of the unit to be selected, the 3-bit octal code of the function to be performed (Read All), and the GO bit are set in Status Register A bits 0-8. This provides the GO signal to the RP15, instructing the controller to,

a. Read the number of words and headers, specified by the Word Count, into memory, starting with the initial memory address, which is specified by the Current Address Register, from the disk, beginning at the location following that specified by the Cylinder, Head, and Sector Address Registers.

b. When this is done, raise the JOB DONE flag.

c. If any errors are encountered in the process, raise the appropriate error flag and shut down.

At this point, the cylinder comparator checks head positioning and, if necessary, the RP15 enters a Seek operation. Once comparison has been found, the Read state is entered. When the desired Header Address is found, a header compare is indicated; since the specified address is one less than the true address, the data field associated with the header found is ignored. Then, on receipt of the next sector pulse, the read heads are turned on and every header and data field are read until Word Count overflows. These fields are serially assembled in the Shift Register, parallel-transferred to the Buffer Register, XORed into the LPR, and transferred to memory in 18-bit bytes in the same manner as Read, except that both header and data words are transferred (see Figure 3-9).

In this function, because the address registers are loaded with one less than the true address, the method of incrementing these registers is modified. In other functions, the increment to head address is given on the sector address transition from eleven to zero, in Read All (and Write All) increment to head address is given on the ten to eleven sector address transition.

At the end of each sector, word count is checked. When overflow is indicated, transfer to memory is stopped. If this should occur in the middle of a sector, the remainder of that sector is read for parity purposes, but is not transferred to memory. At the end of that sector, the RP15 will terminate the operation. Any error along the way is flagged.

3.2.4 Write All Function

A Write All function is loaded in the same manner as a Read All function. At GO time, the decision to Seek or not is made. If a Seek is not necessary, the Read state is entered immediately. If cylinder compare is not generated, Seek is performed before entering Read.

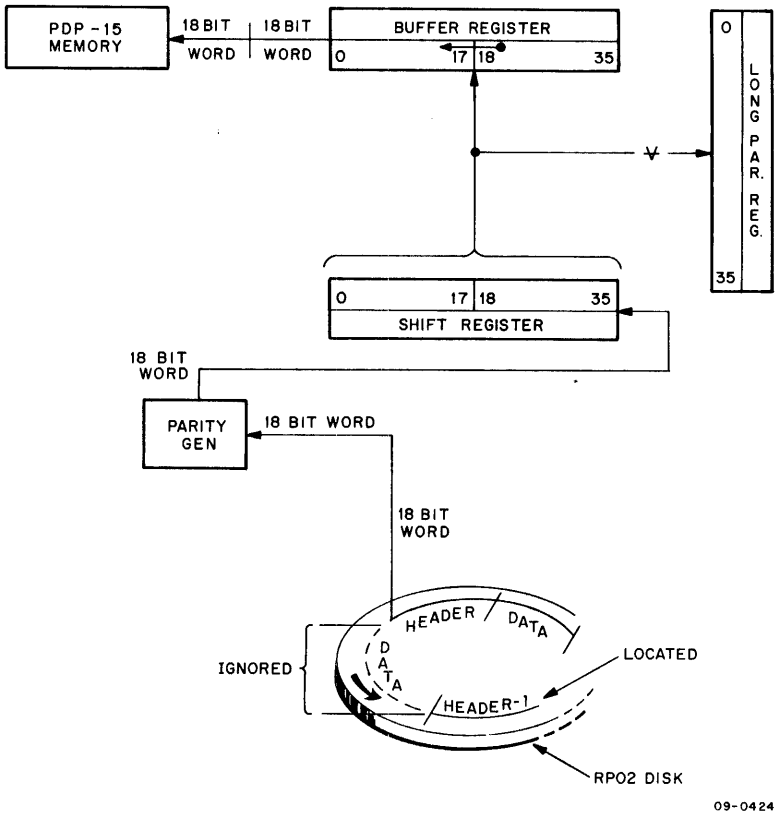


Figure 3-9 READ ALL Function, Transfer States

The Read state is entered in Write All simply to find the specified header that represents true sector address minus one (see Figure 3-10). When the header is found, the data field associated with that header is ignored but, at the next sector pulse, the RP15 enters the Write state and writes everything in that sector including pre-header sync, header, post-header sync, data field, and longitudinal parity. If, at the end of that sector, the word count has not overflowed, the controller remains in the Write state. When the next sector pulse is received, the RP15 writes another entire sector. When Word Count overflows, transfer from memory ceases. If overflow occurs in the middle of a sector, the controller will fill out that sector with zeros, for parity purposes, and then terminate.

3.2.5 Write Check Function

The Write Check function is a combination of the Write and Read functions. As far as memory is concerned, the Write Check function is identical to Write. As far as the disk is concerned, it is identical to Read.

Data words are transferred from the PDP-15 to the RP15 and, at the same time, are read from the RP02 and transferred to the RP15 (see Figure 3-11). In the RP15, the two words are compared bit-for-bit.

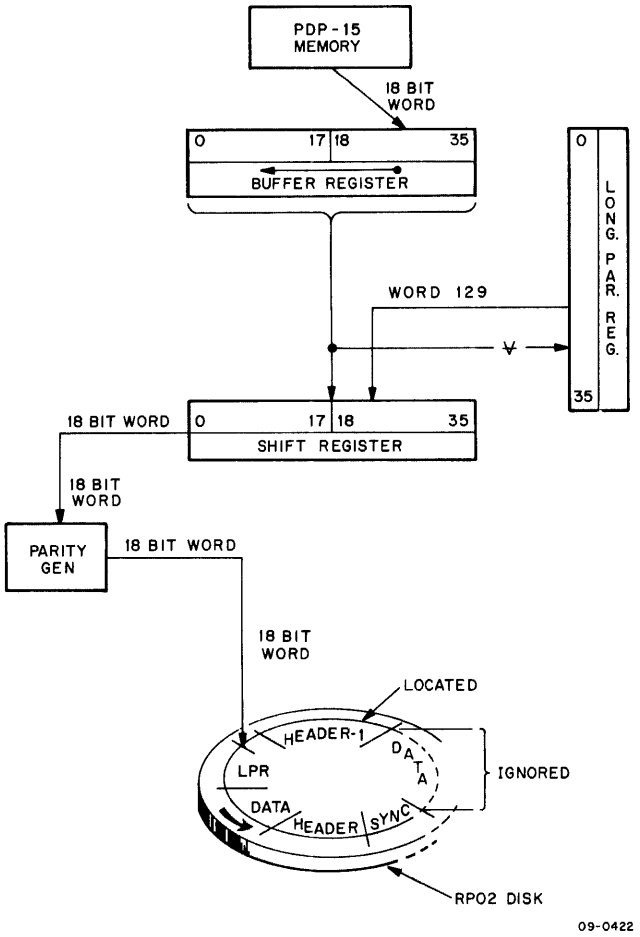


Figure 3-10 WRITE ALL Function, Transfer States

Discrepancies raise a status bit called WRITE CHECK ERROR, which results in the appropriate interrupts. Data remain unchanged in memory, as well as on the disk.

3.2.6 Idle Function

The Idle function is the no operation (NOP) state of the control and can be executed by loading its octal code into the function register. The Idle function is also entered when the PDP-15 is powered up, the I/O Reset key is depressed on the PDP-15 Console, a CAF (CLEAR ALL FLAGS) instruction is issued, or a DPCF instruction is issued.

3.2.7 Seek Function

The Seek function is executed by loading its octal code into the function register. The purpose of the Seek function is to position the heads of the selected unit at the cylinder address specified by the Cyl-

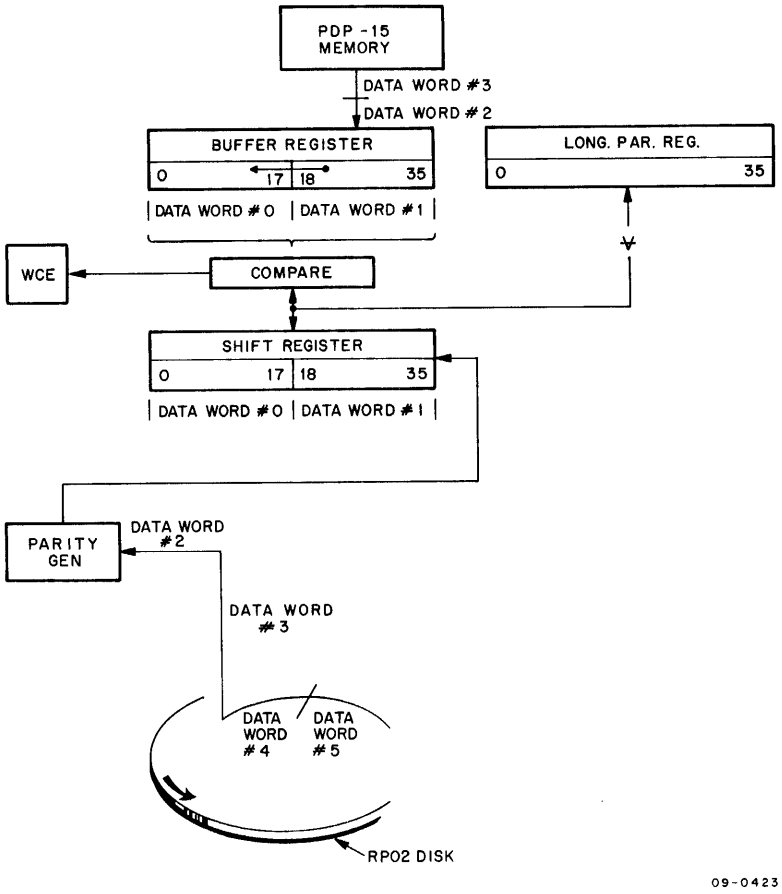


Figure 3-11 WRITE CHECK Function, Transfer States

inder Address Register. When a Seek function is executed, the unit attention line is cleared (provided the heads are not already positioned). This unit attention line is again raised when the Seek has been completed or 100 ms have expired and the Seek was unsuccessful. If the Seek is unsuccessful, a status line called SELECTED UNIT SEEK INCOMPLETE is raised and the appropriate interrupts occur. When a Seek function is successfully completed, the SELECTED UNIT READY status line is set.

3.2.8 Recalibrate Function

The Recalibrate function is executed by loading its function code into the function register. The purpose of the Recalibrate function is to recover the head position after a SELECTED UNIT SEEK INCOMPLETE. When this function is completed, the heads are placed at cylinder 000_8 and UNIT ATTENTION is raised with SELECTED UNIT READY.

3.3 PROGRAM LOOP

The following program loop may be used to debug any execute-type function. The loop repeats the function selected in the data switches and ignores all errors. Data patterns should be loaded from the data switches starting at memory address 1000_8, prior to the start of the program. If the pattern is fixed, the REPT and DEPOSIT NEXT switches can be used. The 2's complement word count and the disk address should be loaded into memory addresses 200_8 and 201_8, respectively, prior to starting the program.

```
100/    703302    CAF        /CLEAR ALL FLAGS
        200200    LAC WC     /PLACE WORD COUNT INTO THE AC
        706364    DPWC       /LOAD THE WORD COUNT REGISTER
        200201    LAC DA     /PLACE DISK ADDRESS INTO THE AC
        706304    DPLA       /LOAD THE DISK ADDRESS
        200202    LAC CA     /PLACE CURRENT ADDRESS INTO THE AC
        706344    DPCA       /LOAD THE CURRENT ADDRESS
        750004    LAS        /GET THE FUNCTION UNIT, AND GO
                             /BIT FROM THE DATA SWITCHES
        706464    DPLF       /LOAD THE FUNCTION REGISTER
        700314    IORS       /READ I/O STATUS
        500203    AND DF     /AND BIT 12 OF THE IORS WORD
                             /BIT 12 IS THE DISK FLAG
        740200    SZA
        600111    JMP .-3    /WASTE 4 μs
        706341    DPSJ
        600115    JMP .-1    /WAIT FOR JOB DONE
        600100    JMP 100    /START OVER
200/    000000               /WC - WORD COUNT
        000000               /DA - DISK ADDRESS
        010000               /CA - CURRENT ADDRESS
        000040               /BIT 12 - DISK FLAG
```

The above routine may also be used for initiate-type functions (with the exception of IDLE), by replacing the DPSJ instruction with a DPSF.

CHAPTER 4
DRAWING CONVENTIONS

4.1 FLOW CHART SYMBOLOGY

The flow charts presented have been prepared in accordance with conventions, all of which may not be familiar to the reader. In the flow diagrams, lines indicate flow; where arrows are not provided, the flow is presumed to be either down or to the right. Wherever a name is enclosed within an oval, a pulse amplifier is indicated. A line leaving the bottom of an oval indicates continuation of flow of control; a line leaving the right side of the oval indicates other actions caused by this pulse.

Horizontal lines that are separated by a time specification indicate delays. The time given is measured through the delay only, and does not include delays through associated gating and pulse amplifier circuits; the time delay of a given operation cannot be determined by simply adding the delays specified.

4.2 BLOCK SCHEMATIC SYMBOLOGY

In the RP15 print set, each logic block schematic has a coordinate system to aid in locating gates etc. Coordinates are numbered from right to left, horizontally from 1 to 8, and lettered from bottom to top vertically from A to D. A label at print coordinate A-1 identifies the logic diagram. The label has three parts:

a. Print name - e.g., Status Control #2
b. Print size and type - e.g., D-BS which means D size, Block Schematic.
c. Print number - e.g., RP15-0-10 which means Print 10 in the RP15 print set.

Connection dots are never used in block schematics. Instead, connections are shown by lines that stop on the line to which they are connected. Lines that cross are not connected.

4.3 LOGIC MODULE SYMBOLOGY

The logic modules used in the RP15 are DEC M-series, which is the integrated circuit, positive logic series. Voltages used are:

LOW(L) = 0V (0V to +0.4V)
HIGH (H) = +3V (+2.4V to +3.6V)

MIL-STD-806B logic symbology is used. The gating symbols use small circles at the inputs of gates to indicate that a low signal activates the function. Absence of a circle indicates that a high signal activates the function. The presence or absence of a circle at the output of a gate indicates that the output is Low (L) or High (H), respectively, when the gate has been activated (its output is true). A gate's output is false if it is at a voltage different from that shown by the gate's polarity indicator (presence or absence of circle). Suffixes L or H indicate the low or high level of a signal when it is true or enabled. A low output polarity indicator from a gate directly connected to a high input polarity indicator of another gate indicates that the input of the fed gate exists only when the output from the feeding gate is not true. The same holds for the opposite set of conditions.

Boolean functions are symbolized as follows:

or * = Logical AND
+ or V = Logical OR (inclusive)
⊻ = Exclusive OR
- = Logical negation (the vinculum is used only for expressions in text)

The most commonly used gating symbols are the NAND (Figures 4-1, 4-2), NOR (Figures 4-3, 4-4), and Inverter (Figures 4-5, 4-6). Each figure shows both the symbol and a Boolean expression of the logical operation it performs. Some of the logic gates are made up of combinations of the basic functions. The operation of these gates can be determined by the combined use of the basic logical relationships (Figure 4-7).

Figures 4-8, 4-9, and 4-10 illustrate the types of flip-flops used in the RP15. The flip-flop in Figure 4-8a requires a high data input when clocked to set; the one in 4-8b requires a low data input to be set. The D-type flip-flop is drawn to agree with the voltage level of the data input necessary to set it.

Figure 4-9 shows the J-K flip-flop. This flip-flop has direct set and reset inputs and clock and clock-gated set and reset inputs. If both gated inputs are high when the flip-flop is clocked, the flip-flop will complement. Figure 4-11 is a representation of the variable clock type M401. The flip-flop in Figure 4-10 is a set-reset flip-flop.

A typical pulse amplifier, as used in the RP15, is shown symbolically in Figure 4-12. Figures 4-13 through 4-16 show other circuit symbols used throughout the RP15.

Each logic symbol is designated alphanumerically as to the following information (see Figure 4-17):

a. Type (M112)

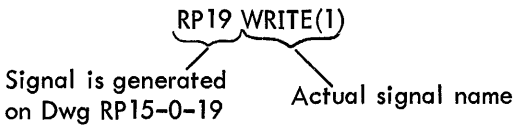
b. Location (L18)

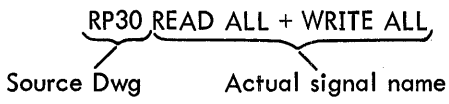
c. Input pins on specific module (P1, R1)

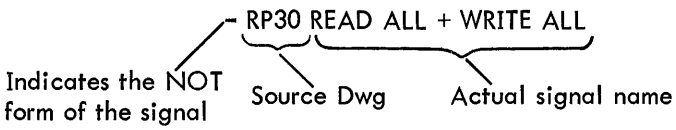
d. Output pin (S1).

Most flip-flop modules include a name in their designation (see Figure 4-18), but synchronizing flip-flops do not (see Figure 4-19).

In the RP15 schematics, a mnemonic convention enables the reader to identify the source print of every signal appearance. Examples are defined in the following:







When a signal originating from a flip-flop is inverted, the signal name is often changed to avoid possible confusion about where the signal actually originated (Figure 4-20).

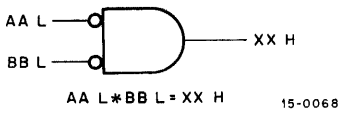


Figure 4-1 NAND Gate (M112)

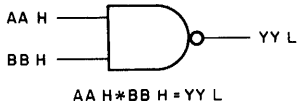


Figure 4-2 NAND Gate (M113)

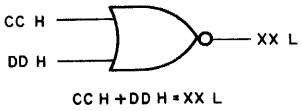


Figure 4-3 NOR Gate (M112)

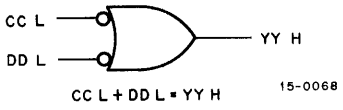


Figure 4-4 NOR Gate (M113)

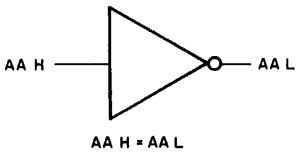


Figure 4-5 Inverter (M111, M611)

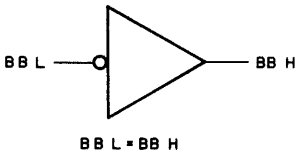


Figure 4-6 Inverter (M111, M611)

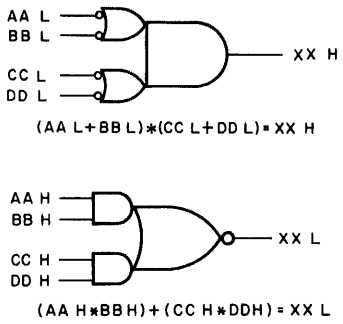


Figure 4-7 Basic Logic Relationships (M121)

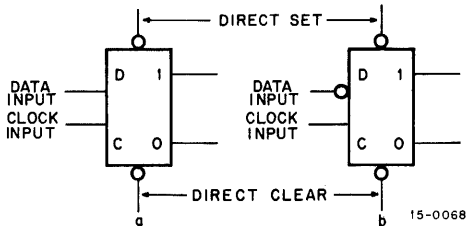


Figure 4-8 D Flip-Flop - Edge Triggered (M216)

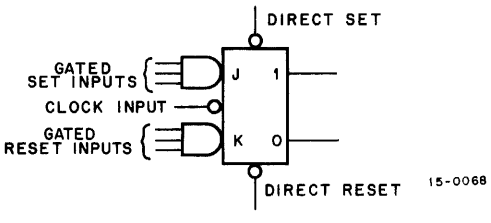


Figure 4-9 J-K Master-Slave Flip-Flop (M204)

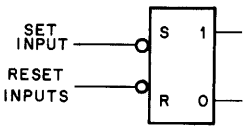


Figure 4-10 R-S Flip-Flop (M203)

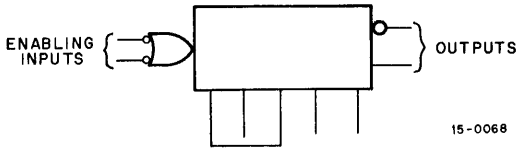


Figure 4-11 Variable Clock (M401)

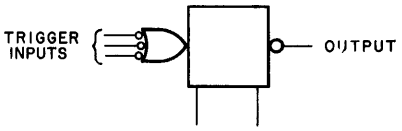


Figure 4-12 Pulse Amplifier (M602)

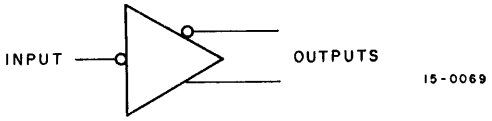


Figure 4-13 I/O Bus Receiver (M510)

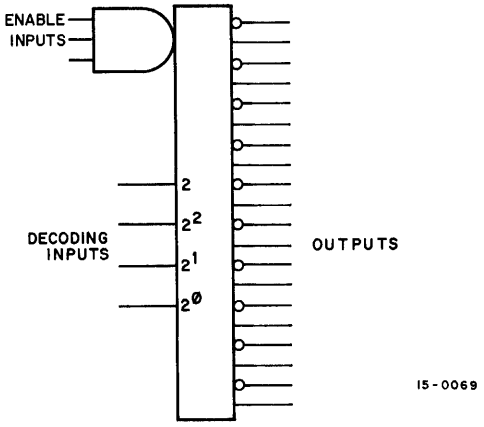


Figure 4-14 Binary to Octal Decoder (M161)

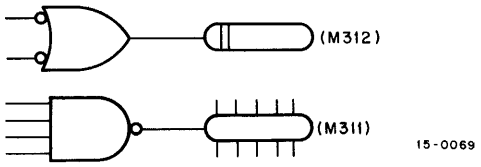


Figure 4-15 Delays

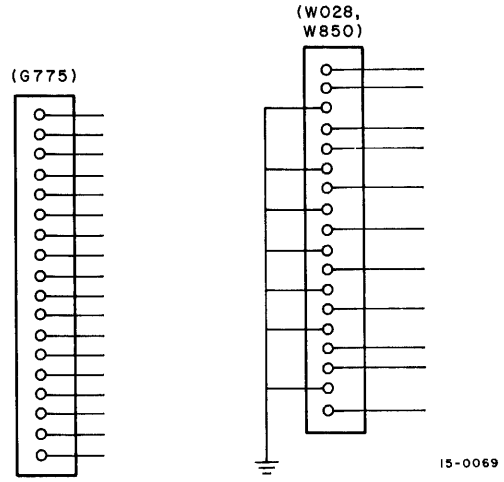


Figure 4-16 Connectors

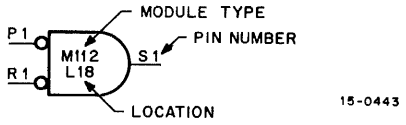


Figure 4-17 NAND Gate

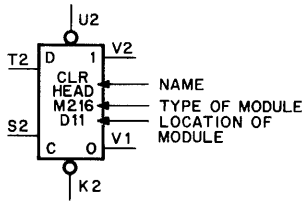


Figure 4-18 CLR HEAD Flip-Flop

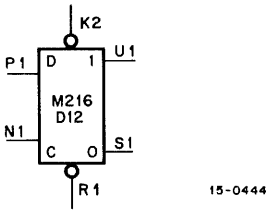


Figure 4-19 Synchronizing Flip-Flop

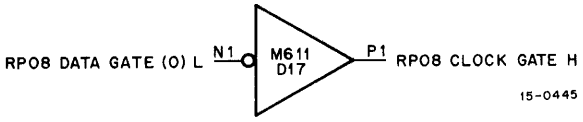


Figure 4-20 Signal Name Changes

CHAPTER 5
PRINCIPLES OF OPERATION AND HARDWARE DESCRIPTION

5.1 GENERAL

The principles of operation of the RP15 are discussed from the hardware standpoint. A detailed block diagram followed by circuit descriptions of the functional blocks are included. In these discussions a knowledge of the PDP-15 I/O Bus, the Data Channel timing diagrams, and the RP02 Disk Pack operation is presumed. Reference is made to some undefined control signals; for the most part, these signals are self-explanatory and are defined when the control logic for that register is described.

5.2 DETAILED BLOCK DIAGRAM

A detailed block diagram of the RP15 Controller is shown in Figure 5-1. This diagram serves a dual purpose by first showing the interrelation of all blocks and then providing a directory to text. The numbers appearing in each block refer to the number of the paragraph that describes that block in detail.

5.3 SELECTING THE CONTROLLER (IOT Selection)

The PDP-15 selects the RP15 Controller through its IOT selection circuit (see Figure 5-1 and Drawing RP15-0-20). The circuit comprises an AND and OR gate matrix configured to decode six device select bits (corresponding to bits 6 through 11 in the MB) and two subdevice bits (corresponding to bits 12 and 13 of the MB) coming from the PDP-15 I/O Cable.

The device select codes, which are fed in as DS0-5, are ANDed in two places to yield 63_8 and 64_8 (decoded as SEL XX L and SEL YY L, respectively). These two signals are ORed to produce DISK SEL H. The signal DISK SEL H is then ANDed with IOP2 (B) H to produce RD RQ L. The SEL XX and SEL YY signals are also inverted to condition two sets of AND MATRIX gates. The subdevice select codes are decoded to produce SUB DEV 00-11 which also conditions both sets of AND MATRIX gates. The outputs of the first column in the matrix are ORed and then ANDed with IOP1 (B) H to produce a SKP RQ L. Column two and column three are conditioned by IOP2 (B) H and IOP4 (B) H, respectively, to produce the remaining RP15 instructions.

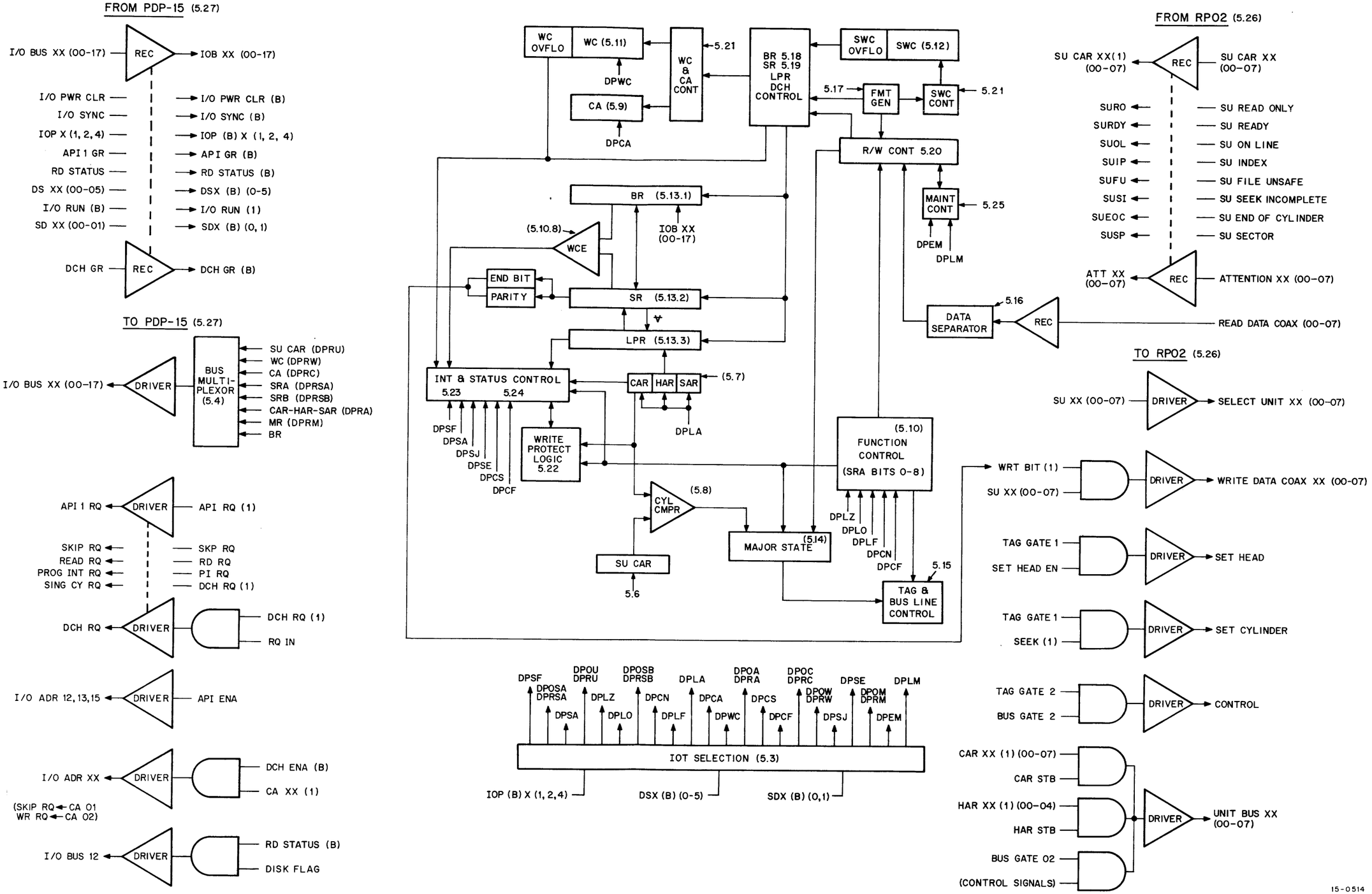


Figure 5-1 RP15 General Block Diagram

5.4 STATUS MONITORING AND DCH DATA (Bus Multiplexer)

Monitoring of RP15/02 status, and data to the PDP-15 Single-Cycle Data Channel, is transferred through the RP15 Bus Multiplexer shown in Figure 5-1 and Drawings RP15-0-42,-43,-44, and -45. The various instructions received from the IOT selection circuit are inverted and then utilized to enable 18-bit sets of AND gates that contain information to be loaded into the PDP-15 Accumulator.

The instruction DPOW (OR the Word Count Register into the AC) places WC00-17 (1) H on BUS00-17 L where the result is then ORed into AC00-17.

The instruction DPOC (OR the Current Address Register into the AC) places CA00-17 (1) H on BUS00-17 L where the result is ORed into the AC00-17.

The instruction DPOSA (OR Status Register A into the AC), which is decoded as DPOF, places the various bits of the Function Register, the Unit Register, and Status Register A on BUS00-17 L where the result is ORed into AC00-17.

The instruction DPOSB (OR Status Register B into the AC), which is decoded as DPOS, places the various bits of Status Register B on BUS00-17 where the result is ORed into AC00-17.

The instruction DPOA (OR the Cylinder, Head, and Sector Address Registers into the AC) places the 8-bit Cylinder Address Register on BUS00-07 L, the 5-bit Head Address Register on BUS08-12 L, and the 4-bit Sector Address Register on BUS14-17 L; where the result is ORed into AC00-17.

The instruction DPOM (OR the Maintenance Register into the AC) places the 6-bit Maintenance Register (MR00-05) on BUS00-05 L where the result is ORed into AC00-05.

The instruction DPOU (OR the Select Unit Cylinder Address Register into the AC) places the 8-bit Selected Unit Cylinder Address Register (SUCAR00-07) on BUS10-17 L where the result is ORed into AC10-17.

The signal DCH DATA L is generated, as shown on Drawing RP15-0-45, during single-cycle breaks on "in" transfers to memory (Read and Read All functions). This signal places the first 18 bits of the Buffer Register (BR00-17) on BUS00-17 L where they are transferred via the I/O bus into the PDP-15 Memory.

NOTE

On Drawing RP15-0-45, the pull up resistors used on the collector ORing of the M149 Bus Multiplexer Module produce the standard logic level used in M-series logic.

5.5 SELECTING THE DRIVE (Unit Register)

The RP15 is designed to interface up to eight RP02 units. These units are addressed by a 3-bit register, called the Unit Register (Drawing RP15-0-21), whose octal content describes the unit presently selected. The octal unit number assigned to a unit depends on its physical location on the bus and is not logically assignable. Unit addresses are coded 00_8 through 07_8.

The Unit Register is decoded as shown in Figure 5-2. The output of the M622 Bus Driver is wired to the appropriate signal cable that connects to the RP02 unit (see Drawing RP15-0-53).

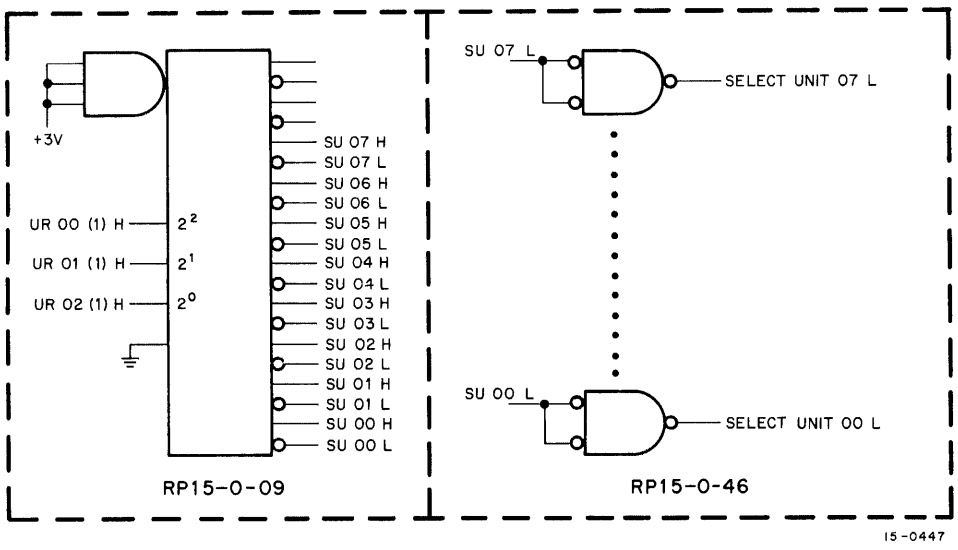


Figure 5-2 Unit Selection Circuit

5.6 SELECTED UNIT CYLINDER INTERROGATION (SUCAR)

When a system is equipped with more than one RP02, it is often desirable to know the location of the heads in any one unit. Their position can be determined by using the Selected Unit Cylinder Address Register contained in each RP02:

Step	Procedure
1	Select the unit to be interrogated.
2	Read the contents of that 8-bit register into the accumulator.

Step 2 is allowed only when it is permissible to change the Unit Select Register and the unit being interrogated is not executing a previously given command. The SUCAR is not a hardware register within the RP15 but is received from the unit presently selected via the unit bus cable. (See Figure 5-3 and Drawings labelled on the figure.)

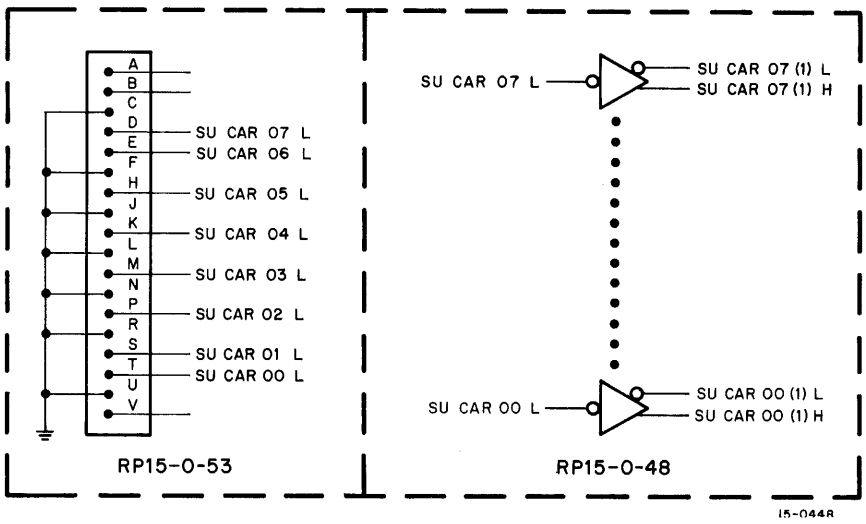


Figure 5-3 SU Cylinder Interrogation Circuit

5.7 ADDRESSING THE PACK (CAR, HAR, and SAR)

The RP02P Disk Pack consists of 11 evenly spaced recording platters mounted on a single shaft. Because of this precarious arrangement, the top- and bottom-most surfaces are not used for recording; instead, a metal disk is attached to the bottom surface. The disk contains 20 evenly spaced notches and a twenty-first notch called the Index.

A circuit, designed to detect these notches, rejects every other one of the twenty notches, thereby dividing the disk pack into ten equal sectors. These sectors are addressed by a 4-bit register called the Sector Address Register (SAR) (see Drawing RP15-0-30). The sector addresses are coded 00_8 through 11_8, which leaves illegal codes 12_8 through 17_8 that may appear in the Sector Address Register. When detected by the controller, illegal codes raise an error flag that results in the appropriate interrupts.

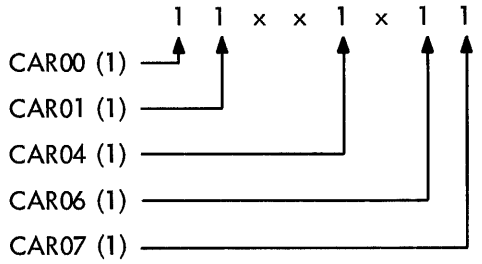
A separate Read/Write head is provided for each of the twenty inner recording surfaces. These heads, mounted in parallel and in vertical alignment to each other, are attached to a common head tower. The heads are selected by a 5-bit register called the Head Address Register (HAR) (see Drawing RP15-0-29). Head addresses are coded 00_8 through 23_8. When detected by the controller, illegal codes 24_8 through 37_8 raise an error flag that results in the appropriate interrupts.

The position of all heads, vertically aligned with respect to the vertical axis that passes through the center of all surfaces, is called a cylinder. Head positioning is controlled by a linear positioning motor and detenting mechanism that is designed to stop the heads in 203 different cylinders. These cylinders are coded 00_8 through 312_8 from the outer-most cylinder to the inner-most cylinder, respectively. Cylinders are addressed by an 8-bit register called the Cylinder Address Register (CAR) (see

Drawing RP15-0-28). When detected by the controller, illegal codes 313_8 through 377_8 raise an error flag that results in the appropriate interrupts.

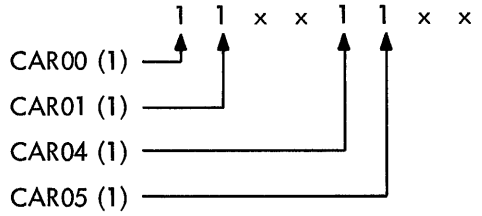
The intersection of a cylinder, head, and sector address defines a unique sector that is the smallest addressable unit in the system. Each sector has a data field of 128 36-bit words plus a header word that uniquely defines that sector. A word constitutes two PDP-15 data words during Read or Write operations.

The decoding circuits for illegal cylinder, head, and sector addresses are shown in simplified form in Figure 5-4. Note that the AND gate that combines CAR00 (1) with CAR01 (1) enables all other inputs in the NECA equation; NECA must be a minimum of $3xx_8$. This signal is then ANDed with CAR04 (1), CAR06 (1), and CAR07 (1) to produce an equation stating:

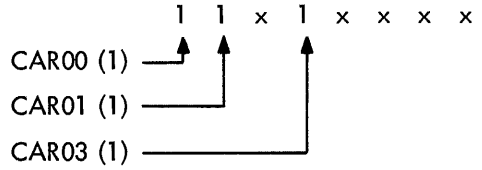


is illegal.

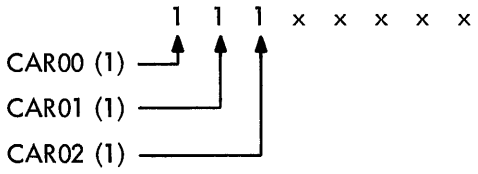
This code includes the number 313_8 (among others). Note also that the conditions for the numbers 314_8, 315_8, 316_8, and 317_8 are decoded by the AND of the original equation [CAR00 (1) and CAR01 (1)] and CAR04 (1) with CAR05 (1).



Two inputs remain which decode the numbers 320_8 to 337_8, inclusive, and all numbers equal to, or greater than, 340_8. They are:



and



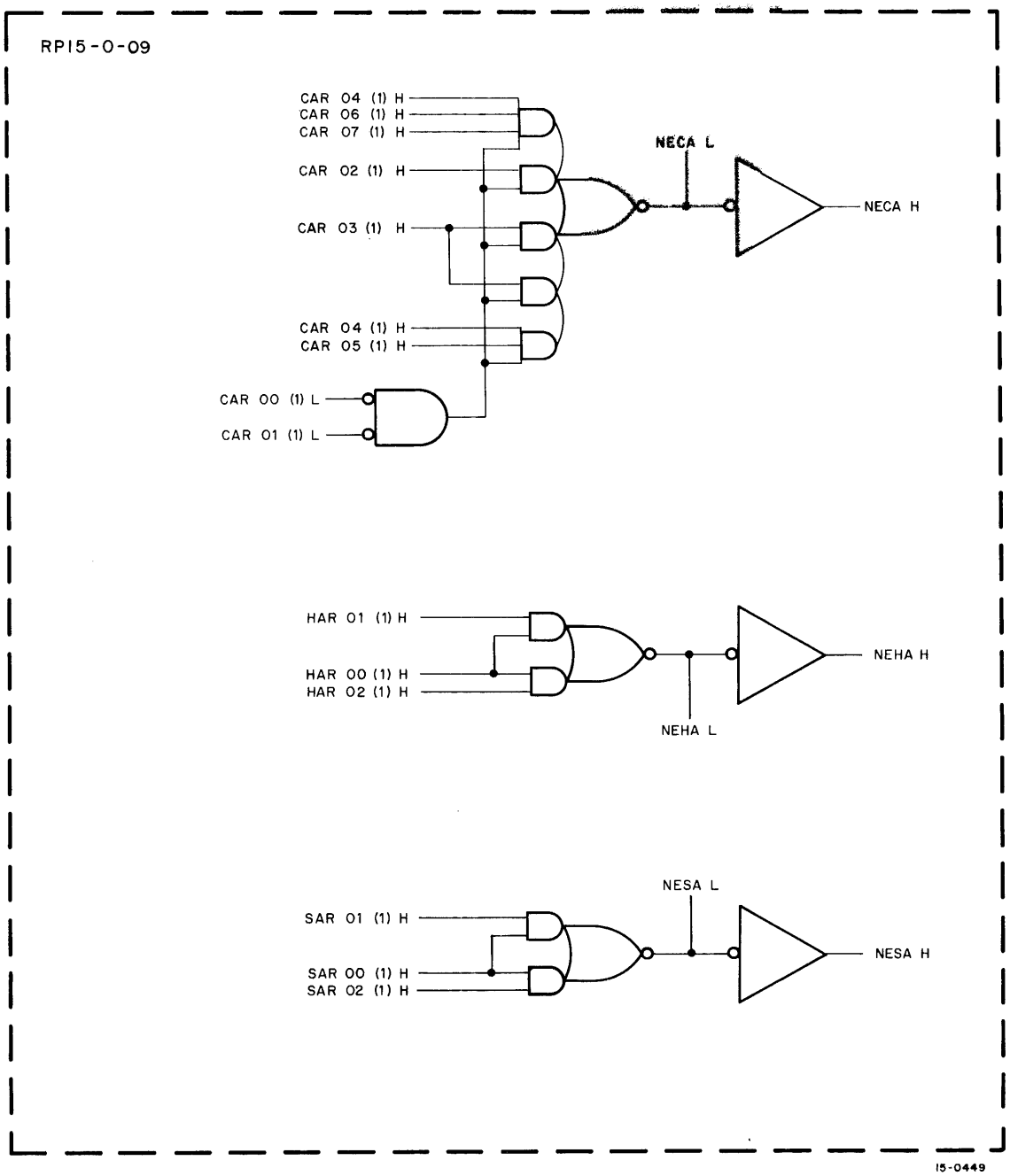


Figure 5-4 Illegal Disk Address Decoding

In this way, coding covers all numbers from 313_8 to 377_8, inclusive, in the NECA equation. NEHA and NESA may be decoded in the same manner.

The Cylinder, Head, and Sector Address Registers comprise three incrementing ripple count registers formed from D-Type flip-flops. These registers are preset by DPLA ANDed with the corresponding IOB bit, and are cleared by CLR CAR, CLR HAR, and CLR SAR, respectively.

Control logic for the Cylinder, Head, and Sector Address Registers is shown on Drawings RP15-0-28, -29, and -30, respectively. Incrementing the SAR is initiated by signals called SECTOR END L (generated after the completion of each sector) or MAINT INC SAR L (see Figure 5-5). SECTOR END is conditioned by five signals: WEE (1), LEE (1), WCEE (1), TE (1), and NORMAL H. Any of the first four signals inhibits incrementing of the SAR if a word or longitudinal parity error was accumulated in a sector, or if a write check error or timing error occurred. The fifth signal inhibits incrementing of the SAR if the control is not in the NORMAL mode. When the controller is in the FORMAT mode, therefore, the SAR is not used.

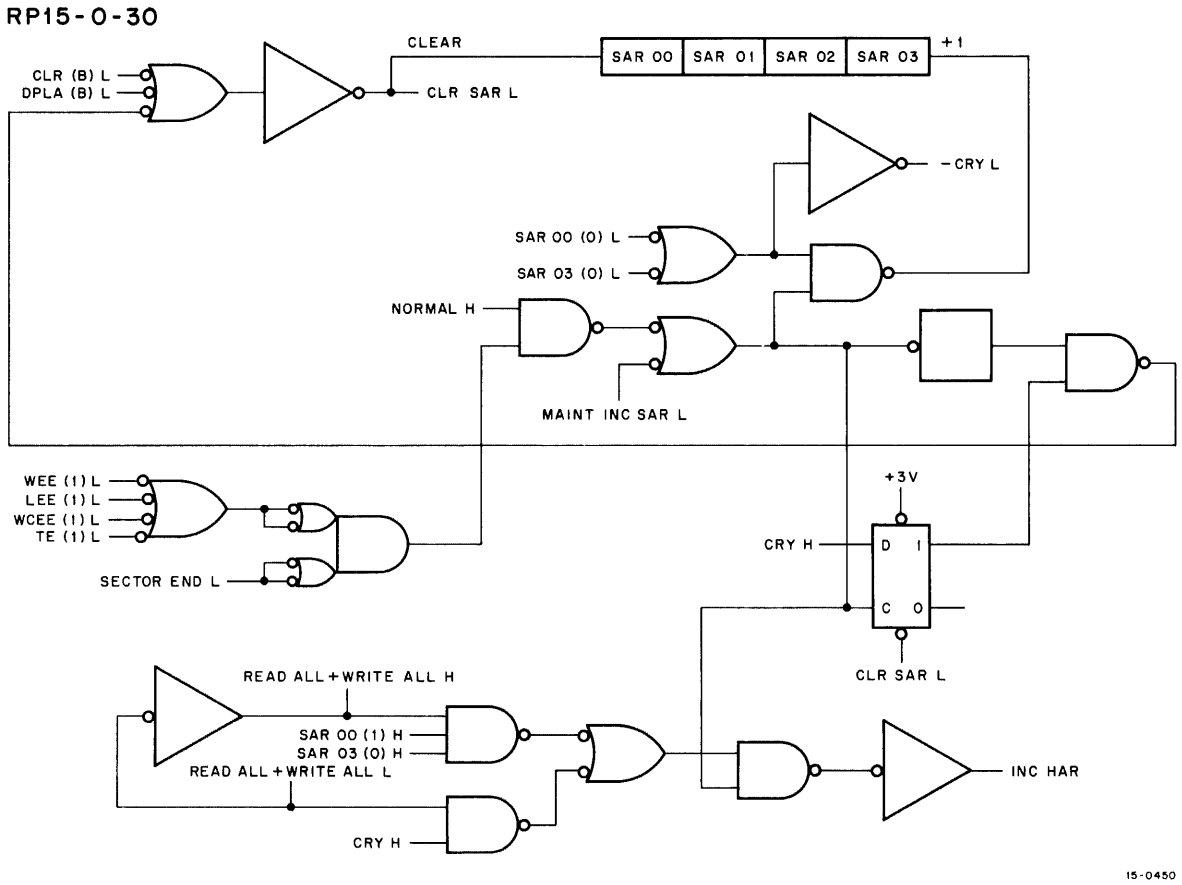


Figure 5-5 SAR Control Logic

The actual incrementing of the SAR is inhibited if SAR00 (1) and SAR03 (1) are both true. This condition produces a signal called CRY H (the NOT condition is shown in Figure 5-5) which indicates that the maximum SAR count has been reached (11_8). If this condition had been true prior to SECTOR END, the data side of the synchronizing D-Type flip-flop would have been enabled and would have allowed this flip-flop to set at the leading edge of SECTOR END. This flip-flop then enables a pulse amplifier (M606) that generates a pulse at the trailing edge of SECTOR END. This pulse is ORed with CLR (B) L and DPLA (B) L to clear the SAR with CLR SAR L. The process just described allows the SAR to increment from the maximum code 11_8 to 00_8.

If CRY H is true before SECTOR END, another decision is made. If the function being executed is not Read All or Write All, then INC HAR H is generated which, in turn, increments the HAR. Note that the SAR now counts from 00_8 to 11_8, and then always back to 00_8. At the transition of 11_8 to 00_8, the HAR is incremented providing the function is Read, Write, or Write Check.

The HAR is also incremented during Read All and Write All functions, but only when the SAR contains a count of 10_8 before SECTOR END. This is done by ANDing READ ALL + WRITE ALL H with SAR00 (1) H and SAR03 (0) H.

The HAR is shown in simplified form in Figure 5-6. Again, the maximum HAR count is decoded and used to disable incrementing of the HAR. The code is:

HAR00 (1) H
HAR03 (1) H
HAR04 (1) H.

This is shown in Figure 5-6 in the NOT condition. In addition to disabling the HAR increment, this signal also enables the creation of INC CAR L and CLR HAR L. DPLA (B) L and CLR (B) L are also ORed to produce CLR HAR L.

Assuming that the maximum HAR count is not present, INC HAR H (generated on Drawing RP15-0-30) will produce the incrementing signal for HAR.

The CAR is shown in Figure 5-7. As with the SAR and HAR, the maximum CAR count is decoded and used to disable the incrementing of the CAR. The code is:

CAR00 (1) H
CAR01 (1) H
CAR04 (1) H
CAR06 (1) H.

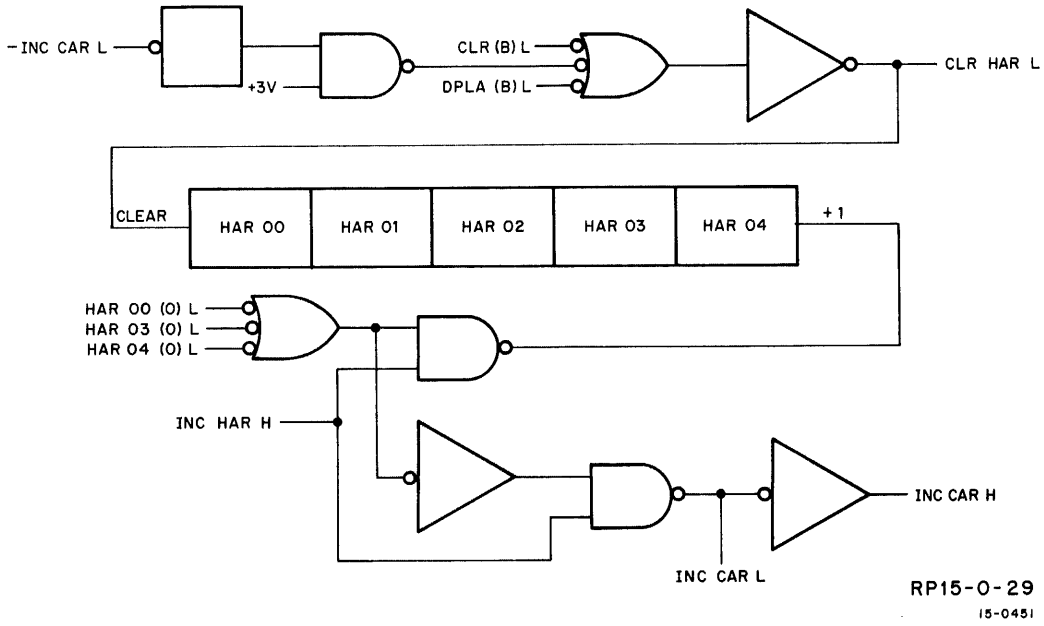


Figure 5-6 HAR, Simplified Schematic

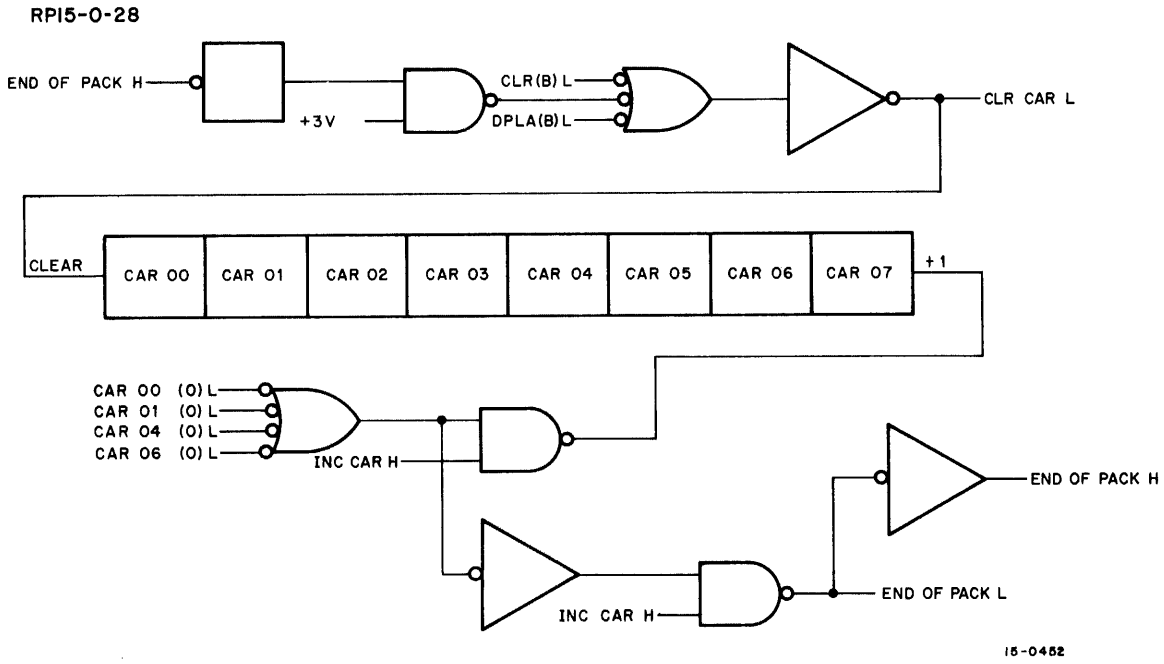


Figure 5-7 CAR, Simplified Schematic

This is shown in the NOT condition in the figure. This code is also used to create END OF PACK H, a signal that indicates to the controller that the physical end of pack has been reached. END OF PACK H is ORed with CLR (B) L and DPLA (B) L to produce CLR CAR L.

Assuming that the maximum CAR count is not present, INC CAR H (created on Drawing RP15-0-29) will produce the signal necessary to increment the CAR.

The CAR, HAR, and SAR are shown functionally in Figure 5-1. Note the connection between the CAR and the INT & STATUS CONTROL box. This connection represents END OF PACK.

5.8 CYLINDER COMPARISON

The RP15 Cylinder Comparator is shown in Drawing RP15-0-27 and in simplified form in Figure 5-8. The Cylinder Comparator maintains a check between the controller Cylinder Address Register and the Selected Unit Cylinder Address Register. This logic is used to determine if the Seek state should be entered. Each state of every CAR bit is ANDed with the opposite state of the same SUCAR bit. Each AND is ORed to one composite OR that issues -CYL CMPR L until all bits correspond. If CYL CMPR H is true, reading or writing proceeds and the Seek state is not entered. This is described in more detail in Major State Control, Paragraph 5.14.

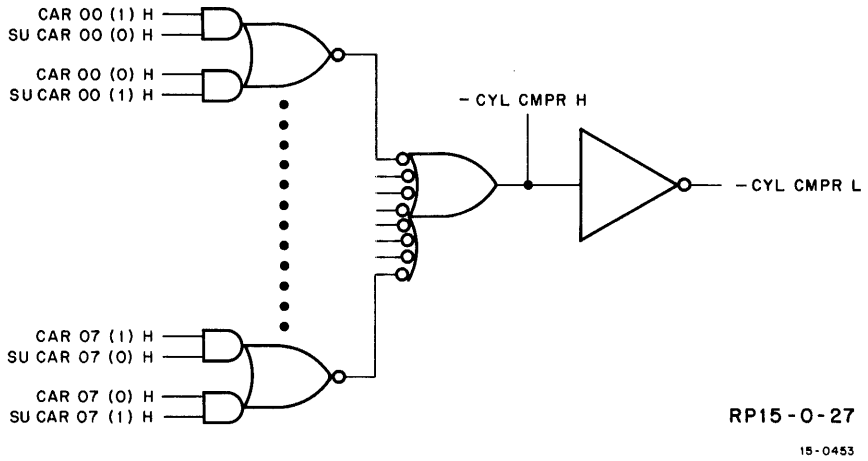


Figure 5-8 Cylinder Comparator, Simplified Schematic

5.9 SEQUENCING THE MEMORY (CA)

Data transfers between the RP15 and the PDP-15 Memory use the single-cycle data channel. The RP15 contains an 18-bit Current Address Register (CA) that locates each data word transferred in consecutive

memory addresses. The initial address is specified by loading it into the Current Address Register before the command to execute a data transfer. The Current Address Register is automatically incremented after each data word is transferred from memory.

The CA Register is made up of 18 D-Type flip-flops connected as a ripple counter (see Drawing RP15-0-32).

NOTE

The connection is actually broken in two places for reasons explained under Word Count and Current Address Control, Paragraph 5.21.

Each flip-flop is preset by the DPCA signal ANDed with the corresponding IOB (I/O Bus) bit. The entire register is cleared with CLR CA L. Refer to Figure 5-1 for the functional flow position of the Current Address Register.

5.10 COMMANDING THE CONTROLLER (Functional Control - SRA Bits 00-08)

The PDP-15 Computer uses the Function Register to tell the controller what function is to be performed. The controller then translates these commands to the drive through the Tag and Bus Line Control described in Paragraph 5.15. The RP15 Function Register is shown in Drawing RP15-0-21 and simplified in Figure 5-9. The register is arranged such that the instruction DPLF is ORed with either DPLO (Load AC 1s) or DPLZ (Load AC 0s) to produce FR EN SET L or FR EN CLR L, and two FR strobes (A and B). The FR EN's are ANDed with their appropriate I/O bus bits (00-08) to inputs of JK flip-flops UR00-02, FR00-02, GO, ATD, and DED. These flip-flops are clocked at the trailing edge with one of two strobes; when DPLF is issued, the Function Control will reproduce the contents of I/O bus bits 00-08; when a DPLO is issued, only 1s on the I/O bus will be set into the registers; when DPLZ is issued, only 0s will be transferred. I/O bus bit 06 can be cleared to produce DED (Done and Error Flag Interrupt Disable), I/O bus bit 07, when cleared, will produce ATD (Attention Flag Interrupt Disable). When I/O bus bit 08 is set, it will produce GO (Enable Execution of the Function Register); bits 00-02 will load the Unit Register. The Function Register is loaded from I/O bus bits 03-05.

The RP15 provides hardware for the performance of eight different functions. These functions can be categorized as either initiate- or execute-type functions (refer to Table 5-1). Initiate-type functions are described as those that require only 4 μs of controller time from the time of the command. During this time, the controller is held in the BUSY state. Although a Seek may require 50 ms for completion, the unit selected need only be selected for the BUSY period. Execute-type functions, however, require all the controller's time necessary to complete the function. The controller is BUSY for the entire operation; the unit requested must also be BUSY for the entire operation, and cannot be deselected to begin an initiate-type function.

RPI5-0-21

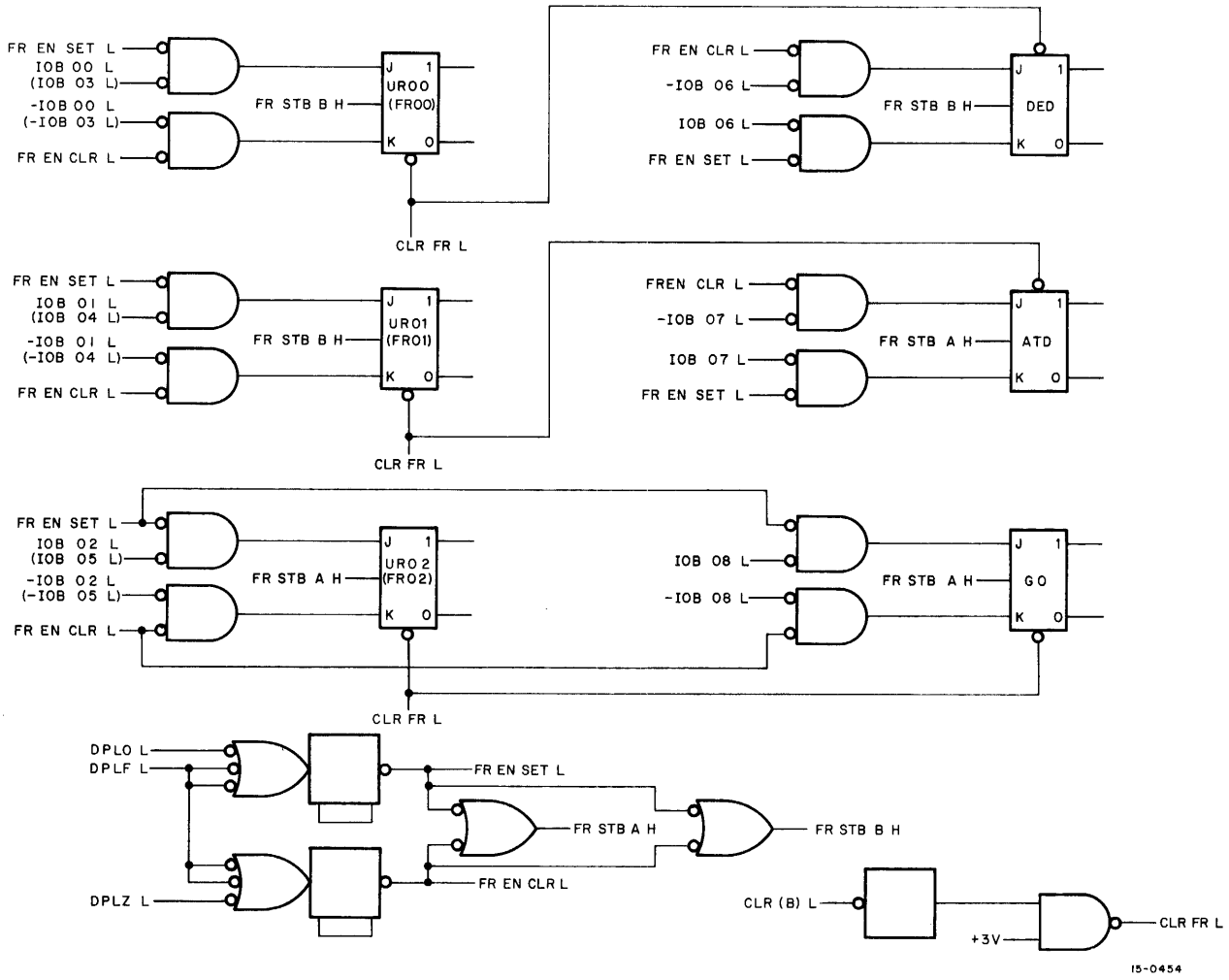


Figure 5-9 Function Register, Simplified Schematic

Table 5-1
RP15 Function Arrangement

Function	Code	Type
Idle	0	Initiate
Read	1	Execute
Write	2	Execute
Recalibrate	3	Initiate
Seek	4	Initiate
Read All	5	Execute
Write All	6	Execute
Write Check	7	Execute

Functions are selected by loading the 3-bit Function Register with an octal number equal to the function code (refer to Table 5-1).

5.10.1 Idle Function (FR = 0)

The Idle function constitutes the NOP state of the controller; it is executed by loading its octal code into the Function Register with a DPLO, DPLZ, or DPLF instruction. The Idle function is also executed when the PDP-15 is powered up, the I/O RESET key on the PDP-15 Console is pressed, a CAF (Clear All Flags) instruction is issued, or a DPCF instruction is issued.

5.10.2 Read Function (FR = 1)

The Read function is executed by loading its octal code into the Function Register with a DPLO, DPLZ, or DPLF instruction. Read transfers data from the RP02 to the PDP-15, starting with the memory location specified by the Current Address Register. Each data word transferred increments the Current Address and Word Count Registers. The contents of the Word Count Register at the beginning of the transfer determine the number of data words to be transferred. When the Word Count Register overflows, data transfer stops. The remainder of the present sector is read and parity is checked before the JOB DONE flag is raised. The Current Address Register contains the address of the last data word transferred plus one. At this point, a Continue may be effected by reloading the Word Count and/or Current Address Registers and issuing a DPCN instruction.

5.10.3 Write Function (FR = 2)

The Write function is executed by loading its octal code into the Function Register with a DPLO, DPLZ, or DPLF instruction. Write transfers data from the PDP-15 to the RP02, starting with the memory location specified by the Current Address Register. Each data word transferred increments the Current Address and Word Count Registers. The contents of the Word Count Register at the beginning of the transfer determine the number of data words to be transferred. When the Word Count Register overflows, data transfer stops. The remainder of the present sector is written with zeros and accumulated parity is written before the JOB DONE flag is raised. The Current Address Register contains the address of the last data word transferred plus one. At this point, a Continue may be effected by reloading the Word Count and/or Current Address Registers and issuing a DPCN instruction.

5.10.4 Recalibrate Function (FR = 3)

The Recalibrate function is executed by loading its octal code into the Function Register with a DPLO, DPLZ, or DPLF instruction. The purpose of the Recalibrate function is to recover the head position

after a Selected Unit Seek Incomplete. When this function is completed, the heads are placed at cylinder 000_8 and both UNIT ATTENTION and SELECTED UNIT READY are raised.

5.10.5 Seek Function (FR = 4)

The Seek function is executed by loading its octal code into the Function Register with a DPLO, DPLZ, or DPLF instruction. The purpose of the Seek is to position the heads of the Selected Unit at that cylinder address which is specified by the Cylinder Address Register. When a Seek function is executed, the Unit Attention line is cleared (provided the heads are not already positioned). The Unit Attention line is again raised when the Seek has been completed or if 100 ms have expired and the Seek has been unsuccessful. If the Seek is unsuccessful, a status line called Selected Unit Seek Incomplete (SUSI) is raised and the appropriate interrupts occur. However, at the successful completion of a Seek function, the Selected Unit Ready (SU RDY) status line is set.

NOTE

Because the Seek is an initiate-type function, the target unit need only remain selected for 4 μs after its execution. A system that has several drives can start Seek operations in chain fashion provided a 4-μs hold exists after each Seek is executed.

5.10.6 Read All Function (FR = 5)

The Read All function is executed by loading its octal code into the Function Register with a DPLO, DPLZ, or DPLF instruction. The Read All function is identical to the Read function, except that the Sector Address Register must be loaded with the sector address minus one, and both the header word and data field are read into memory. The Word Count Register should be loaded to include the header word which consists of two data words. Note that "Sector Address Register must be loaded with the sector address minus one..." only refers to the sector address and not to any other. For example, if the desired sector is

Cylinder 2
Head 23
Sector 0, } Entire Desired Address

"one" should be subtracted from sector 0 to give sector minus one as follows:

Cylinder 2
Head 23
Sector 11 } Load CAR, HAR, and SAR with this.

Note that "one" was not borrowed from Head 23 as shown below,

Cylinder 2 Head 22 Sector 11	DO NOT load CAR, HAR, and SAR with this for a Read All of sector address CYL 2, HD 23, and SEC 0.

Note also, when subtracting, that sectors are numbered octally.

5.10.7 Write All Function (FR = 6)

The Write All function is executed by loading its octal code into the Function Register with a DPLO, DPLZ, or DPLF instruction. The Write All function has two subfunctions designated Write All Normal and Write All Format. The applicable subfunction is determined by the position to which the NORMAL/FORMAT switch on the logic panel is set.

The Write All Normal subfunction is identical to the Write function, except the Sector Address Register must be loaded with the desired address minus one (see Read All function), and both the Header word and data field are written from memory. In loading the Word Count Register, the header word, which consists of two data words, should be included.

The Write All Format subfunction is identical to the Write function, except an entire cylinder is written at a time, and the surface and sector address must be cleared. The entire sector is written, but only those header words required for one cylinder need be in memory. This instruction is used exclusively by the Formatter Diagnostic which initializes disk packs.

5.10.8 Write Check Function (FR = 7)

The Write Check function is executed by loading its octal code into the Function Register with a DPLO, DPLZ, or DPLF instruction. The Write Check function is a combination of the Write and Read functions and is entered in the same way as Write. Data words are transferred from the PDP-15 to the RP15; at the same time, data words are read from the RP02 and also transferred to the RP15. In the controller, the two words are compared bit-for-bit; any discrepancies will raise a status bit called Write Check Error which results in the appropriate interrupts. Data remain unchanged in both memory and disk.

The RP15 Write Check Compare circuit is shown in simplified form in Figure 5-10 and Drawings RP15-0-24, -25, and -26. The Write Check Comparator comprises AND and OR gates feeding four ORs which, in turn, feed a common OR. When in Write Check mode, the controller reads back what has just been written on the disk, to make sure that no errors have occurred. To accomplish this check, each state of each BR bit (filled from memory) is ANDed with the opposite state of the same SR bit (filled from the RP02); in this way, if all SR bits match all BR bits, no output is seen from the

comparator. If any bit state does not match, it results in -WCC H being sent to the Status Control (Drawing RP15-0-10) which is used to raise an error flag and an interrupt. In Figure 5-1, note the arrangement of the Write Check Comparator between the BR and SR blocks.

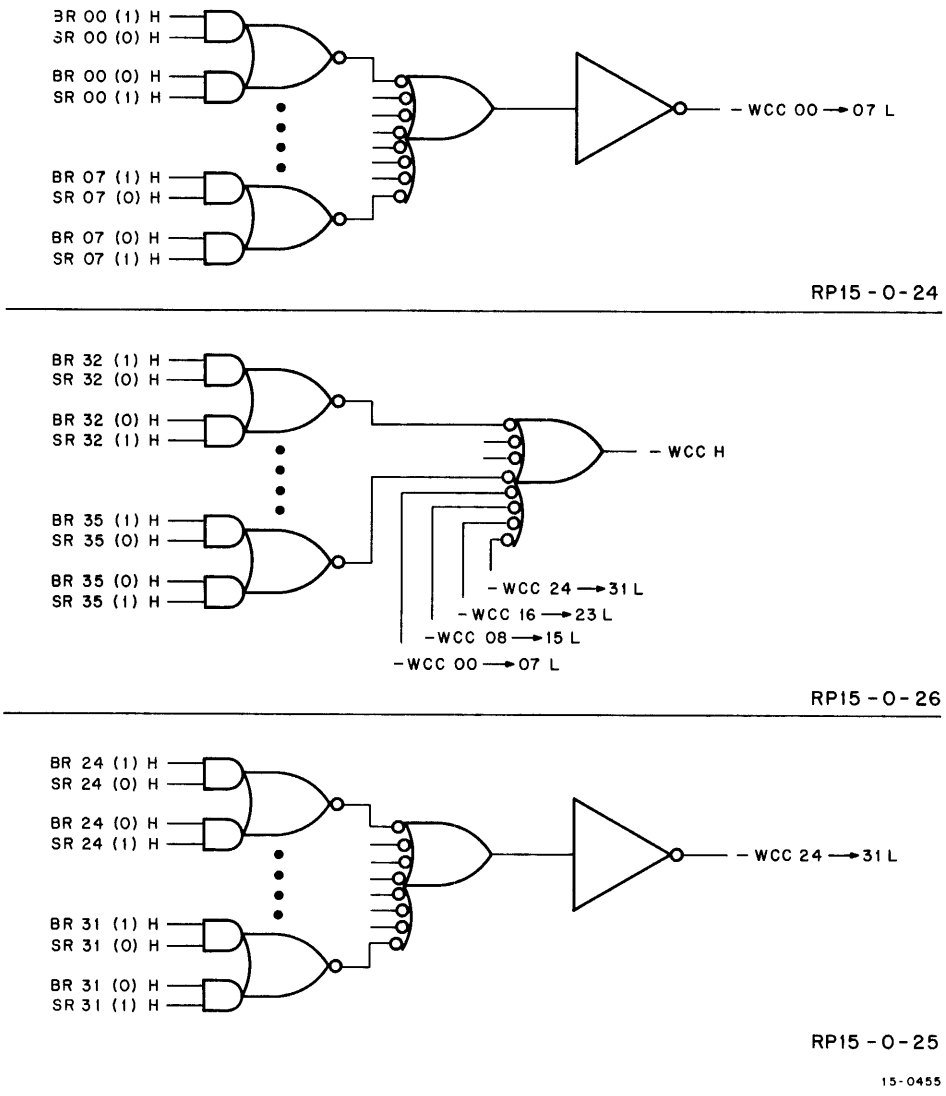


Figure 5-10 Write Check Compare, Simplified Diagram

5.11 DETERMINING LENGTH OF TRANSFER (WC)

The length of each record transferred is controlled by an 18-bit Word Count Register (WC). Before the command is given to execute a transfer, this register is loaded with the 2s complement of the number of data words desired in one transfer. Any number from 1_{10} to $262,144_{10}$ could be specified as a record length, if it were not for the limiting factor of memory capacity.

In general, the smallest addressable unit is the sector; however, record lengths that are shorter than a sector may be transferred. Transfers will start at the beginning of the sector with the remainder of that sector filled with zeros (the unused word positions are wasted). Data transfers can only start at the beginning of a sector.

NOTE

The above is true also of multiple sector transfers ending within the sector.

The RP15 Word Count Register is shown in Figure 5-1 and Drawing RP15-0-31. DPWC presets CD flip-flops WC00-17 from IOB bits 00-17. All 18 bits of the word count can be cleared by CLR WC L. The WC Register is also a ripple count register that can be incremented by INC WC H from the WC and CA Control. This causes the register to count down the desired word count each time a memory transfer occurs.

5.12 MAINTAINING DISK FORMAT (SWC)

The RP15 Sector Word Count circuit is shown in Figure 5-11 and Drawing RP15-0-23. This circuit keeps track of the number of 36-bit data words the controller has either read from or written on the disk, and limits that number to 128 words per sector.

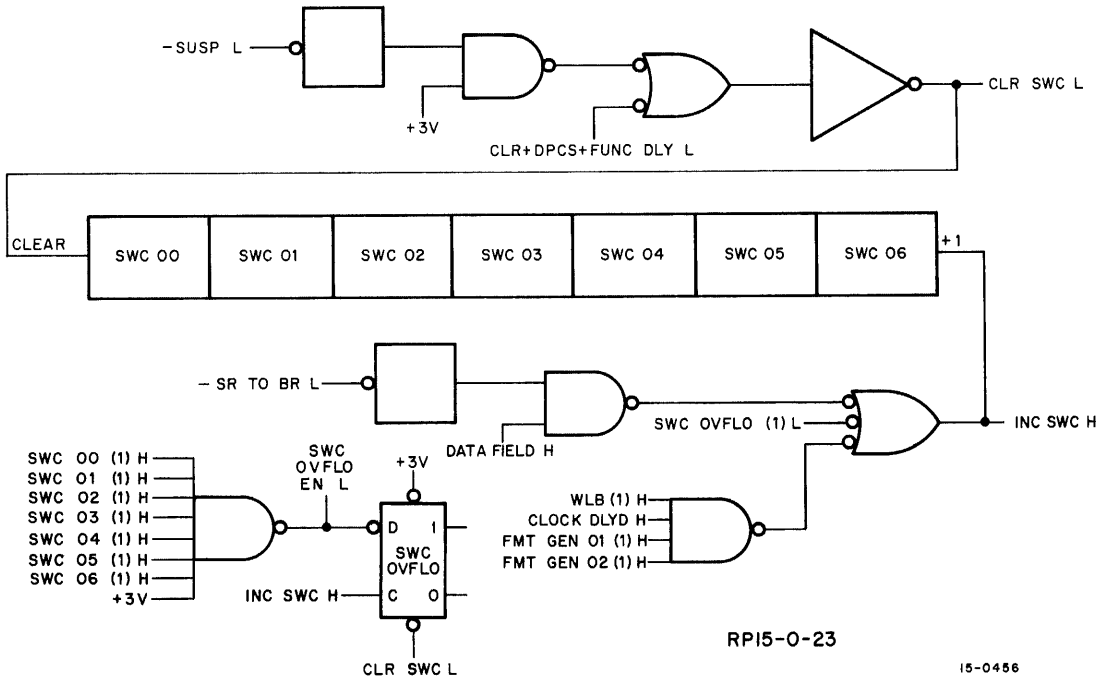


Figure 5-11 Sector Word Counter, Simplified Diagram

This register is a 7-bit ripple counter incremented by INC SWC H. The 1 states of SWC00-06 are ANDed to the D-input of the SWC OVFLO (overflow) flip-flop. This flip-flop is set when all seven bits of the SWC are 1s prior to INC SWC H. INC SWC H is produced under two conditions, each of which are ANDed and then ORed to produce the signal.

In Write, these conditions are WLB (1) H (sets at the end of each word written), CLOCK DLYD H, and FMT GEN01-02 (1) H; at the end of writing each word, the sector word count is incremented.

In Read, if DATA FIELD H is true and -SR TO BR L is received (trailing edge of SR TO BR H), the sector word count is incremented.

At the end of 128 words, all SWC flip-flops will be on a 1; on INC SWC H, the SWC OVFLO flip-flop will be set. This latches INC SWC H so that when the LPR word is written or read the SWC is not again incremented.

CLR SWC L clears both the SWC Register and the SWC OVFLO flip-flop. This signal is produced by the OR of the following:

-SUSP L	(Trailing edge of Selected Unit Sector Pulse)
CLR	(Power clear, CAF (Clear All Flags IOT 3302), DPCF, or I/O RESET on the PDP-15 Console)
DPCS	(Disk Pack Clear Status)
FUNC DLY	(Produced after issuing DPLO, DPLZ, DPLF, or DPCN)

5.13 PROCESSING THE DATA (BR, SR, and LPR)

The RP15 contains three data registers that are not under program control but manipulate data within the controller and provides compatibility between RP02P Disk Packs used on the PDP-15 Computer System and those used on the PDP-10 Computer System. These registers also provide the effect of double buffering between the PDP-15 and the RP15.

5.13.1 Buffer Register

The Buffer Register is 36 bits in length. During Write operations data are transferred from the PDP-15, in two 18-bit words, to the Buffer Register. This transfer is done in two consecutive memory cycles.

During Read operations, the contents of the Buffer Register are broken into two 18-bit words that are transferred to the PDP-15 in two consecutive cycles.

The RP15 Buffer Register is shown in Figure 5-12 and Drawings RP15-0-33, -34, and -35. The Buffer Register sits between the PDP-15 Processor and the RP15 Controller. The register is divided into

quarters with BR STB A H clocking CD flip-flops BR00-08 and BR18-26, and BR STB B H clocking CD flip-flops BR09-17 and BR27-35. These strobes originate in the Buffer Register Control (Drawing RP15-0-13) and are described in Paragraph 5.18. The BR flip-flops are cleared in like fashion by CLR BR A L and CLR BR B L which also originate in the Buffer Register Control.

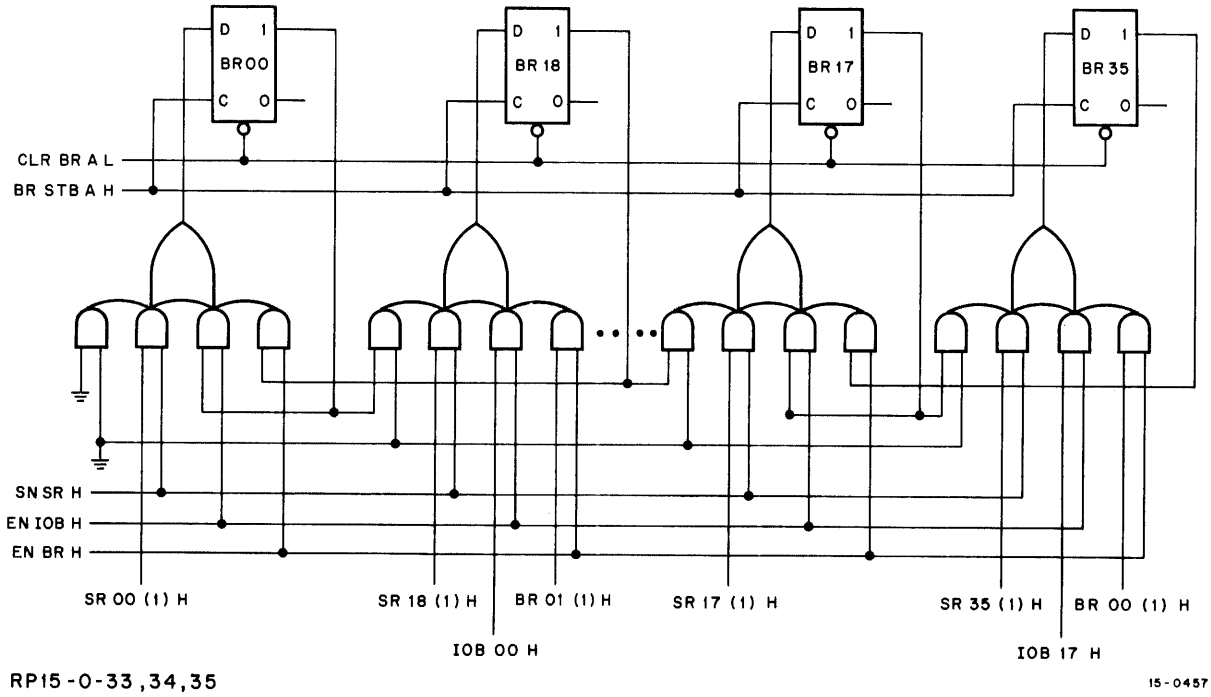


Figure 5-12 Buffer Register, Simplified Diagram

Each BR flip-flop is set by an OR gate of three possible AND gate conditions. One set looks at associated bits in the Shift Register and is enabled by EN SR H. Another set looks at associated IOB bits and is enabled by EN IOB H. The third set of AND gates looks at the 1 state of each comparable bit in the second 18-bit half of the Buffer Register and is enabled by EN BR H. These enabling levels are generated in the Buffer Register Control.

In Write operations, IOB bits from the PDP-15 are enabled into the buffer by EN IOB H and strobed by BR STB A and B, in two consecutive memory cycles (18-bit words). The first word enters BR18-35 and is transferred to BR00-17 by EN BR H. On the second memory cycle, IOB00-17 enters BR18-35 and the entire 36 bits are parallel-transferred to the Shift and Longitudinal Parity Registers for further processing.

In Read operations, the 36 bits, which have been serially assembled in the Shift Register, are parallel-transferred to the Buffer Register by EN SR H and the two BR strobes; from the Buffer Register they are

transferred to the PDP-15 in two 18-bit words during two consecutive memory cycles. This transfer is done by gating BR00-17 onto the I/O bus via the Bus Multiplexer. When the first word is accepted by the PDP-15 I/O, BR18-35 are shifted into BR00-17 by BR EN H and BR STB (A and B). Again, BR00-17 are gated onto the I/O bus and the second word is transferred to the I/O.

5.13.2 Shift Register

The Shift Register is 36-bits in length. For Write operations, the contents of the Buffer Register are loaded into the Shift Register where they are serialized and transferred to the disk.

During Read operations, the serial data from the disk are assembled in the Shift Register and then transferred to the Buffer Register.

The RP15 Shift Register is shown in Figure 5-13 and Drawings RP15-0-36, -37, and -38. The Shift Register sits between the Buffer Register and the Disk. The register is divided in half with SR STB A H clocking CD flip-flops SR00-17 and SR STB B H clocking CD flip-flops SR18-35. These strobes originate in the Shift and Longitudinal Register Control, Drawing RP15-0-15. The SR flip-flops are cleared in like manner by CLR SR A L and CLR SR B L also originating in the Shift and Longitudinal Register Control.

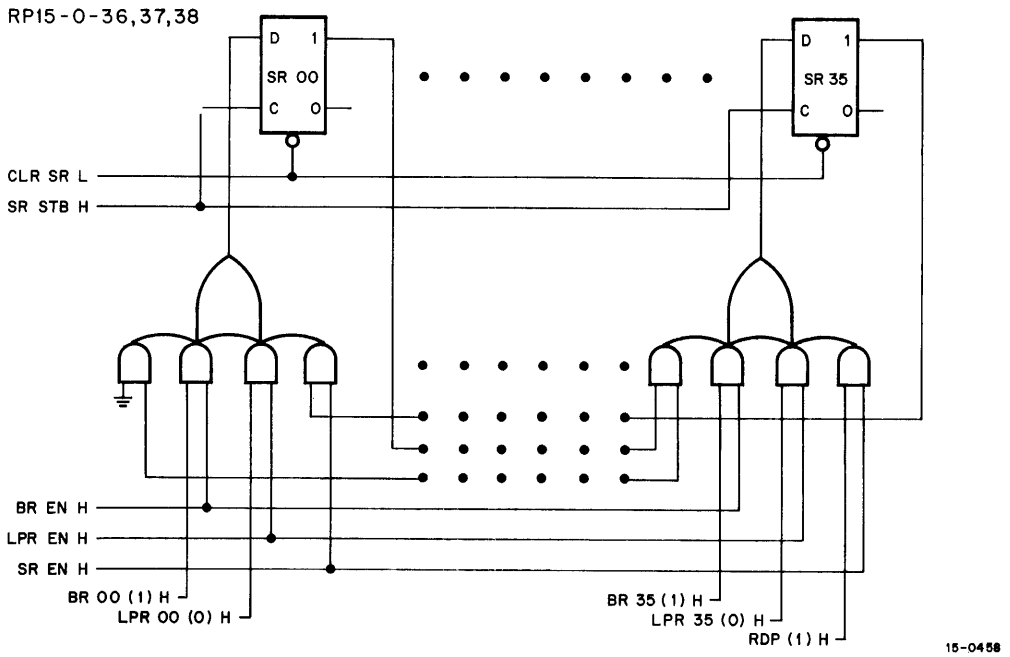


Figure 5-13 Shift Register, Simplified Diagram

Each SR flip-flop is set by an OR gate of three possible AND gate conditions. One set of AND gates looks at associated bits in the Buffer Register and is enabled by BR EN H. Another set looks at associated bits in the Longitudinal Parity Register and is enabled by LPR EN H. The third set of AND gates looks at the 1 state of the next sequential SR bit and is enabled by SR EN H. These enabling levels are generated in the Shift and Longitudinal Register Control.

In Write operations, BR bits are enabled into the register by BR EN H and strobed by SR STB A H and SR STB B H. From the register they are serialized and transferred to the disk. Serialization is accomplished by SR EN H and SR STB A and B shifting data out of the register.

During Read operations, data enters SR35 via READ DATA COAX, RD BIT flip-flop and RDP (1) H from the Read/Write Control (Drawing RP15-0-05). When all 36 bits are assembled, they are parallel-transferred to the Buffer and Longitudinal Parity Registers for further processing.

A thirty-seventh bit, which works in conjunction with the Shift Register, generates and checks word odd parity for both Write and Read operations.

5.13.3 Longitudinal Parity Register

The Longitudinal Parity Register is 36 bits long. During Write operations, each 36-bit word of the Buffer Register is transferred to the Shift Register which then exclusive-ORs the word into the Longitudinal Parity Register. At the end of each sector, the complement contents of the Longitudinal Parity Register are written on the disk. This word is actually a bit-position parity check.

During Read operations, each assembled word of the Shift Register is exclusive-ORed into the Longitudinal Parity Register. At the end of each sector, the Longitudinal Parity Register is checked for comparison with the Longitudinal Parity Word written. Note that the RP15 generates and checks both row and column parity in each sector.

The RP15 Longitudinal Parity Register is shown in Figure 5-14 and Drawings RP15-0-39, -40, and -41. The register is divided in half with LPR STB A H clocking JK flip-flops LPR00-17 and LPR STB B H clocking JK flip-flops LPR18-35. These strobes originate in the Shift and Longitudinal Register Control (Drawing RP15-0-15). The LPR flip-flops are cleared in like manner by CLR LPR A L and CLR LPR B L, which also originate in the Shift and Longitudinal Register Control.

Each LPR flip-flop is fed by an exclusive-ORing arrangement (when both the set and reset inputs of JK flip-flops are fed by the same signal, the resultant flip-flop state is the exclusive-OR of that signal). Flip-flops LPR00-17 are fed directly by SR00 (1) H through SR17 (1) H. Input to LPR18-35 is taken from individual AND gates, each of which is fed by two ORs. One group of ORs looks at SR18-35 (1) L

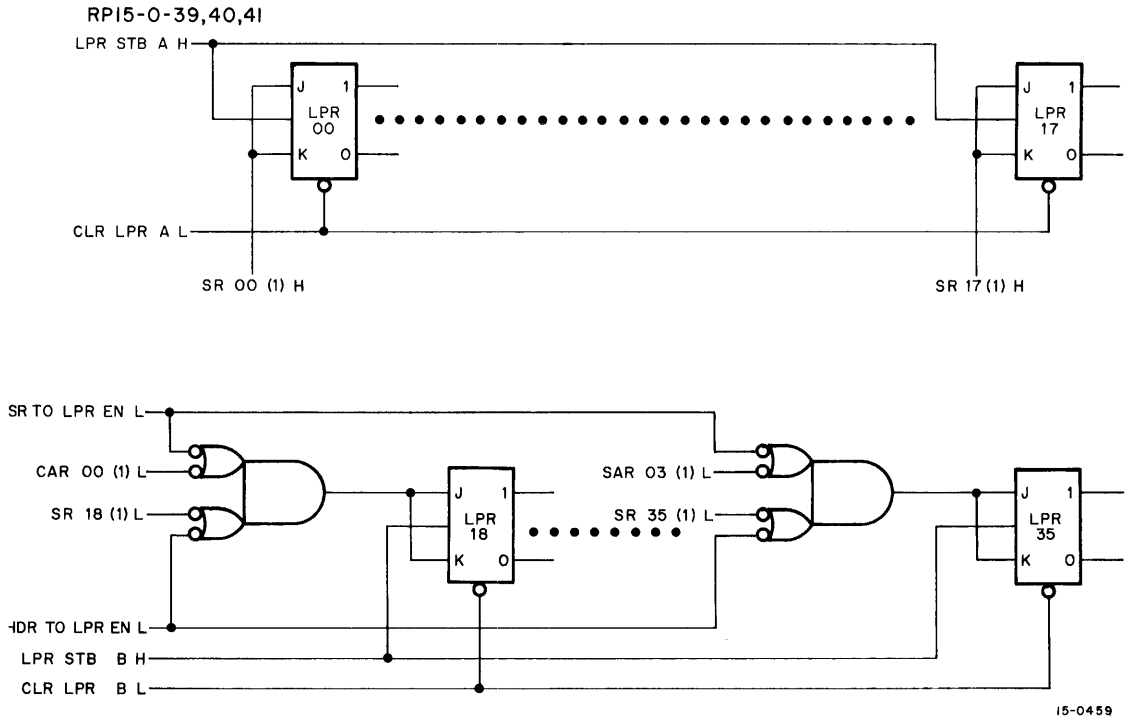


Figure 5-14 Longitudinal Parity Register, Simplified Diagram

and is enabled by SR TO LPR EN L which originates in the Shift and Logitudinal Register Control. The other group of ORs is used to look for a header and is enabled by HDR TO LPR EN L, which also originates in the Shift and Longitudinal Register Control. In these ORs, CAR00-07 (1) L are wired to LPR18-25, HAR00-04 (1) L feeds LPR26-30, and LPR32-35 looks at SAR00-03 (1) L (LPR 31 is not used in this application). The BR, SR, and LPR are shown functionally in Figure 5-1. It is important to keep in mind the data paths, especially through these registers.

5.14 CONTROLLING MAJOR STATE

The RP15 Major State Control is shown in Figures 5-16, -17, -18, -19 and Drawing RP15-0-18. For each function described in Paragraph 5.10, there are various combinations of machine states through which the RP15 must pass to complete the function, e.g., the disk must read before it writes so that it can locate the addressed sector. This circuit controls each state of the many functions performed by the controller. These states are:

IDLE
RECAL
SEEK
CLR HEAD
WRITE
INC HEAD
READ.

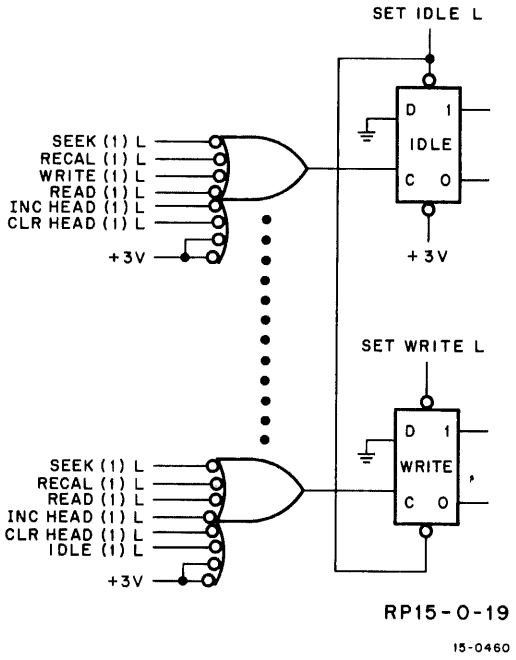


Figure 5-15 Major State Control, Simplified Diagram

For each of these states, an associated "set" pulse is generated to put the controller in that state. The states are maintained by D-Type flip-flops shown on Drawing RP15-0-19 and Figure 5-15. On the clock input of each flip-flop there is an 8-input OR gate (2 inputs unused) that ORs all the control states except the one to which that gate feeds. The data side of each flip-flop is grounded. Because of this arrangement, if any of the states at the input are set, that state is cleared. For example, if Read state is set by SET READ L on the set side of the READ flip-flop, READ (1) L goes to the OR input of all other states to produce a positive edge at their clock inputs and consequently clear all other states. In this way, the control can be in only one state at a time. Note from Drawing RP15-0-19 that SET IDLE L is tied to the Clear side of all states except Idle, in which case it is tied to the Set side. This guarantees that at Power Clear time (CLR L) the control goes into the Idle state.

The logic for SET IDLE L is shown in Figure 5-16. Six equations are ORed to produce SET IDLE L. The first is CLR L. CLR L is an OR of DPCF and I/O PWR CLR (B) L. I/O PWR CLR (B) L is generated in the PDP-15 when the processor is powered up, a CAF instruction is issued, or the I/O RESET key is pushed.

JB DN (1) L is also an input to SET IDLE L. This flip-flop (shown on Drawing RP15-0-10) is set at the completion of a transfer, or the abortion of a transfer due to some error condition. The operation of JB DN is described in more detail in the discussion of Status Control (Paragraph 5.23) and Interrupt Control (Paragraph 5.24).

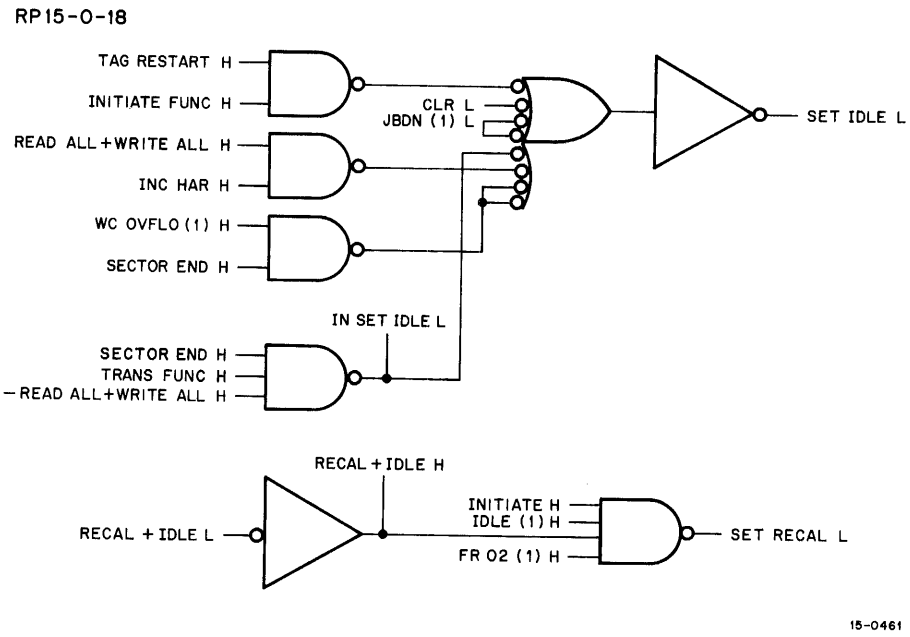


Figure 5-16 Set Idle and Set Recal Logic, Simplified Diagram

A third input to SET IDLE L is the equation:

TAG RESTART · INITIATE FUNC

Initiate-type functions only require one cycle of the Tag and Bus Line timing chain. At the completion of this cycle (TAG RESTART), the Idle state is re-entered.

A fourth input is the equation:

WC OVFLO (1) · SECTOR END

The signal SECTOR END is generated at the completion of each sector transferred. If, at the completion of a given sector, the WC OVFLO flip-flop is set, the Idle state is entered.

A fifth input to SET IDLE L is the equation:

(READ ALL + WRITE ALL) · INC HAR

This equation states that if the Function Register is equal to a Read All or Write All, and the SAR is incremented from 10_8 to 11_8 (INC HAR is generated at this time), the control must then go back into the Idle state momentarily so that the Head Register in the RP02 can be reloaded. This is done by going back to the Idle state, then into Clear Head state, and finally into Read state (or Seek, if necessary).

The last input to SET IDLE L is the equation:

$$-(\text{READ ALL} + \text{WRITE ALL}) \cdot \text{TRANS FUNC} \cdot \text{SECTOR END}$$

The first two terms in this equation eliminate all functions except Read, Write, or Write Check. For any of these three functions, Idle is entered at the end of each sector. If WC OVFLO is not set, Idle state is only entered momentarily, after which time the control goes to the Clear Head state, the Seek state (if necessary), and then to the Read state.

The logic for SET RECAL L is also shown in Figure 5-16. This signal is generated from the following equation:

$$(\text{RECAL} + \text{IDLE}) \cdot \text{INITIATE} \cdot \text{FR02 (1)} \cdot \text{IDLE (1)}$$

To set the Recal state, the RECAL + IDLE instruction must be commanded, Function Register 02 must be on a 1 (tieing it down to a Recal), the controller must be in Idle, and an initiate function pulse must be received. Because Recal is an initiate-type function, the Idle state will be re-entered 4 μs after SET RECAL L.

The logic for SET SEEK L is shown in Figure 5-17. The signal SET SEEK L is the OR of two inputs, the first of which is IN SET SEEK L. This signal is disabled when Function Register 01 equals Function Register 02, and when Function Register 00 is on a 0, which is the equation for RECAL + IDLE L. (Note that RECAL + IDLE L is equivalent to -RECAL + IDLE H.) This means that the operation requested could be Seek, Read, Write, Read All, or Write All. In all these operations, the controller may want to perform a Seek. If a Seek operation is really required depends on whether or not the cylinders compare (-CYL CMPR H), the controller has come from a Clear Head state, and whether a TAG RESTART is received.

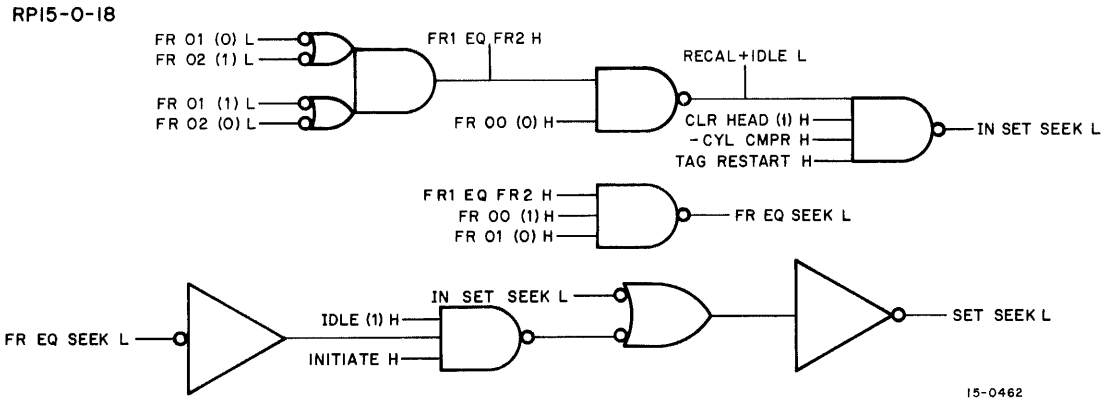


Figure 5-17 Set Seek Logic, Simplified Diagram

SET SEEK L can also be produced if the Function Register is set to the code for Seek (FR EQ SEEK L), if it is an initiate function, and if the controller is leaving the Idle state.

The Clear Head state is entered for any EXECUTE L pulse as shown on Drawing RP15-0-19. This state clears the Head Address Register in the selected RP02; this is necessary because the Head Address Register in the RP02 can only be loaded by first clearing and then jamming 1s into it. The clearing is done during the Clear Head state; the 1s jamming is done at TAG GATE 1 time of a Read state, with SET HEAD EN (see Drawing RP15-0-47).

Three types of Write functions are performed by the controller:

a. Normal write, in which a data field is written
b. Format write, in which the whole disk is formatted
c. Write All Normal, in which the header word and data fields for a particular sector are written.

Three AND gates are used to decode the Function Register, to see what type of Write is called for, and then to set the appropriate mode when it is time to do so. These gates are shown in Figure 5-18 and Drawing RP15-0-18.

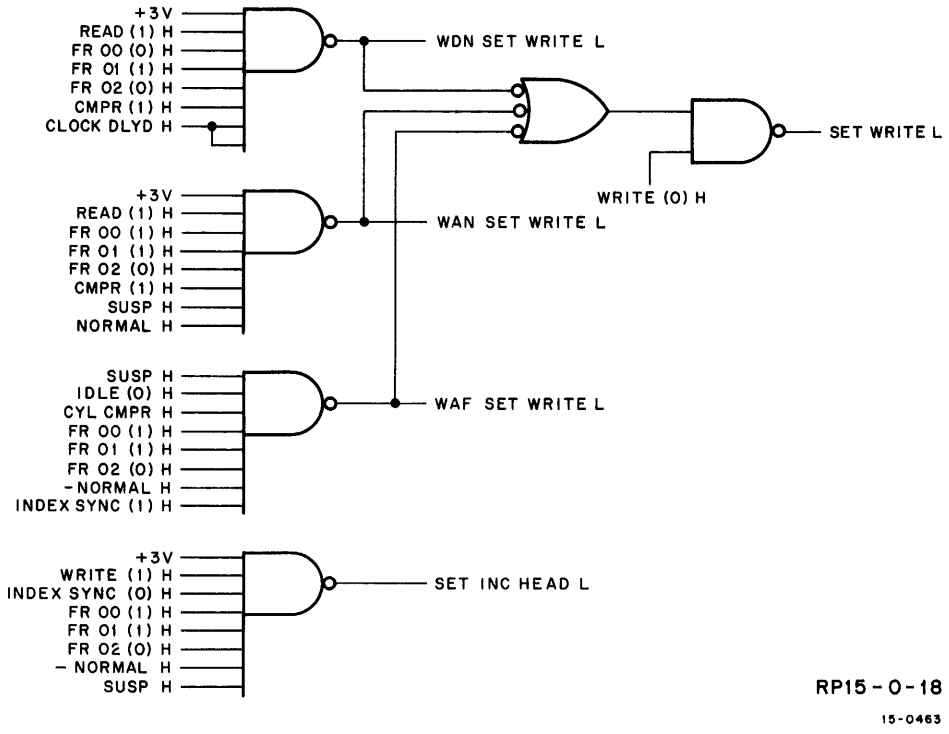


Figure 5-18 Set Write and Set Inc Head Logic, Simplified Diagram

In Write All Format mode, WAF SET WRITE L waits until the Selected Unit Sector Pulse is received before beginning to write, provided the control is not in the Idle mode and the cylinder to be formatted agrees with the Cylinder Address Register. In addition, the panel switch FORMAT/NORMAL must be in the FORMAT position (-NORMAL H) and the Index pulse must have just occurred [INDEX SYNC (1)].

In Write All Normal, WAN SET WRITE L only waits for the Sector Pulse, provided the panel switch is in NORMAL position, and the desired sector has been located in the Read state (CMPR (1) H and READ (1) H). CMPR (Header Compare) is a flip-flop that is set when the header word read from the disk agrees with that located in the CAR, HAR, and SAR.

In Write Data Normal, WDN SET WRITE L is conditioned by Read state (READ (1) H) and header compare (CMPR (1) H). However, WDN SET WRITE L is synchronized to a control timing pulse called CLOCK DLYD H. This signal is discussed in Read Data Separation, Paragraph 5.16 (see Drawing RP15-0-08).

All of the above resultant mode signals are ORed to yield a common SET WRITE L.

An additional AND gate combines conditions not unlike those for Write All Format to yield SET INC HEAD L, which is used during the formatting of the disk. These conditions are characterized by the controller being in the Write state, the Index pulse having just passed (INDEX SYNC (0) H), the Function Register = 6_8 (110 or Write All), the panel switch in FORMAT position, and the occurrence of Selected Unit Sector Pulse. During a formatting operation, the controller will shift from Idle state to Clear Head state, to Write state, then to an Inc Head state, then back to Write state, and again back to Inc Head state, and so on to the end of the cylinder. At that time, the controller will go into a Seek state so that it can move the heads over one track. Once that is accomplished, the Clear Head state will be entered for the next cylinder; this sequence repeats until the entire disk is formatted. This logic is shown in Figure 5-18 and Drawing RP15-0-18.

SET READ L is generated from the OR of two inputs (see Figure 5-19 and Drawing RP15-0-18). The first input implys that READ is entered if the function is <u>not</u> a SEEK, RECAL, or IDLE, provided the FORMAT/NORMAL switch is in the NORMAL position, the CAR equals the SUCAR (CYL CMPR H), the present state is CLR HEAD, and the Tag and Bus Line cycle for CLR HEAD is complete (TAG RESTART H). This AND gate provides the means for the controller to enter the Read state directly from the Clear Head state. This happens only when a Seek operation is not necessary.

If a Seek is required (-CYL CMPR L), IN SET SEEK will be generated to produce SET SEEK and to clear the syncrhonizing D-Type flip-flop shown in Figure 5-19. This flip-flop will remain cleared, thereby disabling the second input gate to SET READ L, until the leading edge of SU RDY H (Selected Unit Ready). When SU RDY occurs, the Seek will have been completed and SET READ is then generated. This gate is also conditioned by Seek state, NORMAL, and a function other than Seek (-FR EQ SEEK H).

RP15-0-18

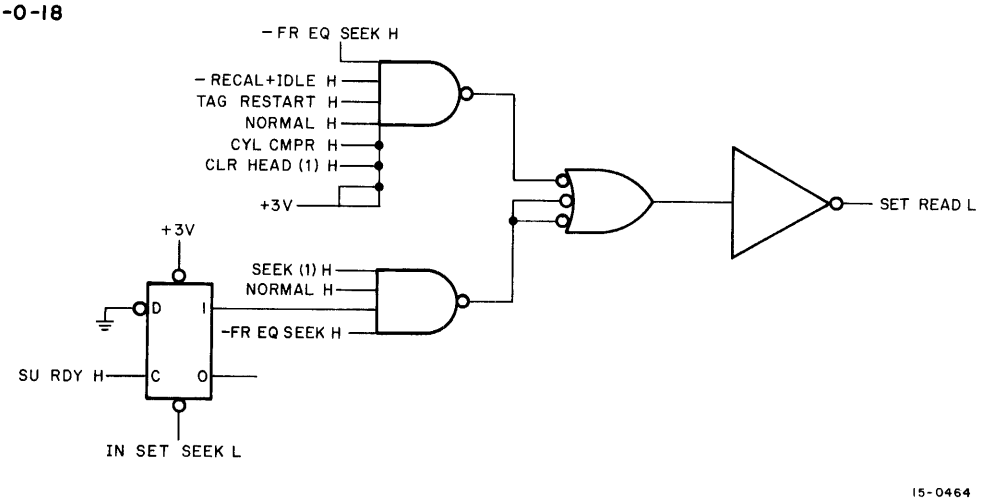


Figure 5-19 Set Read Logic, Simplified Diagram

The major state flows for each of the functions that can be performed in the RP15 are illustrated in Figures 5-20 through 5-25. The states are shown in rectangles, decision points in diamonds, comments or appropriate signals appear in ovals, and physical delays or large time lapses appear between two horizontal lines.

5.15 COMMANDING THE DRIVE (Tag and Bus Line Control)

The main function of the RP15 Tag and Bus Line Control is to control the signals sent to the disk pack and to develop the timing for the disk (see Figures 5-26 through 5-28 and Drawing RP15-0-16). It tells the drive when to read, write, move its head, increment its head, or select a different head (among other commands); commands to the drive are translated for almost every function performed by the control.

During formatting instructions, the disk begins with head zero on surface zero. At the end of that track, the control must switch to head one on surface one, etc., through the entire cylinder. This switching is done by a signal called Increment the Head Address (INC HEAD (B) L). As shown in Figure 5-26, each time this signal is issued to the input of this control, it sets a cross-latched flip-flop (made up of two OR gates) that starts a timing chain which consists of three D-type flip-flops (TAG EN, TAG 1 and TAG 2). Note that this time chain can also be initiated by EXECUTE L, SET READ L, SET WRITE L, SET RECAL L, SET SEEK L, or INITIATE L.

Setting one of these inputs will enable the M401 module, which is a 1-MHz clock. When it is enabled, the first clock sets TAG EN flip-flop and TAG 1 (10).

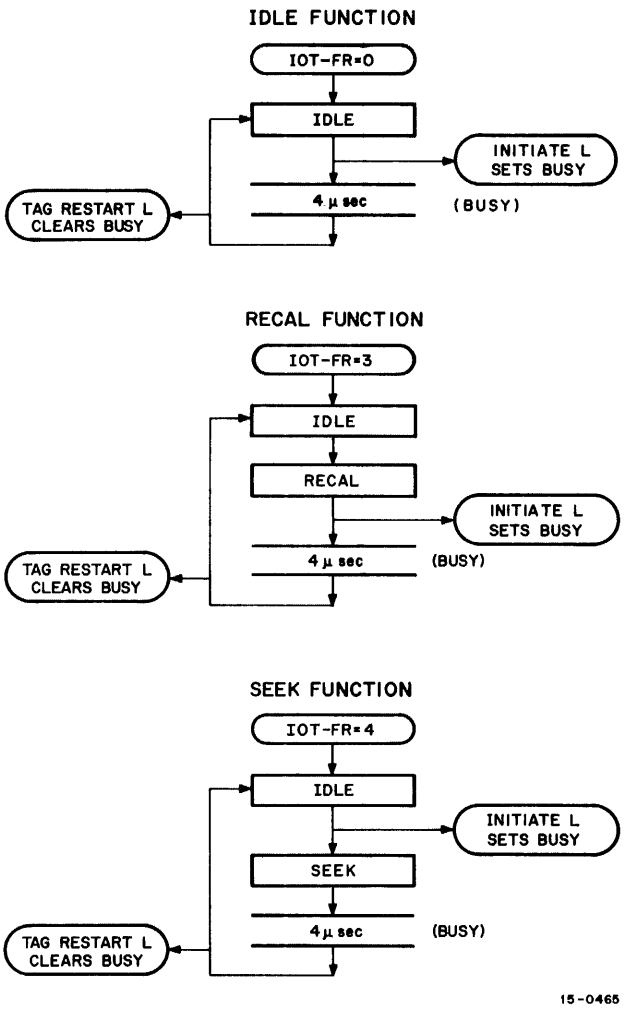


Figure 5-20 Initiate Functions, Flow Diagram

Together the two TAG flip-flops constitute a "Gray Code" counter. The second clock pulse sets TAG 2 (11), the third pulse clears TAG 1 (01), the fourth clears TAG 2 (00), and the fifth clears TAG EN. At this point, counting ceases for that cycle.

In decoding these states (see Figure 5-27), TAG 1 (1) H is delayed by 200 ns to produce TAG 1 DLYD H and L. TAG 1 DLYD H is ANDed with TAG EN (1) H to produce BUS GATE 1 L. Also -TAG 1 DLYD H is ANDed with the equation

$$\text{TAG EN (1)} + [(\text{RD} + \text{ER}) \cdot \text{TAG GATE 2}]$$

to produce BUS GATE 2 L. The purpose of this equation is explained later.

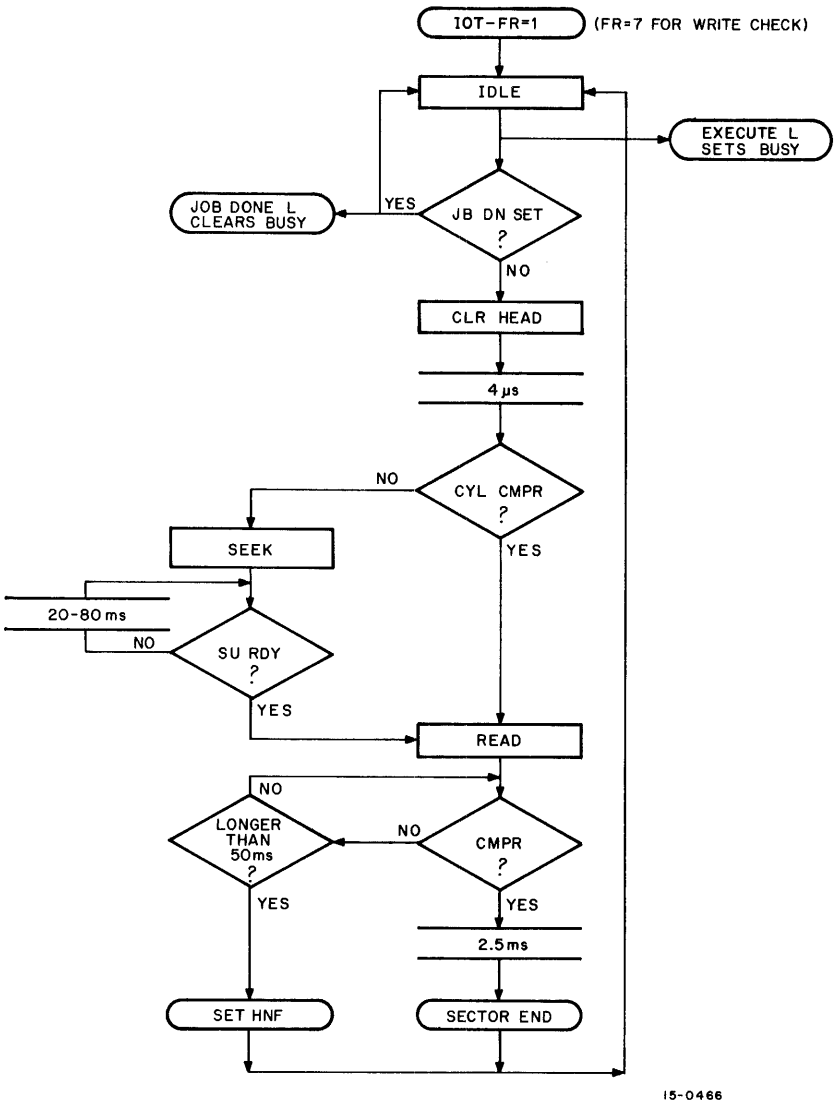


Figure 5-21 Read or Write Check Functions, Flow Diagram

TAG 1, TAG 2, and TAG EN are further decoded to produce TAG GATE 1 L and TAG GATE 2 L. These relationships are shown in Figure 5-28.

TAG 1 is delayed to guarantee that BUS GATE 1 L completely surrounds TAG GATE 1 L. If this were not done, edge triggering in the RP02 would create marginal problems. A small disadvantage of this delay is the false BUS GATE 2 L that is raised for only 200 ns (see Figure 5-28); since this is followed by a real BUS GATE 1 L, which has time to set up the Bus Cable to the RP02, no harm is done by this false pulse.

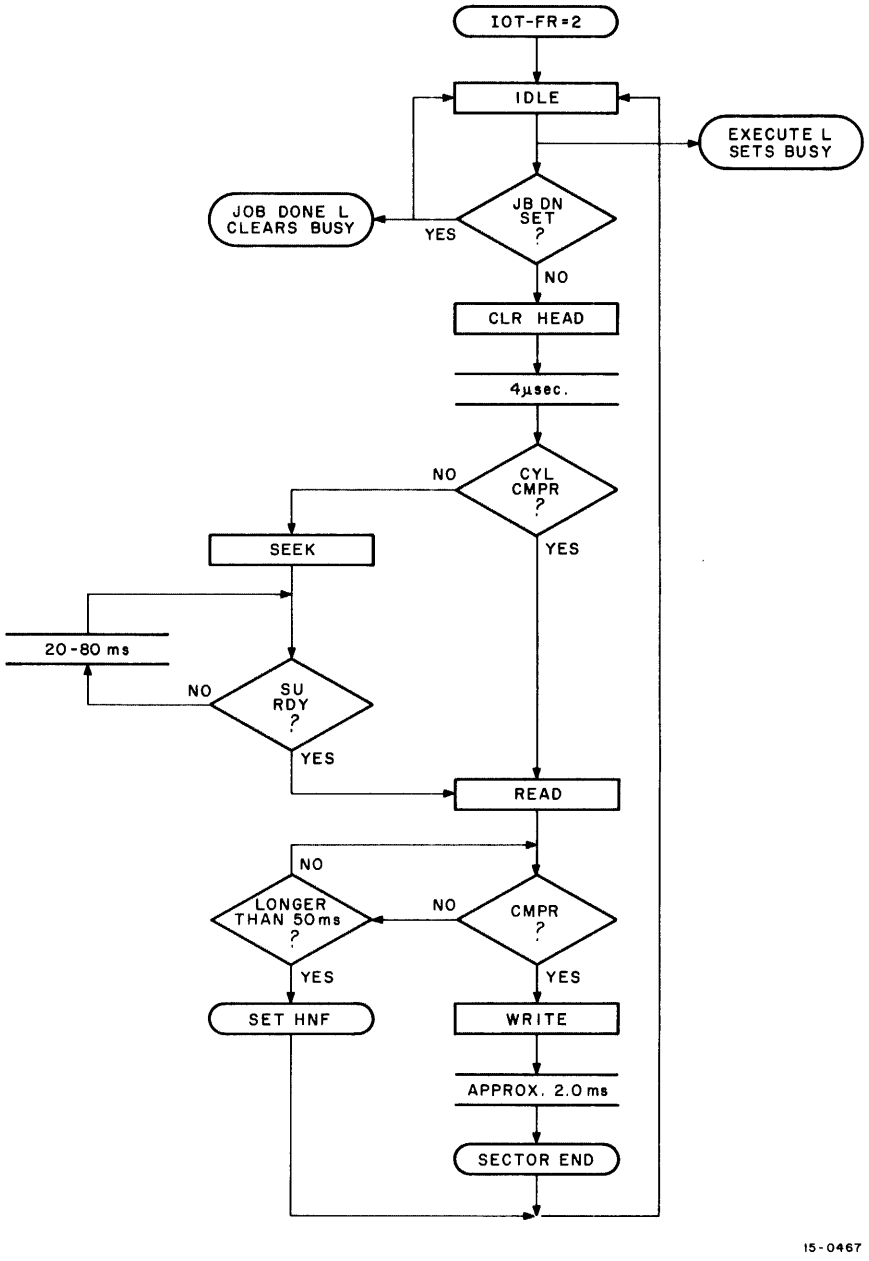


Figure 5-22 Write Function, Flow Diagram

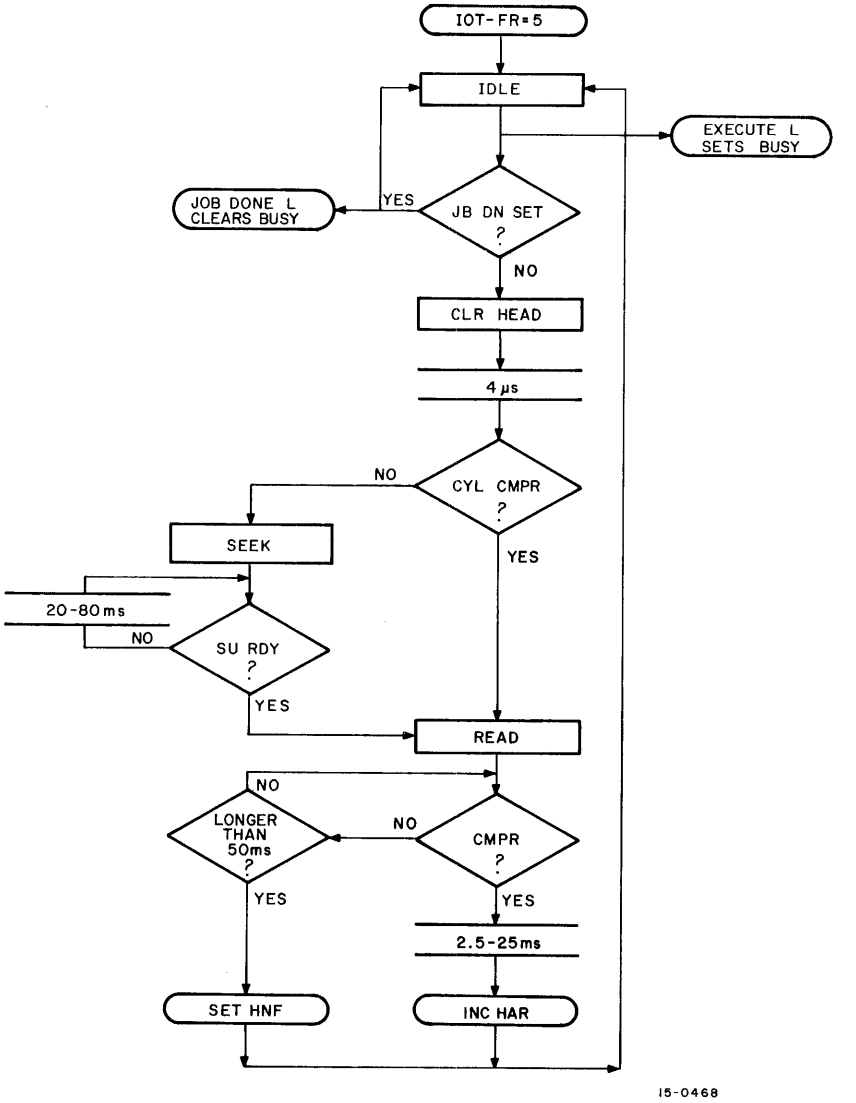


Figure 5-23 Read All Function, Flow Diagram

Four important signals now exist:

BUS GATE 1 L	(Enable)	Time 1
TAG GATE 1 L	(Strobe)	
BUS GATE 2 L	(Enable)	Time 2
TAG GATE 2 L	(Strobe)	

These signals go to the Bus Disk Drivers, which decide what signals to send to the disk drive (see Drawing RP15-0-47). The bus gates raise the bus levels first, then (after the lines have had time to settle) decoding occurs and the tag lines strobe the information down the line to the drive.

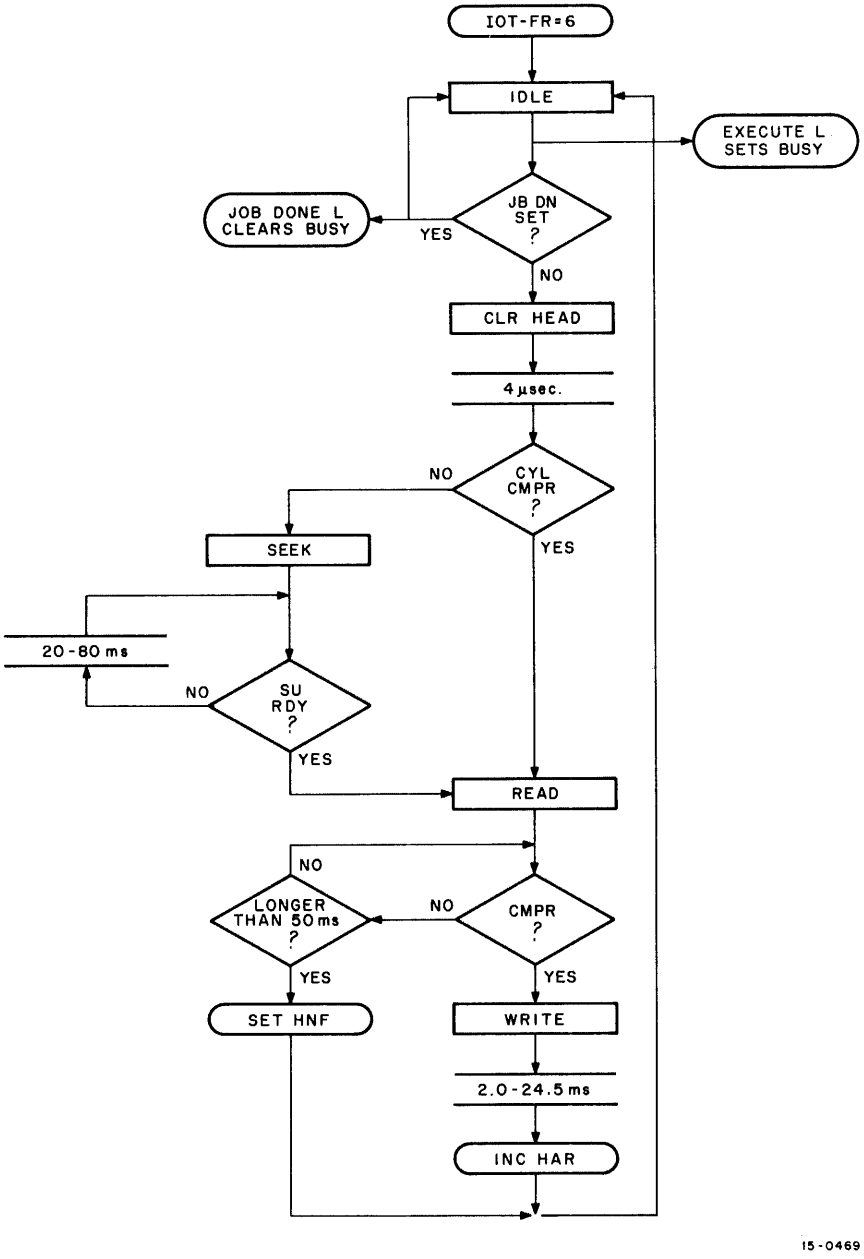
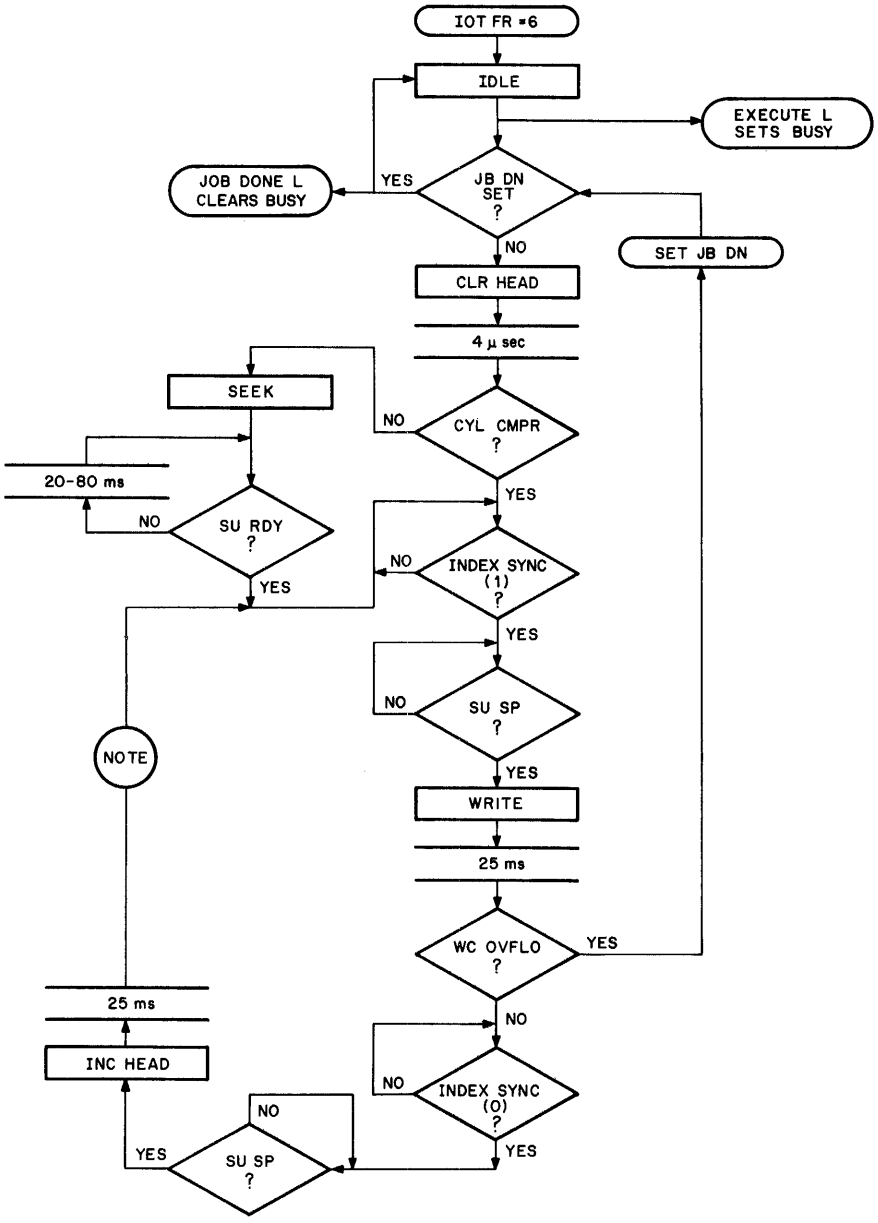


Figure 5-24 Write All Normal Function, Flow Diagram



NOTE:
If the word count register is loaded with a word count greater than 400_{10} file unsafe will be set on the 20th pass of this loop.

15-0470

Figure 5-25 Write All Format Function, Flow Diagram

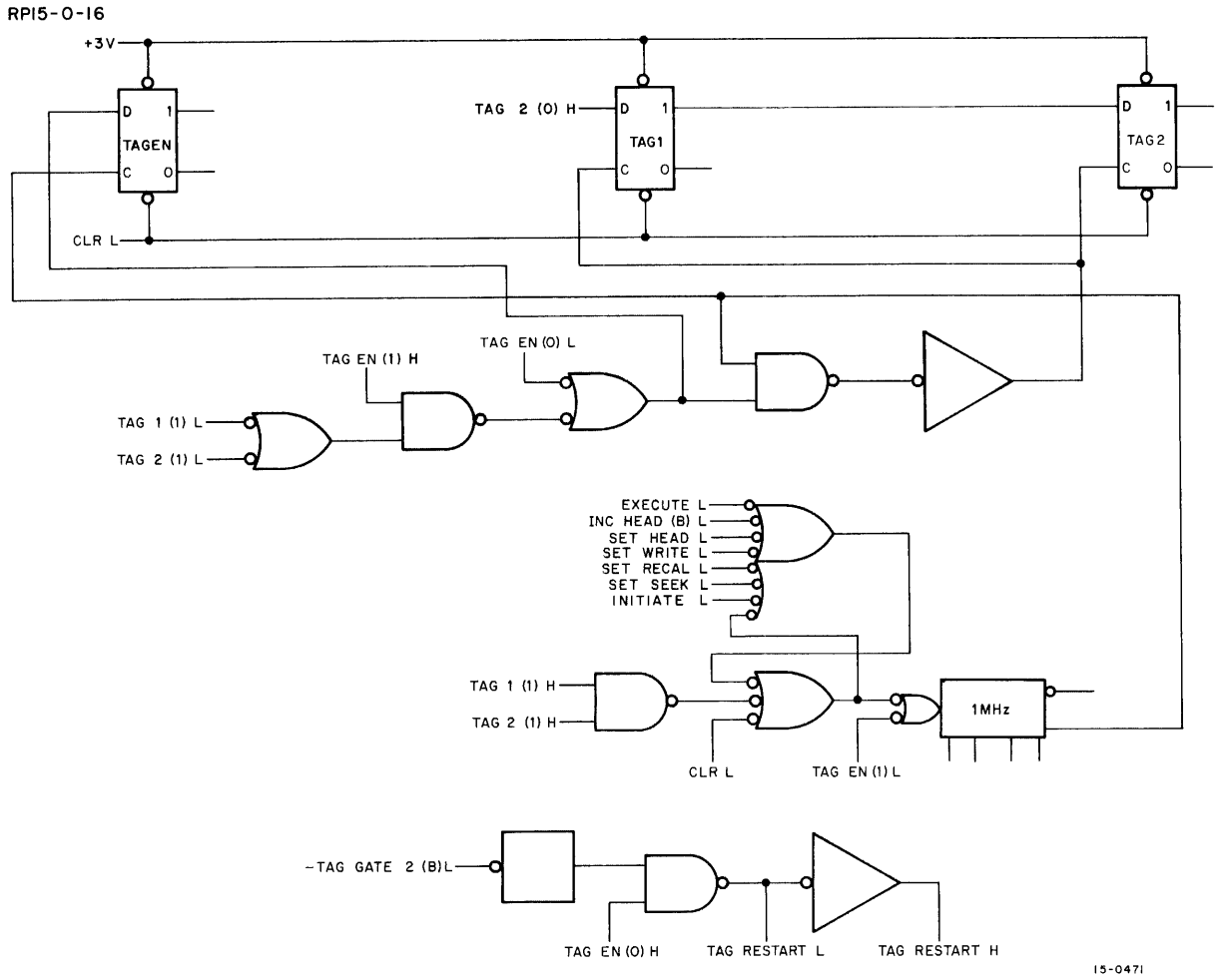


Figure 5-26 Tag and Bus Line Control, Simplified Diagram

The following signals are decoded on Drawing RP15-0-16 but are not shown in Figure 5-27:

CAR STB = SEEK (1) · BUS GATE 1
RD + ER = READ (1) + ERASE GATE (1)
HAR STB = (RD + ER) · BUS GATE 1
SET HEAD EN = (RD + ER) · NORMAL

The signal CAR STB L functions to place CAR bits 00-07 onto the RP02 Bus Cable (see Drawing RP15-0-47) at BUS GATE 1 so that they can be strobed into the RP02 Cylinder Address Register at TAG GATE 1. This is done any time it is necessary to perform a Seek operation.

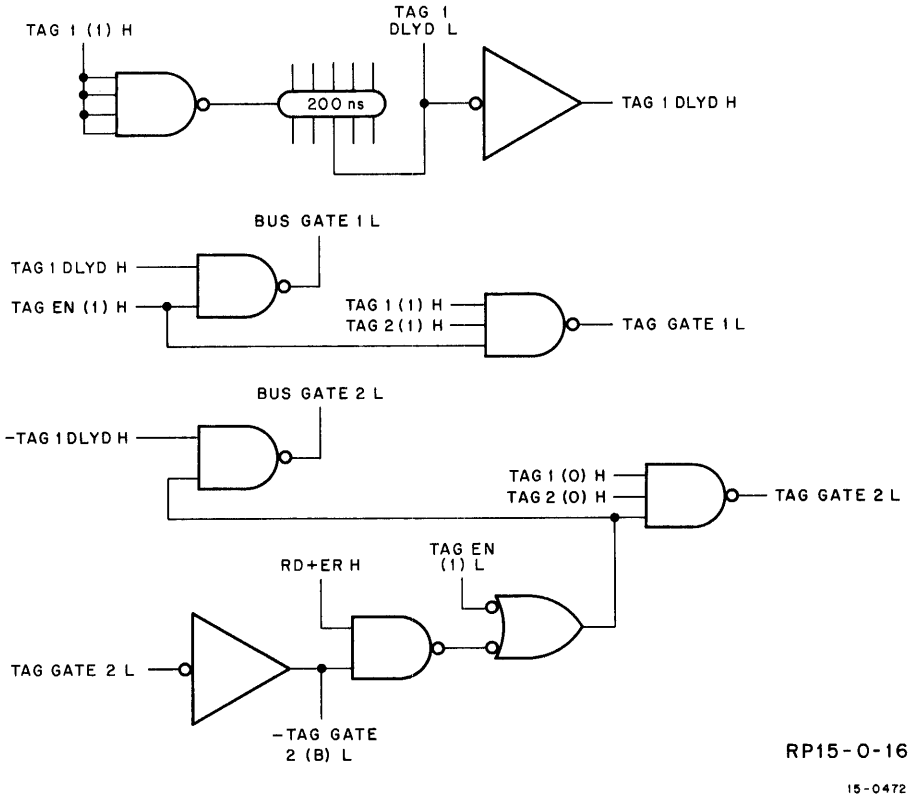


Figure 5-27 Tag and Bus Gate Logic, Simplified Diagram

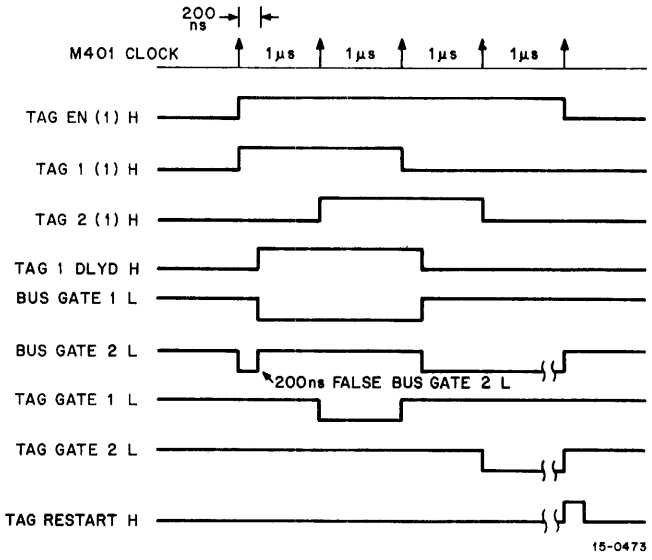


Figure 5-28 Tag and Bus Line Timing Diagram

The signal RD + ER H comes up for the duration of either a Read or a Write operation. The ERASE GATE flip-flop is set with WRITE GATE (1) L and is cleared 20 μs after the trailing edge of WRITE (1) H (see Drawing RP15-0-16); therefore, ERASE GATE is set at Write time and remains up 20 μs longer than Write.

NOTE

Because the Erase head is mounted physically behind the Write head, the Erase signal must be kept on longer to trim erase all of the track that has been written.

For all operations, with the exception of Read or Write, BUS GATE 2 L is 2-μs wide; however, during a Read or a Write (RD + ER), BUS GATE 2 L is "latched" up for the duration of the operation. The equation

$$\text{TAG EN (1)} + [(\text{RD} + \text{ER}) \cdot \text{TAG GATE 2}]$$

referred to earlier, serves this latching function.

HAR STB L places HAR bits 00-03 onto the RP02 Bus Cable (see Drawing RP15-0-47) at BUS GATE 1 so that they can be strobed into the RP02 Head Address Register at TAG GATE 1. This is done for all Read or Write (RD + ER) operations.

On Drawing RP15-0-47 SET HEAD EN L is ANDed with TAG GATE 1 L to produce SET HEAD L. SET HEAD L, in turn, is sent to the selected RP02 to strobe the information on Unit Bus 00-07 into the Head Address Register within the selected RP02. The information on Unit Bus 00-07 is HAR 00-03 which was gated there by HAR STB L.

On Drawing RP15-0-47, note that SEEK (1) is ANDed with TAG GATE 1 L to produce SET CYLINDER L. This signal is sent to the Selected RP02 to strobe the information on Unit Bus 00-07 into the Cylinder Address Register within the selected RP02. The information on Unit Bus 00-07 is CAR00-07 which was gated there by CAR STB L.

As shown on Drawing RP15-0-16, READ GATE and WRITE GATE flip-flops serve as buffering flip-flops that are set with the associated operation (Read or Write) ANDed with TAG 2 (1) H. These flip-flops remain set until the associated operation is cleared.

At the completion of each Tag and Bus Line timing cycle, a TAG RESTART H pulse is generated. The purpose of this signal is to inform the Major State Control that the cycle is complete. Usually this signal is generated 4 μs after the signal that started the cycle:

EXECUTE L
INC HEAD (B) L
SET RECAL L
SET SEEK L;

however, if the operation is a Read or a Write, then TAG GATE 2 (B) H is up for the duration of the operation (2.5 to 25 ms). The trailing edge of TAG GATE 2 (B) H generates TAG RESTART H.

5.16 READ DATA SEPARATION (VFO)

The recording technique used in the RP15 (Double Frequency NRZ) is dictated by the characteristics of the recording material used on the RP02 Disk Pack. The fact that it is a disk, and not a drum, renders the device speed-frequency sensitive, a sensitivity factor that becomes more critical as the recording head nears the center of the disk. (A drum is speed-frequency sensitive, but this sensitivity is a constant since diameter remains constant.) Add to this sensitivity the fact that any magnetizable material, is an imperfect medium, at best, due to its reluctance to change; the need for the technique used for Data Separation becomes apparent.

The disk pack system is susceptible to a phenomenon termed "pulse crowding". When a series of 1s are recorded on a track, they assume positions equally spaced from one another. If, however, a 1 bit is removed, the adjacent bits tend to fill the vacant cell. This effect is similar to lining up a series of bar magnets end-to-end. When a bar magnet located in the middle of the chain is removed, the adjacent magnets move in to fill the gap. Since the resultant locations can shift in either direction, a means must be provided to "read" through a precisely timed "window" so that the original timing may be recovered.

The RP15 uses a double-frequency, non-return-to-zero (NRZ) recording technique. A 5-MHz clock signal is divided to produce two 2.5-MHz signals with a 180° phase relationship (see Drawing RP15-0-08). When writing, the leading 2.5 MHz continuously records 1 bits on the disk surface, while the trailing signal samples the data to produce data bits. If the data to be written are continuous 0s, a 2.5-MHz signal is recorded on the disk surface. If the data to be written are continuous 1s, then a 5.0-MHz signal is recorded. Therefore, for any given data cell, the recorded frequency is either 5-MHz for a 1 data bit, or 2.5 MHz for a 0 data bit.

To recover data recorded in this manner, the 0s rate frequency component must be removed; this is done by using a phase-locked oscillator (VFO) that is similar to a sample-and-hold circuit. The VFO is capable of sampling the 0s rate pattern in the preamble of each record; phase-locking on this pattern; and then maintaining phase through the record, making only minor corrections with the use of the 0s rate component of each data cell. The VFO then removes the 0s rate component with which it is familiar, leaving only the recovered data.

The 0s rate component (2.5 MHz) removed from the Read signal is also used. This signal and its Write counterpart are the main sources of timing in the RP15 Controller. Since the RP02 has no clock track, this system provides self-clocking (see Figure 5-29).

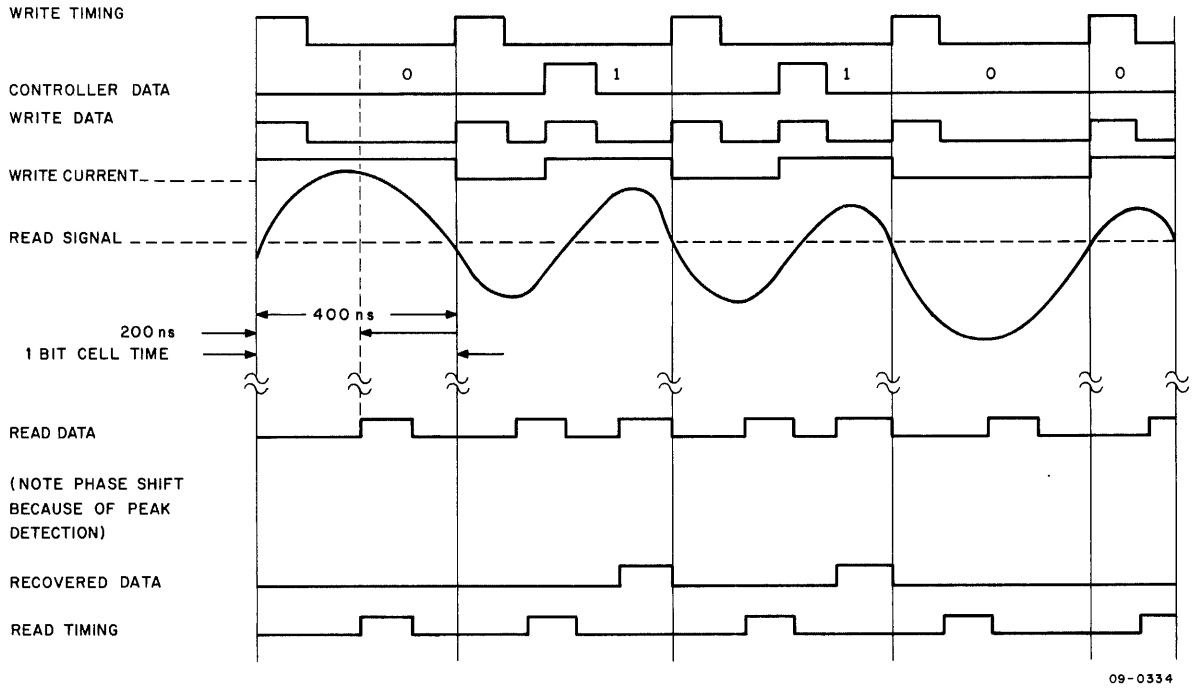


Figure 5-29 RP15/02 Read/Write Timing Waveforms

The RP15 VFO Control is shown in Figure 5-30 and Drawing RP15-0-08. The circuit comprises a 5-MHz source, an M420 Module, a frequency divider flip-flop, and associated delays and gates.

The RP02 Disk Pack has no clock track of its own; therefore, a means must be provided to record the timing on the disk with the data to be stored at the moment that data is recorded. In this way, a firm relationship between clock and data can be established at time of writing so that at time of reading that relationship can be reconstructed regardless of small differences in drive speed over a period of time.

To accomplish this recording, a format has been set up to provide a synchronization period at the beginning of each sector (see Figure 3-2) consisting of no data (continuous 0s). As shown in Figure 5-31a, this signal consists of a string of pulses recorded on the disk, at a frequency of 2.5 MHz, representing the 0s rate component. This signal determines the 1s rate component and establishes the basic timing for information to be written on the disk or read from the disk, independent of drive-speed differentials between time of write and time of read. These 2.5-MHz pulses are recorded at the beginning of each data cell throughout the format, thereby maintaining the basic timing across the entire sector.

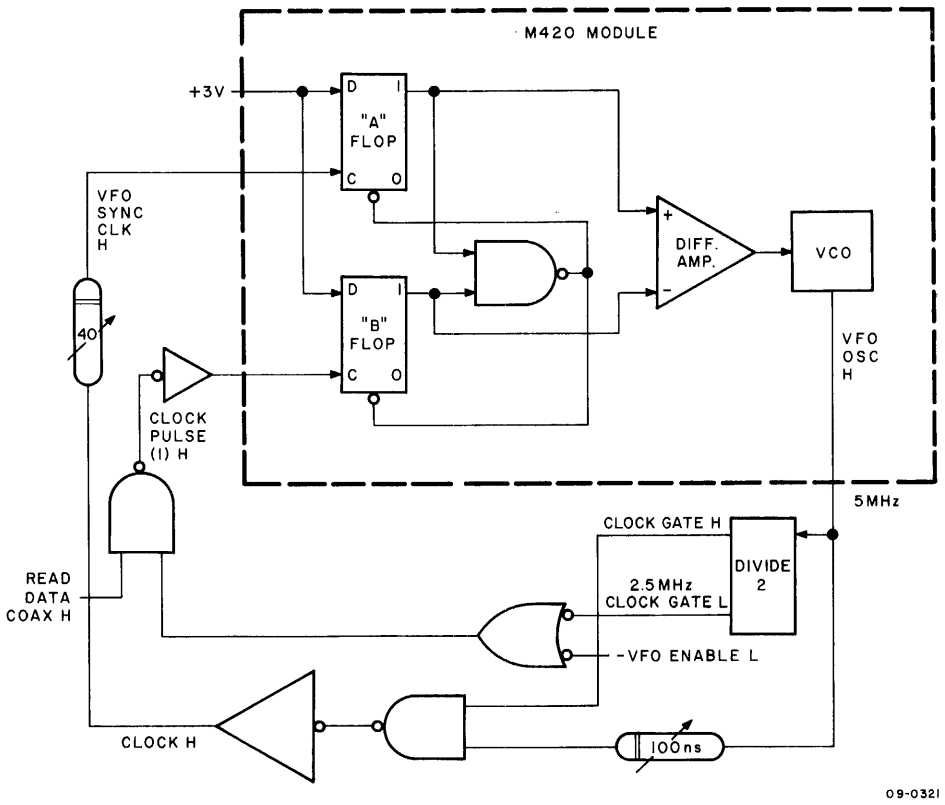


Figure 5-30 RP15 VFO Control, Block Diagram

During Write, the VFO is switched off and the synchronization area is generated in the RP15 from a self-contained crystal-controlled 5-MHz source; the output of this source is divided to produce two 2.5-MHz pulse trains, each of which bears a 180° phase relationship with each other. The leading 2.5-MHz signal produces the sync bits at the beginning of each bit cell time. The trailing 2.5-MHz signal establishes the middle of that bit cell.

The recording system used in the RP02 is termed "double-frequency non-return-to-zero (NRZ);" this is to say that the state of magnetization of the disk material does not change except when excited with a "1" bit, and then in the opposite polarity. The recording head is, in reality, a gap that constitutes discrete space; the actual shape of magnetization change will not be a square waveform, but rather some sinusoid that is an instantaneous function of field strength, field rate-of-change, gap width, surface reluctance, and drive speed (see Figure 5-31b). The waveform is a constant frequency for an all 0s data pattern, but when "1s" are introduced (c), the sync bits tend to be displaced by the data bits. It is this displacement that increases with pulse density and is described as "pulse crowding".

Because both data and sync bits can shift, when they are written and when they are read, the timing for Read must be based on a variable device that can be changed within the limits of expectable variance. The functions of the VFO are:

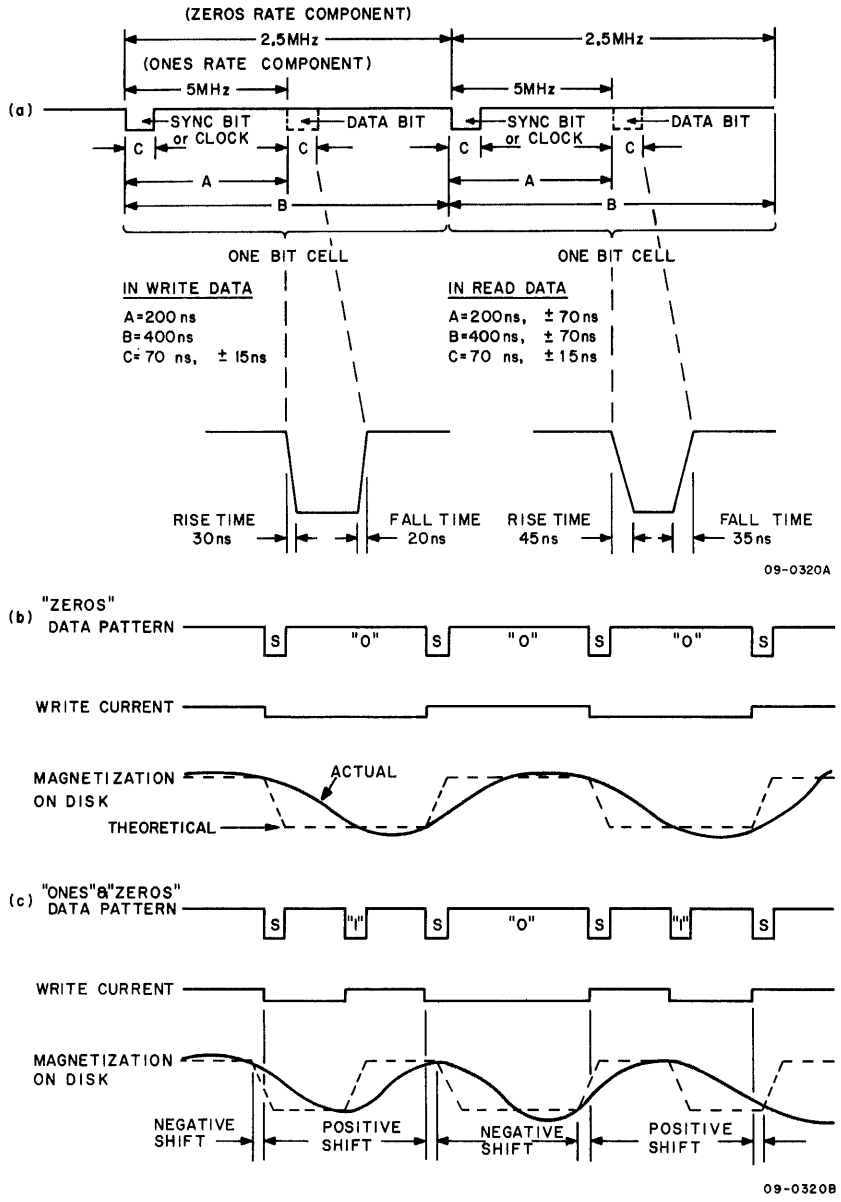


Figure 5-31 RP02 Recording Characteristics

a. To sample the incoming clock bits received from the disk

b. To establish an internal clock gate based upon the average leading edge of those clock bits

c. Set up a reading window during which the condition of data is sampled, since the data variance will be relatively the same as clock variance.

The heart of the VFO Control is the M420 Module, which is shown within the dashed lines in Figure 5-30. Basically, the module contains two D-Type flip-flops with their data inputs tied high; a clearing AND gate tied to the 1 side of both flip-flops; a differential amplifier, whose plus input

looks at the 1 side of one flip-flop and whose minus input looks at the 1 side of the other flip-flop; and a voltage-controlled oscillator, the output frequency of which is controlled by the voltage output of the differential amplifier. As configured, the circuit will reproduce a recurring input for a period of time after that input has been removed.

There are two inputs to the M420 (see Figure 5-30 and Drawing RP15-0-08). The generated clock pulse (VFO SYNC CLK H) from the VFO, which runs at approximately 2.5 MHz, sets the "A" flip-flop; the separated clock pulse (CLOCK PULSE (1) H) from READ DATA COAX H sets the "B" flip-flop. Theoretically, when both flip-flops are set, both are cleared. Figure 5-32a is a timing diagram of this operation. Assume that the frequency of clocks from the disk (CLOCK PULSE (1) H is slightly higher than VFO SYNC CLK H; the "B" flip-flop will be set longer than the "A" flip-flop and the width of its 1 state will lengthen as it sets earlier and earlier before being cleared each time the "A" flip-flop sets. In Figure 5-32b, the opposite is true when the incoming clock pulse frequency (CLOCK PULSE (1) H) is lower than VFO SYNC CLK H. In this case, the "A" flip-flop is set longer and longer as it sets earlier in the cycle. In both cases, the "A" flip-flop reaches a point where it lines up with the "B" flip-flop; at this point the cycle starts again. The up time of the "A" or "B" flip-flops will lengthen at some sinusoidal rate equal to the difference in frequency between CLOCK PULSE (1) H and VFO SYNC CLOCK H. The output width of the flip-flop whose input is lowest in frequency will be very small (close to zero); the output width of the flip-flop whose input is highest in frequency will be finite. As such, the "A" and "B" flip-flops function together as a phase detector that feeds the differential amplifier with an error voltage on the higher frequency input, whether it be "A" or "B", that is proportional to the frequency of mismatch.

The differential amplifier takes the difference of these two flip-flops, integrates that difference, and produces a plus or minus error voltage to the VFO that causes it to increase or decrease its frequency to match that which it received from the disk. At this point, an output from the M420 Module is seen; it is called VFO OSC H. This output is approximately 5 MHz and is fed through associated logic to produce DATA GATE CLOCK H, which is then tied to the DATA GATE flip-flop. The flip-flop functions to divide the output by 2, yielding two 2.5-MHz signals that are 180° out of phase with each other. The 1 state of the flip-flop is designated DATA GATE; the 0 state serves as the CLOCK GATE. The 5-MHz signal (DATA GATE CLOCK H) is also delayed approximately 100 ns to produce VFO CLOCK H which is ANDed with CLOCK GATE H, then inverted, to generate CLOCK H (see Figure 5-32c). CLOCK H occurs at a 2.5-MHz rate and falls in the middle of CLOCK GATE. Because of logic delays and the variability of circuit delays, the 100-ns delay is adjustable so that the leading edge of CLOCK H can be placed exactly in the middle of its gate. CLOCK H is further delayed approximately 40 ns to produce VFO SYNC CLOCK H which, in turn, is fed directly into the input of the M420 closing the loop.

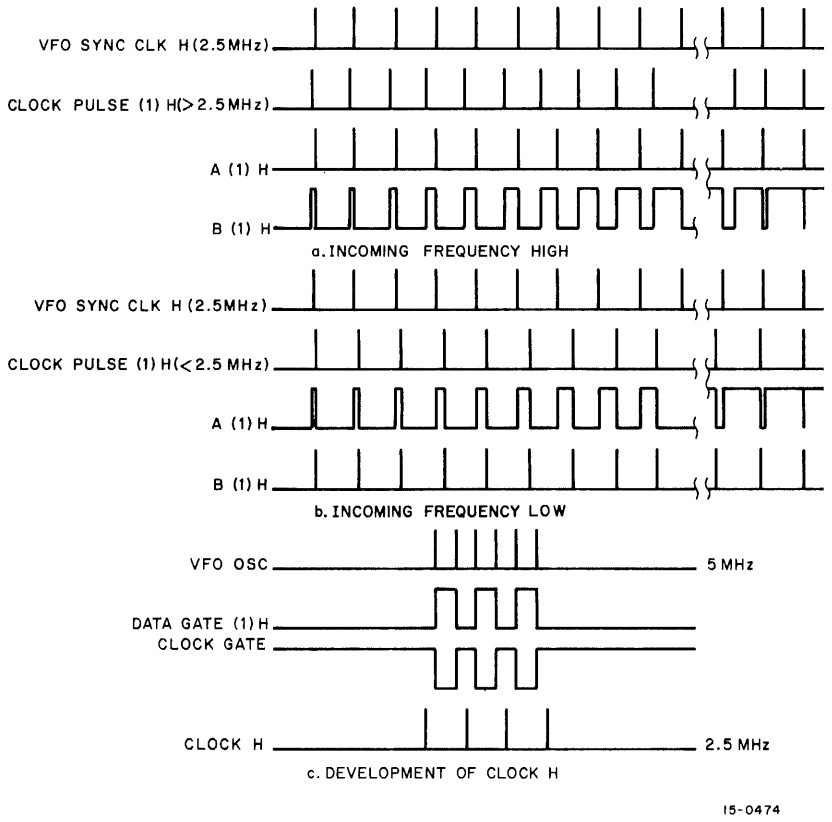


Figure 5-32 VFO Timing Waveforms

During Read, the 1109 sync bits of the preamble are fed to the VFO via READ DATA COAX H for approximately 350 to 400 μs. This is a sufficient sample to force the VFO to reproduce its input so that it can continue as a phase-locked loop through the remainder of the sector. During this synchronization period, -VFO ENABLE L is low; this allows everything on the Read Data Coax to enter the M420. Presumably this period in the format contains no data, but rather clock pulses which are then used to synchronize the VFO. Once the VFO is synchronized, -VFO ENABLE L goes high and the circuit depends on DATA GATE (0) L inverted (equal to CLOCK GATE H) to gate the Read Data Coax into the VFO. Because of the delays discussed, this occurs at the average of all clock pulses received from the disk; the VFO has essentially separated the clock pulses from the READ DATA COAX (CLOCK PULSE (1) H). In Figure 5-30, CLOCK PULSE (1) H is shown as the output of an AND gate; this is a functional equivalent to actual hardware as shown in Drawing RP15-0-08. In reality, this is the CLOCK PULSE flip-flop whose data input is the OR of either DATA GATE (0) L or -VFO ENABLE L, and is clocked by READ DATA COAX. When CLOCK PULSE sets, it clears itself, producing a pulsed input to the M420. In operation, the VFO operates similarly to a closed-loop AFC circuit. Once it is synchronized, the VFO locks in and remains in sync.

The 40-ns delay forces the clock pulses from the Read Data Coax to line up in phase with CLOCK H. Since READ DATA COAX must go through CLOCK PULSE flip-flop before entering the M420, and since CLOCK PULSE flip-flop can have a logical delay of between 0 and 50 ns, this variable delay adjusts for the difference and eliminates constant phase errors.

Relating the simplified diagram shown in Figure 5-30 to the logic schematic in Drawing RP15-0-08, the output of the M420 Module is labelled VFO OSC H. This signal is sent to an M121 where a logic decision is made as to whether or not the controller is in the Read state (WRITE or READ (0) H). If it is not, the VFO is turned off (allowed to go into saturation) and the crystal clock is used as timing for the Write state. If it is in Read state, the output of the VFO is gated through the M121 to a pulse amplifier (PA); provided the controller is not in Maintenance mode (MAINT (0) H), an output called GATED VFO OSC L will be seen at the PA. This signal is fed to M311 to input a coarse adjustment on the centering delay.

From the M311, the signal emerges as DATA GATE CLK H and is used to complement the DATA GATE flip-flop. It is further delayed through the M311, then through a 40-ns variable delay M312, to yield VFO CLOCK H; from there it enters an M627 where it is gated with CLOCK GATE H to produce CLOCK L.

NOTE

This is shown in Figure 5-30 as the output of VFO OSC H going through a 100-ns delay and being gated with CLOCK GATE. The output CLOCK L which goes into another delay gives CLOCK H, the main timing pulse.

CLOCK L is inverted to produce CLOCK H. CLOCK L is delayed by one variable 40-ns delay to yield VFO SYNC CLK H. This pulse is then fed back into the VFO closing the loop.

The other input to the VFO is CLOCK PULSE (1) H, which comes from the CLOCK PULSE flip-flop. CLOCK PULSE flip-flop can be set by any pulse on the Read Data Coax during synchronization; after sync, it can be set by a pulse from Read Data Coax, whenever DATA GATE is on a 0 L (same as CLOCK GATE on a 1). When DATA GATE is on a 0, its output will indicate CLOCK GATE H, thereby separating clock pulses from data pulses on the Read Data Coax.

The flip-flop output CLOCK PULSE (1) H is then fed through an M312 to clear itself; this is done to secure pulses from the flip-flop that are 50-ns wide (30 ns of fixed delay plus 20 ns of logic delay).

During synchronization, -VFO ENABLE L at the input of CLOCK PULSE flip-flop will make the D-input high until the VFO has synchronized. Under this condition, every pulse coming off the Read Data Coax will set CLOCK PULSE. Unless glitches exist in the Sync field, they will all be clock

pulses that are required for synchronization. Once the VFO is synchronized, -VFO ENABLE L goes high. Now CLOCK PULSE will set only when DATA GATE is on a 0 L and the clock pulses from the disk are separated.

A representative set of waveforms are shown in Figures 5-33 through 5-41.

Figure 5-33 is a photograph of the Op Amp error voltage waveform (E11V2) synchronized on CMPR (1) H (A18F1) during a Read All operation. The negative spikes represent the end of sectors; they are the result of that format area following the longitudinal parity called guard bits. This area consists of all 1s because that is what was left in the LPR when the pack was formatted. The number of guard bits written varies depending upon the room left in any one sector. The area can be as short as 20 μs or as long as 80 μs. As the Data Gate input to the VFO is disabled and the VFO is opened up to all information coming in off of the Read Data Coax, the VFO attempts to synchronize to the all 1s pattern of the guard bits which is at a 5-MHz rate. As it does, the Op Amp error signal points toward 5 MHz, a somewhat lower voltage than its nominal 4V running level.

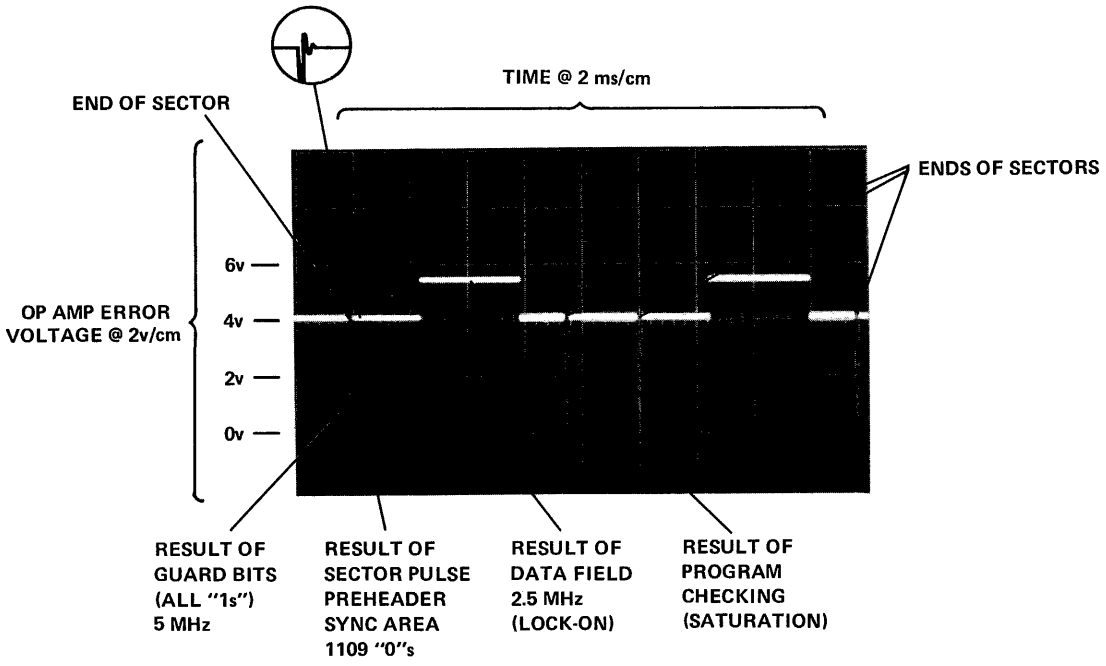


Figure 5-33 Synchronizing on CMPR (A18F1) during a Read All, Op Amp Error Voltage Waveform

When the Sector Pulse is received, the pre-header sync area is presented and the 1109 bits of zeros (a 2.5-MHz rate) cause the error voltage to return to the 4V point, where it finally locks on after a short period of overshoot and ringing.

As it locks on, the controller begins reading the data field and transferring what it is reading to memory. After 2.5 ms, the entire sector has been read and transferred. At this time, the program must check the data that have just been brought in; the controller shuts off the VFO during this period. When it is shut off, the VFO goes to its saturated level of 5.5V and stays there until checking is complete (approximately 3 ms).

When the controller completes checking the transfer, it turns the VFO back on, bringing it down out of saturation, and again starts to sync on data. In Figure 5-33, the second data field is somewhat shorter than 2.5 ms, indicating that the program turned the control on in the middle of a data field.

When the next guard bit field is seen, the error voltage spikes toward 0V, again, and returns on the next sector pulse; at that time it reads the next header. This time the VFO does not saturate; this indicates that, since this is a Read All operation, it has located the "header - 1" it is looking for. The VFO remains synchronized but passes over this data field. After the next sector pulse, the VFO reads that header and data field, saturates for checking, and starts looking for the next "header - 1".

Figure 5-34 is also a photograph of the Op Amp error voltage waveform (E11V2) synchronized on CMPR (1) H (A18F1); but this is as it appears during a normal Read operation. Once again, the negative spikes represent the ends of sectors and are the result of guard bits and sector pulses. In this instance, the controller is reading one sector out of ten. As the trace begins, the VFO is in saturation at 5.5V; then it drops to 4.0V to read a header. Since this is not the header desired, the VFO is left open and drops to a value between 2.0 and 2.5V as it follows the random bits in the data field.

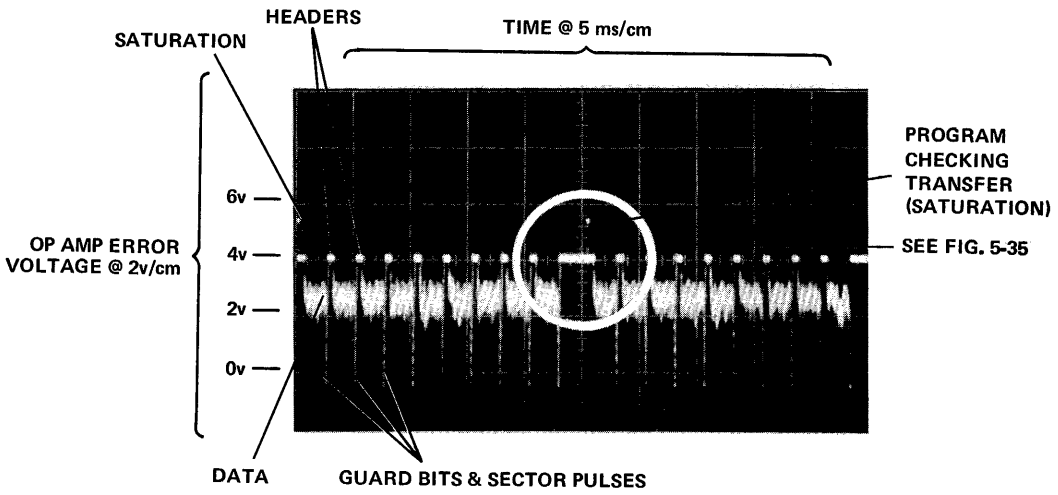


Figure 5-34 Synchronizing on CMPR (A18F1) during a Read, Op Amp Error Voltage Waveform

In this particular case, the procedure is repeated nine times until finally the controller decides that the tenth header is the field it wants. Notice that the 4.0V level is much longer now than it was for all other nine sectors, since this is the header desired and the controller remains synchronized throughout the data field for a full 2.5 ms. Following this, data are transferred into memory and the program checks the transfer, at which time the VFO saturates producing the spike up to 5.5V.

Figure 5-35 provides a closer picture of the desired header. In this photograph, the time scale has been expanded by a factor of ten to blow up the circled area in Figure 5-34. During the first centimeter, the controller has just emerged from the last data field. The spike that results from guard bits and sector pulse is seen more clearly preceding the desired header. Near the end of the second centimeter, the results of header-to-data field gap may be seen as the indeterminant contents of that area momentarily shifts the Op Amp error voltage. The data field follows with the saturation excursion during check; after check, the cycle repeats as the controller seeks the next header desired.

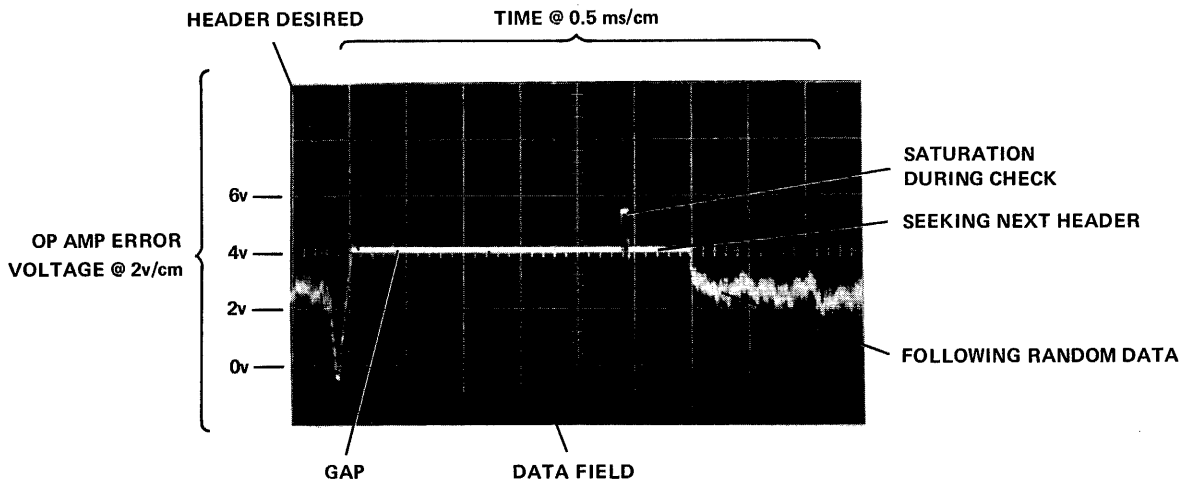


Figure 5-35 Synchronizing on CMPR (A18F1) during Read at X10 Expansion (Header Desired)

In Figure 5-36, the Op Amp error voltage is shown during a normal Write operation. This waveform can be compared to that of Read in Figure 5-34. The signals are similar; the controller remains in Read through nine sectors until it locates the header desired in sector 10. After reading the header, the VFO is turned off during the remainder of that sector, since it is not needed for writing.

As in Figure 5-35, Figure 5-37 is an expansion of the circled portion of Figure 5-36 showing location of header desired, saturation during the time the controller is writing, resynching, and seeking the next header.

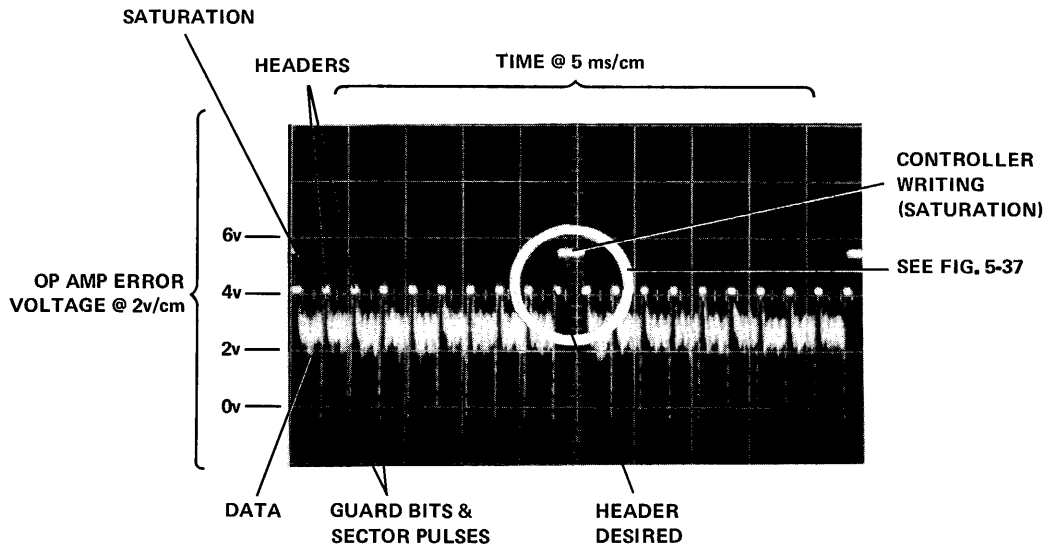


Figure 5-36 Synchronizing on CMPR (A18F1) during a Write, Op Amp Error Voltage Waveform

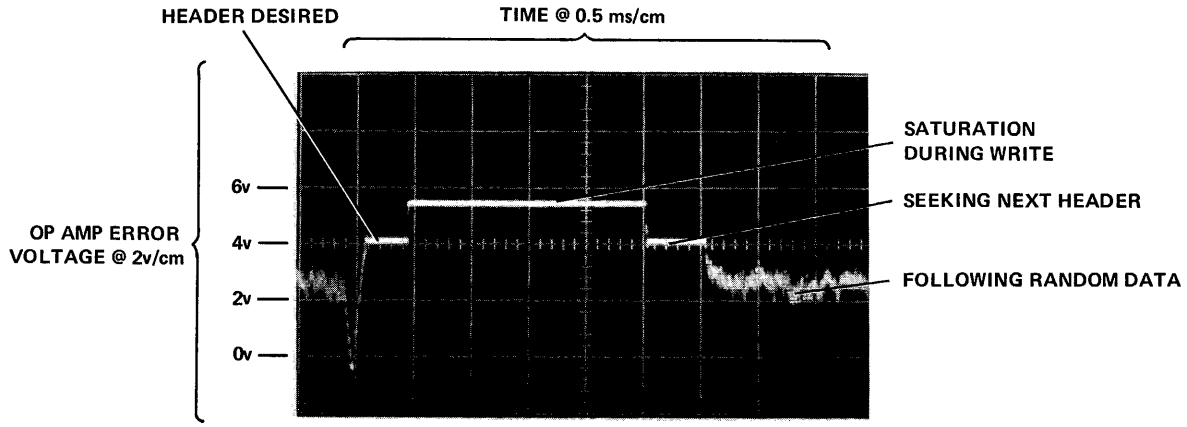


Figure 5-37 Synchronizing on CMPR (A18F1) during Write at X10 Expansion (Header Desired)

A means of determining proper VFO operation is shown in Figure 5-38; it is a dual-trace presentation of clock pulses in from the disk and clock pulses out of the VFO after they have been averaged. This is the first check a technician should make after installing a new VFO. There are no adjustments that can be made with this setup; it is merely a quick way of making certain that the circuit is operating as it should.

The top trace (F11E2) represents separated clock pulses from the Read Data Coax (CLOCK PULSE (1) H), showing at least ± 25 ns of jitter as the pulses come off the disk. The bottom trace is the averaged

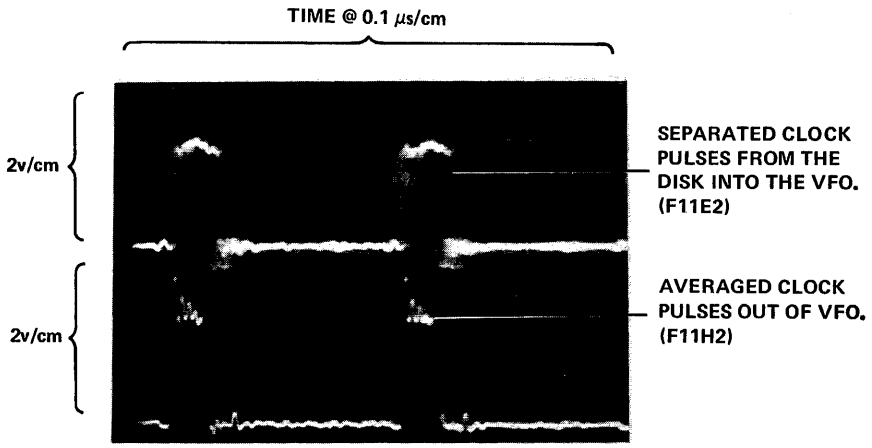


Figure 5-38 Clock Pulses In vs Clock Pulses Out, Proper Operation when Synchronizing on CMPR

clock pulses (VFO SYNC CLOCK H) out of the VFO (F11H2), created by the VFO and synchronized to the jitter pulses. This is the smoothed signal that is used both for timing and as an input to the VFO. When operating correctly, the signal's leading edge lines up with the average leading edge of the top trace.

If something is wrong in the circuit, if the signals are not in phase or if they are not equal in frequency, then one signal cannot be used to trigger the other; therefore, the illustrated waveform will not be obtained. For this reason, it is used to verify proper operation.

The dual trace in Figure 5-39 illustrates the setup used for the first adjustment in the VFO loop. The bottom trace represents raw data coming from the coax at E14B1; the top trace shows the clock pulses produced by the VFO (CLOCK H) at D17L2. This is the phase adjustment in which the leading edge of the developed clock is aligned with the average leading edge of raw data clocks. As such, it is the adjustment that removes the phase error introduced by the circuit.

Clock pulses may be distinguished from data pulse because they have no base line; data pulses, being random, will always have some base line.

When this adjustment is made, the degree of phase error must be determined. If too much delay exists in the circuit, a single wire running from D17M1 to F11H2 (VFO SYNC CLK H) can be rerouted by removing the end connected to D17M1 and connecting it to E12S2. This cuts out two gate delays and allows the variable 40-ns delay E12 to be adjusted to zero, if necessary, to achieve the desired results.

NOTE

These paragraphs are not intended to be an adjustment procedure for the VFO. To make these adjustments, refer to Paragraph 6.2.3 for specific steps to follow.

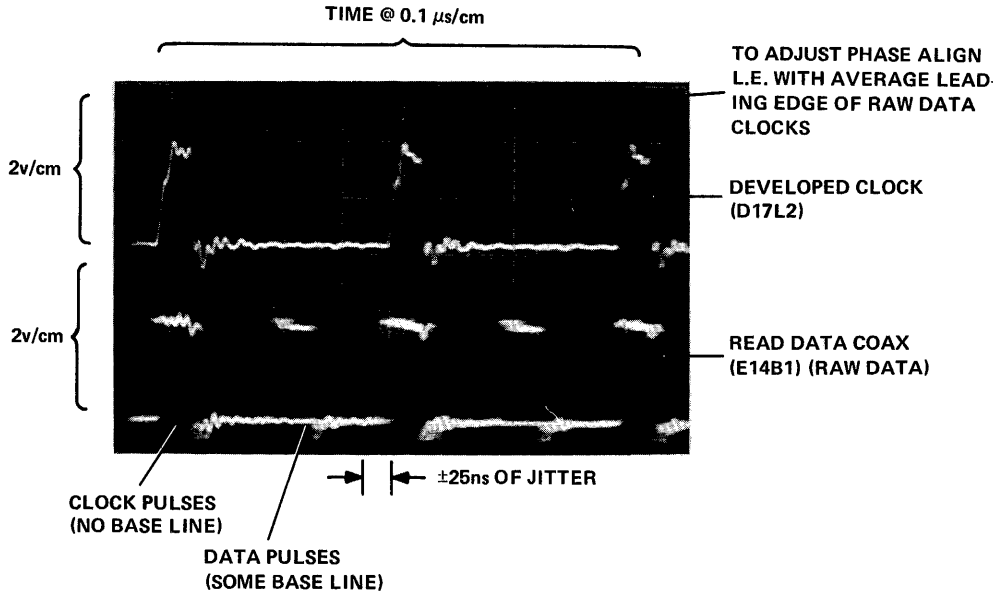


Figure 5-39 Developed Clock (D17L2) vs Read Data Coax (E14B1), Phase Adjustment

If it were determined that more than 40 ns were required, the wire run from E12F1 to D17L1 could be run from E12H1 to D17L1. This change would introduce a fixed delay of 30 ns that would add to the variable 40 ns and provide up to 70 ns of delay.

When these adjustments are made, polarities should be observed since the required signal is a high-going pulse delayed from CLOCK. Further, the tie point chosen should result in the variable delay being set near the center of its range.

Once phase adjustment is complete, the centering adjustment can be made (Figure 5-40). This adjustment centers the data and clock pulses under the data and clock gates, respectively, for best margins. Clock and data pulses are not individually adjustable for centering. If data pulses are adjusted under data gate, clock pulses are not necessarily adjusted; whereas, if clock pulses are adjusted under clock gate, data pulses will automatically fall under data gate. Since clock pulse positioning is more critical than data pulse location, the clock pulse is recommended for adjustment.

The conditions shown in Figure 5-40 occur when the oscilloscope is externally synced on D22F1 (SHIFT ENABLE (1) H), when probe No. 1 is connected to D17P1 (CLOCK GATE), and probe No. 2

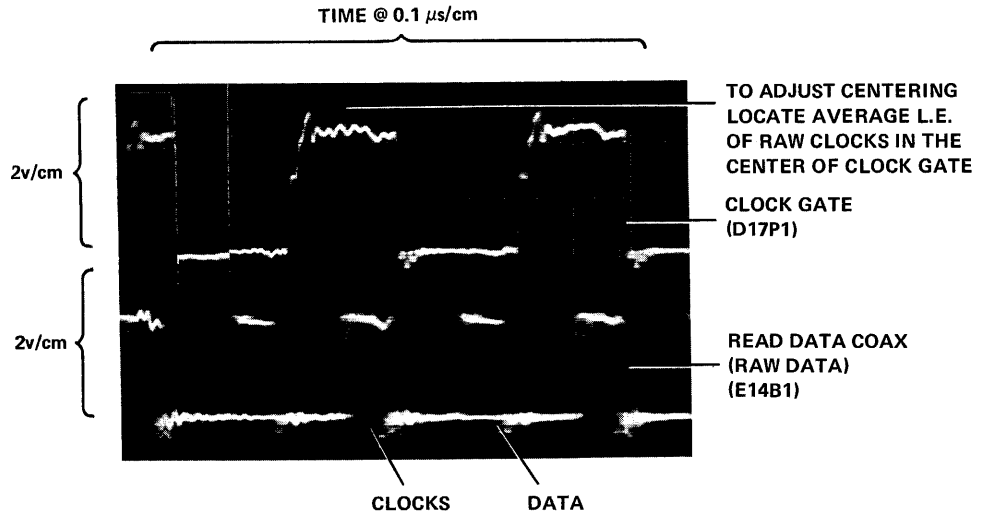


Figure 5-40 Clock Gate (D17P1) vs Read Data Coax (E14B1) during Read

is connected to E14B1 (READ DATA COAX). The associated tapped and variable delays then may be adjusted until the average leading edge of raw clock pulses (those without base line) is situated in the center of CLOCK GATE.

When this adjustment is made, the variable delay C15 is first adjusted to the middle of its range. Then, the one wire run from E14L2 (DATA GATE CLOCK) is removed from the tapped delay D06J1 and is connected to either D06H1, K1, L1, or M1; whichever one puts the waveform closest to the center of its gate. This action constitutes a coarse adjustment upon which a small variable adjustment can be made to place the pulse exactly in the center. In extreme conditions, the N1 tap can be used; in any case, a tap is chosen that allows the C15 adjustment to be fairly near the center of its range.

Figure 5-41 illustrates a visual method of identifying a particular header. By using this setup, it is possible to read the bits in any particular header and determine, by inspection, the cylinder, head, and sector designated.

The upper trace is RD BIT (1) H (C19E1), the flip-flop that separates the data from the Read Data Coax; the lower trace is RD DATA COAX (E14B1), the raw data coming from the disk. In the figure, only the last 18 bits of the header are displayed, the first 18 bits of 0s are not shown.

This display is setup by first setting the word count equal to two sectors. Then, using A delayed by B, the B sweep is externally triggered with CMPR (1) H (A18F1). The A trace is externally triggered by FIRST DATA BIT H (D23F1), and the sweep is then moved to the FIRST DATA BIT H for the second header in the two sectors. Finally, with probes 1 and 2, look at RD BIT (C19E1) and RD DATA COAX (E14B1) and expand the second header in the two-sector record.

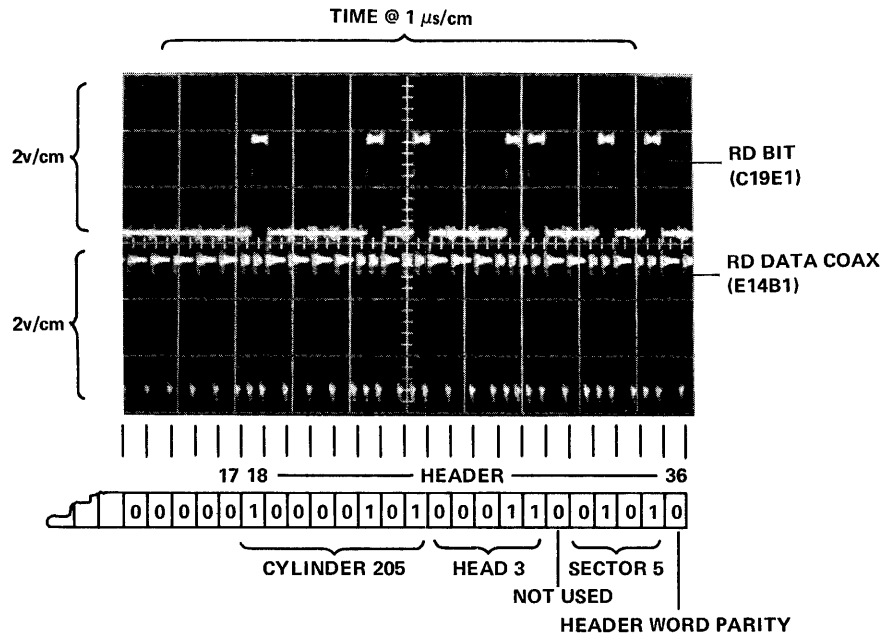


Figure 5-41 RD Bit (C19E1) vs RD Data Coax (E14B1), Identifying Header

As can be seen, the clock pulses appear regularly with occasional pulses occurring between them. Notice that directly above these clumps a bit appears on the upper trace. These are 1 bits of data as separated by the RD BIT flip-flop. Where clumps do not appear, no bit exists on the RD BIT trace; these are 0 bits of data. The constructed word format then may be decoded at sight. Reading from right to left, with each format increment right-justified, it can be determined that Header Word Parity is 0 and the sector is number 5. The next bit position, 0, is not used in RP15. Continuing to the left, Head 3 and Cylinder 205 are identified.

5.17 MAINTAINING CONTROLLER FORMAT (Write Format Generator)

The RP15 Write Format Generator is shown in Drawing RP15-0-22. The circuit contains three counting registers that keep track of the various parts of the format (Figure 3-2) during Write operations, and generate control signals to be used by the BR, SR, LPR, and R/W controls (Paragraphs 5.18, 5.19, and 5.20).

Referring to the drawing, the Write Format Generator is made up of a standard BCD counter (Flip-flops FMT GEN 05-08), two binary counters (Flip-flops FMT GEN 01-02 and FMT GEN 03-04), and an AND gate that generates FMT GEN 00 L when FMT GEN 01 or 02 are on a 1. The three registers are incremented by -INC FMT GEN L, which occurs each 37th bit of the format (once each word) during the bit cell time of Write Parity Enable (WPE (1) H) ANDed with VFO CLOCK H and DATA GATE H.

As shown in Figure 5-42, the BCD counter (FMT GEN 05-08) cycles three times through 30 words of the VFO Sync Area. The BCD counter then stops counting until cleared at Sector Pulse time by SUSP L.

WAF or WAN COUNT	WDN COUNT	Step	Format Generator Bit 00	01	02	03	04	05	06	07	08	Comments
		1	0	0	0	0	0	0	0	0	0	
		2	0	0	0	0	0	0	0	0	1	
		3	0	0	0	0	0	0	0	1	0	
		4	0	0	0	0	0	0	0	1	1	
		5	0	0	0	0	0	0	1	0	0	
		6	0	0	0	0	0	0	1	0	1	
		7	0	0	0	0	0	0	1	1	0	
		8	0	0	0	0	0	0	1	1	1	
		9	0	0	0	0	0	1	0	0	0	
		10	0	0	0	0	0	1	0	0	1	10th Sync Word
		11	0	0	0	0	1	0	0	0	0	
		12	0	0	0	0	1	0	0	0	1	
		13	0	0	0	0	1	0	0	1	0	
		14	0	0	0	0	1	0	0	1	1	
		15	0	0	0	0	1	0	1	0	0	VFO Sync Area
		16	0	0	0	0	1	0	1	0	1	
		17	0	0	0	0	1	0	1	1	0	
		18	0	0	0	0	1	0	1	1	1	
		19	0	0	0	0	1	1	0	0	0	
		20	0	0	0	0	1	1	0	0	1	20th Sync Word
		21	0	0	0	1	0	0	0	0	0	
		22	0	0	0	1	0	0	0	0	1	
		23	0	0	0	1	0	0	0	1	0	
		24	0	0	0	1	0	0	0	1	1	
		25	0	0	0	1	0	0	1	0	0	
		26	0	0	0	1	0	0	1	0	1	
		27	0	0	0	1	0	0	1	1	0	
		28	0	0	0	1	0	0	1	1	1	
		29	0	0	0	1	0	1	0	0	0	
		30	0	0	0	1	0	1	0	0	1	30th Sync Word (Pre-header)
		31	1	0	1	1	1	0	0	0	0	Header Word (5,6,7,8 Stop Counting)
	1	32	1	1	0	0	0	0	0	0	0	←WDN Begins Here
	2	33	1	1	0	0	1	0	0	0	0	VFO Data Sync
	3	34	1	1	0	1	0	0	0	0	0	
	4	35	1	1	0	1	1	0	0	0	0	Last Post-header Sync
	5	36	1	1	1	0	0	0	0	0	0	←(All Bits Stop Counting)
	133	164	1	1	1	0	0	0	0	0	0	Data Field
				BIN CT		BIN CT		BCD COUNT				

Figure 5-42 Write Format Generator Count

The binary counter (FMT GEN 03-04) increments each time the BCD counter is full, i.e., on the 10th, 20th, and 30th sync word when FMT GEN 05 and 08 are both on a 1. On the 30th sync word, FMT GEN 03, 05, and 08 are all set by the process just described. These three conditions ANDed yield the signal PRE HEADER L that conditions 02 for setting and generates Write Sync Bit Enable (WSBE H). This signal says "we are writing the last word of one of the sync areas," and is used to force a 1 bit at parity time, as described in the R/W Control, Paragraph 5.20.

On the next increment (Step 31), the Header Word is written on the disk, FMT GEN 03-04 step to a binary 3, FMT GEN 02 is set, and Format Generator Bit 00 is raised (FMT GEN 00 L).

FMT GEN 03 and 04 now increment four times to produce the VFO Data Sync Area, and on the next increment stop counting (as the format enters the Data Field) until it also is cleared upon receipt of SUSP L.

In Step 32, FMT GEN 01 and 02 increment to a binary 2 and stay there until Step 35, when the conditions for LAST POST HEADER SYNC L are met:

FMT GEN 01 (1) H
FMT GEN 02 (0) H
FMT GEN 03 (1) H
FMT GEN 04 (1) H.

LAST POST HEADER SYNC L increments FMT GEN 01-02 to a binary 3, and generates WSBE H once again to force a 1 bit at the end of the VFO Data Sync Area.

On the next increment (Step 36), the disk enters the data field. FMT GEN 01-02 are both set and FMT GEN 03-04 are reset.

Note that the data field is decoded by conditions FMT GEN 00 H and FMT GEN 1 + 2 L; when -FMT GEN 1 + 2 H is present, the disk is decoding everything else but a data field.

NOTE

The + sign used here and on the drawing does not mean OR, but rather FMT GEN 1 "and" 2 L.

The process just described occurs whenever the control is in either a Write All Format (WAF) or a Write All Normal (WAN) mode. In Write Data Normal (WDN) mode, the count begins at Step 32, with the receipt of WDN SET WRITE L. The resultant signal, WDN CNT L, is used to preset FMT GEN 01 flip-flop.

The conditions in Steps 5/36 prevail throughout the rest of the format, through Steps 133/164, and reset upon receipt of the next sector pulse SUSP L.

5.18 CONTROLLING TRANSFER DIRECTION IN THE PDP-15 (BR and DCH Control)

The RP15 BR/DCH Control is shown in Drawings RP15-0-13 and -14. This circuitry interfaces the RP15 to the PDP-15 Single Cycle Break facility and develops timing for memory.

Referring to Figure 5-43, during Read, when a full word is in the Shift Register, it is transferred to the Buffer Register; at that time, the control will raise a break (BK RQ) request. When the request is granted, the first 18 bits of the Buffer Register are transferred to memory; the last 18 bits of the Buffer Register are shifted into the first 18-bit positions of the Buffer Register and are then transferred to memory in two back-to-back breaks.

During Write, after a word has been shifted out onto the disk, another word is taken from the Buffer Register; at that time, a break request is raised for memory access so that two more words may be transferred from memory. When access is granted, memory will transfer 18 bits into bit positions 18-35 of the Buffer Register. These bits will be shifted into bit positions 0-17, and another 18-bit word will be transferred from memory into bit positions 18-35 of the Buffer Register.

The Buffer and Shift Registers are both 36-bit registers; on every transfer, in or out, two 18-bit words must be transferred at a time. The direction of transfer, in or out (IN = into memory, OUT = out of memory), is decoded by the following equations (see Figure 5-44):

$$\text{(OUT)} \quad -\text{RQ IN} = \text{FR01 (1)} \cdot \overline{\text{TRANS FUNC}}$$
$$\text{(IN)} \quad \text{RQ IN} = \text{FR01 (0)} + \text{TRANS FUNC}$$

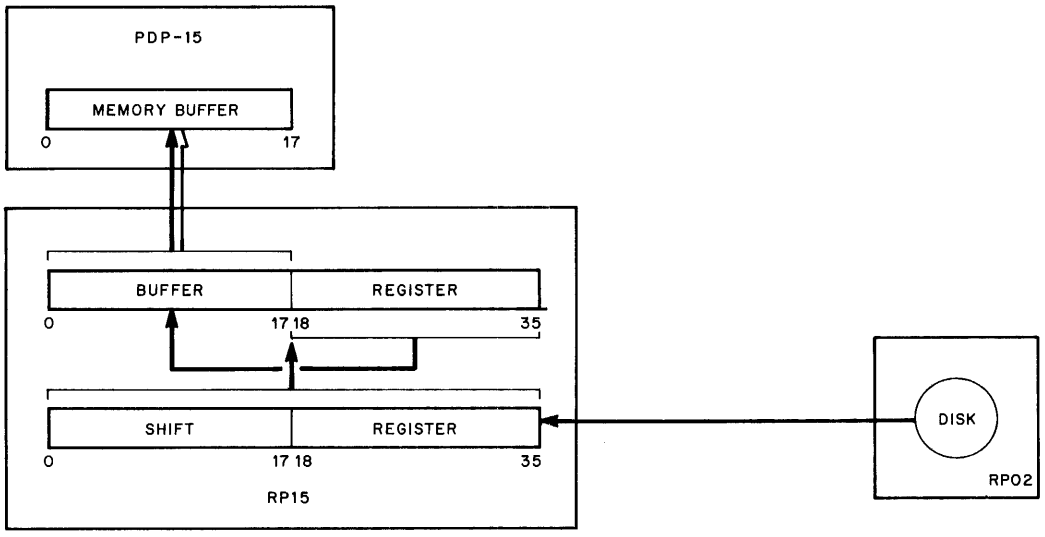
Examining the OUT equation first, the equation states that the function must have a 1 in FR01 leaving the following functions:

Write	2
Recal	3
Write All	6
Write Check	7

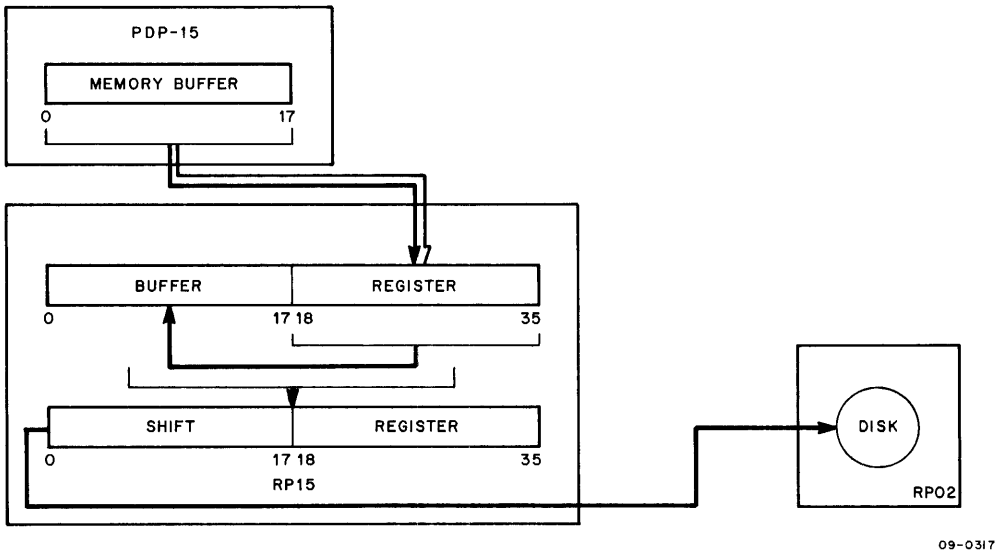
Further, the equation states the function should be a transfer function; that immediately eliminates Recal. It can be seen, then, that an OUT transfer is only necessary for functions that appear as Write functions to memory (Write Check appears as a Write function to memory and a Read function to the disk).

Inspection of the IN equation shows that is is the NOT condition of the OUT equation, and that all functions are included except Write, Write All, and Write Check.

Note that even initiate functions are included in this equation; this is acceptable since the direction of transfer signal is recognized only when a transfer is taking place, which means that the function



a. DATA FLOW DURING 'READ'



b. DATA FLOW DURING 'WRITE'

Figure 5-43 BR/DCH Data Flow

would be a transfer or execute type. This is done by ANDing RQ IN L with DCH RQ (1) L to produce DCH RQ L, which is interpreted in the PDP-15 I/O as the direction of transfer.

When an OUT transfer function is executed, general flow is from the BR to the SR. The flow is indicated by three signals called:

FORMAT BR TO SR
FIRST BR TO SR
BR TO SR.

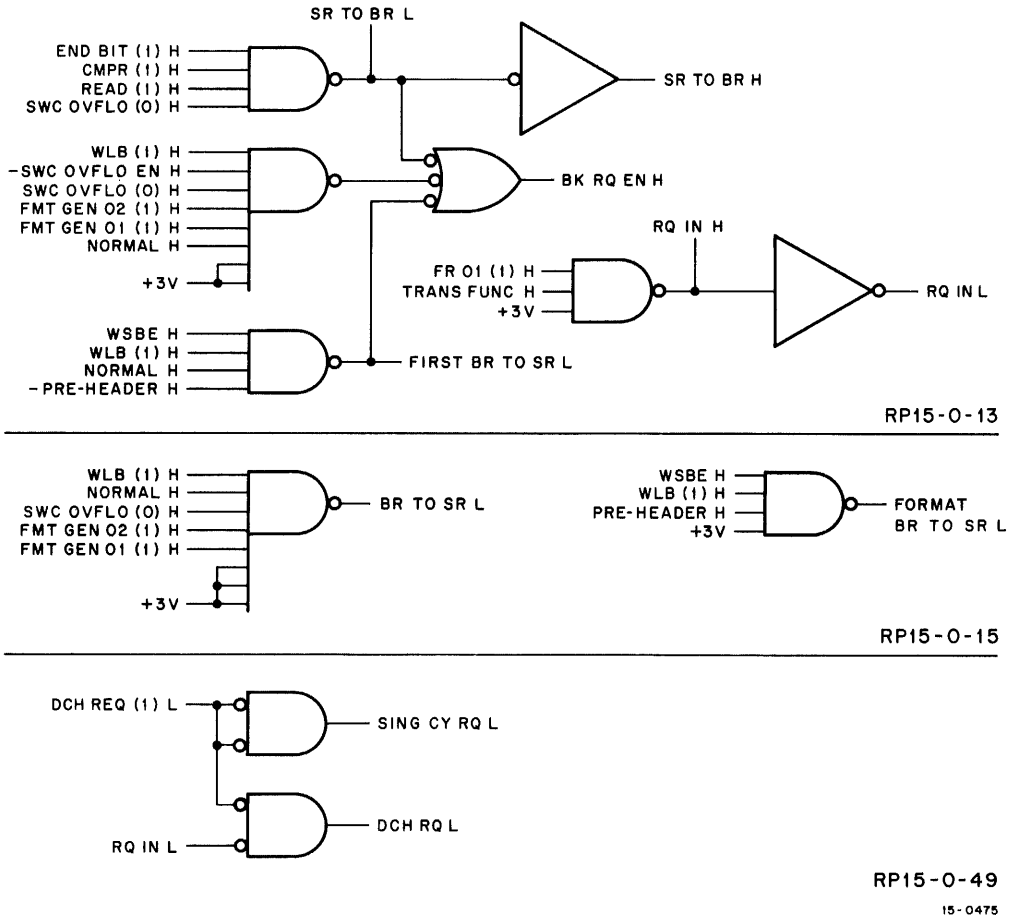


Figure 5-44 BR Control Logic, Simplified Diagram

The signal FORMAT BR TO SR is generated during Write All Normal or Write All Format functions and serves to transfer the header word from the BR to the SR. The signal is expressed as:

$$\text{FORMAT BR TO SR} = \text{WSBE} \cdot \text{WLB(1)} \cdot \text{PRE-HEADER}$$

The WLB (Write Last Bit) signal (created on Drawing RP15-0-06) is present for 400 ns during the time the last bit (bit 35) of each word is being written. The WSBE (Write Sync Bit Enable) signal (created on Drawing RP15-0-22) is present for the duration of the last word written in both the VFO Sync Area (see Figure 3-2) and the VFO Data Sync Area. PRE-HEADER is generated on Drawing RP15-0-22 and inverted on Drawing RP15-0-07. This signal is decoded as all words written prior to the header word.

FORMAT BR TO SR is generated during the writing of the last bit before the header word for both Write All Normal and Write All Format Instructions; it transfers the header word from the BR to the SR when necessary.

The signal FIRST BR TO SR is similar to FORMAT BR TO SR except that it is conditioned by -PRE-HEADER and NORMAL. The signal is expressed as:

$$\text{FIRST BR TO SR} = \text{WSBE} \cdot \text{WLB(1)} \cdot \text{NORMAL} \cdot \overline{\text{PRE-HEADER}}$$

Conditions WSBE, WLB(1), and -PRE-HEADER qualify the gate for the last bit (bit 35) written in the VFO Data Sync Area before the first data word. NORMAL eliminates Write All Format functions because the data field for this function does not come from memory. This equation transfers the first data word in the Data Field from the BR to the SR for Write and Write All Normal functions.

The signal BR TO SR is also similar to FORMAT BR TO SR in that it includes WLB (1) and NORMAL in its equation:

$$\text{BR TO SR} = \text{WLB(1)} \cdot \text{NORMAL} \cdot \text{SWC OVFLO (0)} \cdot \text{FMT GEN 01 (1)} \cdot \text{FMT GEN 02 (1)}$$

The ANDing of FMT GEN 01 (1) (Format Generator) with FMT GEN 02 (1) decodes the Data Field (see Drawing RP15-0-56 or Figure 5-42). SWC OVFLO (0) excludes the Longitudinal Parity Word; the equation then leaves a means to transfer all but the first data word from the BR to the SR for Write and Write All functions.

When an IN transfer is executed, general flow is from the SR to the BR, as indicated by SR TO BR L, which can be expressed as:

$$\text{SR TO BR L} = \text{END BIT (1)} \cdot \text{CMPR (1)} \cdot \text{READ (1)} \cdot \text{SWC OVFLO (0)}$$

READ (1) indicates that the applicable functions are Read, Read All, and Write Check. CMPR (1) eliminates the header word (compare is set after the reading of the header word) and SWC OVFLO (0) eliminates the Longitudinal Parity Word. END BIT is a signal that is present for 400 ns during the time the word read from this disk is completely assembled in the SR. This equation transfers the SR to the BR for Read and Read All functions.

NOTE

The SR is not transferred to the BR for Write Check functions; this condition is later gated out.

Signals SR TO BR L and FIRST BR TO SR L are also two of the three inputs that create BK RQ EN H. The third input is generated from the equation:

$$\text{WLB(1)} \cdot \overline{\text{SWC OVFLO EN}} \cdot \text{SWC OVFLO (0)} \cdot \text{NORMAL} \cdot \text{FMT GEN 01 (1)} \cdot \text{FMT GEN 02 (1)}$$

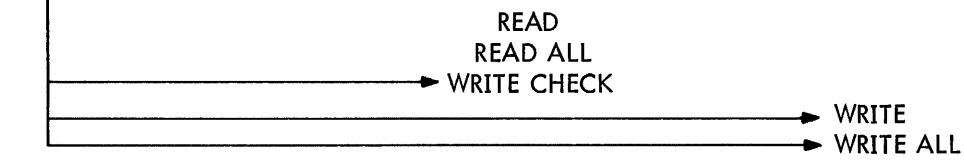
Note that this equation is identical to BR TO SR with the addition of -SWC OVFLO EN. The latter is the NOT of the AND condition of all SWC bits on a 1. This condition occurs when the next to the last word is being read or written. In the case of BR TO SR, the signal SWC OVFLO EN means that the next to last word is being written and the last word is already in the BR; therefore, there is no need for another BK RQ in this sector. If the word count is not zero, then the next word will be requested at the beginning of the next sector.

Before a transfer can be made to or from memory, a Break Request (BK RQ) must be raised. BK RQ is set by SET RQ L, which is generated from the OR of three inputs as shown in Figure 5-45. The first input is called INIT RQ L (Initial Request). This signal supplies the RP15 Buffer Register with the first (or initial) data word(s) for OUT transfers. BK RQ for the remaining data words is self-generating after the initial BK RQ is generated. OUT transfer functions comprise the following:

Write
Write All (Normal)
Write Check.

From the logic in Figure 5-45, the following equation for INIT RQ L can be written:

$$\overline{\text{RQ IN}} \cdot \text{NORMAL} \cdot \text{WC OVFLO (0)} \cdot [\text{CMPR(1)} \cdot \text{FR02(1)} + \text{LAST POST HEADER SYNC} \cdot \text{FR02(0)} \cdot \text{WDE(1)}]$$



Note in the first expression inside the brackets that all odd functions that can result in CMPR (1) are included. Read and Read All, however, are eliminated because they are RQ IN functions. In the second expression, all even functions that can result in Last Post Header Sync are included; also, the function must be in NORMAL mode. This equation only leaves the functions Write, Write All Normal, and Write Check for which it produces the BK RQ for the first data word transferred from memory in each sector.

The second input to SET RQ L is generated from the equation:

$$\text{WPE(0)} \cdot \text{PRE-HEADER} \cdot [\text{READ ALL} + \text{WRITE ALL}]$$

PRE-HEADER was described earlier as the time in which the last word of the VFO Sync Area is written. WPE is generated on Drawing RP15-0-06 and is up for 400 ns of each word written during the time the word parity bit is being transferred to the disk. (Note that since the operation is a Write, Read All is excluded.) The timing for this operation is such that an output from this equation is produced at the

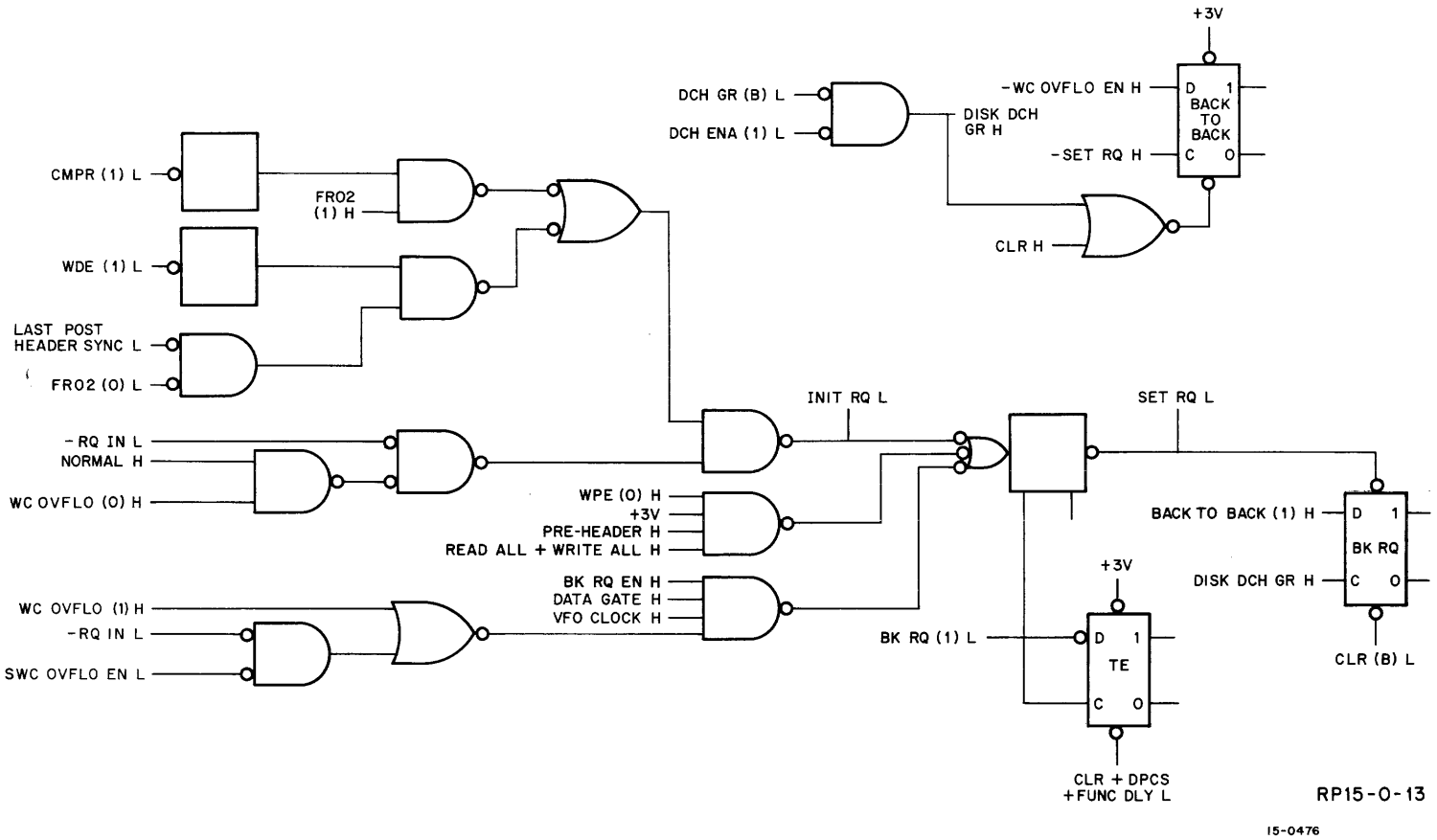


Figure 5-45 DCH Control Logic, Simplified Diagram

trailing edge of the WPE signal that is generated for the Second to Last VFO Sync Area word (i.e., 14.0 μs before the first bit of the header is written).

The third and final input to SET RQ L is given by the equation:

$$\text{BK RQ EN} \cdot \text{DATA GATE} \cdot \text{VFO CLOCK} \cdot \text{WC OVFLO (0) [RQ IN} + \overline{\text{SWC OVFLO EN}}\text{]}$$

DATA GATE and VFO CLOCK only synchronize BK RQ with Read and Write timing. From the expression in the brackets, the function must either be an IN transfer or an OUT transfer, provided that SWC OVFLO EN is not true. This equation produces BK RQ signals for all words transferred in Read and Read All functions and for words 2-128 of Write and Write All Normal functions.

SET RQ L direct sets BK RQ as shown in Figure 5-45, which enables the D-input of DCH REQ. The trailing edge of SET RQ L (-SET RQ H) is used to strobe the C-input of BACK TO BACK. If at this time -WC OVFLO EN H is true ($\overline{\text{WC = all ones}}$), then BACK TO BACK is set. This condition is true when two or more words remain to be transferred. If, however, the last word of an odd word count (only one word) is all that remains, BACK TO BACK is not set.

A short time after BK RQ (1), the PDP-15 I/O will respond with a DCH GR (B) H which generates DISK DCH GR H and clears BACK TO BACK (if set). If BACK TO BACK is set, the first DISK DCH GR H will keep BK RQ set and another break is requested that will result in a second DISK DCH GR H. The second DISK DCH GR H will then clear BK RQ. If BACK TO BACK were not set when the first DISK DCH GR H arrived, then BK RQ would have been cleared at that time.

In short, if two or more words are left, BACK TO BACK is set to request two successive breaks. If only one word remains, BACK TO BACK is not set and only one break is requested. BACK TO BACK and BK RQ are cleared with CLR.

TE (Timing Error) is a flip-flop that is set if a break request is still up (BK RQ (1) L) from a previous SET RQ L when the condition for a new SET RQ L exists. The output of the PA, which strobes the C-input of the TE flip-flop, is actually the output of the three input OR gate (see Figure 5-46). TE is cleared with CLR + DPCS + FUNC DLY L.

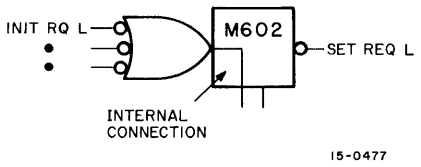


Figure 5-46 TE Strobe Logic, Simplified Diagram

Referring to Figure 5-47, another function of SET RQ L is to direct set BRS SYNC (Buffer Register Shift Sync). The purpose of BRS SYNC is to determine when it is time to shift BR18-35 into BR00-17. As shown in Figure 5-43, this happens for IN transfers after the first 18 bits (BR00-17) have been accepted by memory. The trailing edge of DISK DCH GR H (-DISK DCH GR L) fires a PA which is enabled by DCH ENA (1) H to produce

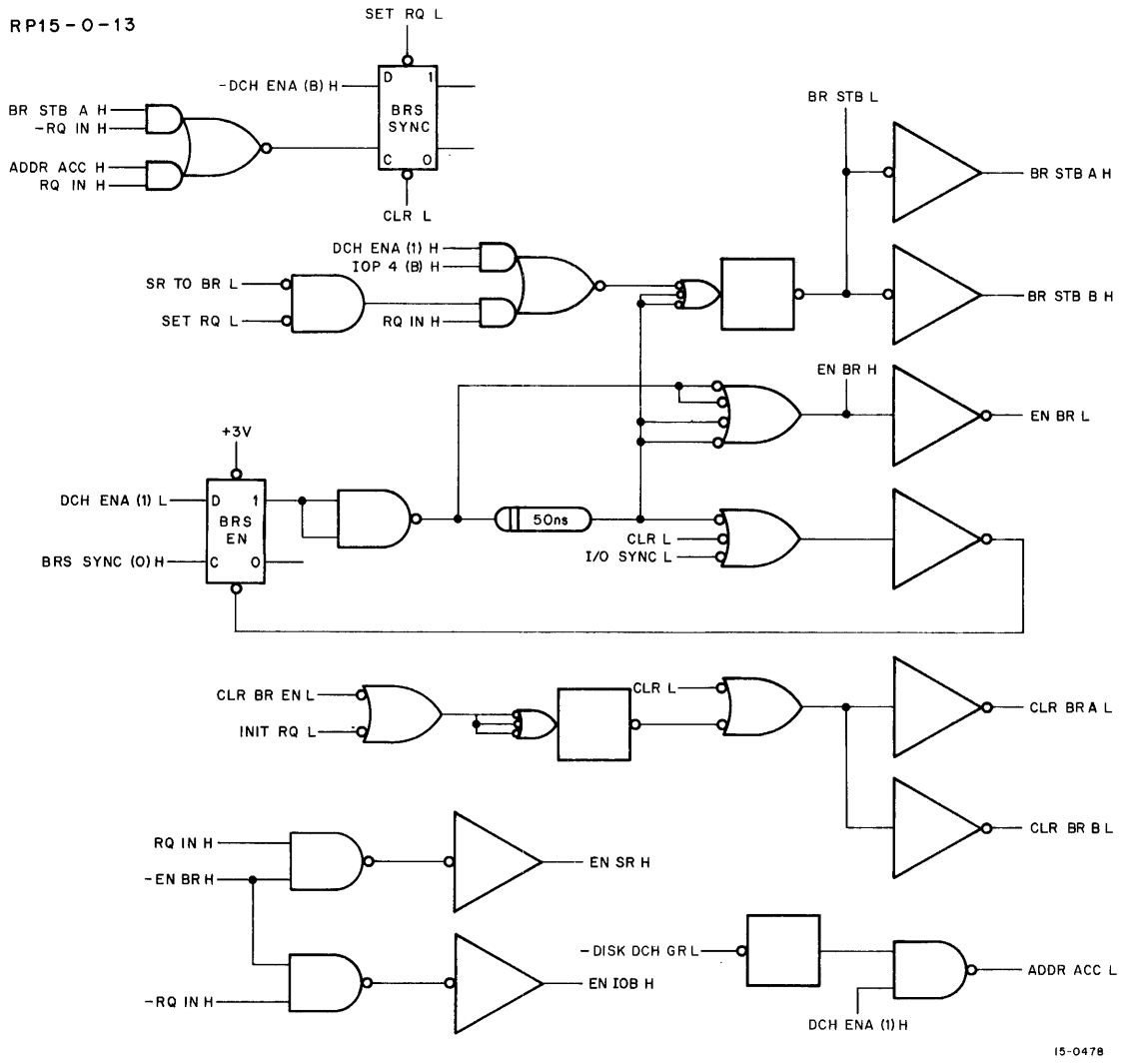


Figure 5-47 BR Control Logic, Simplified Diagram

ADDR ACC L. ADDR ACC L is inverted (not shown) and ANDed with RQ IN H to produce a low signal at the C-input of BRS SYNC. At this time, the D-input of BRS SYNC will be low (-DCH ENA (B) H = DCH ENA (B) L), since DCH ENA was set with the leading edge of DCH GR (B) H. When the C-input of BRS SYNC goes high (trailing edge of ADDR ACC), BRS SYNC will be cleared.

It is the actual clearing of BRS SYNC that shifts bits BR18-35 to bits BR00-17; this operation is common to both IN and OUT transfers. How BRS SYNC gets cleared, however, depends on the direction of transfer; since the actual shifting of BR18-35 to BR00-17 is common for both directions, it will be described here and referred to later.

When BRS SYNC is cleared, BRS EN (Buffer Register Shift Enable) is set. BRS EN (1) H is inverted and parallel fed to both a delay line and two inputs of a power driver (M627). The output of the 50 ns delay line feeds the other two inputs of the power driver. As long as either of these sets of inputs is low, the

output EN BR H is true (also EN BR L after inverting). Note, however, that the output of the delay line is ORed with CLR L and I/O SYNC L to produce a clear signal for BRS EN. The output of the delay line also fires a PA which produces BR STB L, BR STB A, and BR STB B. The timing diagram for this circuit is shown in Figure 5-48. Note particularly from this diagram, that all circuit delays are considered to be 0; otherwise, the leading edge of BR STB A and B H falls in the middle of EN BR H. As pointed out in Paragraph 5.13, this is all that is necessary for the BR to transfer BR18-35 to BR00-17.

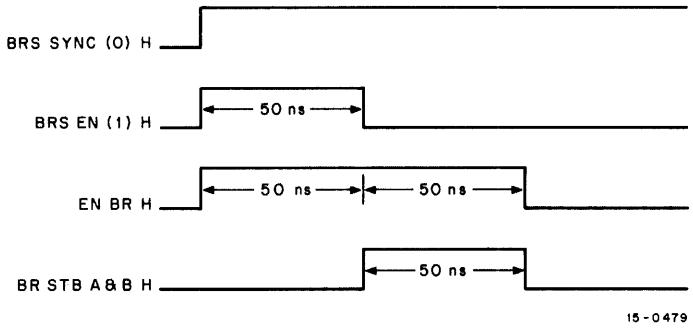


Figure 5-48 BR Control Timing Diagram

Again referring to Figure 5-43, it can be seen that this shift occurs for OUT transfers after the first 18-bit word is received from memory into BR18-35. The BR STB A H that strobes this first 18-bit word into the BR is ANDed with -RQ IN H (equal to RQ OUT) to produce a low pulse input to BRS SYNC.

The other BR operations occur as follows:

a. EN SR H, the enabling level for transfers from the SR to the BR, is decoded as RQ IN H and -EN BR H. During IN transfers, only two operations can take place in the BR: either it is being loaded from the SR, or the last 18 bits are being transferred to the first 18 bits; therefore, at all times other than EN BR, the operation must be EN SR.

b. EN IOB H, the enabling level for transfers from the I/O bus to the BR, is decoded as a -RQ IN H and -EN BR H. During OUT transfers, at all times other than EN BR, the BR looks to the I/O bus for data.

The signals EN SR and EN IOB by themselves, of course, can do nothing. As explained in Paragraph 5.13, they must be accompanied by BR STB A&B H. The BR STB A&B H for EN IOB is generated by the AND condition of DCH ENA (1) H and IOP 4 (B) H (produced by the PDP-15 I/O for all OUT transfer words). The BR STB A&B H associated with EN SR is generated by the following equation:

SR TO BR · SET RQ · RQ IN

As stated before, SR TO BR L, which is generated for Write Check function, will be gated out in a later equation because the SR is not actually transferred to the BR in a Write Check function. Since a Write Check function produces a -RQ IN, the signal SR TO BR cannot produce an output from the above equation.

In Figure 5-47, CLR BR A&B L is generated from the OR of CLR L, the trailing edge of INIT RQ L, and the trailing edge of CLR BR EN L which is described in Paragraph 5.19.

Figure 5-49 shows a simplified block schematic of the M104 I/O Bus Multiplexer module and the signal names that apply to the BR and DCH Control. A timing diagram and general description of this module are given in the PDP-15 Module Manual, DEC-15-H2EA-D.

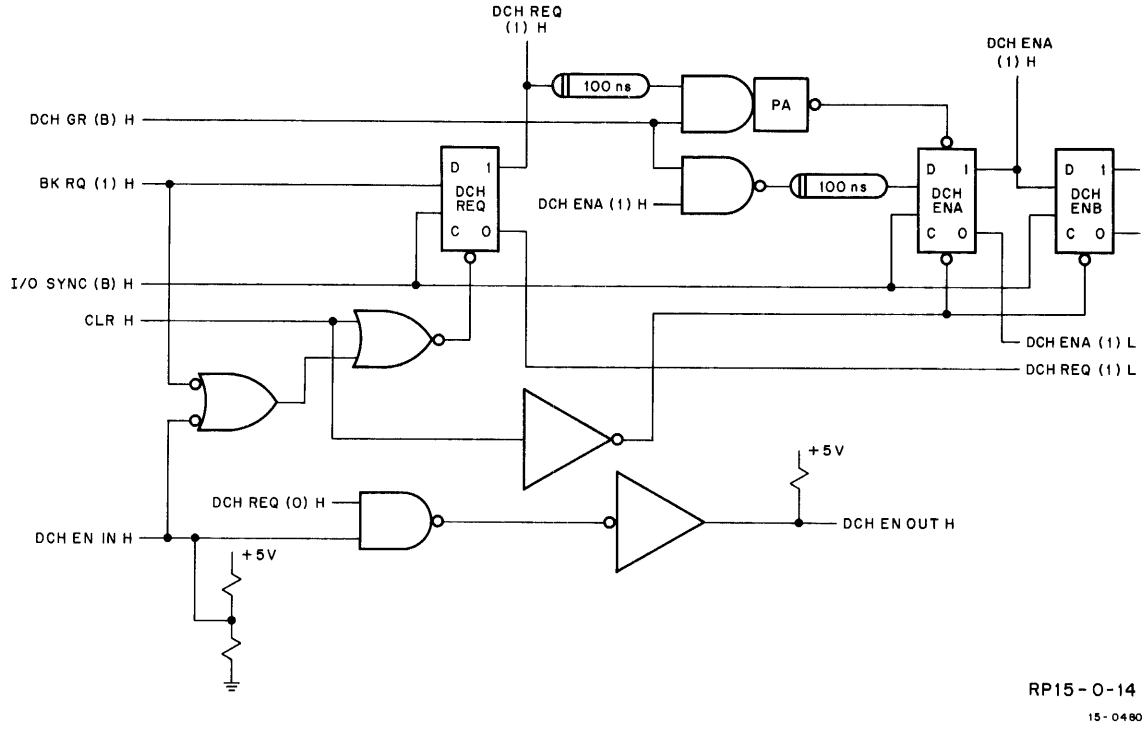


Figure 5-49 M104 Block Diagram for DCH

5.19 CONTROLLING TRANSFER DIRECTION IN THE RP02 (SR and LPR Control)

The SR and LPR Control is shown in Drawing RP15-0-15 and in Figures 5-50 through 5-52.

LPR TO SR L is generated from WLB (1) ANDed with SWC OVFLO (1) (see Figure 5-50). LPR TO SR is used to transfer the generated Longitudinal Parity Register word for a given sector into the SR, where it is then transferred to the disk. It is, therefore, obvious that the transfer should occur after the last bit (WLB) of the sector (SWC OVFLO (1)) has been written. The inversion of LPR TO SR L generates LPR EN H, which gates the 0 sides of each LPR bit to the D-input of the SR.

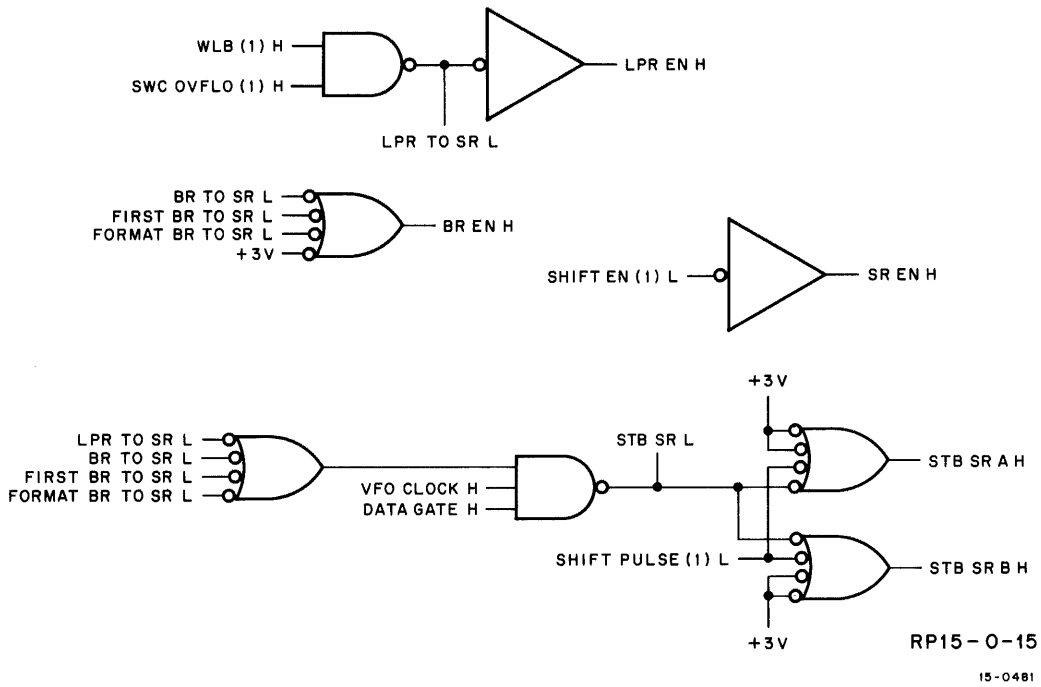


Figure 5-50 BR, SR and LPR Enable and Strobe Signals, Simplified Diagram

In Paragraph 5.18, the signals BR TO SR L, FIRST BR TO SR L, and FORMAT BR TO SR L were generated and used to initiate a BK RQ. In this paragraph, as shown in Figure 5-50, these signals are ORed to produce BR EN H, which gates each of the 36 BR bits to the D-inputs of the SR.

The four signals just described are:

LPR TO SR L
BR TO SR L
FIRST BR TO SR L
FORMAT BR TO SR L

These signals all occur at different times and for different reasons. However, they are ORed to produce a condition which, when ANDed with VFO CLOCK H and DATA GATE H, generates STB SR L and the appropriate STB SR A & B H. Recall from Paragraph 5.13 that STB SR A & B H, and the appropriate enable (BR EN or LPR EN), are all that is required to transfer the BR or LPR to the SR.

SHIFT EN (1) L (generated on Drawing RP15-0-05) is discussed in Paragraph 5.20. At this point, assume that SHIFT EN (1) L is true whenever it is desirable to shift the data in the SR. The signal SHIFT EN (1) is inverted to produce SR EN H which gates SR bit (N + 1) to the D-input of SR bit (N), i.e., SR35 to SR34, SR34 to SR33, etc.).

Before the SR can actually be shifted, STB SR A & B H must be generated at SR EN H time. SHIFT PULSE (1) L, generated on Drawing RP15-0-05, is set for 50 ns each time SR is shifted. This pulse is ORed (along with STB SR L) to produce the necessary STB SR A & B H for shifting.

The control signals for the LPR are shown in Figure 5-51. As discussed in Paragraph 5.13, the LPR can be "loaded" from two sources: CAR-HAR-SAR, or SR. The LPR has two basic functions:

a. To generate longitudinal parity at Write time and generate a check longitudinal parity at Read time, or

b. To compare the header word read from the disk with that contained in the CAR-HAR-SAR.

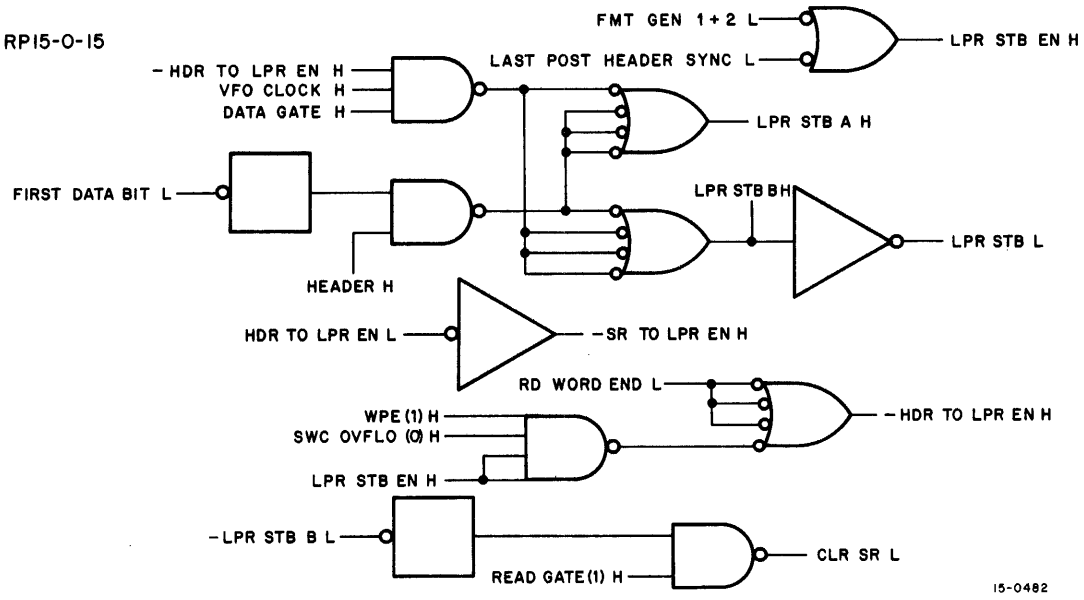


Figure 5-51 LPR Control Signals, Simplified Diagram

The first LPR function (a.) requires an LPR STB for each word written or read in a sector. FMT GEN 1 + 2 L (Format Generator bit 01 and 02 both on a 1, see Paragraph 5.17) is ORed with LAST POST HEADER SYNC L to decode the Data Field during Write operations, and is used to produce LPR STB EN H. LPR STB EN H is ANDed with WPE (1) and SWC OVFLO (0) to produce one of the two signals that generate -HDR TO LPR EN H (same as HDR TO LPR EN L). This signal is then inverted to produce SR TO LPR EN L (same as -SR TO LPR EN H).

The other signal that will produce -HDR TO LPR EN H is RD WORD END L. This signal is generated on Drawing RP15-0-05 and is the AND of READ (1) and END BIT (1). Again, SR TO LPR EN L is produced, this time for READ, which now enables the SR bits to be XORed into the LPR if an LPR STB A & B H

were present. LPR STB A & B H is generated for this operation by the AND of -HDR TO LPR EN H, VFO CLOCK H, and DATA GATE H.

At this point, note that the LPR is never "loaded" but rather XORed from either the CAR-HAR-SAR or the SR. If the LPR were first cleared, then the effect would be a "load".

The signal CLR SR L is generated from the equation:

LPR STB B · READ GATE (1)

This equation states that CLR SR L is generated for any LPR STB B (actually the trailing edge of LPR STB B which is -LPR STB B L) except those that are a result of a word written. Therefore, any word that is read from the disk and XORed into the LPR by LPR STB B will, in turn, clear the SR.

The second LPR function (b.) requires the LPR to be cleared before reading the header word. Referring to Figure 5-52, every SUSP L clears the LPR. As shown on Figure 5-51, since no condition exists for -HDR TO LPR EN H, the HDR TO LPR EN L must be true. Approximately 350 μs after SUSP, the header latch is set, resulting in HEADER H (this is explained in detail in Paragraph 5.20). As the read heads approach even closer to the header word, a sync bit is read, which results in FIRST DATA BIT L. (This is also explained in Paragraph 5.20.) FIRST DATA BIT L fires a PA, which is enabled by HEADER H to produce LPR STB A & B H. Since the LPR has previously been cleared, this results in loading the CAR-HAR-SAR into the LPR.

The contents of the CAR-HAR-SAR are now in the LPR and the header word is being read and assembled in the SR. When the header is completely assembled in the SR, RD WORD END L produces (indirectly) SR TO LPR EN L, which results in LPR STB A & B H. This means that the header word, which has been read from the disk and is presently assembled in the SR, will be XORed in the LPR with the contents of the CAR-HAR-SAR.

NOTE

When the CAR-HAR-SAR was XORed into the LPR, the first 18 bits of the LPR remained clear, while the second 18 bits contained the contents of CAR-HAR-SAR.

If the header read is equal to the desired header address, then the LPR will be all 0s. This is expressed as:

If

CAR-HAR-SAR = Header Word,

the

CAR-HAR-SAR $\forall$ Header Word = 0s.

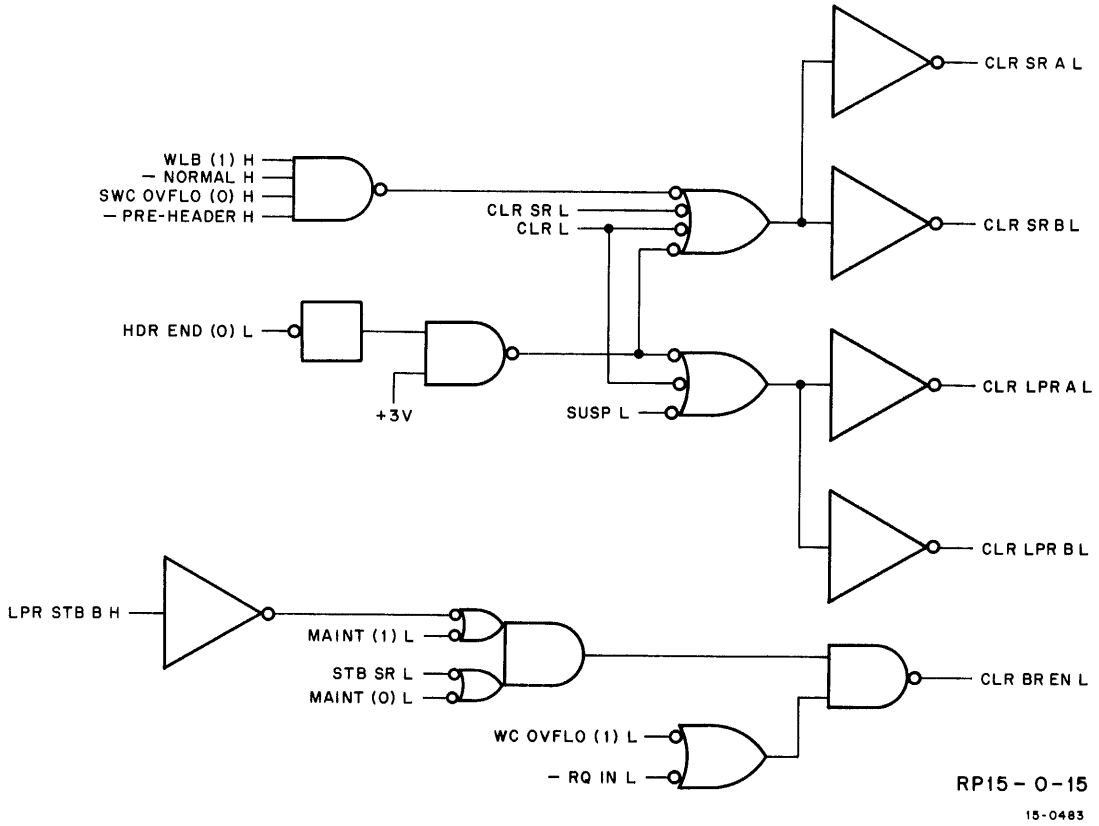


Figure 5-52 BR, LPR and SR Clearing Signals, Simplified Diagram

Actually only the last 18 bits are checked for comparison by a large AND gate shown on Drawing RP15-0-27. The output of this gate is LPR B EQ ZERO H.

Figure 5-52 shows the clearing signals for the BR, LPR, and SR Registers. As pointed out previously, SUSP L generates CLR LPR A & B L as does CLR L. The third input to CLR LPR A & B is the trailing edge of HDR END (1) H (same as HDR END (0) L). HDR END is a signal that is present for 400 ns at the end of each header word read, as described in Paragraph 5.20.

The trailing edge of HDR END (1) H also produces CLR SR A & B L as do CLR SR L and CLR L. The fourth input to CLR SR A & B L is the equation:

$$\text{WLB(1)} \cdot \overline{\text{NORMAL}} \cdot \text{SWC OVFLO (0)} \cdot \overline{\text{PRE-HEADER}}$$

This equation decodes the end of each word in the data field. The equation is good for Write All format function and does not include the header words or LPR words; therefore, at the end of each data field word written, the SR is cleared.

CLR BR EN L is generated by the AND of two inputs. The first input is expressed as:

$$\text{MAINT (0)} \cdot \text{LPR STB B} + \text{MAINT (1)} \cdot \text{STB SR}$$

This equation is a result of timing considerations between maintenance and non-maintenance modes. Of interest is the non-maintenance input which, when ANDed with the second AND gate input, yields the following:

$$\text{MAINT (0)} \cdot \text{LPR STB B} \cdot (\text{WC OVFLO (1)} + \overline{\text{RQ IN}})$$

This equation can be divided to produce:

a. $\text{MAINT (0)} \cdot \text{LPR STB B} \cdot \text{WC OVFLO (1)}$

or it can be divided to produce:

b. $\text{MAINT (0)} \cdot \text{LPR STB B} \cdot \overline{\text{RQ IN}}$

Equation a. states that in the non-maintenance mode each LPR STB B (which occurs once per word) after WC OVFLO (1) clears the BR.

Equation b. states that the BR is to be cleared after each transfer of BR to SR, and after the SR is XORed into the LPR on Write operations. Therefore, a record that ends in the middle of a sector will be filled with 0s.

5.20 CONTROLLING TRANSFER DIRECTION IN THE RP15 (R/W Control)

The Read/Write Control is shown in Figures 5-53, -56, -59, -60, -62, and -63 and in Drawings RP15-0-05, -06, and -07. In addition, timing diagrams are included for quick reference (see Figures 5-55, -57, -58, and -61).

Referring to Figure 5-53, FR01 EQ FR02 H, generated on Drawing RP15-0-18, is inverted to produce FR01 EQ FR02 L. The NOT condition of this signal, -FR01 EQ FR02 H, is ANDed with FR00 (1) H to produce READ ALL + WRITE ALL L. This can be shown by decoding as follows:

EQUATION

$$\overline{(\text{FR01 EQ FR02})} \cdot \text{FR00(1)} = \text{READ ALL} + \text{WRITE ALL}$$

MEANING

$$[\text{FR00}=1] \text{ AND } [\text{FR01} \neq \text{FR02}]$$

FR00	FR01	FR02	
1	0	1	= READ ALL
1	1	0	= WRITE ALL

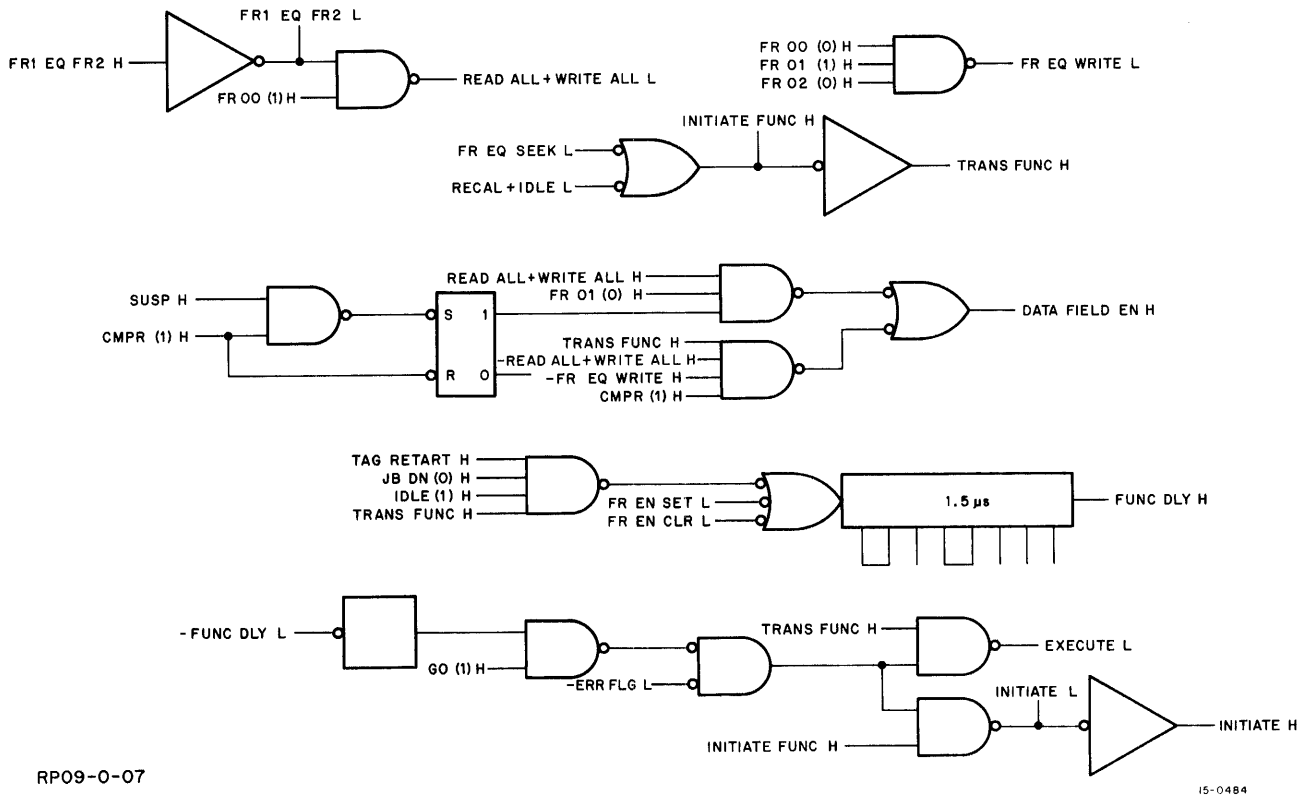


Figure 5-53 Read/Write Sector Decoding Logic, Simplified Diagram

This type of decoding can be used throughout this paragraph to decode the logic equations given. It is included here as an example for future reference.

FR EQ WRITE L is given by the AND condition of FR00 (0), FR01 (1), and FR02 (0).

Two signals called FR EQ SEEK L and RECAL + IDLE L are also generated on Drawing RP15-0-18. The signals are ORed to produce INITIATE FUNC H. The NOT condition of INITIATE FUNC H (-INITIATE FUNC L) is inverted to produce TRANS FUNC H.

These four signals:

READ ALL + WRITE ALL L
FR EQ WRITE L
INITIATE FUNC H
TRANS FUNC H,

are basically all that must be decoded directly from the Function Register (FR) to control the flow of Read and Write states once they have been entered. With these signals, it is possible to decode when

the information coming from the disk (Read State) is part of a Data Field Area. DATA FIELD EN is given by the OR of two equations, one of which is:

$$\overline{\text{TRANS FUNC}} \cdot (\text{READ ALL} + \text{WRITE ALL}) \cdot \overline{\text{FR EQ WRITE}} \cdot \text{CMPR (1)}$$

After reading the desired header, the CMPR flip-flop is set. Note that this equation includes the Read and Write Check functions, but does not include the Read All function. This is because the desired Data Field for a Read All function is not that area that follows the header word which sets CMPR, but rather the area that follows the next header word in line as shown in Figure 5-54.

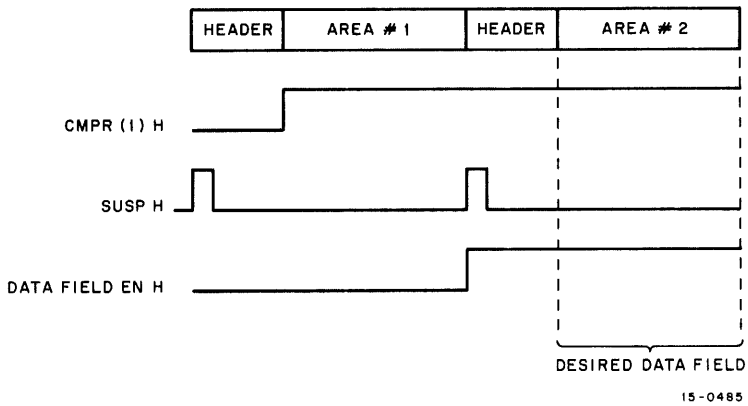


Figure 5-54 Read All Function, Desired Data Field

The first input to DATA FIELD EN H gives the above condition. The SET/RESET flip-flop is set with SUSP H ANDed with CMPR (1) H. The 1 side high of this flip-flop is ANDed with FR01 (0) H and READ ALL + WRITE ALL to produce DATA FIELD EN H. Actually, DATA FIELD EN H is not the decoding for Data Field, but rather the enable level. Data Field will be decoded later in this paragraph.

Control remains in the Idle state until a DPLF, DPLO, DPLZ, or DPCN instruction is issued. At that time one of two (or both) signals are generated (shown on Drawing RP15-0-21), called FR EN SET L and FR EN CLR L. These signals will fire a 1.5-μs delay whose output is FUNC DLY H. When the delay times out, -FUNC DLY L fires a PA, which is enabled by the SRA bit 08, GO (1) H. The output of the PA is gated with -ERR FLG; if an error were present, the signal would end at this point. However, if there is no error condition, the signal is further gated with TRANS FUNC H or INITIATE FUNC H to produce EXECUTE L or INITIATE L, respectively. These signals go to the Major State Control (Paragraph 5.14) to perform their respective functions.

Note from Figures 5-21, -22, -23, -24, and -25, that an EXECUTE L signal always results in a Read or Write state. Also, note that one other way to fire FUNC DLY H (shown in Figure 5-53 and in the above figures) is the equation:

TAG RESTART·JB DN (0)·IDLE (1)·TRANS FUNC

This event can occur many times in one transfer, depending upon how many sectors are required to finish the record. As previously stated, since this is a result of TRANS FUNC, EXECUTE L will result in Read or Write states.

It is likely that Clear Head and Seek will be the states immediately after EXECUTE L. The timing diagrams for these states are shown in Figure 5-55. These states were discussed in detail in Paragraphs 5.14 and 5.15. In Paragraph 5.14, Figures 5-21 through 5-25 should be helpful in understanding these sequences and should be referred to frequently to avoid confusion.

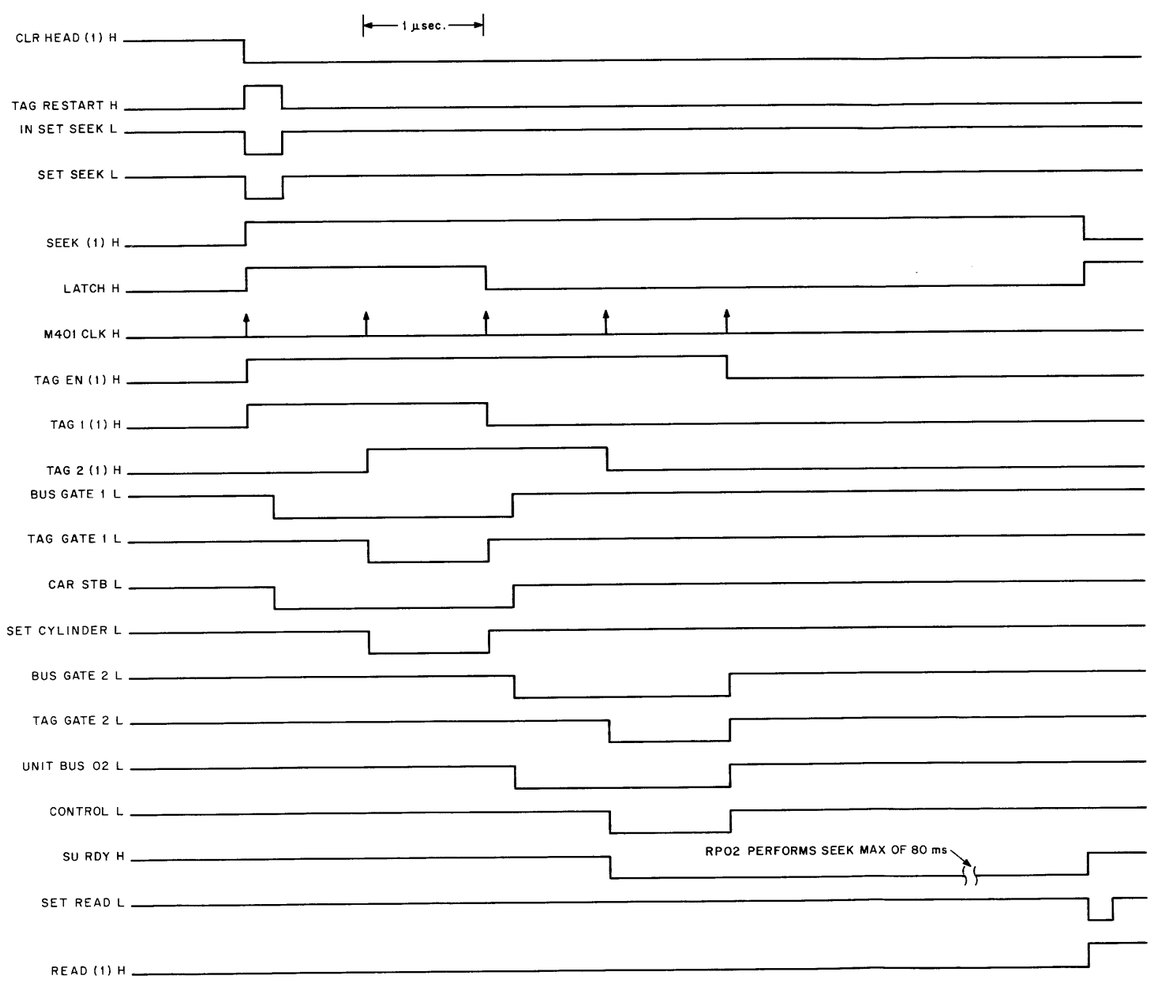
The Read/Write Control also defines the Header and Data Field areas; this logic is shown in Figure 5-56. When SUSP H arrives during a Read state, a 350-μs delay is fired. When this delay times out, it fires a PA which is conditioned by READ GATE (1) H. The output of this PA, SECTOR DLYD L, sets a cross-latched gate called HEADER H/L.

HEADER L is ORed with DATA FIELD L to produce VFO ENABLE H. VFO ENABLE allows the VFO to separate the data pulses from the clock pulses on the Read Data Coax signal line. The data pulses are saved in a flip-flop called RD BIT, which will be described later in this paragraph.

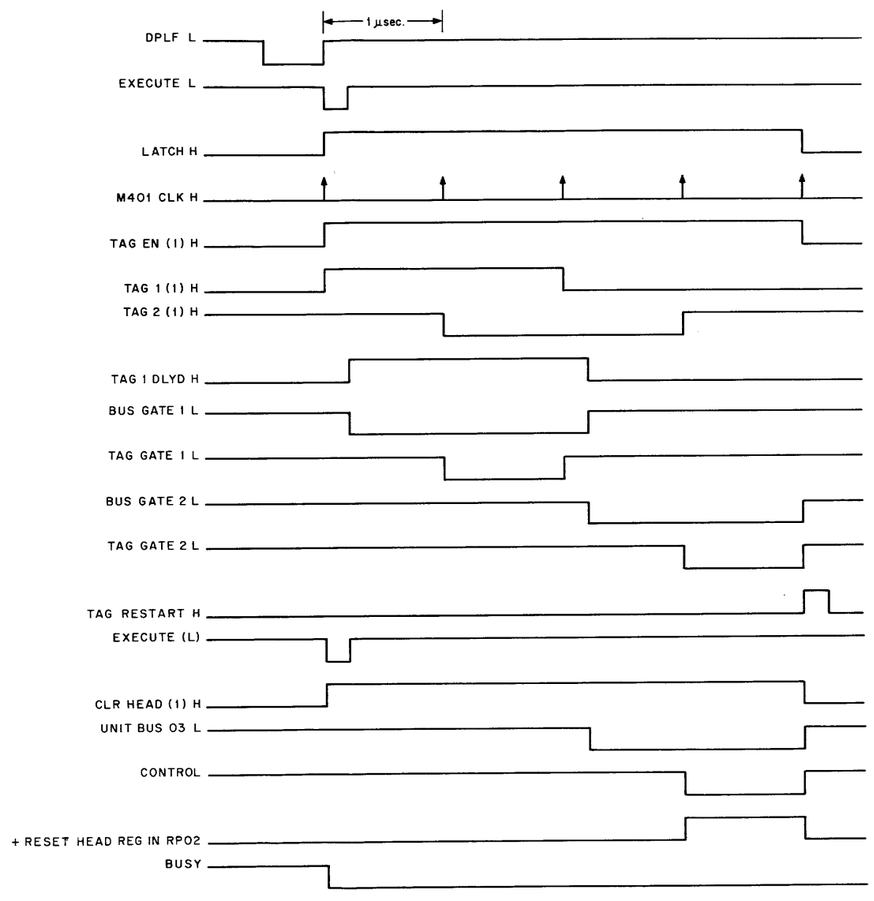
At this time, a flip-flop called END BIT is cleared, VFO ENABLE H is true and, when RD BIT is first set, a cross-latched gate called FIRST DATA BIT H/L is set. Figure 3-2 shows that this occurs one bit cell prior to the first bit of the header word.

Thirty-six bit cells later, END BIT will be set. The AND condition of HEADER H and END BIT (1) H clears FIRST DAT BIT latch, enables the setting of HDR END, and fires a 50-μs delay. HDR END will be set 400-ns later with CLOCK H, and then be cleared again, in another 400 ns, with CLOCK H because END BIT will have been cleared. However, while HDR END is set for 400 ns, it in turn clears HEADER H/L, which results in -VFO ENABLE H.

A glance at the last four paragraphs shows that HEADER H/L was set soon enough and long enough to look only for a header word. Also, the FIRST DATA BIT latch was set at the first sign of a non-synchronizing area (Header or Data Field), and again cleared upon the entering of a synchronizing area. This timing is shown in detail in Figures 5-57 and 5-58.



SEEK TAG GATE TIMING



CLR HEADS TAG GATE TIMING

Figure 5-55 Timing Diagram Number 1

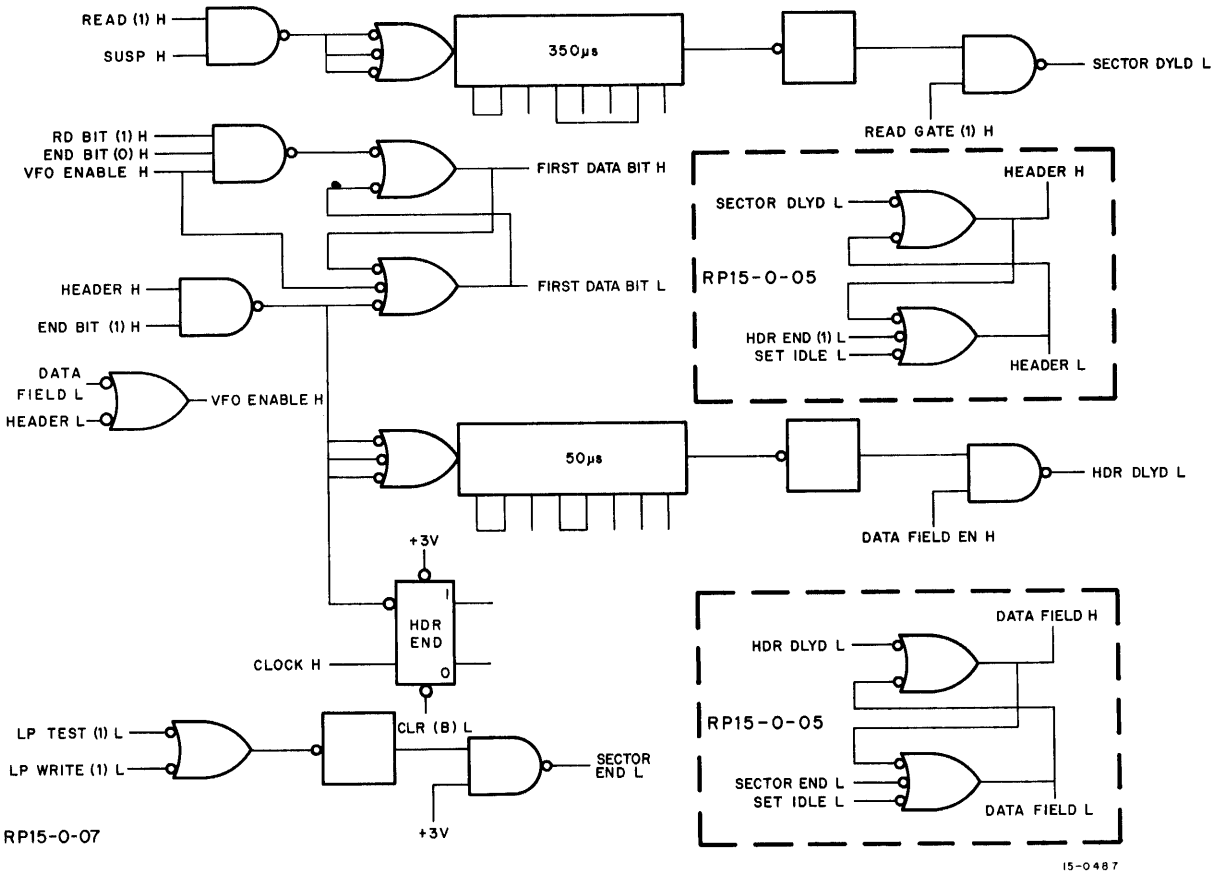
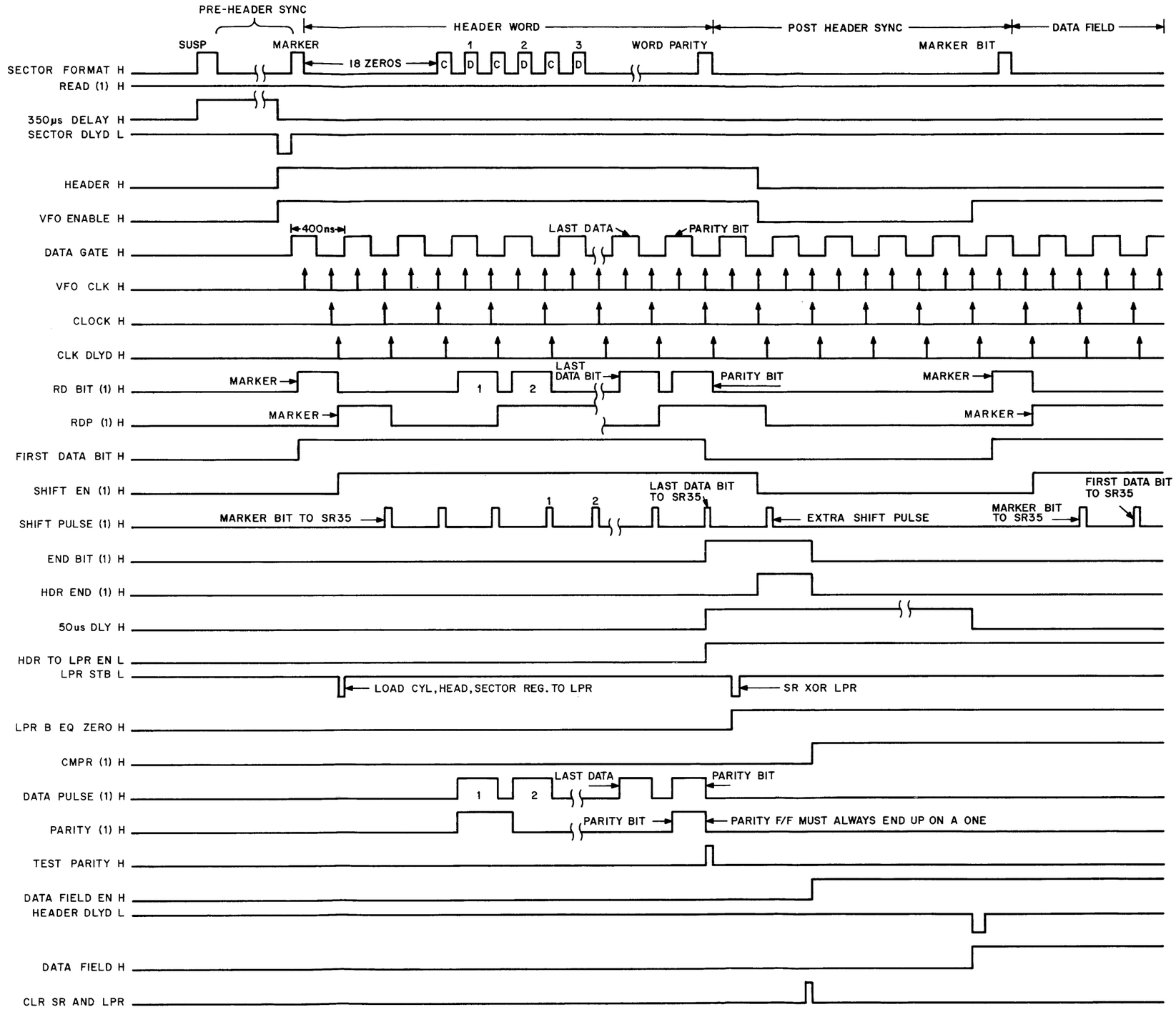


Figure 5-56 Header and Data Field Logic, Simplified Diagram

At this point in the sequence, the 50-µs delay mentioned above is still timing out. After this delay has timed out, it fires a PA that is conditioned by DATA FIELD EN H. The output of this PA, HDR DLYD L, sets a cross-latched gate called DATA FIELD H/L. DATA FIELD L is ORed with HEADER L to produce VFO ENABLE H.

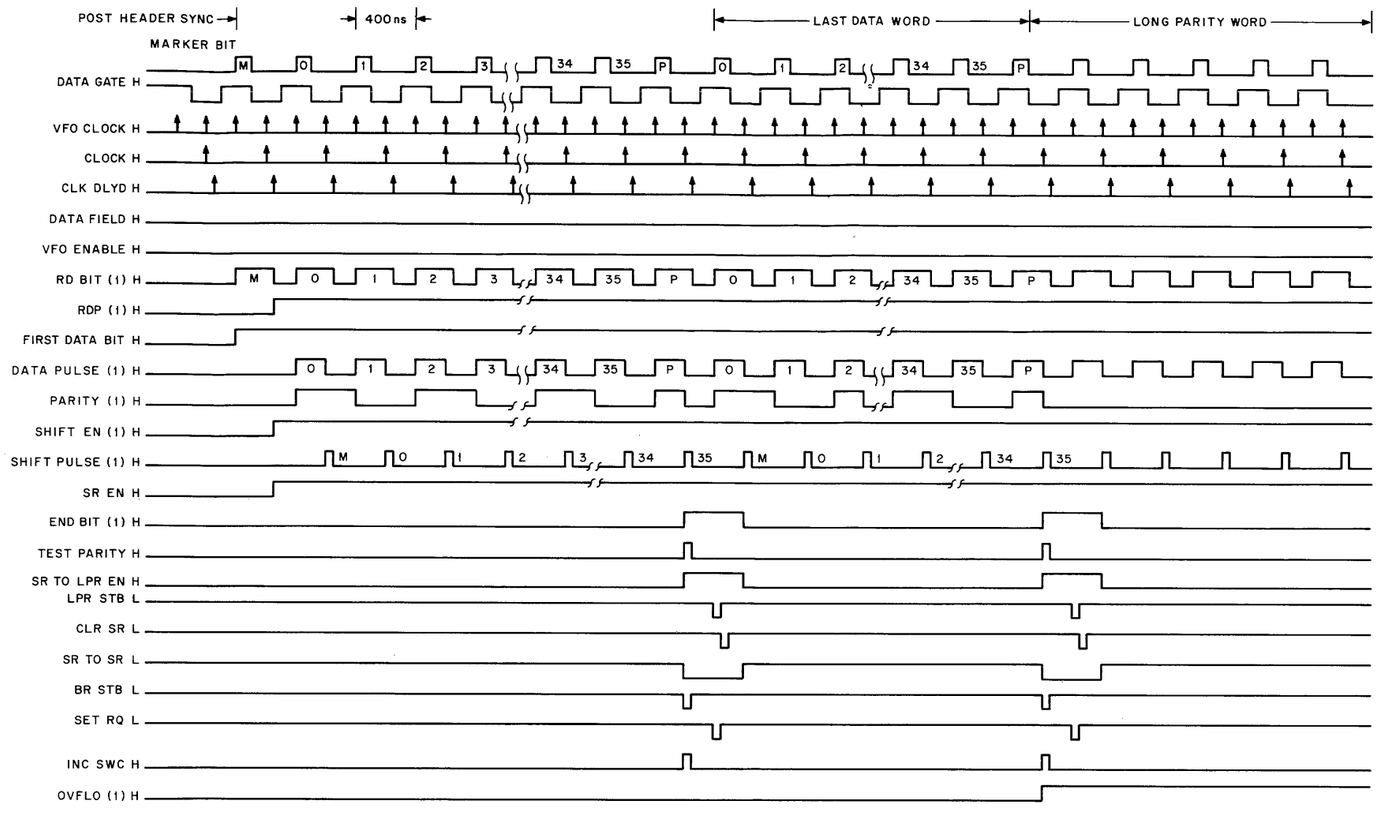
Again, VFO ENABLE H allows the first data bit (which comes along on the Read Data Coax line) to set FIRST DATA BIT H/L. However, this time, this bit is just one bit cell before the first bit of the Data Field as shown in Figure 3-2.

DATA FIELD, VFO ENABLE, and FIRST DATA BIT all remain true until the Data Field has been completely read. When this happens, a flip-flop called LP TEST will be set for 400 ns; on its trailing edge, a PA will be fired to produce SECTOR END L. (Note that SECTOR END L can also be produced by the trailing edge of LP WRITE.) SECTOR END L clears DATA FIELD H/L, resulting in -VFO ENABLE H (or VFO ENABLE L). VFO ENABLE L, in turn, clears FIRST DATA BIT H/L.

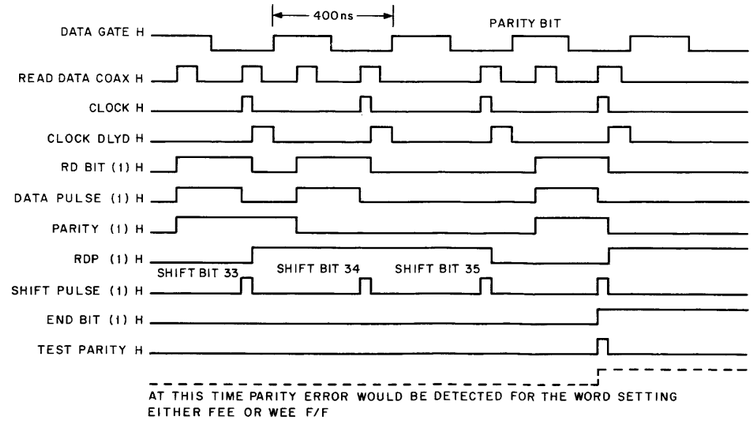


HEADER TIMING

Figure 5-57 Timing Diagram Number 2



READ TIMING



WORD PARITY SENSE TIMING

15-0489

Figure 5-58 Timing Diagram Number 3

Note from the preceding paragraphs once again, that, DATA FIELD has been set soon enough, and long enough, to encompass only the Data Field. Also, VFO ENABLE H and FIRST DATA BIT H/L were true to enable the reading of the non-synchronizing areas only. The timing for the Data Field is shown in detail in Figure 5-58. Note that HEADER and DATA FIELD are cleared with SET IDLE L.

In the discussion thus far, the Sector has been divided into Header and Data Field areas. Smaller segments of these areas (36-bit word plus parity bit) are decoded as shown in Figure 5-59.

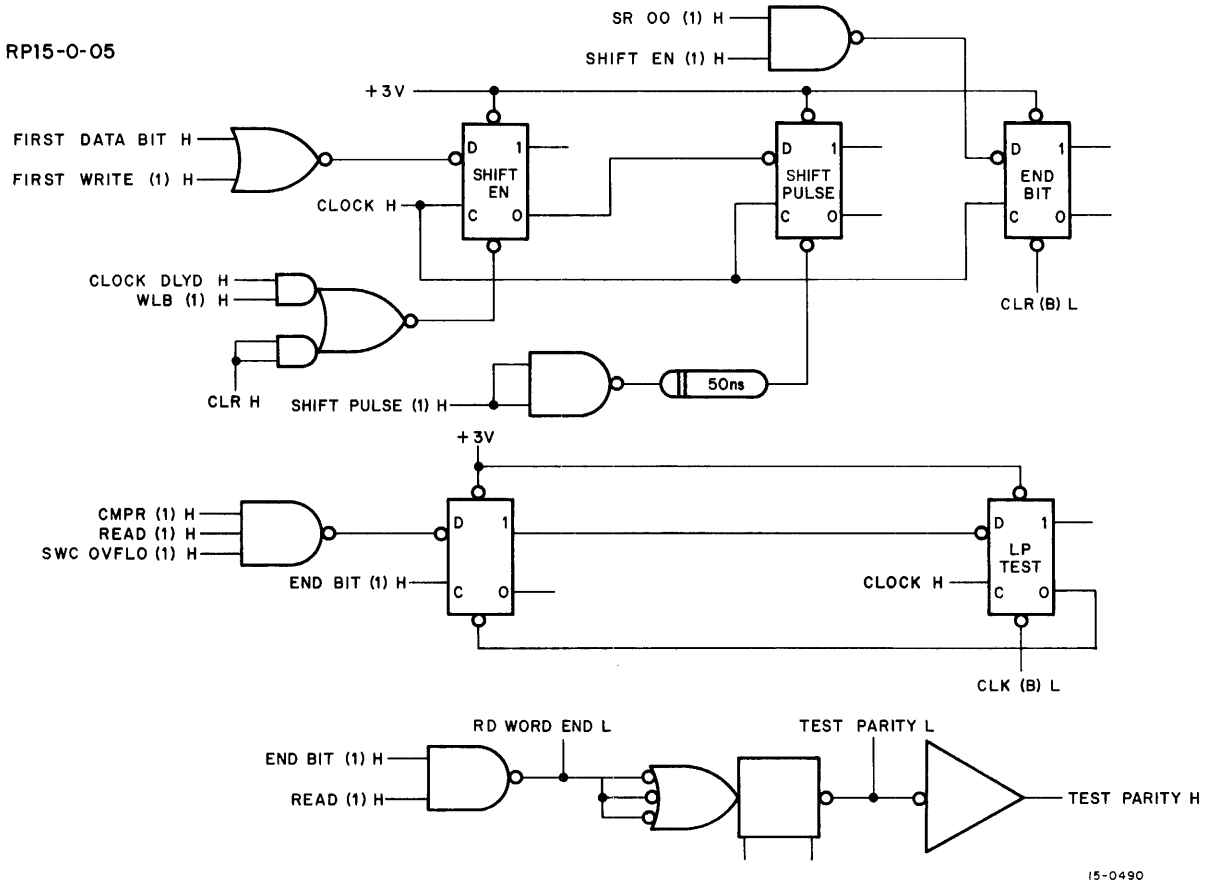


Figure 5-59 Word Plus Parity Decoding during Read, Simplified Diagram

The D-input for SHIFT EN is conditioned by the OR of FIRST DATA BIT H or FIRST WRITE (1) H. For Read states, FIRST DATA BIT H is true for the entire Header or Data Field areas. Therefore, when in the Read state, SHIFT EN is set on the clock pulse (CLOCK H) following FIRST DATA BIT H and remains set until the clock pulse following -FIRST DATA BIT H (or FIRST DATA BIT L). Also, each clock pulse following the setting of SHIFT EN sets SHIFT PULSE which will then clear itself through a 50-ns delay. For Read state then, SHIFT PULSE (1) occurs at each CLOCK H during SHIFT EN.

Since the SR is cleared before reading a word, then END BIT will also be cleared, because SR00 would be on a 0 at CLOCK H time. Also, just before reading a word, a 1 bit is placed in RDP (Read Data Pulse) which is the flip-flop that feeds SR35. This is done initially by the cue bit just prior to the Header or Data Field (see Figure 3-2). After that, this bit is recycled to produce the 1 bit at the beginning of each 36-bit word. RDP will be described later in this paragraph, but its function at this point in the sequence is to feed data to the SR (SR bit 35), the first bit prior to each word always being a 1.

Thirty-seven shifts later, END BIT will be set with the AND of SR00 (1) H and SHIFT EN (1) H. Since everything following this first bit is either data or parity, the data word must now sit in the SR and the parity bit in the parity flip-flop. Because this operation cycles for each word, END BIT (1) H can be used to mark the end of a 36-bit word.

END BIT (1) H is ANDed with READ (1) H to produce RD WORD END L, TEST PARITY L, and TEST PARITY H. Note that END BIT is used to generate SR TO BR H on Drawing RP15-0-13, which then generates INC SWC H on Drawing RP15-0-23. END BIT, therefore, keeps track of the number of 36-bit words read in a sector.

END BIT also detects when it is time to test the longitudinal parity word. This is done by first detecting the following equation with the leading edge of END BIT (1) H:

CMPR (1)·READ (1)·SWC OVFLO (1)

This equation occurs when the parity bit of the longitudinal parity word has been read. Then, 400-ns later, LP TEST is set with CLOCK H.

Note also from Figure 5-59 that SHIFT EN can be cleared by the following equation:

CLOCK DLYD H·WLB (1) + CLR

When in the Write state, the sector must also be broken into 36-bit words plus parity, in a manner similar to Read state. When the Write state is entered, the next CLOCK H sets FIRST WRITE (shown in Figure 5-60). One clock pulse later SHIFT EN is set as shown in Figure 5-59. SHIFT EN (1) L is then inverted on Drawing RP15-0-15 to produce SR EN H.

Referring to Figure 5-60, SHIFT EN (1) L fires a PA that is enabled by FIRST WRITE (1) H to produce SET RDP L which sets the RDP flip-flop. One clock pulse later, WDE is set because of the AND condition of SR EN H and WRITE (1) H at the D-input. At this same clock pulse time, SHIFT PULSE is set and cleared to shift the bit in RDP into SR35 and SR00 into END BIT, where it will then be written. Thirty-four more shift pulses will place the bit, which started in RDP, in bit 01 of the SR. All bits after the first 1 bit in RDP will be 0s until the next SET RDP L signal.

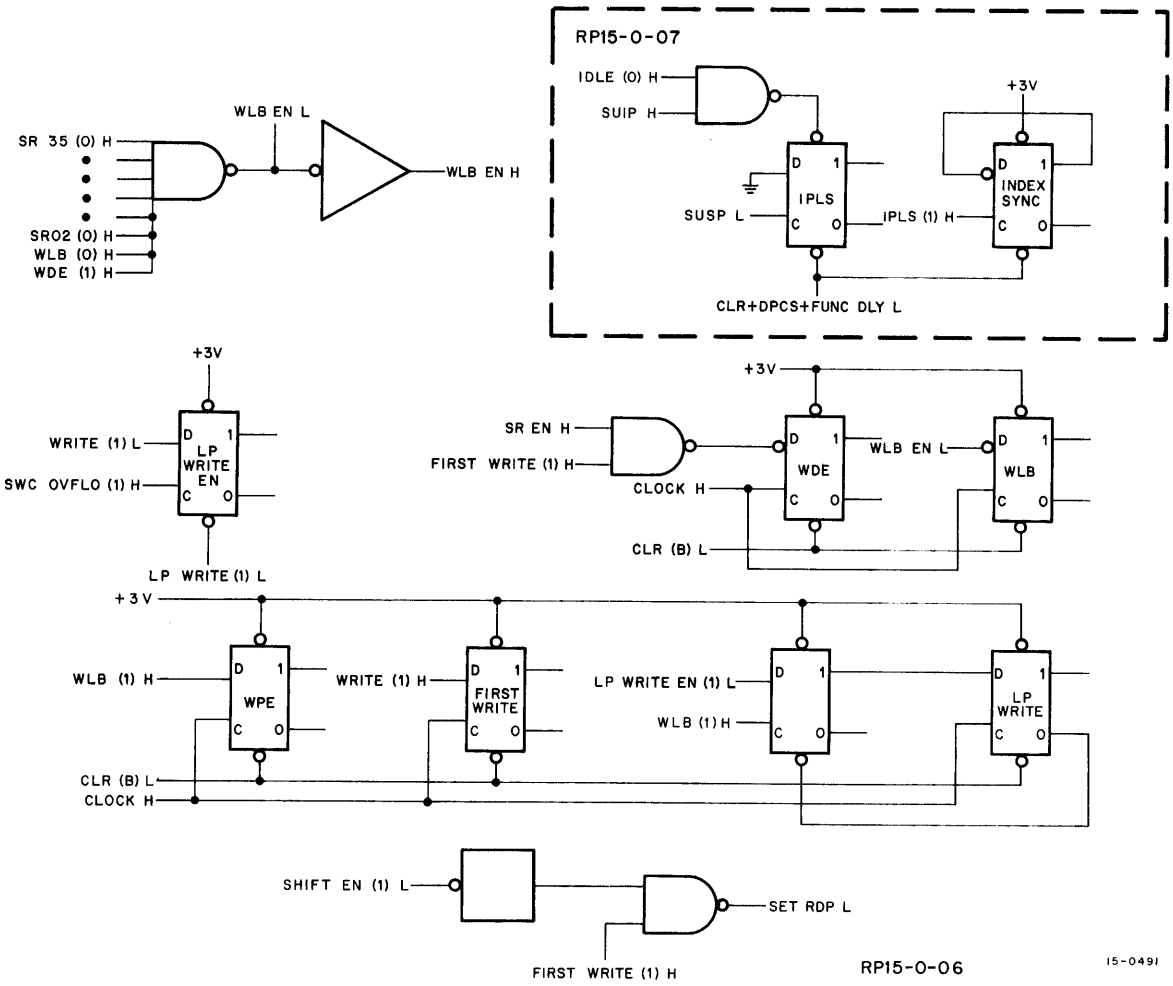


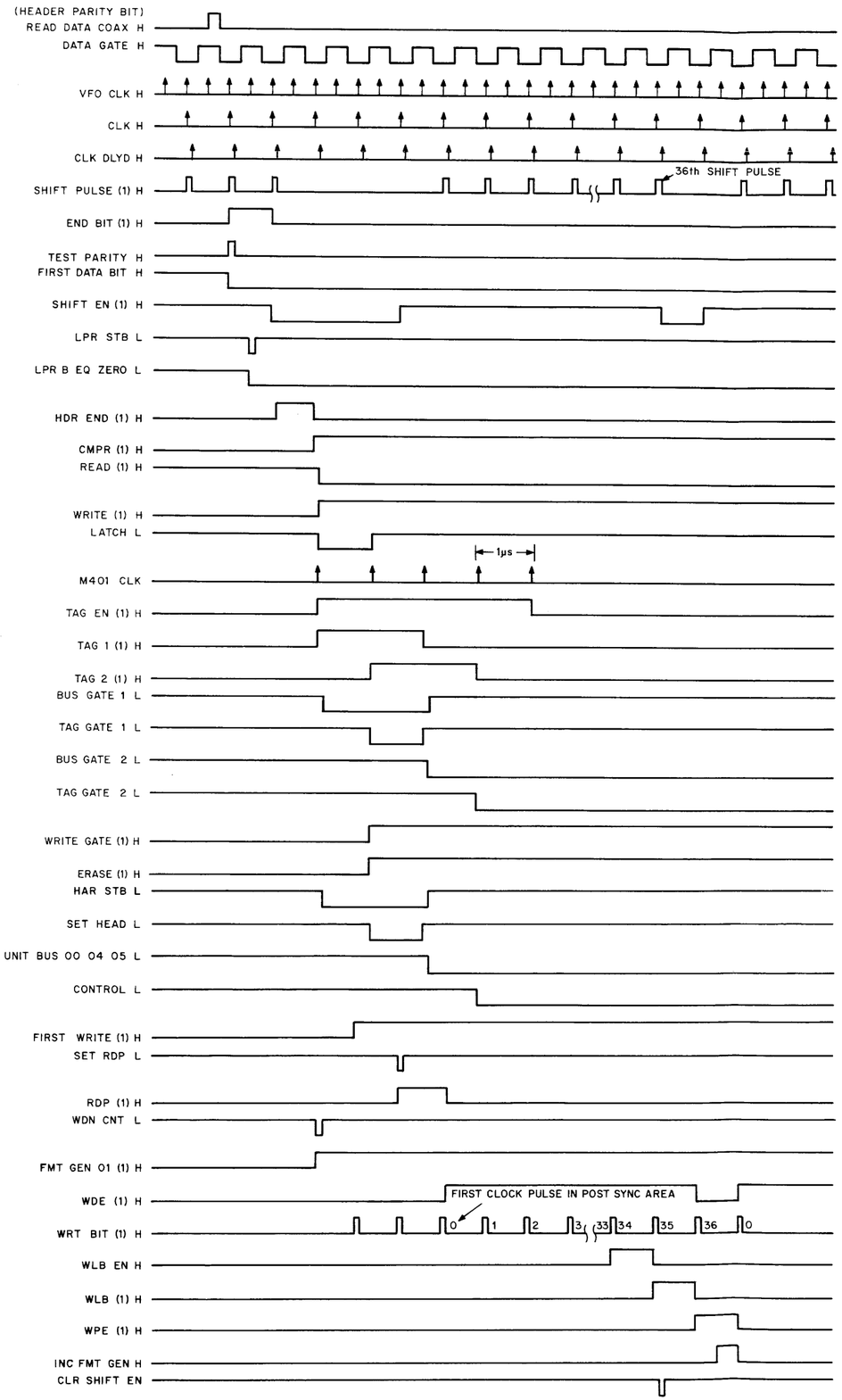
Figure 5-60 Word Plus Parity Decoding during Write, Simplified Diagram

At this point in the sequence, the conditions set are WRITE (1), SHIFT EN (1) (which produces SR EN H), FIRST WRITE (1), WDE (1), and WLB EN H/L. WLB EN H/L is present when SR bits 02 through 35 are cleared, WDE is set, and WLB is cleared (see Figure 5-61). Following this timing diagram, the next CLOCK H produces the 36th SHIFT PULSE (1) H which sets WLB (disables WLB EN); at CLOCK DLYD H time (50 ns later), WLB (1) H clears SHIFT EN flip-flop. WLB (Write Last Bit) means that the bit which started in RDP is now in bit SR00; therefore, the bit which was in SR35 must be in END BIT and in the process of being written.

The next CLOCK H will now clear both WLB and WDE, set WPE (Write Parity Enable), and reset SHIFT EN; but there will be no SHIFT PULSE (1) H because SHIFT EN was on a 0 at CLOCK H time. However, at this time, the leading edge of SHIFT EN (1) L again fires a PA which is enabled by FIRST WRITE (1) H to produce SET RDP L. SET RDP L then sets RDP and the cycle repeats.

NOTE

Another CLOCK H would produce the first SHIFT PULSE (1) H for the next word, which would then set WDE.



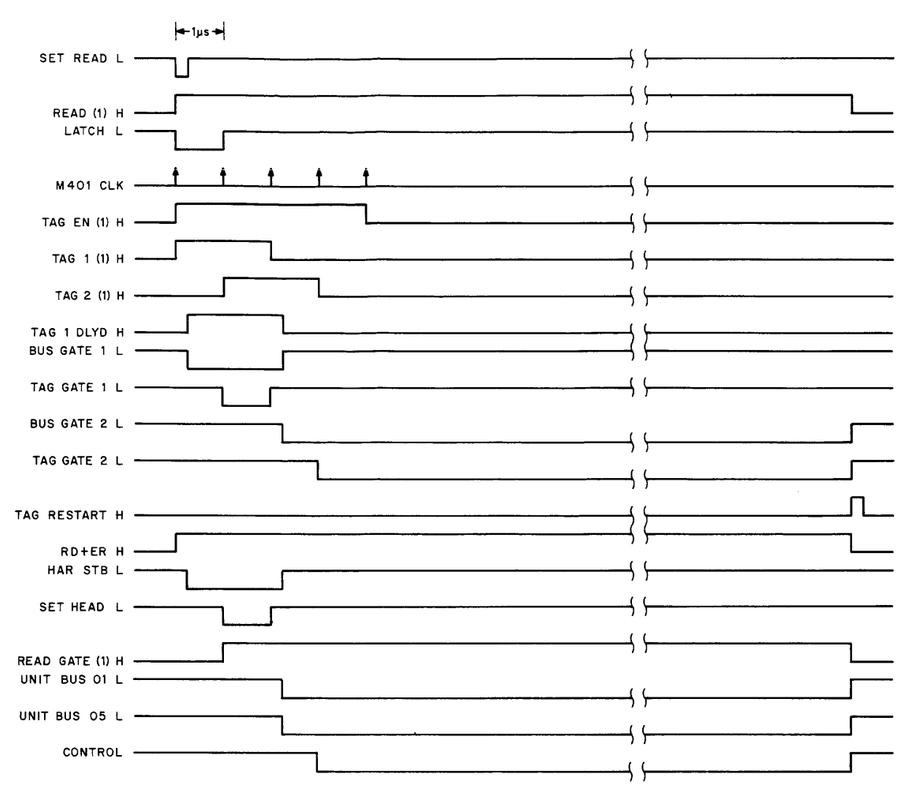


Figure 5-61 Timing Diagram Number 4

The word that has just been written could be the first word in either the VFO Sync Area or VFO Data Sync Area. However, the process is the same for header or data field words. Actually, the format generator is incremented with each WPE (1) H and will soon reach the code for either a Header or Data Field area. At that point, the contents of the BR will be transferred to the SR during WLB (1) H. Once the Data Field has been reached, each WLB (1) H increments the SWC to allow only 128_{10} 36-bit words.

There must then be a means of detecting when it is time to write the longitudinal parity word. On the 128th WLB, SWC OVFLO (1) H is generated; in turn, it sets LP WRITE EN. At WLB time of the LP word, a synchronizing flip-flop is set that enables the D-input to LP WRITE. On the next CLOCK H (WPE time of the LP word), LP WRITE (1) L is generated which then fires a PA to produce SECTOR END L (see Figure 5-56).

Figure 5-60 also shows two flip-flops called IPLS and INDEX SYNC. The purpose of these flip-flops is to synchronize the Write and Increment Head states during the formatting instruction (WRITE ALL FORMAT). When WRITE ALL FORMAT is executed, CLR + DPCS + FUNC DLY L clears both flip-flops. The control state will be CLR HEAD until SUSP H sets IPLS which complements (or sets) INDEX SYNC. The leading edge of the next SUSP H will then set Write state (see Figure 5-18). The trailing edge of that same SUSP L will clear IPLS.

The control will now remain in the Write state for one complete revolution, at which time the next SUIP H will again set IPLS which will complement INDEX SYNC to a 0. The following SUSP will change the control state to Increment Head for one revolution.

This operation repeats until one entire cylinder of the disk pack is formatted. This operation is described in detail in Paragraph 5.14.

Up to this point in the discussion, the disk has been divided into Sectors, then into Headers or Data Fields, then into words. Now, it must be separated into Clock and Data Bits. Considering the Write state first, shown in Figure 5-62, a four-input OR gate is provided whose output enables the D-input of WRT BIT (Write Bit). Also, a 5-MHz signal, called VFO CLOCK H, strobes the C-input. If at VFO CLOCK H time the D-input is true (High), then WRT BIT will be set for 50 ns and then cleared. The pulse output WRT BIT (1) L is shown on Drawing RP15-0-46 feeding one input of eight M622 drivers. The other input is conditioned by SU XX L (Selected Unit XX) which then directs the bit to be written to the appropriate unit.

The first equation that will produce a true signal at the D-input of WRT BIT is:

WSBE·WPE (1)·FIRST WRITE (1)·DATA GATE

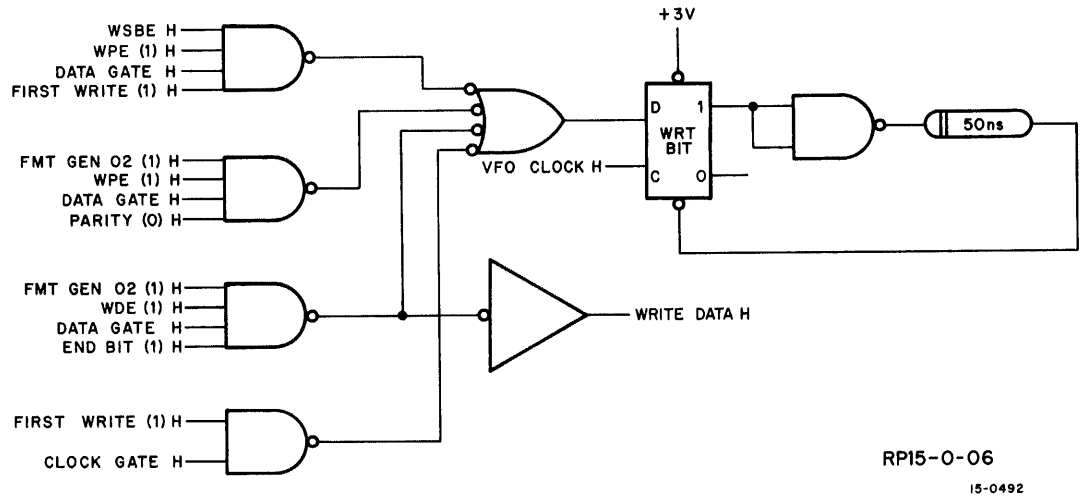


Figure 5-62 Clock and Data Bit Decoding during Write, Simplified Diagram

The first two conditions define the parity bit of the last word in either the VFO Sync Area or VFO Data Sync Area. The last two conditions define a Write operation and Data time. This equation then produces the cue bits in both the VFO Sync Area and VFO Data Sync Area.

The second equation is:

FMT GEN 02 (1)·WPE (1)·DATA GATE·PARITY (0)

The first two conditions of this equation define parity time of either a header or data field word. The third condition produces Data time; the fourth condition provides the value of the bit to be written for odd parity. The parity bit will be described later in this paragraph but note that a 1 is written for parity if the PARITY flip-flop is on a 0.

The third equation is:

FMT GEN 02 (1)·WDE (1)·DATA GATE·END BIT (1)

This equation is the same as the second except that it now defines the Data bit time [WDE(1)] and writes the contents of END BIT.

The last equation is:

FIRST WRITE (1)·CLOCK GATE

This equation provides for the writing of a 1 for each CLOCK GATE, which produces the basic 2.5-MHz 0s rate signal (or Clock Bits) in the double-frequency NRZ writing technique.

WRITE DATA H is the inverted output of the third equation and is used in generating parity.

Considering the Read case shown in Figure 5-63, each READ DATA COAX 00-07 L is ORed to produce READ DATA COAX H. (There can be pulses on only one line at a time.) The leading edge of any pulse on READ DATA COAX H, which occurs during DATA GATE H, will set RD BIT (Read Bit). Once RD BIT is set, it is latched-set with the AND condition of -CLOCK DLYD H and RD BIT (1) H and will only be cleared with the next CLOCK DLYD L, regardless of what appears on READ DATA COAX H during -DATA GATE L. RD BIT then separates Data bits from Clock bits on RDC (READ DATA COAX) and stores them until the next CLOCK DLYD signal.

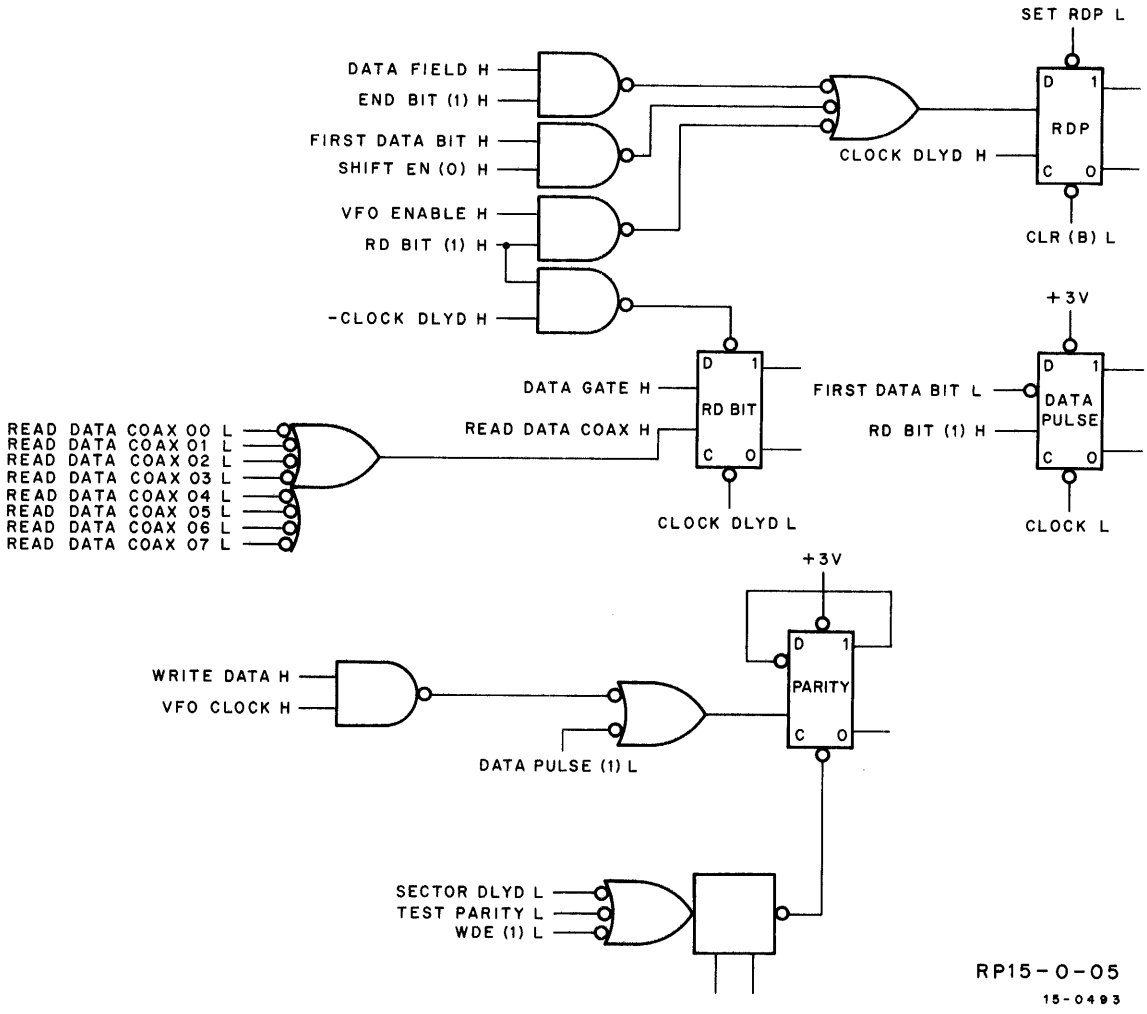


Figure 5-63 Clock and Data Bit Decoding in Read, Simplified Diagram

If the HEADER or DATA FIELD latch is set, producing VFO ENABLE H, then each RD BIT (1) H will condition one input of a 3-input OR gate which, in turn, makes the D-input of RDP (Read Data Pulse) true. On the following CLOCK DLYD H, the contents of RD BIT are strobed into RDP. The purpose of RDP is to de-skew RD BIT, which is following the jitter of RDC.

Another input to the 3-input OR gate that conditions RDP is DATA FIELD ANDed with END BIT (1) H. When the first word of the Data Field is read, the cue bit is the first bit to reach RDP. From there, it is shifted down the SR until it reaches END BIT. Since the next bit to be read is not another cue bit, but rather a parity bit, a cue bit must be simulated to keep a known 1 bit circulating in the SR. This input serves that function.

DATA PULSE is similar to RDP in that it contains the contents of all RD BIT 1s except the cue bit read in prior to the first word. It must be remembered, that FIRST DATA BIT L is a result of the first RD BIT which is the cue bit. Therefore, FIRST DATA BIT L cannot condition the D-input to DATA PULSE soon enough to catch the first RD BIT (1) H. However, all following RD BIT (1) H 1s are stored in DATA PULSE until cleared by CLOCK L.

Now, since DATA PULSE is only data bits, it can be used as one of the OR conditions that complement PARITY to calculate the parity of the word being read. Parity for Read is generated by first clearing PARITY with SECTOR DLYD L or TEST PARITY L (which occurs at the end of each word). Then, each bit read (DATA PULSE (1) L) complements PARITY. At the end of each word, TEST PARITY L strobes FEE and WEE (Format Error Enable and Word Error Enable) to see if PARITY is on a 1, which it should be. If PARITY is not on a 1, the FEE or WEE flip-flop is set indicating an error condition. This operation is described in more detail in Paragraph 5.23. Parity sensing timing for Read is shown in Figure 5-58.

Parity for Write operations is generated by first clearing PARITY with WDE (1) L. Then, each WRITE DATA H ANDed with VFO CLOCK H will produce the complementing pulse for PARITY. After the 36 bits of data have been strobed into WRT BIT, the complement of PARITY is written. This was described in the discussion concerning Figure 5-62.

5.21 WORD COUNT AND CURRENT ADDRESS CONTROL

The RP15 Word Count (WC) and Current Address (CA) Control is shown in Figure 5-64 and on Drawing RP15-0-17. This control operates, with the Current Address Register (CA), to sequence the memory (see Paragraph 5.9), and with the Word Count Register (WC) to regulate the length of each transfer.

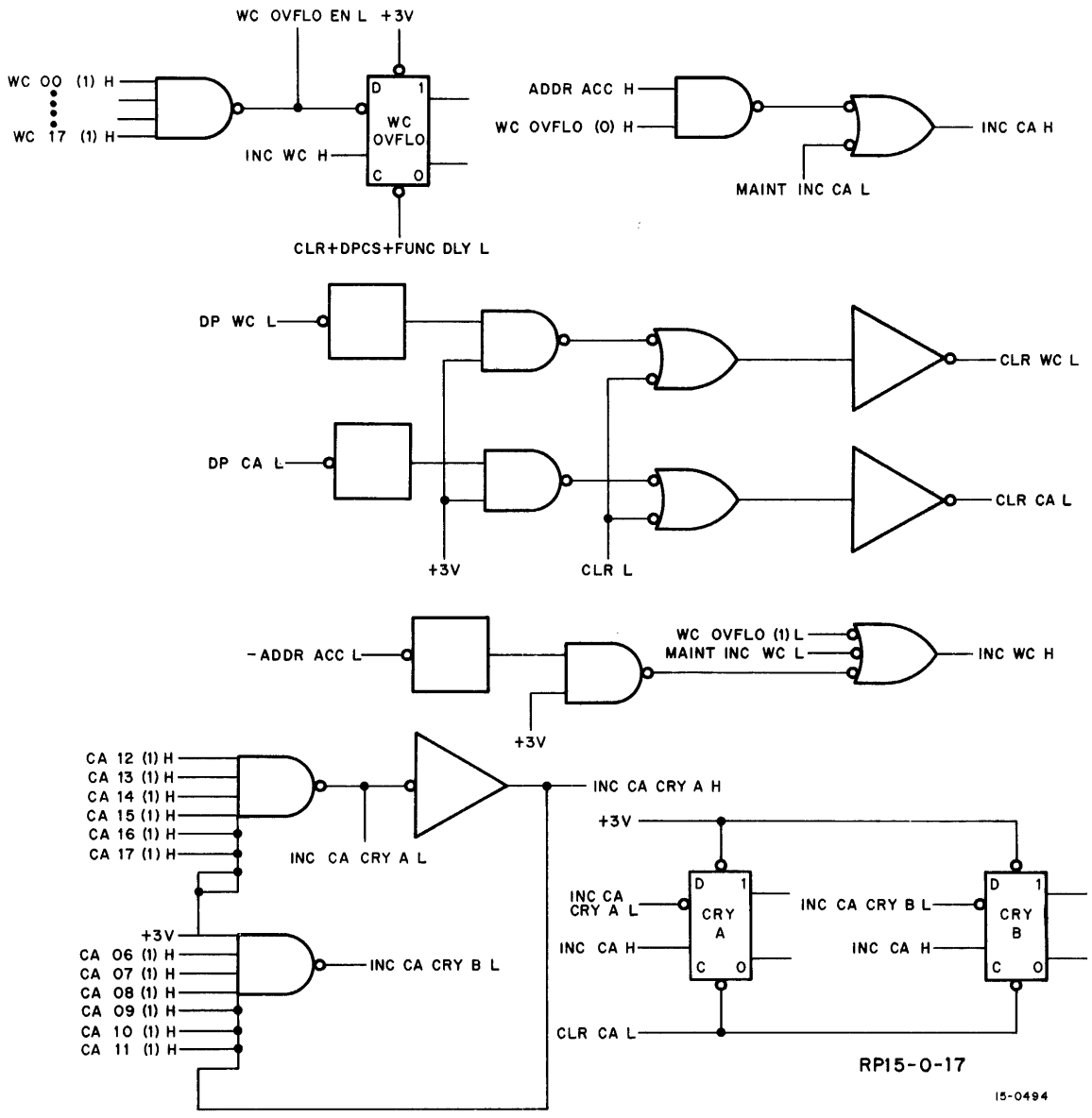


Figure 5-64 WC and CA Control, Simplified Diagram

Since the CA is a ripple counter and since ripple counters can take considerable time in incrementing, provisions are made to speed up this process. As described in Paragraph 5.9, the register is broken into 6-bit sections, with the second two sections decoded before the first. This scheme eliminates the wait for the delay out of each. For example, bits 12-17 of the CA are always incremented; but bits 6-11 are incremented only if bits 12-17 are already on a 1 prior to INC CA H; bits 0-5 are incremented only if bits 6-17 are already on a 1 prior to INC CA H. This is done by creating two separate increments for CA bits 0-5 and 6-11 called CRY A (1) H and CRY B (1) H. The D-type flip-flops are used so that INC CA H can be sampled at its leading edge. In this way, incrementing does not wait for

ripple delay, but rather utilizes an AND conditioning to achieve the same result; the worst-case delay is reduced to one-third of what it would be normally. In a sense, the need for incrementing is predicted in this design rather than waited for.

INC CA H is generated from the following equation:

MAINT INC CA + (ADDR ACC·WC OVFLO (0))

Note that in normal operation the CA can be incremented only if the WC is not yet complete.

WC OVFLO flip-flop is set when WC bits 00-17 are all set prior to INC WC H, at which time WC00-17 are all incremented to 0. INC WC H is generated from the OR of MAINT INC WC L and ADDR ACC. WC OVFLO (1) L also produces INC WC, so that once WC OVFLO is set, it remains set because there can be no more positive transitions on INC WC H until WC OVFLO is cleared by external means.

Two AND/OR gate combinations decode DPWC L (Disk Pack Word Count) and DPCA L (Disk Pack Current Address). These signals are then ORed with CLR L to produce clearing signals for the Word Count Register (CLR WC L) and Current Address Register (CLR CA L). Note that these clear signals are about 50-ns wide. This is important because if a DPWC is issued (which is 1-μs wide) the first 50 ns are spent clearing all WC bits. The remaining 950 ns are used to strobe the preset sides of those WC bits that correspond to existing IOB bits (see Drawing RP15-0-31). This is also true of the CA. If both CLR WC L and DPWC H were the same width, the WC register would be confused.

CLR WC L and CLR CA L are also produced by CLR L.

5.22 WRITE PROTECTION FOR THE DRIVE

The RP15 is equipped with two types of Write protection: both types inhibit the Write operation from occurring and raise the interrupt Write Protect Error via the enabling level WPEE. The logic for this capability is shown in Figure 5-65, Drawings RP15-0-09 and -10.

5.22.1 Entire Unit Protection

Each RP02 contains a Write Protection switch labelled READ WRITE/READ ONLY (see Figure 2-1). As explained in Table 3-1, when this switch is placed in READ WRITE position, information may be both read or written on the disk; but when the switch is in READ ONLY position, information can be read from the disk, but cannot be written on it. When a unit which is set to this condition is selected for a Write operation, the appropriate interrupts are raised and the request is inhibited.

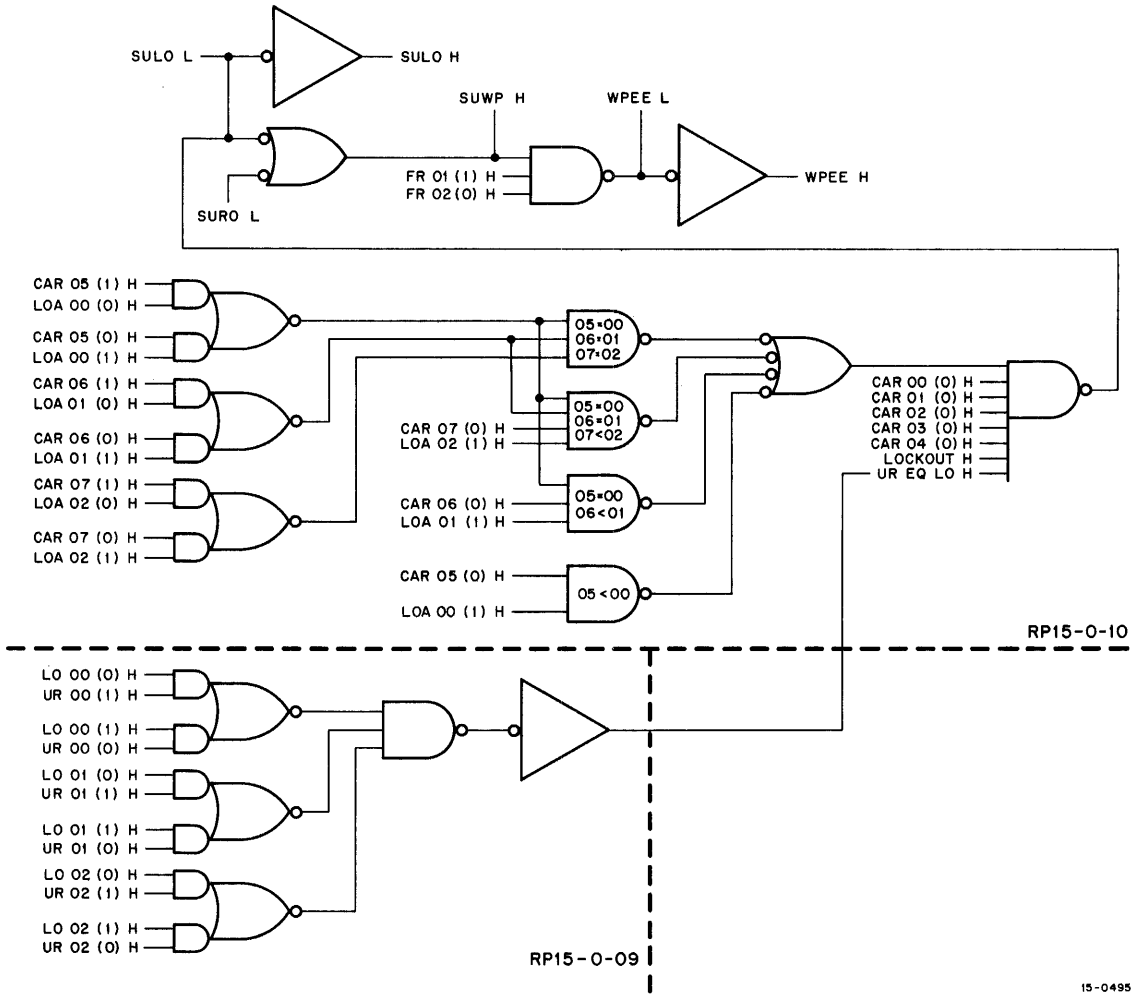


Figure 5-65 Write Protection, Simplified Diagram

The logic for this is shown in Figure 5-65, in which the signal Selected Unit Read Only (SURO L) from the Write Protected unit results in Selected Unit Write Protect (SUWP H). This is ANDed with FR01 (1) H and FR02 (0) H to raise WPEE H/L which, in turn, feeds Status Register A bit 14 and enables the interrupt. The Function Register Code used here ties the operation down to any Write operation except Write Check (not really a Write function).

Note that when a unit is Write Protected it does not inhibit Write operations on other units in the string, but it does inhibit writing on all cylinders of the Disk Pack installed on that drive.

5.2.2 Partial Unit Protection

Mounted on the lower right-hand corner of the RP15 logic panel, is a group of switches labelled as shown in Figure 2-1. To the right of the switch labelled LOCKOUT is a red indicator that lights when

the LOCKOUT switch is in that position. When this indicator is off, if all Write Enable conditions are met, the selected unit is enabled for both Read and Write operations. When this indicator is on (LOCKOUT switch in LOCKOUT position), only the unit designated by the LO toggle switches is protected. On that unit, the number of cylinders which are Write Protected are cylinders zero through the cylinder described by the octal contents of the switch register labelled LOA00-02. This feature is used to protect only cylinders $0\text{-}7_8$ within a single unit. Any unit can be so protected, but only one unit at any one time. Should a unit which has been Selected Unit Lockout designated be selected, and a Write function requested in those cylinders which are protected, the appropriate interrupts would be raised and the Write request would be inhibited.

The logic for LOCKOUT operation is shown in Figure 5-65. Selected Unit Lockout (SULO L), which ORs with SURO L to produce SUWP H, is the AND function of CAR00-04 (0) H, LOCKOUT H, UR EQ LO H, and a composite comparison of CAR05-07 with the Lockout Address switches (LOA00-02).

Since the RP15 can lockout only cylinders $0\text{-}7_8$, CAR00-04 must all be on a 0 for a WPEE to be raised. Also, the LOCKOUT switch, shown on Drawing RP15-0-55, must be in LOCKOUT position (SSLO L) to set the M203 filter flip-flop and yield LOCKOUT H. This flip-flop serves to convert switch operation to logic levels.

The level UR EQ LO H (Unit Register Equals Lockout switches) is the result of comparing the contents of the Unit Register (the unit addressed) UR00-02 with the settings of the LO switches on Drawing RP15-0-55, as seen at the output of their respective flip-flops.

Referring to Figure 5-65, three sets of AND gates compare the High states of LO00-02 (0/1) with the High states of UR00-02 (1/0), respectively, through three associated ORs. The M121 AND/NOR gates, used in this application, comprise pairs of noninverting ANDs feeding single inverting ORs. Figure 5-66 shows the various level distributions for this type gate together with its equivalents. It can be seen that whenever the Lockout Register does not equal the Unit Register, the level distributions will be as shown in a or b of Figure 5-66; when they are equal, the levels will be as shown in c and d of

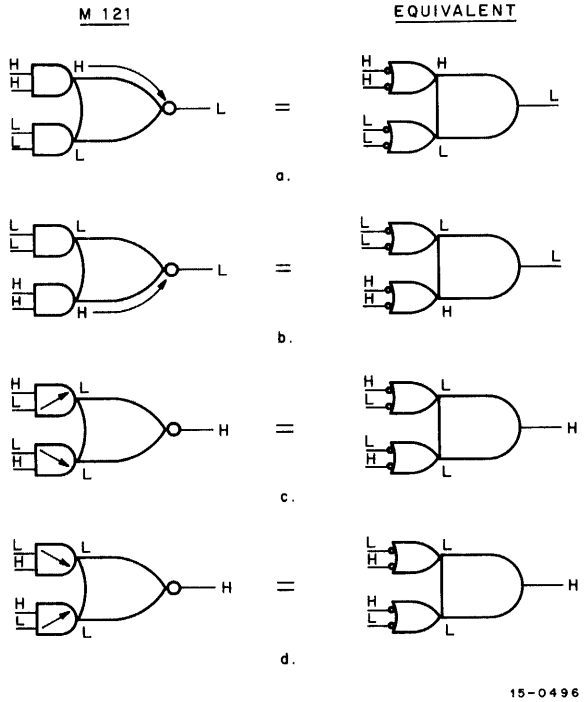


Figure 5-66 Logic Operation of M121 Module

Figure 5-66. Note, then, that if LO00 differs from UR00, the output of its associated OR gate will be low, thereby inhibiting the AND gate and preventing WPEE from being generated. The same is true for the other two Unit Register and Lockout switch digits. If all three digits are alike, all three OR gate outputs will be high and another condition will be met for the Write Protect Error Enable.

The final condition required for the generation of SULO L is the comparison of the Cylinder Address Register (CAR05-07) with the settings of the Lockout Address switches (LOA00-02) to determine if the cylinder address requested has been locked out for Write operations. The logic to determine this develops the following equation:

$$CAR05\text{-}07 \leqq LOA00\text{-}02$$

This equation states: "See if the number in CAR05-07 is equal to or less than the number set in LOA00-02. If so, raise SULO L." This circuit is required to produce an output only if the CAR is equal to or less than the LOA.

As configured, the circuit consists of an OR gate, fed by four AND gates. The four ANDs are fed by an arrangement of signals which checks for equality between all three sets of comparative bits, then checks each CAR bit against its comparable LOA bit to determine which is larger.

Equality is checked by the three AND/NOR gate combinations that check CAR05-07 against LOA00-02 in the same manner that LO00-02 was checked against UR00-02. As shown in Figure 5-65, the four ANDs are fed in such a manner as to check for equality in all three digits through to a difference in the least significant digit. Since the outputs of the ANDs are ORed, any condition can enable SULO L, and, provided the Function Register bits are as indicated, Write Protect Error will be enabled.

5.23 STATUS CONTROL

The RP15 Status Control is shown on Drawings RP15-0-09, -10, and -11. This control serves a status reporting function and controls the termination of an operation either immediately upon sensing an error or at the end of that sector through the control flip-flop JB DN. It also contains the logic for establishing the BUSY status.

Referring to Figure 5-67, the Header Not Found Error (HNF ERROR H) occurs when three consecutive index pulses (SUIP H) are received while looking for a header that has not been found. The expression that enables the counting of the two HNF flip-flops (HNF A and HNF B) is:

$$(READ + WRITE) \cdot HNF\ B\ (0) \cdot NORMAL$$

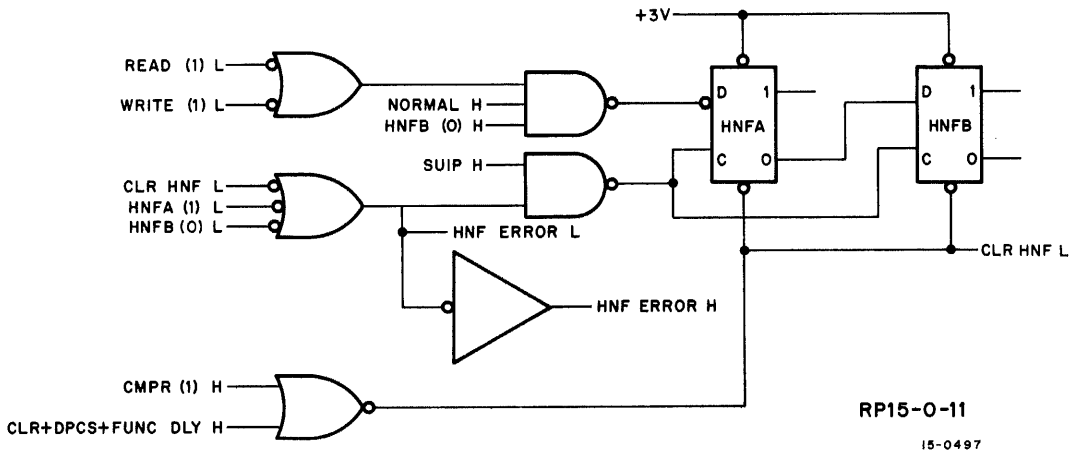


Figure 5-67 HNF Status Control, Simplified Diagram

Note that if CMPR is set, or if the operation is a format instruction (not Normal), then HNF A and HNF B cannot be counted. HNF A and HNF B are cleared by CMPR (1) or CLR + DPCS + FUNC DLY L. FUNC DLY occurs at the beginning of each function such as Read or Write. CMPR is set when the desired header is found. Therefore, HNF A and HNF B begin in the 0 state during a Read or a Write and increment in the following manner with each index pulse (SUIP H):

HNF A	HNF B	
0	0	
1	0	
1	1	
0	1	(error condition)
0	0	

The error state is expressed as:

$$\text{HNF A (0)} \cdot \text{HNF B (1)} \cdot \overline{\text{CLR + DPCS + FUNC DLY + CMPR (1)}}$$

If the error condition state is reached before CMPR is set, HNF ERROR L is raised and remains latched until the next CLR + DPCS + FUNC DLY L.

The logic for BUSY is shown in Figure 5-68 as two sets of cross-latching OR gates. BUSY indicates that the control is actively performing a function and should not be interrupted. BUSY is set by either EXECUTE L or INITIATE L. One of these signals occurs at the beginning of each function. If it is an initiate-type function, BUSY is cleared a standard 4-μs later by TAG RESTART L. If it is an execute-type function, BUSY is cleared with JOB DONE L at the completion of the function. BUSY is also cleared by the OR of CLR H and MAINT (1) H.

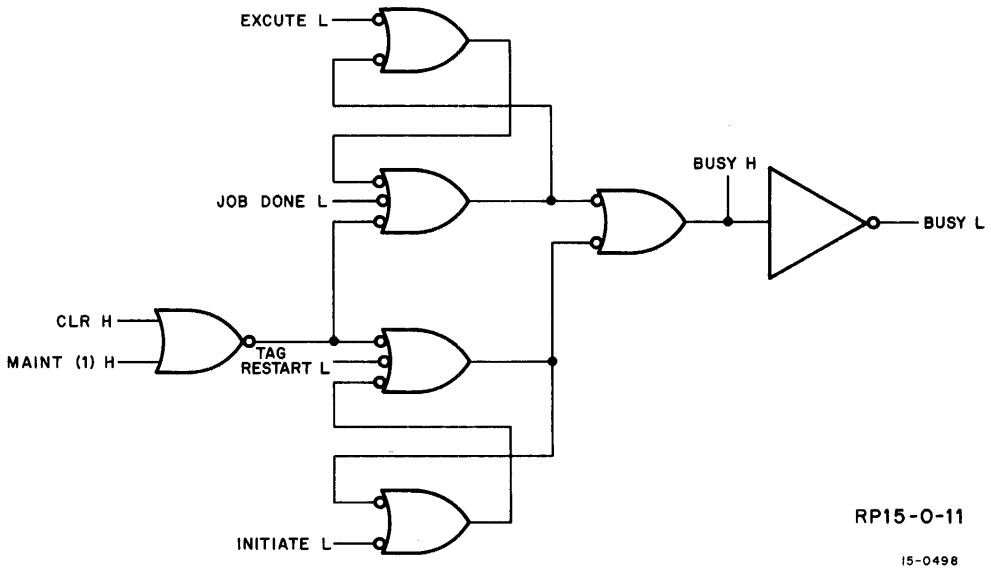


Figure 5-68 Busy Status Control, Simplified Diagram

The Programming Error Enable (PEE) flip-flop, shown in Figure 5-69, sets at IOP 4 (B) time on those instructions which are illegal during BUSY. They are:

DPLZ
DPWC
DPLO
DPLA
DPCN (or any instruction which simulates continue)
DPCA
DPLF
DPCS

NOTE

See Paragraph 3.13 for definitions.

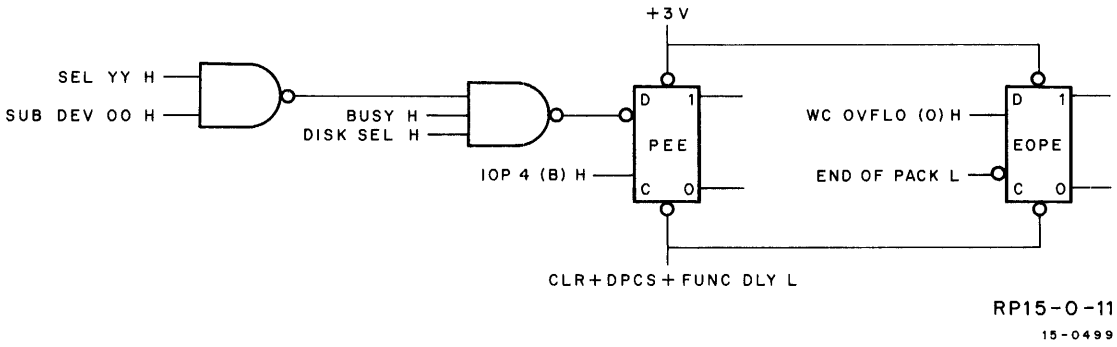


Figure 5-69 PEE and EOPE Status Control, Simplified Diagram

The equation that enables the set of PEE is as follows:

$$\text{DISK SEL} \cdot \text{BUSY} \cdot [\overline{\text{SEL YY}} + \overline{\text{SUB DEV 00}}]$$

PEE and EOPE flip-flops are reset with CLR + DPCS + FUNC DLY L.

The End of Pack Error flip-flop (EOPE), shown in Figure 5-69, will set on WC OVFLO (0) H if END OF PACK L is present, indicating the end of pack has been reached without WC overflow. END OF PACK L means an overflow occurred from the CAR in the middle of a record transfer. It occurs on the following count:

CAR	HAR	SAR
312_8	23_8	11_8

This will happen on an INC SAR and if WC has not as yet set.

The Longitudinal Error Enable flip-flop (LEE), shown in Figure 5-70, is strobed by LP TEST (1) H which is set at the end of each sector during the word parity bit of the longitudinal parity word. During the reading of a sector, each 36-bit word is XORed into the LPR, including the longitudinal parity word. The result should be all 1s in the LPR. The test for this condition is a 36-bit AND gate shown on Drawing RP15-0-26. If any bit is a 0 at this time, either -LPR A EQ ONES L or -LPR B EQ ONES L will be true. This condition enables setting of LEE flip-flop that will set on LP TEST (1) H, thereby enabling the set of the LE flip-flop at the end of that sector (SECTOR END H). Both LE and LEE are cleared by CLR + DPCS + FUNC DLY L.

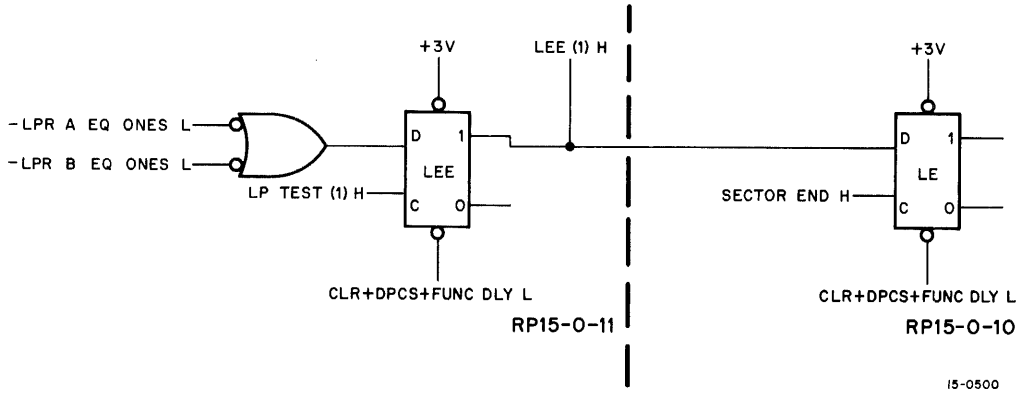


Figure 5-70 Longitudinal Error Status Logic, Simplified Diagram

As shown in Figure 5-71, the signal Selected Unit Seek Underway (SUSU L) is the result of the ANDing of Selected Unit On Line (SUOL H) with Selected Unit Not Ready (-SU RDY H) and Selected Unit Seek Not Incomplete (-SUSI H). This means that if the disk is on line, as long as it is not ready, and if a Seek Incomplete has not been raised, an SUSU will be indicated. The moment a disk is ready or an Incomplete Seek is detected, this indication will be terminated.

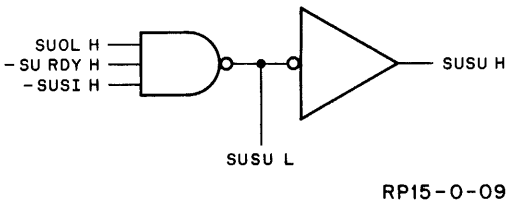


Figure 5-71 SUSU Status Control Logic

The Status Control flag logic is shown in Figure 5-72. DISK FLAG H, which is sent to the interrupt system to indicate termination of operation, is the OR of ERROR FLAG L, ATT FLAG L, or JOB DONE L.

JOB DONE L is generated at the end of a sector and after the ERASE GATE flip-flop has cleared. ATT FLAG L is raised on an attention signal from any drive. ERR FLAG L is raised when any of the error conditions shown as OR gate inputs on Figure 5-72 occur.

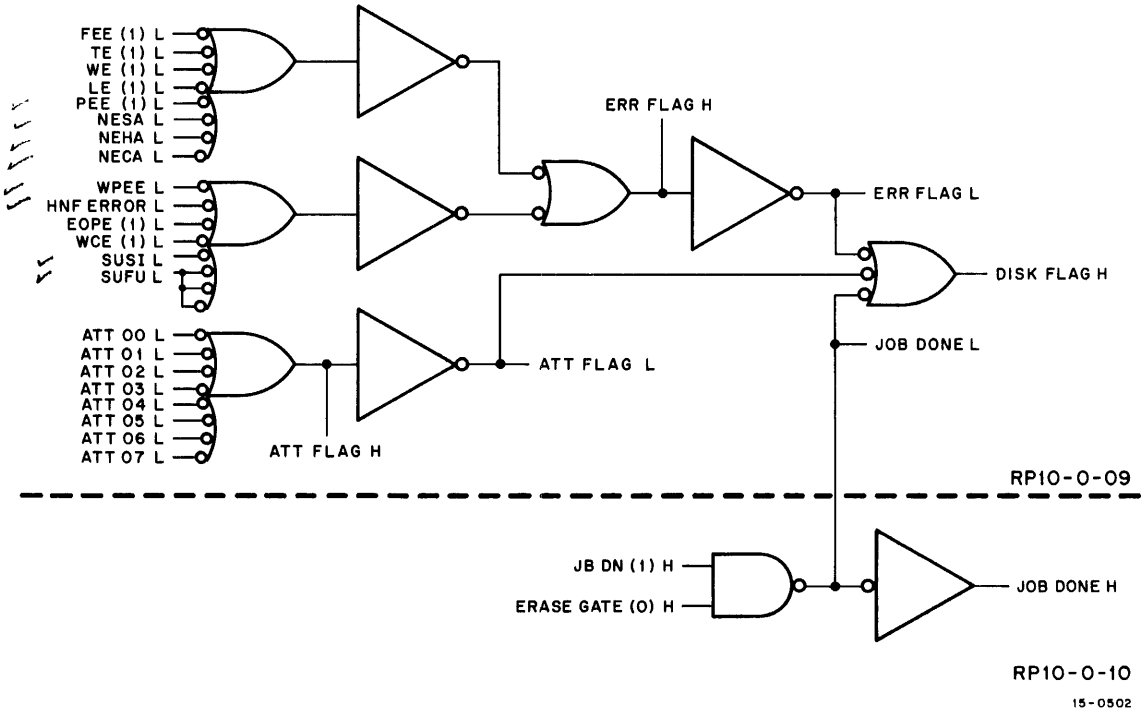


Figure 5-72 Status Control Flag Logic, Simplified Diagram

As can be seen from Figure 5-73, JB DN flip-flop will set under two conditions: either immediately upon certain conditions (SET JOB DONE L) or at the end of a sector under other conditions (SECTOR END H). The flip-flop is reset by CLR + DPCS + FUNC DLY L.

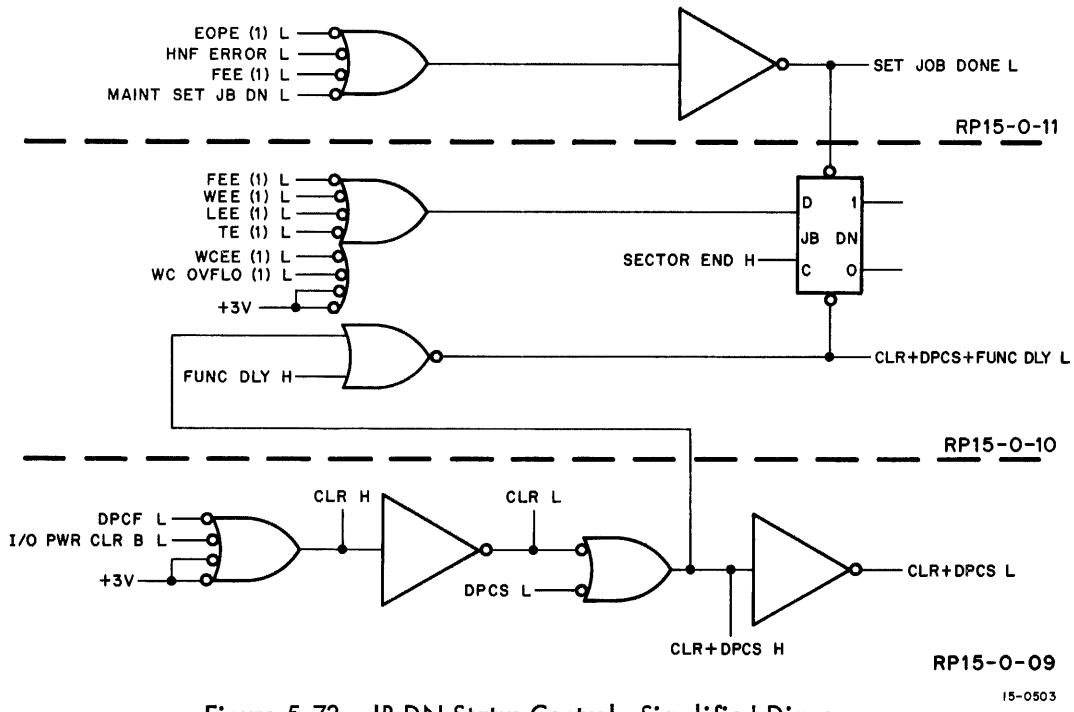


Figure 5-73 JB DN Status Control, Simplified Diagram

Those conditions that preset JB DN are:

EOPE(1) + HNF ERROR + FEE(1) + MAINT SET JB DN

Those conditions that merely enable it to set at the end of the present sector are:

FEE(1) + WEE(1) + LEE(1) + TE(1) + WCEE(1) + WC OVFLO(1)

The Format Error Enable flip-flop (FEE) (Figure 5-74) will be set-enabled when HEADER H and PARITY (0) H are both present, indicating a parity error in a header word. The flip-flop is strobed with TEST PARITY H. FEE(1) L latches the FEE set until cleared by CLR + DPC + FUNC DLY L. If no format error exists, FEE(0) H will AND with LPR B EQ ZEROS H to set CMPR on the transition of HDR END to (0) L. CMPR will latch up upon setting and cannot be cleared until SET IDLE L.

The Word Error Enable flip-flop (WEE), shown in Figure 5-75, sets on -HEADER H and PARITY (0) H when strobed with TEST PARITY H, which occurs at the end of each word read. When WEE sets, it indicates a parity error in a data word, it latches up until cleared by CLR + DPC + FUNC DLY L, and it enables the setting of WE flip-flop, which then sets at the end of that sector.

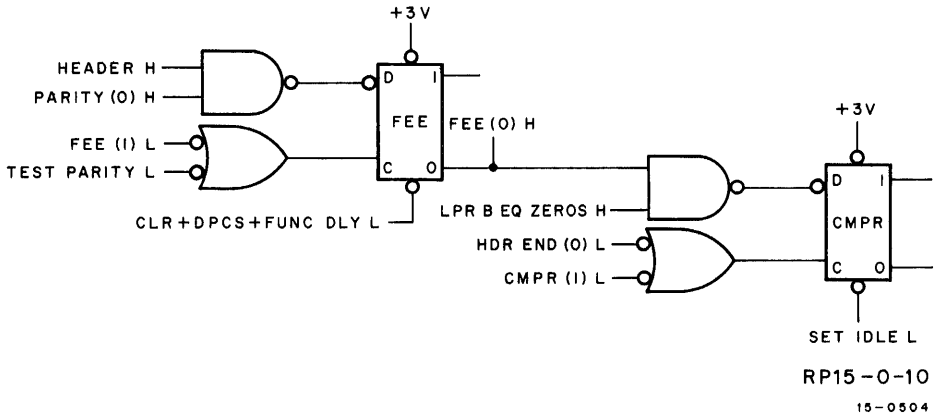


Figure 5-74 Format Error/CMPR Status Logic, Simplified Diagram

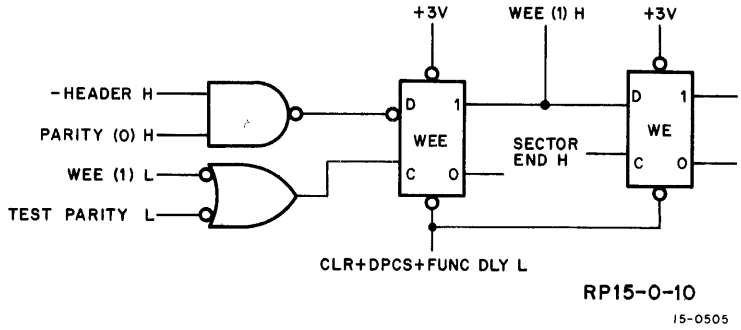


Figure 5-75 Word Error Status Logic, Simplified Diagram

As shown in Figure 5-76, the Write Check Error Enable flip-flop (WCEE) is set during a Write Check function (Function 7) if a corresponding 36-bit word read from the disk differs from the 36-bit word assembled in the Buffer Register. Comparison of the Buffer Register and the Shift Register is accomplished by a 36-bit wide XOR gate shown on Drawing RP15-0-24, -25, and -26. If the two registers differ, the signal -WCC H is generated (not Write Check Compare). WCEE flip-flop is strobed at the end of each 36-bit word read from the disk by LPR STB L, thereby setting WCEE if the function is a Write Check (FR00,01,02 (1) H) with CMPR set, and if the word read is other than a longitudinal parity word (SWC OVFLO (0) H). WCEE is latched when set and can only be cleared by CLR + DPCS + FUNC DLY L. When it sets, WCEE enables WCE flip-flop, which sets at sector end and enables JB DN to set at the same time.

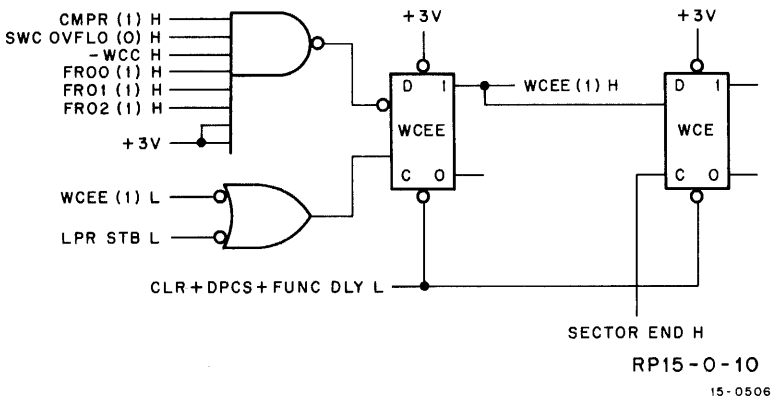


Figure 5-76 Write Check Error Status Logic, Simplified Diagram

5.24 INTERRUPT CONTROL (API)

The RP15 Interrupt Control is shown in Figures 5-77 and 5-78, and in Drawing RP15-0-12. The API Control shown in the drawing consists of a standard M104 Module. This module performs the necessary operations to synchronize a priority interrupt in the PDP-15 on receipt of DISK API RQ H from the status control logic shown in Figure 5-77.

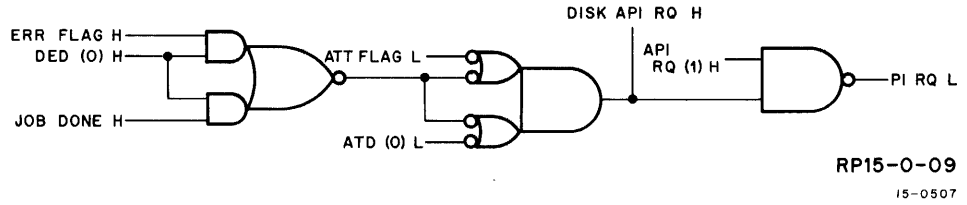


Figure 5-77 Priority Interrupt Status Logic, Simplified Diagram

The conditions for DISK API RQ H can be expressed as follows:

$$DED(0)\cdot(ERR\ FLAG + JOB\ DONE) + (ATT\ FLAG\cdot ATD(0))$$

This expression states that a Disk API Request will be raised on either an Error Flag (ERR FLAG) or a Job Done (JOB DONE) flag, provided the Done and Error Flag Disable (DED (0)) has not been set, or, on an Attention Flag (ATT FLAG), if the Attention Flag Disable (ATD (0)) has not been set.

DISK API RQ H then enables the API REQ flip-flop within the M104 (Figure 5-78) which, on receipt of I/O SYNC (B) H, is set to produce API RQ (1) H. This signal is then ANDed with DISK API RQ H in Figure 5-77 to yield PI RQ L. PI RQ L results in a PROG INT RQ to the PDP-15.

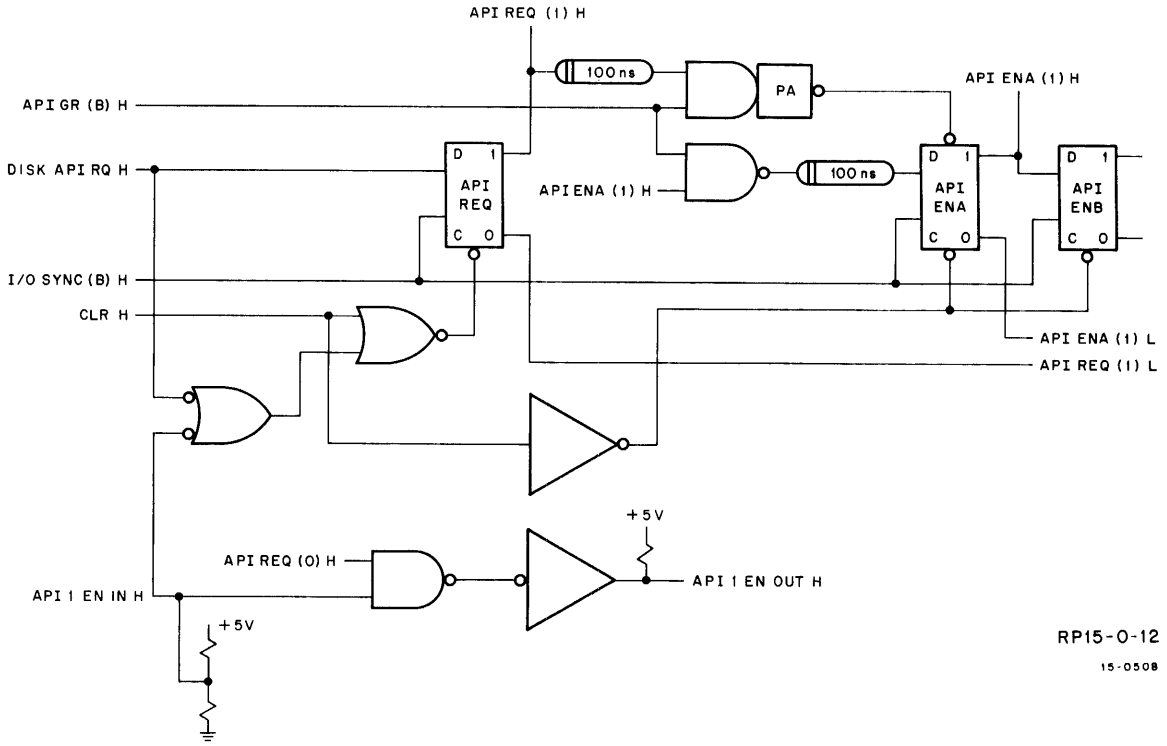


Figure 5-78 M104 Block Diagram for API

5.25 MAINTENANCE CONTROL

The RP15 Maintenance Control circuit is shown in Drawings RP15-0-03 and -04. The Maintenance Control replaces the Disk Pack Drive for maintenance purposes by providing the looping logic and storage facilities necessary to operate the RP15 without the disk as a load.

The purpose of the 6-bit Maintenance Register MR00-05 is to look like a disk to the controller (see Figure 5-79). In Write mode, information from memory enters the Buffer Register in two 18-bit words; it is then transferred to the Shift Register and shifted out, one bit at a time. Normally, each bit would be placed on the disk; in Maintenance mode, it enters the Maintenance Register instead, entering at MR05 (MAINT DATA H) and shifting left (MR SHIFT EN H) as each additional bit is shifted in.

The programmer has control of these shift pulses and can issue them one-at-a-time, at will, with the Maintenance Instruction. He must, however, keep track of the number of shifts so that after each six shifts he can pause and examine the contents of the MR for successful transfer.

This register is a standard shifting register and operates in the same manner as the SR described in Paragraph 5.13. The signal IOB TO MR EN H, applied to each IOB input AND gate, is the inversion of -MR SHIFT EN L which, in turn, is the result of the following (see Figure 5-80):

SEL YY · IOB 09 · SUB DEV 00

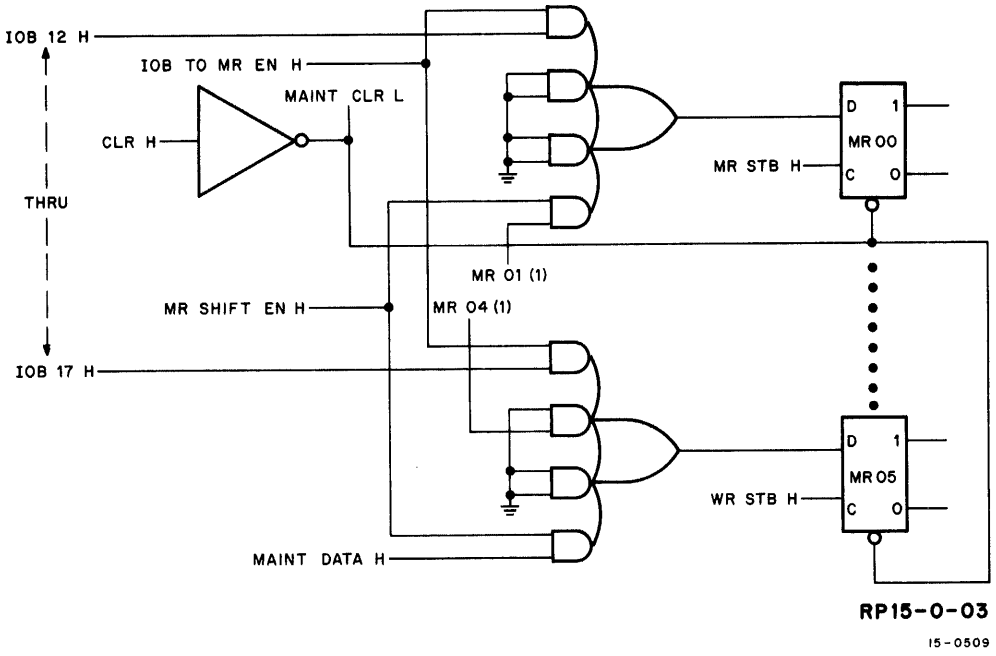


Figure 5-79 Maintenance Register, Simplified Diagram

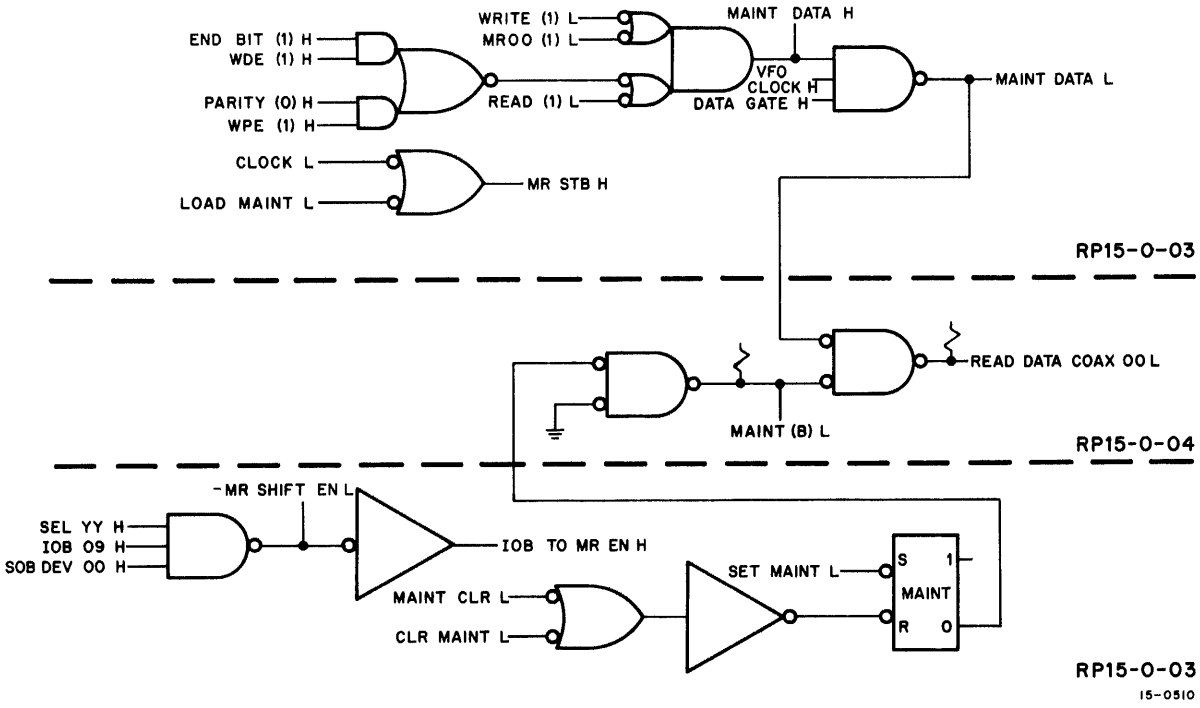


Figure 5-80 Register Control Logic, Simplified Diagram

The register is cleared by MAINT CLR L, the inversion of CLR H, and is strobed by MR STB H, the OR of CLOCK L + LOAD MAINT L.

The logic for MAINT DATA H is the result of the following equation (see Figure 5-80):

$$READ(1)\cdot MR00(1)+WRITE(1)[END\ BIT(1)\cdot WDE(1)+PARITY(0)\cdot WPE(1)]$$

This equation states that if the controller is doing a Read (READ (1) L) then MAINT DATA H looks at the state of MR00 flip-flop; if the controller is performing a Write (WRITE (1) L), then MAINT DATA H is the result of either END BIT (1) H together with Write Data Enable (WDE (1) H) or PARITY (0) H ANDed with Write Parity Enable (WPE (1) H).

MR STB H is the result of CLOCK L from the Data Separator Control (Drawing RP15-0-08) and LOAD MAINT L, which results from IOB 09 H (AC bit 09 (1)) and decoding of the instruction DPEM L from the IOT Selection circuit described in Paragraph 5.3.

As shown in Figure 5-81, the Maintenance Instruction (DPEM - 706401) can perform various operations determined by AC bits 09 through 17 (IOB 9-17 H). The operations performed by these bits are described in Table 3-2. The programmer must set up these AC bits when the instruction is issued. For example, if the programmer issues DPEM, with AC bit 09 on a 1 (IOB 09 H), these conditions will yield LOAD MAINT L. This signal will raise MR STB H, permitting MR00-05 to be loaded with whatever is in bits 12-17 of that same word.

NOTE

IOB 10 and 11 are ineffective in this case, which means that MAINT flip-flop cannot be set and MAINT (B) L cannot enable the buffer gates shown on Drawing RP15-0-04.

When the DPEM instruction is issued with AC bit 09 on a 0 (-IOB 09 H), AC bits 10-17 are then interpreted as maintenance signals to be described.

When this condition exists it will AND with AC bit 10 on a 0 (-IOB 10 H) to clear the MAINT flip-flop, thereby disabling the AND gates that simulate the signals normally received from the drive. When AC bit 10 is set (IOB 10 H), the opposite is true; the MAINT flip-flop is set and the gates are enabled.

When bit 11 is set, the Selected Unit Index Pulse (MAINT SUIP L) is simulated. Bit 12 simulates a Sector Pulse in the same manner. If bit 13 is set, the Maintenance Control will set JOB DONE. Setting bit 14 increments the Current Address Register; while bit 15, when set, increments the Word Count Register. If bit 16 is set, the Sector Address Register is incremented. Successive setting of this bit will cumulatively increment the HAR and CAR.

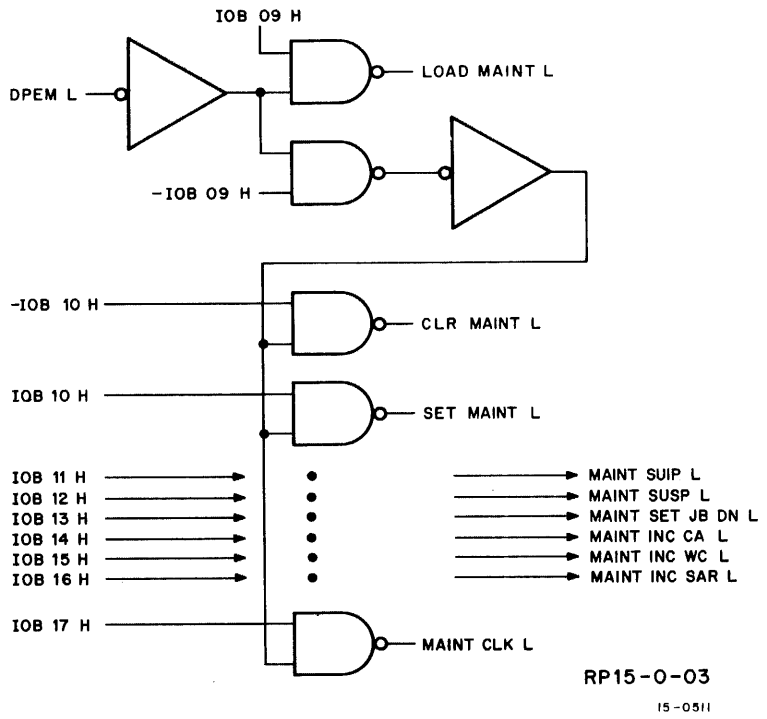


Figure 5-81 DPEM Decoding, Simplified Diagram

When set, bit 17 results in IOB 17 H; this signal yields MAINT CLK L, which is the signal that shifts a single bit. As such, it is similar to a data cell. When this pulse is issued, the control will shift one single bit either from the MR into the SR, or from the SR into the MR, thereby simulating a Read or a Write operation, respectively. During Read, the bits in the MR can be made to cycle around on themselves, eliminating the need for continuous reloading. If the programmer loads a pattern such as 25_8, the sequence circulates and simulates a disk pattern condition.

The Maintenance Control Buffers are shown on Drawing RP15-0-04. In this logic, the various control signals, that are normally generated and sent to the disk, are ANDed with MAINT (B) L and then doubled back into the controller as the proper response usually received from the disk as a result of the signal generated.

MAINT (B) L, shown on Figure 5-80, is the buffered version of MAINT (1) L (same as MAINT (0) H). It is ANDed with MAINT DATA L to yield READ DATA COAX 00 L.

Referring to Drawing RP15-0-04, the loads on the output of each driver terminate the cables to prevent ringing, and, during operation, provide the correct collector loads for the cable drivers. Note that READ DATA COAX 00 L is created from MAINT DATA L, which is shorted back to simulate information that would normally come from the disk.

5.26 INTERFACING THE DRIVE

The RP15 interface to and from the RP02 Disk Pack Drive is shown on the right-hand side of Figure 5-1 and in Drawings RP15-0-46, -47, and -48. The drivers used for this purpose are all type M622; receivers are all type M510. Drawing RP15-0-53 is the cable diagram.

5.27 INTERFAGING THE I/O

The interfacing circuits between the RP15 and the PDP-15 I/O are shown on the left-hand side of Figure 5-1 and in Drawings RP15-0-49, -50, and -51. The driver modules are all type M622; receivers are type M510. Drawings RP15-0-52 is the cable diagram.

CHAPTER 6
MAINTENANCE

6.1 INTRODUCTION

RP15 maintenance philosophy conforms to that of other DEC equipment; i.e., an optimum amount of preventive procedures performed on a routine schedule eliminates many costly equipment breakdowns, and forecasts impending failures long before they occur. When a specific item does fail, the design of the equipment is such that quick replacement of modular elements restores the equipment to service in minimum time. In this chapter, procedures are divided into preventive and corrective categories.

6.2 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed at periodic intervals to ensure proper equipment operation and minimum unscheduled down time. These tasks include visual inspection, operational checks, cleaning, adjustment, and replacement of borderline, or partially defective, parts.

Preventive maintenance scheduling is determined by the existing environmental and work-load conditions at the installation site. Under normal conditions, a schedule of preventive maintenance, consisting of inspection and cleaning every 600 hours of operation, or every four (4) months, whichever occurs first, is recommended. Relatively extreme conditions of temperature, humidity, or dust and/or abnormally heavy work loads demand more frequent maintenance.

Preventive maintenance procedures for the RP02 Disk Pack Drive are not included in this manual. For those procedures, refer to the Memorex Maintenance Manual supplied with each RP02.

6.2.1 Test Equipment Required

Maintenance activities for the RP15 require the standard test equipment and special materials listed in Table 6-1, plus standard hand tools, cleaners, test cables, and probes.

Table 6-1
Test Equipment Required

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 260
Oscilloscope	Tektronix	Type 547 or 454
Plug-In-Unit	Tektronix	Type 1A1
X10 Probe	Tektronix	
X1 Probe	Tektronix	
Hand Unwrapping Tool	Gardner-Denver	H812A505 244-475
Hand-Operated Wire-Wrap Tool with 504221 bit for 30 AWG Wire and 500350 Sleeve	Gardner-Denver	14H1C
Module Extender	DEC	Type W982
Diagnostic Self-Test Routines	DEC	MAINDEC-15-D5HA-D MAINDEC-15-D5DA-D MAINDEC-15-D5EA-D MAINDEC-15-D5FA-D

6.2.2 Mechanical Checks

Inspect the RP15 Controller periodically as follows:

Step	Procedure
1	Inspect the controller for completeness and general condition.
2	Clean the interior and exterior of the cabinet using a vacuum cleaner or clean cloth moistened in nonflammable solvent.
3	Inspect all wiring and cables for cuts, breaks, fraying, wear, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.

6.2.3 Electrical Checks (Timing Adjustments)

Each month proceed as follows:

Step	Procedure
1	Power down system. Remove all cables in slots H19-H24 and in slots J19-J24. Cables should be marked with appropriate locations.
2	Remove M622 Modules located in H14, H15, and H16. Place them in slots H17, J23, and J24.

(Continued on page 6-3)

Step	Procedure
3	Power up system. Set accumulator switches to 760032. Load RP15 Instruction Test. After tape is loaded and the Teletype® bell rings, lower AC switch 00.
4	Set up oscilloscope for internal sync on probe no. 1. Place probe no. 1 on C24F2. Adjust top potentiometer in slot C24 until trace on oscilloscope is a 1.5-μs high level.
5	Place probe no. 1 on C24T2. Adjust lower potentiometer in slot C24 until trace on oscilloscope is a 350-μs high level.
6	Place probe no. 1 on C25F2. Adjust top potentiometer in C25 until trace on oscilloscope is a 50-μs high level.
7	Set accumulator switches to 760130. After bell rings, lower AC switch 00.
8	Place probe no. 1 on C07T2. Adjust lower potentiometer in C07 until trace on oscilloscope is a 20-μs high level.
9	Place probe no. 1 on A05P2. Adjust potentiometer in C06 until trace on oscilloscope is a 4-μs high level.
10	Power down system. Remove M622 Modules located in slots H17, J23, and J24. Replace them in locations H14, H15, and H16.
11	Replace all cables removed in Step 1.
12	Power up system. RP02 disk drive must be on line and ready.
13	Press I/O RESET. Place probe no. 1 on CLOCK H, D17L2. Place probe no. 2 on CLOCK GATE H, D17P1. Adjust potentiometer in slot C15 until leading edge of pulse on probe no. 1 falls exactly in the middle of the high level on probe no. 2.
14	Load the following program from the accumulator switches. Disk pack must be formatted correctly before this step.

```
100/    703302    CAF
        200000    LAC 0
        706344    DPCA
        777400    LAW-400
        706364    DPWC
        200001    LAC 1
        706464    DPLF
        706341    DPSJ
        600107    JMP .-1
        600100    JMP 100

0/      010000    CA = 10000
        011000    FUNCTION = READ & GO
```

®Teletype is a registered trademark of Teletype Corporation.

(Continued on page 6-4)

Step	Procedure
15	Start program at location 100. Place probe no. 1 on E14B1. Place probe no. 2 on F11E2. Measure the delay between the leading edges of probe no. 1 and probe no. 2. (Measure at the 50 percent points of the first pulses in trace only.) Record the delay on paper (≈20 ns).
16	Place probe no. 1 on D17L2. Place probe no. 2 on F11H2. Adjust potentiometer in location E12 until the delay between probe no. 1 and probe no. 2 is equal to recorded delay from Step 15.

6.2.4 Margins

Since the RP15 contains integrated circuits, the standard margining techniques are not required. However, margining of other elements of the PDP-15 are required as called for in individual maintenance manuals.

6.3 CORRECTIVE MAINTENANCE

Standard troubleshooting techniques should be adequate to isolate trouble quickly in the RP15. When an inoperative module is located, replace it with one from spares and return the defective module to DEC for repair or replacement. DEC offers an optional spare modules kit containing one spare for each module. Recommended Module Spares are given in Table 6-2.

Table 6-2
RP15 Recommended Spares

Module	Spares	Module	Spares	Module	Spares
M002	1	M149	1	M312	1
M104	1	M160	1	M401	1
M111	1	M161	1	M405	1
M112	1	M203	1	M420	1
M113	1	M204	1	M510	1
M115	1	M207	1	M602	1
M117	1	M212	1	M606	1
M119	1	M216	1	M611	1
M121	1	M302	1	M622	1
M133	1	M311	1	M627	1
M135	1			M911	1

6.3.1 General Corrective Procedures

Before beginning troubleshooting procedures, ensure that the PDP-15 processor is operating properly. Refer to the specific maintenance manual to determine status. Also examine the maintenance log to determine if the fault occurred before and note what steps were taken to correct the condition. Visually inspect the physical and electrical security of all cables, connectors, modules, and wiring. Particularly check the security of ground connections between the controller and the system. Defective grounds can produce a variety of faults.

6.3.2 Diagnostic Testing

DEC provides special diagnostic programs (MAINDEC) to assist in localizing faults within the equipment. Functionally, the programs fall into two categories: diagnostic and reliability. Diagnostic programs isolate genuine go/no-go type hardware failures that are easily recognizable; reliability programs isolate failures that are more difficult to detect because they are marginal in nature and/or occur infrequently or sporadically.

The family of test programs are written so that, when run successively, they test the equipment beginning with small portions of the hardware and gradually expanding until they involve the entire machine. To accomplish this, the test programs are built around instructions and portions of instructions whose demands upon equipment capabilities progress from simple transfers and skips to the most involved data manipulations and computations. As portions of the system are proven operable, they become available to succeeding tests for use in checking out unproven portions of the machine.

6.3.2.1 RP15 Instruction Test - This test utilizes the self-contained maintenance hardware that the RP15 Controller provides. It conducts an off-line test of data transfer paths as well as basic circuitry. In this paragraph, a brief summary of this test is given. For complete details refer to MAINDEC-15-D5HB-D.

To load the test:

Step	Procedure
1	Load tape into reader.
2	Place BANK MODE switch to BANK MODE.
3	Set address switches to 17700.
4	Press I/O RESET and then READ IN.

To start the test:

Step	Procedure
1	Power down.
2	Remove all cables from slots H19-H24 and J19-J24 (all cables should be labelled).
3	Remove M622 Modules from slots H14, H15, and H16.
4	Insert M622 Modules just removed into slots H17, J23, and J24.
5	Power up. (The RP15 is now able to run using only the maintenance logic.) To place the RP15 back on-line, simply reverse Steps 1 through 5.
6	Set address switches to 200.
7	Select AC switch options from Table 6-3 (see NOTE below).
8	Press I/O RESET and then START.

NOTE

It is suggested that the following be done for the first complete pass of the program. Set AC switch 6 and clear all others (AC switch 4 should also be set if API is not available). This allows all failing tests in the program to make themselves known via TTY output. The failing tests should then be worked on one at a time, starting with the first that failed and working toward the last, using AC switch 0 to select each failing test.

Table 6-3
AC Switch Options for Instruction Test

AC Switch	Function
0	Set to request a manual intervention at the completion of the test currently in progress, or at the beginning of the program. The program indicates when it has acknowledged the setting of the switch by ringing the TTY bell. At this time, the operator may select a specific test by setting the desired number in AC switches 12-17, and then clearing AC switch 0.
1	When set, it will cause a failing test to loop without halting (whether or not the test continues to fail). When cleared, and AC switch 6 is also cleared, the program will halt at the end of the failing test. The operator may press CONTINUE to repeat the test; or, if an oscilloscope loop has been provided for the failing test, he may load the starting address of the oscilloscope loop into the address switches, press I/O RESET and START. The oscilloscope loops provided attempt to duplicate the failing portion of a test in the simplest way possible.
2	When set, it will delete all TTY messages and cause the TTY bell to ring when an error is detected.
3	Set to delete ringing the TTY bell on detecting an error.

Table 6-3 (Cont)
AC Switch Options for Instruction Test

AC Switch	Function
4	Set to indicate that API is not available.
5	Set to loop tests 67 to 150 (data transfer tests) after running tests 00 to 150
6	If AC switch 0 was not used to select a test, and AC switches 1-3 are not set, and a test fails while this switch is set, the program will output the error message and go on to the next test.
12-17	Set to indicate the test number desired. Used in the following manner: Step — Procedure 1 — Set AC switch 0. 2 — Set AC switches 12-17 to indicate desired test number. 3 — Clear AC switch 0 The selected test will loop forever until interrupted by either an error or AC switch 0.

On starting, the program will output the question:

WISH TO CHANGE IOT'S (TYPE Y OR N)?

If the operator types Y, two additional questions will be output, one at a time, allowing the operator to change the two Device Select Codes (DSC) associated with the RP15 IOTs. Following each question, the operator must respond with the two digits that will replace that particular DSC. The two questions will appear as follows:

CHANGE DSC 63 TO ?
CHANGE DSC 64 TO ?

If AC switch 4 is not set, the following question will be output:

WISH TO CHANGE API CHANNEL ADDRESS (TYPE Y OR N)?

If the operator types Y, the following will be output:

CHANGE CHANNEL FROM 64 TO ?

At this time, the operator must respond with the new two digit API channel address. The program will indicate the end of a pass by typing:

END

In analyzing errors, the failing test number and additional information, when required, are output on the TTY. A complete document, with test descriptions and error explanations, is supplied with each MAINDEC. The function of each test is explained in the program listing along with a brief description of what caused the error.

6.3.2.2 RP15 Formatter - This program was designed to format RP02P Disk Packs and to perform a confidence check on both Header and Data Fields after formatting. In this paragraph, a brief summary is given of this test. For complete details, refer to MAINDEC-15-D5FB-D.

To load the diagnostic:

Step	Procedure
1	Load tape into reader.
2	Place BANK MODE switch on BANK MODE.
3	Set address switches to 17700.
4	Press I/O RESET and then READ IN.

NOTE

The program is self-starting.

On starting, the program will ask two basic questions via the TTY. The first will appear as follows:

WISH TO CHANGE IOT'S (TYPE Y OR N)?

If the operator types Y, two additional questions will be output (one at a time), allowing the operator to change the 2 DSCs associated with the RP15 IOTs. Following each question, the operator must respond with the two digits that will replace that particular DSC. The two questions will appear as follows:

CHANGE DSC 63 TO ?

and

CHANGE DSC 64 TO ?

The second basic question will appear as follows:

FORMAT WHAT UNITS?

The operator types the unit number of each drive containing a disk pack that requires formatting, and then a carriage return to terminate the line. If only one unit was selected, the operator is required to make one additional decision. The program responds to the one unit request by typing:

WHAT CYLINDER?

If the operator desires to format and check only one cylinder on the unit selected, he may do so by typing the octal cylinder number and then a carriage return to terminate the line. If the entire disk pack is to be formatted and checked, the operator types only the carriage return.

At this time, the status of the NORMAL/FORMAT switch is sensed and, if necessary, the program outputs the message:

SET NORMAL/FORMAT SW TO FORMAT

After completing the format portion, the program will output the message:

SET NORMAL/FORMAT SW TO NORMAL

The program indicates it is finished by typing:

DONE

The program then restarts.

6.3.2.3 RP15 Address Test - The RP15 Address Test is designed to verify all header words on an RP02 Disk Pack and provide a test of head motion. The test will not destroy any data; it is divided into two parts. The first part of the test is a sequential read of all header words on the pack. The second part is a head motion test that has both known patterns and random patterns. The test will exercise from one to eight units. In this paragraph, a brief summary of the test is given. For complete details, refer to MAINDEC-15-D5DB-D.

To load the diagnostic:

Step	Procedure
1	Set the address switches to 17700.
2	Set BANK MODE switch to BANK MODE.
3	Set the data switches to 000000.
4	Press I/O RESET and then READ IN.

NOTE

The program is self-starting.

After the initial typeout, set the Data Switches as follows (normal setting is 000000_8):

SW00=1 Halt on Error Flag

SW01=1 Ignore Error Flag

SW02=1 Eliminate all typeouts

SW02=1 Stay in presently selected cylinder and surface.

NOTE

The Disk Pack Drive must be running and on line. The FORMAT/NORMAL switch must be in NORMAL position. (The position of the write ENABLE/DISABLE switch is unimportant since no writing is done.)

The starting address is 200. If the program starts at address 201, the random number generator initialization and the change IOT message are eliminated. Selecting IOT DSCs and the units are the only operator actions required; these are done from the keyboard.

Starting by initial loading or at location 200, the following messages will be typed:

--RP09/15 ADDRESS TEST--
CHANGE IOT DEVICE CODES? TYPE Y OR N

At this point, only Y for yes or N for no is acceptable. If no, the next message will be:

TEST UNIT

The expected reply is 0 to 7, which indicates the Drive Number and sequence to be tested in. Up to eight inputs will be accepted. Any sequence is acceptable; e.g., 7,7,4,4,0,0,0,0, will test drive 7 twice, drive 4 twice, and drive 0 four times before repeating the sequence.

The next question concerns the amount of iterations for random address searches before exiting that drive. Each iteration requires about three minutes. Any octal number up to six digits is acceptable as an input. Any number of iterations above seven will result in a further query to the operator as to his intentions. A carriage return terminates all answers. A rubout eliminates previous inputs.

After a static controller check, the following message will be printed:

START UNIT X

At the completion of that unit the following is printed:

END UNIT X

If the IOT codes are to be changed, then the presently selected code will be typed; the expected reply will be two octal characters. This reply is followed by a second question, as there are two device codes for the RP15 Controller.

6.3.2.4 RP15 Random Data Exerciser - The RP15 Random Data Exerciser is intended to provide a checkout of the RP15 Controller and up to eight RP02 Disk Packs. The Exerciser is segmented into various parts that test the surface and VFO. This paragraph gives a brief summary of the test. For complete details, refer to MAINDEC-15-D5EB-D.

To load the diagnostic:

Step	Procedure
1	Set the address switches to 17700.
2	Set the BANK MODE switch to BANK MODE.
3	Set the data switches to 000000.
4	Depress I/O RESET and then READ IN.

The program is self-starting upon initial load. Location 200 is the starting address; location 201 will eliminate the initial dialogue. Normal position for the Data Switches is 000000. The operator must ensure that the drives are powered up and on-line. No attempt is made to preserve data.

On each RP02 Disk Pack to be tested:

Step	Procedure
1	Set ENABLE/DISABLE switch to ENABLE on drives to be tested.
2	Set READ WRITE/READ ONLY switch to READ WRITE.
3	Set START/STOP switch to START.

On the RP15 Controller:

Step	Procedure
1	Set FORMAT/NORMAL switch to NORMAL.
2	Set LOCKOUT switch to unmarked (normal) position.

On the PDP-15 set the following:

NOTE

Normal setting of data switches is 000000.

SW00=1 Halt on error flag
SW01=1 Ignore error flag
SW02=1 Print all data errors
SW03=1 Inhibit all typing
SW04=1 Stay in random write/read test

SW05=1 Do not halt on a controller error

SW17=1 Print error for maintenance operations

6.3.2.5 Vibration Tests - Many malfunctions can be located by performing a timing margin check on the PDP-15 while running a particular diagnostic. In addition, a vibration test may be performed on the RP15.

To perform a vibration test:

Step	Procedure
1	Check switches for immunity from vibration and shock by wiggling them and tapping them with the fingers.
2	Check modules for immunity from vibration and shock in two planes. To check the plane perpendicular to the module mounting plane, tap each module handle with the fingers. To check the plane parallel to the module mounting plane, slide a Teflon rod horizontally across the modules. This should be done slowly and twice in each direction. The Teflon rod should be 8-in. long, 3/8-in. in diameter, and should be held between the fingers 6-in. from the end that is applied to the modules. This test will indicate bad components and poor solder joints.

CAUTION

If vibration tests are applied too vigorously, damage to modules could result.

After localizing the fault to within a functional logic element, run a diagnostic which uses all functions of that element. Trace signal flow through the suspected element with an oscilloscope by synchronizing the oscilloscope sweep with control signals or clock pulses. Check for proper levels, durations, rise and fall times, and timing of all input and output signals.

6.3.3 Switch Panel Testing - LOCKOUT, LO, and LOA Switches

Some isolated faults pertaining to lockout addressing can be located via the RP15 Instruction Test. Refer to the writeup supplied with MAINDEC-15-D5HB-D.

6.3.4 Changing Panel Indicator Bulbs

To replace an indicator bulb when it burns out (see Figure 6-1):

NOTE

Panels are separately removable, but cables must be redressed in this case.

Step	Procedure
1	Power down the system.
2	Remove the indicator bezels from the front of the rack. (They snap out.)
3	Remove the two orange and black power supply pairs behind the rack from the indicator rack.
4	Remove the eight interconnecting cables from the module rack.
5	Remove eight screws that secure the indicator panels to the cabinet and carefully remove the two panels from the front.
6	After replacing faulty bulb(s), reassemble in reverse order.

CAUTION

In reconnecting indicator power supply, be sure to connect black tabs to GND and orange tabs to +6.5V, labelled on the edge of the module.

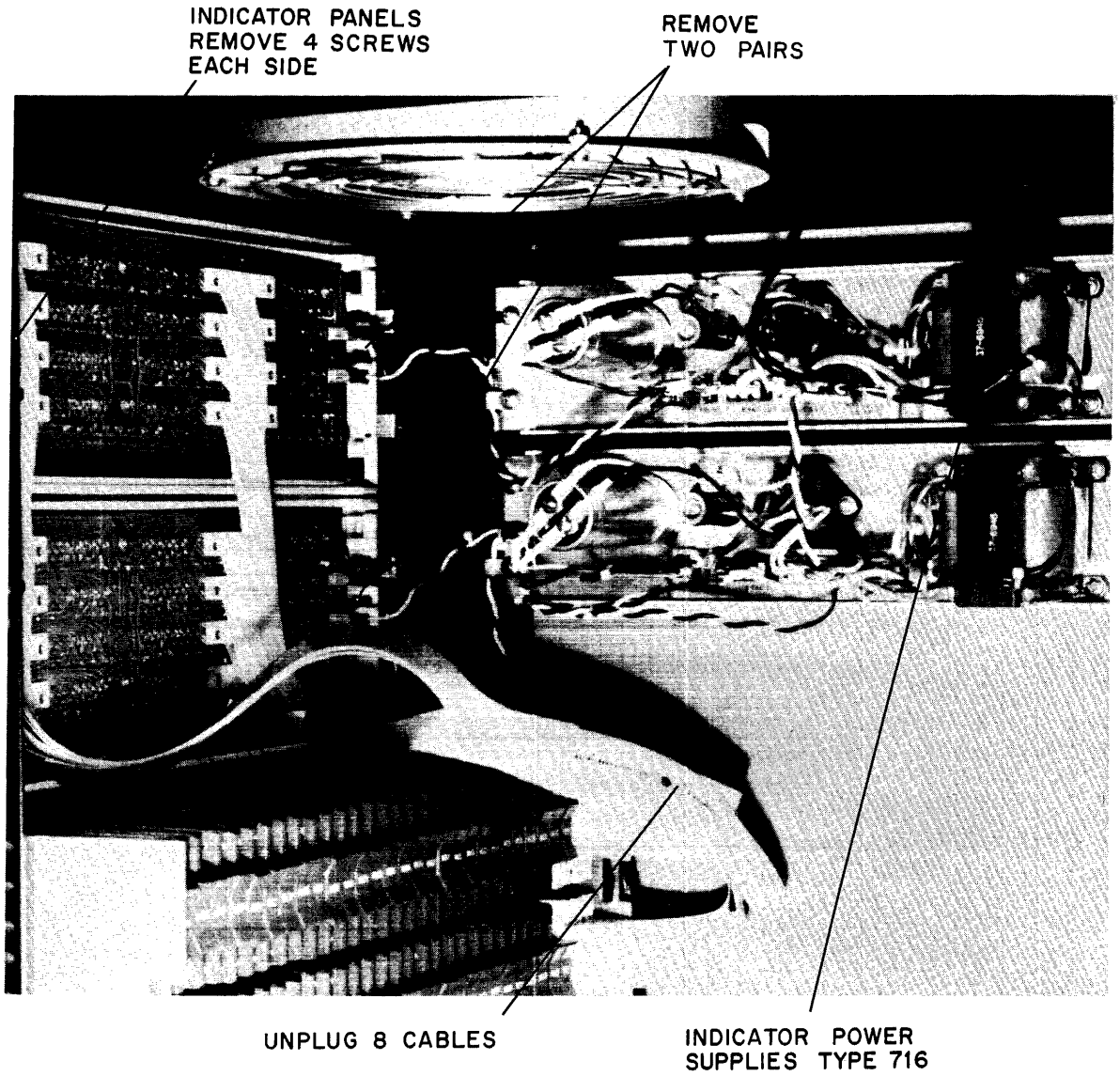


Figure 6-1 RP15 Indicator Panels and Power Supplies

CHAPTER 7
SYSTEM SPECIFICATIONS

7.1 GENERAL

This chapter contains the mechanical description of the RP15/02 System. The various equipment specifications, cable interconnections, and equipment supplied are included in tabular form.

7.2 MECHANICAL DESCRIPTION

The RP15 is housed in an H963 cabinet that contains four H911 mounting panels. The logic utilizes M Series integrated circuit modules. Two indicator panels are located at the top of the unit; switches are located on a logic panel available inside the front door. These panels comprise monitoring and switch facilities for data and address indication and control. The unit contains built-in self-testing facilities, fan assemblies, power supplies for both logic and indicators, and a power control.

The RP15 is shipped complete and factory-tested, including all interconnecting cables to the PDP-15 Computer System. Cables to the RP02 Disk Pack Drive(s) are provided as part of that unit.

Two types of controllers are supplied depending upon requirements: the DEC Type RP15-A for 60-Hz operation, and the RP15-B for 50-Hz operation. The PDP-15 Computer System, when equipped with an RP15 Controller, can accommodate up to eight RP02 Disk Pack Drives per RP15 Controller.

7.3 EQUIPMENT SPECIFICATIONS

The physical, environmental, electrical, and performance specifications for both the RP15 and the RP02 are listed below.

7.3.1 Physical

Dimensions	RP15	RP02
Height	72 in.	39 in.
Width	21 in.	30 in.

(Continued on page 7-2)

Dimensions	RP15	RP02
Depth	30 in.	24 in.
Weight	305 lb	295 lb
Service Clearance		
Front	36 in.	36 in.
Rear	36 in.	36 in.

7.3.2 Environmental

Satisfactory operation is achieved under normal conditions of humidity, shock, and vibration.

Ambient	RP15	RP02
Operating Temp.	55-100°F	60-90°F
Humidity	25-95% Rel	8-80% Rel

7.3.3 Electrical

Power requirements at line cord:

RP15A = 110 Vac 1-ph, 60 Hz @ 7.0A Nominal, 25.0A Surge

RP15B = 220 Vac 1-ph, 50 Hz @ 3.6A Nominal, 13.0A Surge

RP02A = 208 Vac 1 of 3 phases, 60 Hz @ 6.0A Nominal, 25.0A Surge

RP02B = 208 Vac 1 of 3 phases, 50 Hz @ 6.0A Nominal, 25.0A Surge

• NOTE

Three-phase AC power is wired to each unit, but an individual drive will draw current from one phase only. Phases are rotated in a multi-unit system to provide a balanced load.

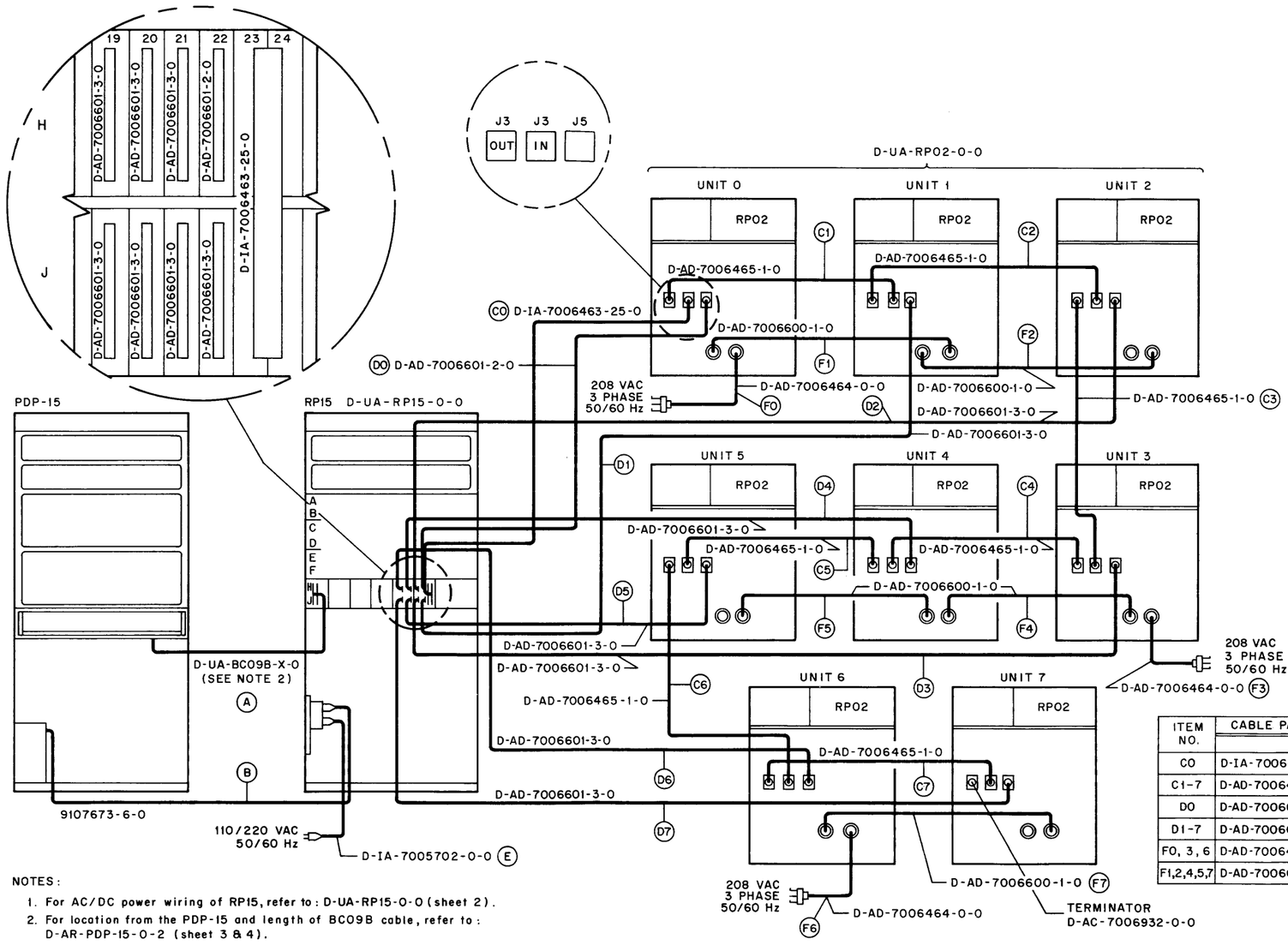
Power/Heat Dissipation:

RP15 = 805W, 2747 Btu/hr

RP02 = 1250W, 4250 Btu/hr

Internal Power: From two self-contained Power Supplies, Types H721 and H716, and one self-contained Type 841B, Power Control providing +10, +5, and -15 Vdc for logic power, 6.5 Vdc for indicator power, and 120 Vac for fans.

Cable Lengths: See Figure 7-1 and Table 7-1.



NOTES:

1. For AC/DC power wiring of RP15, refer to: D-UA-RP15-0-0 (sheet 2).
2. For location from the PDP-15 and length of BC09B cable, refer to: D-AR-PDP-15-0-2 (sheet 3 & 4).
3. Circled letters refer to table 7-1.

ITEM NO.	CABLE PART NO.	UNIT NUMBER							
		0	1	2	3	4	5	6	7
C0	D-IA-7006463-25-0	1							
C1-7	D-AD-7006465-1-0		1	1	1	1	1	1	1
D0	D-AD-7006601-2-0	1							
D1-7	D-AD-7006601-3-0		1	1	1	1	1	1	1
F0, 3, 6	D-AD-7006464-0-0	1			1			1	
F1,2,4,5,7	D-AD-7006600-1-0		1	1		1	1		1

Figure 7-1 Cable Particulars

Table 7-1
Cable Particulars

Cable Interface (See Figure 7-1)	Qty.	Supplied With		From	To	Length Ft	
		RP15	RP02-X			Max.	Std.
A	1	Yes		DW15	RP15	50	7
B	1	Yes		PDP-15	RP15	50	7
C0	1		Yes	RP15	RP02-0	100*	25
C1-C7	1		Yes	RP02-X	RP02-X	100*	8
D0	1		Yes	RP15	RP02-0	50	25
D1-D7	1		Yes	RP15	RP02-X	50	40
E	1	Yes		RP15	outlet	N/A	25
F0, F3, F6	1		Yes	RP02-X	outlet	N/A	25
F1, F2, F4, F5, F7	1		Yes	RP02-X	RP02-X	N/A	8

*Total length of C0 through C7 must not exceed 100 ft.

7.3.4 Performance

Word Transfer Rate = 7.4 μs/word (based on 18-bit word)

Positional Access = 80.0 ms MAX
20.0 ms MIN
50.0 ms AVG

Rotational Access = 25.0 ms MAX
0.0 ms MIN
12.5 ms AVG

Latency Time = 62.5 ms AVG
105.0 ms MAX

Capacity (in 18-bit words) = 80.92×10^6 MAX (8 drives)
10.24×10^6 MIN (1 drive)

Words Available to a Single Addressing = 262,144 MAX
1 MIN

CHAPTER 8
INSTALLLATION

8.1 GENERAL

This chapter is concerned with installation of the RP15. Turn-on and checkout procedures are given to confirm operation of the equipment once it has been installed. Provisions are made for built-in testing of the RP15 alone. These procedures are a part of the checkout.

8.2 UNPACKING

For particular procedures for unpacking, refer to Chapter 4 of PDP-15 Installation Manual, DEC-15-H2AB-D.

8.2.1 Special Handling

The RP15 is packed in accordance with best commercial practice. No special handling procedures are required beyond normal care afforded any piece of scientific equipment of comparable size and weight. Particular care should be exercised in the use of cranes or hoists to prevent damage to the unit.

8.2.2 Inspection

On receipt, the equipment should be inspected for any visible damage in transit, such as dents and abrasions. For general inspection procedures, refer to DEC-15-H2AB-D. Inspect the logic modules for foreign matter which might have lodged in them during shipment. Any damage observed should be reported immediately to both the carrier and the manufacturer. Check the contents of the carton with the shipping document and with Table 8-1. Report any omissions immediately to the local DEC sales office.

8.2.3 Power Requirements

The RP15 is supplied with its own self-contained power supplies and power control. The +10, +6.5, +5, and -15 Vdc requirements of the unit are provided by a DEC Type H721 Power Supply, two DEC

Type 716 Power Supplies, and a DEC Type 841B Power Control. Differences for accommodating either 50 or 60 Hz are made within the basic unit, designated RP15A for 60-Hz and RP15B for 50-Hz operation. Power requirements at the main units are listed in Paragraph 7.3.3.

The RP02 contains its own internal power supply for the transport mechanism and logic circuitry. Ac power for the unit is taken by daisy-chain jumper wiring. Units are wired in phase rotation to equalize ac loading. Power requirements at the main units are listed in Paragraph 7.3.3.

Table 8-1
RP15 Checklist

CUSTOMER: DEC#:
CHECKER: DATE:

I. RP15

A. I/O BUS CABLE (BC09-B) _____
B. REMOTE POWER CABLE (EXTENSION CORD) _____
C. DIAGNOSTIC TAPES, WRITE-UPS & LISTINGS _____
   1. Formatter _____
   2. Instruction Test _____
   3. Address Test _____
   4. Random Data Test _____
D. RP15 MAINTENANCE MANUAL _____
E. RP15 PRINT SET _____
F. RP02 CLEANING KIT _____
G. TERMINATOR FOR LAST UNIT _____
H. SYSTEM SOFTWARE _____
I. ECO STATUS SHEET _____
J. FUSE, 5 AMP SLO-BLOW (5) _____

II. RP02

A. UNIT CABLE _____
B. BUS CABLE _____
C. POWER CABLE _____
D. MAINTENANCE MANUALS (2) _____
E. SPARE PACK FILTER (1 per pack) _____
F. DISK PACK (RP02P) _____
G. DISK PACK LOG _____
H. INSERT KIT, FILE IDENTIFICATION _____
I. KICK PLATE, SIDE (2) _____
J. KICK PLATE FRONT & REAR (2) _____
K. CUP, CASTOR (4) _____
L. SCREW, BINDER HD. #8-32 x .30 (12) _____

8.3 INSTALLATION PROCEDURE

Install the RP15 and RP02/s per site plan. Overall physical dimensions are given in Figure 8-1.

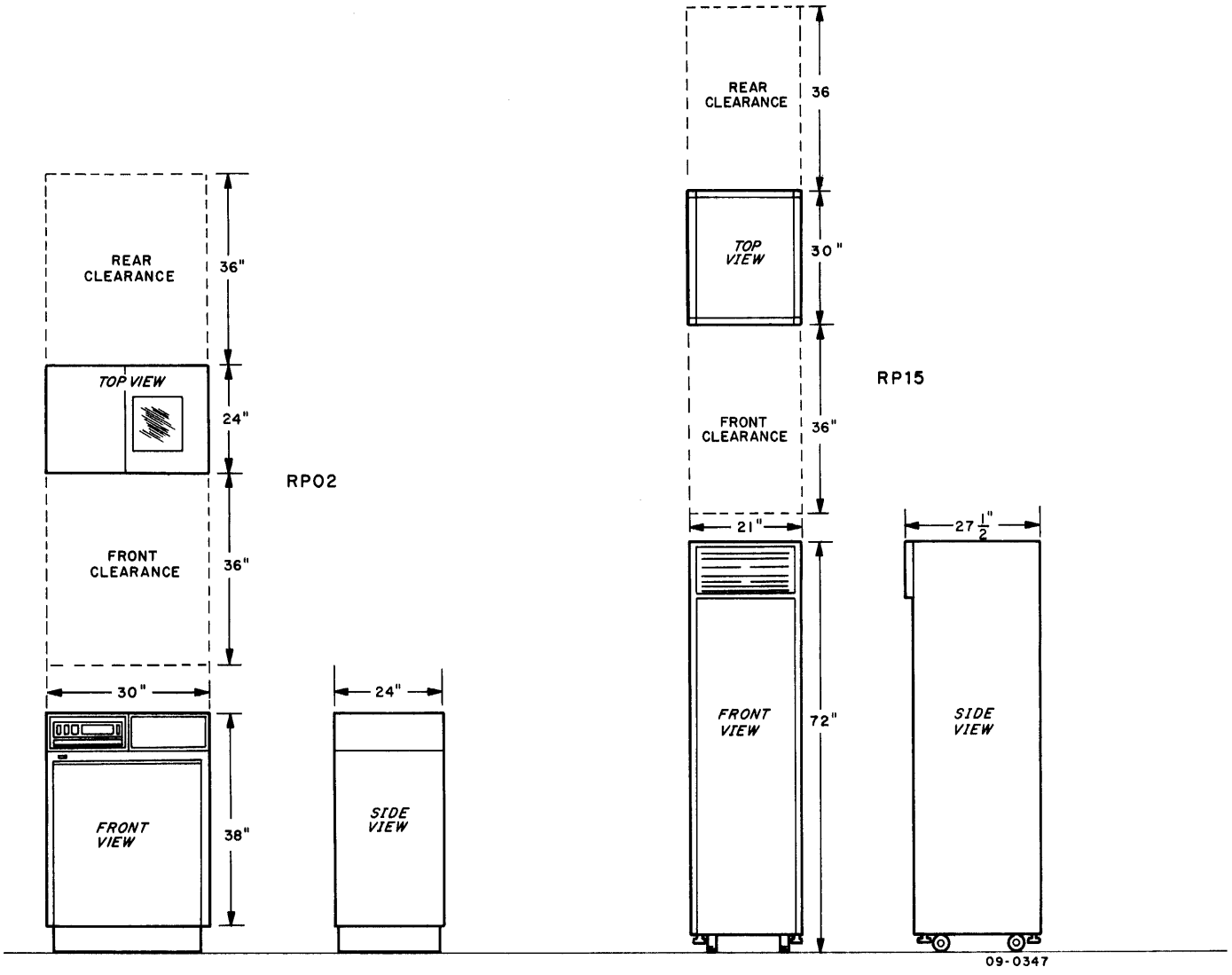


Figure 8-1 RP15/02 Overall Dimensions

8.3.1 Converting to Another Power Source

Equipment is normally shipped with power supplies converted to each customer's requirements. If, however, it becomes necessary to convert the unit to another power source (e.g., from 110 to 220), proceed as follows (see Figures 8-2 and 8-3):

Step	Procedure
1	Remove all power from the PDP-15 and the RP15/02.
2	Remove the two orange jumpers located on the face of the 841B Power Control. These jumpers are marked JUMPER for 110 Vac input (see Figure 8-2).
3	Remove the perforated top on the Logic Power Supply H721 (see Figure 8-2).
4	Remove the jumpers between points 1 and 3, 2 and 4, and 3 and 5, on the terminal block marked TB1 (see Figure 8-3).
5	Add a jumper between points 2 and 3, and 4 and 5 of TB1.

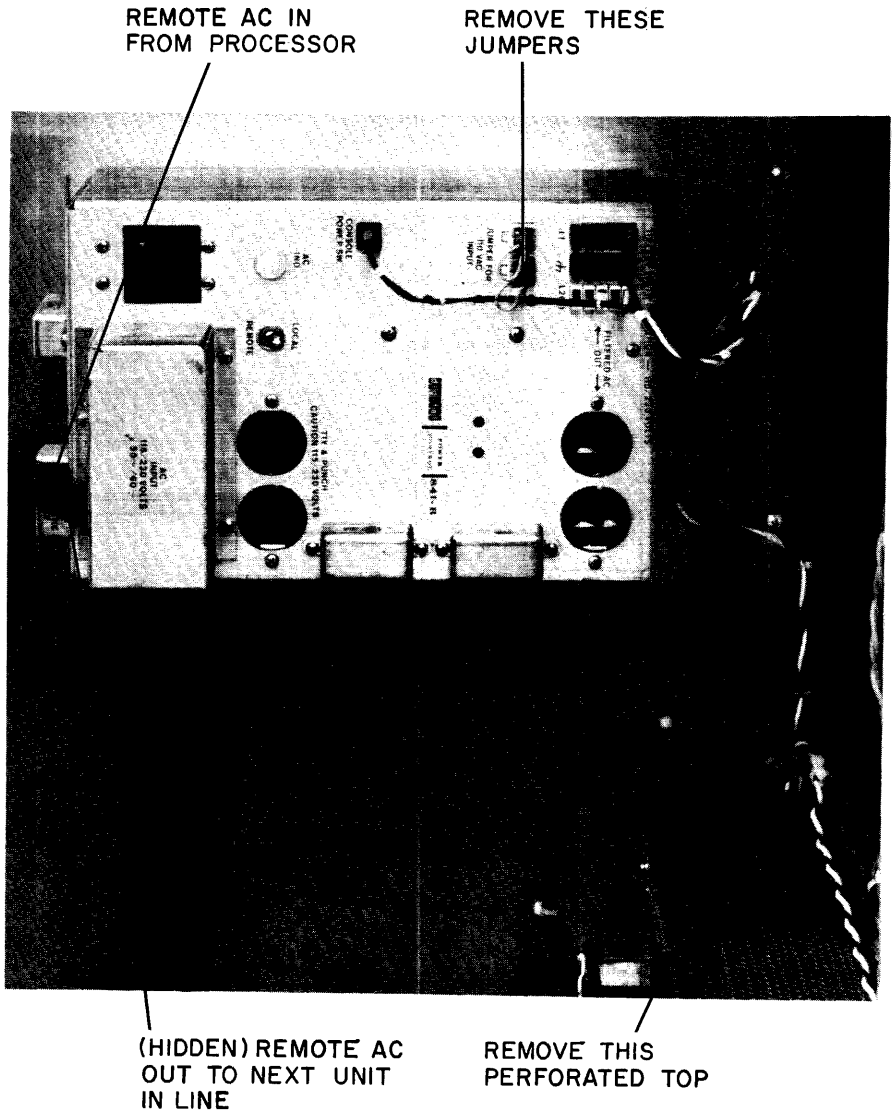


Figure 8-2 RP15 Power Control

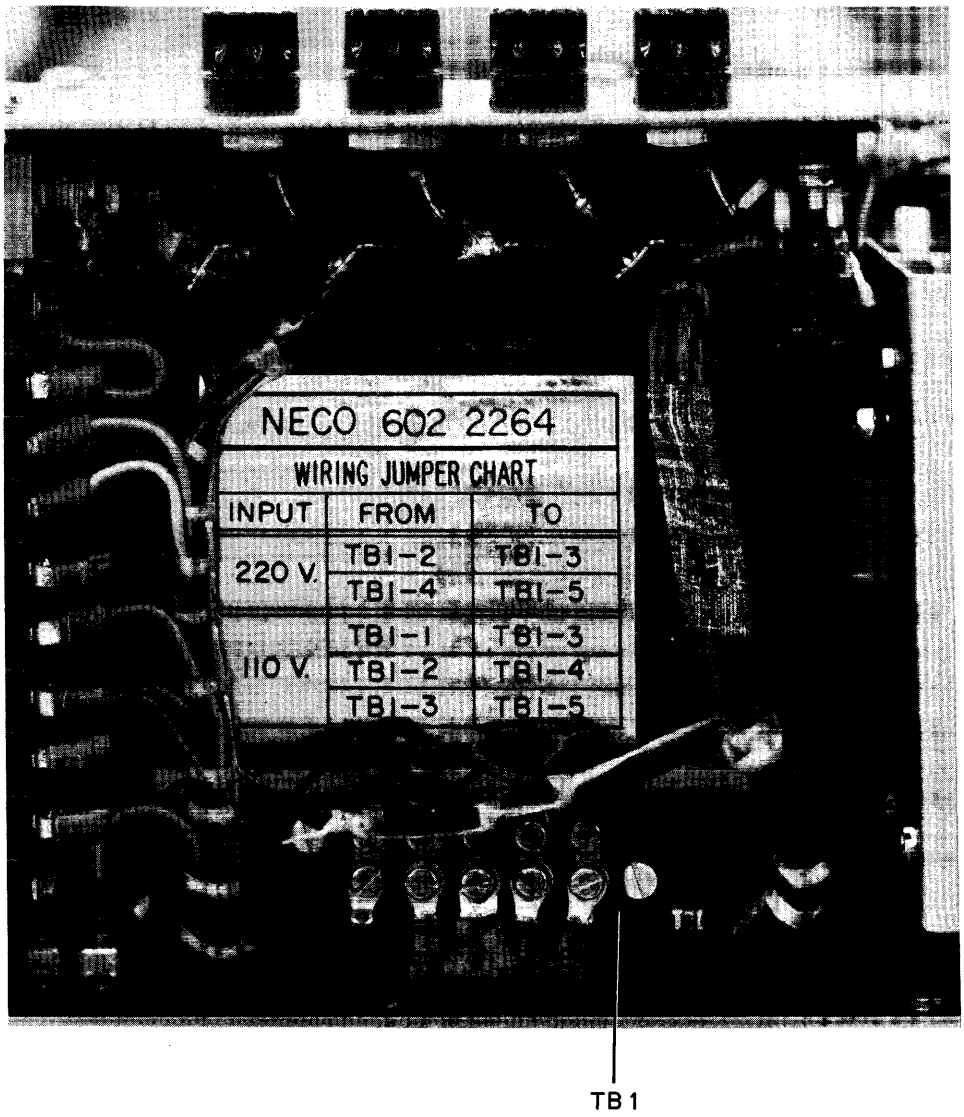


Figure 8-3 RP15 Logic Power Supply Primary Wiring

Five adjustments are provided in the logic power supply Type H721. They are:

a. +5.0V adjust
b. +5.0V over-voltage adjust
c. +5.0V over-current adjust (fold back)
d. +10.0V adjust
e. -15V adjust.

These adjustments are made at the factory.

8.3.2 Installing the RP15 Cabinet

The RP15 Cabinet is provided with roll-around casters and adjustable leveling feet. It is not necessary to bolt the cabinet to the mounting floor unless conditions indicate otherwise (e.g., shipboard installation).

CAUTION

Do not attempt installation until DEC has been notified and a Field Service Representative is present.

Step	Procedure
1	Remove power from all systems.
2	Position the RP15 Cabinet as the first bay to the left of the PDP-15 Processor.
3	Remove the left-hand side panel from the PDP-15 Processor Cabinet and the right-hand side panel from the RP15 Cabinet.
4	Butt the cabinets together while holding the filler strips in place; bolt through both cabinets and the filler strips (see Figure 8-4). Do not tighten the bolts securely at this time.
5	Lower the leveling feet, making sure that the cabinet(s) are not resting on the roll-around casters but are supported on the leveling feet.
6	Level both cabinets with a spirit level and ensure that all leveling feet are seated firmly on the floor.
7	Tighten the bolts that secure the cabinet groups together and then recheck the cabinet leveling. Again ensure that all leveling feet are seated firmly on the floor.

8.3.3 Installing Cables

Normally DEC cabinet interconnecting cables are of standard lengths and are factory installed. In the case where an RP15 is added to a system after it has been installed, only the standard cables to connect the new equipment into the system are supplied. These cables are connected at the installation site, and the termination point of each cable is identified. Proceed as follows:

Step	Procedure
1	Install the grounding cable between a bottom horizontal rack member and either the Processor Main Frame or to a system grounding bus.
2	Connect cables between the RP15 and the RP02 as listed in Table 8-2.
	NOTE When cables are installed, strain-relief cable clamps should be attached to the frame member as shown in Figure 8-5.
3	Tighten connectors, so equipped, into the cable retaining block as shown in Figure 8-5.

(Continued on page 8-7)

Step	Procedure
4	Connect cables between the RP15 and the I/O as indicated in Table 8-3.
	NOTE Install the RP15 physically first on the positive I/O bus string. This is necessary to avoid timing errors.
5	Connect cables, supplied with each RP02, between each Drive in the string.
	NOTE The RP15 requires no margin checking; therefore, this cable is not supplied.
6	Install RP02 Terminator Plug in last RP02 in the string.
7	Connect all power cables including Remote AC lines as shown in Figure 8-2.

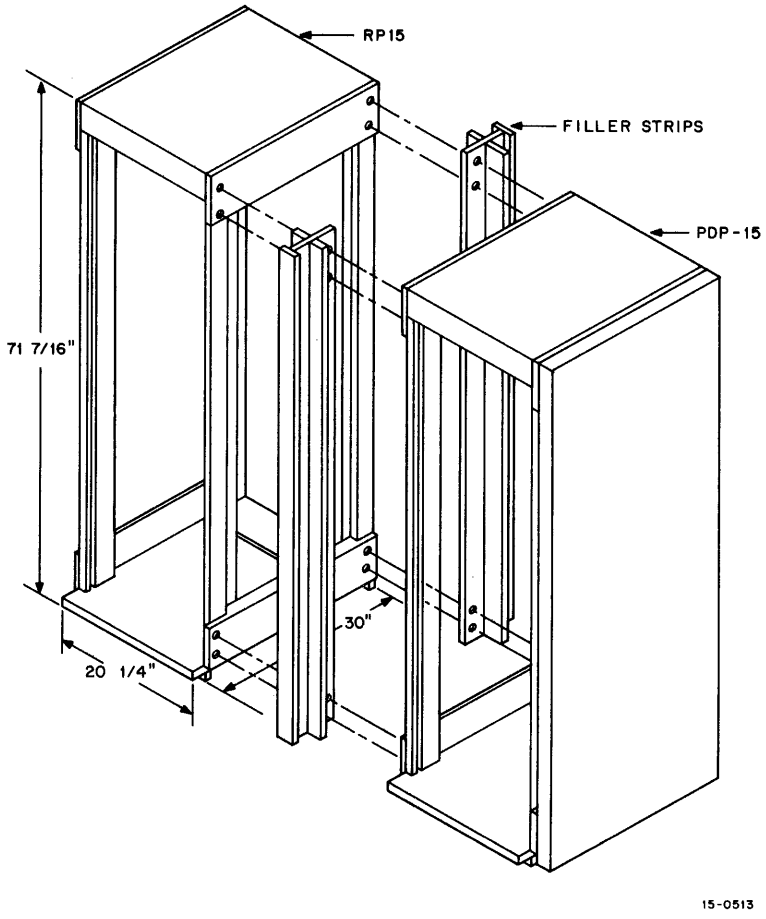


Figure 8-4 RP15 Cabinet Bolting Diagram

Table 8-2
RP15/RP02 Interface Chart

Between		Function	Cable Type	Cable Lgh. (Ft) Max.
RP15	RP02			
H/J-19, 20 21, 22	J5	+5V Terminator Voltage, Select Unit, Read & Write Coax, Attention.	W028	50
H/J-23,24	J3	Tag Lines, Bus Lines, Selected Unit On Line, Read Only, File Unsafe, Ready, Seek Incomplete, Index Pulse, Sector Pulse, Sequence Out, and Cylinder Address.	W850	50

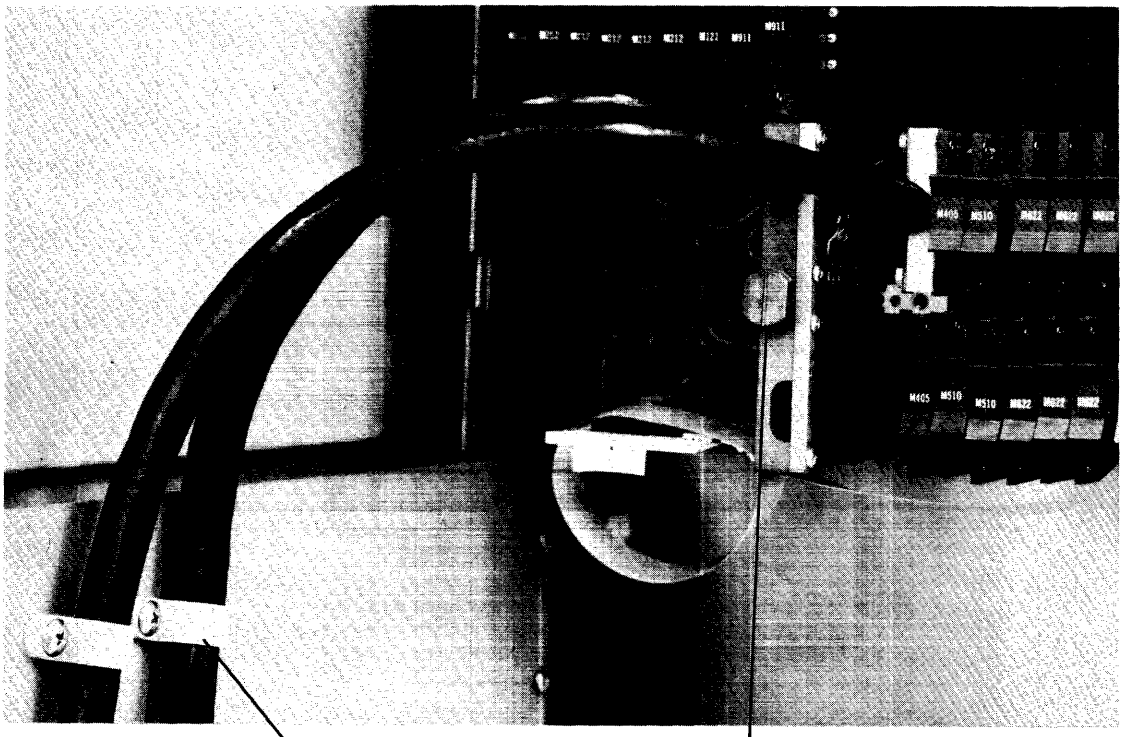


Figure 8-5 RP02 Cable Connections to RP15

Table 8-3
RP15 I/O Interface Chart

Between RP15	Between DW15	Function	Cable Type	Cable Lgh. (Ft) Max.
H-1/2	A-4/5	IO BUS, SYNC, IOPs, SKIP PROG INT, RD RQ, STATUS, PWR CLR, DS, SD	BC09B	7
J-1/2	B-4/5	IO CONTROL SIGS, WRITE RQ, INC MB & CA, API RQ, API GR, API EN, DCH RQ, DCH GRANT, DCH EN		

8.3.4 Setting Unit Number Designator

Once installed, the large unit number designator for each RP02 in line should be set. This static designator is located on the RP02 control panel to the right of the READ WRITE/READ ONLY switch.

To set the unit number designator:

Step	Procedure
1	Raise the top cover of the control panel by releasing the latch located at the back of the RP02.
2	Inside the cabinet, loosen the two thumb screws above the indicator housing and move the glass cover back to gain access to the housing.
3	Move the indicator logo manually to the proper designation for that unit.
4	Replace all hardware in reverse order.

8.4 TURN-ON AND CHECKOUT

When the RP15 has been installed, operation may be verified by proceding as outlined below.

8.4.1 Built-In Testing Without RP02

The RP15 provides self-contained maintenance hardware. The equipment is designed to simulate the RP02, so that the RP15 can be tested and verified without the use of an on-line Disk Pack Drive:

Step	Procedure
1	Power down the system.
2	Remove Bus and Unit Cables to RP02/s (Slots H19-H24 and J19-J24).

Step	Procedure
3	Remove the M622 Modules in locations H14, H15, and H16 on the RP15.
4	Replace these three modules in RP15 locations H17, J23, and J24.
5	Power up the system.
6	Load and run the RP15 Instruction Test, MAINDEC-15-D5HA-D.

8.4.2 Testing With RP02

To perform a final system test:

Step	Procedure
1	Power down the system.
2	Replace the three M622 Modules, repositioned in Paragraph 8.4.1, in their normal positions: H14, H15, and H16.
3	Replace all cables removed in Paragraph 8.4.1.
4	Ensure that all switches are in their normal positions and that all equipment is powered.
5	Load and run the RP15 Random Data Exerciser, MAINDEC-15-D5EA-D.

Digital Equipment Corporation
Maynard, Massachusetts

digital

printed in U.S.A.