Diablo Systems Incorporated

Series 40 Disk Drive · Maintenance Manual

81603 APRIL 1975

24500 Industrial Blvd.
Hayward, California 94545
Phone: (415) 783-3910

Diablo Systems Incorporated
A Xerox Company

ADDENDA

8/75
DATE

PUBLICATION BEING REVISED Series 40 Disk Drive Maintenance Manual-Second Edition Publication No. 81603 4/75 Revision A

PLEASE ENTER THE FOLLOWING REVISIONS AND/OR CORRECTIONS IN YOUR COPY OF THIS MANUAL:

Page 6-5, Section 6.6.3 4; ADD:

Refer to Figure 1, revision "A".

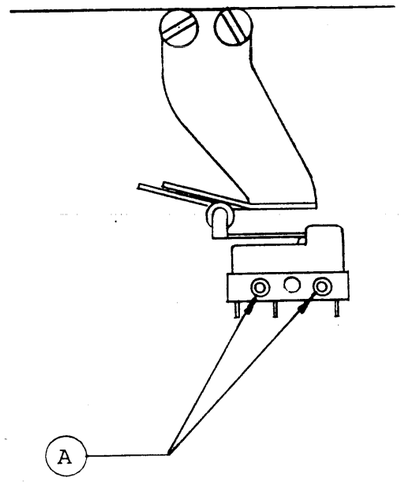


Figure 1 HEAD CARRIAGE RETRACT SWITCH

Page 6-9, Section 6.6.5.1, Items 6, 7, 8, and 11; Change to read:

6. Place the disk drive in the RUN mode.
7. Depress the carriage retract microswitch, which is the top microswitch at the rear end of the bail.
8. Apply power to the drive. The carriage will move forward.
11. Repeat steps (5) through (9) until the clearance between the cone round surface and the alignment bar is 0.006 inches ±.004 inches.

8/75
DATE

Page 6-9, Section 6.6.5.2, first paragraph and items 3 and 5; change to read:

To align the Head Positioner with the Spindle Assembly, it is necessary to use the Alignment Bar (P/N 16438) and the Spindle Cone (P/N 15171). Proceed as follows:

3. Delete item 3. (The tool mentioned is not available or necessary for proper head positioner adjustment).

5. Adjust the Head Positioner until the clearance between the bar and the round portion of the cone is 0.002 inches ±.001 inch.

Page 6-10, Figure 6-23 ALIGNMENT BAR AND CONE

Delete the reference to the "Head Positioner Alignment Tool".

PREFACE

This Maintenance Manual provides the user of a Diablo Series 40 Disk Drive with complete specifications, systems interface information, installation and operation instructions, principles of operation, and maintenance procedures.

All schematic diagrams will be found in a separate booklet entitled "SCHEMATIC DIAGRAMS". This booklet will include only those diagrams applicable to a specific Series 40, and each booklet will be labeled with model and serial numbers identifying it as belonging with that particular machine.

Information in this manual is current as of the date shown on the title page. Applicable change information will be furnished by Diablo Customer Service in the form of revision addenda, and/or Field Service Aid publications. Unless otherwise indicated, all technical specifications are in English terms (inch/pound). Directional or location designations such as "front", "rear", "left", "right", etc. apply to the component in operating position, as observed from the front of the unit. When referring to connections on multi-pin components, the component's PCB location code is given first, followed by a dash and the pin number. When referring to a flip-flop, the pin number for the "Q" output is used. If the flip-flop has two outputs, with neither clearly indicated as the "Q" output, then both pins are used, such as FF H15-6/8.

Printed in the United States of America
Publication No. 81603 – Second Edition

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

FIGURE

SECTION 1
GENERAL DESCRIPTION

1.1 OPERATIONAL CHARACTERISTICS

The Diablo Series 40 Disk Drive shown in Figure 1-1 provides large on-line random access storage and unlimited off-line storage for small, general-purpose digital computers. Its design incorporates features which ensure a high degree of flexibility, reliability, speed of access, and data integrity. It uses both a fixed disk and a removable Type 5440 top loading disk cartridge, for a capacity of up to 100 megabits of data at a recording density of 2200 bits-per-inch (BPI) and an average access time of 38 milliseconds.

The Series 40 Disk Drive is available in two configurations. Model 43 has a lateral track density of 100 tracks per inch (tpi), for a total capacity of 50 megabits. Model 44 has a lateral track density of 200 tpi, for a total capacity of 100 megabits. In addition, several options are available with either model. These are described in Paragraph 1.3, along with a description of the various accessories also available.

The Series 40 consists of six functional groups:

- The Spindle Assembly rotates the recording disks, and provides ventilation for the drive.
- Four Read/Write Head Assemblies "write" data onto, or "read" from the two disks.
- The Head Positioner Assembly moves the read/write heads to the disk track locations commanded by the using system.
- Controls, Indicators, and Interlocks provide the means for front panel operation of the drive, and prevent improper operating sequences.
- The Electronics group accepts, processes, generates, and/or supplies the electrical signals necessary for the disk drive to perform its intended function.
- An external power supply converts AC line power to the several DC operating voltages required by the drive. Normally, this consists of the Diablo Systems, Inc., Model 429 Power Supply furnished with each Series 40 Disk Drive.

The spindle drive motor is mounted on the spindle shaft, eliminating belts, pulleys, and idler systems. This eliminates belt wear and pulley tolerances as factors in spindle speed control, as well as a major source of internal contamination. Spindle speed is controlled electronically, and is independent of normal fluctuations in line voltage or frequency. The air blower for the ventilation system is also mounted on the spindle shaft, eliminating the need for a second motor. Disk contamination from outside sources is virtually eliminated by passing all air drawn into the unit through an absolute no-by-pass air filter. This filter retains 99.97% of all particles 0.3 microns or larger. Filtered air is then directed into both disk areas and through them to cool the electronics areas before exhausting at the rear of the machine. In addition, each disk surface is swept with a cleaning brush each time the drive is powered up.

The head-positioning system's case is designed to contain the strong magnetic field of its drive coil. This reduces stray magnetic flux at the read/write heads to a negligible level, eliminating a common cause of disk system data error. System design also includes temperature compensation to enhance accuracy. This includes appropriate materials selection, component locations to achieve common environment conditions, and, for the 200 tpi drives, electronic compensation for second-order temperature effects.

Head loading is accomplished gently, with no head-to-disk contact, by dashpot regulated solenoid controlled release of compression springs acting directly on the head assemblies. In the event of power failure, the solenoid return spring easily overpowers the head loading springs to unload the heads automatically, providing protection for heads, disks, and data. A system of interlocks also prevents damage to heads or disk surfaces due to operator error.

1.2 GENERAL SPECIFICATIONS

General specifications for the Series 40 Disk Drive are listed in Table 1-1.

1.3 OPTIONS AND ACCESSORIES

The following options and accessories may be included in any Series 40.

Options

- 1500 RPM SPINDLE (100 tpi only) – provides a choice of bit transfer rates. The btr at 1500 rpm is 1.562 mHz, with an average latency of 20 ms.
- ADDRESS COUNTER AND SECTOR MARK – furnishes output signals showing the sector location of the read/write heads at any instant, and generates a pulse to the using system whenever a sector slot on the hub of the disk selected by DISK SELECT passes its transducer.
- WRITE PROTECT – prevents inadvertant writing (recording) over previously recorded data. Either or both disks may be protected.
- VFO – enhances data retrieval reliability by eliminating data errors caused by clock pulse jitter, and provides data/clock separation permitting operation with systems in which missing clock pulses occur, such as Systems 3 hardware.
- DESK-TOP INTERLOCK – provides interlock protection against unsafe cartridge removal in desk top models, similar to that which prevented equipment drawer opening in rack mounted models.

Figure 1-1. Diablo Systems, Inc., Series 40 Disk Drive

- SERIES 30 COMPATIBILITY – provides index and sector marks of 5 μs duration, and reduces addressing response to; Address Acknowledge and Logical Address Interlock occurring 35 ($\pm$ 10) μs for 5 ($\pm$ 2) μs after the leading edge of Strobe. Logical Address Interlock is a pulse, not a dc level.
- UNSEPARATED DATA – provides unseparated read data and clock pulses to the using system.

Accessories

- CABLES – disk drive interconnect cables are available for use when the daisy chain method of operation is used. A controller-drive interconnect cable is also available. All are 50-conductor flat cables.
- TERMINATORS – one per system is required, to be installed in the *output* I/O connector of the last drive in the system chain.
- TYPE 5440 CARTRIDGE – available with or without sector slots.
- POWER SUPPLY – one Diablo Model 429 Power Supply is furnished with each Series 40 Disk Drive, and provides the dc power necessary to operate one drive. The Model 429 operates on either 115 or 220 Vac, 50 or 60 Hz. Additional Model 429 supplies are available as accessories.
- ALIGNMENT CARTRIDGE – necessary for performing adjustments as described in Section 6 of this manual.
- MODEL 500 PROGRAMMABLE TESTER – exercises all seek, read, write functions of the Series 40. It greatly facilitates the performance of alignments described in Section 6 of this manual. Unit can be programmed for use with a standard Series 40, or for use with a Series 40 utilizing Address Mark type format (VFO Option).

Table 1-1.
Specifications

Parameter	Model 43	Model 44
Storage Medium:		
Type	Type 5440 cartridge and a fixed disk.	Type 5440 cartridge and a fixed disk.
Diameter	15 inches.	15 inches.
Lateral Track Density	100 tracks per inch.	200 tracks per inch.
Recording Techniques: (double frequency)		
Tracks	816 (200 plus 4 spares on each surface of each disk.	1632 (400 plus 8 spares on each surface on each disk.
Cylinders	204 (four tracks per cylinder, two per disk.	408 (four tracks per cylinder, two per disk).
Capacity, Bits:*		
Per drive	50,000,000	100,000,000
Per disk	25,000,000	50,000,000
Per inch (innermost track)	2200	2200
Per cylinder	250,000	250,000
Per track	62,500	62,500
Access Time:		
Track-to-track	10ms	8ms
Average	38ms	38ms
Full Stroke	70ms	70ms
Disk Rotation:**	2400 rpm ±2%	2400 rpm ±2%
Average Latency	12.5ms	12.5ms
Bit Transfer Rate	2500kHz	2500kHz
Power Requirement:	+24Vdc ±5%, 6A −24Vdc ±5%, 5A +5Vdc ±5%, 4A	+24Vdc ±5%, 6A −24Vdc ±5%, 5A +5Vdc ±5%, 4A
Heat Dissipation:	900 btu/hr	900 btu/hr
Environment (operating):		
Temperature	50° F to 104° F	60° F to 90° F
Temperature Change Rate	15° F per hour	15° F per hour
Relative Humidity (non-condensing)	20% to 80%	20% to 80%
Maximum Altitude	6000 ft	6000 ft
Environment (storage):		
Temperature	−40° F to 150° F	−40° F to 150° F
Relative Humidity (non-condensing)	5% to 95%	5% to 95%
Physical:		
Width	17-1/2 inches	17-1/2 inches
Height	10-5/16 inches	10-5/16 inches
Weight (w/cartridge)	136 lbs	136 lbs

*The figures shown are nominal. Actual capacity will depend on formatting and data checking methods used.
**1500 rpm available as an option. With 1500 rpm the average latency is 20ms and the transfer rate if 1562kHz.

SECTION 2
INSTALLATION

2.1 DISK DRIVE DIMENSIONS AND CLEARANCES

Figure 2-1 shows the basic dimensions of the Series 40 Disk Drive, including its slide rails for mounting in a standard 19-inch rack cabinet. Rail spacings from 27-1/2 to 28-5/8 inches can be accommodated. The Series 40 I/O connector box remains stationary when the drive is extended, making provision for cable movement unnecessary. The drive extends approximately 20 inches from the rack when opened for disk cartridge insertion or removal, and approximately 31 inches when opened for service.

2.2 UNPACKING

The Series 40 is packed for shipment as shown in Figure 2-2. Remove the machine from the inner packing container, and remove the plastic dust cover. Packing materials should be retained for possible future use. Referring to Figure 2-2, remove the four 7/16" x 4" bolts, washers, and stand-off pillars securing the unit to the plywood base. These are accessible from underneath.

NOTE

DO NOT turn the disk drive upside down!

Next, remove the four slide clamps holding the rack slides to the base. The drive can now be lifted clear of the base.

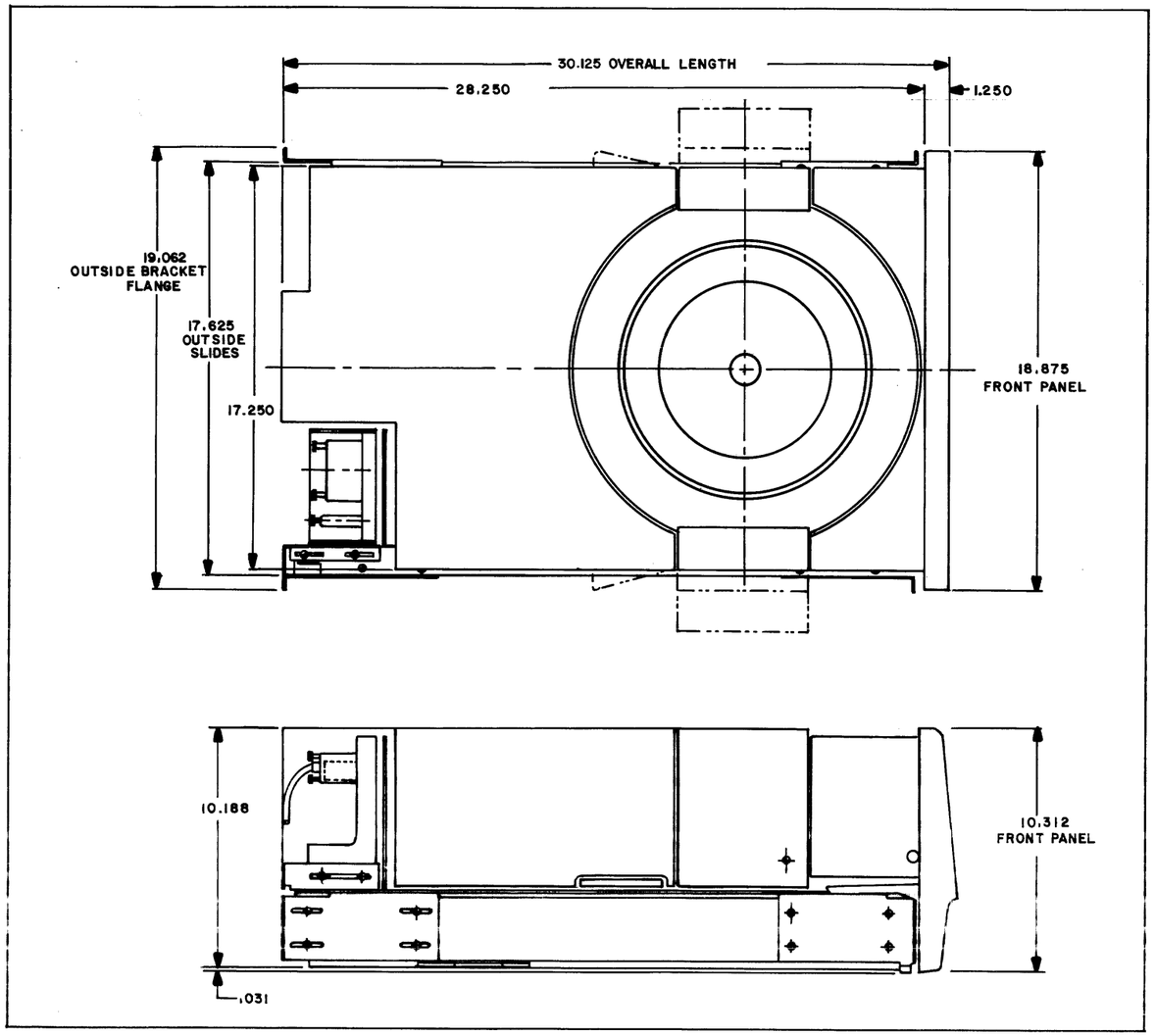


Figure 2-1. Series 40 Basic Dimensions

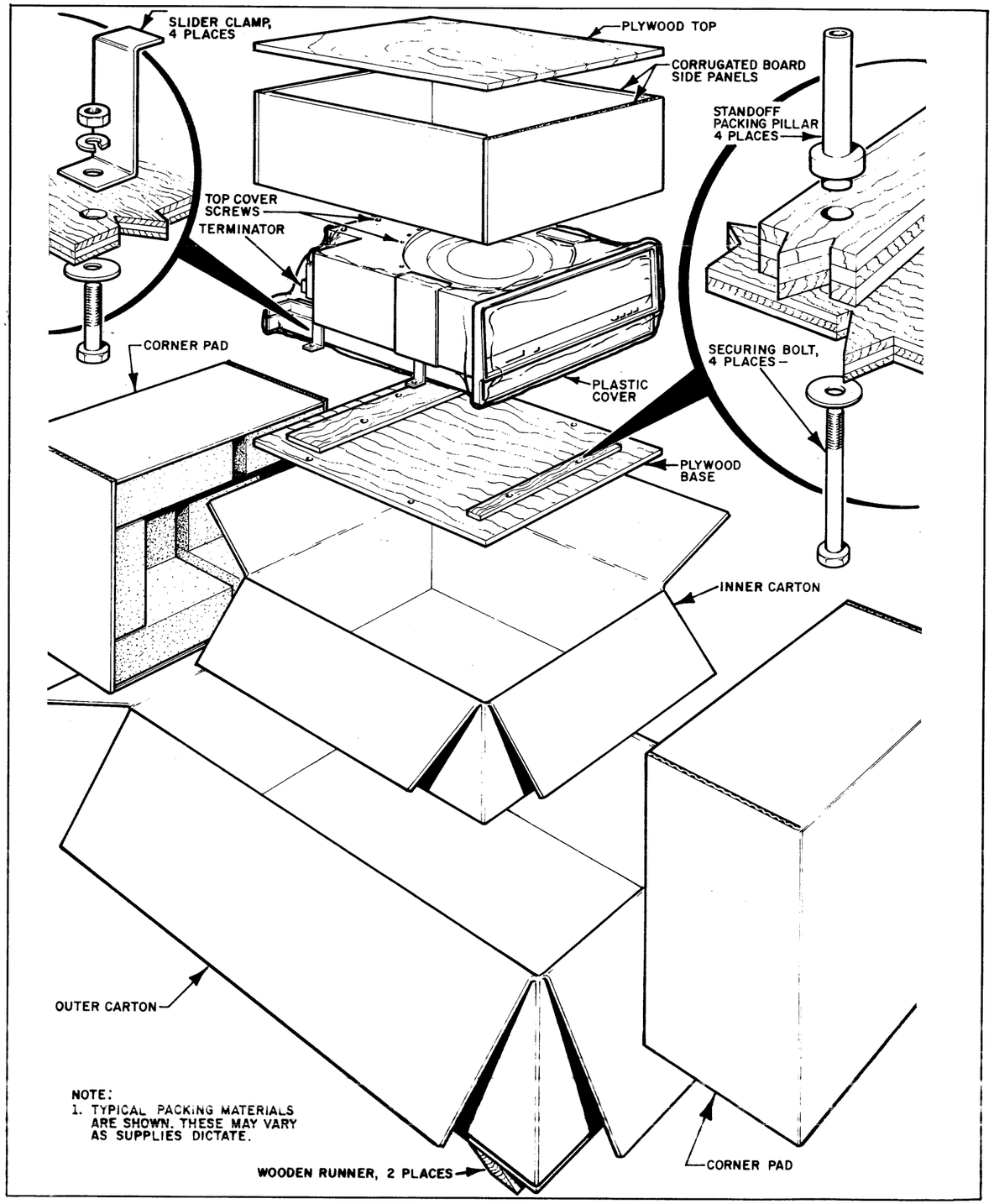


Figure 2-2. Series 40 Packing Shipment

2.3 PREPARING THE SERIES 40 FOR USE

The following four steps may be performed in any order to prepare the disk drive for installation and use.

Check Drawer Interlock Switch Actuator

Referring to Figure 2-3, lift the left hand drawer latch, as shown, and observe the position of the drawer interlock switch actuator arm. The solid line illustration shows the correct position for this arm. If the arm is out of position and wedged beside the stricker plate as shown, move it to its correct position.

Remove the Shipping Clamp

A shipping restraint is installed prior to shipment, to prevent movement of the head assemblies. This restraint must be removed prior to connecting the disk drive to its using system. Referring to Figure 2-2, remove the four screws holding the top rear cover, and remove the cover. Next, loosen the securing screw for the data channel box shown in Figure 2-4, and tip this box up to the right to expose the read/write head area.

Figure 2-5 shows the location of the shipping restraint clamp and its mounting screw. Remove both of these, and store for possible future use. Reposition the data channel box and tighten its securing screw, replace and screw down the top cover.

Installing Select and Attention Line Jumpers

Series 40 Disk Drives are shipped with the select line and attention line jumpers installed in the No. 1 position. If it is desired to change these jumpers, first remove the terminator if installed (see Figure 2-2). Next, remove the I/O Box cover (behind the terminator) by removing the two screws and washers,

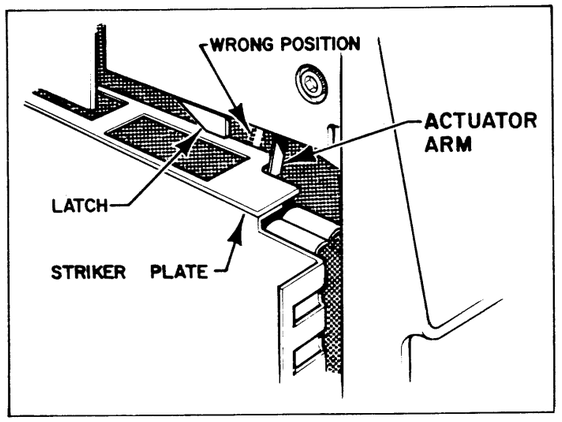


Figure 2-3. Drawer Interlock Switch Position

and gently prying the cover off. The Select And Attention Line Jumpers may now be seen as shown in Figure 2-6. They may be pulled out and replaced easily. Each jumper is to be installed with one of its pins in the center socket, and the other in the socket corresponding to the number assigned to the drive by the user.

NOTE

Both jumpers must be installed in corresponding positions. (1 & 1/2 & 2/ etc.)

When the jumpers have been properly installed, replace the cover and reconnect the terminator or I/O cable connector as required.

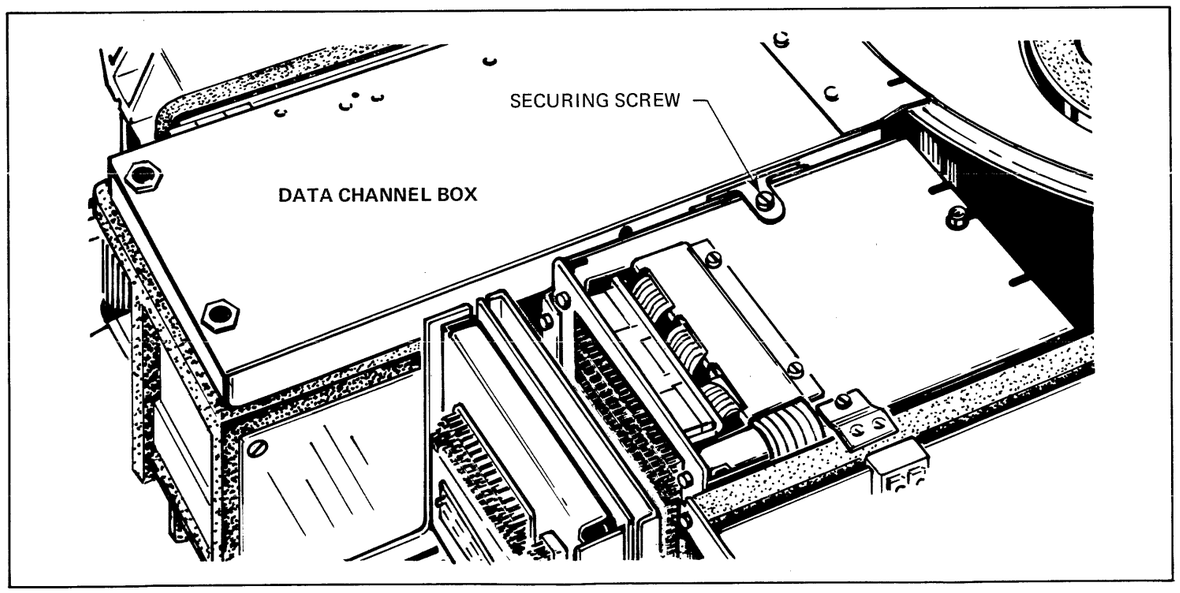


Figure 2-4. Data Channel Box

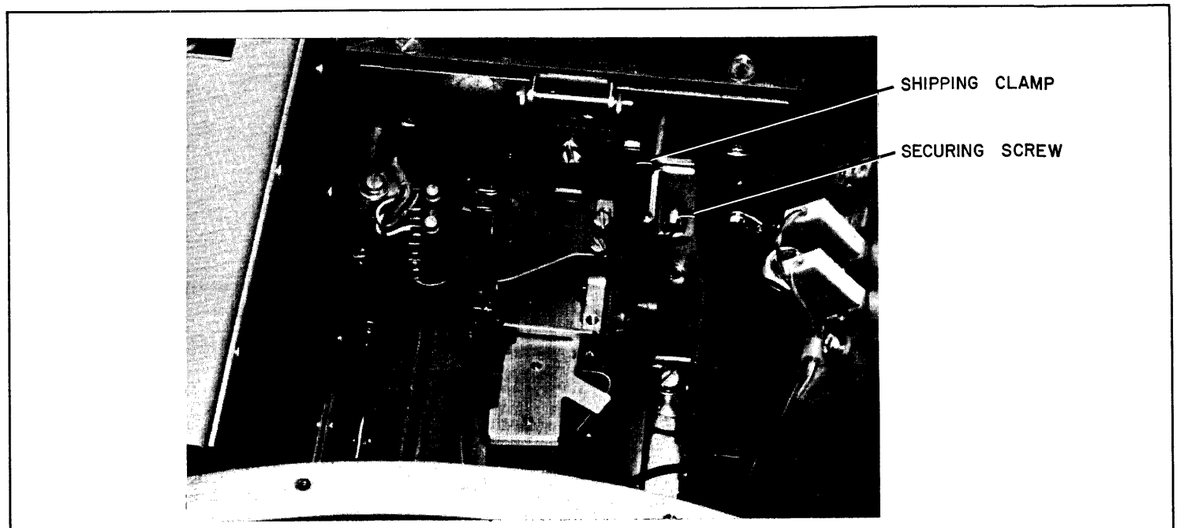


Figure 2-5. Shipping Clamp

2.4. INSTALLATION – RACK MOUNT

The Series 40 may be installed in a standard 19-inch rack with 27-1/2 to 28-5/8 inch rail spacings as follows:

1. Carefully examine the two side mounted rack slides, while referring to Figures 2-3 and 2-7. Locate the drawer latches. Raise the LH latch to release the slide, and extend the slide (with the I/O Assembly attached) to the rear until it stops. Locate the intermediate stop under the slide center, press it in, and continue to extend the slide to its maximum extension or maintenance position.

2. Referring to Figure 2-7, identify the several parts of the assembly, and note carefully how they fit together:
   - I/O Card Cage Assembly (LH only)
   - I/O Assembly Clamp Screws (LH only)
   - Nut Plates (front and rear on each side)
   - Mounting Brackets (2 each side)
   - Slide Assembly Mounting Screws

3. Fully extend the RH slide, remove the two slide assembly mounting screws, and remove the slide from the drive.

4. Fully extend the LH slide. Remove the four (4) I/O Assembly Clamp Screws, while holding the I/O Assembly in place.

5. Carefully move the I/O Assembly away from the extended slide, and gently push it back inside the drive into the area it normally occupies. Retrieve the two nut plates from beneath the top lip of the extended slide member.

6. Remove the LH slide's two mounting screws, and remove the slide from the drive.
7. Install the two slides in the rack per system definition. Adjust the rear mounting brackets as necessary to fit the rack rails. To prevent mounting slippage, use *at least* three (3) screws to attach each mounting bracket to its rail.
8. Position the unit on the fully extended slides.
9. Place the two nut plates in position under the top lip of the LH slide. Gently remove the I/O Assembly from the drive's rear compartment, move it into position on the LH slide, and install the four (4) clamp screws. Adjust assembly and nut plate locations as necessary for hole alignment.
10. Slide the unit fully into the rack, and check for proper operation of the drawer latches. Adjust the latch stricker plate (RH) and/or I/O Assembly (LH) as necessary for proper latch operation. Refer to Section 6.6.3.2.
11. Check shock absorber height adjustment for proper base-to-bottom pan clearance. Adjust the shock absorbers as required. See Figure 2-8.
12. Make necessary I/O Panel connections to complete installation. See Section 4.

CAUTION

The Series 40 Disk Drive weighs approximately 150 pounds. Make sure the rack, if free standing, has enough counter weight to prevent it from tipping forward when the unit is placed on the slides.

Adjust the slide locations as needed for hole alignment, and install the four (4) slide assembly mounting screws to secure the Series 40 to the slides.

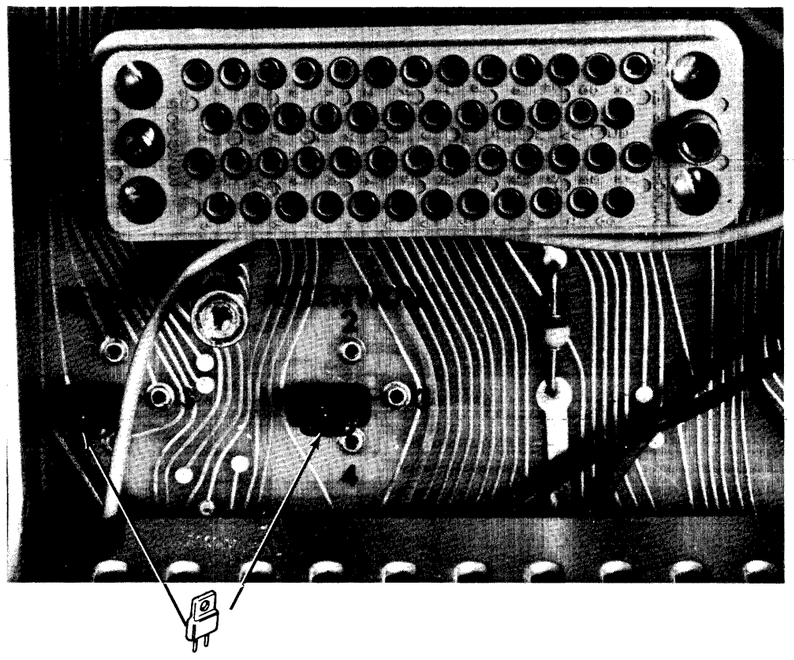


Figure 2-6. Select Line and Attention Line Jumpers

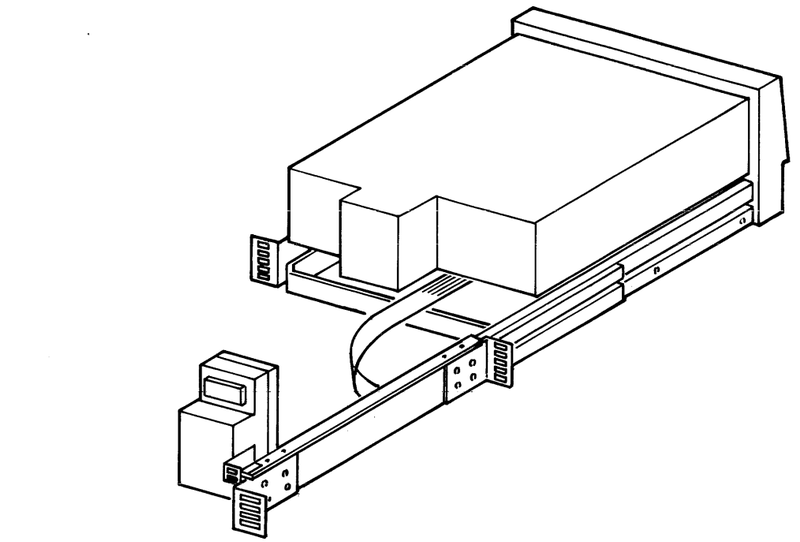


Figure 2-7. Assembly

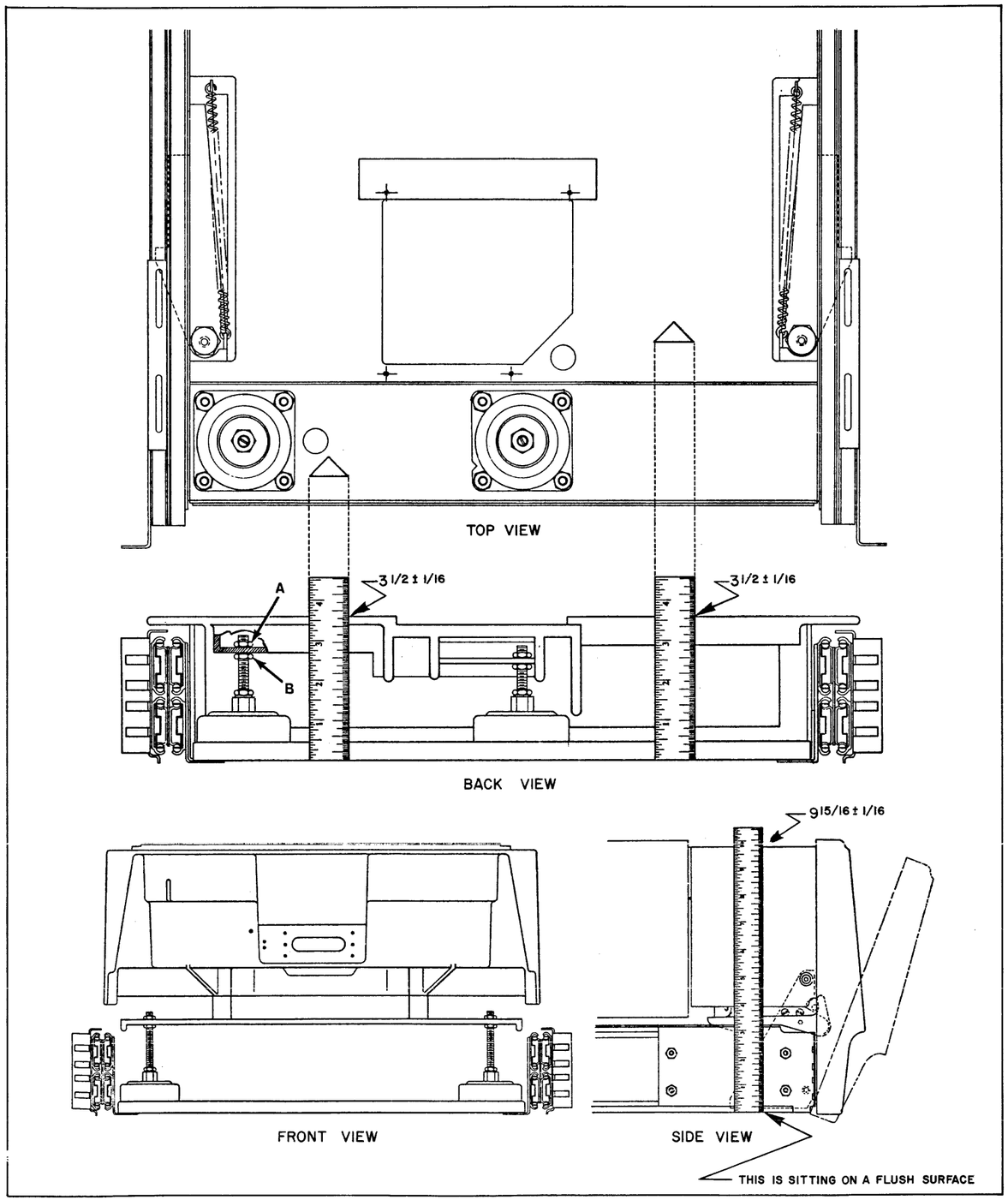


Figure 2-8. Shock Mount Adjustment

SECTION 3
OPERATING INSTRUCTIONS

3.1 OPERATING PRECAUTIONS

Disk Drive Operation

To obtain the best performance and reliability from the Series 40, and to prevent equipment damage, the following precautions should be observed:

- Do not connect or disconnect power or I/O cables while power is turned on.
- Keep the equipment drawer closed to prevent airborne contamination. Either a disk cartridge or the dust cover should be in place in the bowl at all times.
- The drive should be left in the RUN mode whenever possible so that clean filtered air will be supplied to the interior of the machine.
- A sustained audible "tinging" or "scratching" sound may be caused by head-to-disk contact. If it persists, discontinue machine operation and investigate the cause.
- Do not force or attempt to override any interlock. Interlocks are safety devices, included to prevent injury, equipment damage, and loss of data.

Cartridge Handling and Storage

The following precautions should be observed when handling or storing disk cartridges:

- Cartridges are magnetically recorded records. They MUST be kept away from strong magnetic fields, such as large rotating electrical machines, high current buss bars or cables, welding equipment, etc.
- The cartridge dust cover should be in good condition, and kept on the cartridge while it is out of the disk drive. This ensures a positive dust seal, and immobilizes the disk inside.
- Cartridges may be stored on edge or flat. When stored flat, avoid stacking more than five (5) high. Cartridges should never be stored in direct sunlight, or in very dusty or dirty areas.
- Any Disk Cartridge that has been dropped should be inspected by the disk cartridge manufacturer before attempting to use it.
- Refer to the cartridge manufacturer's instructions for maintenance and cleaning procedures.

3.2 CONTROLS AND INDICATORS

Standard Series 40 Disk Drives have one front-panel control and four front-panel indicators:

LOAD/RUN switch
LOAD indicator
READY indicator
CHECK indicator
POWER indicator

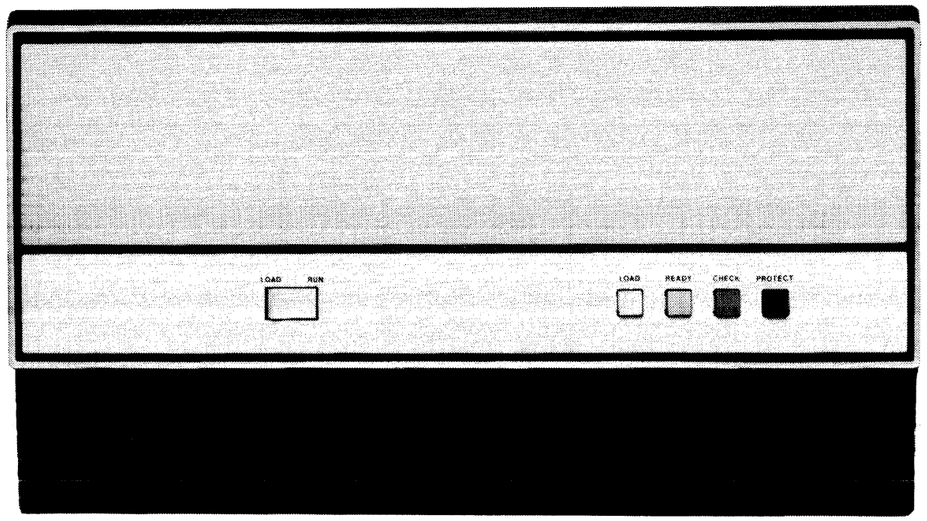


Figure 3-1. Front Panel, Series 40 Disk Drive

Table 3-1.
Controls and Indicators

CONTROL/INDICATOR	FUNCTION
LOAD/RUN Switch	A two position rocker switch that provides a means for starting and stopping the disk drive. Cartridges may be removed and inserted when the switch is in the LOAD position and the LOAD light is on. With a cartridge inserted, and the drawer closed, switching to the RUN position starts the disk drive and brings the disk up to its normal operating speed in about 60 seconds. When the switch is moved to the LOAD position, the disk decelerates to a stop in about 15 seconds, after which the LOAD light turns on, and the equipment drawer can be opened. NOTE: Does not control power to the drive.
LOAD	A white indicator light which shows that cartridges can be loaded or unloaded. The light is on only when the LOAD/RUN switch is in the LOAD position, the disk is not rotating, the brushes are retracted, and power is on.
READY	A yellow indicator light which shows that the drive has completed its start-up sequence. The light comes on when the disk is rotating at its correct speed, heads are in position and no other conditions are present which would prevent a seek, read, or write command from being executed. The light remains on through a seek, read, or write operation. The light extinguishes when the LOAD/RUN switch is set in the LOAD position.
CHECK	An orange indicator light which shows that due to some abnormal condition the Series 40 may be incapable of writing. When the abnormal condition no longer exists, the Series 40 is reset by moving the LOAD/RUN switch to LOAD position and then back to RUN.
POWER	A red indicator light that is on when operating power is present.
Optional Control/Indicator	
PROTECT (located in POWER light position)	A red backlighted momentary-contact pushbutton switch that is installed in place of the POWER indicator on those disk drives that are equipped with the Write Protect option. The switch glows and writing is inhibited whenever the LOAD/RUN switch is changed from RUN to LOAD, and this condition remains when the switch is returned to the RUN position. Write Protect is also set when the using system sends a Write Protect command. To allow writing, Write Protect is turned off by the operator depressing the PROTECT switch. The operator can set Write Protect at any time by moving the LOAD/RUN switch to LOAD and then back to RUN. Write Protect is also set when the drive is first turned on.

If the Write Protect option is installed, the POWER indicator is replaced by a lighted PROTECT switch.

The controls and indicators are shown in Figure 3-1, and depict a drive with the Write Protect option installed. Table 3-1 summarizes the functions of the controls and indicators.

3.3 INTERLOCKS

The disk drive equipment drawer is locked shut while equipment power is off, or while the spindle is rotating. The operator should never attempt to force the equipment drawer open, or to defeat any interlock. This practice could lead to equipment damage. The cartridge clamps cannot be operated while the heads or disk cleaning brushes are positioned over the disk surface, or when equipment power is off. The spindle motor will not rotate if the equipment drawer is open, if the cartridge dust cover is not installed, or if the cartridge clamps are open. With the desk-top interlock option installed, the cartridge clamps assume the same interlock function as the equipment drawer interlock does on a standard drive. This is in addition to their normal interlocking function.

3.4 TYPICAL OPERATING PROCEDURES

Initial Checkout

NOTE

The Series 40 must be removed from its plywood shipping base prior to initial checkout and alignment. If not installed in a rack or cabinet, place the unit on a stable flat surface.

Check for proper supply voltages prior to connecting the power cable to the Series 40 Disk Drive. Completely connect the drive to its power source before applying power. Set the drive's front panel LOAD/RUN switch to the LOAD position and apply power. For standard drives, verify that the POWER indicator is on. For drives with the Write-Protect option installed, the PROTECT light may or may not be on, depending on disk selection and system input. Verify that the front-panel LOAD indicator came on within 60 seconds after applying power.

- Open the equipment drawer by pulling out on the door handle as shown in Figure 3-2.

- Open the two cartridge clamps located on each side of the spindle bowl.

- Refer to Figure 3-3. Slide the tab on the cartridge handle to the left, raise the handle, and lift the cartridge clear of its "dust cover" lower half.

- Place the opened cartridge over the spindle hub oriented so that its handle would fold toward the rear. Lower the cartridge into place with a gentle back and forth rotary motion to ensure that its lower notches engage the alignment tabs inside the bowl. Lower the cartridge as far as it will go, then lower its handle to lock it in place.

- Place the cartridge "dust cover" upside down inside the drive's cartridge bowl on top of the cartridge just installed, and close the two cartridge clamps.

- Slide the drive back into its compartment until the latches engage the slides.

- Set the LOAD/RUN switch to RUN. Verify that the front panel LOAD light goes out.

- Allow the equipment about 60 seconds to complete its start-up cycle. Verify that the READY light comes on at the completion of this cycle.

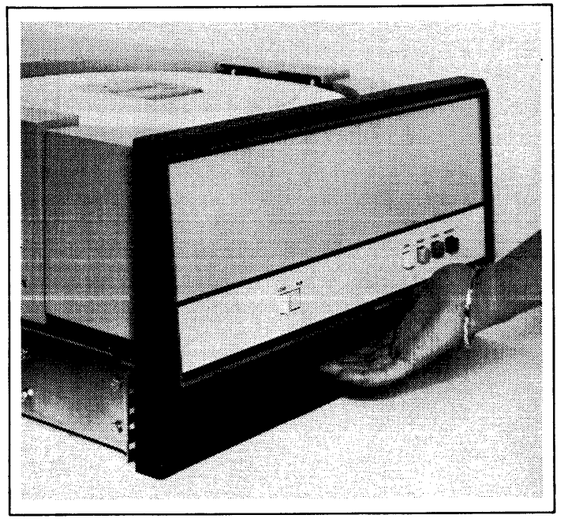


Figure 3-2. Opening the Equipment Drawer

NOTE

If the Write Protect option is installed, the PROTECT light will also be on, and must be depressed to extinguish the light before attempting to "write" on the disk.

Further checkout or operation as appropriate to the using system may now be performed.

NOTE

If data bases which require interchangeability are to be generated, align the R/W heads as described in Section 6 after installation of the disk drive.

When disk operation is complete, or when it is desired to exchange cartridges, the following steps are to be followed:

- Set the LOAD/RUN switch to LOAD. Wait for the LOAD light to come on (about 15 seconds).

- Open the equipment drawer (Figure 3-2), and slide the drive out to its first stop.

- Open the cartridge clamps and lift off the cartridge dust cover.

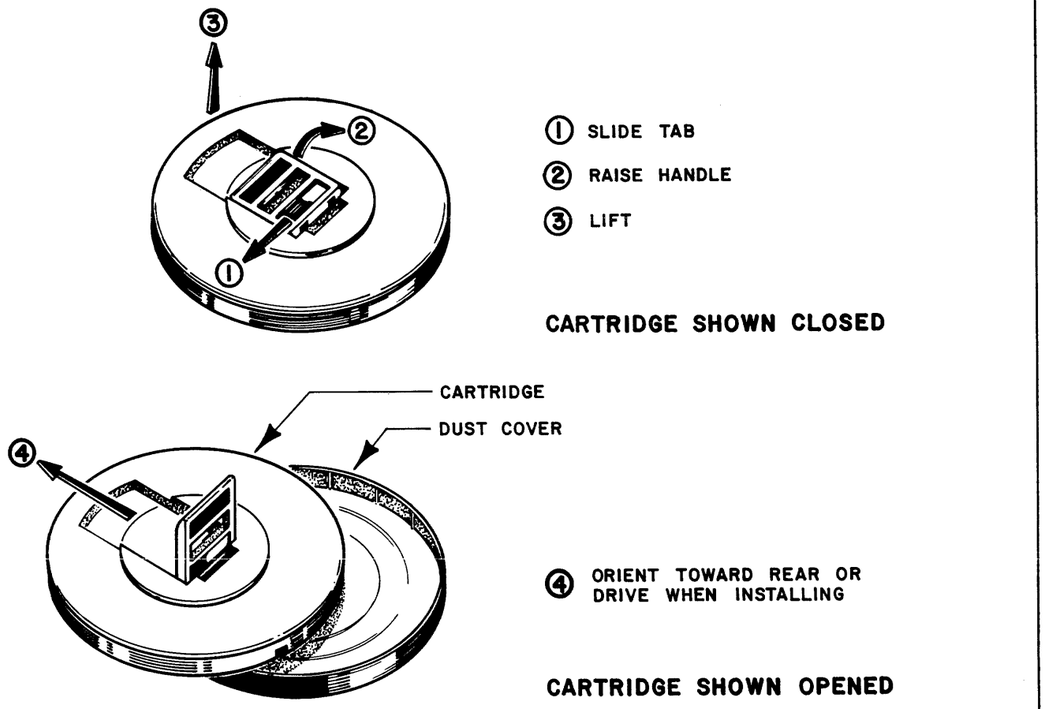


Figure 3-3. Opening the Type 5440 Disk Cartridge

- Slide the tab on the cartridge handle to the left, raise the handle to disengage the cartridge from the spindle, and lift the cartridge clear of the drive.

- Invert the dust cover, lower the cartridge into it, and fold the handle down all the way to engage the cover magnets and release the tab. The cartridge is now ready for storage.

- Install another cartridge and dust cover, close the equipment drawer, and place the drive in the RUN mode or completely deenergize the system.

NOTE

If no cartridge is to be installed at this time, cover the spindle bowl area with a plastic sheet or other lint-free cover.

SECTION 4
INTERFACE INFORMATION

4.1 POWER AND INTERFACE REQUIREMENTS

Series 40 Disk Drives require +24 Vdc ± 5% @ 6A average, −24 Vdc ± 5% @ 5A average, and +5 Vdc ± 5% @ 4A. These voltages are normally supplied by the Diablo Model 429 Power Supply furnished with each drive. The Series 40 does not include provision for power control. All power to the unit must be controlled by the using system.

If the user wishes to utilize a different power supply, several precautions must be observed. In the Series 40, ± 24 Vdc power is distributed separately to the high current drive and low current logic circuits. To avoid common impedance problems, separate leads must be used for these high and low level circuits. If the power cable must exceed 6 feet in length, a 30,000 uF 50 wVdc buffer capacitor should be used in each lead, and located within 2-1/2 feet of the disk drive. Conductors used for the power circuits should not be lighter than 16 AWG, and common flat braid 14 AWG should be used for the 24 volt circuit ground returns. A separate 16 AWG conductor should be used for the 5-volt return. These leads should be twisted together.

Power connector part numbers are given in Table 4-1, and power cable pin assignments are given in Table 4-2 below.

4.2 SIGNAL INTERFACE

Interface Connector

In addition to the power connector, each standard Series 40 Disk Drive has two interface connectors on its I/O box. The top connector is considered to be the *input* connector, receiving input information from a controller or from another disk drive preceding it in a "daisy chain" system. The bottom connector is considered to be the *output* connector, providing circuit connection facilities for a succeeding disk drive in a "daisy chain" system. If this is the last drive in a "daisy chain" system, or the only drive in the system, the bottom connector receives the required terminator. Table 4-3 shows the part numbers for the I/O and mating cable connectors.

Table 4-1.
Power Connector Part Numbers

Power Connectors	Power Cable Connectors
Shell: Winchester MRAC 14 PJ, Diablo #10524-11.	Shell: Winchester MRAC 14 SJTCH, Diablo #10524-10.
Pin Contacts: 100-0919P, Diablo #10525-10.	Socket Contacts: 100-0919S, Diablo #10525-11.

Table 4-2.
Power Connector Pin Assignments

Power Function	Pins
Ground (for 24V circuits)	R
−24 Vdc for Spindle Drive	A
−24 Vdc for Servo and R/W Circuits	L & H
+24 Vdc for Spindle Drive	C
+24 Vdc for Servo and R/W Circuits	N & K
+ 5 Vdc return	P
+ 5 Vdc	M

Interface Pin Assignment Summary

Interface connector pin assignments are summarized in Table 4-4, and are defined in the paragraphs immediately following.

Input Lines

The following input lines are found on the standard Series 40 configuration. Unless otherwise stated, the signals on control input lines must be held for the duration of the function controlled. Signals levels are 0 volts nominal for "true", and +3.5 volts nominal for "false".

- SELECT LINES – the interface has four lines assigned to the unit-select function, in order that the controller may select one particular drive in a system where more than one drive is used. As previously described, the line to be used is jumper selected inside the drive's I/O box. The selected line, when "true", qualifies all of the drive's other interface lines except ATTENTION. SELECT and ATTENTION jumpers must correspond.

- DISK SELECT – this line selects the disk to be used in a forthcoming operation. "True" selects the removeable cartridge disk, while "false" selects the fixed disk.

- HEAD SELECT -- this line selects the upper or lower head for use with the selected disk. "True" selects the upper head, while "false" selects the lower head.

- TRACK ADDRESS – these lines accept 8-bit (9-bit for 200 tpi) binary absolute cylinder addresses. When strobed, their content is supplied to an internal address register to control head movement. These lines must be settled prior to application of the strobe signal, and should be held until the trailing edge of the strobe signal.

- STROBE – this line is used to enable the track address and restore lines. Strobe should be applied only after the appropriate signal lines have settled, and must be held until at least the leading edge of the ADDRESS ACKNOWLEDGE signal. Rise and fall times are to be compatible with commercially available DTL and TTL integrated circuits. The strobe pulse is "true".

- RESTORE – this line carries the "head positioner restore to 0 command". When this command has been completed, the heads are located over cylinder 0, the address registers have been set to address 0, and the Seek Incomplete condition is reset. The RESTORE line must have settled to ± 10% of its steady value prior to the application of the strobe signal. The restore pulse is "true".

- WRITE GATE – signals on this line enable write current in the selected head, and, in conjunction with ERASE GATE,

Table 4-3.
I/O Connector Part Numbers

		Top I/O Connector		Bottom I/O Connector	
		Shell	Pins	Shell	Pins
I/O Box Connector	Diablo	10667-01	10583-01	10667-02	10583-02
	Winchester	MRAC 50 PJ6	1024P	MRAC 50 SJ6	1024S
I/O Cable Connector	Diablo	10670-02	10525-13	10670-01	10525-12
	Winchester	MRAC 50 SJTDH	100-0927S	MRAC 50 PJTDH	100-0917P

Table 4-4.
Interface Pin Assignments

Signal Function	Pin	Signal Function	Pin
−Select Unit 1	L	−File Ready	U
−Select Unit 2	R	−Ready to Seek, Read, Write	F
−Select Unit 3	V	−Address Acknowledge	p
−Select Unit 4	Z	−Logical Address Interlock	y
±Disk Select	AA	−Seek Incomplete	u
±Head Select	a	−Index Mark	Y
−Track Address Bit 1	N	−Write Check	h
Bit 2	s	−Read Clock	A
Bit 4	J	−Read Data	C
Bit 8	X	+Attention 1	CC
Bit 16	f	+Attention 2	DD
Bit 32	T	+Attention 3	EE
Bit 64	b	+Attention 4	FF
Bit 128	BB	Write protect status	P
@** Bit 256	m	+5 volts for terminator	r
−Restore	w	Ground	S
−Strobe	t	Ground	x
−Write Gate	e	Ground	HH
−Read Gate	E	−Sector Mark (see note)	W
−Write Data & Clock	B	−Sector Bit 1 (see note)	c
−Erase Gate	K	−Sector Bit 2 (see note)	j
−Write Protect Input	H	−Sector Bit 4 (see note)	k
Unused at this time	D	−Sector Bit 8 (see note)	n
Designated for future use	M	−Sector Bit 16 (see note)	v
*Unused at this time	z		
**−200 tpi line	z		
Unused at this time	d		

*100 tpi only
**200 tpi only
@Hold "false" on 100 tpi drives

NOTE: These lines are unused on disk drives without Sector Counter options.

disable the read gate circuits. The signal must be applied at least 2 μs prior to writing the first flux transition, and held for the duration of the write operation. The write gate is "true" for current on.

- ERASE GATE – this line, when "true", enables erase current to the selected head and, in conjunction with WRITE GATE, disables the read gate circuits.

- WRITE DATA & CLOCK – this line accepts multiplexed data and clock pulses for double frequency or phase encoding type recording, one complete pulse for each recorded flux reversal. Pulses must have a minimum width of 100 ns, and pulse leading edge must have a transition time of not more than 50 ns. This line is held at +3.5 volts when not writing. Pulses are negative going to 0 volts.

- READ GATE – when "true", this line enables the READ CLOCK and READ DATA output lines. The read gate must be held "true" during the desired read operation.

Output Lines

- FILE READY – this line supplies a maintained "true" level as long as *all* of the following conditions are met:
  a. Power on
  b. Cartridge loaded
  c. Equipment drawer closed
  d. LOAD/RUN switch in RUN position
  e. Start-up cycle complete
  f. WRITE CHECK false
  g. FILE SELECT true

- READY TO SEEK, READ, OR WRITE – (Ready to S/R/W) – a "true" level on this line indicates that the disk drive is in File Ready condition, and is not in the process of executing a seek operation. Following a seek "command" to a valid address (new address received other than present address), or a Restore command, the READY to S/W/R line goes "false" within 1 μs after leading edge of the Strobe signal. This line goes "true" when the seek (or restore) operation has been completed, the heads are fully settled, and the drive is ready to read, write, or seek to another address. This line does not change when the present cylinder address is re-addressed.

- ADDRESS ACKNOWLEDGE – a "true" level on this line indicates that a valid command to move the heads (seek command) had been accepted, and the heads have begun to move. An ADDRESS ACKNOWLEDGE signal (1 μs "true") is issued 500 ns after the leading edge of the Strobe, even if there is no change from the previous address. This signal will not be issued if a command to move to a track position greater than 203 (407 for 200 tpi drives) is received. In this case, execution of the command is suppressed, and a Logical Address Interlock signal is issued on another line.

- LOGICAL ADDRESS INTERLOCK – a "true" level on this line indicates that a track address (seek command) greater than 203 (407 for 200 tpi drives) has been received, and that the command can not be executed. The seek command is suppressed. Logical Address Interlock has the same timing relationships as the Address Acknowledge, and is reset with the next valid Address Acknowledge signal or Restore command.

- SEEK INCOMPLETE – a "true" level on this line indicates that a malfunction has caused an incomplete seek operation. This signal level is maintained until a Restore command has been received and executed by the drive.

- INDEX MARK – this line supplies one "true" 40 μs pulse (5 μs for drives with the Series 30 Compatibility Option) per disk revolution as the mechanical index slot on the disk hub of the selected disk passes its transducer.

- WRITE CHECK – a "true" on this line indicates that one or more of the following conditions exist:
  a. WRITE GATE "true" without write current
  b. Write current without WRITE GATE "true"
  c. Write and select of multiple heads
  d. Erase current without ERASE GATE "true"
  e. ERASE GATE "true" without erase current

  When WRITE CHECK is "true", execution of all external commands is suppressed, and the front panel CHECK light is on. The operator may reset Write Check by moving the LOAD/RUN switch to LOAD and then back to RUN.

  WRITE CHECK is also used to signal out-of-tolerance power supply conditions. In this event, reset is not required.

- READ CLOCK – this line carries clock pulses separated from data pulses during reading. Pulse width is 100 ns ± 50 ns. The leading negative-going edge must be used for reference. For drives with the Unseparated Data Option, there is no output on this line.

- READ DATA – this line carries data pulses which have been separated from clock pulses during reading. Pulse width is 100 ns ± 50 ns. The leading negative-going edge must be used for reference. For drives with the Unseparated Data Option, both clock and data pulses appear on this line.

- ATTENTION LINES – the interface connector has four lines assigned to the attention function, in order that the controller may be signaled by the selected unit in a system where more than one drive is used. Attention Line output is a logical combination of pulses used to inform the using system when the drive is ready, completes seek, fails to complete seek, accepts a seek command to the present address, or receives an invalid address. As with the Select Lines, the Attention line to be used is jumper selected inside the drive's I/O box. Also, SELECT and ATTENTION jumpers must correspond.

- 200 TPI LINE – this line, used only on 200 tpi drives, notifies the controller that the drive is a 200 tpi machine. Output is "false" until the drive is selected, and the heads are loaded.

Optional Input

- WRITE PROTECT – a "true" signal on this line, with a minimum duration of 350 ns sets the write protect circuit on drives with this option installed. Write Protect is also set whenever the LOAD/RUN switch is moved from LOAD to RUN. This option prevents inadvertent writing on the disk by disabling the write amplifier. Write Protect is selectable for either or both disks internally.

Optional Output

- WRITE PROTECT STATUS – this line provides a signal indicating write protect status, where a "true" indicates the drive's write capability is inhibited. The operator may release write protect by depressing the front panel PROTECT lighted push button switch to extinguish the light. Reset of write protect status requires either a controller supplied Write Protect signal, or an operator LOAD/RUN switch movement.

- SECTOR MARKS – this line supplies one "true" 40 μs (5 μs for Series 30 Drive compatible machines) pulse for each sector slot on the disk hub of the selected disk as it passes its transducer.

- SECTOR ADDRESS – these 5 lines continuously define, in binary form, the sector address under the heads. The counter in use is advanced by the leading edge of each sector mark, and is reset to 0 by the leading edge of the first sector mark following the index mark.

Output Line Drive Capability

An output driver circuit for the READ CLOCK and READ DATA lines is shown in Figure 4-1, for the standard configuration. All other lines are shown in Figure 4-2.

Figure 4-3 shows the READ CLOCK and READ DATA lines when the VFO option is installed.

Input Gates

The Series 40 Disk Drives use an 8836 type NOR gate as the input circuit. This device has a higher input threshold in the "low" logic state than most commercially available DTL or TTL circuits, assuring a higher noise margin on all input lines. Input hysteresis of the 8836 gates further increases noise immunity. Low input current, even with no Vcc, prevents a Series 40 with power down from affecting other drives in a daisy chain system. In addition the 8836 input circuit loads the signal transmission lines with significantly less input current under operating conditions, causing less local reflections on the line.

The input of the 8836 circuit has to be "pulled up" in the "high" logic state, and cannot be driven by an open collector driver stage without collector resistance. The Series 40 application has this resistance located in the terminator, which must be installed on the last disk drive in the daisy chain, or on any drive used singly. Figure 4-4 shows the input circuit used in the Series 40.

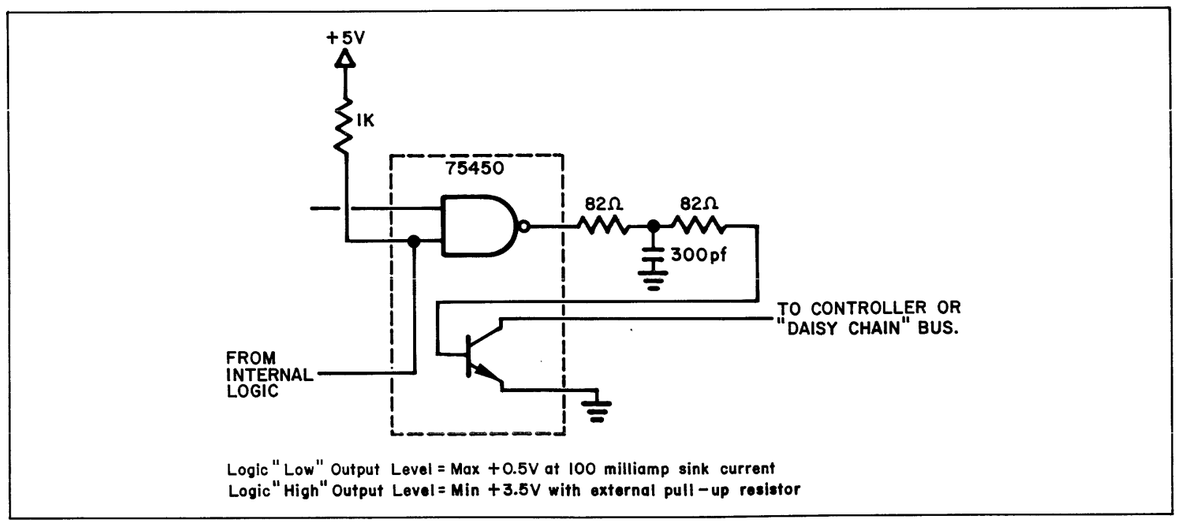


Figure 4-1. Output Driver – Read Clock and Read Data

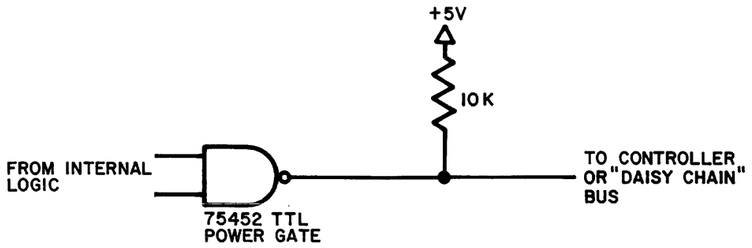


Figure 4-2. Output Driver Circuit

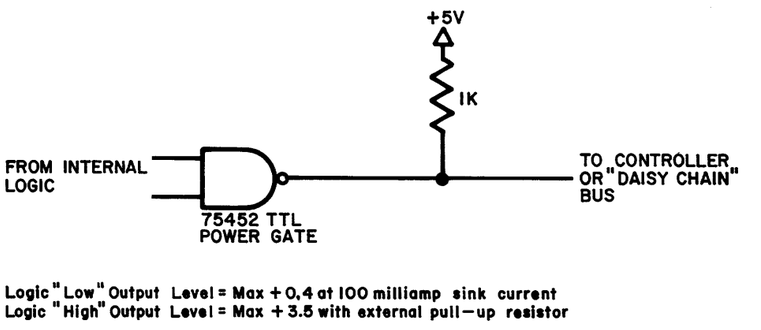


Figure 4-3. Output Driver Circuit

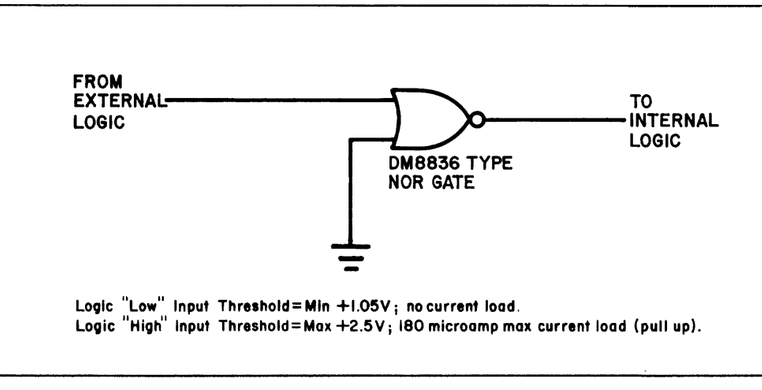


Figure 4-4. Standard Input Circuit

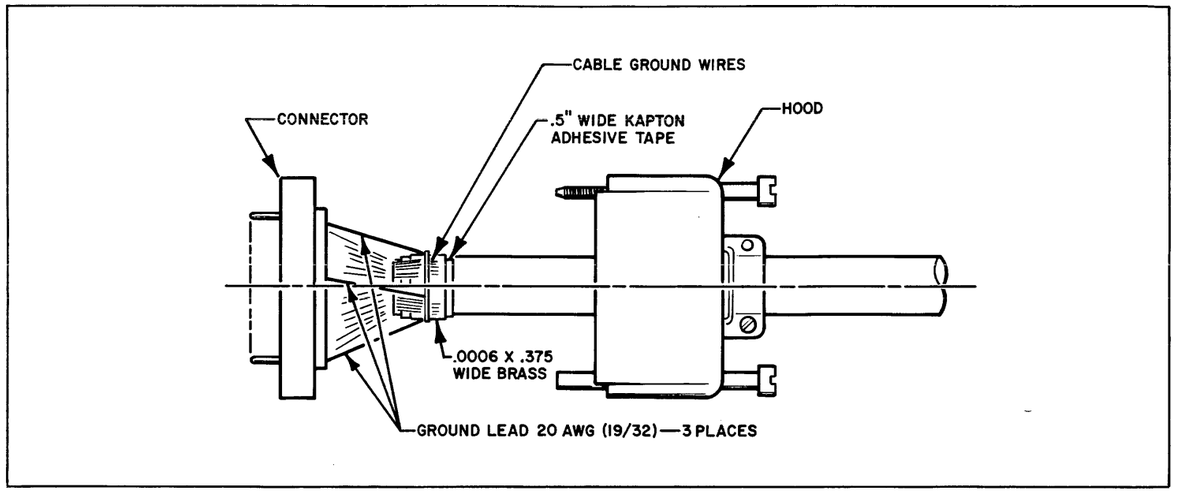


Figure 4-5. Interface Connector Assembly

4.3 INPUT/OUTPUT CABLES

Two types of cable may be considered for use with the Series 40. One type is the conventional round cable consisting of twisted pairs for each signal, with a PVC jacket. The other type is a PVC flat cable with a flexible ground plane.

Flat Cable

Because of the uniform transfer characteristics and production efficiency, a flat cable type is recommended. The flat cable, ordered by option number from Diablo, has the following physical characteristics:

Number of conductors	50
Wire size	30 AWG solid
Shield	Flexible ground plane
Insulation	PVC

The characteristic wave impedance is 80 Ohms, with the shield plane grounded on both ends.

Round Cable Twisted Pair

For those applications where, in spite of the drawbacks, a round cable is preferred, the type recommended is made of twisted pairs insulated with head sealed overlapping MILENE tapes. Physical characteristics of round cables are:

Number of twisted pairs	50
Wire size	28 (7/36) AWG
Nominal OD of insulated wire	.023"
Nominal OD of PVC jacket	.370"
Underwriters' Laboratory rating	Style #2384

The characteristic wave impedance of one single twisted pair is approximately 85 Ohms. If all ground leads of the twisted pairs are grounded on both ends, the wave impedance is reduced to 75 Ohms. If the twisted pairs are jacketed by an overall braided shield, the wave impedance drops to approximately 45 Ohms, which results in excessive current from the drive circuits. Individually shielded twisted pairs cable is not recommended.

Figure 4-5 shows one practical method of dressing the twisted pair wires at the cable end.

Cable Lengths

Maximum recommended cable length between the controller and the first drive is nine (9) feet. Cables between drives in a daisy chain system should not exceed six (6) feet in length. One nine (9) foot cable, between the second and third disk drive, would be permissable where the drives are located in separate cabinets. The total cable run in a daisy chain configuration should not exceed 30 feet.

4.4 TERMINATING RESISTORS

The signal lines carrying pulses transmitted by any disk drive will cause reflection on both ends of the cable if the cable is not properly terminated. Figure 4-6 shows two waveshapes taken on the terminated end of a cable when the other end was left unterminated. The negative going leading edge is not affected significantly, and can be used as an input to logic circuits if properly handled. The trailing edge, however, is determined by the time duration of the pulse, and the length of the cable. Those lines carrying signals of short duration should always be terminated on both ends. No satisfactory system performance can be achieved, even with relatively short cable lengths, if the signal lines are not properly terminated on both ends.

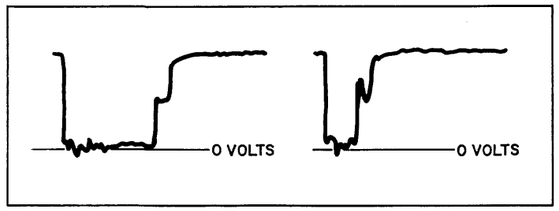


Figure 4-6. Waveshapes

A typical circuit for termination of the cables is shown in Figure 4-7. Cable terminators matched to Diablo supplied flat cable are available.

4.5 DOUBLE FREQUENCY RECORDING

In double frequency recording, a clock bit is recorded at the beginning of each "bit cell time". Recording a clock bit in each bit cell time results in the read back data being self-clocking.

To write a series of logical zeros, only the clock bit is recorded at the beginning of each bit cell time. To record a "one" bit, a flux reversal, or bit, is inserted in the center of a bit cell time. To write a series of ones, a clock bit and a data bit will be recorded in each bit cell time. It then can be seen the frequency of bits for a series of ones is twice the frequency for a series of zeros. Hence the method is called Double Frequency Recording.

Figure 4-8 shows the bit and time relationship for recording and reading back a data bit series of "0-0-0-1-0-1-1-1". Nominal pulse width for the system in 100 ns.

Multiplexed data and clock pulses are sent to the drive on one line; each pulse received on the line results in one current and flux reversal.

In standard Series 40 drives, the read signal's data and clock pulses are sent to the controller on separate interface lines. With the Unseparated Data Option, the combined data and clock pulses are forwarded to the controller on the READ DATA line only.

4.6 DISK FORMAT

Prior to consideration of the disk format information in this paragraph, the reader should become familiar with the basic functioning of the disk drive, as described in Section 5.

Details for the field shown in Figure 4-9 are as follows:

PREAMBLE 1 – all clock bits. Allows for differences in index transducers, alignment cartridge differences, synchronization of data separation circuits, and read amplifier recovery time. There is an overlap of these tolerances within system considerations.

SYNC 1 – a known bit pattern (typically $03_{(8)}$ or $03_{(16)}$), detected within the controller and used to allow gating following

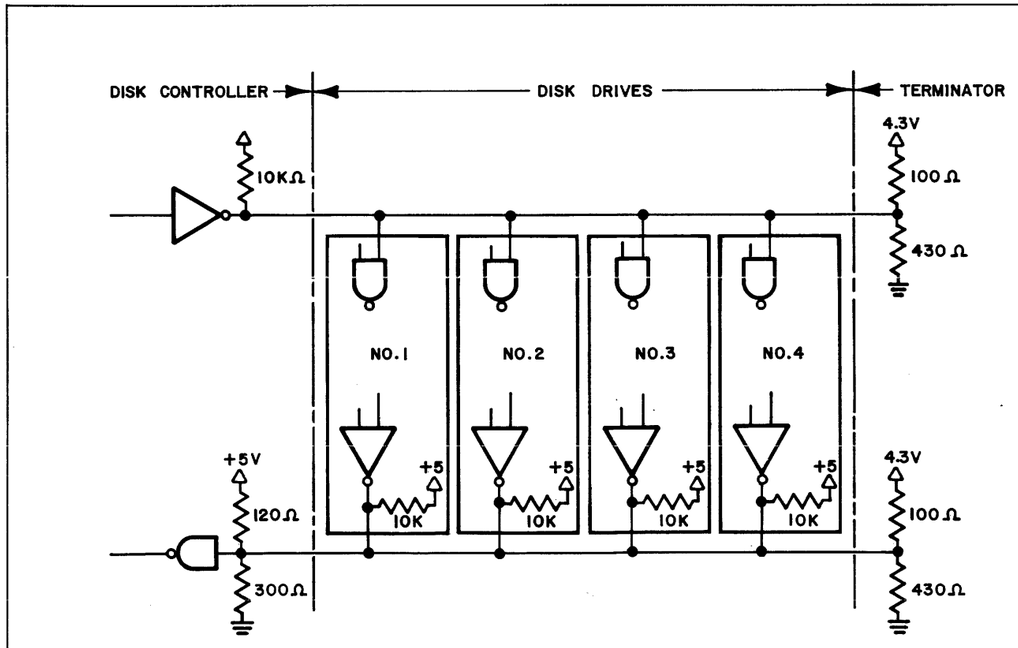


Figure 4-7. Daisy Chain and Terminator

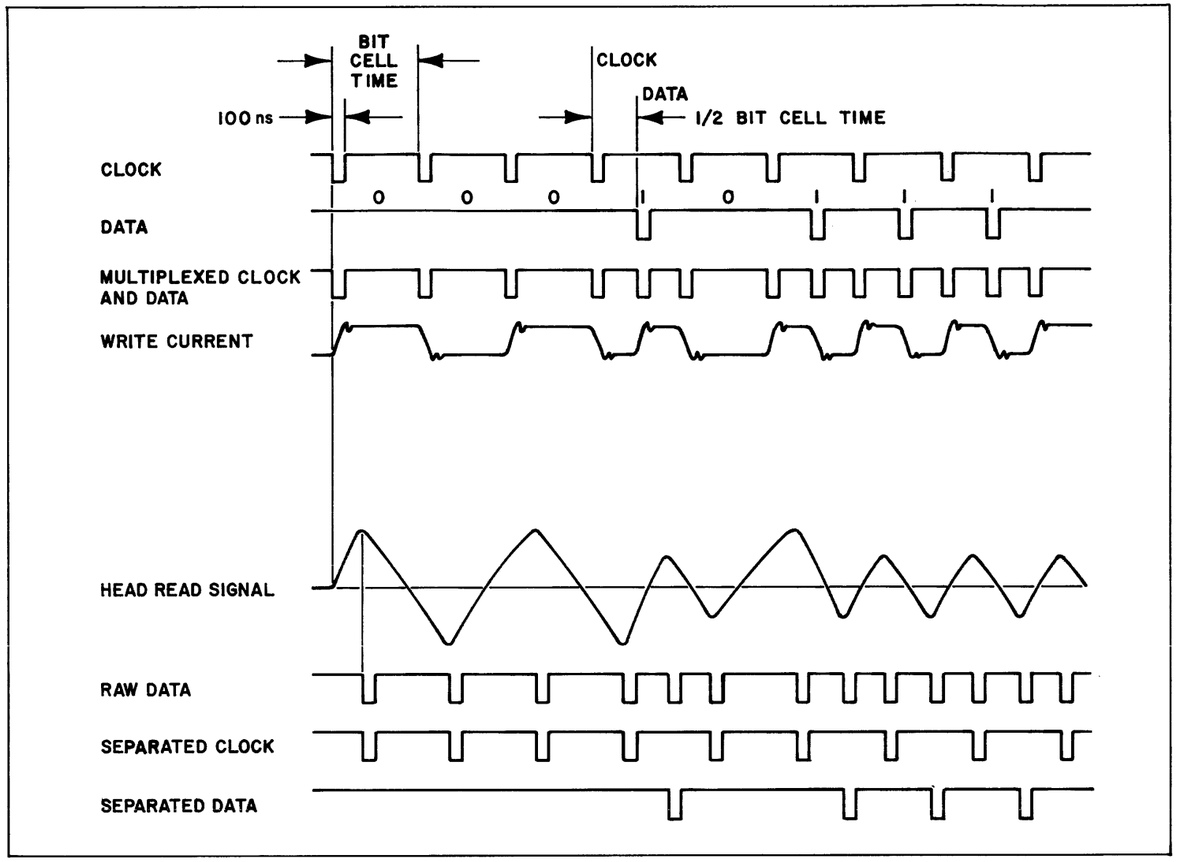


Figure 4-8. Double Frequency Recording

pulses into the using system. The amount of preamble read is variable, because of tolerance. The detection of the SYNC-1 field is required to signal the end of PREAMBLE-1.

HEADER – This field is typically recorded with the cylinder, head, and sector address located beneath the R/W heads. This field is generally compared with the address to which the heads were addressed by the controller to insure the seek operation was successfully completed. This field might also contain masking bits to indicate track surface condition.

CHECK SUM 1 – a check character developed within the controller during the write cycle and recorded on the disk. This check character is compared with the character developed within the controller during the read cycle to insure that the preceeding field was read accurately.

PREAMBLE 2 – all clock bits. This is an optional field that is used as a preamble to the data field. It is used in system applications when a virgin disk surface is initialized (to write all headers) only on the first pass. On subsequent data write operations the header field is not rewritten. When this gap is not used, the header and data field are rewritten during subsequent data write operations.

SYNC 2 – a field required to signal the end of PREAMBLE-2, and the beginning of meaningful data (typically $03_{(8)}$ or $03_{(16)}$).

DATA FIELD – the data recorded to be transferred.

CHECK SUM 2 – a check character developed within the controller during the write cycle and recorded on the disk. This check character is compared with the character developed within the controller during the read cycle to insure that the preceding field was read accurately.

POSTAMBLE – all clock bits recorded until the following sector mark is detected. The postamble allows for write/erase gap placement, disk rotation speed, and write clock frequency variations.

To summarize, typical write format, write data and read operations are described below. Table 4-6 and Figure 4-9 should be used as references with the following explanations.

1. Typical Write Format operation.
   a. Detect leading edge of sector mark "0".
   b. Enable Write/Erase Gate.
   c. Write Preamble 1 (zeros pattern).
   d. Write Sync 1, typically 03_{16} or 03_{8}.
   e. Write Header and Check Sum 1.
   f. Write Preamble 2, Zeros pattern.
   g. Write Sync 2, Data Field and Check Sum 2. Typically a zero's pattern or Header/Check Sum 1 information will be written in the Data Field during format operations. Sync 2 is typically 03_{16} or 03_{8}.
   h. Write Postamble, zero's pattern until the leading edge of the next sector mark is detected.
   i. During format operations Write/Erase Gate would not be disabled until the last sector of that particular track is formatted. Each sector would follow the same format, with only Header and Check Sum 1 information changing. This same track should be read on the next revolution to verify a proper formatting operation. Timing considerations would be identical to a Read Data operation.

2. Typical Write Data operation.
   a. Detect the leading edge of the desired sector mark.
   b. Wait for one-half of Preamble 1 and enable Read Gate.
   c. Read zero's preamble to synchronize data separator circuit.
   d. Read Sync 1 and Header/Check Sum 1 to verify that the correct sector has been found.
   e. Disable Read Gate after last bit of Check Sum 1.
   f. Wait one byte/word time, then enable Write/Erase Gate.
   g. Write Preamble 2, Zero's pattern.
   h. Write Sync 2.
   i. Write Data Field/Check Sum 2.
   j. Disable Write/Erase Gate at the leading edge of the next sector mark.

3. Typical Read operation.
   a. Detect the leading edge of the desired sector mark.
   b. Wait for one-half of Preamble 1 and enable Read Gate.
   c. Read zero's preamble to synchronize Data Separator circuit.
   d. Read Sync 1, Header/Check Sum 1 to verify that the correct sector has been found.
   e. Disable Read Gate after last bit of Check Sum 1.
   f. Wait for one-half of Preamble 2, then enable Read Gate.
   g. Read zero's preamble to sync Data Separator circuit.
   h. Read Sync 2, Data Field/Check Sum 2.
   i. Disable Read Gate.

Each track on the disk is divided into a number of sectors of equal length, as shown in Figure 4-9. This is accomplished by means of slots on the disk hub, or electronically in the using system. The time between index marks is equal to the time of one disk revolution. This is nominally 25ms (40ms for 1500 rpm units). The time duration of each sector is then the time between index marks divided by the number of sectors. If the disk rotation speed varies, the sector time varies by the same percentage. The spindle motor speed tolerance is ± 2% (± 1% for 1500 rpm units), and the sector time can therefore vary by this amount. Other manufacturing and adjustment tolerances also affect sector time.

Formatting of the disk is the organized placement of data zones and guard zones in each sector, the placement of clock pulses and/or data pulses within these zones. The data zones are those areas within each sector where data is to be recorded or read. To provide disk interchangeability and reliable read recovery of data, these data zones must contain a constant number of data cells, even in the presence of disk speed variation and other tolerances described below. The guard zones are variable in length, and ensure a constant number of data cells in each data zone by absorbing variations in sector time.

Each guard zone is a series of recorded clock pulses. The guard zone is recorded at the beginning and ending of each data zone, and is normally defined as a preamble (when at the beginning of the data zone) and as a postamble (when at the end of the data zone). The length of each guard zone must be adequate to allow for a reliable reading of each data zone even under worst-case conditions of tolerances. Each data zone typically contains synchronizing, header, data, and check information. A guard zone and a data zone are defined as a sector, and typically are recorded by a combination of hardware and software control. When sector slots on the disk hub are used, a sector mark format method is commonly employed. Sector mark formatting is explained in paragraph 4.6.1 below. When only the index slot is on the disk hub, it is common to use address mark format. The address mark is a unique recorded pattern on the disk which is detected by the R/W heads. It serves the same function as the sector slots. Address mark format is explained in paragraph 4.6.2.

4.6.1 Sector Mark Format

A typical sector mark format is shown in Figure 4-9 for an eight-sector disk. Typical field size for sector mark format is shown in Table 4-5 for the common numbers of sectors.

As previously explained, the preamble and postamble are required to absorb system tolerances, so that the data field will be constant. Factors contributing to the required allowance for system tolerances include physical separation of the erase and write coils, variation in the spacing of sector slots, alignment of the index transducers, sector jitter, alignment cartridge variance, disk rotational speed variations, write clock frequency, read amplifier recovery time, and variations in the transducers and their associated circuitry.

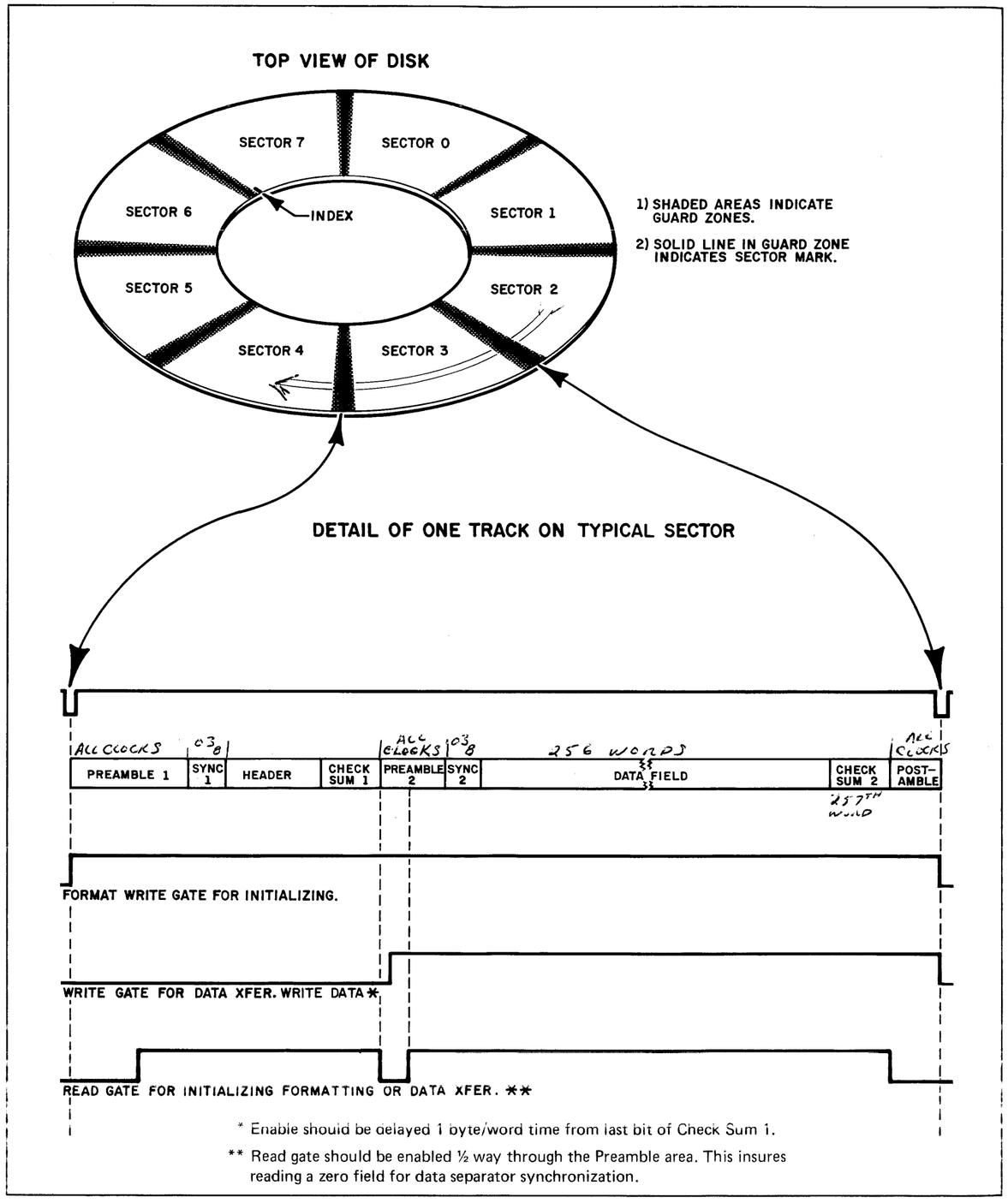


Figure 4-9. Typical Sector Format

Table 4-5.
Field Size

NUMBER OF SECTOR PER REVOLUTION	PREAMBLE 1	SYNC 1	HEADER	CHECK SUM 1	PREAMBLE 2	SYNC 2	DATA FIELD	CHECK SUM 2	POST AMBLE	
8	96.0µs	6.4µs	6.4	6.4	19.2	6.4	2902.53	6.4	VARIABLE FIELD APPROXIMATELY 75µs ALL CLOCK BITS TILL NEXT SECTOR MARK	2400 RPM
12							1860.86			
16							1340.03			
20							1027.53			
24	96.0	6.4	6.4	6.4	19.3	6.4	819.20	6.4		
8	153.6	10.24	10.24	10.24	30.72	10.24	4644.05	10.24	VARIABLE FIELD APPROXIMATELY 120µs ALL CLOCK BITS TILL NEXT SECTOR MARK	1500 RPM
12							2977.38			
16							2144.05			
20							1644.05			
24	153.6	10.24	10.24	10.24	30.72	10.24	1310.72	10.24		

Table 4-6 shows some nominal values of typical system tolerances. The format shown in Figure 4-9 using the time per field shown in Table 4-5 will allow for these variations with a reasonable margin for safety.

4.6.2 Address Mark Format Not used

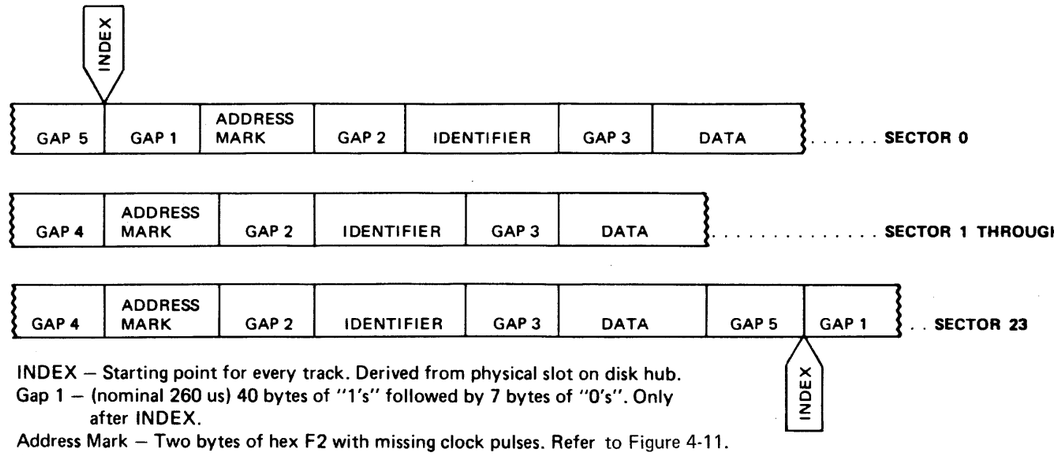
When the Address Mark Format is used, sector slots on the disk hub are not used. Instead, an address mark is recorded in each sector. The address mark serves the same purpose as the SECTOR MARKS described in 4.6.1. This format is characterized by missing clock pulses in the address mark word, and is used with a Series 40 having the Unseparated Data or VFO Options. In this case, the system tolerances affecting disk interchangeability, which are described in 4.6.1, are accounted for in the gaps. Figure 4-10 shows the address mark format.

The format is written while preparing or testing a new disk. Data recorded during subsequent write data operations is written only between gaps 3 and 4.

A write format command will always write the entire track and will always start at the index. Two bytes of "F2" with 2 clock bits missing are recorded for Address Marks. Refer to Figure 4-11. Cyclic code and bit count appendage characters are written at the end of an I.D. and Data Field. A read verify command, which checks the cyclic code and bit-count appendage characters, is used to check for write errors after the Write Format command.

Table 4-6.
Typical System Tolerances

Item	Maximum Sector Time Reduction in microseconds	
	2400 rpm	1500 rpm
Sector Slot Placement	29 µs	45 µs
Transducer Differences	12	18
Transducer Alignment	7	10
Alignment Cartridge Differences	3	5
Write/Erase Gap Placement	16	25
Disk Rotation Speed	63	50
Data Separator Circuit	6	6
Read Amp Recovery Time	25	25



INDEX – Starting point for every track. Derived from physical slot on disk hub.
Gap 1 – (nominal 260 us) 40 bytes of "1's" followed by 7 bytes of "0's". Only after INDEX.
Address Mark – Two bytes of hex F2 with missing clock pulses. Refer to Figure 4-11.
Gap 2 – Sync character – Hex OE. Nominal 5.12 us.
I.D. – Six bytes total. 1 flag byte, 2 address bytes, and 3 bytes of check characters.
Gap 3 – 10 bytes of all "1's", 4 bytes of "0's" and 1 byte Sync character Hex OE.
Data – 256 bytes of data and 3 bytes of check characters.
Gap 4 – 28 bytes of "1's" and 7 bytes of "0's".
Gap 5 – all "1's" until INDEX detected. Only recorded after Sector 23.

Identifier field explanation.

Flag Byte – Bits 0 - 5 not used
Track condition is indicated in bits 6 and 7.
0 0 = Good track
1 0 = Defective track
0 1 = Alternate track
1 1 = Defective alternate track

Address Bytes – Byte 1, Bits 0-7 contain the binary number of the cylinder (0 to 203)
Byte 2, Sector Address
Bit 0 is head number 0 = upper surface
1 = lower surface
Bits 1-5 are sector address
0 to 23 = upper surface
32 to 55 = lower surface
Bits 6-7 are not used should be "0's"

Check characters – Bytes 1 and 2 are Cyclic Check Character.
Byte 3 is Bit Count Appendage.

Figure 4-10. Address Mark Format

4.6.2.1 Data Write

A typical data write operation on a formatted disk would proceed as follows:

1. Seek to desired track.
2. Read for address mark.
3. Detect address mark and Sync Character.
4. Compare Identified field with desired address.
5. Six byte times after desired address had been located write four bytes of F.F., four bytes of 00 and sync character (O.E.).
6. Write Data field of 256 data bytes with cyclic check and bit count appendage.
7. Terminate write operation at end of bit count appendage.

4.6.2.2 Data Read

A typical data read operation on a formatted disk would proceed as follows:

1. Seek to desired track.
2. Read for address mark.
3. Detect address mark and Sync Character.
4. Compare Identifier field with desired address.
5. Detect Sync Character after desired Identifier, at end of gap 3.
6. Read data field of 256 data bytes with cyclic check and bit count appendage.
7. Terminate read operation at end of bit count appendage.

4.7 TYPICAL SIGNAL TIMING AT THE INTERFACE

Figure 4-12 shows the timing relationship at the interface for a typical write and read sequence using the single sector format described in 4.6.2. In the following description the terms "input" and "output" refer to input to, and output from, the disk drive.

Assuming that the disk drive is in the run mode, and that the start-up cycle is complete, a FILE SELECT true input at time t_0 establishes a file ready condition. The FILE READY output goes true when the disk drive is selected.

At this time the controller selects the upper head of the lower disk by making the HEAD SELECT and DISK SELECT input lines low and high, respectively. These lines could have been set up prior to time t_0, but have no internal effect until the FILE SELECT line goes true.

Since the disk drive is now ready and no seek is taking place, the READY TO S/R/W output goes true. The disk drive can now accept any valid command to seek, read, or write. At time t_1 the appropriate Track Address Lines corresponding to the desired track go low. These are shown collectively in the figure, rather than showing all nine track address inputs separately. When the Track Address Lines have settled, at time t_2, the STROBE input

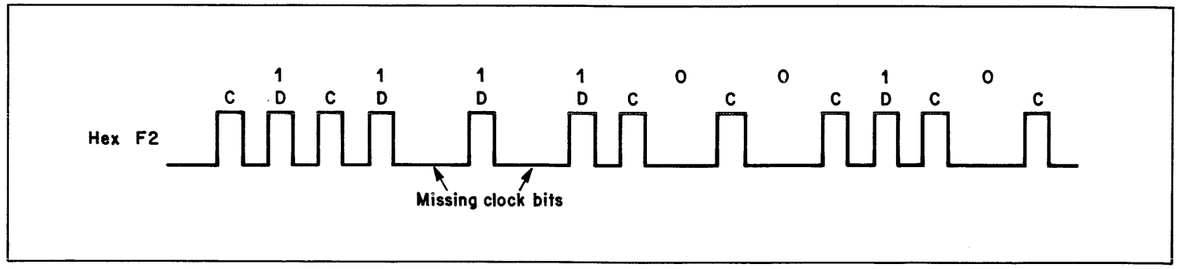


Figure 4-11. Address Marks

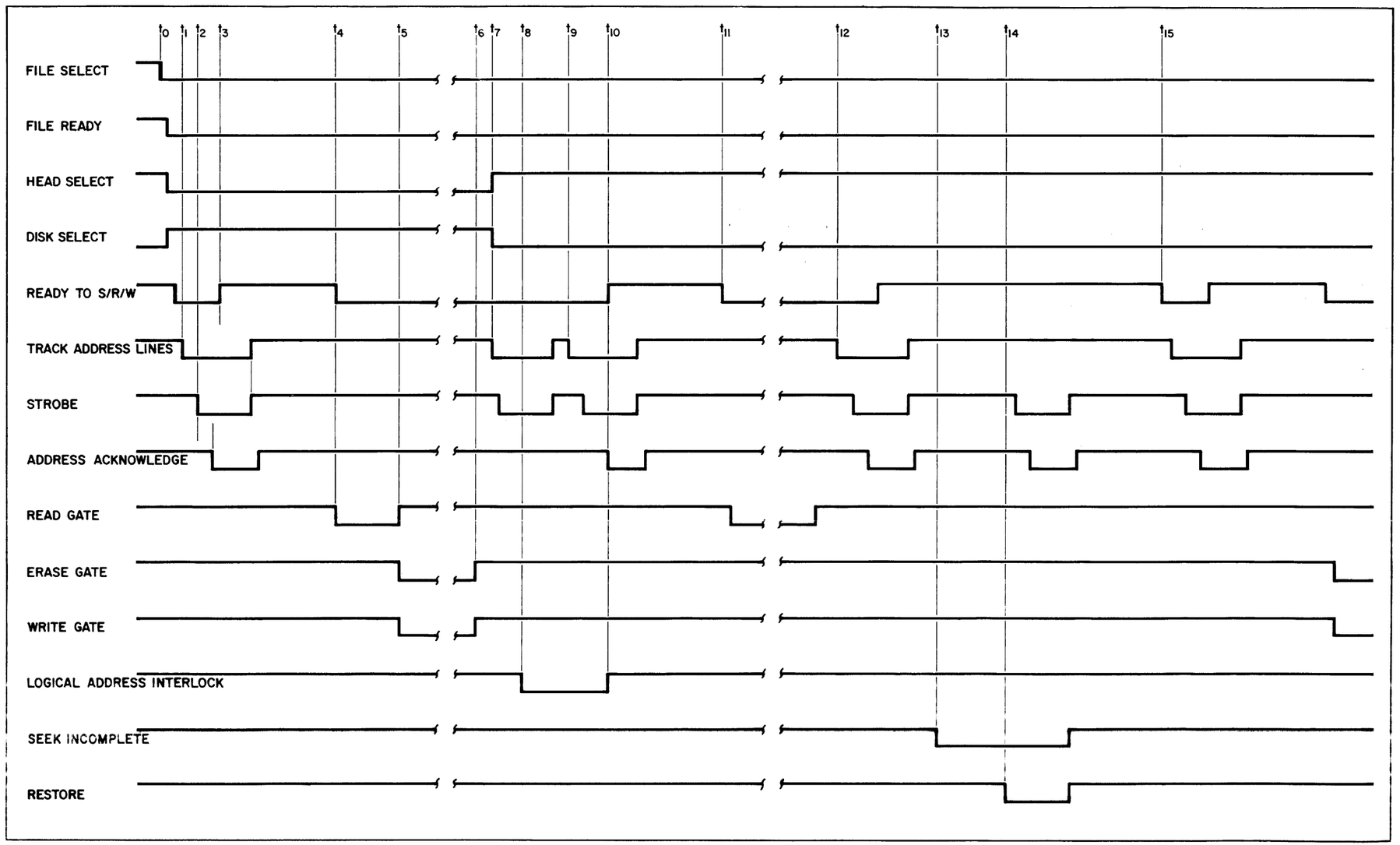


Figure 4-12. Typical System Timing

goes low. The appropriate Track Address Lines must remain low during the Strobe Pulse. About 500 nanoseconds after the leading edge of the Strobe Pulse, the ADDRESS ACKNOWLEDGE output goes true indicating that the command to move the heads to a specific cylinder address has been accepted, and that seek has commenced. Since a seek is in process, the READY TO S/R/W output goes false. This occurs at time t_3, which is within 1μs after the leading edge of the Strobe Pulse. At time t_4, the heads have settled at the desired cylinder address, and the disk drive is now ready to read, write, or seek to another address. This is indicated by the READY TO S/R/W output going true. In our example, the controller now makes the READ GATE input true, so that the address mark can be read prior to writing (see 4.6.2 item 2). The read gate could have been made true prior to time t_4, but the internal read circuitry of the disk drive will not accept a read command unless READY TO S/R/W is true.

When the desired address is reached, at time t_5, the controller sets READ GATE false, and WRITE GATE and ERASE GATE true. Multiplexed data and clock pulses are now furnished by the controller to the WRITE DATA AND CLOCK input. (Write data, read data, and clock pulses are not shown in Figure 4-12).

Writing continues until time t_6. Since the intervals between time t_5 and time t_6, and between time t_{11} and t_{12} are several hundred times larger than other intervals shown, they are not drawn to scale.

At time t_7 the controller selects a different disk and head, and codes a new address on the Track Address Lines. In our example, the controller has commanded an invalid address (greater than 203 for 100 tpi drives, or greater than 407 for 200 tpi drives), and the LOGICAL ADDRESS INTERLOCK output informs the controller of this fact by going true. The ADDRESS ACKNOWLEDGE output remains false. READY TO S/R/W remains true, indicating that the drive is ready to accept a valid address.

At time t_9 the controller codes a valid address onto the disk drive's TRACK ADDRESS LINES. Application of the STROBE starts the seek operation and at time t_{10} READY TO S/R/W goes false, ADDRESS ACKNOWLEDGE goes true, and the LOGICAL ADDRESS INTERLOCK is reset. When the heads have settled at time t_{11}, READY TO S/R/W goes true and a read operation is commenced.

After the read operation is completed a new seek is started at time t_{12}. In our example, some malfunction causes an incomplete seek, and the SEEK INCOMPLETE output goes true. The controller then places a low on the RESTORE input at time t_{14}. The subsequent STROBE input causes the heads to drive to track zero, where they are ready for another seek command at time t_{15}. Figure 4-12 shows another write operation at time t_{16}.

4.8 VFO SEPARATOR OPTION

The VFO option can be used either in the standard configuration (address mark format) or with the sector-mark option installed. In performing the data/clock separation function the VFO provides the following features:

1. Generates a clock signal that is synchronized to the read data.
2. Removes most of the jitter caused by pulse crowding and spindle speed variations.
3. Provides increased timing tolerances over the standard single-shot separator.
4. Provides missing clock bits for single-sector (Address Mark) format systems.

The VFO consists of a phase-locked loop and a data separator. The phase-locked loop provides a stable clock signal which is used to generate a data gate. The data pulse is aligned within this gate. In order to accommodate any synchronizing pattern, a High-gain Control circuit is included to increase loop gain. This circuit provides the high gain gate for 20μs after the start of VFO CLOCK. Phase lock and frequency correction of the phase-locked loop are accomplished during the high-gain gate. It should be emphasized that this phase locking and frequency correction 20μs after VFO clock starts applies only to the phase-locked loop. Subsequent to this, the single-sector data separator must be phased correctly, as later described.

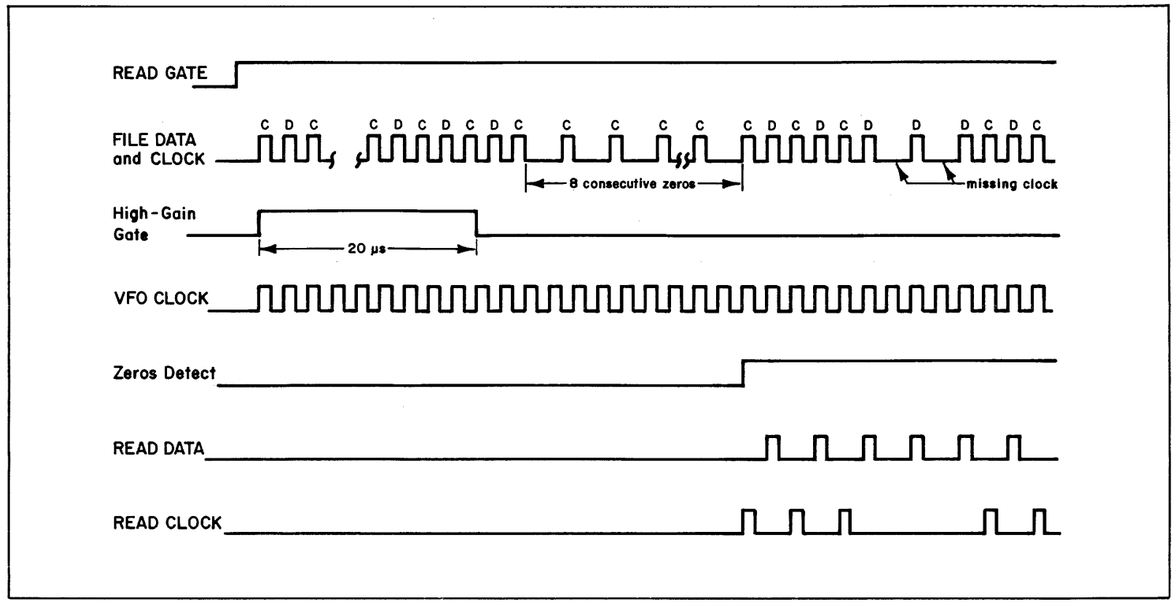


Figure 4-13. VFO Timing Chart

The VFO is turned on and synchronized with the file data by a start-lock control circuit. This insures phase lock within one bit cell time. The remaining lock-in time is used to correct frequency. Turn on of the VFO is controlled by the READ GATE. When READ GATE goes true, the start/lock control circuit turns on the VFO when the next file data bit occurs.

One of two different data separators is used with the VFO, depending on whether single-sector or sector-mark format is being used. Additional circuitry is required for the single-sector format due to the all-bit synchronizing pattern. With this type of synchronizing pattern the data separator may be phased incorrectly, since it cannot distinguish a data bit from a clock bit. The circuitry which corrects the phasing of the data separator is labeled Zeros Detector. This circuitry looks for any eight consecutive zeros. Once these zeros are found any place in the format (after the high-gain gate), the data separator is phased correctly and data is then gated out to the using system.

It should be noted that the VFO will not detect an Address Mark. The missing clocks will appear on the Interface, and it is the user's responsibility to detect the Address Marks. The VFO will guarantee good data on the Interface. Figure 4-13 shows typical timing. Output line drivers for the READ DATA and READ CLOCK lines are as shown in Figure 4-3.

SECTION 5
PRINCIPLES OF OPERATION

5.1 BASIC DISK DRIVE OPERATION

The circuits in the Series 40 Disk Drive can be divided into 6 functional groups. These groupings contain the circuits necessary to: rotate the disks at the proper speed; select the desired disk surface and head; position the heads over the proper disk cylinder address (location); write data; read data; and perform miscellaneous control and indication functions. Refer to Figure 5-1 for Block Diagram description.

5.1.1 Disk Rotation

The spindle assembly, with integral two-phase induction motor, rotates the disks at 2400 rpm (or optional 1500 rpm). One disk (lower) is permanently fixed to the spindle shaft, while the other disk (upper) is contained in a type 5440 removeable disk cartridge. The removeable disk is held to the spindle assembly during operation by a magnetic ring. Spindle speed is maintained within ± 2% by means of a crystal-controlled 2 mHz oscillator whose output is divided, shaped, and split into two 80 Hz (50 Hz for 1500 rpm) square waves, 90° out of phase with each other. These square waves are amplified and applied as driving power to the spindle motor. Since the spindle motor is very lightly loaded, it runs at its approximately synchronous speed of 2400 rpm (or 1500 rpm).

5.1.2 Surface (Head) Selection

Each disk surface has its corresponding read/write head. The surface-select logic receives DISK SELECT and HEAD SELECT signals from the controller which together enable the designated head.

5.1.3 Head Loading and Positioning

Head loading refers to the positioning of the read/write heads at the proper distance from the recording surface, as shown in Figure 5-2. In the Series 40, this distance is 2 microns (80 microinches). When loaded, the heads can then be moved to the proper address on the disk surface as explained in the following paragraph. The heads are loaded by a solenoid-operated mechanism, and are maintained there by spring pressure. Initial loading of the heads is controlled by start-up logic, and occurs when the disk reaches 90% of its normal rotational speed. The heads are unloaded if a power failure occurs, or if disk rotation drops below normal.

5.1.4 Cylinder and Track Addresses

The heads are mounted on arms, which in turn are mounted on a head carriage. The carriage moves the heads radially from the disk periphery toward its center. With the disk rotating and the head stationary, the position of the head describes a circular track on the disk surface, as shown in Figure 5-3. During a write operation, this track is magnetically recorded on the disk surface. The track consists of data signals and other signals which allow the accurate recording, retrieval, and identification of data as explained in Section 4 of this manual.

Similarly, the head can be positioned over a recorded track during a read operation. It can be seen from the representation in Figure 5-1 that there are four tracks, and that these tracks are in line vertically. The four circular tracks together describe a cylinder. If the head carriage moves in toward the center of the disks, a smaller cylinder is described by the four tracks. The position of the carriage, then, is referred to as the cylinder address. The combination of the cylinder address, disk select signal, and head select signal constitutes the track address. However, since the address logic in the Series 40 is used to position the head carriage, the term "address" is used in this manual to mean cylinder address.

Referring again to Figure 5-1, the head positioner servo system compares the latest address command with the current cylinder address, and supplies an error signal to the head carriage drive if these two addresses do not correspond. The polarity of this error signal controls direction of head movement. The magnitude of the error signal depends on the distance the head must move, and decreases as the proper address is approached.

The new address register receives the required address from the controller in a 8-bit binary form (9-bit for 200 tpi). When a new address is strobed into the address register, an address acknowledge pulse is issued. As a linear motor moves the head carriage, each cylinder centerline is detected by the head positioner transducer. An up/down counter in the head positioner servo system is adjusted with each of these centerline detections. As the up/down counter is adjusted, it changes instructions to the servo circuitry, so that the error signal to the drive varies, and the carriage will slow down as the correct address is approached.

If an invalid address is received from the controller, a logic address interlock is generated in place of an address acknowledge.

5.1.5 Writing

The layout of a read/write head is shown in Figure 5-4. The air holes provide the aerodynamic characteristics necessary for the heads to maintain their proper flying position when loaded. Each head assembly contains three separate precisely mounted coils; i.e., two erase coils and one read/write coil. The erase coils limit the physical width of the data tracks on the disk surface.

In a write operation, a single input line delivers multiplexed clock and data pulses; one complete pulse corresponding to each flux transition. The write circuits, activated by a write gate from the controller will allow current to pass through the write head and write one flux transition for each pulse. The erase coil, activated by an erase gate, will trim the written track to a nominal 0.0039" width (0.007" for 100 tpi drives). The read/

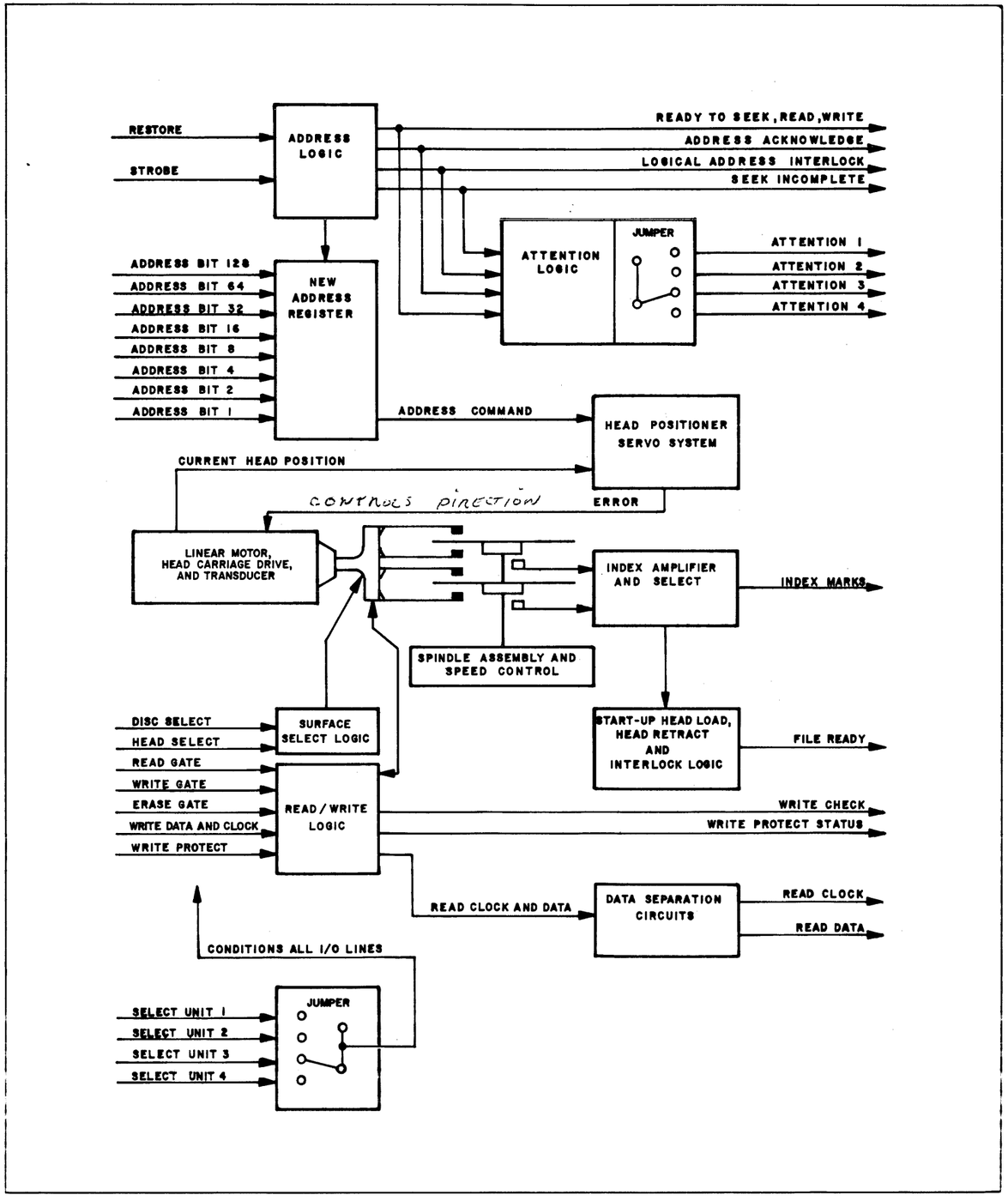


Figure 5-1. Simplified Block Diagram Series 40 Disk Drive

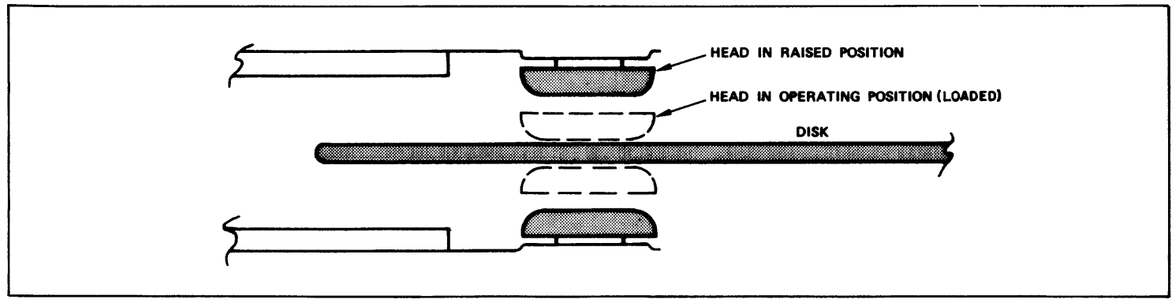


Figure 5-2. Head Positioning

write circuits perform the amplification and signal conditioning necessary for the translation between interface data signal voltages and head currents.

Certain conditions, if they occur, are likely to result in faulty or invalid data being recorded on the disk. These conditions are monitored and if they should occur, the write check interface line is made true and the CHECK indicator lamp is turned on. A write check condition will occur if the supplied voltage drops below the specified 5% or if certain write or erase current faults are present. A write or erase fault will be present, and the write check condition will be set, if write or erase current is flowing when the corresponding gate interface line is false, or if write or erase current is now flowing when the corresponding gate interface line is true. The other write check condition is a multiple head selection when the write or erase gate interface line is true. The write check condition caused by a voltage variation will last only for the duration of the faulty voltage. Any other write or erase fault will set an internal latch that is reset by the operator placing the LOAD/RUN switch in the LOAD position and then back to RUN.

5.1.6 Reading

The read circuitry is enabled by a read gate from the controller. The flux transitions on the disk surface induce head current pulses as they pass the head read/write coil. The read circuits amplify, shape, and separate these pulses into distinct clock and data pulse streams before delivering them to the interface lines.

5.1.7 Control and Indication Functions

5.1.7.1 Daisy Chain Operation

The daisy chain feature allows the controller to select a particular disk drive in a system where more than one drive is used. By means of a jumper on the I/O Box, a disk drive can be designated as Unit 1, 2, 3, or 4. Figure 5-1 shows the jumper installed on a drive designated as Unit No. 3. All interface lines except attention on a Series 40 Drive are inactive until a select signal is applied to the proper select line. The attention-line jumper must correspond with the select-line jumper.

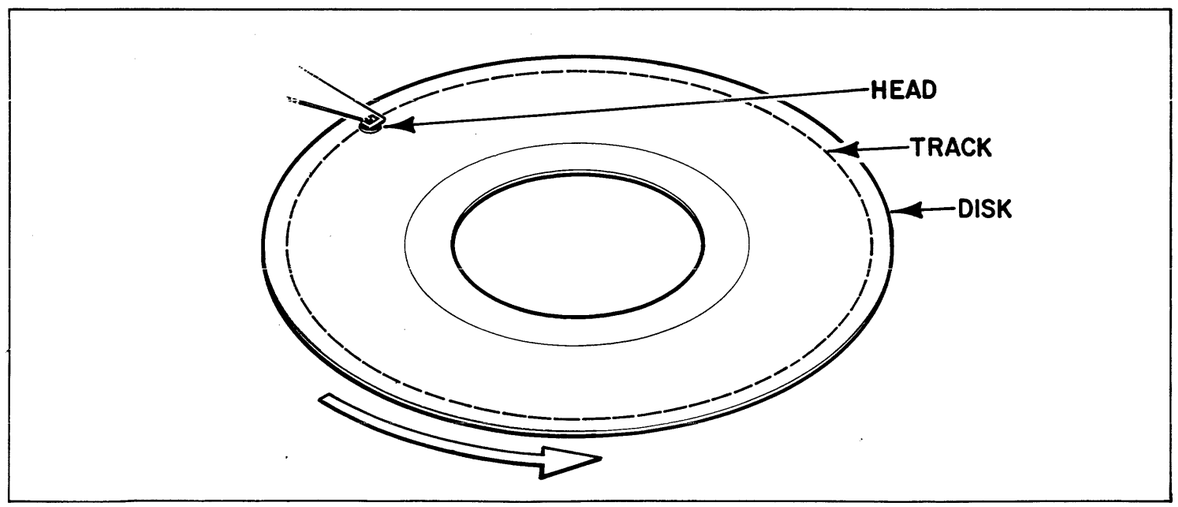


Figure 5-3. Track Layout

5.1.7.2 Start-Up Logic

The start-up logic performs two basic functions; it controls operation of the equipment, including the brush cycle and head load operation, during the start-up cycle, and it also controls the operation of various interlocks used to protect data and equipment. When the disk drive is placed in the RUN mode, power is applied to the spindle motor, starting disk rotation, and a brush is passed over each disk surface to remove any contamination. The hub of each disk contains an index slot, which is sensed by a stationary transducer as the slot passes the transducer. The index mark outputs of the transducers, therefore, occur once per disk revolution. The frequency of the lower disk index mark is used by the start-up logic to determine when the spindle is rotating at the proper speed, after which time the heads can be loaded. The index mark of the selected disk is also furnished to the controller interface.

The heads are retracted beyond the disk surface when power is initially applied or when the LOAD/RUN switch is in the LOAD position. The interlocks and safety devices controlled by the Start-up Logic minimize the possibility of accidental data loss, in routine operation or emergency shut-down. Interlocks are described in Paragraph 3.3.

5.1.7.3 Write Protect Option

The Write Protect Option is used to reduce the possibility of inadvertently writing over recorded information. The option consists of a backlighted momentary-contact front panel switch, an interface input command line, and an interface output status line.

The Write Protect Option functions in the following manner. The disk drive, during its start-up cycle, sets write protect on. Write and erase circuits are now inhibited, the PROTECT switch glows red, and the write protect status line is true. If writing is to be performed, the operator must depress the front panel PROTECT switch to extinguish its light. This switch depression also resets an internal flip-flop that enables the writing process and the write protect status line is made false, indicating to the interface that the recording surfaces are no longer protected.

Write protect status may be re-established at any time by a pulse on the write protect interface line. The write protect feature may be established or reset on the removable cartridge, the fixed disk, or all surfaces. This selection, by a provision on the Read/Write Amplifier PCB, is field changeable.

5.1.8 Sector Counter Option

In addition to the index slot described in 5.1.7.2, the 5440 disk cartridge is also available with equally spaced sector slots cut around the periphery of the disk hub. The more common numbers of sector slots available are 8, 12, 16, 20, or 24. The fixed disk has 24 sector slots in addition to the index slot. The sector slots are sensed by the index transducers, and the resulting

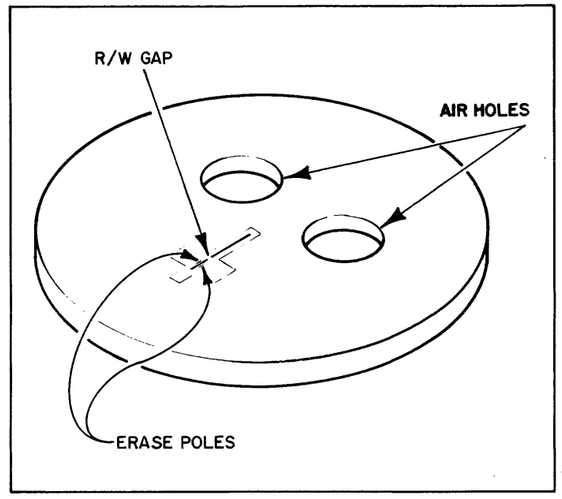


Figure 5-4. Head Configuration

sector marks are electronically separated from the index marks. With the Sector Counter Option installed, the sector marks from the selected disk are furnished to the controller interface and to a sector counter in the Series 40. The sector counter furnishes to the interface a 5-bit binary coded signal indicating which sector is currently passing under the R/W heads. The sector slots, therefore, divide each track into a number of equal segments for disk formatting purposes as described in 4.6. The sectors for an 8-sector disk are shown in Figure 5-5. For clarity, only one track is shown; its width is greatly exaggerated.

5.2 FUNCTIONAL DESCRIPTION

5.2.1 Location of Electronic Assemblies

Electronic circuit boards are contained in five areas in the Series 40 as follows:

1. Input/Output (I/O) Card Cage—this card cage accommodates six pluggable PCBs. Two circuit boards (RDR1 and RDR2) contain line drivers and line receivers, and are installed in all disk drives. A third slot holds either the Data/Clock Separator (D/CS) PCB in standard configuration disk drives, or the Variable Frequency Comparator (VFC) PCB if the VFO Option is installed. The remaining slots hold optional PCBs as follows:
   a. Sector Counter (SC)
   b. Variable Frequency Interface (VFI) or Variable Frequency Sector (VFS)
   c. Variable Frequency Oscillator (VFO)

   The I/O Card Cage also contains the I/O Mother Board, into which the PCBs listed above plug. The I/O Card Cage is attached to the rear of the left-hand slide assembly of the Series 40.

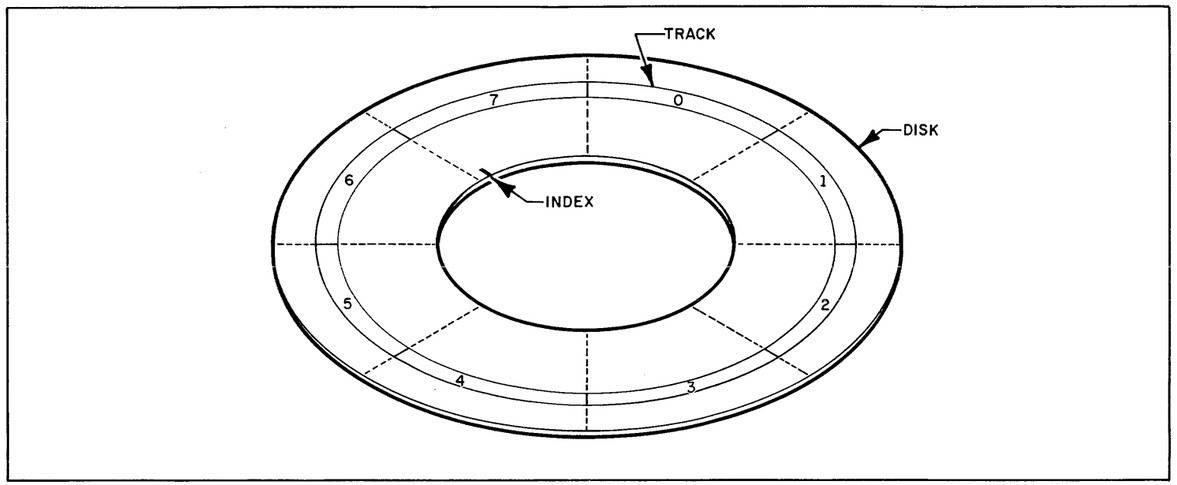


Figure 5-5. Disk Sector Layout

2. Main Electronics Card Cage—this card cage contains the following pluggable PCBs:
   M01 – Spindle Drive (SD)
   M02 – Oscillator (OR)
   M04 – Temperature Compensation (TC) (200 tpi drives only)
   M05 – Sequence Logic (SL)
   M06 – Sensor (SR)
   M07 – Servo (SO)
   M08 – Address Logic 2 (AL2)
   M09 – Address Logic 1 (AL1)

3. Read/Write (R/W) PCB—this circuit board is mounted in a sealed Data Channel Box above the head-positioner linear motor.

4. Head Sink Assembly—this assembly consists of the Heat Sink (HS) PCB, the power transistor heat sink, and the Servo Inhibit (SI) PCB. The Heat Sink Assembly is mounted on the left side of the Main Electronics Card Cage.

5. Panel Distributor PCB—this board is mounted on the rear of the front panel.

5.2.2 Start-up and Interlock Logic

5.2.2.1 Power-Off Condition

With no power applied to the Series 40, the drawer interlock solenoid, the disk-pack safety solenoid, and the head-load solenoid are deenergized. In the deenergized condition, the drawer interlock solenoid prevents the drawer from opening, and the disk-pack safety solenoid prevents the cartridge retaining clamps from opening and the head carriage from moving out of the fully retracted position. However, the cylinder location of the heads is undefined with power off since the head positioner requires power to hold the heads in position; previous maintenance operations may have left the heads extended. With the head-load solenoid deenergized, the heads are unloaded.

If power was turned off during a previous start-up cycle while the disk cleaning brushes were over the disk surface, they will remain in that position until power is reapplied.

5.2.2.2 Initial Power-On

When power is first applied to the Series 40, the following functions occur:

- voltage monitoring
- initial reset (conditions circuitry for initial operation of the disk drive)
- head and brushes retract
- drawer unlock

5.2.2.2.1 Voltage Monitoring

The external power supply supplies +24 Vdc, −24 Vdc, and +5 Vdc to the Series 40. Circuitry within the disk drive also requires +15 Vdc and −15 Vdc, which are obtained from the 24V supply lines by means of a 6030 IC regulator circuit on the Heat Sink PCB.

Some of the circuits in the Series 40 must be disabled whenever out-of-tolerance voltage exists. This occurs when power is first applied, but could also occur during operation if, for example, line voltage were to fall below certain limits. For this reason, the 24V, 15V, and 5V lines are monitored. The monitor circuitry also serves to initialize the Series 40 when power is first applied, in preparation for the receipt and proper execution of the first seek command. This is called initial reset.

Figure 5-6 shows a functional representation of the voltage monitor, which is located on the Sensor PCB. When power is first applied to the Series 40, the voltage monitor senses an out-of-tolerance condition, and causes transistors B14 and B17 to remain cut off. Capacitor A27 charges to 5 volts. When all three supplies are within tolerance, B14 and B17 conduct, A27 discharges, and the waveform shown in Figure 5-6 is produced. If any of the voltages supplied to the monitor drop out of tolerance, B14 and B17 cut off, and the collector of B14 again goes high and remains high during the out-of-tolerance condition.

5.2.2.2.2 Initial Reset

As shown in Figure 5-6, a positive signal is sent to the Initial Reset amplifier when power is first applied to the Series 40. A negative signal appears at the output, and is sent to the address logic circuits, the Sequence Logic PCB, and the Read/Write Amplifier PCB. It is also used to reset circuits on the Sensor and Sequence Logic PCBs. As previously stated, the purpose of the initial reset signal is to initialize the disk drive circuits in preparation for initial seek as explained later.

In the event that the voltage monitor detects an out-of-tolerance condition, another initial reset signal is generated and held until the voltage is back in tolerance.

On the Sensor PCB, the initial reset signal activates the spindle drive cutoff and servo hold, and resets the Servo Hold and Seek Incomplete F/F. It should be noted that this flip-flop is also reset by a RESTORE command. The purpose of spindle drive cut-off and servo hold is to ensure that the spindle motor and the linear motor are not driven during a period when voltage is out-of-tolerance. As shown in Figure 5-6, servo hold and seek incomplete are also activated if a high-current condition in the linear motor is sensed.

5.2.2.2.3 Head and Brushes Retract

The initial reset signal is taken to the AL-1 PCB where it causes a "retract speed" signal and a "reverse direction" signal to be generated and sent to the AL-2 PCB. On AL-2, the "retract speed" signal disables all linear motor speeds except minimum and the "reverse direction" signal causes the linear motor to move in the retract direction. When the heads are fully retracted, a micro-switch on the Head Positioner Assembly removes the drive to the linear motor.

Switches located near the disk cleaning brushes pivot-point are connected to toggle brush cycle flip-flops on the Sequence Logic PCB to indicate whether the brushes are retracted or are extended. One output of these flip-flops is furnished to a NAND gate, together with an internally generated 60 Hz square wave which is present whenever power is applied to the Series 40. The output of the NAND gate is amplified and drives the brush motor. If the brushes are not fully retracted when power is first applied to the disk drive, the output of the flip-flop will furnish a high to the NAND gate, whose output will then be a 60 Hz square wave, driving the brush motor. When the brushes reach the full retract position, the brush switches toggle the flip-flop, and the brush motor stops.

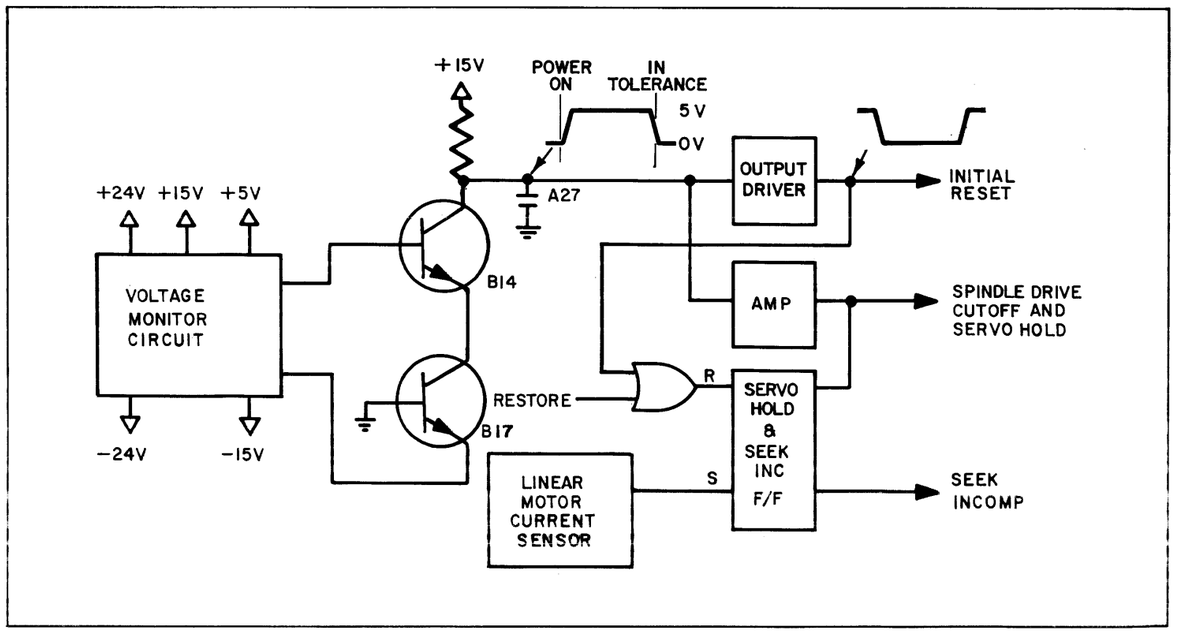


Figure 5-6. Voltage Monitoring and Initial Reset

5.2.2.2.4 Drawer Unlock

Retract switches located just in front of the linear motor are connected to toggle a flip-flop on the Sequence Logic PCB to indicate when the heads are fully retracted. The output of this flip-flop is furnished to a NAND gate, whose other input comes from one of the brush cycle flip-flops previously mentioned. The output of the NAND gate energizes the drawer unlock solenoid which, through mechanical linkage, lifts the drawer latches. It should be remembered that the preceding discussion refers only to the initial power-on stage; it will be seen later that other conditions are necessary to energize the drawer unlock solenoid when the disk drive is already in operation.

5.2.2.3 Cartridge Loading

With the drawer open, a cartridge can now be loaded. There is a disk-pack interlock switch which is open whenever a cartridge and its top cover are installed in the bowl. This switch prevents loading of the heads when no cartridge is installed and also prevents movement of the brushes out of the fully retracted position.

NOTE

It does not prevent movement of the brushes into the fully retracted position.

5.2.2.4 Start-up Sequence

There is a drawer interlock switch which is closed whenever the equipment drawer is not fully shut. This switch is wired in parallel with the disk-pack interlock switch. Therefore, the drawer must be closed and the cartridge and dust cover must be in place before the brush motor, spindle drive, and head loading can be activated.

Figure 5-7 is a simplified functional block diagram showing the start-up sequence from setting of the LOAD/RUN switch to the RUN position until generation of the FILE READY signal, at which time the drive can accept its first seek command. The following description is based on the assumption that the brushes and heads are fully retracted, that a disk cartridge and cover are installed, that the drawer is closed, that initial reset has occurred, and that the LOAD/RUN switch is in the LOAD position.

The sequence of events can be summarized as follows:

1. Set LOAD/RUN switch to RUN.
2. Spindle drive motor energized; heads move to Track Zero; drawer locks; brush cycle starts.
3. Spindle reaches 50% of rated speed; full current applied to spindle drive motor.
4. Spindle reaches 86% of rated speed; head load enable F/F sets.
5. Brush cycle completes, heads load.
6. FILE READY signal is generated.

The remainder of this subparagraph describes how the foregoing six events occur.

Referring to Figure 5-7, the following conditions exist:

- Completion of the previous brush cycle has reset Brush Cycle I F/F and Brush Cycle II F/F.
- The heads-retracted switches have reset the Heads-Retracted F/F. The output is 'NANDed' at "G" with the output of the Brush Cycle I F/F to provide a –UNLOCK DRAWER signal to the Sensor PCB. It is there ANDed with several other interlock functions, to be described later, and energizes the drawer unlock solenoid. The low –DRAWER UNLOCK signal is also applied to a three-input NAND gate at "A", disabling the gate.
- Initial reset has set the Load/Run F/F and reset the Spindle Drive F/F, as well as conditioned the Up-to-Speed F/F and the integrator circuitry.
- The disk-pack interlock switch and the drawer interlock switch, together with the Heads Retracted F/F, have conditioned a three-input AND function at "A".

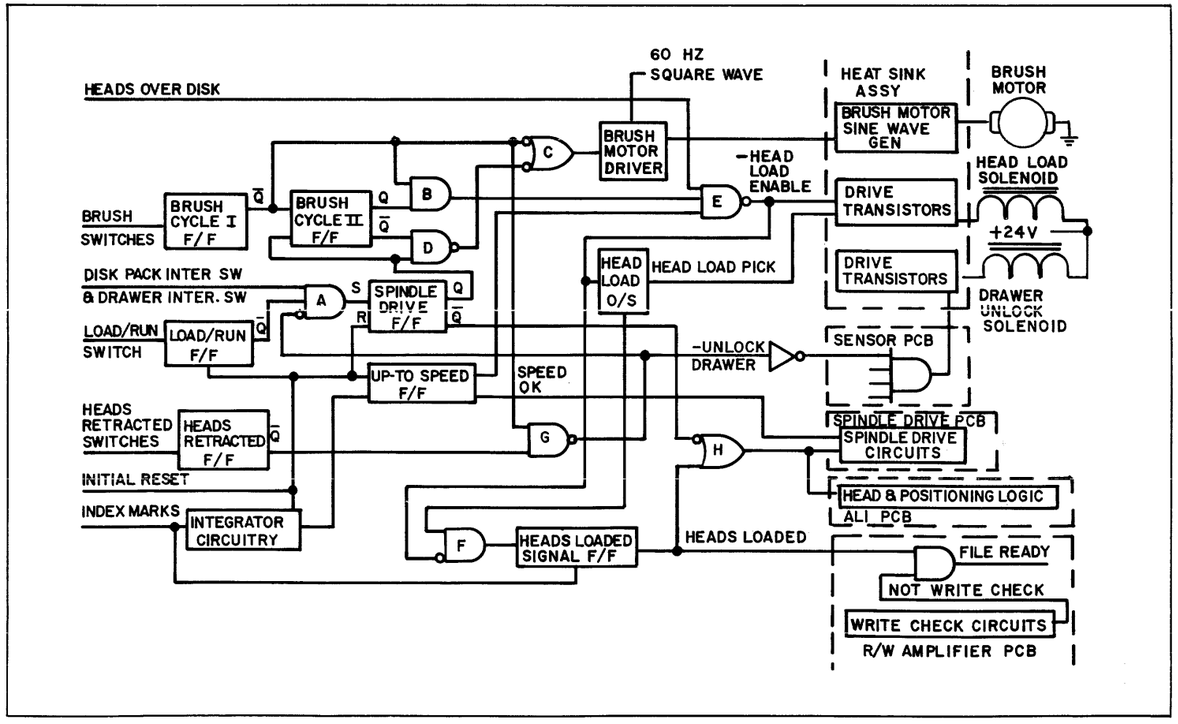


Figure 5-7. Start-Up and Interlock Logic

When the LOAD/RUN switch is set to RUN, the Load/Run F/F is reset, which provides a third high to the AND function at "A". The Spindle Drive F/F is set. Its Q output is NANDed at "D" with the $\overline{Q}$ output of the Brush Cycle II F/F. The low output at "D" is gated through "C" and then gates the brush motor drive circuit. The other input to the brush motor drive circuit is a 60 Hz square wave generated by dividing the output of a crystal oscillator on the Oscillator PCB. The output of the brush motor drive circuit is two 60 Hz square waves 180° out of phase with each other. They are fed to a sine-wave generator on the Heat Sink Assembly. The 60 Hz sine-wave output of the generator drives the brush motor, and the brushes start their cleaning cycle over the disks.

When the Spindle Drive F/F was set by the action of the LOAD/RUN switch, its $\overline{Q}$ output was NANDed at "H" to provide the +SPINDLE DRIVE ON signal. This is fed to the Spindle Drive PCB where it applies power to the spindle drive motor, to be explained later.

The +SPINDLE DRIVE ON signal is also sent to the Address Logic 1 PCB, where it initiates movement of the heads to Track 0 at minimum speed, as later described. When the heads leave the fully retracted position, the Heads Retracted Switches set the Heads Retracted F/F, removing the –UNLOCK DRAWER signal.

When the brushes started their cycle, the brush switches set the Brush Cycle I F/F and the Brush Cycle II F/F. The low $\overline{Q}$ output of the Brush Cycle I F/F maintains drive to the brush motor through the NOR function at "C". With either the Brush Cycle I F/F or the Heads Retracted FF set and providing low signals to the NAND function at "G", drive to the Drawer Unlock Solenoid is removed, and the drawer is locked. It can be seen that the drawer cannot be unlocked while either the head or brushes are out of the full retract position.

As the brushes complete their cycle, the Brush Cycle I F/F and the Brush Cycle II F/F are reset, removing the drive to the brush motor through the NAND function at "C".

With the spindle rotating, index marks are fed to integrator circuitry on the Sequence Logic PCB. When the spindle reaches approximately 50% of its designed speed, the frequency of the index marks is sufficient to cause the integrator circuit output to trigger one section of the Up-to-Speed F/F. One output of the Up-to-Speed F/F is the +SPEED OK signal. This is sent to the Spindle Drive PCB, where it enables full current input to the spindle drive motor, bringing it to full rated speed.

Another output of the Up-to-Speed F/F is triggered by the integrator when the spindle reaches approximately 90% of its designed speed. It is at this speed that the heads can be safely loaded. This signal is sent to a three-input NAND gate function shown at "E". Meanwhile, the heads have moved to Track 0. A shutter on the head carriage prevents the light from a light-emitting diode from falling on a photosensor when the heads are over the disk. The output of photo sensor, amplified and gated on the Sensor PCB, produces a +HEADS OVER DISK signal. This provides another input to the NAND function at "E" in Figure 5-7. The third input to the gate was furnished when the Brush Cycle I F/F was reset by the brushes reaching the fully retracted position. The output is ANDed at "B" with the output of the Brush Cycle II F/F. The output at "E" furnishes the –HEAD LOAD ENABLE signal and also triggers the Head Load One-Shot, whose output is the 700 ms +HEAD LOAD PICK signal. The –HEAD LOAD ENABLE signal and the +HEAD LOAD PICK signal are sent to the Heat Sink Assembly where they drive the transistors which energize the Head Load Solenoid. The pick signal pulls the solenoid in with a 48-volt pulse, while the enable signal maintains the energized condition with 24 volts.

An output of the Head Load One-Shot is also ANDed with the –HEAD LOAD ENABLE signal at "F". The "F" output conditions the Heads Loaded Signal F/F, so that the next index pulse will cause the +HEADS LOADED signal. In addition to maintaining the +SPINDLE DRIVE ON signal at "H", the +HEADS LOADED signal is sent to the R/W Amplifier PCB, where it is ANDed with the NOT WRITE CHECK signal. The NOT WRITE CHECK signal is present in the absence of certain write faults later described.

The FILE READY signal is sent to the interface to inform the controller that the disk drive is ready for its first seek command.

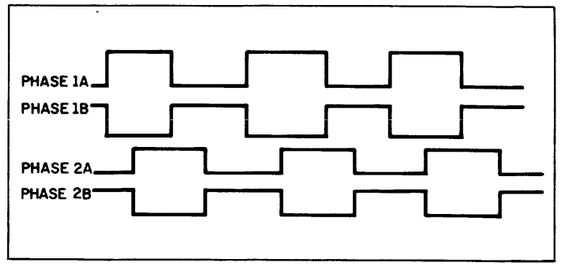


Figure 5-8. Spindle Drive Signals

FILE READY is maintained as long as heads are loaded and there is no write check. FILE READY is also sent to the Address Logic 2 PCB and the Sensor PCB as explained later.

5.2.3 Spindle Drive and Speed Control

Drive signals for the spindle drive motor originate on the Oscillator PCB, where a 1.92 MHz crystal-controlled oscillator operates whenever power is applied to the Series 40. The output of the oscillator is divided into two 80 Hz square waves (50 Hz for 1500 rpm drives) which are 90° out of phase referred to as Phase 1 and Phase 2. These square waves are sent to the Spindle Drive PCB, where an inversion of each phase is also developed. These four signals are shown in their proper phase relationship in Figure 5-8. When properly gated on the Spindle Drive PCB as explained in this paragraph, these four signals drive two push-pull type power amplifiers on the Heat Sink Assembly. The output of each amplifier drives one phase of the two-phase spindle drive motor.

Figure 5-9 is a simplified functional block diagram showing the sequence of operation of the spindle drive and speed control circuits from setting of the LOAD/RUN Switch to the RUN position, through the spindle up-to-rated-speed condition, until stopping of the spindle after placing the disk drive back in the LOAD mode.

The sequence of events can be summarized as follows:

1. Set LOAD/RUN switch to RUN; +SPINDLE DRIVE ON goes high.

2. Outputs of the four phase amplifiers are enabled; Speed Sense F/F and Phase 1 F/F are set; Phase 1 and Phase 2 signals from Oscillator PCB are gated to the four phase amplifiers; Spindle Drive Motor starts rotation.

3. SPEED OK signal from Sequence Logic PCB allows motor to draw full current; spindle comes up to rated speed.

4. Set LOAD/RUN switch to LOAD; +SPINDLE DRIVE ON goes low; output of Phase 2 amplifiers grounded, grounding Phase 2 motor winding.

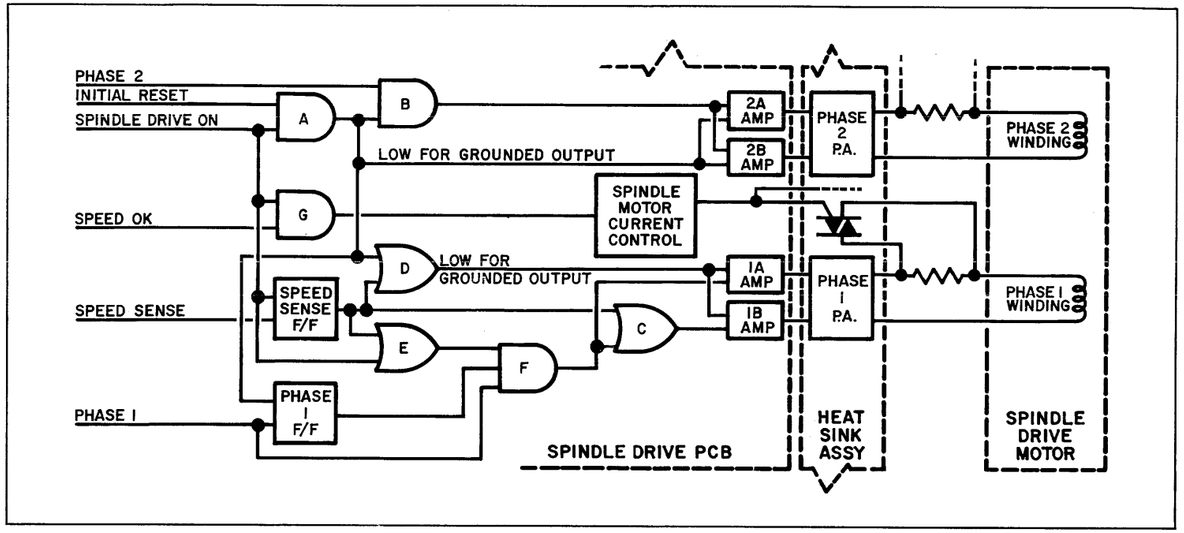


Figure 5-9. Spindle Drive Speed Control

5. Speed Sense F/F grounds Phase 1B output and keeps Phase 1A output high, braking the motor to stop in approximately 15 seconds.

6. When motor stops, Speed Sense F/F grounds outputs of Phase 1 amplifiers.

The remainder of this subparagraph describes how these six events occur. Where a signal or power frequency of 80 Hz is reffered to, a frequency of 50 Hz applies for 1500 rpm disk drives.

Referring to Figure 5-9, the following conditions exist with power on and the disk drive in the LOAD mode:

- The –INITIAL RESET line is high

- PHASE 1 and PHASE 2 80 Hz square waves are present at the input of the Spindle Drive PCB

- The +SPINDLE DRIVE ON line is low

- The outputs of the four phase amplifiers are grounded.

When the disk drive is placed in the RUN mode, +SPINDLE DRIVE ON goes high, as described in 5 2.2.4. This is gated at "A" and again at "D" to remove the grounds from the four amplifier outputs. The output at "A" also gates the Phase 2 square wave through "B", driving the Phase 2B and Phase 2A amplifiers. These in turn drive the Phase 2 Power Amplifier on the Heat Sink Assembly, energizing the Phase 2 winding of the motor.

Meanwhile, the output of the AND function at "A" has reset the Phase 1 F/F, conditioning one input of a three-input AND function at "F". Another input was conditioned by the +SPINDLE DRIVE ON signal gated through "E". Phase 1 square waves are now gated through "F" and "C" to the Phase 1 amplifiers. With both windings energized, the Spindle Drive Motor begins rotating.

When the motor has reached approximately 50% of its rated speed, the +SPEED OK signal is generated as described previously. This signal is gated to the Spindle Motor Current Control circuitry where a ground is furnished to two Triac switches on the Heat Sink Assembly. For clarity, only the Triac for Phase 1 is shown. The Triacs fire, bypassing resistances in the motor winding leads. The motor now operates on full current and attains its rated speed.

When the LOAD/RUN switch is set to the LOAD position, +SPINDLE DRIVE ON goes low. Through gate functions "A" and "B" in Figure 5-9, drive to the Phase 2 amplifiers is removed, and their outputs are grounded. The outputs of the Phase 1 amplifiers are not immediately grounded since a high output at OR function "D" is maintained by a high input from the Speed Sense F/F. This F/F also maintains a high input to the "F" gate through "E". Removal of the +SPINDLE DRIVE ON signal has removed the force reset of the Phase 1 F/F, which is a two-section F/F. To insure that the triacs are off prior to initiation of the braking mode, the Phase 1 F/F counts two Phase 1 pulses before removing its high input to "F". The Phase 1 amplifiers now go into the braking mode with Phase 1B output low and Phase 1A output high. This passes a DC current through the Phase 1 motor winding which acts as a brake. The motor stops in about 15 seconds.

As the motor decelerates, the SPEED SENSE signal decreases. As the motor approaches a complete stop, SPEED SENSE drops to zero, and the Speed Sense F/F toggles. This removes the drive to the Phase 1B amplifier through "C", and grounds the output of the Phase 1 amplifiers through "D".

5.2.4 Servo System

The servo system has two modes of operation, speed control mode and detent mode. It operates in the speed control mode during head positioning operations and in the detent mode when the heads are held stationary between positioning operations.

When the servo is in the speed control mode, it provides controlled drive current to the head positioning motor. The amount of drive current supplied determines head velocity. The drive current's polarity determines the direction of head motion.

When operating in the detent mode, the servo system provides current to the motor as required to counter any drift or forced movement of the heads away from the detent position.

In either mode, the motor drive current is controlled by an analog signal generated by the servo system. This control signal, designated Servo Drive Signal, operates as an error voltage. Its amplitude and polarity represent deviations of the heads from specified velocity or position conditions.

During head positioning operations (speed control mode) the positive or negative amplitude of Servo Drive Signal represents the difference between desired head velocity and actual head velocity. The signal's polarity specifies the direction of head motion. This difference is translated into motor drive current of a value and polarity necessary to bring the actual velocity to the specified level.

Actual head velocity will be less than desired velocity during the acceleration stage of a head positioning operation. On longer seeks, when actual head velocity reaches the maximum specified velocity, Servo Drive Signal returns to zero potential, the drive current is removed and the heads positioner coasts. As friction reduces positioner velocity to below the specified level, the positive or negative amplitude of Servo Drive Signal increases sufficiently to bring the velocity back to the desired level.

As the heads approach the destination cylinder, the velocity requirement is reduced by increments. At each reduction, the specified head velocity drops below the actual head velocity. At those times, Servo Drive Signal increases in amplitude, with a polarity opposite to the one used for acceleration. This causes the motor drive current to act as a brake, decelerating the heads until their velocity equals the new target velocity.

Figure 5-10 provides a conceptual graph of actual versus specified velocity curves for a 10-cylinder seek. These curves do not represent any actual signals. The desired velocity curve for any given seek is determined by cylinder addressing control logic

on AL1 and AL2 circuit boards. This logic is discussed in Sections 5.2.5, 5.3.14 and 5.3.15.

In the detent mode, any movement of the heads away from the detent position causes the amplitude of SERVO DRIVE SIGNAL to become more positive or more negative, depending on the direction of head motion. The resulting potential produces a motor drive current that acts to counter the undesirable head motion and brings the heads back to the detent position.

SERVO DRIVE SIGNAL is produced by summing the voltage levels of two analog signals. This summing junction is illustrated in Figure 5-11.

One input to the summing junction is the speed control term. Its amplitude represents the velocity at which the heads should be moving and its polarity specifies the direction of motion. The other input is the feedback term. Its amplitude represents actual head velocity and its polarity indicates the complement of the direction the heads are moving.

The polarities of the two summing junction input terms are both determined by direction information supplied by the head position transducer. Servo system logic assures that the two terms always have opposite polarities.

Since the amplitudes of the two summing junction inputs are not directly related, they have different values at different stages of a head positioning operation. During the acceleration stage, the speed controller term's amplitude exceeds the amplitude of the feedback term. During deceleration, each time the velocity requirement is incrementally reduced, the feedback term is temporarily greater.

These imbalances in signal levels appear at the summing junction as a positive or negative potential. The polarity of the error signal at the summing point depends on which direction the heads are moving in and whether actual head velocity is less than or greater than the specified velocity.

The resulting signal at the summing junction is inverted by an operational amplifier and sent out as SERVO DRIVE SIGNAL.

The polarity of SERVO DRIVE SIGNAL is such that it has the effect of bringing the error voltage at the summing junction to zero potential. It does this by causing the heads to accelerate or decelerate until the feedback term matches the speed control term in amplitude.

When the two summing junction input terms have equal amplitudes, SERVO DRIVE SIGNAL is at zero potential. This occurs when the heads are actually moving at the specified velocity or when the heads are detented.

In the detent mode, the speed control and feedback terms are both at zero potential so long as the heads remain stationary. If the heads move away from the detent position, the two terms develop opposite polarities and different amplitudes, bringing the summing junction into an imbalance. The resulting SERVO DRIVE SIGNAL acts to move the heads back to the detent position.

Figure 5-12 illustrates the major functional elements of the servo system in block diagram form. These elements, and the principal propagation paths through the servo system are discussed in the following subsections.

5.2.4.1 Power Driver Circuit

The motor drive current is provided by a Power Driver Circuit of the push-pull type. This circuit is on the HS circuit board. The amount of current and its polarity are controlled by SERVO DRIVE SIGNAL, an analog input that originates at the SO circuit board. The development of SERVO DRIVE SIGNAL is described in the following subsections.

A Current Limiting Circuit, which is in series with the motor current's feedback path, limits the amount of current the Power Driver Circuit can supply to the motor. This circuit is also located on the HS circuit board.

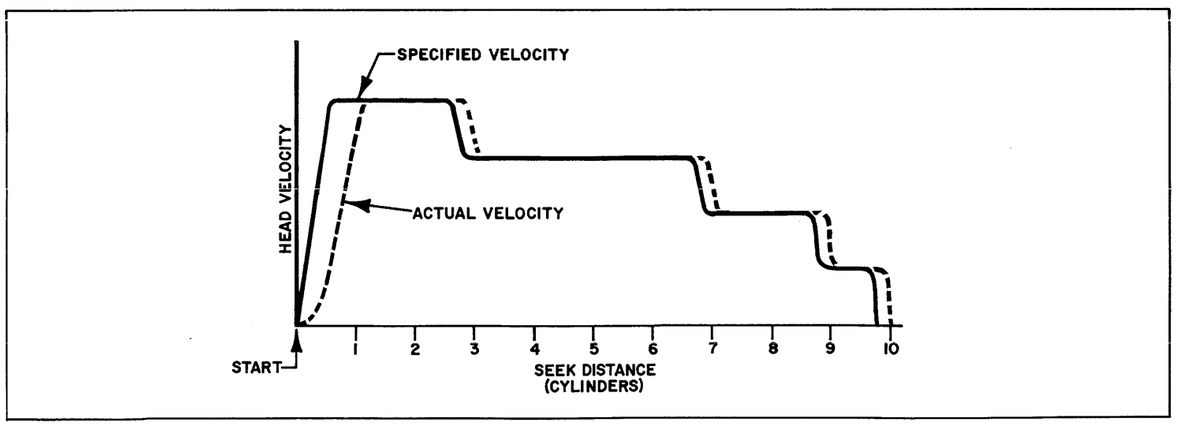


Figure 5-10. Sample Actual Velocity Curve vs. Specified Velocity Curve

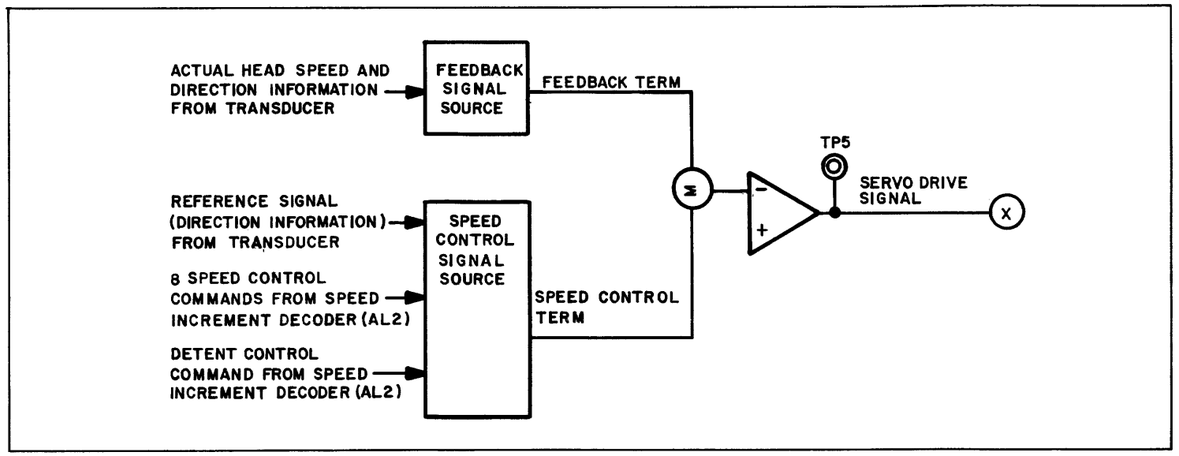


Figure 5-11. Servo System Main Summing Junction

If the positioning motor attempts to draw excessive current, a Current Detector Circuit senses the high current and causes the Servo Disable/Seek Incomplete latch to set. This latch, which is located on the SR circuit board, disables the Servo Driver Circuit. A restore or initial reset operation will reset the flip-flop and return the Power Driver Circuit to normal operation.

5.2.4.2 Head Positioning Transducer

The servo system uses the output of an induction-type printed circuit transducer to develop head position and velocity information. It also decodes this transducer output into cylinder count pulses. These pulses are used by the cylinder addressing control logic to increment or decrement the Present Address Counter.

In this transducer, the primary coil consists of a printed conductor pattern. This member of the transducer, called the slider, is located on the underside of the head positioning carriage. It moves with the carriage during head positioning operations.

The transducer's secondary coil is formed by a pair of interleaved conductor patterns. These patterns are printed on an epoxy glass substrate, which is bonded to the top surface of an aluminum alloy plate. The plate is mounted on the carriage way facing the slider. This secondary member of the transducer, referred to as the scale, is stationary.

The transducer primary is driven by a 480 KHz signal. This signal originates at 1.92 MHz crystal oscillator. The oscillator's output frequency is divided by four. The resulting 480 KHz signal is integrated. The output of the integrator circuit drives the primary coil of a transformer. The signal appearing at the transformer's secondary coil drives the transducer's primary element.

Figure 5-13 provides a conceptual view of the transducer. To simplify the illustration, the slider and scale are shown as if they were opposite pages of an open book. In reality, the slider moves along a path directly above the scale.

During head positioning, the motion of the slider with respect to the scale varies the degree of primary-to-secondary coupling that occurs in each secondary trace. This motion produces a pair of modulated sine wave signals on the transducer's two output channels. The channel A and channel B output wave shapes are represented in Figure 5-14.

The 90° phase displacement between the channel A and channel B modulation envelopes shown in the drawing is a function of the relative spacing between the secondary traces. This phase information is used by the servo system to detect which direction the heads are moving, and to develop track crossing information.

When the heads are detented, the channel A and channel B envelopes have constant amplitudes. If the heads move away from the detent position, this motion shows in the amplitude modulation that occurs on the envelopes.

The channel A and channel B signals are applied to amplifier/demodulating logic on the SO circuit board.

5.2.4.3 Amplifier Demodulation Network

The heart of the servo system's demodulation logic consists of a pair of monolithic balanced modulator devices operating in the demodulation mode. Two differential video amplifiers at the inputs to the demodulation devices amplify the channel A and channel B signals before demodulation is performed.

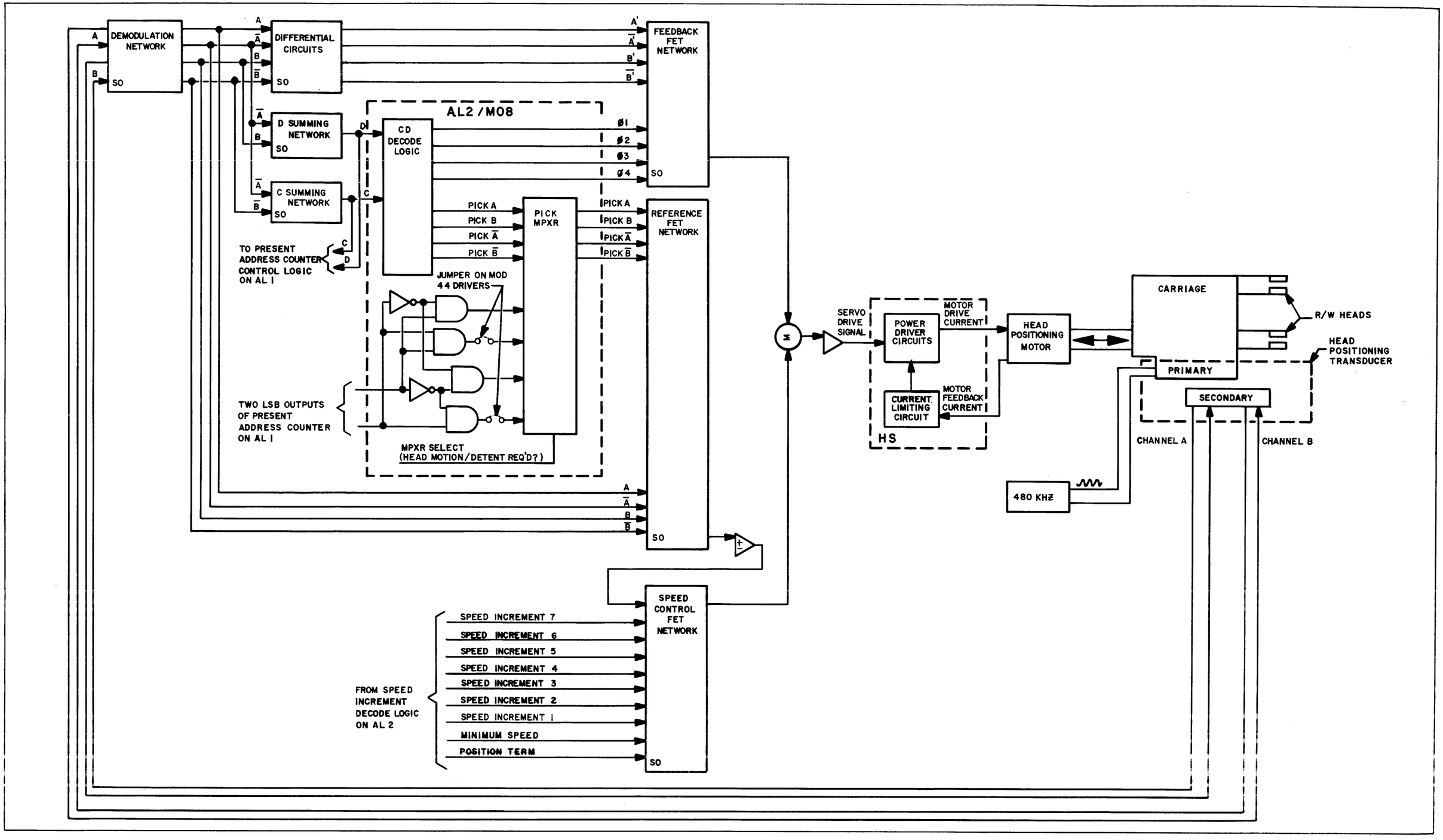


Figure 5-12. Servo System Functional Block Diagram

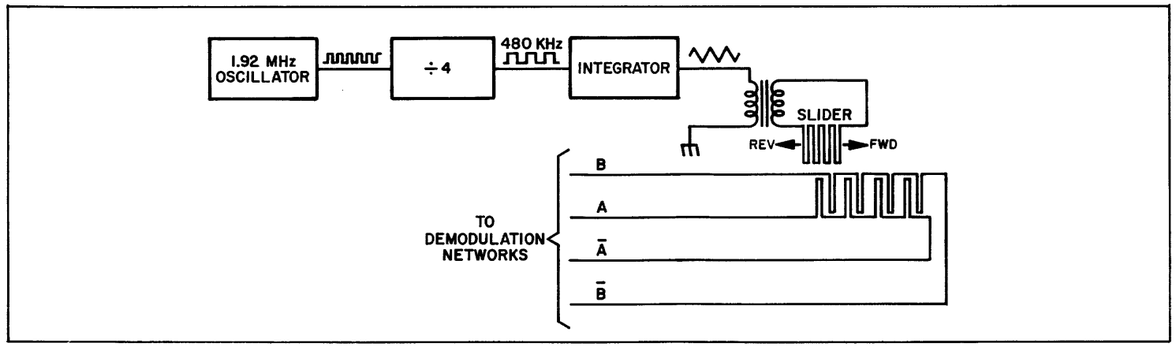


Figure 5-13. Head Position Transducer Slider/Scale Relationship

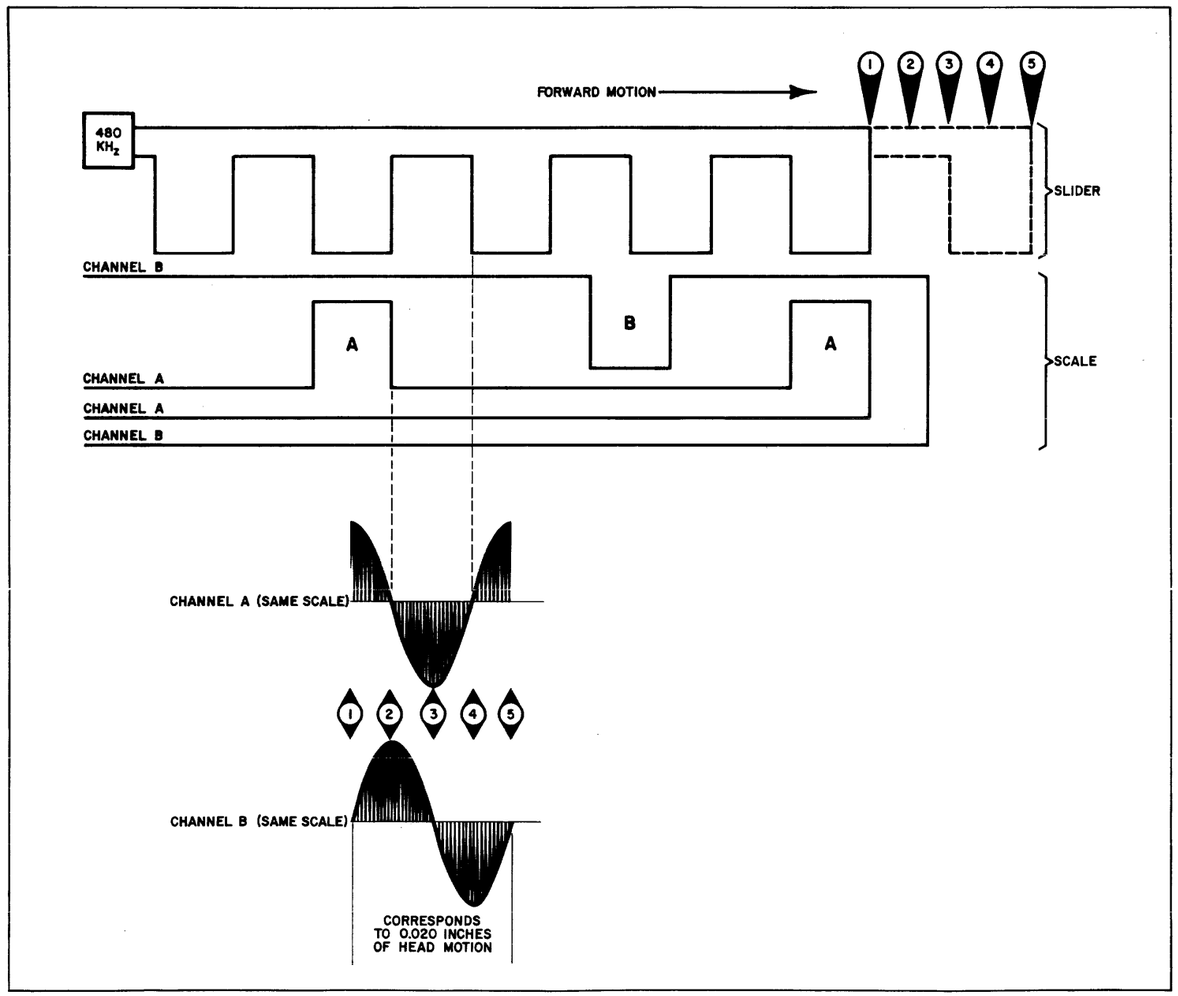


Figure 5-14. Head Position Transducer Output Wave Shapes

Each demodulating device provides both true and complement outputs. These demodulated output signals are amplified and distributed to various functional elements of the servo system.

The four amplified outputs, designated A, $\overline{A}$, B and $\overline{B}$, are used by these elements to perform a variety of related functions.

1. They are used by the Reference FET Network to develop a speed control reference input to the Speed Control FET Network.

2. They are also applied to the Differential Circuits to develop the differentiated wave shapes A′, $\overline{A}$′, B′ and $\overline{B}$′. These are used by the Feedback FET Network to develop the feedback input to the summing junction.

3. A pair of sequence control signals, designated C and D, are developed by logical summation gates acting on $\overline{A}$, B and $\overline{B}$. The resulting C and D signals are square waves, with a 90° phase relationship.

5.2.4.4 C and D Summing Networks

These networks simply consist of one of the Demodulation Network's outputs $\overline{A}$ being tied at separate summing points to two other Demodulation Network outputs, B and $\overline{B}$. See Figure 5-15.

The resulting summation signals are inverted by a pair of operational amplifiers to become SERVO LOGIC CONTROL LEVEL C and SERVO LOGIC CONTROL LEVEL D.

Together, these phase-related square waves provide position and direction information about the heads as they move from cylinder to cylinder. Specific level transitions indicate that the heads have reached a new cylinder position. The order in which the level transitions occur represents the direction of head travel.

These CD pulse trains are sent to CD Decode logic on AL2 to develop the gate control signals ϕ 1 through ϕ 4 and Pick A through Pick $\overline{B}$. The CD Decode logic is described in the following subsection.

SERVO LOGIC CONTROL LEVEL C and SERVO LOGIC CONTROL LEVEL D are also sent to the Present Address Counter Control logic on AL1. There, they are used to generate count up or count down pulses for the Present Address Counter.

5.2.4.5 CD Decode

This logic develops gate control signals for use by the Feedback FET Network and Reference FET Network.

During head positioning operations the ϕ 1 through ϕ 4 outputs are generated in a sequence determined by the order of transitions occurring on the C and D inputs. They are issued to the Feedback FET Network where they are used to control the commutation of the differentiated wave shapes A., $\overline{A}$., B , $\overline{B}$.

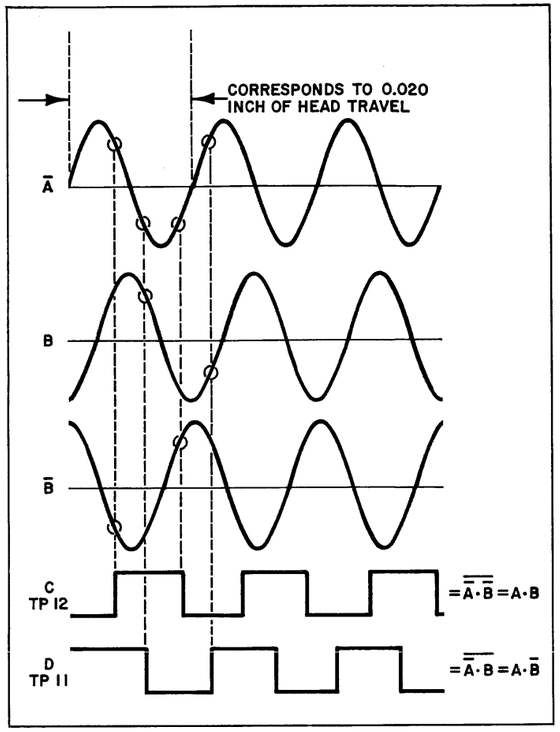


Figure 5-15.
Derivation of C and D Signals from $\overline{A}$, B and $\overline{B}$

The PICK outputs are generated in a similar fashion except that the generation of these signals involves two stages of multiplexing.

One stage controls the sequencing of PICK outputs to provide the proper sequence for forward and reverse head positioning operations.

The other multiplexing stage controls the selection of the PICK output for detenting.

Details regarding the CD Decode logic are provided in Section 5.3.14.2, CD Decode.

5.2.4.6 Differential Circuits

These Differential Circuits consist of four capacitor/resistor pairs. Each pair is connected in series with one of the Demodulation Network outputs.

The capacitance in each of these series circuits produces an AC signal that lags the driving signal by 90° and whose amplitude is directly proportional to the transducer modulation frequency. See Figure 5-16.

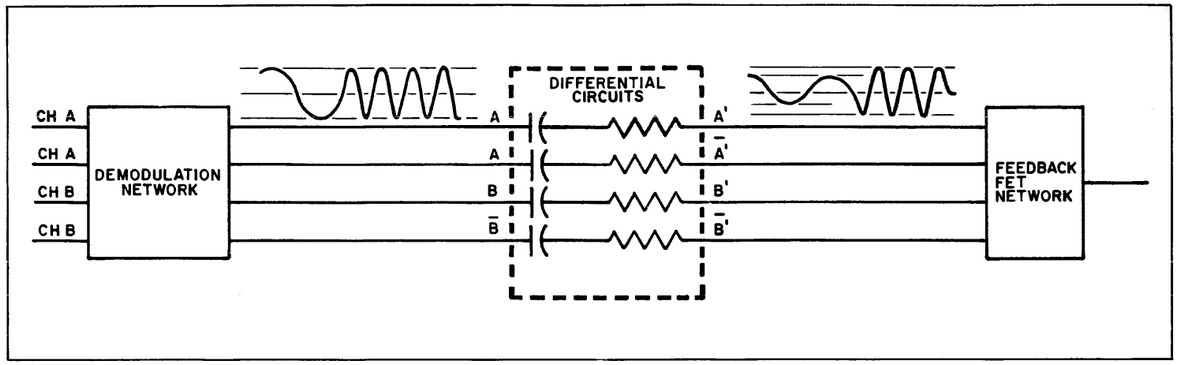


Figure 5-16. Differential Circuits Input/Output Wave Shapes

The differentiated wave shapes, A', $\overline{A}$', B' and $\overline{B}$', are used by the Feedback FET Network to develop the feedback input to the summing junction.

5.2.4.7 Feedback FET Network

The Feedback FET Network provides an analog input to the summing junction. The positive or negative amplitude of this input is directly proportional to actual head velocity. Its polarity represents the complement of the direction of head travel.

This velocity feedback term is derived from the four outputs of the Differential Circuits through a process of commutation. The positive or negative peaks of A', $\overline{A}$', B. and $\overline{B}$' are sequentially gated through the Feedback FET Network to the summing junction by Ø 1, Ø 2, Ø 3 and Ø 4. All other segments of the four signals are blocked at the FET switches.

When the heads are moving forward, the positive peaks are selected by Ø 1, Ø 2, Ø 3 and Ø 4; during reverse head motion, the negative peaks are selected. This commutation process is direction sensitive because the wave shape produced by each differentiated signal during reverse motion is the complement of the forward motion wave shape.

Since the differentiated input signals are also velocity sensitive, the amplitude of the Feedback FET Network's output is directly proportional to head positioner velocity.

These signals and the segments gated through the Feedback FET Network are represented in Figure 5-17. This figure also illustrates the resulting feedback term that appears at the summing junction during head positioning.

The sample feedback signal shown in Figure 5-17 represents a portion of a forward seek during which the heads move at a constant velocity and then decelerate. This drawing is a conceptual illustration only; no scale relationship to an actual wave shape is intended.

When the heads are detented, the Feedback FET Network's output is at zero potential so long as the heads remain stationary. If they move away from the detent position, the feedback term changes amplitude. The polarity of this amplitude depends on the direction of head motion.

5.2.4.8 Reference FET Network

During head positioning operations, the Reference FET Network provides the Speed Control FET Network with a speed control reference term. This rippled DC level serves as a reference voltage for the speed control switches, permitting the active switches to contribute a speed control input to the summing junction. The amplitude of the speed control reference term is constant. Its polarity depends on which direction the heads are required to move. For forward motion, the output of the amplifier shown in Figure 5-12 is negative; for reverse motion, TP3 is positive.

When operating in the detent mode, the speed control reference term functions as a position reference term. As long as the heads remain stationary at the detent position, the Reference FET Network's output is at zero potential.

If the heads begin to move away from the detent position, the speed control/detent reference term changes to a positive or negative amplitude. Head motion toward the spindle (forward) causes TP3 to become negative; if the heads move away from the spindle (reverse), TP3 becomes positive. The resulting DC level is used by the Speed Control FET Network to generate a position correction input for the summing junction.

The speed control reference term is generated through a commutation process equivalent to the one used to generate the feedback term (refer to Section 5.2.4.7 Feedback FET Network). The principal difference between the operations of the two networks is in the characteristics of their respective inputs.

The Feedback FET Network performs the commutation operation on the differentiated wave shapes, A', $\overline{A}$', B' and $\overline{B}$'. The

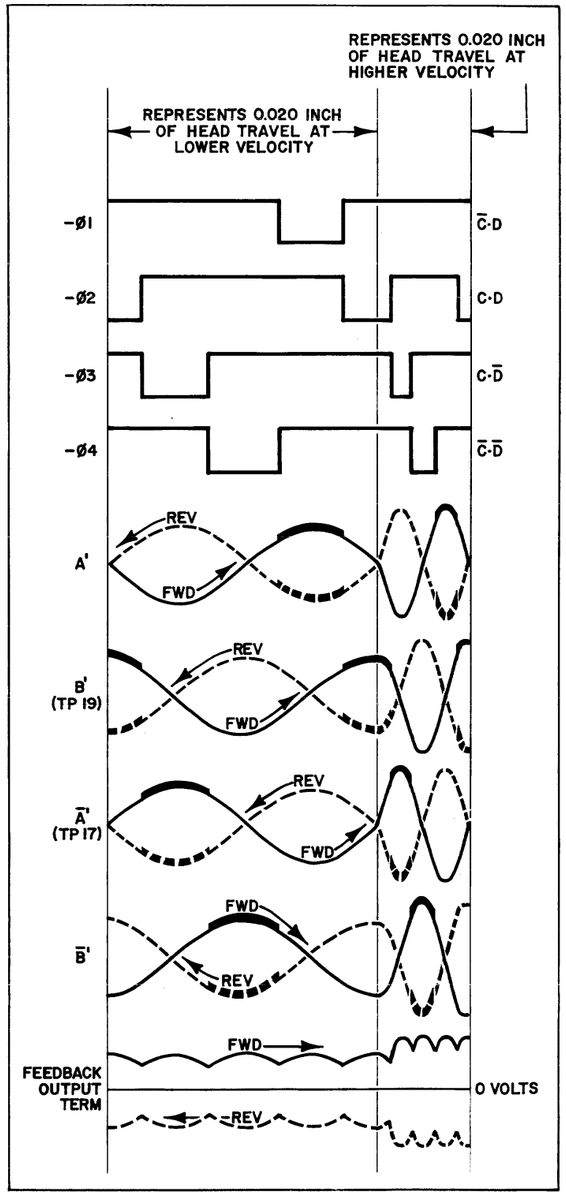


Figure 5-17.
Feedback FET Network Input/Output Signals

Reference FET Network acts directly on the demodulated wave shapes A, $\overline{A}$, B and $\overline{B}$.

Consequently, the feedback term's amplitude is directly proportional to head velocity while the speed control reference term is rippled DC level, that leads the velocity by 90°.

In addition, the two network outputs have a 90° phase displacement with respect to each other. This shift is significant in detent operations where the lag between the two terms in arriving at zero potential has a damping effect on the positioning motor. Because the system detents in a critically damped fashion, the heads are moved directly to the detent position instead of oscillating around the position.

During head positioning operations, the positive or negative peaks of A, $\overline{A}$, B and $\overline{B}$ are sequentially selected by the four commutation control inputs Pick A, Pick $\overline{A}$, Pick B and Pick $\overline{B}$. For forward head motion, the negative peaks are selected; when the heads are moved away from the spindle (reverse motion), the positive peaks are selected.

The order in which PICK A, PICK $\overline{A}$, PICK B and PICK $\overline{B}$ are generated determines which peaks are selected. CD Decode logic on AL2, which is the source of these commutation control inputs, is responsible for controlling their sequencing. Details regarding their origin are presented in Section 5.3.14.2, CD Decode. Figure 5-18 shows the relationship between the four PICK signals and the demodulation envelopes for forward and reverse seeks.

When the servo system enters the detent mode, the PICK sequence is interrupted and the most recent PICK signal generated by the CD Decode logic is maintained.

This is the PICK signal required for detenting because the selected envelope is approaching its zero crossing rather than its peak. As the heads approach the detent position, the selected demodulation envelope moves along the slope and arrives at the zero crossing just as the heads reach the detent position.

Detenting always occurs at the zero crossing of a positive slope. When the servo system enters the detent mode, the system is conditioned for forward head motion. Consequently, the positive slope of a selected envelope during a reverse head positioning operation becomes a negative slope when the servo system enters the detent mode.

This envelope remains selected until a new head positioning operation begins. At that time, the CD Decode logic initiates a new sequence of PICK signals as required for a forward or reverse sequence.

5.2.4.9 Speed Control FET Network

The Speed Control FET Network's output specifies the velocity characteristics of head motion for any given head positioning operation as well as the direction of head motion. The output amplitude represents the velocity at which the heads should be moving and its polarity determines the direction of motion.

When the servo system is operating in the detent mode, this network generates a position correction signal if the heads attempt to move away from the detent position.

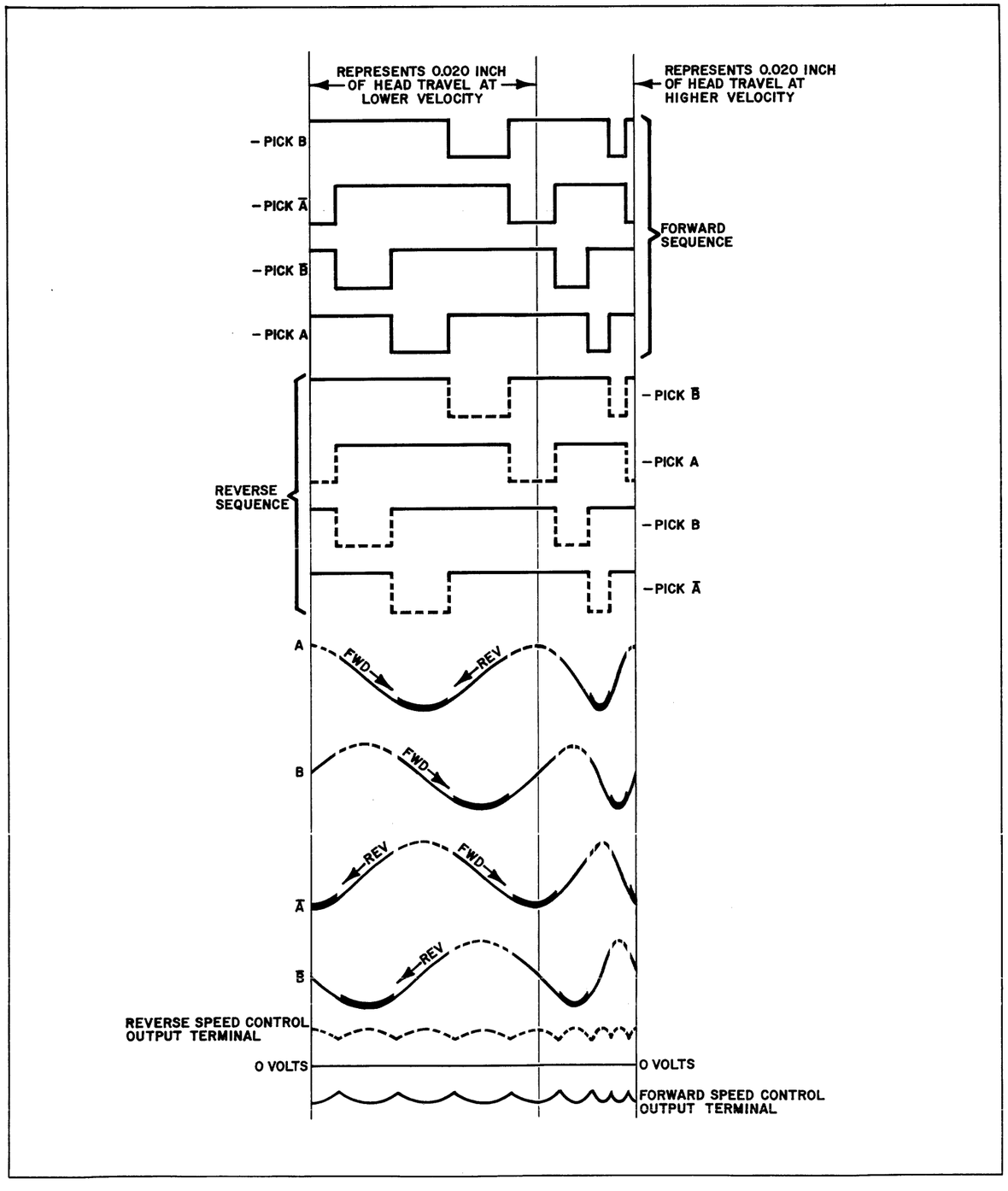


Figure 5-18. Reference FET Network Input/Output Signals

During head positioning operations, the Speed Control FET Network's output is controlled by eight speed command inputs (including MINIMUM SPEED) and a speed control reference signal. The speed commands originate at the Speed Increment Decoder on AL2. The speed control reference term is provided by the Reference FET Network. A ninth input, POSITION TERM controls the network's output in the detent mode. Its function is described later in the subsection when the detent mode is discussed.

Each speed command controls a separate FET switch in the network. During head positioning, one or more of the inputs will gate the speed control reference signal through the network to the summing junction. The amplitude of the FET network output depends on how many switches are enabled.

The number of active speed commands at any given time is directly related to the velocity at which the heads should be moving at that time. That velocity requirement is determined by the Speed Increment Decoder on AL2 (refer to Section 5.3.14 for details).

Figure 5-19 illustrates the changes in SERVO DRIVE SIGNAL caused by enabling and disabling speed commands during a four cylinder seek. The effect of the feedback term on SERVO DRIVE SIGNAL is also shown.

5.2.4.10 Summing Junction

The servo system's main summing junction is formed by coupling the output of the Speed Control FET Network to the output of the Feedback FET Network. This connection is made by printed wire on the SO board at the inverting input to the board's output driver.

Any signal appearing at the summing junction results from the amplitudes of the two inputs to the summing junction being unmatched. Any such error voltage is inverted and amplified by the amplifier and sent to the Power Driver Circuits as SERVO DRIVE SIGNAL.

The effect of SERVO DRIVE SIGNAL on the Power Driver Circuits is to either accelerate or decelerate the heads, whichever will tend to return the summing junction to zero potential.

The following paragraphs describe how the potential at the summing junction is affected by changes to the speed control and feedback terms during head positioning and detent operations. Refer to Figure 5-19, Speed Command vs. Servo Drive Signal in Section 5.2.4.9.

At the start of a seek operation, the appropriate number of speed command inputs to the Speed Control FET Network are activated by Speed Increment Decoder. This causes the speed control input to the summing junction to swing from zero potential to some positive or negative level.

Since the heads are stationary at the start of a seek, the feedback input to the summing junction is at zero potential (test points 17 and 19).

NOTE

These are test points for two of the differentiated signals (B′ and Ā′) as they appear at the outputs of their respective FET switches. To simplify the illustration, the feedback signal trace is drawn as if all four differentiated signals were sampled.

SERVO DRIVE SIGNAL increases in amplitude at the maximum rate initially to start the heads moving. As the heads accelerate, the feedback term appears at the summing junction, causing SERVO DRIVE SIGNAL's amplitude to decrease.

The increasing feedback term continues to reduce the amplitude of SERVO DRIVE SIGNAL until the feedback term matches the speed control term in amplitude. At this point, SERVO DRIVE SIGNAL is at zero potential.

As the heads approach the destination cylinder, the active speed control FET switches are turned off in sequence. One switch is disabled each time the decreasing difference count crosses one of the speed increment thresholds. Disabling these switches reduces the speed control term amplitude by increments.

Each time the value of the speed control term falls below that of the feedback term, a new SERVO DRIVE SIGNAL is generated, with polarity needed to brake the motion of the positioning motor. This polarity is opposite that used to accelerate the head positioner at the beginning of the operation.

With the resulting current acting as a brake, the heads decelerate until the decreasing feedback term matches the new speed control term. At that point SERVO DRIVE SIGNAL again returns to zero potential.

This braking action occurs at each speed increment threshold. When the difference count equals zero, the last switch (MINIMUM SPEED) is disabled and the speed control term returns to zero potential. The resulting SERVO DRIVE SIGNAL slows the heads to zero velocity.

Just before the heads reach the detent position, the servo system enters the detent mode. Operation of the Speed Control FET Network in the detent mode is described below.

When the servo system transfers to the detent mode, a ninth switch in the Speed Control FET Network is turned on by POSITION TERM. This input to the FET network is provided by Speed Increment Decode logic on AL2.

The POSITION TERM switch gates whatever signal is present on the speed control reference line through to the summing junction. When the servo system is in the detent mode, CD

Decode logic on AL2 causes the speed control reference term to be held at zero potential. This is done by selecting whichever one of the four differentiated wave shapes (A, $\overline{A}$, B and $\overline{B}$) will be at the zero crossover of its positive slope when the heads are at the detent position. This selection is made in the Reference FET Network, causing its output, speed control reference term to hold at this zero crossover point.

Details regarding the origin of the speed control reference term are given in Section 5.2.4.8, Reference FET Network and Section 5.3.14.2, CD Decode.

If the heads begin to move in either direction away from the detent position, the speed control reference term moves up or down the selected slope. This change in amplitude causes a corresponding change in the speed control input to the summing junction.

As a result, an error voltage is produced at the SERVO DRIVE SIGNAL output, which brings the heads back to the detent position.

Movement of the heads also causes the feedback term to assume a positive or negative polarity (always the complement of the speed control term). Use of the feedback term in detenting serves to damp the action of the positioning motor. In this way, the heads are brought directly to the detent position.

5.2.5 Head Positioning Control

Direct control of head motion is provided by the servo system, as described in the previous section. However, the servo itself receives instructions for moving the heads from a section of logic referred to in this manual as the head positioning control logic. This area of logic has the following responsibilities.

1. It stores the cylinder address received from the controller. This is the address of the cylinder to which the drive is instructed to move the heads.

2. It checks the destination address for validity. If the address is too large, it notifies the controller (with LOGICAL ADDRESS INTERLOCK).

3. It stores the address of the cylinder at which the heads are presently located and keeps this register updated as the heads move from cylinder to cylinder.

4. It computes the difference between the present cylinder address and the destination address. The result represents the distance the heads must travel and the direction of motion.

5. It issues speed commands to the servo system's Speed Control FET Network. These commands specify the maximum head velocity for each stage of a head positioning operation.

6. It provides direction control to the servo system's CD Decode logic to control the direction of head motion.

7. It specifies the mode of operation for the servo system (i.e., speed control mode or detent mode).

8. Initiates restore operations and controls head speed and direction during restore.

9. Initiates retract operations and controls head speed and direction during the operation.

10. Controls head speed and direction of motion when heads are moved from the fully retracted position to the head loading position. This operation is referred to as the preload head advance.

The four head positioning operations mentioned above, seek, restore, retract and preload head advance, are described in flow chart form in Figures 5-20 through 5-23.

Figure 5-24 illustrates the nine functional blocks that comprise the head positioning control logic. Each functional element shown in that diagram is discussed in the following subsections.

5.2.5.1 Cylinder Address and Command Receivers

These line receivers buffer the cylinder address information present on the I/O cable. The receiver devices are gated by a select from the controller. Gating is also conditioned by an internal requirement for the heads to be loaded.

The Strobe and Restore commands issued by the controller are also buffered by gated line receivers. These two inputs are gated by the same conditions that control the cylinder address receivers.

5.2.5.2 Address Inhibit Gates

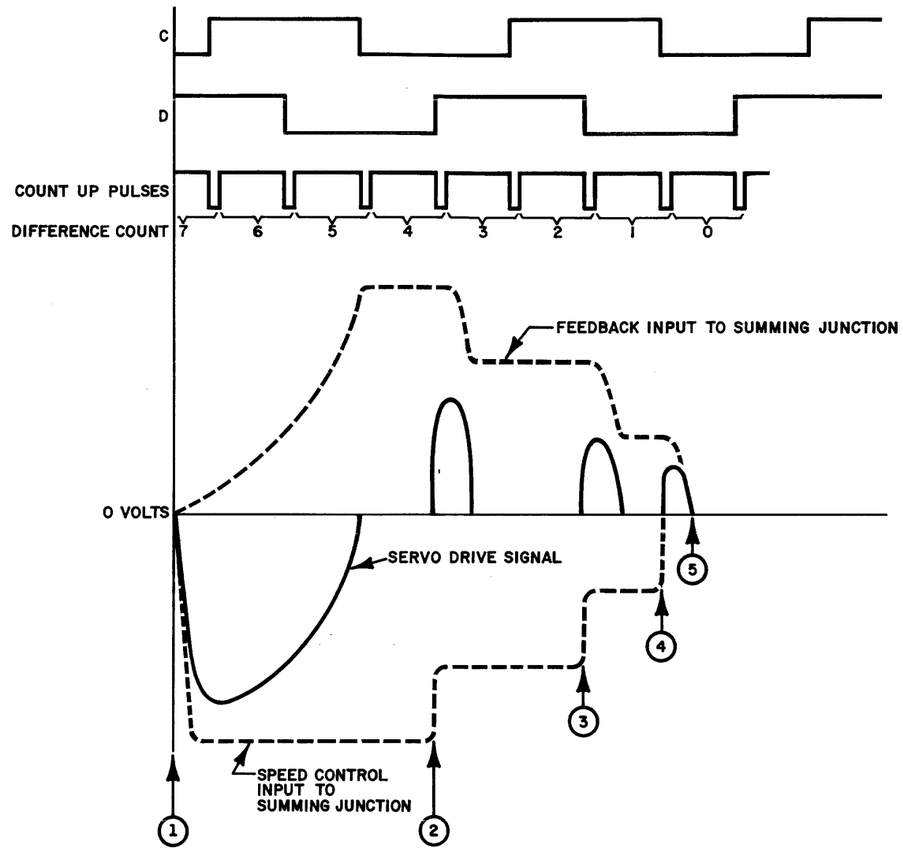
These gates are used to force all cylinder address inputs to the logical ZERO state during any sequence that moves the heads to cylinder 0 (e.g., during restore operations) or that moves the heads to their retracted position. The address word provided by the controller is gated through to the Address Check Logic and Destination Address Register during seeks to addressed cylinders.

5.2.5.3 Address Check Logic

This logic tests the cylinder address at the outputs of the Address Inhibit Gates to determine whether or not its value exceeds the maximum legal address for the disk drive. If the address value exceeds 203 for the Model 43 or 407 for the Model 44, a Logical Address Interlock condition results.

5.2.5.4 Destination Address Register

This register holds the address of the next cylinder to which the heads must be moved.



(1) REMOVE POSITION TERM AND TURN ON MINIMUM SPEED, SPEED INCREMENT 1 AND SPEED INCREMENT 2.
(2) REMOVE SPEED INCREMENT 2.
(3) REMOVE SPEED INCREMENT 1.
(4) REMOVE MINIMUM SPEED COMMAND AND TURN ON POSITION TERM COMMAND. (1/4 CYLINDER AWAY FROM DETENT).
(5) DETENT.

Figure 5-19. Speed Commands vs. Servo Drive Signal

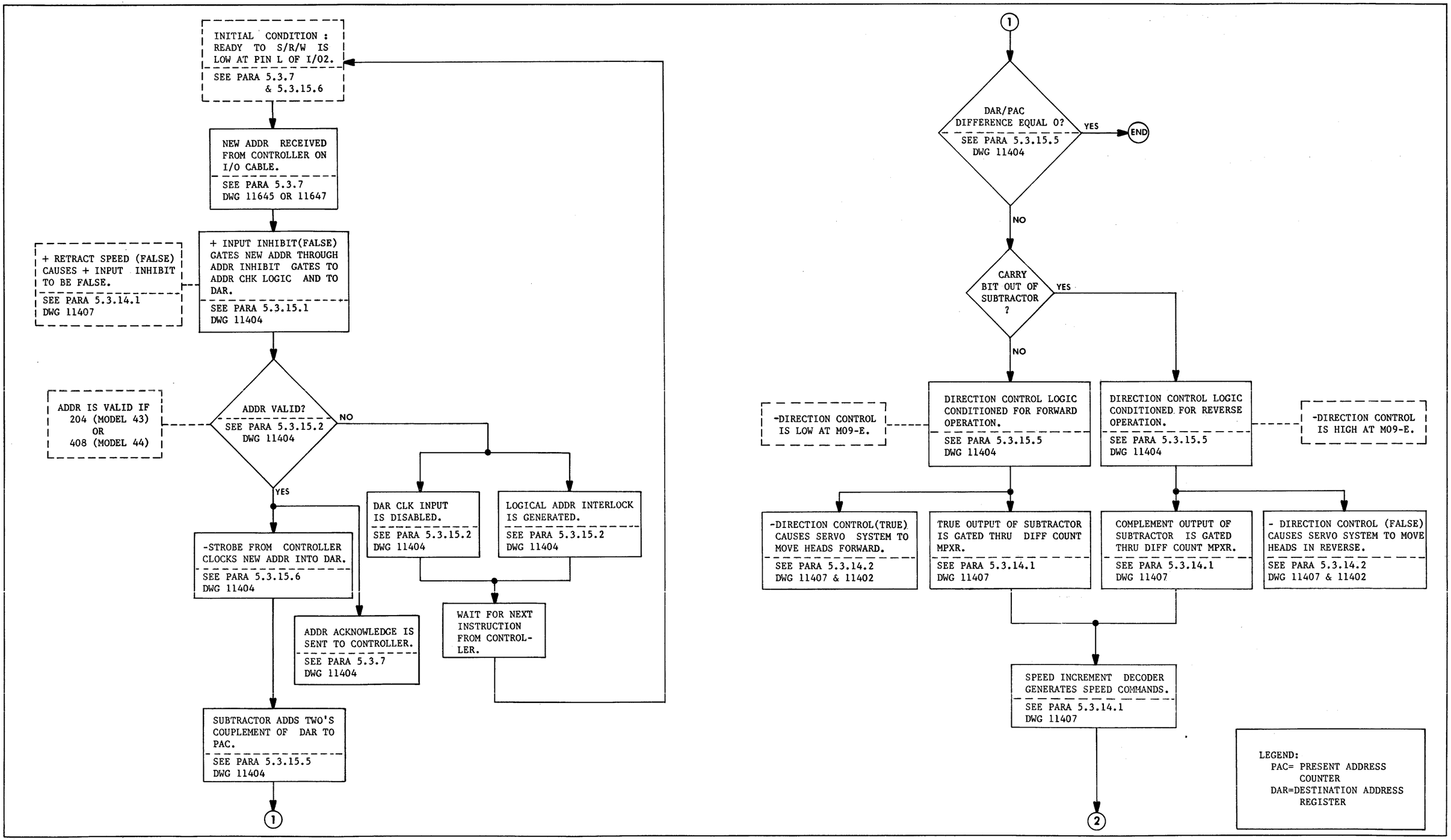


Figure 5-20.A Seek Operation Flow Chart

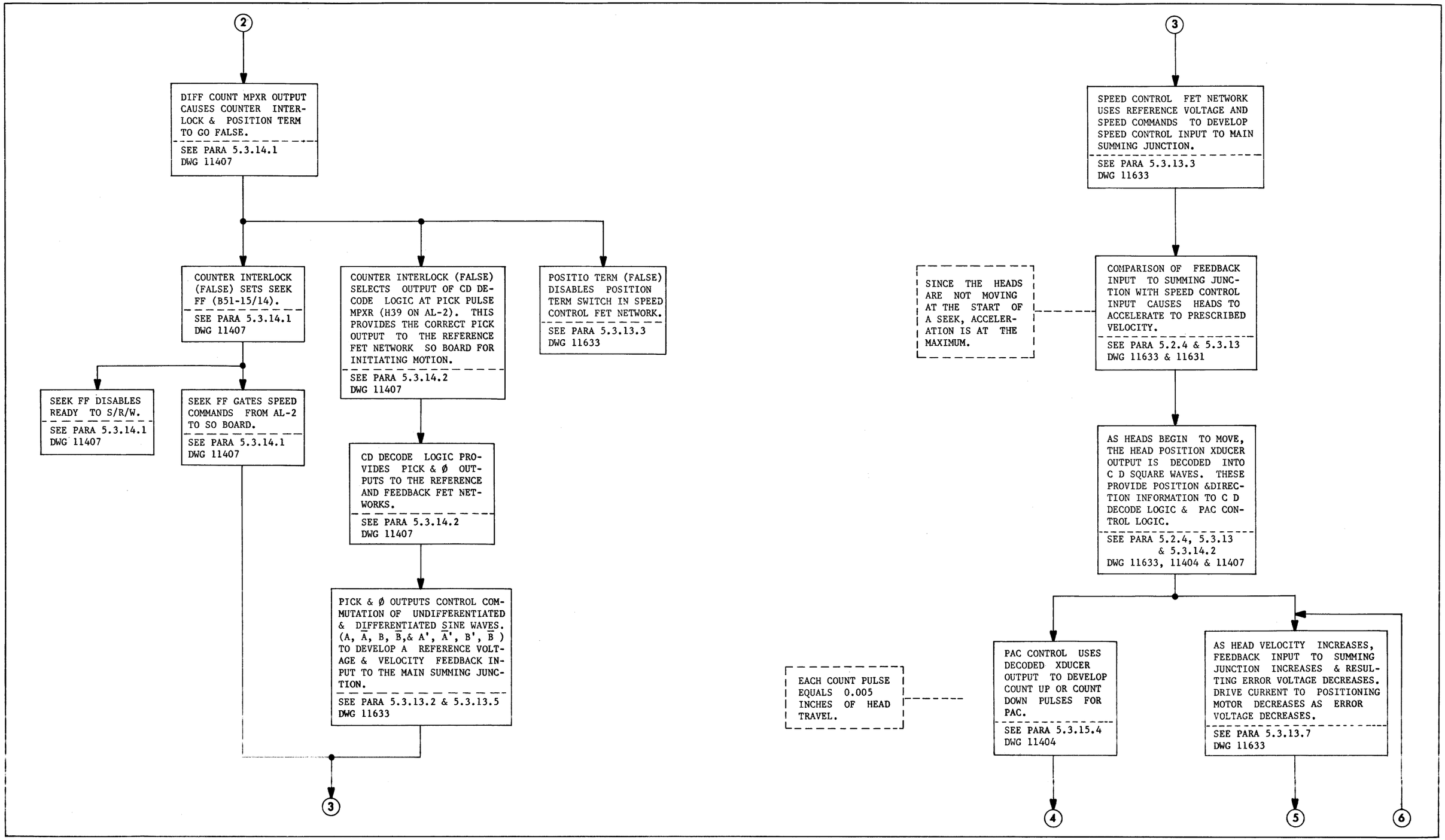


Figure 5-20.B Seek Operation Flow Chart

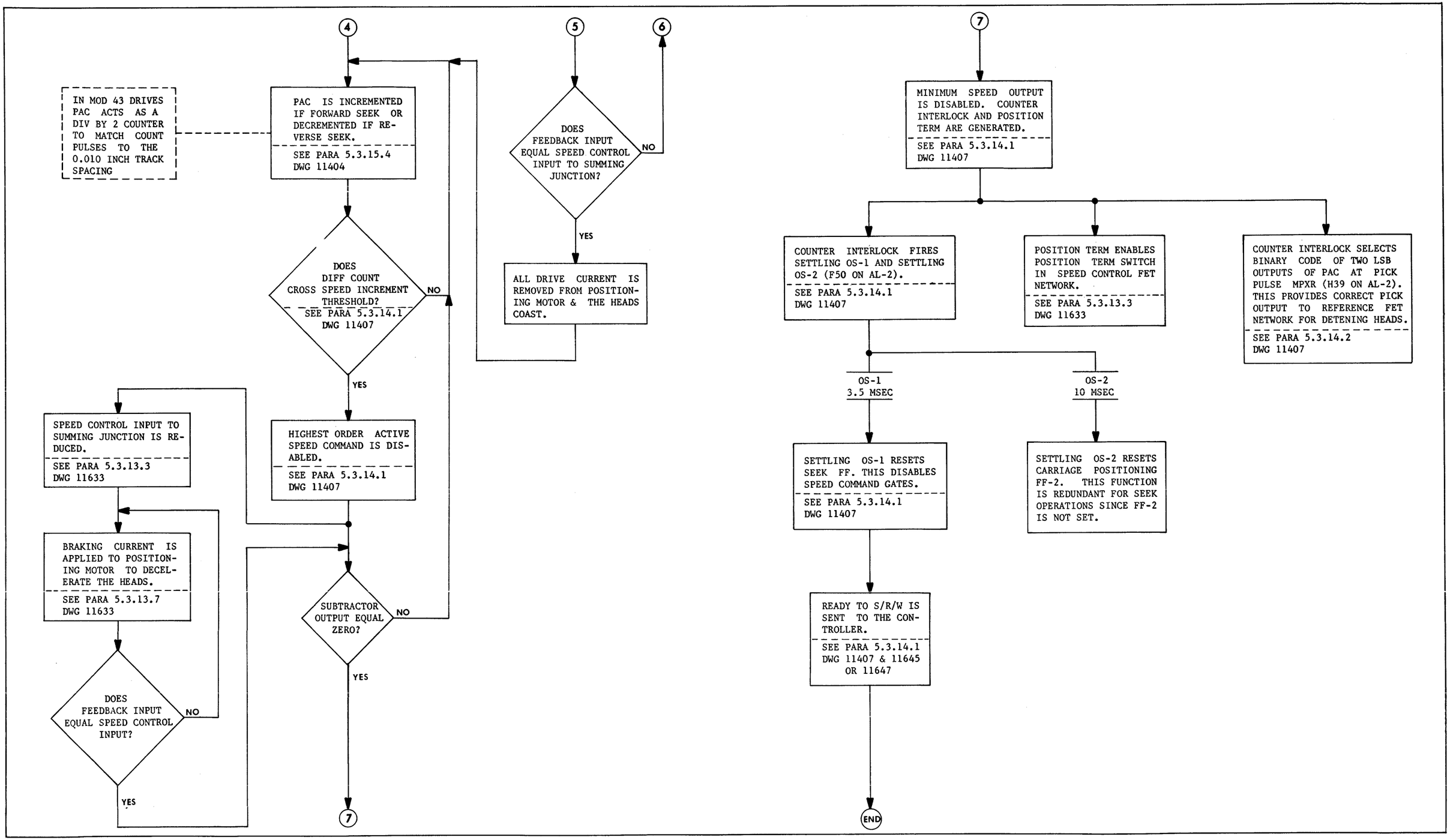


Figure 5-20.C Seek Operation Flow Chart

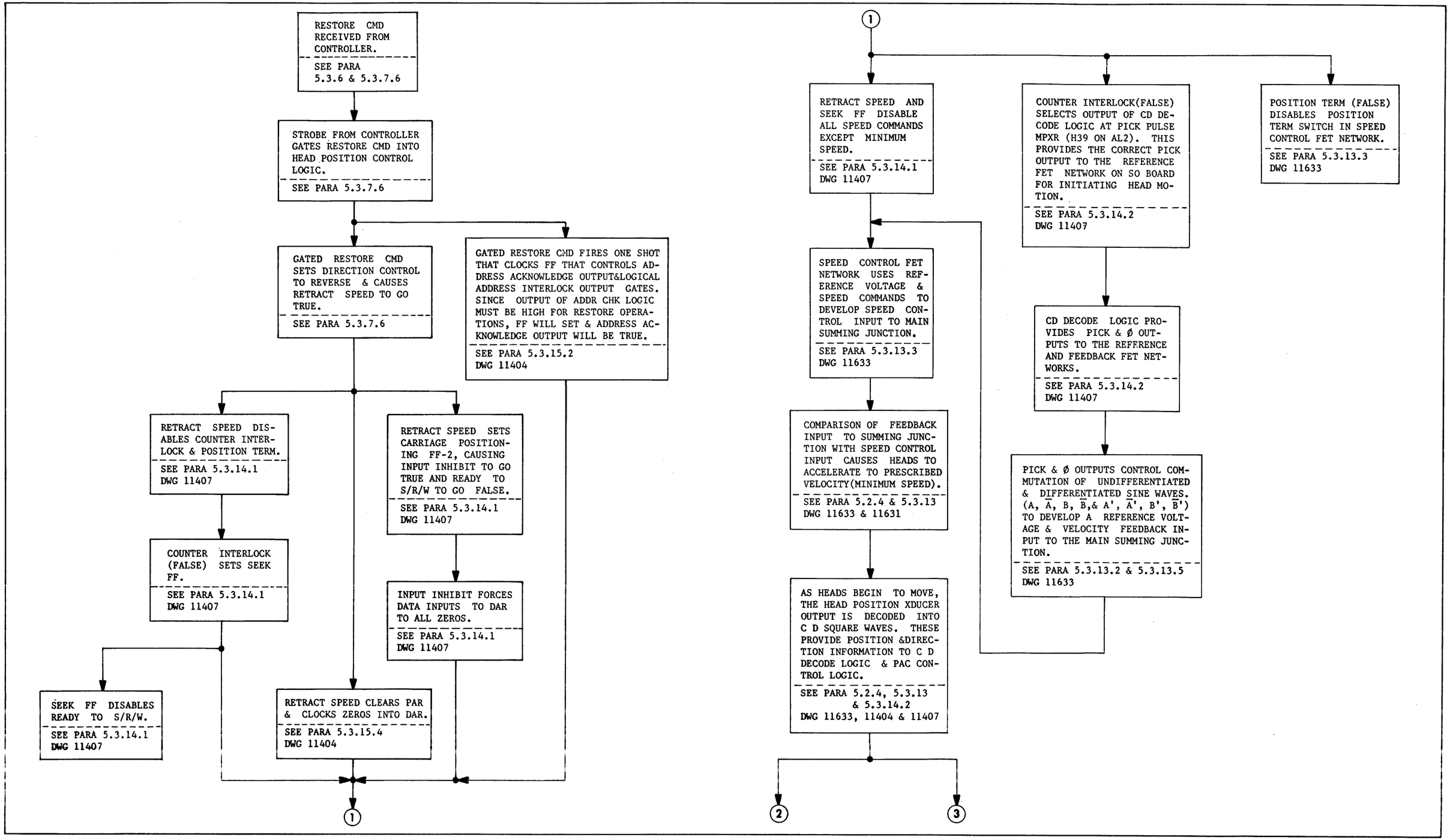


Figure 5-21.A Restore Operation Flow Chart

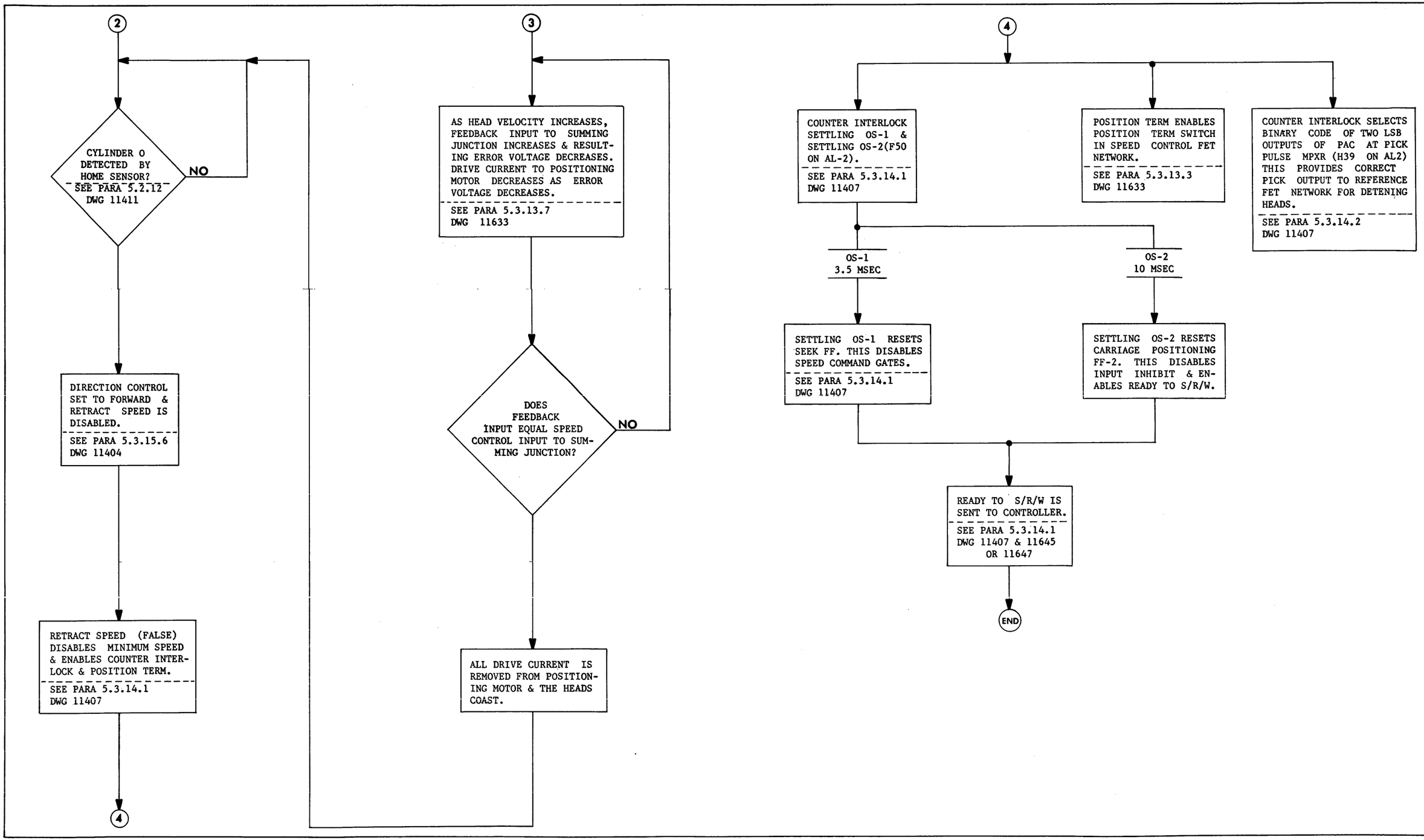


Figure 5-21.B Restore Operation Flow Chart

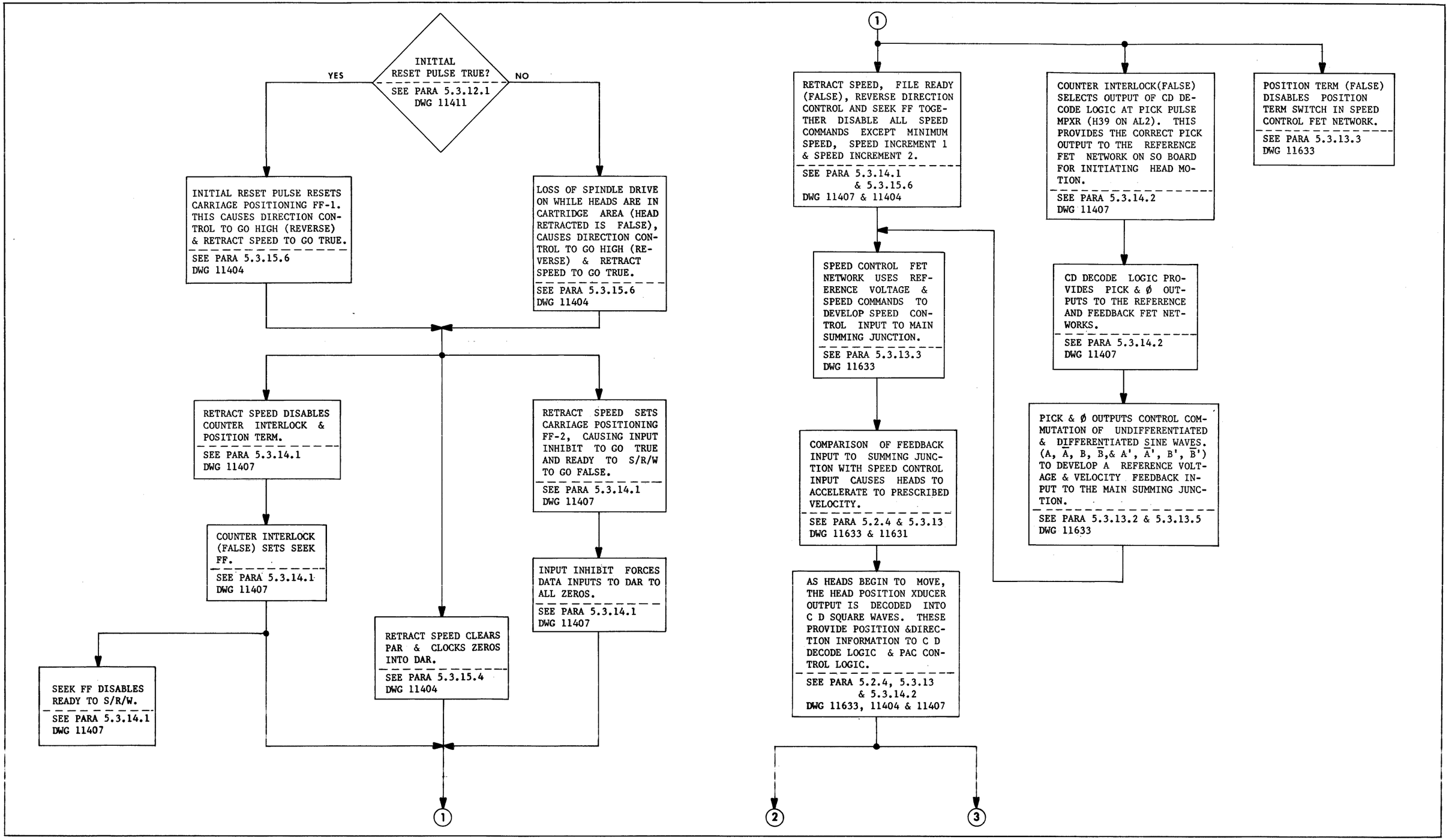


Figure 5-22.A Retrack Operation Flow Chart

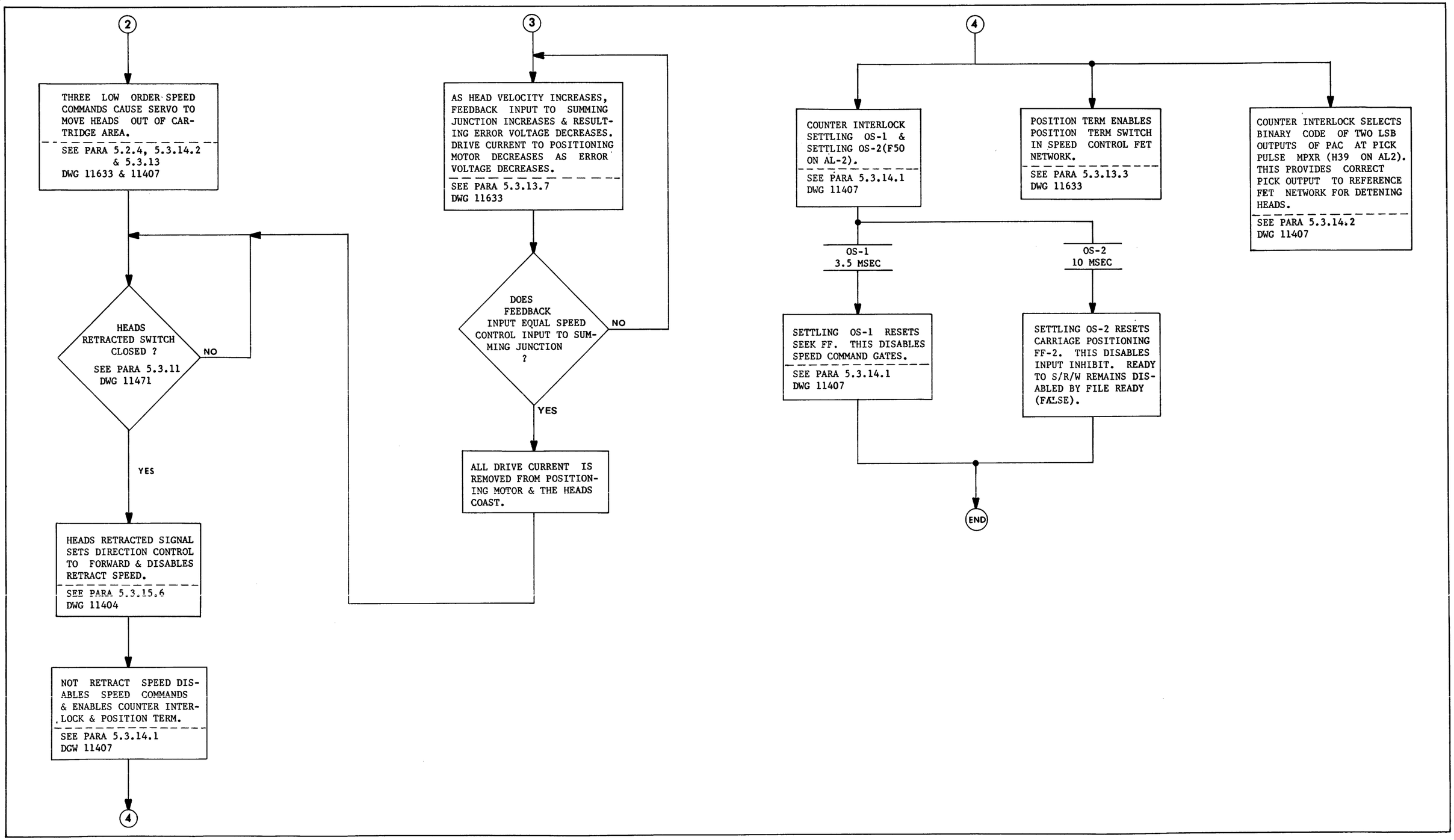


Figure 5-22.B Retrack Operation Flow Chart

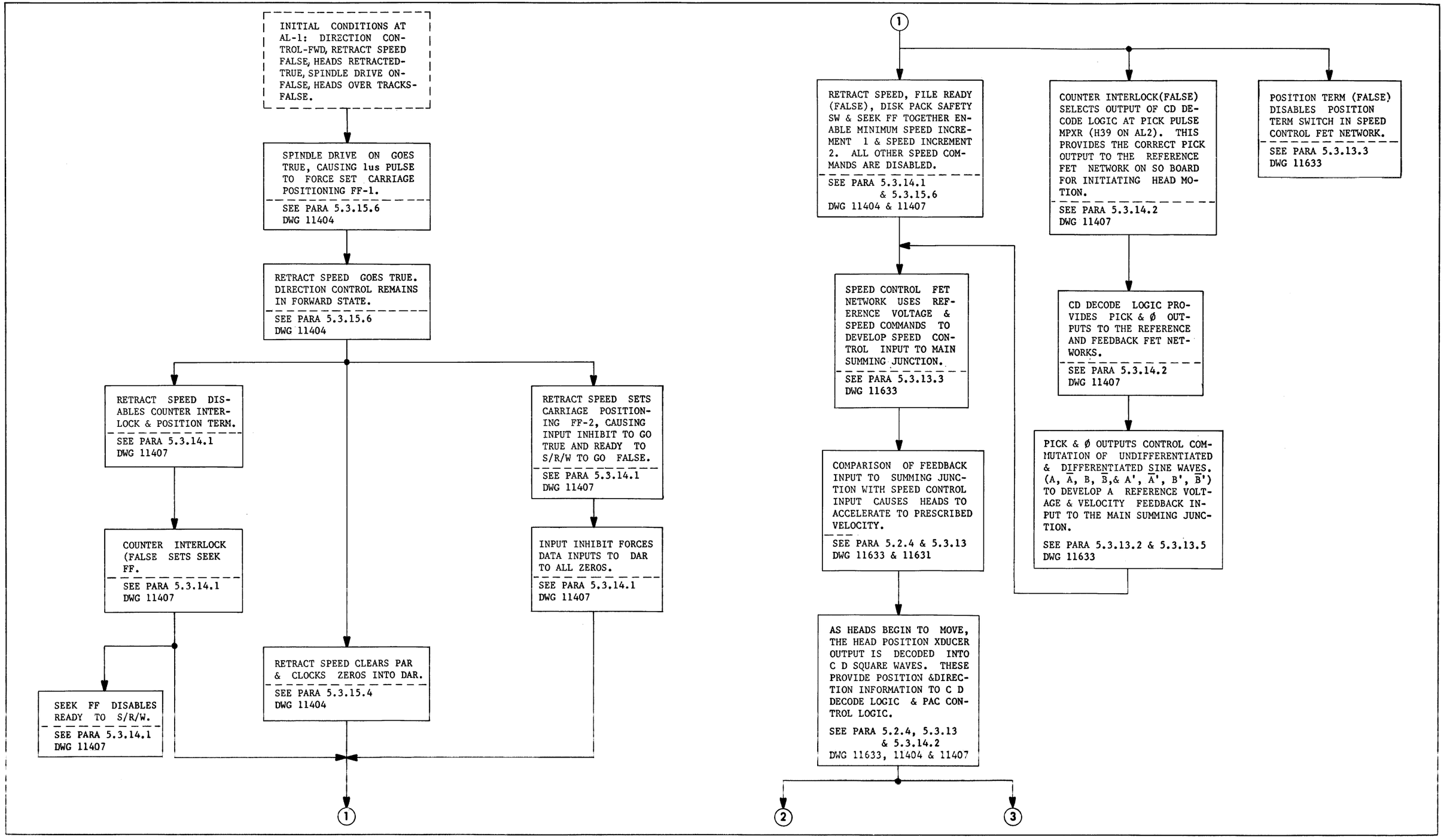


Figure 5-23.A Preload Head Advance Operation Flow Chart

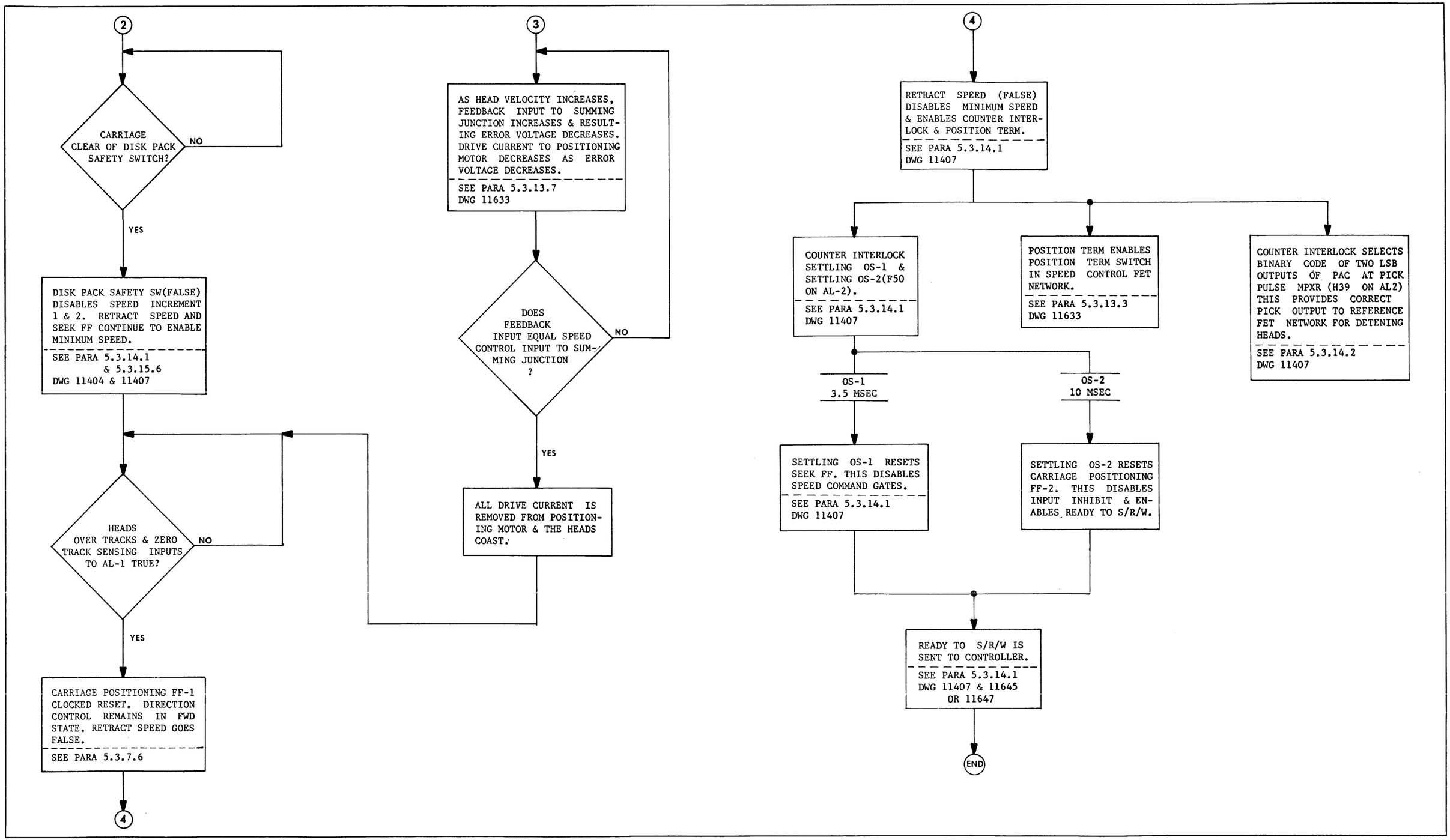


Figure 5-23.B Preload Head Advance Operation Flow Chart

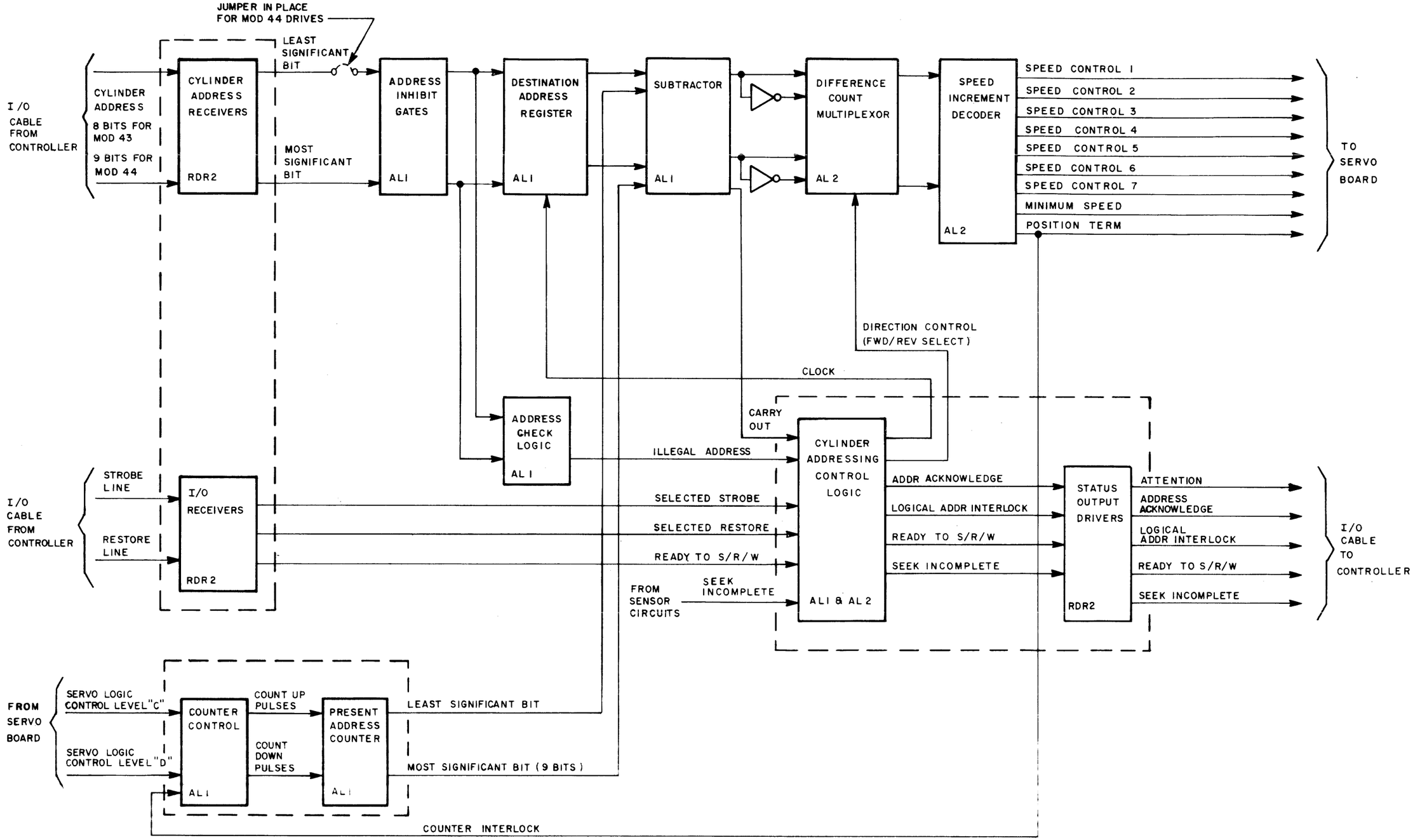


Figure 5-24. Head Positioning Control Logic Functional Block Diagram

The register consists of eight quad-D latches and a D-type flip-flop that stores the least significant address bit. In the Model 43 (100 tpi), the least significant address input is disabled.

5.2.5.5 Present Address Counter and Counter Control

The contents of this counter equal the address of the cylinder at which the heads are located whenever the heads are over the disks.

The counter consists of two four-bit binary counters and a JK flip-flop; the JK flip-flop represents the most significant address bit. Pulses for incrementing or decrementing the counter are provided by a pair of NAND gates in the counter control logic. One gate generates a count up pulse for each 0.005 inch the heads travel in a forward seek; the other gate generates count down pulses at the same intervals during reverse seeks.

The counter control logic develops these counter increment and decrement strobes from a pair of phase related pulse inputs, which are designated SERVO LOGIC CONTROL LEVEL "C" and SERVO LOGIC CONTROL LEVEL "D". These inputs are provided by logic on the Servo PCB.

The phase relationship of the "C" and "D" inputs is used by the counter control logic to determine when the read/write heads reach a new cylinder position as they travel across the disk surface. A network of NOR and NAND gates decodes the phase relationship of these position reference signals, providing a 1μs pulse for every 90°of head movement in either direction.

5.2.5.6 Subtractor

This functional element compares the contents of the Destination Address Register with the contents of the Present Address Counter. The result of this comparison represents the distance (in cylinders) the heads must move to reach the new address). The carry out term specifies the direction the heads must move. A logic 1 carry represents a reverse motion requirement.

If the carry out term indicates a forward seek, the difference count is represented by the true form of the Subtractor output. In a reverse seek, the complement of the difference count is represented at the subtractor output.

5.2.5.7 Difference Count Multiplexer

This logic multiplexes the true and complement forms of the Subtractor output. A direction control bit determines which form of the difference count will be used to develop speed increment commands.

If the direction bit specifies a forward seek, the set of true Subtractor outputs is gated through to the Speed Increment Decoder logic. If the direction bit specifies a reverse seek, the complemented Subtractor outputs are selected.

5.2.5.8 Speed Increment Decoder

This logic examines the selected Subtractor output and generates a set of speed increment commands, which are used by the Servo Logic to develop a drive signal for the head positioning motor.

These commands consist of two to eight signals. One of the eight commands, designated MINIMUM SPEED, is generated for any head positioning operation. For seek operations, one or more of the other seven commands is also issued; the number of commands generated for a given seek depends on the length of the seek (as represented by the value of the difference count).

MINIMUM SPEED is the sole speed command issued for restore operations. During head retract operations, MINIMUM SPEED and the second and third least significant speed commands move the heads back to the fully retracted position. These same three commands move the heads away from the fully retracted position toward cylinder 0. As soon as the carriage clears the Disk Pack Safety switch, the heads are moved by MINIMUM SPEED alone. This extra drive is required to compensate for special complications encountered by the head positioning system when the positioning motor coil is moving outside the main field of the motor's permanent magnet.

At the conclusion of any head positioning operation, the speed control portion of this logic is held disabled and the signal POSITION TERM is sent to the Servo. Position Term is used to detent the heads and hold them in position.

5.2.5.9 Cylinder Addressing Control and Interface Status Output Drivers

This set of logic performs a variety of control functions for the cylinder addressing logic. These control functions include the following:

- Strobes the new address into the Destination Address Register.
- Generates a DIRECTION CONTROL level, which serves as the select input to the Difference Count Multiplexor.
- Develops a RETRACK SPEED signal. This is the signal used to control head travel speed whenever the heads are moved to cylinder 0 or to their retracted position.
- Provides reverse speed control to the Servo after the initial reset period to hold the heads in the retracted position.
- Forces the outputs of the Address Inhibit Gates to the logical ZERO state whenever the heads are moved to cylinder 0 or whenever they are retracted.
- Provides status information to the controller regarding cylinder addressing conditions in the disk drive. This information includes: ADDRESS ACKNOWLEDGE, LOGICAL ADDRESS INTERLOCK, SEEK INCOMPLETE and READY TO SEEK/READ/WRITE. An output line indicating track density is also provided and, if the Attention option is used, an ATTENTION output is available to the controller from this logic.

5.2.6 Disk and Surface Select Logic

By use of the DISK SELECT and HEAD SELECT interface lines the system controller makes two selections on the standard Series 40. These selections are as follows:

1. Index Mark selection—the interface receives the index mark from whichever of the disks is selected.
2. Read/Write Head selection—one of the four heads is enabled for a read or write operation, while the other three heads are disabled.

The DISK SELECT signal also selects the disk whose Write Protect function is enabled, as described in 5.3.17.

Figure 5-25 is a simplified functional block diagram showing the selection logic. The output of the AND gate at "A" in the figure conditions either the upper or lower index mark NAND function ("B" or "C"), depending on which disk is selected by the controller. The selected index mark is thereby gated to the interface. Since the lower disk hub has sector slots as well as an index slot, the index mark must be separated from the sector marks prior to gating. If the upper disk also has sector slots, these are separated on the Sector Counter PCB, as explained in 5.3.2.

The R/W heads are enabled by removing a −1V level from the center tap of the selected head's winding. This is accomplished by furnishing a low to the appropriate Head Driver as shown in Figure 5-25. The output of the disk select AND gate at "A" conditions either the upper two NAND functions ("D" and "E") or the lower two ("F" and "G"), depending on which disk is selected by the controller. The output of the head select AND gate at "H" then selects which head of the selected disk is enabled.

5.2.7 Read/Write Circuits

One head is always enabled for reading or writing. In addition to enabling the selected head as described in 5.2.6, the head driver circuit places the selected head's centertap at +1V for reading or +23V for writing.

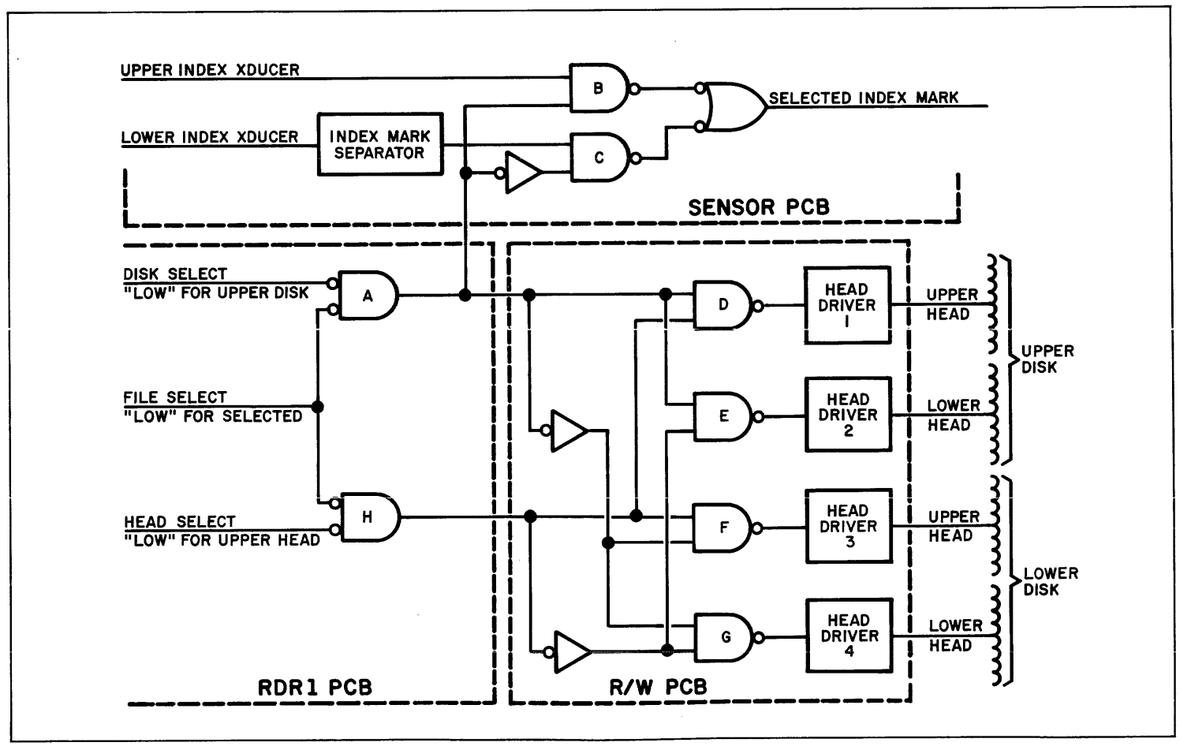


Figure 5-25. Disk and Surface Select Logic

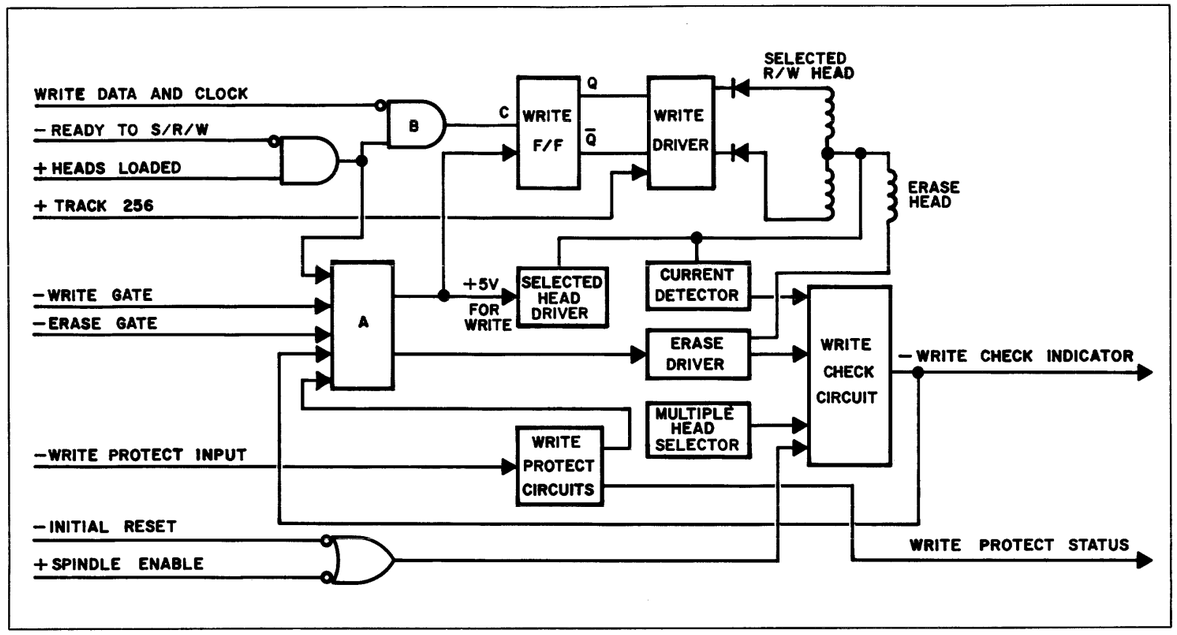


Figure 5-26. Write and Erase Block Diagram

5.2.7.1 Write Circuits

Figure 5-26 is a simplified functional block diagram of the write and erase circuits. When the gating circuits shown at "A" in the figure furnish +5V to the head driver, the driver places the center tap of the selected head at +23V for writing data. No input to the head driver places the center tap at +1V for reading data. Similarly, the gating circuits at "A" cause the Erase Driver circuit to conduct, allowing erase current to flow in the selected erase head. The head and erase drivers are turned on through the gates at "A" when the following conditions exist:

1. –WRITE GATE true
2. –ERASE GATE true
3. –WRITE CHECK false
4. Write protect not set
5. –READY TO SEEK, READ, OR WRITE true
6. Heads are loaded

The last two of these conditions also allow data and clock pulses to be gated through "B" to the Write F/F. When this F/F is conditioned by an input from the "A" gating circuits, each data or clock pulse clocks the Write F/F, driving the Write Driver. Each clock or data pulse, therefore, causes current to flow in alternate windings of the selected head, causing a flux reversal to be written on the disk for each data or clock pulse.

Referring to Figure 5-26, inputs to the Write Check circuits cause –WRITE CHECK to be true when any of the following conditions exist:

- Write current without a true WRITE GATE line or –ERASE GATE line.
- Write and select of more than one head.
- Erase current without a true –ERASE GATE line.
- –ERASE GATE line true without erase current.

5.2.7.2 Read Circuits

Figure 5-27 is a simplified functional block diagram of the read circuitry. In the absence of a true WRITE GATE and ERASE GATE, the selected head is enabled for reading. Each flux reversal on the disk surface represents one data or clock pulse. Each reversal induces a voltage pulse in the heading winding as it passes under the head. These voltages are applied to a buffer amplifier whose output drives a three-section read amplifier providing preamplification, equalization, and final amplification. The read amplifier output waveform is approximately symmetrical around the zero-volt level, and is applied to a zero-crossing detector. This detector is a one-shot multivibrator,

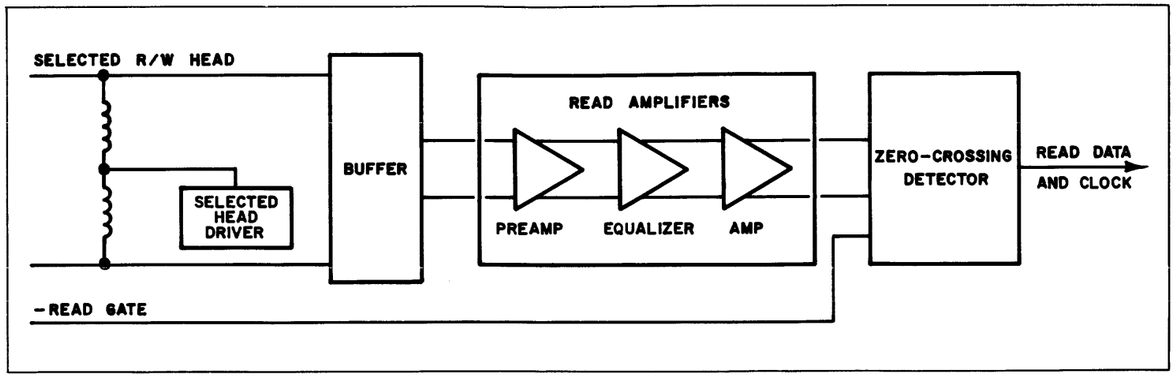


Figure 5-27. Read Circuitry Block Diagram

whose output is a square-wave pulse with a pulse width of approximately 100 ns. The one-shot is triggered each time the input crosses the zero level in either direction. An output pulse, therefore, occurs for each flux reversal on the disk surface under the selected head. Figure 4-8 shows this relationship. As shown in Figure 5-27, the output of the zero-crossing detector is enabled by the –READ GATE from the interface. Read Data and Read Clock pulses are then furnished to the Data/Clock Separator PCB in the Standard Series 40, or to the VFC PCB if the VFO option is installed, where the data pulses are separated from the clock pulses, and presented to the interface on separate lines. If the Data/Clock Separator PCB is used, the Unseparated Data Option is available, in which the data and clock pulses are not separated, but are both presented to the interface on the –READ DATA line.

5.2.7.3 Data/Clock Separation

Figure 5-28 shows the Data/Clock Separator block diagram and associated waveforms. This circuit is also referred to as the one-shot separator, to distinguish it from the VFO circuit which also separates data and clock pulses. Assuming that the +DATA/CLOCK GATE, which is derived from the –READ GATE line, has conditioned the NAND gates at "C" and "D", operation of the Data/Clock Separator is as follows:

Prior to arrival of the first data or clock pulse, the $\overline{Q}$ outputs of the one-shot multivibrators are high, as is the output of NAND gate "A". The output of NAND gate "E" is therefore low, which clears the Data Gate Trigger F/F. Its Q output is low, as shown by the waveform in Figure 5-28. Its $\overline{Q}$ output is high, conditioning NAND gate "B" for the arrival of the first pulse. For purposes of this description, the first pulse is assumed to be a clock pulse. It will be subsequently seen that if the first pulse is a data pulse, circuit action becomes the same as described within three pulses.

The positive-going edge of the first clock pulse, in addition to being gated to the interface by "B" and "D" is applied to the clock inputs of the one-shot multivibrators. The Long O/S is active, since there has been no low preset input to the Ones Trigger F/F. The Long O/S therefore times out, removing the low clear input to the Data Gate Trigger F/F. The trailing edge of the first clock pulse, inverted by NAND gate "B", clocks the Data Gate Trigger F/F. As shown by the waveform in Figure 5-28, the Q output conditions NAND gate "A" for receipt of a data pulse. If the bit cell contains a data pulse, the output of "A" goes low during the window. This is furnished to the interface as a data pulse, and also to the Preset input of the Ones Trigger F/F, making the Short O/S active and the Long O/S inactive. The absence of a pulse in the bit cell will keep the Long O/S the active one. When the active one-shot times out, the Data Gate Trigger F/F is reset through NAND gate "E". Table 5-1 shows times for the one-shot multivibrators. It can be seen that the Short O/S will close the window at "A" prior to receipt of a clock pulse following a data pulse.

Table 5-1.
Data/Clock Separator Timing

Item	2400 rpm	1500 rpm
Bit cell	400 ns	640 ns
Long O/S	290 ns	470 ns
Short O/S	280 ns	450 ns

5.2.8 Variable Frequency Oscillator (VFO)

The VFO Option is an alternative to the standard One-Shot Data/Clock Separator in that its primary purpose is also to separate the READ DATA pulses from the READ CLOCK pulses. The VFO accomplishes this separation by use of a highly stable phase-locked data window which is synchronized with the read data. This allows greater timing margins and provides immunity to missing clock bits for single-sector data format.

Figure 5-29 is a block diagram of the VFO, which consists of a Phase-Locked Loop and a Data Separator. The Phase-Locked

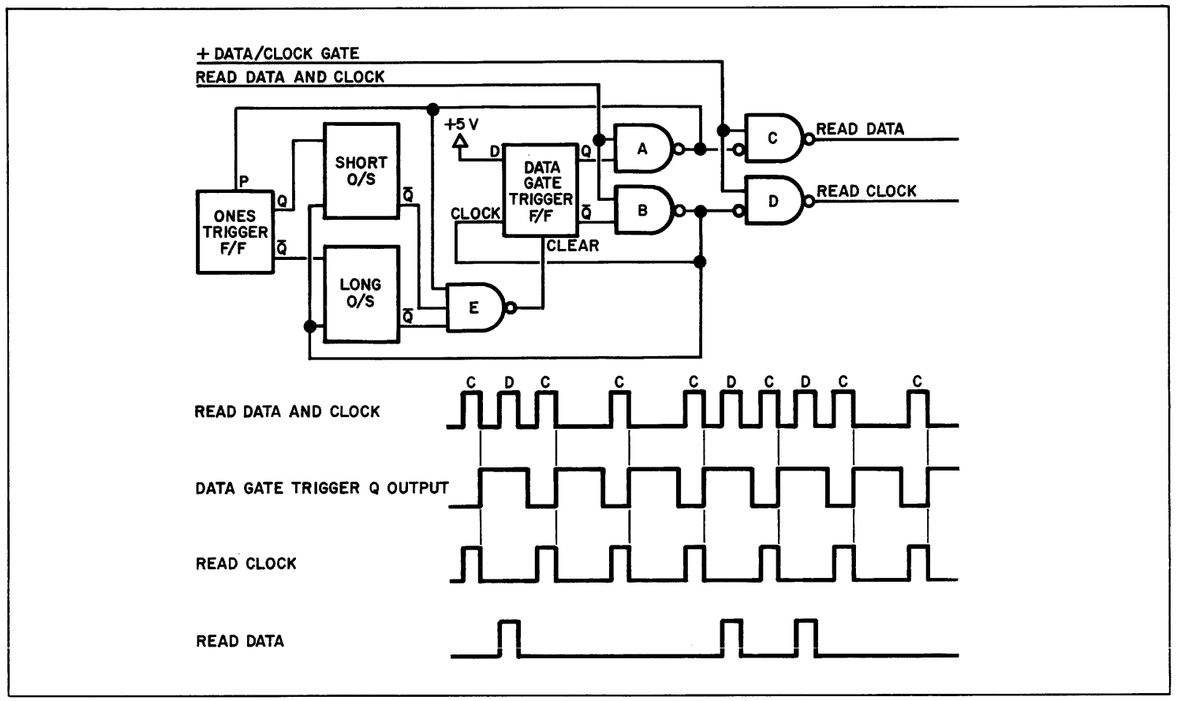


Figure 5-28. Data/Clock Separator Block Diagram

Loop includes a pulse slimmer, start-lock control circuit, high gain control circuit, Phase Comparator, filter, and a voltage-controlled oscillator (VCO).

The Phase Comparator consists of lead and lag detectors and a bi-directional current source. "Lead" or "lag" refers to the phase error of the read data or clock pulses with respect to the VCO 2F Clock output. "Lead" indicates that the data or clock pulses are of a higher frequency than the VCO clock, while "Lag" indicates a lower frequency. The BiDirectional Current Source furnishes an error signal to correct the frequency of the VCO Clock whenever lead or lag exists.

The Phase Comparator samples all bits coming from the disk, and does not distinguish between a data bit and a clock bit. Since sampling occurs only when bits are present, missing bits do not confuse the Phase Comparator. Missing clock pulses therefore do not disturb the VFO.

The filter and amplifier provide the proper low-frequency response required to minimize noise jitter and provide proper loop dynamics, such as damping factor, locking range, and locking time.

The VCO is a triangular wave VCO rather than the conventional ramp type. This design prevents high frequency noise and loop instability during ramp fly back. An RS flip-flop and voltage comparator circuit converts the triangular wave to the square wave VCO 2F Clock. The nominal frequency is 5.083 MHz (3.177 MHz for 1500 rpm drives).

The Data Separator separates the double frequency recorded pulses into data and clock bits. A data window is generated from the VCO output for separation of these bits.

A pulse slimmer is used to slim the incoming data and clock pulses to 15 ns pulses. This maximizes the Phase Comparators lock-in range.

In order to minimize phase lock time, the VFO is turned on and synchronized with the input pulses by the start-lock control circuitry. This insures phase lock within one bit-cell time. The remaining lock-in time is used to correct frequency. Turn on of the VFO is controlled by READ GATE. With READ GATE false, the VFO is turned off, and all outputs are quiescent. With READ GATE true, the VFO is turned on by the next input pulse. The separator is phased under the assumption the first bit is a clock bit.

The lock-in time and capture frequency depend on the bit rate of the input. In order to accommodate an all "ones" as well as an all "zeros" synchronizing pattern, a high-gain feature is provided. The high-gain control circuitry increases the total loop gain by a factor 5, thereby making the loop more sensitive to phase error and insuring frequency lock.

The Data Separator furnishes read data and read clock pulses which are highly stable and properly timed even if the input to the VFO is experiencing considerable jitter. Figure 5-30 shows waveforms which accomplish this separation. When the Phase-Locked Loop becomes phase locked to the data and clock pulses, these pulses will occur at approximately the positive peaks of the triangular waveform. By a system of voltage comparators and a flip-flop as part of the VCO circuitry, the triangular wave is converted into the 2F Clock square wave shown in Figure 5-30. The 2F Clock is sent to the Data Separator, where its positive-going edge triggers a flip-flop to produce the Data Gate. The Data Gate is inverted to produce the Clock Gate window. These two gates are logically ANDed with the input read data and clock pulses to generate Separated Clock and Separated Data pulses. At this point both the input and separated data can have excessive jitter, mainly due to pulse crowding. To eliminate this jitter, a clock latch and a data latch are set by the separated clock and data pulses, respectively, as shown in Figure 5-30. These latches are reset 1/4 bit-cell time later. Their outputs are logically ANDed with the stable 2F clock to provide the stable clock and data outputs of uniform width.

The VFO accommodates either a sectored format, in which case the Sector Counter Option is normally also used, or a single-sector format of the System 3 type. In the latter case, additional circuitry is required to handle the frequency synchronizing pattern consisting of all "ones". With this type of pattern the Data Separator may be phased incorrectly, since it cannot distinguish between a data bit and a clock bit. The additional circuitry is contained on the VFI PCB, and includes a "Zeros Detector". This detector corrects the phasing of the Data Separator, if necessary, by looking for eight consecutive zeros. When these zeros are found in the format, the VFI corrects the Data Separator phasing, and data is then gated out to the controller.

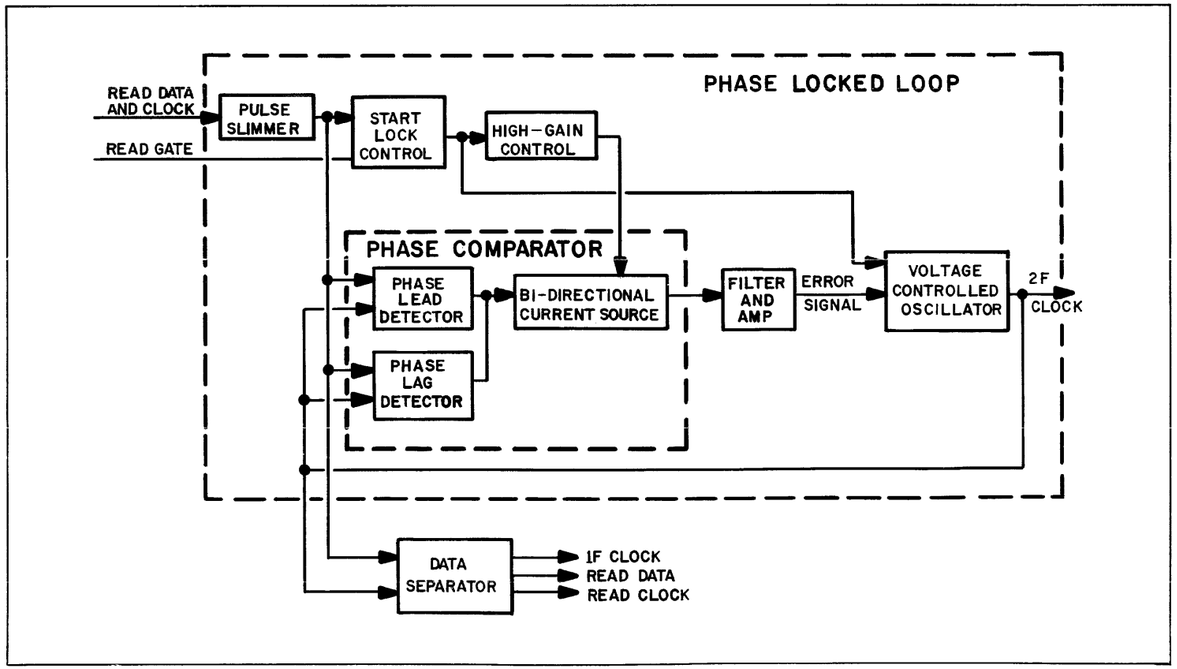


Figure 5-29. VFO Block Diagram

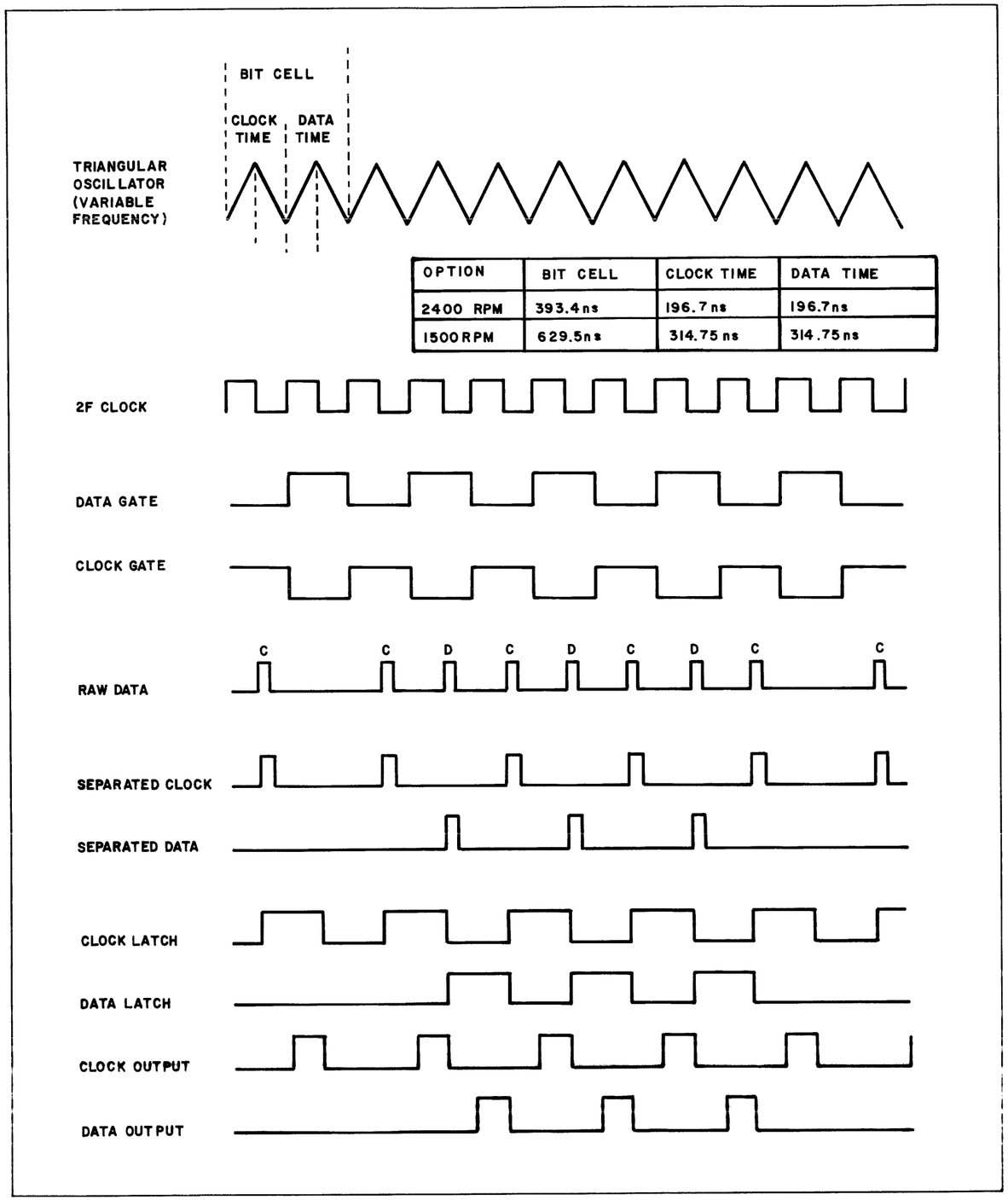
5.3 CIRCUIT BOARD DESCRIPTIONS

5.3.1 I/O-1, Receiver Driver Circuit 1 (RDR1) PCB

The RDR1 PCB contains the circuits necessary to accomplish the following:

- Receive the –FILE SELECT signal from the controller, and use this signal to gate all other interface signals, both input and output, which are received by, or sent from, the RDR1 PCB.

- Upon receipt of the –FILE SELECT signal from the controller, distribute the –SELECTED signal to the RDR2 and Sector Counter PCBs for gating signals to and from the controller. (Note: All interface signals except the +ATTENTION LINE are gated by the –FILE SELECT line.



OPTION	BIT CELL	CLOCK TIME	DATA TIME
2400 RPM	393.4ns	196.7ns	196.7ns
1500RPM	629.5ns	314.75ns	314.75ns

Figure 5-30. Sectored Format VFO Separator Timing

Additionally, many other functions within the Series 40 are enabled only on receipt of the –SELECTED signal from RDR1.)

- When selected, receive certain interface signals from the controller, including write data and clock, and furnish certain interface signals to the controller.

- If either a +WRITE FAULT or +VOLTAGE CHECK signal is received from the Read/Write Amplifier PCB, furnish a +WRITE CHECK to the RDR2 PCB to inhibit the READY TO S/R/W line, and furnish the –WRITE CHECK signal to the interface.

- If the Sector Counter Option is installed, receive the upper index and sector marks from the Sensor PCB, and use these marks to trigger a one-shot multivibrator which permits gating the sector and index pulses separately to the Sector Counter PCB.

The seven gated line receivers are type 8836 NOR gates connected functionally as negative logic AND gates as shown on the RDR1 schematic. They are gated by the –FILE SELECT line which also uses an 8836 as a receiver. The file select line is connected by a jumper on the I/O mother board to one of the four SELECT line pins on the interface connector, so that interface signals are gated to and from a particular Series 40 only when the SELECT line which is jumpered to RDR1 receives a low.

In cases where the outputs of the line receivers must be reinverted, type 380 NOR gates are used.

The circuits with inputs from the controller are simple gates and inverters, as shown on the RDR1 schematic. Circuits with outputs to the controller are also gated by the –FILE SELECT line. However in the case of the –INDEX MARK line, the –FILE READY signal is also necessary for gating the –INDEX MARK signal through A20-5.

If the Interrupt Option is installed, there is no connection at A5, and a 10Ω resistor is installed at A10. The –FILE READY line is therefore no longer gated by the –FILE SELECT signal from the controller. With the Interrupt Option installed without the Sector Counter Option, a 10Ω resistor is installed at D10, so that index marks can be gated by the –FILE SELECT signal.

With no Sector Counter Option installed, index marks of the selected disk are gated to the interface through F15-13 and A20-5. The outputs to the Sector Counter PCB, pins X and J, serve no function if there is no Sector Counter PCB installed.

If the disk drive has the Sector Counter Option installed, combined index and sector marks from the upper disk are received from the Sensor PCB on pin R of the RDR1 PCB, and the jumper at E22 in the –INDEX MARK output line is removed.

Index marks and sector marks are gated through F15-13, and are applied to NAND gates at B15-2 and B15-5. For purposes of this description, assume the first pulse to be a sector pulse. The one-shot multivibrator at F3 is in its stable state, with its Q output low and its $\overline{Q}$ output high. The $\overline{Q}$ output therefore has conditioned NAND gate B15-4 for the receipt of a pulse, and B15-1 is disabled. The arriving sector pulse is gated through B 15-6, inverted at B 15-8, and is sent to the Sector Counter PCB where it advances the sector counter as described in 5.3.2. The pulse at B15-6 also fires the one-shot multivibrator, which has a period of approximately 850 μs. Therefore, B15-1 is now enabled and B15-4 is disabled. If a pulse arrives during this 850 μs period, it must be an index pulse, since sector marks are at least 1 ms apart (1.04 ms for 24 sectors, 2400 rpm). The index pulse will be gated to the Sector Counter PCB via the –UPPER INDEX PULSE line, where it will reset the sector counter. At the end of the 850 μs period, the one-shot will recondition B15-4 for the arrival of the next sector pulse.

5.3.2 I/O-3, Sector Counter (SC) PCB

The purpose of the Sector Counter Option is to provide the interface with an absolute binary signal which continuously indicates the current sector location of the selected head. Sector and index marks from both disks are furnished to the Sector Counter PCB, which contains a counter for each disk. As each sector mark occurs, its counter is advanced one count, except that the first sector mark after the index mark resets the counter. The outputs of both upper and lower sector mark counters are furnished to a two-section multiplexer. By means of the DISK SELECT line, the controller gates the counter output of the desired disk out of the multiplexer. The multiplexer also receives the sector marks and index marks of each disk directly. The DISK SELECT line also gates these out of the multiplexer for the desired disk.

The following description pertains to the upper sector-mark counter. Operation of the lower sector-mark counter is identical.

The upper sector-mark counter circuit consists of a four-bit binary counter at D15, an upper reset F/F at F3-5, an upper bit-16 F/F at H15-5, and associated gates and inverters. The type 7493 counter is connected as a four-bit ripple-through counter, with the counter input at pin 14, and reset inputs at pins 2 and 3. The binary output counts up with each input pulse at pin 14. The fifth bit of the sector address is provided by the upper bit-16 F/F at H15-5, which is toggled by the bit-8 output of the counter when it goes low at the next count after a binary count of 01111. For reset simultaneous highs must exist at both reset pins of the binary counter.

Assume that the next pulse to be received is the –UPPER INDEX PULSE. This pulse is applied to the preset input of the reset F/F at F3-4, resulting in a high Q output. This high is applied to one reset input of the upper counter. At the trailing edge of the index pulse, the preset input at F3-4 again goes high,

enabling the F/F to toggle at the next positive going pulse at the clock input.

When the next sector mark occurs, it is applied to the counter at D15-2 directly, and to the clock input of the F/F at F3-3 after inversion. The reset F/F does not toggle on the leading edge of the sector pulse, because a type 7474 F/F toggles on positive-going edges. Therefore the Q output is still high when the +UPPER SECTOR PULSE is applied to the other reset input to the counter at D13-2. The counter resets to zero. Note that the two high reset signals that are applied to the counter are also applied to the bit-16 F/F through NAND gate J15-3, resetting Q output (the bit-16 output) to zero. On the trailing edge of the sector mark, the reset F/F is toggled, and its Q output removes the high reset from the counter's pin 3.

Each succeeding sector mark is applied to the counter input, advancing the output one count. When the bit-8 output at pin 11 of the counter goes high at count 01000, the clock input to the bit-16 F/F goes low. This has no effect since the F/F toggles only on positive going clock inputs. At this time the $\overline{Q}$ output, preset input, and clear input are all high, so that the Q output will go high when the next positive-going clock is applied. This occurs when the count goes from 01111 to 10000, and pin 11 of the counter goes low. This sets the bit-16 F/F whose Q output is applied to the multiplexer. Counting continues until the next index-mark/sector-mark sequence occurs, at which time the counter and the bit-16 F/F are reset as previously described.

The lower sector counter operation is identical to that of the upper. The outputs of the upper sector counter are applied to the "A" inputs to the multiplexers at B15 and E15, while the lower sector counter outputs are applied to the "B" multiplexer inputs. When the "select" inputs to the multiplexers are low, the "A" inputs are gated to the outputs. High "select" inputs gate the "B" inputs out. This is accomplished by an inversion of the DISK SELECT signal from the interface.

A combination of –SELECTED from the interface and –FILE READY OUTPUT from the Read/Write PCB gates the index mark, sector mark, and sector count to the interface.

As described in 5.3.12, the Sensor PCB requires the separated sector marks of both disks. The lower index and sector marks are separated on the Sensor PCB itself. The separation for the upper disk occurs on the RDR1 PCB, and the sector marks are furnished to the Sensor PCB via pin Y of the Sector Counter PCB interface.

5.3.3 I/O-4, Variable Frequency Sector (VFS) PCB and Variable Frequency Interface (VFI) PCB

With the VFO Option installed in the Series 40, Slot I/O-4 holds either the VFS PCB or the VFI PCB. The VFS PCB is installed if a sector-mark format is to be used, while the VFI is used with the single-sector format.

As shown on the VFS schematic, the purpose of the VFS PCB is merely to conduct data and clock pulses from the VFC PCB to the interface connector, and to provide a constant +5V to the –SET PHASE input to the VFC PCB, as described in 5.3.5.3.

The purpose of the VFI PCB is to

- detect a field of eight consecutive data zeros to determine if the data separator on the VFC PCB has properly identified which file data pulses are clock pulses and which are data pulses.
- issue a –SET PHASE signal to the data separator if it has improperly identified data and clock pulses,
- shift the data pulses so that the leading edge of a "one" read data pulse is coincident with the trailing edge of the previous clock pulse, and
- gate read data and read clock pulses to the interface.

The zeros detector consists of two type 7493 four-bit binary counters and associated gates and flip-flops. The counters are connected with the "A" output feeding the "B" input, so that a straight count from zero to 15 is achieved. The counter at E15 is advanced by the –READ DATA pulses and reset to zero by the –READ CLOCK pulses. Conversely, the counter at F3 is advanced by –READ CLOCK pulses and reset to zero by –READ DATA pulses. Prior to receipt of data or clock pulses, the +START OSC line is low, as described in 5.3.5. Therefore the three flip-flops F15-5, F15-9, and A3-5 are conditioned as shown in Table 5-2.

Table 5-2.
VFI Initial Conditions

Pin	F15-5	F15-9	A3-5
Preset	H	H	L
Clear	L	L	H
J	L	L	L
K	L	L	L
Q	L	–	H
$\overline{Q}$	H	H	L

When the VFC PCB receives the second file data pulse (data or clock) the +START OSC input to the VFI PCB goes high, making both clear and preset inputs to the flip-flops of Table 5-2 high, thereby conditioning them for the receipt of clock inputs. All three flip-flops get their clock input from the –2F REF or –F REF signals.

Both counters are maintained in the reset to zero condition through E3-3 and E3-2 until +START OSC goes high, at which time the counters are enabled. Assume that file data consists of a series of logical ones, i.e., alternate clock and data pulses. Each counter will alternately count to one and then be reset. This will continue until a field of data zeros is encountered, at which time one of the counters will be continuously reset and the other will count up. However, since the data separator cannot distinguish between data and clock pulses with the single-sector format, the count up of clock pulses could occur on either counter. For purposes of this description, assume that the data separator is out of phase, and that the clock pulses are therefore arriving on the –READ DATA line. Counter F3 will be reset with each pulse while E15 will count up. At the eighth clock pulse, pin 11 of the counter will go high (binary 1000), placing a high on the J input of F/F F15-5. At the next positive-going edge of the –2F REF signal, F15-5 will toggle, placing a high on pin 10 of NAND gate E3-8. Since the Q output of F/F A3-5 is already high, the –2F REF pulse will be gated through E3-9, setting the phase of the data separator correctly. Meanwhile, the $\overline{Q}$ output at F15-6 has placed a high at A3-2, so that the next –2F REF signal will toggle A3-5. This locks out further –SET PHASE signals and resets both counters. As A3-5 goes low, A3-6 goes high, enabling NAND gates D3-5 and D3-3 for the gating of –READ DATA and –READ CLK signals through to the interface.

If the data separator is correctly phased when the field of zeros starts, counter F3 will count up while E15 will be continuously reset. At a count of 8, F3-11 will go high. At the next positive-going edge of the –2F REF signal, the $\overline{Q}$ output at F15-7 will go low. This low is gated through B15-6, so that at the next negative-going edge of –2F REF, F/F A3-5 is toggled. As previously described, E3-8 will now be disabled on pin 11 (as well as on pin 10), and D3-5 and D3-3 will be enabled.

The four JK flip-flops at A15 and B3, together with NAND gates B15-8 and B15-11, constitute a standard shift-register which in effect delays each clock pulse by +1F REF, resulting in a time coincidence of the leading edge of a data "one" and the trailing edge of the previous clock pulse.

5.3.4 I/O-5, Data/Clock Separator (D/CS) PCB

The D/CS PCB is used in the Series 40 disk drive when the VFO Option is not installed. This PCB accepts unseparated read data and read clock pulses, separates the data and clock pulses, and, when the –READ GATE signal is received from the controller, gates the data and clock pulses to the interface.

The Data/Clock separator consists of a data gate trigger F/F at F15-5, a ones Trigger F/F at F15-9, a Short one-shot multivibrator at B3, a Long one-shot multivibrator at D15, and associated gates and circuitry. The period of the one-shot multivibrators varies between 2400 rpm disk drives and 1500 rpm disk drives. The following discussion assumes a 2400 rpm disk drive. For a 1500 rpm disk drive, see the D/CS schematic for multivibrator periods.

Prior to arrival of the first –READ DATA AND CLOCK pulse, the low output of OR gate H15-8 disables NAND H15-6, H15-3, E15-6, and E15-12. The outputs of these four gates are therefore high. The $\overline{Q}$ outputs of the multivibrators are also high. The output of the NAND gate at E15-8 is therefore low which clears the data gate trigger F/F at F15-1. The Q and $\overline{Q}$ outputs of this F/F are low and high, respectively. The high $\overline{Q}$ output conditions the NAND gate at H15-2 so that the next data or clock pulse will be gated. The outputs of the Ones Trigger F/F enable the Long O/S and disable the Short O/S. Assume that +DATA/CLOCK GATE is high, conditioning E15-4 and E15-1. These initial conditions are summarized in Table 5-3.

Table 5-3.
Data/Clock Separator Initial Conditions

	Data Gate Trigger F/F	Ones Trigger F/F	Short O/S	Long O/S
Preset	H	H	–	–
Clear	L	H	–	–
D	H	L	–	–
Clock	H	H	H	H
Gate	–	–	L	H
Q	L	L	–	–
$\overline{Q}$	H	H	H	H

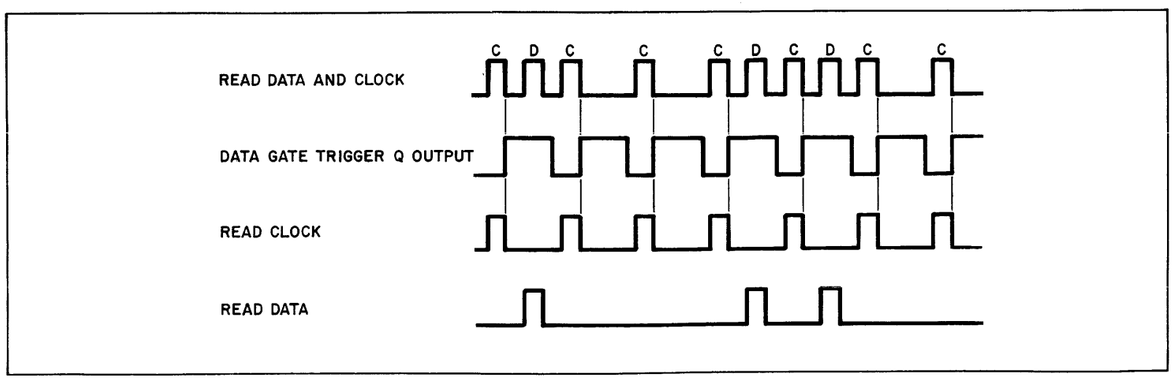


Figure 5-31. Data/Clock Separator Timing

For purposes of this description, assume that the first pulse is a clock pulse. It can be seen that if the first pulse is a data pulse, circuit action becomes the same as described within three pulses. Figure 5-31 shows timing relationships.

The leading edge of the first clock pulse is gated through E15-2 to the read-clock half of the 75450 line driver, which furnishes a −READ CLOCK pulse to the interface. It is also gated through H15-3 to the clock inputs of the data gate trigger F/F and both multivibrators. The data gate trigger F/F does not set at this time, since it toggles on positive going clocks. The Long O/S, being enabled previously by the $\overline{Q}$ output of the Ones Trigger F/F, is clocked, and its $\overline{Q}$ output goes low for approximately 290 ns. This low is applied to the NAND gate at E15-9, whose output now places a high on the clear input at F15-1. This F/F can now be set by its next clock input. This occurs at the trailing edge of the first clock pulse. As shown in Figure 5-31, the Q output at F15-5 goes high. Pins 4 and 5 of NAND gate E15 are now high, so that an incoming data pulse at pin 3 would be gated through to the interface.

The Long O/S times out after 290 ns, prior to the receipt of another clock pulse. If there was no data pulse in the bit cell, the Data/Clock Separator returns to its initial conditions as shown in Table 5-3, and awaits another clock pulse. If there was a data pulse in the bit cell, this pulse, in addition to being gated to the interface, places a low on the preset input to the Ones Trigger F/F. This enables the Short O/S and disables the Long O/S, so that the next pulse at H15-3 will result in a 280 ns high at the clear input of F15-1, rather than a 290 ns high. It can be seen that the Short O/S would close the data window prior to receipt of a clock pulse following a data pulse.

5.3.5 I/O-5, Variable Frequency Comparator (VFC) PCB

The VFC PCB is used on Series 40 disk drives having the VFO Option installed. Referring to Figure 5-29, the VFC PCB contains the Phase Comparator, Start-Lock Control, Pulse Slimmer, and High-Gain Control circuits of the Phase-Locked Loop, as well as the Data Separator circuits. Specifically, the VFC PCB contains the circuits necessary to accomplish the following:

- Turn on and synchronize the VCO with the file data pulses
- Increase the gain of the Phase-Locked Loop during the first 20 ms of a read operation
- Compare the frequency of the file data with that of the VCO 2F CLOCK pulses, and generate error signals if the frequencies differ
- Separate the read data pulses from the read clock pulses, and furnish stable read data and clock pulses of uniform width to the interface.

5.3.5.1 Start-Lock Control and High-Gain Control

The Start-Lock Control and High-Gain Control circuits ensure that the VCO starts in phase-lock synchronization with the file data pulses, that frequency correction occurs within 20 ms of the first file data pulse, and that no read data or clock pulses can be gated to the interface until after the 20 ms frequency correction period has elapsed.

Referring to the VFC schematic, the Start-Lock Control circuit consists of JK F/F F3-5, one-shot multivibrator J15, Start F/F H15-6/8, and associated circuitry.

When power is applied to the unit, the low +DATA/CLOCK GT at F3-15 resets F/F F3-5. When the controller makes the READ GATE true, +DATA/CLOCK GT goes high, enabling the F/F to be set by the trailing edge of the first file data pulse.

When F3-5 receives the first file data pulse, its Q output conditions the Start F/F at H15-4 so that when the second file data pulse is gated through NAND gate H15-11, the Start F/F will be set. The first file data pulse is not gated through H15-11 because the Q output of F3-5 does not become high until the trailing edge of the first data pulse. Since the K input at F3-2 is grounded, the F/F will remain set until the controller makes the READ GATE false.

When the second file data pulse sets the Start F/F, its outputs furnish +OSC START and −OSC START. The +OSC START signal goes to the VFI PCB, is used, where it enables the counters to start count-up as described in 5.3.3. The −OSC START signal is furnished to the VFO PCB, where it turns the VCO on. Since the Start F/F is set by a file data pulse it is here that the synchronization of the VCO with the second file data pulse occurs; the VCO starts coincident with a file data pulse, as described in 5.3.6.

As previously explained, the trailing edge of the first file data pulse sets F/F F3-5. Its $\overline{Q}$ output triggers the 20 ms one-shot multivibrator J15. Its output, the −HI GAIN signal, goes low. This is sent to the VFO PCB where it increases the gain of the Phase-Locked Loop by a factor of about five for 20 ms as described in 5.3.6. This allows frequency correction to be accomplished within 20 ms. The output of the 20 ms one-shot also is applied to JK F/F F3-12, keeping its $\overline{Q}$ output low for the first 20 ms of VFO operation. This prevents the separated −READ DATA and −READ CLK pulses from being gated through to the interface until after frequency correction has been accomplished.

5.3.5.2 Phase Comparator

The Phase Comparator compares the time of occurrence of each file data pulse with the negative-going edge of the 2F REF clock signal, and issues a lead or lag error signal if the file data pulse arrives early (lead) or late (lag). The error signals are sent to the VFO PCB where they adjust the frequency of the VCO as described in 5.3.6.

The Phase Comparator consists of a pulse slimmer circuit, a Lead-Latch F/F, a Lag-Latch F/F, and associated circuitry.

The pulse slimmer narrows the file data pulses to about 15 ns, and includes four inverting amplifiers at H3, an RC network, and NAND gate H15-3. Between pulses, capacitor J6 charges to approximately 4.5V. An incoming file data pulse results in a high at pin 1 of NAND gate H15 and a low at H3-4. However, NAND gate H15 will gate the first part of the pulse through until capacitor J6 discharges to below the threshold level of the NAND gate. This results in a file data output pulse of about 15 ns at H15-3.

The Lead Latch F/F consists of A15-3 and A3-6. At the beginning of a read operation, the F/F is reset at A3-3 when the second file data pulse sets the Start F/F. After that the Lead-Latch F/F is set by the file data pulse at A15-2 and reset by −2F REF at A3-4. If the low file data pulse arrives at A15-2 while −2F REF is high, the F/F is reset and the −LEAD ERR will go low. If there is no lead error, −2F REF will hold A3-4 low and A3-6 high even during a file data pulse at A15-2.

The Lag Latch F/F consists of A15-8 and A15-6. It is set by file data pulses and is automatically reset after a delay of approximately 160 ns, which is one-half the period of −2F REF. This delay is initiated when the +LAG LT signal is sent to the VFO PCB, as explained in 5.3.6. At the end of the delay, the −RST LAG LT signal from the VFO PCB resets the Lag Latch F/F at A15-10. Any lag error signal must be gated through A3-8, whose inputs are the inverted reset output of the Lag Latch F/F, −2F REF, and the −LEAD ERR signal. When the file data pulse sets the Lag Latch F/F, A3-10 is conditioned so that if −2F REF goes high prior to the end of the delay period, a −LAG ERR signal will be gated to the VFO PCB. If there is no lag error, the −RST LAG LT will reset the F/F prior to a high −2F REF signal. The −LEAD ERR input to the NAND gate at A3-9 is necessary to prevent a large lead error from appearing as a lag error to the Lag Latch F/F.

5.3.5.3 Data Separator

The Data Separator consists of divide-by-two JK F/F E3-9, a data latch at E15-8 and D15-8, a clock latch at D15-3/6, and associated gates.

Once the Phase-Locked Loop is phase locked to the file data pulses, these pulses will occur at the negative-going edges of the +2F REF signal. Clock pulses will occur every other +2F REF cycle. Data pulses will also occur every other +2F REF cycle (in the case of ones), but between the clock pulses. The clock and data pulses are separated by applying the file data pulses to two NAND gates at H15-13 and H15-2, and applying a data window to one of the NAND gates and a clock window to the other NAND gate, the two windows being 180° out of phase. The data and clock windows are generated by divide-by-two F/F E3-9. Normally both the preset and clear inputs are high. The clear input is high when the second file data pulse sets JK F/F F3-5. The preset input at E3-10 comes from the VFS or VFI PCB, whichever is in use. The VFS PCB holds E3-10 high at all times. The VFI PCB holds E3-10 high except when the VFI determines that it has clock pulses and data pulses confused, as described in 5.3.3, at which time it applies a low pulse to E3-10, toggling the F/F. With highs on both preset and clear, E3-9 is connected to toggle on the negative-going edge of each +2F REF pulse. Although the Q output at E3-9 divides the +2F REF frequency by two, the signal is modified by the −DATA GT INHIBIT signal at D3-10. As explained in 5.3.6, the −DATA GT INHIBIT signal is a negative pulse of about 100 ns duration, which is centered in time at the negative peaks of the VCO output. Therefore, the other input to the NAND gate at D3-10 is low during the first 50 ns of the high output from E3-9. This results in the positive half of the square wave at D3-8 being about 50% wider than the negative half. The positive half will be the clock window as it is applied to E15-1. The wider clock window is required because clock pulses can move more than data pulses.

The output at D3-8 is applied to E15-1 as the clock window. Its inversion is applied to E15-12 as the data window. With file data being applied to E15-13 and E15-2, the output of E15-11 is separated data pulses, and the output of E15-3 is separated clock pulses. The data pulses are applied to a data latch at E15-8 and D15-8, while the clock pulses are applied to a clock latch at D15-3/6. The data latch and the clock latch are set by the separated data and clock pulses, respectively, but their outputs are not gated through B15 pins 6 and 12 until approximately 1/2 bit time later by the stable −2F REF pulse which enables the three-input NAND gates at B15-2 and B15-3. Jitter can cause a variation in the time the latches are set prior to the positive-going edge of −2 REF pulse, but since this −2F REF signal gates the latch outputs, the signals to the PCB interface are stable and of uniform width. Figure 5-32 shows data separator timing.

5.3.6 I/O-6, Variable Frequency Oscillator (VFO) PCB

The VFO PCB contains the circuitry necessary to accomplish the following:

- Generate the triangular wave. This is accomplished by the voltage-controlled oscillator (VCO).
- Convert the VCO output to the 2F REF square wave (VCO Clock).
- Receive, filter, and amplify the lead or lag error signal from the comparator.
- Apply the lead or lag error signal to the VCO to correct the VCO frequency.
- Generate the −RST LAG LT signal to reset the lag latch in the phase comparator.
- Generate the −DATA GT INHIBIT signal.

Figure 5-33 shows the VCO in block diagram form. A bi-directional current source, shown as +I and −I, is used to charge a capacitor with constant current first in one direction and

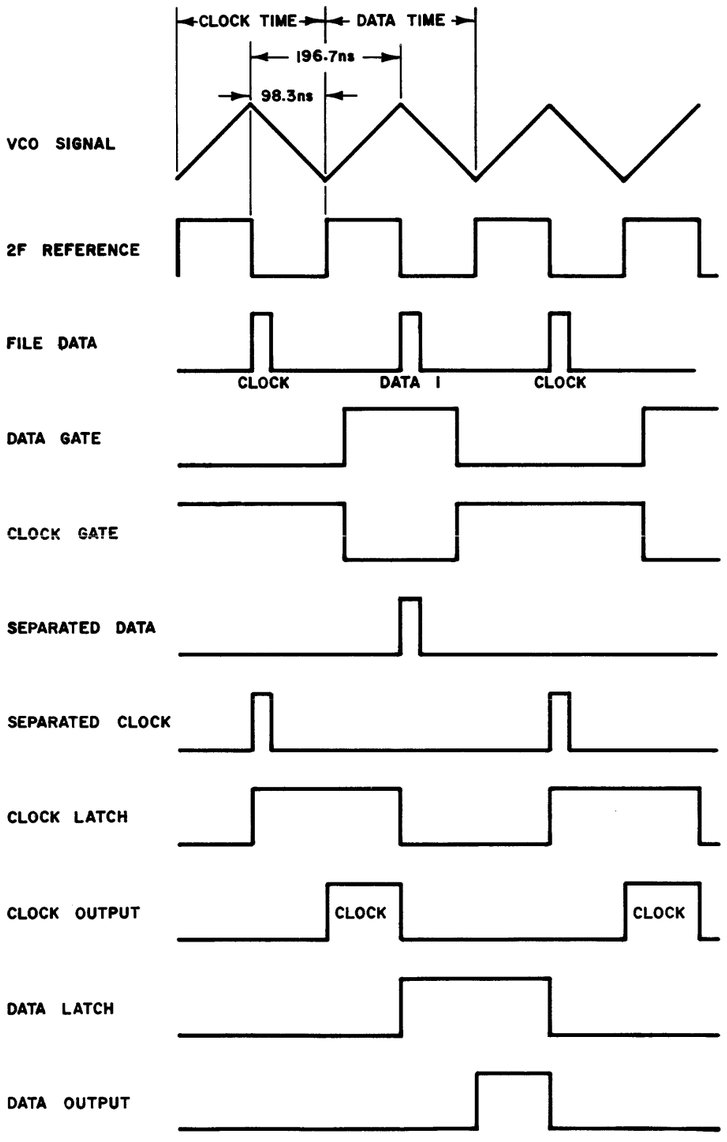


Figure 5-32. Data Separator Timing

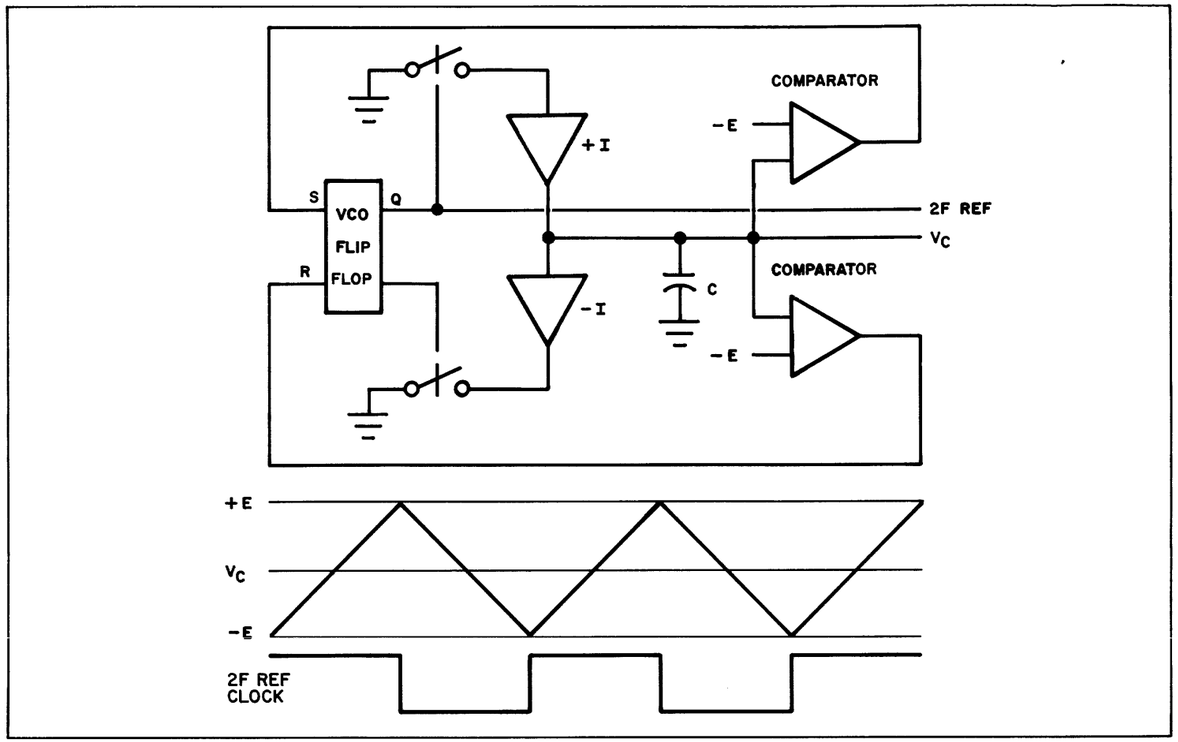


Figure 5-33. VCO Block Diagram

then in the other, resulting in a triangular waveform across the capacitor. Each comparator is triggered when the voltage across the capacitor reaches the comparator's reference level, −E or +E. Upon triggering of a comparator, the VCO F/F is set or reset, depending on which comparator has triggered. Each time the F/F is toggled, the direction of current flow through the capacitor is reversed. A square wave of the same frequency as the triangular wave is available at the output of the F/F as the 2F REF signal.

Referring to the VFO schematic, the bi-directional current source consists of transistors D22, D21, D23, F20 and F22. The capacitor across which the triangular wave is generated is F16. The −E comparator consists of transistors J21 and J22, while transistors J16 and J17 form the +E comparator. These comparators are differential amplifiers, with the reference voltages being determined by a voltage divider consisting of precision resistors at K21, K13, K20 and K12. The voltage divider provides an accurate reference for all comparators on the VFO PCB. Therefore, any drift in voltage affects all comparators uniformly, cancelling out any effort. The VCO F/F consists of two negative logic OR gates at H6-6/8.

Transistor D22 is the reference current source, which adjusts the magnitude of the current through capacitor F16, and, therefore, the frequency of the triangular waveform. An error voltage from the Phase Comparator is applied to the base of D22 as explained later. This error voltage, together with emitter resistors B23 and B22, determine the current magnitude at any given time. Transistors D23, D21, F20, and F22 constitute the current switch, with D23 being the current source transistor and the other three acting as sinks. D21 and D23 act as switches controlled by the H6-6/8 F/F. Transistors F20 and F22 provide the bi-directionality of the current through capacitor F16. With D21 cut off and D23 conducting, F20 and F22 are cut off, allowing a positive current flow through capacitor F16. The triangular waveform across the capacitor is applied to the base of emitter follower H23, whose output is applied to J21 of the differential amplifier comparator. When the signal reaches the reference amplitude, H6-6 of the F/F goes low, causing D21 and D23 to change states. With D21 conducting and D23 cut off, F20 and F22 are conducting. Since the base to emitter voltages are closely matched, the current through F20 will be matched by an equal current through F22. Therefore, F22 collector current will flow through F16 in the reverse direction. For purposes of this description, this current is considered negative. As with the positive half cycle, the output of the emitter follower H23 is applied to the input of the comparators at J16 and J21. The F/F is toggled by the low at H6-9 when the signal at the base of J16 reaches the reference level.

−2F REF and +2 REF are taken from the F/F and furnished to the VFC and, in the case of −2F REF, to the VFI. As described in 5.2.8, these signals are used to produce stable clock and data pulses.

The operation of the VCO is initiated by the −OSC START signal applied to the base of F3. This signal originates in the Start-Lock Control circuit on the VFC PCB, and occurs when the second data or clock pulse is received on the VFC as described in 5.3.5. Proper phase synchronization within one data or clock bit is provided by transistor F3. When −OSC start goes high, F3 conducts, placing the base of D21 at approximately 5V. D21 cuts off, insuring that the triangular waveform across capacitor F16 always starts in the positive direction.

As previously mentioned, the magnitude of capacitor F16's charging current is controlled by transistor D22, whose collector current is controlled, in turn, by the error signal applied to the base. This error signal originates on the VFC PCB as described in 5.3.5. Referring to the VFO schematic, the lead or lag error signal is applied to the base of transistor B5 and A6, respectively. Transistors B5, B8, A6, and A8 constitute a current switch which determines whether capacitor B13 charges through A6 or discharges through A8. As will be seen, the charging or discharging of capacitor B13 determines the polarity of the error signal applied to the base of the current reference transistor D22. During the 20 ms high-gain period described in 5.3.5, the input to the base of transistor B6 causes it to conduct. This effectively places its emitter resistor D7 in parallel with the current switch resistor A7, increasing the current through B13 by a factor of approximately 5 during the time any error signal is present. This greatly increases the sensitivity of the VCO to error signals during the first 20 ms, and frequency correction is more rapidly accomplished. After initial lock-on, the VCO tracks easily without the high-gain feature. Transistor D5 merely acts as a clamping diode.

The lead or lag error signals applied to B5 or A6 of the current switch are narrow pulses, whose width is proportional to the magnitude of the phase error between the 2F REF signal and the incoming data or clock bits. Therefore, the charge or discharge time of capacitor B13 is proportional to the phase error.

The combination of B13, B11, and A5 constitutes a filter. Transistors A12, A17, and A22 amplify and shift the level of the error signal applied to the base of A12 by the current through B13. The amplifier has a gain of approximately 3.

At the emitter of A22, the error signal is a voltage level which varies around a nominal +2.8V in accordance with the lead or lag error. This error signal is applied to the base of D22. It is also applied to the base of D20. Transistors D20, D14, D16, D12, and D15 constitute a current source and switch for charging and discharging capacitor D17 in much the same manner as the VCO charged and discharged capacitor F16. Since the emitter resistor of D12 is significantly different from the emitter resistor of D15, the signal at the emitter of F6 will not have equally sloping edges, and will be flattened, as shown on the schematic. The −RST LAG LT signal at the collector of F6 resets the lag latch F/F as described in 5.3.5.2.

The −DATA GT INHIBIT signal is generated by transistors at J11 and J12. Transistor J11 is cut off during the negative peaks of the VCO output. This causes J12 to be driven rapidly into saturation, resulting in the negative pulse on the collector of J12.

5.3.7 I/O-2, Receiver/Driver Circuit 2 (RDR2) PCB

The circuits on this PCB fall into two general categories: 1) line receivers, which condition cylinder address information and two of the commands received from the controller and 2) line drivers and associated logic, which provide information to the controller about cylinder addressing activities in the disk drive.

5.3.7.1 Line Receivers

Nine gated line receivers buffer the cylinder address present on the I/O cable when the disk drive is selected and the heads are loaded over the disks. Two other gated line receivers on this PCB accept −STROBE LINE and −RESTORE LINE pulses issued by the controller.

All 11 line receivers are gated by the ANDing of −SELECTED and +HEAD LOADED. This AND function is provided by F3-3, E3-3 and F3-13. −SELECTED originates at the controller as −SELECT LINE X(X=1, 2, 3 or 4) and is propagated to RDR2 by way of RDR1. +HEADS LOADED is generated by SL logic when the heads are loaded into flying position over their disks; this occurs just after the sensor circuits detect that the heads are over the disk surface. The circuit that produces +HEADS LOADED is described in Section 5.3.11.

The line receivers are 8836 type NOR gates. The high-true levels at their outputs are inverted back to low-true levels by 380 type NOR gates. These low-true outputs are applied to the Address Inhibit Gates on AL1 (see Sheet 2 of AL1 diagram).

The ninth (and least significant) address receiver gate has no logic function in Model 43 disk drives, since that line is not continuous through the cylinder addressing logic.

5.3.7.2 Line Drivers

−ADDRESS ACKNOWLEDGE LINE is a 1 μs pulse that notifies the controller that the requested seek has begun. This pulse is generated by NANDing −ADDRESS ACKNOWLEDGE OUTPUT (inverted by F15-8) with the high level present at E3-3. E3-3 is enabled by −SELECTED and +HEAD LOADED.

−ADDRESS ACKNOWLEDGE OUTPUT is the gated Q output of a D-type flip-flop on AL1. This flip-flop sets at the beginning of a seek if the Address Check logic determines that the address received from the controller is valid. The leading edge of −ADDRESS ACKNOWLEDGE OUTPUT, which is gated by a one-shot on AL1, occurs approximately 500 ns after the leading edge of −STROBE is received. The circuit that produces −ADDRESS ACKNOWLEDGE OUTPUT is described in Section 5.3.15.

If the Address Check logic rejects the cylinder address provided by the controller, RDR2 responds with −LOGICAL ADDRESS INTERLOCK instead of −ADDRESS ACKNOWLEDGE Line. In this case, the high level at E3-3 gates the set output of R/S flip-flop F15-6/H15-8. This flip-flop is set by −LOGICAL ADDRESS INTERLOCK OUTPUT.

−LOGICAL ADDRESS INTERLOCK OUTPUT originates as the gated $\overline{Q}$ output of the D-type flip-flop on AL1 that produces −ADDRESS ACKNOWLEDGE OUTPUT. This flip-flop is reset by the Address Check logic if the address provided by the controller exceeds the legal address. The leading edge of −LOGICAL ADDRESS INTERLOCK OUTPUT is gated by a one-shot approximately 450 ns after −STROBE arrives at the drive interface.

--LOGICAL ADDRESS INTERLOCK OUTPUT is also NANDed by H15-6 on RDR2 with a high level on −ADDRESS ACKNOWLEDGE OUTPUT and −READY TO S/R/W OUTPUT (inverted by F15-3). −READY TO S/R/W OUTPUT is the result of NANDing four conditions on AL2. These conditions are −SEEK INCOMPLETE (NOT), +FILE READY, the reset state of the Seek FF and the reset state of the Carriage Positioning FF-2. The generation of −READY TO S/R/W OUTPUT is described in Section 5.3.14.

The low level at H15-6 enables H15-12. H15-12 is inverted twice (by F15-11 and D16-3) to result in +ATTENTION LINE. +ATTENTION LINE is available at pin 10 of RDR2 if the Attention option is implemented.

−READY TO S/R/W LINE informs the controller that the drive is in the File Ready condition and that a seek is not in progress. This output is generated by D16-5.

One input to D16-5 is provided by J15-4, which is enabled by −READY TO S/R/W OUTPUT and +WRITE CHECK (NOT). +WRITE CHECK is low if no write fault is detected by the R/W logic and if no voltage check occurs.

The other input to D16-5 is provided by either E3-3 or J15-10, depending on whether or not the Series 30 Compatibility Interrupt option is used. If the Interrupt option is not used, jumper B20* is in place and jumper B21 is not. This causes −READY TO S/R/W LINE to be a function of −SELECT. If the Interrupt option is in use, B21 is substituted for B20*. This allows −READY TO S/R/W LINE to be generated whether or not the drive is selected.

−SEEK INCOMPLETE LINE notifies the controller that the drive was unable to successfully reach the addressed cylinder. This output is generated in the same manner as −READY TO S/R/W LINE, except for its origin as −SEEK INCOMPLETE OUTPUT. −SEEK INCOMPLETE OUTPUT is generated by SR logic, which is described in Section 5.3.12.

The −200 TRACKS PER INCH output is made available to the controller by this PCB in Model 44 disk drives. This output results from ANDing +HEADS LOADED (inverted) with −SELECTED. The AND function is provided by F3-3, E3-3, and A16-5. −200 TRACKS PER INCH identifies the disk drive as a Model 44; use of this output is intended for applications where the system includes a mix of Model 43 and Model 44 disk drives.

5.3.8 M/O-1, Spindle Drive (SD) PCB

The Spindle Drive PCB contains the circuitry necessary to accomplish the following:

- unlock the equipment drawer when all necessary interlock conditions have been met
- control rotation of the Spindle Drive Motor, including dynamic braking.

5.3.8.1 Drawer Unlock

On the standard Series 40 disk drive, the drawer unlock solenoid cannot be energized unless all of the following conditions exist:

1. The brushes and heads are fully retracted, producing a −UNLOCK DRAWER signal at the input to the Spindle Drive PCB.
2. The LOAD/RUN switch is in the LOAD position, removing the +SPINDLE DRIVE ON signal.
3. Spindle rotation has stopped, resulting in no input to the speed sense amplifier. This produces a low at Speed Sense F/F H15-4, resetting the F/F.
4. The −INITIAL RESET line is high, indicating that the disk drive supply voltages are in tolerance.

When all of these four conditions exist, all inputs to NAND gate H39-6 are high. The low output from this NAND gate, −DRAWER UNLOCK ENABLE, is supplied to the Heat Sink PCB through Spindle Drive interface pin 2, where it causes the drawer unlock drive transistor to conduct. This places 24V across the drawer unlock solenoid in series with a 30Ω resistor. This is sufficient to keep the solenoid energized, but it is pulled in by bypassing the 30Ω resistor for 700 ms, allowing increased current through the solenoid.

Bypassing the 30Ω resistor is done by the +DRAWER INTERLOCK PICK signal. When the four interlock conditions previously listed were met and H39-6 went low, one-shot multivibrator A39

*320 is the designator used for this jumper on Model 44 drives (RDR2 drawing 11647).
In Model 43 drives (RDR2 drawing 11645), this jumper is designated D21.

was triggered through A27-3. The period of this one-shot is 700 ms. Its output is fed through NAND gate A27-6, and it causes transistor A13 to cut off. The high signal on the collector is supplied to the Heat Sink PCB where it is used to short out the 30Ω resistor for 700 ms.

Referring to the Spindle Drive PCB schematic, NAND gate H39-6 does not drive the OR gate at A27-3 on disk drives with the Desk Top Interlock Option installed. Rather, the drawer unlock signal comes from H51-8 through a jumper installed at E56 instead of E48.

5.3.8.2 Spindle Control

In the following description, reference to 80 Hz signals applies to 2400 rpm drives. For 1500 rpm drives, the frequency is 50 Hz.

5.3.8.2.1 Start-up

For purposes of this description consider that the disk drive is in the LOAD mode, with the spindle stopped. The +SPINDLE DRIVE ON signal from the Sequence Logic PCB is low. This low is inverted three times through F15-3, A27-8, and B27-10, causing a high on the base of the transistor at J17. The transistor conducts, and the PHASE 2B and PHASE 2A lines are effectively grounded through diodes at D21 and D31. Similarly, the PHASE 1B and PHASE 1A lines are grounded by transistor J21 conducting. The high on the base of J21 is obtained by a high output of NAND gate H15-11 which in turn is caused by a low on H15-3. Both inputs to OR gate H15-3 are high, since the low +SPINDLE DRIVE ON signal is inverted by F15-11. The resulting high is applied to H15-1 and also resets the Speed Sense F/F at H15-6 placing a high on H15-2 also.

When the LOAD/RUN switch is set to the RUN position, +SPINDLE DRIVE ON goes high. Since –INITIAL RESET is already high, the +SPINDLE DRIVE ON signal is gated through F15-3, A27-8 and B27-10 to remove the ground from the outputs of the Phase 2 amplifiers. The +SPINDLE DRIVE ON signal is also gated through F15-11, H15-3, H15-11, and B27-11 to remove the ground from the outputs of the Phase 1 amplifiers. In addition to ungrounding the amplifier outputs, the +SPINDLE DRIVE ON gates the 80 Hz drive signals to the amplifier inputs. The 80 Hz Phase 2 square wave from the Oscillator PCB is gated through F27-3, inverted at F39-4, and applied to the Op Amp at E39-2. The output of the NAND gate at F27-3 is also inverted at F27-6, reinverted at F39-2, and applied to the Op Amp at E39-6. Since the square wave at E39-6 has experienced one more inversion than the signal at E39-2, the two inputs (and hence the outputs) are 180° out of phase. These Phase 2 amplifiers drive power amplifiers on the Heat Sink Assembly which, in turn, drive the Phase 2 winding of the spindle drive motor.

The 80 Hz Phase 1 square wave is also furnished to Op Amps as two signals 180° out of phase. However, since the Phase 1 winding of the motor is also used for dynamic braking, gating of the Phase 1 square wave is different than that of Phase 2. The +SPINDLE DRIVE ON signal, after being inverted at F15-3, is applied to the clear inputs of the Phase 1 flip-flops, J39-5 and J39-9. The low Q output at J39-9 drives H39-10 high. The pin 12/13 input to this NAND gate also went high when the +SPINDLE DRIVE ON signal was inverted at F15-11 and gated through H15-3. The 80 Hz Phase 1 square wave applied to H39-9 is gated through H39-8 and F27-11. Phase splitting is accomplished in the same manner as for Phase 2. The spindle drive motor now has both windings driven, and is coming up to rated speed. When it is within 50% of rated speed, the +SPEED OK signal is generated on the Sequence Logic PCB as described in 5.3.11. This is applied to a NAND gate at F15-9 on the Spindle Drive PCB, where it is NANDed with the +SPINDLE DRIVE ON signal. The output at F15-8, after inversion at B27-3, is applied to the base of a transistor at A5, causing the transistor to conduct. The collector is placed effectively at ground. This fires a triac on the Heat Sink Assembly, bypassing two resistors in series with the Phase 1 winding of the motor. The resistors in series with the Phase 2 winding are similarly bypassed by a low on the base of the transistor at A9 on the Spindle Drive PCB. With these four resistors bypassed, the spindle drive motor comes up to rated speed. The output of the Speed Sense Op Amp at H8-7 is high, which has reset the Speed Sense F/F (H15-6 low, A27-11 high).

5.3.8.2.2 Spindle Motor Braking

When the LOAD/RUN switch is set to the LOAD position, the spindle drive motor is braked to a stop in approximately 15 seconds. This is accomplished by grounding the Phase 2 winding and passing a DC current through the Phase 1 winding.

Referring to the Spindle Drive PCB schematic, the +SPINDLE DRIVE ON signal goes low when the LOAD/RUN switch is set to the LOAD position. This has the immediate effect of turning off the full-current transistors A5 and A9, and blocking the drive to the Phase 2 amplifiers by means of lows on F27-2 and F27-5. This grounds the Phase 2 amplifier outputs through a high on B27-10. The inputs to the Op Amps at E39-6 and E39-2 are low.

Drive to the Phase 1 Op Amps is not immediately removed. When +SPINDLE DRIVE ON went low, a high was applied through F15-3 to the clear inputs of the Phase 1 flip-flops at J39, allowing them to toggle with the next clock input (Phase 1 drive) from the Oscillator PCB. The F/Fs count two Phase 1 pulses and then remove the low from H15-9. Since H15-10 is also high, NAND gate H39-10 is disabled by the low on pin 10, and no further 80 Hz drive reaches the Phase 1 amplifiers. Delaying Phase 1 turn-off for two cycles is necessary to insure that the triacs are off before dynamic braking starts. With H39-8 high, F27-11 is held high, resulting in a low input to pin 2 of the Phase 1A amplifier. The low on pin 2 sets the output on pin 1 high. The input to the Phase 1B amplifier is kept high at this time through Speed Sense F/F H15-6, OR gate H15-3, NAND gate H15-11, and NAND gate F27-8. The high on D39-6 drives the output at pin 7 low, and a DC braking current is passed through phase 1 of the spindle drive motor. It should be noted that the outputs of the Phase 1 amplifiers are not yet grounded, since transistor J21 is still held cut off by the output of the Speed Sense F/F at H15-6.

As the spindle drive motor stops, the voltage between the SPEED SENSE B AND SPEED SENSE A inputs to the PCB drops to zero. At this point the Speed Sense F/F is set by a low input at H15-4. The high at H15-2 causes the input to the Phase 1B amplifier to go low and transistor J21 to ground the amplifier outputs.

5.3.9A M/O-2, Oscillator (OR) PCB No. 11414

The purpose of the Oscillator PCB is to furnish the stable square waves of several frequencies for use in other Series 40 circuits. Specifically, the frequencies and uses are as follows:

- 480 kHz to drive the carriage position transducer.
- 480 kHz for demodulation of the carriage position transducer output.
- 60 Hz for the brush motor.
- 80 Hz, 2 phases, for the spindle drive motor (50 Hz for 1500 rpm disk drives).

The frequency determining element on the Oscillator PCB is a 1.92 MHz crystal-controlled oscillator, consisting of the crystal, two NOR gates at A15-2 and A15-3, and associated circuitry. The oscillator oscillates as long as power is applied to the Series 40. The oscillator output is applied to a divide-by-four circuit consisting of two D-type flip-flops at B15-5 and B15-9. The 480 kHz output is inverted at B4-8, and applied to the carriage position transducer driver. It is also supplied to the Servo PCB, where it is used to demodulate the position transducer output.

Elsewhere in this manual, the frequency of the Phase 1 and Phase 2 spindle drive motor power has been specified as approximately 80 Hz for 2400 rpm disk drives and approximately 50 Hz for 1500 rpm disk drives. These are the synchronous frequencies for the drive motor if no slip were present. However, since a minor amount of slip does occur, the frequency actually furnished to the Spindle Drive PCB is 84 Hz or 51 Hz, selectable by installation of a jumper on the Oscillator PCB. The 84 Hz or 51 Hz is obtained by applying the output of the 1.92 MHz oscillator to a series of three divider circuits.

Referring to the Oscillator PCB schematic, the first divider consists of two four-bit binary counters at E39 and E51, a "D" type F/F at J27, two 8-input NAND gates at F39 and J39, a latch at H39-3/11, and associated gates and other circuitry. Without the special gating circuit involving the 8-input NAND gates, the combination of the two binary counters and the flip-flop would divide by 512 (16 x 16 x 2). However, the circuit is arranged so that a count down of 392 is available at F39-8 for use in 1500 rpm drives, and a count down of 380 is available at J39-8 for use in 2400 rpm drives. The presense or absence of a jumper at H22 determines which of the two 8-input gates drives the latch through H39-8. For 2400 rpm drives, the jumper is installed, and the resulting low at F39-2 disables the 1500 rpm gate. The low at H27-13 is inverted and applied to J39-2, enabling the 2400 rpm gate. On 1500 rpm drives, the jumper at H22 is removed, and the 8-input NAND gate at F39-8 is enabled.

The output of the latch at H39-11 in addition to resetting the divide-by-16 counters E39 and E51, drives the second of the three divider circuits. This second circuit consists of a decade counter at F27, a four-bit binary counter at E27, and three gates at F15 (output pins 11, 6, and 8). The divider circuit has two outputs. The first, at E27-11, provides division by 8, and is used for 1500 rpm drives. The second output is at F27-11, and provides division by 5 for 2400 rpm drives. The output to be gated through to the next divider circuit is also selected by H22. With the jumper installed F15-11 is disabled and F15-6 is enabled, allowing the divide-by-five output to be gated through F15-8.

The last divider circuit consists of two JK flip-flops at E15 and two "D" type flip-flops at D15. This circuit divides the output of F15-8 by 12, and furnishes two square waves 90° out of phase at 84 Hz or 51 Hz.

The "A" output of binary counter E27 drives another divider circuit consisting of two flip-flops at D27, whose output provides the 60 Hz brush motor drive power.

5.3.9B M/O-2, Oscillator (OR) PCB No. 11873

The Oscillator PCB, P/N 11873, performs the following functions:

1. Provides spindle motor drive signals with closed loop spindle speed control.
2. Provides head positioner Transducer Drive and Demodulator reference signals.
3. Generates brush motor signals.

In order to control spindle speed, there must be an accurate means of determining speed at any given time. The Oscillator Board contains a 1.920 MHz crystal oscillator (D50) whose frequency is divided down by a binary counter. Counter F40 is connected so that its output becomes a clock to be used within the board. The counter divides the crystal frequency by either five or eight for spindle speeds of 2400 or 1500 RPM, respectively. This allows the use of the same count translations and board logic for both 2400 and 1500 RPM.

An Index Mark signal line is provided to the board where it is synchronized with the board clock. This Synchronized Index

signal is fed into a set of counters entitled INDEX PERIOD COUNTER.

The INDEX PERIOD COUNTER begins running at the clock frequency upon arrival of the trailing edge of the synchronized index pulse. The counter continues to run until the leading edge of the next index pulse. Therefore, monitoring the counter content determines the time period between index pulses, and thereby spindle rotational speed. This monitoring is done by a gating network which translates the counter output into two signals, –Slightly Overspeed and –Slightly Underspeed. The presence of either of these signals indicates spindle speed is within speed limits of +1/2, –1%.

Note that the high order translated bit of the INDEX PERIOD COUNTER is labeled +This Index Slow. This line is inverted to generate +This Index Fast. These two signals are used to generate count-up and count-down clocks for an up-down counter entitled the SPEED SLIP COUNTER.

The SPEED SLIP COUNTER contains a number which will be a function of spindle motor efficiency and load at any given time. The output of the SPEED SLIP COUNTER presets another set of counters entitled the SPINDLE DRIVE COUNTER. Note that this counter is connected so that a total carry will load in the preset number. Therefore, this preset number will determine how often the SPINDLE DRIVE COUNTER overflows.

The occurrence of an overflow clocks the QUADRATURE PHASE GENERATOR, which produces two square waves with a 90° phase relationship. These output signals are routed from the oscillator board to be amplified and drive the spindle motor. Their frequency will determine spindle speed.

The SPEED SLIP COUNTER may be preset to a nominal slip value. This is done whenever spindle speed was within +1/2, –1% speed limits and has just passed out of these limits. By doing this, speed overshoot during spindle startup is held minimal. When the motor is first started and index marks appear, the time between them is long. This causes the SPEED SLIP COUNTER to count to maximum. The motor will increase in speed and tend to continue increasing past optimum. To prevent as much overshoot as possible, the overshoot condition is minimized by passing normal counting and loading the preset counter to its nominal count. This eliminates the necessity for the SPEED SLIP COUNTER to count bit by bit from maximum to optimum. The SPEED SLIP COUNTER is updated each Synchronized Index when spindle speed is out of speed limits +1/2, –1%. When spindle speed is within these limits, the counter is updated every sixteenth Index. This is done to minimize hunting around optimum spindle speed.

The Transducer Drive and Demodulator signals have a frequency of 480 kHz. This frequency is derived by dividing the crystal frequency by four. This signal is amplified and fed into two current switches, transistors E5 and E7 . The desired slope of the output waveform is provided by capacitor E6. Two zener diodes, F1 and F2, clip to the top and bottom of each cycle at the zener voltage. Transistors E8 and E12 serve as buffers to send the Transducer Drive signal out of the card. The demodulated signal is simply the 480 kHz square wave which has been buffered with hex inverter E29.

Brush motor signal generation is derived from a multivibrator which consists of a 555 timer IC connected for astable operation. The signal is a square wave with a frequency of approximately 60 Hz. It is fed directly to the I/O connector.

5.3.10 M/O-4, Temperature Compensator (TC) PCB

The TC board is used only in Model 44 drives. The circuits used on this board sense the temperature of the air brought into the drive and generate a head position correction signal, which is a function of the drive's ambient temperature.

This output, designated TEMP COMP VOLTAGE, is used to offset the detent position of the R/W head positioning mechanism when the drive's ambient temperature is above or below 25°C. Offsetting the detent position compensates for any minor differences in expansion characteristics among the various elements of the head positioning system that are not corrected by the drive's mechanical compensation.

The circuits responsible for generating TEMP COMP VOLTAGE include the following:

1. Thermistor, which serves as the variable resistance element of a Wheatstone bridge, senses the temperature of the air entering the drive and alters its resistance value as a function of that temperature.

2. Operational amplifier H10-7, which senses the error voltage at the Wheatstone bridge. This amplifier is compensated for an output of 0V at an ambient temperature of 25°C.

3. A noise filter at the output of H10-7, consisting of an RC network.

4. Operational amplifier H10-1. This amplifier's gain characteristic is tailored to satisfy the amplitude requirements of TEMP COMP VOLTAGE for its negative and positive operating ranges (10°C to 25°C and 25°C to 40°C).

In order to monitor the drive's ambient temperature, the thermistor is located near the air intake port in the front of the drive. At normal room temperature (25°C), the resistance of this thermistor is 10KΩ.

Resistor F15 is test selected to balance the bridge and to compensate for the offset voltages of H10-7 so that the output of that operational amplifier is 0V for an ambient temperature of 25°C. Resistor F11 may also be test selected and added to the ground leg of the circuit if zero offset cannot be established using F15. Amplifier H10-7 has a gain of 10.

Noise filtering of the signal appearing at H10-7 is provided by resistor F18 and capacitor F20.

The nonlinear feedback path of the second operational amplifier, H10-1, consists of resistor J6 in parallel with the resistor-diode pair J8 and J9.

When the ambient temperature is between 25°C and 40°C and the required TEMP COMP VOLTAGE is positive, diode J9 is reverse biased and the feedback path is formed by J6. For temperatures in this range, J6 alone determines the amplitude values of TEMP COMP VOLTAGE.

When the ambient temperature is between 10°C and 25°C and the required TEMP COMP VOLTAGE is negative, J9 is forward biased. For temperatures in this range, J8 is connected in parallel with J6 through the forward biased diode J9 to determine the negative amplitude values of TEMP COMP VOLTAGE.

The DC operating range of H10-1 was chosen to be large enough relative to the forward voltage drop of diode J9 to assure that the amplifier's gain conditions are controlled by resistors J6 and J8. Since this range includes output voltages that are significantly higher than the amplitudes required for TEMP COMP VOLTAGE, the output of H10-1 is transmitted through a voltage divider, consisting of resistors J12 and J14.

5.3.11A M/O-5, Sequence Logic (SL) PCB No. 11471-00/-01

The Sequence Logic PCB controls the operation of the disk drive during start-up and, to a certain extent, during the transition from the RUN mode to the LOAD mode. Most of the inter-lock functions are controlled on the Sequence Logic PCB. Specifically, the Sequence Logic PCB contains the circuitry necessary to accomplish the following:

- Insure that the disk drive cannot be placed in the RUN mode until a disk pack is installed and the equipment drawer is closed.

- When all interlocks are satisfied and the LOAD/RUN switch is set to the RUN position, initiate disk rotation, brush cycle, and drawer lock, and cause the heads to move to track zero.

- When spindle rotation has reached 50% of rated speed, cause full rated current to be applied to spindle drive motor.

- When spindle rotation has reached 90% of rated speed, cause the heads to load.

- When the LOAD/RUN switch is set to the LOAD position, initiate spindle braking, head unloading and head retraction, and condition the drawer interlock circuits to unlock the drawer when spindle rotation stops.

- Insure that the equipment drawer cannot be unlocked unless both the brushes and the heads are in the fully retracted position (other drawer interlock functions occur on the Spindle Drive PCB, as previously described).

5.3.11.1A Load-to-Run Sequence

With power on, a disk pack installed, and the drawer closed, the disk drive is ready to be placed in the RUN mode. The following conditions exist:

With the brushes fully retracted, the Brush Cycle I F/F, consisting of H39-8 and H39-6, is reset, with the output at H39-8 high. The Brush Cycle II F/F consisting of E51-11 and E51-8 is also reset, with the output at E51-8 high. The disk-pack interlock switch and the drawer closed switch, which are in parallel, are both open, resulting in a high at NAND gate input F39-4, the Start Gate. The Load/Run F/F consisting of D39-12 and J39-6 is reset, with D39-12 high and J39-6 low. The pin 5 input to the Start Gate at F39 is low, causing the Spindle Drive F/F to be reset, with E39-6 low. This low results in a high at the input to the OR gate at E39-2. Since the other input to the OR gate at E39-1 is low, the 60 Hz brush motor power from the Oscillator PCB cannot be gated through B4-11. With the heads fully retracted, the Heads Retracted F/F is reset, with H39-3 high. Since both inputs to NAND gate E39-11 are high, its output is low, resulting in a high at the pin 3 input to the Start Gate. Line "A" of Table 5-4 summarizes the more significant conditions existing on the Sequence Logic PCB with the disk drive ready to be placed in the RUN mode.

Line "B" of Table 5-4 shows the more significant changes which take place when the LOAD/RUN switch is set to RUN, but

Table 5-4.
Initial Conditions

Time	Load Run F/F		Start Gate		Spindle Drive F/F		Drawer Gate		Brush Gate	
	D39-2	J39-4,5	F39-5	F39-3	E39-4	D39-6	E39-13	E39-12	E39-1	E39-2
A	L	H	L	H	H	H	H	H	H	H
B	H	L	H	H	L	L	H	H	H	L
C	H	L	H	L	H	L	L	L	L	H

before the disk cleaning brushes start to move. Actuation of the LOAD/RUN switch has set the Load/Run F/F, producing the third high at the Start Gate input (F39-5). The output of the Start Gate now sets the Spindle Drive F/F. The low at D39-6 is gated through D39-8. The low at the output of NAND gate D27-11, after inversion at F51-4, is sent to the Spindle Drive PCB where it causes spindle drive motor rotation. It is also sent to the Address Logic 1 PCB, where it causes the heads to move to Track Zero.

The output of NAND gate D27-11 is also gated through E27-13, and is sent to the Read/Write Amplifier PCB where it resets the write-protect circuits on disk drives with this option installed.

At the same time, the low at the Brush Gate input E39-2 conditions NAND gates B4-3 and B4-11. The 60 Hz square wave pulses are gated through B4-11 and applied to the brush motor drive gates B4-6 and B4-3. These gates drive two transistors at J8 and J4. Since one transistor is PNP and the other NPN, two 60 Hz signals 180° out of phase are produced. These signals excite drivers on the Heat Sink assembly, and the brush motor rotates.

The +SPINDLE DRIVE ON signal has caused the heads to extend toward track zero. Line C of Table 5-4 summarizes the conditions which exist as the brushes and heads start to move. The Brush Cycle F/Fs have set, as has the Heads Retracted F/F. The Brush Cycle I F/F low output at H39-8 has disabled the Drawer Gate at E39-13, and the drawer unlock solenoid is deenergized. It has also maintained power to the brush motors by enabling E39-1, although the other input, E39-2, went high when the setting of Brush Cycle II F/F placed a low at E51-2. The drawer gate was also disabled by the low at E39-12 when the Heads Retracted F/F was set. The high output of the Drawer Gate also disables the Start Gate, thereby conditioning the upper half of the Spindle Drive F/F. This is required so that the Load/Run F/F can later reset the Spindle Drive F/F through E39-8.

At this point it should be noted that the NAND gate at E51-6 has had a low on one or the other of its inputs up to now, so that its output has remained high.

As the brushes complete their cycle, the Brush Cycle I F/F is reset. The Brush Cycle II F/F is maintained in the set condition by the low at E51-13. Resetting the Brush Cycle I F/F has placed a high at E39-1, disabling the Brush Gate, and the brush motor stops. With the Brush Cycle I F/F reset and the Brush Cycle II F/F set, a low now is present at the output of NAND gate E51-6.

5.3.11.2A Head Loading

The heads are loaded to their flying position over the disk by a –HEAD LOAD ENABLE signal and a +HEAD LOAD PICK signal. The pick signal, through a driver circuit on the Heat Sink Assembly, pulls in the head-load solenoid with a 48V pulse, while the enable signal, also through a driver circuit on the Heat Sink Assembly, maintains the solenoid in the energized condition with 24V across the coil. In order for these signals to occur, the following three conditions must exist:

- the heads must be over the disk
- the brushes must have completed their cleaning cycle
- the disk must be rotating at more than 90% of its rated speed.

Referring to the Sequence Logic PCB schematic these three conditions are ANDed at F39-12. The +HEADS OVER DISK signal, developed on the Sensor PCB, is applied to the NAND gate at F39-1. The high at F39-2 occurs at the end of the brush cycle, when the Brush Cycle flip-flops are reset producing highs at H39-8 and E51-11. The –HEAD LOAD ENABLE signal will then be gated in the Q output of the Up-to-Speed F/F as D15-9 goes high.

As the disk starts to rotate, index marks are generated on the Sensor PCB, and are furnished to pin T of the Sequence Logic PCB, where they drive a divide-by-two circuit consisting of F/Fs at D15-3 and B27-11. The output at B27-8 drives an integrator circuit consisting of three type 558 Op Amps and associated circuitry. The capacitor at A25 is the integrating capacitor. As the speed of disk rotation increases, so does the frequency of the index marks. When the disk has reached approximately 50% of its rated speed, the capacitor at A25 discharges enough to make the input to the Op Amp at D52-6 go negative. The high output of this amplifier is fed to the D input of the Up-to-Speed F/F at J51-9, which was previously cleared by the –INITIAL RESET signal. With high D input, this F/F is toggled by the next clock pulse furnished from the $\overline{Q}$ output of divide-by-two F/F D15-5. When the $\overline{Q}$ output of F/F J51-9 goes low, it generates the +SPEED OK signal, which is sent to the Sensor PCB, where it is used to apply full power to the spindle drive motor. When the disk has reached approximately 90% of rated speed, the level of charge on capacitor A25 will be sufficient to drive the output of Op Amp A52-1 high. This high is applied to the "D" input of Head-Load Enable F/F D15-9, which is then toggled by the next clock pulse from the divide-by-two F/F D15-5. When the Head-Load Enable F/F toggles, its Q output furnishes the remaining high at the input to the NAND gate at F39-13, and the –HEAD LOAD ENABLE signal is generated. The output of the NAND gate at F39-12 is inverted and used to trigger a one-shot multivibrator at A4. The Q output of the multivibrator is ANDed with the high Head Load Enable signal at B4-8, and drives the head load pick transistor at J12. This transistor conducts furnishing the +HEAD LOAD PICK signal. At the end of the period the Q output of the multivbrator goes high. This is ANDed with the high Head Load Enable signal at D27-3, which is applied as a low to the "D" input of the Heads-Loaded Signal F/F B27-5. At the next clock pulse, the Q output of B27-5 goes high. This is ANDed at D27-8 with the high Head Load Enable signal and results in the +HEADS LOADED signal at E27-2. This signal is sent to the Read/Write Amplifier PCB, where it is ANDed with the not-write-fault signal to produce +FILE READY. It is also sent to the RDR2 PCB where it is used to condition various functions.

The low output of the NAND gate at D27-8 is also sent to one input of the OR gate at D39-11, where it is used to insure that the +SPINDLE DRIVE ON and +SPINDLE ENABLE signals are maintained while the heads are loaded.

5.3.11B M/O-5, Sequence Logic (SL) PCB No. 11471-02/-03

The Sequence Logic PCB, P/N 11471, controls the operation of the disk drive during start-up and, to a certain extent, during the transition from the RUN mode to the LOAD mode. Most of the interlock functions are controlled on the Sequence Logic PCB. Specifically, the Sequence Logic PCB contains the circuitry necessary to accomplish the following:

- Insure that the disk drive cannot be placed in the RUN mode until a disk pack is installed and the equipment drawer is closed.
- When all interlocks are satisfied and the LOAD/RUN switch is set to the RUN position, initiate disk rotation, brush cycle, and drawer lock, and cause the heads to move to track zero.
- When spindle rotation has reached 95% of rated speed, cause the heads to load.
- When the LOAD/RUN switch is set to the LOAD position, initiate spindle braking, head unloading and head retraction, and condition the drawer interlock circuits to unlock the drawer when spindle rotation stops.
- Insure that the equipment drawer cannot be unlocked unless both the brushes and the heads are in the fully retracted position (other drawer interlock functions occur on the Spindle Drive PCB, as previously described).

5.3.11.1B Load-to-Run Sequence

In the LOAD condition, the spindle and brush motors are stopped, the heads are unloaded and retracted, and the Disk Pack Interlock line is active. The following latches will be in the reset state:

Heads Retracted latch F8-8/11 (zone G)

Load/Run latch F8-3/6 (zone C14)

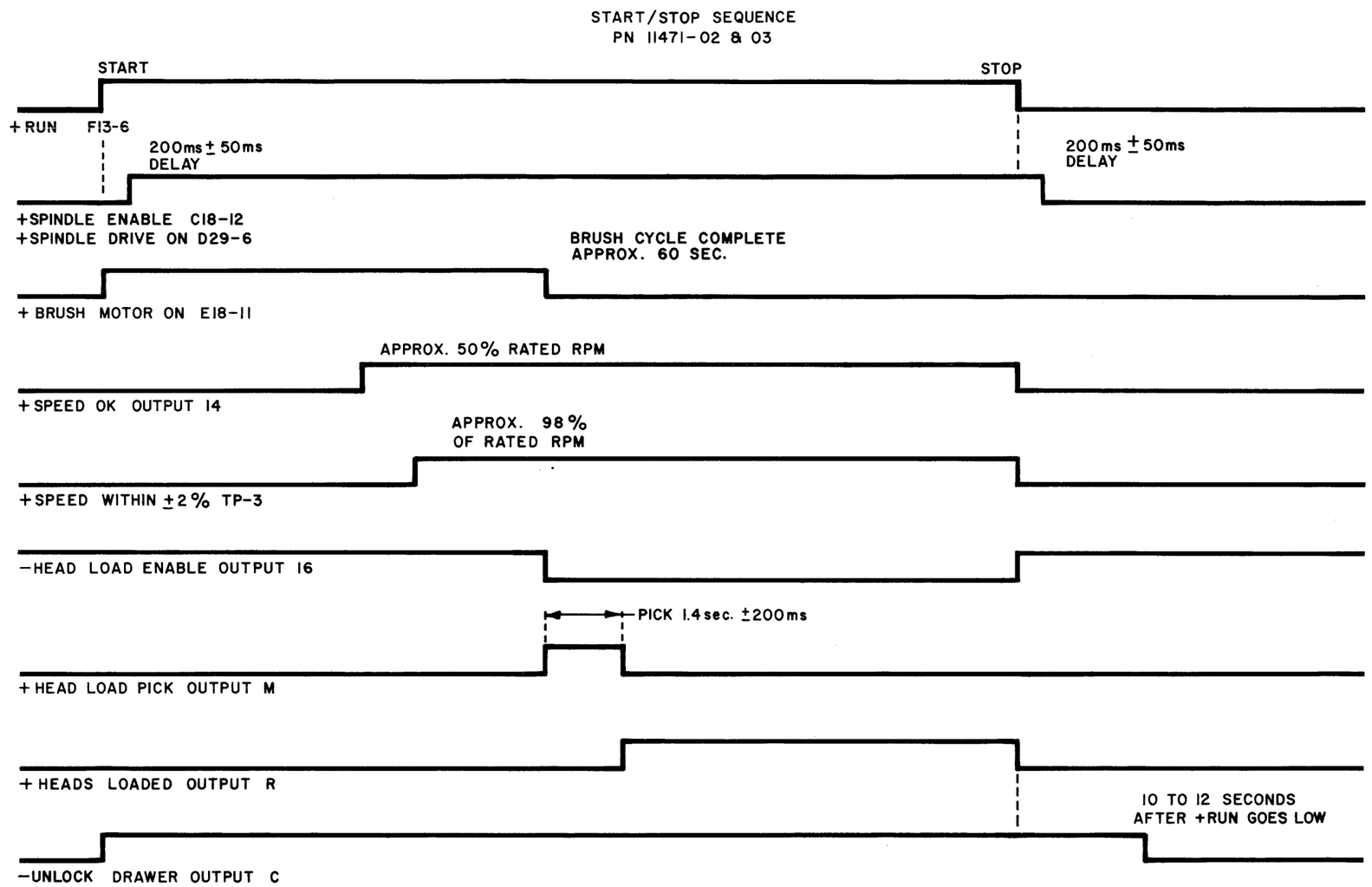
Spindle Run E18-6/E18-12 (zone C12)

Notice the low output from pin 6 of the Spindle Run latch combines with the –Reset signal in gate E18-8 at zone C11. The resulting high from E18-8 goes to zones H4, J4, and K4 to directly reset 3 "D" type flip-flops in the speed control logic. This assures Speed Greater Than 95%, Speed Within 2%, and the Speed O.K. signals will always be in the reset condition when the Run Sequence begins.

The Allow Brush Cycle latch at zone E12 is set by ANDing the +Brushes Home signal and the high output of the Load/Run latch F8-3. This is in preparation for the Run Sequence.

Transferring the LOAD/RUN switch to the RUN position sets the Spindle Run latch at zone C12. (See Figure 5-33A for timing sequence) The +Spindle Run line goes high, and combines with +Allow Brush Cycle and No Reset in gate F18-8 at zone E11. These conditions AND with Brushes Home in gate E18-11 to provide the +Brush Motor On signal. This line AND's with the +60 Hz signal to provide a 60 Hz drive to the bases of transistors B48 and B53 at zone D4. These transistors are driven 180° out of phase, and provide 60 Hz current for the brush motor. Thus, when the +Brush Motor On line goes high, the brush motor starts, and the brushes begin their excursion over the disk. As they move out, the brush transfers, Brushes Home latch D18-3/6 at zone E14 resets, and the set output (D18-3) goes low to hold the +Brush Motor On line high and active. Notice this line is inverted by F29 at zone E10, and this low output disables AND gate B8-6 (zone G10) for Head Load Pick, thus preventing head loading while the brushes are extended over the disk. When the brushes complete the cycle and the brush switch transfers back to bring the brushes home line high, AND gate E18-11 at zone E11 is satisfied, and the +Brush Motor On output goes low. This output will de-gate the 60 Hz line to the brush motor drivers. (The Allow Brush Cycle latch cannot set again with +Brushes Home since the Load/Run latch is in the Run state.)

When Spindle Run was activated and the brush cycle began, the +Spindle Run line also triggered the 200 ms Head Retract Delay at zone B10. The delay has no significance in the Start Sequence, but is necessary when the LOAD/RUN switch is transferred to the LOAD position. When Load becomes active, (Stop Sequence), the Spindle Run latch resets and feeds a low input to gate E18-8 at zone C11. The output of this gate (test point 9) directly resets the three speed flip-flops. When the Speed Equal to or Greater Than 95% flip-flop resets, it disables the gate providing Head Load Enable (test point 6) at zone G10, and the heads unload. To insure complete unloading of the heads before the disk rotation slows down, the Retract Delay is triggered when the Spindle Run latch resets. This holds +SPINDLE ENABLE and +SPINDLE DRIVE active (high) for 200 ms after the head load enable goes inactive to unload the heads. At the end of the 200 ms delay, the Allow Brush Cycle latch sets, Spindle Run latch resets holding a reset on the three speed flip-flops, the heads are unloaded and retracted, and spindle drive goes off. Approximately 1 second later, the heads are fully retracted and the Heads Retracted latch at zone G12 sets. This enables Unlock Drawer gate A8-8 at zone E9. The output of this gate, –UNLOCK DRAWER, is sent to the Spindle Drive Board, M01, as one enable to the drawer unlock solenoid driver. (The solenoid will pick when the spindle has stopped rotation AND the –UNLOCK DRAWER signal is active.) At this time the Stop Sequence is complete.



NOTES

1. 200ms DELAY ON SPINDLE ENABLE AND SPINDLE DRIVE ON IS TO ENSURE HEADS UNLOADED BEFORE SPINDLE TURNS OFF.
2. HEAD LOAD PICK= 1.4 sec. ±200m.s.

Figure 5-33A. Start/Stop Timing Sequence

5.3.11.2B Spindle Speed Monitoring

Timing diagrams, showing both the normal and abnormal speed conditions of the standard 2400 RPM and optional 1500 RPM spindle speed monitoring logic, are provided in Figure 5-33B through 5-33E.

Basic timing control for monitoring spindle speed is a clock signal derived from a Type 555 free running multivibrator shown at zone K16. Since the time period is critical, a one percent tolerance resistor (A43) is used for trimming. The resistance is selected to provide a 195.3 ± 0.3 μs time period. The clock signal, (test point 2 at zone K15), is connected to the "A" input of bit binary counter B40, shown at zone K14. Counter outputs QA, QB, QC, and QD correspond to binary bits 1, 2, 4, and 8. This counter divides the basic clock by 5 for 2400 RPM use, or by 8 for the 1500 RPM option. The bit 4 output, QC, goes through an inverter and a gate to the "A" input of a second four bit counter, D40. Notice this line also is connected to test point 10 at zone L12. Each time the bit 4 output of B40 makes a complete transition, (low to high to low), the second counter advances by one. The bit 4 output of B40 also feeds one input of AND gate F40 at zone L12. The second input to this gate is bit 1 of the counter. When the counter advances to a count of 4, test point 10 will go low, and advance the second counter. When B40 reaches a count of 5, the output of AND gate F40 goes low and resets counter B40. The counter thus counts to 5, resets itself, and starts counting again. Each time it counts to 5, the second counter advances by one.

If the drive has the 1500 RPM option, a 10Ω resistor is placed in location F49 at zone L13. This holds a low input on the reset gate, thus, a count of 5 will not reset the counter. In this case, B40 will count to 4, and the bit 4 line will go high advancing the second counter. The bit 4 line will stay high through counts of 5, 6, 7, and go low when the counter reaches 8. At this time the QD output goes high, is inverted by F29-2, and resets the counter. B40 then counts to 8, resets itself, and begins counting again. During each count to 8, the second counter advances by one.

For the standard 2400 RPM machine, the time period for the waveform at test point 10 is .975 to 0.978 ms. For the 1500 RPM option, (divide by 8), the time period at test point 10 will be 1.560 to 1.565 ms.

D40 and C40 are connected as an 8 bit binary counter. Notice the reset inputs of all three counters and the multivibrator reset are all connected to the Index Mark line. This provides a binary time count from the trailing edge of one index pulse to the leading edge of the next. By translating the counts between index pulses, index time periods and disk rotational speed may be determined. Three counts are translated and used in speed monitoring. These counts are: 24, equal to or greater than 26, and 64. Notice the QC output of C40 (bit 64) is inverted by C18-4 and is ANDed with the divided clock signal by gate A8-3 (zone K12). When the disk first starts rotation, rotating speed is slow and there is a long time period between index pulses. When

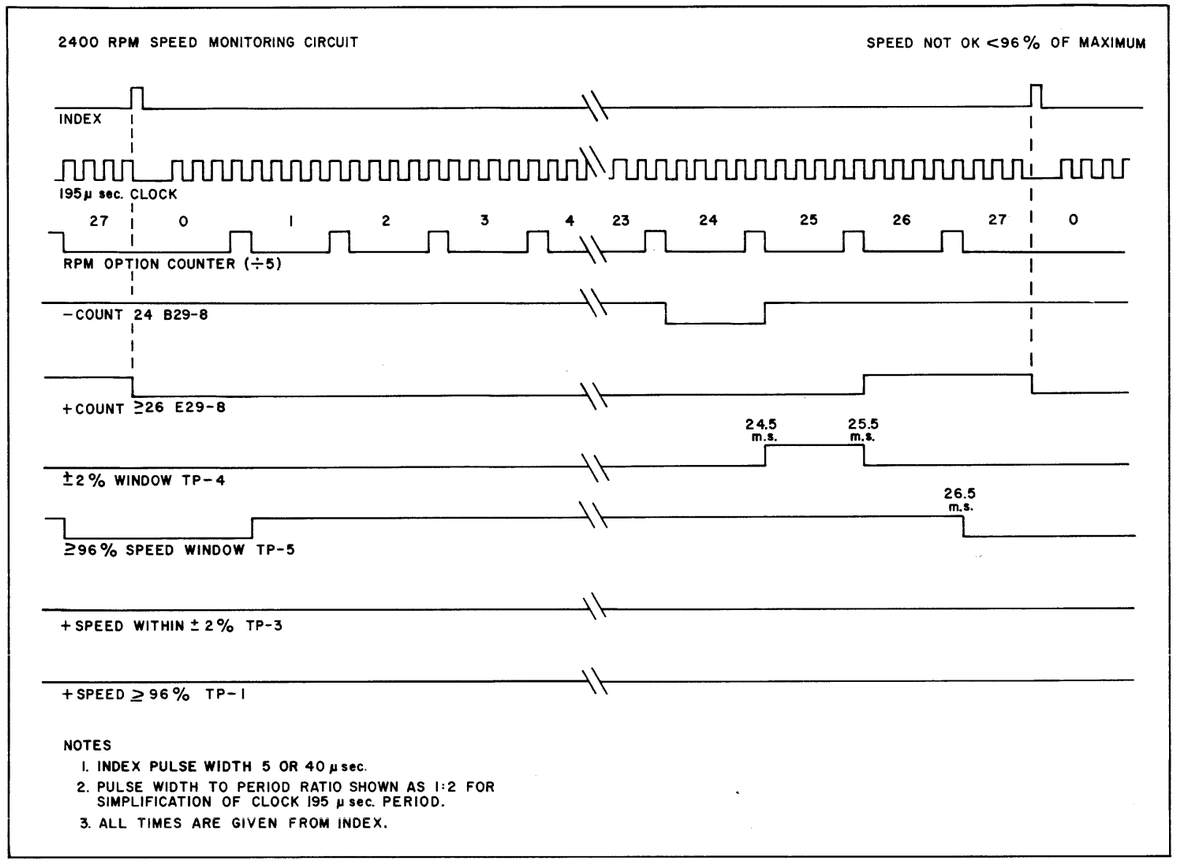


Figure 5-33B. 2400 Spindle Speed Monitoring Logic Timing Diagram (Speed Not OK, < 96%)

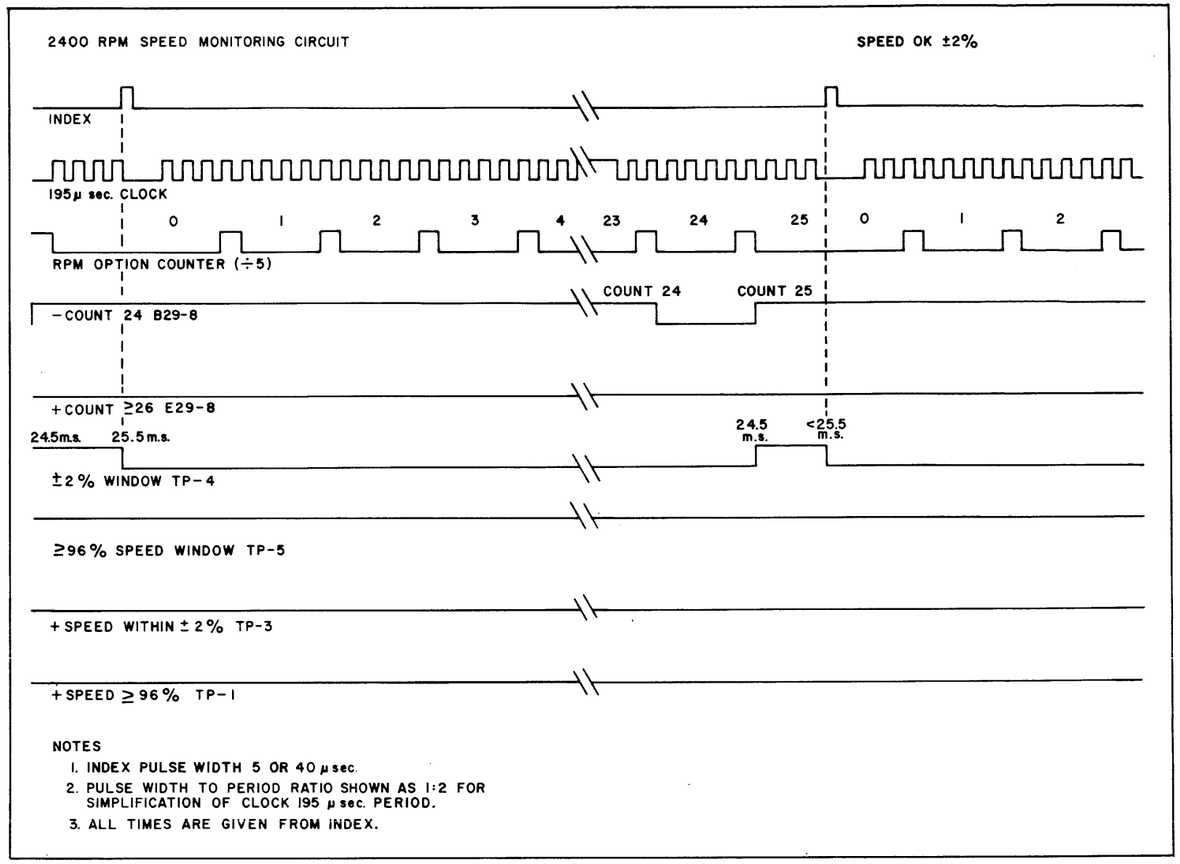


Figure 5-33C. 2400 RPM Spindle Speed Monitoring Logic Timing Diagram (Speed Within ±2%)

the counter reaches a count of 64, clock inputs to the counter are de-gated, and the counter stops at the 64 count. The inverted 64 line, (−Count > 64), is connected to the "D" input of flip-flop C29 at zone H4. Clock input to this flip-flop is index. The next index will reset the flip-flop, and the +SPEED OK line will go inactive or low. This continues until the next index pulse occurs before the counter reaches 64. At this time, the +SPEED OK line will go active and high. This is used to shift the spindle drive motor from a low speed mode to a high speed mode.

Two other "D" type flip-flops, A29-9/8 and A29-5/6, are also clocked by index pulses. Significance of flip-flop A29-9/8 is "Spindle Speed is Equal to or Greater Than 95% of full speed". (This will be used to time head loading.) The pin 5 output of flip-flop A29-5/6 will be high, or active, at any time spindle speed is within ± 2% of full speed.

AND gate E29 at zone J6 translates "Counter Equal to or Greater Than 26". (For standard 2400 RPM rotation, 0.975 to 0.978 ms pulses advance the counter.) The next clock pulse will set "D" type flip-flop A18-5/6 at zone J6. Test point 5 will then go low the determined time after the trailing edge of index. If the next index pulse occurs after this time, the test point 1 flip-flop will be reset, indicating that disk rotation is still less than 95% of full speed. When the disk speeds up so that index pulses occur less than 5% below full speed, the counter will not reach a count of 27, (count 26 plus one more clock pulse to set the test point 5 flip-flop), and test point 5 will be high when the next index pulse occurs. This will set the 95% speed flip-flop. As long as disk rotation does not slow below 5% of the rated RPM, test point 1 will remain high, indicating speed is greater than 95%.

When the counter reaches 24, the "D" input of flip-flop A29-5/6 will go high. If an index pulse occurs after this, the flip-flop will set with index, and the Q output (test point 3) will go high, indicating the disk is within 2% of full speed. Since the "D" (pin 12) input to flip-flop A18-9/8 will be high only during a count translation of 24, index pulses must occur within one count time period for flip-flop A29-5/6 to set. Count pulses as seen at test point 10 for the standard 2400 RPM machine will have a 0.975 to 0.978 ms time period. If index pulses do not fall within that range, test point 3 will go low, and cause the +HEADS LOADED line at zone G5 to go low. This will cause the File Ready line to go inactive, and turn the Ready Light on the front panel off. If spindle speed slows to more than 5% below rated speed, test point 1 will go low, disable the AND gate B8-6 at zone G10, and cause test point 6 and the −HEAD LOAD ENABLE line to go high and unload the heads.

5.3.11.3B Head Load/Unload

When the Load/Run switch is in the Load Position, the carriage and heads are fully retracted to allow changing disk cartridges. (The head load solenoid is de-energized and the heads unloaded before the carriage is retracted.) When the Load/Run switch is placed in the Run position, the spindle drive motor is energized and the spindle starts rotation. At the same time, the carriage begins moving forward, extending the head arms and heads over the disk surface. The servo will lock on, or electrically detent, when the head gaps are located over track zero. The +HEADS OVER DISK line at zone G17 will go active or high at this time providing one input to AND gate B8 at zone G10. The pin 3 output to this AND gate will go high when the speed monitor (test point 1 at zone J4) detects 95% of full rotational speed. The pin 5 input to B8 will go high when the brushes have completed their cycle and are retracted out of the disk area. At this time, test point 6 at zone G9 will go low activating the HEAD LOAD ENABLE line. This line is routed to the Heat Sink to enable holding current to the head load solenoid. The −HEAD LOAD ENABLE line is inverted by C18-6 at zone F6 and provided as the pin 1 input to B18-3. The second input to the AND gate is from the Head Load Pick timer E40. This timer is triggered when test point 6 (−HEAD LOAD ENABLE) at zone G9 goes low. The timer will stay set for a period of 1.4 sec ± 200 ms and provide a high current pick signal for the head load solenoid for that time. The output of the timer is also inverted by

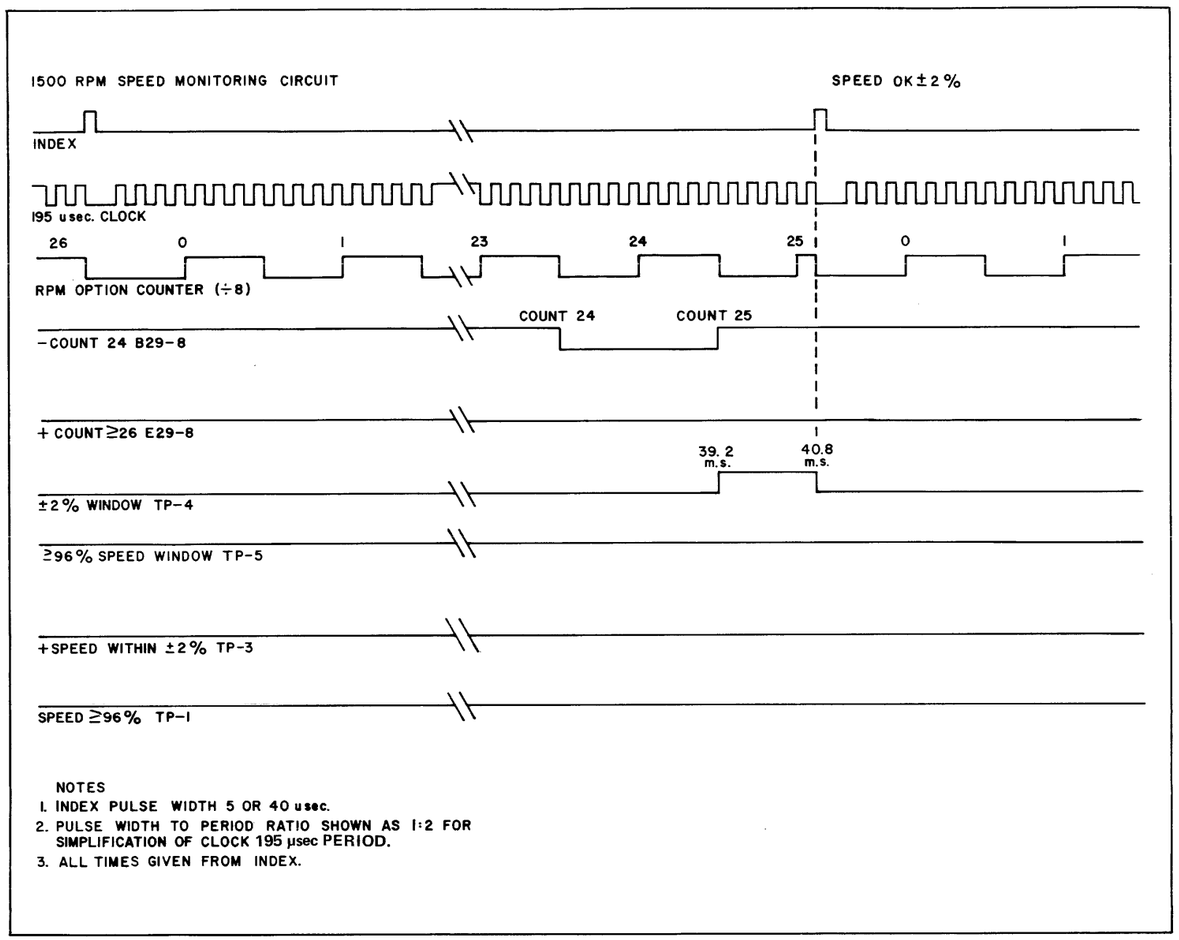


Figure 5-33D. 1500 RPM Spindle Speed Monitoring Logic Timing Diagram (Speed Within ±2%)

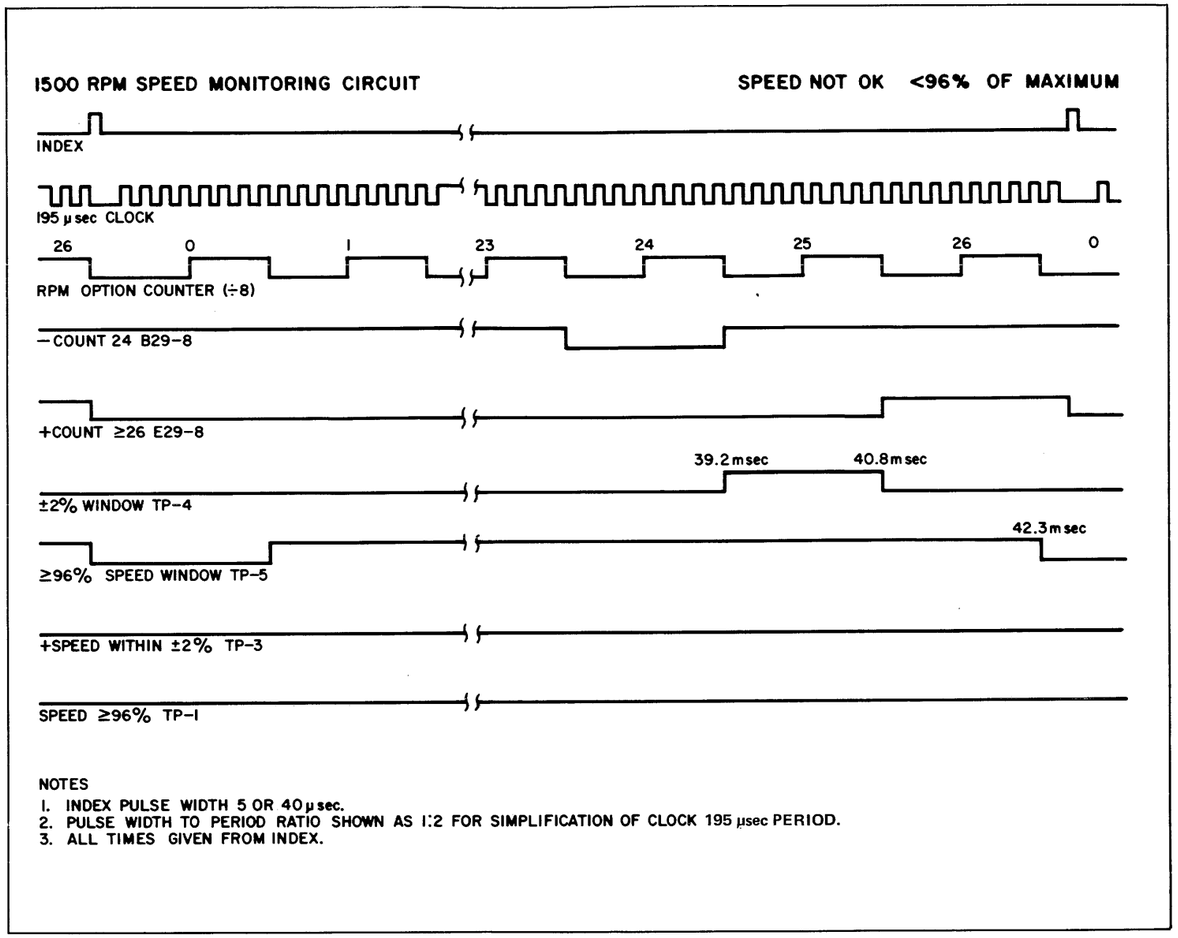


Figure 5-33E. 1500 RPM Spindle Speed Monitoring Logic Timing Diagram (Speed Not OK, < 96%)

AND gate B8-12 to partially enable +HEADS LOADED AND gate B8-8 at zone G5. The +HEADS LOADED line will activate (go high) when:

The disk is within 2% of full speed, and

Head Load Enable is present, and

Head Load Pick delay has timed out.

The −HEAD LOAD ENABLE line will go high or inactive and cause the heads to unload under any of the three following conditions.

1. The disk rotational speed drops under 95% of full speed.
2. The +Brush Motor On signal goes active.
3. The +HEADS OVER DISK line goes low or inactive.

5.3.12 M/O-6, Sensor (SR) PCB

The Sensor PCB contains the circuits necessary to accomplish the following:

- Process the outputs of the home sensors to produce the +HEADS OVER DISK, +HEADS OVER TRACKS, and +ZERO TRACK SENSING signals.
- Monitor current in the linear motor, and generate a −SEEK INCOMPLETE signal and a −SERVO DISABLE signal if the current is excessive.
- Monitor the level of the 5-, 15- and 24-volt supplies, and issue a −INITIAL RESET signal when any of these voltages are out of tolerance, including during the initial power-on period.
- Accept, amplify, and shape the outputs of the index transducers.
- Produce Spindle Drive Cut-off signals during the initial reset period.
- Separate the index and sector marks received from the lower index transducer, and provide these index and sector marks to other Series 40 PCBs, as required.
- On the standard Series 40 configuration, furnish the index marks of the selected disk to the interface via the RDR1 PCB.
- If the Sector Counter Option is installed, furnish unseparated upper-disk index and sector marks to the RDR1 PCB, where separation is accomplished.
- Furnish the Sequence Logic PCB with sector and/or index marks from the selected disk.

5.3.12.1 Voltage Monitoring and Initial Reset

The voltage monitor consists of transistors at B14 and B17, a capacitor at A27, and associated diodes, zener diodes, and resistors. When power is first applied to the disk drive, and before voltages have risen to their within-tolerance values, the five diodes at A6, A8, A10, A16, and A18 conduct. The six zener diodes at B6, B8, B10, A21, A23, and A25 are reverse biased, but not sufficiently so to conduct. The currents through the resistors at A11, A17, and A19 cause a voltage drop across the resistors sufficient to keep the transistors at B14 and B17 cut off. The capacitor at A27 charges toward 15V. When the voltage supplies are within tolerance, the zeners are sufficiently reverse biased to conduct. This places reverse bias on the regular diodes, and they

cut off. With the negative voltage removed from the base of B14, and the positive voltage removed from the emitter of B17, the transistors conduct. Capacitor A27 discharges through B14 and B17. The voltage across the capacitor, then, has risen from zero when the power was initially applied, to some positive value when the voltages reached their in-tolerance values, and then dropped to zero. This is the collector voltage waveform of B14, and is the Initial Reset signal. It is approximately trapezoidal in form. If any of the supply voltages should fall below tolerance, the corresponding zener diode or diodes will cut off, and the transistors B14 and B17 will cut off. In this case, another Initial Reset signal will result.

The Initial Reset signal at the collector of B14 is applied to the base of the transistor at B32, which was originally cut off. B32 conducts during the Initial Reset pulse, and this signal is fed through D42-2 and E42-3/11 to the Sensor PCB interface as a negative-going pulse. The signal on the collectors of B14 and B32 are also supplied to spindle-drive-cutoff transistors at B43 and B47, causing them to conduct. This effectively places the collectors of B43 and B47 at ground, holding the spindle drive cut off during initial reset.

The ground in the collector circuit of B43 and B47 is also applied through diodes B40 and E40 to the SERVO DISABLE line, disabling the servo during initial reset.

5.3.12.2 Lower Index Mark Separation

The output of the lower index transducer consists of unseparated analog index pulses and sector pulses. These analog signals are applied to Schmidt Trigger amplifier H12-10, whose output will be positive pulses clamped to +5V and ground. These pulses are applied to a one-shot multivibrator at E12, which is triggered by the trailing edge of the pulses. The period of the one-shot is 40 μs, and its positive output pulses are termed index marks or sector marks, depending on which slot on the disk hub produced the pulse.

The unseparated index and sector marks at the Q output of E12 are applied to a separator circuit consisting of another one-shot multivibrator at K30 and two NAND gates, J30-6 and J30-3. The one-shot multivibrator is a type 74121 connected so that it will trigger on positive-going pulses at the "B" input. Its timing components give it a period of about 850 μs.

For purposes of this description, assume that the first output of the one-shot at E12 is a sector mark. Prior to arrival of the sector mark K30 is in its stable state. Its low Q output disables J30-4, and its high $\overline{Q}$ output enables J30-1. The high output of J30-3 is applied to the "B" input of the one-shot. When the sector mark arrives, it is gated through J30-3 and is applied as a negative pulse to H30-9/10. The low at J30-3 is also applied to the input of the one-shot. However, it does not trigger at this time, since it is connected to trigger on positive-going pulses. At the end of the sector mark, however, J30-3 goes high, triggering the one-shot. The Q output goes high and the $\overline{Q}$ output goes low, conditioning J30-4 and disabling J30-1 for approximately 850 μs. If the next output of the 40 μs one-shot at E12 is an index pulse, it will arrive within the 850 μs period, and will be gated through J30-6. However, if it is a sector mark, the 850 μs one-shot will have timed out, and the pulse will be gated through J30-3 as before. It can be seen that lower disk sector marks will appear at H30-14, and that lower disk index marks will appear at E30-3.

In the standard configuration the lower sector marks and lower index marks are supplied to the sector counter via Sensor PCB interface pins M and E, respectively. The Lower index mark is also furnished to the Sequence Logic PCB via pin T, and to NAND gate E30-5. The other input to the NAND gate at E30-4 is the DISK SELECT signal. If the lower disk is selected, the index mark is gated through to Sensor PCB interface pins 11 and 12.

If the disk drive has the Sector Counter Option installed, the jumper at F35 is removed, and the lower index marks are supplied only to Sensor PCB interface pins E and T. The jumper at F34 is installed, and the lower sector marks are supplied to E30-5, instead of index marks. When the lower disk is selected, the sector marks are gated through E30-8 to Sensor PCB interface pin 12. They are not applied to interface pin 11, since the jumper at F29 is removed.

5.3.12.3 Upper Disk Index and Sector Marks

Upper disk index transducer pulses are amplified and applied to a 40 μs one-shot multivibrator in a manner identical to that for the lower disk. However, since there are no sector slots (and hence no sector marks) in the standard configuration, there is no separator circuit. Upper disk index marks are applied through jumper F31 to the input of the NAND gate at E30-11. If the upper disk is selected, the index marks are gated through to Sensor PCB interface pin 11.

If the Sector Counter Option is installed, there is a jumper at F30 and none at F31 or F29. Unseparated index and sector marks are then inverted at D30-3/4 and applied to the RDR1 PCB via Sensor PCB interface pin 11. The index and sector marks are separated on the RDR1 PCB as previously described, and the separated upper sector marks are returned to the Sensor PCB interface pin D. Separated index marks will be routed to the Sector Counter PCB, and will be gated to the I/O interface by the DISK SELECT signal.

The jumper at F32 is installed and the sector marks are applied to E30-12. When the upper disk is selected, they are gated through to interface pin 12.

5.3.12.4 Servo Disable and Seek Incomplete

If the servo motor should draw excessive current, this is sensed on the Heat Sink PCB, which furnishes a low CURRENT DETECTOR signal to the Sensor PCB. This low is applied to the base of the transistor at E53, cutting it off. The output of the transistor is applied to a seek incomplete F/F, consisting of transistors at F53 and D53. When E53 cuts off, a high on the base of F53 causes it to conduct, toggling the F/F. The low at the collector of F53 results in a –SEEK INCOMPLETE signal to the AL2 PCB and, if gated through by the +FILE READY signal, a –SEEK INCOMPLETE OUTPUT signal to the interface. In addition, SERVO HOLD is grounded.

5.3.12.5 Heads-Over-Disk/Tracks Signals

The +HEADS OVER DISK, +HEADS OVER TRACKS, and +ZERO TRACK SENSING signals are generated by a system which includes a Home Sensor Light-Emitting Diode (LED), two photo sensors, a moving shutter, and associated amplifiers and gates. The LED and photosensors are in a fixed position on the Head Positioner assembly base plate, while the shutter is attached to the movable head-carriage assembly. When energized, the LED shines on the photosensors to an extent determined by the position of the shutter, which moves between the LED and the sensors, as the head carriage moves back and forth. The outputs of the sensors are furnished to the Sensor PCB, where they are amplified and conditioned to produce the +HEADS OVER DISK, +HEADS OVER TRACKS, and +ZERO TRACK SENSING signals.

In Figure 5-34, views (a) and (b) show the orientation and movement of the shutter with respect to the two photosensors, labeled "A" and "B" in the figure. The shutter is shown in the fully retracted position in view (a). The light from the LED falls fully on both of the sensors, and their output is maximum. View (c) of Figure 5-34 shows the signals at TP-2 and TP-3 of the Sensor PCB as the head carriage, and hence the shutter, moves forward from the fully retracted position. Referring to the Sensor PCB schematic, the outputs of the sensors are applied to two Op Amps. TP-2 and TP-3 are at the Op Amp outputs, and the signals at these test points are proportional to the inputs from the sensors.

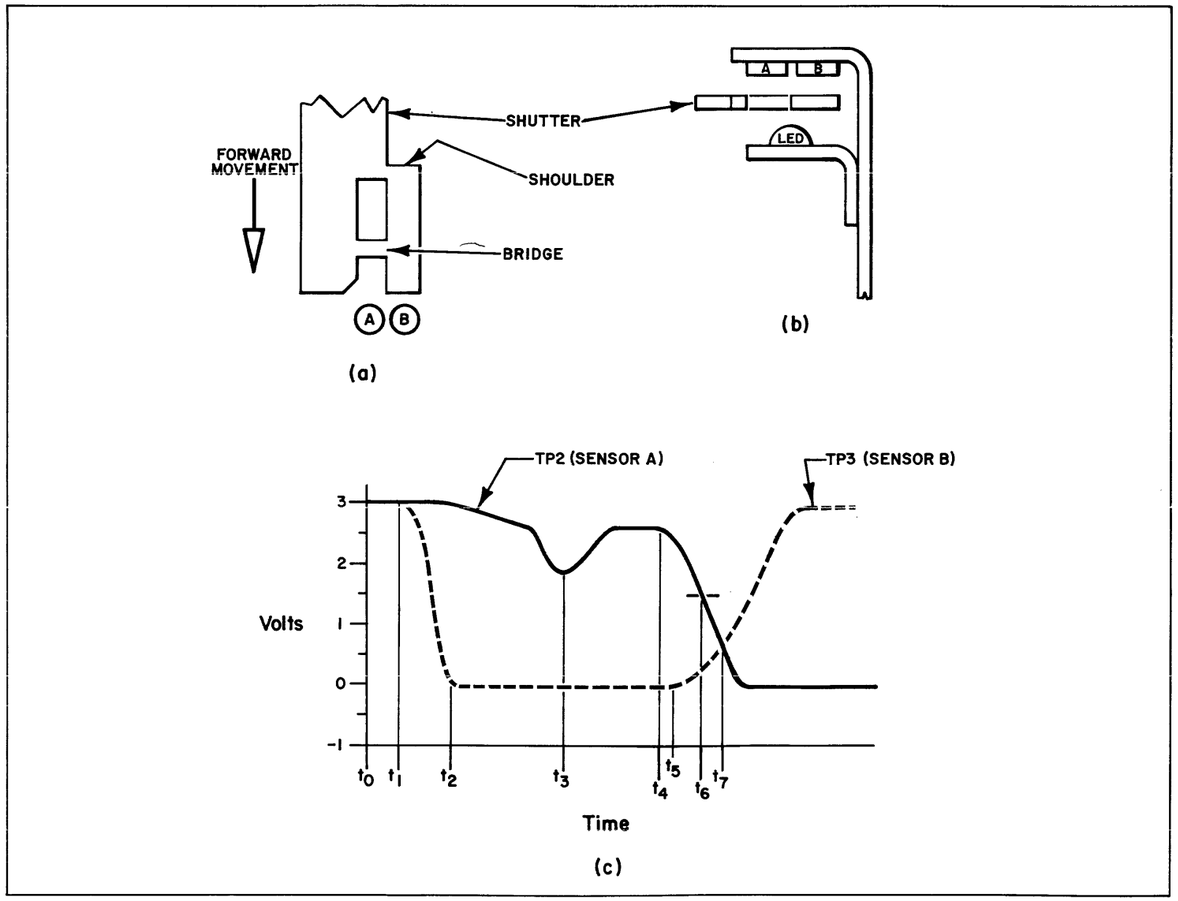


Figure 5-34. Generation of Home Sensor Signals

Referring to Figure 5-34, in the fully retracted position at time t_0 both sensors are completely exposed, and the signals at TP-2 and TP-3 are at 3V, which represents maximum output of the sensors. At time t_1, sensor B begins to be covered by the shutter, and its output starts to decrease. The output of sensor A remains at a maximum, since the slot in the shutter keeps it fully exposed to the LED at this point. At time t_2, sensor B is fully covered, and the output at TP-3 is 0V. At time t_3, the bridge across the Sensor A slot results in a decreased output of sensor A. This serves no purpose electrically; the bridge is necessary to the mechanical strength of the shutter.

At time t_4, the end of the slot begins to cover sensor A, and its output starts to drop. Soon after, at time t_5, sensor B begins to receive energy from the LED as the shoulder on the shutter approaches sensor B. As the shutter continues forward, sensor B remains fully exposed and sensor A remains fully covered. TP-3 remains at 3V and TP-2 remains at 0V.

Referring to the schematic, the amplified signal from sensor A is applied to another Op Amp at K15-2. The non-inverting input of this amplifier is set at approximately 1.5V by a voltage divider consisting of resistors at K25 and K27. When the input from sensor A has dropped to the point where TP-2 is at 1.5V, which occurs at time t_6 in Figure 5-34 (c), the output of the Op Amp at K15-1 goes high. The shutter and the sensor assembly are adjusted so that this occurs as the R/W head slider passes the edge of the disk. The high output is sent to the Sequence Logic PCB as the +HEADS OVER DISK signal, where it enables head loading. The output at K15-1 also conditions a NAND gate at J30-12.

At time t_7 in the figure, the outputs of the two sensors are equal (although B is rising and A is dropping). They cross at approximately 0.7V as measured at TP-2 and TP-3. The outputs of both sensor Op Amps are applied to another Op Amp at K15-7. When the two signals cross at 0.7V, the output at K15-7 goes high. The shutter and sensors are adjusted so that this occurs when the R/W heads reach Track 0. The high output at K15-7 is applied through the parallel combination of resistor F41 and gates H30-3 and H30-13 to J30-13, resulting in the +HEADS OVER TRACKS signal. The high at H30-13 is also applied to a pulse-forming circuit consisting of five type 836 inverters. The output at H38-6 is the +ZERO TRACK SENSING signal, which is a pulse of about 1 μs pulse width.

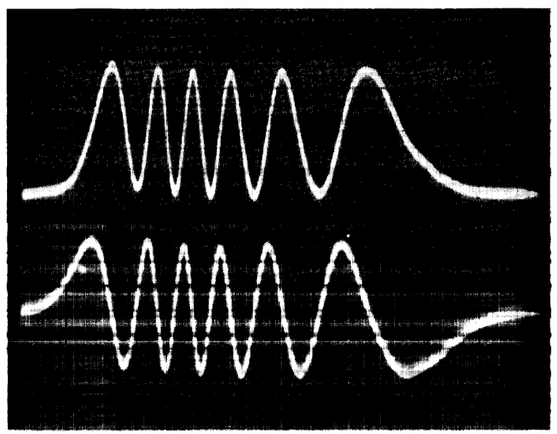


Figure 5-35. Demodulation Network Output Signals

The +HEADS OVER TRACKS and +ZERO TRACK SENSING signals are sent to the AL1 PCB, where they are used to control the direction and speed of the heads as they reach Track 0.

5.3.13 M/O-7, Servo (SO) PCB

The circuits located on the SO board produce three output signals.

The board's principal output is SERVO DRIVE SIGNAL, which is sent to the drive current circuits on the HS board. There it controls the amount and polarity of current supplied to the positioning motor.

The other two outputs are a pair, of phase-related square waves, designated SERVO LOGIC CONTROL LEVEL C and SERVO LOGIC CONTROL LEVEL D. These pulse trains provide position and direction information about the heads to other logic associated with head positioning.

Details regarding the SO circuits responsible for generating these outputs are presented below. The information is organized according to major functional elements on the SO board. These elements and the principal signal paths connecting them are illustrated in Figure 5-12, Servo System Functional Block Diagram (see Section 5.2.4).

5.3.13.1 Demodulation Network

This circuit demodulates the two 480 KHz AC signals received from the head position transducer's secondary element. The signal on channel B has a 90° phase displacement with respect to the signal on channel A.

A 480 KHz square wave, designated DEMOD SIGNAL, is used as the carrier reference input for the demodulation process. DEMOD SIGNAL is taken from the same circuit on the OR board that generates the head position transducer's primary input. This assures that the frequency of DEMOD SIGNAL matches the channel A and channel B carrier frequencies.

The signals on channel A and channel B follow separate and identical paths through the demodulation circuits. The first stage in each path is a wideband video amplifier with differential outputs.

Each amplified signal pair is applied to a balanced modulator/demodulator device, which operates in the demodulation mode.

Figure 5-35 illustrates one pair of Demodulation Network output signals (A and B) as sampled at TP-9 and TP-7. These wave forms represent a 24-cylinder seek.

The outputs of the demodulation devices are amplified by four operational amplifiers. Each amplifier has a gain of approximately 8.

The four amplified demodulation envelopes are designated A, $\overline{A}$, B and $\overline{B}$. They are sent to the Differentiation Circuits and to the Reference FET Network. Three of these signals, $\overline{A}$, B and $\overline{B}$ are also applied to the C and D Summing Networks. All of these functions are performed by circuits located on the SO board. The peak-to-peak amplitude of the demodulated envelopes, as they appear at TP-13, 15, 16 and 18, is 15V ± 1V.

5.3.13.2 Reference FET Network

This network consists of four FET switches connected in parallel. They gate the four demodulation signals (A, $\overline{A}$, B and $\overline{B}$) onto a common output line. The switches are enabled singly and in a controlled sequence to commute the four AC signals into a rippled DC output level. This output serves as a reference voltage for the Speed Control FET Network.

The commutation process involves the selective gating of all positive or all negative peaks. Negative peaks are selected during forward head positioning operations and positive peaks are selected for reverse positioning operations.

The sequence in which the gates are enabled assures that adjacent peaks are selected so that the output signal is uninterrupted during the course of the head positioning operation.

Each switch is controlled by a separate input line. These gate control inputs, designated –PICK A, –PICK $\overline{A}$, –PICK B and –PICK $\overline{B}$, are provided by the CD Decode logic on AL2. This logic controls the sequencing of the PICK signals.

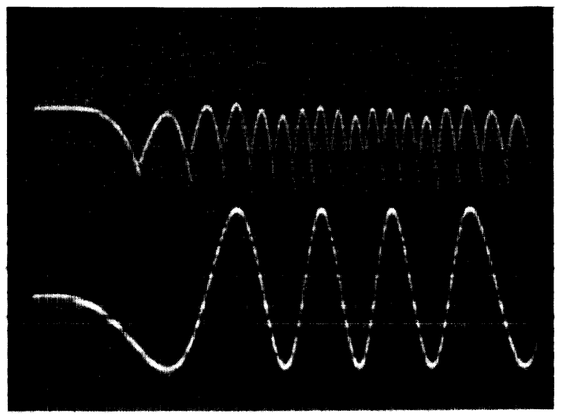


Figure 5-36. Reference FET Network Oscilloscope Trace

The relationship between the PICK inputs and the four demodulation envelopes is shown in Figure 5-18, Reference FET Network Input/Output Signals (see Section 5.2.4.8).

Just before the heads reach the detent position, the servo system enters the detent mode. This causes the CD Decode logic to interrupt its regular sequence of PICK signals. Instead, it continues to issue the most recent PICK signal and allows the selected demodulation envelope to approach its zero crossing.

When the servo system enters the detent mode, the DIRECTION CONTROL line on AL2 conditions the CD Decode logic for forward head motion. Consequently, when the Reference FET Network enters the detent mode during reverse head positioning, the selected envelope's positive slope becomes a negative slope.

The selected envelope's zero crossing marks the exact detent position for the heads. If the heads attempt to move away from this point, the network's output moves up or down the slope, adopting a negative amplitude if the heads move toward the spindle and a positive amplitude if they move away from the spindle.

The signal appearing at the common switch output is amplified by a non-inverting operational amplifier (J16-1). Figure 5-36 provides an oscilloscope photograph of one demodulation envelope and of the rippled DC level that results from commutating all four demodulation envelopes.

The amplifier's output is applied to the inputs of all nine switches in the Speed Control FET Network. It provides a constant voltage for that network to use as a reference for its output signal.

Whenever the heads are in motion, the Reference FET Network's output (TP3) has a nominal amplitude of 4V with respect to ground. Its polarity will be negative if the heads are moving toward the spindle and positive if the heads are moving away from the spindle.

When the heads are detented, the network's output is at zero potential.

5.3.13.3 Speed Control FET Network

This network consists of nine FET switches connected in parallel. All nine switches have common input and output points.

The rippled DC signal level generated by the Reference FET Network provides the source voltage for all the switches. Their common output consists of that portion of the reference signal that is gated through the network. The network's output signal serves as the speed control input to the main summing junction.

During head positioning operations, the amplitude of the speed control output is a direct function of the number of

switches that are enabled. Its polarity is the same as the polarity of the reference signal.

Eight of the nine switches are responsible for gating some portion of the reference signal through to the summing junction during head positioning operations. The distance the heads must move (number of cylinders) determines how many switches are active at a given time.

The relationship between the distance to be traveled and which switches are enabled is presented in Table 5-5. Travel distance is shown as the number of cylinders the heads must traverse.

Each switch is controlled by a separate input to the SO board. These gate control inputs, designated –MINIMUM SPEED and –SPEED INCR NO. 1 through –SPEED INCR NO. 7, originate at the Speed Increment Decoder on AL2.

When any –SPEED INCR NO. input is active, all lower order inputs (including –MINIMUM SPEED) are also active. During the course of a head positioning operation, these speed control inputs are removed one at a time, from the highest order to the lowest. –MINIMUM SPEED is the last speed control input to be removed.

TABLE 5-5.

Active Speed Control Switches vs. Head Travel Distance

CYLINDERS TO BE TRAVERSED		ACTIVE SWITCHES (See Note)
MODEL 43	MODEL 44	
64 or greater	128 or greater	Min. Speed and Speed Incr 1 through 7
32 to 63	64 to 127	Min. Speed and Speed Incr 1 through 6
16 to 31	32 to 63	Min. Speed and Speed Incr 1 through 5
8 to 15	16 to 31	Min. Speed and Speed Incr 1 through 4
4 to 7	8 to 15	Min. Speed and Speed Incr 1 through 3
2 or 3	4 to 7	Min. Speed and Speed Incr 1 and 2
1	2 or 3	Min. Speed and Speed Incr 1
1/2	1	Min. Speed

NOTE: Active switches are identified by input signal that controls switch gates.

A precision resistor is connected in series with the input pin of each switch (i.e., drain side of each FET). The values of these resistors are scaled to provide the appropriate voltage drop across the speed control network for each possible combination of active switches. That is, as the heads approach the destination cylinder and the speed control inputs are removed in sequence, the amplitude of the speed control output signal decreases by appropriate increments. Refer to Table 5-5 for this progression of speed control output voltage levels.

When the difference count equals zero, –MINIMUM SPEED is removed and –POS TERM goes true (low).

–POS TERM enables FET switch D48-2. This switch couples the reference signal to the speed control output.

When the heads are stationary, the reference input and the summing junction are both at zero potential. If the heads begin to move, the reference signal swings to approximately +4V (for reverse motion) or –4V (for forward motion). A 1.21 MΩ resistor in series with the switch provides a voltage drop across the network, causing an error voltage to develop at the output of amplifier J16-7. The polarity of this error signal is such that it causes the head positioning motor to move the heads back toward the detent position.

In Model 44 drives, the zero crossing of the detent slope may be offset in one direction or the other by the input TEMP COMP VOLTAGE. This signal level is the DC output of the TC board (M04). Its purpose is to adjust the servo system's electronic reference for detenting to compensate for dimensional changes in the servo system's mechanics caused by changes in the ambient temperature.

When the head positioning mechanism's ambient temperature is 25°C, TEMP COMP VOLTAGE is at 0V. The zero crossing of the detent slop is not offset. If the ambient temperature is between 25°C and 40°C, TEMP COMP VOLTAGE is positive, with an amplitude that is proportional to the value of the temperature with respect to 25°C. For temperatures between 10°C and 25°C, TEMP COMP VOLTAGE is negative, with an amplitude proportional to the temperature.

When TEMP COMP VOLTAGE goes positive, the position reference input to the summing junction is increased proportionally. This causes SERVO DRIVE SIGNAL to go negative, driving the head positioner toward the spindle. The heads move forward until the detent slope reaches the adjusted zero crossing, at which point the positioner is detented.

A negative level on the TEMP COMP VOLTAGE input has the opposite effect. The input to the summing junction goes below ground, causing a positive SERVO DRIVE SIGNAL. This moves the heads away from the spindle until the detent slope reaches the adjusted zero crossing.

5.3.13.4 Differential Circuits

These circuits differentiate the four demodulation envelopes (A, $\overline{A}$, B and $\overline{B}$) to produce velocity sensitive AC signals for use by the Feedback FET Network. The set of differentiated signals are designed A', $\overline{A}$', B' and $\overline{B}$'.

The important characteristic of these signals is that their amplitudes are directly proportional to the frequencies of their drive signals, which are, in turn, a direct function of actual head velocity.

A secondary characteristic of the differentiated signals is that they lead the input signal by 90°.

Control of the commutation process in the Feedback and Reference FET Networks compensates for this displacement by selecting undifferentiated and differentiated signals in phase-matched pairs. That is, A and A' are not selected at the same time. Instead, A and $\overline{B}$' are selected by their respective networks during forward head positioning, since they are in phase at that time.

Differentiation of each signal is performed by a capacitor, which is connected between the Demodulation Network output and the Feedback FET Network input. A precision resistor, in series with the capacitor and Feedback FET Network, determines the upper and lower limits of the amplitude of the differentiated signal.

Figure 5-37 provides an oscilloscope photograph of one Differential Circuit input/output signal pair ($\overline{A}$ and A'). The sampled wave forms represent a 24-cylinder seek.

5.3.13.5 Feedback FET Network

This network consists of four FET switches connected in parallel. They gate the four differentiated signals (A', $\overline{A}$', B' and $\overline{B}$') onto a common output line. The switches are enabled singly and in a controlled sequence to commute the four differentiated AC signals into a rectified analog output.

This output is used directly as the feedback input to the servo system's main summing junction.

As in the Reference FET Network, the commutation process involves the selective gating of all positive or all negative peaks. Positive peaks are selected during forward head positioning operations and negative peaks are selected for reverse head positioning.

Each switch is controlled separately by gate control signals issued by the CD control logic on AL2. These signals are labeled –Ø1, –Ø2, –Ø3 and –Ø4. The relationship between the four Ø inputs and the differentiated signals is shown in Figure 5-17, Feedback FET Network Input/Output Signals (see Section 5.2.4.8).

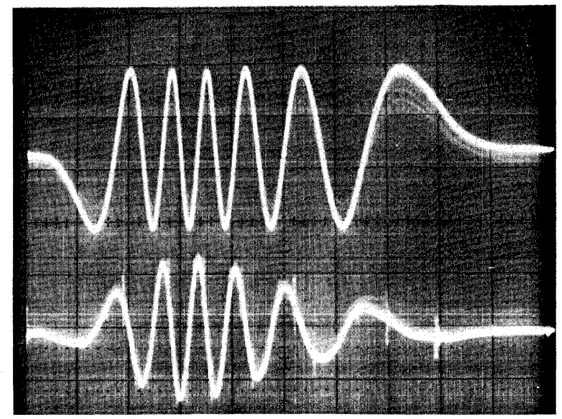


Figure 5-37. Differential Circuit Input/Output Signals

Since the amplitude of each differentiated input signal is determined by actual head speed, the amplitude of the network's output is a direct analog of head speed as well. However, since the network's output is one input to the main summing junction, there is no direct method of sampling the feedback term by itself. Instead, feedback velocity information is available from two of the differentiated inputs to the network (before commutation).

These signals are $\overline{A}$' and B', which can be sampled at TP19 and TP17, respectively.

5.3.13.6 C and D Summing Networks

The C and D Summing Networks develop a pair of phase-related square waves, which are designated SERVO LOGIC CONTROL LEVEL C and SERVO LOGIC CONTROL LEVEL D. These outputs result from voltage summing $\overline{A} \cdot \overline{B}$ and $\overline{A} \cdot B$, respectively.

The resulting summation signals are inverted and amplified by a pair of Schmitt triggers, J40-1 and J40-7.

SERVO LOGIC CONTROL LEVEL C and SERVO LOGIC CONTROL LEVEL D are phase shifted by 90° from one another. Theis phase displacement carries cylinder count information for the Present Address Counter Control Logic on AL1. It also provides sequence control information to the CD Decode logic on AL2 for use in generating PICK and Ø signals.

The amplified outputs of these networks have TTL logic levels. Their periods are directly related to head velocity.

5.3.13.7 Main Summing Junction

The outputs of the Speed Control FET Network is tied to the output of the Feedback FET Network at a voltage summing point. The potential appearing at that point is simply the algebraic sum of the speed control term and the feedback term.

When the amplitudes of the input terms are unmatched (i.e., their absolute values are not equal), a potential appears at the summing junction. Its polarity is the same as the polarity of the larger input term.

The resulting signal is inverted and amplified by operational amplifier J16-7. The output of J16-7 is designated SERVO DRIVE SIGNAL.

Figure 5-38 provides an oscilloscope photograph of SERVO DRIVE SIGNAL as it appears at TP5 on the SO board.

5.3.14 M/O-8, Address Logic 2 (AL2) PCB

The logic located on AL2 fits into two separate function categories, cylinder addressing and servo control. The AL2 board also contains the circuits that generate –READY TO S/R/W.

The cylinder addressing logic on AL2 consists of the Difference Count Multiplexor, Speed Increment Decoder and portions of the addressing control logic.

The CD Decoder is the portion of servo control logic that is located on AL2. This set of logic generates the gate control signals that operate the Reference and Feedback FET Networks on the Servo PCB.

5.3.14.1 Cylinder Addressing Logic

DIFFERENCE COUNT MULTIPLEXOR (B3 and H3)

The Difference Count Multiplexor receives the Subtractor's nine-bit difference count output in its true and complement forms. –DIRECTION CONTROL determines which set of inputs is selected.

A low level on –DIRECTION CONTROL (for forward) selects the true bits in all but the least significant bit position. The complement form of the least significant bit is selected by –DIRECTION CONTROL. When –DIRECTION CONTROL is high, the alternate bits are selected: the true form of the least significant bit and the set of complemented bits in the eight high-order bit positions.

SPEED INCREMENT DECODER

The selected outputs of the multiplexor gates are applied to the Speed Increment Decoder. This logic consists of a network of NAND gates and inverters, which are implemented as negative-logic OR gates, and an output stage consisting of positive-logic NAND gates.

During seek operations, the Speed Increment Decoder generates a minimum of one and a maximum of eight speed commands. These commands, designated –MINIMUM SPEED AND –SPEED INCREMENT 1 through –SPEED INCREMENT 7, are sent to the Servo where they control the gates of eight speed control FET switches.

The number of speed commands issued depends on the value of the difference count (that is, on the number of cylinders to be traversed). The relationship between the value of the different count and which speed commands are issued is shown in Table 5-6.

TABLE 5-6.
Distance vs. Speed Commands

DISTANCE COUNT		SPEED COMMANDS ISSUED
MODEL 43	MODEL 44	
64 or greater	128 or greater	Min. Speed and Speed Incr 1 through 7
32 to 63	64 to 127	Min. Speed and Speed Incr 1 through 6
16 to 31	32 to 63	Min. Speed and Speed Incr 1 through 5
8 to 15	16 to 31	Min. Speed and Speed Incr 1 through 4
4 to 7	8 to 15	Min. Speed and Speed Incr 1 through 3
2 or 3	4 to 7	Min. Speed and Speed Incr 1 and 2
1	2 or 3	Min. Speed and Speed Incr 1
0*	1	Min. Speed

*Represents a distance of 1/2 cylinder.

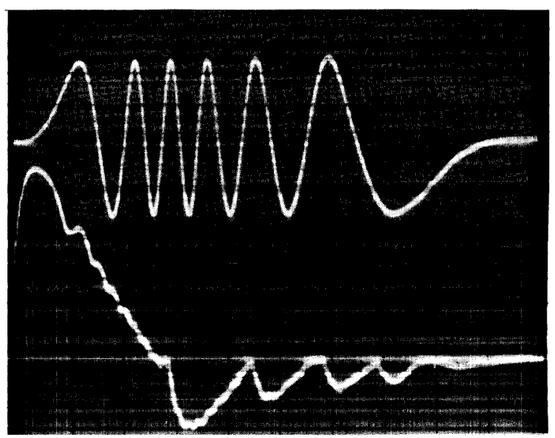


Figure 5-38. Servo Drive Signal Oscilloscope Trace

The active speed commands turn on their respective switches in the Servo's Speed Control FET Network. This results in a drive signal of the appropriate magnitude and polarity being applied to the head positioning motor. Refer to Section 5.3.13, Servo PCB, for details regarding the use of the speed commands by the Speed Control FET Network.

When the heads move from cylinder to cylinder, the difference count value decreases. Each time the difference count crosses one of the thresholds identified in Table 5-6, the highest order speed command that is active is disabled. This has the effect of decreasing head velocity.

Head velocity is incrementally decreased in the manner until the heads reach the destination cylinder. At that time the difference count equals zero (all +SUM BIT inputs to AL2 are false). All speed commands, including –MINIMUM SPEED are disabled.

When the heads reach the destination cylinder, –COUNTER INTERLOCK and –POSITION TERM go true (D27-12 and E27-3 go low). Head detenting occurs at this point.

–COUNTER INTERLOCK establishes the heads detented condition in the cylinder addressing logic. It disables the output stage of the Counter Control logic on AL1, blocking the generation of –COUNT UP FORWARD and –COUNT DOWN REVERSE pulses. –COUNTER INTERLOCK also causes D27-1 on AL1 (see sheet 1) to go high. This brings –DIRECTION CONTROL low (forward), which is the required state when the heads are detented.

The Speed Increment Decoder also provides speed control commands for head positioning operations other than seek operations. These include restore, retract and preload head advance operations. In each of these cases, the Speed Increment Decoder output is determined by output gate control logic rather than by the value of the difference count.

Except during head retract operations and the initial stage of preload head advance operations, –MINIMUM SPEED is the only speed command issued by the Speed Increment Decoder for these head positioning operations.

The presence of –MINIMUM SPEED is assured for each operation by +RETRACT SPEED being true. This input is inverted and applied to D27-2. The resulting high level at D27-12 is inverted at F15-2 and applied to the preset input of Seek FF, setting that flip-flop. The Q output of Seek FF gates the high level provided by D27-12 out to the Servo as –MINIMUM SPEED.

During the initial stage of preload head advance operations and throughout head retract operations, –MINIMUM SPEED is supplemented by two other speed control commands, –SPEED INCREMENT 1 and –SPEED INCREMENT 2.

These two other speed command outputs are needed during that portion of head retract operations when the heads are unloaded. The positioning motor requires more energy to overcome the friction caused by the heads riding in the unloaded position than is needed when the heads are loaded.

The need for these additional speed control commands also results from the fact that the head positioning motor is less effective when the carriage is moving (in either direction) near the fully retracted position. With the carriage in that vicinity, the positioning motor's coil is in a more attenuated flux field than when the carriage is closer to the disks.

NAND gate D27-8 controls the generation and gating of these speed control commands in response to these special requirements. The necessary conditions for enabling D27-8 are described below.

INPUT PIN	CONDITION
D27-9	+RETRACT SPEED – This input is true during initial reset, preload head advance and head retract operations. Details regarding the generation of +RETRACT SPEED are provided earlier in this section.
D27-10	+FILE READY – This input must be false. For these operations, +FILE READY goes false when +HEADS ARE LOADED goes false.
D27-11	B27-3 HIGH – The output of this gate is high when either –DIRECTION CONTROL is false or when –DISK PACK SAFETY is true. –DIRECTION CONTROL is false (indicating a requirement for reverse head motion) during initial reset and retract operations. –DISK PACK SAFETY is true when the carriage is close enough to the fully retracted position to activate the Disk Pack Safety switch.

The low level provided by D27-8 causes D27-6 to go high. This high level is propagated through the low order gates of the Speed Increment Decoder, generating –SPEED INCREMENT 2, –SPEED INCREMENT 1 and –MINIMUM SPEED.

The low level at D27-8 also causes H15-11 to go high, which gates –SPEED INCREMENT 2 and –SPEED INCREMENT 1 through F3-8 and F3-11. Details regarding the gating of Speed Increment Decoder outputs are provided in the following subsection.

CYLINDER ADDRESSING CONTROL

The cylinder addressing logic on AL2 performs the following functions:

1. Controls gating of –SPEED INCREMENT commands.

2. Generates +INPUT INHIBIT signal when required.

During seek operations, the –MINIMUM SPEED output gate is enabled when Seek FF is set. Gating for –SPEED INCREMENT 1 through –SPEED INCREMENT 7 requires +RETRACT SPEED to be false as well as Seek F/F being set.

Seek F/F is set whenever the difference count value in the Speed Increment Decoder is greater than zero. This condition causes D27-12 to go high; that high level is inverted by F15-2 and applied to the preset input of Seek F/F, setting that flip-flop. Seek F/F remains set for the duration of the seek; that is, as long as the difference count is greater than zero and D27-12 is high.

At the conclusion of a seek operation, when the difference count value equals zero, D27-12 goes low. This removes the preset condition at Seek F/F; it also causes Settling OS-1 to fire. Settling OS-1 provides a delay period to allow any mechanical oscillations that accompany the detenting operation to settle out.

The trailing edge of the Settling OS-1 pulse clocks Seek F/F, resetting it. Seek F/F's Q output disables E27-8. The resulting high level at E27-8 is inverted and disables the five most significant Speed Increment Decoder outputs.

Except during the initial stage of a preload head advance operation and during the entire head retract operation, the high level at E27-8 also causes H15-11 to disable the two least significant Speed Increment Decoder output gates, Exceptions to this gating control are described below.

–MINIMUM SPEED is gated out to the Servo for all head positioning operations, including restore, retract and preload head advance operations. Control of the –MINIMUM SPEED gate is provided by Seek F/F.

During the initial stage of preload head advance and throughout head retract operations, –SPEED INCREMENT 1 and –SPEED INCREMENT 2 are gated out to the Servo. NAND gate D27-8 controls this special gating activity. Details regarding the operation of D27-8 are provided in the previous subsection, which is headed SPEED INCREMENT DECODER.

5.3.14.2 CD Decode

During head positioning operations the CD Decode logic generates two sets of control pulses. One set, designated –Ø1, –Ø2, –Ø3 and –Ø4, controls the commutation process in the Feedback FET Network. The other set, designated –PICK A, –PICK $\overline{A}$, –PICK B and –PICK $\overline{B}$ controls the commutation process in the Reference FET Network. Use of these outputs is described in Section 5.2.4.7, Feedback FET Network and Section 5.2.4.9, Reference FET Network.

All eight outputs originate at a set of AND gates, which decode the four possible combinations of CONTROL LEVEL C and CONTROL LEVEL D. CONTROL LEVEL C and CONTROL LEVEL D are the outputs of summing networks in the servo system. CONTROL LEVEL C is the square wave that results from summing the $\overline{A}$ and $\overline{B}$ demodulation envelopes. CONTROL LEVEL D, which has a 90° phase shift with respect to CONTROL LEVEL C, is the squared sum of $\overline{A}$ and B. Both C and D are inverted following the summing operation.

As the heads move from cylinder to cylinder, the level transitions occurring on CONTROL LEVEL C and CONTROL LEVEL D enable one decode gate after another. The sequence in which these gates are enabled depends on the direction of head travel.

FORWARD SEQUENCE

$\overline{C}D$ (H27-3) → CD (H27-6) → $C\overline{D}$ (H27-8) → $\overline{C}\overline{D}$ (H27-11) → $\overline{C}D$ (H27-3)

REVERSE SEQUENCE

In Model 43 drives (100 tpi), $\overline{C}D$ and $C\overline{D}$ are the only two possible starting points for these sequences. In Model 44 drives (200 tpi), all four combinations are starting points for forward or reverse sequences. The reason for this difference is that there are twice as many detent positions in Model 44 drives.

The outputs of these decode gates are inverted by four NAND gates to produce the –Ø1 through –Ø4 pulses.

FORWARD SEQUENCE

CD (Ø1) → CD (Ø2) → CD (Ø3) → CD (Ø4)

REVERSE SEQUENCE

Use of these pulses is illustrated in Figure 5-17, Feedback FET Network Input/Output Signals, which is part of Section 5.2.4.7.

Generation of the four PICK outputs from the various CD combinations requires two stages of multiplexing (devices F39 and H39).

The first four-pair multiplexor (F39) provides one sequence of PICK outputs for forward head positioning operations and another sequence for reverse operations. –DIRECTION CONTROL (AL2 pin E) performs the select function; its low state selects the CD combination inputs in the proper sequence for forward operations.

FORWARD SEQUENCE
(AL2 Pin E Low)

$\overline{C}D$ (Pick B) → CD (Pick A) → $C\overline{D}$ (Pick B) → $\overline{C}\overline{D}$ (Pick A)

REVERSE SEQUENCE
(AL2 Pin E High)

$\overline{C}D$ (Pick $\overline{B}$) ← $\overline{C}\overline{D}$ (Pick $\overline{A}$) ← $C\overline{D}$ (Pick B) ← CD (Pick A)

Different PICK sequences are required to assure proper commutation of the four demodulation envelopes (A, $\overline{A}$, B and $\overline{B}$) for each direction of head motion. Adjacent negative envelope peaks are selected in the commutation process during forward head motion. Adjacent positive envelope peaks are selected in the commutation process during reverse head motion.

Use of the PICK outputs during head positioning operations is illustrated in Figure 5-18, Reference FET Network Input/Output Signals, which is part of Section 5.2.4.9.

The second multiplexing device (H39) selects between two sources for the PICK outputs.

One source is the first multiplexing stage described above. Its outputs are used while the heads are being moved from one cylinder location to another. As previously described, these outputs consist of a selected sequence of CD combinations.

The other source is a set of AND gates which decode the four possible combinations of +BIT 1 and +BIT 2. These are the two least significant outputs of the Present Address Counter on AL1. The outputs of these AND gates are selected by H39 when the heads are about to be detented.

The select input to H39 is controlled by –COUNTER INTERLOCK, inverted. The BIT 1/BIT 2 combination inputs are selected when –COUNTER INTERLOCK goes true (AL2 pin A goes low).

Each of the four BIT 1/BIT 2 combinations generates a separate PICK output. The relationships between the four combinations and the four PICK outputs are shown in the following chart. These relationships are also illustrated in Figure 5-18, Reference FET Network Input/Output Signals (see Section 5.2.4.9).

	+BIT 1 (AL2 Pin 5)	+BIT 2 (AL2 Pin R)
–PICK A	Low	High
–PICK B*	High	High
–PICK $\overline{A}$	Low	Low
–PICK $\overline{B}$*	High	Low

When the heads are being detented, the Reference FET Network uses the active PICK output to select the corresponding demodulation wave shape. For detenting, the wave shape selected is the one that is approaching the zero crossover on its positive slope (i.e., positive from the forward direction viewpoint).

In Model 43 drives, –PICK B and –PICK $\overline{B}$ outputs are not used for detenting. They are not used because there are no actual detent positions that correspond to the positive zero crossover points on the B and $\overline{B}$ demodulation envelopes. These PICK outputs are disabled in the detent mode by grounding their inputs to H39. Jumpers J54 and J56 are removed and jumpers J55 and J57 are installed.

Details regarding the use of the PICK outputs for detenting are given in Section 5.2.4.9, Reference FET Network and Section 5.3.13, Servo PCB.

*These outputs are *not* used in Model 43 drives.

5.3.15 M/O-9, Address Logic 1 (AL1) PCB

Most of the logic responsible for cylinder addressing is located on the AL1 PCB. These functions include the Address Inhibit Gates, Address Check Logic, Destination Address Register, Present Address Counter, Subtractor, and major portions of the Cylinder Addressing Control Logic.

5.3.15.1 Address Inhibit Gates

The Address Inhibit Gates consist of nine 380 type NOR gates, which are implemented as negative-logic NAND gates.

The address bit inputs to these gates are provided by the Cylinder Address Receiver logic on RDR2. For Model 43 drives, these inputs are assigned bit values in the range 0 to 128 and for Model 44 drives, the bit values are from 1 to 256.

+INPUT INHIBIT controls propagation of the address through these gates. When +INPUT INHIBIT is false (low), the address bits are gated through (inverted). If +INPUT INHIBIT goes true, the outputs of all nine gates are held low, which represents the logical ZERO state at this point in the propagation path.

+INPUT INHIBIT is the inverted $\overline{Q}$ output of Carriage Positioning FF-2. These circuits are located on AL2 and described in Section 5.3.14. +INPUT INHIBIT is generated whenever the heads are moved to cylinder 0 (restored) or are retracted from the disk area. These events result from +RETRACT SPEED going high. The conditions that can cause +RETRACT SPEED are identified in Section 5.3.15.6.

5.3.15.2 Address Check Logic

Three NAND gates (with one implemented as a negative-logic NOR gate) and two inverters form the network that tests the value of the address word present at the Address Inhibit Gates. This network generates a low level output if the address value exceeds the limit for that drive model. An address is illegal if it equals 204 or greater (Model 43 drives) or 408 or greater (Model 44 drives).

If an illegal address is detected, the output gate of the Address Check Logic, D15-8, applies a low level to F15-2 and B39-12.

The low level at F15-2 blocks the clock pulse generated at one-shot H39-13. Blocking this clock pulse prevents the illegal address from being strobed into the Destination Address Register. Operation of H39-13 is described in Section 5.3.15.6.

The low level at flip-flop B39-12 causes that flip-flop to be reset by the leading edge of the pulse generated at H39-13. Resetting B39-9/8 causes –ADDRESS ACKNOWLEDGE OUTPUT to go false (high) and –LOGICAL ADDRESS INTERLOCK output to go true (low).

5.3.15.3 Destination Address Register

During seek operations, this nine-bit register holds the address of the cylinder to which the heads are to be moved. The destination address is loaded into the register at the beginning of the seek. During restore operations, all nine inputs to the register are forced to the logical ZERO state.

The least significant bit position in the register is a D-type flip-flop that clocks on the positive-going edge of the strobe provided by the controller. In Model 43 drives, the input to this flip-flop is held disabled (jumper D3 is not installed) so that the register's least significant output bit is always a logical ZERO. In Model 44 drives, the least significant input is part of the cylinder address received from the controller; its state depends on the value of the destination address.

The register's output is taken from the $\overline{Q}$ side of each flip-flop so that it represents the complement of the address received from the controller.

This complemented address is sent to the Subtractor logic where it is added to the true output of the Present Address Counter.

5.3.15.4 Present Address Counter and Counter Control

This nine-bit up/down counter serves as a real time register for the address of the present location of the read/write heads. As the heads change location during a seek, the contents of this counter change concurrently to continuously reflect the present location of the heads. This counter is shown on Sheet 2 of the AL1 logic diagram.

The most significant stage of the counter is provided by a JK flip-flop. The other eight stages consist of a pair of four-bit binary counter devices, connected in series.

The counter is cleared by +RETRACT SPEED; this signal is generated whenever the heads are moved to a cylinder 0 or are retracted.

During forward seeks, the counter is incremented by the trailing edge of –COUNT UP FORWARD pulses. –COUNT DOWN REVERSE pulses decrement the counter during reverse seeks. These increment and decrement commands are generated by the Counter Control Logic (shown on Sheet 1 of the AL1 logic diagram as well as in Figure 5-39).

The output stage of the counter control logic consists of a pair of two-input NAND gates, F15-8 and F15-11. One input of each gate is controlled by –COUNTER INTERLOCK and the other input receives the output of one-half of a phase-relationship decode network.

–COUNTER INTERLOCK, which originates on AL2, disables both F15-8 and F15-11 when it is true (low). This level is generated whenever there is no requirement for head movement. That is, –COUNTER INTERLOCK prevents the generation of –COUNT UP FORWARD or –COUNT DOWN REVERSE pulses whenever the contents of the Destination Address Register equal the value of the Present Address Counter. +RETRACT SPEED will also cause –COUNTER INTERLOCK to be true. This presents the generation of count pulses during any head positioning operation that is not a seek.

The decode logic examines the relative states of a pair of phase-related pulses, which are designated SERVO LOGIC CONTROL LEVEL "C" and SERVO LOGIC CONTROL LEVEL "D". These pulses, which are generated by logic on the Servo PCB, provide position and direction information about the read/write heads as the heads move from cylinder to cylinder. This information is used by the counter control logic to determine which direction the heads are moving in and to detect each arrival of the heads at a new cylinder.

The decode network consists of NAND and NOR gates and inverters; four of the inverter functions are performed by NOR gates.

Each of the four D51 NOR gates generates a positive pulse as a result of a level transition of either SERVO LOGIC CONTROL LEVEL "C" or SERVO LOGIC CONTROL LEVEL "D". The gate/transition relationship is shown below:

Gate	Transition
D51-3	High to Low of "C"
D51-2	Low to High of "C"
D51-14	High to Low of "D"
D51-13	Low to High of "D"

The RC delays at the outputs of F51-3, F51-2, F51-14 and F51-13 determine the pulse durations. The component values are selected to produce 1μs pulse widths.

Each of the D51 pulse outputs is applied to a pair of two-input NAND gates. For example, D51-3 is applied to gates A39-3 and A39-6. A39-3, which is part of the –COUNT UP FORWARD path, is gated by the inverted form of SERVO LOGIC CONTROL LEVEL "D". A39-6 generates pulses only during reverse seeks and is gated by the true form of SERVO LOGIC CONTROL LEVEL "D".

The sequential relationship of SERVO LOGIC CONTROL LEVEL "C" and SERVO LOGIC CONTROL LEVEL "D" provides a time mask to the A39 and B51 NAND gates. For example, during forward seeks, D51-3 pulses occur only when SERVO LOGIC CONTROL LEVEL "D" is false. Consequently, pulses caused by high-to-low transitions of SERVO LOGIC CONTROL LEVEL "C" are propagated through A39-3, A51-6 and F15-11 during forward seeks.

In the same manner, D51-3 pulses coincide with SERVO LOGIC CONTROL LEVEL "D" during reverse seeks. At that time, those pulses are routed through A39-6, A51-8 and F15-8 to become –COUNT DOWN REVERSE pulses.

There are eight NAND gates that are part of the same functional set as A39-3; four are associated with the –COUNT UP FORWARD path and four are part of the –COUNT DOWN REVERSE path. The following lists indicate the relative status of SERVO LOGIC CONTROL LEVEL "C" and SERVO LOGIC CONTROL LEVEL "D" required to produce pulses at these gates during forward and reverse seeks:

Fwd Seek Gates	"C" · "D" STATES
A39-3	$C\downarrow \cdot \overline{D}$
A37-8	$C\uparrow \cdot D$
B51-3	$C\uparrow \cdot \overline{D}$
B51-8	$C\downarrow \cdot D$

Rev Seek Gates	"C" · "D" STATES
A39-6	$\overline{C} \cdot D\uparrow$
A39-11	$C \cdot D\downarrow$
B51-6	$\overline{C} \cdot D\downarrow$
B51-11	$C \cdot D\uparrow$

$\uparrow$ = low-to-high transition
$\downarrow$ = high-to-low transition

5.3.15.5 Subtractor

This functional element adds the two's complement of the Destination Address Register to the contents of the Present Address Counter to determine the number of cylinders the heads must move to reach the cylinder specified by the controller. The direction of the move is determined by the logic level of the carry out term: low means forward and high means reverse.

A set of NAND gates (shown on Sheet 1 of AL1) adds the register's complemented least significant bit and the end around carry bit provided by the higher order adder circuits to the counter's least significant bit.

The output stage of this full adder network consists of H51-8 and E27-8. H51-8 produces the least significant sum bit. In Model 43 drives, this output is designated +SUM BIT "0"; in Model 44 drives, it's +SUM BIT "1". E27-8 provides the carry out bit that results from the addition; this output is forwarded to the higher order Subtractor circuits (shown on Sheet 2).

Two interconnected, four-bit binary full adder devices perform the subtraction function for the other eight bit positions. These devices are J15 and A15.

A15-14 is the final carry out term in the Subtractor circuit. It is routed to the least significant adder circuit to convert the Destination Address Register output from one's complement to two's complement. It is also sent to a direction control gate (shown on Sheet 1), which issues either a forward or reverse DIRECTION CONTROL command, depending on the state of the carry out bit. If A15-14 is low, forward motion is specified.

If the seek requires forward motion, the Subtractor's sum bit output directly represents the number of cylinders to be moved. If a reverse seek is specified, the complement of the sum bit output equals the length of the seek.

Each Subtractor output is applied to the Difference Count Multiplexor in its true and complemented forms. Selection of the appropriate set of sum bits by the multiplexor is controlled by the DIRECTION CONTROL line. The Difference Count Multiplexor is located on AL2; functional elements on the PCB are discussed in Section 5.3.14.

5.3.15.6 Cylinder Address Control Logic

The cylinder addressing control logic located on AL1 is responsible for the following control functions:

- Strobes the new address into the Destination Address Register
- Generates –DIRECTION CONTROL and +RETRACT SPEED commands
- Controls reverse speed command to Servo during and after the initial reset period

ADDRESS STROBE

The Destination Address Register strobe originates at one-shot H39A-13 (shown on Sheet 2 of AL1). H39A-13 is fired by the leading edge of –SELECTED STROBE LINE if either –READY TO S/R/W or –SELECTED RESTORE LINE is true (low). Its generation is described separately for the two conditions.

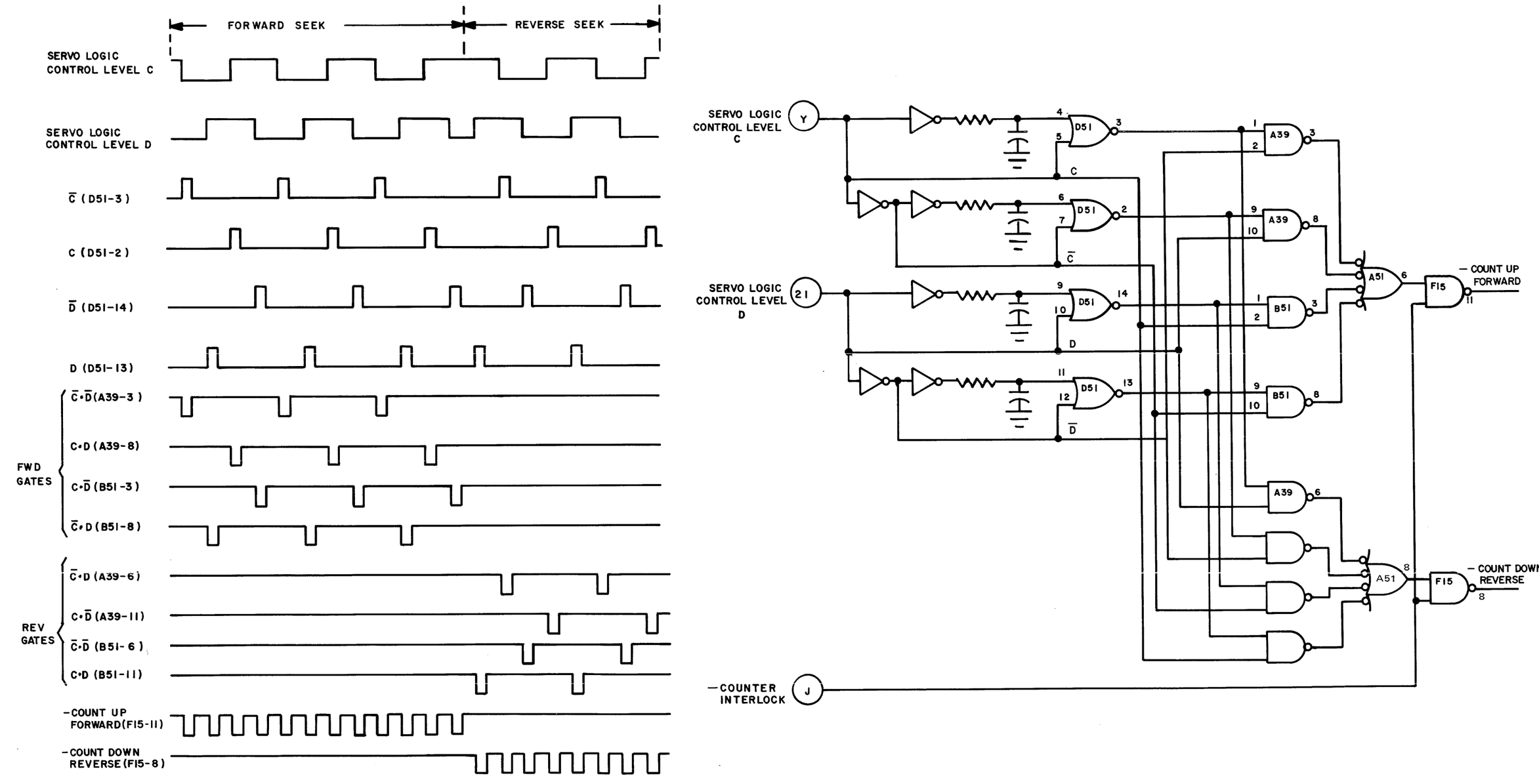


Figure 5-39. Present Address Counter Control Logic and Control Timing

READY TO S/R/W

At the start of a seek operation, –READY TO S/R/W is true and –SELECTED RESTORE LINE is false. The first signal is provided by status logic on AL2; it is true only when all the following requirements are met:

- Carriage Positioning FF-2 is reset.
- Seek FF is reset.
- +FILE READY is true.
- –SEEK INCOMPLETE is false.

These preconditions, which are required for a successful seek operation, are discussed in detail in Section 5.3.14, Address Logic 2.

–SELECTED RESTORE LINE is true only when the controller intends to initiate a restore operation. It must be false for the destination address supplied by the controller to be propagated through the Address Inhibit Gates.

With –READY TO S/R/W true, the leading edge of –SELECTED STROBE LINE enables E15-3. The resulting high level at H39-2 fires the one-shot.

SELECTED RESTORE LINE

–SELECTED RESTORE LINE is true (low level at E15-6) at the start of a restore operation. This allows the leading edge of –SELECTED STROBE LINE to enable E15-2.

The high level generated at E15-2 is inverted by B27-6 and then applied to E27-12. The resulting high level at E27-11 is inverted and applied to E15-4. This gates –SELECTED STROBE LINE through E15-3, firing the clock pulse one-shot.

The pulse issued by E27-3 clocks nine ZERO bits into the Destination Address Register. The ZERO state of these bits is imposed by the high level on +INPUT INHIBIT. The origin of +INPUT INHIBIT is discussed in Section 5.3.14, Address Logic 2.

Since the ZERO output of the Address Inhibit Gates is within the legal range, the high output of the Address Check Logic (at D15-8) gates the pulse generated by the one-shot through F15-3. The low pulse at F15-3 is inverted by E27-3 and applied to the clock inputs of the Destination Address Register.

If –RETRACT SPEED is true (low level at E27-1), E27-3 is held high so the clock pulse is blocked. –RETRACT SPEED will be true during restore operations and when the heads are being retracted.

DIRECTION CONTROL

–DIRECTION CONTROL serves as the select input to the Difference Count Multiplexor. The logic level present on this line determines which set of Subtractor output bits are gated through the multiplexing logic, the true or complemented output. The state of –DIRECTION CONTROL is determined by D27-6.

This point is low under three different circumstances: 1) when the heads are moved from the retracted position to the load position (called preload head advance) 2) when a forward seek is required and 3) while the heads are detented in position between seeks. Each of these circumstances is represented by all four inputs to D27-6 being high. The conditions that bring this about are described below:

INPUT PIN	CONDITION
D27-1	PRELOAD HEAD ADVANCE – When +SPINDLE DRIVE ON force sets Carriage Positioning FF-1, +RETRACT SPEED goes true. This causes D15-6 to go high (see Sheet 2) and, consequently, D27-1 to go high.
D27-1	FORWARD SEEK – The Subtractor's carry out bit goes high whenever the drive is instructed to move the heads from a higher address cylinder to a lower address cylinder. This low enables D15-6, which causes D27-1 to go low. The carry out bit is low at all other times.
D27-1	HEADS DETENTED – When no seek is required, the Subtractor's difference count output equals zero. This causes –COUNTER INTERLOCK to go low (see AL2). –COUNTER INTERLOCK enables D15-6, which causes D27-1 to go high. Since the Subtractor's carry out bit is low at this time, it serves as a redundant influence on D27-1.
D27-2	A3-6 IS HIGH – This gate is enabled only during restore operations. Although A3-4 is high during preload head advance, +HEADS OVER TRACKS is false, disabling A3-6.
D27-4	A3-11 IS HIGH – This point is low only when power to the spindle motor is lost (+SPINDLE DRIVE ON is low) while the heads are in the disk area. A low level at A3-11 causes the heads to retract.
D27-5	–INITIAL RESET IS HIGH – This input is low for 120 ms when the drive is first turned on.

When any one of the four inputs to D27-6 is low, –DIRECTION CONTROL is high, representing a reverse motion requirement. This can occur under four different circumstances: 1) while –INITIAL RESET is true; 2) when a reverse seek is required; 3) when a restore operation is required and 4) when the heads must be retracted from the disk area. The conditions that can cause –DIRECTION CONTROL to go high are identified below.

INPUT PIN	CONDITION
D27-1	REVERSE SEEK – The Subtractor's carry out bit goes high whenever the drive is instructed to move the heads from a higher address cylinder to a lower address cylinder. Since +RETRACT SPEED and –COUNTER INTERLOCK are both false at this time, D15-6 goes low, causing D27-1 to go low. –COUNTER INTERLOCK is true only when the Subtractor's output equals zero or when +RETRACT SPEED is true. +RETRACT SPEED cannot be true during any seek; this is explained in the following subsection, headed RETRACT SPEED.
D27-2	RESTORE OPERATION – Whenever the drive is instructed to restore the heads to cylinder 0, inverter F39-8 goes low, setting Carriage Positioning FF-1. This applies a high level to A3-4. Since restore operations occur only when the heads are in the disk area, +HEADS OVER TRACKS is true at this time, causing A3-6 to apply a low level to D27-2.
D27-4	HEAD RETRACT OPERATION – If +SPINDLE DRIVE ON goes false while the heads are in the disk area (–HEAD RETRACTED is false), A3-11 goes low. This disables D27-6, causing –DIRECTION CONTROL to go high.
D27-5	INITIAL RESET – The –INITIAL RESET pulse that occurs when the drive is first turned on holds D27-5 low for the duration of the pulse.

RETRACT SPEED

+RETRACT SPEED originates at D27-8 (see Sheet 1) and is active during initial reset, preload head advance, restore and retract operations. The conditions that bring about +RETRACT SPEED are described below:

INPUT PIN	CONDITION
D27-9, 13	PRELOAD HEAD ADVANCE – When power is applied to the spindle drive and the spindle reaches the minimum operating speed, +SPINDLE DRIVE ON goes true. This low to high transition causes a positive-going pulse to occur at E15-13; the pulse is inverted and force sets Carriage Positioning FF-1. The resulting low level at the flip-flop's Q output causes +RETRACT SPEED to go true, which initiates the preload head advance operation.
D27-9, 13	RESTORE – Whenever the drive is instructed to restore the heads to cylinder 0, inverter F39-8 goes low, setting Carriage Positioning FF-1. Setting this flip-flop causes +RETRACT SPEED to go true. The role performed by +RETRACT SPEED in restore operations is described below.
D27-10	INITIAL RESET – When power is first applied to the drive, –INITIAL RESET goes low for approximately 120 ms. –INITIAL RESET is received by the AL1 card at pin 8 (see Sheet 2).
D27-12	RETRACT OPERATION – If +SPINDLE DRIVE ON goes false while the heads are over the disks (–HEAD RETRACTED is false), A3-11 goes low. This enables D27-8, which causes +RETRACT SPEED to initiate a retract operation.

+RETRACT SPEED performs a number of functions for cylinder addressing logic on both AL1 and AL2. These functions are identified below:

1. Causes the Speed Increment Decode logic on AL2 to issue a speed command (–MINIMUM SPEED) to the Servo.
2. Prevents the AL2 Speed Increment Decode logic from generating the seven higher speed commands, –SPEED INCREMENT 1 through –SPEED INCREMENT 7.
3. Sets Carriage Positioning FF-2 on AL2, causing +INPUT INHIBIT to go true and –READY TO S/R/W to go false. +INPUT INHIBIT forces the data inputs to the Destination Address Register to the ZERO state.
4. During preload head advance operations, participates in the generation of –DIRECTION CONTROL. +RETRACT SPEED does this by enabling D15-6 (see Sheet 2 of AL1), which causes D27-1 to go high. The other requirements for –DIRECTION CONTROL during preload head advance operations are provided in the preceding subsection, headed DIRECTION CONTROL.
5. Disables the clock inputs to the Destination Address Register and clears the Present Address Counter.

5.3.16A Heat Sink (HS) PCB No. 11631

The circuits located on this board fit into six distinct functional categories.

1. Spindle Driver
2. +15V, –15V Regulator
3. Power Driver Circuits (Servo)
4. Brush Motor Driver

5. Drawer Unlock Solenoid Pick

6. Head Load Solenoid Pick

NOTE

In all circuits shown in the logic diagram, the double weight lines indicate high current paths.

5.3.16.1 Spindle Driver

This section consists of a pair of push-pull transistor networks. Each network supplies alternating current to a separate winding on the spindle motor.

Four phase-related square wave signals control the two networks. Two of the signals, designated PHASE 1A and PHASE 1B operate one network. The other network is controlled by PHASE 2A and PHASE 2B. All four signals originate on the OR board.

PHASE 1A and PHASE 2A are phase-shifted by 90° from one another. PHASE 1B is the complement of PHASE 1A and PHASE 2B is the complement of PHASE 2A. Each square wave has a peak-to-peak swing of 14V.

The positive half cycle of PHASE 1A produces +24V at P7-1; simultaneously, the negative half cycle of PHASE 1B produces −24V at P7-3. Current flows through the spindle winding.

When both signals cross zero voltage at the end of the half cycle, the current flowing between P7-1 and P7-3 changes polarity.

PHASE 2A and PHASE 2B control the other network in the same fashion.

5.3.16.2 ± 15V Regulator

This circuit developes regulated +15V and −15V from the +24V and −24V circuit voltage.

5.3.16.3 Power Driver Circuits

Current for the head positioning motor is provided by a push-pull network similar to the one used in the Spindle Driver. The major functional difference in this network is that the current developed is directly proportional to the amplitude of the drive signal.

This reference input, designated SERVO DRIVE SIGNAL, is an analog signal produced by the SO board. When positive, SERVO DRVIE SIGNAL turns on the upper half of the network. A negative potential at B82-7 turns on the lower half of the network.

When the heads are detented, any motion of the heads away from the detent position causes SERVO DRIVE SIGNAL to take on a positive or negative amplitude. If the heads move toward the spindle, SERVO DRIVE SIGNAL becomes positive. Head motion in the other direction causes SERVO DRIVE SIGNAL to become negative. In either case, the resulting current opposes the motion away from the detent position.

The motor can be freed from the control of SERVO DRIVE SIGNAL in either one of two ways. If the High Current Detector circuit senses excessive current at one of the head positioning motor terminals, logic on the SR board generates −SERVO DISABLE. A low level (ground) on this line neutralizes the Power Driver Circuits, allowing the motor to move freely. The same affect can be achieved by pressing the Servo Release Switch.

5.3.16.4 Brush Motor Driver

Two phase-related input signals, BRUSH MOTOR A and BRUSH MOTOR B, drive this circuit, producing alternating current for the brush motor.

BRUSH MOTOR A consists entirely of positive half cycles of a 60 Hz square wave. BRUSH MOTOR B consists of negative half cycles of a 60 HZ square wave. Since the two rectified signals are phase shifted from one another by 180°, together they comprise a single 60 Hz square wave.

5.3.16.5 Drawer Unlock Solenoid Pick

This circuit provides the high current needed to pick the solenoid that unlocks the cabinet drawer as well as the low level holding current.

One side of the solenoid is permanently held at +24V.

When +DRAWER UNLOCK PICK goes high it provides a high current path to ground through transistor J10-2 for approximately 700 msec.

−DRAWER UNLOCK ENABLE, which went low when +DRAWER UNLOCK PICK went high, provides a path for holding current when +DRAWER UNLOCK PICK times out. This low current path is through J97 to ground.

The LOAD light is on any time the solenoid is energized.

5.3.16.6 Head Load Solenoid Pick

This circuit supplies both pick and holding current to the Head Load Solenoid.

One side of the solenoid is tied to +24V.

When +HEAD LOAD PICK goes high, path for high pick current is provided through transistor J80 to −24V.

When +HEAD LOAD PICK goes low, −HEAD LOAD ENABLE provides a path for the holding current through J112 to ground.

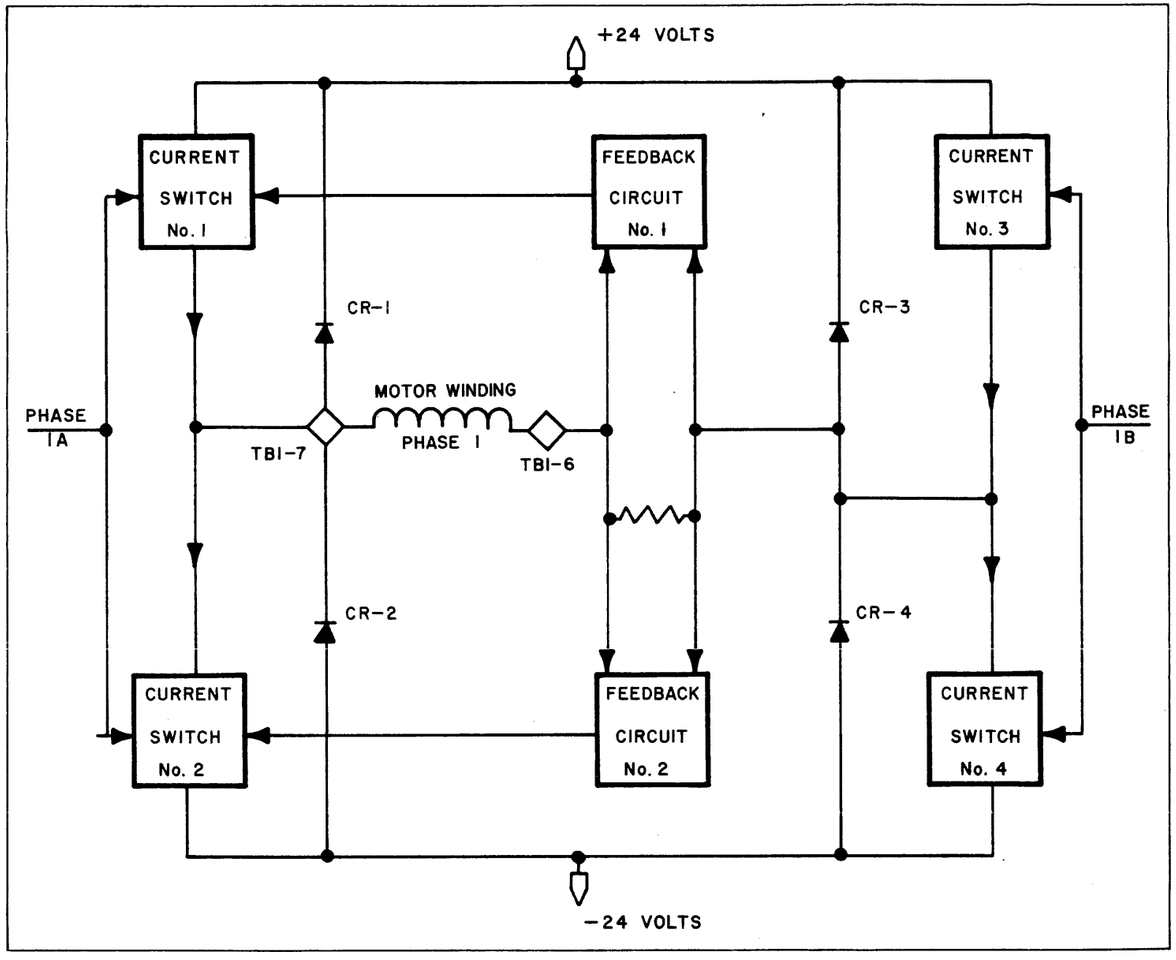


Figure 5-39A. Phase ! Spindle Motor Driver

5.3.16B Heat Sink (HS) PCB No. 11890

The Heat Sink PCB, P/N 11890, consists of the following logical sections:

1. Spindle Motor Driver
2. Positioner Motor Driver
3. Brush Motor Driver
4. Positive and Negative 15 Volt Tracking Regulator
5. Drawer and Head Load Solenoid Drivers
6. Braking (Speed Sense) Timer

5.3.16.1 Spindle Motor Driver

The spindle motor is a synchronous AC induction motor with two stator windings phased 90 electrical degrees apart. The inputs to the stator winding drivers are trapezoidal waveforms with amplitudes of +7V to −7V when the motor is being driven. During the LOAD function of the disk drive, the inputs to the drivers are maintained at 0V to ± 0.8V, permitting no current to flow in the two stator windings. Braking in the motor is accomplished by applying a DC signal to the Phase 1 winding and turning "off" the Phase 2 winding drive. Power dissipation in the motor and driver circuits is limited through the use of a switching current regulator.

The signals applied to the Phase 1A and Phase 1B inputs are complementary as are the signals applied to the Phase 2A and

Phase 2B inputs. The Phase 1 signals are in quadrature (different by 90 degrees) with the Phase 2 signals.

A block diagram of the driver for a single stator winding is shown in Figure 5-39A. This driver consists of four current switches, a current sense resistor, four "free wheeling" diodes and two current feedback circuits. Circuit operation is described in the following paragraphs.

With a positive signal applied to input Phase 1A, current switch 1 is turned "on" applying +24V to motor winding terminal TB1-7. Simultaneously, a negative signal is applied to input Phase 1B, turning "on" current switch 4. As current builds up in the motor winding, a voltage appears across the current sense resistor proportional to the current in the motor winding. When this voltage reaches approximately 0.7V the action of current feedback circuit 1 causes current switch 1 to be turned "off". Motor winding terminal TB1-7 voltage switches from +24V to approximately −24V, where it is limited by current flowing through diode CR2. As the decreasing current flow through the current sense resistor reaches the lower feedback threshold, current switch 1 is again turned "on" repeating the cycle. This action continues as long as the input to Phase 1A remains positive and the input to Phase 1B remains negative, limiting the current to an average value of 4A. Current switch 2, current feedback circuit 2, diode CR1 and the current sense resistor perform this current limiting function for the complemented inputs.

Additional current limiting is provided in the circuitry of current switches 3 and 4 at approximately 4.7A to protect the power devices from overstressing in the event of a component failure.

CAUTION

Probing of the Heat Sink Circuit Board with power applied should be avoided because of the danger of accidental shorts which may destroy a power stage. Operation of the Driver Circuits with a non-inductive dummy load will result in excessive dissipation in the switching current regulator circuit due to the increased switching frequency.

No adjustments are required to the Spindle Motor Driver circuits and no restrictions apply to the input signal duration as long as the power devices are correctly mounted on the Heat Sink. The action of the switching current regulator reduces the device dissipation since the devices are in saturation, dissipating little power, or cut off, dissipating no power. The primary power dissipation occurs while the device is switching.

Pertinent waveforms are indicated in Figure 5-39B. The Phase 1A voltage waveform shows the typical trapezoidal input waveform as a solid line and minimum limit as a dotted line for the motor drive signal. Motor winding terminal TB1-6 indicates the expected signal at this terminal for the above input waveform. Motor winding terminal TB1-7 indicates the expected voltage signal on this terminal as the motor builds up speed. As the motor speed increases, the back EMF of the motor limits the current to an average value of approximately 1.5A and the switching current regulator operates, if at all, only on the peak current. Motor current is indicated in the lower waveform.

5.3.16.2 Positioner Motor Driver

Current for the head positioner motor is provided by a network similar to current switch 3 and current switch 4 of the Spindle Motor Driver circuit. The major functional difference in this network is that the current developed for small signals is directly proportional to the amplitude of the drive signal. For large signals, the current is limited by the impedance of the motor winding and an integrator detecting the time/amplitude product of the motor current. A block diagram indicating the functional divisions of the positioner motor driver is shown in Figure 5-39C. These divisions are: (1) A summation amplifier to sum the servo drive signal with the current feedback signal, (2) A current amplifier to amplify the output of the summation amplifier to a level to drive the position motor, (3) A clamp circuit to disable the current amplifier, and (4) An integrator and detector circuit to detect over-current conditions.

The servo Drive Signal is an analog signal generated on the Servo (SO) board. When this signal is positive, the Servo Drive signal turns on the positive driver network. When the heads are detented (held stationary over a track), any motion of the heads away from the detent position causes the Servo Drive signal to generate an opposing signal. Since positive drive current causes the positioner motor to move toward the spindle, attempting to manually move the positioner motor toward the spindle will cause negative drive current to flow in the motor. The amount of current flowing will be proportional to the amount of force applied up to the limit of the motor impedance or the detection of an over-current condition (full drive for more than approximately 65 milliseconds).

The current amplifier may be disabled from control by the Servo Drive signal in three different conditions: (1) during the load condition via the clamp circuitry, (2) if an overcurrent condition has been detected via the integrator/detector circuit and (3) by manual operation of the servo release switch.

The current integrator has a time constant of 47 milliseconds and the over-current detector a threshold of 0.54V. The resulting time constant for the combination of the integrator and the detector for a full current condition (6.25 A) is 32 milliseconds for currents of either polarity. At the end of the time constant, the over-current signal will go low, initiating a similar time delay on the Sensor (SR) board. Lower current values cause longer delay times with values less than 2.7A being below the threshold of the detector circuit.

5.3.16.3 Brush Motor Driver

Inputs to the Brush Motor Driver circuit are from complementary open collector amplifiers on the sequence logic (SL) board. The collector load for each amplifier consists of a 2.2KΩ resistor on the SL board in series with a parallel combination of a 1KΩ and the emitter-base resistance of each transistor to their respective supply voltages. Each drive transistor is turned on for one half the 60 Hz input, alternatively applying +24V and −24V to the brush motor at a 60 Hz rate.

5.3.16.4 Positive and Negative 15 Volt Tracking Regulator

The control for the plus and minus 15 volt operational amplifier power supply is derived from an MC1458L dual ± 15 volt IC regulator. This IC is a dual polarity tracking regulator designed to provide balanced positive and negative output and may be externally adjusted for voltage and balance with resistors K82 and K79 respectively.

5.3.16.5 Drawer Unlock Solenoid Pick

This circuit provides the high current needed to pick the solenoid that unlocks the cabinet drawer as well as the low level holding current.

One side of the solenoid is permanently held at +24V.

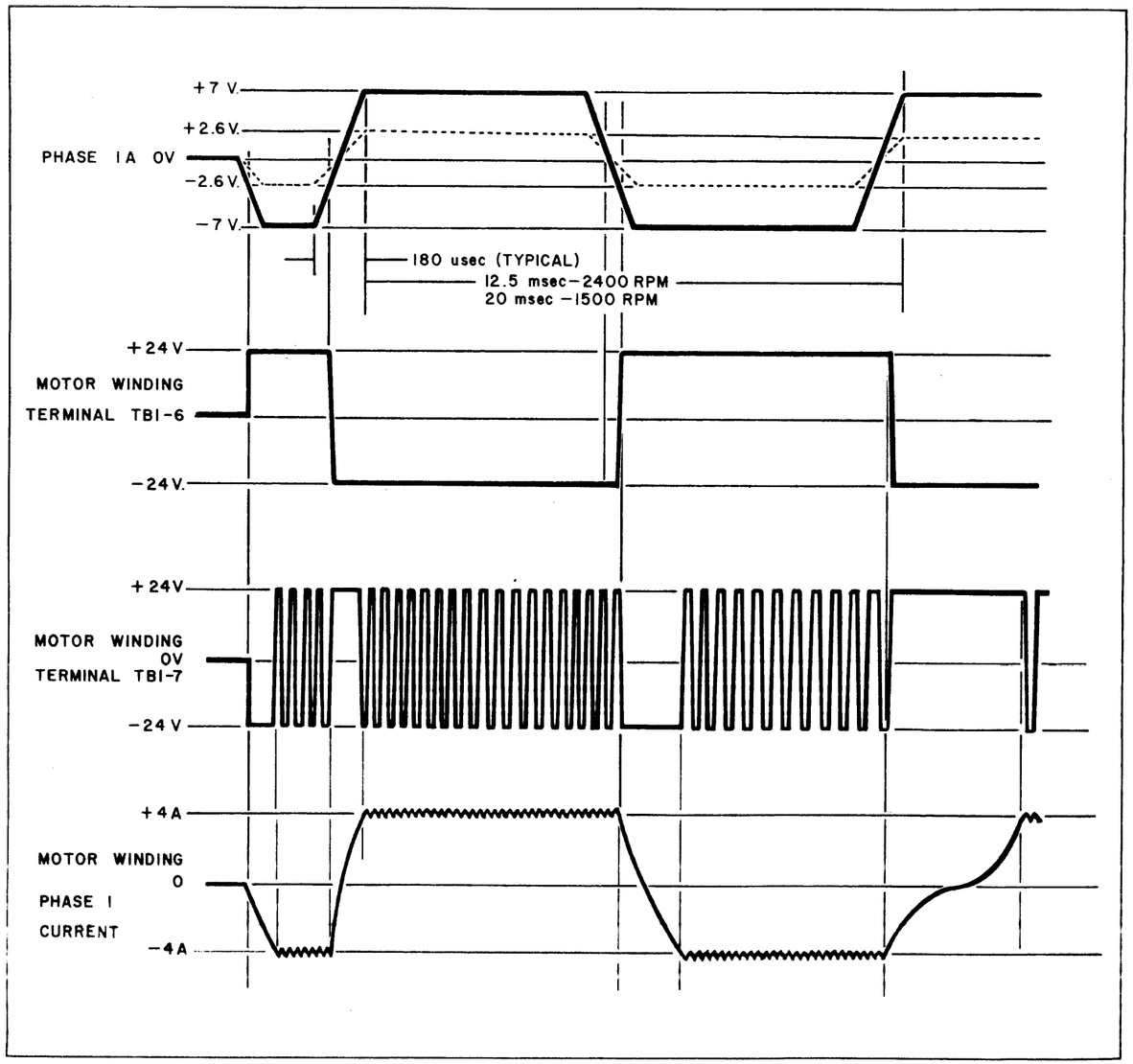


Figure 5-39B. Spindle Driver Waveforms

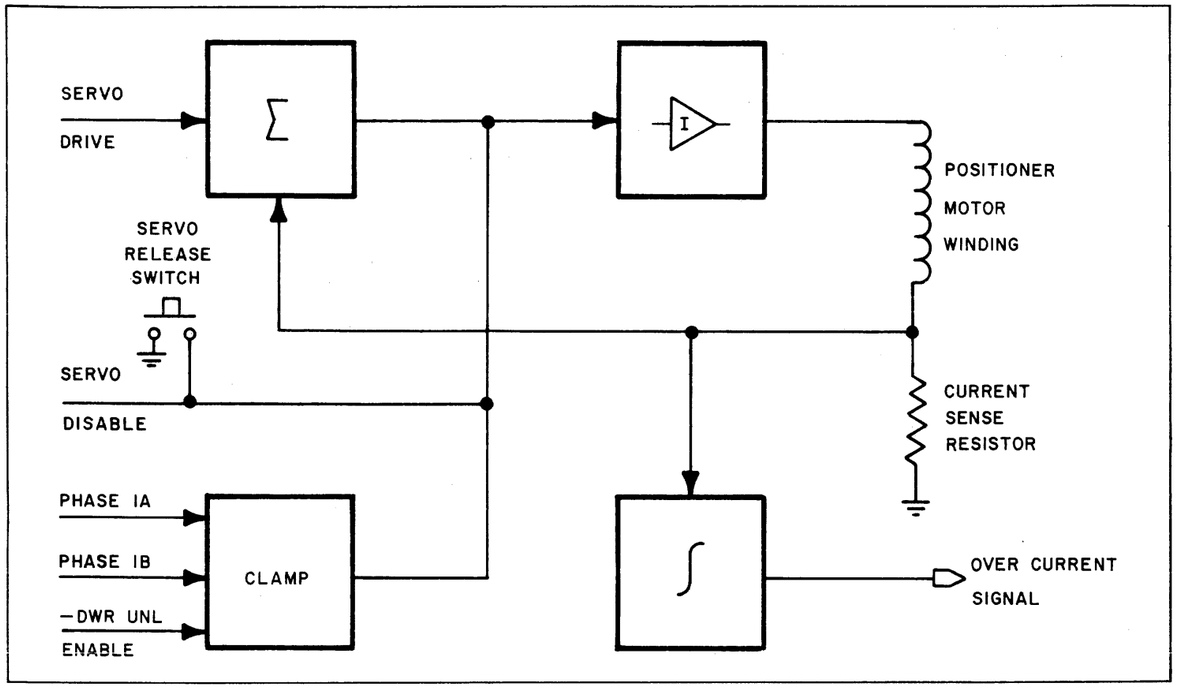


Figure 5-39C. Positioner Motor Driver Block Diagram

When +DRAWER UNLOCK PICK goes high, it provides a high current path to ground through transistor E107. This high current is required to overcome solenoid pull-in inertia.

–DRAWER UNLOCK ENABLE, which went low when +DRAWER UNLOCK PICK went high, provides a path for holding current through emitter follower action of E107 when +DRAWER UNLOCK PICK times out.

5.3.16.6 Head Load Solenoid Pick

This circuit supplies both pick and holding current to the Head Load Solenoid. One side of the solenoid is tied to +24V.

When +HEAD LOAD PICK goes high, a path for high pick current is provided through transistor H106 to –24V. This causes a drop of 48V across the solenoid.

When +HEAD LOAD PICK goes low, –HEAD LOAD ENABLE provides a path for the holding current through H105 to +12V by the action of voltage divider H101 and H102.

5.3.16.7 Braking (Speed Sense) Timer

The braking timer is a retriggerable one-shot, driven by the Phase 2 Spindle Drive signal to the Spindle Motor. The timing element is a 555 Integrated Circuit timer adjusted for a nominal period of 14 seconds. Retriggerable operation is obtained by the use of an open collector interface driver (J97) to keep timing capacitor H25 discharged as long as drive is applied to the Phase 2 Spindle Winding. When the LOAD/RUN switch is changed from the RUN position to the LOAD position, a DC signal of +7V is applied to Phase 1A, –7V to Phase 1B, 0V to Phase 2A and 0V to Phase 2B. This results in a logic "high" signal occurring at the output of J97 and capacitor H25 is allowed to charge through resistor H27. When the voltage on H25 reaches 3.3 volts the output of the timer (H1905) switches from a logic "high" to a logic "low". The output is level shifted by resistors J16 and J17 to provide a signal centered around ground to the detector on the SD board. No alignment or adjustment is required on this circuit.

5.3.17 R/W Amplifier (R/W) PCB

The R/W Amplifier PCB contains the circuitry necessary to accomplish the following:

- Enable the head selected by the using system.
- Energize the straddle erase winding on the selected head when the erase function is gated.
- Accept write data and clock pulses and, when the write function is gated, to convert each pulse into a current reversal in the selected head.
- Determine when a write check condition exists, and activate the write check functions.
- Receive read data and clock signals from the selected head, condition these signals and, when the read function is gated, present these signals to the interface as unseparated data and clock pulses.
- Provide to the interface the necessary indicator and/or control signals for write check, write fault, and file ready functions.
- Provide special voltages required by the R/W amplifier circuitry.
- On drives with the Write Protect Option, inhibit the write circuitry under write protect conditions as described in 1.3.1(4), and provide write protect indicator and control signals to the interface.

5.3.17.1 Enabling the Selected Head

The R/W winding of each head is centertapped. A head is disabled by placing a –1V signal on the centertap. A head is enabled for writing or reading by placing a signal of +23V or +1V, respectively, on the centertap. The centertap of each head is driven by its corresponding three-transistor circuit called a head driver. Each of the four drivers has two inputs, one from the head select logic and one from the write gate logic. The head select logic determines which driver removes the –1V from its corresponding head center tap, while the write gate logic determines whether the selected driver places the centertap at +23V (write) or +1V (read).

Referring to the R/W Amplifier schematic, the head driver for the upper head of the upper disk consists of transistors at B85, E86 and E85, plus associated circuitry. Input from the head-select logic is applied to the base of the transistor at E86, while input from the write gate logic is applied to the base of the transistor at E85. In the "not selected" condition the input from the head-select logic is high, and E86 is cut off. The R/W head centertap is held at –1V under these conditions, regardless of the write gate logic input. If the head-select input to this driver goes low, E86 conducts. The collector of B85 (and consequently the centertap) now goes to either +1V or +23V, depending on the input from the write gate logic. For a "write" condition, the input is high, and E85 conducts. This causes B85 to conduct, and heavy current is drawn through the 150 kΩ resistor at D86. The centertap of the upper-disk upper head is now at +23V, and the head is ready to receive write data from the write driver (see 5.3.17.3).

If the input from the write gate is low, E85 and B85 are cut off. With only E86 conducting, the voltage drop across the resistor at D86 is only about 23V, placing the head centertap at +1V, which is the "read" condition.

Examination of the R/W Amplifier schematic shows that each of the other R/W heads has a head driver exactly the same as the one just described.

The head-select logic receives DISK SELECT and HEAD SELECT signals from the interface through the Receiver-Driver Circuit No. 1 PCB, and applies an enabling signal to the head driver of the selected head. Referring again to the R/W Amplifier schematic, assume that the using system has selected the upper head of the upper disk. The low DISK select is inverted by the gate at D56-13. The resulting high is applied to the upper disk NAND gates at E66-1 and E66-4. The output of either of these two gates will then go low on receipt of a high on the other input pin. The high at D56-13 is also inverted at D66-12, and applied to lower disk NAND gates at E66-9 and E66-12, disabling these two gates. The upper disk has now been selected by the head select logic.

The low HEAD SELECT signal is inverted by gate D56-14, and the resulting high is applied to upper-head NAND gates E66-2 and E66-13. E66 now has a high on both pin 1 and pin 2, and the low output is applied to the base of the transistor at E86, causing it to conduct. As previously described, the driver enables the upper-disk upper head.

The head driver for the upper-disk lower-head does not receive an enabling low because its corresponding NAND gate receives a low at pin 5.

Similar circuit analysis will show that any one of the heads can be enabled, through its corresponding head driver, by a combination of the DISK SELECT and HEAD SELECT signals.

5.3.17.2 Erase Gate

In order for the erase function to be gated for the selected head, the following three conditions must exist:

- READY TO S/R/W input must be low (indicating "ready")
- HEADS LOADED input must be high (indicating "heads loaded")
- The ERASE GATE must be low

Referring to the R/W Amplifier schematic, it can be seen that a low READY TO S/R/W and a high HEADS LOADED will produce a low at NOR gate B47-13. This places a low on one pin of the input NOR gates for the following functions:

- WRITE DATA
- WRITE GATE
- ERASE GATE
- READ GATE

When a low ERASE GATE is received, B56-13 goes high. This high is applied to D47-12. Assuming that the write protect input at D47-13 is high, a low appears at D47-11. This low accomplishes the following:

- gates H47-3 so that the head drivers receive a "write" signal.
- conditions exclusive OR gates E56-11 and E56-8 for write check functions (to be explained later)
- causes a high at NAND gate H47-11

When H47-11 goes high, the transistor at H85 conducts. The transistor's collector is connected to the erase bus. One end of each erase winding is connected to the erase bus and the other end is connected to the centertap of its corresponding R/W winding. When the transistor at H85 conducts, collector current passes through the erase winding of the head selected as previously explained, since that erase winding will be the only one with +23V on one end.

5.3.17.3 Data Write Function

In order for write data and clock pulses to cause current flow in the selected R/W head, the following conditions must exist:

1. The selected head must be in the Write Mode.
2. Heads must be loaded, and READY TO S/R/W must be ready.
3. The +5V supply must be within its lower tolerance limit.

The WRITE GATE, through B56-2 and D47-3, places a low at H47-1. The resulting high output is applied to the head drivers, and the selected head is placed in the write mode. This is redundant to the ERASE GATE function of causing a high at H47-3.

Write protect and write check are explained in subsequent paragraphs. It will be noted here that a high write-protect is needed at D47-2 or D47-13 in order to obtain the high at H47-3, thereby placing the selected head in the write mode. It will also be noted that a high write-check at H47-4/5 will prevent the necessary high from being applied to the head drivers.

As previously explained, when the heads are loaded and the drive is ready to S/R/W, a low is applied to B56-9, the write data input NOR gate. The output of this gate can then go high whenever a low data or clock pulse is received on pin 22. Note that B56-14 will remain low and data and clock pulses cannot be applied to the write circuitry, if either the HEADS LOADED or READY TO S/R/W change state.

With B56-14 enabled, and with a high on pins 2 and 13 of AND gate E47-12, data and clock pulses are applied to the write flip-flop at B66. The write gate has previously caused a high to be applied to the set and reset inputs of the flip-flop. Each pulse received by the write flip-flop causes it to change the state of its Q and $\overline{Q}$ outputs, which drive the write drivers. With each change in state, these drivers cause current to flow in alternate halves of the R/W winding. Since the direction of current flow is opposite in the two halfs, each change of state of the write flip-flop causes a flux transition on the selected disk surface.

It will be noted that the high on E47-2/13, which drives the write flip-flop, is furnished by a voltage divider off the +5 Vdc line. If the voltage falls below approximately 5V, the voltage applied to E47-2/13 will be insufficient to constitute a high condition, and this gate will then block data and clock pulses from reaching the write flip-flop.

5.3.17.4 Read Function

When there is no WRITE GATE signal (or no ERASE GATE signal), the output of the head-driver write conditioning NAND gate H47-3 is low, and the selected-head centertap is at +1V, the "read" mode. Flux transitions on the disk surface now induce voltages in the selected head winding; the resulting signal is amplifier and shaped to produce read data and clock pulses at the interface.

Referring to the R/W Amplifier schematic, signals induced in the selected R/W winding are applied to a buffer amplifier consisting of transistors at D97 and D106, whose output drives a three-section read amplifier. The three sections provide preamplification, equalization, and final amplification, respectively, using three 592A operational amplifiers. The output of the amplifier is applied to an 8T20B zero-crossing detector at J39. The Schmitt trigger section provides a step leading edge to trigger the monostable multivibrator section, which produces an output pulse of 100 ns (nominal). A 100 ns pulse is therefore produced for each flux transition. However, there is no output from the multivibrator unless it is enabled by a low on pin 3. This low is produced by the low –READ GATE signal at PCB interface pin 20. With the heads loaded and the drive ready to S/R/W, the –READ GATE causes a high at gate B47-14, which is inverted by a NAND gate at D9-6.

The positive READ DATA AND CLOCK pulses at the Q output of the zero-crossing detector are inverted by NOR gate D37-2, and applied to the Data Clock Separator PCB through R/W Amplifier PCB interface pin 32.

5.3.17.5 Write-Check

Write-check circuitry on the R/W Amplifier PCB prevents the head driver of the selected head from being in the write mode whenever any of the following conditions occur:

- Write current without a true –WRITE GATE line or –ERASE GATE line,
- Write and select of more than one head,
- Erase current without a true –ERASE GATE line, or
- –ERASE GATE line true without erase current.

Any of the foregoing conditions will set the write-fault F/F, which consists of negative logic AND gates at H37-13 and H37-3. Setting this F/F results in a high at H37-3. This high is applied to a NAND gate at H47-4/5. The low output of this NAND gate prevents the input transistors of any of the head drivers from conducting, and the write operation is prevented.

For purposes of this description assume that the disk drive is in the LOAD mode. The +SPINDLE ENABLE signal input of pin 30 of the R/W PCB connector is low. This is gated through E47-6, inverted at H37-2, and is applied as a high to the reset input to the write-fault F/F at H37-5. Its output at H37-3 is therefore low, as is H37-12. The set input is also low, and is determined at E47-8. As will be explained later in this paragraph, all three inputs to the negative-logic NOR gate at E47-8 will be high under conditions of no write-fault. The high at H47-9/10 is inverted and applied as a low to the set input of the write-fault F/F at H37-11. With both inputs at H37-11, 12 low, the output at H37-13 is high.

When the disk drive is switched to the RUN mode, +SPINDLE ENABLE goes high, resulting in a low at the reset input of the write-fault F/F at H37-5. This has no effect, since the input at H37-4 is still high, but an additional low at H37-4 would now set the F/F. The F/F is now completely reset, and if no write fault exists, disk drive operation is normal. A write fault will cause one of the inputs at E47-9, 10, 11 to go low, setting the F/F and inhibiting writing as described previously. Reset is accomplished with the +SPINDLE ENABLE signal, by switching the disk drive to LOAD and back to RUN. It should be noted that the write-fault F/F is also reset by the –INITIAL RESET PULSE.

One of the conditions which will cause a low input to E47-9, 10, 11, thereby setting the write-fault F/F, is write current flowing without a true –WRITE GATE line or –ERASE GATE line. Write current is sensed by a transistor at H86. With no write current, and with the head drivers not in the write mode, the drop across the 27Ω resistor at H82 is only about 78 mv, which is insufficient to allow the transistor at H86 to conduct. With H86 cut off, the diode at H77 is forward biased, and conducts. Its cathode, then, is approximately at ground when no write current is flowing. During a write operation, with all transistors of the selected head driver conducting, the current through the 27Ω resistor at H82 is sufficient to cause at least 13 ma of collector current to flow through the 2.2kΩ resistor at H79. This places the cathode of the diode at H79 at approximately +5V. The two diodes at H78 and H77 therefore clamp the junction between them at ground (low) for no write current, and at +5V (high) for write current. This junction is connected to one input of an exclusive OR gate at E56-13. The other input will be high when neither the –WRITE GATE nor the –ERASE GATE is true. With no write or erase gate, but with write current flowing, both inputs to the exclusive OR gate will be high, and its low output will set the write fault F/F.

Another condition which will cause a low input to E47-9, 10, 11, thereby setting the write-fault F/F, is write and select of more than one head. This condition is sensed by a transistor at J71. This transistor is normally cut off, and its collector is at +5V. If more than one head is selected and is writing, the current through the resistor at H70 will be sufficient to cause the transistor at J71 to conduct. Its collector will go low, setting the write-fault F/F.

The write-fault F/F is also set when the status of erase current does not agree with the condition of the –ERASE GATE line. This condition is sensed by an exclusive OR gate at E56-8. The input at pin 10 of this gate is high when erase current flows through the resistor at H88, and low when no erase current is flowing. The input at pin 9 of the exclusive OR gate is low when –ERASE GATE is true, and high when it is false. If –ERASE GATE is false but write current is flowing, both inputs to the exclusive OR gate will be high, and its low output will then set the write-fault F/F. Conversely, when –ERASE GATE is true but no erase current flows through H88, both inputs to the exclusive OR gate will be low, and its low output will set the write-fault F/F.

As previously explained, the high at H37-3 when the write-fault F/F is set will inhibit writing. The high is also applied to a negative logic AND gate at H28-6, where it inhibits FILE READY indicator and control signals.

The other section of the write-fault F/F, H37-13, goes low when set. Its output provides the +WRITE FAULT signal and the –WRITE CHECK INDICATOR signal.

The –WRITE CHECK INDICATOR signal also occurs if the high voltage supply on the R/W Amplifier PCB falls below tolerance. This is sensed by a transistor at J74. Two zener diodes at J78 and J80 are reverse biased sufficiently for them to conduct, holding the base of the transistor at J71 approximately 10 volts more positive than the 11–volt supply. With a base-emitter voltage of –1V, the transistor is cut off. If the 11–volt supply drops to less than about 9½ volts, the transistor will conduct. The collector will go low, and the –WRITE CHECK INDICATOR and +VOLTAGE CHECK signals will occur.

5.3.17.6 Write Protect Option

When the Write Protect Option is installed on the Series 40, circuitry on the Read/Write Amplifier PCB requires a specific front-panel action by the disk drive operator in order to enable writing after the write-protect condition is set. Write protect is initially set when the disk drive is placed in the LOAD mode, or it can be set by interface signal from the controller. Write protect is cleared (reset) by depressing a front-panel switch. However, the switch has no effect unless the disk drive is in the RUN mode when the switch is depressed. An indication of the status of write-protect is furnished to a front-panel indicator and to the interface.

Referring to the R/W PCB schematic, there are two write-protect flip-flops, one for the upper disk and one for the lower disk. The upper write-protect F/F consists of two negative logic OR gates at D18-6 and D18-12. The lower write-protect F/F consists of two similar gates at E9-8 and E9-12. When write protect is set, both F/Fs will be set, and a low will occur at either D18-8 or E9-6, depending on which disk is the selected disk. Either of these lows will be gated through H9-6, H9-8, and D37-3, and will result in the following:

1. The –WRITE PROTECT signal at H9-8 will disable the write gate D47-3 and the erase gate D47-11, both on the R/W PCB.

2. The –WRITE PROTECT signal at H9-8 will be gated through H9-3 and H18-3. The low at H18-3 will ground one end of the lamp in the PROTECT switchlight on the front panel, illuminating the PROTECT switchlight.

3. The low at D37-3 will be sent to the RDR1 PCB, where it will be ANDed with the –FILE SELECT signal from the controller and then sent to the interface as the WRITE PROTECT STATUS signal.

The following text describes the functioning of the upper write-protect F/F, D18-6/12. Operation of the lower write-protect F/F is the same. The following description assumes that both disks are enabled for write protect by the absence of jumpers at E10 and E11. It is also assumed that the Series 40 has been enabled for write protect by the absence of a jumper between ground and connector pin P8A-8 on the Panel Distributor PCB. Absence of this jumper results in no electrical connection to R/W PCB interface pin 8 (–WRITE PROTECT DISABLE). Under this condition, a high remains at D18-10 and E9-4.

With the upper disk selected, a high exists at D18-11. Since pins 10 and 11 of D18-8 are high, any low input to D18-6 will set write protect.

With power on, no +WRITE PROTECT INPUT signal from the controller, and the disk drive in the LOAD mode, the conditions shown on the first line of Table 5-7 exist.

The write-protect F/F is set by lows on pins 4 and 3 of D18-6. The low at D18-4 is due to the high on D28-1, which exists whenever the spindle drive is enabled. The low on D18-3 exists because all inputs to D18-12 are high. Note that at this time, depressing the PROTECT switchlight on the front panel would only remove the low from D18-3. D18-4 would still be low, and write-protect would still be set.

Switching from the LOAD mode to the RUN mode removes the high from D28-1 and the low from D18-4. As shown in Table 5-7, a low still exists on D18-3, since the PROTECT switchlight has not been depressed, and the F/F is therefore still set.

The disk drive operator can now depress the PROTECT switchlight to reset the write-protect F/F. As shown in Table 5-7, this removes the low from D18-3. The table shows conditions which exist while the switchlight is depressed. When the switch is released, D18-1 goes high again. However, D18-2 is now low since the F/F has been reset.

Receipt of a +WRITE PROTECT INPUT signal from the controller is also shown in Table 5-7. This signal is applied to NAND gate D9-3, and sets the write-protect F/F by means of a low at D18-5. As previously descirbed, depressing the PROTECT switchlight will again reset the F/F.

When the disk drive is switched from RUN to LOAD and the spindle motor is disabled, the F/F is set through D28-3.

It should be noted that if a jumper is installed at E10, the F/F is automatically reset when the drive is switched from LOAD to RUN.

Table 5-7.
Write Protect Conditions

	D9-3			D28-3			D28-8			D18-12			D18-6			
CONDITION	**1**	**2**	**3**	**1**	**2**	**3**	**9**	**10**	**8**	**2**	**13**	**1**	**12**	**5**	**4**	**3**	**6**
Load	H	L	H	H	H	L	H	L	H	H	H	H	L	H	L	L	H
Run	H	L	H	L	H	H	L	L	H	H	H	H	L	H	H	L	H
Switch	H	L	H	L	H	H	L	L	H	L	H	L	H	H	H	H	L
Protect Input	H	H	L	L	H	H	L	L	H	H	H	H	L	L	H	L	H

SECTION 6
MAINTENANCE

6.1 GENERAL MAINTENANCE INFORMATION

6.1.1 Maintenance Requirements

Reduced preventive and corrective maintenance are inherent in the Series 40 Disk Drives. Alignments are simple to perform and infrequently required (see paragraph 6.6.1). Mechanical wear has been virtually eliminated by the absence of belts, pulleys, friction drives, potentiometers, or other mechanisms normally requiring field maintenance. Spindle speed and the head position are controlled electronically, with a minimum amount of mechanical hardware. As a result of this design, normal preventive maintenance is reduced to cleaning and air-filter replacement, as described in Paragraph 6.4.

6.1.2 Maintenance Instructions

The Series 40 user should consult Paragraph 6.2 of this manual, compare the lists with his existing or projected tools and test equipment, and determine the level of maintenance capability he intends to maintain. Preventive maintenance is described in 6.4, while corrective maintenance is covered by 6.5. Prior to performing any alignment or maintenance, the user should familiarize himself with the location of assemblies in the Series 40, as shown in Paragraph 6.3. Particular attention is invited to Paragraph 6.7.1, which gives the location within this section of instructions for replacement of the various parts and assemblies.

6.1.3 Maintenance Precautions

To avoid damage to the Series 40 or an associated disk cartridge, observe the following precautions during maintenance:

1. Never connect or disconnect any cable assembly to or from the Series 40 with the power present at the DC power connector.

2. When the lower disk is exposed, avoid scratching, nicking, fingerprints or other contact with the coated surface of the disk.

3. Electronic detenting holds the head carriage in position when power is applied. Do not attempt to move the carriage by hand while power is on unless the servo release switch is in the release position. Figure 6-1 shows the location of this switch on the heat sink assembly.

4. Keep the Series 40 as clean as possible. When the drive is open for maintenance but is not actually being worked on, protect it from dust with a lint-free cover. The assembled disk drive should never be stored without either a cartridge dust cover or a plastic bag in place.

5. When the top cover is in place, the drive should be left in the RUN mode whenever possible. This will insure that clean air will be drawn through the filter and supplied to the interior of the disk drive.

6.2 REQUIRED TOOLS, TEST EQUIPMENT, AND SPARES

6.2.1 Levels of Maintenance

This paragraph (6.2) describes the tools, test equipment, and spares required for preventive and corrective maintenance of a Series 40 Disk Drive. For brevity, common hand tools are not listed in the manual. Preventive maintenance of the drive is simple, and it is assumed that all users will perform such maintenance themselves. Corrective maintenance capability varys greatly between organizations. Some Series 40 users may have a trained service force, spare drives, and complete facilities, whereas others may be limited to circuit-board replacement. Consequently, the corrective maintenance described in this manual is divided into three levels, each requiring successively more extensive test equipment, spares, and technical capability of personnel. The test equipment and spares are listed separately in 6.2.3 for the different levels. For corrective maintenance beyond the user's capability, contact Diablo Customer Service. As used in this manual, the corrective maintenance levels are as follows:

1. LEVEL 1 – minimum corrective maintenance. Substitution of circuit boards. Simple component replacements and adjustments, not requiring significant disassembly of the drive.

2. LEVEL 2 – Level 1 maintenance plus replacement and alignment of R/W heads. Component replacement requiring limited disassembly of some parts of the drive.

3. LEVEL 3 – Level 2 plus major disassembly, reassembly, and alignment.

In the following lists, all part numbers shown are Diablo part numbers. Numbers in parentheses represent recommended quantities if greater than one.

6.2.2 Preventive Maintenance Items

The following items should be available to each person servicing a disk drive on a scheduled basis:

a. Head cleaning pads, 91% isopropyl alcohol (Texpads, or equivalent) P/N 99000-01 (10)

b. Air filters, P/N 16163 (2)

c. Bottle of touch-up lacquer, P/N 99004-01 (gray), 02 (brown), 03 (white)

d. Adhesive tape (1 roll)

e. Tongue depressors (1 box)

f. Cotton swabs

g. Metal cleaner, P/N 70677 (1 bottle)

6.2.3 Corrective Maintenance Items

6.2.3.1 Level 1 Maintenance

a. One each of all pluggable PCBs

b. Extender board: P/N 11427

c. Power transistors, 3 each type

d. Lamp, miniature flange, 28V; P/N 10545-01 (12)

e. Brushes, P/N 16082

f. Oscilloscope, vbw $\geqslant$ 15 MHz, vds $\geqslant$ 100 mV/cm, sweep speed $\geqslant$50 ns/cm.

6.2.3.2 Level 2 Maintenance

a. All Level 1 maintenance items.

b. Alignment cartridge, P/N 70306 (100 tpi) or 70709 (200 tpi).

c. Set of R/W Head Assemblies, P/N 16781-01, 02, 200 tpi; P/N 16272-03, -04, 100 tpi.

d. Head-loading Spring, P/N 16260 (2400 rpm) or 16360 (1500 rpm).

e. R/W Head Adjustment Tool; P/N 16087.

f. R/W Head Alignment Plug, P/N 25104A.

g. Plastic feeler gauges.

h. Torque screw driver, P/N 99001.

i. "L" shaped Allen wrench, 9/64.

j. Index Transducer Adjustment Tool, P/N 16533.

6.2.3.3 Level 3 Maintenance

a. All Level 2 maintenance items.

b. Spindle cone, P/N 15171.

c. Alignment bar, P/N 16438.

d. Spindle Assembly, P/N 16117 (100 tip disk drives only)

e. Head-Positioner Assembly, P/N 16010-10 (100 tpi) or 16010-20 (200 tpi)

f. Heat Sink Assembly, P/N 16712.

g. Head-Positioner gasket, P/N 16258.

6.3 LOCATION OF ASSEMBLIES

Figure 6-1 shows the location of major assemblies of the Series 40. The disk drive is shown with the Card Cage and Heat Sink Assemblies in the extended, or "maintenance" position. Figure 6-2 shows other positions. Location of PCBs within the I/O Box and the Card Cage is shown in Figure 6-3. Location of lower level assemblies and parts is shown in the various illustrations in Section 7.

6.4 PREVENTIVE MAINTENANCE

6.4.1 Preventive Maintenance Philosophy

The principle of maximum machine available time governs the preventive maintenance recommendations contained herein. Unless a preventive maintenance procedure increases overall machine available time, it is not recommended. Except for the procedures recommended in Paragraph 6.4.2, no maintenance or adjustment should be performed on a drive that is operating satisfactorily.

6.4.2 Preventive Maintenance Procedures

Table 6-1 summarizes the recommended preventive maintenance procedures, and is based on one-shift-per-day operation in a normal office environment. Operation in an abnormally dirty environment, a high frequency of cartridge changing, or multi-shift operation would increase the frequency of preventive maintenance required. In addition to the maintenance listed in Table 6-1, the base plate should be wiped with a lint-free cloth and vacuumed whenever the bowl is removed.

Table 6-1.
Preventive Maintenance Action

Interval	Action	Paragraph
Semi-annual	Clean and inspect R/W Heads	6.4.2.1
Semi-annual	Clean and inspect magnetic ring	6.4.2.2
Semi-annual	Replace air filter	6.4.2.3

Prior to performing any of the preventive maintenance procedures listed in Table 6-1, insure that there is no disk cartridge installed, and that power to the Series 40 is off. See Paragraph 6.7.2.2 for removal of disk pack with power off. Remove the top cover as described in 6.7.2.1.

6.4.2.1 Cleaning of R/W Heads

In order to clean the R/W heads, the card cage must be lowered to provide access to the lower heads. To accomplish this, refer to Figure 6-2 and proceed as follows:

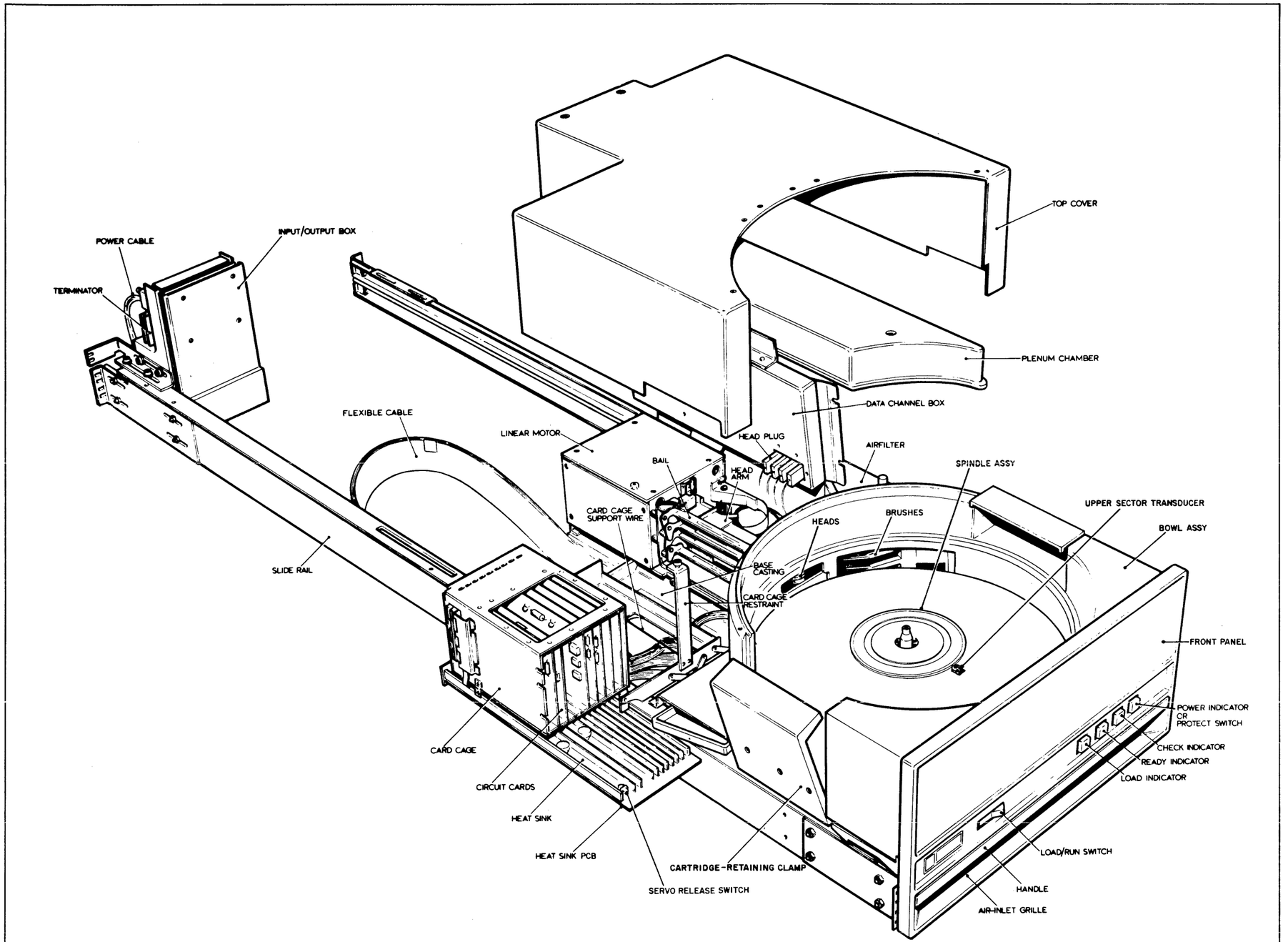


Figure 6-1. Location of Assemblies Series 40 Disk Drive

1. Loosen the securing screw at the left edge, middle, of the data channel box, as shown in Figure 6-2a. Lift the data channel box and move the card cage to the intermediate position.

2. Loosen the card cage restraint screw, move the restraint slightly forward until the restraint screw is clear of the slot.

3. Swing the card cage down into the maintenance position, unhook the card-cage support wire, and lower the card cage into the head-cleaning position.

Access to the lower heads is now possible by manually moving the head carriage all the way to the rear. Clean both lower heads by rubbing lightly with a pad soaked with 91% isopropyl alcohol (Texpad, or equivalent). The pad should be wrapped around a tongue depressor, so that light to moderate pressure can be exerted. Use a lint-free wiper to remove alcohol residue. Clean the upper heads in a similar manner, except the head carriage can be moved forward to make the upper heads easily accessible in the bowl. See 6.6.2(4) for procedure to move carriage with power off.

Complete removal of all contamination from the heads is mandatory, including fingerprints.

6.4.2.2 Cleaning and Inspection of the Magnetic Ring

Use adhesive tape to remove any particles from the magnetic ring at the top of the Spindle Assembly. If there is any sign of corrosion on the magnetic clutch surface, remove the corrosion as follows:

1. Remove the lower disk cover by removing the four screws which hold it to the inside of the bowl.

2. Using a very small quantity of metal cleaner (P/N 70677) on the end of a "Q-tip," rub the clutch surface (see Figure 6-4) until the corrosion is lifted. Exercise care to ensure that fluid does not run between the magnet and the clutch.

3. Clean the clutch surface with alcohol, P/N 5002.

4. Repeat Steps (2) and (3) until all traces of corrosion are removed.

5. Thoroughly clean clutch surface and sides with alcohol. Exercise caution to ensure that the clutch surface is not touched with fingers after performing this step.

6. When the alcohol has evaporated, coat the clutch surface with a smooth, thin layer of corrosion inhibitor (P/N 70191) applied with a clean "Q-tip."

7. Replace the lower disk cover.

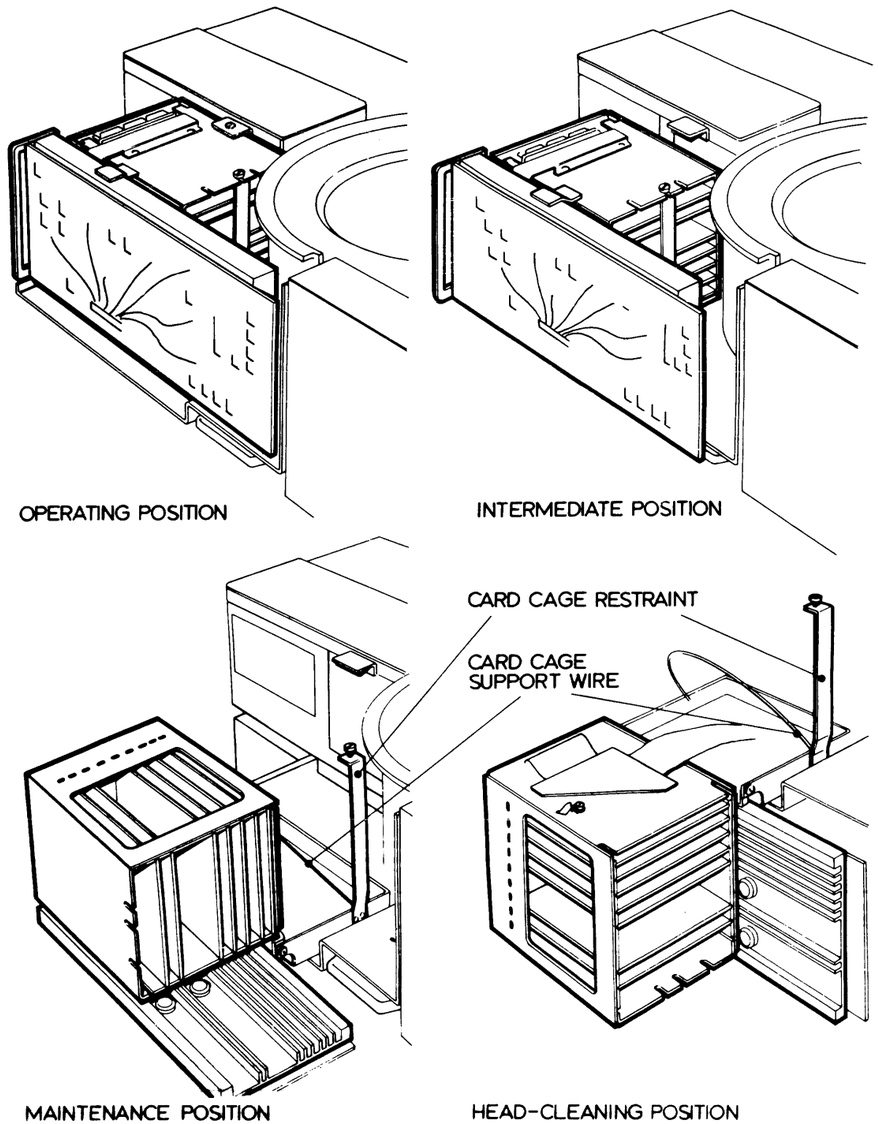


Figure 6-2. Card Cage Positions

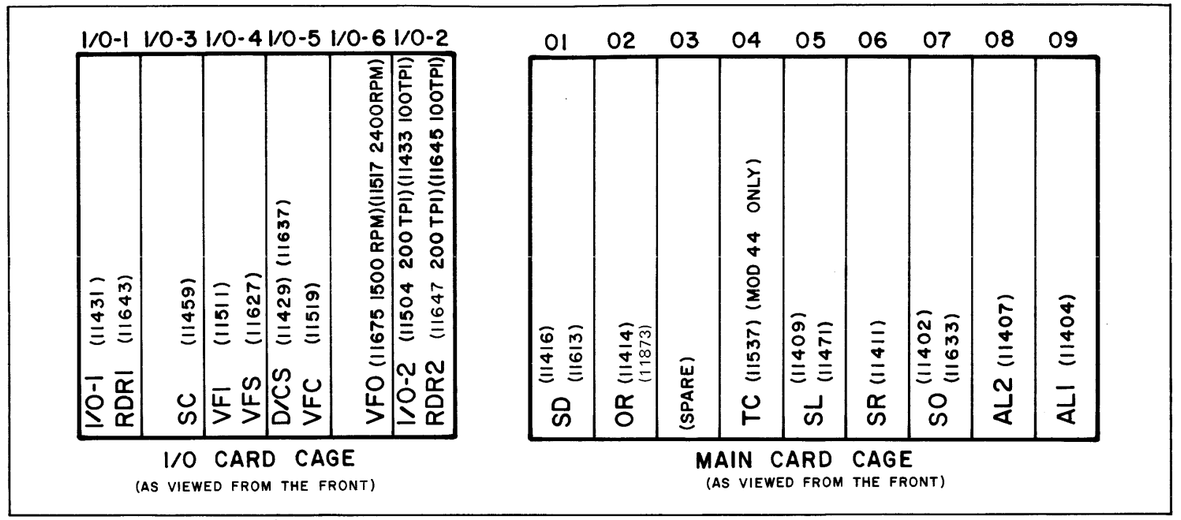


Figure 6-3. PCB Locations

6.4.2.3 Replacing the Air Filter

To replace the air filter, first remove the plenum chamber (see Figure 6-1), which is held in place with two screws. Exercise caution so that the gasket around the sealing edges of the plenum chamber is not damaged. The air filter and pad can now be lifted straight up. Install a new air filter and pad, observing the air-flow direction printed on the filter label (arrow up), and replace the plenum chamber. Insure that both gaskets are well seated on their sealing edges.

6.5 CORRECTIVE MAINTENANCE

6.5.1 Corrective Maintenance Philosophy

The corrective maintenance philosophy involves two periods—the warranty period and the post-warranty period. While the Series 40 warranty is in effect, corrective maintenance by the user should normally be limited to circuit board replacement; if equipment malfunction cannot be cured by PCB replacement, Diablo should be contacted for technical assistance or for return of the unit for repair.

6.5.2 General Troubleshooting Techniques

The recommended first step in troubleshooting is to identify in which of the following categories the malfunction falls:

- Series 40 problem
- Non-Series 40 problem
- Interchangeability problem

If all indications are normal except for the presence of non-intermittent data errors, the problem is probably one of disk pack interchangeability. The alignment of the Read/Write heads may be off. In this case, verify machine alignment by performing the adjustments described in Paras. 6.6.4.3, 6.6.4.4, and 6.6.4.5.

If the problem is not one of disk interchangeability, it should then be determined if the Series 40 is malfunctioning or if the problem is actually originating externally to the disk drive. Check the cartridge seating, verify that all cable connections (including the terminator) are properly made, and that correct signals are being presented to the Series 40 interface. If malfunctioning persists, turn off the DC power supply, disconnect the I/O cable, and turn on and verify DC power. A CHECK light in the LOAD mode indicates low voltage in the R/W electronics.

Load a cartridge onto the disk drive, and attempt to place the drive in the RUN mode. If the spindle does not start, the problem is with the disk drive, and trouble in the Oscillator PCB, Spindle Drive PCB, Sequence Logic PCB, Heat Sink, or mechanical interlocking is indicated.

If the spindle starts, either the READY or CHECK light should come on within one minute, and the corresponding output at the interface connector should be true if the unit is selected.

CHECK light ON indicates low voltage or trouble in the "write" circuitry. The READY light on indicates that the cartridge is properly seated, the spindle speed is correct, and heads are loaded.

If neither light comes on within one minute, power or other internal difficulty is indicated.

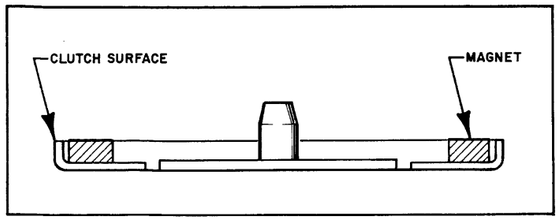


Figure 6-4. Clutch Surface and Magnet

The Series 40 is designed so that each PCB has well-defined functions, as described in Section 5 of this manual. The interchange of PCBs should be used to isolate faulty PCBs. For instructions on the removal of PCBs see 6.7.1.

6.5.3 Head Crash

If a "head crash" (head touches disk surface) occurs, this is usually detectable audibly. If this occurs, both the disk and the "crashed" head must be replaced as described in 6.7, in addition to rectification of the cause of the head crash. (NOTE: the vast majority of head crashes are due to contamination caused, in turn, by careless handling and operation of the drive. See 3.1.1b and 6.1.3.

6.6 ADJUSTMENTS

6.6.1 Adjustment Requirements

Figure 6-5 shows the conditions under which adjustments are normally required. Except under these conditions, no adjustment should be attempted unless equipment malfunction indicates a definite need for a specific adjustment. Numbers in the grid of Figure 6-5 indicate the maintenance level of the adjustment as defined in 6.2.1.

Several of the adjustments described in 6.6 require the use of an alignment cartridge. Instructions in this manual do not pertain to the use of alignment cartridges other than the Diablo Systems cartridge. When using the cartridge for making adjustments on disk drives with the Write Project Option installed, write protect should be set to prevent inadvertent writing on the disk.

In several of the adjustment procedures, the use of a programmable tester (exerciser), while not mandatory, greatly facilitates the adjustments. Where use of the exerciser is specified, the Series 40 user may choose to provide the same interface signals by some other means.

Removal of the top cover, as described in 6.7.2.1, constitutes the first step of each of the adjustments described herein. For simplicity, however, the removal procedure is not cited in each adjustment.

Condition	Adjustment: Major Track zero 6.6.5.1	R/W Heads 6.6.4.3	Upper Index Transd. 6.6.4.4	Head Load Dashpot 6.6.3.3	Lower Index Transd. 6.6.4.2	Striker Plate; Home Sw. 6.6.3.2	Spindle-to-Head Pos. 6.6.5.2	Write Protect Jumpers 6.6.3.1	Brush Mechanism 6.6.4.1	Fine Track Zero 6.6.4.5
Any Upper Disk R/W Head replaced		2	2							
Lower Disk repiaced			2							
Bowl Assembly replaced			2		2					
Head Positioner replaced	3	2	2	1	2		3			
Spindle Assembly replaced	3		2		2		3			
Front Panel won't latch or is loose						1				
Write Protect disk selection to be changed								1		
Brush motor replaced									2	
Disk Interchangeability off		2	2							2
Upper Index Transducer replaced			2							
Lower Index Transducer replaced					2					

Figure 6-5. Adjustment Requirements

6.6.2 Defeat of Interlocks

Most of the adjustment procedures described herein require defeat of one or more interlocks, particularly if the disk drive is being adjusted while installed in a rack. Defeat of interlocks is accomplished as follows:

1. Opening the drawer with the power off—the drawer latches can be operated with power off by reaching through the hole in the center of the underside of the drawer handle, and pushing the interlock level to the left while pulling on the drawer handle.

2. Opening the cartridge clamps—with the top cover removed, the cartridge clamps can be spread under any conditions of power, head position, or brush position by manually moving the cartridge clamp interlock link forward. This link is accessible by reaching between the right-hand cartridge clamp and the cartridge clamp safety stop. See Figure 6-24.

3. Operating the Spindle with drawer open and no cartridge installed—the spindle motor can be operated by manual operation of the unit home switch (see Figure 6-8) and the dust cover interlock switch.

4. Moving the head carriage with power off—the head carriage can be moved from the full retract position by moving the carriage interlock link forward as in 6.6.2(2) preceding.

6.6.3 Level 1 Adjustments

6.6.3.1 Write-Protect Jumpers

With the Write Protect option installed, either or both disks can be individually enabled or disabled for write protect by proper connections on the R/W Amplifier PCB. Figure 6-6 shows the PCB. A 10Ω, ± 5%, 1/4W resistor connected between E10 and ground disables write protect on the upper disk, while a similar resistor installed between E11 and ground disables write protect on the lower disk. For access to, and removal of, the R/W Amplifier PCB see 6.7.2.9.

6.6.3.2 Striker Plate and Unit Home Switch Adjustment

This adjustment must be made with the disk drive fully mounted in the rack. Proceed as follows:

1. Loosen the right-hand striker plate by loosening the two screws as shown in Figure 6-7.

2. Repeat Step (1) for the left-hand striker plate; in addition, the two screws on the rear end of the striker plate and the two screws holding the I/O mounting bracket to the striker plate must be loosened.

3. Adjust both striker plates so that the drawer latches shown in Figure 6-8 engage when light pressure is applied to the front panel. Tighten the eight screws.

4. Check that the unit home switch overtravel is 0.060 inches ± 0.030 inches. Loosen holding screws (see Figure 6-8) and adjust overtravel if necessary.

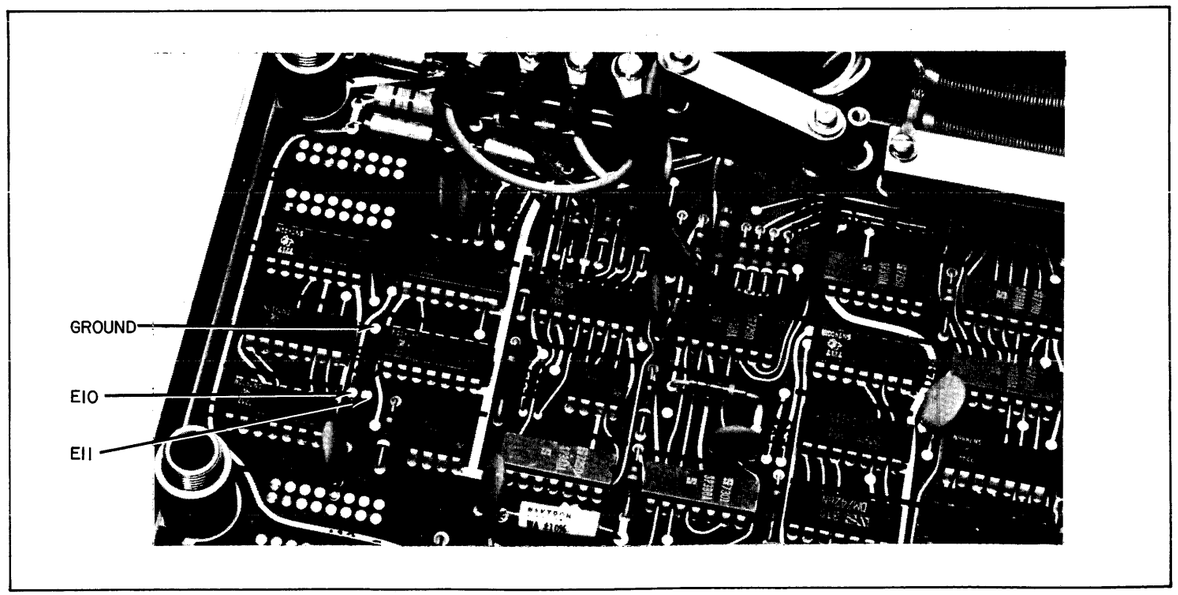


Figure 6-6 Write Protect Disk Select

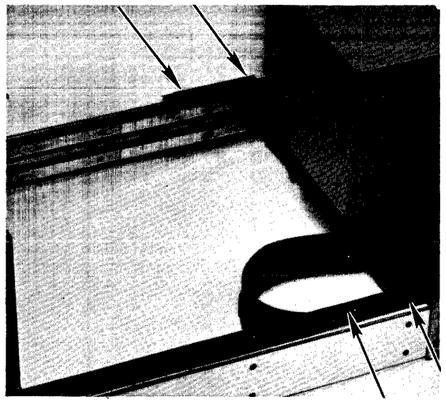


Figure 6-7. Striker Plate Screw Locations

6.6.3.3 Head-Load Dashpot Adjustment

Adjustment of the dashpot requires an oscilloscope and a disk pack having information written at track zero. To perform this adjustment, the data channel box must be swung out of the way as described in 2.2.3 to expose the head positioner. The dashpot adjustment screw is located slightly in front of the right front vertical edge of the linear motor housing, as shown in Figure 6-9. The adjustment procedure is as follows:

1. Install a disk pack having data written on track zero, and place the disk drive in the RUN mode. Allow the drive to come to READY.
2. Using the negative-going leading edge of the head-load pick signal at Pin P7-12 of the heat sink as a trigger, observe the signal at TP1 of the R/W Amplifier PCB.
3. Trigger the head-load one-shot by grounding Pin 3 of the Sequence Logic PCB.
4. Observe the trace on the oscilloscope. A data burst appears at TP1 when the heads are fully loaded.
5. Repeat Steps (3) and (4), and turn the dashpot adjustment screw until the first pulse appears 60 ms ± 5 ms after the start of the sweep, as shown in Figure 6-10.

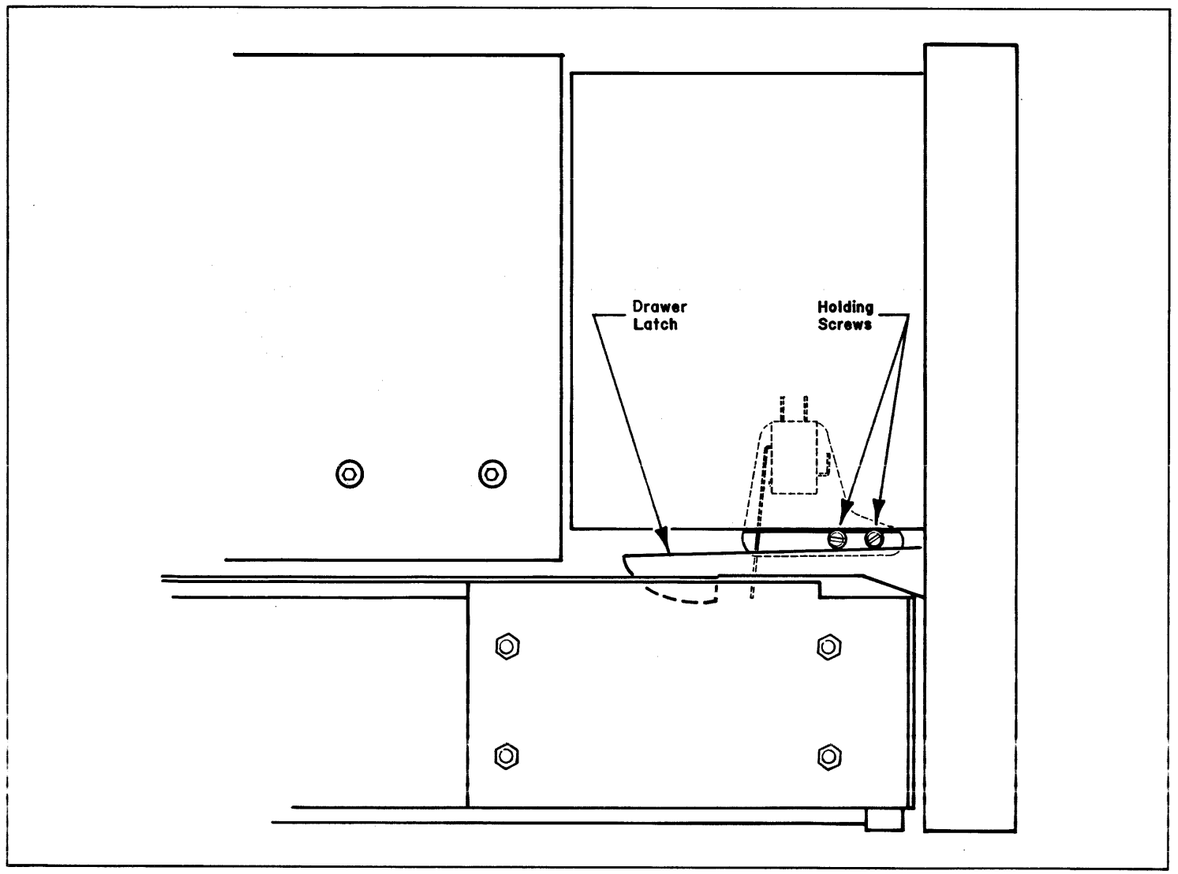


Figure 6-8. Latch and Switch Location

6.6.3.4 Head Carriage Retract Switch Adjustment

1. Loosen the screws and adjust both switches so that the retract switch (the top switch) "makes" when the carriage is .060 ± .020 inch from contacting the read end-stop.
2. Secure screws

   Note: Separate adjustment of the interlock switch (the lower switch) should not be necessary.

6.6.4 Level 2 Adjustments

6.6.4.1 Brush Mechanism Adjustment

1. Lower the front panel to the maintenance position as described in 6.7.2.5.
2. Loosen the three hex-head screws which fasten the brush-motor plate to right front corner of the baseplate as shown in Figure 6-11. For visibility, the bowl, front panel, and other parts have been omitted from the figure.
3. Remove the plenum chamber by removing the two plenum chamber holding screws.
4. Exerting a light clockwise pressure on the upper brush arm, measure the clearance between the brush bristles and the bowl wall. If the clearance is not 0.062 ± .031, loosen the jam nut on the eccentric (A) in Figure 6-12, and rotate the eccentric until proper brush-to-wall clearance is obtained. Tighten the jam nut.
5. If the brush motor arm is not in the position as shown in Figure 6-12, manually rotate the brush motor arm clockwise to that position. Insure that the pin is detented in the rear end of the slot in the brush mechanism link, as shown in Figure 6-12.
6. Slide the brush-motor plate backwards or forward to set the clearance between the eccentric and the brush level to 0.005 ± .004. Tighten the three brush-motor plate screws.

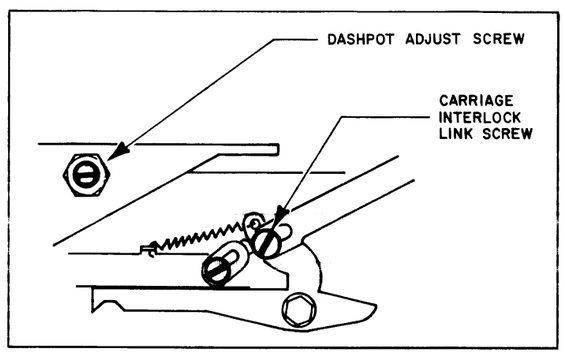


Figure 6-9. Dashpot Adjustment Screw

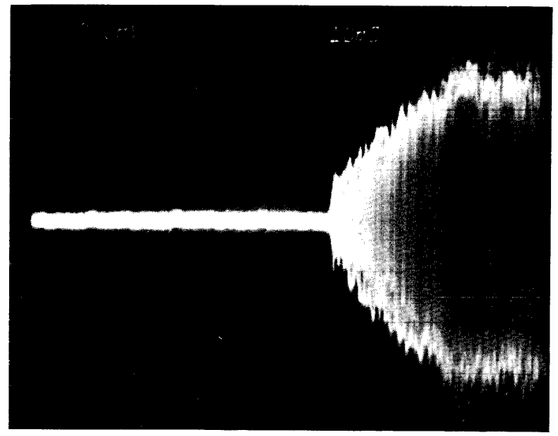


Figure 6-10. Head Load Dashpot Waveform

7. Loosen the two screws holding the brush switch. With the brush mechanism still in the position described in Step (5) preceding, adjust the switch level to be depressed 0.030 ± .005 beyond the "make" point. Tighten the two screws.
8. With drawer and cartridge interlocks defeated as described in 6.6.2(3), place the drive in the RUN mode, and check for proper operation of the brush mechanism. Brushes should make one cycle and then stop.
9. Start another brush cycle by placing the drive in the LOAD mode and then the RUN mode. Remove power to the drive when the brush motor reaches the midpoint of its cycle.
10. Manually push the brushes back into the full retracted position. Apply power to the disk drive.
11. The brush motor cycle should complete, and the pin should be detented in the rear end of the slot in the brush mechanism link. (Note: An additional cycle can occur before the brush motor stops. This is acceptable).

6.6.4.2 Lower Index Transducer Adjustment

Place the drive in the RUN mode, and observe the signal at pin W on the Sensor PCB. The amplitude of the positive peaks should be between 450 and 800 mV. If the signal falls outside the 450-800 mV range, procede as follows:

1. Place the drive in the LOAD mode and, when able, remove the upper disk cartridge.
2. Remove the lower disk per instructions in section 6.7.3.2.
3. Using a plastic feeler gauge, verify transducer lamination-to-sector ring clearance of .008" ± .003", as shown in

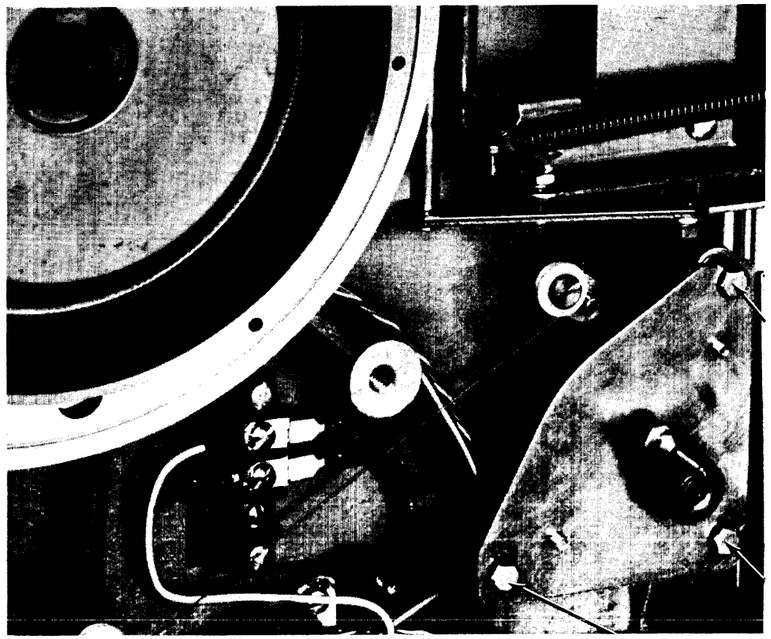


Figure 6-11. Brush Motor Plate

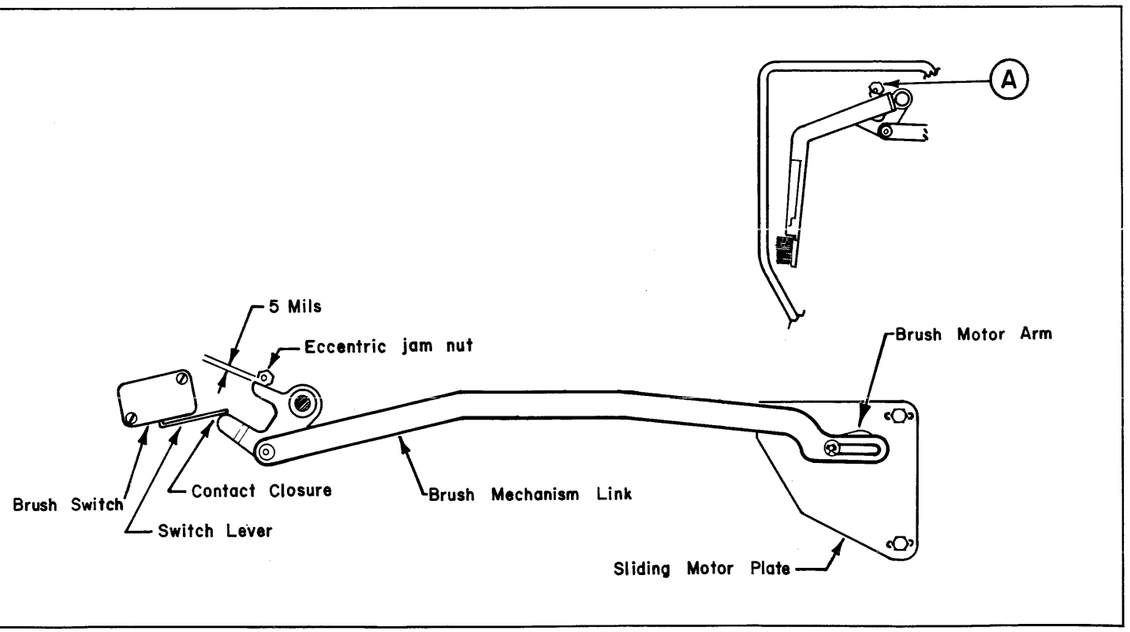


Figure 6-12. Brush Mechanism Adjustments

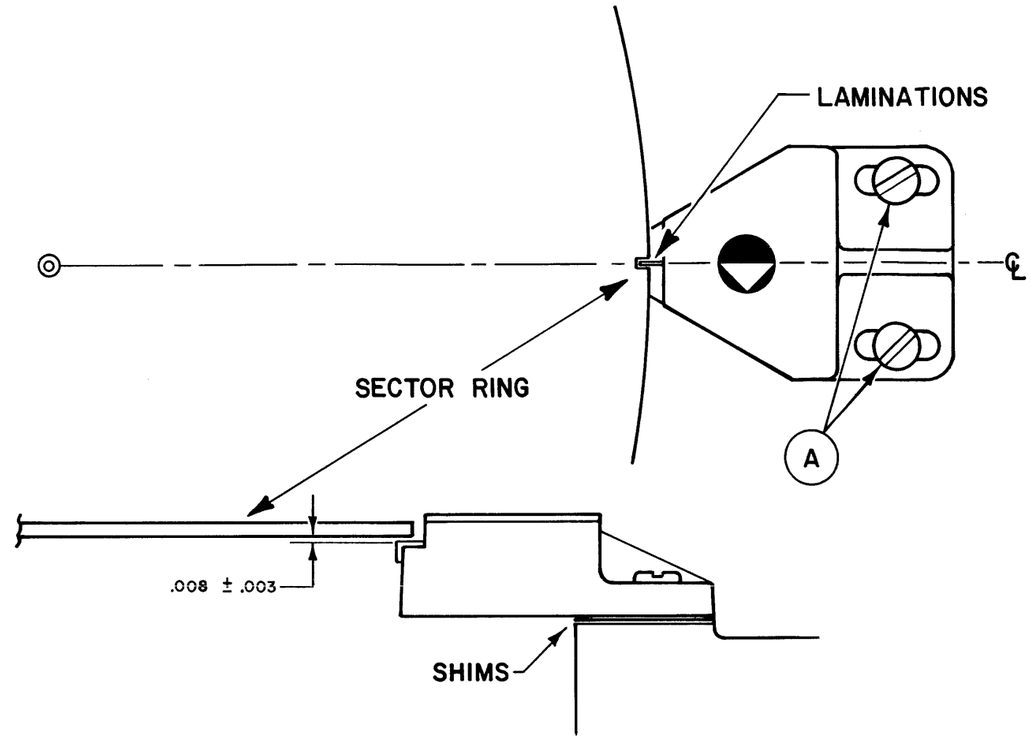


Figure 6-13. Lower Index Transducer Adjustment

Figure 6-13. If the clearance is out of tolerance, loosen screws A, and add or remove shims (P/N 16358) as required. Re-tighten screws A just enough to secure the transducer and still allow slight lateral movement.

4. Align the transducer/lamination center line with the spindle hub center, and move the transducer in or out radially until the inner edge of the lamination is approximately even with the base of the sector slots as observed through one of the holes in the hub.

5. Place the drive in the RUN mode, and observe the signal. Being careful not to greatly disturb its radial alignment with spindle center, move the transducer gently in and out to produce optimum signal level.

6. Hold the transducer in this position and carefully tighten screws A. Recheck the signal for proper level, and readjust as necessary.

6.6.4.3 Adjustment of R/W Heads

6.6.4.3.1 Upper Heads

NOTE

Unit must be removed from its shipping base, and either rack mounted or placed on a stable surface before attempting these adjustments.

To adjust the upper heads, an exerciser or other means of positioning the heads to a desired track, an alignment cartridge, oscilloscope, torque screwdriver, R/W Head Alignment Plug (P/N 25104A), and the head adjustment tool (P/N 16087) are needed. The procedure for adjustment is as follows:

1. Install the alignment cartridge, and then proceed with the alignment, observing the temperature stabilization criteria outlined below.

CAUTION

Thoroughly clean all cartridge/spindle mating surfaces using head cleaning pads listed in 6.2.2. Be certain the cartridge is write protected. If write protect option is not installed, disable write function at controller or CPU.

TEMPERATURE STABILIZATION

The alignment cartridge shall be temperature stabilized to the disk drive operating temperature prior to attempting alignment.

CAUTION

Only after the disk drive has been temperature stabilized can the alignment cartridge stabilization be accomplished.

DRIVE TEMPERATURE STABILIZATION

The Series 40 Disk Drive is temperature stabilized after two hours of head-loaded operation from a cold start-up in the recommended machine operating environment.

ALIGNMENT CARTRIDGE TEMPERATURE STABILIZATION

The time required for temperature stabilization of the alignment cartridge is dependent upon the cartridge storage environment.

- Storage in the Drive Operating Environment– if the cartridge storage temperature is essentially the same as the recommended machine operating environment, the cartridge shall be allowed to run in the drive with heads loaded for *15 minutes* prior to attempting the alignment procedure.

- Storage in Other Than The Drive Operating Environment–if the cartridge storage temperature is essentially different from the recommended drive operating environment, the cartridge shall be allowed to run in the drive with heads loaded for *30 minutes*. After this initial period the cartridge shall be removed, reinstalled, and the drive operated with heads loaded for an additional *15 minutes* prior to attempting the alignment procedure.

2. Lower the card cage to the head-cleaning position as described in section 6.4.2.1, then set up the oscilloscope as follows:

   - Connect channel 1 to TP-1 of R/W board. This provides a differentialted read signal (see logic diagram 11486).

   - Connect channel 2 to pin 11 of SR board (location M06). This provides –SELECTED INDEX MARK (see logic diagram 11411). This line will provide unseparated sector index marks when the Sector Counter Option is installed. Due to the drive electronics, the index pulse will be gated on this line.

   - Trigger on negative (leading) edge–SELECTED INDEX MARK.

   - Set vertical scale for channel 1 to 50 mV/Div–100 tpi, or 20 mV/Div–200 tpi.

   - Set vertical scale for channel 2 to 2 V/Div.

   - Set horizontal scale to 2ms/Div–100 tpi, or 1 ms/div–200 tpi.

3. A. Observe the negative going INDEX signal on channel 2, adjust the variable sweep control until two INDEX pulses appear on the screen, one at the left-most graticle, and one at the right-most graticle, as shown in Figure 6-14. (100 tpi Alignment Cartridge P/N 70306).

   B. Observe the negative going INDEX signal, one at the left-most graticle only. (200 tpi Alignment Cartridge P/N 70709).

4. Position the heads to track 073 (100 tpi) or 146 (200 tpi).

NOTE

Head positioning cannot be done manually. Slew the heads into position using the CPU or an exercisor.

5. Refer to Figure 6-1. Locate the four Head Plugs on the bottom of the Data Channel Box. Physically select the upper disk R/W head to be checked/aligned, and install the R/W Alignment Plug (P/N 25104) between its head plug and companion connector on the Data Channel Box. These plugs are oriented, from the rear forward: upper head/upper disk; lower head/upper disk. The forward most two plugs are for the lower disk heads.

6. Electronically select the head chosen in #5 above. Locate the RDR-1 PCB in the I/O Box. Place the RDR-1 board on an extender for ease of access, and ground the –DISK SELECT input. If the upper head is to be checked, also ground the –HEAD SELECT input. Removing this ground later will select the lower head.

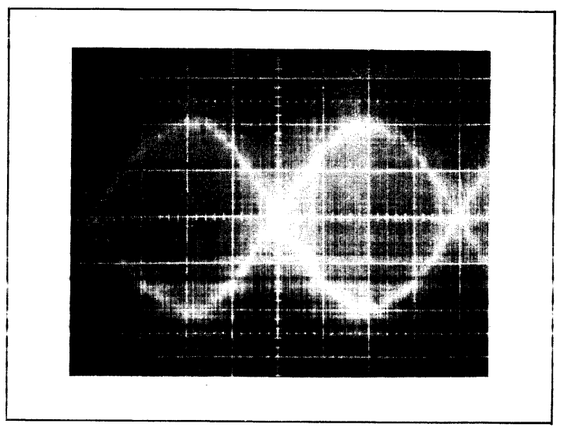


Figure 6-14. 100 tpi Head Properly Aligned

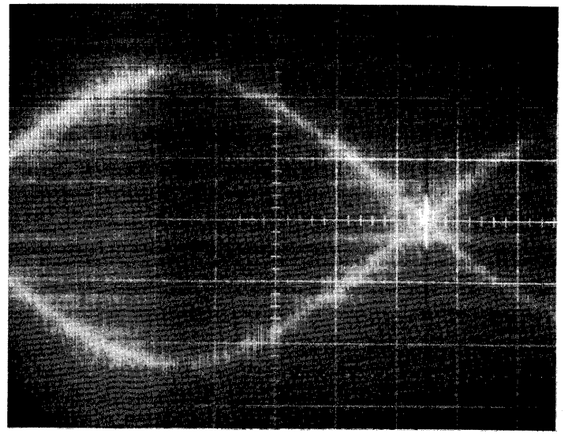


Figure 6-15. 200 tpi Head Properly Aligned

7. Observe the alignment signal presentation on the oscilloscope for channel 1.

8. A. 100 tpi alignment description (using Alignment Cartridge P/N 70306). If the head being checked is properly aligned, the oscilloscope presentation will be approximately as shown in Figure 6-14., with the time between zero crossings for both loops being equal.

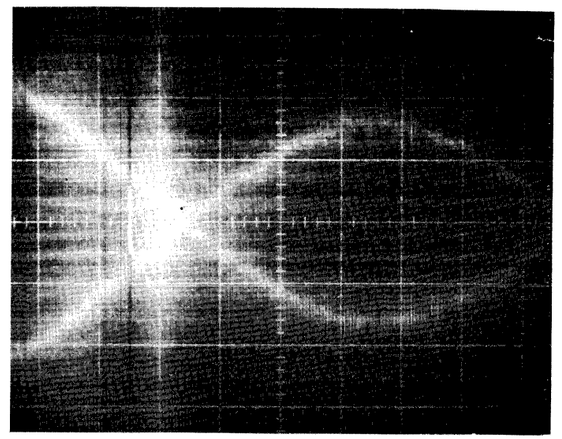


Figure 6-16. 200 tpi Head Misaligned

B. 200 tpi alignment description (using Alignment Cartridge P/N 70709). Observe the oscilloscope pattern, and refer to Figures 6-15 and 6-16.

The oscilloscope pattern should consist of two sinusoidal traces and an alignment marker. When the head is properly aligned, the pattern should resemble that shown in Figure 6-15. A misaligned head will produce a pattern similar to that shown in Figure 6-16.

9. If the head(s) requires alignment, install the R/W Head Adjustment Tool (P/N 16087) as shown in Figure 6-17A. Figure 6-17B may then be referred to during the remainder of the R/W Head Alignment procedure.

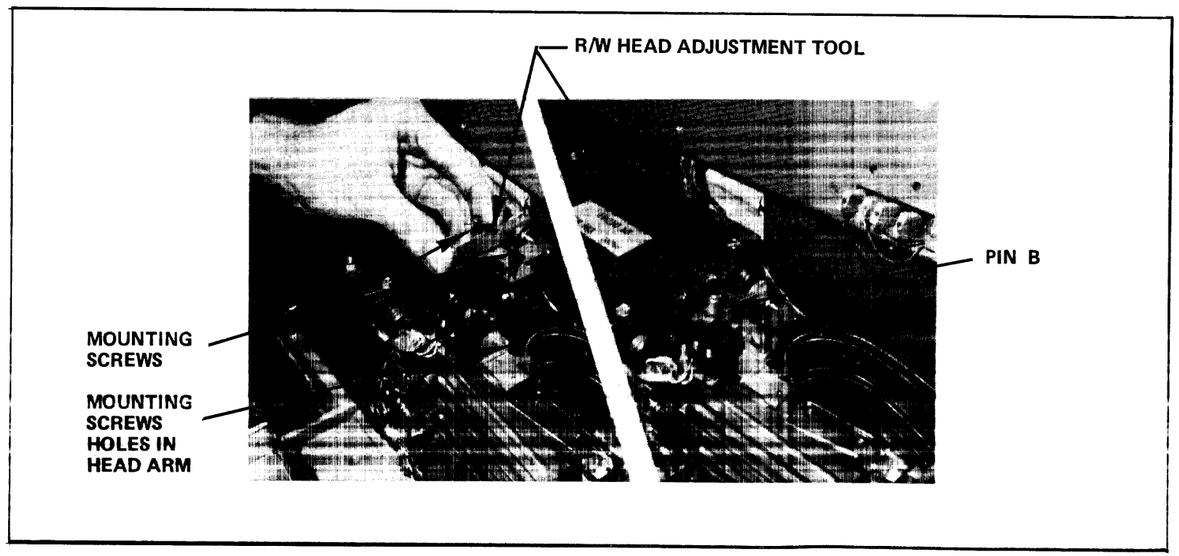


Figure 6-17A. Install R/W Head Adjustment Tool

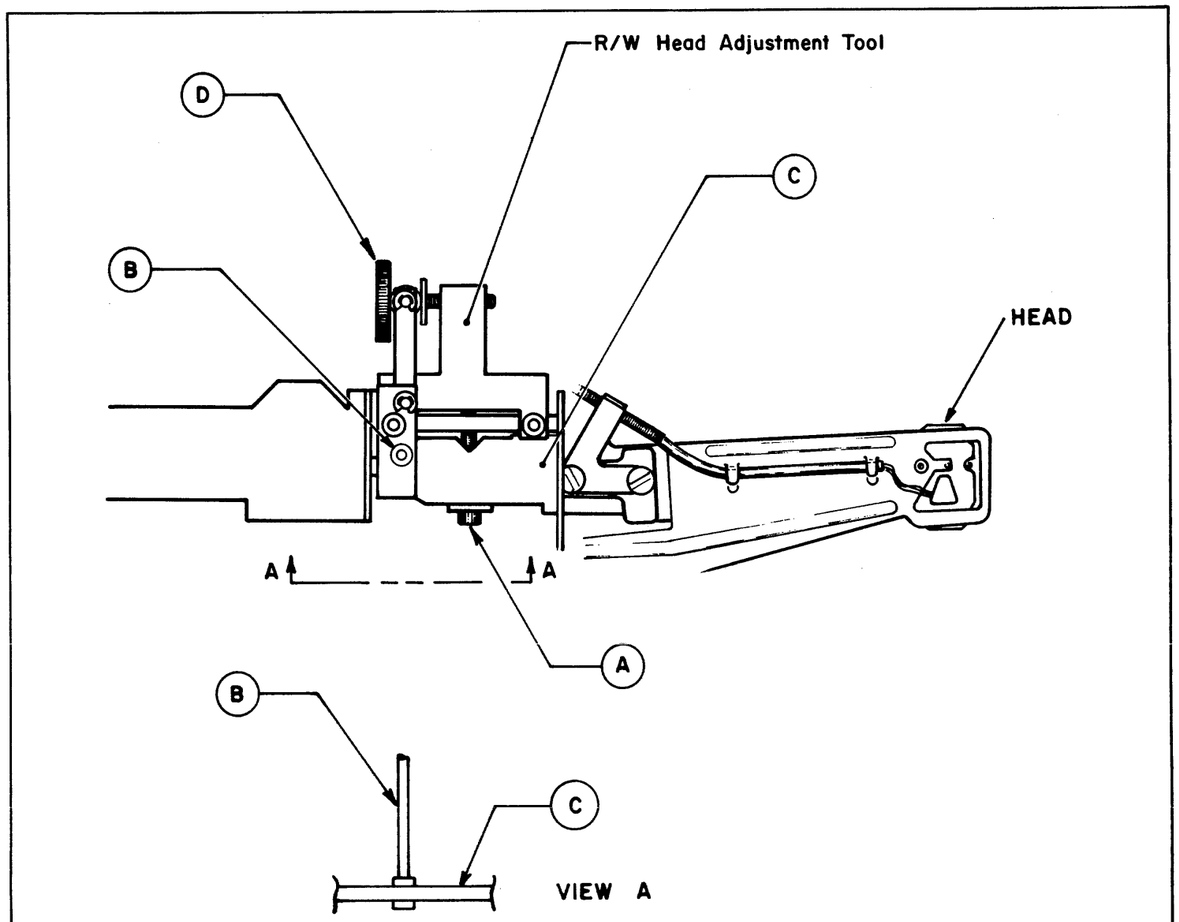


Figure 6-17B. R/W Head Adjustment

a. Slightly loosen screw A of the selected head.

b. Engage the large end of pin B in the large hole in head mounting plate C (see View A)

c. To move the head out (away from the spindle), turn screw D counter-clockwise.

d. To move the head in (toward the spindle), turn screw D clockwise.

e. Tighten screw A to 95 inch ounces.

NOTE

As screw A is tightened, the head may move slightly toward the spindle. If necessary, readjust the head position, allowing for any head movement caused by tightening screw A.

f. Physically and electronically select the opposite head, and repeat steps a through e.

10. Remove the R/W Head Adjustment Tool

CAUTION

Failure to remove the R/W Head Adjustment Tool will result in damage to the R/W Head Positioner Assembly and associated hardware.

11. Switch the unit from RUN to LOAD to retract the heads, and then return to the RUN mode of operation.

12. Reposition the R/W heads back to the alignment track, and recheck the alignment of the heads. Reinstall the R/W Head Adjustment Tool and repeat the adjustment procedure as necessary.

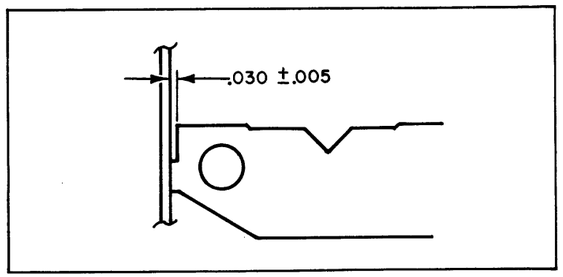


Figure 6-18. Lower Head Adjustment

13. Remove the R/W Head Alignment Plug, and the R/W Head Adjustment Tool as required.

6.6.4.3.2 Lower Heads

Since disk interchangeability is not affected by the lower heads, the adjustment consists of merely lowering the card cage to the head-cleaning position as described in 6.4.2.1, inserting a 0.030 ± .005 shim between the head mounting plate and the carriage roller plate, tightening the set screw to 95 inch-ounces, and removing the shim. This adjustment is shown in Figure 6-18.

6.6.4.4 Upper Index Transducer Adjustment

Install an alignment cartridge (100 tpi—P/N 70306, 200 tpi—P/N 70709). Place the drive in the RUN mode, and observe the signal at pin V on the Sensor PCB. The amplitude of the positive peaks should be between 165 and 450 mV for narrow sector slots, or between 300 and 1000 mV for wide sector slots. If the signal falls outside the appropriate range, proceed as follows:

1. Place the drive in the LOAD mode and, when able, remove the alignment cartridge.

2. Verify the transducer lamination-to-sector ring clearance of .008" ± .003" by laying a straight-edge across the spindle hub and checking the gap between its lower edge and the top of the lamination with a plastic feeler gauge. If the clearance is out of tolerance, loosen the hold-down screws (same as screws A in Figure 6-13), and add or remove shims (P/N 16358) as required. Retighten the screws just enough to secure the transducer and still allow slight lateral movement.

3. Align the transducer/lamination center line with the spindle hub center, and move the transducer in or out radially until the tip of the lamination clears the outside of the spindle hub flange by approximately 3/64". Tighten the hold-down screws a little.

4. Reinstall the alignment cartridge, switch from LOAD to RUN mode and, when able, recheck the signal level. If the signal is in tolerance, the cartridge may be removed and the hold-down screws tightened firmly. If the signal is not in tolerance, repeat step 3—moving the transducer radially a small amount either in or out each time until optimum signal level is achieved.

NOTE

A disk hub and sector ring, retrieved from a defective disk cartridge and used here in a manner similar to the procedure outlined for the lower transducer, will appreciably shorten the time needed to achieve a proper signal level.

5. Locate the index transducer base plate, which is screwed to the outside front of the bowl assembly at the centerline. This plate, shown in Figure 6-19, has four hex-head fastening screws ("A") and a slotted-head adjustment screw ("B").

6. Slightly loosen the four fastening screws just enough to permit side movement of the transducer base plate.

7. Install the alignment cartridge, place the drive in the RUN mode, and select the upper disk.

8. Using the exerciser, seek to track 5 (100 tpi) or track 10 (200 tpi).

9. Using the leading edge (negative-going) of the index pulse at Pin 11 of the Sensor PCB as a trigger, observe the signal at TP1 of the R/W amplifier PCB. This signal is shown in Figure 6-20. Note the long pulse followed by a long burst of signal. The long pulse is the read gate.

10. Using the adjustment screw, position the index transducer so that the leading edge of the read gate occurs 18.8 μs after the leading edge of the index mark. (Note: for 1500

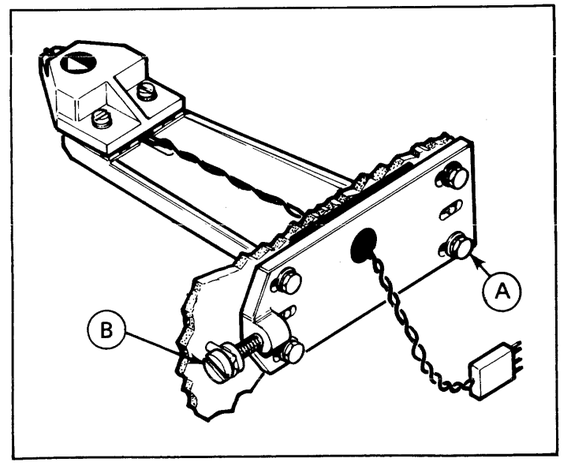


Figure 6-19. Index Transducer Adjustment

rpm drives the proper setting is 30 μs ± 5μs). Do not tighten the fastening screws yet.

11. Alternately selecting each of the upper heads, adjust the index transducer so that the read gate is symmetrical around the 18.8 μs point (30 μs for 1500 rpm). Pulse separation between the heads shall not exceed 6.25 μs (10 μs for 1500 rpm).

12. Tighten the four fastening screws, observing that tightening the screws does not result in misalignment.

13. Return the front panel to the operating position.

6.6.4.5 Fine Track-zero Adjustment

To perform the track zero adjustment, a disk pack, exerciser, and oscilloscope are necessary. If the track zero adjustment is being made as part of a Head Positioner or Spindle Assembly replacement, or if for any other reason it is considered that the track zero adjustment could be more than three tracks off, then the adjustment is considered Level 3, and the procedure of 6.6.5.1 should be followed. When the adjustment is not done as part of Head Positioner or Spindle Assembly replacement, proceed as follows:

1. Install the disk pack and place the disk drive in the RUN mode.

2. Locate the track-zero adjustment screw. This is a hexagon socket screw located just below the bail plate as shown in Figure 6-21.

3. Using position term (TP14 on Servo PCB) as trigger, observe the waveform at TP13.

4. When the drive goes ready, alternately seek to track-zero and restore.

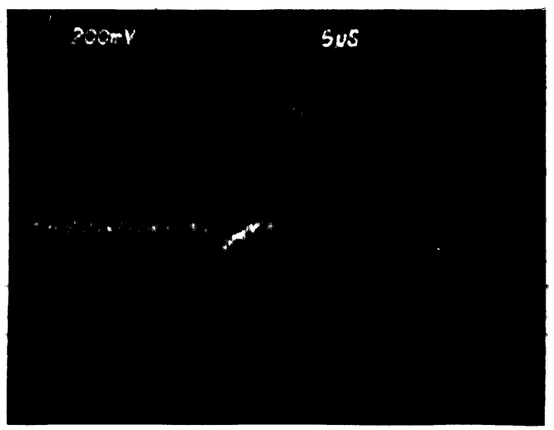


Figure 6-20. Upper Index Transducer Waveform

Figure 6-21. Track Zero Adjustment Screw

5. Using a 9/64 "L" shaped Allen wrench, turn the adjustment screw to obtain waveform shown in Figure 6-22.

6. Check the alignment of the R/W heads following the procedure described in 6.6.4.3.1.

6.6.5 Level 3 Adjustments

6.6.5.1 Major Track-zero Adjustment

Major track-zero adjustment requires an alignment pack, exerciser, oscilloscope, alignment bar (P/N 16439), and spindle cone (P/N 15171). Proceed as follows:

NOTE

When the adjustment is not done as part of Head Positioner or Spindle Assembly replacement, see 6.6.4.5.

1. Remove the R/W Head Assembly from position H-00, if one is installed.

2. Install the alignment bar in head position H-00 tight against the rear plate, and tighten the head assembly set screw (see Figure 6-23).

3. Install the spindle cone on the spindle, with the flat surface parallel to the front panel. (Note: flat surface of cone is not a datum surface).

4. Jumper TP1 to TP2 on the Sequence Logic PCB, and remove the Spindle Drive PCB. This bypasses the drawer-closed and disk-pack-installed interlocks, and prevents spindle rotation.

5. Move the alignment bar so that its tip is firmly touching the cone's flat surface.

6. Apply power to the drive.

7. Depress the carriage retract microswitch, which is the top microswitch at the rear end of the bail.

8. Place the disk drive in the RUN mode. The carriage will move forward.

9. Locate the track-zero adjustment screw. This is a hexagon socket screw located just below the bail plate as shown in Figure 6-21 and 6-23. It requires a 9/64 "L" shaped Allen wrench.

10. Attempt to rotate the cone counter-clockwise. If the round part of the cone touches the alignment bar, turn power off and rotate the adjusting screw counter-clockwise approximately 1/8 turn.

11. Repeat Steps (5) through (9) until the clearance between the cone flat surface and the alignment bar is 0.006 inches ± .004 inches.

12. Turn power off, remove the cone and the alignment bar, remove the jumper from the Sequence Logic PCB, and replace the Spindle Drive PCB.

13. Remove the alignment bar and install the R/W Head Assembly in position H-00.

14. Perform the adjustments described in 6.6.4.5 and 6.6.4.3.1, respectively.

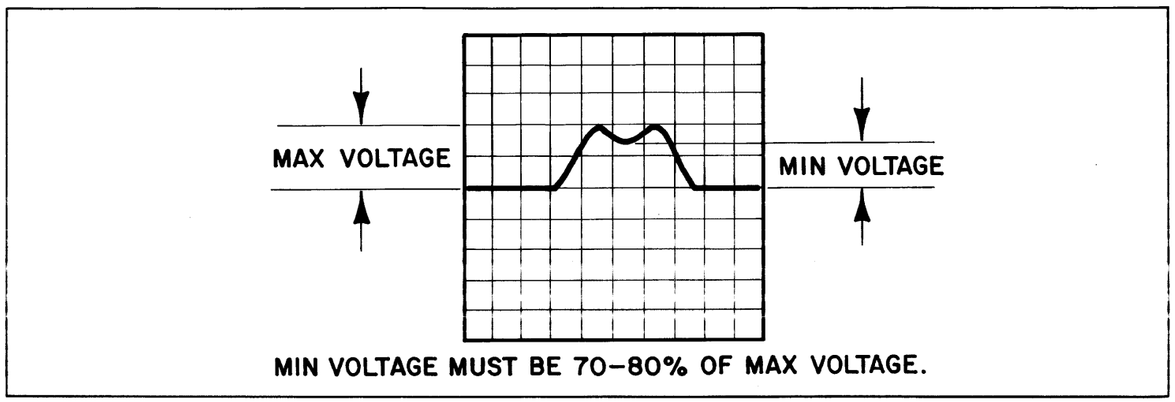


Figure 6-22. Track Zero Waveform

6.6.5.2 Head-Positioner Alignment

To align the Head Positioner with the Spindle Assembly, it is necessary to use the alignment bar (P/N 16438), the spindle cone (P/N 15171), and the head-positioner alignment tool (P/N 16372). Proceed as follows:

1. Remove the R/W Head from position H-00, if one is installed. Install the alignment bar in position H-00, tight against the rear plate. Tighten the head assembly set screw (see Figure 6-23).

2. Install the spindle cone on the spindle with the flat surface parallel to the front panel.

3. Install the head-positioner alignment tool. This tool is fastened to the disk drive base plate, just behind the air filter, as shown in Figure 6-23.

4. Loosen the six screws mounting the Head Positioner to the base-plate. The four rear screws fasten from the underside, and are accessible from the rear or underside of the disk drive. The two front screws are accessible from the top.

5. Turn the screw on the head-positioner alignment tool until the clearance between the bar and the round portion of the cone is 0.002 inches ± .001.

6. Tighten the head positioner mounting screws and remove the bar, cone, and alignment tool.

6.7 REMOVAL/REPLACEMENT OF ASSEMBLIES & PARTS

6.7.1 Location of Instructions

Table 6-2, which is arranged alphabetically, shows the location within this section of instructions for removal or replacement of various Series 40 assemblies, sub-assemblies, and parts. Prior to

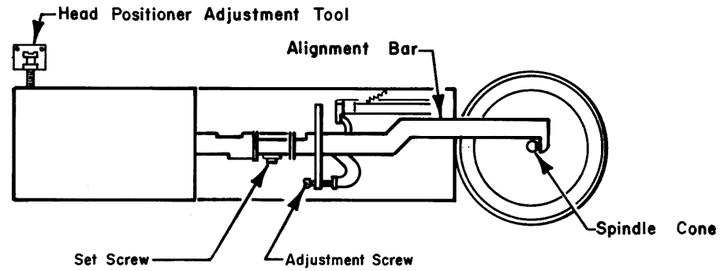


Figure 6-23. Alignment Bar and Cone

attempting any disassembly of the Series 40, service personnel should become familiar with the nomenclature and location of assemblies as shown in Para 6.3. Except for removal of front-panel and I/O components, the first step in any of the procedures of this paragraph (6.7) is removal of the top cover, as described in 6.7.2.1.

Table 6-2.

Assy/Component	Part No.	Manual Paragraph
Air Filter	16163	6.4.2.3
Base-plate-mounted components	various	6.7.4.3
Bowl Assembly	16447-02	6.7.4.1
Brushes	16082	6.7.2.12
Brush Motor	16023	6.7.3.3
Card Cage PCBs	various	6.7.2.3
Cartridge (with power off)	———	6.7.2.2
Cartridge Retainer Assembly	16143	6.7.4.2
Disk Pack Safety Solenoid	16017	6.7.4.3
Drawer Interlock Solenoid	15302	6.7.2.5
Front Panel	16016	6.7.2.6
Front Panel components	various	6.7.2.5
Head Load Solenoid	16362	6.7.2.13
Head Positioner	16010	6.7.4.5
Heat Sink Assembly	16712	6.7.2.7
Heat Sink PCB and components	various	6.7.2.8
I/O Mother Board	11400-01	6.7.2.11
I/O PCBs	various	6.7.2.4
Index Transducers	16361	6.7.3.4
Interlock linkage parts	various	6.7.4.3
Lower Disk	16483	6.7.3.2
Main Harness	11508	6.7.4.6
Mother Board	11400-20	6.7.2.10
R/W Amplifier PCB	11486	6.7.2.9
R/W Heads	16272	6.7.3.1
Slide Assemblies	16024	6.7.2.14
Spindle Assembly	16117	6.7.4.4
Top Cover	16019	6.7.2.1
Unit Home Switch	70275	6.7.2.5

6.7.2 Level 1 Removal/Replacement

6.7.2.1 Top Cover

The top cover is held in place by securing screws, which must be removed in order to take the top cover off. Four are on the top surface around the rear periphery of the bowl, as shown in Figure 2-2.

6.7.2.2 Removal of Cartridge with Power Off

1. Loosen the screw at the left edge, middle, of the data channel box (see Figure 2-4). Lift the data channel box, and observe the position of the head carriage assembly. If it is not already fully retracted, manually retract it.

2. To insure that the brushes are fully retracted, locate the brush lever and eccentric on the right side of the drive (see Figure 6-24). Rotate the brush lever clockwise until it hits the eccentric, if it is not already in that position.

3. Spread the cartridge-retaining clamps as described in 6.6.2(2), and remove the cartridge.

6.7.2.3 Card-Cage PCBs

To remove card-cage PCBs, lower the card cage to the maintenance position as described in 6.4.2.1. Location of the PCBs is shown in Figure 6-3, and each PCB is clearly marked in the upper front corner of the board. Figure 6-25 shows the method of board removal.

6.7.2.4 I/O PCBs

After removal of the slotted plate at the bottom rear of the I/O box, the pluggable I/O PCBs are removed simply by sliding them out of their slots.

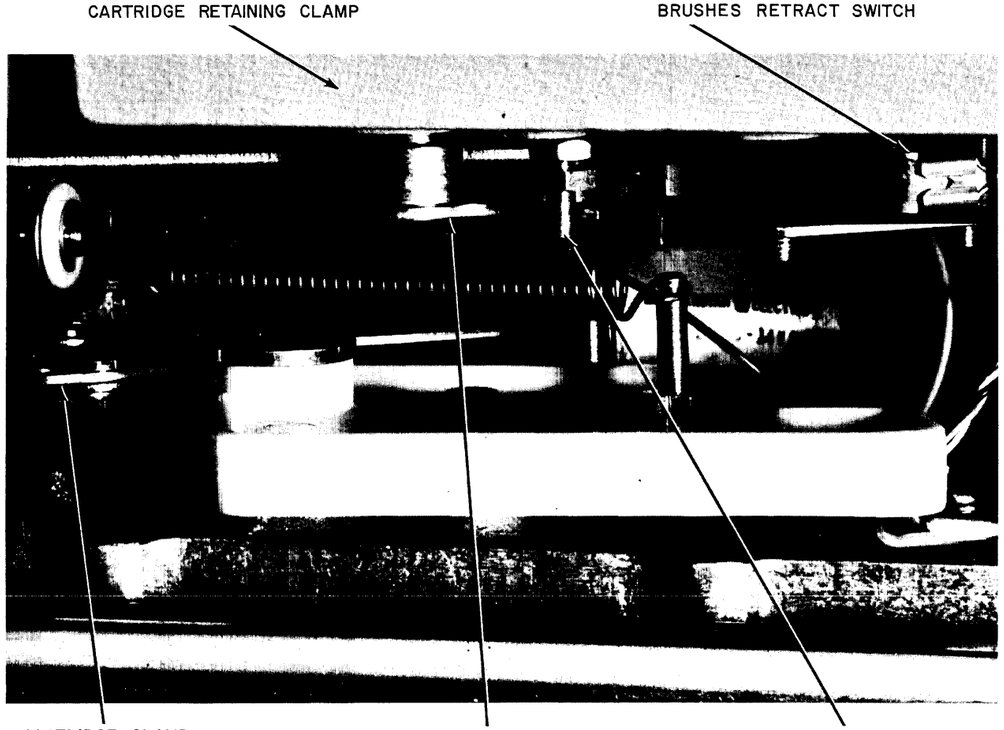


Figure 6-24. Brush Mechanism

6.7.2.5 Front-Panel Components

Front-panel components are accessible for removal or replacement by removing the two hexagon socket screws which hold the front panel in position. Access to these screws is through two holes, one on each side of the bowl, as shown in Figure 6-26. To permit the front panel to swing freely, two lower screws, one on each side, may require loosening. These screws are located between the front panel and the lower section of the slide inner member. The front panel now swings down partially, giving access to components mounted on the rear of the front panel. Some components mounted on the pan or baseplate are also accessible by lowering the front panel.

6.7.2.6 Front Panel

To remove the front panel, first lower the panel to the maintenance position as described in 6.7.2.5. Then unplug the panel distributor PCB connectors, and remove the screw-type connections, which connect the panel distributor PCB with the remainder of the disk drive. Remove the two hexagon socket screws which hinge the front panel to the pan.

To replace the front panel, perform the preceding operations in reverse order. When closing the front panel, insure that the interlock pins (see Figure 6-27) properly engage the side drawer latches. If necessary, adjust the two set screws in the front handle stiffener so that the drawer handle is approximately flush with the face of the front panel, and so that the side latches work properly. If proper adjustment is not possible using only the set screws, the striker plate may need adjustment as described in 6.6.3.2.

6.7.2.7 Heat Sink Assembly

To remove the Heat Sink Assembly it is necessary to disconnect all cable harnesses and individual wires which connect the Heat Sink Assembly with other parts of the disk drive. This involves removing a harness clamping bar, unplugging two connectors, and disconnecting screw-type terminals. The clamping bar, connectors, and terminals are all located on the heat sink PCB.

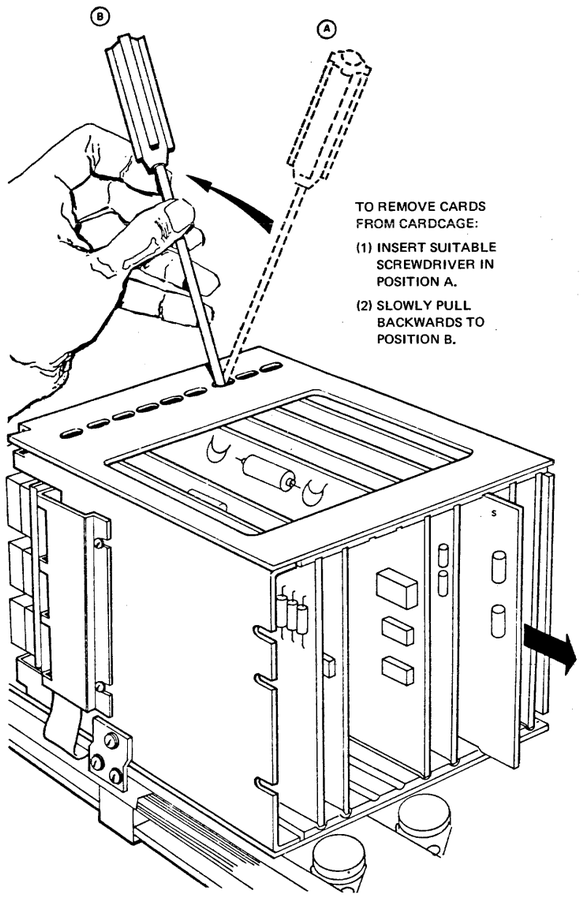


Figure 6-25. Removal of Pluggable PCBs

Disconnected wires should be tagged to insure accurate reconnection. After electrical disconnection, remove the screw holding the Heat Sink Assembly to the top of the card cage and the two screws hinging the bottom of the Heat Sink Assembly. Installation is performed in reverse order.

6.7.2.8 Heat Sink PCB and Components

Most electronic components in the Heat Sink Assembly are directly accessible after removal of the top cover. Additionally, access to the ten power transistors, two power resistors, and the servo release switch is accomplished by removing the screw holding the Heat Sink Assembly to the card cage.

Access to the rear of the heat sink PCB is accomplished as follows:

1. Remove the screw holding the Heat Sink Assembly to the top of the card cage.
2. Remove the screws which mount the ten power transistors to the heat sink.
3. Detach the two power resistors and the servo release switch on the front of the heat sink.
4. Remove the seven screws which hold the PCB to the heat sink. These screws are shown by arrows on Figure 6-28. The PCB will now swing partially clear of the heat sink. If complete removal of the PCB is required, follow the preceding steps and then disconnect all wires and cable harnesses which connect the Heat Sink Assembly to the remainder of the disk drive. An alternate procedure is first to remove the Heat Sink Assembly as described in 6.7.2.7 and then to follow Steps (2) through (4) of this paragraph (6.7.2.8).

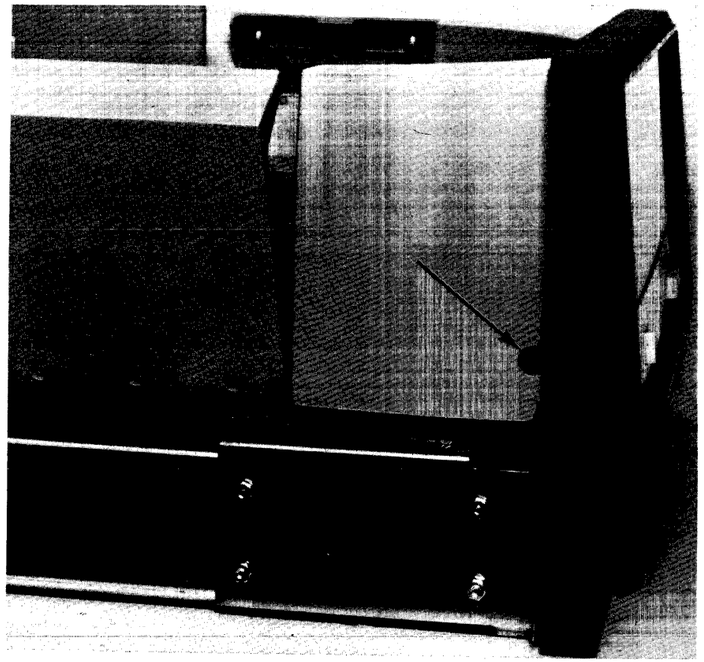


Figure 6-26. Front Panel Holding Screw Access

6.7.2.9 R/W Amplifier PCB

1. Remove the top cover of the data channel box. This is accomplished by removing two hex nuts from the rear corners of the cover, two screws from the front corners.
2. Remove the stand-off collars which support the rear corners of the cover.
3. Disconnect the PCB electrically. This is accomplished by unplugging the two connectors, removing the four screw-terminal connections, and disconnecting the head cables.
4. Remove the mounting screw at J82 on the PCB. The PCB can now be lifted out.

Installation is accomplished by following the preceding steps in reverse order.

6.7.2.10 Mother Board

To remove the mother board, proceed as follows:

1. Remove all pluggable PCBs from the card cage.
2. On the top of the card cage remove the clamping plate which holds the three cable harnesses against the card cage.
3. Remove the two screws which hold the three-connector clamp in place. Unplug the three connectors.
4. Lower the card cage to the head-cleaning position as described in 6.4.2.1.
5. Remove the triangular clamp assembly which holds the cable harnesses to the bottom of the card cage.
6. On the bottom edge of the mother board, unplug the two connectors and remove the +5V and ground connections. It is necessary to remove two screws from each connector in order to unplug the connectors.

7. Remove the eight screws which fasten the mother board to the card cage frame. Slide the mother board out.

To install the mother board, follow the preceding steps in reverse order.

6.7.2.11 I/O Mother Board

6.7.2.11.1 Removal

1. Remove the slotted plate covering the I/O PCBs.
2. Remove the two screws below the bottom I/O connector. Remove the rear I/O cover plate.
3. Remove all pluggable PCBs from the I/O box.
4. Looking inside the I/O box from the rear, remove the two screws from the horizontal bottom flange below the card connectors.
5. From the front of the I/O box, remove the six screws holding the I/O box shield (front cover) and remove the shield.
6. Unplug the two connectors on the front, bottom of the I/O mother board.
7. Disconnect the four wires which are connected by screw terminals to the back of the I/O mother board.
8. Remove the two screws from the back of the I/O module assembly, located over the power connector and the top I/O connector.
9. From the front of the I/O mother board, remove the four screws holding the mother board to the I/O module assembly. Two of these screws are on the bottom edge of the mother board, and two are half-way up.
10. Slide the I/O mother board out of the I/O module assembly.
11. Remove the two screws holding the small power connector PCB to the I/O mother board.

6.7.2.11.2 Installation

To install the I/O mother board, follow preceding steps in reverse order. When re-installing the I/O box shield (Step 5), insure that the two ground wires are installed. Do not tighten the six screws until the flange screws removed in Step (4) are in place.

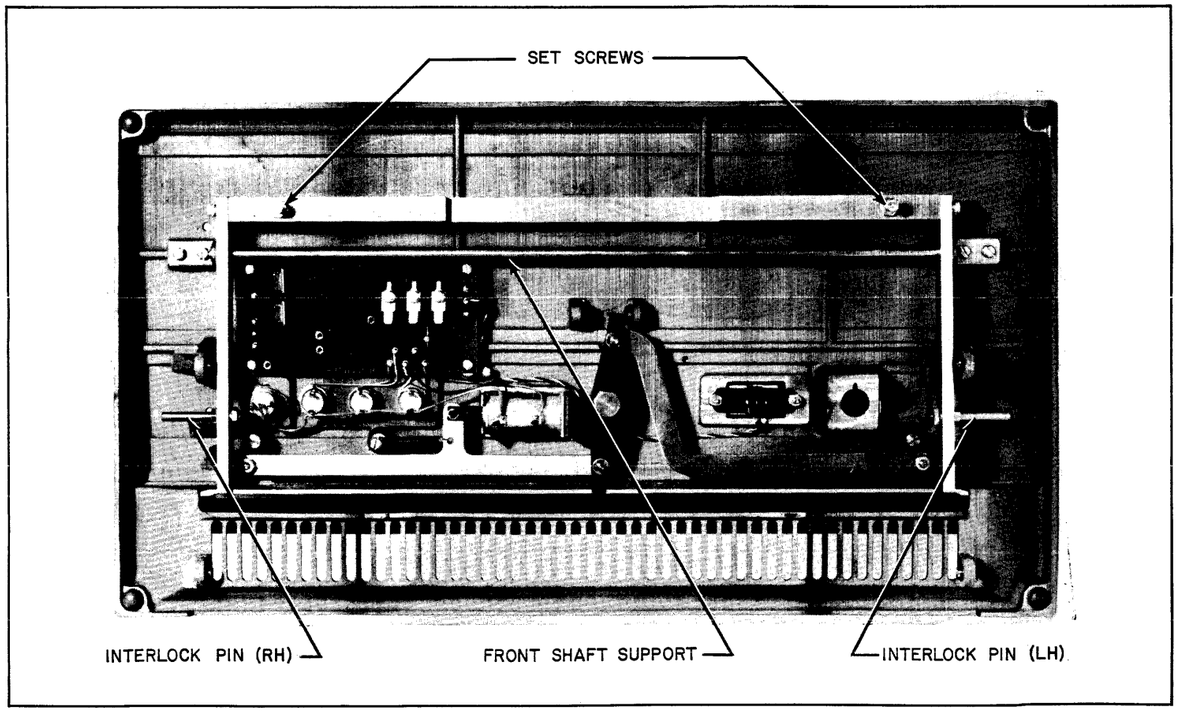


Figure 6-27. Front Panel Adjustments

6.7.2.12. Brushes

To remove the brushes, loosen the set screw which fastens the brush lever to the brush mechanism shaft. See Figure 6-24. Rotate the brush arm out into the bowl for easy access to the brushes. Loosen the set screw holding the brush in the arm, and remove the brush. Follow the procedure in reverse for installing a new brush. Insure that the brush arms are returned to their original position prior to tightening the brush level set screw.

6.7.2.13 Head-Load Solenoid

The head-load solenoid is removed as follows:

1. On the underside of the disk drive, remove the head-load solenoid access cover plate at the rear of the pan.
2. Disconnect the two solenoid leads from the terminal block next to the solenoid.
3. Remove the two "C" clips from the head-load linkage and the dashpot linkage, as shown in Figure 6-29. Disconnect the two linkages.
4. Remove the three mounting screws, also shown in Figure 6-29, which fasten the solenoid to the baseplate. Remove the solenoid.

Installation of the head-load solenoid is accomplished by following the foregoing procedure in reverse.

6.7.2.14 Slide Assemblies

Each slide assembly is fastened to the pan by two screws. With the slide fully extended these screws can be seen on the lower track to the front and in the middle. To remove the slide assembly, simply remove the two screws.

6.7.3 Level 2 Removal/Replacement

6.7.3.1 R/W Heads

If lower heads are to be removed or installed, the lower disk should be removed first. Although removal or installation of lower heads is possible with the lower disk in place, the possibility of scratching the disk surface is high.

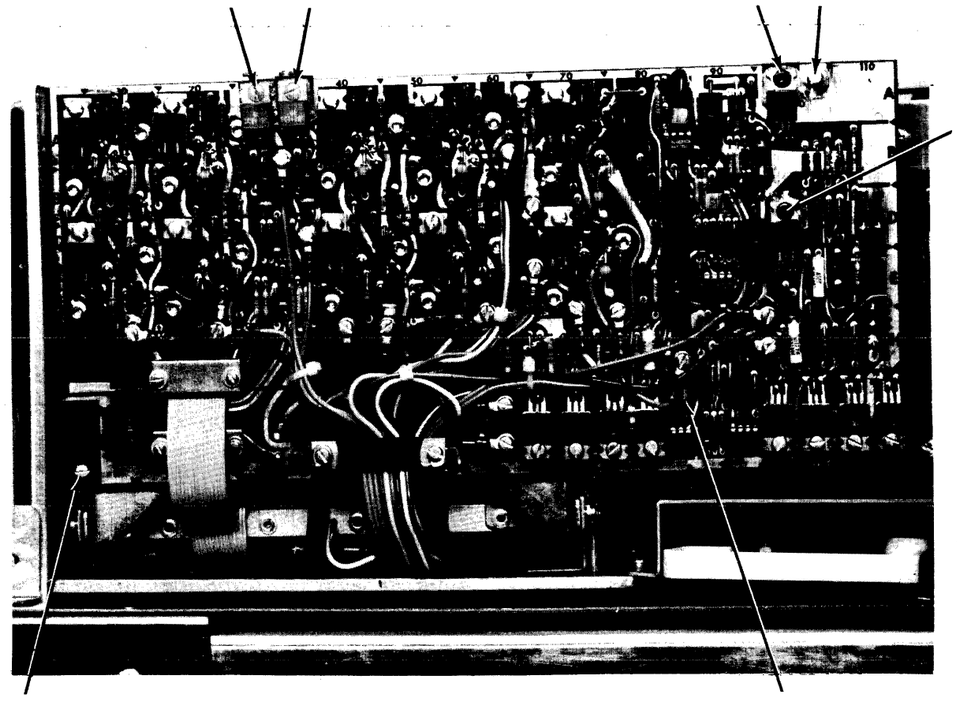


Figure 6-28. Heat Sink PCB

6.7.3.1.1 Removal

1. If applicable, remove the lower disk as described in 6.7.3.2.

2. Loosen the data channel box securing screw (see Figure 2-4), and swing the box up into the maintenance position.

3. Electrically disconnect each head to be changed by loosening the clamp which holds the flexprint cable to the head load bracket, unplugging the connector on the data channel box, and removing or loosening any other cable clamp holding the head wiring.

4. Loosen the hexagon-socket set screw which holds the head assembly in the carriage (see Figure 6-30).

5. Holding the head carriage in position, slide the head assembly straight forward out of its slot.

6.7.3.1.2 Installation

1. Insert the head assembly into the carriage. Torque the set screw to 25 inch-ounces. Install the head-load springs.

2. Electrically connect the head to the data channel box. Reinstall and/or tighten cable clamps.

3. Perform head adjustments as required by Figure 6-5.

4. Reinstall the lower disk, if applicable.

6.7.3.2 Lower Disk

6.7.3.2.1 Removal

1. Lower the front panel to the maintenance position as described in 6.7.2.5.

2. Spread the cartridge retaining clamps as described in 6.6.2(2).

3. Remove the four screws holding the lower disk cover to the inside of the bowl. Remove the lower disk cover.

4. The upper index transducer assembly is held to the front outside surface of the bowl by four screws as shown in Figure 6-19. Detach the index transducer assembly, and withdraw it from the bowl recess far enough so that the lower disk can be removed without striking it. Insure that the assembly is withdrawn straight forward, so that the adjusting screw and fork are not damaged.

5. Remove the eight screws holding the spindle clamp ring. This ring holds the lower disk to the spindle assembly.

6. Remove the lower disk, being careful not to scratch the disk surface. Avoid touching the surface of the disk. If the disk is to be reinstalled, or otherwise reused, store it in a manner that will protect its recording surfaces.

6.7.3.2.2 Installation

During installation of the lower disk, exercise caution to insure that the disk's recording surfaces remain free of contamination, including fingerprints.

1. Using pads soaked in 91% isopropyl alcohol, thoroughly clean all the disk surfaces and also the spindle surface on which the disk seats. Polish the disk to remove all alcohol residue.

2. Place the disk on the spindle, insuring that it is properly seated. Place the spindle clamp ring on the disk, grooved side down.

3. Line up the eight screw holes, and install the screws. Do not tighten the screws more than finger tight.

4. Snug-up two opposite screws. Use very light torque; this is not final tightening.

5. Snug-up two more opposite screws 90° from the first two.

6. Snug-up the remaining four screws in opposite pairs as in (4) and (5) preceding.

7. Following the sequence given in the preceding three steps, tighten the spindle clamp ring screws. Only moderate torque is required.

8. Replace the upper index transducer. Do not tighten the mounting screws.

9. Reinstall the lower disk cover, insuring that the cut-out for the upper index transducer is properly oriented.

10. Adjust the upper index transducer as described in 6.6.4.4.

11. Close the front panel and reinstall the two front panel retaining screws.

6.7.3.3 Brush Motor

6.7.3.3.1 Removal

1. Lower the front panel to the maintenance position as described in 6.7.2.5.

2. The brush motor is located at the right front corner of the baseplate as shown in Figure 6-11. For visibility, the bowl, brush link, front panel, and other parts have been omitted from the figure. Disconnect the brush mechanism link by removing the pin holding the link to the brush-motor crank arm. The head of the pin is slotted, and the pin is removed

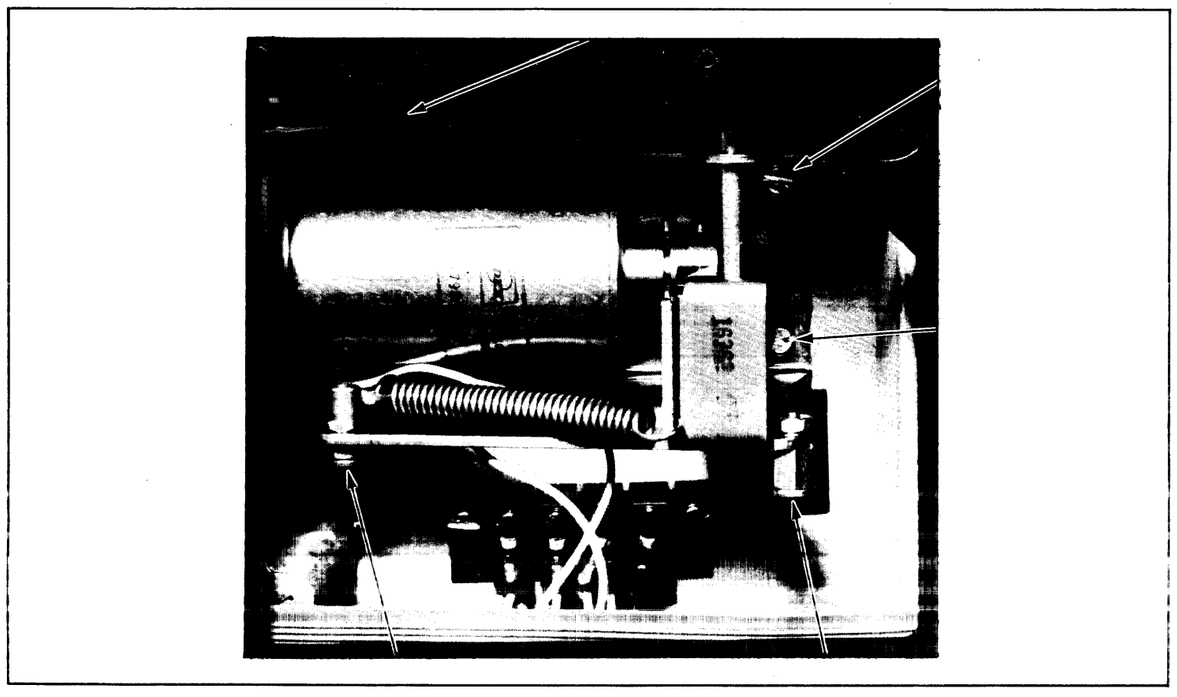


Figure 6-29. Head Load and Dashpot Linkages

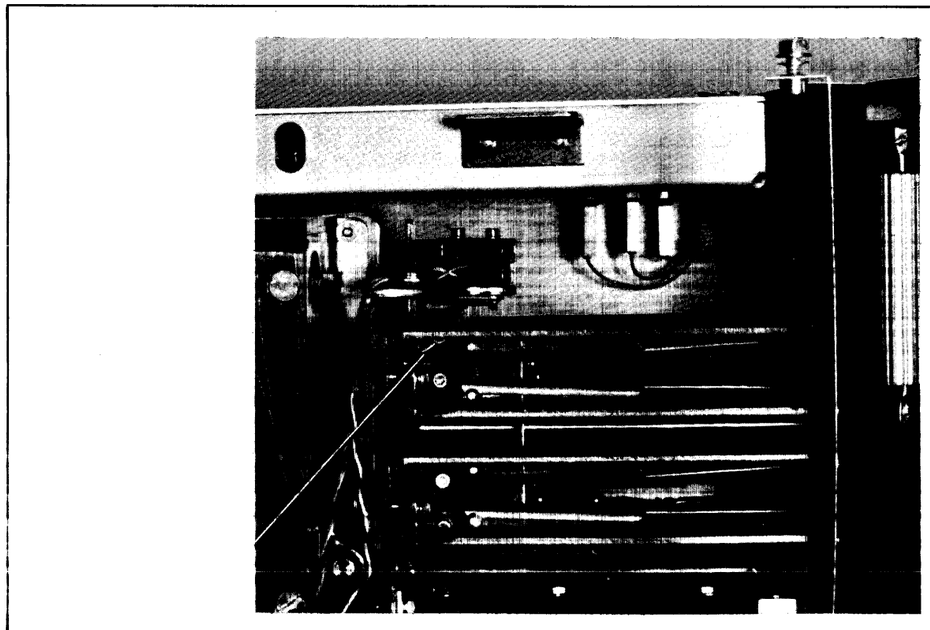


Figure 6-30. Head Assembly Set Screw

by removing the nut holding it to the crank arm. Retain the washers and spring for re-installation.

3. Pull off the two tab receptacles by which the brush motor is electrically connected to the terminal block at the left of the brush motor.

4. Remove the three screws which fasten the brush motor plate to the baseplate. Remove the brush motor assembly.

6.7.3.3.2 Installation

1. Perform the steps listed in 6.7.3.3.1(2) through (4) in reverse, but do not tighten the three brush-motor mounting plate screws.

2. Adjust the brush mechanism as described in 6.6.4.1.

3. Return the front panel to the operating position.

6.7.3.4 Index Transducers

6.7.3.4.1 Upper Index Transducer

1. Lower the front panel to the maintenance position as described in 6.7.2.5.

2. Spread the cartridge clamps as described in 6.6.2(2).

3. Remove the four screws holding the lower disk cover to the inside of the bowl. Remove the lower disk cover.

4. Unplug the upper index transducer connector. This is the upper connector on the panel distributor PCB on the rear of the front panel.

5. The upper index transducer leads pass through a grommet in the transducer baseplate. Push the grommet out into the bowl, and pass the leads and connector through the grommet hole in the baseplate.

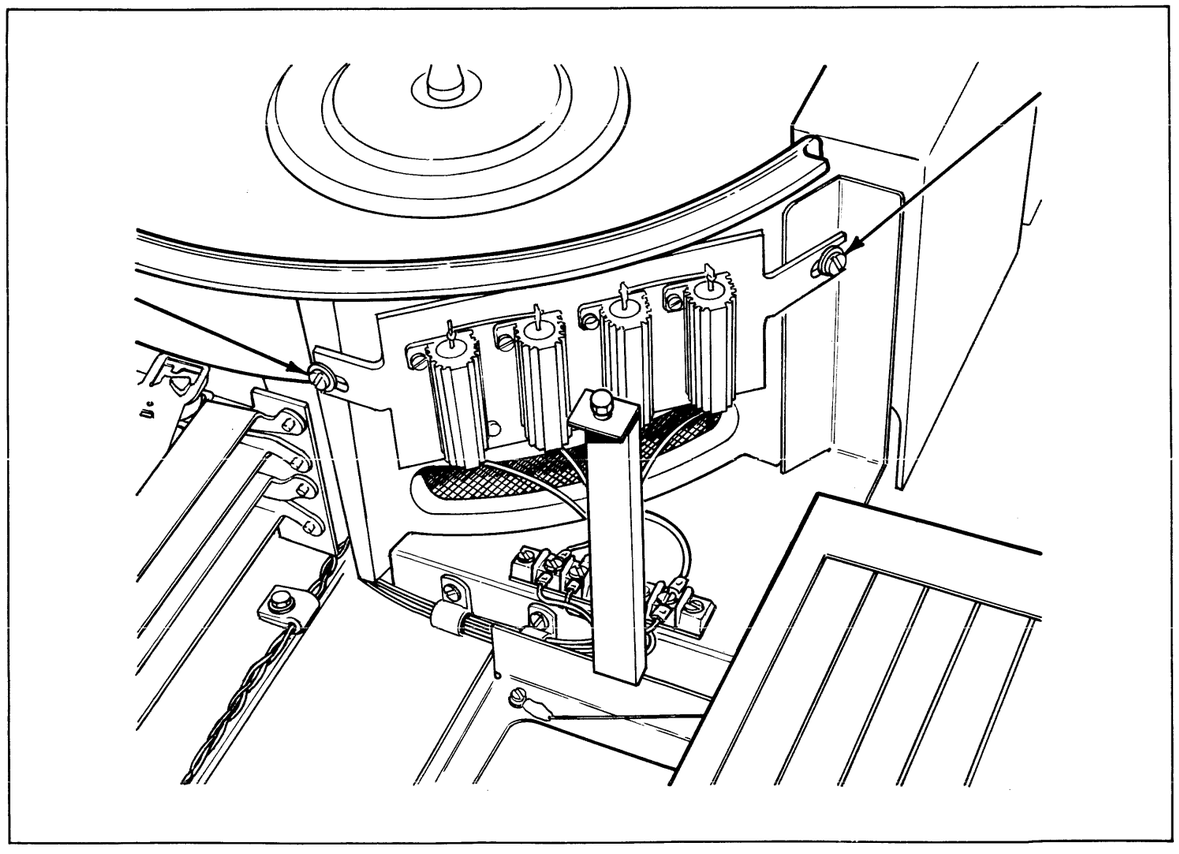


Figure 6-31. Power Resistor Mounting Bracket

6. Remove the two screws which hold the transducer to the transducer arm. Remove the transducer and shims, saving the shims for use with the replacement transducer.

To install the upper index transducer, follow the preceding steps in reverse order. Prior to mating the connector, dress the transducer leads over the front shaft support (see Figure 6-27) and down between the support and the front panel. Perform the upper index transducer adjustments described in 6.6.4.4.

6.7.3.4.2 Lower Index Transducer

1. Remove the lower disk as described in 6.7.3.2.

2. Unplug the lower index transducer connector. This is the lower connector on the panel distributor PCB on the rear of the front panel.

3. The lower index transducer leads pass through a grommet in the bottom of the bowl. Push the grommet up into the bowl, and draw the leads and connector up through the grommet hole in the bowl.

4. Remove the two screws which hold the transducer to the bowl. Remove the transducer and shims, saving the shims for use with the replacement transducer.

To install the lower index transducer, follow the preceding steps in reverse order. Prior to mating the connector, dress the transducer leads over the front shaft support (see Figure 6-27) and down between the support and the front panel. Perform the lower index transducer adjustment described in 6.6.4.2.

6.7.4 Level 3 Removal/Replacement

6.7.4.1 Bowl Assembly

6.7.4.1.1 Removal

1. Remove the lower disk as described in 6.7.3.2.1.

2. Remove the plenum chamber and air filter by removing the two plenum chamber holding screws. Observe the precautions stated in 6.4.2.3.

3. Lower the card cage to the maintenance position as described in 6.4.2.1.

4. The shield is the large panel separating the head positioner from the air filter. Remove the screw which fastens the upper front corner of the shield to the bowl.

5. Spread the cartridge retaining clamps as described in 6.6.2(2).

6. Referring to Figure 6-31, remove the screws which fasten the power resistor mounting bracket assembly to the left rear surface of the bowl.

7. Loosen the set screw which fastens the brush lever to the brush mechanism shaft. See Figure 6-24.

8. Disconnect the brushes retract-switch wires.

9. Unplug both index transducers from the panel distributor PCB on the rear of the front panel. These are the two connectors on the upper right corner of the PCB.

10. Remove the lower index transducer as described in 6.7.3.4.2.

11. Remove the four hexagon recessed screws which fasten the bowl to the baseplate.

12. Lift the bowl straight up and off, manually guiding the brush lever off the brush mechanism shaft.

6.7.4.1.2 Installation

1. Perform the steps listed in 6.7.4.1.1 in reverse. While tightening the four screws which fasten the bowl to the baseplate, twist the bowl in a counter-clockwise direction as far as possible and torque the screws to 120 ± 5 inch-pounds. When placing the brush lever on the brush mechanism shaft, insure that the flat of the shaft is toward the brush lever set screws.

2. Perform the adjustments required by Figure 6-5.

6.7.4.2 Cartridge Retainer Assembly

6.7.4.2.1 Removal

1. Remove the Bowl Assembly as described in 6.7.4.1.

2. There is a spring fastened between the cartridge retaining clamp mechanism and the cartridge retainer safety stop on each side. Disconnect the springs from the cartridge-holding clamp mechanisms.

3. Remove the four screws which fasten each cartridge retaining clamp mechanism to the base plate.

4. Remove the mechanisms, being careful not to bend the end of the bell crank which sits in a notch in the left cartridge-retaining clamp mechanism.

6.7.4.2.2 Installation

1. Perform the steps listed in 6.7.4.2.1(2) through (4) in reverse order, insuring that the bell crank end rests in the notch in the left-hand mechanism.

2. Manually test the interlocking of the cartridge retaining clamps by attempting to spread the clamps with and without holding in the armature of the disk pack safety solenoid.

3. Replace the Bowl Assembly as described in 6.7.4.1.2.

6.7.4.3 Baseplate-Mounted Components

To remove or reinstall the disk pack safety solenoid, interlock linkage, or other components mounted on the top surface of the base-plate, remove the bowl as described in 6.7.4.1 for access to these components.

6.7.4.4 Spindle Assembly

For replacement of the Spindle Assembly on 200 tpi disk drives, consult Diablo Customer Service. The Spindle Assembly on 100 tpi drives is removed as follows:

1. On the underside of the pan, remove the circular fan cover.

2. Remove the 12 screws around the periphery of the static ground strap assembly shown in Figure 6-32. Remove the assembly.

3. Remove the keeper from the spindle shaft end.

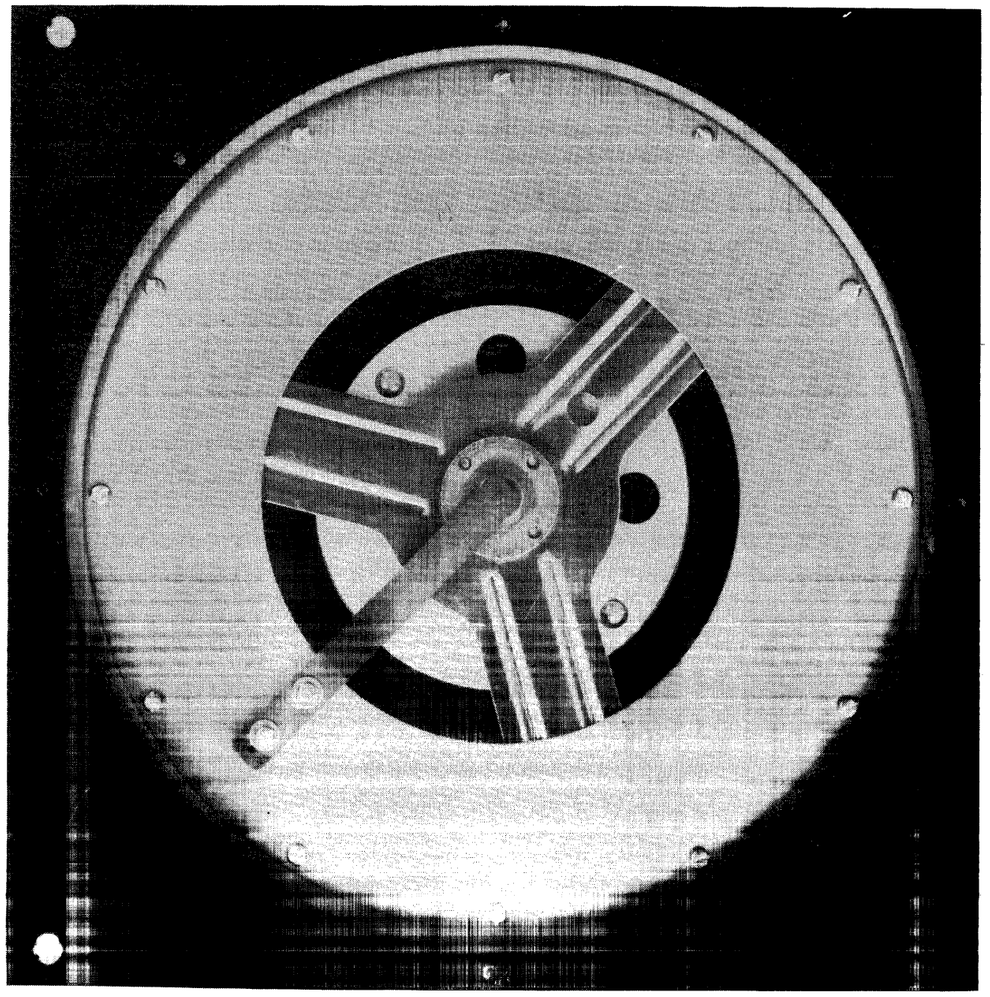


Figure 6-32. Static Ground Strap Assembly

4. Loosen the two set screws on the fan collar, and slide the fan off the spindle shaft.

5. Remove the Bowl Assembly as described in 6.7.4.1.

6. Disconnect the four-conductor cable bundle from the bottom of the power resistor terminal strip. Pull the cable bundle free of the resistor bracket assembly. Tag the wires to facilitate reconnection.

7. Remove the three screws which fasten the spindle to the baseplate, and lift the spindle off.

The Spindle Assembly is installed by reversing the preceding procedures. When installing the spindle, insure that the machined baseplate ridge on which the spindle rests is clean, and that the spindle is firmly seated on the ridge.

6.7.4.5 Head Positioner

6.7.4.5.1 Removal

1. Remove the Bowl Assembly as described in 6.7.4.1.

2. Remove the R/W Heads and head-load springs as described in 6.7.3.1.

3. There is a bracket fastening the linear motor housing to the rear edge of the shield. Detach the shield from the bracket.

4. Unplug the R/W cable harnesses from the data channel box.

5. Remove the three screws which fasten the shield to the baseplate. Move the shield to the right out of the way, being careful not to bend the carriage interlock link passing through the slot in the front end of the shield.

6. Remove the large screw which fastens the carriage interlock link to the carriage interlock lever, as shown in Figure 6-9.

7. Detach the two wires (1 black, 1 white) which come from underneath the Head Positioner and are screwed to the flexible power strap tie point.

   Note color coding of the wires to aid re-assembly.

8. From the underside of the disk drive, remove the head-load-solenoid access cover plate, which is fastened to the bottom of the pan by four screws.

9. Remove the two "C" clips from the head-load linkage and the dashpot linkage as shown in Figure 6-29. Disconnect the linkages.

10. On the PCB at the front of the head-positioner bottom plate there are several connectors, as shown in Figure 6-33. After removing five screws and a clamp bar, disconnect the three connectors labeled "A" in Figure 6-33.

NOTE

Upon re-assembly, insure that a flat washer is placed on both sides of the rear end of the clamp bar and on top side of the front end of the clamp bar. These flat washers are in addition to the two lockwashers. Insure that the clamp bar is reinstalled with the pad down.

11. On 200 tpi drives only, disconnect the two pin-form connectors marked "B" in Figure 6-33.

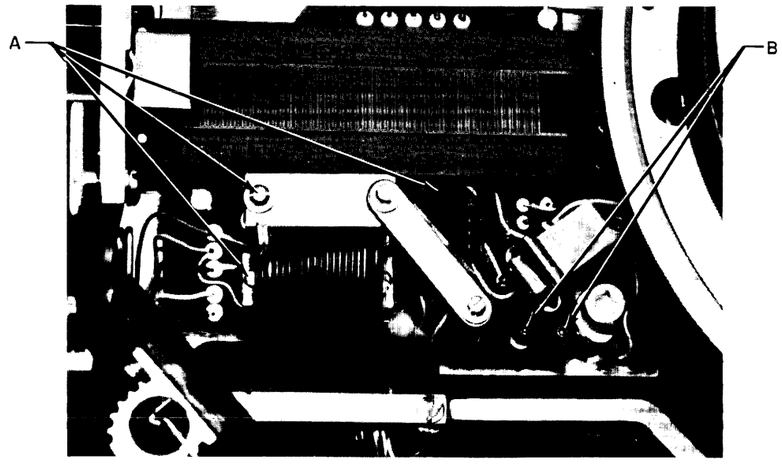


Figure 6-33. Head-Positioner PCB Connections

12. Remove the four hex-head screws which hold the rear end of the linear motor housing to the disk drive baseplate. These screws are inserted from the bottom of the baseplate as shown in Figure 6-34 (screws 10 through 13).

13. Remove the two hex-head screws which fasten the front end of the head-positioner bottom plate to the disk drive baseplate.

14. Lift the rear end of the Head Positioner slightly, slide forward, and lift out.

15. Remove the back expansion plate by removing screws 1 through 9 in Figure 6-34. Save this plate for use with the replacing Head Positioner.

16. Remove the linkage from the dashpot piston, and save for use with the replacing Head Positioner.

6.7.4.5.2 Installation

1. Attach the linkage removed in 6.7.4.5.1(16) to the dashpot.

2. Place gaskets around the back expansion plate.

3. Loosely attach the back expansion plate to the linear motor housing with nine screws.

4. Referring to Figure 6-34, tighten screws 1 through 4 in numerical sequence.

5. Using only a very light torque, snug up screws 5 through 9 in numerical sequence.

6. Install and tighten screws 10 through 13 in numerical sequence.

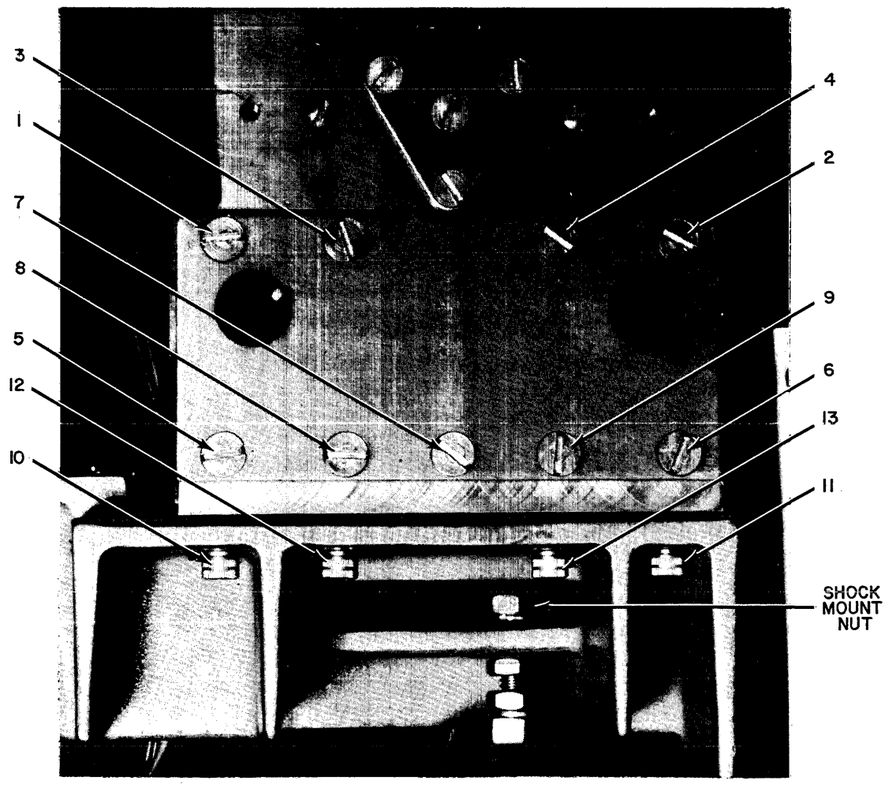


Figure 6-34. Expansion Plate Screws

7. Tighten screws 5 through 9 in numerical sequence.

8. Perform the steps listed in 6.7.4.5.1(8) through (14) in reverse order of numerical sequence.

9. Observing the color coding of the wires, reconnect the wires removed in 6.7.4.5.1(7).

10. Perform the steps listed in 6.7.4.5.1(1) through (6) in reverse order of numerical sequence.

11. Perform the adjustments required by Figure 6-5.

6.7.4.6 Main Harness

Removal and replacement of the main harness is a major task, and should be attempted only by thoroughly trained and experienced personnel. It requires extensive disassembly of the drive, including wiring which is not part of the main harness. Prior to attempting removal of the main harness, the reader should become familiar with 6.7.4.6 in its entirety. During disassembly, wires not part of the main harness should be tagged as they are disconnected. Cable and connector clamps should also be tagged.

6.7.4.6.1 Removal

Removal of the Main Harness is accomplished as follows:

1. Remove the Bowl Assembly as described in 6.7.4.1.

2. Remove all cable clamps, connector clamping bars, and terminal screws which hold wires or cables to the outside of the heat sink.

3. Drop the card cage to the maintenance position as described in 6.4.2.1, and remove the triangular clamping plate from the bottom of the card cage.

4. Unplug all connectors, and disconnect all wires, which connect the card cage or heat sink to the remainder of the drive.

5. There are six wires which come from directly under the resistor bracket assembly, and which are attached to the terminal block on the assembly. These wires have no brown trace in the insulation. Disconnect these six wires from the terminal block.

6. On the head-positioner PCB, unplug the two flat ribbon cable connectors and remove the clamp which holds the cables against the baseplate.

7. On the panel distributor PCB, disconnect the yellow, purple, and black quick-disconnect leads.

NOTE

On disk drives with the desk top interlock option, there is no black quick-disconnected lead.

8. On the brush motor terminal block, disconnect the white and red leads from terminals 1 and 2.

NOTE

On disk drives having the desk top interlock option, also disconnect the black lead from the right-hand side of terminal 3.

9. Remove all cable clamps holding the large wire bundle which runs along the front of the baseplate, back down the left side, and down through the baseplate hole which is beside the head-positioner PCB.

10. Clip the cable ties of the bundle referred to in (9), and separate those wires not entering the baseplate hole beside the head-position PCB.

11. Remove the lid from the data channel box as described in 6.7.2.9.

12. Along the right-hand side of the R/W Amplifier PCB, disconnect the four screw terminal connections, and unplug the flat ribbon cable connector.

13. Remove the plenum chamber and the air filter by removing the two screws holding the plenum chamber in place. Observe the precaution stated in 6.4.2.3.

14. Extend the left slide assembly fully and provide support for the I/O box, so that it will not fall when separated from the slide assembly during the next step.

15. Remove the four screws from the top of the left striker plate. Separate the I/O box and cable support from the slide assembly, but place no load on the flexible cable.

16. Remove the four nuts by which the baseplate is held to the pan shock mounts. Two of these nuts are located on the extreme front corners of the baseplate, one is in the pneumatic chamber under the air filter, and one is in a horizontal slot underneath the rear end of the head positioner, as shown in Figure 6-34.

17. Separate the baseplate from the pan.

18. Disconnect the main harness from the terminal block next to the head-load solenoid.

19. Remove the trapezoidal clamping plate which holds the flat ribbon cable to the spiral base cover.

20. From the top of the baseplate, in the card cage well, remove the eight screws which hold the three-piece cover assembly to the bottom of the baseplate. Remove the cover assembly.

21. Carefully pull the disconnected cables of the main harness down through the holes in the baseplate. Exercise particular caution that the cables from the R/W Amplifier PCB are not damaged as they are pulled past the shield and the Head Positioner.

6.7.4.6.2 Installation

Installation of the Main Harness is accomplished as follows:

1. There is a cable bracket at the end of the cable follower assembly on the main harness, as shown in Figure 6-35. Cables and wire bundles leave this bracket in three directions. Position the bracket on the underside of the baseplate, near the card cage well.

2. Referring to Figure 6-35, pass the cables and wire bundles marked "A" up through the front baseplate hole (beside the head-positioner PCB on the assembled disk drive).

3. Pass the cables and wire bundles marked "B" in the figure up through the hole in the card cage well.

4. Pass the cables and wire bundles marked "C" in the figure up through the small baseplate hole between the shield and the Head Positioner.

5. Loosely attach the cable bracket shown in Figure 6-35 to the underside of the baseplate. This bracket is attached by four screws inserted from the top of the baseplate.

6. Loosely install two more brackets, one on each side of the bracket installed in the preceding step. Screws for these brackets are also inserted from the top of the baseplate.

7. Connect the four wires which go to the screw terminal posts on the R/W Amplifier PCB, and mate the connector.

NOTE

If the PCB and data channel box are not installed at this point, adjust the position of the flat ribbon cable so that its end is 7-1/2 inches above the baseplate.

8. The cable and wires referred to in the preceding step must be clamped to the large spiral cover plate on the bottom of the baseplate. This is accomplished by installing the trapezoidal clamping plate, checking the position of the cable and wires going to the R/W Amplifier PCB, and tightening the clamp. Insure that the black and white wires going to the Head Positioner (but not part of the main harness) are also under the clamping plate.

9. Connect the green and blue wires in the "C" bundle (see Figure 6-35), to terminals 1 and 2, respectively, of the head-load solenoid terminal block.

10. Mount the pan to the baseplate but do not tighten the mounting nuts.

11. Mount the clamps and striker plate to the drawer slide.

12. Tighten the eight screws installed in steps (5) and (6) of this procedure.

13. Placing the pan on a level surface, level the baseplate by adjusting the shock-mount nuts. Tighten the nuts which hold the baseplate to the pan.

14. Perform steps (1) through (13) of 6.7.4.6.1 in reverse. When clamping cables and connectors to PCBs, insure that the clamps with gaskets are positioned with gasket material facing down. When installing the connector clamping bar on the head-position PCB, insure that the right end of the bar has a washer installed between the bar and the connector.

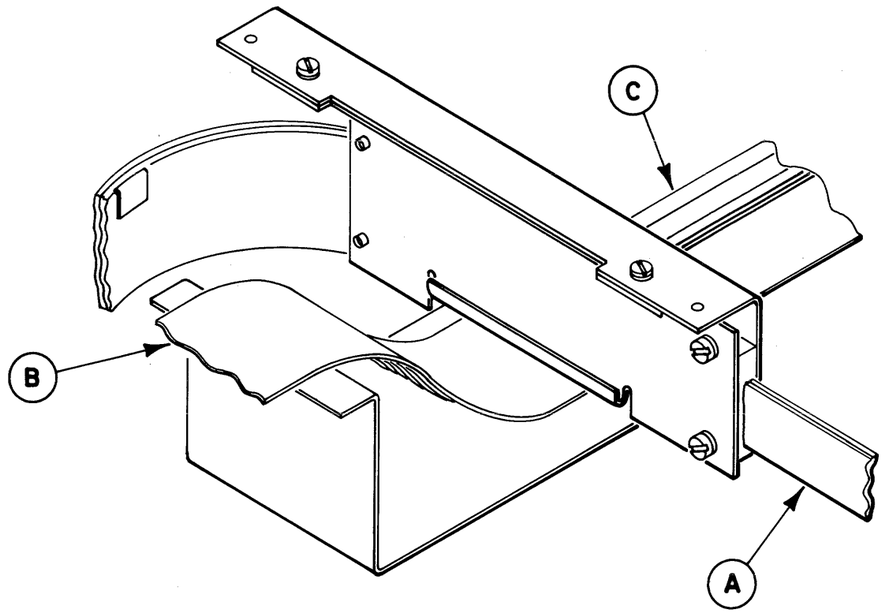


Figure 6-35. Cable Bracket Assembly

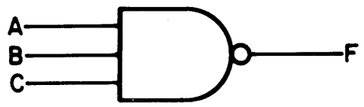
SECTION 7
LOGIC DIAGRAM CONVENTIONS
LOGIC DIAGRAMS

7.1 GENERAL

Diablo Systems logic diagrams are primarily intended for use by field service personnel as troubleshooting aids and by system design engineers as sources of design theory information. As such, the first responsibility of a set of logic diagrams is to illustrate a design's principles of operation. For this reason, Diablo Systems logic diagrams emphasize the functions performed by the logic elements in a design rather than the kinds of devices used to implement the functions.

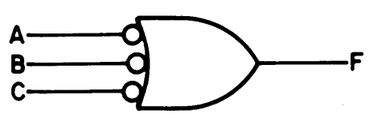
For example, a NAND gate may appear on a Diablo Systems logic diagram as either a positive logic AND function with the output inverted (NAND) or as a negative logic OR function with the inputs inverted (NOR).

AND Function



(Positive Logic NAND)

OR Function



(Negative Logic NOR)

This practice runs contrary to some logic drawing standards, which require the use of the NAND symbol for both functions. But, in Diablo Systems diagrams, different symbols are used to distinguish between the two functions because the functional elements of a design are considered to be more relevant to the design theory than symbolic representation of the kinds of devices used.

This functional approach to logic symbology is basic to the logic documentation conventions employed by Diablo Systems. The conventions that govern logic symbology and signal nomenclature are explained below. Other information concerning drawing standards that may help the reader interpret Diablo Systems logic diagrams is also included.

A	B	C	F
L	L	L	H
H	L	L	H
L	H	L	H
H	H	L	H
L	L	H	H
H	L	H	H
L	H	H	H
H	H	H	L

L = Relative low
H = Relative high

7.2 SIGNAL NOMENCLATURE

The active level of each logic signal is assigned a descriptive name. A signal is considered active when it either causes or represents some logic event that is significant to the progress of an operation. Consequently, the name given a signal usually provides one of two kinds of functional information:

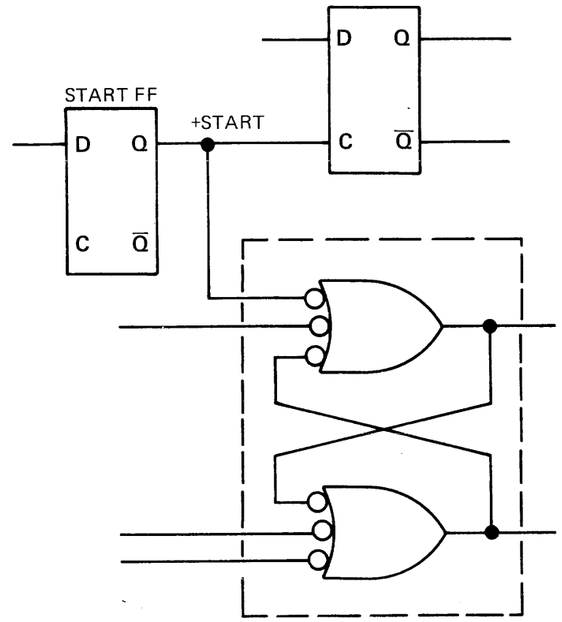
1. Describes the effect that signal's active level has on the logic it feeds; for example, –Load Print Wheel Buffer is the name of the signal that clocks data into the Print Wheel Buffer.

2. Represents a condition or event that develops elsewhere in the logic; for example, –Print Wheel Ready is the name of the signal that is active whenever the print wheel logic is able to accept a new print command.

A + or – sign precedes each signal name to identify which of the two voltage levels used in the logic system is considered to be that signal's active level. The + sign represents the relatively higher logic level and the – sign, the relatively lower level. This means relatively higher or lower with respect to each other; the signs do not indicate signal polarity with respect to ground.

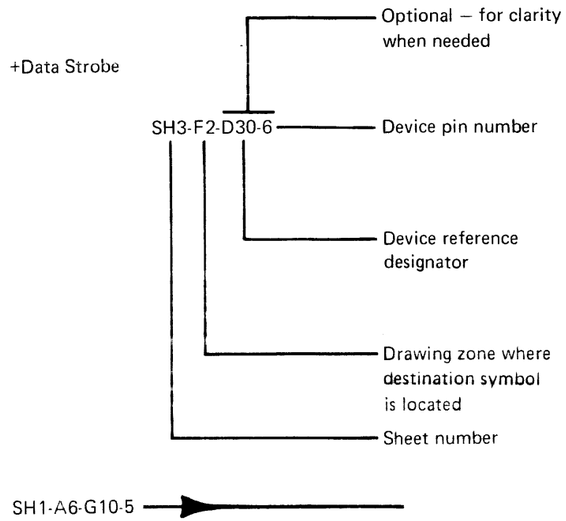
The actual voltage levels represented by the signs will depend on the logic family being used. For example, in TTL circuits, the signal identified by –Print Wheel Ready is active when it is at 0V (nominal) and inactive a +4V (nominal).

Sometimes a signal serves as the input to both positive logic and negative logic elements. Ordinarily in such cases, the sign preceding the signal name agrees with the active level indicated at the output of the logic element that produced the signal. An example of this is illustrated by the following sketch.



7.3 INTERPAGE REFERENCING

When a printed circuit board assembly requires more than one logic diagram page, an interpage reference scheme is used at the points on each diagram page where the signal lines enter and leave the page. The reference scheme includes the following information.



7.4 LOGIC SYMBOLOGY

The logic function symbols used in Diablo Systems logic diagrams conform closely to those set forth in MIL-STD-806.

Most small scale integration (SSI) circuits are represented by function symbols.

Medium scale integration (MSI) devices, such as shift registers and read-only memories, may be represented by rectangles with functional labels.

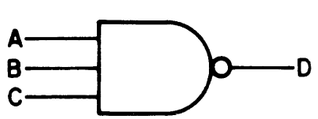
Since positive logic and negative logic conventions can both appear in a single set of logic diagrams, the unfilled circle negation symbol specified by MIL-STD-806 is used to distinguish between low-true and high-true signals.

A circle drawn at an input to a symbol indicates that that input is active at its relatively lower potential. The absence of a circle at an input means that input is logically active at its relatively higher potential. The presence or absence of a circle at a symbol output has similar meanings for the active level of that output.

Usually, all logic symbols are drawn with inputs on the left and outputs on the right. Some device symbols (e.g., one-shots, J-K flip-flops) show some inputs and other external connections on the top and/or bottom of the symbol for clarity. Also, drawing layout restriction occasionally requires that some symbols be drawn with a vertical orientation so that signal flow through them is from top to bottom. However, logic symbols are never drawn with inputs on the right or outputs on theleft of the symbol; nor are they always drawn with inputs and outputs on the same side of the symbol.

The symbols used by Diablo Systems for the basic logic functions are explained below. Manufacturer's information concerning the IC devices represented in this manual's logic diagrams appears at the end of this section.

AND Function (with inversion)/NAND Gate



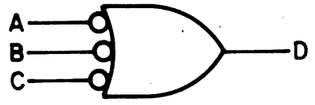
$\overline{D} = A \cdot B \cdot C$

Output is low (active) only if all inputs are high (active)

NOTE

$\overline{D}$ means D is low

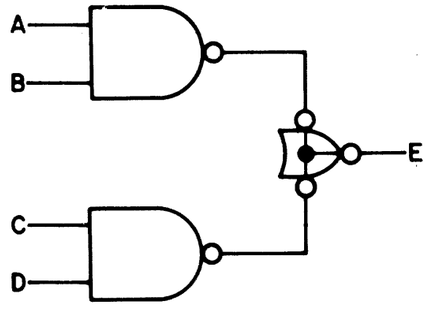
OR Function (with inversion)/NAND Gate



$D = \overline{A} + \overline{B} + \overline{C}$

Output is high (active) if any one or more inputs are low (active)

Collector OR (Dot OR)



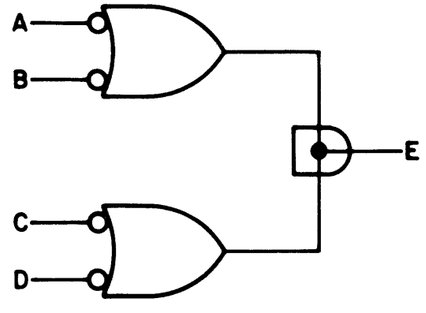
$\overline{E} = A \cdot B + (C \cdot D)$

Output of dot OR is low (active) if both inputs to either (or both) NAND gates are high (active)

NOTE

Negative logic OR function is provided by the solder junction of the two NAND gate outputs and is represented by junction dot. OR symbol represents function provided by junction.

Collector AND (Dot AND)



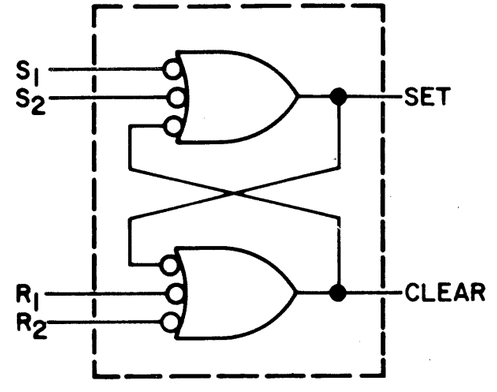
$E = (\overline{A} + \overline{B}) \cdot (\overline{C} + \overline{D})$

Output of dot AND is high (active) only if at least one input to each negative logic NOR gate is low (active)

NOTE

Positive logic AND function is provided by solder junction of the two negative logic NOR gate outputs and is represented by junction dot. AND symbol represents function provided by junction.

R/S Flip-Flop



SET OUT $(\overline{S}_1 + \overline{S}_2)\ (R_1\ R_2)$

CLEAR OUT $(S_1\ S_2)\ (\overline{R}_1 + \overline{R}_2)$

Flip-flop is considered set (SET output is high and CLEAR output is low) when at least one "S" input is low and both "R" inputs are high. Flip-flop is considered reset (SET output is low) when both "S" inputs are high and at least one "R" input is low.

When all inputs are high, flip-flop remains in last state.

A low applied to both an "S" input and an "R" input will make both outputs high. Flip-flop will remain in state of last input removed.

NOTE

This function is provided by cross-coupling the outputs of a pair of negative logic NOR gates. Any low "S" will SET flip-flop (SET high/clear low). Any low "R" will RESET flip-flop (SET low/clear high).

NOTE

Series 40 schematic diagrams are selected to closely match a particular unit, and bound separately. This specialized matching set of diagrams and a maintenance manual accompany each Series 40 when shipped from the factory.

PRODUCT NO. 11265

PRODUCT NO. 11265 DEVELOPMENT REV. D5

PC B ASSY OPTIONS

REFERENCE DESIG.	PRINTED CIRCUIT BOARD	ASSEMBLY & SCHEMATIC
AL1-CB	11403	11404
AL 2-CB	11406	11407
SO-CB	11401	11402
	11401-01	11402
	11401-01	11633
SR-CB (NO SECT COUNTER)	11410	11411
(SECT CNTR)	11410	11411
SL-CB	11408	11409
	11470	11471
TC-CB	11536	11537
OR-CB	11413	11414
SD-CB	11415	11416
	11612	11613
MB	11412	11400-00
	11412-01	11400-20
	11634-00	11635
HS-CB	11417	11418
	11630	11631
RW-CB	11422	11423
	11485	11486
PD-CB	11438	11439
	11498	11499
AW-CB	11434	11435-00
	11434-00	11435-20
IO1-CB	11430	11431
RDR 1-CB (NO SECT COUNTER)	11642	11643
(SECT CNTR)	11642	11643
IO 2-CB	11432	11433
RDR 2-CB	11644	11645
D/CS-CB	11428	11429
	11636	11637
SC-CB	11458	11459
VFO (1500 RPM)	11516	11675
(2400 RPM)	11516	11517
VFC	11518	11519
VFI	11510	11511
VFS	11626	11627
IO-MB	11420	14000-01
	11520	11521

OPTIONAL FEATURES	OPTION CODE
UNSEPARATED DATA	408
POS. GOING ATTN. LINE (SERIES 30 COMPAT.)	447
DEDICATED INTERRUPTS (SERIES 30 COMPAT.)	448
WITH WRITE PROTECT	405
SECTORED FORMAT (2400RPM VFO OPTION)	406-24
SING. SECT. FORMAT (2400RPM VFO OPTION)	407-24
DESK TOP INTERLOCK	417
SECTOR COUNTER	424-XX
STANDARD (2400 RPM)	
UNSEPARATED DATA	408
POS GOING ATTN LINE (SERIES 30 COMPAT.)	447
DEDICATED INTERRUPTS (SERIES 30 COMPAT.)	448
WITH WRITE PROTECT	405
SECTORED FORMAT (1500RPM VFO OPTION)	406-15
SING. SECT. FORMAT (1500RPM VFO OPTION)	407-15
DESK TOP INTERLOCK	417
1500 RPM	415
SECTOR COUNTER	424-XX
STANDARD (2400 RPM)	

100 TPI MODELS: 43 REMOVABLE & FIXED DISK, 41 REMOVABLE DISK ONLY *

200 TPI MODELS: 44 REMOVABLE & FIXED DISK, 42 REMOVABLE DISK ONLY *

NOTES:
1. THE PARTICULAR VERSION OF EACH PCB ASSEMBLY REQUIRED BY A LISTED OPTION OR COMBINATION OF OPTIONS IS TABULATED AT THE CROSS POINT OF THE RELATED ROW AND COLUMN.
2. FOR EACH PCB ASSEMBLY IF NO DASH NUMBER OR CROSS (X) IS SHOWN FOR ANY OPTION OF THE REQUIRED MACHINE CONFIGURATION, USE THE VERSION WHICH IS TABULATED IN THE "STANDARD" COLUMN.
3. THE TABULATION USES CROSS MARKS (X) FOR THOSE PCB ASSEMBLIES WHICH HAVE NO DASH NUMBER VARIATIONS.
4. STRAIGHT HORIZONTAL LINES (—) INDICATE OPTIONAL FEATURES FOR WHICH THE RELATED PCB ASSEMBLY CANNOT BE USED.
5. HORIZONTAL ARROWS (↔) INDICATE THE MOST RECENT SET OF PCB ASSEMBLIES. AS SOON AS THEY ARE AVAILABLE, THE USE OF EARLIER TYPES SHOULD BE DISCONTINUED.
6. * PRODUCTION OF MODELS 41 & 42 DISCONTINUED.

Diablo Systems Incorporated
Hayward California 94545

TITLE: TABULATION CHART PC B ASSY OPTIONS

MODEL 40

PROPRIETARY INFORMATION: UNAUTHORIZED DISCLOSURE OR USE PROHIBITED. SYSTEM LOGIC NO. SL00001

SHEET - TOTAL SHEETS - SIZE D PRODUCT NO. 11265 REV B

REV	E.C.O. NO.	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J								
H								
G								
F								
E								
D								
C								
B	5638	6-26-75						
A	3556							

PRODUCT NO. 11265 — REFERENCE DESIGNATIONS NOT USED — REFERENCE DESIGNATIONS LAST USED

I/O MOTHER BOARD
I/O MB 11521

PI0 I/O RECP SOCKET
P9 I/O PINS SOCKET

FF EE DD CC
BB b T f X J s N m t w y u p F z
B H Y E K P U a e h AA D Z V R L
r HH S x
A C M

4 3 2 1 [4]

ATTENTION LINE
TRACK ADDRESS LINE-BIT 128
TRACK ADDRESS LINE-BIT 64
TRACK ADDRESS LINE-BIT 32
TRACK ADDRESS LINE-BIT 16
TRACK ADDRESS LINE-BIT 8
TRACK ADDRESS LINE-BIT 4
TRACK ADDRESS LINE-BIT 2
TRACK ADDRESS LINE-BIT 1
TRACK ADDRESS LINE-BIT 0
STROBE LINE
RESTORE LINE
LOGICAL ADDRESS INTERLOCK LINE
SEEK INCOMPLETE LINE
ADDRESS ACKNOWLEDGE LINE
READY TO S/R/W LINE

SECTOR ADDRESS BIT 16 LINE
SECTOR ADDRESS BIT 8 LINE
SECTOR ADDRESS BIT 4 LINE
SECTOR ADDRESS BIT 2 LINE
SECTOR ADDRESS BIT 1 LINE
SECTOR MARK LINE
INDEX MARK LINE

WRITE DATA LINE
WRITE PROTECT INPUT LINE
INDEX MARK LINE
READ GATE LINE
ERASE GATE LINE
WRITE PROTECT STATUS LINE
FILE READY LINE
HEAD SELECT LINE
WRITE GATE LINE
WRITE CHECK LINE
DISK SELECT LINE

4 3 2 1 [4] SELECT LINE

+5V [1]

RECEIVER-DRIVER CIRCUIT-2
RDR2-CB-100TPI
SLOT 1/02
11645-XX

BIT 128
BIT 64
BIT 32
BIT 16
BIT 8
BIT 4
BIT 2
BIT 1
BIT 0
LOGICAL ADDRESS INTERLOCK OUTPUT
ADDRESS ACKNOWLEDGE OUTPUT
STROBE
RESTORE
SELECTED
INITIAL RESET
SPINDLE ENABLE
HEADS LOADED
SEEK INCOMPLETE OUTPUT
READY TO S/R/W OUTPUT
WRITE CHECK
FILE READY

[5]
SECTOR COUNTER SC-CB
SLOT 1/03
11459

LOWER INDEX MARK OUTPUT
UPPER SECTOR MARK IN
SECTOR MARK LOWER
SELECTED
READY TO S/R/W
FILE READY OUTPUT
UPPER INDEX PULSE
SELECT DISK
UPPER SECTOR PULSE

RECEIVER-DRIVER CIRCUIT-1 RDR1-CB
*11643-XX
SLOT 1/01

UPPER SECTOR PULSE
SELECT DISK
UPPER INDEX PULSE
WRITE CHECK
SEEK INCOMPLETE OUTPUT
SELECTED INDEX MARK OUTPUT
READY TO S/R/W
FILE READY OUTPUT
WRITE FAULT
VOLTAGE CHECK
INITIAL RESET
SPINDLE ENABLE
FILE READY
HEADS LOADED
WRITE CHECK OUTPUT
DISK SELECT
HEAD SELECT
WRITE GATE
ERASE GATE
WRITE DATA
WRITE PROTECT INPUT
WRITE PROTECT STATUS
WRITE PROTECT STATUS OUTPUT
READ GATE

Z 22

* IF SC-CB(11459) IS NOT USED

SELECTED
DATA/CLOCK GATE

NOT USED

PII POWER CONNECTOR
A D C F L N H K P R J M
-24 V (PWR)
+24 V (PWR)
-24 V (CKT)
+24 V (CKT)
-24 V (R/W)
+24 V (R/W)
GND
+5V

VFC 1/05 [5]
- READ CLOCK LINE
- READ DATA LINE
21 READ DATA AND CLOCK
- SET PHASE
+ IF REF
- IF REF
+ START OSC
- READ CLK
- READ DATA
- LAG ERR
- LEAD ERR
- HI GAIN
+ LAG LT
- OSC START
- RST LAG LT
+ 2F REF
- DATA GT INHIBIT
- 2F REF

VFO 1/06 [5]

C R 1/04 [6]

DATA CLOCK SEPARATION D/C S-CB [5]

NOT USED

+5V
-24V
GND

P5A
14 16 12 13 24 20 26 22 9 32 31 15 18 8 10 30 28 6 11 23 27 29 17 5 19 25 21 7

SHEET 2

P6A
6 14 28 27 2 17 30 31 11 8 25 24 15 18 23 22 21 19 29 13 20 32 34 33 1

SHEET 3

1500 RPM & 2400 RPM 100 TPI

Diablo Systems Incorporated

TITLE: WIRING DIAGRAM 41 & 43 DISK DRIVE

MODEL: 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO. SL00002

SHEET 1 TOTAL SHEETS 3 SIZE D PRODUCT NO. 11670-XX REV D

REV ECO NO	REV ECO NO	REV ECO NO	REV ECO NO	REV ECO NO	REV ECO NO	REV ECO NO	REV ECO NO	REV ECO NO	MFG	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J	H	G	F	E	D4931	C 3563	B 3528	A								

PRODUCT NO 11670-XX

PRODUCT NO 11670-XX | DEVELOPMENT REV. D 2

MOTHER BOARD
MB 11635

ADDRESS LOGIC 1
ALI-CB 100 TPI
11404-00
M09

ADDRESS LOGIC 2
AL2-CB 100TPI
11407-00
M08

SERVO CIRCUIT
SO-CB
11633-00
M07

OSCILLATOR
OR-CB
11414-XX
M02

SPINDLE DRIVE
SD-CB
11613-00
M01

SEQUENCE LOGIC
SL-CB
11471-XX
M05

SENSOR CIRCUITS
SR-CB
11411-XX
M06

+5V
+5V
GND

P5
BIT 128
BIT 64
BIT 32
BIT 16
BIT 8
BIT 4
BIT 2
BIT 1
BIT 0
LOGICAL ADDRESS INTERLOCK OUTPUT
ADDRESS ACKNOWLEDGE OUTPUT
STROBE
RESTORE
SELECTED
INITIAL RESET
READY TO S/R/W
TRACK 256

SHEET 1

CONTROL LEVEL C
CONTROL LEVEL D
SUM BIT 0
SUM BIT 1
SUM BIT 2
SUM BIT 4
SUM BIT 8
SUM BIT 16
SUM BIT 32
SUM BIT 64
SUM BIT 128
COUNTER INTERLOCK
INPUT INHIBIT
DIRECTION CONTROL
RETRACT SPEED
BIT NO. 1
BIT NO. 2
READY TO S/R/W
INITIAL RESET
READY TO S/R/W OUTPUT
FILE READY

PICK A
PICK A
PICK B
PICK B
MINIMUM SPEED
SPEED INCREMENT 1
SPEED INCREMENT 2
SPEED INCREMENT 3
SPEED INCREMENT 4
SPEED INCREMENT 5
SPEED INCREMENT 6
SPEED INCREMENT 7
POSITION TERM
DISK PACK SAFETY

CHANNEL A - 1
CHANNEL A - 2
CHANNEL B - 1
CHANNEL B - 2
DEMOD SIGNAL
60 Hz
INITIAL RESET
PHASE 1
PHASE 2
INDEX MARK LOWER

TRANSDUCER DRIVE A
TRANSDUCER DRIVE B

PHASE 2
PHASE 1
INITIAL RESET
POS SPINDLE DRIVE CUT OFF
NEG SPINDLE DRIVE CUT OFF
SPINDLE DRIVE ON
UNLOCK DRAWER
SPEED OK
H BRUSH HOME

DRAWER UNLOCK PICK
DRAWER UNLOCK ENABLE
SPEED SENSE A
SPEED SENSE B
SPINDLE MOTOR CURRENT CONTROL
SPINDLE MOTOR CURRENT CONTROL
PHASE 1A
PHASE 1B
PHASE 2A
PHASE 2B

SERVO DRIVE SIGNAL
+24V (CKT)
-24V (CKT)
CURRENT DETECTOR
SERVO DISABLE
DISK PACK SAFETY SW

POWER BUSES: +5V, +15V, -15V

SPEED OK
UNLOCK DRAWER
SPINDLE DRIVE ON
INITIAL RESET
60 Hz
HEADS OVER TRACKS
SPINDLE ENABLE
HEADS LOADED
HEADS RETRACTED
VOLTAGE CHECK
SELECTED

H BRUSH HOME
HEAD LOAD ENABLE
HEAD LOAD PICK
BRUSH MOTOR A
BRUSH MOTOR B

SHEET 3

HEADS OVER TRACKS
ZERO TRACK SENSING
VOLTAGE CHECK

INITIAL RESET
SELECTED
RESTORE
STROBE
FILE READY
SEEK INCOMPLETE OUTPUT
LOWER INDEX MARK OUTPUT
UPPER SECTOR MARK IN
SECTOR MARK LOWER
SELECTED INDEX MARK OUTPUT
DISK SELECT

SEEK INCOMPLETE
+24V (CKT)
-24V (CKT)
CURRENT DETECTOR
SERVO DISABLE
POS SPINDLE DRIVE CUT OFF
NEG SPINDLE DRIVE CUT OFF
SELECTED SECTOR MARK
INDEX MARK LOWER
HEADS OVER DISK

DISK PACK SAFETY SWITCH

RETRACT SWITCH B
RETRACT SWITCH A
BRUSH SWITCH A
BRUSH SWITCH B
LOAD/RUN SWITCH B
LOAD/RUN SWITCH A
DISK PACK INTERLOCK SWITCH

UPPER INDEX MARK TRANSDUCER
LOWER INDEX MARK TRANSDUCER
HOME SENSOR "A"
HOME SENSOR "B"
HOME SENSOR LED

1500 RPM & 2400 RPM 100 TPI

Diablo Systems Incorporated

TITLE: WIRING DIAGRAM 41 & 43 DISK DRIVE

MODEL: 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED

SYSTEM LOGIC NO: SL00003

SHEET 2 | TOTAL SHEETS 3 | SIZE D | PRODUCT NO 11670-XX | REV D

PRODUCT NO 11670-XX

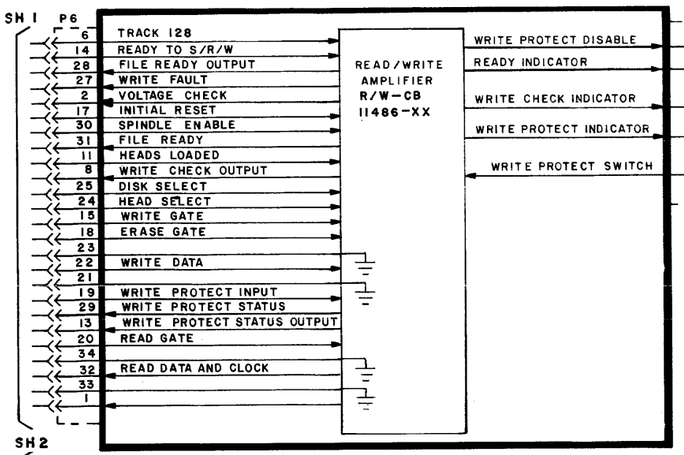
REFERENCE DESIGNATORS NOT USED

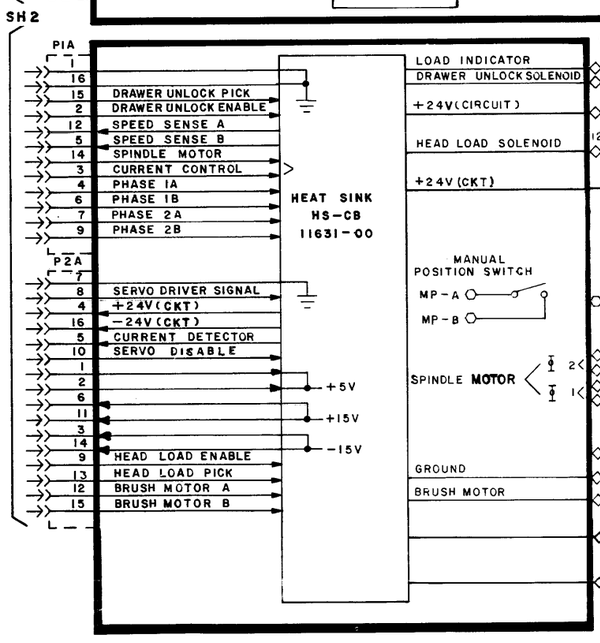
REFERENCE DESIGNATORS LAST USED

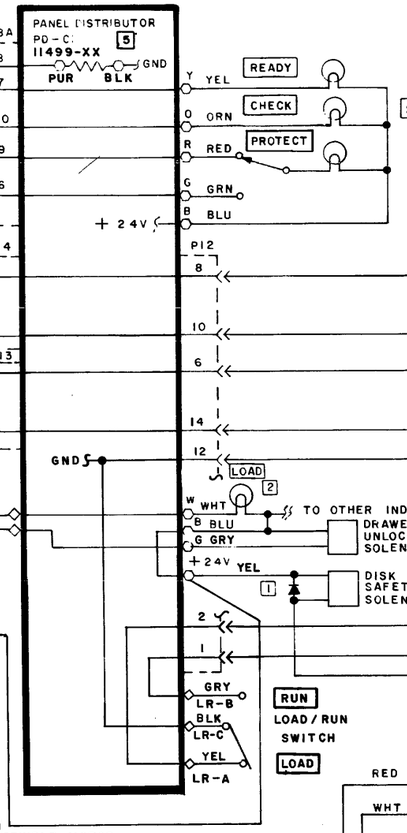
REV J	REV H	REV G	REV F	REV E	REV D 4931	REV C 3563	REV B 3528	REV A	MFG DATE	ENG DATE	CHECKED DATE	DRAWN DATE
REV E.C.O. NO.	REV E.C.O. NO.	REV E.C.O. NO.	REV E.C.O. NO.	REV E.C.O. NO.	REV E.C.O. NO.	REV E.C.O. NO.	REV E.C.O. NO.	REV E.C.O. NO.				

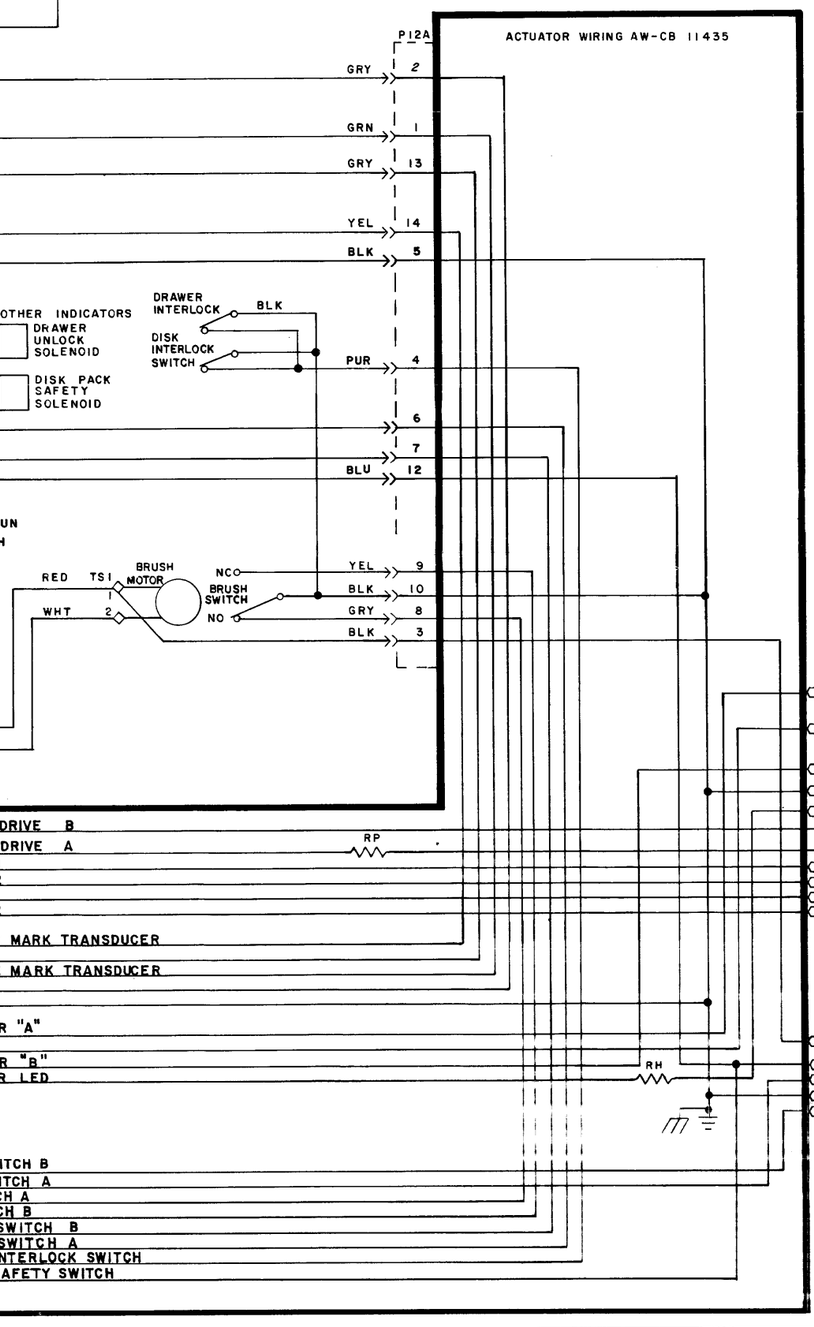
PRODUCT NO. 11670-XX

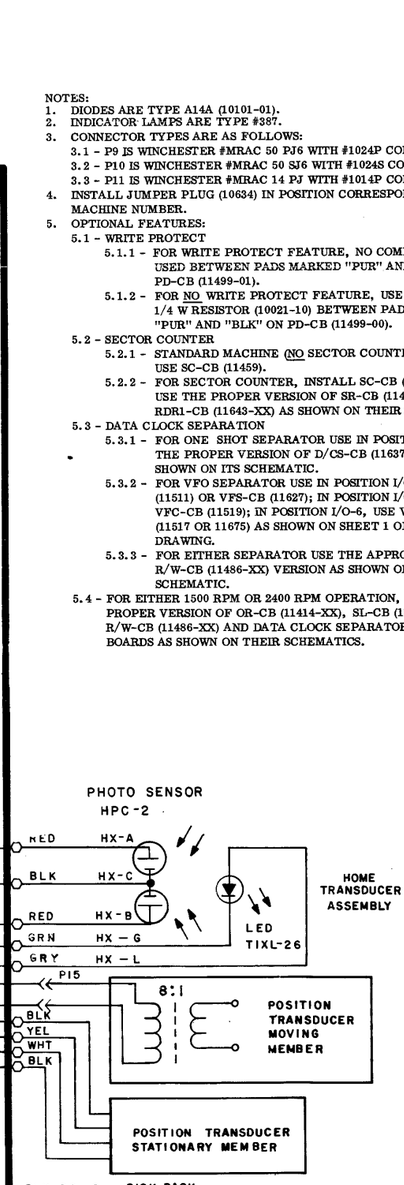
PRODUCT NO 11670-XX | DEVELOPMENT REV. D2











NOTES:
1. DIODES ARE TYPE A14A (10101-01).
2. INDICATOR LAMPS ARE TYPE #387.
3. CONNECTOR TYPES ARE AS FOLLOWS:
   - 3.1 - P9 IS WINCHESTER #MRAC 50 PJ6 WITH #1024P CONTACTS.
   - 3.2 - P10 IS WINCHESTER #MRAC 50 SJ6 WITH #1024S CONTACTS.
   - 3.3 - P11 IS WINCHESTER #MRAC 14 PJ WITH #1014P CONTACTS.
4. INSTALL JUMPER PLUG (10634) IN POSITION CORRESPONDING TO MACHINE NUMBER.
5. OPTIONAL FEATURES:
   - 5.1 - WRITE PROTECT
     - 5.1.1 - FOR WRITE PROTECT FEATURE, NO COMPONENT IS USED BETWEEN PADS MARKED "PUR" AND "BLK" ON PD-CB (11499-01).
     - 5.1.2 - FOR NO WRITE PROTECT FEATURE, USE 10Ω, ± 5%, 1/4 W RESISTOR (10021-10) BETWEEN PADS MARKED "PUR" AND "BLK" ON PD-CB (11499-00).
   - 5.2 - SECTOR COUNTER
     - 5.2.1 - STANDARD MACHINE (NO SECTOR COUNTER) DOES NOT USE SC-CB (11459).
     - 5.2.2 - FOR SECTOR COUNTER, INSTALL SC-CB (11459) AND USE THE PROPER VERSION OF SR-CB (11411-XX) AND RDR1-CB (11643-XX) AS SHOWN ON THEIR SCHEMATICS.
   - 5.3 - DATA CLOCK SEPARATION
     - 5.3.1 - FOR ONE SHOT SEPARATOR USE IN POSITION I/O-5 THE PROPER VERSION OF D/CS-CB (11637-XX) AS SHOWN ON ITS SCHEMATIC.
     - 5.3.2 - FOR VFO SEPARATOR USE IN POSITION I/O-4, VFI-CB (11511) OR VFS-CB (11627); IN POSITION I/O-5 USE VFC-CB (11519); IN POSITION I/O-6, USE VFO-CB (11517 OR 11675) AS SHOWN ON SHEET 1 OF THIS DRAWING.
     - 5.3.3 - FOR EITHER SEPARATOR USE THE APPROPRIATE R/W-CB (11486-XX) VERSION AS SHOWN ON ITS SCHEMATIC.
   - 5.4 - FOR EITHER 1500 RPM OR 2400 RPM OPERATION, USE THE PROPER VERSION OF OR-CB (11414-XX), SL-CB (11471-XX), R/W-CB (11486-XX) AND DATA CLOCK SEPARATOR CIRCUIT BOARDS AS SHOWN ON THEIR SCHEMATICS.

1500 RPM & 2400 RPM 100 TPI

Diablo Systems Incorporated

TITLE: WIRING DIAGRAM 41 & 43 DISK DRIVE

MODEL: 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO. SL00004

SHEET 3 TOTAL SHEETS 3 SIZE D

PRODUCT NO 11670-XX REV D

PRODUCT NO 11670-XX

REFERENCE DESIGNATORS NOT USED

REFERENCE DESIGNATORS LAST USED

REV	ECO NO	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J								
H								
G								
F								
E								
D	4931							
C	3563							
B	3528							
A								

PRODUCT NO 11671-XX

I/O MOTHER BOARD
I/O MB 11521

P10 I/O RECP SOCKET
P9 I/O PINS SOCKET

FF 4
EE 3
DD 2
CC 1
4
ATTENTION LINE → 10

m TRACK ADDRESS LINE-BIT 256 → B
BB TRACK ADDRESS LINE-BIT 128 → 9
b TRACK ADDRESS LINE-BIT 64 → D
T TRACK ADDRESS LINE-BIT 32 → H
f TRACK ADDRESS LINE-BIT 16 → C
X TRACK ADDRESS LINE-BIT 8 → E
J TRACK ADDRESS LINE-BIT 4 → K
s TRACK ADDRESS LINE-BIT 2 → 3
N TRACK ADDRESS LINE-BIT 1 → J
t STROBE LINE → 8
w RESTORE LINE → 7
y LOGICAL ADDRESS INTERLOCK LINE → 5
u SEEK INCOMPLETE LINE → 4
p ADDRESS ACKNOWLEDGE LINE → 2
F READY TO S/R/W LINE → L
z 200 TPI LINE → M

RECEIVER-DRIVER CIRCUIT-2 RDR2-CB 200 TPI 11647-XX SLOT I/O 2

BIT 256 ← 18
BIT 128 ← 19
BIT 64 ← 17
BIT 32 ← W
BIT 16 ← U
BIT 8 ← Y
BIT 4 ← 16
BIT 2 ← 21
BIT 1 ← S
LOGICAL ADDRESS INTERLOCK OUTPUT ← 14
ADDRESS ACKNOWLEDGE OUTPUT ← R
STROBE ← X
RESTORE ← 20
SELECTED ← N
INITIAL RESET ← 12
SPINDLE ENABLE ← 15
HEADS LOADED ← T
SEEK INCOMPLETE OUTPUT ← 11
READY TO S/R/W OUTPUT ← V
WRITE CHECK ← 13
FILE READY ← P

+5V
-24V
GND

P5A
14 16 12 13 24 20 26 22 9 32 31 15 18 8 10 30 28 6 11 23
SHEET 2

5

d
v SECTOR ADDRESS BIT 16 LINE → H
n SECTOR ADDRESS BIT 8 LINE → 2
k SECTOR ADDRESS BIT 4 LINE → 9
j SECTOR ADDRESS BIT 2 LINE → K
c SECTOR ADDRESS BIT 1 LINE → E
W SECTOR MARK LINE → D
INDEX MARK LINE → 5

SECTOR COUNTER SC-CB 11459 SLOT I/O 3

LOWER INDEX MARK OUTPUT ← V
UPPER SECTOR MARK IN ← Y
SECTOR MARK LOWER ← W
SELECTED ← N
READY TO S/R/W ← M
FILE READY OUTPUT ← 21
UPPER INDEX PULSE ← X
SELECT DISK ← 8
UPPER SECTOR PULSE ← J

27 29 17 5 19 25 21 7

B WRITE DATA LINE → K
H WRITE PROTECT INPUT LINE → C
Y INDEX MARK LINE → 5
E READ GATE LINE → 3
K ERASE GATE LINE → D
P WRITE PROTECT STATUS LINE → 16
U FILE READY LINE → 4
a HEAD SELECT LINE → E
e WRITE GATE LINE → 7
h WRITE CHECK LINE → H
AA DISK SELECT LINE → 9
D
Z
V
R
L
4 3 2 1 SELECT LINE → 8
4

RECEIVER DRIVER CIRCUIT-1 RDR 1-CB 11643-XX SLOT I/O 1

UPPER SECTOR PULSE ← J
SELECT DISK ← 8
UPPER INDEX PULSE ← X
WRITE CHECK ← 13
SEEK INCOMPLETE OUTPUT ← M
SELECTED INDEX MARK OUTPUT ← R
READY TO S/R/W ← S
FILE READY OUTPUT ← 21
WRITE FAULT ← 11
VOLTAGE CHECK ← 14
INITIAL RESET ← V
SPINDLE ENABLE ← L
FILE READY ← 12
HEADS LOADED ← T
WRITE CHECK OUTPUT ← 15
DISK SELECT ← P
HEAD SELECT ← 20
WRITE GATE ← U
ERASE GATE ← 17
WRITE DATA ← 19
WRITE PROTECT INPUT ← 2
WRITE PROTECT STATUS ← Y
WRITE PROTECT STATUS OUTPUT ← W
READ GATE ← 18
SELECTED ← N
DATA / CLOCK GATE ← 10

*IF SC-CB (11459) IS NOT USED

+5V
1

r
HH
S
x

A
C
M

P6A
6 14 28 27 2 17 30 31 11 8 25 24 15 18 23 22 21 19 29 13 20
SHEET 3

P11 POWER CONNECTOR
A → −24 V (PWR)
D
C → +24 V (PWR)
F
L → −24 V (CKT)
N → +24 V (CKT)
H → −24 V (R/W)
K → +24 V (R/W)
P → GND
R
J → +5V
M

NOT USED

VFC I/05 5
N 10 e
21 C R 14 Y 9 K 2 8 4 H 12 S 17 15 18 11

− READ CLOCK LINE
− READ DATA LINE
READ DATA AND CLOCK
− SET PHASE
+ IF REF
− IF REF
+ START OSC
− READ CLK
− READ DATA
− LAG ERR
− LEAD ERR
− HI GAIN
+ LAG LT
− OSC START
− RST LAG LT
+ 2F REF
− DATA GT INHIBIT
− 2F REF

VFO I/06 5
2 9 4 9 12 S 17 21 18

C R 14 Y 9 K U I/04 5
7 8 Z 22

DATA CLOCK SEPARATION D/C S-CB 5

NOT USED

32 34 33 1

2400 RPM 200TPI

Diablo Systems Incorporated

TITLE WIRING DIAGRAM 42 & 44 DISK DRIVE
MODEL 40
PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.
SYSTEM LOGIC NO. SL00005
SHEET 1 TOTAL SHEETS 3 SIZE D PRODUCT NO. 11671-XX REV D

REV	E.C.O. NO.	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J			MFG					
H								
G								
F								
E								
D	4931							
C	3563							
B	3528							
A								

PRODUCT NO 11671-XX

MOTHER BOARD
MB 11635

ADDRESS LOGIC 1
ALI-CB 200 TPI
11404-20
M09

ADDRESS LOGIC 2
AL2-CB 200 TPI
11407-20
M08

SERVO CIRCUIT
SO-CB
11633-20
M07

OSCILLATOR
OR-CB
11414-01
M02

SPINDLE DRIVE
SD-CB
11613-00
M01

SEQUENCE LOGIC
SL-CB
11471-01
M05

SENSOR CIRCUITS
SR-CB
11411-XX
M06

TEMP COMPENSATOR
TC-CB 11537
M04

SHEET 1

P5

BIT 256
BIT 128
BIT 64
BIT 32
BIT 16
BIT 8
BIT 4
BIT 2
BIT 1
LOGICAL ADDRESS INTERLOCK OUTPUT
ADDRESS ACKNOWLEDGE OUTPUT
STROBE
RESTORE
SELECTED
INITIAL RESET
READY TO S/R/W
TRACK 256

CONTROL LEVEL C
CONTROL LEVEL D
SUM BIT 1
SUM BIT 2
SUM BIT 4
SUM BIT 8
SUM BIT 16
SUM BIT 32
SUM BIT 64
SUM BIT 128
SUM BIT 256
COUNTER INTERLOCK
INPUT INHIBIT
DIRECTION CONTROL
RETRACT SPEED
BIT NO. 1
BIT NO. 2
READY TO S/R/W
INITIAL RESET
READY TO S/R/W OUTPUT
FILE READY

PICK A
PICK A
PICK B
PICK B
MINIMUM SPEED
SPEED INCREMENT 1
SPEED INCREMENT 2
SPEED INCREMENT 3
SPEED INCREMENT 4
SPEED INCREMENT 5
SPEED INCREMENT 6
SPEED INCREMENT 7
POSITION TERM
DISK PACK SAFETY

CHANNEL A -1
CHANNEL A -2
CHANNEL B -1
CHANNEL B -2
DEMOD SIGNAL
60 Hz
INITIAL RESET
PHASE 1
PHASE 2
INDEX MARK LOWER

TRANSDUCER DRIVE A
TRANSDUCER DRIVE B

PHASE 2
PHASE 1
INITIAL RESET
POS SPINDLE DRIVE CUT OFF
NEG SPINDLE DRIVE CUT OFF
SPINDLE DRIVE ON
UNLOCK DRIVER
SPEED OK

DRAWER UNLOCK PICK
DRAWER UNLOCK ENABLE
SPEED SENSE A
SPEED SENSE B
SPINDLE MOTOR CURRENT CONTROL
SPINDLE MOTOR CURRENT CONTROL
PHASE 1A
PHASE 1B
PHASE 2A
PHASE 2B

SERVO DRIVE SIGNAL

+24 V (CKT)
-24 V (CKT)
CURRENT DETECTOR
SERVO DISABLE

DISK PACK SAFETY SW

SPEED OK
UNLOCK DRIVER
SPINDLE DRIVE ON
INITIAL RESET
60 Hz

HEADS OVER TRACKS
SPINDLE ENABLE
HEADS LOADED
HEADS RETRACTED
VOLTAGE CHECK
SELECTED

HEAD LOAD ENABLE
HEAD LOAD PICK
BRUSH MOTOR A
BRUSH MOTOR B

RETRACT SWITCH B
RETRACT SWITCH A
BRUSH SWITCH A
BRUSH SWITCH B
LOAD/RUN SWITCH B
LOAD/RUN SWITCH A
DISK PACK INTERLOCK SWITCH

HEADS OVER TRACKS
ZERO TRACK SENSING
VOLTAGE CHECK

INITIAL RESET
SELECTED
RESTORE
STROBE
FILE READY
SEEK INCOMPLETE OUTPUT
LOWER INDEX MARK OUTPUT
UPPER SECTOR MARK IN
SECTOR MARK LOWER
SELECTED INDEX MARK OUTPUT
DISK SELECT

SEEK INCOMPLETE
+24 V (CKT)
-24 V (CKT)
CURRENT DETECTOR
SERVO DISABLE
POS SPINDLE DRIVE CUT OFF
NEG SPINDLE DRIVE CUT OFF
SELECTED SECTOR MARK
INDEX MARK LOWER
HEADS OVER DISK

TEMP COMP VOLTAGE
TEMP SENSING "B"
TEMP SENSING "A"
DISK PACK SAFETY SWITCH

UPPER INDEX MARK TRANSDUCER
LOWER INDEX MARK TRANSDUCER
HOME SENSOR "A"
HOME SENSOR "B"
HOME SENSOR LED

GND
P4 (SHIELDED)
P1
P2
P3
P4
POWER BUSES +5V +15V -15V
SHEET 3

2400RPM 200TPI

Diablo Systems Incorporated

TITLE WIRING DIAGRAM
42 & 44 DISK DRIVE

MODEL 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO. SL00006

SHEET 2 | TOTAL SHEETS 3 | SIZE D | PRODUCT NO 11671-XX | REV D

REV	J	H	G	F	E	D	C	B	A
E.C.O. NO.						4931	3563	3528	

MFG DATE ENG DATE CHECKED DATE DRAWN DATE

PRODUCT NO 11671-XX REFERENCE DESIGNATORS REFERENCE DESIGNATORS

PRODUCT NO 11671-XX

PRODUCT NO 11671-XX DEVELOPMENT REV. D2

SH 1

P6

6	TRACK 256
14	READY TO S/R/W
28	FILE READY OUTPUT
27	WRITE FAULT
2	VOLTAGE CHECK
17	INITIAL RESET
30	SPINDLE ENABLE
31	FILE READY
11	HEADS LOADED
8	WRITE CHECK OUTPUT
25	DISK SELECT
24	HEAD SELECT
15	WRITE GATE
18	ERASE GATE
23	
22	WRITE DATA
21	
19	WRITE PROTECT INPUT
29	WRITE PROTECT STATUS
13	WRITE PROTECT STATUS OUTPUT
20	READ GATE
34	
32	READ DATA AND CLOCK
33	
1	

READ/WRITE AMPLIFIER 2400 RPM 200 TPI 11486-XX

WRITE PROTECT DISABLE
READY INDICATOR
WRITE CHECK INDICATOR
WRITE PROTECT INDICATOR
WRITE PROTECT SWITCH

P8 → P8A

PANEL DISTRIBUTOR PD-CB 5

8	8
7	7
10	10
9	9
6	6

GND PUR BLK

Y YEL READY
O ORN CHECK
R RED PROTECT 2
G GRN
B BLU
+24V

P14 LOWER INDEX TRANSDUCER
P13 UPPER INDEX TRANSDUCER

P12

8	GRY
10	GRN
6	GRY
14	YEL
12	BLK

GND 5

LOAD 2

W WHT
B BLU
GRY
+24V YEL

TO OTHER INDICATORS
DRAWER UNLOCK SOLENOID
DISK PACK SAFETY SOLENOID 1

DRAWER INTERLOCK BLK
DISK INTERLOCK SWITCH
PUR

2
1
GRY
LR-B
BLK
LR-C
YEL
LR-A

RUN
LOAD/RUN SWITCH
LOAD

11499-XX

P12A → ACTUATOR WIRING AW-CB 11435

GRY	2
GRN	1
GRY	13
YEL	14
BLK	5
PUR	4
	6
	7
BLU	12
YEL	9
BLK	10
GRY	8
BLK	3

RED TS1 BRUSH MOTOR NC BRUSH SWITCH NO
WHT 2

SH 2

P1A

1	
16	
15	DRAWER UNLOCK PICK
2	DRAWER UNLOCK ENABLE
12	SPEED SENSE A
5	SPEED SENSE B
14	SPINDLE MOTOR
3	CURRENT CONTROL
4	PHASE 1A
6	PHASE 1B
7	PHASE 2A
9	PHASE 2B

HEAT SINK HS-CB 11631-00

P2A

8	SERVO DRIVER SIGNAL
4	+24V(CKT)
16	-24V (CKT)
5	CURRENT DETECTOR
10	SERVO DISABLE
1	
2	+5V
6	
11	+15V
3	
14	-15V
9	HEAD LOAD ENABLE
13	HEAD LOAD PICK
12	BRUSH MOTOR A
15	BRUSH MOTOR B

(P7)

LOAD INDICATOR
DRAWER UNLOCK SOLENOID 10 LOAD 9 SOL PUR BLK
+24V(CIRCUIT) 11 BLU TS3 2
HEAD LOAD SOLENOID 12 GRN 1 HEAD LOAD SOLENOID
+24V (CKT) YEL

MANUAL POSITION SWITCH
MP-A
MP-B

SPINDLE MOTOR 2 1

6 GRY TS2 4Ω 50W 2 4Ω 50W
5 ORN 3 BLU
4 BRN 1 YEL
1 YEL 5 GRN
2 BLU 4 RED
4Ω 50W
4Ω 50W
3 GRN 6

SPINDLE MOTOR

GROUND 8
BRUSH MOTOR 7

PLUS WHT 3
MINUS BLK 4 TS3
SERVO POSITIONER

P4A

9	TRANSDUCER DRIVE A
8	TRANSDUCER DRIVE B
2	CHANNEL A-1
15	CHANNEL A-2
16	CHANNEL B-1
1	CHANNEL B-2
11	HOME SENSOR LED
3	UPPER INDEX MARK TRANSDUCER
14	
4	LOWER INDEX MARK TRANSDUCER
13	
10	
12	HOME SENSOR "A"
5	
7	HOME SENSOR "B"
6	

P3A

6	
9	
11	
12	DISK PACK SAFETY SWITCH
4	RETRACT SWITCH B
14	RETRACT SWITCH A
2	BRUSH SWITCH A
3	BRUSH SWITCH B
7	LOAD/RUN SWITCH B
5	LOAD/RUN SWITCH A
15	DISK PACK INTERLOCK SWITCH
1	TEMP SENSING "B"
16	TEMP SENSING "A"

RP
RH

PHOTO SENSOR HPC-2

RED	HX-A
BLK	HX-C
RED	HX-B
GRN	HX-G
GRY	HX-L

HOME TRANSDUCER ASSEMBLY
LED TIXL-26

P15

BLK
YEL
WHT
BLK

POSITION TRANSDUCER MOVING MEMBER
POSITION TRANSDUCER STATIONARY MEMBER

BLK DS-C
WHT DS-B
GRY RT-A
BLK RT-C
WHT RT-B

DISK PACK SAFETY SWITCH NO NC
RETRACT SWITCH NO

B
t°
A
THERMISTOR

NOTES:
1. DIODES ARE TYPE A14A (10101-01).
2. INDICATOR LAMPS ARE TYPE #387.
3. CONNECTOR TYPES ARE AS FOLLOWS:
   3.1 - P9 IS WINCHESTER #MRAC 50 PJ6 WITH #1024P CONTACTS.
   3.2 - P10 IS WINCHESTER #MRAC 50 SJ6 WITH #1024S CONTACTS.
   3.3 - P11 IS WINCHESTER #MRAC 14 PJ WITH #1014P CONTACTS.
4. INSTALL JUMPER PLUG (10634) IN POSITION CORRESPONDING TO MACHINE NUMBER.
5. OPTIONAL FEATURES:
   5.1 - WRITE PROTECT
      5.1.1 - FOR WRITE PROTECT FEATURE, NO COMPONENT IS USED BETWEEN PADS MARKED "PUR" AND "BLK" ON PD-CB (11499-01).
      5.1.2 - FOR NO WRITE PROTECT FEATURE, USE 10Ω, ± 5%, 1/4W RESISTOR (10021-10) BETWEEN PADS MARKED "PUR" AND "BLK" ON PD-CB (11499-00).
   5.2 - SECTOR COUNTER
      5.2.1 - STANDARD MACHINE (NO SECTOR COUNTER) DOES NOT USE SC-CB (11459).
      5.2.2 - FOR SECTOR COUNTER, INSTALL SC-CB (11459) AND USE THE PROPER VERSION OF SR-CB (11411-XX) AND RDR1-CB (11643-XX) AS SHOWN ON THEIR SCHEMATICS.
   5.3 - DATA CLOCK SEPARATION
      5.3.1 - FOR ONE SHOT SEPARATOR USE IN POSITION I/O-5 THE PROPER VERSION OF D/CS-CB (11637-XX) AS SHOWN ON ITS SCHEMATIC.
      5.3.2 - FOR VFO SEPARATOR USE IN POSITION I/O-4, VFI-CB (11311) OR VFS-CB (11627); IN POSITION I/O-5 USE VFC-CB (11519); IN POSITION I/O-6 USE VFO-CB (11517), AS SHOWN ON SHEET 1 OF THIS DRAWING.
      5.3.3 - FOR EITHER SEPARATOR USE THE APPROPRIATE R/W-CB (11486-XX) VERSION AS SHOWN ON ITS SCHEMATIC.

2400RPM 200TPI

Diablo Systems Incorporated

WIRING DIAGRAM
42 & 44 DISK DRIVE

SIZE 40

SYSTEM LOGIC NO SL00007

SHEET 3 OF 3 SHEETS SIZE D PRODUCT NO 11671-XX REV D

11671-XX

J H G F E D4931 C3563 B3528 A

PRODUCT NO. 11672-XX

PRODUCT NO 11672-XX DEVELOPMENT REV. D2

I/O MOTHER BOARD
I/O MB 11521

+5V
-24V
GND

P10 I/O RECP SOCKET
P9 I/O PINS SOCKET

FF 4
EE 3
DD 2
CC 1
4
ATTENTION LINE

BB TRACK ADDRESS LINE-BIT 128
b TRACK ADDRESS LINE-BIT 64
T TRACK ADDRESS LINE-BIT 32
f TRACK ADDRESS LINE-BIT 16
X TRACK ADDRESS LINE-BIT 8
J TRACK ADDRESS LINE-BIT 4
s TRACK ADDRESS LINE-BIT 2
N TRACK ADDRESS LINE-BIT 1
m TRACK ADDRESS LINE-BIT 0
t STROBE LINE
w RESTORE LINE
y LOGICAL ADDRESS INTERLOCK LINE
u SEEK INCOMPLETE LINE
p ADDRESS ACKNOWLEDGE LINE
F READY TO S/R/W LINE
z

RECEIVER-DRIVER CIRCUIT 2 RDR 2-CB 100 TPI SLOT I/O 2 11645-XX

10 ATTENTION LINE
9 TRACK ADDRESS LINE-BIT 128
D TRACK ADDRESS LINE-BIT 64
H TRACK ADDRESS LINE-BIT 32
C TRACK ADDRESS LINE-BIT 16
E TRACK ADDRESS LINE-BIT 8
K TRACK ADDRESS LINE-BIT 4
3 TRACK ADDRESS LINE-BIT 2
J TRACK ADDRESS LINE-BIT 1
8 TRACK ADDRESS LINE-BIT 0
8 STROBE LINE
7 RESTORE LINE
5 LOGICAL ADDRESS INTERLOCK LINE
4 SEEK INCOMPLETE LINE
2 ADDRESS ACKNOWLEDGE LINE
L READY TO S/R/W LINE

18 BIT 128
19 BIT 64
17 BIT 32
W BIT 16
U BIT 8
Y BIT 4
16 BIT 2
21 BIT 1
S BIT 0
14 LOGICAL ADDRESS INTERLOCK OUTPUT
R ADDRESS ACKNOWLEDGE OUTPUT
X STROBE
20 RESTORE
N SELECTED
12 INITIAL RESET
15 SPINDLE ENABLE
T HEADS LOADED
11 SEEK INCOMPLETE OUTPUT
V READY TO S/R/W OUTPUT
13 WRITE CHECK
P FILE READY

P5A
14 BIT 128
16 BIT 64
12 BIT 32
13 BIT 16
24 BIT 8
20 BIT 4
26 BIT 2
22 BIT 1
9 BIT 0
32 LOGICAL ADDRESS INTERLOCK OUTPUT
31 ADDRESS ACKNOWLEDGE OUTPUT
15 STROBE
18 RESTORE
8 SELECTED
10 INITIAL RESET
30 SPINDLE ENABLE
28 HEADS LOADED
6 SEEK INCOMPLETE OUTPUT
11 READY TO S/R/W OUTPUT
23 WRITE CHECK
SHEET 2

d
v SECTOR ADDRESS BIT 16 LINE
n SECTOR ADDRESS BIT 8 LINE
k SECTOR ADDRESS BIT 4 LINE
j SECTOR ADDRESS BIT 2 LINE
c SECTOR ADDRESS BIT 1 LINE
W SECTOR MARK LINE
INDEX MARK LINE

5
SECTOR COUNTER SC-CB SLOT I/O 3 11459

H SECTOR ADDRESS BIT 16 LINE
2 SECTOR ADDRESS BIT 8 LINE
9 SECTOR ADDRESS BIT 4 LINE
K SECTOR ADDRESS BIT 2 LINE
E SECTOR ADDRESS BIT 1 LINE
D SECTOR MARK LINE
5 INDEX MARK LINE

V LOWER INDEX MARK OUTPUT
Y UPPER SECTOR MARK IN
W SECTOR MARK LOWER
N SELECTED
M READY TO S/R/W
21 FILE READY OUTPUT
X UPPER INDEX PULSE
8 SELECT DISK
J UPPER SECTOR PULSE

27 LOWER INDEX MARK OUTPUT
29 UPPER SECTOR MARK IN
17 SECTOR MARK LOWER
5 SELECTED
19 READY TO S/R/W
25 FILE READY OUTPUT
21 UPPER INDEX PULSE
7 SELECT DISK

B WRITE DATA LINE
H WRITE PROTECT INPUT LINE
Y INDEX MARK LINE
E READ GATE LINE
K ERASE GATE LINE
P WRITE PROTECT STATUS LINE
U FILE READY LINE
a HEAD SELECT LINE
e WRITE GATE LINE
h WRITE CHECK LINE
AA DISK SELECT LINE
D
Z
V
R
L
4
3
2
1
4
SELECT LINE
r
HH
S
x
1
+5V
A
C
M

RECEIVER-DRIVER CIRCUIT 1 RDR 1-CB SLOT 1/01 11643-XX

K WRITE DATA LINE
C WRITE PROTECT INPUT LINE
5 INDEX MARK LINE
3 READ GATE LINE
D ERASE GATE LINE
16 WRITE PROTECT STATUS LINE
4 FILE READY LINE
E HEAD SELECT LINE
7 WRITE GATE LINE
H WRITE CHECK LINE
9 DISK SELECT LINE
B SELECT LINE

J UPPER SECTOR PULSE
8 SELECT DISK
X UPPER INDEX PULSE
13 WRITE CHECK
M SEEK INCOMPLETE OUTPUT
R SELECTED INDEX MARK OUTPUT
S READY TO S/R/W
21 FILE READY OUTPUT
11 WRITE FAULT
14 VOLTAGE CHECK
V INITIAL RESET
L SPINDLE ENABLE
12 FILE READY
T HEADS LOADED
15 WRITE CHECK OUTPUT
P DISK SELECT
20 HEAD SELECT
U WRITE GATE
17 ERASE GATE
Z
22
WRITE DATA
19
2 WRITE PROTECT INPUT
Y WRITE PROTECT STATUS
W WRITE PROTECT STATUS OUTPUT
18 READ GATE

N SELECTED
10 DATA/CLOCK GATE

P6A
6
14
28
27
2
17
30
31
11
8
25
24
15
18
23
22
21
19
29
13
20
SHEET 3

PII POWER CONNECTOR
A -24 V (PWR)
D +24 V (PWR)
C -24 V (CKT)
F +24 V (CKT)
L -24 V (R/W)
N +24 V (R/W)
H GND
K
P +5V
R
J
M

NOT USED

- READ CLOCK LINE
- READ DATA LINE
21 READ DATA AND CLOCK
- SET PHASE
+ IF REF
- IF REF
+ START OSC
- READ CLK
- READ DATA
- LAG ERR
- LEAD ERR
- HI GAIN
+ LAG LT
- OSC START
- RST LAG LT
+ 2F REF
- DATA GT INHIBIT
- 2F REF

VFC I/05 5
N 10 5
C R 14 Y 9 K 2 B 4 H 12 S 17 15 19 11

VFO I/06 5
2 B 4 9 12 S 17 21 18

C R 14 V 9 K U I/04 6 7 8 Z 22

32
34
35

DATA CLOCK SEPARATION D/C S-CB 5

1500 RPM & 2400 RPM 100 TPI

Diablo Systems Incorporated

TITLE WIRING DIAGRAM 41 & 43 DISK DRIVE

MODEL 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED

SYSTEM LOGIC NO SL00008

SHEET 1 TOTAL SHEETS 3 SIZE D PRODUCT NO 11672-XX REV D

REV	J	H	G	F	E	D	C	B	A
ECO NO.						493	3563	3528	
DATE									

MFG DATE | ENG DATE | CHECKED DATE | DRAWN DATE

PRODUCT NO 11672-XX | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED

PRODUCT NO 11672-XX

MOTHER BOARD
MB 11635

+5V
+5V
GND

P5
14 BIT 128
16 BIT 64
12 BIT 32
13 BIT 16
24 BIT 8
20 BIT 4
26 BIT 2
22 BIT 1
9 BIT 0
32 LOGICAL ADDRESS INTERLOCK OUTPUT
31 ADDRESS ACKNOWLEDGE OUTPUT
15 STROBE
18 RESTORE
8 SELECTED
10 INITIAL RESET
READY TO S/R/W
TRACK 256

SHEET 1

30
28
6
11
23
27
29
17
5
19
25
21
7

ADDRESS LOGIC 1
ALI-CB 100 TPI
11404-00
M09

CONTROL LEVEL C
CONTROL LEVEL D
SUM BIT 0
SUM BIT 1
SUM BIT 2
SUM BIT 4
SUM BIT 8
SUM BIT 16
SUM BIT 32
SUM BIT 64
SUM BIT 128
COUNTER INTERLOCK
INPUT INHIBIT
DIRECTION CONTROL
RETRACT SPEED
BIT NO. 1
BIT NO. 2
READY TO S/R/W
INITIAL RESET
READY TO S/R/W OUTPUT
FILE READY

ADDRESS LOGIC 2
AL2-CB 100 TPI
11407-00
M08

PICK A
PICK A
PICK B
PICK B
Σ1
Σ2
Σ3
Σ4
MINIMUM SPEED
SPEED INCREMENT 1
SPEED INCREMENT 2
SPEED INCREMENT 3
SPEED INCREMENT 4
SPEED INCREMENT 5
SPEED INCREMENT 6
SPEED INCREMENT 7
POSITION TERM
DISK PACK SAFETY

SERVO CIRCUIT
SO-CB
11633-00
M07

CHANNEL A-1
CHANNEL A-2
CHANNEL B-1
CHANNEL B-2
DEMOD SIGNAL
60 Hz
INITIAL RESET
PHASE 1
PHASE 2
INDEX MARK LOWER

OSCILLATOR
OR-CB
11414-XX
M02

TRANSDUCER DRIVE A
TRANSDUCER DRIVE B

PHASE 2
PHASE 1
INITIAL RESET
POS SPINDLE DRIVE CUT OFF
NEG SPINDLE DRIVE CUT OFF
SPINDLE DRIVE ON
UNLOCK DRAWER
SPEED OK

SPINDLE DRIVE
SD-CB
11613-01
M01

DISK PACK
BRUSH HOME

DRAWER UNLOCK PICK
DRAWER UNLOCK ENABLE
SPEED SENSE A
SPEED SENSE B
SPINDLE MOTOR CURRENT CONTROL
SPINDLE MOTOR CURRENT CONTROL
PHASE 1A
PHASE 1B
PHASE 2A
PHASE 2B

SERVO DRIVE SIGNAL
+24V (CKT)
-24V (CKT)
CURRENT DETECTOR
SERVO DISABLE
DISK PACK SAFETY SW

SPEED OK
UNLOCK DRAWER
SPINDLE DRIVE ON
INITIAL RESET
60 Hz

BRUSH HOME
SEQUENCE LOGIC
SL-CB
11471-XX
M05

HEADS OVER TRACKS
SPINDLE ENABLE
HEADS LOADED
HEADS RETRACTED
VOLTAGE CHECK
SELECTED

HEAD LOAD ENABLE
HEAD LOAD PICK
BRUSH MOTOR A
BRUSH MOTOR B

RETRACT SWITCH B
RETRACT SWITCH A
BRUSH SWITCH A
BRUSH SWITCH B
LOAD/RUN SWITCH B
LOAD/RUN SWITCH A
DISK PACK INTERLOCK SWITCH

DISK PACK SAFETY SWITCH

SENSOR CIRCUITS
SR-CB
11411-XX
M06

HEADS OVER TRACKS
ZERO TRACK SENSING
VOLTAGE CHECK

SEEK INCOMPLETE
+24V (CKT)
-24V (CKT)
CURRENT DETECTOR
SERVO DISABLE
POS SPINDLE DRIVE CUT OFF
NEG SPINDLE DRIVE CUT OFF
SELECTED SECTOR MARK
INDEX MARK LOWER
HEADS OVER DISK

INITIAL RESET
SELECTED
RESTORE
STROBE
FILE READY
SEEK INCOMPLETE OUTPUT
LOWER INDEX MARK OUTPUT
UPPER SECTOR MARK IN
SECTOR MARK LOWER
SELECTED INDEX MARK OUTPUT
DISK SELECT

UPPER INDEX MARK TRANSDUCER
LOWER INDEX MARK TRANSDUCER
HOME SENSOR "A"
HOME SENSOR "B"
HOME SENSOR LED

GND
P4 (SHIELDED)
P1
P2
P3
P4

POWER BUSES +5V +15V -15V

SHEET 3

1500 RPM & 2400 RPM 100 TPI

Diablo Systems Incorporated

TITLE WIRING DIAGRAM
41 & 43 DISK DRIVE

MODEL 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO. SL00009

SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
2	3	D	11672-XX	D

REV	E.C.O. NO.	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J								
H								
G								
F								
E								
D	4931							
C	3563							
B	3528							
A								

PRODUCT NO 11672-XX | REFERENCE DESIGNATORS | REFERENCE DESIGNATORS

PRODUCT NO 11672-XX

PRODUCT NO 11672-XX DEVELOPMENT REV. D2

SH1

P6

6	TRACK 128
14	READY TO S/R/W
28	FILE READY OUTPUT
27	WRITE FAULT
2	VOLTAGE CHECK
17	INITIAL RESET
30	SPINDLE ENABLE
31	FILE READY
11	HEADS LOADED
8	WRITE CHECK OUTPUT
25	DISK SELECT
24	HEAD SELECT
15	WRITE GATE
18	ERASE GATE
23	
22	WRITE DATA
21	
19	WRITE PROTECT INPUT
29	WRITE PROTECT STATUS
13	WRITE PROTECT STATUS OUTPUT
20	READ GATE
34	
32	READ DATA AND CLOCK
33	
1	

READ/WRITE AMPLIFIER R/W-CB 11486-XX

WRITE PROTECT DISABLE
READY INDICATOR
WRITE CHECK INDICATOR
WRITE PROTECT INDICATOR
WRITE PROTECT SWITCH

P8 — P8A — PANEL DISTRIBUTOR PD-CB 11499-XX [5] — GND — PUR BLK

8	8	Y YEL	READY
7	7	O ORN	CHECK [2]
10	10	R RED	PROTECT
9	9	G GRN	
6	6	B BLU	

+24V

P14 — LOWER INDEX TRANSDUCER

P13 — UPPER INDEX TRANSDUCER

P12

8	GRY	P12A 2
10	GRN	1
6	GRY*	13
14	YEL	14
12	BLK	5

GND

LOAD [2]

W WHT — TO OTHER INDICATORS
B BLU — DRAWER UNLOCK SOLENOID
G GRY
+24V YEL — DISK PACK SAFETY SOLENOID [1]

DRAWER INTERLOCK — BLK
DISK INTERLOCK SWITCH — PUR — 4

2 — 6
1 — 7 — BLU — 12

GRY — LR-B
BLK — LR-C
YEL — LR-A

RUN — LOAD/RUN SWITCH
LOAD

RED — TS1 — BRUSH MOTOR — NC — BRUSH SWITCH — NO — YEL — 9 — BLK — 10
WHT — 2 — GRY — 8
3 — BLK — 3

ACTUATOR WIRING AW-CB 11435

SH2

P1A

1	
16	
15	DRAWER UNLOCK PICK
2	DRAWER UNLOCK ENABLE
12	SPEED SENSE A
5	SPEED SENSE B
14	SPINDLE MOTOR
3	CURRENT CONTROL
4	PHASE 1A
6	PHASE 1B
7	PHASE 2A
9	PHASE 2B

HEAT SINK HS-CB 11631-01

P2A

7	
8	SERVO DRIVER SIGNAL
4	+24V (CKT)
16	−24V (CKT)
5	CURRENT DETECTOR
10	SERVO DISABLE
1	
2	+5V
6	
11	+15V
3	
14	−15V
9	HEAD LOAD ENABLE
13	HEAD LOAD PICK
12	BRUSH MOTOR A
15	BRUSH MOTOR B

LOAD INDICATOR — 10 LOAD — PUR
+24V (CIRCUIT) — 11 BLU — TS3 2
HEAD LOAD SOLENOID — 12 GRN — 1 — HEAD LOAD SOLENOID
+24V (CKT) — YEL
9

MANUAL POSITION SWITCH — MP-A — MP-B

6 GRY — TS2 2 — 4 Ω 50W — 4 Ω 50W

SPINDLE MOTOR — 2 — 1

5	ORN	3	BLU
4	BRN	1	YEL
1	YEL	5	GRN
2	BLU	4	RED

SPINDLE MOTOR

4 Ω 50W — 4 Ω 50W

3 GRN 6

GROUND — 8
BRUSH MOTOR — 7

PLUS WHT 3 — MINUS BLK 4 — TS3 — SERVO POSITIONER

P4A

9	TRANSDUCER DRIVE B
8	TRANSDUCER DRIVE A
2	CHANNEL A-1
15	CHANNEL A-2
16	CHANNEL B-1
1	CHANNEL B-2
3	UPPER INDEX MARK TRANSDUCER
14	
4	LOWER INDEX MARK TRANSDUCER
13	
10	
12	HOME SENSOR "A"
5	
7	
6	HOME SENSOR "B"
11	HOME SENSOR LED

P3A

6	
9	
11	
4	RETRACT SWITCH B
14	RETRACT SWITCH A
2	BRUSH SWITCH A
3	BRUSH SWITCH B
7	LOAD/RUN SWITCH B
5	LOAD/RUN SWITCH A
15	DISK PACK INTERLOCK SWITCH
12	DISK PACK SAFETY SWITCH

RP — RH

PHOTO SENSOR HPC-2

RED	HX-A
BLK	HX-C
RED	HX-B
GRN	HX − G
GRY	HX − L

LED TIXL-26 — HOME TRANSDUCER ASSEMBLY

P15

BLK	
YEL	
WHT	
BLK	

8:1 — POSITION TRANSDUCER MOVING MEMBER

POSITION TRANSDUCER STATIONARY MEMBER

DISK PACK SAFETY SWITCH

BLK DS-C	NO
WHT DS-B	NC
GRY RT-A	RETRACT
BLK RT-C	SWITCH
WHT RT-B	NO

DESK TOP INTERLOCK OPTION
1500 RPM & 2400 RPM 100TPI

NOTES:
1. DIODES ARE TYPE A14A (10101-01).
2. INDICATOR LAMPS ARE TYPE #387.
3. CONNECTOR TYPES ARE AS FOLLOWS:
   - 3.1 - P9 IS WINCHESTER #MRAC 50 PJ6 WITH #1024P CONTACTS.
   - 3.2 - P10 IS WINCHESTER #MRAC 50 SJ6 WITH #1024S CONTACTS.
   - 3.3 - P11 IS WINCHESTER #MRAC 14 PJ WITH #1014P CONTACTS.
4. INSTALL JUMPER PLUG (10634) IN POSITION CORRESPONDING TO MACHINE NUMBER.
5. OPTIONAL FEATURES:
   - 5.1 - WRITE PROTECT
     - 5.1.1 - FOR WRITE PROTECT FEATURE, NO COMPONENT IS USED BETWEEN PADS MARKED "PUR" AND "BLK" ON PD-CB (11499-01).
     - 5.1.2 - FOR NO WRITE PROTECT FEATURE, USE 10Ω, ± 5%, 1/4 W RESISTOR (10021-10) BETWEEN PADS MARKED "PUR" AND "BLK" ON PD-CB (11499-00).
   - 5.2 - SECTOR COUNTER
     - 5.2.1 - STANDARD MACHINE (NO SECTOR COUNTER) DOES NOT USE SC-CB (11459).
     - 5.2.2 - FOR SECTOR COUNTER, INSTALL SC-CB (11459) AND USE THE PROPER VERSION OF SR-CB (11411-XX) AND RDR1-CB (11643-XX) AS SHOWN ON THEIR SCHEMATICS.
   - 5.3 - DATA CLOCK SEPARATION
     - 5.3.1 - FOR ONE SHOT SEPARATOR USE IN POSITION I/O-5 THE PROPER VERSION OF D/CS-CB (11637-XX) AS SHOWN ON ITS SCHEMATIC.
     - 5.3.2 - FOR VFO SEPARATOR USE IN POSITION I/O-4, VFI-CB (11511) OR VFS-CB (11627); IN POSITION I/O-5 USE VFC-CB (11519); iN POSITION I/O-6, USE VFO-CB (11517 OR 11675) AS SHOWN ON SHEET 1 OF THIS DRAWING.
     - 5.3.3 - FOR EITHER SEPARATOR USE THE APPROPRIATE R/W-CB (11486-XX) VERSION AS SHOWN ON ITS SCHEMATIC.
   - 5.4 - FOR EITHER 1500 RPM OR 2400 RPM OPERATION, USE THE PROPER VERSION OF OR-CB (11414-XX), SL-CB (11471-XX), R/W-CB (11486-XX) AND DATA CLOCK SEPARATOR CIRCUIT BOARDS AS SHOWN ON THEIR SCHEMATICS.

Diablo Systems Incorporated

WIRING DIAGRAM
41 & 43 DISK DRIVE

MODEL 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED

SYSTEM LOGIC NO. SL00010

SHEET 3 TOTAL SHEETS 3 SIZE D PRODUCT NO 11672-XX REV D

PRODUCT 11672-XX

REFERENCE DESIGNATORS NEXT USED

REFERENCE DESIGNATORS LAST USED

REV	REV ECO NO	DATE	BY	CHKD
J				
H				
G				
F				
E				
D	4731			
C	3563			
B	3528			
A				

PRODUCT NO 11673-XX DEVELOPMENT REV. D2

I/O MOTHER BOARD
I/O MB 11521

PIO I/O RECP SOCKET

P9 I/O PINS SOCKET

FF 4
EE 3
DD 2
CC 1 — [4] — ATTENTION LINE

m — TRACK ADDRESS LINE-BIT 256
BB — TRACK ADDRESS LINE-BIT 128
b — TRACK ADDRESS LINE-BIT 64
T — TRACK ADDRESS LINE-BIT 32
f — TRACK ADDRESS LINE-BIT 16
X — TRACK ADDRESS LINE-BIT 8
J — TRACK ADDRESS LINE-BIT 4
s — TRACK ADDRESS LINE-BIT 2
N — TRACK ADDRESS LINE-BIT 1
t — STROBE LINE
w — RESTORE LINE
y — LOGICAL ADDRESS INTERLOCK LINE
u — SEEK INCOMPLETE LINE
p — ADDRESS ACKNOWLEDGE LINE
F — READY TO S/R/W LINE
z — 200 TPI LINE

RECEIVER-DRIVER
RDR 2-CB-200TPI
CIRCUIT 2
SLOT I/O 2
11647-XX

10 — ATTENTION LINE
B — TRACK ADDRESS LINE-BIT 256
9 — TRACK ADDRESS LINE-BIT 128
D — TRACK ADDRESS LINE-BIT 64
H — TRACK ADDRESS LINE-BIT 32
C — TRACK ADDRESS LINE-BIT 16
E — TRACK ADDRESS LINE-BIT 8
K — TRACK ADDRESS LINE-BIT 4
3 — TRACK ADDRESS LINE-BIT 2
J — TRACK ADDRESS LINE-BIT 1
8 — STROBE LINE
7 — RESTORE LINE
5 — LOGICAL ADDRESS INTERLOCK LINE
4 — SEEK INCOMPLETE LINE
2 — ADDRESS ACKNOWLEDGE LINE
L — READY TO S/R/W LINE
M — 200 TPI LINE

18 — BIT 256
19 — BIT 128
17 — BIT 64
W — BIT 32
U — BIT 16
Y — BIT 8
16 — BIT 4
21 — BIT 2
S — BIT 1
14 — LOGICAL ADDRESS INTERLOCK OUTPUT
R — ADDRESS ACKNOWLEDGE OUTPUT
X — STROBE
20 — RESTORE
N — SELECTED
12 — INITIAL RESET
15 — SPINDLE ENABLE
T — HEADS LOADED
11 — SEEK INCOMPLETE OUTPUT
V — READY TO S/R/W OUTPUT
13 — WRITE CHECK
P — FILE READY

+5V
-24V
GND

P5A
14 — +5V
16 — -24V
12 — GND
13
24
20
26
22
9
32
31
15
18
8
10
30
28
6
11
23

SHEET 2

[5]

SECTOR COUNTER
SC-CB
SLOT I/O 3
11459

d — SECTOR ADDRESS BIT 16 LINE
v — SECTOR ADDRESS BIT 8 LINE
n — SECTOR ADDRESS BIT 4 LINE
k — SECTOR ADDRESS BIT 2 LINE
j — SECTOR ADDRESS BIT 1 LINE
c — SECTOR MARK LINE
W — INDEX MARK LINE

H — SECTOR ADDRESS BIT 16 LINE
2 — SECTOR ADDRESS BIT 8 LINE
9 — SECTOR ADDRESS BIT 4 LINE
K — SECTOR ADDRESS BIT 2 LINE
E — SECTOR ADDRESS BIT 1 LINE
D — SECTOR MARK LINE
5 — INDEX MARK LINE

V — LOWER INDEX MARK OUTPUT
Y — UPPER SECTOR MARK IN
W — SECTOR MARK LOWER
N — SELECTED
M — READY TO S/R/W
21 — FILE READY OUTPUT
X — UPPER INDEX PULSE
8 — SELECT DISK
J — UPPER SECTOR PULSE

27
29
17
5
19
25
21
7

RECEIVER DRIVER
CIRCUIT 1
RDRI-CB
SLOT 1/01
11643-XX

B — WRITE DATA LINE
H — WRITE PROTECT INPUT LINE
Y — INDEX MARK LINE
E — READ GATE LINE
K — ERASE GATE LINE
P — WRITE PROTECT STATUS LINE
U — FILE READY LINE
a — HEAD SELECT LINE
e — WRITE GATE LINE
h — WRITE CHECK LINE
AA — DISK SELECT LINE
D
Z — SELECT LINE — [4]
V
R
L
r — +5V — [1]
HH
S
x
A
C
M

K — UPPER SECTOR PULSE
C — SELECT DISK
5 — UPPER INDEX PULSE
3 — WRITE CHECK
D — SEEK INCOMPLETE OUTPUT
16 — SELECTED INDEX MARK OUTPUT
4 — READY TO S/R/W
E — FILE READY OUTPUT
7 — WRITE FAULT
H — VOLTAGE CHECK
9 — INITIAL RESET
B — SPINDLE ENABLE
FILE READY
HEADS LOADED
WRITE CHECK OUTPUT
DISK SELECT
HEAD SELECT
WRITE GATE
ERASE GATE
Z — 22 — WRITE DATA
2 — WRITE PROTECT INPUT
Y — WRITE PROTECT STATUS
W — WRITE PROTECT STATUS OUTPUT
18 — READ GATE
N — SELECTED
10 — DATA / CLOCK GATE

J — UPPER SECTOR PULSE
8 — SELECT DISK
X — UPPER INDEX PULSE
13 — WRITE CHECK
M — SEEK INCOMPLETE OUTPUT
R — SELECTED INDEX MARK OUTPUT
S — READY TO S/R/W
21 — FILE READY OUTPUT
11 — WRITE FAULT
14 — VOLTAGE CHECK
V — INITIAL RESET
L — SPINDLE ENABLE
12 — FILE READY
T — HEADS LOADED
15 — WRITE CHECK OUTPUT
P — DISK SELECT
20 — HEAD SELECT
U — WRITE GATE
17 — ERASE GATE
19 — WRITE DATA
2 — WRITE PROTECT INPUT
Y — WRITE PROTECT STATUS
W — WRITE PROTECT STATUS OUTPUT
18 — READ GATE
N — SELECTED
10 — DATA / CLOCK GATE

P6A
6
14
28
27
2
17
30
31
11
8
25
24
15
18
23
22
21
19
29
13
20

SHEET 3

PII POWER CONNECTOR
A — -24 V (PWR)
D
C — +24 V (PWR)
F
L — -24 V (CKT)
N — +24 V (CKT)
H — -24 V (R/W)
K — +24 V (R/W)
P — GND
R
J — +5V
M

NOT USED

- READ CLOCK LINE
- READ DATA LINE
21 READ DATA AND CLOCK
- SET PHASE
+ IF REF
- IF REF
+ START OSC
- READ CLK
- READ DATA
- LAG ERR
- LEAD ERR
- HI GAIN
+ LAG LT
- OSC START
- RST LAG LT
+ 2F REF
- DATA GT INHIBIT
- 2F REF

VFC 1/05 [5]
VFO 1/06 [5]
C R 14 Y 9 K U 1/04 7 8 Z 22 [5]

DATA CLOCK SEPARATION D/C S-CB [5]

NOT USED

32
34
33
1

DESK TOP INTERLOCK OPTION
2400 RPM 200TPI

Diablo Systems Incorporated

TITLE: WIRING DIAGRAM 42 & 44 DISK DRIVE
MODEL: 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED
SYSTEM LOGIC NO. SL00011
SHEET 1 TOTAL SHEETS 3 SIZE D PRODUCT NO. 11673-XX REV D

PRODUCT NO 11673-XX
REFERENCE DESIGNATORS NOT USED
REFERENCE DESIGNATORS LAST USED

REV	E.C.O. NO.	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J								
H								
G								
F								
E								
D	4931							
C	3563							
B	3528							
A								

PRODUCT NO. 11673-XX

MOTHER BOARD
MB 11635

+5V
+5V
GND

P5

SHEET 1

BIT 256 — 14
BIT 128 — 16
BIT 64 — 12
BIT 32 — 13
BIT 16 — 24
BIT 8 — 20
BIT 4 — 26
BIT 2 — 22
BIT 1 — 9
LOGICAL ADDRESS INTERLOCK OUTPUT — 32
ADDRESS ACKNOWLEDGE OUTPUT — 31
STROBE — 15
RESTORE — 18
SELECTED — 8
INITIAL RESET — 10
READY TO S/R/W
TRACK 256

30
28
6
11
23
27
29
17
5
19
25
21
7

ADDRESS LOGIC 1
ALI-CB 200 TPI
11404-20
M09

L M 10 11 14 13 R P K 16 T 12 N 7 8 H 9

Y 21 V X Z 20 19 2 3 C B J D E 4 5 U S A 17 18

CONTROL LEVEL C
CONTROL LEVEL D
SUM BIT 1
SUM BIT 2
SUM BIT 4
SUM BIT 8
SUM BIT 16
SUM BIT 32
SUM BIT 64
SUM BIT 128
SUM BIT 256
COUNTER INTERLOCK
INPUT INHIBIT
LIRECTION CONTROL
RETRACT SPEED
BIT NO. 1
BIT NO. 2
READY TO S/R/W
INITIAL RESET
READY TO S/R/W OUTPUT
FILE READY

ADDRESS LOGIC 2
AL2-CB 200 TPI
11407-20
M08

14 X Z 17 U 2 3 C B A D E 4 5 R H 10 L P

Y 21 18 15 V S W 19 T 16 11 J 9 M 12 8 K 20 N 7 13

PICK A
PICK Ā
PICK B
PICK B̄
SUM 1
SUM 2
SUM 3
SUM 4
MINIMUM SPEED
SPEED INCREMENT 1
SPEED INCREMENT 2
SPEED INCREMENT 3
SPEED INCREMENT 4
SPEED INCREMENT 5
SPEED INCREMENT 6
SPEED INCREMENT 7
POSITION TERM
DISK PACK SAFETY

SERVO CIRCUIT
SO-CB
11633-20
M07

Y 21 — 18 15 V S W 19 T 16 11 J 9 M 12 8 K 20 N 17 — R 14 B 2 — H

Z
X

CHANNEL A-1
CHANNEL A-2
CHANNEL B-1
CHANNEL B-2
DEMOD SIGNAL
60 Hz
INITIAL RESET
PHASE 1
PHASE 2
INDEX MARK LOWER

OSCILLATOR
OR-CB
11414-01
M02

H B K 15 16 U — T S

TRANSDUCER DRIVE A
TRANSDUCER DRIVE B

PHASE 2
PHASE 1
INITIAL RESET

SPINDLE DRIVE
SD-CB
11613-01
M01

16 15 K — U V S B R D — Y DISK PACK H BRUSH HOME — 5 2 E 12 C 3 4 7 J 9 — X

DRAWER UNLOCK PICK
DRAWER UNLOCK ENABLE
SPEED SENSE A
SPEED SENSE B
SPINDLE MOTOR CURRENT CONTROL
SPINDLE MOTOR CURRENT CONTROL
PHASE 1A
PHASE 1B
PHASE 2A
PHASE 2B

POS SPINDLE DRIVE CUT OFF
NEG SPINDLE DRIVE CUT OFF
SPINDLE DRIVE ON
UNLOCK DRAWER
SPEED OK

SERVO DRIVE SIGNAL
+24V(CKT)
-24V(CKT)
CURRENT DETECTOR
SERVO DISABLE
DISK PACK SAFETY SW

POWER BUSES: +5V, +15V, -15V

SPEED OK
UNLOCK DRAWER
SPINDLE DRIVE ON
INITIAL RESET
60 Hz

SEQUENCE LOGIC
SL-CB
11471-01
M05

H BRUSH HOME 14 C S 9 2 — 17 J R B N 7 — 11 T 3 — W V 18 19 21 20 U

HEADS OVER TRACKS
SPINDLE ENABLE
HEADS LOADED
HEADS RETRACTED
VOLTAGE CHECK
SELECTED

HEAD LOAD ENABLE
HEAD LOAD PICK
BRUSH MOTOR A
BRUSH MOTOR B

RETRACT SWITCH B
RETRACT SWITCH A
BRUSH SWITCH A
BRUSH SWITCH B
LOAD/RUN SWITCH B
LOAD/RUN SWITCH A
DISK PACK INTERLOCK SWITCH

SENSOR CIRCUITS
SR-CB
11411-XX
M06

HEADS OVER TRACKS — 17 U
ZERO TRACK SENSING
VOLTAGE CHECK — B

INITIAL RESET — 9
SELECTED — 7
RESTORE — N
STROBE — K
FILE READY — J
SEEK INCOMPLETE OUTPUT — C
LOWER INDEX MARK OUTPUT — E
UPPER SECTOR MARK IN — D
SECTOR MARK LOWER — M
SELECTED INDEX MARK OUTPUT — 11
DISK SELECT — S

SEEK INCOMPLETE — 14
+24V(CKT) — 16
-24V(CKT) — 8
CURRENT DETECTOR — R
SERVO DISABLE — 15
POS SPINDLE DRIVE CUT OFF — 4
NEG SPINDLE DRIVE CUT OFF — 5
SELECTED SECTOR MARK — 12
INDEX MARK LOWER — T
HEADS OVER DISK — 3

18 V — UPPER INDEX MARK TRANSDUCER
19 W — LOWER INDEX MARK TRANSDUCER
22
Y
21
20 X

HOME SENSOR "A"
HOME SENSOR "B"
HOME SENSOR LED

TEMP COMP VOLTAGE

TEMP COMPENSATOR
T TC-CB 11537
M04

7 17

TEMP SENSING "B"
TEMP SENSING "A"

DISK PACK SAFETY SWITCH

GND

P4 (SHIELDED)
2 15 16 1 — 8 9

P1
1 16 — 15 2 12 5 14 3 4 6 7 9

P2
7 8 — 4 16 5 10 — 1 2 6 11 3 14

P3
6 9 11 — 4 14 2 3 7 5 15 — 1 16 12

P4
3 14 4 — 13 10 12 5 7 6 11

SHEET 3

DESK TOP INTERLOCK OPTION
2400 RPM 200 TPI

Diablo Systems Incorporated
Hayward California 94545

TITLE: WIRING DIAGRAM 42 & 44 DISK DRIVE

MODEL: 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO. SL00012

SHEET 2 | TOTAL SHEETS 3 | SIZE D | PRODUCT NO. 11673-XX | REV D

PRODUCT NO 11673-XX

REFERENCE DESIGNATORS NOT USED

REFERENCE DESIGNATORS LAST USED

REV	E.C.O. NO.	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J								
H								
G								
F								
E								
D	4931							
C	3563							
B	3528							
A								

PRODUCT NO 11673-XX

PRODUCT NO. 11673-XX DEVELOPMENT REV. D2

SH1 P6

READ/WRITE AMPLIFIER R/W-CB 2400 RPM 200TPI 11486-XX

6	TRACK 256
14	READY TO S/R/W
28	FILE READY OUTPUT
27	WRITE FAULT
2	VOLTAGE CHECK
17	INITIAL RESET
30	SPINDLE ENABLE
31	FILE READY
11	HEADS LOADED
8	WRITE CHECK OUTPUT
25	DISK SELECT
24	HEAD SELECT
15	WRITE GATE
18	ERASE GATE
23	
22	WRITE DATA
21	
19	WRITE PROTECT INPUT
29	WRITE PROTECT STATUS
13	WRITE PROTECT STATUS OUTPUT
20	READ GATE
34	
32	READ DATA AND CLOCK
33	
1	

WRITE PROTECT DISABLE — P8 8 — P8A 8
READY INDICATOR — P8 7 — P8A 7
WRITE CHECK INDICATOR — P8 10 — P8A 10
WRITE PROTECT INDICATOR — P8 9 — P8A 9
WRITE PROTECT SWITCH — P8 6 — P8A 6

PANEL DISTRIBUTOR PD-CB [5]

PUR — BLK — GND

Y YEL — READY
O ORN — CHECK
R RED — PROTECT
G GRN
B BLU
+24V

[2]

P14 — LOWER INDEX TRANSDUCER
P13 — UPPER INDEX TRANSDUCER

P12

8	GRY
10	GRN
6	GRY
14	YEL
12	BLK

GND

[5] LOAD [2]

W WHT — TO OTHER INDICATORS
B BLU — DRAWER UNLOCK SOLENOID
P PUR — DISK PACK SAFETY SOLENOID
+24V YEL [1]

DRAWER INTERLOCK — BLK
DISK INTERLOCK SWITCH — PUR

2 [5]
1
GRY — LR-B
BLK — LR-C
YEL — LR-A

RUN — LOAD/RUN SWITCH
LOAD

11499-XX

RED — TS1 — BRUSH MOTOR
WHT — 2
BLK — 3

BRUSH SWITCH: NC, NO

YEL	9
BLK	10
GRY	8
BLK	3

ACTUATOR WIRING AW-CB 11435

P12A

GRY	2
GRN	1
GRY	13
YEL	14
BLK	5
PUR	4
	6
	7
BLU	12

SH1 P1A

HEAT SINK HS-CB 11631-01

1	
16	
15	DRAWER UNLOCK PICK
2	DRAWER UNLOCK ENABLE
12	SPEED SENSE A
5	SPEED SENSE B
14	SPINDLE MOTOR
3	CURRENT CONTROL
4	PHASE 1A
6	PHASE 1B
7	PHASE 2A
9	PHASE 2B

P2A

7	
8	SERVO DRIVER SIGNAL
4	+24V(CKT)
16	-24V (CKT)
5	CURRENT DETECTOR
10	SERVO DISABLE
1	
2	+5V
6	
11	+15V
3	
14	-15V
9	HEAD LOAD ENABLE
13	HEAD LOAD PICK
12	BRUSH MOTOR A
15	BRUSH MOTOR B

LOAD INDICATOR — (P7) 10 LOAD — PUR
DRAWER UNLOCK SOLENOID — 9
+24V(CIRCUIT) — 11 BLU — TS3 2
HEAD LOAD SOLENOID — 12 GRN — 1 — HEAD LOAD SOLENOID
+24V(CKT) — YEL

MANUAL POSITION SWITCH
MP-A
MP-B

SPINDLE MOTOR — 2 / 1

5	ORN	3	BLU
4	BRN	1	YEL
YEL		5	GRN
2	BLU	4	RED

SPINDLE MOTOR

6 GRY — TS2 — 4Ω 50W — 2 — 4Ω 50W
4Ω 50W — 4Ω 50W
3 GRN — 6

GROUND — 8
BRUSH MOTOR — 7

PLUS WHT — 3
MINUS BLK — 4 — TS3

SERVO POSITIONER

SH2 P4A

5	TRANSDUCER DRIVE B
8	TRANSDUCER DRIVE A
2	CHANNEL A-1
15	CHANNEL A-2
16	CHANNEL B-1
1	CHANNEL B-2
11	HOME SENSOR LED
3	UPPER INDEX
14	LOWER INDEX MARK TRANSDUCER
13	
10	
12	HOME SENSOR "A"
5	
7	
6	HOME SENSOR "B"

P3A

6	
9	
11	
12	DISK PACK SAFETY SWITCH
4	RETRACK SWITCH B
14	RETRACK SWITCH A
2	BRUSH SWITCH A
3	BRUSH SWITCH B
7	LOAD/RUN SWITCH B
5	LOAD/RUN SWITCH A
13	DISK PACK INTERLOCK SWITCH
1	TEMP SENSING "B"
16	TEMP SENSING "A"

RP — RH

PHOTO SENSOR HPC-2

RED	HX-A
BLK	HX-C
RED	HX-B
GRN	HX-G
GRY	HX-L

LED TIXL-26

HOME TRANSDUCER ASSEMBLY

P15

BLK	
YEL	
WHT	
BLK	

8:1 — POSITION TRANSDUCER MOVING MEMBER

POSITION TRANSDUCER STATIONARY MEMBER

BLK DS-C	DISK PACK SAFETY SWITCH NO
WHT DS-B	NC
GRY RT-A	RETRACT SWITCH NO
BLK RT-C	
WHT RT-B	

B — t° — A — THERMISTOR

NOTES:
1. DIODES ARE TYPE A14A (10101-01).
2. INDICATOR LAMPS ARE TYPE #387.
3. CONNECTOR TYPES ARE AS FOLLOWS:
   3.1 - P9 IS WINCHESTER #MRAC 50 PJ6 WITH #1024P CONTACTS.
   3.2 - P10 IS WINCHESTER #MRAC 50 SJ6 WITH #1024S CONTACTS.
   3.3 - P11 IS WINCHESTER #MRAC 14 PJ WITH #1014P CONTACTS.
4. INSTALL JUMPER PLUG (10634) IN POSITION CORRESPONDING TO MACHINE NUMBER.
5. OPTIONAL FEATURES:
   5.1 - WRITE PROTECT
      5.1.1 - FOR WRITE PROTECT FEATURE, NO COMPONENT IS USED BETWEEN PADS MARKED "PUR" AND "BLK" ON PD-CB (11499-01).
      5.1.2 - FOR NO WRITE PROTECT FEATURE, USE 10Ω, ± 5%, 1/4W RESISTOR (10021-10) BETWEEN PADS MARKED "PUR" AND "BLK" ON PD-CB (11499-00).
   5.2 - SECTOR COUNTER
      5.2.1 - STANDARD MACHINE (NO SECTOR COUNTER) DOES NOT USE SC-CB (11459).
      5.2.2 - FOR SECTOR COUNTER, INSTALL SC-CB (11459) AND USE THE PROPER VERSION OF SR-CB (11411-XX) AND RDR1-CB (11643-XX) AS SHOWN ON THEIR SCHEMATICS.
   5.3 - DATA CLOCK SEPARATION
      5.3.1 - FOR ONE SHOT SEPARATOR USE IN POSITION I/O-5 THE PROPER VERSION OF D/CS-CB (11637-XX) AS SHOWN ON ITS SCHEMATIC.
      5.3.2 - FOR VFO SEPARATOR USE IN POSITION I/O-4, VFI-CB (11511) OR VFS-CB (11627); IN POSITION I/O-5 USE VFC-CB (11519); IN POSITION I/O-6 USE VFO-CB (11517), AS SHOWN ON SHEET 1 OF THIS DRAWING.
      5.3.3 - FOR EITHER SEPARATOR USE THE APPROPRIATE R/W-CB (11486-XX) VERSION AS SHOWN ON ITS SCHEMATIC.

DESK TOP INTERLOCK OPTION
2400 RPM 200TPI

Diablo Systems Incorporated

WIRING DIAGRAM 42 & 44 DISK DRIVE

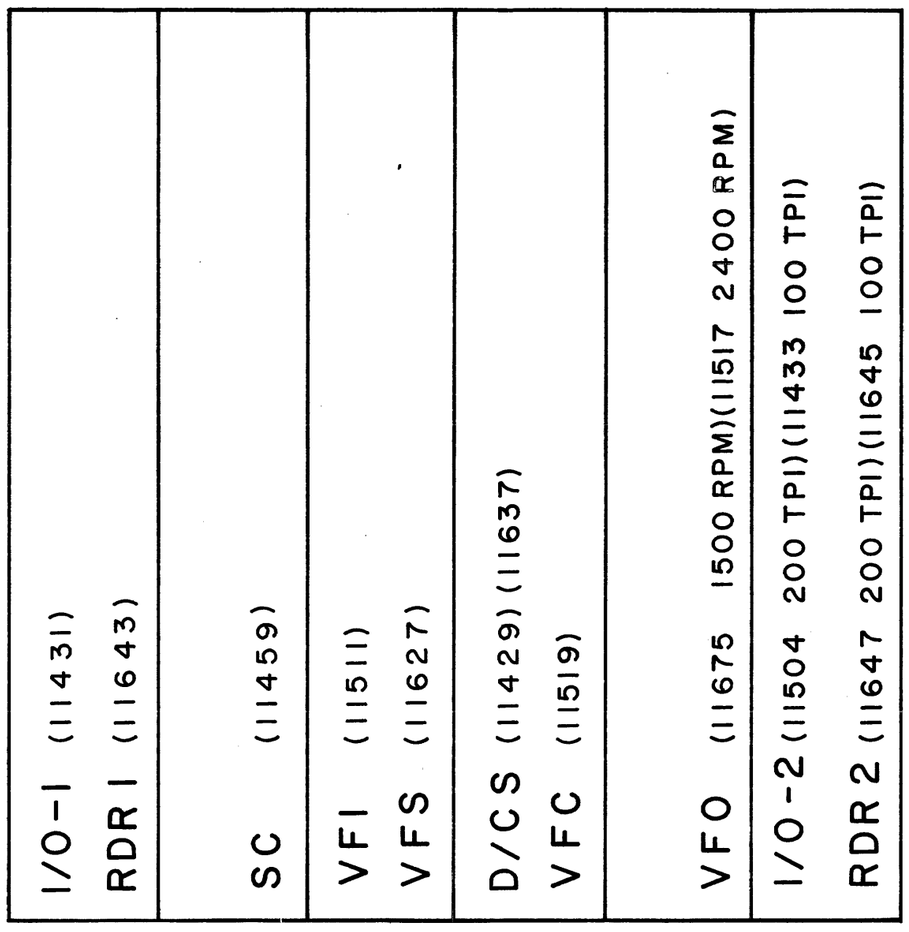
MODEL 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED. SYSTEM LOGIC NO. SL00013

SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
3	3	D	11673-XX	D

REV	ECO NO	MFG	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J									
H									
G									
F									
E									
D	4931								
C	3563								
B	3528								
A									

PRODUCT NO 11673-XX



I/O CARD CAGE

(AS VIEWED FROM THE FRONT)

PRODUCT NO.	REFERENCE DESIGNATORS NOT USED	REFERENCE DESIGNATORS LAST USED

REV	E.C.O. NO.	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J								
H								
G								
F								
E								
D								
C								
B								
A								

Diablo Systems Incorporated
Hayward, California 94545

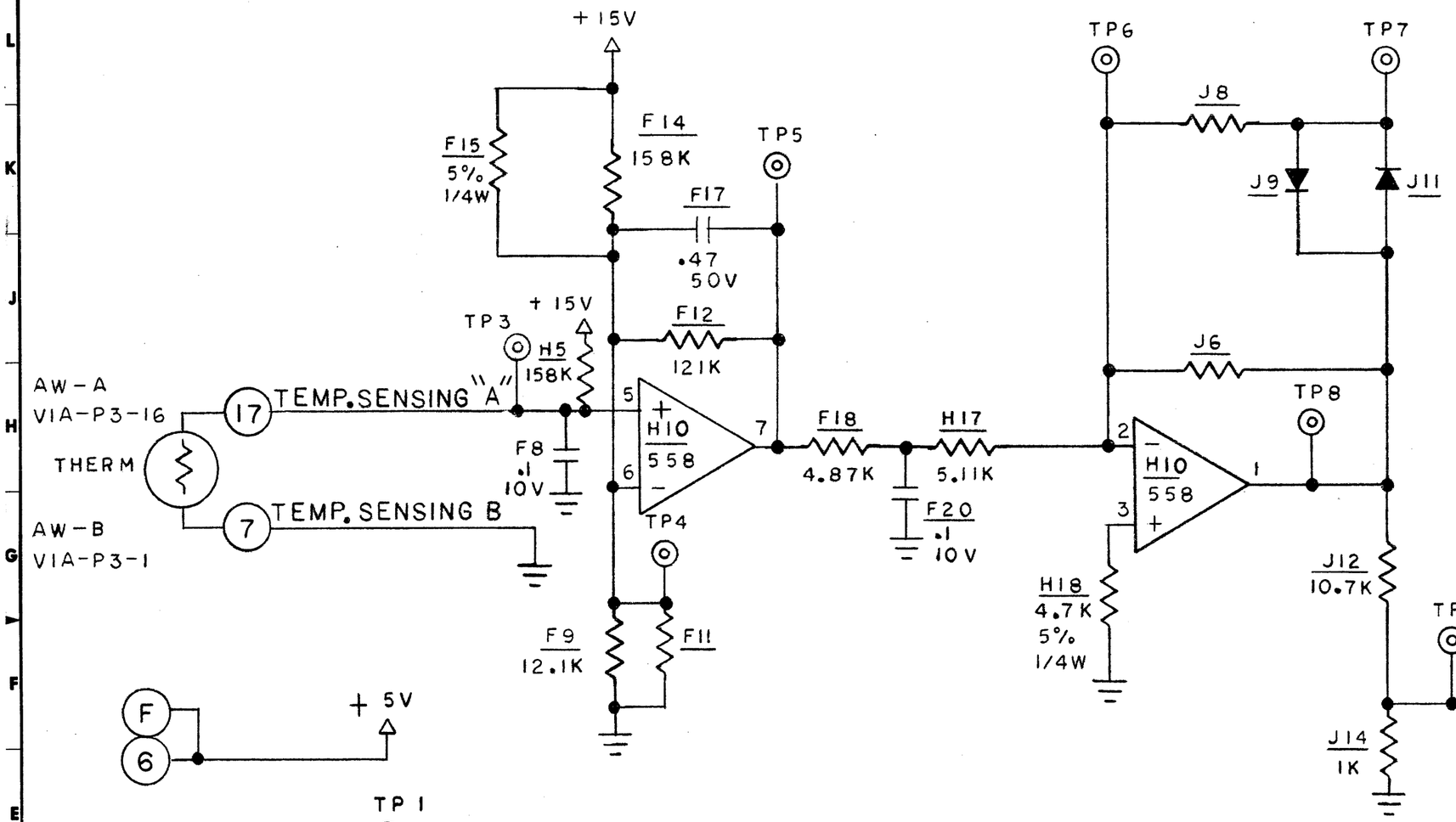
TITLE: I/O CARD CAGE LOCATOR MAP

MODEL: 40

SYSTEM LOGIC NO. SL00014

SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
1	1	B		A

PRODUCT NO. 11537 DEVELOPMENT REV. D2



NOTES:

UNLESS OTHERWISE SPECIEIED

1. ALL 1% RESISTORS ARE 1/8W.
2. ALL DIODES ARE IN4454.
3. SELECTED ACCORDING TO TEST SPECIFICATION; F11,F15,J6,J8,J9,J11.

TC MO4

Diablo Systems Incorporated
Hayward California 94545

TITLE: TEMP COMPENSATOR (TC-CB) SCHEMATIC

MODEL: MOD 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED

SYST: SL00030

SHEET | TOTAL SHEETS | SIZE B | PRODUCT 11537 | REV A

REV	E.C.O. NO.	DATE
J		
H		
G		
F		
E		
D		
C		
B		
A	3326	

MFG DATE | ENG DATE | CHECKED DATE | DRAWN DATE

PRODUCT NO. 11431-XX

P9/P10 – E (3) READ GATE INPUT (LOW TO "READ")

P9/P10 – AA (9) – DISK SELECT LINE (LOW FOR "UPPER DISK")

P9/P10 – a (E) HEAD SELECT LINE (LOW FOR "UPPER HEAD")

P9/P10 – H (C) WRITE PROTECT INPUT LINE (LOW TO "SET WRITE PROTECT")

P9/P10 – K (D) ERASE GATE LINE (LOW TO "ERASE")

P9/P10 – A (K) WRITE DATA LINE ("WRITES" ON LOW-GOING TRANSITIONS)

P9/P10 – 8 (7) WRITE GATE LINE (LOW TO "WRITE")

P9/P10 (B) FILE SELECT INPUT (LOW FOR "SELECTED") (VIA SELECT JUMPER)

M01 – R VIA P9 – 28 (T) + HEADS LOADED (NOT USED)

R/W-CB VIA P6-29 (Y) WRITE PROTECT STATUS (LOW FOR "PROTECTED")

R/W-CB VIA P6 – 28 (21) FILE READY OUTPUT (LOW FOR "READY")

M06 – 11 VIA P5 – 19 (R) SELECT INDEX MARK OUTPUT (LOW FOR "INDEX")

R/W-CB VIA P6 – 27 (11) WRITE FAULT (HIGH FOR "FAULT")

M05 – N VIA P5 – 21 (14) VOLTAGE CHECK (HIGH FOR "CHECK")

SPARES:

DATA/CLOCK GATE (HIGH FOR "DATA & CLOCKS") (10) D/C/S – 10

– DISK SELECT (LOW FOR "UPPER DISK") (P) R/W – CB VIA P6 – 25, M06 – S VIA P5 – 23

+ SELECT DISK (HIGH FOR "UPPER DISK") (8) I/O 3 – 8

HEAD SELECT (LOW FOR "UPPER HEAD") (20) R/W – CB VIA P6 – 24

WRITE PROTECT INPUT (LOW TO "SET WRITE PROTECT") (2) R/W – C3 VIA P6 – 19

ERASE GATE (LOW TO "ERASE") (17) R/W – CB VIA P6 – 18

WRITE DATA ("WRITES" ON LOW-GOING TRANSITIONS) (19) R/W – CB VIA P6 – 22

WRITE GATE (LOW TO "WRITE") (U) R/W – CB VIA P6 – 15

READ GATE (LOW TO "READ") (18) R/W – CB VIA P6 – 20

SELECTED (LOW FOR "SELECTED") (N) M06 – 7 VIA P5 – 8, M05 – 7 VIA P5 – 8, I/O 2 – N, I/O 3 – N, D/C/S – N, M09 – 7 VIA P5 – 8

PROTECT STATUS LINE (LOW FOR "PROTECTED") (16) P9/P10 – P

FILE READY LINE (LOW FOR "FILE READY") (4) P9/P10 – U

INDEX MARK LINE (LOW FOR "INDEX") (5) P9/P10 – Y

WRITE CHECK LINE (LOW FOR "WRITE CHECK") (H) P9/P10 – h

WRITE CHECK (HIGH FOR "WRITE CHECK") (13) I/O 2-13

UPPER INDEX PULSE (LOW FOR "INDEX") (X) I/O 3 – X

UPPER SECTOR PULSE (HIGH FOR "SECTOR") (J) I/O 3 – J

NOTES:
UNLESS OTHERWISE SPECIFIED
1 ALL RESISTORS ARE 1/4W 5%
2. ALL 1% RESISTORS ARE 1/8W
3. ALL DIODES ARE IN4454
4. OPTIONAL FEATURES
4.1 FOR STANDARD MACHINE (11431-00) E22 USED
4.2 FOR SECTOR COUNTER FEATURE (11431-01) E22 INDUCTOR IS NOT USED
5 ALL RESISTORS IN OHMS
6. ALL CAPACITORS IN µf

RDRI I/O I

Diablo Systems Incorporated
Hayward, California 94545

TITLE: RECEIVER/DRIVER 1
RDR I-CB

MODEL: 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO. SL00015

PRODUCT NO. 11431-XX | REV C

SHEET 1 | TOTAL SHEETS 2 | SIZE D

REFERENCE DESIGNATORS NOT USED

REFERENCE DESIGNATORS LAST USED

REV	E.C.O. NO.	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J								
H								
G								
F								
E								
D								
C	3586							
B	2570							
A	3031							

PRODUCT NO. 11643-XX

P9/P10 - E (3) — -READ GATE LINE

P9/P10 - AA (9) — -DISK SELECT LINE
LOW FOR "UPPER DISK"

P9/P10 - K (D) — -ERASE GATE LINE

P9/P10 - e (7) — -WRITE GATE LINE

P9/P10 - B (K) — -WRITE DATA LINE

P9/P10 - d (E) — HEAD SELECT LINE
LOW FOR "UPPER HEAD"

P9/P10 - H (C) — -WRITE PROTECT INPUT LINE

P9/P10 (B) — -FILE SELECT LINE
VIA SELECT JUMPER

R/W - CB (21) — -FILE READY OUTPUT
VIA P6 — 28

M05-28 (T) — -HEADS LOADED (NOT USED)
VIA P5-28

M06-11 (R) — -SELECTED INDEX MARK OUTPUT
VIA P5-19

R/W - CB (11) — + WRITE FAULT
VIA P6 - 27

R/W - CB (14) — + VOLTAGE CHECK
VIA P6-2 TO M05-N VIA P5-21

R/W - CB (Y) — -WRITE PROTECT STATUS
VIA P6-29

+ DATA / CLOCK GATE (10) — D/C/S-10

— DISK SELECT
LOW FOR "UPPER DISK" (P) — R/W - CB VIA P6 - 25; M06 - S VIA P5 - 25

— SELECT DISK
HIGH FOR "UPPER DISK" (8) — I/03 - 8

— ERASE GATE
VIA P6 - 18 (17) — R/W - CB

— WRITE GATE
VIA P6 - 15 (U) — R/W - CB

— READ GATE
VIA P6 - 20 (18) — R/W - CB

HEAD SELECT
LOW FOR "UPPER HEAD" VIA P6 - 24 (20) — R/W - CB

WRITE PROTECT INPUT
LOW TO "SET WRITE PROTECT" VIA P6 - 19 (2) — R/W - CB

— SELECTED (N) — M06-7 VIA P5 - 8; M05-7 VIA P5 - 8; I/02 - N; I/05 - N; M09-7 VIA P5 - 8; I/03 - N

— FILE READY LINE (4) — P9/P10 - U

— INDEX MARK LINE (5) — P9/P10 - Y

— WRITE CHECK LINE (H) — P9/P10 - h

+ WRITE CHECK (13) — I/02 - 13

— WRITE PROTECT STATUS LINE (16) — P9/P10 - P

— WRITE DATA
LOW GOING TRANSITIONS USED VIA P6-22 (19) — R/W - CB

— UPPER INDEX PULSE (X) — I/03 - X

+ UPPER SECTOR PULSE (J) — I/03 - J

SPARES:

NOTES

UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE 5%, 1/4W.
2. ALL 1% RESISTORS ARE 1/8W.
3. ALL DIODES ARE IN4454.
4. OPTIONAL FEATURES:
   - 4.1 FOR NO INTERRUPT OPTION A5 IS 10Ω, 5%, 1/4W, A10 & D10 ARE NOT USED.
     - 4.1.1 WITH NO SECTOR COUNTER, E22 IS A WIRE JUMPER (11643-00).
     - 4.1.2 WITH SECTOR COUNTER, E22 HAS NO WIRE JUMPER (11643-01).
   - 4.2 FOR INTERRUPT OPTION, A5 IS NOT USED.
     - 4.2.1 WITH SECTOR COUNTER, A10 IS 10Ω, 5%, 1/4W, D10 & E22 ARE NOT USED (11643-02)
     - 4.2.2 WITH NO SECTOR COUNTER, A10 & D10 ARE 10Ω, 5%, 1/4W, AND E22 IS A WIRE JUMPER (11643-03)
5. ALL RESISTORS ARE IN OHMS.
6. ALL CAPACITORS ARE IN μf.

OPTIONAL FEATURE DASH NUMBERS		
	NO INTERRUPT OPTION	INTERRUPT OPTION
NO SECTOR COUNTER	- 00	- 03
SECTOR COUNTER	- 01	- 02

RDR1 I/01

Diablo Systems Incorporated
Hayward, California 94545

TITLE: RECEIVER DRIVER CKT I
RDR1-CB SCHEMATIC

MODEL 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

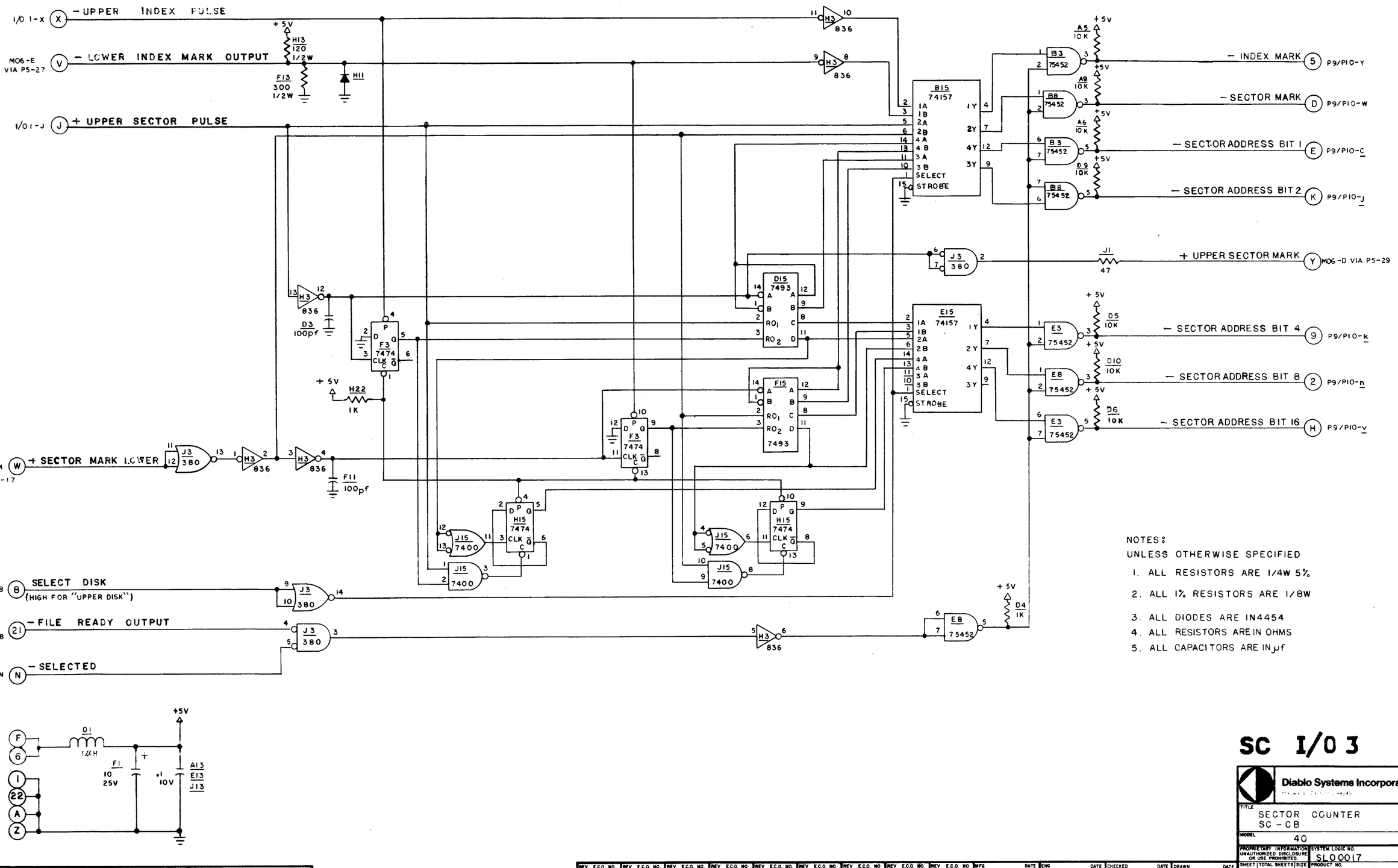
SYSTEM LOGIC NO. SL00016

SHEET 1 | TOTAL SHEETS 2 | SIZE D | PRODUCT NO. 11643-XX | REV 6

DRAWN - DATE 6/5/73 | CHECKED - DATE 7-73 | ENG - DATE | MFG - DATE

REV	E.C.O. NO.
J	
H	
G	
F	
E	
D	
C	
B	4048
A	2998

PRODUCT NO 11643-XX | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED



NOTES:
UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W 5%
2. ALL 1% RESISTORS ARE 1/8W
3. ALL DIODES ARE IN4454
4. ALL RESISTORS ARE IN OHMS
5. ALL CAPACITORS ARE IN μf

SC I/O 3

Diablo Systems Incorporated

TITLE: SECTOR COUNTER SC-CB

MODEL: 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO. SL00017

SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
1	2	D	11459	C

REV	J	H	G	F	E	D	C	B	A
E.C.O. NO.							3471	3340	

MFG | DATE | ENG | DATE | CHECKED | DATE | DRAWN | DATE

REFERENCE DESIGNATORS

REFERENCE DESIGNATORS

PRODUCT NO. 11511

PRODUCT NO. 11511 DEVELOPMENT REV. D1

I/05-K (K) -READ DATA

I/05-18 (U) -2F REF

I/05-9 (9) -READ CLK

I/05-Y (Y) +START OSC

I/05-R (R) +IF REF

I/05-14 (14) -IF REF

- SET PHASE (C) I/05-C

-READ DATA I/O (7) P9-C P10-C

-READ CLK I/O (8) P9-A P10-A

+5V

E10 120

E15

E3 S10

7493

D15 S04

E22 1K

F15 CLK S112

B15 S00

F3

DI0 120

TP1

A15 CLK S112

B3 CLK S112

D3 75452

D7 1K

D8 1K

TP2

TP3

6 F

1 22 A Z

D1 1μH

F1 10 25V

A13, E13, J13 .1 , 10V

TP4 GND

NOTES:

UNLESS OTHERWISE SPECIFIED

1 ALL LOGIC GATES 7400 "S" SERIES.

2 ALL RESISTORS 5% , 1/4 W.

3 ALL RESISTORS ARE IN OHMS.

4 ALL CAPACITORS ARE IN μf.

VFI I/O 4

Diablo Systems Incorporated
Hayward, California 94545

TITLE: VFI - SCHEMATIC

MODEL: MOD 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO. SL00018

SHEET 1 TOTAL SHEETS 2 SIZE D PRODUCT NO. 11511 REV A

PRODUCT NO. 11511

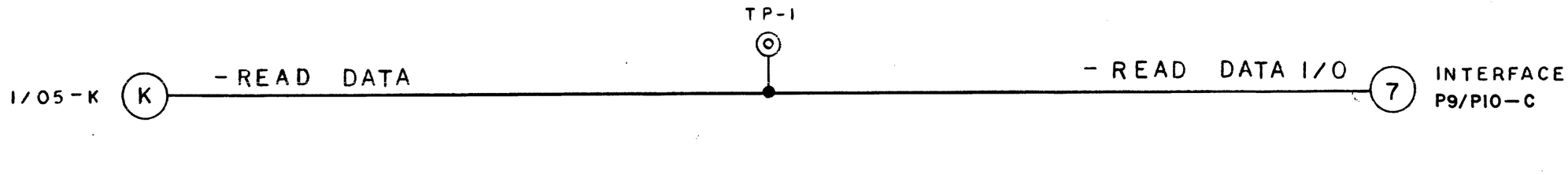
REFERENCE DESIGNATORS NOT USED

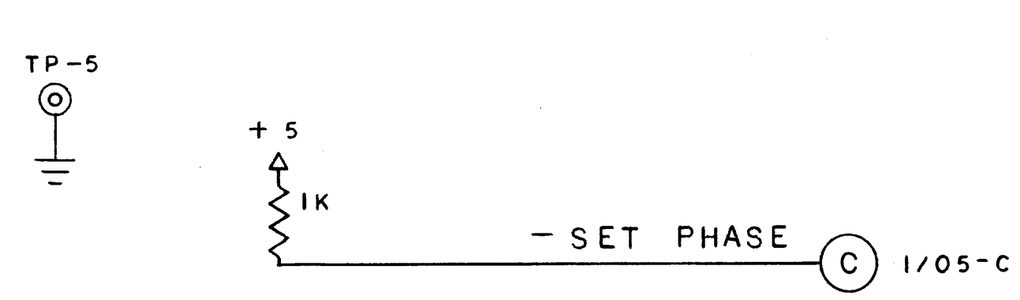
REFERENCE DESIGNATORS LAST USED

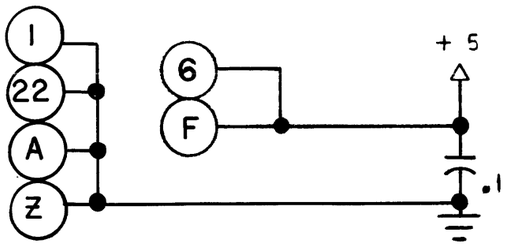
REV E.C.O. NO. J | H | G | F | E | D | C | B | A 3440 5-3-73

MFG DATE ENG DATE CHECKED DATE DRAWN DATE

PRODUCT NO 11627 DEVELOPMENT REV. D1







VFS I/O 4

Diablo Systems Incorporated
Hayward, California 94545

TITLE: VFS — SCHEMATIC

MODEL: MOD 40

SYSTEM LOGIC NO. SL 00019

SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
1	2	B	11627	B

PRODUCT NO	REFERENCE DESIGNATORS NOT USED	REFERENCE DESIGNATORS LAST USED
11627		

REV	ECO NO	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J								
H								
G								
F								
E								
D								
C								
B	3647							
A	—		MFG					

PRODUCT NO. 11429-XX DEVELOPMENT REV. D4

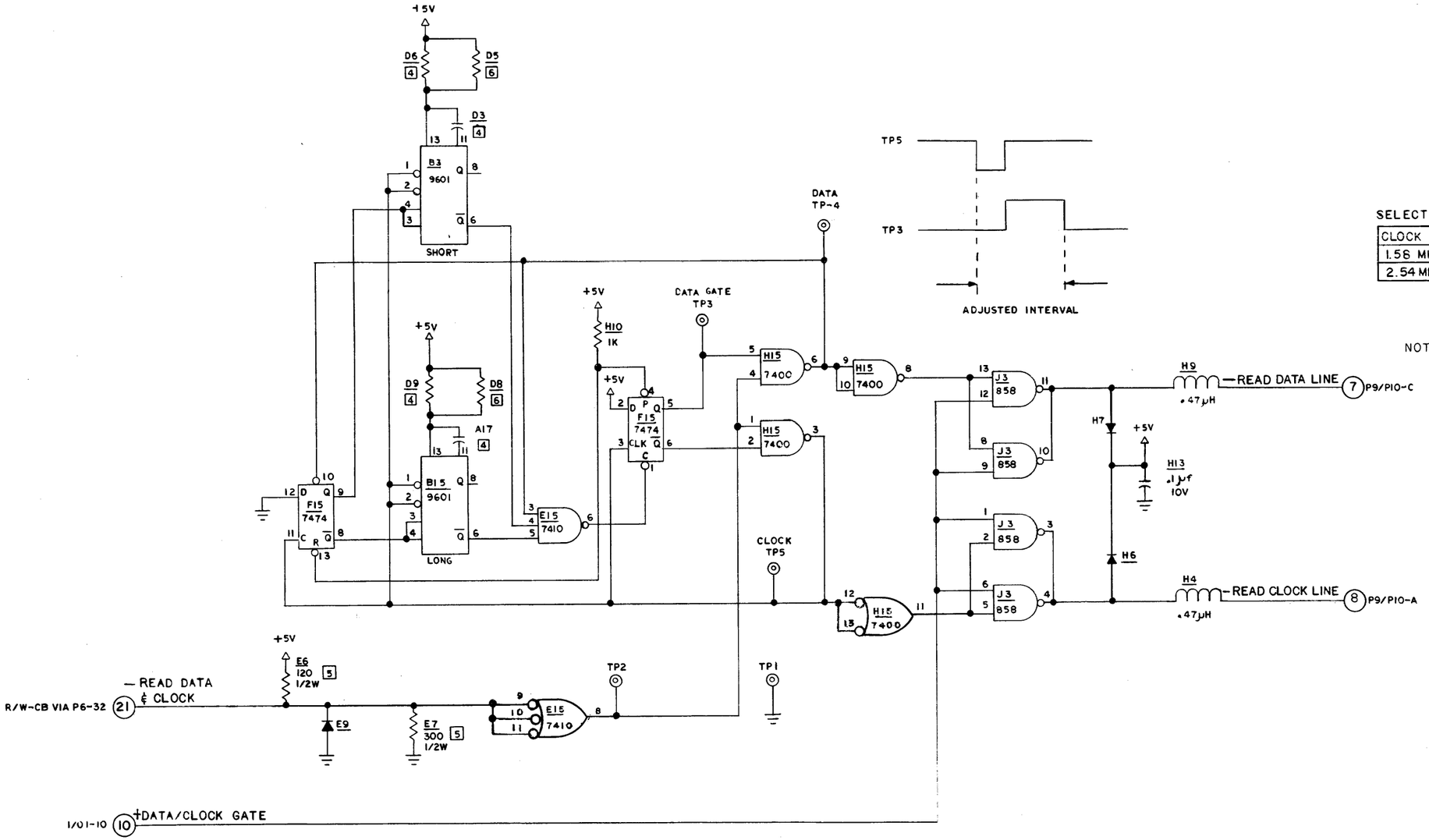
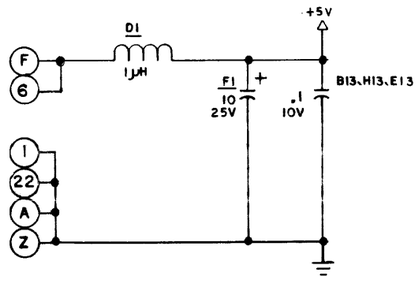


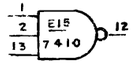
TABLE I
SELECT FOR INTERVALS AS FOLLOWS:

CLOCK RATE	"D5" INTERVAL	"D8" INTERVAL
1.58 MHZ	450 NS	470 NS
2.54 MHZ	290 NS	305 NS

NOTES:
UNLESS OTHERWISE SPECIFIED
1 ALL RESISTORS ARE 1/4W 5%.
2 ALL 1% RESISTORS ARE 1/8W.
3 ALL DIODES ARE IN4454.
4 OPTIONAL FEATURES
11429-00 1500 RPM USE:
100PF(10062-10)IN LOCATION A17-D3,
10.5K 1/8W 1%(10004-03) IN D6-D9.
11429-01 2400 RPM USE:
62PF(10061-62)IN LOCATION A17-D3
8.25K 1/8W 1%(10003-89) IN D6-D9.
5 RES 120Ω 1/2W 10032-12 AT LOCATION E6 & 300Ω 1/2W 10032-30 AT LOCATION E7 ARE TO BE REMOVED IF USED IN MACHINE WITH R/W ASSY #'S 11486-XX OR 11497.
6 D5 & D8 ARE SELECTED TO GIVE TIME INTERVALS SHOWN IN TABLE I ABOVE.
7 ALL RESISTORS ARE IN OHMS.
8 ALL CAPACITORS ARE IN µf.



SPARE



D/CS 1/05

Diablo Systems Incorporated

TITLE DATA/CLOCK SEPARATOR CKT.
D/CS-CB SCHEMATIC

MODEL 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED. SYSTEM LOGIC NO. SL00020

SHEET 1 TOTAL SHEETS 2 SIZE D PRODUCT NO. 11429-XX REV B

PRODUCT NO. 11519

PRODUCT NO. 11519 DEVELOPMENT REV. D2

I/06-21 (15) -DATA GT INHIBIT

I/06-17 (17) +2F REF

I/04-C (C) -SET PHASE

I/06-18 (18) -2F REF

I/06-S (S) -RST LAG LT

P6-32 (21) -FILE DATA

I/01-10 (10) +DATA/CLOCK GT

(19) -24VOLTS

TP1

TP2

TP3

TP4 GROUND

J5 120

J6 120pf

J7 1.2K

J23 0.1

J20 5.1K

J15 74S5601

F20 1K

F5 1K

D1 1μH

B1 0.1

B13 0.1

A1 0.1

F1 0.1

A13 0.1

E13 0.1

J13 0.1

E1 0.1

H1 82, 1W

J3 IN4746, 1W

J4 0.1

F15 240 2W

J9 IN4736, 1W

J8 0.1

-18V

-6.8V

B8 1K

B7 1K

+5V

+4V

GND

160ns

240 ns

-READ DATA (K) I/04-K

-READ CLK (9) I/04-9

+ I F REF (R) I/04-R

— I F REF (14) I/04-14

-LAG ERR (2) I/06-2

+LAG LT (H) I/06-9

-LEAD ERR (B) I/06-B

+OSC START (Y) I/04-Y

-OSC START (12) I/06-12

-HI GAIN (4) I/06-4

-18 VOLTS (E) I/06-E

-6.8 VOLTS (D) I/06-D

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL LOGIC GATES: 7400 "S" SERIES.
2. ALL RESISTORS: 5%, METAL FILM 1/4W.
3. ALL CAPACITORS ARE μf.
4. ALL RESISTORS ARE OHMS.
5. ALL WAVEFORMS SYNC ON POS TRANSITION OF DATA GATE, TPI ON VFC CARD.
▲ DENOTES TRIGGER.
VERT DIVISION = 1V, HORIZ DIVISION = 40ns.
DATA PATTERN ONES FREQ 5.085 MHZ.

VFC I/O 5

Diablo Systems Incorporated
Hayward California 94545

TITLE: VFC — SCHEMATIC

MODEL: SERIES 40 DRIVE

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED. SYSTEM LOGIC NO. SL00021

REV	E.C.O. NO.	DFS	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J									
H									
G									
F									
E									
D									
C									
B	3985								
A	3440								

SHEET 1 TOTAL SHEETS 2 SIZE D PRODUCT NO. 11519 REV B

PRODUCT NO. 11519 | REFERENCE DESIGNATORS | REFERENCE DESIGNATORS

PRODUCT NO. 11637-XX

PRODUCT NO. 11637-XX DEVELOPMENT REV. D5

TABLE 1						
SPINDLE SPEED	CAPACITORS D3 & D13	RESISTORS D6 & D9	RESISTOR F10	D5 INTERVAL	D8 INTERVAL	ASSY IDENTIFICATION
1500 RPM	100pf ±5% MICA	10.5K±1%, 1/8W	–	450 NS	470 NS	11637-00
2400 RPM	62 pf ±5% MICA	8.25K±1%, 1/8W	–	280 NS	290 NS	11637-01
UNSEP. DATA	–	–	10Ω±5%, 1/4W	SEE NOTE 4.2		11637-02

R/W-CB VIA P6-32 (21) -READ DATA AND CLOCK

F9

H15 7400

TP-2 TP-1 GND

+5V

D5 D6

D3

B3 9601 SHORT

ONES TRIG

F15 7474

F10

DATA TP-4

H15 7400

H10 1K

DATA GATE TP-3

E15 7410

H15 7400

CLOCK TP-5

D8 D9

D13

D15 9601 LONG

E15 7410

I/O 1-10 (10) +DATA/CLOCK GATE

TP 5

TP 3

ADJUSTED INTERVAL

H4 82 F4 300pf H7 82

-READ DATA LINE (7) P9/P10-C

-READ CLOCK LINE (8) P9/P10-A

J10 1K

H5 82 H9 300pf H6 82

J3 75450

SPARE

H15 7400

D1 1 μH

B1 12μf 20V

E1,H1 12μf 20V

E13,H13, E13,J1 .1μf 10V

NOTES:
UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4 w, 5%.
2. ALL 1% RESISTORS ARE 1/8W.
3. ALL DIODES ARE IN4454.
4. OPTIONAL FEATURES:
   - 4.1 FOR SEPARATED DATA F10 IS NOT USED. RESISTORS D5 & D8 ARE SELECTED TO GIVE TIME INTERVALS SHOWN IN TABLE 1 ABOVE.
   - 4.2 FOR UNSEPARATED DATA F10 IS 10Ω, ±5%, 1/4W. COMPONENTS D3, D13, D6 AND D9 ARE NOT USED. TIME INTERVAL ADJUSTMENT IS NOT REQUIRED (11637-02).
5. 9601 SHOULD NOT BE SUBSTITUTED WITH A 74122.
6. ALL RESISTORS ARE IN OHMS.
7. ALL CAPACITORS ARE IN μf.

D/CS I/O 5

Diablo Systems Incorporated
Hayward, California 94545

TITLE: DATA/CLOCK SEPARATOR CKT. D/CS-CB SCHEMATIC

MODEL: 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO. SL00022

SHEET 1 TOTAL SHEETS 2 SIZE D PRODUCT NO. 11637-XX REV B

PRODUCT NO. 11637-XX

REFERENCE DESIGNATORS NOT USED

REFERENCE DESIGNATORS NOT USED

REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO	REV	E.C.O. NO.	REV	E.C.O. NO	MFG	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J		H		G		F		E		D		C		B	3625	A	2998								

PRODUCT NO. 11675

DEVELOPMENT REV. b2

I/05-2 (2) -LAG ERR

I/05-B (B) -LEAD ERR

I/05-H (9) +LAG LT

I/05-4 (4) -HI GAIN

I/05-12 (12) -OSC START

I/05-D (D)

I/05-E (E)

(I, 22, A, Z) (F, 6)

+5V, -6.8V, -18V

TP1 +2.8V NOM.

TP2, TP3, TP4

10 TRIGGER 320 ns +2V GND

10 TRIGGER 320 ns GND -4V

10 TRIGGER 320ns GND -3V

10 TRIGGER 350 ns +4V GND

-RST LAG LT (S) I/05-S

- DATA GT INHIBIT (21) I/05-15

- 2F REF (18) I/05-18 I/04-U

+2F REF (17) I/05-17

SPARE

NOTES:

UNLESS OTHERWISE SPECIFIED

1 ALL LOGIC GATES 7400 "S" SERIES.
2 ALL RESISTORS 5% , METAL FILM 1/4W
3 ALL 0.1μf CAP'S ARE 50V.
4 ALL 1% RESISTORS ARE 1/8W.
5 ALL POTS 20 TURN CERMET.
6 ALL PNP TRANSISTORS MPS 3640
7 ALL NPN TRANSISTORS MPS 2369
8 ALL CAPACITORS ARE μf
9 ALL RESISTORS ARE OHMS

10 ALL WAVEFORMS SYNC ON POS TRANSITION OF DATA GATE, TP1 ON VFC CARD. VERT DIVISION = 1V, HORIZ UNCALIBRATED TO SHOW TWO CYCLES, DATA PATTERN ONES FREQ 3.177 MHZ.

11 ALL DIODES ARE IN4454.

VFO I/O 6

Diablo Systems Incorporated

VFO SCHEMATIC (1500RPM)

MODEL MOD 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED

SYSTEM LOGIC NO. SL00023

SHEET 1 TOTAL SHEETS 2 SIZE D PRODUCT NO 11675 REV C

PRODUCT NO 11675 | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED

REV J	REV H	REV G	REV F	REV E	REV D	REV C 3699	REV B 3649	REV A 3531	MFG	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE

PRODUCT NO. 11517 | DEVELOPMENT REV. D3

I/05-2 (2) -LAG ERR
I/05-8 (8) -LEAD ERR
I/05-H (9) +LAG LT
I/05-4 (4) -HI GAIN
I/05-12 (12) -OSC START
I/05-D (D)
I/05-E (E)
(1, 22, A, Z)

TP1 +2.8V NOM.
TP2
TP3
TP4

-RST LAG LT (S) I/05-S
-DATA GT INHIBIT (21) I/05-15
-2F REF (18) I/05-18 I/04-U
+2F REF (17) I/05-17

SPARE

NOTES:
UNLESS OTHERWISE SPECIFIED
1 ALL LOGIC GATES 7400 "S" SERIES.
2 ALL RESISTORS 5% , METAL FILM 1/4W
3 ALL 0.1μf CAP'S ARE 50V.
4 ALL 1% RESISTORS ARE 1/8W.
5 ALL POTS 20 TURN CERMET.
6 ALL PNP TRANSISTORS MPS 3640
7 ALL NPN TRANSISTORS MPS 2369
8 ALL CAPACITORS ARE μf
9 ALL RESISTORS ARE OHMS

10 ALL WAVEFORMS SYNC ON POS TRANSITION OF DATA GATE, TP1 ON VFC CARD.
VERT DIVISION = 1V, HORIZ DIV = 40ns.
DATA PATTERN ONES FREQ 5.085 MHZ.

11 ALL DIODES ARE IN4454.

VFO I/O 6

Diablo Systems Incorporated
Hayward, California 94545

TITLE: VFO-SCHEMATIC (2400RPM)
MODEL: MOD 40
PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE ON USE PROHIBITED.
SYSTEM LOGIC NO. SL00024
SHEET 1 | TOTAL SHEETS 2 | SIZE D | PRODUCT NO. 11517 | REV D

REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	MFG	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J		H		G		F		E		D	3699	C	3592	B	3505	A	3440 5-3-73						

PRODUCT NO. 11517 | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED

PRODUCT NO. 11645-XX

P9/P10-BB (9) — TRACK ADDRESS LINE — BIT 128
P9/P10-b (D) — BIT 64
P9/P10-T (H) — BIT 32
P9/P10-f (C) — BIT 16
P9/P10-X (E) — BIT 8
P9/P10-J (K) — BIT 4
P9/P10-S (3) — BIT 2
P9/P10-N (J) — BIT 1
P9/P10-m (B) — TRACK ADDRESS LINE — BIT 0
P9/P10-t (8) — STROBE LINE
P9/P10-W (7) — RESTORE LINE

I/O1-N (N) — SELECTED
M05-R VIA P5-28 (T) — +HEADS LOADED
M09-T VIA P5-31 (R) — -ADDRESS ACKNOWLEDGE OUTPUT
M09-16 VIA P5-32 (14) — -LOGICAL ADDRESS INTERLOCK OUTPUT
(P) FILE READY (NOT USED)
M06-9 VIA P5-10 (12) — -INITIAL RESET
M[illegible]-C VIA P5-6 (11) — -SEEK INCOMPLETE OUTPUT
I/O1-13 (13) — +WRITE CHECK
M08-[illegible] VIA P5-[illegible] (V) — -READY TO S/R/W OUTPUT

(1, 22, A, Z) (F, 6) D1 1μH, F1 10 25V, A11-A13, D13, D14 .1 10V

+5V A22 3.3K
+5V A23 10K
+5V B22 10K
+5V B23 10K
+5V D22 10K
+5V A14 4.7K
+5V J23 120 1/2W
+5V H23 120 1/2W
+5V H13 120 1/2W
+5V D18 120 1/2W
+5V A21
+5V D23 10K

J22 300 1/2W
H22 300 1/2W
J11 300 1/2W
B13 300 1/2W
E11 10K
E12
E13
J13
B12
B21
D21

F11 47 — BIT 128 (18) M09-L VIA P5-14
J8 47 — BIT 64 (19) M09-M VIA P5-16
J9 47 — BIT 32 (17) M09-10 VIA P5-12
J7 47 — BIT 16 (W) M09-11 VIA P5-13
J10 47 — BIT 8 (U) M09-14 VIA P5-24
J3 47 — BIT 4 (Y) M09-13 VIA P5-20
E23 47 — BIT 2 (16) M09-R VIA P5-26
J4 47 — BIT 1 (21) M09-P VIA P5-22
E22 47 — BIT 0 (S) M09-K VIA P5-9
J5 47 — STROBE (X) M09-12 M06-K VIA P5-15
J6 47 — RESTORE (20) M09-N M06-N VIA P5-18

-ADDRESS ACKNOWLEDGE LINE (2) P9/P10-P
-LOGICAL ADDRESS INTERLOCK LINE (5) P9/P10-Y
+ATTENTION LINE (10) P9/P10 VIA ATTENTION JUMPER
-SEEK INCOMPLETE LINE (4) P9/P10-U
-READY TO S/R/W LINE (L) P9/P10-F

SPARES:

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTORS ARE 1/4 ±5%.
2. ALL 1% RESISTORS ARE 1/8W.
3. ALL DIODES ARE IN4454.
4. OPTIONAL FEATURES:
   4.1 FOR STANDARD MACHINE (11645-00) A21 & B21 ARE NOT USED D21 IS A WIRE JUMPER.
   4.2 FOR SERIES 30 COMPATIBILITY WITHOUT INTERRUPT CAPABILITY (11645-02) A21 IS 1K, 1/4W, 5%. D21 IS A WIRE JUMPER
   4.3 FOR SERIES 30 COMPATIBILITY WITH INTERRUPT CAPABILITY (11645-03) A21 IS 1K, 1/4W, 5%. WIRE JUMPER IN POSITION D21 IS ELIMINATED AND ONE INSERTED INTO POSITION B21.
5. ALL CAPACITORS ARE μf.
6. ALL RESISTORS ARE OHMS.

RDR2 I/O 2

Diablo Systems Incorporated

TITLE: RECEIVER-DRIVER CKT 2 RDR2-CB(100TPI) SCHEMATIC
MODEL 40
PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.
SYSTEM LOGIC NO. SL[illegible]025
SHEET 1 | TOTAL SHEETS 2 | SIZE D | PRODUCT NO. 11645-XX | REV A

PRODUCT NO. 11645-XX | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED

REV	E.C.O. NO.	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J								
H								
G								
F								
E								
D								
C								
B								
A	2998	MFG						

P9/P10-BB (9) — TRACK ADDRESS LINE -BIT 128
P9/P10-b (D) — -BIT 64
P9/P10-T (H) — -BIT 32
P9/P10-f (C) — -BIT 16
P9/P10-x (E) — -BIT 8
P9/P10-J (K) — -BIT 4
P9/P10-s (3) — -BIT 2
P9/P10-N (J) — TRACK ADDRESS LINE -BIT 1
P9/P10-t (8) — STROBE LINE
P9/P10-w (7) — RESTORE LINE
P9/P10-m (B) — TRACK ADDRESS LINE -BIT 256

D3 8836 · B3 8836 · B3 8836 · A3 8836 · B3 8836 · D3 8836 · A3 8836 · D3 8836 · D3 8836 · B3 8836 · A3 8836

F3 380 · E15 380 · F3 380 · E15 380 · H3 380 · E15 380 · H3 380 · E15 380 · H3 380 · E3 380

J8 47 · J9 47 · J7 47 · J10 47 · J3 47 · E23 47 · J4 47 · E22 47 · J5 47 · J6 47 · F11 47

-BIT 128 (19) M09-M VIA P5-16
-BIT 64 (17) M09-10 VIA P5-12
-BIT 32 (W) M09-11 VIA P5-13
-BIT 16 (U) M09-14 VIA P5-24
-BIT 8 (Y) M09-13 VIA P5-20
-BIT 4 (16) M09-R VIA P5-26
-BIT 2 (21) M09-P VIA P5-22
-BIT 1 (S) M09-K VIA P5-9
-STROBE (X) M09-12 VIA P5-15, M06-K VIA P5-15
-RESTORE (20) M09-N VIA P5-18, M06-N VIA P5-18
-BIT 256 (18) M09-L VIA P5-14

M05-R VIA P5-28 (T) + HEADS LOADED
I/01-N (N) - SELECTED
M09-T VIA P5-31 (R) - ADDRESS ACKNOWLEDGE OUTPUT
(P) FILE READY (NOT USED)
M06-9 VIA P5-10 (12) - INITIAL RESET
M06-C VIA P5-6 (11) - SEEK INCOMPLETE OUTPUT
I/01-13 (13) + WRITE CHECK
M09-P VIA P5-32 (14) - LOGICAL ADDRESS INTERLOCK OUTPUT
M08-L VIA P5-11 (V) - READY TO S/R/W OUTPUT

F3 380 · J15 7402 · B21 [4] · E3 380 · J23 120,1/2W · F3 380 · F15 7400 · E12 · B11 · J22 300 1/2W · E4 [4] · E11 10K · A3 8836 · A14 4.7K · J15 7402 · D17 120,1/2W · B12 · B13 300 1/2W · J15 7402 · J15 7402 · H23 120 1/2W · E13 · H22 300 1/2W · H13 120 1/2W · J13 · J11 300 1/2W · H15 7410 · F15 7400 · H15 7410 · H15 7410 · F15 7400 · D16 75452 · D23 10K · +ATTENTION LINE (10) P9/P10 VIA ATTENTION JUMPER

A16 75452 · A23 10K · -ADDRESS ACKNOWLEDGE LINE (2) P9/P10-P
B16 75452 · B22 10K · -LOGICAL ADDRESS INTERLOCK LINE (5) P9/P10-y
A16 75452 · A22 10K · -200 TRACKS PER INCH (M) P9/P10-z
[4] B20
B16 75452 · B23 10K · -SEEK INCOMPLETE LINE (4) P9/P10-u
D16 75452 · D22 10K · -READY TO S/R/W LINE (L) P9/P10-F

SPARES: E3 8836 · E3 8836

F1 10 25V · D1 1μh · A11, A13 D13, D14 .1 10V · +5V

NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 5%, 1/4W.
2. ALL 1% RESISTORS ARE 1/8W.
3. ALL DIODES ARE IN4454.
4. OPTIONAL FEATURES:
4.1 FOR STANDARD MACHINE (11647-00) B11 & B21 ARE NOT USED. B20 IS A WIRE JUMPER.
4.2 FOR SERIES 30 COMPATIBILITY WITHOUT INTERRUPT CAPABILITY (11647-02) B11 IS 1K, 1/4W, 5%. B20 IS A WIRE JUMPER.
4.3 FOR SERIES 30 COMPATIBILITY WITH INTERRUPT CAPABILITY (11467-03) B11 IS 1K, 1/4W, 5%, WIRE JUMPER IN POSITION B20 IS ELIININATED AND ONE INSERTED INTO POSITION B 21.
5. ALL RESISTORS ARE IN OHMS.
6. ALL CAPACITORS ARE IN μf.

REFERENCE DESIGNATORS NOT USED
REFERENCE DESIGNATORS NOT USED

REV J · E.C.O. NO. · REV H · E.C.O. NO. · REV G · E.C.O. NO. · REV F · E.C.O. NO. · REV E · E.C.O. NO. · REV D · E.C.O. NO. · REV C · E.C.O. NO. · REV B 3507 · REV A · MFG · DATE · ENG · DATE · CHECKED · DATE · DRAWN · DATE

RDR2 I/O 2

Diablo Systems Incorporated
Hayward California 94545

TITLE: RECEIVER/DRIVER CIRCUIT 2 RDR2 - CB SCHEMATIC (200 TPI)
MODEL: 40
PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.
SYSTEM LOGIC NO. SL00026
SHEET 1 TOTAL SHEETS 2 SIZE D
PRODUCT NO. 11647-XX REV B

01	02	03	04	05	06	07	08	09
SD (11416) (11613)	OR (11414)	(SPARE)	TC (11537) (MOD 44 ONLY)	(11409) SL (11471)	SR (11411)	(11402) SO (11633)	AL2 (11407)	AL1 (11404)

MAIN CARD CAGE

(AS VIEWED FROM THE FRONT)

Diablo Systems Incorporated
Hayward, California 94545

TITLE: MAIN CARD CAGE LOCATOR MAP

MODEL: 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO. SL.00027

SHEET 1 | TOTAL SHEETS 1 | SIZE B | PRODUCT NO. | REV A

DEVELOPMENT REV. D2

PRODUCT NO. 11613-XX

PRODUCT NO. 11613-XX DEVELOPMENT REV. D6

DPSS VIA P3-12 (X) DISK PACK SAFETY SWITCH (HIGH WHEN HEADS RETRACTED)

E55 A14F — E52 820 1/2W — +15V — E54 390 — E51 2K 1/2W — −15V

DISK PACK SAFETY (Y) M08-7 (LOW FOR "INTERLOCKED")

M05-H (H) + BRUSH HOME

M05-B (D) − HEADS RETRACTED

M05-14 (R) + SPEED OK

HS-CB VIA P1-5 (12) SPEED SENSE B

HS-CB VIA P1-12 (E) SPEED SENSE A — F6 1K

H6 2M — H8 558 — J10 — J11 — H14 1M — J12 1 5% — F10 470 — H8 558 — F9 100K — −15V

F11 3.3K — F12 — F13 — +5V — +SPINDLE STOPPED

H15 7400 — A27 7426 — +SPINDLE ROTATING

F15 7400 — TP2 — H36 4.7K — +5V

M05-C (B) −UNLOCK DRAWER

F15 7400

H39 7420 — E56 [6] — E48 10 [6]

F51 7400 — F51 7400 — F51 7400 — F51 7400 — H51 7410

TP3 — B6 2,2K — +15V — B5 1,5K — A5 2N3643 — B4 22K — −15V

+SPINDLE MOTOR CURRENT CONTROL (GND FOR "FULL" CURRENT) (C) HS-C8 VIA P1-14

SPINDLE MOTOR CURRENT CONTROL

B27 858 — B9 2K — +15V — B8 1K — A9 2N3644 — B7 3,9K — −15V

SPINDLE MOTOR — CURRENT CONTROL (GND FOR "FULL" CURRENT) (3) HS-C8 VIA P1-3

− DRAWER UNLOCK ENABLE (2) HS-CB VIA P1-2

+5V — B51 27K — B47 39 10V — A1 Q — A39 — A2 74121 — B — Q — B10 4.7K — +5V

A27 7426 — A27 7426 — +15V — B12 1,5K — B11 5.6K — B13 27K — −15V — A13 2N3643

+ DRAWER UNLOCK PICK (5) HS-CB VIA P1-15

+15V — J26 3,3K — J27 2K — J29 7,5K — −15V — J17 2N3643

−CLAMP Ø2

M06-9 (K) −INITIAL RESET

M05-S (S) + SPINDLE DRIVE ON

F15 7400 — H15 7400 — H15 7400 — A27 7426 — TP9 — D22 4.7K — +5V

B27 858 — D28 200pf — D29 1M — F27 7400 — F39 836 — D27 100K — E39 558 — D30 2K — D31 — TP7 — PHASE 2B (9) HS-CB VIA P1-9 (GND IF "BRAKING")

B53 — D53

(I) (22) (A) (Z) — (F) (6) — D4 1μH — F4 10 25V — .1 10V — A38, A48, D47, E36, E25, H25, J35, J47

M02-16 (16) +PHASE 2

F27 7400 — F39 836 — D17 100K — D18 200pf — D19 1M — E39 558 — D20 2K — D21 — TP8 — PHASE 2A (J) HS-CB VIA P1-7 (GND IF "BRAKING")

B54 — D54

(13) (P) — F1 27μH — H1 10 25V — F7 .1 50V — +15V

TP4 — F39 836 — B27 858 — J28 3,3K — +15V — J30 2K — J31 7,5K — −15V — J21 2N3643

M06-4 (U) POS. SPINDLE DRIVE CUT OFF (GND IF CUT OFF)

−CLAMP Ø1

F27 7400 — F39 836 — D9 100K — D10 200pf — D11 1M — D39 558 — D12 2K — TP6 — PHASE 1B (7) HS-CB VIA P1-6 (LOW IF "BRAKING")

B55 — D55 — D13

M06-5 (V) NEG. SPINDLE DRIVE CUT OFF (GND IF CUT OFF)

(L) (10) — D1 27μH — A1 10 25V — H12 .1 50V — −15V — +5V — H48 1K

J39 7474 — J39 7474 — TP1 — H15 7400 — −BRAKE — H39 7420 — F39 836 — F27 7400 — F39 836 — B17 100K — B18 200pf — B19 1M — D39 558 — B20 2K — TP5 — PHASE 1A (4) HS-CB VIA P1-4 (HIGH IF "BRAKING")

B56 — D56 — B21

M02-15 (15) +PHASE 1

+5V — D45 22K — E45 22K

SPARE — H51 7410

SD M01

NOTES; UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE ±5% 1/4W
2. ALL 1% RESISTORS ARE 1/8W
3. ALL DIODES ARE IN4454
4. ALL RESISTORS IN OHMS
5. ALL CAPACITORS ARE IN μf

[6] OPTIONAL FEATURES
6.1 FOR STANDARD MACHINE (11613-00) INSTALL JUMPER IN POSITION E48.
6.2 FOR INTERLOCK OPTION (11613-01) INSTALL JUMPER IN POSITION E56.

Diablo Systems Incorporated
Hayward, California 94545

TITLE: SPINDLE DRIVE SD-CB SCHEMATIC

MODEL: 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO. SL00028

SHEET 1 TOTAL SHEETS 2 SIZE D PRODUCT NO. 11613-XX REV F

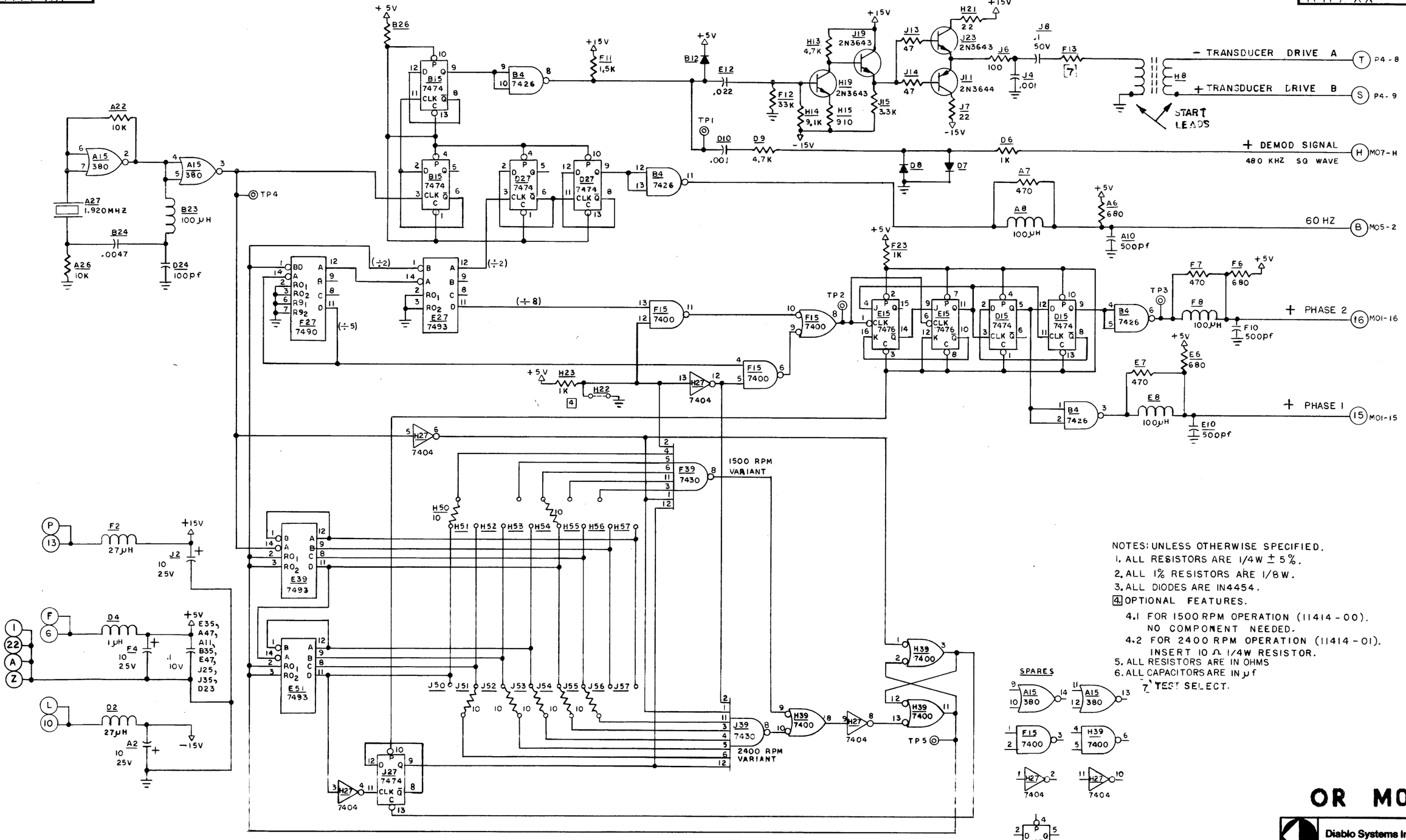
F4136

REV	E.C.O. NO.	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J								
H								
G								
F	3993							
E	3652							
D								
C								
B								
A								

PRODUCT NO. 11613-XX — REFERENCE DESIGNATORS — REFERENCE DESIGNATORS

PRODUCT NO. 11414-XX

PRODUCT NO. 11414-XX | DEVELOPMENT REV. D4



NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTORS ARE 1/4W ± 5%.
2. ALL 1% RESISTORS ARE 1/8W.
3. ALL DIODES ARE IN4454.
4. OPTIONAL FEATURES.
   - 4.1 FOR 1500 RPM OPERATION (11414-00). NO COMPONENT NEEDED.
   - 4.2 FOR 2400 RPM OPERATION (11414-01). INSERT 10 Ω 1/4W RESISTOR.
5. ALL RESISTORS ARE IN OHMS
6. ALL CAPACITORS ARE IN µf
7. TEST SELECT.

SPARES

OR M02

Diablo Systems Incorporated

TITLE: OSCILLATOR CIRCUIT OR - CB SCHEMATIC

MODEL: 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO. S1.00029

SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
1	2	D	11414-XX	E

PRODUCT NO. 11414-XX

REFERENCE DESIGNATORS NOT USED

REFERENCE DESIGNATORS LAST USED

REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	MFG	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J		H		G		F		E	4063	D	4025	C	29.8	B		A	3031							

PRODUCT NO. 11411-XX

PRODUCT NO. 11411-XX DEVELOPMENT REV. D6

HOME SENS LED — TO P4-11 (X) — K4 150 1/2W — J4 .1 10V — K6 10 25V — H6 2.7µH — + 5V — K10 10K — K9 100K — TP2

HOME SENSOR A — P4-5 (Y) — K11 22K — J9 558

HOME SENSOR B — P4-6 (20) — K12 22K — J14 10K — J15 100K — J9 558 — TP3

J16 1K — J17 1K — K13 .1µf 50V — -15V

K8 1K — K15 558 — TP1 — J19 2.7K — J20 — J21 — +5V — J18 1K — H30 380 — F40 .1 50V — F41 22K

+15V — K25 1% — K27 1K 1% — K26 100K 1% — J8 .1µf 50V — J24 2.7K — J22 — J23 — TP4

+ HEADS OVER DISK — (3) MO5-3

+ HEADS OVER TRACKS — (17) MO9-17, MO5-17 — J30 7400 — H38 836 — K45 .001 — H46

+ ZERO TRACK SENSING — (U) MO9-18 — K43 .001 — +5V — E38 10K

+ FILE READY — R/W-CB VIA P6-31 & P5-23 (J)

- SEEK INCOMPLETE OUTPUT — (C) I/O2-11, I/O1-M VIA P5-6 — E42 858 — B54 27K — D42 380 — A52 4.7K — A51 47K — -15V

+15V — H2 27µH — K2 10 25V — E37 5.6K — F45 — F47 2.2 35V — H50 16K — THRESHOLD AT +8.5V — K49 10K — F43 — F42 5.6K

HS-CB VIA P2-5 (R) CURRENT DETECTOR (LOW FOR "HIGH CURRENT") — E53 2N3643 — F50 .1 50V

+24V — H51 10K — H54 2.4K 1/2W — H48 5.6K — F49 68K — F53 2N3643 — K54 — K48 — B56 5.6K — -24V — D53 2N3644 — K53 — B55 10K — K51 2.4K 1/2W — -24V — K50 5.6K

I/O2-20 VIA P5-18 (N) -RESTORE — I/O2-X VIA P5-15 (K) -STROBE — D42 380 — K47 — - CLEAR SEEK INCOMPLETE

SEEK INCOMPLETE FLIP-FLOP

SERVO DISABLE — (15) HS-CB VIA P2-10 — (GND ± 0.8 V FOR "DISABLE")

+5V — E56 4.7K — A55 2N3643

+ INITIAL RESET

E42 858 — +5V — F44 10K — - INITIAL RESET — (9) MO5-9, MO1-K, MO8-10, I/O1-V VIA P5-10, I/O2-12 VIA P5-10, R/W-CB VIA P6-17 — MO2-K, MO9-8

(6) (F) — D4 1µH — H4 10 25V — .1 10V — B29 E50 K41 — +5V

+15V — B8 13V 20% — A8 — A7 6.8K 1/2W — A5 10K 1/2W — B6 13V 2% — B4 2.7K — A6 — HS-CB VIA P2-4 (16) +24V (CKT)

+5V — B10 5V 20% — A10 — A9 2.2K 1/2W — A13 — +15V — A11 27K — B14 2N3643 — B17 2N3643

HS-CB VIA P2-16 (8) -24V (CKT) — A25 13V 20% — A23 5V — A15 4.7K — A18 — A19 1K — A16 — A17 1K — A12 100K — A21 13V 2%

+15V — A14 5.6K — A28 — +24V — A29 27K — A31 — A30 — A34 12 20V — +15V — B37 27K — B38 27K — B39 — B32 2N3643 — D50 .1 10V

+ VOLTAGE ERROR — A36 5.6K — A27 1 35V

A41 — A38 10K — +24V — A48 2.4K 1/2W — B50 27K — D42 380

POS. SPINDLE DRIVE CUT OFF — (GND FOR "CUT OFF") — (4) MO1-U

A39 5.6K — B43 2N3643 — A37 5.6K — A40 68K — -24V — B52 5.6K — A43 5.6K — B47 2N3644 — A46 10K — A44 2.4K 1/2W — -24V — B40 — TP5 — E40

NEG. SPINDLE DRIVE CUT OFF — (GND FOR "CUT OFF") — (5) MO1-V

- SELECTED INDEX MARK OUTPUT — (UNSEPARATED MARKS IF SECTOR COUNTER OPTION) — (11) I/O1-R VIA P5-19

+ SEL SECTOR/INDEX — (SELECTED SECTOR MARKS IF SECTOR COUNTER OPTION) — (12) MO5-11

P4-3 (V) UPPER INDEX MARK XDUCER — H8 .0033 — K21 3.3K — H20 709 — F23 3.3K — F22 — F21 — +5V — F20 — E8 — A1 Q — A2 74121 — B Q — 40±10µs — F23 100 — F24 4.7K — P4-14 (18) GND

DISK SELECT — I/O1-P VIA P5-25 (S) — LOW FOR "UPPER DISK" — H27 — F27 — E28 — H30 380

I/O3-Y VIA P5-29 (D) + UPPER SECTOR MARK IN — H38 836 — F30 — F32 — F31 — E30 7400 — F33 — F34 — F35 — D30 858 — D26 10K — D25 — D24 .47µH — TP6 — F29

P4-4 (W) LOWER INDEX MARK XDUCER — H10 .0033 — K22 3.3K — H12 709 — F17 3.3K — F13 — F14 — +5V — F12 — E10 — A1 Q — A2 74121 — B Q — 40±10µs — F15 100 — F16 4.7K — P4-13 (19) GND

D30 858 — D23 10K — D22 — D21 .47µH — +15V — - LOWER INDEX MARK OUTPUT — (LOW FOR "INDEX") — (E) I/O3-V VIA P5-27

+ SECTOR MARK LOWER — (HIGH FOR "SECTOR") — (M) I/O3-W VIA P5-17 — F28 47

+ INDEX MARK LOWER — (T) MO5-7

F38 — F39 — K38 14K 10% — J50 — 5% 200V — K30 — A1 Q — A2 74121 — B Q — K40 — SELECT FOR O.S. PERIOD OF 850 ±50µs — +5V — K42 4.7K

J30 7400 — J39 — -LOWER INDEX MARK — E30 7400 — J30 7400 — -LOWER SECTOR MARK — J28 — H30 380

L — 10 — D2 27µH — A2 10 25V — -15V — I — 22 — A — Z

NOTES:
UNLESS OTHERWISE SPECIFIED
1 ALL RESISTORS ARE 5% 1/4W
2 ALL 1% RESISTORS ARE 1/8W
3 ALL DIODES ARE IN4454
4 ALL RESISTORS ARE IN OHMS
5 ALL CAPACITORS ARE IN µf

OPTIONAL ASSY NO.	REVLEVEL	LAST ECO	DESCRIPTION	COMPONENTS F29 F31 F35	F30 F32 F34	E8,E10	F12,F20
11411-00	L	3824	40µs INDEX PULSE NO SECTOR COUNTER	10	—	4700PF	12K
11411-01	L	3824	40µs INDEX PULSE SECTOR COUNTER	—	10	4700PF	12K
11411-02	C	3824	5µs INDEX PULSE, NO SECTOR COUNTER	10	—	1000PF	7.5K
11411-03	C	3824	5µs INDEX PULSE, SECTOR COUNTER	—	10	1000PF	7.5K

SR M06

Diablo Systems Incorporated

TITLE: SENSOR CIRCUITS SR-CB SCHEMATIC

MODEL 40 — PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED. — SYSTEM LOGIC NO. SL00032 — SHEET 1 TOTAL SHEETS 2 — SIZE D — PRODUCT NO. 11411-XX — REV L

REV	Q	P	O	N	M	L	K	J	H
E.C.O. NO.						3824	3778	3665	2973

MFG — DATE — ENG — DATE — CHECKED — DATE — DRAWN — DATE

PRODUCT NO. 11411-XX — REFERENCE DESIGNATORS — REFERENCE DESIGNATORS

PRODUCT NO 11402-XX

PRODUCT NO 11402-XX | DEVELOPMENT REV D2

M08 -N (N) -POSITION TERM [6]
M04 -T (17) TEMP COMP VOLTAGE
M08 -20 (20) -SPEED INCR NO. 7 [6]
M08 -K (K) -SPEED INCR NO. 6 [6]
M08 -8 (8) -SPEED INCR NO. 5 [6]
M08 -12 (12) -SPEED INCR NO. 4 [6]
M08 -M (M) -SPEED INCR NO. 3 [6]
M08 -9 (9) -SPEED INCR NO. 2 [6]
M08 -J (J) -SPEED INCR NO. 1 [6]
M08 -11 (11) -MINIMUM SPEED [6]
M08 -16 (16) -04 [6]
M08 -S (S) -PICK $\overline{B}$ (LOW IF "PICK")
M08 -19 (19) -02 [6]
M08 -V (V) -PICK B (LOW IF "PICK")
M08 -T (T) -03 [6]
M08 -15 (15) -PICK $\overline{A}$ (LOW IF "PICK")
M08 -W (W) -01 [6]
M08 -18 (18) -PICK A (LOW IF "PICK")

+ REFERENCE VOLTAGE

P4-2 (R) TRANSDUCER SIGNAL CHANNEL—A
P4-15 (14) TRANSDUCER SIGNAL CHANNEL—A
M02-H (H) DEMOD SIGNAL (480 KHz SQUARE WAVE)
P4-1 (B) TRANSDUCER SIGNAL CHANNEL—B
P4-1 (2) TRANSDUCER SIGNAL CHANNEL—B

+ SERVO DRIVE SIGNAL (+ FOR FORWARD) (X) HS-CB VIA P2-8

SERVO LOGIC CONTROL LEVEL "D" (21) M09-21 M08-21
SERVO LOGIC CONTROL LEVEL "C" (Y) M09-Y M08-Y

NOTES:
UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 5%, 1/4W.
2. ALL 1% RESISTORS ARE 1/8W.
3. ALL RESISTORS ARE IN OHMS.
4. ALL DIODES ARE IN4454.
5. ALL CAPACITORS ARE IN µf.
6. LOW TO TURN THE FET "ON".
7. SELECTED ACCORDING TO TEST SPECIFICATION ; A30, A31, A41, A42, B13, B41, B42, E13, E30, E29, E41, E42, F41, F42.
8. OPTIONAL FEATURES:
   - 8.1 FOR 100TPI OPERATION; 11402-00 E37 AND E38 COMPONENTS ARE NOT USED.
   - 8.2 FOR 200TPI OPERATION; 11402-20 AS INDICATED.
9. E48-GND=PINS 7&8, J48-GND=PINS 7&8.

SO M07

Diablo Systems Incorporated

TITLE: SERVO CIRCUIT SO-CB SCHEMATIC

MODEL 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO. SL 00033

SHEET 1 TOTAL SHEETS 2 SIZE D PRODUCT NO. 11402-XX REV A

PRODUCT NO 11402-XX | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED

REV	E.C.O. NO.	MFG	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J									
H									
G									
F									
E	2970								
D									
C									
B									
A									

M08-N (N) -POS TERM [6]
M04-T (17) TEMP COMP VOLTAGE
M08-20 (20) -SPEED INCR NO. 7 [6]
M08-K (K) -SPEED INCREMENT 6 [6]
M08-8 (8) 5 [6]
M08-12 (12) 4 [6]
M08-M (M) 3 [6]
M08-9 (9) 2 [6]
M08-J (J) -SPEED INCREMENT 1 [6]
M08-11 (11) -MINIMUM SPEED [6]
M08-16 (16) -Ø4 [6]
M08-S (S) -PICK D [6]
M08-19 (19) -Ø2 [6]
M08-V (V) -PICK B [6]
M08-T (T) -Ø3 [6]
M08-15 (15) -PICK C [6]
M08-W (W) -Ø1 [6]
M08-18 (18) -PICK A [6]

TP14 +15V 1,16 B47 1M B47 6.2K D48 E38 [8] 1.21M, 1/4W, 1% E37 .47,50V

J8 1K J7 1M B47 1M B47 6.2K B47 1M B47 6.2K B47 1M B47 6.2K B47 1M B47 6.2K B47 1M A58 1M B47 6.2K B47 1M B47 6.2K B47 1M A57 1M B47 6.2K

D48 D48 D48 D48 D48 D48 D48 D48

J9 P1086E A48 A48 A48 A48 A48 A48 A48 A48

D45 1.30M 1/4W, 1%
A51 130K, 1%
A45 182K, 1%
A50 324K, 1%
A46 511K, 1%
D50 681K, 1%
D46 909K, 1/4W, 1%
D51 1.10M 1/4W, 1%

+ REFERENCE VOLTAGE

TP3

H47 6.2K ×8 H47 1M ×8 H55 510pf H56 510pf H57 1M H58 510pf J46 510pf J45 510pf J56 510pf J44 510pf F43 510pf

F48 ×8 H48 ×8

+15V J11 1K J12 1.5K 1% J14 1.5K 1% J13 47 J16 558 J10 10K 1%

J23 249K 1% J21 .001 J16 558 TP5 J22 200 J24 18K

+ SERVO DRIVE SIGNAL (+ FOR FORWARD) (X) HS-CB VIA P2-8

F1 27uH J1 10 25V
D3 1uH F3 10 25V
D1 27uH A1 10 25V

NOTES:
UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 5%, 1/4W.
2. ALL 1% RESISTORS ARE 1/8W.
3. ALL RESISTORS ARE IN OHMS.
4. ALL DIODES ARE IN4454.
5. ALL CAPACITORS ARE IN µf.
6. LOW TO TURN THE FET "ON".
7. SELECTED ACCORDING TO TEST SPECIFICATION; A30, A31, A41, A42, B13, B41, B42, E13, E29, E30, E41, E42, F41, F42.
8. OPTIONAL FEATURES:
   8.1 FOR 100 TPI OPERATION; 11633-00 E37 AND E38 COMPONENTS ARE NOT USED.
   8.2 FOR 200 TPI OPERATION; 11633-20 AS INDICATED.
9. E48-GND: PINS 7 & 8
   J48-GND: PINS 7 & 8
10. USE MOTOROLA MC1496L (DIABLO PART NO. 10320) ONLY FOR 200 TPI OPERATION.

P4-2 (R) CHANNEL-A1 (TRANSDUCER SIGNAL)
P4-15 (14) CHANNEL-A2 (TRANSDUCER SIGNAL)

E5 .001 E8 100pf F5 620 F6 620 F8 100pf F9 4.7K F10 4.7K F12 733C E9 6.2V E11 12 E26 .1 50V E6 330 1/2W E8 330 1/2W E25 1K GAIN ADJ F23 1496 [10] -CARRIER +CARRIER +SIG IN -SIG IN +OUTPUT -OUTPUT E28 13K E29 E30 E31 4.99K 1% E33 4.99K 1% E34 .0056 -6.2V TP2 TP4 E18 .0047 E19 .0047 E20 750pf E21 620 E27 620 E23 12 E21 2.2K E13 E14 510 E16 5% J27 J26 B5 330 1/2W B6 330 1/2W TP9 TP8

P4-14 (B) CHANNEL-B1 (TRANSDUCER SIGNAL)
P4-1 (2) CHANNEL-B2

A3 .001 A5 620 A6 620 A8 100pf A9 4.7K A10 4.7K A13 733C A29 .1 50V E22 1.2K B24 1K GAIN ADJ A23 1496 [10] -CARRIER +CARRIER +SIG IN -SIG IN +OUTPUT -OUTPUT B26 13K A30 A31 A34 4.99K 1% A32 4.99K 1% A35 .0056 +6.2V TP6 TP1 B21 .0047 A20 750pf B22 620 B19 620 B17 .0047 B13 B14 510 B16 5% B27 B23 B10 12 B8 6.2V TP7 TP10

M02-H (H) DEMOD SIGNAL (480 KHz SQUARE WAVE) B30 .0047 B28 620

F39 26.1K 1% F33 26.1K 1% F35 26.1K 1% F37 26.1K 1% F38 26.1K 1% F42 F40 422K 1% F41 F34 558 A F31 422K 1% E42 E40 422K 1% E41 E36 422K 1% TP15 TP13 TP19 J48 20K 1% J48 2K 1% J48 20K 1% J58 .01 1% [9]

B42 B39 26.1K B32 26.1K B37 26.1K A38 26.1K A42 B40 422K 1% B41 B34 558 B B31 422K 1% A41 A39 422K 1% TP18 TP16 TP17 E43 5.11K 1% B43 5.11K 1% E48 20K 1% F44 5.11K 1% F45 .01 1% [9] A43 5.11K 1% D58 .01 1% [9]

J40 558 J31 1.5K J32 560K H41 J33 5.6K J29 TP11 J30 CONTROL LEVEL "D" (21) M09-21 M08-21

J40 558 J36 1.5K J37 560K J38 5.6K J39 J35 TP12 J34 CONTROL LEVEL "C" (Y) M09-Y M08-Y

SO M07

Diablo Systems Incorporated

TITLE: SERVO CIRCUIT SO-CB SCHEMATIC
MODEL 40
PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.
SYSTEM LOGIC NO SL00034
SHEET 1 TOTAL SHEETS 2 SIZE D PRODUCT NO. 11633-XX REV A

A 4196
A 4122
A 2968

PRODUCT NO. 11633-XX | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED

REV J E.C.O. NO. | REV H E.C.O. NO. | REV G E.C.O. NO. | REV F E.C.O. NO. | REV E E.C.O. NO. | REV D E.C.O. NO. | REV C E.C.O. NO. | REV B E.C.O. NO. | REV A E.C.O. NO. | MFG | DATE | ENG | DATE | CHECKED | DATE | DRAWN | DATE

PRODUCT NO. 11407-XX

PRODUCT NO. 11407-XX DEVELOPMENT REV. D6

M09 B (B) SUM BIT "256" (128 FOR 100TPI) (HIGH IF "BINARY 1")

M09-C (C) SUM BIT "128" (64 FOR 100 TPI)

M09-3 (3) SUM BIT "64" (32 FOR 100TPI)

M09-2 (2) SUM BIT "32" (16 FOR 100TPI)

M09-19 (U) SUM BIT "16" (8 FOR 100 TPI)

M09-20 (17) SUM BIT "8" (4 FOR 100 TPI)

M09-Z (Z) SUM BIT "4" (2 FOR 100 TPI)

M09-X (X) SUM BIT "2" (1 FOR 100TPI)

M09-V (14) SUM BIT "1" (0 FOR 100 TPI) (HIGH IF "BINARY 1")

M09-E (E) DIRECTION CONTROL (LOW IF "FORWARD")

M09-5 (5) BIT 1 (HIGH IF "SET")

M09-U (BLK) (R) BIT2 (HIGH IF "SET")

M07-21 (21) CONTROL LEVEL D

M07-Y (Y) CONTROL LEVEL C

M01-Y (7) DISK PACK SAFETY SW (LOW IF "D.P. UNLOCKED")

M09-4 (4) + RETRACT SPEED

R/W-CB VIA P6-31 & P5-23 (P) + FILE READY

M06-14 (13) -SEEK INCOMPLETE

B3 74157 8122 — FWD — REV — SELECT — STROBE

H3 74157 8122 — FWD — REV — SELECT — STROBE

F39 74157 8122 — SELECT — STROBE

H39 74157 8122 — SELECT — STROBE

+5V

J54 (200 TPI) 10 J55 (100 TPI)

(200 TPI) J56 10 J57 (100 TPI)

B25 4.7K

D25

D1 1μh

F1 10 25V

.1 10V

A13, A25, A37, A49, E13, E25, E37, E49, J37, J50

J51 20K

H49 2.2 35V

B23 470

E42 10K

E39 4.7K

E45 4.7K

J53 1K

F13 100pf

E51 1/4W 5% .47 50V

E52 39.2K 1%

E53

E15 10

SETTLING OS-1 3.5MS ±.35MS

SETTLING OS-2 10MS ±2.5MS

CARRIAGE POSITIONING FF-2

SEEK FF

- SPEED INCREMENT 7 (20) M07-20
6 (K) M07-K
5 (8) M07-8
4 (12) M07-12
3 (M) M07-M
2 (9) M07-9
- SPEED INCREMENT 1 (J) M07-J
- MINIMUM SPEED (11) M07-11
- COUNTER INTERLOCK (A) M09-J
- POSITION TERM (N) M07-N
- PICK A (18) M07-18
B (V) M07-V
$\bar{A}$ (15) M07-15
- PICK $\bar{B}$ (S) M07-S
- Ø2 (19) M07-19
- Ø1 (W) M07-W
- Ø4 (16) M07-16
- Ø3 (T) M07-T
+ INPUT INHIBIT (D) M09-D
- READY TO S/R/W OUTPUT (L) I/02-V VIA P5-11
(H) R/W-CB VIA P5-5 & P6-14 I/01-S VIA P5-5 MC 9-H

SPARES:

NOTES:
UNLESS OTHERWISE SPECIFIED
1 ALL 1% RESISTORS ARE 1/8W.
2 ALL 5% RESISTORS ARE 1/4W.
3 ALL DIODES ARE IN4454.
4 ALL RESISTORS ARE IN OHMS.
5 ALL CAPACITORS ARE IN μf.

[6] 1. FOR 100 TPI OPERATION JUMPER IN J55 & J57
2. FOR 200 TPI OPERATION JUMPER IN J54 & J56

AL2 M08

Diablo Systems Incorporated

TITLE: ADDRESS LOGIC 2 AL 2 (200 TPI & 100 TPI)

MODEL: 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED. SYSTEM LOGIC NO. SL00035

SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
1	2	D	11407-XX	G

PRODUCT NO. 11407-XX | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED

REV	J	H	G	F	E	D	C	B	A
E.C.O. NO.			3594						
DATE									

MFG | ENG | CHECKED | DRAWN

PRODUCT NO. 11404-XX

PRODUCT NO. 11404 XX | DEVELOPMENT REV. D5

SH2 F10 B39-6 — − TRACK 1

SH2 H7 H27-3 — + BIT NO. 1

SH2 C4 B27-12 — − DIRECTION ENABLE

SH2 E14 E15-2 — −RESTORE COMMAND

M05-S (S) — + SPINDLE DRIVE ON

M06-17 (17) — + HEADS OVER TRACKS

M06-U (18) — + ZERO TRACK SENSING

M05-B (A) — + HEADS NOT RETRACTED

SH2 C11 H39-11 — − INITIAL RESET

M07-Y (Y) — + CONTROL LEVEL-C

M07-21 (21) — + CONTROL LEVEL-D

M08-A (J) — −COUNTER INTERLOCK

SET ON LEADING EDGE OF "SPINDLE DRIVE ON" OR RESTORE IS EXECUTED

1μs NEGATIVE PULSE ON LEADING EDGE OF "SPINDLE DRIVE ON"

+ SPINDLE DRIVE OFF

CARRIAGE POSITIONING FF-1

END AROUND CARRY

÷ CARRY BIT 1 → SH2 H5 J15-13

(SUM BIT "0" FOR 100 TPI)

+ SUM BIT 1 (V) → M08-14

− DIRECTION CONTROL (HIGH TO RETRACT) (E) → M08-E

+ RETRACT SPEED → SH2 C14 F39-5

+ RETRACT SPEED (HIGH TO "RETRACT") (4) → M08-4

− RETRACT HEADS

− COUNT UP FORWARD → SH2 H8 H27-5

SPARES:

− COUNTER INTERLOCK → SH2 C6 D15-5

− COUNT DOWN REVERSE → SH2 H8 H27-4

NOTES:
UNLESS OTHERWISE SPECIFIED
1 ALL RESISTORS ARE 1/4W ± 5%
2 ALL 1% RESISTORS ARE 1/8W
3 ALL DIODES ARE IN4454
4 ALL RESISTORS ARE IN OHMS
5 ALL CAPACITORS ARE IN μf
[6] SEE CHART FOR VALUES AND TIME DELAYS.

REV.	PART NO.	DESCRIPTION	REMARKS TIME DELAY H39A	REMARKS TIME DELAY H39B	CAPACITORS J39	CAPACITORS J44	RESISTORS J41	RESISTORS J45	JUMPER D3
F	11404-00	PCB ASSY-ADDRESS LOGIC I 100TPI	500 NS ±150NS	1 μS ±.3μS	.270 pf	300pf	5.1K	10K	
D	11404-01	PCB ASSY-ADDRESS LOGIC I 100TPI SERIES 30 COMPAT	35 μS ±10 μS	5 μS ±2 μS	.0033	.001	33 K	15K	
F	11404-20	PCB ASSY-ADDRESS LOGIC I 200TPI	500NS ±150NS	1 μS ±.3μS	270 pf	300 pf	5.1K	10K	22AWG
D	11404-21	PCB ASSY-ADDRESS LOGIC I 200TPI SERIES 30 COMPAT	35 μS ±10 μS	5 μS ±2 μS	.0033	.001	33K	15K	22 AWG

ALI M09

Diablo Systems Incorporated

TITLE: ADDRESS LOGIC I
ALI-CB
MODEL 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED

SYSTEM LOGIC NO. SL00037

SHEET 1 | TOTAL SHEETS 3 | SIZE D | PRODUCT NO. 11404-XX | REV F

PRODUCT NO 11404-XX | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED

REV J E.C.O. NO. | REV H E.C.O. NO. | REV G E.C.O. NO. F 3813 | REV E E.C.O. NO. | REV D E.C.O. NO. 3553 | REV C E.C.O. NO 3814 | REV B E.C.O. NO. | REV A E.C.O. NO | MFG | DATE | ENG | DATE | CHECKED | DATE | DRAWN | DATE

PRODUCT NO. 11404-XX

SHI F5 F15-11 → -COUNT UP FORWARD

SHI C5 F15-8 → -COUNT DOWN REVERSE

M08-D (D) +INPUT INHIBIT

I/02-19 P5-16 (M) -BIT 128 (64 FOR 100 TPI)

I/02-17 P5-12 (10) -BIT 64 (32 FOR 100TPI)

I/02-W P5-13 (11) -BIT 32 (16 FOR 100TPI)

I/02-U P5-24 (14) -BIT 16 (8 FOR 100TPI)

VIA CABLE P5

E3 (NOT USED)

I/02-Y P5-20 (13) -BIT 8 (4 FOR 100TPI)

I/02-16 P5-26 (R) -BIT 4 (2 FOR 100TPI)

I/02-21 P5-22 (P) -BIT 2 (1 FOR 100TPI)

I/02-S P5-9 (K) -BIT 1

NOT USED FOR 100 TPI

I/02-18 P5-14 (L) -BIT 256 (128 FOR 100TPI)

I/02-X P5-15 (12) -STROBE

I/02-20 P5-18 (N) -RESTORE

M08-H (H) -READY TO S/R/W

-RESTORE COMMAND

M06-9 (8) -INITIAL RESET

SHI D27-8 +RETRACT SPEED

SHI D8 F13-10 -COUNTER INTERLOCK

SHI L6 E27-8 +CARRY BIT 1

B15 7475 SEEK ADDRESS REGISTER

H15 7475

LOW IF ILLEGAL ADDRESS (> 203)

J27

H27 74193

A27

TRACK COUNTER

F27 74193

(NO SIGNAL FOR 100 TPI)

+ TRACK 256 (HIGH IF "ADDR>256") (9) P5-7 P6-6 R/W-CB

A15 7483

+ SUM BIT 128 (C) M08-C

+ SUM BIT 64 (3) M08-3

+ SUM BIT 32 (2) M08-2

+ SUM BIT 256 (HIGH IF BINARY 1) (B) M08-B

(NO 256 W/100TPI)

SUBTRACTOR

J15 7483

+ BIT NO. 1 SHI K12 J51-2

+ BIT NO. 1 (5) M08-5

+ SUM BIT 8 (20) M08-17

+ SUM BIT 4 (Z) M08-Z

+ SUM BIT 2 (X) M08-X

+ SUM BIT 16 (19) M08-U

+ BIT NO. 2 (HIGH IF "SET") (U) M08-R

- TRACK 1 → SHI K12 J51-1

-ADDRESS ACKNOWLEDGE OUTPUT (T) I/02-2 P5-31

-LOGICAL ADDRESS INTERLOCK OUTPUT (16) I/02-14 P5-32

- INITIAL RESET → SHI G9 E39-8

- DIRECTION ENABLE → SHI H9 B27-11

-RESTORE COMMAND → SHI J11 A3-1

ALI M09

Diablo Systems Incorporated

TITLE: ADDRESS LOGIC I
ALI-CB

MODEL: 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO. SL00038

SHEET 2 TOTAL SHEETS 3 SIZE D PRODUCT NO. 11404-XX REV F

REV J E.C.O. NO. | REV H E.C.O. NO. | REV G E.C.O. NO. F3813 | REV E E.C.O. NO. D3553 | REV C E.C.O. NO. 3814 | REV B E.C.O. NO. | REV A E.C.O. NO.

APP'D DATE | ENG DATE | CHECKED DATE | DRAWN DATE

PRODUCT NO. 11486-XX

PRODUCT NO. 11486-XX DEVELOPMENT REV. D6

M09-9 VIAP5-7 (6) +TRACK 256

(21)

(22) WRITE DATA

1/01-9 (23)

1/01-P (25) DISK SELECT (LOW FOR "UPPER")

1/01-20 (24) HEAD SELECT (LOW FOR "UPPER")

SH2-F7-H9-8 — WRITE PROTECT

1/01-U (15) -WRITE GATE

1/01-17 (18) -ERASE GATE

M06-9 VIA P5-10 (17) -INITIAL RESET

M05-J VIA P5-30 (30) +SPINDLE ENABLE

1/01-18 (20) -READ GATE

M09-H VIA P5-5 (14) -READY TO S/R/W

M05-R VIA P5-28 (11) +HEADS LOADED

1/01-2 (19) -WRITE PROTECT INPUT

(3) (NOT USED)

SEE NOTE 7

UPPER HEAD / UPPER DISK / LOWER HEAD / LOWER DISK

HEAD BUS A → SH2-J16-B108

HEAD BUS B → SH2-J16-B109

ERASE BUS

-DISK SELECT → SH2-E13-D9-12

+ DISK SELECT → SH2-F13-D9-1

(NOT USED) (10)

+ WRITE FAULT (27) 1/01-11

- WRITE CHECK INDICATOR (10) P8 PANEL VIA P8A-10

+ VOLTAGE CHECK (2) 1/01-14

- FILE READY OUTPUT (28) 1/01-21 1/03-21

- FILE READY INDICATOR (7) P8 PANEL VIA P8A-7

- READ ENABLE → SH2-J5-J39-3

+ FILE READY (31) 1/02-P M08-P M06-J VIA P5-23 1/01-12 (HIGH FOR "READY")

- SPINDLE ENABLE → SH2-F13-D28-1

+ WRITE PROTECT INPUT → SH2-F13-D9-2

(HIGH FOR "WRITE FAULT")

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE ± 5%, 1/4 W.
2. ALL 1% RESISTORS ARE 1/8 W.
3. ALL DIODES ARE IN4454.
4. FOR WRITE PROTECT OPTIONS, FOR UPPER OR LOWER DISK, INSTALL 10Ω RESISTOR IN E11 OR E10. FOR WRITE PROTECT ON BOTH DISKS, OMIT E10 & E11 RESISTOR.
5. ALL RESISTORS ARE IN OHMS.
6. ALL CAPACITORS ARE IN μf.
7. RESISTORS B71 & J43 ARE TEST SELECT.

PART NO.	E.C.O.	REV.
11486-00	4860	L
11486-02	4860	K
11486-10	4860	C

PART NO.	E.C.O.	REV.
11486-12	4860	F
11486-20	4081	G
11486-30	4081	B

L 4860 K 4081

REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.
J	3725	H	3692	G	3856	F		E	3361	D	3691	C		B	3793	A	

MFG	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE

PRODUCT NO. 11486-XX | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED

R/W

Diablo Systems Incorporated
Hayward, California 94545

TITLE: READ WRITE AMPLIFIER R/W

MODEL 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED. SYSTEM LOGIC NO. SL00039

SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
1	9	D	11486-XX	L

PRODUCT NO. 11486-XX

PRODUCT NO. 11486-XX DEVELOPMENT REV. D6

SHI-K6-B107 → HEAD BUS A

SHI-J6-B105 → HEAD BUS B

SHI-C6-D9-6 → -READ ENABLE

SHI-H12-E66-4 → +DISK SELECT

SHI-C6-D56-2 → -SPINDLE ENABLE

SHI-G12-E66-9 → -DISK SELECT

SHI-C15-D56-3 → +WRITE PROTECT INPUT

PANEL VIA P8-6 (6) → WRITE PROTECT SWITCH +24 TO RESET W.P.

PANEL VIA P8-8 (8) → -WRITE PROTECT DISABLE

4 WRITE PROTECTED — LOWER ONLY E10 — UPPER ONLY E11

J43 SEE NOTE 7

-READ DATA & CLOCK → (32) 1/05-21 (26)

WRITE PROTECT STATUS (LOW FOR "PROTECTED") → (29) 1/01-Y

-WRITE PROTECT → SHI-F15-D47-2

WRITE PROTECT INDICATOR (LOW FOR "PROTECTED") → (9) P8 PANEL VIA P8A9 (12) (16)

(1) (33) (34) GND

SPARES

PART NO		DESCRIPTION	REMARKS	CAPACITOR J94 J104	CAPACITOR E105	CAPACITOR H95 H105	CAPACITOR H94, H104, J99	CAPACITOR E94	CHOKE H96, H106	CHOKE W93, H97 H100, H108	RESISTOR B75	RESISTOR B92, B93	RESISTOR J102	RESISTOR E108	WIRE	WIRE
11486-00	100 TPI	2400 RPM, SINGLE SHOT SEPARATOR		.022µf 50V	510pf 500V	39pf 500V	120pf 500V	150pf 500V	4.7µH	22µH	165 1%, 1/2W	470 5%, 1/4W	620 5%, 1/4W	1.3K 5%, 1/4W		WIRE 20AWG
11486-02		1500 RPM, SINGLE SHOT SEPARATOR		.033µf 50V	.001µf 200V	62pf 500V	180pf 500V	240pf 500V	6.8µH	33µH	165 1%, 1/2W	430 5%, 1/4W	620 5%, 1/4W	1.3K 5%, 1/4W		WIRE 20AWG
11486-10		2400 RPM, VFO SEPARATOR		.022µf 50V	510 pf 500V	39pf 500V	120pf 500V	150pf 500V	4.7µH	22µH	165 1%, 1/2W	430 5%, 1/4W	620 5%, 1/4W	1.3K 5%, 1/4W		
11486-12		1500 RPM, VFO SEPARATOR		.033µf 50V	.001µf 200V	62pf 500V	180 pf 500V	240pf 500V	6.8µH	33µH	165 1%, 1/2W	430 5%, 1/4W	620 5%, 1/4W	1.3K 5%, 1/4W		
11486-20	200 TPI	2400 RPM, SINGLE SHOT SEPARATOR		.022µf 50V	.001µf 200V	39pf 500V	120 pf 500V	150pf 500V	4.7µH	22µH	86.6 1%, 1/2W	330 5%, 1/4W	330 5%, 1/4W	1.5K 5%, 1/4W		WIRE 20AWG
11486-30		2400 RPM, VFO SEPARATOR		.022µf 50V	.001µf 200V	39pf 500V	120 pf 500V	150pf 500V	4.7µH	22µH	86.6 1%, 1/2W	330 5%, 1/4W	330 5%, 1/4W	1.5K 5%, 1/4W		

R/W

Diablo Systems Incorporated
Hayward, California 94545

TITLE: READ WRITE AMPLIFIER R/W

MODEL 40

PROPRIETARY INFORMATION — UNAUTHORIZED DISCLOSURE OR USE PROHIBITED. CONTROL LOAD NO. SL00040

SHEET 2 TOTAL SHEETS 9 SIZE D PRODUCT NO. 11486-XX REV L

L4860 K4081

REV	E.C.O. NO.	DATE
J	3725	
H	3692	
G	3856	
F		
E	3361	
D	3691	
C		
B	3793	
A		

BY | DATE | CHKD | DATE | DRAWN | DATE

PRODUCT NO. 11486-XX | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED

PRODUCT NO. 11418 | DEVELOPMENT REV. D3

PII-C&F +24V PWR

PII-A&D -24V PWR

MOI-7 PIA-6 PHASE 1B

MOI-4 PIA-4 PHASE 1A

PII-P MOTHER CB PIA-1

PII-R MOTHER-CB PIA-16

PIA-8 GND

MOI-C PIA-14 +SPINDLE MOTOR CURRENT CONTROL (GND FOR "FULL" CURRENT)

MOI-3 PIA-3 -SPINDLE MOTOR CURRENT CONTROL (GND FOR "FULL" CURRENT)

MOI-9 PIA-9 PHASE 2B

PII-J&M MOTHER-CB P2A-1 +5V

P2A-2

MOI-J PIA-7 PHASE 2A

SPINDLE DRIVE MOTOR WINDING Ø1

SPINDLE DRIVE MOTOR WINDING Ø2

SPEED SENSE "A" PIA-12 MOI-E

SPEED SENSE "B" PIA-5 MOI-12

PII-N +24V(CKT)

PII-L -24V(CKT)

+15V P2A-6 MOTHER-CB

P2A-11 MOTHER-CB

-15V P2A-3 MOTHER-CB

P2A-14 MOTHER-CB

P2A-8 MO6-8

P2A-16 MO6-16

NOTES:
UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W ± 5%.
2. ALL 1% RESISTORS ARE 1/8W.
3. ALL DIODES ARE A15A.
4. CURRENT LIMITING RESISTORS MOUNTED ON SIDE OF BOWL.
5. ALL RESISTORS ARE IN OHMS.
6. ALL CAPACITORS ARE IN µf.
7. RESISTOR B93 IS SELECTED TO OBTAIN +15V ±0.1V AT P2A-6. THEN RESISTOR B100 IS SELECTED TO OBTAIN -15V ± 0.1V AT P2A-3.

HS

Diablo Systems Incorporated
Hayward, California 94545

TITLE: HEAT SINK CIRCUIT BOARD HS-CB SCHEMATIC

MODEL 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO. SL00043

PRODUCT NO. 11418 | REV P

SHEET 1 | TOTAL SHEETS 2 | SIZE D

REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	MFG	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
S		R		Q		P	3936	N	3607	M	3560	L	2976	K	2923	J	2908								

PRODUCT NO. 11418 | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED

MO6-15 P2A-10 SERVO DISABLE
(GND ±0.8V FOR DISABLE)
MP-A
B A
SERVO RELEASE SWITCH
P2A-7 GND
MP-B

MO7 X P2A-8 +SERVO DRIVE SIGNAL
(+ FOR FORWARD)
B83 4.02K 1%
B86 3.9K
B82 558
B81 .1 50V
B85 42.2K 1%
A86 1K
A80 10.2K 1%
B78 2.2K
B77 510pf
B87 .1 50V
A84 2.7M
A82 510pf
+15V
-15V

+24(CKT)
B66 1K
A68 TIP-32A
B72 2N5881
B71
B70 1K 1/2W
B76 2N3643
A72 510pf
A73 10C
E75 680 1/2W
A75 300 1/2W
E76 51pf
D76 2N3644
E71 510pf
D73 100A
D71 1K 1/2W
E68 TIP-31A
E72 2N5879
E64 1K
E73
-24V(CKT)
E78 1K 1%
D80 .2 1% 10W CURRENT SENSE RESISTOR

+15V
D85 27K
E85 558
D83 IN4454
-CURRENT DETECTOR P2A-5 MO6-R
(LOW FOR "HIGH CURRENT")
D86 1.5K
D87 1.5K
E85 558
D84 IN4454
H86 5.6K
E82 27K
H85 .1 50V
D88 27K
-15V
PLUS
MINUS
M
HEAD POSITIONER
MOTOR POLARITY:
+ FOR FORWARD
K+ = 1.6 LBS/AMP
I MAX = 6.25 AMP

+24V(CKT)
H65 1K
H62 220
H61 27μH
H59 1 35V
H64 A14A
J65 TIP-32A
BRUSH MOTOR 'A'
60HZ SQUARE WAVE
MO5-12 P2A-12

H70 A14A
H73 1 35V
J70 TIP-31A
BRUSH MOTOR 'B'
60HZ SQUARE WAVE
MO5-8 P2A-15
-24V(CKT)
H71 1K
H68 220
H67 27μH

P7-7
M BRUSH MOTOR
P7-8

J90 75451
J91 .001μf
J92 A14A
J94 1.5K 1/2W
R1 30 10W
R2
DRAWER UNLOCK SOLENOID
P7-9
P7-10 #387 LOAD
+24V(CKT) P7-11

MO1-2 P1A-2 -DRAWER UNLOCK ENABLE

+24(CKT)
H100 2.2K 1/2W
MO1-5 P1A-15 +DRAWER UNLOCK PICK
H99 2.2K
J99 TIP-31A
H98 18K
-24(CKT)
H103 100
J102 TIP-31A
J88 A14A
R3 20 10W
R4
+24V(CKT)
H78 IN4454
H78 A14A
P7-12
HEAD LOAD SOLENOID

J85 75451
J86 75451
J86 .001
MO5-16 P2A-9 -HEAD LOAD ENABLE
MO5-M P2A-13 +HEAD LOAD PICK
J75 TIP-31A
J80 TIP-31A
H81 100
H76 1K
-24V(CKT)

HS

Diablo Systems Incorporated

TITLE HEAT SINK CIRCUIT BOARD
HS-CB SCHEMATIC

MODEL 40
PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.
SYSTEM LOGIC NO SL00044
SHEET 2 TOTAL SHEETS 2 SIZE D
PRODUCT NO 11418 REV P

REV	ECO NO	REV	ECO NO	REV	ECO NO	REV	ECO NO	REV	ECO NO	REV	ECO NO	REV	ECO NO	REV	ECO NO	REFS	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
T		S		R		P3936		N3607		M3560		L2976		K2923		J2908							

PRODUCT NO 11418 REFERENCE DESIGNATORS NOT USED REFERENCE DESIGNATORS NOT USED

PRODUCT NO. 11631-XX

DEVELOPMENT REV. D5

P11-C & F + 24V PWR

P11-A & D − 24V PWR

PART NO.	E.C.O.	REV.
11631-00	3936	G
11631-01	3936	F

NOTES:
UNLESS OTHERWISE SPECIFIED

1 ALL RESISTORS ARE 1/4W ± 5%.

2 ALL 1% RESISTORS ARE 1/8W.

3 ALL DIODES ARE A15A.

[4] CURRENT LIMITING RESISORS MOUNTED ON SIDE OF BOWL.

5 ALL RESISTORS ARE IN OHMS.

6 ALL CAPACITORS ARE IN μf.

[7] OPTIONAL FEATURES:
7.1 FOR STANDARD MACHINE (11631-00), CONNECT A 30Ω JOW RESISTOR ACROSS POINTS R1 & R2.
7.2 FOR INTERLOCK OPTION (11631-01), CONNECT POINTS R1 & R2 WITH A WIRE JUMPER.

[8] RESISTOR B94 IS SELECTED TO OBTAIN +15V ± 0.1V AT P2A-6.
THEN RESISTOR B103 IS SELECTED TO OBTAIN −15V ± 0.1V AT P2A-3.

M01-4 P1A-4 PHASE 1A

P11-P MOTHER-CB P1A-1

P11-R MOTHER-CB P1A-16

P1A-8 GND

M01-C P1A-14 +SPINDLE MOTOR CURRENT CONTROL (GND FOR "FULL" CURRENT)

M01-3 P1A-3 -SPINDLE MOTOR CURRENT CONTROL (GND FOR "FULL" CURRENT)

M01-7 P1A-6 PHASE 1B

M01-9 P1A-9 PHASE 2B

P11-J & M MOTHER-CB P2A-1 +5V

P2A-2

M01-J P1A-7 PHASE 2A

SPINDLE DRIVE MOTOR WINDING Ø1

SPINDLE DRIVE MOTOR WINDING Ø2

P11-N +24V (CKT)

P11-L −24V (CKT)

SPEED SENSE A P1A-12 M01-E

SPEED SENSE B P1A-5 M01-12

P2A-11 MOTHER-CB +15V

P2A-6 MOTHER-CB

P2A-14 MOTHER-CB -15V

P2A-3 MOTHER-CB

P2A-16 M06-8

P2A-4 M06-16

−24V CKT

+24V CKT

HS

Diablo Systems Incorporated
Hayward, California 94545

TITLE: HEAT SINK CIRCUIT BOARD HS-CB SCHEMATIC

MODEL: 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO. SL00045

SHEET 1 | TOTAL SHEETS 3 | SIZE D | PRODUCT NO. 11631-XX | REV G

REV J E.C.O. NO. | REV H E.C.O. NO. | REV G E.C.O. NO. 3936 | REV F E.C.O. NO. 3720 | REV E E.C.O. NO. | REV D E.C.O. NO. 3680 | REV C E.C.O. NO. 3561 | REV B E.C.O. NO. | REV A E.C.O. NO. | MFG | DATE | ENG | DATE | CHECKED | DATE | DRAWN | DATE

PRODUCT NO 11631-XX | REFERENCE DESIGNATORS MAY VARY | REFERENCE DESIGNATORS MAY VARY

PRODUCT NO. 11631-XX

PRODUCT NO 11631-XX DEVELOPMENT REV. D5

SERVO RELEASE SWITCH

SERVO INHIBIT
SI-CB
11679

J91-8 (ORN) 2 +5V

SHI-P7-1 (YEL) 5

SHI-P7-3 (GRN) 4

CR1 IN4454

CR2 IN4454

R1 16K 5%, 1/4W

R2 3.3K 5%, 1/4W

R3 4.7K 5%, 1/4W

U1 380

CR3

K1

(YEL) 7

(BLK) 6

A B

(BLU) 3

(NOT USED) 1

(BLK) 8

(YEL) 9

MP-A

MP-B

M06-15 P2A-10 SERVO DISABLE
(GND ± 0.8V FOR DISABLE)

P2A-7 GND

M07-X P2A-8 SERVO DRIVE SIGNAL
(+ FOR FORWARD)

B87 4.02K 1%

+15V B90 IN4454

B88 42.2K 1%

B89 3.9K

B82 558

A82 .1 50V

A86 1K

A81 10.2K 1%

B82 558

A77 2.2K

A75 510pf

B91 .1 50V

A84 2.7M

A83 510pf

E81 1K 1%

-15V

+24V (CKT)

H65 1K

H62 220

H61 27MH

H59 1 35V

H64 A14A

M05-12 P2A-12 BRUSH MOTOR "A" 60HZ SQUARE WAVE

J65 TIP-32A

H70 A14A

M05-8 P2A-15 BRUSH MOTOR "B" 60HZ SQUARE WAVE

J70 TIP-31A

H73 1 35V

-24V (CKT)

H71 1K

H68 220

H67 27MH

M01-2 P1A-2 -DRAWER UNLOCK ENABLE

M01-5 P1A-15 +DRAWER UNLOCK PICK

M05-16 P2A-9 -HEAD LOAD ENABLE

M05-M P2A-13 +HEAD LOAD PICK

SI-2

J91 75452

J83 75451

J86 4.7K

J88 IN4454

H90 10K

H101 56 1W

H103 A14A

J92 56 1W

J94 A14A

J97 TIP-31A

J90 22K

J89 22K

J107 TIP-31A

J112 TIP-31A

H106 100

J91 75452

+5V

+24V (CKT)

-24V (CKT)

-24(CKT)

B66 1K

A68 TIP-32A

B72 2N5881

B73

B70 1K 1/2W

B77 2N3643

A72 510pf

A73 100

B79 680 1/2W

D81 300 1/2W

B81 51pf

D74 2N3644

E71 510pf

E76 100

D71 1K 1/2W

E68 TIP-31A

E72 2N5879

E75

E64 1K

- 24V(CKT)

D84 .2 1% 10W CURRENT SENSE RESISTOR

H87 5.6K

E80 27K

H88 .1 50V

D89 27K

D90 1.5K

D91 1.5K

E88 558

D87 IN4454

D88 IN4454

D92 27K

- 15V

— CURRENT DETECTOR (LOW FOR "HIGH CURRENT") P2A-5 M06-R

PLUS

MINUS

M

HEAD POSITIONER MOTOR POLARITY:
+ FOR FORWARD
K_T = 1.6 LBS/AMP
I_{MAX} = 6.25AMP

P7-7

P7-8

P7-9

P7-10

P7-11

P7-12

BRUSH MOTOR

DRAWER UNLOCK SOLENOID

#387

LOAD

HEAD LOAD SOLENOID

H98 IN4454

J87 A14A

J85 1.5K 1/2W

H99 .001

H77 IN4454

H78 A14A

H80 .001

R1 7

R2

R3

R4 20 10W

H107 A14F

J102 TIP-31A

J75 TIP-31A

J80 TIP-31A

H81 100

H75 1K

HS

Diablo Systems Incorporated
Hayward California 94545

TITLE HEAT SINK CIRCUIT BOARD
HS-CB SCHEMATIC

MODEL 40

PROPRIETARY REPRODUCTION OR UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO SL00046

SHEET 2 TOTAL SHEETS 3 SIZE D PRODUCT NO. 11631-XX REV G

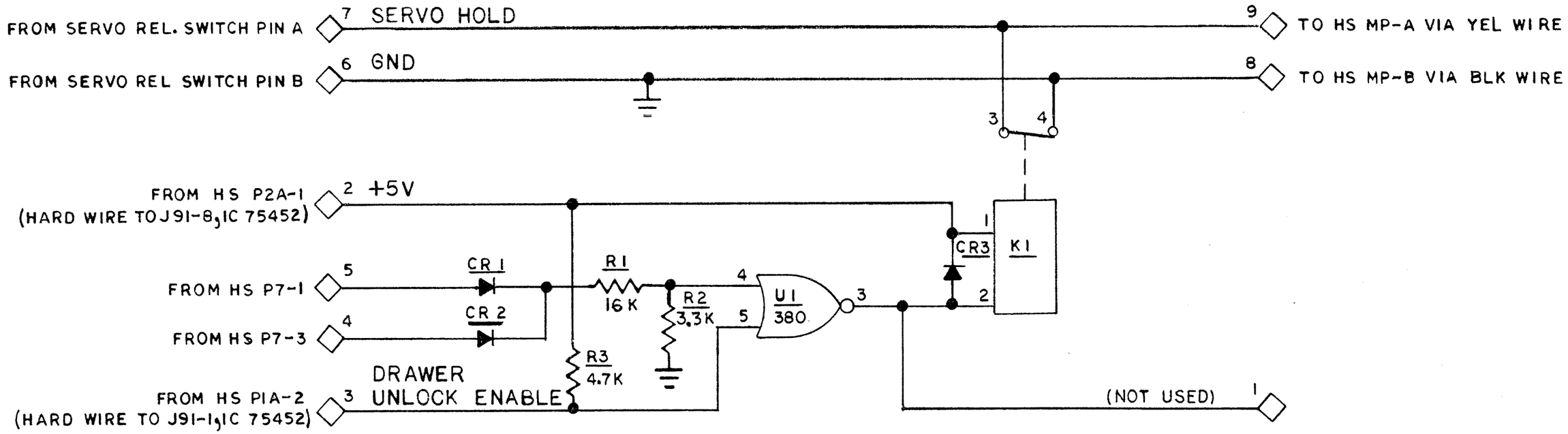
PRODUCT NO 11631-XX

REFERENCE DESIGNATORS NOT USED

REFERENCE DESIGNATORS LAST USED

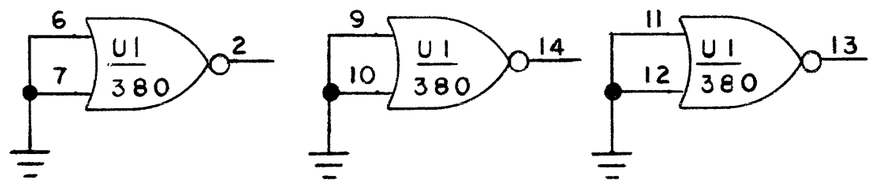
REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	MFG	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J		H		G	3936	F	3720	E		D	3680	C	3561	B		A								

PRODUCT NO. 11679 DEVELOPMENT REV. D1



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL DIODES ARE IN4454.
2. ALL RESISTORS IN OHMS, 5%, 1/4W.

SPARES:



Diablo Systems Incorporated
Hayward, California 94545

TITLE SERVO INHIBIT
SI-CB SCHEMATIC

MODEL 40

PROPRIETARY INFORMATION
UNPUBLISHED DISCLOSURE
ALL RIGHTS RESERVED

SYSTEM LOGIC NO. SL00047

SIZE B | PRODUCT NO. 11679 | REV A

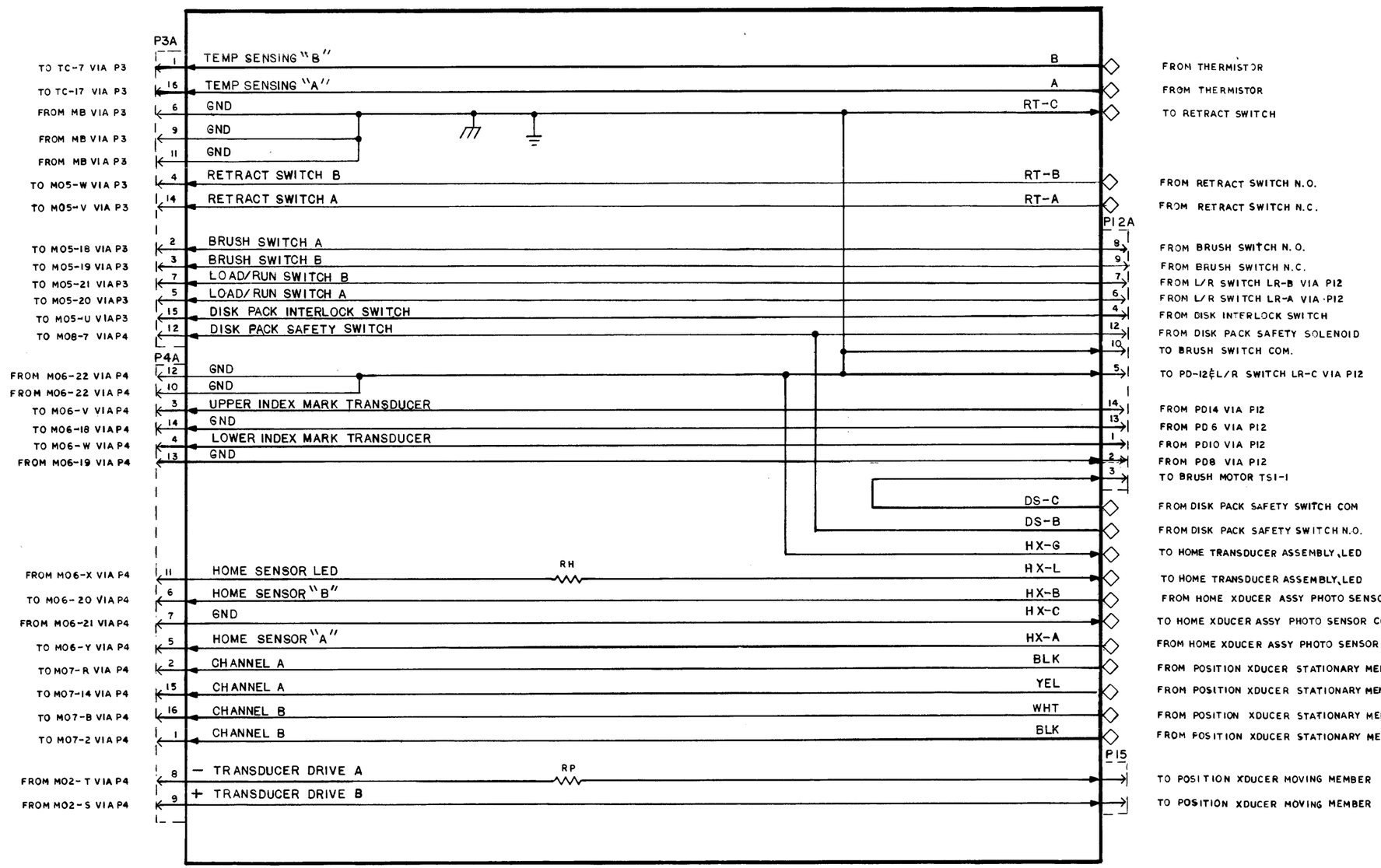
SHEET 1 OF 3

REV	E.C.O. NO.	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J								
H								
G								
F								
E								
D								
C								
B								
A	3949							

PRODUCT NO. 11435

PRODUCT NO. 11435

DEVELOPMENT REV. D1



Diablo Systems Incorporated
Hayward, California 94545

TITLE: WIRING DIAGRAM ACTUATOR AW-CB

MODEL: 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO. SL00048

SHEET 1 TOTAL SHEETS 2 SIZE D PRODUCT NO. 11435 REV G

PRODUCT NO.	REFERENCE DESIGNATORS	REFERENCE DESIGNATORS
11435		

REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO.	REV	E.C.O. NO	REV	E.C.O. NO.	REV	E.C.O. NO	MFG	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J		H		G	3724	F	3575	E	3349	D		C		B		A									

PRODUCT NO. 11691

PRODUCT NO 11691 | DEVELOPMENT REV. → D1

I/O CARD CAGE

I/O 1 (F 6 A Ƶ 1 22) | I/O 3 (F 6 A Ƶ 1 22) | I/O 4 (5 12 F 6 A Ƶ 1 22) | I/O 5 (19 F 6 A Ƶ 1 22) D −6.8 V, E −18 V | I/O 6 (D E, F 6 A Ƶ 1 22) | I/O 2 (F 6 A Ƶ 1 22)

(+5V)
(GND)

(BLU)
(RED)
(ORN) (BLK)

P3

MAIN CARD CAGE

GND
−15 V
+5 V
+15 V

M01 (L 1 22 A Ƶ / 10 F 6 13 P)
M02 (L 1 22 A Ƶ / 10 F 6 13 P)
M03 (L 1 22 A Ƶ / 10 F 6 13 P)
M04 (L 1 22 A Ƶ / 10 F 6 13 P)
M05 (L 1 22 A Ƶ / 10 F 6 13 P)
M06 (L 1 22 A Ƶ / 10 F 6 13 P 8 16)
M07 (L 1 22 A Ƶ / 10 F 6 13 P)
M08 (1 22 / F 6)
M09 (1 22 A Ƶ / F 6)

P2

AW PCB ASSY
P3A
P12A 5
(BLK)

GND
GND
GND
FLAT CABLE

D1 PCB ASSY (OPTIONAL)
B21 +24V (RED)
B33 GND (BLK)

H/S PCB ASSY

P2A
1 +5V — PAIR — FLAT CABLE
6 +15V — PAIR
11
3 −15V — PAIR
14
16
4

PWR (−24V) (BRN)
PWR (+24V) (GRY)
CKT (−24V) (GRN)
CKT (+24V) (YEL)
(ORN)
(BLU)
(PUR)
(BLK)

J91-8 / MP-8
(BRAID) GND
+5 V (ORN)
GND (BLK)

S1 PCB ASSY (2, 6)

(YEL)
(BRAID)

P12 12
(BLK)
PD PCB ASSY
+24V
GND
+24V

PAIR
+5V (RED) (WHT)

P11 PCB ASSY 11425

A — − 24V PWR (BLU), − 24V PWR (BRN), − 24V PWR (GRY)
D
C — + 24V PWR (RED), + 24V PWR (GRN), + 24V PWR (YEL)
F
L — − 24V CKT (ORN), − 24V CKT (BLU)
N — + 24V CKT (PUR), + 24V CKT (BLK)
H — − 24V R/W (GRY)
K — + 24V R/W (BRN)
J — + 5V (ORN), + 5V (ORN), + 5V (RED), + 5V (WHT)
M
P — GND (1/4" BRAID), GND (1/2" BRAID), GND (BLK)
R

(GRY) −24V
(BRN) +24V
(ORN) +5V
(BRAID) GND

R/W PCB ASSY

Diablo Systems Incorporated

TITLE: DC POWER DISTRIBUTION

MODEL 40

PROPRIETARY INFORMATION — UNAUTHORIZED DISCLOSURE OR USE PROHIBITED

SYSTEM LOGIC NO. SL00049

SHEET / TOTAL SHEETS / SIZE D / PRODUCT NO. 11691 / REV. A

PRODUCT NO. 11691 | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED

REV ECO NO.	REV ECO NO	REV ECO NO	REV ECO NO	REV ECO NO	REV ECO NO	REV ECO NO	REV ECO NO	REV ECO NO	MFG	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J	H	G	F	E	D	C	B	A								

PRODUCT NO. 16750C

PRODUCT NO 16750 — DEVELOPMENT REV.

11562

115VAC 60Hz

T1 11500

11575

BR1 MDA990-2

BR2 MDA990-2

C3 51K 40V

C2 51K 40V

R2 100 50W

R1 50 50W

C1 18K 25V

C4 .15 440 VAC

FAN

RED A33 — +24V PWR (8A)

ORN A41 — +24V CKT (8A)

BLK B25 — AUX GND (D28 A15A, D36 A15A)

BLK A25 — GND

BLU A11 — -24V PWP (8A, D20 A15A, D12 A15A)

VIO A18 — -24V CKT (8A)

GRY A3 (7A) — +5.3V AUX (B41 10 1/4W 5%), +5.3V (B59 .01 2W 3%)

BLK A45 / A48 — +5V RET, +5V RET AUX

B3 2N5885 A56 (GRY, YEL, BLU A52)

D56 TIP31A

B65 100 1/4W 5%

B63 100 1/2W 5%

B61 100 1/2W 5%

B50 100 20V TA.

E60 C22.0F

E75 .1 50V

E74 12 20V

E72 100 1/4W 5%

+24V CKT — E80 680 1W 5% — E70 A14F — E67 5V 1% — +24V CKT — B66 1K

TP1 — TP3

TP2 — B62 500 1/2W

D61 750

D63 2.21K

D76 LM 723C

D75 .1 50V

B71 750

D72 1.82K

B70 33.2K

B76 558

B68 1K

D71 IN4454

D70 IN4454

D69 IN4454

D68 IN4454

D66 2.4K 1/4W 5%

-24V CKT

115VAC 50Hz

T1 11500

11575

C4 .15 440 VAC

LOAD

FAN

220VAC 60Hz

T1 11500

11575

C4 .15 440 VAC

5A

LOAD

FAN

220VAC 50Hz

T1 11500

11575

C4 .15 440 VAC

5A

LOAD

FAN

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL CAPACITOR VALUES IN MICROFARADS.
2 ALL RESISTOR VALUES IN OHMS, ±1%, 1/8 W.

Diablo Systems Incorporated
Hayward California 94545

TITLE: SCHEMATIC - PWR SUPPLY

MODEL 429

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO. SL0005C

SHEET | TOTAL SHEETS | SIZE B | PRODUCT NO. 16750 | REV D

PRODUCT NO. 1675C | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED

REV	E.C.O. NO.	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J								
H								
G								
F								
E								
D	3642							
C								
B								
A								

PRODUCT NO. 11473-XX

PRODUCT NO. 11473-XX DEVELOPMENT REV. D1

B	1	— WRITE DATA LINE
V	2	— SELECT LINE 3
Z	3	— SELECT LINE 4
R	4	— SELECT LINE 2
L	5	— SELECT LINE 1
F	6	— READY TO S/R/W LINE
A	7	— READ CLOCK LINE
D	8	(NOT USED)
C	9	— READ DATA LINE
E	10	— READ GATE LINE
J	11	— TRACK ADDR BIT 4
N	12	— TRACK ADDR BIT 1
H	13	— WRITE PROT INPUT LINE
K	14	— ERASE GATE LINE
M	15	(NOT USED)
T	16	— TRACK ADDR BIT 32
P	17	— WRITE PROT STATUS LINE
X	18	— TRACK ADDR BIT 8
S	19	GROUND
B	20	— TRACK ADDR BIT 64
U	21	— FILE READY LINE
W	22	— SECTOR MARK LINE
F	23	— TRACK ADDR BIT 16
Y	24	— INDEX MARK LINE
A	25	HEAD SELECT LINE (LOW FOR UPPER)
C	26	— SECTOR ADDRESS BIT 1 LINE
M	27	— TRACK ADDR BIT 256
E	28	— WRITE GATE LINE
H	29	— WRITE CHECK LINE
K	30	— SECTOR ADDRESS BIT 4 LINE
N	31	— SECTOR ADDRESS BIT 8 LINE
R	32	+5V
T	33	— STROBE LINE
S	34	— TRACK ADDR BIT 2
V	35	— SECTOR ADDRESS BIT 16 LINE
X	36	GROUND
W	37	— RESTORE LINE
AA	38	DISC SELECT LINE (LOW FOR UPPER)
Z	39	— 200 TPI
BB	40	— TRACK ADDR BIT 128
DD	41	— ATTENTION LINE 2
Y	42	— LOGICAL ADDR INTERLOCK LINE
EE	43	— ATTENTION LINE 3
FF	44	— ATTENTION LINE 4
CC	45	— ATTENTION LINE 1
U	46	— SEEK INCOMPLETE LINE
P	47	— ADDR ACKNOWLDGE LINE
J	48	— SECTOR ADDRESS BIT 2 LINE
D	49	(NOT USED)
HH	50	GROUND

RECP

A

Diablo Systems ASSY NO. 11438 REV

PINS

A

Diablo Systems ASSY NO. 11446 REV

NOTE:
UNDERLINED PIN DESIGNATIONS DENOTES LOWER CASE LETTERS.

CONNECTOR

WIRE SEQUENCE

LINE LABEL

Diablo Systems Incorporated
Hayward, California 94545

TITLE: SCHEMATIC
50 LEAD FLAT CABLE

MODEL: 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED. SYSTEM LOGIC NO. SL00051

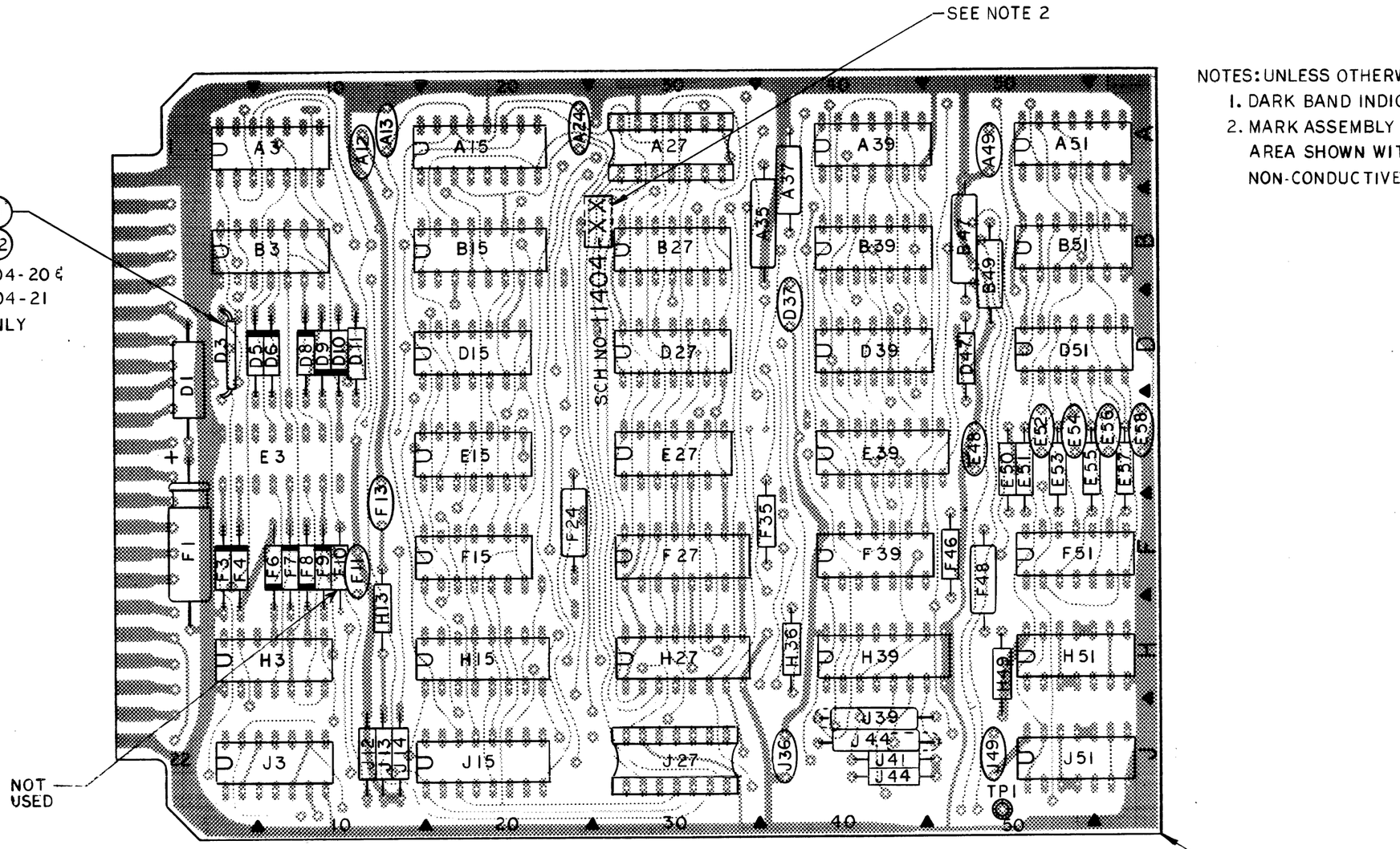
SHEET 1 TOTAL SHEETS 2 SIZE B PRODUCT NO. 11473-XX REV D

PRODUCT NO. 11473-XX | REFERENCE DESIGNATORS NOT USED | REFERENCE DESIGNATORS LAST USED

REV	E.C.O. NO.	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J								
H								
G								
F								
E								
D	3981							
C								
B								
A								

PRODUCT NO. 11404-XX

PRODUCT NO. 11404-XX DEVELOPMENT REV. D1



NOTES: UNLESS OTHERWISE SPECIFIED

1. DARK BAND INDICATES CATHODE OF DIODE.
2. MARK ASSEMBLY WITH APPROPRIATE DASH NO. IN AREA SHOWN WITH CLEARLY LEGIBLE, PERMANENT, NON-CONDUCTIVE CHARACTERS.

			TIME DELAY		CAPACITORS		RESISTORS		JUMPER
REV.	PART NO.	DESCRIPTION	H39A	H39B	J39	J44	J41	J45	D3
F	11404-00	PCB ASSY-ADDRESS LOGIC 1, 100 TPI	500 NS ±150NS	1 µS ± .3µS	270 PF	300 PF	5.1 KΩ	10 KΩ	⟍
D	11404-01	PCB ASSY- ADDRESS LOGIC 1, 100 TPI, SERIES 30 COMPAT.	35µS ±10µS	5µS ±2µS	.0033µF	.001µF	33K	15KΩ	⟍
F	11404-20	PCB ASSY- ADDRESS LOGIC 1, 200 TPI	500 NS ±150NS	1 µS ± .3µS	270 PF	300 PF	5.1 KΩ	10 KΩ	22 AWG
D	11404-21	PCB ASSY ADDRESS LOGIC 1, 200 TPI, SERIES 30 COMPAT.	35 µS ± 10µS	5µS ±2µS	.0033µF	.001µF	33 K	15 KΩ	22AWG

Diablo Systems Incorporated
Hayward, California 94545

TITLE: ADDRESS LOGIC 1
ALI-CB

MODEL 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED. SYSTEM LOGIC NO. SL00052

SHEET | TOTAL SHEETS | SIZE D | PRODUCT NO. 11404-XX | REV H

PRODUCT NO. 11404-XX

REFERENCE DESIGNATORS NOT USED

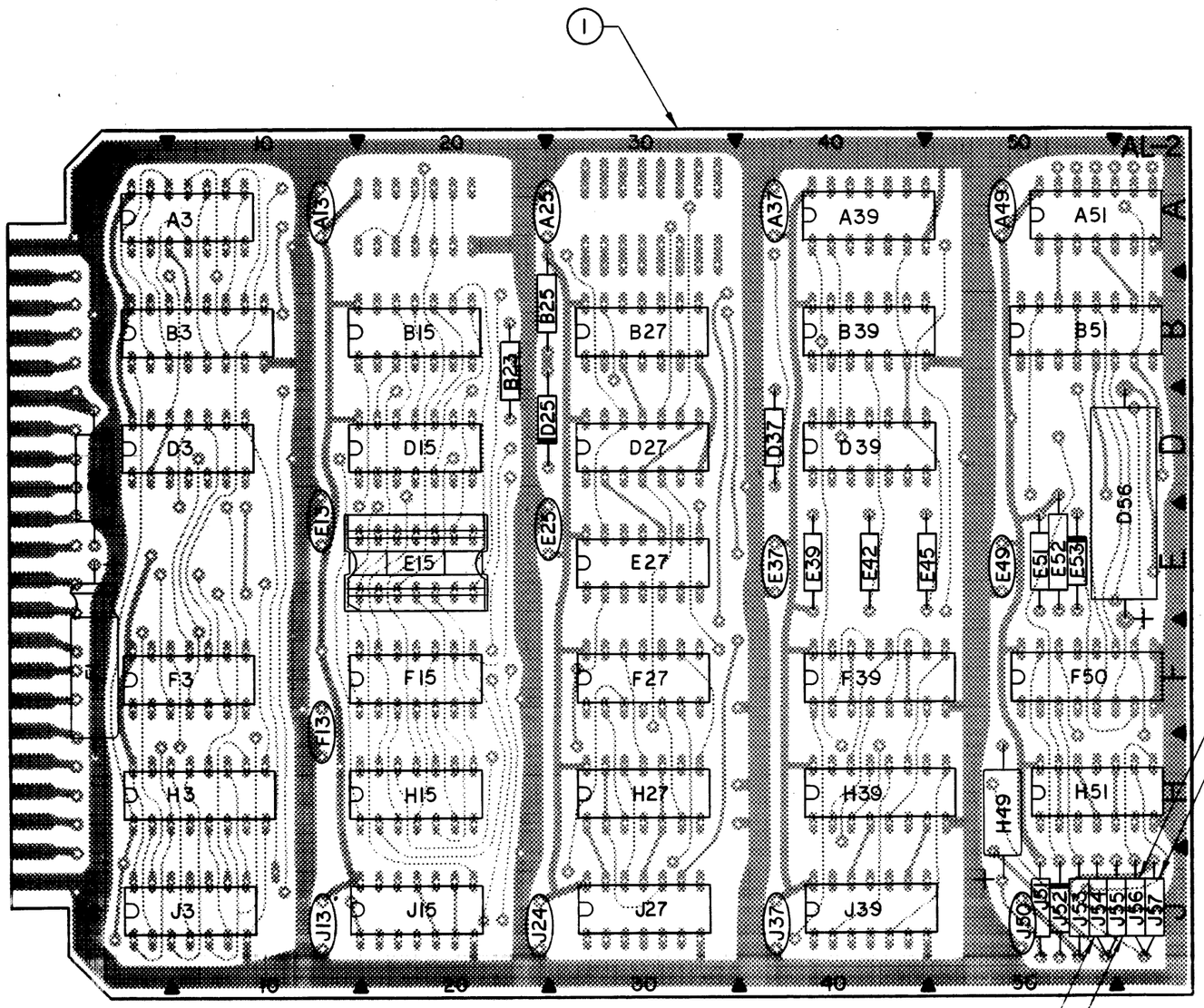
REFERENCE DESIGNATORS LAST USED

REV E.C.O. NO.	REV E.C.O. NO.	REV E.C.O. NO.	REV E.C.O. NO.	REV E.C.O. NO.	REV E.C.O. NO.	REV E.C.O. NO.	REV E.C.O. NO.	REV E.C.O. NO.	MFG DATE	ENG DATE	CHECKED DATE	DRAWN DATE
J	H 3813	G	F	E	D 3553	C 3814	B	A				

PRODUCT NO. 11407-XX DEVELOPMENT REV. →

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL 5% RESISTORS ARE 1/4W.
2. ALL 1% RESISTORS ARE 1/8W.
3. ALL DIODES ARE IN4454.
4. DARK BAND INDICATES CATHODE OF DIODE.
5. OPTIONAL FEATURES:
   - 5.1 FOR 100 TPI OPERATIONS: (11407-00), J55 AND J57 COMPONENTS ARE USED.
   - 5.2 FOR 200 TPI OPERATIONS: (11407-20), J54 AND J56 COMPONENTS ARE USED.



TABULATION SCHEDULE

PART NO.	DESCRIPTION	J54	J55	J56	J57
11407-00	PCB ASSY-100 TPI ADDRESS LOGIC 2	/	10Ω	/	10Ω
11407-20	PCB ASSY-200 TPI ADDRESS LOGIC 2	10Ω	/	10Ω	/

PART NO.	E.C.O. NO.	REV
11407-00	3594	G
11407-20	3594	C

Diablo Systems Incorporated
Hayward California 94545

TITLE: ADDRESS LOGIC 2
AL2 - CB

MODEL: 40

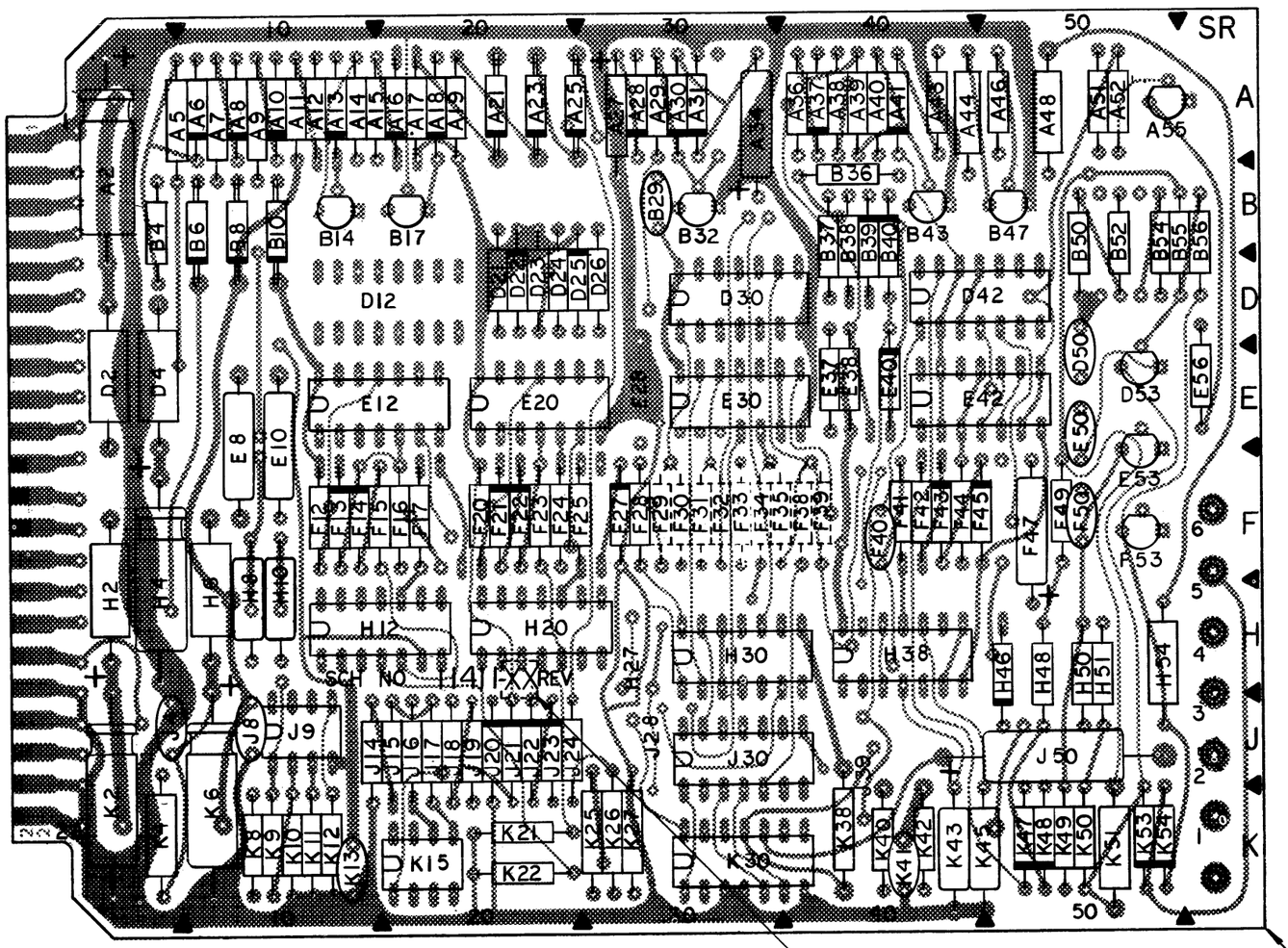
PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED. SYSTEM LOGIC NO. SL00053

SHEET	TOTAL SHEETS	SIZE	PRODUCT NO.	REV
2	2	D	11407-XX	G

REV	E.C.O. NO.	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
J								
H								
G	3594							
F								
E								
D								
C								
B								
A								

PRODUCT NO. 11411-XX

DEVELOPMENT REV. D5



NOTES: UNLESS OTHERWISE SPECIFIED
1. DARK BAND INDICATES CATHODE OF DIODE.
2. SQUARE PAD INDICATES EMITTER OF TRANSISTOR.
3. MARK ASSEMBLY WITH APPROPRIATE DASH NO. IN AREA SHOWN WITH CLEARLY LEGIBLE, PERMANENT, NON-CONDUCTIVE CHARACTERS.

TABULATION SCHEDULE

PART NO.	DESCRIPTION	REMARKS	RESISTORS F12, F20	RESISTORS F29, F31, F35	RESISTORS F30, F32, F34	CAP. E8, E10
11411-00	PCB ASSY-SENSOR, W/O SECT. COUNTER		12KΩ	10Ω	—	.0047μF
11411-01	PCB ASSY-SENSOR, W/SECT. COUNTER		12KΩ	—	10Ω	.0047μF
11411-02	PCB ASSY-SENSOR, W/O SECT. COUNTER, SERIES 30 COMPAT.		15KΩ	10Ω	—	.001μF
11411-03	PCB ASSY-SENSOR, W/SECT. COUNTER, SERIES 30 COMPAT.		15KΩ	—	10Ω	.001μF

Diablo Systems Incorporated
Hayward California 94545

TITLE: SENSOR CIRCUITS SR-CB

MODEL: 40

PROPRIETARY INFORMATION UNAUTHORIZED DISCLOSURE OR USE PROHIBITED.

SYSTEM LOGIC NO. SL00054

SHEET 2 TOTAL SHEETS 2 SIZE D PRODUCT NO. 11411-XX REV L

PRODUCT NO. 11411-XX

REFERENCE DESIGNATORS

REFERENCE DESIGNATORS

REV ECO NO.	REV ECO NO.	REV E.C.O. NO.	REV E.C.O. NO.	REV E.C.O. NO.	REV E.C.O. NO.	REV E.C.O. NO.	REV E.C.O. NO.	REV E.C.O. NO.	REV E.C.O. NO.	MFG	DATE	ENG	DATE	CHECKED	DATE	DRAWN	DATE
L 3824	K 3778	J 3665	H 2973	G	F	E	D	C	B	A							

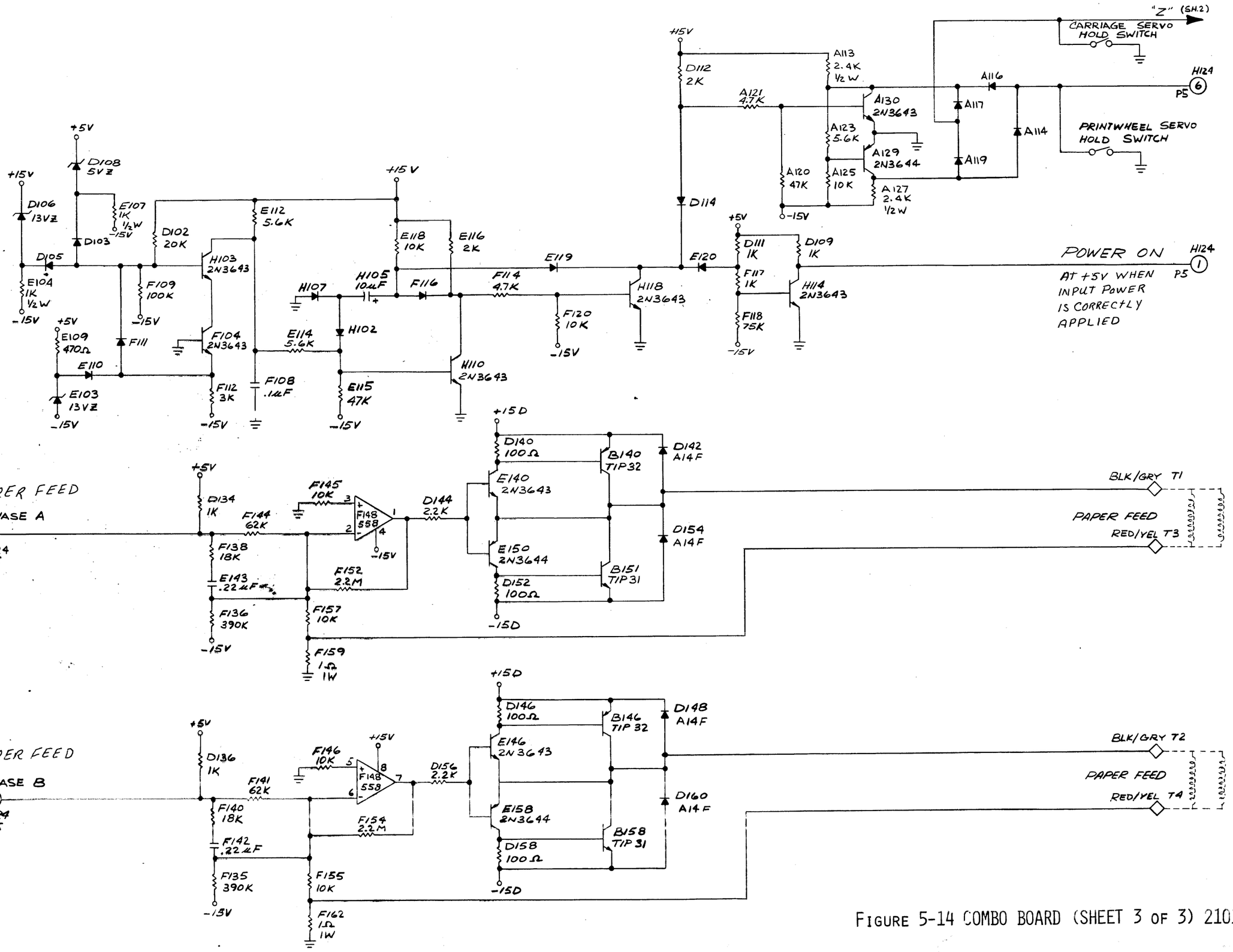


FIGURE 5-14 COMBO BOARD (SHEET 3 OF 3) 21012E