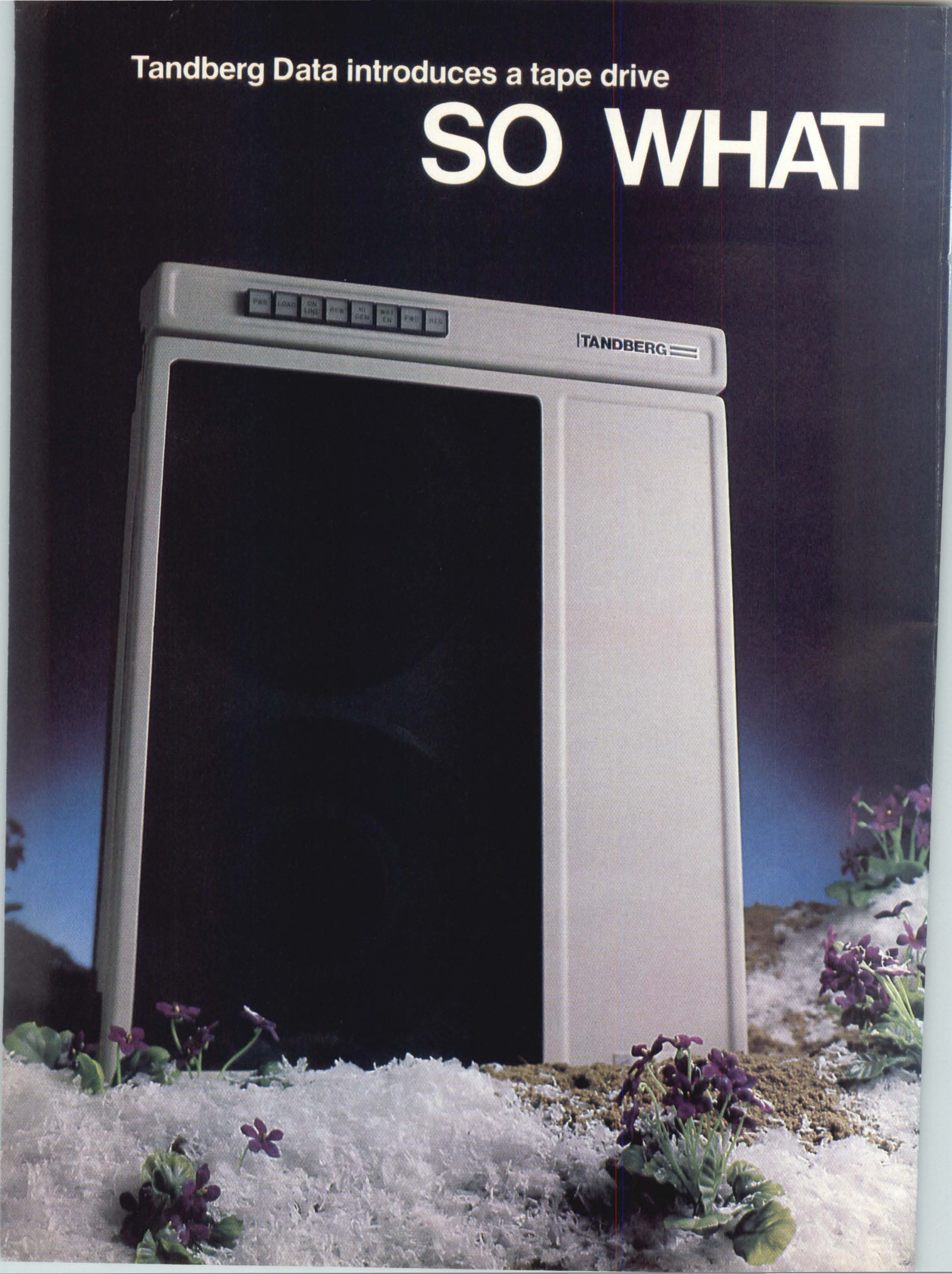
digital design

the magazine of digital systems

CRT Terminals: up-up and away

The POLY 88 Microcomputer System
PolyMorphic Systems now offers the complete, assembled, personal computer system—the POLY 88 System 16. A full 16K system with high speed video display, alphanumeric keyboard, and cassette program storage. A BASIC software package providing the most advanced features available in the personal computing market. Features like PLOT and TIME, which utilize our video graphics and real-time clock. Others like VERIFY, so that you know your tape is good before you load another. Or input type-ahead so you can tell your program to run while the tape is still loading (it stores up to 64 characters of commands or question responses to be executed). All these plus a complete package of scientific functions, formatting options, and string capabilities. With the POLY 88 System 16 you can amaze your timesharing friends the very first night!
PolyMorphic Systems 11K BASIC
Size: 11K bytes.
Scientific Functions: Sine, cosine, log, exponential, square root, random number, x to the y power.
Formatted Output • Multi-line Function Definition • String Manipulation and String Functions • Real-Time Clock • Point-Plotting on Video Display • Array dimensions limited by memory • Cassette Save and Load of Names Programs • Multiple Statements per Line • Renumber • Memory Load and Store • 8080 Input and Output • If Then Else • Input type-ahead.
Commands: RUN, LIST, SCR, CLEAR, REN, CONT.
Statements: LET, IF, THEN, ELSE, FOR, NEXT, GOTO, ON, EXIT, STOP, END, REM, READ, DATA, RESTORE, INPUT, GOSUB, RETURN, PRINT, POKE, OUT.
Built in Functions: FREE, ABS, SGN, INT, LEN, CHR$, VAL, STR$, ASC, SIN, COS, RND, LOG, TIME, WAIT, EXP, SQRT, CALL, PEEK, INP, PLOT.
Systems Available. The POLY 88 is available in either kit or assembled form. It is suggested that kits be attempted only be persons familiar with digital circuitry. The following are two of the systems available.
System 2: is a kit consisting of the POLY 88 chassis, CPU, video circuit card, and cassette interface. Requires keyboard, TV monitor, and cassette recorder for operation. $690
System 16: consists of an assembled and tested System 2 with 16K of memory, keyboard, TV monitor, cassette recorder, 11K BASIC and Assembler on cassette tapes. $1995.
Prices and Specifications subject to change without notice.
California residents add 6% sales tax.
Thanks for the help
AW GEE, YOU DIDN'T HAVE TO DO THAT
LIST
10 PRINT "AW GEE, YOU DIDN'T HAVE TO DO THAT"
PolyMorphic Systems
460 Ward Drive Santa Barbara, Ca. 93111 (805) 967-2351
POLY 88
PolyMorphic Systems
On
Reset


Tandberg Data introduces a tape drive
SO WHAT
TANDBERG

ELSE IS NEW?

Performance. On an absolutely new level.

With the name Tandberg you expect top performance. And innovation. And being a little ahead of the competition in certain fresh and subtle ways. Ditto our new TDI 1050 Synchronous Tape Transport.

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A few other goodies are our 5,000-hour MTBF, a dual ceramic-blade tape cleaner, and our proven microprocessor control system. A choice of 7 or 9 track. And IBM geometry provides minimal dynamic skew. Also, a fully documented maintenance manual with all the data and schematics necessary for easy and economical upkeep.

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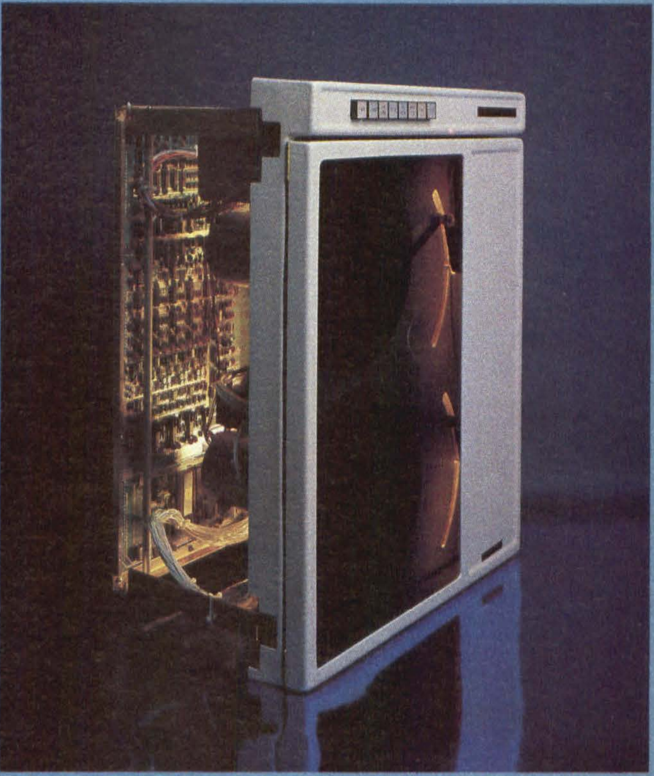
San Diego, California 92117
Telephone (714) 270-3990



Mr. Peter A. Gilbody, Vice President, Tandberg Data Inc.
4060 Morena Blvd., San Diego, CA 92117

I'd like to know more about the NEW TDI 1050 Synchronous Tape Transport from Tandberg Data. Please send me the TDI 1050 data sheet ☐ and have a Tandberg engineer give me a call to discuss my needs ☐.

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Company ____________

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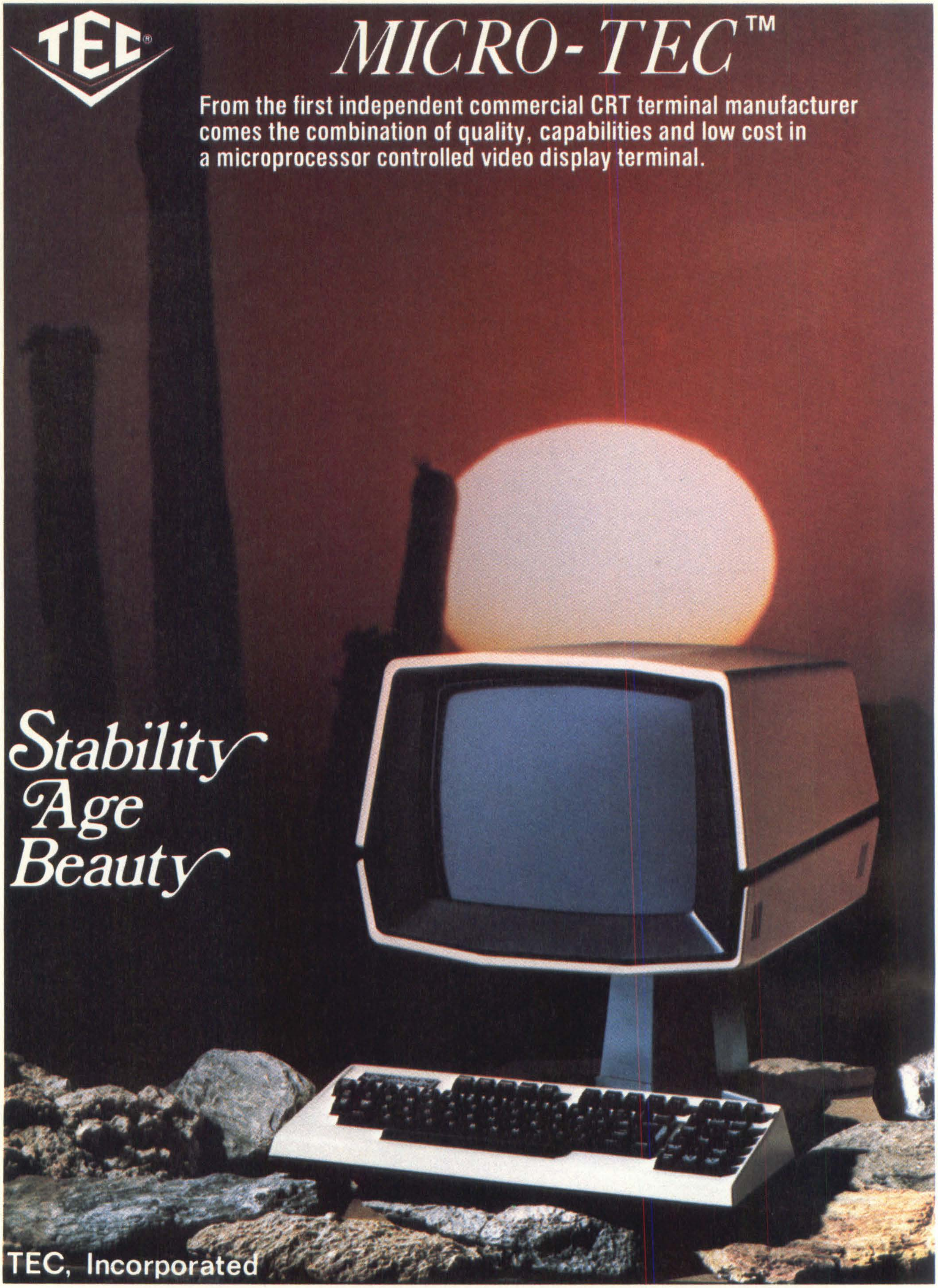
Computer type ____________

TANDBERG

CIRCLE 5



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CIRCLE 6

CONTENTS

digital design

Volume 7 Number 4 April 1977

this month

departments

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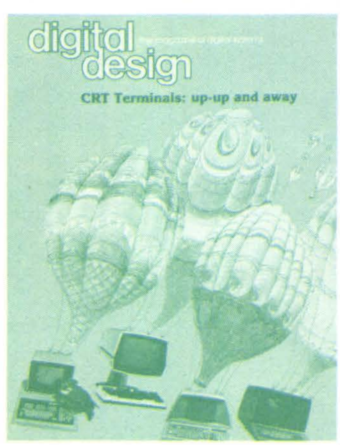
cover



Photographs courtesy of, from left to right: Perkin-Elmer, TEC, Lear Siegler and Beehive. Cover design & illustration by Mary Ann Parker.

next month

In May, we introduce a new kind of service for you – a new addition to the kind of technology assessment articles we publish almost monthly. Next month, our article on **Magnetic Bubble Memories** will tell you what magnetic bubbles are, who holds the first patent, who holds successive patents – including patent numbers, dates of issue, conceptual schemes and their technology thrust.

The material should be of use to design engineers, to researchers, to market planners, to legal staffs – primarily to those of you who always worry about what should come off your production lines in the next 2 to 5 years.

We've organized the information to help you assess the extent to which bubble memory advances could be an aid or a threat, the extent to which bubble memories could force their way into your systems designs, the extent to which you may continue to ignore them. This and future articles of importance to the digital systems market place will help you analyze the strength of your technological base, the protection your technology possesses, the proprietary portion of your current and future designs, the early warning procedures you can setup to anticipate competition.

These problems – more than ever before – belong to the domain of the digital systems designer. We aim to help you solve them with this additional kind of investigative assessment of important digital technology.

digital design

staff

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CALCOMP

letters

positioner uses bit-slice ICs

• With reference to your article on my positioning system (October, page 74), I would like to note that because the algorithms that digitally generate the system's linear velocity ramp produce pulses representing small incremental motion commands – typically on a machine tool as fine as 0.0001 in/pulse with positioning velocities up to 500 in/min – those algorithms must be performed very rapidly. The variety of programmable bit-slice integrated circuits now available provides an economical means of performing the fast incremental type of computation of the linear velocity ramp generator of my positioning system.

HYMIE CUTLER
President
Master Controls Co.
Detroit, MI

excellence

• Just a quick note to say that Terry Dollhoff's article on microprocessors (part one, November) was excellent. It will make an excellent series – and an excellent prototype for similar areas. (And I *rarely* use the word *"excellent"*. .)

MICHAEL RADOW
Telefusion
New York City

correction

• *Editor's note: Dollhoff's November article contained a misprint. The routine on page 69 should read*

```
        CLR  PORT
        LDA  B
LOOP    BSR  WAIT
        STA  A PORT
        ROR  A
        DEC  B
        BNE  LOOP
        BSR  WAIT
        INC  A
        STA  PORT
        BSR  WAIT
```

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The works.

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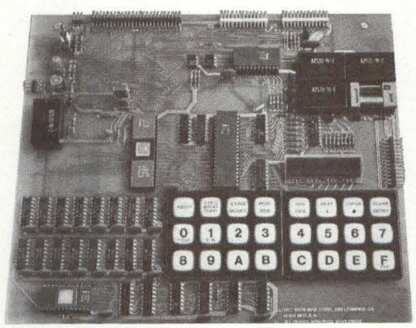
You can be running hardware configurations today. Without adding a single component.

The IMSAI Control Computer is RS232 compatible, which means you can interface just about any peripheral available. There are 12 quasi-bidirectional I/O lines with handshaking, and 14 more regular I/O lines, 5 heavy duty relays, and Teletype and audio cassette interfaces. Plus, a 24 pad hexadecimal keyboard and a 9-digit LED hex display. All on one board.



There's already an extra 1K of RAM on board, plus sockets for another 1K of RAM and 2K of ROM/EROM. Still need more memory? The IMSAI 8048 allows expansion up to 64K of RAM off board.

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CIRCLE 22

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With help from dual microprocessors, carousel accesses 16 3M-type cartridges

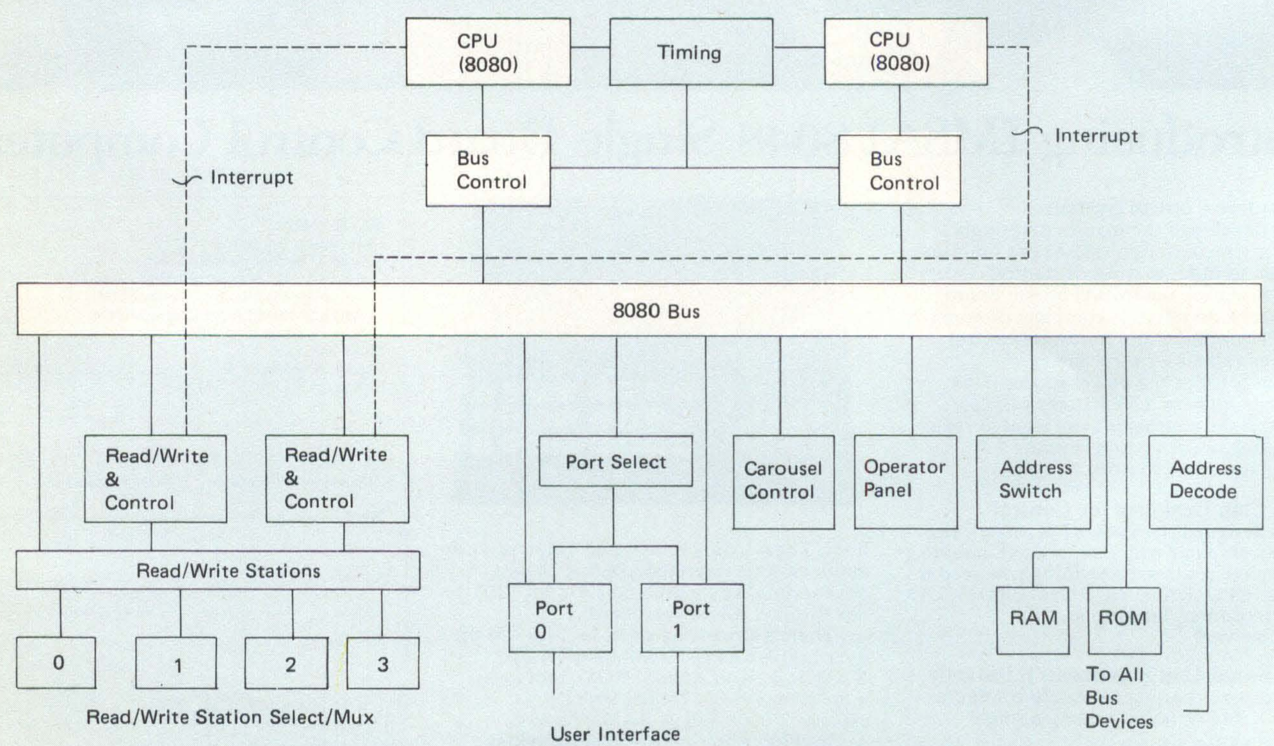
Incorporating dual Intel 8080 microprocessors to control all facets of its operation, a recently introduced carousel storage system houses and accesses up to 16 3M-type quarter-inch tape cartridges in a removable pack. The system's chief designer claims that designing a similar system without using microprocessors would have proved prohibitively expensive.

James Bauch, product manager at National Computer Systems, Minneapolis, explains that the firm's Carousel 5200 is aimed at applications in which large amounts of storage are more important than fast response time. The 32-Mbyte system can load a cartridge into a read/write station in 2.7 sec, can index its 16-slot carousel pack by one slot position in 0.65 sec, and can move the pack eight positions in 1.55 sec.

Dual micros aid operation. Though it superficially resembles a 35-mm circular slide projector, the system doesn't handle its tape cartridges like a slide projector handles slides. Each cartridge is positively held by springs in the pack; when the system wants to read or write data on a cartridge it must grab the cartridge with a pair of mechanical arms, pluck the holding springs aside and, aided by a downward force from

Duplicating the system's functions without microprocessors would have proved expensive.

Carousel 5200 houses 16 3M-type tape cartridges in a removable pack and can load a cartridge into a read/write station in 2.7 sec.



Dual Intel 8080 microprocessors in the cartridge-storage system perform interfacing functions and handle routine housekeeping tasks. They also keep track of the cartridge-pack's position and optimize the pack's rotational speed as it moves to access different cartridges.

Your Single Bored Computer can be the life of the party.

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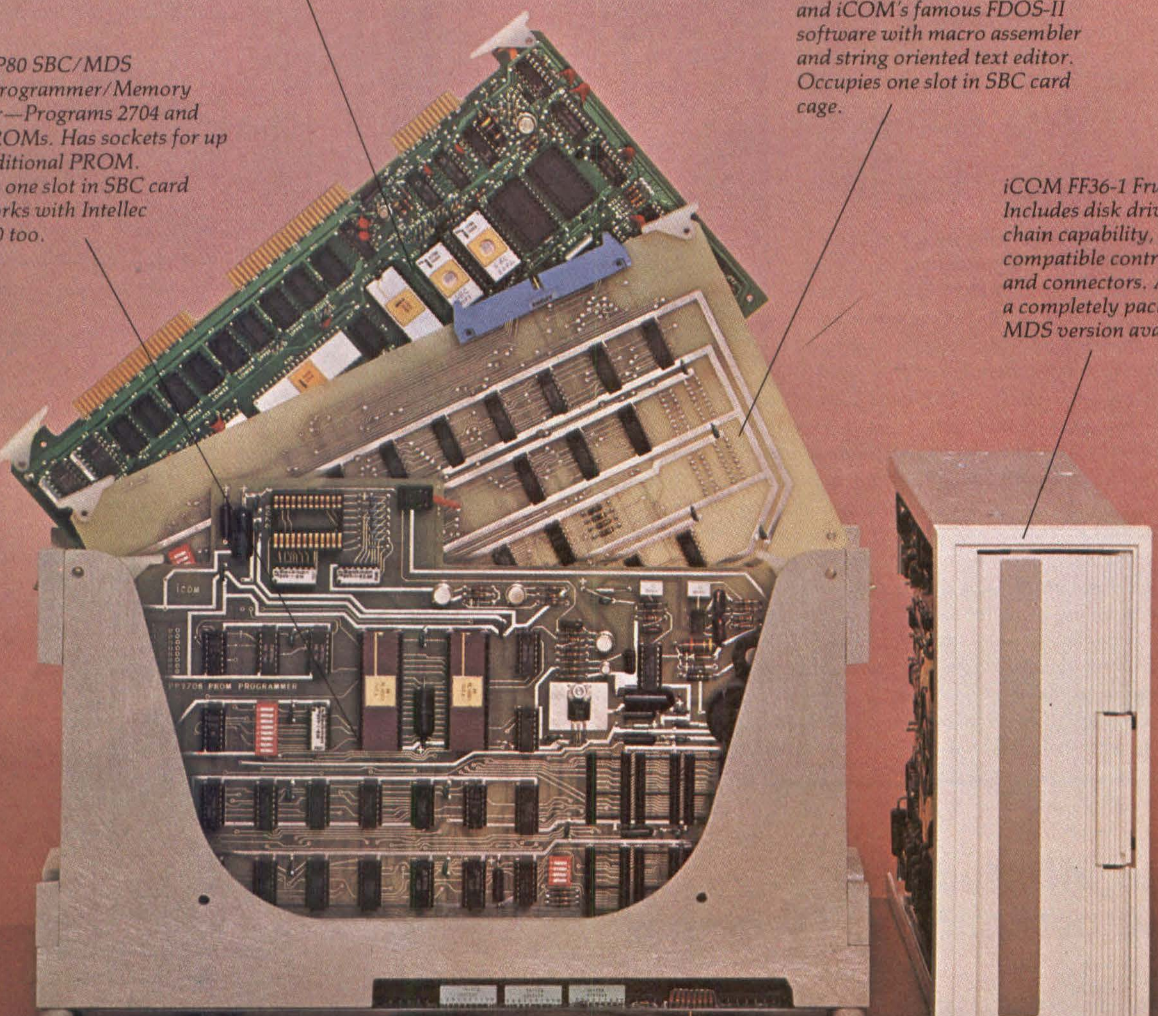

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So you have a computer on a board. Now what? iCOM has the answers with two essential Microperipherals.

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So call iCOM today.

an overspring, lower the cartridge until it is properly positioned in a slot.

A feedback mechanism warns if the cartridge is incorrectly oriented, according to Bauch. If not, the arms retract and the system forces the cartridge horizontally into a 3M-type read/write station. One system can contain up to four of these stations.

Unattended operation. The system operates unattended; it indexes, loads, processes and unloads cartridges automatically. It can thus copy data, sort files, update information and spool reports as required.

The system keeps track of the cartridge-pack's position by counting signals generated by a tooled plastic part housed on the pack's hub. Each time the part encounters one of 16 notches in the hub, it outputs a signal; by counting how many signals have occurred since generation of a "home" signal, the system can determine the pack's position. Once it knows that position, the storage system can optimize the pack's rotational speed if it must move to another position, says Bauch.

Strong fibers hasten lightwave comm

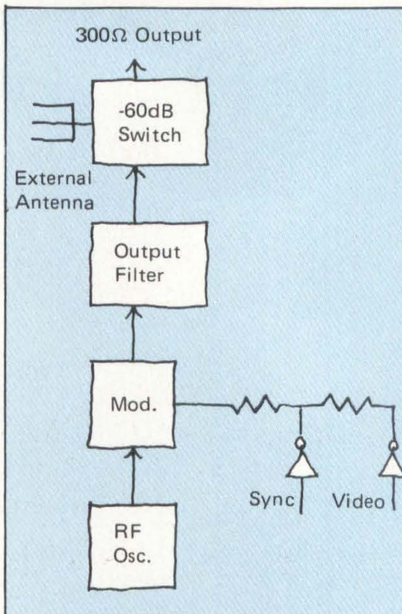
Shown supporting 5 kg in photo at left and capable of withstanding pulling forces of up to 600,000 lbs/in^2, a glass fiber developed at Bell Labs could reduce the cost of lightguides for optical communication and improve their resistance to deterioration. The development could speed the commercial implementation of lightwave communication systems. Developed primarily by Charles Kurkjian (holding fiber) and Harold Schonhorn (looking on as Hargovind Vazirani releases the 5 kg weight), the fiber's fabrication process involves reducing flaws in glass surfaces before and during fabrication and protecting each finished fiber with a coating of organic resin. The researchers first fire-polish a synthetic silica rod with an oxyhydrogen torch to remove surface defects, then soften it in a clean environment with a focused laser beam (part of the production apparatus is adjusted by researcher Tom Miller in photo at right). Drawing a continuous length of fiber from the softened rod, they immediately coat the fiber, using an applicator developed at the Murray Hill, NJ, research facility. Tests indicate the kilometer-length coated fibers – stronger than stainless steel fibers of the same diameter – could maintain their strength for years. Previous high-strength glass fibers were limited to lengths of inches and deteriorated rapidly when handled or exposed to the atmosphere.

Video interface for home computers, TV games

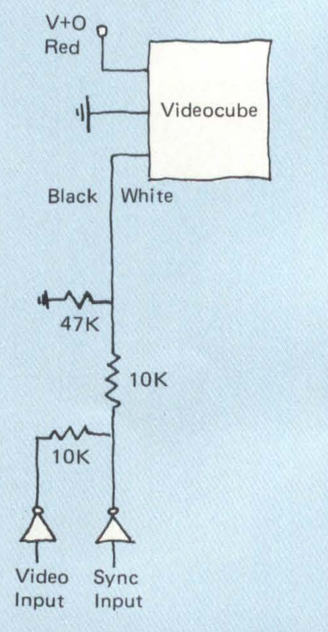
Aimed at uses in tv games, home computer systems, home closed-circuit tv and other similar applications, a self-contained interface transforms any composite video signal into a form suitable for display on a home tv screen. The Videocube's developer claims the device is the first self-contained unit that – when properly connected – meets all Federal Communication Commission (FCC) specifications for equipment that feeds signals to tv sets.

Glen Dash explains that previous interfaces have been "pieced together" from available components; their designers have "gambled" that the resulting equipment will meet the FCC specs, which Dash terms some of the strictest currently in force. The FCC grants approval only after testing a designer's work itself, not after merely examining a report on the work.

Because the Videocube is already in use in two FCC-approved tv games, future equipment that incorporates it



Video interface accepts composite video signals at any standard logic level and outputs an rf signal that can go directly to a tv's VHF input terminals.

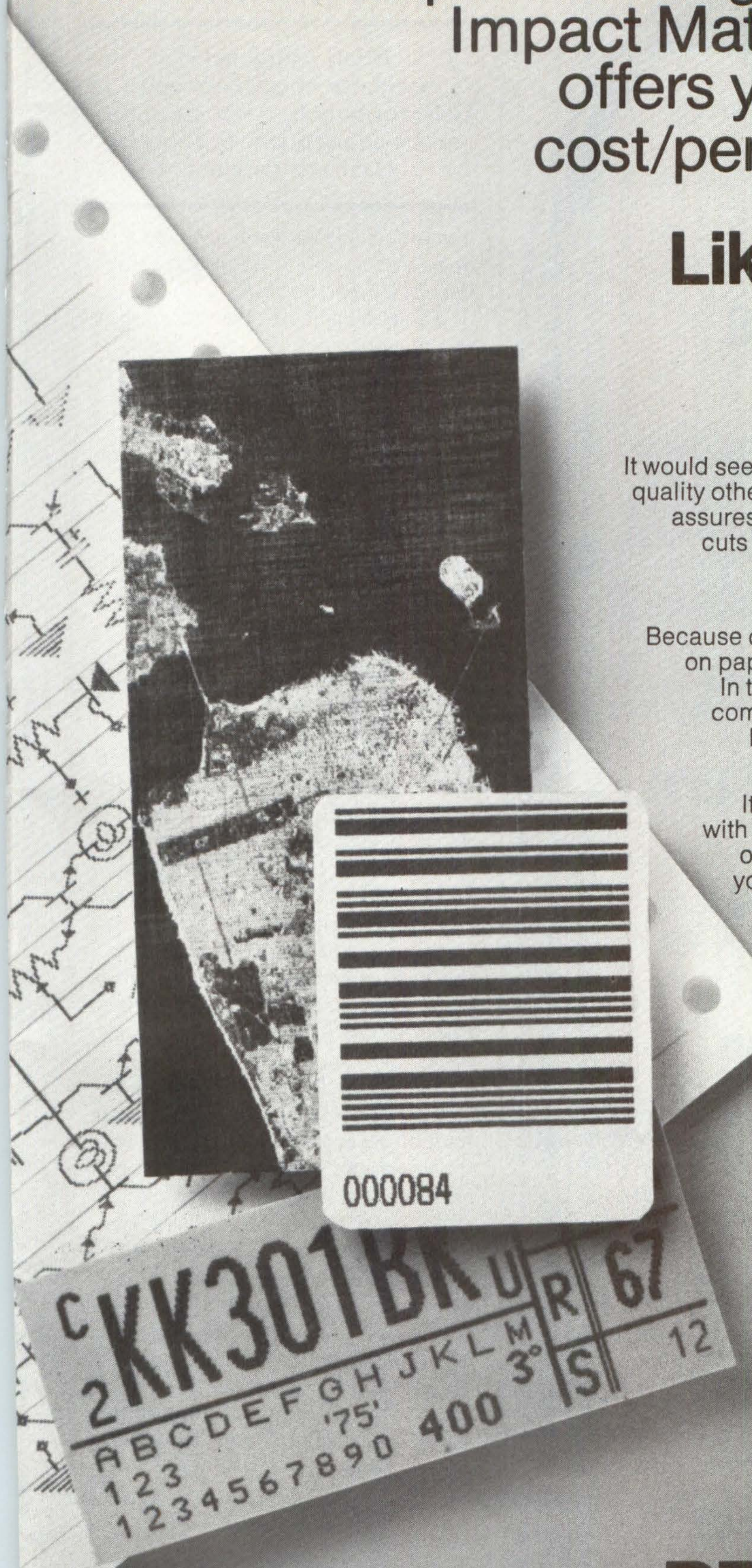


Typical application of the interface produces a black and white display. If V = +5 V, and the open-collector sync and video inputs are both low, the Videocube's output equals about 7 μV. If sync is high and video low, the output equals about 200 μV; a low sync and a high video produces about 120 μV. Changing the resistor values adjusts the relative values of these outputs.

CIRCLE 25 ▶

The concept and design of the Printronix 300 Impact Matrix Line Printer/Plotter offers you several remarkable cost/performance advantages.

Like plotting capability ...at no extra cost.



It would seem enough to find a 132 column, 300 lpm printer with print quality others can't match, with an elegantly simple mechanism that assures a greater MTBF, and a modular design that dramatically cuts MTTR. The Printronix 300 offers all of these advantages. But it also offers plotting capability. At no extra cost.

Because of its unique mechanism, it can put a single dot anywhere on paper. It forms characters a dot row at a time when printing. In the plot mode, it can form any pattern a dot at a time upon command. Drawings. Graphs. Bar codes. Large character labels. You name it and you can do it on a Printronix 300.

It's a handy capability to have around, and it comes to you with our compliments . . . at no extra charge . . . along with the other remarkable advantages that make the Printronix 300 your best buy. Send for our brochure. You'll discover why the Printronix 300 prints better, will last longer, and require far less maintenance. That's why it's been sold with a one-year warranty from the beginning.

Printronix Inc., 17421 Derian Ave., Irvine, California 92714. (714) 549-8272.

PRINTRONIX 300

It's your best buy!

should experience shorter FCC approval time, says Dash. The two current applications include a ski demonstration device manufactured by Northeast International, Marblehead, MA, and a tv hockey game developed by Executive Games, Dorchester, MA.

A self-contained rf oscillator, modulator and selector switch, the Videocube meets all pertinent FCC specs, claims its designer.

TV-tennis spinoff. The second firm also manufactures a tv tennis game, which Dash – currently chief engineer at Condat, Inc., Dorchester, MA, but assigned to the MIT Innovation Center, Cambridge, MA – helped develop while he was a student at MIT. The game incorporates Videocube-like circuitry, but only after it reached the market did Dash and his associates decide to market the Videocube as a separate 3" package.

The device consists of a self-contained rf oscillator and modulator, a -60dB selector switch for choosing between the tv set's external antenna and the modulator's output and a 300 Ω output lead that goes to the tv's VHF input terminals. Composite video signals from a game or other source go to a modulation lead; the device also requires V+ and ground connections.

Accepting signals from any type of standard digital logic or linear device, the Videocube comes in two models – one draws 62 mW @ +16 V, the other draws 35 mW @ +12 V. Both units interface to tv channel 3.

Typical application. In one typical circuit, a 47 KΩ resistor sets the white level of the unit's output. That is, when the interface's sync and video inputs are both low, its white lead goes to ground only through the resistor; the Videocube then outputs about 70 μV.

When the sync input goes high, the output jumps to about 200 μV, and with a high video input and a low sync input, the interface's output measures 120 μV. Changing the resistor values adjusts the relative values of output at sync, dark screen and light screen, according to Dash.

COMING NEXT MONTH

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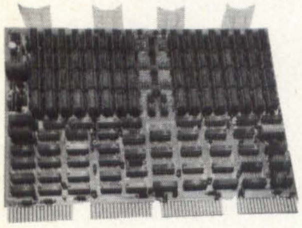

MSC 4501
January

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Requires 75% less power than equivalent core memories (8K words requires only 0.6A at +5 volts DC).

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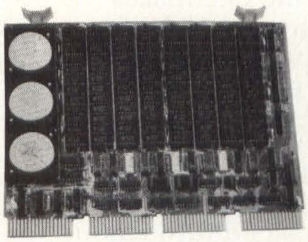

MSC 3201
February

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Up to 64K words, with or without parity, in a hex wide "SPC" slot.

Totally PDP-11/04/34 hardware and software compatible.

Expandable in 4K increments to 16K words, and in 16K increments to 64K words.

One year warranty on parts and labor.

$1495* (16K words) single quantity. OEM discounts available.

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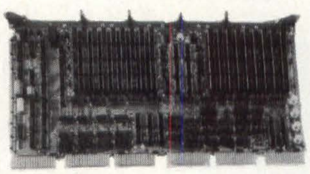

MSC 3501
March

CIRCLE 28 CIRCLE 29 CIRCLE 30

Multi-level, μP-based traffic-control system helps clear jammed Dutch intersections

At some crowded metropolitan intersections, playing in traffic is safe, because traffic hardly ever moves. And the unpredictability of traffic-flow changes can often stymie hardwired traffic-control hardware, which can only cope with a limited number of traffic conditions.

Faced with these problems, traffic-control engineers in The Netherlands installed a microprocessor based control system at six intersections near Eindhoven. Displaying recommended speeds on successive advisory signs, the system allows drivers to move "into step" with the green-light cycles of successive intersections; the signs also warn motorists if they must stop at an intersection to regain phase with the green cycle.

Because one of the six intersections experiences especially heavy traffic with highly unpredictable patterns, the engineers provided it with a separate microprocessor based controller that interfaces with the supervisory control system. The intersection controller allows traffic-dependent changes in the crossing's control sequences, unlike the hardwired system it replaced.

Subject to wide and almost unpredictable variations in traffic volume, sequential intersections like this one are ill-suited to control by inflexible, hardwired traffic systems. A microprocessor based system, however, can react readily to such intersections' constantly changing traffic conditions. ***(Courtesy Philips Telecommunication Review)***

Revamping that hardwired system to cope with the intersection's growing traffic volumes would have been expensive and wouldn't have provided the necessary operating flexibility, according to Philips Telecommunicatie Industrie. Indeed, before installing the μP-based controller at the unpredictable intersection, the engineers had contemplated scrapping all cyclic traffic controls and trusting that any jams that developed would eventually correct themselves.

Solutions lack uniformity. The design of Philips' all-purpose traffic control system, of which the Eindhoven controllers form one configuration, grew out of several considerations, explain C. J. Krayenbrink and A. Vlaanderen, who note in the *Philips Telecommunication Review* that the philosophy of traffic control has evolved from an emphasis on safety and junction capacity to a more general emphasis on traffic management. Hardware must conform to a variety of requirements that depend on the relative importance traffic engineers give to such factors as minimization of wait and travel times, priorities for mass transit, pedestrians and cyclists, and environmental considerations.

One approach to dealing with these requirements uses a centralized, general-purpose computer hooked to controllers at each intersection. But complicated intersections require complicated communication links with this computer, and if the computer fails, all attached intersection controllers also fail.

Aware of these drawbacks, the Philips engineers formulated design goals for their control system that included:

★ Suitability to a variety of control and supervision functions

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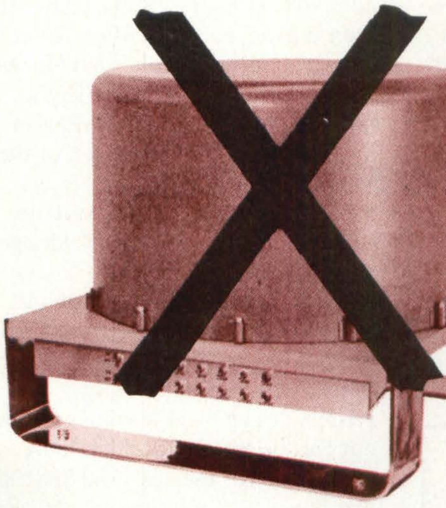

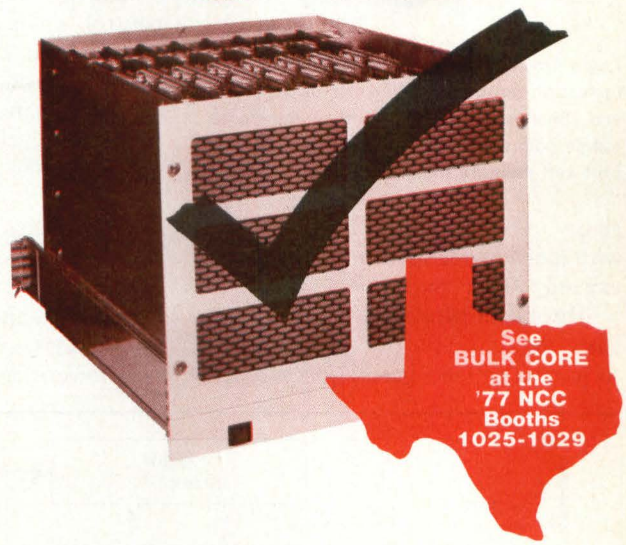

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CIRCLE 31

★ Ease of programming and reprogramming
★ Modularity to allow implementation of control functions either at local, district or area levels
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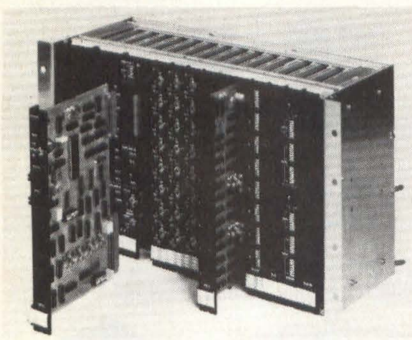


Logic frame in a microprocessor based intersection controller incorporates processor and supervisory cards as well as interfaces, a data communication card, a phase control unit and memory cards.

ability to build a system that starts with individual intersections and can expand to area control.

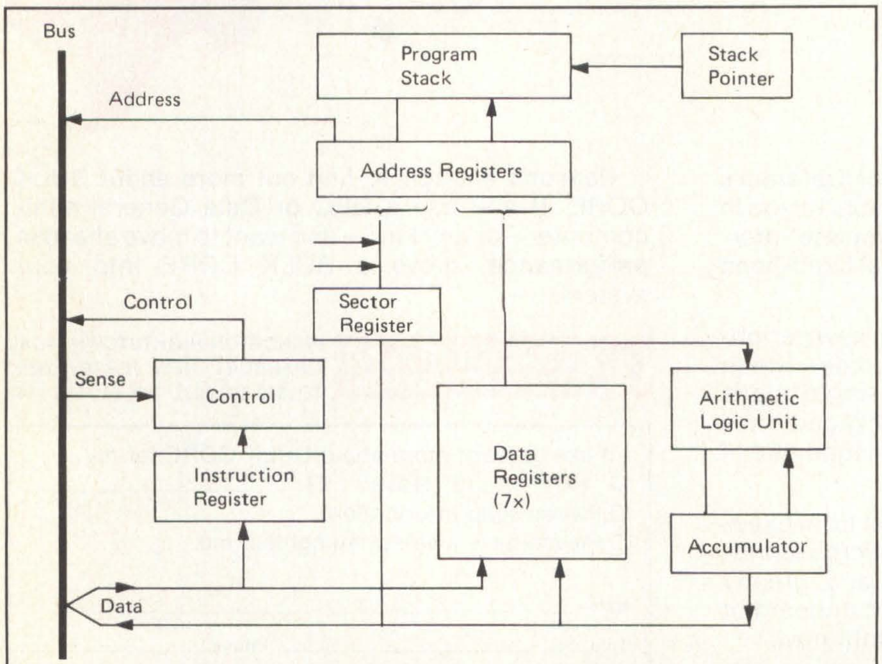
Three configurations. To meet these goals, the traffic-control system incorporates an 8-bit parallel microprocessor with a 52-instruction set. The microprocessor can address up to 16K bytes of memory and requires about 6μs to process an average instruction in a traffic-control program.

With the appropriate programming and modular hardware, the unit can function either as an intersection controller, a sub-area master controller that oversees several intersection controllers, or an area controller that supervises several sub-area masters.

Split software. To accommodate a variety of control philosophies, the system's designers split its software package into two parts: a standardized "instrument program" and customer oriented "traffic data tables" generated from intersection information provided by traffic engineers. The instrument program, which contains subroutines that implement the system's control actions, further divides into four heirarchical levels.

The highest of these levels – macro control – uses the information in the data tables to generate an intersection's basic traffic-control program; it passes such information as plan number, control mode, cycle-time offset and stage number to the next lower level – micro control.

At the micro control level, the system generates on/off commands for each phase within an operating stage. Classified as either "forced" or "request," these commands go to the next lower stage – phase control – where they are transformed into forced commands after adjustments for such factors as green timing and clearance times. At the lowest level – output control – these forced commands then switch the intersection's traffic lights and maintain the system's safety factors.



Processor unit in the intersection controller executes an average traffic-control instruction in 6 μs. An 8-bit parallel machine with a 52-instruction set, the microprocessor system can address up to 16K bytes of memory. *(Courtesy Philips Telecommunication Review)*

Intel's 8085: a critical assessment

"The 8085 is a clear advance on the 8080A. It has a single power supply, runs 50% faster, uses one package instead of three, has a better interface and better interrupt capability. It is directly program compatible with the 8080A, and because, apart from minor exceptions, instructions take the same number of clock cycles, any program optimization will still be valid."

This assessment of the capabilities of Intel's recently announced 8085 microprocessor, and the MCS-85 microcomputer system it heads, comes from Iann Barron, editor of *Microcomputer Analysis* (subscriptions from Mackintosh Publications, Victoria House, Victoria St., Luton LU1 5DH, England). In his December 1976 rundown of the system, he concludes that:

★ Users with small 8080A systems should consider immediate redesigns with the 8085;
★ Users with large 8080A systems shouldn't consider such redesigns unless performance or tolerancing limitations force them to;
★ Users designing new systems should opt for the 8085 over the 8080A.

System bus the key. The 8085's system bus, which multiplexes data and address lines, forms the key development in the new MCS-85 system, according to Barron. The bus reduces pinout count on the 8085 and other system components; it incorporates the bus control and clock logic that in the MSC-80 microcomputer system require two additional devices, the 8224 and the 8228. Bus timing has been improved, so storage is used more efficiently than in the MCS-80. And the bus is directly extendable to 16 bits; it will "clearly be the Intel standard for some years to come."

The bus operates under the control of a single-phase, 3-MHz clock, compared with the 8080A's 2-phase, 2-MHz clock. Eight data lines multiplex with the microprocessor's eight low-order address lines. Control signals and timing are different compared with the 8080A; status signals define the type of interface transfer, and the 8085's busy-signal logic has been improved. The 8085 also has extended interrupt facilities and provides "rudimentary" serial input and output; it presents a "rational" pinout sequence, claims Barron.

User impact. Intel's switch to a single-phase clock will have little effect on users, because the properties of the

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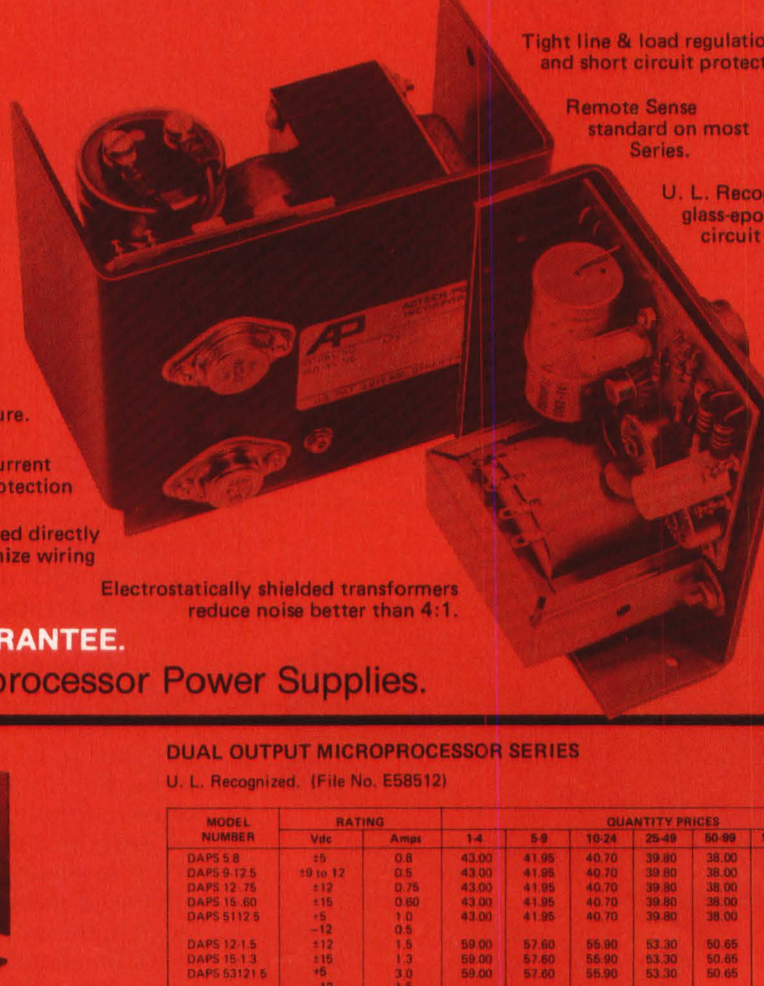

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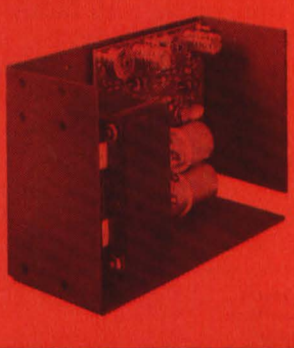

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	Vdc	Amps	1-4	5-9	10-24	25-49	50-99	100-249	250-499
DAPS 5-8	±5	0.8	43.00	41.95	40.70	39.80	38.00	36.80	33.00
DAPS 9-12.5	±9 to 12	0.5	43.00	41.95	40.70	39.80	38.00	35.80	33.00
DAPS 12-.75	±12	0.75	43.00	41.95	40.70	39.80	38.00	35.80	33.00
DAPS 15-.60	±15	0.60	43.00	41.95	40.70	39.80	38.00	35.80	33.00
DAPS 5112.5	+5 −12	1.0 0.5	43.00	41.95	40.70	39.80	38.00	35.80	33.00
DAPS 12-1.5	±12	1.5	59.00	57.60	55.90	53.30	50.65	47.60	43.80
DAPS 15-1.3	±15	1.3	59.00	57.60	55.90	53.30	50.65	47.60	43.80
DAPS 53121.5	+5 −12	3.0 1.5	59.00	57.60	55.90	53.30	50.65	47.60	43.80

REGULATION: ±0.05% Line, ±0.1% Load. RIPPLE (PK/PK) 3mV.

DIMENSIONS: (Small unit) 4"x2.75"x4.87" (Large Unit) 7"x3.40"x4.87"

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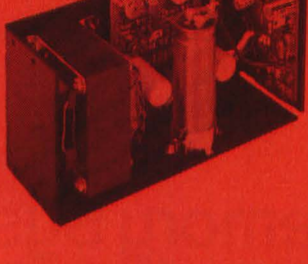

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MODEL NUMBER	RATING		QUANTITY PRICES						
	Vdc	Amps	1-4	5-9	10-24	25-49	50-99	100-249	250-499
TAPS 1	5V ±9 - 12*	4.0 0.5	94.15	91.85	89.20	85.05	80.85	75.90	71.00
TAPS 2*	5V ±9 - 12*	6.0 1.0	107.00	104.60	101.60	96.85	92.10	89.00	87.50
TAPS 3	5V ±9 - 12*	9.0 1.5	137.00	134.00	129.80	127.80	125.00	123.75	113.85
TAPS 4	5V ±9 - 12*	12.0 3.0	163.00	159.00	154.45	151.50	149.00	148.00	147.00

* Also available with ±12-15V output. Specify if desired.

REGULATION: ±0.1% Line, ±0.1% Load. RIPPLE (PK/PK): 5mV

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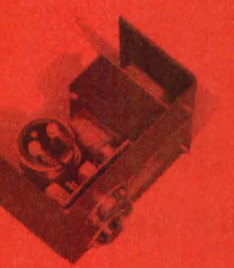
MODEL NUMBER	RATING		REGULATION		RIPPLE (PK/PK)	OVP MODEL SUFFIX	PRICES-ALL MODELS		
	Vdc	Amps	Line	Load			QTY	POWER SUPPLY	OVP UNIT
APS 5-3*	5	3	±0.05%	±0.1%	3mV	OV1-53	1-4	34.00	7.00
APS 6-2.5	6	2.5	±0.05%	±0.1%	3mV	OV1-63	5-9	33.15	6.90
APS 12-1.6*	12	1.6	±0.05%	±0.1%	3mV	OV1-122	10-24	32.20	6.70
APS 15-1.5*	15	1.5	±0.05%	±0.1%	3mV	OV1-152	25-49	30.70	6.40
APS 20-1	20	1.0	±0.05%	±0.1%	5mV	OV1-201	50-99	29.20	6.05
APS 24-1*	24	1.0	±0.05%	±0.1%	5mV	OV1-241	100-249	27.00	5.70
APS 28-0.8*	28	0.8	±0.05%	±0.1%	5mV	OV1-281	250-499	25.20	5.25

DIMENSIONS: 4" x 2.75" x 4.87 REQUEST BULLETIN APS-277



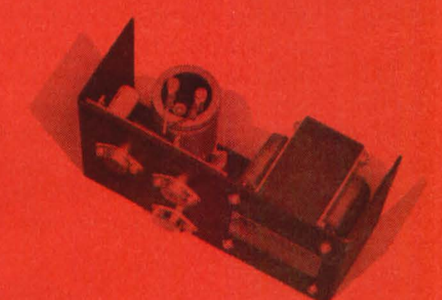
30 TO 60 WATT "GREEN HORNET" SERIES. SINGLE OUTPUT

† U. L. Recognized (File No. E58512)

MODEL NUMBER	RATING		REGULATION		OVP MODEL SUFFIX	POWER SUPPLY PRICES			OVP PRICES
	Vdc	Amps	Line	Load		QTY	APS 48-1	ALL OTHERS	
APS 5-6†	5	6.0	±0.05%	±0.1%	OV2-56	1-4	68.00	55.00	15.00
APS 6-5	6	5.0	±0.05%	±0.1%	OV2-65	5-9	66.70	53.65	14.85
APS 12-4†	12	4.0	±0.05%	±0.1%	OV2-124	10-24	64.75	52.10	14.40
APS 15-3†	15	3.0	±0.05%	±0.1%	OV2-153	25-49	61.75	49.65	13.75
APS 20-2.4*	20	2.4	±0.05%	±0.1%	OV2-203	50-99	58.75	47.25	13.05
APS 24-2.2*†	24	2.2	±0.05%	±0.1%	OV2-245	100-249	55.15	44.35	12.25
APS 28-2 *†	28	2.0	±0.05%	±0.1%	OV2-284	250-499	50.75	42.00	11.30
APS 48-1 *	48	1.0	±0.05%	±0.1%	OV2-481	500-999	49.60	40.00	11.05

* RIPPLE: (PK/PK) 5mV. All others 3mV.

DIMENSIONS: 5.62"x3.40"x4.87" REQUEST BULLETIN APS-277



50 TO 120 WATT "BLACK BEAUTY" SERIES. SINGLE OUTPUT

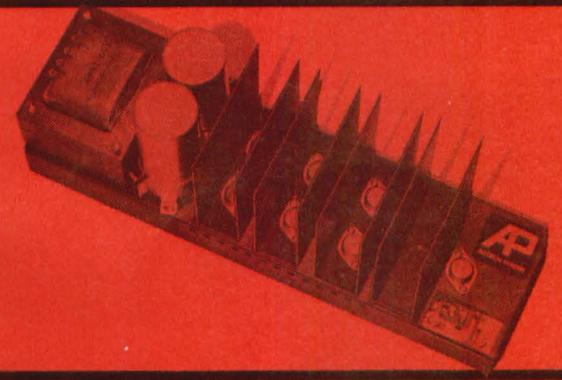
5 Vdc @ 9 Amps to 28 Vdc @ 4 Amps. U. L. Recognized. (File No. E58512) *

MODEL NUMBER	RATING		OVP MODEL SUFFIX	POWER SUPPLY PRICES					OVP PRICES
	Vdc	Amps		QTY.	APS 5-9	APS 5-12	APS 5-18	ALL OTHERS	
APS 5-9	5	9	OV2-510	1-4	71.00	85.00	108.00	75.20	15.00
APS 5-10*	5	10	OV2-510	5-9	68.75	82.95	104.50	73.40	14.85
APS 5-12	5	12	OV2-512	10-24	66.74	80.55	101.45	71.30	14.40
APS 5-18	5	18	OV2-518	25-49	63.90	76.80	96.70	67.95	13.75
APS 12-7*	12	7	OV2-127	50-99	61.05	73.00	91.95	64.60	13.05
APS 15-6*	15	6	OV2-156	100-249	57.30	68.55	86.35	60.65	12.25
APS 24-5*	24	5	OV2-245	250-499	52.75	65.00	79.45	55.80	11.30
APS 28-4*	28	4	OV2-284	500-999	51.60	57.90	77.70	54.60	11.05

REGULATION: Line ±0.05% Load ±0.1%. RIPPLE (PK/PK): 3mV on 5, 12, 15V models, 5mV on 24, 28V.

DIMENSIONS: 9"x3.65"x4.87"

APS 5-18 DIMENSIONS: 14"x3.65"x4.87" REQUEST BULLETIN APS-277



125 TO 250 WATT "BLUE MAX" SERIES. SINGLE OUTPUT

5 Vdc @ 25 Amps to 28 Vdc @ 9 Amps.

MODEL NUMBER	RATING		REGULATION		OVP MODEL SUFFIX	POWER SUPPLY PRICES			OVP PRICES
	Vdc	Amps	Line	Load		QTY	APS 5-30	ALL OTHERS	
APS 5-25	5	25	±0.05%	±0.0.1%	OV3-525	1-4	163.00	158.00	25.00
APS 5-30	5	30	±0.05%	±0.0.1%	OV3-530	5-9	159.25	154.40	24.50
APS 6-22	6	22	±0.05%	±0.0.1%	OV3-622	10-24	154.65	149.95	24.25
APS 12-17	12	17	±0.05%	±0.0.1%	OV3-1217	25-49	147.45	142.95	23.15
APS 15-15	15	15	±0.05%	±0.0.1%	OV3-1515	50-99	140.20	135.90	22.00
APS 20-11	20	11	±0.05%	±0.0.1%	OV3-2011	100-249	131.65	127.60	20.65
APS 24-10	24	10	±0.05%	±0.0.1%	OV3-2410	250-499	121.10	117.40	19.00
APS 28-9	28	9	±0.05%	±0.0.1%	OV3-289	500-999	118.50	114.85	18.60

RIPPLE (PK/PK): 3mV on 5,6,12,15V models, 5mV on 20,24,28V models.

DIMENSIONS: 16.72"x4.87"x6.60" Max. APS 5-30 only. All others 16. 72"x4.87"x5.75".

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CIRCLE 35

8080A's 2-phase clock have remained hidden by that microprocessor's 8224 clock generator, says Barron. But deglitching a fully synchronous bus driven from a regular clock is theoretically impossible, a property that could cause problems in systems with a high proportion of DMA or interrupt operations, or in which several independent microprocessors interconnect.

The microprocessor's multiplexed bus reduces pinout count but requires 31 timing-tolerance specifications.

One disadvantage of the multiplexed bus lies in the need to demultiplex to accommodate devices that require a constant address throughout an interface transfer, continues Barron. But as Intel extends the MCS-85 system, this disadvantage should decline in importance.

Currently, designers who require demultiplexing can use the 8212 8-bit I/O port, strobed by the 8085's ALE signal. The port introduces a 30-ns address-line delay and reduces the 8085's nominal maximum access time from 575 ns to 545 ns for 3-MHz operation. But overall, "the use of a multiplexed bus provides little performance penalty to microcomputers."

Timing complexities. Barron is highly critical of the large number of timing tolerances (31) specified for the 8085 system bus: "It is really quite unsatisfactory (and unnecessary) to have as many arbitrary timings in an interface. It costs money to the vendor, who commits himself to measure and maintain a large number of parameters, and it costs money to the user, because it makes the interface difficult to comprehend and systems hard to design."

And Intel has neglected to specify three "key" timings, he claims:

★ The relationship between the rising edge of ALE and a valid address on the bus, required when the front edge of ALE gates an address;

★ The relationship between the clock and the valid address on the bus (or the rising edge of ALE), required if the addressed device must use the clock as a basis for its timings;

★ The switching time of the 8085's IO/M, S0 and S1 interface signals, which many devices must use to determine the type of interface transfer.

Overall marks: good. Still, says Barron, "the timing relationships on the 8085 are far more uniform than on the 8080A, the majority apparently being related to the falling edge of the clock rather than to arbitrary internal timings within the microprocessor."

Summarizing his overall assessment of the 8085 interface as "a considerable step forward," Barron offers these thoughts:

■ *Efficiency:* "The use of a multiplexed bus provides a useful reduction in pinout count, thereby freeing pinouts for other purposes . . . This should give the 8085 a competitive advantage in small systems . . . "

■ *Compatibility:* "The 8085 is broadly compatible with the 8080A combination. However, the changes in control signals and bus timings would necessitate considerable redesign of existing systems that use the 8080A combination. Also, the 8085 bus has less drive capability than the 8080A combination. Compatibility really means that the 8085 can use components from the 8080A (family), not that the 8085 can replace the 8080A combination in current designs."

■ *Speed:* "The 8085 bus is considerably more efficient than the 8080A combination . . . At 3 MHz, the 8085 can operate at full speed using standard 450-ns store, whereas the 8080A-1 would require 250-ns store and be more difficult to engineer . . . Selected faster versions of the 8085 should be practical, operating at rates up to 5 MHz or beyond."

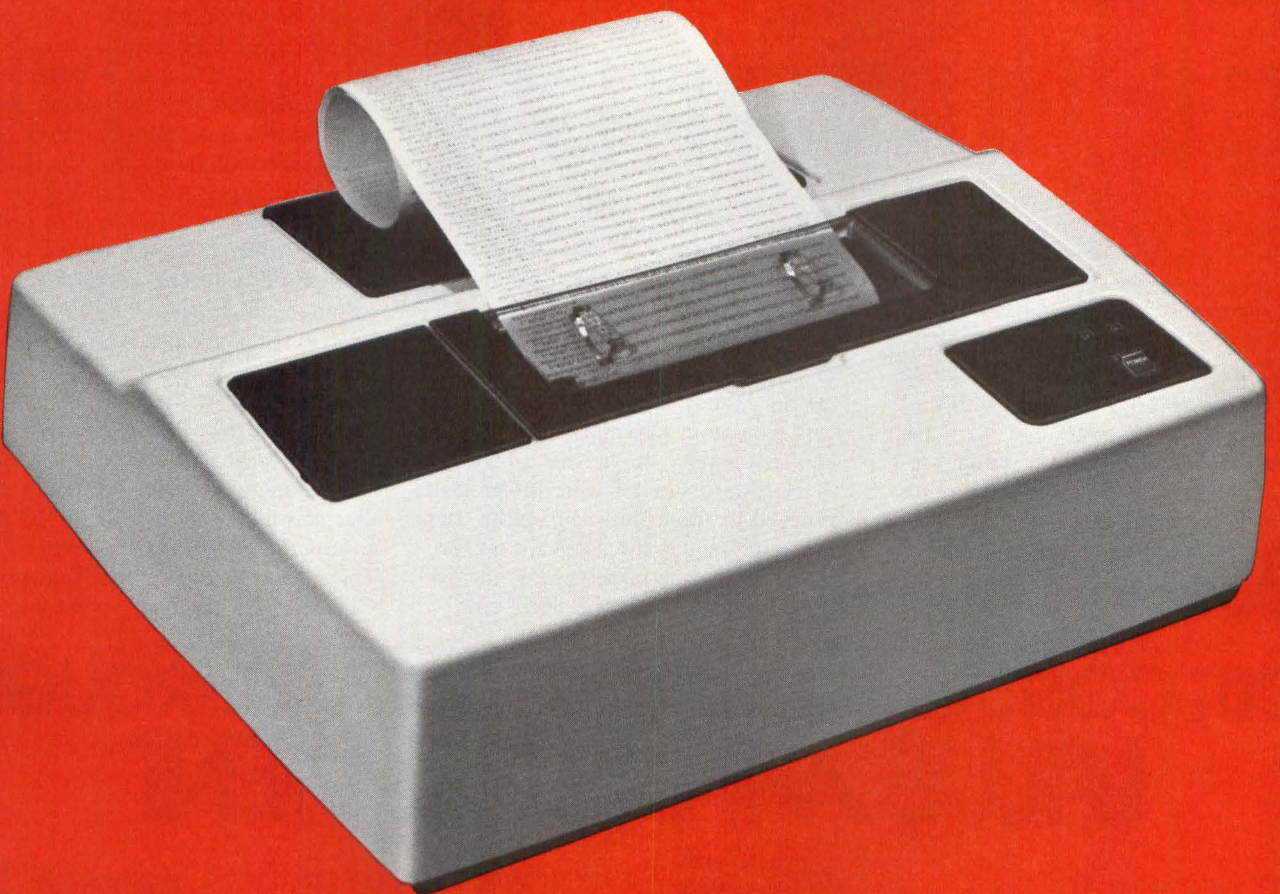
With master/slave CPU architecture, development system serves several CPUs

To allow microprocessor-system designers to choose between several CPUs, an instrument manufacturer has recently unveiled two microprocessor development systems that accommodate both Intel 8080 and Motorola 6800 microprocessors. The firm will provide development capability for the Zilog Z80 late this summer, and it will also support new microprocessors as they appear.

Key to the Tektronix 8002 μP Lab – and its less extensive 8001 counterpart – is a master/slave CPU architecture that allows the systems to emulate different microprocessors with no hardware reconfiguration other than the change of a slave CPU and emulator cable. The 8002 system can simultaneously accommodate up to three such slave CPU cards, each emulating a different microprocessor.

Microprocessor-system developer enters and edits programs on a Tektronix 8002 μP Lab. By changing a slave CPU card and an in-circuit emulation cable (visible in front of the development system's dual floppy-disk drives), the user can develop software and integrate it with hardware for both 8080- and 6800-based systems; future cards will accommodate the Z80 and other microprocessors.

New serial unitized "RO" high speed thermal printer



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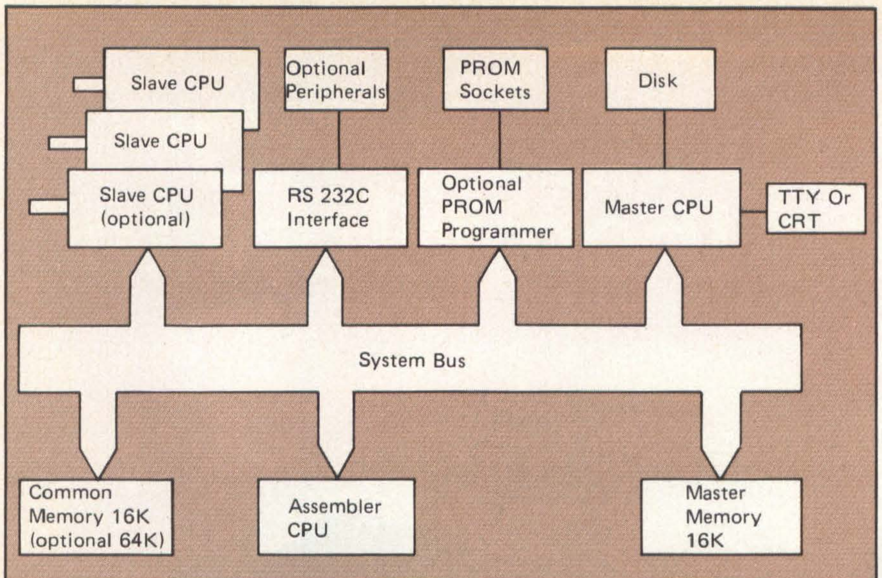
Terminal Systems Division — Ithaca

CIRCLE 36



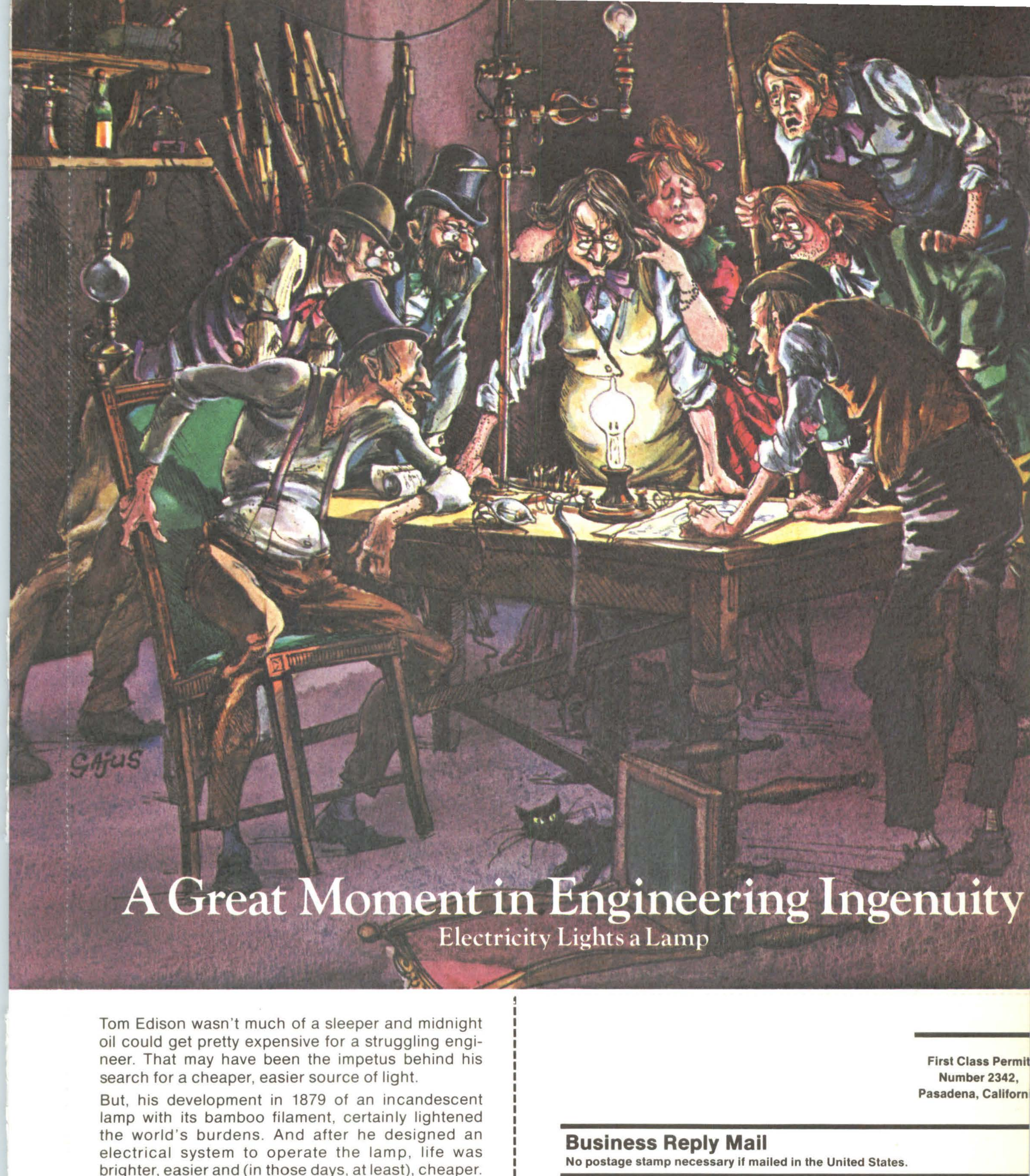
A Signetics 2650 constitutes the development system's master CPU; a Zilog Z80, its assembler CPU, helps optimize program assembly time.

Three-level integration. According to the Beaverton, OR, firm, with the 8002 a user can create and maintain files on dual floppy disks, enter programs on a system console, edit those programs, assemble the source language into object code and store that code on disk. A slave CPU board lets the user trace the object code, set breakpoints and examine registers or memory, and its cable allows in-circuit emulation of a microprocessor and its memory in the user's hardware.

Hardware and software integration proceed in three steps. First, the user runs and debugs the software on the slave CPU – the same type as in the user's system. Next, the 8002 emulates the prototype microprocessor and memory while input and output functions utilize the prototype hardware through the in-circuit emulation cable. Finally, the user can program the object code in 1702 or 2704/2708 PROMS, using an optional built-in programmer; the system then runs the program under slave CPU control to provide trace, breakpoints and memory and register examinations.

A hardware trace option also lets the user trace logic transactions in the prototype hardware and the development system's address and data buses in real time, adds the firm.

System configurations. The 8002 consists of a mainframe and power supply, plus a dual floppy-disk system and controller that can support up to four disk drives. The mainframe incorporates a Signetics 2650 master CPU, a 16K dynamic RAM master memory, a 16K dynamic RAM common memory (expandable to 64K), a debug and front-panel I/O board, a Z80 CPU board to control assembly and a communications interface board that provides three RS 232C I/O ports and memory map for the slave CPUs. The system accepts either Tektronix's CT8100 CRT terminal or the user's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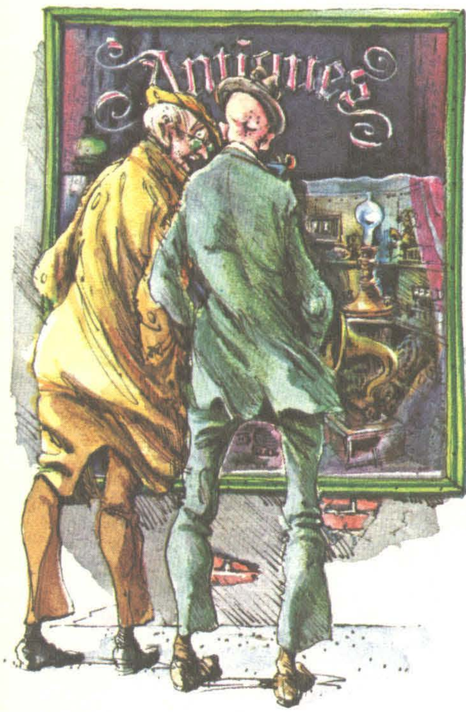

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All the most popular standard codes; choice of red or white LED lighting; ten dial positions; completely interchangeable with other space-saving switches currently on the market . . . and with all the high-quality features for which Digitran is famous. *Great!* (Of course, the bad news is that practically every other lighted switch on the market is now obsolete.)

The new series 43000 MINISWITCH is a half-inch wide back-mounted modular switch with all the advantages of our traditional better approach to switching plus "snap-together" construction.

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With LED-lighted MINISWITCHES, you can make your designs a glowing success.

Maybe even have your own Great Moment.

See pages 2720-2725 of 1976-77 EEM Directory for more Digitran product information.

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RS 232-compatible terminal.

For users with facilities for program development and assembly, the 8001 provides the in-circuit emulation features of the 8002 but doesn't allow source code entry and assembly; its operating system is stored in ROM rather than on floppy disk. A user can upgrade an 8001 to an 8002 by adding a master memory card, an assembly CPU card, a floppy-disk drive and disk operating software.

Assembler commonality. That operating software, dubbed Tekdos, is specifically tailored for multiple CPU architecture, according to Tektronix.

The floppy-disk-stored system has its own protected memory and includes

★ File management with utilities
★ An interactive text editor
★ A system-readiness test
★ A relocatable macro assembler for one microprocessor, selectable at time of purchase.

Table-driven, the relocatable macro assembler allows assembler commonality for the microprocessors served by the system, says Tektronix. And if the user makes changes in a source code program, only the routines affected need be reassembled into object code.

Bubble memory suits portable storage, serves smart terminals, word processing

A mass storage, non-volatile 92,304-bit magnetic bubble memory heads the list of seven new high technology, solid-state memory circuits announced today by Texas Instruments:

- The bubble memory;
- A 65K-bit charge-coupled device (CCD) memory;
- A 16,384-bit ultraviolet-light erasable, electrically-programmable read-only memory (EPROM);
- A dynamic high performance MOS RAM; and
- Four fully static MOS random-access memories.

Designated the TBM0103, the magnetic bubble memory features high packing density and low access time for reliable solid-state mass storage. Modularity, provided by a single chip package, allows low entry price of $200 coupled with packaging flexibility and efficiency.

A custom MOS controller is available to provide microprocessor compatibility and a family of interface integrated circuits is in development with prototype availability scheduled for late 1977. The magnetic bubble memory system is suited for portable storage.

Applications include intelligent terminals, programmable calculators, data loggers, word processing, voice storage, measurement and test equipment and disk memory replacement in commercial and military equipment.

The 92K-bit bubble chip is comprised of a gadolinium-gallium garnet substrate upon which a magnetic epitaxial film is grown. The diameter of the magnetic bubble domains is five microns. Patterns of permalloy metal are deposited on the epitaxial film to define the path of the bubble domains in the presence of a rotating magnetic field. As the field rotates, the bubble domains move under the permalloy pattern in shift register fashion.

Device architecture is major loop/minor loop. Data bits are written into and read out of the major loop; data bits are transferred to minor loops for storage. A total of 157 minor loops, each consisting of 641 bubble positions, results in a single chip memory storage capacity of 100,637 bits. However, a maximum of any 13 of the 157 minor loops on the chip is allowed to be defective. Therefore, the minimum data capacity of the remaining 144 good loops is 92,304 bits. Bubble control functions such as generate, transfer in, transfer out, replicate and annihilate are executed by providing current pulses through the appropriate control elements on the chip.

The bubble memory is packaged in a 14-pin dual-in-line module measuring 1.0 x 1.1 x 0.4 inches. The module contains a 92K-bit-bubble chip surrounded by two orthogonal coils that provide the rotating magnetic field, a permanent magnet set and a magnetic shield to protect data from external fields.

Performance specifications at 100 kilohertz operation are access time of four milliseconds for the first bit, cycle time for the 144 bit page of 12.8 milliseconds, and an approximate power consumption of one half watt for continuous operation. Operating temperature initially is 0° to 50°C with a nonvolatile storage range of -40° to 85°C.

The 65K-bit charge-coupled device (CCD), designated the TMS3064, is organized externally as 65,536 1-bit words and internally as 16 addressable 4096-bit serial-parallel-serial (SPS) loops.

A new two-phase coplanar electrode CCD structure, developed by TI, is combined with the standard double poly N-channel silicon-gate MOS process to fabricate the device. This CCD structure uses ion implant storage wells allowing the simple two-phase non-overlapping clock. The two clock and the chip enable inputs can be driven by standard MOS-level drivers.

All other inputs have 200 millivolts of dc noise immunity when interfacing with standard TTL. No pull-up resistors are required. The three-state output will drive at least two standard series 74, 74S or 74LS loads without the use of pull-up resistors.

The maximum data rate is 5 megabits per second. Maximum access time (at 5 megahertz) is 800 microseconds. The TMS3064 has a typical operating power dissipation of 300 milliwatts at 5 megahertz and a standby power dissipation of less than 30 milliwatts. The memory comes in a 16-pin ceramic dual-in-line package with pin rows on 400-mil centers. Designed for operation over a 0°C to 70°C temperature range the TMS3064JL has a single-piece price of $195.

Designated the TMS2716, the EPROM is a direct plug-in replacement that doubles the capacity of TI's 8,192-bit TMS2708 and TMS27L08 as well as other 2780s currently on the market, and one TMS2716 dissipates less total power than most 2780s with half the memory capacity.

The TMS2716 has the same package and pin-outs, the same basic chip design and circuitry, the same power supplies and power requirements so that the new 16K-bit device may be plugged into all existing 2708 sockets.

Other TMS2716 features include:

- Production proven N-channel silicon-gate technology for ready availability.
- Low power consumption, 375 mW typical.
- Guaranteed dc noise immunity in both high and low states so that all inputs can be driven by series 74 TTL circuits without use of external pull-up resistors.

The memory circuit, organized as 2048 words of 8-bit length, is designed for high-density, fixed-memory applications requiring low power dissipation, fast turnarounds, and/or program changes. Maximum access and minimum cycle times are 450 nanoseconds. The data outputs of the TMS2716 are three-state for OR-tying multiple devices on a common bus.

The EPROM can be erased by exposing the chip through the transparent quartz lid to high-intensity ultraviolet light. Existing PROM/EPROM programmers can be used with the TMS2716 since it has the same programming characteristics as the 2708s now in common use. The TMS2716JL is supplied in a 24-pin dual-in-line ceramic package designed for insertion in mounting-hole rows on 600-mil centers and operates for 0°C to 70°C. It is available now at $54.75 each in 100s.

The high-performance 4096-bit, 16-pin dynamic RAM expands TI's line of dynamic memories to 14 devices, making TI a supplier with 4K dynamic RAMs in 16, 18 and 22-pin versions.

Designated the TMS4027, the new

RAM features:

- 150 nanosecond access time, 320 nanosecond cycle time;
- $\pm$ 10% power supply tolerance (+12V, $\pm$5V);
- Low power 460 mW active, 27 mW standby (maximum);
- Common I/O capability;
- Gated RAS, RAS-only refresh, and page-mode capability;
- Input latches for addresses, chip select, and data in;
- Three-state TTL-compatible high-drive outputs;
- Output data latched and valid into next cycle.

The TMS4027, a 4096 word x 1 bit MOS random access memory fabricated with TI's N-channel silicon-gate process, uses a single transistor storage cell with new dynamic storage and control circuits, achieving high performance and low power dissipation. The multiplexing/latching of address inputs allows it to be packaged in a 16-pin 300 mil-pin-row DIP, reducing memory board space requirements by 40 percent over 22-pin packages.

System advantages of using the TMS-4027 include: direct interfacing with TTL, elimination of external interface register, reduction of address lines to only six low-capacity lines, increased noise immunity, and a choice of two chip-select methods, and the ability to add read-modify-write page mode, or RAS only refresh modes. Price: $19.20 in 100 piece quantities.

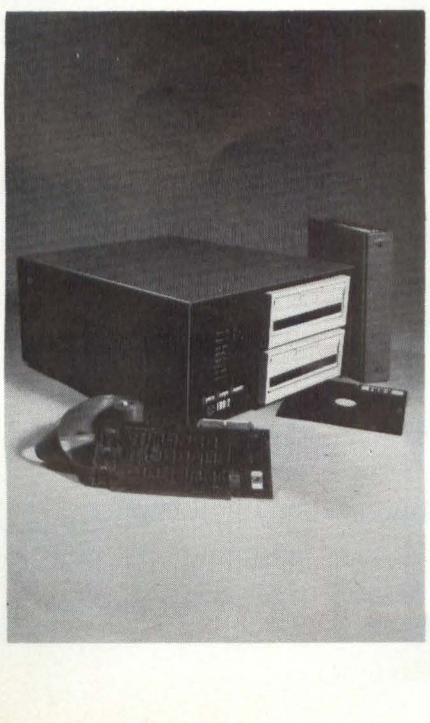
The four fully static random access memory (RAM) circuits are designated TMS4044 and TMS4047 (organized 1024 x 4). Each type comes in four speed ranges: 450, 300, 200 and 150 nanosecond maximum access times. Since the RAMs are fully static, no clock, refresh or timing strobe inputs are required. All operate from single +5 volt supplies and are fully TTL compatible. A three-state output and a chip select make memory expansion simple.

Typical operating power dissipation for the 200 nanosecond versions is less than 325 milliwatts. All offer identical performance, with the TMS4046 and TMS4047 series offering an additional feature of power down operation with very low power consumption of less than 10 milliwatts. The TMS4044 and TMS4045 are packaged in an 18-pin package; the TMS4046 and TMS4047, in a 20-pin package.

All the RAMs have fully decoded direct addressing and are available in plastic or ceramic DIP rated over a temperature range of 0°C to 70°C.

Prices in 100-piece quantities for parts in plastic DIP (with N suffix) range from $12.40 for devices with 450 nanosecond maximum access times, to $20.15 for those with 150 nanosecond access times. Prototype quantities are available now. Texas Instruments, Incorporated, Inquiry Fulfillment Service, P.O. Box 1443, M/S 669, Houston, TX 77001.

Hardware and services

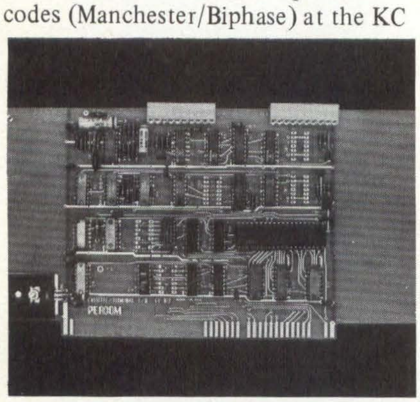


Floppy system for S-100 bus. FDS-2 floppy disk system utilizes the iCOM Frugal Floppy and iCom's executive system, text editor and assembler. It also incorporates an executive handler, which provides for all I/O vector assignments, I/O device handlers, USART and CPU initialization and program relocation requirements, transparent to the operating system. A source copy of the executive handler supports sophisticated users in building more complex operating environments. The 2-drive system comes in an 8.75" H x 17" W x 20" D cabinet and includes power supplies, RFI filter, fan and all necessary cables and connectors. Define end system and port assignments plus options when ordering; OEM and dealer discounts available. Synetic Designs Co., P.O. Box 2627, Pomona, CA 91766. (714) 629-1974 **Circle 158**

Universal development system. Designated the 8/16, this development system comes with Quickrun, an in-memory operating system for developing 8080 or 6800 programs. The system runs in 32K bytes and consists of a monitor/debugger, an editor and an assembler, all co-resident in memory with source- and object-code workspace. The Quickrun package lets you allocate 20K bytes of user memory as desired be-

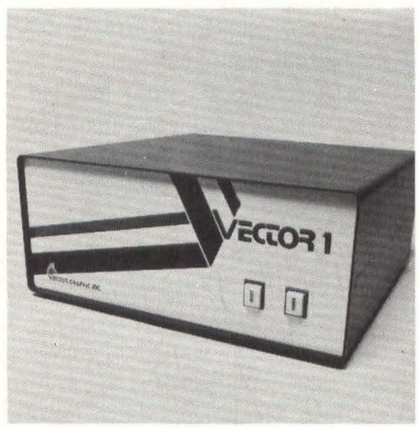
tween source code, object code and symbol table. The system's screen based editor and monitor/debugger are designed around a 20,000-char./sec CRT display; the entire screen can be rewritten in 50 ms. With a Microemulator in-circuit emulation option, you can single-step, slow-step or trace execution through critical program areas. Price for a system that serves either the 8080 or the 6800, plus 32K bytes of memory, dual cassette tapes and CRT console: $5275. Microkit, 2180 Colorado Ave., Santa Monica, CA 90404. (213) 828-8539
Circle 163

Cassette/RS 232 card for S-100 bus. Designated CI-812, this dual-function card combines interfacing functions normally requiring two or three PC cards. Its cassette interface phase encodes (Manchester/Biphase) at the KC



Standard rate of 30 bytes/second and at 60, 120 or 240 bytes/second for rapid loading of frequently used programs. The cassette interface record and playback circuits are completely independent, and the RS 232 terminal interface is full duplex and provides for data exchange at 300 to 9600 baud. Price: $89.95 in kit, $119.95 assembled. Add 5% for mail orders; 10% if COD. Per-Com Data Co., 4021 Windsor, Garland, TX 75042. (214) 276-1968 **Circle 157**

S-100 microcomputer. The vector 1 includes custom cabinet 18-slot motherboard, S-100 bus with 6 connectors, power supply (18A, 8V; 2A, ±16V), fan, card supports and guides for 6 cards, all hardware, wire and solder. Its 8080-based CPU board has 8-level vectored priority interrupts, current status register and dual-mode, real-time clock. A PROM/RAM board houses 1K RAM and has room for 2K of type 1702A ROM. You also get a 512-byte monitor for use with Tarbell cassette and Altair, Imsai or Polymorphic I/O boards. The unit requires an I/O board and terminal or a video board, keyboard and moni-



tor. Price: $619 kit, $849 assembled. Vector Graphic, 717 Lakefield Rd., Suite F, Westlake village, CA 91361. (805) 497-0733 **Circle 160**

Intel-compatible data acquisition systems. Model 735 series of data acquisition systems come on PC cards that plug into the card cages used by the Intel SBC-80/20 computers as well as the Intel MDS-80 microcomputer development system. The basic system in the series consists of 16 single-ended or eight differential analog input channels, either voltage or current inputs (4-20 mA or 5-50 mA), 12-bit A/D converter, sample and hold, and bus interface. Throughput rate measures 35 kHz. You can expand the card to 64 single-ended or 32 differential voltage or current inputs, up to two 12-bit D/A converters with 4-20 mA voltage or current outputs, and a software programmable gain amplifier. Basic system price: $495. ADAC Corp., 15 Cummings Park, Woburn, MA 01801. (617) 935-6668
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Yet the machine itself, remarkable as it is, represents only the beginning. The right Software, tailored to meet a user's specific requirements, is a vital part of any computer system. MITS wants to insure that Altair users everywhere have the best applications software available today and in the future. For this reason, a new MITS subsidiary, the ALTAIR SOFTWARE DISTRIBUTION COMPANY, has been formed. Its purpose: to acquire the highest quality software possible and distribute it nationally through Altair Computer Centers.

That's where you come in. The ASDC will pay substantial royalties to the originators of all software accepted into the ASDC library. If you have written business, industrial or commercial use software for the Altair 8800, ASDC wants to hear from you. It is the aim of the ASDC to stimulate and reward creativity in producing useful software that makes those dreams of "computers for everyone" come true. The ASDC will select only software that measures up to its high standards for system design, coding and documentation. The software will then be further documented and distributed through Altair Computer Centers around the country.

For more information on how to submit software to the ASDC, ask your Local Altair Computer Center for an ASDC Software Submittal Packet or contact the ALTAIR SOFTWARE DISTRIBUTION COMPANY.

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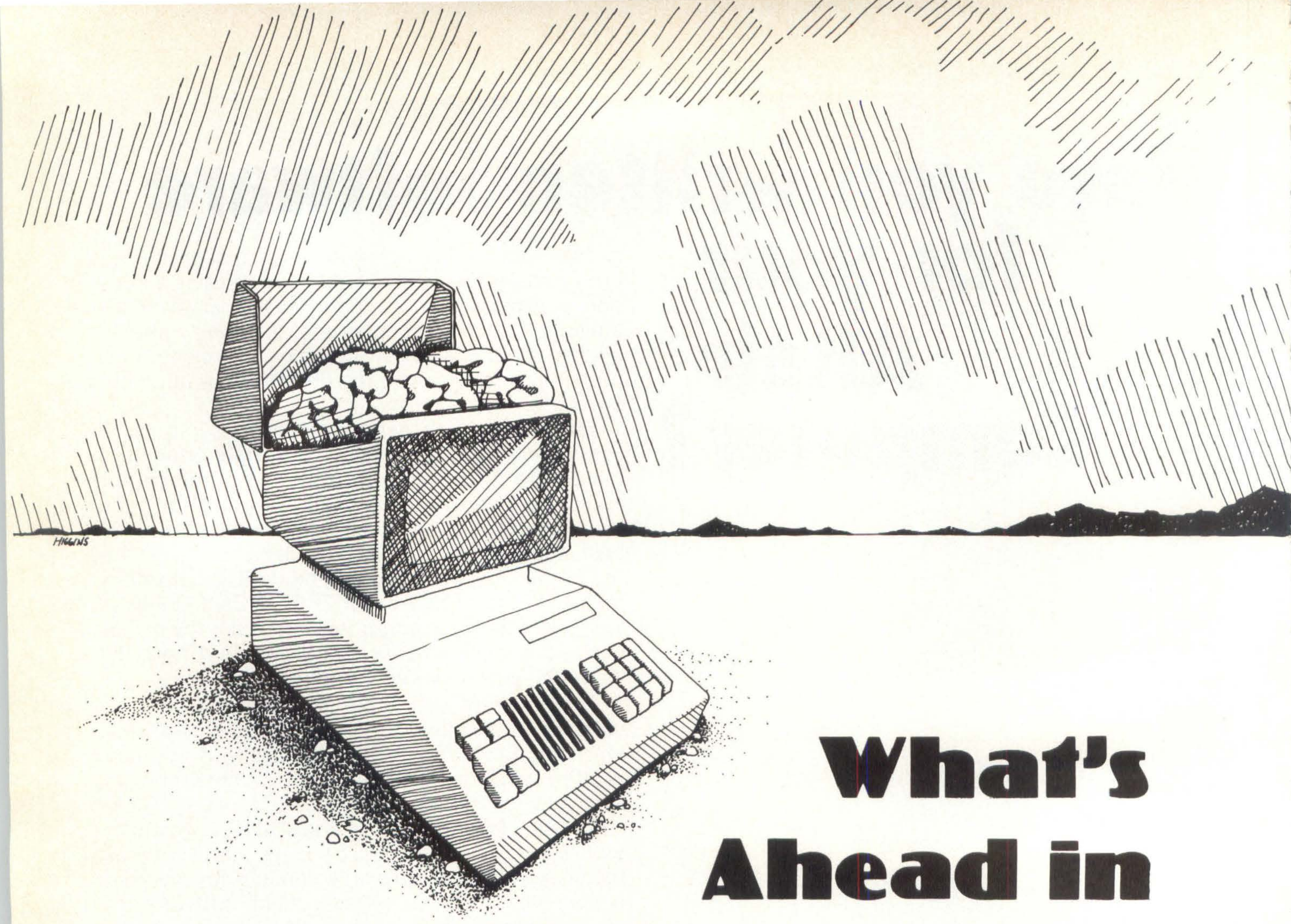


What's Ahead in CRT Terminals?

by **Leigh Cropper**

Now that combinations of the CRT terminal and the microprocessor have become commonplace, so have ads for "intelligent" terminals; such microprocessor based terminals appear to OEMs as ideal replacements for rack-mounted minicomputers in most turnkey systems. The μP terminal is a package with nearly as much memory and processing power as a minicomputer, and it costs little more than the terminals of a few years ago, which merely replaced Teletypes. As μPs and support chips proliferate, their further impact on terminals should be profound. What can OEMs expect? What pitfalls do they face? What new features will appear? What about prices? And what about new display technologies?

Before I can try to answer these questions, I must take a look at the current breed of μP terminals. Terminals are often described as "intelligent" or "programmable." "Intelligent" implies that a unit has processing power available to the user, while "programmable" means that the terminal contains a processor, but not necessarily that the user has access to that processor. Unfortunately, neither term tells the user enough. And "user programmable" can mean:

★ The terminal is programmable, but by the time the user buys all the hardware options (extra memory, printer, tape reader, floppy-disk drives) and software (editor, assembler, compiler, debugger) necessary for convenient programming, he has invested about $10,000.

★ The terminal is programmable as it stands or with one or two low-cost options, but only limited changes to an existing program are possible.

★ The terminal is programmable and contains a higher-level, self-modification routine that assists the user in tailoring the terminal to specific needs. But the modified program must reside in RAM and must be backed up by a storage device.

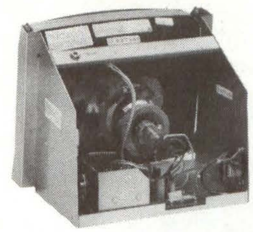
An OEM may find that any or none of these "user programmable" terminals meet these needs. For example, suppose the OEM must assemble a μC operating system that will drive two or three peripheral devices. To decide if a programmable terminal will do the job, he should ask:

- How much support software is provided by the vendor?
- How difficult and how expensive is interfacing the needed peripherals? (Consider both hardware and software interfacing.)

Leigh Cropper *is a design engineer at Beehive International, Salt Lake City, UT.*

If you make top-quality data terminals, here are four reasons to use Setchell Carlson CRT display modules in your system.

Reliability:



Our data displays are outstanding solid-state designs with critically matched magnetics to optimize the performance levels and dependability demanded by your customers. We use the most advanced engineering and production techniques to assure consistency of performance. No data display is built with more deliberate attention to quality and reliability.

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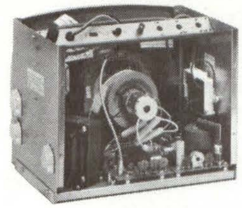
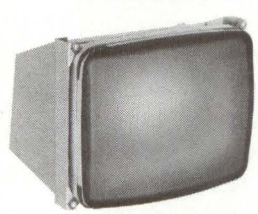


We've built thousands of displays for many of the major manufacturers in the country. Perhaps we already have a unit that would meet your requirements. With slight modifications. It would be less costly than starting from scratch. If you need a new, special package — we'll produce it for you, in the configuration you want, at minimal expense.

Cooperation:



If you're developing a new data terminal, we will be glad to cooperate with your terminal design engineers in reviewing your exact specifications and developing the most economical display possible. And quickly! Whatever you need, we have the experience and talent to design it. And improve it.

But don't take our word. See for yourself by contacting us today.

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CIRCLE 44

■ What percentage of the processor's time will be required to handle terminal functions? Will the remaining time be sufficient to get the job done?

■ How hard is adding the application program to the terminal firmware? Are there packaging or memory allocation problems?

Suppose, on the other hand, that the OEM needs a few hundred terminals. No hardwired terminal meets the system's specifications, and the OEM plans to adapt a programmable terminal by modifying its firmware. He should ask such questions as:

■ Is a copy of the source code for the standard terminal firmware available? On what medium? For how much?

■ What support programs and documentation are available to assist in modifying the firmware?

■ What hardware options are required to form a software development system?

■ Will the final program reside in PROMs, in mask ROMs or in mass storage (to be loaded into RAM)?

■ What form of firmware will the vendor ship in production models of the terminal – the standard form of the special?

As a general precaution, any OEM should assume that putting together a programmable terminal system will be as complex as putting together a minicomputer system.

How have programmable terminals evolved? Some experimentation occurred on CRT terminals in the early sixties, but those devices were expensive research projects that remained in the laboratory. The first serious market entry was the IBM 2260, introduced in 1965. The PDP-8 made its debut the same year, and the long marriage of the ASR-33 teletypewriter and the minicomputer began. About 1970, large mainframe manufacturers built terminals that they sold as part of total computer installations, and independent terminal manufacturers either second sourced IBM or began building teleprinter replacements. This first generation of terminals was characterized by relatively small display memories (usually 1000 characters), diode matrix character generators, limited functions like carriage return, line feed and home, and I/O speeds of 110, 150 or 300 bps.

From 1970 to 1972, the second generation of terminals appeared, with several features that have endured, among them a display size of 80 characters x 24 (or 25) lines, backed up by a 2K display memory and a ROM character generator. As designers explored new possibilities, terminals began sporting editing features, protected fields, tab stops, selective erase and block transmission. The RS 232 interface became dominant, and I/O speeds increased to about 2400 bps.

The Intel 8008 microprocessor was announced in late 1971, and during 1972 designers were hard at work blending hardware and software into workable terminal designs. The Super Bee, introduced by my firm in 1973, provided such features as back tab, cursor sensing and addressing, multiple display pages, message-oriented block send and I/O speeds to 9600 bps, all made possible by the microprocessor. Simultaneously, the low-cost terminals grew less expensive faster.

The current generation of terminals is characterized by more powerful μPs (like the Intel 8080), expandable RAM and larger ROM character generators with 128-256 characters. They feature programmable function keys, self test, easier user programming, expanded I/O capabilities and I/O speeds ranging to 19,200 bps. And even more features wait in the wings. Let's examine some of them.

displays and display formats

The CRT will remain the dominant display device in terminals for the next few years. Ever since the inception of the display terminal, designers have relied on the CRT technology developed by the tv industry. As a result, display formats hover around the 80 x 24 pattern dictated by the tv scan frequency of 15,750 Hz and the 60 Hz (non-interlaced) frame rate. Not that users wouldn't stand in line for a display that holds as many characters as an 8½" x 11" typed page, if its price were right. CRT monitors with improved characteristics to allow 90-character x 60-line display are in the works but they will cost from three to five times as much as monitors currently used in terminals. CRT technology has already achieved the necessary speed and resolution while meeting the needs of oscilloscopes and graphic display systems. But until some price breakthroughs develop, the 80-character x 24-line display will remain king.

Plasma panels remain in the wings, waiting for additional research to make them cost competitive; right now they cost at least an order of magnitude more than CRT monitors. Plasma panels' inherent memory was once viewed as an advantage, but LSI costs are eroding so fast that by 1980 (when the plasma panel is likely to start making inroads) a 4K x 8 memory will probably cost about $10 and CRT refresh circuitry about $5. So an alternate technology will have to approach the $100 level for a 2000-character display in order to spur a wholesale takeover. A large force like IBM or the tv industry could speed the advance when plasma panels approach the necessary cost range. But prediction is a dangerous game. An EIA report of May 1972 (discussed in *Electronic Design,* June 22, 1972) predicted the 1985 advent of the $25 hand-held electronic slide rule. The same report predicted that CRT terminals would match costs with teletypewriters between 1972 and 1975. Users are still waiting for a "dumb terminal" to outprice a KSR-33 teletypewriter but the hand-held electronic slide rule is available today at local discount stores for $19.95. The report acknowledged that political and economic factors are at least as important as technological ones.

While CRT display technology may not change overnight, the rapid decline in memory prices is spurring display memories to multipage sizes. The 4K RAM chip is replacing 1K RAMs and shift registers as the standard display memory element; this change makes a 4000-character capacity a natural feature. When 16K RAMs become price competitive late this year or in 1978, a 16,000-character memory will cost little more than a 2000-character memory in 1974.

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A note of caution is in order, however. The 2000-character display memory has set certain standards of versatility that may be hard to achieve with larger memories. Scrolling, editing and protected format features are expected to work at high transmission and reception speeds (9600 and 19,200 bps). With multipage memories, scrolling can be achieved with clever hardware and software techniques, but full memory editing and formatting will cause significant speed reductions. Designers will probably compromise by editing by the line and the paragraph, and formatted areas may be restricted to 2000- or 4000-character blocks. Savings in memory and central control circuitry achieved by μPs may be offset by the cost of special support circuits to assist high-speed search and erase capabilities.

As I've stated the 80 x 24 display format will remain as a standard; smaller arrays find use only where price and/or size are governing factors. If there is any de facto standard emerging in small displays, it is the 32 x 16 format found in the IBM 5100 and the Informer terminal.

A standard format for the word processing terminal remains to appear; 80 x 50 may form a reasonable compromise between typed-page requirements and technological and cost constraints. An office that uses elite-face typewriters might like a display as large as 102 x 66 to facilitate alignment with the full dimensions of a typed page, but it could probably manage nearly as well with a 90 x 60 format. Matching the pica-face format of 85 x 66 is easier; the current line length of 80 characters would be sufficient. Vertically, 60 lines would be preferable, but 50 may be considered adequate, especially because some typewriters now format with 55 lines/page.

All of these formats assume a 5 x 7 or 7 x 9 character dot matrix, adequate for most applications. But some alphabets like the Arabic and Russian require greater resolution for adequate readability. Until now, a large dot matrix like 10 x 16 required a unique design in the display timing logic, character generator and video dot shifter. But at least one of the recently announced CRT controller ICs has programmable flexibility in the dot matrix size, as well as in line length and number of lines, which will make it much easier to adapt a standard display logic circuit to a larger character size with fewer characters on the screen. The character generator will have to be changed as well, but that change will be straightforward for the ROM vendors as soon as sufficient demand appears.

One of the classic design techniques used to synchronize a terminal display requires a crystal oscillator to generate the basic dot frequency; that dot frequency is repeatedly divided to obtain the character, scan (or horizontal sync), line and page (or vertical sync) frequencies. The crystal frequency is chosen so that the vertical sync frequency matches the line frequency; failure to achieve an exact match results in a "swimming" display: the beat frequency between the magnetic field generated by the power supply transformer and the vertical deflection frequency causes the characters on the screen to shift annoyingly. Expensive magnetic shielding and changes in the frequency dividing logic can eliminate the "swim," but a more desirable approach involves synchronizing the beginning of each vertical scan with the line frequency. So far this approach has proved difficult and expensive. Inexpensive and highly stable phase-locked loops promise to provide the means of synchronizing automatically with any changes in line frequency, a particularly important consideration outside of the U.S.

character generators and keyboards

My firm's B500 terminal uses a UV-erasable PROM as a character generator, a feature that lets a low-quantity user customize character fonts without having to absorb a $1000 ROM-masking charge and agreeing to buy at least a few hundred character generators. The 1K x 8 PROM size allows a 128-character set with an 8 x 8 matrix for each character; as larger and faster PROMs appear they can be used to generate 7 x 9, 8 x 12 or larger character fonts.

And as electrically alterable ROMs (EAROMs) become larger and less expensive, they will become an ideal element for implementing dynamically programmable character sets. With such a character generator in a library terminal, the main computer could change the alphabet displayed by the terminal each time a user changes languages. But it will probably be about two or three years before such PROMs grow large enough and cheap enough to be practical. In the meantime, large ROMs can be used to achieve character sets of 256 and up.

A look at today's high-level terminals reveals greatly expanded typewriter keyboards. Extra keys are everywhere; in addition to the basic ANSI or typewriter layout, you'll find numeric pads, function keys arranged in rows and clusters, lighted keys, switches and special controls. In an effort to adapt to many varied users, terminal manufacturers have kept adding special keys. By making difficult functions possible, manufacturers can't avoid adding complexity to the simple functions.

Ideally, OEMs would buy the simplest terminal that satisfies their requirements, but usually they must accept a few functions that they don't need or want in order to get two or three functions they require. Vendors, on the other hand, find it necessary to cluster functions to avoid the pitfalls of too many different versions of their products. Programmable keyboards provide a compromise solution to this problem; they allow the user to specify keycaps and codes for each key position. The vendor buys a standard keyboard module, which connects to a standard terminal, then programs custom PROMs with the user's coding requirements and exchanges the special keycaps as needed. The service isn't free, but it has two important advantages: It is usually less expensive than a custom terminal design, and it helps keep the keyboard as simple as possible.

OEMs must also serve growing foreign markets. Wages and manufacturing cost are so high in Europe that it is often

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cheaper to import electronic systems there from the U.S. But European customers expect vendors to adapt equipment to exacting national requirements, which require anything from minor to major changes in keyboards. OEMs can adapt much more easily if they use a terminal with a programmable keyboard, especially for countries with low sales volume. Looking ahead, you can see an obvious application in the market segment for the EAROM as the programmable element in terminal keyboards.

In the next few years keyboard costs should gradually drop, because:

★ Calculators have bred a large number of inexpensive and reliable keyboard designs, and terminal keyboards should inherit some of their benefits.

★ The home computer market will demand a keyboard similar to one used on a terminal, but at very low cost. That market's potential volume will provide plenty of incentive to keyboard designers.

★ Keyboard electronics are evolving toward one lower-cost LSI chip.

programmability with EAROMs

As I've pointed out, "programmable" is a fine word if you want to avoid being specific. In this discussion I'll use a narrow formulation – "keyboard programmable" – which means that the performance characteristics of a terminal can be changed by typing at the keyboard. I'll exclude such operations as setting switches, installing or removing straps and changing parts.

Here's why. In terms of programmability the OEM and the user would like to be able to easily modify any terminal function by entering a simple sequence at the keyboard, and they would like all such changes to persist indefinitely once they are selected. Existing terminals meet neither need sufficiently. A limited number of terminal functions can be modified by setting switches (usually at the rear of the terminal, where they are hard to reach and impossible to see, or inside the terminal, which is even worse), by installing straps (inside the terminal, often requiring a soldering iron) or by reprogramming PROMs (which require a PROM programmer and other backup hardware and software). Such modifications persist once you make them, but they are just as hard to change the second time.

A μP terminal allows some keyboard programmable feature, but all the changes are lost each time the unit is turned off. A partial solution is to place the function-change information in mass storage and load it in every time the terminal is powered on. Enter again the EAROM as an exciting solution to a problem. The next generation of terminals will attain significant versatility with even a small EAROM (~4 x 64). For example, the transmission rate, parity check and word length (10 or 11 bits) could all be set at the keyboard by calling up a short conversational routine. On a polling terminal, the feature could be expanding to allow selection of the polling address and certain features of the polling protocol. As larger EAROMs become available, a dispatching table could be stored and then changed at will. Thus a user who wanted to change the code for "cursor up" from "ESCAPE, A" to "CONTROL, A" could do so by simply changing one or two entries in a table. Other applications will flourish as designers work further with EAROMs.

But EAROMs also have several disadvantages that will slow their entry into the terminal area:

★ They have slow read speeds (2-10 μs typical).

★ They have very slow write and erase speeds (100 ms to 1 sec typical).

★ They have no second sources.

★ They have awkward word sizes (no 8-bit units).

★ They require unusual voltages.

★ They are expensive (about 10 times the cost per bit of UV PROMs).

But users can live with these problems, and vendors are working on improvements.

terminal-system software

OEMs who bought the first programmable terminals found themselves in a position similar to the first μP users; they had very little support software and very little documentation. But as with μPs, terminal software continues to improve. And much μP software can be adapted for use on a μP-based terminal by an enterprising OEM. But the buyer who desires the same kind of software support on a terminal available in a μP development system will have to search long and hard. Some terminal manufacturers advertise monitors, compilers, editors and debug programs, and most programmable terminals have a monitor program of sorts, resident in ROM or PROM with the basic terminal program. If the terminal manufacturer offers such programs, an OEM should ask some hard questions to find out whether he can use them:

★ What medium – paper tape, PROM/ROM, floppy disk – stores the program?

★ How does a user load the program into the terminal – through a paper-tape reader, a disk drive or PROM sockets? Does the resident monitor program support transfers from such devices? If the program lies in ROM/PROM, are there enough extra sockets in the terminal, or must part of the basic terminal program be pulled to accommodate another program?

★ How much memory must support program execution? An assembler will probably require between 4K and 12K of memory for the program itself and another 4K or more of working storage. Editors and compilers also have substantial working storage requirements.

★ What does the terminal use as an auxiliary storage medium while editing and assembling?

If the answers to these questions are less than pleasing, an OEM may find it advantageous to purchase or lease a μP development system for the type of μP used in the terminal. For example, assume that an OEM wants to use a program-

mable terminal as part of a small data collection station, consisting of the terminal, a frequency counter with an RS 232 interface (or parallel interface if the terminal has one) and a printer. The system monitors oscillators on an assembly line, and the counter makes measurements and sends the data to the terminal. A custom program in the terminal must respond to the interrupt from the counter, read in the data, make simple calculations and format the data in an easily read display. Periodically or on demand, the terminal must send a page of data to the printer as a permanent record. An output might be added so the terminal could also drive selection machinery to sort the oscillators by frequency. The custom program is a significant modification to the existing terminal program, but once the new program is written it is put into ROMs or PROMs and used in all such systems.

Therefore, this OEM needs a development system while he writes and debugs the program. The hardware cost of such a system is less than the other costs of developing the program (programmer salaries, software training courses and documentation), so the OEM is well advised to lease or rent a μP development system, which should include a printer, dual floppy-disk drive, emulator and PROM programmer. He should acquire from the terminal vendor a source copy of the terminal program on a floppy disk. The OEM should use the development system to edit and add to the terminal program and, when the program is assembled and ready to debug, connect the emulator system to the programmable terminal in place of the terminal μP. Then he should load the program into the terminal RAM and use the emulator system to debug the program. When the program is debugged, it's programmed into PROMs. For such an application, which requires a fixed, custom program for a turnkey system, the vital characteristics of the user programmable terminal are the μP and the RAM used while debugging the program. Once the program is developed, the OEM can probably do without the RAM except for a small scratchpad.

Other OEMs will cater to end users who want programmable features in their terminals but who have neither the money nor the software expertise to perform assembly language programming. They want programmability analogous to that of a programmable calculator. Think of a terminal as having an instruction set that consists of "carriage return," "line feed," "clear screen," "write an A," "insert a B," etc.; that is, all the functions (display and control) that the terminal normally performs. Add a small set of new program-oriented terminal functions such as conditional branches, compare and I/O read commands. A programmable function key feature allows the user to key in a program and assign it to a function key and also display the program and edit it using the normal terminal functions.

Such capabilities, which allow a non-programmer to write programs on the terminal, are sure to appear within a year. The ability to store such keystroke sequences as a file on the mass storage of the host CPU is already built into the B500. Some terminals incorporate cartridge or cassette drives, and you can look for more programmable terminals to include integral mass storage units, especially now that floppy-disk cassette-drive controllers are being integrated into single LSI chips. As 16K RAMs grow cheaper it will become practical to expand a terminal's program memory to the full addressing limit of the μP (in most cases, 64K).

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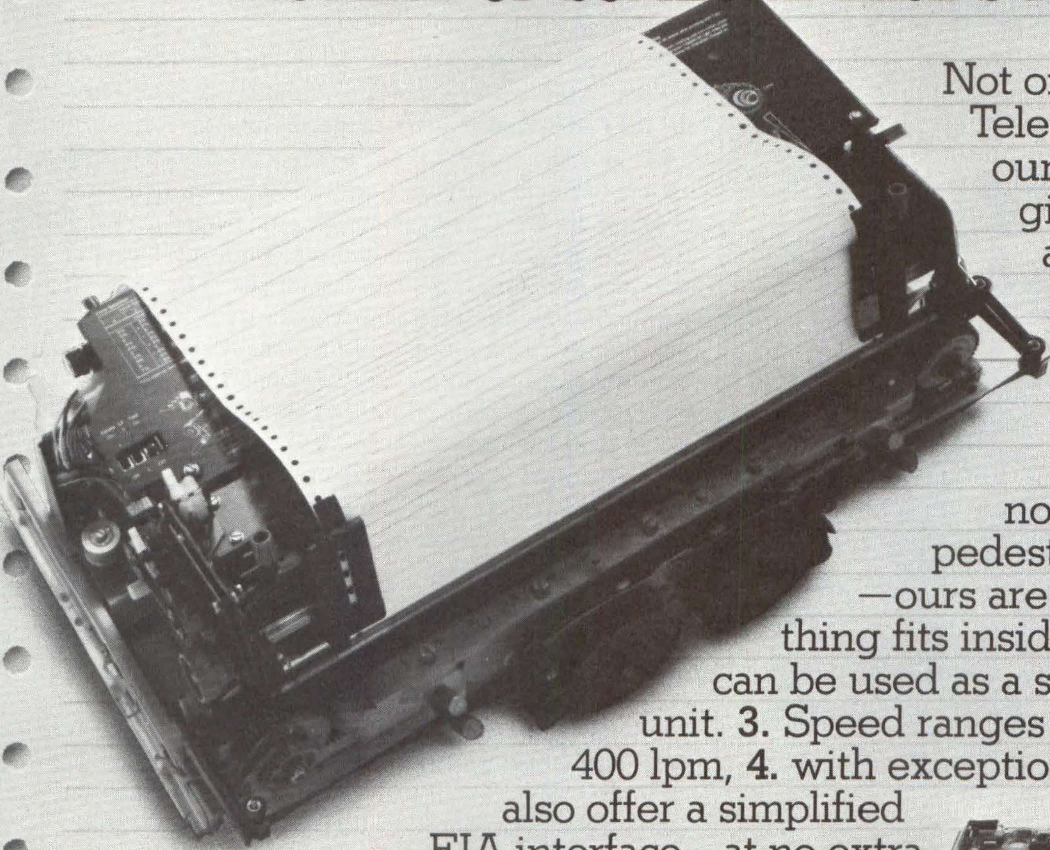

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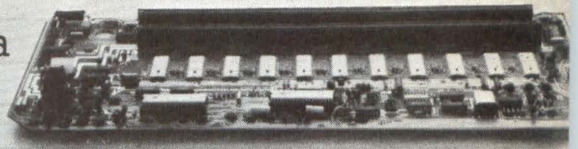

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trends in I/O

RS 232C asynchronous I/O is and will remain the standard interface for CRT terminals. Any drawbacks are offset by the enormous number of devices that use this standard. Current loop interfaces (20 and 60 mA primarily) will remain popular for maintaining Teletype compatibility and for cable transmission in high noise environments and over 50-2000 ft ranges.

Parallel interfaces have been unusual in the past, probably because of the lack of a standard. With the establishment of the IEEE 488 parallel interface specification for instruments, it will only be a matter of time before terminal manufacturers join the ranks of its users; with its μP power, keyboard and large display, the programmable terminal is a natural controller for programmable instruments. Another standard of sorts may arise for parallel interfaces if one of the μP programmable interface chips achieves industry dominance.

Currently most programmable terminals have two or three I/O ports, to which a user can connect the host CPU, a mass storage device, a printer and other devices. As terminals grow more powerful, the number of I/O ports is sure to grow. Future terminals will connect to badge readers, light pens, product code wands and instruments as they encroach on the territory of dedicated minicomputers.

Polled terminals, most of which have synchronous interfaces, have suffered from the lack of standards; several mainframe manufacturers have produced such units, each with a different protocol. The word- or byte-oriented protocols, such as IBM's Bi-Sync, have been used almost exclusively, but more recently bit-oriented protocols such as IBM's SDLC have begun to achieve strong inroads.

Until recently, terminal designers have had to decide on one or two similar protocols and concentrate their efforts in those areas, but the semiconductor houses are beginning to change that approach. During the past few months, several special interface chips have appeared; some operate in either synchronous or asynchronous mode, and others, though synchronous only, easily adapt to byte-or bit-oriented protocols. Suddenly designers have the resources to adapt easily to a variety of interface requirements with the same basic terminal, an ability that means more competition for mainframe manufacturers and more options for OEMs.

some final thoughts

It will be only a matter of time until an OEM can buy a ruggedized terminal. The major problem is obviously the CRT. Tough, hermetically sealed key switches already exist. The rest includes ICs, passive components, logic boards, connectors and cables, all available in rugged versions. As terminals serve more tasks in heavy industry, the demand will increase for units that can tolerate extremes.

The microprocessor based terminal will soon reach a fork in the road. One route leads to a highly adaptable terminal that will perform more and more functions but will remain a peripheral device to a host computer. The other route leads to a standalone, interactive computer that contains a CPU, display, keyboard, memory, printer, mass storage and interface ports. If past trends continue, prices for terminals will drop slowly, but features will be added to give the OEM more value at a given price. ♦

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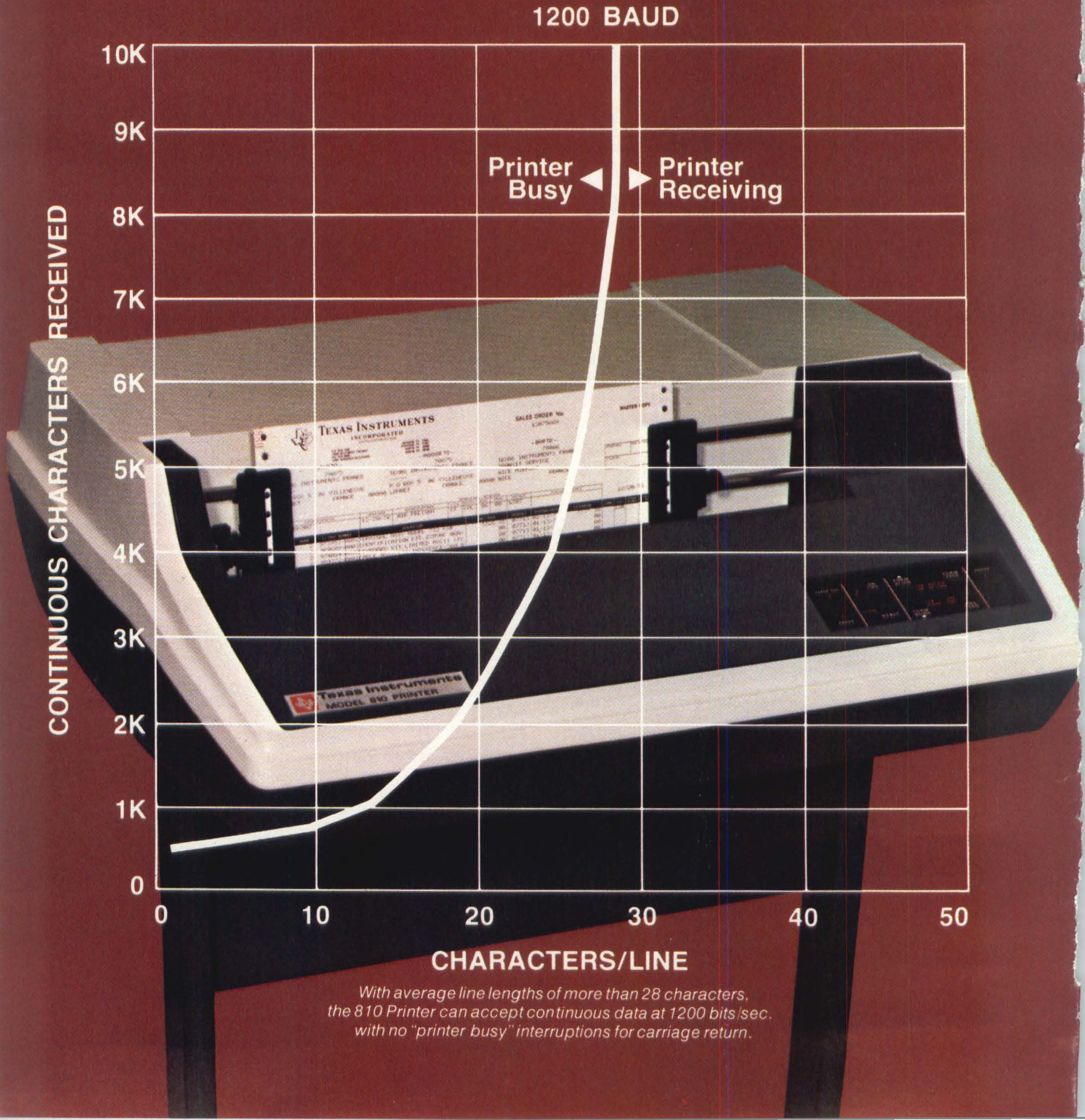

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IMPROVING CRT-MODULE PERFORMANCE IN TODAY'S CRT TERMINALS

How the systems-design considerations that govern the readability, stability and reliability of CRT modules affect the incorporation of those modules in CRT terminals

by **John Logeman**
and **John McCabe**

As computer users expand existing data bases or install smaller systems that utilize such relatively new components as microprocessors, the video data terminal has become one of the fastest growing types of computer peripheral. CRT requirements have also changed since the introduction of yesterday's relatively simple data-entry systems; the large "middle-of-the-road" market continues to grow, but a pronounced emphasis on more sophisticated terminals that can display more information on the screen has also appeared.

But increasing the amount of information on a screen isn't just a matter of using a larger screen; it requires a major revision of existing technology. A full-page display for word processing applications that presents 5000 or more characters places unusual demands on a technology that originally evolved from commercial television receiver design. Of course, the display device used in such a terminal need not be a CRT; other display techniques are becoming increasingly available. But in any display of more than a few words or characters, the low cost per character of CRT technology will continue to dominate the market until a major breakthrough occurs in an alternative character-display technology.

A video data terminal is a combination of logic, CRT and cabinetry design. Because the CRT module is usually the most expensive single hardware item in such a terminal and affects all other terminal-design aspects, users of CRT terminals should evaluate the many facets of the module's design. The primary factors are readability of the characters, stability of the display, reliability and system tradeoffs.

We define a CRT display module (Fig 1) as a cathode ray tube and the associated electronic circuits required to drive it. These circuits typically include horizontal and vertical deflection systems, a high-voltage supply and a video drive system. A CRT module doesn't include any logic or character generation electronics.

Many variations on the electronic content of a CRT display module exist, depending on the desired display format and on the approach used in interfacing the module with the character generation system. Because of the interdependence of logic and display electronics, as well as mechanical and formatting parameters, terminal design requires a coordinated effort between the systems designer and the display module manufacturer from the beginning of the design. We limit our comments to raster-scan-type displays, although many of the points we make apply to other display tubes.

increasing character density

Designers can use several methods to increase the quality and amount of data displayed on the screen of a terminal. The major limiting factor to the number of characters displayed is the horizontal sweep (or scan) rate of the display module. The original standard horizontal rate of 15.7 kHz is adequate for the majority of applications using an 80-character, 24-line, 5 x 7 dot matrix format, but higher-density displays, including those that present both upper- and lower-case characters, require an increased number of active horizontal scan lines. To achieve this goal, a designer can increase the horizontal sweep rate, and horizontal rates of 18.5 kHz and higher are becoming common. While this method is acceptable within limits, scan rates over 18.5 kHz require a significantly more sophisticated (and more costly) video amplifier and horizontal deflection technique, because a module's high voltage is normally derived from the horizontal deflection system.

Removing the scan lines between rows of characters can also increase the effective scan rate. This technique, termed StepScan, speeds up the vertical scan during one horizontal line and can provide four or more lines of vertical intercharacter spaces while actually utilizing only one line, with no increase in character or dot rates. Implementing this method requires modified vertical sweep circuitry and an additional input to the display module to identify the lines to be "skipped." When the normal vertical intercharacter spacing is completely removed, the cursor must be provided by increasing the brightness of the character or by using reverse video for that character. Using a higher-amplitude signal or changing the video gain to accomplish this effect re-

John Logeman *and* **John McCabe** *are, respectively, chief engineer and marketing manager of Motorola Data Products, Carol Stream, IL. McCabe is based at the firm's Holbrook, NY, office.*

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CIRCLE 52

quires special circuit design, and the process is both complex and expensive for a display module manufacturer. An excellent method of highlighting selected characters results from using 50% or 75% duty cycle dot pulse for normal brightness and a 100% duty cycle for highlighting.

A third method that can increase the number of available active scan lines at a given scan rate is termed interlacing; in an interlaced scanning system, only half of the image is refreshed during each vertical sweep cycle. In an alternate field, the horizontal scan lines are interleaved with the previous field (Fig 2). In a data display, alternate fields contain different data and must be balanced to keep the high-voltage supply current balanced. The slightest imbalance in beam current can cause high-voltage variations, which in turn cause size differences between successive fields and produce character distortion.

The major disadvantage to interlaced scanning is that the interlace refresh rate produces a flicker that can be seen by the human eye if normal (short- to medium-persistence) phosphors are used. The only satisfactory solution to the flicker problem in an interlaced system is to use a long-persistence phosphor like P39.

Increasing the number of characters on the screen beyond the limit of normal horizontal sweep rates requires an interlaced format if the display must have a refresh rate synchronous with the power line frequency. If the refresh rate – in both interlaced and noninterlaced displays – is not synchronized with the power line frequency, the CRT's electron beam can be deflected by stray magnetic fields, especially those produced by nearby power transformers. This phenomenon, termed "swim," is very difficult and usually expensive to correct if a designer doesn't deal with it during the initial logic system design. But don't construe "synchronized" to mean that the refresh rate must be line-locked to the power line; the refresh frequency need only lie less than 1 Hz away from the power line frequency. These considerations are particularly important if the terminal will be exported to countries that use 50 Hz power.

phosphor characteristics

The use of P4 (white) phosphor in data displays arose naturally from its use as a standard monochrome television phosphor, but a trend in the direction of green phosphor has appeared since IBM began using a green phosphor in the 3270 Series terminals. Green corresponds to the peak of the human eye's spectral response, and many of the phosphors that minimize flicker resulting from interlaced scan and 50 Hz refresh are green. A terminal designer can control the choice of phosphor as a part of the CRT display module specifications. The characteristics of common phosphors appear in the table; phosphors other than the ones shown have poor delivery times and higher costs.

While long-persistence phosphors minimize flicker problems, they also have some disadvantages that a systems designer must consider. First, they "burn" much more easily than short- to medium-persistence phosphors; after a time, the often-repeated portions of the character format grow visible as a dark pattern on the face of the turned-off tube. This susceptibility to burn is roughly proportional to persistence. Second, the minimum achievable spot size of a very long-persistence phosphor like P39 is greater than that possible with a short- or medium-persistence phosphor. This condition arises from the method by which longer persistence is achieved: Of the two types of phosphors that constitute a long-persistence phosphor, one is the normal type, which is excited by the electron beam and emits light; the second is in turn excited by the light emitted from the first. This two-step process causes a scattering effect, which increases the spot size and results in some loss of resolution in a dense data display.

display readability

CRT display module manufacturers specify the "readability" of their products in terms of "resolution," typically defined as the fineness of detail achievable on the CRT screen. The traditional denotation of resolution is in standard tv lines –

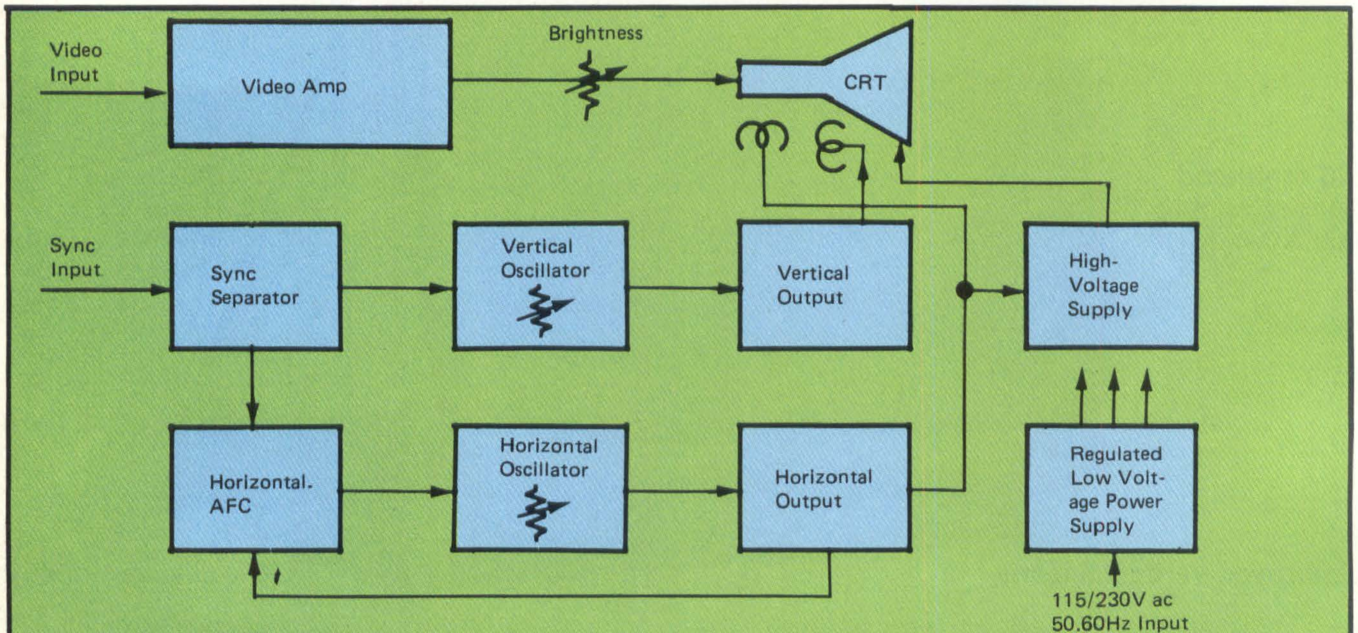


Fig 1 Typical CRT display module incorporates a cathode ray tube and associated drive electronics, including horizontal and vertical deflection systems, a high-voltage power supply and a video drive system. It doesn't incorporate logic or character generation electronics.

An Editing Pet That's

The perfect editing terminal for transaction processing must be more than a little bit smart. It has to be wise like our OWL-1200. With features that assure high accuracy source data entry, fast data editing, simplified host computer programming, and reduced host computer loading.

Our OWL gives you all the human engineering features you get with our FOX-1100, plus a lot more. And the price is right. Just $1496 in quantities of 25.

Check the comparison chart of editing terminals to see all the reasons why the OWL-1200 is simply "incomparable."

		PERKIN-ELMER	HAZEL-TINE	LEAR SIEGLER		ADDS
USER REQUIREMENT	FEATURES	OWL-1200	MOD. 1 EDITING	ADM-1A	ADM-2	980
High Operator Data Entry Accuracy	Protected fields	Yes	Yes	Yes	Yes	Yes
	Low-intensity fields	Yes	Yes	Partial	Partial	Partial
	Numeric only fields	Yes	Yes	No	No	No
	Inverse video fields	Yes	Yes	No	No	No
	Blink fields	Yes	Yes	No	Yes	Yes
	Line drawing capability	Yes	No	No	No	Yes
Simple, Fast Editing of Data	Insert/delete character	Yes	Yes	Partial[1]	Yes	Yes
	Insert/delete line	Yes	Yes	Partial[1]	Yes	Yes
Minimized Loading on Host Computer	Host programmable send keys: send all data, send only unprotected data, send only data modified by operator, send only a "request to send" header.	Yes	No	No	No	No
Simplified Programming	Ability of host CPU to read device status	Yes	No	No	No	No
	Ability of host CPU to read device mode key settings and communication option straps	Yes	No	No	No	No
	Program override on mode key settings	Yes	No	No	Yes	No
Simplified Program Debugging	Transparent mode permits all characters to be displayed	Yes	No	No	No	No
Cost Effectiveness	OEM price in quantities of 25*	$1496	$1670	~~$1795~~ * $1595	~~$2395~~ * $2095	$1995

*When unit includes editing capabilities, 24 x 80 display, numeric pad, and upper/lower case characters.

[1] No Key. Requires Two Key Code.

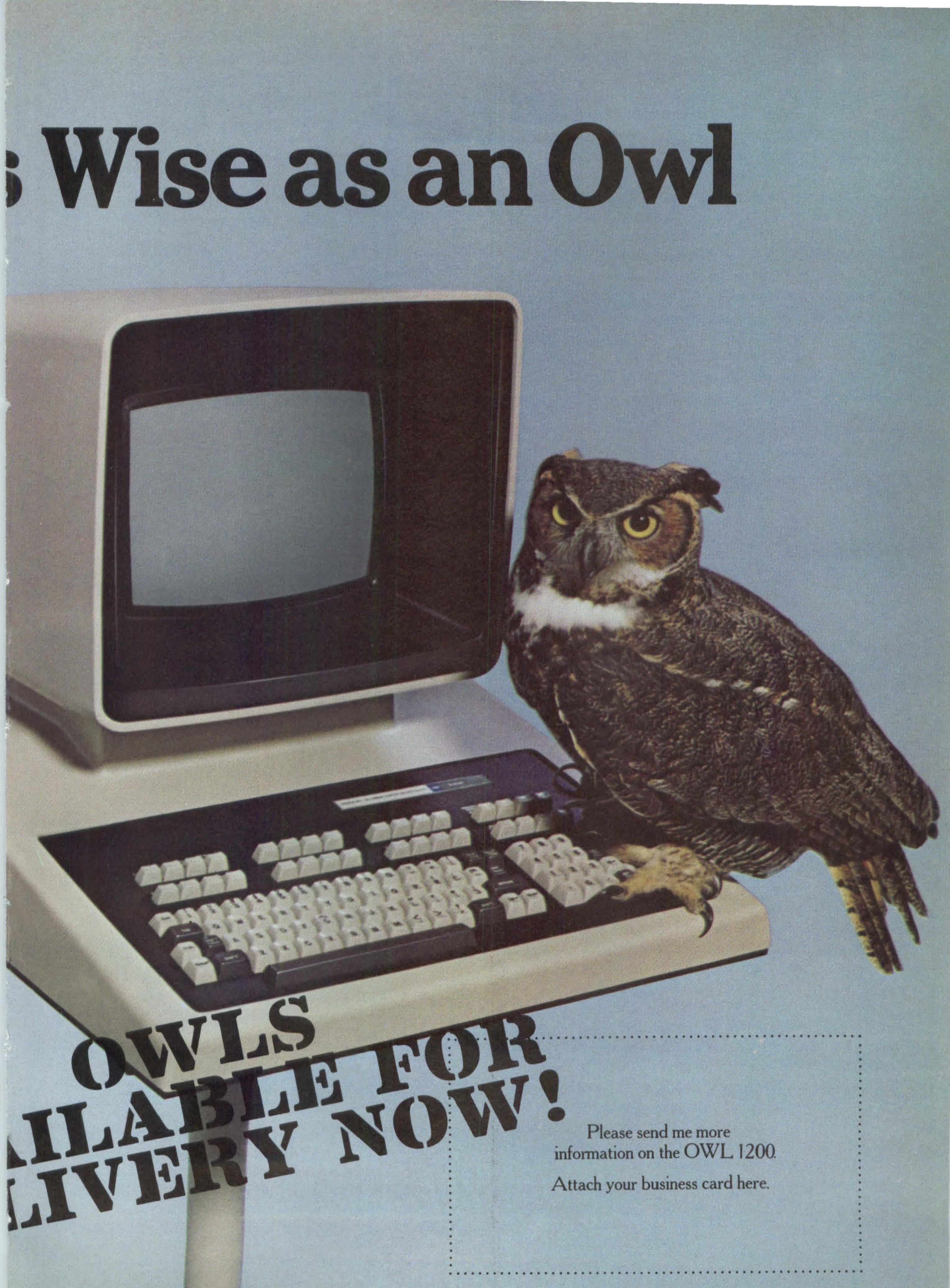
* Just announced price changes

PERKIN-ELMER DATA SYSTEMS | TERMINALS DIVISION

Randolph Park West, Route 10 & Emery Avenue
Randolph, N.J. 07801 (201) 366-5550 TWX: 710-987-7913

Overseas, call: 44895-52441 Uxbridge, UK
887-1000 Sydney, Australia
416-677-8990 Mississauga, Ontario, Canada
031/450/160 Frolunda, Sweden
2200949 Singapore

AVA
DE



s Wise as an Owl
OWLS
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Please send me more
information on the OWL 1200.
Attach your business card here.

CIRCLE 54

the number of individual picture elements (alternate black and white lines) that can be distinguished in a horizontal scanning line within a distance equal to the picture height.

While this traditional method of measuring resolution is still used, it is invalid for a dot matrix type of presentation. While the ability to distinguish individual dots in a character has long provided an indicator of performance, designers are realizing that merging the dots within a character produces a more pleasing presentation. Engineers evaluating a design mustn't lose sight of the standards that the user will ultimately apply; that user merely requires a clear, legible presentation; he is not interested in individual dots.

Higher resolution requires, among other things, smaller spot size. The spot size of a CRT depends upon the phosphor type, beam current, deflection circuitry and spot location on the tube face. If the spot is minimized in the center of the screen it may grow larger as the beam moves away from the center. Careful yoke design can minimize

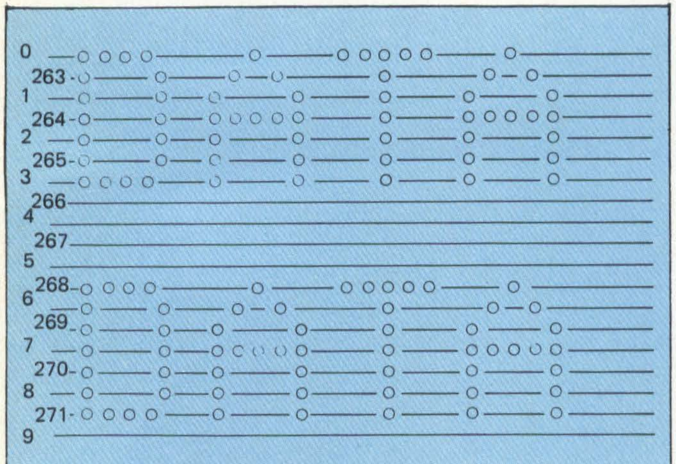

Fig 2 Interlaced scanning refreshes half of an image during each vertical sweep cycle. The alternate fields must be balanced to prevent size variations between successive fields and the resulting character distortion.

this location defocusing, or astigmatism, and electron-lens design can minimize the spot size. The only practical way to obtain uniform focus is to apply a correction voltage (dependent on deflection angle) to the focus grid. This procedure, termed "dynamic focus," is available in most high-quality CRT display modules.

As the number of displayed characters increases, the size of each character and the spot size grow smaller and demand a higher-quality display module. When the distance between scan lines decreases, the spot size must decrease, and the size of the dots that constitute the characters becomes smaller. This adjustment in turn requires greater performance capability in the video amplifier. Video amplifier designs for high-density data terminals require bandwidths approaching 50 MHz, which requires the use of a linear amplifier, because any nonsymmetrical switching amplifier propagation delay would make the display useless.

A point often overlooked by logic designers when evaluating video amplifiers response is that a video amplifier must accept square waves. This requirement makes the pulse duration as related to rise and fall time important – the specified rise and fall time of the video amplifier is a major consideration, particularly if a less than 100% duty cycle

Characteristics Of Common CRT Phosphors

Type	Color	Peak (Range) (mm)	Persistence	Decay to 10% Brightness	Advantage	Disadvantage
P4	White	450 & 540 (390 to 700)	Medium Short	60µs	Standard alphanumeric display phosphor; lowest cost; most readily available; good focus and small dot size capability moderate resistance to burn	Not suitable for interlaced operation (flicker objectionable)
P21	Green	520 (420 to 600)	Medium Short	38µs	Easier on eyes for long term viewing; highest luminescence; highest resistence to burn; good focus and small dot size capability	Flicker objectionable in interlaced operation; slight cost premium
P39	Yellowish	525 (490 to 580)	Long	150 µs	Eliminates interlaced mode flicker; usable to 25 Hz without flicker	Moving cursor appears to smear or trail; focus and dot size poorest of all phosphors; burns easily; lowest light output; slight cost premium
P42	Yellowish	520 (450 to 590)	Medium	8µs	Easier on eyes for long-term viewing; brightness comparable to P4; spot size and focus better than P39; usable to 50Hz refresh without flicker; no cursor smear as in P39	Not as readily available as other phosphors; slight cost premium; flicker objectionable in interlaced operation

provides intensity differences in parts of the displayed text.

An antireflective – more accurately a "nonglare" – faceplate usually serves a CRT in areas of high ambient lighting or in other conditions where reflections from the CRT face may pose a problem. Several glare-control methods exist: an etched glass faceplate permanently bonded to the CRT

MEMO:

TO: All potential Microprocessor Users

Consider the NEW Memodyne 760 Series of high-performance digital cassette recorders with your micro processor (or your mini-computer or terminal)

Model 764 (Shown)

HIGH PERFORMANCE DIGITAL CASSETTE RECORDERS

FEATURES

HIGH SPEED Up to 32 kilobits per second. Searches forward and reverse at 100 inches per second.

FAST RESPONSE 200 millisecond start-stop-settle time.

RUGGED AND RELIABLE Only 2 moving parts. • MTBF > 10,000 hours. Soft error rate of 1 in 10^7.

LARGE CAPACITY Up to 1600 flux changes per inch or 5 million bits per standard Philips cassette.

VERSATILITY Accurate speed, very low skew and ANSI/ ECMA compatibility permits use of all popular encoding schemes.

STATUS INDICATIONS BOT/EOT hole and leader sensor, Cassette-In-Place, File Protect and Busy/Ready.

DESCRIPTION

The Memodyne 760 Series of cassette recorders are compact, removable medium, storage devices for digital information. Their two track and high density capability provide up to 5 million bits of storage on a single standard Philips cassette. In their standard configuration they are capable of storing or retrieving data at a rate of 16 kilobits per second per track. A patented reel-to-reel constant tape speed servo (U.S. Patent Office #3,733,529) coupled with precision tape guidance allows implementation of any of the popular encoding schemes with low error rates, minimal tape wear, and high tape utilization. The simplicity of the transport mechanism and the use of conservatively rated, high quality parts give high reliability and maintenance-free operation. Three of these compact units can be fit on a single 5" x 19" standard panel. The enclosed cassette chamber holds the cassette firmly, resisting vibration while shielding the cassette from airborne contaminants.

SPECIFICATIONS

Status Signals:
Cassette-In-Place, File Protect, B/EOT, Busy/ Ready — TTL Compatible.

Control Signals:
Run/Stop, Forward/Reverse, Slow/Fast — TTL Compatible.

READ AND WRITE PERFORMANCE (Read-While-Write)

Gap Spacing:
.150, ± .005 inch.

Dynamic Skew:
± 100 microinches max.

Recording Density:
To 1600 flux reversals per inch nominal.

Transition Spacing:
Down to 625 microinches nominal.

Read and Write Rate:
Up to 32,000 transitions per second.

TAPE MOTION

Tape Speed:
20 inches per second,
100 inches per second,

Start Time to ± 5% of 20 Inches Per Second:
75 milliseconds.

Start Distance to ± 5% of 20 Inches Per Second:
1.00 to 1.25 inch.

Start Distance to ± 5% of 100 Inches Per Second:
500 milliseconds maximum.

Stop and Settle Time:
150 millisecond recommended minimum.

ERROR RATES
Soft errors: 1 in 10^7 is easily obtainable in typical applications.

Priced $300. and up in OEM Quantities F.O.B. Newton, Mass.
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CIRCLE 55

face (currently the most common method); a variety of plastic materials, either removable (recommended) or permanently attached to the bezel; and vacuum-deposit optical coatings. Optical coatings and bonded etched glass faceplates are typically very costly, and while plastic materials may be less reliable or durable, they are also more cost effective. The advantages of antireflective faceplates are obvious from the human engineering standpoint, but again, tradeoffs exist. Antireflective faceplates produce a diffusion effect that reduces resolution, and they also reduce light output, thus requiring a higher beam intensity to achieve the brightness as exhibited by a CRT without such treatment.

CRT-module reliability

To the display module manufacturer, a failed unit is one that doesn't meet internal product specifications due to a failure or component drift. To the terminal designer, the criteria may be completely different.

One of the gray areas in reliability considerations is the outward appearance of the display – size, brightness, character location, curvilinear distortion and jitter, for example. Many of these subjective differences can be eliminated if the terminal designer and display module manufacturer work together during the design stage, so that each understands the possibilities and limitations of the relevant components and technologies. The system designer must also work with stylists and cabinet designers to provide adequate unlit borders between the edges of the displayed character format and any cabinet bezel or fixed reference lines the terminal user can see. This practice eliminates most of the field complaints on changes in the display that result from normal drift in the electronics.

MTBF figures on CRT display modules are a fairly accurate measure of component reliability; their accuracy depends on whether the figures are real, calculated or estimated. One important reliability consideration is the cost to repair a failure. While the published MTBF of an oscillator-driven CRT display module resembles that of a direct drive (logic-driven) CRT display module, the cost of an average failure may differ considerably. A typical failure in an oscillator system requires the replacement of one or two relatively inexpensive components, while a direct-drive failure can damage the cathode ray tube.

future CRT developments

Current terminal display technology is limited to CRT systems and some relatively low-density plasma-type units. Color CRT displays will appear in more special terminal designs but will remain fairly expensive compared with monochrome displays. Multiple interlace and supervertical scan systems, as well as stroke-type character displays, may at times offer small advantages in logic cost, but the resulting display complexity usually produces a cost penalty.

Generally, the CRT display module that provides the most performance per dollar is the one that can be built using widely available components and relatively conventional raster scanning techniques. Raster-scan systems now offer the best value, and will continue to do so for several years; increased character density and larger screen sizes will become more prevalent. ♦

CRT TERMINAL REVIEW: a product sampler

Developments in the design of both CRTs and the terminals that incorporate them appear regularly, and elsewhere in this issue you've read about some of those developments. To round out this month's coverage of CRT terminals, we present this sampler of current offerings of firms in the field.

The table below outlines some key specifications of several CRTs. These terminals range in price from under $1200 to around $7000. Most of the units highlighted can be termed editing terminals; they allow operators to change copy displayed on their screens through the positioning of a cursor. Some even offer software for text editing and include the memory and intelligence for program implementation.

Where no communications protocol is specified, the terminal is asynchronous.

Company	Model	Display Size (Inches Diag.) Display Config. (lines x char) Char, Set	Comm Protocol	Data Transfer	Major Edit Functions	Program Memory (Bytes)	Price
ADDS	Consul 980	12 24 x 80 96 ASCII	None	By char, message, page	Insert/delete line or char	None	$2350 in singles
Ann Arbor Terminals	K2480D	15 24 x 80 64 ASCII	None	By char or block	Insert/delete line or char, erase to end of page or line	None	$1795 in singles
Beehive International	B500	12 or 15 24 x 80 128 ASCII	None	By char, line, page or block	Insert/delete char, page/line edit, erase char, to end of line or end of memory	2K ROM or PROM (48K RAM optional); allows 8 user-programmable keys	$2695 base
Computek	216	15 24 x 80 128-256 ASCII	BSC, SDLC, Programmable	Programmable	Full text editing, data entry package	128K RAM and PROM/RAM; allows table lookup, text ed., range check, etc.	$2300 per screen, cluster of 4 screens, in quantity
Computer Optics	CO:77	15 24 x 80 64 or 96 EBCDIC	BSC	Serial	N.A.	None	N.A.
Conrac	480/25	8" x 6.5" 25 x 80 64 or 128 ASCII	Burroughs TD700/800 Univac U100/200	By char or block	Tabs, insert/delete char or line	4K PROM or 4K RAM	N.A.
Control Data	92451	12 24 x 80 128 ASCII	None	By char, line or block	Insert/delete char or line, erase char, page or line	12K EROM; allows app. oriented features	$1900 for 50
Courier Terminal Systems	2700	13 12 x 40 or 80, 24 x 80 ASCII	BSC,SDLC	By block	Insert/delete char, erase to end of field	None	N.A.
Dataview	Marquis	12 24 x 80 128 ASCII	None	By char	N.A.	None	$1195 in singles
Delta Data Systems	4050	14 25 x 80 224 disp. char	Burroughs, Honeywell, Univac	By message or block	Insert/delete char or line, clear memory or line	4K or 8K PROM; allows text processing, field validation, multi-form storage	$2370 for 25-49 (base)
Hewlett-Packard	2649A	11 24 x 80 64 or 128 ASCII	BSC	By char, line or page	Insert/delete char or line with or without wraparound	4K or 8K RAM, 4K PROM, 2K-24K ROM	$2600-$3700 for 50-99 (U.S.A.only)

A number of the terminals listed can emulate the operation of terminals offered by mainframe vendors such as Honeywell, IBM, Burroughs and Univac. All of the units shown communicate in both half or full duplex modes, except for the Computer Optics and Courier systems, which are half-duplex only.

Data transfer modes vary from unit to unit. Some handle a character at a time. Others transfer a block at a time. And still others can handle transfers on a line or page basis.

All units accept ASCII I/O signals, except for the Courier, Hewlett-Packard, ICC and Megadata units (ASCII or EBCDIC), the Computer Optics unit (EBCDIC only) and the Computek unit (programmable). Some of the entries are intelligent, and users can run applications programs on them.

Company	Model	Display Size (Inches Diag.) Display Config. (lines x char) Char. Set	Comm Protocol	Data Transfer	Major Edit Functions	Program Memory (Bytes)	Price
ICC	System 400	15 12 or 24 x 80 127 ASCII	BSC, HIS7700, Uniscope	By block	Insert/delete char or line, cursor control	16K PROM, factory programmed	$4210-$4890 in 100s
Intelligent Systems	Intecolor 8001	19 25 or 48 x 80 64 ASCII	None	By char or block	Cursor X-Y address, write vertical or 45°, insert/delete char or line	64K total	$1495 for 1-100
Lear Siegler	ADM-2	12, 9 or 15 24 x 80 128 ASCII	None	By char, block, message or line	Insert/delete char or line, horizontal tabs, protected fields, erase line or field	None	$2495 for 1-100
Megadata	System 700	15 24 x 80 96 ASCII + 32	BSC or synch. (emulates IBM 3270, 2265, Hazeltine 2000, Uniscope 200, TTY and others)	By char or block	Full package	12K PROM	N.A.
Ontel	OP-1	14 20 x 80 24 x 80 128-256 ASCII	BSC	By char or block	Full text editing, data entry package	64K RAM or 64K PROM/ ROM/RAM	$1,795 for 100
PCC Business Systems	7100	5.5" x 8.25" 24 x 80 96 ASCII	Synch (adaptable to user's)	By char, line or block	Insert/delete char or line	2K PROM; allows protocols, cursor control, spec. functions	$2750 for 25-99
Perkin-Elmer	Owl-1200	12 24 x 80 96 ASCII	None	By line, page or message	Insert/delete char or line, clear screen, clear unprotected, clear line (field)	N.A.	$1496 for 25
Tandberg Data	TDV-2100	15 25 x 80 128 ASCII	BSC	By char, line or page	Insert/delete char, line or word	64K ROM/ PROM; allows table lookup, range check, text edit.	$5800 for 1-9
TEC	Teletec 1445	12 24 x 80 128 ASCII	None	By char	All editing from CPU	None	$1225 for 26-50
Telray	3841	12 24 x 80 96 ASCII (displayable)	None	By char	Erase screen, erase to end of screen and end of line	None	$1450 in singles
Teletype	40/2	13 24 x 80 127 ASCII	None	By char or block	Insert/delete char or line	None	$5322-7098

HP'S CRT LETS USERS CUSTOMIZE TERMINALS

With both an HP 13290A Development Terminal and the HP 2649A Mainframe Terminal, the technically oriented user can design custom firmware in order to produce a CRT terminal specialized for a particular application. Hewlett-Packard's Development Terminal consists of a keyboard, display, dual Mini Cartridge mech-

anisms, and communications interface, all controlled by an integral microprocessor. A binary loader stored in ROM can transfer microprocessor instructions from Mini Cartridges to 24K bytes of writeable control store. After debug, users can purchase multiple 2649A Mainframe Terminals and can pick from a variety of modules to produce a hardware configuration designed to fit the particular application.

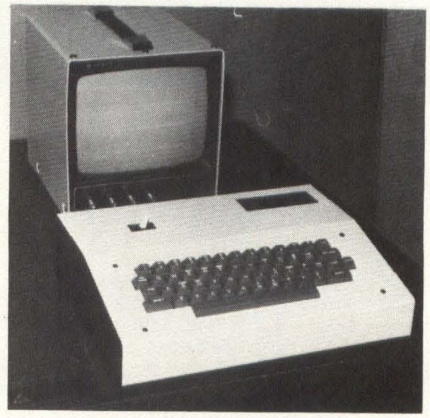
OWL AND FOX COMPRISE PET TERMINAL LINE

Perkin-Elmer Data Systems Terminal Division has entered the CRT marketplace with two Pet terminals. The OWL-1200 is an asynchronous editing CRT with a full range of field attribute controls and an optional line drawing capability. The Fox-1100 is a low-cost asynchronous CRT with a 24 X 80 display, upper and lower case characters, and full cursor addressing and control. Both units are designed around the 6800 microprocessor. The field attribute capabilities of the

OWL-1200 include inverse video, half intensity, blink, numeric only, protected, non-display and modified data field definitions. OWL-1200's line drawing capability permits exact images of source documents to be displayed. This is said to reduce operator training time and error rates.

CRT TERMINAL FEATURES DETACHABLE KEYBOARD

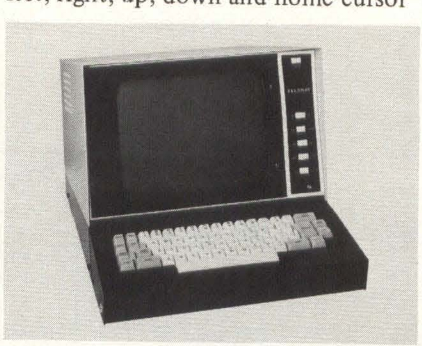
Terminal Data Corp.'s Teletype-compatible CRT terminal features switch selectable speeds to 9,600 baud, switch selectable parity, automatic line feed and page erase. Model 675's screen can be located



up to four feet from the keyboard. Weighing ten pounds, the CRT comes with an RS232C interface which can be replaced at the users option with a 20 milliamp current loop interface. Under a 12-month lease, model 675 with monitor, keyboard workstand leases for $39 per month.

TELERAY ENTRY HANDLES X-Y ADDRESSING

Model 3841 CRT terminal from the Teleray Division of Research Inc. provides left, right, up, down and home cursor



movements either by use of control characters or ESCAPE sequences. Cursor movements can be controlled from the keyboard or from a remote source. Available on the keyboard for cursor control are the back space key (cursor left), tab key (cursor right), line feed key (cursor down), and Control +K keys (cursor up). Absolute X-Y positioning is accomplished by a four character sequence – ESCAPE followed by "Y" followed by a line code followed by a column code. The company claims that this feature reduces the amount of communications time required to position a cursor from the computer when compared to the normal incremental cursor control commands.

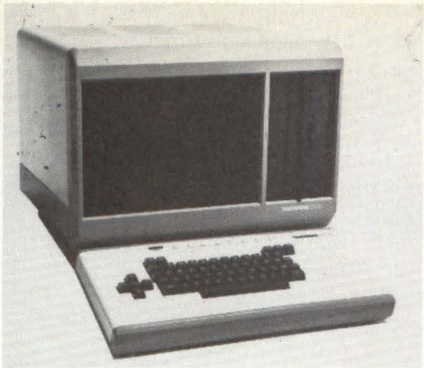
COURIER UNIT SUITS BOTH LOCAL AND REMOTE CLUSTERS

Courier Terminal Systems, Inc.'s model 2700 display terminal is designed for local operation using Courier's Local Terminal Controller (LTC) or Virtual

Line Controller (VTLC) and for remote operation using the Remote Terminal Controller (RTC). Model 2700 connects to Courier controllers for clustered operation with a centrally located IBM 360/370 or any mainframe supporting the 3270 BSC or SDLC line protocol. Up to 32 intermixed model 2700 screen sizes and any or Courier's printers attach to the LTC, VTLC or RTC.

TANDBERG OFFERS VERSION FOR EVERY NEED

Tandberg Data, Inc.'s TDV 2100 series of display terminals and systems gives users a complete line from Teletype-compatible terminals to advanced units that include processing capability and mass storage. Model TDV 2155 is a Teletype-compatible data display. The model TDV 2116 offers a buffer so that data can be prepared on a page basis and transfered to the computer as such. And the model TDV 2114 is an intelligent terminal built around a microprocessor.



For data entry applications, the TDS 8020 records information on floppy disks. And the top of the line TDS 8030 lets a clustered display system communicate with a central computer over a single communications line.

LOW COST CRT HAS CURSOR CONTROL KEYS

For $1,225 in quantities of 50, users can buy TEC, Inc.'s Teletec model 1445 teletypewriter-compatible CRTs. Model 1445 operates at 15 switch selectable speeds from 50 to 9,600 baud. A detachable keyboard uses TTY formats for easy operator adaptation. Twenty-three standard switch selectable options are accessible from the rear of the unit. Five cursor control keys move the cursor in four directions as well as to the home

position. The Teletec model 1445 can interface to a computer in three ways; RS232C, 20/60 milliamp current loop or TTL.

MARQUIS AIMED AT TTY REPLACEMENT MARKET

Intended to serve as a teletypewriter replacement, Dataview's Marquis display terminal features TTY current loop and RS232C communications capability. Transmission speeds are switch selectable from 50 to 9,600 bits/second. One externally controlled speed provides a transmission rate of 1,800 characters/second. Further, both parity and full/half duplex operation are switch selectable. Display

characteristics include 80 characters/line, 24 lines/display, 64 character ASCII set and 5 X 7 dot matrix upper case character format.

TERMINAL FEATURES BATCH TRANSMIT OPTION

Ann Arbor Terminals, Inc. has released its K2480D terminal with a new batch transmit option. This option equips the

KSR unit with a screen-transmit capability that enables the operator to write to the screen off-line at typing speed, and then transmit the data to the computer at a faster speed. The company has also released an edit option for that terminal which allows users to edit both complete lines of text and line fragments from the cursor's position to the end of a line. This edit option can be added to terminals that already include the batch transmit option.

COMPUTEK UNVEILS SERIES 216 LINE

Computek, Inc. has just announced a new line of intelligent terminals that feature a 16-bit LSI microcomputer and up to 128K bytes of internal memory. These terminals can exist in standalone configurations or in clustered systems and they will support peripherals such as disk drives, magnetic tape units, character and line printers. An exclusive linked-list memory structure for display refresh allows up to 1,920 characters of screen data to reside anywhere in memory. Screen data is linked to the next list by a special "link" word which precedes the list. Each character displayed on the

screen can contain any of five attributes – bright, blink, underline, reverse video and either blank or horizontal slash. In autumn, Computek expects to release a data entry package for series 216 which will use ISAM search and replace techniques.

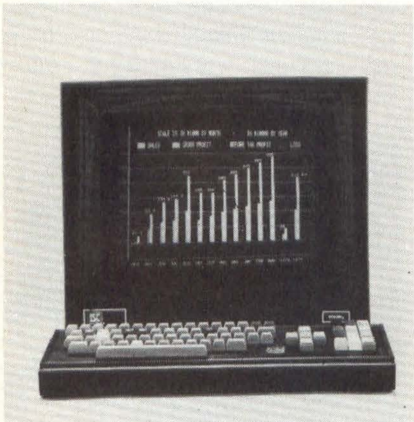
DELTA 4050 SUITS MULTIDROP NETWORKS

Delta Data Systems Corp.'s model 4050 display terminal works in multidrop data communications networks that use Burroughs, Honeywell or other computers. This microprogrammable CRT terminal can be interconnected with many ter-

minals on the same communications line and linked to a central computer for random or sequential polling. With this daisy chain capability, many terminals can connect to a central computer via a single modem. Four 8-position switches permit selective group or individual terminal addressing. This is said to allow optimum use of the intelligence capabilities of the terminals in a data communications network.

INTELLIGENT CRT SPORTS THREE MICROPROCESSORS

Ontel Corporation's OP-1 series of intelligent terminals uses up to three microprocessors – one for display, another for



CPU and the third for I/O. Designed in a modular format, the OP-1 series lets users design any terminal systems such as basic interactive keyboards operating on-line to a host computer, intelligent data entry stations, text editing or word processing work stations and full remote batch systems. Nine controllers will interface disks, diskettes, tapes, printers, more processors, and a range of communications systems to the OP-1.

PERTEC CRTS FEATURE PROGRAMMABLE PROTOCOLS

Pertec Business Systems Division has offered the model 7100 CRT display terminal with data communications protocol

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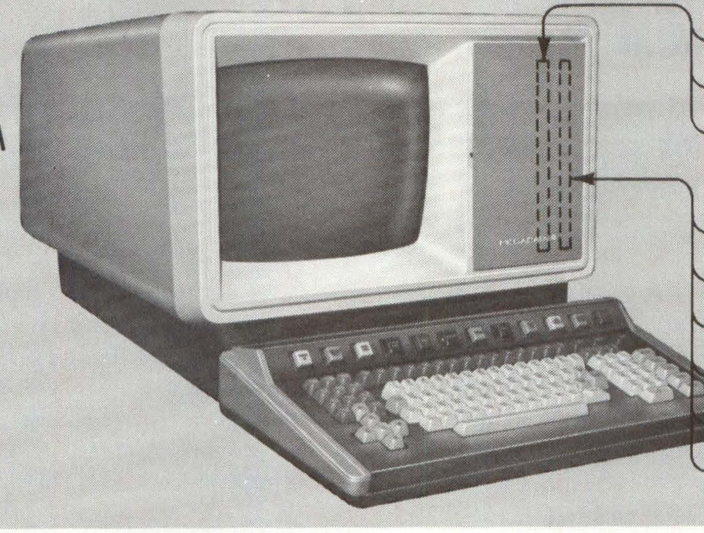

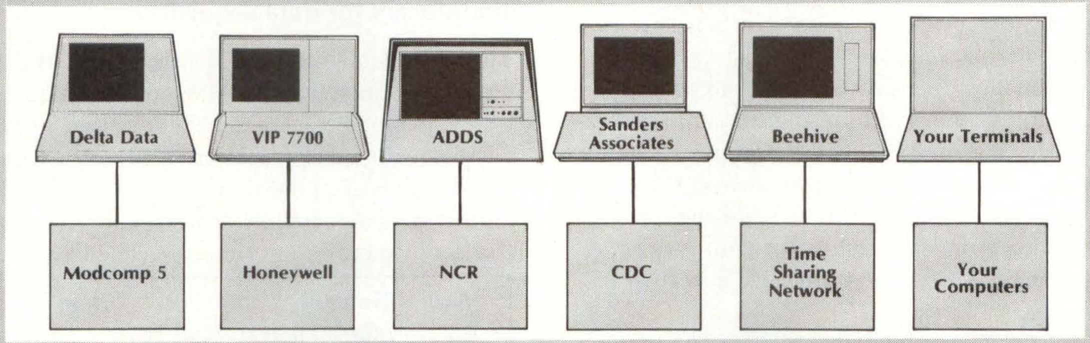

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CIRCLE 59

BALANCING µP-INTERFACE TRADEOFFS

Should you implement a microprocessor-transducer interface primarily in hardware or software? Some thoughts on how to treat Motorola 6800 systems.

by **Michael Hordeski**

At first glance, you might think that designing data acquisition interfaces for small digital systems is a cut-and-dried process, one that draws on a few traditional techniques, each with its advantages and disadvantages. Not so – the process is an art, and close study and careful partitioning can optimize data acquisition interfaces in terms of both hardware and software.

Your primary concern when designing an interface to link data acquisition components with a digital processor must revolve around data transmission. Most transducers output analog signals; you must first decide whether to remotely convert those outputs to digital form and transmit them to the processor using digital techniques, or transmit the outputs using analog techniques and convert them at the processor. Next, you must decide whether to make the conversion hardware or software-oriented. And if your system contains digital transducers, you must decide how to deal with them.

In all cases, strive to achieve digital transmission over a minimum number of parallel wires, with a minimum number of hardware connections and a minimum number of software-control memory locations. The details of your design depend on the type of transducers your system incorporates; I'll examine a few examples here. Your design also depends on the processor your system uses; I focus on Motorola 6800 systems, but many of the techniques I'll discuss also apply to other microprocessors.

transducers for data acquisition

Most commonly used transducers detect either temperature or pressure changes. Some temperature transducers – filled system thermometers or bimetallic sensors, for example – convert the thermal expansion of a liquid or solid into proportional electrical signals. Others – resistors, diodes, thermistors or thermocouples, for example – sense temperature changes by monitoring changes in conductivity or voltage.

Michael Hordeski *is president of Siltran Digital, Silverado, CA. Consultant A. Haemming, also based in that city, assisted him in preparing this article.*

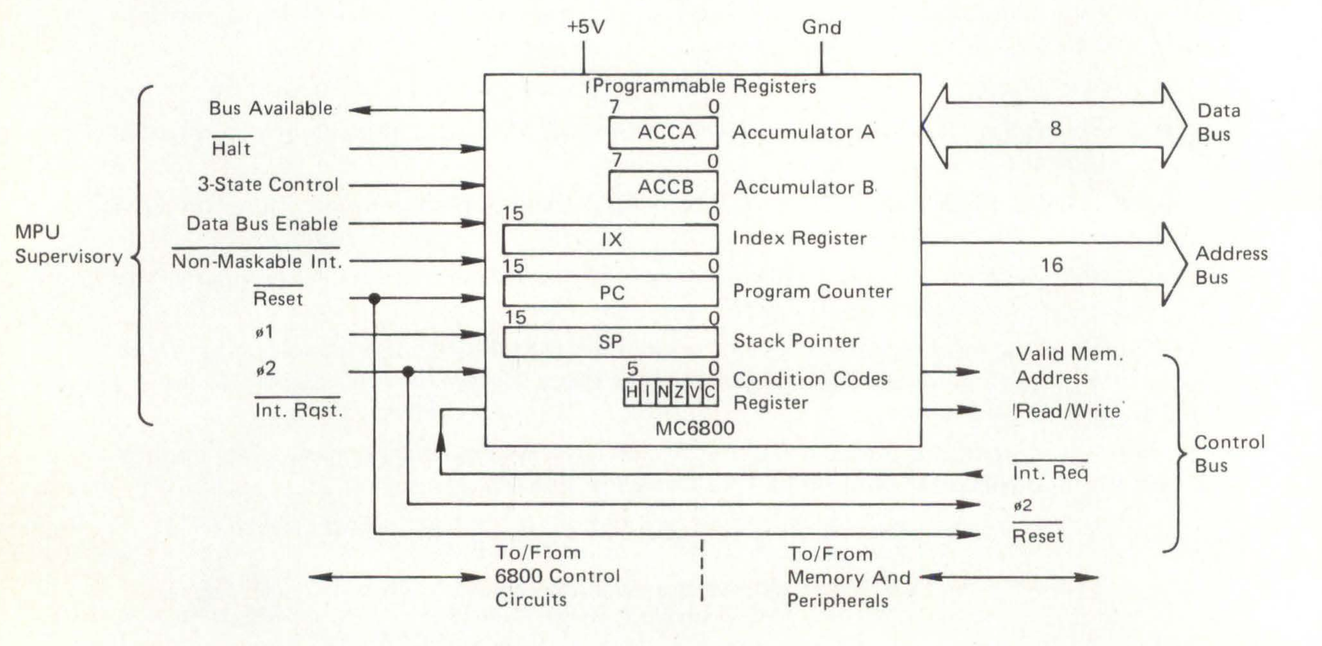


Fig 1a MC8000 bus and control signals.

Silicon diodes cover the -200 to 200°C range, while thermistors operate over -240 to 300°C. Resistors and thermocouples operate over -272 to 1600°C and -250 to 1600°C, respectively; the resistor based units are useful for measuring average temperatures, while thermocouples require reference calibration junctions.

Pressure transducers function by converting a mechanical change in a sensing element into a proportional signal. Strain gauges and piezoelectric units produce such signals directly, although the outputs require some conditioning. Diaphragms and Bourdon or straight tubes generate signals through potentiometers, variable reluctance or capacitance devices, or encoders. Diaphragm units work at up to 1000 psi; Bourdon tubes and strain gauges register as much as 200,000 psi; and most other types register up to 10,000 psi.

Analog transducers output either voltages in the 1-5, 2-10, 5-25 or ±10 V ranges or currents in the 1-5, 4-20 or 10-50 mA ranges. Digital transducers fall into two basic categories. Some incorporate a sensing unit as part of an oscillator circuit and determine the frequency of that circuit as a function of the measured quantity. Others detect the position or a primary sensor and convert that quantity into a coded digital word.

interfacing analog transducers

I'll discuss how you can interface the voltage-output type of analog transducer and the coded type of digital transducer with several Motorola 6800 system configurations and show how your interface can achieve minimum hardware usage or minimum software usage in each system. In all cases, I'll maintain the primary constraints of digital transmission with minimum wiring, connections and memory.

The Motorola 6800 (Fig 1) requires an adapter – designated the 6820 PIA – to interface with I/O equipment. A control bus channels data flow in the PIA's data bus, and an address bus lets the 6800 read or write into the PIA's registers. Divided into two independent sections, each with a control, data and address register, the PIA's register group has two sets of eight parallel I/O lines (PA0-7 and PB0-7) and two sets of two control mode lines (CA1-2 and CB1-2.) A data direction register in each section determines the status (input or output) of the P lines.

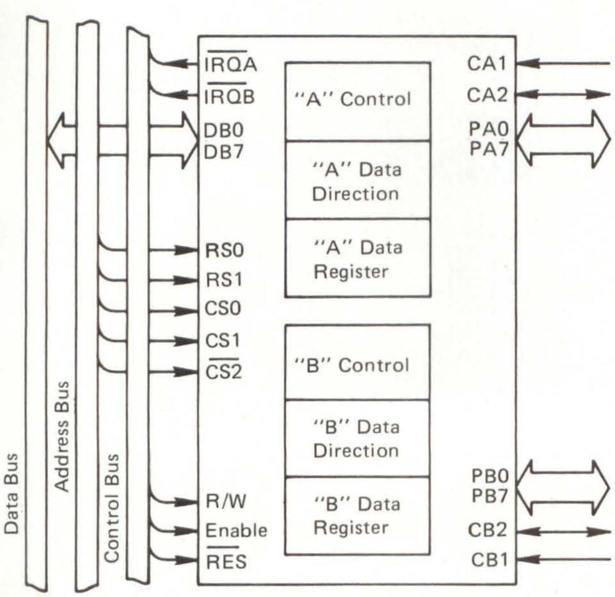


Fig 1b MC6820 PIA I/O diagram.

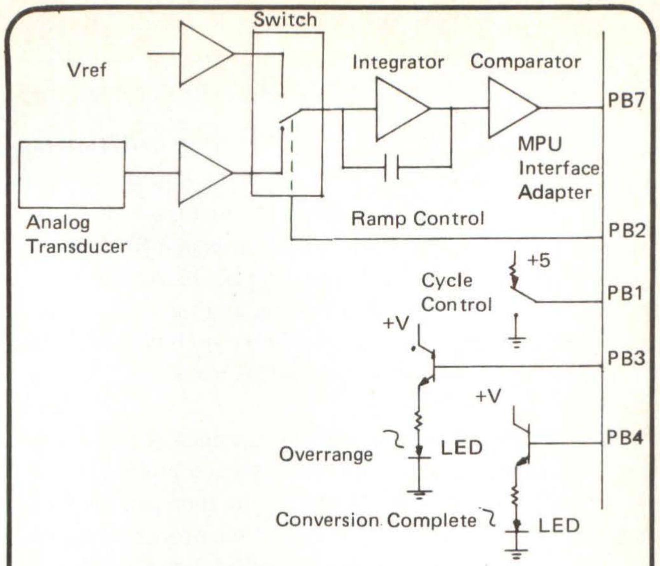


Fig 2 Interface connections for 12 - bit software oriented mechanization.

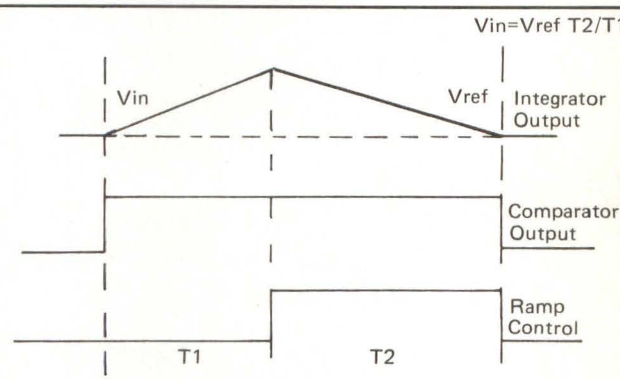


Fig 3 Dual slope or ramp-timing diagram.

Suppose you wish to connect this microprocessor system to an analog transducer with an interface that uses a minimum amount of hardware. The interface shown in Fig 2 achieves that goal; it uses dual-ramp A/D conversion, outputs 12-bit signals and allows 2-wire digital transmission with a minimum amount of wiring connections.

Using the dual-ramp A/D conversion technique (Fig 3), the circuitry integrates the transducer's output for a fixed number of clock periods during time T1; at the end of T1 the integrator's voltage is proportional to the transducer's output. The circuit then applies a lower reference voltage to the integrator's input, and the integrator's voltage decreases to this reference level in time T2. This ramp control time is proportional to the input voltage; by comparing it with the comparator output time (T1), the microprocessor calculates the value of the transducer's output.

In the software that performs this comparison (Fig 4), lines 16-22 program the interface connections and lines 25 and 26 provide memory locations that store the final answer \$0000 and \$0001. The first hexadecimal location contains the answer's four most significant bits, while the second contains the rest of them. Lines 37-42, the first instructions, initialize the PIA's input and output configuration, while lines 46-49 set the ramp control and test the comparator output to ensure that it lies below the reference voltage level when conversion begins.

The software sets a conversion-finished flag, and the microprocessor enters the loop shown in the flow chart. This loop operates on the PB1 cycle input from the PIA and starts a new cycle by resettling the conversion-finished flag when the ramp control goes low. The hexadecimal number \$2000, loaded into the index register and then decremented, provides ramp-up timing. Lines 67-69 switch the comparator output from low to high and cause the microprocessor to enter this ramp-up timing cycle.

Continuing the comparison process, lines 74 and 75 increment the index register when the depletion process is complete; a dummy statement equalizes the time periods for ramp up and ramp down to maintain the proper timing ratio. At the end of the ramp-down period, line 82 stores the

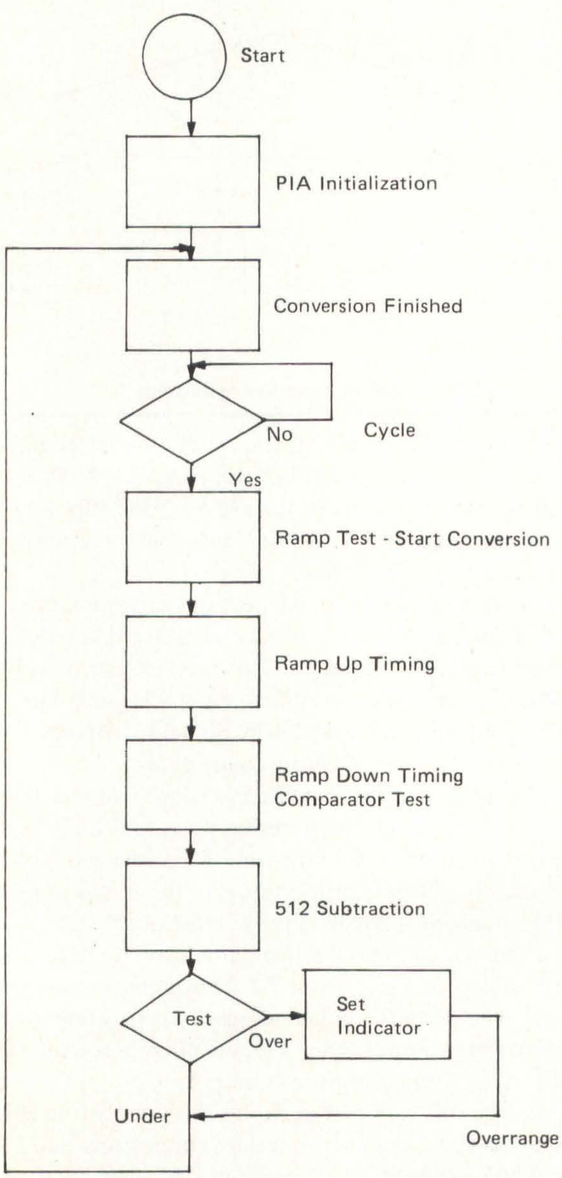


Fig 4a 12-bit software oriented flow diagram.

```
 1. NAM DWA10
 2. OPT MEM
 3. *
 4. *
 5. *
 6. *
 7. *
 8. **
 9. *
10. *  12-BIT SOFTWARE ORIENTED MECHANIZATION
11. *
12. **
13. *
14. *
15. *
16. *                 INPUT/OUTPUT PIA  LOCATIONS
17. *
18. *                 RAMP CONTROL (OUTPUT)   PB2
19. *                 CYCLE CONTROL (INPUT)   PB1
20. *                 OVERRANGE (OUTPUT)      PB3
21. *                 CONVERSION COMPLETE (OUTPUT)  PB4
22. *                 COMPARATOR OUTPUT (INPUT)     PB7
23. *
24. *
25.  ORG $0
26. TEST RMB 2   FINAL 12 BIT ANSWER MEMORY LOCATIONS
27. *
28.  ORG $4004
29. PIA1AD RMB 1
30. PIA1AC RMB 1
31. PIA1BD RMB 1  B SIDE, DATA REGISTER
32. PIA1BC RMB 1  B SIDE, CONTROL REGISTER
33. *
34.  ORG $0A00    BEGINNING ADDRESS
35. *
36. *                     **PIA ASSEMBLY**
37.  CLR PIA1AC
38.  CLR PIA1BC
39.  LDA A +$7C
40.  STA A PIA1BD  SET PIA TO HAVE 3 INPUTS AND 5 OUTPUTS
41.  LDA A +$04    SET BIT 3 OF PIA CONTROL REGISTER
42.  STA A PIA1BC
43. *
44. *
45. *
46.  LDA A +$04
47.  STA A PIA1BD         RAMP CONTROL HIGH
48. START LDA A PIA1BD    COMPARATOR TEST TO ENSURE THAT RAMP IS LOW
49.  BMI START            STARTS CONVERSION
50. RSTART LDA A +$14
51.  STA A PIA1BD         CONVERSION READY - RAMP CONTROL HIGH
52. *
53. *
54. *                          **CYCLE TEST**
55. CYCLE LDA A PIA1BD
56. AND A +$02
57. BEQ CYCLE
58. LDX +$2000            INITIALIZATION FOR RAMP UP TIMING
59. *
60.  CLR PIA1BD           RESET OVERRANGE - CONVERSION COMPLETED
61. *                     AND SET RC LOW
62. COMP LDA A PIA1BD
63. BPL COMP
64. *
65. *
66. *                     **RAMP UP TIMING CYCLE**
67. RAMPUP LDA B +$04
68.  DEX
69.  BNE RAMPUP
70. *
71. *                     **RAMP DOWN TIMING CYCLE**
72. *
73. *
74. RAMPDN STA B PIA1BD  RC HIGH
75.  INX
76.  CPX +0000            DUMMY STATEMENT FOR TIME DELAY
77.  LDA A PIA1BD         COMPARATOR TEST
78.  BMI RAMPDN
79. *
80. *
81. *
82.  STX TEST
83.  LDA A TEST           512 COUNT SUBTRACTION
84.  SUB A +$02
85.  STA A TEST
86.  SUB A +$10           OVERRANGE TEST
87.  BCS RSTART
88.  LDA A +$1C           SET CONVERSION FINISHED - OVERRANGE
89.  STA A PIA1BD         AND SET RAMP CONTROL HIGH
90.  BRA CYCLE
91.  MON
```

Fig 4b Cross assembler source instructions (Motorola time-share system).

\$Hexadecimal, % Binary, @ Octal

contents of the index register in locations $0000 and $0001. The software then allows for offset counts by subtracting $01 from $0000 and storing the result in $0000. An overrange test checks the contents of location TEST for a number greater than 4095; if such a number is there, conversion is complete; if not, the microprocessor branches back to line 50.

Now suppose you wish to connect the 6800 system to an analog transducer with an interface that requires a minimum amount of software. Fig 5 shows such a hardware oriented interface and its software; the circuit generates a 3½-digit input to the PIA, reduces the required number of transmission lines and instructions, and offers display capabilities. If you tried to implement this interface using less hardware and more software, you'd have to use a binary-to-BCD converter and almost three times as many memory locations.

In the interface's software, lines 18-25 and 36-39 simulate the main microprocessor program; the conversion subroutine starts at line 42. The software then sets the display update low and allows data to enter the circuitry's latches. A WAI instruction stores the microprocessor stack until the comparator output causes CA1 to interrupt, and then control goes to line 50, which demultiplexes the BCD input data. A pointer selects the least significant digit, and when the pointer's line (PA5) switches low, the BCD data goes to location $0100. The pointer then shifts, and when PA6 goes low the next digit goes to location $0101. The most significant digit and the half digit then go to locations $0102 and $0103 respectively, the display update line switches high, and the microprocessor returns from the interrupt and subroutine to the main program that requested the data.

interfacing digital transducers

Using digital transducers can simplify your microprocessor-system interfaces even further. For example, to achieve minimum software usage, you could in some systems connect each of the eight outputs of a digital transducer to a corresponding PA line in the PIA. Unclocked, the transducer outputs present a constant word, which the microprocessor can

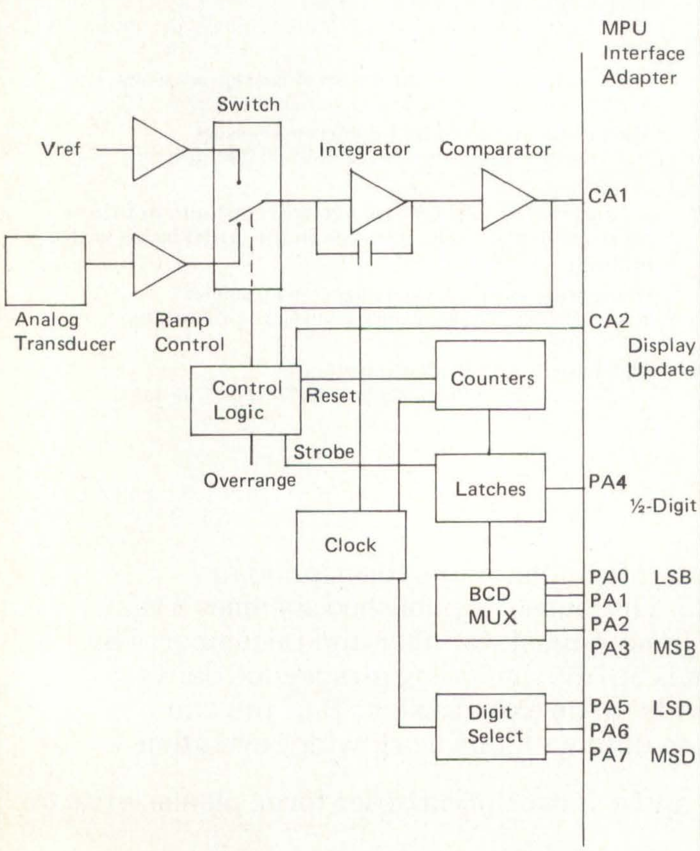


Fig 5a Interface corrections for 3½ digit hardware oriented mechanization.

```
 1. NAM DWA4
 2. OPT OT
 3. *
 4. **
 5. *          3½ DIGIT HARDWARE ORIENTED MECHANIZATION
 6. *
 7. **
 8. *
 9.  ORG $0010
10. POINTR RMB 1                 DIGIT SELECT POINTER
11. *
12. *
13.  ORG $400A
14. PIA1AD RMB 1
15. PIA1AC RMB 1
16. *
17. *
18. *                **PIA1AD CONFIGURATION**
19. **
20. *PA7*PA6*PA5*PA4*PA3*PA2*PA1*PA0*
21. **
22. *MSD      LSD   *½D*   MSB       LSB*
23. **
24. *  DIGIT SELECT  *    *  BCD  *
25. **
26. *
27. *                RESULTS STORED IN LOCATIONS 0100-0103
28. *                   LSD=0100    ½DIGIT=0103
29. *
30.  ORG $0900
31.  CLI
32.  CLR PIA1AC        PIA ASSEMBLY
33.  CLR PIA1AD
34.  LDA A +$3C
35.  STA A PIA1AC
36.  LDS +$0020
37. *
38. *
39.  NOP               MAIN PROGRAM SIMULATION
40.  JSR CONVRT
41. END NOP
42.  BRA END
43. *
44. *
45. CONVRT LDA A +$35     A/D CONVERSION SUBROUTINE
46.  LDA B PIA1AD         DUMMY READ OF PIA DATA REGISTER
47.  STA A PIA1AC
48.  WAI
49.  RTS
50. *
51. *
52. *
53. *
54. BEGIN LDA A +$20     BEGINNING OF INTERRUPT PROGRAM
55.  STA A POINTR
56.  LDX +$0100
57. NEXT LDA A PIA1AD
58.  TAB
59.  AND A POINTR
60.  BNE NEXT
61.  ROL POINTR
62.  AND B +$0F
63.  STA B 0,X
64.  INX
65.  BCC NEXT
66.  LDA A PIA1AD
67.  AND A +$10
68.  LSR A
69.  LSR A
70.  LSR A
71.  LSR A
72.  STA A 0,X
73.  LDA A +$3C
74.  STA A PIA1AC
75.  RTI
76. *
77. *
78. *
79.  MON
```

Fig 5b 8-bit mechanization with minimum software for

CIRCLE 84▶

sample at any rate. Even for a relatively long sampling period, only the least significant bits will change during the measurement of most parameters, and the measurement error will equal about 1% (less than two parts in 256). This configuration requires software only to define its connections as inputs; sampling occurs under main program control.

How can you achieve minimum hardware usage in an interface for a digital transducer? In one such software oriented interface (Fig 6) a digital transducer with a serial output requires two connections – PA0 and ground – with the PIA. The flow diagram shows one way to simulate the serial-to-parallel register this interface requires. The software defines PA0 and cycle control PA1 as inputs and PA3 as an output to control the interface's conversion-finished LED (you can eliminate this PA3 output if you make the program a subroutine of a larger control program).

The software's cycle loop causes the microprocessor to wait until PA1 switches high and then clears a memory location for use as a pointer that tracks bit processing. The program rotates the carry bit and resets the conversion-finished line, and it uses a conditional branch to determine if all eight bits have been tested. After nine rotations, the program again sets the carry bit to signify that all bits have been checked; it uses another branch for bit testing and pointer control and prepares all bits for the microprocessor.

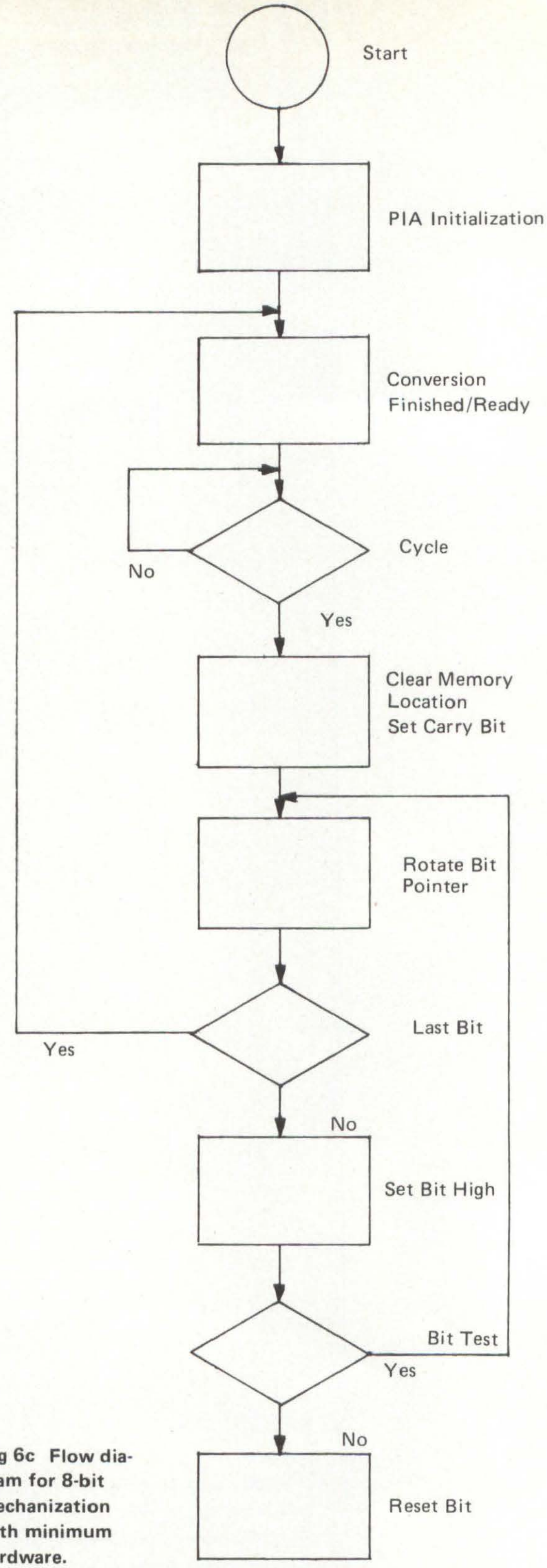


Fig 6c Flow diagram for 8-bit mechanization with minimum hardware.

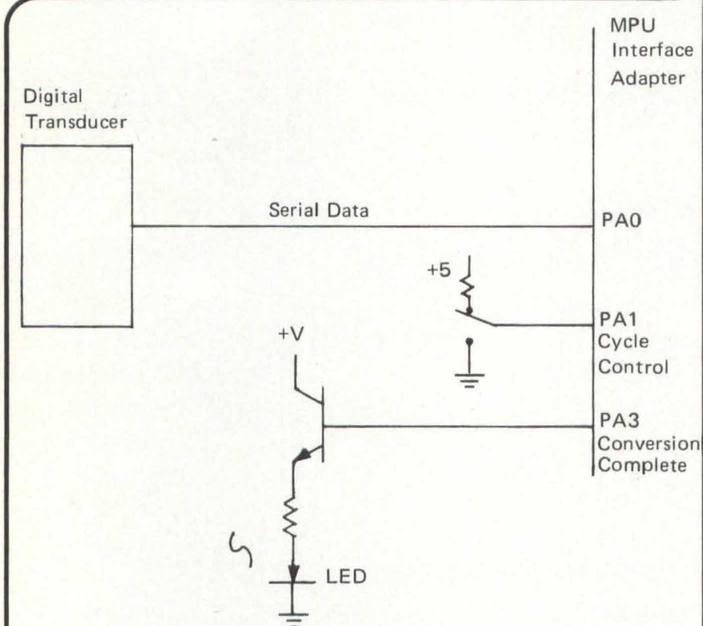


Fig 6a Interface connections.

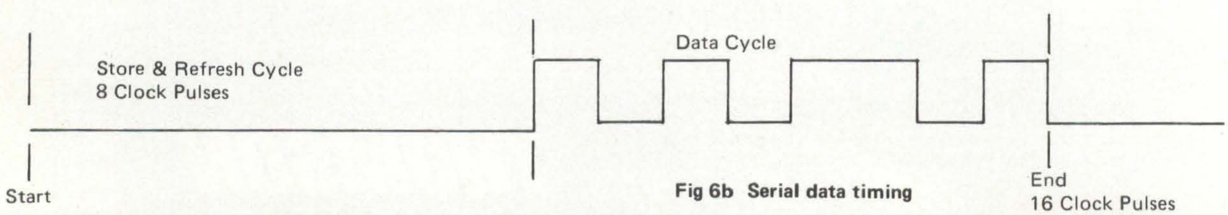


Fig 6b Serial data timing

designers' notebook

Hybrid DP bit-synchronizer resists noisy interference

Left unchecked, high noise levels can scramble electrical signals, distort information and otherwise disrupt the operation of data processing equipment. And one important component of a data processing system, the bit synchronizer, is especially sensitive to such noise. This unit detects and synchronizes data demodulation and decoding, and converts received analog signals to digital equivalents.

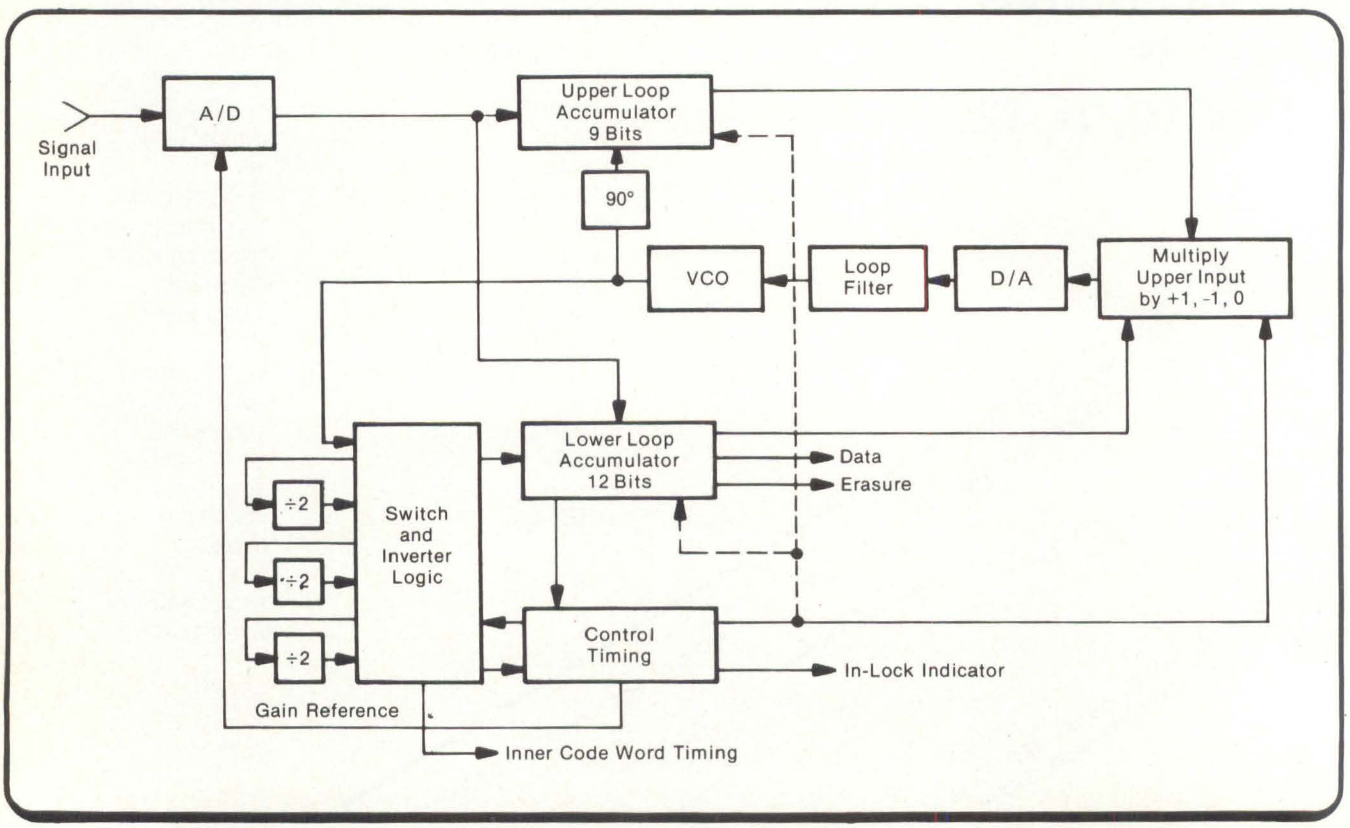
Unable to completely shield equipment from severe noise, you can still guard against its effects by utilizing a noise-resistant bit synchronizer developed at Raytheon Co. under contract to NASA's Johnson Space Center. This hybrid, general-purpose device combines analog and digital circuitry in a decision-directed feedback loop, modified to suit Biphase-L, NRZ or PSK-Biphase-L signal formats.

The synchronizer first locks onto and then tracks a rapid-acquisition-sequence clock component while acquiring both bit and word synchronization during the rest of its acquisition mode. To boost hardware economy, the same circuitry controls both the acquisition and tracking modes: a bit demodulator in the tracking mode also functions as a sequence cross-correlator during acquisition. The same device also activates the circuit's automatic gain control. Transition from the acquisition to the data transmission mode occurs automatically and requires no return communication, say the circuit's developers, J. Stiffler and A. Van Doren.

In the acquisition mode, the synchronizer's lower-accumulator (matched filter) bit detector serves as an overflow indicator. During word synchronization, this device also divides an internal-locked clock by increasing powers of two and correlates the results against received data. With each operation, the lower accumulator indicates the correlation with either a positive or negative overflow.

To implement the upper-loop multiplier and remove upper-loop modulation, Stiffler's and Van Doren's synchronizer recognizes a nondetectable bit (erasure) and multiplies the upper-loop accumulator's output by zero under low signal-to-noise ratios. As a result, they note, the circuit avoids erroneous updating by not updating the loop at all.

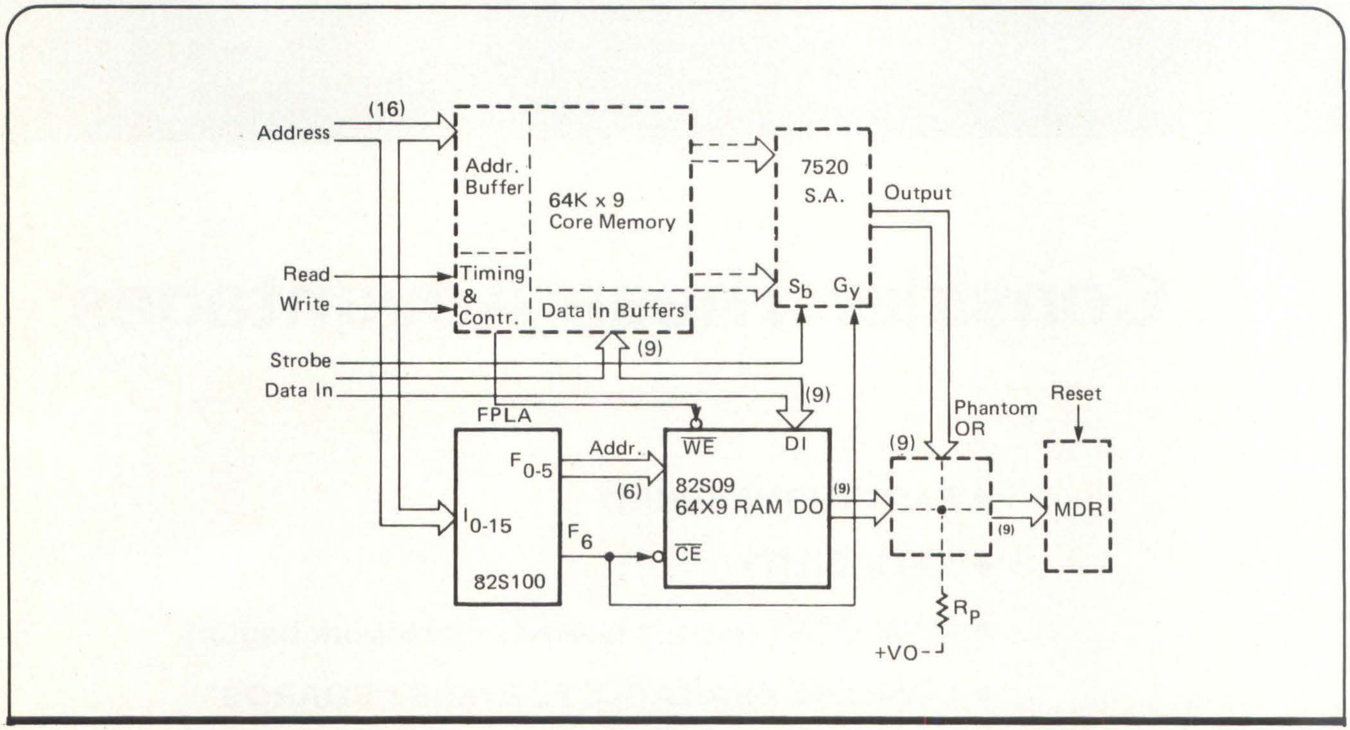
To ensure rapid, coarse adjustment, the circuit maintains a short integration interval during acquisition mode. For slower, smoother reaction during track mode, this interval increases. At a 3-dB post-detection signal-to-noise ratio, the total acquisition procedure can take place in under 0.5 sec, report Stiffler and Van Doren. False synchronization and synchronization failure probabilities approach 10^{-18} and 5×10^{-3}, respectively, they add.



FPLA 'patches' cut core-repair costs

A typical 64K x 9 add-on core memory system incorporates two core planes, each holding about 300K cores – up to 100 of which can prove broken or improperly tested.

One method of repairing these defective cores – a hand "restringing" procedure – involves replacing each malfunctioning device at a cost of about $2/core. An even more effective repair technique entails using an auxiliary memory to patch all addresses that incorporate faulty devices. But patching memory locations with PROM usually proves expensive; because flaws can appear anywhere in the core plane, you need an auxiliary memory with an address field as large as the original memory's.



A field programmable logic array (FPLA), however, incorporates a programmable address matrix that lets you choose any finite subset from a large number of input states. The FPLA thus provides greater address selectivity than a PROM, which utilizes a fixed decoder to access all internal words, explains Napoleone Cavlan, manager of advanced products marketing at Signetics Corp., Sunnyvale, CA.

This increased address selectivity reduces memory-size requirements and thus reduces hardware costs, he claims. One memory user, for example, reported that one FPLA costing $21 replaced 49 ICs costing $1 each in an aircraft automatic landing system. In that same application, the FPLA occupied 2 in^2, compared with 50 in^2 for the random logic.

Used as a core-memory patch, an FPLA can map the location of defective bits in its "AND" matrix and use sequential address pointers to direct its output "OR" matrix to a small auxiliary RAM that stores the correct data. In one such patch, a 16-input FPLA serves as an address map and a 64K x 9 RAM provides auxiliary memory. The FPLA's 48 P-terms let you dynamically repair 48 core-memory addresses situated anywhere in the core plane, and six FPLA outputs programmed as a binary table address the correct data, stored in the 82S09 RAM.

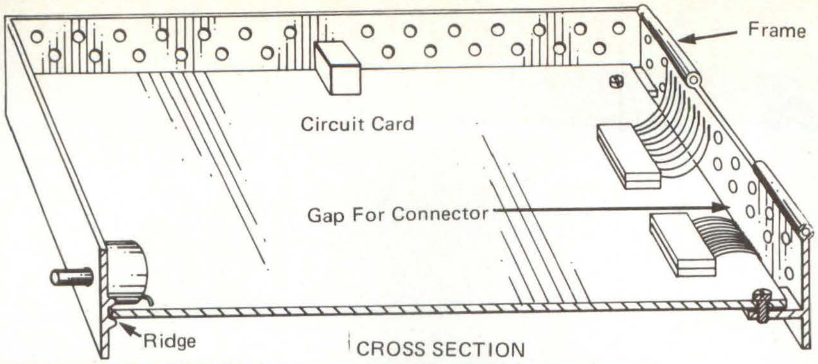
To jam the contents of the MDR's auxiliary memory when you address a faulty core location, the FPLA's F_6 output provides memory-select control, which also lets you write in auxiliary memory only at the patched addresses.

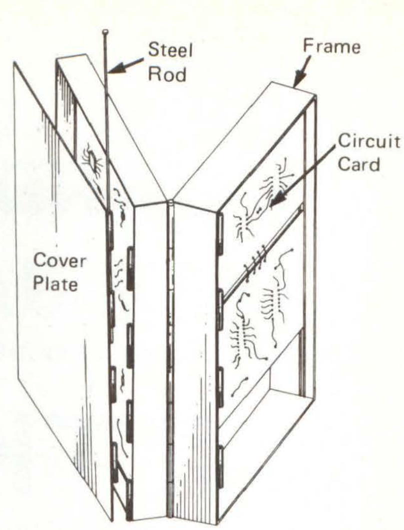
Core memory systems usually incorporate sockets and connections for both the FPLA and the auxiliary RAM. Immediately after the final test, program the FPLA input table with the addresses of core failures, says Cavlan.

With appropriate modifications, you can also apply this patching technique to memory systems that incorporate partially functional bipolar or MOS memories, he notes. You can also apply the technique to ROM systems or utilize spare PROM locations to extend the circuit-package life following random or repeated changes.

Hinged frames improve system expandability

When specifying packaging systems for their designs, today's systems engineers most often choose plug-in card arrangements, in which circuit cards attached to edge connectors communicate through backplane wires or a mother board. Such systems can offer compactness, but they can also lack expandability, often provide poor communication between their component circuitry and the outside world, and accommodate a limited number of component types, claims Olav Naess, computer programmer and electronics hobbyist from Bergen (Welhavensgt. 65), Norway. To deal with these difficulties, Naess has devised an alternative, hinged-frame packaging technique, for which he has applied for a patent. Here is his report on the

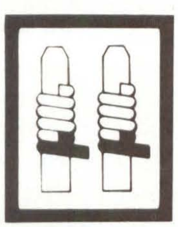


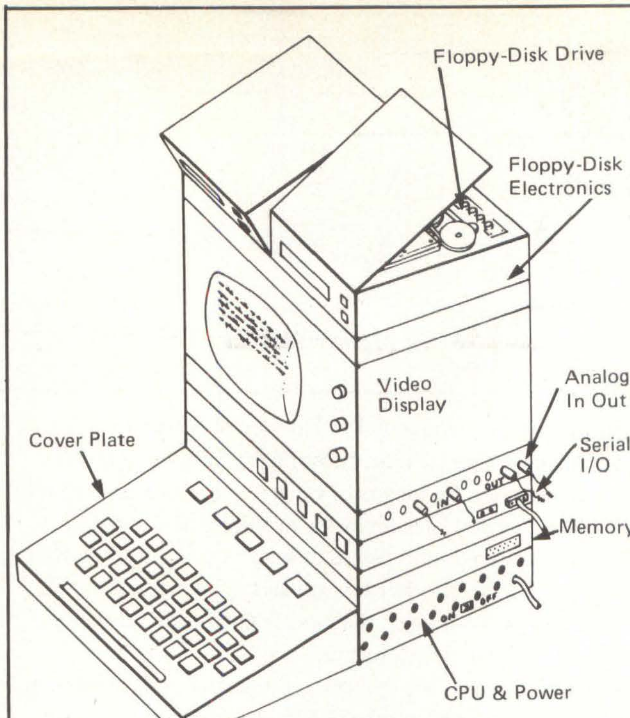


hinged-frame system, special to Designers' Notebook: In the hinged-frame system, circuit cards mount in metal frames that attach by means of hinges to each other and to cover plates; removable steel rods in the hinges allow a designer to join frames and plates in many combinations. Flat cables or a flexible mother board can connect the system's circuit cards at the hinges; the card frames and end plates constitute a complete enclosure.

One advantage of the system is flexibility; a designer can combine an unlimited number of modules in one properly enclosed apparatus, split a system into several subsystems or merge two subsystems together. Conventional enclosures, by contrast, often can't accommodate the additional communication points (controls, contacts and displays) required by newly added modules.

A module in a hinged-frame system can house all required communication points on its frame, and the enclosure formed by a group of such modules can have communication points on up to four sides, including a front panel. The connections between circuits and their communication points remain short, fixed and unaffected by module changes or additions. A system's end plates can function as control panels, and less-frequently used controls and indicators can mount on a framed board behind the system's end plate. A hinged-frame system can open like a book while all its mod-





SMALL-COMPUTER APPLICATION

ules continue to function, a capability that should please service technicians.

The packaging system offers some additional capabilities as well. A module can contain a metal chassis instead of a circuit card or can hold several small cards mounted side by side as submodules. A designer can mount mechanical units like floppy-disk and cassette-drives in frames or in frame-compatible hinged boxes. Finally, shield plates and ground planes can mount in or between frames, and heat-generating components mount in perforated frames to ease cooling.

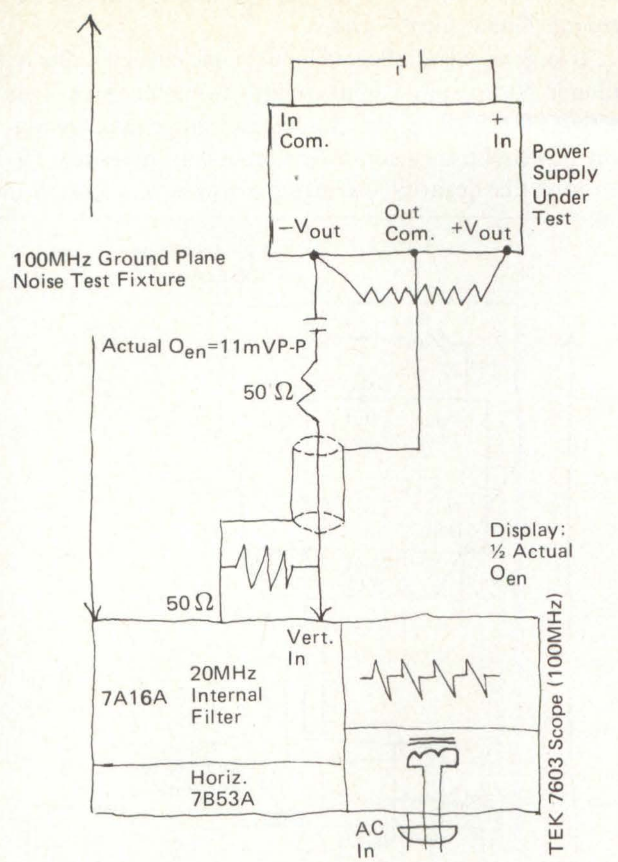
In one potential application of the packaging scheme, a complete small computer system can mount in one tabletop housing; using standard packaging techniques would require at least four separate cabinets. The unit's keyboard, mounted on a cover plate, rests on a special wedge-shaped frame that opens 180° relative to the next frame.

Multi-parameter readings of dc/dc converter noise

Measuring a dc/dc converter's noise output demands more care and skill than performing the same task for conventional line-operated power supplies. Indeed, the procedure for measuring the high-frequency components of a converter's switching spikes more closely resemble the techniques for dealing with high-frequency pulses or square waves.

One dc/dc-converter noise measurement will not suffice. To accurately evaluate a switching power supply, examine output-noise voltage, reflected input-ripple current and output "common mode" noise current, advises Frank Goodenough, product specialist at Teledyne Philbrick, Dedham, MA.

To obtain valid rms measurements of converter noise, utilize an rms-responding instrument with a bandwidth ranging



TEST CIRCUIT FOR OUTPUT NOISE VOLTAGE (Oen)

from at least 5 Hz to 10 or 20 MHz. Even if scaled to read rms values, no conventionally responding instrument can accommodate switching components or accurately measure non-sinusoidal components, Goodenough warns.

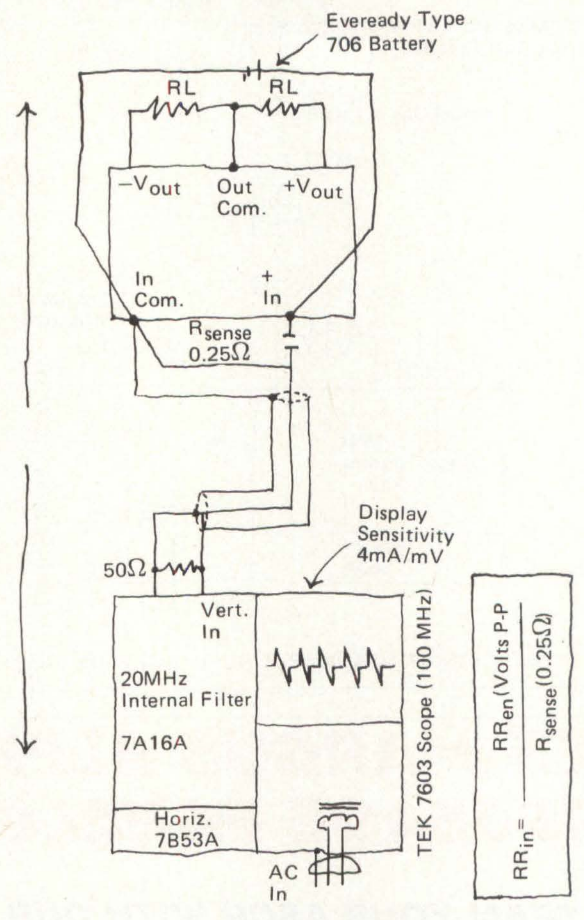
In most modern converters, switching frequencies range from a few to 100 kHz; input and output switching spikes usually vary in duration from 50 to a few hundred ns with amplitudes ranging from a few to several hundred mV. Thus, you'll need a test-system bandwidth of a least 20 MHz (with correct termination) to achieve a valid peak-to-peak measurement, the product specialist explains.

Before trying to measure wideband peak-to-peak noise, arrange a shielded ground-plane as close as possible to your oscilloscope's input connector and use nonreactive 50Ω terminations plus high-speed wiring. To minimize line-coupling and ground-loops, also use an isolated battery as the dc/dc converter's power source. Make noise measurements as close as possible to the converter/module's pins, Goodenough adds.

To prevent the oscilloscope from displaying ripple and ground-current pickup, unplug the power supply and create a short-circuit by connecting the power supply's output socket to the common output. When you take this precaution, the scope should display its own residual noise. In the unlikely event that this noise proves excessive, add a ground current or a pickup in series with the scope's input.

If you must trace a residual noise's source, remove the socket's short-circuit, plug in the power supply and shut off the input power source. Under these conditions, the presence of noise signals indicates a pickup between the power supply and the scope. To eliminate this interference, connect the oscilloscope's third pin – the case ground – to the earth ground, Goodenough advises.

If large enough, reflected input-ripple current – the unfiltered portion of an input circuit's switching spike – can activate flip-flops, gates, counters and other circuitry usually powered from a converter's input-voltage source. To measure this quantity – sometimes also termed spike-feed-



TEST CIRCUIT FOR
REFLECTED INPUT RIPPLE CURRENT (RR_{in})

back current – directly at the supply input terminals, use a dc-coupling capacitor (with adequate high-frequency characteristics) and a current-sampling nonreactive resistor. These components' time constant should prove no less than five, and preferably at least ten, times larger than the duration of the spike you wish to measure, Goodenough explains. To ensure that you've measured a switching spike in the linear circuit region, cross-check the current-sampling by using a current probe or by setting an R-value above and below the specified value.

In reflected input-ripple current measurements, as in peak-to-peak measurements, set your troubleshooting system's bandwidth at about 20 MHz and specify the sampling resistor's value, he adds.

A converter's common-mode noise current usually occurs at the isolated output, common terminal. The magnitude of this differential noise-current spike partially reflects the quality of a dc/dc converter's design and shielding techniques, Goodenough says. If large enough, a spike current can saturate a differential op amp or instrumentation amplifier powered by the converter supply.

OCR system, wand speed processing of bank data

At the Burlington Savings Bank in Burlington, VT, an OCR system processes monthly loan payments by scanning account numbers and amount fields. The operator uses a hand-held wand to read the information into the M3 system, marketed by Key Tronic Corp. The OCR system interfaces with a 3277 Genesis CRT that is plug compatible with an IBM 3271 control unit. The control unit connects directly to the central processing unit.

Classified as a low-volume OCR application user, Burlington Savings previously used randomly selected teller stations as the sources of batching, verification and entering payment data. No one specific individual processed the loan payments received through the mail.

Lyman W. Hill, the bank's group vice president, who had been searching for a viable data entry method for three years for this application, found that OCR performed the required functions effectively. However, he could not cost justify any of the systems he had looked at because of their high cost. After witnessing a demonstration of Key Tronic's low-cost hand held OCR system, Hill purchased the unit.

The M3 system needed no additional or new forms for successful implementation into bank operation. It did require, however, a relocation of the information scan band containing the account number and the amount, just below where the previous billing information was printed. The system now reads a 407 font generated by a 1403 IBM printer and suffers from no degraded print reading problems.

When the payment slip is returned to the bank with the remittance, the clerk checks to see whether the amount of the payment corresponds with the amount due. For those that do, the clerk tabulates the checks on adding machine tape to total the receipts. Then, the operator passes a wand over to read and optically enter the data at a rate of up to ten times faster than the previous method of manual key entry.

The system operates on-line, because the CRT holds 24 documents on the screen at one time. After the system has entered the 24 documents into the screen format, it sends the information to the central processing site. As a result of Burlington-written special software, these formatted pages of 24 documents can be recalled for manual editing, if necessary.

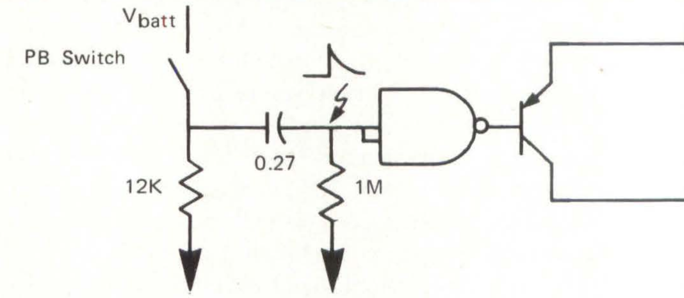
In this application, the system eliminates overtime costs and shifts the responsibility of processing these payments to one person who processes all payment slips in an average of three hours per day. A worker requires little or no previous experience to operate the M3. Mr. Hill said that a mail clerk handles the processing load easily during a normal workday.

Although the number of documents processed each day at Burlington vary, the first seven business working days of the month usually require processing approximately 1400 to 1600 documents. For the remainder of the month, approximately 400 documents per day are processed. According to Hill, the first four months of experience indicates that the M3 will pay for itself in the first twelve months of operation solely on the basis of eliminating operator overtime. He also foresees other applications for the OCR System within his savings bank.

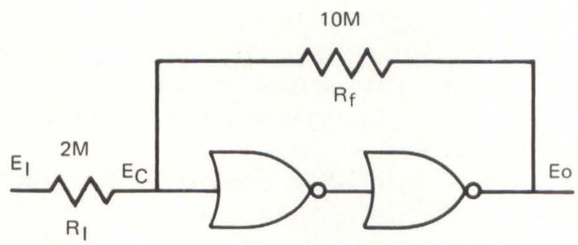
CMOS gates implement variable-length timer

Low cost and low current drain constituted the primary design constraints on a timer for a tv control system, a special-purpose unit configured by Herman Sheffield, president of Data Engineering Associates, Houston. To meet these constraints, he chose to use CMOS gates, which, he points out, suit a variety of battery powered, non-logic applications because of their low cost, wide supply voltage range and high input impedance.

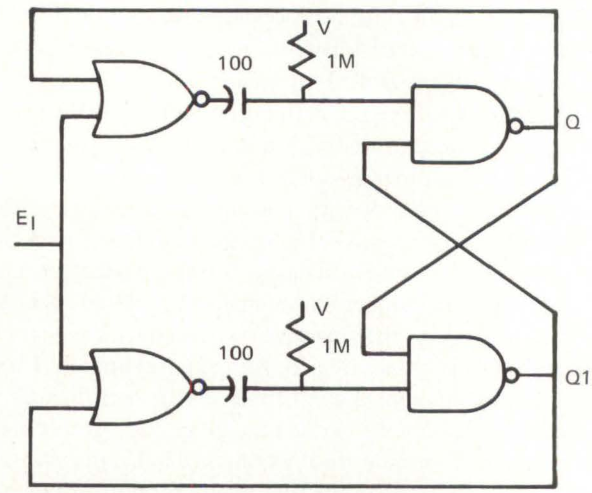
To implement the variable-length timer, Sheffield used the 4011AE quad 2-input NAND, which, with its companion 4001AE quad 2-input NOR, costs about \$0.32 – eight



45-MINUTE, LOW-CURRENT TIMER



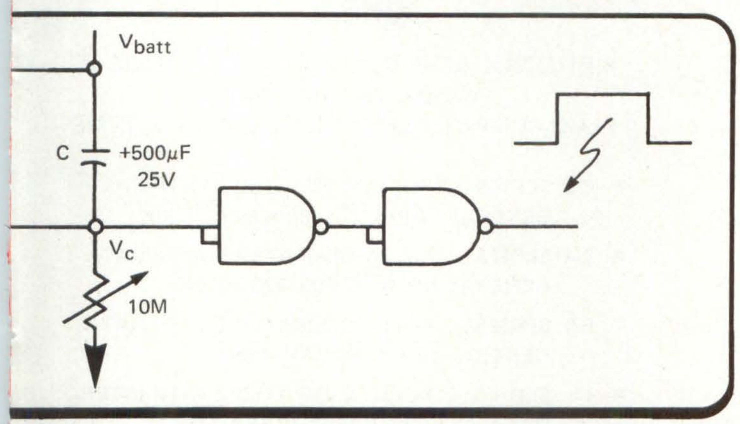
SCHMIDT TRIGGER



TOGGLE FLIP FLOP

cents per gate. The timer, which could operate from a 9V battery, times out in about 45 min., and its current drain is negligible in most applications, he claims. The final gate provides wave squaring and would be unused in many applications.

Because many inexpensive capacitors exhibited leakage currents too high for the circuit, Sheffield chose a 25V unit. High leakage current means that V_c won't go to the low rail (shown as ground). That is, with the capacitor completely discharged, the circuit behaves like a capacitor leakage resistance, R_c, in series with R_t; if the leakage is too high, R_c supplies enough current to raise V_c from ground.



To avoid this problem, he says, make the leakage current – $(V_{batt} - V_c)/R_c$ – small compared with V_c/R_t. That way, when the transistor pulls V_c to V_{batt}, the initial voltage across C measures 0 and remains smaller than the voltage across R_t.

Sheffield also configured two other circuits that incorporate CMOS gates. The first, a Schmidt trigger, incorporates the 4001AE and produces clean outputs from slow-moving inputs; it could find uses in consumer devices or in other circuitry with spare unused gates. As a general rule, make R_f at least twice as large as R_I so that if E_0 is high and E_I goes low, E_c will drop below the CMOS threshold (normally 0.5 times the supply voltage but possibly as low as 0.3 times that value).

In the second circuit, a toggle flip flop, outputs Q and Q1 alternate high and low each time E_I crosses the input threshold going high. The circuit, which uses both the 4001AE and the 4011AE, behaves the same whether Q goes high or low, in contrast with CMOS flip flops like the 4013, in which Q switches high on a slow-moving input but requires a relatively sharp input to switch low. Thus the circuit could suit some CMOS applications better than the 4013 – for example, because it doesn't respond to extremely slow inputs, you could use it to discriminate against such signals.

If you require a response to dc waveforms, use the Schmidt trigger's output as the toggle flip flop's input, advises Sheffield. And if you require a flip flop that changes on low-going signals, interchange the positions of the NOR and NAND gates in the toggle flip flop and connect its resistors to ground instead of V, he concludes.

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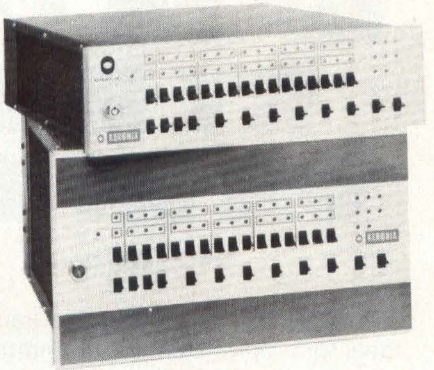

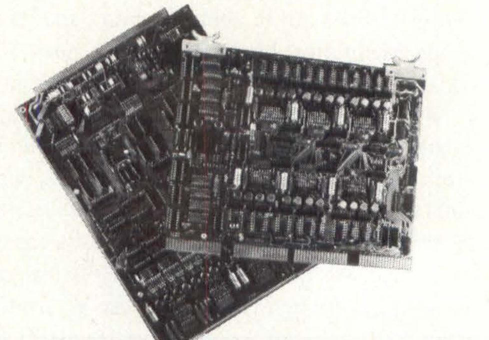

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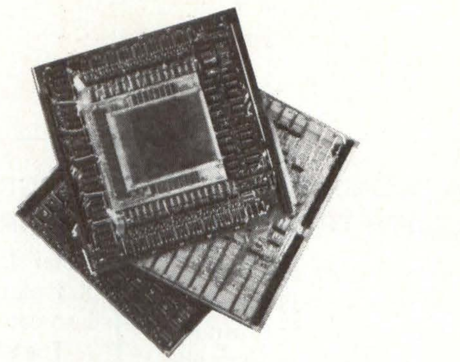

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- 1046 DISK CONTROLLER
- 1146 FLEXIBLE DISK CONTROLLER
- 1054 EXTENDER BOARDS
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CIRCLE 72

product news

80-MBYTE DISK DRIVE SWAPS WITH TRIDENTS

The 80-Mbyte BD-80 is an IBM-3330 type (short stack version) disk drive and can interface with the manufacturer's 3300 formatter, a standalone, IBM-3330 compatible disk controller. It supports sophisticated file-management techniques in real time and serves multi-terminal and batch processing systems requiring high-speed, randomly accessible

mass storage. The basic BD-80 contains dynamic braking, standard digital I/O and an ac power cable and power supply. Standard logic features include write protection, address mark detection, variable sector sizes and sector address and cylinder status. With the standard I/O, the BD-80 is directly interchangeable with Trident-class drives. An optional differential I/O interface for SMD-class drives is also available. The disk pack is based on IBM 3336-11 components; equivalent packs are generally available and have been qualified by the manufacturer. It contains five read/write surfaces with 815 cylinders/surface at 370 tpi. Recording densities are 6060 bpi, 20,160 bytes/track. Start and stop times measure 20 sec, and average access time equals 30 ms. Ball Computer Products, 860 E. Arques Ave., Sunnyvale, CA 94086 (408) 733-6700 **Circle 241**

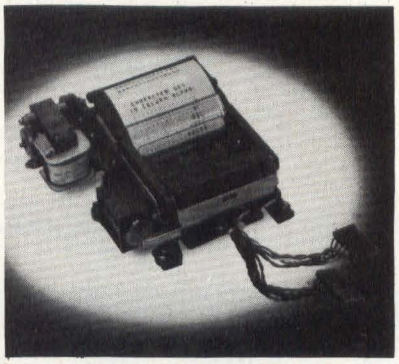
PROGRAMMABLE FOUR-COLOR PLOTTING

Poster size brochure describes 9872A X/Y plotter that changes pens automatically under program control.

The 9872 is a microprocessor-based A3-sized plotter that works with HP's 9825 and 9831 desktop computers. It features addressable moves as small as 0.025 mm, selectable pen speed, point digitizing, window plotting, five resident character sets, off-scale handling, symbol mode plotting, dashed-line fonts and axes generation. Hewlett-Packard Company, 1501 Page Mill Road, Palo Alto, CA 94304. **Circle 281**

15-COL. IMPACT PRINTERS USE 54-CHAR. SET

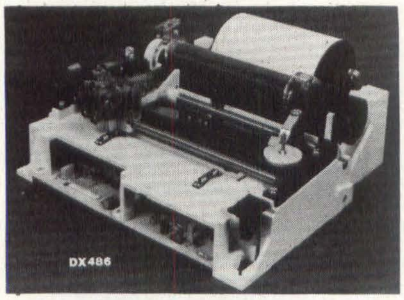
These 15-column impact printers with full alphanumeric capability can output up to 3 lps for numeric data and 1.5 lps for alphanumeric data. The Series PR1500 units offer a full 54-character set and multi-copy printing capabilities and start in 500ms with subsequent line feed of up to 10 lps. They use standard paper and a snap-in 2-color ribbon cartridge. Power consumption measures 11W. Options include special drum type



fonts, 50 Hz operation, vertical mounting, either single or multiline printing, ticket printing, combination ticket/tape printing and special voltages. Sheldon-Sodeco, 4 Westchester Plaza, Elmsford, NY 10523. (914) 592-4400 **Circle 250**

40-COL. PRINTER USES ONE 12-V SUPPLY

Type DX486 dot matrix printer produces up to 40 columns of alphanumeric or graphic information for such applications as data processing terminals, communications, instrumentation, ticket printing and point-of-sale terminals. It uses one 12 Vdc supply and measures 4"H. The unit produces 40 characters in 4" on paper 4½" wide, using standard paper and a reversible ribbon. Two additional copies can be made using self-acting paper or carbon. To accommodate graphics printing, paper advance is designed to allow the continuous printing of dots, one under the other. All controls occur through 5V TTL levels on one connector. Amperex



Electronic Corp., Hicksville Div., Hicksville, NY 11802. (516) 931-6200 **Circle 251**

DRIVES AND STEPPERS FOR FLOPPIES

These drive motors and stepping motors suit floppy-disk drive applications. A 1/100-hp ac drive motor has output speeds of 1500 rpm @ 50 Hz or 1800 rpm @ 60 Hz and is a permanent-split-capacitor reluctance synchronous unit with automatic reset thermal overload protector. Size 18 and 20 stepping motors have single or multiple start lead screws and come in 3- or 4-phase versions with 15° step angle. Eastern Air Devices, Holtzer-Cabot Motors, Dover, NH 03820. (603) 742-3330 **Circle 253**

product news

HIGH SPEED DEFLECTION AMPLIFIER

Display Components, Inc., of Littleton, Mass., has developed an ultra-linear deflection system which provides a 3 HMz bandwidth while conserving power. Designed to operate in a Class A mode, with a push-pull deflection coil, it draws constant current from the power supply only slightly greater than the deflection coil's sensitivity.

Beam deflection is achieved through proportional splitting of the current between the positive and negative half-axes of the deflection coil. In this manner, the difference in current is always proportional to the sine of the deflection angle. This constant current, differential drive mode delivers a high order of stability and low noise. Also, sampling of the deflection currents at the output of the coil windings, providing negative feedback to the input, guarantees linearity.

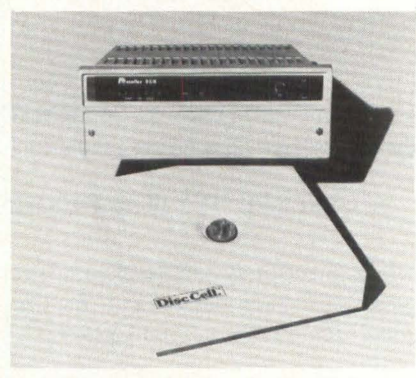
All deflection is accomplished in one major-axis system. High frequency small signal inputs, such as characters and symbols, are entered at the same amplifier input as are the large signals, such as major positioning, vector and raster. Thus, functional simplicity and accuracy are achieved with high frequency signals processed by the same feedback amplifiers and driven through the same deflection windings as are the larger signals.

Labelled the DA3000, it is designed to meet today's needs in alphanumeric/vector type display systems requiring fast major positioning, wide bandwidth, low power consumption and low cost.

Optional features include 945 TV-voltage boost capability, with no increase in power, to attain a fly-back recovery of 7 μ sec to 1%. This feature operates automatically with no external keying or additional power supplies. The power required is approximately 40% of that used in a brute force system. Display Components, Inc., 550 Newtown Rd., Box 488, Littleton, MA 01460. **Circle 282**

FIXED-HEAD DISK DRIVES USE REMOVABLE MEDIA

Head-per-track disk drives, designated Model 980 Series, come with storage capacities ranging from 0.5 to 2.0 Mbytes, with larger capacities achievable by daisy-chaining. All units utilize a proprietary, head-per-track disk



cartridge, termed Disc Cell, which has a self-contained spindle and Winchester-type media and read/write head assemblies. The drives also offer integral dc power supplies constant data rate and access time regardless of power source and 10,000 hrs MTBF. Price: $3900 to $61,000. Dataflux Corp., 1195 E. Arques Ave., Sunnyvale, CA 94086. (408) 723-7070 **Circle 243**

CIRCLE 74▶

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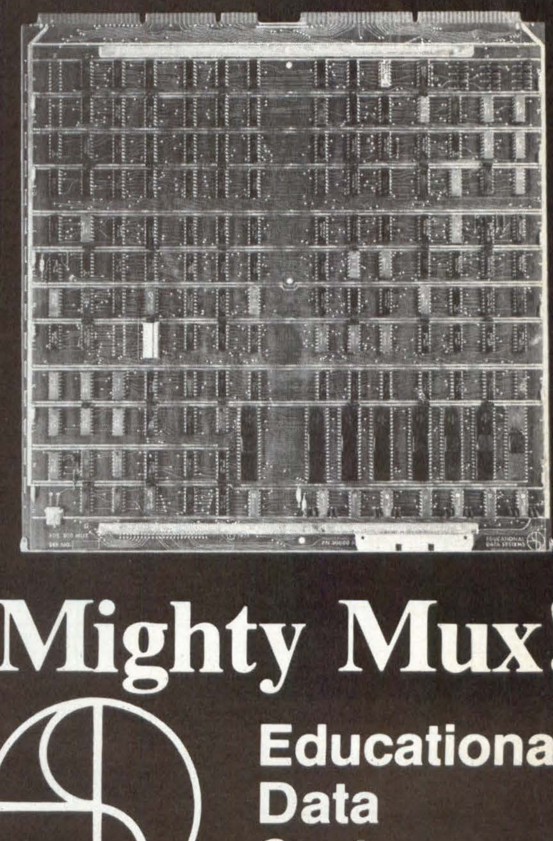


- Why use 4 boards in your Nova-type* mini (master terminal interface, line printer controller, card reader controller, and four port mux) when Mighty Mux does it all with one board?
- Why add a board for each 4 ports when Mighty Mux gives 24 async ports or 8 sync ports per expansion board?
- Why use the PIO bus when Mighty Mux will interface all your devices via the DMA channel, reducing CPU overhead to almost zero?
- Why use more chassis space, power, and dollars when Mighty Mux does more for less?

*"Nova" is a registered trademark of Data General Corp.

Mighty Mux!

Educational Data Systems

Mighty Mux

DESCRIPTION

Mighty Mux is a complete I/O Communications System for any NOVA-type computer. It interfaces from 4 to 128 peripheral devices to the computer via the Direct Memory Access (DMA) channel. By using the DMA channel instead of the Programmed I/O bus, I/O processing overhead on the CPU can be reduced from 60% or 80% to 1% or 2%.

The low I/O overhead and provision of extra control lines on each port make it possible to interface and control printing terminals, CRT's, graphics terminals, modems, even floppy discs, line printers and card readers equipped with RS-232-C interfaces.

A master terminal interface, real time clock, and modem controls on each port are standard features which eliminate separate boards required in competitive multiplexers.

ASYNCHRONOUS COMMUNICATION

One board (the 310) provides asynchronous communication to four or eight local or remote devices at speeds up to 50K baud. Port 0 of the 310 serves both as the master terminal interface and as a time shared port. All interfaces are RS-232-C, current loop, or both. All DC power is normally obtained from the host computer; however, independent supplies for ± 12V and for current loop operation are available.

The 301 board permits expansion to 16, 24, or 32 asynchronous ports. Thus, a thirty-two port multiplexer, including real-time clock, master terminal interface, and all necessary modem controls is implemented by two boards. Each additional 301 adds up to 24 ports to a maximum of 128 ports.

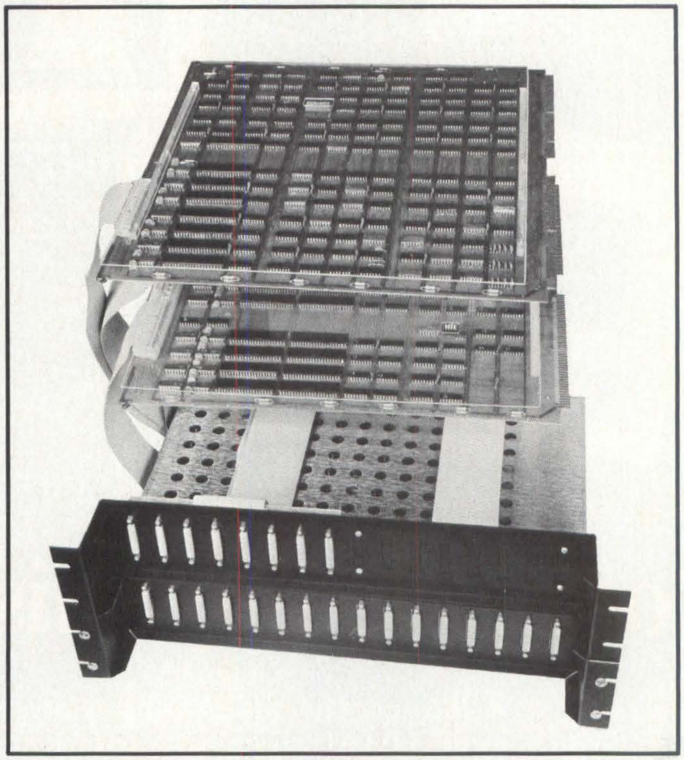
SYNCHRONOUS COMMUNICATION

The 302 board adds synchronous communication at speeds up to 50K baud over the same DMA channel interface. The 302 provides 2, 4, 6 or 8 channels and performs Cyclic Redundancy Check (CRC) generation and checking in hardware. It fully complies with the new national standard (ADCCP) and the new IBM standard (SDLC) for synchronous communication.

PROGRAMMING FLEXIBILITY

All important parameters are under program control on a port-by-port basis. For instance, each port is assigned its own input and output buffers in core. These may be of any size and any location in core. The program also controls parity mode, character size, automatic echo, and baud rate for each port. A user can sign onto the system at one baud rate and switch to any other standard baud rate from his terminal.

Drivers are available to use the EDS-8 under IRIS, RDOS, and RTOS and to interface printers, card readers, and modems through the multiplexer.



THREE IMPLEMENTATIONS OF A 32-PORT MUX

OUR WAY	THEIR WAY*-4060	THEIR WAY-DCU/50*
1. One 310-A8 board One 301-A24 board The 310-A8 includes real time clock and master terminal interfaces	1. Eight 4060 boards One 4007/4010 board for real time clock and master terminal interface	1. One DCU-50 board One Comm. Chassis Two ALM-16 boards Eight 4261's; One 4007/4010 board
2. Modem control-included above	2. Two 4026 boards for modem control	2. Use four ALM-8's instead of two ALM-16's if modem control needed
3. Requires two slots, no external chassis	3. Requires 11 slots (& probably an expansion chassis)	3. Requires two slots and an external chassis
4. Operates on the DMA channel (1 interrupt/transmission)	4. Operates on PIO channel (1 interrupt/character)	4. DMA between CPU & DCU-50; PIO between DCU-50 & peripherals
5. Easily handles 32 terminals at 9600 baud each	5. Bogs down with 3 terminals at 9600 baud	5. Programmable, but complex programs limit data rate
6. Baud rates under program control	6. Baud rates hard wired	6. Baud rate under program control
7. Approximate price: $6400	7. Approximate price: $15,000	7. Approximate price: $10,000
8. Warranty: one year	8. Warranty: 60 days	8. Warranty: 60 days

*Using standard Data General equipment.

Educational Data Systems

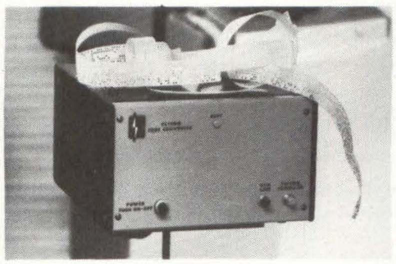
1682 Langley Avenue, Irvine, California 92714, 714 / 556-4242

CIRCLE 75

product news

BCD-TO-ASCII CONVERTER LINKS INSTRUMENTS, TTYS

The CC 1200 code converter accepts 10 digits of parallel BCD data from any digital instrument and transmits the reading in serial ASCII to teletypewriters, CRT terminals, tape recorders, computers or other data



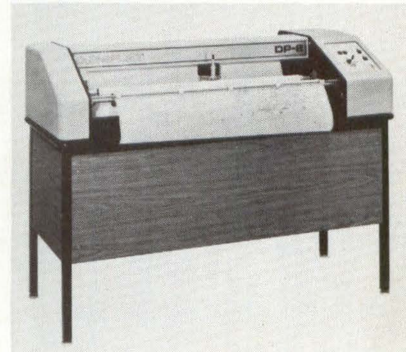
equipment. It suits such data logging applications as laboratory research, production testing and communications traffic monitoring. Data inputs are TTL/DTL compatible, buffered for up to 80-V logic (either negative or positive-true). When you press the Log Command button the code converter strobes the input data into memory and sends it out in serial ASCII. An isolated 20mA loop output is standard with selectable even or odd parity. After seven loggings, the device automatically generates a carriage return, line feed and rubout. Price: $972 ($100 discount in effect until June 30). Nationwide Electronic Systems, 1536 Brandy Parkway, Streamwood, IL 60103. (312) 289-8820 **Circle 247**

DC SERVO MOTOR FOR PRINT WHEEL DRIVES

This dc servo motor can accelerate a matched inertia at 30,000 rad/sec^2. It produces 22.5 ox-in at 58 W (25°C) and has an armature inertia of 0.00036 in-ox-sec^2. Its electrical time constant equals 0.5 ms, and it measures 1.375" in dia and 1.7" long. Typical applications include matrix printer carriage drives, paper advances in computer peripheral equipment and print wheel drives. Magnetic Technology, 21001 Kittridge St., Canoga Park, CA 91303. (213) 887-7700 **Circle 252**

QUIET 36" PLOTTER DRAWS AT 4.5 IPS

Dubbed "the Quiet One," the DP-8S3 36" plotter outputs drawings on-line, off-line, on timeshare or with remote-batch graphics. For con-



tour mapping, subdivision plots and PC-board design, the unit comes with 3 pens and has 9 switch-selectable step sizes ranging from 0.00125" to 0.01", positive paper feed and a 4.5-ips plotting speed. It also accommodates 12" paper for A- and B-size drawings. Price: $9500. Houston Instrument, One Houston Square, 8500 Cameron Rd., Austin, TX 78753. (512) 837-2820 **Circle 249**

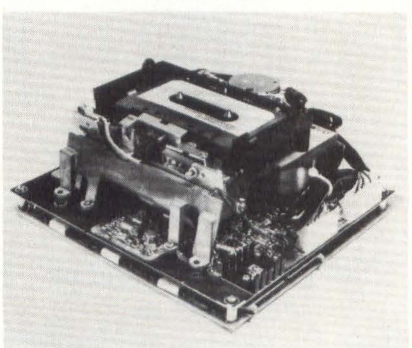
product news

INTERFACE MODULE LINKS GPIB AND CAMAC

Model 3388 GPIB Interface, part of the manufacturer's line of Camac modules, is a double-width module that provides the interface between a Camac system (IEEE Standard 583) and the general-purpose interface bus (IEEE Standard 488). It can connect up to 14 digital multimeters, counters, printers, calculators, display terminals or other devices that meet the GPIB standard to a Camac system via standard GPIB cables. The module functions as a controller, talker and listener as described in IEEE Standard 488. Model 3388 comes with the 24-contact connector specified by IEEE 488 (Model 3388A) or with the 25-contact connector specified in Europe by the International Electrotechnical Commission (Model 3388E). Price (domestic): $850 (quantity 1-9). KineticSystems Corp., 11 Maryknoll Dr., Lockport, IL 60441. (815) 838-0005 **Circle 242**

CASSETTE RECORDER OUTPUTS 125 CPS

The STR-150 digital cassette recorder comes with complete interface electronics and requires eight data-in

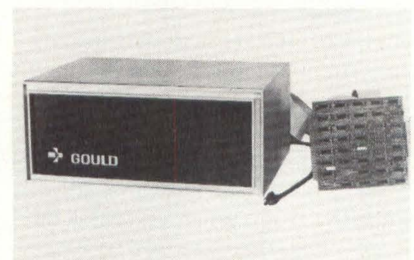


lines with strobe, eight data-out lines with strobe and separate line for rewind. All lines are DTL/TTL compatible, and no external clocking is required. The recorder accepts asynchronous 8-bit parallel inputs at rates up to 125 cps and outputs data at the same rate. It requires ±12V dc and +5Vdc power supplies and measures 8" x 8" x 3.8". The unit also comes with power supplies and enclosure for stand-alone or portable applications. Price: $503 in singles, $376 in 100s. Electronic Processors, Inc., 1265 W. Dartmouth Ave., Englewood, CO 80110. (303) 761-8540 **Circle 245**

HIGH-SPEED CAPABILITY FOR REMOTE ALPHA-NUMERIC DISPLAY

Gould, Inc., Instrument Systems Division, has developed a remote graphics processor (RGP) that gives remote terminals the capability of generating high-speed graphic hardcopy when coupled with its 5000 Series electrostatic printer/plotter.

With the RGP unit and a 5000 or 5005 printer/plotter, charts, graphs and engineering drawings can be printed at paper speeds averaging ½ inch/second when the serial data rate is 9600 Hz. Instantaneous paper speed varies from 0.14 to 1.0 inch/second, depending on the plotter model, the baud rate at which data is received and the complexity of the plot.



Using Gould's proprietary PLOT graphics software and RGP option software on the host computer, input data is processed and transmitted over the communication line in a highly encoded character form. The RGP data can, therefore, be handled by standard host computer spooling software without modification. Using an RS-232C interface connection to the terminal, the RGP processes the transmitted graphic data and sends raster data to the Gould plotter.

Software is available for host computers of the following types: IBM 360/370, Univac 1100 Series, and Control Data 6000, 7000, or Cyber 70 Series. An optional hardware character generator is available to provide alphanumeric printer/plotter output for most terminal configurations using ASCII format. The microprocessor based RGP is supplied with an enclosed cabinet. An option is available for 19-inch rack mounting. Gould, Inc., Instrument Systems Division, 3631 Perkins Avenue, Cleveland, Ohio 44114. **Circle 283**

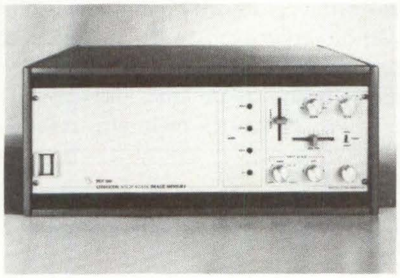
FLOPPY-DISK DRIVE SWITCH-SELECTS 6 MODES

This multifunctional floppy disk drive has a six-position switch that can select hard or soft sectoring, gating of "write protect" or "ready" with select, stepping motor power control, and separation of data and clock. The 142M performs as a single density (243K bytes) or double density drive (650K bytes) with no requirements for additional control logic. A 6400-bpi, 48-tpi unit with 6-ms track-to-track access time, it transfers 500,000 bps. Price: $625 in singles, with OEM discounts available. Calcomp, 2411 W. La Palma Ave., Anaheim, CA 92801. (714) 821-2541 **Circle 248**

IMAGE MEMORY/SCAN CONVERTER

The PEP-500 Lithocon Solid State Image Memory/Scan Converter for electronic image storage and manipulation is a beam addressed solid state image memory designed for widespread commercial application for visual display of electronic signals from any source such as medical ultrasound waves, industrial and medical x-ray, oscillographic wave forms, computer graphics, medical nuclear scanners, infrared imaging systems or even image signals from outer space.

Featuring a high image gray scale resolution coupled with high image stability, operating specifications are guaranteed regardless of extremes in



operating temperature, vibration or magnetic ambience.

The single-ended scan converter is operable in any of four modes: read, write, selective erase and full screen clear. The beam address of the Lithocon TX-100 solid state target can be driven either by internal raster generators of the PEP-500 or external X, Y signals. Image writing may be accomplished in either integration or equilibrium modes. Princeton Electronic Products, Inc., P.O. Box 101, North Brunswick, NJ 08902. **Circle 284**

12-DIGIT DISPLAY BOARD

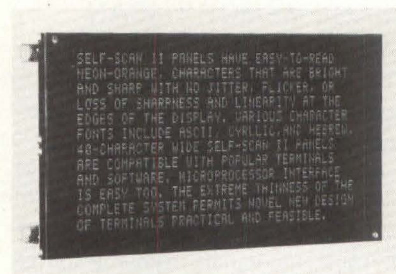
Texas Instruments has introduced a multi-digit visual light-emitting diode (VLED) display stick with 12 digits, claimed as the largest number available on a single board in the industry today. The TIL804 characters are seven segment red VLEDs, 0.27 in. high and feature typical brightness of 500ucd at 20mA. Features include right hand decimals at each digit, continuous uniform brightness of segments within each digit and a wide viewing angle for distances up to 15 ft. It is available now in common cathode configuration for ease in multiplex operation on rugged, one-piece printed circuit board construction. Applications include Citizens Band radios, scanners, digital instrumentation, electronic games, medical electronics, test and measurement equipment and desk top calculators. Prices are $14.65 each in quantities up to 100 and $11.65 each in quantities of 100 to 999. Texas Instruments Inc., P.O. Box 5012, M/S 308 (Attn: TIL804) Dallas, TX 75222. **Circle 296**

product news

LARGE SCREEN DATA DISPLAYS

A 480 character alphanumeric panel display, offered at prices comparable with CRT displays, requires lower voltages than CRTs and can be packaged as a complete display sub-system in an ultra-thin design (less than 2" in depth). The display provides improved character readability with no focusing or linearity problems and can be directly interfaced with digitally addressed microprocessor-based systems. Neon orange in color with a high contrast dark background, characters are arranged in a 5 x 7 dot matrix, each measuring 0.26 inch high x 0.14 inch wide to provide uniformity, intensity and high visibility without edge distortion. Characters can be viewed for extended periods in daylight or at night with low reading fatigue. The matrix maintains stable, low glare fixed characters not influenced by voltage changes or external disturbances. With 480 characters, 12 lines of 40 characters each, the display panel area is a compact 11 inches long x six wide. It is 1-1/4" deep, including drive electronics.

Each display is supplied complete with a panel driver board. The driver board includes all electronics necessary to digitally address the full panel including drivers, shift registers, latches, blanking, dimming and signal/component detection failure. The driver board is designed to present a minimum interface to its host controller or system. For example, only 5 interface signal input leads are essentially required. Interconnection to the driver board is through a 26 pin connector. Voltage input re-



quirements are +5V, -12V as well as a -250V low current supply which can readily be obtained from a low cost DC to DC converter.

Prototypes are now available at $480 each with production prices at the 100 quantity level of $315 each.

All 64 ASCII characters can be displayed as well as over 100 different characters and symbolic fonts including Cyrillic, Hebrew and Katakana plus special characters such as math symbols, fractions and geometric symbols. Burroughs Corporation Electronic Components Division, P.O. Box 1226, Plainfield, NJ 07061. **Circle 292**

DIGITAL PANEL METER READABLE AT 40 FEET

A 3½-digit panel meter incorporating 0.8-inch (2.03-cm) LEDs permits easy visibility at up to 40 feet, suiting it for any application where read-out distances are greater than those typically encountered in bench-top applications.

"The range of applications for these devices is quite wide," said Dom Norcia, Fairchild marketing manager for instruments. "Since these DPMs convert an analog signal to a digital display, they are perfect for control and monitoring applications on the factory floor, at a utility, or for use in a wide range of

CIRCLE 77

medical instrumentation."

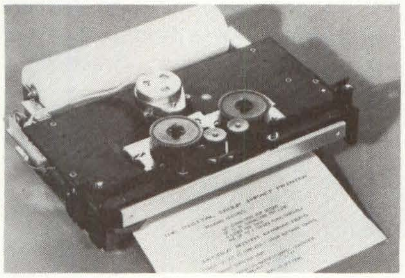
Models are available with either a 15-pin dual row connector or 8-pin terminal block. The 15-pin connector offers greater applications flexibility. Features such as bit serial, decimal point selection and external hold are available from terminals provided at the connector. The 8-pin terminal block is a simpler, more efficient termination method for applications that do not require external access to all the features available with the 15-pin connector.

BCD (Binary Coded Decimal) bit serial outputs capable of driving one TTL load are standard; BCD bit parallel is available as an option on a separate PC board which can be added in the factory or field. Characteristics of this feature include a grounded configuration, non-floating input, four TTL signals and a read-ready signal. All data bits are latched and a sign is included in the data transfer (sign is valid into overrange). Designated Model 80, it is also equipped to drive external circuitry – 25mA of 5VDC and 15mA of -8VDC.

The panel housing is 3.580 inches (91 mm) by 1.645 inches (41.8 mm) permitting installation in either the proposed NEMA domestic cutout or in DIN cutouts. Instrumentation Unit, Fairchild Camera and Instrument Corporation, 1725 Technology Dr., San Jose. CA 95110. **Circle 295**

96-COL IMPACT PRINTER COMES IN $495 KIT

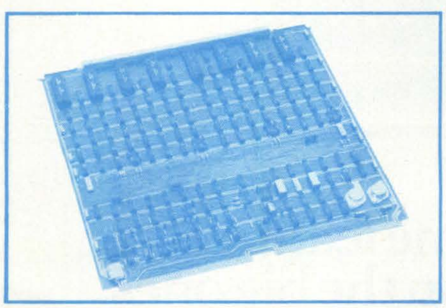
This full-size, kit-built, impact printer outputs 120 cps, 96 characters/line.



Character spacing measures 12 to the inch, and line spacing equals six to the inch. The unit prints up to four copies simultaneously, and character set and pitch are variable under software control, allowing for double-width characters and varying-width characters within the same line. The printer has a 5" x 7" character matrix, and its ribbon has built-in re-inkers for a life of 10,000,000 characters. Paper can be either a standard 8½" roll, fanfold or cut page, and the unit interfaces to 8-bit parallel ports. Price: from $495. Digital Group, P.O. Box 6528, Denver, CO 80206. (303) 777-7133 **Circle 246**

MULTI-CONTROLLER BOARD INTERFACES D.G. MINIS

Slot Saver, a multi-controller interface board for Data General Nova and Eclipse computers, measures 15" square and contains interface controllers for low-speed peripherals devices commonly used with minicomputers. A maximum configuration consists of controllers for two CRTs or TTYs, a real-time clock, a paper-tape punch and a line printer. The system is compatible with the instruction sets and operating systems software supplied by Data General for each specific peripheral device. Price varies with number of controllers and quantity of boards. Custom Systems, Inc., 2415 Annapolis La., Minneapolis, MN 55441. (612) 553-1112 **Circle 244**



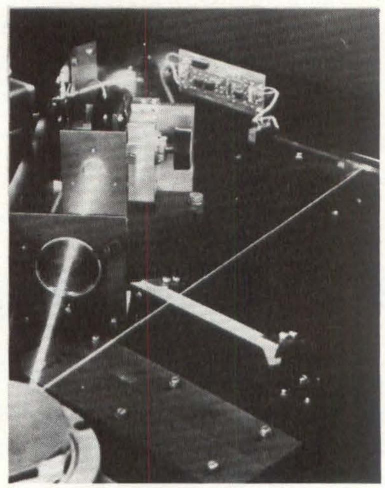
product news

PRINTERS: FROM IMPACT TO LASER

up to 10 times the performance of conventional printers

Although electromechanical printers provide sterling service at printing speeds of 1,000 to 2,000 lines/min, they can be too slow for fast data processing and storage systems now available. Mechanical considerations restrict further increase in their printing speed. The two main sections of this printer are the character generator and the electrophotographic system for printing on normal single-part printer paper. In the character generator, a laser projects coherent light onto an acousto-optical beam deflector in which very high frequency ultrasonic waves produce pressure variations that act as a diffraction grating for the coherent light. If the ultrasonic frequencies are now varied by means of a control electronics driven by the CPU, the angle of deflection of the laser beam behind the diffraction grating changes in such a way that the beam fans out in the vertical axis. This light fan is moved in the horizontal axis by a polygon mirror and then falls on the rotating photoconductor drum.

Characters thus generated and still to be printed are transferred onto single-part printer paper by means of electrophotography. The photoconductor surface is charged electrically prior to exposure. The surface of the drum is then discharged at those points which are struck by the light beam; charged toner powder is then applied to the drum and adheres electrostatically to the exposed points. After transfer of the powder particles to the synchronously running



Siemens used laser beams and electrophotography to attain printing speeds of up to 1.2 million lines per hour, or around 70,000 characters per second – roughly ten times the performance of impact printers.

paper, the toner is fused into the paper by means of heat and pressure.

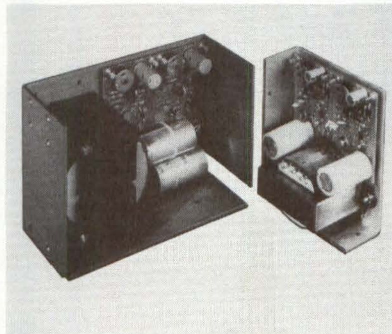
Parallel to data output via the laser beam, an overlay image, e.g. a form blank, may be overprinted enabling unprinted paper to be used. The finished printed paper is stacked by a powered forms stacker integrated in the printer. Various commercially available forms handling machines can be attached to this stacker. These devices facilitate bursting of forms, programmed stacking or sorting by various criteria.

Use of this laser printer, Siemens says, has a number of advantages. The specified printing rate – up to

220 DIN A4 forms per minute – is independent of the character set and line spacing. Besides various fonts and font sizes, finished graphic representations can be printed, thus dispensing with the need for preprinted form paper. Small fonts make for further paper savings. The print quality in general is better, reliable and higher. Finally, Siemens claims that its laser printer provides a further contribution to environmental protection: the operating noise level has been reduced to below 60 decibels. Siemens AG, Postfach 3240, D-8520 Erlangen 2, Federal Republic of Germany. **Circle 262**

DUAL OUTPUT DC SUPPLIES FOR MICROPROCESSORS

A complete series of dual output power supplies for microprocessors and op-amps has primary ac input capabilities to operate over a range of 115/230 V ±10%, 47-63 Hz at a temperature up to 50°C ambient with no derating required for 47-63 Hz operation. Calculated MTBF using MIL-HDBK-217A guide lines is over 60,000 hours. Warranty is 2 years. DAPS Units are constructed on an open aluminum chassis; mounting may be accomplished in various orientations with optional fasteners available. Overvoltage protection is available with either one OVP on each output or a single one to protect both outputs. Electrostatically shielded transformers provide lower high frequency noise experience. All units are regulated by hermetically sealed integrated circuit regulators in metal enclosures and all transistors



used are hermetically sealed TO 3 can types. Regulation is ±0.05% for line; ±0.1% for load. Ripple is 1 mV RMS; (3mV peak to peak maximum). Adtech Power, Inc., 1621 S. Sinclair St., Anaheim, CA 92806. **Circle 263**

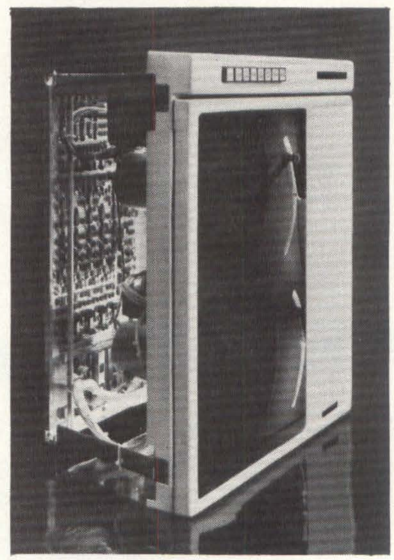
TRIPLE-OUTPUT POWER SUPPLY FOR MICROPROCESSORS

Triple-output power supply from Hewlett-Packard is designed to power OEM microprocessor systems that need independently adjustable and isolated voltages. The HP 62312D supply simultaneously provides three outputs with a wide latitude of voltage combinations. Main output is rated at 4.75V to 5.25V at 3A; the other two each range from 4.75V at 0.38A to 12.6V at 0.6A. Output effects for source and load are listed as 0.1 percent respectively. Periodic and random deviation is 1mV rms, 3mV p-p; 20 Hz to 20MHz. Input voltage taps can be changed by the user to cover the range of 104VAC to 127VAC or 208VAC to 250VAC at 48 to 63Hz. Protection features include an internal AC fuse, fixed foldback current limit and standard overvoltage protection on the main 5V output (optional on the other two outputs). Price: $116 each in quantities of 100. Hewlett-Packard Co., 1501 Page Mill Rd., Palo Alto, CA 94304. **Circle 256**

product news

SYNCHRONOUS TAPE DRIVE

The microprocessor-based TDI 1050 Transport from Tandberg Data uses two 10½-inch reels and features an optional internal formatter. With an interface of industry-wide compatibility, the TDI 1050 reads and writes data at densities of 1600 cpi phase-encoded or 800, 556, and 200 cpi NRZI at speeds of 12.5 to 45 ips, with a rewind speed of 200 ips average, on either 7 or 9 tracks. The internal formatter permits users to daisy-chain up to four transports. ANSI and IBM compatibility is provided for any mode. Tandberg Data, Inc., 4901 Morena Blvd., Suite 407, San Diego, CA 92117. (714) 270-3990. **Circle 270**



OEM PRINTER

A non-impact printer now available in APL for OEM applications features dual-font printing capability, offering selectability to either of two character sets – APL or ASCII (upper/lower case). With full APL and ASCII character sets, 188 printable characters are available. Operating at speeds up to 30 cps, the Q-3 prints 80 characters per line in a 5 x 7 dot matrix, with automatic carriage return and line field at 81st column. Price: less than $890 in OEM quantities of 25 units or more. Computer Devices, Inc., 21 North Ave., PO Box 421, Burlington, MA 01803.
Circle 259

SWITCHABLE INTERFACE OPTION FOR 2480 CRT TERMINALS

Ann Arbor Model 2480 Terminals are now available with a Switchable Interface option which provides for external switch-selection of either an RS232 or 20MA current-loop interface. The terminal displays 24 lines x 80 characters alphanumerics. Characters are 64-character ASCII displayed in a 5 x 7 dot matrix. The KSR-version features a detachable TTY-style keyboard, including separate numeric and cursor control pads. Three general function keys are provided that may be labeled and encoded to perform user-specific functions. Only one of the interfaces is enabled at any time, depending on the setting of the switch. If the RS232 interface is selected, the input and output current loops are maintained through the AUX1 connector, but the terminal will not accept data from or send data on the current loops. If the 20MA interface is selected, the RS232 outputs RTS and DTR remain at Space, but the Data output is held at Mark and the Data input is ignored. Three case options are available to allow maximum flexibility in tailoring the configuration to the user's application. They include (1) Design III desktop case including a 14-inch monitor and detachable keyboard, (2) Series 200 modular case (controller only) for use with free-standing monitors and keyboards, and (3) R-case (controller only) for rack mounting in a standard 19-inch rack. Single

quantity prices range from $1130 for the controller to $1780 for the complete terminal. OEM and quantity discounts available. For further information contact: Ann Arbor Terminals, Inc., 6107 Jackson Rd., Ann Arbor, MI 48103. **Circle 264**

DOT-MATRIX IMPACT TABLE PRINTER

Presenting flexible symbol-generating capabilities, low noise and low initial and maintenance cost, Model 7022 dot matrix impact printer has 22 column capacity at 12 characters/inch, 1.58 lines/sec, 1.86" print line capacity, top of form sensor option. It accepts multi-copy forms up to 0.015" thickness of almost any size and is suited for label applications. The design uses a printing element comprised of 7 print solenoids and print wires; external electronics generate the print pulses to the solenoids which by impacting wires on a ribbon or pressure sensitive paper form a wide variety of character fonts and densities. An electronic clock, instead of feedback signals, determines character positioning with attendant savings in electronics. Maximum H x W x D: 6.4 x 6.85 x 4.62 inches. Developed and manufactured by LRC, Inc., Riverton, Wyoming, U.S.A., the line is represented and guaranteed by C. Itoh Electronics, Inc., 280 Park Ave., NY, NY. **Circle 260**

product news

CASSETTE RECORDERS

16 page catalog describes cassette recorder products. Included are descriptions, specifications and application information on low power recorders for data logging, complete data loggers with crystal controlled clocks, universal readers, incremental transports and OEM high speed continuous recorders. Information on accessories, supplies and cassettes is also included with two pages devoted to recording techniques and tape formats and a handy ASCII Code Chart. Memodyne Corp., 385 Elliot St., Newton Upper Falls, MA 02164. **Circle 258**

30 AMP-HOUR LITHIUM BATTERY FOR CMOS LOGIC

A high performance lithium primary cell provides 30 ampere-hours at 1.0 ampere drain for an energy density of 135 whr/lb. Model 660-5A has a shelf life greater than 5 years; low temperature performance to -65°F; 2.8 volts nominal operating voltage; and a high rate discharge performance. Ten ounces in weight, 1.64 inches in diameter and 5.5 inches high, it has been designed for: emergency locator

transmitters; underwater transponders, pingers, sonobuoys and instrumentation; meter reading, meteorological instruments; and even the unusual such as animal biotelemetry. Delivery is from stock to 2 weeks; pricing is under $10.00 each in OEM quantities. Power Conversion, Inc., 70 MacQuesten Parkway South, Mt. Vernon, NY 10550. **Circle 265**

PROTOTYPE MAGNETIC HEADS SERVE DOUBLE-SIDED FLOPPIES

These prototype magnetic heads for double-sided floppy-disk drives serve units designed for media interchange with the IBM Model 43FD. Each assembly consists of a ferrite/ceramic, single-track magnetic head with a read/write section and a tunnel erase section, a flexible printed circuit lead-in cable and a load arm, all mounted on a flexure spring attached to a flexure support. A catamaran head bearing surface contacts the disk. In operation, two head assemblies face each other on opposite sides of the flexible disk and squeeze the disk so that each head acts as the head/media interface force for the other. Read/write track width equals 13 mils, and the two adjacent erase track widths measure 6 mils each. Both the read/write and erase cores have gap lengths of 100 μin. Write current varies from 10 mA peak-to-peak on the outer tracks to 7 mA peak-to-peak on the inner tracks, and the dc tunnel erase current equals 80 mA. Typical output with the disk rotating at 360 rpm and the load force set at 7 gm ranges from 20 mV peak-to-peak maximum at the outer track at half frequency (125 kHz) to 3 mV peak-to-peak minimum at the inner track at full frequency (250 kHz). Maximum packaging density equals 3268 bpi, and radial density measures 48 tpi. Price for Models 623100 (side 0) and 623101 (side 1) head/flexure assemblies: $50 each in sets of two. Applied Magnetics, Magnetic Head Div., 75 Robin Hill Rd., Goleta, CA 93017. **Circle 238**

4K DYNAMIC BIPOLAR RAM ACCESSES IN 100 NS

This 4K dynamic bipolar RAM incorporates fast paging, controllable data latch and two chip selects. Its faster version, the 93481A, has a maximum access time of 100 ns and a 240 ns cycle time. The standard 93481 has a maximum access time of 120 ns and a 280 ns cycle time. Both devices operate over the 0° to 70° C range and require a 5V ±5% supply. All pins on the 4K x 1 units meet standard TTL specifications. Power consumption measures 350 mW active, 70 mW standby and 500 mW in page mode at +5V. Page mode access and cycle times are 75 ns for the 93481 and 65 ns for the 93481A. Both units come in standard 16-pin ceramic DIPs. Prices: $24 for the 93481 and $31.20 for the 93481A, both in 100s. Fairchild Camera and Instrument Corp., 464 Ellis St., ms 20-1050, Mountain View, CA 94042. (415) 962-3951 **Circle 233**

20-LB PORTABLE CASSETTE SYSTEM MULTIPLEXES 8-CHANNEL ANALOG DATA

Model 331 data acquisition/storage system multiplexes 8 channels of -10 to +10 V analog information on 9-track digital tape cassettes. Information is recorded in 800 bpi, NRZI format, on ½" computer-compatible magnetic tape. Software for subsequent analysis is available and may be tailored to the user's specifications. Biological Technical Services, 18 Fraley Dr., Somerset, NJ 08873. (201) 981-7132 **Circle 235**

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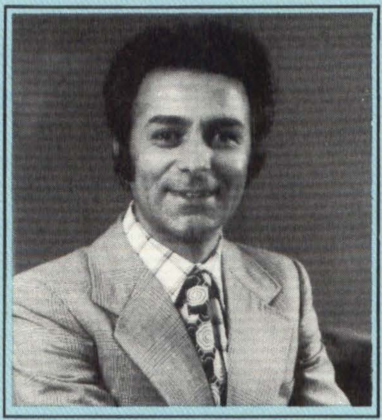

What Makes a Microcomputer Company?

What type of firm can best tap the microcomputer revolution? What, indeed, *is* a microcomputer? The second question is easy to answer; a microcomputer is simply the product of the marriage of LSI technology with the concept of the computer – a hardware structure adaptable to different tasks through programming changes. Indeed, you can best define "microcomputer" by replacing the prefix "micro" with the phrase "LSI implementation of a."

The computer concept is so general and powerful that we now find microcomputers in wristwatches, pocket calculators and video games as well as in the more traditional areas of industrial controllers, terminals and computer peripherals. In the not-too-distant future, we'll also find microcomputers in the implementation of mini and midicomputers, and later, in megacomputers.

What, then, is a microcomputer company? Is it a semiconductor manufacturer that makes pocket calculator circuits organized as microcomputers? Or is it a minicomputer manufacturer that uses LSI implementation for its computers?

Neither of these firms is a microcomputer company, although both manufacture microcomputers. The real potential of microcomputers can only be tapped by a company – distinguished from a traditional component or minicomputer manufacturer – that *controls, innovates in* and *merges* four technologies: semiconductor processing, LSI design, system architecture and software. Only such a company can take full advantage of the merger of LSI technology with the computer; traditional computers and computer architecture, and the firms that implement them, have evolved under the economic pressure and reality of a technology other than LSI.

With LSI, it will be possible within ten years to produce a universal component or building block that will function as a basic network component in both small and large systems. But to achieve this goal, coordinated innovation in all four key technologies will be essential. What we see today in the microcomputer market is only the beginning of a long, irreversible process that will take us into unexplored territories of artificial intelligence.

Federico Faggin *is president of Zilog, Cupertino, CA. We will be pleased to provide space for opposing views.*

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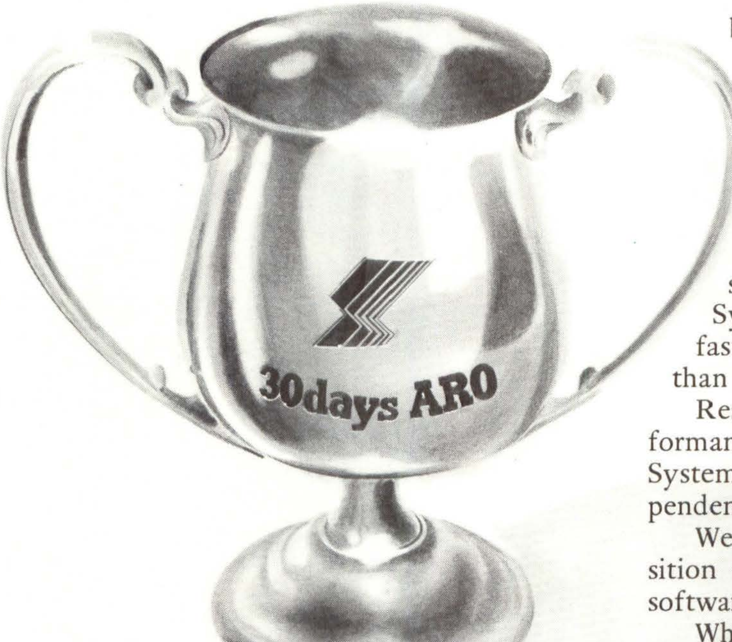

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