DIGITAL DESIGN

SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS

FEBRUARY 1985

- UNLOCKING THE MYSTERIES OF GATE ARRAY DESIGN: PART II
- TAPE DRIVES FILL SECONDARY STORAGE GAP
- UNIX/VMS
- MACHINE VISION
- 1984 EDITORIAL INDEX

LAN & DISK VENDORS SCRAMBLE FOR COMPATIBILITY WITH IBM PC NETWORK

Now your computer can have 20/20 vision.

Now with real time image processing and IBM PC compatibility.

ROBOTICS
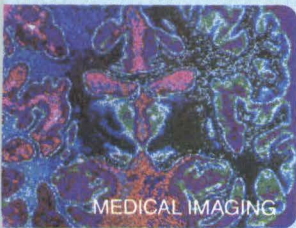
MEDICAL IMAGING

SURVEILLANCE

Datacube continues to be the single source leader in image processing and graphics for your Multibus, Q-Bus, and now IBM PC's. Solutions are available from single boards to fully integrated systems.

Resolutions range from 320H x 240V to 1400H x 1100V with pixel depths from 1 to 24 bits.

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The new IVG-128 is a complete video acquisition and display module on a single IBM PC compatible card. It features input & output look up tables, an 8-bit digitizer, and RGB 8-bit outputs.

The new DC-1000 and DC-1500 systems are complete workstations capable of video acquisition and image processing.
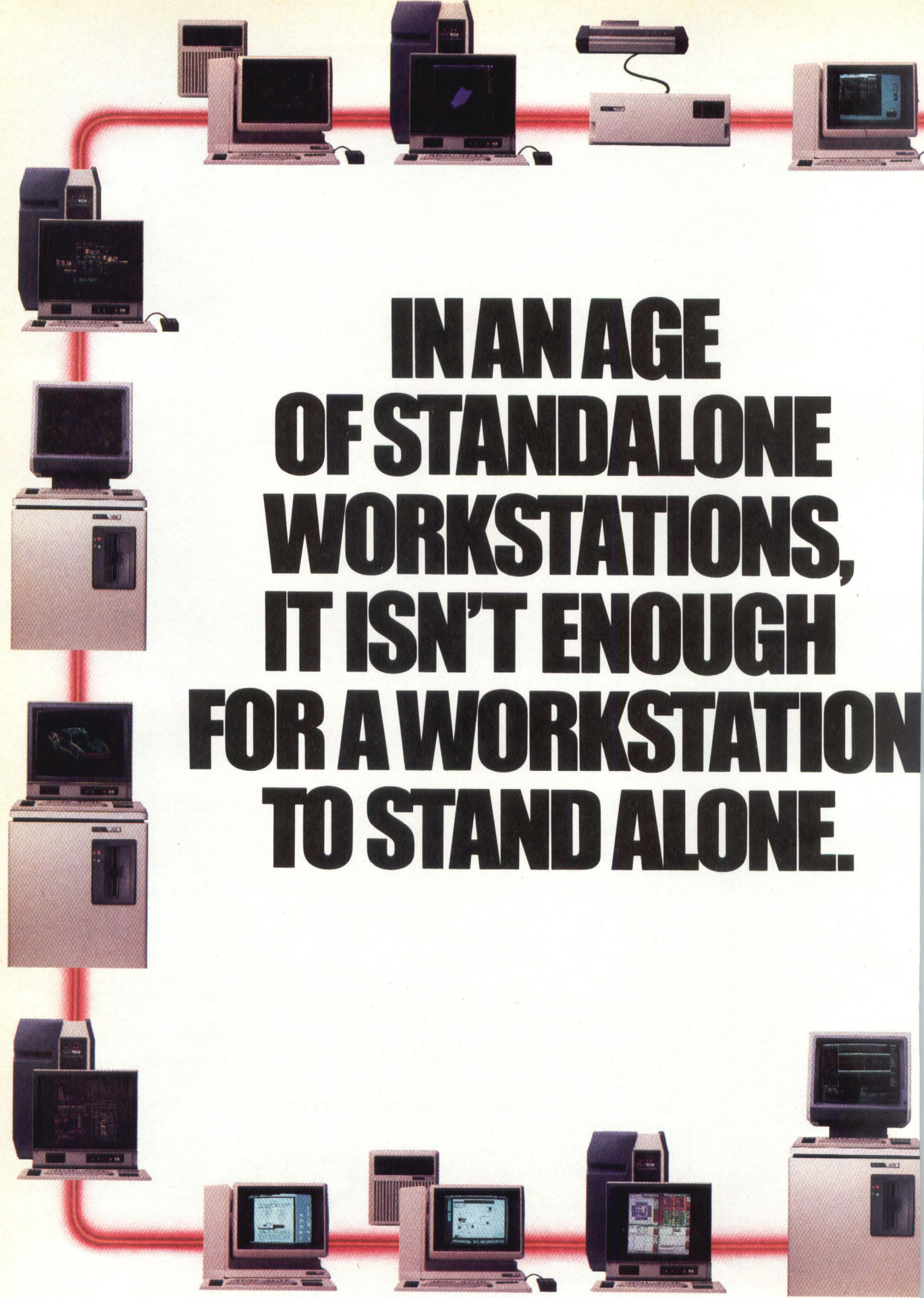
Datacube products provide reliable vision and real time image processing for robotics, medical imaging, surveillance, inspection, teleconferencing, animation, etc. And at surprisingly low prices.

Call or write for our new Product Guide of Multibus, Q-Bus, and IBM PC compatible boards and systems. Datacube Incorporated, 4 Dearborn Road, Peabody, MA 01960, Telephone: (617) 535-6644. Western Sales Office: Telephone: (408) 737-9978.
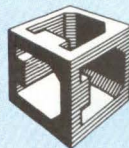
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Circle 4 on Reader Inquiry Card

IN AN AGE OF STANDALONE WORKSTATIONS, IT ISN'T ENOUGH FOR A WORKSTATION TO STAND ALONE.

It's a well-accepted dictum that the bigger the technical problem, the more compute power needed to solve it. A valid reason for engineers and scientists to demand their own standalone computers and the processing power that comes with them.

But experience tells us that the results of one person's efforts are inevitably meant to be shared with other people. A requirement that even the best standalone computers fail to meet.

One computer company has successfully solved this apparent dilemma. Apollo. Instead of simply building standalone computers, we've engineered DOMAIN® processing. A computing environment that adheres to our belief that both processing power and the ability to share that power are equally important in measuring a computer system's true value.

Our workstations don't stand alone because you don't work alone.

Thus DOMAIN combines dedicated 32-bit workstations in a computer system that lets users transparently share both information and resources across a high-speed local area network. Logically offering the advantages of both timesharing and dedicated computers without the drawbacks of either. Timesharing without a terminal case of limited power. Dedicated

workstations without isolation from co-workers and their data.

DOMAIN processing also delivers something else uncommon to standalone computers. A family of compatible workstations. They range from high performance color units for demanding applications such as solids modeling to monochromatic workstations for applications like software engineering.

Adding to DOMAIN's range and choice are more than 300 applications from the world's best software suppliers. Applications that cover electronic design, mechanical design, computer integrated manufacturing and much more. Letting you automate entire development processes rather than individual tasks.

While these facts no doubt attest to the efficacy of DOMAIN processing, it's also reassuring to know that the DOMAIN network even connects to other computer systems via industry standard protocols such as X.25 and ETHERNET.® Of course DOMAIN supports the UNIX® software environment as well.

A reminder that it's because our workstations don't stand alone, that we do stand alone. Call (617) 256-6600 x4497. Or write Apollo, 330 Billerica Rd., Chelmsford, MA 01824, MS 17.

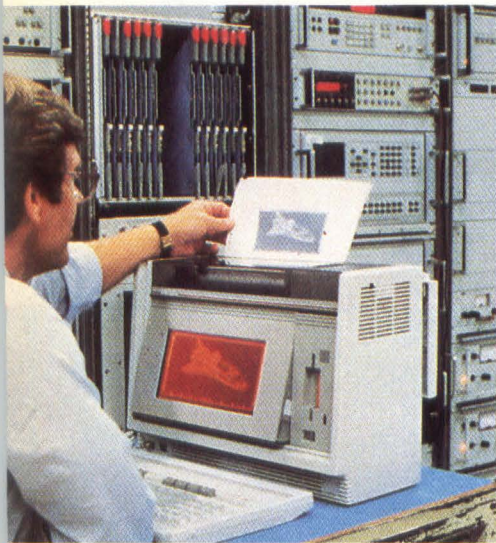# apollo

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DIGITAL DESIGN

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FEATURES

ON THE COVER

The huge installed base of personal computers has revolutionized the way people work; but compared to multiuser computer systems, individuals lack access to common information. With local communication capabilities, PCs will be even more useful. IBM's announcement of a network for their PC products may provide further impetus for the trend to link small systems together into local area networks. Typical components of a LAN for PCs include computers, file servers, interface boards, diskettes, coaxial and twisted pair cables and working blueprints for installation. Photo courtesy Novell, Inc.

DIGITAL'S NETWORKING. AN OPEN WINDOW TO DYNAMIC MARKET GROWTH.

If you want to significantly enhance your OEM product offerings and enable your products to fit in easily with your customers' distributed computing environments, consider the advantages of Digital Network Architecture.

No other company offers a wider range of efficient networking options tailored to OEM requirements. And no other company does so much to help you and your customers achieve the full benefits that networking can provide.

With Digital as your OEM supplier, you'll have the products you need to make local and wide area networking an essential part of your marketing plan. And that opens up an endless growth path for you and your customers.

DIGITAL NETWORK ARCHITECTURE, YOUR WINDOW TO THE WORLD.

Digital Network Architecture (DNA) is the most comprehensive communications strategy yet developed, and currently implemented in proven, deliverable products. It supports several communications technologies. And it can accommodate future standards as they emerge because DNA is implemented in a layered structure consistent with the ISO Open Systems Interconnect model.

As an OEM, DNA gives you tremendous marketing and product opportunities. You can incorporate the best price performance components in your systems.

DIGITAL NETWORK ARCHITECTURE

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2 X.25 | Digital's DDCMP | Ethernet
1

VAX

Packet Switch Network
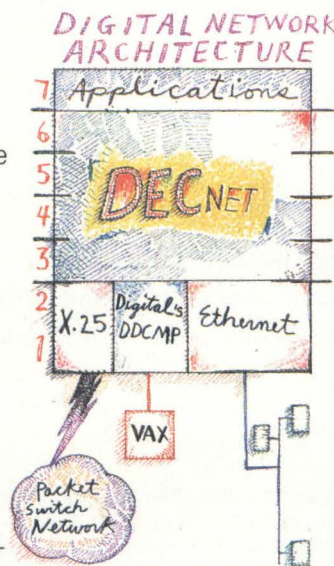
You can communicate with mainframe systems. You can match the technology to the job. And, most importantly, you can keep pace with your customers' distributed processing needs as they develop.

DECnet™ software lets you link Digital's systems in both local and wide area configurations. It supports high-speed local area network communications using Ethernet. And it provides gateways to allow Digital's computers to communicate with other vendors' systems over private lines or packet switched X.25 networks. This means you can tailor your products to fit in with your customers' current and future networks.

BENEFITS FOR YOUR USERS. BENEFITS FOR YOU.

The benefits you and your customers get by incorporating Digital's networking capabilities are virtually unlimited.

First of all, your systems can incorporate recognized industry standards. Such as Ethernet (IEEE 802.3 specification), X.25, and others.

In addition, our growing set of network-based products, including a distributed database system, allow your single systems to easily grow into networks. Your applications can access remote data and other resources transparently, with no extra development required.

This means that, with Digital, your systems are in an excellent position to be widely used in your customers' computing environments.

ENGINEERED FOR SUCCESS IN MULTIVENDOR ENVIRONMENTS.

Your products need to communicate with equipment from different vendors. Ethernet was designed with this fact in mind. Today, Ethernet-based networks are proliferating across all application segments – such as CAD/CAM, ATE, factory automation and medical applications.

Digital's networking systems allow Ethernet to be part of a single-source solution for your OEM installations. And DECnet gateways provide highly functional links to other non-Digital communications environments.

In short, DNA and Digital's products do the most to ensure that your systems will fit in with both new and existing networks.

WE'LL BACK YOU WITH TRAINING AND SUPPORT.

If you're already a Digital OEM, you know the advantages of Digital training and support. It's second to none in the industry.

We can give you the skills to configure, market, install and service local and wide area networks effectively. We'll help you make the most of our networking products in your systems.

Digital representatives are available for pre-sales consultation and installation assistance. And our world-wide service organization can provide all the on-site network maintenance your customers require.

BEST ENGINEERED MEANS ENGINEERED TO A PLAN.

The communications systems implemented as part of Digital Network Architecture, like all Digital hardware and software products, are engineered to conform to an overall computing strategy. This means our systems are engineered to work together easily and expand economically.

Every system we make – from the Professional™ 300 Series workstations, to our MicroVAX I™ supermicro, to our high-end VAX™ computing systems – can cooperate using DECnet software. Only Digital provides you with a single, integrated computing strategy, from chips to 32-bit systems, and direct from desktop to data center.

For more information about how you can make networking from Digital part of your product line, send in the coupon below or contact your Digital Sales Representative or a Digital Authorized Industrial Distributor. Or call 1-800-848-4400, ext. 139.

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☐ I'd like the whole story about OEM networking opportunities with Digital. Please have your representative call today.

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The lean, mean plotting machine from Houston Instrument

Houston Instrument's brand new servo driven DMP-51 is the fastest drum plotter we've designed to date. This superb plotter offers a pen speed of up to 22 inches/second; programmable accelerations, and a pen-on-paper resolution of 1/1000 of an inch! That means you'll turn out quality 17″ x 22″ and 22″ x 34″ drawings a lot faster, increasing your firm's productivity and profitability.

Now, for more good news. The DMP-51, priced at $4,495*, is as fast as other plotters costing three times more. At that price, you can afford to put a DMP-51 at individual drafting work stations.

This is the professional plotter that meets the needs—and the budgets—of all companies, large or small.

The DMP-51 is intelligent, too. The DMP-51 can execute complex graphics operations from the simplest commands. A mechanical/architectural version, the DMP-52, with its 18″ x 24″ and 24″ x 36″ paper size, is available for the same price from Houston Instrument.

So, watch our new plotter in action . . . it won't take much time to realize it's the best buy for your money. For the name, address and phone number of your nearest dealer or distributor, write Houston Instrument, 8500 Cameron Rd., Austin, Texas, 78753. You can also call 1-800-531-5205 or 1-512-835-0900 (Texas residents). In Europe, contact Houston Instrument Belgium NV, Rochesterlaan 6, 8240 Gistel, Belgium. Tel: 059-27-74-45. Tlx: 846-81399.
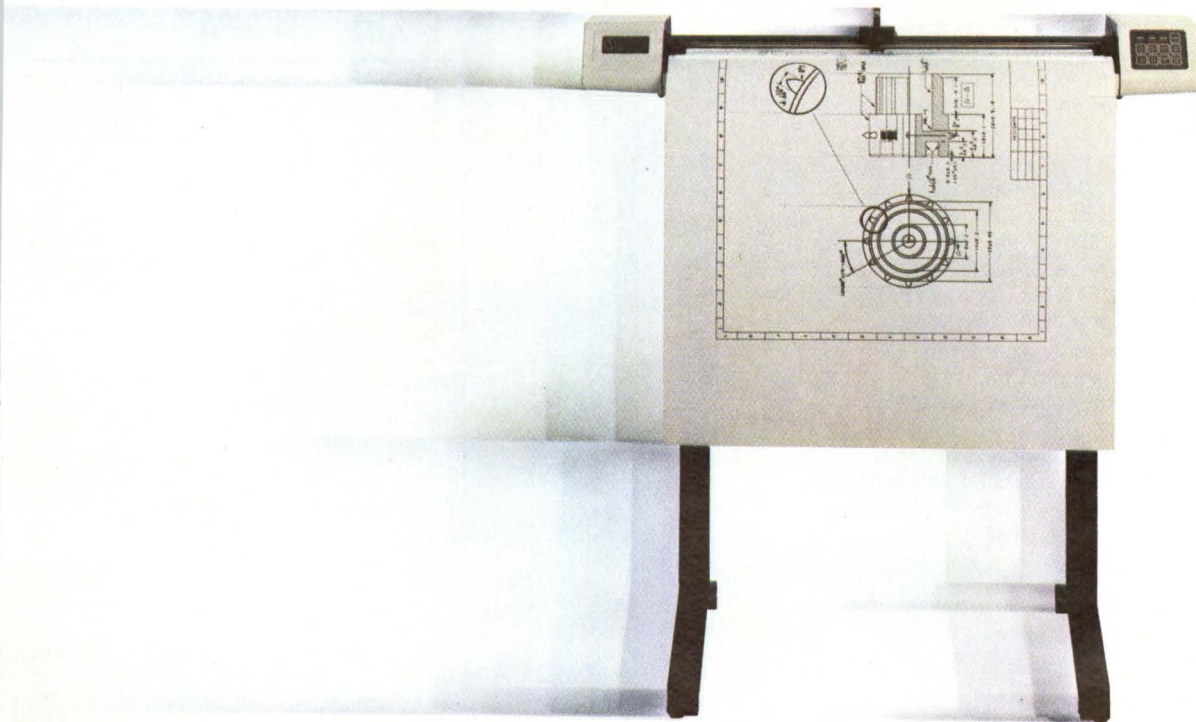
*Suggested U.S. retail price

houston instrument

25th Anniversary 1959-1984

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1. High Speed (MicroCAD Software)
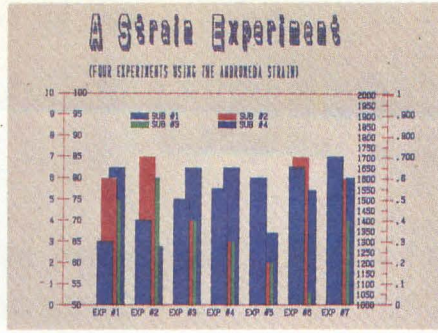
2. Dual Display Modes (Energraphics Software)
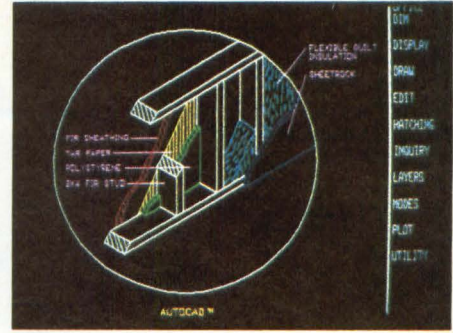
3. Simplified Processing (AutoCAD Software)
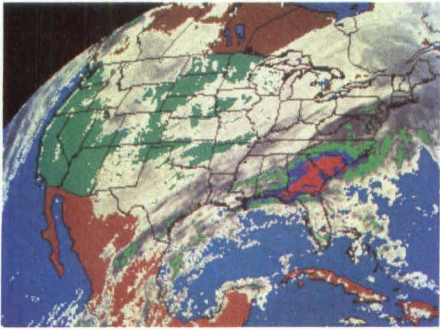
4. 9 Bit Planes (Courtesy WSI Inc., Bedford, MA)

5. 16.8M Color Shades (Courtesy Catherine Del Tito, Wave Graphics)
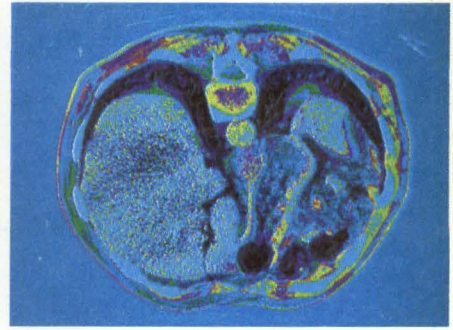
6. High Resolution (Courtesy University of North Carolina at Chapel Hill, Depts of Computer Science and Radiology)

Six reasons why professionals continue to choose Vectrix for quality IBM XT/PC graphics.

Even though IBM offers a color graphics card, professionals still choose Vectrix. It's not surprising. Especially once they've seen us in action. Professionals know that our VX/PC Board Set delivers the quality and performance they need for serious color graphics.

The VX/PC Board Set provides advanced features that help simplify sophisticated graphics design. Besides displaying 512 simultaneous colors from a palette of 16.8 million, the VX/PC supports an extensive library of on-board graphics macros for ease of programming and fast design, as well as full emulation of the IBM color card. And, an on-board 16-bit micro-processor frees your computer to concentrate on other tasks.

But that's not all. Our 9 bit planes add an extra dimension of sharpness and clarity to your image that must really be seen to be appreciated. That's why it's not surprising to see Vectrix color cards in applications such as medical imaging, weather satellite data mapping, computer aided design and drafting, and graphics arts, to name a few.
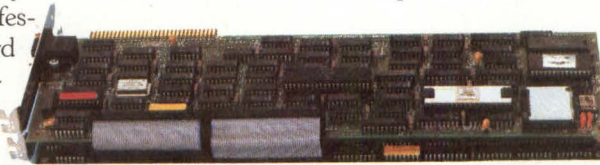
What you will find most surprising, however, is the price. Our VX/PC Board Set was designed with the OEM in mind. So when comparing the performance of Vectrix with the competition, check the price too. You'll like what you see. For more information, contact Vectrix Corporation, 2606 Branchwood Drive, Greensboro, North Carolina 27408. Phone (919) 288-0520. Telex 574417.

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PDOS

UNIX V

COHERENT

PASCAL

C

FORTRAN

PDOS

UNIX V

COHERENT

> **'Write, call, drop in or communicate in any way you see fit, but let us know where you stand.'**

The Secret Is Out

When I accepted the position as editor-in-chief of *Digital Design*, I had some misgivings. It's not the most successful magazine in the industry and has been in the position of an also-ran for most of its 14 year history. Nonetheless, I knew that something was happening to the magazine because it had been improving for a year — most noticeably in the last six months. But despite those good signs, I still expected to find the editorial staff in disarray.

Instead, I found the best kept secret in trade magazine publishing: the staff is the brightest, youngest, most energetic and technically competent group of editors that I have ever worked with. Working long hours, they remain dedicated to the task of making *Digital Design* the best in the industry. It is my job to make it easy for this enthusiastic group of editors to do their best work and to provide the best editorial coverage available.

Good editorial coverage is achieved, very simply, by serving our readers' professional needs. It is not so simple, however, to recognize the real needs of the readers. Although that is the key to editorial success, it is probably the hardest information to come by.

All controlled circulation magazines, of course, claim to know exactly what the readers in their particular market niche want and need. They base their positions on readership studies, industry knowledge and, less apparently, old-fashioned guessing and editorial whim. Studies alone are not sufficient, and good intuitive editorial judgement is needed to set a magazine apart from its competitors.

Whether a magazine serves the reader or not, its success will depend on whether the advertisers are convinced that it does. And, of course, the best way to convince potential advertisers is to actually serve the readers — to give them what they need. Only very fat, successful magazines can afford the luxury of not serving their reader's interests; and such self-deception cannot go on forever. Eventually, it catches up with them. Consequently, *Digital Design* has no choice. We must find out what our readers need and do the best we possibly can to fulfill their expectations.

What do the design engineers who read *Digital Design* need to know and how should it be organized? We have formal readership studies and focus groups to help us with the answers but we need dialogue with the readers. Write, call, drop in or communicate in any way you see fit, but let us know where you stand.

During the coming year we will make a number of changes to *Digital Design*. Most of these will be developed from what you've already told us but some may be experimental. Anything can be done or undone, within the limits of common sense, but we need your feedback to keep us on the right track.

With some help we can make this the best design magazine in the industry. We have a staff that is knowledgeable, eager and ready to turn *Digital Design* into the best-read magazine around — with a little help from our friends — the readers.

John Bond, Editor-in-Chief

UPDATE

Floppy Disk With Narrow Read/Write Gap

Nippon Telegraph jointly developed with Telephone Public Corp. a 3½″ microfloppy disk drive with a 1.6 Mbit storage capacity. Features of the floppy disk include a magnetic head with improved magnetic efficiency, a narrower read/write gap which overcomes accuracy reducing mutual interference and interchangeable specifications with previous models with 77 tracks, a 14,000 bpi maximum bit density and a 135 tpi track density.

Department Of Defense Requires LOGMARS

More than 50,000 US manufacturers will be directly affected by the Department of Defense's requirement for application of bar code markings to material procured by the military. The Logistics Applications of Automated Marking and Reading Systems (LOGMARS) project for barcoding is expected to save the Government more than $100 million per year in inventory costs.

Ultra-Short Light Pulses

Using a laser and an IBM developed "light compressor", IBM scientists claim they have generated the world's shortest light pulses. The ultra-short pulses (12 femtoseconds) are made by alternately switching and compressing laser light. They can serve as a "strobelight", slowing or feeezing the apparent motion of molecules, atoms and electrons so that their extremely rapid interaction may be studied in detail.

JEDEC To Revise CMOS Standard

The Joint Electron Device Engineering Council (JEDEC) Committee JC-40.2 on HC/HCT Logic Standard plans to revise Standard No. 7 titled "Standard for Description of 54/74XXXX, 54/74HCU XXXX and 54/74HCTXXXX High Speed CMOS Devices" to include higher speed families. The revised Standard, targeted to be completed by the end of 1985, also includes an I_{CC} value for HCT when inputs are at V_{IH}, Schmitt Trigger type switching and hysteresis voltage standards, Hex level converter standards, DC standards for analog multiplexers operating up to 10 V.

Cipher Data To Acquire Spectra Logic

Cipher Data Products Inc. signed a letter of intent to acquire privately-held Spectra Logic Corp. for an undisclosed number of shares of its common stock. Cipher intends to develop more intelligent memory subsystem products by combining Spectra Logic's knowledge of peripheral controllers with its data storage devices.

PA Technology Forms Semiconductor Company

PA Technology, the science and technology division, of PA Consulting Services, formed a new semiconductor manufacturing company, Array Logic. The company will design and manufacture prototype and small volume semicustom devices. Manufacture begins in March 1985.

Corvus, NEC To Develop CMOS Single-Chip Controller

Corvus Systems, Inc. and NEC Corp. are jointly developing a CMOS single-chip Omninet LAN controller. The one-chip controller will be manufactured and distributed by NEC to Corvus and its Omninet licensees and increases transmission speeds from 1 Mbit/sec to 4 Mbits/sec. The one-chip controller will be upwardly compatible with the current three-chip set.

Paladin Software, VisiCorp Combine Forces

Paladin Software Corp. and VisiCorp signed a letter of intent to merge through an exchange of stock. The new company, named Paladin Software Corp., develops and markets personal computer software, including a range of VisiCorp products.

AMD Suspends IC Shipments To Government Contractors

Advanced Micro Devices has suspended shipment of certain ICs purchased by government contractors until it can verify that all test procedures specified in the customers' source control drawings (SCDs) are being accurately followed. Discrepancies between AMD's procedures and the customer's requirements were uncovered by an internal audit. AMD expects to have all SCDs reviewed and discrepancies resolved by the end of March 1985.

Winchester Disk Drive Suppliers Merge

Under a definitive merger agreement between Vertex Peripherals and Priam Corp., Priam will exchange shares of newly issued common stock for shares of common and preferred stock held by Vertex shareholders. Priam currently has 15.7 million shares of common stock outstanding, and plans to issue approximately 7.12 million shares to current Vertex shareholders.

Summit Peripherals Introduces Microfloppy Disk Drive

Summit Peripherals, Inc. plans to enter the 3½″ disk drive market with a family of high performance, low power consumption 3½″ microfloppy disk drives. The initial product, SuPer 100, is a 1 Mbyte microfloppy disk drive, designed for the new generations of desktop and portable computer systems. Slated for first quarter 1985 production, the SuPer 100 will be followed by the introduction of higher capacity microfloppy disk drives over the next few years.

Data I/O, FutureNet Merger

The acquisition by Data I/O Corp. of FutureNet Corp. in exchange for 2,006,030 shares of Data I/O common stock has been completed. In addition, approximately 154,000 shares of common stock have been reserved to cover the exercise of stock options previously granted to FutureNet employees.

Anritsu Enters Peripheral Market

Anritsu American, a supplier of test and measurement instruments for electronics, telecommunications and broadcast industries, will join the computer peripheral market in its US operations with its family of ANSI/IBM-compatible tape drives. The family of products comprises a series of compact, ½″ streaming magnetic tape drives, a series of cartridge tape drives and a series of 10½″ reel magnetic tape drives.

Because You need to run FORTRAN programs 10X to 100X faster...
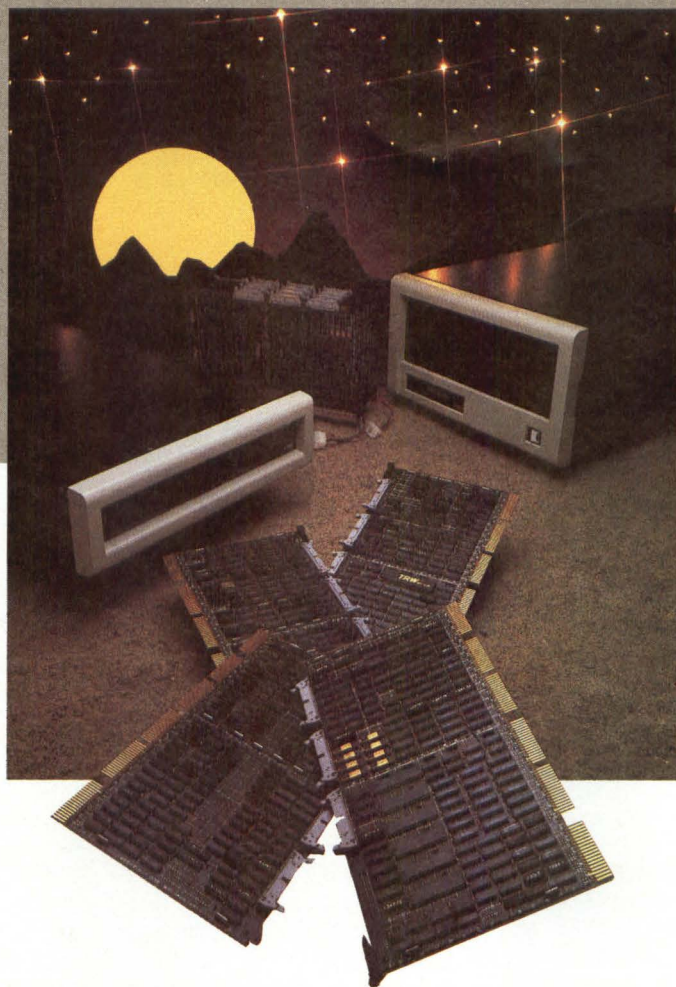
Mini-MAP makes it practical to apply array processing to general-purpose scientific and engineering computing.

Practical in terms of use: Mini-MAP's compiler allows you to program the array processor directly in FOR-TRAN. An assembler, a linker, and a debugger are also part of the package. Plus you can use our library of over 250 highly optimized scientific subroutines.

Practical in terms of throughput: Because it is an array processor, Mini-MAP increases the computing speed of a mini or super-mini computer as much as 10 to 100 times. Where it takes a typical minicomputer minutes to perform tasks such as image rotation, Mini-MAP reduces interactive response times to seconds. Your computer may require hours to perform each step of a trial-and-error-process such as simulation, but Mini-MAP, can zip through in mere minutes.

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Practical in terms of cost: Mini-MAP is available as an economical, four-board set or as a packaged system. Now, with Mini-MAP, OEMs can offer their customers a better product at lower costs. Mini-MAP's low power demands, small size, and high reliability make the package extremely attractive. And end users will find our FORTRAN compiler and other software tools minimize program development costs.

Some practical things to know about Mini-MAP: 32-bit DEC™ floating point format □ Interfaces to DEC PDP-11, LSI-11, and VAX-11 series □ Up to 16 MBytes of data memory □ 1024 x 1024 2-D FFT in 8.8 seconds □ Extensive software tools plus dedicated applications assistance including training, convenient parts depots, and field service staff support our worldwide installations.
To find out how Mini-MAP can work for you, **call toll free 1 800 325-3110.**

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WASHINGTON REPORT

by Anne A. Armstrong

New Standard Proposed For Computer Software

The National Information Standards Organization, a committee of the American National Standards Institute, has completed a draft standard for numbering computer software. The group decided against adopting any of the three identifying systems currently being used by publishers and has devised a new system.

In 1983, the committee identified 10,000 producers of some 40,000 programs. With numbers of that size, the committee decided that an adequate system must have the ability to handle 99,999 organizations, and 9,999 products per organization.

The proposed Standard Computer Software Number (SCSN) is a 13-digit number, which is coded to show the registering organization, a 4-digit product number assigned by the publisher, a 3-digit unit number that indicates version or operating system required and finally a check character to guard against improper data transcription, (e.g., SCSN 11013-1234-123-5).

If adopted as a standard, the SCSN would appear on all packaging, price lists, promotional literature, catalog information and manuals or instruction sheets. Copies of the draft standard may be obtained from NISO (Z39), National Bureau of Standards, Admin. 101, Library E106, Gaitherburg, MD 20899.

More Companies Halt Shipments To DOD Contractors

Schlumberger's Fairchild Semiconductor Division and Advanced Micro Devices are reported to have halted shipments of source control drawing devices to DOD contractors because of improper testing. The two companies join the growing ranks of semiconductor manufacturers who have run afoul of the Defense Logistics Agency's testing procedures. Texas Instruments and Signetics have also had to recall and retest thousands of specially designed circuits.

Although DLA made public announcements about the first two recalls, officials have not acknowledged the Fairchild and AMD testing problems. A group of electronics industry officials is working with DOD to try to devise methods less drastic than stopping shipments for dealing with testing deficiencies.

New Supercomputer Research Center Established By DOD

The Department of Defense has awarded the Institute of Defense Analysis a $12 million contract to set up a supercomputer research center in Prince George's County, a Maryland suburb of Washington, DC. The new center would be managed by the National Security Agency and would be an important part of NSA's signal intelligence, encryption and code-breaking work.

Although most information about NSA is classified, observers believe that the agency is a prime user of supercomputers and that the new research center would investigate parallel processing techniques for decoding ciphers.

The new research activity is distinct from the Defense Advanced Research Projects Agency (DARPA) and is not part of its strategic computing project, although officials of both programs say they will cooperate and will exchange information. DOD has recently established another research center, the Software Engineering Institute at Carnegie Mellon University in Pittsburgh.

Conference Predicts Writable Drives Soon

Industry analysts and market researchers attending the 1984 Videodisc, Optical Disk and Compact Disc Conference held in Washington last December offered some predictions and timetables about when various models of new optical drives will be on the market. Steven K. Sieck of Link Resources told conference attendees that he expects all major CD-ROM (compact disc-read only memory) manufacturers to have writable drives ready for the marketplace within the next year. Most are expected to fit the floppy disk footprint of a personal computer.

Ed Rothchild, publisher of Optical Memory News, said IBM will have a writable 5¼" optical disk drive ready within the next six months. Although speculation about IBM's interest in optical drives appears periodically in the press, Rothchild offers some new details. He says that the writable disk will hold only 100 Mbytes of data, instead of the 600 Mbytes possible on a mastered compact disk. One reason given for the disparity is that the write head cannot pack data as tightly as a mastering facility. In addition, he says the thrust of IBM's entrance into optical technology will be for the PC because it already has a secure hold on mass memory for mainframes.

Rothchild also reported that Hitachi is demonstrating in private showings a prototype of a 5¼" magneto-optical erasable drive and media. Shown to some analysts privately in Tokyo, rumors of the new drive prompted Hitachi to demonstrate the equipment to a very select group of preferred clients. The hybrid system, which requires a special pre-grooved disk with a magnetic film under a plastic coating, is similar to one under development by Matsushita.

Tandon Accuses 3 Firms Of Infringing Patents

Tandon Corp. has filed a Section 337 petition with the International Trade Commission in Washington and a civil lawsuit in the US District Court in Los Angeles against three firms it says have infringed on its floppy disk drive patent. Tandon, which is based in Chatworth, CA, says that Mitsubishi, TEAC Corp. and Sony Corp. have violated its patent No. 4,151,573 which covers the 3½" double-sided drive.

The ITC scheduled a vote on the question of whether to investigate Tandon's claims for early January (results of the vote were not available by press deadline). If, as expected, the commission decides to conduct an investigation, then, by statute, the probe should be completed in a year.

An attorney at the commission told us it is important to understand that if the ITC decides for Tandon it could act not just against the three companies named—but could issue a general exclusion order against all drives that fit the classification. And the commission has been told by Tandon that it believes a number of other companies may be involved.

One reason why companies use the ITC procedure is that it offers US firms expedited proceedings, the attorney said. "A company can get an answer and some relief in a year at ITC. A District Court case can drag on for three or four years."

Tandon filed another petition in August 1984 against a Korean firm, Gold Star, and its US distributor Format Corp. However, Tandon officials emphasize that the two cases are not related. The Gold Star case centers on industrial espionage and sabotage, not patent infringement.

Suddenly, everyone's headed for MARS.

The MARS-432 32-bit, programmable, floating point array processor.

And with good reason. Because the MARS-432 has opened up a new world of speed, power and ease-of-use that's hard for anyone to resist.

The MARS-432 already interfaces with some of this world's leading computers — DEC, Apollo, Elxsi — to provide users with a new level of computational power. Interfaces for other leaders such as IBM, Perkin-Elmer, and Gould/SEL are scheduled to arrive soon.

Simply put, we're setting the direction in state-of-the-art array processors with features such as:

Programming Ease

All of the computational power of an array processor doesn't mean much if accessing that power requires days of tedious programming, debugging and reprogramming. That's why we engineered the MARS-432 with an architecture specifically designed to support a FORTRAN compiler and a screen-oriented debugging system that make accessing and utilizing its raw power a very civilized process.

The MARS-432 also provides:

☐ *A Microcode Development System for off-line program development.*

☐ *An AP Run Time Executive Support Package (AREX) for simplified processor initialization, I/O operations, and array function executions.*

☐ *Applications Libraries for math, signal processing, and image processing.*

Speed

☐ *Add and multiply times of 100ns.*
☐ *Computational power of 30 megaflops.*
☐ *Computes a 1024-point complex FFT in 1.7ms.*
☐ *DMA transfers at I/O bus rates of 20 megabytes/sec.*
☐ *Data memory write or two reads in 100ns.*
☐ *Memory paging for uninterrupted processing during I/O transactions.*

Impressive Memory

Program memory contains a physical address space of 4K words and a virtual address space of 64K words via a cache configuration. Data memory contains a physical address space of 16 million words.

The MARS-432 from Numerix: a journey to faster, more affordable array processing power. With programming ease that sets it worlds apart.

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VAX

MICRO VAX

APOLLO

ELXSI

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On the other hand there is Apollo. We believe that computer systems should aid engineers and scientists in their design efforts. Not tax them with unimportant details like remembering where a piece of information is stored.

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With DOMAIN processing it doesn't matter where a file was entered or stored.

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If your product developers spend too much time searching for information and too little developing new products, we suggest you contact Apollo. And see how productive computing can be. Call (617) 256-6600 x4497. Or write Apollo, 330 Billerica Rd., Chelmsford, MA 01824, MS 17.

Each workstation on the DOMAIN network provides transparent access to needed information.

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UNIX-Based Portable Provides Multitasking For Instrument Control And Data Acquisition

Hewlett-Packard's Integral Personal Computer provides portability and enhanced real time and I/O features.

Using UNIX in addition to I/O and IEEE-488 instrumentation ports on a microcomputer is a good base for instrument control and data acquisition. To allow such a machine to be moved around in a lab or industrial environment, Hewlett-Packard has burned the kernel of their HP-UX UNIX into ROM and built in a microfloppy disk drive, 9″ electroluminescent display and ink jet printer. The HP Integral Personal Computer is based on an 8 MHz 16/32 bit MC68000 and has a 16-bit graphics processor as well as window and user-interface software in ROM to make the system easier to use.

The entire system measures just over 8″ wide (at its widest) × 13″ long × 16″ high and weighs 25 pounds. Initial list price for the system is $4,995, including disks for HP-UX commands, utilities and applications. Since OS and other basic software are ROM-based, no hard disk is needed. The trade-off for eliminating the hard disk is that, except the kernel, software must run on floppy disks.

A standard system comes with 800 Kbytes of memory: 512K for user RAM, 32 Kbytes for display RAM and 256 Kbytes of ROM for the HP-UX, Windows and Personal Applications Manager software (though UNIX takes several Mbytes, this kernel takes only about 100K). A ROM plug-in port allows OS versions to be upgraded easily. By using a copy to root command, any or all of the user RAM acts as a RAM disk. RAM disk allows rapid data access and looks like a second disk drive to applications that need two disks.

According to HP, their HP-UX version of UNIX is optimized for I/O through real time extensions and soon, DIL (device-independent library). Real time operation is especially critical for data acquisition and control applications; for this machine, HP defines real time as about 100 msec per interrupt.

The extensions provided include shared memory, memory lock, real time priority, sync file system, interval and time of day clocks and reliable software signals to assure that an interrupt put in when the processor is busy will not be lost. DIL provides subroutines for high-level language calls to instrumentation and will initially support HP-IB, Serial, GPIB and BCD devices. To provide an upgrade for existing HP Series 80 users, HP-UX Basic is offered as an option; C is another option available.

As many as 14 instruments can be daisy-chained to the built-in HPIB interface. And, unlike some low-end portables, the Integral PC has two expansion slots. Option cards available for I/O include RS-232, GPIB, HP-IL, BCD, current loop and a 300/1200 baud modem. The slots could also be used for 256K or 512K RAM cards.

Like the 68000 processor, peripherals built into the system are more powerful than the average portable's. The ink jet printer is quiet and prints 150 cps in 80 or 142 columns. A 9″ flat panel display of 512 × 255 pixels gives 31 lines × 80 characters. The hard-jacket 3½″ microfloppy is used in other HP personal computer systems; each double-sided disk holds 710 Kbytes. The keyboard is detachable and low profile with the numeric pad included. For other forms of input, two human-interface loop ports accommodate mouse, tablet or bar-code reader devices.

Should a larger system be desired, a bus expander with five added slots is offered. Not only can more I/O cards be used, but memory expansion up to 5.5 Mbytes is possible. With two bus expanders, 12 slots (two in the main chassis) are available for add-ons. Additional microfloppy and Winchester disk drives up to 55 Mbytes can be added. Other peripherals that will operate with the Integral PC include daisy wheel, dot matrix and laser jet printers and HP model 7470/75 and 7550 plotters.

With their inside track on the instrumentation market, the need for a powerful portable computer must be strong. The combination of multitasking UNIX software with real time features, built-in I/O expansion slots and 488 interface makes this particularly suited to instrumentation and control applications. Integration of peripherals into the package should provide a versatile tool for many environments. —*Pingry*

Circle 238

Multibus II Boards Support Advanced System Architecture

Since the introduction of the specification, it was obvious that the Multibus II would allow the systems architect to implement a high performance multiprocessing system. Now, the introduction of several Multibus II products from Intel will allow the realization of that architecture (**Figure 1**). The lineup is impressive. It includes a single board computer, several cache-based memory boards, a central services module and software support.

The CPU board, the iSBC 286/100, utilizes the Intel 8 MHz iAPX286 and supports the iPSB bus features of interconnect space, built-in self-test diagnostics and message-based interrupts. Multibus II interconnect space is a standardized set of read-only and software configurable registers: the read-only registers hold information such as board type, and the software configurable registers allow read and write operations under software control.

The iSBC 286/100 board uses Multibus II interconnect space for dynamic software system configuration and remote diagnostics and testing. A software monitor can be used to dynamically change iLBX II bus memory sizes, to disable on-board resources, such as PROM or JEDEC sites, and to read if iSBX bus or PROM are installed as well as to access the results of built-in self-tests or user installed diagnostics.

Resident firmware to support Multibus II's built-in self-test power-up diagnostics is supplied by on-board microcontrollers. These improve the reliability and error reporting and recovery capability of Multibus II boards. In a Multibus II
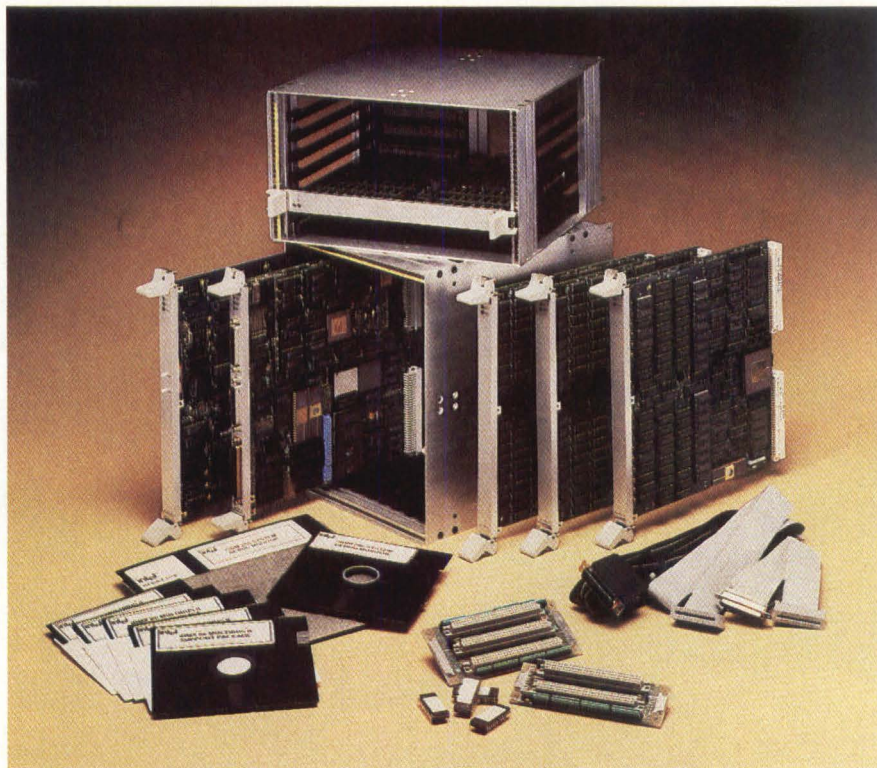
New family of Multibus II products from Intel.

system, external interrupts (originating off the CPU board) are messages over the bus rather than signals on individual lines. Message-based interrupts are handled by a Message Interrupt Controller located on a bus interface piggyback module. This allows one interrupt line to handle interrupts from up to 256 sources.

The iSBC MEM/3XX family of memory boards are dual ported with access to the interfaces of both the Multibus II Parallel System Bus (iPSB) and the iLBX II (Local Bus Extension). The four main subsystems of the iSBC MEM/3XX boards are the cache controller subsystem, the cache memory subsystem, the DRAM memory subsystem and the interconnect space subsystem (**Figure 2**). The cache memory system is designed around the 32-bit architecture of the main memory system. The cache memory controller and the 8 Kbytes of SRAM cache memory subsystems improve CPU to RAM execution to zero wait state read accesses over the iLBX II bus when data requested is in the cache. A cache hit takes 125 nsec with an 8 MHz iLBX II clock. Using this series of memory boards, the maximum system memory capacity based on one CPU board and 19 memory boards is 76 Mbytes on the iPSB bus. (Similarily, the maximum iLBX II memory capacity is 20 Mbytes.) The memory partitioning is independent of the iPSB bus interface and the iLBX II bus interface.
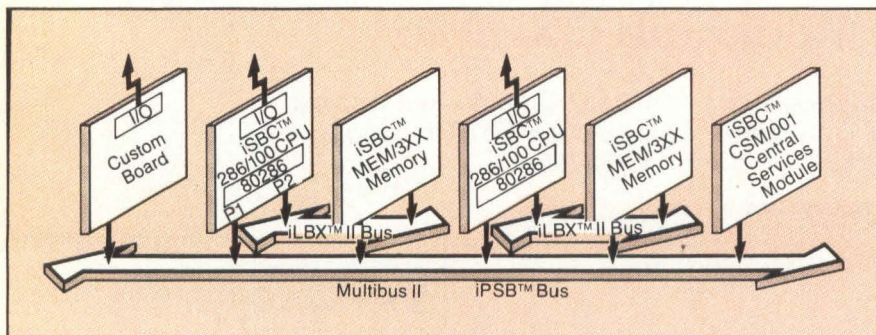
Figure 1: Typical Multibus II system configuration.

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CHUM stands for CMOS High-speed Universal Microarray. There are two products available: the CHUM-99 (22 pads), and the CHUM-180 (40 pads). Both have high-frequency performance, low power dissipation, and a wide power-supply range (3–8 volts).

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CHUM SPECIFICATIONS

Parameter	CHUM-99	CHUM-180
Bonding Pads	22	40
Gates	99	180
Output Drive	9 ma	6 ma
Frequency	25 MHz	25 MHz
Voltage Range	3–8 Vdc	3–8 Vdc

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Circle 17 on Reader Inquiry Card

Figure 2: iSBC MEM/3XX board block diagram.
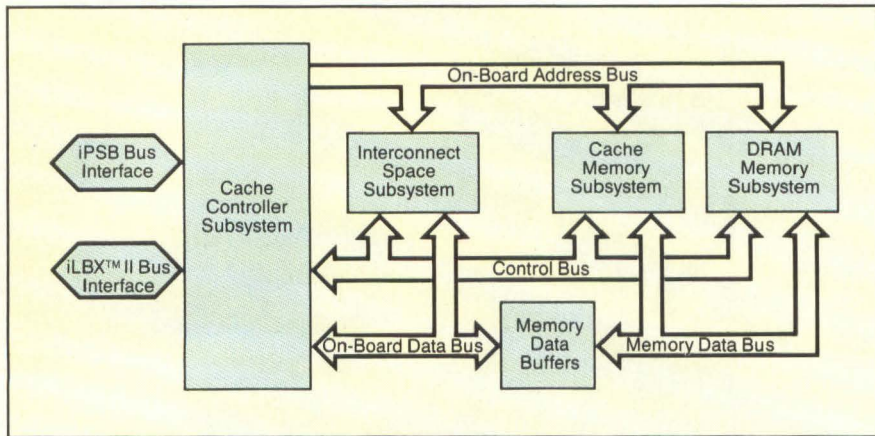
The iSBC CSM/001 Central Services Module is responsible for managing the central system functions of clock generation, power-down and reset, time out and assignment of IDs defined by the Multibus II specification. The integration of these central functions in a single module improves overall board area utilization in a multiboard system since these functions do not need to be duplicated on every board. The iSBC CSM/001 module additionally provides a time of day clock and the interface to a Multibus I link board.

To allow the iRMX 86 Operating System to work in a Multibus II environment, Intel has released an iRMX 86 Multibus II package that contains system modules that replace portions of the iRMX 86 Release 6. All the functions available in the iRMX 86 operating system are available in the iRMX 86 Multibus II operating system.

Applications in Real Address Mode are supported for the iSBC 286/100 board including support for the SCSI peripheral interface.

Obviously, now that third party board manufacturers have working products to test in their laboratories, it will not be long before more Multibus II products appear in the marketplace. Although the VME bus has a lead at the present time in the 32-bit market, the number of Multibus I board vendors that may support Intel's new bus is certain to challenge that lead very quickly.

—Wilson
Circle 239

DEPARTMENTS/Software

Prioritized Job Scheduling In Operating System Allows Multiuser Plus Real Time Use Of PDP-11

DEC offers several choices for PDP-11 operating systems: the single-user RT-11, event-driven, fixed-priority RSX-11 optimized for real-time use and RSTS round-robin fixed-slice time-sharing system. UNIX is another popular option for the PDP, offering an ideal programming environment; it is widely used for multiuser systems. There is some gap there, in which a demand of prioritized timesharing and fixed-priority for real time tasks is desirable. S & H Computer Systems (Nashville, TN) have honed their TSX-Plus operating system to respond to that combination. Version 5.1 of TSX-Plus runs on the DEC Professional 350 as well as the PDP and has enhanced support for communication options.

The heart of its ability is an Adaptive Scheduling Algorithm in which priorities are dynamically set, according to both user-specification and status of a job.

TSX-Plus allows some tasks to have fixed priorities either high or low; the state of these jobs only influences priority when in a wait-state, and two tasks of the same fixed priority are scheduled round-robin. Fixed-high-priority status is meant for real-time programs; fixed-low-priority should be assigned only to background tasks. All regular timesharing tasks fall between these two.

RSX-11 scheduling is event-driven; every task is assigned a priority from 1 to 250, and runs according to both that number and the events which determine whether it can execute (wait states). The highest priority task in memory executes until a significant event occurs, i.e., an I/O request. DEC does offer an option for round-robin scheduling on a priority range or all jobs during SysGen. Another option in RSX-11M and RSX-11M-PLUS is for a task to be made "checkpointable"
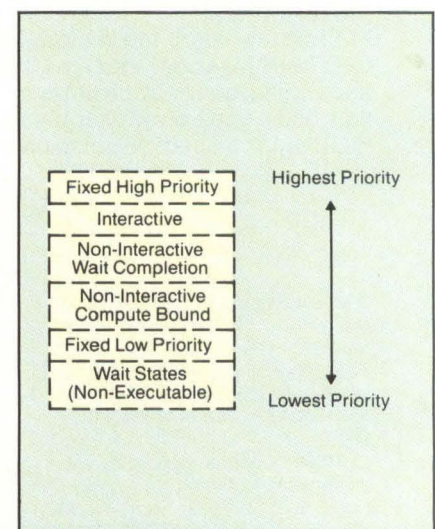
Figure 1: Five general priority levels are provided with TSX-Plus; fixed high is for real time and fixed low is for only background jobs while three are for normal timesharing prioritization.

or able to be swapped out of memory when a task of higher priority requests the partition in which it is executing.

UNIX is a timesharing operating system; tasks are assigned a priority and scheduled for execution based on how long they have executed since being swapped into memory and on the user-set bias. Here, jobs that are compute-bound have a lower priority than those waiting for I/O or recently swapped into memory.

With TSX-Plus, priorities range from 0 to 127; real time tasks are assigned fixed high-priority between 127 and a fixed PRIHI value. Background tasks are allocated from 0 to PRILOW. Normal-priority jobs between PRIHI and PRILOW are scheduled both by assigned priority and by external events affecting their state (**Figure 1**). Job state is the primary factor in the scheduling algorithm. When a task receives a character from the terminal, it is classified as interactive and remains in that state until it has either executed for a predetermined period of time (round-robin or time-slice) or performed an I/O operation (event-driven). It is then rescheduled into the interactive-CPU state, just below in priority, but still higher than any non-interactive state.

Interactive tasks that accumulate a certain number of time units (QUAN1) or perform more than a pre-set number (INTOC) of I/O operations are reclassified and put into the noninteractive compute-bound state (**Figure 2**). Jobs that are noninteractive usually execute in a noninteractive compute-bound state; as they come out of a wait state (when the resource needed is available), they go into a wait-completion state. Wait-completion is higher priority than the noninteractive-CPU state; a task remains in that state until it either executes for a set period of time (QUAN1A) or goes back into a wait state. A noninteractive job can be moved into an interactive state when it receives input from the terminal.

Scheduling in TSX-Plus occurs on the basis of priority state and user-assigned priority of jobs in memory. If the highest priority job is not in memory, the algorithm searches down the queue. Meanwhile, the job swapper must bring into memory the jobs with highest priority in an executable state. How much swapping must occur is, naturally, a product of memory size. Users may set a system parameter determining how long an executable job remains in memory. Appropriate setting of this and the other system
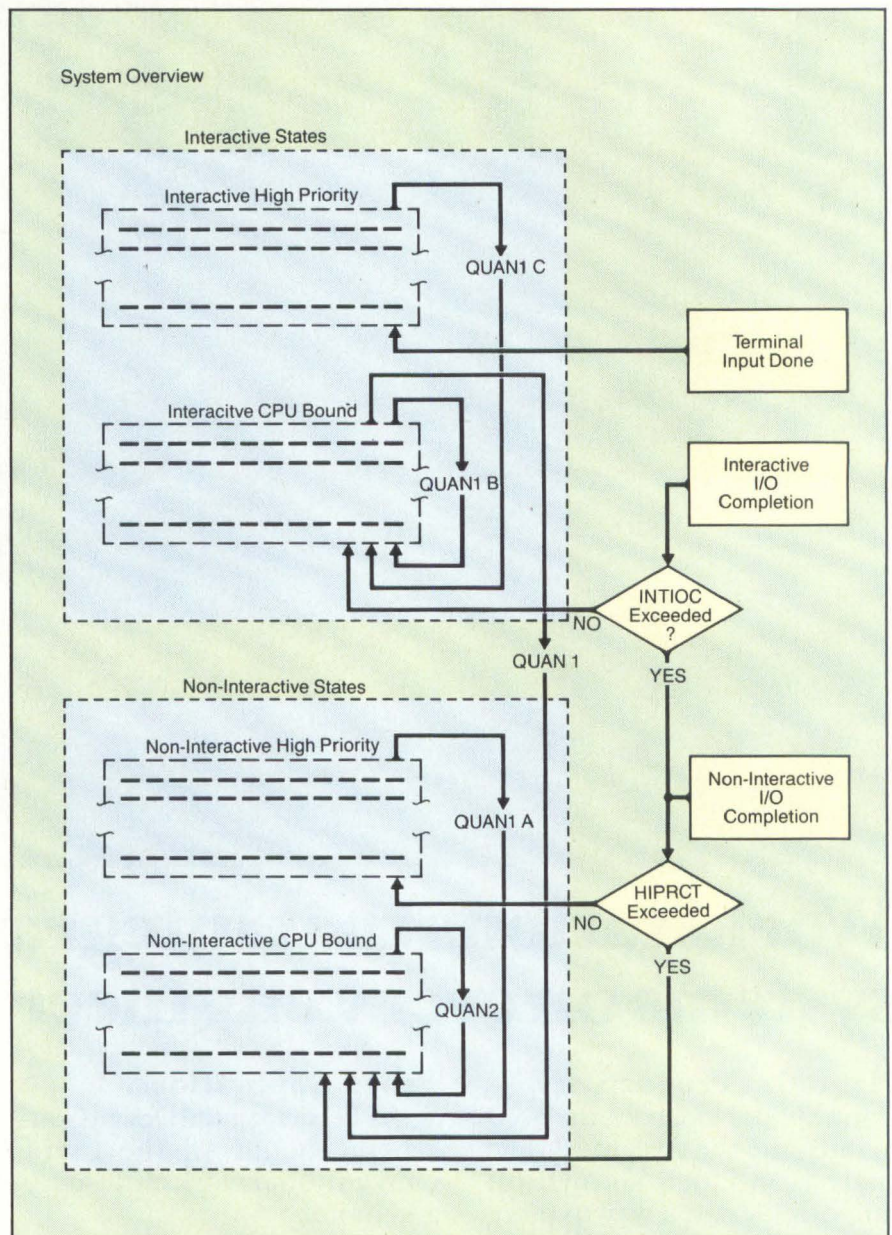
Figure 2: How time-slice parameters (QUAN) and external events reclassify state transitions of nonfixed priority jobs in TSX-Plus.

parameters regarding how long a job may execute and how many I/O operations are allowed in an interactive state are especially critical in smaller systems.

While all of this scheduling handles interactive and timeshared applications, real time applications, well addressed by DEC's RSX, are placed in fixed high-priority under TSX-Plus. As a result, tasks like process control or monitoring always have priority over all other tasks. The interactive features are similar to UNIX, for multiuser applications. In environments where most tasks are real time, RSX-11 provides more priorities (0-250) for jobs. And the universality of UNIX has advantages in familiarity as well as optimum design for programming. The combination of fixed high-priority for real time and weighted, time-shared medium-priority for interactive jobs in TSX-Plus provides one system for a range of tasks.

— Pingry
Circle 237
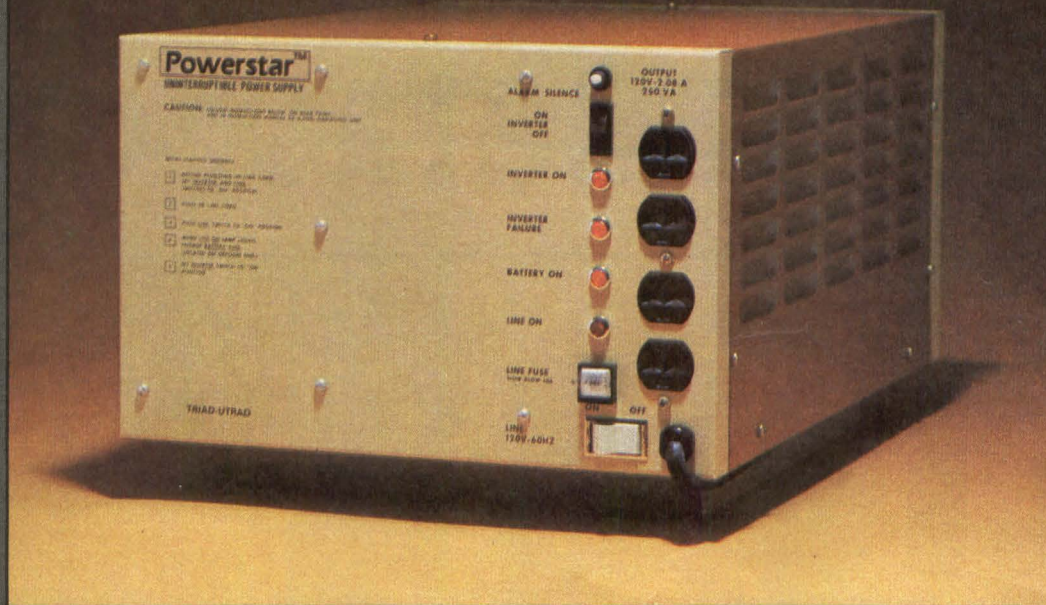
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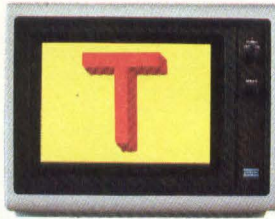
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Instead of glitches.

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CMOS

TECHNOLOGY	GATE LENGTH	PROP DELAY TIME*	GATE COUNT
STD CMOS	$3.6\,\mu$	7.0 ns	700-3900
H CMOS	$2.8\,\mu$	5.0 ns	440-3900
VH CMOS	$2.3\,\mu$	2.5 ns	2600-8000

*2-Input NAND Gate, F/O = 2

BIPOLAR

TECHNOLOGY	PROP DELAY TIME*	GATE COUNT	POWER DISSIPATION PER GATE
LSTTL	1.8 ns	500	2.3 mW
LSTTL	1.9 ns	240-1100	0.8 mW
LSTTL	0.95 ns	2000	0.65 mW

*3-Input NAND Gate, F/O = 1

TEAM ON THE CIRCUIT.

Graphics Display Controller For CAD Fits On IBM PC

As graphics demands increase, so does the burden of extensive computation from the host, which is often a microcomputer such as the IBM PC. Executing advanced programs such as CAD and solid modeling can be a slow and arduous process simply because the architecture was not intended for graphics demanding applications. A solution is the use of dedicated hardware for executing graphics intensive functions that liberate the host to do managerial chores. This is especially important for today's higher resolution multiple color graphics workstations aimed at CAD and solid modeling applications.

The pervasive IBM PC and look-alikes are becoming popular for graphics functions, not because of its computational sophistication, but the ability to act as manager for various functions. IGC (Hauppauge, NY) makes a high resolution graphics controller that mates easily with the PC for CAD/CAM-related graphics. The RGC-1040 remote graphics controller displays 1280×1024 pixels at 256 colors from a 16.3 million color palette. Through software, resolution can be changed to 25 other formats, such as 10,240×1024×1 or 1,280×8,192×1

which is excellent for CAD applications. Standard features are double buffering, overlaying and the ability to read/write and display during double buffering. The display formatter allows four independent windows to be revealed simultaneously on the display. Pixel by pixel panning is also possible, in addition to zoom, which can be incremented from one to eight times.

Graphics commands are executed from a 68000 having 128K of RAM and 128K of ROM which can be increased to 256K. The RGC-1040 utilizes four boards: a graphics processor board, a pixel memory controller board and a video controller board. The graphics processor controller board interfaces with a number of hosts having a 16-bit parallel port, two RS-232 ports, and a VAX DMA DR-1W interface. A PC interfaces with RGC-1040 with a high speed DMA interface. The data transfer avoids use of the 8088 attaining transfer rates of 170K 16-bit words/sec. The graphics processor relies on a Versabus interface for data communication between boards. The pixel memory controller board controls raster timing and control and has a high performance state machine for vec-

tor generation for solid, dashed or dotted lines. A FIFO inputs vector data while the vector generator draws the previous vector. The same board avoids memory matrix boundary problems during vector generation. The pixel data controller has the responsibility of controlling the non-vector generated data to the pixel memory board and has six modes of operation for pixel fill, screen overwrite and reading and writing of pixel data. The same board has a display formatter that controls pan, zoom, flip and split screen memory.

Panning and zooming can be time and execution intensive, however, so the RGC-1040 uses a feature of reading of raster scan technology called dynamic image memory organization (DIMO) for real time (1/30th sec) execution. This technique allows a user to organize the eight memory planes for best control and to use it as a high level command. Using DIMO, a user can store up to four images of the two page space. Each page has independent overlay planes which allows a user to look at one view while the host updates the second page and its overlay.

— *MacNicol*
Circle 236

Altera Allows Custom IC Development On PC

Development of custom ICs and PLAs can be complex and time consuming, especially when research time is included to calculate the right technology for the right function. Standard gate array development can take between 6 and 20 weeks. The cost of programming can vary between $10,000 and $40,000 and usually requires a minimum order above 1,000 parts. Altera Corp. (Santa Clara, CA) is offering a solution that is similar to the speed and ease in programming EPROMs. Using an IBM PC or look-alike as host, the Altera system can create

a logical equivalent of a TTL series circuit. Better yet, the CMOS gate array is erasable. The erasable programmable logic device (EPLD) can be programmed and, if needed, erased by an ultraviolet light. EPROMs found great success in the past because the devices could be used both for development and production. The convenience of erasure and modification allowed the ability for bugs to be worked out and new revisions to be made easily. Altera is hoping that erasable gate array technology will become as popular and convenient as EPROMs.

The $1,250 system comes with a disk, manual, plug-in card, a box with the interface to the IC and two EP300 ICs. Each IC, which sells for $17 in hundreds, is a 20-pin, 300-gate array. The EP300 is equivalent to 15 to 17 TTL ICs.

A newer version of the system is the EP1200 which has 1200 gates in a 40-pin configuration. Using the same technology, the CMOS chip dissipates 400 mW during operation and 15 mW during standby. Altera's EPLD technology allows similar speeds to bipolar TTL. The chips can run at 16 MHz having a propa-

gation speed of 35 nsec. The EP1200 is $129 in 100 unit quantities, and second sourcing by Intel is currently available.

In addition to the newer chip is software that increases programming productivity. Entry of logical functions can be in the form of Boolean constructs, a net list, state diagram entry or schematic capture programs. The new software package, called A-Plus for Altera Programmable Logic User System, allows use of all four methods of logic entry. The fastest method is schematic capture, such as FutureNet's (Canoga Park, CA) DASH-1, which costs about $6,280. This allows the ability to create, build and edit schematics for entry into the Altera system for a working custom IC in one day. The cost of A-Plus is $2,500.

Additional features of A-Plus include the ability to produce a resource utilization report which prints out the total amount of remaining logic on the chip. This is useful for optimization and chip creation telling the designer what is the best logical structure to use. A-Plus also allows partitioning specific logic elements for test purposes. The software was

The Altera Corp. Logic Programming System.

written in C providing portability. As a result, the software is now available on Daisy System's Personal Logical Workstation, and plans are being made to port the software on the VAX series and several 68000-based systems.

Software and hardware security is becoming an important issue in new IC de-velopment. The problem with EPROMs is that the code is easily read and copied. Altera EPLD devices have a security bit option which prevents the reading of a device after it has been programmed.

– MacNicol
Circle 235

DEPARTMENTS/ICs

Software Defined DSP Chips Take Expanding Role

Introduced nearly two years ago, Texas Instruments' (Dallas, TX) TMS 320 16/32-bit processor is finding increased use in many areas of the signal processing arena. Based on the unique Harvard architecture, which separates program memory from data memory, information is retrieved from both spaces simultaneously. As a result of this concurrency, the chip executes instructions at a rate of five-million instructions per second (**Figure 1**).

In a strict Harvard architecture, the program and data memory are in two separate spaces, and there is little communication, if any, between the two. In TI's implementation, however, additional hardware is implemented to transfer data between the two locations thereby allowing greater flexibility of the application software.
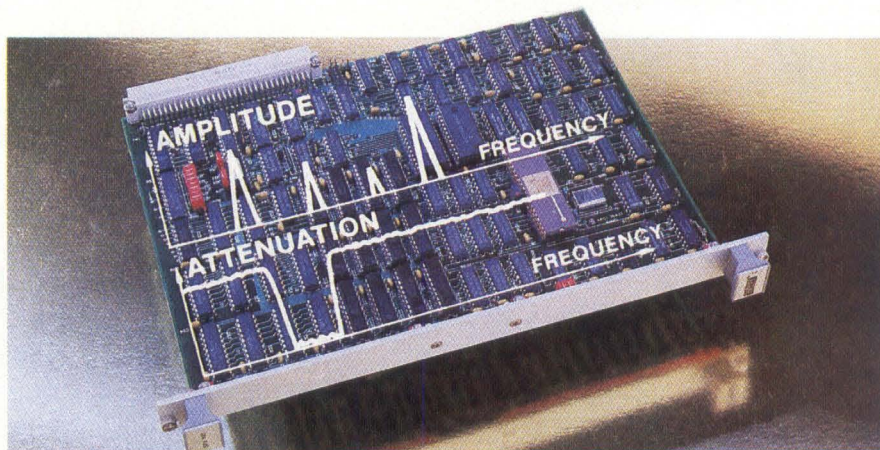
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Of the near 60 member instruction set, 90% can be executed in a single 200 nsec cycle. In additon, a 16×16 parallel multiplier residing on the TMS 320 can multiply two 16-bit numbers and produce a 32-bit result in one cycle.

Exceptional speed has pushed the TMS-320 into a recognized position in the single-chip DSP market against competitors like NEC, AMI and Intel. But with the DSP market burgeoning and the competition getting rougher, TI is not

resting on its laurels. An enhanced version of the TMS 320 that offers speeds up to 13 MIPS, a 544×16-bit RAM and multitasking capability is expected to be announced. The new chip, which is implemented in 2.4-micron NMOS, is also reported to provide single cycle multiply/accumulate instructions.

TI is not the only supplier looking to capitalize on this virtually untapped market, NEC (Natick, MA) is offering their μPD7281 Image Pipelined Processor. This new DSP chip is the first VLSI-based dataflow machine. Unlike conventional computer architectures, dataflow configurations are data-driven as opposed to instruction-driven. Both the TMS 320 and μPD7281 are designed to avoid, or at least mitigate, the von Neumann bottleneck, which can severely dampen performance. In short, dataflow architectures attempt to exploit the inherent parallelism of certain applications. (For a complete analysis of the von Neumann bottleneck and dataflow machines, see *Digital Design* Nov., Dec. 1984, CPU Architecture Series.)

The most recent product to use the TMS 320 is Burr-Brown's (Tucson, AZ) VME-based SPV100 fixed-point digital signal processing (DSP) board (**Figure 2**). The new board is targeted for applications requiring real time analysis such as advanced industrial instrumentation. Other applications include speech processing, image processing, vibration analysis and digital filtering. (The TMS 320 has probably gained the most notariety in voice recognition applications, which rely heavily on autocorrelation type algorithms.)

The difference between this board and similar competing products is that the SPV100 is software defined. This allows the product to be used in different signal processing applications by simply altering the software. Manufacturers such as DSP Systems (Anaheim, CA) and Sky Computer (Lowell, MA) offer products that resemble the SPV100, but their boards are tailored with discrete multiplier/accumulators from manufacturers like Analog Devices (Norwood, MA) and TRW (La Jolla, CA). Using such high performance hardware obviously provides maximum number-crunching speed but at a cost of decreased flexibility.

On the other hand, Burr-Brown is betting on the flexibility of their board to challenge the competition. Since the

Figure 1. The TMS 320 is based on a modified Harvard architecture that allows communication between the program memory and data memory. But since the two storage areas remain separated, both can be accessed simultaneously.
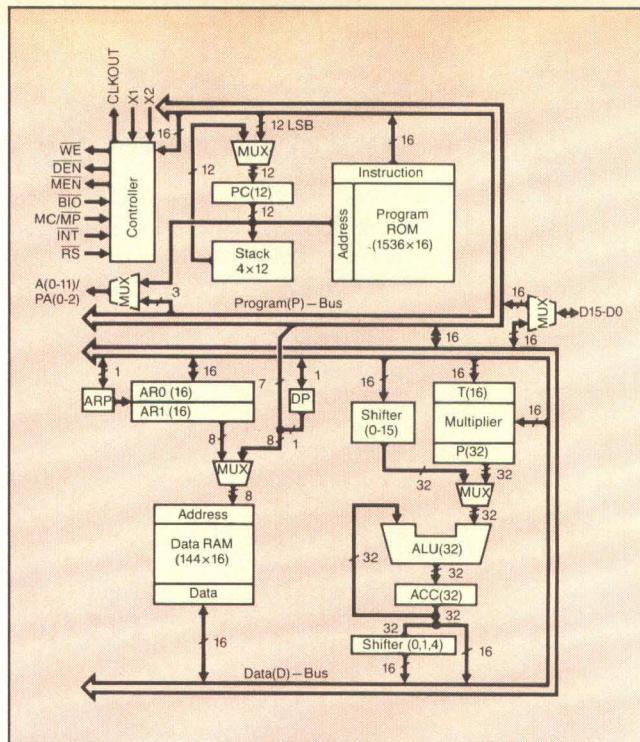
SPV100 is completely software dependent, however, functions such as FFTs will be executed at slower rates in comparison to DSP boards that utilize dedicated hardware. Although, with the help of the TMS 320 and its built-in multiplier, speed may not be such a formidable problem.

Software for the SPV100 resides in a 4K×16-bit RAM and 4K×16-bit PROM; for data storage, the board houses a dual 4K×16-bit RAM. With two banks of data RAM, the board's efficiency is further in-

creased since data held in one area can be accessed while data residing in the second bank can undergo processing.

Fourier transform software (64 pt, 256 pt, 512 pt and 1024 pt) is currently available for the SPV100. Other application programs soon to be announced include finite impulse response filtering, correlation, convolution and Levinson matrix conversion.

— Collett

Texas Instruments . . . . **Circle 232**
Burr-Brown . . . . **Circle 233**
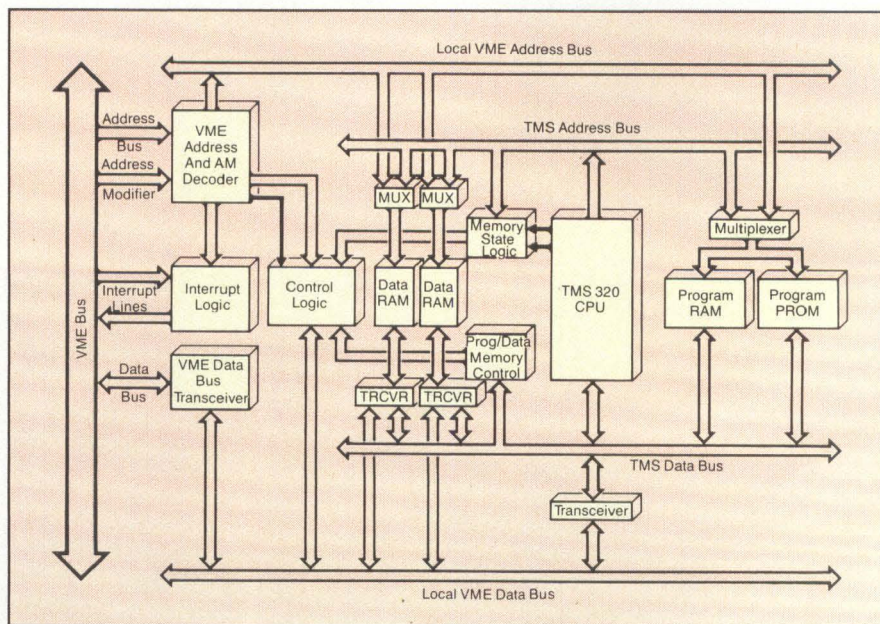
Figure 2. Burr-Brown's SPV100 DSP board uses the Harvard architecture based TMS 320 which runs at five MIPS. The new board purports to offer the most flexibility among the competition because of its complete software programmability.

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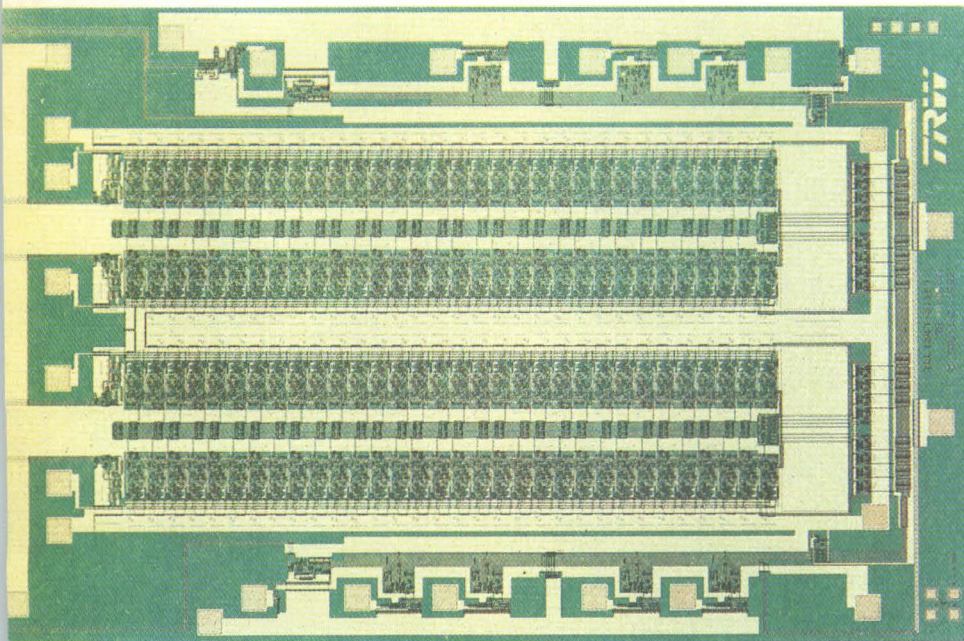
TRW's new TDC1047, a 7-bit A/D flash converter, operates at 20 megasamples per second.

Flash converters, or parallel analog-to-digital converters, have enabled systems architects to reach sampling speeds of up to 100 MHz for resolutions of 6- to 9-bits. However, they are anything but user-friendly to systems architects unfamiliar with the workings of analog parts. Their ultra-fast speeds can cause driving and timing problems which reduce the ICs performance to something far below specified sampling rate figures. Testing of flash converters, made difficult by those same speeds, also cause data sheets to present less than accurate specifications. As a result, implementing a flash converter becomes a difficult, and sometimes impossible, task.

The flash converter circuit employs 2^n-1 analog comparators to directly implement the quantizer transfer function of an A/D converter. The trip points of the comparators are spaced 1 LSB apart by the series resistor chain and voltage reference. For a given analog input, all comparators biased below the voltage turn on; those biased above it remain off. All the comparators change states simultaneously, making the quantizing process a one-step operation. The second step requires an ultra-fast decoder circuit to convert the logic output of the comparators to binary form.

Since the entire conversion takes only two steps, the flash converter is faster than either successive approximation or integrating type A/D converters. But, there are limitations to the method of parallel conversion not found in other conversion processes.

One limitation is the large number of comparators required for even moderate resolution — whereas a 4-bit converter needs 15 comparators, an 8-bit flash converter requires 255, and so on. As a result, most flash manufacturers agree that achieving resolutions of over 9-bits for true flash converters will be difficult because of size, circuit complexity, and cost considerations.

Matsushita has announced a 10-bit single stage converter; a chip, however, has yet to be seen. TRW's LSI Products (La Jolla, CA), the acknowledged leader in the flash converter marketplace, is currently developing a similar bipolar device.

Two stage flash converters, developed with digital corrective subranging, will more than likely become the primary design for high resolution ultra-high speed converters. Multiplexing two A/D converters and their outputs may attain higher sampling rates, in addition to yielding a converter of higher resolution.

Several manufacturers of flash converters have begun to design parts with this cascading trend in mind. For example, Siemens (Iselin, NJ) produces two ECL bipolar devices, the SDA 5200N and the SDA 5200S which differ only in their method of overranging. When the 5200N is overranged, the overflow bit goes high and data bits D1-D6 go low. The 5200S overranging not only sets the overflow bit high, but also leaves bits D1-D6 high. Motorola (Phoenix, AZ) also manufactures two ECL bipolar converters which behave similarily (the MC10315L and the MC10317L).

The logical classification scheme for flash converters centers on the manufacturing technology used: CMOS or bipolar. Among the companies making CMOS flash converters are RCA (Somerville, NJ) which uses the silicon-on-sapphire technique, Telmos (Sunnyvale, CA), and Micro Power Systems (Santa Clara, CA). Some manufacturers employing bipolar technology are TRW, Siemens, Motorola, Ferranti (Commack, NY) and Analog Devices (Norwood, MA).

The major difference between these two technologies is speed and power. CMOS devices specify much lower power dissipation figures, bipolar flash converters, higher sampling rate speeds. For those applications that require low power consumption and conversion rates of around 20 MHz and under, CMOS flash converters may be a good design choice. On the other hand, if power consumption is not a vital consideration for a system and the systems architect wants the highest conversion rates available (up to 100 MHz), bipolar flash converters are probably the ideal choice.

Because flash converters are so difficult to implement, all of the manufac-

turers offer applications aid to systems architects. According to the applications departments, the most common problems for architects working with flash converters are grounding and power supplies.

Since the converter is both an analog and a digital device, special care must be taken to separate and isolate the analog ground from the digital one, otherwise, digital noise interferes. Noiseless power supplies, within the power supply rail, are also critical in order for the converter to function to specfication. Clock timing is another important facet of an analog part which systems architects, now dealing primarily with digital devices, fail to consider.

With the high speeds of the flash converter, the performance and the matching of the comparators used in the conversion circuit becomes critical. Signal level variations across the comparator network may cause the converter to yield codes which indicate that more than two signals were detected at the same time. Therefore, the latch time for a comparator must be as short as possible. Also, the comparators may not receive the convert command simultaneously, causing them to latch on different portions of the changing signal.

Spec sheets are the basis for most of the complaints from converter users. There are so many parameters on the data sheets that users have a difficult time determining which values are the most important to their applications. Many specs, such as linearity, are hard to comprehend, and there are still several typical specs listed that should be absolute ones. Extended temperature range testing is also difficult for the companies to perform. However, until better testing procedures are developed for the ultra-high speed converters, those spec values will remain typical. To overcome this problem, many users have begun to do more testing and analyzation themselves on the devices.

Finally, systems architects planning to implement flash converters should remember that, in general, parts from different manufacturers are not compatible with each other. Pin compatibility, indeed even supply compatibility, is rare. Input ranges for the various flash converters vary widely; level-shifting and gaining a signal for one flash converter may not ensure its correct input into another converter. Matching two

converters for subranging purposes is difficult due to aperture time differences, and output drive capabilities also differ.

Advances in flash converter technology may help the device to break out of its niche market. Hybrid converters may ease the burden of the systems architect somewhat, and the further development of those hybrids may lead to a more user-friendly monolithic chip. But one thing is certain: At present, the flash converter is not a device for the fainthearted.

—Meng

PC Network Compatibility Promotes Versatile Systems

by Julie Pingry, Senior Editor

The huge quantity of installed personal computers has changed the way people work. But even the near-standard IBM PC does not lessen the need for shared information and facilities. Over the past several years, local area network schemes have emerged which allow the PC to provide some of the advantages of large multiuser computers as well as standalone PC functions. Now that IBM has announced a broadband PC Network, the popularity and usefulness of networked PCs will likely soar.

Sharing resources has been a major thrust behind PC networking, especially since prices of high-capacity Winchesters and laser printers can rival that of a PC. LAN connections should be more than just that, however: file sharing is an important asset of multiuser systems. On-line access to updated common information can enhance the efficiency of a group of people working on one project, and most LANs are predicted

The IBM PC AT and PC Network hardware: Sytek supplies the adapter card and IBM is a licensee of Sytek's LocalNet/PC protocols.

to connect departments of under 50 nodes.

Most networks for PCs use a rigid disk subsystem as a disk server, with software for file server functions residing in the PC to which the disk is attached. At present, few file servers are configured in the disk subsystem. But with the introduction of the Sytek-developed PC Network from IBM (Boca Raton, FL) and Sytek (Santa Clara, CA) as well as MS-Network protocols from Microsoft (Bellevue, WA), it may pay to put file server protocols in firmware in disk subsystems.

IBM's well-supported network scheme will likely spawn activity similar to the crush after the introduction of the IBM PC itself. Application programs to run across the network, gateways into other networks, file, print and communication server software and subsystems will probably appear from many sources.

The IBM PC Network

Though there are many personal computer networking companies and schemes, it is a good guess that all of these will provide gateways to or compatibility with the broadband IBM system. A brief overview of the IBM PC Network should help in clarifying the distance other PC LAN suppliers will have to go to remain IBM compatible.

The IBM PC Network (**Figure 1**) connects IBM (or compatible) personal computers running PC DOS 3.1, to be released soon. A Network Adapter board for the PC, AT, XT or Portable slots into every computer to be attached to the net. NETBIOS (Network Basic Input/Output System) ROM on this Adapter implements the Network, Transport and Session layers of software protocol (see *Digital Design*, January 1985 for description of the seven layers of OSI networking protocols). Each network, regardless of size, needs one Translator Unit, or broad-

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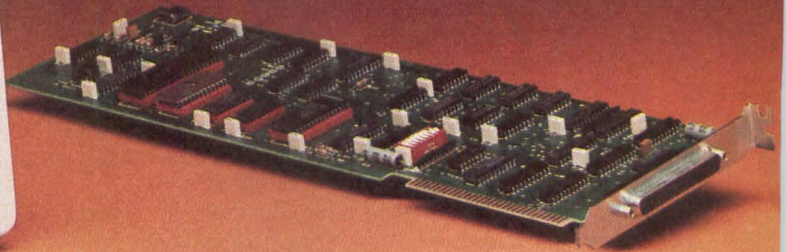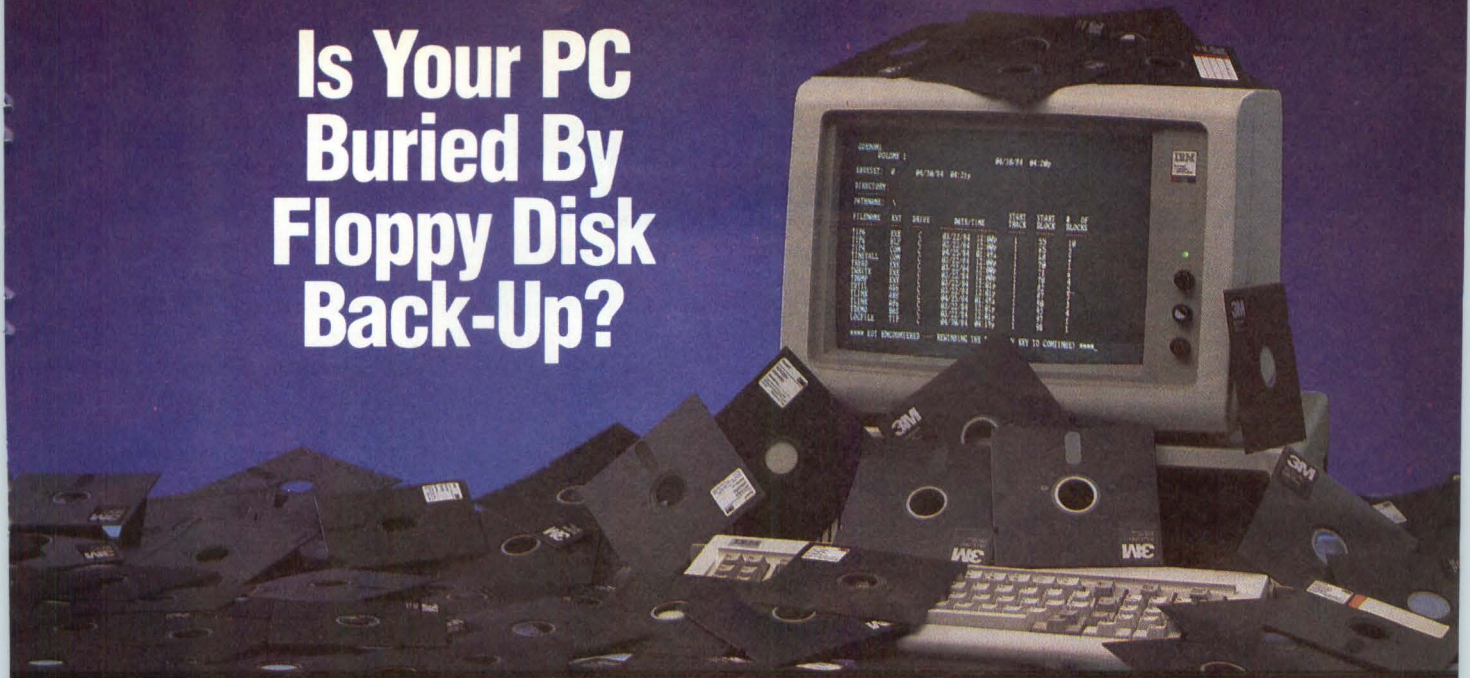
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band headend, with connection hardware and broadband cable to interconnect network nodes (PCs) to the Translator Unit.

Debates over the virtues of broadband versus baseband technology have been overshadowed by other issues. However, there are significant differences. Broadband systems are analog, and though tweaking and high costs are common in analog systems, the volume of broadband equipment used in the cable TV industry has produced reliable, cost-effective products. Digital baseband also uses coaxial cable, and the cable specified for Ethernet is relatively expensive.

Few PC networks have used broadband; IBM purchased the technology from Sytek. According to Greg Ennis of Sytek, IBM chose broadband technology because the medium allows longer cable links than baseband, offering the potential for larger area connection. In addition, broadband cable can support many separate services simultaneously, so there is an installed base, and firms can view it as a utility, rather than an expense incurred in conjunction with one product. IBM's translator, however, provides only one channel. So although the technology has the potential for many signals or combined channels for a high speed signal, the IBM PC Network *per se* does not.

The Network Adapter board design (**Figure 2**) offloads the PC processor of most communication processing. Its Host Interface Controller (HIC) and TTL bus receivers make the board look like an array of I/O spaces to the PC. An Intel 82586 CSMA/CD LAN controller chip and Sytek Serial Interface Controller (SIC) together interface to the on-board RF modem and network. NETBIOS resides in an 8K × 8 ROM; other memory is used to store a permanent ID, Adapter for program and protocol information, and 16K × 8 of RAM is used for data. Significantly, the board also uses the Intel 80188 microprocessor, so the card is a powerful networking front-end.

Since the system uses logical layers (as most networking schemes do), software may be more critical for interoperability than the hardware. NETBIOS and the basic protocol architectures, in particular the uppermost Session protocol, will be critical; IBM has proclaimed that NETBIOS will be the interface to all of their networking systems.

Protocols included in the BIOS on the IBM Adapter, according to the ISO's OSI model, are levels 3 through 5. For Network (3), the Packet Transfer Protocol (PTP) provides simple transfer services including routing and address location. It is used by the Transport (4) level protocols, for both virtual error-free connection, called Reliable Stream (RSP), and unacknowledged Datagram (DTP) transmission. These, in turn, are used by the Session layer, a network protocol level that has often been missing or partially implemented.

IBM's Session (5) level includes Session Management to allow users to connect to a name or named process; this uses the RSP. User Datagram Protocol (UDP) makes use of DTP for best-effort datagram delivery to an alias or named process. This level also includes Name Management (NMP) for linking alias names to network addresses and translating remote names to network addresses, and Diagnostic and Monitoring (DMP). All commands between DOS and NETBIOS take a standard form, the Network Control Block (NCB).

NETBIOS actually sits beneath PC DOS 3.1, so although the common BIOS seems intended for compatible software building, either may be the base for applications. The IBM PC Network Program interface to DOS uses Interrupt 21, (INT 21H), INT 2FH and INT 2AH. The sections of particular interest for multiuser applications are INT 21H 3D, or an extended open where specified access (read, write or read/write) or sharing mode (defining the type of I/O other processes can do to a file, namely, compatibility, deny read/write, deny write, deny read or deny none) can be chosen and 5D for physically locking and unlocking files.

To assure that these locks do not adversely affect network access, both IBM and Microsoft protocols require all locks (under 5D) to be unlocked before a file is closed. IBM's concurrent file server software uses a utility to close and unlock files. Under Microsoft's protocols, closing a locked file is not allowed, but there is no similar server utility to prevent the condition.

Some of the interesting features of the IBM PC Network are that each adapter can maintain 16 simultaneous two-way sessions and be addressed with 16 user-assigned names. Inclusion of name management at every node is also important; many systems centralize this function. Especially with the popularity and power of the AT, provision for multiuser nodes is important. The layering of the protocols allows them to be used with other operating systems and network architectures as well. In addition, the built-in NETBIOS programming interface allows application programs to be smaller.

Sytek claims that at the 2 Mbit/sec line speed, the protocol functionality on the adapter card allows application-to-application throughput in excess of 600 Kbits/sec. This is a notable improvement over the 150 Kbits/sec throughput if protocols run within the PC itself. In fact, 600 Kbits/sec rivals the throughput of many Ethernet systems with a 10 Mbit/sec line speed. In reality, the line speed has less effect on throughput between applications than installation and software design.

Sytek is licensing their LocalNet Protocols, on which the IBM Network is built, for $5,000 per specification package. System components from IBM are not expensive: the Network Adapter card is $695, and the Network Translator Unit is $595. Cable extension kits for more than eight users on the network are also available.

Other PC LANs

Several companies have already made inroads into the market for networking personal computers. Though compatibility with the IBM scheme will be a critical factor in their survival, many existing LANs will survive intact. During the next six months
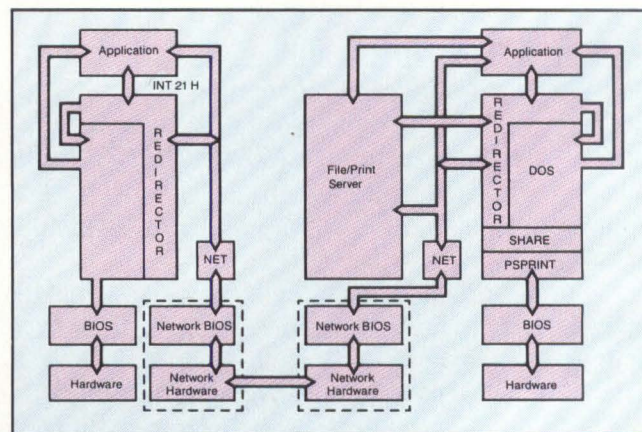
Figure 1: Block diagram of the IBM PC Network, with a server on the right and a workstation node on the left; all disk I/O requests go through DOS.

Alloy. We b

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QICSTOR-PLUS, PC-DISC, PC-BACKUP, PC-CARD, and PC-9 TRA(

ackup IBM.

to a year, these firms will scramble to achieve NETBIOS and PC DOS 3.1 compatibility or internetwork gateways.

Availability of the protocol license from Sytek will be key; with a copy of what resides in the NETBIOS of the IBM adapter, some software developers will not need to go to the operating system. The Microsoft protocols could also play an important role; these have been developed in conjunction with Intel, and are operating system and hardware independent. They are designed to provide application-level compatibility with the IBM PC Network for networking companies and software developers.

The MS offering is not, however, identical to IBM's protocols. These differences limit communications compatibility between MS and PC protocols. Microsoft needs to implement some form of lower level network protocols because many of the network systems they are targeting for sales do not have all of the protocol levels implemented in NETBIOS. The IBM Redirector is Microsoft's design, but server software is not the same.

Both MS and PC Network software treat the file/print server as an application and provide separate redirector software for the server node in addition to the redirector and utilities for each node. Unlike IBM's protocols, the MS-Net File/Print server does not allow concurrent applications. This can be a drawback in relatively slow server functions like backing up data or printing. IBM also offers a high level interface through DOS to the NETBIOS uppermost (Session) layer.

Microsoft will probably purchase a license to make their protocols fully IBM-compatible. But meanwhile, MS-NET is allowing many PC LAN vendors to keep up. Some of the companies who announced MS-Networks before the end of 1984 are: Corvus Systems (San Jose, CA), Proteon (Natick, MA), 3Com (Mountain View, CA), Orchid Technology (Fremont, CA), Davong Systems (Sunnyvale, CA), Nestar Systems (Palo Alto, CA), Ungermann-Bass (Santa Clara, CA), Interlan (Westford, MA) and Western Digital (Irvine, CA). This list includes some of the leading firms in the networking business; some, but not all, focus on only personal computers.

Many of these firms' systems have characteristics that might be advantageous. 3Com, for example, uses Ethernet. By adhering to this international standard, the system is compatible with standard networks of other types of equipment. Another leading PC LAN company is Novell (Orem, UT); though their system operates on twisted pair, it uses a proprietary network operating system efficient enough to make throughput speed exceptional. Corvus and Xcomp (San Diego, CA) also operate over low cost twisted pair. Multivendor PC networking, including Apple and others, is another potential bonus of Corvus' Omninet.

For PCs and other machines, Proteon uses a token-passing scheme, now recognized as a performance boost for applications requiring assured access to a line. Nestar has long hit the high-end of the PC network market with token-passing PLAN products aimed at 50 or more user nodes per network. The MIL-1553 bus is used for Standard Data's (Pompano Beach, FL) network, which can also hook up S-100 bus machines.

Large OEM agreements like 3Com's with Xerox and Ungermann-Bass' with GE should keep some PC networking firms strong. Installed base may help some of these companies through familiarity and the need for network expansion. And should a customer turn coat and go to IBM, most systems will be compatible.

As for software, Software Connections (Santa Clara, CA) has
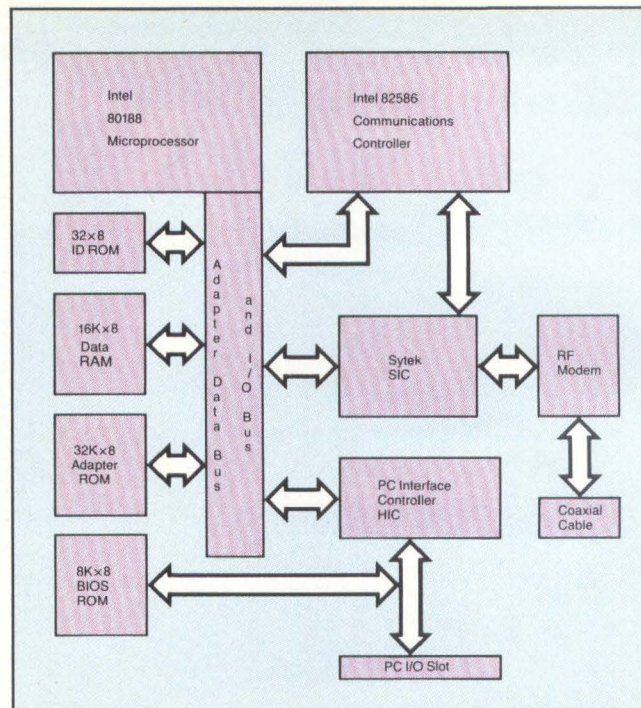
Figure 2: The IBM PC Network Adapter includes an 80188 microprocessor RAM, ROM and standard Ethernet-compatible 82586, in addition to the RF modem, host (HIC) and serial (SIC) interface control circuitry.

already declared support of the IBM dictates. Look for companies like Micro Data Base Systems (MDBS) (Lafayette, IN) and others to bring out products this year, as well. Now that there is a standard interface to PC networks, multitasking applications will be far less risky.

Because IBM's PC DOS was not designed for multitasking, many networking schemes have used semaphores to allow file locking and shared data. Several dozen application packages have been written for the more popular of the PC networks that use this type of logical file locking. Now that IBM is providing physical locking in DOS 3.1, more elegant forms will be possible.

Disk/File Servers

In addition to the software and hardware changes needed to communicate effectively between PCs, file, print and communication servers are critical. Currently, most servers available for PC networks consist of software to run in a PC (preferably the AT for all but the smallest networks) plus a hard disk or subsystem. The IBM scheme also uses one PC as both server and node.

Nearly all networking companies offer servers for their systems. As communication companies, however, most are not using terribly innovative or high-performance disk systems. Those firms offering very low cost networks may even provide software for a standard PC AT, with no additional disk storage. For larger networks, disks as large as several hundred Mbytes may be used. Many PC networks allow each node to request space on the shared disk with inadequate management.

The people at Novell feel their file server will help them compete. They define a file server as one in which the server itself manages the shared disk and one in which the individual PC nodes on the network manage access to the disk as a disk server.

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Intel Introduces VLSI Controller Specifically For PC LANs

At the lower bit rates of networks designed for PCs, a single chip can now provide the physical and data link level control that requires three chips (one not yet available) in higher-speed LAN controllers. The 82588 from Intel (Santa Clara, CA) in a 28-pin DIP includes a programmable CSMA/CD controller, Manchester or NRZI encoder/decoder and collision detection logic for networks operating at 1-2 Mbits/sec.

Like Intel's 82586 LAN processor chip for 10 Mbps Ethernet or Cheapernet systems, the 82588 is programmable. In this case, the options are designed for control of the two network schemes backed by the giants: IBM PC Network and StarLAN proposed by AT&T. For the IBM/Sytek "optimized broadband" network, the chip supports 2 Mbps NRZI encoding/decoding and SDLC framing. For a baseband system like StarLAN, 1 Mbps Manchester code and end-of-carrier framing can be selected. Other programmable parameters include slot time (or worst case turn-around time) for different distances, address length, interframe spacing and station priority.

Two modes of collision detection are supported to lessen chances of undetected transmission problems. Code violation checks incoming bits for adherence to NRZI or Manchester code schemes. Bit comparison is a signature analysis: a node listens to the signals it transmits on the receive channel and checks them for a match. The latter method is particularly useful for systems with separate transmit and receive channels, like the IBM and StarLAN systems.

A feature of the 588 used before in the 586 is buffer chaining. So that short frames do not waste the rest of large storage spaces, buffers are short (100 bytes). Longer frames are stored in several buffers linked together. The 586 links buffers automatically, but in systems using the 588, the CPU must specify the buffer start address. Still, making the most of buffer space is critical for PC systems with limited memory.

Both high-level software commands and direct hardware interface to Intel 80188 or 80186 microprocessors ease interface to the chip . No low-level driver software must be written; the CPU invokes high-level commands such as Transmit, Configure and Diagnose directly. A 16 byte FIFO provides efficient use of bus bandwidth, and no wait state operation is possible on an 8 MHz bus.

The FIFO and data link controller silicon is a direct duplicate of the older 82586. Both chips are HMOS, and experience with the 586 allowed relatively easy design of the IC. Allowances for various types of networks as well as direct interface to popular processors (Sytek/IBM boards use the 80188 and 82586 now) should provide designers with good entry into LAN board design. Other target applications include serial backplanes.

A similar single chip for the physical and link layers of the Corvus Omninet should appear within the year. Late in 1984, NEC and Corvus announced that such an IC is in development. In that case, the controller will likely be Omninet-specific.

Circle 300

In a system based on the 80188, the 82588 requires no TTL to interface to the processor.

Figure 3: U.S. Design's CSS-800 Winchester disk subsystem has many features useful for good performance on a network.

In addition to server disk control, Novell's network operating system includes file server functions, rather than running file management as an application on top of DOS. The operating system has further been written for multitasking, allowing concurrent operations in the server.

In a recent announcement, 3Com has introduced a multifunction server, called 3Server. This 80186-based engine is dedicated to file, print and communication server functions. No keyboard, monitor or floppy disk drives are used, which could be an advantage in both cost and reliability of the system. It does include a 36 Mbyte Winchester, 60 Mbyte backup tape, 512K RAM, print server for either parallel or serial ports and remote mail and terminal emulation. Up to six additional 36-Mbyte disks as well as 384K for additional cache and port expanders can be added. The initial price for the 3Server is $7,495.

Some disk subsystem companies are also attacking the server market. As long as IBM and other leading networks put server software in a PC, separate vendors for drives and networks may be common. Many drives offer only relatively good performance and capacity. But as networks grow and complex database and transaction processing software is adapted for networks, better performance and capacity will be expected.

Perhaps the most important storage subsystem feature for network performance is cache. If sufficient cache for several full tracks is available, every node requesting a disk read can expect relatively fast access to consecutive data. Emulex (Costa Mesa, CA), Priam (San Jose, CA) and other major disk subsystem manufacturers provide cache as well as built-in backup.

To increase performance further, optimized (or elevator) seeking may be used. With several requests present at the server simultaneously, each requested sector or track can be read as the head passes that area. This speeds track seek, the major component of disk access time. A leader in this field is U.S. Design (Lanham, MD); they also offer cache with management **(Figure 3)** and features like dynamic relocation, so the most commonly used data is where access will be fastest.

Data interleaving on the disk is a common feature of products claiming to be in the server market. With this scheme, logically contiguous records are not physically contiguous on the disk, but intermixed with sectors of other files, so data is not received faster than the controller and system can buffer and use it. Interleaving can reduce head movement when requests from several controllers or for different files are received at about the same time. Though this can provide some speed advantages, they are not as great as those cache can afford.

Access speed is one major network performance factor; another is backup. Built-in tape systems are almost essential to shared disks. Disk subsystem companies concentrating on good backup include Racet (Orange, CA) and Emulex. Using commands in the SCSI bus interface, Emulex's subsystems can copy disk to tape without host intervention.

U.S. Design uses two controllers, one for the tape and one for the disk, so that backing up data does not affect disk performance or tie up the network. Since streamers are a disk dump type of backup, they can waste valuable line time if not managed correctly. File server utilities can allow selective backup even with streaming drives. Tallgrass (Overland Park, KS) uses a start-stop tape that, though slow, emulates floppy backup.

Many of the performance features of network disk server systems are those common in single-user systems as well. Sunol Systems (Pleasanton, CA) touts run length limited coding (RLLC) in their 'Universal Networking Mass Storage Systems'. Each flux transition (or magnetized physical area) of an RLL encoded disk represents more data than the same area encoded with standard FM or MFM methods. Major drive companies also provide defect mapping, so the drive appears error-free to the host. This improves reliability and speeds handling of problems. Ongoing mapping can be an even more important feature: as a disk deteriorates, all problems, new and original, can be avoided.

The main features to look for in systems for networking are cache, access speed, backup and reliability. At some point, the limits of the standard PC as a server will provide further impetus for dedicated server boxes. Though IBM doesn't offer this, large networks can benefit from sophisticated subsystems now.

Effective PC Networks

Now that IBM has specified a networking system for its PCs, there is a *de facto* standard; this lends credibility to PC networking as well as impetus for a broad range of product developments. But as with all areas of IBM compatibility, it may not be as easy as plug-and-play.

Certainly OEMs of networks and systems will be digging into the BIOS, DOS 3.1, Microsoft and Sytek specifications to become compatible. Already, the differences between the IBM and Microsoft protocols are apparent; as more work is done, as much incompatibility as compatibility may be fostered.

Once internetworking is accomplished, users will likely need greater capability in servers. Dedicated server nodes with very high performance from both hardware and software will be required. Servers for concurrent printer, disk and backup access should find markets as well.

With silicon like the Intel 82588 for the IBM PC network already available, developing compatible hardware products within market windows will be somewhat eased. Software compatibility is more critical, and until Microsoft and IBM are compatible, probably much more difficult. **DD**

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Somewhat Useful 603

Magnetic Tape: Filling The Secondary Storage Gap

by Bob Hirshon, Contributing Editor

For magnetic tape, a technology generally considered stodgy and unchanging, these are tumultuous times. From low end to high end, the tape industry is undergoing unprecedented activity.

Not that the basic technology is undergoing dramatic change; in fact, magnetic tape technology hasn't changed substantially in decades. But the computer industry overall has changed. Today the industry demands removable secondary mass storage for systems using fixed disks for primary mass storage. The increase in capacity of those disks demands a secondary storage system using media with high capacity and low cost per Mbyte. And of course, the more widely interchangeable the media is, in terms of both physical configuration and data format, the better systems designers feel about specifying it.

In addition to these overall industry demands, another force is shaping the future of tape drives: the increasing acceptance of standard I/O interfaces, such as IPI and SCSI. These intelligent interfaces could make the difficult task of selecting and integrating a tape drive a simple matter of plug and play.

Standards Pros And Cons

Standardization is both a blessing and a curse for the magnetic tape industry. When competing tape drive manufacturers agree on a common media and format, the industry is assured of sufficient supplies of media from multiple sources and interchangeability of media between

Figure 1: Magnetic tape offers the twin advantages of mature technology and lower cost per Mbyte. Here, an engineer tests high density tape at 3M's new Sagamihara, Japan facility.

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systems. When drive manufacturers settle on interface standards, it helps strengthen the tape industry overall by providing systems integrators with multiple sources of compatible drives. Without cooperation—at least at the data format level—magnetic tape could not command a leading position in secondary memory storage.

On the other hand, standardization stifles innovation. While tape drive manufacturers are free to add bells and whistles to their products, they are handcuffed to the basic drive standards. "Standardization . . . does not allow you to take

quantum leaps in technology," says Larry Hemmerich, Vice President and General Manager of Cipher Data Products (San Diego, CA). "Disk manufacturers can put in thin film heads, and they can put in plated media and they put a box around it and the user doesn't care," he explains. "But when you are dealing with interchangeable and removable media, then you can't go out and violate everybody's libraries and software distribution methods. That's why the disk industry is able to revolutionize markets, while the secondary storage market has to go through the evolutionary stage."

For systems integrators designing secondary storage subsystems, the major question will not be "Should I include tape drives" but rather "Which tape drives should I include?"

The Primary And Secondary Storage Gap

The difference between revolutionary and evolutionary product development has created a serious gap between primary and secondary storage devices. Rapid advances in rigid disk performance and capacity have outstripped slowly evolving tape drive technology.

At the low end, the solution has been to incorporate secondary storage solutions originally intended for high performance systems into small systems. Consequently, quarter-inch cartridge drives, originally intended for minicomputers, find increasing use with small computers. And in some applications, half-inch, high performance tape drives originally designed for supermini and mainfame computer applications have been adapted for use in minicomputer, and even personal computer systems.

At the high end, systems architects have had little choice but to remain compatible with existing standards and wait for the next generation of drives from IBM, the traditional pacesetter for half-inch tape products. Designers working with systems that don't demand broad interchangeability of media and that can accept a lower data transfer rate have the option of selecting one of several high performance, but nonstandard half-inch cartridge tape drives. These are offered by Rosscomp and Megatape, with another, called CompacTape, being developed by Digital Equipment Corp. working in cooperation with 3M. Lower performance half-inch cartridge drives are offered by Tandon and Electronic Processors Inc. (second-sourced by Memorex).

Waiting For IBM

Those choosing to remain compatible with industry standards have had to be patient. For years, designers in both the IBM plug-compatible market and the OEM market waited for IBM to introduce an upgrade to their eleven-year old 3420 drives, which have been overmatched by the Winchester drives they were meant to support.

Last spring, IBM ended the wait by introducing their 3480 half-inch cartridge tape drive. The 3480 drives use a $4'' \times 5''$ tape cartridge, chromium oxide tape and thin film heads. A recording density of 38 Kbits/inch, and a parallel, 18-track format provide 200 Mbytes of storage per cartridge. Tape speed is 79"/sec, and operation may be in either streaming or start/stop mode. Data transfer rate is up to 3 Mbytes/sec, streaming. To keep the drive streaming, there is a 512 Kbyte cache memory in the controller.

However, although IBM ended one long wait—the wait to see what basic configuration they would choose for the next generation tape drives—a whole new wait has just begun. This is the wait for the specifics of IBM's drive, the wait for actual products designed around the basic technology and the wait for adjunct products extending the basic technology to other areas. Most important among these is a lower-cost serial-recording tape drive suitable for OEM applications, to augment the original parallel-recording drive.

Half-Inch Serial Standards

Specifications for IBM's cartridge are scheduled to be released to ANSI this quarter. This will allow drive manufacturers to build mechanical drives based around the cartridge. But release of IBM's parallel recording format for the cartridge is still in the indefinite future, and as far as any serial recording format is concerned, there is no indication that IBM is even working in the area.

Consequently, tape drive manufacturers are taking matters into their own
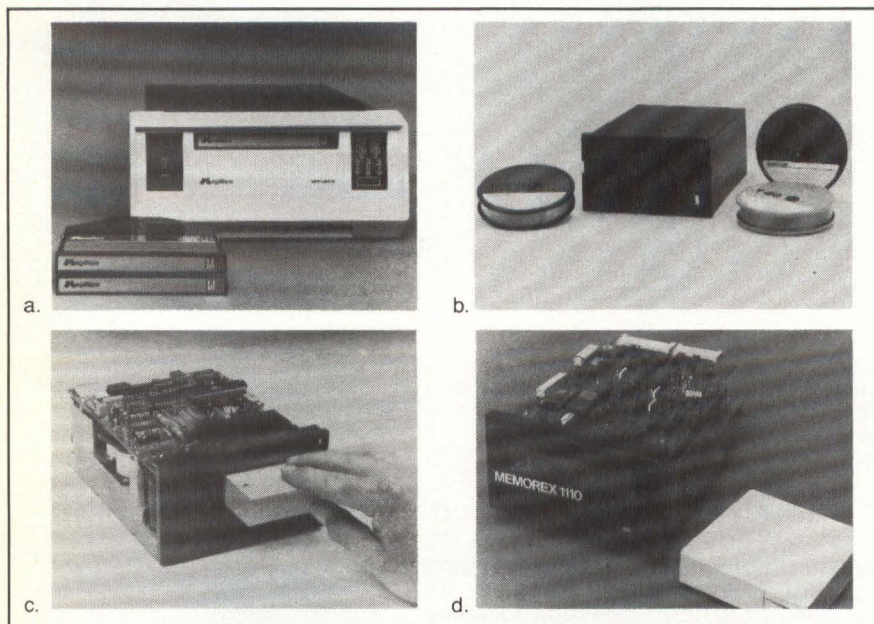
Figure 2: In addition to drives not yet in production by DEC and IBM, four companies offer half-inch cartridge tape products. Megatape's new MT-500 stores up to 500 Mbytes on a single, book-sized cartridge (a). Rosscomp's Series 50 (b) fits into a standard 5¼" Winchester footprint and stores up to 190 Mbytes. Tandon's TM951 (c) also fits the 5¼" Winchester footprint and stores 50 Mbytes. Developed by Electronic Processors Inc. and second sourced by Memorex and Fujitsu, the 1110 (d) has a capacity of 130 Mbytes, operates in streaming or start/stop modes and uses an ESDI interface.

Introducing
the little backup with the
20 megabyte appetite.
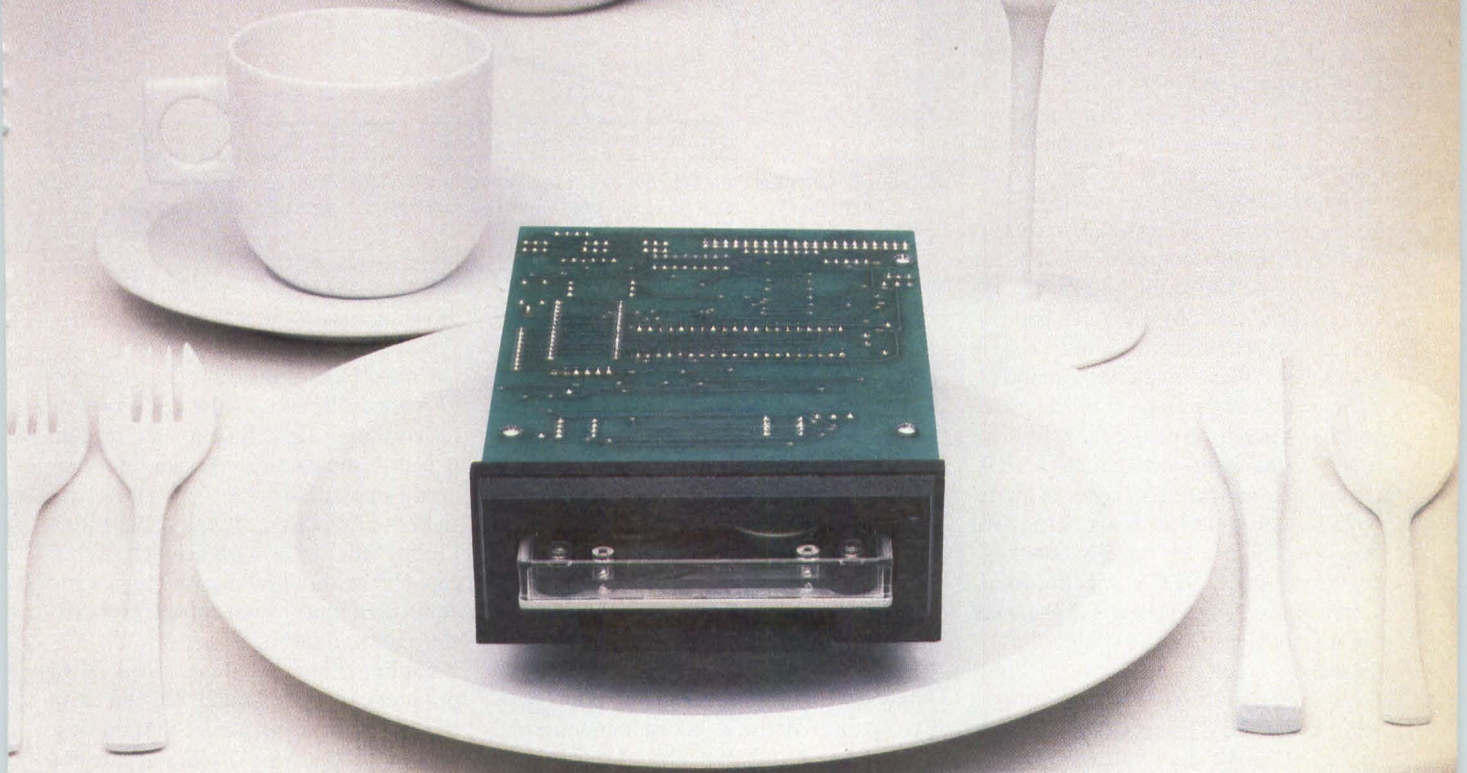
When Irwin came out with the Irwin 110 and 210 tape drives, both of which fit 10 megabytes of formatted capacity in a DC-1000™ cartridge, a lot of people said we bit off more than we could chew.

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Now we're backing you up with the Irwin 125 tape drive—20 megabytes of formatted data on a DC-1000 cartridge.

The Irwin Recipe: Simplicity, Reliability, and Ease of Use.

Because the Irwin 125 has a standard minifloppy interface, it daisy chains right onto your existing controller — without any additional cables, controllers or hardware. Add a simple software driver and an applications program for file transfer or streaming, and the Irwin 125 is ready to go.

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If we've whetted your appetite, perhaps it's time you ordered a 125 tape drive for evaluation.

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hands, setting up a committee to develop first a serial format and then interface standards for drives using the 3480 cartridge. This committee, called the Half-Inch/Tape Cartridge (HI/TC, pronounced "High Tech") committee was organized by Ray Freeman, Freeman Associates (Santa Barbara, CA), an industry consultant who performed a similar role in the formation of a standards committee called QIC for quarter-inch tape cartridge drives. The committee so far includes Kennedy, Pertec, Wangtek, Xebec and Computer Periperals Inc. (a subsidiary of Control Data Corp.) as members and numerous other companies as observers.

Notably, three of these companies — Kennedy, Pertec and Wangtek — have already purchased licenses from DEC for the DEC/3M CompacTape and are working with DEC and 3M to develop that format as well. However, although DEC is working to make CompacTape an industry standard and, in fact, submitted a proposal to ANSI long before the release of IBM's 3480, many companies believe DEC's tape standard will serve primarily DEC computer systems. This still makes it a significant format, considering the size of the DEC-compatible marketplace. Kennedy, Pertec and Wangtek see no conflict in working on both formats concurrently.

One tape drive manufacturer working with neither HI/TC nor CompacTape is Cipher. They have a joint development agreement with IBM to develop tape drives using the 3480 cartridge; therefore, they are obliged to wait for IBM to introduce a format. "We do not believe we can put ourselves in a position of compromise," explains Hemmerich. He believes that tape drive manufacturers who try to develop a format independent of IBM may be taking a risk. "Let's assume those companies all get together, and they say 'we're going to come out with a format' and then, four months later, IBM says 'this is what we're going to use.' They're either going to have to have a secondary format that's IBM-compatible, or drop what they're doing."

Freeman believes the risk is minimal since any announcements from IBM concerning format, at least in the near term, will be for parallel recording. "A parallel format would imply a plug-compatible product with the IBM 3480, and that's very large and very expensive, and it's not the kind of product that OEM tape drive
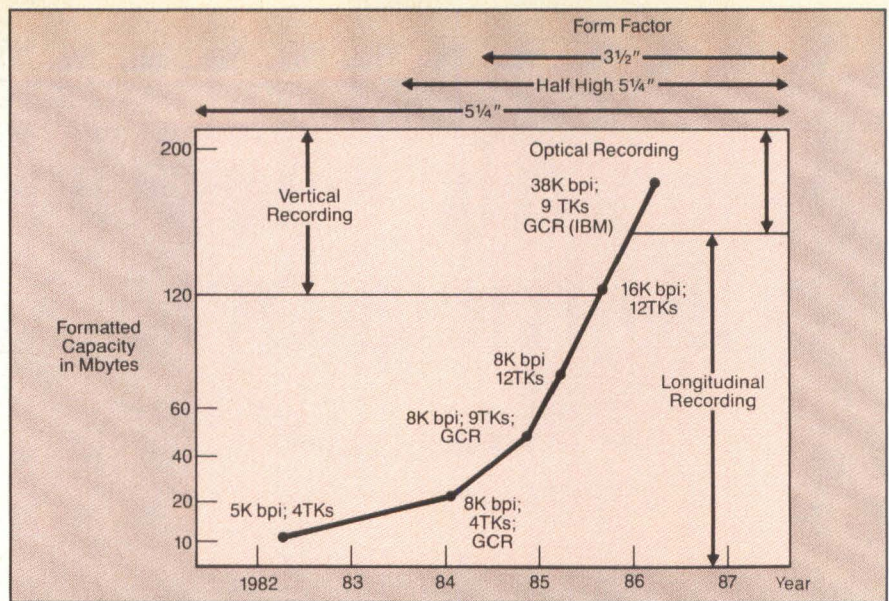
Figure 3: Although critics claim that cassette drives are limited by low capacity, Memtec, a maker of digital cassette drives, has a different view. They predict that cassettes will be capable of storing over 120 Mbytes by next year.

buyers are looking for," says Freeman. "Serial recording would imply. . .a more compact, lower cost product."

Hemmerich, however, doesn't think IBM will allow standards to become established without them. "I believe their (IBM's) intent is to steer the marketplace," he explains. "Therefore, I do not believe that they will allow it (the HI/TC effort) to get so far that it's going to damage the marketplace as opposed to building a new standard."

There is also a possibility that IBM may wait to see how the HI/TC effort develops and choose to incorporate some or all of the HI/TC specification themselves.

3M Cartridge Media Drives

While IBM sets the pace for half-inch tape products, no one company dominates the quarter-inch cartridge market. In this market most of the key companies worked together in the Quarter Inch Cartridge (QIC) Working Group to develop standards for streaming tape drives. The result was the QIC-02, a parallel interface between the streaming controller and an intelligent streaming cartridge drive; the QIC-24, a recording format for data on the cartridge; and the QIC-36, a basic drive interface for reading and writing of data and error detection and correction. In addition, the group developed another basic drive interface — QIC-44 — which Tandberg Data and their second source partner Data Electronics Inc. use rather than QIC-36. Recently QIC announced the high capacity QIC-50 recording format and a QIC-59 basic

drive interface, which allow capacities of 120 Mbytes.

Cipher Data offers a low cost, low performance alternative to the QIC formats called FloppyTape. It simulates the data structure and physical interface of a standard floppy disk drive. This allows designers to replace a floppy drive with a FloppyTape drive with a much higher capacity without having to change the controller. Only minor software modifications are required.

Cipher offers the drive as an OEM product called the model 526 and as an end-user subsystem, model 5210, consisting of a drive packaged with software and ready to plug into an IBM-PC/XT without additional interface electronics. Alloy Computer Products (Framingham, MA) currently purchases drives from Cipher and offers a subsystem of their own called the MT-25. AT&T is using the Floppy-Tape drives in their small business systems. And to further promote Floppy-Tape as a standard for low end products, Cipher has announced they will license the technology to any interested drive manufacturers.

3M also offers a quarter-inch cartridge format. Their HCD-75 is a high-end format which uses cartridges hard-formatted at the factory. Similar in structure to a hard disk, the format uses 16 tracks, a directory structure and data blocks with "keys" that allow the user to identify and access individual records.

Tallgrass Technologies and Hewlett-Packard offer a format called PC/T similar to 3M's but intended for personal computer applications. PC/T is charac-

terized by GCR data coding, rather than the lower-density MFM coding used on HCD-75 and FloppyTape. Like HCD-75, but unlike either FloppyTape or QIC, PC/T has error correction integral to the data, allowing error correction on the fly. PC/T allows over-writing data without prior erasure, which means that files may be modified or appended and a directory can be maintained. Also, PC/T uses a single-gap head design, lowering head cost and eliminating one set of read electronics. However, it is more costly than FloppyTape, and it doesn't support direct read after write, as do the QIC formats.

"We've clearly demonstrated that you can achieve all the data reliability that you want without any read after write – essentially because of 3M's error correction techniques," claims Dave Allen, President of Tallgrass Technologies, who developed PC/T. "This is technology which 3M has effectively contributed to the industry. It's new, and the rest of the tape industry is largely unaware of it and frequently skeptical about it; but the fact of the matter is, 3M's error correction technique works. It's extremely reliable, and it's very appropriate to the cartridge environment."

Minicartridges Enter Spotlight

Recently attention has turned from 3M's standard quarter-inch cartridge to another media from 3M: the DC1000/2000 minicartridge. As late as last year, cartridge drive manufacturers downplayed the significance of the minicartridge, claiming that it would find only limited use in specialized applications, such as field recording and data logging. Two factors have altered that forecast considerably.

The first factor is the expected high demand for 3½" Winchester disk drives, along with a corresponding high demand for small format tape drives to back them up. Since standard quarter-inch cartridges are too large for 3½" footprint drives, most cartridge tape drive manufacturers are now developing minicartridge drives to address the market.

The second factor was 3M's announcement of the DC2000 cartridge to be shipped later this year. The DC2000 media resembles the DC1000, but uses quarter-inch tape rather than 0.15" tape. This will allow development of 20-Mbyte and 40-Mbyte minicartridge drives suitable for backing up 3½" Winchesters
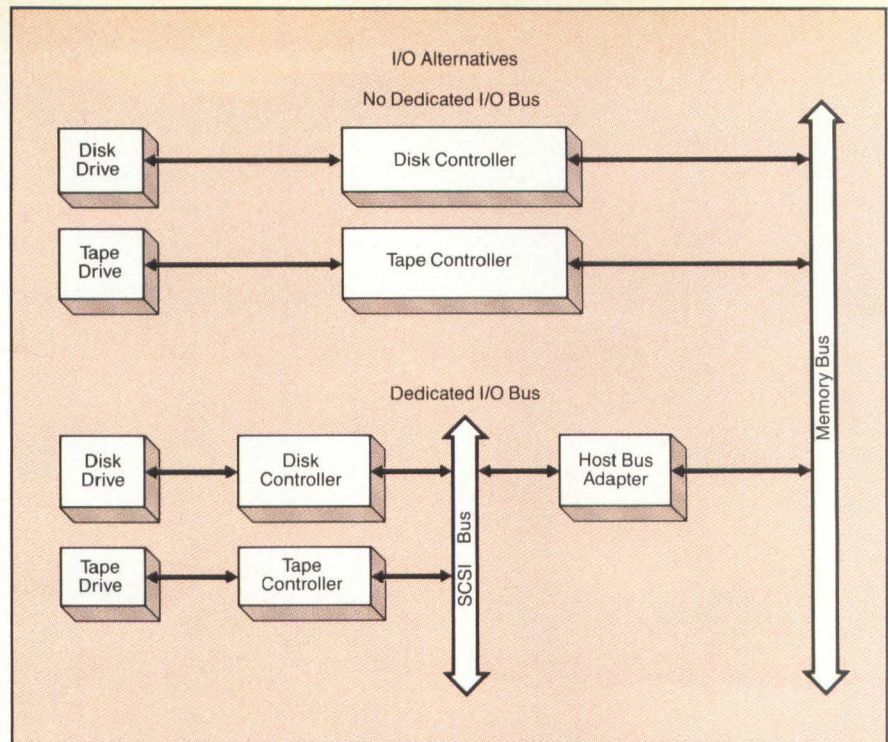
Figure 4: Dedicated I/O buses, such as SCSI and IPI, allow multiple peripherals to connect to a standard host bus adapter.

with similar capacities.

While a number of companies have built minicartridge drives for such applications as data logging, until recently, only Irwin Magnetics (Ann Arbor, MI) built a drive for Winchester back-up. However, products have been announced by Tallgrass Technologies (Overland Park, KS) and APTEC (Columbia, MD), and a variety of other companies have indicated that they are developing drives.

The sudden burst of activity in the area has prompted the QIC group to devote itself to working out standards to keep the young market from fragmenting. At the first meeting of the DC1000/2000 group, they decided to use the PC/T format as a working document from which to develop standards. Other formats under consideration were the QIC-24, the QIC-50, Irwin Magnetics' floppy-compatible format and Cipher Data Products' Floppy-Tape format.

"All the contenders were evaluated using basically a decision matrix that prioritized various features and weighted them as to desirability," explained Tallgrass Technologies President Dave Allen, who presented the PC/T format. "It was very gratifying; we felt as though the industry is finally starting to realize some of the advantages we've been trying to explain these many months."

However, selection of PC/T as a working document for the QIC group does not mean that PC/T will become the QIC

group's proposed standard. "They've elected to use the PC/T document as a working document rather than a sheet of blank paper. But that doesn't mean they endorse the document," explains Freeman. "It doesn't mean that it can't happen either," he adds, "but it would be very presumptuous to assume that at this stage."

Cassettes Offer Small Format Alternative

Another contender for small Winchester back-up is cassette tape. Small enough in size for 3½" Winchester footprints and high enough in capacity (up to 40 Mbytes) for 5¼" Winchester back-up, the biggest stumbling block for cassettes is probably their name. Because of their association with low performance cassette recorders used with small personal computers, high performance cassette drives are often overlooked by systems architects. This perception problem is so severe that one manufacturer – Memtec – refuses to use the term cassette with reference to their product, preferring to call them "miniature reel-to-reel drives."

In addition to their small size and high capacity, streaming cassette drives offer other advantages. Cassettes have a lower cost per Mbyte than any other media suitable for small Winchester back-up. They are currently being shipped in volume and have been extensively field tested. And, they conform to QIC and

SCSI standards, making them easy to integrate.

The companies involved with cassette drives and media have a working group of their own called D/CAS. Currently, the group consists of Memtec, Raymond Engineering, TEAC, Verbatim and Braemer.

Microwafer Fills Low End

As cassette drives move upward in performance, a low cost alternative "Microwafer" from Entrepo, seeks to replace them at the very low end. Microwafer is a small cartridge containing a continuous loop of videotape. Capacity of the cartridge is currently 128 Kbytes, with a 256 Kbyte version to be available soon. Price of the drives, in OEM quantities, is between $20 and $30.

Microwafer technology was originally introduced five years ago by a company called Exatron, who sold a product called the "Stringyfloppy" drive. Entrepo took over the technology in 1983. "There was some big business for that product," says Entrepo President Robert McDonald, "but it turned out it didn't work very well. So we took it off the market, redesigned it completely and now we're putting it back out on the market. We're just starting to get people to have faith in the technology again."

McDonald expects Microwafer to find a niche above standard audio cassettes, but below floppy disks in both performance and cost. "We'll try to get in there for about a third of what a floppy disk would cost."

Currently, Entrepo offers the model

Figure 5: Irwin Magnetics' model 210 tape drive is the first to use DC100A-class minicartridges in a 3½" Winchester footprint. Interface is floppy compatible.

101, which is the basic tape drive, and the model 107, which is the drive plus controller. In addition, they have announced a storage system called Quick Cassette for Commodore 64 and Vic 20 computers. Suggested retail price of the system is under $85.

I/O Standards

A growing trend in mass memory subsystems is the use of standard I/O interfaces such as SCSI and IPI. Systems built around these interfaces allow the host to interconnect to a variety of peripherals through a standard host adapter (**Figure 4**). Devices built to the proper specifications should interconnect to the host and to each other without modification, regardless of device type.

Both SCSI and IPI are expected to coexist, SCSI serving the low- to medium-performance systems and IPI serving the

medium- to high-performance systems (**Figure 5**). SCSI specifies an asynchronous data transfer rate of 1.5 Mbytes/sec, and a synchronous rate of 4 Mbytes/sec. Maximum cable length is six meters using single-ended line drivers, or up to 25 meters using differential drivers. IPI has a transfer rate of 10 Mbytes/sec, with a double-byte transfer path and a cable length of 125 meters.

SCSI tape drives are already widely available in nearly every product class. These include cassette drives, cartridge drives and half-inch tape drives.

Stable Future

At the low end, magnetic tape's low cost should assure its future. It is, and should remain, the cheapest removable storage media for low cost computers, electronic typewriters and other electronic instruments. For mid-range systems, there are few other alternatives to magnetic tape for secondary storage needs. Removable Winchester disks offer higher performance, but at a much higher media cost and with a lower capacity. And at the high end, IBM's commitment to magnetic tape assures its future well into the 1990s and beyond. Consequently, as has been the case throughout the history of the computer industry, designers can count on the fact that magnetic tape will be a part of most systems for a long time to come. **DD**

| PERSONAL COMPUTER | BUSINESS COMPUTER | | MINICOMPUTER | | MAINFRAME | |
	SINGLE USER	MULTI USER	REGULAR	SUPER	REGULAR	SUPER
Controller Function Integrated into CPU						
	Controller Supports Multiple Device Types					
			Controller is Head of String			
				Multiple Tiers of Controllers		
	Imbedded SCSI					
	ANSC IPI Level 2					
	ANSC SCSI					
	ANSC IPI Level 3					

Figure 6: The market application areas for the two ANSC interfaces, SCSI and IPI, are overviewed in this table.

Magnetic Tape Drives: The Key Manufacturers

Half-Inch Open Reel

Anritsu, **Circle 302**
Burroughs, **Circle 303**
Cipher Data Products,
Circle 304
Control Data Corp,
Circle 305
Datatape, **Circle 306**
Fujitsu America, **Circle 307**
Honeywell Informations
Systems, **Circle 308**
Ibex Computer Corp.,
Circle 309
Innovative Data Technology,
Circle 310
International Business
Machines, **Circle 311**
Kennedy, **Circle 312**
Perkin-Elmer, **Circle 313**
Pertec, **Circle 314**
Storage Technology,
Circle 315

Telebyte Technology,
Circle 316
Telex, **Circle 317**
Thorn EMI Technology,
Circle 318

Half-Inch Cartridge (second source)

Digital Equipment Corp./3M
(no product available yet),
Circle 319
Electronic Processors, Inc.
(Memorex), **Circle 320**
Memorex OEM Equipment
Sales, **Circle 321**
International Business
Machine (no product
available yet), **Circle 322**
Megatape, **Circle 323**
Rosscomp, **Circle 324**
Tandon, **Circle 325**

Quarter-Inch Cartridge

Archive, **Circle 326**
Chiper Data Products,
Circle 327
Data Electronics, Inc.,
Circle 328
Kennedy, **Circle 329**
North Atlantic Industries,
Circle 330
Northern Telecom,
Circle 331
Data Park, **Circle 332**
Tandberg Data, **Circle 333**
3M, **Circle 334**
Wangtek, **Circle 335**

Minicartridge Drives

Advanced Peripheral
Technology, **Circle 336**
Irwin Magnetics, **Circle 337**
Tallgrass Technologies,
Circle 338

Cassette Drives

Braemer Computer Devices,
Circle 339
Memtec, **Circle 340**
Raymond Engineering,
Raycorder Products Div.,
Circle 341
Saylor Electronics,
Circle 342
TEAC Corp. of America,
Circle 343

Other Tape Formats

Entrepo (128-Kbyte to
256-Kbyte Microwafer),
Circle 344
Interdyne (10-Mbyte
to 40-Mbyte tape reel),
Circle 345

A number of companies offer a variety of tape drive options in nearly any configuration, ranging in capacity from 128 Kbytes to 500 Mbytes.

Machine Vision — Coming Of Age

by Gregory MacNicol, West Coast Technical Editor

Shadowed by robotics, machine vision is now being recognized as a fast growing industry. This should be no surprise, as machine vision systems have immediate applications.

The ability of a computer to see, identify and make a decision rapidly is critically useful in manufacturing, scientific analysis and identification. Associated with robotics, artificial intelligence (AI) and computer graphics, machine vision is one of the critical elements in making the system complete and functional.

As the field of machine vision matures, new applications arise that were never before considered. Motion Analysis (Santa Rosa, CA) uses their Expertvision to automatically analyze intricate movements of microscopic organisms, humans, robots and even fish. But the number one

market of machine vision is the automotive industry. Machine vision holds so much promise that GM, for example, invested in four major players in machine vision for their "factory of the future." Ford Motor paid $2 million for 16% of Synthetic Vision Systems (Ann Arbor, MI). The three major auto manufacturers plan on spending $600 million collectively over the next four years. Car manufacturers of the future are expecting vision systems that circumvent human control. As the diameter of a drive shaft is drifting out of tolerance due to the wearing down of the cutting tool, the system

can spot the change long before humans and automatically change the cutting tool. A major reason for their desire for direct involvement is to ensure that the systems are truly functional and not just research projects. They want to bridge the gap between factory-based users and laboratory-based development projects.

The difficulty in understanding machine vision is often underestimated. Ten years ago when machine vision was just emerging, experts said that it would be only two more years before the process of intelligent vision in humans would be understood. Today it is still an enigma. Vision not only relies on identification but symbolic representation. The mystery is based on the difficulty in comprehend-

Above: (left) The CYTO 4 computer from Synthetic Vision Systems Inc. and (right) a pseudo-color image/flaw display.

As the technology of machine vision matures, applications increase.
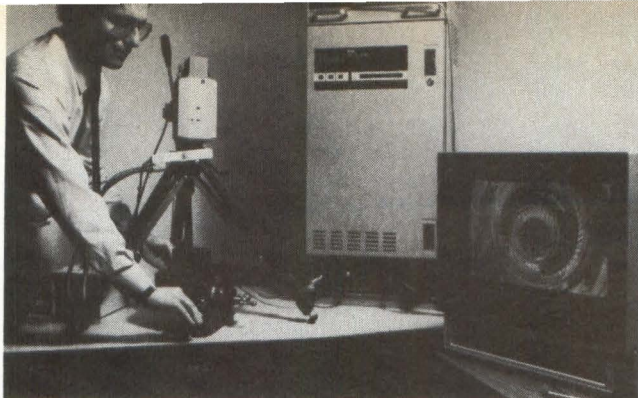
The Itran 8000 vision inspection system is counting the rollers in an auto bearing.

ing why the simple act of seeing is so difficult to understand, not to mention implementing the process in a computer.

The process is further complicated by the environment typical for machine vision. The workplace is more commonly a harsh industrial setting with poor temperature control, very poor power regulation, sparse lighting and nontechnical operators using the system. To make matters worse, oil spray, metal flakes and varying light levels change the quality of the sensor data. A good systems integrator, nevertheless, has many good choices of components to integrate into a functional and reliable system.

What Is Machine Vision?

Machine vision, sometimes called computer vision, is the implementation of the pattern recognition process for the interpretation of visual data. Machine vision, thus includes hardware, optics, feedback control, software and systems integration. There are five basic processes that incorporate machine vision: image input, sampling and quantization, preprocessing, feature extraction and object recognition. Advanced systems with simple closed loops provide feedback for focusing after sampling. The source data can originate from sources such as X rays, tomography, video cameras, 3D sources or radar. While vidicon cameras have been popular for some time, they suffer streaking from bright light sources. Second generation CCD solid state cameras are replacing them also because of their high bandwidth and direct digital output. This is important for rapidly moving objects. Sampling and quantization is critical and is dependent on the speed and quality of analog to digital converters that transform the information for the frame buffer. Preprocessing is used to

adjust for contrast and average image intensity. Feature extraction and object recognition is only one of the intelligent functions of machine vision, which can also include identification, description, 3D mapping and other complex operations. Finally, all of this information must be useful, that is, easy for the end user to control and augment for an end goal to be realized.

The problems that surround machine vision are not limited to the gruesome environmental conditions that are typical for installations. Most machine vision systems solve a very specific application problem. This means that most hardware and software is custom tailored and generally not applicable for other situations. This can pose a serious threat to the survivability of a company dedicated to machine vision. A system must be easily upgradable for future functions. Further, equipment should be compatible with other equipment, both electronic and mechanical.

Another basic problem is software. Having similar problems in AI, machine vision also has to resolve ambiguous visual situations. For example, how does a system identify new parts or ones with different colors, or differentiate between surface blemishes and true failures? A serious and unresolved issue is 3D perception. A complex object with convex and concave artifacts can be very confusing to correctly identify. While simple solutions involve the rotation of the object or use of two or more cameras, the process that correctly identifies and qualifies is still a major issue. A solution may exist for one object, but programming a solution for every object is unrealistic. This is related to a very basic aspect of mechanics involved with machine vision, lighting of the 3D object. A gray object on a gray conveyor belt must be lit in such a way as to not produce stark shadows and provide just the right diffuse lighting for the computer to gain all the necessary data.

Still, the most important issue for machine vision to become real is making the system operate in real time. Real time systems which are used in automated applications, must provide pattern recognition at speeds fast enough to control manufacturing operations. General purpose computers are often taxed by complicated applications because of the complexity of the programs required to perform the recognition process. Additionally, the motion of fast moving objects requires fast data capture and storage, requiring proper sensor equipment and A/D converters.

Applications of real time systems range from simple presence to robot guidance systems. Other applications include inspection, part recognition, quality control, visual guidance and dimensional analysis. Secondary applications include part tracking, measuring, recognition and part location.

The Bottleneck

After the scene is digitized, translation of the data for analysis is next. The amount of data needed for a 256×256 image is 65536 bits per bit plane, which if processed at 30 frames/sec is very demanding on the transformation process.

The two steps of processing and analyzing the data have shortcuts. Coverting each pixel into a binary value reduces data but at the cost of reducing the accuracy of analysis. This is called global thresholding. Another method of reducing the data to be analyzed is windowing the digital scene. Windowing eliminates unnecessary data and focuses only on relevant information.

The most common method of data reduction is segmentation. This method divides the relevant areas and interpolates the surrounding data. Segmentation, like most data reduction schemes, also makes the data less accurate. One of the oldest algorithms for segmentation is the SRI algorithm, developed at SRI (Stanford, CA). It consists of about 50 global fea-

tures such as area and perimeter that are extracted from a binary image. Its popularity is being quickly replaced by newer algorithms, one of which is convolution that depends on the rate of light change per pixel instead of light intensity. Neighborhood processing depends on gray levels, where each pixel is treated as if it were a part of a group. This data reduction process averages the scene into a group of regions. String encoding or run length encoding takes a scan line and determines whether the pixels belong to a specific region. Modifications to the generated tables can also determine vertical and diagonal regions. At Portland State University, researchers are applying artificial intelligence to the SRI algorithm using rule-based representation as derived from situation-action functions.

Itran Corp. (Manchester, NH) uses gray scaling for 6 bits of resolution that gives the system 64 shades of 320×240 pixels. The final image is then pseudocolored for highlighting and text. The frame buffer can hold up to eight 320×240 images or one 1024×1024 image.

Storage of eight images is especially useful because the system can accept eight camera inputs. Itran has chosen to use their own proprietary array processor chip to compute normalized correlations and carry out edge detection. The choice was based on factory environmental conditions and easy specific implementation of PALs. Using the 68000 and the 68450 DMA, the Itran system is based around the VME bus.

A reason why the processing remains a bottleneck is largely because the data is computed serially. Thus, a major trend in the image processing field is use of parallel processing where large matrices are computed in parallel. Board level array processors also take part in increasing the calculation speed. Systems integrators have many choices of boards on common buses. The two most popular buses presently are the Multibus for 16-bit operation and the VME bus for 32-bit.

As each system is vastly different from the other, it is important to evaluate how a system is to be installed. While some manufacturers have distributers set up and program a system, other manufac-

turers play an active role in configuring and programming a system. Machine Vision International provides a language called BLIX, which allows customers to write their own programs. Clearly, the more complex and powerful a system is, the more complicated it will be to install.

For the OEM developing machine vision products, there are many routes for configuring a powerful system without having to develop custom equipment. This is very important for a fast moving technology. Imaging Technology (Woburn, MA) offers a full line of imaging boards and software for the Qbus and Multibus. Included in their product line is a frame buffer, analog processor, extraction module and analog processor. Available for the IBM PC is a frame grabber that accepts an RS-170 video signal at video rates and digitizes a $512 \times 512 \times 8$-bit image at 30 frames/sec.

Another supplier of imaging boards is Datacube (Peabody, MA). Pattern Processing Technologies (Minneapolis, MN) uses Datacube's VG-921 videographics board for their APP vision system. Resolution is 320×484 pixels at 6
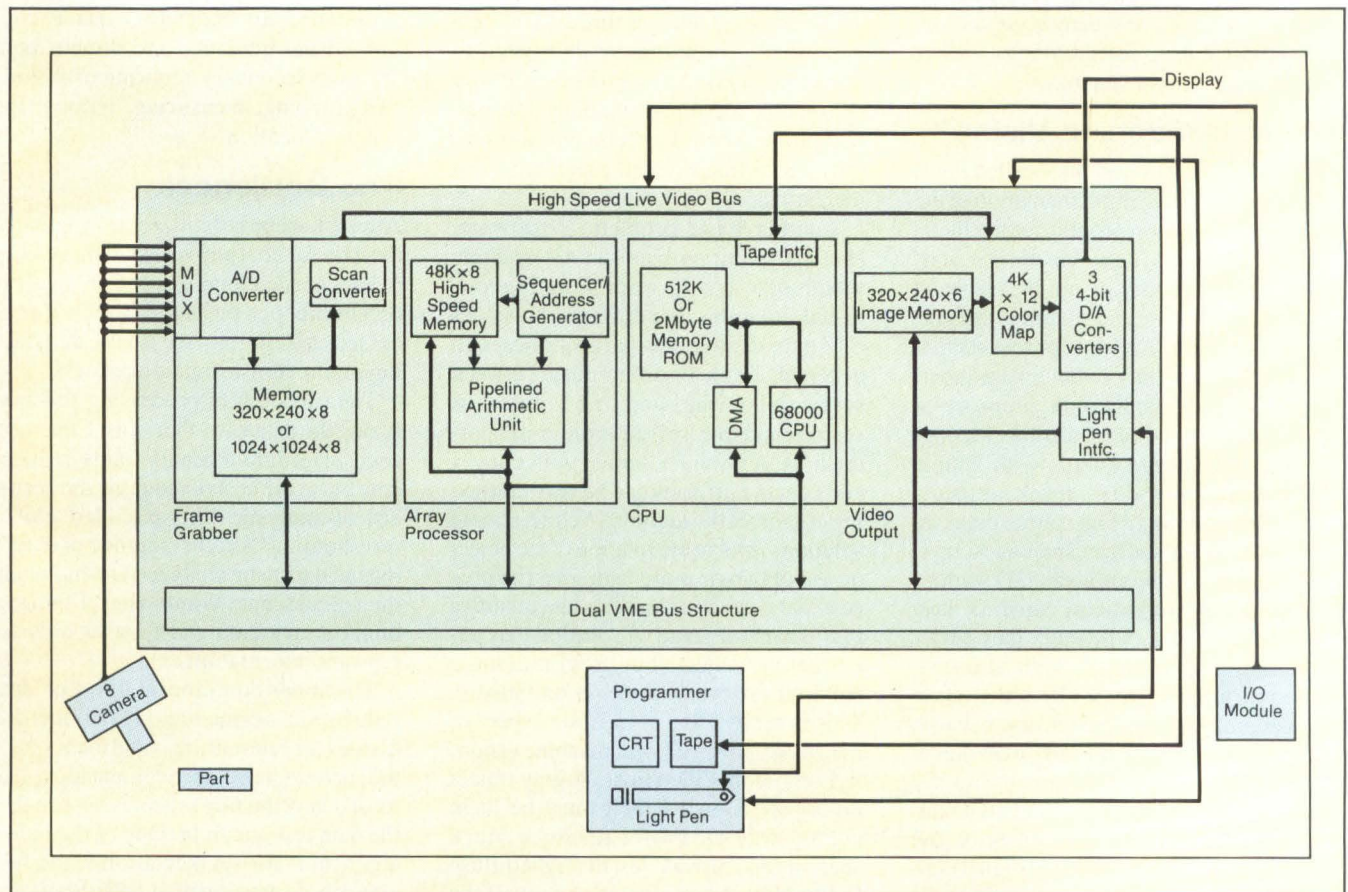
Figure 1: Schematic diagram of the Model 8000 Vision Inspection Controller from Itran.
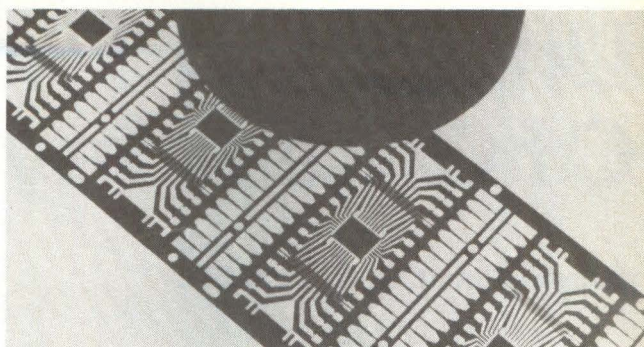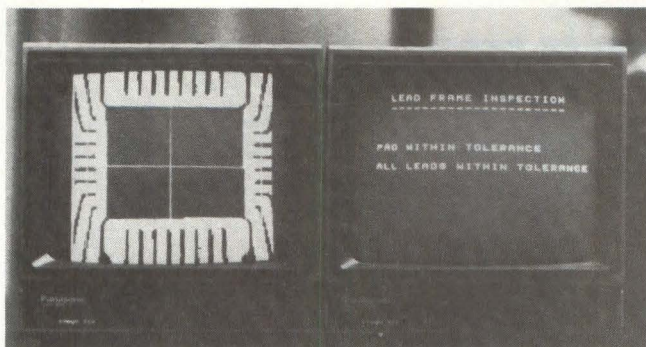
Control Automation's InterVision 1000 vision system is a computer-based inspection system with solid state camera.

bits deep, and the system has the ability to inspect 3000 parts per minute. Control Automation (Princeton, NJ) uses Datacube's VG-121 controller and Multibus boards from Intel for their Intervision 2000. Control Automation is also using an array processor board from Marinco (San Diego, CA) for fast video processing.

Newer sensor chips are adding power to vision systems. Philips (Cologne, West Germany) has developed a 600×600 pixel image sensor chip, where one half of the chip is used for pick-up and the other for storage. Surface area of the chip is 66mm² (½″ diagonal). More importantly, the chip does not suffer from burn-in and lag, typical problems from vidicons. The small size, rugged structure, storage capability and solid state performance is excellent for industrial environments.

Vision Of The Future

In the past, machine vision systems were used for simple pass/fail or quantity tests.
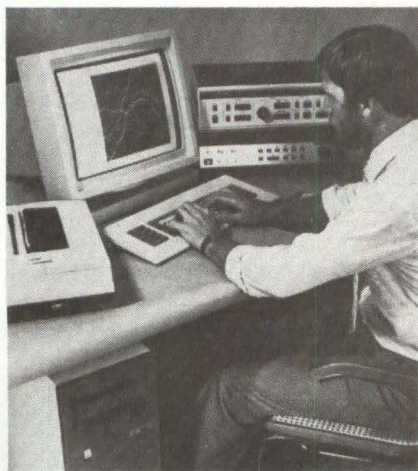
ExpertVision by Motion Analysis Corp. integrates data collection, analysis and reporting into a single automated system.

Most vision systems today only do simple inspection. If there is a problem, an operator intervenes. Machine vision systems of the future are going to be radically different, not because of profound understanding of human vision, but because of closer ties between the laboratory and the factory floor. One of the goals is closed-loop systems where the machine vision system is an integral part of the whole process. As parts go out of alignment, the vision system will spot the flaw and resolve it in several ways. It will be able to spot the problem, identify the type of flaw and oversee a complete process to resolution. It will act as an intelligent eye for a robot arm to manipulate the part for closer inspection and guide the arm for binning. GM is planning an impressive automated factory in Saginaw, MI from the ground up with machine vision capabilities and process controls for controlling robots and machinery. GM is also interested in AI, investing $3 million for 13% of Techknowledge (Palo Alto, CA).

As computational issues remain a bottleneck, help is coming in the form of silicon. Hitachi introduced their HD 6184OR image processing chip which can process a 256×256 image in 10.9 msec. They are representing a major trend in image processing where data stream processing, pipelining and parallel processing are being used for real time, video rate computation. NEC, too, has a single chip image processor capable of five million instructions/sec. Touted as a non-von Neumann, the μPD7281D is data driven with the pipeline and can be cascaded for better performance. Systems architects can get help utilizing the 7281 through available software support such as an assembler, simulator and a program library.

Another new demand is networking.

The system of the future will be able to take data retrieved from other systems or other data bases and create new histograms for advanced or new tasks. It will also be able to compile the data in other useful forms such as failure rate or factory volume. Machine vision is based on information gathering, and the information has greater importance than pass/fail tests.

If machine vision is to meet its expectation, it will be necessary to alter its course. Faster and better general purpose computers are not the answer. Instead, new approaches to data processing and image processing will become dedicated and implemented in silicon. Furthermore, new architectures will be necessary to handle parallel processing, data flow processing and finite state analysis. Additionally, artificial intelligence research is getting closer to helping understand the visual process as well as implementing the process of visual comprehension. Not only should the vision system be able to accurately identify a part, but also describe the contents of a room it has never seen.

Vision systems of the future will be based on modular components. Systems integrators will be able to choose, modify and target specific answers to specific problems through the use of common buses, standardized I/O and networking protocol. The new generation of machine vision systems will be able to perform in real time with greater intelligence. **DD**

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Unlocking The Mysteries Of Gate Array Design, Part II

by Ronald Collett, Sr. Technical Editor

S uccessful gate array design on a workstation requires an understanding of the potential problems. In Part I of this series (January, 1985), we described the CMOS gate array to be designed as well as the goals to be achieved. This report covers some of the potential stumbling blocks designers should be aware of before undertaking the task.

Thus far we have found no single crippling flaw in the design cycle. Instead, there are many small problems that have the potential to seriously delay the project. All design projects are filled with these types of small problems, regardless of whether it is an IC, printed circuit board (pc board) or even a higher level implementation. However, designing a gate array on a workstation is likely to be a new experience for most design engineers. Thus, the solutions to the inevitable small problems, which are easily handled in a pc board design, are not necessarily resolved as quickly in a gate array. (A flowchart of the typical design cycle is shown in **Figure 1.**)

Whose Gate Array To Select

One pitfall to avoid is choosing a gate array vendor who offers array sizes that are separated by more than 500 gates (i.e., a vendor offering arrays with 1000, 2000 and 3000 gates). The potential problem is subtle, so the best way to appreciate the situation is to look at a typical design scenario.

Suppose a circuit requires approximately 1600 gates, and a vendor offering both a 2000- and 3000-gate array is selected. It appears logical to choose a supplier whose chips provide the level of integration necessary to accomodate the circuit. However, this is only a preliminary estimate of the number of gates needed; it does not adequately address the possibility of slightly expanding the amount of circuitry to be put onto the array. Additional test circuitry, for example, is often added well after a design has begun. Furthermore, how many designs proceed through the development cycle without an engineering change notice (ECN)?
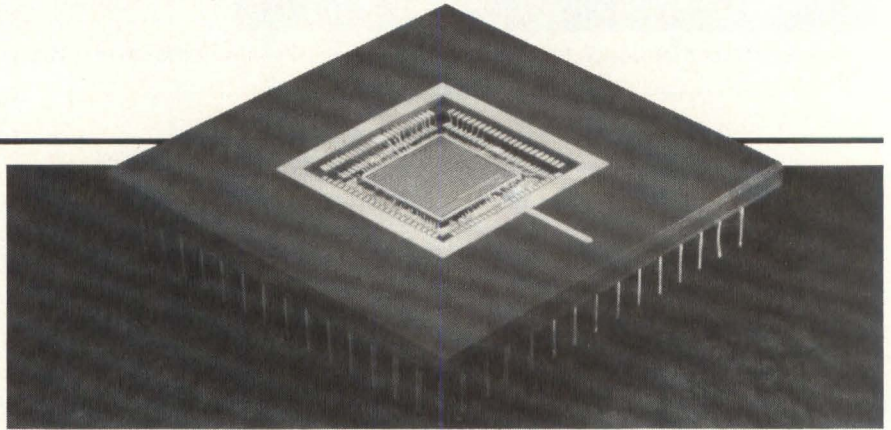
In nearly all gate arrays a maximum of 90% of the gates can be utilized. The remaining 10% are used for wiring channels when the chip is routed (and in most cases, this number is really 15% to 25%). Although predefined wiring channels are carved out on the array, additional paths are often necessary; thus, a certain number of cell locations must be seized. As a result, if we assume that only 85% of the gates can be used and we selected a 2000-gate array, then already we have decreased our original array size by 300 gates and are left with only a 100-gate margin.

Assume that during the course of the design cycle we decided to implement some additional logic requiring 200 more gates. We now have an 1800-gate circuit that must fit onto a 1700-gate array. At this point we would use the next highest available array — 3000 gates. Our gate requirement would certainly be met, but of course a 3000-gate chip is more costly. Once we switch to a bigger array, the cost remains the same whether or not the extra gates are utilized. We could put more logic on the array, but additional logic usually requires more I/O pins and a large, more expensive package. Thus, we are faced with an important decision when we jump to a 3000-gate chip: Should we increase the size and cost of our circuit by using the additional gates and adding more I/O pins or save I/O costs and waste hundreds of gates? Neither alternative is appealing.

If a supplier who offered arrays with 2000, 2500 and 3000 gates had been chosen from the start, we could have switched to the chip with 2500 gates and the problem would have been immediately solved. Although some gates would undoubtedly be left unused, the waste is far less than that in a 3000-gate chip.

Cell Library Vs. Off-The-Shelf

Using a cell library on a workstation is virtually the same as searching through a TTL or CMOS data book. LSI Logic's library is compatible with Valid's Scaldsystem I and a single command is all that is required to access a logic function.

An important factor, often hidden when using a cell library in conjunction with a workstation, is the number of logic functions (macros) that can be accessed via the workstation. For example, a gate

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array vendor may offer a library of 300 functions on their proprietary CAD/CAE system but only 100 for a workstation. In many instances, only those that are most popular are ported to the workstation. With this in mind, investigate which macrofunctions are offered on the in-house CAD/CAE system versus on the workstation.

If some particularly important models are not offered on the workstation, but do exist on the in-house CAD/CAE system, the customer should urge the vendor to port them to the workstation's library. Customers themselves can build these models from primitives, but for complex functions like ALUs or unique counters it can be a truly laborious chore. When constructing these high level functions, they cannot be haphazardly built and thrown into the library. Instead, they must be simulated and thoroughly checked for timing errors. A customer paying anywhere from $10,000 to $75,000 for NRE expenses plus additional costs for the cell library should not be burdened with the task.

The Propagation Delay Trap

Since CMOS is a highly load dependent technology, very careful attention must be given to the circuit's timing as well as the tools used to verify the timing. This includes device propagation delay, fanout delay and wiring delays. Propagation delays of functions found in a cell library may not be fixed because these delays are dependent upon how the array is routed. Looking at it from another angle, consider the situation when using an off-the-shelf counter for a board-level design. The gates that comprise the counter are wired inside the chip in a defined manner such that the various delays from one gate are within fixed range. Thus, the total delay time of that particular counter can be anticipated when put on the board.

In comparison, when a counter is used on an array, the various logic gates that make up the counter are not necessarily located in a single area of the chip. As illustrated in **Figure 2**, sections of the counter's logic could be located at one corner, while other portions may be found at the opposite corner. Essentially, the auto place-and-route algorithm needs this freedom of scattering the logic around the array to maximize the number of gates that can be automatically routed.

Figure 1: The typical gate array design cycle is exemplified by the flowchart; however, some slight variations may exist among vendors. Note the dotted line separating the front-end from the back-end of the cycle marks the dividing point between those tasks traditionally performed by the customer versus those done by the IC vendor.
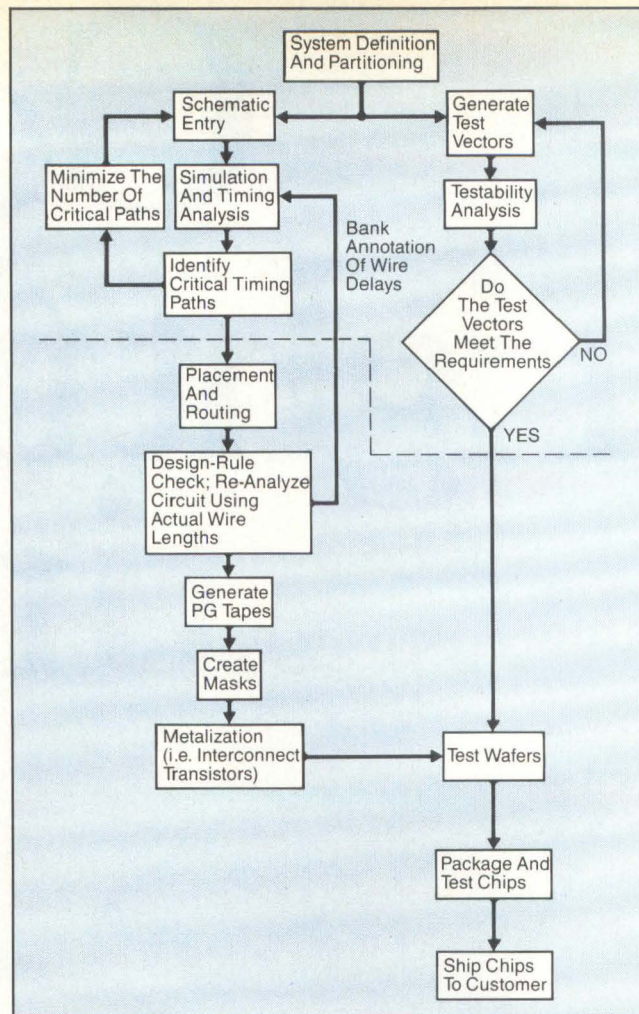
Introducing varying propagation delays is not likely to cause a complex timing problem unless the CMOS array is fully packed with logic and is expected to operate at high speeds (above 20 MHz). When this situation arises, the router must make the wires as short as possible but it has great difficulty in doing so due to the lack of cells available for wiring channels. As a result, longer delays will be created and paths that are not viewed to be critical in the eyes of the design engineer may become critical when the chip is undergoing layout. (Critical paths are signals that demand minimal delay between devices.)

Typically, when the design is ready for input to the automatic place-and-route software, critical paths are defined specifically to the layout program and are routed first. Suppose, however, that a particular signal within a counter is not identified as critical, since under conventional design practices the delay through such a device might be assumed to be approximated to within a tolerable value. When the router begins to partition and interconnect the array's transistors, it is indifferent to whether displacing the counter's flip-flops throughout the chip causes excessive delays which were assumed to be somewhat fixed. So unless a signal line is designated as a critical path, the counter could end up having an excessive propagation delay.

Although it seems intuitively obvious that simply identifying the signal line as a critical path relieves the problem, only critical paths that are noticeable will initially be spotted by the design engineer. And of course designating every signal in the design as a critical path is self-defeating, if not absurd.

This would not be a difficult problem if it occurred once or twice during the design cycle's layout phase, but if the array is densely packed and is supposed to operate at high speed, it could happen at a multiplicity of nodes and introduce a slew of timing problems. So, the end result might demand that a larger array be chosen to accommodate the speed and density requirements. With a larger array, the router has more freedom to adjust wire lengths for the chip's high speed paths since more cells can be used as
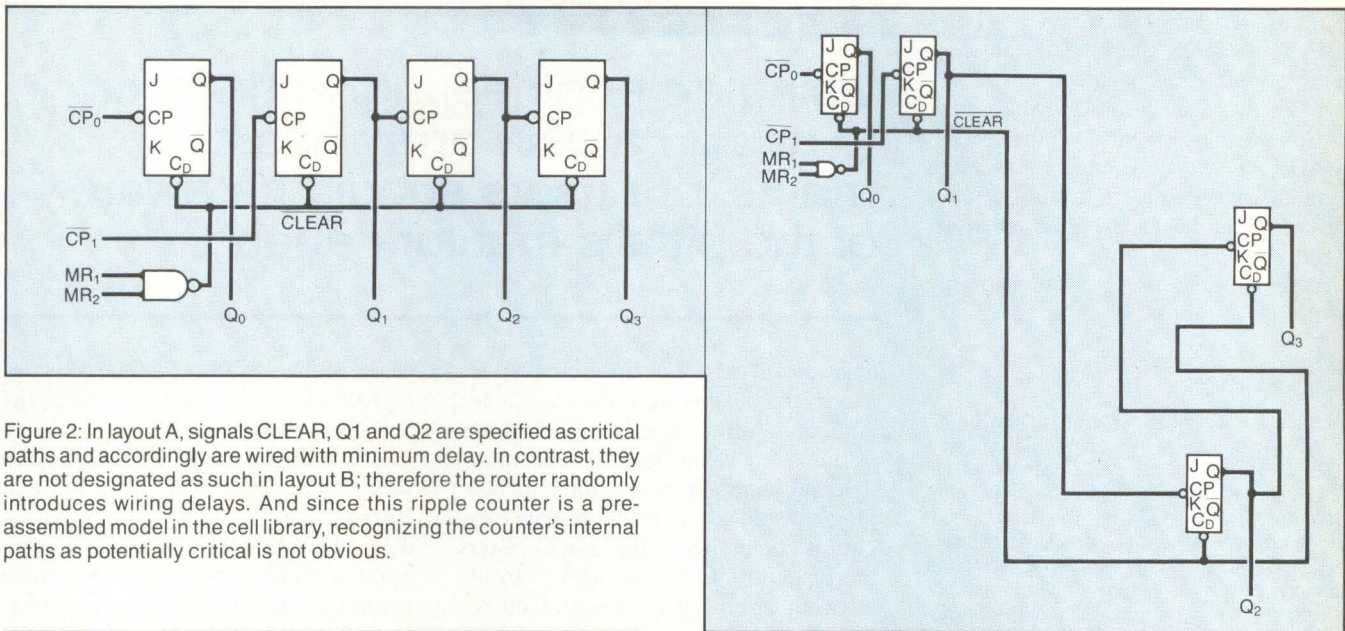
Figure 2: In layout A, signals CLEAR, Q1 and Q2 are specified as critical paths and accordingly are wired with minimum delay. In contrast, they are not designated as such in layout B; therefore the router randomly introduces wiring delays. And since this ripple counter is a pre-assembled model in the cell library, recognizing the counter's internal paths as potentially critical is not obvious.

wiring channels. As noted earlier, larger arrays come with higher price tags.

A second solution would be to switch to a faster array, but this is usually more expensive than raising the gate count. Moreover, most CMOS array vendors do not offer chips above 20 MHz. LSI Logic, however, claims that their high speed CMOS array series provides speeds up to 40 MHz. Of course, another option would be to change to a bipolar technology; but, this is also more expensive and has many drawbacks.

LSI Logic has taken action to at least warn designers of this routing problem by developing a software program called the Design Verifier. The cost of the optional program is $28,000. (There is also a monthly maintenance fee that amounts to around $2,000 to $3,000 per year.) The Verifier estimates the percentage of wires that can be automatically routed. With this tool, potential wiring problems can be resolved before routing. In addition, the software calculates the number of gates actually used and contains a statistical database of the timing delays associated with propagation, wiring and fanout.

Statistical wire length data is one of the more important features the Design Verifier provides. When timing analysis is being performed on a circuit, the Verifier is used to model the wiring delays that will eventually be introduced into the circuit. Although the system is not foolproof, (since it is based on probability theory and statistical analysis), it does offer the designer a way to more effectively ana-

lyze a circuit's timing. (In Part III of this series, March 1985, we will examine the Design Verifier more closely.)

The Back Annotation Problem

Comprehensive timing analysis is crucial to the success of any gate array design. After the circuit has been fully simulated and undergone a thorough timing analysis on the workstation, it is sent to the vendor for routing. The routing software typically completes 80% to 95% of the job and leaves the remainder of the task to the design engineer. In most instances, if the remaining unconnected wires are not too difficult to route, LSI Logic will do it for the customer. However, in the case of a monumental job, the customer will be forced to route the remaining gates or reconfigure the troublesome circuits. After the routing is finished, the array's actual wire lengths are calculated.

Back annotation of actual wire delays is the most significant shortcoming of the interface between LSI Logic and Valid's workstation. Back annotation, in this context, means that those post-layout actual wire-lengths can be downloaded back to the workstation so that a 100% accurate timing analysis can be performed on the workstation. Presently, this empirical wiring data can be used only in conjunction with LSI Logic's mainframe — not on the workstation.

Timing analysis is accomplished prior to layout as well as after layout. Pre-layout timing verification can be executed on the

workstation, and as mentioned earlier, it is based on statistical wire-lengths (if the Design Verifier is used). But to ensure the chip will function properly once it is committed to silicon, a timing analysis that utilizes the actual wire lengths is performed. This is usually executed by the vendor on their mainframe-based CAD/CAE system. (LSI Logic has an Amdahl system that runs at 4.3 MIPS). The issue is whether the post-layout timing analysis can be performed on both the workstation and vendor's mainframe. The IC supplier should certainly run the analysis first on their system, but if timing problems occur, the customer should have the opportunity to rectify the problems using his workstation.

If no timing errors arise after the circuit is re-analyzed using the actual wire lengths, then the issue is moot. If timing problems are detected, however, the customer will indeed be forced to make some alterations in the circuit and then re-check the circuit's timing. Since, at the present time, the post-layout analysis can be done only on the LSI Logic's mainfame, workstation users must travel to an LSI Logic design center to rectify any timing problems, or link up to LSI's system via a modem. Of course the user must be familiar enough with the syntax of the LSI CAD/CAE system to perform the analysis. This situation is not unique to LSI Logic and Valid; it is an industry-wide problem and the burden rests on the gate array suppliers.

Correcting problems using the IC ven-

dor's CAD/CAE system may not be as easy as it sounds since the design engineer probably has been working solely with the workstation and may have very little experience, if any, on the foreign CAD/CAE system. Therefore, the design engineer will likely go through a short learning (or relearning) period to become familiar with the system.

Manually entering the actual timing

Using an engineering workstation to design a gate array has its merits, but users should be aware of the pitfalls that lurk ahead.

Figure 3: Using the "sizing" technique on Valid's Scaldsystem I, we were able to fit nine B-sheets of logic onto a single page. However, as illustrated in the resulting one page schematic, neither the logic nor the interconnections are represented in a conventional style which causes difficulty in understanding the circuit's operation. At the same time though, using the "sizing" technique increased simulation and compilation speeds by 300%.

delay data of each node in the circuit is an alternative, but this is even less favorable. Although, Valid's Scaldsystem I allows timing delay values to be placed on individual wires and nodes, imagine how long it would take to enter this data for a circuit containing 10,000 nodes. Even more significant, there is a high probability of human error when doing this chore. And there is a strong chance that such an

error would be extremely time consuming to track down. Clearly, for a large circuit, this is not feasible.

On the brighter side, LSI Logic plans to introduce a software program that automatically back annotates the wiring delays to Valid's workstation. The program is expected to be available in the second quarter of 1985. Since this interface problem surely exists between other
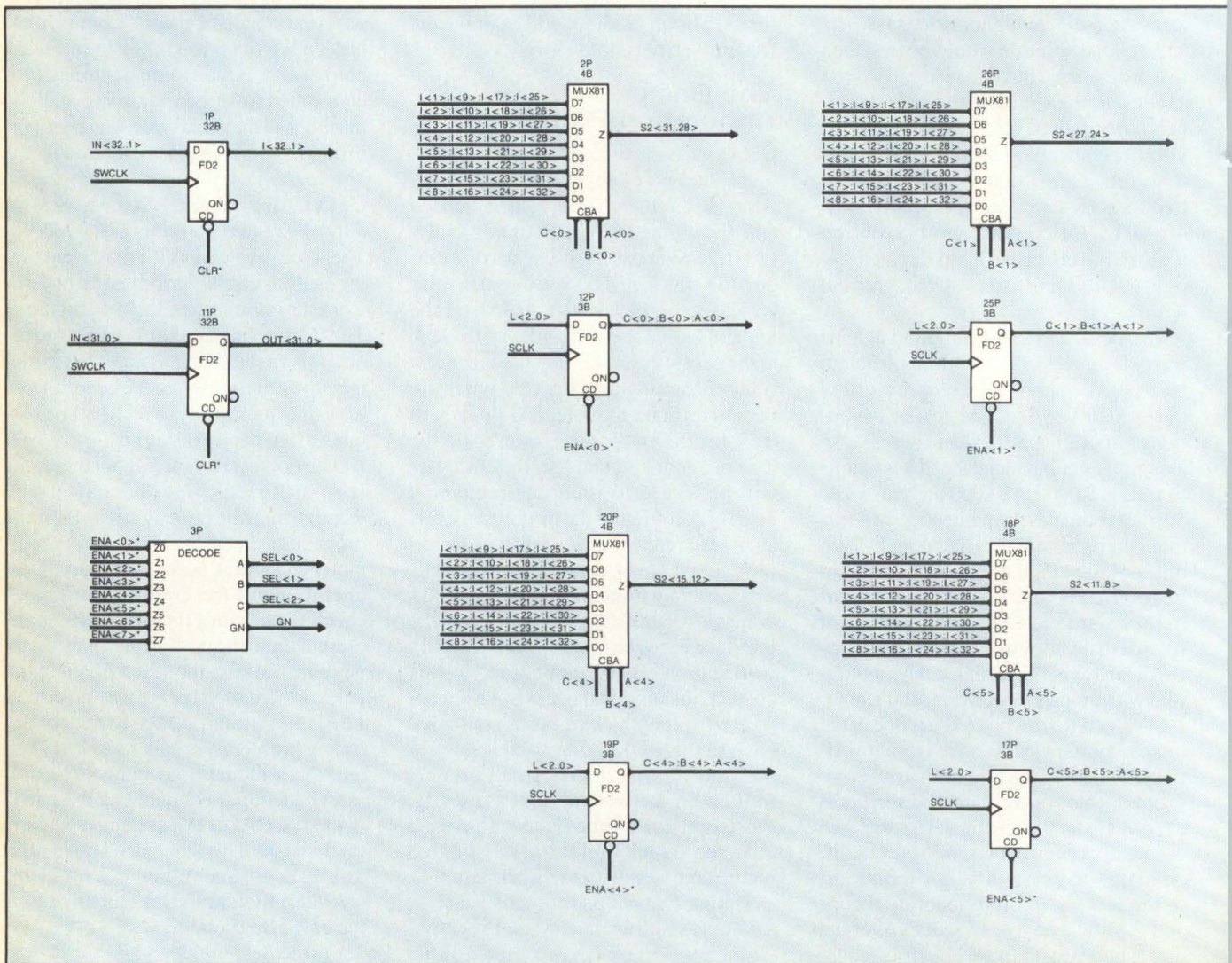
IC suppliers and workstation manufacturers, determining whether a particular IC vendor offers such a software package is strongly recommended.

Simulation On The Workstation

Much time is spent simulating the circuit. However, the design must first be compiled into a format that is compatible with the simulator. The amount of time that the system expends on compilation is directly related to both the size of the circuit and the manner in which it is described. On the Scaldsystem I, schematics can be entered in either of two ways. The first method is exactly the same as if a design engineer were drawing the circuit — each wire and logic element is sketched. When drawn in this fashion, the schematic is said to be entered "flat."

The second way is to streamline the circuit description by using certain commands to describe a function, instead of actually drawing the function. A 16-bit bus, for example, could be shown as a single wire with the term "16B" placed on it. This kind of streamlining can be applied to all portions of the schematic where repetition exists. Another example might be six flip-flops that are being used as a register. Instead of drawing all six flip-flops, only one needs to be shown, and a "6B" would be placed next to it. This is known as "sizing" the schematic. There are other syntax commands available that offer the design engineer similar capabilities, but these are better left for the design manual.

At first glance it may seem that the only reason for having this capability is to reduce schematic entry time. Assuming the workstation user is proficient at using the machine, this is certainly true. The significant time saving, however, comes during the compilation stage.

The workstation compiles the data two to three times faster when the schematic is entered using the sizing method. In our design, the schematic was entered on two separate occasions. First done in the flat style, the system compiled the drawing in 45 minutes; the machine also required an additional 30 minutes to prepare the database for simulation. When the compilation was completed, 600 Kbytes of memory were used and nine B-size pages were needed to illustrate the logic. (Note: Our circuit is roughly estimated to be approximately 1400 gates.)

The second time the schematic was entered, the workstation's sizing capabilities were used. Compilation of the logic was accomplished in 15 minutes, preparation for simulation took 10 minutes, 150 Kbytes of memory were used and the entire schematic fit onto one B-size page. Judging from this benchmark, using the sizing properties to enter a schematic is almost mandatory.

A drawback to using this faster method is that the logic can be somewhat difficult to decipher when represented in this manner (**Figure 3**). Since many of the logic elements are not illustrated graphically, a netlist is the only way to get a point-to-point description of the circuit. Unfortunately, this problem becomes tedious during the circuit's debugging stage. Like most design engineers, we were accustomed to seeing the logic fully illustrated.

Training Courses

Training courses are one of the most important aspects of designing a gate array with a workstation and should not be viewed nonchalantly. Typically, the charge for a one week course is about $1,500. If we include the price of travel as well as the engineering time lost, the true cost of one of these courses ranges from $3,000-$6,000.

We enrolled in both Valid Logic's (San Jose, CA) workstation course and LSI Logic's (Milpitas, CA) design course. Each lasted for a week and was taken at the firms' Boston facilities. LSI Logic also offers a one-day course that covers material concerning their cell library when ported to Valid's workstation.

Studying the design manuals several weeks before attending the course is a must. Otherwise, absorbing several volumes of information in a week is virtually

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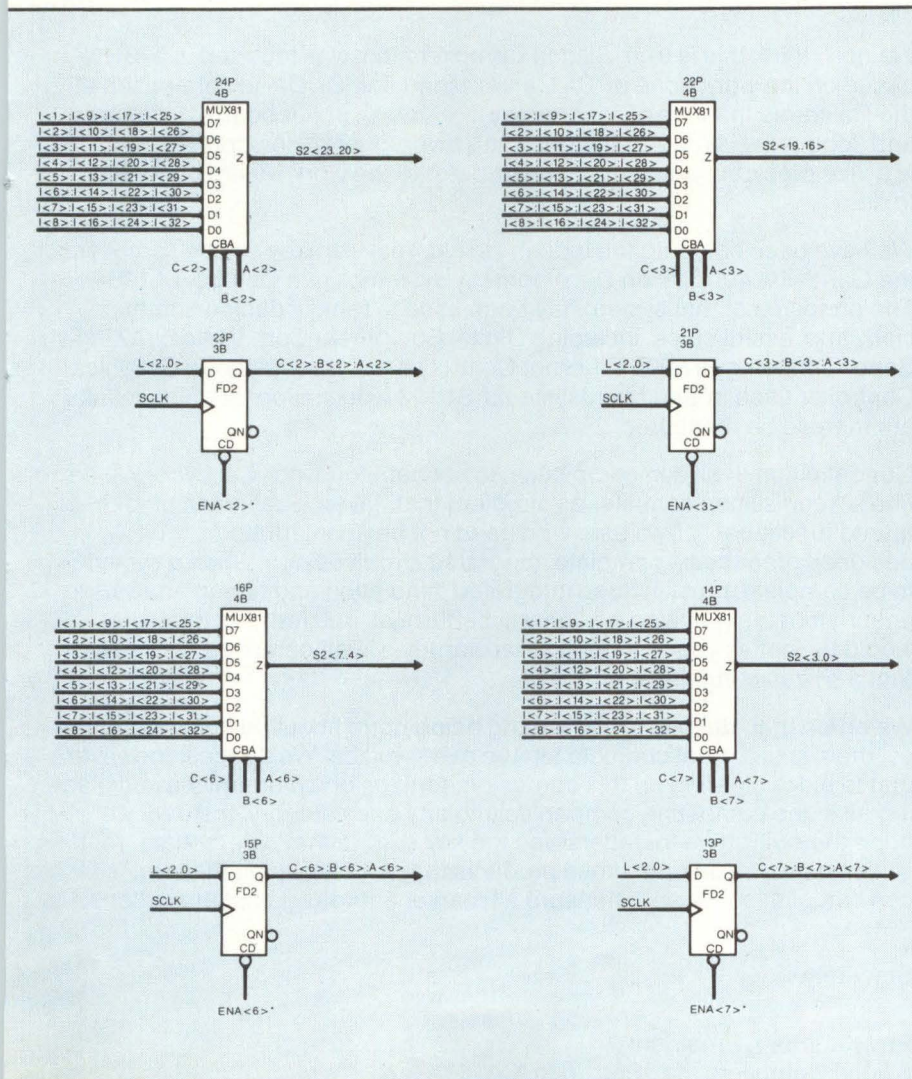
impossible. We recommend requesting the course notes and manuals beforehand as well as inquiring about which sections are most important to study. (If LSI Logic is your vendor, request the CMOS Macrocell manual. If you plan to use Valid's Scaldsystem I, request Volume I of the design manual and look over the timing verification and simulation sections.) This is especially true in the case of the workstation.

Operating Valid's workstation requires no prior knowledge of UNIX although a UNIX background would be very helpful. All necessary UNIX commands are covered in the course, but this overview is hardly adequate to fully exploit the flexibility that the operating system offers in typical design situations.

Prior to attending either the workstation or gate array course, familiarity with your circuit is invaluable. Knowing this beforehand may be impossible, but if you have a clear idea of how the logic is to be implemented, questions posed can relate directly to how the circuit is to be implemented when using the workstation and cell library.

We found the Valid Logic course was well presented and organized. Plenty of time was allotted for hands-on experience and the instructor had a strong appreciation for the design problems typically encountered by systems architects and engineers. Consequently, most questions were adequately fielded.

Part III Preview

In Part III of this series we will report on the timing verification aspect of the design and analyze the difference between LSI Logic's Design Verifier and Valid's timing verifier. Since the former costs an extra $28,000, we will compare its capabilities with respect to Valid's offering. We will also look at other workstations on the market and make some comparisons among the various features. The remaining stages of the design cycle will be scrutinized, and we will offer some general guidelines for the designer as well as our own conclusions about designing a gate array on a workstation.   **DD**

To the Editor:

In the "Editor's Comment" section of *Digital Design's* November 1984 issue, you present a dictionary definition of a silicon compiler. You define it in a box at the top of the page as, "1. a nebulous term used to describe a system that automatically synthesizes integrated circuits. 2. a term primarily used for marketing hype."

This definition, though obviously tongue-in-cheek, concerned me. After reading the entire piece, however, I realized that I was in complete agreement with what I believe you were attempting to say. It is a fact that there has been a great deal of positive response (including *Digital Design's* August article entitled "Silicon Compilation: A Revolution in VLSI Design") to the introduction of silicon compilation as a tool to help systems engineers design efficient VLSI chips and get products using those chips to market sooner than their competition.

The widespread demand for such a tool has crowded the design-automation market with a number of companies offering what they call a silicon compiler. I agree with your point that the prospective buyer should understand exactly what is meant by silicon compilation and just what each company offers; however, the way that point is presented in your piece suggests that *all* existing silicon compilers are nothing more than marketing hype.

We don't think this is true. Silicon Compilers Inc. was founded in 1981, based on the work done by Dr. Carver Mead and Dr. David Johannsen at the California Institute of Technology. Mead sits on our board of directors, and Johanssen, who is credited as the inventor of silicon compilation, is a vice president and a major contributor to the work we are continuing to do.

We have been shipping the industry's first "real" turnkey silicon compiler, the Genesil™ 400 Silicon Development System, since October of 1984. The prototype of that system has been used to rapidly design commercially successful chips, including Digital Equipment Corp.'s MicroVAX™ I, Seeq Technology's 8002 Ethernet Controller and the RasterOp Graphics Controller used in Sun Microsystems' SUN 2 workstation line. The results are there to be measured.

Our definition of silicon compilation is not nebulous, nor is it hype. We define a "real" silicon compiler as a system that, given a definition of required functionality by a user who need not be an integrated circuit designer, produces a complete integrated circuit design. Such a system, to be complete, must include integrated simulation and timing analysis to ensure that the resulting design will perform as desired. Anything else would be, not as you put it, a "garden variety silicon compiler," but rather "not a silicon compiler at all."

We agree that, despite all the writing being done about this new technology, there is still great confusion in the marketplace. We suggest, however, that to aid in clearing up this confusion, the design community avoid placing all of the competing companies into any one category. Instead, we hope they will strive to understand the key criteria that differentiate "real" silicon compilation from those products that simply exploit the term "silicon compilation" — and measure all market entries against that criteria.

Sincerely,

Phil Kaufman, President
Silicon Compilers Inc., San Jose, CA

Systems Architect's Guide To UNIX/VMS

by Dave Wilson, Executive Editor

Over the past few years, the industry demand for a standard operating system has led to the widespread use of UNIX. Today, different factors trigger interest in the UNIX operating system, many of which are more marketing issues than technical considerations. For instance, since numerous college graduates have gained experience with the UNIX operating system, a given engineering operation may find it easier to locate UNIX programmers than individuals with knowledge of a proprietary operating system, such as VMS. Or, it may be that the portability issue, moving the operating system from one processor to another, is considered important. Unfortunately, the marketplace offers so many different versions of UNIX, the idea that UNIX can provide portability is somewhat misplaced. These different versions emerged, primarily because users put pressure on systems manufacturers to provide enhancements that were not supported by the original release from AT&T.

UNIX has always been a good match for a system software development environment since it provides a file system that is targeted almost exclusively at that environment. VMS, on the other hand, is targeted towards a much broader range of applications and has a much wider variety of file system characteristics.

Both VMS and UNIX are interactive time sharing systems, in which the user types a command and receives a response from the operating system. They resemble each other much more than either resembles IBM's TSO time sharing system. Both systems are based on a kernel that performs file management, process scheduling and I/O services. Running outside the kernel is a command language interpreter that provides the

user with access to the kernel services either with prewritten commands and programs or by facilitating the writing of programs. Some of the general aspects of these systems are similar. Both have hierarchically organized file systems and terminal handlers with similar capabilities and functionalities. However, other details of the system are widely divergent. Several features of VMS, such as dynamic loading and shared libraries, UNIX lacks, and some features of UNIX, such as pipes and device independent I/O and Job Control, VMS lacks. The grammar of the command languages are almost completely different in detail, as are the file naming conventions, most command names, editors, language dialects and specific philosophies of system design.

Every time sharing system has its own idea of what commands are acceptable to

its command reading program. The function of a command interpreter is to execute the commands that the user enters. On the VAX/VMS, there are two command language interpreters, DCL (Digital Command Language) and MCR (Monitor Console Routine). The chief difference is the way they treat indirect files.

The command interpreter on the UNIX system, known as the shell, comes in two varieties—the Bourne shell (after its author) and the C shell which provides many more features and options. Some computer systems have a simple and effective interactive command interpreter, but they lack the ability to program sophisticated command sequences. Other computers have elaborate command level programming languages but no provisions for simply running a program. The UNIX operating system com-
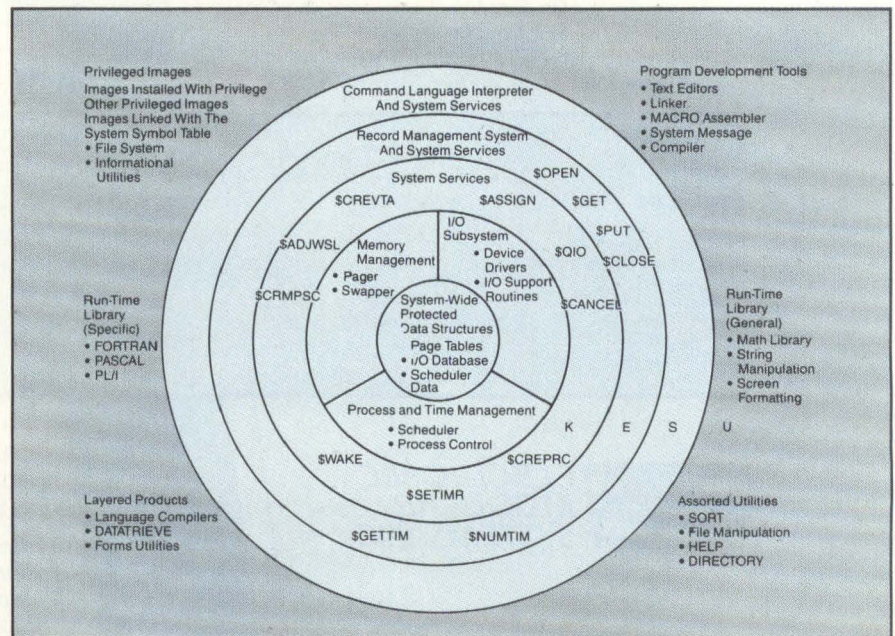
Figure 1: Layered Design of the VAX/VMS Operating System.

More sophisticated features are being added to UNIX that make it more VMS-like.

bines both abilities in the shell.

One difference between Version 6 and Version 7 of the UNIX system is the shell. The Version 6 shell is a good interactive command interpreter but a weak programming language. The Version 7 shell combines all of the Version 6 interactive features with a better programming language. Nevertheless, neither UNIX nor VMS is a truly interactive program development tool. With the exception of interpretative languages such as BASIC and APL, the task of program development still involves preparing a source program, running a compiler program on the source file, linking an executable file and running it.

The major development language on virtually all UNIX systems is the language C. Almost all UNIX system software is written in this language, with only small critical sections resorting to assembly language. This strategy has resulted in the number of UNIX implementations on different microprocessor families. The Berkeley distributions of UNIX provide other languages such as Fortran 77, Lisp and APL. DEC now supports the C language and offers it for both VMS and VAX Ultrix, a Berkeley version of UNIX.

The kernel is the memory resident portion of an operating system. Compared to other operating systems, the UNIX system kernel provides a relatively small repertoire of services. The UNIX kernel consists of two major parts—the process management section and the device management section. The process management section allocates resources, schedules processes and honors process requests for service. The device management section supervises the transmission of data between the main memory and the peripheral devices. The device management section for a given computer contains a module for every peripheral device that is attached to the computer. Each time a computer is attached to a new type of I/O

peripheral, a program module has to be added to the device management section. Whenever the UNIX system is moved to a different type of computer, the device management section has to be largely rewritten because different computers usually have different peripheral devices with different control principles.

The kernel also maintains a set of tables that coordinate the actions of the interrelated threads of execution. Most of the kernel's work concerns maintaining and modifying these tables. Like UNIX, the VMS operating system kernel also includes a process management section and a device management section as well as a memory management subsection.

The I/O subsystem consists of device drivers and their associated data structures, device independent routines within the executive and several system services. The scheduling and process control section selects processes for execution and removes processes from execution that can no longer execute. The scheduler also handles clock servicing and includes time-related services. Possibly the most important part of the VMS kernel is the memory management subsystem.

Currently, AT&T's UNIX System V does not support virtual memory. Unless the user implements UNIX with Berkeley enhancements, it is impossible to run up to anything larger than the physical size of memory in the system. But with VMS, as its name implies, the concept of virtual memory has always been an important one.

The main components of the memory management subsystem are the page fault handler, which implements the virtual memory support of the VAX/VMS operating system, and the swapper, which allows the system to more fully utilize the amount of physical memory available.

From the users point of view, UNIX and VMS file systems are organized similarly, in that both systems present the files as a hierarchical tree structure. This

tree structure contains a root directory that is simply a special file containing the name and address of other files. The directory is said to contain other files. Since these files can also be directories, the entire structure can be represented as a directory tree.

In VMS, there are several directory trees, one for each mounted disk volume. In UNIX, there is only one directory tree, with each disk volume represented as a subtree or directory somewhere in that tree. Beyond this, the two systems are nearly identical in their file hierarchies. However, the way a user refers to a file or names a file differs greatly between VMS and UNIX. In UNIX a directory is always referred to in exactly the same way as any other file. In VMS, however, the distinction between directory-as-directory and directory-as-file can lead to confusion.

Record locking has been a major problem with the UNIX system for some time. Two users may access the same file and write to it at the same time, scrambling the information contained within it. The /usr/group, an independent body for the UNIX community has, however, proposed a file locking technique that will be adapted in the future by AT&T. One of the features of UNIX is the association of all the I/O hardware with special files. Access to I/O hardware itself mimics access to ordinary disk files. Each I/O device has at least one special file. A program can access a special file in order to actually access the I/O hardware.

In many ways VMS is a more adult operating system than UNIX. Many of the features that make UNIX more "VMS-like," such as real-time processing and virtual memory capability, have come out of Berkeley. This has created two different types of UNIX in the marketplace, UNIX System V and Berkeley UNIX. Also, VMS, a proprietary operating system, is a lot further down the road in terms of being able to support advanced computing features. A main emphasis at DEC has been to support VAX clusters or the connection of a number of VAXes and mass storage controllers in a multiprocessing environment. Several new features of VMS Version 4.0 introduced the provision for increased data sharing and enhanced data and system availabilty.

A distributed File System, for example, allows all VAX processors in a cluster to share disk mass storage. A dis-

tributed Job Controller provides a form of load balancing across processors since a batch job distribution algorithm numerically balances the batch jobs over the VAX processors. The advantages of dynamic load balancing and dynamic load splitting are obvious to those designers of UNIX-based machines as well.

In many cases, multiple CPU systems that feature fault-tolerant operation that are UNIX-based have been announced, but this has been achieved through a totally rewritten UNIX kernel. A totally rewritten UNIX kernel may not have the same system calls as the original UNIX, and compatibility will be lost. A program ported from one environment will not run in another. Nevertheless, if the user only interacts with the shell and utilities, a rewritten kernel may provide enough similarity between the original UNIX to be considered compatible. In this instance, the portability of the UNIX operating system is more with the programmer than with the system itself.

As well as supporting the VMS operating system, Digital Equipment announced a version of the UNIX operating system, Ultrix 32 for its range of mid- to high-end VAX family and Ultrix-32m for the Micro-VAX 1. The user command language interface for the Ultrix-32 system is provided by two user-selectable command language interpreters—the Version 7 Bourne Shell and the Berkeley C Shell. Programming languages include C, Fortran 77, Pascal, FranzLisp and UNIX assembler.

The Ultrix-32 has two line-oriented editors and a screen-oriented editor. The system provides a file transfer utility as well as a backup/restore, file system integrity checking and bad storage block handling capabilities to protect stored data. The Ultrix-32m is the newest member of Digital's family of Ultrix products that currently run on larger machines. The product brings the Ultrix-32 operating system to a microcomputer environment, enabling users with larger systems to expand programming operations to the low-cost Micro-VAX 1 computer. Ultrix-32m has compatibility with Version 4.2 of Berkeley 4BSD, Ultrix-1.1 Version 2, and AT&T System V.

Ultrix-32m is a subset of Berkeley 4BSD UNIX and is supplied with two command language interfaces, UNIX Version 7 Bourne shell and Berkeley C shell. Version 2.0 of Ultrix-ll was an-

nounced concurrently with Ultrix-32m. The new version has been improved to provide hardware support for the Micro PDP-ll/73 computer system. In addition, Digital announced Version 1.0 of DEC/Shell, a command line interpreter that provides users with an interface similar to the interface on a UNIX V7 operating system. To a user, the DEC/Shell environment appears like the V7 Bourne Shell.

Over half of the existing licensed UNIX systems are based on the Xenix operating system from Microsoft that is based on the UNIX Version 7 and System III. Offering the same features as System V, it has allowed a UNIX-like environment to be implemented on personal computers. DEC also offers support for its Professional 300 workstations in the form of the VENIX operating system. The VENIX product is based on Version 7 and, like the XENIX system, includes some functions of the System V version. VenturCom, developers of VENIX, also offers layered application software to run under its VENIX system, such as spread-

sheet, wordprocessing and relational database programs.

Undoubtedly, UNIX is gaining a great deal of impetus in the marketplace, mainly, because there is a need for a portable operating system. The enhancements coming out of Berkeley have done a great deal to make the operating system more flexible and user-friendly. It would appear the Berkeley version of the operating system is becoming a standard in the scientific and technical environment. UNIX has a great deal of catching up to do before it rivals the sophistication of the VMS operating system from DEC. Enhancements that are and will be made in the future seem to point to more VMS-like features being incorporated. **DD**

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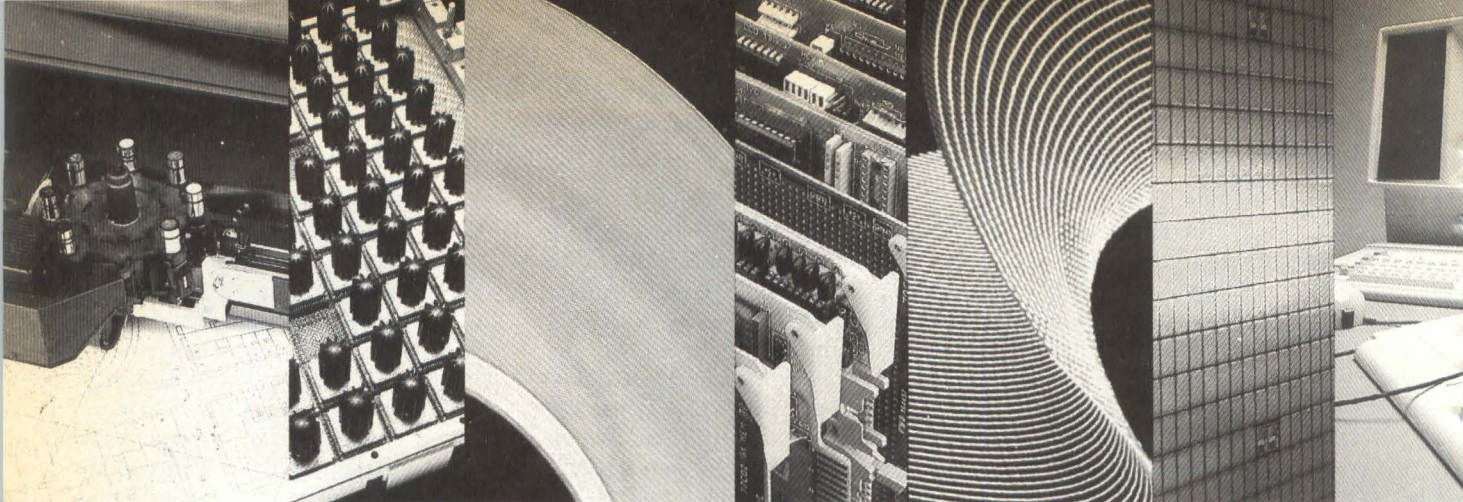
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Compiled by Sherri Mack and Winnie Jenkins Rubino

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Caching Disk Controller Relieves System Bottlenecks. The primary technical problem to overcome during the design of a caching disk controller is the limitation on cache access time. Sept., pg. 102.

The Design Of A High Performance Multibus Memory Board. FAST logic circuitry and a discrete logic RAM controller contribute to speed. Jan., pg. 78.

Designer's Guide To The IEEE 488 Bus: New Life For An Old Workhorse. Wider applications for the GPIB will now impact the systems integrator. Jan., pg. 53.

Designer's Guide To The Multibus. The Multibus has found commercial acceptance in the industrial, scientific and commercial marketplace. April, pg. 67.

Designer's Guide To The STD Bus. The range of applications for STD products continues to grow, mainly in automation, process control, monitoring and data acquisition areas. Sept., pg. 63.

Designer's Guide To The S-100 Bus. One of the differences between the Multibus and the S-100 is in current applications. Unlike the Multibus, the S-100 is a development/commercial systems bus. July, pg. 71.

Designer's Guide To The Q-bus/Unibus. The Digital Storage Architecture and Mass Storage Control Protocols may present problems for third parties trying to emulate DEC designs. Oct., pg. 67.

Designer's Guide The VME Bus. The push toward higher performance systems is now evident in the industrial automation world and inevitably, 32-bit buses have emerged to provide a solution to the systems architect looking to upgrade. Dec., pg. 44.

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Local Area Networking Becomes A Standard Feature. No single network medium, access method or set of protocols will be the "standard" over the next several years. March, pg. 70.

Industry Review: Universal Access Boosts Value Of Data & Systems. As VLSI technology profoundly changes the configuration of computer systems, it is impacting communications as well. Dec., pg. 36.

Tackling Design Environmental Issues. Sophisticated workstations have sparked debate over whether to base the design environment on a mainframe or a network of self-contained workstations. July, pg. 100.

Widening Communications Environments Spark Innovation In Modems. A demand for communications for new terminals and computers will keep the growth of the modem industry steady for at least several years. Jan., pg. 40.

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AI Makes The Transition From Theory To Practice. AI becomes an advanced problem-solving methodology used to answer practical problems in the real world. Oct., pg. 78.

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Defense Electronics And Industry Synergism. Military electronics is broadening as the push for advancements creates collaborative efforts between commercial enterprise, university research and the Department of Defense. June, pg. 100.

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Display Functions Migrate To Graphics Devices. Today the traditional display processor's tasks are divided into raster processing, vector generation, software or firmware processing and, in some cases, databased processing and interaction. May, pg. 65.

The Expanding Realm Of The IBM PC. The IBM Personal line is invading a range of markets formerly the territory of dedicated machines. Feb., pg. 80.

Function Determines Form In Workstation Ergonomic Design. Design processes now include human factors evaluation labs which can specify variables affecting human behavior and design performance. Sept., pg. 96.

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Industry Review: Multiple Bus Structure And Custom Chips Increase Multiuser System Performance. When looking at multiuser systems, it is important to look at the architecture of minicomputers to discover which of their features small systems emulate. June, pg. 54.

Industry Review: Trends And Developments In Engineering Workstations. CAD/CAE users demand fully integrated systems, portable software and a full line of engineering application programs. Oct., pg. 54.

Modular Architecture May Be The Next Array Processor Design. Array processors can be categorized as those that perform floating point operations and those that carry out block floating point and fixed point calculations. May, pg. 50.

New Architectural Designs Push Fault-Tolerance Into The Market. Fault-tolerant machines may be suitable for the commercial or business environments or the industrial environments. June, pg. 122.

Parallel Processing Meets Computationally Intensive Requirements. As AI applications increase, computational requirements will be staggering and the use of multiple processors will be inevitable. April, pg. 122.

Process Control: Intelligence Moves To The Factory Floor. To compete with the low labor cost and huge production volumes of offshore industries, US companies look to computer technologies for help. Sept., pg. 74.

UNIX Standards Move To The Forefront. UNIX has various implications for the entire computer industry including OEMs, users, value-added resellers and manufacturers. Feb., pg. 122.

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Designing Printed Circuit Boards From The Workstation. The newer generation of CAD products for PCB layout are designed to optimize the use of not only computer power, but also the knowledge and skills of the board designer. April, pg. 86.

Device Level Intelligence For Graphic Systems. There is a need to off-load graphics functions from the over-burdened host to the graphics device. May, pg. 98.

Display Processors—Where Fast Isn't Fast Enough. New display processor technologies offer graphic designers an ever increasing choice of possibilities for creating the next generation of low cost, high performance computer graphics systems. July, pg. 94.

Graphics Research Points Toward Fifth Generation Systems. Different applications of graphics have individual requirements which create disparate design approaches. Jan., pg. 68.

Industry Review: Building Graphics Systems From The Board Level. The graphics board integrator is faced with a major choice: which system interface bus to use. Aug., pg. 46.

Industry Review: Graphics Terminals. Describing the design changes in graphic terminals is difficult because of the great diversity of performance and functionality. Feb., pg. 42.

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Making Fast Faster: The Design Of A Small Graphics System Enhancement. A new board designed to speed up terminals with a large installed base is worth the effort in meeting users' demand. June, pg. 128.

Microcomputer-Based CAD Provides Low Cost Design Tools. Product developments and associated upgrade devices provide micro-based CAD systems with performance levels rivaling those of more expensive dedicated systems. Jan., pg. 74.

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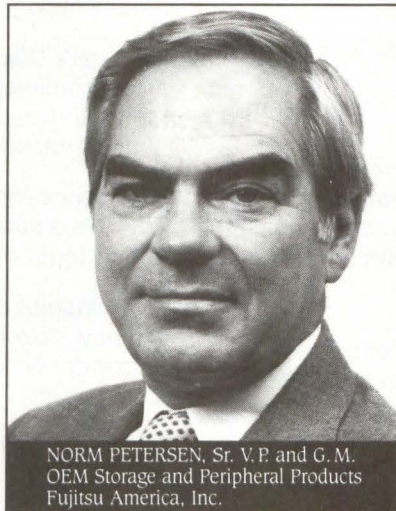
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High-Performance Event Interface For A Microcomputer. As silicon technology advances to provide denser geometries, timer structures have become more elegant and powerful. Feb., pg. 110.

Integrated Circuits: Advanced Microprocessor Designs Will Rely On OS Support. Programmable, semi-custom and custom logic will be used in the design of advanced computer systems. Feb., pg. 90.

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Industry Review: Silicon Support For Solid Modeling. Graphic manufacturers are depending more on applications-specific VLSI to perform demanding tasks in solid modeling. Sept., pg. 54.

32-Bit ICs Enhance Array Processor Performance. The need for virtual memory support, increased memory bandwidth and improved precision means a growing demand for 32-bit performances. Dec., pg. 61.

32-Bit Microprocessors Support Parallelism And Cache. The implementation of pipelined architecture, cache memory and memory management on 32-bit chips is unique to manufacturers. Aug., pg. 96.

Silicon Compilation: A Revolution In VLSI Design. Silicon compilation is the realization of computers designing computers. Aug., pg. 88.

Designing With EEPROMs. Most EEPROM applications include single-chip microcontrollers, so the combination of EEPROM on-board was a predictable step in the evolution of EEPROMs. Sept. pg. 108.

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Intelligence Migrates Toward Small Systems Peripherals. There is a steady trend toward equipping disk storage subsystems with intelligence. March, pg. 92.

Microfloppies Squeeze Their Way Into The Market. There are now dozens of companies with announced microfloppy drives and few manufacturers producing media. Oct., pg. 88.

Mid-Size Winchesters Succeed Quietly. Despite the popularity of 5¼" micro-Winchester disk drives, 8" and 14" drives continue to outsell 5¼" drives. Jan., pg. 62.

PCMs Track The Leading Edge Of Winchester Technology. Plug-compatible manufacturers (PCMs) compete with IBM for both end-user and OEM market share. April, pg. 54.

Refined Media Extend Magnetic Recording Capabilities. Refinements in materials and processes for manufacture are providing substantial increase in media capacity. June, pg. 88.

Mass Memory For Tight Spots. Demand for higher performance PC and more compact desktops has spurred a demand for smaller, lower power disk and tape drives. Aug., pg. 78.

Optical Disk Technology Creates A New Class Of Peripheral. Optical disks offer higher density than magnetic memory with more bits and more tracks per inch. Aug., pg. 68.

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Designer's Guide To Uninterruptible Power Supplies. To ascertain the quality of the power output, it is necessary to have some familiarity with the nature of the problems that may exist. Aug., pg. 59.

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Color In Hardcopy Device Development. Most users or systems integrators are looking for a low-cost, reliable, high-quality, easy-to-use hardcopy device. July, pg. 80.

Electrostatic And Vector Plotter Developments. Advances have been made in simplifying designs, cutting component counts, raising performance and reliability, and making them easier to use. June, pg. 108.

Dot Matrix Printers Approach Letter Quality. Dot matrix printers emerge as intelligent devices for high speed, color graphics and word processing applications. Oct., pg. 96.

Industry Review: Demand Heightens For Color Printers. As output moves from monochrome to color, users place emphasis on devices that offer higher quality images. Nov., pg. 48.

Software

Extensions And Performance Improvements Keep Pascal Competing. Many in the industry feel Pascal isn't a very good example of structured programming when applied to "real world" programming problems. Aug., pg. 106.

Solid-State Memory Developments Continue Apace. The development of new types of memory promises to generate improvements in computing. April, pg. 110.

Software Strategies Control Micro Market. The principal issue separating the winners from the losers in the vendor shakeout will be the quality of the software. Jan., pg. 90.

Terminals

Monochrome Terminals—Compatibility Vs. Emulation. The difference between compatibility and emulation can spell disaster to an OEM. Nov., pg. 78.

Trends In Flat Information Display Technology. The flat CRT will likely enter the market in this decade, mainly for desktop and/or transportable computers. May, pg. 122.

Test Equipment

Bypassing In-Circuit Test Of Microprocessor-Based Boards. In-circuit testing does everything that continuity testing does but more. March, pg. 106.

Development Tools Take Aim At 32-Bit Chips. Although much has been published about the capabilities of 32-bit microprocessors, the market still belongs to 8- and 16-bit chips. Sept., pg. 86.

In-Circuit Programming: A Solution To Several Design Problems. In-circuit programming allows the installation of blank EPROMs and PROMs onto the printed circuit board and after complete assembly, the entire board is programmed. July, pg. 84.
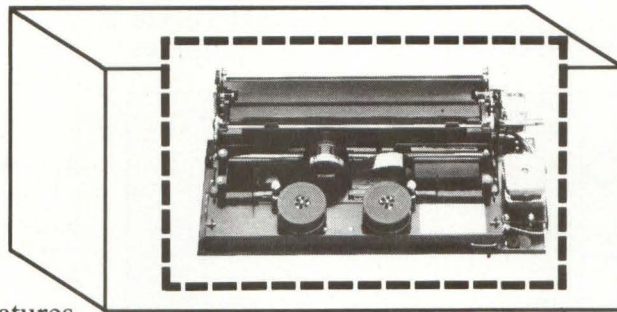
1984 Salary Survey. Prospects for engineering professionals remain bright, with predictions showing the demand will have increased 40% between 1978 and 1990. Dec., pg. 56.

Signal Processing Without A Multiplier

by Sidhartha Maitra and Munsi Alaul Haque, Advanced Micro Devices, Sunnyvale, CA

Although multipliers and signal processors with multipliers are becoming increasingly available, a novel and cost-effective alternate method is to use a logarithmic representation of the data and a high-density Read-Only Memory (ROM) for arithmetic. With this approach, any general-purpose 8- or 16-bit microprocessor can be transformed into a real-time system that can process audio band signals. **Figure 1** shows the basic system with the three main components: the A/D, D/A in the Am7901A, the microprocessor and the high density ROM.

Types of equipment and applications that currently use digital signal processing, but do not need the high precision signal-to-quantization ratio (SQR) possible with linear 16-bit multiplier-accumulators, include speech synthesis, speech compression, speech analysis—coefficient estimation/pitch detection, spectrum analysis, fast fourier transforms, filters, echo-cancellation and modems.

These signals must be able to be adequately processed by an 8-bit system. All voice-grade signals fall into this category. To ensure adequate SQR over a large dynamic range, a logarithmic quantization is generally used for the 8-bit digital representation. The compression/expansion (companding) process (Mu-Law or A-Law) results in the same SQR as 12-bit linear quantization.

The most cost-effective A/D and D/A converters for the front end of telecommunications, voice and modem systems are combination codec/filters (COMBO) chips that convert analog signals directly to and from an 8-bit Mu-Law digital representation. The Am7901A, also known as the Subscriber Line Audio Circuit (SLAC), is one such device. The SLAC performs the codec and filtering functions necessary for the analog interface of the DSP system to the analog world.

Design Concepts

Unlike other COMBO chips capable of performing the same function, the SLAC uses a high sampling rate A/D and D/A converter that simplifies the antialiasing filter. Internally, the SLAC uses digital signal processing and has programmable gain and filters in the receive and transmit paths. The settings and coefficients can be controlled by the microprocessor. This process control can be advantageous in speech processing applications because pre-emphasis and de-emphasis filters as well as gain adjustments can be made before the digitized signal reaches the microprocessor.

When digitized signals from the SLAC are processed with standard multiplier/accumulators, they must be converted from the logarithmic domain to a linear representation. When performing the same operation via table look-up in a ROM, no transformation is necessary and the two 8-bit inputs for multiplication can form a 16-bit address for the answer. The key difference between a conventional linear multiplier/accumulator approach and the one proposed here lies in the representation of the signal samples prior to, during and after the multiplication operation. If the logarithmic domain look-up multiplication table is designed with care, the signal processing chain can preserve the SQR for all the intermediate stages between the input and the output at an equivalent 12-bit linear representation.

The task at hand will usually dictate whether the answer in the ROM table should be in the linear or the logarithmic domain. For instance, in filters with a large number of taps, one might wish to accumulate the sum of products as 16-bit linear values; the values can be accumulated in 16 or higher bit precision within the microprocessor. The microprocessor usually will be able to perform addition at speeds sufficient to keep up with the signal flow. When the answer is accumulated as a 16-bit linear result, the Am7901A also allows the option of creating an analog output directly from the linear representation.

If, on the other hand, filters are implemented with a smaller number of stages, it might be sufficient to operate with an 8-bit companded answer. For a 1 Mbit ROM, the other half of the table can then be reserved for the results of the addition of two 8-bit, companded input values. Thus, half of the table is used for multiplying and the other half for addition. Using Am27512s, two EPROMs will be necessary for the complete multiplication and addition tables.

The advantage with such a scheme is that the data remains in the logarithmic domain from the point of conversion to the point of being sent back out to the SLAC chip for transformation to the an-
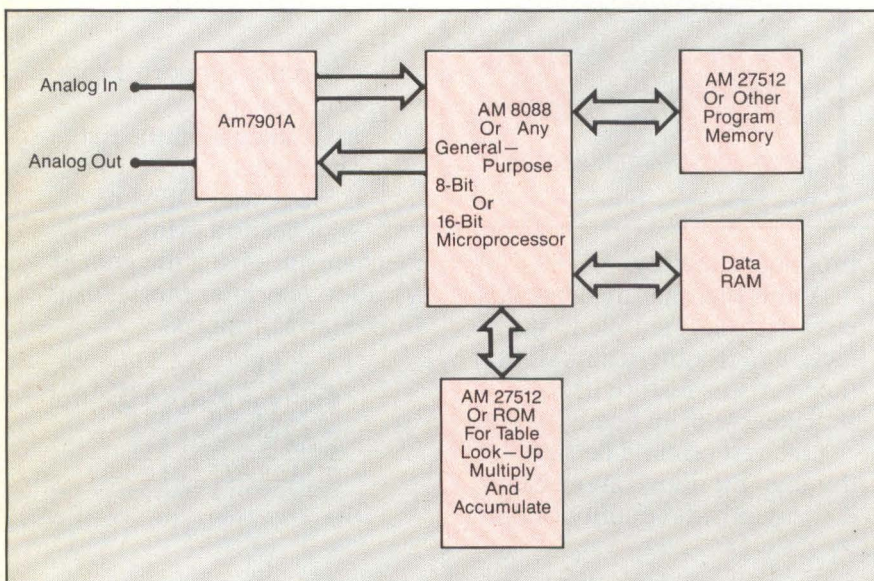

Figure 1: General purpose signal processor using ROM look-up, microprocessor and A/D, D/A SLAC front-end.
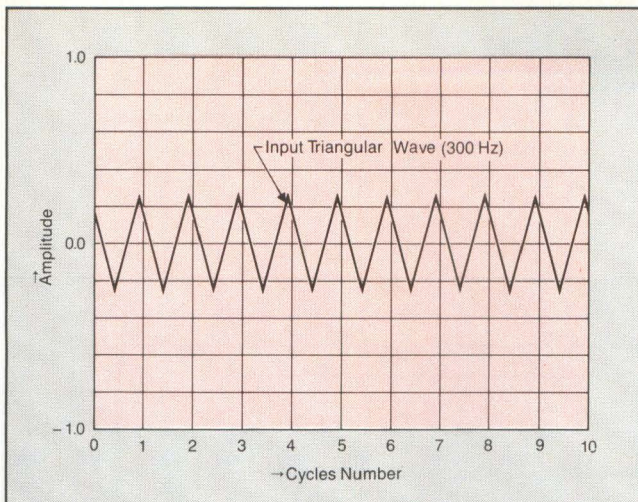
Figure 2: 300 Hz triangle wave used as input for simulation of a filtering application.
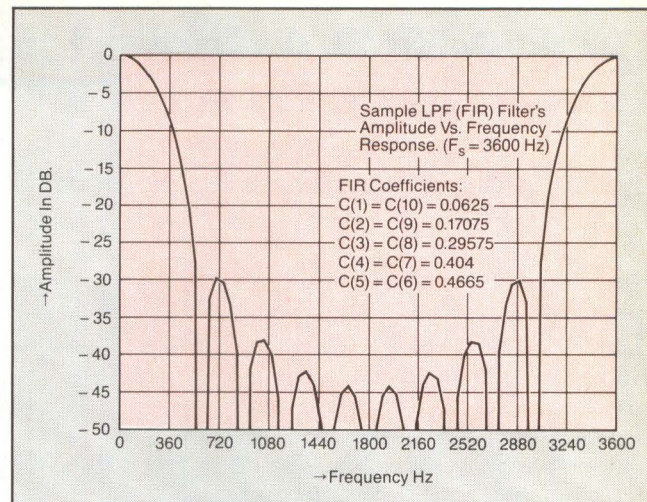

Figure 3: Sample Finite Impulse Response filter's amplitude vs. frequency response ($F_s = 3600$ Hz).

alog domain. All arithmetic, multiplication and addition, is performed by forming a 16-bit address from two 8-bit operands and using this address to locate the answer in the ROM table.

The processing speed of the arrangement shown in **Figure 1** is limited by the slower of the microprocessor instruction cycle time and the ROM access time. Using the set-up described, with an analog sampling rate between 8 and 10 KHz, a reasonably fast microprocessor (like the Am8088, running at 10 MHz) coupled with the 200 nsec Am27512s can perform approximately 100 multiplies and adds per input sample. In a speech compression application, the simple system described here can operate in full-duplex, providing coefficient estimation, pitch detection and feedback synthesis. In this

application, an LPC-10 algorithm can be implemented with five ICs. As an added bonus, the general-purpose microprocessor used in the system can be time-shared for housekeeping and interfacing chores.

Experimental Verification

The potential power of table look-up signal processing was experimentally verified by computer simulation of a simple filtering application. A 10-tap Finite Impulse Response (FIR) was convolved with a 300 Hz triangular wave. This convolution was done two ways: 1) with floating point 32-bit precision for all arithmetic and 2) with Mu-Law representation of the data and the filter coefficients and a simulated 1 Mbit ROM (16-bit input and 8-bit output) table look-up for multiplying and adding two 8-bit Mu-Law quantities.

Figure 2 shows the input triangle wave and **Figure 3** the low pass filter frequency response for the 10-tap FIR coefficients. Since the cut-off for this filter is at the fundamental frequency of the triangle wave (in this case at 300 Hz), the harmonics are eliminated by convolution with the FIR filter. As shown in **Figure 4**, there is only a very slight difference in the output of the filter with floating point calculations and with table look-up arithmetic.

Operations performed on analog voice frequency waveforms do not usually need more than 1% SQR accuracy. In such applications, a table look-up digital signal processing approach is less expensive than higher-precision linear multiplier/accumulator implementations with comparable performance.
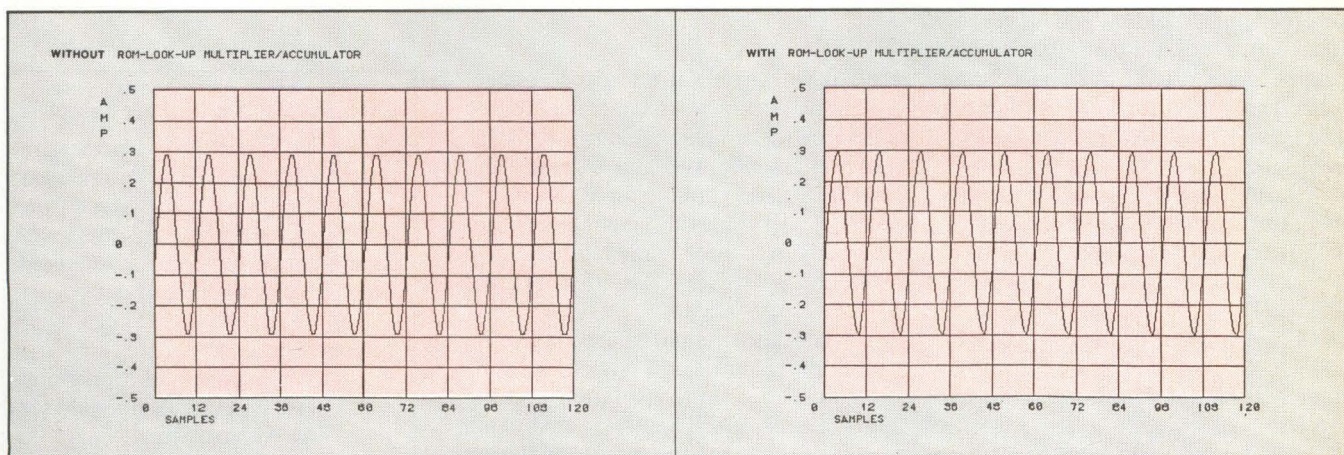
Circle 230

Figure 4: Graphs of a low-pass filter output, left: implemented with 32-bit floating point precision, and right: using Mu-Law representation and the ROM look-up multiplier/accumulator are very similar.

Dual 12-Bit D/A Converters Reduce Board Space By A Factor Of Two

by Mark Logan, Analog Devices Inc., Norwood, MA

Digital components have provided increased PCB density through the availability of 256K RAMs, programmable array logic and increased functional density of microprocessors. DACs with multiple converters on the same IC save board space for designers. However, these have been limited to the 8-bit resolution range until the introduction of Analog Devices' dual 12-bit D/A converter, the AD7549.

Improvements in CMOS technology have enabled Analog Devices to manufacture two 12-bit CMOS D/A converters on one IC at a cost below two individual 12-bit CMOS DACs with similar architecture. By using high-speed digital logic circuits and the Linear Compatible CMOS (LC^2MOS) process, multiple high-precision analog circuits can be integrated on a chip. The AD7549 is a monolithic dual 12-bit current-output D/A converter, packaged in a 0.3″ wide 20-pin DIP. In addition to saving board space where two DACs are required, the on-chip data latches and control logic for microprocessor interface eliminate the need for external digital support chips.

The DAC in **Figure 1** consists of two 12-bit converters, each with a DAC register, reference input, control logic and an input register structured in three 4-bit nibbles. Data from a microprocessor is loaded in 3 bytes for each D/A converter and then transferred to the DAC register. The microprocessor loads data by using address lines A0, A1, A2 and $\overline{CS}$ (chip select) and $\overline{WR}$ write lines. A logic high level on the CLR (clear) input clears all registers.

The double-buffered structure allows both DACs to be updated individually or simultaneously using the $\overline{UPD}$ input. Precise matching and tracking between the two D/A converters is inherent since both are fabricated on the same chip. Designers can now be assured of closely matched ladder resistances and gain errors.

Each converter operates as a unipolar-2-quadrant or a bipolar-4-quadrant multiplying D/A converter when sup-
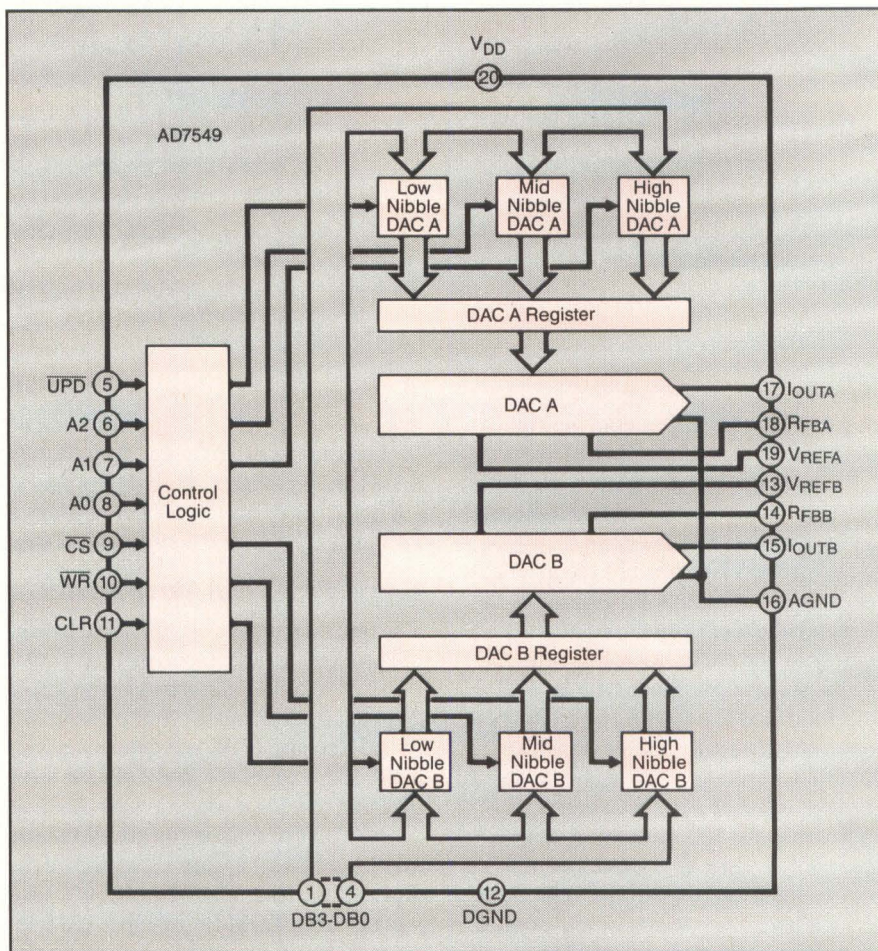
Figure 1: Block diagram of the AD7549 dual 12-bit DAC IC.

plied with external reference voltage. Relative accuracy is guaranteed over the devices' full temperature range: ± 1LSB, maximum, for A, J and S grades and ± ½LSB, maximum, for B, K, and T grades. All grades also guarantee monotonicity over three temperature ranges: 0°C to +70°C, −25°C to 85°C and −55°C to +125°C.

A key specification, wherever there are multiple channels on a single chip, is the channel-to-channel isolation and the digital crosstalk. The AD7549 exhibits a −70dB channel-to-channel isolation reading. Digital crosstalk is a negligible 10nV-sec.

An application in which the dual DACs in the AD7549 are an advantage is shown in the programmable gain/attenuation circuit in **Figure 2**. The gain of the amplifier in **2A** is set by the ratio of the two resistors R_A and R_B. By replacing each fixed resistor with a D/A converter, a microprocessor can change the gain/attenuation of the circuit. **Figure 2B** shows how the two D/A converters on the AD7549 can be used as variable resistances. By loading DACs A and B with suitable codes, programmable gain/attenuation over the range -72dB to $+72$dB can be achieved. The resultant gain expression for the circuit with $R_{LD}A = R_{LD}B$ is:

$$V_{OUT}/V_{IN} = -N_A/N_B$$

$$0 = D_A = 1$$
$$0 = D_B = 1$$

$$V_{OUT} = -V_{REF}D/Q_B*$$

*If $D_B = 0$, the amplifier is open loop.

Dual converter design eliminates a number of error sources. Since the DACs

Figure 2: Programmable gain amplifier using dual DAC; the gain of amplifier in 2A is set by ratio of the two resistors R_A and R_B. The two DACs of the 7549 can be used to vary resistances.

are on the same chip with gain error D_A/D_B, tracking in the same ratio eliminates any drift errors. Previous circuits have always had to be trimmed to accommodate the DAC 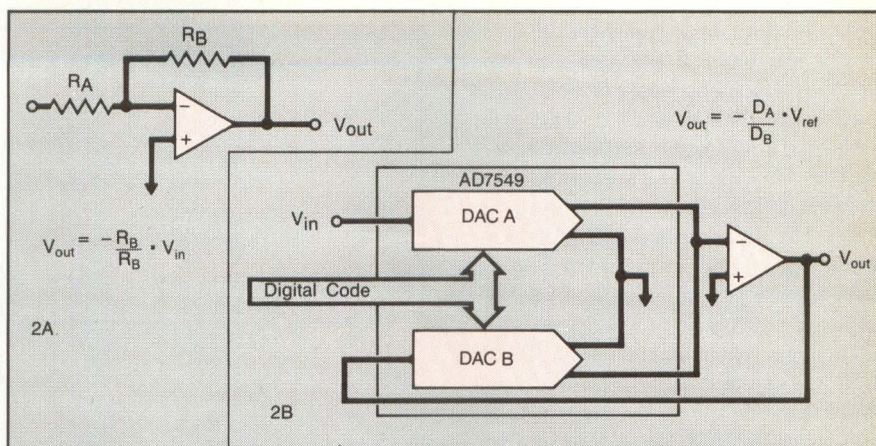ladder resistance which usually has a wide tolerance (from 8K to 20K). With $R_{LD}A$ and $R_{LD}B$ matched to better than 1%, the circuit doesn't suffer from this problem. The circuit also has a constant input resistance of $R_{LD}A$. The two unused feedback resistors, $R_{FB}A$ and $R_{LD}B$ are also precisely matched and could be used to provide other DAC code vs. gain relationships. **Circle 231**

Small ECL Gate Array Improves Data Bus Performance Of FPS-264 Scientific Computer

by Roger Rees, Floating Point Systems, Beaverton, OR

Ongoing architectural improvements are important to keep product lines competitive. Floating Point Systems (FPS) wanted to transform their basic Scientific Computer architecture into a higher performance ECL machine. The application of a small, specially designed gate array, the Fairchild FGE0020, was a significant aid in that design. The FPS-264 enhanced 100K ECL computer offers a minimum of 3.6 times the speed and twice the performance for the price of the earlier FPS-164.

A requirement of this design was for 5 nsec data transfers across a multisourced, multidestination Data Pad Bus (DPBS). **Figure 1** graphically presents the physical length and loading present on this bus. The propagation delay time of the bus is dependent on the length of the line, the transmission line impedence and the load-

ing effects.

The FPS-264 backplane interconnects are mostly of a stripline type, with an unloaded propagation delay of 2.2 nsec/foot or 4.2 nsec over the length of this bus. Initially, this appears to offer an acceptable timing margin compared to the 5

nsec budget, but the stubs can have a catastrophic effect on timing.

If the round trip propagation delay for the stub is less than the rise time of the signal, then the stub can be treated as a capacitive load. Assuming the stubs can be kept within this restriction and further
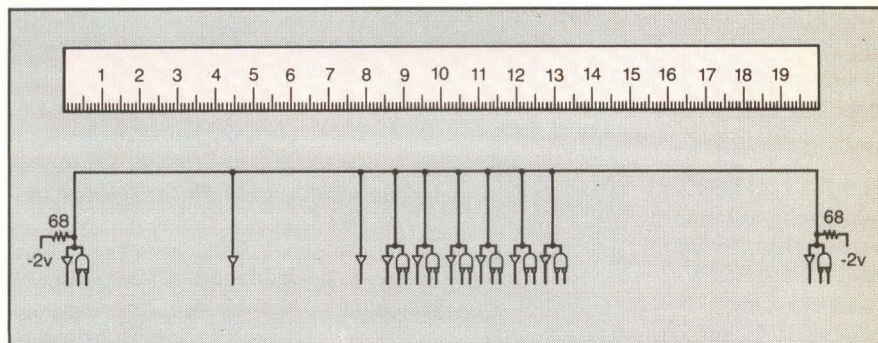

Figure 1: Logical connections of the Data Pad Bus in the FPS-264. Meeting performance goals with the length and loading of this bus provided an engineering challenge.

approximating these capacitive stubs as evenly distributed 10 pF loads along the bus, the resultant propagation delay is 3.0 nsec/foot or 5.9 nsec worst case delay for the loaded bus. This timing is over budget and the stub lengths had to be minimized to prevent further degradation. A 2″ budget for stub lengths (excluding connector path length) was adopted as the shortest reasonable limit for the FPS-264's packaging technology.

The biggest problem in meeting this 2″ limit was presented by the bidirectional loads. Implementing a transceiver function in 100K ECL requires separate driver (100123) and receiver (100122) ICs which, for all practical purposes, prevent obtaining less than 2″ stub lengths. Two ICs also increase the capacitance of the stub load since the majority of the load capacitance is due to the IC package and physical etch.

One solution is to use a single 100K IC. At the projected chip volume, a pure custom part would not be cost-effective; however, it appeared that a gate array would be. The recent emphasis in gate array technology has been on density, but since this part would interface mostly with the standard 100K family, a high density transceiver would have degraded performance by longer interconnect delays when laid out on the PCB.

Since the FPS-264 has a multisourced bus, bus drivers must have 25 ohm drive capability and special low level output characteristics to avoid loading the line when they are not enabled. The FGE0020 gate array from Fairchild had the proper density, but it could not offer the exact function required by the design. Fairchild designers modified component values in the output drivers and eliminated temperature compensation on these outputs. The lack of temperature compensation was not a technical concern since output voltage levels are guaranteed within spec if the junction temperature is at least 25°C. This requirement is easily met under the specified operating conditions for the FPS-264.

The ground lead inductance of the transceiver was a concern with this design. Most high speed ICs use flat packages, leadless chip carriers or similar packaging techniques to reduce parasitic package inductance and increase packaging density to achieve smaller interconnect delays. DIP technology was chosen for FPS-264, however, mainly to lower the manufacturing risks.
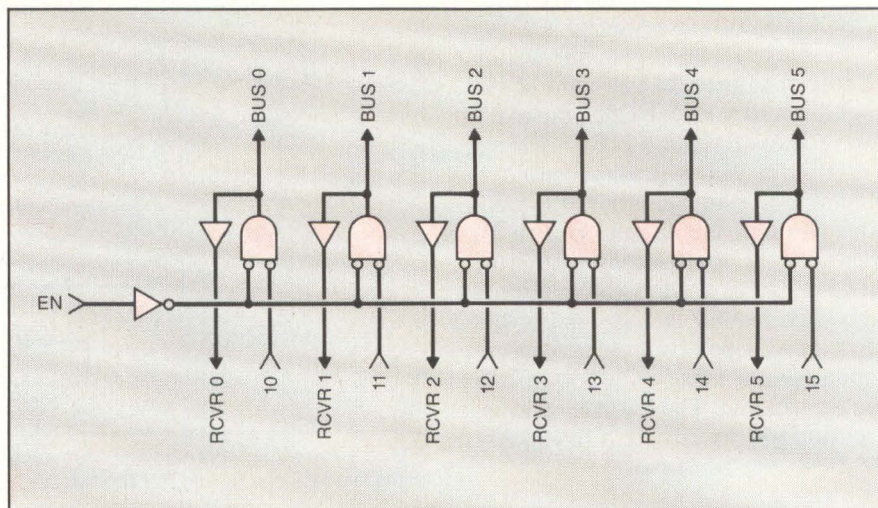

Figure 2: Transceiver logic diagram: although there is no inversion in the bus receivers to combat worst case switching currents and there are 12 unbalanced outputs, designers achieved acceptable performance levels with only three Vcca pins.
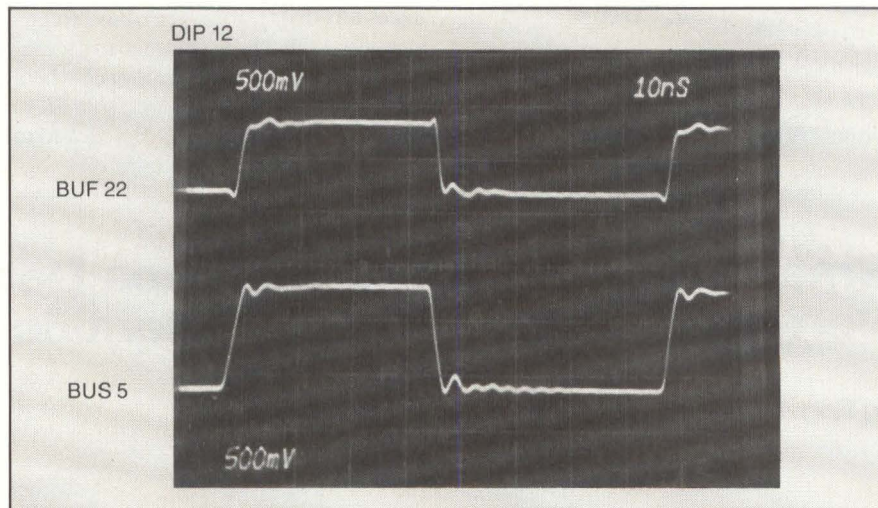
Figure 3: The actual performance of the FGE0020 transceiver gate array under worst case loading conditions with all six bits switching the same direction, all terminated and with added Vtt decoupling.

Figure 2 shows a block diagram of the transceiver function as implemented in the FGE0020. Although it was recognized that having a logical inversion in the bus receivers would be most desirable to help combat the worst case switching current seen on the Vcca pins, the FGE0020 could not accomplish this. As a result, the worst case ground current change in the Vcca pins is about 225 mA (68 ohm termination resistors are used throughout the FPS-264).

With this level of change in ground pin currents, lead inductance is very important for good performance. After consulting with Fairchild, FPS tested devices in both flat packages and DIPs and decided to use the DIP due to its impressive per-formance. The waveforms generated under the worst case switching current condition are shown in **Figure 3**.

In the system, the resulting modified FGE0020 exhibited a considerable improvement in speed over standard 100K parts. The bus driver propagation delay from the enable input is specified at 1.8 nsec, worst case. The equivalent 100K function would use a 100123, which has a 5.3 nsec maximum delay. This speed increase more than offsets the amount the transmission line delay was over budget. In fact, the use of this part probably saves close to 5 nsec in the maximum delay for DPBS transfers.

Circle 234

NEW PRODUCTS

16×16 Bit Multiplier Chip

The NCR45CM16 16 × 16 bit single-port multiplier chip performs successive multiply-accumulate operations at a 5 MHz rate. The chip can be directly interfaced to a 16-bit bus without additional logic, and can also be plugged into many existing microcomputer boards without extensive re-engineering or redesign of the system. Consuming 10mA (maximum), the NCR45CM16 is available in a 0.6″ wide 24-pin plastic DIP and in a 0.3″ wide 24-pin ceramic DIP. Price is $60 (plastic package) and $75 (ceramic package). **NCR**, Dublin, OH

Circle 130
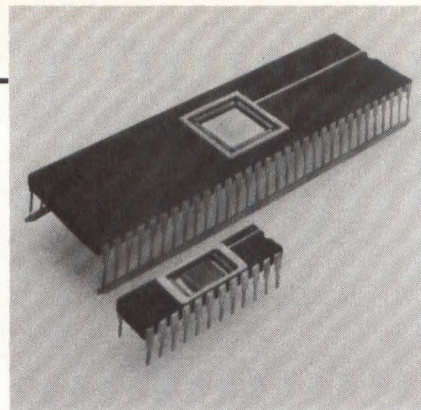
Upgrade For Older PDP-11 Computers

The Microverter 73 LSI 11/73 Unibus upgrade for earlier DEC PDP-11 computers replaces the PDP-11 Unibus processor and memory with an 11/73 processor and Q-bus memory. It consists of a quad-width Microverter board, a dual width power regulator/console interface board, a 1 Mbyte memory board, an LSI-11/73 processor board and a 9-slot backplane with four hex-width Q-bus slots and five Unibus slots. The board performs Q-bus to Unibus signal conversion and handles the 22-bit memory mapping for 18-bit Unibus devices. With its Unibus mapping registers, the Microverter 73 is recognized as a PDP-11/44 by the system software. The Microverter 73 system resides in an older PDP-11 computer chassis in the space left vacant by the old processor boards, memory and backplane. It is applicable for PDP-11/34, 11/34A, 11/04, 11/05 and 11/60. Price is $9,950. **Able Computer**, Costa Mesa, CA
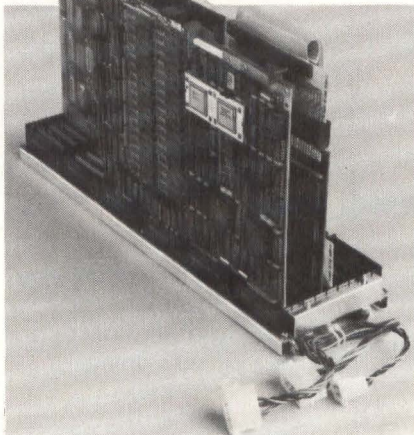
Circle 222

Personal Logician CAE System

The Personal Logician AT CAE System includes design entry capabilities and the Personal Daisy Logic Simulator (PDLS) for design verification. The system offers integrated design entry and simulation on an IBM PC-based system. The Personal Logician AT system can be networked with any other high-end Daisy workstation to share data via Ethernet. The system also includes 640 Kbytes of RAM, a 20 Mbyte hard disk drive and a 1.2-Mbyte floppy drive. The two Daisy system families are fully compatible, use the same databases, user interface and can be connected on Daisy's network. The Personal Daisy Logic Simulator (PDLS) will soon be available for the Personal Logician AT. Price is $25,000. **Daisy Systems**, Mountain View, CA

Circle 148
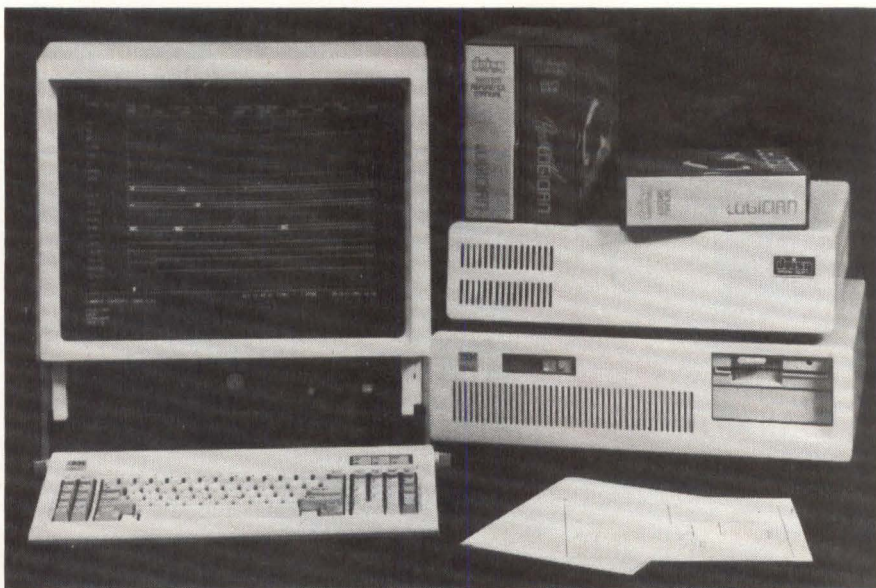
COMPUTERS/SYSTEMS

MULTIUSER 80286-BASED BUSINESS SYSTEM
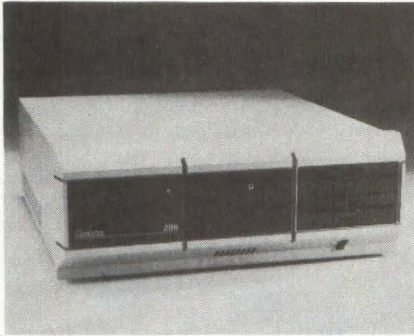
The CompuPro 286 16-bit multiuser business computer system is based on an 80286 microprocessor featuring 8-bit slave processing capabilities. It combines the 80286 CPU for 16-bit operation with CompuPro's Z80-based slave processor unit to simultaneously perform all 8-bit slave processing tasks. The CompuPro 286 accomodates four users and can be expanded to as many as 14 users. The system comes standard with 512 Kbytes of main memory, an 800 Kbyte 5.25″ floppy disk drive, a 40 Mbyte 5.25″ hard disk, one parallel and one Centronics printer port and four serial ports. Price is $9,995. **CompuPro,** Hayward, CA   **Circle 164**

EXPANDED COMMUNICA-TIONS GATEWAY

Offering bi-directional text file transfer capabilities with a variety of remote host mainframes, the Domain Networking RJE Access Gateway allows users on an Apollo Domain network to access remote environments using a KMW protocol converter. The RJE Access Gateway software emulates IBM's Hasp and the standard 2780 and 3780 environments; the software and protocol converter can be implemented on one workstation within the network. Price is $1,800. **Apollo,** Chelmsford, MA   **Circle 225**

DATA SWITCH SYSTEM

Supporting 180 terminal-to-computer port connections, or 360 lines, the DS01 CommXchange data switch is compatible with any async terminal. Expansion units can be added for an additional 480 connectors, or 960 lines. With speeds of up to 9600 bps on all lines, bandwidth rate is 6.336 mpbs. **Emulex,** Costa Mesa, CA   **Circle 229**

32-BIT MULTIUSER SYSTEM

Permitting up to 32 users, this 32-bit multiuser system (Model 550) features floating-point CPU, up to 10 Mbytes of memory and an enhanced HP-UX operating system. A second and third CPU can increase the throughput up to 2.7 times the rate of one CPU. Four software packages are available. Price is $19,425-$36,325. **Hewlett-Packard,** Palo Alto, CA   **Circle 240**

DESIGN AUTOMATION SYSTEM

The CDA 5000 design automation system is built on complexity management techniques developed by artificial intelligence research. The system supports hierarchical logical design, including the ability to design top down or bottom up, through multiple levels. The CDA's integrated database allows rule checking to be done as the design is created. **Cericor,** Salt Lake City, UT   **Circle 226**

LOTUS ON AN MV/1000

A hardware and software combination, the Bridge System provides microcomputer functionality as a central system resource. A terminal connected to the host mini can act as a dedicated micro and run applications like Wordstar, dBase II and Lotus 1-2-3. Host-system processing, utilities and peripherals are available to Bridge users. **Virtual Microsystems,** Berkeley, CA   **Circle 227**

EMULATOR

Available as a subsystem to the HP 64000 logic development system ， the 64194S emulator supports design and development of products based on the 146805G2 microcomputer. Featuring real-time transparent emulation of microprocessor-based systems, these HP 64000 emulators run controls, feature single-stepping, display-and-modify registers, display-and-modify emulation memory, command-file operation and more. Price for the 64194S 146805G2
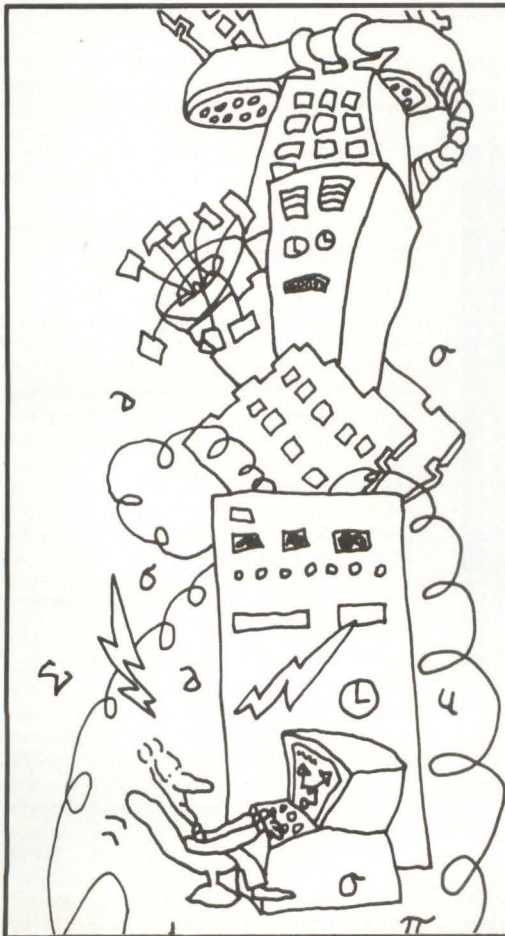
NEW PRODUCTS

is $3,800. **Hewlett-Packard**, Palo Alto, CA

Circle 228

Q BUS BASIC BOX SYSTEMS

The Basic Box System includes the MDB 800 series chassis, a DEC 11/12 Plus CPU and MDB memory modules in sizes of 256 or 512 Kbytes on dual size boards or a 1 Mbyte RAM module on a quad size board. A 5¼″ high chassis can contain 11/23 Plus CPU, 1.5 Mbytes of main memory and 32 DZII compatible multiplexer ports, an SMD disk controller and a line printer controller, all using connectors mounted on the rear distribution panel. Price is $4,545-$5,920. **MDB**, Orange, CA   **Circle 168**

GRAPHICS TERMINALS

The Freedom 240 Graphics/ANSI Video Display Terminal and the Freedom 210 Graphics/ASCII Video Display Terminal feature 14″ 132-column alphanumeric displays. The Freedom 240 is DEC VT220/VT100 and Tektronix 4010 and 4014 compatible. The Freedom 210 is compatible with the Freedom 200 and emulates the TeleVideo 950, ADM 31 and Tektronix' 4010 and 4014. Both terminals feature 665 × 288 pixel resolution, 4096 × 4096 addressability, and drawing speeds faster than the VT240 graphics terminal. An amber screen is optional. Price is $1,295 (210) and $1,395 (240). **Liberty**, San Francisco, CA   **Circle 163**

MULTIUSER/MULTITASKING COMPUTER

The Datavue 4000 system, designed for OEMs, includes 80186 and Z80 processors, 512 Kbytes of RAM expandable to 1 Mbyte, up to 80 Mbytes of online storage, four serial RS-232C ports and one Centronics port, and Concurrent DOS. Six simultaneous users are supported, depending upon available memory and systems requirements. Optional boards on the DV4000 provide eight additional RS-232C ports. The Z80 8-bit processor included with the 16-bit 80186 allows an OEM to convert 8-bit application code to 16-bit code in stages. Price is $4,995. **Datavue**, Norcross, GA   **Circle 158**

PCB CAD SYSTEM

The 100AR is a 16-bit stand-alone workstation, the third generation of the Model 100. It is equipped with schematics, autorouting, design rule checking software, and a rastnesting technique to aid component placement. The system can design boards of up to 20″ × 20″ with 200 16-pin equivalent ICs with 64 colors and layers. Screen resolution is 512 × 512. Hardware consists of a system console, keyboard, VT-100 type terminal, 14″ color monitor, line printer, proprietary graphics board and digitizer tablet. The CPU is the DEC LSI-11/23+ with four serial ports. Options include a 20 Mbytes Winchester, modem,

digitizer, pen plotter, UPS and more. Price is $4,500. **Paragon Technology**, Pleasant Hill, CA

Circle 216

Z-SCAN 80 EMULATOR

The Z-Scan 80 emulator runs at speeds up to 80 MHz. It can operate as a standalone or on a host system such as the VAX, or Zilog's 8000 supermicros. Operation, which can be set on the Z-Scan at 4, 6, or 8 MHz, is transparent. The Z-Scan 80 provides a real-time emulation from mappable memory, allowing designers to develop programs without a target system, through 32 1 Kbyte blocks or mappable memory. The emulator includes a 4K by 32-bit block of RAM. 4,096 trace cycles can be handled by the Z-Scan 80's trace facility. Based on the Z8001R CPU, the Z-Scan 80 interfaces 2 RS-232 serial ports to the host computer and CRT terminal. Price is $6,695. **Zilog**, Campbell, CA   **Circle 160**

CMOS SINGLE-CHIP MICROCOMPUTER

The new 8-bit single-chip CMOS microcomputer permits users of the Oki Semiconductor 80C48 and 80C49 to double or quadruple on-board RAM or ROM capacity without changing the instruction set. The 80C50 is upward op-code compatible with HMOS devices supplied by Intel, NEC and others. It can execute the same instruction set that is used with the HMOS 8050 device, but the 80C50 offers an additional 13 instructions. The 80C50 is a static device that has an operating frequency range from 0 to 6 MHz and a Vcc range of 2.5 V to 6.0 V. When operating at 6 MHz, the 80C50's Vcc range extends from 3.5 V to 6.0 V. Price, in quantities of 100, is $11.50. **Oki Semiconductor**, Sunnyvale, CA

Circle 212

MULTIUSER SUPERMICRO
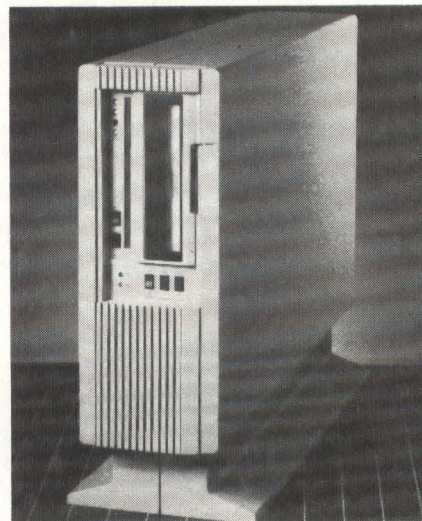
The Spirit 73 supermicrocomputer addresses up to 4 Mbytes of parity MOS memory. It uses the DEC PDP-11/73 processor and runs on DEC RSTS/E, RT-11/TSX-Plus, RSX-11M or RSX-11M-Plus operating systems. Spirit 73 features 40 Mbytes of online disk storage including a 20 Mbyte removable disk cartridge. The processor includes a MMU with 22-bit addressing capability (4 Mbytes). Spirit 73 is available in a clamshell, pedestal-style that opens along the full length of the unit, and a standard rack mount unit. Price is $17,000 – $25,000. **First Computer Corp.**, Westmont, IL   **Circle 159**

LOGIC ANALYZER

The K205 logic analyzer offers 48 channels at 100 MHz. It features 16 independent triggering decision levels with four commands in each level. Four decisions can be made every 20 nsec. The K205's tolerance compare feature can analyze logic circuits by comparing timing sequences against stored references. The auto save feature displays transient noise on all channels and a latching scheme maintains full channel width and memory depth when using glitch mode. Three separate measurement input sections monitor independent circuit clocks for multiprocessor systems. Price is $14,000. **Gould**, Santa Clara, CA   **Circle 217**

HIGH-END COMPUTER

The VAX 8600 is approximately the same physical size as the VAX 11/780 and has almost the same power requirements. It uses customized ECL gate array semiconductor technology, a dedicated memory bus, write-back cache and a pipelined operation. The VAX 8600 can provide 32 Mbytes of main memory, 160 billion bytes of online storage, up to 512 communication lines directly and more with the addition of Ethernet LAN support under DECnet, 4 billion bytes of program address capacity and support for the Unibus, DR780 and Massbus general purpose I/O interfaces. Cycle time on the VAX 8600 has been reduced to 80 nsec compared to the 200 nsec cycle time on the VAX 11/780. Price is $576,000 – $970,000. **DEC**, Maynard, MA

Circle 165

3D GRAPHICS SYSTEM

The Model One/380 is a 3D graphics system designed to provide local manipulation and realistic shaded display of 3D objects. The system features local 3D 32-bit floating point transformations with perspective, up to 4 Mbytes local display list, local light source modeling with variable surface properites, local hidden surface removal and full color smooth shading, flicker-free 1280 × 1024 resolution at 60 Hz, up to 24 bits of image memory for true color, and full size 16-bit depth buffer. Price is $41,500. **Raster Technologies**, North Billerica, MA

Circle 166

WORKSTATION

The Sun-2/50 workstation operates without a local disk. Several diskless machines can share the disks of a Sun-1/120FS or Sun-2/170 fileserver. Demand paging is handled by a network over the Ethernet to mass storage on the fileserver. The Sun-2/50 CPU is MC68010-based operating at 10 MHz with no wait states. The memory management design allows for 1 to 40 Mbytes of physical memory and up to 16 Mbytes of virtual address space per process. The 19″ high-resolution (1152 × 900), 66 Hz non-interlaced display, provides a flicker-free image. Price is $9,900. **Sun Microsystems**, Mountain View, CA

Circle 161

MS-DOS COMPUTER
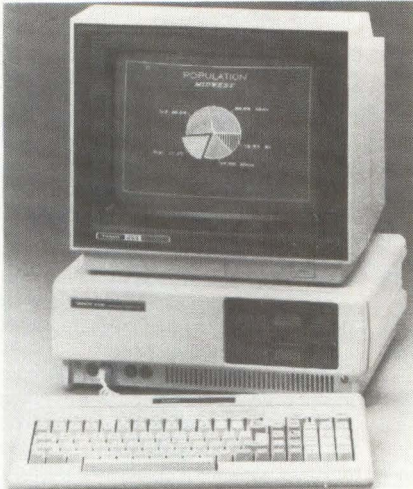
The Tandy 1000's design and 360K floppy disk format allow it to run off the shelf IBM PC software including Lotus' 1-2-3, Ashton -Tate's dBase III and Multimate International's Multimate, as well as Tandy's Deskmate program. The Tandy 1000 accepts up to three IBM PC plug-in option cards and memory is expandable to 640K. Monochrome and color graphics to 640×200 dot resolution are built in, as are parallel printer, joystick and light pen ports. The Tandy 1000 also features composite audio/video and RGB outputs. Display modes are user selectable at 40 or 80 characters $\times$ 25 lines. The computer uses an 8088 16-bit microprocessor operating at 4.77 MHz and comes with a floppy disk drive. Price is $1,199. **Tandy**, Fort Worth, TX
Circle 162

VAXSTATION I WORKSTATION SYSTEM

The VAXstation I 32-bit single user workstation system incorporates the MicroVAX I and provides VAX/VMS resources in a desk unit, including high resolution graphics and multi-windowing capabilities. The VAXstation I supports GKS (Graphics Kernal System) and can be connected to DECnet/Ethernet computer networks. The system features a 60 Hz noninterlaced 19" screen display with a 960×864 resolution. The VAXstation I also consists of a 1 Mbyte processor, $1K \times 2K$ bitmapped video RAM, RX50 dual 400 Kbyte 5¼" diskette drive, RD52 31 Mbyte 5¼" mini-Winchester-technology disk and mouse. Price is $21,095. **Digital Equipment Corp.**, Maynard, MA **Circle 215**

125 MHZ STATE AND TIMING ANALYZER

The HP 64610S timing/state analyzer features realtime, transparent state analysis to 125 MHz, timing analysis to 400 MHz in fast-sample mode, 200 MHz for wide-sample, dual threshold and glitch modes, 8, 16, 24 or 32 input channels for sync or async analysis, three modes, each with 4K memory, and fast sample mode with 8K memory, pattern and transitions triggering, compare mode for matching against sample measurement, and postprocessing of measurements for sequence triggering up to four levels deep, calculating statistics, and marking defined events. The HP 64610S analyzer is installed in HP 64000 system development stations. Price is $7-$20,000. **Hewlett Packard**, Palo Alto, CA
Circle 213

68000-BASED MICROCOMPUTERS

The 440 and 460 are additions to the Stride 400 Series of microcomputers. Both systems feature a 10 MHz 68000 processor, 256 Kbytes RAM, 640 Kbyte 5¼" floppy disk storage, 10 (440) and 15 Mbyte (460) Winchester hard disk storage, VME bus, 10 RS-232-C ports, battery-backed real-time clock, Omninet LAN hardware, Liaison network software, p-system Version IV.2 operating system and a Centronics-parallel port. The 460 also features a VME expansion card cage. Some options for both micros include a 12 MHz 68000 processor, RAM expansion to 2 Mbytes (440) and 3 Mbytes (460), memory management unit and more. Price is $5,900 (440) and $8,900 (460). **Stride Micro**, Reno, NV
Circle 214

MULTIUSER BUSINESS SYSTEM

The Tower XP is an addition to NCR's UNIX-based family of multiuser business systems. The new system includes the same interface modules as the Tower 1632, including 5¼" (ST506) and 8" SMD) disk drive interfaces. Multibus, ¼" cartridge tape drive (QIC II) I/Fs and communication I/Fs for low-order and high-order communications. It also features networking capabilities, including SNA, X.25 and LANs, power failure recovery with battery backup, a MMU with error check and error correction, a separate memory bus and extensive diagnostics, including concurrent and online remote support. Price is $19,495. **NCR**, Dayton, OH
Circle 167

COLOR PCB CAD SYSTEM

The Artworker III is a stand-alone, benchtop, turnkey CAD system that offers capabilities for both schematic design and PCB layout of analog and digital boards. The Artworker III separates design and layout functions into two software packages. The 14" high resolution monitor displays the schematic or PCB layout in full size and 8 colors and the 9" monochrome monitor shows size, mode, X-Y coordinates, etc. The Artworker III comes with a full-sized ASCII keyboard, separate numeric keypad, separate function keys and a joystick. Data is stored and retrieved by a dual floppy disk system with a combined capacity of 2 Mbytes. Price is $22,000. **Wayne Kerr**, Woburn, MA **Circle 218**

NEW PRODUCTS

PERIPHERALS

2400 BPS DIAL MODEM

The F1935D two-wire full duplex modem operates at 2400 and 1200 bps. The unit is compatible with CCITT V.22 bis at 2400 bps. The fallback speed of 1200 bps is in full compliance with either Bell 212A or CCITT V.22. The F1935D has built-in automatic calling and answering functions, and pulse or tone dialing is selectable. Diagnostics include local analog and digital loopback, and remote digital loopback tests. The modem works with both sync and async terminals. Price is $995. **Fujitsu America**, San Jose, CA **Circle 178**

RIBBONLESS COLOR INK-DOT PRINTER MECHANISM

The Model 3740 40-column, dot matrix color ink-dot, ribbonless, impact printer mechanism prints and drafts in seven colors. It produces text and graphics at up to 480 dps dual density. The printhead design, by which the motion of the print wire clears ink from the wire path, reduces clogging and drying problems. The mechanism's standard character font is 9 × 13 measuring 1.82mm × 2.62mm. Effective print size is 96mm × 192mm. Printing speed is 70mm/sec on an XY axis, 100mm/sec on a 45° angle. Price is $50. **Epson**, North Hollywood, CA **Circle 171**

DUAL-MODE PLOTTER

The 1044 dual-mode plotter features eight pens and full-width plotting capability up to ANSI size E or ISO size AO. It operates in cut-sheet and continous-roll modes. The 1044 accommodates mechanical design, architectural, engineering and construction applications, integrated circuit design, printed circuit board design and mapping. Features include an eight-pen turret with automatic pen-capping, an integrated communications interface, non-volatile setup memory, automatic logon messages, self diagnostics and a joystick. The plotter provides a resolution of 0.001″. Price is $11,995. **Calcomp**, Anaheim, CA **Circle 208**

MOBILE DATA TERMINAL

The KDT 480 mobile, wireless data terminal can be used as a dedicated radio system, or be incorporated into an existing radio system. Storage of up to 3,000 characters in the RAM are dynamically allocated. Featuring a text area of over 20 sq. in., the CRT can display up to 480 characters, formatted into 12 lines of 40 characters each. Two additional lines provide 80 characters of operational status information. The terminal display is designed for varying light conditions of the vehicular environment. **Motorola**, Schaumburg, IL **Circle 179**

VAX-BASED LAN

The Inplant LAN is designed to connect VAX and other computers to a variety of peripherals, devices and factory automation equipment. Inplant uses Ethernet , broadbend cabling or fiber optic lines for physical transmission. It allows users to connect over 1,000 terminals or devices, including smart equipment, to VAXs running the VMS operating system, via the LAN. VAX communications I/O processing is offloaded to network microprocessors. Connections to each VAX are made through a single cable interface. Inplant has virtual circuit capability, which allows connection to different computers, intelligent equipment, RS-232 devices and printers. Price is $750. **Fairchild**, Los Altos, CA **Circle 177**

14-PEN PLOTTER
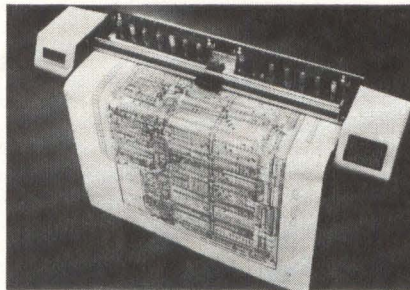
The DMP-51/52 MP 14-pen plotter features a resolution of .001″, a maximum plotting speed of 22 ips and a user-selectable acceleration rate of up to 4 Gs. The DMP-51/52 has two stables that hold seven pens each. The C and D size plotter also includes constant velocity control for uniform inking regardless of the angle of pen movement and an automatic self-capping feature to prevent pens from drying out. The servo-driven plotter contains built-in DM/PL intelligence and can be interfaced with any computer featuring an RS-232C port. **Houston Instrument**, Austin, TX **Circle 172**

DEC-COMPATIBLE COLOR TERMINAL

The ColorTrend 210 terminal offers a low profile, detached keyboard and a one-touch tilt display. Its ColorKey feature lets the user add color to existing black and white software without reprogramming. The terminal is compatible with DEC's VT100 and any ANSI X3.64 environment. It provides eight foreground and eight background colors and character graphics. A foldover capability permits viewing of 132 column reports. Twenty-four keys are programmable for 72 different functions. Price is $1,295. **Intecolor**, Norcross, GA **Circle 173**

ENHANCED FAME II SMART TERMINAL

The Fame II distribution terminal is now available with a DEC VT 102 emulation option, enabling users to use double wide and double high wide characters. Features include a standard 14″ screen, an IBM selectric-style keyboard correction key, ergonomic housing and 50 non-volatile user PF keys. The smart terminal offers DEC VT-100 and VT-52 modes and also features non-embedded video attributes, block mode, the capability to handle 24 lines by 80 and 132 columns and a 25th status line. It also provides full page soft setup screen, smooth scrolling, split screen and local editing. **Falco**, Sunnyvale, CA **Circle 211**

3 1/2″ MICROFLOPPY DISK DRIVES
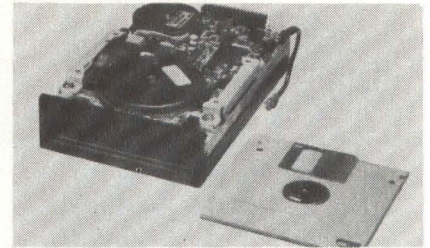
The JU-312, JU-322 and JU-362 3 1/2″ microfloppy disk drives offer storage capacity of 250 Kbytes, 500 Kbytes and 1 Mbytes (unformatted) and are 104mm wide and 161mm deep. They are compatible with 5 1/4″ floppy disk drive interfaces. Features include same or double the storage capacity of conventional 5 1/4″ drives, single button disk ejection/insertion, 3ms track to track access time (500 Kbyte and 1 Mbyte models), low power consumption (3.5 W in the read mode) and a direct drive brushless motor and a steel band. All units are compatible with 3 1/2″ disk media. Price ranges from $125 - $200. **Panasonic**, Secaucus, NJ **Circle 180**

FIBER OPTIC INTER-PROCESSOR LINK

The CBE-202 fiber optic interprocessor link comprises a parallel to serial multiplexer and a bus interface module (BIM) which plugs into the DEC backplane SPC slot. A duplex fiber optic cable links the two multiplexers. The link operates at 250K words/sec and can be as long as 2K meters. The BIMs are software compatible with any operating system that is compatible with the DEC DR11-B or DR11-W modules. The link can be configured for Unibus to Unibus, Qbus to Qbus or Unibus to Qbus DMA transfers. Price is $4,500. **Canoga Data Systems**, Canoga Park, CA **Circle 176**

PROTOCOL CONVERTER

The VTS 361 Protocol converter can support one or two host lines, either direct connection or dial-up and can handle up to eight async devices. Devices and front-end processor links are supported at speeds up to 19.2 Kbps. Features include menu-driven setup, password security, internal diagnostics, automatic speed detection, non-volatile EEPROM setup memory, and automatic log-on and inactivity disconnect. **Infotron Systems**, San Diego, CA **Circle 210**

3½" AND 1.6 MBYTE FLOPPY DISK DRIVES
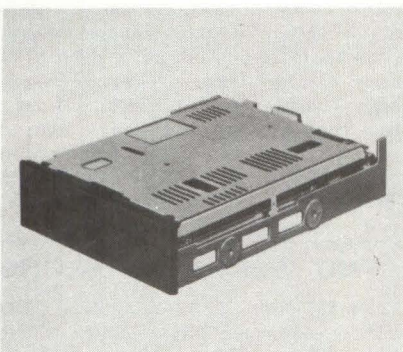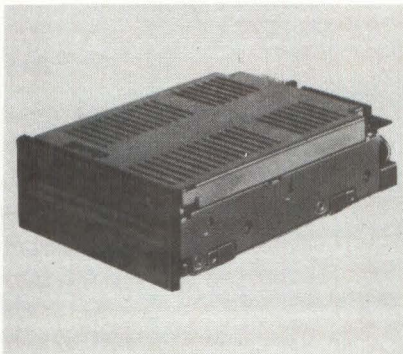
The FDA-3000 Series 3½" and FDA-5400 Series 1.6 Mbyte half-high floppy drives offer single or double density formats and full or half-high face plates. Other features include a direct drive D.C. Servo Spindle Motor, and Alpha-Winding steel belt head positioning mechanism, proprietary LSI Controller chips, LED photosensing and EMI/RFI shielding. Price is $130-$200. **Sumitomo**, Sunnyvale, CA
Circle 209

NINE NEW PRINTERS

Nine models introduced by Dataproducts include three daisy wheel printers, four dot matrix printers, a check printer and the laser non-impact printer. The three daisy wheel models are the DP-20, DP-55Q and DP-55SQ. The DP-20 prints at 20 cps, and the DP-55Q and DP-55SQ print 55 cps. The four dot matrix impact printers are the 8011, 8021, 8051 and 8071. The 8011 and 8021 are monochrome printers. Both the 8051 and 8071 offer color graphics capability. All are IBM compatible. The NP24 employs solid state laser imaging technology and prints 24 pages/minute and 300 dpi. The CP40 check printer prints 55 cps at 12 cpi. **Dataproducts**, Woodland Hills, CA
Circle 174

LETTER QUALITY INK-JET PRINTER

The PT-90 ink-jet printer has a full letter quality print mode at four pages/minute (200 cps), eight page/minute (400 cps) printing speed in a draft mode, the ability to print on standard copy paper, graphics compatibility and versatile paper handling. It prints 240 dpi horizontally and vertically and character resolution is 96 × 32 dots in a letter quality mode at 200 cps, and 48 × 16 dots draft at 400 cps. The PT-90 accepts plug-in interface cards for serial,

parallel or IEEE-488 ports. Various protocols including IBM compatibility and Diablo 630 emulation are available. Price is $3,495. **Siemens**, Iselin, NJ
Circle 175

MICROPRINTERS

The Model 860 XL microprinter is designed for data processing, graphics and office correspondence printing. It combines a 16" carriage, letter quality and data processing printing, graphics and customer removable font modules. Adjustable snap-in tractors are standard on the 865 and friction drive capability provides vertical alignment for continuous forms. The 860 XL prints data processing and rough draft copy at 150 cps in a 9 × 9 matrix. Switching between draft and correspondence print modes is via a button on the control panel. The 865 prints letter quality at 35 cps in a 32 × 18 matrix, and draft at 150 cps in a 9 × 9 matrix. Both printers print Mosaic and Raster graphics and have standard parallel and serial interfacing. **Texas Instruments**, Dallas, TX
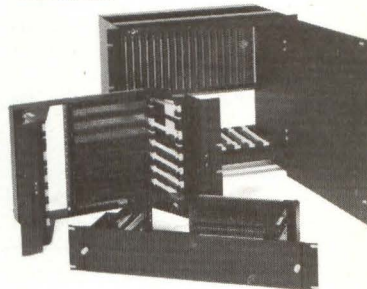**Circle 170**

NEW PRODUCTS

WINCHESTER DISK DATA SEPARATOR

The WD10C20 is a self-adjusting Winchester disk data separator and write precompensation device. It is designed for use with ST506 and the WD1010/2010 hard disk single-chip controllers. Available in a 28-pin DIP or QSM surface mount package, the chip can read or write MEM data at a 5 MHz rate. The WD10C20 incorporates proprietary CMOS technology to minimize power consumption on the hard disk controller. There are three major functional sections within the WD10C20: a crystal controlled reference oscillator, data timing and precompensation circuits for write operations, and a phase-locked VCO for data detection and synchronization in the read mode. Price in quantities of 100 is $30. **Western Digital**, Irvine, CA **Circle 126**

32-BIT BIPOLAR PROCESSOR FAMILY

The first available members of the Am29300 32-bit bipolar processor family include the Am29323 32-bit parallel multiplier, Am29325 32-bit floating point processor, Am29331 microprogram sequencer, Am29332 32-bit arithmetic logic unit, and the Am29334 four-port, dual access register file. The Am29300 family devices are functionally partitioned building blocks. They feature sub-100 nsec cycle time, a symmetric instruction set, a 3-bus flow through architecture and complete interlocking fault detection. **AMD**, Sunnyvale, CA **Circle 133**

Z80 MICROCOMPUTER CPU

The MK3880-6 CPU allows 50% greater throughput than the 4 MHz MK3880-4. The MK-3880-6 features arithmetic and bus control, a single phase system clock, +5V supply and on-chip dynamic memory refresh counter. It also features a vectored interrupt handling system for da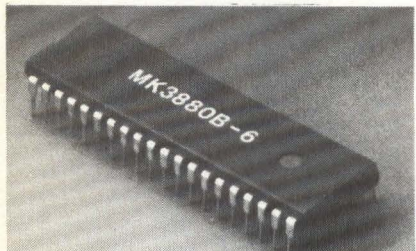isy-chain arrangement of a priority interrupt scheme. N-channel silicon-gate depletion load technology is used in manufacturing the MK3880-6 CPU. The MK3880-6 microcomputer is software compatible with the 8080A CPU. Price, in quantities of 100, is $5.50. **Mostek**, Carrolton, TX **Circle 154**

256K EPROMs

The HN27256G-25 and HN27256G-30 are 250 nsec and 300 nsec ultra-violet EPROMs that are organized in 32K × 8-bit words. These NMOS EPROMs require 45mA in typical applications. The 2-micron geometry reduces the die size of the EPROMs by 40%. The HN27256G-25 and HN27256G-30 are packaged in 28-pin, JEDEC-compatible ceramic DIPs. Price is $63 (HN27256G-25) and $57 (HN-27256G-30). **Hitachi**, San Jose, CA **Circle 136**

SIGNAL CONDITIONING MODULES

Six signal conditioning modules offer system users a plug-in alternative to strain gage, dynamic voltage and power monitoring applications. The 3B18 module provides wide-band width signal conditioning of strain gage sensors; the 3B40 and 3B41 offer a 10 KHz isolated input capability to monitor power-line voltages or currents. Designed to plug into Analog Devices' 3B Series Signal Conditioning Subsystem, the modules expand the signal conditioning options for computer-based industrial measurement and control. Price is $175-$200. This release was run in the October issue of *Digital Design* with the improper photo. **Analog Devices**, **Circle 146**

POWER MOSFET DRIVERS

The TSC426, TSC427 and TSC428 dual drivers translate a TTL/CMOS low level input signal to an output voltage swing equalling the supply. The 4.5V to 18V supply voltage minimizes MOSFET conduction power dissipation. The driver outputs swing within 25 millivolts of ground and the positive supply. The TSC426/427/428 swing a 1000pf load 18V in 30 nsec. Driver output impedance is 6Ω with a 1.5 amp peak output current. Input current is a 1μA. The CMOS drivers require 1/5 the quiescent supply current of the pin compatible bipolar DS0026 driver, 8mA vs 40mA. Typical quiescent supply current with a 100 KHz switching rate is 5mA (C_L 1000pf). Price is $1.45 to $9. **Teledyne Semiconductor**, Mountain View, CA **Circle 127**

BIDIRECTIONAL 8-BIT INTERFACE

The 54/74ACT646 interface device is pin and electrically compatible with existing LS-TTL bipolar interface circuits, and electrically compatible with existing HCT-CMOS circuits. The 74ACT646 combines two registers and two multiplexers for bidirectional data flow. Data can be stored or transmitted via the register. The multiplexers, acting as switches, transfer real-time stored data from one side to the other. The 74ACT646 has an output drive current (IOL) of 12mA, and operates up to 25 MHz in the commercial range. Maximum clock-to-output is 30 nsec and maximum data-to-output delay is 35 nsec. Price is $8.58 – $9.92. **Monolithic Memories**, **Circle 128**

GaAs SEMICUSTOM IC
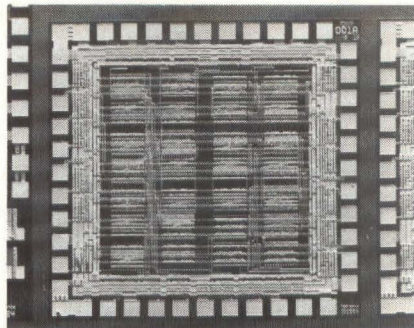
The GaAs Quick Chip cell array can be used to build both high speed digital and microwave analog circuits. It supports digital circuits with clock rates up to 2 GHz and analog circuits with bandwidths to 5 GHz. The Quick Chip provides a level of performance for systems operation at clock rates above 500 MHz. It can integrate subsystems that currently require the use of a whole board of SSI ECL parts, and provides a three to five times speed advantage over current ECL circuits. Price begins at $55,000. **Tektronix**, Beaverton, OR **Circle 134**

16-BIT MICROPROCESSORS

The MSM80C88 and the MSM80C86 CMOS microprocessors are fully compatible with the HMOS 8086 and 8088 in terms of package, electrical characteristics and software. The 8-bit MSM80C88 and 16-bit MSM80C86 can execute current software on existing 8088 and 8086 system designs. All four of these microprocessors share the same set of instructions. Both microprocessors have a 20-bit address bus allowing access of up to 1 Mbyte of RAM. The MSM80C86 and -88 operate at 5 MHz, guaranteed over the full temperature range, with typically 15% of the system power dissipation of the equivalent HMOS system. Price in quantities of 100 is $36.75. **Oki Semiconductor**, Sunnyvale, CA **Circle 138**

SINGLE CHIP MICROCOMPUTER
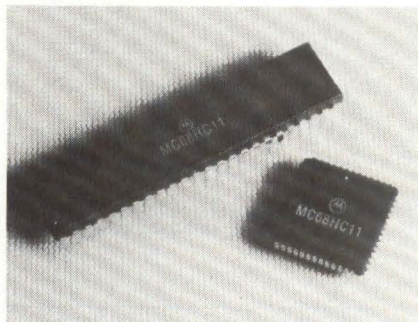
The MC68HC11A8FN single chip MCU is upward object-coded compatible with the M6801 family and provides new 16-bit instructions to the instruction set. Features include 3V to 5.5V operation, 8 Kbytes of ROM, 512 bytes of EEPROM, 256 bytes of static RAM, a real-time interrupt circuit, an 8-channel 8-bit A/D converter and an 8-bit pulse accumulator circuit. The MC68HC11A8 also has an enhanced 16-bit timer system with three input capture and five output compare functions. Price is $20. **Motorola**, Austin, TX **Circle 144**

MONOLITHIC V/F CONVERTER
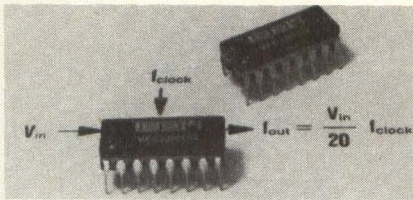
The VFC100 monolithic voltage to frequency converter requires no critical external components. The charge balance technique is used, but the critical reset integration period is derived from an external clock frequency. The VFC100 eliminates the critical external one-shot capacitor which limits accuracy and drift from previous V/F devices. A precision laser trimmed input resistor sets a 10V full scale input voltage. The resulting function of the VFC100 is internally controlled to 0.5% gain and 50 ppm/°C max drift. Nonlinearity is less than 0.2% at 100 KHz. An accurate 5V reference is also provided. Price in quantities of 100 starts at $8.85. **Burr-Brown**, Tucson, AZ   **Circle 131**

ERASABLE PROGRAM-MABLE LOGIC DEVICE

The EP1200 erasable reprogrammable logic device has 28 on-board registers, 236 product terms, on-board latches for the inputs, programmable I/O and product term sharing. The EP1200 incorporates programmable architecture under EPROM control, has buried registers, variable product term distribution, global and local busing and two independent programmable clocks. The EP1200's erasable feature allows generic testing prior to shipment. The EP1200 can operate at clock speeds above 16 MHz, while dissipating 400 mW in the active mode. Standby power dissipation is 15 mW. Price is $129.50. **Altera**, Santa Clara, CA   **Circle 132**

256K DRAMs

The HM50464P and HM50465P DRAMs are organized in 64K 4-bit words for parallel transmission of data. The HM50464P transfers data in page mode and the HM50465P uses nibble mode for faster reading and writing. Both DRAMs are available in 120-, 150- and 200-nsec access times. In nibble mode, the HM50465P can read or write 16 bits, 4 parallel bits in 4 sequential locations, in a total of 400 nsec on the fastest version. The HM50464P and HM50465P are housed in 18-pin, plastic DIPs. Both consume 350 mW while active and 23 mW while on standby. Price, in quantities of 1-24, is $75. **Hitachi**, San Jose, CA   **Circle 196**

12-BIT CMOS A/D CONVERTER

The AD7582 is a four-channel, successive approximation 12-bit A/D converter which guarantees maximum total unadjusted error of ± LSB over its operating temperature ranges and a maximum conversion time of 100 μs. The AD7582 is microprocessor compatible with byte-selectable interface to an 8-bit bus. The converter operates from +5 V and +15 V power supplies and consumes maximum power of 150 mW. Maximum differential nonlinearity for all grades is ± 3/4 LSB, maximum full scale is ± 1/4 LSB and maximum offset error is ± 1/4 LSB. The AD7582 is packaged in a 28-pin DIP. Price, in quantities of 100, is $32.50 to $92.37. **Analog Devices**, Norwood, MA   **Circle 194**

MULTIPLYING D/A CONVERTER

The AD562A 12-bit multiplying D/A converter has a maximum settling time of 400 nsec to ½ LSB (200 nsec typical). It features fully monotonic over temperature range, binary coded inputs, selectable digital thresholds (CMOS/TTL), internal span resistors, output voltage ranges and 210 mW power consumption. The AD562AKD has an accuracy of ± 1/2 LSB (± 0.01%) and a temperature range of 0°C to +70°C. The AD562ASD has an accuracy of ± 1/4 LSB (± 0.005%) and a temperature range of -55°C to +125°C. Price, in quantities of 100-999, is $11.95(AKD) and $55 (ASD). **Motorola**, Phoenix, AZ   **Circle 193**

DIRECT MEMORY ACCESS CONTROLLER

The 82258 ADMA controller is designed for microcomputer systems using the iAPX 286 microprocessor, and systems based on the iAPX 86/186 microprocessor family. The controller has an 8 Mbyte/sec data transfer rate when used with the iAPX 286's pipelined architecture. The 82258 supports up to 35 different data channels. Its four-channel design allows high speed data transfers on all channels. The on-chip bus interface can be programmed to support the iAPX 286 bus and the multiplexed iAPX 86 family bus, with a maximum memory addressability of 16 Mbytes for iAPX 286 systems. Price, in quantities of 100, is $170. **Intel**, Santa Clara, CA   **Circle 197**

2-MICRON CMOS STANDARD CELL CIRCUITS

The ISC20000 standard cell arrays use macro functions compatible with the IGC20000 series gate arrays. The series uses a silicon gate CMOS process with 2-micron channel lengths and two-level metal interconnect. It features 1.7 nsec typical delay for 2-input NAND, a 2.0V to 5.5V power supply range and full -55°C to 125°C range. Up to 16K static RAM and up to 128K ROM is also included. The ISC20000 also provides more than 100 Flexicell functions for conversion of 7400- and 4000-based designs. **General Electric**, Albany, NY **Circle 143**

16-BIT DACS
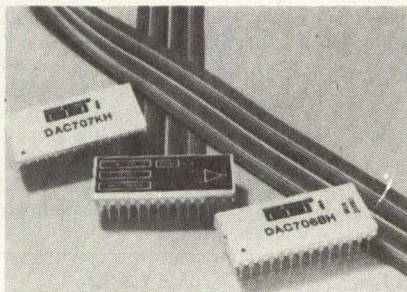
The DAC710KH and DAC711KH are 16-bit monolithic DACs which provide high resolution monotonic output transitions around bipolar zero. The DAC710KH provides ±1 mA current output while the DAC711KH offers a ± 10 V output. Both accept complementary binary coded digital input and are TTL, LSTTL, 54/74HC compatible. The DAC711Kh adds a low noise, fast settling op amp to its single chip. Both models are packaged in hermetic 24-pin ceramic dual wide DIPs. Price, in quantities of 100, is $29. **Burr Brown**, Tucson, AZ   **Circle 195**

NEW PRODUCTS

BOARDS

CACHE BUFFER COUPLER
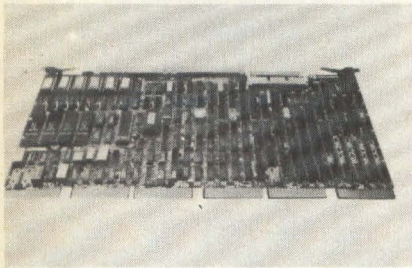
The Tape Dimension IV CacheCoupler is a cache buffer coupler which emulates the DEC TS11 tape subsystem. The TD-IV coupler contains a 64 Kbyte cache buffer and provides the interface for an industry compatible formatted streaming tape drive at 1600, 3200 or 6250 bpi at speeds up to 125 ips. It also supports start/stop tape drives at densities up to 6250 bpi and tape speeds of 200 ips. The TD-IV provides total immunity to "data late" conditions of heavily populated buses while maintaining the tape at streaming speeds. **Western Peripherals**, Tustin, CA   Circle 198

MULTIBUS HOST ADAPTER

The MBO1 host adapter provides an 8-bit data path link between the microcomputer Multibus and the SCSI interface. It can be applied to the Multibus system as a standalone host adapter or as a component used with Emulex's micro-storage subsystems, including the Javelin. The MBO1 can be configured for either serial or parallel bus arbitration through DIP switch selection, and responds to vectored and non-vectored interrupts. It can support 8-, 16- or 24-bit I/O addressing with response time under 350 nsec. It also supports 8- and 16-bit microprocessors. Power requirement is +5 V ±5% at 1.1 amps maximum. Price is $695. **Emulex**, Costa Mesa, CA
Circle 199

DIAGNOSTIC CARD
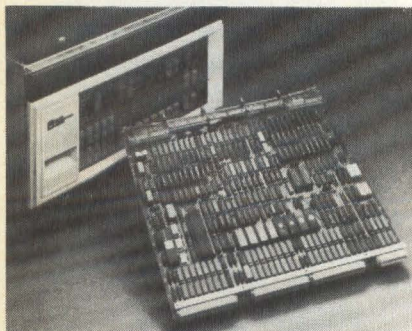
The MK8151 diagnostic card is designed specifically for the MK8200 general purpose mass memory system family. The MK8151 verifies that the MK8200 system is fully functional before it is placed online. The MK8151 features a test processor which can execute up to 12 different diagnostic algorithms and report any failures to its built-in diagnostic log. Operator-selectable scope loop tests can assist in isolating system problems. The user can communicate with the MK8151 via the control and display panel, and integral RS-232-C serial link, or the front panel bus. Price is $6,500. **Mostek**, Carrollton, TX
Circle 200

DR11-W EMULATORS FOR VERSA BUS AND VME BUS

The 10083 and 10084 provide pin-compatible emulations of DEC's DR11-W parallel DMA interface which can link to the PDP11, VAX or any device with a DR11-W compatible interface. Both use DEC-style unified bus transceivers for all external signals. Byte swapping is provided with separate switches for DMA and programmed I/O. The 10083, for VERSA bus computers, is available in etched board form. It uses the 32-bit features of the VERSA bus with a bus efficiency of an 8+ Mbyte/sec device. The 10084, for VME bus computers, has a transfer rate of 2 Mbyte/sec and bus efficiency of a 4 Mbyte/sec device. Price is $2,150 (10083) and $1,550 (10084). **Ikon**, Seattle, WA   Circle 201

MEMORY ENHANCEMENT BOARDS

The PC/Memory Plus Clock board and the PC/Short Memory board provide memory expansion and functional enhancement for the IBM PC family and compatibles. The Persyst PC/Memory Plus Clock is a full-size, multifunction board that supports up to 576 Kbytes of socketed RAM and occupies a single PC slot. It features memory capacity expandable in 64 Kbytes increments, and a clock/calendar with an on-board five year battery. The PC/Memory Plus Clock offers split memory addressing, a software lock feature, and includes the Insta-Drive and the Wait-Less Printing software programs. The PC/Short Memory board is a 4″ × 5″ board which mounts in the short expansion slot of the IBM PC/XT or Portable to provide 384 Kbytes of add-on memory. Board memory is available in five configurations, expandable in 64 Kbytes increments. Memory capacities of 128 Kbytes, 192 Kbytes, 256 Kbytes and 384 Kbytes are switch selectable. Price is $345-$1,145 (PC/Memory) and $259-$759 (PC/Short). **Emulex**, Costa Mesa, CA
Circle 202

LAN HARDWARE, SOFTWARE

The LAN hardware product line includes the LANS100 and S100 bus LAN controller card, the WS80 processor board which converts dumb terminals into 8-bit intelligent workstations with onboard LAN capability, and the LANPC controller card which allows integrating PCs and PC lookalikes into ICM's LAN. The MicroNet networking system links these hardware products. MicroNet is TurboDOS based. ICM's product line allows building of multi-user networks with any combination of S-100 bus structured networks, IBM PCs or lookalikes and 8-bit individual workstations. **ICM**, Anaheim, CA   Circle 203

ONE MBYTE VME CPU

The DVME102 68000/68010-based CPU card has two serial RS-232C channels, optional 68451 MMU, two 28-pin byte wide PROM sockets and one software controlled status LED. Byte parity generation and checking is provided for onboard DRAM. Two serial channels support either sync or async modes, and two independently controlled baud rate generators are provided. Onboard system controller functions include system clock, bus time out, single level arbiter, poweron and pushbutton reset. Seven interrupt levels are supported. Price is $5,063. **dy4 Systems**, Ottawa, Ontario   Circle 169

HARDCOPY INTERFACE FOR MULTIBUS
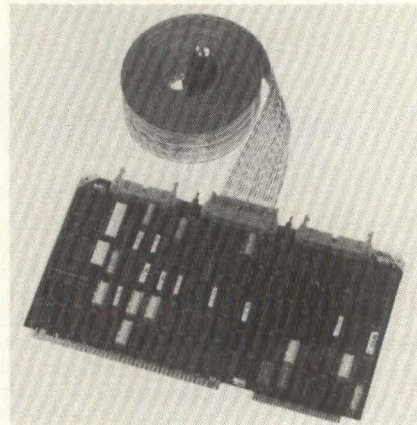
The Ikon Model 10085 is an interface which expands the hardcopy output potential of any Multibus computer system. It interfaces to Versatec electrostatic plotter/printers, Imagen laser printers, Tektronix color copiers, and any Centronics-compatible device. The 10085 uses all bipolar async DMA logic providing a board transfer rate of up to 1 Mbytes/sec. On-board diagnostic and device exercising is available by flipping an edge-mounted toggle switch. Test patterns in PROM can be tailored to customer specifications. Price is $1,100. **Ikon**, Seattle, WA
Circle 205

CONTROLLER BOARD

The ACB-4010 is a controller board capable of controlling hard-sector, removable disk drives. It has the features of the ACB-4000 controller, including non-interleaved operation for rapid data transfer and sector-level defect skipping. Combining the ACB-4010 controller board with the 11R disk drive provides reliable data interchange at high track densities in applications such as image processing and data logging. Price in quantities of 100 is $225. **Adaptec**, Milpitas, CA   Circle 206

16-BIT SINGLE BOARD COMPUTER
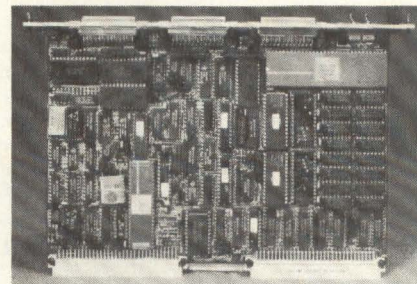
The PME-68-1B is a VME bus single board computer with a 32-bit 68000 CPU (8 MHz optionally 10 MHz) and up to 512K on board RAM. It features 16 Kbytes firmware expandable to 64 Kbytes, 3 serial RS-232-C I/O ports with jumper selectable baud rates from 110 to 38400 baud and a 16-bit parallel port. Furnished as a double Eurocard 234 × 160 mm, the PME-68-1B provides 24 address lines, 16 data lines, priority bus arbitration, interrupt control, system clock generation and special control lines for data handling. All seven interrupt lines are fully implemented. **Plessey Microsystems**, Pearl River, NY   Circle 207

SINGLE BOARD COMMUNICATIONS COMPUTER
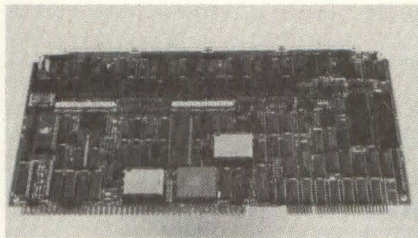
The iSBC 188/48 communications board distributes processing functions by offloading data from a host computer. It can function as a cluster controller, a front-end processor or a standalone system. The iSBC 188/48 board contains eight high performance I/O channels, dual-port RAM and sites for PROM/EPROM. The iSBC 188/48 board can provide cluster control where communications functions are concentrated in a central area, act as a front-end processor and serve as a standalone communications computer. It contains an 80188 microprocessor, four 82530 serial communications controllers that provide eight channels of I/O, 64 Kbytes of dual-port RAM and two universal memory sites accommodating up to 64 Kbytes of PROM/EPROM. Price is $2,995. **Intel**, Hillsboro, OR
Circle 147

NON-VOLATILE VME BUS MEMORY BOARD

The MM-6600C VME bus-compatible board provides up to 256 Kbytes of non-volatile memory with a cycle and access time of 200 nsec. Non-volatile operation is achieved with 8K × 8 CMOS RAMs and on-board batteries. The board can use CMOS RAM and EPROMs. With no CMOS RAM, the MM-6600C can provide 512 Kbytes of 2128 EPROMs and can also mix CMOS RAM and EPROM in equal proportions. Other features include 24-bit random access address of up to 16 Mbytes, address modifiers in EPROM that support both user and supervisory modes, module selection on 1000_H boundaries, single 5V supply @ 850 mA, and operating temperature of 0 to +65°C. Price is $1,750. **Micro Memory**, Chatsworth, CA
Circle 150

VIDEO ACQUISITION AND DISPLAY BOARD FOR IBM PC

Baby Blue Eyes (IVG-128) is designed to provide real-time video acquisition and display capabilities for the IBM PC family. Features include low-power consumption through CMOS components, 384 × 512 × 8 bits/pixel resolution matching CCD cameras and 256 grey levels of pseudocolor from a palette of 16M colors. Two bands of 256 × 8 bit input look-up tables provide binary thresholding and gain linearity control. Six banks of 8 bit LUT provide pseudocolor RGB or greyscale transformations on output. The board is rated for +5V @ 2.9A (max), +12V @ 0.25A (max). Price is $2,995. **Datacube**, Peabody, MA
Circle 149

IBM PC-COMPATIBLE VIDEO BOARD

Based on a Motorola 6845 video display controller, the PC Video Board can be programmed to create a range of timing characteristics allowing connection to color and monochrome display monitors. Featuring variable wait states, up to eight boards can be accessed independently with the PC Video Board. The board comes with 16 Kbytes of static CMOS RAM, 24-bit memory addressing and 16-bit addressing for I/O ports, and meets IEEE 696/S-100 timing specifications. In the color display mode, the graphic screen offers 160 horizontal by 200 vertical

8088-BASED CHANNEL COMMUNICATION PROCESSOR

The ZADC-518 Multibus board set incorporates either a complete microcomputer system or an intelligent communications controller into a two-board set. The ZADC-518 offers eight 8088 controlled full-duplex communication channels. Each channel has a software selectable protocol and baud rate. The board has async, character sync (monosync and bisync) and bit sync (HDLC, SDLC, CCIT ×.25) communications protocol capability. Four channels can operate under high speed DMA control and four channels are medium speed interrupt driver channels. The ZADC-518 communications capabilities are controlled by an 8088-based processor board. Price in quantities of 100 is $1,850. **Zendex**, Dublin, CA
Circle 155

pixels in 16 colors using an alphanumeric 4 × 2 dot character box, 320 horizontal by 200 vertical pixels in four colors, or 640 horizontal by 200 vertical pixels in one color and black. In the monochrome mode, the graphic screen features 320 or 640 horizontal by 200 vertical pixels. Price is $495. **CompuPro**, Hayward, CA
Circle 157

VOICE INPUT AND OUTPUT BOARD FOR IBM PC
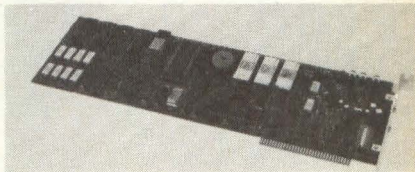
The SAR-10 Voice Plus is a fully integrated voice recognition and audio response plug in board for IBM PC. The voice recognition function uses a custom LSI chip set with 250 word capability. Spoken inputs are digitized and user defined ASCII outputs are sent to the PC. ADPCM chip digitally reproduces speech, as well as other sounds. The 256K DRAM stores 65 seconds of audio response at 32 bps. Price is $1,495. **NEC**, Melville, NY
Circle 153

Circle 8 on Reader Inquiry Card

VME BUS 1 MBYTE MEMORY BOARD
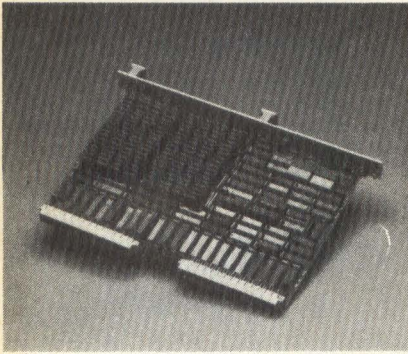
The MK75702 VME bus dynamic RAM board features a longword cache with typical read access time of 135 nsec on a cache hit, and 300 nsec on a cache miss. It is also available with or without parity generation and checking. This board is capable of byte (8 bit), word (16 bit), or longword (32 bit) data transfers. The MK75702 contains a control and status register (CSR), which allows on-board option selection by software and programmable starting address on any 4K boundary. Other features include 23-bit address and access and status LED indicators. Address modifiers are decoded in a PROM. Price is $3,500. **Mostek**, Carrollton, TX   **Circle 151**

IBM PC SINGLE-BOARD COMPUTER

The Colby single-board computer is physically identical to the IBM PC board. It offers integration on a single IBM-PC format eight 1/2″ × 12″ printed circuit board. The board can hold up to 256K of RAM (using 64K RAM chips), 8 Kbytes of EPROM, and integrated floppy disk controller which can operate dual 5 1/4″ floppy drives, an integrated SASI hard disk interface, an 8088 processor and an optional 8087 coprocessor. Price is $569. **Colby Computer**, Mountain View, CA   **Circle 156**

INTELLIGENT MODEM INTERFACE BOARD

The Model MOD-MB intelligent modem for the IBM PC family and compatibles is Bell 212A and 103 compatible and features auto dial and auto answer. The modem's auto dialer can be instructed to dial either voice or data calls. The board automatically selects DTMF tone or rotary pulse dialing. There is an auxiliary RS-232C port standard for connecting a printer for hard copy. Price is $345. **Metra Byte**, Stoughton, MA   **Circle 152**

SOFTWARE

UPGRADED SOFTWARE FOR DATA ACQUISITION/ SIGNAL ANALYSIS SYSTEM

Version 1.2 is an upgrade of the Version 1.1 Instrument Operating System software package for the DASA 9000 Data Acquisition/Signal Analysis System. The 1.2 IOS software transforms the DASA 9000 into a transient recording workstation. In its 8-channel configuration, the unit functions as a general purpose bench instrument with more signal handling capability than a dual-trace DSO. The 1.2 software allows the user to trigger the signal digitizing subsystem directly from the keyboard, to capture and display selected snapshots of up to eight dynamic signals for examination, further processing and/or storage on disk. Subroutines built into the 1.2 software allow users to command calculations on displayed waveforms. Price is $13,615. **Gould**, Cleveland, OH   **Circle 184**

RELIABILITY PREDICTION SOFTWARE FOR IBM PC

The RelCalc 2 software package features the ability to automate MIL-HDBK 217D part stress procedure, part parameter entry and editing, part forms with menu windows for each field entry, global editing functions, reports and part library. RelCalc 2 is appropriate for military and commercial applications, proposal feasibility studies, design phase tradeoffs, final design predictions, cost reduction analysis and warranty analysis. Price is $1,500. **T-Cubed Systems**, Westlake Village, CA **Circle 185**

CAD/CAM SOFTWARE

The AIM (Artwork Input Module) software program allows the conversion, merging and manipulation of printed circuit board and hybrid artwork from one file to another, regardless of the PCB CAD system on which it was created. The purpose of AIM is to read artwork data from magnetic tape and convert it into a Paragon-compatible database. AIM facilitates the updating of wiring and parts lists and design rule checking of the converted database. It requires a magnetic tape drive, 7″ or 10″, both offered by Paragon at 800 or 1600 bpi, and can be paired with any Paragon workstations. Price is $5,000. **Paragon**, Pleasant Hill, CA   **Circle 187**

SIMULATION SOFTWARE PACKAGE

Torlog is a logic simulation software package which runs on engineering computers. Torlog simulates the logical operation of a digital network. Modeling elements are input clocks, standard and clocked gates and ROMs, RAMs and PLAs. Standard logic levels are low, high, and indeterminate, with checking for spike conditions. To simplify data entry, groups of logic elements may be first defined and later repeated with selected changes. Price is $6,000. **Torric**, Scottsdale, AZ   **Circle 188**

ETHERSERIES SUPPORT FOR IBM PC AT

The LAN hardware and software that support MS-DOS 3.0 are compatible with networked IBM PCs, PC/XTs and compatibles, HP 150s and TI Professionals running MS-DOS 2.0 and 2.1. Using the EtherSeries product line, customers can link the IBM PC AT to products from multiple vendors for sharing networked application software, disks and printers as well as sending electronic mail. EtherSeries software permits the use of the PC AT as an EtherSeries network server and a full functional workstation. **3Com**, Mountain View, CA   **Circle 204**

BEHAVIORAL MODELING LANGUAGE

With the addition of ADLIB behavioral modeling language, Lasar Version 6 can perform true mixed mode simulation at any level, from device submodules to entire systems. Lasar Version 6 is able to maintain simulation accuracy through a behavioral model, because ADLIB supports four logic states: 1s, 0s, tristate outputs and Xs. The behavioral circuit module is evaluated by Lasar Version 6 at a rate 30-50 times faster than the equivalent structural representation. Functional timing characteristics, including minimum and maximum propagation delays and input timing constraints, can be assigned to a behavioral model using the Chronos timing language in Lasar Version 6. **Teradyne**, Boston, MA   **Circle 221**

BASIC INTERPRETER STORED ON-CHIP

The MCS BASIC-52 package includes the 8052AH chip and features eight-digit floating point arithmetic, a built-in capability to program an EPROM and EEPROM and a user accessible function library. The floating point math capability allows control algorithms to be calculated directly using MCS BASIC-52. The built-in EPROM and EEPROM programmer and a file management system let a programmer write a program and save it in an EPROM/EEPROM that is already installed in the target system. The file management structure on the chip permits up to 225 programs to be stored in the EPROM/EEPROM. Price in quantities of 1,000 is $45. **Intel**, Chandler, AZ   **Circle 189**

ELECTRONICS DESIGN SIMULATION SOFTWARE

The SALT program, a logic and timing analysis program for chips, boards and systems, accepts input directly from Control Data's electronics design workstation, which allows entry of schematics, extract netlists and design documentation. The program features dynamic circuit timing, automatic computation of fan and fan-out delays, multiple checkpoint restart, rapid recompilation of networks through incremental compilation, classification of transistors as uni-or bidirectional, critical path determination, output assertions and multi-level simulation. **Control Data**, Santa Clara, CA   **Circle 190**

COMMUNICATION SOFTWARE

The 3B BLAST for AT&T's 3B Series minicomputers links AT&T computers with any computer running BLAST software. A virtual file format translates text file formats between operating systems. Binary data, operating system files, programs, executable commands or text data can be transferred. BLAST operates out of standard RS-232 ports and on regular dial-up telephones. It uses async modems or can be directly cabled at speeds to 19.2 Kbaud. Price is $250+ (micros/minis) and $2,495 (mainframes). **Communications Research Group**, Baton Rouge, LA   **Circle 219**

DATA ACQUISITION AND CONTROL SOFTWARE

ProGen software allows the user to program up to 500 I/O channels in batch processing, process control and automated testing. Compatible with Fluke's 2425 Measurement and Control System, ProGen features two separate disks for programmer and operator functions. No programming knowledge is required to use ProGen. It allows an application to be divided into task groups; each task group consists of related channels that can be priortized as necessary for the given application. The operator disk is created directly from the programmer disk through

a selection on the main menu. ProGen automatically chains scan tasks together, performs limit checking and runs the defined procedures. Price is $2,990. **Fluke**, Everett, WA **Circle 181**

CSI LINKS UNIX TO IBM

The Access/SNA 3270 links UNIX systems to IBM mainframes through IBM's SNA. Access/SNA, written in the C language, can be used with UNIX System 3, UNIX System V and Xenix systems. It can connect any ASCII terminal to an SNA network to simultaneously support different types of printers and to perform the functions of 3270 cluster controllers. With the UNIX version of Access/SNA, single and multi-user UNIX systems can emulate IBM systems such as the 3274/3276, 8100 and 3770. The UNIX version of Access/SNA can also co-exist with other UNIX products. Price is $75,000-$100,000. **CSI**, San Jose, CA **Circle 220**

TERMINAL SUPPORT SOFTWARE

The Acces Network Virtual Terminal Service (VTS) software package permits transparent communication between terminals and hosts on a network. It provides a uniform terminal interface that does not change due to operating system differences or terminal characteristics. Incompatibilities between terminals and hosts are resolved by Acces VTS through a translation to a single network terminal format. The interface is the same for any host terminal or network a user selects. Acces VTS also features intelligent buffering and flow control. Acces VTS currently supports the ASCII terminals on VAX/VMS and UNIX operating systems. **Advanced Computer Communications**, Santa Barbara, CA **Circle 192**

PASCAL COMPILER

The Pascal-2 compiler was developed by Oregon Software for UniSoft's UNIX-based operating system, UniPlus. Pascal-2 programs can call subroutines written in C or assembler, allowing the user to take advantage of existing UniPlus software. Program development tools include a high-level interactive debugger and an execution profiler. The Pascal-2 compiler supports all capabilties of standard Pascal and conforms to level one of the ISO 71885. Pascal-2 features eight types of code optimization, global register allocation, common subexpression elimination, expression targeting, array index simplification, range tracking, constant folding, dead-code elimination and short circuit evaluation. Price is $1,000. **Unisoft Systems**, Berkeley, CA **Circle 182**

PROTOCOLS FROM INTEL AND MICROSOFT

Intel and Microsoft have developed network software protocols that allow files to be shared concurrently by multiple users on a LAN. The network protocols are fully compatible with IMB's PC Network. The protocols are the basis of the Microsoft Networks software that allow network file access among micros using the MS-DOS operating system. They will be used by OEMs building networked microcomputer systems for software development, transaction processing and data collection. The new protocols are hardware independent and can support systems based on Xenix, iRMX, PC-DOS and MS-DOS. **Intel**, Santa Clara, CA **Circle 186**

SOFTWARE FOUNDATION FOR FACTORY AUTOMATION

The Baseway software package is designed to integrate industrial controllers with manufacturing applications. The package consists of three software components: the Shop Floor Gateway, Baseway Application Software Bus and Programmable Device Support. The Shop Floor Gateway is an intelligent hardware/software communication device, running on a PDP-11 system which acts as a translator between specific shop floor devices and a host computer. The Programmable Device Support software is a menu-driven application that is capable of uploading/downloading, reading/writing, comparing, documenting and maintaining a library of ladder logic programs. Price is $4,000. **DEC**, Maynard, MA **Circle 191**

UNIX OPERATING SYSTEM FOR IBM PC/AT

The Encore version is an update of the original Venix operating system (Venturcom, Inc.) and represents a second generation of high performance UNIX software from Unisource. The kernel and driver have been squeezed into 50 Kbytes so they reside permanently in main memory. The package contains Berkeley extensions (vi, termcap, more and C shell), real time capability (raw I/O, shared data segments, I/O page addressing and async I/O), record-locking and graphics support (plot and graph for medium-and high-resolution graphics). **Unisource Software**, Cambridge MA **Circle 183**

GRAPHICS SUPPORT PACKAGE

Developed to provide an interface between the HSR-11B high-speed raster processor and applications software compatible with Applicon, Calcomp, Versaplot 7, and optionally Precision Visuals DI-3000 and GK-2000 graphics packages, the HSRCOL graphics support package for the Versatec ECP42 plotter handles all plotter control functions and transfers the color rasterization process from the host to the HSR-11B. This combination, called Speedcolor, provides increased color throughput and reduced CPU time for existing applications programs. Speedcolor is an addition in AMF Logic Sciences' line of rasterizing products and simplifies support of the Versatec color plotter on IBM, Amdahl, DEC, Perkin-Elmer, CDC and Gould SEL computer systems. **AMF Logic Sciences**, Houston, TX **Circle 224**

SOFTWARE SUPPORT DISKETTE

The PCI-4901-1 Software Support Diskette, PCI Soft, provides the user with a dedicated set of basic callable subroutines for operations of the PCI-4301 series of instrumentation boards. The 5¼" floppy diskette allows the user to read and write directly to the I/O channels. The program incorporates a Reference Table to define the I/O points, a BASIC Call Routine package and an Edit package for updating the reference table. It also provides thermocouple compensation and linearization. Price is $425. **Burr-Brown**, Tucson, AZ **Circle 223**

Technical Literature Package. Techniques for Time Interval Measurement are described in a set of four application notes and supporting technical data sheets from LeCroy Research Systems Corp. Discussed are how time measurement problems can be addressed by using modular, computer interfaced, precision, real-time and quasi real-time time interval meters, histogramming memories, and programmable, precision gate and delay generators.
**LeCroy** **Circle 261**

Microcomputer Board Data Book. This data book from Motorola describes 16- and 32-bit microcomputer board-level products. Chapters cover VME modules, VERSA modules, I/O modules, operating systems, development systems, system bus technical summaries, and customer support. Technical specifications, photos, charts, and graphs are also included.
Motorola **Circle 256**
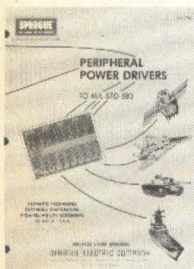
Peripheral Power-Drivers Catalog. This 12-page catalog from Sprague Electric Company's Integrated Circuit Operations describes the peripheral power drivers it furnishes in accordance with MIL-STD-883. Illustrated are 59 different integrated circuits intended for military and aerospace applications.
Sprague **Circle 260**
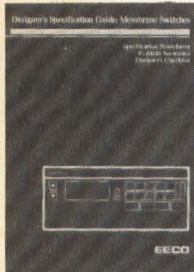
Membrane Switch Guide. This eight-page guide from EECO Inc. will help in the design of membrane switch panels. Contained is information that will aid the designer in communicating membrane switch requirements to the manufacturer. Diagrams showing procedures, and a design checklist are also included.
**EECO** **Circle 262**
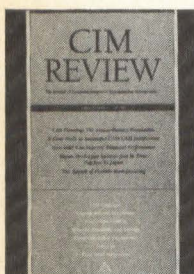
CIM Review. This quarterly journal from Auerbach Publishers addresses aspects of computer integrated manufacturing systems from a strategic planning and implementation viewpoint. Explored are the current and potential uses and applications. Offered are recommendations on procedures, policies, and timing of decisions.
Auerbach **Circle 263**
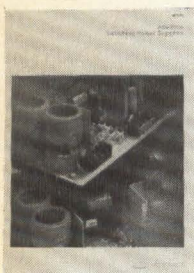
Switching Power Supplies Brochure. This brochure describes a line of switching power supplies. Included are high-efficiency open-frame, modular, enclosed and miniature units for use in a variety of business, industrial, consumer and military products and systems. These rugged switchers operate at 110 or 220 Vac nominal, and provide single or multiple, low-noise, low-ripple, highly-regulated outputs at all common potentials from 2 to 28 Vdc, with power ratings from 25 to 750 watts.
**Advance Power Supplies** **Circle 259**

A/D, D/A Superposition Errors Application Note. This four-page note from ILC Data Device Corp. (DDC) defines A/D and D/A converter superposition errors and is illustrated with examples of these errors in various applications. Suggestions are included for identifying and eliminating or reducing superposition errors in each application. A table shows results of a typical linearity test.
**DDC** **Circle 250**
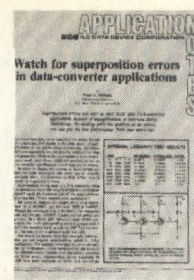
Microcomputer Software Catalog. This 24-page catalog from Scientific Software Products, Inc. describes scientific software for the IBM PC and Apple II computers, plus hardware, books and accessories for microcomputer users. All software in the catalog has been evaluated, and technical support services are described.
**Scientific Software** **Circle 252**
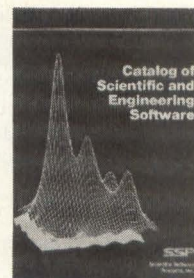
Vision Products Brochure. This 16-page brochure from Chorus Data Systems discusses adding vision to personal computer graphics and database management systems. Covered are PC-Eye, a video capture system board; ImiGit, an icon-driven graphics system; and PhotoBase, a software package. Contained is information on applications, system configuration and specifications.
Chorus **Circle 254**
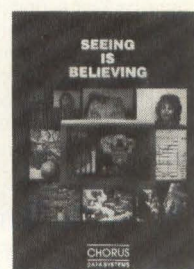
VLSI Products Catalog. This six-page catalog on VLSI products for Digital Signal Processing from TRW LSI Products Div. offers applications on currently available multipliers, multiplier-accumulators, A/D and D/A converters, storage products, and special function products. Also listed is availability of products.
TRW Electronic **Circle 251**

DC-DC Converters. This 48-page catalog from Power General contains technical data on its line of DC-DC converters. Products are organized into selection charts and are followed by data sheets.
**Power General** **Circle 264**

CAD/CAE Implementation Book. This 288-page report from Electronic Trend Publications addresses the impact of CAD/CAE upon the design of VLSI integrated circuits and the shift of the design control from the traditional IC manufacturer to the end user. It is written for the design manager of the equipment manufacturers and deals with the application of CAD/CAE tools and the impact on his design approaches and organization. Also profiled are CAD/CAE hardware and software companies.
**Electronic Trend** **Circle 253**
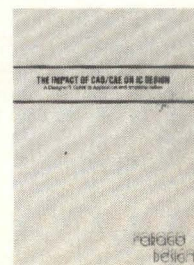
NEW LITERATURE

Microcomponents Catalog. This 45-page catalog from Digital Equipment Corp. lists the l6-bit processors, modules, chips, peripheral equipment and software that make up its Q-bus family of computer products. Described are operational capabilities and principal applications of the MicroPDP-ll computer, LSI-ll/73, LSI-ll/23-Plus and LSI-ll/23 central processors, Falcon and Falcon-Plus single-board computers, as well as Jll and Tll chip-level microcprocessors.

DEC   Circle 257
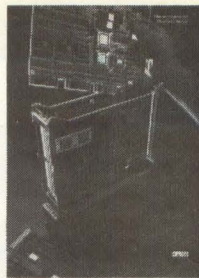
Telecommunications Data Book. This reference guide from Motorola Logic and Special Functions Div. provides technical data for the design engineer of telecommunications devices. Seven chapters offer information to aid in the application of devices and completion of systems using its semiconductor products. Included are specifications, applications notes and technical articles.

Motorola   Circle 265
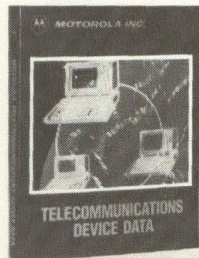
Microminicomputer Report. This 250-page book from Electronic Trend Publications examines issues surrounding an increase in microcomputer utilization and the strategic impact on manufacturers and component suppliers. The report looks at the technology and design trends driving the current 8−, 16− and 32−bit micromini increase, including a look at the corporate computer future for 1990.

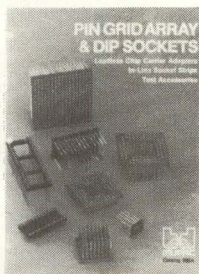**Electronic Trend Publications**   Circle 266
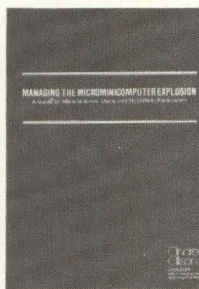
Surface-Mount Components Brochure. This 24-page brochure from Sprague Electric Co. describes its surface-mount components. These include multi-layer ceramic and solid tantalum capacitors, resistor networks, discrete semiconductors and integrated circuits.

Sprague   Circle 267

Surface Mounting Directory. This directory from D. Brown Associates serves to help the electronic industry keep up with surface mounting technology. Discussed are developments in product and service availability, as well as trends in the technology.

D. Brown   Circle 268

Pin Grid Array and Dip Sockets Catalog. This 16-page catalog from Mupac Corp. outlines its line of PGA, DIP and SIP sockets plus leadless chip carrier adapters and test accessories. Also contained are specifications, photos, features, line drawings and ordering information.

Mupac   Circle 269

CALENDAR

February 26-28

Automated Design and Engineering for Electronics. Anaheim, CA. Contact: Show Manager, ADEE, 1350 E. Touhy Ave., Des Plaines, IL 60018. (312)299-9311.

February 26-28

Nepcon West '85. Anaheim, CA. Contact: Show Manager, Nepcon West '85, 1350 E. Touhy Ave., Des Plaines, IL 60018. (312)299-9311.

March 4-6

Data Communications. Boston, MA. (Also in New York, NY, March 25-27). Contact: Data-Tech Institute, Lakeview Plaza, PO Box 2429, Clifton, NJ 07015. (201)478-5400.

March 4-6

Network Design. Boston, MA. Contact: Seminars, Educational Services — MS F019, Data General Corp., 4400 Computer Drive, Westboro, MA 01580. (617)366-2900.

March 12-14

Surface Mounted Device Technology Seminars. Milwaukee, WI. Contact: North American Philips SMD Technology, Seminar Dept., 5855 N. Glen Park Rd., Milwaukee, WI 53209. (414)228-7632.

March 12-15

Knowledge-Based Systems, AI & 5th Generation Computing. Washington, D.C. (Also in San Diego, CA, March 26-29). Contact: Ruth Dordick, Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213)417-8888.

March 21-22

Second Annual International Conference on Artifical Intelligence for Robotics. Arlington, VA. Contact: Dr. Diener, IIT Research Institute, 10 W. 35th St., Chicago, IL 60616. (312)567-4376.

March 21-24

COMDEX/Winter. Anaheim, CA. Contact: The Interface Group, Inc., 300 First Ave., Needham, MA 02194. (617)449-6600.

March 25-28

IEEE Infocom '85. Washington, D.C. Contact: IEEE Infocom '85 Publicity Chairman, Room 1855, 160 Elgin St., Ottawa, Ontario, Canada K1G 3J4. (613)239-4510.

March 25-29

C Programming Workshop. Bellevue, WA. Contact: Specialized Systems Consultants, PO Box 7, Northgate Station, Seattle, WA 98125-0007. (206)367-8649.

March 26-28

Vision '85. (Conference on Applied Machine Vision). Detroit, MI. Contact: Society of Manufacturing Engineers, PO Box 930, Dearborn, MI 48121. (313)271-1500.

March 29

Systems Network Architecture Extensions and Products Seminars. Denver, CO. (Also in Chicago, IL, April 12). Contact: CSI, 922 S. Sunnyvale-Saratoga Rd., San Jose, CA 95129. (408)725-1568.

April 10-12

Structured Techniques Using 4th Generation Languages. Chicago, IL. Contact: Digital Consulting Associates, Inc., 6 Windsor St., Andover, MA 01810. (617)470-3870.

April 14-18

Computer Graphics '85. Dallas, TX. Contact: National Computer Graphics Association, Suite 601, 8401 Arlington Blvd., Fairfax, VA 22031. (703)698-9600.

April 16-18

ATE Silicon Valley '85. San Mateo, CA. Contact: Morgan-Grampian Exposition Group, Two Park Ave., New York, NY 10016-5667. (212)340-9780.

ADVERTISER INDEX