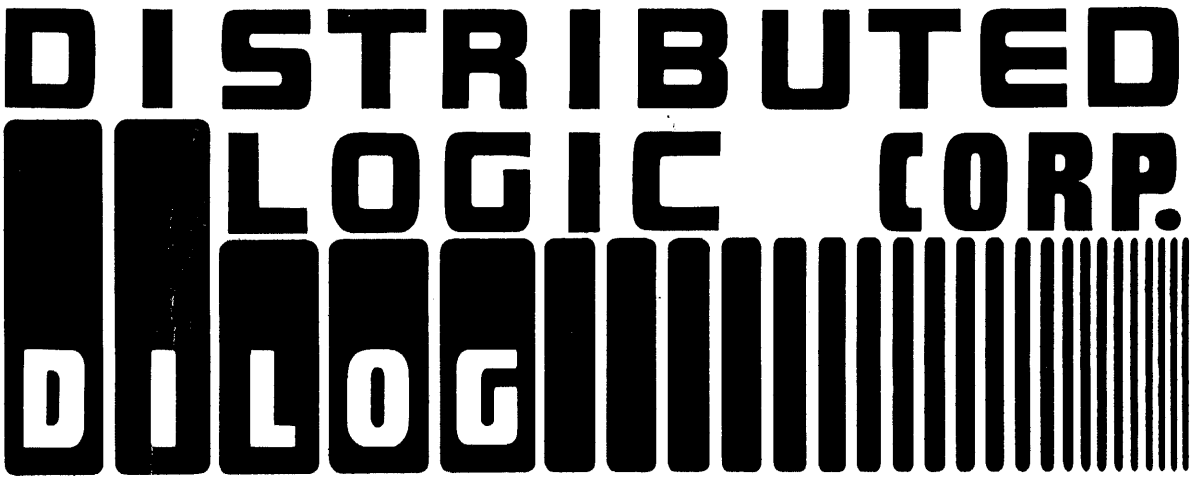
MODEL DQ202A
DISC CONTROLLER
INSTRUCTION MANUAL



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MODEL DQ202A DISC CONTROLLER INSTRUCTION MANUAL

September 1981

DISTRIBUTED LOGIC CORP.
DILOG

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DESCRIPTION

INTRODUCTION

This manual describes the installation, operation, programming, troubleshooting, and theory of operation of Distributed Logic Corporation (DILOG) Model DQ202A Disc Controller. The controller interfaces DEC* LSI-11 based computer systems to SMD I/O-compatible removable media or Winchester disc drives. The complete controller occupies one quad module in the backplane. Full sector buffering in the controller matches the transfer rate of the disc drive and the CPU. The controller is software compatible with DEC drivers, emulating RP02/ RP03 drives.

CONTROLLER CHARACTERISTICS

The disc controller links the LSI-11 computer to one or two disc storage units. Commands from the computer are received and interpreted by the controller and translated into a form compatible with the disc units. Buffering and signal timing for data transfers between the computer and the discs are performed by the controller.

A microprocessor is the sequence and timing center of the controller. The control information is stored as firmware instructions in read-only-memory (ROM) on the controller board. One section of the ROM contains a diagnostic program that tests the functional operation of the controller. This self-test is done automatically each time power is applied or under operator control by pressing the RESET switch. A green DIAGnostic indicator on the controller board lights if self-test passes.

Data transfers are directly to and from the computer memory using the DMA facility of the LSI-11 I/O bus. In addition, the controller monitors the status of the disc units and the data being transferred and presents this information to the computer upon request. The controller is capable of controlling up to two disc drives in various configurations up to a total on-line capacity of 419 megabytes. Figure 1-1 is a simplified diagram of a disc system.

One 60- and two 26-pin connectors, located near the top center of the controller board, are the connection points between the controller and the disc drives. The cable connected to the 60-pin connector conducts the daisy-chained control signals among the disc drives. Data signals between the controller and disc drives are conducted over the 26-pin cables.

LSI-11 Q BUS INTERFACE

Commands, data and status transfers between the controller and the computer are executed via the parallel I/O bus (Q bus) of the computer. Data transfers are direct to memory via the DMA facility of the Q bus; commands and status are under programmed I/O. Controller/Q bus interface lines are listed in Table 1-1.

*DEC is a registered trademark of Digital Equipment Corporation.

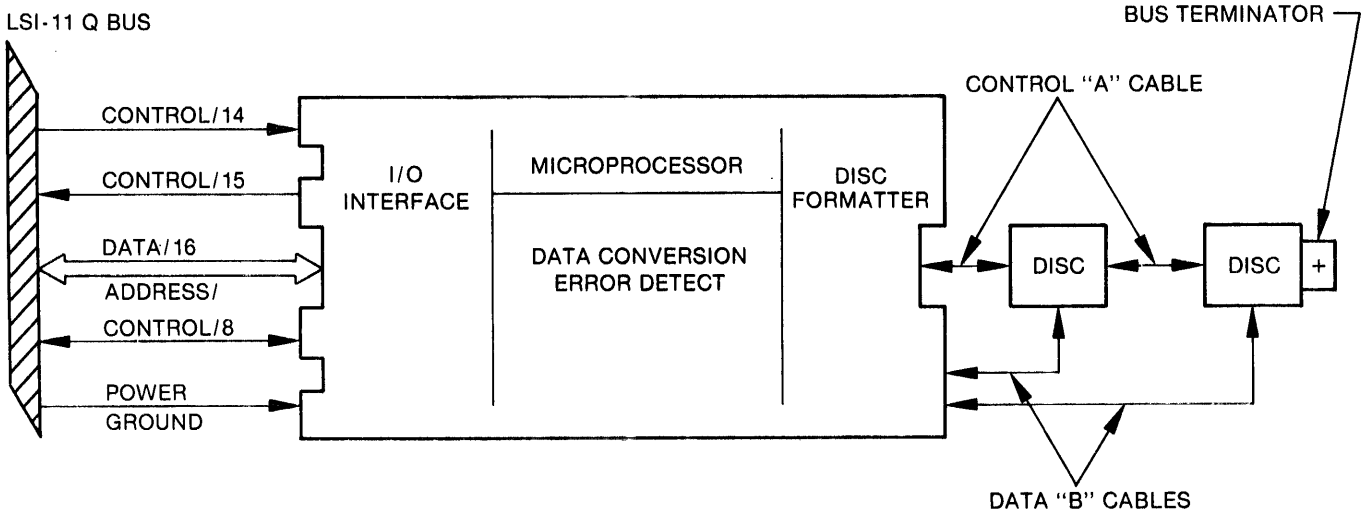


Figure 1-1. Disc Controller System Simplified Diagram

Table 1-1. Controller/Q Bus Interface Lines

BUS PIN	MNEMONIC	TO/FROM Q BUS	DESCRIPTION
AJ1, AM1, RT1	GND		Signal Ground and DC return.
AN1	BDMR L	To	Direct Memory Access (DMA) request from controller: active low.
AP1	BHALT L	To	Stops program execution. Refresh and DMA is enabled. Console operation is enabled.
AR1	BREFL	From	Memory Refresh
BA1	BDCOK H	From	DC power ok. All DC voltages are normal.
BB1	BPOK H	From	Primary power ok. When low activates power fail trap sequence.
BJ1, BM1, BT1, BC2	GND		Signal Ground and DC return.
BN1	BSACK L	To	Select Acknowledge. Interlocked with BDMGO indicating controller is bus master in a DMA sequence.
BR1	BEVNT L	To	External Event Interrupt Request.
BV1, AA2, BA2	+5	From	+5 volt system power.
AD2, BD2	+12	From	+12 volt system power.
AE2	BDOUT L	From/To	Data Out. Valid data from bus master is on the bus. Interlocked with BRPLY.
AF2	BRPLY L	From/To	Reply from slave to BDOUT or BDIN and during IAK.
AH2	BDIN L	From/To	Data Input. Input transfer to master (states master is ready for data). Interlocked with BRPLY.
AJ2	BSYNCL	From/To	Synchronize: becomes active when master places address on bus; stays active during transfer.
AK2	BWTBT L	From/To	Write Byte: indicates output sequence to follow (DATO or DATOB) or marks byte address time during a DATOB.
AL2	BIRQ L	To	Interrupt Request.
AM2 AN2	BIAK1 L BIAK0 L	From/To	Serial Interrupt Acknowledge input and output lines routed from Q Bus, through devices, and back to processor to establish an interrupt priority chain.
AP2	BBS7 L	From/To	Bank 7 Select. Asserted by bus master when address in upper 4K bank (28-32K words) is placed on the bus.
AR2 AS2	BDMG1 L BDMG0 L	From/To	DMA Grant Input and Output. Serial DMA priority line from computer, through devices, and back to computer.
AT2	BINIT L	From	Initialize. Clears devices on I/O bus.
AU2, AV2	BDAL0/DAL1	From/To	Data/address lines 0 & 1, (2 of 16)
BE2, BF2, BH2 BJ2, BK2, BL2 BM2, BN2, BP2 BR2, BS2, BT2 BU2, BV2	BDAL2 through BDAL15	From/To	Data/address lines, 2-15, (14 of 16)
AC1	BDAL16	To	Extended Address Bit.
AD1	BDAL17	To	

INTERRUPT

The interrupt vector address is factory set to address 254. The vector address is programmed in a prom on the controller, allowing user selection.

The controller generates interrupt requests to the computer if bit 6 or 13 in the controller register RPCS is set. Bit 6, Interrupt on Done (Error) Enable, raises an interrupt request when a disc operation is completed or if an error occurs. Bit 13, Attention Interrupt Enable, raises an interrupt request when a drive raises its attention line. If interrupts are enabled, bit 13 must be on. Interrupt requests are generated under the following conditions:

1. A hard error occurs.
2. A soft error occurs. Soft errors are either write check errors (WCE) or checksum errors (CSE).
3. The designated number of words has been transferred.
4. A selected disc drive has accepted a seek or drive reset command.
5. A seek or drive reset function has been completed.

DISC INTERFACE

The controller interfaces with the disc drive, or first of a series of disc drives, through the 60-pin and two 26-pin connectors at the center of the controller board. The maximum cable length from the controller to the last disc drives in a system is 100 feet. Ribbon cables connect the controller to the disc. The 60-pin "A" cable is connected serially among the disc drives. The 26-pin "B" cables are each connected to one disc drive. Table 1-2 lists "A" cable controller-to-drive interface lines. Table 1-3 lists "B" cable controller-to-drive interface lines.

Table 1-2. Controller To Drive I/O Interface — "A" Cable

Signal Name (DILOG Term)	Pin Polarity (Active)		Source
	–	+	
DEVICE SELECT 0 (USEL0)	23	53	Controller
DEVICE SELECT 1 (USEL1)	24	54	Controller
DEVICE SELECT 2 (USEL2)	26	56	Controller
DEVICE SELECT 3 (USEL3)	27	57	Controller
SELECT ENABLE (USTAG)	22	52	Controller
SET CYLINDER TAG (TAG1)	1	31	Controller
SET HEAD TAG (TAG2)	2	32	Controller
CONTROL SELECT (TAG3)	3	33	Controller
BUS OUT 0 (BIT0)	4	34	Controller
BUS OUT 1 (BIT1)	5	35	Controller
BUS OUT 2 (BIT2)	6	36	Controller
BUS OUT 3 (BIT3)	7	37	Controller
BUS OUT 4 (BIT4)	8	38	Controller
BUS OUT 5 (BIT5)	9	39	Controller
BUS OUT 6 (BIT6)	10	40	Controller
BUS OUT 7 (BIT7)	11	41	Controller
BUS OUT 8 (BIT8)	12	42	Controller
BUS OUT 9 (BIT9)	13	43	Controller
BUS OUT 10 (BIT10)	30	60	Controller
DEVICE ENABLE (OCD)	14	44	Controller
INDEX (INDEX)	18	48	Drive
SECTOR MARK (SEC)	25	55	Drive
FAULT (FAULT)	15	45	Drive
SEEK ERROR (SERR)	16	46	Drive
ON CYLINDER (ONCYL)	17	47	Drive
UNIT READY (UNRDY)	19	49	Drive
WRITE PROTECTED (WPRT)	28	58	Drive
ADDRESS MARK (AMF)	20	50	Drive
BUS-DUAL-PORT ONLY	21	51	Drive
SEQUENCE IN (PICK)	29		Controller
HOLD (HOLD)	59		Controller

Table 1-3. Controller To Drive I/O Interface — "B" Cable

Signal (DILOG Term)	Pin Polarity (Active)			Source
	–	+	Ground	
Ground			1	
SERVO CLOCK (SCLOCK)	2	14		Drive
Ground			15	
READ DATA (RDATA)	3	16		Drive
Ground			4	
READ CLOCK (RCLOCK)	5	17		Drive
Ground			18	
WRITE CLOCK (WCLOCK)	6	19		Controller
Ground			7	
WRITE DATA (WDATA)	8	20		Controller
Ground			21	
UNIT SELECTED (USEL)	22	9		Drive
SEEK END (SEEK)	10	23		Drive
Ground			11	
Reserved for Index	12	24		
Ground			25	
Reserved for Sector	13	26		

DISC FORMAT

DILOG's Universal Firmware Program performs two functions: the program formats the disc pack and partitions the pack for the user's application. Formatting is writing header records, which are address and flag information for use by the controller. The headers are detached; that is, the address and data portions of the sector are separated by a write splice gap. Details of formatting are described in Section 3 under Format and Diagnostic Test Program.

Partitioning is dividing the disc pack horizontally or vertically into logical units which the computer recognizes. The advantage of the Universal Firmware is that the operator may partition the pack for a particular application. Partitioning is described in detail in Section 3 under Format and Diagnostic Test Program.

CONTROLLER SPECIFICATIONS

- Data Format Emulation*
  - 512 data byes per sector
  - 10 sectors per track
  - Up to 404 (RP03) cylinders per disc drive
  - Up to 20 heads per cylinder
  - Maximum of 8 Logical Units per controller.
- Register Addresses:
  - Drive status (RPDS) 776 710
  - Error (PRER) 776 712
  - Control Status (RPCS) 776 714
  - Word Count (RPWC) 776 716
  - Bus Address (RPBA) 776 720
  - Cylinder Address (RPCA) 776 722
  - Disc Address (RPDA) 776 724
  - Data Buffer (RPDB) 776 726
- Computer I/O Interface:
  - Interrupt vector address 254.
- Disc Interface:
  - Control Data SMD Compatible
  - Controller is compatible with discs manufactured by Control Data, Ampex, Fujitsu, Century Data, PRIAM, Kennedy, etc. The connectors at the controller end are a 3M 60-pin and two 26-pin ribbon cable connectors.

*Actual drive parameters may be greater; for example, the controller is currently running a drive with 1645 cylinders per drive. See Table 3-1. Section 3, for a partial list of drive parameters.

- Bootstrap Loader:
  - On board bootstrap loader.
- Packaging:
  - The controller is completely contained on one quad module 10.45 inches wide by 8.8 inches deep. Optionally supplied with the controller are two 10-foot cables to the first disc drive. Adapter connectors may be required at the disc end depending on the disc manufacturer.
- Documentation:
  - One instruction manual is supplied with each controller.
- Power:
  - +5, ±.25 VDC at 3.5 AMPS
    +12, ±5 VDC at 0.3 AMPS
- Environment:
  - Operating temperature 50° to 140°F.
  - Operating humidity 0 to 90% non-condensing.
- Shipping Weight:
  - 5 pounds, including documentation.
- Options:
  - On-site installation, factory integration of disc. Complete disc systems.

SECTION 2
INSTALLATION

INSPECTION

The padded shipping carton that contains the controller board also contains an instruction manual and cables to the first disc drive (if this option is exercised). The controller is completely contained on the quad-size printed circuit board. The disc (or discs), if supplied, is contained in a separate shipping carton. Inspect the controller and cables for damage.

CAUTION

If damage to any of the components is noted, do not install. Immediately inform the carrier and DILOG.

Installation instructions for the disc drive are contained in the disc drive manual. Before installing any components of the disc system, read Sections 1, 2 and 3 of this manual. Figure 2-1 illustrates the configuration of the controller.

PRE-INSTALLATION CHECKS

There are various LSI-11 configurations, many of which were installed before DEC made a hard disc available for LSI-11 based systems. Certain configurations require minor modifications before operating the disc system. These modifications are as follows:

A. If the system contains a REV11-C module, it must be placed closer to the processor module (higher priority) than the controller if the DMA refresh logic on the REV11-C is enabled.

B. If the 4K memory on the DK11-F is not used and the memory in the system does not require external refresh, the DMA refresh logic on the REV11-C should be disabled by removing jumper W2 on the REV11-C module.

C. If the system contains a REV11-A module, the refresh DMA logic must be disabled since the module must be placed at the end of the bus (REV11-A contains bus terminator).

D. If the REV11-C module is installed, cut the etch to pin 12 on circuit D30 (top of board) and add a jumper between pin 12 and pin 13 of D30.

E. If the system requires more than one backplane, place the REV-11 terminator in the last available location in the last backplane.

INSTALLATION

To install the controller module, proceed as follows:

CAUTION

Remove DC power from mounting assembly before inserting or removing the controller module.

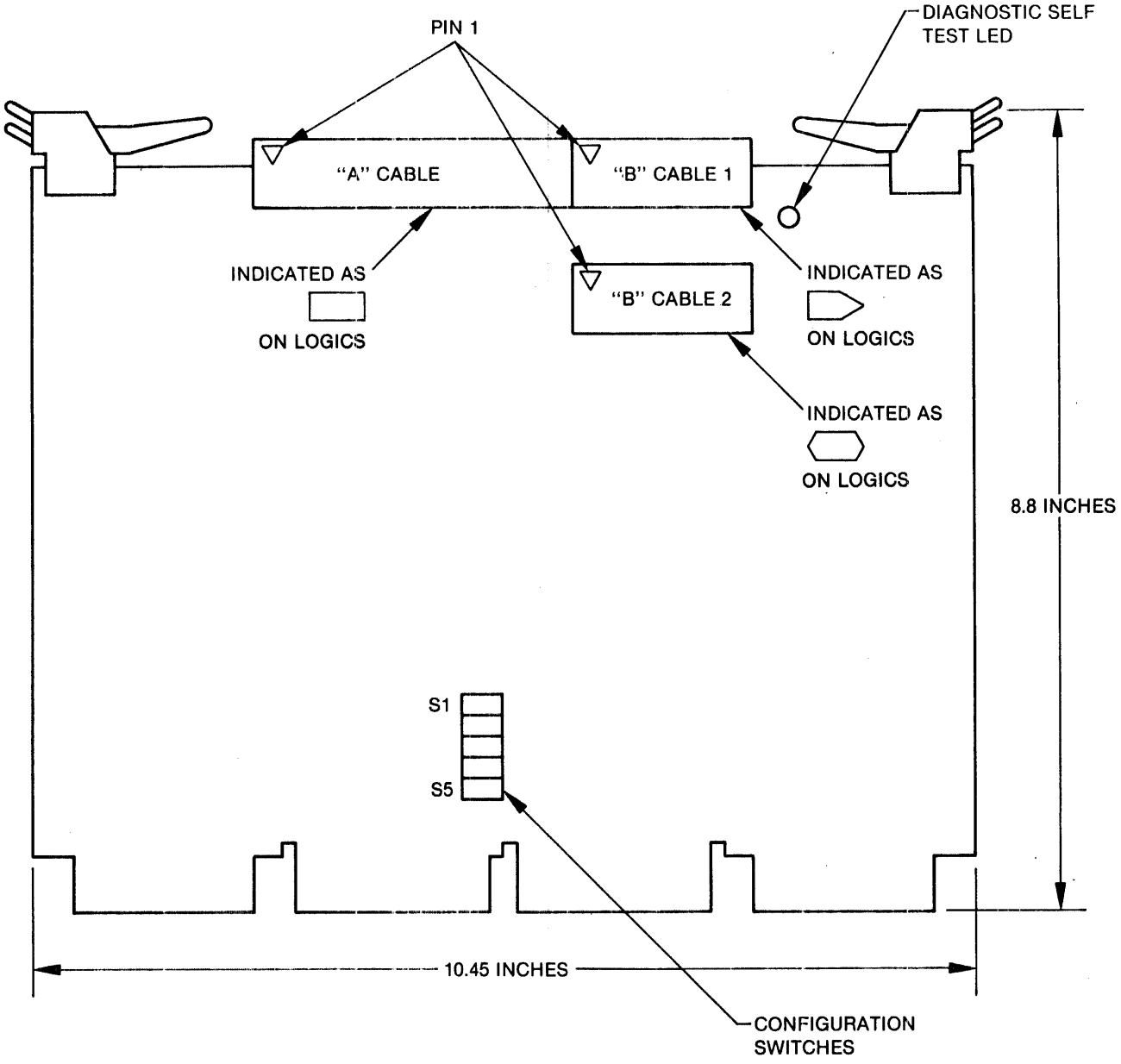
Damage to the backplane assembly may occur if the controller module is plugged in backwards.

1. Select the backplane location into which the controller is to be inserted. Be sure that the disc controller is the lowest priority DMA device in the computer except if the DMA refresh/bootstrap ROM option module is installed in the system. The lowest priority device is the device farthest from the processor module. Note that the controller contains a bootstrap ROM.

   There are several backplane assemblies available from DEC and other manufacturers. Figure 2-2 shows typical backplane configurations. Note that the processor module is always installed in the first location of the backplane or in the first location in the first backplane of multiple backplane systems.

   It is important that all option slots between the processor and the disc controller be filled to ensure that the daisy-chained interrupt (BIAK) and DMA (BDMG) signal be complete to the controller slots. If there must be empty slots between the controller and any option board, the following backplane jumpers must be installed:

FROM	TO	SIGNAL
C0 X NS	C0 X M2	BIAK1/L0
C0 X S2	C0 X R2	BDMG1/L0
↑ Last Full Option Slot	↑ Controller Slot	



SWITCHES

S1 (LSB) **S2** **S3** (MSB) **S4** **S5**

BINARY NUMBER OF THE FIRST LOGICAL UNIT OF THE SECOND PHYSICAL DRIVE.*

ON RP03
OFF RP02

ON BOOTSTRAP ENABLE
OFF BOOTSTRAP DISABLE

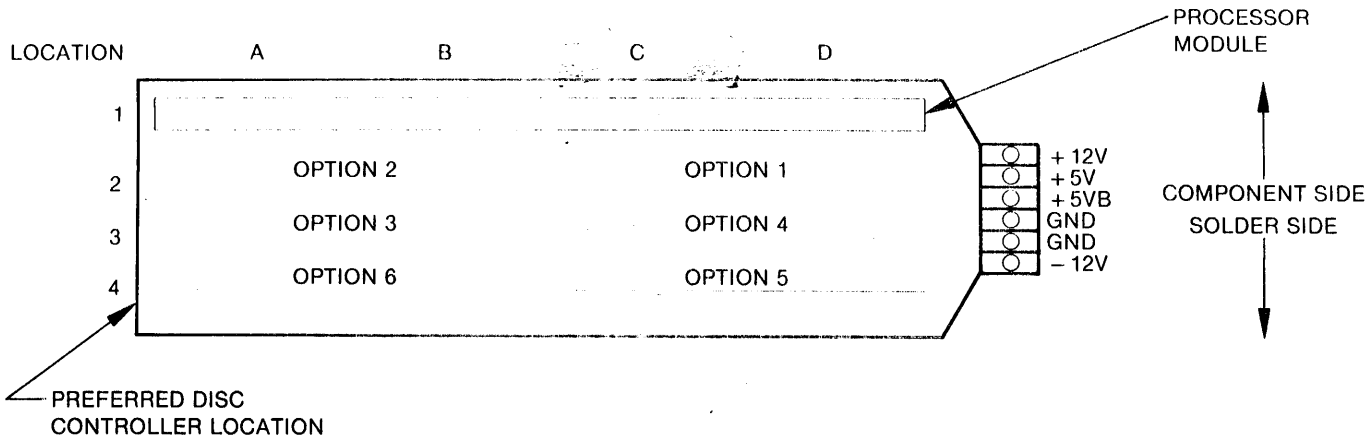
*FOR EXAMPLE, IF THERE ARE FOUR LOGICAL UNITS (NUMBERED 0-3) IN THE FIRST DRIVE, SET THE SWITCHES FOR THE FIFTH LOGICAL UNIT (NUMBER 4) AS FOLLOWS:

(LSB) S1	S2	(MSB) S3
0	0	1

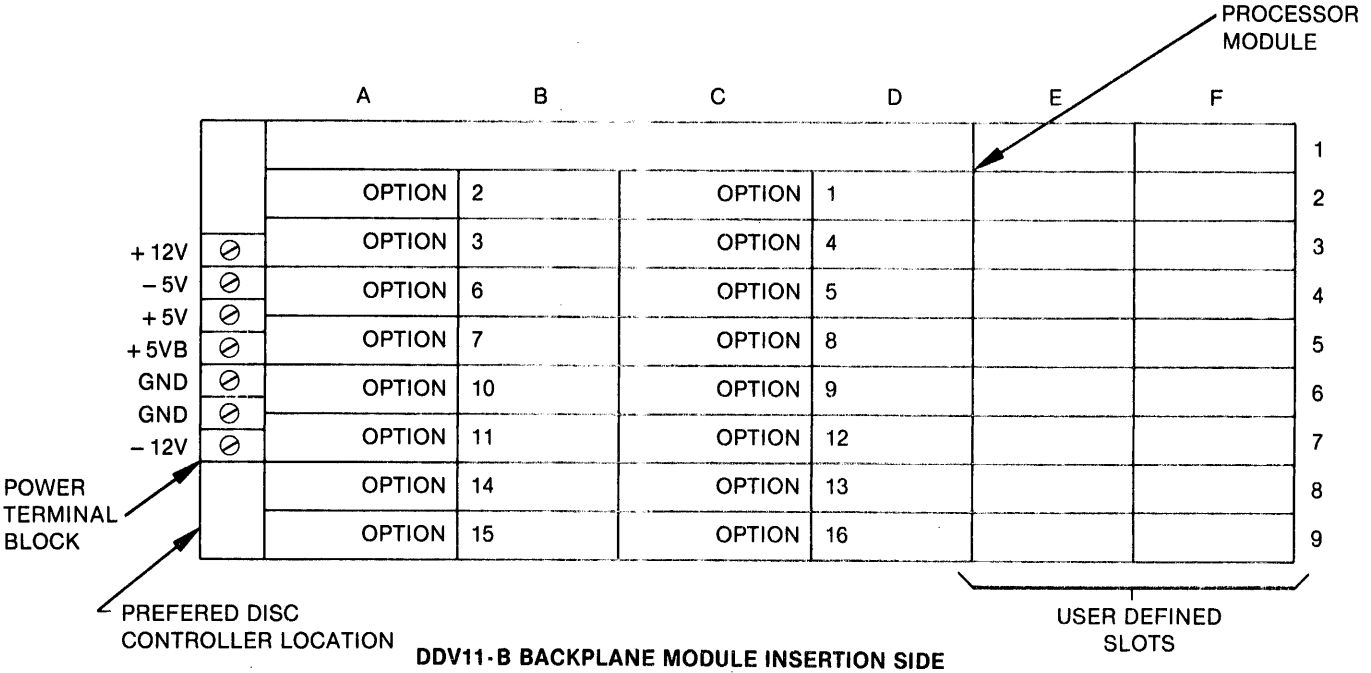
NOTE

*IF S1, S2, AND S3 ARE OFF (000), THE CONTROLLER WILL DEFAULT TO ALL LOGICAL UNITS ON THE **FIRST** PHYSICAL DRIVE (DRIVE 0). BECAUSE OF THE CHARACTERISTICS OF SOME OPERATING SYSTEMS, THE SWITCHES SHOULD BE SET FOR TWO DRIVES EVEN IF ONLY ONE DRIVE IS PRESENT.*

Figure 2-1. Controller Configuration



H9270 MODULE INSERTION SIDE



DDV11-B BACKPLANE MODULE INSERTION SIDE

NOTE

MEMORY CAN BE INSTALLED IN ANY SLOT; IT IS NOT PRIORITY DEPENDENT AND DOES NOT NEED TO BE ADJACENT TO THE PROCESSOR.
CONTROLLERS ARE ALSO COMPATIBLE WITH H9273A MODULES.

Figure 2-2. Typical Backplane Configuration

2. Insert the controller into the selected backplane position. Be sure the controller is installed with the components facing row one, the processor.

   The controller module is equipped with handles on the side opposite the slot connectors. Gently position the module slot connectors into the backplane then press until the module connectors are firmly seated into the backplane. Both handles must be pressed simultaneously. When removing the module, apply equal pulling pressure to both handles.

3. Feed the module connector end of the disc I/O cables into the controller module connectors. Install the cable connectors into the module connectors. Verify that the connectors are firmly seated.

4. Connect the disc-end of the I/O cables to the disc I/O connectors. Be sure that the bus terminator is installed at the last disc in the system.

5. Refer to the disc manual for operating instructions and apply power to the disc and computer.

6. Observe that the green DIAGnostic LED on the controller board is lit.

7. The system is now ready to operate. Refer to Section 3 for operating instructions, diagnostics, and formatting.

SECTION 3
OPERATION

INTRODUCTION

This section contains procedures for operating the computer system with the controller and a disc drive or drives. An understanding of DEC operating procedures is assumed. The material here is provided for "first time users" of disc subsystems and describes procedures for bootstrapping, formatting, and diagnostic testing.

PRECAUTIONS AND PREOPERATION CHECKS

The following precautions should be observed while operating the system. Failure to observe these precautions could damage the controller, the disc cartridge, the computer, or could erase a portion or all of the stored software.

1. If the controller bootstrap is to be used, set controller switch S4 on, and disable other bootstraps that reside at that address.
2. See Figure 2-1 for proper positions of the switches.
3. Do not remove or replace the controller board with power applied to the computer.
4. If system does not operate properly, check operating procedures and verify that the items in Section 2 have been performed.

Before operation the following checks should be made:

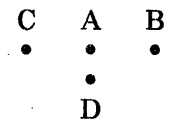
1. Verify that the controller board is firmly seated in backplane connector.
2. Verify that the cables between the controller and the disc drive are installed.
3. Be sure the disk drive cartridge is installed (if it is to be used).
4. Apply power to the computer and the console device.
5. Verify that green DIAG light on front edge of the controller board lights.
6. Be sure power is applied to disc drive and READY light is on.

BOOTSTRAP PROGRAM, SWITCHES AND JUMPERS

The DILOG Program will boot the system from RP02/03 or TM-11 mag tape. The controller bootstrap program is disabled when Switch 4 (Figure 2-1) is OFF. In addition to Switch 4, one of three jumper wires may be inserted to select the controller bootstrap starting address. The jumper connections are located in the lower right corner of the board (component side) between components F20 and F21. The jumper and address configurations for selecting the bootstrap program are as follows:

Jumper	Address
A to B (Standard Address)	DILOG = 173000
A to C (Alternate Address)	DILOG = 172000
A to D (hardware disabled)	

The etch or jumpers are factory installed for the user's requirements, but may be changed. On the solder side of the board, the configuration resembles the following:



To change the configuration, cut the existing etch and rewire as described above.

Note

If a system has more than one device with bootstrap capabilities enabled, the bootstraps must be at different addresses.

BOOTSTRAP PROCEDURE

The following assumes the system is in ODT mode. Note that the bootstrap can be used under processor Power Up Mode 2 conditions. Refer to the appropriate DEC manual for a discussion of the Power Up Modes. Further note that the disc drive does not need to be READY to enter the bootstrap.

Reset the system by pressing RESET or enter the following (characters underlined are output by the system; characters not underlined are input by the operator):

@ 173000G or 172000G
Depends on switch and jumper configuration above.

* DP0 or MT0 <CR>
DP if disc, MT if tape. Booting can be executed from logical units other than "0" shown in the example by entering the desired logical unit number, i.e., 1, 2, 3... or 7.

FORMAT AND DIAGNOSTIC TEST PROGRAM

Description

DILOG's Universal Firmware and Diagnostic Program permits the user to format a disc pack for his particular application; compensate for media errors; and test the controller and drive. When formatted, the disc may be partitioned horizontally or vertically. Either way the pack is divided into logical units which the computer recognizes. The user may select one of three types of partitioning: 1-head, 2-head or vertical.

The constraints for selecting each are:

1-head:
- Maximum number of heads (surfaces) is 8.
- Maximum number of logical units is 8.
- Maximum size of logical units is 102,400 records.

2 head:
- Maximum number of heads (surfaces) is 16.
- Number of fixed and removable heads (surfaces) must be even.
- Maximum number of logical units is 8.
- Maximum size of logical units is 102,400 records.

Vertical:
- Maximum number of logical units is 8.
- Maximum size of logical units is 102,400 records.

Drive types CMD or DFR are formatted for a 1-head partition. SMD or MMD types are usually formatted vertically.

The disc pack is divided vertically by cylinders and horizontally by heads (or data surfaces). Each head (surface) is further divided into tracks. A track is addressed by cylinder number and head number. Tracks are further divided into sectors (or records or blocks) which the computer recognizes as increments within a logical unit. Sectors consist of overhead bytes (such as address, sync, error correction) and data bytes. The standard number of data bytes, bytes usable by the computer, is 512 data bytes per sector. Figure 3-1 illustrates vertical and head partitioning.

Table 3-1 is a partial list of disc drives and specifications for partitioning. Column 1 lists the manufacturers and model numbers. Column 2 lists the unformatted capacity of each drive (removable plus fixed surfaces). Column 3 lists the sectors (also called records and blocks) per track. Column 4 lists the number of heads (surfaces) per drive. Some drives have two heads per surface which, for the purposes of this text, doubles the capacity. Column 5 lists the cylinders per drive. Column 6 lists the sectors (records, blocks) accessible to the computer for each drive.

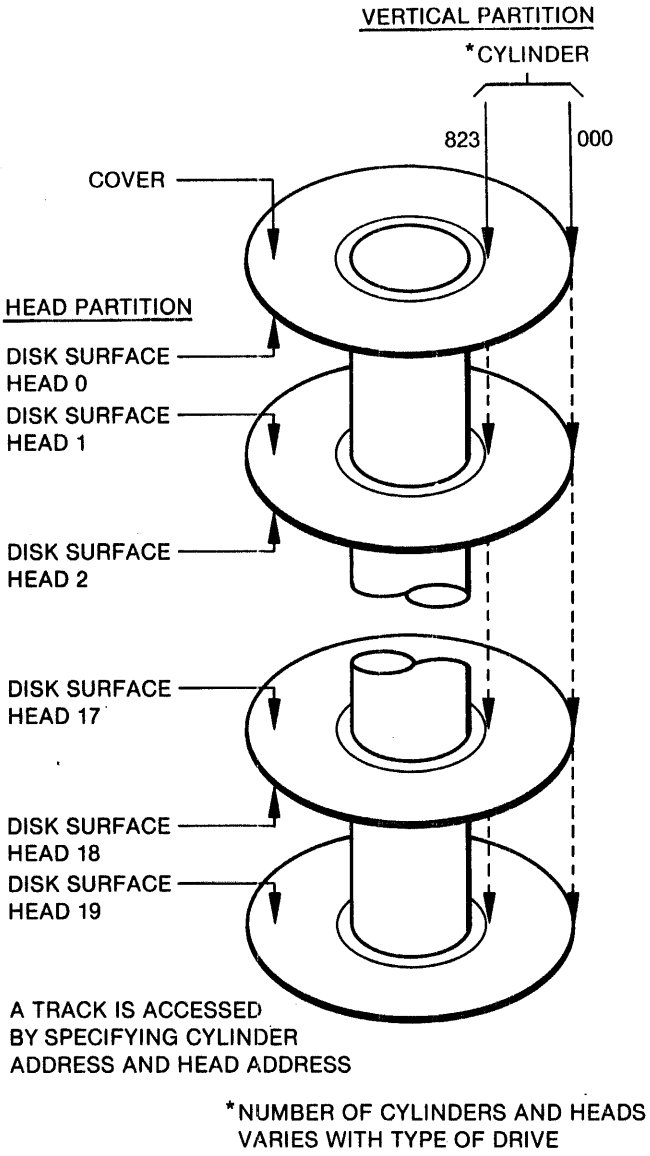


Figure 3-1. Partitions

Parameters for disc drives not listed in Table 3-1 may be determined from manufacturer's specifications and the following: Determine the number of bytes per track from the manufacturer's specification. The number of bytes per sector (data and overhead) for DILOG controllers is 568. Divide the number of bytes per track by the number of bytes per sector. Drop the remainder. This value is the number of sectors per track. Then, number of sectors per track × number of heads × number of cylinders per drive = number of sectors per drive.

Table 3-1. Values For Partitioning With Universal Firmware

(1) Manufacturer	Model Number	(2) Unformatted Capacity Megabyte		(3) Sectors (Records) (Blocks)/ Track	(4) Heads (Data Surfaces)/ Drive		(5) Cylinders/ Drive**	(6) Accessible Sectors (Records) (Blocks)/ Drive
		Removable	Fixed		Removable	Fixed		
DIGITAL EQUIPMENT CORPORATION	RP02*	31.2	0	10	20	0	200	40,000
AMPEX	DFR-932	16.5	16.5	35	1	1	823	57,610
AMPEX	DFR-964	16.5	49.5	35	1	3	823	115,220
AMPEX	DFR-996	16.5	82.5	35	1	5	823	172,830
AMPEX	DM980	82.9	0	35	5	0	823	144,025
BALL	DB50	54.7	0	24	5	0	815	97,800
BALL	BD80	82.1	0	35	5	0	815	142,625
BASF	6172	0	24	23	0	3	600	41,400
CENTURY DATA SYS.	Trident T-82RM	82.9	0	35	5	0	823	114,025
CONTROL DATA CORP.	CMD 9448-32	16.5	16.5	35	1	1	823	57,610
CONTROL DATA CORP.	CMD 9448-64	16.5	49.5	35	1	3	823	115,220
CONTROL DATA CORP.	CMD 9448-96	16.5	82.5	35	1	5	823	172,830
CONTROL DATA CORP.	MMD 9730-24	0	25.8	35	0	2(2) = 4	320	44,800
CONTROL DATA CORP.	MMD 9730-80	0	82.9	35	0	5	823	144,025
CONTROL DATA CORP.	MMD 9730-160	0	165.9	35	0	2(5) = 10	823	288,050
CONTROL DATA CORP.	SMD 9766	82.9	0	35	5	0	823	144,025
CONTROL DATA CORP.	SMD 9764	157.4	0	35	19	0	411	273,315
CONTROL DATA CORP.	SMD 9766	315.2	0	35	19	0	823	547,295
FUJITSU	M-2284	0	166.9	35	0	2(5) = 10	815	285,250
KENNEDY	5303	0	43.2	35	0	3	700	73,500
KENNEDY	5305	0	70.5	35	0	5	700	122,500
NEC	D1240	0	83.1	35	0	2(4) = 8	530	148,400
PRIAM	DISKOS 3350	0	33.2	35	0	3	561	58,905

* Will not interface — used as reference only.
** For a 1-head partition, the value of cylinders/drive = tracks/head.

The user may require alternate cylinders, or spares, to compensate for media flaws, soft errors, or marginal drive conditions. All three types of partitioning in the program make provisions for sparing. The program accounts for alternates when calculating the number and size of logical units.

If the number of logical units is to be changed, the configuration switches, shown in Figure 2-1, should also be changed after completion of format and test.

The descriptions below indicate what parameters will be changed as various elements are changed; for example, if the number of logical units is changed, the size of logical units will change.

1-Head Partition

Parameters for 1-head partitioning are determined as follows:

1. Determine the number of alternate tracks required for each logical unit. Subtract the number of alternates from the number of tracks per head. The number of tracks per head is the same number as cylinders/drive, Table 3-1, column 5. This value is the *usable* tracks per head. Then,

2. Sectors per track × (tracks per head minus alternates) = Number of sectors per logical unit.
3. Sectors per logical unit × 512 = Megabyte capacity per logical unit.
4. Number of heads = Number of logical units

For example, an AMPEX DFR-932 has 35 sectors/track (Column 3 in the table) and 823 tracks/head (Column 5). With no spares there are 57,610 sectors/drive (Column 6). Since there are two heads, one removable and one fixed, there are two logical units of 28,805 sectors/logical unit. It may be determined that four alternates (spares) are required. The equation then becomes:

$$35 \times (823-4) = 28{,}665$$

The program then displays the new parameters.

2-Head Partition

The parameters for 2-head partitioning are the same as for 1-head except the number of sectors/logical unit is multiplied by two:

1. Determine the number of alternate tracks required for each logical unit. Subtract the number of alternates from the number of tracks per head. The number of tracks per head is in Table 3-1, Column 5. Then,
2. Sectors per track × (tracks per head minus alternates) × 2 = Number of sectors per logical unit.
3. Sectors per logical unit × 512 = Megabyte capacity per logical unit.
4. Number of heads per drive divided by 2 = Number of logical units per drive.

The previous example, AMPEX Model DFR-932, cannot be used since the number of removable/fixed heads is not even. Consider CDC Model 9730 with 3 alternates selected:

$$35 \times (320-3) \times 2 = 22{,}190$$

In this instance, there are 4 heads with 2 heads/surface. There are two logical units in this example.

Vertical Partition

With vertical partitioning, the user may select the number of logical units or the size of the logical unit. If the number of logical units is selected, the logical units will be of equal size. If the size of logical units is selected, all logical units may not be of equal size. For example there may be 3 equal logical units of 40,000 sectors/logical unit and a partial logical unit of 27,000 sectors/logical unit.

Parameters for vertical partitioning are determined as follows:

User specifies the number of logical units (all logical units are of equal size):

1. Determine the required number of alternate cylinders per drive. Subtract the number of alternates from the number of cylinders per drive (Column 5). This value is the usable cylinders per drive.
2. Determine the number of logical units per drive required. Then,
3. Number of usable cylinders per drive divided by number of logical units required = Number of cylinders per logical unit. The remainder is assigned as alternate.
4. Number of cylinders per logical unit × sectors per track × number of heads = Number of sectors per logical unit.
5. Number of sectors per logical unit × 512 = Megabyte capacity per logical unit.

For example, if the user has a Century Data drive, Model T-82, and 2 alternates and 3 logical units are required, then,

$$823 - 2 = 821 \text{ usable cylinders}$$

and

$$\frac{821}{3} = 273.6 \text{ cylinders per logical unit}$$

The remainder (.6) is assigned as alternate. (The number of alternates will be more than initially selected in this instance.)

Then,

$$273 \times 35 \times 5 = 47{,}775 \text{ sector per logical unit}$$

And,

$$47{,}775 \times 512 = 24.46 \text{ megabytes per logical unit.}$$

User specifies the size of logical units in sectors per logical unit (the last logical unit will be a different size).

1. Determine the required number of alternate cylinders per drive. Subtract the number of alternates from the number of cylinders per drive (Column 5). This value is the usable cylinders per drive.
2. Determine the required number of sectors (blocks) per logical unit. Then,
3. Sectors per track (Column 3) × number of heads (Column 4) divided into sectors per logical unit = cylinders per logical unit. If there is a remainder, the number of cylinders per logical unit is rounded off to the next higher number.

4. Number of usable cylinders divided by cylinders per logical unit = number of logical units. If there is a remainder, the number of logical units is rounded off to the next higher number.
5. Number of cylinders per logical unit × number of full (equal size) logical units = Number of cylinders full (equal size) logical units.
6. Number of usable cylinders per drive minus number of cylinders in full logical units = Number of cylinders in partial logical unit.

For example, if the user has a Century Data T82 and 4 alternates and 40,000 sectors per logical unit are required, then,

$$823 - 4 = 819 \text{ usable cylinders}$$

and

$$\frac{40{,}000}{35 \times 5} = 228.57 \text{ cylinders per logical units}$$

which becomes

229 cylinders per logical unit

then

$$\frac{819}{229} = 3.576 \text{ logical units per drive}$$

or four logical units, three equal and one partial.

For the partial logical units:

$$229 \times 3 = 687$$

$$819 - 687 = 132 \text{ cylinders per partial logical unit.}$$

The logical units are numbered as follows:

Logical unit number	Cylinder numbers
0	0-228
1	229-457
2	458-687
3	688-818

The partial logical unit is calculated as follows:

$$132 \times 35 \times 5 = 23100 \text{ sectors per logical unit}$$

In this example, the configuration switches should be set for logical unit number 4 even if only one drive is present. Some operating systems will be seeking eight logical units, and setting the switches informs the operating system that there are only four in the first drive.

Partitioning Program

When the program is initialized the following display will appear on the terminal:

DILOG'S UNIVERSAL FIRMWARE AND DIAGNOSTIC PROGRAM VERIFIES PROPER FUNCTIONING OF THE DILOG DQ202A DISC CONTROLLER AND FORMATS THE DISC TO YOUR SPECIFICATIONS.

YOUR DEFAULT PARAMETERS ARE:

SECTORS __ __
HEADS __ __
CYLINDERS __ __ __ __
ALTERNATES __ __
SIZE OF LOGICAL UNIT (RECORDS)
__ __ __ __ __ __ __

The parameters displayed are calculated for the efficiency of most applications. The units of measure are as follows: sectors/track; heads/drive; cylinders/drive; alternates/drive; and the size of logical unit in sectors/logical unit.

The next display will be:

ARE YOU RUNNING THE DIAGNOSTIC VIA A CRT (Y or N).

If the answer is no, the CRT will not display the current cylinder address during the test program.

The next displays to appear are as follows:

ARE YOU FORMATTING A CMD DRIVE?
IS YOUR DRIVE A 32 MEGABYTE DRIVE?
IS YOUR DRIVE A 64 MEGABYTE DRIVE?
IS YOUR DRIVE A 96 MEGABYTE DRIVE?
CHANGE NUMBER OF ALTERNATES?
HOW MANY?

If the type of drive is a CMD or a DFR to be formatted (AMPEX and CDC drives in Table 3-1), enter Yes (Y) to the first question. If No (N or carriage return), the program will display the next sequence described below. To the next three questions, "IS YOUR DRIVE . . . ", enter (Y) or (N) for the drive capacity. To the question "CHANGE NUMBER OF ALTERNATES?", a No response will default to the alternates in the default parameters. A Yes response and a response to HOW MANY will change the number of alternates to the number requested.

The next display to appear is as follows:

SELECT ONE OF THE FOLLOWING TYPES OF PARTITIONING:

(1) 1-HEAD PARTITION
(2) 2-HEAD PARTITION
(3) VERTICAL PARTITION

PLEASE ENTER THE CORRESPONDING NUMBER _____.

For a 1-head or 2-head partition, responses to the following display are required:

CHANGE NUMBER OF SECTORS?
CHANGE NUMBER OF HEAD?

If yes is entered, "HOW MANY" will be displayed. If the numbers entered are not within the constraints, the following error messages will occur:

MAXIMUM NUMBER OF HEADS WITH (1 or 2)
HEAD PARTITION IS (8 or 16)

NUMBER OF HEADS MUST BE AN EVEN NUMBER WITH 2-HEAD PARTITION.

The maximum number of heads for a 1-head partition is 8; for a 2-head partition 16.

The next series of questions displayed is:

CHANGE NUMBER OF CYLINDERS?
CHANGE NUMBER OF ALTERNATES?
CHANGE SIZE OF LOGICAL UNITS?
CHANGE NUMBER OF LOGICAL UNITS?

If any of the responses are Yes, "HOW MANY," appears. If No to all inquiries, the program responds with the default parameters. The user may change either the size or number of logical units but not both. Units for the above are cylinders/drive, alternate cylinders/drive, sectors/logical unit, and number of logical units/drive.

The program will then calculate and display the following:

NEW FORMAT PARAMETERS ARE:
SECTORS =
HEADS =
CYLINDERS =
ALTERNATES =
SIZE OF LOGICAL UNIT =
NUMBER OF LOGICAL UNITS =

In a vertical partition, the number of alternates to appear may be more than selected; the program calculates the remainder of equal size logical units and adds these to the alternates requested. For example, if 4 alternates are requested and 7 alternates remain after calculation, the total to appear on the display will be 11. The program will then display:

DURING CALCULATION OF EQUAL SIZE LOGICAL UNITS, _____ EXTRA ALTERNATE CYLINDERS HAVE BEEN OBTAINED.

The following error messages may occur if the constraints are violated:

MAXIMUM SIZE OF LOGICAL UNIT IS 102,400 RECORDS.

or

THIS COMPUTES TO _____ LOGICAL UNITS. LIMIT IS 8 LOGICAL UNITS.

After errors are corrected, the following display will appear:

THE DRIVE WILL BE FORMATTED AS _____ LOGICAL UNITS.

DP0-__ WILL BE FORMATTED TO A _____ MBYTE UNIT.

EACH LOGICAL UNIT WILL BE _____ RECORDS.

DP___ WILL BE A _____ MBYTE UNIT (_____ RECORDS).

WITH _____ CYLINDERS USED FOR ALTERNATE CYLINDERS.

The total number of logical units will include equally divided units and partial units. "DPO" and equal units will have the same number of megabytes and records (sectors/logical unit). DP___ will be the last unit and will have a different number of megabytes and records; this message will not appear if all the units are of equal size.

Format and Diagnostic Test Program

The format/test program contains the following:

1. TEST CONTROLLER
   A. Registers
   B. Data Buffer
2. TEST DISC DRIVE
   A. Disc Ready
   B. Disc Restore (seek to cylinder 0)
3. FORMAT
   A. Write Headers
   B. Read Headers
   C. Write Data Test Pattern
   D. Read Data Test Pattern
4. SEQUENTIAL READ
5. SELECTED READ
6. RANDOM SEEK, READ
7. RANDOM SEEK, WRITE, READ, AND COMPARE

Test Controller

The program will automatically test the controller registers and data buffer. The program will only display error messages during this test; the display will be:

DATA BUFFER ERROR

or the mnemonics of the seven controller registers, the location and contents (in Octal). The display of the registers is followed by a 4-line message to aid in isolating the specific problem.

Note

Whenever an error occurs and the registers are displayed, an audio alarm signal is generated to notify the operator.

The 4-line message is as follows:

DISC ADDRESS
SECTOR _____ HEAD _____ CYLINDER _____
TYPE OF COMMAND _____
CONTROL STATUS ERROR _____
DRIVE STATUS _____

"DISC" lists the sector, head and cylinder (in decimal) where the error occurred. An example of Type of Command is Read Data Command. An example of Control Status is Seek Error. The Drive Status will display:

DRIVE OK
USE C TO CONTINUE
USE O TO TRANSFER TO ODT
USE L TO REBOOT YOUR SYSTEM

"C" is used to continue the test. "O" is used for ODT (on-line debugging technique). "L" is used to initiate the system bootstrap. If ODT is specified, the program will display:

YOUR RETURN ADDRESS IS
_ _ _ _ _ _ _ _

This enables the operator to return to the point where the error occurred. The return address should be written down as it will be used later for re-entry.

Test Disc Drive

After the controller test is performed, the program will automatically test the drive for ready and restore. The disc address is not displayed during this test. If the disc will not restore, the program will display the register for cylinder 0.

Format

The operator may either select logical units sequentially or select one or more specific logical units to be formatted. Program messages are presented for formatting in logical unit number sequence, i.e.:

FORMAT DP0 (Y OR N)?
FORMAT DP1 (Y OR N)?
FORMAT DP2 (Y OR N)?
•
•
•
FORMAT DP7 (Y OR N)?

At this time, if there is an error in the number of sectors, the following messages will appear:

YOU SPECIFIED _ _ _ SECTORS PER TRACK

YOUR DRIVE IS SET FOR _ _ _ SECTORS PER TRACK PLEASE CORRECT THIS DISCREPANCY AND THEN PRESS R TO RESTART THE DIAGNOSTIC.

The program will then return to the beginning.

Note

Before any write operation, the program will display ARE YOU SURE? This aids the operator in preventing reformatting of a previously formatted logical unit (possibly destroying good data).

During formatting, the following messages will appear sequentially:

WRITING HEADERS
CURRENT CYLINDER ADDRESS _ _ _ _
READING HEADERS
CURRENT CYLINDER ADDRESS _ _ _ _
WRITING DATA TEST PATTERN _ _ _ _
CURRENT CYLINDER ADDRESS _ _ _ _
READING DATA TEST PATTERN _ _ _ _
CURRENT CYLINDER ADDRESS _ _ _ _

When reading and writing headers, the program will display the cylinder addresses sequentially. The test pattern tests are also sequentially selected, and the cylinder address displayed will correspond to current address being read.

After each logical unit is formatted, the display will be:

DP___ FORMAT AND VERIFICATION COMPLETE

Sequential Read

For this test, the display will be:

SEQUENTIAL READ (ALL CYLINDERS AND HEADS?)

If the response is No, the program will jump to the Selected Read test. If the response is Yes, the current cylinder address is displayed as each cylinder is read. If an error is detected, the register contents and location are displayed with the 4-line identification message, and the following:

ASSIGN ALTERNATE TRACK FOR DEFECTIVE TRACK?

If no alternates (spares) are available, the following will be displayed:

NO ALTERNATE CYLINDER AVAILABLE

When marking or assigning alternate tracks, the following error messages may occur:

TRACK HAS ALREADY BEEN MARKED DEFECTIVE
TRACK HAS ALREADY BEEN MARKED ALTERNATE

Selected Read

For this test, the display will be:

READ DP0? (Y or N)?

If the response is No, the next logical unit will be displayed. If the response is Yes, the current cylinder address is displayed and each cylinder is read. If an error is detected, the register contents and location are displayed with the 4-line identification message. The ASSIGN ALTERNATE TRACK message appears, and error messages if the track has been marked DEFECTIVE or ALTERNATE.

Random Seek, Read

For this test, the display will be:

RANDOM SEEK, READ OF DRIVE (ALL CYLINDERS AND HEADS)?

This test selects a random cylinder, logical unit, and a sector address within the cylinder. The test then reads data and tests for errors. All logical units are used in this test. Alternate cylinders cannot be assigned during this test. The terminal keyboard space (SP) character is used to exit this test.

If an error is detected, the register content and locations are displayed with the 4-line identificiation message.

Random Seek, Write Data, Read Data, Compare Test

If the response is No, each logical unit will appear in sequence until the response is Yes:

DP0?
DP1?
•
•
•
DP7

This test selects a random cylinder address and random sector address and writes five sectors (2560 bytes) of random data. The data written is then read into CPU memory and compared for read errors. This test allows logical units to be tested. The terminal keyboard space character (SP) is used to exit from this test.

Assign Alternate Track

This test may be used if the disc drive manufacturer provides a map describing defective tracks. the message is:

ASSIGN ALTERNATE TRACK FOR DEFECTIVE TRACK (Y or N)?

If the response is No, the program will revert to:

USE R TO REPEAT
USE O TO TRANSFER TO ODT
USE L TO REBOOT YOUR SYSTEM

If the response is yes, the display will be:

CYLINDER ADDRESS (0 TO ____)?

Enter the cylinder address, in decimal, of the defective track. If the cylinder address entered is incorrect, the message will be repeated.

The next message will be:

HEAD ADDRESS (0 TO ____)

Enter the head address, in decimal, of the defective track. If the head address entered is incorrect, the message will be repeated.

The next message will be:

MAP OUT
CYLINDER ____ HEAD __
ARE YOU SURE? (Y or N)

If No, the program will repeat the first message of this test. If Yes, an alternate cylinder is assigned and the message is:

ALTERNATE CYLINDER ASSIGNED

Other message to appear may be:

TRACK ALREADY MARKED DEFECTIVE

or

TRACK ALREADY MARKED ALTERNATE

The program will then repeat the first message of this test.

SECTION 4
PROGRAMMING

PROGRAMMING DEFINITIONS

Function — The expected activity of the disc system (write, seek, read, etc.).

Command — To initiate a function (halt, clear, go, etc.)

Instruction — One or more orders executed in a prescribed sequence that causes a function to be performed.

Address — The binary code placed in the BDAL0-15 lines by the bus master to select a register in a slave device. Note memory other than computer internal memory, i.e., peripheral device registers, the upper 4K (28-32K) address space is used.

Register — An associated group of memory elements that react to a single address and store information (status, control, data) for use by other assemblies of the total computer system. Classically, registers have been made up of groups of flip-flops. More and more often registers are the contents of addressed locations in solid-state or core memory.

DISC CONTROLLER FUNCTIONS

The disc controller performs 11 functions. A function is initiated by a GO command after the processor has issued a series of instructions that store function-control information into controller registers. To accept a command and perform a function, the controller must be properly addressed and the disc drive(s) must be powered up, be at operational speed, and be ready.

The 11 functions performed by the controller are established by bits 01, 02, 03 and 11 of the control status register (RPSC). The function and bit codings are given in Table 4-1. Descriptions of the functions are given in the following paragraphs.

The controller functions are specified by bits 01, 02, 03, and 11 of the Control Status (RPCS) register. The bit configurations and functions are specified in Table 4-1.

Table 4-1. Controller Functions

Bits				Functions
11	03	02	01	
0	0	0	0	Controller reset
0	0	0	1	Write data
1	0	0	1	Write headers
0	0	1	0	Read Data
1	0	1	0	Read headers
0	0	1	1	Write check
0	1	0	0	Seek
0	1	0	1	Write
1	1	0	1	Write headers only
0	1	1	0	Seek home (restore)
0	1	1	1	Read

Controller Reset

Clears controller logic to initial conditions and terminates data transfers at the end of the sector currently being transferrred. This function is entered when the controller is initially cleared or when the function register contents equal 0. If GO is set while the contents of the function register equals zero, CONTROL RESET is generated. The RESET command can be executed even if the controller is in the NOT READY state.

Write Data

The Write Data function includes a Seek to the desired starting disc address (cylinder and track). The function is executed by loading octal code (1) into the Function register and setting GO. Causes the controller to write one or more data records on the addressed disc. Writing starts at the drive, cylinder, head, and sector address specified by the RPCS, RPCA, and RPDA registers. The amount of data written is specified by the RPWC register. Write data transfer start from memory address specified by the RPBA register. Each data word transferred increments the Bus Address and Word Count registers. When the RPWC overflows, data transfers cease on the Bus and the remainder of the present sector is filled with zeros. As data is written a CRCC is calculated and written as the last word of each sector. Prior to writing, the Header record is read to verify proper head positioning. If the last word specified requests data be written past the last head, cylinder, and sector, the Overflow Error flag (bit 01 or RPER) will be set and the Function will terminate. If the AIE bit is set, this will in turn cause an interrupt.

Write Headers

If the Write Data and the Header bits are set, the Write Headers function is initiated when GO is set. This function causes the controller to write a five-

word header, which is used by the controller when either writing or reading data to determine:

a. Cylinder address
b. Head address
c. Sector address
d. Flags

Read Data

Causes the controller to read one or more data records from the disc drive. The Read function includes a Seek to the starting disc address (cylinder, head, sector) and is initiated by loading octal code 4 into the RPCS register and setting GO. Data transfers from the disc are stored in memory starting with the memory address specified by the RPBA register. Each data word transferred increments the Bus Address and Word Count registers. The contents of the RPWC at the beginning of the transfer specify the number of words to be transferred. When the RPWC overflows, data transfers stop. The remainder of the present sector is read and parity checked before the DONE flag is set.

Attempts to read beyond the last sector and head of the last cylinder of a disc will generate the OVERFLOW ERROR (bit 01 of RPER) flag and terminate the operation.

While data is being read, the controller calculates a CRC. At the end of the sector, the calculated CRC is compared with the CRC read from the sector. If they disagree, the CheckSum Error (CSME of RPER) bit sets.

Prior to reading the data record the header record is read to verify proper head position.

Read Headers

If the read data and the header bits are set, the Read Headers function is initiated when GO is set. This function causes the controller to read all headers starting at the Index mark. Each 5-word header is read in the order in which it appears on the disc. If a CRC error is detected in the header, the CSME bit of RPER is set.

Write Check

The Write Check function includes a Seek to the starting disc address (cylinder, head, sector). This function is a combination of the Write and Read functions. Data words are transferred from memory to the controller and simultaneously read from the disc drive and transferred to the controller. The two words read are compared in the controller. Discrepancies set the WCE bit in RPER to cause an appropriate interrupt. Data remains unchanged in both the memory and the disc.

If the data transfer is sufficiently large as to exceed the disc head, cylinder, and sector boundaries, the Overflow Error flag bit will be set and the function will terminate. If the AIE bit is set, this will in turn cause an interrupt.

Seek

The Seek function is responded to by the controller if octal code 10 is loaded in the RPCS register and GO is set; all the proper responses are made to the RP02/03 handler by the controller to indicate the proper completion of this function, seek complete interrupt, etc. . . . However, the controller does not actually issue a seek command to the disc drive. This function was originally implemented when each physical disc drive was one logical unit. Now that multiple logical units are in one physical drive, the function is no longer practical. Furthermore, all Read and Write functions include automatic seeks.

Write

This Write function is identical to the other Write Data function (octal code 2). An automatic seek is performed to the address specified in the RPCA and RPDA registers.

If the data transfer is sufficiently large to exceed the disc head, cylinder, and sector boundaries, the Overflow Error flag bit will be set then the function will terminate. If the AIE bit is set, this will in turn cause an interrupt.

Write Headers Only

Loading the RSCS register with the bit configuration for the Write Headers Only function and setting GO permits the headers to be re-written without disturbing the data records. This is a method of setting individual flag bits on a sector basis.

Seek Home

The Seek Home function is executed by loading its function into the Function register and setting GO. This function restores the head carriage assembly to cylinder 000_8 and the Unit Attention is set with Selected Unit Ready.

This function is used to recover from a Selected Unit Seek Incomplete.

Read

This function is identical to the other Read Data function (octal code 4). An automatic seek is performed to the address specified in the RPCA and RPDA registers.

If the data transfer is sufficiently large to exceed the disc head, cylinder, and sector boundaries, the Overflow Error flag bit will be set and the function will terminate. If the AIE bit is set, this will in turn cause an interrupt.

CONTROL REGISTERS

All software interaction between the disc controller, the processor, and the processor memory is accomplished by eight registers in the disc controller. These registers are assigned memory addresses and can be read or written into (except as noted) by instructions that reference respective register addresses. The eight controller registers, their addresses, their mnemonics, and their bit assignments are shown in Figure 4-1.

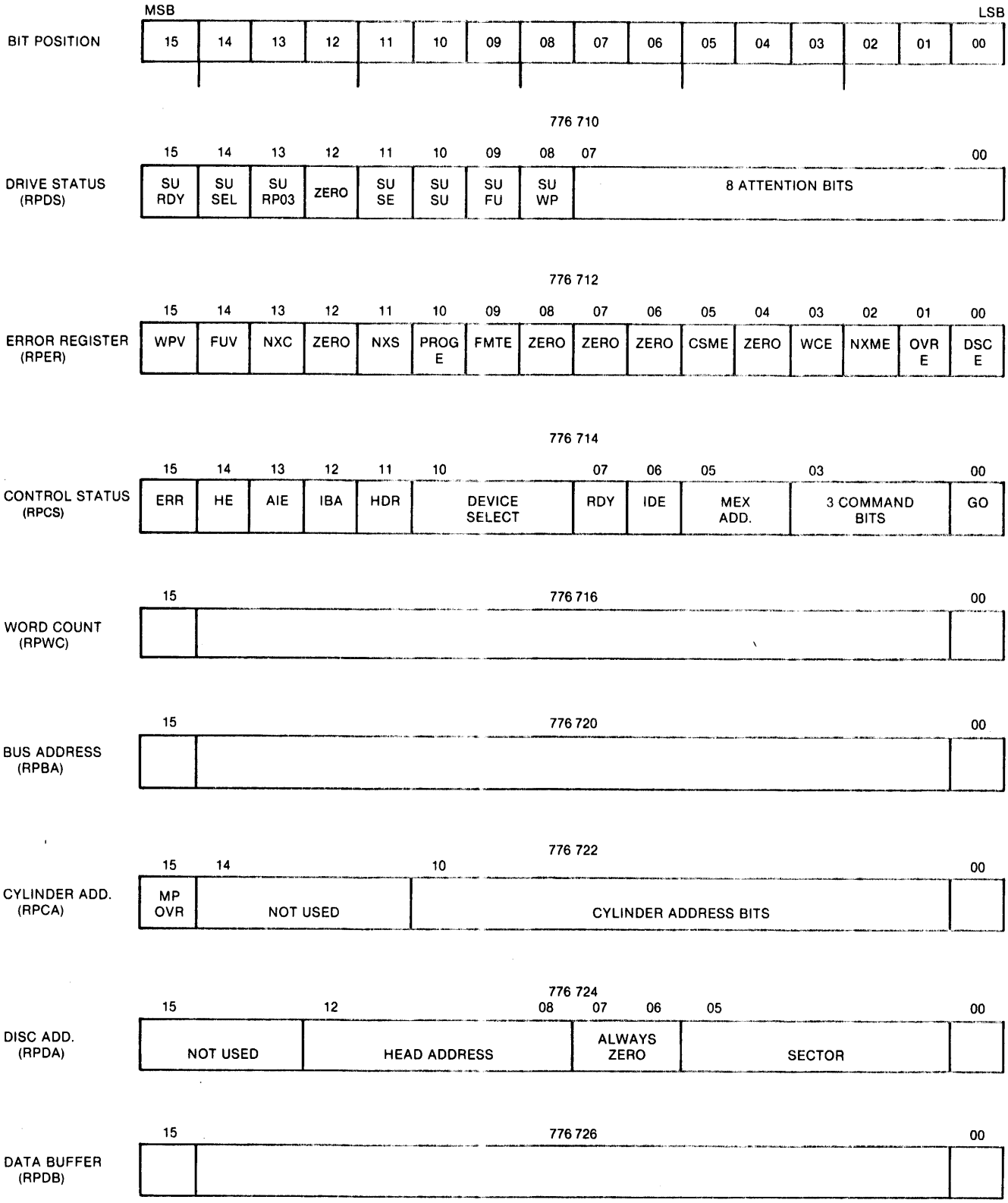
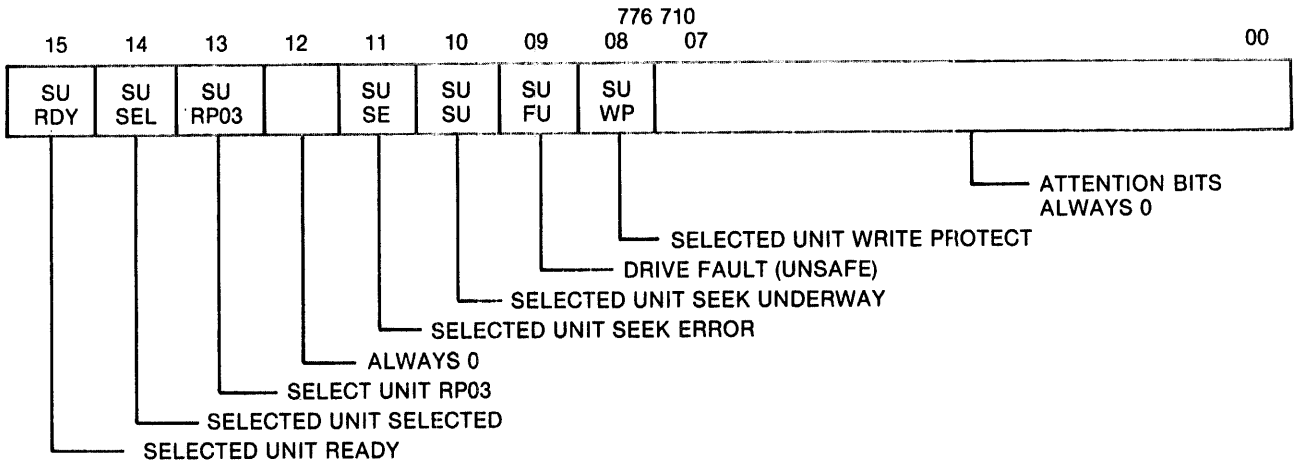


Figure 4-1. Controller Register Configurations

Drive Status Register (RPDS)

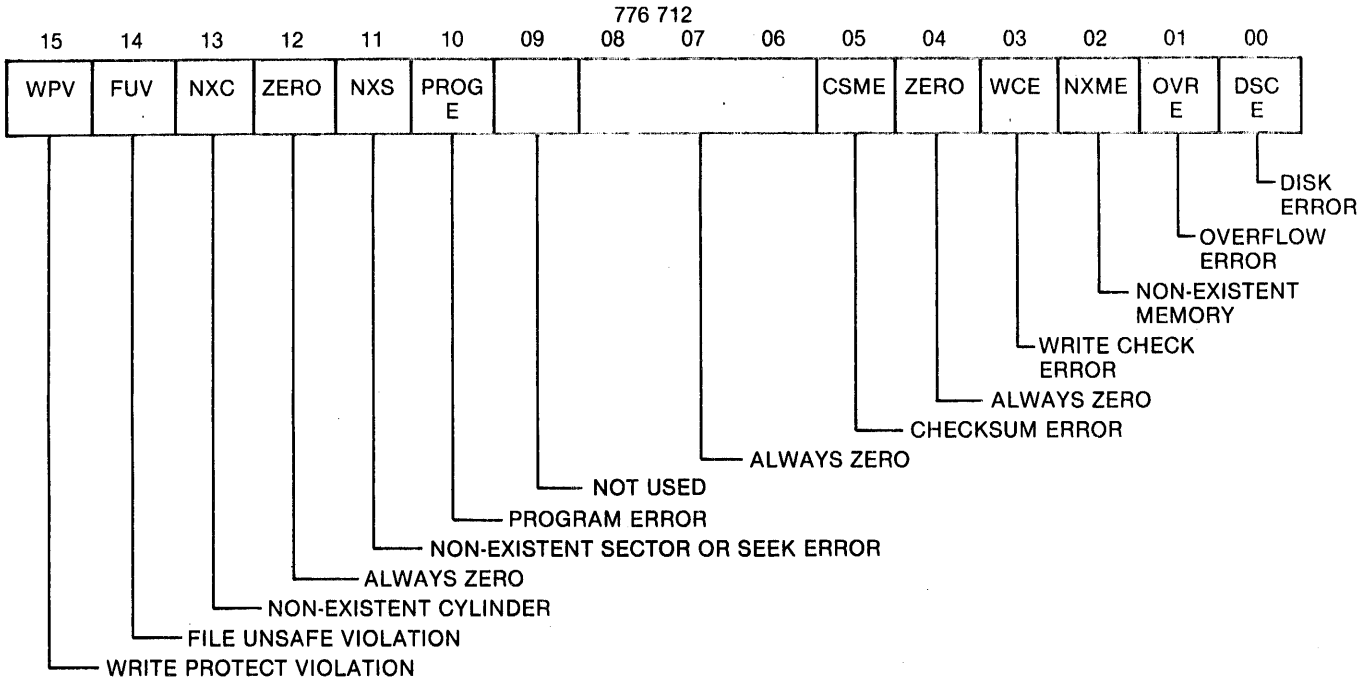


The address of RPDS is 776 710. RPDS is a read only register except that the eight attention bits can be selectively cleared by moving a 1 to the desired bit location(s). In most cases, the controller will be connected to only one disc drive, which will contain one or more logical units (emulating the RP02/03 physical units).

The significance of the bits of RPDS is as follows:

Bit(s)	Definitions
00-07	ATTENTION BITS — Always zero.
08	SELECTED UNIT WRITE PROTECTED — Sets when the selected disc is write protected.
09	DRIVE FAULT (UNSAFE) — Sets if an error condition is detected within the drive and is prohibiting all operations. This bit is reset manually by clearing the fault condition within the drive.
10	SELECTED UNIT SEEK UNDERWAY — Sets after a seek has been initiated and is reset after completion of the seek.
11	SELECTED UNIT SEEK ERROR — Sets if a seek is not completed within 100 milliseconds after it was initiated.
12	ALWAYS SET TO A ZERO.
13	SELECTED UNIT RP03. Reset when unit is RP02.
14	SELECTED UNIT SELECTED — Sets when the drive has been selected and is on line.
15	SELECTED UNIT READY — Sets after a successful seek operation. It is reset during any seek operation and set again after seek is completed.

Error Register (RPER)



The address of RPER is 776 712. This register contains all error conditions generated within the controller. RPER is a read only register. This register is cleared when the GO bit is set in RPCS.

The significance of the bits of RPER is as follows:

Bit(s)	Definitions
00	DISC ERROR — An attempt to use the drive with NOT READY, SEEK ERROR, or DRIVE FAULT conditions will set this bit. Reset by INIT or RESET functions.
01	OVERFLOW ERROR — Sets if a data transfer (read or write) is attempted across the end of the last sector of the logical unit. Reset by INIT or RESET functions.
02	NON-EXISTENT MEMORY — More than 10 microseconds were required to complete a Q-Bus transaction. Reset by INIT or RESET functions.
03	WRITE CHECK ERROR — Data read from the drive does not compare with the data read from memory during the Write Check function. Reset by INIT or RESET functions.
04	ALWAYS ZERO.
05	CHECKSUM ERROR — Calculated checksum does not compare with that read from the drive. Reset by INIT or RESET functions.
06, 07, 08	ALWAYS ZERO.
09	NOT USED
10	PROGRAM ERROR — Data transfer operation was attempted with an off-line drive, or while another instruction was still in progress. Reset by INIT or RESET functions.
11	NON-EXISTENT SECTOR — Operation was attempted when the contents of the Sector Address register was not within the proper range or the requested sector was not found. Reset by INIT or RESET functions.

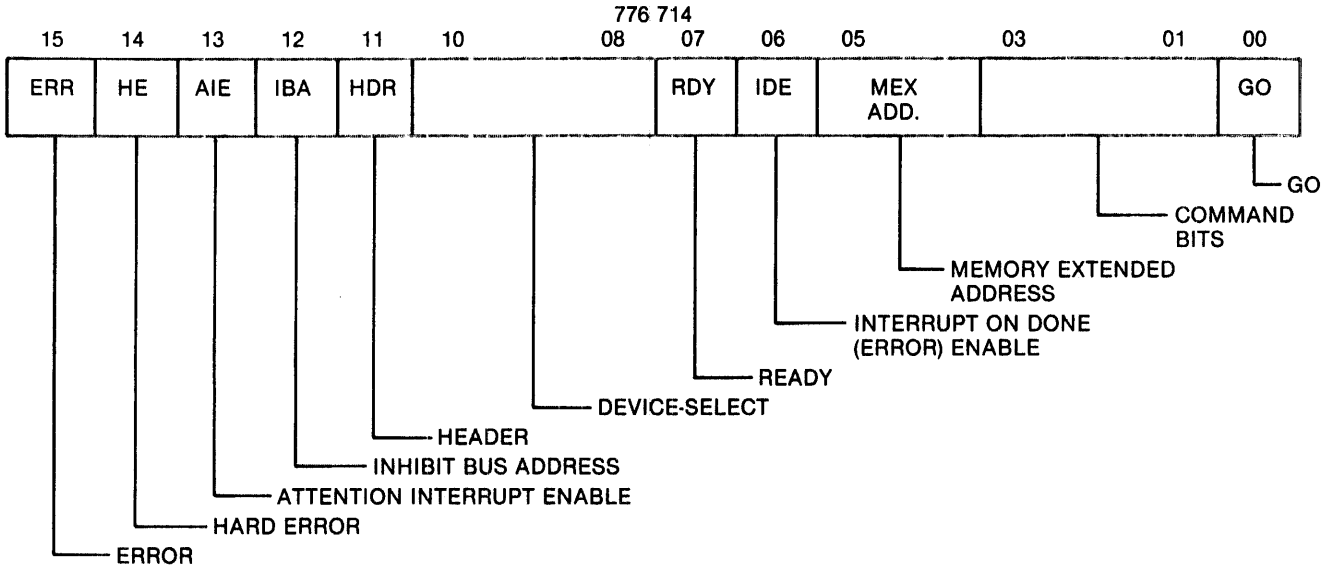
12 ALWAYS ZERO.

13 NON-EXISTENT CYLINDER OR SEEK ERROR — Operation was attempted when the contents of the Cylinder Address register was not within the proper range or controller unable to verify head position. Reset by INIT or RESET functions.

14 FILE UNSAFE VIOLATION — Operation was attempted while the SUFU (bit 09 of RPDS) was set. Reset by INIT or RESET functions.

15 WRITE PROTECT VIOLATION — Operation was attempted when the SUWP (bit 08 of RPDS) was set. Reset by INIT or RESET functions.

Control Status Register (RPCS)



The address of RPCS is 776 714. The bit configuration loaded into this register initiates and controls a disc function. All bits of this register are read/write unless otherwise indicated.

The significance of the bits of RPCS is as follows:

Bit(s)	Definitions
00	GO — When set causes the controller to initiate the operation encoded in bits 01-03 of RPCS. This is a write only bit always read as a zero.
01-03	COMMAND BITS — These bits are also referred to as function bits and specify the operation to be performed. These bits are described in Table 4-1. These are read/write bits, cleared by INIT or RESET functions.
04-05	MEMORY EXTENDED ADDRESS — Extended bus address bits for systems with memory larger than 32K 16-bit words. Used in conjunction with the RPBA register. These bits increment each time RPBA overflows. These are read/write bits cleared by INIT or RESET functions.
06	INTERRUPT ON DONE (ERROR) ENABLE — Causes the controller to raise an interrupt request when either a disc operation is complete or if an error occurs. This read/write bit is cleared by INIT or RESET functions.
07	READY — Indicates the controller is in a condition to accept and execute a new operation. This is a read only bit.
08-10	DEVICE SELECT — Specifies one of eight logical units which are to be the subject of any controller action. These read/write bits are cleared by INIT or RESET functions.

11 HEADER — Used in conjunction with the function bits specifying read or write operations. It is primarily used to format a new disc or reformat a disc erased due to a controller or drive failure. This read/write bit is cleared by INIT or RESET functions. The write format function causes a header record to be written in each sector. The header record contains five words obtained from a table in computer memory. These words are read from the disc by the controller to determine sector number (address verification).

A write header function starts at the Index and continues to write to the next Index. The headers are recorded in the order in which they are stored in the write table in memory. The controller properly spaces the sectors around the tracks of the disc.

The read header function reads all header records on one disc starting at the Index. The headers are read and stored in memory in the order in which they appear on the disc. If a CRC error is detected in the header record, the FMTE bit in RPER is set.

The Write Header Only function does not erase the data fields but writes header fields only. Thus, this function is used to set the write protect bit and to mark a sector bad.

12 INHIBIT BUS ADDRESS — Inhibits RBPA register from incrementing during normal read or write transfer functions. This allows transfers to occur from (write) or to (read) the same memory location throughout the entire transfer operation.

13 ATTENTION INTERRUPT ENABLE — Causes the controller to raise an interrupt request whenever any disc raises its Attention line. Cleared at the completion of the interrupt, by INIT or RESET functions. This is a read/write bit.

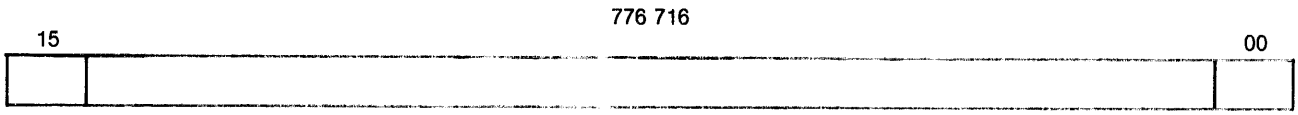
14 HARD ERROR — The OR of all errors except data error. This is a read only bit.

15 ERROR — The OR of all errors. This is a read only bit.

Note

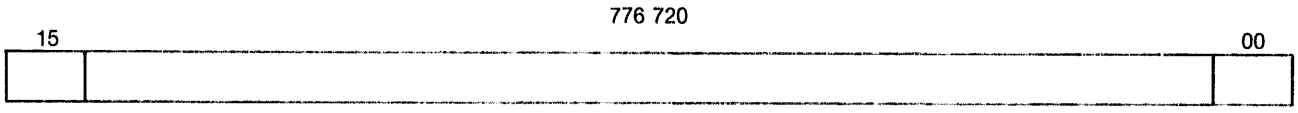
The controller device handler software must include routines that test the ERR and the HE flags to validate the current operation before proceeding.

Word Count Register (RPWC)



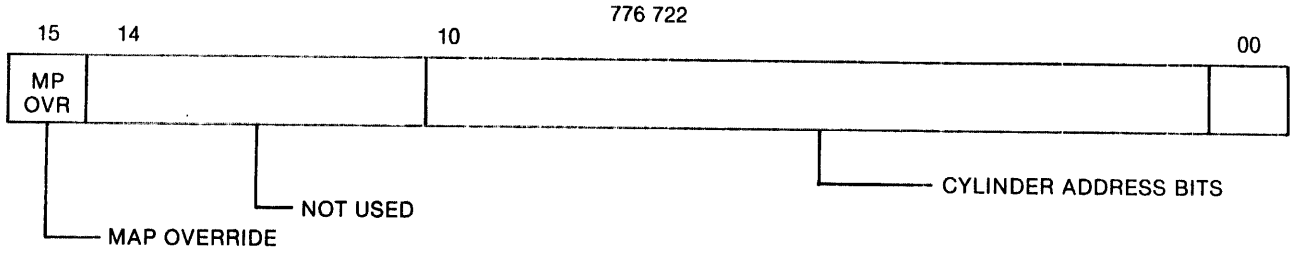
The address of RPWC is 776 716. This is a read/write register. The bits of this register contain the 2's complement of the total number of words to be transferred during a read, write, or write check operation. The register is incremented by one after each transfer. When the register overflows (all WC bits go to zero), the transfer is complete and controller action is terminated at the end of the present disc sector. Only the number of words specified in the RPWC are transferred. Cleared by INIT or RESET functions.

Bus Address Register (RPBA)



The address of RPBA is 776 720. The bits of this register contain the bus address of data transferred during read, write, or write check operations. The register is incremented by two at the end of each transfer (except if the IBA on the RPCS register is set). If the system has extended memory, the RPBA will overflow to the EX MEM bits (04, 05) of the RPCS to reflect the extended bus address. This is a read/write register cleared by INIT or RESET functions.

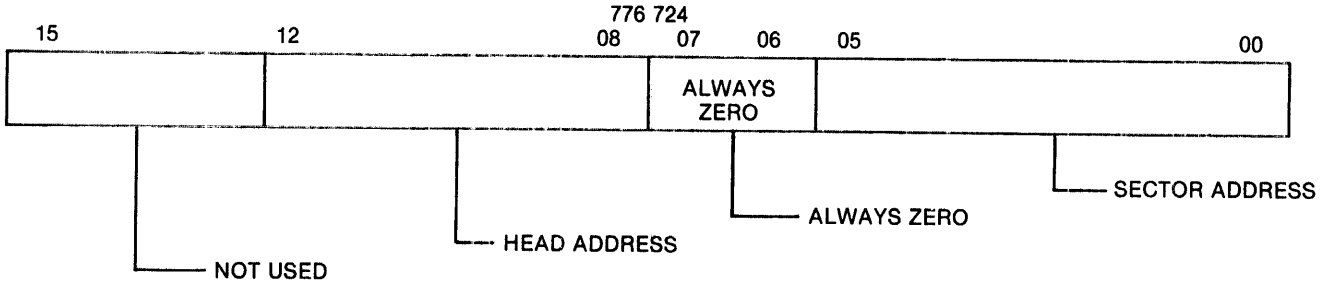
Cylinder Address Register (RPCA)



The address of RPCA is 776 722. Bits 00-10 contain the binary representation of the disc cylinder to be used for any disc operation. Bits 00-10 are read/write bits cleared by INIT or RESET functions.

Bit 15 is a MAP OVERRIDE bit. This bit can be set by the programmer to override the controller mapping algorithm. When set, the head, cylinder, and sector addresses supplied to the controller specify absolute addresses to the disc. Could be typically used to permit the RP02/03 device handler to be modified to take advantage of the head per track options available in some disc drives. This bit is always set during the initialization of the format routine. In Emulation mode MP is off and cylinder address range is 0-511 cylinders. Cleared by INIT or RESET functions. Bits 11-14 are not used.

Disc Address Register (RPDA)



The address of RPDA is 776 724. In Emulation mode the head address range is 0-19 heads; sector address range is 0-9 sectors. The bits of this register are read/write bits cleared by INIT or RESET functions.

The significance of the bits of this register is as follows:

Bit(s)	Definitions
00-05	SECTOR ADDRESS — Specifies the disc sector to be used for any operation other than Seek Home (Restore). Cleared by INIT or RESET functions.
06-07	ALWAYS ZERO.
08-12	HEAD ADDRESS — Specifies the head (surface) of the disc to be used for the next operation. Cleared by INIT or RESET functions.
13-15	NOT USED.

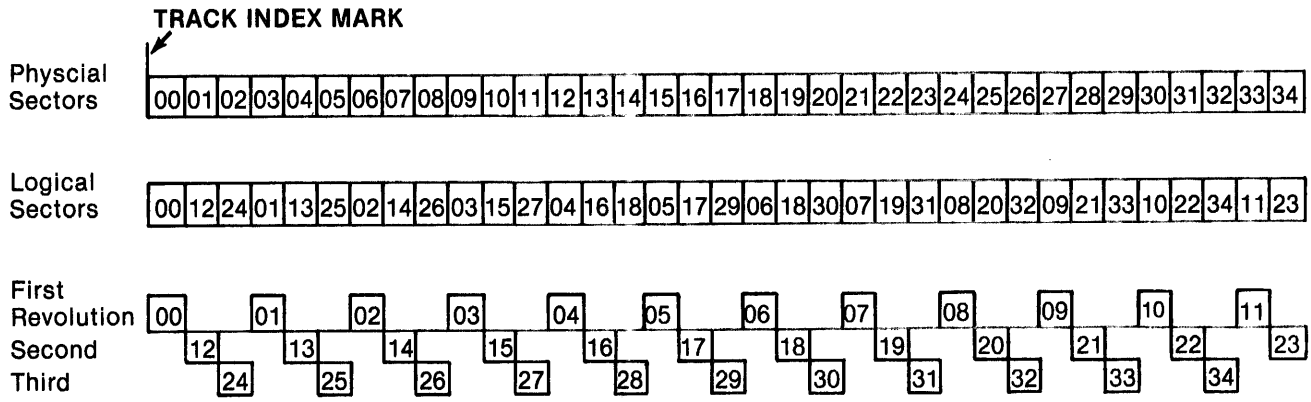
Data Buffer Register (RPDB)

The address of RPDB is 776 726. This is a read/write register cleared by INIT or RESET functions. This register functions as a general purpose data handler.

INTERLACING

Interlacing is the technique used to match the transfer rate of the disc to the transfer rate of the computer. The data transfer rate of the disc is typically 1.2 megabytes per second (600 kilowords per second). The transfer rate via the DMA facility of the LSI-11 is approximately 500,000 16-bit words per second.

To match this difference in transfer rates, first, full-sector buffers are contained in the controller, second, data records are interlaced on the tracks of the disc. Figure 4-2 illustrates a 3:1 interlace for a typical SMD-type disc with 35 sectors per track and rotating at 3600 RPM.



1. Disc speed = 3600 RPM
2. Sector size = 512 Data bytes per sector
3. Each disc revolution reads or writes 12 consecutive logical sectors.

Figure 4-2. Sector Relationships for a 3:1 Interlace

SECTION 5
TROUBLESHOOTING AND THEORY

This section describes troubleshooting procedures at three levels of complexity: basic system, controller symptoms and detailed analysis. Basic system troubleshooting procedures are visual checks not requiring test equipment and may be performed by the operator. Controller symptom procedures may require a scope, meter, extender board or diagnostics and should be performed by a technician. Detailed analysis is troubleshooting at the IC level, and is presented for engineers or system analysts for controller evaluation. The latter method may require the use of test equipment and the material presented here: board layout, term listing, theory of operation and logic diagrams.

CAUTION

Any troubleshooting requires a familiarity with the installation and operation procedures in this manual, the appropriate DEC manual, and the disc drive manufacturers manual. Ensure power is off when connecting or disconnecting board or plugs.

BASIC SYSTEM TROUBLESHOOTING

The following should be checked before power is applied:

1. Verify that all signal and power cables are properly connected. Ribbon cable connectors are *not* keyed. The arrows on the connectors should be properly aligned.
2. Verify that all switches are properly set as described in Sections 2 and 3.
3. Verify that all modules are properly seated in the computer and properly oriented.

The following should be checked during or after application of power:

1. Verify that the computer and disc drive generate the proper responses when the system is powered up.
2. Verify that the computer panel switches are set correctly.
3. Verify that the console can be operated in the local mode. If not, the console may be defective.
4. With the drive power switch on, verify that the drive READY light is on.
5. Verify that the green diagnostic light on the controller is on.

CONTROLLER SYMPTOMS

Controller symptoms, possible causes and checks/corrective action are described in Table 5-1. Voltage checks should be performed before troubleshooting more complex problems. The +12V and −5V sources are shown on Logic Diagram Sheet 3. The +5V source may be checked from any component shown on the other logic diagrams.

PHYSICAL LAYOUT

The physical layout of the board is shown in Figure 5-1. Column and row numbers on the layout correspond to the numbers on each IC on the logic diagrams.

TERM LISTING

The input and output terms for each logic diagram are described in Table 5-2. The sources and destinations refer to the sheet numbers on the logic diagrams.

Table 5-1. Controller Symptoms

Symptom	Possible Causes	Check/Corrective Action
1. Green DIAG light on the controller is OFF.	1. Microprocessor section of controller inoperative: a. Bad oscillator (Sheet 3, B22) b. Short or open on board c. Bad IC d. PROMs not properly seated (Sheet 8 A1 through A7)	1. Controller/Place controller on extender board. With a scope, check the pins on the 2901 (Sheet 7 and 9). All pins except power and ground should be switching. Check for "stuck high" or "stuck low," or half-amplitute pulses. Check +12V and −5V power (Sheet 3) and +5V at various IC's. Check PROMs A1 through A7 for proper seating. Check oscillator B22.
2. No communication between console and computer.	2. I/O section of controller "hanging" Q Bus: a. $\overline{\text{DEN}}$ always low b. Shorted bus tranceiver IC. c. Bad CPU board.	2. Computer interface logic of controller/ a. Check signal $\overline{\text{DEN}}$ for constant assertion. b. Check I/O IC's. Remove controller board to see if trouble goes away. (Ensure slot is filled or jumpered.) c. Run CPU diagnostics.
3. No data transfers to/from disc.	3. Disc not ready, bad connection, or bad IC in register section of the controller.	3. Disc/Consult the disc manufacturer's manual for proper setting of disc switches, or READY, NO FAULT, or UNSAFE lights. Check cable connections. Controller Registers/Using ODT, examine controller register RPDS, 176710. Bits 15 and 14 must be "ones". These bits represent DISC UNIT READY AND SELECTED and must be present for proper communication. Using ODT, deposit "ones" and "zeros" in the remaining disc registers and verify proper register data.
4. Data transferred to/from disc incorrect.	4. Multiple Causes: a. Bad memory in backplane b. Noise or intermittent source of DC power in computer. c. Bad IC in disc I/O section of controller. d. Bad area on disc. e. Disc heads not properly aligned.	4. Computer-controller-disc/ a. Run memory diagnostics. b. Check AC and DC power. c. While operating, check lines from controller to disc with a scope for short or open. d. Run the Format and Diagnostic Test program (Section 3). If errors occur at the same place on the disc, it is probably a bad area on the disc. Assign alternate tracks as specified in Section 3. e. Consult disc drive manufacturer's manual and align heads.
5. Intermittent failure-Controller runs for a short time after power is applied and then fails.	5. Failure of heat sense component on controller.	5. Isolate the bad component by using heat and cooling methods (heat gun, freon spray) and replace the bad cornponent.

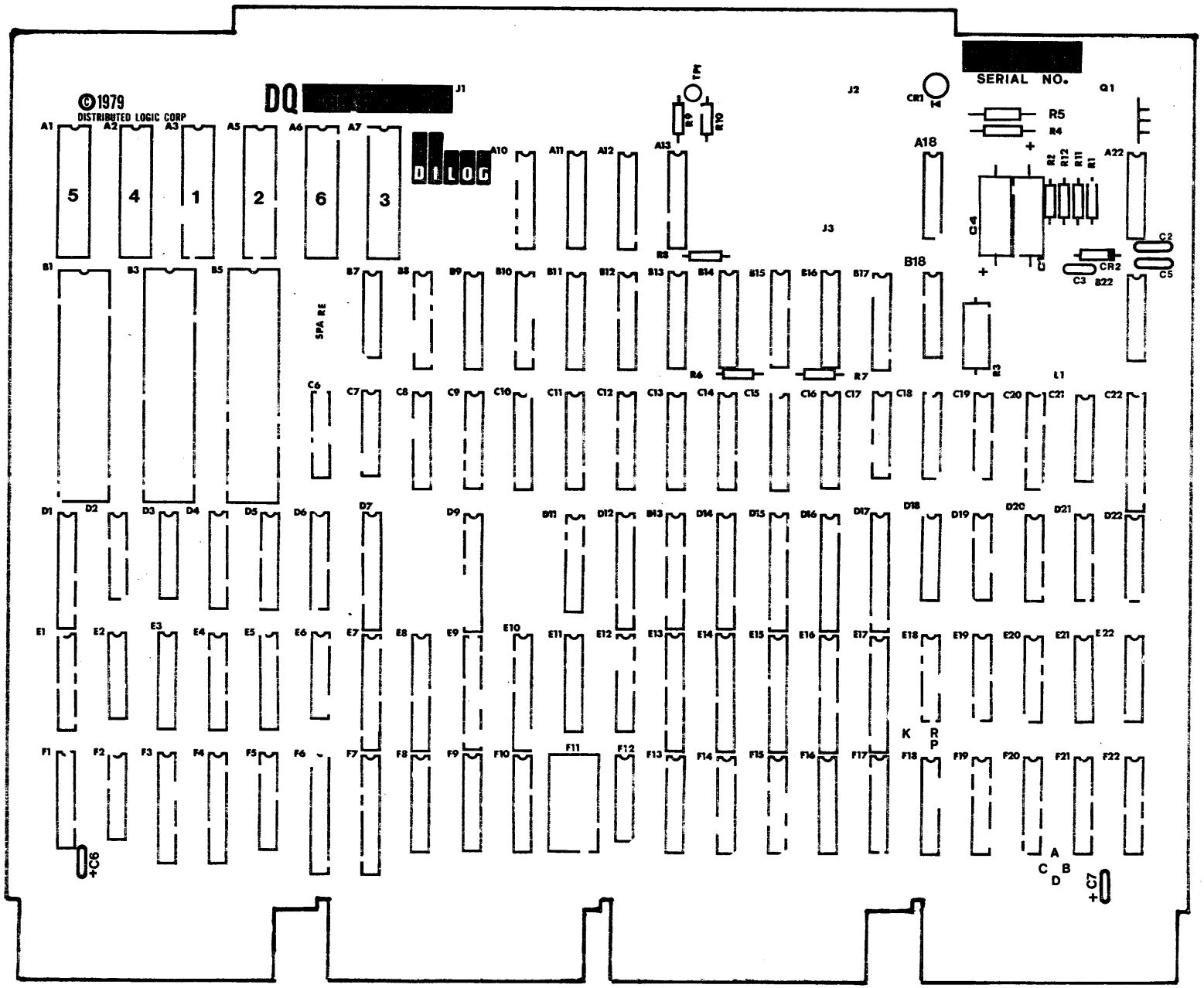


Figure 5-1. Board Layout

Table 5-2. Term Listing

Term	Source	Destination	Description
BA02+	13	16	Buffer Address
BA03+	13	16	Buffer Address
BA04+	13	16	Buffer Address
BBS7L	4	BUS (AP2)	Bus Peripheral Address Select
BBS7+	4	2	Peripheral Address Select
BC4+	12	13	Bit Count 4
BDAL00L	5	BUS (AU2)	Data Bus D/R
BDAL01L	5	BUS (AV2)	Data Bus D/R
BDAL02L	5	BUS (BE2)	Data Bus D/R
BDAL03L	5	BUS (BF2)	Data Bus D/R
BDAL04L	5	BUS (BH2)	Data Bus D/R
BDAL05L	5	BUS (BJ2)	Data Bus D/R
BDAL06L	5	BUS (BK2)	Data Bus D/R
BDAL07L	5	BUS (BL2)	Data Bus D/R
BDAL08L	6	BUS (BM2)	Data Bus D/R
BDAL09L	6	BUS (BN2)	Data Bus D/R
BDAL10L	6	BUS (BP2)	Data Bus D/R
BDAL11L	6	BUS (BR2)	Data Bus D/R
BDAL12L	6	BUS (BS2)	Data Bus D/R
BDAL13L	6	BUS (BT2)	Data Bus D/R
BDAL14L	6	BUS (BU2)	Data Bus D/R
BDAL15L	6	BUS (BV2)	Data Bus D/R
BDCOK–	4	7	DC Power OK
BDCOKH	BUS (BA1)	4	DC Power OK
BDIN+	4	2, 11	Data In
BDINL	4	BUS (AH2)	Master Ready For Data
BDMG1L	4	BUS (AR2)	DMA Grant Input/ Output
BDMRL	4	BUS (AN1)	Q Bus Request
BDOUT+	4	11	Data Out
BDOUTL	4	BUS (AE2)	Valid Data From Master on Bus
BD16L	4	BUS (AC1)	Extended Address
BD17L	4	BUS (AD1)	Extended Address
BFULE+	3	13	Enable Buffer Full (16)
BFULL–	13	11, 12, 14	Buffer Full
BIAKIL	4 BUS	BUS (CM2)	Bus Acknowledge Interrupt Levels In
BIAKIL	4	BUS (AM2)	Bus Acknowledge Interrupt Levels In
BIAKOL	4	BUS (CN2)	Interrupt Acknowledge Output
BIAKOL	4	BUS (AN2)	Interrupt Acknowledge Output
BINITL	4	BUS (AT2)	Initialize-Clear Devices on I/O Bus
BIRQL	4	BUS (AL2)	Host I/O Interrupt Request
BIT0+/ BIT 10+	14	J1	Disc Control Cable Drivers
BIT 0–/ BIT 10–	14	J1	Disc Control Cable Drivers
BITCK+	12	13	Bit Check
BIT5	14	15	Hard Sector Applicable
BMBGIL	4	BUS (CR2)	DMA Grant I/O
BMBGOL	4	BUS (CS2)	DMA Grant I/O
BMBGOL	BUS 4	BUS (AS2)	DMA Grant Out

Term	Source	Destination	Description
BPOK-H	BUS (BB1)	15, 14	Primary Power OK
BRLYL	4	BUS (AF2)	Reply From Slave
BRPLY+	4	2, 3, 11	Q Bus Reply
BSACKL	4	BUS (BN1)	DMA Request Acknowledge
BSYNCL	4	BUS (AJ2)	Synchronize I/O Address
BTSPF+	2	11	Bootstrap Flag
BWTBTL	4	BUS (AK2)	Host I/O Write Byte
BWTBT+	4	11	Controller Write Byte
COUT+	9	7	Carry Out
CPO–	11	4	Control Decode-Reset Slave Request
CP1–	11	3	Control Decode-Set Data Out
CP2–	11	4	Control Decode-Reset Controller
CP3–	11	12	Control Decode-Reset Data Read Sync
CP4–	11	15	Control Decode-Reset Index Flop
CP5–	11	15	Control Decode-Set Index Flop
CP6–	11	2	Control Decode-Reset Q Bus Request
CP7–	11	3	Control Decode-Reset Data Out
CRCER+	11	16	CRC Error Detector
CR1-0/ CR1-2	8	7, 9	Microcode Instruction
CR1-3	8	9, 10, 15	Microcode Instruction
CR1-4/ CR1-7	8	9, 10	Microcode Instruction
CR2-0/ CR2-7	8	9	Microcode Instruction
CR3-0	8	7	Microcode Instruction
CR3-1/ CR3-3	8	9	Microcode Instruction
CR3-4/ CR3-7	8	10	Microcode Instruction
CR4-0/ CR4-7	8	7	Microcode Instruction
CR5-0/ CR5-7	7	8	Vector Address Register
CR5-0/ CR5-7	8	7	Microcode Instruction
CSA0+/ CSA8+	7	8	Control Store Memory Address
DAT0+/ DAT7+	12	13	Data Buffer Data Bus-Bidirectional
DAT0+/ DAT7+	13	12	Data Buffer Data Bus-Bidirectional
DA16+	3	4	Extended Data
DA17+	3	4	Extended Data
DBWS–	12	13	Data Buffer Write Strobe
DB07+/ DB07+	5	2, 11	Data Bus D/R

Table 5-2. Term Listing (Continued)

Term	Source	Destination	Description
DB13+/ DB15+	6	11	Data Bus D/R
DB08+/ DB12+	6	2, 11	Data Bus D/R
DEN–	5	4, 6	Enable Data
DMGI+	4	2	DMA Grant In
D00+/ D07+	2	9	Slave Address Register
D00+/ D07+	8	9	Source Bus Data Bit
D00+/ D07+	10	9	Interrupt Vector Bootstrap Loader
D00+/ D07+	11	9	Data Input MUX
D00+/ D07+	12	9	Source Bus Data Bit
D00+/ D07+	15	9	Switch Signals MUX
D00+/ D05+	15	9	Disk Status Register MUX
D00+/ D07+	16	9	Seek End/Unit Sel/ Status Reg/MUX
EADD+	3	5, 6	Enable Address-Q Bus Control
EADD–	5	4	Enable Address-Q Bus Control
EBITC+	3	12	Enable Bit Count
EDATA+	3	5	Enable Data- Q Bus Control
GDATA+	12	11	Enable/Read
GSCLK–	3	7, 8, 9, 10	Gated System Clock
HOLD	14	J1	Soft Sector Applicable
IAKI+	4	2	Host Interrupt Acknowledge In
IAKIG–	2	11	Interrupt Acknowledge Inverted
INIT+	4	7	Initialize
LCOUT–	7	9	Latch Carry Out
LXRA–	10	14	Drive Control (Bus 0-7)
LXRB–	10	7	Load Vector Address
LXRC–	10	3	System Control
LXRD–	10	3	Reset Data In
LXRE–	10	3	Q Bus Control
LXRO–	10	6	Data Out Register (MSB)
LXR1–	10	5	Data Out Register
LXR2–	10	6	DMA Address (MSB)
LXR3–	10	5	DMA Address (LSB)
LXR4–	10	13	Data Buffer Address (LSB)
LXR5–	10	13	Data Buffer Address (MSB)
LXR6–	10	12	Data Buffer Data
LXR7–	10	11	Control Pulse Strobe
LXR9–	10	14	Drive Control (TAGS)
MRQB+	3	2	Request Q Bus
OCD+	14	J1	Output Cable Detect
OCD–	14	J1	Output Cable Detect

Term	Source	Destination	Description
PICK	14	J1	Soft Sector Applicable
RCLOCKA+	J2	16	Read Clock Receiver
RCLOCKA–	J2	16	Read Clock Receiver
RCLOCKB+	J3	16	Read Clock
RCLOCKB–	J3	16	Read Clock
RDATA+	16	12	Serial Data Input
RDATAA+	J2	16	Read Data Receiver
RDATAA–	J2	16	Read Data Receiver
RDATAB+	J3	16	Read Data Receiver
RDATAB–	J3	16	Read Data Receiver
RESET–	4	2, 3, 7, 14	Controller Reset
RSYNC	4	2, 11	Synchronize 2901 to Host I/O Lines
R/WCK	16	12, 11	Read/Write Check
R/WSRE+	3	12	Shift Register Reset
SCLK+	3	10, 12, 13	Controller Clock
SCLK–	3	7, 11, 15, 16	Controller Clock
SCLOCKA+	J2	16	Servo Clock
SCLOCKA–	J2	16	Servo Clock
SCLOCKB+	J3	16	Servo Clock
SCLOCKB–	J3	16	Servo Clock
SEEKA+	J2	16	Seek A Receiver
SEEKA–	J2	16	Seek A Receiver
SL/IN+	2	7	Slave/Interrupt Acknowledge Request
TAG1+/ TAG3+	14	J1	Disc Tag Cable Drivers
TAG1–/ TAG3–	14	J1	Disc Tag Cable Drivers
TDIN+	3	4	Q Bus Data In
TDOUT+	3	4	Q Bus Data Out
TIAK+	2	4	Interrupt Acknowledge
TIRQ+	3	2, 4	Interrupt Request
TDMG+	2	4	Bus Grant To D/R
TMDR+	2	4	Memory Request To D/R
TQBUSA+	2	11	Q Bus Acknowledge
TRPLY+	3	4	Q Bus Reply
TSACK+	2	4, 3	System Acknowledge
TSACK–	2	4	System Acknowledge
TSYNC+	3	4	Q Bus Sync
TWTBT+	3	4	Write Byte Q Bus Control
USELA+	J2	16	Unit Select A Receiver
USELA–	J2	16	Unit Select A Receiver
USELB+	J3	16	Unit Select B Receiver
USELB–	J3	16	Unit Select B Receiver
USTAG+	14	J1	Unit Select Tag
USTAG–	14	J1	Unit Select Tag
USEL0+/ USEL3+	14	J1	Unit Select Cable Drivers
USEL0–/ USEL3–	14	J1	Unit Select Cable Drivers

Table 5-2. Term Listing (Continued)

Term	Source	Destination	Description
VEC –	7	8	Vector
WCLOCKA +	16	J2	Write Clock Driver
WCLOCKA –	16	J2	Write Clock Driver
WCLOCKB +	16	J3	Write Clock Driver
WCLOCKB –	16	J3	Write Clock Driver
WDATA	12	16	Write Data
WDATAA +	16	J2	Write Data
WDATAA –	16	J2	Write Data
WDATAB +	16	J3	Write Data
WDATAB –	16	J3	Write Data
WREN +	3	12, 13, 16	Write Enable
WREN –	12	13, 16	Write Enable
XSDO –	10	2	Slave Address
XSD1 –	10	11	Data Input (MSB)
XSD2 –	10	11	Data Input (LSB)
XSD3 –	10	11	Q Bus Status
XSD4 +	12	13	Data Buffer Source Decode
XSD4 –	10	12	Data Buffer Source Decode
XSD5 –	10	15	Disk Drive Status
XSD6 –	10	16	Seek End Status
XSD7 –	10	15	Select Bootstrap PROM
Y00 + / Y07 +	9	3, 5, 6, 7 10, 12, 13, 14	Y Bus
ZERO +	9	7	2901 Output At Zero
1KOV +	13	16	1024 Count Buffer Address

THEORY

The controller may be examined as three parts: computer interface, disc interface and controller internal functions. Signals from and to the computer are described in Section 1, Table 1-1. Signals from and to the disc drive are described in Tables 1-2 and 1-3. Figure 5-2 is a simplified block diagram illustrating the interfaces and some of the functional components. Single lines in the illustration represent serial data and the wider lines represent parallel data. A detailed block diagram of the controllers is shown on Sheet 1 of the logic drawings. The numbers in the blocks on Sheet 1 refer to the sheet numbers of the other logic diagrams.

Computer Interface

The purpose of the computer interface is to (1) buffer lines between the Q-Bus of the LSI-11 computer and the controller, and (2) to synchronize information transfers. The controller is a slave device during initialization and status-transfer sequences. The controller is selected by base address 776 710_8. The controller is bus master during data transfers and either receives data from or outputs data to the computer memory via the LSI-11 DMA facility.

The control lines request information transfers, select the type and direction of transfers, and synchronize the transfers. The control lines are unidirectional and used for "bus arbitration." Bus synchronization is fully controlled by the controller microprocessor. This allows the computer bus to be used by other devices when the disc controller is busy with internal functions and controller/disc data transfers.

Data bus driver/receivers F13 through F16 (Sheets 5 and 6) buffer the input data and distribute it as DB 00-15 in the controller. The DB signals are routed to data and address decode registers located on Sheets 11 and 2.

Output data from the microprocessor Y Bus (Y00-Y07) is latched by registers E13 through E15, and transferred to the Q Bus via bus driver/receivers F13 through F16.

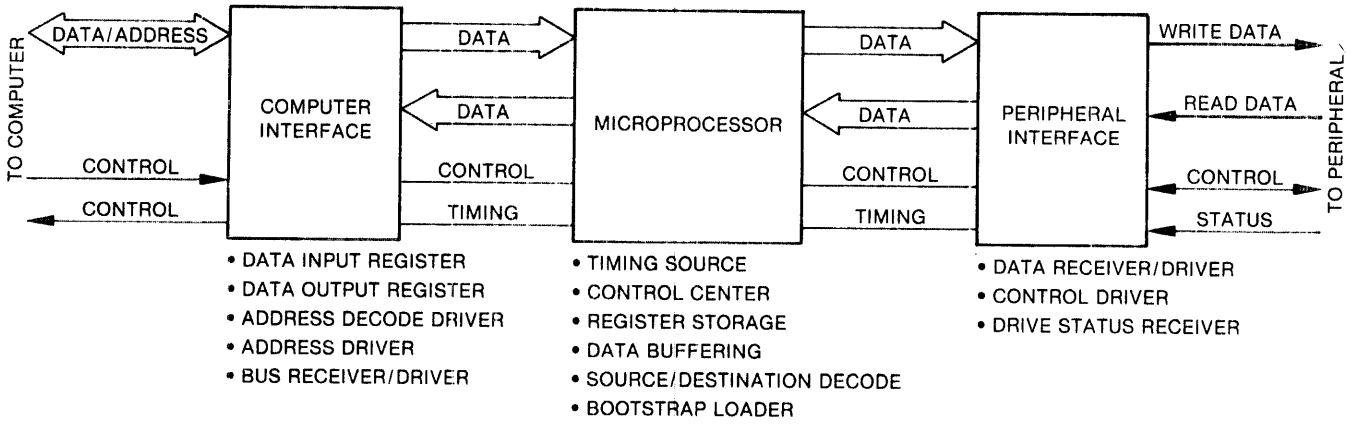


Figure 5-2. Simplified Block Diagram

Note that the Device Enable signal (DEN-) is active when either Address Enable (EADD) or Data Enable (EDATA) signal is active. DEN controls the operating mode of all data and address driver/receivers, under control of the firmware via the Y Bus (Sheets 5 and 6).

Disc Interface

The disc is connected to the controller by separate data and control cables. A common control cable is daisy-chained to both drives in a multiple-drive configuration, while separate data cables are always used.

Serial read data is received by receivers C16 or C15 (Sheet 16) and then converted to parallel data by the read/write shift register F7 (Sheet 12). In the reverse direction, parallel data from the data buffer is converted to serial data by the shift register, then sent to dual line drivers (Sheet 16).

The Control Cable drivers B8, B10, C8 and C10 (Sheet 14) are always enabled and are driven by the output of registers E8 and E10, which act as latches to capture the Y Bus data from the microprocessor.

Control Cable receivers B12 and C12 (Sheet 15) supply data to the disc status multiplexer D12 (Sheet 15) at all times. The data is available to the microprocessor via the D Bus when signal XDS5- is active.

Controller Internal Functions

The microprocessor is the timing and control center of the controller. The microprocessor is controlled by instructions stored in programmable read-only memory (PROM). The instructions, called "firmware", cause the microprocessor to operate in a prescribed manner during each of the computer-selected functions. The functions are established by a series of instructions issued by the LSI-11.

Because the disc and computer transfer data at different rates, it is necessary to buffer data going to and from the disc. High-speed RAM allows a full sector of data to be buffered during read and write operations.

All data transfer and computer/disc protocol is under microprocessor control. This feature allows modification of controller operating characteristics by making only changes to the firmware. Input/output logic remains essentially unchanged.

The output from the microprocessor is the "Y Bus". Y Bus instructions govern all controller operations by acting as the controller source for all receivers and drivers either directly or through the source/destinations decode IC's (Sheet 10).

The "D Bus" is the data input to the microprocessor. Tri-state drivers allow many signal sources to be connected to the bus while only one at a time is enabled by the source/destination decode logic on Sheet 10.

The following list describes D Bus enabling signals:

Function	Term	Component Enabled	Sheet
Slave Address	XDS0	D16	2
Data Input (MSB)	XDS1	D14	11
Data Input (LSB)	XDS2	D15	11
Q-Bus Status	XDS3	D17	11
Data Buffer	XDS4	D7	12
Disc Status	XDS5	D12	15
Seek End/Unit Select	XDS6	D13	16
Option Select	XDS7	D11	15
Bootstrap/Interrupt	XDS7	D9	10

All data on the D Bus is under control of the firmware as decoded by PROM F8 on Sheet 10. The microprocessor selects the proper input data by enabling one of the above lines.

The Y Bus is the microprocessor output. Output of the microcode PROM A7 (Sheet 8) is decoded by F9 and F10 (Sheet 10) to select the destination of the data on the Y bus.

The following list describes Y Bus enabling signals:

Function	Term	Component Enabled	Sheet
Data Out Register (MSB)	LXR0	E13	6
Data Out Register (LSB)	LXR1	E15	5
DMA Address (MSB)	LXR2	E14	6
DMA Address (LSB)	LXR3	E16	5
Data Buffer Address (LSB)	LXR4	E4	13
Data Buffer Address (MSB)	LXR5	E5	13
Data Buffer Data	XLR6	E7, C18	12
Control Pulse Strobe	LXR7	C20	11
Drive Control (Tags)	LXR9	E8	14
Drive Control (Bus 0-7)	LXRA	E10	14
Load Vector Address	LXRB	D1	7
System Control	LXRC	E17	3
Reset Data In	LXRD	E22	3
Q Bus Control	LXRE	E12, E22	3
Interrupt Vector Prom	LXRF	E9	10

With the single exception of bus reply detector D18 (Sheet 3), all data and address activity is controlled by the 15 signals shown above.

Each LXR (Load External Register) signal activates a register which, in conjunction with Y Bus data latches the appropriate data word.

Control Registers CR1 through CR5 are the outputs of the microcode PROMs (Sheet 8). These signals control the microprocessor functions and provide the data to the source/destination decode logic (Sheet 10).

Data Buffer

The data buffer and associated logic are shown on Sheets 12 and 13. Data Transfers to and from the buffer are both two-step operations. First, an entire sector of data is loaded into the buffer during either a read or write operation. Once loaded, the buffer contents are then transferred to disc or LSI-11 memory in a completely separate operation. Figure 5-3 illustrates read and write operations to and from the RAM data buffer.

During a write operation, parallel data (Y00-Y07) is transferred from LSI-11 memory via microprocessor to the storage latch E7 (Sheet 12). The data (DAT0-DAT7) is then transferred to the buffer F3 and F4 (Sheet 13). Parallel data (DAT0-DAT7) from the buffer is then transferred to shift register F7, converted to serial data (W DATA), and transferred to the data cable driver B17 (Sheet 16).

During a read operation, serial read data (R DATA) from the data cable receivers is ANDED with Enable Bit Count (E BIT C) resulting in the signal G DATA. This signal enters the shift register F7 and is transferred as parallel data to the storage latch F6, for transfer to the data buffer while the next byte is being shifted through shift register F7. The read data from the buffer (DAT0-DAT7) is transferred to driver D7 (Sheet 12) and to the microprocessor for transfer to LSI-11 memory.

The counter located at E3, E4 and E5 (Sheet 13) is used to address the location in the buffer to which data can be written into or read from. The counter has the capability of being preset to a specific starting address via the Y Bus of the microprocessor.

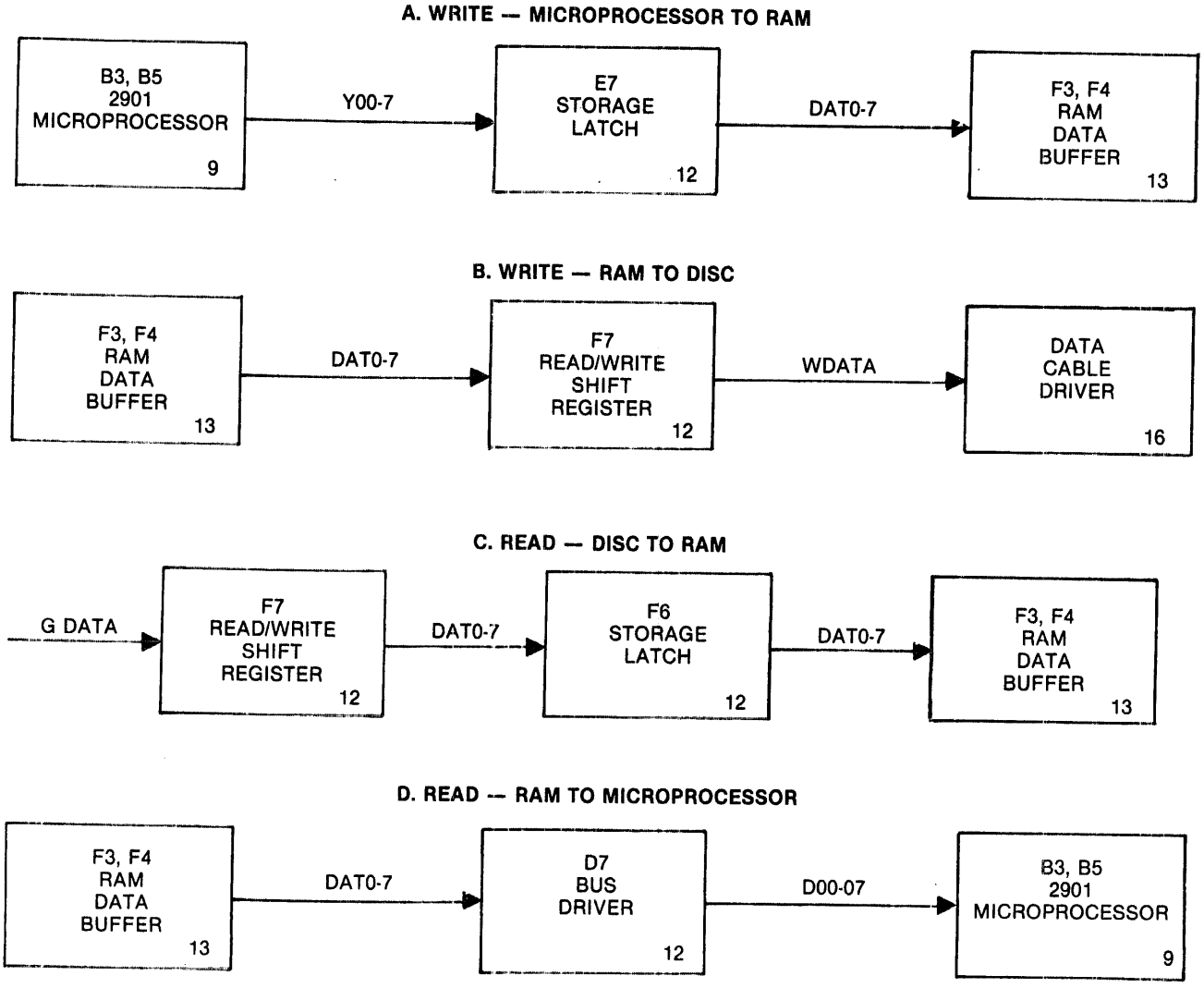
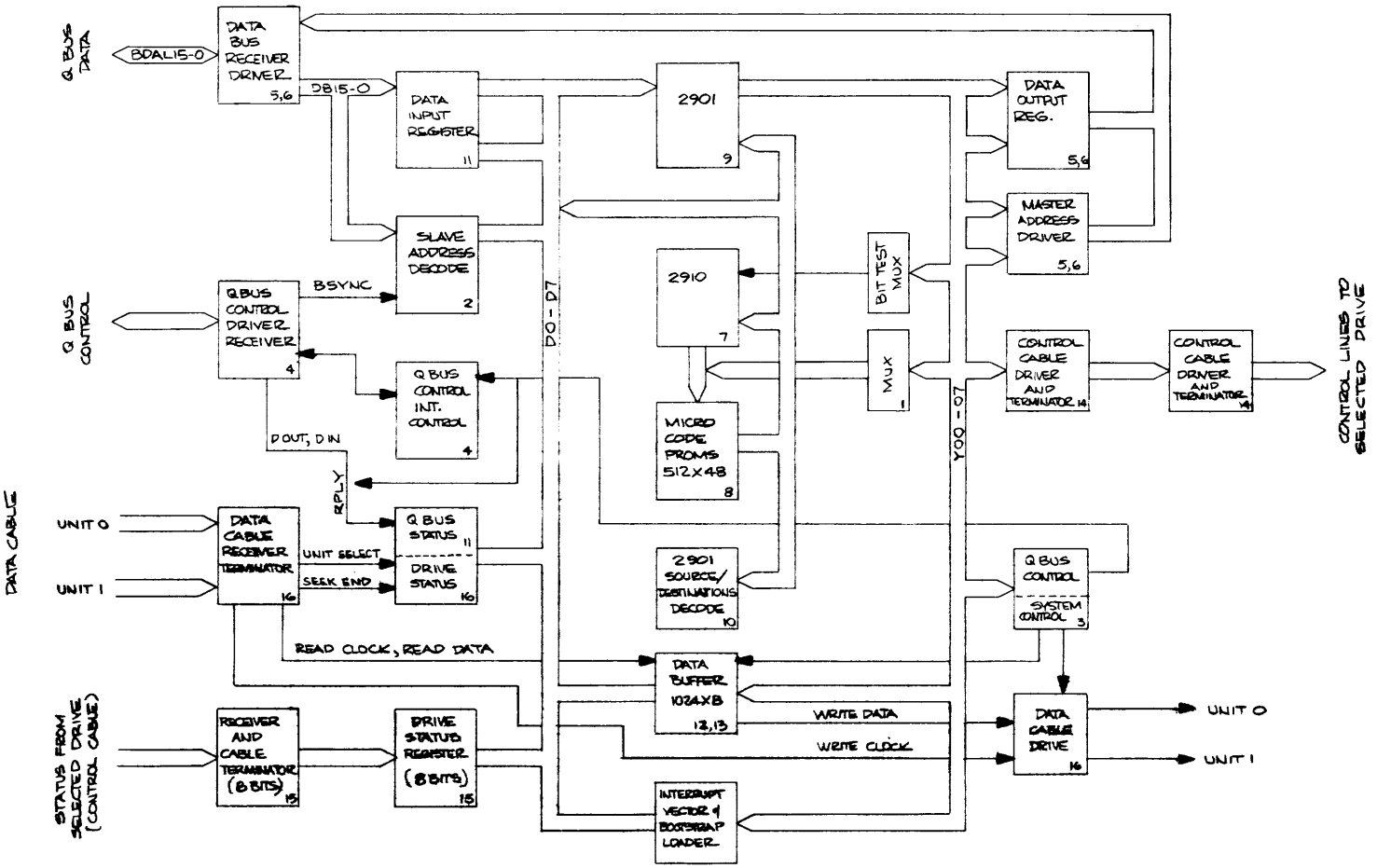


Figure 5-3. Data Paths



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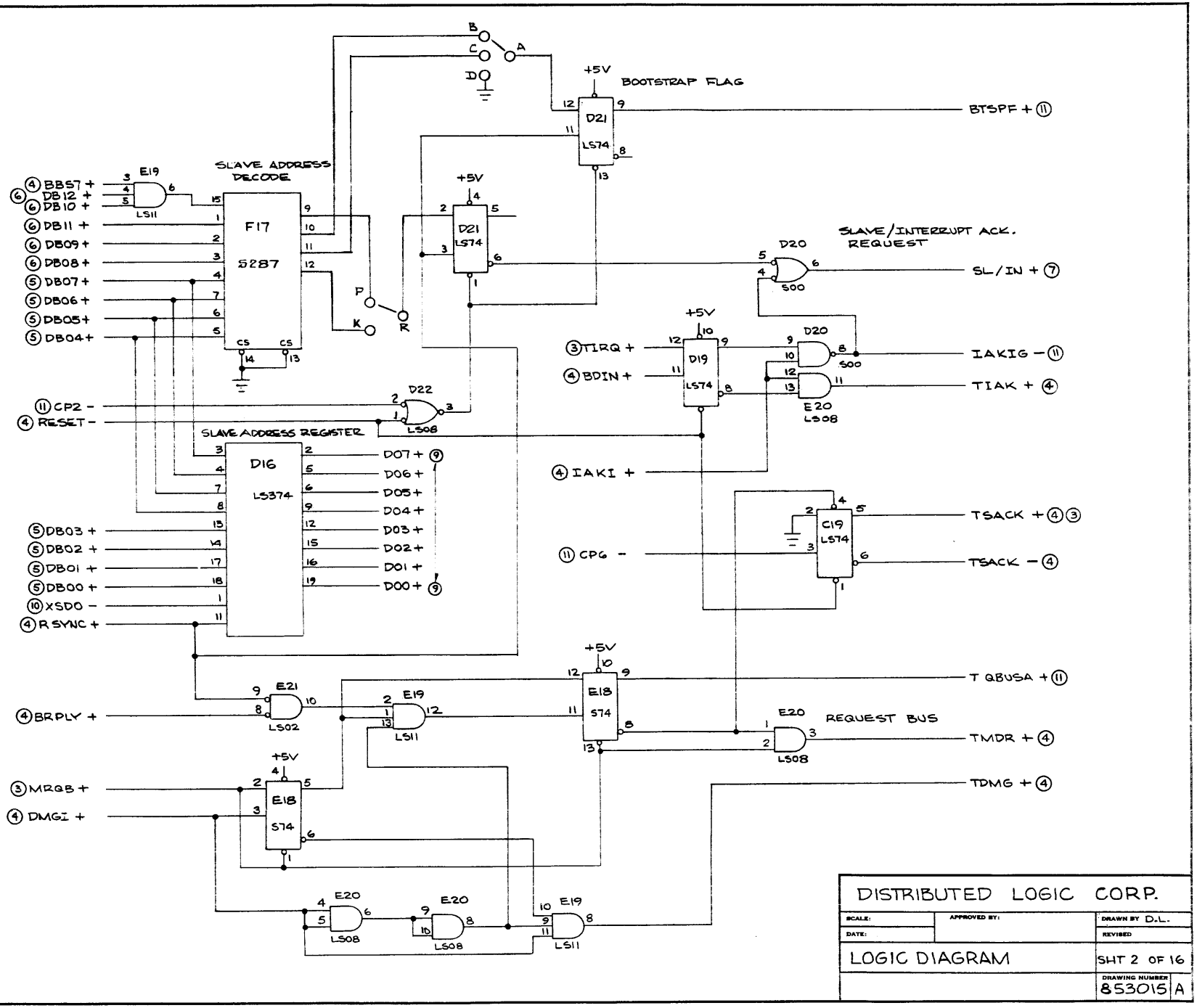
DQ202A DQ202 DQ200 USED ON	LOGIC DIAGRAM — SHT 1 OF 16
	DRAWING NUMBER 853015 A



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LOGIC DIAGRAM		SHT 2 OF 16
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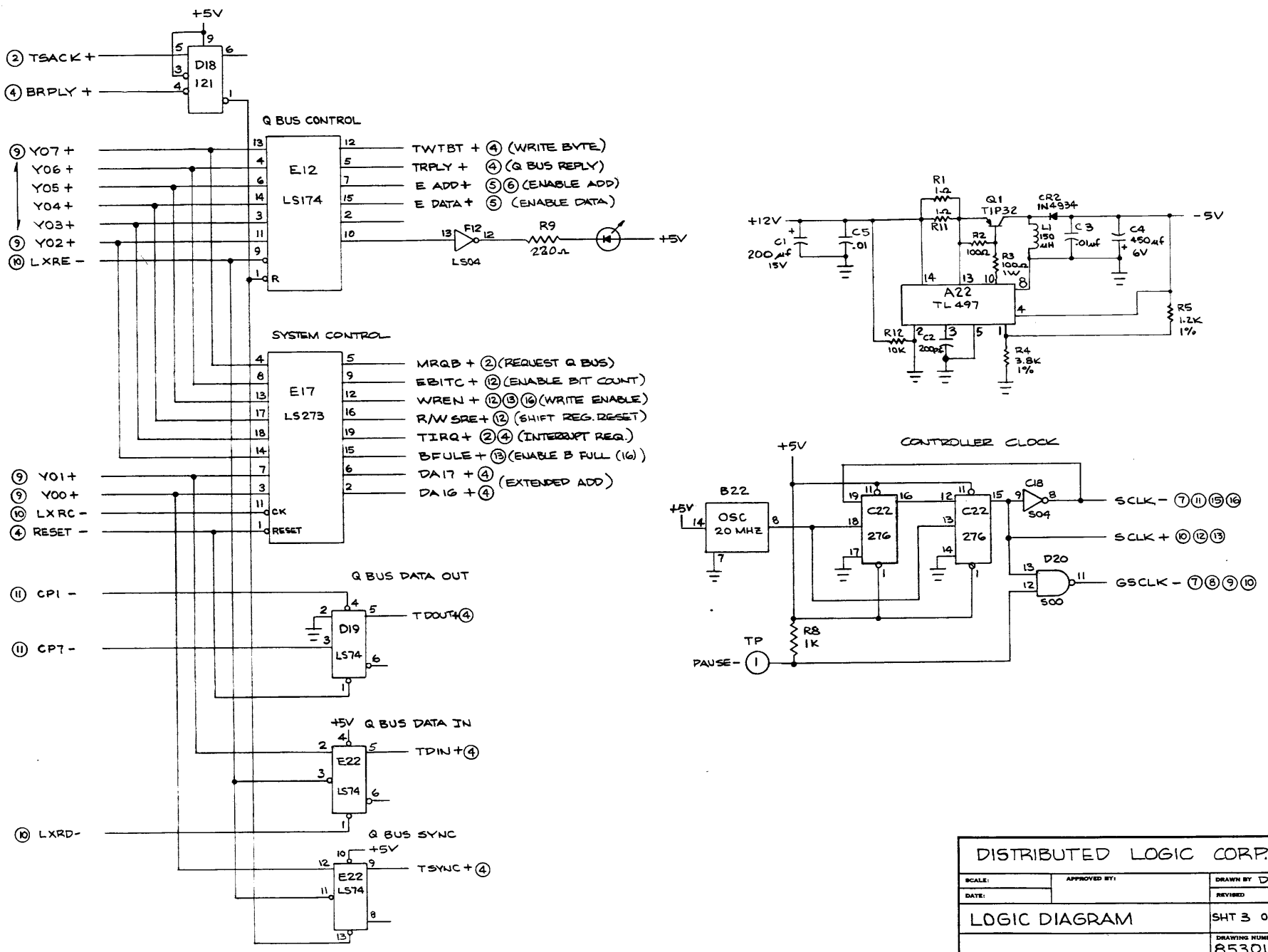

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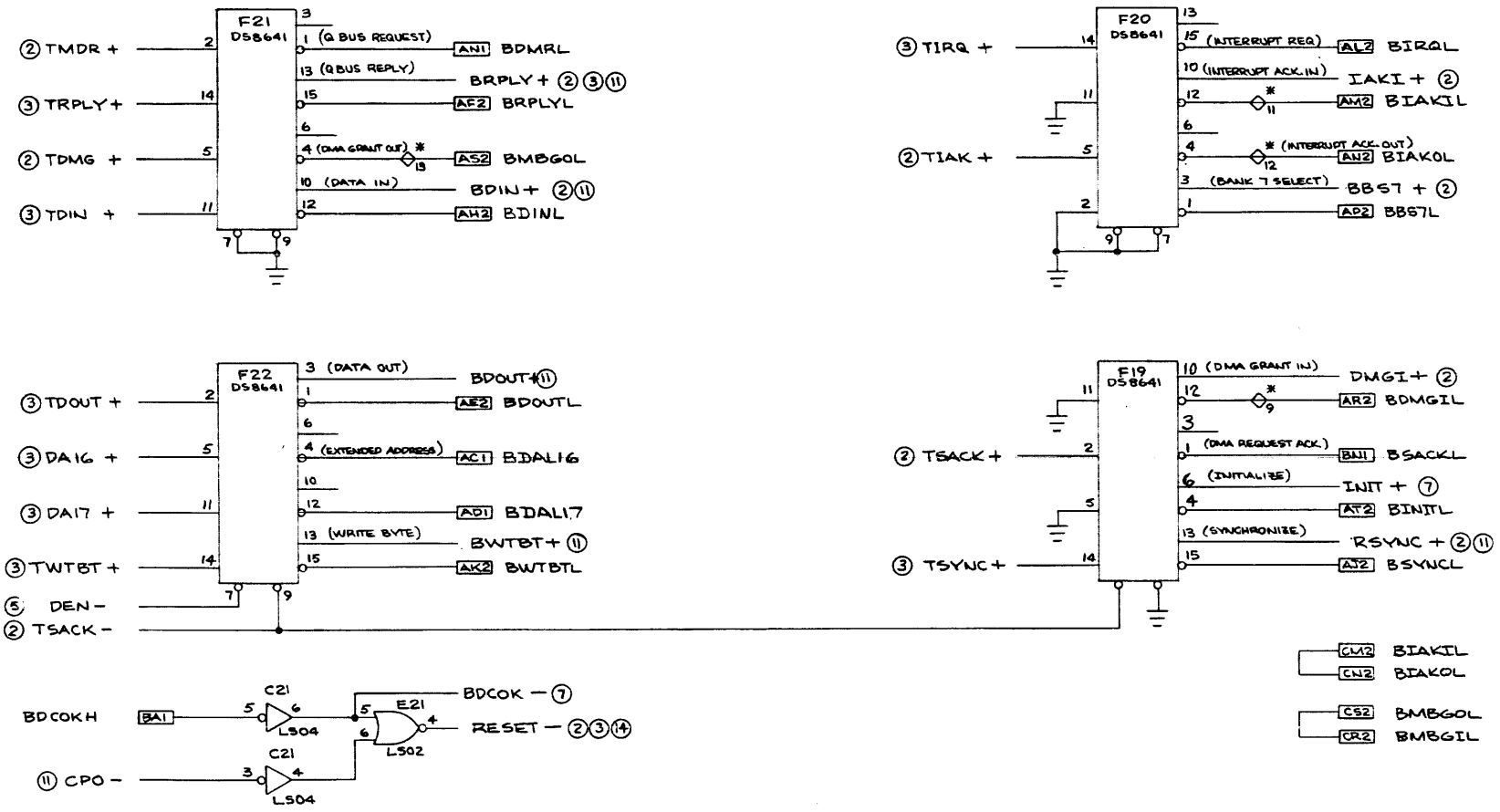

NOTE: * ◇—12 SYMBOL INDICATES PULL-UP (180Ω) / PULL-DOWN (390Ω) RESISTORS. NUMBER SHOWN IS PIN NUMBER USED IN PACK., LOCATION F18.

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LOGIC DIAGRAM		SHT 4 OF 16
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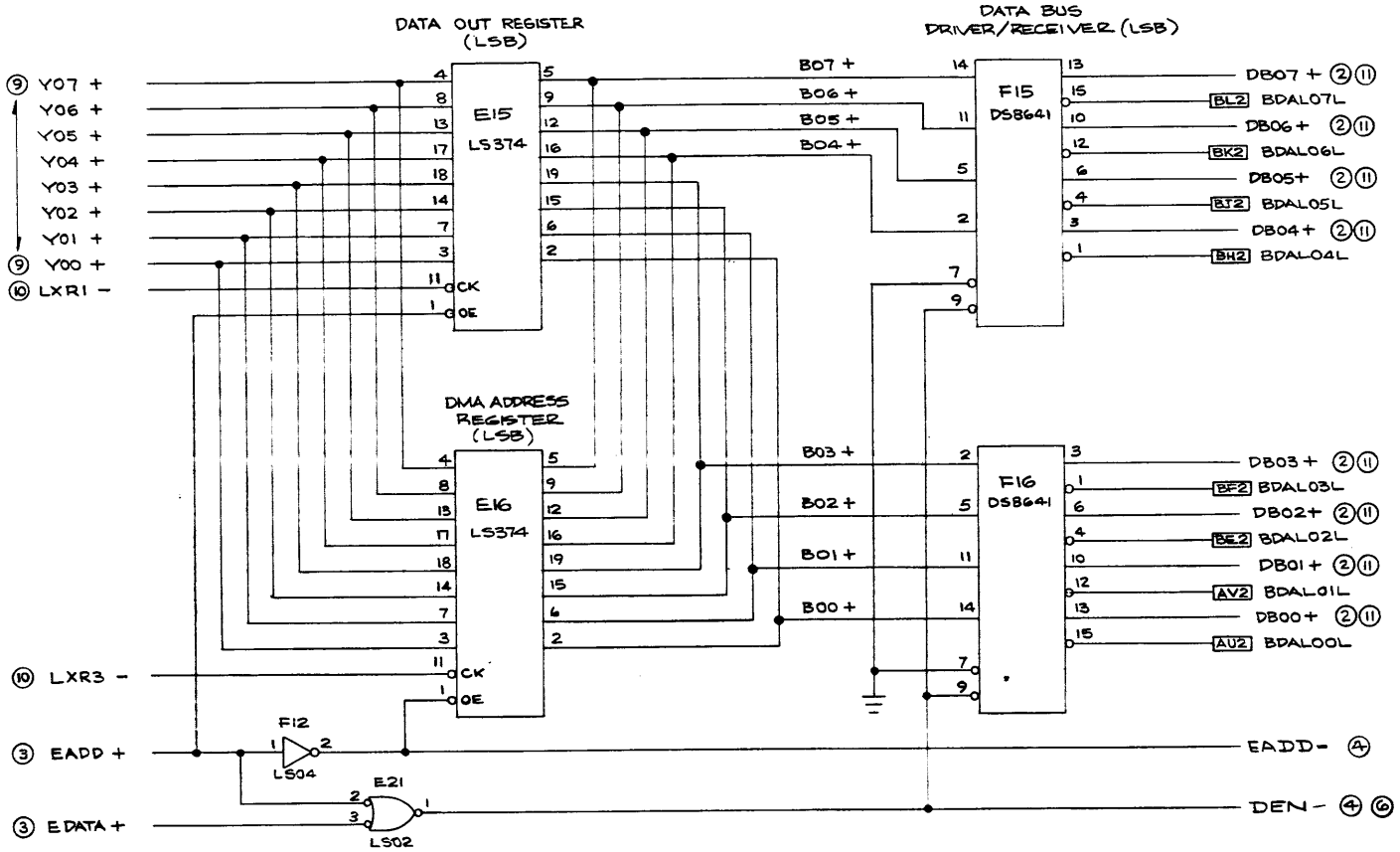

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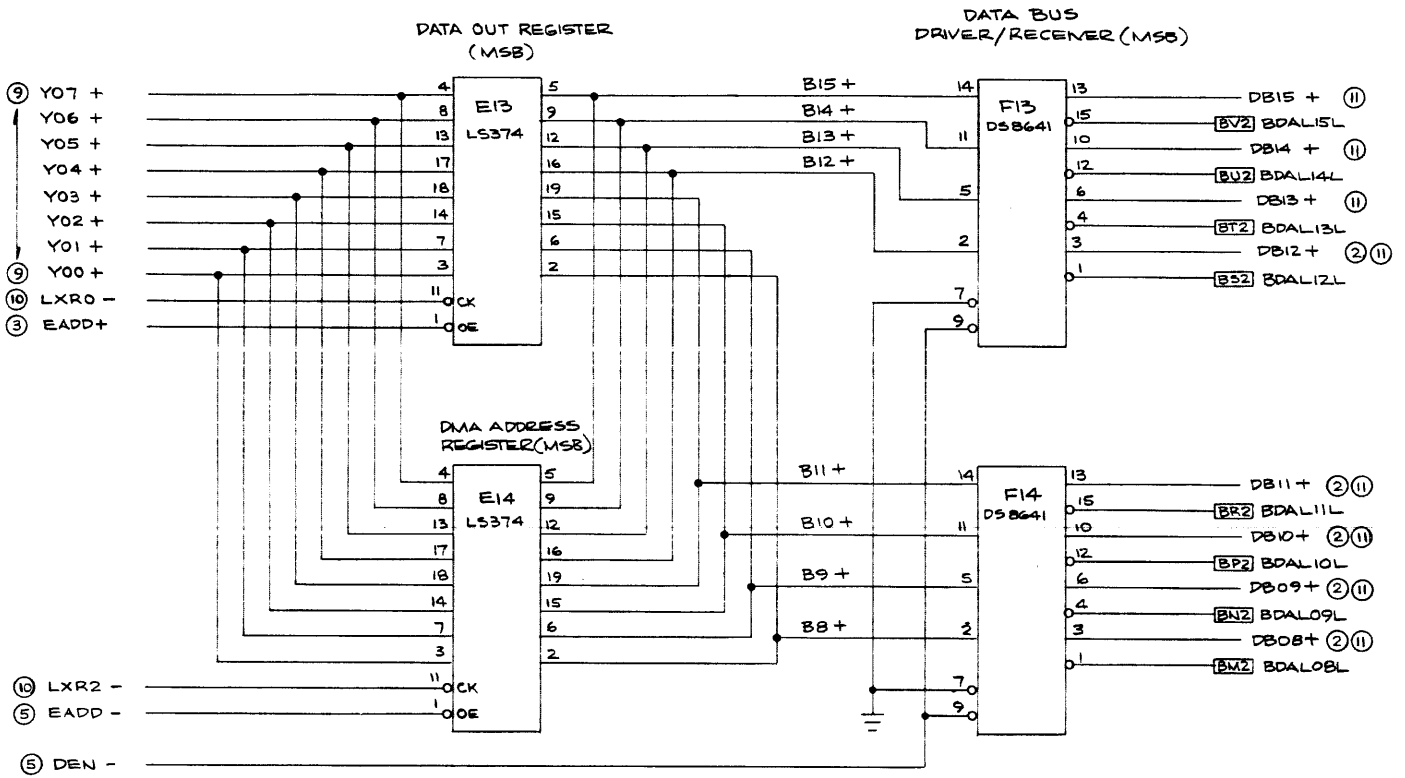

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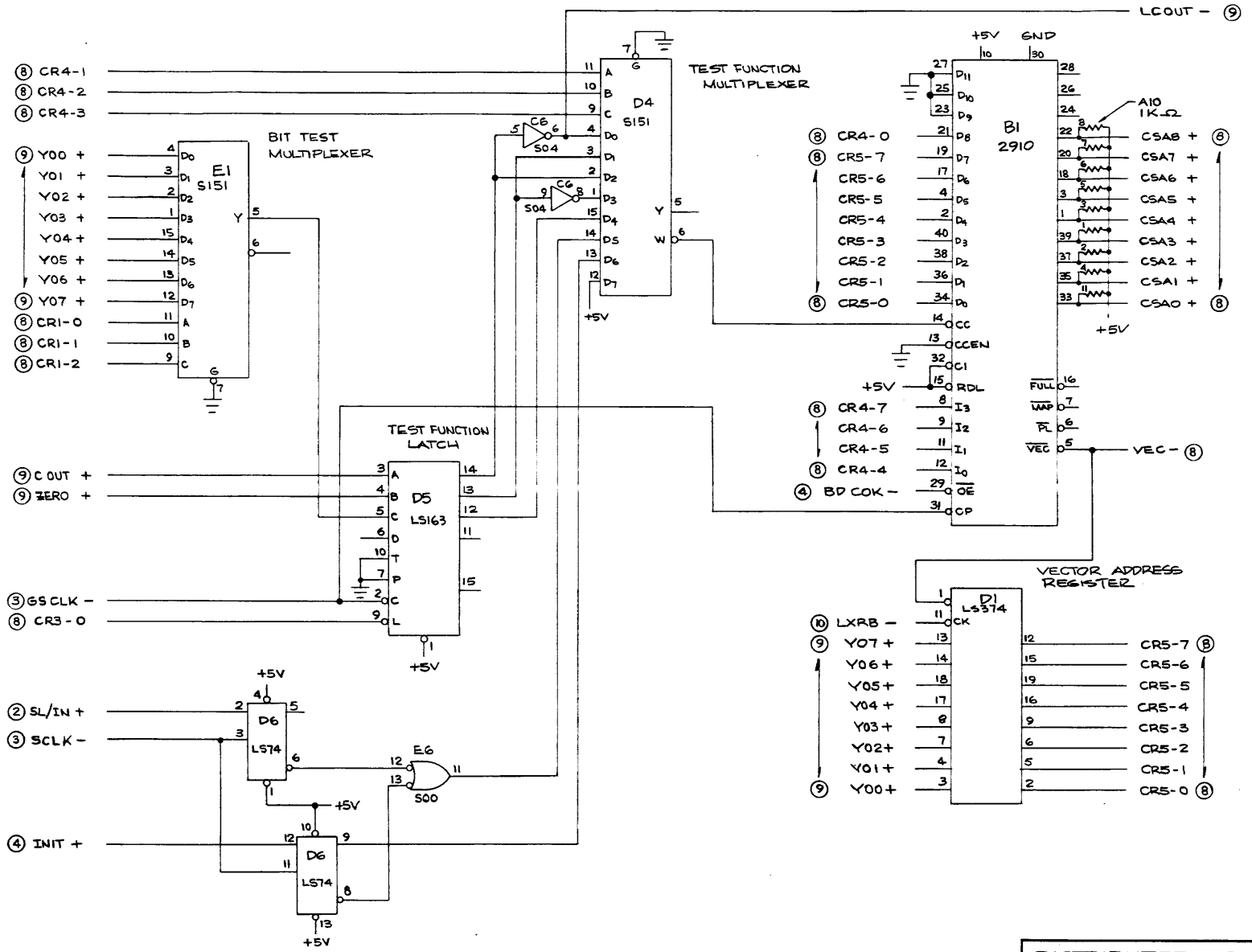

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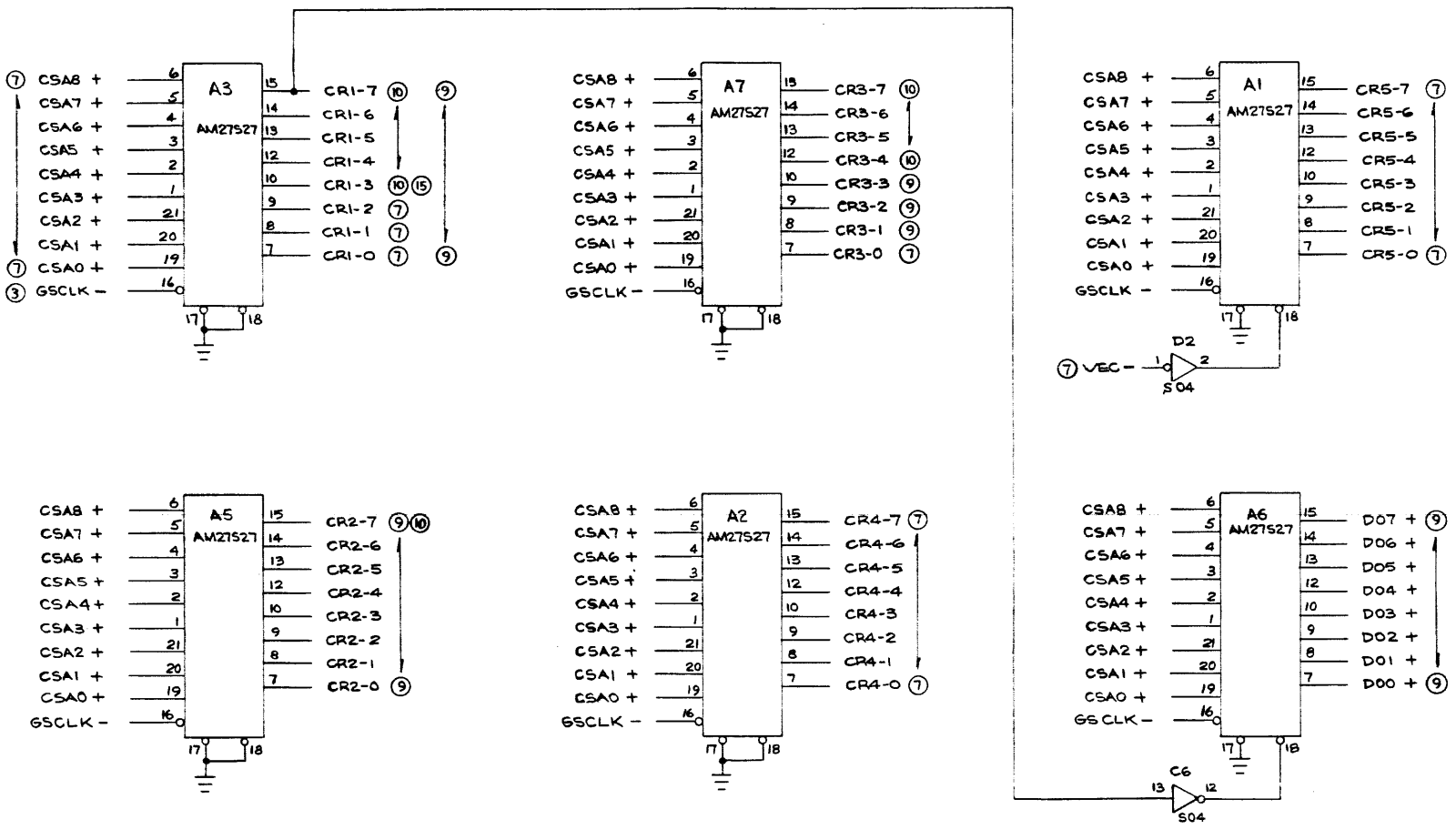

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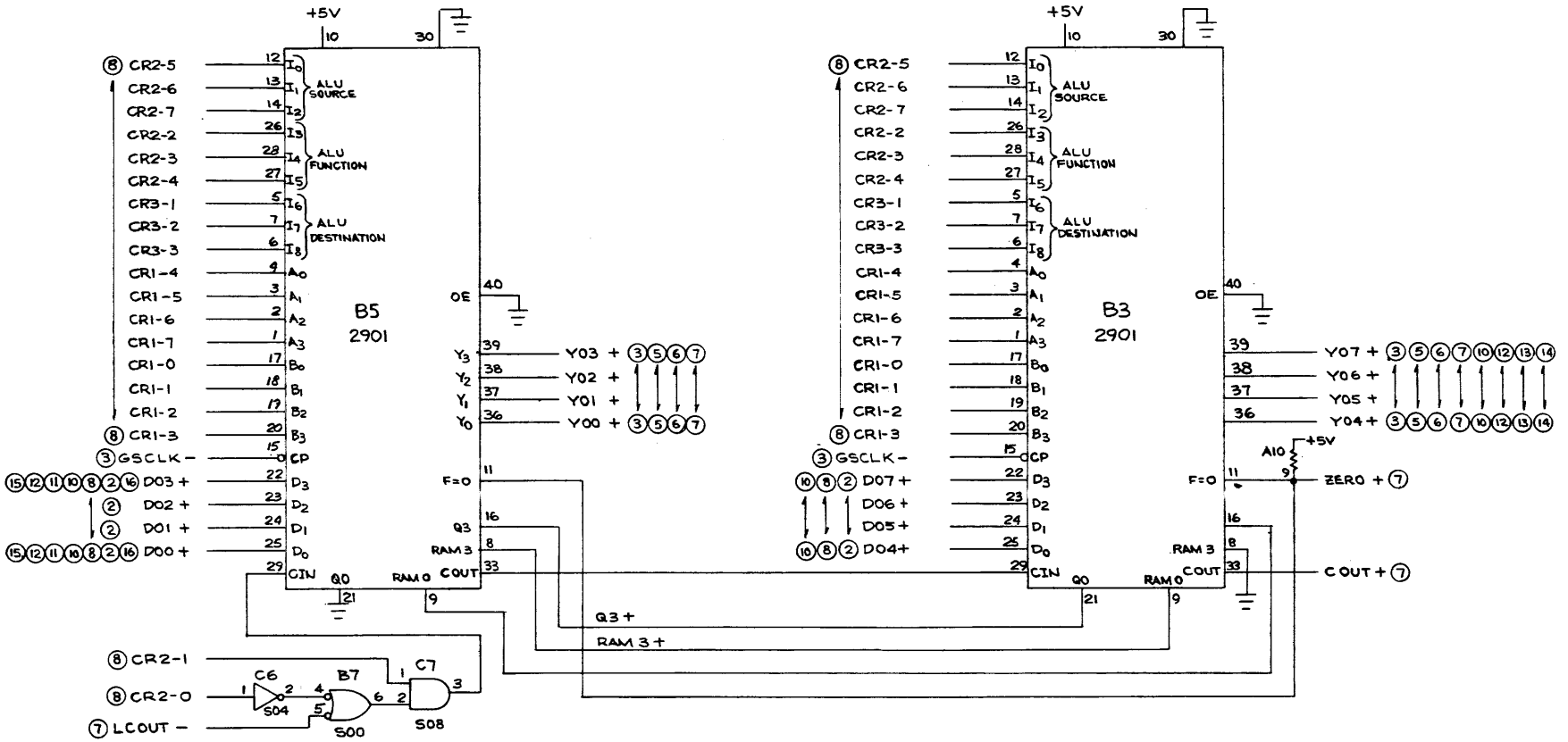

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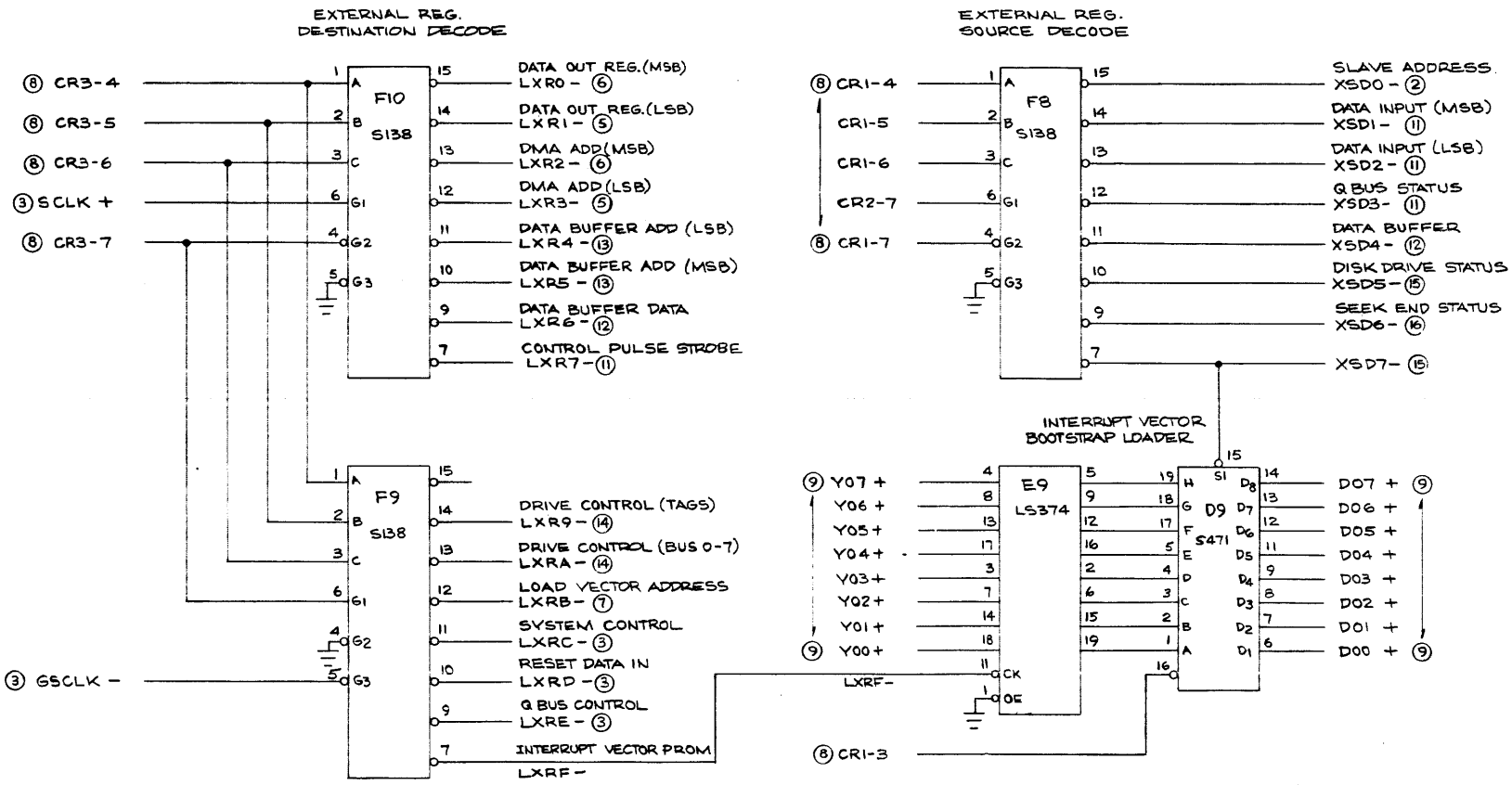

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LOGIC DIAGRAM		SHT 10 OF 16
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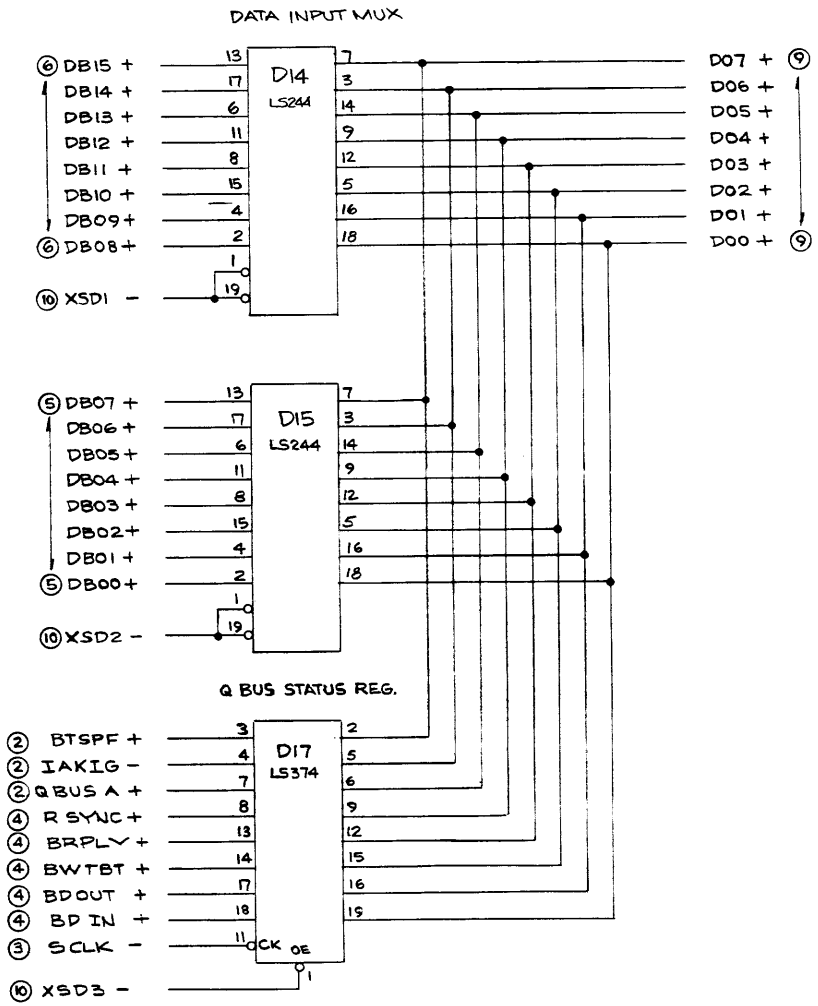

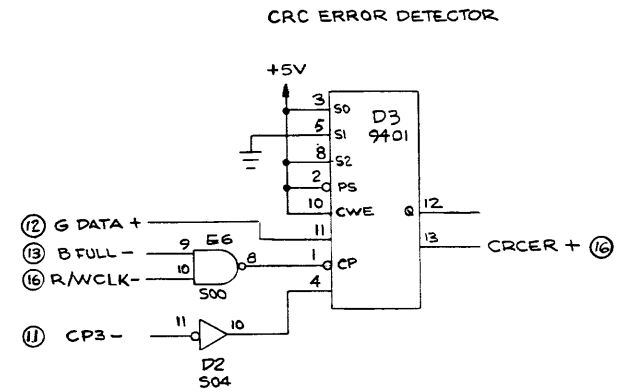

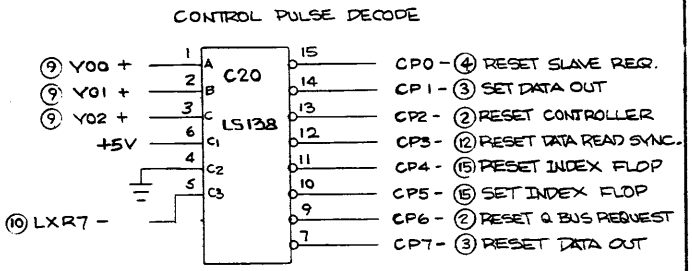

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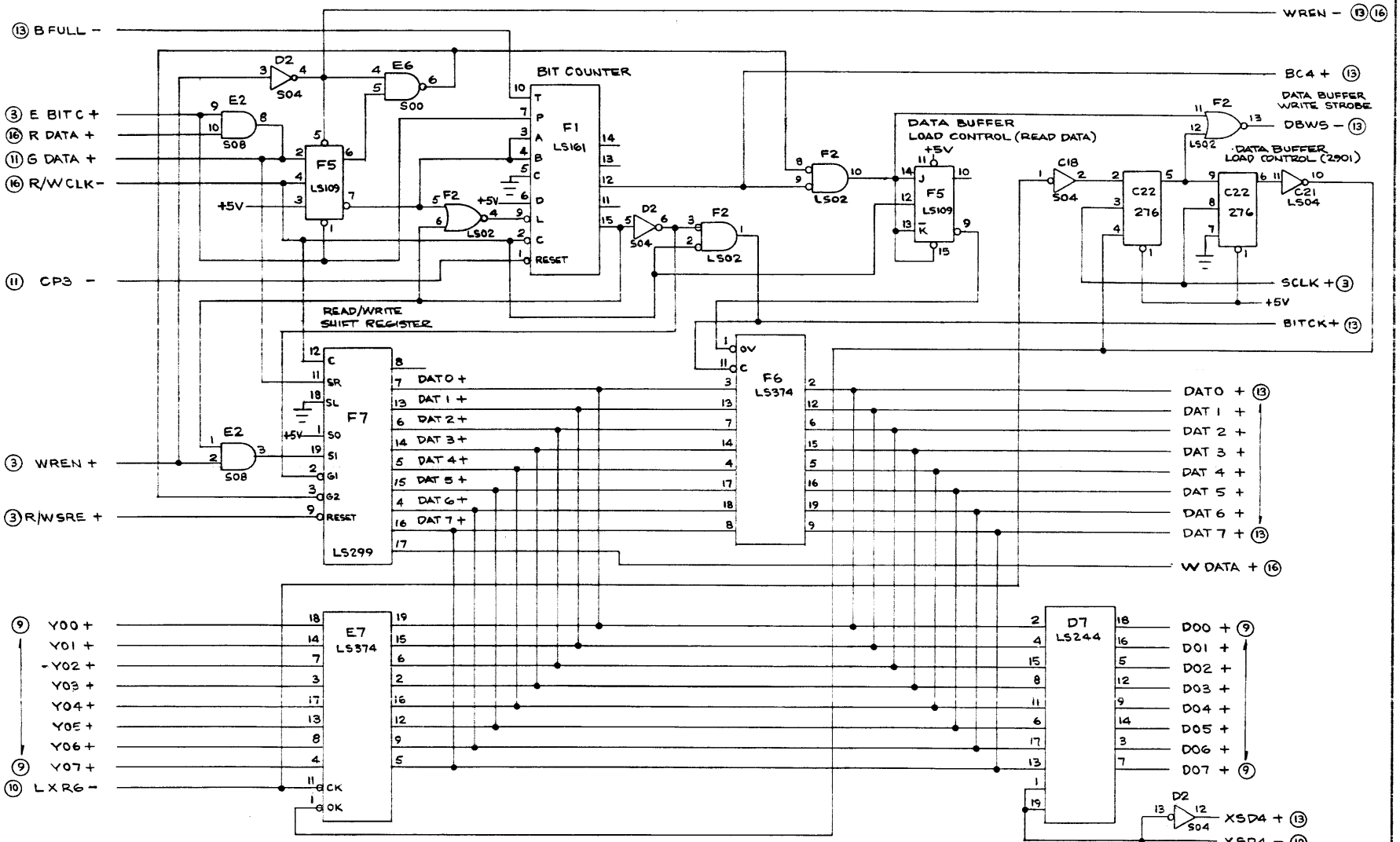

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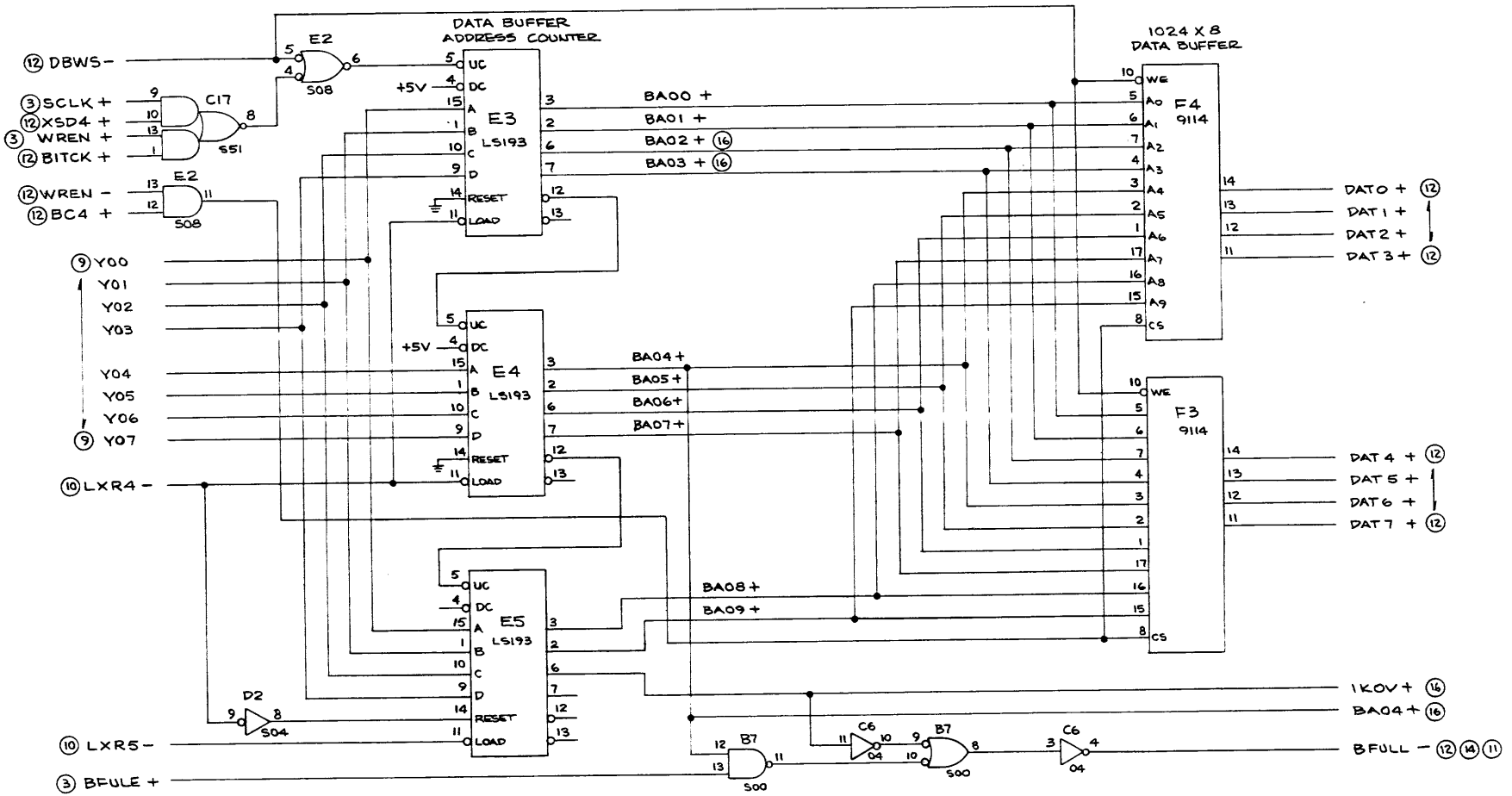

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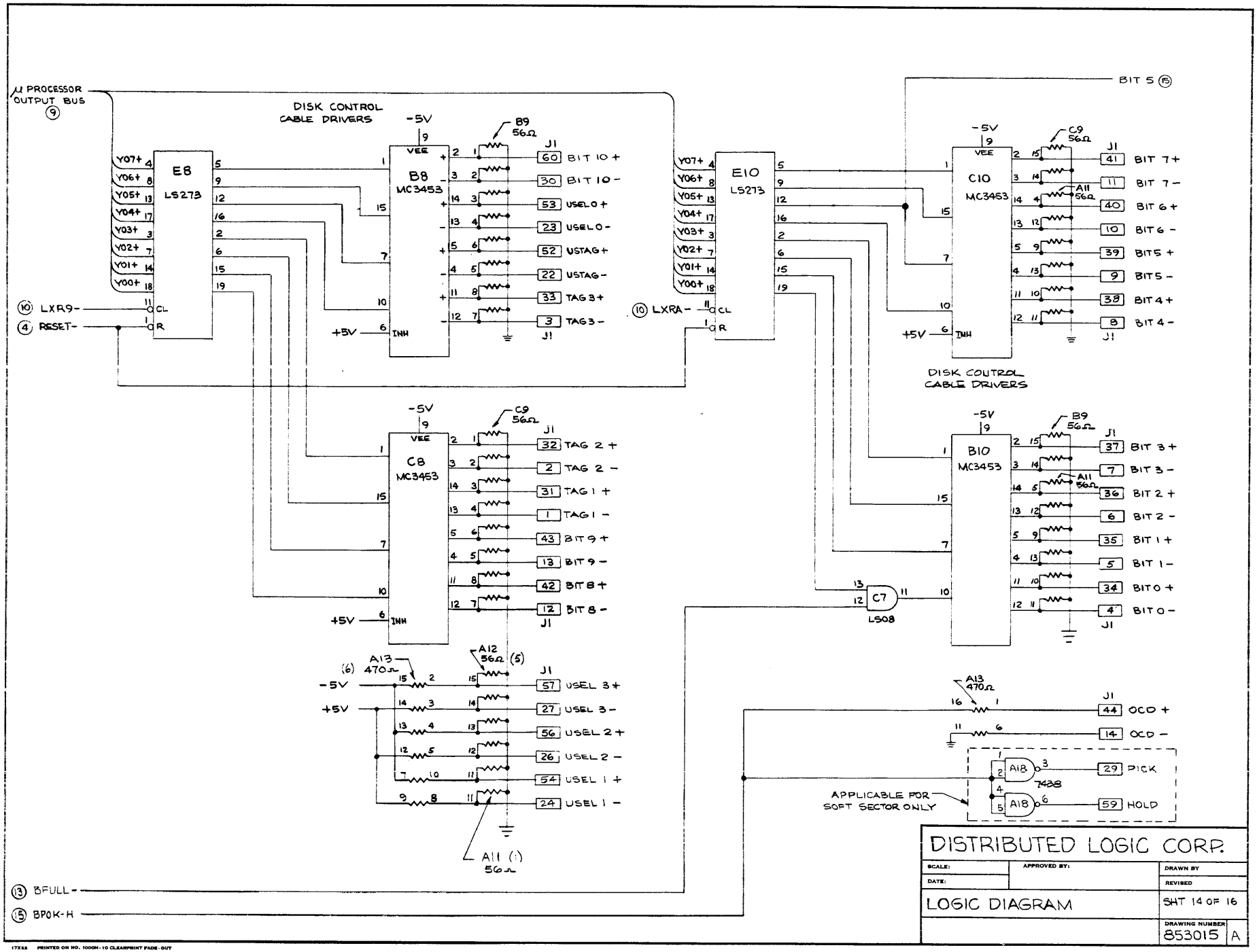

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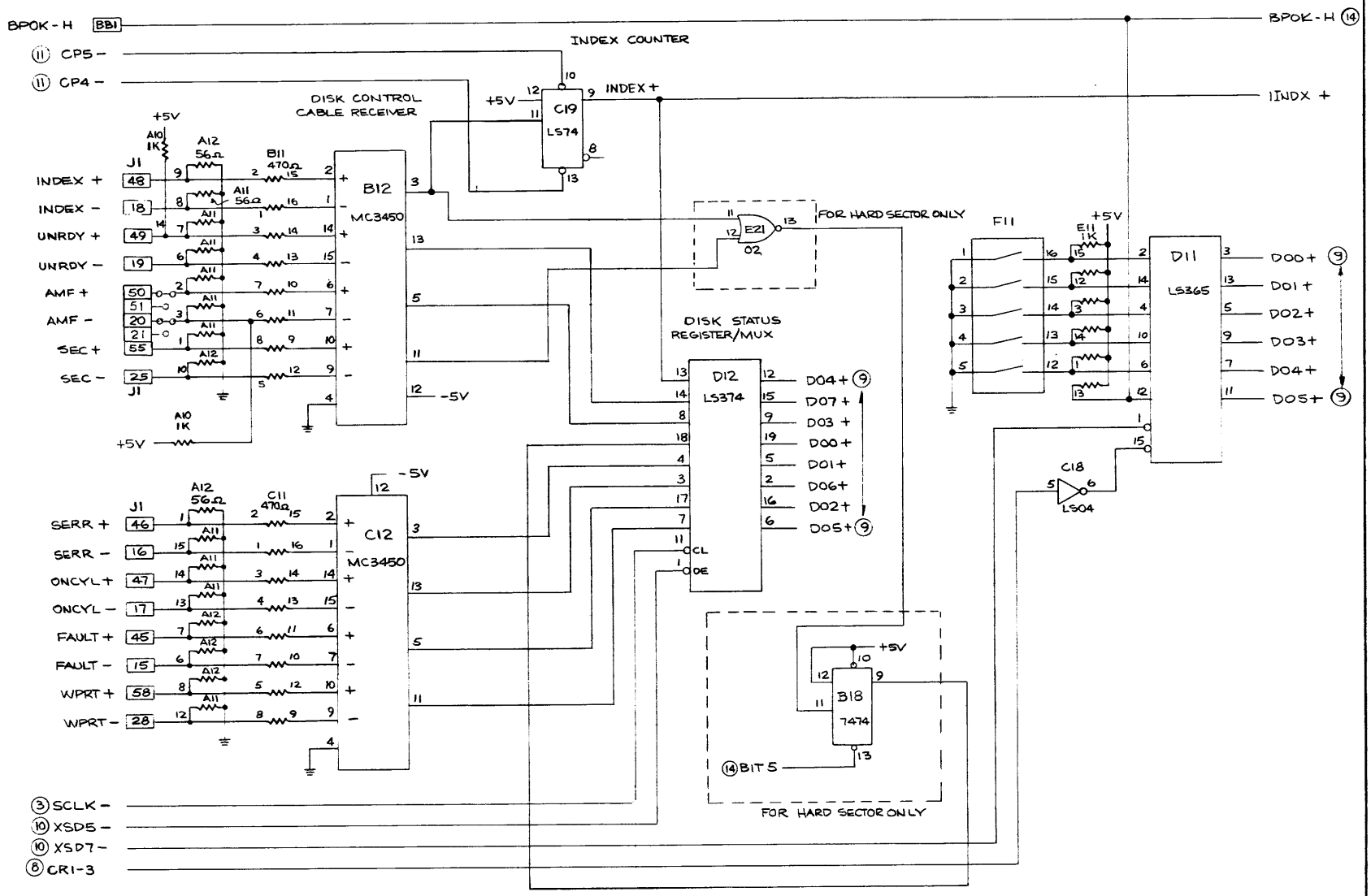

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