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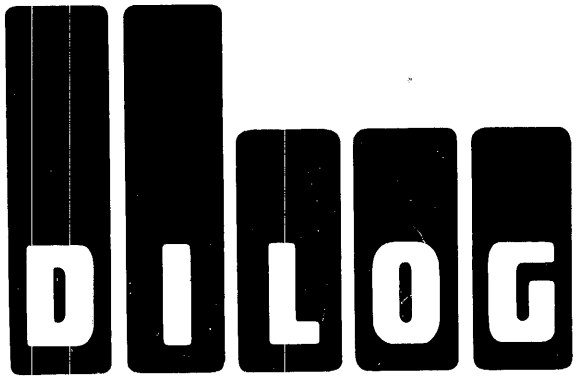
MODEL DU142
TAPE COUPLER
INSTRUCTION MANUAL



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MODEL DU142
MAGNETIC TAPE COUPLER
INSTRUCTION MANUAL

July 1987

DISTRIBUTED LOGIC CORPORATION
1555 S. Sinclair Street
P.O. Box 6270
Anaheim, California 92806
Telephone: (714) 937-5700
Telex: 6836051

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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

ILLUSTRATIONS

TABLES

SECTION 1
DESCRIPTION

INTRODUCTION

This manual defines the functional characteristics of the Model DU142 Magnetic Tape Coupler which, when used with any industry standard formatted magnetic tape drive, comprises a complete PDP-11 compatible nine-track magnetic tape subsystem. Magnetic tape drives from manufacturers other than DEC can be used while still retaining software and format compatibility with the DEC TS 11 and TU80 tape systems. The coupler is completely contained on one quad module that occupies one SPC slot in the backplane. Data transfers are via the NPR (direct memory access) facility of the UNIBUS. Transfer rates vary, depending upon the density and speed of the tape drives included in the system, between 10,000 and 645,000 characters per second, with burst rates to 800,000 bytes per second.

Up to four embedded-formatter tape drives or one embedded-formatter tape drive and three additional slave drives may be connected to the coupler. Drives can be streaming, cached, start/stop, or multimode.

The optimal usage of the coupler is in situations where nine-track, multidensity, 800/1600/6250 bpi tape recording capabilities are required; however, the coupler is compatible with Streamer, CacheTape, and GCR (6250 bpi) tape drives.

Long gap/normal gap switch selection is provided to permit use of standard DEC disc-backup software when the tape system includes the GCR Streaming drives.

The primary functions of the coupler in a magnetic tape subsystem are to buffer and interlock data and status transfers between the computer I/O bus and the tape formatter, and to translate CPU commands into tape formatter control signals such as Read, Read Reverse, Write, Write Tape Mark, Erase, etc. The primary function of the formatter is to control tape motion, establish data format, and perform error checking. The overall tape control function is a combination of the coupler functions, which are related to the computer, and the formatter functions, which are related to the tape drive.

A microprocessor is the sequence and timing center of the coupler. The control information is stored as firmware instructions in Read Only Memory (ROM) on the coupler board. One section of the ROM contains a diagnostic program that tests the functional operation of the coupler. This self test is performed automatically each time power is applied or whenever a diagnostic command is issued by the CPU. A green diagnostic indicator on the board lights if self test passes.

GENERAL DESCRIPTION

The coupler links a UNIBUS-based computer to from one through four formatted tape drives. The coupler performs the following major functions:

a. Buffers and interlocks data and status transfers across the computer I/O bus.

b. Translates computer program command words into control signals compatible with the tape drive formatter.

c. Buffers and interlocks data and status transfers between the coupler and the tape drive formatter.

The formatter in a system performs the following major functions:

a. Controls the timing and the format of data transfers to the tape drives.

b. Monitors the status of the tape drives and the quality of the data transferred onto the tape and presents this information to the coupler.

c. Generates all discrete control signals to the tape drives.

A coupler can link up to four tape drives to the computer in various configurations. Figure 1-1 illustrates a simplified system using four embedded-formatter tape drives; Figure 1-2 illustrates a simplified system using one embedded formatter and three slave tape drives.

UNIBUS Interface

Commands, data, and status transfers between the coupler and the computer are executed via the UNIBUS. Data and extended status words are transferred via the NPR facility of the UNIBUS;

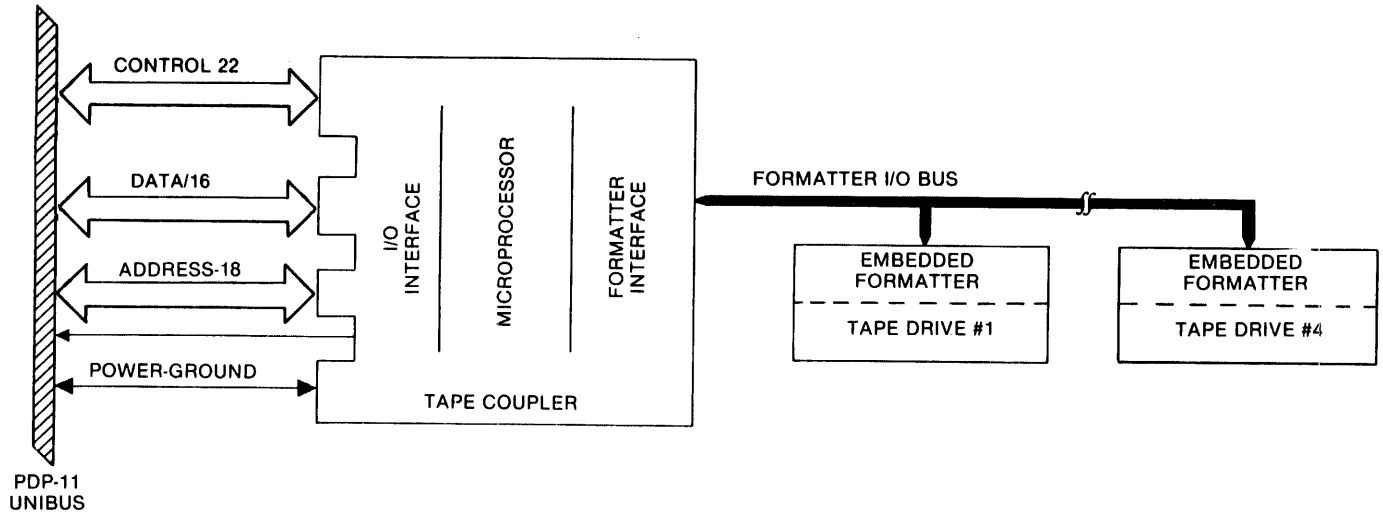


Figure 1-1. Tape System (Maximum Configuration) Four Embedded Formatter Tape Drives

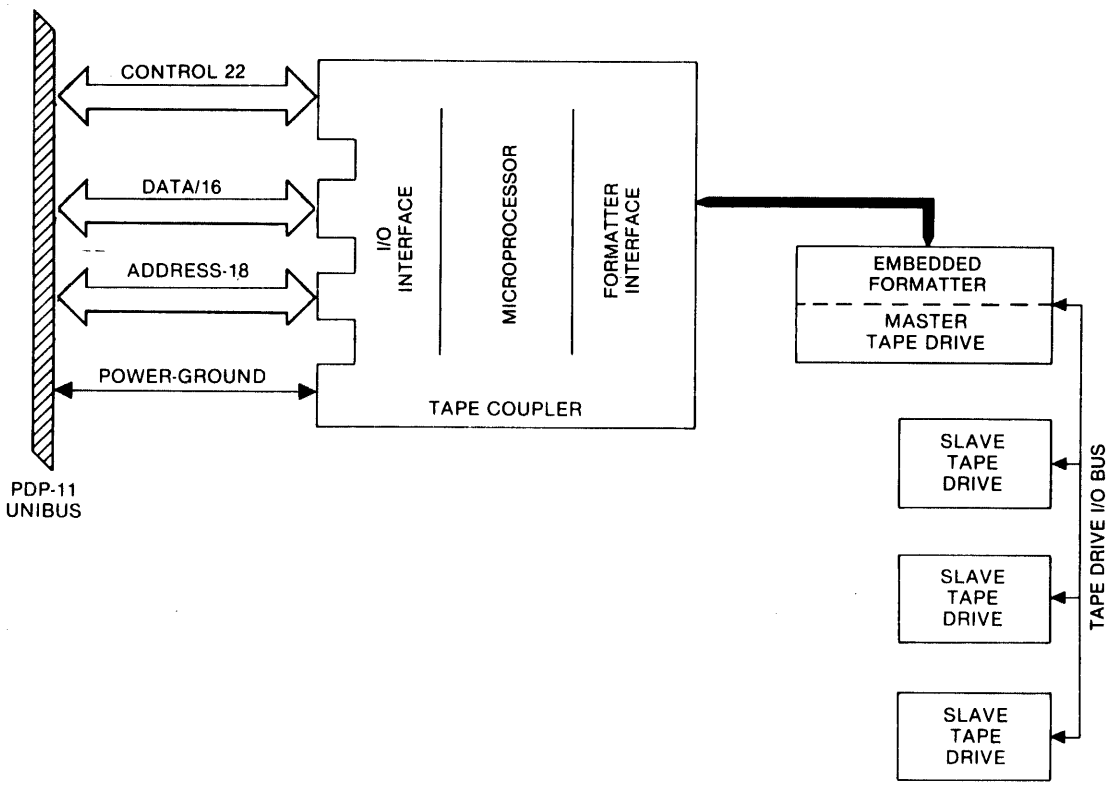


Figure 1-2. Tape System (Maximum Configuration) One Embedded Formatter Tape Drive with Three Slave Tape Drives

commands and basic status information are transferred via the programmed I/O facility of the UNIBUS under interrupt control. Data transfer rates are from 5,000 to 327,000 16-bit words per second, depending upon tape packing density and tape drive speed. Coupler/UNIBUS interface lines are listed in Table 1-1.

Interrupt

The interrupt vector address for drive zero is factory set (PROM programmed) to a standard address of 224_8, which is compatible with TS 11 software, and an alternate address of 274_8 (switch selectable). Floating interrupt vector addresses for addi-

Table 1-1. Coupler/UNIBUS Interface Lines

BUS PIN	MNEMONIC	DESCRIPTION
CA1	NPG INH	Non-Processor Grant In—Generated by the processor in response to NPR whenever the processor is not using the bus. NPG is daisy-chained through the devices connected to the bus and is received and regenerated by each device until it reaches the requested device.
CB1	NPG OUTH	Non-Processor Grant Out
CC1	PAL	Parity Bit A
CD2	D15L	Data Line Bit 15—These 16 lines DXXL, are used to transfer data and register control/status information to and from the controller.
CE2	D14L	Data Line Bit 14
CF2	D13L	Data Line Bit 13
CH1	D11L	Data Line Bit 11
CH2	D12L	Data Line Bit 12
CJ2	D10L	Data Line Bit 10
CK2	D09L	Data Line Bit 9
CL2	D08L	Data Line Bit 8
CM2	D07L	Data Line Bit 7
CN1	DCLOL	DC Power Low
CN2	D04L	Data Line Bit 4
CP2	D05L	Data Line Bit 5
CR2	D01L	Data Line Bit 1
CS1	PBL	Bus Parity Bit B
CS2	D00L	Data Line Bit 0
CT2	D03L	Data Line Bit 3
CU2	D02L	Data Line Bit 2
CV1	ACLOL	AC Power Low
CV2	D06L	Data Line Bit 6
DD2	BR7L	Bus Request 7—One of these lines BRXL, will be asserted by the controller to request control of the bus for the purpose of transferring data.
DE2	BR6L	Bus Request 6
DF2	BR5L	Bus Request 5
DH2	BR4L	Bus Request 4
DK2	BGI7H	Bus Grant Bit 7 In—These daisy-chained Bus Grant lines are asserted by the processor after completing the instruction in progress. Issued in response to the corresponding Bus Request line, the Bus Grant will be generated by each device until it reaches the requested device.
DL1	INITL	INITIALIZE—This signal is asserted by the processor to initialize or clear all devices connected to the bus.
DL2	BGO7H	Bus Grant Bit 7 Out
DM2	BGI6H	Bus Grant Bit 6 In
DN2	BGO6H	Bus Grant Bit 6 Out
DP2	BGI5H	Bus Grant Bit 5 In
DR2	BGO5H	Bus Grant Bit 5 Out
DS2	BGI4H	Bus Grant Bit 4 In
DT2	BGO4H	Bus Grant Bit 4 Out

Table 1.1 Coupler/UNIBUS Interface Lines (Continued)

BUS PIN	MNEMONIC	DESCRIPTION
EC1	A12L	Address Bit 12—These lines are the 18-bit address bus over which memory and peripheral register address information is communicated. Address information is placed on the bus by the bus master device and received and decoded by the selected slave device. The master device then either receives input data from, or outputs data to the addressed slave device (memory) over the data bus lines.
ED1	A17L	Address Bit 17
ED2	A15L	Address Bit 15
EE1	MSYNL	Master Sync—This control signal is issued by the master device to indicate that Address and Control information is present on the bus.
EE2	A16L	Address Bit 16
EF1	A02L	Address Bit 2
EH1	A01L	Address Bit 1
EH2	A00L	Address Bit 0
EJ1	SSYNL	Slave Sync—This control signal is issued by the slave device in response to the signals (MSYN or INTR) generated by the master device.
EK1	A14L	Address Bit 14
EK2	A13L	Address Bit 13
EL1	A11L	Address Bit 11
EN2	A08L	Address Bit 8
EP1	A10L	Address Bit 10
EP2	A07L	Address Bit 7
ER1	A09L	Address Bit 9
EU1	A06L	Address Bit 6
EU2	A04L	Address Bit 4
EV1	A05L	Address Bit 5
EV2	A03L	Address Bit 3
EJ2	C0L	Control Bit Zero—These two control lines are coded by the master device to describe the type of transfer: **C1 C0 OPERATION** 0 0 DATI—Data In (to master) 1 0 DATO—Data Out (from master) 1 1 DATOB—Data Out, Byte (from master)
EF2	C1L	Control Bit One
FD1	BBSYL	Bus Busy—This signal is asserted by the bus master to indicate the bus is in use. When BBSY goes false, control of the bus is passed to the new bus master.
FJ1	NPRL	Non-Processor Request—This signal is asserted by the controller to request control of the bus for the purpose of transferring data directly to or from memory.
FM1	INTRL	Interrupt Request—The controller asserts this signal after becoming bus master to indicate that the desired Interrupt Vector information is present on the bus.
FT2	SACKL	Selection Acknowledge—This signal is asserted by the controller in response to the processor's NPG or Bus Grant signal, indicating that control of the bus will pass to the controller when the current bus master completes its operation.

tional drives one, two, and three are switch selectable. The priority level is jumper selected at the factory to BR5. Interrupts are generated when processor attention is required—end of an operation or the occurrence of an error.

Formatter Interface

The coupler interfaces with the tape formatter through two 50-pin 3M connectors at the top center of the coupler board. The maximum cable length from the coupler to the formatter is 25 feet. Coupler-to-formatter interface lines are listed in Tables 1-2 and 1-3; Table 1-4 correlates the coupler connectors with connector labeling on the formatters from various manufacturers.

Table 1-2. Coupler Connector J1 to Formatter Interface Lines

J1 Signal	J1 Return	Mnemonic	Description
2	1	FFBY	Formatter Busy
4	3	FLWD	Last Word
6	5	FWD4	Write Data 4
8	7	FGO	Initiate Command
10	9	FWD0	Write Data 0
12	11	FWD1	Write Data 1
14	13		Not Used
16	15	FLOL	Load on Line
18	17	FREV	Reverse/Forward
20	19	FREW	Rewind
22	21	FWDP	Write Data Parity
24	23	FWD7	Write Data 7
26	25	FWD3	Write Data 3
28	27	FWD6	Write Data 6
30	29	FWD2	Write Data 2
32	31	FWD5	Write Data 5
34	33	FWRT	Write/Read
36	35	FRTH2 (FLGAP)	Read Threshold 2
38	37	FEDIT	Edit
40	39	FERASE	Erase
42	41	FWFM	Write File Mark
44	43	FRTH1 (SPARE)	Read Threshold 1
46	45	FTAD0	Transport Address 0
48	47	FRD2	Read Data 2
50	49	FRD3	Read Data 3

NOTE: ( ) Parentheses are applicable to streaming and GCR drives. Refer to Table 1-4 for Coupler-to-Formatter Connector Correlation.

Table 1-3. Coupler Connector J2 Formatter Interface Lines

J2 Signal	J2 Return	Mnemonic	Description
1		FRDP	Read Data Parity
2		FRD0	Read Data 0
3		FRD1	Read Data 1
4		FLDP	Load Point
6	5	FRD4	Read Data 4
8	7	FRD7	Read Data 7
10	9	FRD6	Read Data 5
12	11	FHER	Hard Error
14	13	FFMK	File Mark
16	15	FCCG/ID	Check Character Gate/ Identity
18	17	FFEN	Formatter Enable
20	19	FRD5	Read Data 5
22	21	FEOT	End of Tape
24	23	FOFL	Off Line
26	25	FNRZ (FGOR)	NRZI (GCR status)
28	27	FRDY	Ready
30	29	FRWD	Rewinding
32		FFPT	File Protect
34	33	FRSTR	Read Strobe
36	35	FDWDS	Demand Write Data Strobe
38	37	FDBY	Data Busy
40	39	(FHSPD)	High Speed Status
42	41	FCER	Corrected Error
44	43	FONL	On-Line
46	45	FTAD1	Transport Address 1
48	47	FFAD	Formatter Address
50	49	FDEN (FHISD)	Speed/Density Select

Note: ( ) Parentheses are applicable to streaming and GCR drives. Refer to Table 1-4 for Coupler-to-Formatter Connector Correlation.

Table 1-4. Coupler to Formatter Connection Correlation

Coupler Connector J1 to:		
Manufacturer	**Model**	**Connector**
CDC	Keystone II 92181	J4
CDC	Spirit 92180	J124
Cipher	F880, M89X, M99X	P1
	F100X, F900X	
	(Adapter required)	P4
Digi-Data	Formatted	JC
Fujitsu	M244X	JA
IDT	1012	J1
	1050	J124
Kennedy	6809 Streamer	J1
	Formatted	
Pertec	Formatted (Embedded)	P4
	External Formatter	
	(Adapter required)	P4
STC	2921/2	J7

Coupler Connector J2 to:		
Manufacturer	**Model**	**Connector**
CDC	Keystone 92181	J5
CDC	Spirit 92180	P125
Cipher	F880, M89X, M99X	P2
	F100X, F900X	
	(Adapter required)	P5
Digi-Data	Formatted	JD
Fujitsu	M244X	JB
IDT	1012	J2
	1050	J125
Kennedy	6809 Streamer	J1
	Formatted	J1
Pertec	Formatted (Embedded)	P5
	External Formatter	
	(Adapter required)	P5
STC	2921/2	J6

TAPE SYSTEM GENERAL SPECIFICATIONS*

Data Format

Industry standard non-return-to-zero (NRZ), Phase Encoded (PE) or Group Coded Recording (GCR) recording.

9 tracks

Recording densities:
800 characters per inch
1600 characters per inch
800/1600 characters per inch
800/1600/6250 characters per inch

Interrecord gap 0.50 inch min. (1600 cpi) or 0.3 inch min. (6250 cpi)

Tape parity marks: LPC, CRC, LRC (800 cpi)

Media Characteristics

Type

½" wide mylar base, oxide coated, magnetic tape.

Reel Size

7", 8½", or 10½" diameter tape reels containing 600, 1,200 and 2,400 feet of tape respectively.

Data Capacity (megabytes)

Assumes approximate 80% recording efficiency:

	800 CPI	1600 CPI	6250 CPI
600 Ft. =	5.75	11.5	
1,200 Ft. =	11.5	23.0	
2,400 Ft. =	22.0	44.0	172.0

Data Transfer Rate (Characters/Second)

	800 CPI	1600CPI	6250 CPI
12.5 ips =	10,000	20,000	
25.0 ips =	20,000	40,000	
37.5 ips =	30,000	60,000	
45.0 ips =	36,000	72,000	280,000
75.0 ips =	60,000	120,000	470,000
100.0 ips =	80,000	160,000	625,000
125.0 ips =	100,000	200,000	780,000

Register Address

Data/Address Buffer (TSDB/TSBA) 772 520*
Status (TSSR) 772 522*
*Addresses for Drive one; addresses for Drives two, three, four are Modulo four higher than next-lower numbered drive.

Computer I/O Interface

Interrupt Vector Address 224 or 274 (first drive); switch selectable from floating vector locations for drives two, three, four.
Priority Level BR5 (jumper selectable).
NPR data transfers.
Packet Processing type programming.
One bus load all lines.

Coupler/Formatter Interface

Coupler is compatible with formatters manufactured by CDC, Cipher, Digi-Data, Kennedy, Pertec, Ampex, Thorn Data, Fujitsu, STC.

Packaging

The coupler is completely contained on one quad module 10.44 inches (26.51cm) wide by 8.88 inches inches (22.55cm) inches deep.

Documentation

One Instruction Manual is supplied with the coupler.

Power

+5, ±.25 VDC at 4.0 amps, from computer backplane.

Environment

Operating temperature 50°F (10°C) to 140°F (60°C)
Operating humidity 10% to 95% non-condensing

Note

The quality of recording and reading information on magnetic tape is affected by temperature and humidity. The environment where the tape is used should be maintained within the following limits:
Temperature: 60°F (15°C) to 85°F (32°C)
Humidity: 20% to 80% non-condensing

Shipping Weight

Five pounds including documentation.

*Specifications subject to change without notice.

SECTION 2
INSTALLATION

INTRODUCTION

The padded shipping carton that contains the coupler board also contains an instruction manual and cable set to the formatter (if this option is exercised). The coupler is completely contained on the quad-size printed circuit board. The formatter and tape drive, if supplied, are contained in a separate shipping carton.

CAUTION

If damage to any of the components is noted, do not install! Immediately inform the carrier and Dilog.

Installation instructions for the formatted tape drive are contained in the tape drive manual.

Installation

To install the coupler module, proceed as follows:

CAUTION

Remove DC power from computer chassis before inserting or removing coupler module! Damage to the backplane assembly and the coupler module will occur if the coupler module is plugged in backwards!

1. Select the backplane Small Peripheral Controller (SPC) location into which the coupler is to be inserted. SPC locations are connectors C, D, E, and F of a UNIBUS backplane assembly.
2. To use the NPR facility required with the coupler, the backplane wiring of the SPC slot must be modified. The modification is as follows:

   Remove the wire on the connector C between A1 and B1 of the slot into which the coupler is to be plugged. This allows the non-processor grant priority line to be carried through the coupler.

   Note that any connector rows which do not have a card installed, must have a bus grant jumper card installed in the D slot to continue the bus grants to other devices in the UNIBUS.

   On older PDP-11 backplanes, the following additional wiring changes may be necessary if slot 1 AU1 is directly connected to slot 4 AU1 of the system unit into which the coupler is to be installed:

   A. Remove wire between 1 AU1 and 4 AU1.
   B. At the coupler slot, connect 1 AU1 to CA1 and 4 AU1 to CB1.
3. Perform jumpering/switch settings on coupler board as required; see "Configuring the Coupler" below.
4. Insert the coupler into the selected backplane position. Be sure the coupler is installed with the components facing Row One (1).

   The coupler module is equipped with handles on the side opposite the slot connectors. Gently position the module slot connectors into the backplane, then press until the module connectors are firmly seated into the backplane. Both handles must be pressed simultaneously. When removing the module, apply equal pulling pressure to both handles.
5. Feed the module connector end of the formater I/O ribbon cable set into the computer module area. Install the cable connectors into module connectors J1 and J2. Verify that the connector is firmly seated. Note that ribbon cable connectors are not keyed and, therefore, CAN be plugged in backwards. The connectors have a triangle marked on one end to identify Pin 1. These triangles on the cable and controller connectors MUST be lined up.
6. Connect the tape formatter end of the I/O ribbon cables to the formatter I/O connectors. Refer to Tables 1-2, 1-3, and 1-4.
7. If the formatter is equipped with a 100-pin connector, adapter Part No. ACC993A must be used to convert the 100-pin connector to two 50-pin connectors. If the formatter has a 72-pin connector, use Part No. ACC993B.

8. Apply power to the computer and verify that the green DIAGnostic LED indicator on the controller board is lighted. If the DIAG LED is not lighted, power is not applied to the coupler, the coupler board is bad, or the LED is bad.
9. Refer to the tape drive manual for operating instructions and apply power to the tape drive. Install a known good reel of tape on the tape drive and place the tape drive ON LINE.
10. Refer to the DEC software manual and run the diagnostics (see Diagnostics, p. 2-7).
11. The tape system is now ready for data transfer operations.

CONFIGURING THE COUPLER

The coupler board contains jumper locations, two board-edge switches, and a 10-switch pac that permit the user to configure a magnetic tape subsystem to meet specific requirements. Those configuration parameters that change infrequently are modified by jumpers; more frequently modified parameters are selected by switches. The coupler is shipped with jumpers installed and switches set to a so-called "default" configuration. The default configuration is that which is typical of TS 11/TU80 compatible installations.

Figure 2-1 illustrates the locations of the jumpers and switches. Since the jumper positions are infrequently changed, the default configuration jumpers are etched on the PC board. Thus to change jumpers,

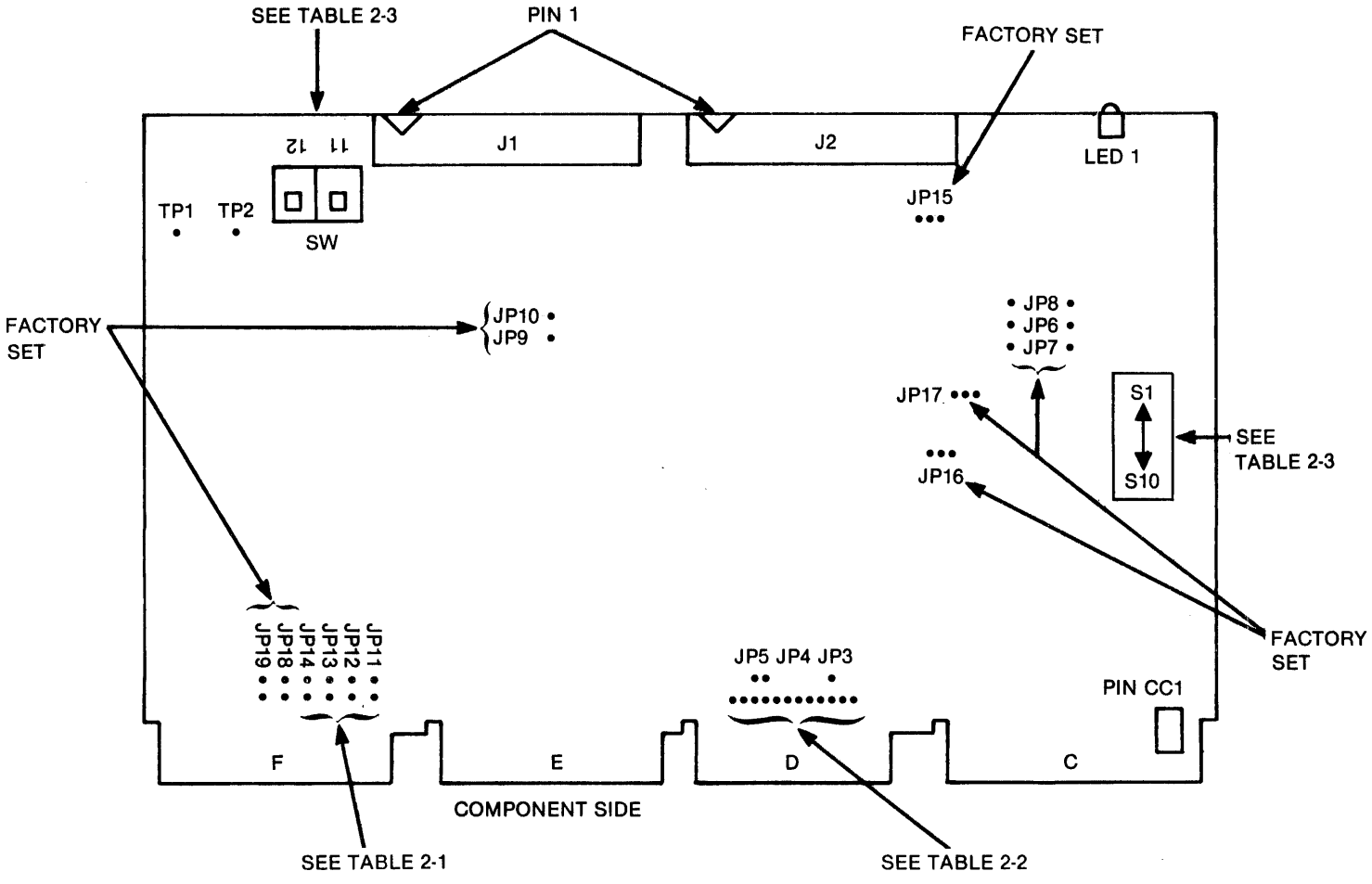


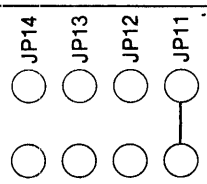
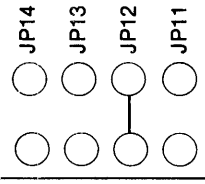
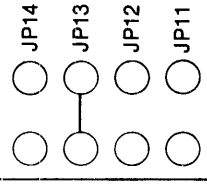
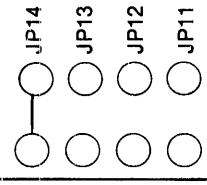
Figure 2-1. Coupler Configuration

board etch must be cut and jumpers added. The purpose of each jumper group and of the switches is as follows.

Controller Address Select Jumper

Jumper positions JP11, JP12, JP13, JP14 permit the address of the controller (Registers TSDB/TSDA and TSSR) to be changed. This is a useful feature if the computer system already has one TS 11 compatible tape system installed. Table 2-1 illustrates the jumper-position possibilities and resultant register addresses. Default settings are TSDB/TSDA = 772520 and TSSR = 772522 for logical unit zero.

Table 2-1. Controller Address Select

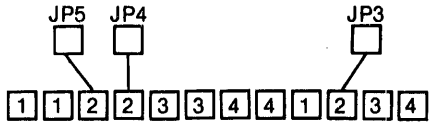
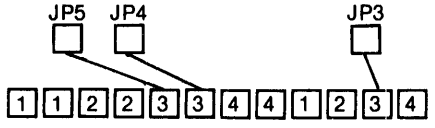
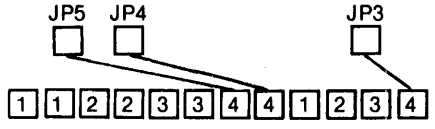
Register Addresses		Logical	Jumper	Jumper
TSDB/ TSBA	TSSR	Unit #	Installed	Configuration
772520	772522	0		
772524	772526	1	JP11	
772530	772532	2	(DEFAULT)	
772534	772536	3		
772720	772722	0		
772724	772726	1	JP12	
772730	772732	2		
772734	772736	3		
777360	777362	0		
777364	777366	1	JP13	
777370	777372	2		
777374	777376	3		
777420	777422	0		
777424	777426	1	JP14	
777430	777432	2		
777434	777436	3		

Instructions for changing addresses: Remove any existing jumpers (including the one etched on the back of the board for the default setting) and install jumper shown for desired address. Diagram reference is component side of board.

Priority Level Select Jumpers

Jumper positions JP3, JP4, JP5 permit the interrupt priority level to be changed. Table 2-2 illustrates the jumper-position possibilities and resultant priority levels selected. Default setting is BR5.

Table 2-2. Interrupt Priority Level Select

Jumper Configuration	Priority Level
	LEVEL 4
	LEVEL 5 (DEFAULT)
	LEVEL 6
	LEVEL 7

Instructions for changing priority level: Remove any existing jumpers (including those etched on back of board for the default setting) and install jumpers for desired priority level as shown. Diagram reference is component side of board.

Tape Drive Density and Speed Selection

Selection of tape drive density and speed is done manually at the tape drive.

Interrupt Vector, DMA Burst Size, Drive Quantity Select

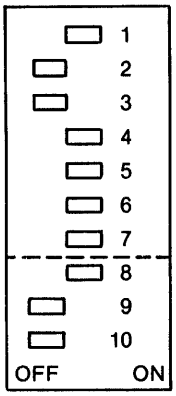
The switch pac in board location 20C contains 10 two-position switches. Switches S1 through S7 select the starting address of a floating interrupt vector table for logical drives after drive zero. Switch S8 sets the DMA burst size. Switches S9 and S10 are set to define the number of tape drives addressed through the coupler. Table 2-3 shows the purpose of each switch position.

Interrupt Vector Address

If only one drive is connected to the coupler, switches S1 through S7 need not be set to any specific value. The interrupt vector address for drive zero is jumper set to address 224_8 or address 274_8. JP1 installed is vector address 224_8 for Unit 0 (standard). JP1 cut is vector address 274_8 for Unit 0 (alternate). If the coupler connects with two or more drives, then switches S1-S7 must be set to one of the floating interrupt vector addresses (see Table 2-4).

Table 2-3. Interrupt Vector, DMA Burst Size, No. of Tape Drives, Long Gap Mode Switches

SW1 SWITCHES
(Standard switch settings are shown)



ON = 0
OFF = 1

INTERRUPT VECTOR							
SW1 Switch #	1	2	3	4	5	6	7
Bit Position	8	7	6	5	4	3	2
Standard*	ON	OFF	OFF	ON	ON	ON	ON
Octal	3			0			0
*Standard switch settings show start of floating vectors.							

Logical Unit #	Interrupt Vector
0	Switch SW 12 Selectable Factory set at 224 (SW12 OFF) SW12 ON = 274
1	SW1 Switches (Floating)
2	SW1 Switches + #4 (Floating)
3	SW1 Switches + #8 (Floating)

#Logical Units	1 (Std)	2	3	4
Switch SW1-9	OFF	OFF	ON	ON
Switch SW1-10	OFF	ON	OFF	ON

DMA Burst Size	2 Word	4 Word
Switch SW1-8	ON Std on PDP	OFF Std on RX11/780

Long Gap Mode	Disabled	Enabled
Switch SW11	OFF	ON

Note that if a third or fourth drive is added to the coupler, interrupt vector addresses for these drives are automatically assigned when switches S9 and S10 are set correctly. The addresses of the third and fourth drives are displaced four and eight addresses respectively above the address of the second drive. For example, if floating vector address 300_8 was assigned to the second drive (as shown in Table 2-4), the vector address of the third drive would be 304_8, and for the fourth drive the address would be 310_8. The default value is switch set to 300_8.

DMA Burst Size

Switch S8 controls the number of data words transferred between memory and the coupler during each NPR transfer. Either two (S8 ON) or four (S8 OFF) word transfers can be selected; two are standard for PDP-11 CPUs and the smaller VAXes; four are standard for the VAX-11/780. The default value is S8 ON.

Number of Tape Drives

Switches S9 and S10 must be set to define the number of logical drives addressed by the coupler. The default values are S9 and S10 OFF (one drive).

Floating Vector Addresses

A floating vector convention is used for communications and other devices that interface with the PDP-11. These vector addresses are assigned in order starting at 300_8 and proceeding upwards to 774_8. Table 2-4 shows the assigned sequence. It can be seen that the first vector address, 300_8, is assigned to the first DC-11 in the system. If another DC-11 is used, it would then be assigned vector address 310_8, etc. When the vector addresses have been assigned for all the DC 11s (up to a maximum of 32), addresses are then assigned consecutively to each unit of the next highest-ranked device (KL 11, DP11, or DM 11, etc.), then to the other devices in

Table 2-4. Priority Ranking for Floating Vectors (starting at 300_8 and proceeding upwards)

Rank	Option	Decimal Size (words)	Octal Modulus (address)
1	DC11	4	10
1	TU58	4	10
2	KL11 (extra)	4	10
2	DL11-A (extra)	4	10
2	DL11-B (extra)	4	10
3	DP11	4	10
4	DM11-A	4	10
5	DN11	2	4
6	DM11-BB	2	4
7	DH11 modem control	2	4
8	DR11-A	4	10
9	DR11-C	4	10
10	PA611 (reader + punch)	8	10
11	LPD11	4	10
12	DT11	4	10
13	DX11	4	10
14	DL11-C	4	10
14	DL11-D	4	10
14	DL11-E	4	10
15	DJ11	4	10
16	DH11	4	10
17	GT40	8	10
17	VSV11	8	10
18	LPS11	12	10
19	DQ11	4	10
20	KW11-W	4	10
21	DU11	4	10
22	DUP11	4	10
23	DV11 + modem control	6	10
24	LK11-A	4	10
25	DWUN	4	10
26	DMC11	4	10
26	DMR11	4	10 (DMC before DMR)
27	DZ11	4	10
28	KMC11	4	10
29	LPP11	4	10
30	VMV21	4	10
31	VMV31	4	10
32	VTV01	4	10
33	DWR70	4	10
34	RL11/RLV11	2	4 (after the first)
35	RX02	2	4
36	TS11	2	4 (after the first)
37	LPA11-K	4	10
38	IP11/IP300	2	4
39	KW11-C	4	10
40	RX11	2	4 (after the first)
41	DR11-W	2	4
42	DR11-B	2	4 (after the first)

accordance with the priority ranking. The TS 11 has a rank of 36.

Streaming Drive Long Gap Select Switch

Switch S11 allows the operator to select "long gap" mode for PE or GCR streaming drives equipped with this option. The default switch setting is OFF. S11 ON selects the long gap mode.

Note

DEC always selects the long gap mode for their TU80 streaming tape subsystem. This 1600 cpi PE streamer operates at 100 ips in the high speed mode. The long gap mode can reduce the amount of data written on tape, depending on record size, software instruction times, tape drive Long Gap option type (fixed gap, variable gap), etc. Tapes with either normal or long gaps can be read regardless of the setting of S11.

The long gap mode should be selected when using any DEC disc backup software with a streaming tape drive. Selecting long gap mode does not mean that all inter-record gaps (IRG) written on tape will be long; the gap length is primarily a function of software instruction times. Tapes with either normal or long gaps can be read regardless of the setting of S11. Note that start/stop or cached tape drives do not have this option, thus, the S11 switch setting is ignored.

The long gap mode merely extends the "reinstruct time" window of the streamer after the end of each record. This delays triggering the repositioning cycle longer than normal. Note that if the software does not provide sequential write instructions within the streamer reinstruct time, the streamer will enter a repositioning cycle which can take over one second. Table 2-5 compares normal and long gap reinstruct times for various models of PE and GCR tape drives.

If sequential software write commands occur within the normal reinstruct time window, a normal IRG will be erased. If sequential software write commands occur after the normal reinstruct time, but before the end of the long gap window, a longer IRG will be written but the drive will not enter the reposition cycle. If a sequential write command does not occur until after the long gap window time out, the repositioning cycle time penalty is invoked before a new write command can be accepted.

Therefore, the long gap mode is appropriate for two cases:

A. When streaming disc backup software usually generates the next write instruction within the normal reinstruct time window, but occasionally is delayed due to missing a disc rotation (seek command). This results in negligible loss of tape capacity because only a small percentage of tape records are followed by a longer than normal IRG.

B. When minimum time to perform a disc backup is more important than tape capacity, and the software usually cannot meet the normal reinstruct time window requirements,

Table 2-5. Normal/Long Gap Reinstruct Time Comparisons

DRIVE	SPEED IPS	FORMAT	PE GAP (ms)				GCR GAP (ms)			
			NORMAL		LONG		NORMAL		LONG	
			WR	RD	WR	RD	WR	RD	WR	RD
Cipher F880	100	PE	3	4	7	8				
CDC 92181	100	PE	3.5	12	9.5	12				
CDC 92185	75	PE/GCR	5.5	15.5	13.5	15.5	1.5	3	5.5	7.5
DEC TU80	100	PE			9.5	12				
FUJ. M2442A	100	PE/GCR	4	5.5	10	11.5	1	2.5	4	5.5
STC 2922	100	PE/GCR	3.5	5	9.5	11	0.5	2	6.5	8

but does fall within the long gap reinstruct time requirements. Even though longer than normal gaps are erased between records (reducing tape capacity), a high-speed streaming mode will be maintained to guarantee disc backup. If large record sizes are written to tape, the ratio of record size to blank tape will be such that good tape capacity will still be realized.

There is a major difference in reinstruct time between GCR and PE streaming tape drives even when operated at the same tape speed (see Table 2-5). This is because of the difference in the IRG size between the two formats: PE IRG size is 0.6 inch: GCR IRG size is 0.3 inch. Typical reinstruct times (normal gap) for 100 ips streamers in the write mode are 3.5 milliseconds in PE and 0.5 to 1.0 millisecond in GCR. Read mode reinstruct times are slightly longer because the physical distance between the write/read heads does not have to be subtracted from the gap spacing as is required for write mode calculations. This is because read-after-write parity checking is required in the write mode.

Since all DEC streaming software is designed for the TU80 PE streaming tape drive, which always has long gap mode selected, the long gap mode is recommended for both PE and GCR streamers when using DEC software. To re-emphasize, streaming performance is dependent upon software response time between records—not hardware response time.

Alternate Interrupt Vector Switch S12

Switch S12 allows the operator to select an alternate interrupt vector for logical tape unit zero. Switch S12 ON selects interrupt address vector 274_8 The default switch position is OFF, which selects standard interrupt address vector 224_8.

DIAGNOSTICS

The DEC software diagnostics and "exerciser" programs that can be run with the coupler depend upon the computer and software operating system being used.

Note

Some of the functional tests report invalid errors when cached tape drives are used with the coupler. These errors occur in subtests that involve specific time delay measurements and simulate detection of blank tape. For example, after erasing a long gap on tape, an OPI error is expected when the tape is re-read. The OPI error will not be generated when testing a cached tape subsystem. The known errors caused by cached tape subsystems are noted where appropriate in the following text.

VAX:

A. EVMAA TS11 Data Reliability (see note 1)
B. EVMBD TU80 Functional Test #1
C. EVMBE TU80 Functional Test #2

PDP-11 XXDP+:

A. CZTUVBO TU80 Data Reliability
B. CZTUVAO TU80 (no drive)
C. CZTUXAO TU80 Functional Test #1 (see note 2)
D. CZTUYAO TU80 Functional Test #2 (see note 3)
E. CZTUZAO TU80 Functional Test #3 (see note 4)
F. CZTSCHCO TS11 Data Reliability
G. CXTSAAO TS11 DEC/X11 System Exerciser

OPERATING SYSTEM SOFTWARE

Most DEC operating system software packages include some form of concurrent DMA I/O exerciser tests. In some cases these tests can be run even while the operating system is on line—as long as the peripherals to be tested are either not in use or, like discs, can have a reserved area assigned.

These exercisers are typically called UETP (User Environment Test Package), IOX (Input/Output Exerciser), or MTEXER (Magnetic Tape Exerciser).

The best way to run these exerciser tests is to activate testing on more than one DMA device simultaneously (such as disc and magnetic tape). In this way concurrent DMA operations are also tested.

NOTES:

1. *Reports two "Data Compare Errors" when run on the VAX-11/780. However, this is normal even for the DEC TS 11. If EVMAA is run in the on-line mode, no errors should be reported.*

2. *CZTUXAO diagnostic test 4 verifies that the coupler returns to Non Existent Memory (NXM) status for DMA memory transfer attempts into the upper 8K byte I/O page.*

   Two invalid error messages occur if, during DMA transfers, computer memory increments across the upper 8K byte I/O page memory boundary or the coupler subsystem contains a cache tape that has a limit on the maximum record size.

   The first error typically occurs when more than 248K bytes of memory is installed and the upper 8K bytes have not been configured to be disabled; this allows DMA transfers to overlay the I/O page. If the following error occurs, check the memory configuration options:

   A. *Error 418, test 4, subtest 4, PC 037254 Error Message, "TSSR not correct after WRITE command reject due to NXM."*

   The second errorr is due to the cache tape drive's limitation on maximum record size. The cache tape can be internally configured to define the maximum record size. Typical configuratons are between 16K and 24K bytes. The diagnostic program causes the coupler to advance through DMA memory addresses until either addresses past installed memory are issued or addresses are issued into the I/O page. This should cause NXM status to be reported by the coupler. The diagnostic does this by writing several large records (approximately 62K bytes), which causes the coupler to advance through computer memory until available memory is exceeded and NXM is generated. Unfortunately, the cache tape goes into a "drive fault" mode if the configured maximum record size is exceeded. This results in the following error:

   A. *Error 421, test 4, substest 5, PC 037520 Error Message, "TSSR not correct after WRITE to nonexistent memory."*

   The following software patch will cause this diagnostic test to operate correctly with a cache tape:

   A. *Address = 37412: was = 0, patch to = 1*

3. *Test 3, subtest 5 reports invalid error 355 at PC 055434 if cache tape is used with the coupler. The error message is, "write data retries erase tape not long enough."*

4. *Test 4, subtest 3 reports invalid errors 427/428 at PC 050772, 051026, 050772 if cache tape is used with the coupler. The error messages are as follows:*

   A. *Erase failed to clear tape (ERASE) properly.*

   B. *OPI bit (XST3) failed to set.*

   Test 5, subtest 1 reports invalid errors 517/526 at PC 054200, 055014 if cache tape is used with the coupler. The error message is, "unable to clear EOT indication, bit 0 (XST0)."

SECTION 3
OPERATION

INTRODUCTION

Prior to operating the system, the instruction manual sections describing the controls and indicators on the tape drive and the procedures for mounting and removing tape reels should be read. To prevent loss of data or damage to the magnetic tape, the following precautions should be observed:

a. Always handle a tape reel by the hub hole. Squeezing the reel flanges can cause damage to the tape edges when winding or unwinding tape.

b. Never touch the portion of tape between the BOT and EOT markers. Oils from fingers attract dust and dirt. Do not allow the end of the tape to drag on the floor.

c. Never use a contaminated reel of tape. This spreads dirt to clean tape reels and can affect tape drive operation.

d. Always store tape reels inside their containers. Keep empty containers closed so dust and dirt cannot get inside.

e. Inspect tapes, reels, and containers for dust and dirt. Replace take-up reels that are old or damaged.

f. Do not smoke near the tape drive or tape storage area. Tobacco smoke and ash are especially damaging to tape.

g. Do not place the tape drive near a line printer or other device that produces paper dust.

h. Clean the tape path frequently.

Note that tape drives permit off-line or on-line operation. The off-line mode is controlled by switches on the tape drive. The on-line mode is controlled by programmed commands from the computer via the coupler and formatter. When system operation is desired, be sure the tape drive ON-LINE indicator is lit. On-line operation is a function of program commands and is described in Section 4 of this manual.

Tape Format

For detailed information on tape format characteristics see the formatter and tape drive manuals.

Booting From Magnetic Tapes

1. Place the tape transport "ON LINE" and position the tape at "Beginning of Tape."
2. If the CPU is equipped with a TS 11 hardware boostrap, simply type "MS0" Carriage Return <CR>. If no hardware bootstrap is installed, boot as shown in Table 3-1.

Table 3-1. TS11 / TU80 / TSV05 Bootstrap Routine

Address	Data		Code			
			TSBA	=	172520	TS11 ADDRESS REGISTER ADDRESS
			TSSR	=	172522	TS11 STATUS REGISTER ADDRESS
001000	012700	172520	START:	MOV	#TSBA, R0	GET ADDRESS OF TSBA INTO R0
001004	012701	172522		MOV	#TSSR, R1	GET ADDRESS OF TSSR INTO R1
001010	005011			CLR	(R1)	INIT AND REWIND TAPE
001012	105711			TSTB	(R1)	TEST IF 'SSR' IS SET
001014	100376			BPL	.−2	AND WAIT UNTIL IT IS
001016	012710	001066′		MOV	#PKT1, (R0)	ISSUE SET-CHARACTERISTICS COMMAND
001022	105711			TSTB	(R1)	TEST IF 'SSR' IS SET
001024	100376			BPL	.−2	AND WAIT UNTIL IT IS
001026	012710	001106′		MOV	#PKT2, (R0)	ISSUE READ OF FIRST RECORD (MS HEADER FILE)
001032	105711			TSTB	(R1)	TEST IF 'SSR' IS SET
001034	100376			BPL	.−2	AND WAIT UNTIL IT IS
001036	012710	001106′		MOV	#PKT2, (R0)	ISSUE READ OF SECOND RECORD ('MS:' BOOT)
001042	105711			TSTB	(R1)	TEST IF 'SSR' IS SET
001044	100376			BPL	.−2	AND WAIT UNTIL IT IS
001046	005711			TST	(R1)	ANY ERRORS ? ? ? ?
001050	100422			BMI	HLT	HALT IN FRONT OF MESSAGE IF ERRORS
001052	012704	001102′		MOV	#NUM + 2, R4	ADDRESS OF 'NUM' + 20 TO REG. 4
001056	005000			CLR	R0	0→R0 (UNIT #0)
001060	005007			CLR	PC	RESUME EXECUTION AT ZERO IF NO ERRORS
001062	046523		NUM:	046523		MS (ASCII) = 046523 (OCTAL)
				SET-CHARACTERISTICS PACKET		
001064	140004		PKT1:	140004		COMMAND (SET CHARACTERISTICS)
001066	001074′			PK		LS ADDRESS OF PACKET
001070	000000			0		MS ADDRESS OF PACKET
001072	000010			8.		NUMBER OF BYTES IN PACKET
001074	001116′		PK:	MES		LS ADDRESS OF MESSAGE PACKET (END STATUS)
001076	000000			0		MS ADDRESS OF MESSAGE PACKET
001100	000016			14.		NUMBER OF BYTES IN PACKET
001102	000000			0		
				READ-DATA PACKET		
001104	140001		PKT2:	140001		COMMAND (READ 1 RECORD)
001106	000000			0		LS BUFFER START ADDRESS
001110	000000			0		MS BUFFER START ADDRESS
001112	001000			512.		NUMBER OF BYTES
001114	000000		HLT:	HALT		
001116			MES:			START OF 7 WORD MESSAGE PACKET (END STATUS)

SECTION 4
PROGRAMMING

PROGRAMMING DEFINITIONS

FUNCTION: The expected activity of the tape system (read, write, rewind).

COMMAND: The instruction which initiates a function.

INSTRUCTION: One or more orders executed in a prescribed sequence that cause a function to be performed.

ADDRESS: The binary code placed on the A00L-A17L lines by the bus master to select a register in a slave device. Note that "register" can be either discrete elements (flip flops) or memory elements (core, solid state RAM or ROM). When addressing devices other than computer internal memory, i.e., peripheral device registers, the upper 8K bytes of address space is used.

REGISTER: An associated group of memory elements that react to a single address and store information (status, control, data) for use by other assemblies of the total computer system.

PROGRAM SEQUENCES

Commands, data, and status are sent between the coupler and the processor (CPU) in groups of bytes called "packets." There are four types of packets:

1. Command packet
2. Data packet
3. Characteristics packet
4. Message packet (also called end packet). A summary is shown at the end of this section.

The packets are established in main memory by the CPU. Typically there are two main memory packet (buffer) areas: Data buffers and control/status buffers. Both areas can be controlled by either the CPU or the coupler. The buffer contents and sources are as follows:

Data Buffer	Packet Buffer	Size	Source
	command	8 bytes	CPU
data from tape		1 byte to 65 Kbytes	Coupler
data to tape		1 byte to 65 Kbytes	CPU
	set characteristics	8 bytes	CPU
	message	14 bytes	Coupler

This packet technique for communicating between the CPU and the coupler improves computer system efficiency by reducing the number of information transfers to and from the tape system under processor control; in addition to data transfers, status and command information is transferred via the NPR facility.

The coupler has two program-accessible registers: the Status register (TSSR) and the combination Bus Address/Data Buffer register (TSBA/TSDB). As mentioned, the additional registers required for proper control and monitoring of the operation of a tape drive are contained in main memory. For example, five additional status words which reflect the state of the tape subsystem are stored in a main memory location by the coupler.

A typical Read or Write command sequence is as follows:

1. CPU reads the status register (TSSR).
2. CPU loads (writes) the Data Buffer register (TSDB) with the starting address of the command packet, which is then shifted and loaded into the coupler's TSBA register.
3. Coupler's Bus Address register (TSBA) contents access a command word, which is typically "Set Characteristics." Note that the Set Characteristis command packet comprises four successive memory locations (eight bytes) that contain (see Figure 4-2):
   A. Command words
   B. Least significant bits of the characteristics packet address
   C. Most significant bits of the characteristics packet address
   D. Byte count of the characteristics packet

   The contents of the Set Characteristics packet are now accessed by the coupler. The principle purpose of executing this command is to get the starting address of the End Message packet. Upon conclusion of a read or write operation, the message packet locations are loaded with extended status words by the coupler.

4. CPU loads the Data Buffer register (TSDB) with the starting address of the next command packet.

5. The coupler TSBA contents access the next command word—a read or a write command. Read/Write command packets comprise four successive memory locations (eight bytes) that contain (see Figure 4-1):

   A. Command word

   B. Least significant bits of the starting location in memory where data is to be read from (write command) or written to (read command)

   C. Most significant byte of the starting memory location

   D. Number of bytes to be transferred (byte count)

6. The coupler as bus master now begins the transfer of data between main memory and the selected tape drive.

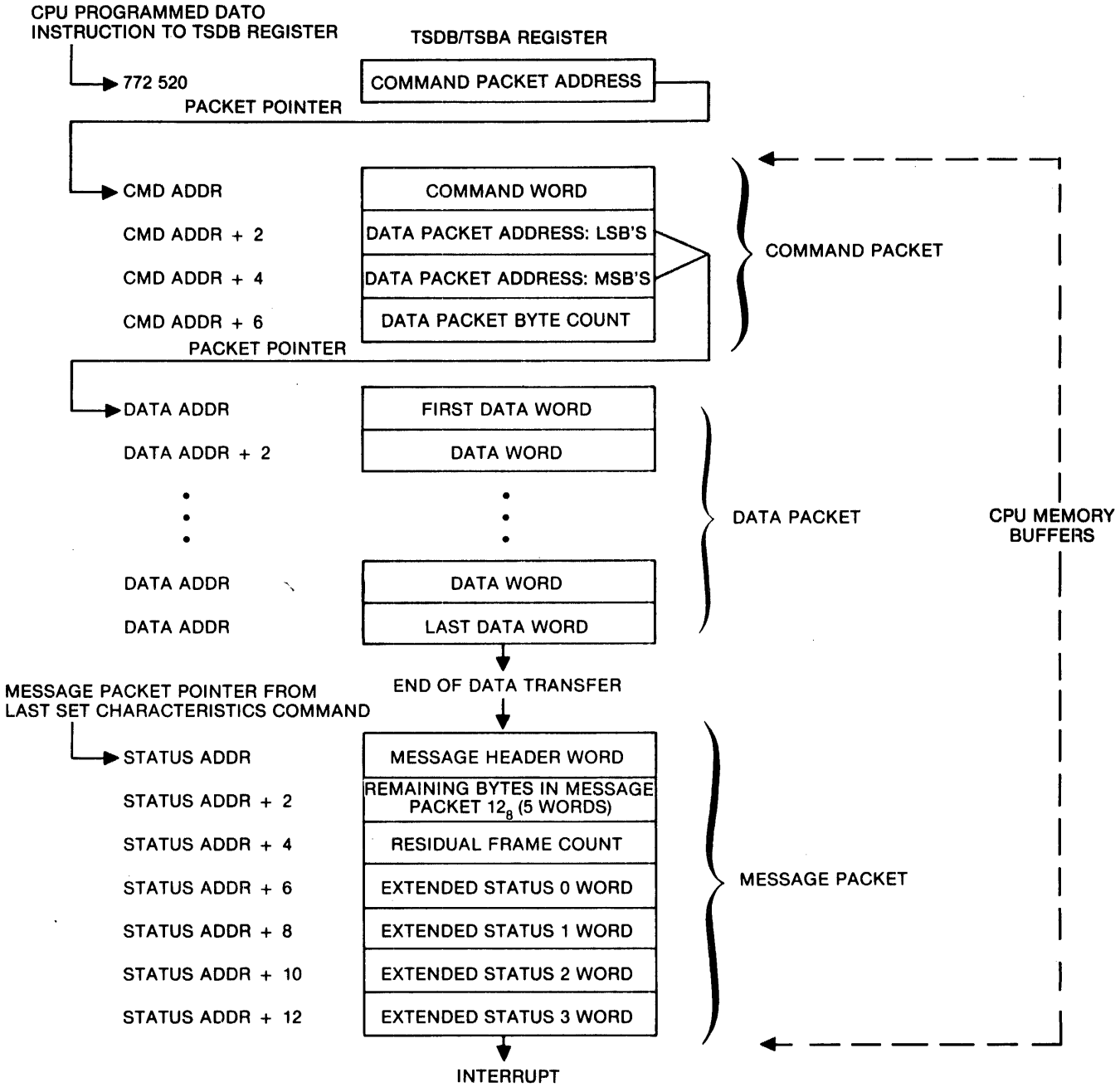


Figure 4-1. READ/WRITE Command Sequence

7. The reading or writing of data continues until either the proper byte count is reached or until the end of a record (reading) is detected.
8. Status information is now loaded into:
   A. Register TSSR in the coupler
   B. Seven memory locations (the message packet) defined by the last Set Characteristics command
9. The coupler generates an interrupt to signal the end of a command

A "Set Characteristics" command packet was mentioned in step 3 of the Read/Write command sequence. The Set Characteristics command is one of five commands that do not cause tape motion. The principle purpose of this command is to load the starting address of the message packet into the coupler. The secondary purpose is to load a characteristics word into the coupler. The characteristics word controls "interrupt" and "space files stop" conditions in the coupler. Figure 4-2 shows a Set Characteristics Command sequence.

REGISTERS AND PACKETS

The following material describes the coupler registers and illustrates and describes the contents of the packets.

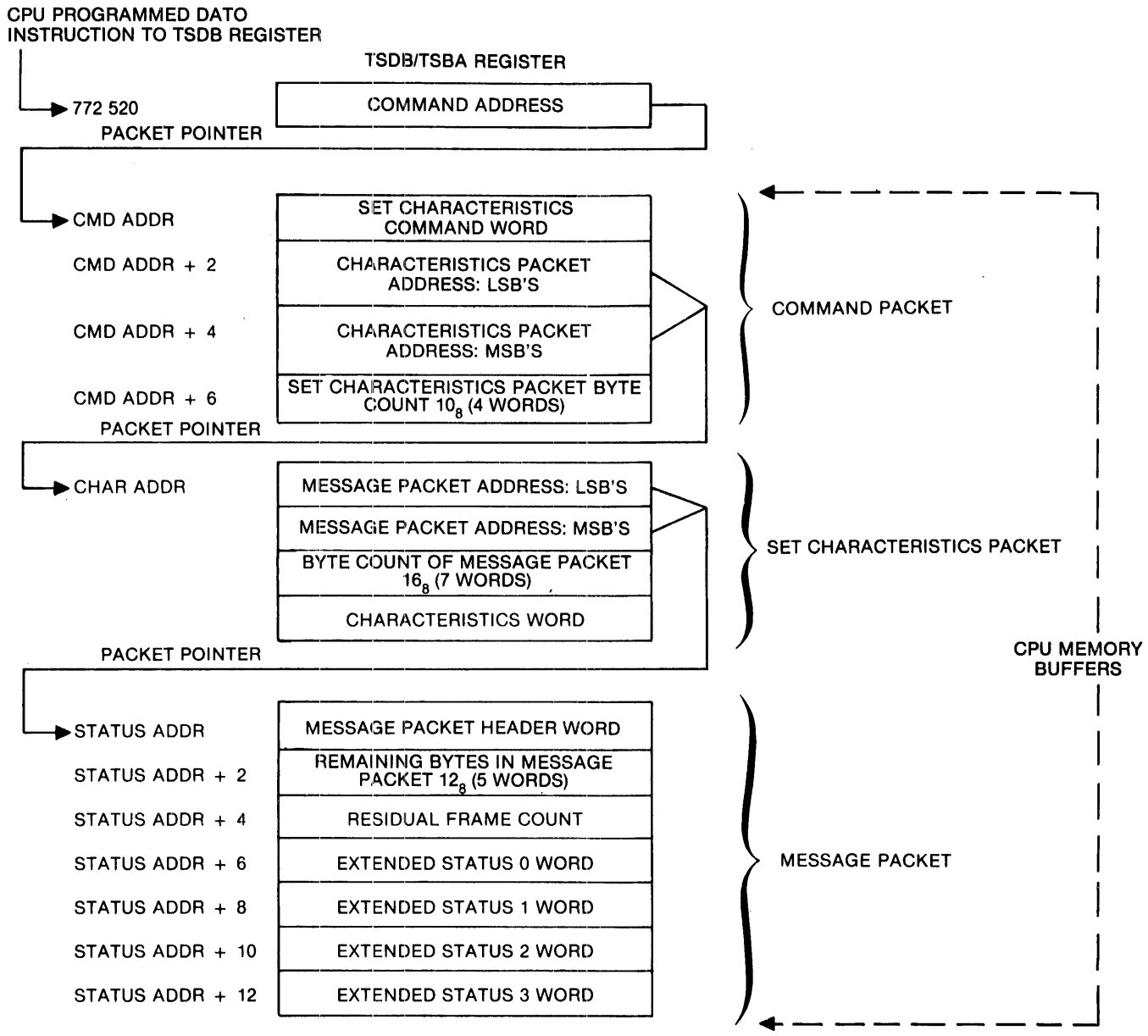
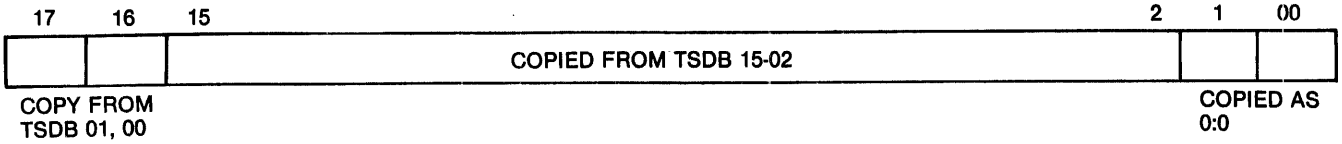


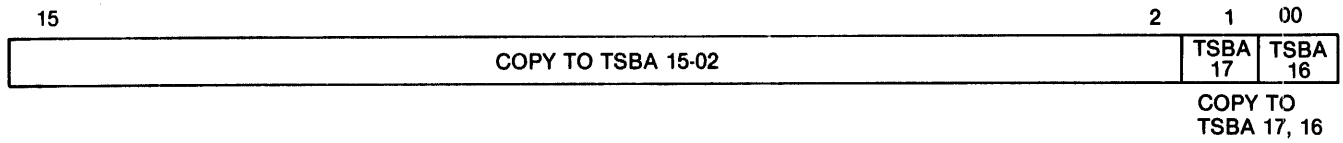
Figure 4-2. SET CHARACTERISTICS Command Sequence

Bus Address Register (TSBA) Read Only
772520 (Transport 0) **772530 (Transport 2)**
772524 (Transport 1) **772534 (Transport 3)**



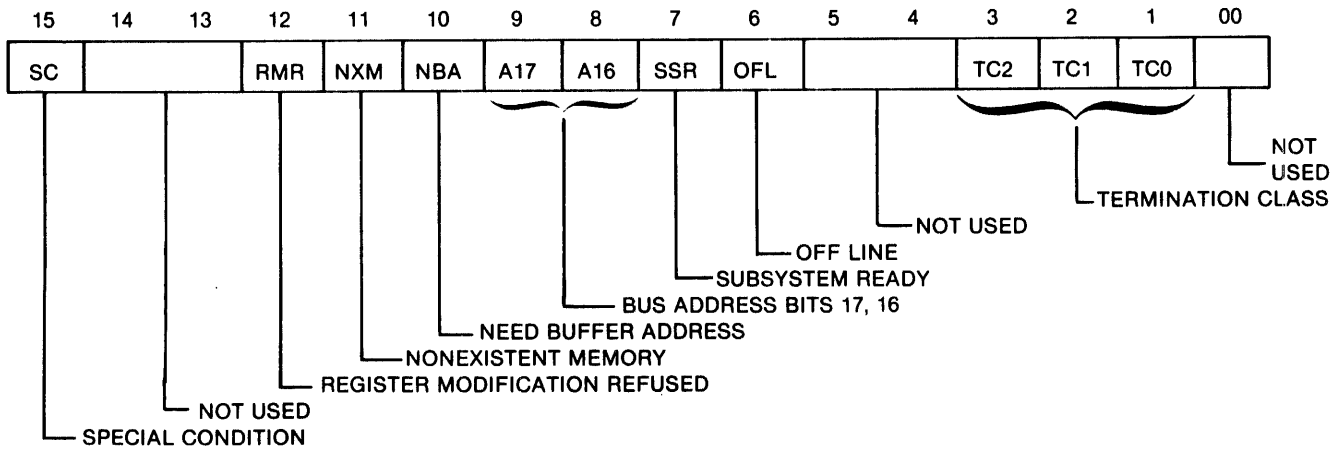
This 18-bit register is parallel loaded from TSDB each time TSDB is loaded as a UNIBUS slave by the CPU. TSDB bits 15-2 load into TSBA bits 15-2; TSDB bits 1 and 0 load into TSBA bits 17 and 16. Zeroes are loaded into TSBA bits 1 and 0. TSBA bits 17-16 are displayed in Status Register (TSSR) bits 9 and 8 respectively. TSBA is a read-only register that contains the address of the last command packet address written into TSDB.

Data Buffer Register (TSDB) Write Only
772520 (Transport 0) **772530 (Transport 2)**
772524 (Transport 1) **772534 (Transport 3)**



This 16-bit register is parallel-loaded from the UNIBUS. This register is used to store command packets when the coupler is the bus slave (for beginning an operation). The packet pointer is shifted and copied automatically into the 18-bit TSBA to form the command packet address to memory. TSDB is also used for data during NPR transfers when the controller is bus master. When the controller is bus slave, TSDB can be loaded by three different transfers from a bus master; two transfers are for maintenance purposes (DAT0B to high byte and DAT0B to low byte); the third transfer is for normal command initiation (DAT0). This is a write-only register and is not cleared by Subsystem Initialize, or Bus Initialize. The coupler responds with SSYN any time TSDB is written to by the program.

Status Register (TSSR) Read/Write (write causes Subsystem Initialize and rewinds tape to BOT)
772522 (Transport 0) **772532 (Transport 2)**
772526 (Transport 1) **772536 (Transport 3)**



In addition to loading this register, the coupler loads five extended status words into memory locations.

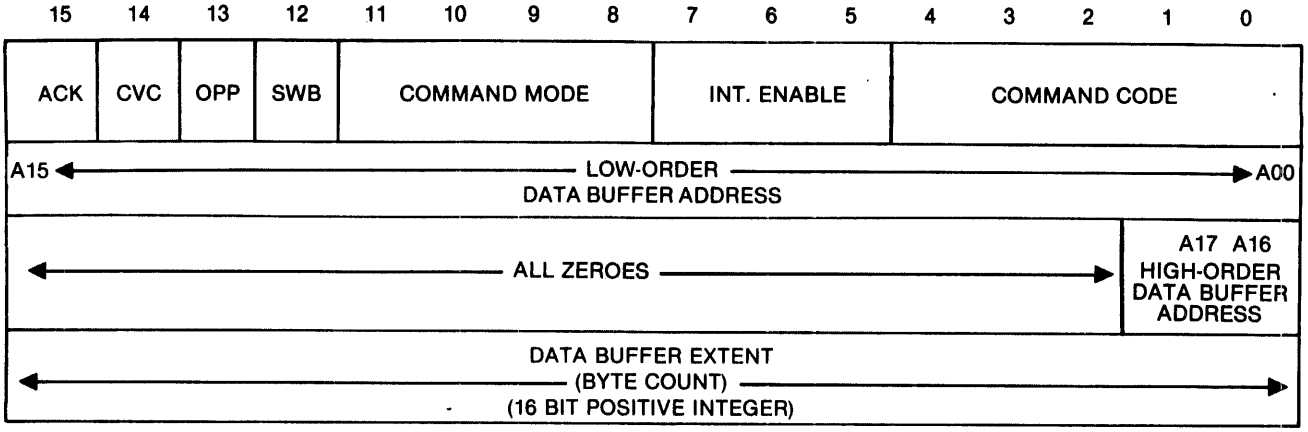
Status Register Bit Definitions

Bit	Name	Termination Class (TC) Octal Code	Definition
00	—	—	NOT USED
01	TC0	—	Termination Class Bit 00: See TC2 (bit 03) below.
02	TC1	—	Termination Class Bit 01: See TC2 (bit 03) below.
03	TC2	—	Termination Class Bit 02: This bit, along with bits TC1 and TC0, acts as an offset value when an error or exception condition occurs on a command. Each of the eight possible values of this field represents a particular class of errors or exceptions. It is expected that the code provided in this field will be utilized as an offset into a dispatch table for handling the condition. These bits are valid only when Special Condition (SC) bit 15 is set. See Table 4-1.
04, 05	—	—	NOT USED
06	OFL	—	Off-Line: When set, this bit indicates that the transport is off-line and unavailable for any tape motion commands.
07	SSR	—	Subsystem Ready: When set, this bit indicates that the TS11 subsystem is not busy and is ready to accept a new command pointer.
08	A16	—	Bus Address Bit 16: See A17 below (bit 09).
09	A17	—	Bus Address Bit 17: A17 and A16 (bits 08 and 09) display the values of bits 17 and 16 in the TSBA register.
10	NBA	—	Need Buffer Address: When set, this bit indicates that the transport needs a message buffer address. This bit is cleared during the Set Characteristics command if the transport gets valid data; it is always set after subsystem initialization.
11	NXM	4/5	Nonexistent Memory: This bit is set by the controller when trying to transfer to or from a memory location which does not exist. It may occur when fetching the command packet, fetching or storing data, or storing the message packet.
12	RMR	—	Register Modifications Refused: This bit is set by the controller when a command pointer is loaded into TSDB and Subsystem Ready (SSR) is not set. This bit may set on a bug-free system if ATTN interrupts are enabled.
13	—	—	NOT USED
14	—	—	NOT USED
15	SC	—	Special Conditions: When set, this bit indicates that the last command was not completed without incident. Specifically, either an error was detected or an exception condition occurred. An exception condition could be a tape mark on read commands, reverse motion at BOT, EOT while writing, etc.

Table 4-1. Status Register Termination Class Codes

TSSR Bits 3, 2, 1	Description
000	Normal termination.
001	Attention Condition: Set by a change in off-line (bit 06) or a microdiagnostic failure defined by Extended Status 3 word.
010	Tape status alert: Set by tape mark, short records, long records, or EOT bits in Extended Status 0 word.
011	Function reject: Set by off-line, write lock error, illegal command, illegal address, status change, or BOT in Extended Status 0 word.
100	Recoverable error (tape position—one record down from start of function)
101	Recoverable error (tape not moved)
110	Unrecoverable error (tape position lost)
111	Fatal controller error

Command Packet: Command Word Data Buffer Address, Byte Count



Command Word Bit Description

Bit	Name	Definition
0-4	Command Code Field	These bits are used with command mode field data to specify tape subsystem commands. See bits 8-11 and Table 4-1.
5-7	Interrupt Enable Bits	The following two values are defined in this field. If Interrupt Enable is on, an interrupt is generated when the SC bit or Ready bit (Status register) sets. **Bit Values** **Definition** 000 Interrupt disable 100 Interrupt enable
8-11	Command Mode Field	These bits are used with command code field data to specify tape subsystem commands. See Tables 4-2 and 4-3.
12-14	Device Dependent Bits	These three bits are implemented as follows: **Bit** **Name** **Definition** 14 CVC Clear Volume Check 13 OPP Opposite (reverse the execution sequence of the reread commands) 12 SWB Swap Bytes (reverse byte order during read/write commands)
15	Acknowledge	This bit is set when a command is issued by the CPU indicating that the message buffer is now available to the controller for any pending or subsequent message packets. This bit passes control of the message buffer to the controller.

Table 4-2. Command Code and Mode Field Definitions — Standard

Command Code Field	Command Name	Command Mode Field	Mode Name
00001	Read	0000	Read next (forward)
		0001	Read previous (reverse)
		0010	Reread previous (space reverse, read forward)
		0011	Reread next (space forward, read reverse)
00100	Set Characteristics	0000	Set status message packet address and device characteristics word.
00101	Write	0000	Write data
		0010	Write data retry (space reverse, erase, write data)
01000*	Position	0000	Space records forward
		0001	Space records reverse
		0010	Skip tape marks forward (space files)
		0011	Skip tape marks reverse (space files)
		0100	Rewind
01001**	Format	0000	Write tape mark
		0001	Erase (erase 3 inches of tape)
		0010	Write tape mark retry (space reverse, erase, write tape mark)
01010**	Control	0000	Message packet buffer release
		0001	Rewind and unload
		0010	Clean
01011**	Initialize	0000	Drive initialize
01111**	Get Status	0000	Get status (END message packet)

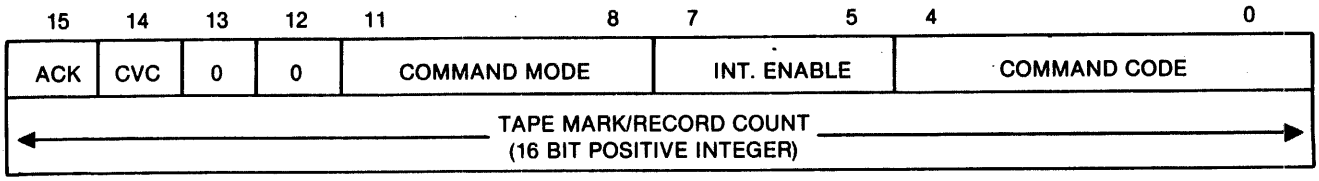
*Short (2 word) command packet
**One word command packet

Table 4-3. Command Code and Mode Field Definitions—Streaming*

Command Code Field	Command Name	Command Mode Field	Mode Name
10001	Read Streaming	0000	Read next (forward)
		0001	Read previous (reverse)
		0010	Reread previous (space reverse, read forward)
		0011	Reread next (space forward, read reverse)
10101	Write Streaming	0000	Write data
		0010	Write data retry (space reverse, erase, write data)
11000**	Position Streaming	0000	Space records forward
		0001	Space records reverse
		0010	Skip tape marks forward (space files)
		0011	Skip tape marks reverse (space files)
		0100	Rewind
11001***	Format Streaming	0000	Write tape mark
		0001	Erase (erase 3 inches of tape)
		0010	Write tape mark retry (space reverse, erase, write tape mark)

*Jumper JP6 to FDEN, JP7 to FTAD0, and JP8 to FTAD1.
**Short (2 word) command packet
***One word command packet

Short Command Packet: Command Word and Count



This command causes the tape to space records forward or reverse, skip tape marks forward or reverse, or to rewind to BOT. An exact tape mark/record count must be the second word of the packet for Skip Tape Mark and Space Record commands.

A Space Records operation automatically terminates when a tape mark is traversed. Also, Record Length Short (RLS) is set if the record count was not decremented to zero.

A Skip Tape Marks command terminates when it encounters a double tape mark and the Enable Skip Stop mode is specified (ESS bit set) in the characteristics word. Termination will also occur if a tape mark is the first record off BOT and the ESS and ENB bits are set in the characteristics word. Record Length Short (RLS) is set if the record count was not decremented to zero.

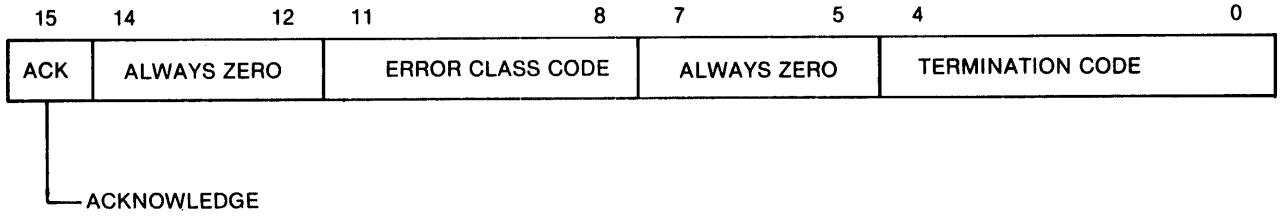
A Space Records Reverse or Skip Tape Marks Reverse, which runs into BOT, sets Reverse Into BOT (RIB) and causes a tape status alert termination.

When a Rewind command is issued, the interrupt will not occur until the tape reaches BOT.

Note

If the tape is positioned between BOT and the first record, and a Space Reverse or Skip Reverse is done, RIB will set and the residual frame count will equal the specified count in the original command.

Message Packet Header Word



Message Header Word Bit Definitions

Bit	Function
0-4	Termination codes.

Class Code	4-0 Value	Definition
0,2	10000	End—no errors
3	10001	Failure to execute
4,5,6,7	10010	Error during execution (1 or more)
1,7	10011	Attention. Interrupt caused by condition specified by error class codes.

5-7 ALWAYS ZERO

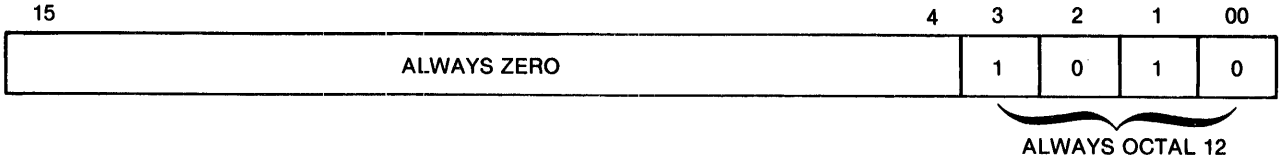
8-11 Error class codes—These bits define the class of failures found in the rest of the message buffer.

MSG Type	Class Code	Definition
ATTN	0000	Drive went on- or off-line (termination code = 10011)
FAIL	0001	Other error (ILC, ILA, NBA) (termination code = 10001)
FAIL	0010	Write lock error or non-executable function (termination code = 10001)

12-14 ALWAYS ZERO

15 This bit is used by the controller to inform the CPU that the command buffer is now available for any pending or subsequent command packets. On an ATTN message, this bit will not be set since the controller does not control the command buffer.

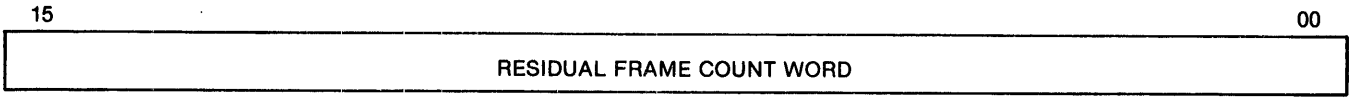
Message Packet Byte Count



These bits follow the message header word in the message packet. This byte count represents the number of bytes remaining in the message packet.

These bits always contain an Octal 12 representing 10 bytes (five words): the residual frame count and four status words.

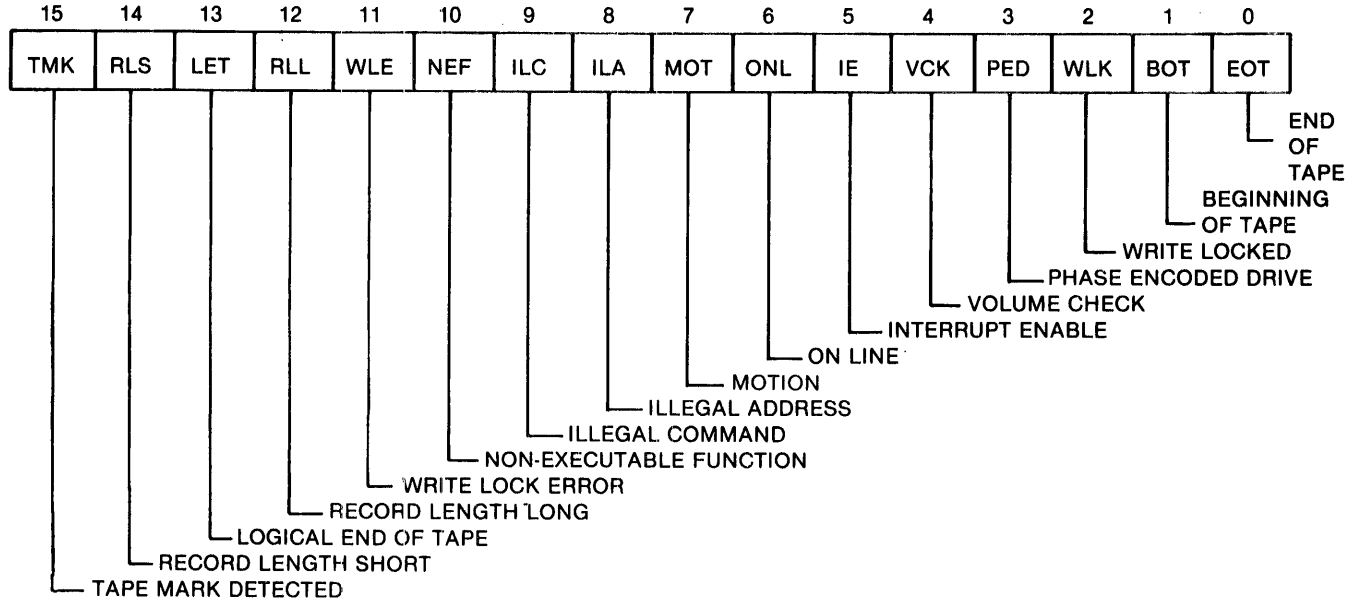
Residual Frame Count (RBPCR) Word



Word Three in the Message Packet

Bits	Description
00-15	This word contains the octal count of residual bytes, records, tape marks for the read, space records, and skip tape mark commands. The contents are meaningless for all other commands.

Extended Status 0 (XSTAT0) Word

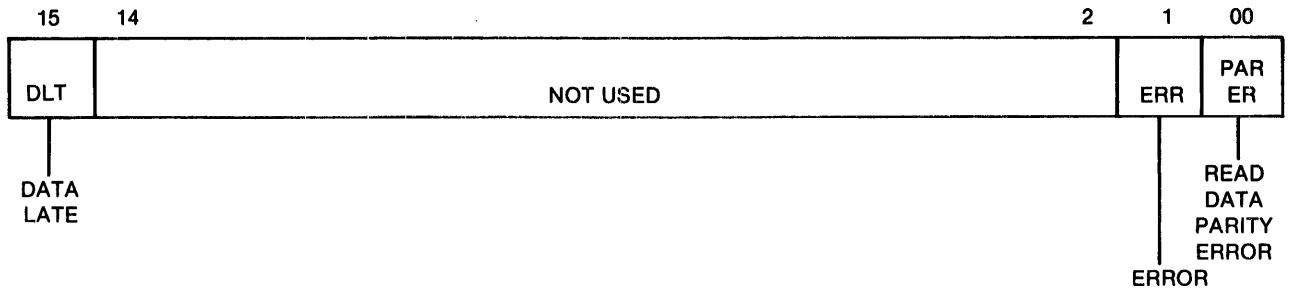


Extended Status 0 Word Bit Definitions

Bit	Name	Termination Code (TC)	Definition
00	EOT	2	End of Tape: This bit is set whenever the tape is positioned at or beyond the end-of-tape reflective strip. It is not reset until the tape passes over the reflective strip in the reverse direction under program control. Subsystem initialization always resets this bit (status on a read, TC2 on a write). Manually moving the EOT strip over the EOT sensor will not set or reset the EOT bit.

01	BOT	2/3	Beginning of Tape: When set, this bit indicates that the tape is positioned at the load point as denoted by the BOT reflective strip on the tape. This causes TC2 if reversed to BOT, and TC3 if at BOT when a reverse command occurs.
02	WLK	3	Write Locked: When set, this bit indicates that the mounted tape reel does not have a write-enable ring installed. Therefore, the tape is write protected.
03	PED	—	Phase Encoded Drive: When set, this bit indicates that the transport is capable of reading and writing 1600-bit, phase-encoded data. When 0, this bit indicates 800 bpi, NRZ data.
04	VCK	3	Volume Check: This bit is set when the transport changes state (on-line to off-line and vice versa). It is always set after initialization.
05	IE	—	Interrupt Enable: This bit, when set, reflects the state of the Interrupt Enable bit in the last command.
06	ONL	1/3	On-Line: When set, this bit indicates that the transport is on-line and operational. It causes a TC1 on an ATTN interrupt, or a TC3 for a non-executable function if the function was rejected because the transport was off-line.
07	MOT	—	Motion: When set, this bit indicates that the capstan has moved.
08	ILA	3	Illegal Address: When set, this bit indicates that the address contains more than 18 bits or is an odd number.
09	ILC	3	Illegal Command: This bit is set when a command is issued and either its command code field or its command mode field contains codes not supported by the transport.
10	NEF	3	Non-Executable Function: When set, this bit indicates that the command could not be executed due to one of following conditions: • The command specified reverse tape direction but the tape was already positioned at BOT. • A motion command was issued without the Clear Volume Check (CVC) bit being set while the Volume Check bit was set. • A motion command was issued when the transport was off-line. • A write command was issued when the tape did not contain a write-enable ring (write lock status [WLS]).
11	WLE	3	Write Lock Error: When set, a TC3 indicates that a write operation was issued but the mounted tape did not contain a write-enable ring.
12	RLL	2	Record Length Long: When set, this bit indicates that the record read was longer than the byte count specified.
13	LET	2	Logical End of Tape: This bit is set only on the Skip Tape Marks command under two conditions: when either two contiguous tape marks are detected, or, when moving off BOT, the first record encountered is a tape mark. This bit will not set unless this mode of termination is enabled through use of the Set Characteristics command. LET will set only in the forward direction.
14	RLS	2	Record Length Short: This bit, when set, indicates one of the following: 1) The record length was shorter than the byte count on a read operation; 2) a Space Record operation encountered a tape mark or BOT before the position count was exhausted; 3) a Skip Tape Marks command was terminated by encountering BOT or a double tape mark (if Skip Tape Marks command is enabled, see LET, bit 13) before exhausting the position counter.
15	TMK	2	Tape Mark Detected: This bit is set when a tape mark is detected during a read, space, or skip command and as a result of the Write Tape Mark or Write Tape Mark Retry commands.

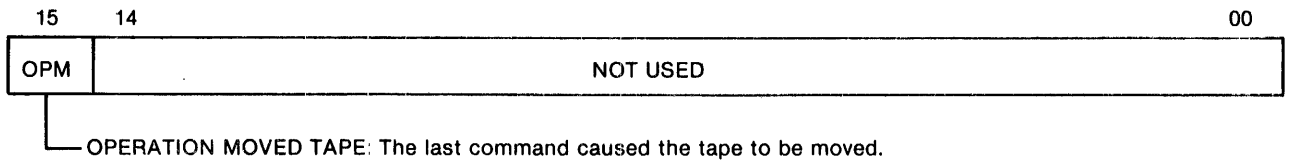
Extended Status 1 (XSTAT1) Word



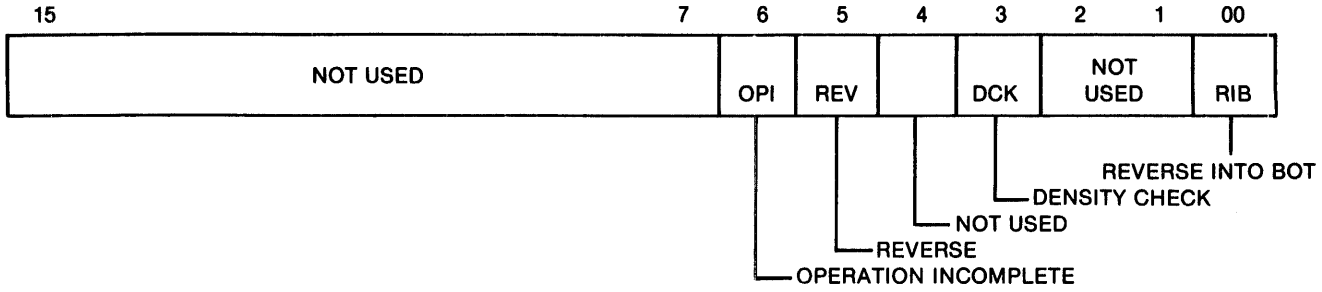
Extended Status 1 Word Bit Definitions

Bit	Name	Termination Class (TC) Octal Code	Definition
00	PARER	4	Read-Data Parity Error: This bit, when set, indicates that the controller has detected a parity error on the read-data lines coming from the transport.
01	ERR	4	Uncorrectable Data: This bit is set when either a parity error occurs without a corresponding dead track indicator, or more than one dead track occurs in either the preamble or in the data field.
02-14	—	—	NOT USED
15	DLT	4	Data Late: This bit is set when the FIFO is full on a read command or empty on a write command. These conditions occur whenever the UNIBUS latency exceeds the transport's data transfer rate for a significant number of transfers.

Extended Status 2 (XSTAT2) Word



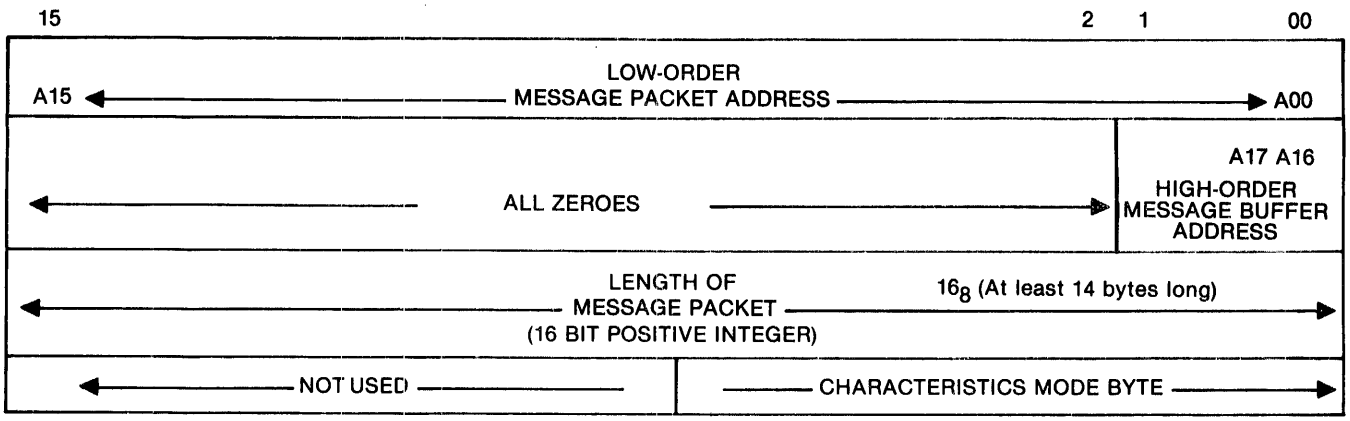
Extended Status 3 (XSTAT3) Word



Extended Status 3 Word Bit Definitions

Bit	Name	Termination Code (TC)	Definition
00	RIB	2	Reverse into BOT: This bit is set when a read, space, skip, or reverse command already in progress encounters the BOT marker when moving tape in the reverse direction. Tape motion will be halted at BOT.
01-02	—	—	NOT USED
03	DCK	6	This bit, when set, signifies that an invalid identification burst (IDB), indicating that the tape was not written in PE, was sensed at BOT. However, the tape can still be read if IDB is incorrect and the tape is actually written in PE. **Note** *If a tape with a bad IDB is appended, a termination code 6 will not occur until a write is attempted.*
04	—	—	NOT USED
05	REV	—	Reverse: This bit is set when the direction of the current tape operation is reverse. For multifunction retry commands, this bit is set if at least one of the commands is reverse.
06	OPI	6	Operation Incomplete: This bit is set when a read, space, or skip operation has moved 25 feet of tape without detecting any data on the tape. It is also set by a write command when the read head fails to see data transitions after moving four feet of tape.
07-15	—	—	NOT USED

Characteristics Packet



Characteristics Mode Byte Bit Definitions

Bit	Name	Definition
00-03	—	NOT USED
04	ERI	Enable Message Packet Release Interrupts to the CPU: If this bit is 0, interrupts will not be generated when a Message Packet Release command is received by the coupler; upon recognition of the command, only Subsystem Ready (SSR) will be reasserted. If ERI is a 1, an interrupt will be generated.
05	EAI	Enable Attention Interrupts: When this bit is a 0, attention conditions, such as off-line, on-line, and microdiagnostic failure, will not result in interrupts to the CPU. If this bit is a 1, interrupts will be generated. **Note** *The coupler must control the message buffer, via message buffer release, to set Attention Interrupts.*
06	ENB	Enable Skip Tape Marks Stop at BOT: This bit is meaningful only if the ESS bit is set. If the drive is at BOT when a Skip Tape Marks command is issued, and the first record seen is a tape mark, then the transport will set LET (XSTAT0) and stop after the first tape mark. If ENB is clear, the drive would not set LET but just count the tape mark and continue.
07	ESS	Enable Skip Tape Marks Stop: When this bit is set, the transport stops during a Skip Tape Mark command when a double tape mark (two contiguous tape marks) is detected. If this bit is cleared, the Skip Tape Marks command will terminate only on Tape Mark Count Exhausted or if BOT is detected.
08-15	—	NOT USED

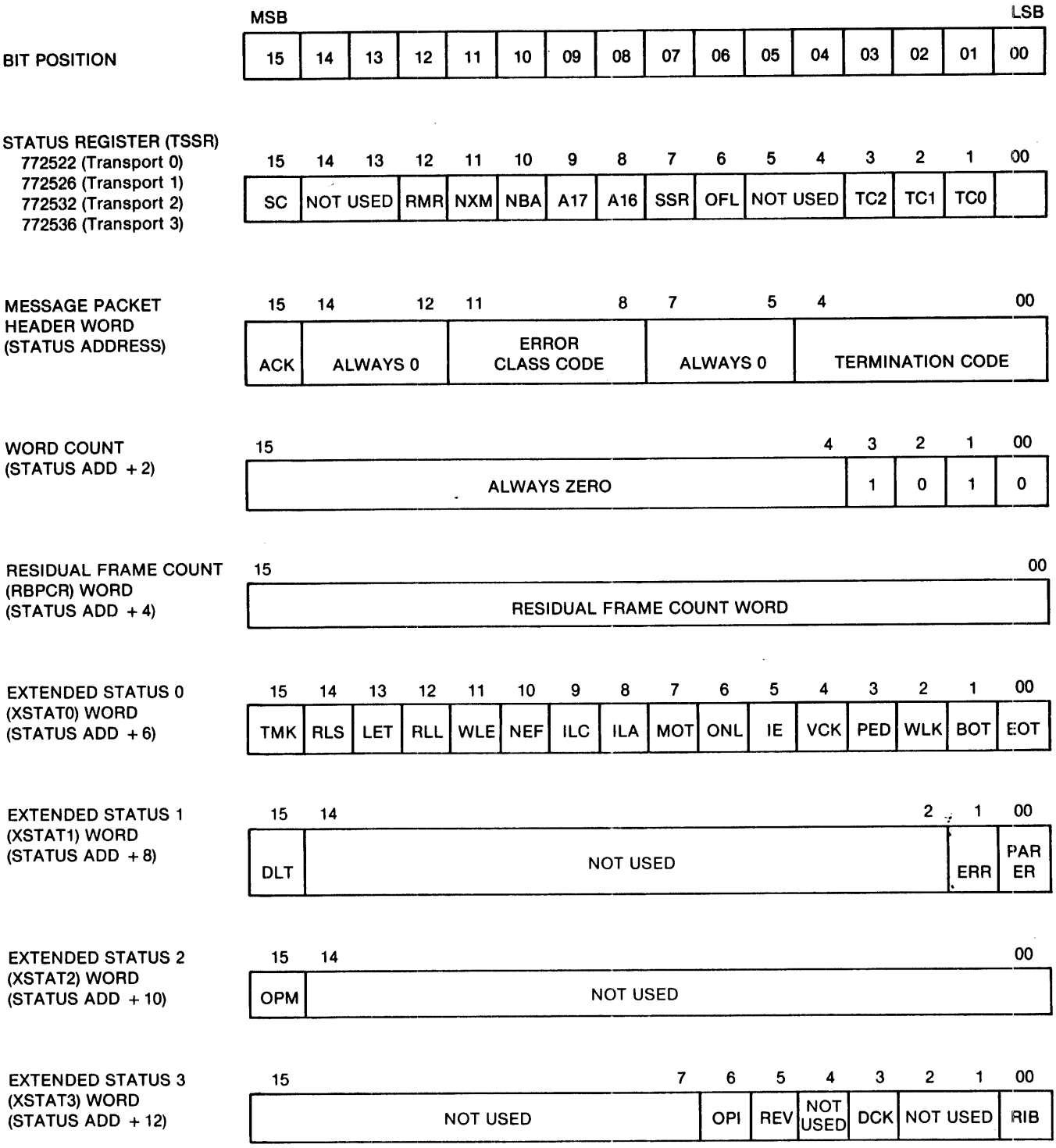


Figure 4-3. Message Packet Summary of Registers

SECTION 5
TROUBLESHOOTING AND THEORY

This section describes troubleshooting procedures at three levels of complexity: basic system, symptoms, and detailed analysis. Basic system troubleshooting procedures are visual checks not requiring test equipment and may be performed by the operator. Coupler symptom procedures may require a scope, meter, extender board or diagnostics and should be performed by a technician. Detailed analysis is troubleshooting at the IC level, and is presented for engineers or system analysts for coupler evaluation. The latter method may require the use of test equipment and the material presented here: board layout, term listing, theory of operation and logic diagrams.

CAUTION

Any troubleshooting requires a familiarity with the installation and operation procedures in this manual, the appropriate DEC manual, and the tape drive manufacturer's manual. Ensure power is off when connecting or disconnecting the board or plugs.

BASIC SYSTEM TROUBLESHOOTING

The following should be checked before power is applied:

1. Verify that all signal and power cables are properly connected. Ribbon cable connectors are *not* keyed. The arrows on the connectors should be properly aligned.
2. Verify that all switches are properly set as described in Sections 2 and 3.
3. Verify that all modules are properly seated in the computer and are properly oriented.

The following should be checked during or after application of power:

1. Verify that the computer and tape drive generate the proper responses when the system is powered up.
2. Verify that the computer panel switches are set correctly.
3. Verify that the console can be operated in the local mode. If not, the console may be defective.
4. Verify that the green diagnostic LED on the coupler is on and the red LED is off.

COUPLER SYMPTOMS

Coupler symptoms, possible causes and checks/corrective action are described in Table 5-1. Voltage checks should be performed before troubleshooting more complex problems. The +5V power source may be checked from any component shown on the logic diagrams.

PHYSICAL LAYOUT

The physical layout of the board is shown in Figure 5-1. Column and row numbers on the layout correspond to the numbers on each IC on the logic diagrams.

TERM LISTING

The input and output terms for each logic diagram are described in Table 5-2. The origin sheets refer to the sheet numbers on the logic diagrams.

The logic diagrams follow the Theory section.

THEORY

This section contains the theory of operation of the coupler. The text refers to block and timing diagrams interspersed with text, a term listing, and detailed logic diagrams. The material begins with a general description followed by a functional description.

The general description depicts the interconnection of the major logic elements that make up the coupler. The principal reference is the simplified block diagram. The functional description depicts the individual logic elements within the coupler. The text is referenced to the detailed block diagram. The numbers in the corners of the boxes on the detailed block diagram (Sheet 1) refer to the sheet number of the schematic showing that circuit. The description assumes an understanding of the PDP-11 I/O bus and a basic understanding of digital computer theory.

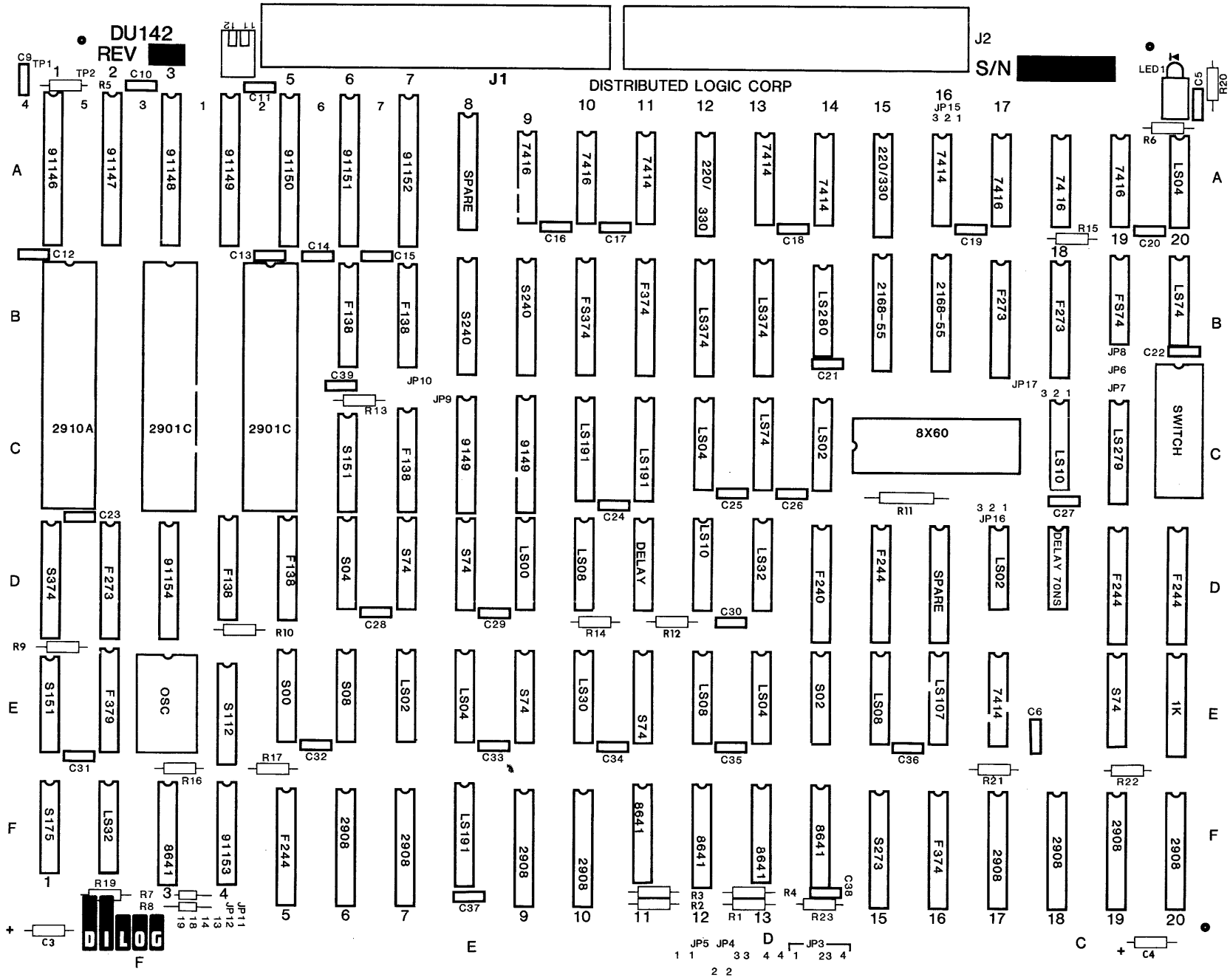


Figure 5-1. Board Layout

Table 5-1. Coupler Symptoms

Symptom	Possible Cause	Check/Replace
1. GREEN DIAGnostic light on coupler is OFF.	A. Microprocessor section of coupler inoperative. B. Short or open on board. C. Bad integrated circuit. D. No DC power.	Put board on extender. With scope look at pins of 2901. All pins except power and ground should be switching. Look for "stuck high", or "stuck low", or half-amplitude pulses. If no switching, either power or oscillator bad.
2. No communication between console and computer.	A. Shorted bus transceiver IC. C. Bad CPU board. B. Run CPU diagnostics.	A. Check I/O IC's. Remove coupler board to see if trouble goes away.
3. No data transfers to/from tape.	A. Tape not ready or bad cable connection. B. Improper communication with tape registers on coupler or bad IC in register section of coupler.	A. Check tape switches and cable connector. B. Run DEC diagnostics.
4. Data transferred to/from tape incorrect.	A. Bad memory board in backplane. B. Noise or intermittent source of DC power in computer. C. Bad IC in tape I/O section of coupler.	A. Run memory diagnostics. B. Check AC and DC power. C. While operating, check lines from coupler to tape with a scope for short or open.

Table 5-2. Term Listing

TERM	ORIGIN SHEET	DESTINATION	DESCRIPTION
A00L	Bus (EH2)	6	Address Bus Bit 00 (LSB)
A01L	Bus (EH1)	6	Address Bus Bit 01
A02L	Bus (EF1)	6	Address Bus Bit 02
A03L	Bus (EV2)	6	Address Bus Bit 03
A04L	Bus (EU2)	6	Address Bus Bit 04
A05L	Bus (EV1)	6	Address Bus Bit 05
A06L	Bus (EU1)	6	Address Bus Bit 06
A07L	Bus (EP2)	6	Address Bus Bit 07
A08L	Bus (EN2)	6	Address Bus Bit 08
A09L	Bus (ER1)	6	Address Bus Bit 09
A10L	Bus (EP1)	6	Address Bus Bit 10
A11L	Bus (EL10)	6	Address Bus Bit 11
A12L	Bus (EC1)	6	Address Bus Bit 12
A13L	Bus (EK2)	6	Address Bus Bit 13
A14L	Bus (EK1)	6	Address Bus Bit 14
A15L	Bus (ED2)	6	Address Bus Bit 15
A16L	Bus (EE2)	5	Address Bus Bit 16
A17L	Bus (ED1)	5	Address Bus Bit 17 (MSB)
AD00+/AD15+	6	2	Buffered Address Bits 00-15 From Address Bus Into Coupler
AD16+, AD17+	5	2	Buffered Address Bits 16 and 17 Into Coupler
ADDOVFL	6	4	Address Overflow
BBSYL	5	Bus (FD1)	Bus Busy
BG4 (in)	5	Bus (DS2)	Bus Grant In
BG5 (in)	5	Bus (DP2)	Bus Grant In
BG6 (in)	5	Bus (DM2)	Bus Grant In
BG7 (in)	5	Bus (DK2)	Bus Grant In
BG4 (out)	5	Bus (DT2)	Bus Grant Out
BG5 (out)	5	Bus (DR2)	Bus Grant Out
BG6 (out)	5	Bus (DN2)	Bus Grant Out
BG7 (out)	5	Bus (DL2)	Bus Grant Out
BR4L	5	Bus (DH2)	Bus Request Level 4
BR5L	5	Bus (DF2)	Bus Request Level 5
BR6L	5	Bus (DE2)	Bus Request Level 6
BR7L	5	Bus (DD2)	Bus Request Level 7
BSYCR+	3	5	Bus Busy
COL	5	Bus (EJ2)	Control Line Defining Type of Data Transfer
CIL	5	Bus (EF2)	Control Line Defining Type of Data Transfer
CCE-	8	9	Condition Code
CCG-	14	15	Check Character Gate-PE Identification Burst Detected
CCROK-	12	4, 6	Coupler Check Read OK
CER+	14	13	Corrected Error

Table 5-2. Term Listing (Continued)

TERM	ORIGIN SHEET	DESTINATION	DESCRIPTION
CLREOT-	12	14	Clear End of Tape
COUT +	11	8	Carry Out
CR1-0/CR1-2	10	8, 11	Control Register One Output Bits 0-2
CR1-3/CR1-7	10	11	Control Register One Output Bits 3-7
CR2-0/CR2-7	10	11	Control Register Two Output Bits 0-7
CR3-0	10	11	Control Register Three Output Bit 0
CR3-1/CR3-7	10	11	Control Register Three Output Bits 1-7
CR4-0	10	9	Control Register Four Output Bit 0
CR4-1/CR4-3	10	8	Control Register Four Output Bits 1-3
CR4-4/CR4-7	10	9	Control Register Four Output Bits 4-7
CR5-0/CR5-7	10	9	Control Register Five Output Bits 0-7
CR6-0/CR6-6	10	12	Control Register Six Output Bits 0-6
CR6-7	10	9	Control Register Six Output Bit 7
CSA0 + /CSA9 +	9	10	Control Store Address Bits 0-9 (10-bit)
D00 + /D07 +	4	11	D Bus Bits 0-7
D00 + /D07 +	6, 7	13	D Bus Bits 0-7
D00 + /D07 +	10	11	D Bus Bits 0-7
D00 + /D07 +	13	16	D Bus Bits 0-7
D00 + /D07 +	16	11	D Bus Bits 0-7
D00L	7	Bus (CS2)	Data Bit 0 to/from UNIBUS
D01L	7	Bus (CR2)	Data Bit 1 to/from UNIBUS
D02L	7	Bus (CU2)	Data Bit 2 to/from UNIBUS
D03L	7	Bus (CT2)	Data Bit 3 to/from UNIBUS
D04L	7	Bus (CN2)	Data Bit 4 to/from UNIBUS
D05L	7	Bus (CP2)	Data Bit 5 to/from UNIBUS
D06L	7	Bus (CV2)	Data Bit 6 to/from UNIBUS
D07L	7	Bus (DM2)	Data Bit 7 to/from UNIBUS
D08L	7	Bus (CL2)	Data Bit 8 to/from UNIBUS
D09L	7	Bus (CK2)	Data Bit 9 to/from UNIBUS
D10L	7	Bus (CJ2)	Data Bit 10 to/from UNIBUS
D11L	7	Bus (CH1)	Data Bit 11 to/from UNIBUS
D12L	7	Bus (CH2)	Data Bit 12 to/from UNIBUS
D13L	7	Bus (CF2)	Data Bit 13 to/from UNIBUS
D14L	7	Bus (CE2)	Data Bit 14 to/from UNIBUS
D15L	7	Bus (CD2)	Data Bit 15 to/from UNIBUS
D16L, D17L	4	5	D Bus Bits 16 and 17 Become Address
DATLAT-	15	14	Data Late
DCLOL	5	Bus (CN1)	From UNIBUS-DC Line Low Power Detection
DCLO +	5	2	From UNIBUS-DC Line Low Buffered
DCOK +	2	4	DC Voltage OK
DMAGO +	3	6	Direct Memory Access Go Clock Pulse
DMAREQ +	12	3	Direct Memory Access Request
EADD-	3	5, 6	Enable Address
EDATA-	7	5	Enable Data
EMPTY +	15	14, 16	Empty Signal From FIFO Buffer
ENAFIFO +	4	15, 16	Enable FIFO Buffer
ENMSYN-	3	8	Enable Master Synchronize
EOTSTA +	14	13	End of Tape Status
ERASE +	14	13	Erase Command
FAD0/FAD9	15	16	FIFO Buffer Address Lines
FCCG/ID	14	J2 (16)	Formatter Check Character Gate/Identification
FCER	14	J2 (42)	Formatter Corrected Error Status
FDBY	14	J2 (38)	Formatter Data Busy Status
FDEN	14	J2 (50)	Formatter Density Select Command
FDWDS	J2 (36)	15	Formatter Demand Write Data Strobe Request Signal
FEDIT	14	J1 (38)	Formatter Edit Mode Command
FEOT	14	J2 (22)	Formatter End of Tape Mark Status
FERASE	14	J1 (40)	Formatter Erase Command
FFAD	14	J2 (48)	Formatter Address Control Line
FFBY	14	J1 (2)	Formatter Busy Status
FFEN	14	J2 (18)	Formatter Enable Control Line
FFMK	14	J2 (14)	Formatter File Mark Detected Status
FFPT	14	J2 (32)	Formatter Write File Protected Status
FGO	14	J1 (8)	Formatter Go (Initiate Activity) Control Line
FHER	14	J2 (12)	Formatter Hard Error Status
FIFRD-	15	15, 16	FIFO Buffer Read Clock
FIFWT-	15	15, 16	FIFO Buffer Write Clock
FLDP	14	J2 (4)	Formatter Load Point Mark Status
FLOL	14	J1 (16)	Formatter Load On Line Command
FLWD	16	J1 (4)	Formatter Last Word
FMK-	14	13	File Mark Detected Status Line

Table 5-2. Term Listing (Continued)

TERM	ORIGIN SHEET	DESTINATION	DESCRIPTION
FNRZ	13	15	Formatter NRZ Data Format Status Signal
FOFL	14	J2 (24)	Formatter Off Line Command
FONL	14	J2 (44)	Formatter On Line Status Signal
FRD0	16	J2 (2)	Read Data and Parity Line 0
FRD1	16	J2 (3)	Read Data and Parity Line 1
FRD2	16	J1 (48)	Read Data and Parity Line 2
FRD3	16	J1 (50)	Read Data and Parity Line 3
FRD4	16	J2 (6)	Read Data and Parity Line 4
FRD5	16	J2 (20)	Read Data and Parity Line 5
FRD6	16	J2 (10)	Read Data and Parity Line 6
FRD7	16	J2 (8)	Read Data and Parity Line 7
FRDP	16	J2 (1)	Read Data and Parity Lines
FRDY	14	J2 (28)	Formatter Ready Status
FREV	14	J1 (18)	Formatter Reverse Command
FREW	14	J1 (20)	Formatter Rewind Command
FRSTR	15	J2 (34)	Formatter Read Strobe Signal
FRTH1	14	J1 (44)	Formatter Read Threshold 1 Control
FRTH2	14	J1 (36)	Formatter Read Threshold 2 Control
FRWD	14	J2 (30)	Formatter Rewinding Status
FTAD0	14	J1 (46)	Formatter Address Line 0 Control (MSB)
FTAD1	14	J2 (46)	Formatter Address Line 1 Control (LSB)
FULL+	15	14	FIFO Is Full
FWD0	16	J1 (10)	Formatter Write Data Line 0
FWD1	16	J1 (12)	Formatter Write Data Line 1
FWD2	16	J1 (30)	Formatter Write Data Line 2
FWD3	16	J1 (26)	Formatter Write Data Line 3
FWD4	16	J1 (6)	Formatter Write Data Line 4
FWD5	16	J1 (32)	Formatter Write Data Line 5
FWD6	16	J1 (23)	Formatter Write Data Line 6
FWD7	16	J1 (24)	Formatter Write Data Line 7
FWDP	16	J1 (22)	Formatter Write Data Parity Line
FWFM	14	J1 (42)	Formatter Write File Mark Command
FWRT	14	J1 (34)	Formatter Write Command
GO-	14	13	Buffered Initialize Signal to Formatter
INACT+	15	14	Input Active to FIFO
INCRAM-	12	13	Increment RAM Buffer Address Lines
INIT+	5	2	Buffered Go Pulse to Formatter
INITL	5	Bus (DL1)	Initialize Signal at UNIBUS
INTG+	2	4, 8	Interrupt Grant Logic Signal
INTR+	4	3, 5, 7	Interrupt Signal
INTRL	5	Bus (FM1)	Interrupt Signal at (to) UNIBUS
ISACK-	2	3	Interrupt Select Acknowledge
LCOUT-	8	11	Latched Carry Out
LDDIR+	3	7	Load Data Into Registers From UNIBUS
LXR0-	12	7	Data Out Register (MSB)
LXR1-	12	7	Data Out Register (LSB)
LXR2-	12	6	DMA Address (MSB)
LXR3-	12	6	DMA Address (LSB)
LXR4-	12	4	UNIBUS Control
LXR5-	12	14	Transport Command
LXR6-	12	15, 16	FIFO Buffer Load
LXR7-	12	14	Transport Control
LXRB-	12	9	Microvector Address
LXRC-	12	2	Light Off
LXRD-	12	13	ROM Address
LXRE-	12	13	RAM Address
LXRF-	12	13	RAM Destination
MASTR+	3	4	Bus Master
MSYN+	5	2	Master Sync
MSYNL	5	Bus (EE1)	Master Sync from Bus
NBSYSYN+	3	2	Not Busy *and* Not Slave Sync
NPGOUTH	5	Bus (CB1)	Non-Processor Grant Out
NPGINH	5	Bus (CA1)	Non Processor Grant In To Coupler
NPRBSY+	3	7	Non Processor Request Busy
NPRL	5	Bus (FJ1)	Non Processor Request To UNIBUS
OUTACT+	15	14	Output of FIFO Active
PARER+	16	4	Parity Error
RBBSY+	5	3	Received Bus Busy From UNIBUS
RBG-	5	2	Received Bus Grant
RC0+, RC1+	5	4	Received Control 0 and 1 Signals From UNIBUS
RELBUS-	12	3	Release Bus

Table 5-2. Term Listing (Continued)

TERM	ORIGIN SHEET	DESTINATION	DESCRIPTION
RESET+	2	5, 12	Reset Signal
RESET-	2	4, 10, 14	Reset Signal
REV+	14	6	Reverse Signal
RNPG-	5	3	Received Non Processor Grant
RSSYN+	5	3, 4	Received Slave Sync Signal From UNIBUS
RSTR+	15	13	Read Strobe Plus
RSTR-	15	16	Read Strobe Minus
SACKL	5	Bus (FT2)	System Acknowledge
SCLK-	4	4,8,9,10,11,12,15	System Clock 6 MHz
SETEOT-	12	14	Set End of Tape Control Pulse
SLAVE+	2	7, 8	Slave Coupler Address Detected
SSYNL	5	Bus (EJ1)	Slave Sync Signal at UNIBUS
STLGOOD+	4	4	Coupler Self Test Still Good
STPDMA-	7	3	Stop DMA Cycle
STRTCYCL-	12	3	Start DMA Cycle
TBG-	2	5	Transmit Bus Grant
TBR+	4	2	Transmit Bus Request
TBRI+	2	5	Transmit Bus Request In To UNIBUS
TC0+	4	5	Transmit Control 0 Signal To UNIBUS
TC1+	4	5, 7	Transmit Control 1 Signal To UNIBUS
TMSYN+	3	5	Transmit Master Sync
TNPG-	3	5	Transmit Non Processor Grant
TNPRI+	2	5	Transmit Non Processor Request
TSACK+	3	5	Transmit Select Acknowledge
TSSYN+	4	5, 7	Transmit Slave Sync
VEC+	9	10	Enable Vector Register
WRT+	14	16	Write Command
WRT-	14	15, 16	Write Command
XCLK-	4	12	Extra Clock; Same Phase as SCLK
XSD0-	12	6	Slave Address
XSD1-	12	7	Data Input (MSB)
XSD2-	12	7	Data Input (LSB)
XSD3-	12	4	CPU Bus Status
XSD4-	12	15, 16	FIFO Buffer
XSD7-	12	14	Transport Status 1
XSD8-	12	14	Transport Status 2
XSD9-	12	13	Switches 1
XSDA-	12	10	Literal
XSDD-	12	13	Switches 2
XSDE	12	13	ROM Source
XSDF-	12	13	RAM Source
Y00+/Y07+	11	4,6,7,8,9,14,15,16	Internal Y Bus Bits 0-7 (8)
ZERO+	11	8	Indicates Result of ALU Operation is Zero

GENERAL DESCRIPTION

Figure 5-2 is a simplified block diagram of the coupler. The coupler comprises three logical sections:

A. Computer interface

B. Microprocessor

C. Formatter (peripheral) interface

The three sections function together to transfer data between the I/O bus of the computer and up to four tape drives. The two interface sections match the voltage levels and load/drive characteristics of the computer I/O bus and tape drive I/O lines to the logic levels of the coupler. The microprocessor is the control, timing, and data conversion section of the coupler.

The microprocessor functions under control of firmware instructions stored in solid state, Programmable Read Only Memory (PROM). The microprocessor is implemented with AM2900-series bit-slice microprocessor chips. Refer to **MICROPROGRAMMING HANDBOOK** from Advanced Micro Devices, Inc., 1901 Thompson Place, Sunnyvale, California 94086 for introductory material on microprogramming a bipolar microprocessor.

The logic elements within the three major sections are connected internally by two 8-bit buses; the D Bus and the Y Bus. The D Bus carries information from the logic elements to the Arithmetic and Logic Unit (ALU) of the microprocessor; the Y Bus carries information from the ALU to the logic elements.

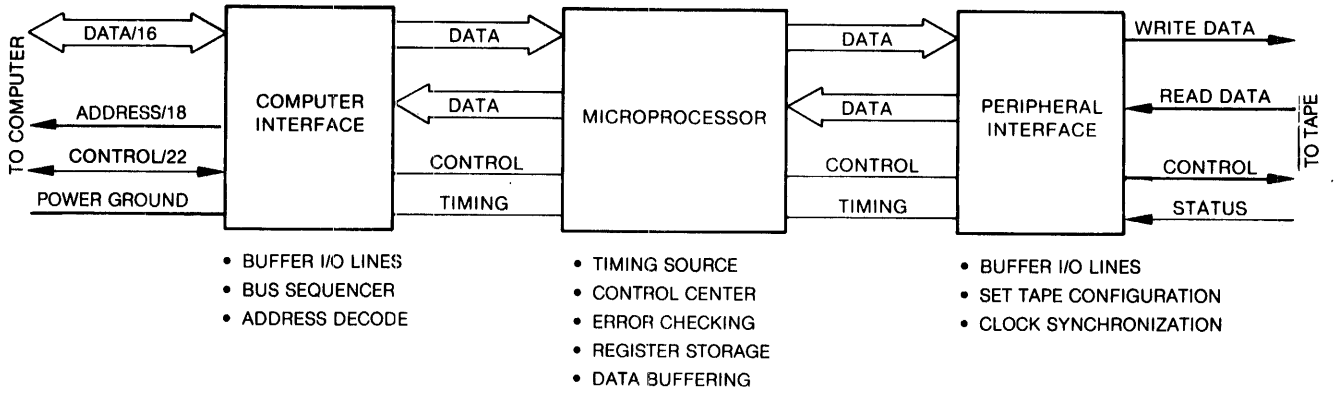


Figure 5-2. Simplified Block Diagram

Computer Interface

The purpose of the computer interface is to: (1) buffer lines between the UNIBUS of the computer and the controller, and (2) synchronize information transfers. There are three major classes of lines connected to the computer interface:

A. Data lines

B. Address lines

C. Control lines

There are 16 bidirectional data lines and 18 bidirectional address lines between the UNIBUS and the coupler. The 22 control lines may originate either at the UNIBUS or at the coupler. The control lines request information transfers, select the type and direction of the transfers, and synchronize the transfers.

Information transfers are initiated by a bus master placing an address on the address lines. The bus master then either receives data from, or outputs data to, the addressed slave device (coupler or memory). During initialization and coupler status word transfer sequences, the coupler is a slave. During data and message packet transfer sequences, the coupler is bus master and either receives data from or outputs data and extended status words to the computer memory via the NPR (DMA) facility.

The computer interface also controls the synchronization of NPR transfers on the UNIBUS. Bus synchronization is done by delay-line logic separate from the microprocessor to minimize bus use by the coupler. This permits many devices in addition to the tape coupler to use the NPR facility on a time-multiplexed basis.

Microprocessor

The microprocessor is the timing and control center of the coupler. The microprocessor is controlled by instructions stored in Programmable Read Only Memory (PROM). These instructions, called firmware, cause the microprocessor to operate in a prescribed sequence during each of the computer program selected functions. The functions are established by a series of instructions (a "packet") stored in computer memory. The starting address of this packet is issued to the coupler by the computer. The contents of the packet are accessed by the coupler and stored in registers within the microprocessor. The microprocessor acts upon the contents of the packet to perform the requested functions in the required sequence. The basic functions are read/write data, tape positioning, tape format, and coupler/tape drive control. Note that certain functions (rewind, rewind-unload) can be performed simultaneously with data transfers on any tape drive which is not involved in a data transfer operation.

The microprocessor contains a 256-byte Random Access Memory (RAM) dedicated to buffering data and message packets between the UNIBUS and the coupler. This RAM provides four words of data buffering. This buffer, in conjunction with a 4096 X 8-bit FIFO RAM data buffer and two hardware byte registers in the peripheral interface, provides a total of 4106 bytes of data buffer between the tape drives and the UNIBUS. This virtually eliminates data late errors.

The rate and order (format) of data transfers to the tape drive is controlled by the microprocessor. Within the microprocessor, data is handled in 8-bit parallel bytes. In addition to the decision making required prior to, during, and after a data transfer sequence, the microprocessor monitors error and status conditions within the coupler and from the tape drive. It assembles these error and status condition bits into bytes for transfer to the computer memory as a message packet.

Peripheral Interface

The purpose of the peripheral interface is to match the characteristics of the tape drive to the characteristics of the microprocessor. The peripheral interface:

A. Contains line drivers and receivers that buffer the data, status, and control lines between the coupler and the tape drive formatter over cable lengths up to 25 feet.

B. Contains jumpers and switches that permit configuring the coupler to match different tape subsystem configurations.

C. Contains a 4K X 8-bit FIFO data buffer between the coupler and the tape drive.

FUNCTIONAL DESCRIPTION

The detailed block diagram (Sheet 1) shows the functional elements of the tape coupler. The number (or numbers) within the blocks of the diagram refers to the detailed logic drawing(s) represented by the block. The term listing defines the mnemonics used in this text and on the logic drawings.

Computer Interface

The computer interface comprises the following logic elements:

A. UNIBUS data register and receiver/drivers

B. UNIBUS address register/counter and receiver/drivers

C. Address decode logic

D. UNIBUS control receiver/drivers

E. UNIBUS status and control logic

The computer interface is a hard-wired logic section that buffers and synchronizes information transfers between the UNIBUS and the other logic sections of the coupler. The address decode logic dynamically monitors the UNIBUS address lines. When the address of the TSDB/TSBA or TSSR register associated with one of the tape drives connected to the coupler is detected, the UNIBUS status and control logic is enabled. This logic alerts the microprocessor logic of impending activity and synchronizes information transfers between the UNIBUS and the D/Y buses of the coupler.

Address Decode Logic (Sheet 2)

The address decode PROM (4F) and gate (10E-8) assert signal SLAVE+ if the base address of the coupler is detected. The base address is the selected address of the TSDB/TSBA register of drive zero. One of four possible base addresses can be selected by the jumper points connected to pin 6 of gate 10E-8. The lowest base address is 772 520. The base address possibilities are given in Section 2.

The address of a specific tape drive among a possible four and the specific register associated with a tape drive are determined by the microprocessor. The eight least significant address bits are gated to the D Bus by XSD0−, which is the "decode slave address" signal from the source decode logic (Sheet 12).

The inputs to the address decode logic are from the UNIBUS address register and receiver/drivers (Sheets 5, 6) and the MSYNL signal from the UNIBUS (buffered to become MSYN+). The SLAVE+ signal enables the Test Slave Request flip flops to be set by the coupler clock. When this condition is detected by the microprocessor, an information transfer sequence is begun.

UNIBUS Address Register Receiver/Drivers (Sheets 5, 6)

The 16 least significant address bits are buffered between the UNIBUS and the coupler Y Bus by circuits 6F, 7F, 9F, and 10F, shown on Sheet 6; the two most significant address bits are buffered by circuit 11F, shown on Sheet 5. The two most significant address bits originate at UNIBUS control register 15F (Sheet 4). The circuits comprise a latch and open collector driver between the Y Bus and the UNIBUS and latch and receivers between the UNIBUS and address destinations within the coupler. The 14 most significant address bits received are connected to the address decode logic (Sheet 2). The eight least significant address bits received are connected through tri-state buffer circuit 5F to the D Bus by XSD0−. Signal EADD− connects address bits from the coupler address register to the UNIBUS. The byte-wide Y Bus is strobed into the 18-bit wide address register by signals LXR2 and LXR3.

Note that three of the four least significant bits are connected through up/down counter 8F to address bus transceiver circuit 9F. This counter is part of the up/down address counter that keeps track of the addresses required during a data transfer functin. On a Modulo 20 (octal) address boundary, signal ADDOVFL+ is generated.

UNIBUS Data Register Receiver/Drivers (Sheet 7)

Tri-state receiver latches and register/open collector driver circuits 17F, 18F, 19F, and 20F buffer data lines D00L-D15L between the UNIBUS and the coupler. Received data lines are labeled D00+-

D15+. The received data signals are latched into receiver registers by LDDIR+ and connected to the D Bus by XSD1 and XSD2. Data from the Y Bus is stored in driver register by LXR0, and LXR1, and is connected to the UNIBUS by INTR+ or TSSYN+ or TC1 and NPRBSY+.

UNIBUS Control Receiver/Drivers (Sheet 5)

The control lines between the UNIBUS and the control circuits of the coupler are buffered by circuits 3F, 11F, 12F, 13F, and 14F. The receivers are always connected to the UNIBUS. Most of the drivers are also permanently enabled, but circuit 11F is enabled by Enable Address (EADD) and circuit 13F is enabled by a delayed Enable Data (EDATA−) signal.

UNIBUS Status and Control Logic (Sheets 2, 3, 4)

To ensure the fastest response time, the synchronization of I/O bus transfers is done by hard-wired logic. Information transfers are of two kinds: programmed I/O and Non-Processor Request (NPR). During programmed I/O transfers the processor is bus master. During NPR (DMA) transfers the coupler is bus master.

During programmed I/O transfers, either the starting address of a command packet is stored in the TSDB register or the contents of the coupler TSSR register are accessed. These registers are located in the 256 X 8 RAM shown on Sheet 13. As mentioned in a previous paragraph, signal SLAVE+ in the address decode logic is asserted when the processor requires access to the coupler registers.

The UNIBUS status and control logic comprises:

A. Coupler interrupt logic (Sheet 2)

B. DMA logic (Sheet 3)

C. Timing, control, status, and self-test logic (Sheet 4)

The crystal-controlled time base for the coupler is established by circuit 3E-8 (see Sheet 4). The 12-megahertz output of 3E-8 is divided by two by flip-flop 4E-9 to generate symmetrical 167-nanosecond clock signals SCLK− and XCLK−.

Self-test latch 20B-9 controls the DIAGnostic light and supplies the STLGOOD+ signal via the UNIBUS status register to the D Bus. A loss of power to the coupler or a self-test failure (DCOK+ goes false) immediately clears 20B-9. Flip-flop 20B-9 sets if the coupler passes self test (CCROK− pulses).

The microprocessor provides control signals to the UNIBUS over the Y Bus via register 15F. The register contents are updated by register clock LXR4−. The register outputs are connected to the various control lines (INTR+, TBR+, etc.) unless a RESET occurs. The status of the UNIBUS control lines to the coupler, as well as internal coupler status conditions, are stored by tri-state register 16F and connected to the microprocessor D Bus by XSD3.

The controller interrupt logic is shown on Sheet 2 and the relationship of the logic signals is illustrated by Figure 5-3. Numbers preceding terms relate to the drawing where the terms originate.

Note that both interrupts and NPR transfers must be preceded by a bus request sequence to permit the coupler to become bus master. Some of the bus request signal lines are shown on Sheet 5 with the NPR logic. NPR timing is shown in Figures 5-4 and 5-5.

For a detailed discussion of UNIBUS timing and control, review the "UNIBUS THEORY AND OPERATION" section of the appropriate DEC handbook.

Microprocessor

The microprocessor comprises the following major elements:

A. 256 X 8 RAM

B. 256 X 8 ROM

C. Condition code and bit test multiplexers

D. 8-bit Arithmetic and Logic Unit (ALU)

E. 1K X 56-bit control store

F. 2910 sequencer

G. Vector register

H. Source, destination, and pulse decode logic

These elements are interconnected to perform the control, timing, error, and data manipulation functions of the coupler. Information is transferred among the elements over internal tri-state buses (primarily the Y and the D Buses).

A microprocessor functions under control of instructions stored in Read Only Memory (ROM or PROM). These instructions are called microinstructions because it often requires a series of them to perform a function. All of the microinstructions are called firmware, since once stored in the PROM they cannot be altered. To understand the function of a microprocessor, please refer to "The Microprogramming Handbook" from Advanced Micro Devices, Inc., 901 Thompson Place, Sunnyvale, California 94086. Detailed technical descriptions of the 2901 four-bit bipolar microprocessor slice and of

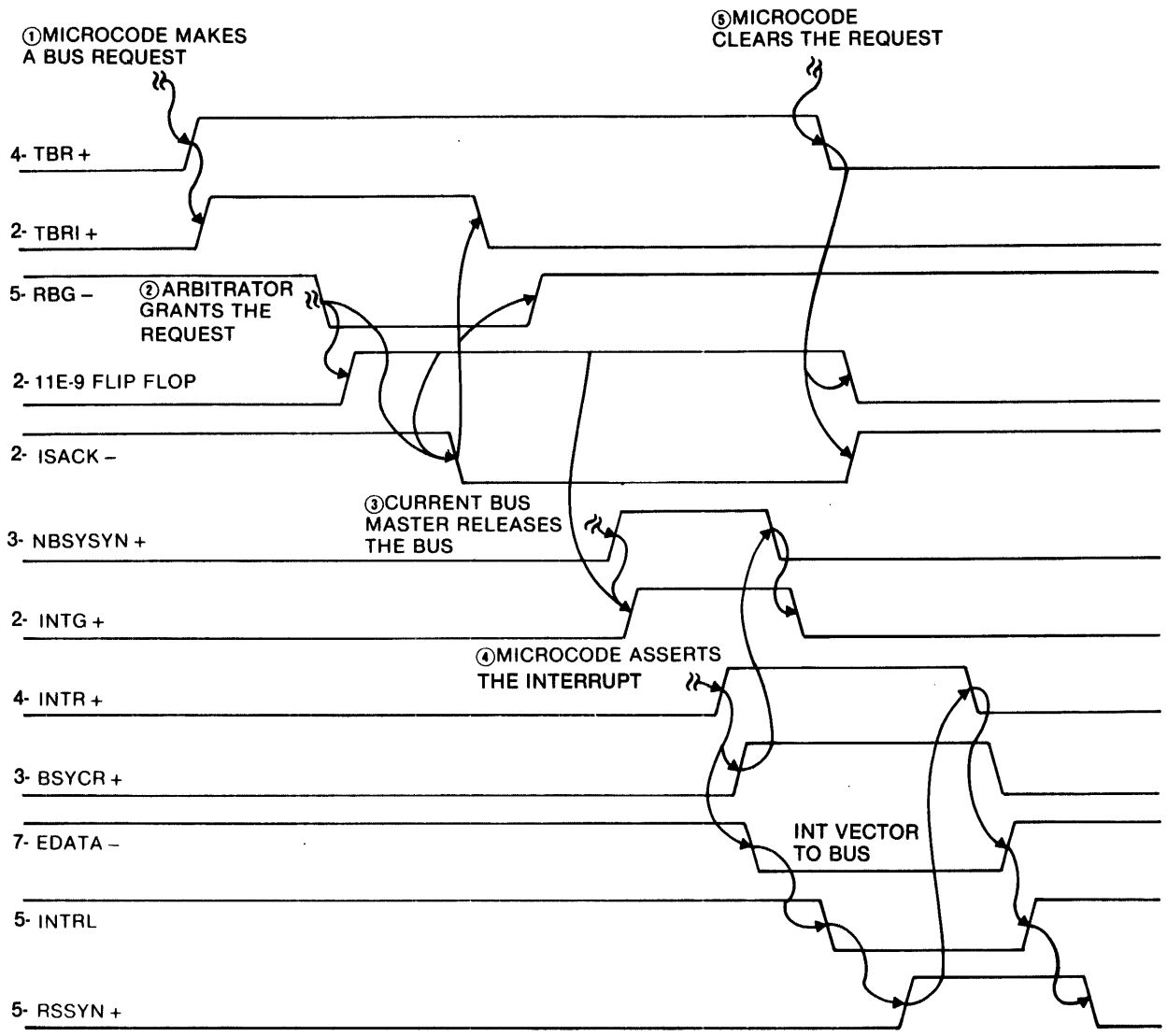


Figure 5-3. Interrupt Timing

the 2910 sequencer are given in Advanced Micro Devices "AM2900 Family Data Book". These two elements are the major components of the coupler.

256 X 8 RAM (Sheet 13)

This RAM is the dynamic "operating conditions" storage section of the coupler. Tables 5-3 and 5-4 show the contents of the RAM. The first 16 locations are reserved for the TSBA and TSSR register contents for each of the four tape drives that can be connected to the coupler.

Hex location 1F is the transport control register (TCTL), which is an image of the transport control register contents (18B, Sheet 14).

Hex locations 20-27 contain the contents of the last characteristics packet received.

Hex locations 30-37 are the NPR data buffer between the coupler FIFO and main memory.

The next 64 locations (Units 0-3 Context) contain the current status packet memory address, operating condition, and status packet words for all four tape drives that could be connected to the coupler.

Address register/counters 10C and 11C control the RAM address lines. The starting address of the section of RAM to be written/read is loaded into the address register from the Y Bus by LXRE—. Signal INCRAM increases the address count in the register based upon the area of RAM to be accessed.

The RAM consists of circuits 8C and 9C. The RAM data lines are connected to D-Bus tri-state Driver 9B.

Signal LXRF— writes the contents of the Y Bus into the addressed RAM location. Signal XSDF— gates the contents of the addressed RAM location to the D Bus.

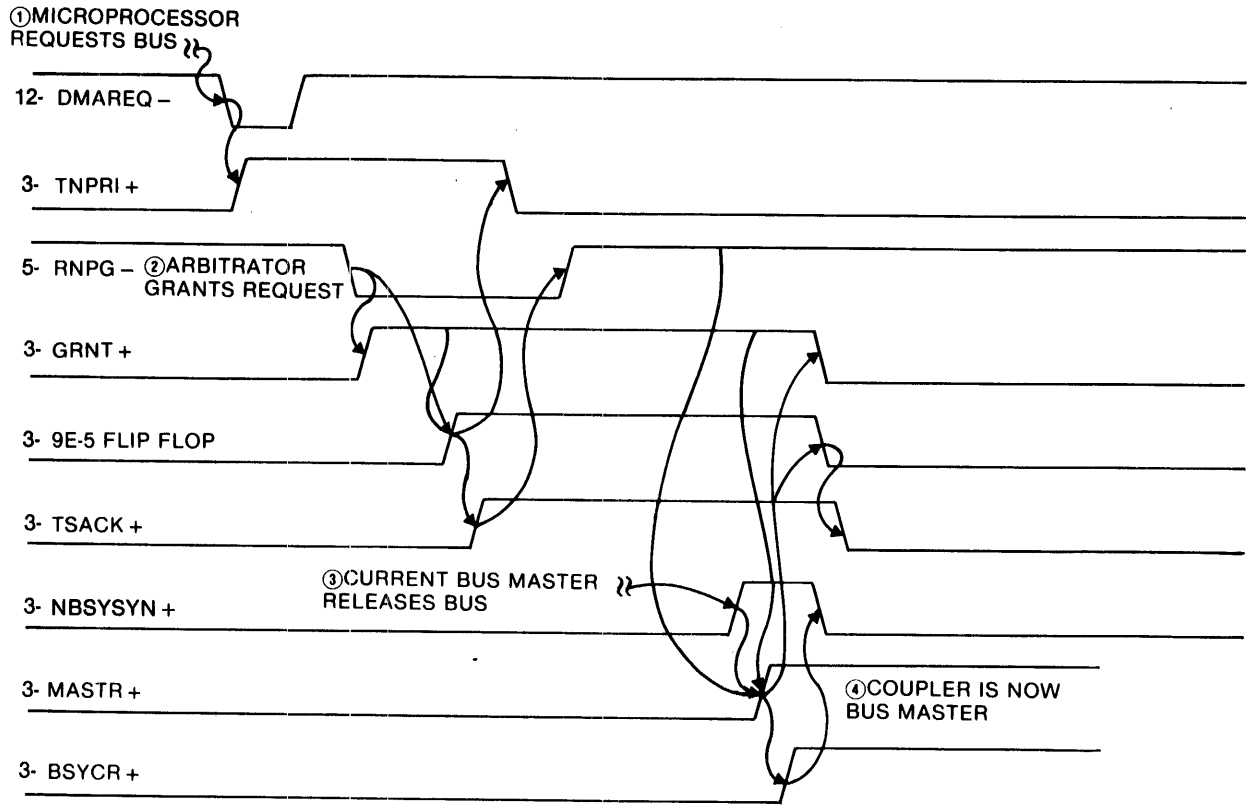


Figure 5-4. NPR Request Timing

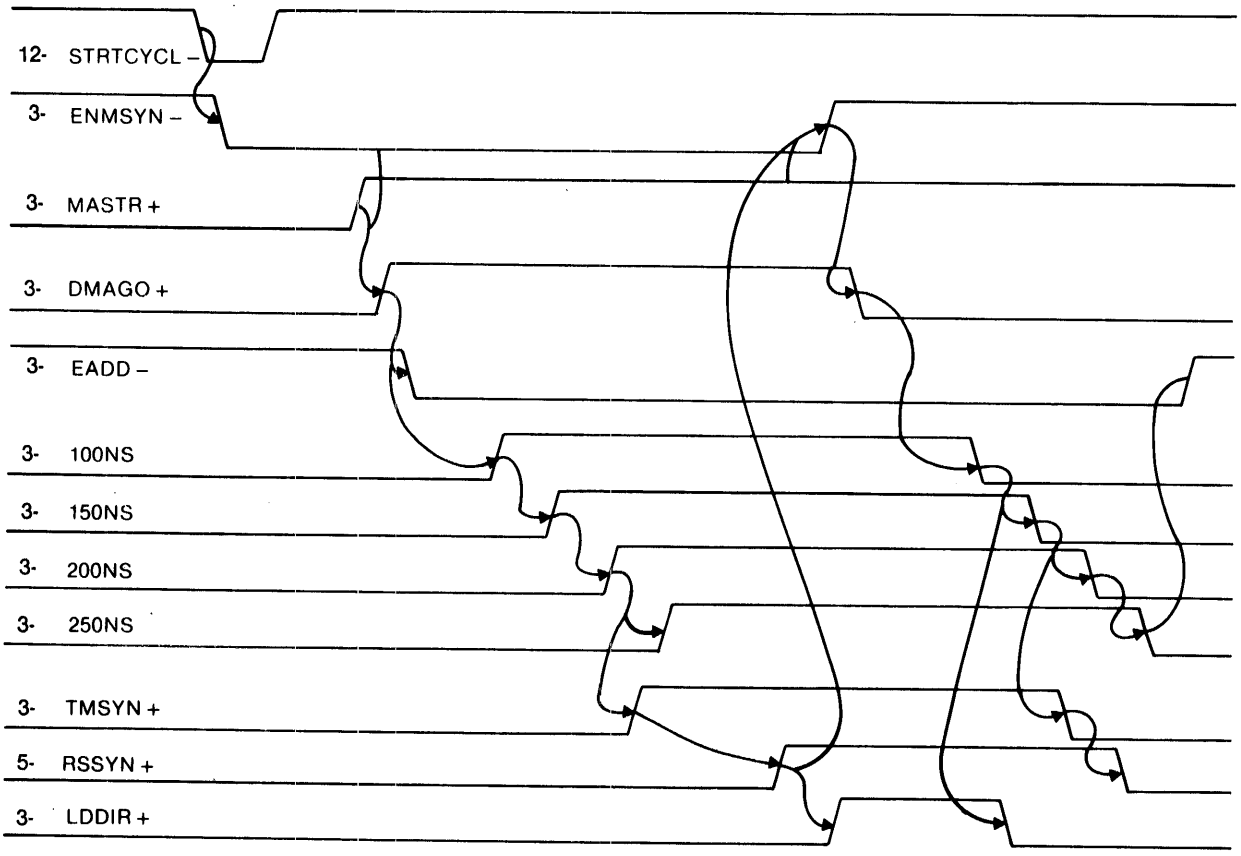
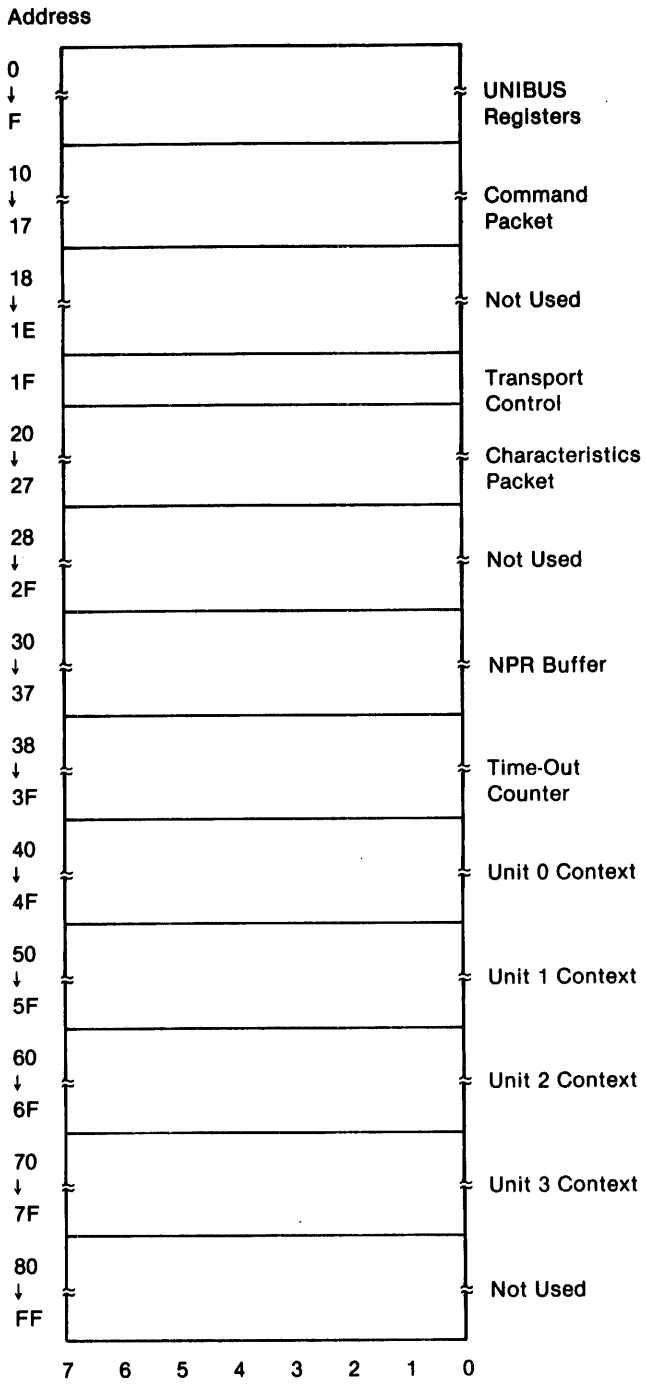


Figure 5-5. Data Transfer Timing

Table 5-3. RAM Map



256 X 8-Bit ROM (Sheet 13)

ROM 3D is the "data look-up table" of the microprocessor It contains constants and mask bits that permit rapid manipulation of tape subsystem information by the 2901 ALU. The tri-state ROM contents are typically used during:

A. Command decoding,

B. Error logging,

C. Command/interrupt queuing,

D. Logical unit handling (address queuing, etc.),

ROM address register 2D is loaded from the Y Bus by LXRD−. The contents of the addressed location are gated to the D Bus by XSDE−.

Controller Test Logic (Sheet 8)

The purpose of this logic is to select one signal during conditional-type instructions to the CCE− input of the microsequencer. The eight conditions tested are gated to the CCE− output of test function multiplexer 1E by microcode field CR4-1 through CR4-3. The conditions that can be tested for are:

A. A previously selected bit from the Y Bus (ALU output)

B. ALU result = zero

C. ALU result = not zero

D. ALU carry out

E. ALU no carry out

F. CPU programmed I/O request or interrupt grant received

G. NPR cycle complete

H. True (force conditional test to pass)

Y Bus bits to be tested are selected by microcode field CR1-0 through CR1-2, which controls multiplexer 6C. The selected bit is latched in register 2E by SCLK at the end of an instruction. Register 2E also stores the result = zero and carry out conditions of the ALU.

The first five conditions must be stored at the end of a prior instruction before being tested by a conditional instruction. Latch 2E stores the conditions when microcode bit CR3-1 enables the latch. The last three conditions can be tested at any time.

The flip flops in both the slave request and NPR cycle-complete circuits guarantee that the external signals associated with these events are synchronized with the system clock.

2910B Microprocessor ALUs (Sheet 11)

The microprocessor ALUs comprise two AM2901B four-bit, bipolar, microprocessor-slice integrated circuits connected in cascade to perform data manipulation on 8-bit bytes. A description of the operation of this device is given in the "AM2900 Family Data Book".

Table 5-4. DU142 Unit "N" Context (4 Total)

RAM ADDRESS (HEX)	7	6	5	4	3	2	1	0	
x0	A7	A6	A5	A4	A3	A2	A1	A0	MESSAGE PACKET POINTER ADDRESS AND CHARACTERISTICS MODE
x1	A15	A14	A13	A12	A11	A10	A9	A8	
x2	ESS	ENB	EAI	ERI	MBR	VCK	A17	A16	
x3	ATTN	ONL	RWD QUEUE	RWD ING	DCK	EOT	OLD CMD REV	OLD CMD WRT	TRANSPORT CONTROL/STATUS
x4				MESSAGE CODE					MESSAGE PACKET
x5	ACK						CLASS CODE		HEADER WORD
x6	RBPCR LOW								RESIDUAL FRAME COUNT
x7	RBPCR HIGH								
x8	MOT	ONL	IE	VCK	PED	WLK	BOT	EOT	XSTAT0
x9	TMK	RLS	LET	RLL	WLE	NEF	ILC	ILA	
xA							HER	PAR	XSTAT1
xB	DLT								
xC									XSTAT2
xD	OPM								
xE		OPI	REV		DCK			RIB	XSTAT3
xF									

The D Bus supplies external data to the ALUs; output data from the ALUs appears on the Y Bus. Control inputs to the ALUs are from the control store and are shown in Table 5-5. Table 5-6 lists the outputs of the ALUs.

Microsequencer (Sheet 9)

The control processor (also referred to as the microsequencer) is an AM2910 microprogram control circuit described in "The AM2900 Family Data Book". It controls the sequence of execution of microinstructions stored in the control store.

Control store output address lines CSA0 through CSA9 select one of 1024 locations in the control store. Bits 4 through 7 of field five (CR5) supply instruction codes to the microsequencer. Any one of 16 instructions can be selected. The conditional instructions make pass/fail path decisions based on the low/high level of the CCE− input. The instructions select the next address for the control store. The primary sources of addresses are as follows:

Table 5-5. Control Inputs to 2901B ALU

ALU Mnemonic	Signal Source	Definition
A0-A3	Control Store CR1-4 to CR1-7	Address inputs to the A port of the 16-byte ALU memory.
B0-B3	Control Store	Address inputs to the B port of the 16-byte ALU memory.
I0-I8	Control Store	Instruction control lines: lines 0-2 select the data source to the ALU; lines 3-5 select the ALU function to be performed; lines 6-8 determine the destination of the output of the ALU (within the ALU) and the source of data supplied to the Y (output) bus.
CIN	Control Store	Carry input to ALU. Used during arithmetic operations. Can be forced O/I or Latched Carry Out from prior result.
CP	Crystal Oscillator	167 nanosecond clock to ALUs.

Table 5-6. 2901B ALU Outputs

Mnemonic	Definition
Zero+ (F = 0)	Indicates result of ALU operation is Zero.
COUT+	Indicates a "carry out" of ALU.
RAM0	Least significant bit of RAM right/left shift multiplexer.
RAM3	Most significant bit of RAM right/left shift multiplexer.
Q0, Q3	Q Register right/left shift ports.
Y0-Y7	8-bit output of ALU, Y0 is LSB.

A. The next sequential instruction (PC+1)

B. A counter/register within the microsequencer

C. A five-word LIFO stack within the microsequencer

D. Branch address directly from control store bits 0-7 of field five (CR5), CR4-0, and CR6-7

E. Microvector address register ID

Control Store (Sheet 10)

The control store contains the firmware instructions that control the operation of the coupler. It comprises seven 1024 X 8-bit Programmable Read-Only-Memory (PROMs) identified as 1A, 2A, 3A, 4A, 5A, 6A, and 7A. The PROMs have a pipeline register at the output. The seven PROMs produce a 56-bit instruction word divided into seven 8-bit fields.

The contents of the control store are addressed by the microsequencer and strobed into the pipeline register by the SCLK clock. The contents of the pipeline register (CR1-0/7 through CR6-0/7 and literal D00/07) are routed throughout the logic of the coupler.

Signal VEC+ disables the CR5 PROM outputs while the microvector address register is connected to the control processor. Signal XSDA− connects the contents of literal PROM 7A to the tri-state D Bus.

Microvector Address Register (Sheet 9)

This register is loaded with the contents of the Y Bus by signal LXRB−. If conditional testing makes the VEC+ output of the microsequencer true, the output of register 1D supplants CR5 bits 0-7 as direct address inputs to the microsequencer. Note that VEC+ disables the tri-state outputs of PROM 2A.

Source, Destination, and Pulse Decode Logic (Sheet 12)

This logic comprises decoders enabled by bits of control registers CR6 and CR3 and the XCLK signal. The decoder outputs synchronize interaction of the various elements of the coupler.

Destination decoders 4D and 5D generate outputs that load registers with data from the ALU Y Bus. See Table 5-7. Source decoders 6B and 7B connect the outputs of registers to the ALU tri-state input D Bus. See Table 5-8. The terms "source" and "destination" refer to the microprocessor ALU: the source of data to the ALU, and the destination of data from the ALU.

Control pulse decoder 7C generates pulses that initiate or terminate a function. The pulses primarily clock, direct set, or direct clear control flip-flops.

Note that the effect or function of each line of the registers is labeled on the logic drawing.

Peripheral Interface

The peripheral interface comprises the following logic sections:

A. Tape drive configuration switches

B. Tape drive control, command, and status logic

C. FIFO data buffer controller

D. FIFO data buffer and tape drive data I/O logic drivers and receivers

Tape Drive Configuration Switches (Sheet 13)

Switch PAC 20C permits the operator to:

A. Select the floating interrupt vector base address for drives 1 through 3 (S1-S7),

B. Set the number of words to be transferred during each DMA cycle (S8), and

C. Set the number of drives addressed by the system (S9, S10).

See Table 2-5 for a description of the switch settings.

The switch settings are gated to the D Bus via tri-state buffers 20D and 19D by signals XSD9− and XSDD−. Buffer 19D also gates selected tape drive status bits to the D Bus.

Table 5-7. DU142 External Destinations

	7	6	5	4	3	2	1	0	
0	U-BUS HIGH DATA								
1	U-BUS LOW DATA								
2	U-BUS ADDRESS HIGH								
3	U-BUS ADDRESS LOW								
4	INTR	BR	SSYN	ENA FIFO	C1	C0	UNIBUS ADDRESS A17	A16	UNIBUS CONTROL
5	FLOL	FOFL	FREW	EDIT	ERASE	WFM	REV	WT	TRANSPORT COMMAND
6	FIFO DATA								
7	GO	RTH1	RTH2	FEN	FAD	DEN	TAD 1	TAD 2	TRANSPORT CONTROL
8									
9									
A									
B	VECTOR REGISTER								
C	LIGHT OFF PULSE								
D	ROM ADDRESS								
E	RAM ADDRESS								
F	RAM DATA								

Control, Command, and Status Logic (Sheet 14)

This logic comprises registers that store the control (18B) and command (17B) signals to the tape drives and gate status signals from the drives to the D Bus (14D, 15D).

Signal LXR7 stores the contents of the Y Bus in 18B; LSR5 stores the contents of the Y Bus in 17B.

Tape drive status is gated to the D Bus during XSD7 and XSD8 times. Transitory signals, such as file mark, hard or corrected error, end of tape mark, etc., are stored by latches 19C-7, 19C-13, 13C-5, and 13C-9.

The relationship of the control, command, and status signals is described in the "Interface Description" section of the tape drive manual.

FIFO Controller (Sheet 15)

The FIFO controller supplies addresses and control signals to the FIFO data buffer. The FIFO buffer is a RAM between the tape drive read/write data lines and the NPR buffer in the 256 X 8 RAM. All data between the CPU and tape drives passes through the FIFO and NPR buffer.

The FIFO controller logic is enabled by the ENAFIFO+ signal. FIFO address circuit 15C is basically two 12-bit, wrap-around counters, used as pointers, multiplexed internally to produce the FAD0-FAD11 address lines to the FIFO RAM. The input-to-FIFO counter is advanced by SI; the ouptut-from-FIFO counter is advanced by SO. After SI is clocked, FIFWT− is asserted. After SO is clocked, FIFRD− is asserted. FIFWT− means "write data into FIFO from either tape or the Y Bus." FIFRD− means "read data from FIFO to either tape or the D Bus."

S-R latches are associated with the SO and SI inputs. Flip flop 19C-9 and the associated gates control SO; flip flop 19C-4 and the associated gates control SI.

When reading data from tape, signal FRSTR causes 19C-4 to set and SI to advance the associated address counter and generate FIFWT−. LXR6− sets 19C-4 when the FIFO is loaded from the NPR data buffer. 19C-4 is cleared by FIFWT−, delayed by C2 and R8.

Table 5-8. DU142 External Sources

0	SLAVE ADDRESS								
1	U-BUS HIGH DATA BYTE								
2	U-BUS LOW DATA BYTE								
3	BG	MASTR	PAR ER	STL GOOD	ADD OVFL	SSYN	C1	C0	UNIBUS STATUS
4	FIFO DATA								
5									
6									
7	FMK	ONL	FIFO IN ACT	FIFO OUT ACT	FIFO EMPTY	FIFO FULL	HER	RWS	TRANSPORT/FIFO STATUS #1
8	DATA LATE	TRDY	FBSY	DBSY	DENS CHK	FILE PROT	BOT	EOT	TRANSPORT/FIFO STATUS #2
9	SW 7	SW 6	SW 5	SW 4	SW 3	SW 2	SW 1	SW 0	SWITCH REGISTER #1
A	LITERAL								
B									
C									
D	PE	EOT FLOP	CER	0	SW 9	SW 8		OPI	
E	ROM DATA								
F	RAM DATA								
	7	6	5	4	3	2	1	0	

19C-9 is set by either FDWDS (write to tape from FIFO) or XSD4− and SCLK− (write to DMA data buffer from FIFO). FIFRD−, delayed by C1 and R7, clears 19C-9.

Conditions OUTACT+, INACT+, FULL+, EMPTY+, and DATLAT− are FIFO status signals gated to the D Bus for monitoring by the microprocessor.

Note that the SI and SO inputs are enabled after the trailing edge of the clock signals to the latches.

The Data Late (DATLAT−) signal is generated if either 16E-5 or 16E-3 sets. These flip-flops set if either write or read strobes occur before the previous write or read strobe was serviced.

FIFO Data Buffer (Sheet 16)

The 4096 X 8-bit FIFO (15B and 16B) buffers all data between the tape drive and the NPR buffer in the 256 X 8 microprocessor RAM. (See Note 1.)

Circuit 14B is a parity generator/checker. Odd parity is generated to the output buffers; if even parity is detected at the input to the FIFO, PARER+ flip-flop 19B-9 sets. Signal FIFRD− clocks flip-flop 19B-5 causing odd parity to be generated during data transfers to tape. During this time, the PARER+ flip flop is disabled.

The following sequence occurs during data transfers to tape:

A. ENAFIFO+ signal asserted;

B. LXR6− clocks Y-Bus data (from NPR RAM) into register 12B and clocks the SI input to FIFO controller 15C;

C. FIFWT− enables 12B tri-state outputs to FIFO data lines and writes data into the FIFO location addressed by FAD0-11;

D. Sequences B through D repeat until the sequence is terminated.

E. Before the preceding sequence, signal FGO was issued to the addressed tape drive. Tape motion was started and, after the tape is up to speed (FDBY asserted), the FDWDS strobe is received.

F. FDWDS clocks the SO input to FIFO controller 15C.

G. Address lines FAD0-FAD11 select the first FIFO location that had been loaded with data.

H. Trailing edge of FIFRD− clocks the FIFO data into register 10B and clocks parity bit flip flop 19B-5.

I. FIFO input/output transfers continue concurrently (see Note 2) until: 1) word count is zero, which terminates input transfers and 2) EMPTY+ is detected, which terminates output transfers.

NOTES

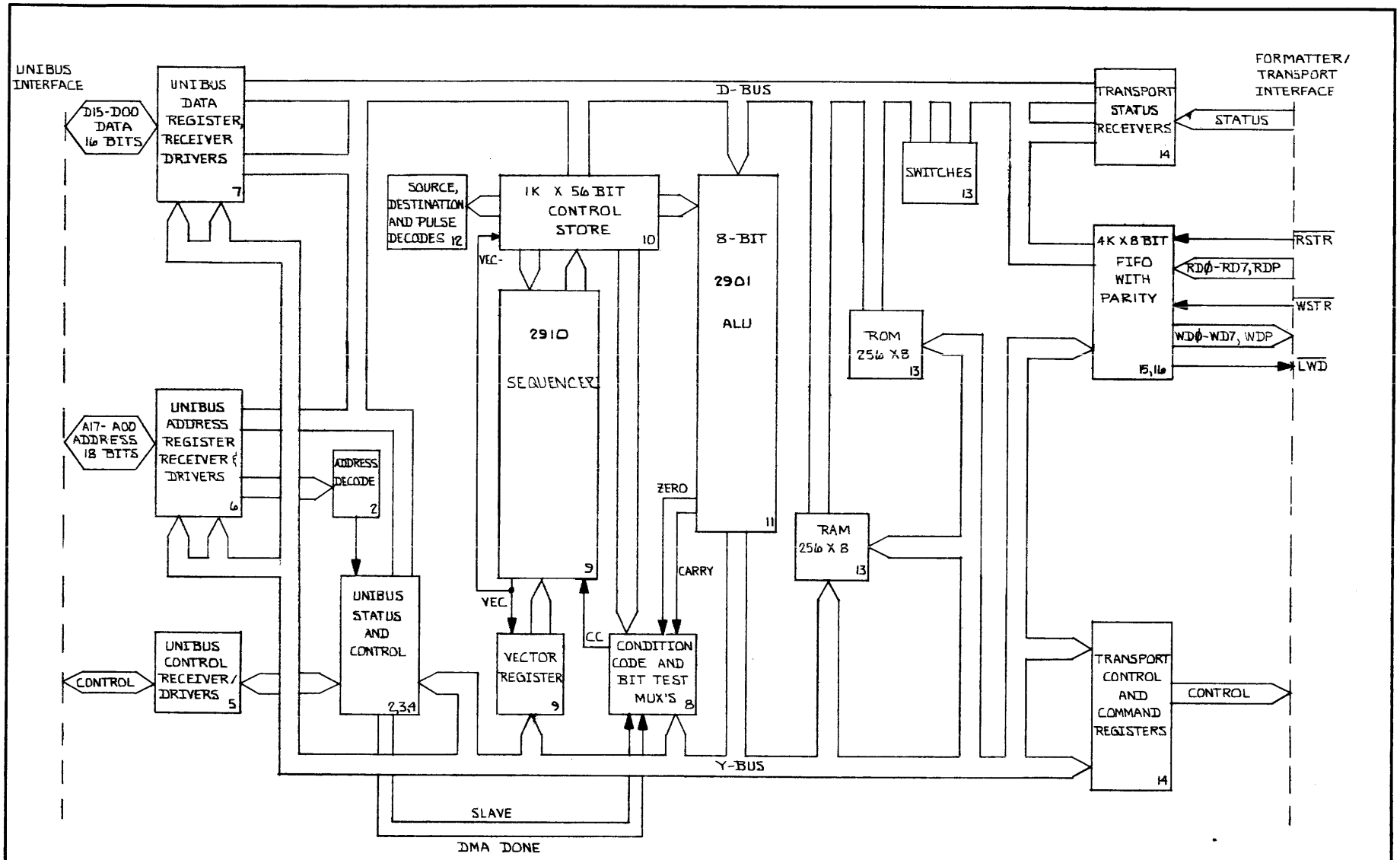
1. *The total data buffer size in the coupler is actually 4106 bytes: 4096 byte FIFO buffer, input and output FIFO registers, and an eight-byte buffer in the 256 X 8 RAM.*

2. *The FIFO input and output transfers are asynchronous with respect to each other. Transfers appear to be able to occur simultaneously as far as the 2910/2901 microprocessor and tape interface are concerned. However, FIFO controller 15C treats its SI and SO inputs as "requests for transfers" and sorts them out internally to allow only one transfer at a time, in case SI and SO occur simultaneously.*

   Controller 15C does this by selecting only one of the requests for service, gating the associated internal address counter to the FAD0-11 address lines, and responding with the appropriate FIFWT− or FIFRD− pulse. To complete the transfer, the internal address counter is advanced and the 19C flip-flop that triggered the SI or SO input is cleared.

   The basic system criteria is that the FIFO must always "stay ahead" of the tape interface during data transfers. Therefore, when reading tape, FIFO data must be transferred into computer memory faster than data is being received from tape. If not, the FIFO will fill up and overflow. When writing to tape, data must be supplied to the FIFO from computer memory faster than it is being written to tape. If not, the FIFO will empty too soon and underflow. Overflow or underflow will cause the data late (DATLAT−) error status to be generated.

During data transfers from tape, RSTR− strobes tape data into register 13B. WRT+ is false in the read mode. Therefore, the output of 12B is disabled and the output of 13B is connected to the FIFO data lines and written into FIFO by FIFWT−. The addressed contents of the FIFO are connected to the tri-state D Bus lines by XSD4− after register 11B is loaded with FIFO data by FIFRD−.



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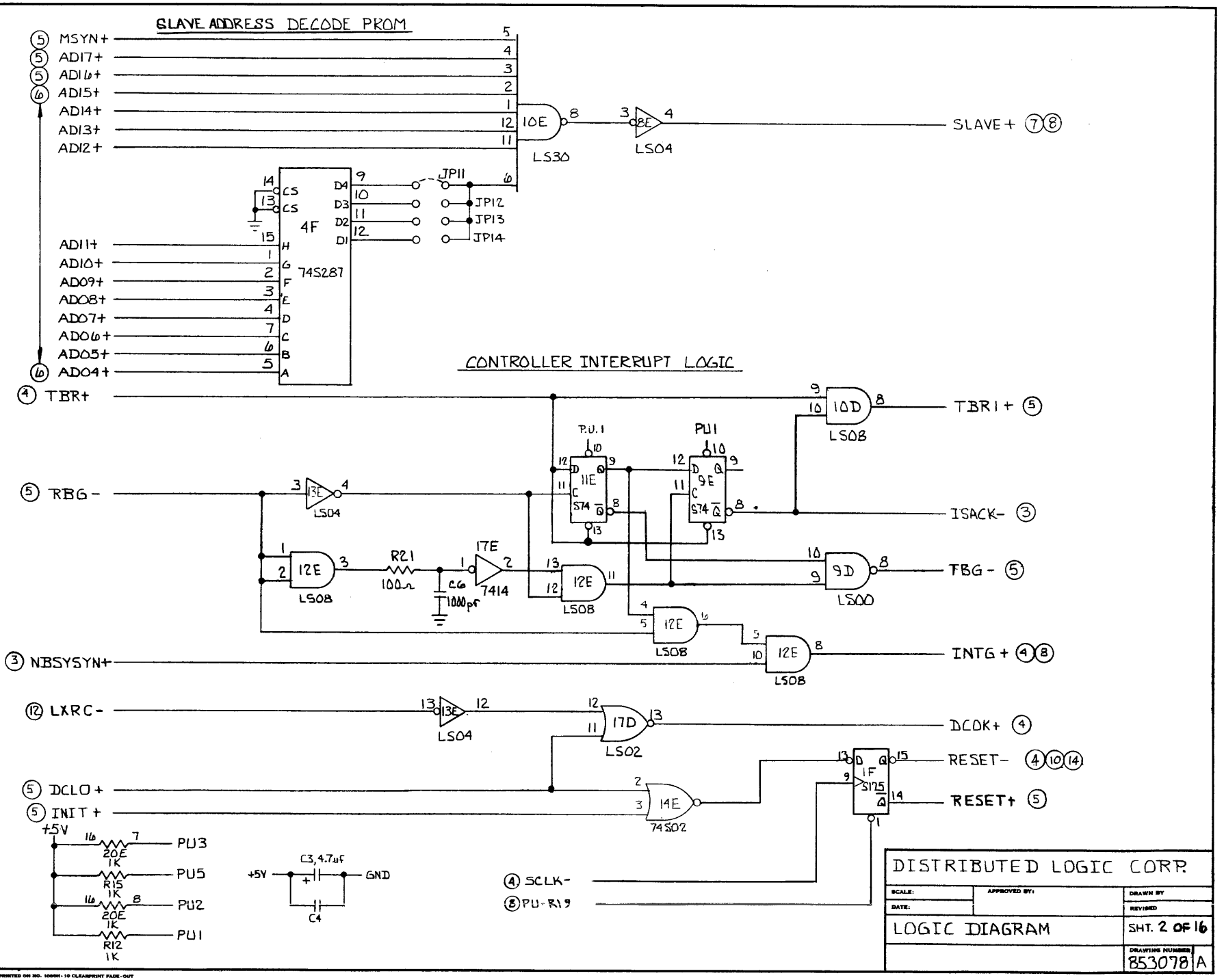
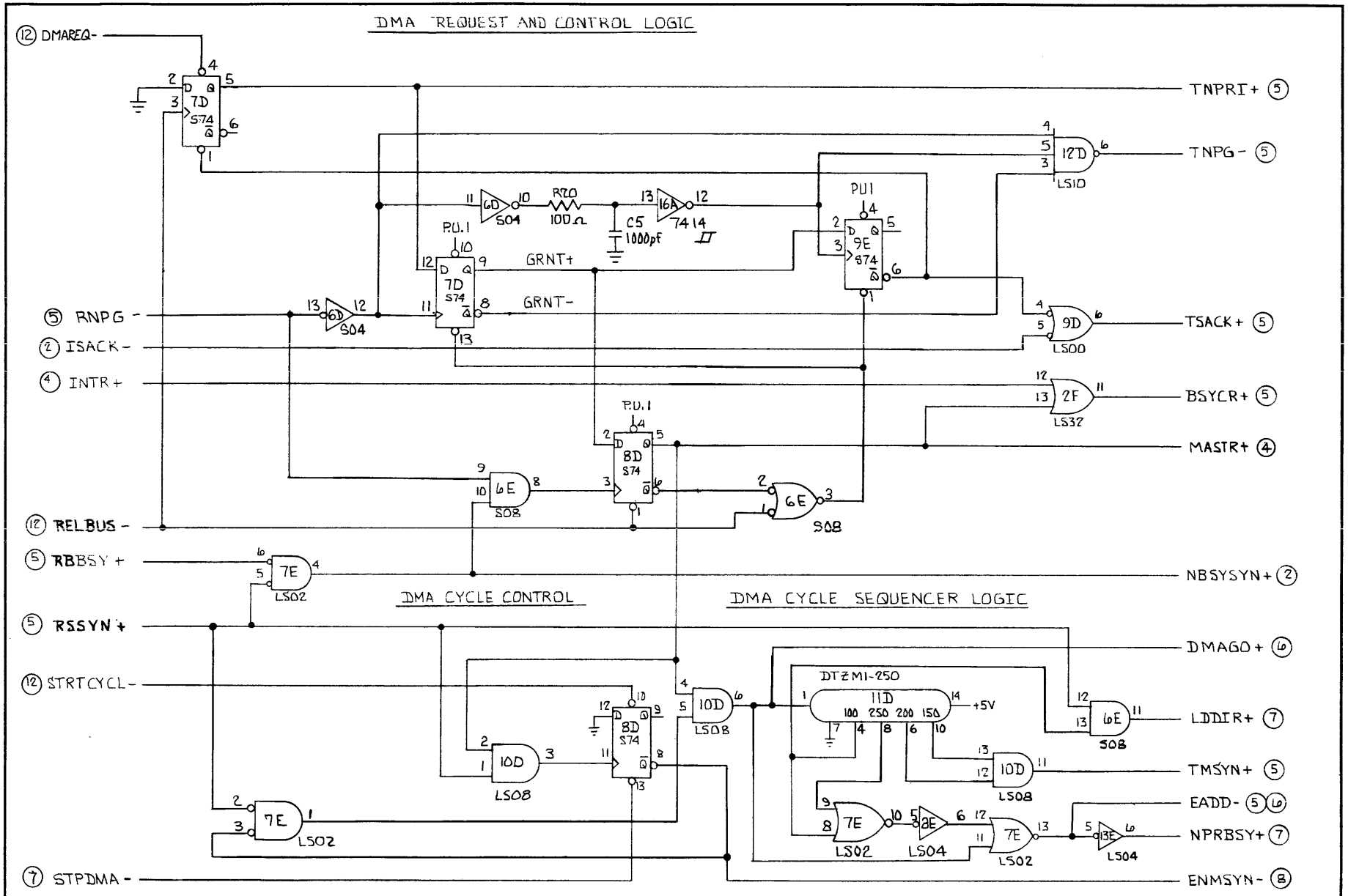
	DATE:	REVISED
DU142	LOGIC DIAGRAM	SHT 1 OF 16
USED ON		DRAWING NUMBER 853078 A

17 X 22 PRINTED ON NO. 1000H-10 CLEARPRINT FADE-OUT


SLAVE ADDRESS DECODE PROM
MSYN+
ADI7+
ADI6+
ADI5+
ADI4+
ADI3+
ADI2+
ADI1+
ADI0+
AD09+
AD08+
AD07+
AD06+
AD05+
AD04+
10E
LS30
8E
LS04
SLAVE+ 7 8
4F
74S287
JPI1
JPI2
JPI3
JPI4
CONTROLLER INTERRUPT LOGIC
TBR+
10D
LS08
TBRI+ 5
P.U.1
PU1
11E
9E
ISACK- 3
RBG-
13E
LS04
12E
LS08
R21
100Ω
C6
1000pf
17E
7414
9D
LS00
TBG- 5
INTG+ 4 8
NBSYSYN+
LXRC-
17D
LS02
DCOK+ 4
DCLO+
INIT+
14E
74S02
1F
S175
RESET- 4 10 14
RESET+ 5
+5V
20E
1K
R15
R12
PU3
PU5
PU2
PU1
C3, 4.7uf
C4
GND
SCLK-
PU-R19
DISTRIBUTED LOGIC CORP.
SCALE:
APPROVED BY:
DRAWN BY
DATE:
REVISED
LOGIC DIAGRAM
SHT. 2 OF 16
DRAWING NUMBER
853078 A



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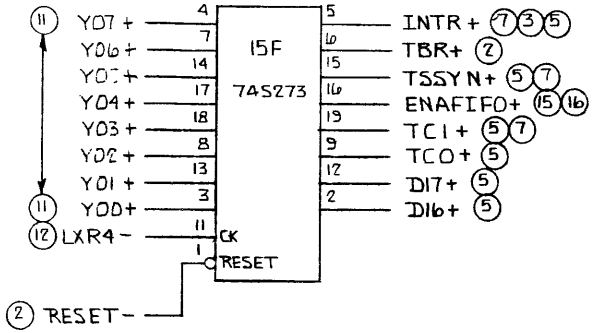
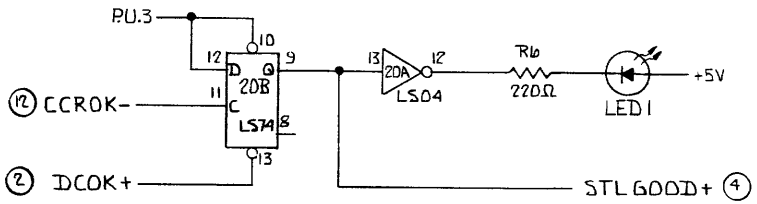
LOGIC DIAGRAM		SHT. 3 OF 16
		DRAWING NUMBER 853078 A

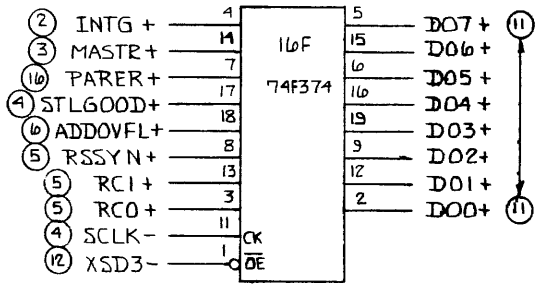
UNIBUS CONTROL



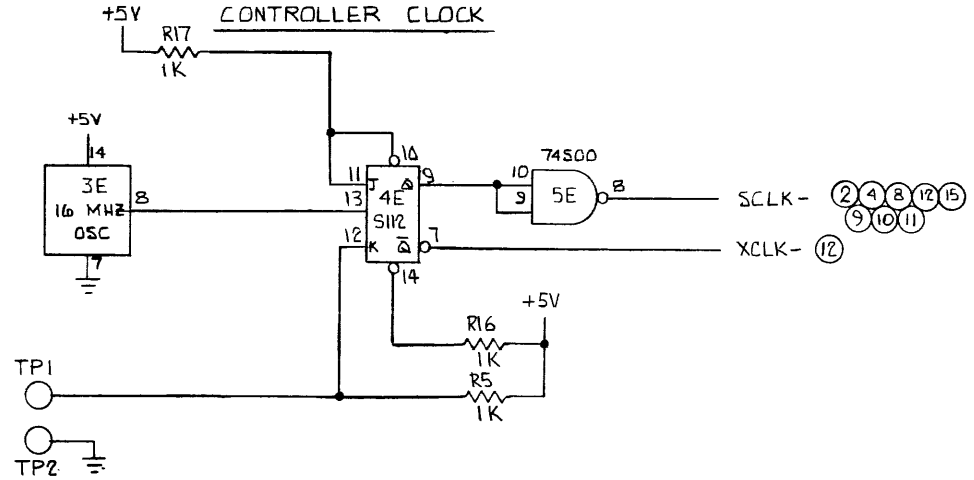
SELF TEST OK INDICATOR



UNIBUS STATUS



CONTROLLER CLOCK



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LOGIC DIAGRAM		SHT. 4 OF 16
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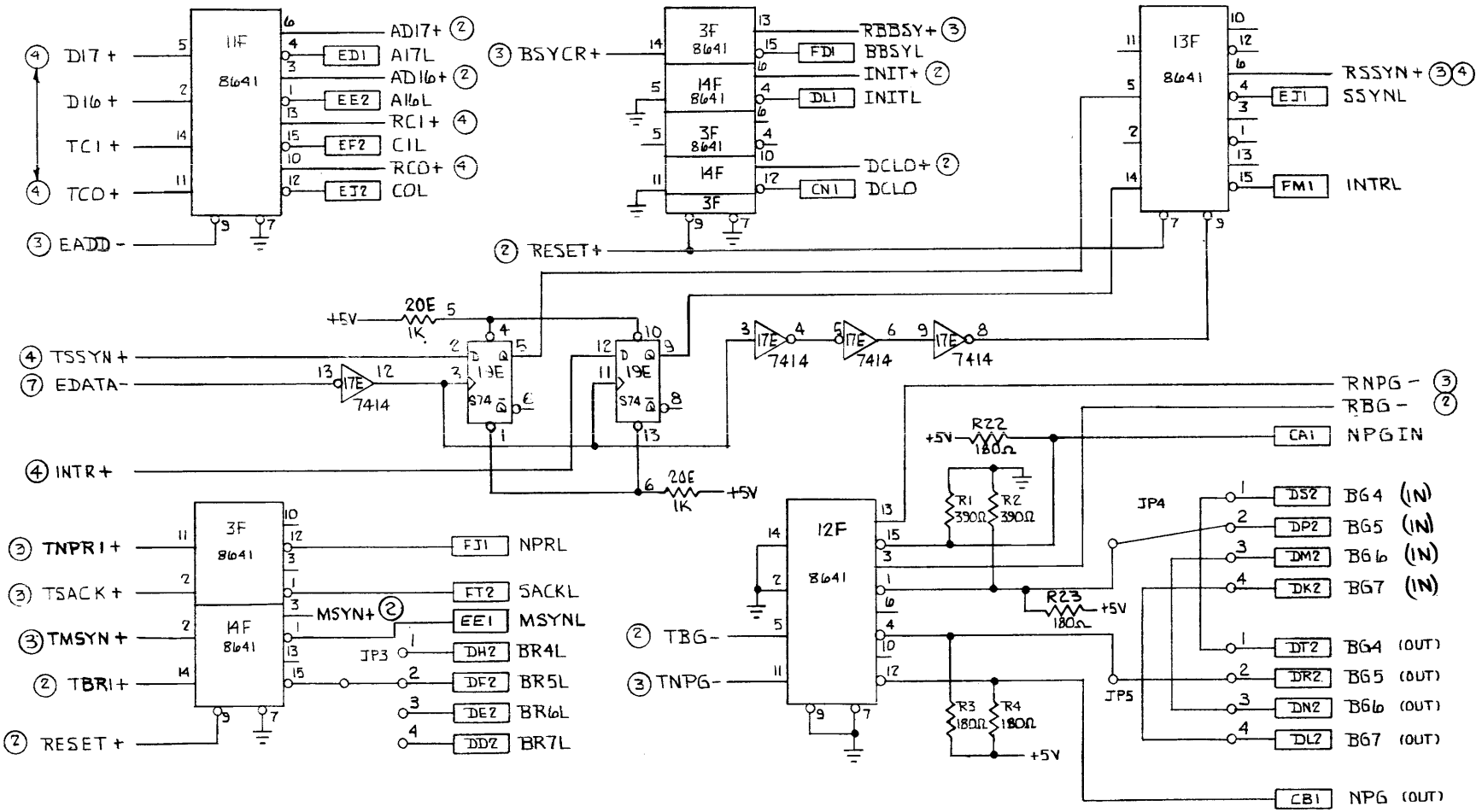
UNIBUS CONTROL SIGNALS TRANSCEIVERS



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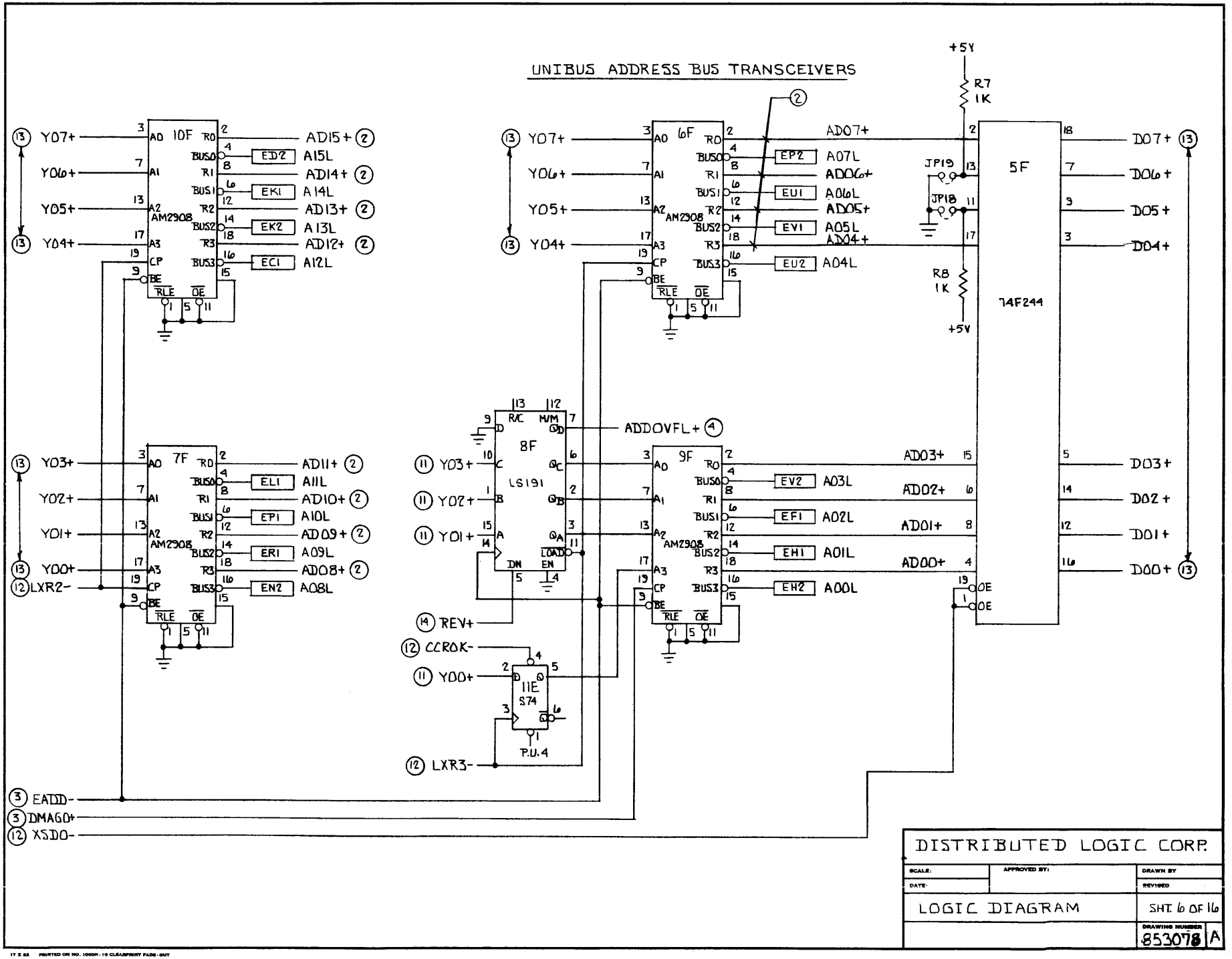
LOGIC DIAGRAM		SHT 5 OF 16
		DRAWING NUMBER 853078 A



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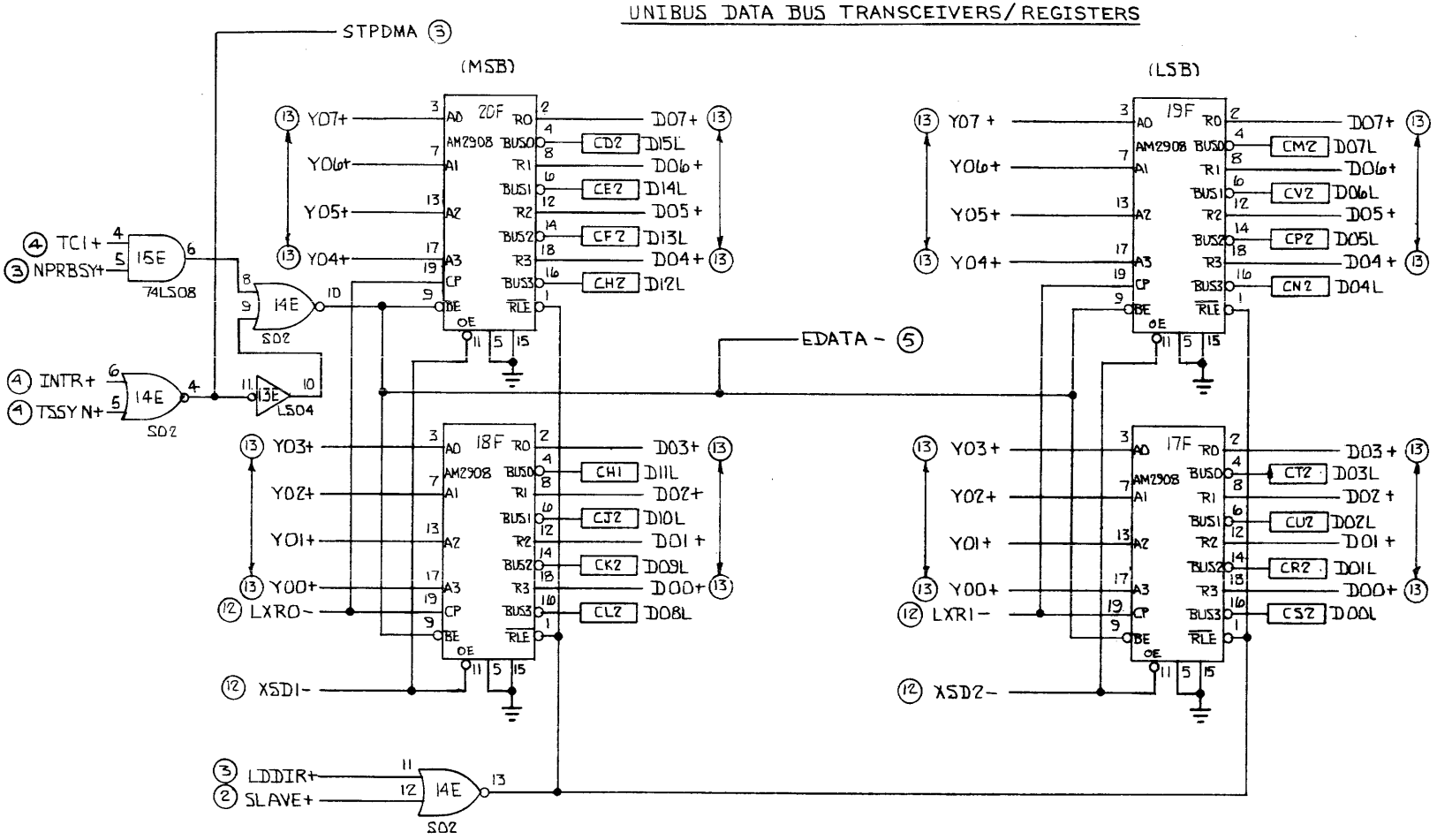
LOGIC DIAGRAM		SHT. 6 OF 16
		DRAWING NUMBER 853078 A

UNIBUS DATA BUS TRANSCEIVERS/REGISTERS



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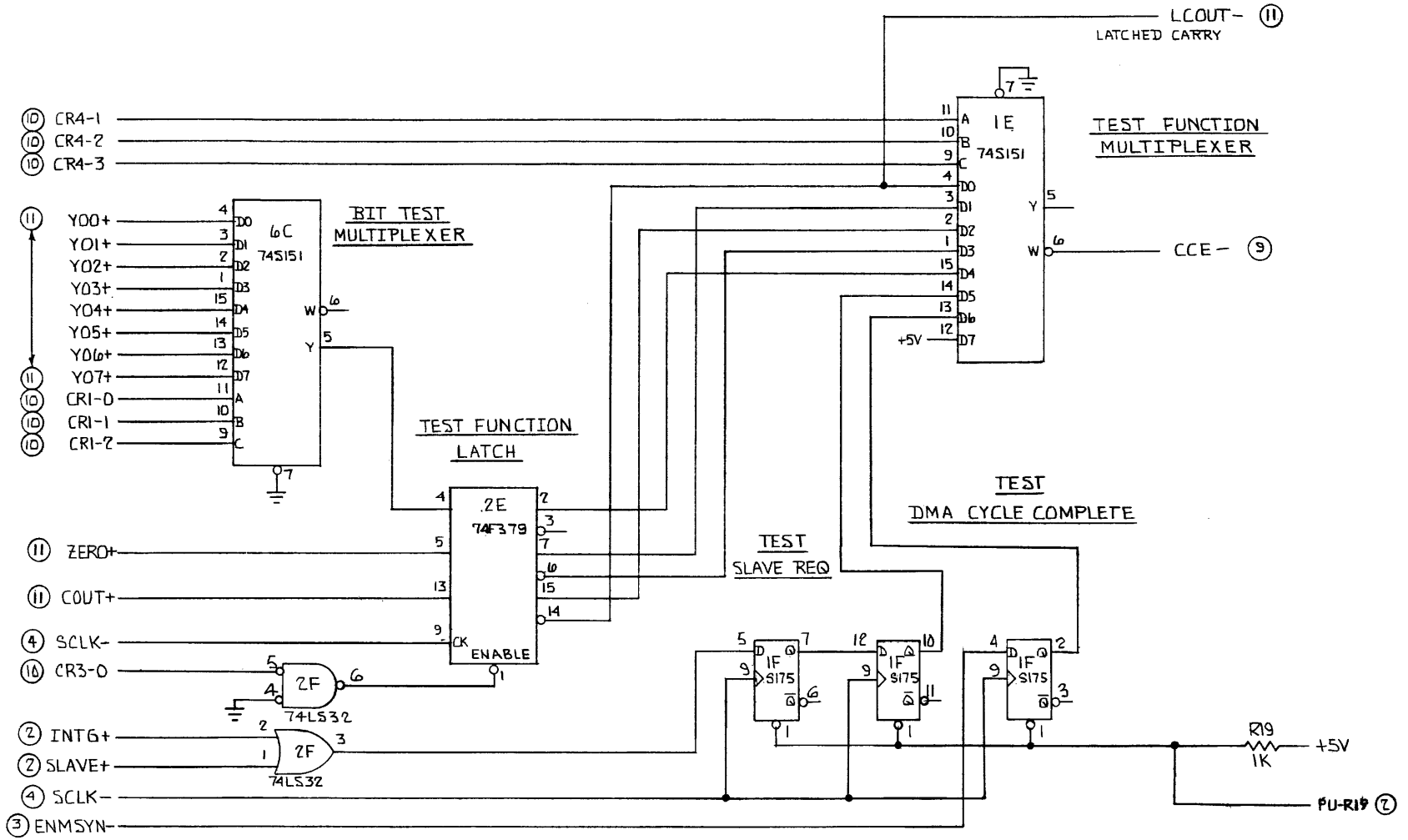
LOGIC DIAGRAM.		SHT 7 OF 16
		DRAWING NUMBER 853078 A

CONTROLLER TEST LOGIC



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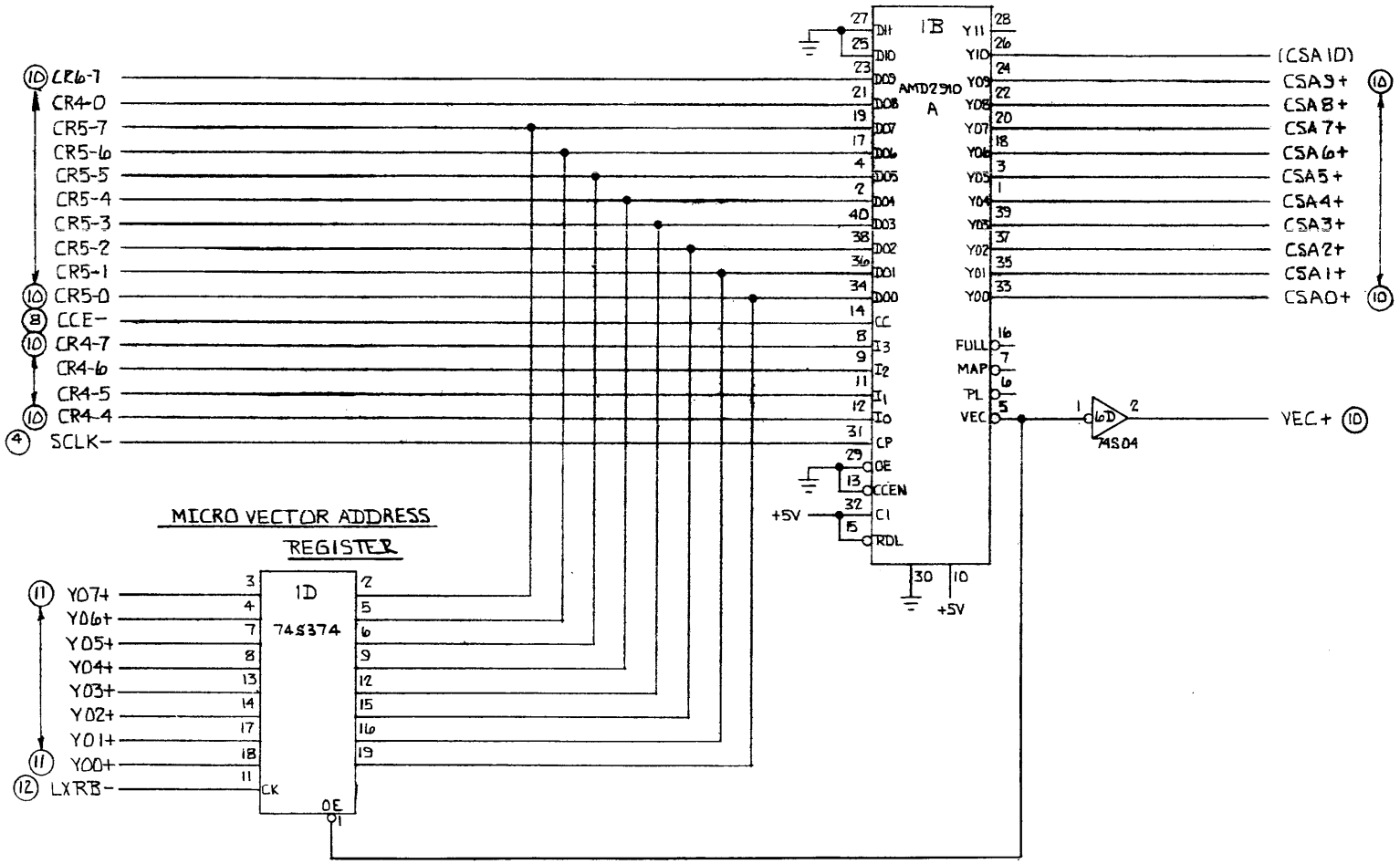
LOGIC DIAGRAM		SHT 8 OF 16
		DRAWING NUMBER 853078 A

MICRO SEQUENCER



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LOGIC DIAGRAM		SHT. 9 OF 16
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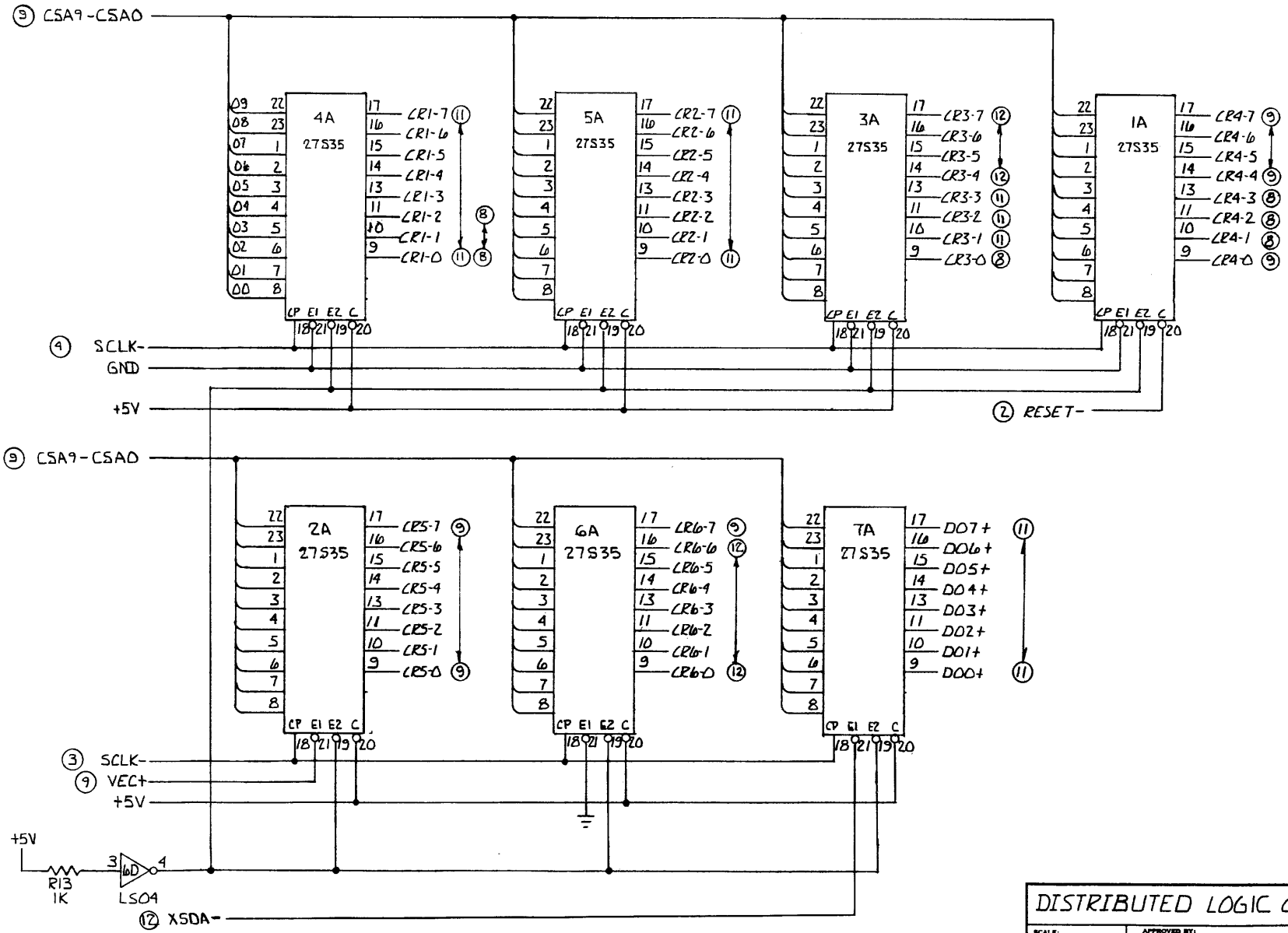

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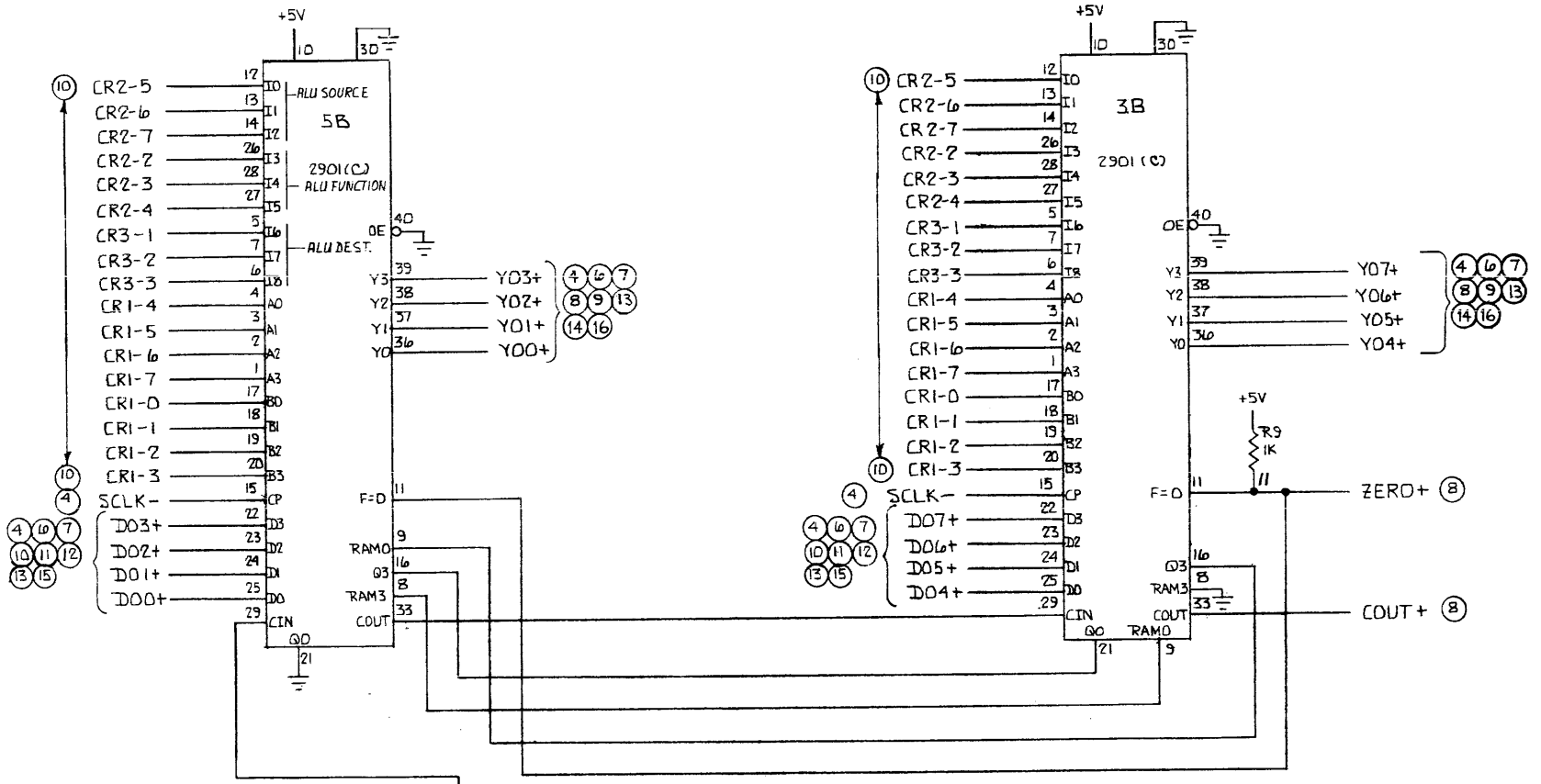
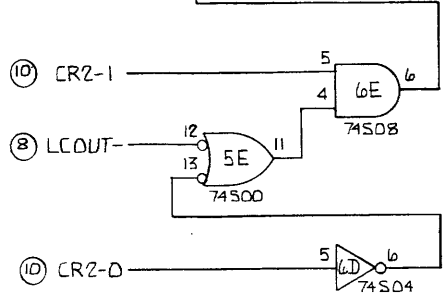
MICRO PROCESSOR ALUS





CARRY IN SELECT

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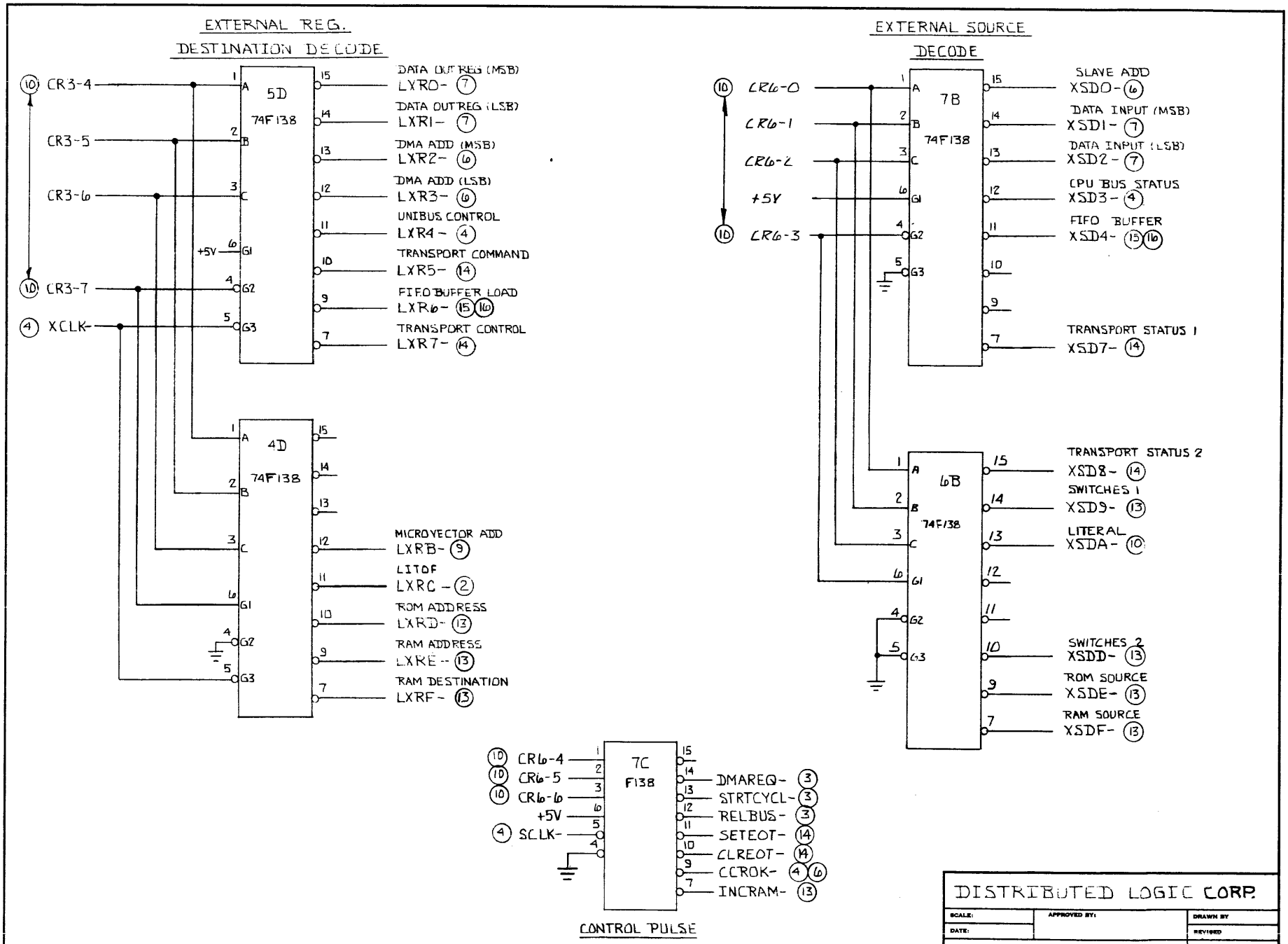
LOGIC DIAGRAM		SHT 11 OF 16
		DRAWING NUMBER 853078 A



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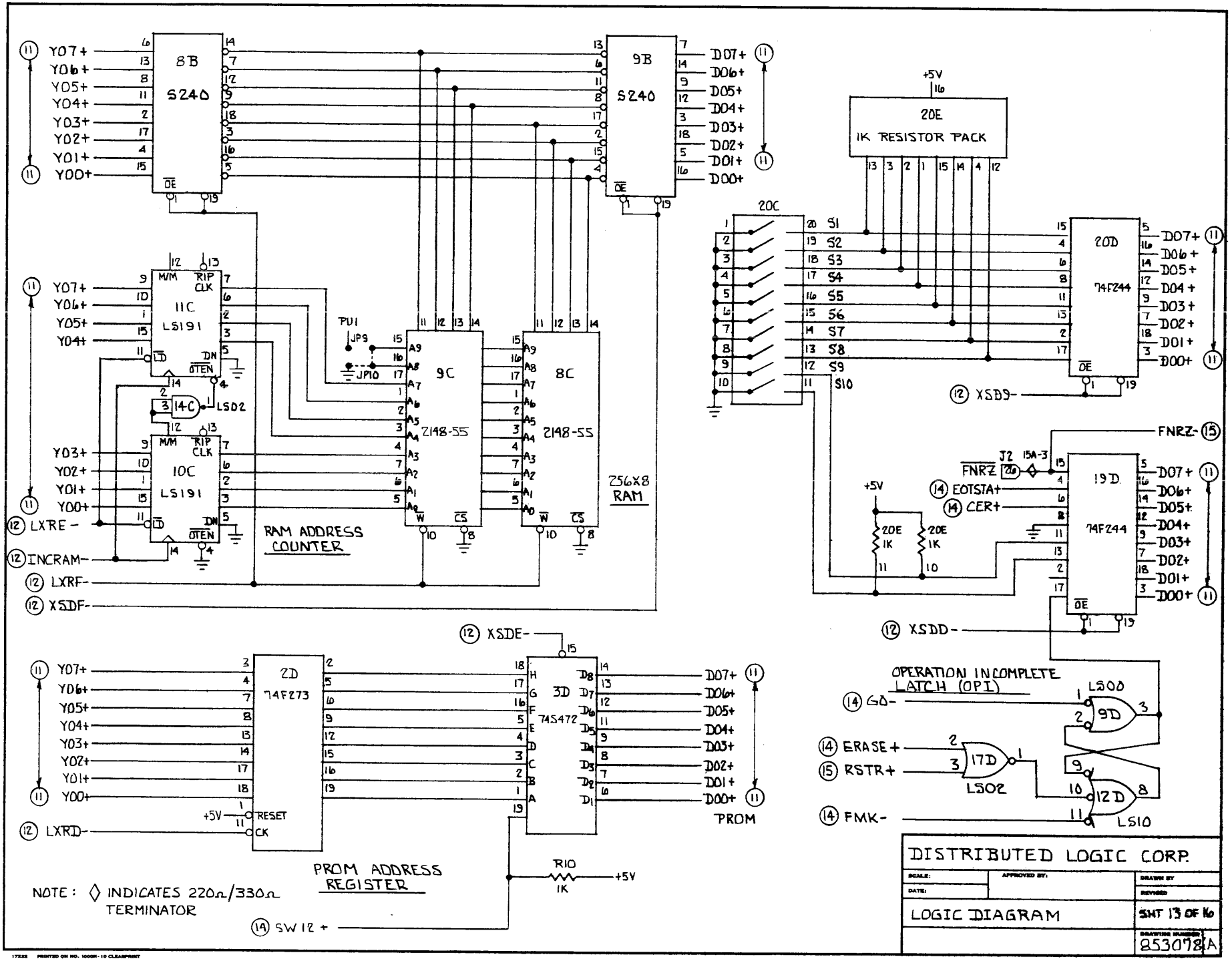
LOGIC DIAGRAM		SHT 12 OF 16
		DRAWING NUMBER 853078 A



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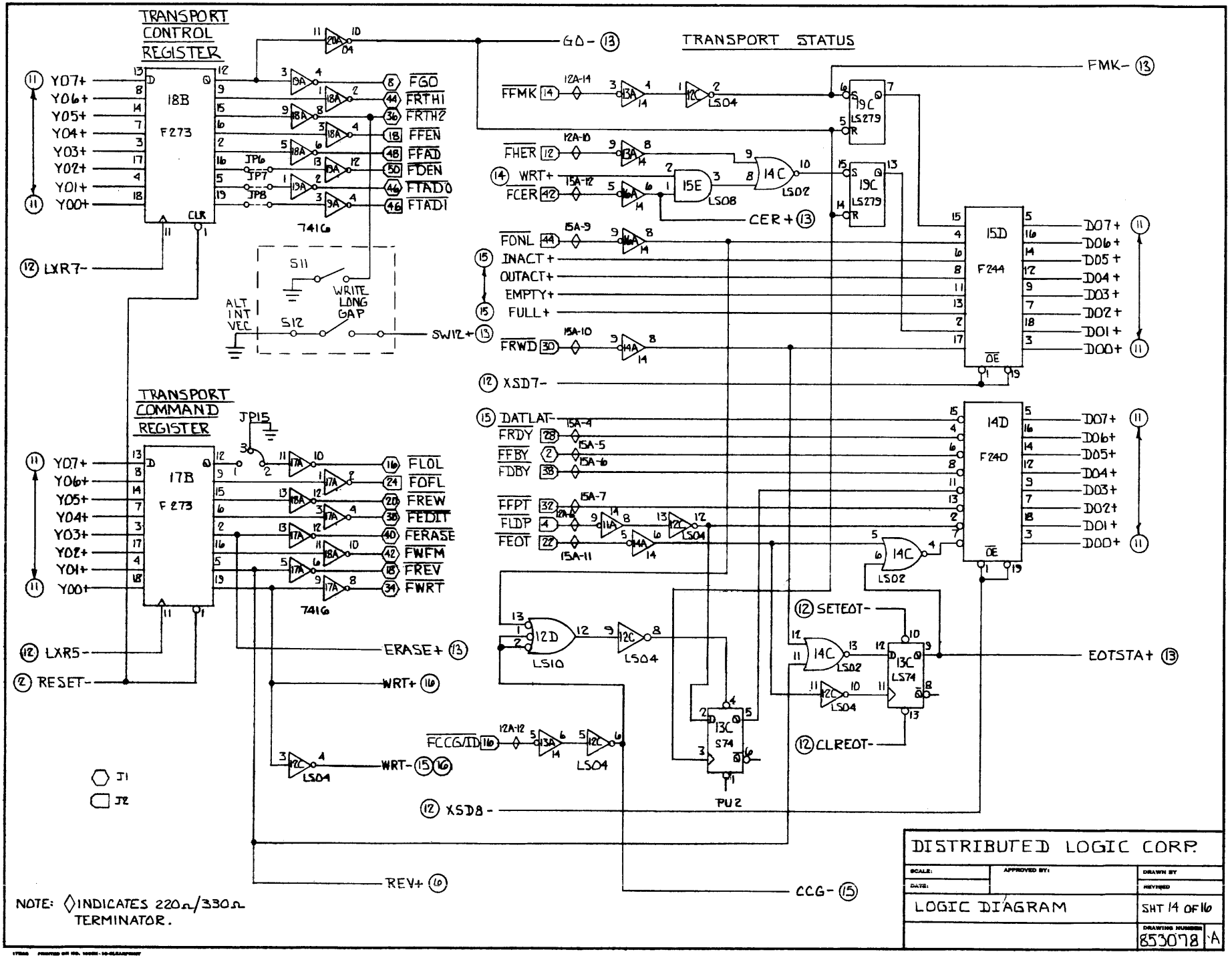
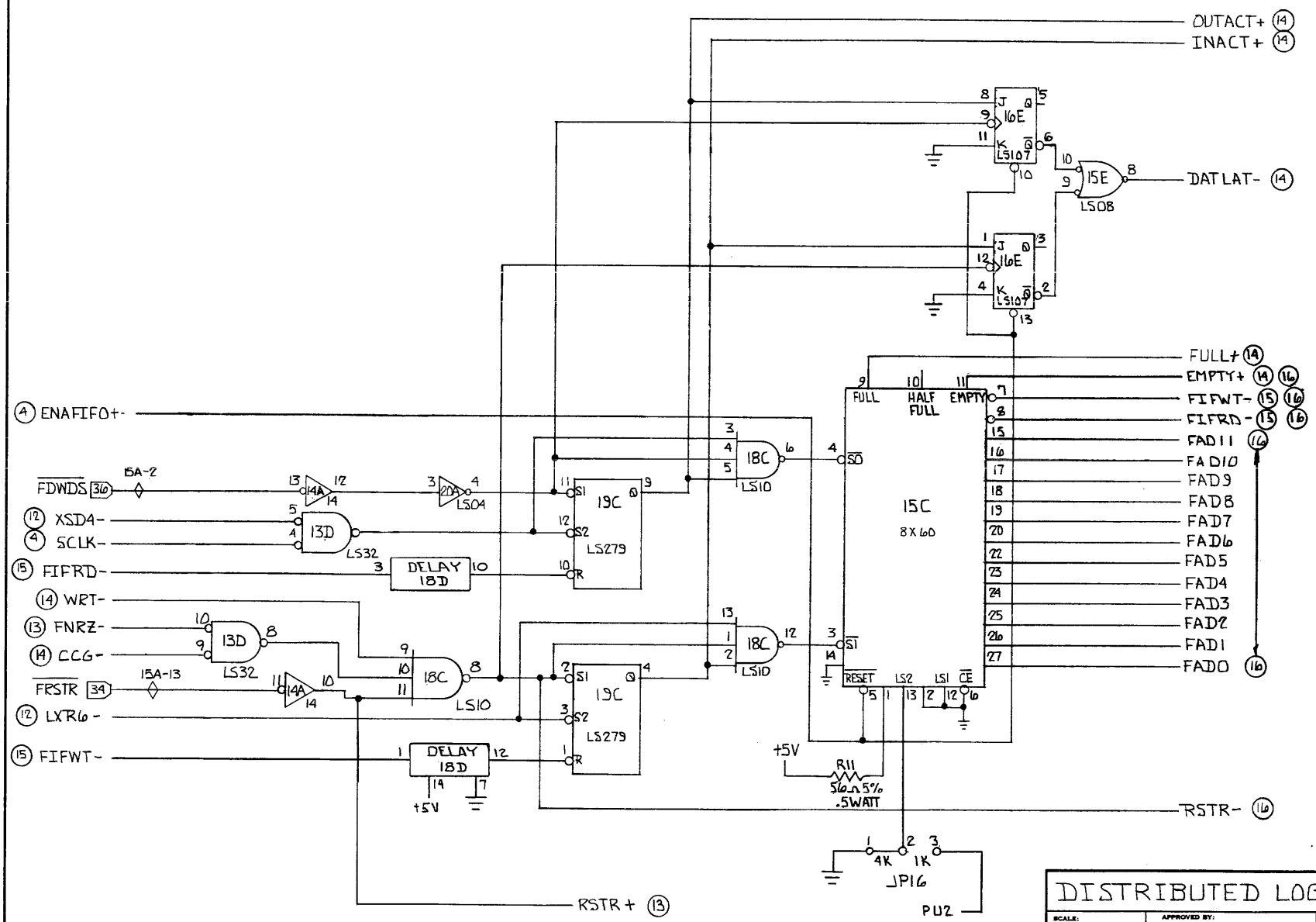
		DRAWING NUMBER 853078A


TRANSPORT CONTROL REGISTER
18B
F273
74LS16
S11
S12
WRITE LONG GAP
ALT INT VEC
TRANSPORT STATUS
15D
F244
14D
F240
TRANSPORT COMMAND REGISTER
17B
F273
12D
LS10
13C
S74
PU2
DISTRIBUTED LOGIC CORP.
LOGIC DIAGRAM
SHT 14 OF 16
853078 A
NOTE: ◇ INDICATES 220Ω/330Ω TERMINATOR.

FIFO CONTROLLER



NOTE: ◇ INDICATES 220Ω/330Ω TERMINATOR.

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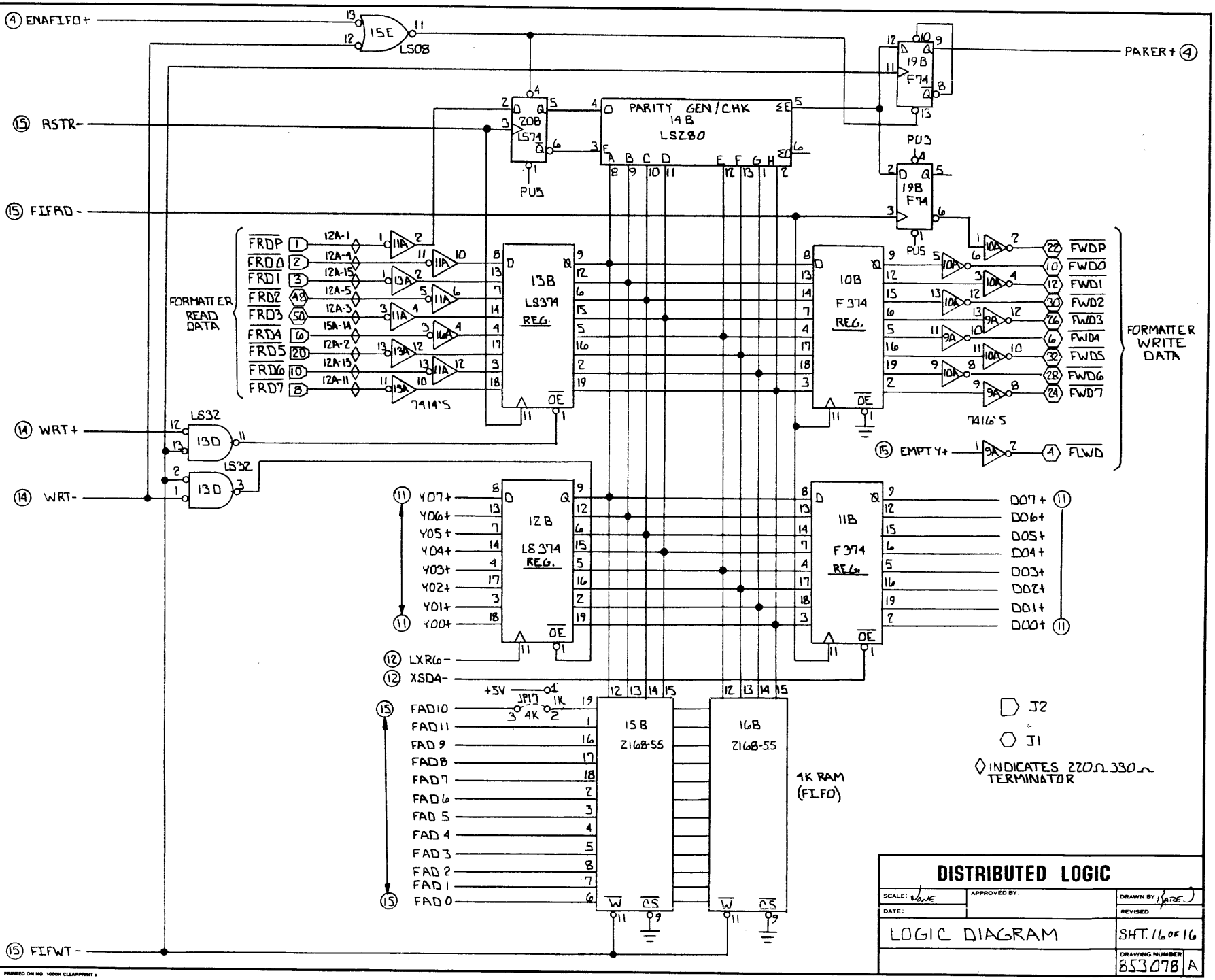

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SCALE: None	APPROVED BY:	DRAWN BY	
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LOGIC DIAGRAM		SHT. 16 OF 16	
		DRAWING NUMBER	853078 A

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LOGIC
CORPORATION

Corporate Headquarters
1555 S. Sinclair Street
P.O. Box 6270
Anaheim, California 92806
Telephone: (714) 937-5700
Telex: 6836051

Eastern Regional Sales Office
64-A White Street
Red Bank, New Jersey 07701
Telephone: (201) 530-0044

European Sales and Service
Chester House
Chertsey Road
Woking, Surrey GU21 5BJ
ENGLAND
Telephone: (04862) 70262/7
Telex: 859321 DILOGI G