SPECIFICATIONS FOR TRANSISTORIZED GENERAL-PURPOSE ANALOG COMPUTER

1. GENERAL DESCRIPTION

1.1 Reliability, accuracy, and operating convenience shall be paramount considerations in the design of the equipment comprising the computer as outlined herein. The computer is to be completely transistorized to insure the best reliability, stability, and extreme compactness. So that it shall be suitable for desktop use, the computer, when fully expanded, shall weigh no more that 330 pounds and shall be no greater in size than 20 inches in width, 25-3/8 inches in height, and 43-3/16 inches in length.

1.2 One each computer in accordance with Section 2.

1.3 (Up to 58) operational amplifiers in accordance with Section 3.

1.4 (Up to 40) integrator channels in accordance with Section 4.

1.5 (Up to 60) precision potentiometers in accordance with Section 5.

1.6 (Up to 23) multipliers in accordance with Section 6.

1.7 (Up to 5) variable diode function generators in accordance with Section 7.

1.8 (Up to 23) unipolar X^2 diode function generators in accordance with Section 8.

1.9 (Up to 23) unipolar Log X diode function generators in accordance with Section 9.

1.10 (Up to 23) Sine-cosine generators in accordance with Section 10.

1.11 (Up to 24) comparators in accordance with Section 11.

1.12 (Up to 5) function switches in accordance with Section 12.

1.13 One or more patching kits in accordance with Section 13.

1.14 (Up to 1) repetitive operation display in accordance with Section 14.

1.15 One each digital voltmeter in accordance with Section 2.3.7.

1.16 One each reference supply in accordance with Section 2.9.

1.17 Extended pushbutton readout system in accordance with Section 2.3.3.

1.18 One or more pre-patch panels in accordance with Section 2.6.

1.19 One each reference supply in accordance with Section 2.9.

1.20 One each power supply in accordance with Section 2.10.

PRINTED IN U.S.A.

PS62008-2 JULY 1964

1.21 One each service shelf in accordance with Section 2.8.

1.22 One each centrally located visual overload alarm system in accordance with Section 16.

1.23 High speed repetitive operation mode in accordance with Section 2.7.

2. COMPUTER

This will contain the following features:

2.1 The computer shall be pre-wired to accommodate up to forty-eight operational amplifiers and sixty precision potentiometers. It shall also be pre-wired to accept the following additional computing components.

2.1.1 (Up to 40) integrator channels.

2.1.2 (Up to 23) quarter-square multipliers in accordance with Section 6.

2.1.3 (Up to 5) variable diode function generators.

2.1.4 (Up to 23) X^2 diode function generators.

2.1.5 (Up to 23) Log X diode function generators.

2.1.6 (Up to 24) comparators.

2.2 Control Panel

2.2.1 Mode Selection--The following computer mode controls shall be available at the computer control panel.

2.2.1.1 Reset--This mode shall restore problem to initial conditions.

2.2.1.2 Hold--This mode shall hold problem solution.

2.2.1.3 Operate--This mode shall place computer in operate condition.

2.2.1.4 Pot-Set--This mode makes reference available to the top of all grounded pots, shorts amplifiers and connects digital voltmeter to selector output.

2.2.1.5 Slave--This mode makes computer mode slave to the signals coming in via the slave connector.

2.2.1.6 Repetitive Operation--Places the entire computer in repetitive operation when integrator networks are patched normally.

2.3 Controls

2.3.1 Readout--The following component outputs shall be selectable by push-button at a centrally located pushbutton matrix for readout on the volt-meter or electronic digital voltmeter at the operator's choice. Push-

2.3 Controls (Cont)

buttons shall be arranged in two columns so that the actuation of one button in each column will accomplish a selection when either the "A" button or the"P" button is also actuated. The control panel and push-button marking system shall correspond with the patch panel marking so that no code need be remembered by the opeator.

2.3.1.1 Amplifier Outputs--(60 when A button is depressed).

2.3.1.2 Potentiometer Coefficients (60 when P button is depressed).

2.3.1.3 Trunks (Incoming 15 when A button is depressed).

2.3.2 Readout in accordance with the above shall be included for all such components supplied. Provision shall be included for readout of all such components that may be added at a future date in order to make up a fully expanded console.

2.3.3 Readout Panel--A readout panel shall be provided on every patch panel. It shall provide access to:

(a) The output of the signal selector (SEL).
(b) Input to the digital voltmeter.
(c) Input to the voltmeter.
(d) Output to a vertical and horizontal oscilloscope sweep. This panel shall make possible connections to connectors, at rear of computing consoles for X-Y plotters, strip chart recorders, and ten cross computer trunks.

2.3.4 Control panel of console shall contain a voltmeter which shall be a precision multi-range meter for the monitoring of amplifier outputs, input trunks, and power supply voltages, which shall also be capable of being used for the balancing of operational amplifiers. Five meter ranges shall be selectable by a rotary switch. A voltmeter selector switch will also be available which shall select all power supply voltages for readout on the voltmeter.

2.3.5 A centrally located visual overload indicator shall be available on the control panel which will immediately identify any amplifier which is in an overload condition.

2.3.6 A pushbutton power switch illuminated by light when in the "On" position shall be available on the control panel which will allow control of primary power to the computer.

2.3.7 A completely transistorized digital voltmeter shall be provided on the control panel for the precise, rapid, digital readout of computing voltages. This voltmeter shall offer a five-digit display and polarity from 1.0 millivolts to $\pm$11.999 volts dc with fixed decimal point. This voltmeter shall give readings accurate to $\pm$0.01% and $\pm$1 digit over the entire reading range. It shall have a high brilliance optical projection system to display reading, sign and decimal point.

2.4 Console Construction--All power supply voltages to be supplied to amplifiers and other computing components via bus bars, e.g., it shall be possible to remove any power supply voltages from any amplifier by merely unplugging the proper taper pin from a bus bar carrying that voltage behind the amplifier chassis.

2.5 All operational components and power supplies are to be of a plug-in type.

2.6 Pre-Patch Panel

2.6.1 Construction

The computing console shall accept a removable pre-patch panel. All computing components shall terminate inputs and outputs on this pre-patch panel. The design of the pre-patch board and the grouping of components shall be such as to allow the maximum use of bottle plugs to reduce pre-patch panel clutter to a minimum. Construction shall be such as to eliminate possibility of "open" connections due to loose or partial insertion of patch cords. The pre-patch panel shall be constructed so that that it can be modified to conform to changes in the number and type of computing components in the computing console. This shall be accomplished by adding or replacing component blocks on the pre-patch panel as required by the new computer component configuration without any changes or additions to systems wiring. The pre-patch panel shall be at least twenty-nine inches in width and twenty-two inches in height in order to allow the programmer proper access to, and vision of, the pre-patch panel connections.

2.6.2 Color-coding of pre-patch panel--To be color-coded as follows...

2.6.2.1 Green--input

2.6.2.2 Red--output

2.6.2.3 Yellow--potentiometer

2.6.2.4 Black--ground

2.6.2.5 White--integrator networks

2.6.2.6 Tan--switching and non-linear components

2.7 High-Speed Repetitive Operation System

2.7.1 Shall permit computer to be operated in either real time or high speed repetitive operation.

2.7.2 Shall be capable of producing compute times from 20 to 500 milliseconds per solution. Reset time shall be ten milliseconds. The HSRO shall be capable of cycling solutions at least 33 times a second.

2.7.3 Shall have switch control of solution times at fixed values of 20, 50, 100 and 200 milliseconds per solution. Vernier control to obtain solution times between fixed values shall also be available.

2.7.4 Timing unit shall be completely solid state.

2.7.5 Shall have "slave" system to allow control of two or more computers in either real time or repetitive operation mode.

2.7.6 Shall have automatic time scale change of 500 to 1 from real time to repetitive operation which may be accomplished simultaneously on all integrators from mode control buttons on control panel.

2.7.7 Shall utilize high speed electro-mechanical relays to cycle computer between reset and operate modes.

2.8 Service Shelf

2.8.1 Shall permit convenient maintenance of computing components under normal operating conditions.

2.9 Reference Supply System

2.9.1 Reference supplies of plus or minus 10 volts and 250 milliamperes capacity shall be furnished.

2.9.2 Terminations for plus and minus reference shall be provided on the prepatch panel.

2.9.3 The noise on either positive or negative reference voltages shall not exceed 300 microvolts RMS.

2.9.4 The balance between positive and negative reference voltages shall be adjustable to $\pm 0.01\%$ or better. The long term stability of this balance shall be * $\pm 0.002\%/^{o}F$ or better.

2.9.5 The absolute value of the reference voltage shall be adjustable to $\pm .05\%$ or better. The long term stability of this absolute value shall be $\pm 0.003\%/^{o}F$ or better.

2.10 Power Supply

2.10.1 A transistorized power supply shall be furnished which is capable of operating from line voltages of 100 to 125 volts, 50 to 60 cycles per second within the accuracy specifications of the computing components.

2.10.2 This supply shall have sufficient capacity to supply necessary power to the computer when it is fully expanded.

---

*Note items specified in % per degree F.

3. AMPLIFIERS

3.1 All operational amplifiers shall be uncommitted. That is, shall be capable of being used as either integrators, summers, or high gain amplifiers in conjunction with multipliers and function generators, depending on the patching utilized.

3.2 Each amplifier shall have an overload indicator tied to an individual, centrally located, visual overload indicator located on the computer control panel which will indicate excessive departure of the summing point voltage from zero.

3.3 The amplifiers shall be packaged in identical interchangeable amplifier modules, each consisting of two transistorized dc amplifiers terminated on the patch panel as high-gain amplifiers. Companion networks, consisting of input and feedback resistors matched to 0.01% accuracy shall be terminated in the module so that the amplifier may be converted to inverter or summer operation by bottle plugs.

3.4 The amplifier shall be connected to its pre-patch panel connections at all times except in the pot-set mode at which time a short shall be placed on the amplifier internally.

3.5 Output current shall be 20 milliamps at plus-minus ten volts.

3.6 Bandwidth of a standard 10K-10K inverter shall be 350 kc typically.

3.7 Phase shift of a standard 10K-10K inverter at twenty volts peak-to-peak and 1000 cps shall be no more than 0.15^{o}.

3.8 The dynamic amplitude error of a standard 10K-10K inverter at ten volts peak-to-peak at 1000 cps shall be no greater than 0.1% maximum.

3.9 The amplifier offset temperature coefficient for a unity gain inverter with 10K resistors shall be plus or minus 0.5 microvolts per degree fahrenheit.

3.10 Peak noise and ripple standard 10K-10K inverter 100μ volts peak typical.

3.11 All amplifiers shall be individually chopper stabilized.

3.12 Expansion Capability (Above 48 Amplifiers)

3.12.1 Computer may be expanded to a total of 58 amplifiers packaged as quads which shall be uncommitted. That is, shall be capable of being used as inverters, or high gain amplifiers, depending on the patching utilized.

3.12.2 Each amplifier shall have an overload indicator tied to an individual, centrally located, visual overload indicator located on the computer control panel which will indicate excessive departure of the summing point voltage from zero.

3.12.3 The amplifiers shall be packaged in identical interchangeable amplifier modules, each consistiing of four transistorized dc amplifiers terminated on the patch panel as high-gain amplifiers. Companion networks, consisting of input and feedback resistors matched to 0.01% accuracy shall be terminated in the module so that the amplifier may be converted to inverter operation by bottle plugs.

3.12.4 The amplifier shall be connected to its pre-patch panel connections at all times except in the pot-set mode at which time a short shall be placed on the amplifier internally.

3.12.5 Output current shall be 20 milliamps at plus-minus ten volts.

3.12.6 Bandwidth of a standard 10K-10K inverter shall be 350 kc typically.

3.12.7 Phase shift of a standard 10K-10K inverter at twenty volts peak-to-peak and 1000 cps shall be no more than 0.15^{o}.

3.12.8 The dynamic amplitude error of a standard 10K-10K inverter at ten volts peak-to-peak at 1000 cps shall be no greater than 0.1% maximum.

3.12.9 The amplifier offset temperature coefficient for a unity gain inverter with 10K resistors shall be plus or minus 0.5 microvolts per degree fahrenheit.

3.12.10 Peak noise and ripple standard 10K-10K inverter 100μ volts peak typical.

3.12.11 All amplifiers shall be individually chopper stabilized.

4. INTEGRATOR NETWORK

4.1 The integrator network shall, when used with high gain amplifiers, pro-vide two integrator channels. The network pre-patch module will be so designed as to permit the use of a bottle plug to make all necessary connections with the high gain amplifier to form an integrator channel.

4.2 Shall contain all relays necessary for switching the integrator to reset, hold, operate modes of operation.

4.3 Shall have available "IC" termination for introducing initial conditions other than zero directly into the integrator for both "real time" and "repetitive operation" modes. No additional amplifiers shall be required when in repetitive operation mode.

4.4 Individual integrator 10 to 1 time change shall be accomplished by bottle plug patching in either "real time" or high speed repetitive operation.

4.5 Precision $\pm$0.05% polystyrene capacitors shall be used for real time, adjustable for repetitive operation.

4.6 Shall be capable of time scale change of 500 to 1 between "real time" and "repetitive operation" modes.

4.7 Shall have patching terminations available to allow control for each dual unit mode of operation.

5. POTENTIOMETERS

5.1 Shall be 10 turn, 5000 OHM wirewound potentiometers individually current limited and equipped with calibrated adjustment knobs.

5.2 The potentiometers shall be mounted in groups of five on the front of the computer console and shall be immediately accessible to the operator. (The mounting of potentiometers on sliding trays, which do not allow immediate access to all potentiometers, shall not be acceptable.)

5.3 The high end and arm of four potentiometers in each group shall be terminated on the patch panel with low ends grounded. The fifth potentiometer shall be terminated on the patch panel with the low end ungrounded.

5.4 All inputs shall be uncommitted.

5.5 Resolution shall be .025% typical.

5.6 When the computer is in the "Pot-Set" mode, relays within the module shall place reference on the high end of the four grounded pots and the arms shall be connected to the readout selector system. In any other mode just the arms of all five potentiometers shall be available for readout selection.

6A. QUARTER-SQUARE MULTIPLIERS (MEDIUM ACCURACY)

6A.1 Shall be a completely solid state unit which is capable of producing a product of two input variables of either polarity. It shall also be capable of performing the operations of division, squaring and square root. (Interchangeable with 6B Multiplier.)

6A.2 The maximum static multiplying error shall not exceed plus or minus 0.4% full scale (20 volts full scale).

6A.3 Phase shift shall be less than 0.28^{o} when multiplying plus or minus ten (10) volts dc by twenty (20) volts peak-to-peak at 1000 cps.

6A.4 The maximum dynamic amplitude error when multiplying plus or minus ten volts dc by 20 volts peak-to-peak at 1000 cps shall be $\pm$0.25% of full scale.

6B. QUARTER-SQUARE MULTIPLIERS (HIGH ACCURACY)

6B.1 Shall be a completely solid state unit which is capable of producing a product of two input variables of either polarity. It shall also be capable of performing the operations of division, squaring and square root.

6B.2 The maximum static multiplying error shall not exceed plus or minus 0.09% full scale (20 volts full scale).

6B.3 The maximum static multiplying error shall not exceed plus or minus 0.06% for sum of inputs equal to or less than 9 volts ($|x|+|y| \leq 9.0$ volts.

6B.4 The maximum zero error with either input zero shall be less than plus or minus $\pm 0.05\%$ of full scale. For both inputs zero - $\pm 0.005\%$ maximum.

6B.5 Phase shift shall be less than 0.2 degrees at 1000 cps maximum.

6B.6 The total instantaneous dynamic error shall be less than 0.35% of output - maximum at 1000 cps.

7A. VARIABLE DIODE FUNCTION GENERATORS (FIXED BREAKPOINT)

7A.1 Each diode function generator shall be capable of generating a single 19-segment or two independent 10-segment functions when used in conjunction with amplifiers.

7A.2 Shall incorporate single turn carbon potentiometers for slope adjustments.

7A.3 Maximum slopes for each 10 segment section shall be as follows:

Segment No. 1 ..... at least 4 volts/volt (slope at the origin)

Segment Nos. 2 through 10 .... at least 1 volt/volt

7A.4 Frequency response shall be compatible with associated amplifier.

7A.5 Noise shall be less than 1 millivolt RMS.

7B. VARIABLE DIODE FUNCTION GENERATORS (VARIABLE BREAKPOINT)

7B.1 Each diode function generator shall be capable of generating a single 19-segment or two independent 10-segment functions when used in conjunction with amplifiers.

7B.2 Shall incorporate single turn carbon potentiometers for slope adjustments.

7B.3 Maximum slopes for each 10 segment section shall be as follows:*

Segment No. 1 ..... at least 2 volts/volt (slope at the origin)

Segment Nos. 2 through 10 ... at least 1 volt/volt

7B.4 Frequency response shall be 35 kc minimum.

7B.5 Phase shift shall be 0.4° maximum at 1000 cps.

---

*With addition of potentiometers in second amplifier feedback, slopes in the order of 20v/v may be obtained.

8. X^2 DIODE FUNCTION GENERATOR

8.1 Shall be a dual fixed diode function generator composed of completely solid state components.

8.2 One dual unit shall be capable of the following operations:

A. When operated in combination with an operational amplifier it will yield an X^2 output for X of one polarity.

B. When operated in combination with two operational amplifiers, it will deliver outputs of $(X_1)^2$ and $(X_2)^2$ when both X_1 and X_2 are unipolar and of opposite sign.

C. When operating in combination with two operational amplifiers it will deliver an output of X^2 with the input X varying both plus and minus in sign.

D. A square root output may be obtained by using the X^2 DFG in the feedback of an operational amplifier.

8.3 Shall accept inputs from plus to minus ten volts and provide outputs from plus to minus 10 volts.

8.4 Frequency response shall be compatible with associated amplifier.

8.5 Total error at 5.0 cps shall be plus or minus .2% full scale typically and plus or minus .4% full scale maximum.

9. LOG DIODE FUNCTION GENERATOR

9.1 Shall be a dual diode function generator composed of completely solid state components.

9.2 Each dual unit shall be capable of the following operation when used in conjunction with operational amplifiers.

A. Output of $Log_{10}X$ for an X input of one polarity.

B. Outputs of $Log_{10}X_1$ and $Log_{10}X_2$ when inputs X_1 and X_2 are unipolar and opposite sign.

C. An exponential output when the Log DFG is used in feedback of high gain amplifier.

9.3 Shall accept inputs from plus to minus ten volts and provide outputs from plus to minus ten volts.

9.4 Frequency response shall be compatible with associated amplifier.

9.5 Log X, actual input deviation from theoretical input for a given output shall be plus or minus 0.5% F.S., typical.

10. SINE-COSINE DIODE FUNCTION GENERATOR

10.1 Shall be a dual diode function generator composed of completely solid state components.

10.2 Each section shall be capable of the following operation when used in conjunction with operational amplifiers:

A. Sine θ $\pm 180^{o}$

B. $\pm$Cosine θ $\pm 180^{o}$

10.3 Shall accept inputs from plus to minus ten volts and provide outputs from plus to minus ten volts.

10.4 State error at set up temperature shall be plus or minus 0.15% of full scale maximum.

10.5 State error at any temperature between $12^{o}C$ and $50^{o}C$ shall be plus or minus 0.25% of full scale maximum.

10.6 Phase shift shall not exceed 5 degrees at 1000 cps.

10.7 Typical frequency response is 12 kc/s.

10.8 Zero error shall be less than 1 millivolt.

10.9 Noise shall be less than 10 millivolts peak-to-peak.

11A. COMPARATOR (RELAY)

11A.1 The comparator module shall contain two separate comparator channels each with a double-pole, double-throw relay. Each channel shall compare a variable input voltage to an arbitrary fixed voltage and cause a switching operation to be performed.

11A.2 Each comparator channel shall contain at least one double-pole, double-throw relay.

11A.3 An amplifier shall be furnished as a part of the comparator.

11A.4 Each comparator shall have an input range of plus ten to minus ten volts.

11A.5 Switching time shall be no greater than 10 milliseconds maximum.

11A.6 Sensitivity (minimum change in input voltage required to cause switching action in either direction) shall be no greater than 3 millivolt.

11A.7 The relay contacts shall be capable of handling at least 2 amperes at 24 volts for non-inductive loads.

11B. COMPARATOR (ELECTRONIC)

11B.1 The comparator module shall contain one comparator channel which shall compare a variable input voltage to an arbitrary fixed or variable voltage and cause a switching operation to be performed.

11B.2 The comparator shall have an input range of plus ten to minus ten volts.

11B.3 Switching sensitivity shall be plus or minus one millivolt, maximum.

11B.4 Propagation time shall not exceed 5 microseconds typical.

11B.5 Comparator may be latched upon command.

11B.6 Comparator output is binary one -5 vdc, binary zero -.2 vdc and the complement which may be used to control electronic switches or other electronic devices.

11B.7 Electronic switch input impedance is 10,000 ohms.

11B.8 Electronic switch propagation time is 1 microsecond typical (neglecting the rise time of the output amplifier).

11B.9 Dc offset of electronic switch is ±500 microvolts maximum.

12. FUNCTION SWITCHES

12.1 Shall be single-pole, double-throw center off switches for performing manual switching operations.

12.2 Switch contacts shall be capable of handling at least 2 amperes at 24 volts for non-inductive loads.

13. PATCHING KITS

13.1 Patching kit shall include the following:

20 each patch cords, 6 inches long; Color: Black

30 each patch cords, 12 inches long; Color: Brown

20 each patch cords, 18 inches long: Color: Orange

10 each patch cords, 30 inches long; Color: Blue

30 each bottle plugs, 2 prong horizontal

32 each bottle plugs, 4 prong

8 each bottle plugs, 6 prong "T" (For connecting integrator networks)

2 each Multiply blocks (For off-the-panel tie points)

14. REPETITIVE OPERATION DISPLAY

14.1 Display is all solid state (except cathode ray tube) with four channels displayed sequentially while computer is in repetitive operation mode.

14.2 Y axis display accuracy is plus or minus 1% of full scale (plus or minus ten volts).

14.3 Linearity is plus or minus 0.25% (within principal square).

14.4 Writing speed is up to 20,000 inches per second.

14.5 Display area is 4.16 inches by 6.24 inches.