# SC03/BX

# RM03/RM05/RM80/RP04/RP05/RP06 COMPATIBLE

# DISK CONTROLLER

# TECHNICAL MANUAL

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Section 1
INTRODUCTION

## 1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the SC03/BX Disk Controller manufactured by Emulex Corporation. In addition, this manual provides diagnostic and application information.

## 1.2 OVERVIEW

### 1.2.1 General Description

The SC03/BX Disk Controller is a one board, embedded controller for LSI-11 computers manufactured by Digital Equipment Corporation (DEC). This controller can be used to interface any large disk having a Storage Module Drive (SMD) interface. The SC03/BX controller emulates the RH11 and RH70 disk controllers manufactured by DEC for use with RM02, RM03, RM05, RM80, RP04, RP05 and RP06 disk drives.

### 1.2.2 Register Addresses in this Manual

The register addresses given in this manual are standard Q-Bus addresses for an RP/RM disk subsystem. All addresses are given for an 18-bit Q-Bus. For 22-bit addressing, add 17000000 to obtain the desired register address.

## 1.3 FEATURES

Features that enhance performance and increase versatility are described in the following paragraphs. Table 1-1 lists specifications for the SC03/BX Disk Controller.

### 1.3.1 Microprocessor Design

The SC03/BX design incorporates a unique 16-bit bipolar microprocessor to perform all controller functions. The microprocessor approach provides for a reduced component count, high reliability, easy maintainability, and most importantly, the ability to adapt a single set of hardware to a wide range of emulation capabilities through the use of microprogramming. The Emulex controllers achieve functional capability beyond that of the DEC controllers which they emulate, by providing enhancement features such as built-in self-test during power-up, built-in disk formatting and the ability to work with disk drives of various capacities.

### 1.3.2 Packaging

The SC03/BX is constructed on a single, quad-size, multi-layer printed circuit board assembly (PCBA) which plugs directly into the LSI-11 chassis or an expansion chassis. No cabling is required between the computer and the disk controller. The controller obtains its power from the chassis in which it is mounted.

### 1.3.3 Self-Test

The controller incorporates an internal self-test routine which is executed upon power-up. This test exercises all parts of the microprocessor, buffer and disk data logic. Although this test does not completely test all controller circuitry, successful execution indicates a very high probability that the controller is operational. If the controller fails the self-test, it leaves the Fault LED ON and the controller cannot be addressed from the central processing unit (CPU).

### 1.3.4 Buffering

The controller contains a 4K x 16 high-speed random access memory (RAM) buffer. It is used to store the device registers of the controller plus fourteen sectors of data buffering. Because of the buffering and the strategies used to employ it, data late situations on the Q-Bus are not possible.

### 1.3.5 Error Correction

The controller incorporates a 32-bit error correcting code (ECC) capable of correcting single error bursts of up to 11 bits long, and detecting multiple error bits in bursts of any length. The controller determines the pattern and location of the error so that the software may correct the data after it is transferred to memory. A 16-bit cyclic redundancy check (CRC) is employed with the header of every sector.

### 1.3.6 Dual Port Mode

The controller can operate with disk drives which have dual port capability; therefore, a second controller can have access to the drive on a priority basis. This mode should be selected only when the disk drive has dual ports and is configured for Dual Port operation.

### 1.3.7 Dual Access Mode

In order to provide compatibility with dual access drivers when configured for dual access, the Dual Access mode is provided. When in this mode, the controller sets DPM in the Drive Type Register and PGM in the Drive Status Register to imitate the DEC neutral state.

### 1.3.8 Option and Configuration Switches

Sockets provide for insertion of optional 512 word bootstrap PROMS, 22-bit addressing and Q-Bus termination resistor packs. Provisions are also made to enable an optional software-controlled line time clock (LTC) which is BDV11 compatible.

DIP switches are used to configure the controller for various disk sizes, Q-Bus addresses and options. It is possible to select one of several possible combinations of disk characteristics for the two drives which can be handled by the controller, including mixtures of disk sizes and drive type codes.

## 1.4 FUNCTIONAL COMPATIBILITY

### 1.4.1 Media Compatibility

In all cases, the headers written on the drives are standard DEC headers. Packs may be formatted by utilizing the hardware formatting capability of the extended command set. Disk packs formatted with an SC03/BX controller are media compatible with other Emulex controllers and with the equivalent DEC packs when appropriate disk drives are used.

### 1.4.2 Disk Mapping

Depending upon the type and size of the disk drive, one or two logical units may be mapped on it. Various mapping organizations are used; some of which do not leave direct 1:1 correlation between the logical and physical addresses.

### 1.4.3 Diagnostics

The controller executes the following standard DEC RM02/RM03 and DEC RP05/RP06 diagnostics:

ZRMA - Formatter
ZRMB - Performance Exerciser
ZRMC - Functional Controller, Part I*
ZRMD - Functional Controller, Part II*
ZRME - Functional Controller, Part III*
ZRMF - Extended Drive Test
ZRMI - Drive Compatibility Test

ZRJA - Mechanical and Read Write Test
ZRJB - Formatter
ZRJD - Multi-Drive Exerciser
ZRJG - Diskless Controller Test, Part 1 *
ZRJH - Diskless Controller Test, Part 2 *
ZRJI - Functional Controller Test, Part 1 *
ZRJJ - Functional Controller Test, Part 2 *

The diagnostics marked with an asterisk require certain patches to correct coding problems or to bypass unsupported maintenance

functions. All diagnostics require patches to run with drive capacities other than that of a standard RM02/RM03 or RP06. In addition, the ZRMB Performance Exerciser will not run on any drive with more than 16 bad sectors.

Emulex has available self-sizing RM diagnostics which have all the required patches, will work on any size drive and can handle 126 bad sectors.

Appendix B contains modifications to DEC's RM02 diagnostics. Appendix C contains modifications to DEC's RP06 diagnostics.

### 1.4.4 Operating Systems

The SC03/BX controller is compatible with DEC operating systems without modification when emulating any standard DEC disk subsystem. Patches to the operating system are required when operating with other than standard size disks. These patches numerically redefine the logical drive capacity to the operating system and generally do not involve modification to program instructions.

The RM02/03/05/80 and RP06 disk drives are not supported by all DEC operating systems, in particular, RT11.

Table 1-1
General Specifications

| | |
|---|---|
| **FUNCTIONAL** | |
| Emulation | DEC RM02/RM03/RM05/RM80, RP04/RP05/RP06 |
| Media Compatibility | DEC RM02, RM03, RM05 and RP06 when using appropriate disk drives. |
| Drive Interface | SMD |
| Drive Ports | 2 |
| Error Control | 32-bit ECC for data and 16-bit CRC for headers. Correction of single data error burst of up to 11 bits. |
| Sector Size | 256 words (512 bytes) |
| Sectors/Track | Selectable for each drive. |
| Tracks/Cylinder | Selectable for each drive. |
| Cylinders/Drive | Selectable for each drive. |
| Drive Type Code | Selectable for each drive. |
| Computer Interface | Q-Bus |
| Q-Bus Address | |
| Standard | 776700-776752 |
| Alternate | 776300-776352 |
| Vector Address | |
| Standard | 254 |
| Alternates | 150, 270, 274, 354, 224, 370, 374 |
| Priority Level | BR5 |
| Data Buffering | 14 full sectors |
| Data Transfer | High speed NPR operation. |
| Maximum Disk Data Rate | 16 MHz (2 MBytes/second) |

Table 1-1 (cont'd)

| | |
|---|---|
| Self-Test | Extensive internal self-test on powering up. |
| Indicators | Fault/Activity LED |
| DESIGN | High-speed bipolar microprocessor using 2901 bit-slice components. |
| PHYSICAL | |
| Packaging | One DEC quad-size PCBA. |
| Mounting | Any slot in CPU or expansion box. |
| Connectors | One 60-pin A Cable flat connector and two 26-pin B Cable connectors. (Flat cable type.) |
| Electrical | |
| Q-Bus Interface | DEC approved line drivers and receivers. |
| Drive Interfaces | Differential line drivers and receivers. A Cable cumulative length to 35 feet. B Cable length to 25 feet. |
| Power | +5 V, 8 A maximum |

Section 2
GENERAL DESCRIPTION

## 2.1 CONTROLLER ORGANIZATION

A block diagram showing the major functional elements of the SC03/BX controller is shown in Figure 2-1. The controller is organized around a 16-bit high-speed bipolar microprocessor. The arithmetic and logic unit (ALU) and register file portion of the microprocessor are implemented with four 2901 bit-slice components. The microinstruction is 48 bits in length and the control memory of 4K words is implemented with six 4K x 8 bit PROMs.

The controller incorporates a 4K x 16 bit high-speed RAM buffer which is used to store the controller's device registers plus fourteen sectors (3584 words) of data buffering.

The A Cable Register (ACR) latches all A Cable signals going to or from the disk drives. The inputs from the selected drive are testable by the microprocessor.

The Shift Register converts parallel write data from the data bus to serial data for the disk drives. The register also converts serial read data from the drives back into parallel data. Serial read and write data is provided to the ECC logic via the Shift Register.

Serial data from the drive is converted into eight-bit parallel data and transferred to the buffer via the microprocessor. Likewise, the data accessed from the buffer by the microprocessor is serialized and sent to the drive under the control of the servo clock received from the drive. A 32-bit ECC Shift Register is used to generate and check the ECC for the data field. The same register is also used in a 16-bit CRC mode for the headers. The actual ECC polynomial operation is done independently of the microprocessor, but the determination of the error position and error pattern is done under the control of the microprocessor.

The Q-Bus interface consists of 42 bidirectional lines (which include lines A18 to A21) and two unidirectional signal lines. The Q-Bus interface is used for programmed input/output (I/O), CPU interrupts, and Data Transfers. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed controller register. The microprocessor also controls all DMA operations and transfers data between the Q-Bus data lines and the buffer.

## 2.2 PHYSICAL DESCRIPTION

The SC03/BX controller consists of a single quad-size board which plugs directly into an LSI-11 chassis or an expansion chassis. The controller PCBA is shown in Figure 2-2.

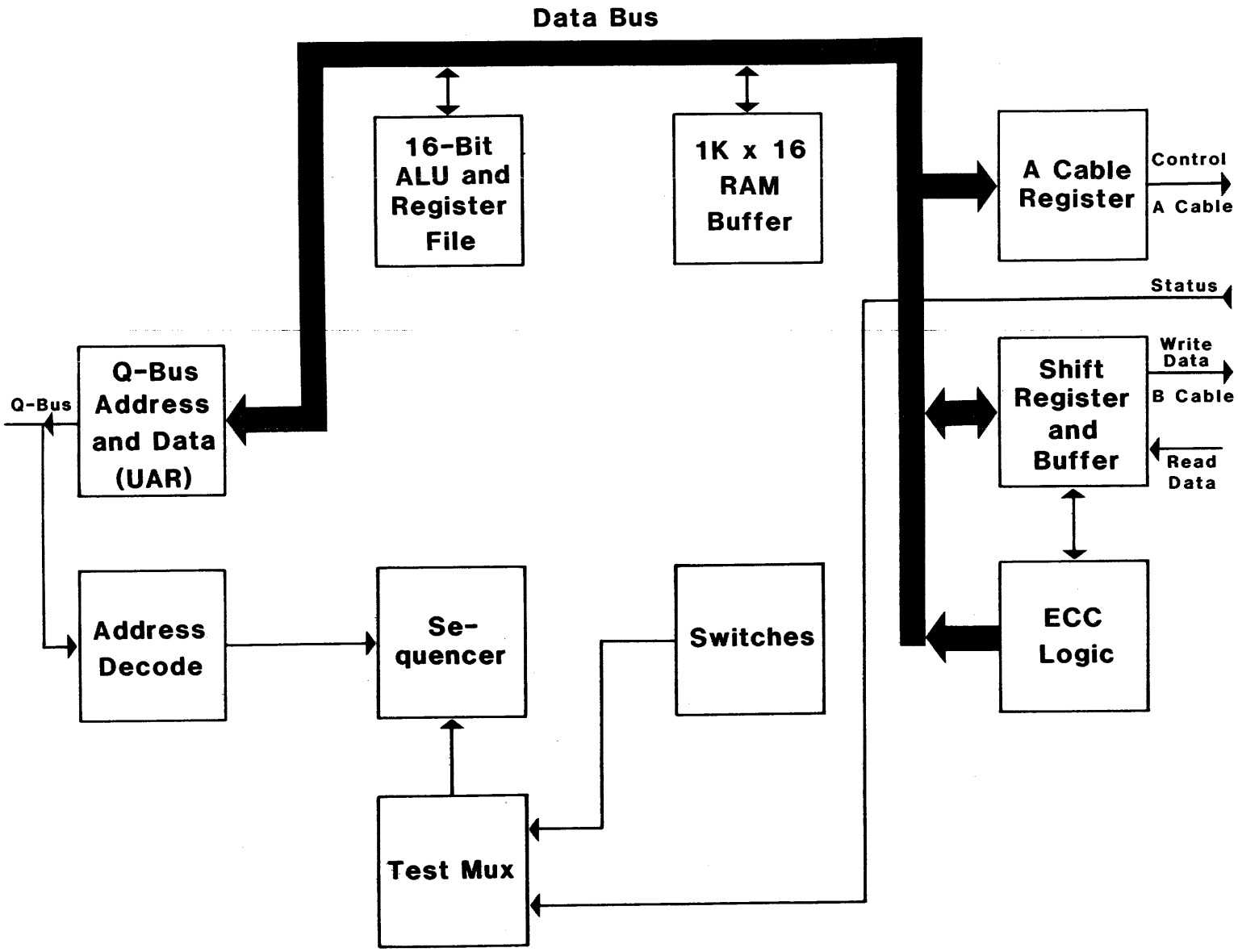
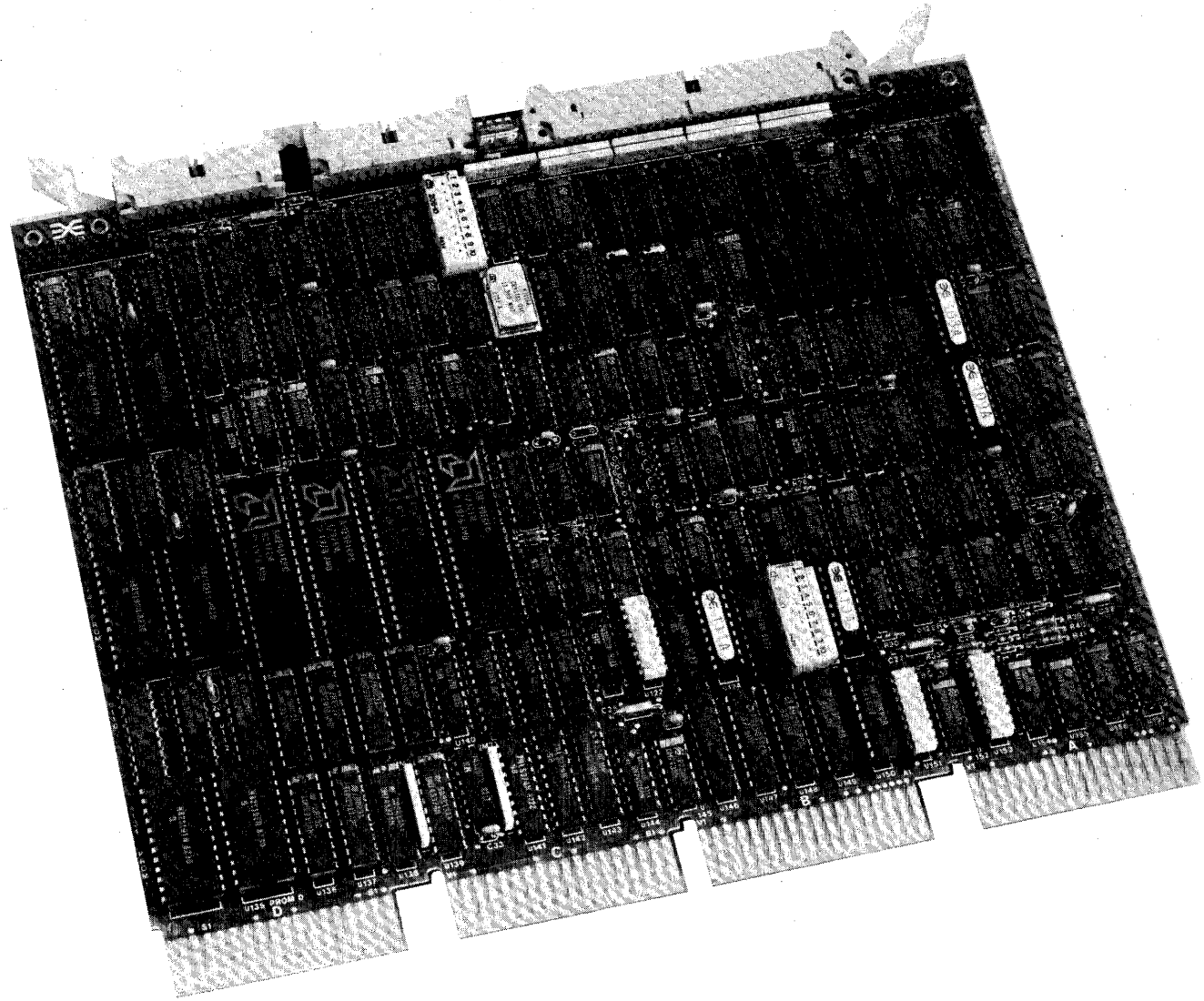



Figure 2-1 SC03 Block Diagram



SC0302-0080

Figure 2-2. SC03 Controller Board

### 2.2.1 Connectors

#### 2.2.1.1 A Cable Connector

The 60-pin flat cable connector labeled J3 at the top edge of the board is for the A Cable which daisy-chains to all the drives for control and status. Pin 1 is located on the right side of the connector.

#### 2.2.1.2 B Cable Connector

The two 26-pin flat cable connectors labeled J1 and J2 are for the radial B Cables to each of two physical drives which may be attached to the controller. Pin 1 is identified by an arrowhead on the connector. The two B Cable ports are identical and either drive may be plugged into either connector.

#### 2.2.1.3 Test Connectors

Connectors J4 and J5 are used with the Emulex test panel during manufacturing test and factory repair. They have no use in normal operation.

### 2.2.2 Switches

There are three sets of switches labeled SW1, SW2 and SW3. SW1 is a four pole DIP "piano-type" switch accessible from the PC board edge. SW1 is located so that it is accessible to the operator while the controller is imbedded in an LSI-type chassis.

Switches SW1, SW2 and SW3 provide controller address decoding selection, option selection and drive configuration selection. (See Section 3 for a complete description of the switch functions.)

### 2.2.3 LED Indicator

There is an LED indicator mounted between the B Cable connectors at the top of the board. The controller executes an extensive self-test when powering up. The microprogrammed organization of the controller permits most logic other than the interface circuitry to the disk to be validated before the controller becomes ready. The LED lamp is turned ON as the controller starts its self-test and is turned OFF only when the controller successfully completes the test. If a malfunction is detected by the built-in diagnostics, the LED remains ON and the controller will not respond to program I/O. The LED blinks at approximately a one second rate if the self-test is successful but no drive is seen on-line. The LED also functions as an activity indicator during read and write operations.

### 2.2.4 Firmware PROMs

There are six PROM sockets, used for the control memory, located along the left edge of the board when viewed from the component

side. The sockets are labeled PROM 0 through PROM 5 in a discontinuous physical order. The numbers on the top of the PROM ICs are Emulex part numbers, which identify the unique pattern of the PROM. See paragraph 3.5.3 for information on PROM replacement.

### 2.2.5 Bootstrap PROMs

There are two sockets provided for the installation of optional bootstrap PROMs. They are at location U71 and location U92. PROM number 794 goes in location U92, and PROM number 795 goes in location U71. The Emulex part number of the option kit is SC0313001. See paragraph 3.4.4.2 for information on the boot option.

## 2.3 INTERFACES

### 2.3.1 Disk Interface

The controller's disk interface conforms to the Flat Cable Interface Specification for the SMD, MMD, and CMD (CDC Document No. 64712400). The controller has been tested with most drives using the SMD, MMD and CMD interfaces and is compatible with the electrical and timing characteristics of such disk drives.

The following paragraphs define the electrical interface and the recommended cables.

#### 2.3.1.1 A Cable

The 60-conductor A Cable is daisy-chained to all disk drives and terminated at the last drive. The signals in this cable, along with their function when the control tag (Tag 3) is asserted, are listed in Table 2-1. The A Cable should be a 30-twisted-pair flat cable with an impedance of 100 ohms and a cumulative length of no greater than 35 feet.

Spectra-Strip P/N 455-248-60 flat cable or its equivalent is recommended. It is possible to order A-Cable assemblies from Emulex that are made up in one of four lengths:

| EMULEX P/N | LENGTH (FT.) |
|---|---|
| SU1111201 | 8.0 |
| SU1111203 | 15.0 |
| SU1111205 | 25.0 |
| SU1111207 | 35.0 |

#### 2.3.1.2 B Cable

The 26-conductor B Cable is radial to all drives and contains the data and clock signals. The signals and grounds in this cable are listed in Table 2-1. The B Cable should be a 26 conductor flat cable with ground plane and drain wire. The impedance should be 130 ohms and the length must not be greater than 50 feet.

Table 2-1
Disk Drive Connections

| Pins Lo/Hi | Signal | (Tag 3 Function) | From/To |
|---|---|---|---|
| A Cable: | | | |
| 22,52 | Unit Select Tag | | To |
| 23,53 | Unit Select bit 0 | | To |
| 24,54 | Unit Select bit 1 | | To |
| 26,56 | Unit Select bit 2 | | To |
| 27,57 | Unit Select bit 3 | | To |
| 1,31 | Tag 1 | | To |
| 2,32 | Tag 2 | | To |
| 3,33 | Tag 3 | | To |
| 4,34 | Bit 0 | (Write Gate) | To |
| 5,35 | Bit 1 | (Read Gate) | To |
| 6,36 | Bit 2 | (Servo Offset Plus) | To |
| 7,37 | Bit 3 | (Servo Offset Minus) | To |
| 8,38 | Bit 4 | (Fault Clear) | To |
| 9,39 | Bit 5 | (AM Enable) | To |
| 10,40 | Bit 6 | (Return to Zero) | To |
| 11,41 | Bit 7 | (Data Strobe Early) | To |
| 12,42 | Bit 8 | (Data Strobe Late) | To |
| 13,43 | Bit 9 | (Release) | To |
| 30,60 | Bit 10 | | To |
| 14,44 | Open Cable Detect | | To |
| 15,45 | Fault | | From |
| 16,46 | Seek Error | | From |
| 17,47 | On Cylinder | | From |
| 18,48 | Index | | From |
| 19,49 | Unit Ready | | From |
| 20,50 | Not Used | | From |
| 21,51 | Busy (dual port only) | | From |
| 25,55 | Sector | | From |
| 28,58 | Write Protected | | From |
| 29 | Power Sequence Hold | | To |
| 59 | Power Sequence Pick | | To |
| B Cable: | | | |
| 8,20 | Write Data | | To |
| 6,19 | Write Clock | | To |
| 2,14 | Servo Clock | | From |
| 3,16 | Read Data | | From |
| 5,17 | Read Clock | | From |
| 10,23 | Not Used | | From |
| 22,9 | Unit Selected | | From |
| 12,24 | Not Used | | From |
| 13,26 | Not Used | | From |

3M-P/N 3476/26 flat cable or its equivalent is recommended. It is possible to order B Cable assemblies from Emulex that are made up in one of three lengths:

| EMULEX P/N | LENGTH (FT.) |
|---|---|
| SU1111202 | 8.0 |
| SU1111204 | 15.0 |
| SU1111206 | 25.0 |

### 2.3.2 Q-Bus Interface

The LSI-11 Bus consists of 42 bidirectional and 2 unidirectional signal lines. These form the lines along which the processor, memory and I/O devices communicate with each other.

Addresses, data, and control information are sent along these signal lines, some of which contain time-multiplexed information. The lines are divided as follows:

1. Sixteen data/address lines - <BDAL00:BDAL15>
2. Six extended address lines - <BDAL21:BDAL16>
3. Six Data Transfer control lines - BBS7, BDIN, BDOUT, BRPLY, BSYNC, BWTBT
4. Three direct memory access control lines - BDMGI, BDMR, BSACK
5. Six interrupt control lines - BEVENT, BIAKO, BIRQ4, BIRQ5, BIRQ6, BIRQ7
6. Five system control lines - BPCOK, BHALT, BINIT, BPOK, BREF.

The MS four data/address lines (BDAL <21:18>) are used only for addressing and do not carry data. BDAL <17:16> reflect the parity status of the 16-bit data word during the data transfer portion of the bus cycle.

#### 2.3.2.1 Interrupt Priority Level

The controller is hardwired to issue level 4 and level 5 interrupt requests. The level 4 request is necessary to allow compatibility with either an LSI-11 or LSI-11/2 processor.

#### 2.3.2.2 Register Address

The register address and the number of registers assigned to the controller are decoded by a PROM at U124. The selections available are determined by configuration switches SW3-7 and SW3-8 as discussed in Section 3.

Table 2-2
Q-Bus Connections

| | A | | B | |
|---|---|---|---|---|
| | 1 | 2 | 1 | 2 |
| A | BIRQ5 | +5V | BPCOK | +5V |
| B | BIRQ6 | | BPOK | |
| C | BDAL16 | GND | BDAL18 | GND |
| D | BDAL17 | | BDAL19 | |
| E | | BDOUT | BDAL20 | BDAL02 |
| F | | BRPLY | BDAL21 | BDAL03 |
| H | | BDIN | | BDAL04 |
| J | GND | BSYNC | GND | BDAL05 |
| K | | BWTBT | | BDAL06 |
| L | | BIRQ4 | | BDAL07 |
| M | GND | BIAKI | GND | BDAL08 |
| N | BDMR | BIAKO | BSACK | BDAL09 |
| P | BHALT | BBS7 | BIRQ7 | BDAL10 |
| R | BREF | BDMGI | BEVENT | BDAL11 |
| S | | BDMGO | | BDAL12 |
| T | GND | BINIT | GND | BDAL13 |
| U | | BDAL00 | | BDAL14 |
| V | | BDAL01 | | BDAL15 |

#### 2.3.2.3 DCOK and INIT Signals

The DCOK and INIT signals both perform a Controller Clear. The self-test is performed only when DC power is initially applied.

## 2.4 DISK FORMAT

### 2.4.1 Disk Pack Organization

The formatting of a disk pack and the mapping of one or two logical drives onto a physical drive varies with the drive size. Some of this information is supplied by the configuration PROM.

### 2.4.2 Mapping

Depending upon the type and size of the disk drive, one or two logical units may be mapped on it. The controller can handle a maximum of four logical units distributed across a maximum of two physical drives. A logical drive may not be mapped across a physical unit boundary.

In most cases there is a 1:1 correspondence between logical and physical disk addresses. The controller has the capability to alter a logical address to a different physical address so that drives which do not match the number of tracks and cylinders of the unit being emulated can be run without software patches.

### 2.4.3 Sector Organization

Figure 2-3 shows the RM sector format used by the controller. With the exception of an additional two words, the RP sector format is similar. Each track of 20,160 bytes is divided into 32 sectors of 630 bytes. The four byte header is preceded by a preamble of 30 bytes ending in the sync byte and is followed by a two byte CRC. The 512 byte data field is preceded by a preamble of 20 bytes ending in the sync byte, and is followed by four bytes of ECC.

If the actual size of the useful data information is less than 256 words, the remainder of the data field will be filled with zeros until 256 words have been written. During disk formatting procedures, each data track is located and recorded with header information by means of the Write Header and Data command. A disk pack should be formatted and the format verified before any real data is written on it. Once formatted, individual or groups of sectors should not be reformatted unless absolutely necessary.

| Sector Length 630 Bytes | | | | | | |
|---|---|---|---|---|---|---|
| Preamble | Sync | Header | CRC | Preamble | Sync | Data Field | ECC | Recovery |
| 30 | | 6 | | 20 | | 512 | 4 | 58 |

Figure 2-3 Sector Format

Header Word 1:

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | SSF | 1 | 0 | Cylinder Address | | | | | | | | | | |

Header Word 2:

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Track Address | | | | | | | | Sector Address | | | | | | | |

Header Word 3:

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Cyclic Redundancy Code (CRC) | | | | | | | | | | | | | | | |

Figure 2-4 RM Header Format

### 2.4.4 Header

#### 2.4.4.1 RM Header Description

Figure 2-4 shows the RM header format, which consists of the following three words:

Word One: This word contains the cylinder address. It contains a 1 in bit 12 to identify 16-bit format to the software and 1-bits in bit positions 14 and 15 to identify a good sector. For RM80 emulations only, bit 13 will contain a 1-bit to identify skipped sectors and a 0-bit for normal sectors.

Word Two: The low-order eight bits of this word contain the sector address. Each track on the drive typically contains 32 sectors. The upper byte of this word contain the track address.

Word Three: This is the CRC word which is generated and checked by the controller logic. This word is not available to the software.

#### 2.4.4.2 RP Header Description

The RP header format consists of the following five words:

Word One: This word contains the cylinder address. It contains a 1 in bit 12 to identify 16-bit format to the software.

Word Two: The low-order eight bits of this word contain the sector address. Each track on the drive typically contains 22 sectors. The upper byte of this word contains the track address.

Words Three and Four: These are user words, and are not checked by firmware unless the replacement track mode is enabled.

Word Five: This is the CRC word which is generated and checked by the controller logic. This word is not available to the software.

#### 2.4.4.3 Header Field Handling

After the drive reports that it is on cylinder, the controller locates the desired sector by means of the sector counters. The sector counters for each drive are maintained in the controller. The controller compares the first two words of the header against the desired track, sector and cylinder and then checks the CRC word for errors. An error in the header field is indicated by turning on the appropriate error bit in the error register (format error,

header compare error, bad sector error, skip sector error or CRC error). A header error is only valid when the sector count field of the RPLA/RMLA register and the sector field of the RPDA/RMDA have already matched. It is immaterial where a CRC error occurs in the header field since the controller cannot determine its location in the field. However, software may read the header to memory by means of a Read Header and Data command. The header compare may be inhibited by setting the HCI bit in the RPOF/RMOF register.

## 2.5 GENERAL PROGRAMMING INFORMATION

### 2.5.1 Clearing the Controller

The controller is cleared by the following methods:

a. Controller Clear: Controller Clear is performed by writing a 1-bit into the CLR bit (bit 05 of RPCS2/RMCS2) or Q-Bus INIT. This causes the following registers to be cleared:

   RP Drives:

   RPCS1 bits <15:12>, <10:08>, <06:00>; RPCS2 bits <15:07>, <05:00>; RPBA bits <15:00>; RPBAE bits <15:00>; RPCS3 bits <15:04>. Sets bit 06 of RPCS2 and bit 07 of RPCS1.

   In all RP drives: RPER1; RPER2; RPER3; RPDA; RPEC1; RPEC2; RPAS ATA bit; RPOF bits <07:00>, RPDS ATA, ERR and LST bits; RPMR bits <15:09>, <07:00>. Sets bit 08 of RPMR.

   RM Drives:

   RMCS1 bits <15:12>, <10:08>, <06:00>; RMCS2 bits <15:07>, <05:00>; RMBA bits <15:00>; RMBAE bits <15:00>; RMCS3 bits <15:04>. Sets bit 06 of RMCS2 and bit 07 of RMCS1.

   In all RM drives: RMER1; RMER2; RMDA; RMAS ATA bit; RMEC2; RMDS ATA, ERR and LST bits; RMMR1 bits <15:04>, <02:00>. Sets bit 03 of RMMR1.

b. Error Clear: The Error Clear is performed by writing a one-bit into the TRE bit (bit 14 of RPCS1/RMCS1). This writing causes a clearing of RPCS1/RMCS1 bits 13 and 14, and bits <15:08> of RPCS2/RMCS2. RPCS1/RMCS1 SC bit (bit 15) is reset if RPAS/RMAS equals zero.

c. Drive Clear: The Drive Clear is a command. (Code 11) This command causes the following registers in the drive selected by U2-U0 to be cleared:

RP Drives:

ATA and ERR bits in RPDS; RPAS ATA bit; bits <15:09> and <07:00> in RPMR, bits <15:00> in RPER1, RPER2, RPER3, RPEC1, and RPEC2; and bits <07:00> in RPOF. Sets bit 08 of RPMR.

RM Drives:

ATA and ERR bits in RMDS; RMAS ATA bit; bits <15:04> and <02:00> in RMMR1; and bits <15:00> in RMER1, RMER2, and RMEC2. Sets bit 03 of RMMR1.

### 2.5.2 Interrupt Conditions

The controller generates an interrupt on the following conditions:

a. Upon termination of Data Transfer if interrupt enable is set when the controller becomes ready.

b. Upon assertion of attention or occurrence of a controller error (SC being set) while the controller is not busy and the interrupt enable is set.

c. When the program writes a one into IE and RDY at the same time. Note that this can be done by Read-Modify-Write instructions (BIS, ADD, etc.) which set the IE bit.

### 2.5.3 Termination of Data Transfers

A Data Transfer which has been successfully started may terminate in the following ways:

a. Normal Termination - Word count overflows to zero and the controller becomes ready at the end of the current sector.

b. Controller Error - An error occurs in the RPCS2/RMCS2 register bits <15:08>. Any of these errors sets TRE which terminates the Data Transfer immediately and makes the controller ready.

c. Drive Error - The ERR bit in the RPDS/RMDS register and at least one bit in an error register are set. TRE is also set and the controller becomes ready. The ATA for the drive doing the Data Transfer becomes asserted.

d. Program-Caused Abort - By performing a Controller Clear or a RESET instruction, the program can cause an abort of any operation. Status and error information is lost when this is done, and the controller and drive become ready immediately.

### 2.5.4 Ready Bits

RDY is the ready indicator for the controller. When RDY equals one, the controller is ready to accept a Data Transfer command. RDY is reset when the controller is doing a Data Transfer command. DRY is the ready indicator for the selected drive and is the complement of the drive's GO bit. To successfully initiate a Data Transfer command, both of these bits must be asserted. However, a non-data transfer command (Search, Drive Clear) may be issued to a drive at any time DRY is asserted regardless of the state of the RDY bit.

When a Data Transfer command is successfully initiated, both RDY and DRY become negated. When a non-data transfer command is successfully initiated, only DRY bit becomes negated.

The assertion of RDY after the execution of a Data Transfer command will not occur until the DRY bit is set and the controller is done. RDY is asserted on the completion of the last memory cycle (or at the time of an abort condition) and the last disk transfer.

If any command other than Drive Clear is issued to a drive which has ERR asserted, the command is ignored by the drive. If a Data Transfer command is issued to a drive which has ERR asserted, the drive does not execute the command and the missed transfer error (MXF, bit 09 in RPCS2/RMCS2 register) is set.

### 2.5.5 22-Bit Memory Addressing

Twenty-two-bit addressing capability is available as an option for the SC03/BX. The Emulex part number for the option kit is CS0113001. The kit consists of a single AMD2908 IC which is placed in socket U150 on the SC03 PCBA.

The controller can be switched from an RH11 mode (18-bit addressing) to an RH70 mode (22-bit addressing) by closing SW2-3. This will allow access to the RPBAE/RMBAE and RPCS3/RMCS3 registers which are a part of the RH70 only.

NOTE: A patch is required to enable 22-bit addressing with the following operating systems: RSX11M Plus (versions 2.0 and lower), RSX11M (version 3.2), and all versions of RSTS/E. The patch is available from:

Emulex Technical Support
3545 Harbor Blvd.
Costa Mesa, CA 92626
(714) 662-5600 TWX 910-595-2521

**WARNING**

Some manufacturers of Q-Bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing an SC03 with

the extended addressing option in such a system will damage the option IC. Before installing the option confirm that there is neither positive nor negative potential between lines BC1, BD1, BE1, BF1 and logic ground. An SC03 without the addressing option will not be damaged if power is present on those lines.

### 2.5.6 Line Time Clock (LTC)

The Line Time Clock is a 60 Hz clock generated by the power supply and distributed on the backplane as the BEVNT signal. A high to low transition of this signal interrupts the processor. BEVNT has the highest external interrupt priority; only processor interrupts have higher priorities. If external interrupts are enabled (PS bit 07 equals zero), the processor PC (R7) and PS words are pushed onto the processor stack. The LTC (or external event device) service routine is entered by vector address 100; the usual interrupt vector address input operation by the processor is not required since vector 100 is generated by the processor.

The LTC can be software controlled by using the Line Clock Register on the SC03/BX. The Line Clock Register has a bus address of 777546. It is a one-bit, write-only register. Reads to this register return all-zero data. Bit 06 is the only bit implemented. A write to this register with bit 06 set enables the line clock. A write to this register with bit 06 reset disables the line clock. The enable bit need not be set again after an interrupt has been processed. The clock will continue to interrupt until bit 06 is reset or an INIT is generated.

There is a jumper on the CPU that must be removed before the LTC interrupt vector is generated by the processor. See paragraph 3.4.4.12 for information on how to configure the processor for use with the LTC.

### 2.5.7 Bootstrap Routines

Installing the Emulex bootstrap option kit (number SC0313001) makes available two bootstrap routines: the standard console bootstrap and auto-boot sequence. See paragraph 3.4.4.2 for installation instructions.

#### 2.5.7.1 Standard Console Bootstrap

The CPU enters the standard console bootstrap routine at location 773000. The CPU board can be jumpered to start at location 773000 automatically on power-up (or external DCLO set-reset). See paragraph 3.4.4.2.

After performing several CPU tests, the bootstrap program will prompt the operator with a dollar sign ($) on the standard terminal (bus addresses 777560-777564). At this point the bootstrap routine

expects terminal input. If no $ is printed, then the boot program failed one of the CPU tests it executed prior to entering terminal input mode.

When the $ prompt has been printed, the boot program is ready for input from the terminal. The user should enter one of the two-character codes from Table 2-3 (plus a single octal number if one is required and the unit number to be booted is not zero) followed by a carriage return. The two-character codes represent bootstrap routines for specific device types. When the code is entered, the routine that the code represents will be executed. If the code is not recognized, a question mark (?) is printed, followed by the $. The code to use for the SC03/BX is "DB" or "DR".

If the code selected represents a peripheral device boot routine, then the controller will execute three more CPU tests and two memory tests prior to executing the actual boot. The two memory tests will check all available memory, but they require a minimum of 8K bytes (0-17776) to operate.

Table 2-3
Bootstrap Routines

| | | |
|---|---|---|
| XM | = | Execute memory tests only. |
| OD | = | ODT Halt. No routines executed. A proceed (P) returns the program to the terminal input mode. |
| MTn | = | TM11 mag tape boot. Can boot units 0-7. |
| DXn | = | RX01 floppy disk boot. Can boot units 0-1. |
| DKn | = | RK05 disk boot. Can boot units 0-7. |
| RPn | = | RP02/3 disk boot. Can boot units 0-7. |
| DMn | = | RK06/7 disk boot. Can boot units 0-7. |
| DBn | = | RM02/3/5/80, RP04/5/6 disk boot. Can boot units 0-7. |
| DYn | = | RX01/RX02 disk boot. Can boot units 0-7. |
| DLn | = | RL01/02 disk boot. Can boot units 0-7. |
| MSn | = | TS11 mag tape boot. Can boot units 0-7. |
| DD | = | TU58 (Unit 0 only) |

Note: If "n" is not entered, a default unit number of 0 is assumed.

The following is a list of halt locations which the PROM program will execute should the boot be unsuccessful.

| HALT Address | Reason for HALT |
|---|---|
| 765320 | Non-existent unit, unit not on-line and ready, controller ready equals one |
| 765612 | Read Error, Disk Error aborted read |
| 765674 | Read failed to complete within time limit |
| 773434 | Failure in CPU test #7 |
| 773530 | Failure in CPU test #8 |
| 773550, 773556, or 773604 | Failure in CPU test #9 |
| 773730 | Failure in Memory test #1 |
| 773760 | Failure in Memory test #2 |

2.5.7.2 Auto-boot Sequence

The auto-boot sequence will automatically bootstrap the system without operator intervention when the system is powered up or when an external DCLO signal is generated.

The CPU enters the auto-boot sequence at location 765000. The LSI-11/23 CPU can be jumpered to start at location 765000 automatically. See paragraph 3.4.4.2.

After performing a memory test, the auto-boot program will first attempt to boot the system from an RM02/03/05 or an RP06 at the standard address. The auto-boot program will only attempt to boot from drive zero.

If none of the above drives are present, the program will print the $ prompt and expect the operator to enter a device code as described in paragraph 2.5.7.1, above.

## 2.6 DUAL CONTROLLER OPERATION

SMD drives may be equipped with a Dual Port option which provides the capability for two controllers (generally on separate computers) to access the drive. The SC03/BX controller supports this type of operation as a standard feature. This mode of controller operation is selected by setting SW2-6 ON. Most of the dual port functions of the DEC controller being emulated are supported, and those which are not should be transparent to a properly written dual port driver. Table 2-4 summarizes the controller register responses in Dual Port operation.

### 2.6.1 Dual Port Drives

The two drive ports are known as Channel I and Channel II. Because only one controller may access the drive at a time, access is granted on a first-come, first-served basis. Once a controller has gained access to the drive, the other controller is denied access until the first controller's operation is complete. However, each channel has a physical disable switch which can disable the port and prevent the associated controller from having access to it.

### 2.6.2 Unseized State

The drive is in the unseized state when it is not logically connected to either controller. The CPU must issue a request for the controller to seize the drive. This request is done in one of the following ways:

a. Writing into any drive register, including read-only registers.

b. Writing a one-bit into the drive's ATA bit in RPAS/RMAS.

### 2.6.3 Seized State

The drive is seized when it is logically connected to one of the controllers. At that time DVA (RPCS1/RMCS1, bit 11) is set indicating that the drive is ready to communicate with the controller which has seized it. If the drive has already been seized by the other controller, then the DVA bit will not set, all the drive registers will read as zeros and any write to a register will be ignored. Attempts to seize a drive which is busy with the other port are remembered and then acted upon when the drive is released by the other controller.

### 2.6.4 Returning to the Unseized State

The drive is released and returned to the unseized state by issuing a Release command. In addition, a one second timer in the controller will timeout and release the drive if one of the events listed in section 2.6.2 for seizing the drive is not performed periodically to keep resetting the timeout timer. Reading the RPCS1/RMCS1 register will also reset the timeout timer if the drive is currently seized. This allows the CPU to check a drive's seized state, and if seized, not have to worry about a time-out release occurring.

When the controller sees a previously busy drive becoming unseized, it checks its request flag. If the flag is set (the drive had been requested while busy on the other port), the controller will seize the drive and set ATA causing an interrupt to the CPU if the IE bit is set. If the CPU does not respond to the attention within one second the drive will be released, but ATA remains set.

### 2.6.5 DEC Compatibility

The SC03/BX controller differs from the equivalent DEC controller in three important areas.

First, there is no neutral state. Since the SC03 does not have instantaneous access to all drives at the same time (a limitation of the daisy-chained A Cable and the microprocessor organization of the controller), the controller assumes the drive is busy on the other port if the controller has not already seized it. Thus, a read of RPCS1/RMCS1 will always indicate that the drive is seized by the other controller (DVA, bit 11 equals zero) unless the drive has been previously requested. The CPU must request the drive by writing into any drive register and wait until the ATA bit is set which indicates that the controller has seized the drive. If the drive was in reality not seized by the other controller, this will happen almost immediately. The DEC controllers, however, can switch from neutral to seized state within the time required to do a single read or write of a drive register. Thus, if the drive is not already seized, no ATA is set and the drive is immediately available to the seizing controller.

Second, the release command is not instantaneous since the controller takes a few microseconds to execute the command. During this time the drive will appear to be unseized.

Third, during a Data Transfer the timeout timers will not operate and the drives can not be polled to see if they are not busy. Therefore no drives are seized or released during the execution of a Data Transfer.

The software driver should not issue a Release command and then attempt to save the current status of a drive, since the Release command will immediately show the drive in the unseized state, thus returning zero data for the drive registers. In order to allow the other controller time to poll the drive, the CPU should not communicate with any of the released drive's registers until required to seize the drive again.

### 2.6.6 Dual Port Drives in Single Port Mode

When using an operating system which does not have dual port drive software support, it may still be advantageous to use dual port drives while operating in the controller in Single Port mode. This will allow for a non-dynamic type of operation between two CPUs. In this type of operation the controller does not unseize the drive and, in effect, it is seized by both controllers all the time.

The one second timeout timer (and the release command) operate exactly as stated in Paragraph 2.6.4. Even when released, a drive will still appear to be seized to the releasing controller. No attention is generated when the other controller finds the drive not busy. Should a command be issued to a controller while a drive

is busy on the other port, the controller will wait until the drive becomes unbusy before executing the command (no timer exists in this case).

This mode of operation eliminates the need for manually switching the drive from one controller to another.

### 2.6.7 Dual Access Mode

In order to provide compatibility with dual access software, the Dual Access mode is provided (SW2-7 ON). When in this mode, the controller sets Dual Port Mode (Drive Type Register) and Programmable (Drive Status Register) to imitate the DEC neutral state.

When DPM and PGM are set, the operating system will attempt to seize a drive by simply writing a command to it. If the drive is unbusy the command is executed. If the drive is already busy on its other port, the controller simply waits until it is released and then seizes and commands it. Software timers are sufficiently long to prevent causing a timeout when it is forced to wait.

The first time the SC03 sees a drive, it is ignored for one second. This one-second stall occurs once for each drive on the controller. It prevents the controller from seeing erroneous status information when power is applied to the drive after the controller has been powered-up. For a drive in Dual Port mode the stall will prevent the other CPU from accessing the drive until the stall completes. The Dual Access option switch bypasses the stall in all cases. For proper system operation with the dual access option switch ON, all drives must have power applied before either controller is powered-up.

Setting the Dual Port Option switch overrides the Dual Access Option, except for the one-second stall override.

### 2.6.8 Dual Port Drives Busy Signal

When operating dual port drives it is necessary to enable the busy signal. This is accomplished by setting SW2-9 OFF (open). When operating single port drives it is necessary to disable the undriven busy signal. This is accomplished by setting SW2-9 ON (closed). In two-drive configurations both drives must be of the same type (i.e., either both dual port or both single port dives). A dual port drive cannot be properly run with a single port drive that does not drive the Busy signal on the A Cable.

Table 2-4
Register Access on Dual Controller Operation

| Controller Action<br>Drive State: | Response With Respect To Action On Ch. I |
|---|---|
| **Read RPCS1/RMCS1** | |
| Drive Not Seized: | Reads the controller portion of RPCS1/RMCS1 only. The drive's portion is read as all zeros. No request flag is set. |
| Drive Seized by Ch. I: | DVA equals one; reads the register. Resets timer. |
| Drive Seized by Ch. II: | DVA equals zero; reads all zeros for the drive's portion of the register. No request flag is set. |
| **Read any other drive register** | |
| Drive Not Seized: | Reads all zeros. |
| Drive Seized by Ch. I: | Reads the register. |
| Drive Seized by Ch. II: | Reads all zeros. |
| **Write RPCS1/RMCS1** | |
| Drive Not Seized: | The function code is attempted if GO equals one. A port request flag is set. |
| Drive Seized by Ch. I: | Loads the function code. (Switches to unseized if the function is a Release). |
| Drive Seized by Ch. II: | The function code is attempted if GO equals one. A port request flag is set. |
| **Write any drive register** | |
| Drive Not Seized: | The write is ignored, and a port request flag is set. |
| Drive Seized by Ch. I: | Loads the register. |
| Drive Seized by Ch. II: | The write is ignored, and a port request flag is set. |

BLANK

Section 3
INSTALLATION

This section describes the step-by-step procedure for installation of the SC03/BX Disk Controller in an LSI-11 system. The following list is an outline of the procedure. Each step corresponds to a second level heading in this section (i.e., item one, Inspect the SC03, is covered in paragraph 3.1).

Emulex recommends that Section 3 be read in its entirety before installation is begun.

1. Inspect the SC03.
2. Prepare the disk drives.
3. Prepare the LSI-11.
4. Configure the SC03.
5. Install the SC03.
6. Route the drive I/O cables.
7. Test the system.

## 3.1 INSPECTION

Before unpacking the SC03/BX, examine the packaging for any signs of damage. Notify the carrier if any damage is noted.

A visual inspection of the board is recommended after unpacking. Specific checks should be made for such items as bent or broken connector pins, damaged components or any other visual evidence of physical damage. The PROMs should be examined carefully to ensure that they are firmly and completely seated in their sockets.

## 3.2 DISK DRIVE PREPARATION

The disk drive must be configured for the proper number of sectors and have an ID plug or address selection switches properly configured.

### 3.2.1 Drive Placement

Uncrate and install the disk drives according to the manufacturer's instructions. Position and level the disk drives in their final places before beginning the installation of the SC03. This positioning allows the I/O cable routing and length to be accurately judged. Place the drives side by side to make installation of the daisy-chained A Cable simpler.

### 3.2.2 Local/Remote

The Local/Remote switch controls whether the drive can be powered up from the drive (local) or the controller (remote). Place the switch in the REMOTE position. With the LSI-11 powered down, press the Start switch on the front panel of each of the drives (the Start LED will light, but the drive will not spin up and become ready). When the LSI-11 is powered up, the drives will spin up sequentially. This prevents the heavy current draw that would be caused if all of the drives were powered up at once. When in the remote mode the drives will power down when the LSI-11 is powered down. While the LSI-11 is powered ON, the drives may be powered up and down individually (to change disk media, for example) using the drive Start switch.

### 3.2.3 Sectoring

See Appendix A, Configuration Selection, for the correct sector count settings for the disk drives in use. The exact method of entering the sector count differs from one drive manufacturer to another and the particular drive manual should be consulted for the exact procedure. A minimum of 609 bytes per sector are required for proper operation.

### 3.2.4 Drive Numbering

An address from 0 to 3 must be selected for each drive. Be careful that no two drives are assigned the same number. To determine the number that each drive should be assigned, the user must first decide on the particular configuration that will be used. The drive numbers should then be assigned according to that configuration by matching the number of cylinders and tracks in Table A-2 to the drives. See paragraph A.2.1.2 for an example.

CDC drive addresses are selected by means of an address plug. Drives by other manufacturers have their addresses selected by switches on one of the logic cards. Consult the particular drive manual for the exact procedure.

### 3.2.5 Index and Sector Pulse Selection

The SC03 controller is designed to have the Index and Sector signals on the daisy chained A Cable and the signals must be gated by the unit select logic within the drive.

### 3.2.6 Lark Drive Configuration

The SC03/BX requires that the Seek-On-Head-Select switch in the Lark drive be ON. See the Lark drive hardware maintenance manual.

### 3.2.7 Memorex 677 Drive Configuration

Three models of Memorex drive are covered here, the 677-00 (200 Mb), the 677-30 (300 Mb) and the 677-70 (200 Mb). The 677-30 is merely an updated version of the 677-00 and configuration parameters are identical for these two drives. However, the switches on the option board (D07) are in different positions. Consequently, separate switch setting tables are given for the two models. For all drive models, configuration is done using the switches on the PCBA at location D07. For the 200 Mb drives, the sectors per track parameter is set to 22. The bytes per sector parameter for the 200Mb units is set to 609. The 300 Mb 677-30 has its sector per track parameter set to 32. The bytes per sector parameter for the 300Mb unit is 630. Of the other options available, the pad operations, suppress last sector and MFM data transfer features must be enabled for all models of the drive. The proper switch settings are listed in the three tables below. Card D09 must not be installed.

NOTE: The parameters entered for sector per track and bytes per sector are actually the desired number minus one as required by the Memorex drive logic.

Table 3-1
Memorex 677-00 Configuration Switch Settings

| 1A | 2J | 4A | 4H |
|---|---|---|---|
| 1-on | 1-off | 1-off | 1-on |
| 2-off | 2-on | 2-off | 2-off |
| 3-on | 3-off | 3-off | 3-on |
| 4-off | 4-off | 4-off | 4-on |
| 5-on | 5-off | 5-off | 5-off |
| 6-off | 6-on | 6-on | 6-on |
| 7-off | 7-on | 7-on | 7-on |
| 8-off | 8-off | 8-off | 8-off |

NOTE: For single port drives jumpers J1 to J3 on D07 must be installed. J1 does not exist on some cards.

Table 3-2
Memorex 677-70 Configuration Switch Settings

| 1B | 3B | 5B | 4G |
|---|---|---|---|
| 1-on | 1-off | 1-off | 1-on |
| 2-off | 2-on | 2-off | 2-off |
| 3-on | 3-off | 3-off | 3-on |
| 4-off | 4-off | 4-off | 4-on |
| 5-on | 5-off | 5-off | 5-off |
| 6-off | 6-on | 6-on | 6-on |
| 7-off | 7-on | 7-on | 7-on |
| 8-off | 8-off | 8-off | 8-off |

Table 3-3
Memorex 677-30 Configuration Switch Settings

| 1B | 3B | 5B | 4G |
|---|---|---|---|
| 1-on | 1-off | 1-on | 1-on |
| 2-on | 2-on | 2-off | 2-off |
| 3-on | 3-off | 3-on | 3-on |
| 4-on | 4-off | 4-off | 4-on |
| 5-on | 5-off | 5-on | 5-off |
| 6-off | 6-on | 6-on | 6-on |
| 7-off | 7-on | 7-on | 7-on |
| 8-off | 8-off | 8-off | 8-off |

## 3.3 SYSTEM PREPARATION

Power down the system and switch OFF the main AC breaker at the rear of the cabinet (the AC power indicator will remain lit). Slide the CPU out of the cabinet and remove the top cover. Tilt the card cage up to obtain access to the CPU and other modules.

## 3.4 CONTROLLER SETUP

Several configuration setups must be made on the controller before inserting it into the chassis. These are made by option switches SW1, SW2 and SW3.

Refer to Figure 3-1 for the locations of the configuration switch, PROMs and connectors on the SC03 Controller Board.

### 3.4.1 Controller Address Selection

All Q-Bus controllers have a block of several command and status registers through which the system can command and monitor the controller. The registers are addressed sequentially from a starting address assigned to that device type, in this case an RH70 or RH11 disk controller.

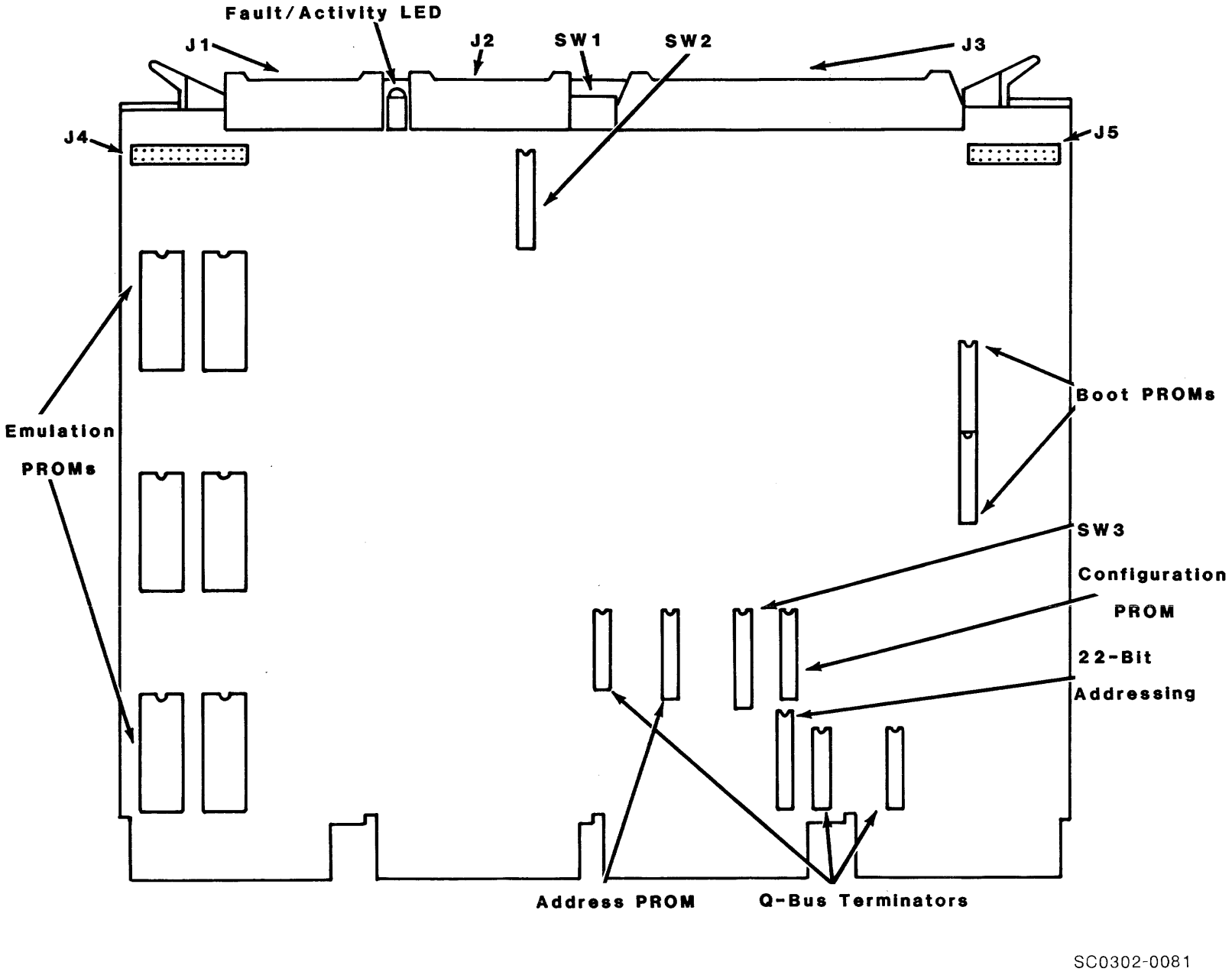



Figure 3-1 SC03 Controller Assembly

On the SC03 register addresses are decoded by PROM 696, located at U124. The starting address for the controller's Q-Bus registers is selected by DIP switch SW3. See Table 3-4 for register address switch settings. Make sure only one of the two switches is closed.

Table 3-4
Controller Address Switch Settings

| SW3-7 | SW3-8 | Address |
|---|---|---|
| O | C | 776700 (Standard) |
| C | O | 776300 (Alternate) |

### 3.4.2 Interrupt Vector Address

The interrupt vector address is selected by means of SW1-4, SW2-1 and SW2-2. The standard vector address is 254. The alternates are 150, 224, 270, 274, 354, 370 and 374. Listed below are the switch settings for the standard and alternate interrupt vector addresses.

| SW1-4 | SW2-2 | SW2-1 | Vector |
|---|---|---|---|
| O | O | O | 254 (Standard) |
| O | O | C | 150 (Alternate) |
| O | C | O | 370 (Alternate) |
| O | C | C | 374 (Alternate) |
| C | O | O | 354 (Alternate) |
| C | O | C | 224 (Alternate) |
| C | C | O | 270 (Alternate) |
| C | C | C | 274 (Alternate) |

### 3.4.3 Drive Configuration Selection

The phrase "drive configuration selection" describes the process that is used to select the logical disk drives that will be emulated by the SC03/BX controller when using a given set of physical disk drives. Using those disk drives and the SC03/BX, the user emulates a specific type and arrangement of DEC subsystems. (The emulated system is referred to as a logical disk drive.) Setting SW3-1 through SW3-6 on the controller allows selection of the logical disk drive configuration (limited, of course, by the physical disk drives available).

The SC03/BX has the capability to emulate both RM and RP type drives when certain configurations are selected. The drive types are roughly divided into three groups: RM02/03/05, RM80 and RP04/05/06. Each physical drive can support any drive type. When a physical drive has two logical units assigned to it, each logical unit is the same type and capacity, except the CDC 9448-96 drive. It has an RM02 as one logical unit and a different capacity RM03 as the other unit (see configuration numbers 20 and 22). Examples of configurations with mixed (both RP and RM) drive types may be seen in configuration numbers 42 and 43 in Table A-2.

For ease of manual maintenance, the configuration table for the SC03/BX is contained in Appendix A.

### 3.4.4 Options

There are a number of other SC03 options that can be implemented by the user. These features are selected by physically installing the option on the PCBA or by enabling it using one of the option switches.

#### 3.4.4.1 Q-Bus Terminator Option

To provide the equivalent of 120 ohms electrical termination to the Q-Bus, DIP resistor networks are installed in U122, U151, and U153. These resistor packs provide a 180 ohm resistor connection to +5 volts and a 390 ohm resistor connection to ground on each Q-Bus line.

These three resistor networks may be ordered from Emulex or the customer may provide his own terminating resistor networks by using an equivalent part such as BOURNS P/N 4116R-003-181/391, or BECKMAN 898-5-R180/390, or CTS 761-5-R181/391.

**WARNING**

> Some manufacturers of Q-Bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing an SC03 with the Q-Bus Terminator Option in such a system will damage the option ICs. Before installing the option confirm that there is neither positive nor negative potential between lines BC1, BD1, BE1, BF1 and logic ground. If there is power on any of the above lines and you wish to use the terminator option, cut pins 2, 3, 4 and 5 of the IC in socket U151. An SC03 without the option will not be damaged if power is present on those lines.

#### 3.4.4.2 Bootstrap PROM Option

The Bootstrap Option is a firmware routine executed by the CPU that loads the system memory with software that is stored on disk or tape. The option kit consists of two PROMs. Its Emulex part number is SC0313001. See paragraph 2.5.7 for operating information. This feature is enabled by opening (OFF) SW3-9 on the SC03 PCBA.

The bootstrap option has two sections; standard console bootstrap and auto-boot. The standard console bootstrap routine is entered by the CPU at address 773000, DEC's conventional starting address. The auto boot sequence is entered at address 765000.

The LSI-11 and LSI-11/02 both require that power-up mode 2 be selected to take advantage of the standard console bootstrap option. This is done by installing jumper W6 and removing jumper W5 on the CPU PCBA. The configuration for both the LSI-11 and the LSI-11/02 is the same. The auto-boot routine is not available for these units.

The LSI-11/23 may be configured to take advantage of either the standard console boot or the auto-boot routines. This CPU also requires that power-up mode 2 be selected (install jumper W6 and remove jumper W5 on the CPU PCBA). The bootstrap starting address, however, is selected using jumpers W8 through W15. To select the standard console bootstrap routine install W8. This will cause the processor to default to starting address 773000. To use the auto-boot option, remove W8, W10 and W12; install W9, W11, W13, W14 and W15.

In order to use this option on an LSI-11/23 Plus, a jumper connection must be made from J15 to J10 (on the CPU card).

3.4.4.3 22-Bit Memory Addressing

Twenty-two-bit addressing capability is available as an option for the SC03. The Emulex part number for the option kit is CS0113001. The kit consists of a single AMD2908 IC which is placed in socket U150 on the SC03 PCBA. The controller can be switched from RH11 (18-bit) mode to RH70 (22-bit) mode by closing SW2-3. See paragraph 2.5.5 for programming instructions.

NOTE: A patch is required to enable 22-bit addressing with the following operating systems: RSX11M Plus (versions 2.0 and lower), RSX11M (version 3.2), and all versions of RSTS/E. The patch is available from:

Emulex Technical Support
3545 Harbor Blvd.
Costa Mesa, CA 92626
(714) 662-5600 TWX 910-595-2521

**WARNING**

Some manufacturers of Q-Bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing an SC03 with the extended addressing option in such a system will damage the option IC. Before installing the option confirm that there is neither positive nor negative potential between lines BC1, BD1, BE1, BF1 and logic ground. An SC03 without the addressing option will not be damaged if power is present on those lines.

### 3.4.4.4 Sector Interleave

Option switch SW1-2 enables a 2:1 sector interleave (1:1 is the default). This feature requires an even number of sectors per track. This switch must be ON when using a Fujitsu 2351A (Eagle) drive. When this feature is enabled, some subtests in the Functional diagnostics will fail.

NOTE: Media compatibility (see paragraph 1.4.1) exists only so long as the SC03 is used with a 1:1 sector interleave.

### 3.4.4.5 Logical Unit Swap

The SC03/BX has the ability to swap logical units 0 and 1 with 2 and 3. For example, in configuration 0A, logical unit 0 would be an RM02, logical unit 1 would be an RM02, logical unit 2 would be an RM03 and logical unit 3 would be an RM03. This swap is accomplished by setting option switch SW2-4 ON (closed).

### 3.4.4.6 Replacement Track Mode

This option functions with RP units only, and requires a custom formatter provided by the user. When this mode is enabled, the DEC Formatter and some subtests in the Functional diagnostics will fail. This mode is enabled by setting option switch SW2-5 ON.

### 3.4.4.7 Dual Port Mode

Dual Port mode is selected by setting SW2-6 ON. This option should only be selected when used in conjunction with a properly written dual port driver. See paragraph 2.6. In addition, this mode should only be selected when the disk drive has dual ports and is configured for Dual Port operation. When this mode is enabled, the Functional diagnostics will not run.

### 3.4.4.8 Dual Access Mode

In order to provide compatibility with dual access software when it is configured for dual access, this mode is provided. To enable the Dual Access mode, SW2-7 must be ON. This mode should be selected only when the disk drive has dual ports and is configured for Dual Port operation. When this mode is enabled, some subtests in the Functional diagnostics will fail. See paragraph 2.6.7 for programming instructions.

### 3.4.4.9 DMA Bandwidth Control

This feature is enabled by setting SW2-8 ON and loading the proper register with a desired additional delay time period. See paragraph 5.5.1 for complete information on enabling this feature. When this feature is enabled, some subtests in the Functional diagnostics will fail.

### 3.4.4.10 A Cable Busy Bias

In order for dual port drives to function properly, the busy signal on the A Cable must be unbiased. This may be accomplished by setting option switch SW2-9 OFF (open).

### 3.4.4.11 Suspended DMA Operations

The controller will suspend its DMA operations temporarily whenever it sees the DMR signal active on the bus. This feature prevents data late conditions from occurring on other devices. This optional command is not enabled with a switch. See paragraph 5.5.3.

### 3.4.4.12 Line Time Clock Option

The Line Time Clock Option allows program control of the Line Time Clock. This feature is enabled by opening (OFF) SW3-10 on the SC03 PCBA. See paragraph 2.5.6 for programming instructions.

Before the LTC can be used, the CPU must be configured to enable that feature. On the LSI-11 and LSI-11/02, remove jumper W3 (BEVNT Line Enable). On the LSI-11/23, remove jumper W4 (BEVENT Line Enable). The LTC switch on the front panel must also be ON.

In order to use this feature on an LSI-11/23 Plus a jumper connection must be made from J11 to J10 (on the CPU card).

When using the SC03 with the RSTS operating system, the Line Time Clock Option must be enabled (SW3-10 = open). The CPU should be configured to enable the option.

### 3.4.4.13 Mapping Two RP06s on 19 Head Drives

This option allows two standard DEC RP06 drives to be mapped onto a 19-head drive. The drive must have 44 sectors per track, 815 cylinders, and at least 19 heads.

This option is enabled by setting switch SW1-3 ON (closed). Setting switch SW1-3 OFF (open) disables this option. SW1-3 should be OFF for use with drives with more than 19 heads.

NOTE: Use of this option requires Rev. D and above firmware.

## 3.5 PHYSICAL INSTALLATION

### 3.5.1 Slot Selection

If the three optional Q-Bus terminator resistor networks are installed, the SC03 should be installed in a quad slot such that it provides the termination required at the end of the bus, i.e., the last occupied slot.

If the optional Q-Bus terminators are not installed, the SC03 may be assigned to any desired slot since it uses the LSI four-level interrupt scheme to perform distributed interrupt arbitration.

### 3.5.2 Mounting

The controller board should be plugged into the LSI-11 backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the boards with the computer power OFF to avoid possible damage to the circuitry. Be sure that the board is properly positioned in the throat of the connector before attempting to seat the board by means of the extractor handles.

### 3.5.3 PROM Replacement

There are six emulation PROMs on the SC03 PCBA, located along the left edge of the board when viewed from the component side. The sockets are labeled PROM 0 to PROM 5 in a discontinuous physical order. When replacing PROMs, the ID numbers (found on top of the PROM), must be placed in the same sequence as the PROM numbers silkscreened on the board next to each socket.

To remove the existing PROMs, pry them from their sockets using an IC puller or a small screwdriver. When replacing PROMs make certain that they are firmly seated and that no pins are bent or misaligned. If the two rows of pins on the PROM are too far apart to fit into the socket, grasp the PROM at its ends, and, using your thumb and forefinger, bend one of the pin rows inward by pressing it against a flat surface (such as a table top).

## 3.6 CABLING

The subsystem cabling of the drives and controller is shown in Figure 3-2.

### 3.6.1 A Cable

The 60-wire A Cable should be plugged into the large connector on the controller and wired to the first drive. If more than one drive is used, it is then daisy-chained to the other drives. The last drive on the A Cable must have a terminator installed. This part is available from the drive manufacturer. The terminator is generally plugged into one of two A Cable connectors on the drive. In some cases, a ground wire emerging from the terminator assembly will have to be connected to the drive to provide a ground return for the resistors in the terminator. Pin 1 of the board connector is on the right. Pin 1 of the cable connector has a notch on the connector body to identify it. Twist and flat cable will have brown-brown twist followed by red-brown twist on the pin 1 edge of the cable. The cable will normally egress to the rear of the controller.

NOTE: The connector is not keyed and can be physically reversed in the header. No damage should result, but the system will not operate.

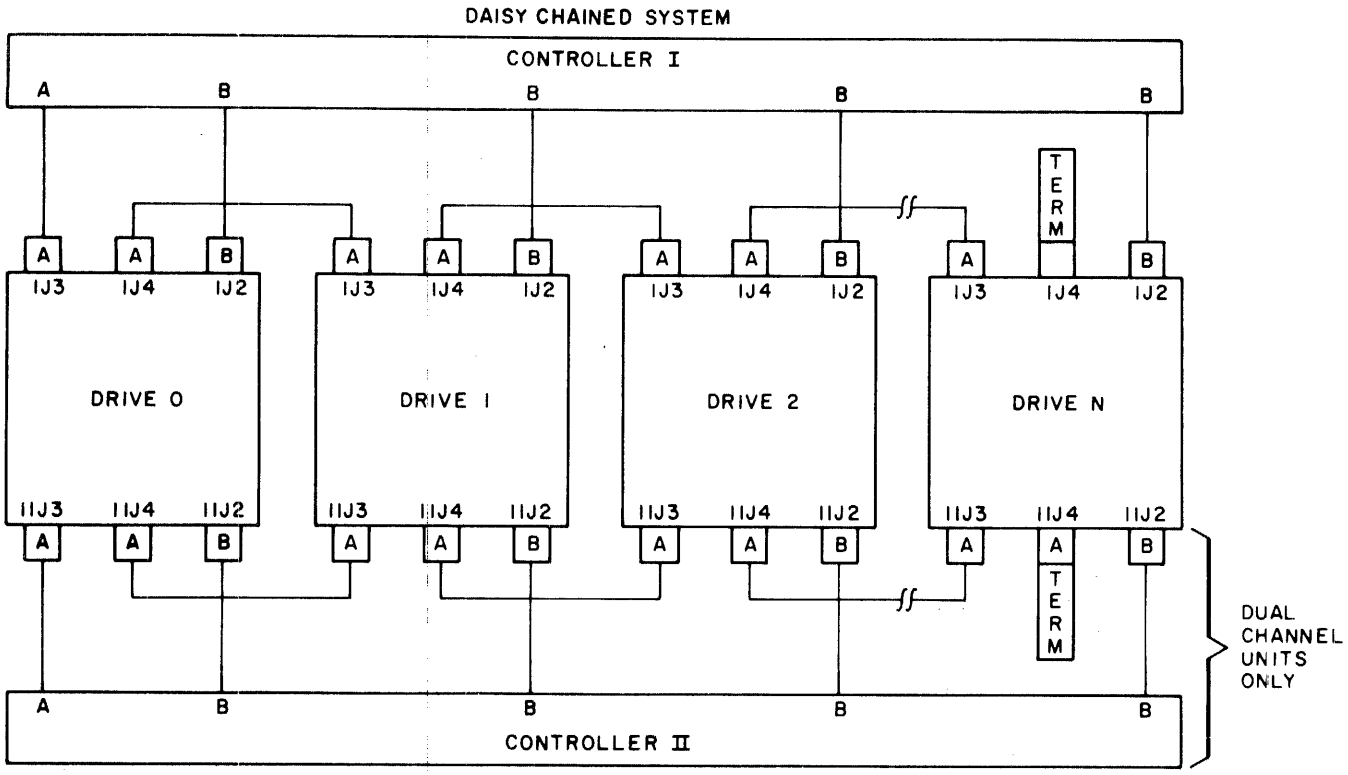



Figure 3-2 SC03 Cabling Diagram

### 3.6.2 B Cable

Each drive must have a 26-wire B Cable wired from the drive to one of the B ports of the controller. It makes no difference which B port connection is used by a drive. No external terminators are used with the B Cable. Pin 1 of the cable connector has a notch on the connector body to identify it. The pin 1 edge of the cable has a black stripe. Pin 1 of the board connector is on the right.

NOTE: Observe the same caution on connector reversal given in paragraph 3.6.1.

### 3.6.3 Grounding

For proper operation of the disk subsystem, it is very important that the disk drives have a good ground connection to the logic ground of the computer. The ground connection should be a 1/4 inch braid (preferably insulated) or AWG No. 10 wire or larger. The grounding wire may daisy-chain between drives. If the drive has a switch or jumper which connects the logical signal ground to the cabinet ground (DC ground to AC ground), this connection should be

removed once the drive is put on-line with the controller. It can be connected for performing local off-line maintenance on the drive.

NOTE: Failure to observe proper grounding methods will generally result in marginal operation with random error conditions. In particular, care must be taken when Fujitsu Eagle and CDC disk drives are placed on the same line. The procedures below should be followed on any system which mixes Eagles and CDC drives on the same daisy chain:

1. Disable Tags 4 and 5 on the Eagle as described on pages 3-7 of the Fusjitsu manual.

2. Use one of the following three grounding procedures:

   A. Install CDC drives with chassis (AC) and signal (DC) grounds connected together at the drive. Refer to the system grounding section of the CDC drive manual for details.

      Install grounding strap SG (DC) to FG1 (AC) on the Eagle.

      Install separate ground straps from each drive to the common system ground on the CPU.

   B. Install FCC-approved drive cables and attach all cable shields to the CPU and drive chassis grounds.

   C. Separate the chassis (AC) and signal (DC) grounds on each drive.

      Install FCC-approved cables and attach the shield grounds to the chassis (AC) ground of each drive. Daisy chain the signal(DC) ground of each drive to the signal (DC) ground of the controller.

3. If the cable from the controller to the **first** drive is less than 25 feet, place the Eagles first in the daisy chain. If the cable from the controller to the **first** drive is more than 25 feet, place the Eagles last on the daisy chain, closest to the terminator. If the **total** daisy chain length is more than 50 feet, use FCC approved cables whenever possible.

## 3.7 TESTING

Note: The register addresses given below are 18-bit addresses. For 22-bit machines add 17000000 to obtain the correct address for each register (i.e., 776700 becomes 17776700).

### 3.7.1 Self-Test

When power is applied to the CPU, the controller automatically executes a built-in self-test. This self-test is not executed with every bus INIT but only on powering up. If the self-test has been executed successfully, the LED on the top edge of the controller board will be OFF or flashing. The LED flashes when the controller cannot properly address at least one drive after successfully executing its self-test. This will occur if the A and B Cables are not properly plugged in, a drive is not powered up with a code plug, or two drives have an identical code plug. If the LED is ON steadily the controller did not pass its self-test and the controller cannot be addressed from the CPU.

### 3.7.2 Register Examination

After powering up the CPU and noting that the LED indicator is not ON steadily, a quick check should be made to ensure that the controller registers can be read from the computer console. Control Status Register 1 (776700) contains 004200 if the controller and drive 0 are ready and the drive is plugged into the controller.

### 3.7.3 Hardware Formatting the Disk

The controller has the means to format the disk by writing standard headers and zero data in all sectors of the disk. This command does not verify the data or headers.

If the drive is on line, the formatting is carried out as follows:

1. Perform a subsystem clear by depositing 000040 into RPCS2/RMCS2 (776710).

2. Select the drive to be formatted by depositing the drive number in the three least significant bits of RPCS2/RMCS2 (776710).

3. Deposit a pack acknowledge command (23) in RPCS1/RMCS1 (776700).

4. Deposit a 1777777 in RPCC/RMHR (776736).

5. Deposit a hardware format command (77) in RPCS1/RMCS1 (776700) to start formatting. The Activity LED will be lit during the format. The operation will finish in a couple of minutes with the RDY bit set in RPCS1/RMCS1.

### 3.7.4 Diagnostics

The DEC diagnostics should be run. Generally it will be necessary to run only the Formatter and the Performance Exerciser. See paragraph 1.4.3 for a list of diagnostics. See Appendix B for patches to the standard DEC RM02/03 diagnostics. See Appendix C for patches to the standard DEC RP06 diagnostics.

## 3.8 OPERATING SYSTEMS

When running the SC03/BX in 22-bit (RH70) mode on an LSI-11/23, the user must patch the software to bypass the set up of the (non-existent) Unibus maps. Emulex has application notes on how to do this for RSX-11M and RSX-11M Plus operating systems. The application notes are listed in Table 3-5.

Table 3-5
List of Operating System Patches

| Operating System | Version | Emulex Document Number |
|---|---|---|
| RSX-11M | V4.0 | SC0351401 |
| RSX-11M | V4.1 | No patches needed |
| RSX-11M Plus | V2.0 | SC0351402 |
| RSX-11M Plus | V2.1 | No patches needed |

BLANK

## 4.1 OVERVIEW

There are 20 or 22 device registers in the SC03/BX. The exact number of registers employed depends on the drive types used. These are used to interface the controller to the drives and the computer. The registers are loaded and/or read under program control in order to initiate selected disk commands and monitor status and error conditions. Most registers can be written into with word or byte operations.

The SC03/BX has the ability to emulate both RM and RP type drives when certain configurations are selected. Many registers in this section are both (but not simultaneously) RP and RM registers. Those that are not are indicated as such by their single (unslashed) mnemonic and are broken down into two third level headings. The second level header gives the address which is common to both registers. For example, section 4.12 lists 776724 as the address which pertains to both RMMR1 (4.12.1) and RPMR (4.12.2). Table 4-1 lists the registers and their names. Whether an RP or an RM register is activated depends on the drive configuration setup of the user (see Table A-2).

The RPWC/RMWC, RPBA/RMBA, RPCS2/RMCS2, RPDB/RMDB and bits <15:12> and <10:06> of RPCS1/RMCS1 are common to all drives. Loading and reading of these registers is independent of the unit selected. A separate set of the other registers and bits 11 and <05:00> of RPCS1/RMCS1 exists for each of the drives. Loading and reading of these registers is dependent on the drive selected by the unit number in RPCS2/RMCS2. In addition, the eight ATA bits in RPAS/RMAS are each associated with an individual drive. Any attempt to write into the drive registers (except RPAS/RMAS) while the drive's GO bit is asserted will cause a Register Modification Refused error and the register is not modified.

Table 4-1
Register Names and Addresses

| Register Name | Mnemonic | Address | Drive Type |
|---|---|---|---|
| Control/Status Register One | RPCS1/RMCS1 | 776700 | RP, RM |
| Word Count Register | RPWC/RMWC | 776702 | RP, RM |
| Bus Address Register | RPBA/RMBA | 776704 | RP, RM |
| Disk Address Register | RPDA/RMDA | 776706 | RP, RM |
| Control/Status Register Two | RPCS2/RMCS2 | 776710 | RP, RM |
| Drive Status Register | RPDS/RMDS | 776712 | RP, RM |
| Error Register One | RPER1/RMER1 | 776714 | RP, RM |
| Attention Summary Register | RPAS/RMAS | 776716 | RP, RM |
| Look-Ahead Register | RPLA/RMLA | 776720 | RP, RM |
| Data Buffer | RPDB/RMDB | 776722 | RP, RM |
| Maintenance Register | RMMR1 | 776724 | RM |
| Maintenance Register | RPMR | 776724 | RP |
| Drive Type Register | RPDT/RMDT | 776726 | RP, RM |
| Serial Number Register | RPSN/RMSN | 776730 | RP, RM |
| Offset Register | RPOF/RMOF | 776732 | RP, RM |
| Desired Cylinder Register | RPDC/RMDC | 776734 | RP, RM |
| Current Cylinder Register | RPCC | 776736 | RP |
| Holding Register | RMHR | 776736 | RM |
| Maintenance Register Two | RPER2 | 776740 | RM |
| Error Register Two | RPER2 | 776740 | RP |
| Error Register Two | RMER2 | 776742 | RM |
| Error Register Three | RPER3 | 776742 | RP |
| ECC Position Register | RPEC1/RMEC1 | 776744 | RP, RM |
| ECC Pattern Register | RPEC2/RMEC2 | 776746 | RP, RM |
| Bus Address Extension | RPBAE/RMBAE | 776750 | RP, RM |
| Control/Status Register Three | RPCS3/RMCS3 | 776752 | RP, RM |

## 4.2 CONTROL/STATUS REGISTER ONE (RPCS1/RMCS1) 776700

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SC | TRE | 0 | 0 | DVA | PSEL | A17 | A16 | RDY | IE | F4 | F3 | F2 | F1 | F0 | GO |
| ---Common To--- All Drives | | | | | | ---- Common To---- All Drives | | | | | | | | | |

The RPCS1/RMCS1 register can be read or written by program control, and is used to store the current disk command function code and operational status of the controller. Setting the GO bit will cause the controller to recognize the function code in the register and initiate the operation for the selected drive. The actual start of execution of the command does not begin when the function code is loaded into the control register, but commences when the controller has finished any previous operation and polls through the drive RPCS1/RMCS1 registers in search of a command needing initiation.

Special Condition (SC) - Bit 15

This read only bit is set as long as TRE in RPCS1/RMCS1 or any of the drive ATA bits are set. This bit causes a CPU interrupt if IE is also set.

Transfer Error (TRE) - Bit 14

This read/write bit is set by DLT, WCE, UPE, NED, NEM, PGE, MXF, or a drive error during a Data Transfer. Writing a one into the bit causes the Controller Error bits in RPCS2/RMCS2 to be cleared. These Controller Error bits are also cleared at the start of every Data Transfer operation.

Drive Available (DVA) - Bit 11

This read-only bit is set when the drive is seized by the controller. When not in Dual Port mode, the drive is seized as long as it is powered-up.

Port Select (PSEL) - Bit 10

This is a read/write bit that has no effect on any controller operations. (For diagnostic compatibility.)

Extended Bus Address (A16, A17) - Bits <09:08>

Upper extension of the RPBA/RMBA register. This two-bit counter is incremented by one every time RPBA/RMBA overflows. These bits cannot be altered if RDY equals zero and no error results when attempted. Replicated in RPBAE/RMBAE if RH70 mode is enabled (see paragraph 4.22).

Ready (RDY) - Bit 07

This read-only bit is reset when the controller starts a Data Transfer Command (codes 51 - 77) and is set at the termination of the Data Transfer operation.

Interrupt Enable (IE) - Bit 06

When IE is set an interrupt can be generated when RDY is asserted at the end of a Data Transfer or by any ATA being asserted. It is reset automatically when the interrupt is accepted by the CPU. When a zero is written into IE by the program, any pending interrupts are cancelled. An interrupt is generated by writing ones into IE and RDY at the same time. Replicated in RPCS3/RMCS3 if RH70 mode is enabled (see paragraph 4.23).

Function Code (F4-F0) - Bits <05:01>

F4-F0 and the GO bit make up the Function (command) code which determine the action to be performed by the controller and drive as shown below:

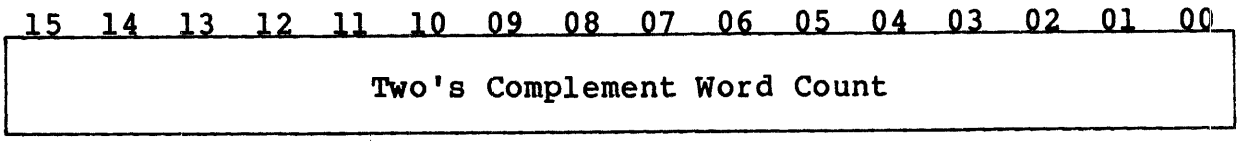
| | | | |
|---|---|---|---|
| 01 | No Operation | 35 | Suspended DMA Stall Count* |
| 03 | Unload (RP only) | 37 | Transparent ECC Correction* |
| 05 | Seek Command | 41 | Word Count Equals Sector Count* |
| 07 | Recalibrate | 51 | Write Check Data |
| 11 | Drive Clear | 53 | Write Check Header and Data |
| 13 | Release | 55 | Physical Write Check Header and Data* |
| 15 | Offset Command | 61 | Write Data |
| 17 | Return to Centerline | 63 | Write Header and Data |
| 21 | Read-In Preset | 65 | Physical Write Header and Data* |
| 23 | Pack Acknowledge | 71 | Read Data |
| 25 | DMA Bandwidth Set* | 73 | Read Header and Data |
| 27 | DMA Burst Length* | 75 | Physical Read Header and Data* |
| 31 | Search Command | 77 | Format* |

*Optional

GO (GO) - Bit 00

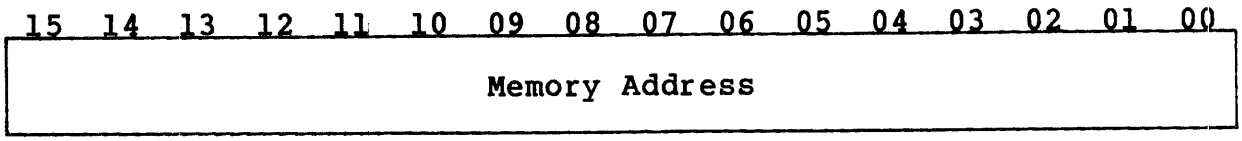
The GO bit must be set to cause the controller to respond to a command. The GO bit is reset after command termination.

## 4.3 WORD COUNT REGISTER (RPWC/RMWC) 776702




The RPWC/RMWC register is loaded with the two's complement of the number of data words to be transferred to or from main memory. The register is incremented by one after each word transferred, and accommodates a maximum transfer of 65,536 words. The RPWC/RMWC register is not cleared by INIT or Controller Clear.

## 4.4 BUS ADDRESS REGISTER (RPBA/RMBA) 776704




The RPBA/RMBA register is initially loaded with the low-order 16 bits of the memory address for a Data Transfer. The low-order bit (00) is always forced to a zero. The RPBA/RMBA register is incremented by two after transfer of a word to or from memory, unless the BAI bit is set. RPBA/RMBA is cleared by INIT or Controller Clear.

## 4.5 DISK ADDRESS REGISTER (RPDA/RMDA) 776706

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Track Address | | | | | | | | Sector Address | | | | | | | |

This register is used to address the sector and track on the disk to or from which a transfer is desired. It can only be loaded as a word. The RPDA/RMDA is incremented each time a sector of data is transferred so that consecutive blocks are automatically addressed when the word count indicates that more than one block is to be transferred. At the end of a transfer, RPDA/RMDA contains the address of the sector following the last one involved in the Data Transfer.

For RM drives, this register is a full 16-bit read/write register. For RP drives, only bits <13:08> and <04:00> are read/write. The rest are zeros.

The RPDA/RMDA contains a sector counter providing up to 32 or 64 sectors per track. The register also contains a track counter which is incremented by one every time the sector counter overflows its maximum count. When the sector address and the track address reach their maximum counts, they are reset to zero and the RPDC/RMDC is incremented by one. The Invalid Address error (IAE, RPER1/RMER1, bit 10) is set if the address in the RPDA/RMDA is invalid when a Data Transfer, Seek, or Search function is initiated. The maximum sector and track addresses are obtained from the selected configuration.

## 4.6 CONTROL/STATUS REGISTER TWO (RPCS2/RMCS2) 776710

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DLT | WCE | BPE | NED | NEM | PGE | MXF | MDPE | OR | IR | CLR | PAT | BAI | U2 | U1 | U0 |

The RPCS2/RMCS2 register can be read or written under program control and is used to store the current drive select code and controller operational status. In addition, the register can initiate a Controller Clear operation. It is recommended that writes to the unit select bits be done with byte operations since two of the error bits in the upper byte are read/write.

### Data Late (DLT) - Bit 15

This bit cannot normally be set because of the fourteen-sector buffer in the controller. It can be set by accessing RPDB/RMDB without the appropriate status bit (06 or 07) in RPCS2/RMCS2 set to a one. This is a read-only bit.

Write Check Error (WCE) - Bit 14

Set when the controller is performing a Write Check operation and a word from the disk does not match the corresponding word in memory. When the mismatch occurs, the reading of the disk terminates and the WCE bit is set. The memory address displayed in RPBA/RMBA is the address of the word following the one which did not match (if BAI is not set). The mismatched data word on the disk is displayed in the data buffer (RPDB/RMDB). RPDA/RMDA and RPDC/RMDC contain the address of the sector following the one that caused the error. This is a read-only bit.

Bus Parity Error (BPE) - Bit 13

Set if a parity error occurs in the system memory while the controller is performing a Write or Write Check command. When the error occurs, the RPBA/RMBA register contains the address of the word following the word with the parity error (if BAI is not set). This is a read/write bit in RH11 mode, and a read-only bit in RH70 mode.

Nonexistent Drive (NED) - Bit 12

Set when the program Reads or Writes a device register associated with a drive (selected by U2-U0) which is not recognized because of a wrong code plug, not powered up, or is non-existent. This is a read-only bit.

Nonexistent Memory (NEM) - Bit 11

Set when the controller is performing an NPR transfer and the memory does not respond within 10 microseconds. The memory address displayed in RPBA/RMBA is the address of the word following the memory location causing the error. This is a read-only bit.

Program Error (PGE) - Bit 10

Set when the program attempts to initiate a Data Transfer operation while the controller is currently performing one. This is a read-only bit.

Missed Transfer (MXF) - Bit 09

Set if a Data Transfer cannot be executed (RPDS/RMDS ERR bit equals one). This is a read/write bit in RH11 mode, and read-only in RH70 mode.

Massbus Data Bus Parity (MDPE) - Bit 08

This read-only bit is always a zero.

Output Ready (OR) - Bit 07

Set when a word is present in RPDB/RMDB and can be read by the program. Cleared by reading RPDB/RMDB. Any attempt to Read RPDB/RMDB register before OR is asserted will cause a DLT error. This is a read-only bit.

Input Ready (IR) - Bit 06

This read-only bit is always a one.

Controller Clear (CLR) - Bit 05

When a one-bit is written into this bit position, the controller is initialized. This is a write-only bit. It is always read as a zero.

Parity Test (PAT) - Bit 04

This read-write bit has no effect on any controller operation. (For diagnostic compatibility.)

Bus Address Increment Inhibit (BAI) - Bit 03

When BAI is set, the controller will not increment the RPBA/RMBA register during data transfers, causing all data words to be read from or written into the same memory location. This is a read/write bit.

Unit Select (U2-U0) - Bits <02:00>

These bits select one of eight drives for communicating with the CPU. The Unit Select bits can be changed at any time without interfering with current operations. These are read/write bits.

## 4.7 DRIVE STATUS REGISTER (RPDS/RMDS) 776712

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ATA | ERR | PIP | MOL | WRL | LST | PGM | DPR | DRY | VV | 0 | 0 | 0 | 0 | 0 | OFM |

This register contains various status indicators for the drive selected by the unit number in RPCS2/RMCS2. The register is a read-only register.

Attention Active (ATA) - Bit 15

An Attention condition will set the ATA bit in this register and The Attention Summary register (RPAS/RMAS). It is cleared by INIT, Controller Clear, loading a command with the GO bit set or loading a 1-bit in RPAS/RMAS register corresponding to the drive's unit number. The last method of clearing the ATA bit will not clear the error indicators.

An Attention condition is caused by: an error in the error registers; the completion of a positioning operation; the change of state of the MOL bit; Dual Port operation with the drive presently available if previously not available; correct sector identification for the Search command; completion of the Unload command.

Error (ERR) - Bit 14

Set when one or more of the errors in the error registers (RPER1/RMER1, RPER2 or RPER3/RMER2) for a selected drive is set. While ERR is asserted, commands other than Drive Clear are not accepted.

Positioning in Progress (PIP) - Bit 13

Set when a positioning command is accepted. These commands are: Seek, Offset (RP drives only), Return-to-Centerline (RP drives only), Recalibrate, and Search. Cleared when the moving function is completed at the time the DRY and ATA bits are set. Also set during implied and mid-transfer seeks executed as part of a Data Transfer command. For RM02/03/05 drives, set if MOL equals zero.

Medium On-Line (MOL) - Bit 12

Set when the Unit Ready line from the drive is asserted indicating that the drive is up to speed, the heads are positioned over the recording tracks and no fault condition exists within the drive. Cleared when the spindle is powered down or the drive is off-line. Whenever the MOL bit changes state, the ATA bit is set.

Write-Lock (WRL) - Bit 11

Set when the Write Protected line from the drive is asserted as enabled by a switch located on the drive. A Write command on a write-locked drive will cause the Write-Lock error (WLE, bit 11 of RPER1/RMER1) to be set. For RM80 drives, set if MOL equals zero.

Last Sector Transfer (LST) - Bit 10

Set when the last addressable sector on the disk pack has been read or written. Cleared when a new write to RPDA/RMDA is received.

At the time LST is set, the RPDA/RMDA register is reset to zero and the RPDC/RMDC register increments by one to the first illegal cylinder address. If the RPWC register is not zero, a mid-transfer Seek command will abort, causing the AOE status bit (RPER1/RMER1, bit 09) to be set, indicating that the desired cylinder register overflowed during a Read or Write.

Programmable (PGM) - Bit 09

This bit is set when Dual Port or Dual Access operation is enabled.

Drive Present (DPR) - Bit 08

This bit is set if the controller has seized the drive and is reset when the other controller has seized the drive. This bit is a reflection of the DVA bit in RPCS1/RMCS1.

Drive Ready (DRY) - Bit 07

Set at the completion of every command and cleared at the initiation of a command. When set, this bit indicates the readiness of the drive to accept a command. If a mechanical movement command was initiated, the ATA bit will also be set when DRY is set. This bit is the complement of the drive's GO bit.

Volume Valid (VV) - Bit 06

Set by the Pack Acknowledge or Read-In Preset commands. Cleared whenever the drive cycles up from the OFF state. When reset, this bit indicates that the drive has been off-line and a disk pack may have been changed.

Offset Mode (OFM) - Bit 00

This bit is enabled only with RM drives. Set by the Offset command to indicate that a read will be done with the heads in the offset position as determined by RMOF bit 07. Cleared by a Read-In Preset, Return-to-Centerline, Recalibrate or Write command, or a mid-transfer Seek command.

## 4.8 ERROR REGISTER ONE (RPER1/RMER1) 776714

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DCK | UNS | OPI | DTE | WLE | IAE | AOE | HCRC | HCE | ECH | WCF | FER | PAR | RMR | ILR | ILF |

The RPER1/RMER1 register is a read/write register that is used to store the error status of the drive whose unit number is in RPCS2/RMCS2. The RPER1/RMER1 register can only be written as a word. Any attempt to Write a byte will cause an entire word to be written. If the program attempts to Write into this register while the drive is busy, an RMR (RPER1/RMER1 register, bit 02) error is set, and the contents of the register are not otherwise modified. Writing zeros into this register should not be used as the normal way of clearing errors. The Drive Clear command should be used instead.

Data Check (DCK) - Bit 15

Set during a Read operation when the ECC hardware detects an ECC error. The Data Transfer terminates with the current sector. If the Error Correction Inhibit (ECI) bit is off, the controller will

go into the error correction process, and the RDY bit will not be set until the end of the process. If ECI bit is on, the error correction process is inhibited, the Data Transfer terminates immediately.

Unsafe (UNS) - Bit 14

This bit is a composite error bit of the unsafe and seek incomplete error conditions in RPER2 and RPER3/RMER2 registers. With UNS set, correct results on any operation cannot be guaranteed. Some faults must be cleared by manual intervention at the drive.

Operation Incomplete (OPI) - Bit 13

Set when a Read or Write command involving header search cannot find the physical sector within three Index pulses. Also set during a Search operation where a sector count match is not made within three Index pulses. When OPI is set, the GO bit is cleared and the RDY bit is set.

Drive Timing Error (DTE) - Bit 12

Set when either the header or data sync pattern is not found. When DTE is set, the GO bit will be cleared and the RDY bit set. Also set if a Sector pulse occurs before the end of a sector's data field.

Write Lock Error (WLE) - Bit 11

Set when a Write command is issued to a write-locked drive.

Invalid Address Error (IAE) - Bit 10

Set when the address in RPDC/RMDC or RPDA/RMDA is invalid and a Seek, Search or Data Transfer command is initiated.

Address Overflow Error (AOE) - Bit 09

Set when the RPDC/RMDC register overflows during a Read or Write operation indicating that the address has exceeded the cylinder address limit. With AOE set, the controller will terminate the operation when the last sector of the last cylinder has been read or written.

Header CRC Error (HCRC) - Bit 08

Set by a CRC error in the header. If a CRC error is detected during a Read or Write command, the controller will not make any Data Transfer. In the event of a CRC error during a Read Header and Data command, the entire sector will be transferred with the HCRC bit set.

Header Compare Error (HCE) - Bit 07

Set when the first two words of the header read at the sector whose count is equal to the desired sector field of RPDA/RMDA do not match the contents of RPDC/RMDC and RPDA/RMDA. If the HCE bit is set during a Read or Write command, the controller will not perform any Data Transfer. In the event of a Read Header and Data command, the entire sector will be transferred with the HCE bit set.

ECC Hard Error (ECH) - Bit 06

Set when the error correction procedure indicates that the error was a non-correctable ECC error. DCK (bit 15) is also set.

Write Clock Fail (WCF) - Bit 05

This bit is normally a zero unless written into.

Format Error (FER) - Bit 04

Set if the FMT16 bit in RPOF/RMOF does not match bit 12 in word 1 of a sector's header. The controller does not implement 18-bits per word mode. If FER is set, then HCE may not be set.

Parity Error (PAR) - Bit 03

This bit is normally a zero unless written into.

Register Modification Refused (RMR) - Bit 02

Set when a Write is attempted to any drive register (except RPMR/RMMR1 or RPAS/RMAS) with DRY equals zero. The drive will continue to execute the command in progress.

Illegal Register (ILR) - Bit 01

This bit is normally a zero unless written into.

Illegal Function (ILF) - Bit 00

Set when the function code in RPCS1/RMCS1 is illegal and the GO bit is set.

## 4.9 ATTENTION SUMMARY REGISTER (RPAS/RMAS) 776716

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ATA 7 | ATA 6 | ATA 5 | ATA 4 | ATA 3 | ATA 2 | ATA 1 | ATA 0 |

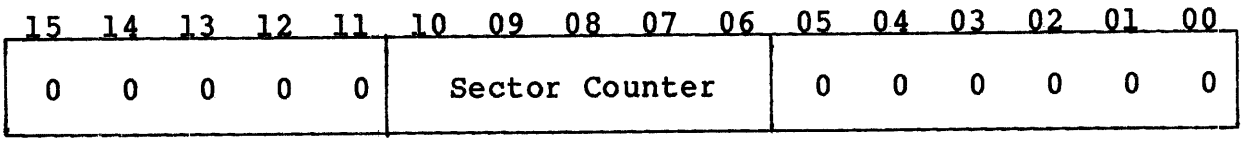
The RPAS/RMAS register allows the program to examine the attention status of all drives with only one Register Read operation. It also provides a means of resetting the attention logic in a selected group of drives. The eight low-order bits of this

register correspond to the ATA bits in the RPDS/RMDS of the drive having the same unit number as the bit position of this register.

A drive's ATA bit can be reset by loading a one into the bit position corresponding to the drive's unit number. Loading a zero has no effect. For a program to use the RPAS/RMAS without losing status information, the program must use MOV instructions for all Writes to this register. An instruction that does a Read-Restore (such as BIS) may cause bits that became asserted just prior to the Read to be lost. This register can be read or written at any time.

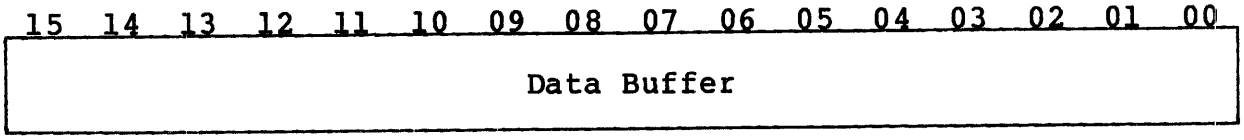
A persistent error, just like any error condition, will cause the ATA bit to be reasserted. Attempts by the controller to clear the error will not work in this case.

## 4.10 LOOK-AHEAD REGISTER (RPLA/RMLA) 776720




The RPLA/RMLA register contains the drive sector counter and is used to present the angular position of the disk relative to the read/write heads for the disk whose unit number appears in RPCS2/RMCS2. The purpose of this register is to provide the programmer with a means of optimizing disk accesses by minimizing rotational delays. The counter counts from zero to the maximum sector count selected for the drive.

## 4.11 DATA BUFFER (RPDB/RMDB) 776722




The RPDB/RMDB register provides a maintenance tool to check the controller data paths. The IR (Input Ready) and OR (Output Ready) status indicators in RPCS2/RMCS2 registers are provided so that the programmer can determine when words can be read from or written into RPDB/RMDB.

RPDB/RMDB is used as an access to the Silo Buffer for a DEC drive. This controller has no Silo Buffer. All Write operations to this register are ignored. If a Write-Check error occurs, the data word, as read from the disk, is placed in RPDB/RMDB and the OR bit in RPCS2/RMCS2 is set. Reading RPDB/RMDB resets OR. Any further attempts to read RPDB/RMDB will create a DLT error.

## 4.12 MAINTENANCE REGISTERS 776724

### 4.12.1 Maintenance Register (RMMR1)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | MUR | MOC | MSER | MDF | 0 | 0 | MWP | 0 | 0 | DMD |

RMMR1 is a read/write register that allows a program to simulate various signals from the disk for diagnostic testing of the controller. The DMD bit must be set before any other bit has an effect on the controller. This register may be written into as a word or a byte. Writing to RMMR1 can occur at any time regardless of the status of the drive. A drive or controller Clear resets this register except for bit 03, which is set.

Maintenance Unit Ready (MUR) - Bit 09

Set by a diagnostic program to simulate the Unit Ready signal from the drive.

Maintenance On Cylinder (MOC) - Bit 08

Set by a diagnostic program to simulate the On Cylinder signal from the drive.

Maintenance Seek Error (MSER) - Bit 07

Set by a diagnostic program to simulate the Seek Error signal from the drive.

Maintenance Drive Fault (MDF) - Bit 06

Set by a diagnostic program to simulate the Fault signal from the drive.

Maintenance Write Protect (MWP) - Bit 03

Set by a diagnostic program to simulate the Write Protect signal from the drive.

Diagnostic Mode (DMD) - Bit 00

Set by the diagnostic program to reconfigure the drive into Maintenance mode. None of the other bits in this register have any effect on the controller unless DMD is one. Before a drive can be set to Maintenance mode, it must first be ready and not busy. No positioner motion is initiated for a Seek, Home, Search or Implied Seek and all Data Transfer commands are ignored.

### 4.12.2 Maintenance Register (RPMR)

The Maintenance mode is not supported for RP units, except that if DMD equals one, then no Seek operations occur, and all Data Transfers are bypassed.

## 4.13 DRIVE TYPE REGISTER (RPDT/RMDT) 776726

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | MOH | 0 | DPM | 0 | 0 | 0 | Drive Type Code | | | | | | | |

Moving-Head (MOH) - Bit 13

This bit is always a one indicating that the drive is a moving-head device.

Dual Port Mode (DPM) - Bit 11

When set, this bit signifies that the drive is operating in Dual Port mode as selected by SW2-6 or Dual Access mode as enabled by SW2-7.

Drive Type Code - Bits <07:00>

This code specifies the type of drive as follows:

20 - RP04 21 - RP05 22 - RP06
24 - RM03 25 - RM02 26 - RM80 27 - RM05

## 4.14 SERIAL NUMBER REGISTER (RPSN/RMSN) 776730

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SW2 -8 | SW2 -7 | SW2 -6 | SW2 -5 | SW2 -4 | SW2 -3 | SW2 -2 | SW2 -1 | Firmware Rev. | | | | Port No. | | | |

The purpose of the RPSN/RMSN register was to distinguish a drive From similar drives attached to the controller by means of a four-decade serial number. Here, it consists of the controller port number for which the drive is attached, the firmware revision level, and the eight SW2 switch settings.

## 4.15 OFFSET REGISTER (RPOF/RMOF) 776732

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X | 0 | 0 | FMT 16 | ECI | HCI | SSEI | 0 | OFS 7 | X | OFS 5 | OFS 4 | X | X | X | X |

The RPOF/RMOF register contains inhibit bits, the drive offset direction bit and two offset function bits. The offset direction bit determines if a Read will be done with the heads and/or PLO advanced or retarded from normal position.

The following paragraph describes functions which exists with RP drives only. Although bit 07 is not exclusive to RP drives, bits 05 and 04 are. The status of OFS5 and OFS4 determines the actual offset. Bits <12:10> are cleared by a Read-in Preset command. Bits <07:00> are reset by INIT, and Drive Clear command. Bits marked 'X' are read/write but they have no affect on controller operation.

With RM drives, bits <15:00> are cleared by a Read-In Preset, but no bits are reset by INIT or Drive Clear command. SSEI is used in RM80 drives only.

Format Bit (FMT 16) - Bit 12

Set for 16 bit mode and reset for 18 bit mode. Since the controller only handles 16 bits/word format, this bit should always be a one. When reset, the controller operates with two fewer sectors per track.

Error Correction Code Inhibit (ECI) - Bit 11

Set to inhibit error correction when an ECC error is detected.

Header Compare Inhibit (HCI) - Bit 10

Set to inhibit header compare and CRC check. With HCI set, the controller depends only on the sector count for sector identification. It is recommended that the HCI bit be reset during a Write operation.

Skip-Sector Error Inhibit (SSEI) - Bit 09

For RM80 emulations only. Set to inhibit Skip-Sector errors during a header check. When this bit is set the drive operates with one extra sector per track. This bit is reset whenever a Data Transfer command increments RMDA to a new track address. This bit cannot be set unless the FMT16 bit is already set.

Offset Direction (OFS7) - Bit 07

Set under software control to select the direction of positioner and/or PLO offset. A one retards and a zero advances.

PLO Offset Enable (OFS5) - Bit 05

This bit enables the data strobe advance/retard and is enabled only with RP drives. There is no PLO offset with RM drives.

Positioner Offset Enable (OFS4) - Bit 04

This bit enables the positioner offset. This bit is enabled only with RP drives. For RM drives positioner offset is implied.

## 4.16 DESIRED CYLINDER REGISTER (RPDC/RMDC) 776734

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | Desired Cylinder Address | | | | | | | | | | |

The RPDC/RMDC register contains the address of the cylinder to which the positioner is to move. The RPDC/RMDC register will be cleared by the Read-in Preset command. Following an initial load, the value in the RPDC/RMDC register will be incremented by one whenever the RPDA/RMDA register is reset to zero during a Data Transfer. When the RPDC/RMDC register is incremented and the RPWC/RMWC register is not equal to zero, a mid-transfer Seek is initiated by the controller.

The Invalid Address Error (IAE) bit will be set when, upon asserting the GO bit, the RPDC/RMDC register contains an address greater than the largest addressable cylinder.

## 4.17 CURRENT CYLINDER AND HOLDING REGISTERS 776736

### 4.17.1 Current Cylinder Register (RPCC)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | Current Cylinder Address | | | | | | | | | | |

The RPCC register is a read-only register that reflects the approximate position of the positioner. It is made equal to RPDC at the end of a Seek operation. Other functions are as follows: If the register is written into with one of the values listed below, it is possible to read out the configured size of the selected disk from the same register.

100027 - Maximum cylinder address
100030 - Maximum track address
100031 - Maximum sector address (FMT16 bit must be set)

Writing a $177777_8$ into the register enables several optional commands (see Section 5) to be executed when loaded into RPCS1. The enable remains set until either the end of a Data Transfer command or the writing of some data other than $177777_8$ into RPCC.

### 4.17.2 Holding Register (RMHR)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RMHR is a read-only register that always returns a zero when read except as follows: If the register is written into with one of the

values listed below, it is possible to read out the configured size of the selected disk from the same register.

100027 - Maximum cylinder address
100030 - Maximum track address
100031 - Maximum sector address (FMT16 bit must be set)

Writing a $177777_8$ into the register enables several optional commands (see Section 5) to be executed when loaded into RMCS1. The enable remains set until either the end of a Data Transfer command or the writing of some data other than $177777_8$ into RMHR.

## 4.18 MAINTENANCE AND ERROR REGISTERS TWO 776740

### 4.18.1 Maintenance Register Two (RMMR2)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $11777_8$ | | | | | | | | | | | | | | | |

RMMR2 is a read-only register. It will return a $11777_8$ when read with drive connected and selected via RMCS2.

### 4.18.2 Error Register Two (RPER2)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | PLU | 0 | IXE | 0 | MDS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Error Register 2 is a read/write register that contains status information relating to the performance of the drive whose unit number is in RPCS2. This register may be written as a word only. If any bit is set in this register, then the ERR bit in RPDS is also set. In some cases, the UNS bit in RPER1 will also be set. Writing zeros into this register should not be used as the normal way of clearing errors. A Drive Clear or a Controller Clear should be used instead. If the program attempts to write into this register while the drive is busy, the RMR bit in RPER1 will be set and the Write will be ignored.

PLO Unsafe (PLU) - Bit 13

Set if the controller does not detect at least 16 servo clocks within 3.0 microseconds.

Index Error (IXE) - Bit 11

Set when the controller detects more than 128 Sector pulses without an Index pulse.

Multiple Drive Select (MDS) - Bit 09

Set if more than one drive responds to a logical address on the A Cable.

## 4.19 ERROR REGISTERS TWO AND THREE 776742

### 4.19.1 Error Register Two (RMER2)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BSE | SKI | OPE | IVC | LSC | LBC | MDS | 0 | DVC | ACU | SSE | 0 | DPE | 0 | 0 | 0 |

RMER2 is a read-write register that contains status information relating to the electromechanical performance of the drive whose unit number is in RMCS2. This register may be written as either a word or a byte. If any bit is set in this register, then the ERR bit in RMDS is also set. In some cases, the UNS bit in RMER1 will also be set. Writing zeros into this register should not be used as the normal way of clearing errors. A Drive Clear or a Controller Clear should be used instead. If the program attempts to write into this register while the drive is busy, the RMR bit in RMER1 will be set and the Write will be ignored.

Bad Sector Error (BSE) - Bit 15

Set whenever the controller detects a zero in bit 14 or 15 of the first header word and the HCI bit in RMOF equals zero. HCE in RMER1 may also be set.

Seek Incomplete (SKI) - Bit 14

Set whenever a Seek Error is received from the drive. This error also sets the UNS bit in RMER1. The controller automatically issues a Fault Clear and a Return-to-Zero to the drive if a Seek Error is detected.

Operator Plug Error (OPE) - Bit 13

Set whenever the drive's address plug is removed and then reinstalled. This bit can be cleared by issuing a Drive Clear.

Invalid Command (IVC) - Bit 12

Set whenever any command is issued to a drive with MOL equals zero. Set whenever any command except a Read-in Preset or a Pack Acknowledge is issued to a drive with VV equals zero.

Loss of Sector Clock (LSC) - Bit 11

Set when the controller detects more than 128 Sector pulses without an Index pulse.

Loss of Bit Clock (LBC) - Bit 10

Set if the controller does not detect at least 16 servo clocks within three microseconds.

Multiple Drive Select (MDS) - Bit 09

Set when more than one drive responds to a logical address on the A Cable. This bit cannot be set by a program.

Device Check (DVC) - Bit 07

Set if a Fault indication is received from the drive. This error also sets the UNS bit in RMER1. The controller automatically issues a Fault Clear and a Return-to-Zero to the drive if a Fault is detected.

AC Power Unsafe (ACU) - Bit 06

Set if an ACLO indication is received from the Q-Bus.

Skip-Sector Error (SSE) - Bit 05

For RM80 emulations only. Set whenever bit 13 of the header Word One is set and bit 09 of RMOF is reset. This error indicates that the sector has been skipped and the data resides in the next sector. This bit cannot be written into unless the drive is an RM80.

Data Parity Error (DPE) - Bit 03

This bit is normally a zero unless written into.

4.19.2 Error Register Three (RPER3)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OCYL | SKI | OPE | 0 | 0 | 0 | 0 | 0 | 0 | ACL | 0 | 0 | URW | 0 | 0 | 0 |

Error Register Three is a read/write register that contains status information relating to the electromechanical performance of the drive whose unit number is in RPCS2. This register may be written as a word only. If any bit is set in this register, then the ERR bit in RPDS is also set. In some cases, the UNS bit in RPER1 will also be set. Writing zeros into this register should not be used as the normal way of clearing errors. A Drive Clear or a Controller Clear should be used instead. If the program attempts to write into this register while the drive is busy, the RMR bit in RPER1 will be set and the Write will be ignored.

Off-Cylinder (OCYL) - Bit 15

Set if an off-cylinder indication occurs at the completion of a Seek operation. Also sets UNS in RPER1.

Seek Incomplete (SKI) - Bit 14

Set whenever a Seek Error is received from the drive. This error also sets the UNS bit in RPER1. The controller automatically issues a Fault Clear and a Return-to-Zero to the drive when a Seek error is detected.

Operator Plug Error (OPE) - Bit 13

Set whenever the drive's address plug is removed and then reinstalled. Can be cleared by issuing a Drive Clear.

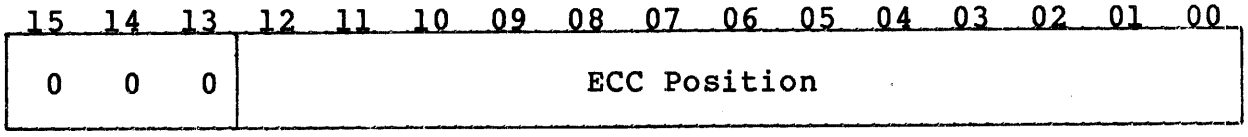
AC Power Unsafe (ACL) - Bit 06

Set if an ACLO indication is received from the Q-Bus.

Unsafe to Read or Write (URW) - Bit 03

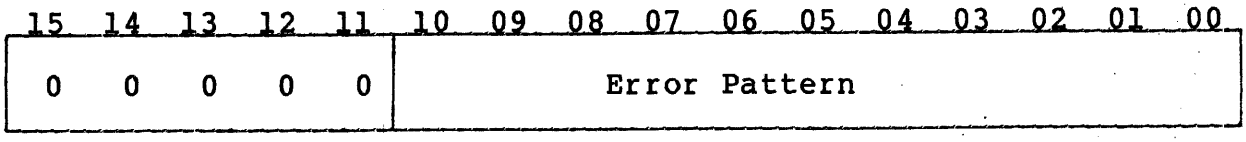
Set if a fault indication is received from the drive. Also sets UNS in RPER1. The controller automatically issues a Fault Clear to the drive when a fault indication is received from the drive.

4.20 ECC POSITION REGISTER (RPEC1/RMEC1) 776744




The Error Correction Code (ECC) Position register is a read-only register that contains the position of the error pattern as determined by the ECC correction procedure. The error position is the number of bit positions from the beginning of the sector's data field to (and including) the right-most bit position of the error pattern stored in RPEC2/RMEC2. If the detected error is not correctable using ECC, the ECH error bit in RPER1/RMER1 will be set.

4.21 ECC PATTERN REGISTER (RPEC2/RMEC2) 776746




The Error Correction Code (ECC) Pattern register is a read-only register that contains the 11-bit error correction pattern obtained from the ECC correction procedure. A one in the error pattern indicates a bit of the data in memory from the last read sector

which is in error. The error pattern may straddle two 16-bit words in memory. The bit displacement to the right-most bit of the pattern is determined by the bit count in RPEC1/RMEC1. The actual correction is done by an exclusive-OR of the error pattern and the data in memory.

## 4.22 BUS ADDRESS EXTENSION (RPBAE/RMBAE) 776750

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A21 | A20 | A19 | A18 | A17 | A16 |

This register contains the upper 6 bits of the memory address which is combined with the lower 16 bits in RPBA/RMBA to form the complete 22-bit address. The 6-bit field is incremented each time the RPBA/RMBA overflows. Note that A16 and A17 are replicated in RPCS1/RMCS1. Writing in either affects both. This register is accessible only when the controller is operating in RH70 mode.

## 4.23 CONTROL/STATUS REGISTER THREE (RPCS3/RMCS3) 776752

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | DPE HI | DPE LO | WCE HI | WCE LO | 0 | 0 | 0 | 0 | IE | 0 | 0 | IP 3 | IP 2 | IP 1 | IP 0 |

This register is accessible only when the controller is operating in the RH70 mode.

### Data Parity Errors (DPE HI and LO) - Bits 14 and 13

Set if parity error is detected on data read from memory when performing a write or write check command. Also sets BPE in RPCS2/RMCS2.

### Write Check Errors (WCE HI and LO) - Bits 12 and 11

Set if data fails to compare between memory and the disk on a write check command. Also sets WCE of RPCS2/RMCS2.

### Interrupt Enable (IE) - Bit 06

When IE = 1, an interrupt may occur due to RDY or SC being asserted. Cleared when the interrupt is recognized. Writing 0 into IE by the program cancels any pending interrupts. This bit is replicated in RPCS1/RMCS1. Writing into either affects both.

### Invert Parity (IP3:IP0) - Bits <03:00>

These bits are used to invert and test cache parity on a DEC RH70 controller. They have no effect on the Q-Bus.

BLANK

## 5.1 OVERVIEW

Operations on the drive selected by the Unit Select bits in RPCS2/RMCS2 are initiated by loading the function code and GO bit into RPCS1/RMCS1. The function code specifies a specific command. The commands can be divided into three categories: Data Transfer commands, Positioning commands, and Housekeeping commands. Commands and their corresponding function codes (always odd since the GO bit must be asserted to execute the command) are described below.

Some commands are divided into two descriptions, one of which describes how it functions with RP drives, and the other describing its function with RM drives. Those that are divided as such can be distinguished by the fourth level heading.

## 5.2 DATA TRANSFER COMMANDS

These commands involve Data Transfers to or from the disk and are designated by function codes 51 through 77.

All Data Transfer commands have seek and sector search functions implied. When the desired cylinder does not equal the current cylinder during the execution of the Data Transfer, a Seek command will be issued to the desired cylinder. The controller will then search the desired track for the desired sector and, when found, will start the Data Transfer. On all commands except the Write Header and Data command (which is the format operation) and Read Header and Data command, a match of the sector header must be made before the Data Transfer is started. If the header compare inhibit (HCI bit 10 in RPOF/RMOF) is set, the header will not be compared or checked and, like the Write Header and Data command, the transfer will be started based on the pre-recorded Sector pulses. With the HCI bit set, header errors will not be reported. With the HCI bit cleared, the transfer will be aborted if a header error is detected. The Read Header and Data command aborts only the transfers following the sector that caused the error. A Write Check Header and Data command operates the same as the Read Header and Data command.

The desired sector, track and cylinder addresses are updated after the transfer of a sector. Therefore, at the end of a transfer, the disk is set up to transfer the next sequential sector. This allows multiple sector transfers and spiral transfers across tracks and cylinders. When the desired cylinder address changes during a Data Transfer operation, the implied Seek is performed and is termed a Mid-Transfer Seek.

The header size is two words for RM drives, and four words for RP drives. In all cases the data field size is 256 words.

The Data Transfer commands are described below:

### 5.2.1 Write Check Data (51)

This command reads data from the selected drive and compares it on a word by word basis with that obtained from memory. If the data fails to compare, the WCE status bit is set and the command is terminated immediately. For additional information on Write Check errors see Section 4.11 and the WCE bit in Section 4.6.

### 5.2.2 Write Check Header and Data (53)

This command reads the header field and data field from the selected drive and compares it on a word by word basis with data obtained from memory. If the header and data fail to compare, the WCE status bit is set and the command is terminated immediately.

### 5.2.3 Write Data (61)

This command writes the 256-word data field of the selected sector with words obtained from memory. A two word ECC is appended to each sector. If the word count in RPWC/RMWC goes to zero during the sector, the rest of the sector is zero filled. After a sector transfer the word count in RPWC/RMWC is checked; if not zero, the Data Transfer operation is continued to the next sector; otherwise the command is terminated by setting the RDY bit.

### 5.2.4 Write Header and Data (format operation) (63)

This command writes the header field and the data field of the selected sector with words obtained from memory. A one word CRC is appended to each header field, and a two word ECC is appended to each data field. After a sector transfer the word count in RPWC is checked; if not zero, the Data Transfer operation is continued to the next sector; otherwise the command is terminated by setting the RDY bit. If RPWC/RMWC goes to zero during the sector, the rest of the sector is zero filled.

### 5.2.5 Read Data (71)

This command reads the 256-word data field from the selected sector and transfers the data to memory. When the sector Data Transfer is complete, the ECC is checked to ensure that the data read from the disk was error free. If a data error occurred, the ECC correction procedure is initiated (if the ECI bit in RPOF/RMOF is reset) to determine whether the error is correctable. When finished, the command is terminated to allow software to apply the correction information. Assuming no data errors, the word count in RPWC/RMWC is checked; if not zero, the Data Transfer operation is repeated with the next sector. No data is transferred after RPWC/RMWC goes to zero.

### 5.2.6 Read Header and Data (73)

This command transfers the header field and the data field from the selected sector to memory. When the sector Data Transfer is complete, the ECC is checked to ensure that the data read from the disk was error free. If a data error occurred, the ECC correction procedure is initiated (if the ECI bit in RPOF/RMOF is reset) to determine whether the error is correctable. When finished, the command is terminated to allow software to apply the correction information. Assuming no data errors, the word count in RPWC/RMWC is checked; if not zero, the Data Transfer operation is repeated with the next sector.

## 5.3 POSITIONING COMMANDS

Positioning commands are mechanical movement commands used to position the heads over the disk pack and take milliseconds to complete. Upon initiating the Positioning commands, the controller will set the PIP bit and reset the DRY bit. Upon completion of the Positioning operation, the controller resets the PIP and GO bits, sets the DRY bit and sets the ATA bit. The Positioning commands are described below:

### 5.3.1 Unload (03)

This command is valid for RP units only. The command is intended to cause the drive to retract its heads and stop the spindle. This can not be done with SMD-type drives, so the command is simulated. A three second cycle-down/cycle-up sequence is generated in the controller. At the end of the sequence, the controller resets the GO bit, resets Volume Valid, sets MOL, DRY and ATA, and performs a Drive Clear. The MOL bit is reset for the duration of the cycle-down/cycle-up sequence.

### 5.3.2 Seek Command (05)

This command causes the heads to be moved to the cylinder address specified by the contents of RPDC/RMDC. When the controller sees the Seek command with the GO bit set, it sends the cylinder address to the corresponding drive. Any attempt to write into RPDC/RMDC while the Seek is in progress will cause the RMR bit to be set and RPDC/RMDC will not be modified. Upon completion of the Seek operation, the ATA and DRY bits in RPDS/RMDS are set, and the GO bit is reset. If the drive is unable to complete a move within 500 milliseconds or if it has moved the carriage to a position outside the recording field, the drive asserts the Seek Error signal and the controller sets the appropriate seek error bit(s). The ERR, ATA and DRY bits in RPDS/RMDS are also set. The controller will automatically issue a Fault Clear and a Return-to-Zero to the drive so that Drive Clear command can clear the error. The Seek Error is not reported until the Return-To-Zero terminates.

### 5.3.3 Recalibrate (07)

This command will cause the drive positioner to position the heads over cylinder 0. A Return-to-Zero is automatically performed with each Head Load sequence, and whenever a Fault or Seek Error is detected.

### 5.3.4 Offset Command (15)

#### 5.3.4.1 Offset Command for RP Drives

The command causes the positioner to be offset by an incremental amount from the track centerline and/or the data strobe to be advanced or retarded by a small amount on the next Read operation. This operation offers additional data recovery attempts over that provided by the ECC capability. An Offset command uses the contents of RPOF to determine the offset. At the completion of the Offset operation, the ATA bit is set indicating that a Read command can be issued. The actual Offset is simulated during this time and instead occurs at the beginning of the following Read command.

The RPOF register (except for FMT16, ECI and HCI bits) is cleared and the drive will leave the Offset state by any one of the following methods:

1) Seek to another cylinder by means of a Seek command or Mid-Transfer Seek operation.

2) A Write command.

3) A Return-to Centerline command.

#### 5.3.4.2 Offset Command for RM Drives

This command causes the OFM bit in RMDS to be set. Subsequent reads will be done with the heads offset from the track centerline in the direction specified by RMOF bit 07. This operation offers additional data recovery attempts over that provided by the ECC capability when an ECC error is detected. If an ECC hard error occurs, two offset positions should be used. At the completion of the Offset command, the ATA bit is set, indicating that a Read command should be issued to the cylinder and track in order to recover data.

The OFM bit in RMDS will be cleared by any one of the following methods:

a. Seek to another cylinder by means of implied or Mid-Transfer Seek.
b. Write command.
c. Return-To-Centerline command.
d. Recalibrate command.
e. Read-In Preset command.

### 5.3.5 Return-to-Centerline Command (17)

#### 5.3.5.1 Return-to-Centerline Command for RP Drives

This command is used to clear bits <07:00> in RPOF, and set the ATA bit in RPDS. This command is simulated. The actual return-to-centerline occurs at the completion of the Read command.

#### 5.3.5.2 Return-to-Centerline Command for RM Drives

This command is used to clear the OFM bit, set the ATA bit in RMDS and clear bit 07 in RMOF.

### 5.3.6 Search Command (31)

The Search command causes the controller to first perform a Seek to the desired cylinder and then compare the sector counter with the desired sector in the RPDA/RMDA register. When they match, it sets the ATA bit, causing an Interrupt to the computer if IE in RPCS1/RMCS1 is set. An unsuccessful completion of a Search command occurs when a sector count and desired sector address match is not made during the interval of three Index pulses. In this case the OPI bit is set.

## 5.4 HOUSEKEEPING COMMANDS

Housekeeping commands are used to place drive logic into a known or initialized state and usually take only a few microseconds to execute. The Housekeeping commands are listed below.

### 5.4.1 No Op (01)

This command does not perform any operation, except to clear the ATA bit.

### 5.4.2 Drive Clear (11)

#### 5.4.2.1 Drive Clear for RP Drives

This command causes the following registers and conditions associated with the drive selected by the Unit Select bits in RPCS2 to be cleared: ATA, and ERR bits in RPDS; RPAS ATA bit; bits <15:09> and <07:00> in RPMR, bits <15:00> in RPER1, RPER2, RPER3, RPEC1, and RPEC2, and bits <07:00> in RPOF. Sets bit 08 of RPMR.

#### 5.4.2.2 Drive Clear for RM Drives

This command causes the following registers and conditions associated with the drive selected by the Unit Select bits in RMCS2 to be cleared: ATA, and ERR bits in RMDS; RMAS ATA bit; bits <15:04> and <02:00> in RMMR1; and bits <15:00> in RMER1, RMER2 and RMEC2. Sets bit 03 of RMMR1.

### 5.4.3 Release Command (13)

This command performs a Drive Clear function and releases the drive for use by the other port when in Dual Port mode of operation.

### 5.4.4 Read-In Preset (21)

#### 5.4.4.1 Read-In-Preset for RP Drives

This command sets the VV (volume valid) bit, clears the ATA bit in RPDS, clears the RPDC and RPDA registers, and clears the FMT16, HCI and ECI bits in the RPOF register.

#### 5.4.4.2 Read-In-Preset for RM Drives

This command sets the VV (volume valid) bit in RMDS, clears the RMDC, RMDA, and RMOF registers, and resets the OFM and ATA bits in RMDS.

### 5.4.5 Pack Acknowledge (23)

This command sets the VV bit for the selected drive. This command or a Read-In Preset command must be issued before any Data Transfer Or Positioning command can be given if the pack has gone off-line and then on-line (i.e., MOL change of state). It is primarily intended to avoid unknown pack changes.

## 5.5 OPTIONAL COMMANDS

With the exception of DMA Bandwidth Control (Op Code 25), the optional commands can be enabled only by writing a $177777_8$ into RMHR/RPCC. They remain enabled until either the end of a Data Transfer command, or the writing of some data other than $177777_8$ into RMHR/RPCC.

### 5.5.1 DMA Bandwidth Set (25)

This op code is enabled by setting DIP switch SW2-8 ON (closed). The function of this code is to extend the delay between bursts, so that the amount of bus bandwidth used by the controller during DMA is reduced. The standard delay is five usec. An additional delay (as caused by this op code) is in addition to the standard delay and any delay caused by DMA suspensions. The amount of additional delay is programmable on a drive-by-drive basis. The additional delay is programmed by the following methods:

1. Enable this op code by setting SW2-8 ON.
2. Load RPWC/RMWC with an unsigned positive number which represents the desired amount of additional delay.
3. Execute this op code.

Counts from zero to $65535_{10}$ are programmable, with each count adding 0.5 usec of delay and a count of zero representing a base of one usec.

### 5.5.2 DMA Burst Length (27)

This op code allows the user to specify the number of words (from one to 128) per DMA burst. To enable this code, load RPWC/RMWC with an unsigned positive number (representing the desired burst length minus one) into the low-order seven bits, then enable and execute this command. This command can be executed from any on-line drive, but it will affect all drives.

The default burst length at power-up is 16.

### 5.5.3 Suspended DMA Stall Count (35)

This op code allows the user to specify the amount of additional DMA suspend time to stall if eight or fewer DMA cycles occur between DMRs. To enable this code, load RPWC/RMWC with an unsigned positive number which represents the desired additional delay, then enable and execute this command. A count of one represents a base of one usec and each additional count adds another 0.5 usec. The count can be loaded from any on-line drive, but will affect all drives. The default count at power-up is 32 (17 usec).

### 5.5.4 Transparent ECC Correction (37)

When this feature is enabled, correctable ECC errors are fixed within the controller before the data is transferred to the memory on a Read, or Read Header and Data operation. Reading continues with the next sector if the data is ECC correctable. If the data is not ECC correctable, Data Transfers terminate with the bad sector and an uncorrectable read error is flagged in the normal manner. Upon completion of the Read, RPEC2/RMEC2 will contain the number of corrected ECC errors for the current command. It is preset to zero at the start of a Read command.

When disabled, Read Errors are handled in the normal manner and RPEC2/RMEC2 is not precleared. A cumulative corrected error count is maintained for each drive and may be read out of RPCC/RMHR by writing a $100023_8$ into RPCC/RMHR and then reading the register. It is cleared only upon power up.

This code can be set during a Write but it is not used during the Write unless the drive is an RM80 (see Automatic Skip-Sector Feature, paragraph 5.4.8). Because a separate flag exists in RPOF/RMOF for each drive, the op code enables this feature only for the drive selected in RPCS2/RMCS2. Bit 14 of RPOF/RMOF reflects the status of Transparent ECC mode. A one indicates that the function is enabled. It is cleared at the end of any Data Transfer and at the beginning of any Write Check, since the function is not supported during a Write Check.

### 5.5.5 Word Count Equals Sector Count (41)

When this feature is enabled, the contents of RPWC/RMWC contain the number of sectors to be transferred, rather than the number of words. It is valid for Read, or Read Header and Data operation and for Write or Write Header and Data operation. This command is not supported during a Write Check. Partial sector transfers cannot be done in this mode.

When disabled, RPWC/RMWC contains a word count. The count is negative in both cases.

Because a separate flag exists in RPOF/RMOF for each drive, the op code enables this command only for the drive selected in RPCS2/RMCS2. Bit 13 of RPOF/RMOF reflects the status of RPWC/RMWC equals sector count. A one indicates that the function is enabled. This bit is cleared at the end of any Data Transfer and at the start of any Write Check.

This command is primarily intended for users who wish to transfer very long bursts of data through single Q-Bus I/O ports.

### 5.5.6 Physical Read/Write/Write Check Header and Data

This heading comprises three op codes which are designed for users who wish to write their own custom formatter programs to take advantage of the track replacement feature offered on the RP04/05/06. The RP04/05/06 drives have two extra words in the header which the controller can utilize to specify an alternate track and cylinder in place of the current (assumed defective) track. Users who wish to take advantage of this mode should contact Emulex for details.

### 5.5.7 Format (77)

#### 5.5.7.1 Format for RP Drives

This command executes a Return-to-Zero; clears RPDC, RPDA; sets FMT16 in RPOF; and formats the entire pack in standard format. Each sector has the FMT16 bit set in header word 1, all zeros in header words 3 and 4, and an all 0's data field. RPDC will be set to the last cylinder number plus one at completion, and the LST bit in RPDS will be set.

#### 5.5.7.2 Format for RM Drives

This command executes a Return-to-Zero; clears RMDC, RMDA; sets FMT16 in RMOF; and formats the entire pack in standard format. Each sector has bits <15:14> and the FMT16 bit set in header word 1 and an all 0's data field. RMDC will be set to the last cylinder number plus one at completion, and the LST bit in RMDS will be set.

### 5.5.8 Automatic Skip-Sector Feature

This feature enables drives running as RM80 units to automatically execute the Skip-Sector function which is standard in the RM80. The firmware will set the Skip-Sector Error inhibit bit in RMOF if either Transparent ECC mode (op code 37) or Word Count Equals Sector Count mode (op code 41) is enabled and a Skip-Sector Error is encountered. In this case the firmware will also bump the number of usable sectors per track by one (to gain access to the skip-sector), bump RMDA by one and continue the Data Transfer with the next sector.

As is the case in the normal mode, the Skip-Sector enable is reset if the end of the track is reached. Therefore, multiple skip errors can occur and all will be skipped. This feature functions for Read Data and Write Data commands only.

To ensure proper operation of this feature, the Skip-Sector error inhibit bit in RMOF must be reset immediately prior to the execution of a Read or Write. The firmware will ignore all other header errors except a CRC error on the sector being skipped, and will ignore only Skip-Sector errors on all remaining sectors of the track. This is in compliance with standard DEC RM80 formatters.

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# APPENDIX A

# SC03/BX CONFIGURATION AND OPTION SELECTION

## A.1 INTRODUCTION

To allow the SC03/BX user maximum flexibility in disk drive selection, the SC03/BX supports a wide variety of disk types. This appendix provides the switch settings which make possible this flexibility.

## A.2 CONTROLLER CONFIGURATION

The SC03/BX unit is capable of supporting a wide variety of disk drives. Switches SW3-6 through SW3-1 select the various configurations that are supported, and a list of these drive types and capacities may be found in Table A-1. Table A-2 lists the proper switch settings for each of the various configurations.

### A.2.1 Physical vs Logical Disk Numbering

A primary feature of the SC03/BX is its ability to emulate four DEC disk subsystems using two physical disk drives. This is accomplished by mapping two logical disk subsystems onto one disk drive which contains twice as much capacity as the standard DEC subsystem. In the event of this usage the mapping of logical units onto physical units is as follows:

| Physical Unit Number | Logical Unit Numbers |
|---|---|
| 0 | 0 and 2 |
| 1 | 1 and 3 |

The physical/logical assignments for specific disk configurations can be found by comparing the Physical drive column to the Logical drive column in Table A-2.

The SC03/BX supports both RM and RP type drives. The RP types drives have 22 sectors, and the RM type drives have 32 sectors. With the support of both types, the SC03 can more effectively utilize the amount of sectors on some drives.

#### A.2.1.2 Unit Number Assignment

The disk drives need to be assigned a distinct unit number. This number may be determined after the configuration to use has been

decided upon. The unit number for each drive must correspond to the physical unit number found in Table A-2. Thus, for configuration 04, unit 0 would be an 823 cylinder, 5 track drive; unit 1 would be an 823 cylinder, 5 track drive; unit 2 would not be present; and unit 3 would be an 823 cylinder, 5 track drive.

### A.2.3 Sectoring CDC Drives and the 2351A Fujitsu

To allow CDC drives and the 2351A Fujitsu to function properly with the SC03/BX, some alterations must be made to the sector select switch settings found in their manuals.

To configure CDC drives for 33 sectors, switch 0 must be CLOSED, with all other switches set as per the CDC manual. To configure the 2351A Fujitsu for 48 sectors the jumpers at location BC7 must be set such that bit one is jumpered 2-3 (rather than 3-4), bit 2 is jumpered as 6-7 (rather than 5-6), and all other jumpers are as per the Fujitsu manual.

### A.2.4 Drive Configuration Selection

The SC03/BX emulates five different DEC disk subsystems, the RM02, RM03, RM05, the RM80 and the RP06. The RM02 and RM03 have an unformatted capacity of 80 Mb. The RM05 has an unformatted capacity of 300 Mb, and the RM80 has an unformatted capacity of 160 Mb. The RP06 has an unformatted capacity of 200 Mb.

There are essentially three different types of drive configurations. With the first type, each emulated DEC drive exists on one physical drive. In the second type, two emulated drives are mapped onto one physical drive. The third type is a combination of the first two.

To find the configuration switch settings which are compatible with your system use the following procedure:

1. Locate your drive type and size in Table A-1. Note the KEY assigned to each type of drive you intend to use.

2. Scan down the KEY column of Table A-2 until you find your drive's number. Check the corresponding emulation in the Logical Drive column. If the emulation is not one that you require, continue to scan the KEY column in search of the required emulation.

3. After finding a suitable match for Drive 0, check the drive key and type for Drives 1, 2 and 3 for that configuration row. It is not necessary to use all drive ports.

4. When you have found a configuration which is entirely suitable, set the configuration switches as indicated.

TABLE A-1
DRIVES SUPPORTED

| Mfg. | Model | Key | Physical Cyl | Trk | Sec | Configurations |
|---|---|---|---|---|---|---|
| Ampex | 330 | 1024-16 | 1024 | 16 | 32 | 12,14 |
| Ampex | 330 | 1024-16 | 1024 | 16 | 33 | 09 |
| Ampex | 9380 | 823-05 | 823 | 5 | 32 | 00,04,05,15,16,18,19,1B |
| Ampex | 93160 | 1645-05 | 1645 | 5 | 32 | 10,11 |
| APS | 4830# | 823-10 | 823 | 10 | 64 | 04,12-15,20-23,32,33,43 |
| CDC | 9448-96 | 823-06 | 823 | 6 | 32 | 0A,0B,0C |
| CDC | 9457 | 624-04 | 624 | 4 | 32 | 27 |
| CDC | 9457 | 624-04 | 624 | 4 | 32 | 29 |
| CDC | 9715-340 | 711-24 | 711 | 24 | 32 | 2E,2F |
| CDC | 9730-80 | 823-05 | 823 | 5 | 32 | 00,04,05,15,16,18,19,1B |
| CDC | 9730-160 | 823-10 | 823 | 10 | 32 | 02-05,14,17-19,30,31 |
| CDC | 9760 | 411-05 | 411 | 5 | 32 | 0D |
| CDC | 9762 | 823-05 | 823 | 5 | 32 | 00,04,05,15,16,18,19,1B, 2A,36,37,3A,3B |
| CDC | 9766 | 823-19 | 823 | 19 | 32 | 01,07,08,0B,0C,15,1B,2B 2C,2F,31,33-35,38,39 |
| CDC | 9771 | 1024-16 | 1024 | 16 | 32 | 33 |
| CDC | 9771 | 1024-16A | 1024 | 16 | 64 | 34-37 |
| CDC | 9771 | 1024-16B | 1024 | 16 | 84 | 38-3B |
| CDC | 9775 | 842-40 | 842 | 40 | 32 | 06-08,13 |
| Century | T82RM | 823-05 | 823 | 5 | 32 | 00,04,05,15,16,18, 19,1B |
| Century | T302RM | 823-19 | 823 | 19 | 32 | 01,07,08,0B,0C,15, 1B,28 |
| Fujitsu | 2280 | 823-05 | 823 | 5 | 32 | 00,04,05,15,16,18, 19,1B |
| Fujitsu | 2284 | 823-10 | 823 | 10 | 32 | 02-05,14,17-19,30 |
| Fujitsu | 2294 | 1024-16 | 1024 | 16 | 32 | 12,14 |
| Fujitsu | 2294 | 1024-16 | 1024 | 16 | 33 | 09 |
| Fujitsu | 2312 | 589-07 | 589 | 07 | 33 | 0E,1A,2A,30,31 |
| Fujitsu | 2322 | 823-10A | 823 | 10 | 32 | 2-5,14,17-19,30,31 |
| Fujitsu | 2351A | 842-20 | 842 | 20 | 44 | 22-26 |
| Fujitsu | 2351A | 842-20 | 842 | 20 | 48 | 20*,21* |
| Memorex | 677 | 815-19 | 819 | 19 | 22 | 26 |
| Memorex | 677-30 | 823-19 | 823 | 19 | 32 | 01,07,08,0B,0C,15,1B,2B, 2C,2F |
| NEC | 2257 | 1024-08 | 1024 | 08 | 32 | 2D |
| NEC | D2351 | 760-19 | 760 | 19 | 60 | 32 |
| Priam | 3350 | 561-03 | 561 | 3 | 32 | 1F |
| STC | 8775 | 1124-30 | 1124 | 30 | 33 | 1C,1D |
| Tecstor | 160 | 700-12 | 700 | 12 | 32 | 1E |

#Set sector size to 630 bytes/sector (switch count equals 629) and enable the track length compatibility switch located on the SLOG board. This makes the drive look like a CDC 9766.

*These configurations must have option switch SW1-2 (sector interleave) ON.

TABLE A-2
DRIVE CONFIGURATIONS

| CONF. NO. | SW3- 6 | 5 | 4 | 3 | 2 | 1 | PHYSICAL KEY | Unit | LOGICAL Unit(s) = Dr Type | Rev |
|---|---|---|---|---|---|---|---|---|---|---|
| 00 | O | O | O | O | O | O | 823-05 | 0 | 0 = RM03 | A |
| | | | | | | | 823-05 | 1 | 1 = RM03 | A |
| 01 | O | O | O | O | O | C | 823-19 | 0 | 0 = RM05 | A |
| | | | | | | | 823-19 | 1 | 1 = RM05 | A |
| 02 | O | O | O | O | C | O | 823-10 | 0 | 0,2 = RM03/RM03 | A |
| | | | | | | | 823-10 | 1 | 1,3 = RM03/RM03 | A |
| 03 | O | O | O | O | C | C | 823-10 | 0 | 0 = RM80 | A |
| | | | | | | | 823-10 | 1 | 1 = RM80 | A |
| 04 | O | O | O | C | O | O | 823-05 | 0 | 0 = RM03 | A |
| | | | | | | | 823-10 | 1 | 1,3 = RM03/RM03 | A |
| 05 | O | O | O | C | O | C | 823-10 | 0 | 0,2 = RM03/RM03 | A |
| | | | | | | | 823-05 | 1 | 1 = RM03 | A |
| 06 | O | O | O | C | C | O | 842-40 | 0 | 0,2 = RM05/RM05 | A |
| | | | | | | | 842-40 | 1 | 1,3 = RM05/RM05 | A |
| 07 | O | O | O | C | C | C | 823-19 | 0 | 0 = RM05 | A |
| | | | | | | | 842-40 | 1 | 1,3 = RM05/RM05 | A |
| 08 | O | O | C | O | O | O | 842-40 | 0 | 0,2 = RM05/RM05 | A |
| | | | | | | | 823-19 | 1 | 1 = RM05 | A |
| 09 | O | O | C | O | O | C | 1024-16 | 0 | 0 = RM05 | A |
| | | | | | | | 1024-16 | 1 | 1 = RM05 | A |
| 0A | O | O | C | O | C | O | 823-06 | 0 | 0,2 = RM03/RM02* | A |
| | | | | | | | 823-06 | 1 | 1,3 = RM03/RM02* | A |
| 0B | O | O | C | O | C | C | 823-06 | 0 | 0,2 = RM03/RM02* | A |
| | | | | | | | 823-19 | 1 | 1 = RM05 | A |
| 0C | O | O | C | C | O | O | 823-19 | 0 | 0 = RM05 | A |
| | | | | | | | 823-06 | 1 | 1,3 = RM03/RM02 | A |
| 0D | O | O | C | C | O | C | 411-05 | 0 | 0 = RM03* | A |
| | | | | | | | 411-05 | 1 | 1 = RM03* | A |
| 0E | O | O | C | C | C | O | 589-07 | 0 | 0 = RM03 | A |
| | | | | | | | 589-07 | 1 | 1 = RM03 | A |
| 0F | O | O | C | C | C | C | 823-10 | 0 | 0 = RM03* | A |
| | | | | | | | 823-10 | 1 | 1 = RM03* | A |
| 10 | O | C | O | O | O | O | 1645-05 | 0 | 0 = RM03* | A |
| | | | | | | | 1645-05 | 1 | 1 = RM03* | A |
| 11 | O | C | O | O | O | C | 1645-05 | 0 | 0,2 = RM03/RM03 | A |
| | | | | | | | 1645-05 | 1 | 1,3 = RM03/RM03 | A |
| 12 | O | C | O | O | C | O | 1024-16 | 0 | 0 = RM05* | A |
| | | | | | | | 1024-16 | 1 | 1 = RM05* | A |
| 13 | O | C | O | O | C | C | 842-40 | 0 | 0 = RM05* | A |
| | | | | | | | 842-40 | 1 | 1 = RM05* | A |
| 14 | O | C | O | C | O | O | 823-10 | 0 | 0 = RM03/RM03 | A |
| | | | | | | | 1024-16 | 1 | 1 = RM05* | A |
| 15 | O | C | O | C | O | C | 823-05 | 0 | 0 = RM03 | A |
| | | | | | | | 823-19 | 1 | 1 = RM05 | A |
| 16 | O | C | O | C | C | O | 823-05 | 0 | 0 = RM02 | A |
| | | | | | | | 823-05 | 1 | 1 = RM02 | A |

TABLE A-2 (con't)
DRIVE CONFIGURATIONS

| CONF. NO. | SW3- 6 | 5 | 4 | 3 | 2 | 1 | PHYSICAL KEY | Unit | LOGICAL Unit(s) = Dr Type | Rev |
|---|---|---|---|---|---|---|---|---|---|---|
| 17 | O | C | O | C | C | C | 823-10 | 0 | 0,2 = RM02/RM02 | A |
| | | | | | | | 823-10 | 1 | 1,3 = RM02/RM02 | A |
| 18 | O | C | C | O | O | O | 823-05 | 0 | 0 = RM02 | A |
| | | | | | | | 823-10 | 1 | 1,3 = RM02/RM02 | A |
| 19 | O | C | C | O | O | C | 823-10 | 0 | 0,2 = RM02/RM02 | A |
| | | | | | | | 823-05 | 1 | 1 = RM02 | A |
| 1A | O | C | C | O | C | O | 589-07 | 0 | 0 = RM02 | A |
| | | | | | | | 589-07 | 1 | 1 = RM02 | A |
| 1B | O | C | C | O | C | C | 823-05 | 0 | 0 = RM02 | A |
| | | | | | | | 823-19 | 1 | 1 = RM05 | A |
| 1C | O | C | C | C | O | O | 1124-30 | 0 | 0,2 = RM05/RM05 | A |
| | | | | | | | 1124-30 | 1 | 1,3 = RM05/RM05 | A |
| 1D | O | C | C | C | O | C | 1124-30 | 0 | 0,2 = RM05/RM05 | A |
| | | | | | | | 823-19 | 1 | 1 = RM05 | A |
| 1E | O | C | C | C | C | O | 700-12 | 0 | 0 = RM02* | A |
| | | | | | | | 700-12 | 1 | 1 = RM02* | A |
| 1F | O | C | C | C | C | C | 561-03 | 0 | 0 = RM03* | A |
| | | | | | | | 561-03 | 1 | 1 = RM03* | A |
| 20# | C | O | O | O | O | O | 842-20 | 0 | 0 = RM80* | A |
| | | | | | | | 842-20 | 1 | 1 = RM80* | A |
| 21# | C | O | O | O | O | C | 842-20 | 0 | 0 = RM02* | A |
| | | | | | | | 842-20 | 1 | 1 = RM02* | A |
| 22 | C | O | O | O | C | O | 842-20 | 0 | 0,2 = RP06/RP06 | A |
| | | | | | | | 842-20 | 1 | 1,3 = RP06/RP06 | A |
| 23 | C | O | O | O | C | C | 842-20 | 0 | 0 = RP06* | A |
| | | | | | | | 842-20 | 1 | 1 = RP06* | A |
| 24 | C | O | O | C | O | O | 823-10 | 0 | 0,2 = RM03/RM03 | A |
| | | | | | | | 842-20 | 1 | 1 = RP06/RP06 | A |
| 25 | C | O | O | C | O | C | 823-10 | 0 | 0 = RM80 | A |
| | | | | | | | 842-20 | 1 | 1,3 = RP06/RP06 | A |
| 26 | C | O | O | C | C | O | 842-20 | 0 | 0,2 = RP06/RP06 | A |
| | | | | | | | 815-19 | 1 | 1 = RP06 | A |
| 27 | C | O | O | C | C | C | 624-04 | 0 | 0,2 = RM02* | B |
| | | | | | | | 624-04 | 1 | 1,3 = RM02* | B |
| 28 | C | O | C | O | O | O | 823-19 | 0 | 0 = RP06* | B |
| | | | | | | | 823-19 | 1 | 1 = RP06* | B |
| 29 | C | O | C | O | O | C | 624-04 | 0 | 0,2 = RM02* | C |
| | | | | | | | 624-04 | 1 | 1,3 = RM02* | C |
| 2A | C | O | C | O | C | O | 589-07 | 0 | 0 = RM02 | D |
| | | | | | | | 823-05 | 1 | 1 = RM02 | D |
| 2B | C | O | C | O | C | C | 823-19 | 0 | 0 = RM05 | D |
| | | | | | | | 1024-16 | 1 | 1 = RM05 | D |
| 2C | C | O | C | C | O | O | 1024-16 | 0 | 0 = RM05 | D |
| | | | | | | | 823-19 | 1 | 1 = RM05 | D |
| 2D | C | O | C | C | O | C | 1024-08 | 0 | 0 = RM02* | D |
| | | | | | | | 1024-08 | 1 | 1 = RM02* | D |

TABLE A-2 (con't)
DRIVE CONFIGURATIONS

| CONF. NO. | SW3- 6 | 5 | 4 | 3 | 2 | 1 | PHYSICAL KEY | Unit | LOGICAL Unit(s) = Dr Type | Rev |
|---|---|---|---|---|---|---|---|---|---|---|
| 2E | C | O | C | C | C | O | 711-24 | 0 | 0 = RM05 | D |
| | | | | | | | 711-24 | 1 | 1 = RM05 | D |
| 2F | C | O | C | C | C | C | 711-24 | 0 | 0 = RM05 | D |
| | | | | | | | 823-19 | 1 | 1 = RM05 | D |
| 30 | C | C | O | O | O | O | 589-07 | 0 | 0 = RM03 | F |
| | | | | | | | 823-10 | 1 | 1,3 = RM03/RM03 | F |
| 31 | C | C | O | O | O | C | 823-10 | 0 | 0,2 = RM03/RM03 | F |
| | | | | | | | 823-19 | 1 | 1 = RM05 | F |
| 32 | C | C | O | O | C | O | 760-19 | 0 | 0,2 = RP06/RP06* | F |
| | | | | | | | 760-19 | 1 | 1,3 = RP06/RP06* | F |
| 33 | C | C | O | O | C | C | 1024-16 | 0 | 0,2 = RP06/RP06* | G |
| | | | | | | | 823-19 | 1 | 1 = RM05 | G |
| 34 | C | C | O | C | O | O | 823-19 | 0 | 0 = RM05 | H |
| | | | | | | | 1024-16A | 1 | 1,3 = RM05/RM05 | H |
| 35 | C | C | O | C | O | C | 1024-16A | 0 | 0,2 = RM05/RM05 | H |
| | | | | | | | 823-19 | 1 | 1 = RM05 | H |
| 36 | C | C | O | C | C | O | 1024-16A | 0 | 0,2 = RM05/RM05 | H |
| | | | | | | | 823-05 | 1 | 1 = RM03 | H |
| 37 | C | C | O | C | C | C | 823-05 | 0 | 0 = RM05 | H |
| | | | | | | | 1024-16A | 1 | 1,3 = RM05/RM05 | H |
| 38 | C | C | C | O | O | O | 823-19 | 0 | 0 = RM05 | H |
| | | | | | | | 1024-16B | 1 | 1,3 = RM05/RM05 | H |
| 39 | C | C | C | O | O | C | 1024-16B | 0 | 0,2 = RM05/RM05 | H |
| | | | | | | | 823-19 | 1 | 1 = RM05 | H |
| 3A | C | C | C | O | C | O | 823-05 | 0 | 0 = RM03 | H |
| | | | | | | | 1024-16B | 1 | 1,3 = RM05/RM05 | H |
| 3B | C | C | C | O | C | C | 1024-16B | 0 | 0,2 = RM05/RM05 | H |
| | | | | | | | 823-06 | 1 | 1 = RM03 | H |

*These configurations have a non-standard cylinder and/or track number and are not supported by DEC diagnostics or DEC operating systems.

#These configurations must have option switch SW1-2 (sector interleave) ON.

C = Closed (ON)  O = Open (OFF)

TABLE A-3
NON-STANDARD DRIVE SIZE TABLE

| Config. | Description |
|---|---|
| 0A | RM03 is 164 cylinders mapped on a 9448 cartridge |
| 0B | RM03 is 164 cylinders mapped on a 9448 cartridge |
| 0C | RM03 is 164 cylinders mapped on a 9448 cartridge |
| 0D | RM03 is a 5 track, 411 cylinder drive |
| 0F | RM03 is a 10 track, 823 cylinder drive |
| 10 | RM03 is a 5 track, 1645 cylinder drive |
| 12 | RM05 is a 16 track, 1024 cylinder drive |
| 13 | RM05 is a 40 track, 842 cylinder drive |
| 14 | RM05 is a 16 track, 1024 cylinder drive |
| 1E | RM02 is a 12 track, 700 cylinder drive |
| 1F | RM03 is a 3 track, 561 cylinder drive |
| 20 | RM80 is a 20 track, 842 cylinder, 48 sector drive |
| 21 | RM02 is a 20 track, 842 cylinder, 48 sector drive |
| 23 | RP06 is 1772 cylinders mapped on a 44 sector drive |
| 27 | RM02 is a 5 track, 249 cylinder, 32 sector drive |
| 28 | RP06 is a 19 track, 823 cylinder, 32 sector drive |
| 29 | RM02 is a 2 track, 624 cylinder, 32 sector drive |
| 2D | RM02 is a 5 track, 1638 cylinder, 32 sector drive |
| 32 | RP06 is a 19 track, 760 cylinder, 30 sector drive |
| 33 | RP06 is a 16 track, 1024 cylinder, 40 sector drive |
| 38 | RM05 is a 16 track, 1024 cylinder, 42 sector drive |
| 39 | RM05 is a 16 track, 1024 cylinder, 42 sector drive |
| 3A | RM05 is a 16 track, 1024 cylinder, 42 sector drive |
| 3B | RM05 is a 16 track, 1024 cylinder, 42 sector drive |

## A.3 USER SELECTABLE OPTIONS

Several other options including the register starting address for the SC03/BX can be user selected. The factory switch settings are listed in Table A-3. The functions of the switches that select those options are defined in Tables A-4, A-5 and A-6, below.

TABLE A-4
SC03 FACTORY SWITCH SETTINGS

| Switch | Setting | Switch | Setting | Switch | Setting |
|---|---|---|---|---|---|
| SW1-1 | OFF | SW2-1 | OFF | SW3-1 | OFF |
| SW1-2 | OFF | SW2-2 | OFF | SW3-2 | OFF |
| SW1-3 | OFF | SW2-3 | OFF | SW3-3 | OFF |
| SW1-4 | OFF | SW2-4 | OFF | SW3-4 | OFF |
| | | SW2-5 | OFF | SW3-5 | OFF |
| | | SW2-6 | OFF | SW3-6 | OFF |
| | | SW2-7 | OFF | SW3-7 | OFF |
| | | SW2-8 | OFF | SW3-8 | ON |
| | | SW2-9 | ON | SW3-9 | ON |
| | | SW2-10 | ON | SW3-10 | ON |

The factory switch settings enable a standard register address of 776700 and a standard interrupt vector address of 254.

OFF = Open, ON = Closed

TABLE A-5
OPTION SWITCH SW1 SETTINGS

| Option Sw | Open | Closed | Function |
|---|---|---|---|
| SW1-1 | Run | Halt-Reset | Controller Run/Halt-Reset |
| SW1-2 | 1:1 | 2:1 | Sector interleave[1] |
| SW1-3 | Disable | Enable | 2 RP06s mapped on 19-head drives[3] |
| SW1-4 | | | Interrupt vector select #32 |

[1]Requires an even number of sectors per track. Will fail some subtests in Functional diagnostics if enabled.

[2]See paragraph 3.4.2.

[3]Requires Rev. D and above firmware. See paragraph 3.4.4.13.

Closed = ON, Open = OFF

TABLE A-6
OPTION SWITCH SW2 SETTINGS

| Option Sw | Open | Closed | Function |
|---|---|---|---|
| SW2-1 | | | Interrupt vector select #1[2] |
| SW2-2 | | | Interrupt vector select #2[2] |
| SW2-3 | RH11 | RH70 | RH11 vs RH70 select |
| SW2-4 | Disable | Enable | Swap logical units 0 and 1 with 2 and 3 |
| SW2-5 | Disable | Enable | Replacement track mode (RP units only)[3,4] |
| SW2-6 | Disable | Enable | Dual port mode |
| SW2-7 | Disable | Enable | Dual access mode |
| SW2-8 | Disable | Enable | DMA bandwidth control[4,5] |
| SW2-9 | ENABLE | DISABLE | A Cable busy signal[6] |
| SW2-10 | 2K | 4K | PROM size select[7] |

[1]All unused switches MUST BE OFF.

[2]See paragraph 3.4.2.

[3]Requires custom user formatter. Will fail DEC formatter.

[4]Will fail some subtests in Functional diagnostics if enabled.

[5]See paragraph 5.5.1.

[6]See paragraph 2.6.8.

[7]Must be closed.

Closed = ON, Open = OFF

TABLE A-7
OPTION SWITCH SW3 SETTINGS

| Option Sw | Open | Closed | Function |
|---|---|---|---|
| SW3-1 | | | Drive configuration[1] |
| SW3-2 | | | Drive configuration[1] |
| SW3-3 | | | Drive configuration[1] |
| SW3-4 | | | Drive configuration[1] |
| SW3-5 | | | Drive configuration[1] |
| SW3-6 | | | Drive configuration[1] |
| SW3-7 | | 776300 | Controller address (Alternate) |
| SW3-8 | | 776700 | Controller address (Standard) |
| SW3-9 | Enable | Disable | Bootstrap PROMs |
| SW3-10 | Enable | Disable | Line time clock |

NOTE: SW3-7 and SW3-8 must not both be closed at the same time.

[1]See Table A-2.

Closed = ON, Open = OFF

# Appendix B
# Modifications for DEC Diagnostics

The SC03/BX controller executes all DEC RM02/RM03 diagnostics. Several of the lower level diagnostics require patching to by-pass unsupported maintenance mode functions.

Emulex provides diagnostics which are self-sizing and need no patching. They are listed at the end of this appendix.

The following describes how to patch the DEC diagnostics for non-standard disk sizes. All locations and contents are in octal.

## B.1 ZRMA-C0 FORMATTER (August 1977)

### B.1.1 Modifications to Correct Programming Errors

| Location | From | To |
|---|---|---|
| 12632 | 10011 | 1 |
| 23630 | 13746 | 12746 |
| 27154 | 1750 | 1503 |
| 27512 | 10164 | 110164 |
| 31602 | 10164 | 110164 |
| 32772-32774 | 5702, 1426 | 4737, 34676 |
| 32776-33000 | 4737, 34676 | 5702, 1424 |

### B.1.2 Modifications For Number of Cylinders and Tracks

| Location | From | To |
|---|---|---|
| 30044 | 4037 | 406 |
| 11260-11262 | 112737, 4 | 113737, 31472 |
| 11266-11270 | 12737, 1466 | 13737, 31470 |
| 11510-11512 | 22737, 151466 | 23737, 31466 |
| 11520-11522 | 22737, 2000 | 23737, 31464 |
| 12530-12532 | 12702, 1466 | 13702, 31470 |
| 12560-12562 | 12737, 5 | 13737, 5660 |
| 12612-12614 | 62737, 5 | 63737, 5660 |
| 15200-15202 | 22737, 1466 | 23737, 31470 |
| 15210-15212 | 122737, 4 | 123737, 31472 |
| 15402-15404 | 12737, 1466 | 12737, 31470 |
| 15410-15412 | 112737, 4 | 113737, 31472 |
| 16410-16412 | 22737, 4 | 23737, 31472 |
| 16430-16432 | 22737, 1466 | 23737, 31470 |
| 16440-16442 | 122737, 4 | 123737, 31472 |
| 16502-16504 | 22737, 1467 | 23737, 5652 |
| 20070-20072 | 12737, 1466 | 13737, 31470 |
| 20076-20100 | 12737, 4 | 13737, 31472 |
| 27176-27200 | 22705, 20024 | 122705, 24 |
| 27204-27206 | 22705, 24024 | 122705, 27 |
| 27220-27222 | 22705, 20025 | 122705, 25 |

Modifications For Number of Cylinders and Tracks (con't)

| Location | From | To |
|---|---|---|
| 27226-27230 | 22705, 24025 | 122705, 25 |
| 10734-10740 | 12737, 1466, 1320 | 104412, 13703, 26644 |
| 10742-10746 | 132762, 3, 26526 | 13702, 1220, 10263 |
| 10750-10752 | 1003, 12737 | 10, 4737 |
| 10754-10756 | 1466, 1320 | 31320, 104413 |

The following subroutine must be inserted where indicated. It replaces a rotational position sensing routine that the formatter does not need since it only formats one drive at a time. The contents of the existing routine are not shown.

Locations: 31320-31452

Contents: 62703, 36, 12713, 100027, 11304, 12713, 100030, 11305, 12713, 100036, 10437, 1320, 10537, 1324, 12703, 31464, 105023, 110523, 10413, 52723, 150000, 10423, 10523, 5204, 5205, 10437, 5652, 10537, 5660, 10437, 5666, 10537, 5674, 10437, 5704, 10537, 5712, 10437, 5730, 10537, 5736, 10437, 5754, 10537, 5762, 207.

### B.1.3 Formatter Operation

The Formatter program writes either all zeros, all ones or a worst case pattern in every sector, and at the same time it writes the headers. It does this by writing the complete track at one time. The program will print out five errors while attempting to read the Bad Sector File on the last track of the disk if the pack has not been previously formatted. After the errors it will continue in a normal manner and will put a Bad Sector File on the pack. The program will ask for a pack I.D. if none already exists in the Bad Sector File.

The program can be loaded by XXDP. The normal starting location is $200_8$, but should be started at $204_8$ initially if it is desired to change the Q-Bus address or vector.

The program will type:

MODE (C OR F)

C should be typed for check and F for format, followed by a carriage return. Format mode does one pass, check mode does three passes with a rotating worst-case data pattern.

The program will then ask:

OPERATE IN 32 SECTOR (16 Bit) MODE (Y or N)

Y followed by carriage return should be typed.

The program will then ask for a drive:

DRIVE:

Enter the number (0-7) of the drive to be formatted followed by a carriage return.

The program will ask for address limits:

ENTER ADDRESS LIMITS:

Min and max sector, track and cylinder numbers may be entered in decimal followed by a carriage return. Just a carriage return will use the normal values. A period followed by a carriage return will terminate this phase.

The program will then ask for data pattern to which a carriage return should be typed to select worst-case. No pattern is asked for in Check mode.

The program will then type:

STARTING FORMAT (CHECK) ON DRIVE N

The program will list all errors and will indicate when it is done. The Bad Sector File is written just prior to the done message. During the format, typing a Control-O will display the current cylinder and track being formatted.

## B.2 ZRMB-B0 PERFORMANCE EXERCISER (August 1977)

### B.2.1 Modifications to Correct Programming Errors

| Location | From | To |
|---|---|---|
| 11134-11136 | 400, 46116 | 100000, 46144 |
| 32144 13746 | 12746 | |
| 35130 1750 | 1503 | |
| 35466 10164 | 110164 | |
| 37556 10164 | 110164 | |
| 41036-41040 | 5702, 1426 | 4737, 34676 |
| 41042-41044 | 4737, 34676 | 5702, 1424 |

All of the above items are unidentified program bugs.

### B.2.2 Modifications For Number of Cylinders and Tracks

| Location | From | To |
|---|---|---|
| 4440 | 57512 | 60410 |
| 4472 | 57512 | 60410 |
| 6364-6366 | 22760, 1465 | 26060, 106 |
| 13534-13540 | 123727, 1415, 5 | 240, 4737, 60304 |
| 13554-13560 | 23727, 1412, 151466 | 240, 4737, 60230 |
| 16654-16656 | 62705, 5 | 66005, 112 |
| 16672-16676 | 20527, 4, 101402 | 26005, 112, 3002 |
| 16700-16702 | 162705, 5 | 16005, 112 |
| 22614-22616 | 112766, 4 | 116066, 112 |
| 25442-25446 | 10004, 62704, 2 | 10046, 4737, 60064 |
| 25664 | 12737 | 402 |
| 25762-25764 | 16403, 55252 | 4737, 60206 |
| 26214-26220 | 12737, 1466, 40674 | 240, 4737, 60262 |
| 26222-26226 | 112737, 4, 40673 | 240, 4737, 60326 |
| 35152-35154 | 22705, 20024 | 122705, 24 |
| 35160-35162 | 22705, 24024 | 122705, 27 |
| 35174-35176 | 22705, 20025 | 122705, 25 |
| 35202-35204 | 22705, 24025 | 122705, 25 |

The following subroutine must be added to the end of the program at the indicated locations.

Locations: 60064-60204

Contents: 10146, 111001, 13704, 34620, 4037, 35050, 401, 403, 105761, 34512, 1375, 105761, 34472, 3424, 62704, 36, 6301, 6301, 62701, 60350, 12714, 100027, 11421, 11400, 5300, 10037, 1446, 12714, 100030, 11421, 11437, 1444, 12714, 100036, 12601, 16604, 2, 12600, 62704, 2, 200.

Locations: 60206-60346

Contents: 16403, 55252, 13763, 1444, 16, 13763, 1444, 24, 207, 5046, 111016, 6316, 6316, 67716, 60350, 13646, 52716, 150000, 5216, 22637, 1412, 207, 5046, 111016, 6316, 6316, 62716, 60350, 13637, 46074, 207, 5046, 111016, 6316, 6316, 62716, 60352, 123637, 1415, 207, 5046, 111016, 6316, 6316, 62716, 60352, 113637, 46073, 207.

Those users running on drives with more than 80 MB capacity will require the following patches. The Performance Exerciser limits the number of allowable bad sectors on any drive to 16, even though the Bad Sector File can handle 126. The following patches allow the program to run with 126 bad sectors or less. The first two patches move the base address of the buffer. These locations have already been patched, and the "from" column reflects those patches.

| Location | From | To |
|---|---|---|
| 4440 | 60410 | 70410 |
| 4472 | 60410 | 70410 |
| 17202 | 20 | 176 |
| 17206 | 62702 | 16002 |
| 20274 | 12701 | 16001 |
| 20300 | 60001 | 240 |
| 20304 | 20 | 176 |
| 25504 | 14 | 22 |
| 25510 | 162 | 154 |
| 25716 | 122 | 126 |
| 26166 | 62701 | 16001 |
| 26174 | 40 | 400 |
| 26344 | 62701 | 16001 |
| 26352 | 40 | 400 |
| 43146 | 0 | 60410 |
| 43452 | 0 | 61410 |
| 43756 | 0 | 62410 |
| 44262 | 0 | 63410 |
| 44566 | 0 | 64410 |
| 45072 | 0 | 65410 |
| 45376 | 0 | 66410 |
| 45702 | 0 | 67410 |

### B.2.3 Performance Exerciser Operation

This program has the ability to do various operations on one to four drives. The Formatter must be run before this program can be run so as to provide proper patterns and a Bad Sector File.

A carriage return can be given to the requests for date and operator I.D. The program will then type:

ENTER PARAMETERS:

A carriage return should be given since it is normally not necessary to change the program parameters and the full instructions would be needed. After listing the availability of the eight drives the program is started with those drives that are on-line if started at location 200. Starting at 204 requires further keyboard commands as follows:

The program can be commanded from the keyboard by typing Control-C. It will then respond with ENTER COMMANDS. The command letter followed by the drive number (or the letter A for all drives) and a carriage return should be typed. The commands are:

T - Do normal random testing on drives.

D - Deassign a drive from testing.

W - Write data pattern starting at min address and proceeding to max address. Headers and Bad Spot File are not written.

R - Read data starting at min address and proceeding to max address.

WT - Same as write command, but then does test command.

S - Summary of current status.

Most of the commands will ask for min and max address limits. Sector, track and cylinder numbers may be entered in decimal, or a carriage return will give normal values. A period followed by a carriage return will terminate the requests.

The program will then ask for a Drive I.D. A 0-6 character I.D. followed by a carriage return should be entered. The I.D. is used during the status summary printouts that occur every 5 minutes.

Once the I.D. has been entered the program begins execution.

## B.3 ZRMC-B0 FUNCTIONAL TEST - PART 1 (August 1977)

### B.3.1 Modifications For Correct Operation

| Loc. | From | To |
|---|---|---|
| 25024, 25026 | 4737, 43216 | 137,25622 |
| 10730 | 40001 | 0 |
| 13062 | 1012 | 412 |
| 26600 | 1007 | 407 |
| 27014 | 1011 | 411 |
| 35570 | 1406 | 406 |
| 45152 | 4 | 10 |
| 60000 | 7 | 1405 |
| 66074 | 13746 | 12746 |
| 10356-10362 | 5007, 110102, 1 | 11102, 105002, 240 |

### B.3.2 Modifications For Number of Cylinders and Tracks

| Location | From | To |
|---|---|---|
| 7634 | 24024 | 20025 |
| 7654 | 24025 | 20027 |
| 7732-7734 | 12706, 1100 | 4737, 104106 |
| 27500-27502 | 12737, 1466 | 13737, 104400 |
| 30522-30524 | 22726, 1000 | 23726, 104400 |
| 31372-31374 | 12737, 1466 | 13737, 104400 |
| 32022-32024 | 12737, 1466 | 13737, 104400 |
| 32240-32242 | 22737, 1466 | 23737, 104400 |
| 32730-32732 | 12737, 2400 | 13737, 104410 |
| 33224 | 3400 | 37400 |

Modifications For Number of Cylinders and Tracks (con't)

| Location | From | To |
|---|---|---|
| 33250-33252 | 12737, 2400 | 13737, 104410 |
| 33344-33346 | 12737, 1467 | 13737, 104402 |
| 33636 | 2000 | 4000 |
| 33662-33664 | 12737, 1467 | 13737, 104402 |
| 36364 | 633 | 40 |
| 36370 | 634 | 41 |
| 36754 | 634 | 40 |
| 36760 | 633 | 41 |
| 37436-37440 | 12737, 2400 | 13737, 104410 |
| 37700 | 4000 | 40000 |
| 37724-37726 | 12737, 2400 | 13737, 104410 |
| 40032-40034 | 12737, 1467 | 13737, 104402 |
| 40304 | 2000 | 4000 |
| 40330-40332 | 12737, 1467 | 13737, 104402 |
| 51114 | 177770 | 177700 |
| 51134-51140 | 23727, 51702, 240 | 23737, 51702, 104412 |
| 51150-51152 | 162737, 5 | 163737, 104412 |
| 51224-51226 | 22737, 1467 | 23737, 104402 |
| 51340-51342 | 22737, 1467 | 23737, 104402 |
| 51600 | 176000 | 170000 |
| 52236-52242 | 23727, 1432, 1466 | 23737, 1432, 104400 |
| 52304-52310 | 123727, 1405, 4 | 123737, 1405, 104404 |
| 57730-57736 | 23727, 1432, 1466 | 23737, 1432, 104400 |
| 57776-60002 | 123727, 7, 4 | 123737, 1405, 104404 |

The following subroutine must be inserted where indicated. The previous contents of the locations should all be zeros.

Locations: 104106-104174

Contents: 13700, 1276, 062700, 36, 12701, 104400, 12710, 100027, 11021, 11011, 5221, 12710, 100030, 11021, 11011, 5221, 105021, 116121, 177775, 12710, 100036, 16100, 177776, 6200, 6200, 6200, 10011, 207.

## B.4 ZRMD-B0 FUNCTIONAL TEST - PART 2 (August 1977)

### B.4.1 Modifications for Correct Operation

| Location | From | To |
|---|---|---|
| 40452 | 4 | 10 |
| 63360 | 13746 | 12746 |

Both of the above modifications correct unidentified program bugs.

## B.4.2 Modifications For Number of Cylinders and Tracks

| Location | From | To |
|---|---|---|
| 7656 | 24024 | 20025 |
| 7674 | 24025 | 20027 |
| 7732-7734 | 12700, 1100 | 4737, 101550 |
| 17514-17516 | 12737, 2037 | 13737, 102514 |
| 20374-20376 | 12737, 1466 | 13737, 102500 |
| 22272-22274 | 22737, 2000 | 23737, 102506 |
| 22300 | 103402 | 101402 |
| 23014-23016 | 22737, 1466 | 23737, 102500 |
| 23076-23100 | 12737, 1466 | 13737, 102500 |
| 23104-23106 | 12737, 2037 | 13737, 102514 |
| 23374-23376 | 12737, 1466 | 13737, 102500 |
| 23402-23404 | 12737, 2037 | 13737, 102514 |
| 24406-24410 | 12737, 2400 | 13737, 102510 |
| 25066 | 3400 | 37400 |
| 25126-25130 | 12737, 1467 | 13737, 102502 |
| 25614 | 1777 | 3777 |
| 34714 | 5737 | 0 |
| 36766-36770 | 122763, 4 | 123763, 102504 |
| 44414 | 177770 | 177700 |
| 44434-44440 | 23727, 45202, 240 | 23737, 45202, 102512 |
| 44450-44452 | 162737, 240 | 163737, 102512 |
| 44474-44500 | 23727, 45200, 5 | 23737, 45200, 102506 |
| 44510-44512 | 162737, 5 | 163737, 102506 |
| 44524-44526 | 22737, 1467 | 23737, 102502 |
| 44640-44642 | 22737, 1467 | 23737, 102502 |
| 45100 | 176000 | 170000 |
| 45536-45542 | 23727, 1434, 1466 | 23737, 1434, 102500 |
| 45604-45610 | 123727, 1407, 4 | 123737, 1407, 102506 |
| 53764-53766 | 22737, 1466 | 23737, 102500 |
| 54002-54004 | 122737, 4 | 123737, 102504 |

The following subroutine must be inserted where indicated. The previous contents of the locations should be all zeros.

Location: 101550-10646

Contents: 13700, 1276, 62700, 36, 12701, 102500, 12710, 100027, 11021, 11011, 5221, 12710, 100030, 11021, 11011, 5221, 105021, 116121, 177775, 12710, 100036, 16100, 177776, 6200, 6200, 6200, 10021, 112721, 37, 116111, 177767, 207.

## B.5 ZRME-B0 FUNCTIONAL TEST - PART 3 (August 1977)

### B.5.1 Modifications For Correct Operation

| Location | From | To |
|---|---|---|
| 31032 | 42702 | 52702 |
| 30070, 30072 | 404, 240 | 402, 0 |
| 30076, 30100 | 137, 30470 | 5237, 1336 |
| 30416, 30420, | 404, 240 | 402, 0 |
| 30424, 30426 | 137, 30470 | 5237, 1336 |
| 44472 | 4 | 10 |
| 67364 | 13746 | 12746 |

### B.5.2 Modifications For Number of Cylinders and Tracks

| Location | From | To |
|---|---|---|
| 7632 | 24024 | 20025 |
| 7652 | 24025 | 20027 |
| 7706-7710 | 12706, 1100 | 4737, 111760 |
| 20040-20042 | 12737, 1466 | 13737, 112100 |
| 20444-20442 | 12737, 1466 | 13737, 112100 |
| 22076-22100 | 12737, 2037 | 13737, 112114 |
| 32604-32610 | 23727, 1434, 1400 | 23737, 1434, 112100 |
| 32710-32712 | 12737, 2037 | 13737, 112114 |
| 36722-36724 | 22737, 2037 | 23737, 112114 |
| 41000-41002 | 12737, 2000 | 13737, 112116 |
| 41006-41010 | 12737, 1466 | 13737, 112100 |
| 42012-42014 | 12737, 2012 | 13737, 112120 |
| 42426-42430 | 112737, 4 | 123737, 112104 |
| 42446-42450 | 22737, 1466 | 23737, 112100 |
| 42516-42520 | 122737, 4 | 123737, 112104 |
| 42536-42540 | 22737, 1466 | 23737, 112100 |
| 43006-43010 | 122763, 4 | 123763, 112104 |
| 50434 | 177770 | 177700 |
| 50454-50460 | 23727, 51222, 240 | 23737, 51222, 112112 |
| 50470-50472 | 162737, 240 | 163737, 112112 |
| 50514-50520 | 23727, 51220, 5 | 23737, 51220, 112106 |
| 50530-50532 | 162737, 5 | 163737, 112106 |
| 50544-50546 | 22737, 1467 | 23737, 112102 |
| 50660-50662 | 22737, 1467 | 23737, 112102 |
| 51120 | 176000 | 170000 |
| 51556-51562 | 23727, 1434, 1466 | 23737, 1434, 112100 |
| 51624-51630 | 123727, 1407, 4 | 123737, 1407, 112104 |
| 60004-60006 | 22737, 1466 | 23737, 112100 |
| 60022-60024 | 122737, 4 | 123737, 112104 |

The following subroutine must be added to the test at:

Locations: 111760-112052

Contents: 13700, 1276, 62700, 36, 12701, 112100, 12710, 100027, 11021, 11011, 5221, 12710, 100030, 11021, 11011, 5221, 105021, 116121, 177775, 12710, 100036, 16100, 177776, 6200, 6200, 6200, 10021, 112721, 37, 116121, 177767, 105021, 116121, 177776, 112721, 12, 116111, 177776, 207.

## B.6 ZRAF-11 EXTENDED DRIVE TEST (August 1977)

### B.6.1 Modifications for Correct Operation

| Location | From | To |
|---|---|---|
| 21464 | 13746 | 12746 |
| 27722-27726 | 5737, 4322, 1011 | 32737, 100000, 4350 |
| 27730-27734 | 32737, 100000, 4350 | 1405, 12737, 177777 |
| 27736-27742 | 1405, 12737, 177777 | 1446, 137, 30370 |
| 27744-27750 | 1446, 137, 30370 | 5737, 4322, 1401 |
| 37246 | 1750 | 1503 |
| 37604 | 10164 | 110164 |
| 41674 | 10164 | 110164 |
| 43064-43066 | 5702, 1426 | 4737, 44770 |
| 43070-43072 | 4737, 44770 | 5702, 1424 |

All of the above are unidentified program bugs.

### B.6.2 Modifications For Number of Cylinders and Tracks

**Note: Required on drives of less than 100 logical cylinders only

| Location | From | To |
|---|---|---|
| 1774 | 400 | 1466 |
| 2040 | 400 | 1466 |
| 2176 | 144 | 100** |
| 37270-37272 | 22705, 20024 | 122705, 24 |
| 37276-37300 | 22705, 24024 | 122705, 27 |
| 37312-37314 | 22705, 20025 | 122705, 25 |
| 37320-37322 | 22705, 24025 | 122705, 25 |
| 17574-17576 | 20127, 1466 | 20137, 1574 |
| 17602-17604 | 20227, 4 | 20237, 1602 |
| 17022-17026 | 22700, 5, 3365 | 23700, 1602, 2365 |
| 17222-17224 | 122737, 4 | 123737, 1602 |
| 20312-20314 | 122737, 5 | 123737, 1602 |
| 20320 | 3370 | 2370 |
| 33530-33534 | 122702, 5, 3003 | 123702, 1602, 2003 |

The following subroutine must be inserted where indicated. It replaces an existing subroutine of similar function that is no longer needed. The contents of the existing routine are not shown.

Locations: 26632-27004

Contents: 104412, 113704, 1102, 6304, 16401, 1620, 13704, 1450, 62704, 36, 12702, 1566, 5003, 12122, 6237, 1566, 103002, 12122, 401, 5022, 5203, 20327, 14, 1405, 20327, 3, 1363, 24242, 761, 12714, 100027, 11405, 12703, 1574, 5713, 1412, 21327, 1466, 1407, 21327, 1465, 1002, 5305, 402, 20513, 2001, 10513, 12714, 100030, 11437, 1602, 104413, 207.

## B.7 ZRMI-B0 DRIVE COMPATIBILITY TEST (August 1977)

### B.7.1 Modifications For Correct Operation

| Location | From | To |
|---|---|---|
| 21000 | 13746 | 12746 |

The above item is an unidentified program bug.

There are no Part 2 modifications to this test. It is impractical to rewrite this test. To do so would require allocating an indeterminate amount of buffer space near the beginning of the test. The test uses cylinders 0-800 (but not all of them), and tracks 0-4. Any configuration with 801 or more cylinders and 5 or more tracks is compatible with this test.

## B.8 EMULEX DIAGNOSTICS

Self-sizing diagnostics for the RM02, RM03, and RM05 may be ordered from Emulex. The diagnostics are as follows:

S1B18X Formatter
S1B19X Performance Exerciser
S1B10X Functional Test (Part 1)
S1B11X Functional Test (Part 2)
S1B12X Functional Test (Part 3)
S1B13X Extended Drive Test

BLANK

# Appendix C

## Modifications to DEC RP06 Diagnostics

This appendix describes the modifications required in the Digital Equipment Corporation RP06 diagnostics to run on the Emulex Model SC03/BX Controller.

The modifications are in two parts. Part one contains modifications that correct program errors and bypass unsupported features, such as diagnostic mode. Part two contains modifications to change the number of cylinders from 815 to some other value.

Users running on LSI-11 systems without 4 level interrupt and explicit Processor Status Word (PSW) addressing will require ECO #254 for additional PSW patches.

### C.1 CZRJGB0 - RP04/5/6 DISKLESS CONTROLLER TEST - PART 1

Product Code: AC-9208B-MC

MODIFICATIONS (Part 1)

| Item | Location | From | To |
|---|---|---|---|
| 1. | 5714, 5716 | 5737, 1700 | 5777, 173760 |
| 2. | 10776 | 4537 | 406 |
| 3. | 11052, 11062 | 104200, 104200 | 4200, 4200 |
| 4. | 11140, 11150 | 10, 10 | 0, 0 |
| 5. | 11310, 11330 | 1642, 176714 | 1632, 176702 |
| 6. | 11364, 11400 | 5, 401 | 1, 1 |
| 7. | 11542, 11560, 11562 | 1644, 17437, 176706 | 1634, 177776, 176704 |
| 8. | 11620 | 4037 | 474 |
| 9. | 12564 | 177777 | 0 |
| 10. | 12734, 12746 | 4276, 4276 | 4200, 4200 |
| 11. | 13010, 13022 | 17437, 17437 | 0, 0 |
| 12. | 13064, 13076 | 116000, 116000 | 16000, 16000 |
| 13. | 13664 | 17437 | 0 |
| 14. | 14004 | 4276 | 4200 |
| 15. | 14022 | 116000 | 16000 |
| 16. | 14202, 14204 | 4737, 42614 | 137, 15444 |
| 17. | 16352, 16354 | 12706, 1000 | 137, 41064 |
| 18. | 12520 | 177777 | 175777 |

| Item | Explanation |
|---|---|
| 1. | This modification fixes an unidentified program error. The purpose of the instruction is to test for the presence of an RH70 controller vs. an RH11 controller. It does this by testing for the existence of an RH70 register whose address is in location $1700_8$. As written, however, the program |

checks for the existence of location $1700_8$, not the existence of the location whose address is in $1700_8$. This fix corrects the instruction.

2. This modification branches around a portion of the test that only works in maintenance mode.

3-7. These modifications alter bits in the expected results of certain registers, after various register operations, to reflect their expected status when the controller is not in maintenance mode.

8. This modification branches around a portion of the test that can only be run in maintenance mode.

9-15. Same as modification 3-7.

16-17. These modifications jump around maintenance mode read/write tests. These tests can only be run in maintenance mode.

18. Allow for either a 10-bit or 11-bit cylinder address register.

NOTE: This test assumes that the controller is being tested after a system power-up. Certain registers which are not cleared by a Bus Init are assumed to be zeroed, as would be the case on a power-up.

There are no part two modifications to this diagnostic.

## C.2 CZRJHB0 - RP04/5/6 DISKLESS CONTROLLER TEST - PART 2

Product Code: AC-9213B-MC

MODIFICATIONS (Part 1)

| Item | Location | From | To |
|---|---|---|---|
| 1. | 21250, 21252 | 5737, 15020 | 5777, 173544 |
| 2. | 24170 | 15010 | 15014 |
| 3. | 26756 | 177677 | 175777 |
| 4. | 30650, 30652 | 4037, 45702 | 137, 44132 |
| 5. | 30646 | 31154 | 44132 |

Item Explanation

1. This is an unidentified program error. It is exactly the same error as outlined in Modification 1 of the Diskless Controller Test - Part 1.

2. This modification corrects a program error to ensure that all of the controller registers are tested.

3. This modification corrects a program error to test the status of the PSEL bit (the bit under test) instead of the IE bit (which is not under test).

4-5. These modifications jump around those data I/O tests that can only be run in maintenance mode.

There are no part two modifications to this diagnostic.

## C.3 CZRJIB0 - RP04/5/6 FUNCTIONAL CONTROLLER TEST - PART 1

Product Code: AC-9218B-MC

MODIFICATIONS (Part 1)

| Item | Location | From | To |
|---|---|---|---|
| 1. | 6526, 6530 | 5737, 2340 | 5777, 173606 |
| 2. | 12744 | 1005 | 1003 |
| 3. | 17732, 20410 | 30500, 30500 | 10500, 10500 |
| 4. | 21344, 21474 | 20400, 20400 | 400, 400 |
| 5. | 22430, 22724 | 30500, 30500 | 10500, 10500 |
| 6. | 23014 | 116000 | 16000 |
| 7. | 33656, 34356 | 30500, 30500 | 10500, 10500 |
| 8. | 41210-41216 | 240, 240, 240, 240 | 32777, 200<br>141104, 1774 |
| 9. | 42300-42304 | 240, 32777, 100 | 4737, 400, 30377 |
| | 400-406 | 402, 0, 406, 0 | 12703, 100, 5303 |
| | 410-414 | 412, 0, 416 | 1376, 12703<br>100, 207 |
| 10. | 15472 | 177777 | 157777 |
| 11. | 15506 | 177777 | 175777 |

Item — Explanation

1. This is an unidentified program error. It is the same error that is outlined in Modification 1 of the Diskless Controller Test - Part 1.

2. This modification changes a branch to bypass a maintenance mode test.

3-5. These modifications remove the "PIP" bit from a test of RPDS. The "PIP" bit will set during these tests, but not as quickly as in the DEC controller.

6. This test removes the sign change bit from a test of RPOF. Since there is no hardware signal from a storage module drive available to the controller to indicate a phase change in the PLO, this bit is not implemented.

7. Same as modifications 3-5.

8. This modification changes a maintenance mode seek to a normal seek.

9. This modification inserts a timeout loop into the program between the loop that waits on some bit becoming set and the routine that tests for IE equals zero, thus indicating that the interrupt occurred and was serviced. This same timeout loop exists in Part 2 of the functional test. The use of maintenance mode in certain parts of this test may have eliminated the need for the timeout in this test.

10. Allows for either a 5-bit or a 6-bit track address register.

11. Allows for either a 10-bit or an 11-bit cylinder address register.

There are no part two modifications to this diagnostic.

## C.4 CZRJJB0 - RP04/5/6 FUNCTIONAL CONTROLLER TEST - PART 2

Product Code: AC-9223B-MC

MODIFICATIONS (Part 1)

| Item | Location | From | To |
|---|---|---|---|
| 1. | 6412, 6414 | 5737, 2240 | 5777, 173622 |
| 2. | 15342, 15352 | 177702, 2410 | 177672, 2370 |
| 3. | 15366, 15370 | 200,0 | 0, 1 |
| 4. | 15404, 15414, 15430 | 177774, 2574, 200 | 177672, 2370, 0 |
| 5. | 21446, 21456, 21512 | 3402, 0, 200 | 3400, 177777, 0 |
| 6. | 23132, 23142 | 177502, 2574 | 177400, 2370 |
| 7. | 23110, 23120 | 177410, 2410 | 177400, 2370 |
| 8. | 26622, 26630<br>26636, 26644 | 204, 102, 1200<br>100 | 0, 0, 1000, 0 |
| 9. | 26706, 26714, 26734 | 2164, 177774, 100 | 2370, 177672, 0 |
| 10. | 27366, 27270 | 13700, 2270 | 137, 27646 |
| 11. | 33566 | 25 | 1000 |

Item — Explanation

1. This is an unidentified program error. It is the same error that is outlined in Modification 1 of the Diskless Controller Test - Part 1.

2-4. These modifications alter the expected contents of RPBA, RPWC, and the IR and OR bits in RPCS2 at the completion of an aborted write test to compensate for the lack of a SILO buffer. This controller does not alter the values of those registers if the write command cannot be done. The DEC controller does.

5-9. Same as 2-4 above.

10. This modification jumps around a maintenance mode test.

11. This modification increases a stall timer to compensate for the delay between the detection of an error and the setting of the interrupt. This modification is required on processors with cache memory.

MODIFICATIONS - Part 2

| Location | From | To |
|---|---|---|
| 11706 | 11456 | 10000+C-1 |
| 11770 | 1456 | C-1 |
| 12256 | 1456 | C-1 |
| 17366 | 11457 | 10000+C |
| 17444 | 1457 | C |
| 21156 | 11456 | 10000+C-1 |
| 21240 | 11457 | 10000+C |
| 21316 | 1456 | C-1 |
| 21576 | 1457 | C |
| 21606 | 1456 | C-1 |
| 21704 | 11456 | 10000+C-1 |
| 22012 | 1456 | C-1 |
| 22244 | 1457 | C |

NOTE: "C" = #Logical cylinders per drive

C.5 DZRJA-B-D - RP04/5/6 MECHANICAL AND READ-WRITE TEST

Product Code: MAINDEC-11-DZRJA-A-D

MODIFICATIONS Part 2

All of the following locations are changed from '1456' to 'C-1':

1614, 1616, 1620, 1672, 1740, 2004, 2026, 2050, 2072, 2112, 2132, 2170, 2220, 2260, 2312, 2336, 2404, 2450, 2472, 2514, 2536, 2556, 2576, 2634, 2664, 2724, 2756.

C.6 CZRJBB0 - RP04/5/6 FORMATTER PROGRAM

Product Code: AC-9185B-MC

MODIFICATIONS - Part 2

| Location | From | To |
|---|---|---|
| 3352 | 1456 | C-1 |

C.7 CZRJDC0 - RP04/5/6 MULTIDRIVE EXERCISER

Product Code: AC-9195C-MC

MODIFICATIONS - Part 2

| Location | From | To |
|---|---|---|
| 16676 | 1457 | C |
| 25504 | 1456 | C-1 |

C.8 CZRJCB0 - RP04/5/6 HEAD ALIGNMENT PROGRAM

Product Code: AC-9190B-MC

This test is not run. The test is designed to use the hardware and 25 microinch steps in the DEC drives to find the point at which the head crosses the center of the recorded track. Storage module drives do not have a signal available to the controller that would allow the detection of the cross-over point, as they have only a +/-400 microinch offset from nominal.

C.9 CZRJEB0 - RP04/5/6 DUAL CONTROLLER LOGIC TEST - PART 1

Product Code: AC-9200B-MC

See note under section C.10.

C.10 DZRJF-A-D - RP04/5/6 DUAL CONTROLLER LOGIC TEST - PART 2

Product Code: MAINDEC-11-DZRJF-A-D

Neither of these two tests can be run. They require that the drive under test be tied to a single controller via a special cable from the second port, and that the drive have a "neutral" position. The neutral position allows any asynchronous request via either port to immediately seize the drive without having to wait for it. This controller does not have the ability to examine any drive at any given moment since only one drive can be addressed at a time via the A-cable. The "busy" signal is a function of the addressed drive. Therefore, with this controller a "neutral" position must appear as a "busy" to both controllers. The differences are enough that the lack of an immediate seizable state will cause errors in almost all of the sub-tests in each of the dual controller logic diagnostics.

EMULEX

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