TECHNICAL MANUAL

EMULEX CORPORATION

SC11 SERIES

LARGE CAPACITY DISK CONTROLLER

USER CONTROL NO. _____

EMULEX DOCUMENT NO.: SC1151001

REVISION: B

DATE: OCTOBER 1979

Printed in U.S.A.

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SECTION 1
INTRODUCTION

1.1 SCOPE

This manual provides information related to the capabilities, design and installation of the SC11 disk controller. This controller can be used in PDP-11 based systems to interface to any large disks having a Storage Module Drive (SMD) interface. This controller is capable of emulating a number of disk subsystems built for the PDP-11 by Digital Equipment Corporation. Details of the functional characteristics of the controller in a particular emulation can be found in the appropriate User's Manual.

1.2 GENERAL INFORMATION

The SC11 Disk Controller is an embedded two board controller for use with the DEC PDP-11/04-60. Other companion products with similar design include the SC01 for the LSI-11, 11/2, 11/23, and the SC70 for the PDP-11/70. The basic controller is based on an advanced design concept which permits it to be readily adapted to a wide range of controller applications. On the host computer side, the SC11 interfaces to the PDP-11 Unibus, and executes all programmed I/O and DMA operations executed by its DEC disk controller counterpart. On the drive side, the SC11 interfaces to the industry standard Storage Module Drive (SMD) interface, originally defined by CDC, but currently available on almost all large disk drives. Most versions of the SC11 controller emulate a DEC large disk controller. In many cases, these controllers are capable of operating with disks having different characteristics than those used in the DEC disk subsystems. The SC11 controller provides the capability of operating with disks having storage of 12 to 600 megabytes.

1.3 FEATURES

1.3.1 Microprocessor Architecture

The SC11 design incorporates a unique (patent pending) 16-bit bipolar microprocessor to perform all control operations. The microprocessor application provides for reduced component count, high reliability, easy maintainability, and, most importantly, the ability to change the functional capability of the controller by

means of microprogramming. The Emulex controllers achieve functional capability beyond that of the DEC controllers which they emulate by providing enhancement features such as built-in self-test during power-up and built-in disk formatting.

1.3.2 Packaging

The SC11 is constructed on two PC boards which plug directly into the PDP-11 backplane. No cabling is required between the computer and the disk controller. The controller obtains its power from the PDP-11 backplane. The two boards of the controller are connected together with AMP pins along each side of the board, thus eliminating cables between the two boards or special backplane wiring. Cables to the disk drives are connected on the top edge of the board.

1.3.3 Buffering

The controller contains a 1K x 16 high speed RAM buffer used to store the device registers of the controller being emulated and for data buffering. Most emulations set aside 768 words for data buffering providing for three sectors (768 words) of buffering. With this amount of buffering, and the strategies used to employ it, data late situations on the computer bus are not possible.

1.3.4 Error Correction

The controller incorporates a 32-bit error correcting code (ECC) generator and checker capable of correcting single burst errors of up to 11-bits in length and detecting a burst of longer length. In some emulations the data correction is performed in the controller and is therefore transparent to the user, while in others the error position and pattern are presented via registers to the computer for software correction. The latter technique is employed for emulations of DEC controllers which include this error correcting technique.

1.3.5 Self-Test

The controller incorporates internal self-test routines which are executed upon power-up. This test exercises all parts of the microprocessor, buffer and disk interface circuitry. Although this test does not completely test all controller circuitry, successful execution indicates a very high probability that the controller is completely operational. If the controller fails the self-test, it leaves at least one LED error lamp turned on, and the controller cannot be addressed from the computer.

1.3.6 Option and Configuration Switch

A single eight pole DIP switch (SW1) located on the A board is used to configure the firmware for disk sizes and to invoke certain options. The meaning of these switches is dependent on model and are listed in Appendix B for the current SC11 models.

A second four pole DIP siwtch (SW2) located at the top of the A board is used to enable extended functions of the various controller versions; it is accessible to the user while the controller is installed in the system. The meanings of these switches is dependent on the model and are also listed in Appendix B.

1.3.7 Device Addressing

The controller has means of selecting different bus device starting addresses and the number of device registers which can be accessed by the computer. In the SC11, selection is accomplished by means of a pair of DIP switches on the B board. The interrupt vector address is also programmable by means of another DIP switch.

1.4 FUNCTIONAL CHARACTERISTICS

The functional characteristics of the controller are provided by the firmware of its microprocessor. Firmware is available to emulate a number of DEC's large disk subsystems. These are:

Model SC11/A	-	emulates the DEC RP11 controller with RP02 or RP03 drives.
Model SC11/B	-	emulates the DEC RJM02/03 and RJP06 disk subsystems.
Model SC11/C	-	emulates the DEC RK611 controller with RK06 or RK07 drives.
Model SC11/F	-	emulates the DEC RJS04 fixed head disk subsystems.

Some models of the SC11 provide for a one-to-one mapping between the logical drive being emulated and the physical drive attached to the controller. Others provide for mapping two or more logical drives onto a single physical drive. In such cases, there is some reduction in performance because of the elimination of overlapped seeks.

A further description of the four emulation models is given below. Detailed functional characteristics of these models can be found in the applicable User's Manuals.

1.4.1 Model SC11/A

The Model SC11/A emulates the operation of the DEC RP11E controller which was designed to interface with RP02 or RP03 disk drives. This basic controller architecture is used in numerous Model A versions to handle a wide variety of disk drives whose specifications do not match those of any comparable DEC drive and are not suited for other emulations. All versions of the Model A controller entail the mapping of a standard, expanded, or contracted size logical RP02 or RP03 onto a specific make or class of disk drives. The characteristics of the RP02 and RP03 drives are given in Table 1-1.

1.4.2 Model SC11/B

The Model SC11/B emulates the functions of the RJM02/03 or RJP06 disk subsystems. In these DEC disk subsystems, the majority of the controller logic is located redundantly in each of the disk drives which interface to the Unibus via the Massbus and the RH11 Massbus Controller. The SC11/B controllers emulate the entire functions contained in the disk drives and the RH11 Massbus Controller. These subsystems are not available from DEC for the LSI-11. These drives are supported by all operating systems except RT-11. The SC11/B is primarily applicable to disk drives of 40, 80, 160, 200, 300 and 600 megabytes.

Versions of the SC11/B entail mapping of either: standard or expanded size RM02 logical units onto 40, 80, 160 or 300 megabyte disk drives; or a standard or expanded size RP06 logical unit onto 200 or 300 megabyte disk drives. A definition of the DEC RM02/03 and RP06 disk drives is given in Table 1-1.

1.4.3 Model SC11/C

The Model SC11/C emulates the operation of the DEC RK611 controller which interfaces to RK06 and RK07 disk drives. These drives are supported by all DEC operating systems. The SC11/C model is used with the Cartridge Module Drive (CMD) or Hunter Drive. Refer to Table 1-1.

1.4.4 Model SC11/F

The Model SC11/F emulates the functions of the DEC RJS04 fixed head-per-track disk subsystem. The SC11/F maps either standard or expanded logical RS04 size units (1.024 MByte) onto CDC 9733 head-per-track-disks. It is intended to be used with the CDC 9733 fixed head drive. Refer to Table 1-1.

TABLE 1-1

CHARACTERISTICS OF DEC DISK SUBSYSTEMS

CHARACTERISTICS	RP02	RP03	RP06	RM02	RK06	RS04
Platters/Drive	11	11	11	3	2	1
Tracks/Cylinder	20	20	19	5	3	64
Cylinders/Drive	203	406	815	823	411	1
Sectors/Track	10	10	22	32	22	64
Bytes/Sector	512	512	512	512	512	256
MBytes/Drive	20.8	41.6	174.4	67.4	13.9	1.05
Speed	2400	2400	3600	2400	2400	3600
Bit Density (BPI)	2020	2020	4040	6060	2400	2200
Data Rate (K Words/Sec)	102.4	102.4	400	403	270	250

1.5 ORGANIZATION AND USE OF MANUALS

Emulex disk controller documentation is organized into three basic categories: Technical Manuals, User's Manuals, and Applications Notes. There are also other references applicable to application of the controllers.

1.5.1 Technical Manuals

A Technical Manual is provided for each basic disk controller model; SC01, SC11, and SC70. This manual provides information which is common to all microcode versions of the applicable controller, including: general information and features; functional characteristics and specifications; general design description; physical description; configuration and installation procedures; and interface specifications. This manual does not contain any information related to a specific emulation version, programming procedures, and other such data required to functionally apply the controller; such information is contained in other manuals as specified below.

Technical Manuals available for the current Emulex controller series are:

SC0151001 - SC01 Series Controllers

SC1151001 - SC11 Series Controllers

SC7051001 - SC70 Series Controllers

Similar manuals will be made available for future controller product series.

1.5.2 User's Manuals

Controllers are classified into basic models according to the class of DEC disk subsystem being emulated. A model designation has common functional characteristics for all hardware controller series (i.e., SC01, SC11, SC70). The basic models available are:

A - RP11/RP02/RP03

B - RJM02/RWM03, RJP06/RWP06

C - RK611/RK06/RK07

F - RJS04/RWS04

Within each model, there may be several versions of microcode (e.g., A1, A2, etc.) designed to support a particular set of disk drive characteristics.

Since application is dependent upon the model and, in some cases, version, there are separate User's Manuals provided for each model/ version as applicable. These are designated as:

SCXX50901 - SCXX/B1 Models

SCXX50902 - SCXX/A Models

SCXX50903 - SCXX/B2 Models

The appropriate User's Manual contains such information as: functional specifications; disk drive characteristics (typical); applicable diagnostics; disk pack formatting; CSR definitions and function codes; and controller option switch settings. In addition, applicable Applications Notes related to diagnostic patches and operations plus other detailed information are included.

1.5.3 Applications Notes

Emulex Applications Notes are published as supplemental information to the Technical and User's Manuals, and contain specific and detailed technical information. Certain of these, particularly those related to diagnostic and operating system patches, are included in the User's Manuals. A complete list of currently available Applications Notes is available upon request.

1.5.4 References

Other applicable reference documents are listed in Appendix A. In general, Emulex manuals assume the user is completely familiar with all pertinent aspects of DEC computers, packages, peripherals and controllers, etc. and no type of tutorial material on these elements is included. Also, information on applicable disk drives is very limited in Emulex documents, and the manufacturer's documentation should be consulted for details.

Table 1-2
SC11 Series
GENERAL SPECIFICATIONS

The following specifications apply to all SC11 series large disk controllers.

CHARACTERISTIC	SPECIFICATION
FUNCTIONAL	
Design	High-speed bipolar microprocessor-based controller for integration of industry-standard SMD and Winchester type mass storage devices to host PDP-11 computer; incorporates unique (Patent Pending) design to achieve extreme high-speed operations with minimum hardware.
Cumputer Interface	Standard Unibus via SPC interface on B board (power and ground only to A board). Unibus data parity check performed on all transfers.
Disk Interface	Storage Module Drive (SMD) interface standard; serial data rate up to 10 Mhz.
Bus Address Range	0 - 128K Words.
Bus Register Base Address	Slide switch selectable, range 760000_8 - 777770_8.
Vector Address	Slide switch selectable, range 0 - 774_8.
Priority Level	Jumper selectable, BR4-7.
Error Control	On-board 32-bit ECC and 16-bit CRC hardware for error detection/correction under microprogram control.
Status Display	Up to 8 edge-mounted LED's for mode/error/status display under microprogram control.
Option Switches	Eight on-board slide switches for selection of program-controlled operating/configuration options.

Table 1-2 (Cont'd)

CHARACTERISTIC	SPECIFICATION
Buffer Memory	2048 byte high-speed RAM buffer, accessible to the microprogram, for data buffering and internal storage operations. Typically 1536 bytes used for data buffering.
PHYSICAL	
Packaging	Two printed circuit boards interconnected by Amp Mod 1 pins; standard SPC 4-connector interface. Extractor handles provided for easy insertion/removal.
Mounting	Any two adjacent SPC slots in standard backplane or system unit.
Disk Cable and Connectors	One common 60-pin control (A) flat cable connector on SC Microprocessor Board; four 26-pin radial data (B) flat cable connectors on SC B Board:
Physical Drives	1 - 4 per controller.
ELECTRICAL	
Unibus Interface	Approved line drives/receivers used exclusively; one unit load per bus signal line.
Disk Interface	Differential line drivers and receivers used on all signal lines. Daisy-chain (A) and radial (B) cable lengths up to 100 and 50 feet respectively.
Power	+5V ±5%, 9 amps max; -15V ±5%, 0.7 amps max; standard backplane/system unit pins used.
ENVIRONMENTAL	Exceeds all environmental ranges and conditions specified for commercial PDP-11 computers and applicable disk drives.

SECTION 2
DESIGN INFORMATION

2.1 PHYSICAL DESCRIPTION

All Emulex SC11 series controllers incorporate the same physical hardware. The controller consists of two printed circuit boards which are designed to plug directly into a PDP-11 card cage and backplane. The printed circuit boards are coupled electrically and physically by two rows of AMP mod 1 pins. Proper separation of the two boards is maintained by four spacers which are held in place by screws. Figure 2-1 shows the complete SC11 two board assembly.

2.1.1 SC Microprocessor Board (A Board)

The top board of the controller assembly is Part Number SU1110401 and is known as the SC Microprocessor or A board. This board contains the high speed bipolar microprocessor elements of the controller, and is common to both the Emulex SC01 and SC11 series of controllers.

The A board is shown in Figure 2-2. The board is a four layer PCB with power and ground planes on the inner layers and interconnects on the outer layers. The board dimensions are 8.7 inches wide by 10.4 inches high corresponding to the DEC quad board size.

The board plugs into the four backplane connectors of a PDP-11 backplane. The 18 pins of each connector row are designated A through V - excluding the letters G, I, O, and Q - from right to left. The component side pins are designated 1 and the bottom side pins are designated 2. Except for PDP-11 and LSI-11 daisy-chain signals, this board interfaces only the standard plus 5 volt and ground pins. Although the A board does not interface to the Unibus, it does occupy a full quad slot, and therefore, provision is made to jumper through the four daisy-chain bus grant signals to ensure continuity to the B board and succeeding devices. These jumpers are S, T, U, V, and Y. The jumpers labeled P, R, W, and X should be left open as these are the Q-Bus bus grant signals used in the SC01 controller series.

2.1.1.1 Switches and Connector

The A board has a 60-pin flat cable connector labeled J1 at the top edge. This connector is for the A cable which daisy-chains control and status information to all the drives.

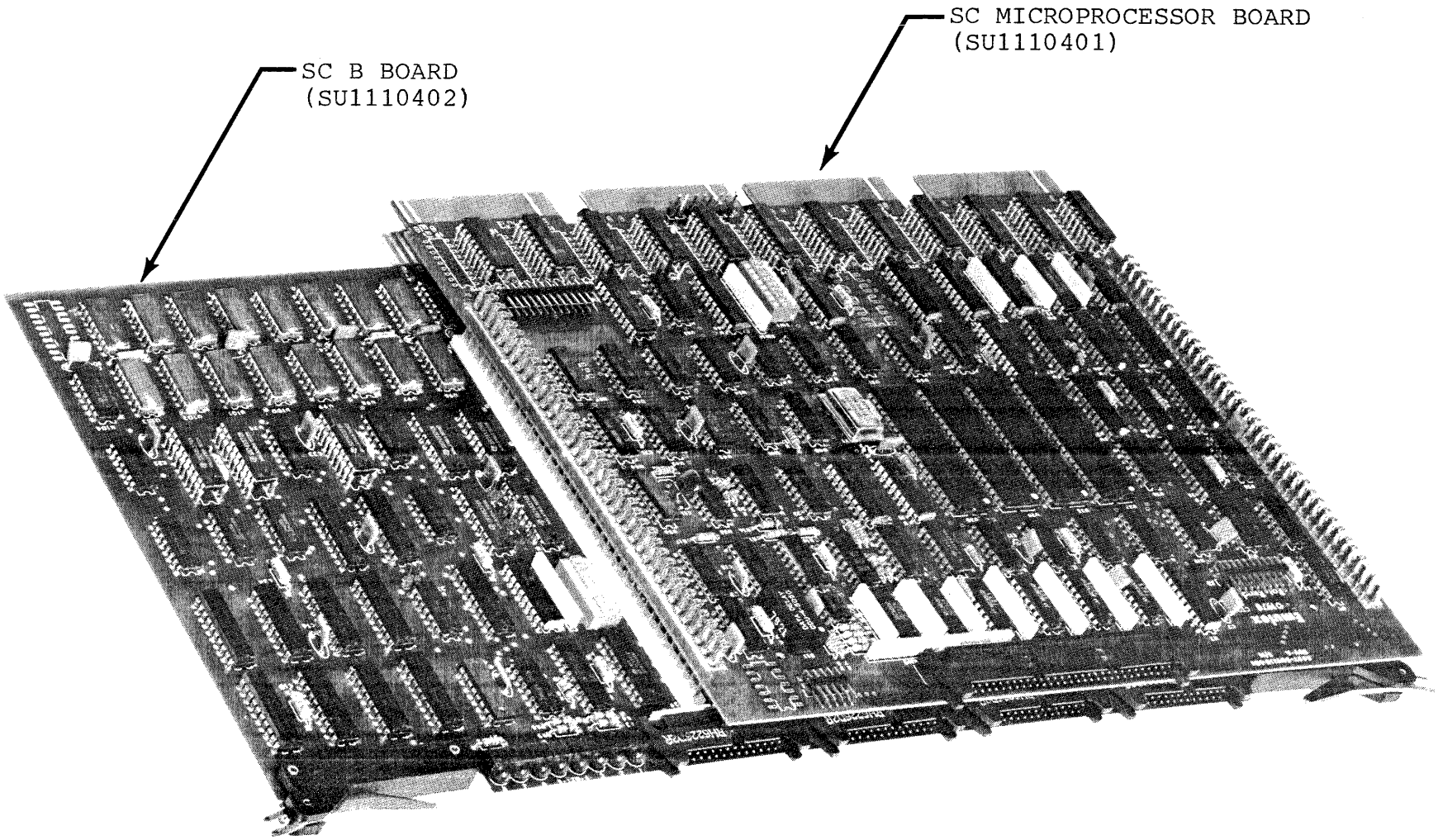


FIGURE 2-1
SC11 SERIES CONTROLLER

Table 2-1

PROM SIZE/MEMORY CAPACITY

PROM LOCATIONS	PROM SIZE	ADDRESS	TOTAL CAPACITY
0-11	4x1024	0-1023	48x1024
12-23	-	-	
0-11	4x1024	0-1023	48x2048
12-23	4x1024	1024-2047	
0-11	4x2048	0-2047	48x2048
12-23	-	-	
0-11	4x2048	0-2047	48x3072
12-23	4x1048	2048-3071	
0-11	4x2048	0-2047	48x4096
12-23	4x2048	2048-4095	

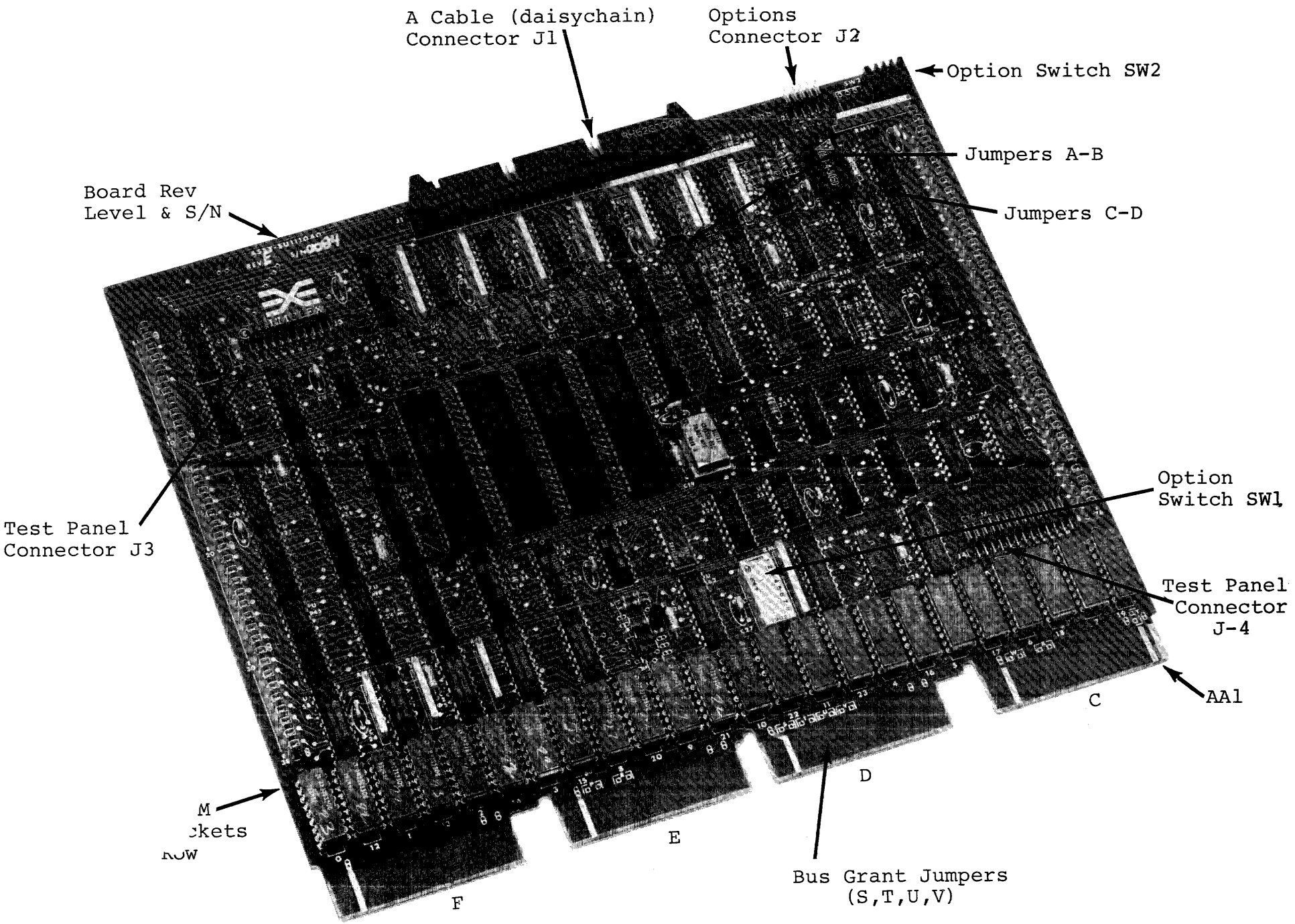


Figure 2-2
SC Microprocessor Board

Connector J2 (if present) parallels switch SW2 and can be used to remote the switch.

Connectors J3 and J4 are used with the Emulex test panel during manufacture test and factory repair. They have no use in normal operation.

The DIP switch labeled SW1 is the option switch used to configure the firmware for drive and functional options to the basic controller. The use of these switches differs from one model to another. A summary of its use is found in Appendix B.

The switch labeled SW2 on the top right edge of the board is used to enable extended functions and formatting.* Refer to Appendix B.

2.1.1.2 PROM Locations

The microprocessor board contains a total of 24 locations for the PROM control memory. These IC locations are on the bottom row as indicated in Figure 2-2. Each location may have either a 4 x 1024 or a 4 x 2048 bit PROM installed to achieve different control memory capacities. PROM locations 0-11 (marked below the IC) contain the lower portion of control memory, and PROM locations 12-23 contain the upper portion. Table 2-1 gives the total control memory size for the different PROM sizes which can be installed.

Most of the SC11/A emulations require only 1K of program space and therefore 12 4 x 1024 PROMS are used. The SC11/B emulations require 2K of program space and either 12 4 x 2048 or 24 4 x 1024 PROMS are used.

2.1.2 SC B Board

The bottom board of the controller assembly is designated Part Number SU1110402 and is known as the B board. This board contains the interface circuitry to the PDP-11 Unibus, the RAM buffer, the disk data circuitry including the ECC, and the interface to four drive B cables. The B board is shown in Figure 2-3. The board is a four layer PCB with power and ground planes on the inner layers and interconnects on the outer layers. The board dimensions are 8.7 inches high by 15.7 inches wide.

*Note: Switch SW2 is not incorporated on Rev. A levels of the A Board.

The board contains card handles which interface mechanically with the board insertion/extraction facilities contained in DEC standard PDP-11 computer and expansion boxes; these handles are used for convenience in inserting and extracting the two-board controller assembly and also act as a card retention mechanism when the controller is installed.

Although overall hex height, the board interfaces only to connector rows C, D, E, F as shown in Figure 2-3. The same pin designation applies to this board as described for the SC Microprocessor Board (paragraph 2.1.1). This board connects to the standard power and ground pins plus all Unibus signal lines defined for the so-called Small Peripheral Controller (SPC) interface used throughout the PDP-11 product line. This interface is defined in detail elsewhere in this manual and in applicable DEC reference documents.

The B Board interfaces to all disk drives via a set of four 26-pin connectors, designated J1-J4, at the top edge. These connectors drive the radial B cables which transfer data and status signals individually to each drive in the system. Refer to paragraph 2.4 for specifications and reference part numbers for this cable and connectors.

Switch SW1 is used to set up the Unibus interrupt vector for the controller; Switches SW2 and SW3 are used together to set up the starting bus location of the control register set defined for the particular controller model implemented. This set of switches perform the same functions for all models of the SC11 Series.

A set of eight LED display lights are mounted along the top edge of the board as shown in Figure 2-3. These lamps display operating and diagnostic status of the controller; the interpretation depends upon the model/version of the controller.

2.1.3 Product Identification and Marking

The SC11 controller consists of the two boards defined in paragraph 2.1.1 and 2.1.2. Each board has a unique part number and carries its own current revision level and board serial number. Locations of these identifications is shown in Figure 2-2 and 2-3 respectively. An individual disk controller board has the letter prefix "SU" to designate it as a board subassembly.

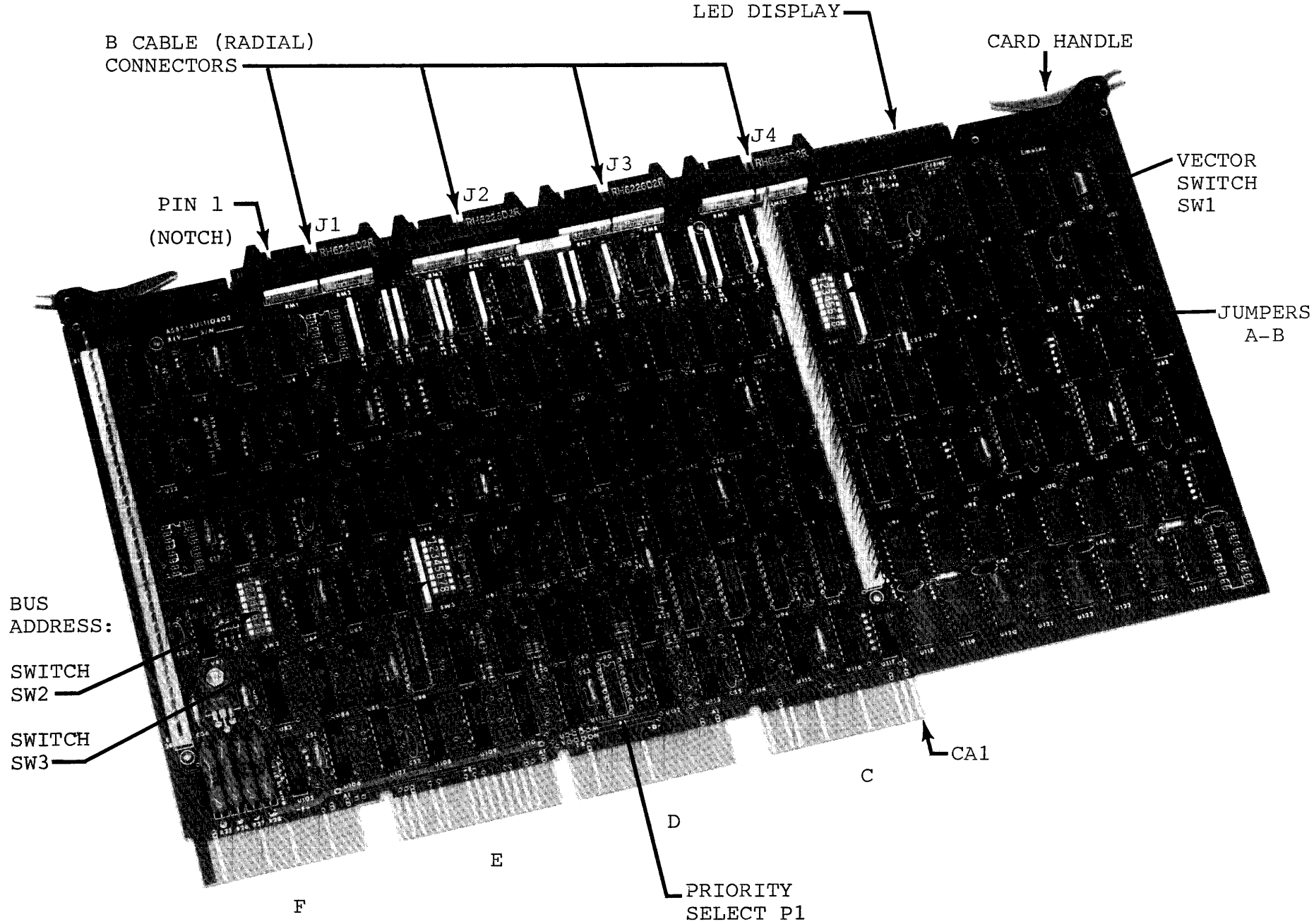


FIGURE 2-3
[illegible] B BOARD

The two board set is combined into a controller assembly; for the PDP-11 compatible controller, the complete 4-digit prefix is "SC11", where the "SC" defines it as a complete two board assembly. This assembly is defined by a configuration code and revision level as follows:

SC11WW - XXX-YY-Z REV. W

1. The designation "WW" is a sequence number which differentiates between any different hardware versions which may exist in the SC11 series. The standard version is "01".

2. The designation "XXX" identifies the microcode PROM set which implements the model (e.g., A, B, F), version (e.g., 1, 2, etc.), and revision level. For example, the B revision level of the A1 version will carry the code "A1B".

3. The "YY" designates any special hardware configuration. Currently, the only such configuration involves jumper strapping of the location of the Sector and Index pulses (A or B cable) and the bus address/range decode. Current codes are:

   X0 - S&I on B Cable
   X1 - S&I on A Cable
   1X - SC01/A
   2X - SC01/B
   3X - SC01/C
   4X - SC01/F

4. The designation "Z" specifies the bus interrupt level: 4 = BR4; 5 = BR5.

   The configuration is given on a label located on the SC Microprocessor Board. This label is installed at the time of shipment, and also contains the serial number of the completed assembly (which differs from the individual board serial numbers). The revision level is also for the completed assembly. This serial number is maintained for the complete assembly as long as the original boards stay together. Should one board be replaced by Emulex, a new serial number will be issued.

The individual boards are also marked with the Emulex name and have a "Made in USA" designation.

> NOTICE
>
> A patent application is pending on certain elements of the controller design, and this is so marked on the boards.

2.2 CONTROLLER ORGANIZATION

A block diagram showing the major functional elements of the SC11 controller is shown in Figure 2-4. The controller is organized around a 16-bit high speed bipolar microprocessor. The ALU and register file portion of the microprocessor are implemented with four 2901 bit slice components. The microinstruction is 48 bits in length and a control store is implemented with 1K x 4 or 2K x 4 PROMS Control store size is normally 1K or 2K depending on the emulation.

The controller incorporates a 1K x 16 high speed RAM buffer which is used to store the device registers of the controller being emulated and provide three sectors (768 words) of data buffering.

The A Cable Register (ACR) provides the storage for all the A cable signals going to the drives. The inputs from the selected drive can be tested by the microprocessor.

Serial data from the drive is converted to 16-bit parallel data and transferred to the buffer by the microprocessor. Likewise, data accessed from the buffer by the microprocessor is a serialized and sent to the drive under control of the servo clock received from the drive.

A 32-bit ECC shift register is used to generate and check the ECC for the data field. The same register is also used in a 16-bit CRC mode for the headers. The actual ECC generation and checking is done independent of the microprocessor, but the correction process which involves the determination of the error position and pattern is done under the control of the microprocessor.

The Data and Address lines are separate bidirectional busses using DEC approved transmitters and receivers. The data lines transmit the interrupt vector as well as programmed I/O and data transfers. All data transfers are controlled by the microprocessor. Address detection of the device address is performed by decoders associated with the two address DIP switches on the B board. The interrupt vector is also programmable by a DIP switch. All DMA timing is done by hardware.

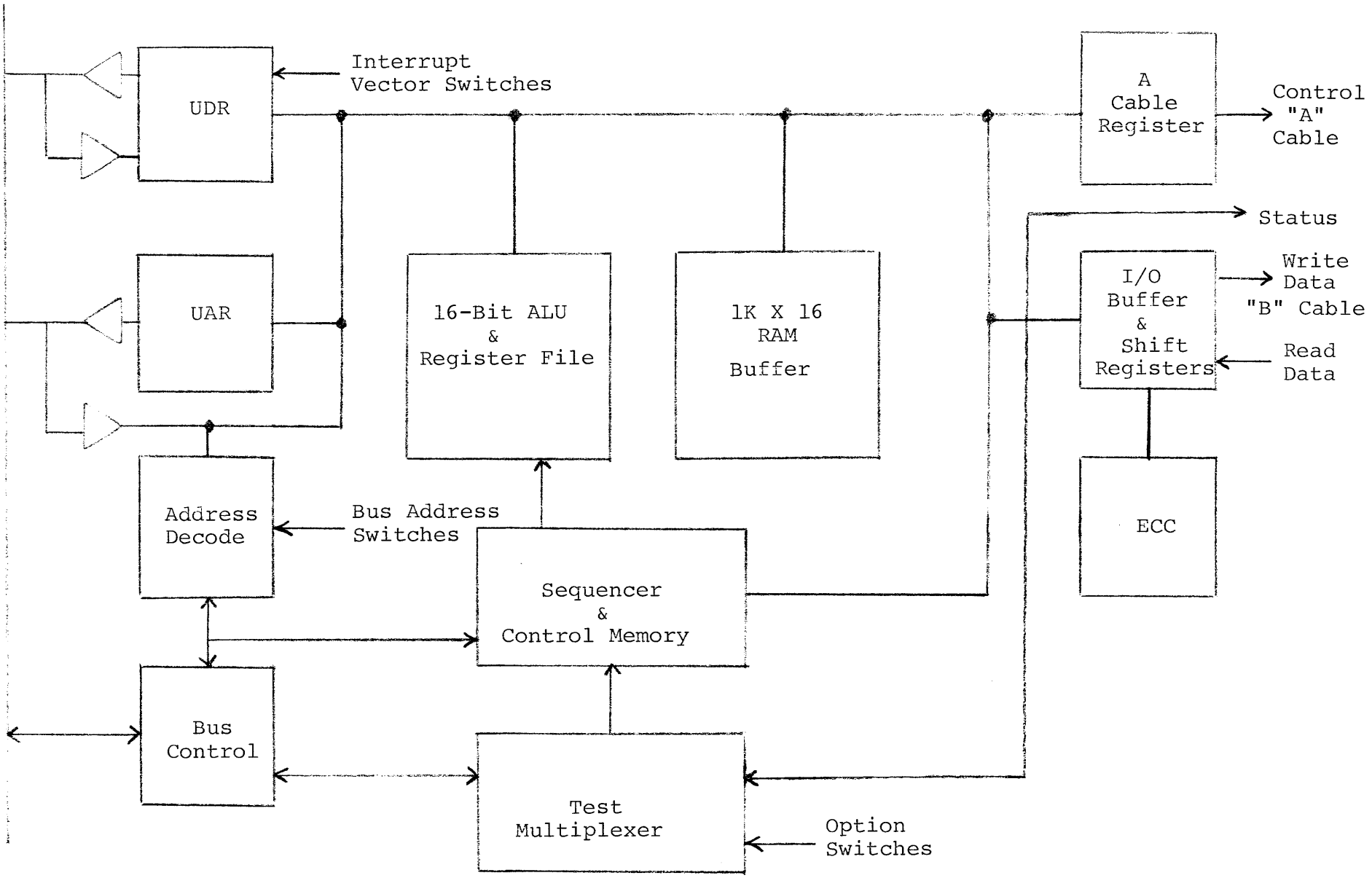


Figure 2-4

SC11 Block Diagram

SECTION 3
INSTALLATION

This section describes the step by step procedure for installation of the SC11 disk controller in a PDP-11 system.

3.1 INSPECTION

A visual inspection of the unit is recommended after unpacking. Specific checks should be made for such items as bent or broken pins or component leads, damaged components, or any other visual evidence of physical damage. The PROMS should be examined carefully to insure that they are firmly and completely seated into the sockets.

3.2 SETUP

Several configuration setups must be made on the controller before mounting it into the computer. In general, the unit will be configured to the customer requirements at the factory; the setup information is listed here in case it becomes necessary to alter the setup after leaving the factory

To perform configurations on the B board, it will be necessary to separate the two boards. This is done by removing the four screws holding the Microprocessor A board to the B board and gently pulling the two boards apart until the AMP pins of the B board are clear of their receptacles. When the configurating is complete, the two boards should be reconnected again by carefully inserting the AMP pins into their correct and respective receptacles and replacing the four screws on the top of the A board. Inspect the AMP pins to insure that pins on the B board have not been misaligned into wrong sockets on the A board.

3.2.1 Register Address Selection

Register address starting location and range is set up by means of DIP switches SW2 and SW3 on the B board. Refer to paragraph 4.2 for detailed information on switch settings.

3.2.2 Interrupt Vector Address

In the SC11, the interrupt vector address is programmed by means of switch SW1 on the B board. Refer to paragraph 4.2 for details.

3.2.3 Interrupt Selection

The SC11 controller can interrupt on one of four interrupt lines. The selection is made by jumpers on the B board. Refer to paragraph 4.2 for details.

3.2.4 Index and Sector Pulse Selection

The SC11 series controllers are designed to have the Index and Sector pulse signals on the B cable from each physical drive. These signals are necessary to drive the sector counter associated with each B port. All the DEC emulations require an updated sector counter which can be read by the computer. Failure to have a valid sector counter can cause incorrect operation of rotational position sensing software. In some cases, this may not be important.

Depending on the disk drive, the Index and Sector signals may not be standardly available in the B cable. The Century drives have these signals available on both the A and B cables. The CDC drives standardly provide Index and Sector only on the A cable, but can be moved to the B cable by minor rewiring of the drive backplane or can be ordered from the factory with this wiring. Sector and Index pulses are usually gated signals on a CDC drive. They must be ungated for proper system operation.

> NOTE
>
> It is recommended that all disk drives always be ordered to specify that Sector and Index be on the B cable.

It is possible to operate with the Index and Sector signals from the A cable if there is only a single physical drive or if proper operation of the sector counter in the device registers is of no concern. To operate with the Index and Sector pulses from the A cable, they must be ungated in the drive so that they are not a function of the drive being selected and will constantly be available even while the controller's microprocessor is polling nonexistent drives.

> CAUTION
>
> Failure to ungate the Sector and Index pulses may result in improper controller/drive operation. Refer to the Drive Manual.

A controller must be configured for receiving the Index and Sector pulses from the B cable or the A cable. This is done on both the A board and the B board as described below. (Refer to Figure 2-2 and 2-3 for location of the jumpers):

For Index and Sector pulses on the B cable:

a. Install jumper A-B on the B board.

b. Leave out jumpers A-B and C-D on the A board.

For Index and Sector pulses on the A cable:

a. Leave out jumper A-B on the B board.

b. Install jumpers A-B and C-D on the A board.

> NOTE
>
> The single drive permitted for A cable Sector and Index pulse operation must be selected as Physical Drive Zero.

> NOTE
>
> If not specified in the purchase order, Emulex will standardly wire the A and B boards for Sector and Index pulses on the B cable.

3.2.5 Option and Configuration Switch

The DIP switches labeled SW1 at the bottom center of the A board are used to configure the firmware for certain disk drive characteristics and functional options. The use of these switches varies from one SC11 model to another. In addition, there is a four pole switch labeled SW2* on the top of the A board which is used to invoke disk formatting and extended functions. Definition of the use of each switch can be found in Appendix B of this manual for currently available emulations. A more detailed description can be found in the User's Manual for the particular emulation model.

3.3 PHYSICAL INSTALLATION

In determining which slots to plug the controller into, it must be remembered that there must be boards in all slots ahead of the disk controller so that the daisy-chained bus grant signals on the backplane have continuity up to the controller. The SC11 can be placed

*SW2 is not implemented on revision level Rev. A of the A Board.

far down the DMA priority chain since it has an adequate amount of buffering to prevent data late errors, permitting assignment of higher DMA priority to other modules plugged into the PDP-11.

The controller boards should be plugged into the PDP-11 backplane with components oriented in the same direction as the CPU and other modules. An attempt to force the boards into a slot with the components facing in the wrong direction may damage the backplane connectors. Always insert and remove the boards with the computer power off to avoid possible electrical damage to the boards. If the PDP-11 card cage can accommodate the extractors on the B board, they should be engaged and will be very useful for inserting and extracting the dual board controller. Be sure that both boards are properly in the throat of the connectors before attempting to seat the boards into the backplane.

> NOTE
>
> The NPG signal jumper between CA1 and CB1 on the backplanes must be removed on the connector used by the B board of the controller. See Section 4.2.1

3.4 DISK DRIVE SETUP

The disk drive must be configured for the proper number of sectors and have an ID plug or address selection switches properly set up.

3.4.1 Sectoring

The disk drive must be configured for 32-sectors on all controller models except the SC11/F which is configured for 64-sectors. 32-sectors per track is equivalent to a sector size of 420 dibits. The exact method of entering this 420 count into the logic of the drive will differ from one drive manufacturer to another and the particular drive manual should be consulted for the exact procedure.

For CDC drives, a value of 419 should be entered into the sector length switches. This is done by closing sector switches 0, 1, 5, 7, and 8.

3.4.2 ID Plug

An ID plug in the range of 0-3 should be placed in the drive. Be careful that no two drives have the same number. Some drives have their address selected via switches on one of the logic cards, and do not use an ID plug.

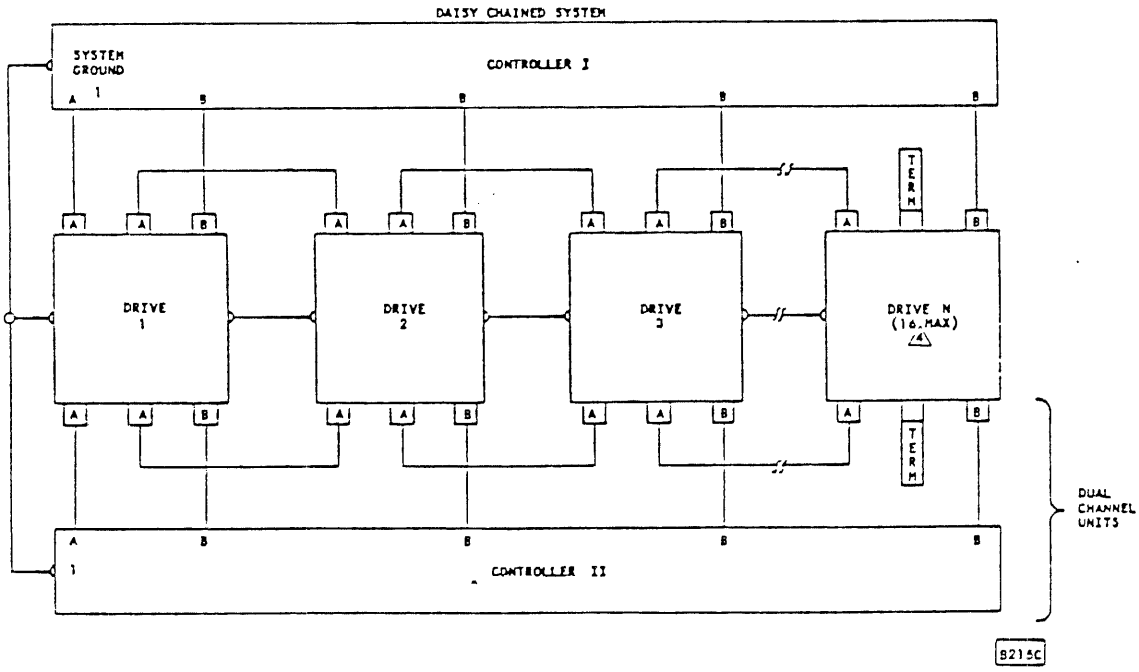
3.5 CABLING

The subsystem cabling of the drives and controller is shown in Figure 3-1.

3.5.1 A Cable

The 60-wire A cable should be plugged into the connector on the A board of the controller and wired to the first drive. If more than one drive is used, it is then daisy-chained to the other drives. The last drive on the A cable must have a terminator installed. This part is supplied by the drive manufacturer. The terminator is generally plugged into one of two A cable connectors on the drive. In some cases, a ground wire emerging from the terminator assembly will have to be connected to the drive to provide a ground return for the resistors in the terminator. Pin 1 of the board connector is on the left. Pin 1 of the cable connector has a notch on the connector body to identify it. Twist and flat cable will have brown-brown twist followed by red-brown twist on the pin 1 edge of the cable. The cable will normally egress to the rear of the controller.

> CAUTION
>
> The connector is not keyed and can be physically reversed in the header. No damage should result, but the system will not operate properly.



Notes:

1. Termination of "A" cable lines are required at controller and the last unit of the daisy chain.
2. Termination of "B" cable receiver lines are made at the controller and are on the unit's receiver cards.
3. Maximum cumulative A cable length per controller = 100 feet.
   Maximum individual B cable length = 50 feet.
4. The **SC01** controller is limited to two physical drives.

Figure 3-1
Unit Cabling

3.5.2 B Cable

Each drive must have a 26-wire B cable wired from the drive to one of the B ports on the B board of the controller. It makes no difference which B port connection is used by a drive. No external terminators are used with the B cable. Pin 1 of the cable connector has a notch on the connector body to identify it. The pin 1 edge of the cable has a black stripe.

> CAUTION
>
> Observe the same caution on connector reversal given in paragraph 3.5.1.

3.5.3 Grounding

For proper operation of the disk subsystem, it is very important that the disk drives have a good ground connection to the logic ground of the computer. The ground connection should be a 1/4 inch braid (preferably insulated) or AWG No. 10 wire or larger. The grounding wire may daisy-chain between drives. If the drive has a switch or jumper which connects the logical signal ground to the cabinet ground (DC ground to AC ground), this connection should be removed once the drive is put online with the controller. It can be connected for performing local offline maintenance on the drive.

> CAUTION
>
> Failure to observe proper grounding methods will generally result in marginal operation with random error conditions.

3.6 TESTING

3.6.1 Self-Test

When power is applied to the computer, the controller will execute a built-in self-test. The LED indicators on the top edge of the B board will flash momentarily. If all LED's turn off, the controller has completed its self-test. If an LED is on after the power-up, there is a problem in the controller and it is unusable. The controller is not addressable from the computer bus when the LED is on. See Appendix C for meaning of LED indicators.

3.6.2 Register Examination

A quick check of the ability to read the controller's registers from the computer console can be made. All of the registers can be examined. A good register to examine at this point is the Drive Status Register. If the Drive Ø is online and ready, the contents of the register should be as follows:

Model	Address	Contents
SC11/A	776710	140000 or 160000
SC11/B	776712	110600 or 111600
SC11/C	777452	100301
SC11/F	772052	000600

3.6.3 Diagnostics

The Emulex SC11 controllers execute the DEC diagnostics for the controller being emulated.

3.6.3.1 Diagnostic Patches

The diagnostics may require some patches if they have not already been patched. The patches fall into three categories:

a. Patches required to connect coding problems in the diagnostics. In some cases, they are supplied by DEC.

b. Patches required to handle non-standard disk size, e.g., 19 track RM02 in the SC11/B1 emulation.

c. Patches to delete DEC controller maintenance-oriented functions not implemented in the controller. These patches are generally associated with the maintenance mode or where testing is done in the lower level logic test diagnostics. The performance exercises and formatters to not have any patches of this type.

The required patches for all three types of patches are available in the form of Application Notes from Emulex.

3.6.3.2 Loading Diagnostics

The diagnostic program required should be loaded from paper tape, disk or magnetic tape. A convenient way of handling diagnostics is by the XXDP Diagnostic Monitor program. XXDP will allow the patches to be placed into the program so that they do not have to be entered

every time the program is loaded. It also will allow for convenient loading for disk or mag tape.

3.6.3.3 Running Diagnostics

Although the diagnostics may be started and run without the listings, the listing will provide a complete set of operational instructions and explain all the function capabilities of the program. In general, it is not necessary to have a complete listing of the diagnostic program for normal evaluation or maintenance of the disk subsystems.

When errors do occur, be sure to carefully evaluate the complete printout and try to correlate between error printouts. It should be remembered that with the SC11/A emulations, the cylinder and track numbers of the printout do not correspond to the cylinder and track of the physical drive.

SECTION 4
INTERFACES

4.1 GENERAL

The controller interface conforms to the Flat Cable Interface Specification for SMD, MMD, FMD, and CMD disk drive families of Control Data Corporation (refer to Table A for reference document numbers). It should be noted that because of certain differences in drive characteristics, the interpretation and/or timing of various interface signals may differ between CDC drive types and also between a given CDC type drive and the equivalent drive type of another manufacturer.

Generally, each version of the controller is set up to interface a given type of drive so that these differences are handled by firmware, in which case no adapter is required. Subtle differences between makes and/or models of drives may require timing and/or functional modifications to an existing firmware package and/or addition of a hardware adapter to the disk drive.

For disk drives which do not incorporate the standard flat cable interface, a hardware adapter will generally be required at the disk drive to physically interface the standard flat cable connector to the type of connector on the drive. This adapter may in some cases include circuitry to handle functional/timing conversion of various signals to match an existing firmware set. In some cases, a special firmware implementation may be necessary.

The following defines the general physical electrical and functional characteristics of the controller disk interface.

4.1.1 Connectors and Cables

The disk controller interfaces with the disk drive by two cables. The 60 conductor A cable daisy-chains to all the drives and plugs into the connector on the A board of the controller. The 26 conductor B cable is a cable between the drive and the controller and plugs into one of the connectors on the B board of the controller. The I/O cable characteristics are as follows:

A cable

Type	30 twisted pair, flat cable
Twist Per Inch	2
Impedance	100 ±10 ohms
Wire Size	#28 AWG, 7 strands
Propagation Time	1.6 to 1.8 ns./ft.
Maximum able Length	100 ft. cumulative
Connector Type	2 x 30 pins, 0.025" Sq, on 0.1" grid

B cable (with ground plane)

Type	26 conductor, flat cable with ground plane and drain wire
Impedance	130 ±15 ohms
Wire Size	#28 AWG, 7 strands
Propagation Velocity	1.65 ns./ft.
Maximum Cable Length	50 ft.
Connector Type	2 x 13 pins, 0.025" Sq, on 0.1" grid

4.1.2 Input Circuits

The input receivers for the A and B cables are MC3450 quad differential receivers equivalent to 75108 receivers. The lines of the A cable are terminated with 82 ohms to ground. The lines of the B cable are terminated with 56 ohms to ground.

4.1.3 Output Circuits

All output circuits to the drive are MC3452 quad transmitters equivalent to 75110A transmitters. The A cable is terminated with 82 ohms to ground from each line.

4.1.4 A Cable Signals

There are 21 signals defined to the drive from the controller, and there are eight signals defined to the controller from the drive via the A cable. Refer to Figure 4-1.

Of the controller-to-drive signals, 10 lines form a Tag Bus on which either Cylinder Address, Track Address, or Control functions are transmitted according to the state of three Tag designator lines. These operations are defined in Table 4-1 for SMD, MMD, and CMD class drives.

One signal, Busy, is used for dual channel drive operation only. The Address Mark Found signal is not used by SC11 series controllers.

There are special considerations associated with the Index and Sector pulses which are always on the A cable (refer to Section 3).

4.1.4.1 Signals to Disk Drive

1. Unit Select Tag

   When this signal is asserted, the drive selected by the binary code on the Unit Select lines becomes selected and remains selected as long as the Unit Select Tag is asserted. In dual channel drives, this signal is also used to reserve the selected drive.

2. Unit Select

   These four lines are a binary code to select a logical number of the drive. The two high order bits are always zero since the controller can only select four drives (0-3).

3. Tag 1

   A pulse of approximately 1.2 microseconds which strobes the cylinder address, specified on the Bit lines, into the drive.

4. Tag 2

   A pulse of approximately 1.2 microseconds which strobes the head address, specified on the Bit lines, into the drive.

5. Tag 3

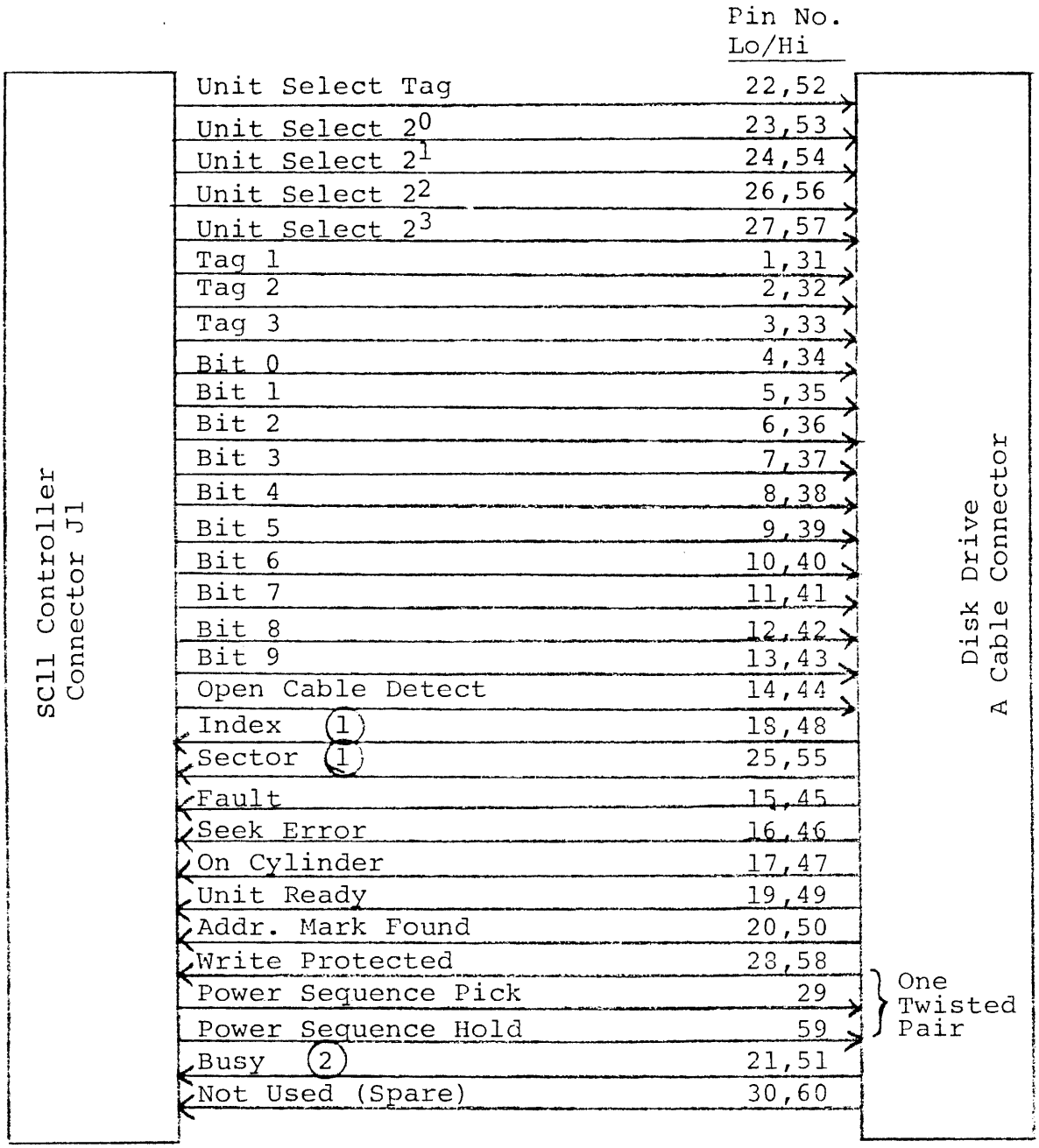
   The Tag 3 is asserted for initiation of control functions specified on the Bit lines.

6. Bit Lines (Tag Bus)

   These ten lines carry the cylinder address (Tag 1), the head address (Tag 2), or a control function (Tag 3).

7. Open Cable Detector

   This signal is asserted all times to the drives when the cable is connected and the controller powered-up.



Notes

1. If Index and Sector pulses on A Cable are used; SC11 must be properly configured, system is limited to single drive operation, and drive must be selected as Unit 0.

2. Dual Channel Units only

Figure 4-1
A Cable Signals

Table 4-1

TAG BUS DECODE, SMD/MMD/CMD

BUS	TAG 1 IN CYLINDER ADDRESS	TAG 2 IN HEAD SELECT	TAG 3 IN CONTROL SELECT
Bit 0	2^0	2^0	Write Gate
1	2^1	2^1	Read Gate
2	2^2	2^2	Servo Offset Plus
3	2^3	2^3	Servo Offset Minus
4	2^4	2^4 (2)	Fault Clear
5	2^5		AM Enable
6	2^6		RTZ
7	2^7		Data Strobe Early
8	2^8		Data Strobe Late
9	2^9		Release (1)

(1) Dual channel units only.

(2) This bit is volume address which is stored in a bi-stable within the CMD drive. The stored volume address and "Tag 1" result in a volume select if the cylinder address is valid. A zero denotes the removable cartridge and a one denotes the fixed disks.

8. Power Sequence Pick and Hold

These two signals are used to control the power-up sequencing of the drives so that only one drive powers-up at a time. These two signals will be at a ground potential when the controller is powered-up.

4.1.4.2 Signals From Disk Drive

1. Fault

When this signal is asserted, a fault condition exists in the drive.

2. Seek Error

When this signal is asserted, a Seek Error has occured. The error is cleared by performing a return to zero. The signal indicates that the drive was unable to complete a seek within 500 miliseconds.

3. On Cylinder

This signal indicates that the drive has positioned the heads over the desired track.

4. Unit Ready

This signal indicates that the drive is selected and up to speed, that the heads are positioned over the recording tracks, and that no fault condition exists within the drive.

5. Write Protected

This signal is asserted when the drive is Write Protected. Any attempt to write while protected will cause a fault to be issued.

6. Busy (Dual Channel Only)

This signal is asserted when the drive is reserved and/or selected by the other channel.

7. Index

See paragraphs 3.2.4 and 4.1.5.2.

8. Sector

See paragraphs 3.2.4 and 4.1.5.2.

4.1.5 B Cable Signal

There are two signals defined to the drive from the controller, and there are seven signals defined to the controller from the drive via the B cable (refer to Figure 4-2).

Two of the signals from the drive - Index and Sector - are not always present in all drives, although these signals can be wired into the B cable. There are special considerations associated with these signals when they are not on the B cable (refer to Section 3).

4.1.5.1 Signals to Disk Drive

1. Write Data

   This signal carries the data which is to be recorded on the disk pack.

2. Write Clock

   This signal is the clock used to transmit the Write Data to the drive. It has a positive edge in the center of the bit cell. The Write Clock is derived from the Servo Clock received from the selected drive.

4.1.5.2 Signals From Disk Drive

1. Read Data

   This signal transmits the recovered data in NRZ form.

2. Read Clock

   The Read Clock positive edge clocks the Read Data into the controller. This signal must be in phase lock with the data on the pack within ten microseconds after turning on Read Gate.

3. Servo Clock

   This signal is a phase locked 9.677 MHz clock synchronized with the servo track of the drive. This signal is used to generate the Write Clock during write operation.

4. Seek End

   Seek End is the logical combination of On Cylinder and Seek Error to indicate that a seek operation has terminated.

5. Unit Selected

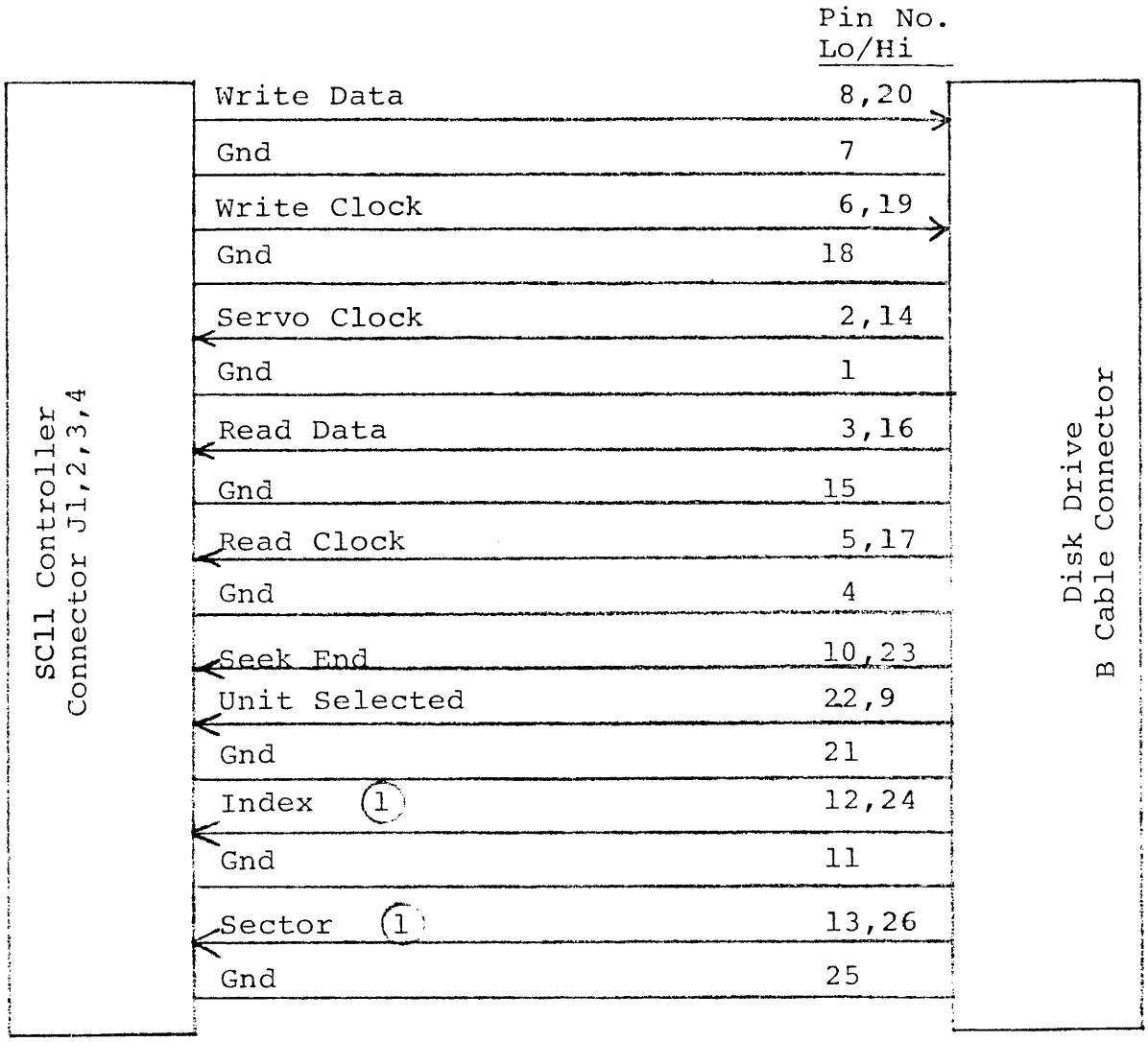
This signal is asserted when the unit is selected. It is used by the controller to verify that a unit has been selected in response to the assertion of the unit select tag.

6. Index

This signal is a pulse of approximately 2.5 microseconds occuring once per revolution. The leading edge of this pulse is considered to be the leading edge of sector zero.

7. Sector Mark

This signal is a pulse of approximately 1.25 microseconds defining the beginning of all sectors except sector zero. The timing of the sector mark must be established in the drive by switches or jumpers as specified by the manufacturer. In some cases, there may be a sector mark defining a short unused sector immediately preceeding the index pulse.



Note

1. Index and Sector pulses must be on the B Cable for multiple drive operation. Not all drives have these signals available on both the A and B Cables.

Figure 4-2
B Cable Signals

4.2 UNIBUS INTERFACE

All models of the SC11 controller series interface to the PDP-11 Unibus via a Small Peripheral Controller (SPC) slot. Several SPC slots are typically provided in the various backplane configurations available with each PDP-11 processor model, and these locations are generally recommended for installation of the SC11 controller. SPC slots may also be obtained in several types of system units included either in expansion boxes or as stand-alone items.

4.2.1 Functional Interface

A diagram of three specific PDP-11/34 series backplanes is shown in Figure 4-3 to illustrate the interface details typical of all current PDP-11 computers. Either the standard or modified Unibus is carried in the A and B colums (not used by the SC11), and the SPC slots are contained in colums C-F. The orientation of the component side of all boards installed in these backplanes is shown for reference. The SC11 may be installed in any adjacent pair of these SPC slots.

Figure 4-4 shows the SPC pin designations (refer to Figure 2-2 and 2-3 for the orientation of the SC11 Unibus connectors and pins). Signals that are used by the SC11 are identified.

The following should be observed in installing and using the SC11 in a typical backplane:

1. The signals NPG (IN) on CA1 and NPG (OUT) on CB1 must not be jumpered together in the slot occupied by the SC B Board (SU1110402). Typically, PDP-11 backplanes come with jumpers installed across these pins in all SPC slots, and the applicable jumper must cut for the SC11 to operate. Similarly, all other NPG (IN) and NPG (OUT) pins must be connected either through wire jumpers or through appropriate on-board grant propagation circuitry in all SPC slots preceeding the SC11, and the backplane should be carefully inspected to insure that these conditions exist. Note that it is not necessary to either open or short these pins in the slot occupied on the SC Microprocessor Board (SU1110401) since an on-board etch connection is made between these two pins.

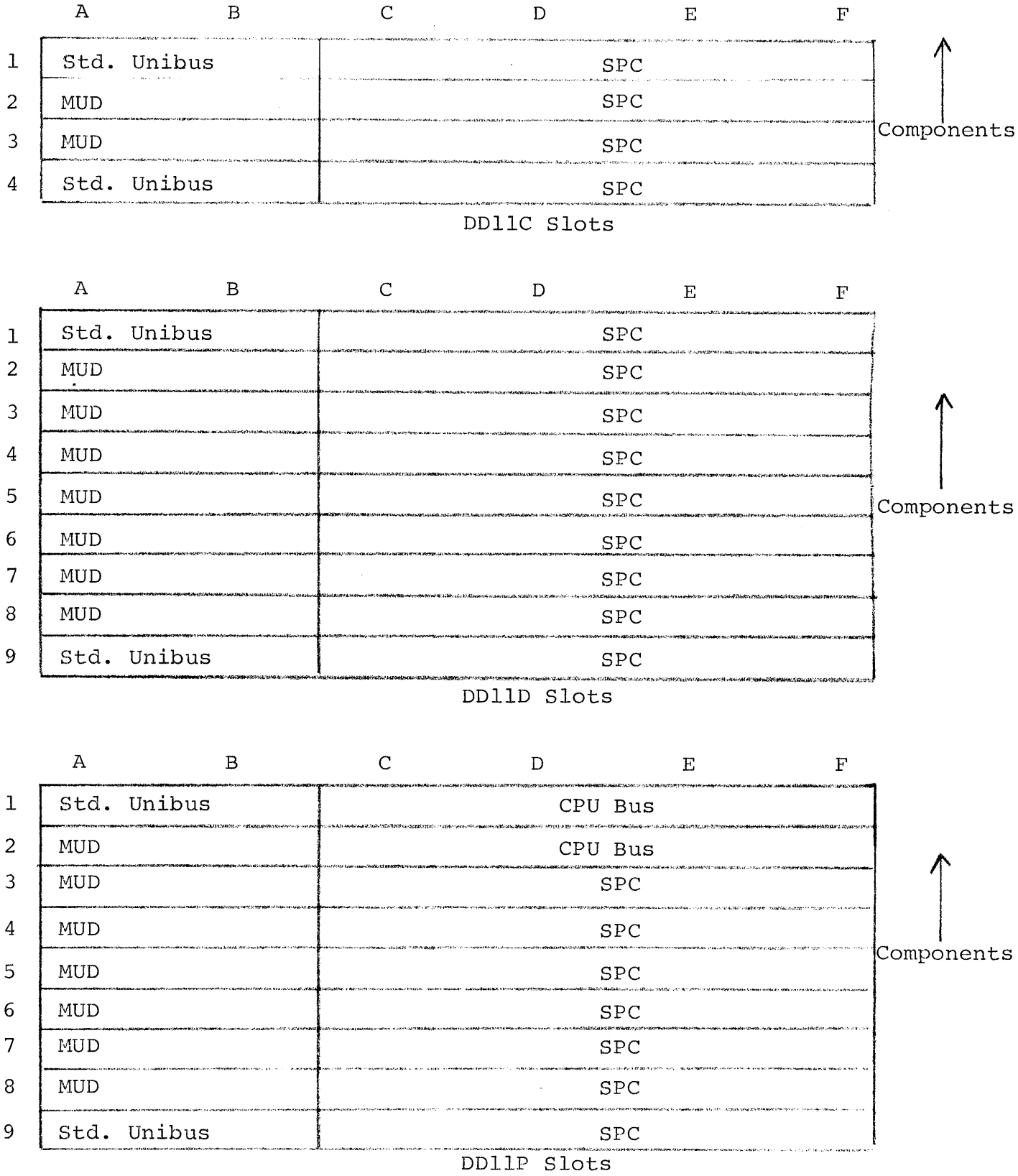


Figure 4-3
PDP 11/34 Backplanes

Column	C		D		E		F	
Side / Pin	1	2	1	2	1	2	1	2
A	NPG IN	+5V		+5V		+5V		+5V
B	NPG OUT					-15V		-15V
C	PAL	GND		GND	A12L	GND		GND
D		D15L		BR7L	A17L	A15L	BBSY L	
E		D14L		BR6L	MSYN L	A16L		
F		D13L		BR5L	A02L	C1L		
H	D11L	D12L		BR4L	A01L	A00L		
J		D10L			SSYN L	COL	NPRL	
K		D09L		BG7 IN	A14L	A13L		
L		D08L	INITL	BG7 OUT	A11L			
M		D07L		BG6 IN			INTR L	
N	DCLO	D04L		BG6 OUT		A08L		
P		D05L		BG5 IN	A10L	A07L		
R		D01L		BG5 OUT	A09L			
S	PBL	D00L		BG4 IN				
T	GND	D03L	GND	BG4 OUT	GND			SACK L
U		D02L			A06L	A04L		
V	ACLO	D06L			A05L	A03L		

Note: Undesignated pins are not used by SC11.

Figure 4-4
SPC Pin Designations

2. The same general kind of rules apply for the four sets of Bus Grant priority lines contained in the D column as follows:

Grant In		Grant Out	
Signal	Pin	Signal	Pin
BG4(IN)	DS2	BG4(OUT)	DT2
BG5(IN)	DP2	BG5(OUT)	DR2
BG6(IN)	DM2	BG6(OUT)	DN2
BG7(IN)	DK2	BG7(OUT)	DL2

All BG in and out pins on all levels must be closed ahead of the two SP slots occupied by the SC11, and the pair of pins associated with the BR level of the SC11 (BR5 is standard, but the SC11 may be assigned to another level by on-board jumpers) must be open on the backplane. The BG pins on all levels are jumpered by etch on the SC microprocessor board, and the BG pins on all unused levels are jumpered by appropriate wiring on the SC B Board.

Typically, the BG lines are left open on backplanes and system units and must be jumpered by backplane wiring or closed through appropriate propagation circuitry on preceeding boards. Open BG lines created by improper wiring or removal of boards from a backplane are a very common cause of system hang-up.

4.2.2 Unibus Address and Interrupt Vector

The SC11 must be configured for a starting address of its control register group and for the vector location of its interrupt operations. The standard addresses used for these parameters may differ with the particular controller model; different addresses must be assigned when more than one controller is installed in a system.

Slide switches are provided on the SC B Board for conveniently assigning address and interrupt vectors. Switches SW1 is used for the interrupt vector setting, and SW2 and SW3 are used for the register starting address (refer to Figure 2-3 for the physical locations of these switches). It should be noted that the two bus address switches SW2 and SW3 are not accessible when the two controller boards are assembled, therefore, the bus starting address should be specified, if possible, at the time of original delivery of the unit.

4.2.2.1 Bus Address

Switches SW2 and SW3 on the B Board control both the starting bus address of the control register set and the address block size (i.e., number of control register addresses) that will be decoded. To accomplish this, the individual contacts on the two switches (designated 1-8) are divided into three groups which are used for the following functions:

Group 1: SW3-1 through 7, SW2-1 through 3 } starting address of Register Block

Group 2: SW2-4 through 6: max size of Register Block

Group 3: SW2-7 and 8: upper address limit of Register Block

1. Group 1 Switches

   The ten switches in this group set up the decode of the 18 Unibus Address lines (A17-A00) used to determine the starting address of the control register block of the controller. Bus address bits A17-A13 are always decoded as Ones, and address bits A02-A00 are ignored as "don't care" conditions. The Group 1 switches therefore select a starting address decode range of 760000-777777 (octal). Table 4-2 summarizes the correspondence of Group 1 switches to the Unibus address lines.

2. Group 2 Switches

   Since Unibus address bits A02-A00 are not decoded, selection of a starting address automatically provides a 4-word address block (note that A00 is the byte control and does not apply to bus register addressing which is always a full word address). The Group 2 switches may be used to assign a "don't care" condition in the decode to Unibus address bits A03, A04, or A05 to select a maximum register block size of 8, 16, or 32 words. Assignment of the switches to the Unibus address lines is given in Table 4-3. The following should be noted:

   a. The "don't care" condition is selected by turning a given switch OFF; that is, if the switch is OFF, the corresponding address line will be ignored in the address decode. Note that the case of all three switches ON selects a four-word block size which is not a useful setting.

Table 4-2

ADDRESS SWITCH GROUP 1
REGISTER BLOCK STARTING ADDRESS

Unibus Address Bit	Address Switch	Notes
A12	SW3-7	Switch ON=1
A11	SW3-6	Switch OFF=0
A10	SW3-5	
A09	SW3-4	
A08	SW3-3	
A07	SW3-2	
A06	SW3-1	
A05	SW2-3	
A04	SW2-2	
A03	SW2-1	

Table 4-3

ADDRESS SWITCH GROUP 2
REGISTER BLOCK SIZE

Unibus Address Bit	Address Switch		Block Size (Words)
	No.	State	
A03	SW2-4	ON	4
		OFF	8, 16, 32
A04	SW2-5	ON	4-8
		OFF	16, 32
A05	SW2-6	ON	4-16
		OFF*	32

*Switches SW2-4, 5 must also be OFF

b. The switches should be set to OFF in the progressive order A03, A04, A05; that is, a switch corresponding to a higher number address line should never by OFF when a lower number switch in this group is ON.

3. Group 3 Switches

These switches are used to set up an upper address limit on the register block which is less than would be obtained by the Group 2 Switches. These are provided for specific definitions of controllers being emulated. The two switches in this group are used to effectively subtract either eight or twelve words from the upper limit established by the Group 2 Switches as defined above. Table 4-4 summarizes the functions of these switches. Note that if SW2-7 is ON then SW2-8 must be oFF, and vice versa. Switches SW2-4, SW2-5, and SW2-6 must be OFF for proper operation of Group 3 Switches.

4.2.2.2 Interrupt Vector

There are seven switches provided on switch SW1 to program the interrupt vector address transmitted to the Unibus by the SC11 controller. Table 4-5 summarizes the switch assignments used.

Note the following:

1. Unibus data bits D15-D09 are always generated as zeros by the controller, so the vector address range is 0-774 (octal).

2. The data bits D00 and D01 are ignored since the vector is always a full two word address starting at an even word location.

4.2.2.3 Standard Addresses and Vectors

The standard bus address and interrupt vector address switch settings for the three basic SC11 models are summarized in Table 4-6.

4.2.3 Unibus Priority Level

The SC11 generates a processor interrupt request by asserting a signal on one of the four bus request levels, BR4-BR7. Availability of the bus on this level is determined by the proper level on the corresponding bus grant line, BG4-BG7. Unused BR lines are left open, and unused in and out BG lines must be jumpered together.

Table 4-4

ADDRESS SWITCH GROUP 3
REGISTER BLOCK LIMIT

Unibus Address Decode Inhibit Function	Group 3 Switch	Function
A04 . A03 (Switch ON=Inhibit)	SW2-8 ON	Subtract last 8 words from block
A05.(A04+A03) (Switch ON=Inhibit)	SW2-7 ON	Subtract last 12 words from block

Note: SW2-4, SW2-5, and SW2-6 must all be OFF.

Table 4-5

INTERRUPT VECTOR ADDRESS SWITCHES

Unibus Data Bit	Vector Address Switch	Notes
D08	SW1-8	Switch OFF=0
D07	SW1-7	Switch ON=1
D06	SW1-6	
D05	SW1-5	
D04	SW1-4	
D03	SW1-3	
D02	SW1-2	

Table 4-6

STANDARD BUS ADDRESS/INTERRUPT VECTOR SWITCH SETTINGS

Switch (OFF unless noted)	SC11 MODEL		
	SC11/A (DEC RP02,03)	SC11/B (DEC RM02, RP04,05,06)	SC11/C (DEC RK06,07)
SW3: 7	ON	ON	ON
6	ON	ON	ON
5	ON	ON	ON
4			ON
3	ON	ON	ON
2	ON	ON	
1	ON	ON	
SW2: 8			
7		ON	
6	ON		ON
5			
4			
3			ON
2			
1			
SW1: 8			
7	ON	ON	ON
6			
5	ON	ON	
4			
3	ON	ON	ON
2	ON	ON	
Start Address	776700	776700	777440
Last Address (Blk. Size)	776736 (16)	776746 (20)*	777476 (16)
Interrupt Vector	254	254	210

*Note: Last address is 776752 for PDP-11/70 controllers

The standard priority for current large-capacity disk controllers is level 5, and the SC11 is generally set up for this level. However, the level can be reassigned by appropriate changes on the SC B Board (SU1110402).

All BR and BG in and out lines are terminated at a 16-pin IC location designated P1 (refer to Figure 2-3). On the standard B board, the appropriate interconnects for use of BR5 and BG5 are made in etch at the socket location; unused BR levels are open, and unused BG levels are jumpered in etch. The pin assignments for location P1, including the standard interconnects made, are given in Table 4-7.

To change priority levels, a total of four etch cuts and four jumpers must be made. An alternate method would be to cut all etched interconnects, install an IC socket, and use wired headers for setting up the proper level.

4.2.4 Electrical Interface

Except as defined below, all Unibus input lines to the SC11 are interfaced with an 8837 line receiver, and all Unibus output lines from the SC11 are driven by an 8641 line driver. The SC11 imposes no more than one unit load (as defined) on any line of the bus.

The only excepted input line to the SC11 is the selected BG IN signal which terminates in 180 ohms to +5 volts and 390 ohms to ground.

The selected BG OUT line and NPG OUT lines are driven by a 7438 with its collector connected to +5 volts through 180 ohms.

The following signals are driven by an open collector 7438: NPR, SACK, and the selected BR line.

4.3 MISCELLANEOUS INPUT/OUTPUT SIGNALS

The SC11 has additional special-purpose interface connectors - J2, J3, J4 - provided on the SC Microprocessor Board (SU1110401); refer to Figure 2-2 for physical location of these connectors.

4.3.1 Options Connector J2

Connector J2 is a 10-pin connector provided for implementation of external control input/output functions. The meaning of the active pins in this connector are a function of the microprocessor firmware, and therefore the functional definition of these signals is given in the technical manual for a particular SC11 model. Table 4-8 specifies the signal name, its sense (in or out), and the type of input or output interface circuit used.

The input signals are asserted by a switch closure to the ground level available on pin 5. This permits any external control functions implemented to be mounted on a remotely located control panel.

4.3.2 Test Panel Connectors J3, J4

Test panel signals are defined in applicable documentation for the Emulex Test Panel.

Table 4-7

UNIBUS PRIORITY LEVEL CONNECTIONS

SIGNAL	P1 PIN	UNIBUS PIN	COMMENTS/STANDARD CONNECTIONS
Open	1	-	Unused
BG IN H	2	N/A	Connect selected BGn input level to this pin (BG5 IN Standard)
BG OUT H	3	N/A	Connect selected BGn output level to this pin (BG5 OUT H Standard)
BG4 OUT H	4	DT2	Etch jumpered to P1-5
BG4 IN H	5	DS2	Etch jumpered to P1-4
BG5 OUT H	6	DR2	Etch jumpered to P1-3
BG5 IN H	7	DP2	Etch jumpered to P1-2
BG6 OUT H	8	DN2	Etch jumpered to P1-9
BG6 IN H	9	DM2	Etch jumpered to P1-8
BG7 OUT H	10	DL2	Etch jumpered to P1-11
BG7 IN H	11	DK2	Etch jumpered to P1-10
BR L	12	N/A	Connect selected BR level to this pin (BR5L Standard)
BR4 L	13	DH2	Open
BR5 L	14	DF2	Etch jumpered to P1-12
BR6 L	15	DE2	Open
BR7 L	16	DD2	Open

Table 4-8

OPTIONS CONNECTOR J2 PIN DEFINITION

Pin No.	Signal Name	Sense	Circuit
1	+5V	Output	-
2	PSWI H	Input	74S251
3	PSWM H	Input	74S251
4	PSW2 H	Input	74S251
5	OV	Gnd	74S19 thru 220 Ω
7	OV	Gnd	-
8	PSCLR L	Output	74S194
9	OV	Gnd	-
10	PSINC L	Output	74S273

APPENDIX A
REFERENCE DOCUMENTS

Company	Document No.	Title
CDC	64712400	Flat Cable Interface Specification for the SMD, MMD, and CMD Families
CDC	64709300	Product Specification, Storage Module Drive
CDC	64709700	Product Specification, Mini-Module Drive
CDC	75888221	Product Specification, Cartridge Module Drive
CDC	75888415	Hardware Maintenance Manual, CMD
DEC	1978	PDP-11 Peripherals Handbook
DEC	EK-11034-UG-001	PDP-11/34 System User's Manual
DEC	EK-RP11E-MM-001	RP11-E Disk Pack Drive Controller Maintenance Manual
DEC	EK-RP056-OP	RP05/RP06 User's Manual
DEC	EK-RM023-UG-001	RM02/03 Disk Subsystem User's Guide

APPENDIX B
OPTION SWITCHES

Table B-1 is a summary of the SW1 and SW2 option switches for most SC11 models. See appropriate User's Manual for a detailed description of the switches and the recommended settings.

Table B-1

	A1	A2	A3	A4	A5	A6	A7	B1	B2	F1
SW1-1	Format Enable	Format Enable	Format Enable	Format Enable	Format Enable	Format Enable	Format Enable	411 Cylinder Select	5 Track Select	Not Used
SW1-2	CMD Fixed Volume	CMD Fixed Volume	CMD Fixed Volume	Config. Select #1	CMD Fixed Volume	Not Used	Config. Select #1	Checksum Enable	Checksum Enable	Checksum Enable
SW1-3	Not Used	823 Cylinder Select	12/24 MByte Select	Config. Select #2	Not Used	Not Used	Config. Select #2	815 Cylinder Select	823 Cylinder Select	Not Used
SW1-4	No ECC Correc-tion	No ECC Correc-tion	No ECC Correc-tion	No ECC Correc-tion	No ECC Correc-tion	No ECC Correc-tion	No ECC Correc-tion	19 Track Select	32 Sector Select	No ECC Correc-tion
SW1-5	Alt. ECC Correc-tion	Alt. ECC Correc-tion	Alt. ECC Correc-tion	Alt. ECC Correc-tion	Alt. ECC Correc-tion	Alt. ECC Correc-tion	Alt. ECC Correc-tion	CMD Fixed Volume	Not Used	Alt. ECC Correc-tion
SW1-6	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Single Port Select	Single Port Select	Config. Select #1
SW1-7	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	DMA Bandwidth Control	DMA Bandwidth Control	Config. Select #2
SW1-8	ECC Test Mode	ECC Test Mode	ECC Test Mode	ECC Test Mode	ECC Test Mode	ECC Test Mode	ECC Test Mode	ECC Test Mode	ECC Test Mode	ECC Test Mode
SW2-1	Format Enable	Format Enable	Format Enable	Format Enable	Format Enable	Format Enable	Format Enable	Extended OP Codes	Extended OP Codes	Extended OP Codes
SW2-2	Extended Diag.	Extended Diag.	Extended Diag.	Extended Diag.	Extended Diag.	Extended Diag.	Extended Diag.	Extended Diag.	Extended Diag.	Extended Diag.
SW2-3	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	4 Wd. DMA Burst Select	4 Wd. DMA Burst Select	4 Wd. DMA Burst Select
SW2-4	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used

APPENDIX C

LED INDICATORS

The LED's are used on some models to indicate problems during self-test. They should all be off after powering-up, except as noted below. The following lights have meaning to the user.

LIGHT 1: Activity indicator which is turned on during data transfers to or from the disk.

LIGHT 5: This light will be on if the controller fails the self-test or if a drive is not connected and powered-up. In some models, the light will blink if the self-test is completed properly and a drive is not connected or powered-up with proper code plug.