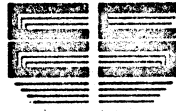


LINE GENERATOR
MAINTENANCE MANUAL

EVANS & SUTHERLAND COMPUTER CORP.



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USE OF THIS MANUAL

This manual was designed to be used with the logic drawings and wire list which form the primary documentation for the Line Generator. The manual makes constant reference to the logic drawings, and it is impossible to use the manual without the logic drawings available for constant cross reference. The drawings and the wire lists are primary documents and have priority in cases where conflict arise between them and this manual.

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OVERVIEW

1.1 General Characteristics

The Evans & Sutherland Line Generator has been carefully designed to generate precision lines. The use of two ramps in the digital to analog conversion provides for a minimum of disruption in the beam position and thus a minimum time loss between lines. All lines, except very, very short lines, are drawn at the same rate. Exact intensity compensation is made for the very short lines, so that all lines appear as if drawn at the same rate. Intensity control is exponential, so that dimmer and contrast controls provided to the operator have real meaning. For 3-dimensional pictures depth cueing is provided which allows the intensity of any part of a line to be a function of its Z coordinate. In addition, a large wraparound protection area is provided, so that lines which extend off the edge of the scope do not wrap around, but rather are omitted entirely.

1.2 Theory of Operation

1.2.1 The α , $1-\alpha$ Ramps

The Line Generator produces two basic ramp signals which are inverses of each other and referred to as α and $1-\alpha$. These signals are used to drive multiplying D/A converters to produce the X and Y deflection voltages and the Z intensity control. The output voltage of the D/A converters is given by the equation:

$$(1) \quad V = \alpha(IO) + (1-\alpha)(IE)$$

where IE and IO are the endpoints of the line.

For example, at the beginning of a ramp α is 0, and the $1-\alpha$ ramp is at 1, so that the deflection voltages are simply proportional to the coordinates of the beginning point of the line. At the end of the ramp α has gone from 0 to 1, so that the voltages are proportional to the coordinates of the endpoint of the line. Since the α and $1-\alpha$ ramps ascend and descend linearly, the deflection voltages vary linearly, and a smooth line is drawn from one endpoint to the other. When the next line is drawn, α descends from 1 back to 0 and $1-\alpha$ goes from 0 back to 1.

The E&S Line Generator uses an alternative form of this basic ramp method to improve precision. Looking at the equation for the voltages bit by bit, it can be seen that there are only four possibilities, namely:

<u>IO</u>	<u>IE</u>	<u>Result</u>
$\alpha 0$	$(1-\alpha) 0$	0
$\alpha 1$	$(1-\alpha) 1$	1
$\alpha 0$	$(1-\alpha) 1$	$1-\alpha$
$\alpha 1$	$(1-\alpha) 0$	α

The important thing to notice here is that, when the inputs match for any pair of bits, the ramp signals make no difference and that bit of the D/A converter can simply be tied to 0 or 1. For short lines, where the ramp is running at high speed, this greatly increases the precision of the line, because small inaccuracies in α and $1-\alpha$ ramps would otherwise tend to distort the line. A switch is associated with each bit of the D/A converter which can choose between 0, 1, α , or $1-\alpha$, depending on the state of the inputs. The Line Generator thus implements an alternative form of equation (1), which is equivalent, but yields better results:

$$(2) \quad V=0(\text{BITS } 00) + 1(\text{BITS } 11) + \alpha(\text{BITS } 10)+(1-\alpha)(\text{BITS } 01)$$

1.2.2 Redundant Coding

Using the alternative form of the equation, (2), accomplishes nothing if the upper bits for a short line are all different. The digital logic of the Line Generator detects this condition and chooses another coding form for one endpoint of the line, so that the most significant bits of both ends will be identical. The fact that redundant coding has been used is recorded and sent to the D/A converter, so that the appropriate compensation can be made. It should be remembered that redundant coding is only used for short lines (and is, in fact, only needed for fast ramps required by short lines).

1.2.3 Ramp Speed

The rate at which the line is drawn is dependent upon the speed of the ramp. In order to have lines appear at appropriate intensities, it is necessary to run the ramp at a speed inversely proportional to the length of the line. For this reason, the basic ramp signals are produced by an integrator whose integration rate is controlled by an estimate of the line length. The X and Y components of the line length are computed digitally by subtracting one endpoint from the other. The resulting difference is normalized by shifting delta X and delta Y left, until the larger is between 1/2 and unity. The number of places shifted becomes a line length exponent, while the resultant shifted numbers serve as mantissas. The analog line length estimating circuit accepts the line length mantissas as inputs and calculates an analog voltage proportional to the reciprocal of the normalized line length. The line length exponent is used to scale the results to give an accurate estimate of the line length. Thus, all lines, except very, very short ones, are generated at a constant writing rate. For very short lines compensation is made by decreasing the intensity of the beam, so that these lines appear at the same intensity as longer lines.

1.2.4 Crossover Detection

In order to get crisp endpoints for lines on the scope, the beam is started somewhat before the beginning point and travels

to a point somewhat past the endpoint. The beam is thus at full speed during the whole line. It is necessary to control beam intensification (i.e., when the beam is turned on), so that only the appropriate portion of the line appears. The overshoot is implemented by running the ramps from somewhat less than 0 to somewhat more than 1. A crossover detector is used to detect when the ramp is between 0 and 1. The output of the crossover detector controls beam intensification.

1.2.5 Wraparound Protection

The Line Generator provides a very large wraparound protection area for use with systems that do not have Clipping Dividers. For such systems (denoted as -104) an extra twelve bits of input is accepted. Any line which extends beyond the addressing limits of the scope is omitted entirely. This is done to protect against wraparound. The Line Generator also eliminates lines whose endpoints (one or both) have Z coordinates which are negative or which are larger than twelve bits ($2^{12}-1$), which would make them too faint to be seen.

1.2.6 Intensity and Contrast Control

The intensity control portion of the scope system treats Z coordinate information as the logarithm of the intensity to be shown on the scope. The numbers given to the Z axis D/A converter correspond to the logarithm of the scope's light output. Because the human eye responds subjectively to the logarithm of the signal that it receives, this form of Z intensity modulation corresponds exactly to "subjective brightness."

The E&S Line Generator allows the operator to control both the intensity of lines and the contrast. A video gain control is provided on the scope assembly which allows the operator to set the maximum intensity. The ratio of the intensity of the brightest line to the dimmest line is set by the contrast control. It is in fact possible to mark the video gain control in F-stop settings such as those used by cameras so that reduction of the dimmer by one F-stop will reduce the intensity by 1/2 at all intensities. When photographing the scope, setting the camera up one F-stop and setting the scope down one F-stop results in the same picture as if they had been unaltered. Similarly, the contrast can be adjusted so that it is appropriate to the gamma of the film being used.

1.2.7 Multiple Scopes

Several scopes may be driven by the same Line Generator. These scopes may all present the same picture simultaneously, or may present different pictures sequentially. The selection of which scope is to show the picture is made by the user, but his choice is masked against the permissible scopes, so that scopes can be protected. The different scopes in a single system may

be of widely differing properties and cost. Associated with each scope is a Driver Card which accommodates the timing and voltage range characteristics of that scope.

1.3 Hardware Characteristics

In order to understand the basic hardware design of the Line Generator, it is best to first study the block diagram 108101-900. Sheet 1 deals with the digital logic (the general flow of data is from left to right). Sheet 2 deals with the analog circuits (the flow here, however, is from right to left).

1.3.1 Control

The Line Generator operates as a pipeline with four separate stages. These stages are controlled by four separate clock pulses. The first three stages have to do with the digital logic, and the fourth stage is comprised of the analog section of the Line Generator. The clock pulse for each stage comes only when the conditions necessary to that stage of processing have been fulfilled. Thus, for example, CLOCK 2 cannot fire until the third stage has accepted the second stage's output, and Stage 1 has new input ready. The communications between the stages of the pipeline are handled through standard flag/acknowledge pairs (see Section 7).

1.3.2 Input (Stage 1)

The first stage of the Line Generator captures the incoming data and commands in the input registers. The data input registers are shown on the left side of Sheet 1 of the functional block diagram. The Line Generator will accept 24 bits of X, 24 bits of Y, and 20 bits of Z information (the 4 bits of Z that are missing are on the low order end of the word). The least significant 12 bits of X and Y come into the XY Digital Cards, while the 8 bits of the 20 bits of Z go to the Z Digital Card. These least significant bits are used in the actual positioning of endpoints on the scope or, in the case of Z, for intensity modulation.

The 12 most significant bits of X and Y go to the Most Significant XY Card, and the 12 most significant bits of Z go to the Most Significant Z Card. These bits are used for wraparound protection; that is, if the coordinates for the endpoints extend into these bits, the whole line is omitted.

1.3.3 The TRUE Registers (Stage 2)

Between CLOCK 1 and CLOCK 2 the output of the TRUE registers is either added to or subtracted from the incoming data. The Line Generator needs both the absolute location of the endpoints (for scope positioning) and the relative displacement (for estimating the line length). Thus, if the input is in absolute form, it serves as the position coordinates directly and the value in the TRUE registers, which represents the coordinates of the last endpoint, is subtracted from the input to give the relative

displacement. If the incoming data are relative, they serve as the displacement directly and must be added to the value in the TRUE registers to compute the new absolute location.

The adders and switches shown on Sheet 1 perform these functions. The OLD lines carry the output of the TRUE registers, and the NEW lines carry the new absolute location which will be clocked into the TRUE registers at CLOCK 2. The relative displacement is clocked into a separate set of registers whose output form the *MAG lines which are sent to the Z Digital Card. Since the Z magnitude is not used in the line length estimate, it is not calculated.

The data on the NEW lines are clocked into either the odd or the even TRUE registers at CLOCK 2. Use of the odd and even registers alternates to make use of the α and $1-\alpha$ ramps.

1.3.4 CODED Registers (Stage 3)

Between Stages 2 and 3 the COMPARE logic must detect when redundant coding is necessary to make the upper 3 or upper 5 bits of the endpoint coordinates the same. The COMPARE logic generates two bits, R4 and R6, which indicate that redundant coding is necessary. These bits control the adders (shown just to the left of the CODED registers) which will subtract the appropriate amount from one of the coordinate values, so that the upper bits will be the same as those of the other coordinate. At CLOCK 3 output of the TRUE registers, which have possibly been recoded, are strobed into the CODED registers.

The *MAG numbers from X and Y are sent to the Z Digital Card, where they are jointly normalized, possibly exchanged, and clocked into registers which hold the values LARGER and SMALLER needed by the line length estimating circuit. The amount that these numbers were shifted is also registered and sent to the analog circuit as a line-length exponent.

1.3.5 Ramp

The α ramp, the $1-\alpha$ ramp, and two reference voltages are generated by the Ramp Card. The speed of the α and $1-\alpha$ ramps is controlled by the line length estimate. This estimate is calculated by a function generator which converts the LARGER and SMALLER inputs provided by the digital logic and the length exponent and produces an output which is proportional to the normalized length of the line. The α ramp is then produced by an integrator whose rate is controlled by the line length estimate. The $1-\alpha$ ramp is generated by precision inversion of the α ramp. The Ramp Card also produces closely regulated reference voltages for 0 (analog ground) and 1 (-REF).

The ramps produced vary from slightly less than 0 to slightly more than 1. This overshoot is provided to avoid transients in the line that might be caused by starting up or slowing

down the beam. A "crossover detector" on the Ramp Card detects when the ramp is between 0 and 1 and sends this information to the "intensify" circuit.

1.3.6 The Multiplying D/A Converter

The D/A converters for X, Y and Z accept two sets of digital inputs from the odd and even CODED registers and the four analog signals produced by the Ramp Card. The digital inputs represent the endpoints of the line to be drawn. The two endpoints are compared for each bit and, as explained in Section 1.2.1, are used to control selection switches which choose one of the four analog signals for that bit of the D/A converter's ladder network. The output of the D/A converters are deflection ramps which are sent to the Scope Driver Cards.

1.3.7 Scope Selection

The Scope Selection Card provides the selection of the scope(s) on which the picture is to be presented. This card also contains the logic which controls the blinking and line-dashing facilities of the Line Generator. In addition, this card provides the intensity correction signals needed to correct the intensity for very short lines.

1.3.8 Scope Driver

With each scope used in the system, there is a Scope Driver Card which provides the video gain and contrast controls and which converts the basic deflection ramps from the D/A converters into deflection signals matched to the characteristics of a particular scope. The Scope Driver Card also compensates for timing and delay characteristics of the particular type of scope. External video signals may also be mixed at this point to cause the scope to present a video picture. The clock diagram shows Scope Driver Cards for Kratos and Hewlett-Packard scopes.

1.4 Operation (See Logic Drawing 108109-604, Control)

The type -104 Line Generator is designed to accept the Group 3 or Group 4 LDS-1 commands which normally go to the LDS-1 pipeline. The Line Generator has its own directive register (on the Scope Selection Card). The information in this directive register and the information in the incoming command are used to control the operation of the Line Generator.

The following operations can be performed by the Line Generator:

Group 3:

2D Absolute or Relative
LOAD XY
LOAD SELECT/INTENSITY (Z)
LOAD DIRECTIVE

3D Absolute or Relative
LOAD XYZ

2D
STORE/SINK XY
STORE/SINK SELECT/INTENSITY
STORE/SINK DIRECTIVE

3D
STORE XY
STORE Z

Group 4:

2D and 3D with or without depth cueing
DRAW TO ABSOLUTE
DRAW TO RELATIVE
DRAW FROM ABSOLUTE
DRAW FROM RELATIVE
DOT ABSOLUTE
DOT RELATIVE
SETPOINT ABSOLUTE
SETPOINT RELATIVE

1.4.1 Loading

The most important thing to remember in loading operations is that the X, Y, and Z registers have both odd and even second stages which alternate in use. This requires that values be copied from odd to even (or vice versa) for those registers which are not being loaded. In order to accomplish this the Line Generator makes use of the fact that it can accept either absolute or relative input. The input stage of the register not being

loaded is cleared, and the control is configured to select a relative load. The result is that the OLD data (see Sheet 1 of the block diagram) are added to zero, and then on the next CLOCK 2 this value is copied back into the other second stage register. This same process is used to keep a constant value in the Z register to give constant intensity when depth cueing is not called for. The logic which controls these operations is shown on location D2-1 on Sheet 5 of the Control Card logic drawings.

1.4.2 Fetching

For fetch-type operations (store or sink) the registers of the Line Generator and the odd/even sequence should not be disturbed. For this reason the poke signals for the stage 2 registers and the change in the odd/even sequence are inhibited. Fetch operations raise a flag to memory and configure the *WD buss to indicate the type of fetch (store or sink). Fetch operations also inhibit CLOCK 3 by inhibiting CDOS (C1, Sheet 5) which prevents the output flag from CLOCK 2 from being raised.

1.4.3 Drawing

With the exception of DOT and DRAW FROM operations, drawing instructions cause data to flow through the Line Generator in the normal manner. For DOT and DRAW FROM instructions, two CLOCK 2 signals must be generated. This is indicated by the signal CDOUBLE (D3, Sheet 5). The first CLOCK 2 computes the location of the new point and causes the Line Generator to perform a setpoint to that location. For DOT operations, the input register is then cleared and the control configured to select relative data, so that the second CLOCK 2 pulse puts a copy of the new location into the other stage 2 register (odd for even or vice versa), and a line of zero length is drawn.

For DRAW FROM operations the signal *TFLINE inhibits the poking of the second stage registers, so the old value is left in the other register and the line is drawn back to the old point.

There are many conditions that can cause the Line Generator to do a setpoint operation. On Location D3 of Sheet 5 of the Control Card drawings, the logic which generates the CSET signal is shown. CSET is generated (1) if a setpoint is called for in the command, (2) if a load is called for, or (3) if either end of the line is off the scope or has Z values which are beyond the limits. This last condition causes any lines which are off the scope to be treated as setpoints, and thus they are not displayed. CSET is also gated with the *MOVE STEP signal generated by DRAW FROM operations (C4, Sheet 6), so that the first CLOCK 2 pulse for DRAW FROM or DOT will cause a setpoint.

ANALOG POWER AND GROUNDING SYSTEM

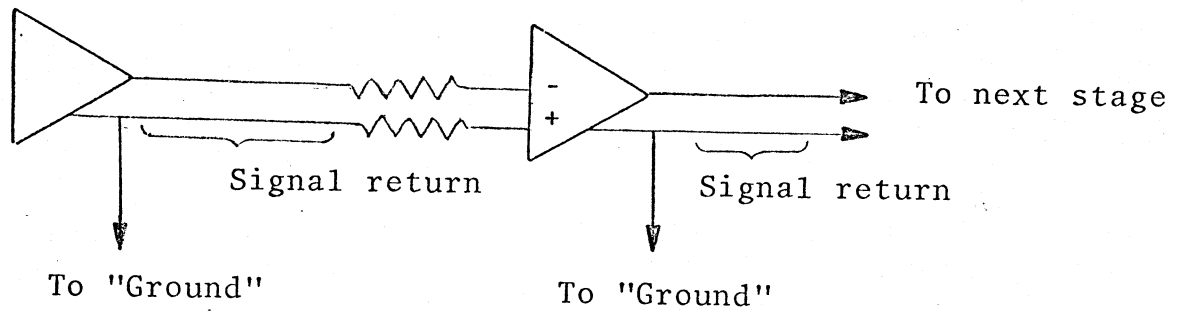
2.1 General

There are two broad principles to be applied in the analog power and grounding system. First, the area within the loop around which sensitive signal currents flow should be minimized, so that the EMF induced in the loop by stray magnetic fields may be minimized. Second, the current actually flowing in sensitive signal paths and their return paths should be minimized to minimize the EMF induced in these paths by IR drop. These two principles have been carefully applied to the design of the analog power and grounding system. The addition of new wires connecting "ground" points should be studiously avoided, because such wires may cause violation of one or both of the above principles.

2.2 Specific Characteristics

These two principles result in several rules of thumb for the design of the power and ground system. First, a sensitive signal wire and its return path will run closely spaced and parallel. Thus, the paths run very close to the "shield" path in the back panel and on the cards in which they appear. The "shield" path should be thought of as the signal return path, and despite its large size should never be used as a power supply return or "grounded" in any way. Second, the power supply return path is separated from the signal return paths. On the Ramp Card, this separation results in "slits" in the "ground" wiring. These slits separate the power supply return from the signal return paths. Third, "ground loops" are avoided. That is, the signal return paths are made to be single point-to-point wires just like the signal paths themselves. Were the signal return path to take two separate routes, back to the signal source, induced EMF's in the loop would appear as a part of the signal. "Ground loops" are ok in the power supply return and delivery paths where such induced EMF's do not really matter.

The overall strategy of delivering accurate signals from the ramp to the scope depends on the use of balanced input amplifiers. The output of a particular amplifier is taken on pair of signal wires intimately co-located to the differential input of the next amplifier. This configuration is as shown in the following figure.



The signal return wires are kept free of stray currents. Only the input currents to the next amplifier flow in them.

This separate return from balanced amplifier is applied in taking the signals:

- (1) From the ramp to the D/A converter
- (2) From the D/A converter to the Scope Card,
- (3) From the Scope Card to the scope itself.

In the last case, of course, the outside of the coax is the return path. Application of the guiding principles implies that no other currents must be allowed to flow in the scope shields! Scope grounding, if desired, should be done with a separate piece of wire connected between its case and the LDS-1 case.

It is also possible to remove the X and Y deflection amplifiers and associated power supplies from a common ground tie-point and independently ground the X and Y deflection systems through the X and Y coaxial shields, thus providing a remote, common tie-point to ground at the Scope Select Card.

XY DIGITAL CARD

108103-101

3.1 Function

The XY Digital Card accepts the digital input and calculates the digital coordinate values required by the Line Generator. Two cards are used in the Line Generator: One for the X component and one for the Y component. The XY Digital Card can accept input data in either absolute or relative form. For each input the card produces (1) the absolute coordinate location for the D/A converters, and (2) the relative displacement required by the line length estimating circuit. This card also stores the previous coordinate value in a "save point" register and produces the redundant coding used by the analog circuitry. The general structure of the data paths of the XY Digital Card can best be understood by studying the Block Diagram 108101-901.

3.2 References

Logic Drawing 108103-601, XY Digital

Block Diagram 108101-901, Line Generator Functional Block Diagram

3.3 Overall Structure

The XY Digital Card has three stages or three levels of buffering which are referred to as CLOCK 1, CLOCK 2, and CLOCK 3. There are also two levels of processing; between CLOCK 1 and CLOCK 2, and between CLOCK 2 and CLOCK 3. These three stages act as a "pipeline" so that the Line Generator actually is processing three different lines at once in its digital circuitry. The logic on the Control Card (see Section 7) controls the clocking of the three stages so that data flow through the pipeline in a well-regulated manner. It should also be noted that the upper 12 bits of the input registers and the TRUE registers are found on the Most Significant XY Card.

3.4 Input Registers and the Absolute/Relative Calculation (Sheet 1)

The input register is shown at the center of Sheet 1 of the logic drawing. This register is designed to accept input in either serial or parallel form. The serial input (SIN) is unused in parallel input systems and can be tied to ground on the back panel. The serial output (SOUT) is likewise unused and is left open. SOUT is buffered to avoid external loading of the register circuits.

The control signal PARALLEL (Location 1B) must be tied high for parallel input systems, because if it is low the register will shift its input in serially. The parallel inputs to the register are named IN(1) through IN(12), where IN(1) is the most significant input. Data on the IN lines are clocked into the input register when both POKEL and CLOCK1 are high (Location 1C).

The output of the input register is named VA(1) through VA(12). This output is added to the data on the OLD lines. To understand why the switches at the bottom of Sheet 1 select OLD as they do, it is important to realize how the result of the addition (SUM) is to be used. The Line Generator requires both the absolute coordinate value for the D/A converters and the relative displacement for the line length estimator. Now, if the incoming data is relative, it must be added to the current point (which is held in the TRUE registers) to give the absolute location, while the incoming data itself provides the relative displacement. If, on the other hand, the incoming data are absolute, they provide the absolute location as they stand, and the relative displacement must be calculated by subtracting the current point value from the incoming data. The situation is further complicated by the fact that the ODD and EVEN registers are used alternately to drive the analog circuits, and, thus, the proper selection of either the TRUE ODD (TO) or TRUE EVEN (TE) register outputs must be made in order to get the proper "current point."

The switches at the bottom of Sheet 1 make the proper selection of TO or TE and, if necessary, complement the output to produce the OLD data. These switches are controlled by the signals SR, SE, and SSP (Location 1B). The truth table at the bottom of Sheet 1 shows how these three signals are coded to make the selection of OLD and what the resulting SUM will be.

The SP inputs are provided so that data from other registers within the Line Generator can be selected onto the OLD lines. The OLD signals are brought out to connectors so that the "save point" (i.e., the X, Y, and Z values in the true registers) and scope selection data can be returned to memory. If this feature is not operational, or is made redundant by the presence of a Clipping Divider in the system, the OLD lines are only used to drive indicator lights.

The adder (shown at the top of Sheet 1) uses Signetics fast carry integrated circuits. The carry chain of the adder involves the two-rail system using the outputs Cg and Cr from each circuit. When subtraction is required (to calculate the relative displacement when the input is in absolute form), the OLD data comes to the adder in one's complement form. The SR signal is routed up to the adder to effect a carry injection to correct for two's complement subtraction.

At the top left corner of the drawing is the logic to generate the correct sign of the sum or difference, to detect overflow, and to generate a carry output signal when appropriate. The gate 63.8 generates the carry output signal by combining the multiple carry outputs of the Signetics adder. (An AND-OR-Invert gate is used here because there was a spare one available.)

The two exclusive-OR gates 53.11 and 53.8 are connected as full adder. The three inputs to this adder are the carry from the previous addition stage (63.8) and a copy of the two most significant bits of the data being added. Thus this adder stage produces output as if the two inputs were sign-extended one place. The sign output is complemented by gate 53.3 (which is connected as an inverter), because the sign input to the adder was inverted by 63.8.

The overflow function is defined such that it is true whenever the sign bit as generated above fails to agree with the twelfth bit of the sum generated by the adder 54. The exclusive-OR gate 53.6 implements this function.

3.5 Selection Switches and the Delta Register (Sheet 2)

The switches shown on Sheet 2 select the appropriate data for the position coordinate location and the relative displacement. The lower row of switches is used to select the proper absolute location by selecting either the input data VA (for absolute input) or the SUM input from the adder (for relative input). The upper switch chooses between the same inputs, but chooses the opposite from that which the lower switch chooses. The switch control signals (shown at the right of the drawing) are connected such that the two rows of switches will always select opposite values.

The line length estimating logic requires the absolute (i.e., unsigned) value of the relative displacement. For this reason the logic at the left of the upper row of switches detects when the output of these switches should be complemented. The two conditions which cause the switch to select complement values are (1) when SUM data are being selected and the sign is negative (SIGN=hi), or (2) when VA data are being selected and the most significant bit of VA is 1 (indicating a negative value of the relative input). The way in which the signal sign is generated takes care of overflow in the adder for very large displacements, insuring that the absolute magnitude of the displacement is a 12-bit unsigned number.

The output of the upper row of switches is clocked into the latches shown at the top of Sheet 2, when POKEM and CLOCK2 are high (see Sheet 3). The output of this register, which contains delta X (or delta Y), is sent to the Z Digital Card on the *MAG lines for use by the line length estimator.

3.6 Redundant Coding and the Generation of CLOCK 2 and CLOCK 3 (Sheet 3)

The logic shown on the left side of Sheet 3 is intended to detect when redundant coding is necessary to make the most significant bits of the absolute coordinate locations the same. Redundant coding only takes place if the lines are short enough and if the upper bits of the coordinate values are not already the same. In the upper left corner of Sheet 3, lines short enough for the Redundant bit 4 are shown and those lines where R4 actually applies are indicated.

There are two redundant bits, R4 and R6. If R6 applies, then R4 is inhibited so that only one redundant bit can be active at a time. Gates 69.8 and 59.8 provide the definition of "short enough." These wide NAND gates test the *MAG values of the upper bits. If the MAGNITUDE values are all zero, then the line is short enough. The exclusive-OR gates 20.6 and 20.8 test to make sure that the upper bits of the coordinate values are not already the same, thus making redundant coding unnecessary.

The redundant bits produced by the logic on Sheet 3 are sent to the adders on Sheets 4 and 5 for use in recoding the data for the CODED registers. These bits are also required by the D/A converter to compensate for the redundant coding, so they are clocked into the latch 37 at clock time 3 and sent as CR(4) and CR(6).

Redundant coding comes out right even though it may be testing one's complement data (the delta register may have complemented the *MAG value). The examples on the bottom of Sheet 3 illustrate this fact. It should also be noted that the redundant coding logic is entirely on this card. Thus, the redundant codings for X and Y are entirely independent, and a line may be sent to the D/A converters with redundant coding in one component and normal coding in the other.

The logic on the right half of Sheet 3 generates the clock pulses for clock times 2 and 3. CLOCK2 is gated with the poke signals EVEN, ODD and POKEM to provide the stobe pulse for level two registers. These strobe pulses are buffered by the 7440 buffer drivers 30.6, 30.8, and 70.6. CLOCK3 is not gated, but is buffered by the buffer drivers in Position 27 to drive the Stage 3 registers.

3.7 The TRUE Registers and the CODED Registers (Sheets 4 and 5)

Sheets 4 and 5 are identical with the exception that Sheet 4 deals with the even registers, while Sheet 5 deals with the odd registers. The row of latches shown at the bottom of the drawings represent the TRUE register. This is the level 2 register which contains the absolute coordinate locations in uncoded form. It is the output of this register which is used in calculating position coordinates and relative displacements for the input values (see Section 3.4).

The adder in the middle of the drawing is set up to provide redundant coding and to correct for the location of the origin. Redundant coding is effected by subtracting either 100_8 (R6), 400_8 (R4), or 0 (if neither R4 nor R6). The most significant bit input to the adder has a ground connection rather than the power connection used for the other bits. This is to change from the addressing scheme used up until this point, where the origin is in the middle of the screen, to the addressing scheme required by the D/A converters, where the origin is in the lower left-hand corner. If the scope is to be used with lower left origin data as input, then these pins should be connected to power instead of ground.

The final output registers (CO and CE) provide digital input to the D/A converters. They are provided with a separate power supply, separately filtered, which is intended to provide very quiet power to this register. The intent is to isolate the electrical noise which might otherwise find its way into the analog signal through the drive to the D/A converter.

MOST SIGNIFICANT XY

4.1 Function

The Most Significant XY Card provides an extension for the upper 12 bits of the input register and the upper 12 bits of both the even and the odd TRUE registers. The card also contains logic to detect when the coordinate values for the endpoints extend into this upper 12-bit area and thus indicate that the line is off the scope. A single card is used for both the X and Y components.

4.1 Reference

Logic Drawing 108117-600, Most Significant XY
Section 3 of this manual

4.3 Input Registers and Selection Switches (Sheets 1 and 2)

The input registers are shown near the middle of Sheets 1 and 2 of the logic drawing. These registers operate in the same manner as those for the least significant bits (see Section 3) with the exception that the serial inputs are disabled (tied to ground).

The switches at the bottom of the Sheets 1 and 2 also operate just as those for the least significant bits and select TO, TE, SP, or their complements onto the OLD buss. The carry-ins for the adders come from the XY Digital Cards, so that the adders on the Most Significant XY Card act as extensions of the adders on the XY Digital Cards. Overflow and carry-out (left side of drawing) are also handled in the same way as on the XY Digital Cards.

The selection switch for the NEW data is also on this sheet. (Note that no magnitude data is required for the most significant 12 bits, so both the switches required to select this data and the magnitude registers are omitted.)

4.4 Generation of NON and PON (New ON and Previous ON)

In order to avoid the wrap-around problem, the Line Generator omits lines any part of which extend off the scope. This very rudimentary clipping function is provided by the set of comparator gates shown at the bottom of Sheets 3 and 4 of the logic drawings. The comparator gates (21, 31, 41, 51, 61, 71) operate with the following truth table:

Input										Output		
Number	A ₄	A ₃	A ₂	A ₁	Number	B ₄	B ₃	B ₂	B ₁	Strobe	X	Y
Pin	13	12	11	10		1	2	3	4	8	6	9
		A			>			B		0	1	0
		A			<			B		0	0	1
		A			=			B		0	1	1
		A			≠			B		1	0	0

For these comparators B is simply a copy of the most significant bit from the XY Digital Card which comes across as NEW(13). This bit provides an indication of the sign of the coordinate value. The comparators produce the signals A, B, C, D, E and F which are gated in a wide NAND gate (Position B1). All of these signals will be one only if the A value is equal to B (i.e., the line does not extend into the upper 12 bits).

The signal produced by the wide NAND gate is called *XON (*YON for the Y component). This signal is strobed into either the even or the odd second-stage register (TRUE) to become the 13th bit of these registers. These 13th bits are then used by the logic shown on Sheet 5 to produce the signal PON. PON is true, if for the selected register (odd or even) the 13th bit indicates that both the X components and the Y components were on. Similarly, NON is true, if both *XON and *YON are low.

Z DIGITAL CARD

5.1 Function

The Z Digital Card provides two functions for the Line Generator. First, it accepts the digital input of the Z component of the coordinate value (which is used to control intensity), stores this value, and provides the Z input needed by the analog circuit. Second, it takes the magnitude numbers from the XY Digital Cards, determines which is greater (X or Y), normalizes both, and if necessary interchanges them to produce two groups of signals called "SMALLER" and "LARGER."

5.2 Reference

Logic Drawing 108104-601, Z Digital Card

Block Diagram 108101-901, Line Generator Functional Block Diagram

5.3 The Z Component

The logic shown on Sheets 1 and 2 of the logic drawing handles the Z component with the same 3 levels of registers that are provided for the X and Y components on the XY Digital Card. The input register is shown in Position B on Sheet 1. It should be noted that only 8 bits of input are provided for Z. Because of pin limitations the parallel/serial operation of the input register is controlled by jumpers. For parallel operation Pin 45.9 should be jumpered to ground. If serial input is called for, 45.9 is jumpered to power and IN(8) becomes SIN (serial in), while IN(1) is jumpered to the most significant bit output and becomes SOUT.

The switch at the bottom of Sheet 1 simply selects between the output of the even or odd TRUE register for the OLD buss. OLD is added to the contents of the input register by the adder in Location C. The switch at the top of the sheet selects the output of the adder if SR (select relative) is high and otherwise selects the VA buss from the input register.

The odd and the even registers for both Stage 2 and Stage 3 are shown on Sheet 2. Since there is no redundant coding involved for Z, no processing is necessary between the Stage 2 (TRUE) and Stage 3 (CODED) registers. (Note that because the use of the even and odd registers alternates, double buffering is not required and simple latches suffice for these registers.)

The slightly peculiar drive arrangement for the clock signals at the top of Sheet 2 comes about because of loading conventions and the vagaries of laying out the printed circuit board. Logically, the entire upper register is loaded at once.

5.4 Magnitude Comparison

The magnitude numbers generated by the XY Digital Cards are fed to the comparison gates shown on Sheet 3. The comparator integrated circuit used has the following truth table:

Input										Output		
Number	A ₄	A ₃	A ₂	A ₁	Number	B ₄	B ₃	B ₂	B ₁	Strobe	X	Y
Pin	13	12	11	10		1	2	3	4	8	6	9
		A			>			B		0	1	0
		A			<			B		0	0	1
		A			=			B		0	1	1
		A			≥ =			B		1	0	0

The outputs of the lower level of comparator gates feed the upper comparator gate which generates the signal MYGTMX (Magnitude of Y Greater Than the Magnitude of X). This signal is used to interchange X and Y (Sheet 5) and is tied to an output connector to drive an indicator light.

5.5 Normalization

The analog circuitry requires normalized magnitude numbers and a line length exponent. The logic on Sheet 4 determines how many places to shift the magnitude numbers by counting the leading zeros. The magnitude numbers are normalized such that the larger will have a one in the most significant bit.

Very wide gates are used to determine the amount of shift required. There is a great deal of redundancy in the logic to provide very fast selection of the normalization factor. The row of NAND gates at the bottom of the drawing combine zeros for X and Y. Since the magnitude signals (*MAG(1-12)) are inverted, any stage with both X and Y zero will cause the output of the corresponding NAND gate to be low. After inversion, the signals on the horizontal lines (Location B) are high, if the corresponding stages had zeros for both X and Y. The row of NAND gates in Location B determine if a non-zero value has been detected for a particular stage and if all preceding stages had zero values. The signals *S4M, *S8M, and *S9M (Shift 4 or More, etc.) are not conditioned by the actual detection of a non-zero bit, but only by the preceding stages.

The resulting signals are used to form two 3-bit binary shift numbers (MSN(1-3), SN(1-3) where (3) is the least significant bit). These two numbers are used to drive the shift registers on Sheet 5. (Note that these two numbers should always add to 8 (1000 binary).)

At the right edge of the drawing the actual lengths of lines that would be produced for various shift constants are shown (assuming a maximum deflection of 10 inches, i.e., a screen 10 inches square). The lines are magnified on this picture, but the width-to-length ratio is correct. Notice that the lines for S7, S8, and S9 are really very short.

The actual shifting is performed by the shift registers shown on Sheet 5. These registers operate in pairs; one shifting one direction and the other in the other direction. The output goes onto an open collector buss, so that the result is an 8-bit shifted number. The switches at the top of Sheet 5 exchange X and Y, if MYGTMX (magnitude of Y greater than the magnitude of X) is high.

5.6 Move Commands and the Line Length Exponent

When a move command is executed, the ramp generator may go faster than when a draw is executed. To increase the speed of the ramp generator for move commands, the switch on Sheet 6 transports some of the unary coded normalization constants to the right two places, thus making the ramp think that the "line" is shorter than the actual move command is. The transport of unary coded bits is not accomplished fully, because only a few of the bits are relevant. NAND gates 22.11 and 23.8 generate the C6M signal.

The latches above all this logic form the stage 3 register for the line length exponent. The shift signals CO - C9M can properly be thought of as the exponent of the line length, a unary-coded exponent. The Line Generator will combine the value of this exponent with a line length mantissa derived by analog circuits to provide the proper line length estimate for the line.

The gates and drivers at the right of Sheet 6 provide the clock signals for the various registers involved on the Z Digital Card. Notice that CLOCK2 is gated by the ODD and EVEN signals to control which of the two registers is poked.

5.7 The "LARGER" and "SMALLER" Numbers

The X and Y magnitude numbers, after they have been normalized and possibly exchanged are clocked into stage three registers. The outputs of these registers are named LARGER and SMALLER (LA and SM) and are sent to the analog line-length estimating circuit on the Ramp Card.

MOST SIGNIFICANT Z

6.1 Function

The Most Significant Z Card contains the upper 12 bits of the Stage 1 (input) and Stage 2 (TRUE) registers for the Z component. This card also contains logic to omit lines whose Z value is too large (i.e., extends into the upper 12 bits), or whose Z value is negative.

6.2 Reference

Logic Drawing 108118-600, Most Significant Z

Section 4 of this manual

6.3 Extension for the Z Component

The extensions of the Z component input register, the selection switches for OLD, the adder to compute relative displacements, and the selection switches for NEW are all shown on Sheet 2 of the logic drawing. These elements of the logic behave exactly like their counterparts on the Z Digital Card. Overflow and carry-out are handled in the same manner as on the XY Digital Card (see Section 3.3).

Unfortunately, the pin limitations of the Z Digital Card prohibited the possibility of using the carry-out signal for the least significant bits as a carry-in for the extension of the adder. To remedy this situation, a copy of the input register logic for the least significant 8 bits is included on the Most Significant Z Card. This logic is shown on Sheet 1. The only signals of this logic that are used are the carry-out signals CA and CB.

The extensions for the odd and even TRUE registers are found on Sheet 3.

6.4 Generation of NON and PON

The elimination of lines whose Z values extend out of bounds is handled in the same manner as that for X and Y (see Section 4.4). Comparator gates are used to determine if the value on the NEW lines is equal to ZTYPE. The output of the comparators is fed to a wide NAND gate which generates *ZON. *ZON is inverted (Sheet 1) to become NON. At the time of clock pulse 2, *ZON is clocked into either the even or the odd TRUE register as TO(13) or TE(13). One of these output signals is selected (again on Sheet 1) to become PON.

CONTROL CARD

7.1 Function

The Control Card serves two basic functions for the Line Generator. First, it provides the 4-clock pulses for the four levels of processing in the Line Generator. Second, it stores and interprets the commands which the Line Generator receives. The Control Card also handles synchronization with external devices through standard flag/acknowledge pairs.

7.2 Reference

Logic Drawing 108109-604 Line Generator Control

7.3 The Four Clocks

The Line Generator processes data as it flows through a "pipeline" of registers. This pipeline processing makes control very simple and speeds up the processing for the Line Generator so that it is considerably faster than it would be with sequential processing and fewer registers. The throughput rate of the Line Generator's digital logic is extremely high, since each step takes only about 250 nanoseconds to perform.

The four stages in the processing pipeline are controlled by four separate clocks. Each clock will fire, when the conditions for that stage have been satisfied. The four clocks are connected in a standard pipeline chain with a flag/acknowledge pair between each clocking circuit and the next. If the data for the Line Generator are provided slowly, then the processing stages will spend most of their time in "wait" states, and the processing of each line will be sequential. If, on the other hand, data are provided faster than the lines can be drawn on the screen, the pipeline will fill up with partially processed data, and each stage can process the next datum only when the next stage relieves it of its present data. Thus, in the "choked-up" condition the four clock pulses seem to come in reverse order (e.g., immediately after CLOCK3, CLOCK2 is able to process another piece of data which, in turn, permits CLOCK1 to fire).

7.4 The Basic Clock Model (CLOCK3)

The basic clock circuit is best understood by studying Sheet 3 of the logic drawings. The basic clock circuit consists of three parts, each of which contains a flip-flop composed on NAND gates. The three parts include:

- (1) Condition detection, gates 44.3, 44.6, and 56.12
- (2) Clock generation, gates 59.8, 58.6, and delay 49

(3) Outflag generation, gates 56.8, 58.8, and 58.11

The NAND gate 56.12 detects when all the conditions are met for generating the clock pulse. The conditions which must be satisfied are:

- (1) Incoming flag (FL2 56.1) which indicates that the previous stage has just clocked so that new data are available.
- (2) Single step (see Section 7.9 for a description of the single step logic which is located on the drawings in Position B4 and provides an input at 56.2).
- (3) WAIT3 which is itself a composite signal composed of:
 - (3a) *AKG3 (45.1) which indicates that the acknowledge for the previous incoming flag (and thus the flag itself) has gone away.
 - (3b) The acknowledge signal from the next stage has been removed (here called ANALOG WAIT, 45.2, but on the other clock circuits referred to as *AKGn).
 - (3c) The outgoing flag has been lowered in response to an acknowledge signal (45.4).
 - (3d) The clock itself is over (45.5).

When the conditions are satisfied, the output at 56.12 goes low, which sets the flip-flop composed of the gates 58.6 and 59.8, thus initiating the clock signal. When the flip-flop is set 59.8 goes low, 45.5 is pulled low, and the WAIT3 condition is destroyed. Thus, the clock initiating signal at 56.12 is of short duration and is only long enough to toggle the clock flip-flop. The signal is, however, guaranteed to be long enough to toggle the flip-flop, because it is only turned off as a result of successful toggling.

When the clock flip-flop is set, the monostable multivibrator (delay) in Position 49 is triggered and Pin 49.6 goes low for the specified period of the clock pulse (in this case 500 nsec). The output pin going low sets the output flip-flop composed of the gates 58.8 and 56.8 which pulls test point L low. Since 45.4 is also pulled low, further clock pulses are prohibited. The output flip-flop also clears the clock flip-flop by pulling 59.10 low, thus ending the clock pulse. The time duration of the clock pulse is determined by the setup delay of the multivibrator 49 and the gate delays of 56.8 and 58.8. If a wider clock pulse is required, additional delay should be inserted between *CL3 and the input to the multivibrator 49.

The clock pulse also sets the acknowledge flip-flop 44.3, 44.6 which signals the previous unit that its flag has been acknowledged (i.e., that a clock signal has indeed been generated). The acknowledge signal will clear the outflag flip-flop of the previous stage, so that the flag signal goes low. This, in turn, clears the acknowledge flip-flop (44.5). The acknowledge flip-flop must be cleared before the condition WAIT3 is satisfied again (45.1). The *AKG signal is an inverted version of 44.3 rather than the signal 44.6 in order to assure that the flip-flop has been properly cleared before the acknowledge signal is removed.

When the delay multivibrator 49 times out, and 49.6 again becomes high, the output flag for this stage is raised. In order for the outflag to be generated, the signal on 49.6 must be high and the output flip-flop must be set (58.12). When the next unit acknowledges the flag, the acknowledge signal (here called ANALOG WAIT) clears the output flip-flop, thus lowering the outflag. The ANALOG WAIT signal also takes over the responsibility of inhibiting further clocking (45.2), until the acknowledge has been removed in response to the lowering of the outflag. When the acknowledge signal goes away (ANALOG WAIT becomes high), the condition WAIT 3 is again satisfied, and the clock circuit returns to a wait state.

Throughout the design of the clock circuits the principle of causality has been implemented. That is, a signal takes over responsibility for inhibiting further clock pulses, and then clears the previous reason for not generating the clock. Assuming that the gate delays are at least as long as the signal transition times, this design guarantees that there will be no transient spikes on the WAIT3 signal which might otherwise generate false clock pulses.

7.5 CLOCK 1 (Sheet 1)

The other clock circuits operate almost identically to the simple model provided by CLOCK 3. The only difference is that additional signals are gated into these circuits to effect special control as required by each particular stage. The CLOCK 1 circuit differs from the CLOCK 3 circuit in the following details:

- (1) The input flag is not recognized, unless the signal ME is present.
- (2) Raising the outflag may be inhibited by *MORE.
- (3) The "no overlap" conditions must be satisfied in order for the clock to be generated.
- (4) The clock flip-flop is cleared directly by the output of the delay multivibrator.

The signal ME indicates that the Line Generator has recognized that the incoming data are intended for it. ME is generated on Sheet 5 by decoding the command lines. ME is gated into 57.1 and 57.2, so that INFLG is not recognized unless ME is high.

The output flip-flop (77.11 and 78.8) can be forced clear by the signal *MORE. *MORE also inhibits the outflag (75.9). The *MORE signal means that additional CLOCK 1 pulses are necessary to get all of the incoming data into the registers (e.g., in 3D). As long as *MORE is low, additional CLOCK 1 pulses will be generated without generating any CLOCK 2 pulses.

When the system is in "no overlap" mode, lines are processed sequentially rather than in a pipeline fashion (i.e., each unit of the pipeline waits until the last line has been completely processed before beginning processing on the next line. In "no overlap" mode the Line Generator waits until all of the processing stages (clock circuits) are in the wait state, before it issues another CLOCK 1 pulse. This is done by ANDing all of the respective WAIT signals from the four stages (72.6). If no overlap is specified (either by the system through the cable input or by the control panel switch of the Line Generator - see Location D3), all of the WAIT signals must be high before another CLOCK 1 pulse can be generated.

Because the signal *MORE inhibits the setting of the output flip-flop in some cases, it is not possible to use the output of the flip-flop (78.8) to clear the clock flip-flop, as is done in the case of CLOCK 3. Instead, the clock flip-flop is cleared directly by the output of the delay multivibrator. Because of this, the output of the multivibrator is also gated into gate 19.8 to prevent false signals on INPUT WAIT.

7.6 CLOCK 2 (Sheet 2)

The CLOCK 2 logic is identical to the CLOCK 3 model, with the exception of some logic required in output-to-memory operations and logic to generate an additional CLOCK 2 pulse for "dot" and "draw from" operations.

The signal *MOVE STEP (see Section 7.10) causes the CLOCK 2 circuit to produce two clock pulses. At 62.12, *MOVE STEP inhibits the setting of the scknowledge flip-flop, so that the input flag is not lowered. *MOVE STEP also forces a second clock pulse (at 67.2) after the first one has been completed, and WAIT 2 is again high. Following each of these CLOCK 2 pulses, pipeline processing of the data through Stages 3 and 4 continues. The control logic for *MOVE STEP is such that the signal goes high again after the first clock pulse, so that only two clock pulses are generated.

CLOCK 2 contains two outflag circuits. The first is used in the normal manner to signal the next stage of the Line Generator, and the second is used for fetching information from the Line Generator into memory. These two flags are controlled

by the signals DOS (Do Output to Scope) and DOM (Do Output to Memory) which are generated by the control logic (see 7.10). The WAIT 2 condition must detect when both output circuits have completed their operations before it goes high (63.8).

The additional flip-flop and delay associated with the second output circuit provides a "post fetch delay" to allow time for the gates controlled during the output to memory to return to their normal internal uses before another CLOCK 2 pulse can be generated. The flip-flop 55.8, 65.8, and the delay 53 operate in the same way that the standard clock flip-flop and delay do. The flip-flop gets set when the flag acknowledge (OUTAKG) is received. The delay is fired after the flip-flop has been set (53.4) and the acknowledge signal is removed (53.3). As soon as the delay fires, it takes over the job of inhibiting a further clock (63.2) and clears the flip-flop.

The CLOCK 2 system is declared to be in the "output" state, whenever the output to memory flag is to be raised. The output state line is generated by the logic shown in Position B2 on the drawing. OUTPUT and *OUTPUT are used by the control logic to condition the gates that deliver the output data to go with the output flag.

7.7 CLOCK 4 (Sheet 4)

The CLOCK 4 logic controls the time at which the Ramp Card begins to generate the ramp. Because of this, its output stages are different from the other clock circuits. Instead of raising an output flag, the CLOCK 4 logic clocks the flip-flop which generates the UP and DOWN signals which are sent to the Ramp Card. As soon as the flip-flop (48.6) changes state, the RAMPING signal (Location B-C1) comes on, indicating that the ramp is underway. When the Ramp Card has completed the ramp, so that the ramp output agrees with the UP or DOWN command, the signal AGT1 or ALTO comes on to end the RAMPING signal. Since the cross-over detectors that generate AGT1 and ALTO may switch several times before reaching a crisp decision, the "bounce kill delay" 37 is used to produce a cleanly changing output signal. The bounce kill delay should be set as short as possible, but should be longer than the maximum expected duration of the bounces. The signal ANALOG WAIT (Location B2) indicates that the Ramp Card is in a waiting state and is ready to be used again.

The delay called "first short line delay" is used to extend the duration of the clock pulse if additional settling time is required by the D/A converters. This extra delay is required for the first short line after a sequence of long ones, or whenever the redundant bit is inserted or deleted in such a way as to require recoding of the most significant bits of the D/A converters. These two conditions are reflected in the signal *DELAY REQUIRED. If the delay is required, the clock flip-flop (50.8, 51.3) is not cleared until the multivibrator times out.

If the delay is not required, the clock flip-flop is cleared as soon as the delay is initiated.

The circuitry at Location C3 is provided to permit a sweep to be synchronized with an external video pulse. If activated by a low signal on DISABLE SYNC, this sync pulse circuit will hold up completion of the CLOCK 4 pulse until the arrival of the sync pulse. Normally, the DISABLE SYNC signal is wired high or left open so that this circuitry has no effect.

7.8 The Odd-Even Logic Chain (Sheet 4)

The chain of flip-flops which controls the odd-even functions of the Line Generator is shown at the top of Sheet 4. The first of these flip-flops produces the signals ODD and EVEN which indicate which of the stage two registers is to be used. This flip-flop feeds itself, so that every time it is clocked it complements, thus the use of the odd and even registers alternates. The CLOCK 3 pulse will copy the outputs of the first flip-flop into a second flip-flop which generates the signals Codd and CEVEN which indicate that the ODD or EVEN side, respectively, has just been loaded. The CLOCK 4 signal copies this odd and even information into the UP and DOWN signals which are sent to the Ramp Card to control the direction of the ramp. The timing diagram at the bottom of Sheet 4 indicates the sequence of these events.

7.9 Single Step and Master Clear (Sheet 1)

The flip-flop 74.11, 75.12 controls the single step logic which can be used to inhibit clock pulses, if the signal *SINGLE STEP (controlled by a panel switch) is low. If *SINGLE STEP is low, clock pulses will be prohibited until the "continue" button is first pushed (to clear the flip-flop which has been set by the last clock pulse) and then released (to enable the clock pulse via 74.9). As soon as the clock pulse occurs again, the flip-flop is again set and further clock pulses are inhibited until the continue button is again pushed and released.

Because there is a single step flip-flop associated with each of the clock circuits, each stage of the pipeline will fire when the continue button is pressed, thus processing a single line completely. If the "no overlap" condition is also present (Location D3), then the composite clock signal generated by ORing the clocks from each stage (72.8) is enabled at gate 71.6, so that the single step flip-flop gets cleared by any clock pulse, so that only one stage of processing occurs with any push of the continue button. The composite clock is brought out to a connector so that it can be checked on an oscilloscope.

MASTER CLEAR (a cable input signal) and *RESET (a control panel push button) are ORed together by the gate 71.8 to provide

the internal reset signal called *RST. *RST initializes all of the flip-flops in the control, so that processing will begin correctly.

7.10 Command Logic (Sheets 5 and 6)

The logic for detecting that the incoming command is intended for the Line Generator is shown at the bottom of Sheet 5. This logic develops the signal ME (which is used to gate the input flag for Stage 1) and *ICU which is put on to an open collector buss to indicate to the system that the Line Generator has recognized that the command was intended for it.

The row of latches at the bottom of Sheet 5 is used to capture the incoming directive at CLOCK 1 time. The command is then decoded to develop the control signals needed for getting the correct data into the State 2 registers.

The command decoded 29 provides for selection of the various kind of drawing instructions and the logic associated with the output of the decoder develops the appropriate control signals for the respective types of drawing instructions. The signal CSET, indicating a "setpoint" operation, can be generated not only by setpoint instructions themselves, but also by load instructions or when the line extends off the screen (as indicated by NONXY, PONXY, NONZ, and PONZ).

Some of the partially decoded command signals are clocked into another set of registers at CLOCK 2 time (see bottom of Sheet 6). The logic in Position C4 is used to generate the *MOVE STEP signal which causes a second CLOCK 2 pulse. The CDOUBLE controls this logic and indicates that either a "dot" or a "line from" operation is called for. After the first CLOCK 2 pulse CDOUBLE complements the flip-flop 22.14, so that the *MOVE STEP signal again goes high. The *TFLINE and *TDOT signals generated indicate that the additional motion is being provided to generate a "from line" or a "dot."

The latches at the top of the sheet capture the actual move, draw, and timed sweep commands at CLOCK 3 for use by the Ramp Card.

RAMP CARD

8.1 Function

The purpose of the Ramp Card is to generate the basic ramps and the reference voltages needed by the Line Generator. The ramp is produced by an integrator, whose integration rate is controlled by the length of the line to make the drawing rate constant for all lines. To insure accuracy in end-point positioning the ramp is run from slightly less than zero to slightly more than one. The indication that the ramp is within the active range is provided by timing signals which are produced by a cross-over detector.

8.2 Reference

Logic Drawing 108108-600 Ramp Card

8.3 Line Length Estimation (Sheet 1)

The speed of the ramp is controlled by the line length. The circuits shown on Sheet 1 of the logic drawings are designed to provide an estimate of the length of the line being drawn. The input for this logic are the "larger" (LA(n)) and "smaller" (SM(n)) digital numbers from the Z Digital Card (see Section 5), and the outputs are positive and negative reciprocals of the line length estimate.

8.3.1 D/A Converters (Sheet 1, Right Side)

The Ramp Card is provided with digital inputs called SM(0-7) and LA(0-7). These inputs represent the normalized magnitude of the X and Y displacements for the line. These numbers can always be treated as positive (or zero). If we consider the binary point to follow the most significant bit of input, SM(0) or LA(0), then the numbers will always lie in the following ranges:

$$0 \leq \text{smaller} \leq \text{larger}$$

$$1 \leq \text{larger} < 2$$

The larger number always lies between one and two, because of the normalization process. We could also think of the larger number as being between one-half and one, but it is simpler to think of the shortest normalized line as being one unit long.

The two inputs LA(0-7) and SM(0-7) are converted to analog voltages. Because LA is guaranteed to lie between one and two, its most significant bit, LA(0), will always be one. Therefore, the digital-to-analog converter for the larger difference number ignores this input (see Location B1 on Sheet 1). The fixed bias input provided by the 8.06K and 39 ohm resistors from -15 volt supply compensates for this omission to bias the output voltage from the converter in the proper direction.

The smaller number, SM(0-7), is also converted to an analog signal. Since the maximum current controlling the "smaller" number is less than 1/2 the larger current, the SM(7) bit is ignored.

The D/A converters are relatively straightforward diode types. Open-collector microcircuit inverters either absorb the resistor currents or permit them to flow through the diodes into the operational amplifier input. This converter works, because the saturation output voltage of the inverter is less than the conduction voltage of the diode.

Each digital-to-analog converter is followed by an operational amplifier (see Location B2 and C2). The feedback networks around these amplifiers are computed to provide for the correct range for the output voltages. In particular:

$$0 \leq V_L \leq +10$$
$$-10 \leq V_S \leq +10$$

as shown on the print. Actually, because of the nature of the digital inputs, V_S will never be more positive than V_L . These two output voltages are available at test points D and E. The operational amplifiers are provided with a 500 ohm trim resistor to approximately compensate their input offset voltages. This fixed, low precision resistor is used because only moderate accuracy is required.

8.3.2 Line Length Approximation (Sheet 1, Center)

The correct length of a line is given by:

$$L = \sqrt{\Delta X^2 + \Delta Y^2}$$

but since that is too difficult a function to generate on this card, an approximation must be used. One popular method is to estimate the line length by taking the larger displacement plus 1/3 of the smaller, or the larger plus 1/2 of the smaller. The errors in these methods are shown approximately in the graph at Location A4 on the drawing. We have discovered empirically that the function:

$$L = \left| \text{larger} \right| + \left| 0.15 \cdot \right| \left| \text{smaller} \right|$$

provides a very close estimate, if the smaller length is quite small. For lines having a larger/smaller displacement ratio less than 1:0.38, the function:

$$L = 0.848 \cdot \text{larger} + 0.55 \cdot \text{smaller}$$

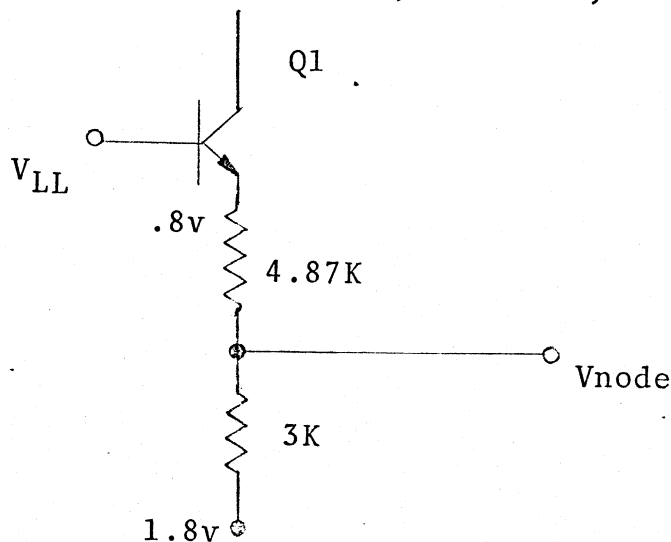
provides a very close estimate of the length. The line length correction circuit implements this two-part function. The total line length estimate is given by:

$$L = \text{larger} + 0.15 \cdot \text{smaller} + [0.4 \cdot (\text{smaller} - 0.38 \cdot \text{larger})]$$

where the expression in brackets applies only if it is positive. The approximate error curve for this function is shown on the bottom graph at Location A4.

Operation of the line correction circuit is best understood by considering some equivalent circuits. The output of the "larger" digital-to-analog converter (V_L) drives a follower transistor at Location C2 on the drawing. This follower drives a network of four resistors.

Consider first the properties of the resistor network if it were connected to neither transistor. The node point would assume a voltage of -10.8 volts. The resistor pair 4.12K connected to the analog ground and 10.7K connected to the -15 volt supply with an impedance of 3.0K. Now, consider what happens if only the follower is connected. The voltage at the node will be produced by voltage-divider action between the 4.87K resistor and the equivalent 3.00K resistor of the supply. Since a zero-length of line corresponds to $V_L = -10$ and $V_S = -10$, the following equations are references to -10 volts. Thus $V_{LL} = V_L + 10$, $V_{SS} = V_S + 10$. The equivalent circuit, thus far, looks like:



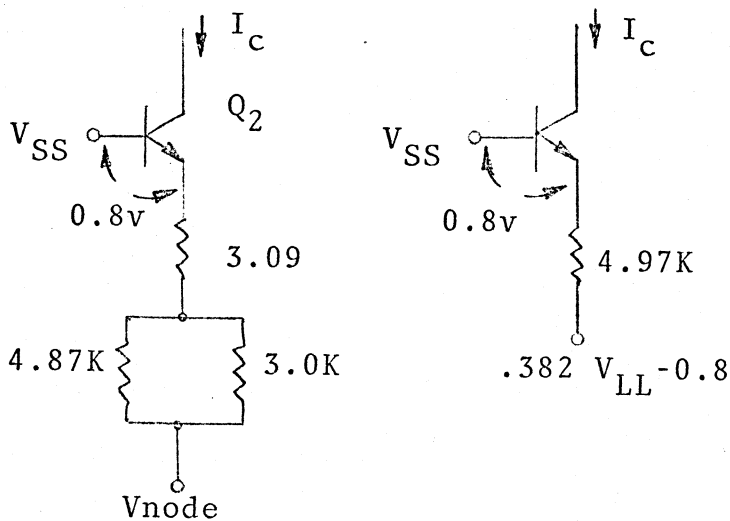
ALL VOLTAGES REFERENCED TO -10V

and the equation for Vnode (referred to -10 volts) is:

$$V_{node} = (V_{LL} - 0.8) - (-0.8V) \times \frac{3K}{3K + 4.87K} - 0.8V$$

$$= .382 V_{LL} - 0.8V$$

The equivalent circuit for computing I_C becomes:



ALL VOLTAGES REFERENCED TO -10V

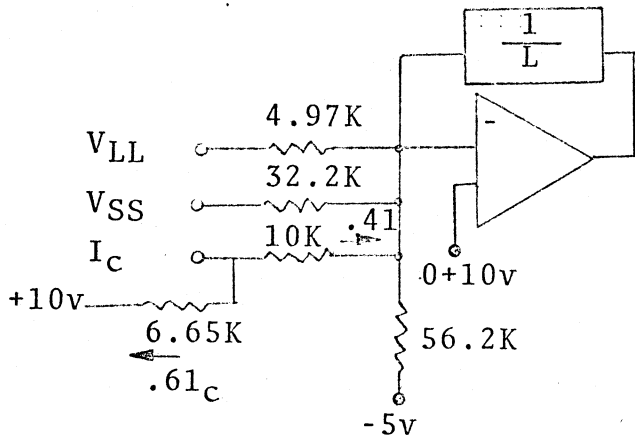
$$I_C = \frac{[(V_{SS} - 0.8) - (.382 V_{LL} - 0.8)]}{4.97K}$$

Note that I_C can only be a zero or positive current, never negative.

The current I_C is reversed by the transistor Q_3 circuit and $0.4 \times I_C$ is applied to the summing junction of the operational amplifier in the reciprocal circuit.

8.3.3 The Summing Junction (Sheet 1, Left Center)

An equivalent circuit for the summing junction of the reciprocal circuit can be shown to be:



ALL VOLTAGES REFERENCED TO -10V

The summing junction of the reciprocal circuits provides addition of the currents as follows:

$$I_{SUM} = \frac{V_{LL}}{4.99K} + \frac{V_{SS}}{33.2K} + \frac{0.4(V_{SS} - 0.382V_{LL})}{4.97K} - \frac{10}{4.99K} - \frac{10}{33.2K} - \frac{(10+5)}{56.2K}$$

The two terms before the last term must be added to account for the difference between the zero voltage connection of the "+" input of the operational amplifier and our -10 volt reference system. The last term represents a bias added to provide a 15 volt output (referred to -10 volts) from the reciprocal circuit, when the line length is at a minimum of "unity." Representative currents and voltages for several input conditions are shown in table (following page).

8.3.4 Reciprocal Circuit (Sheet 1, Left Center)

The reciprocal circuit consists of an operational amplifier with a non-linear feedback network. The non-linear network of diodes and resistors shown above the operational amplifier has been computed to provide an output voltage that is proportional to the reciprocal of the input current over the range of values desired. When the line length estimate corresponds to 2.828 (the longest possible estimate), the reciprocal output is -7.9 volts. When the line length estimate corresponds to 1.000 (the shortest possible estimate), the reciprocal output is +0.500 volts. The curve between the two outputs is sketched on Sheet 2 at Location D3.

The reciprocal of the line length is always a positive number, but since the reciprocal output is offset from zero to provide a wider range of output voltages, negative output voltages are provided. The voltage outputs are shown in the table on page 8.7.

CURRENT INTO SUMMING JUNCTION OF RECIPROCAL GENERATOR

Line Length	V_L	V_S	V_{LL}	V_{SS}	$\left[\frac{V_{LL}}{4.99K} + \frac{V_{SS}}{33.2K} + \left(.4 \frac{V_{SS} - .382 V_{LL}}{4.97K} \right)^* \right]$	-2.57ma	$= \text{Isum (ma)}$	Relative Current $\left(\frac{\text{Isum}}{2} = \frac{2.52}{2} \right)$
0 (not used)	-10V	-10V	0	0	0 + 0 + (0)*	-2.57	= -2.75	0
1	0V	-10V	10	0	2 + 0 + (0)*	-2.57	= - .57	1
1.414	0V	0V	10	10	2 + .303 + $\frac{.4 (10 - 3.82)}{4.97}$	-2.57	= .23	1.4
2	10V	0V	20	0	4 + 0 + (0)*	-2.57	= 1.43	2
2.828	10V	10V	20	20	4 + .606 + $\frac{.4 (20 - 7.64)}{4.97}$	-2.57	= 3.027	2.8

OUTPUT FROM RECIPROCAL GENERATOR AND $\pm \frac{1}{L}$ CIRCUITS

LINE LENGTH	ISUM (MA)	RECIPROCAL $\frac{1}{L}$ Gen. Output (Volts-Ref to 0)	$+\frac{1}{L}$ (volts)	$-\frac{1}{L}$ (volts)
0 (not used)		α		
1	-.57 ma	+5	+5	-5
1,414	.23 ma	-0.86	+3.55	-3.55
2	1.43 ma	-5	+2.5	=2.5
2,828	3.027 ma	-7.9	+1.77	-1.77
α (not used)		-15	0	0

*Note: Positive values used only

The reciprocal range of 0 to 1 is represented by a voltage range from -15 volts to +5 volts. The portion of this range more negative than -7.93 is never used, because it is below the minimum value of reciprocal required. The actual computed break points for this circuit are shown in the Reciprocal Function Generator figure on the next page.

8.3.5 Output (Sheet 1, Left Side)

The reciprocated voltage output represents one line length estimate with an offset of 10 volts. This output voltage must be turned into two output signals:

$$+ \left[\frac{1}{L} \right]; \text{ and } - \left[\frac{1}{L} \right]$$

by the output section shown on Sheet 1, (Location 4B and C).

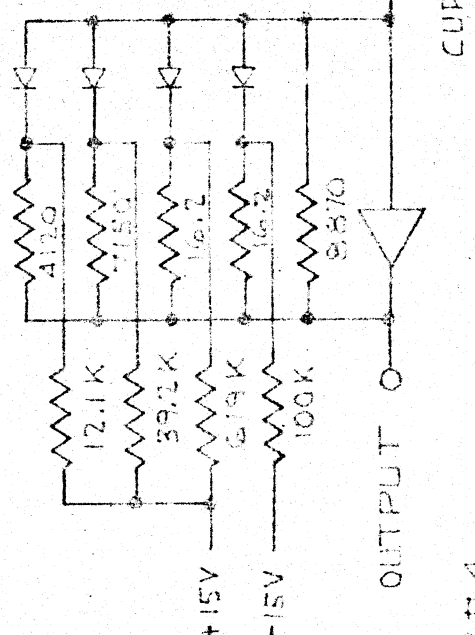
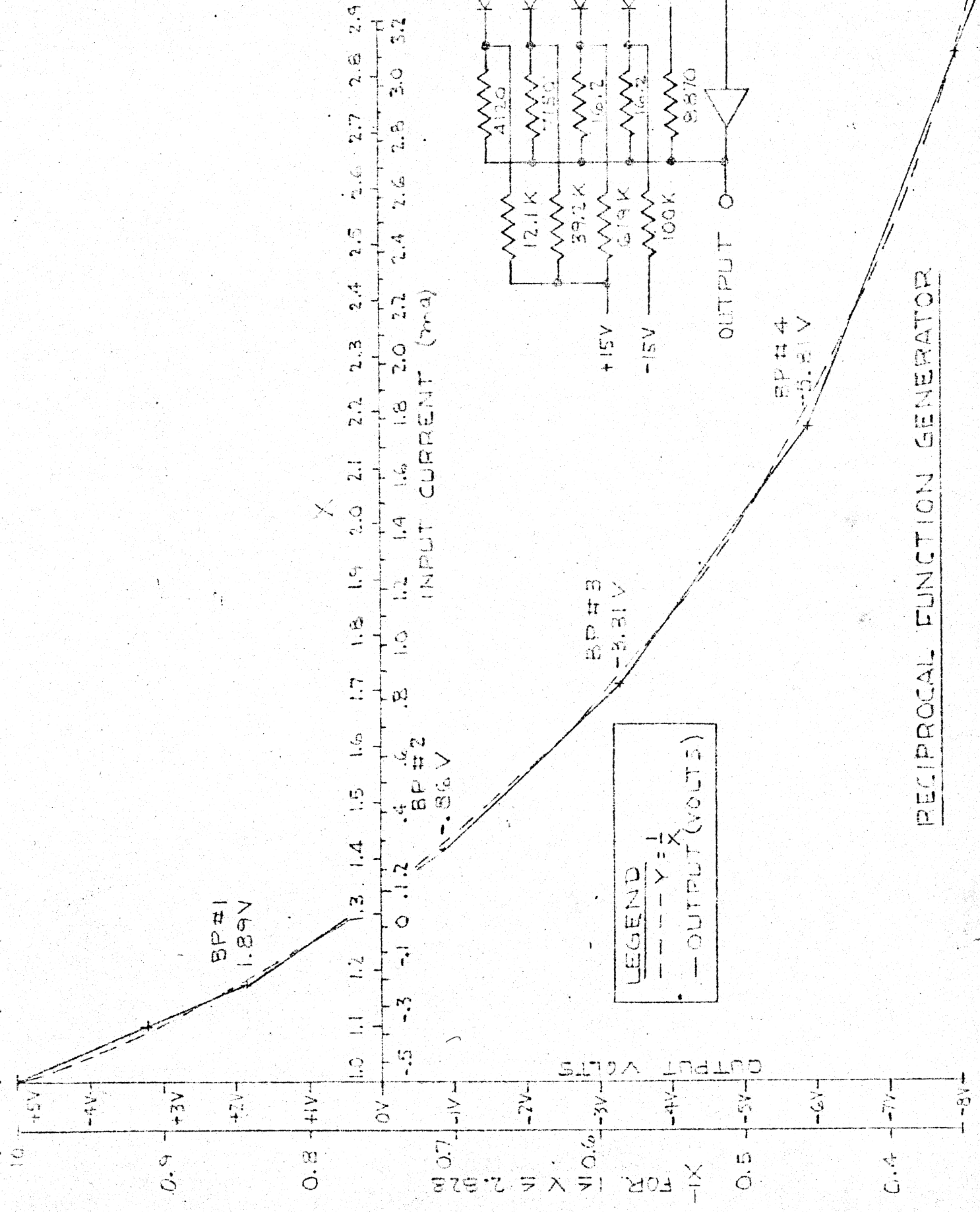
The output section consists of two operational amplifiers. The upper one is connected in a follower configuration with an input divider (2.49K and 7.50K) which provides both for the decrease in magnitude of the signal desired and correction for the offset voltage at the output of the reciprocal circuit. These two resistors have been computed for a positive reference voltage of 5.0 volts. For a line of infinite length, the reciprocal output would be -15 volts, which with this divider network would give a final output of 0 volts. With a line of length "one," the reciprocal output will be +5 volts which gives a final output of +5 volts.

The lower output amplifier is connected in an inversion circuit. The 10K and 2.49K resistors provide for the same change of scale as applied in the follower. The 3.32K resistor to the plus reference supply provides for the required offset. These resistors are computed in such a way that the positive output and negative outputs at the left of Sheet 1 should be exactly the inverse of each other.

Actually, two kinds of reciprocal line length estimates may be selected. The switches (Location B3, Sheet 1) just below the reciprocal circuit can connect the output amplifiers either to the reciprocal output or to the minus reference supply. The MM8800 drivers for the switches are connected through an appropriate resistor and diode network to select either output. If the minus reference supply is selected as the line length estimate, standard voltages will appear at the

$$+ \left[-\frac{1}{L} \right] \text{ and } - \left[\frac{1}{L} \right]$$

outputs. These standard voltages will provide for a constant integration rate. If the reference supply changes voltage, the integration rate provided by this connection will also change. The number of volts of integrated output required for a complete



BP # 4
-5.81V

BP # 3
-3.31V

BP # 2
-3.86V

BP # 1
1.89V

LEGEND
 --- Y = 1/X
 — OUTPUT (VOLTS)

RECIPROCAL FUNCTION GENERATOR

line will, however, also change. (See section on Integrator). These two changes will exactly cancel, so that the time for a sweep using the minus reference input should be exactly constant. This "timed sweep" is intended for presentation of radar data on the scope.

8.4 Ramp Generation (Sheet 2)

Sheet 2 contains the logic for the integration networks for the ramp, the inversion network for the $1-\alpha$ ramp and +REF, and the crossover detectors which determine when the ramp is in the active range. The general flow of this sheet is from left to right.

8.4.1 Integration Section

At the left of the Integration section are two switches which select either

$$+ \left[\frac{1}{L} \right] \text{ or } - \left[\frac{1}{L} \right]$$

signals as input to the integrator. These switches use the MM8800 driver which provides a 30-volt swing at this output. For example, when the terminal labeled *DOWN is high, the output of its MM8800 will be low or -14 volts. Under these circumstances, the diode in the output line will conduct, so that the gate of the field effect switch will be at -13.4 volts and the switch will be off. When the terminal labeled *DOWN is low, the output of the MM8800 will be high, that is to say +15 volts, in which case the diode will be open circuit and the field effect switch will conduct.

The positive or negative selected input is fed into a resistor chain. The impedance of this chain is controlled by the seven field-effect transistors. The impedance of the chain can be varied by the factors of 2 in order to change the total current flowing into the integrating amplifier. If all of the field-effect devices are open, an extra 150K resistor and 20K pot are switched into the circuit to provide for varying the sweep length in the "timed sweep" mode. The final field-effect device is switched by the same signal which selects the minus reference input to the length estimators.

The field-effect switches work exactly as described above. A 1.5K pull-up resistor to +15 volts (Location C3) is provided to compensate partly for the currents required by the MM8800. The MM8800 inputs, *C1, *C2, etc., are driven by the digital logic in such a way that the conducting FET nearest the integrating amplifier solely controls the speed of integration.

The integrating amplifier (Location D2) is an extra-high precision, extra-fast operational amplifier. The integration

rate can be changed by changing the value of the 560 pf capacitor connected across this amplifier. Very slow rates can be provided by using very large capacitors. Integration limits are provided by the two transistors immediately below the integrating amplifier. These two transistors conduct, when the output from the integrating amplifier is outside the range: Ground to -REF. The integrating amplifier will, therefore, limit at a voltage slightly more positive than ground or slightly more negative than minus reference voltage. The 100 ohm resistor in the emitter circuit of these two transistors causes the overshoot in voltage to be proportional to the amount of input current to the integrating amplifier. Thus, for example, if a high integration rate is used, a larger overshoot will result. This larger overshoot voltage in part compensates for the fact that larger integration rates are used for shorter lines. The overshoot on the scope measured in inches is nearly constant regardless of the line length.

Just below the integrating amplifier is shown an LM304 high-precision reference supply generator. This device produces the reference voltage of 5.000 volts. Because several resistor values are computed to function correctly only when the reference voltage is 5.000, this reference voltage should be carefully adjusted.

8.4.2 Inversion Section

The Inversion section of the circuit provides:

- (1) Precision inversion of the basic ramp signal α
- (2) Precision inversion of the constant negative reference supply to provide a positive reference voltage

The dynamic inversion of the signal α and negative offset ($1-\alpha$) is done by a high-precision, high-speed operational amplifier. The 0 to 5 pf trimmer capacitor is used to compensate for the delays inherent in the amplifier. Careful trimming of this capacitor is required to make the $1-\alpha$ signal be exactly the inverse of the α signal. In particular, the sum of α and $1-\alpha$ must, at all times, be exactly the minus reference voltage. A matched triple of resistors is used in this inversion to insure precision.

Below the dynamic inverter is a static inverter for the reference supply, Location C1. This 148A operational amplifier simply inverts the minus reference voltage to produce a positive reference voltage. Its resistors are matched to .005% in order to provide for precision in the inversion. This amplifier should be trimmed to balance out its input offset voltages.

8.4.3 Crossover Detector (Sheet 2, B1-2)

The purpose of the crossover detector is to determine when the basic ramp signals α and $1-\alpha$ lie within the range where the parameter α lies between 0 and 1. Three outputs are provided from the crossover detector. These are $\alpha < 0$, $\alpha > 1$, and $0 < \alpha < 1$. The crossover detector compares the α and $1-\alpha$ signals to the analog ground to determine when α is within range. The LM306 is a high-speed crossover detector which determines which of its two inputs is more positive. Its output signal available at test points R or P, is a logical low (due to the inverters), whenever the voltages shown at its input bear the relationship + to - indicated. That is, Pin 7 is a logical high whenever input 3 is more negative than input 2. Thus, the LM306 at Location B2 will have a high output whenever the basic ramp α is a negative voltage. The basic ramp α will be a positive voltage only when the parameter α is less than 0. Similarly, the LM306 at Location B1 detects the polarity of the inverted signal, $1-\alpha$. An AND gate (79.6) is provided for these two signals to indicate when the basic ramp is within the workable range.

8.5 Adjustment Procedures

There are several adjustments available on the Ramp Card. In the order in which signals pass through the card, the first adjustment met is the trim adjustment on the output amplifiers on Sheet 1, Location B4 and C4. These trim adjustments should be set at mid-range. Critical adjustment of these trim adjustments need only be made, if precision sweep-timing is required.

If precision sweep-timing is required, these trim adjustments should be made as follows: With the *UP and *DOWN inputs (Location B4, Sheet 2) high, short together the positive and negative inputs of the

$$- \left[\frac{1}{L} \right]$$

amplifier (Location B4, Sheet 1). Adjust its trim potentiometer to the value at which its output just switches from maximum positive to maximum negative voltage. Now, short together the two inputs of the 148A amplifier at Location C4 on Sheet 1. Adjust its trim resistor to the location at which its output just switches from maximum positive to maximum negative voltage. With inputs provided so that the negative reference input to the output amplifiers on Sheet 1 is provided, the output voltages

$$+ \left[\frac{1}{L} \right] \text{ and } - \left[\frac{1}{L} \right]$$

should be exactly equal and opposite in sign. Minor adjustment of the trim potentiometers on those two amplifiers may be used to insure this equality.

8.6 Timed Sweep-Rate Control

The 20K potentiometer (Location B4, Sheet 2) may be used to adjust the time of a total sweep. Sweep-time should be measured as the duration of the low signal at the $\frac{0 < \alpha < 1}{}$ output.

The trim potentiometers on the two-type 501 operational amplifiers (Location D2 and D1, Sheet 2) must be adjusted correctly. To adjust each of these, connect the negative input terminal of the amplifier temporarily to the common terminal. Adjust the trim potentiometer until the output is as close as possible to switching from positive saturation to negative saturation. A similar adjustment should be used for the trim potentiometer on the 148A amplifier at Location C1, on Sheet 2.

The most critical adjustment on the entire card is the trimmer adjustment at Location D2. This trimmer should be adjusted so that the α and $1-\alpha$ ramps exactly cancel. A precision resistor network should be connected between the α and $1-\alpha$ ramp. The midpoint of this precision resistor network should remain at a constant potential equal to $1/2$ of the negative reference voltage. The adjustment of the trimmer should be made at the highest integration rate to insure that the α and $1-\alpha$ ramp signals are as nearly identical as possible.

X & Y D/A CONVERTER

9.1 Function

The X & Y D/A Converter Cards are used to generate the deflection voltages for the Scope Driver Cards. The card accepts the output of the even and odd CODED registers from the XY Digital Card and four ramp and reference signals from the Ramp Card, and from these signals generate the deflection voltages.

The incoming ramp signals are called α and $1-\alpha$. The reference voltages are called -REF and "analog ground." The "analog ground" signal is actually a voltage reference signal and should never be used as ground for power supply return or other purposes. As far as the D/A converter is concerned, it is an incoming signal.

The name α applies to both a wire and a mathematical parameter. In the description of the operation of the D/A converter which follows, we are using α in the mathematical sense. The Line Generator produces the deflection voltages by multiplying α times one of the end-points and $1-\alpha$ times the other. Now, since α is a ramp signal, that is it changes linearly with time, the values for the deflection voltages vary smoothly from the beginning point to the end. The voltage can be given by the equation:

$$(1) \quad V = (-REF) [\alpha (\text{BITS OF IO}) + (1-\alpha) (\text{BITS OF IE})]$$

Where -REF enters into the equation because the actual ramp varies from 0 to -REF while α varies from 0 to 1 and IE and IO stand for Input Even and Odd, respectively.

By looking at the products bit-by-bit, one can see that, if the corresponding bits of IE and IO are both 0, both of the terms and their sum will be zero, and there is thus no need to multiply by the ramp signals, α and $1-\alpha$. Similarly, if they are both 1, the sum will be

$$\alpha \cdot 1 + (1-\alpha) \cdot 1 = 1$$

and again there is not need of multiplying by the ramp signals. If IO is 1 and IO is 0, the equation is simply

$$\alpha \cdot 1 + (1-\alpha) \cdot 0 = \alpha$$

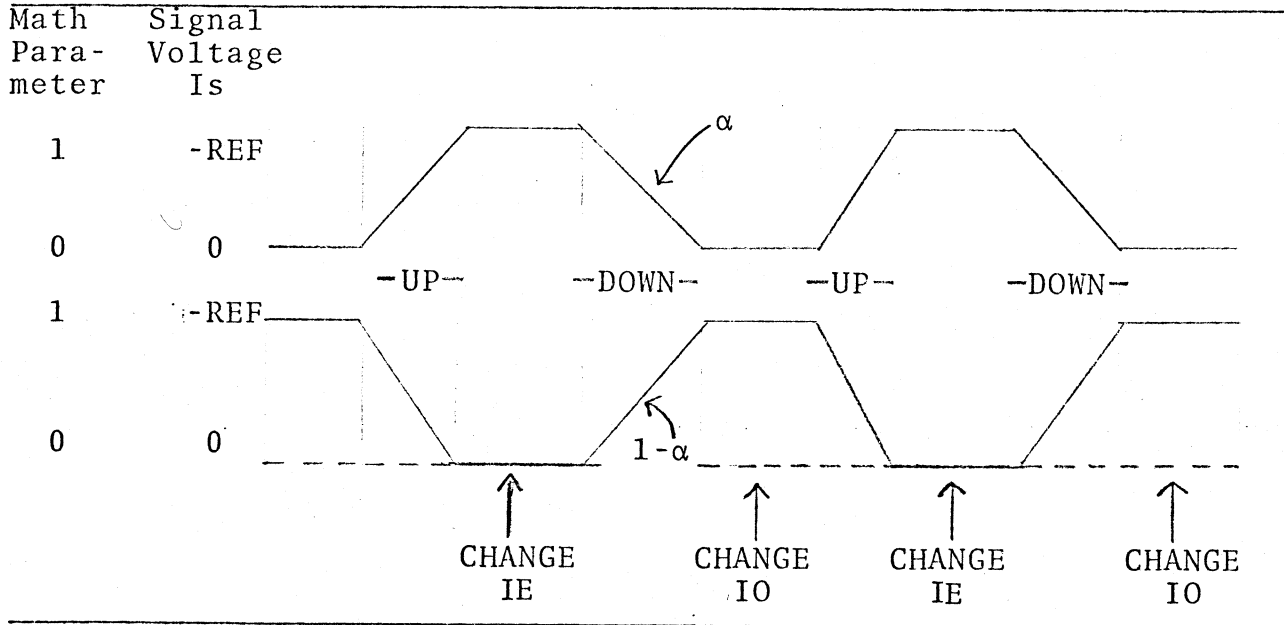
and the α ramp can be used. And similarly, if the IO input is 0 and the IE input is 1, the sum is simply $1-\alpha$. These reductions of the equation are used to increase the precision of the D/A converter. Since the -REF and "analog ground" signals can be

controlled much more precisely than the ramps, it is possible to achieve much better results by computing the voltage equation in its alternative form:

$$(2) \quad V = (-REF) [1 * (\text{BITS ON } -REF) + \alpha (\text{BITS ON } \alpha) + (1 - \alpha) (\text{BITS ON } 1 - \alpha) + 0 * (\text{BITS ON GROUND})]$$

This is done by placing a switch on each bit of the D/A converter which selects between "analog ground," $-REF$, α , and $1 - \alpha$.

Between the times when the Line Generator is actually drawing lines, the values of the parameters α and $1 - \alpha$ will always be either 0 or 1 (i.e., the voltages on the α and $1 - \alpha$ wires will be either zero or $-REF$; actually, they will be a little bit less or a little bit more than those voltages due to the overshoot). At such times it is possible to change the digital inputs IO and IE without changing the output voltage. The timing sequence of these signals is shown in the chart below.



The ability to change the digital inputs without changing the output voltage is an important part of the design of the Line Generator. The digital signals are changed alternately, so that the ramp signals can always change smoothly up and down without ever having to be reset.

The redundant bit coding used by the Line Generator insures that lines which are short will have upper bits that are identical. This is simply so that the reference signals, rather than the ramp signals, will control these upper bits, and thus the precision of the Line Generator is increased. The compensation for the redundant bits is then added to the sum produced by the D/A converter.

9.2 Reference

Logic Drawing 108110-600, XY D/A Converter

9.3 The Switches (Sheet 1)

Each bit of the D/A converter consists of a discrete component switch. The model for these switches is shown on Sheet 1 (labeled D). The circuit consists of digital selection gates (the actual gates used are shown on Sheet 3), four transistors, four field effect devices, diodes, and bias supplies.

The digital selection gates compare the inputs on IE and IO to drive one of the transistors. The NAND gates combine the signals such that:

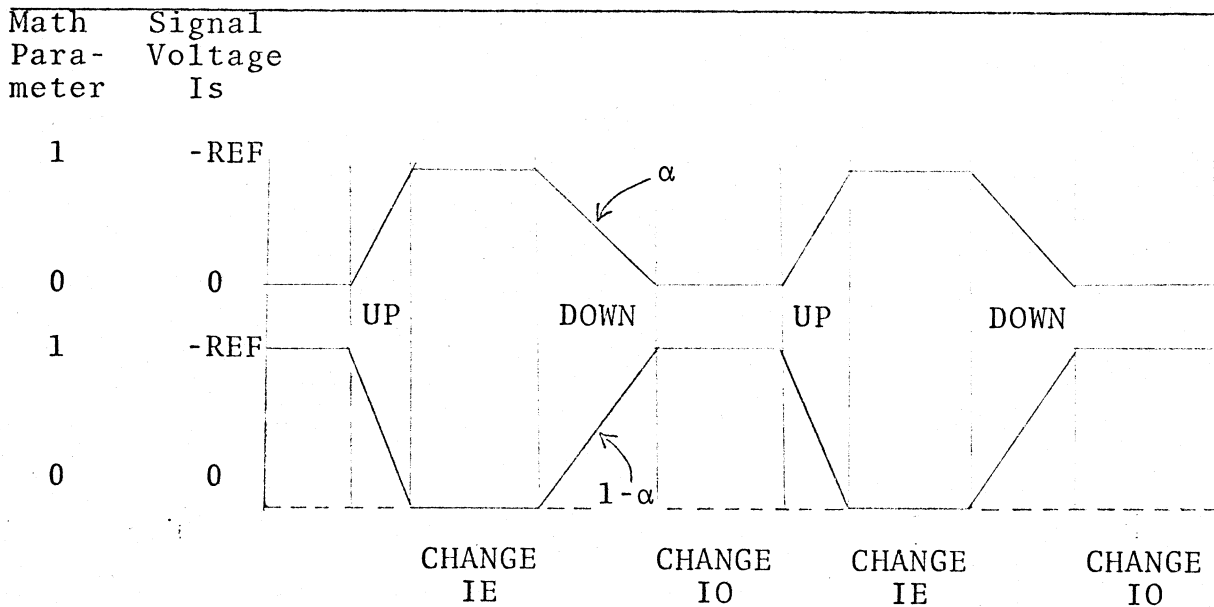
<u>IE</u>	<u>IO</u>	<u>Selects</u>
0	0	Analog ground
0	1	α
1	0	$1-\alpha$
1	1	-REF

The emitters of the four transistors are connected together and connected to a 6.81K resistor to +15 volts. The 6.81K resistor provides a current source of approximately 2 mills. In this configuration, only one of the transistors can possibly conduct. The one which conducts will be the one whose base voltage is nearest to ground potential. Thus, if any of the NAND gate outputs are low, the 1K divider networks will cause their corresponding base to be the one closest to ground potential and cause the corresponding transistor to conduct. If none of the AND gates are low, then the transistor whose base is connected to +4.3 volts will conduct. In any case, the current through the 6.81K resistor will be nearly constant.

The transistor which is conducting will raise its collector towards ground potential. In the little group of three diodes, this will cause the right-hand diode to conduct. The collector of the conducting transistor will, therefore, be clamped to the "ground," " α ," " $1-\alpha$," or "-REF" voltage. The collector will actually be different in potential from these reference voltages by the amount of the diode drop. The central diode of the group will be conducting because of the 68.1K resistor to the -60 volt supply. The voltage drop across the central diode will exactly cancel the voltage drop across the right-hand diode, so that the potential of the gate input to the field-effect device will be about equal to the potential of reference voltage. The field-effect device will, therefore, conduct.

For those transistors which are not conducting, the collector voltage will drop until clamped at -25 volts by the left-hand diode of the group. This will apply a large negative voltage to the gate of the field-effect device and cause it to be an open circuit. The basic switch, therefore, connects its output (shown at the bottom) to one only of the four input reference voltages.

The input switch for the redundant bits, S, is constructed in analogous manner, but has only two possible connections. The representative symbols for these two switches are shown in the lower left corner of Sheet 1.



9.4 The Ladder Network (Sheet 2)

The basis for the D/A Card is the ladder network shown on Sheet 2. The ladder network is made of highly precise resistors, so that the effect of each successive bit of the ladder network is exactly one-half of the effect of the next most significant bit. The ladder network is of a standard type. The effective impedance looking back into the network is always either 10K or 20K, assuming that all of the switching points are grounded. The switching points are always connected to one of the four source signals which are AC grounds.

The ladder network combines the voltages on the four input signal lines in a linear manner. Each bit of the ladder network that is connected to the α line contributes its percentage of α signal; each bit connected to analog ground contributes its percentage of analog ground; each bit connected to -REF contributes its percentage of the -REF signal; and each bit connected to $1-\alpha$ contributes its percentage of $1-\alpha$. The output voltage will be the combination of all of these voltages to form the sum shown in equation (2) (Section 9.1).

9.5 Redundant Bits (Sheet 2)

The signals IR(4) and IR(6) from the XY Digital Cards indicate that redundant coding has been used in order to make the upper three bits, or the upper five bits of the input numbers IE and IO the same, and thus increase the precision of the D/A conversion for these most critical bits by eliminating the need for using the ramp signals. The redundant bit signals are used to control the S switches (Location C3). If one of these bits is set the appropriate compensation will be made by adding voltage into the D/A conversion line.

9.6 The Output Amplifier (Sheet 2)

The currents provided by the ladder network and the redundant bits are added together at the input summing junction of the operational amplifier. The operational amplifier serves two purposes. First, it drives the analog output buss to provide the signals to the Scope Driver Cards. Second, it provides isolation in the grounding system between the Scope Cards and the ramp generator.

The isolation of the grounding system is the more difficult concept to understand, so it will be described in some detail. The resistor configuration around the operational amplifier provides for balanced output from the balanced input. The two resistors connected between ground and -REF provide an effective input voltage for the positive input of $-REF/2$. If the ladder network were half connected to -REF and half connected to ground, then the two inputs to the operational amplifier would be identical as far as the input side is concerned. Under these conditions, the two outputs of the operational amplifier must also be the same, but the particular voltage at the outputs is not important, as far as the amplifier is concerned. Thus, the outputs of the operational amplifier could have been set at any desired voltage. We have chosen to fasten one of the outputs to the power supply return wire. Notice that noise on this wire will contribute only to the common mode signal in the two output wires and not to the difference signal. Both of the output wires are run as the analog buss to feed the differential amplifiers on the Scope Driver Cards.

Z D/A CONVERTER

10.1 Function

The D/A conversion for Z is carried out by the same logic as for X and Y, with the exception that the four least significant bits and the redundant coding switches are omitted.

10.2 References

Logic Drawing 108107-600 (same as 108110-600, XY D/A Converter)

Section 9 of this manual

SCOPE SELECTION CARD

11.1 Function

The Scope Selection Card contains the SELECT and PERMIT registers, which control the selection of the scope on which the picture is to be drawn, the directive register for the Line Generator, and circuits which implement the blinking and dashing facilities of the Line Generator. The Scope Selection Card also detects when very short lines require intensity correction and generates the analog intensity correction signal for the Scope Driver Cards.

11.2 Reference

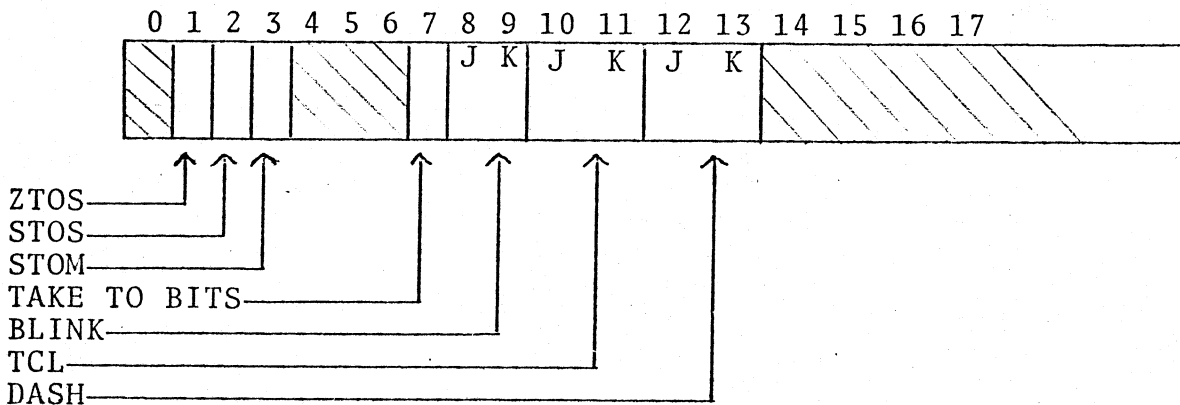
Logic Drawing 108115-604, Scope Selection Card

11.3 SELECT and PERMIT Registers (Sheets 1 and 2)

The SELECT, PERMIT and directive registers have the same three stages as the other registers in the Line Generator. At CLOCK 1 time data are strobed into the input registers shown at the bottom of Sheet 1, when POKE 1 is high. The data are then transferred to either the SELECT and PERMIT registers, or to the directive register, if the proper control signals are enabled.

The SELECT register is 8 bits long. The 9th bit of input is used as a "take" bit, that is the other 8 bits are not loaded unless bit 9 is high. Similarly, the PERMIT register is 8 bits and is not loaded unless the 17th bit, PRIV, is set. The SELECT and PERMIT registers are loaded at CLOCK 2, if their respective enabling bits are set and if LOAD and *CZ are present.

The directive register is shown at Location C on the logic drawing. The format for this register is shown below:



The directive register is loaded at CLOCK 2, whenever LOAD and *CDIR are present. Note that the "TO" bits are only loaded, if

the "TAKE" bit is high, and that the other bits are J-Ked so that the bits of the directive register can be manipulated independently.

The row of switches at the top of Sheet 1 selects either the SELECT and PERMIT registers or the directive register onto the OLD lines, so that these registers may be saved in memory.

The row of gates at the bottom of Sheet 2 compares the SELECT and the PERMIT bits and detects when a scope selection violation has occurred. It should be noted that both of these registers are unary coded. The TUT TUT FORBID signal is sent back through the command cable to initiate an interrupt in the case of scope selection violation.

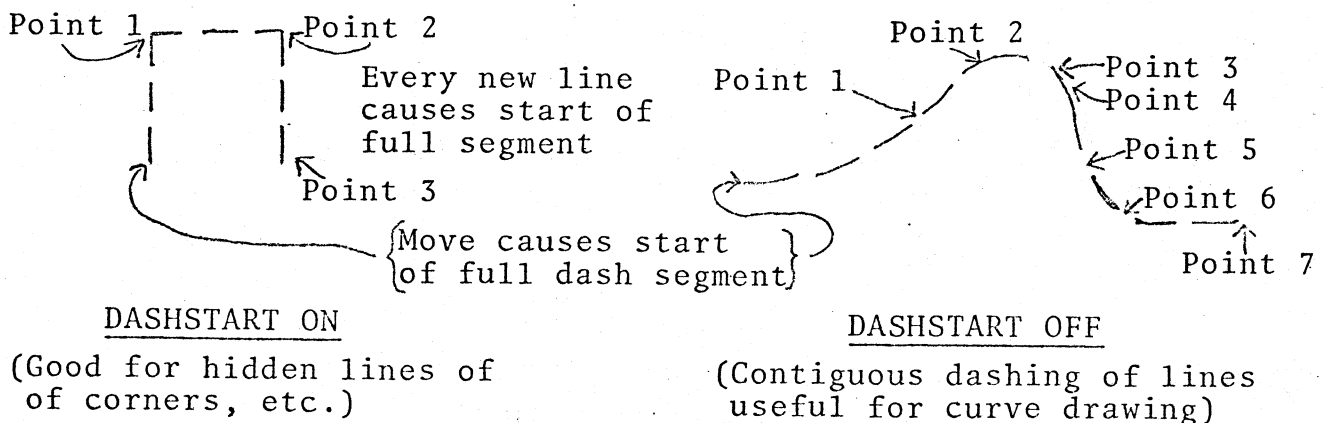
12.4 Blinking

Blinking is implemented by interrupting the scope selection so that no scope is selected while the blink is off. When blinking is set, the multivibrator 54 will cause the picture to blink on and off at a 5-cycle per second rate by interrupting the scope selection.

The register at the top of Sheet 2 contains the current scope selection bits which control the use of the Scope Driver Cards. The dash code (DASH and CENTER) is also registered at this point. These registers are loaded at CLOCK 3 when POKE 3 is high.

12.5 Line Dash Circuit (Sheets 3 and 4)

The line dash circuit enables an operator to select short dashed lines, long dashed lines, or short-long-short dashed lines. A dashed line always starts with a full-length intensified segment following a MOVE. If DASHSTART is high, then each DRAW also causes the line to start with a full-length dash (see Location A2). If DASHSTART is not given, then dashing continues smoothly (contiguously) for each successive DRAW, as if the series of lines were only one line. The effect of DASHSTART is shown below:



The DASHSTART gate control is wired to ground or + 5V on the back panel.

The dashed line oscillator (left side of Sheet 3) operates at 160 megahertz. This frequency is reduced by high frequency MECL counters to 20 MHz and further reduced by high speed TTL to 5 MHz. Thereafter, it is decoded into a series of short dashes, long dashes, and short-long-short dashes that may be selected by combinations of the CENTER and DASH signals (Sheet 4).

Use of high frequency is necessary to provide the contiguous dashing capability. After a MOVE, or while DASHSTART is ON, all of the countdown counters are reset before the beginning of each line, so a full-length dash segment is always begun. On the other hand, when DASHSTART is OFF, the countdown counters are reset on MOVE only. For a series of lines, the count is held and continued only during the intensification periods of the line drawing cycles.

A constant frequency produces uniform length dashed lines because of the constant velocity characteristic of the Line Generator. However, for the shorter lines, this velocity is cut to half, then half again, etc. For these slower velocity short lines, the frequency of the dash oscillator is automatically cut in half correspondingly (see A3-4), so that the observed dashed pattern does not change for any length line.

The dashed line code is controlled by plug-in wired connectors in Position 52, 62 and 72 (see Sheet 4, Location D2). The patterns may be changed if desired by changing the connector wiring. A 10-to-1 decoder provides a wired selection of the number of parts of a cycle; up to a limit of 10. Following any one of these parts of a cycle, a JK flip-flop (C2) may or may not be complemented according to the wired code in the connector.

12.6 Intensity Correction Circuit (Sheet 5)

The intensity correction circuit provides voltages that are used by Scope Driver Cards for correction of intensity for short lines.

For an α , $1-\alpha$ line generating method, the ramp generator must run faster for short lines in order to maintain constant beam sweep velocity. A speed is reached, however, where a further increase in ramp speed is no longer practical. Thus, for lines having horizontal and vertical length components between $1/128$ th and $1/64$ th the screen width, the ramp speeds are the same as for lines longer than $1/64$ th the screen width. The result is a beam sweep velocity with one-half the "normal" velocity. For lines between $1/256$ th and $1/128$ th the screen width, and between $1/512$ th and $1/256$ th the screen width, the same ramp speeds are again used, and the corresponding beam sweep velocities becomes $1/4$ th and $1/8$ th normal.

Slower beam sweep velocity for short lines causes an increase in phosphor light energy which must be reduced, if constant brightness is to be maintained. The intensity correction circuit provides four analog voltage levels, called INTCOR, which are used by the Scope Driver Cards for intensity correction. These voltages are a logarithmic function of the sweep velocity. The voltages produced are 0 volts (normal velocity), -1 volt ($\frac{1}{2}$ normal velocity), -2 volts ($\frac{1}{4}$ normal velocity) and -3 volts ($\frac{1}{8}$ normal velocity).

The required voltages are obtained by using a diode digital-to-analog converter with a 715C integrated circuit operational amplifier.

SCOPE DRIVER CARD

12.1 Function

Associated with each scope of the system is a Scope Driver Card which interfaces the Line Generator with that scope. Each different kind of scope will have its own Scope Driver Card. Basically, the operation of the card is the same for all scopes, but the values of delays and gains and the setting of switches can be adjusted for a particular scope.

The Scope Driver Card provides for meaningful adjustment of line intensity and contrast, generates the necessary unblank signals, and provides the deflection voltages for both the major and minor X and Y deflection systems of the scope.

12.2 Reference

Logic Drawing 108113-600, Scope Driver

12.3 Intensity (Sheet 1)

The circuits shown on Sheet 1 of the logic drawing provide facilities to control line intensity and contrast through the potentiometers mounted on the oscilloscope. The currents provided are used to vary the intensity of light sources in the Raysistors (left side of Sheet 1). The light generated provides electrically isolated control of the variable resistors on the Raysistors, which in turn control the input signals to the intensity circuit. The output voltage from the intensity circuit is described by the following equation:

$$V_{out} = \pm [K_4 + K_3 e^{(K_2 + K_1 V_z + K_0 V_{video})}]$$

BEAM INTENSITY CONTROL (K₄)

The K₄ coefficient is directly related to the maximum beam intensity. It is controlled by R26 (Location B2) and is normally factory adjusted, but may have to be readjusted as the CRT ages.

CONTRAST RANGE CONTROL (K₃)

The maximum contrast is set using R22 which controls the gain coefficient K₃. R22 should be set for maximum contrast in a dark room.

VIDEO GAIN CONTROL (K₂)

The video gain coefficient, K₂, is operator-controlled through Raysistor R78. R78 controls the offset current extracted

from the summing node of the function generator. After exponentiation the effect of this input control is to provide dimming.

CONTRAST CONTROL ($K_1 V_z$)

The contrast coefficient, K_1 , is provided through the Ray-sistor R77 and is operator-controlled. The contrast control conditions the Z input signal, and the resultant signal is applied to the summing node of the operational amplifier for the function generator. As a result of exponentiation, this input control becomes the contrast control for internal Z signals.

EXTERNAL CONTRAST CONTROL ($K_0 V_{\text{video}}$)

A log video signal, such as a radar or TV signal, can be mixed with the Z-intensity input. This input is activated by the digital signal *SHOW VIDEO which drives an MM8800-level shifter which converts the digital logic levels of 0 and 4 volts to -14 and 0 volts. When *SHOW VIDEO is low, FET Q1 is switched on and the VIDEO INPUT signal is enabled onto the summing node. Raysistor R76 controls the gain of the video signal (K_0), which after exponentiation becomes the external video contrast control.

12.3.1 Short Line Correction

When lines become very short, it is no longer possible to run the ramp fast enough to keep the beam velocity constant. For such extremely short lines, the velocity is cut in half, fourths, etc. In order to draw such lines at the appropriate intensity, the intensity circuit compensates for short lines by injecting the analog intensity control signal INTCOR (Location A4) into the summing node. Adjustment of the degree of coupling of this signal (R7) should be made when the CRT screen is filled with a mixture of long and short lines (e.g., variable-sized characters). Variable resistor R7 should be adjusted until all lines appear equally intensified.

12.3.2 Function Generator

Resistors R9 through R19, together with diodes CR5 through CR10, form a fast diode function generator which has the output shown in the upper right corner of the drawing. The range of the function generator was selected to adequately cover the range of output corresponding to the dynamic light intensity range of a CRT in a dark room. The cathode of all diodes are connected to the summing node which is maintained at zero volts because of the operational-type connection. Thus, a diode is switched in at voltages above about 0.5V. Resistors R9 through R14 are

successively switched in to change the slope,

$$R = \frac{\Delta E}{\Delta I}$$

of the output, where R is simply the parallel combination of the switched-in resistors. The switch point for each diode is adjusted to occur at the required voltage break point by adjustment of corresponding resistors R15 through R19.

12.3.3 Tap Delay

A 0 to 500 NS tapped delay line (25 NS/tap) provides adjustable delay for the analog intensity voltage. The 511 Ω resistors R21 and R79 properly match the input to, and output from, the delay line. The resistance in the tap line is sufficiently high to prevent undesirable reflections.

12.3.4 Output Amplifier

The output amplifier can be connected either potentiometrically (non-inverting) or operationally (inverting) and various gains and offsets can be selected. The 91 Ω resistance between the amplifier and the output 91 Ω coaxial cable provides a matched impedance.

12.3.5 Tuning Procedures

The tuning procedure for the intensity circuit must be accomplished in a room that can be made very dark.

STEP 1: Program the display to provide a raster of long lines, each of which start at minimum intensity and end at maximum intensity. The field should repeat at a 60 cycle/second rate.

STEP 2: Turn remote dimmer control to the maximum intensity position (CW).

STEP 3: Turn the video and Z contrast controls to the minimum position (CCW).

STEP 4: Adjust MAX SET (R2) until EA=EB (Location B2 on drawing).

STEP 5: Adjust scope intensity on the oscilloscope and BEAM INTENSITY (R26) until a maximally-bright signal is displayed for which reasonably sharp lines can be obtained using the oscilloscope focus control.

STEP 6: Darken the room and turn the Z contrast control to maximum contrast position (CW) and adjust the

CONTRAST RANGE CONTROL (R22) until the least bright portion of the lines just disappear. Observe that variation of this control should not affect the intensity of the brightest portion of the line.

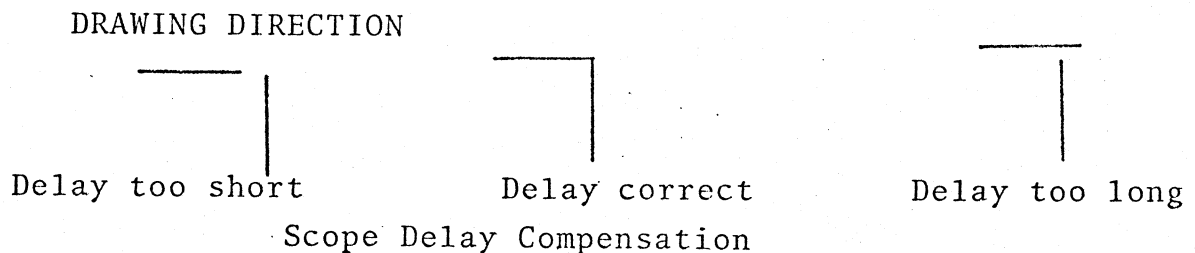
STEP 7: Program the display to provide a large number of equal intensity but mixed long and short lines. Adjust the INTENSITY CORRECTION ADJUST (R7) until all lines appear to have equal intensity.

When the above procedure is followed, it becomes possible to alter contrast so that minimum intensity lines just disappear for a wide variation in room lighting. Variation of the contrast control does not change a maximum intensity line. The dimmer control can change the light level for a camera. Indeed, the dimmer control could be marked in F-stop numbers. A picture taken at one F-stop setting should then appear the same as a second picture taken with the scope dimmer control adjusted one F-stop down and the camera adjusted one F-stop up.

12.4 Unblank Circuit (Sheet 2)

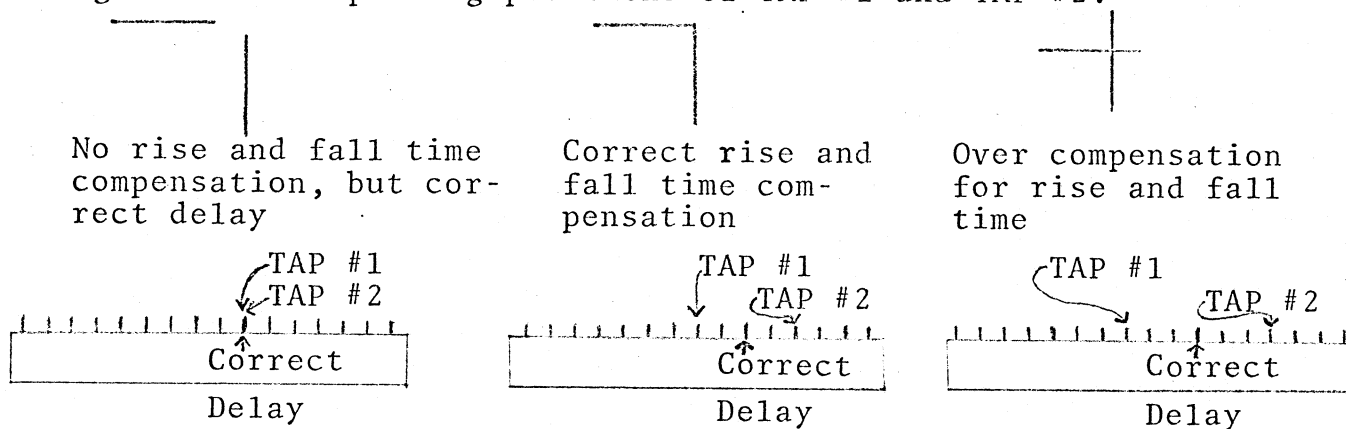
The unblank circuit adapts the Line Generator scope select and draw signals to the blanking requirements of any one of a variety of scopes. The circuit consists of an input intensity select gate, a vernier microcircuit delay, a tapped delay line and an output driver. The unblank circuit is activated by the combination of the scope select signal SEL(n) and the intensify signal INT (which is initiated by the crossover detector on the Ramp Card and modified by the DRAW, BLINK and DASH signals in the Scope Select Card). Overall unblanking delay for a given scope can be selected in 12 nanosecond steps from 20 to 530 nanoseconds. A dual tap capability on the delay line enables compensation for the rise and fall times in the unblanking circuits of both the Line Generator and the scope; this compensation is obtained by combining the outputs of the two taps, thus providing a controlled widening of the basic INT signal as well as delay. Finally, the output drive circuit allows selection of output polarity and levels for the unblanking signal.

Adjustment of the unblanking delay should be accomplished while observing the effect on the display of random sets of two or more nonparallel lines having end-points that meet at a common point. The displays resulting from too short a delay, from the correct delay, and from too long a delay are shown in the following figure:



The correct delay is obtained by tying the two tap lines (TAP #1 and TAP #2) together and running these lines up and down the delay tap points until the correct picture appears. Wired switch S1 can be changed, if a delay between adjacent taps is desired.

Compensation for rise and fall times within the unblanking circuits of the Line Generator and scope may be needed for the fast, short vectors. After the correct delay has been obtained, as described in the preceding paragraph, short vectors may appear with gaps between successive vectors that should be connected. The result of no rise/fall time compensation, correct compensation and too much compensation are shown in the following figure, along with corresponding positions of TAP #1 and TAP #2.



Short Vector Rise and Fall Time Compensation

If long lines appear as shown above, this method of correction will not work. Correction for long lines is obtained by adjustment of the crossover detector points in the Ramp Card.

The output unblanking amplifier drives the 90 Ω coaxial cable which should be properly terminated at the scope. Wired switches S3 and S4 provide the ability to select the inversion of the output pulse. Wired switch S2 changes output voltage swing range from 0 to + 5 volts to 0 to - 5 volts.

11.5 X, Y, X-Minor, Y-Minor Output Analog Voltage Amplifiers

Provision is made on the Scope Driver Card for four identical analog voltage amplifiers. These amplifiers provide drive to the X, Y, X-minor and Y-minor output to any one of a variety of types of scopes. Gain can be changed and polarity may be selected. The input impedance to the amplifiers is high, thus allowing a number of Scope Driver Cards to be connected to the Line Generator without appreciable loading of the basic analog deflection signals. Signal and signal ground inputs to these amplifiers are balanced to provide rejection for the common-mode noise that can occur on the input signal ground.