FIRST AID KIT

for

LINE GENERATOR

BY

MHO SALIM

M E M O

DATE: October 23, 1972

TO: Whom it may concern

FROM: Mho

SUBJECT: First Aid Kit for LG or What to do until Cheadle comes

A copy of the test procedure for the Line Generator is available to all interested parties from the Engineering file.

This procedure is written in the form of if... then... and has been used by the test department for system test. The prodedure is not complete and the idea is to complete it as time goes by and more systems get tested.

As it stands, however, it may be helpful to anybody who happens to have a problem with the Line Generator. Any suggestions regarding this document should be directed to Test department.

Thanks

Mho

TEST PROCEDURE FOR LINE GENERATOR
OR WHAT TO DO UNTIL CHEADLE COMES

ACCEPTANCE

The Line Generator should not be accepted to test unless the following are checked.

1) Power Supplies

Three power supplies are used in the linear (analog) portion of the LG. The LG cannot share these supplies with any other device.

These power supplies must be checked before installation and must have acceptance tags.

**Do not begin test without being sure that the supplies have been tested.

Check the following for possible error:

Quiet VCC (+5 volts)
Uses blue and black twisted pair to the back pannel. Blue =+5 if black=ground.

+,-15 Volts
Uses purple/black; red/black twisted pairs. red=+15, black=ground, purple=-15.

-6Ø volts
Uses orange/black twisted pair orange=-6Ø , black=ground.

These wires should be connected to the back pannel according to the printed circuit writings.

In addition to these another power supply is used for the digital portion of the system that is connected to the conventional place on the cage.

2) The Cards

The system uses the following boards.

Assy#	Quan.
1Ø81Ø9	1
1Ø9114	1
1Ø81Ø3	(2)

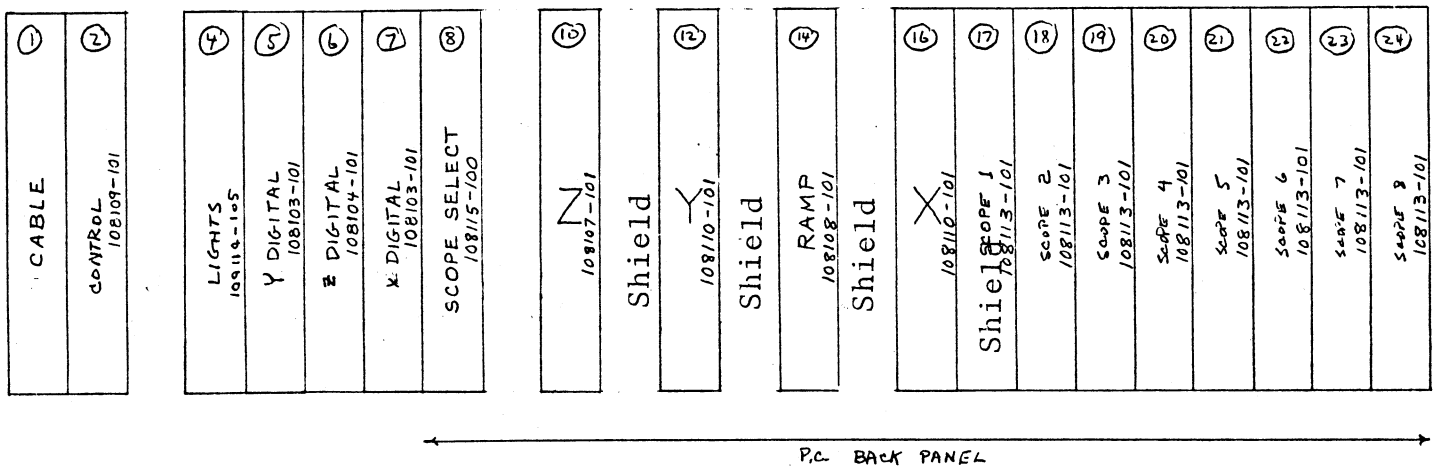
Assy#	Quan.
1Ø81Ø4	1
1Ø8115	1
1Ø81Ø7	1
1Ø811Ø	(2)
1Ø81Ø8	1
1Ø8113 or A 1Ø8114	

A pattern generator may take the place of a cable.

There are also four matal shields that are quite sacred and should be in their respective position or Allah will mess up the system.

The print on the next page (1Ø81Ø1 - 6Ø1) shows the card layout. Note that slot 17 is occupied by one of these shields. Slot 17 would normally be "Scope 1" to the conventional line generators. This is our nice way of saying that the conventional line generators (as they leave E & S) do not have a "Scope 1" to the programmers.

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED



CONTRACT NO.	
DRAWN	
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MECH	
ELEC	
PROJ. ENG.	
DESIG. AUTO.	
APPROVED	

EVANS & SUTHERLAND
COMPUTER CORPORATION
SALT LAKE CITY, UTAH 84112

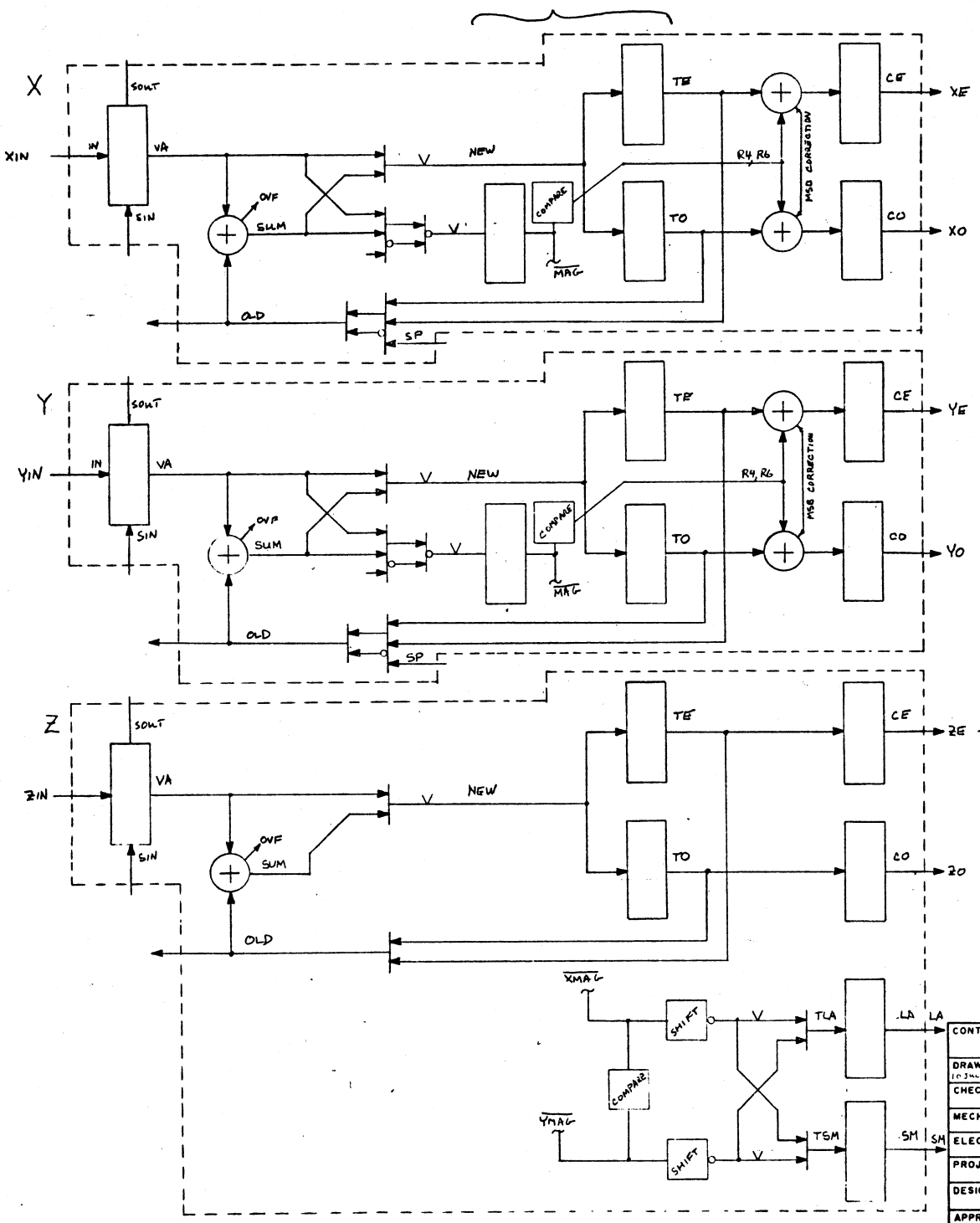
TITLE

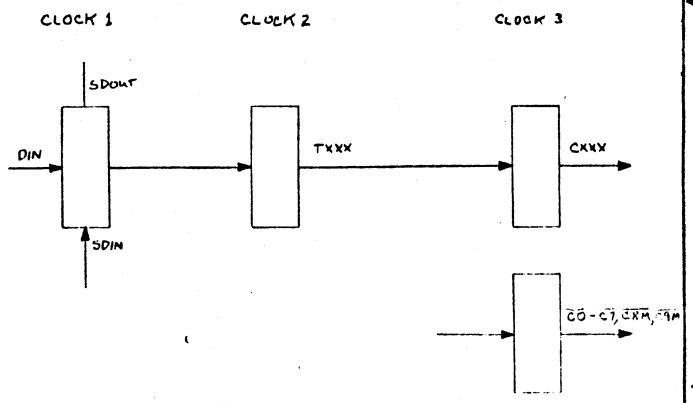
LINE GENERATOR
CARD LAYOUT

C	DWG 108101-601 / 605	REV A 8
SCALE		SHEET 1 OF 6

REVISIONS			
ZONE	DES...ON		AP
	OVF, TEST PTS	21 JAN 70	JG

4





CONTRACT NO.	
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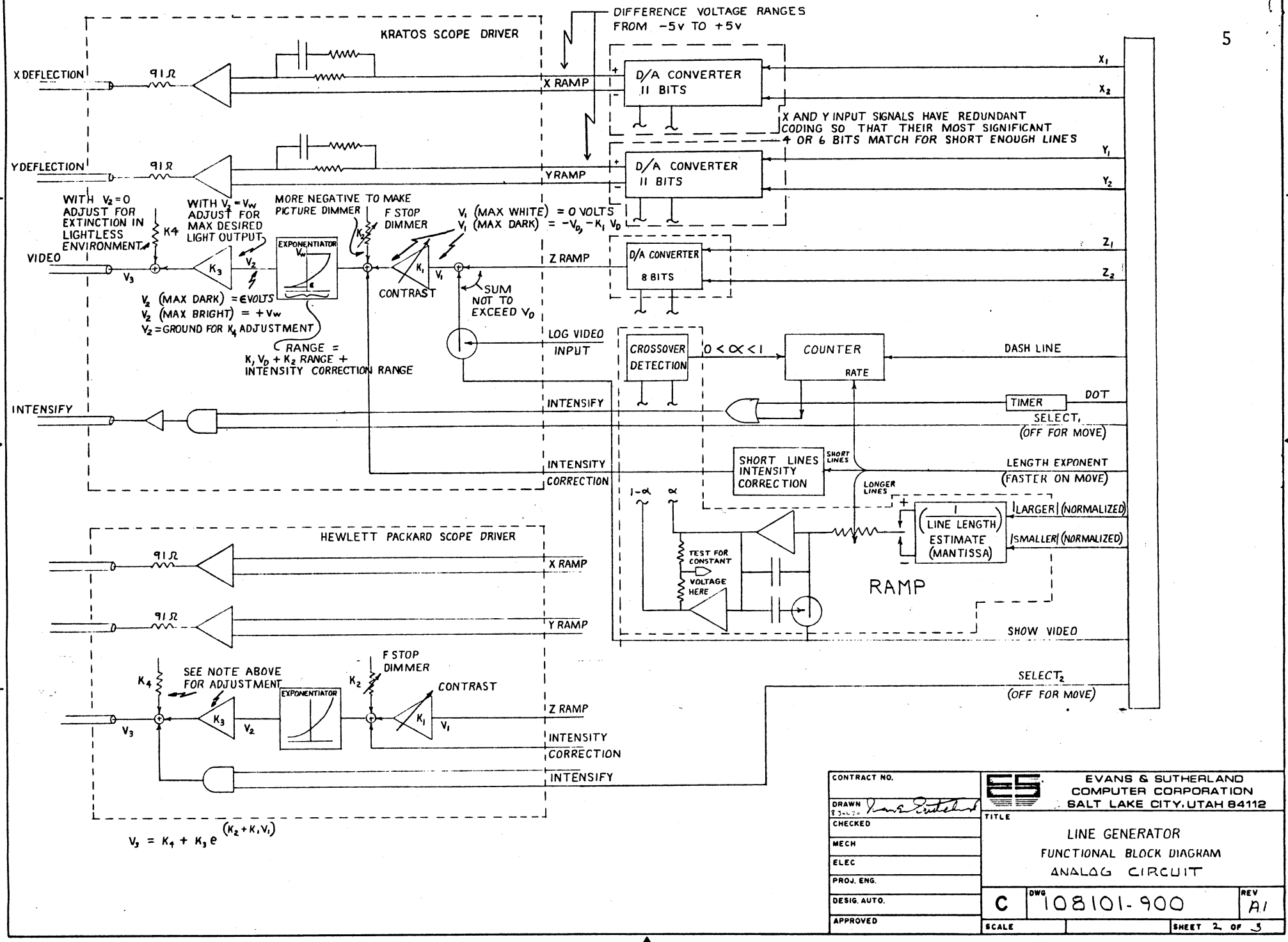
ELEC	
PROJ. ENG.	
DESIG. AUTO.	
APPROVED	

EVANS & SUTHERLAND
COMPUTER CORPORATION
SALT LAKE CITY, UTAH 84112

TITLE
LINE GENERATOR
FUNCTIONAL BLOCK DIAGRAM
DIGITAL CIRCUIT

SCALE	DWG	REV
C	109101-900	A1

SHEET 1 OF 3



CONTRACT NO.	
DRAWN	
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EVANS & SUTHERLAND COMPUTER CORPORATION
SALT LAKE CITY, UTAH 84112

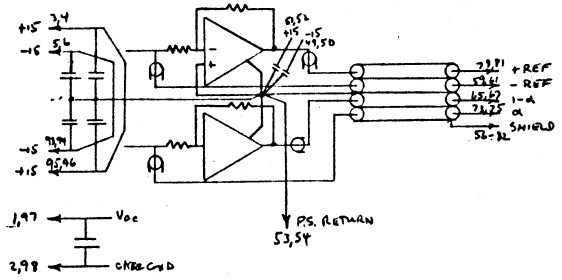
TITLE
LINE GENERATOR
FUNCTIONAL BLOCK DIAGRAM
ANALOG CIRCUIT

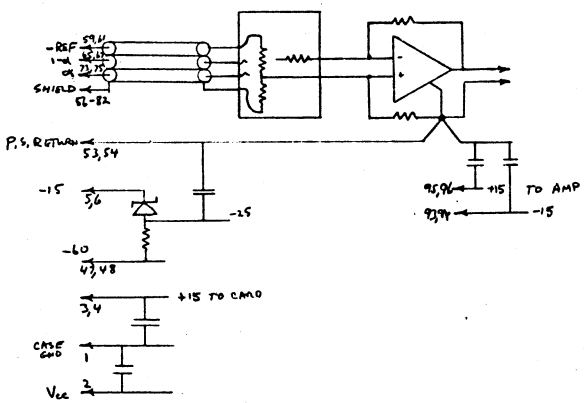
SIZE	DWG	REV
C	108101-900	A1

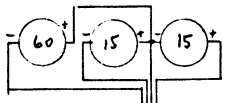
SCALE | SHEET 2 OF 3

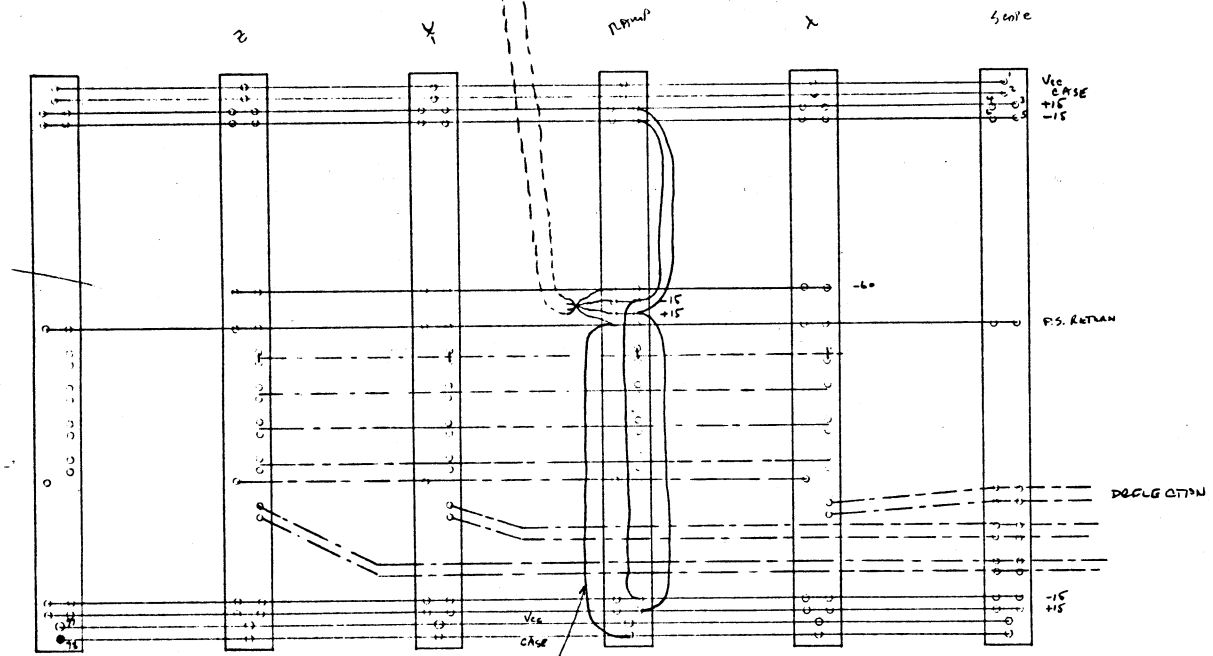
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

RAMP

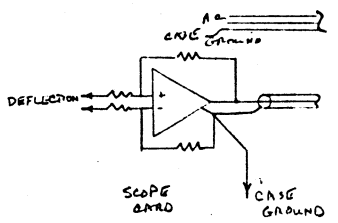


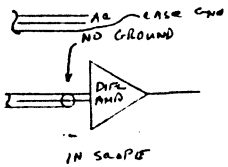






N.B. THIS IS THE ONLY WIRE CONNECTING THE ANALOG P.S. RETURN TO THE CASE





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DESIG. AUTO.	
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EVANS & SUTHERLAND COMPUTER CORPORATION
SALT LAKE CITY, UTAH 84112

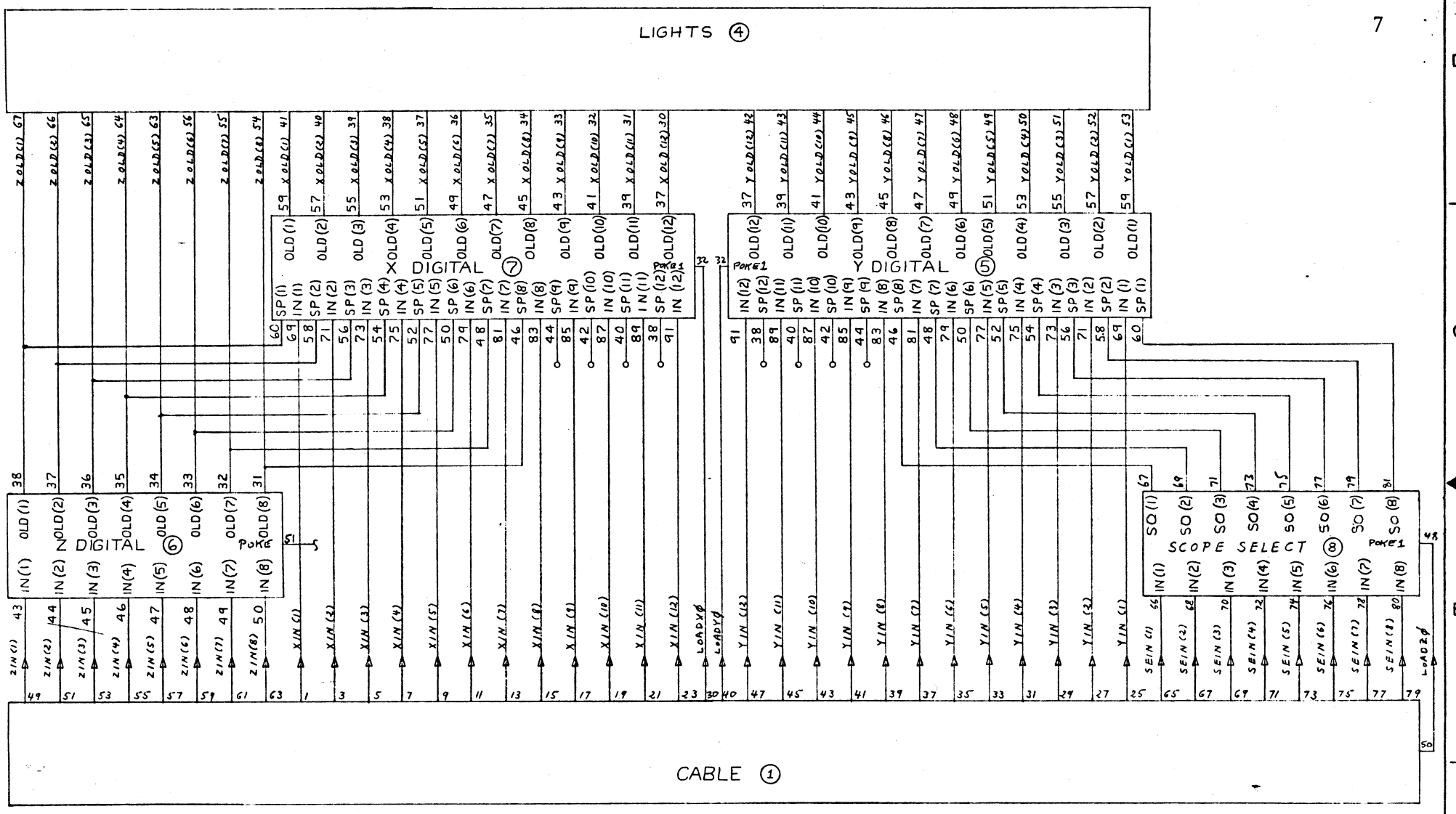
TITLE
LINE GENERATOR
FUNCTIONAL BLOCK DIAGRAM
GROUNDING SYSTEM

SIZE	DWG	REV
C	108101-900	A1

SCALE | SHEET 3 OF 3

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

7



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PROJ. ENG.	
DESIG. AUTO.	
APPROVED	

EVANS & SUTHERLAND
COMPUTER CORPORATION
SALT LAKE CITY, UTAH 84112

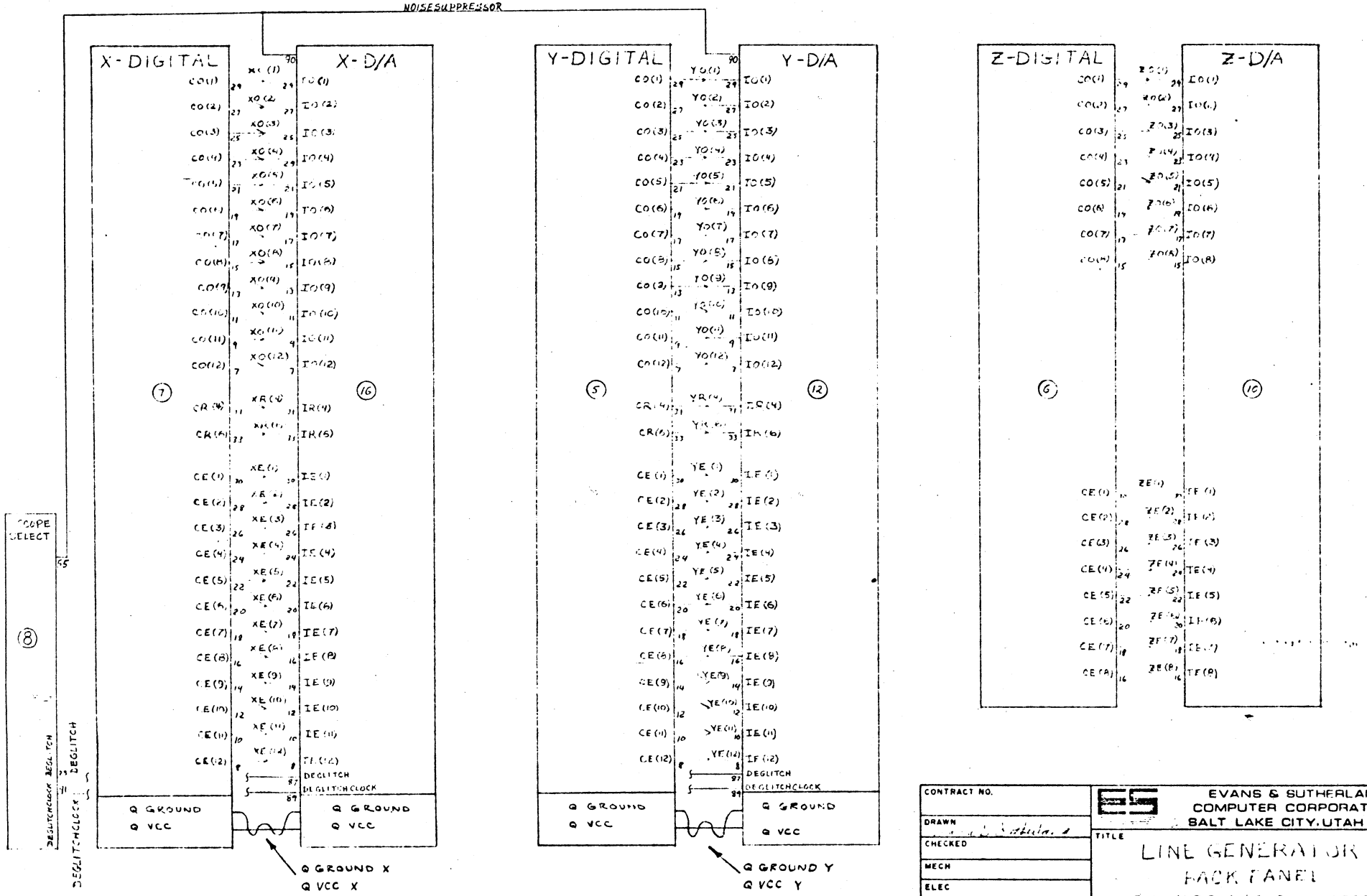
TITLE
LINE GENERATOR
BACK PANEL
DATA TO DIGITAL CARD

SIZE	DWG	REV
C	108101-601/605	4-9

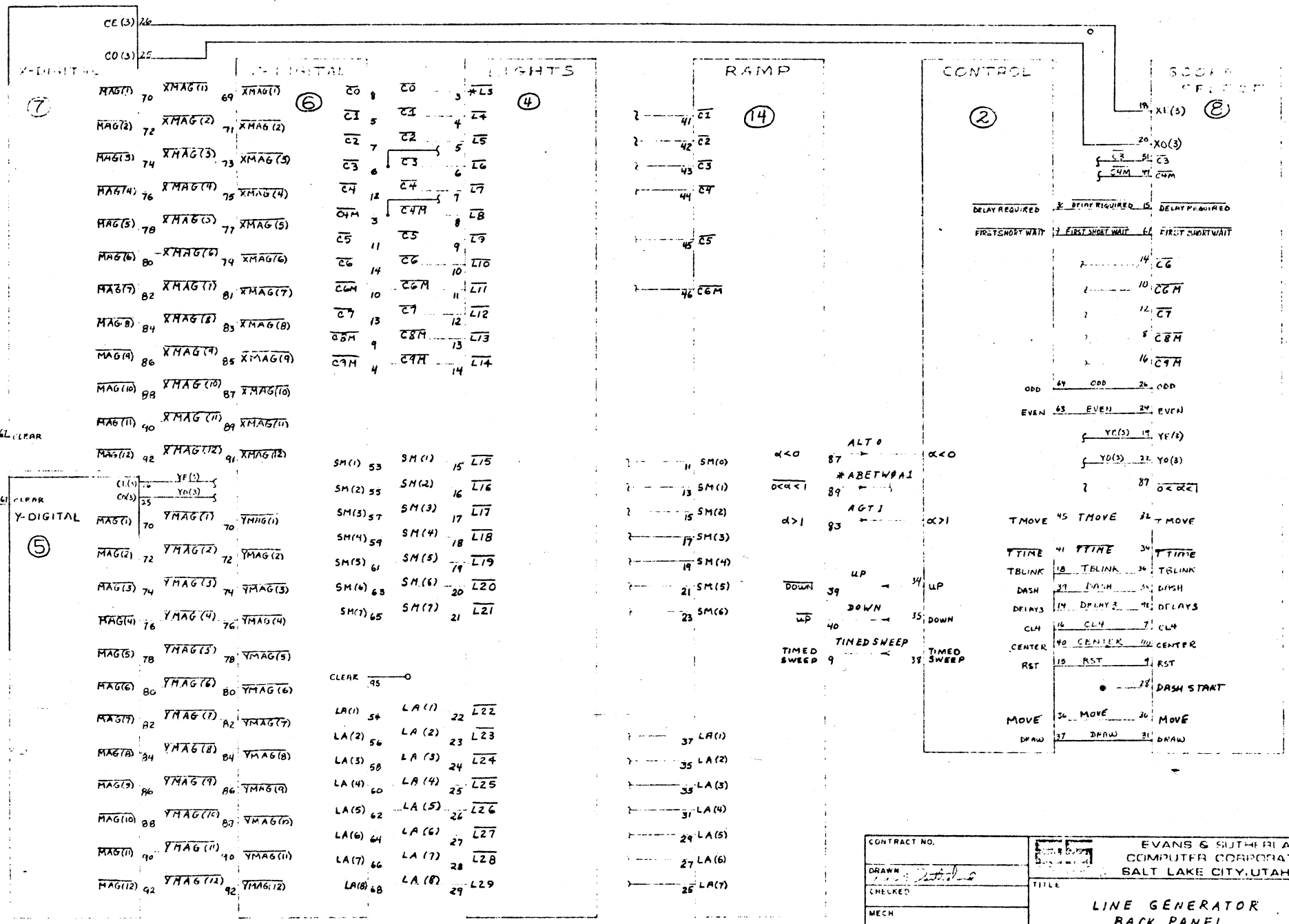
SCALE | SHEET 2 OF 6

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED



CONTRACT NO.	EVANS & SUTHERLAND COMPUTER CORPORATION SALT LAKE CITY, UTAH 84112		
DRAWN	TITLE		
CHECKED	LINE GENERATOR BACK PANEL DATA TO ANALOG CARDS		
MECH			
ELEC			
PROJ ENG			
DESIG AUTO.	C	DWG 108101-601/605	REV A
APPROVED	SCALE	SHEET 7 OF 5	



CONTRACT NO.	
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DESIG AUTO	
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EVANS & SUTHERLAND COMPUTER CORPORATION
SALT LAKE CITY, UTAH 84112

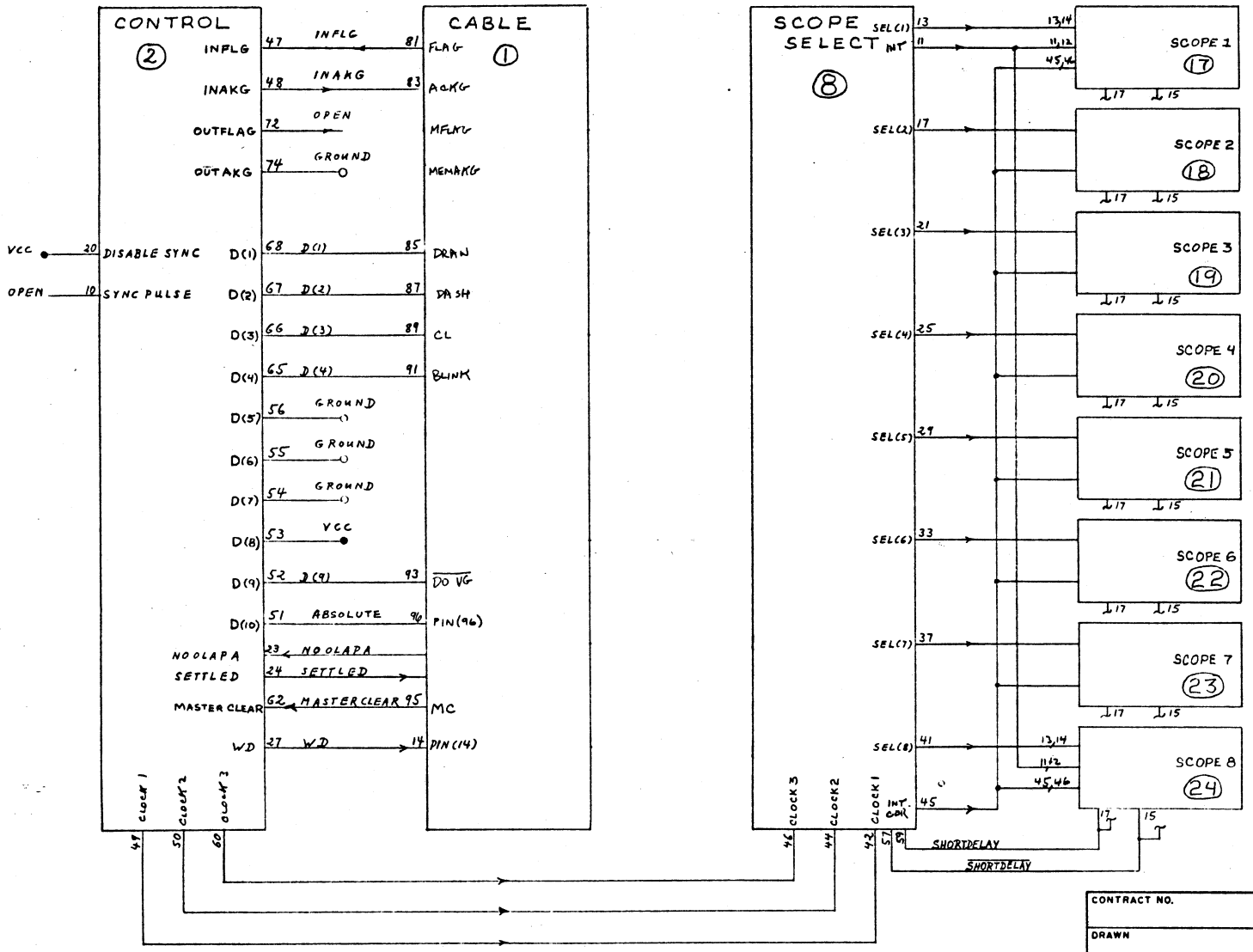
TITLE
LINE GENERATOR
BACK PANEL

C | DWG [illegible] | REV A-19

SCALE | SHEET 4 OF 6

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

PRINTED WIRES
NOT IN WIRELIST



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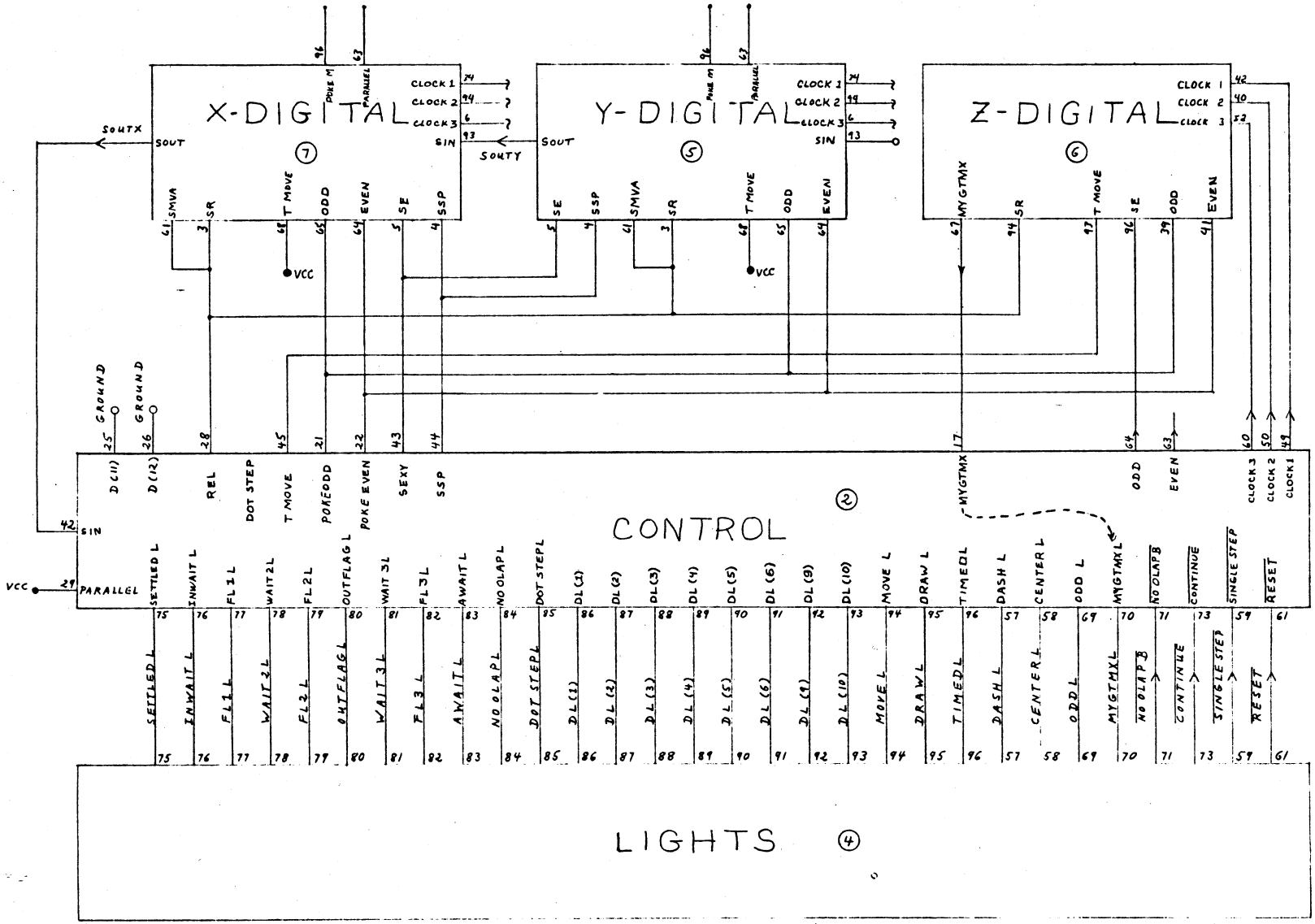
EVANS & SUTHERLAND
COMPUTER CORPORATION
SALT LAKE CITY, UTAH 84112

TITLE
LINE GENERATOR
BACK PANEL

SIZE	DWG	REV
C	108101-601/605	A-9

SCALE | SHEET 5 OF 6

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



CONTRACT NO.		EVANS & SUTHERLAND COMPUTER CORPORATION SALT LAKE CITY, UTAH 84112	
DRAWN		TITLE	LINE GENERATOR BACK PANEL CONTROL SIGNALS
CHECKED			
MECH			
ELEC			
PROJ. ENG.			
DESIG. AUTO.			
APPROVED			
	C	DWG 108101-601/605	REV A-9
	SCALE		SHEET 6 OF 6

TEST PROCEDURE

During the test of LG any time there is a need for pulling out or inserting a card power should be turned off. Let us say this applies to analog and digital boards for a few reasons.

1) Power Up

Powering up is mainly making sure that all voltages are

**********OF THE CORRECT POLARITY**********
AND VALUE.

A) Without the cards plugged in

Adjust all voltages to .Ø1 volts (for now) for ground use the ground on the back pannel where all analog grounds meet as referance for analog voltages and the digital ground for +5 digital v. Set TO 5.112 AT P.S. (V.A.)

B) Turn power off and plug in the following boards

Pattern generator or cable from the clipper.
Control 1Ø81Ø9
Sw. light 1Ø9114
X and Y Digital 1Ø81Ø3
Z Digital 1Ø81Ø4

Put the DVM probes on the digital V and power up. If the voltage has dropped more than .3 volts you have got problems. See Note 1

C) Turn off power and plug in the ramp card 1Ø81Ø8
This time check + or - 15 volt line. If those are OK check qiuet VCC.

D) Turn off power and plug in scope select 1Ø8115
this fellow uses +-15, and digital VCC.

E) Before inserting the D/A converters use an ohmmeter to check the Ohmic resistance between analog ground and the -6ØV strip on each D/A card. This needs to be done only the first time the board is being tested or if a component has been replaced.

The following table is a list of resistances for a typical board.

-60V. - Analog ground 200K
A.ground - -60V. 100ohms

-Ref. ground Short either way

-25 - ground 1 MEG
Ground - -25 20 OHMS
+ and -15 - A. ground 200K
1-Alpha and alpha ramps have very little resistance to ground.

After plugging these boards in try all the voltages. The levels should not be less than .3 volts different from original settings.

F) With all the cards plugged in adjust all voltages to the nominal levels (+ or - .01 volts or less)

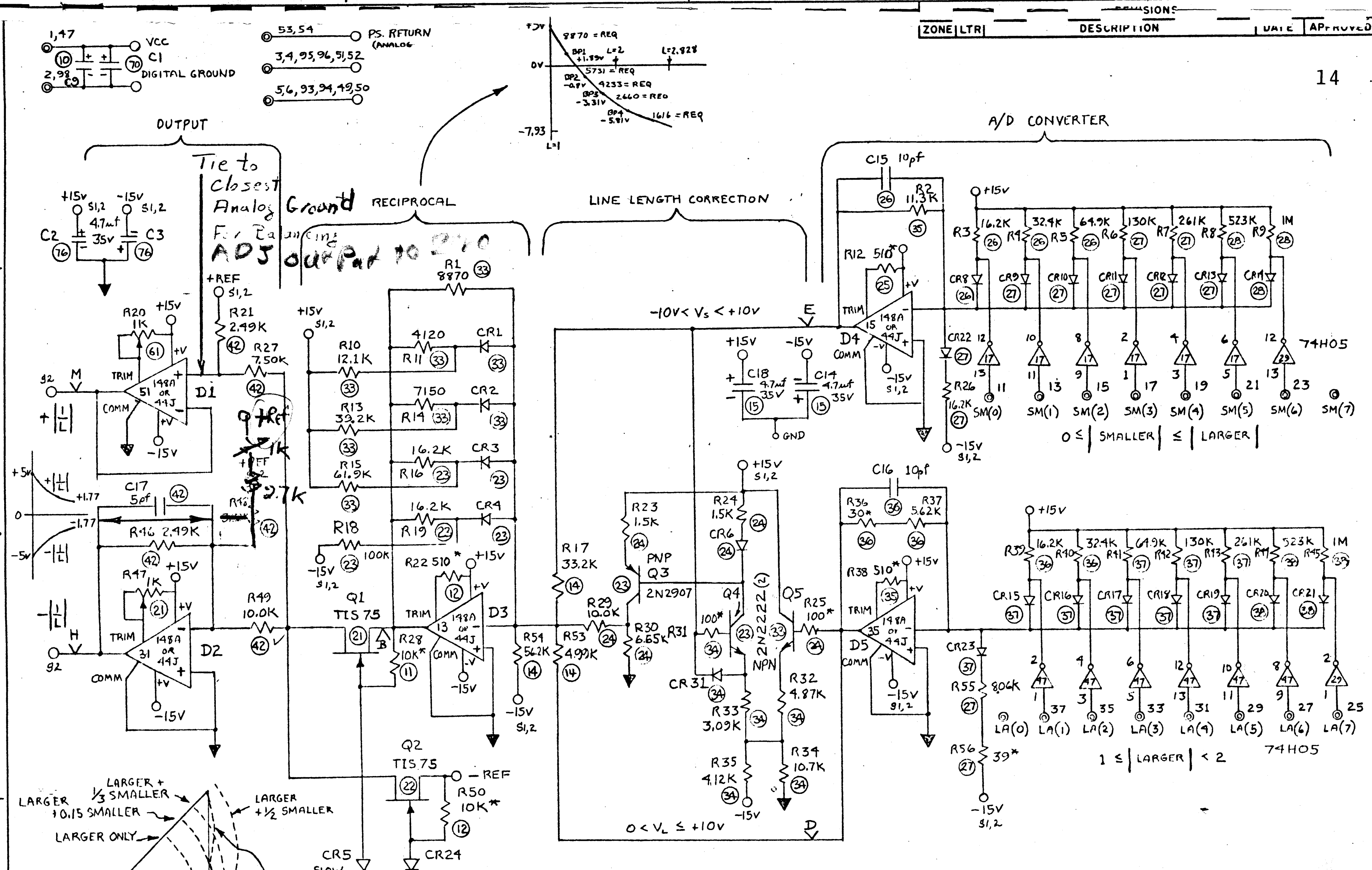
**NOTE 1 **

If at any time during test of the line generator a voltage is shorted due to a board stop test and find the short. Do not take chances because many problems may be caused. Note that the problem may not be on the board.

2) Adjusting the ramp card

Check this card for the following wrong polarity capacitors
There must be at least 12 of these. If you could not find any backwards capacitors let someone else look for them.
If there is a capacitor in backwards and the system is turned on for any appreciable amount of time the opamp associated with the capacitor may stop to serve.

The next two sheets are schematic of the ramp card 10810B-605

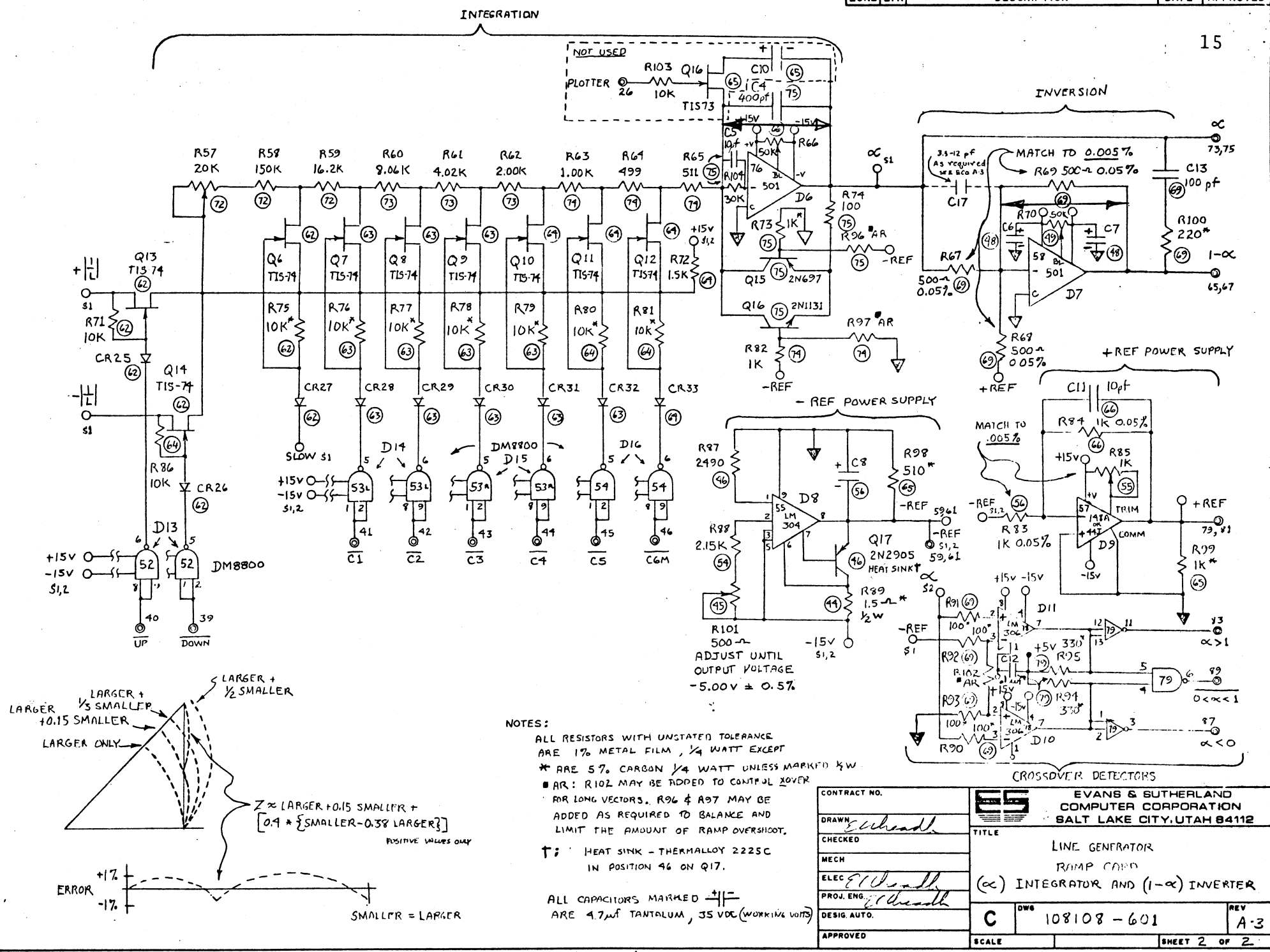


NOTE:
ALL RESISTORS 1% METAL FILM 1/4 WATT EXCEPT
* IS 5% CARBON 1/4 WATT
ALL DIODES IN4148

-REF = 5.00 V±1%
STABLE TO 0.1%

CONTRACT NO.	EVANS & SUTHERLAND COMPUTER CORPORATION SALT LAKE CITY, UTAH 84112
DRAWN	TITLE: LINE GENERATOR RAMP CARD LINE LENGTH ESTIMATOR
CHECKED	
MECH	
ELEC	
PROJ. ENG.	
DESIG AUTO.	C — DWG 108103-601 — REV A-3
APPROVED	SCALE — SHEET 1 OF 2

ZONE	LTR	DESCRIPTION	DATE	APPROVED



NOTES:

ALL RESISTORS WITH UNSTATED TOLERANCE ARE 1% METAL FILM, ¼ WATT EXCEPT

* ARE 5% CARBON ¼ WATT UNLESS MARKED ½W

■ AR: R102 MAY BE ADDED TO CONTROL XOVER FOR LONG VECTORS. R96 & A97 MAY BE ADDED AS REQUIRED TO BALANCE AND LIMIT THE AMOUNT OF RAMP OVERSHOOT.

†: HEAT SINK - THERMALLOY 2225C IN POSITION 46 ON Q17.

ALL CAPACITORS MARKED ⊣|⊢ ARE 4.7μf TANTALUM, 35 VDC (WORKING VOLTS)

CONTRACT NO.	
DRAWN	E Uhrenholdt
CHECKED	
MECH	
ELEC	E Uhrenholdt
PROJ. ENG.	E Uhrenholdt
DESIG. AUTO.	
APPROVED	

EVANS & SUTHERLAND COMPUTER CORPORATION
SALT LAKE CITY, UTAH 84112

TITLE

LINE GENERATOR
RAMP CORD
(α) INTEGRATOR AND (1-α) INVERTER

C	DWG 108108-601	REV A-3
SCALE		SHEET 2 OF 2

Four Opamps need to be zeroed out (input offset set to zero)

These four are
(Page 1) D1 and D2

(Page 2) D6 and D7

All except D1 can be adjusted by shorting the input through the output** and adjusting the output to less than .2 Mvolts of its respective ground.

D1 is a follower and should be adjusted by grounding the +input and setting the output to zero

** note that in setting the offset for D6 the input compensation network (IE 30K and 10 PF) must be considered a part of the Opamp.

****** If you cannot zero any one opamp for any reason there may be one of the following reasons

Bad Pot
Wrong value pot
Pot leads not soldered
Amp leads not soldered
Bad Amp
Amp Oscilating
If the last one is the case you are in trouble. Check the frequency of oscilation and if it is high (around 10 MHZ) chances are a small capacitor at the output will help out. (See note 2)
At any rate this is really the classic case of Engineer vs. unstability.

Note 2

If the frequency of oscilation is too high chances are that the wire that is being used as a short is too long. To verify this you can put a 100PF capacitor in parallel with the short and see if the oscilation stops. If this is the case Zero the opamp and don't worry anymore. Ever.

3) Testing the control sequence.

** For this part of the test only, the following cards are not needed

Scope select
X,Y, and X D/A
Scope Driver

To start the test input a pattern that is fairly simple.

Preferably a move draw command. Note the following.

The LG is never used in relative mode and therefore the REL light must be off. If it is not refer to cable pin 96 (absolute 1.96) or the control card (sheet 5 of 1Ø81Ø9-6Ø1/6Ø5 B2).

Try to stay away from dash, center, or timed modes at this stage they will just add to the confusion.

The drawing on the next page (1Ø8114=1Ø1 S1) (This will be refered to as the maintenance pannel in this write up)
Shows the lights and their respective names.

For this part of the test the system should be put in single step and nooverlap mode.

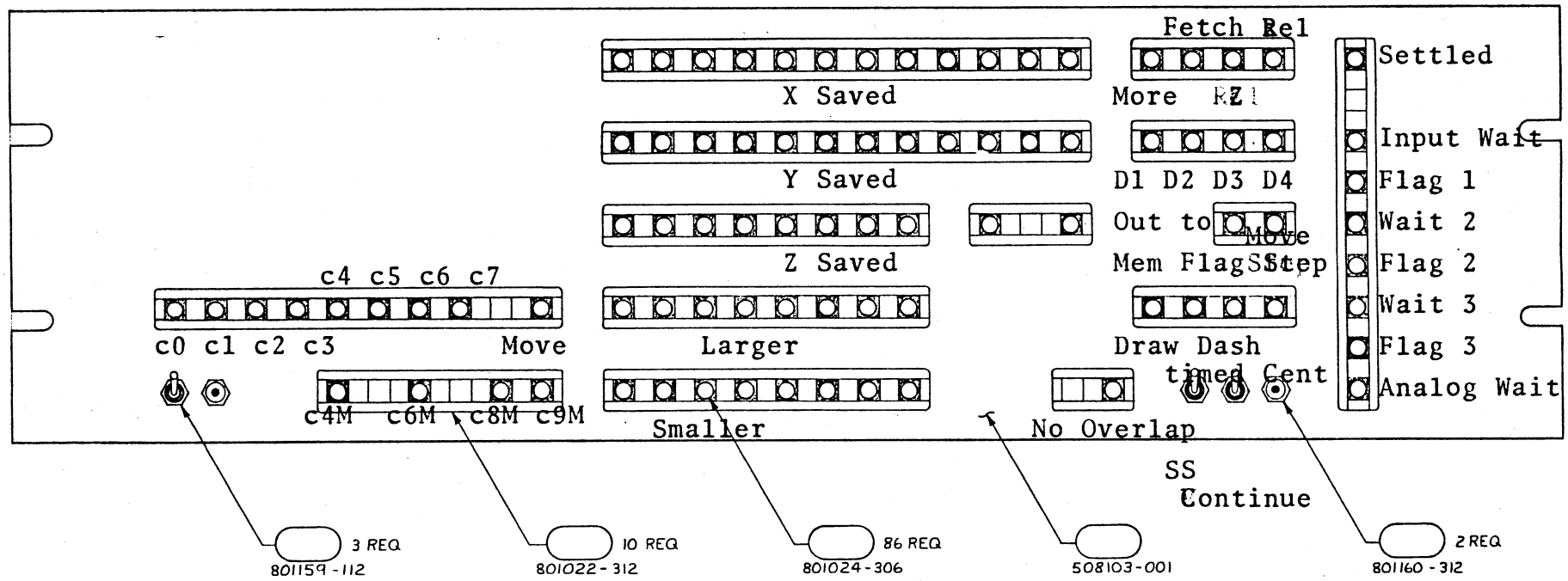
A reset should put us in wait state.

The system must single step through as shown in the state chart.

The control card only receives a flag from the cable and two flags from the ramp card (pages 1 and 4 of 1Ø81Ø9-6Ø1). As a result if it does not leave wait state or not return to it chances are that the other guys are not flagging.
A case where 32 or 33 on the back pannel are held low is shown.

** It is adviseable to check the values of R & C's on the control card against the guzzinta before test.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



NOTES:

1. INSTALL THE TOGGLE AND PUSH BUTTON SWITCHES MOUNTED ON THE BOTTOM OF THE PANEL WITH THE FLAT PART OF THE SHAFT TOWARD THE TOP OF THE PANEL.
2. INSTALL WHITE PLASTIC SLEEVES ON ALL TOGGLE SWITCHES.
3. INSTALL RED PLASTIC SLEEVE ON THE PUSHBUTTON SWITCH.

CONTRACT NO.	EVANS & SUTHERLAND COMPUTER CORPORATION SALT LAKE CITY, UTAH 84112
DRAWN R Flygare 11-6-70	TITLE: LINE GENERATOR
CHECKED Hess Mannings 11-9-70	PANEL ASSY, CONTROL
MECH	
ELEC	
PROJ. ENG.	
DESIG. AUTO.	
APPROVED	C DWG 108114-101 REV A1
	SCALE 1/1 SHEET 1 OF 2

Sequence ; No Overlap

	Wait State	state 1	state 2	state 3
Settled	1	0	0	0
Input Wait	1	0	1	1
Flag 1	0	1	0	0
Wait 2	1	1	0	1
Flag 2	0	0	1	0
Wait 3	1	1	1	0
Flag 3	0	0	0	1
Analog Wait	1	1	1	1

After state 3 the control card is expectin two signals from the ramp card. These signals are (alpha 1 or alpha Ø) If one of these signals is not coming through the machine will go into some undefined state. To verify that the problem is coming from the ramp card you can unseat it and try to single step the line generator. If it goes through its states the problem is in the ramp card otherwise you have to check the control card.

4) Testing the ramp

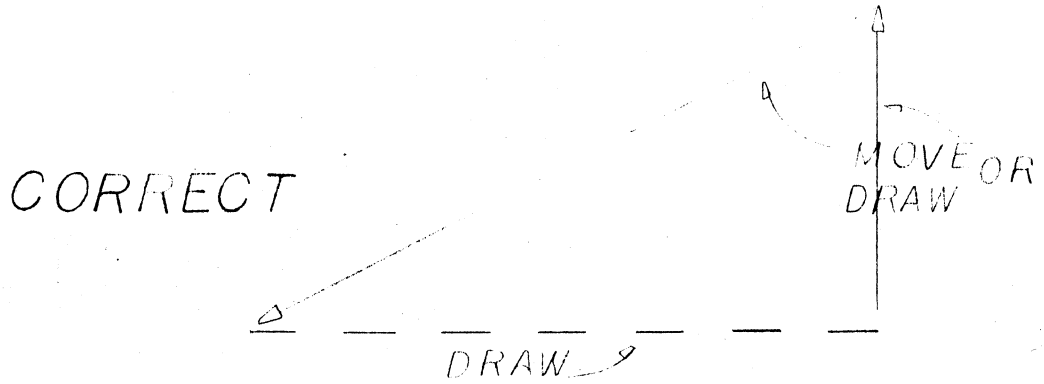
The cards X,Y, and Z digital go through card test and it is safe to believe that they are OK. (During the system test)

The ramp card generates the ramp according to the size of the SM and LA numbers. (Sheet 1 of 1Ø81Ø8-6Ø5)

A few words should be said about the operation of this card since it is the heart of the system.

The A/D converter on Page 1 is really a D/A. The operation is simple. There will be current flowing through the diodes into the opamp except for when the input to the corresponding inverter is holding the anode side of the diode low.

A 1K pot is put in series with the 2.7K resistor at the input of D2. This will change the offset level of D2 in order to get the two ramps exactly equal. The pattern on the next page is a demo of where this can be adjusted. Note that the dashed lines are drawn on alternate cycles (odd, even)

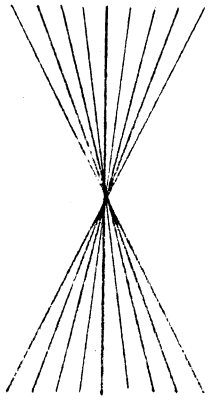


RAMPS NOT EQUAL

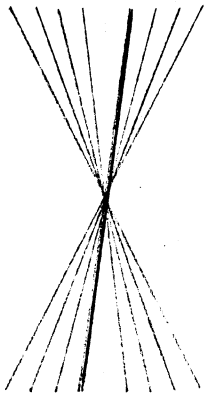
CONTRACT NO.	EVANS & SUTHERLAND COMPUTER CORPORATION SALT LAKE CITY, UTAH 84112		
DRAWN		DWG	REV
APPROVED			
APPROVED	SCALE		SHEET OF

** Note that the +ref is the output of an inverter that changes the polarity of -ref. This inverter is supplied with a trim pot (R85 1Ø81Ø8-6Ø1 sheet 2). This pot can be used to further equalize the ramps. It could be adjusted best using the pattern shown on the next page.

CORRECT



+REF. NOT ADJUSTED



CONTRACT NO.	EVANS & SUTHERLAND COMPUTER CORPORATION SALT LAKE CITY, UTAH 84112	
DRAWN		
APPROVED	DWG	REV
APPROVED	SCALE	SHEET OF

If this level is not quite right the difference between the two ramps will be observed in a group of lines that are drawn from (to) a single point.

** Note that the two TIS75 fets never get switched because the system is never used in timed mode.

The multiplying D/A converter on sheet 2 of 1Ø81Ø8-6Ø5 is a little more elaborate. The two tis 73's are used to enable or inhibit I/L or -1/L signals into the D/A. These fets are used because of their low on resistance. They should however, turn off at about the same voltage. If the off voltages are drastically different the ramps may or may not show a difference but the lines will.

Alpha Ramp must go from .7 volts to -5.7 volts. If the limits of the ramp are not close to these numbers the 1-alpha ramp will be offset in the other direction. If this is the case check the two transsistors. (2N697 and 2N1131 @75)

The LM3Ø4 and its driver the 2N29Ø5 are fairly good friends they live together and burn together. As a result if -ref is not holding steady it is not wise to change only one of the two.

** The RC network going from alpha to (1-alpha) ramps (1Ø81Ø8-6Ø1 sheet 2 D-1) is a fix.
The test engineer is allowed
to change the values of 22Ø ohms and 1ØØ PF to some other values if the finds necessary.

** The test engineer is also allowed to put a lead network on the (1-alpha) amp by putting a 7.5 capacitor across R67.
The effect of this capacitor will become observable in a star pattern.

5) Testing the D/A's

The X and Y D/A's (1Ø811Ø) accept 12 pairs of bits and output an analog signal that is between Ø and -1Ø volts.

There are also two deglitching signals that are used to keep the oupt quiet while the numbers are changing size (such as a transition from A 3 to 4 or 7 to 8 etc.)

Two voltage levels are generated on each card (+4.3 and -25 volts). It is adviseable that these levels are checked before the test begins.

Four analog signals are introduced to the card (alpha, 1-alpha ramps; -ref and analog ground). It is important to make sure that the D/A is not loading any one of these signals.

** It is adviseable that the 1-alpha ramp be checked when a D/A card is plugged in for the first time. This will reflect any distortion that may be introduced into the alpha ramp as well as 1-alpha.

Sheets 1 and 2 of 1Ø811Ø-6Ø1 are shown.

ZONE	LTR	DESCRIPTION	DATE	APPROVED
		ISION		

REPRESENTS NUMBERS 1 TO 5; LOCATION FOR COMPONENTS FOR LADDER DRIVER 8A1 ARE NEAR (13), (23), (33), (43) OR (53)

SEE SHEETS 2 & 3 FOR LADDER DRIVER DETAIL

59,61 −REF
65,67 1−α
73,75 α
56-82 (EVEN NOS) ANALOG GROUND

IE(1) IO(1) IE(2) IO(2) IE(3) IO(3) IE(4) IO(4) IE(5) IO(5) IE(6) IO(6) IE(7) IO(7) IE(8) IO(8) IE(9) IO(9) IE(10) IO(10) IE(11) IO(11) IE(12) IO(12)

1A1 2A1 3A1 4A1 5A1 6A1 7A1 8A1 9A1 10A1 11A1 12A1

−REF 1−α α −REF

RESISTANCE VALUES FOR R1 TO R24 ARE MEASURED TO 0.01 % AND VALUES FOR D/A NETWORK ARE PICKED BY COMPUTER PROGRAM. FET RESISTANCE IS MEASURED WITH GATE SHORTED TO SOURCE AND FETS FOR DRIVERS ARE SELECTED BY COMPUTER PROGRAM.

R1 19.98K R2 19.98K R3 19.98K R4 19.98K R5 19.98K R6 19.98K R7 19.98K R8 19.98K R9 19.98K R10 19.98K R11 19.98K R12 19.98K

19.98 RESISTORS ARE 19.978K TO COMPENSATE FOR FET RESISTANCE OF 22 Ω. THE MANUFACTURER FOR THESE PRECISION RESISTORS MUST BE VISHAY.

R14 10.00K R15 10.00K R16 10.00K R17 10.00K R18 10.00K R19 10.00K R20 10.00K R21 10.00K R22 10.00K R23 10.00K R24 10.00K R13 19.98K

1A2 2A2 −REF −REF

160.0K R25 IR(4) 690.0K R26 IR(6)

C1 5pf
R27 18.7K
+15V
510 TRIM R28 5%
148A or 741 OUT COMM
−15V R31
R30 18.7K
18.7K
R29 18.7K
−REF
OPAMP S1
SIGNAL GND S1
P.S. RETURN

EQUIVALENT RESISTANCE = 10K

EQUIVALENT RESISTANCE = 10K ‖ 160K ‖ 640K = 9.27536 K

OUTPUT VOLTAGE DIFFERENCE VARIES BETWEEN +4.675 VOLTS AND −4.675 VOLTS VALUES COMPUTED FOR −REF = 5.00 VOLTS

95,96 +15V → S1,2 +15V
C2 4.7μf 35 VDC
PS RETURN 53,54 P.S. RETURN
C3 4.7μf 35 VDC
−15V 93,94 → S1,2 −15V

DEGLITCH CIRCUIT

OP AMP S1
Q1 TIS-73
R39 10K
R35 10K
C7 200pf
LM 302
220 Ω 5%
83,84 SIGNAL OUTPUT
85,86 SIGNAL GND S1
CR4 IN4148
DEGLITCH CLOCK 89
DEGLITCH 87
R36 1K

Vcc (+5VDC) 1 → +5V
C1 4.7μf 35 VDC
CR2 IN4148
+4.3V S2
LOGIC GND 2
C5 4.7μf 35 VDC
LOGIC GROUND
+15V 3,4 → +15V (TO DRIVER (1) CIRCUITS ONLY)

−15V 5,6 → −15V
CR1 IN3020
CR3 IN4148
R33 6.8K ½W
−60V 47,48 → −60V
4.7μf 50VDC C6
−25V
P.S. RETURN 54
P.S. RETURN

NOTE: RESISTOR TOLERANCE IS INDICATED BY NUMBER OF DIGITS. FOR EXAMPLE:
10.00K IS 0.1% METAL FILM, ¼W
10.0 K IS 1% METAL FILM, ¼W
10K IS 5% METAL FILM, ¼W
EXCEPT WHEN MARKED OTHERWISE

CONTRACT NO.	
DRAWN	T. Heath
CHECKED	
MECH	
ELEC	T. Heath
PROJ. ENG.	T. Heath
DESIG. AUTO.	
APPROVED	

EVANS & SUTHERLAND COMPUTER CORPORATION
SALT LAKE CITY, UTAH 84112

TITLE
LINE GENERATOR
(X OR Y) D/A CONVERTER
LADDER NETWORK AND DEGLITCH CKT

C | DWG 108110 − 601 | REV

SCALE | SHEET / OF 3

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

28

DRIVER SUBASSEMBLY A1

NOTE: INTEGRATED CIRCUITS GROUNDED TO LOGIC LEVEL GROUND ONLY
USE SN7400N
SEE SHEET 3

USE SN7400N SEE SHEET 3

IE(n) IO(n) { DRIVEN BY XE(n) XO(n) OR YE(n) Yo(n) }

+5V S1 +4.3V S1 +15V S1 (FOR DRIVER (D) CIRCUITS ONLY)

TOP BOTTOM MIDDLE

R101-112 1K R113-124 1K
R125-136 1K R137-148 1K
R149-160 1K R161-172 1K
R173-184 1K
R185-196 6.81K* 1%

NOTE: PIN DATA FOR TIS73

SOURCE (S) DRAIN (D) GATE (G)

BOTTOM VIEW

2N2907 Q101-112 Q113-124 Q125-136 Q137-148

ANALOG GND 56-82 (EVEN NOS)

-25V CR101-112 CR113-124 CR125-136

TIS73 Q149-160

-25V CR137-148 CR149-160 CR161-172

TIS73 Q161-172

-25V CR173-184 CR185-196 CR197-208

TIS73 Q173-184

-25V CR209-220 CR221-232 CR232-244 CR12

TIS73 Q185-196

68.1K* 1% R197-208 R209-220 R221-232 R233-244

S1 -60V

-REF

0 ∝ 1-∝

0V -8V -16V -24V ±500 NS -25.8V

IO & IE BOTH HIGH APPLIES -REF
IO ONLY HIGH APPLIES ∝
IE ONLY HIGH APPLIES 1-∝

10K/20K LADDER NETWORK

DRIVER SUBASSEMBLY A2

+15V S1 (FOR DRIVER (D) CIRCUITS ONLY)

R303-304 6.81K* 1%

R301-302 4.7K 2N2907 2N2907 +4.3V 1K R305-306

Q301-302 Q303-304

IR(n) DRIVEN BY XR(n) or YR(n)

1K R307-308 -25V CR305-306 -REF

CR313-314 R309-310 22K LOGIC GND CR307-308 CR309-310 CR311-312 CR303-304 CR301-302

Q305-306 TIS73 ANALOG GROUND

TIS73 Q307-308

R311-312 68.1K* 1% R313-314 68.1K* 1%

S1 -60V

IR(n) HIGH APPLIES -REF

160K/640K 0.01%

IE(n) IO(n) A1 A2 -REF 1-∝ ∝ -REF IR(n)

SWITCH EQUIVALENT CIRCUITS

ALL RESISTORS 5% FILM 1/4 WATT EXCEPT AS MARKED *

ALL DIODES ARE 1N4148

CONTRACT NO.	
DRAWN	E Church
CHECKED	
MECH	
ELEC	E Church
PROJ. ENG.	E Church
DESIG. AUTO.	
APPROVED	

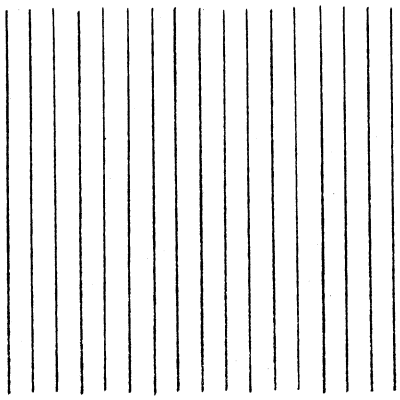
EVANS & SUTHERLAND COMPUTER CORPORATION
SALT LAKE CITY, UTAH 84112

TITLE
LINE GENERATOR
(X OR Y) D/A CONVERTER
LADDER DRIVER SUBASSEMBLYS A1 & A2

C DWG 108110-601 REV

SCALE SHEET 2 OF 3

BASIC PATTERN FOR TESTING D/A'S



X HIGH ORDER BITS

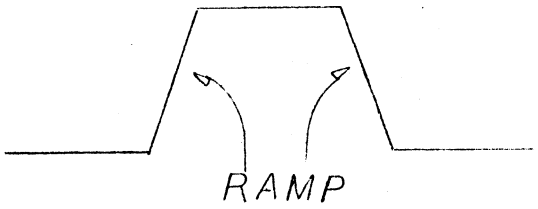
GND

-REF

LOW ORDER BITS

GND

-REF



CONTRACT NO.	EVANS & SUTHERLAND COMPUTER CORPORATION SALT LAKE CITY, UTAH 84112	
DRAWN	DWG	REV
APPROVED		
APPROVED	SCALE	SHEET OF

Note that the fet's are symmetric and in that sense they are all used in similar manner.

Also note that the 29Ø7 transistors are connected in a pseudo differencial configuration and therefore Q137-148 will turn on only if all other transistors in their corresponding rows are off.

A suggested pattern for testing the X D/A is shown on the next page. A similar pattern could be used for Y.

The output of each bit is taken on the fet side of the 19.98 K resistors.

If the D/A card passes this test it is almost home. A number of other patterns should be tried and in a failing case the problem can be traced to its source by noting the frequency of occurance of the problem in one cycle. For example in the above pattern if the lines are bad in half of the scope and OK in the other half it is obvious that the most significant bit is not working right.

A supplement to this manual will be available that has a number of patterns and their respective signifance listed.

The Z D/A

The Z D/A is similar to X and Y D/A's except in a few points.

The output opamp has a gain of 1 therefore the output levels are ground to -ref.

No reencoding is done here.

There are only 8 Z bits.

The same procedure can be used to test this card with the exception that the output will not be observable as easily on the scope.

It is adviseable that the output of the Z D/A studied carefully with an osiloscope.

6) Scope Select Card

This card takes care of the dash and center dash sequences.

There is a mecl oscilator on this card that generates a 5Ø mhz sine wave that is run through a bunch of flip flops to get down to some reasonable frequency.

With any luck this setup will be redesigned sometime soon. So don't sweat it.

The parts of this that are important to note follow the scope select logic can be checked easily by grounding one of the "IN" inputs and making sure that the corresponding "Sel" follows.

The signal intcor should be checked as a function of the line length. (refer to 1Ø8115-6ØØ sheet 3)

If the output of X and Y D/A's are noisy the deglitch logic may be failing.

7) The scope drivers.

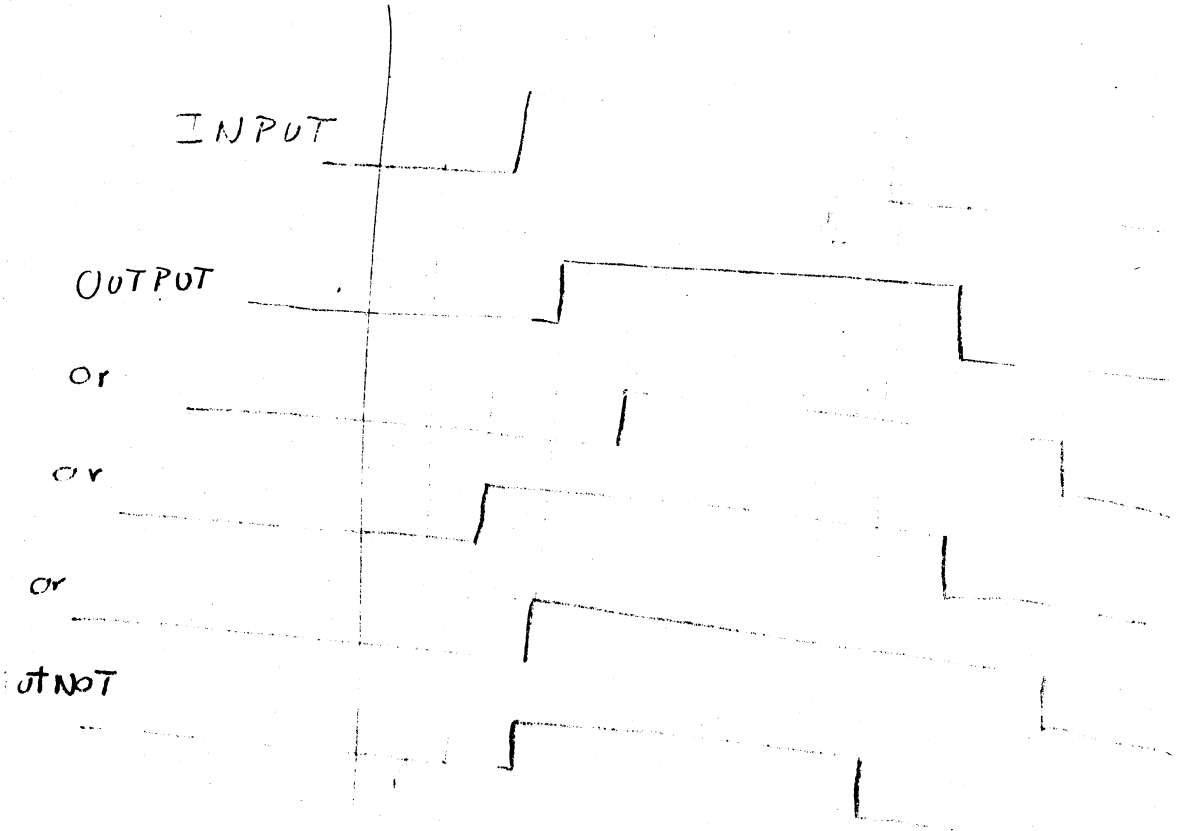
ECO A-1 on Mho's Memo on What to do untill Cheadle comes.

Setting the tabs on the scope driver.

The scope driver (108 113) has two delay lines that are used to compensate for the length of the cable between the Line generator and the scope and also for the delay (if any) of the scope yoke with respect to its video amplifier.

The INTENSIFIER signal (logical product of Select and Intensify) is fed into a delay line and there are 20 taps available from the delay line.

The delay line enables us to delay the start point of the' input signal or to lengten it or both. The circuit does not allow shortening the signal in any way



The circuit that makes this magic possible is the transisitor pair (Q4,Q5 or Q6,Q7) .

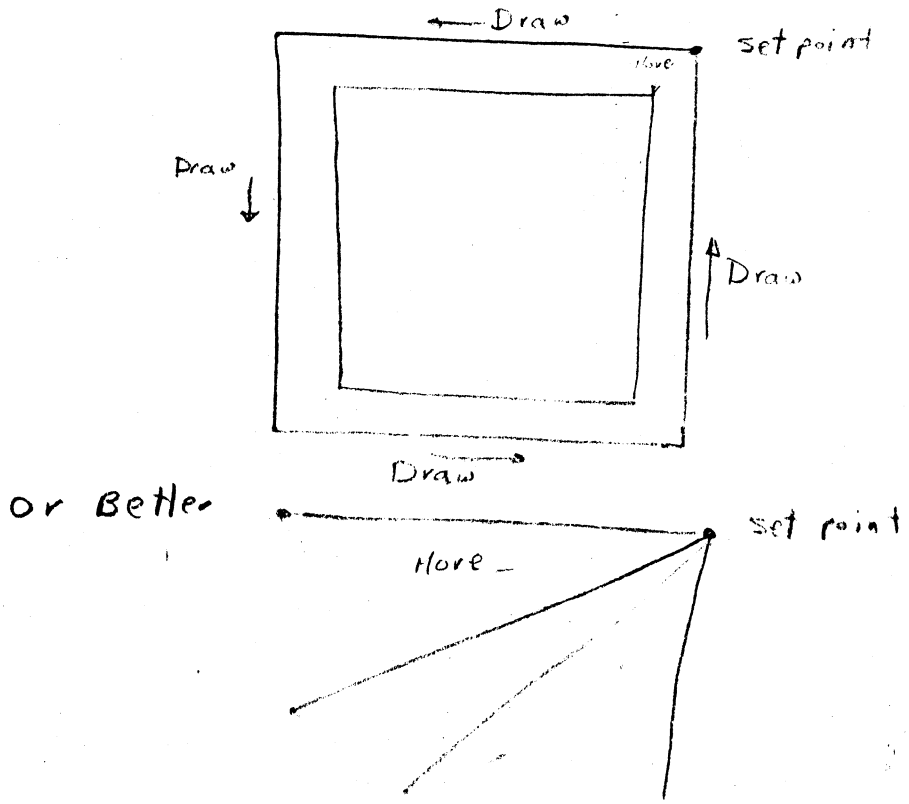
A decision was made sometime after the first system to treat the short vectors defferent therefore there are two transistor pairs and four tap connectors available. For any line ,however, only one of the pair is used.

When the intensifier signal is on the tap connector that is closest to the input will determine the begining of the line. Note that the two tap connectors are symmetric and therefore the first transistor that is turned on will start the line.

On the other hand the second tap, the one further down the line, will stay on longer and therfore the end point is determined by this one.

This results in the following procedure for setting these taps.

Connect both wires together and find the best starting point for the lines (staps for short lines and Ltaps for long ones) the following pattern is recommanded



Once the starting point of the line is found the end can be extended if necessary.

NOTE

This is not going to be quite so easy so the Prophet suggests trying to center the lines first. That means that if you are showing the squares tie the two taps together and try to find the best picture (which means that the lines may not quite meet but they are off the same from both sides) Then move the two taps away from each other hence changing the begining and the end of the lines simultaneously.

If more delay is required it will be evident when you are following the procedure but if the thing acts like nothing you have seen before check and see if the Unblank cable is terminated properly.

~~OVERLAP~~ WITH OVERLAP

① Stopped on 1004

② S. Stepped 9 times
a) Data into Layer & Smaller
b) C2, move, Settled, input wait, Wait 2, Wait 3, Analyze } all on

③ Stepped 1 time
a) Settled went out
b) odd value, ~~D(1)~~ on
c) new layer & smaller
d) C1, input wait, wait 2 are on

④ Stepped 11 times
a) D(1) out, odd out
b) C2 on, input wait & Flag 2 on

⑤ Stepped Once
a) D(1), Flag 1 on
b) Flag 2 still on
c) input wait out

⑥ Stepped 29 times a) Channel looks up
b) LG same as above

Stat settled, input wait, wait 2, wait 3, analog wait } on

NO OVERLAP

(1) Skipped 9 times
- a) b(1) out
- b) c(2) on c(1) out
- c) none on
- d) data into Lower & Smaller

(2) Skipped once
- a) b(1) on
- b) settled out
- c) wait 3, ~~analog~~ wait out
- d) odd values on
- e) c(1) on, c(2) off
- f) 2 saved ~~on~~ data

(3) Skipped 28 times
- a) channel Catch Lock up

(4) reset once

before: input wait, wait 2 } on

~~after~~ during: wait 2, wait 3, analog wait } on

after: input, wait 2 } on

reset again: settled, W2, AW, input, W3, C4M, C6M, C8M, C9M } all on