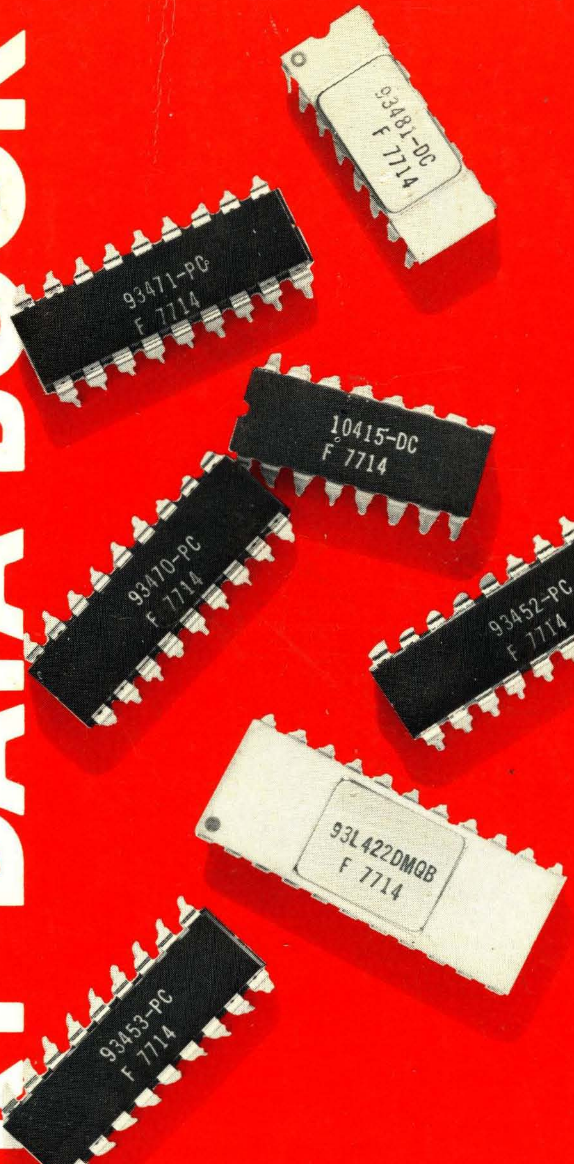
BIPOLAR MEMORY DATA BOOK

$3.00



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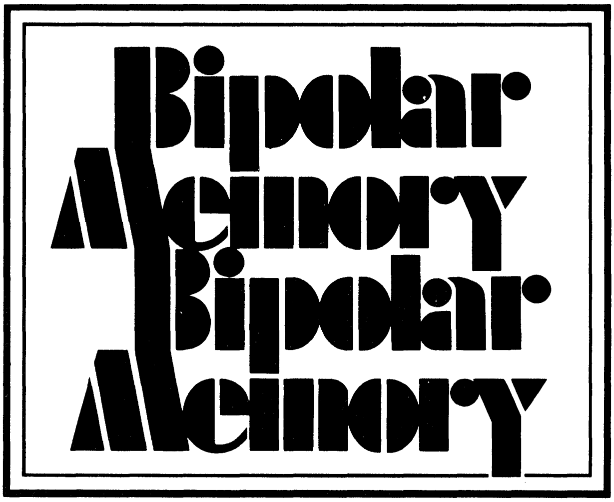

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CHAPTER 1

- Introduction

Chapter 1
INTRODUCTION

At one time, bipolar memories were relegated to a very restricted list of applications. Their bit density was quite low, while their power consumption per bit and their price per bit were quite high. Their only advantage was speed; they were used only where speed was required at any cost.

Today's bipolar memories are still fast but other factors have changed in a most dramatic way. Density has surged to 8K bits per package for ROMs and 4K for RAMs. Power density has tumbled spectacularly. For the popular 1K TTL RAM, for example, power density is below 0.5 mW per bit for the standard version and less than 0.2 mW per bit for the low power version; their respective access times of 25 and 35 ns are still on a downward trend.

And what about prices? System designers' acceptance has led to high volume production, while continuing advances in technology and design innovation have brought chip sizes down to MSI levels. These factors have brought prices down well below 1¢ per bit. Combine this low component cost with the advantages of having the same power supply and I/O characteristics as the logic circuits and the system cost savings are very impressive.

The combination of speed, efficiency, cost effectiveness and design flexibility have made bipolar memories the standards by which other memories are compared.

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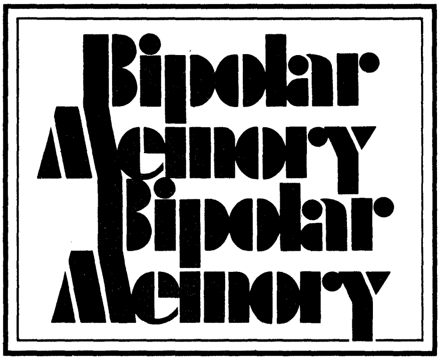

CHAPTER 2

- Numerical Index of Devices

Chapter 2
NUMERICAL INDEX OF DEVICES

DEVICE	DESCRIPTION	PAGE
ECL STATIC MEMORIES		
F100414	256 x 1 Bit Fully Decoded Random Access Memory	7-3
F100415	1024 x 1 High Speed Random Access Memory	7-8
F100416	256 x 4 Programmable Read Only Memory	7-40
F10145A	16 x 4 Random Access Memory	7-12
F10405	128 x 1 Random Access Memory	7-16
F10410	256 x 1 Random Access Memory	7-20
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F10415A	1024 x 1 High Speed Random Access Memory	7-35
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TTL STATIC MEMORIES		
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93411	256 x 1 Random Access Memory – Open Collector Outputs	7-50
93411A	256 x 1 High Speed Random Access Memory – Open Collector Outputs	7-50
93L412	256 x 4 Low Power Random Access Memory – Open Collector Outputs	7-56
93412	256 x 4 Fully Decoded Random Access Memory – Open Collector Outputs	7-61
93L415	1024 x 1 Low Power Random Access Memory – Open Collector Outputs	7-65
93415	1024 x 1 Random Access Memory – Open Collector Outputs	7-70
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93L420	256 x 1 Low Power, High Speed Random Access Memory – 3-State Outputs	7-83
93L421	256 x 1 Low Power Random Access Memory – 3-State Outputs	7-89
93421	256 x 1 Random Access Memory – 3-State Outputs	7-95
93421A	256 x 1 High Speed Random Access Memory – 3-State Outputs	7-95
93L422	256 x 4 Low Power Random Access Memory – 3-State Outputs	7-101
93422	256 x 1 Fully Decoded Random Access Memory – 3-State Outputs	7-107
93L425	1024 x 1 Low Power Random Access Memory – 3-State Outputs	7-113
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93425A	1024 x 1 High Speed Random Access Memory – 3-State Outputs	7-120
93427	256 x 4 Schottky Programmable Read Only Memory – 3-State Outputs	7-125
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93436	512 x 4 Schottky Programmable Read Only Memory – Open Collector Outputs	7-130
93438	512 x 8 Schottky Programmable Read Only Memory – Open Collector Outputs	7-132
93441	512 x 4 Schottky Read Only Memory – 3-State Outputs	7-135
93442	512 x 8 Schottky Read Only Memory – 3-State Outputs	7-136
93446	512 x 4 Schottky Programmable Read Only Memory – 3-State Outputs	7-137
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93450	1024 x 8 Programmable Read Only Memory – Open Collector Outputs	7-143
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93453	1024 x 4 Schottky Programmable Read Only Memory – 3-State Outputs	7-144
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93458	16 x 48 x 8 Field Programmable Logic Array – Open Collector Outputs	7-153
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CHAPTER 3

- RAMs, PROMs, ROMs Selection Guide
- Bipolar Memory Selection Guide by Function
- Bipolar Memory Cross Reference
- Fairchild MOS Memory Product Guide
- MOS Memory Product Cross Reference

RAMs, PROMs, ROMs SELECTION GUIDE

WORDS	BITS PER WORD				
	1	2	4	8	9
16	16	32	RAM 10145A		
32		64	128		
64			256		RAM 93419 576
128	RAM 10405		512		
256	RAMs 10410 10411 93L420 10414 93L421 100414 93421/93421A 93411/93411A 93410/93410A		1024 RAMs 93L412/93L422 93412 93422 ROMs 93457/93467 PROMs 93417/93427 10416 100416		
512			2048 ROMs 93431/93441 PROMs 93436/93446	ROMs 93432/93442 PROMs 93438/93448	
1024	RAMs 93415/93415A 93L415 93L425 93425/93425A 10415/10415A 100415		4096 PROMs 93452/93453	ROMs 93454/93464 PROMs 93450/93451	
2048			8192	16384 ROMs	
4096	RAMs 93481 93470/93471 10470			32768	

Numbers on shaded lines indicate overall complexity.

BIPOLAR MEMORY CROSS REFERENCE

Pin-for-Pin Equivalents except if otherwise noted.

AMD	FSC
AM27LS00	93L420
AM27S10	93417
AM27S11	93427
AM27S40	93432
AM27S41	93442
AM27S80	93454
AM27S81	93464
93415A	93415A
93415	93415
93425A	93425A
93425	93425
93L415	93L415

INTEL	FSC
3106	93421
3107	93411
3301	93457
3302	93431
3304	93432
3322	93441
3324	93442
3601	93417
3602	93436
3604	93438
3605	93452
3621	93427
3622	93446
3624	93448
3625	93453

INTERSIL	FSC
IM53S08	93454
IM53S18	93464
IM5508A	93415A
IM5508	93415
IM5518A	93425A
IM5518	93425
IM5523A	93421A
IM5523	93421
IM5533A	93411A
IM5533	93411
IM5603A	93417
IM5603	93417
IM5604	93436
IM5605	93438
IM5623	93427
IM5624	93446
IM5625	93448

*Functional replacement

HARRIS	FSC
HM7610	93417
HM7611	93427
HM7620	93436
HM7621	93446
HM7640	93438
HM7641	93448
HM7642	93452
HM7643	93453
HPROM1024	93417
HPROM1024A	93427

MMI	FSC
5200/6200	93457
5201/6201	93467
5205/6205	93431
5206/6206	93441
5240/6240	93432
5241/6241	93442
5280/6280	93454
5281/6281	93464
5300/6300	93417
5301/6301	93427
5305/6305	93436
5306/6306	93446
5340/6340	93438
5341/6341	93448
5350/6350*	93452
5351/6351*	93453
5530/6530	93411
5531/6531	93421
5555/6555	93419
10149	10416

MOTOROLA	FSC
MCM4004	93457
MCM10144	10410
MCM10145	10145A
MCM10146	10415
MCM10147	10405
MCM10149	10416

NATIONAL	FSC
DM7573/8573	93417
DM7574/8574	93427
DM7595/8595	93432
DM7596/8596	93442
DM7597/8597	93467
DM8582	93411

NATIONAL	FSC
DM54/74187	93457
DM54/74S200	93421
DM54/74S206	93411

SIGNETICS	FSC
82S09	93419
82S10	93415
82S11	93425
82S16	93421
82S17	93411
82S115*	93448
82S116	93421A
82S117	93411A
82S126	93417
82S129	93427
82S130	93436
82S131	93446
82S136	93452
82S137	93453
82S140	93438
82S141	93448
82S215*	93442
82S226	93457
82S229	93467
82S230	93431
82S231	93441
82S280	93454
82S281	93464
54/74S200	93421
54/74S201	93421
54/74S301	93411
10145	10145A
10149	10146
93415A	93415A
93425A	93425A

TI	FSC
SN10144	10410
SN10145	10145A
SN10147	10405
SN54/74187	93457
SN54/74S201	93421
SN54/74S209	93425
SN54/74S287	93427
SN54/74S301	93411
SN54/74S309	93415
SN54/74S387	93417
SN54/74S472*	93448
SN54/74S473*	93438
SN54/74S470*	93436
SN54/74S471*	93446

PRODUCT CODE CROSS REFERENCE

MANUFACTURER	TEMPERATURE RANGES		PACKAGES		
	MILITARY −55°C to +125°C	COMMERCIAL 0°C to +70°C	CERAMIC DIP	PLASTIC DIP	FLATPAK
Advanced Micro Devices (AMD)	XXXM	XXXC	D	P	F
Fairchild Semiconductor (FSC)	XXXXM	XXXXC	D	P	F
Harris Semiconductor	XXX-2	XXX-5	1	–	9
Intel	MXXX	–	D or C	P	F
Intersil	XXXM	XXXC	DE	PE	FE
Monolithic Memories (MMI)	5XXX	6XXX	D/J	N	F
Motorola	105XX/106XX	101XX/102XX	L	P	F
National	54XXX/7XXX	74XXX/8XXX	D/J	N	F/W
Signetics	SXXX	NXXX	F/I	B/N	Q
Texas Instruments (TI)	54XXX	74XXX	J/JE	N	W

All package designation are suffixes with the exception of Harris and Intel.

BIPOLAR MEMORY SELECTION BY FUNCTION

PART NO.	ORGAN-IZATION	OUT-PUTS	ACCESS TIME (TYP) ns	ACCESS TIME 0 to 70°C MAX, ns	ACCESS TIME −55 to +125°C MAX, ns	POWER DISS. (TYP) mW	PKG. (Note 1)	TEMP. (Note 2)	NO. OF PINS	DATA PAGE NO.
TTL RAMs										
9410	16 x 4	3S	35	–	–	375	D,P	C,M	18	7-199
93419	64 x 9	OC	35	45	60	725	D	C,M	28	7-78
93410	256 x 1	OC	45	60	70	450	D,F,P	C,M	16	7-45
93410A	256 x 1	OC	35	45	–	450	D,P	C	16	7-45
93411	256 x 1	OC	45	55	65	475	D,F,P	C,M	16	7-50
93411A	256 x 1	OC	40	45	–	475	D,P	C	16	7-50
93L420	256 x1	3S	40	45	55	275	D,F,P	C,M	16	7-83
93421	256 x 1	3S	35	50	60	475	D,F,P	C,M	16	7-95
93421A	256 x 1	3S	30	40	–	475	D,P	C	16	7-95
93L421	256 x 1	3S	45	90	100	275	D,F,P	C,M	16	7-89
93412	256 x 4	OC	35	45	60	475	D,F,P	C,M	22**	7-61
93L412	256 x 4	OC	45	60	75	250	D,F	C,M	22**	7-56
93422	256 x 4	3S	35	45	60	475	D,F,P	C,M	22**	7-107
93L422	256 x 4	3S	45	60	75	250	D,F	C,M	22**	7-101
93415	1024 x 1	OC	30	45	60	475	D,F,P	C,M	16	7-70
93415A	1024 x 1	OC	25	30	–	475	D,P	C	16	7-70
93L415	1024 x 1	OC	35	60	70	200	D,F,P	C,M	16	7-65
93425	1024 x 1	3S	30	45	60	475	D,F,P	C,M	16	7-120
93425A	1024 x 1	3S	25	30	–	475	D,P	C	16	7-120
93L425	1024 x 1	3S	35	60	70	200	D,F,P	C,M	16	7-113
93470	4096 x 1	OC	35	–	–	800	D,P	C	18	7-160
93471	4096 x 1	3S	35	–	–	800	D,P	C	18	7-160
93481□	4096 x 1	3S	90	120	–	50/350	D,P	C	16	7-166
93481A□	4096 x 1	3S	90	100	–	50/350	D,P	C	16	7-166
ECL RAMs										
10145A	16 x 4	–	6.5	9	–	500	D,F	C	16	7-12
10405	128 x 1	–	11	15	–	470	D,F	C	16	7-16
10410	256 x 1	–	18	30	–	475	D,F,P	C	16	7-20
10411	256 x 1	–	20	35	–	360	D,F,P	C	16	7-25
10414	256 x 1	–	7	10	–	500	D,F	C	16	7-30
100414	256 x 1	–	7	10	–	500	D,F	C	16	7-3
10415	1024 x 1	–	20	35	–	475	D,F	C	16	7-35
10415A	1024 x 1		12	20	–	475	D,F	C	16	7-35
100415	1024 x 1	–	12	20	–	500	D,F	C*	16	7-8
10470	4096 x 1	–	25	–	–	900	D,F	C	18	7-41
TTL ROMs										
93457	256 x 4	OC	25	45	60	425	D,F,P	C,M	16	7-153
93467	256 x 4	3S	25	45	60	425	D,F,P	C,M	16	7-159
93431	512 x 4	OC	30	50	60	475	D,F,P	C,M	16	7-128
93441	512 x 4	3S	30	50	60	475	D,F,P	C,M	16	7-136
93432	512 x 8	OC	35	55	70	650	D,F,P	C,M	24	7-129
93442	512 x 8	3S	35	55	70	650	D,F,P	C,M	24	7-137
93454	1024 x 8	OC	30	45	60	550	D,F,P	C,M	24	7-150
93464	1024 x 8	3S	30	45	60	550	D,F,P	C,M	24	7-156
TTL PROMs										
93417	256 x 4	OC	25	45	60	425	D,F,P	C,M	16	7-75
93427	256 x 4	3S	25	45	60	425	D,F,P	C,M	16	7-125
93436	512 x 4	OC	30	50	60	475	D,F,P	C,M	16	7-130
93446	512 x 4	3S	30	50	60	475	D,F,P	C,M	16	7-138
93438	512 x 8	OC	35	55	70	650	D,F,P	C,M	24	7-133
93448	512 x 8	3S	35	55	70	650	D,F,P	C,M	24	7-141
93452	1024 x 4	OC	35	–	–	650	D,F	C,M	18	7-145
93453	1024 x 4	3S	35	–	–	650	D,F	C,M	18	7-145
ECL PROMs										
10416	256 x 4	–	15	–	–	500	D,F	C	16	7-40
100416	256 x 4	–	15	–	–	500	D,F	C	16	7-40
TTL FPLA										
93458	16x48x8	OC	35	–	–	–	D	C,M	28	7-154
93459	16x48x8	3S	35	–	–	–	D	C,M	28	7-154
TTL LIFOs										
9406	16 x 4	3S	–	–	–	500	D,P	C	24	7-188
TTL FIFOs										
9403	16 x 4	3S	–	–	–	575	D,P	C	24	7-174
9423	64 x 4	3S	–	–	–	750	D,P	C	24	7-203

Note 1: D = Ceramic DIP, F = Flatpak, P = Plastic DIP
Note 2: M = Mil. Temp. Range −55 to +125°C, C = Commercial Temp. Range 0 to +70°C. (Plastic DIP available only in Comm. Temp. Range).

*100K ECL "C" Temperature Range 0°C to +85 °C. **24-Pin in Flatpak. □I^{3}L Dynamic RAM

Ordering Information – An example order code is 93415DC for the 1024 x 1-Bit TTL Ram where "D" is for Ceramic DIP package and "C" is for Comm. Temp. Range 0 to +70°C. The same part in a Flatpak and the Mil. Temp. Range would be 93415FM.

FAIRCHILD MOS MEMORY PRODUCT GUIDE

RANDOM ACCESS MEMORIES SELECTION MATRIX

PART NO.	BIT CAPACITY	ORGANIZATION	ACCESS TIME	PKG/TEMP*	STATIC/DYNAMIC
2102	1024	1024 x 1	1000 ns	DC,DL,DM	Static
2102-2	1024	1024 x 1	650 ns	DC,DL,DM	Static
2102-1	1024	1024 x 1	450 ns	DC,DL,DM	Static
2102F	1024	1024 x 1	350 ns	DC,DL,DM	Static
2102FL	1024	1024 x 1	250 ns	DC	Static
2102L2**	1024	1024 x 1	650 ns	DC	Static
2102L1**	1024	1024 x 1	450 ns	DC	Static
2102LF**	1024	1024 x 1	350 ns	DC	Static
3542	1024	1024 x 1	150 ns	DC	Static
3542-2	1024	1024 x 1	120 ns	DC	Static
3539	2048	256 x 8	650 ns	DC	Static
3539-2	2048	256 x 8	500 ns	DC	Static
3539-1	2048	256 x 8	400 ns	DC	Static
4096-5	4096	4096 x 1	350 ns	DC,DL,FL	Dynamic
4096-4	4096	4096 x 1	300 ns	DC,DL,FL	Dynamic
4096-3	4096	4096 x 1	250 ns	DC,DL,FL	Dynamic
4096-2	4096	4096 x 1	200 ns	DC,DL,FL	Dynamic

ROMs AND CHARACTER GENERATORS

3515	512 x 8 (4096-Bit) ROM
3257	64 x 5 x 7-Output ASCII Font C.G.
3258	64 x 7 x 5-Output ASCII Font C.G.
3260	64 x 9 x 7-Output ASCII Font C.G.

FIRST-IN FIRST-OUT MEMORY (FIFO)

3341	64 x 4-Bit
3351	40 x 9-Bit

SHIFT REGISTERS

CCD450	1024 x 9-Bit Dynamic
CCD460	16,384-Bit Laram
3342	Quad 64-Bit Static
3347/3357	Quad 80-Bit Static
3348	Hex 32-Bit Static with Buffer Enable
3349	Hex 32-Bit Static

*DC = Ceramic DIP/Commercial (0°C to +70°C)
DL = Ceramic DIP/Limited Military (−55°C to +85°C)
DM = Ceramic DIP/Military (−55°C to +125°C)
FL = Flatpak/Limited Military (−55°C to +85°C)

**Low Power Versions

MOS MEMORY PRODUCT CROSS REFERENCE

Competitor	Competitor Part No.		Fairchild Part No.	Equivalency*
AMD	2812	32 x 8-Bit FIFO	3351	F
	2813	32 x 9-Bit FIFO	3351	F
	2841	64 x 4-Bit FIFO	3341A	P
	3341	64 x 4-Bit FIFO	3341/3341A	P
	9102	1024 x 1-Bit Static RAM	2102	P
Intel	1403/4	1024 x 1-Bit Dynamic Shift Register	CCD450	F
	2102	1024 x 1-Bit Static RAM	2102	P
	2107A/2107B	4096 x 1-Bit Dynamic RAM	4096	F
	2104	4096 x 1-Bit Dynamic RAM	4096	P
	2416	16,384-Bit Dynamic Shift Register	CCD460	F
Mostek	2302	64 x 5 x 7 Character Generator	3257	P
	2500	512 x 8 (4096-Bit) ROM	3514/3515	F
	2600	512 x 8 (4096-Bit) ROM	3514/3515	P
	4096	4096 x 1-Bit Dynamic RAM	4096	P
	4102	1024 x 1-Bit Static RAM	2102	P
	5002/5007	Digital Voltmeter	3814/3815	F
	1007	Quad 80-Bit Dynamic Shift Register	3347/3357	P
	4006/8/9	1024 x 1-Bit Dynamic RAM	2102	F
	4027	4096 x 1-Bit Dynamic RAM	4096	P
National	1403/4	1024 x 1-Bit Dynamic Shift Register	CCD450	F
	2102	1024 x 1-Bit Static RAM	2102	P
	3705	8-Bit Multiplexer	3705/3708	P
	5233	512 x 8 (4096-Bit) ROM	3514/3515	P
	5316	Digital Clock Chip	3817	P
Signetics	2504	1024 x 1-Bit Dynamic Shift Register	CCD450	F
	2518	Hex 32-Bit Static Shift Register	3349	P
	2530	512 x 8 (4096-Bit) ROM	3514	F
	2532	Quad 80-Bit Static Shift Register	3347/3357	P
	2602	1024 x 1-Bit Static RAM	2102	F
T.I.	3112/3122	Hex 32-Bit Static Shift Register	3348	P
	3120/3409	Quad 80-Bit Static Shift Register	3347/3357	P
	3121/3417	Quad 64-Bit Static Shift Register	3342	P
	4024	64 x 9-Bit FIFO	3351	F
	4030/4060	4096 x 1-Bit Dynamic RAM	4096	F
	4033	1024 x 1-Bit Static RAM	2102	P
Western Digital	1502	40 x 9-Bit FIFO	3351	F
AMI	3514	512 x 8-Bit ROM	3515	P
	4006/8/9	1024 x 1-Bit Dynamic RAM	2102	F
	1998	Digital Clock Chip	3817	P

*F = Functional Equivalent
P = Pin-for-Pin Equivalent

Bipolar Memory
Bipolar Memory

Bipolar Memory Bipolar Memory

CHAPTER 4

- Impact of Process Technology on Bipolar Memory Characteristics
- Memory Cell
- Input Characteristics
- Output Characteristics
- Timing Parameters
- Read Mode
- Write Mode
- Reliability
- References

Chapter 4
GENERAL CHARACTERISTICS

IMPACT OF PROCESS TECHNOLOGY ON BIPOLAR MEMORY CHARACTERISTICS

Perhaps the most important characteristics of a memory chip are the number of bits, the speed capability , the power dissipation and the capability of being produced economically. In early bipolar memory chips, the number of bits was severely restricted by both chip area, for economical production, and by the power required to operate as usable speeds. These restrictions were eased dramatically by the Isoplanar (I, II) processes, developed by Fairchild and announced in 1971. A 1K TTL RAM, not even practical with conventional processes at that time, was introduced in 1972. Its physical size has been reduced 50% through continued development, as indicated in *Figure 4-1*. Performance has also been improved, since the address access time has been cut in half.

Figure 4-2 compares a conventional Planar* transistor with Isoplanar and Isoplanar II transistors. The Isoplanar process substitutes thermally grown oxide for the p-type diffusions that isolate active elements of conventional bipolar devices. Notice that the oxide eliminates the base-to-isolation separation required in the conventional transistor, and also allows the base and collector contact openings to abut the isolation. The area is cut in half and the reduction in parasitic capacitance reduces propagation delays.

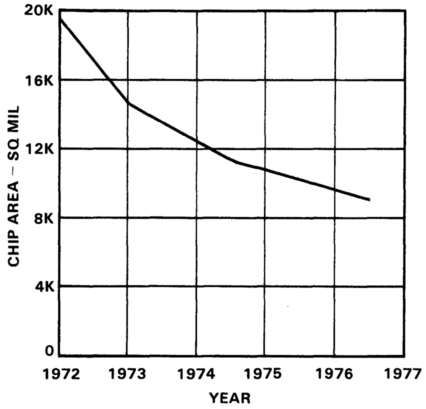

Fig. 4-1. 1K TTL RAM Die Size Evolution

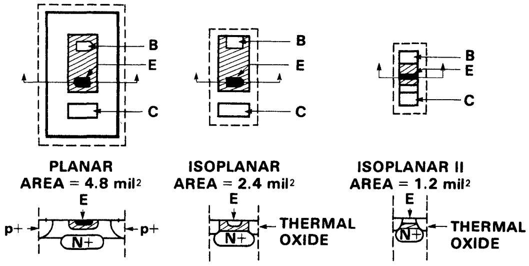

Fig. 4-2. Comparison of Geometries of Integrated Circuit Transistors using Conventional Planar* Diffused Isolation, Isoplanar Technology, and Isoplanar II Technology

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*Planar is a Fairchild patented process.

Further advances led to the Isoplanar II process, which cut the transistor area by half again and reduced parasitic capacitance even further. Isoplanar transistors have a gain-bandwidth of 5 GHz, as shown in *Figure 4-3*, which represents a factor-of-three improvement.

MEMORY CELL

Memory cell design is based on a simple cross-coupled latch, as shown in *Figure 4-4*. In the standby condition, *i.e.,* cell not addressed or chip not selected, the voltage drop across the resistors is less than a junction voltage and the diodes do not conduct. Only a few tens of microamperes flow and thus the standby power is very low. When a cell is selected, however, the diodes conduct and provide extra current to help charge stray capacitance and thus reduce propagation delays. This method of power focusing keeps the overall dissipation low and the performance high by using power only where it is needed.

The impact of Isoplanar and Isoplanar II on cell size, illustrated in *Figure 4-5*, has been even greater than on chip size. More recent developments demonstrate even greater reductions. In the 93481 4K Dynamic RAM[4], for example, the cell size is only 1 square mil. *Figure 4-6* shows this cell schematically and in cross-section. The design uses Isoplanar integrated injection logic (I^3L)™ technology, which opens up new vistas for innovative designs.

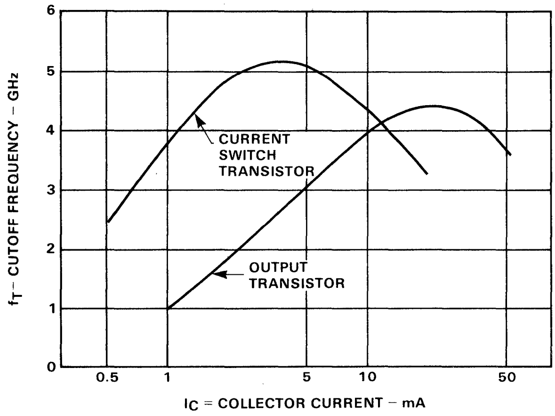


Fig. 4-3. Cutoff Frequency of Isoplanar II Transistors

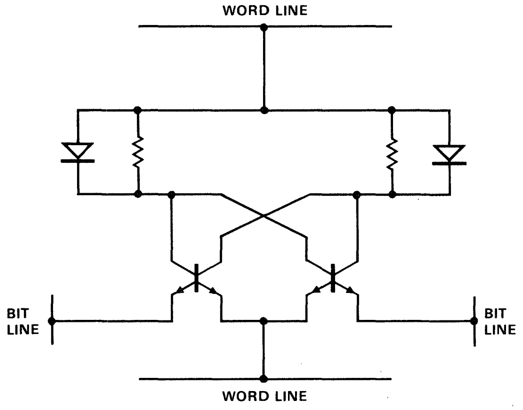


Fig. 4-4. Typical Memory Cell

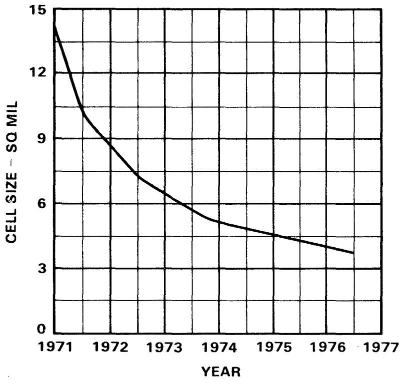
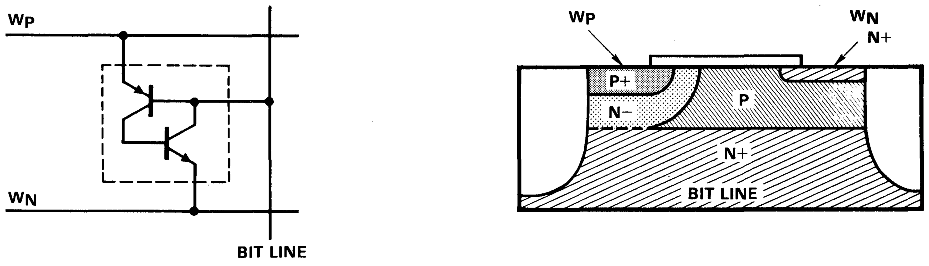


Fig. 4-5. Cell Size Evolution



a) Cell Circuit

b) Device Structure

Fig. 4-6. I3L™ Cell used on 93481 4K RAM

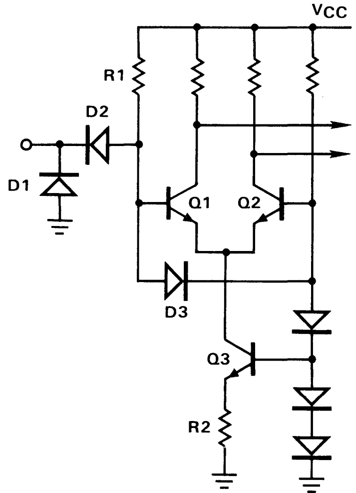


Fig. 4-7. Input TTL-to-ECL Translator

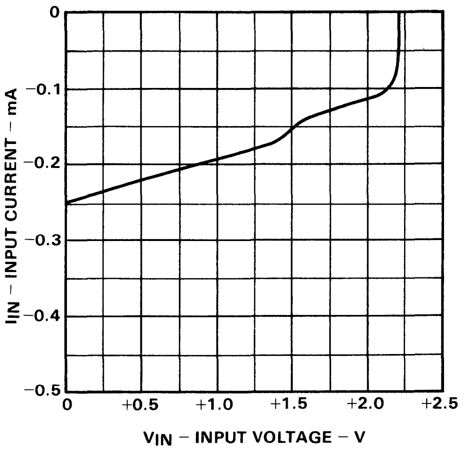


Fig. 4-8. Translator Input Characteristic Showing Threshold Break

INPUT CHARACTERISTICS

The decoding logic of bipolar memories uses ECL circuitry since this eliminates any need for gold doping to control storage time, while the relatively small voltage swing of ECL enhances the delay-power product. TTL memories use a TTL-to-ECL converter such as that shown in *Figure 4-7*. When the input signal is LOW, Q2 conducts the current from the current source transistor Q3. As the input signal rises through the 1.5 V level, Q1 collector voltage goes LOW. As the input signal goes through this transition region, there is a slight break in the input current-voltage characteristic, as shown in *Figure 4-8*. This change represents the base current required by Q1 as it turns on. This base current is a fixed amount since Q1 emitter current is fixed by Q3 and R2. Thus as the input voltage continues to rise above this transition region, the input I-V characteristic again has the slope of R1. As the input signal rises above 2.1 V, current from R1 is diverted away from D2; it starts flowing through D3 and the diode string that supplies the bias voltage for Q2 base. Those accustomed to TTL characteristics should note that the point where the input current goes to zero is not the threshold; rather, the threshold is identified by the slight break in the I-V characteristic. A clamping diode is provided on each input to limit undershoot and ringing. It is intended only for transient currents and should not be used for steady-state clamping.

OUTPUT CHARACTERISTICS

The ECL memories have emitter-follower outputs with the same characteristics as ECL logic circuits. To simplify data bussing, no pull-down resistors are used on the chip. TTL memories have either an open collector output or a 3-state output. *Figure 4-9* is a partial schematic of a 3-state output. The Q6 – Q7 Darlington provides the pull-up function for the HIGH state, while Q8 is the pull-down transistor, with Q5 providing current gain. Diode D1 clamps Q8 out of saturation. On some of the later designs, a Schottky diode is used for clamping. The pull-up and pull-down circuits are driven from the complementary outputs of the Q3-Q4 current switch, which in turn is driven by signals from the sense amplifier. In the non-selected mode, the logic of the sense amplifier turns off the pull-down transistor. To achieve the high impedance condition of the 3-state outputs the pull-up circuit is turned off by the Q1-Q2 current switch, which in turn is activated by signals derived from the Chip Select and Write Enable logic.

Diode D2 limits overshoot and ringing, and also protects Q8 from any overvoltage condition on the bus lines. An external pull-up resistor is required for the open collector output to establish the HIGH state voltage. The minimum load resistor value is determined by the current-sinking capability of the output. The maximum value is determined by the leakage currents of OR-wired outputs as well as driven inputs, which must be supplied to hold the outputs at V_{OH}. The upper and lower limits on the pull-up resistor are determined by the following equation.

$$\frac{V_{CC(min)}}{I_{OL} - FO\,(1.6)} \leqslant R_L \leqslant \frac{V_{CC(min)} - V_{OH}}{n\,(I_{CEX}) + FO\,(0.04)}$$

R_L is in kΩ

n = number of wired-OR outputs tied together

FO = number of TTL Unit Loads (UL) driven

I_{CEX} = Memory Output Leakage Current

V_{OH} = Required Output HIGH Level at Output Node

I_{OL} = Output LOW Current

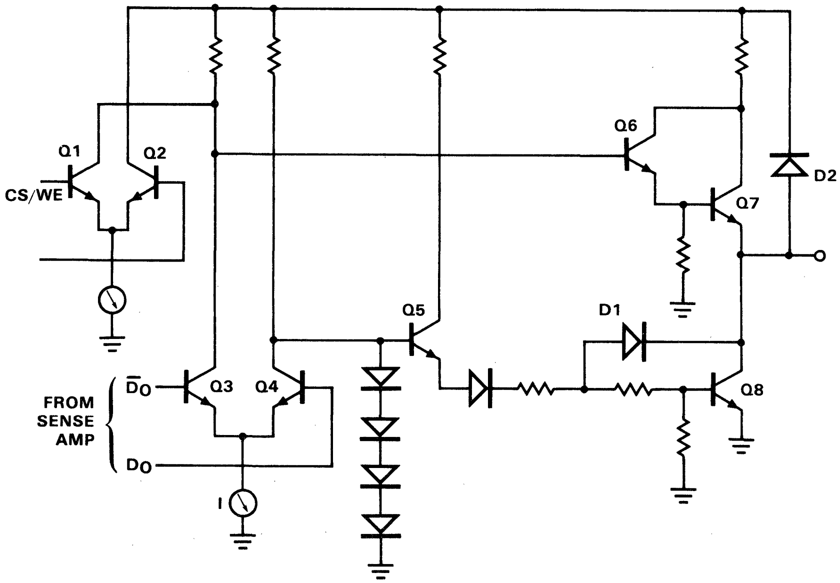


Fig. 4-9. 3-State Output and Simplified Drive Circuitry

Note that the worst-case ac parameter limits shown in the data sheets apply over the recommended operating temperature and supply voltage ranges for the various devices.

Access times of bipolar memories have proven to be quite insensitive to the pattern of stored information. Extensive investigation has shown that variations, if any, in the access time of a particular cell are related only to the status of surrounding cells or to the status of cells in the same row or column. These relationships, which were predictable, can be appreciated by considering the symbolic representations of *Figures 4-10* and *4-11*. In *Figure 4-10*, the central cell abuts eight others and there is always a possibility of crosstalk due to a random defect. The access time of a particular cell can be influenced by cells in the same row or column because of loading effects on the common drivers (see *Figure 4-11*).

From these investigations, there have evolved some very effective ac test patterns in which the access time of each cell is tested as a function of the status of cells in the same row and column and the adjacent corner cells. For an n-bit memory the number of tests is $2n\sqrt{n}$. This method has proven to be fully as effective at detecting out-of-tolerance conditions as the exhaustive method of testing each cell as a function of all other cells in the memory, *i.e.,* N^2 testing, yet consumes an order-of-magnitude less time; this is a very important cost factor in large memories.

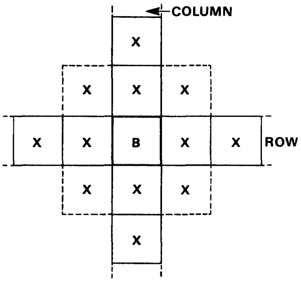


Fig. 4-10.

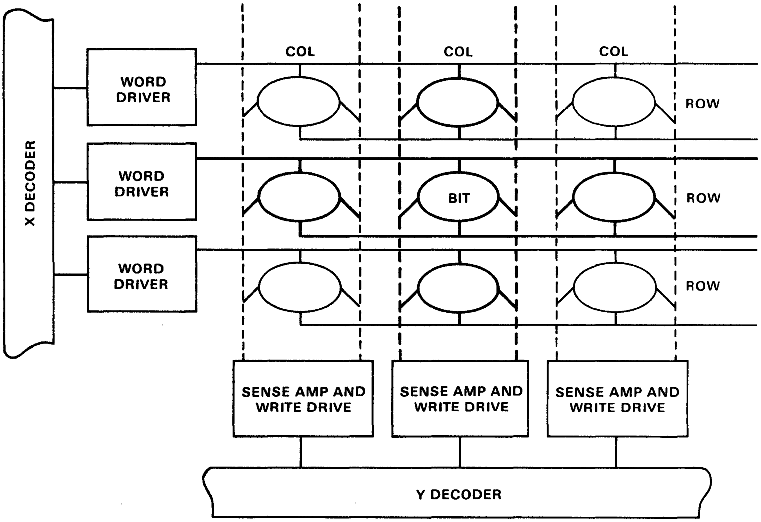


Fig. 4-11.

Read Mode

Output is guaranteed to be valid:

- t_{AA} after last address change
- t_{ACS} after beginning of Chip Select

Output is guaranteed to be inactive (open):

- t_{RCS} after end of Chip Select

WORST CASE MAXIMUM TIMES			
	93410A	93415	F10405
t_{AA}	45 ns	45 ns	15 ns
t_{ACS}	25 ns	35 ns	8 ns
t_{RCS}	25 ns	35 ns	8 ns

TIMING PARAMETERS

Since ROM and PROM parameters are the same as those of a RAM in the Read mode, a discussion of RAM parameters covers all three types. Compared to other technologies (MOS and core) the timing requirements of bipolar RAMs are very simple and can be explained in only a few statements. A RAM can be in either Read or Write mode, determined by the level on the Write Enable input. Usually a LOW level means Write, a HIGH level means Read.

READ MODE

In the Read mode, there are two important system parameters.

- Read Access Time
- Read Recovery Time

Read Access Time

Read Access Time is the time after which RAM data output is guaranteed to be valid. This time is specified as t_{AA}, address access time, and t_{ACS}, chip select access time. When the Address inputs have been stable for the worst-case (longest) value of t_{AA} and Chip Select has been active for the somewhat shorter worst-case value of t_{ACS}, the data outputs are guaranteed to represent the correct information.

Read Recovery Time

After deselect, the RAM outputs require some time to reach the inactive state; this time is called t_{RCS}, chip select recovery time. After the worst-case (longest) value of this time, the outputs are guaranteed to be inactive.

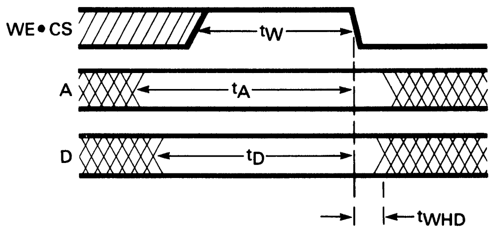
WRITE MODE

In the Write mode (Write Enable active, usually LOW) there are two different and almost independent considerations.

- The information must reliably be written into the addressed location.
- In the process of achieving this, no other locations may be disturbed.

These two considerations put separate constraints on the timing, and obviously both must be met by the system design.

Write Mode



WORST CASE MINIMUM TIMES REQUIRED			
	93410A	93415	F10405
t_W	30 ns	30 ns	8 ns
t_A	40 ns	40 ns	12 ns
t_D	35 ns	35 ns	11 ns
t_{WHD}	5 ns	5 ns	3 ns

Guarantees desired data is written into proper location.

Write Operation

The Write operation occurs during the logic AND condition of Write Enable and Chip Select. Again, Write Enable is usually active LOW and Chip Select is often a multi-input AND gate with some inputs active LOW. This WE·CS condition must last for a minimum length of time, specified as t_W, minimum required write pulse width. It does not matter in which sequence this AND condition is established, whether WE is there first and CS comes later, or vice versa, or whether they arrive or disappear simultaneously. It is the longest value of this minimum required write pulse width that is the critical, worst-case value. Unfortunately, data sheets list it in the Min column.

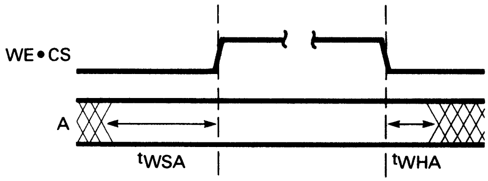
Backtracking in time from the end of the write pulse, the Address inputs must be stable for t_A and the Data input must be stable for t_D and data must also remain stable for t_{WHD}, data hold time during write, after the end of the write pulse. Obviously the data input may change during the early part of a sufficiently long write pulse. It is the data present during the final t_D of the write pulse that ends up in the addressed cell.

The second important consideration is that no other locations are unintentionally disturbed during the write operation. To guarantee this, the Address inputs must have stabilized t_{WSA}, address write set-up time, before the beginning of the write pulse, and they must remain stable for t_{WHA}, address write hold time after the end of the write pulse. This write pulse is, again, the AND condition of Write Enable and Chip Select.

Write Recovery Time

The Write Recovery Time, t_{WR}, is the period during which the outputs remain deactivated after the end of a write pulse. This recovery time is of no consequence to the system designer since it is shorter than, and hidden in, the address access time of the subsequent read operation.

Write Mode



WORST CASE MINIMUM TIMES REQUIRED			
	93410A	93415	F10405
t_{WSA}	10 ns	10 ns	4 ns
t_{WHA}	5 ns	5 ns	3 ns

Guarantees no other location is disturbed.

RELIABILITY

Accelerated stress testing of Fairchild bipolar memories, both ECL and TTL, totaling more than 12 million device hours in mid 1976, has demonstrated a failure rate of 0.29% per 1000 hours at +175°C. Using the Arrhenius[5-7] model assuming an activation energy of 1.1 eV (*Figure 4-12*), this extrapolates to a failure rate of less than 0.001% per 1000 hours at a junction temperature of +100°C. Experience in large mainframe applications is proving that the predicted low failure rates are being achieved in actual system usage.

Reliability testing started with circuits in the solder-seal ceramic package with side-brazed leads. More recently, Fairchild bipolar memories have been qualified in the glass-seal CERDIP and in the plastic DIP packages. Copies of the latest reliability reports are available from your local Fairchild representative or through Bipolar Memory Marketing, MS 20-1050, 464 Ellis Street, Mountain View, CA 94042.

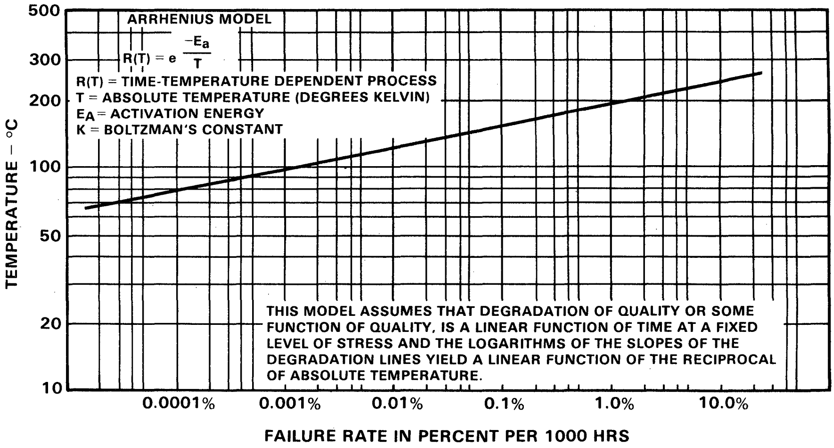


Fig. 4-12. Arrhenius Plot

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Bipolar Memory Bipolar Memory

Bipolar Memory
Bipolar Memory

CHAPTER 5

- Memory Organization
- Addressing Techniques
- General Timing Considerations
- Interface
- Micro-Control Storage using Read/Write Memory
- Buffer Memories
- Main Memories
- Conclusion
- Reference

Chapter 5

RANDOM ACCESS MEMORIES

A RAM is an array of latches with a common addressing structure for both reading and writing. A Write Enable input defines the mode of operation. In the Write mode, the information at the Data input is written into the latch selected by the address. In the Read mode, the content of the selected latch is fed to the Data output.

All semiconductor memories have non-destructive readout as opposed to the destructive readout of most magnetic core memories. With the exception of the 93481 I^3L^{TM} element, bipolar RAM operation is static, *i.e.,* the information is stored in bistable transistor cells (latches) and requires no refreshing such as required in some popular MOS RAMs using capacitor storage. Data storage in all semiconductor read/write memories is volatile; data can only be stored as long as power is uninterrupted. In contrast, a ROM offers non-volatile storage; data is retained indefinitely, even when power is shut off.

Bipolar memories are an integral part of a large number of digital equipment designs. From a tenuous beginning of 16 bits per package, bipolar RAMs have advanced to 4K bits per package. Performance figures also show an interesting comparison: the 1K TTL RAM, which has been in volume production for several years, has a typical access time of 30 ns versus 25 ns for the early 16-bit device; typical power consumption is 475 mW versus 250 mW. These remarkable advances are the reasons that bipolar memories are so widely accepted by system designers.

MEMORY ORGANIZATION

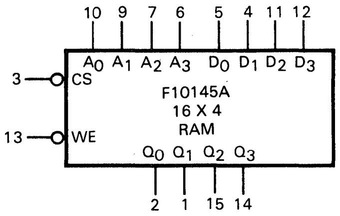
Memory subsystems are generally identified by number of words, number of bits and function. For example, a 1024 x 16 RAM is a random access read/write memory containing 1024 words of 16 bits each. Semiconductor memory device organizations follow the same rule. Since the advent of LSI allowing densities of hundreds of gates on a chip, most memory devices contain address decoders, output sensing, and various control and buffer/driver functions in addition to the array of storage cells. High density RAM devices tend to be organized n words by one bit to optimize lead usage (see logic symbols on following pages). ROM devices tend toward n words by four or eight bits to reduce cost of truth table changes.

ADDRESSING TECHNIQUES

Addressing (word selection) in a semiconductor memory subsystem consists of two parts. First, a given device or group of devices must be selected; second, a given location in a device or group of devices must be selected. Device selection may be accomplished by linear select using a binary-to-n decoder feeding the chip select function on n chips, or by coincident select using two binary-to-$\sqrt{n}$ decoders and two chip selects on each device. When n is large, linear select requires excessive hardware. For example, if $n = 64$, linear select requires four 1-of-16 decoders and a 1-of-4 decoder, or nine 1-of-8 decoders; whereas coincident selection can be accomplished with two 1-of-8 decoders with final decoding at the two input chip select gates included on the memory devices. Selection of a given location on a chip is accomplished by connecting the binary address lines directly to the chip. In summary, 64 256 x 1 RAMs in a 16K x 1-bit array using coincident selection requires 14 address lines, as follows: eight connected to 2^0 through 2^7 inputs on all chips (using necessary drivers), three feeding a 1-of-8 decoder to the CS_1 inputs, and three feeding a 1-of-8 decoder connected to the CS_2 inputs.

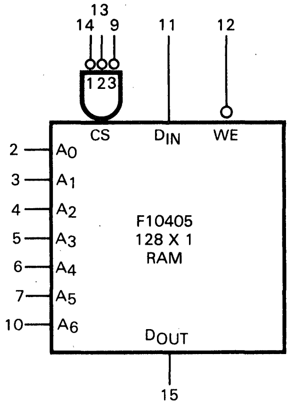
For maximum control, predictability and flexibility, an address counter should have certain characteristics—fully synchronous counting, synchronous parallel entry, a means of eliminating any ambiguity as to its mode of operation, and capability for synchronous expansion. A few examples are the 9316 and the 9LS161 for TTL; examples for ECL are the F10016 and F10136. System designers should also bear in mind that decoder outputs are subject to spikes when the inputs are changed. This can cause momentarily false Address or Chip Select signals. Memory system timing should allow for the specified maximum propagation delays for the decoders involved.

64-Bit RAM



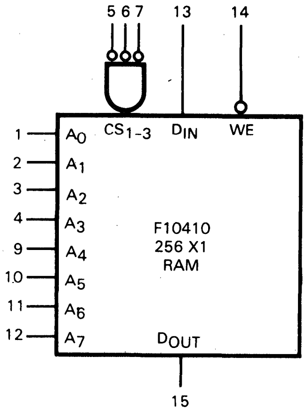
t_{AA} = 6.5 ns typ
P_D = 500 mW

128-Bit RAM



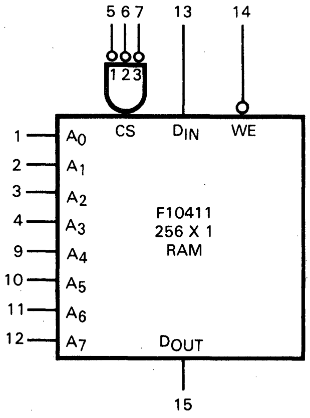
t_{AA} = 11 ns typ
P_D = 470 mW

256-Bit RAM



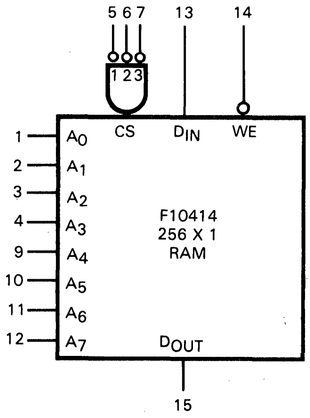
t_{AA} = 18 ns typ
P_D = 475 mW

256-Bit RAM



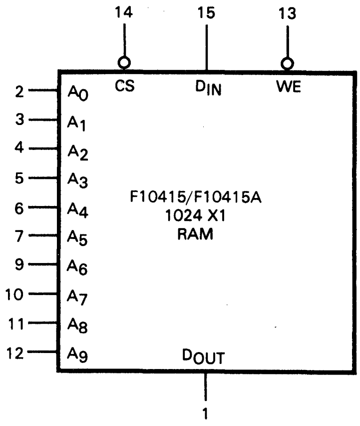
t_{AA} = 20 ns typ
P_D = 360 mW

256-Bit RAM



t_{AA} = 7 ns Typ
P_D = 475 mW

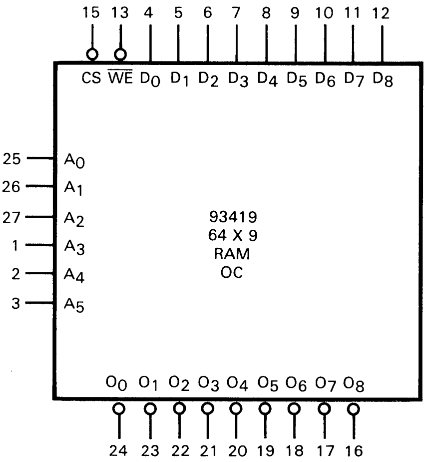
1K RAM



t_{AA} = 12/25 ns typ
P_D = 475 mW

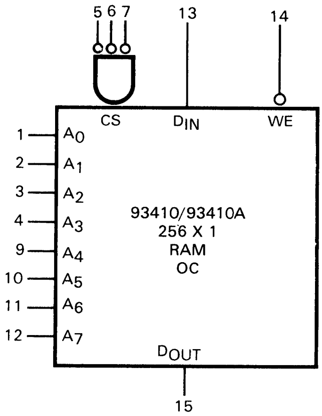
RAM Logic Symbols

576-Bit RAM



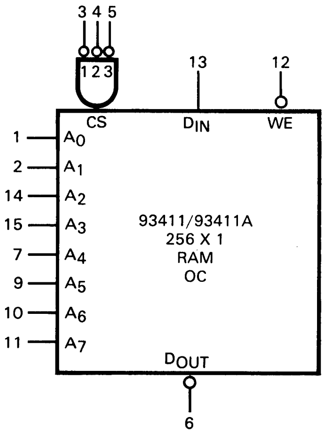
t_{AA} = 30 ns typ
P_D = 725 mW

256-Bit RAM



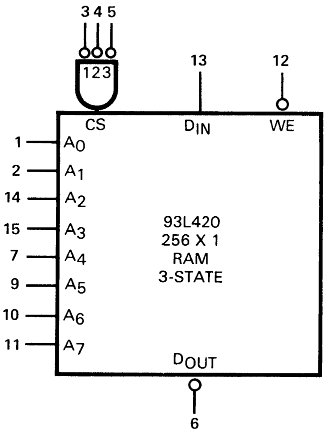
t_{AA} = 45/35 ns typ
P_D = 450 mW

256-Bit RAM



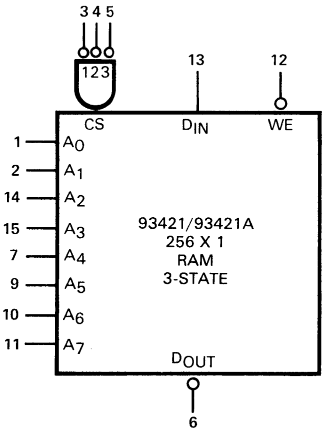
t_{AA} = 45/40 ns typ
P_D = 475 mW

256-Bit RAM



t_{AA} = 40 ns typ
P_D = 275 mW

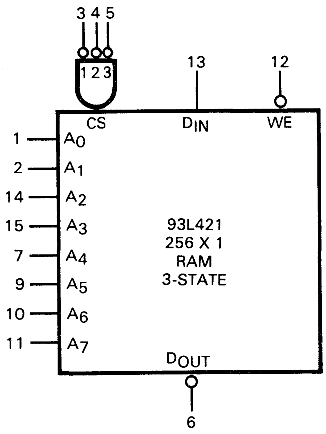
256-Bit RAM



t_{AA} = 35/30 ns typ
P_D = 475 mW

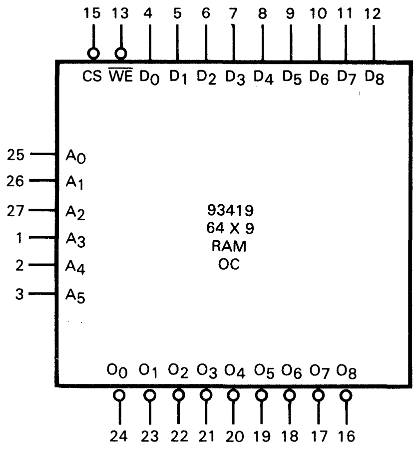
RAM Logic Symbols

256-Bit RAM



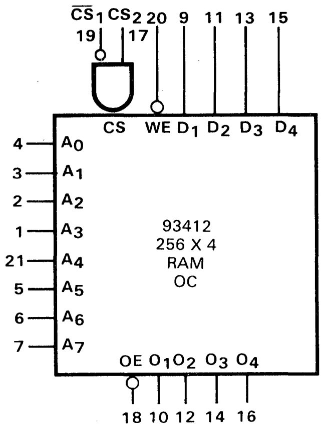
t_{AA} = 45 ns typ
P_D = 275 mW

576-Bit RAM



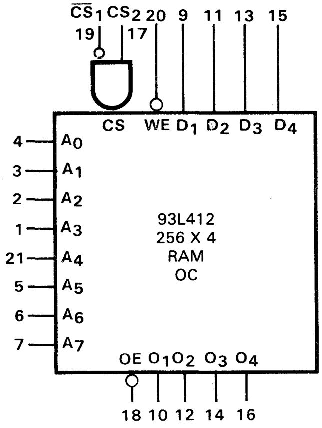
t_{AA} = 30 ns typ
P_D = 725 mW

1K RAM



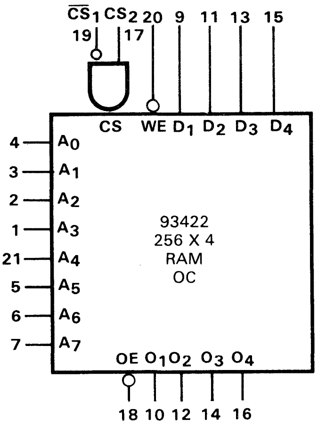
t_{AA} = 30 ns Typ
P_D = 475 mW

1K RAM



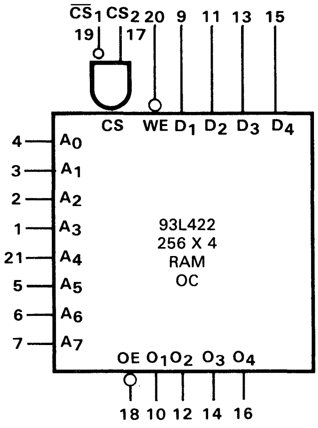
t_{AA} = 45 ns typ
P_D = 250 mW

1K RAM



t_{AA} = 30 ns Typ
P_D = 475 mW

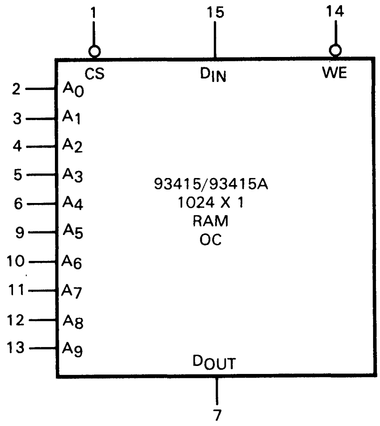
1K RAM



t_{AA} = 45 ns typ
P_D = 250 mW

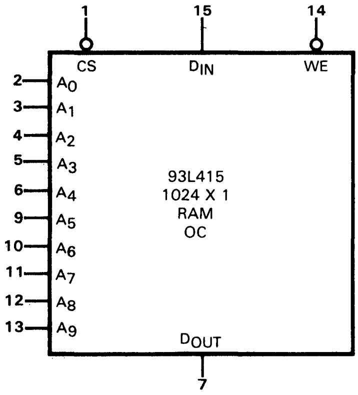
RAM Logic Symbols

1K RAM



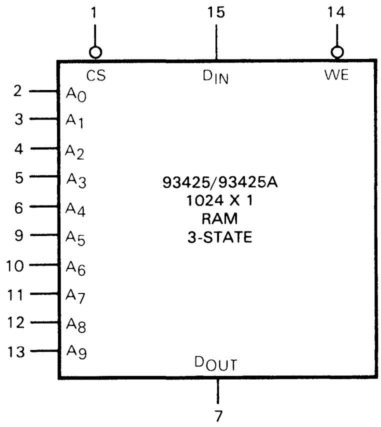
t_{AA} = 30/25 ns typ
P_D = 475 mW

1K RAM



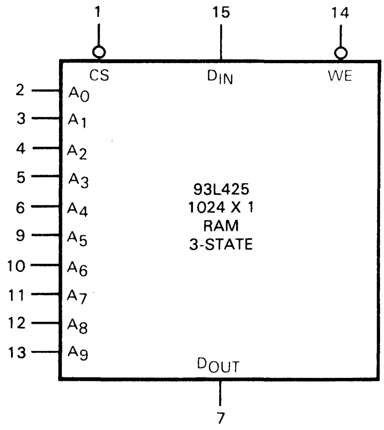
t_{AA} = 35 ns typ
P_D = 200 mW

1K RAM



t_{AA} = 30/25 ns typ
P_D = 475 mW

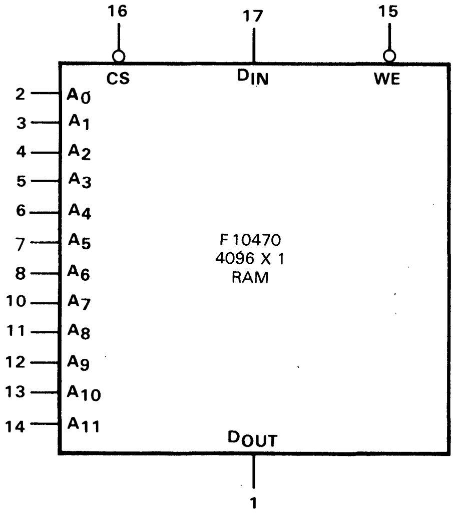
1K RAM



t_{AA} = 35 ns typ
P_D = 200 mW

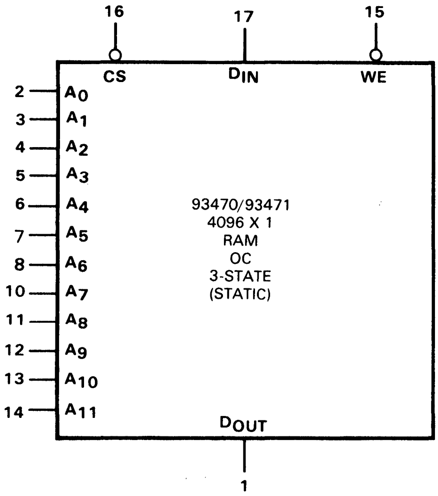
RAM Logic Symbols

4K RAM



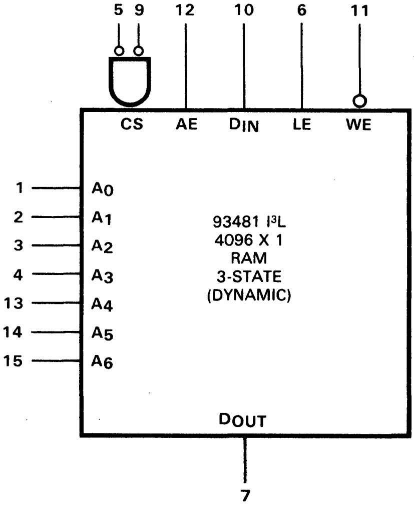
t_{AA} = 25 ns typ
P_D = 900 mW

4K RAM



t_{AA} = 30 ns typ
P_D = 750 mW

4K RAM



t_{AA} = 90 ns typ
P_D = 350 mW (Active)
50 mW (Standby)

RAM Logic Symbols

GENERAL TIMING CONSIDERATIONS

The various ac characteristics of memory chips are discussed in the preceding section. These delays, setup times and hold times must be combined with those of the other logic elements of a memory system to determine the limitations on the basic timing signals. The scratchpad memory shown in *Figure 5-1* offers a simple example for discussion. For the sake of simplicity all of the elements are shown as blocks. Also, in this form, elements from any circuit family can be assumed.

For this discussion, elements of the F10K ECL family are assumed. *Table 5-1* identifies the circuits and lists only the ac parameters that are pertinent to the worst-case timing limits to be explored. The signals in *Figure 5-1* are shown in the timing diagram of *Figure 5-2*, except for the parallel data inputs and mode control signals for the address counter. These are assumed to be in the desired state at time zero. The signals in *Figure 5-2* are listed in the order of occurrence, and the indicated numerical values are cumulative from time zero.

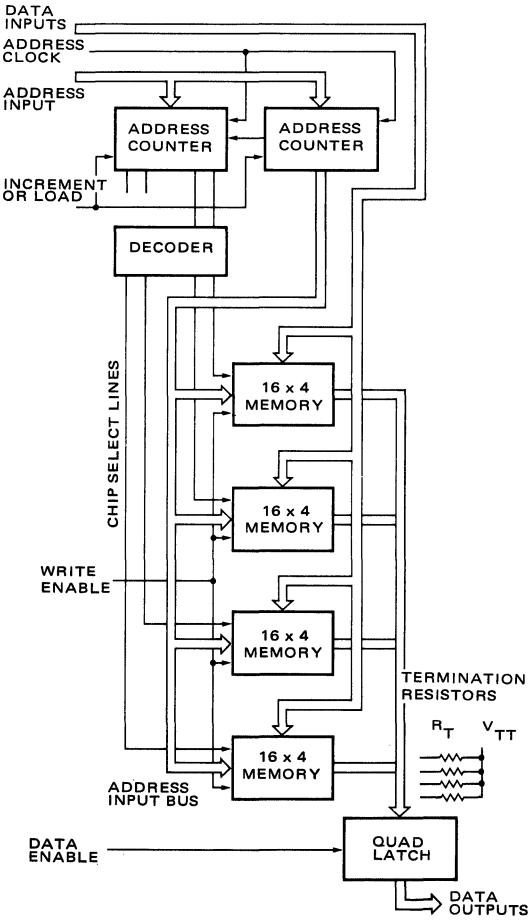


Fig. 5-1. Block Diagram of 64 x 4 ECL Scratchpad Memory

FUNCTIONAL ELEMENT		THROUGHPUT DELAY, ns		SET-UP/HOLD TIMES, ns	
		t_p(min)	t_p(max)	t_s(max)	t_h(max)
ADDRESS COUNTER	F10136 HEXADECIMAL	1.3	2.9	–	–
CHIP SELECT DECODER	F10101 QUAD OR/NOR GATE	1.0	2.9	–	–
DATA OUTPUT LATCHES	F10153 QUAD LATCH	1.0	5.4	2.5	1.5
MEMORY CHIPS	F10145A 16 x 4 RAM	ACCESS TIMES			
READ MODE:	Address Access	t_{AA}(min) 4.5	t_{AA}(max) 9.0		
	Chip Select Access	t_{ACS}(min) 3.0	t_{ACS}(max) 6.0		
WRITE MODE:	Address Set-up/Hold			t_{WSA} 3.5	t_{WHA} 1.0
	Chip Select Set-up/Hold			t_{WSCS} 0.5	t_{WHCS} 0.5
	Data Set-up*/Hold (*for 4 ns write pulse, t_W)			t_{WSD} 4.5	t_{WHD} −1.0

Table 5-1. Worst-case Parameters for 64 x 4 ECL Scratchpad

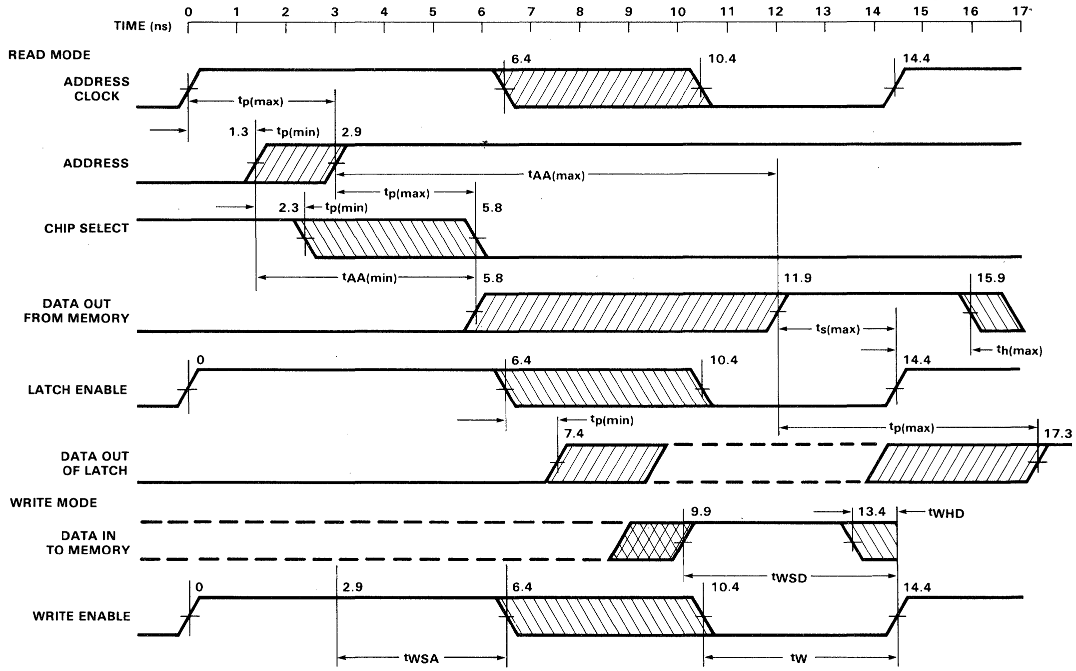


Fig. 5-2. Timing Limitations for 64 x 4 Scratchpad

One important assumption is that the Address Clock, the Latch Enable and, in the Write mode, the Write Enable all have the same waveform. This infers that all three signals are derived from the same basic function, which is perhaps the least complicated approach. This commonality also means that factors from both the Read and Write modes play a part in shaping this basic function. These factors become evident by following through the cycles in the timing diagram.

In the Read mode a new address appears at 1.3 to 2.9 ns, corresponding to the delay limits of the F10136 counter. The F10101 gate delay is between 1.0 and 2.9 ns, which thus makes the net Chip Select delay between 2.3 and 5.8 ns. The earliest time that new data can appear is 5.8 ns, determined by the minimum address counter delay plus the minimum address access time of the memory chips. The latest time for new data to appear is also determined by the counter and the address access, amounting to a total of 11.9 ns. The F10153 latch is transparent when the Enable is LOW; it is latched when the Enable goes HIGH. The latch has a maximum set-up time of 2.5 ns from Data to Enable, which means that the Latch Enable signal can go HIGH no earlier than 14.4 ns. Thus, under the commonality assumption, the cycle time can be no less than 14.4 ns for either Read or Write, since the Address Clock and, in the Write mode, the Write Enable go HIGH at that time.

Limitations on the time that the Address Clock/Latch Enable/Write Enable can go LOW are determined in the Write mode, starting from 14.4 ns on the Write Enable and working backwards. The write pulse width requirement of 4 ns means that the Write Enable can go LOW no later than 20.4 ns. The maximum address set-up time (for the F10145A) of 3.5 ns added to the address counter delay of 2.9 ns means that Write Enable must not go LOW before 6.4 ns, to avoid writing into the wrong location. Thus the Address Clock/Latch Enable/Write Enable must go LOW between the times 6.4 and 10.4 ns.

The chart shows that the Data In should be stable no later than 9.9 ns. This is based on the data set-up time of 4.5 ns, which is measured backwards from the end of the write pulse, *i.e.,* from the time Write Enable goes HIGH. It is important to note that on some data sheets the data set-up time is specified with respect to the beginning of the write pulse. In these cases, adding the specified minimum set-up time to the specified minimum write pulse duration will give the correct figure to use for minimum Data In set-up time with respect to the end of the write pulse, regardless of how long the write pulse duration might be in a given application. In this regard the memory behaves like any D-type latch, wherein the D input can change randomly except for a certain period of time (the set-up time) preceding the active edge of the enable.

Referring again to the timing diagram, if the write pulse starts at 6.4 ns the Data In must still be stable from 9.9 ns onward. Note in *Table 5-1* that the data hold time is −1.0 ns, meaning that the data can change 1 ns before the end of the write pulse without affecting the reliability of the Write operation. Accordingly, the timing diagram shows that Data In can change any time after 13.4 ns.

Notice in the Read mode that the data out of the latches is assuredly stable after 17.3 ns. Thus if the basic cycle time is 14.4 ns, this data can be sampled after 2.9 ns of the next cycle. Further, this data remains stable until the Latch Enable next goes LOW, plus 1.0 ns.

At the expense of more complex timing signal generation, shaping the Address Clock, Latch Enable and Write Enable separately can allow faster operation. For example, the second positive-going edge of the Address Clock can occur at 10.6 ns rather than 14.4 ns. The address counter output would then change no sooner than at 11.9 ns, with the Chip Select following no sooner than at 12.9 ns. The minimum delay from Chip Select to Data Out of a memory chip is 3.0 ns. Thus the Data Out could change no sooner than at 15.9 ns, which agrees with the timing requirement shown in *Figure 5-2*. Thus the opportunity exists to reduce the read cycle time by 3.8 ns by offsetting the Latch Enable with respect to the Address Clock. Similarly, in the write mode the Write Enable pulse can begin (go LOW) at 6.4 ns and end at 10.6 ns, which would make the Write Enable coincide with the revised Address Clock. These modifications would naturally have an effect on the timing requirements of the Data In signals and on the sampling window at the latch outputs.

INTERFACE

In most bipolar-memory applications, the devices are combined with other TTL or ECL logic elements into a subsystem such as a CPU buffer controller or other function. The memory device interface is at standard logic levels, and the additional hardware required is usually limited to pull up resistors at the outputs of most TTL memories, and load resistors or termination resistors for the ECL memories.

In some cases, the application may require location of the memory several feet or more away from the other functions in the subsystem. The general subject of data transmission and the effects of cable length and bandwidth on maximum data rates is discussed in the Fairchild Interface Handbook, which also discusses interface elements for TTL. Line drivers and receivers for ECL are discussed in the Fairchild ECL Handbook and subsequent data sheets.

MICRO-CONTROL STORAGE USING READ/WRITE MEMORY

Early in semiconductor memory development, a significant amount of attention was devoted to Read-only memories for micro-control storage. In many cases, difficulties were encountered in developing firmware for new machines. These difficulties involved turnaround time of weeks and months in making firmware changes, with costs ranging from tens to thousands of dollars per change. One solution to these problems is to use RAMs for micro-control storage. Firmware may then be changed almost instantaneously, thus greatly accelerating the development program and eliminating cost and downtime for pattern changes. If desired, conversion from RAM to ROM can be made at the preproduction phase. Availability of 1024-bit bipolar RAMs such as the 93415 and 10415 has prompted designers to consider this approach.

BUFFER MEMORIES

Buffer memories are small to medium memories inserted between I/O interfaces and CPU, between main memory and CPU, or at other locations where fast intermediate storage is required. The availability of 256 and 1024-bit RAM devices has resulted in many bipolar buffer memory designs.

MAIN MEMORIES

Main memories vary from 4K to 16K bits in minicomputers up to 256K or more words in large mainframes. Before the availability of bipolar 1024 RAMs, system designers were limited to low-cost core with 1 to 2 μs access, expensive core with 400 ns to 1 μs, or MOS with $>$ 200 ns access. Some n-channel MOS products offer faster access time. Present bipolar RAM technology allows implementing large main memories with 50 to 80 ns worst case maximum access times for the subsystem. A Read-Modify-Write cycle of less than 100 ns is possible.

Typical Applications

Word Expansion

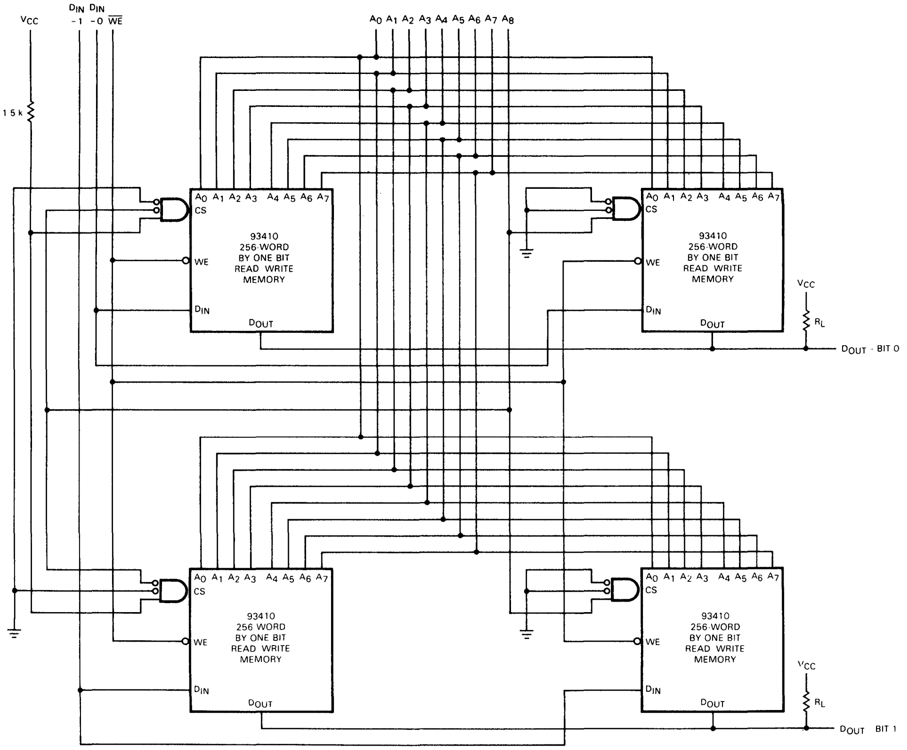
The 93410 may be used in memories requiring expansion of both the number of words and number of bits. A 512 x 2 array and the necessary signal interconnects for accomplishing expansion is shown in *Figure 5-3*. The number of words may be expanded to 4096 by using only one 9321 dual 1-of-4 decoder.

256-Word by 8-Bit Buffer Memory System

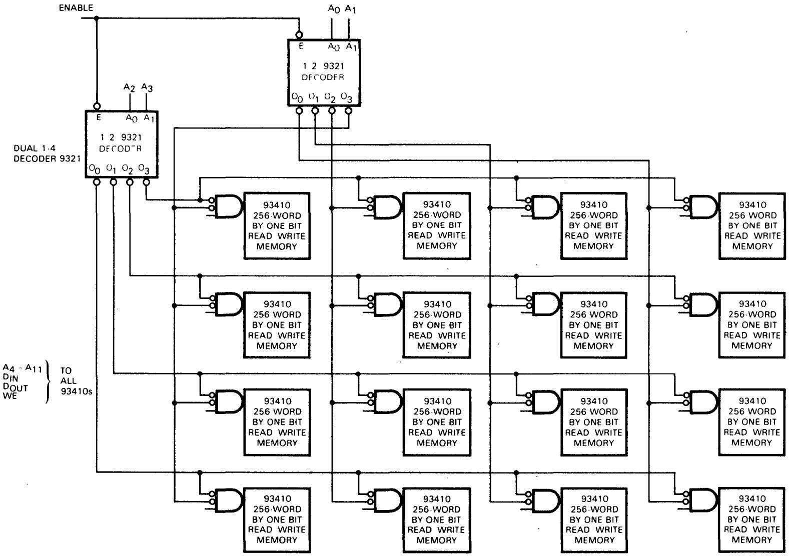
A 256-word by 8-bit buffer memory based on the 93410 is shown in *Figure 5-4*. Input and output data latches and a modulo 256 address counter may be implemented with MSI devices such as the 9308 quad latch and 9316 binary counter.

Last In/First Out (LIFO) Push-Down Stack Memory

A Last In/First Out (LIFO) push-down stack memory, 254 words deep by 4-bits wide, is shown in *Figure 5-5*. This synchronous memory system accepts data on four parallel inputs ($I_0 - I_3$) and, controlled by two independent inputs (Read and Write), presents the "youngest" word that has not yet been read on the four outputs ($Q_0 - Q_3$). It also provides status information on four outputs: Full, Almost Full, Empty, Almost Empty.



a. 512-Word by 2-Bit Array



b. 4096-Word Memory Plane

Fig. 5-3. Word Expansion

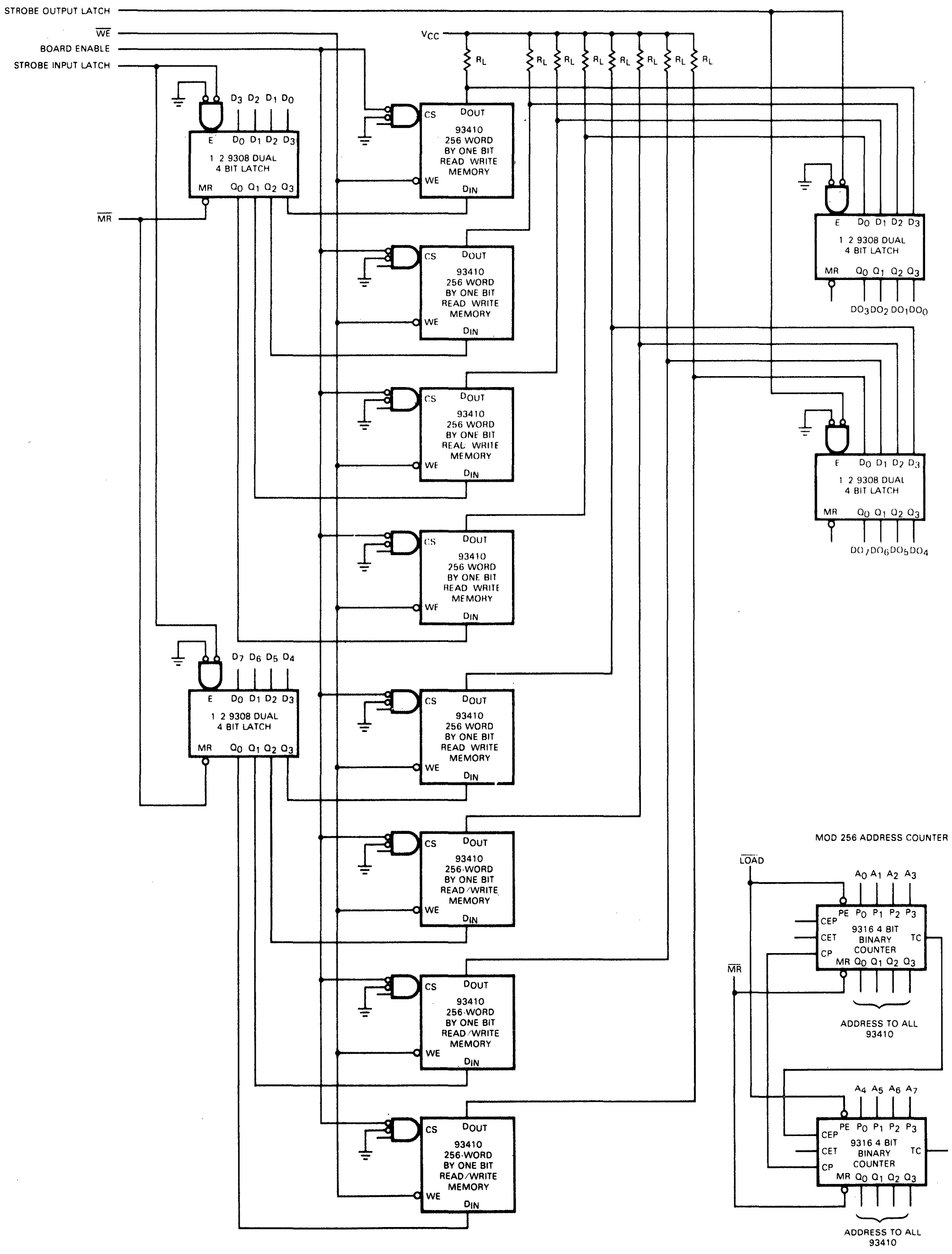
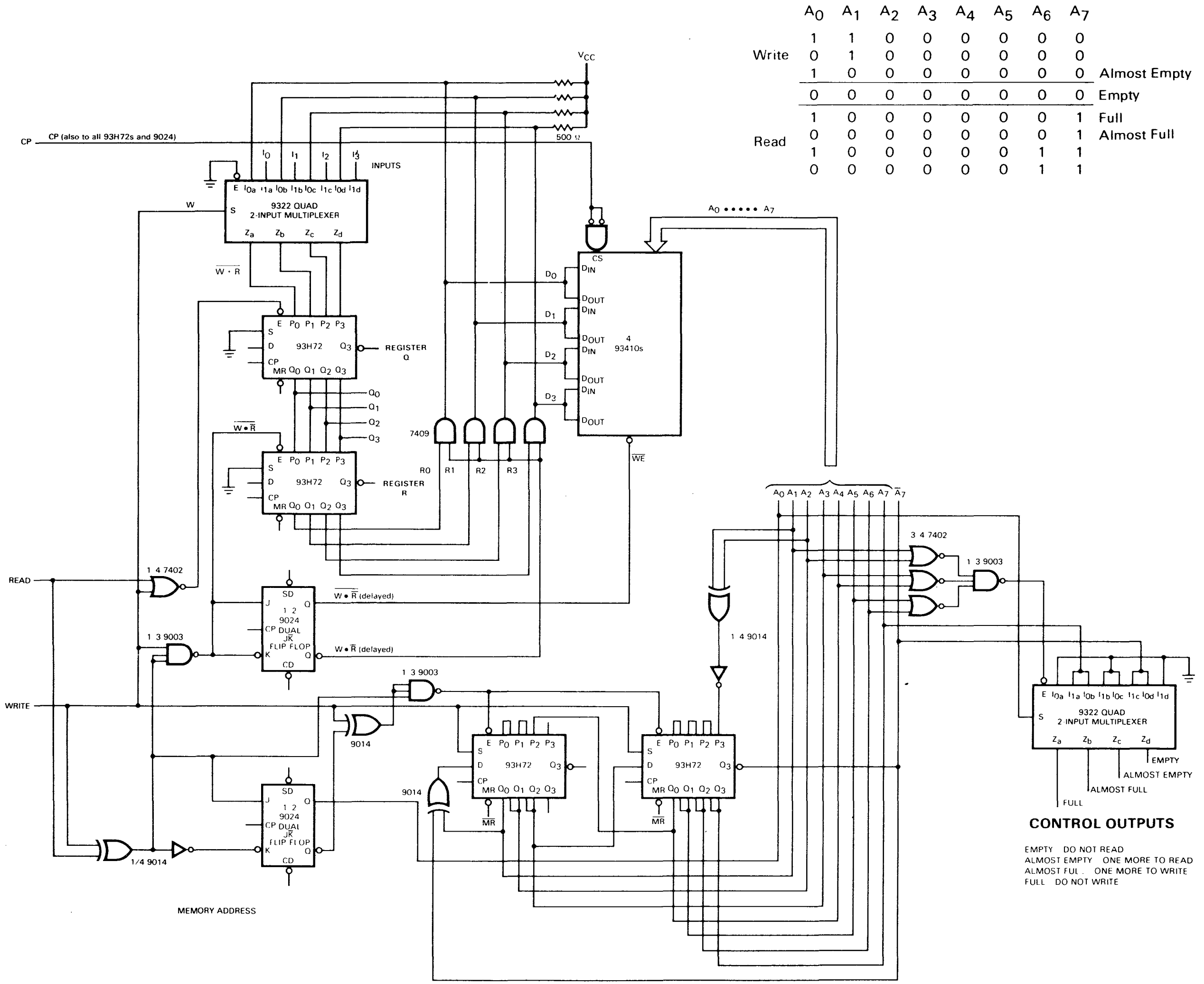


Fig. 5-4. 256 Word by 8-Bit Buffer Memory System



	A0	A1	A2	A3	A4	A5	A6	A7	
	1	1	0	0	0	0	0	0	
Write	0	1	0	0	0	0	0	0	
	1	0	0	0	0	0	0	0	Almost Empty
	0	0	0	0	0	0	0	0	Empty
	1	0	0	0	0	0	0	1	Full
Read	0	0	0	0	0	0	0	1	Almost Full
	1	0	0	0	0	0	1	1	
	0	0	0	0	0	0	1	1	

CONTROL OUTPUTS

EMPTY DO NOT READ
ALMOST EMPTY ONE MORE TO READ
ALMOST FULL ONE MORE TO WRITE
FULL DO NOT WRITE

Fig. 5-5. LIFO Push-Down Stack Memory

Operation is synchronous and edge-triggered on Data as well as Control inputs. It depends on the state of the $I_0 - I_3$, Read and Write inputs, and a setup time (≈30 ns) before the rising edge of the clock that should not exceed 15 MHz at 50% duty cycle.

There are four different modes of operation:

$W \bullet \bar{R}$ = Write – I is shifted into Q, the old information in Q is shifted into R, the address counter is incremented, and on the next clock Low period, the content of R is written into the new memory location.

$\overline{W} \bullet R$ = Read – Data in the wired-OR D is shifted into Q, the information in R is maintained, the address counter is decremented. If the previous clock cycle had executed a Write instruction, then D is controlled by the register R. If the previous clock cycle had been one of the other three modes, then D is controlled by the memory.

$W \bullet R$ = Read and Write Simultaneously – Input data is shifted into Q; register R and address counter are maintained.

$\overline{W} \bullet \bar{R}$ = Do Nothing – No change.

The control outputs allow normal computer "handshaking", and also supply a warning signal one operation in advance.

The synchronous up/down address counter is built as a shift register counter. This is both faster and more economical than using 9366 binary counters. The non-binary count sequence is no drawback in this application, and the sacrifice of two of the 256 states is insignificant.

Bipolar RAM Design Example

The best way to illustrate the ease of design and other advantages of bipolar static RAMs is to give a design example. It is assumed that the designer needs a modular rack-mounted system to cover a broad range of applications. Since all parts of the system–components, architecture, packaging, modularity, testing, etc.,–are closely interrelated, they have equal importance and must all be considered. Consequently, for this design, the packaging for example assumes the same importance as the circuit considerations. No part of the design should be treated separately.

Memory Modularity

Basic Memory Cards: (*Figure 5-6*)

One with 8K words and 8 or 9 bits, *i.e.,* one design with last row not inserted, for 8 bits.

One with 4K words and 8 or 9 bits, *i.e.,* one 8K design may be used with 93L415s for 4K words not inserted and for 8 bits, one row is not inserted.

Basic Memory Module: (*Figure 5-7*)

One memory card (basic)
One address drive card
One base
Power
Card cage (rack mount)

Expanded Memory Module: (*Figure 5-7*)

Modular from one to eight memory cards
One address drive card
One base
Power
Cables
Card cage (rack mount)

WORDS/BYTES	WORDS/BITS	CARDS/MODULE
4K x 8/9	4K x 8/9	1/2
-----	4K x 16/18	1
8K x 8/9	8K x 8/9	1
16K x 8/9	8K x 16/18	2
24K x 8/9	8K x 24/27	3
32K x 8/9	8K x 32/36	4
40K x 8/9	8K x 40/45	5
48K x 8/9	8K x 48/54	6
56K x 8/9	8K x 56/63	7
64K x 8/9	8K x 64/72	8

Memory Size Range Using Multiple Cards in One Module

WORDS/BYTES	WORDS/BITS	NO. MODULES
64K x 8/9	8K x 16/72	1
128K x 8/9	16K x 16/72	2
192K x 8/9	24K x 16/72	3
256K x 8/9	32K x 16/72	4
320K x 8/9	40K x 16/72	5
384K x 8/9	48K x 16/72	6
448K x 8/9	56K x 16/72	7
512K x 8/9	64K x 16/72	8

Memory Size Range Using Multiple Modules

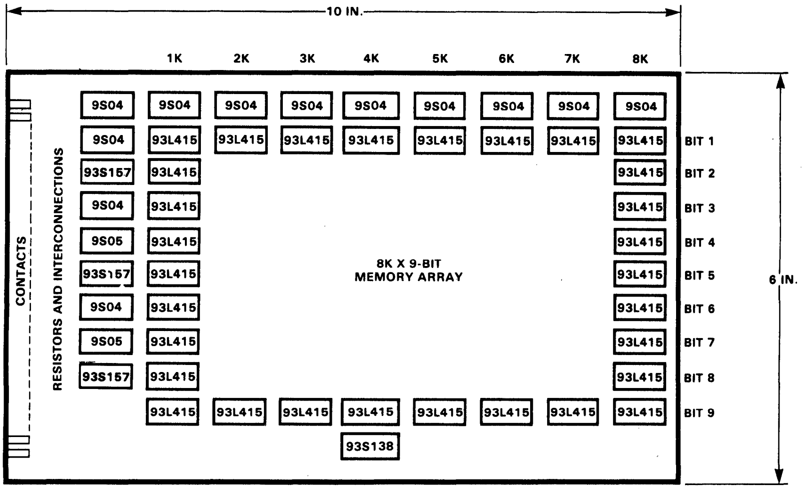


Fig. 5-6. Memory Board Component Layout

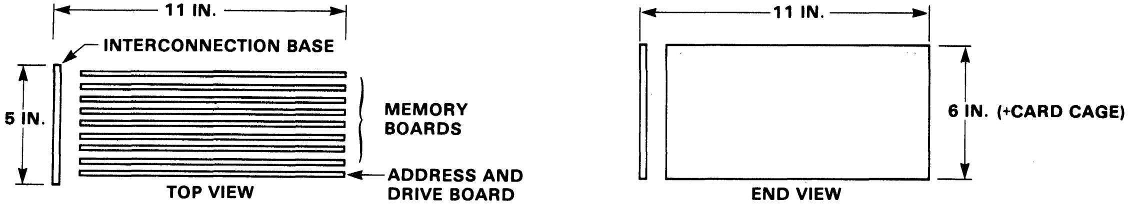


Fig. 5-7. Physical Layout for a Bipolar Memory Module

Packaging System
Memory and Address Boards: Two-sided printed circuit boards with plated holes.

Base: A two-sided printed circuit board.

Memory Board Connectors: Conventional pc board connectors which permit wire wrap on the back side. All memory address and control interconnections are directly on the base.

> Byte-oriented systems: All wiring on the base; no wire wrap needed.
>
> Word-oriented systems: The address and control lines remain on the base. The data input and data output cables to the computer are brought directly to the pins on the respective memory cards.

Power Distribution: Power conducted along the base and distributed to pins on each pc card. Power distribution bars for ground and the one voltage, +5 V, augment the copper on the base pc board.

Cooling: Forced air cooling, 400 or more feet per minute flowing between the cards. Stacks of memories up to four deep require about 500 feet per minute.

Card Cage: Available standard catalog-item card guides.

The Basic Memory Card
Figure 5-6 shows the layout of the components on the basic memory card. The contact pins are located on the left. The resistors terminating the input data cables from the computer are in the first component column. Next is a column of ICs with the following functions.

ITEM	NO. PACKAGES	SIGNALS	FIGURE	FUNCTION
9S04	2	$A_0 - A_9$ $\overline{WE}$	5-8 5-10	Drive In
93S157	1	$D_{OUT1} - D_{OUT3}$	5-12	Output Latches
9S04	1	Data Strobe $D_{IN1} - D_{IN3}$	5-12 5-11	Drive In
9S05	1	$D_{OUT1} - D_{OUT3}$	5-12	Drive Out
93S157	1	$D_{OUT4} - D_{OUT6}$	5-12	Output Latches
9S04	1	$D_{IN4} - D_{IN9}$	5-11	Drive In
9S05	1	$D_{OUT4} - D_{OUT9}$	5-12	Drive Out
93S157	1	$D_{OUT7} - D_{OUT9}$	5-12	Output Latches

IC Column 1

ROW	ITEM	SIGNAL COL. 2	SIGNAL COL. 3	FIGURE
Top	9S04	WE	A_1	
		A_0	A_3	5-8
		A_2	A_5	5-10
		A_4	A_7	5-13
		A_6	A_9	
		A_8	--	
Bit 1	93L415	0-1K	1K-2K	5-13
Bit 2	93L415	0-1K	1K-2K	
Bit 3	93L415	0-1K	1K-2K	
Bit 4	93L415	0-1K	1K-2K	
Bit 5	93L415	0-1K	1K-2K	
Bit 6	93L415	0-1K	1K-2K	
Bit 7	93L415	0-1K	1K-2K	
Bit 8	93L415	0-1K	1K-2K	
Bit 9	93L415	0-1K	1K-2K	

IC Columns 2 and 3

The memory columns are organized in pairs. The 9S04 inverters are used at the top to give fan-out drive to each pair of columns. The schematic of this drive/fan-out is illustrated in *Figures 5-8* and *5-10*. Since there are six inverters per package and eleven lines to be driven, *i.e.,* A_0 through A_9 plus WE, two 9S04 hex inverter packages are sufficient. The input characteristics of the 93L415 1024-bit RAM are such that two columns represent only 4.1 unit loads for the 18 inputs. The four inverters represent 5 unit loads to the driver.

The same arrangement is used to provide four column pairs. The additional pairs implement memory words as follows:

Pair #2: 2K-3K and 3K-4K
Pair #3: 4K-5K and 5K-6K
Pair #4: 6K-7K and 7K-8K

A 93S138 1-of-8 decoder, located under column 4 of the array, performs the address selection to choose the column representing 1K of the possible 8K words of memory. As illustrated in *Figure 5-9*, the decoder drives each column separately to control chip selection. Addresses A_{10}, A_{11}, and A_{12} as well as E_1, *i.e.,* memory select, are the inputs controlling the decoder.

When arranged this way, all lines on the memory board are short enough so that terminating resistors and controlled impedance lines are unnecessary. The longest line running from the address drive to the last column is approximately eight inches. The vertical lines driving the array start at row 1, split into a "U" shape and drive two columns with branches about five inches long. The 1-of-8 decoder drive lines vary from five to eight inches long. TTL and ECL systems operate satisfactorily in this type of packaging environment.

Memory Module Packaging

Figure 5-7 shows one possible layout for a memory module. The base on the left is used to connect the address card with one to eight memory cards. For byte-oriented systems, the cables to other equipment are connected to the base at one end. The cable termination and fan-out drive circuits are contained on the address and drive board. For word-oriented systems, the address and control lines are routed to one end of the base and through the address board to drive the memory cards. However, due to the large number of cables involved, the data input and data output lines should be attached, *i.e.,* wire wrap or other means, directly to the data input and output pins of each memory card. The cards are designed so that termination for data input is on the memory board (*Figure 5-11*) and sufficient drive is provided on the output (*Figure 5-12*). A pair of resistors to $+V_{CC}$ and ground should be used to terminate the data output lines within the receiving equipment.

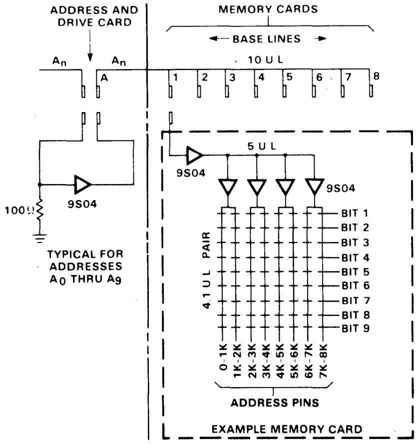


Fig. 5-8. Address Selection for Bits Within a 1024 RAM

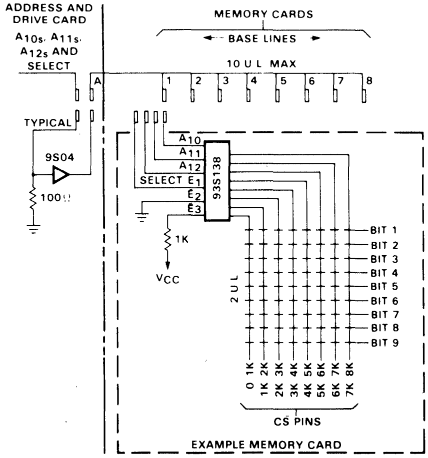


Fig. 5-9. Address Selection Groups of 1024 RAMs

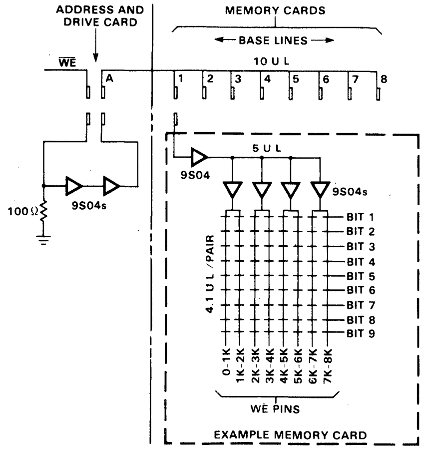
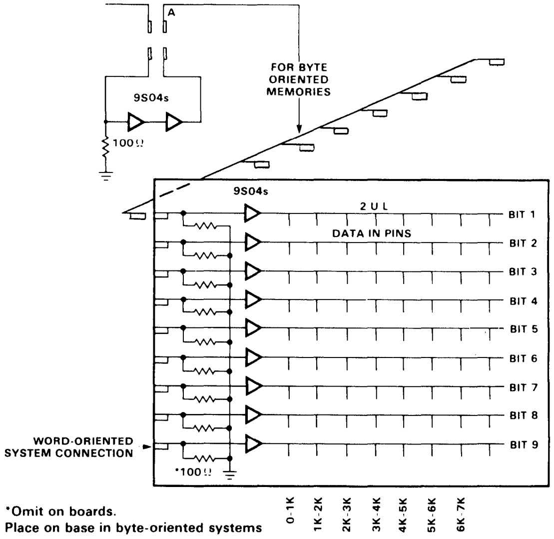


Fig. 5-10. Read/Write Selection



*Omit on boards.
Place on base in byte-oriented systems

Fig. 5-11. Data Input System

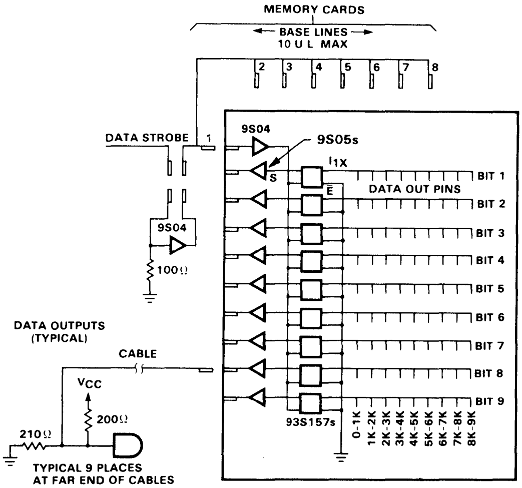


Fig. 5-12. Data Output System

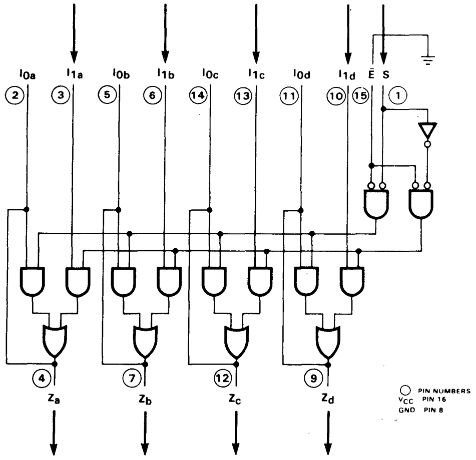


Fig. 5-13. 93S157 as a Pass Through Latch for Data Output System

*100 Ω terminating resistors to ground are assumed on each input

ITEM	*SIGNAL	FIGURE
9S04	A_0	5-8
	A_1	
	A_2	
	A_3	
	A_4	
	A_5	
9S04	A_6	5-8
	A_7	
	A_8	
	A_9	
	WE $\overline{WE}$	5-10
9S04	A_{10}	5-9
	A_{11}	
	A_{12}	
	$\overline{E}_1$	
	DS	5-12

Address Board Components

For tightly packaged systems where the other logic is adjacent to the memory, omit the address card and include the required signal drive and inverters as part of the computer. The memory card design provides great flexibility for integration into other systems. Normal TTL circuit rules apply.

Address Board

The address board is a very simple two-layer pc board. It receives the address and control signals from the equipment attached to the memory and provides the necessary fan-out drive. The inversion function is also performed if required. There are few components and pin connections on the address board. In tightly coupled systems, it may be omitted and the required circuits can be part of the other equipment. In this case, it may be necessary to provide circuits that can drive 10 unit loads plus a terminating resistor mounted on the base opposite the input cable end. When using an address board, the longest output line is less than nine inches so no terminating resistors are needed within the memory for a TTL design.

Memory Board Circuits and Layouts

Figures 5-8 through *5-12* are combination circuit and pseudo-physical routing schematics. *Figure 5-8* through *5-10* illustrate (on the upper left side) the circuits that can be either on an address board or in attached equipment. The base lines for plugging in the eight memory boards are illustrated across the top. An example memory board circuit/routing schematic is shown in each figure along with the relationships of bits and words in the rows and columns. Refer to *Figure 5-6* for the memory board layout. The ICs include Schottky TTL types 9S04, 9S05, 93S138, 93S157, and the TTL 1K RAM 93L415. The faster higher powered 93415 or 93415A can be substituted without any electrical design or layout changes. The power supply must be increased and more cooling provided; also memory timing pulses must be adjusted to take advantage of these faster parts.

Figure 5-11 illustrates the data input system. If the cables for word-oriented systems come directly to the memory card, the 100 Ω terminating resistors are used. In byte-oriented systems, these resistors are omitted. The drive circuits for byte-oriented systems may be located either on the address drive board or in the attached equipment. If sufficient fan-out drive is supplied from the equipment and long cables are used, a terminating resistor is placed at the far end of the base.

The data output system is shown in *Figure 5-12*. The 93L415 outputs for each bit are connected together and run to the I_{1x} pin of a 93S157 multiplexer. The multiplexer is connected to provide a pass through latch as shown in *Figure 5-13* to permit rapid data access, long data hold time, and to minimize strobe skew. 9S05 drivers with open collectors are provided for output drive so the various bits in a byte-oriented memory can be OR-tied together. A resistor network as illustrated in *Figure 5-12* is placed at the receiving end of the output data cables.

Some Interconnection Hints

The dual-in-line package is designed with space to run one pc board conductor between pins. Two-layer printed circuit boards provide for running horizontal connections on the back and vertical connections on the front. This and the regularity of connections in a memory array allow very tight packaging. IC spacing on the memory board can be on a pitch of one inch horizontally and one-half inch vertically, which is a common industry practice.

Interconnections are made using straightforward simple wire routings on two-layer boards. *Figure 5-14* presents part of the actual layout showing three columns of the array. The connections to the 9S04 address drive are at the top. Ground and $+V_{CC}$ trees are also illustrated; note that one ground and one $+V_{CC}$ line go between each column. It is important that the designer run one line horizontally across the board and attach it through plated holes to $+V_{CC}$ at every other package row. This forms a screen or mesh for power distribution. A similar arrangement should be used for ground.

The vertical lines are routed to pin rows of the DIPs. This provides address, Read/Write and chip selection on the front side of the pc board. The data input and output lines are on the back side along with the V_{CC} and ground cross connections. Appropriate capacitors should be placed between V_{CC} and ground for about every four packages. Normal TTL design rules apply.

Performance Characteristics

The chart below and *Figure 5-15* summarize the performance that can be expected from a system using Schottky TTL parts and 90-ns 93L415 1K RAMs. The power dissipation is calculated for worst-case conditions for the Schottky parts and for typical dissipation on the memory parts. This is reasonable, since so many memory parts are used, the averages apply. The timing calculations are made using 2 ns/foot delays for signals on conductors and worst-case Schottky values. The Read and Write cycle times for the 93L415 are assumed to be 90 ns for the example calculations; however the user may specify shorter access times at added cost. To adjust the times shown, a designer may add the nanosecond differences for maximum RAM times or subtract the differences if he uses faster parts. Pipelining effect through the memory system logic is not included; if it is, the cycle times can be reduced a few nanoseconds.

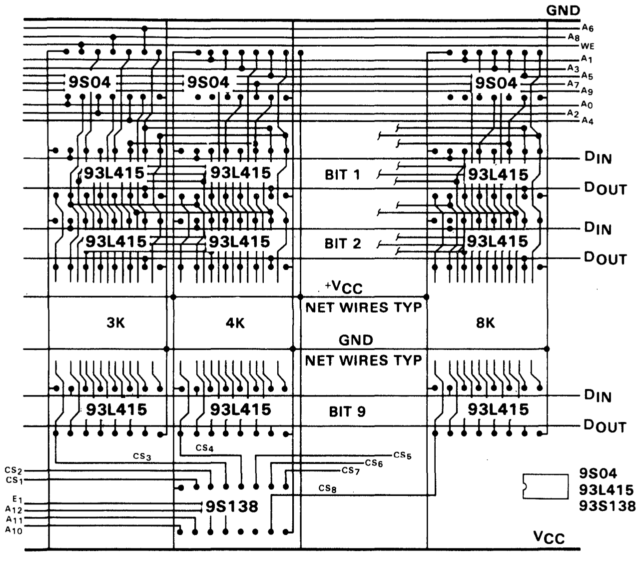


Fig. 5-14. Memory Column Interconnection System

ITEM	SINGLE 8K x 9 CARD	MODULE 8 CARDS	SYSTEM *8 MODULES
Size: Words/Bits	8K/9	8K/72 or 64K/9	64K/72 or 512K/9
Total Bits	73,728	589,824	4,718,592
Read Access	120 ns typ	125 ns typ	135 ns typ
Data Window	80 ns typ	80 ns typ	80 ns typ
Read Cycle	120 ns typ	125 ns typ	135 ns typ
Write Cycle	120 ns typ	125 ns typ	135 ns typ
Inputs & Outputs	TTL	TTL	TTL
Supply Voltage (one)	+5.0 V	+5.0 V	+5.0 V
Supply Current	3.11 A	24.9 A	199 A
Power	15.6 W	125 W	998 W
Inlet Air	0°C to 55°C	0°C to 55°C	0°C to 55°C
Cooling Air	400 fpm	400 fpm	500 fpm

*Two rows of four modules.

Table 5-2.
Memory Performance Summary Using 93L415 RAMs and Schottky TTL Parts

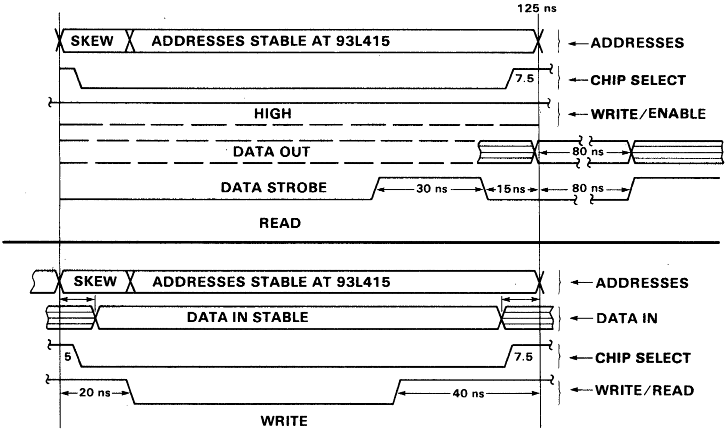


Fig. 5-15. Timing Example for 93L415 Memory

Minor adjustments in timing may have to be made to accommodate a specific design. Layout dimensions and the minimum and maximum times established for all components will affect the system delays. The time values used in this example take line-length delays and circuit skews into account with appropriate allowance for margins.

CONCLUSION

Smaller die size, increased yields and economical packaging have reduced bipolar 1K RAM costs to the point where bipolar memories have become attractive for some applications reserved, in the past, for slower, lower cost MOS memories. Instead of emphasizing the cost per bit, the designer should look at the total memory system cost and inherent device characteristics when choosing a RAM for a specific application. The chief advantages of bipolar RAMs are outlined below.

- Simple design, construction, testing and field maintenance features of static bipolar TTL memories mean lower total system-lifetime hardware costs.

- Fast static memories greatly ease system interrupt and software storage and access problems as well as enhance system throughput, thus providing system lifetime savings.

REFERENCE

Rice, R., Green, F. and Sander, W., "Design Considerations Leading to the ILLIAC IV Process Element Memory," IEEE Solid-State Circuits Journal, October 1970.

Bipolar
Memory
Bipolar
Memory

Bipolar Memory Bipolar Memory

CHAPTER 6

Chapter 6
READ ONLY MEMORIES

A Read-Only Memory is a random access memory in which the stored information is fixed and non-volatile. By convention, a semiconductor ROM is a circuit whose stored information is fixed by a masking operation during wafer processing, whereas a PROM is one whose contents are uniquely determined after processing and packaging. A ROM is best suited for systems produced in large volume, where the tooling charge for a unique mask is relatively small on a per-unit basis and is often counterbalanced by the economies of batch processing. PROMs are the best choice in low volume production, in systems having a limited useful life, in short procurement cycle situations and for applications wherein some degree of system tailoring is required for each installation. For developmental and prototype work, wherein design changes are normal occurrences and short turn-around times are essential, PROMs are an obvious choice.

Bipolar ROMs and PROMs offer access times in the 25–50 ns range for TTL and 15–20 ns for ECL, which represent an order of magnitude improvement over equivalent MOS circuits. Historically, MOS ROMs and PROMs have offered greater bit densities than have bipolar circuits. More recently, however, technological advances have placed bipolar densities between those of PMOS and silicon gate NMOS; continuing development promises to narrow the gap even further.

Certain types of MOS PROMs (EPROMs) can be completely erased and reprogrammed but bipolar PROMs cannot. Fairchild bipolar PROMs are manufactured with all bits in the HIGH state. As indicated in *Figure 6-1*, changing a bit from HIGH to LOW consists of steering an applied current from the pertinent output back to the intersection of the word and bit lines for the addressed cell. The current causes the fuse to open, and thus a bit that has been changed to the LOW state cannot be changed back to the HIGH state. Fairchild bipolar PROMs use nichrome fuses, since this material has a long history of usage in microelectronics[1–4] and a great deal of experience has been gained. The fuse has a notch in the middle to concentrate the energy and assure a wide, clean break.

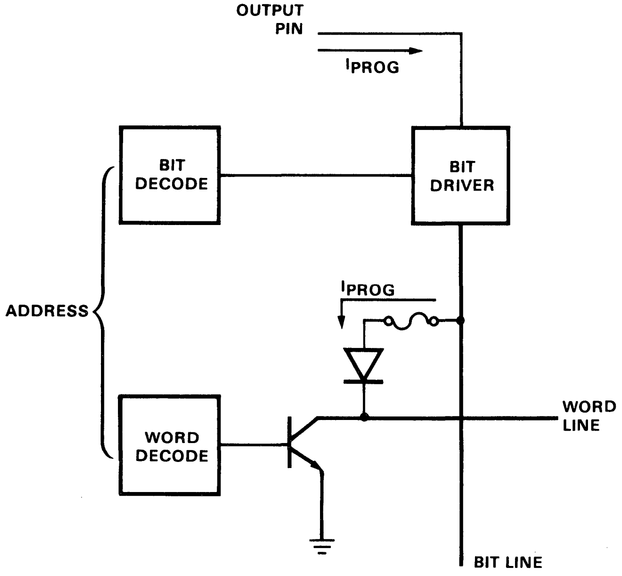
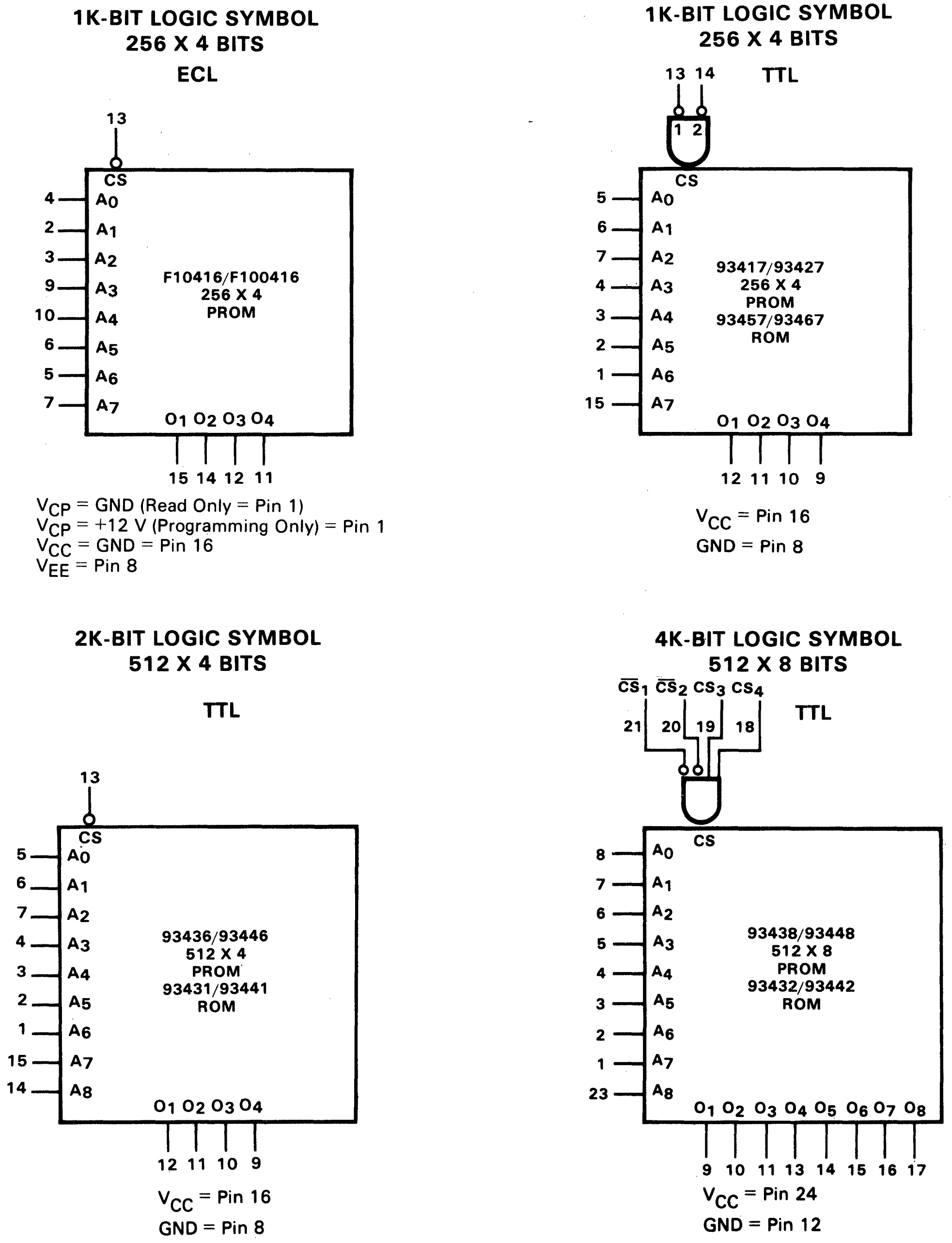


Fig. 6-1. Programming Current Path

Fairchild offers a broad range of ROMs and PROMs, as indicated in the Selection Guide. Logic diagrams for the bipolar circuits are shown in *Figure 6-2*. Each basic TTL type is available with open-collector outputs or with 3-state outputs. ECL outputs are open emitter. Worst-case specifications for each device type, as listed in the individual data sheets, are guaranteed over the applicable temperature and supply voltage range.


1K-BIT LOGIC SYMBOL
256 X 4 BITS
ECL

V_{CP} = GND (Read Only = Pin 1)
V_{CP} = +12 V (Programming Only) = Pin 1
V_{CC} = GND = Pin 16
V_{EE} = Pin 8

1K-BIT LOGIC SYMBOL
256 X 4 BITS
TTL

V_{CC} = Pin 16
GND = Pin 8

2K-BIT LOGIC SYMBOL
512 X 4 BITS
TTL

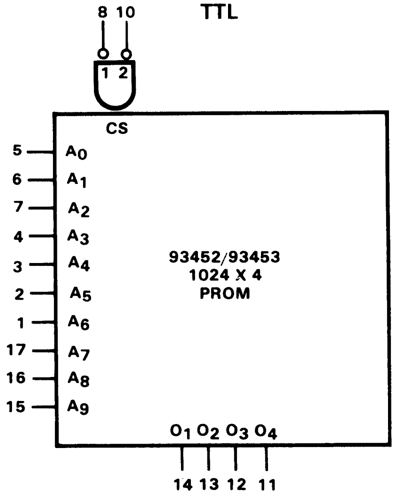
V_{CC} = Pin 16
GND = Pin 8

4K-BIT LOGIC SYMBOL
512 X 8 BITS
TTL

V_{CC} = Pin 24
GND = Pin 12

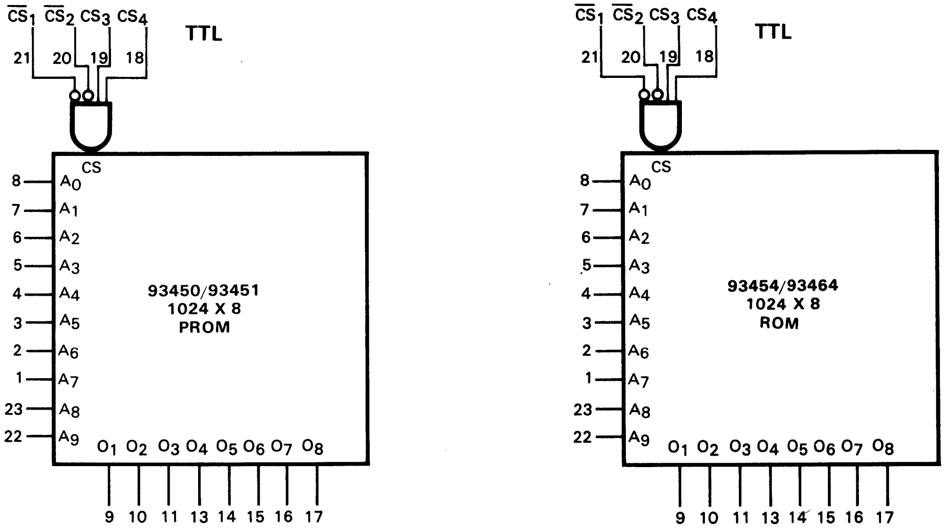
Fig. 6-2a PROM and ROM Logic Symbols

4K-BIT LOGIC SYMBOL
1024 X 4 BITS



V_{CC} = Pin 18

GND = Pin 9



8K-BIT LOGIC SYMBOL
1024 X 8 BITS

V_{CC} = Pin 24

GND = Pin 12

8K-BIT LOGIC SYMBOL
1024 X 8 BITS

V_{CC} = Pin 24

GND = Pin 12

Fig. 6-2b PROM AND ROM Logic Symbols

On older data sheets, ROM and PROM outputs were called O_n and were drawn with bubbles to show that the open-collector output pulls LOW and to indicate that an unprogrammed output is HIGH. Since the bars and bubbles are not normally used to convey such a meaning, this publication and all future data sheets describe the outputs as active HIGH, call them O_n and, therefore, show no bubbles. When the terms "0" and "1" are used in coding or describing ROMs and PROMs, positive-true logic is assumed, *i.e.,* a "0" is a LOW and a "1" is a HIGH signal.

APPLICATIONS

ROMs and PROMs are widely used in computers of all sizes. They are finding increased usage in other areas such as peripheral controllers, terminals, instruments and digital controls of all kinds. Specific applications include data and instruction storage in computers, microprogrammed system control storage, look-up and decision tables, and address and priority mapping. Other applications include character/vector generation, encoding/decoding and sequential controllers.

ROMs and PROMs are also finding increased usage as replacements for combinatorial logic, wherein they can replace from two to twenty packages[5]. In this type of service a ROM or PROM is treated as a truth table. For example, a 4K PROM organized as 512 x 8 bits implements the truth table for eight functions of nine variables. As a matter of convenience, the application examples that follow use the PROM part numbers.

4-BIT COMPARATOR

The 93417/93427 1K (256 x 4-bit) memory can readily be used as a 4-bit comparator (*Figure 6-3*). In this example, four of eight address lines are assigned to each of the input variables. Unlike conventional MSI comparators with outputs limited to A=B, A<B, A>B, the four PROM outputs can be programmed for a wide variety of functions. Some of the possible functions are:

1. $A + B: = n, > n, < n$
2. $A - B: = n, > n, < n$
3. $B - A: = n, > n, < n$
4. $A \times B: = n, > n, < n$
5. $A \div B: = n, > n, < n$
6. $B \div A: = n, > n, < n$
7. $n < A < m$
8. $n < B < m$

where n and m can be any number or set of numbers and can be assigned different values for each output.

If a 2K (512 x 4-bit) memory (93436/93446) is used, the function can be programmed for two different values or sets of n and m. The desired value or set can then be selected by the A_8 input.

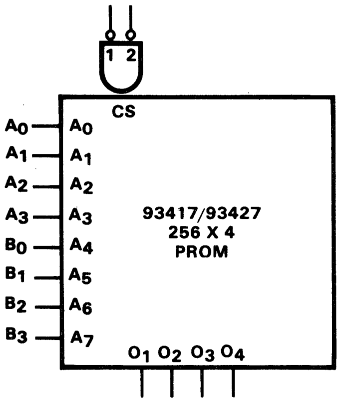


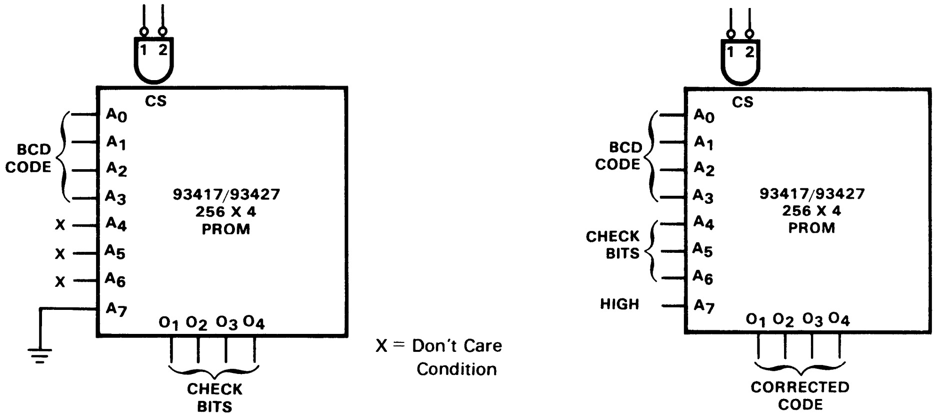
Fig. 6-3. 4-Bit Comparator

HAMMING CODE GENERATOR/CHECKER/CORRECTOR

A PROM can also be efficiently used as a Hamming code generator/checker/corrector. By adding three additional check bits to a 4-bit code, it is possible to detect and correct a single error. A 1K (256 x 4-bit) PROM can be used to generate the three additional bits and to check and correct the 7-bit code (see *Figure 6-4*).

ENCODER/DECODER

A 512 x 8-bit PROM (93438/93448) is used as an encoder/decoder in another simple application illustrated in *Figure 6-5*. Since the ninth address (A_8) is the Decoder/Encoder Select, both functions can be implemented in a single package. Specific applications include emulation, mapping and code conversion.



Check-Bit-Generating Mode

Code-Checking/Correcting Mode

Fig. 6-4. Hamming Code Generator and Checker/Corrector

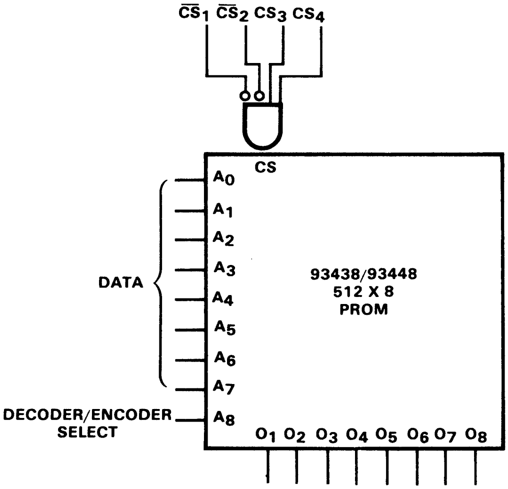
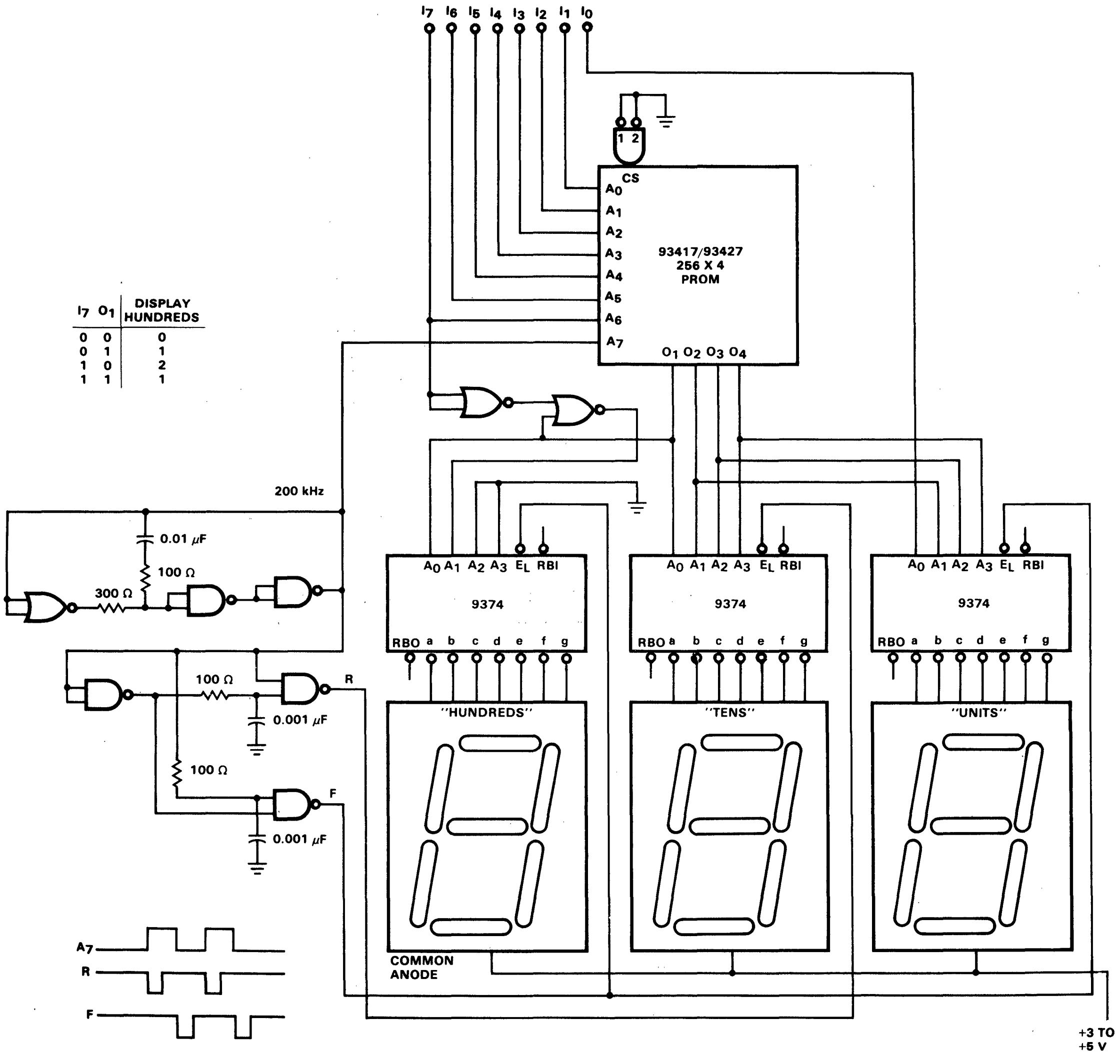


Fig. 6-5. Encoder/Decoder

8-BIT BINARY TO 3-DIGIT DECIMAL DISPLAY DECODER

The popular 8-bit microprocessor has created a demand for 8-bit binary-to-decimal display converters, since a 3-digit number is not only easier to read, interpret, and remember than an 8-bit binary word, but also requires less panel space for read-out. ROMs and PROMs are particularly well suited for such code conversion, but a brute-force textbook design would require a 256 x 10 ROM plus three 7-segment decoder/drivers. The circuit in *Figure 6-6* achieves the same result with only a 256 x 4 PROM, three 7-segment decoder/drivers with input latches (9374) and two gate packages.



I_7	O_1	DISPLAY HUNDREDS
0	0	0
0	1	1
1	0	2
1	1	1

Fig. 6-6. 8-Bit Binary to 3-Digit Decimal Display Decoder

The total number of required PROM bits is reduced by excluding the least significant bit from the code conversion ($LSB_{in} \equiv LSB_{out}$) and by generating the three possible values of 'hundreds' information (0, 1, 2), according to the small truth table, by combining the I_7 input with one PROM output. This reduces the PROM requirement to 128 x (3+4+1) bits. Since a PROM of this size is not commercially available, a 256 x 4 PROM can be used in a time multiplexed arrangement with the latches at the decoder inputs for demultiplexing the PROM output information.

PROGRAMMED LOGIC CONTROLLER

This easy-to-understand TTL/MSI oriented design for a small dedicated controller is applicable where a minicomputer would be too expensive and a microcomputer would be too slow, too cumbersome to program or too complicated to understand. This concept uses one or two dozen inexpensive TTL/MSI circuits plus one or two PROMs and can implement practically any control function with up to 16 inputs and up to 50 outputs.

A simple open loop controller, as found in every washing machine, is a good beginning. Here a synchronous motor drives a reduction gear, which in turn drives a drum with programming pins or cams that activate the output switches (*Figure 6-7*). The electronic equivalent of this pin-drum controller is shown in *Figure 6-8* where an oscillator (motor) drives a ÷ 256 counter (gearbox) addressing a PROM (drum) with eight outputs. If the objective were to generate eight arbitrarily changing, completely random outputs, the design would stop here. Fortunately the real world does not usually require outputs that change in a completely random fashion. Rather, the requirement is to be able to activate and hold certain outputs (solenoids, valves, lights, etc.) starting at a certain position in the program, and deactivate them later at a different position. For this purpose the PROM represents an overdesign. It is simple to reduce the number of PROM outputs and/or increase the number of system outputs by using additional inexpensive MSI components.

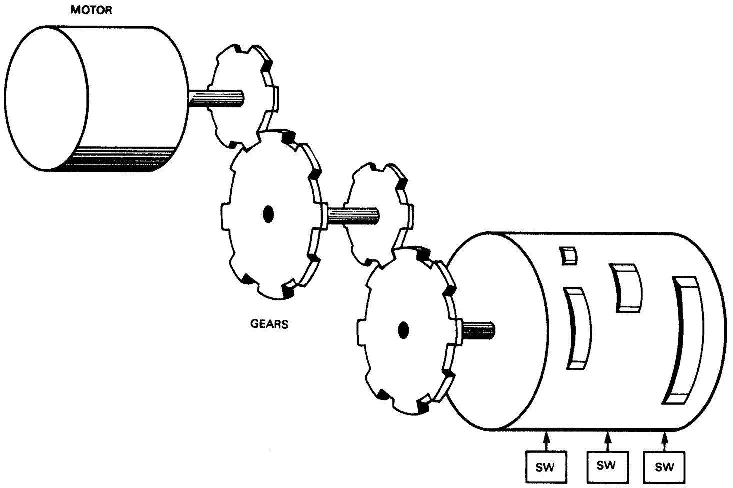


Fig. 6-7. Simple Open-Loop Controller

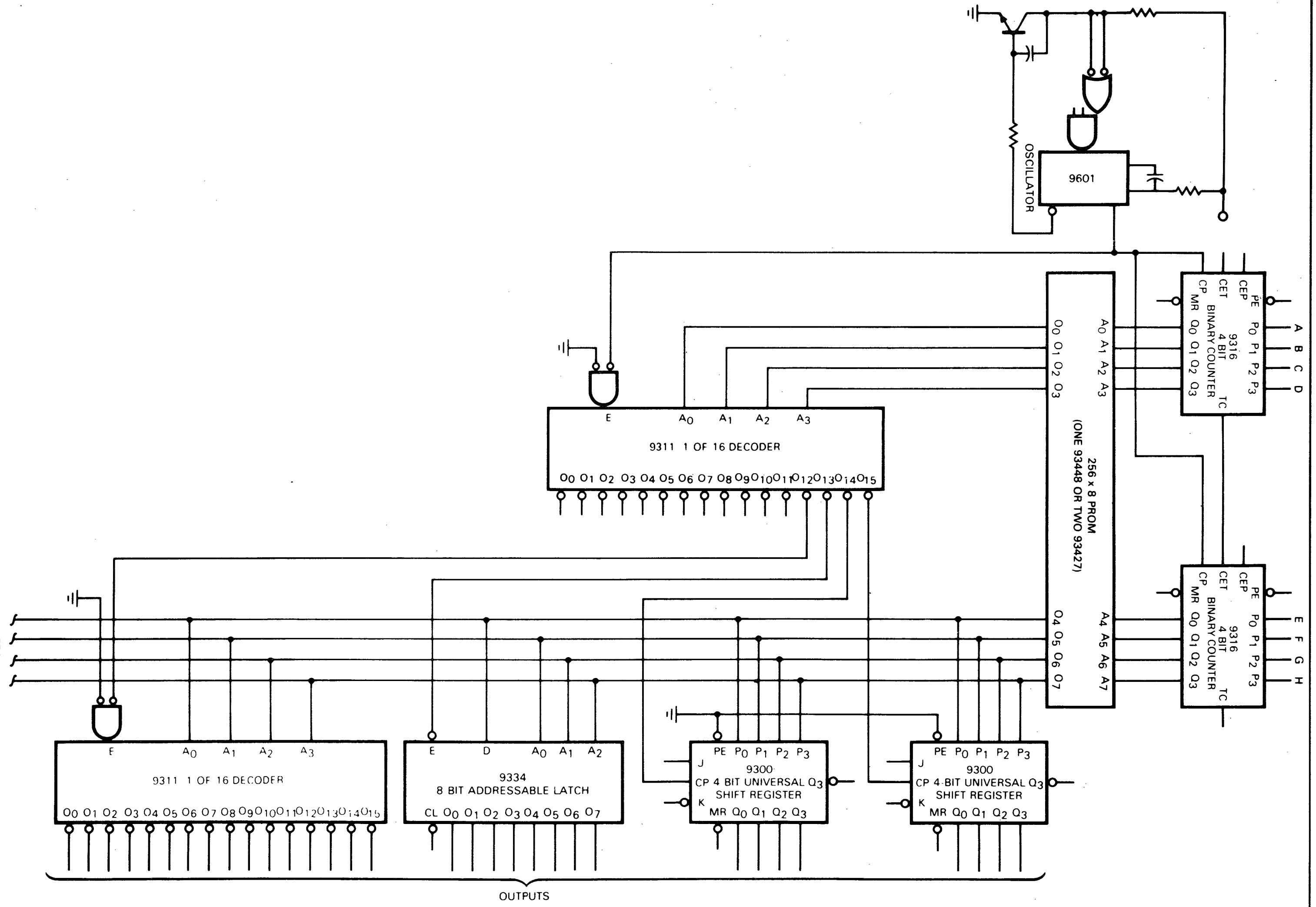


Fig. 6-8. Programmed Logic Controller, Open Loop

The PROM outputs can be interpreted as addresses and instructions. As shown in the example of *Figure 6-8*, the first four outputs are an address activating, through a 9311 1-of-16 decoder, any one of up to 16 MSI circuits. The remaining four PROM outputs are used as instructions to the selected MSI circuit. Address 15 activates the first 4-bit register, changing its four outputs to the associated 4-bit instruction code coming out of the PROM. Address 14 selects another 4-bit register while address 13 selects a 9334 8-bit addressable latch. The 4-bit instruction determines which output is to be changed and to what level it is to be changed. For an insignificant increase in cost, the number of outputs has been increased from eight to over 64, with the constraint that only one group can be changed simultaneously.

This is still a very unsophisticated open-loop controller. It can be improved by adding a controlled speed reduction, consisting of a presettable counter (*Figure 6-9*). One instruction can change the instruction rate to any one of 16 values, maintaining it there until it is changed again. The real power of this design is shown, however, when a conditional feedback, or – in programming terms – a conditional jump capability is included (*Figure 6-10*). One of the 16 addresses is used to interrogate the status of eight input lines, and the associated instruction defines which input is to be interrogated and which level is the desired one. The subsequent PROM output is then not interpreted as an address/instruction pair, but rather as a program jump address. If the input under test has the expected level (HIGH or LOW), this jump address is loaded into the program counter and the program continues from this new address. If the input under test does not have the expected level, the jump address is ignored and the program continues without a jump.

Obviously this design can be made even more sophisticated by adding arithmetic capabilities, data memory, address stacks, etc., but carrying this too far would defeat the basic advantage of this design, its simplicity and economy. The advantage of this approach over conventional logic implementation lies in the flexibility that it gives to the circuit designer.

The design of a small control system usually starts with a clear knowledge of the number of outputs and inputs required and their electrical characteristics. But, the exact definition of how the control inputs affect the outputs (under all normal and abnormal circumstances) takes most of the time and leads to most of the usual errors. The classical logic design can only start when the system design is finished, and will require extensive changes if the system design is changed due to mistakes or new requirements.

The programmed controller, however, can be designed, constructed and tested as soon as the required inputs and outputs are defined, essentially simultaneous with the detailed systems design. System design, programming, and circuit design can be done in parallel, significantly reducing turn-around time. System changes can be implemented by changing the PROM, and can be tested and verified in hours instead of weeks.

ADDRESS AND WORD EXPANSION

Many PROM applications require expansion of the word length or the number of words. *Figure 6-11* shows the interconnection of two 256 x 4-bit memories to develop a 256 x 8-bit array. Address expansion is shown in *Figure 6-12*, which illustrates the use of two 256 x 4-bit memories to form a 512 x 4-bit array. A 512 x 6-bit array utilizing three 256 x 4-bit devices is shown in *Figure 6-13*. As a final example of the expansion versatility of PROMs, *Figure 6-14* shows how sixteen 512 x 4-bit memories are interconnected to form a 2048 x 16-bit array.

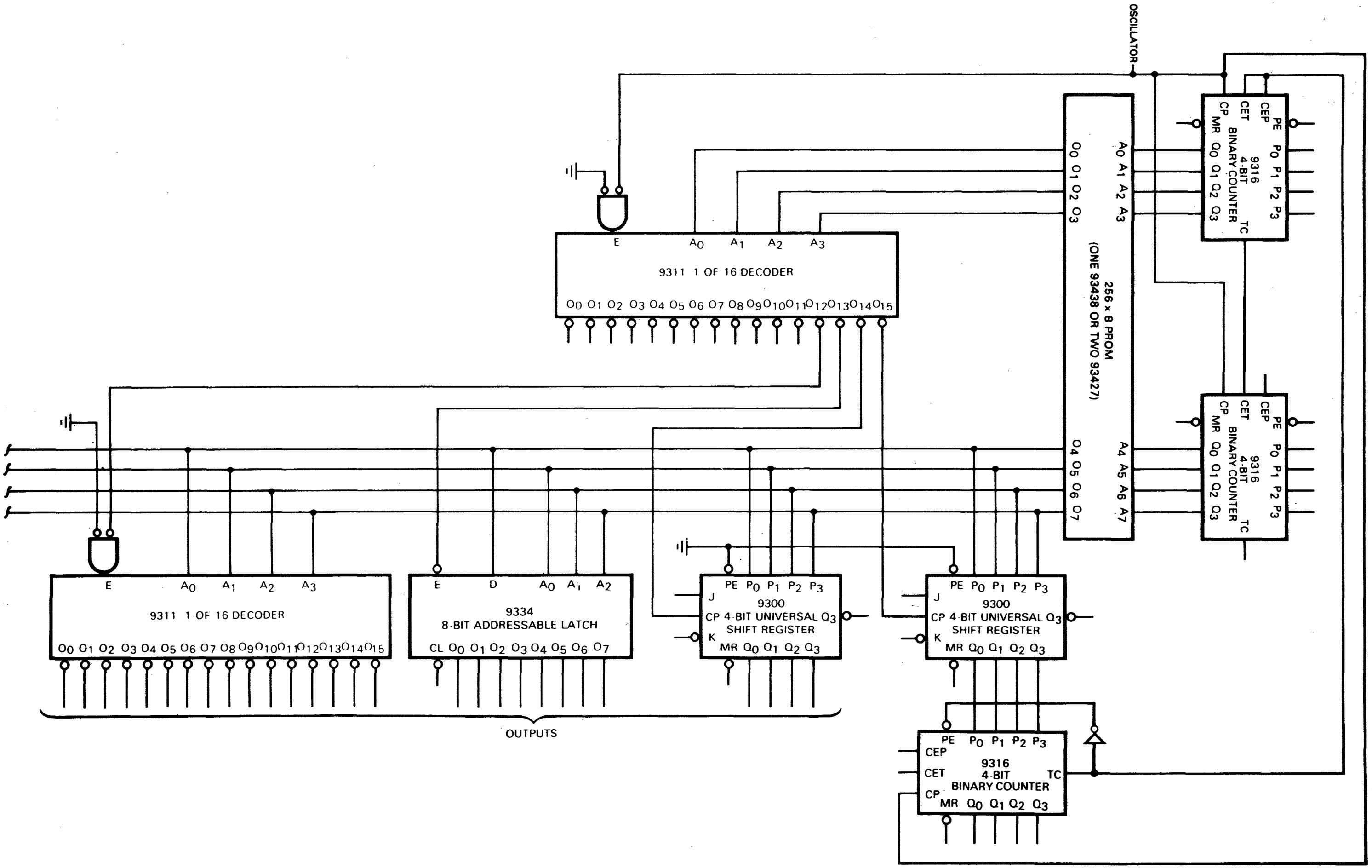


Fig. 6-9. Programmed Logic Controller, Open Loop, Variable Speed

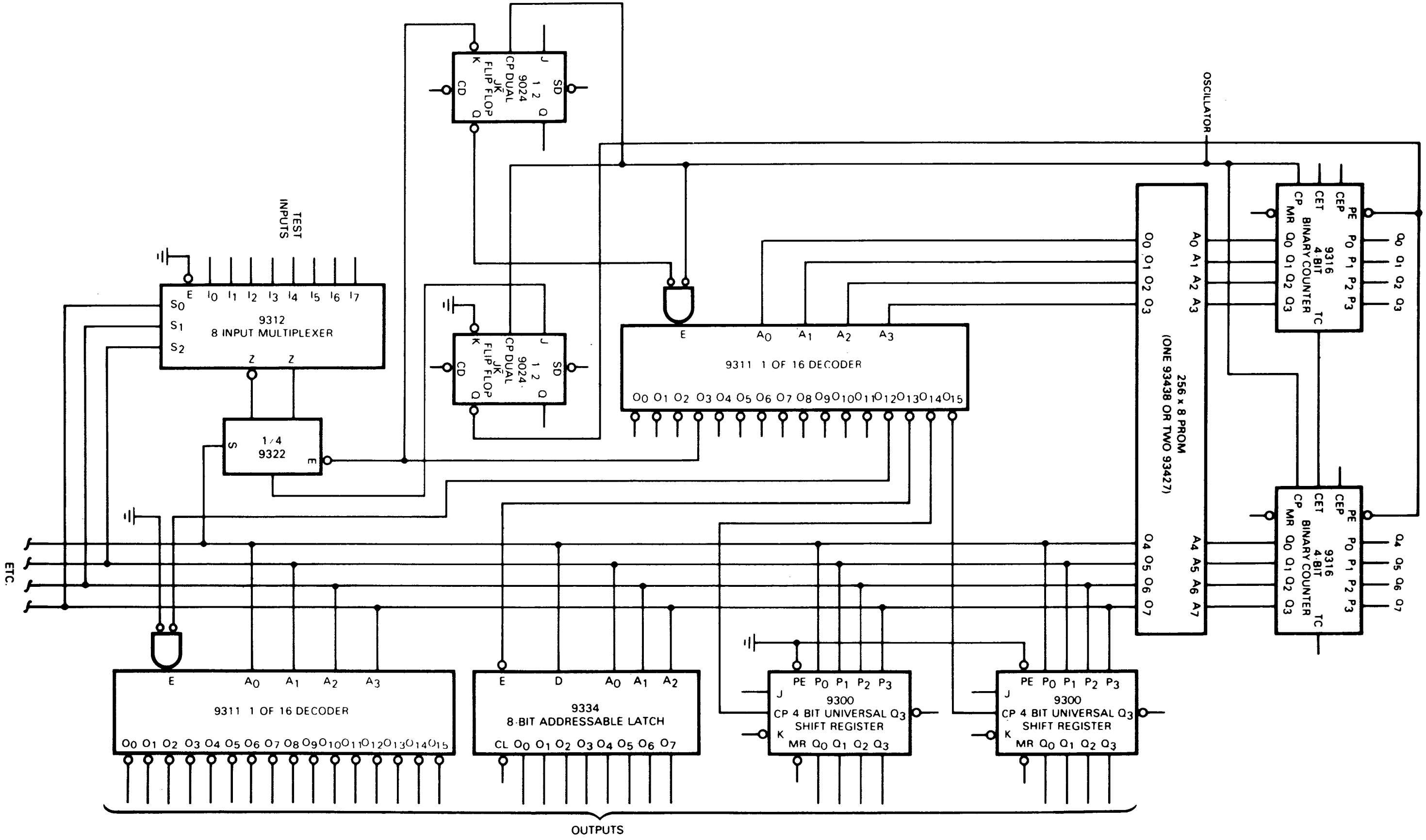


Fig. 6-10. Programmed Logic Controller, Conditional Jump

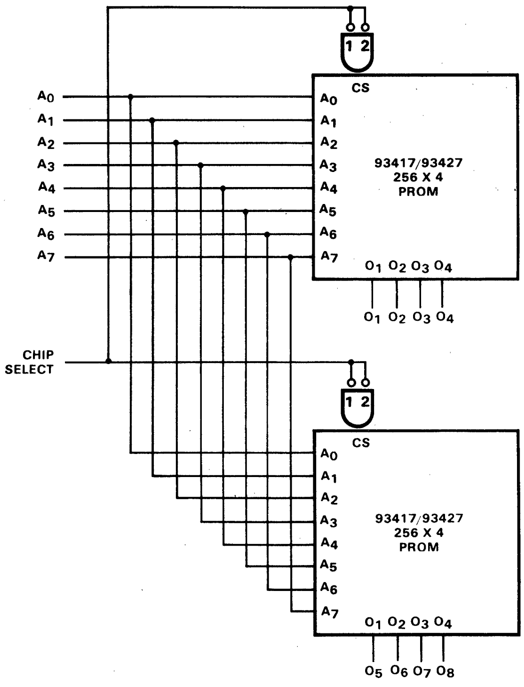


Fig. 6-11. Word-Size Expansion, 256 x 8-Bit Array

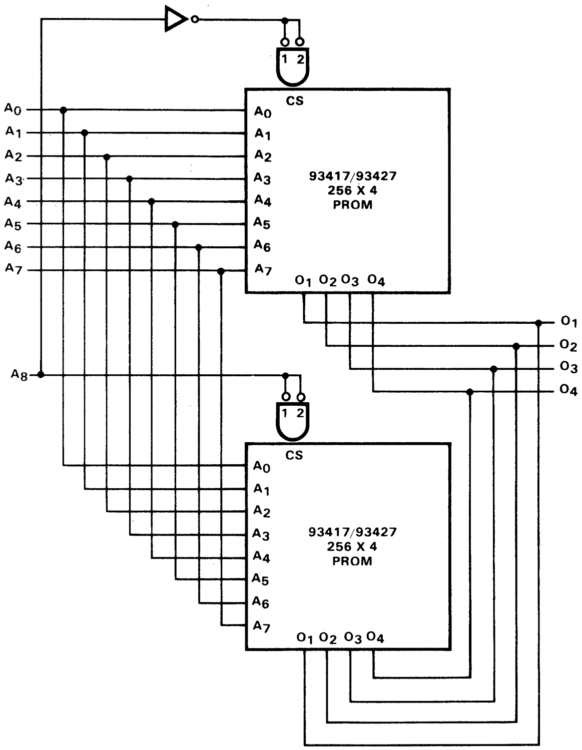


Fig. 6-12. Address Expansion, 512 x 4-Bit Array

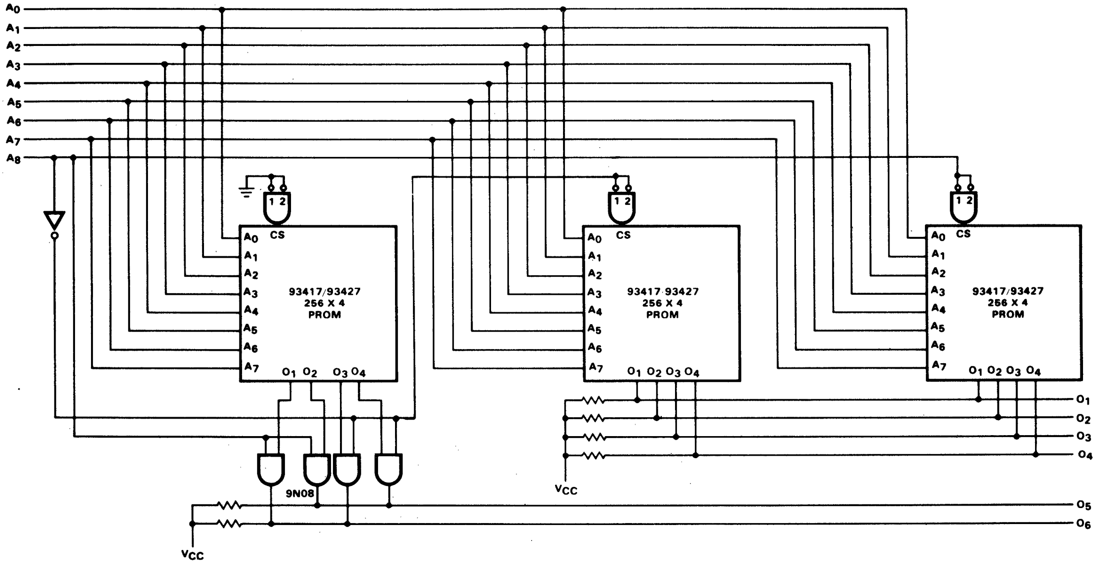


Fig. 6-13. 512 x 6-Bit Array

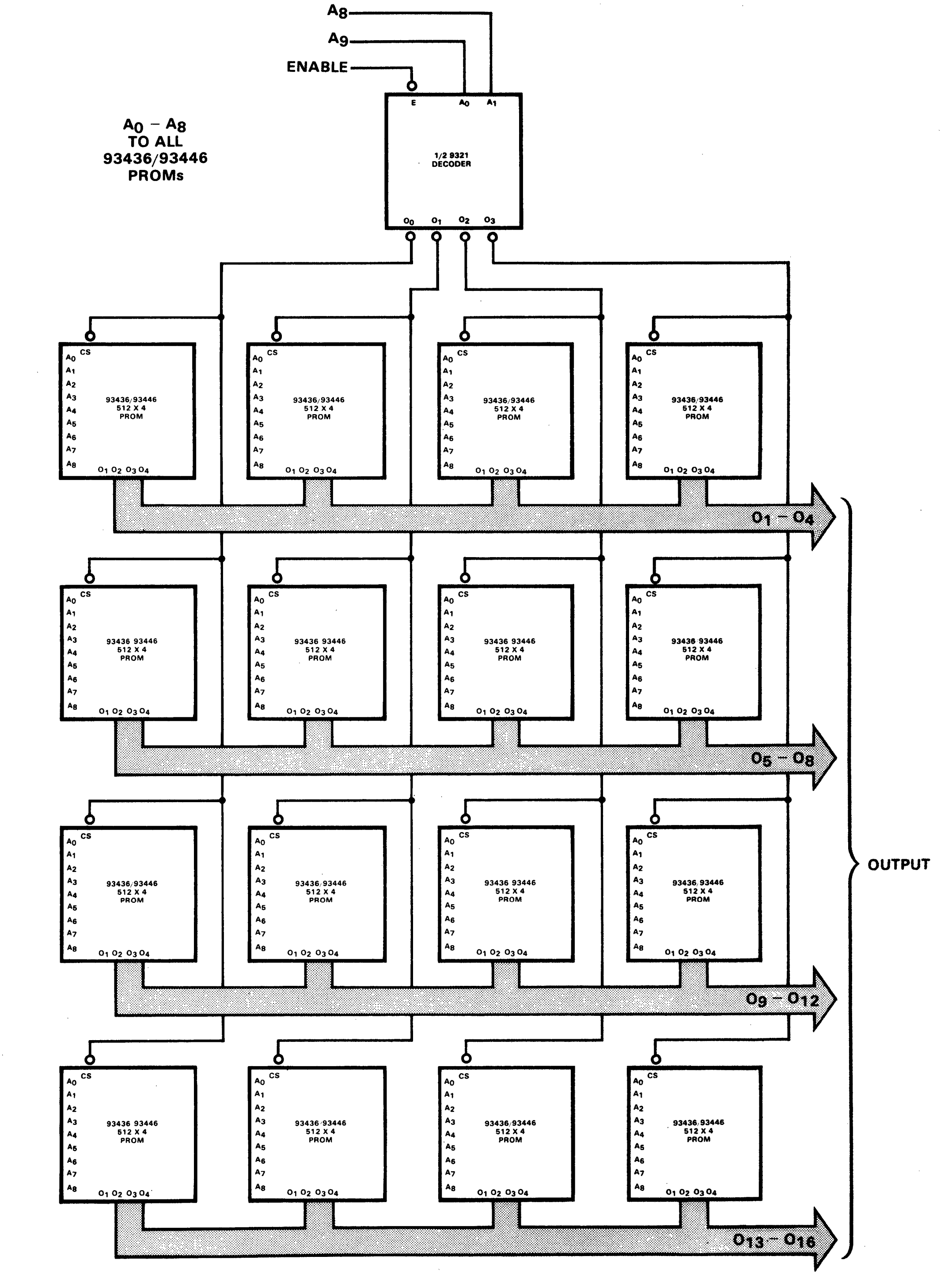


Fig. 6-14. Combined Word and Address Expansion, 2048 x 16-Bit Array Using 512 x 4-Bit PROMs

PROM PROGRAMMING

Fairchild Isoplanar Schottky TTL PROMs are manufactured with all bits in the HIGH state. Any bit can be programmed LOW by following the procedure below and referring to the specifications in *Table 6-1.* When a programming pulse is applied to a bit (output), current is driven into the circuit as shown in *Figure 6-1.* Due to careful device design, almost all of the energy is delivered to the fuse consisting of a notched nichrome link. Minimal losses to leakage paths and intermediate circuits permit the link to open rapidly with a low-energy programming pulse. This in turn enhances reliability. These nichrome fuses actually program on the rise time of the programming pulse which permits reduction in programming pulse width for high-speed low-energy programming.

Programming Procedure (refer to *Table 6-1*)

1. Apply the proper power, $V_{CC} = 5.0$ V, and ground.
2. Select the word to be programmed by applying the appropriate levels to the Address pins.
3. Select the chip for programming by deselecting it; apply logic "1" (input HIGH) to the active LOW Chip Select input(s) or logic "0" (LOW) to the active HIGH input(s) if present. All PROMs have active LOW CS inputs; only the 93438/93448 have active HIGH CS inputs as well.
4. Apply a 21 V programming pulse to the output associated with the bit to be programmed. The other outputs may be left open or tied to any logic "1" (output HIGH), *i.e.,* 2.4 V to 4.0 V. Note that only one output at a time may be programmed.
5. To verify a LOW in the bit just programmed, remove the programming pulse from the output, lower V_{CC} to 4.4 V, and sense the output after applying a logic LOW to the active LOW Chip Select(s) and a logic HIGH to any active HIGH Chip Select(s).
6. Repeat steps 1–5 as necessary for each bit that requires programming.

Although, for convenience, most programming is done by commercially available programmers, the circuit shown in *Figure 6-15* can be used to sequentially program all bits of a given word for up to an 8-output PROM. Selection of the bit patterns to be programmed is made by the bit switches while the address of the word to be selected is selected by the address switches. The contents of the PROM at the address, defined by the address switches, are displayed on the eight FLV117 LEDs until the program switch is depressed. If a bit is a logic HIGH or the chip is deselected, the associated LED is turned on with current supplied by the 390 Ω resistors. If the content of the PROM is a logic LOW and the PROM is enabled, the

PARAMETER	SYMBOL	MIN	RECOMMENDED VALUE	MAX	UNITS	COMMENTS
Address Input	V_{IH}	2.4	5.0	5.0	V	Do not leave inputs open
	V_{IL}	0	0	0.4	V	
Chip Select	$\overline{CS}_1, \overline{CS}_2$	2.4	5.0	5.0	V	Either or both
	CS_3, CS_4	0	0	0.4	V	
Programming Voltage Pulse	V_{OP}	20	21	21	V	Applied to output to be programmed
Programming Pulse Width	t_{pw}	0.05	0.18	50	ms	
Duty Cycle Programming Pulse			20	20	%	Maximum duty cycle to maintain $T_C < 85°C$
Programming Pulse Rise Time	t_r	0.5	1.0	3.0	μs	
Number of Required Pulses		1	4	8		
Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Case Temperature	t_c		25	85	°C	
Programming Pulse Current	I_{OP}			100	mA	If pulse generator is used, set current limit to this max value.
Low V_{CC} Read	V_{CC}		4.4	5.0	V	Programming Read Verify

Table 6-1. Programming Specifications

output is logic LOW turning the LEDs off. The 1N4002s isolate the LEDs from the 21 V programming pulse. One-half of a 9024 JK flip-flop is used as a switch debouncer while the other half is the "run" flip-flop. The 9601 is a 10 kHz oscillator. When the program is initiated by depressing the program switch, the first half of the 9024 (switch debouncer) is set and clocks the other half of the 9024 ("run" flip-flop) to the "run" state. This enables the pulse and bit counters to operate and enables the PROM for programming. The pulse counter is preset to 5 to provide the 20% duty factor and the bit counter is preset to 8. To avoid overlap problems between the programming pulse, the chip enable and the scan, the bit counter advances when the pulse counter goes from state 3 to state 4. The bit to be programmed is decoded by the 9301 and wired-OR with the bit switch. The OR gate is a high-voltage driver supplying the drive to the programming transistors. When the last bit has been programmed, the counter presets itself and resets the "run" flip-flop. The programming sequence is now complete for the selected word.

It is often convenient to program PROMs mounted on a circuit board in wired-OR configurations such as the one shown in *Figure 6-14*. The Fairchild devices are particularly convenient for board programming in that only the Chip Select and Output pins need to be accessed to program the part. *Figure 6-16* shows the circuit and procedure for board programming. The programmer is connected to the output bus as shown, while the Chip Selects are driven by a decoder with elevated voltage levels. Thus, all that is required for board programming is the ability to raise V_{CC}, V_{EE} and the Device Select inputs on the decoder 7.6 V above their normal operational levels. The standard 21 V programming pulse will now program bits in the PROM having an active LOW Chip Select input of approximately 7.8 V.

POWER SWITCHING

Power dissipation in a bipolar PROM can be reduced by applying power only when the PROM is selected or when the outputs are required to be valid. Some bipolar PROMs have been developed with on-chip power switching circuitry but they are much slower than standard PROMs. An external switching circuit, such as that shown in *Figure 6-17*, provides power switching with little loss in speed.

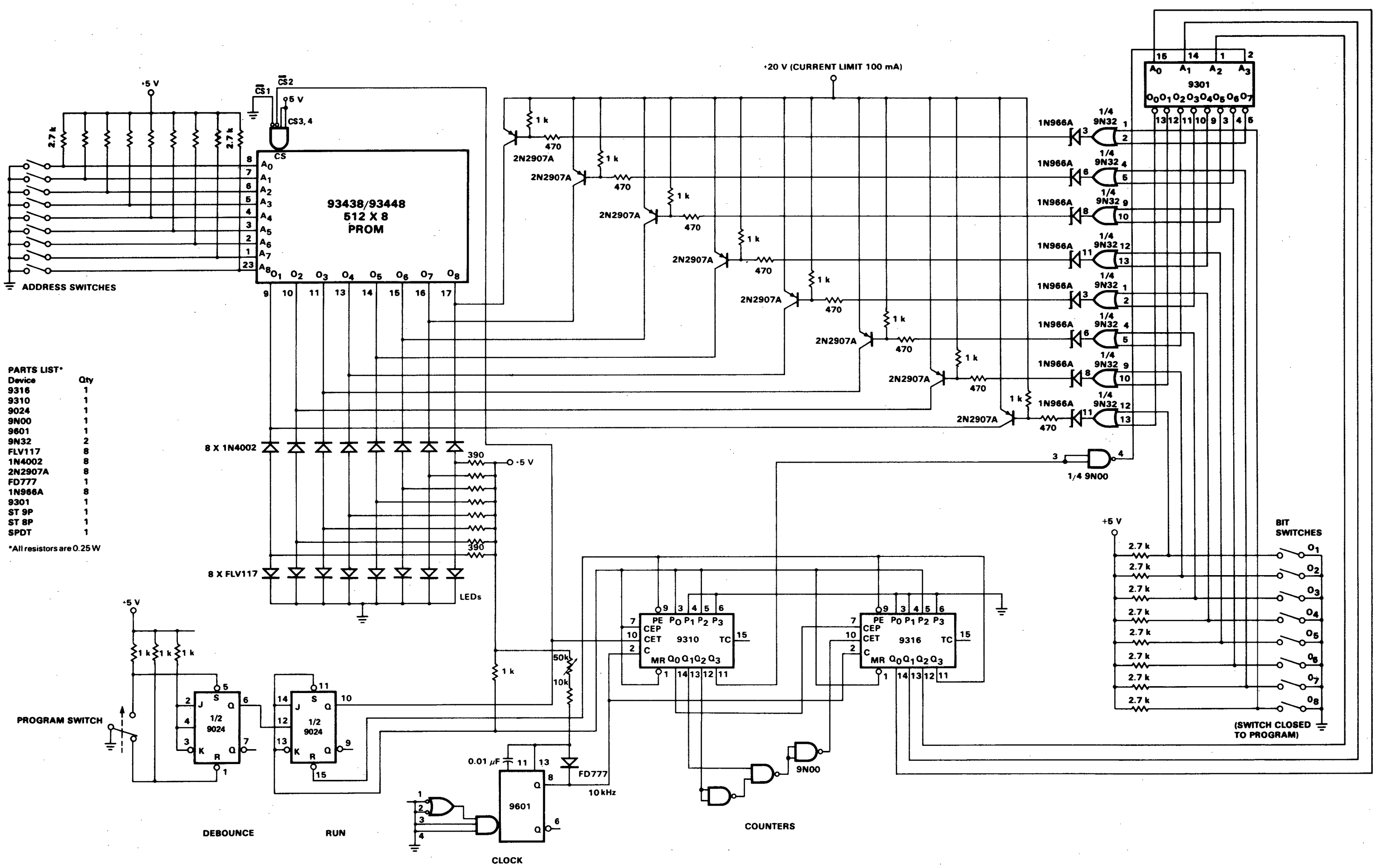
The switching circuit must be capable of switching the worst-case power supply current of the PROM, have very short switching delays and have a small collector-to-emitter voltage drop V_{CE}. This is important because the power supply voltage at the PROM is reduced by the amount of this voltage drop. A high-speed pnp saturated logic switch, *e.g.,* the 2N5455, and a 100 pF speed-up capacitor provide a switching delay of approximately 10 ns at the V_{CC} pin. Using this circuit, the effective access time, which is the delay between applying the power strobe to the V_{CC} pin and availability of valid data, is approximately 10% greater than the normal address access time t_{AA}.

Conditions during power switching, both on and off, must also be considered. *Figure 6-18* shows the power strobe, V_{CC} and HIGH and LOW output waveforms for an open-collector and a 3-state device. Note the glitch in the HIGH output of both parts during power-up and the exponential rise of the LOW output during power-down. Care should be taken in system design to ensure that transient conditions do not adversely affect other parts of the system.

6

It is also important to consider the effect of the collector-emitter voltage drop V_{CE} across the switching transistor on PROM performance. Fairchild Isoplanar PROMs are capable of operating over the full commercial range (0° to 75°C) with the standard 5 V ± 5% power supply reduced by a V_{CE} of 300 mV. Military grade devices operate from 0° to 125°C with the standard 5 V ± 10% power supply reduced by 300 mV. For operating to −55°C, screened parts or tightened power supply specs are recommended.

The steady state condition must also be considered. In a typical memory array, inputs and/or outputs of several devices are bussed together (see *Figure 6-13*). Therefore, PROMs that are to be used in power-switched arrays should be specified for input and output leakage under power-down conditions, since any leakage in the powered-down devices loads the powered device(s). The allowable leakage is a function of the number of devices bussed together and the drive requirements of the bus. Since manufacturers do not normally specify devices under power-down conditions, customer specifications should reflect the actual system requirements under power-down operation.

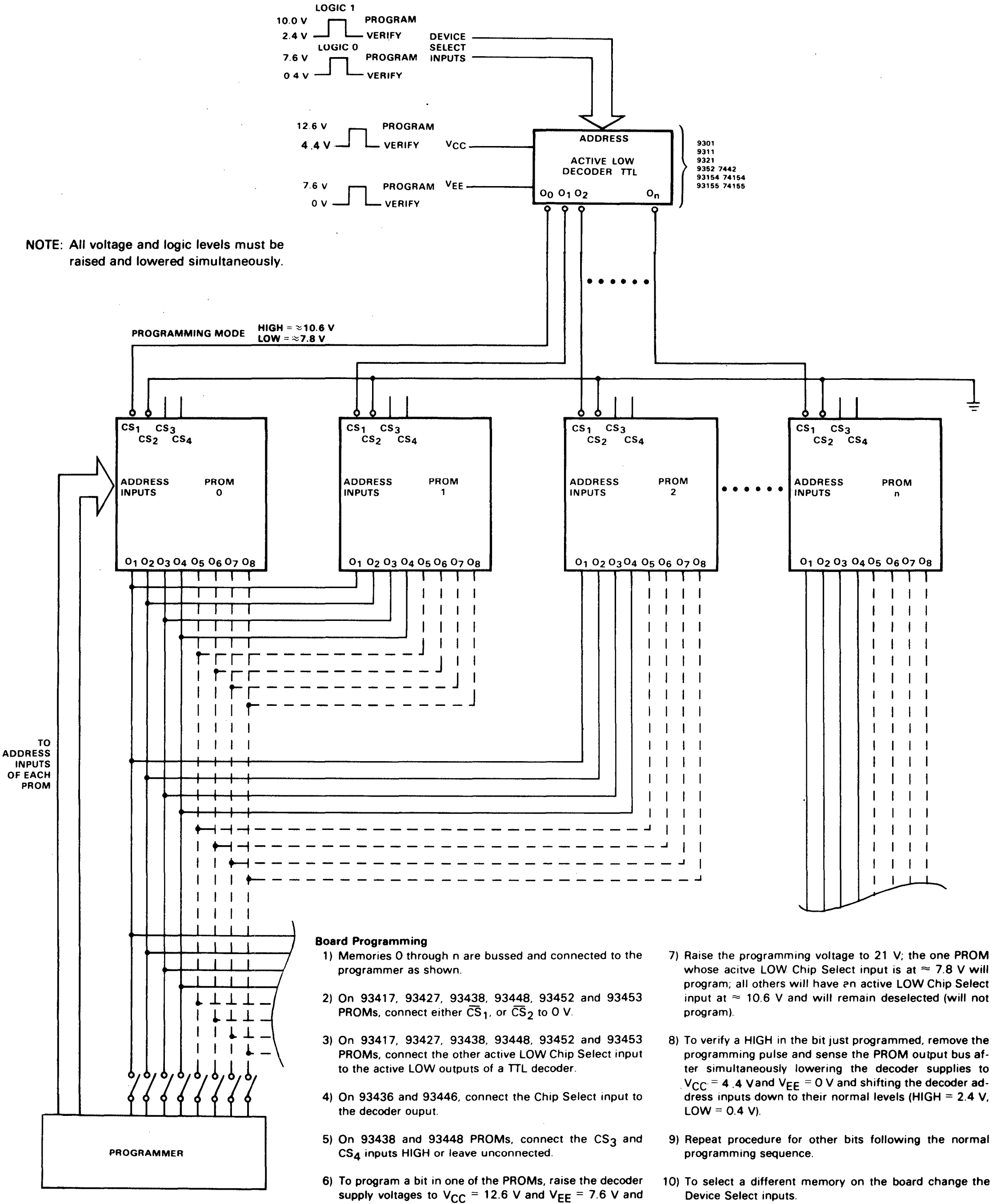


PARTS LIST*

Device	Qty
9316	1
9310	1
9024	1
9N00	1
9601	1
9N32	2
FLV117	8
1N4002	8
2N2907A	8
FD777	1
1N966A	8
9301	1
ST 9P	1
ST 8P	1
SPDT	1

*All resistors are 0.25 W

Fig. 6-15. PROM Programming Circuit



NOTE: All voltage and logic levels must be raised and lowered simultaneously.

Board Programming

1) Memories 0 through n are bussed and connected to the programmer as shown.

2) On 93417, 93427, 93438, 93448, 93452 and 93453 PROMs, connect either $\overline{CS}_1$, or $\overline{CS}_2$ to 0 V.

3) On 93417, 93427, 93438, 93448, 93452 and 93453 PROMs, connect the other active LOW Chip Select input to the active LOW outputs of a TTL decoder.

4) On 93436 and 93446, connect the Chip Select input to the decoder ouput.

5) On 93438 and 93448 PROMs, connect the CS_3 and CS_4 inputs HIGH or leave unconnected.

6) To program a bit in one of the PROMs, raise the decoder supply voltages to V_{CC} = 12.6 V and V_{EE} = 7.6 V and select the appropriate device via the Device Select inputs (HIGH = 10.0 V, LOW = 7.6 V).

7) Raise the programming voltage to 21 V; the one PROM whose acitve LOW Chip Select input is at ≈ 7.8 V will program; all others will have an active LOW Chip Select input at ≈ 10.6 V and will remain deselected (will not program).

8) To verify a HIGH in the bit just programmed, remove the programming pulse and sense the PROM output bus after simultaneously lowering the decoder supplies to V_{CC} = 4.4 V and V_{EE} = 0 V and shifting the decoder address inputs down to their normal levels (HIGH = 2.4 V, LOW = 0.4 V).

9) Repeat procedure for other bits following the normal programming sequence.

10) To select a different memory on the board change the Device Select inputs.

Fig. 6-16. Board Programming

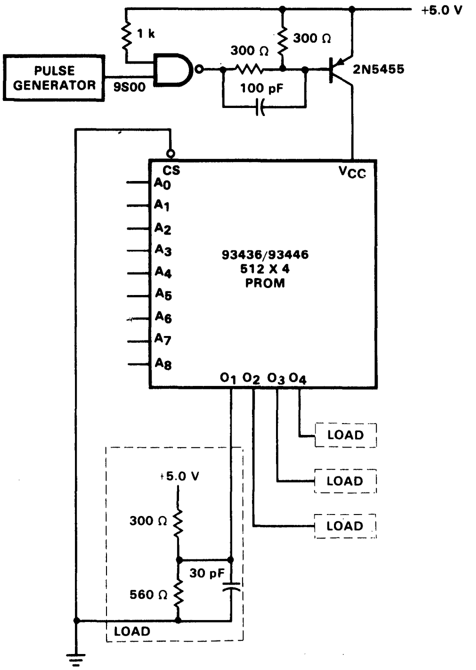
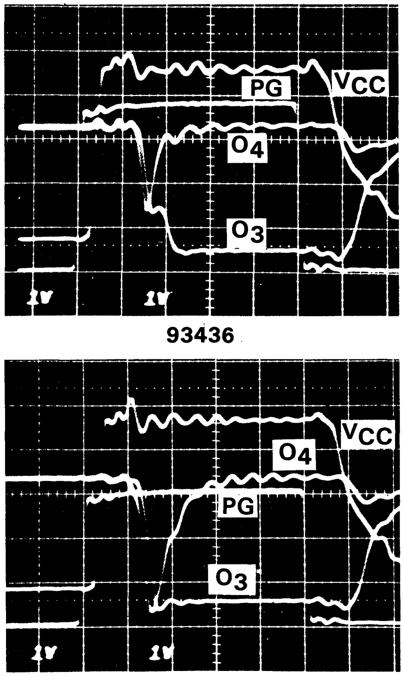


Fig. 6-17. Power Switching Circuit



93436

93446

Fig. 6-18. Output Waveforms

PROM MARKING

Since PROMs come marked with a device type for the unprogrammed part, it is usually necessary for the user to mark the parts after programming so that he can identify individual patterns. An ordinary pencil works well on the common white ceramic packages but any convenient marking method can be used as long as it is relatively permanent. Fairchild PROMs are marked with device type and date code on the lower 2/3 of the top surface. This leaves the upper 1/3 available for customer marking, which can be performed using a thermosetting ink such as Markem*. The ink can be applied with a stick stamp readily available from many suppliers. Acetone removes illegible or incorrect marks and isopropyl alcohol can be used for clean up. After marking, the packages should be baked for one hour at 150°C to fix the ink.

REFERENCES

1. Barnes, D.E., and Thomas, J.E., "Reliability Assessment of a Semiconductor Memory by Design Analysis," IEEE 12th Annual Proceedings on Reliability Physics, (1974).
2. Eisenberg, P.H., and Nalder, R., "Nichrome Resistors in Programmable Read Only Integrated Circuits," IEEE 12th Annual Proceedings on Reliability Physics, (1974).
3. Mo, R.S., and Gilbert, D.M., "Reliability of NiCr 'fusible link' used in PROMs," Journal of Electrochemical Society, Vol 120, No. 7 (1973), p. 1001.
4. Franklin, P., and Burgess, D., "Reliability Aspects of Nichrome Fusible Link PROMs," IEEE 12th Annual Proceedings on Reliability Physics, (1974).
5. "The New LSI," Electronics, (July 10, 1975).
6. Devaney, J.R., and Sheble III, A.M., "Plasma Etching and Other Problems," IEEE 12th Annual Proceedings on Reliability Physics, (1974).

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*Markem Corporation, 150 Congress Street, Keen, NH 03431. Stock numbers 8055521 for cerdip, 8058791 for solderseal (white) ceramic or 805933 for plastic.

93454/93464 DATA CARD FORMAT

The most efficient method of ordering the 93454/93464 is to punch the desired truth table on punched cards in the format described below. Fairchild will generate mask and test program data directly from these inputs. This eliminates the chance of error when transcribing inputs from a handwritten truth table.

Data should be provided on a deck of 173 standard 80 column cards containing the following information.

CARD NO. 1 – Customer Identification

Column	Content
1–80	Customer Name, Drawing or Specification control number, date, "93454" or "93464", "XC" or "XM" (See Guaranteed Operating Ranges). This card is entered in free format.

CARD NO.2 – Fairchild SL Number and Low Count

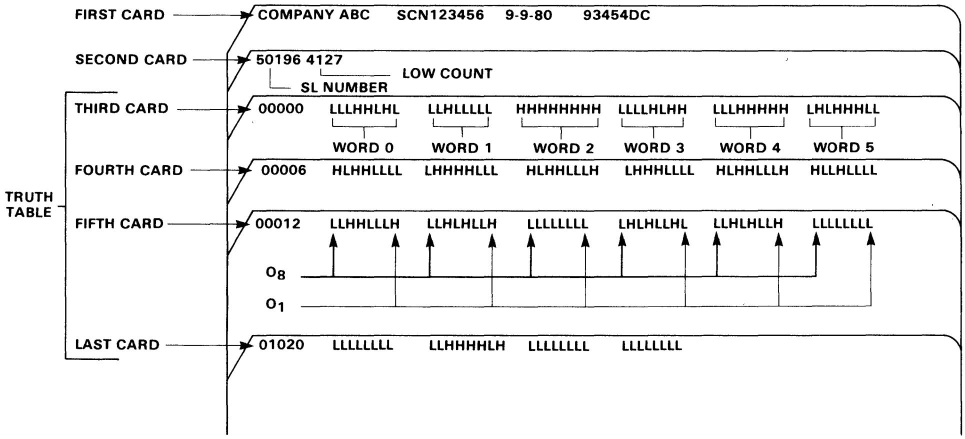
Column	Content
1–5	Punch the 5-digit Fairchild SL number. This SL number is supplied by the factory through your Fairchild sales representative.
7–10	Punch the 4-digit number which represents the total number of "L"s in the data pattern. (For verification of data).

CARDS NO. 3 through 173 – Truth Table Deck

Each card will contain instructions for the output levels for six input words.

Column	Content
1–5	Punch the numerals representing the decimal address of the first word on that card. The words are entered sequentially (0 through 1023).
10–17	Punch the desired combination of "H"s and "L"s representing the output levels for outputs O_8, O_7, O_6, O_5, O_4, O_3, O_2 and O_1 (in that order), for the first word on the card. "H" signifies a HIGH voltage on the data line. "L" signifies a LOW voltage on the data line.
21–28	Punch the desired combination of "H"s and "L"s representing the output levels for the second word on the card.
32–39	Punch the desired combination of "H"s and "L"s representing the output levels for the third word on the card.
43–50	Punch the desired combination of "H"s and "L"s representing the output levels for the fourth word on the card.
54–61	Punch the desired combination of "H"s and "L"s representing the output levels for the fifth word on the card.
65–72	Punch the desired combination of "H"s and "L"s representing the output levels for the sixth word on the card.

Example:



CUSTOMER CODING FORM

The customer can also specify the desired ROM code by using the 4K/8K-Bit TTL ROM and PROM Customer Coding Form (available from Fairchild) printed in the format below.

WORD NO.	OUTPUTS								REMARKS
	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	
0	L	L	L	H	H	L	H	L	
1	L	L	H	L	L	L	L	L	
2	H	H	H	H	H	H	H	H	
↓	↓	↓	↓	↓	↓	↓	↓	↓	
1022	L	L	L	L	L	L	L	L	
1023	L	L	L	L	L	L	L	L	

93454/93464 ADDRESS SCHEME

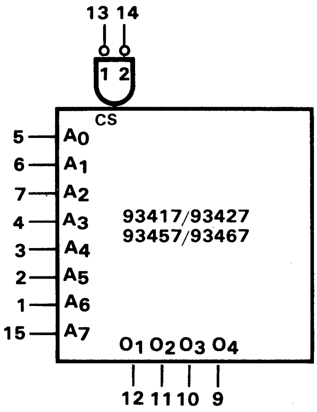
The 1024 decimal addresses are defined by their binary equivalent with A_9 = MSB and A_0 = LSB as shown below.

	BINARY ADDRESS INPUTS									
DECIMAL ADDRESS	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	L	L	L	L	L	L	L	L	L	L
1	L	L	L	L	L	L	L	L	L	H
2	L	L	L	L	L	L	L	L	H	L
3	L	L	L	L	L	L	L	L	H	H
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
1023	H	H	H	H	H	H	H	H	H	H

"H" signifies a HIGH voltage applied to the address inputs. "L" signifies a LOW voltage applied to the address inputs.

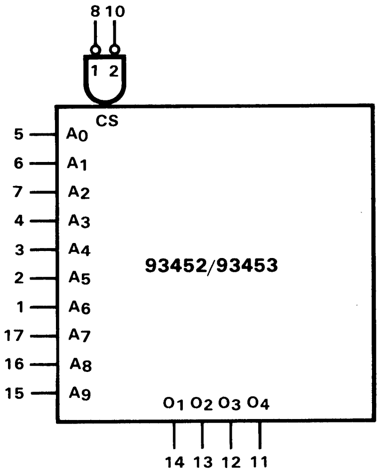
1K/2K/4K-BIT TTL ROM AND PROM CUSTOMER CODING FORM

1K-BIT LOGIC SYMBOL
256 X 4 BITS



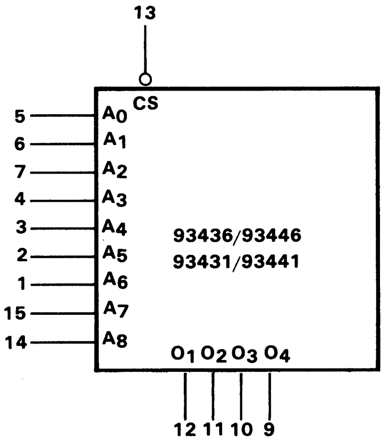
V_{CC} = Pin 16
GND = Pin 8

4K-BIT LOGIC SYMBOL
1024 X 4 BITS



V_{CC} = Pin 18
GND = Pin 9

2K-BIT LOGIC SYMBOL
512 X 4 BITS



V_{CC} = Pin 16
GND = Pin 8

ROM/PROM TABLE

SIZE	ROM	PROM	ORGANIZATION	PINS	OUTPUTS	T_{AA} TYP	TECHNOLOGY
1K	93457 93467	93417 93427	256 x 4	16	OC 3-S	25 ns	Schottky Isoplanar
2K	93431 93441	93436 93446	512 x 4	16	OC 3-S	30 ns	Schottky Isoplanar
4K		93452 93453	1024 x 4	18	OC 3-S	35 ns	Schottky Isoplanar

TRUTH TABLE FOR ROMs – 4-BIT WORDS

CUSTOMER ______________________________

CUSTOMER P/N ________________ **CUSTOMER DWG. NO.** ________________

FUNCTION ________________ **SL NO.** ________________

Customer's Authorizing Signature ________________ **Date** ________

Qualified Fairchild Representative ________________ **Date** ________

LEAST SIGNIFICANT BIT →

ADDRESS	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
PIN NO.										

WORD NO.	OUTPUTS				REMARKS
	04	03	02	01	
0					
1					
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WORD NO.	OUTPUTS				REMARKS
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WORD NO.	OUTPUTS				REMARKS
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WORD NO.	OUTPUTS				REMARKS
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WORD NO.	OUTPUTS				REMARKS
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WORD NO.	OUTPUTS				REMARKS
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WORD NO.	OUTPUTS				REMARKS
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WORD NO.	OUTPUTS				REMARKS
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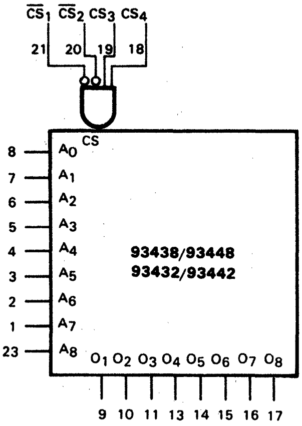
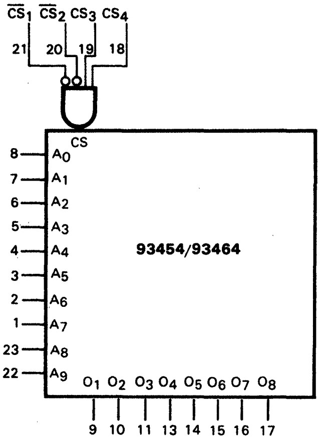
4K/8K-BIT TTL ROM AND PROM CUSTOMER CODING FORM

4K-BIT LOGIC DIAGRAM
512 X 8 BITS



V_{CC} = Pin 24
GND = Pin 12

8K-BIT LOGIC SYMBOL
1024 X 8 BITS



V_{CC} = Pin 24
GND = Pin 12

ROM/PROM TABLE

SIZE	ROM	PROM	ORGANIZATION	PINS	OUTPUTS	T_{AA} TYP	TECHNOLOGY
4K	93432 93442	93438 93448	512 x 8	24	OC 3-S	35 ns	Schottky Isoplanar
8K	93454 93464	– –	1024 x 8	24	OC 3-S	30 ns	

TRUTH TABLE FOR ROMs — 8-BIT WORDS

CUSTOMER ____

CUSTOMER P/N ____________________ CUSTOMER DWG. NO. ____________

FUNCTION ____________________________ SL NO. __________________

Customer's Authorizing Signature ____________________ Date ________

Qualified Fairchild Representative ____________________ Date ________

LEAST SIGNIFICANT BIT →

ADDRESS	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
PIN NO.										

WORD NO.	OUTPUTS								REMARKS
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WORD NO.	OUTPUTS								REMARKS
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DECIMAL TO BINARY/OCTAL CONVERSION TABLE FOR ROMs AND PROMs

(UP TO 1024 ADDRESSES)

DEC.	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	OCTAL
0	0	0	0	0	0	0	0	0	0	0	0000
1	0	0	0	0	0	0	0	0	0	1	0001
2	0	0	0	0	0	0	0	0	1	0	0002
3	0	0	0	0	0	0	0	0	1	1	0003
4	0	0	0	0	0	0	0	1	0	0	0004
5	0	0	0	0	0	0	0	1	0	1	0005
6	0	0	0	0	0	0	0	1	1	0	0006
7	0	0	0	0	0	0	0	1	1	1	0007
8	0	0	0	0	0	0	1	0	0	0	0010
9	0	0	0	0	0	0	1	0	0	1	0011
10	0	0	0	0	0	0	1	0	1	0	0012
11	0	0	0	0	0	0	1	0	1	1	0013
12	0	0	0	0	0	0	1	1	0	0	0014
13	0	0	0	0	0	0	1	1	0	1	0015
14	0	0	0	0	0	0	1	1	1	0	0016
15	0	0	0	0	0	0	1	1	1	1	0017
16	0	0	0	0	0	1	0	0	0	0	0020
17	0	0	0	0	0	1	0	0	0	1	0021
18	0	0	0	0	0	1	0	0	1	0	0022
19	0	0	0	0	0	1	0	0	1	1	0023
20	0	0	0	0	0	1	0	1	0	0	0024
21	0	0	0	0	0	1	0	1	0	1	0025
22	0	0	0	0	0	1	0	1	1	0	0026
23	0	0	0	0	0	1	0	1	1	1	0027
24	0	0	0	0	0	1	1	0	0	0	0030
25	0	0	0	0	0	1	1	0	0	1	0031
26	0	0	0	0	0	1	1	0	1	0	0032
27	0	0	0	0	0	1	1	0	1	1	0033
28	0	0	0	0	0	1	1	1	0	0	0034
29	0	0	0	0	0	1	1	1	0	1	0035
30	0	0	0	0	0	1	1	1	1	0	0036
31	0	0	0	0	0	1	1	1	1	1	0037
32	0	0	0	0	1	0	0	0	0	0	0040
33	0	0	0	0	1	0	0	0	0	1	0041
34	0	0	0	0	1	0	0	0	1	0	0042
35	0	0	0	0	1	0	0	0	1	1	0043
36	0	0	0	0	1	0	0	1	0	0	0044
37	0	0	0	0	1	0	0	1	0	1	0045
38	0	0	0	0	1	0	0	1	1	0	0046
39	0	0	0	0	1	0	0	1	1	1	0047
40	0	0	0	0	1	0	1	0	0	0	0050
41	0	0	0	0	1	0	1	0	0	1	0051
42	0	0	0	0	1	0	1	0	1	0	0052
43	0	0	0	0	1	0	1	0	1	1	0053
44	0	0	0	0	1	0	1	1	0	0	0054
45	0	0	0	0	1	0	1	1	0	1	0055
46	0	0	0	0	1	0	1	1	1	0	0056
47	0	0	0	0	1	0	1	1	1	1	0057
48	0	0	0	0	1	1	0	0	0	0	0060
49	0	0	0	0	1	1	0	0	0	1	0061
50	0	0	0	0	1	1	0	0	1	0	0062
51	0	0	0	0	1	1	0	0	1	1	0063
52	0	0	0	0	1	1	0	1	0	0	0064
53	0	0	0	0	1	1	0	1	0	1	0065
54	0	0	0	0	1	1	0	1	1	0	0066
55	0	0	0	0	1	1	0	1	1	1	0067
56	0	0	0	0	1	1	1	0	0	0	0070
57	0	0	0	0	1	1	1	0	0	1	0071
58	0	0	0	0	1	1	1	0	1	0	0072
59	0	0	0	0	1	1	1	0	1	1	0073
60	0	0	0	0	1	1	1	1	0	0	0074
61	0	0	0	0	1	1	1	1	0	1	0075
62	0	0	0	0	1	1	1	1	1	0	0076
63	0	0	0	0	1	1	1	1	1	1	0077

DEC.	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	OCTAL
64	0	0	0	1	0	0	0	0	0	0	0 1 0 0
65	0	0	0	1	0	0	0	0	0	1	0 1 0 1
66	0	0	0	1	0	0	0	0	1	0	0 1 0 2
67	0	0	0	1	0	0	0	0	1	1	0 1 0 3
68	0	0	0	1	0	0	0	1	0	0	0 1 0 4
69	0	0	0	1	0	0	0	1	0	1	0 1 0 5
70	0	0	0	1	0	0	0	1	1	0	0 1 0 6
71	0	0	0	1	0	0	0	1	1	1	0 1 0 7
72	0	0	0	1	0	0	1	0	0	0	0 1 1 0
73	0	0	0	1	0	0	1	0	0	1	0 1 1 1
74	0	0	0	1	0	0	1	0	1	0	0 1 1 2
75	0	0	0	1	0	0	1	0	1	1	0 1 1 3
76	0	0	0	1	0	0	1	1	0	0	0 1 1 4
77	0	0	0	1	0	0	1	1	0	1	0 1 1 5
78	0	0	0	1	0	0	1	1	1	0	0 1 1 6
79	0	0	0	1	0	0	1	1	1	1	0 1 1 7
80	0	0	0	1	0	1	0	0	0	0	0 1 2 0
81	0	0	0	1	0	1	0	0	0	1	0 1 2 1
82	0	0	0	1	0	1	0	0	1	0	0 1 2 2
83	0	0	0	1	0	1	0	0	1	1	0 1 2 3
84	0	0	0	1	0	1	0	1	0	0	0 1 2 4
85	0	0	0	1	0	1	0	1	0	1	0 1 2 5
86	0	0	0	1	0	1	0	1	1	0	0 1 2 6
87	0	0	0	1	0	1	0	1	1	1	0 1 2 7
88	0	0	0	1	0	1	1	0	0	0	0 1 3 0
89	0	0	0	1	0	1	1	0	0	1	0 1 3 1
90	0	0	0	1	0	1	1	0	1	0	0 1 3 2
91	0	0	0	1	0	1	1	0	1	1	0 1 3 3
92	0	0	0	1	0	1	1	1	0	0	0 1 3 4
93	0	0	0	1	0	1	1	1	0	1	0 1 3 5
94	0	0	0	1	0	1	1	1	1	0	0 1 3 6
95	0	0	0	1	0	1	1	1	1	1	0 1 3 7
96	0	0	0	1	1	0	0	0	0	0	0 1 4 0
97	0	0	0	1	1	0	0	0	0	1	0 1 4 1
98	0	0	0	1	1	0	0	0	1	0	0 1 4 2
99	0	0	0	1	1	0	0	0	1	1	0 1 4 3
100	0	0	0	1	1	0	0	1	0	0	0 1 4 4
101	0	0	0	1	1	0	0	1	0	1	0 1 4 5
102	0	0	0	1	1	0	0	1	1	0	0 1 4 6
103	0	0	0	1	1	0	0	1	1	1	0 1 4 7
104	0	0	0	1	1	0	1	0	0	0	0 1 5 0
105	0	0	0	1	1	0	1	0	0	1	0 1 5 1
106	0	0	0	1	1	0	1	0	1	0	0 1 5 2
107	0	0	0	1	1	0	1	0	1	1	0 1 5 3
108	0	0	0	1	1	0	1	1	0	0	0 1 5 4
109	0	0	0	1	1	0	1	1	0	1	0 1 5 5
110	0	0	0	1	1	0	1	1	1	0	0 1 5 6
111	0	0	0	1	1	0	1	1	1	1	0 1 5 7
112	0	0	0	1	1	1	0	0	0	0	0 1 6 0
113	0	0	0	1	1	1	0	0	0	1	0 1 6 1
114	0	0	0	1	1	1	0	0	1	0	0 1 6 2
115	0	0	0	1	1	1	0	0	1	1	0 1 6 3
116	0	0	0	1	1	1	0	1	0	0	0 1 6 4
117	0	0	0	1	1	1	0	1	0	1	0 1 6 5
118	0	0	0	1	1	1	0	1	1	0	0 1 6 6
119	0	0	0	1	1	1	0	1	1	1	0 1 6 7
120	0	0	0	1	1	1	1	0	0	0	0 1 7 0
121	0	0	0	1	1	1	1	0	0	1	0 1 7 1
122	0	0	0	1	1	1	1	0	1	0	0 1 7 2
123	0	0	0	1	1	1	1	0	1	1	0 1 7 3
124	0	0	0	1	1	1	1	1	0	0	0 1 7 4
125	0	0	0	1	1	1	1	1	0	1	0 1 7 5
126	0	0	0	1	1	1	1	1	1	0	0 1 7 6
127	0	0	0	1	1	1	1	1	1	1	0 1 7 7

DEC.	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	OCTAL
128	0	0	1	0	0	0	0	0	0	0	0 2 0 0
129	0	0	1	0	0	0	0	0	0	1	0 2 0 1
130	0	0	1	0	0	0	0	0	1	0	0 2 0 2
131	0	0	1	0	0	0	0	0	1	1	0 2 0 3
132	0	0	1	0	0	0	0	1	0	0	0 2 0 4
133	0	0	1	0	0	0	0	1	0	1	0 2 0 5
134	0	0	1	0	0	0	0	1	1	0	0 2 0 6
135	0	0	1	0	0	0	0	1	1	1	0 2 0 7
136	0	0	1	0	0	0	1	0	0	0	0 2 1 0
137	0	0	1	0	0	0	1	0	0	1	0 2 1 1
138	0	0	1	0	0	0	1	0	1	0	0 2 1 2
139	0	0	1	0	0	0	1	0	1	1	0 2 1 3
140	0	0	1	0	0	0	1	1	0	0	0 2 1 4
141	0	0	1	0	0	0	1	1	0	1	0 2 1 5
142	0	0	1	0	0	0	1	1	1	0	0 2 1 6
143	0	0	1	0	0	0	1	1	1	1	0 2 1 7
144	0	0	1	0	0	1	0	0	0	0	0 2 2 0
145	0	0	1	0	0	1	0	0	0	1	0 2 2 1
146	0	0	1	0	0	1	0	0	1	0	0 2 2 2
147	0	0	1	0	0	1	0	0	1	1	0 2 2 3
148	0	0	1	0	0	1	0	1	0	0	0 2 2 4
149	0	0	1	0	0	1	0	1	0	1	0 2 2 5
150	0	0	1	0	0	1	0	1	1	0	0 2 2 6
151	0	0	1	0	0	1	0	1	1	1	0 2 2 7
152	0	0	1	0	0	1	1	0	0	0	0 2 3 0
153	0	0	1	0	0	1	1	0	0	1	0 2 3 1
154	0	0	1	0	0	1	1	0	1	0	0 2 3 2
155	0	0	1	0	0	1	1	0	1	1	0 2 3 3
156	0	0	1	0	0	1	1	1	0	0	0 2 3 4
157	0	0	1	0	0	1	1	1	0	1	0 2 3 5
158	0	0	1	0	0	1	1	1	1	0	0 2 3 6
159	0	0	1	0	0	1	1	1	1	1	0 2 3 7
160	0	0	1	0	1	0	0	0	0	0	0 2 4 0
161	0	0	1	0	1	0	0	0	0	1	0 2 4 1
162	0	0	1	0	1	0	0	0	1	0	0 2 4 2
163	0	0	1	0	1	0	0	0	1	1	0 2 4 3
164	0	0	1	0	1	0	0	1	0	0	0 2 4 4
165	0	0	1	0	1	0	0	1	0	1	0 2 4 5
166	0	0	1	0	1	0	0	1	1	0	0 2 4 6
167	0	0	1	0	1	0	0	1	1	1	0 2 4 7
168	0	0	1	0	1	0	1	0	0	0	0 2 5 0
169	0	0	1	0	1	0	1	0	0	1	0 2 5 1
170	0	0	1	0	1	0	1	0	1	0	0 2 5 2
171	0	0	1	0	1	0	1	0	1	1	0 2 5 3
172	0	0	1	0	1	0	1	1	0	0	0 2 5 4
173	0	0	1	0	1	0	1	1	0	1	0 2 5 5
174	0	0	1	0	1	0	1	1	1	0	0 2 5 6
175	0	0	1	0	1	0	1	1	1	1	0 2 5 7
176	0	0	1	0	1	1	0	0	0	0	0 2 6 0
177	0	0	1	0	1	1	0	0	0	1	0 2 6 1
178	0	0	1	0	1	1	0	0	1	0	0 2 6 2
179	0	0	1	0	1	1	0	0	1	1	0 2 6 3
180	0	0	1	0	1	1	0	1	0	0	0 2 6 4
181	0	0	1	0	1	1	0	1	0	1	0 2 6 5
182	0	0	1	0	1	1	0	1	1	0	0 2 6 6
183	0	0	1	0	1	1	0	1	1	1	0 2 6 7
184	0	0	1	0	1	1	1	0	0	0	0 2 7 0
185	0	0	1	0	1	1	1	0	0	1	0 2 7 1
186	0	0	1	0	1	1	1	0	1	0	0 2 7 2
187	0	0	1	0	1	1	1	0	1	1	0 2 7 3
188	0	0	1	0	1	1	1	1	0	0	0 2 7 4
189	0	0	1	0	1	1	1	1	0	1	0 2 7 5
190	0	0	1	0	1	1	1	1	1	0	0 2 7 6
191	0	0	1	0	1	1	1	1	1	1	0 2 7 7

DEC.	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	OCTAL
192	0	0	1	1	0	0	0	0	0	0	0 3 0 0
193	0	0	1	1	0	0	0	0	0	1	0 3 0 1
194	0	0	1	1	0	0	0	0	1	0	0 3 0 2
195	0	0	1	1	0	0	0	0	1	1	0 3 0 3
196	0	0	1	1	0	0	0	1	0	0	0 3 0 4
197	0	0	1	1	0	0	0	1	0	1	0 3 0 5
198	0	0	1	1	0	0	0	1	1	0	0 3 0 6
199	0	0	1	1	0	0	0	1	1	1	0 3 0 7
200	0	0	1	1	0	0	1	0	0	0	0 3 1 0
201	0	0	1	1	0	0	1	0	0	1	0 3 1 1
202	0	0	1	1	0	0	1	0	1	0	0 3 1 2
203	0	0	1	1	0	0	1	0	1	1	0 3 1 3
204	0	0	1	1	0	0	1	1	0	0	0 3 1 4
205	0	0	1	1	0	0	1	1	0	1	0 3 1 5
206	0	0	1	1	0	0	1	1	1	0	0 3 1 6
207	0	0	1	1	0	0	1	1	1	1	0 3 1 7
208	0	0	1	1	0	1	0	0	0	0	0 3 2 0
209	0	0	1	1	0	1	0	0	0	1	0 3 2 1
210	0	0	1	1	0	1	0	0	1	0	0 3 2 2
211	0	0	1	1	0	1	0	0	1	1	0 3 2 3
212	0	0	1	1	0	1	0	1	0	0	0 3 2 4
213	0	0	1	1	0	1	0	1	0	1	0 3 2 5
214	0	0	1	1	0	1	0	1	1	0	0 3 2 6
215	0	0	1	1	0	1	0	1	1	1	0 3 2 7
216	0	0	1	1	0	1	1	0	0	0	0 3 3 0
217	0	0	1	1	0	1	1	0	0	1	0 3 3 1
218	0	0	1	1	0	1	1	0	1	0	0 3 3 2
219	0	0	1	1	0	1	1	0	1	1	0 3 3 3
220	0	0	1	1	0	1	1	1	0	0	0 3 3 4
221	0	0	1	1	0	1	1	1	0	1	0 3 3 5
222	0	0	1	1	0	1	1	1	1	0	0 3 3 6
223	0	0	1	1	0	1	1	1	1	1	0 3 3 7
224	0	0	1	1	1	0	0	0	0	0	0 3 4 0
225	0	0	1	1	1	0	0	0	0	1	0 3 4 1
226	0	0	1	1	1	0	0	0	1	0	0 3 4 2
227	0	0	1	1	1	0	0	0	1	1	0 3 4 3
228	0	0	1	1	1	0	0	1	0	0	0 3 4 4
229	0	0	1	1	1	0	0	1	0	1	0 3 4 5
230	0	0	1	1	1	0	0	1	1	0	0 3 4 6
231	0	0	1	1	1	0	0	1	1	1	0 3 4 7
232	0	0	1	1	1	0	1	0	0	0	0 3 5 0
233	0	0	1	1	1	0	1	0	0	1	0 3 5 1
234	0	0	1	1	1	0	1	0	1	0	0 3 5 2
235	0	0	1	1	1	0	1	0	1	1	0 3 5 3
236	0	0	1	1	1	0	1	1	0	0	0 3 5 4
237	0	0	1	1	1	0	1	1	0	1	0 3 5 5
238	0	0	1	1	1	0	1	1	1	0	0 3 5 6
239	0	0	1	1	1	0	1	1	1	1	0 3 5 7
240	0	0	1	1	1	1	0	0	0	0	0 3 6 0
241	0	0	1	1	1	1	0	0	0	1	0 3 6 1
242	0	0	1	1	1	1	0	0	1	0	0 3 6 2
243	0	0	1	1	1	1	0	0	1	1	0 3 6 3
244	0	0	1	1	1	1	0	1	0	0	0 3 6 4
245	0	0	1	1	1	1	0	1	0	1	0 3 6 5
246	0	0	1	1	1	1	0	1	1	0	0 3 6 6
247	0	0	1	1	1	1	0	1	1	1	0 3 6 7
248	0	0	1	1	1	1	1	0	0	0	0 3 7 0
249	0	0	1	1	1	1	1	0	0	1	0 3 7 1
250	0	0	1	1	1	1	1	0	1	0	0 3 7 2
251	0	0	1	1	1	1	1	0	1	1	0 3 7 3
252	0	0	1	1	1	1	1	1	0	0	0 3 7 4
253	0	0	1	1	1	1	1	1	0	1	0 3 7 5
254	0	0	1	1	1	1	1	1	1	0	0 3 7 6
255	0	0	1	1	1	1	1	1	1	1	0 3 7 7

DEC.	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	OCTAL
256	0	1	0	0	0	0	0	0	0	0	0 4 0 0
257	0	1	0	0	0	0	0	0	0	1	0 4 0 1
258	0	1	0	0	0	0	0	0	1	0	0 4 0 2
259	0	1	0	0	0	0	0	0	1	1	0 4 0 3
260	0	1	0	0	0	0	0	1	0	0	0 4 0 4
261	0	1	0	0	0	0	0	1	0	1	0 4 0 5
262	0	1	0	0	0	0	0	1	1	0	0 4 0 6
263	0	1	0	0	0	0	0	1	1	1	0 4 0 7
264	0	1	0	0	0	0	1	0	0	0	0 4 1 0
265	0	1	0	0	0	0	1	0	0	1	0 4 1 1
266	0	1	0	0	0	0	1	0	1	0	0 4 1 2
267	0	1	0	0	0	0	1	0	1	1	0 4 1 3
268	0	1	0	0	0	0	1	1	0	0	0 4 1 4
269	0	1	0	0	0	0	1	1	0	1	0 3 1 5
270	0	1	0	0	0	0	1	1	1	0	0 4 1 6
271	0	1	0	0	0	0	1	1	1	1	0 4 1 7
272	0	1	0	0	0	1	0	0	0	0	0 4 2 0
273	0	1	0	0	0	1	0	0	0	1	0 4 2 1
274	0	1	0	0	0	1	0	0	1	0	0 4 2 2
275	0	1	0	0	0	1	0	0	1	1	0 4 2 3
276	0	1	0	0	0	1	0	1	0	0	0 4 2 4
277	0	1	0	0	0	1	0	1	0	1	0 4 2 5
278	0	1	0	0	0	1	0	1	1	0	0 4 2 6
279	0	1	0	0	0	1	0	1	1	1	0 4 2 7
280	0	1	0	0	0	1	1	0	0	0	0 4 3 0
281	0	1	0	0	0	1	1	0	0	1	0 4 3 1
282	0	1	0	0	0	1	1	0	1	0	0 4 3 2
283	0	1	0	0	0	1	1	0	1	1	0 4 3 3
284	0	1	0	0	0	1	1	1	0	0	0 4 3 4
285	0	1	0	0	0	1	1	1	0	1	0 4 3 5
286	0	1	0	0	0	1	1	1	1	0	0 4 3 6
287	0	1	0	0	0	1	1	1	1	1	0 4 3 7
288	0	1	0	0	1	0	0	0	0	0	0 4 4 0
289	0	1	0	0	1	0	0	0	0	1	0 4 4 1
290	0	1	0	0	1	0	0	0	1	0	0 4 4 2
291	0	1	0	0	1	0	0	0	1	1	0 4 4 3
292	0	1	0	0	1	0	0	1	0	0	0 4 4 4
293	0	1	0	0	1	0	0	1	0	1	0 4 4 5
294	0	1	0	0	1	0	0	1	1	0	0 4 4 6
295	0	1	0	0	1	0	0	1	1	1	0 4 4 7
296	0	1	0	0	1	0	1	0	0	0	0 4 5 0
297	0	1	0	0	1	0	1	0	0	1	0 4 5 1
298	0	1	0	0	1	0	1	0	1	0	0 4 5 2
299	0	1	0	0	1	0	1	0	1	1	0 4 5 3
300	0	1	0	0	1	0	1	1	0	0	0 4 5 4
301	0	1	0	0	1	0	1	1	0	1	0 4 5 5
302	0	1	0	0	1	0	1	1	1	0	0 4 5 6
303	0	1	0	0	1	0	1	1	1	1	0 4 5 7
304	0	1	0	0	1	1	0	0	0	0	0 4 6 0
305	0	1	0	0	1	1	0	0	0	1	0 4 6 1
306	0	1	0	0	1	1	0	0	1	0	0 4 6 2
307	0	1	0	0	1	1	0	0	1	1	0 4 6 3
308	0	1	0	0	1	1	0	1	0	0	0 4 6 4
309	0	1	0	0	1	1	0	1	0	1	0 4 6 5
310	0	1	0	0	1	1	0	1	1	0	0 4 6 6
311	0	1	0	0	1	1	0	1	1	1	0 4 6 7
312	0	1	0	0	1	1	1	0	0	0	0 4 7 0
313	0	1	0	0	1	1	1	0	0	1	0 4 7 1
314	0	1	0	0	1	1	1	0	1	0	0 4 7 2
315	0	1	0	0	1	1	1	0	1	1	0 4 7 3
316	0	1	0	0	1	1	1	1	0	0	0 4 7 4
317	0	1	0	0	1	1	1	1	0	1	0 4 7 5
318	0	1	0	0	1	1	1	1	1	0	0 4 7 6
319	0	1	0	0	1	1	1	1	1	1	0 4 7 7

DEC.	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	OCTAL
320	0	1	0	1	0	0	0	0	0	0	0500
321	0	1	0	1	0	0	0	0	0	1	0501
322	0	1	0	1	0	0	0	0	1	0	0502
323	0	1	0	1	0	0	0	0	1	1	0503
324	0	1	0	1	0	0	0	1	0	0	0504
325	0	1	0	1	0	0	0	1	0	1	0505
326	0	1	0	1	0	0	0	1	1	0	0506
327	0	1	0	1	0	0	0	1	1	1	0507
328	0	1	0	1	0	0	1	0	0	0	0510
329	0	1	0	1	0	0	1	0	0	1	0511
330	0	1	0	1	0	0	1	0	1	0	0512
331	0	1	0	1	0	0	1	0	1	1	0513
332	0	1	0	1	0	0	1	1	0	0	0514
333	0	1	0	1	0	0	1	1	0	1	0515
334	0	1	0	1	0	0	1	1	1	0	0516
335	0	1	0	1	0	0	1	1	1	1	0517
336	0	1	0	1	0	1	0	0	0	0	0520
337	0	1	0	1	0	1	0	0	0	1	0521
338	0	1	0	1	0	1	0	0	1	0	0522
339	0	1	0	1	0	1	0	0	1	1	0523
340	0	1	0	1	0	1	0	1	0	0	0524
341	0	1	0	1	0	1	0	1	0	1	0525
342	0	1	0	1	0	1	0	1	1	0	0526
343	0	1	0	1	0	1	0	1	1	1	0527
344	0	1	0	1	0	1	1	0	0	0	0530
345	0	1	0	1	0	1	1	0	0	1	0531
346	0	1	0	1	0	1	1	0	1	0	0532
347	0	1	0	1	0	1	1	0	1	1	0533
348	0	1	0	1	0	1	1	1	0	0	0534
349	0	1	0	1	0	1	1	1	0	1	0535
350	0	1	0	1	0	1	1	1	1	0	0536
351	0	1	0	1	0	1	1	1	1	1	0537
352	0	1	0	1	1	0	0	0	0	0	0540
353	0	1	0	1	1	0	0	0	0	1	0541
354	0	1	0	1	1	0	0	0	1	0	0542
355	0	1	0	1	1	0	0	0	1	1	0543
356	0	1	0	1	1	0	0	1	0	0	0544
357	0	1	0	1	1	0	0	1	0	1	0545
358	0	1	0	1	1	0	0	1	1	0	0546
359	0	1	0	1	1	0	0	1	1	1	0547
360	0	1	0	1	1	0	1	0	0	0	0550
361	0	1	0	1	1	0	1	0	0	1	0551
362	0	1	0	1	1	0	1	0	1	0	0552
363	0	1	0	1	1	0	1	0	1	1	0553
364	0	1	0	1	1	0	1	1	0	0	0554
365	0	1	0	1	1	0	1	1	0	1	0555
366	0	1	0	1	1	0	1	1	1	0	0556
367	0	1	0	1	1	0	1	1	1	1	0557
368	0	1	0	1	1	1	0	0	0	0	0560
369	0	1	0	1	1	1	0	0	0	1	0561
370	0	1	0	1	1	1	0	0	1	0	0562
371	0	1	0	1	1	1	0	0	1	1	0563
372	0	1	0	1	1	1	0	1	0	0	0564
373	0	1	0	1	1	1	0	1	0	1	0565
374	0	1	0	1	1	1	0	1	1	0	0566
375	0	1	0	1	1	1	0	1	1	1	0567
376	0	1	0	1	1	1	1	0	0	0	0570
377	0	1	0	1	1	1	1	0	0	1	0571
378	0	1	0	1	1	1	1	0	1	0	0572
379	0	1	0	1	1	1	1	0	1	1	0573
380	0	1	0	1	1	1	1	1	0	0	0574
381	0	1	0	1	1	1	1	1	0	1	0575
382	0	1	0	1	1	1	1	1	1	0	0576
383	0	1	0	1	1	1	1	1	1	1	0577

DEC.	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	OCTAL
384	0	1	1	0	0	0	0	0	0	0	0600
385	0	1	1	0	0	0	0	0	0	1	0601
386	0	1	1	0	0	0	0	0	1	0	0602
387	0	1	1	0	0	0	0	0	1	1	0603
388	0	1	1	0	0	0	0	1	0	0	0604
389	0	1	1	0	0	0	0	1	0	1	0605
390	0	1	1	0	0	0	0	1	1	0	0606
391	0	1	1	0	0	0	0	1	1	1	0607
392	0	1	1	0	0	0	1	0	0	0	0610
393	0	1	1	0	0	0	1	0	0	1	0611
394	0	1	1	0	0	0	1	0	1	0	0612
395	0	1	1	0	0	0	1	0	1	1	0613
396	0	1	1	0	0	0	1	1	0	0	0614
397	0	1	1	0	0	0	1	1	0	1	0615
398	0	1	1	0	0	0	1	1	1	0	0616
399	0	1	1	0	0	0	1	1	1	1	0617
400	0	1	1	0	0	1	0	0	0	0	0620
401	0	1	1	0	0	1	0	0	0	1	0621
402	0	1	1	0	0	1	0	0	1	0	0622
403	0	1	1	0	0	1	0	0	1	1	0623
404	0	1	1	0	0	1	0	1	0	0	0624
405	0	1	1	0	0	1	0	1	0	1	0625
406	0	1	1	0	0	1	0	1	1	0	0626
407	0	1	1	0	0	1	0	1	1	1	0627
408	0	1	1	0	0	1	1	0	0	0	0630
409	0	1	1	0	0	1	1	0	0	1	0631
410	0	1	1	0	0	1	1	0	1	0	0632
411	0	1	1	0	0	1	1	0	1	1	0633
412	0	1	1	0	0	1	1	1	0	0	0634
413	0	1	1	0	0	1	1	1	0	1	0635
414	0	1	1	0	0	1	1	1	1	0	0636
415	0	1	1	0	0	1	1	1	1	1	0637
416	0	1	1	0	1	0	0	0	0	0	0640
417	0	1	1	0	1	0	0	0	0	1	0641
418	0	1	1	0	1	0	0	0	1	0	0642
419	0	1	1	0	1	0	0	0	1	1	0643
420	0	1	1	0	1	0	0	1	0	0	0644
421	0	1	1	0	1	0	0	1	0	1	0645
422	0	1	1	0	1	0	0	1	1	0	0646
423	0	1	1	0	1	0	0	1	1	1	0647
424	0	1	1	0	1	0	1	0	0	0	0650
425	0	1	1	0	1	0	1	0	0	1	0651
426	0	1	1	0	1	0	1	0	1	0	0652
427	0	1	1	0	1	0	1	0	1	1	0653
428	0	1	1	0	1	0	1	1	0	0	0654
429	0	1	1	0	1	0	1	1	0	1	0655
430	0	1	1	0	1	0	1	1	1	0	0656
431	0	1	1	0	1	0	1	1	1	1	0657
432	0	1	1	0	1	1	0	0	0	0	0660
433	0	1	1	0	1	1	0	0	0	1	0661
434	0	1	1	0	1	1	0	0	1	0	0662
435	0	1	1	0	1	1	0	0	1	1	0663
436	0	1	1	0	1	1	0	1	0	0	0664
437	0	1	1	0	1	1	0	1	0	1	0665
438	0	1	1	0	1	1	0	1	1	0	0666
439	0	1	1	0	1	1	0	1	1	1	0667
440	0	1	1	0	1	1	1	0	0	0	0670
441	0	1	1	0	1	1	1	0	0	1	0671
442	0	1	1	0	1	1	1	0	1	0	0672
443	0	1	1	0	1	1	1	0	1	1	0673
444	0	1	1	0	1	1	1	1	0	0	0674
445	0	1	1	0	1	1	1	1	0	1	0675
446	0	1	1	0	1	1	1	1	1	0	0676
447	0	1	1	0	1	1	1	1	1	1	0677

DEC.	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	OCTAL
448	0	1	1	1	0	0	0	0	0	0	0700
449	0	1	1	1	0	0	0	0	0	1	0701
450	0	1	1	1	0	0	0	0	1	0	0702
451	0	1	1	1	0	0	0	0	1	1	0703
452	0	1	1	1	0	0	0	1	0	0	0704
453	0	1	1	1	0	0	0	1	0	1	0705
454	0	1	1	1	0	0	0	1	1	0	0706
455	0	1	1	1	0	0	0	1	1	1	0707
456	0	1	1	1	0	0	1	0	0	0	0710
457	0	1	1	1	0	0	1	0	0	1	0711
458	0	1	1	1	0	0	1	0	1	0	0712
459	0	1	1	1	0	0	1	0	1	1	0713
460	0	1	1	1	0	0	1	1	0	0	0714
461	0	1	1	1	0	0	1	1	0	1	0715
462	0	1	1	1	0	0	1	1	1	0	0716
463	0	1	1	1	0	0	1	1	1	1	0717
464	0	1	1	1	0	1	0	0	0	0	0720
465	0	1	1	1	0	1	0	0	0	1	0721
466	0	1	1	1	0	1	0	0	1	0	0722
467	0	1	1	1	0	1	0	0	1	1	0723
468	0	1	1	1	0	1	0	1	0	0	0724
469	0	1	1	1	0	1	0	1	0	1	0725
470	0	1	1	1	0	1	0	1	1	0	0726
471	0	1	1	1	0	1	0	1	1	1	0727
472	0	1	1	1	0	1	1	0	0	0	0730
473	0	1	1	1	0	1	1	0	0	1	0731
474	0	1	1	1	0	1	1	0	1	0	0732
475	0	1	1	1	0	1	1	0	1	1	0733
476	0	1	1	1	0	1	1	1	0	0	0734
477	0	1	1	1	0	1	1	1	0	1	0735
478	0	1	1	1	0	1	1	1	1	0	0736
479	0	1	1	1	0	1	1	1	1	1	0737
480	0	1	1	1	1	0	0	0	0	0	0740
481	0	1	1	1	1	0	0	0	0	1	0741
482	0	1	1	1	1	0	0	0	1	0	0742
483	0	1	1	1	1	0	0	0	1	1	0743
484	0	1	1	1	1	0	0	1	0	0	0744
485	0	1	1	1	1	0	0	1	0	1	0745
486	0	1	1	1	1	0	0	1	1	0	0746
487	0	1	1	1	1	0	0	1	1	1	0747
488	0	1	1	1	1	0	1	0	0	0	0750
489	0	1	1	1	1	0	1	0	0	1	0751
490	0	1	1	1	1	0	1	0	1	0	0752
491	0	1	1	1	1	0	1	0	1	1	0753
492	0	1	1	1	1	0	1	1	0	0	0754
493	0	1	1	1	1	0	1	1	0	1	0755
494	0	1	1	1	1	0	1	1	1	0	0756
495	0	1	1	1	1	0	1	1	1	1	0757
496	0	1	1	1	1	1	0	0	0	0	0760
497	0	1	1	1	1	1	0	0	0	1	0761
498	0	1	1	1	1	1	0	0	1	0	0762
499	0	1	1	1	1	1	0	0	1	1	0763
500	0	1	1	1	1	1	0	1	0	0	0764
501	0	1	1	1	1	1	0	1	0	1	0765
502	0	1	1	1	1	1	0	1	1	0	0766
503	0	1	1	1	1	1	0	1	1	1	0767
504	0	1	1	1	1	1	1	0	0	0	0770
505	0	1	1	1	1	1	1	0	0	1	0771
506	0	1	1	1	1	1	1	0	1	0	0772
507	0	1	1	1	1	1	1	0	1	1	0773
508	0	1	1	1	1	1	1	1	0	0	0774
509	0	1	1	1	1	1	1	1	0	1	0775
510	0	1	1	1	1	1	1	1	1	0	0776
511	0	1	1	1	1	1	1	1	1	1	0777

DEC.	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	OCTAL
512	1	0	0	0	0	0	0	0	0	0	1000
513	1	0	0	0	0	0	0	0	0	1	1001
514	1	0	0	0	0	0	0	0	1	0	1002
515	1	0	0	0	0	0	0	0	1	1	1003
516	1	0	0	0	0	0	0	1	0	0	1004
517	1	0	0	0	0	0	0	1	0	1	1005
518	1	0	0	0	0	0	0	1	1	0	1006
519	1	0	0	0	0	0	0	1	1	1	1007
520	1	0	0	0	0	0	1	0	0	0	1010
521	1	0	0	0	0	0	1	0	0	1	1011
522	1	0	0	0	0	0	1	0	1	0	1012
523	1	0	0	0	0	0	1	0	1	1	1013
524	1	0	0	0	0	0	1	1	0	0	1014
525	1	0	0	0	0	0	1	1	0	1	1015
526	1	0	0	0	0	0	1	1	1	0	1016
527	1	0	0	0	0	0	1	1	1	1	1017
528	1	0	0	0	0	1	0	0	0	0	1020
529	1	0	0	0	0	1	0	0	0	1	1021
530	1	0	0	0	0	1	0	0	1	0	1022
531	1	0	0	0	0	1	0	0	1	1	1023
532	1	0	0	0	0	1	0	1	0	0	1024
533	1	0	0	0	0	1	0	1	0	1	1025
534	1	0	0	0	0	1	0	1	1	0	1026
535	1	0	0	0	0	1	0	1	1	1	1027
536	1	0	0	0	0	1	1	0	0	0	1030
537	1	0	0	0	0	1	1	0	0	1	1031
538	1	0	0	0	0	1	1	0	1	0	1032
539	1	0	0	0	0	1	1	0	1	1	1033
540	1	0	0	0	0	1	1	1	0	0	1034
541	1	0	0	0	0	1	1	1	0	1	1035
542	1	0	0	0	0	1	1	1	1	0	1036
543	1	0	0	0	0	1	1	1	1	1	1037
544	1	0	0	0	1	0	0	0	0	0	1040
545	1	0	0	0	1	0	0	0	0	1	1041
546	1	0	0	0	1	0	0	0	1	0	1042
547	1	0	0	0	1	0	0	0	1	1	1043
548	1	0	0	0	1	0	0	1	0	0	1044
549	1	0	0	0	1	0	0	1	0	1	1045
550	1	0	0	0	1	0	0	1	1	0	1046
551	1	0	0	0	1	0	0	1	1	1	1047
552	1	0	0	0	1	0	1	0	0	0	1050
553	1	0	0	0	1	0	1	0	0	1	1051
554	1	0	0	0	1	0	1	0	1	0	1052
555	1	0	0	0	1	0	1	0	1	1	1053
556	1	0	0	0	1	0	1	1	0	0	1054
557	1	0	0	0	1	0	1	1	0	1	1055
558	1	0	0	0	1	0	1	1	1	0	1056
559	1	0	0	0	1	0	1	1	1	1	1057
560	1	0	0	0	1	1	0	0	0	0	1060
561	1	0	0	0	1	1	0	0	0	1	1061
562	1	0	0	0	1	1	0	0	1	0	1062
563	1	0	0	0	1	1	0	0	1	1	1063
564	1	0	0	0	1	1	0	1	0	0	1064
565	1	0	0	0	1	1	0	1	0	1	1065
566	1	0	0	0	1	1	0	1	1	0	1066
567	1	0	0	0	1	1	0	1	1	1	1067
568	1	0	0	0	1	1	1	0	0	0	1070
569	1	0	0	0	1	1	1	0	0	1	1071
570	1	0	0	0	1	1	1	0	1	0	1072
571	1	0	0	0	1	1	1	0	1	1	1073
572	1	0	0	0	1	1	1	1	0	0	1074
573	1	0	0	0	1	1	1	1	0	1	1075
574	1	0	0	0	1	1	1	1	1	0	1076
575	1	0	0	0	1	1	1	1	1	1	1077

DEC.	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	OCTAL
576	1	0	0	1	0	0	0	0	0	0	1 1 0 0
577	1	0	0	1	0	0	0	0	0	1	1 1 0 1
578	1	0	0	1	0	0	0	0	1	0	1 1 0 2
579	1	0	0	1	0	0	0	0	1	1	1 1 0 3
580	1	0	0	1	0	0	0	1	0	0	1 1 0 4
581	1	0	0	1	0	0	0	1	0	1	1 1 0 5
582	1	0	0	1	0	0	0	1	1	0	1 1 0 6
583	1	0	0	1	0	0	0	1	1	1	1 1 0 7
584	1	0	0	1	0	0	1	0	0	0	1 1 1 0
585	1	0	0	1	0	0	1	0	0	1	1 1 1 1
586	1	0	0	1	0	0	1	0	1	0	1 1 1 2
587	1	0	0	1	0	0	1	0	1	1	1 1 1 3
588	1	0	0	1	0	0	1	1	0	0	1 1 1 4
589	1	0	0	1	0	0	1	1	0	1	1 1 1 5
590	1	0	0	1	0	0	1	1	1	0	1 1 1 6
591	1	0	0	1	0	0	1	1	1	1	1 1 1 7
592	1	0	0	1	0	1	0	0	0	0	1 1 2 0
593	1	0	0	1	0	1	0	0	0	1	1 1 2 1
594	1	0	0	1	0	1	0	0	1	0	1 1 2 2
595	1	0	0	1	0	1	0	0	1	1	1 1 2 3
596	1	0	0	1	0	1	0	1	0	0	1 1 2 4
597	1	0	0	1	0	1	0	1	0	1	1 1 2 5
598	1	0	0	1	0	1	0	1	1	0	1 1 2 6
599	1	0	0	1	0	1	0	1	1	1	1 1 2 7
600	1	0	0	1	0	1	1	0	0	0	1 1 3 0
601	1	0	0	1	0	1	1	0	0	1	1 1 3 1
602	1	0	0	1	0	1	1	0	1	0	1 1 3 2
603	1	0	0	1	0	1	1	0	1	1	1 1 3 3
604	1	0	0	1	0	1	1	1	0	0	1 1 3 4
605	1	0	0	1	0	1	1	1	0	1	1 1 3 5
606	1	0	0	1	0	1	1	1	1	0	1 1 3 6
607	1	0	0	1	0	1	1	1	1	1	1 1 3 7
608	1	0	0	1	1	0	0	0	0	0	1 1 4 0
609	1	0	0	1	1	0	0	0	0	1	1 1 4 1
610	1	0	0	1	1	0	0	0	1	0	1 1 4 2
611	1	0	0	1	1	0	0	0	1	1	1 1 4 3
612	1	0	0	1	1	0	0	1	0	0	1 1 4 4
613	1	0	0	1	1	0	0	1	0	1	1 1 4 5
614	1	0	0	1	1	0	0	1	1	0	1 1 4 6
615	1	0	0	1	1	0	0	1	1	1	1 1 4 7
616	1	0	0	1	1	0	1	0	0	0	1 1 5 0
617	1	0	0	1	1	0	1	0	0	1	1 1 5 1
618	1	0	0	1	1	0	1	0	1	0	1 1 5 2
619	1	0	0	1	1	0	1	0	1	1	1 1 5 3
620	1	0	0	1	1	0	1	1	0	0	1 1 5 4
621	1	0	0	1	1	0	1	1	0	1	1 1 5 5
622	1	0	0	1	1	0	1	1	1	0	1 1 5 6
623	1	0	0	1	1	0	1	1	1	1	1 1 5 7
624	1	0	0	1	1	1	0	0	0	0	1 1 6 0
625	1	0	0	1	1	1	0	0	0	1	1 1 6 1
626	1	0	0	1	1	1	0	0	1	0	1 1 6 2
627	1	0	0	1	1	1	0	0	1	1	1 1 6 3
628	1	0	0	1	1	1	0	1	0	0	1 1 6 4
629	1	0	0	1	1	1	0	1	0	1	1 1 6 5
630	1	0	0	1	1	1	0	1	1	0	1 1 6 6
631	1	0	0	1	1	1	0	1	1	1	1 1 6 7
632	1	0	0	1	1	1	1	0	0	0	1 1 7 0
633	1	0	0	1	1	1	1	0	0	1	1 1 7 1
634	1	0	0	1	1	1	1	0	1	0	1 1 7 2
635	1	0	0	1	1	1	1	0	1	1	1 1 7 3
636	1	0	0	1	1	1	1	1	0	0	1 1 7 4
637	1	0	0	1	1	1	1	1	0	1	1 1 7 5
638	1	0	0	1	1	1	1	1	1	0	1 1 7 6
639	1	0	0	1	1	1	1	1	1	1	1 1 7 7

DEC.	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	OCTAL
640	1	0	1	0	0	0	0	0	0	0	1 2 0 0
641	1	0	1	0	0	0	0	0	0	1	1 2 0 1
642	1	0	1	0	0	0	0	0	1	0	1 2 0 2
643	1	0	1	0	0	0	0	0	1	1	1 2 0 3
644	1	0	1	0	0	0	0	1	0	0	1 2 0 4
645	1	0	1	0	0	0	0	1	0	1	1 2 0 5
646	1	0	1	0	0	0	0	1	1	0	1 2 0 6
647	1	0	1	0	0	0	0	1	1	1	1 2 0 7
648	1	0	1	0	0	0	1	0	0	0	1 2 1 0
649	1	0	1	0	0	0	1	0	0	1	1 2 1 1
650	1	0	1	0	0	0	1	0	1	0	1 2 1 2
651	1	0	1	0	0	0	1	0	1	1	1 2 1 3
652	1	0	1	0	0	0	1	1	0	0	1 2 1 4
653	1	0	1	0	0	0	1	1	0	1	1 2 1 5
654	1	0	1	0	0	0	1	1	1	0	1 2 1 6
655	1	0	1	0	0	0	1	1	1	1	1 2 1 7
656	1	0	1	0	0	1	0	0	0	0	1 2 2 0
657	1	0	1	0	0	1	0	0	0	1	1 2 2 1
658	1	0	1	0	0	1	0	0	1	0	1 2 2 2
659	1	0	1	0	0	1	0	0	1	1	1 2 2 3
660	1	0	1	0	0	1	0	1	0	0	1 2 2 4
661	1	0	1	0	0	1	0	1	0	1	1 2 2 5
662	1	0	1	0	0	1	0	1	1	0	1 2 2 6
663	1	0	1	0	0	1	0	1	1	1	1 2 2 7
664	1	0	1	0	0	1	1	0	0	0	1 2 3 0
665	1	0	1	0	0	1	1	0	0	1	1 2 3 1
666	1	0	1	0	0	1	1	0	1	0	1 2 3 2
667	1	0	1	0	0	1	1	0	1	1	1 2 3 3
668	1	0	1	0	0	1	1	1	0	0	1 2 3 4
669	1	0	1	0	0	1	1	1	0	1	1 2 3 5
670	1	0	1	0	0	1	1	1	1	0	1 2 3 6
671	1	0	1	0	0	1	1	1	1	1	1 2 3 7
672	1	0	1	0	1	0	0	0	0	0	1 2 4 0
673	1	0	1	0	1	0	0	0	0	1	1 2 4 1
674	1	0	1	0	1	0	0	0	1	0	1 2 4 2
675	1	0	1	0	1	0	0	0	1	1	1 2 4 3
676	1	0	1	0	1	0	0	1	0	0	1 2 4 4
677	1	0	1	0	1	0	0	1	0	1	1 2 4 5
678	1	0	1	0	1	0	0	1	1	0	1 2 4 6
679	1	0	1	0	1	0	0	1	1	1	1 2 4 7
680	1	0	1	0	1	0	1	0	0	0	1 2 5 0
681	1	0	1	0	1	0	1	0	0	1	1 2 5 1
682	1	0	1	0	1	0	1	0	1	0	1 2 5 2
683	1	0	1	0	1	0	1	0	1	1	1 2 5 3
684	1	0	1	0	1	0	1	1	0	0	1 2 5 4
685	1	0	1	0	1	0	1	1	0	1	1 2 5 5
686	1	0	1	0	1	0	1	1	1	0	1 2 5 6
687	1	0	1	0	1	0	1	1	1	1	1 2 5 7
688	1	0	1	0	1	1	0	0	0	0	1 2 6 0
689	1	0	1	0	1	1	0	0	0	1	1 2 6 1
690	1	0	1	0	1	1	0	0	1	0	1 2 6 2
691	1	0	1	0	1	1	0	0	1	1	1 2 6 3
692	1	0	1	0	1	1	0	1	0	0	1 2 6 4
693	1	0	1	0	1	1	0	1	0	1	1 2 6 5
694	1	0	1	0	1	1	0	1	1	0	1 2 6 6
695	1	0	1	0	1	1	0	1	1	1	1 2 6 7
696	1	0	1	0	1	1	1	0	0	0	1 2 7 0
697	1	0	1	0	1	1	1	0	0	1	1 2 7 1
698	1	0	1	0	1	1	1	0	1	0	1 2 7 2
699	1	0	1	0	1	1	1	0	1	1	1 2 7 3
700	1	0	1	0	1	1	1	1	0	0	1 2 7 4
701	1	0	1	0	1	1	1	1	0	1	1 2 7 5
702	1	0	1	0	1	1	1	1	1	0	1 2 7 6
703	1	0	1	0	1	1	1	1	1	1	1 2 7 7

DEC.	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	OCTAL
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705	1	0	1	1	0	0	0	0	0	1	1 3 0 1
706	1	0	1	1	0	0	0	0	1	0	1 3 0 2
707	1	0	1	1	0	0	0	0	1	1	1 3 0 3
708	1	0	1	1	0	0	0	1	0	0	1 3 0 4
709	1	0	1	1	0	0	0	1	0	1	1 3 0 5
710	1	0	1	1	0	0	0	1	1	0	1 3 0 6
711	1	0	1	1	0	0	0	1	1	1	1 3 0 7
712	1	0	1	1	0	0	1	0	0	0	1 3 1 0
713	1	0	1	1	0	0	1	0	0	1	1 3 1 1
714	1	0	1	1	0	0	1	0	1	0	1 3 1 2
715	1	0	1	1	0	0	1	0	1	1	1 3 1 3
716	1	0	1	1	0	0	1	1	0	0	1 3 1 4
717	1	0	1	1	0	0	1	1	0	1	1 3 1 5
718	1	0	1	1	0	0	1	1	1	0	1 3 1 6
719	1	0	1	1	0	0	1	1	1	1	1 3 1 7
720	1	0	1	1	0	1	0	0	0	0	1 3 2 0
721	1	0	1	1	0	1	0	0	0	1	1 3 2 1
722	1	0	1	1	0	1	0	0	1	0	1 3 2 2
723	1	0	1	1	0	1	0	0	1	1	1 3 2 3
724	1	0	1	1	0	1	0	1	0	0	1 3 2 4
725	1	0	1	1	0	1	0	1	0	1	1 3 2 5
726	1	0	1	1	0	1	0	1	1	0	1 3 2 6
727	1	0	1	1	0	1	0	1	1	1	1 3 2 7
728	1	0	1	1	0	1	1	0	0	0	1 3 3 0
729	1	0	1	1	0	1	1	0	0	1	1 3 3 1
730	1	0	1	1	0	1	1	0	1	0	1 3 3 2
731	1	0	1	1	0	1	1	0	1	1	1 3 3 3
732	1	0	1	1	0	1	1	1	0	0	1 3 3 4
733	1	0	1	1	0	1	1	1	0	1	1 3 3 5
734	1	0	1	1	0	1	1	1	1	0	1 3 3 6
735	1	0	1	1	0	1	1	1	1	1	1 3 3 7
736	1	0	1	1	1	0	0	0	0	0	1 3 4 0
737	1	0	1	1	1	0	0	0	0	1	1 3 4 1
738	1	0	1	1	1	0	0	0	1	0	1 3 4 2
739	1	0	1	1	1	0	0	0	1	1	1 3 4 3
740	1	0	1	1	1	0	0	1	0	0	1 3 4 4
741	1	0	1	1	1	0	0	1	0	1	1 3 4 5
742	1	0	1	1	1	0	0	1	1	0	1 3 4 6
743	1	0	1	1	1	0	0	1	1	1	1 3 4 7
744	1	0	1	1	1	0	1	0	0	0	1 3 5 0
745	1	0	1	1	1	0	1	0	0	1	1 3 5 1
746	1	0	1	1	1	0	1	0	1	0	1 3 5 2
747	1	0	1	1	1	0	1	0	1	1	1 3 5 3
748	1	0	1	1	1	0	1	1	0	0	1 3 5 4
749	1	0	1	1	1	0	1	1	0	1	1 3 5 5
750	1	0	1	1	1	0	1	1	1	0	1 3 5 6
751	1	0	1	1	1	0	1	1	1	1	1 3 5 7
752	1	0	1	1	1	1	0	0	0	0	1 3 6 0
753	1	0	1	1	1	1	0	0	0	1	1 3 6 1
754	1	0	1	1	1	1	0	0	1	0	1 3 6 2
755	1	0	1	1	1	1	0	0	1	1	1 3 6 3
756	1	0	1	1	1	1	0	1	0	0	1 3 6 4
757	1	0	1	1	1	1	0	1	0	1	1 3 6 5
758	1	0	1	1	1	1	0	1	1	0	1 3 6 6
759	1	0	1	1	1	1	0	1	1	1	1 3 6 7
760	1	0	1	1	1	1	1	0	0	0	1 3 7 0
761	1	0	1	1	1	1	1	0	0	1	1 3 7 1
762	1	0	1	1	1	1	1	0	1	0	1 3 7 2
763	1	0	1	1	1	1	1	0	1	1	1 3 7 3
764	1	0	1	1	1	1	1	1	0	0	1 3 7 4
765	1	0	1	1	1	1	1	1	0	1	1 3 7 5
766	1	0	1	1	1	1	1	1	1	0	1 3 7 6
767	1	0	1	1	1	1	1	1	1	1	1 3 7 7

DEC.	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	OCTAL
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769	1	1	0	0	0	0	0	0	0	1	1 4 0 1
770	1	1	0	0	0	0	0	0	1	0	1 4 0 2
771	1	1	0	0	0	0	0	0	1	1	1 4 0 3
772	1	1	0	0	0	0	0	1	0	0	1 4 0 4
773	1	1	0	0	0	0	0	1	0	1	1 4 0 5
774	1	1	0	0	0	0	0	1	1	0	1 4 0 6
775	1	1	0	0	0	0	0	1	1	1	1 4 0 7
776	1	1	0	0	0	0	1	0	0	0	1 4 1 0
777	1	1	0	0	0	0	1	0	0	1	1 4 1 1
778	1	1	0	0	0	0	1	0	1	0	1 4 1 2
779	1	1	0	0	0	0	1	0	1	1	1 4 1 3
780	1	1	0	0	0	0	1	1	0	0	1 4 1 4
781	1	1	0	0	0	0	1	1	0	1	1 4 1 5
782	1	1	0	0	0	0	1	1	1	0	1 4 1 6
783	1	1	0	0	0	0	1	1	1	1	1 4 1 7
784	1	1	0	0	0	1	0	0	0	0	1 4 2 0
785	1	1	0	0	0	1	0	0	0	1	1 4 2 1
786	1	1	0	0	0	1	0	0	1	0	1 4 2 2
787	1	1	0	0	0	1	0	0	1	1	1 4 2 3
788	1	1	0	0	0	1	0	1	0	0	1 4 2 4
789	1	1	0	0	0	1	0	1	0	1	1 4 2 5
790	1	1	0	0	0	1	0	1	1	0	1 4 2 6
791	1	1	0	0	0	1	0	1	1	1	1 4 2 7
792	1	1	0	0	0	1	1	0	0	0	1 4 3 0
793	1	1	0	0	0	1	1	0	0	1	1 4 3 1
794	1	1	0	0	0	1	1	0	1	0	1 4 3 2
795	1	1	0	0	0	1	1	0	1	1	1 4 3 3
796	1	1	0	0	0	1	1	1	0	0	1 4 3 4
797	1	1	0	0	0	1	1	1	0	1	1 4 3 5
798	1	1	0	0	0	1	1	1	1	0	1 4 3 6
799	1	1	0	0	0	1	1	1	1	1	1 4 3 7
800	1	1	0	0	1	0	0	0	0	0	1 4 4 0
801	1	1	0	0	1	0	0	0	0	1	1 4 4 1
802	1	1	0	0	1	0	0	0	1	0	1 4 4 2
803	1	1	0	0	1	0	0	0	1	1	1 4 4 3
804	1	1	0	0	1	0	0	1	0	0	1 4 4 4
805	1	1	0	0	1	0	0	1	0	1	1 4 4 5
806	1	1	0	0	1	0	0	1	1	0	1 4 4 6
807	1	1	0	0	1	0	0	1	1	1	1 4 4 7
808	1	1	0	0	1	0	1	0	0	0	1 4 5 0
809	1	1	0	0	1	0	1	0	0	1	1 4 5 1
810	1	1	0	0	1	0	1	0	1	0	1 4 5 2
811	1	1	0	0	1	0	1	0	1	1	1 4 5 3
812	1	1	0	0	1	0	1	1	0	0	1 4 5 4
813	1	1	0	0	1	0	1	1	0	1	1 4 5 5
814	1	1	0	0	1	0	1	1	1	0	1 4 5 6
815	1	1	0	0	1	0	1	1	1	1	1 4 5 7
816	1	1	0	0	1	1	0	0	0	0	1 4 6 0
817	1	1	0	0	1	1	0	0	0	1	1 4 6 1
818	1	1	0	0	1	1	0	0	1	0	1 4 6 2
819	1	1	0	0	1	1	0	0	1	1	1 4 6 3
820	1	1	0	0	1	1	0	1	0	0	1 4 6 4
821	1	1	0	0	1	1	0	1	0	1	1 4 6 5
822	1	1	0	0	1	1	0	1	1	0	1 4 6 6
823	1	1	0	0	1	1	0	1	1	1	1 4 6 7
824	1	1	0	0	1	1	1	0	0	0	1 4 7 0
825	1	1	0	0	1	1	1	0	0	1	1 4 7 1
826	1	1	0	0	1	1	1	0	1	0	1 4 7 2
827	1	1	0	0	1	1	1	0	1	1	1 4 7 3
828	1	1	0	0	1	1	1	1	0	0	1 4 7 4
829	1	1	0	0	1	1	1	1	0	1	1 4 7 5
830	1	1	0	0	1	1	1	1	1	0	1 4 7 6
831	1	1	0	0	1	1	1	1	1	1	1 4 7 7

DEC.	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	OCTAL
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833	1	1	0	1	0	0	0	0	0	1	1 5 0 1
834	1	1	0	1	0	0	0	0	1	0	1 5 0 2
835	1	1	0	1	0	0	0	0	1	1	1 5 0 3
836	1	1	0	1	0	0	0	1	0	0	1 5 0 4
837	1	1	0	1	0	0	0	1	0	1	1 5 0 5
838	1	1	0	1	0	0	0	1	1	0	1 5 0 6
839	1	1	0	1	0	0	0	1	1	1	1 5 0 7
840	1	1	0	1	0	0	1	0	0	0	1 5 1 0
841	1	1	0	1	0	0	1	0	0	1	1 5 1 1
842	1	1	0	1	0	0	1	0	1	0	1 5 1 2
843	1	1	0	1	0	0	1	0	1	1	1 5 1 3
844	1	1	0	1	0	0	1	1	0	0	1 5 1 4
845	1	1	0	1	0	0	1	1	0	1	1 5 1 5
846	1	1	0	1	0	0	1	1	1	0	1 5 1 6
847	1	1	0	1	0	0	1	1	1	1	1 5 1 7
848	1	1	0	1	0	1	0	0	0	0	1 5 2 0
849	1	1	0	1	0	1	0	0	0	1	1 5 2 1
850	1	1	0	1	0	1	0	0	1	0	1 5 2 2
851	1	1	0	1	0	1	0	0	1	1	1 5 2 3
852	1	1	0	1	0	1	0	1	0	0	1 5 2 4
853	1	1	0	1	0	1	0	1	0	1	1 5 2 5
854	1	1	0	1	0	1	0	1	1	0	1 5 2 6
855	1	1	0	1	0	1	0	1	1	1	1 5 2 7
856	1	1	0	1	0	1	1	0	0	0	1 5 3 0
857	1	1	0	1	0	1	1	0	0	1	1 5 3 1
858	1	1	0	1	0	1	1	0	1	0	1 5 3 2
859	1	1	0	1	0	1	1	0	1	1	1 5 3 3
860	1	1	0	1	0	1	1	1	0	0	1 5 3 4
861	1	1	0	1	0	1	1	1	0	1	1 5 3 5
862	1	1	0	1	0	1	1	1	1	0	1 5 3 6
863	1	1	0	1	0	1	1	1	1	1	1 5 3 7
864	1	1	0	1	1	0	0	0	0	0	1 5 4 0
865	1	1	0	1	1	0	0	0	0	1	1 5 4 1
866	1	1	0	1	1	0	0	0	1	0	1 5 4 2
867	1	1	0	1	1	0	0	0	1	1	1 5 4 3
868	1	1	0	1	1	0	0	1	0	0	1 5 4 4
869	1	1	0	1	1	0	0	1	0	1	1 5 4 5
870	1	1	0	1	1	0	0	1	1	0	1 5 4 6
871	1	1	0	1	1	0	0	1	1	1	1 5 4 7
872	1	1	0	1	1	0	1	0	0	0	1 5 5 0
873	1	1	0	1	1	0	1	0	0	1	1 5 5 1
874	1	1	0	1	1	0	1	0	1	0	1 5 5 2
875	1	1	0	1	1	0	1	0	1	1	1 5 5 3
876	1	1	0	1	1	0	1	1	0	0	1 5 5 4
877	1	1	0	1	1	0	1	1	0	1	1 5 5 5
878	1	1	0	1	1	0	1	1	1	0	1 5 5 6
879	1	1	0	1	1	0	1	1	1	1	1 5 5 7
880	1	1	0	1	1	1	0	0	0	0	1 5 6 0
881	1	1	0	1	1	1	0	0	0	1	1 5 6 1
882	1	1	0	1	1	1	0	0	1	0	1 5 6 2
883	1	1	0	1	1	1	0	0	1	1	1 5 6 3
884	1	1	0	1	1	1	0	1	0	0	1 5 6 4
885	1	1	0	1	1	1	0	1	0	1	1 5 6 5
886	1	1	0	1	1	1	0	1	1	0	1 5 6 6
887	1	1	0	1	1	1	0	1	1	1	1 5 6 7
888	1	1	0	1	1	1	1	0	0	0	1 5 7 0
889	1	1	0	1	1	1	1	0	0	1	1 5 7 1
890	1	1	0	1	1	1	1	0	1	0	1 5 7 2
891	1	1	0	1	1	1	1	0	1	1	1 5 7 3
892	1	1	0	1	1	1	1	1	0	0	1 5 7 4
893	1	1	0	1	1	1	1	1	0	1	1 5 7 5
894	1	1	0	1	1	1	1	1	1	0	1 5 7 6
895	1	1	0	1	1	1	1	1	1	1	1 5 7 7

DEC.	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	OCTAL
896	1	1	1	0	0	0	0	0	0	0	1 6 0 0
897	1	1	1	0	0	0	0	0	0	1	1 6 0 1
898	1	1	1	0	0	0	0	0	1	0	1 6 0 2
899	1	1	1	0	0	0	0	0	1	1	1 6 0 3
900	1	1	1	0	0	0	0	1	0	0	1 6 0 4
901	1	1	1	0	0	0	0	1	0	1	1 6 0 5
902	1	1	1	0	0	0	0	1	1	0	1 6 0 6
903	1	1	1	0	0	0	0	1	1	1	1 6 0 7
904	1	1	1	0	0	0	1	0	0	0	1 6 1 0
905	1	1	1	0	0	0	1	0	0	1	1 6 1 1
906	1	1	1	0	0	0	1	0	1	0	1 6 1 2
907	1	1	1	0	0	0	1	0	1	1	1 6 1 3
908	1	1	1	0	0	0	1	1	0	0	1 5 1 4
909	1	1	1	0	0	0	1	1	0	1	1 6 1 5
910	1	1	1	0	0	0	1	1	1	0	1 6 1 6
911	1	1	1	0	0	0	1	1	1	1	1 6 1 7
912	1	1	1	0	0	1	0	0	0	0	1 6 2 0
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914	1	1	1	0	0	1	0	0	1	0	1 6 2 2
915	1	1	1	0	0	1	0	0	1	1	1 6 2 3
916	1	1	1	0	0	1	0	1	0	0	1 6 2 4
917	1	1	1	0	0	1	0	1	0	1	1 6 2 5
918	1	1	1	0	0	1	0	1	1	0	1 6 2 6
919	1	1	1	0	0	1	0	1	1	1	1 6 2 7
920	1	1	1	0	0	1	1	0	0	0	1 6 3 0
921	1	1	1	0	0	1	1	0	0	1	1 6 3 1
922	1	1	1	0	0	1	1	0	1	0	1 6 3 2
923	1	1	1	0	0	1	1	0	1	1	1 6 3 3
924	1	1	1	0	0	1	1	1	0	0	1 6 3 4
925	1	1	1	0	0	1	1	1	0	1	1 6 3 5
926	1	1	1	0	0	1	1	1	1	0	1 6 3 6
927	1	1	1	0	0	1	1	1	1	1	1 6 3 7
928	1	1	1	0	1	0	0	0	0	0	1 6 4 0
929	1	1	1	0	1	0	0	0	0	1	1 6 4 1
930	1	1	1	0	1	0	0	0	1	0	1 6 4 2
931	1	1	1	0	1	0	0	0	1	1	1 6 4 3
932	1	1	1	0	1	0	0	1	0	0	1 6 4 4
933	1	1	1	0	1	0	0	1	0	1	1 6 4 5
934	1	1	1	0	1	0	0	1	1	0	1 6 4 6
935	1	1	1	0	1	0	0	1	1	1	1 6 4 7
936	1	1	1	0	1	0	1	0	0	0	1 6 5 0
937	1	1	1	0	1	0	1	0	0	1	1 6 5 1
938	1	1	1	0	1	0	1	0	1	0	1 6 5 2
939	1	1	1	0	1	0	1	0	1	1	1 6 5 3
940	1	1	1	0	1	0	1	1	0	0	1 6 5 4
941	1	1	1	0	1	0	1	1	0	1	1 6 5 5
942	1	1	1	0	1	0	1	1	1	0	1 6 5 6
943	1	1	1	0	1	0	1	1	1	1	1 6 5 7
944	1	1	1	0	1	1	0	0	0	0	1 6 6 0
945	1	1	1	0	1	1	0	0	0	1	1 6 6 1
946	1	1	1	0	1	1	0	0	1	0	1 6 6 2
947	1	1	1	0	1	1	0	0	1	1	1 6 6 3
948	1	1	1	0	1	1	0	1	0	0	1 6 6 4
949	1	1	1	0	1	1	0	1	0	1	1 6 6 5
950	1	1	1	0	1	1	0	1	1	0	1 6 6 6
951	1	1	1	0	1	1	0	1	1	1	1 6 6 7
952	1	1	1	0	1	1	1	0	0	0	1 6 7 0
953	1	1	1	0	1	1	1	0	0	1	1 6 7 1
954	1	1	1	0	1	1	1	0	1	0	1 6 7 2
955	1	1	1	0	1	1	1	0	1	1	1 6 7 3
956	1	1	1	0	1	1	1	1	0	0	1 6 7 4
957	1	1	1	0	1	1	1	1	0	1	1 6 7 5
958	1	1	1	0	1	1	1	1	1	0	1 6 7 6
959	1	1	1	0	1	1	1	1	1	1	1 6 7 7

DEC.	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	OCTAL
960	1	1	1	1	0	0	0	0	0	0	1 7 0 0
961	1	1	1	1	0	0	0	0	0	1	1 7 0 1
962	1	1	1	1	0	0	0	0	1	0	1 7 0 2
963	1	1	1	1	0	0	0	0	1	1	1 7 0 3
964	1	1	1	1	0	0	0	1	0	0	1 7 0 4
965	1	1	1	1	0	0	0	1	0	1	1 7 0 5
966	1	1	1	1	0	0	0	1	1	0	1 7 0 6
967	1	1	1	1	0	0	0	1	1	1	1 7 0 7
968	1	1	1	1	0	0	1	0	0	0	1 7 1 0
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970	1	1	1	1	0	0	1	0	1	0	1 7 1 2
971	1	1	1	1	0	0	1	0	1	1	1 7 1 3
972	1	1	1	1	0	0	1	1	0	0	1 7 1 4
973	1	1	1	1	0	0	1	1	0	1	1 7 1 5
974	1	1	1	1	0	0	1	1	1	0	1 7 1 6
975	1	1	1	1	0	0	1	1	1	1	1 7 1 7
976	1	1	1	1	0	1	0	0	0	0	1 7 2 0
977	1	1	1	1	0	1	0	0	0	1	1 7 2 1
978	1	1	1	1	0	1	0	0	1	0	1 7 2 2
979	1	1	1	1	0	1	0	0	1	1	1 7 2 3
980	1	1	1	1	0	1	0	1	0	0	1 7 2 4
981	1	1	1	1	0	1	0	1	0	1	1 7 2 5
982	1	1	1	1	0	1	0	1	1	0	1 7 2 6
983	1	1	1	1	0	1	0	1	1	1	1 7 2 7
984	1	1	1	1	0	1	1	0	0	0	1 7 3 0
985	1	1	1	1	0	1	1	0	0	1	1 7 3 1
986	1	1	1	1	0	1	1	0	1	0	1 7 3 2
987	1	1	1	1	0	1	1	0	1	1	1 7 3 3
988	1	1	1	1	0	1	1	1	0	0	1 7 3 4
989	1	1	1	1	0	1	1	1	0	1	1 7 3 5
990	1	1	1	1	0	1	1	1	1	0	1 7 3 6
991	1	1	1	1	0	1	1	1	1	1	1 7 3 7
992	1	1	1	1	1	0	0	0	0	0	1 7 4 0
993	1	1	1	1	1	0	0	0	0	1	1 7 4 1
994	1	1	1	1	1	0	0	0	1	0	1 7 4 2
995	1	1	1	1	1	0	0	0	1	1	1 7 4 3
996	1	1	1	1	1	0	0	1	0	0	1 7 4 4
997	1	1	1	1	1	0	0	1	0	1	1 7 4 5
998	1	1	1	1	1	0	0	1	1	0	1 7 4 6
999	1	1	1	1	1	0	0	1	1	1	1 7 4 7
1000	1	1	1	1	1	0	1	0	0	0	1 7 5 0
1001	1	1	1	1	1	0	1	0	0	1	1 7 5 1
1002	1	1	1	1	1	0	1	0	1	0	1 7 5 2
1003	1	1	1	1	1	0	1	0	1	1	1 7 5 3
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1005	1	1	1	1	1	0	1	1	0	1	1 7 5 5
1006	1	1	1	1	1	0	1	1	1	0	1 7 5 6
1007	1	1	1	1	1	0	1	1	1	1	1 7 5 7
1008	1	1	1	1	1	1	0	0	0	0	1 7 6 0
1009	1	1	1	1	1	1	0	0	0	1	1 7 6 1
1010	1	1	1	1	1	1	0	0	1	0	1 7 6 2
1011	1	1	1	1	1	1	0	0	1	1	1 7 6 3
1012	1	1	1	1	1	1	0	1	0	0	1 7 6 4
1013	1	1	1	1	1	1	0	1	0	1	1 7 6 5
1014	1	1	1	1	1	1	0	1	1	0	1 7 6 6
1015	1	1	1	1	1	1	0	1	1	1	1 7 6 7
1016	1	1	1	1	1	1	1	0	0	0	1 7 7 0
1017	1	1	1	1	1	1	1	0	0	1	1 7 7 1
1018	1	1	1	1	1	1	1	0	1	0	1 7 7 2
1019	1	1	1	1	1	1	1	0	1	1	1 7 7 3
1020	1	1	1	1	1	1	1	1	0	0	1 7 7 4
1021	1	1	1	1	1	1	1	1	0	1	1 7 7 5
1022	1	1	1	1	1	1	1	1	1	0	1 7 7 6
1023	1	1	1	1	1	1	1	1	1	1	1 7 7 7

Bipolar
Memory
Bipolar
Memory

Bipolar
Memory
Bipolar
Memory

CHAPTER 7

- Data Sheets

ECL ISOPLANAR MEMORY F100414

256 × 1-BIT FULLY DECODED RANDOM ACCESS MEMORY

FAIRCHILD TEMPERATURE AND VOLTAGE COMPENSATED ECL

GENERAL DESCRIPTION – The F100414 is a 256-bit Read/Write Random Access Memory, organized 256 words by one bit. It has typical access time of 7 ns and is designed for high speed scratch pad, control and buffer storage applications. The device includes full address decoding on the chip, has separate Data In and non-inverted Data Out lines, and has three active LOW Chip Select lines.

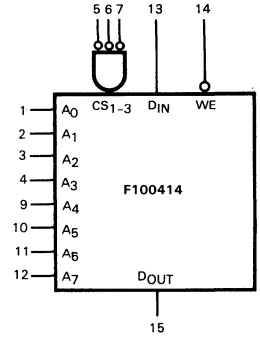
With on chip voltage and temperature compensation the F100414 is compatible with the F100K and F95K series of ECL Logic. The device is packaged in the hermetic ceramic 16-pin dual in-line or 16-pin flat package and specified for operation over the temperature range 0° to 85°C.

- **VERY HIGH SPEED**
- **COMPATIBLE WITH F100K and F95K ECL LOGIC**
- **READ ACCESS TIME – 7 ns TYP**
- **CHIP SELECT ACCESS TIME – 4 ns TYP**
- **POWER DISSIPATION – 1.8 mW/BIT**
- **50 kΩ INPUT PULL-DOWN RESISTORS ON CHIP SELECT**
- **OUTPUTS CAN BE WIRED-OR FOR EASY MEMORY EXPANSION**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**
- **ORGANIZED – 256 WORDS X 1 BIT**

PIN NAMES

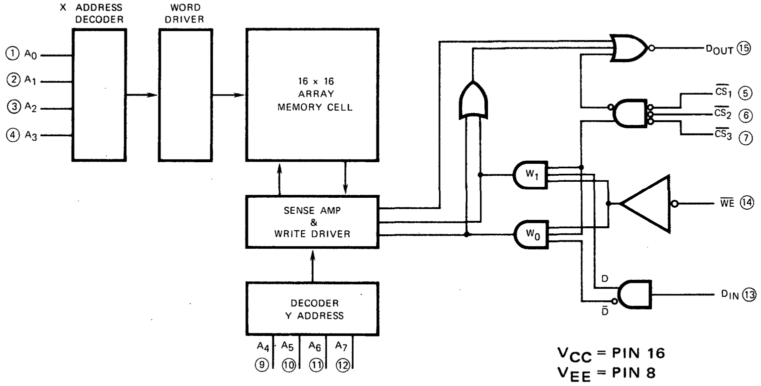
$\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$	Chip Select Inputs
$A_0 - A_7$	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input

LOGIC SYMBOL



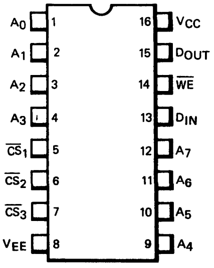
V_{CC} = PIN 16
V_{EE} = PIN 8

LOGIC DIAGRAM



V_{CC} = PIN 16
V_{EE} = PIN 8
○ = PIN NUMBERS

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The F100414 is a fully decoded 256-bit Read/Write Random Access Memory, organized 256 words by one bit. Word selection is achieved by means of an 8-bit address A_0 to A_7.

The active LOW chip select inputs are provided for increased logic flexibility. This permits memory array expansion up to 2048 words with the 10161 decoder. For larger memories, the fast chip select time permits the decoding of Chip Select, $\overline{CS}$, from the address without affecting system performance.

The read and write operations are controlled by the state of the active LOW Write Enable, ($\overline{WE}$, pin 14). With $\overline{WE}$ held LOW, and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH, and the chip selected. Data in the addressed location is presented at D_{OUT} and is read out non-inverted. The D_{OUT} is LOW except when reading a stored HIGH.

Open emitter outputs are provided on the F100414 to allow maximum flexibility in output wired-OR connection for memory expansion.

TABLE 1 – TRUTH TABLE

INPUT					OUTPUT	MODE
$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_3$	$\overline{WE}$	D_{IN}		
X	X	H*	X	X	L	NOT SELECTED
L	L	L	L	L	L	WRITE "0"
L	L	L	L	H	L	WRITE "1"
L	L	L	H	X	D_{OUT}	READ

*One or more Chip Selects HIGH

NOTE:
L = LOW Voltage Levels = –1.7 V
H = HIGH Voltage Levels = –0.9 V
(Nominal Values)
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to 150°C
Temperature (Ambient) Under Bias	–55°C to 125°C
V_{EE} Pin Potential to Ground Pin	–7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	–30 mA to +0.1 mA

GUARANTEED OPERATING RANGES

SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE SEE NOTE 4
MIN	TYP	MAX	
–5.7 V	–4.5 V	–4.2 V	0°C to 85°C

DC CHARACTERISTICS: V_{EE} = –4.5 V, V_{CC} = GND, T_A = 0°C +85°C, output load 50 Ω to –2.0 V

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		B	TYP	A			
V_{OH}	Output HIGH Voltage	–1025	–955	–880	mV	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to –2.0 V
V_{OL}	Output LOW Voltage	–1810	–1705	–1620	mV		
V_{OHC}	Output HIGH Voltage	–1035			mV	$V_{IN} = V_{IHB}$ or V_{ILA}	
V_{OLC}	Output LOW Voltage			–1610	mV		
V_{IH}	Input HIGH Voltage	–1165		–880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	–1810		–1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IH}	Input HIGH Current			220	μA	$V_{IN} = V_{IHA}$	
I_{IL}	Input LOW Current, $\overline{CS}$ All others	0.5 –50		170	μA	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current		–100		mA	All inputs and output open	

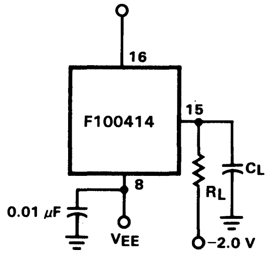
AC CHARACTERISTICS: V_{EE} =−4.5 V, ±10%→Output Load = 50 Ω 10 pF to −2.0 V

SYMBOL	PARAMETER	MIN LIMIT	TYP (Note 3)	MAX LIMIT	UNITS	CONDITIONS
READ MODE						
t_{ACS}	Chip Select Access Time		4		ns	Fig. 1a & b Measured at 50% of Input to Valid Output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH}). Note 5.
t_{RCS}	Chip Select Recovery Time		4		ns	
t_{AA}	Address Access Time		7		ns	
WRITE MODE						
t_W	Write Pulse Width	6	4		ns	t_{WSA} = 3 ns
t_{WSD}	Data Set-up Time Prior to Write		0		ns	
t_{WHD}	Data Hold Time After Write		0		ns	
t_{WSA}	Address Set-up Time		1		ns	t_W = 6 ns Fig. 2 Measured at 50% of Input to Valid Output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})
t_{WHA}	Address Hold Time		0		ns	
t_{WSCS}	Chip Select Set-up Time		0		ns	
t_{WHCS}	Chip Select Hold Time		1		ns	
t_{WS}	Write Disable Time		4		ns	
t_{WR}	Write Recovery Time		5		ns	
RISE AND FALL TIME						
t_r	Output Rise Time		4		ns	Measured between 20% & 80% points. (Fig. 1a)
t_f	Output Fall Time		4		ns	
CAPACITANCE						
C_{IN}	Input Lead Capacitance		4		pF	Measure with a Pulse Technique
C_{OUT}	Output Lead Capacitance		7		pF	

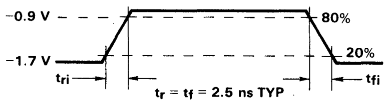
NOTES:
1. Conditions for testing, not shown in the tables are chosen to guarantee operation under "worst case" conditions.
2. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{EE} = −5.2 V, T_A = +25°C and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and two minute warm up period. Typical thermal resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   θ_{JC} (Junction to Case) = 25°C/Watt
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
6. DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET:
   The symbols and terms used in this data sheet have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are:
   "A" the value closest to positive infinity.
   "B" the value closest to negative infinity.

AC TEST LOAD AND WAVEFORMS

LOADING CONDITIONS



INPUT LEVELS



All Timing Measurements Referenced to 50% of Input Levels
C_L = 10 pF including Jig and Stray Capacitance
R_L = 50 Ω to −2.0 V

READ MODE PROPAGATION DELAY FROM CHIP SELECT

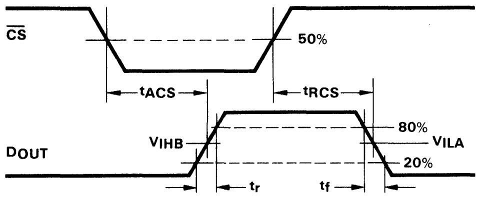


Fig. 1a

READ MODE PROPAGATION DELAY FROM ADDRESS

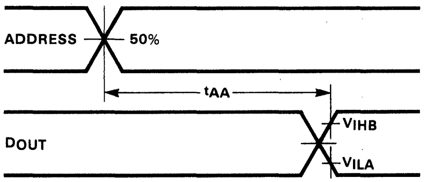


Fig. 1b

WRITE MODE

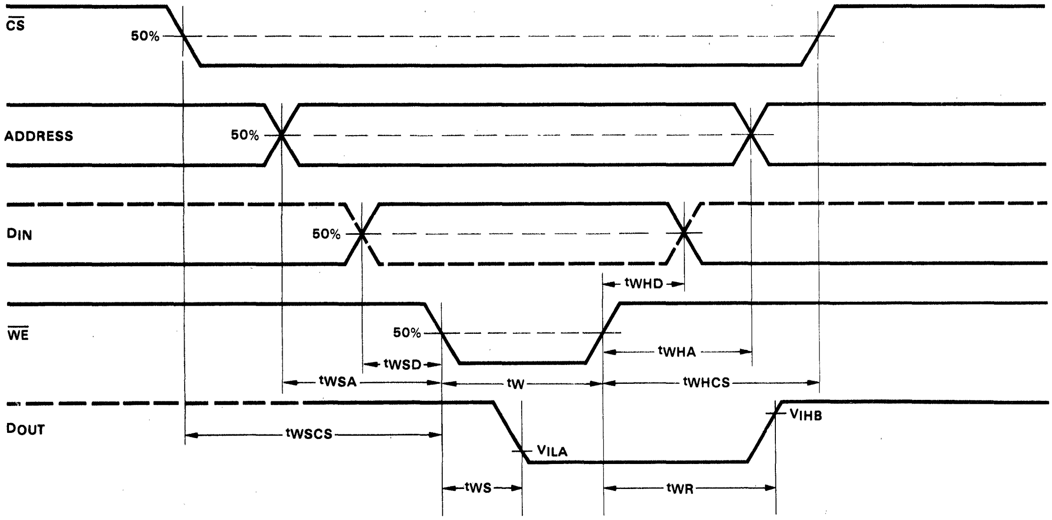


Fig. 2

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

4096 WORD X N–BIT SYSTEM

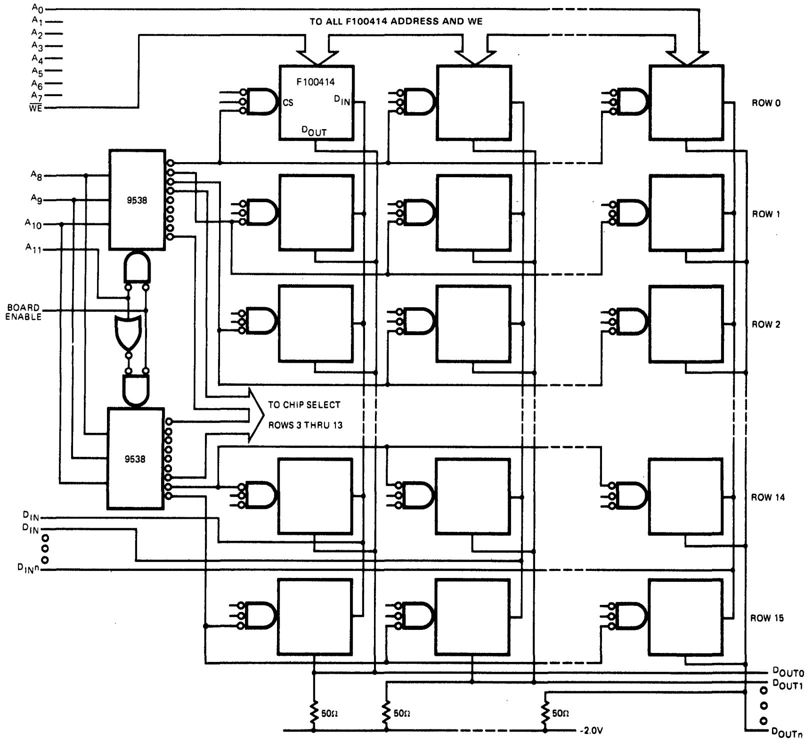


Fig. 3.

F100415
ECL ISOPLANAR MEMORY
1024×1-BIT FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION – The F100415 is a 1024-bit Read/Write Random Access Memory organized 1024 words by one bit per word. Designed for high speed scratchpad, control and buffer storage applications. The device is specified with a maximum read cycle time of 20 ns over the commercial temperature and voltage range.

With on-chip voltage and temperature compensation, this memory is compatible with the F100K and F95K Series of ECL logic.

Other features include full address decoding on chip, separate Data In and non-inverting Data Out lines, and an active LOW Chip Select input.

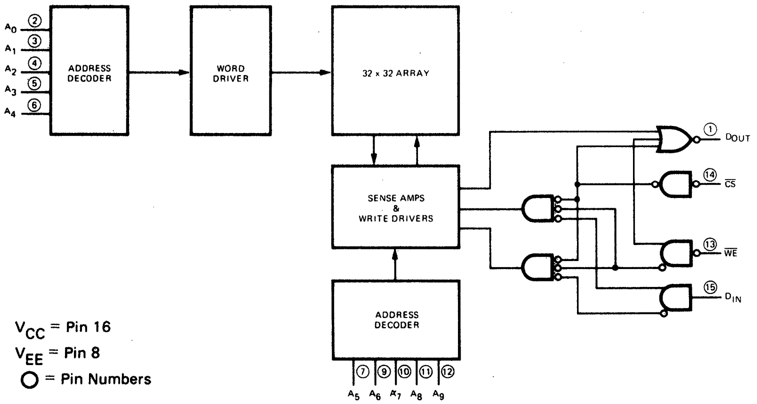
The F100415 is packaged in a hermetic ceramic 16-pin dual in-line package and is specified for operation over the 0°C to +85°C temperature range.

- **COMPATIBLE WITH F100K AND F95K ECL LOGIC**
- **MAXIMUM CYCLE TIME OF 20 ns OVER TEMPERATURE**
- **OPEN EMITTER OUTPUTS FOR EASE OF MEMORY EXPANSION**
- **ORGANIZATION – 1024 WORDS X 1 BIT**
- **POWER DISSIPATION OF 0.5 mW/BIT**

PIN NAMES

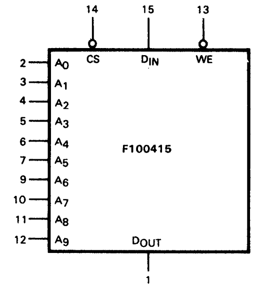
$\overline{CS}$	Chip Select Input
A_0 to A_9	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input

LOGIC DIAGRAM



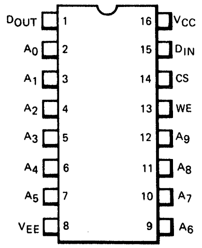
V_{CC} = Pin 16
V_{EE} = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
V_{EE} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The F100415 is a fully decoded 1024-bit Read/Write Random Access Memory organized 1024 words by one bit. Bit selection is acheived by means of a 10-bit address, A_0 to A_9. One Chip Select input is provided for memory array expansion up to 2048 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of Chip Select ($\overline{CS}$) form the address without increasing address access time. The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$). With $\overline{WE}$ and $\overline{CS}$ held LOW, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and $\overline{CS}$ held LOW. Data in the specified location is presented at D_{OUT} and is non-inverted.

An unterminated emitter-follower output is provided on the F100415 to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many F100415 can be tied together. In other applications the wired-OR is not used. In either case an external 50 Ω pull down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is off.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{EE} Pin Potential to Ground Pin	−7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	−30 mA to +0.1 mA

TABLE 1 – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	OPEN EMITTER	
H	X	X	L	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	L	WRITE "1"
L	H	X	D_{OUT}	READ

L = LOW Voltage Levels = −1.7 V
H = HIGH Voltage Levels = −0.9 V
(Nominal values)
X = Don't Care

GUARANTEED OPERATING RANGES

SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE NOTE 4
MIN	TYP	MAX	
−5.7 V	−4.5 V	−4.2 V	0°C to 85°C

DC CHARACTERISTICS: V_{EE} = −4.5V, V_{CC} = GND, T_A = 0°C to +85°C (Note A)

SYMBOL	CHARACTERISTIC	LIMITS (Note 6)			UNITS	CONDITIONS	
		B	TYP (Note 3)	A			
V_{OH}	Output Voltage HIGH	−1025	−955	−880	mV	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to −2.0 V
V_{OL}	Output Voltage LOW	−1810	−1705	−1620	mV		
V_{OHC}	Output Voltage HIGH	−1035			mV	$V_{IN} = V_{IHB}$ or V_{ILA}	
V_{OLC}	Output Voltage LOW			−1610	mV		
V_{IH}	Input Voltage HIGH	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input Voltage LOW	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IH}	Input Current HIGH			220	μA	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW, $\overline{CS}$ All others	0.5 −50		170	μA	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current	−150	−105		mA	All Inputs and Output open	

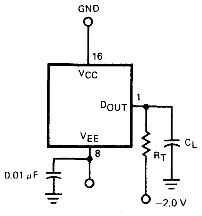
NOTES:

1. Conditions for testing, not shown in the tables are chosen to guarantee operation under "worst case" conditions.
2. The specified Limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{EE} = −5.2 V, T_A = 25°C and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   θ_{JC} (Junction to Case) = 25°C/Watt
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
6. DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET:
   The symbols and terms used in this data sheet have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.

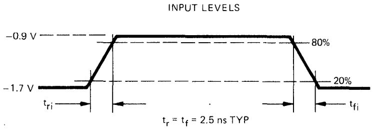
AC CHARACTERISTICS: $V_{EE} = -4.5$ V, $T_A = 0°C$ to 85°C, V_{CC} = GND

SYMBOL	PARAMETER	MIN	TYP (Note 3)	MAX	UNITS	CONDITIONS
t_{ACS}	Chip Select Access Time		5		ns	Fig 1a and b measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} or V_{OH})
t_{RCS}	Chip Select Recovery Time		5		ns	
t_{AA}	Address Access Time		12	20	ns	
t_W	Write Pulse Width (to Guarantee writing)	12	9		ns	t_{WSA} = 8 ns
t_{WSD}	Data Sep-up Time Prior to Write		0		ns	
t_{WHD}	Data Hold Time After Write		0			
t_{WSA}	Address Set-up Time Prior to Write		5		ns	t_W = 12 ns
t_{WHA}	Address Hold Time After Write		0		ns	
t_{WSCS}	Chip Select Set-up Time Prior to Write		0		ns	Fig. 2 measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})
t_{WHCS}	Chip Select Hold Time After Write		0		ns	
t_{WS}	Write Disable Time		5		ns	
t_{WR}	Write Recovery Time		10		ns	
t_r	Output Rise Time		4.5		ns	Measured between 20% and 80% points. (Fig. 1a)
t_f	Output Fall Time		5.5		ns	
C_{IN}	Input Pin Capacitance		4	5	pF	Measure with a Pulse Technique
C_{OUT}	Output Pin Capacitance		7	8	pF	

LOADING CONDITIONS



INPUT LEVELS



All Timing Measurements Referenced to 50% of Input Levels

C_L = 30 pF including Jig and Stray Capacitance

R_T = 50 Ω Termination of Scope

READ MODE PROPAGATION DELAY FROM CHIP SELECT

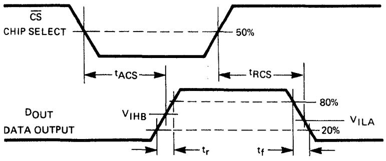


Fig. 1a

READ MODE PROPAGATION DELAY FROM ADDRESS

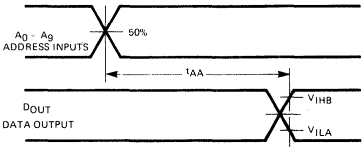


Fig. 1b

WRITE MODE

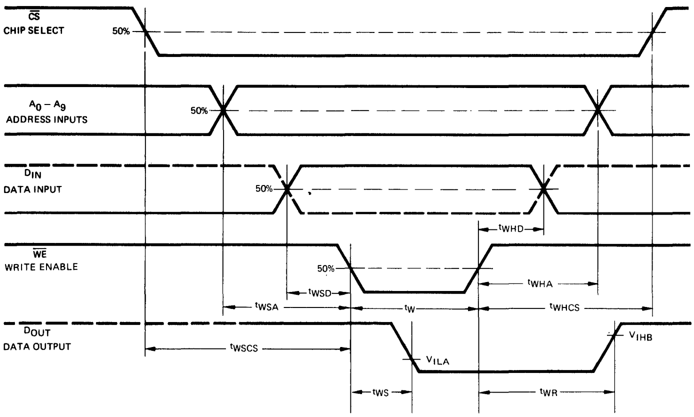
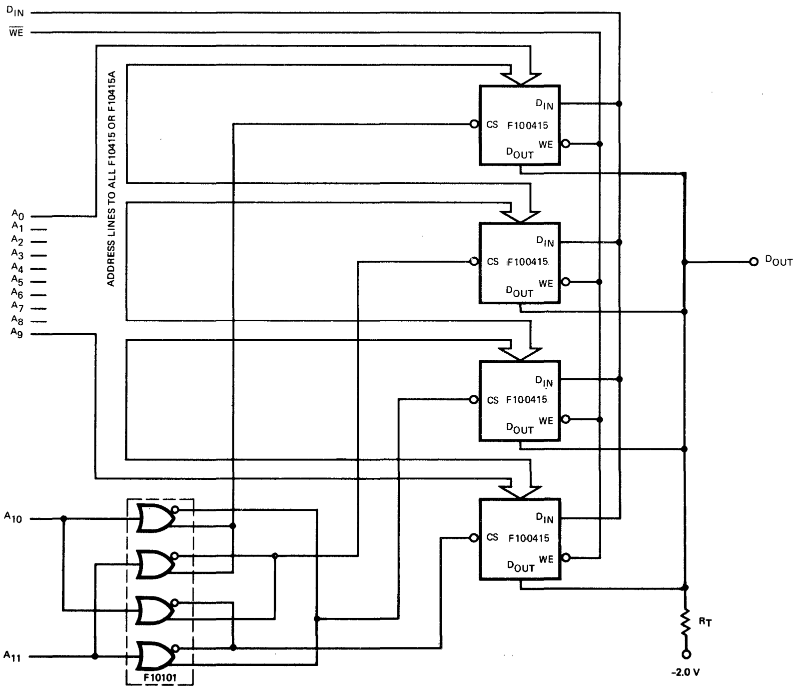


Fig. 2

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

APPLICATIONS



4096-WORD X 1-BIT SYSTEM

Fig. 3

F10145A

16×4 REGISTER FILE (RAM)

F10K-VOLTAGE COMPENSATED ECL

GENERAL DESCRIPTION — The F10145A is a high speed 64-bit Random Access Memory organized as a 16-word by 4-bit array. External logic requirements are minimized by internal address decoding, while memory expansion and data bussing are facilitated by the output disabling features of the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs.

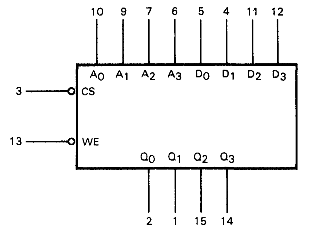
A HIGH signal on $\overline{CS}$ prevents read and write operations and forces the outputs to the LOW state. When $\overline{CS}$ is LOW, the $\overline{WE}$ input controls chip operations. A HIGH signal on $\overline{WE}$ disables the Data input (D_n) buffers and enables readout from the memory location determined by the Address (A_n) inputs. A LOW signal on $\overline{WE}$ forces the Q_n outputs LOW and allows data on the D_n inputs to be stored in the addressed location. Data exits in the same logical sense as presented at the data inputs, *i.e.,* the memory is non-inverting.

- READ ACCESS TIME — 7 ns TYP
- 50 kΩ INPUT PULL-DOWN RESISTORS
- OUTPUTS CAN BE WIRED-OR FOR EASY MEMORY EXPANSION
- CHIP SELECT ACCESS TIME — 4 ns TYP
- VOLTAGE COMPENSATED, INSENSITIVE TO POWER SUPPLY VARIATIONS
- FULLY COMPATIBLE WITH ALL 10,000 SERIES ECL

PIN NAMES

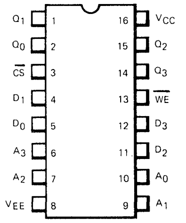
$\overline{CS}$	Chip Select
A_n	Address Lines
D_n	Data Input Lines
$\overline{WE}$	Write Enable
Q_n	Data Output Lines

LOGIC SYMBOL

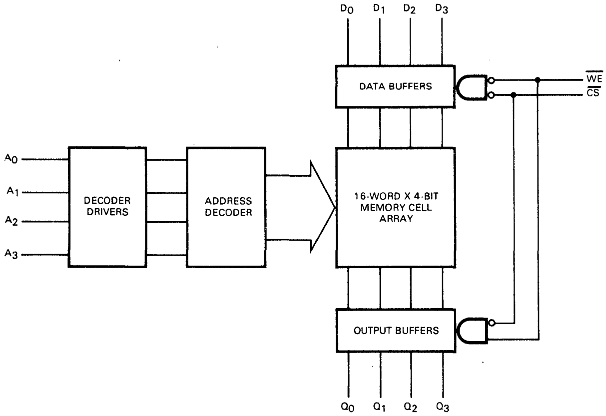


V_{CC} = Pin 16, V_{EE} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



LOGIC DIAGRAM



V_{CC} = Pin 16
V_{EE} = Pin 8

DC CHARACTERISTICS: $V_{EE} = -5.2\ V$, $V_{CC} = GND$

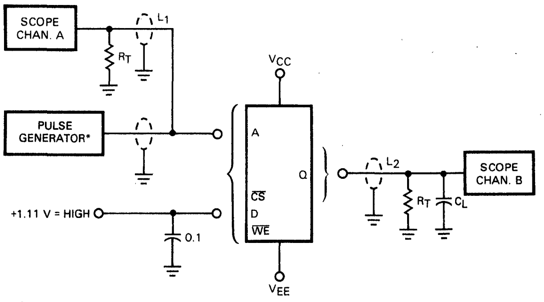
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	-1000		-840	mV	0°C	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to -2 V
		-960		-810		25°C		
		-900		-720		75°C		
V_{OL}	Output Voltage LOW	-1870		-1665	mV	0°C		
		-1850		-1650		25°C		
		-1830		-1625		75°C		
V_{OHC}	Output Voltage HIGH	-1020			mV	0°C	$V_{IN} = V_{IHB}$ or V_{ILA}	
		-980				25°C		
		-920				75°C		
V_{OLC}	Output Voltage LOW			-1645	mV	0°C		
				-1630		25°C		
				-1605		75°C		
V_{IH}	Input Voltage HIGH	-1145		-840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs	
		-1105		-810		25°C		
		-1045		-720		75°C		
V_{IL}	Input Voltage LOW	-1870		-1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs	
		-1850		-1475		25°C		
		-1830		-1450		75°C		
I_{IH}	Input Current HIGH				μA	25°C	$V_{IN} = V_{IHA}$	
	Pins 3, 6, 7, 9, 10			200				
	Pins 4,5,11,12,13			220				
I_{IL}	Input Current LOW	0.5			μA	25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Supply Current	-130	-100		mA	25°C	Inputs and Outputs Open	

AC CHARACTERISTICS: $V_{EE} = -5.2\ V$, $T_A = 25°C$

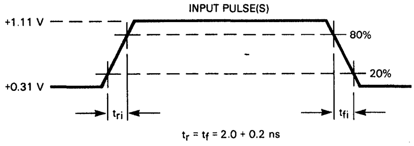
SYMBOL	CHARACTERISTIC	LIMITS B	LIMITS TYP	LIMITS A	UNITS	CONDITIONS
	Access/Recovery Times					
t_{ACS}	Chip Select Access	3.0	4.5	6.0	ns	Figures 1, 3
t_{RCS}	Chip Select Recovery	3.0	4.5	6.0	ns	
t_{AA}	Address Access	4.5	6.5	9.0	ns	
	Write Times					
	Set-Up					
t_{WSD}	Data	4.5	3.0		ns	
t_{WSCS}	Chip Select	4.5	2.5		ns	
t_{WSA}	Address	3.5	1.5		ns	Figures 1, 2a
	Hold					
t_{WHD}	Data	-1.0	-2.5		ns	
t_{WHCS}	Chip Select	0.5	0.0		ns	
t_{WHA}	Address	1.0	-1.0		ns	
t_{WR}	Write Recovery Time	3.0	4.5	6.0	ns	Figures 1, 3
t_{WS}	Write Disable Time	3.0	4.5	6.0	ns	
t_W	Write Pulse Width, Min	4.0	2.5		ns	Figures 1, 2a
t_{CS}	Chip Select Pulse Width, Min	4.0	2.5		ns	
	Select Times					
	Set-Up					
t_{CSD}	Data	4.5	3.0		ns	
t_{CSW}	Write Enable	4.5	2.5		ns	
t_{CSA}	Address	3.5	1.5		ns	Figures 1, 2b
	Hold					
t_{CHD}	Data	-1.0	-2.5		ns	
t_{CHW}	Write Enable	0.5	0.0		ns	
t_{CHA}	Address	1.0	-1.0		ns	
	Transition Times					
t_{TLH}	20% to 80%	1.5	2.5	3.9	ns	Figures 1, 3
t_{THL}	80% to 20%	1.5	2.5	3.9	ns	

SWITCHING CIRCUIT AND WAVEFORMS

Fig. 1



*ONE OR MORE GENERATORS, AS REQUIRED

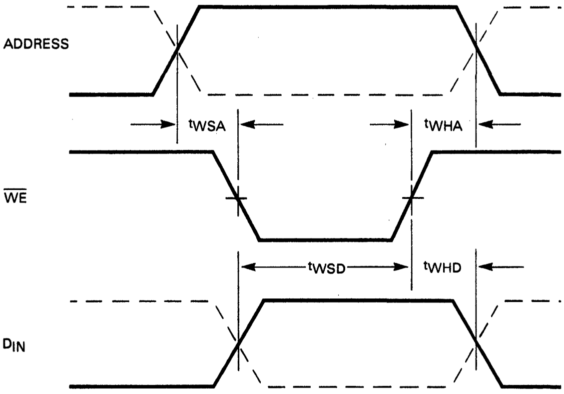


L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance ⩽ 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2} = 2.0$ V
$V_{EE} = -3.2$ V
Open input = LOW

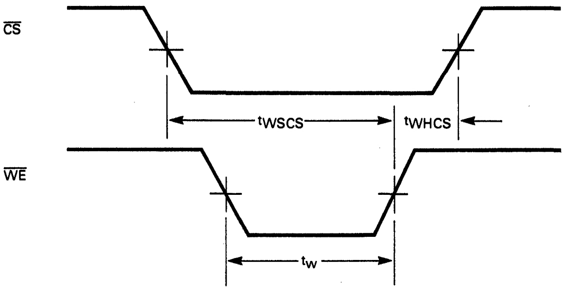
Fig. 2. WRITE MODES

2a. WRITE ENABLE STROBE

ADDRESS AND D_{IN} SET-UP AND HOLD TIMES ($\overline{CS}$ = LOW)

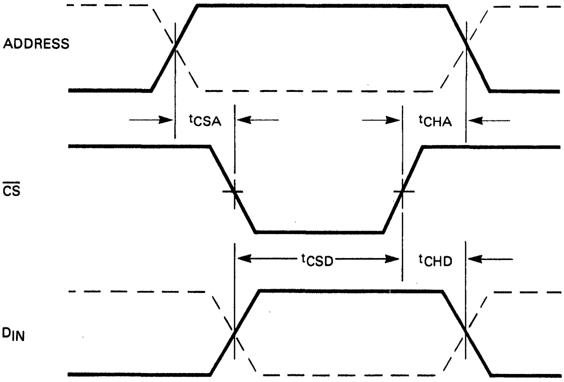


CHIP SELECT SET-UP AND HOLD TIMES

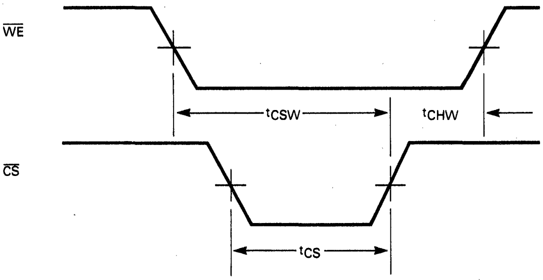


2b. CHIP SELECT STROBE

ADDRESS AND D_{IN} SET-UP AND HOLD TIMES ($\overline{WE}$ = LOW)



WRITE ENABLE SET-UP AND HOLD TIMES, $\overline{CS}$ PULSE WIDTH^2

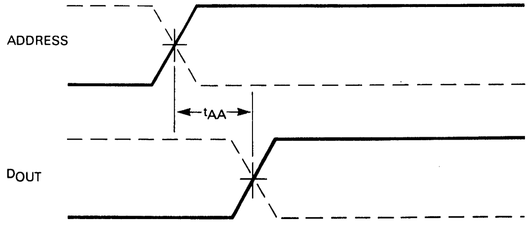


WAVEFORMS (Cont'd)

Fig. 3. READ MODES

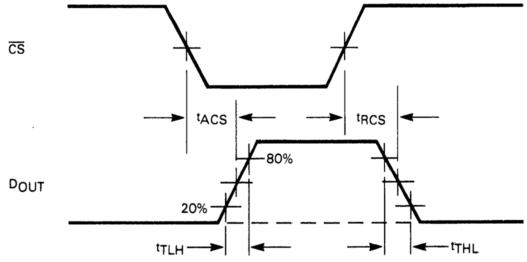
ADDRESS INPUT TO DATA OUTPUT ($\overline{WE}$ = HIGH, $\overline{CS}$ = LOW)

ADDRESS ACCESS TIME



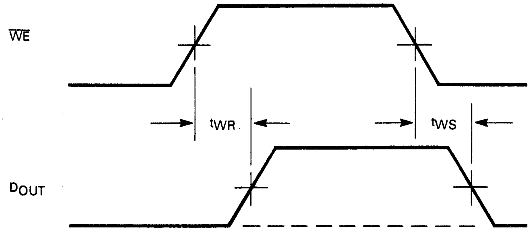
CHIP SELECT INPUT TO DATA OUTPUT ($\overline{WE}$ = HIGH)

CHIP SELECT ACCESS AND RECOVERY TIMES



WRITE ENABLE INPUT TO DATA OUTPUT ($\overline{CS}$ = LOW)

WRITE RECOVERY, DISABLE TIMES



ECL ISOPLANAR MEMORY F10405

128×1-BIT FULLY DECODED RANDOM ACCESS MEMORY

FAIRCHILD VOLTAGE COMPENSATED ECL

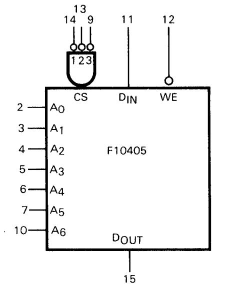
GENERAL DESCRIPTION – The F10405 is a 128-bit Read/Write Random Access Memory, organized 128 words by one bit. It has typical access time of 12 ns and is designed for high speed scratch pad, control and buffer storage applications. It is fully compatible with F10K voltage compensated ECL and is usable with fully compensated F95K ECL and uncompensated 10,000 ECL.

The F10405 has full address decoding on chip, separate Data In and non-inverted Data Out lines and three active LOW Chip Select lines.

The F10405 is packaged in the hermetic ceramic 16-pin dual in-line package and specified for operation over the temperature range 0°C to 75°C.

- **FULLY COMPATIBLE WITH F10K ECL**
- **READ ACCESS TIME – 12 ns TYP**
- **50 kΩ INPUT PULL DOWN RESISTORS ON CHIP SELECT**
- **USABLE WITH F95K AND UNCOMPENSATED 10,000 ECL**
- **OUTPUTS CAN BE WIRED-OR FOR EASY MEMORY EXPANSION**
- **CHIP SELECT ACCESS TIME – 5 ns TYP**

LOGIC SYMBOL

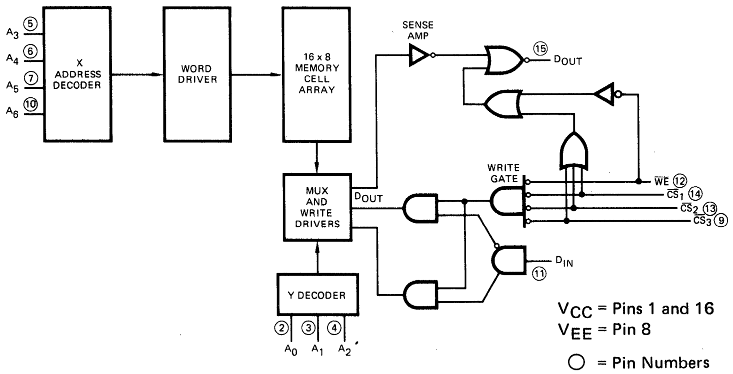


V_{CC} = GND (Pins 1 and 16)
V_{EE} = −5.2 V(Pin 8)

PIN NAMES

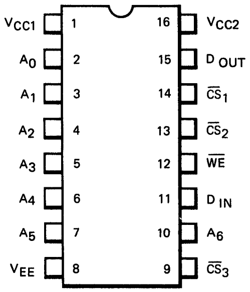
$\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$	Chip Select Inputs
A_n	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input

LOGIC DIAGRAM



V_{CC} = Pins 1 and 16
V_{EE} = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



FUNCTIONAL DESCRIPTION — The F10405 is a fully decoded read/write random access ECL memory, organized 128 words by one bit. The desired word is selected by a 7-bit address (A0 to A6).

The Chip Selects and Write Enable are active LOW. Three Chip Selects are provided for memory expansion. This permits memory array expansion up to 1024 words with the 9538 decoder. For larger memories, the third Chip Select line permits the decoding of Chip Select, $\overline{CS}$, from the address without affecting system performance.

The read and write operations are controlled by the state of the active LOW Write Enable, $\overline{WE}$ (pin 12). With $\overline{WE}$ held LOW, and the chip selected, the data at D_{IN} is written into the addressed location. To Read, $\overline{WE}$ is held HIGH, and the chip is selected. Data in the addressed location is presented at D_{OUT} and is read out non-inverted. The D_{OUT} is LOW except when reading a stored HIGH.

Open emitter outputs are provided on the F10405 to allow maximum flexibility in output wired-OR connections for memory expansion.

A write operation may be performed with the write pulse applied to one of the Chip Select inputs. The two other Chip Selects and the Write Enable must be LOW.

TABLE 1 — TRUTH TABLE

INPUT					OUTPUT	MODE
$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_3$	$\overline{WE}$	D_{IN}		
X	X	H*	X	X	L	NOT SELECTED
L	L	L	L	L	L	WRITE "0"
L	L	L	L	H	L	WRITE "1"
L	L	L	H	X	D_{OUT}	READ

L = LOW Voltage Levels = -1.7 V
H = HIGH Voltage Levels = -0.9 V
(Nominal values)
X = Don't Care
*One or more Chip Selects HIGH

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{EE} Pin Potential to Ground Pin	-7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	-30 mA to +0.1 mA

GUARANTEED OPERATING RANGES

SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE
MIN	TYP	MAX	Note 4
−5.46 V	−5.2 V	−4.94 V	0°C to +75°C

DC CHARACTERISTICS: V_{EE} = −5.2 V, V_{CC} = GND (Notes 1-4)

SYMBOL	CHARACTERISTIC	LIMITS (Note 6)			UNITS	CONDITIONS		
		B	TYP	A				
V_{OH}	Output Voltage HIGH	−1000		−840	mV	0°C	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to −2.0 V
		−960		−810		+25°C		
		−900		−720		+75°C		
V_{OL}	Output Voltage LOW	−1870		−1665	mV	0°C		
		−1850		−1650		+25°C		
		−1830		−1625		+75°C		
V_{OHC}	Output Voltage HIGH	−1020			mV	0°C	$V_{IN} = V_{IHB}$ or V_{ILA}	
		−980				+25°C		
		−920				+75°C		
V_{OLC}	Output Voltage LOW			−1645	mV	0°C		
				−1630		+25°C		
				−1605		+75°C		
V_{IH}	Input Voltage HIGH	−1145		−840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs	
		−1105		−810		+25°C		
		−1045		−720		+75°C		
V_{IL}	Input Voltage LOW	−1870		−1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs	
		−1850		−1475		+25°C		
		−1830		−1450		+75°C		
I_{IH}	Input Current HIGH			200	µA	0 to +75°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW (Chip Selects)	0.5		160	µA	+25°C	$V_{IN} = V_{ILB}$	
I_{EE}	Power Supply Current		−90		mA	+25°C	Inputs and Output Open	

AC CHARACTERISTICS: $V_{EE} = -5.2V \pm 5\%$, Output Load = 50 Ω, 10 pF to −2.0 V, $T_A = 0^\circ C$ to $+75^\circ C$ (Note 4)

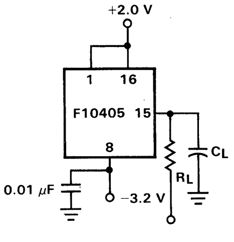
SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN	TYP Note 3	MAX			
READ MODE							
t_{ACS}	Chip Select Access Time		5	8	ns	Fig. 1a & b Measured at 50% of Input to 50% of Output	
t_{RCS}	Chip Select Recovery Time		5	8	ns		
t_{AA}	Address Access Time (Note 5)		12	15	ns		
WRITE MODE							
t_W	Write Pulse Width	8	6		ns	t_{WSA} = 4 ns	
t_{WSD}	Data Set-up Time Prior to Write	4	3		ns		
t_{WHD}	Data Hold Time After Write	3	0		ns		Fig. 2 Measured at 50% of Input to Valid Output
t_{WSA}	Address Set-up Time	4	3		ns	t_W = 8 ns	
t_{WHA}	Address Hold Time	3	2		ns		
t_{WSCS}	Chip Select Set-up Time	4	3		ns		
t_{WHCS}	Chip Select Hold Time	3	2		ns		
t_{WS}	Write Disable Time		6	9	ns		
t_{WR}	Write Recovery Time		6	10	ns		
RISE AND FALL TIME							
t_r	Output Rise Time		3		ns	Measured between 20% & 80% points. (Fig. 1a)	
t_f	Output Fall Time		3		ns		
CAPACITANCE							
C_{IN}	Input Lead Capacitance		4	5	pF		
C_{OUT}	Output Lead Capacitance		7	8	pF		

NOTES:

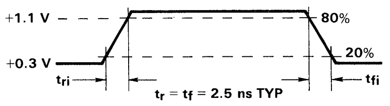
1. Conditions for testing not shown in the tables are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at $V_{EE} = -5.2$ V, $+25^\circ$C, and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F. P. M. and a two minute warm-up period.
   Thermal resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F. P. M. air flow)
   θ_{JC} (Junction to Case) = 25°C/Watt
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
6. DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET.
   The symbols and terms used in this data sheet have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are:
   "A" the value closest to positive infinity.
   "B" the value closest to negative infinity.

AC TEST LOAD AND WAVEFORM

LOADING CONDITIONS



INPUT LEVELS



All Timing Measurements Referenced to 50% of Input Levels
C_L = 10 pF including Jig and Stray Capacitance
R_L = 50 Ω to −2.0 V

READ MODE PROPAGATION DELAY FROM CHIP SELECT

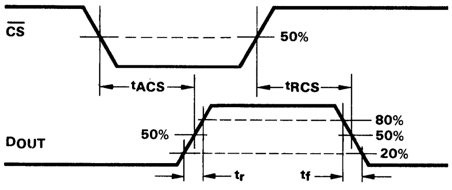


Fig. 1a

READ MODE PROPAGATION DELAY FROM ADDRESS

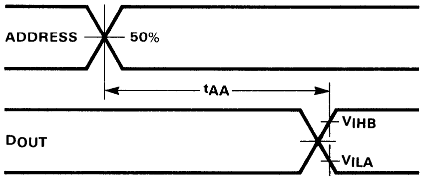


Fig. 1b

WRITE MODE

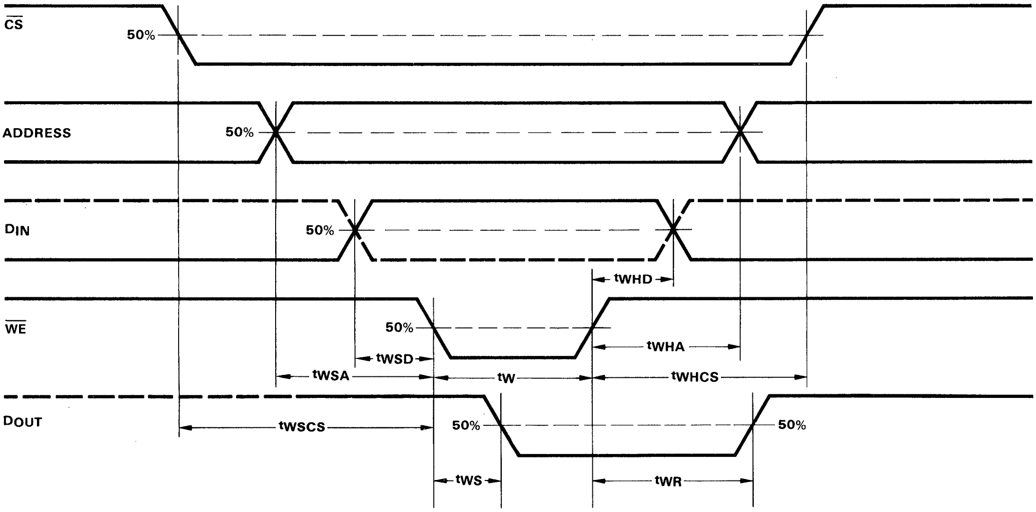


Fig. 2

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

ECL ISOPLANAR MEMORY F10410

256×1-BIT FULLY DECODED RANDOM ACCESS MEMORY

FAIRCHILD VOLTAGE COMPENSATED ECL

GENERAL DESCRIPTION - The F10410 is a 256-bit Read/Write Random Access Memory, organized 256 words by one bit. It has typical access time of 18 ns and is designed for high speed scratch pad, control and buffer storage applications. The device includes full address decoding on the chip, has separate Data In and non-inverted Data Out lines, and has three active LOW Chip Select lines.

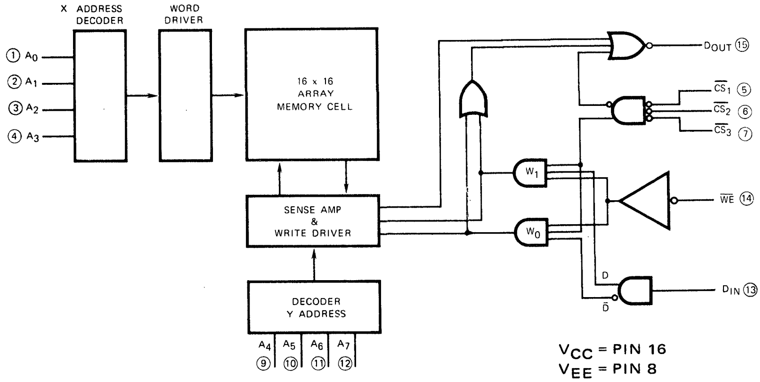
The F10410 is compatible with the F10K and uncompensated 10K ECL families and includes on-chip voltage compensation for improved noise margin. The device is packaged in the hermetic ceramic 16-pin dual in-line package and specified for operation over the temperature range 0°C to 75°C.

- **COMPATIBLE WITH F10K AND UNCOMPENSATED ECL LOGIC**
- **READ ACCESS TIME – 18 ns TYP**
- **CHIP SELECT ACCESS TIME – 7 ns TYP**
- **POWER DISSIPATION – 1.8 mW/BIT**
- **50 kΩ INPUT PULL-DOWN RESISTORS ON CHIP SELECT**
- **OUTPUTS CAN BE WIRED-OR FOR EASY MEMORY EXPANSION**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**
- **ORGANIZED – 256 WORDS X 1 BIT**

PIN NAMES

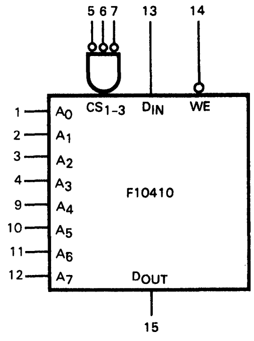
$\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$	Chip Select Inputs
A_0 - A_7	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input

LOGIC DIAGRAM



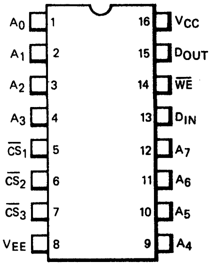
V_{CC} = PIN 16
V_{EE} = PIN 8
○ = PIN NUMBERS

LOGIC SYMBOL



V_{CC} = PIN 16
V_{EE} = PIN 8

CONNECTION DIAGRAM
DIP(TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The F10410 is a fully decoded 256-bit Read/Write Random Access Memory, organized 256 words by one bit. Word selection is achieved by means of an 8-bit address A_0 to A_7.

The active LOW Chip Select inputs are provided for increased logic flexibility. This permits memory array expansion up to 2048 words with the 10161 decoder. For larger memories, the fast chip select time permits the decoding of Chip Select, $\overline{CS}$, from the address without affecting system performance.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$, pin 14). With $\overline{WE}$ held LOW, and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH, and the chip selected. Data in the addressed location is presented at D_{OUT} and is read out non-inverted. The D_{OUT} is LOW except when reading a stored HIGH.

Open emitter outputs are provided on the F10410 to allow maximum flexibility in output wired-OR connection for memory expansion.

TABLE 1 – TRUTH TABLE

INPUT					OUTPUT	MODE
$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_3$	$\overline{WE}$	D_{IN}		
X	X	H*	X	X	L	NOT SELECTED
L	L	L	L	L	L	WRITE "0"
L	L	L	L	H	L	WRITE "1"
L	L	L	H	X	D_{OUT}	READ

*One or more Chip Selects HIGH

NOTE:
L = LOW Voltage Levels = –1.7 V
H = HIGH Voltage Levels = –0.9 V
(Nominal Values)
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to 150°C
Temperature (Ambient) Under Bias	–55°C to 125°C
V_{EE} Pin Potential to Ground Pin	–7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	–30 mA to +0.1 mA

GUARANTEED OPERATING RANGES

SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE
MIN	TYP	MAX	Note 4
-5.46 V	-5.2 V	-4.94 V	0°C to 75°C

DC CHARACTERISTICS: V_{EE} = -5.2 V, Output Load = 50 Ω to -2.0 V, T_A = 0°C to 75°C (Note 4)

SYMBOL	CHARACTERISTIC	B LIMIT	TYP (Note 3)	A LIMIT	UNITS	CONDITIONS		
V_{OH}	Output HIGH Voltage	-1000		–840	mV	0°C	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to –2.0 V
		-960		–810		+25°C		
		-900		–720		+75°C		
V_{OL}	Output LOW Voltage	-1870		-1665	mV	0°C		
		-1850		-1650		+25°C		
		-1830		-1625		+75°C		
V_{OHC}	Output HIGH Voltage	-1020			mV	0°C	$V_{IN} = V_{IHB}$ or V_{ILA}	
		-980				+25°C		
		-920				+75°C		
V_{OLC}	Output LOW Voltage			-1645	mV	0°C		
				-1630		+25°C		
				-1605		+75°C		
V_{IH}	Input HIGH Voltage	-1145		-840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs	
		-1105		-810		+25°C		
		-1045		-720		+75°C		
V_{IL}	Input LOW Voltage	-1870		-1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs	
		-1850		-1475		+25°C		
		-1830		-1450		+75°C		
I_{IH}	Input HIGH Current			220	µA	0 to +75°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input LOW Current ($\overline{CS}$)	0.5		170	µA	+25°C	$V_{IN} = V_{ILB}$	
	All Others	–50						
I_{EE}	Power Supply Current (Pin 8)		-85		mA	+75°C	All Inputs and Outputs Open	
		–130	-95		mA	0°C		

AC CHARACTERISTICS: V_{EE} = −5.2 V ±5%, Output Load = 50 Ω, 30 pF to −2.0 V, T_A = 0°C to 75°C (Note 4)

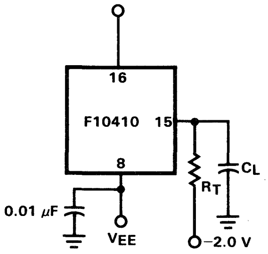
SYMBOL	PARAMETER	MIN LIMIT	TYP (Note 3)	MAX LIMIT	UNITS	CONDITIONS
READ MODE						
t_{ACS}	Chip Select Access Time		7	12	ns	Fig. 1a & b Measured at 50% of Input to Valid Output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH}). Note 5.
t_{RCS}	Chip Select Recovery Time		7	12	ns	
t_{AA}	Address Access Time		18	30	ns	
WRITE MODE						
t_W	Write Pulse Width	25	15		ns	t_{WSA} = 8 ns
t_{WSD}	Data Set-up Time Prior to Write	5	3		ns	
t_{WHD}	Data Hold Time After Write	5	3		ns	
t_{WSA}	Address Set-up Time	8	5		ns	t_W = 25 ns Fig. 2 Measured at 50% of Input to Valid Output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})
t_{WHA}	Address Hold Time	5	0		ns	
t_{WSCS}	Chip Select Set-up Time	5	3		ns	
t_{WHCS}	Chip Select Hold Time	5	3		ns	
t_{WS}	Write Disable Time	3	7		ns	
t_{WR}	Write Recovery Time		8	20	ns	
RISE AND FALL TIME						
t_r	Output Rise Time		5		ns	Measured between 20% & 80% points. (Fig. 1a)
t_f	Output Fall Time		5		ns	
CAPACITANCE						
C_{IN}	Input Lead Capacitance		4	5	pF	Measure with a Pulse Technique
C_{OUT}	Output Lead Capacitance		7	8	pF	

NOTES:

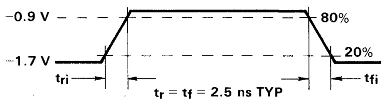
1. Conditions for testing, not shown in the tables are chosen to guarantee operation under "worst case" conditions.
2. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{EE} = −5.2 V, T_A = +25°C and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and two minute warm up period. Typical thermal resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   θ_{JC} (Junction to Case) = 25°C/Watt
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
6. DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET:
   The symbols and terms used in this data sheet have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are:
   "A" the value closest to positive infinity.
   "B" the value closest to negative infinity.

AC TEST LOAD AND WAVEFORMS

LOADING CONDITIONS



INPUT LEVELS



All Timing Measurements Referenced to 50% of Input Levels
C_L = 30 pF including Jig and Stray Capacitance
R_L = 50 Ω to −2.0 V

READ MODE PROPAGATION DELAY FROM CHIP SELECT

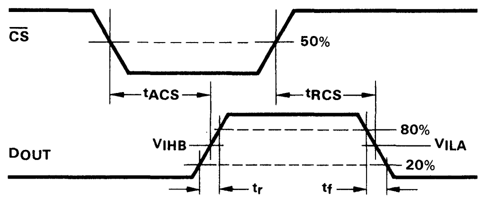


Fig. 1a

READ MODE PROPAGATION DELAY FROM ADDRESS

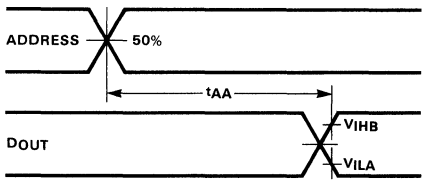


Fig. 1b

WRITE MODE

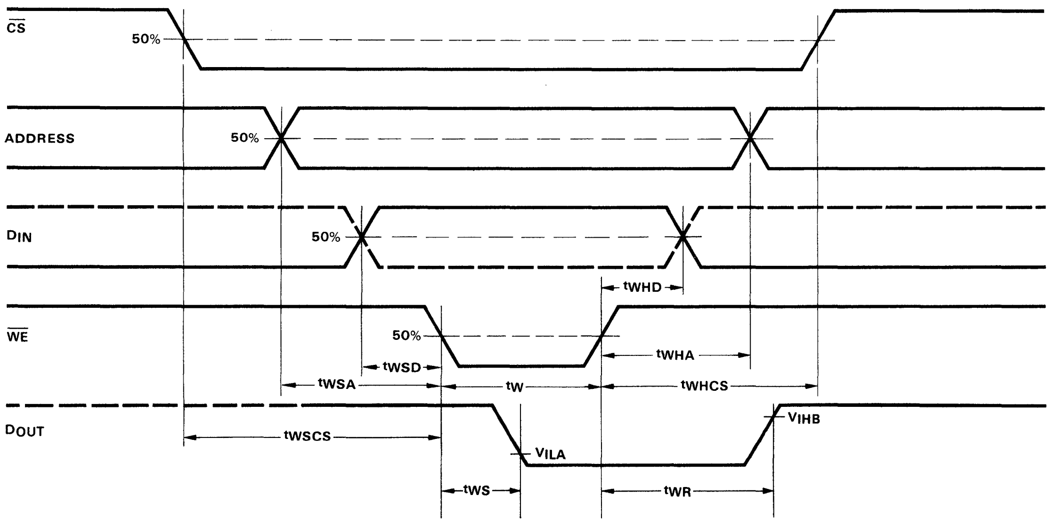


Fig. 2

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

4096 WORD X N–BIT SYSTEM

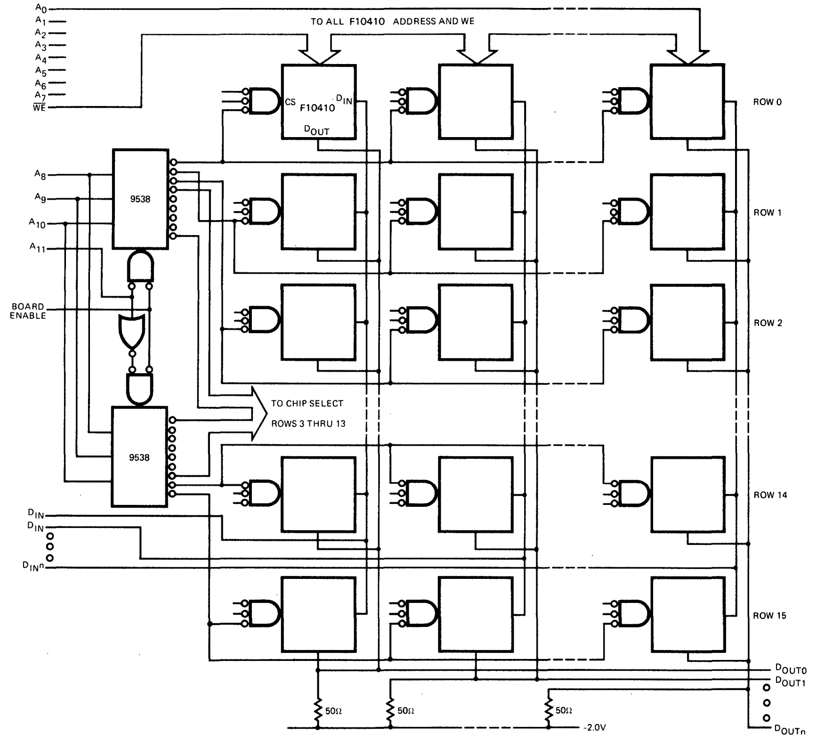


Fig. 3.

ECL ISOPLANAR MEMORY F10411

256×1–BIT FULLY DECODED RANDOM ACCESS MEMORY

FAIRCHILD VOLTAGE COMPENSATED ECL

GENERAL DESCRIPTION – The F10411 is a low voltage 256-bit Read/Write Random Access Memory, organized 256 words by one bit. It has a 20 ns typical access time and is designed for high speed scratchpad, control and buffer storage applications. The device includes full address decoding on the chip, has separate Data In and non-inverted Data Out lines, and has three active LOW Chip Select lines.

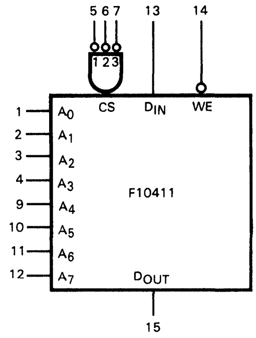
The F10411 is compatible with the F10K and uncompensated 10K ECL families and includes on-chip voltage compensation for improved noise margin. The device is packaged in the hermetic ceramic 16-pin dual in-line package and specified for operation over the temperature range 0°C to 75°C.

- **OPERATES WITH REDUCED POWER SUPPLY VOLTAGE**
- **READ ACCESS TIME – 20 ns TYP**
- **CHIP SELECT ACCESS TIME – 7 ns TYP**
- **POWER DISSIPATION – 1.4 mW/BIT TYP**
- **50 kΩ INPUT PULL-DOWN RESISTORS ON CHIP SELECT**
- **OUTPUTS CAN BE WIRED-OR FOR EASY MEMORY EXPANSION**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**
- **ORGANIZED 256 WORDS X 1 BIT**

PIN NAMES

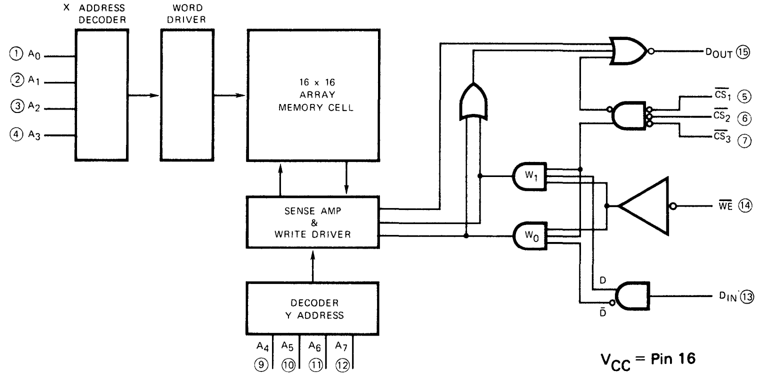
$\overline{CS}_1$ – $\overline{CS}_3$	Chip Select Inputs
A_0 – A_7	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input

LOGIC SYMBOL



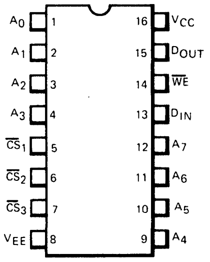
V_{CC} = 16
V_{EE} = 8

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



FUNCTIONAL DESCRIPTION – The F10411 is a fully decoded 256-bit Read/Write Random Access Memory, organized 256 words by one bit. Word selection is achieved by means of an 8-bit address, A_0 thru A_7.

The active LOW Chip Select inputs are provided for increased logic flexibility. This permits memory array expansion up to 2048 words with the 10161 decoder. For larger memories, the fast chip select time permits the decoding of Chip Select, $\overline{CS}$, from the address without affecting system performance.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$, pin 14). With $\overline{WE}$ held LOW, and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH, and the chip selected. Data in the addressed location is presented at D_{OUT} and is read out non-inverted. The D_{OUT} is LOW except when reading a stored HIGH.

Open emitter outputs are provided on the F10411 to allow maximum flexibility in output wired-OR connection for memory expansion.

TABLE I – TRUTH TABLE

INPUTS					OUTPUT	MODE
$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_3$	$\overline{WE}$	D_{IN}		
X	X	H*	X	X	L	Not Selected
L	L	L	L	L	L	Write "0"
L	L	L	L	H	L	Write "1"
L	L	L	H	X	D_{OUT}	Read

L = LOW Voltage Levels = −1.7 V
H = HIGH Voltage Levels = −0.9 V
(Nominal values)
X = Don't Care
*One or more Chip Selects HIGH

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to 150°C
Temperature (Ambient) Under Bias	−55°C to 125°C
V_{EE} Pin Potential to Ground Pin	−7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	−30 mA to +0.1 mA

GUARANTEED OPERATING RANGES

SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE
MIN	TYP	MAX	Note 4
−4.46 V	−4.25 V	−4.04 V	0°C to 75°C

DC CHARACTERISTICS: V_{EE} = −4.25 V, Output Load = 50 Ω to −2.0 V, T_A = 0°C to 75°C (Note 4)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS	
		B LIMIT	TYP (Note 3)	A LIMIT				
V_{OH}	Output HIGH Voltage	−1000 −960 −900		−840 −810 −720	mV	0°C +25°C +75°C	V_{IN} = V_{IHA} or V_{ILB}	Loading is 50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1870 −1850 −1830		−1605 −1590 −1565	mV	0°C +25°C +75°C		
V_{OHC}	Output HIGH Voltage	−1020 −980 −920			mV	0°C +25°C +75°C	V_{IN} = V_{IHB} or V_{ILA}	
V_{OLC}	Output LOW Voltage			−1585 −1570 −1545	mV	0°C +25°C +75°C		
V_{IH}	Input HIGH Voltage	−1045 −1025 −1000		−735 −705 −615	mV	0°C +25°C +75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input LOW Voltage	−1870 −1850 −1830		−1490 −1475 −1450	mV	0°C +25°C +75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input HIGH Current			200	μA	0 to +75°C	V_{IN} = V_{IHA}	
I_{IL}	Input LOW Current (CS) All Others	0.5 −50		150	μA	+25°C	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current (Pin 8)	 −125	−80 −90		mA mA	+75°C 0°C	All Inputs and Outputs Open	

AC CHARACTERISTICS: V_{EE} = −4.25 V ±5%, Output Load = 50 Ω, 30 pF to −2.0 V, T_A = 0°C to 75°C (Note 4)

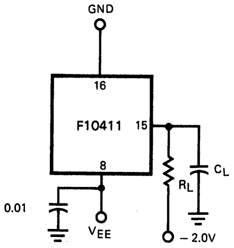
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		MIN LIMIT	TYP (Note 3)	MAX LIMIT			
READ MODE							
t_{ACS}	Chip Select Access Time		7	12	ns		Fig. 1a and b Measured at 50% of Input to Valid Output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH}). Note 5.
t_{RCS}	Chip Select Recovery Time		7	12	ns		
t_{AA}	Address Access Time		20	35	ns		
WRITE MODE							
t_W	Write Pulse Width	30	20		ns	t_{WSA} = 10 ns	
t_{WSD}	Data Set-Up Time Prior to Write	7	3		ns		
t_{WHD}	Data Hold Time After Write	7	3		ns		
t_{WSA}	Address Set-Up Time	10	6		ns	t_W = 30 ns	Fig. 2 Measured at 50% of Input to Valid Output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})
t_{WHA}	Address Hold Time	5	0		ns		
t_{WSCS}	Chip Select Set-Up Time	5	3		ns		
t_{WHCS}	Chip Select Hold Time	5	3		ns		
t_{WS}	Write Disable Time	3	7		ns		
t_{WR}	Write Recovery Time		9	20	ns		
RISE AND FALL TIME							
t_r	Output Rise Time		5		ns		Measured between 20% and 80% points. (Fig. 1a)
t_f	Output Fall Time		5		ns		
CAPACITANCE							
C_{IN}	Input Load Capacitance		4	5	pF		Measure with a Pulse Technique
C_{OUT}	Output Load Capacitance		7	8	pF		

NOTES:

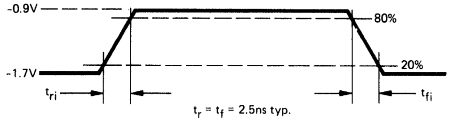
1. Conditions for testing, not shown in the tables are chosen to guarantee operation under "worst case" conditions.
2. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at $V_{EE} = -4.25$ V, $T_A = +25°C$ and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and a two minute warm-up period. Typical thermal resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C / Watt (still air)
   θ_{JA} (Junction to Ambient) = 50°C / Watt (at 400 F.P.M. air flow)
   θ_{JC} (Junction to Case) = 25°C / Watt
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
6. DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET.
   The symbols and terms used in this data sheet have been chosen to agree with the lateststandards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are:
   "A" the value closest to positive infinity.
   "B" the value closest to negative infinity.

AC TEST LOAD AND WAVEFORMS

LOADING CONDITIONS



INPUT LEVELS



All Timing Measurements Referenced to 50% of Input Levels
C_L = 30 pF including Jig and Stray Capacitance
R_L = 50 Ω to −2.0 V

READ MODE PROPAGATION DELAY FROM CHIP SELECT

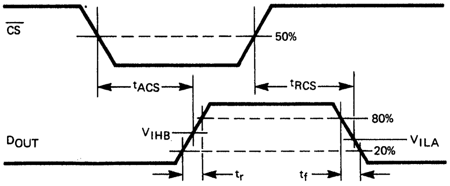


Fig. 1a

READ MODE PROPAGATION DELAY FROM ADDRESS

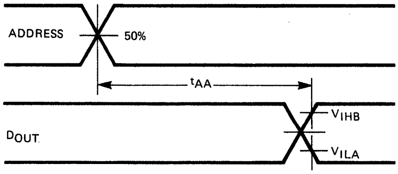


Fig. 1b

WRITE MODE

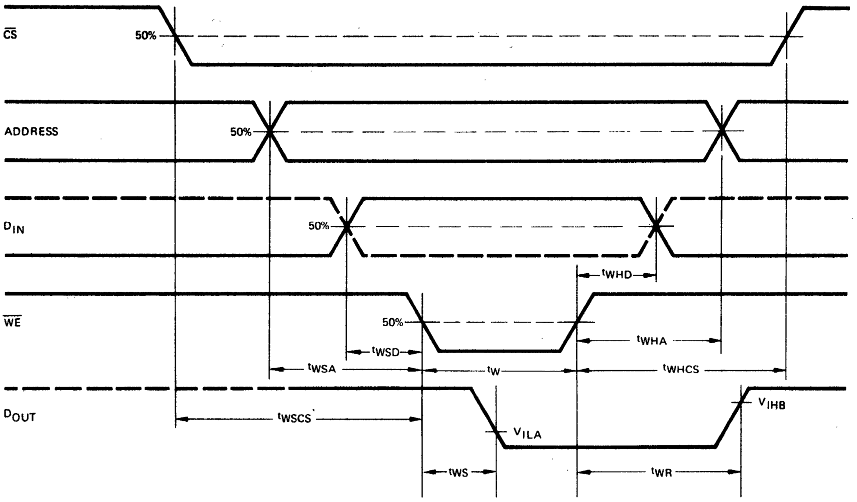


Fig. 2

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

4096-WORD X N-BIT SYSTEM

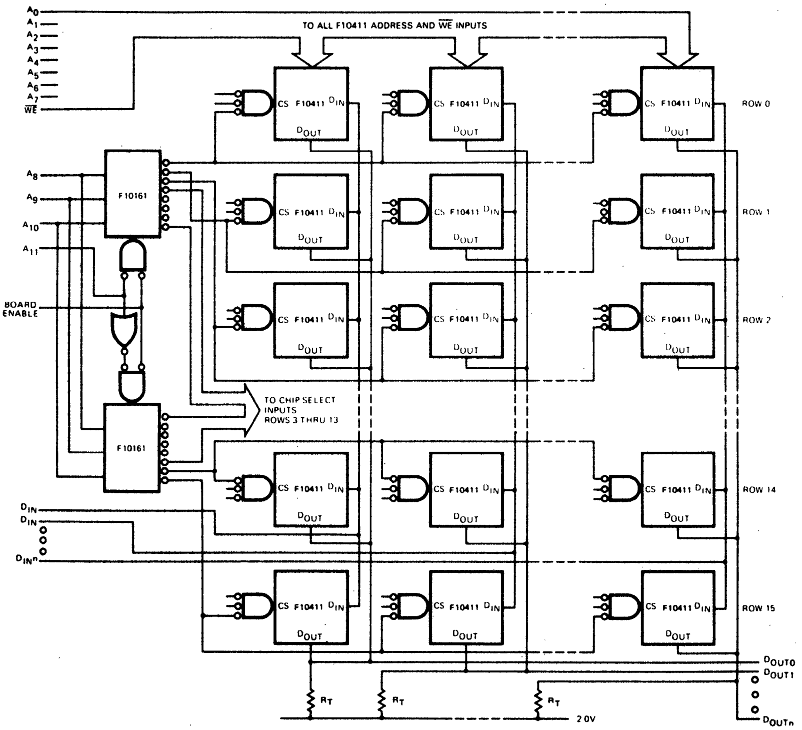


Fig. 3

ECL ISOPLANAR MEMORY F10414

256 × 1-BIT FULLY DECODED RANDOM ACCESS MEMORY

FAIRCHILD VOLTAGE COMPENSATED ECL

GENERAL DESCRIPTION – The F10414 is a 256-bit Read/Write random access Memory, organized 256 words by one bit. It has typical access time of 7 ns and is designed for high speed scratch pad, control and buffer storage applications. The device includes full address decoding on the chip, has separate Data In and non-inverted Data Out lines, and has three active LOW Chip Select lines.

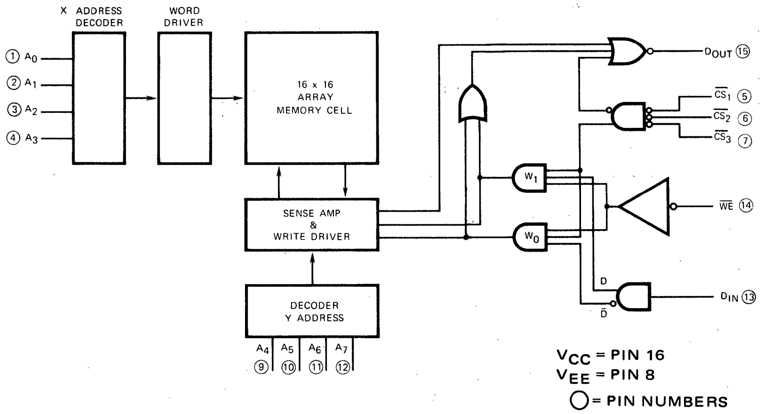
The F10414 is compatible with the F10K and uncompensated 10K ECL families and includes on-chip voltage compensation for imporved noise margin. The device is packaged in the hermetic ceramic 16-pin dual in-line package and specified for operation over the temperature range 0°C to 75°C.

- **VERY HIGH SPEED**
- **COMPATIBLE WITH F10K AND UNCOMPENSATED ECL LOGIC**
- **READ ACCESS TIME – 7 ns TYPICAL**
- **CHIP SELECT ACCESS TIME – 4 ns TYPICAL**
- **POWER DISSIPATION – 1.8 mW/BIT**
- **50 kΩ INPUT PULL-DOWN RESISTORS ON CHIP SELECT**
- **OUTPUTS CAN BE WIRED-OR FOR EASY MEMORY EXPANSION**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**
- **ORGANIZED – 256 WORDS X 1 BIT**

PIN NAMES

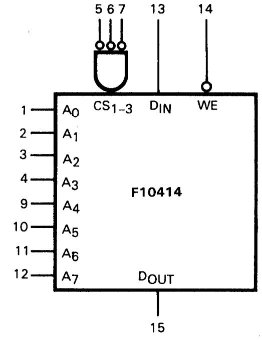
$\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$	Chip Select Inputs
A_0 - A_7	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input

LOGIC DIAGRAM



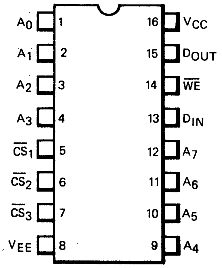
V_{CC} = PIN 16
V_{EE} = PIN 8
○ = PIN NUMBERS

LOGIC SYMBOL



V_{CC} = PIN 16
V_{EE} = PIN 8

CONNECTION DIAGRAM DIP(TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The F10414 is a fully decoded 256-bit Read/Write Random Access Memory, organized 256 words by one bit. Word selection is achieved by means of an 8-bit address A_0 to A_7.

The active LOW chip select inputs are provided for increased logic flexibility. This permits memory array expansion up to 2048 words with the 10161 decoder. For larger memories, the fast chip select time permits the decoding of Chip Select, CS, from the address without affecting system performance.

The read and write operations are controlled by the state of the active LOW Write Enable, ($\overline{WE}$, pin 14). With $\overline{WE}$ held LOW, and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH, and the chip selected. Data in the addressed location is presented at D_{OUT} and is read out non-inverted. The D_{OUT} is LOW except when reading a stored HIGH.

Open emitter outputs are provided on the F10414 to allow maximum flexibility in output wired-OR connection for memory expansion.

TABLE 1 – TRUTH TABLE

INPUT					OUTPUT	MODE
$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_3$	$\overline{WE}$	D_{IN}		
X	X	H*	X	X	L	NOT SELECTED
L	L	L	L	L	L	WRITE "0"
L	L	L	L	H	L	WRITE "1"
L	L	L	H	X	D_{OUT}	READ

*One or more Chip Selects HIGH

NOTE:
L = LOW Voltage Levels = –1.7 V
H = HIGH Voltage Levels = –0.9 V
(Nominal Values)
X = Don't Care

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to 150°C
Temperature (Ambient) Under Bias	–55°C to 125°C
V_{EE} Pin Potential to Ground Pin	–7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	–30 mA to +0.1 mA

GUARANTEED OPERATING RANGES

SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE
MIN	TYP	MAX	Note 4
–5.46 V	–5.2 V	–4.94 V	0°C to 75°C

DC CHARACTERISTICS: V_{EE} = –5.2 V, Output Load = 50 Ω to –2.0 V, T_A = 0°C to 75°C (Note 4)

SYMBOL	CHARACTERISTIC	B LIMIT	TYP (Note 3)	A LIMIT	UNITS	CONDITIONS		
V_{OH}	Output HIGH Voltage	–1000		–840	mV	0°C	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to –2.0 V
		–960		–810		+25°C		
		–900		–720		+75°C		
V_{OL}	Output LOW Voltage	–1870		–1665	mV	0°C		
		–1850		–1650		+25°C		
		–1830		–1625		+75°C		
V_{OHC}	Output HIGH Voltage	–1020			mV	0°C	$V_{IN} = V_{IHB}$ or V_{ILA}	
		–980				+25°C		
		–920				+75°C		
V_{OLC}	Output LOW Voltage			–1645	mV	0°C		
				–1630		+25°C		
				–1605		+75°C		
V_{IH}	Input HIGH Voltage	–1145		–840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs	
		–1105		–810		+25°C		
		–1045		–720		+75°C		
V_{IL}	Input LOW Voltage	–1870		–1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs	
		–1850		–1475		+25°C		
		–1830		–1450		+75°C		
I_{IH}	Input HIGH Current			220	µA	0 to +75°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input LOW Current ($\overline{CS}$)	0.5		170	µA	+25°C	$V_{IN} = V_{ILB}$	
	All Others	–50						
I_{EE}	Power Supply Current (Pin 8)		–90		mA	+75°C	All Inputs and Outputs Open	
			–100		mA	0°C		

AC CHARACTERISTICS: V_{EE} = −5.2 V ±5%, Output Load = 50 Ω, 10 pF to −2.0 V, T_A = 0°C to 75°C (Note 4)

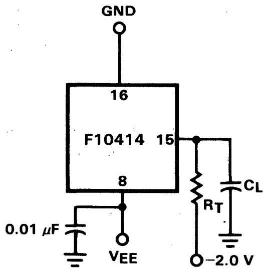
SYMBOL	PARAMETER	MIN LIMIT	TYP (Note 3)	MAX LIMIT	UNITS	CONDITIONS
READ MODE						
t_{ACS}	Chip Select Access Time		4		ns	Fig. 1a & b Measured at 50% of Input to Valid Output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH}). Note 5.
t_{RCS}	Chip Select Recovery Time		4		ns	
t_{AA}	Address Access Time		7		ns	
WRITE MODE						
t_W	Write Pulse Width	6	4		ns	t_{WSA} = 3 ns
t_{WSD}	Data Set-up Time Prior to Write		0		ns	
t_{WHD}	Data Hold Time After Write		0		ns	
t_{WSA}	Address Set-up Time		1		ns	t_W = 6 ns Fig. 2 Measured at 50% of Input to Valid Output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})
t_{WHA}	Address Hold Time		0		ns	
t_{WSCS}	Chip Select Set-up Time		0		ns	
t_{WHCS}	Chip Select Hold Time		1		ns	
t_{WS}	Write Disable Time		4		ns	
t_{WR}	Write Recovery Time		5		ns	
RISE AND FALL TIME						
t_r	Output Rise Time		4		ns	Measured between 20% & 80% points. (Fig. 1a)
t_f	Output Fall Time		4		ns	
CAPACITANCE						
C_{IN}	Input Lead Capacitance		4	5	pF	Measure with a Pulse Technique
C_{OUT}	Output Lead Capacitance		7	8	pF	

NOTES:

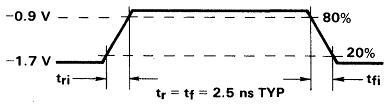
1. Conditions for testing, not shown in the tables are chosen to guarantee operation under "worst case" conditions.
2. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{EE} = −5.2 V, T_A = +25°C and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and two minute warm up period. Typical thermal resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   θ_{JC} (Junction to Case) = 25°C/Watt
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
6. DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET:
   The symbols and terms used in this data sheet have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are:
   "A" the value closest to positive infinity.
   "B" the value closest to negative infinity.

AC TEST LOAD AND WAVEFORMS

LOADING CONDITIONS



INPUT LEVELS



All Timing Measurements Referenced to 50% of Input Levels
C_L = 10 pF including Jig and Stray Capacitance
R_L = 50 Ω to −2.0 V

READ MODE PROPAGATION DELAY FROM CHIP SELECT

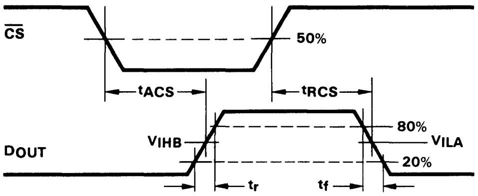


Fig. 1a

READ MODE PROPAGATION DELAY FROM ADDRESS

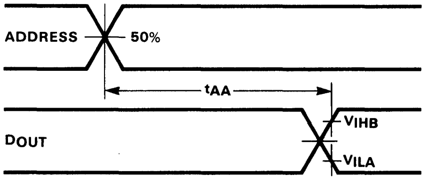


Fig. 1b

WRITE MODE

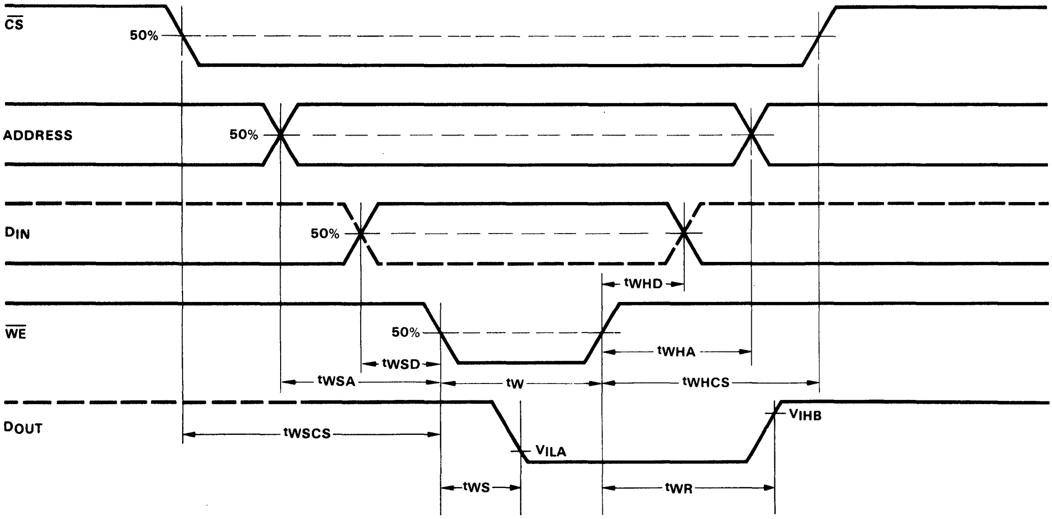


Fig. 2

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

4096 WORD X N—BIT SYSTEM

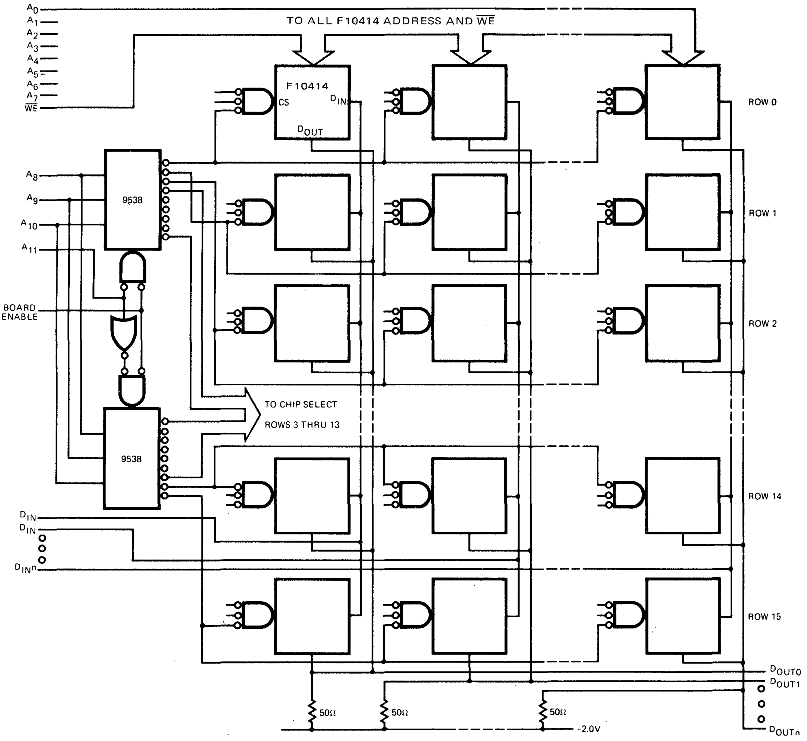


Fig. 3.

ECL ISOPLANAR MEMORY F10415 / F10415A
1024×1-BIT FULLY DECODED RANDOM ACCESS MEMORY
FAIRCHILD VOLTAGE COMPENSATED ECL

GENERAL DESCRIPTION – The F10415 and F10415A are 1024-bit Read/Write Random Access Memories organized 1024 words by one bit. They are designed for high speed scratch pad, control and buffer storage applications. Both include full address decoding on the chip, have separate Data In and non-inverted Data Out lines, and active LOW Chip Select lines. They are compatible with F10K and uncompensated 10K ECL families and include on-chip voltage compensation for improved noise margin.

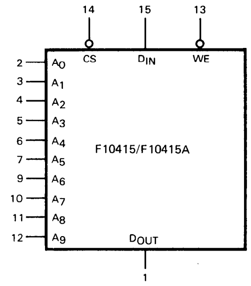
The F10415 and F10415A are packaged in a hermetic ceramic 16-pin dual in-line package and are specified for operation over the temperature range 0°C to 75°C.

- **COMPATIBLE WITH F10K AND UNCOMPENSATED 10K ECL LOGIC**
- **TYPICAL READ ACCESS TIME**
  - **F10415 – 25 ns**
  - **F10415A – 12 ns**
- **TYPICAL CHIP SELECT ACCESS TIME**
  - **F10415 – 7 ns**
  - **F10415A – 5 ns**
- **ORGANIZED 1024 WORDS X 1 BIT**
- **OPEN EMITTER OUTPUT FOR EASE OF MEMORY EXPANSION**
- **POWER DISSIPATION 0.5 mW/BIT**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**

PIN NAMES

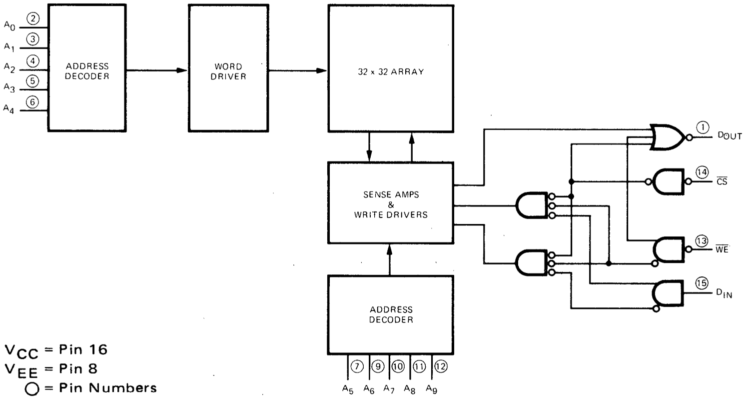
$\overline{CS}$	Chip Select Input
A_0 to A_9	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input

LOGIC SYMBOL



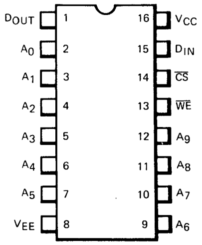
V_{CC} = Pin 16
V_{EE} = Pin 8

LOGIC DIAGRAM



V_{CC} = Pin 16
V_{EE} = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The F10415 and F10415A are fully decoded 1024-bit Read/Write Random Access Memories organized 1024 words by one bit. Bit selection is acheived by means of a 10-bit address, A_0 to A_9. One Chip Select input is provided for memory array expansion up to 2048 words without the need for external decoding. For larger memories, the fast chip select access time permits the decoding of Chip Select ($\overline{CS}$) from the address without increasing address access time. The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$). With $\overline{WE}$ and $\overline{CS}$ held LOW, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and $\overline{CS}$ held LOW. Data in the specified location is presented at D_{OUT} and is non-inverted.

An unterminated emitter-follower output is provided on the F10415 and F10415A to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many F10415s or F10415As can be tied together. In other applications the wired-OR is not used. In either case an external 50 Ω pull down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is off.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{EE} Pin Potential to Ground Pin	−7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	−30 mA to +0.1 mA

TABLE 1 – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	OPEN EMITTER	
H	X	X	L	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	L	WRITE "1"
L	H	X	D_{OUT}	READ

L = LOW Voltage Levels = −1.7 V
H = HIGH Voltage Levels = −0.9 V
(Nominal values)
X = Don't Care

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE
	MIN	TYP	MAX	See Note 4
F10415DC,F10415ADC	−5.46 V	−5.2 V	−4.94 V	0°C to 75°C

DC CHARACTERISTICS: V_{EE} = −5.2 V, Output Load = 50 Ω and 30 pF to −2.0 V, T_A = 0°C to 75°C (Note 4)

SYMBOL	CHARACTERISTIC	B LIMIT	TYP (Note 3)	A LIMIT	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	−1000		−840	mV	0°C	V_{IN} = V_{IHA} or V_{ILB}	Loading is 50 Ω to −2.0 V
		−960		−810		+25°C		
		−900		−720		+75°C		
V_{OL}	Output Voltage LOW	−1870		−1665	mV	0°C		
		−1850		−1650		+25°C		
		−1830		−1625		+75°C		
V_{OHC}	Output Voltage HIGH	−1020			mV	0°C	V_{IN} = V_{IHB} or V_{ILA}	
		−980				+25°C		
		−920				+75°C		
V_{OLC}	Output Voltage LOW			−1645	mV	0°C		
				−1630		+25°C		
				−1605		+75°C		
V_{IH}	Input Voltage HIGH	−1145		−840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs	
		−1105		−810		+25°C		
		−1045		−720		+75°C		
V_{IL}	Input Voltage LOW	−1870		−1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs	
		−1850		−1475		+25°C		
		−1830		−1450		+75°C		
I_{IH}	Input Current HIGH			220	µA	0 to +75°C	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW, $\overline{CS}$	0.5		170	µA	+25°C	V_{IN} = V_{ILB}	
	All others	−50						
I_{EE}	Power Supply Current		−90		mA	+75°C	All Inputs and Outputs Open	
	(Pin 8)	−150	−105			0°C		

NOTES:

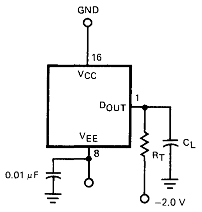
1. Conditions for testing, not shown in the tables are chosen to guarantee operation under "worst case" conditions.
2. The specified Limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{EE} = −5.2 V, T_A = 25°C and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   θ_{JC} (Junction to Case) = 25°C/Watt
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
6. DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET:
   The symbols and terms used in this data sheet have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.

AC CHARACTERISTICS: $V_{EE} = -5.2$ V ± 5%, Output Load = 50 Ω, 30 pF to −2.0 V, $T_A = 0°C$ to 75°C

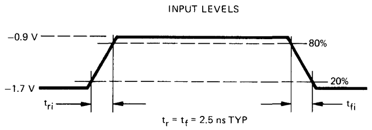
SYMBOL	PARAMETER	F10415ADC* MIN	F10415ADC* TYP (Note 3)	F10415ADC* MAX	F10415DC MIN	F10415DC TYP (Note 3)	F10415DC MAX	UNITS	CONDITIONS
READ MODE									Fig 1a & b measured at
t_{ACS}	Chip Select Access Time		5			7	10	ns	50 % of inpur to valid
t_{RCS}	Chip Select Recovery Time		5			7	10	ns	output (V_{ILA} for V_{OL}
t_{AA}	Address Access Time		12	20		25	35	ns	or V_{IHB} for V_{OH})
WRITE MODE									
t_W	Write Pulse Width (to Guarantee writing)	12	9		25	20		ns	F10415A t_{WSA} = 8 ns F10415 t_{WSA} = 20 ns
t_{WSD}	Data Set-up Time Prior to Write		0		5	0		ns	
t_{WHD}	Data Hold Time After Write		0		5	0			
t_{WSA}	Address Set-up Time Prior to Write		5		8	5		ns	F10415A t_W = 12 ns F10415 t_W = 25 ns
t_{WHA}	Address Hold Time After Write		0		4	1		ns	
t_{WSCS}	Chip Select Set-up Time Prior to Write		0		5	0		ns	Fig. 2 measured
t_{WHCS}	Chip Select Hold Time After Write		0		5	0		ns	at 50 % of input to valid output
t_{WS}	Write Disable Time		5			7	10	ns	(V_{ILA} for V_{OL} or
t_{WR}	Write Recovery Time		7			7	10	ns	V_{IHB} for V_{OH})
RISE TIME AND FALL TIME									
t_r	Output Rise Time		5			5		ns	Measured between 20 %
t_f	Output Fall Time		5			5		ns	and 80 % points. (Fig. 1a)
CAPACITANCE									
C_{IN}	Input Pin Capacitance		4	5		4	5	pF	Measure with a Pulse
C_{OUT}	Output Pin Capacitance		7	8		7	8	pF	Technique

*Note: The F10415A Ac limits are preliminary

LOADING CONDITIONS



INPUT LEVELS



All Timing Measurements Referenced to 50% of Input Levels

C_L = 30 pF including Jig and Stray Capacitance

R_T = 50 Ω Termination of Scope

READ MODE PROPAGATION DELAY FROM CHIP SELECT

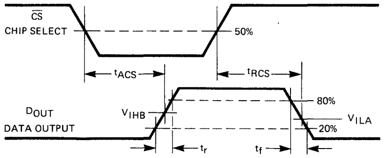


Fig. 1a

READ MODE PROPAGATION DELAY FROM ADDRESS

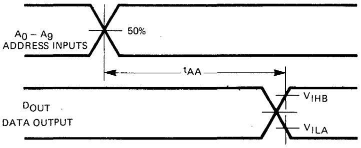


Fig. 1b

WRITE MODE

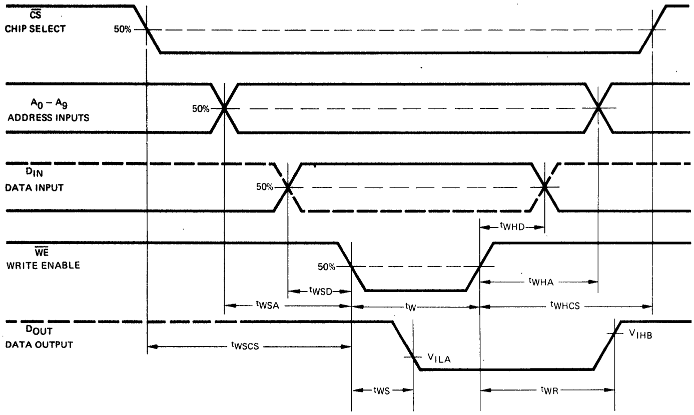
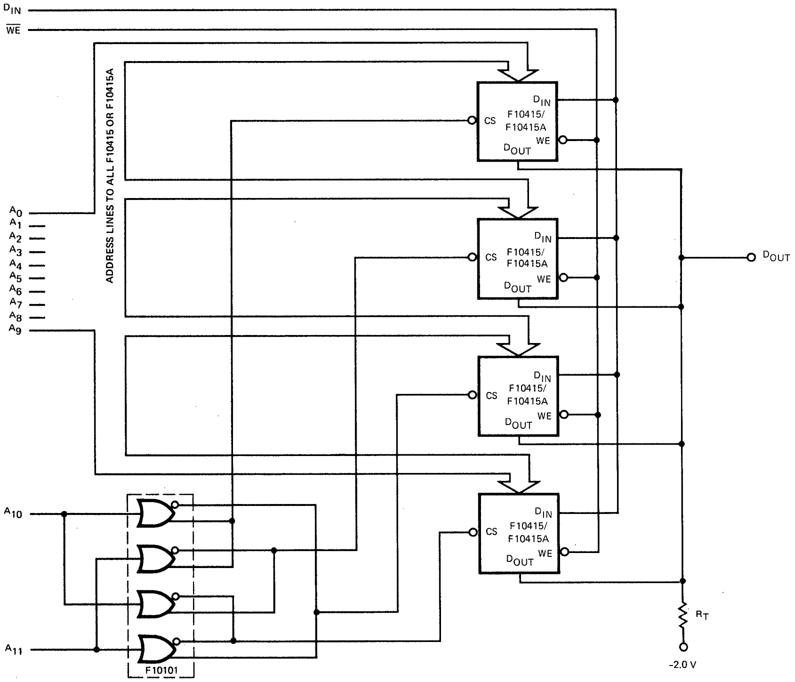


Fig. 2

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

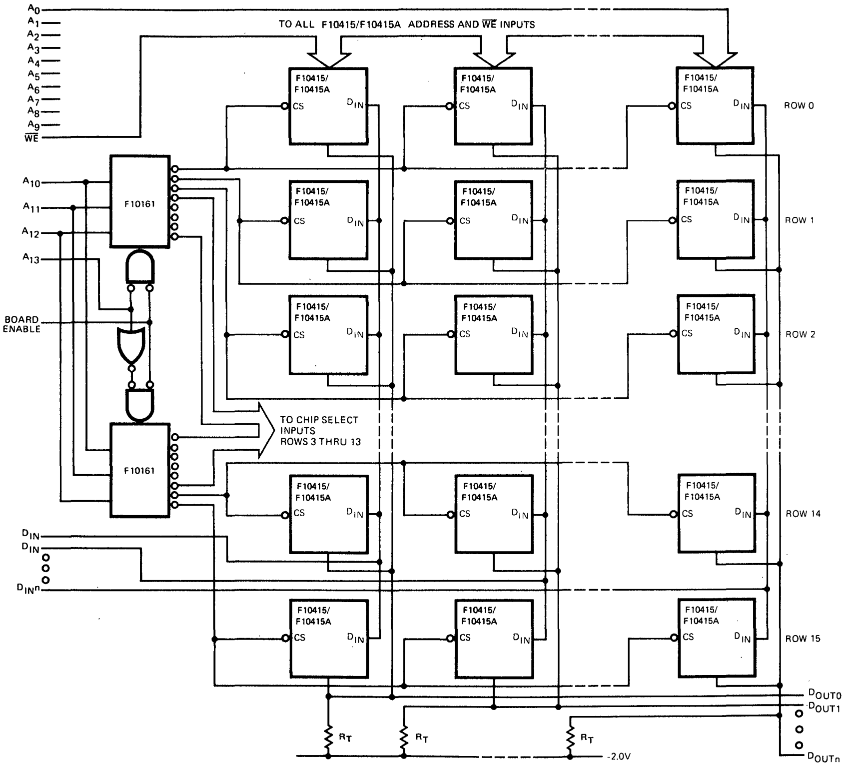
APPLICATIONS



4096-WORD X 1-BIT SYSTEM

Fig. 3

APPLICATIONS(Cont'd)



16,384-WORD X n-BIT SYSTEM
Fig. 4

F10416 / F100416

ECL ISOPLANAR MEMORY

256×4-BIT PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION – The F10416 and F100416 are fully decoded high speed 1024-bit field Programmable Read Only Memories, organized 256 words by four bits. The F10416 is voltage compensated and compatible with 10K ECL families. The 100416 is voltage and temperature compensated and compatible with the F100K family. Either device is enabled when $\overline{CS}$ is LOW. Prior to programming, all outputs are active HIGH in the enabled state. Programmed bits will furnish LOW levels at corresponding outputs. When either device is disabled ($\overline{CS}$ is HIGH) all outputs are forced LOW.

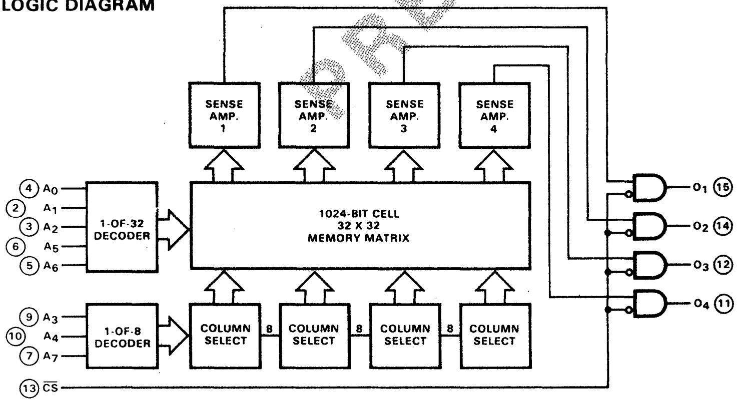
- **ADVANCED ISOPLANAR PROCESS**
- **FAST CYCLE TIME – 15 ns TYP**
- **ORGANIZATION – 256 WORDS X 4 BITS**
- **F10K AND UNCOMPENSATED 10K ECL LOGIC – F10416**
- **F100K LOGIC – F100416**
- **CHIP SELECT INPUT PROVIDES EASY MEMORY EXPANSION**
- **OPEN EMITTER OUTPUTS FOR MEMORY EXPANSION**
- **STANDARD 16-PIN DUAL IN-LINE PACKAGE**
- **FULL ADDRESS DECODING ON CHIP**

PIN NAMES

$\overline{CS}$	Chip Select Input
A_0 to A_7	Address Inputs
O_1 to O_4	Data Outputs

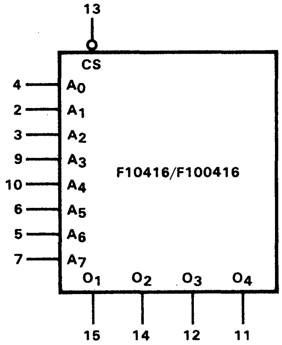
PRELIMINARY

LOGIC DIAGRAM



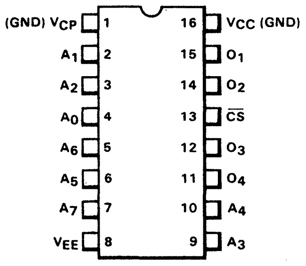
V_{CP} = GND (Read only) = Pin 1
V_{CP} = +12 V (Programming only) = Pin 1
V_{CC} = GND = Pin 16
V_{EE} = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CP} = GND (Read only) = Pin 1
V_{CP} = +12 V (Programming only) = Pin 1
V_{CC} = GND = Pin 16
V_{EE} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
V_{CP} (Pin 1) is connected to the Programmer (+12 V) during programming only.

ECL ISOPLANAR MEMORY F10470

4096 × 1-BIT FULLY DECODED RANDOM ACCESS MEMORY

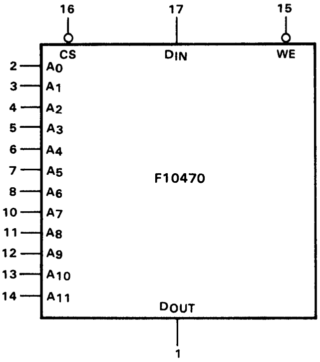
FAIRCHILD VOLTAGE COMPENSATED ECL

GENERAL DESCRIPTION – The F10470 is a 4096-bit Read/Write Random Access Memory organized 4096 words by one bit. It is designed for high speed scratch pad, control and buffer storage applications. The Device includes full address decoding on the chip, has separate Data In and non-invertered Data Out lines, and active LOW Chip Select lines. They are compatible with F10K and uncompensated 10K ECL families and include on-chip voltage compensation for improved noise margin.

The F10470 is packaged in a hermetic ceramic 18-pin dual in-line package and is specified for operation over the temperature range 0°C to 75°C.

- **COMPATIBLE WITH F10K AND UNCOMPENSATED 10K ECL LOGIC**
- **TYPICAL READ ACCESS TIME – 30 ns**
- **TYPICAL CHIP SELECT ACCESS TIME – 10 ns**
- **ORGANIZED 4096 WORDS X 1 BIT**
- **OPEN EMITTER OUTPUT FOR EASE OF MEMORY EXPANSION**
- **POWER DISSIPATION 0.25 mW/BIT**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**
- **REPLACES FOUR 1024 BY ONE RAMs**

LOGIC SYMBOL

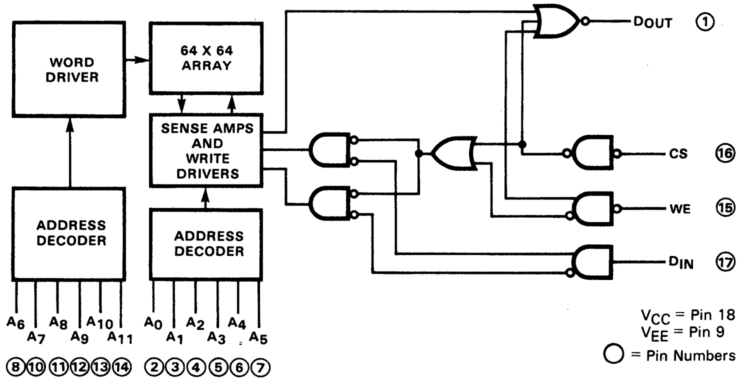


V_{CC} = Pin 18
V_{EE} = Pin 9

PIN NAMES

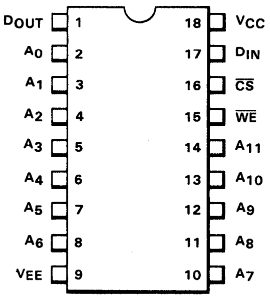
$\overline{CS}$	Chip Select Input
$A_0 - A_{11}$	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

LOGIC DIAGRAM



V_{CC} = Pin 18
V_{EE} = Pin 9
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The F10470 is a fully decoded 4096-bit Random Access Memoy organized 4096 words by one bit. Word selection is achieved by means of a 12-bit address, A_0 thru A_{11}.

One chip Select input is provided for memory array expansion up to 8192 words without the need for external decoding. For larger memories, the fast Chip Select access time permits the decoding of Chip Select, $\overline{CS}$, from the address withoutincreasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable, $\overline{WE}$ (pin 15). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at D_{OUT} and is non-inverted.

An unterminated emitter-follower output is provided on the F10470 to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many F10470s can be tied together. In other applications the wired-OR is not used. In either case an external 50 Ω pull down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is off.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{EE} Pin Potential to Ground Pin	−7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	−30 mA to +0.1 mA

TABLE 1 – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	OPEN EMITTER	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

L = LOW Voltage Levels = −1.7 V
H = HIGH Voltage Levels = −0.9 V
(Nominal values)
X = Don't Care

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{EE}) MIN	TYP	MAX	AMBIENT TEMPERATURE See Note 4
F10470	−5.46 V	−5.2 V	−4.94 V	0°C to 75°C

DC CHARACTERISTICS: V_{EE} = −5.2 V, Output Load = 50 Ω and 30 pF to −2.0 V, T_A = 0°C to 75°C (Note 4)

SYMBOL	CHARACTERISTIC	B LIMIT	TYP (Note 3)	A LIMIT	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	−1000		−840	mV	0°C	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to −2.0 V
		−960		−810		+25°C		
		−900		−720		+75°C		
V_{OL}	Output Voltage LOW	−1870		−1665	mV	0°C		
		−1850		−1650		+25°C		
		−1830		−1625		+75°C		
V_{OHC}	Output Voltage HIGH	−1020			mV	0°C	$V_{IN} = V_{IHB}$ or V_{ILA}	
		−980				+25°C		
		−920				+75°C		
V_{OLC}	Output Voltage LOW			−1645	mV	0°C		
				−1630		+25°C		
				−1605		+75°C		
V_{IH}	Input Voltage HIGH	−1145		−840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs	
		−1105		−810		+25°C		
		−1045		−720		+75°C		
V_{IL}	Input Voltage LOW	−1870		−1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs	
		−1850		−1475		+25°C		
		−1830		−1450		+75°C		
I_{IH}	Input Current HIGH			220	µA	0 to +75°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW, $\overline{CS}$	0.5		170	µA	+25°C	$V_{IN} = V_{ILB}$	
	All others	−50						
I_{EE}	Power Supply Current (Pin 8)		−180		mA	+75°C	All Inputs and Outputs Open	
			−200			0°C		

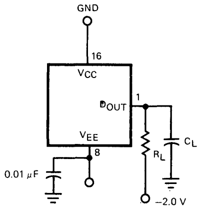
NOTES:

1. Conditions for testing, not shown in the tables are chosen to guarantee operation under "worst case" conditions.
2. The specified Limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at $V_{EE} = -5.2$ V, $T_A = 25°$C and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   θ_{JC} (Junction to Case) = 25°C/Watt
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
6. DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET:
   The symbols and terms used in this data sheet have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.

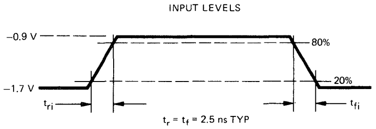
AC CHARACTERISTICS: $V_{EE} = -5.2$ V ±5%, Output Load = 50 Ω, 30 pF to −2.0 V, $T_A = 0°$C to 75°C

SYMBOL	PARAMETER	MIN	TYP (Note 3)	MAX	UNITS	CONDITIONS
t_{ACS}	Chip Select Access Time		10		ns	Fig 1a and b measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} or V_{OH})
t_{RCS}	Chip Select Recovery Time		10		ns	
t_{AA}	Address Access Time		30		ns	
t_W	Write Pulse Width (to Guarantee writing)		25		ns	
t_{WSD}	Data Sep-up Time Prior to Write		1		ns	
t_{WHD}	Data Hold Time After Write		1			
t_{WSA}	Address Seo-up Time Prior to Write		5		ns	
t_{WHA}	Address Hold Time After Write		1		ns	
t_{WSCS}	Chip Select Set-up Time Prior to Write		1		ns	
t_{WHCS}	Chip Select Hold Time After Write		1		ns	Fig. 2 measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})
t_{WS}	Write Disable Time		6		ns	
t_{WR}	Write Recovery Time		15		ns	
t_r	Output Rise Time		5		ns	Measured between 20% and 80% points. (Fig. 1a)
t_f	Output Fall Time		5		ns	
C_{IN}	Input Pin Capacitance		4		pF	Measure with a Pulse Technique
C_{OUT}	Output Pin Capacitance		7		pF	

LOADING CONDITIONS



INPUT LEVELS



All Timing Measurements Referenced to 50% of Input Levels

C_L = 30 pF including Jig and Stray Capacitance

R_L = 50 Ω Termination

READ MODE PROPAGATION DELAY FROM CHIP SELECT

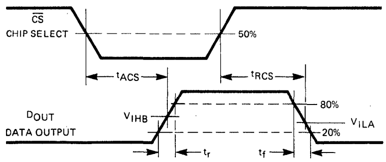


Fig. 1a

READ MODE PROPAGATION DELAY FROM ADDRESS

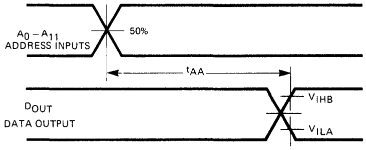


Fig. 1b

WRITE MODE

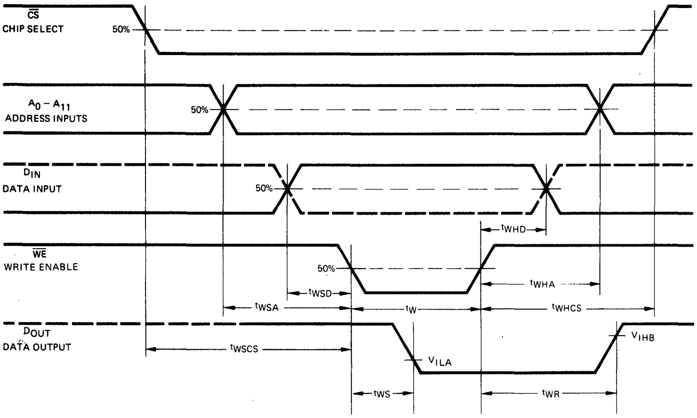


Fig. 2

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

TTL ISOPLANAR MEMORY 93410/93410A

256×1-BIT FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION – The 93410 and 93410A are high speed 256-bit TTL Random Access Memories with full decoding on chip. They are organized 256 words by one bit and are designed for scratchpad, buffer and distributed main memory applications. The devices have three Chip Select lines to simplify their use in larger memory systems. Address input pin locations are specifically chosen to permit maximum packaging density and for ease of PC board layout. An uncommitted collector output is provided to permit "OR-ties" for ease of memory expansion.

- **ORGANIZATION – 256 WORDS X 1 BIT**
- **THREE HIGH SPEED CHIP SELECT INPUTS**
- **TYPICAL ACCESS TIME**

93410A	**Commercial**	**35 ns**
93410	**Commercial**	**45 ns**
93410	**Military**	**45 ns**

- **NON INVERTED DATA OUTPUT**
- **ON-CHIP DECODING**
- **POWER DISSIPATION – 1.8 mW/BIT**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**

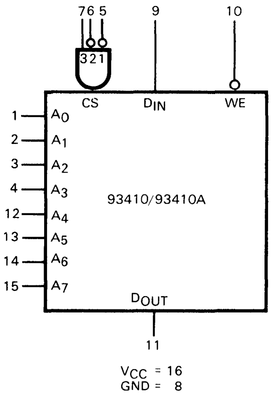
PIN NAMES		**LOADING (Notes a, b)**
$\overline{CS}_1$, $\overline{CS}_2$, CS_3	Chip Select Inputs	0.5 U.L.
$A_0 - A_7$	Address Inputs	0.5 U.L.
D_{IN}	Data Input	0.5 U.L.
D_{OUT}	Data Output	10 U.L.
$\overline{WE}$	Write Enable	0.5 U.L.

NOTES:

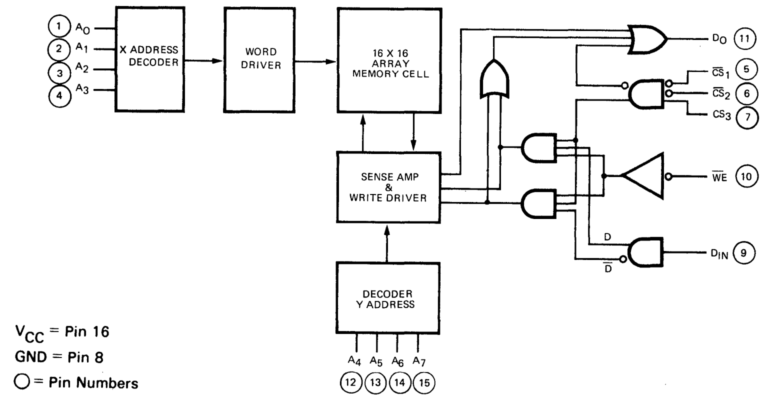
a. 1 Unit Load (U.L.) = 40 μA HIGH / 1.6 mA LOW

b. 10 U.L. is the output LOW drive factor. An external pull-up resistor is needed to provide HIGH level drive capability. This output will sink a maximum of 16 mA at V_{OUT} = 0.45 V.

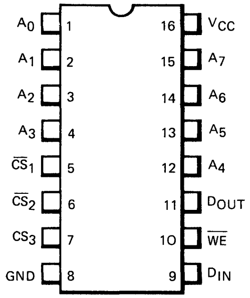
LOGIC SYMBOL



LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The 93410/93410A are fully decoded 256-bit Random Access Memories organized 256 words by one bit. Word selection is achieved by means of an 8-bit address, A_0 thru A_7.

Three Chip Select inputs are provided, two are active LOW ($\overline{CS}_1$ and $\overline{CS}_2$) and the third active HIGH (CS_3) for maximum logic flexibility. This permits memory array expansion up to 2048 words without the need for additional external decoders. For larger memories the fast chip select access time permits the decoding of Chip Select, CS, from the Address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable, $\overline{WE}$ (pin 10). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at D_{OUT} and is non-inverted.

Uncommitted collector outputs are provided to allow maximum flexibility in output connection. In many applications, such as memory expansion, the outputs of several 93410s or 93410As can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of R_L value must be used to provide a HIGH at the output when it is off. Any value of R_L within the range specified below may be used.

$$\frac{V_{CC}\,(MAX)}{16 - F.O.\,(1.6)} \leqslant R_L \leqslant \frac{V_{CC}\,(MIN) - V_{OH}}{N\,(I_{CEX}) + F.O.\,(0.04)}$$

R_L is in kΩ
N = number of wired-OR outputs tied together
F.O. = number of TTL Unit Loads (U.L.) driven
I_{CEX} = Memory Output Leakage Current in mA
V_{OH} = Required Output HIGH level at Output Node

The minimum value of R_L is limited by output current sinking ability. The maximum value of R_L is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}.

TABLE I – TRUTH TABLE

INPUTS					OUTPUT	MODE
$\overline{CS}_1$ PIN 5	$\overline{CS}_2$ PIN 6	CS_3 PIN 7	$\overline{WE}$	D_{IN}	D_{OUT}	
H	X	X	X	X	H	Not Selected
X	H	X	X	X	H	Not Selected
X	X	L	X	X	H	Not Selected
L	L	H	L	L	H	Write "0"
L	L	H	L	H	H	Write "1"
L	L	H	H	X	D_{OUT}	Read data from addressed location

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
**Voltage Applied to Outputs (output HIGH)	0.5 V to +5.50 V
Output Current (dc) (Output LOW)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93410XC, 93410AXC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93410XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges. Notes 1, 2 and 3

SYMBOL	PARAMETER		LIMITS			UNITS	CONDITIONS	
			MIN	TYP	MAX			
V_{OL}	Output LOW Voltage			0.3	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage		2.0	1.6		V	Guaranteed input logical HIGH voltage for all inputs.	
V_{IL}	Input LOW Voltage			1.5	0.85	V	Guaranteed input logical LOW voltage for all inputs.	
I_{IL}	Input LOW Current			−530	−800	μA	V_{CC} = MAX , V_{IN} = 0 V	
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX , V_{IN} = 4.5 V	
I_{CEX}	Output Leakage Current			1.0	50	μA	V_{CC} = MAX , V_{OUT} = 4.5 V	
V_{CD}	Input Clamp Diode Voltage			−1.0	−1.5	V	V_{CC} = MAX , I_{IN} = −10 mA	
I_{CC}	Power Supply Current	93410XC		90	135	mA	T_A = +75°C	V_{CC} = MAX
		93410AXC		100	140		T_A = 0°C	All inputs grounded
		93410XM		90	135		T_A = +125°C	See Power Supply
				100	145		T_A = −55°C	vs Temp. Curve

AC CHARACTERISTICS: Over Operating Voltage and Temperature Range

SYMBOL	PARAMETER	93410AXC			93410XC			93410XM			UNITS	CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
READ MODE	DELAY TIMES											
t_{ACS}	Chip Select Access Time		20	25		25	30		25	40	ns	**See Test Circuit and Waveforms Note 5**
t_{RCS}	Chip Select Recovery Time		20	25		25	35		25	40	ns	
t_{AA}	Address Access Time		35	45		45	60		45	70	ns	
WRITE MODE	DELAY TIMES											
t_{WS}	Write Disable Time	10	20	35	10	20	40	10	20	50	ns	
t_{WR}	Write Recovery Time		25	35		25	40		25	50	ns	
	INPUT TIMING REQUIREMENTS											
t_W	Minimum Write Pulse Width	30	20		30	25		40	25		ns	
t_{WSD}	Data Set-up Time Prior to Write	5	0		5	0		5	0		ns	**See Test Circuit and Waveforms Notes 6**
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0		ns	
t_{WSA}	Address Set-Up Time	10	0		10	0		10	0		ns	
t_{WHA}	Address Hold Time	5	0		5	0		5	0		ns	
t_{WSCS}	Chip Select Set-up Time	5	0		5	0		5	0		ns	
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0		ns	
C_{IN}	Input Pin Capacitance		4	5		4	5		4	5	pF	Measured with a
C_{OUT}	Output Pin Capacitance		7	8		7	8		7	8	pF	pulse technique

NOTES:

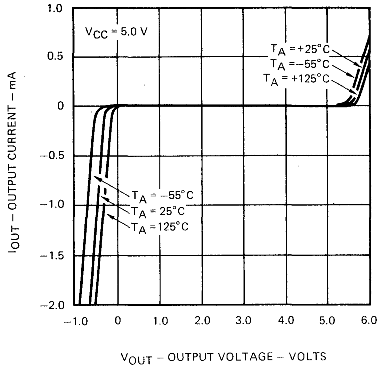
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.

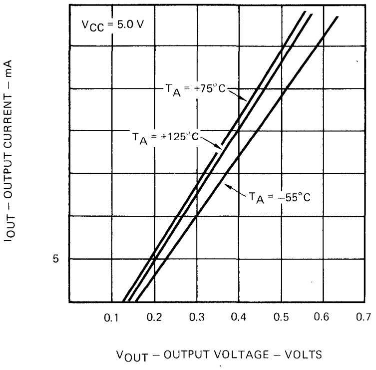
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.

TYPICAL ELECTRICAL CHARACTERISTICS

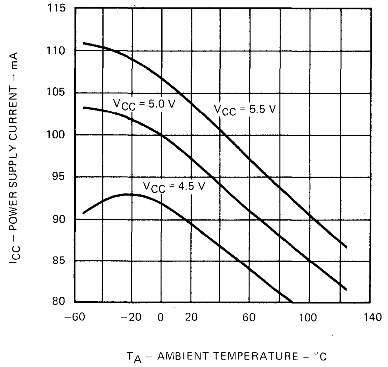
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



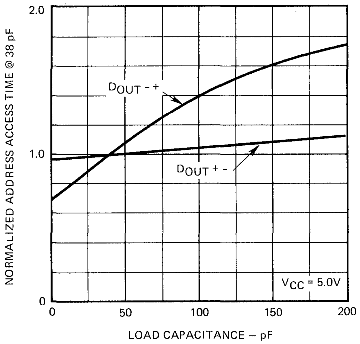
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



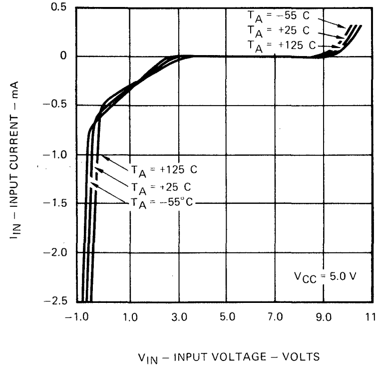
POWER SUPPLY CURRENT VERSUS TEMPERATURE



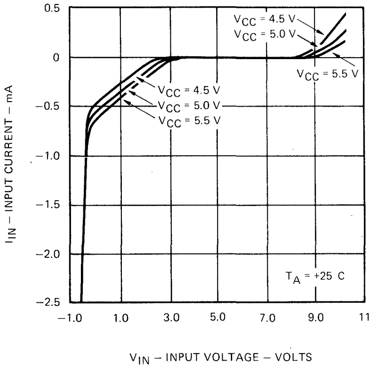
NORMALIZED ADDRESS ACCESS TIME VERSUS LOAD CAPACITANCE



INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS TEMPERATURE

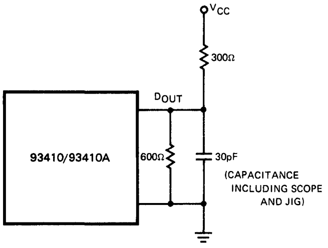


INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS SUPPLY VOLTAGE

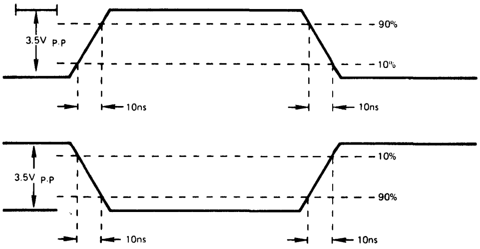


AC TEST LOAD AND WAVEFORM

LOADING CONDITION



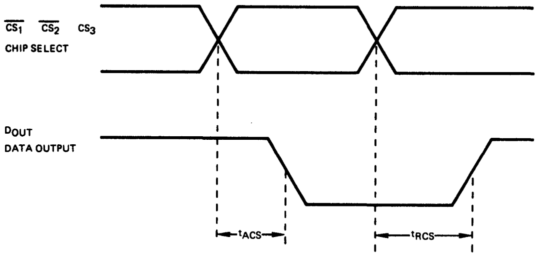
INPUT PULSES



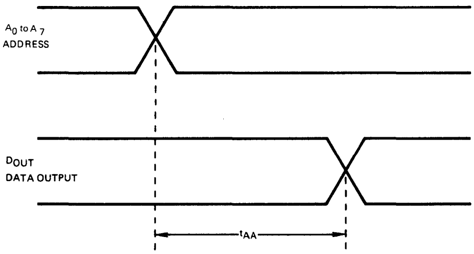
AC WAVEFORMS

READ MODE

PROPAGATION DELAY FROM CHIP SELECT

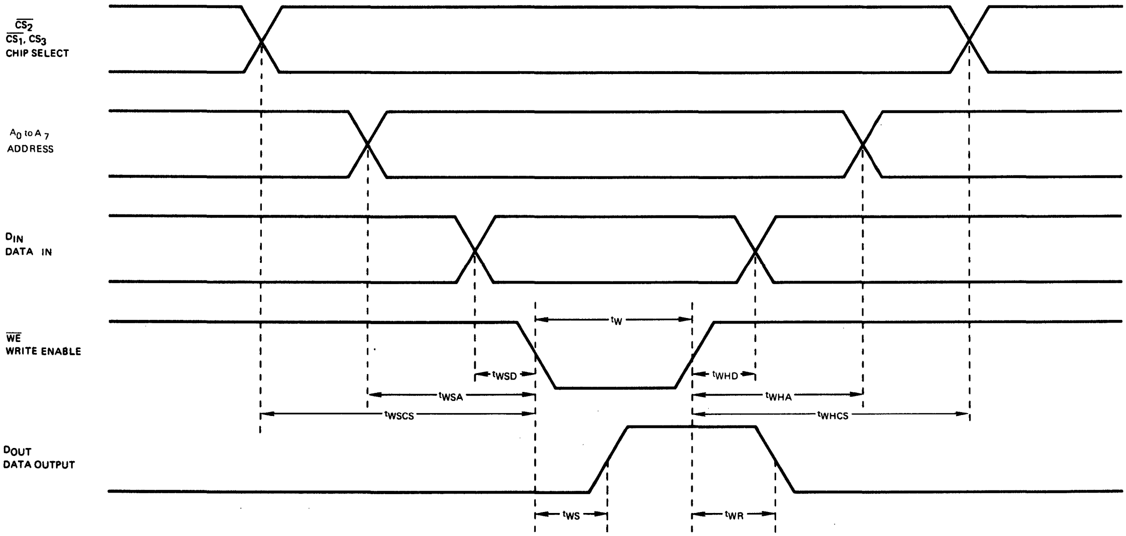


PROPAGATION DELAY FROM ADDRESS



(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

WRITE MODE



(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

TTL ISOPLANAR MEMORY 93411/93411A

256×1—BIT FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION – The 93411 and 93411A are high speed 256-bit TTL Random Access Memories with full decoding on chip. They are organized 256 words by one bit and are designed for scratchpad, buffer and distributed main memory applications. The devices have three chip select lines to simplify their use in larger memory systems. Address input pin locations are specifically chosen to permit maximum packaging density and for ease of PC board layout. An uncommitted collector output is provided to permit "OR-ties" for ease of memory expansion.

- **REPLACEMENT FOR 54/74S206 AND EQUIVALENT DEVICES**
- **ORGANIZATION – 256 WORDS X 1 BIT**
- **THREE HIGH SPEED CHIP SELECT INPUTS**
- **TYPICAL ACCESS TIME**

93411A	**Commercial**	**40 ns**
93411	**Commercial**	**45 ns**
93411	**Military**	**45 ns**

- **ON CHIP DECODING**
- **POWER DISSIPATION – 1.8 mW/BIT**
- **POWER DISSIPATION DECREASES WITH TEMPERATURE**
- **INVERTED DATA OUTPUT**

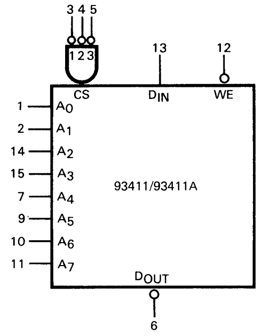
PIN NAMES		**LOADING (Notes a, b)**
$\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$	Chip Select Inputs	0.5 U.L.
$A_0 - A_7$	Address Inputs	0.5 U.L.
D_{IN}	Data Input	0.5 U.L.
$\overline{D_{OUT}}$	Data Output	10 U.L.
$\overline{WE}$	Write Enable	0.5 U.L.

NOTES:

a. 1 Unit Load (U.L.) = 40 μA HIGH / 1.6 mA LOW

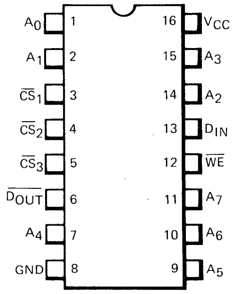
b. 10 U.L. is the output LOW drive factor. An external pull-up resistor is needed to provide HIGH level drive capability. This output will sink a maximum of 16 mA at V_{OUT} = 0.45 V.

LOGIC SYMBOL



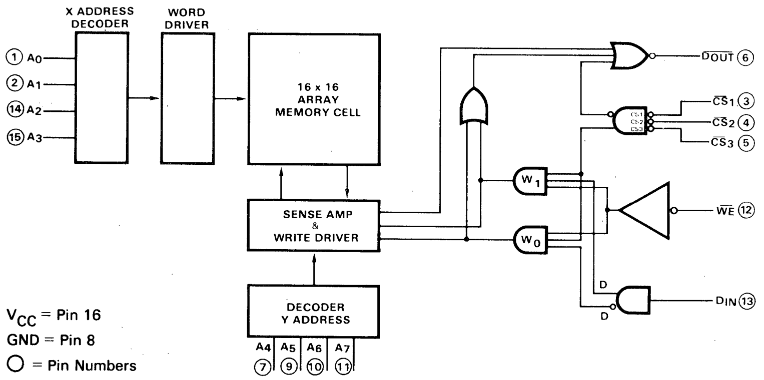
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The 93411/93411A are fully decoded 256-bit Random Access Memories organized 256 words by one bit. Word selection is achieved by means of an 8-bit address, A_0 thru A_7.

Three Chip Select inputs are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of Chip Select, $\overline{CS}$, from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$, pin 12). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at $\overline{D_{OUT}}$.

Uncommitted collector outputs are provided to allow maximum flexibility in output connection. In many applications, such as memory expansion, the outputs of several 93411s or 93411As can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of value R_L must be used to provide a HIGH at the output when it is off. Any value of R_L within the range specified below may be used.

$$\frac{V_{CC}(MAX)}{16 - F.O.\ (1.6)} \leq R_L \leq \frac{V_{CC}(MIN) - V_{OH}}{n\ (I_{CEX}) + F.O.\ (0.04)}$$

R_L is in kΩ
n = number of wired-OR outputs tied together
F.O. = number of TTL Unit Loads (U.L.) driven
I_{CEX} = Memory Output Leakage Current in mA
V_{OH} = Required Output HIGH level at Output Node

The minimum value of R_L is limited by output current sinking ability. The maximum value of R_L is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}.

TABLE I – TRUTH TABLE

INPUTS					OUTPUT	MODE
$\overline{CS}_1$ PIN 3	$\overline{CS}_2$ PIN 4	$\overline{CS}_3$ PIN 5	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	
H	X	X	X	X	H	Not Selected
X	H	X	X	X	H	Not Selected
X	X	H	X	X	H	Not Selected
L	L	L	L	L	H	Write "0"
L	L	L	L	H	H	Write "1"
L	L	L	H	X	$\overline{D_{OUT}}$	Read inverted data from addressed location

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
**Voltage Applied to Outputs (output HIGH)	−0.5 V to +5.50 V
Output Current (dc) (output LOW)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93411AXC, 93411XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93411XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges. Notes 1, 2 and 4

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP (Note 3)	LIMITS MAX	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage			0.3	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage		2.0	1.6		V	Guaranteed Input Logical HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage			1.5	0.85	V	Guaranteed Input Logical LOW Voltage for all Inputs	
I_{IL}	Input LOW Current			−530	−800	μA	V_{CC} = MAX, V_{IN} = 0 V	
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
I_{CEX}	Output Leakage Current			1.0	50	μA	V_{CC} = MAX, V_{OUT} = 4.5 V	
V_{CD}	Input Clamp Diode Voltage			−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA	
I_{CC}	Power Supply Current	93411XC		90	124	mA	T_A = +75°C	V_{CC} = MAX, WE Grounded, all other inputs @ 4.5 V, see Power Supply vs Temp. Curve
		93411AXC		100	135		T_A = 0°C	
		93411XM		90	117		T_A = +125°C	
				100	143		T_A = −55°C	

AC CHARACTERISTICS: Over Guaranteed Operating Ranges. Notes 1, 2, 4, 5, 6

SYMBOL	CHARACTERISTIC	93411AXC MIN	93411AXC TYP (Note 3)	93411AXC MAX	93411XC MIN	93411XC TYP (Note 3)	93411XC MAX	93411XM MIN	93411XM TYP (Note 3)	93411XM MAX	UNITS	CONDITIONS
READ MODE	DELAY TIMES											
t_{ACS}	Chip Select Time		25	30		25	30		25	40	ns	See Test Circuit and Waveforms Note 5
t_{RCS}	Chip Select Recovery Time		25	25		25	25		25	35		
t_{AA}	Address Access Time		40	45		45	55		45	65		
WRITE MODE	DELAY TIMES											
t_{WS}	Write Disable Time	10	20	35	10	20	35	10	20	45	ns	
t_{WR}	Write Recovery Time		25	40		25	40		25	50		
	INPUT TIMING REQUIREMENTS											
t_W	Write Pulse Width (to guarantee write)	40	25		40	25		50	25		ns	See Test Circuit and Waveforms Note 6
t_{WSD}	Data Set-Up Time Prior to Write	0	0		0	0		0	0			
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0			
t_{WSA}	Address Set-Up Time	0	0		0	0		0	0			
t_{WHA}	Address Hold Time	5	0		5	0		5	0			
t_{WSCS}	Chip Select Set-Up Time	0	0		0	0		0	0			
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0			
C_I	Input Lead Capacitance		4	5		4	4		4	5	pF	Measured with pulse technique
C_O	Output Lead Capacitance		7	8		7	8		7	8		

NOTES:

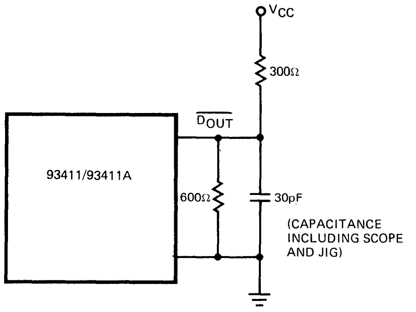
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.

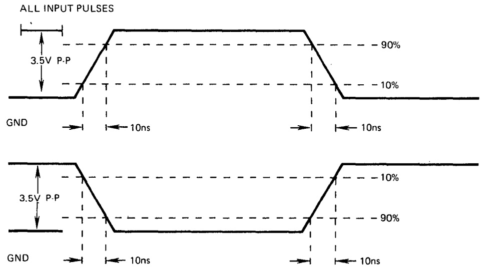
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.

AC TEST LOAD AND WAVEFORM

LOADING CONDITION



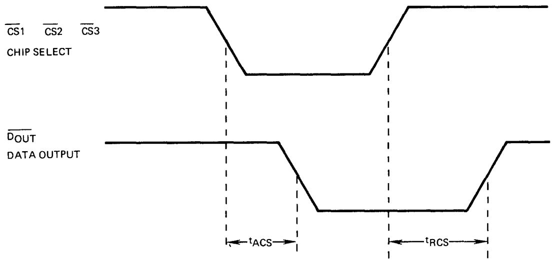
INPUT PULSES



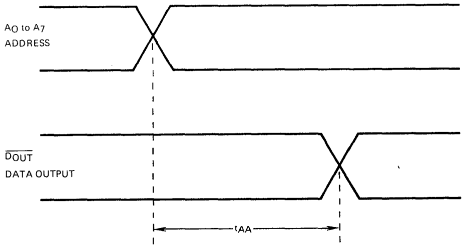
AC WAVEFORMS

READ MODE

PROPAGATION DELAY FROM CHIP SELECT

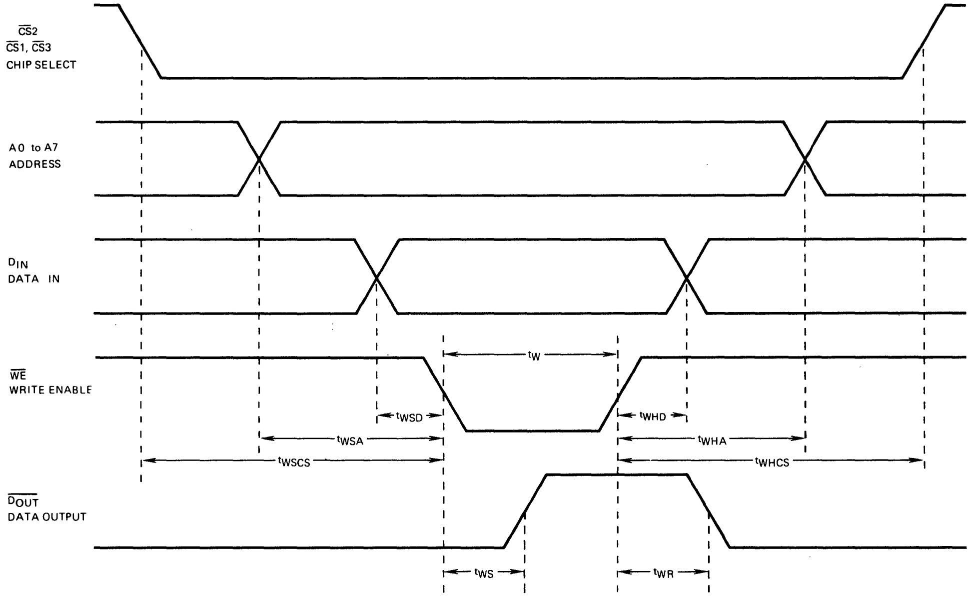


PROPAGATION DELAY FROM ADDRESS



(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

WRITE MODE

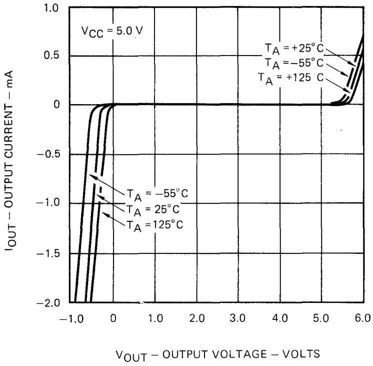


(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

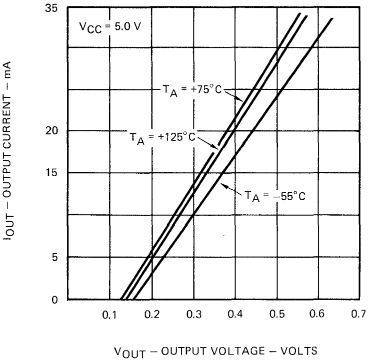
NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

TYPICAL ELECTRICAL CHARACTERISTICS

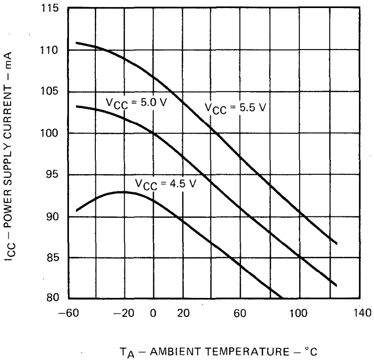
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



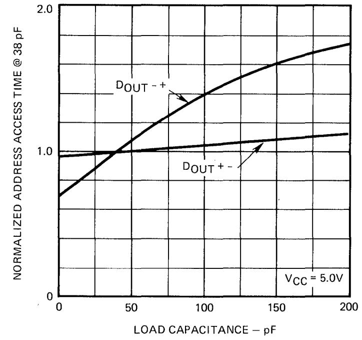
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



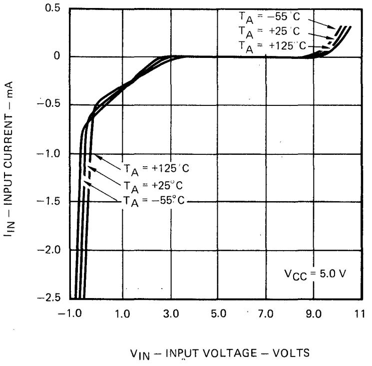
POWER SUPPLY CURRENT VERSUS TEMPERATURE



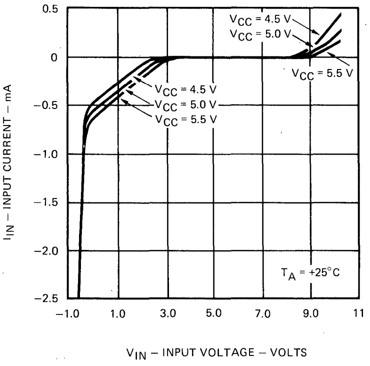
NORMALIZED ADDRESS ACCESS TIME VERSUS LOAD CAPACITANCE



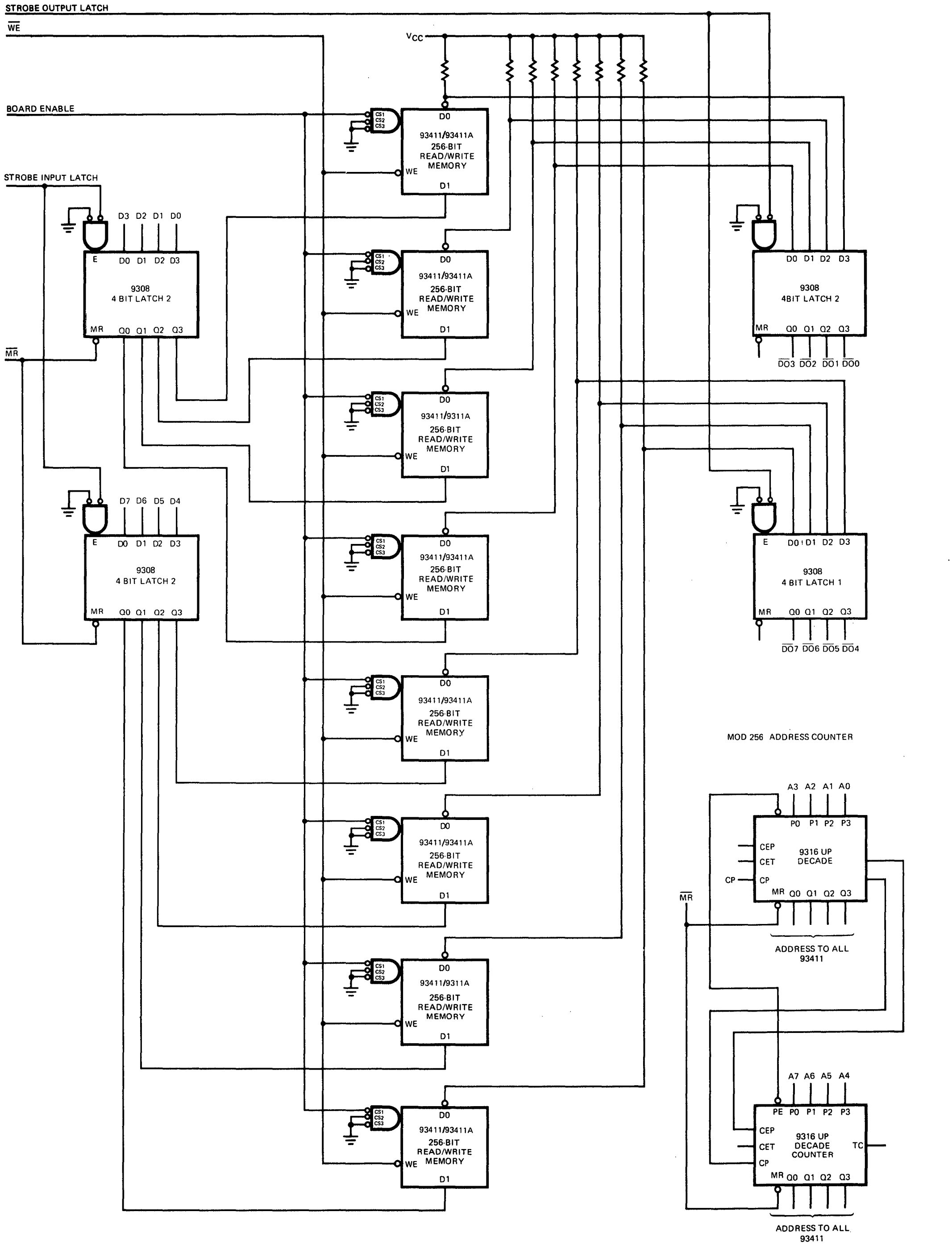
INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS TEMPERATURE



INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS SUPPLY VOLTAGE



APPLICATIONS



256-WORD BY 8-BIT BUFFER MEMORY SYSTEM

TTL ISOPLANAR MEMORY 93L412

256×4-BIT FULLY DECODED RANDOM ACCESS MEMORY

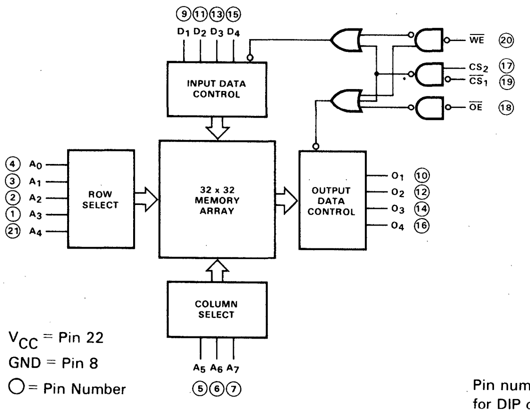
DESCRIPTION – The 93L412 is a 1024-bit Read/Write Random Access Memory organized 256 words by four bits per word. The 93L412 has uncommitted collector outputs and is designed primarily for buffer control storage and high performance main memory applications. the device has a typical address access time of 45 ns.

- **ISOPLANAR TECHNOLOGY**
- **ORGANIZATION – 256 WORDS X 4 BITS**
- **UNCOMMITTED COLLECTOR OUTPUTS**
- **STANDARD 22-PIN DUAL IN-LINE PACKAGE**
- **TWO CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION**
- **LOW POWER DISSIPATION – 0.27 mW/BIT TYP**
- **TYPICAL READ ACCESS TIME – 45 ns**

PIN NAMES

$A_0 - A_7$	Address Inputs
$D_1 - D_4$	Data Inputs
$\overline{CS}_1$, CS_2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
$O_1 - O_4$	Data Outputs
$\overline{OE}$	Output Enable

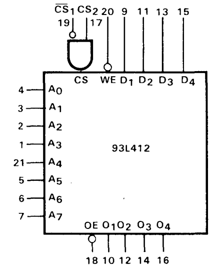
LOGIC DIAGRAM



V_{CC} = Pin 22
GND = Pin 8
○ = Pin Number

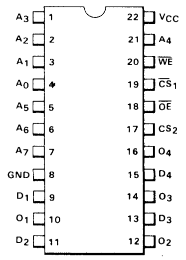
Pin numbers specified for DIP only.

LOGIC SYMBOL

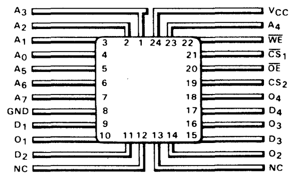


V_{CC} = Pin 22
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



FUNCTIONAL DESCRIPTION – The 93L412 is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A_0 thru A_7.

Two Chip Select inputs are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of Chip Select, CS, from the address without increasing address access time.

The 93L412 has uncommitted collector outputs to allow maximum flexibility in output connection. In many applications, such as memory expansion, the outputs of several 93L412s can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of value R_L must be used to provide a HIGH at the output when it is off. Any value of R_L within the range specified below may be used.

$$\frac{V_{CC}(\text{MAX})}{8 - \text{F.O.}\,(1.6)} \leq R_L \leq \frac{V_{CC}(\text{MIN}) - V_{OH}}{N\,(I_{CEX}) + \text{F.O.}\,(0.04)}$$

R_L is in kΩ
N = number of wired-OR outputs tied together
F.O. = number of TTL Unit Loads (U.L.) driven
I_{CEX} = Memory Output Leakage Current in mA
V_{OH} = Required Output HIGH level at Output Node

The minimum value of R_L is limited by output current sinking ability. The maximum value of R_L is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}.

TRUTH TABLE

INPUTS					OUTPUTS	MODE
$\overline{OE}$ PIN 18	$\overline{CS}_1$ PIN 19	CS_2 PIN 17	$\overline{WE}$ PIN 20	D_{1-4} PINS 9,11,13,15	93L412 O.C.	
X	H	X	X	X	H	Not Selected
X	X	L	X	X	H	Not Selected
L	L	H	H	X	$O_1 - O_4$	Read Stored Data
X	L	H	L	L	H	Write "0"
X	L	H	L	H	H	Write "1"
H	L	H	H	X	H	Output Disabled
H	L	H	L	L	H	Write "0" (Output Disabled)
H	L	H	L	H	H	Write "1" (Output Disabled)

H = HIGH Voltage; L = LOW Voltage; X = Don't Care (HIGH or LOW); OC = Open Collector

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Lead Potential to Ground Lead	−0.5 V to +7.0 V
Input Voltage (dc)*	−0.5 V to +5.5 V
Input Current (dc)*	−12 mA to +5.0 mA
Voltage Applied to Outputs (output HIGH)**	−0.5 V to +5.50 V
Output Current (dc)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93L412XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93L412XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2, 4)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		MIN	TYP (Note 3)	MAX			
V_{OL}	Output LOW Voltage		0.3	0.45	V	V_{CC} = MIN, I_{OL} = 8 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current		−150	−300	µA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	40	µA	V_{CC} = MAX, V_{IN} = 4.5 V	
				1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
V_{CD}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = MAX, IN = −10 mA	
I_{CEX}	Output Leakage Current		1.0	100	µA	V_{CC} = MAX, V_{OUT} = 4.5 V	
I_{CC}	Power Supply Current 93L412XC		55	75	mA	T_A = +75°C	V_{CC} = MAX, All Inputs and Outputs Open
	93L412XC		60	80		T_A = 0°C	
	93L412XM		50	70		T_A = +125°C	
	93L412XM		65	90		T_A = −55°C	

AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

SYMBOL	CHARACTERISTIC	93L412XC			93L412XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Time		20	35		20	45	ns	See Test Circuit and Waveforms
t_{RCS}	Chip Select Recovery Time		20	35		20	45		
t_{AOS}	Output Enable Time		20	35		20	45		
t_{ROS}	Output Enable Recovery Time		20	35		20	45		
t_{AA}	Address Access Time		45	60		45	75		
WRITE MODE	DELAY TIMES								See Test Circuit and Waveforms
t_{WS}	Write Disable Time		20	40		20	45	ns	
t_{WR}	Write Recovery Time		25	45		25	50		
	INPUT TIMING REQUIREMENTS								
t_W	Write Pulse Width (to guarantee write)	45	30		55	35		ns	
t_{WSD}	Data Set-Up Time Prior to Write	5	0		5	0			
t_{WHD}	Data Hold Time After Write	5	0		5	0			
t_{WSA}	Address Set-Up Time	10	0		10	0			
t_{WHA}	Address Hold Time	5	0		10	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0			
t_{WHCS}	Chip Select Hold Time	5	0		10	0			
C_I	Input Pin Capacitance		3	5		3	5	pF	Measure with Pulse Technique
C_O	Output Pin Capacitance		5	8		5	8		

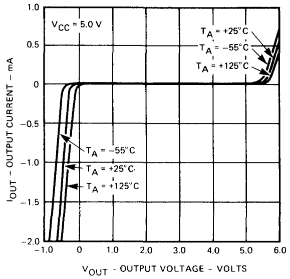
NOTES:

1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:

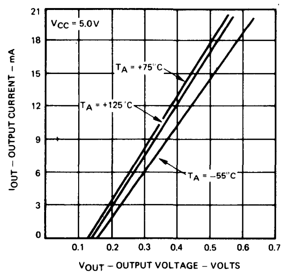
   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 15 °C/Watt, Flatpak.
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.

TYPICAL ELECTRICAL CHARACTERISTIC CURVES

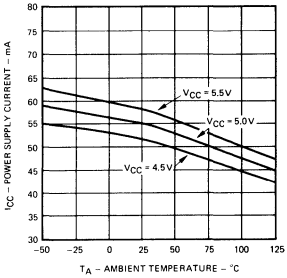
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



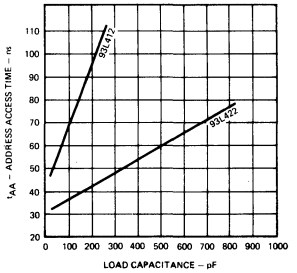
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



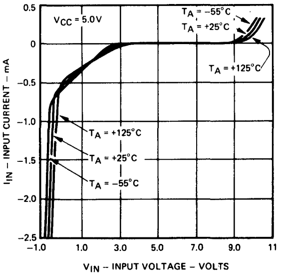
POWER SUPPLY CURRENT VERSUS TEMPERATURE



ADDRESS ACCESS TIME VERSUS LOAD CAPACITANCE

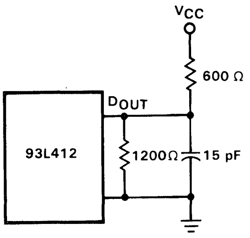


INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS TEMPERATURE



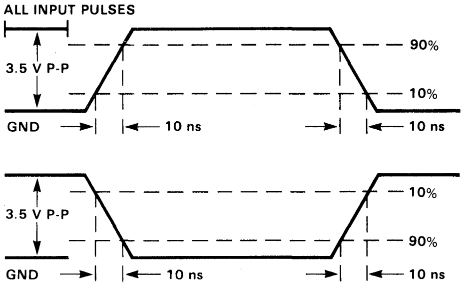
AC TEST LOAD AND WAVEFORM

LOADING CONDITIONS

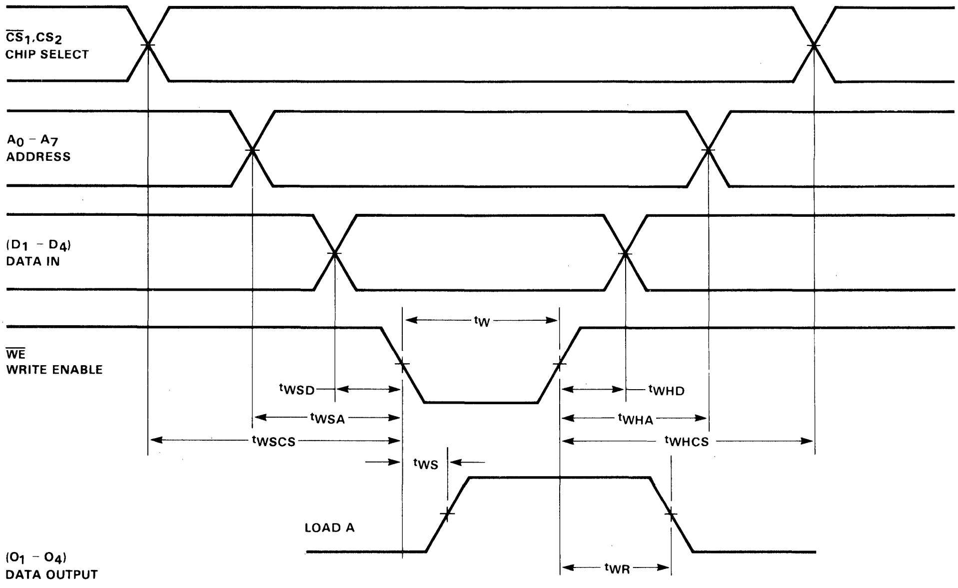


Load A

INPUT PULSES

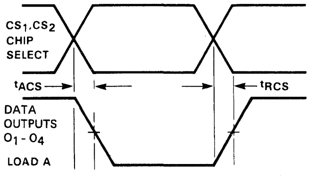


WRITE MODE

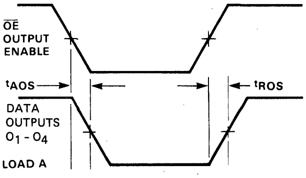


READ MODE

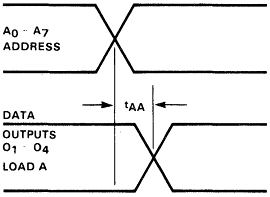
PROPAGATION DELAY FROM CHIP SELECT



PROPAGATION DELAY FROM OUTPUT ENABLE



PROPAGATION DELAY FROM ADDRESS INPUTS



(All above measurements referenced to 1.5 V unless otherwise indicated)

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

93412

TTL ISOPLANAR MEMORY

256 × 4-BIT FULLY DECODED RANDOM ACCESS MEMORY

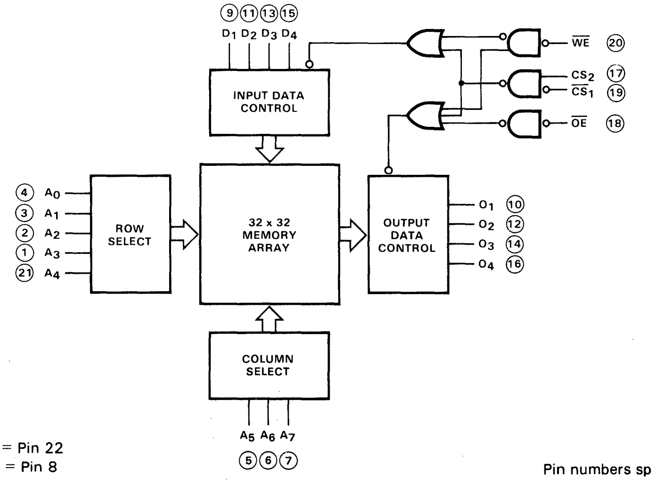
DESCRIPTION – The 93412 is a 1024-bit Read/Write Random Access Memory organized 256 words by four bits per word. The 93412 has uncommitted collector outputs and is designed primarily for buffer control storage and high performance main memory applications. The device has a typical address access time of 30 ns.

- **ISOPLANAR TECHNOLOGY**
- **ORGANIZATION – 256 WORDS X 4 BITS**
- **UNCOMMITTED COLLECTOR OUTPUTS**
- **STANDARD 22-PIN DUAL IN-LINE PACKAGE**
- **TWO CHIP SELECT INPUTS PROVIDES EASY MEMORY EXPANSION**
- **POWER DISSIPATION – 0.475 mW/BIT TYPICAL**
- **TYPICAL READ ACCESS TIME – 30 ns**

PIN NAMES

$A_0 - A_7$	Address Inputs
$D_1 - D_4$	Data Inputs
$\overline{CS}_1$, CS_2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
$O_1 - O_4$	Data Outputs
$\overline{OE}$	Output Enable

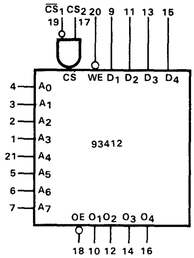
LOGIC DIAGRAM



V_{CC} = Pin 22
GND = Pin 8
○ = Pin Number

Pin numbers specified for DIP only

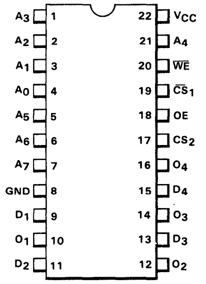
LOGIC SYMBOL



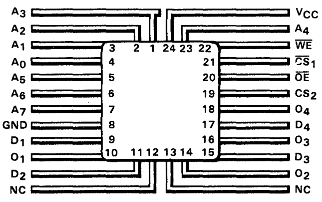
V_{CC} = Pin 22
GND = Pin 8

CONNECTION DIAGRAMS

DIP (TOP VIEW)



FLATPAK (TOP VIEW)



FUNCTIONAL DESCRIPTION – The 93412 is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A_0 thur A_7.

Two Chip Select inputs are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of Chip Select, CS, from the address without increasing address access time.

The 93412 has uncommitted collector outputs to allow maximum flexibility in output connection. In many applications, such as memory expanxion, the outputs of several 93412s can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of value R_L must be used to provide a HIGH at the output when it is off. Any value of R_L within the range specified below may be used.

$$\frac{V_{CC}\,(\text{MAX})}{8 - \text{F.O.}\,(1.6)} \leqslant R \leqslant \frac{V_{CC}\,(\text{MIN}) - V_{OH}}{N\,(I_{CEX}) + \text{F.O.}\,(0.04)}$$

R_L is in kΩ
N = number or wired-OR outputs tied together
F.O. = number of TTL Unit Loads (U.L.) driven
I_{CEX} = Memory Output Leakage Current in mA
V_{OH} = Required Output HIGH level at Output Node

The minimum value of R_L is limited by output current sinking ability. The maximum value of R_L is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}.

TRUTH TABLE

INPUTS $D_1 - D_4$					OUTPUTS	
$\overline{OE}$ PIN 18	$\overline{CS}_1$ PIN 19	CS_2 PIN 17	$\overline{WE}$ PIN 20	D_{1-4} PINS 9, 11,13, 15	93412 O.C.	MODE
X	H	X	X	X	H	Not Selected
X	X	L	X	X	H	Not Selected
L	L	H	H	X	$O_1 - O_4$	Read Stored Data
X	L	H	L	L	H	Write "0"
X	L	H	L	H	H	Write "1"
H	L	H	H	X	H	Output Disabled
H	L	H	L	L	H	Write "0" (Output Disabled)
H	L	H	L	H	H	Write "1" (Output Disabled)

H = HIGH Voltage, L = LOW Voltage, X = Don't Care (HIGH or LOW), OC = Open Collector

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
**Voltage Applied to Outputs (output HIGH)	0.5 V to +5.50 V
Output Current (dc)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93412XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93412XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2, 4)

SYMBOL	CHARACTERISTIC		LIMITS MIN	LIMITS TYP (Note 3)	LIMITS MAX	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage			0.3	0.45	V	V_{CC} = MIN, I_{OL} = 8 mA	
V_{IH}	Input HIGH Voltage		2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage			1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current			−150	−300	μA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
V_{CD}	Input Diode Clamp Voltage			−10	−1.5	V	V_{CC} = MAX, IN = −10 mA	
I_{CEX}	Output Leakage Current			1.0	100	μA	V_{CC} = MAX, V_{OUT} = 4.5 V	
I_{CC}	Power Supply Current	93412XC		95	130	mA	T_A = +75°C	V_{CC} = MAX, All Inputs and Outputs Open
		93412XC			155		T_A = 0°C	
		93412XM			120		T_A = +125°C	
		93412XM			170		T_A = −55°C	

AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

SYMBOL	CHARACTERISTIC	93412XC MIN	93412XC TYP (Note 3)	93412XC MAX	93412XM MIN	93412XM TYP (Note 3)	93412XM MAX	UNITS	CONDITIONS
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Time		20	30		20	45	ns	See Test Circuit and Waveforms
t_{RCS}	Chip Select Recovery Time (93412)		20	30		20	45		
t_{AOS}	Output Enable Time		20	30		20	45		
t_{ROS}	Output Enable Recovery Time (93412)		20	30		20	45		
t_{AA}	Address Access Time		30	45		40	60		
WRITE MODE	DELAY TIMES								
t_{WS}	Write Disable Time (93412)		20	35		20	45	ns	See Test Circuit and Waveforms
t_{WR}	Write Recovery Time		25	40		25	50		
	INPUT TIMING REQUIREMENTS								
t_W	Write Pulse Width (to guarantee write)	30	20		40	30		ns	
t_{WSD}	Data Set-Up Time Prior to Write	5	0		5	0			
t_{WHD}	Data Hold Time After Write	5	0		5	0			
t_{WSA}	Address Set-Up Time	10	0		10	0			
t_{WHA}	Address Hold Time	5	0		10	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0			
t_{WHCS}	Chip Select Hold Time	5	0		10	0			
C_I	Input Pin Capacitance		3	5		3	5	pF	Measure with Pulse Technique
C_O	Output Pin Capacitance		5	8		5	8		

NOTES:

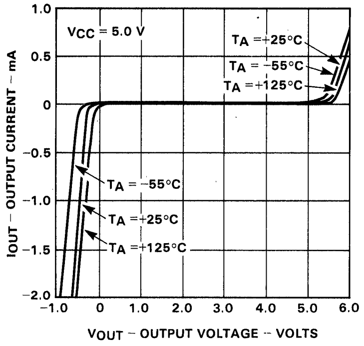
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military Range an additional reguirement of a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.

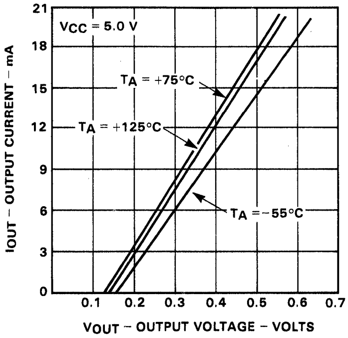
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.

TYPICAL ELECTRICAL CHARACTERISTIC CURVES

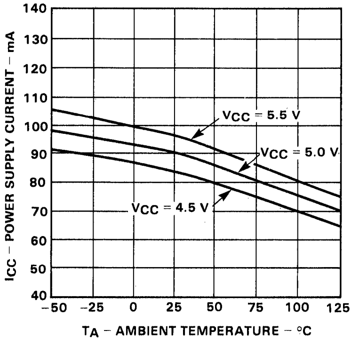
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



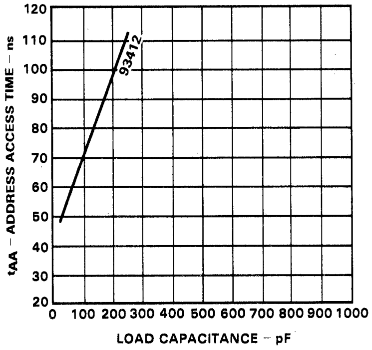
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



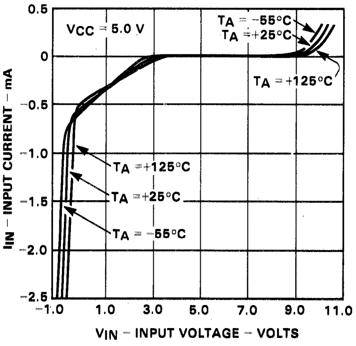
POWER SUPPLY CURRENT VERSUS TEMPERATURE



ADDRESS ACCESS TIME VERSUS LOAD CAPACITANCE



INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS TEMPERATURE



Note:
AC Test Load and waveform same as 93L412. See Page 7 60

TTL ISOPLANAR MEMORY 93L415

1024×1-BIT FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION – The 93L415 is a low power 1024-bit Read/Write Random Access Memory organized 1024 words by one bit. It has a typical access time of 35 ns and is designed for buffer and control storage and high performance main memory applications requiring low power.

The 93L415 includes full decoding on chip, has separate Data Input and Data Output lines and an active LOW Chip Select line.

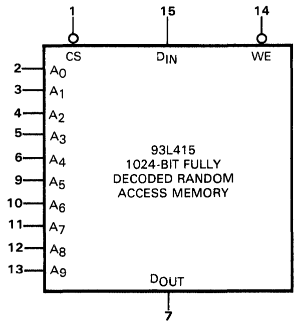
The device is fully compatible with the standard DTL and TTL logic families and has an uncommitted collector output for ease of memory expansion.

- **FULL MIL AND COMMERCIAL RANGES**
- **TTL INPUTS AND OUTPUT**
- **NON-INVERTING DATA OUTPUT**
- **ORGANIZED 1024 WORDS X 1 BIT**
- **READ ACCESS TIME 35 ns TYPICAL**
- **CHIP SELECT ACCESS TIME 20 ns TYPICAL**
- **POWER DISSIPATION 0.20 mW/BIT TYPICAL**
- **UNCOMMITTED COLLECTOR OUTPUT**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**

PIN NAMES

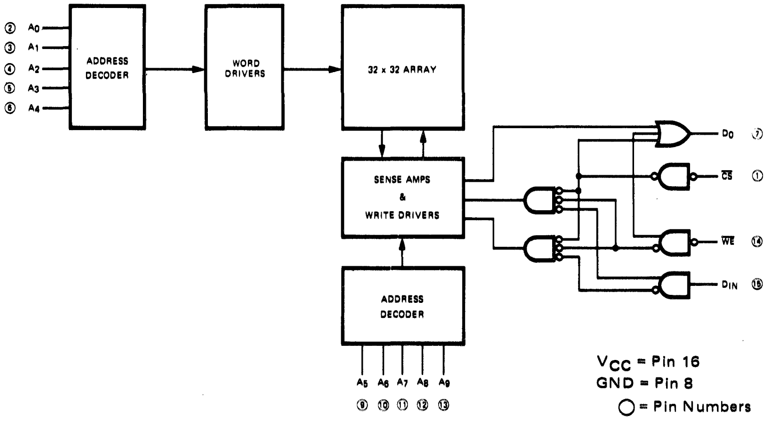
$\overline{CS}$	Chip Select Input
$A_0 - A_9$	Address Inputs
$\overline{WE}$	Write Enable Input
D_{IN}	Data Input
D_{OUT}	Data Output

LOGIC SYMBOL



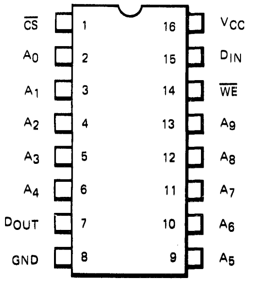
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAMS
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The 93L415 is a fully decoded 1024-bit Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A_0 to A_9.

The Chip Select input allows memory array expansion. For large memories, the fast chip select access time permits decoding of the Chip Select ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$, Pin 14). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at D_{OUT} and is non-inverted.

Uncommitted collector outputs are provided on the 93L415 to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93L415s can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of R_L value must be used to provide a HIGH at the output when it is off. Any R_L value within the range specified below may be used.

$$\frac{V_{CC}\ (\text{min})}{I_{OL} - FO\ (1.6)} \leqslant R_L \leqslant \frac{V_{CC}\ (\text{min}) - V_{OH}}{n\ (I_{CEX}) + FO\ (0.04)}$$

R_L is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output HIGH Level at Output Node
I_{OL} = Output LOW Current

The minimum R_L value is limited by output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}. One Unit Load = 40 μA HIGH/1.6 mA LOW.

TABLE I – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	Open Collector	
H	X	X	H	NOT SELECTED
L	L	L	H	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +5.5 V
*Input Current (dc)	–12 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +5.5 V
Output Current (dc) (Output LOW)	+20 mA

*Either input voltage or input current limit is sufficient to protect the input.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE (Note 4)
	MIN	TYP	MAX	
93L415XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93L415XM	4.50 V	5.0 V	5.50 V	-55°C to +125°C

X = package type; D for Ceramic DIP, F for Flatpak, P for Plastic DIP. See packaging information section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2, 4)

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 3)	LIMITS MAX	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage		0.35	0.50	V	V_{CC} = MIN, I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current		−150	−300	µA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	40	µA	V_{CC} = MAX, V_{IN} = 4.5 V	
				1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
I_{CEX}	Output Leakage Current		1.0	100	µA	V_{CC} = MAX, V_{OUT} = 4.5 V	
V_{CD}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA	
I_{CC}	Power Supply Current			55	mA	$T_A \geq 75°C$	V_{CC} = MAX, All Inputs Grounded
			45	65	mA	$T_A = 0°C$	
				75	mA	$T_A = -55°C$	

AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

SYMBOL	CHARACTERISTIC	93L415XC MIN	93L415XC TYP (Note 3)	93L415XC MAX	93L415XM MIN	93L415XM TYP (Note 3)	93L415XM MAX	UNITS	CONDITIONS
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Time		20	40		20	45	ns	See Test Circuit and Waveforms
t_{RCS}	Chip Select Recovery Time		20	40		20	50		
t_{AA}	Address Access Time		35	60		35	70		
WRITE MODE	DELAY TIMES								
t_{WS}	Write Disable Time		20	45		20	45	ns	See Test Circuit and Waveforms
t_{WR}	Write Recovery Time		20	45		30	55		
	INPUT TIMING REQUIREMENTS								
t_W	Write Pulse Width (to guarantee write)	45	25		50	25			
t_{WSD}	Data Set-Up Time Prior to Write	5	0		10	0			
t_{WHD}	Data Hold Time After Write	5	0		10	0			
t_{WSA}	Address Set-Up Time	10	0		10	0			
t_{WHA}	Address Hold Time	5	0		10	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		10	0			
t_{WHCS}	Chip Select Hold Time	5	0		10	0			
C_I	Input Lead Capacitance		4	5		4	5	pF	
C_O	Output Lead Capacitance		7	8		7	8		

NOTES:

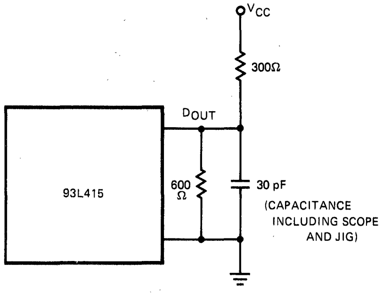
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Operating Temperature Ranges are guaranteed with transverse air flow exceed ing 400 linear feet per minute. For military range on additional requirement of a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°CC/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.

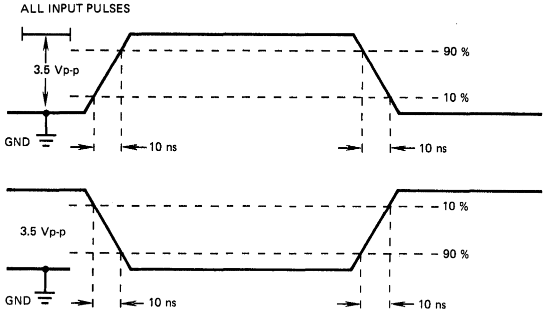
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.

AC TEST LOAD AND WAVEFORM

LOADING CONDITION



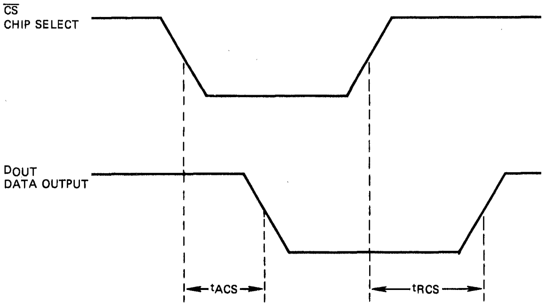
INPUT PULSES



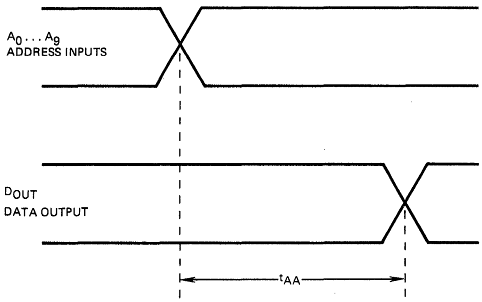
AC WAVEFORMS

READ MODE

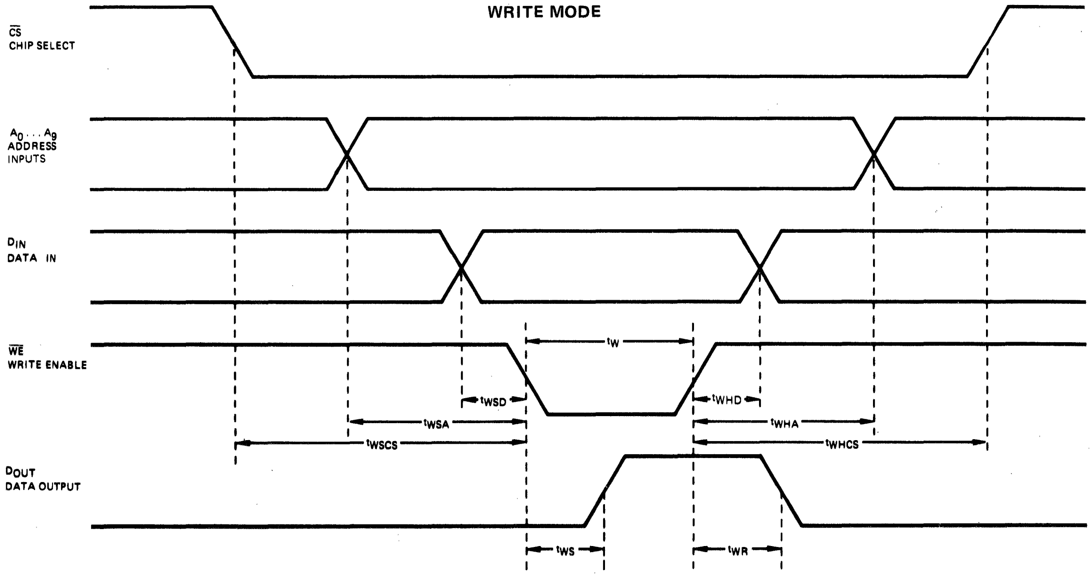
PROPAGATION DELAY FROM CHIP SELECT



PROPAGATION DELAY FROM ADDRESS INPUTS



WRITE MODE

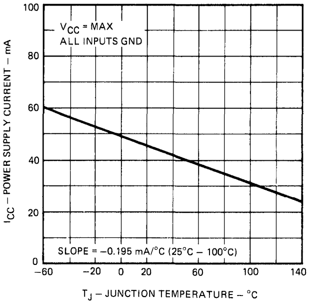


(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

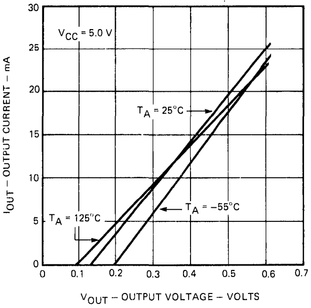
NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

TYPICAL ELECTRICAL CHARACTERISTICS

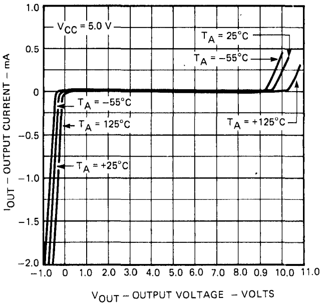
POWER SUPPLY CURRENT VERSUS TEMPERATURE



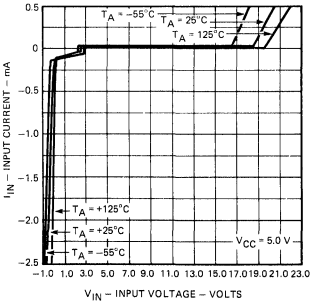
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)



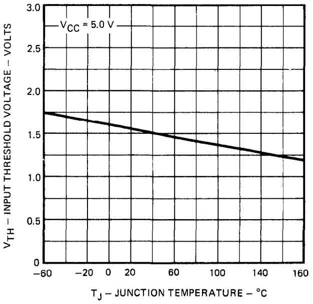
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



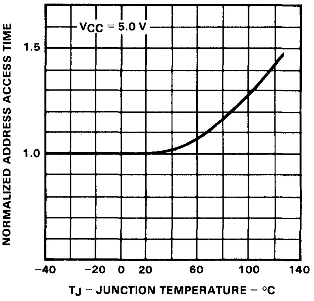
INPUT CURRENT VERSUS INPUT VOLTAGE



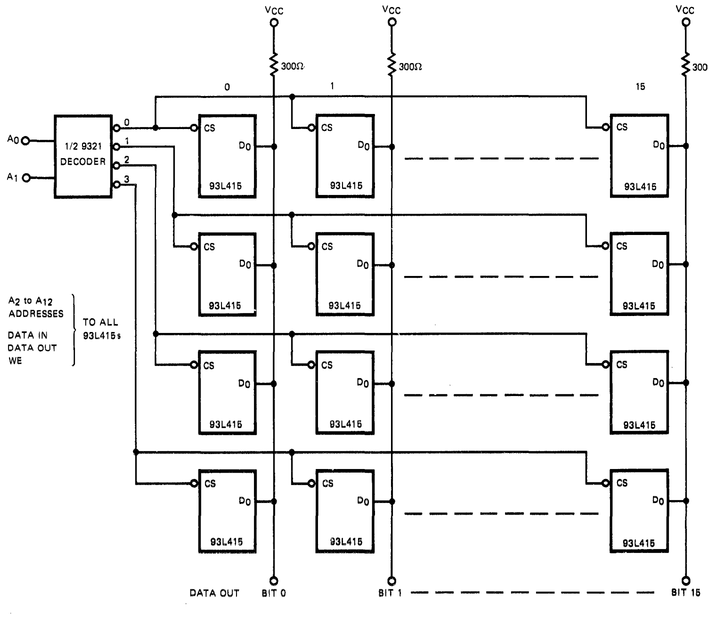
INPUT THRESHOLD VOLTAGE VERSUS TEMPERATURE



NORMALIZED ADDRESS ACCESS TIME VERSUS TEMPERATURE



APPLICATIONS



Addressing for a 4096-bit memory plane by 16 bits (4K x 16) requires only half of a 9321 1-of-4 decoder and any necessary buffers.

TTL ISOPLANAR MEMORY 93415/93415A

1024×1-BIT FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION – The 93415 and 93415A are 1024-bit Read/Write Random Access Memories organized 1024 words by one bit. They are designed for buffer control storage and high performance main memory applications. The devices have typical access times of 30 ns for the 93415 and 25 ns for the 93415A.

The 93415 and 93415A include full decoding on chip, separate Data Input and Data Output lines and an active LOW Chip Select. They are fully compatible with standard DTL and TTL logic families and have an uncommitted collector output for ease of memory expansion.

- **UNCOMMITTED COLLECTOR OUTPUT**
- **TTL INPUTS AND OUTPUT**
- **NON-INVERTING DATA OUTPUT**
- **ORGANIZED 1024 WORDS X 1 BIT**
- **TYPICAL READ ACCESS TIME**

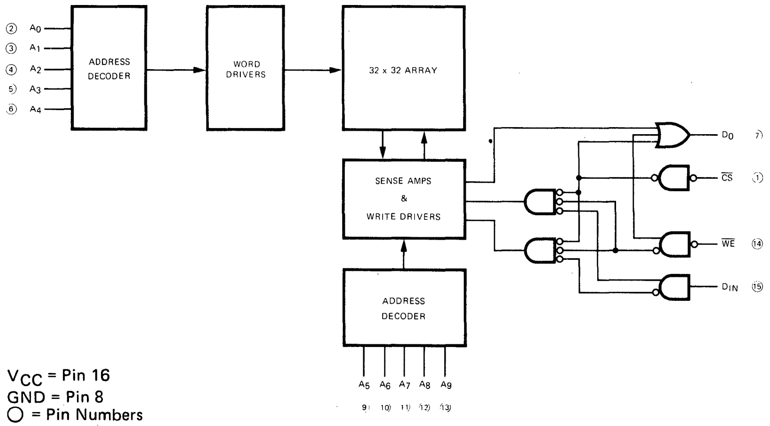
93415A	Commercial	25 ns
93415	Commercial	30 ns
93415	Military	40 ns

- **CHIP SELECT ACCESS TIME 15 ns TYPICAL**
- **POWER DISSIPATION 0.5 mW/BIT TYPICAL**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**

PIN NAMES

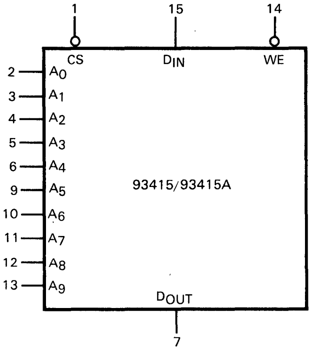
$\overline{CS}$	Chip Select
$A_0 - A_9$	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

LOGIC DIAGRAM



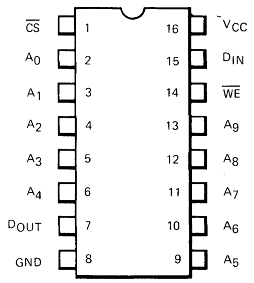
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP(TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The 93415/93415A are fully decoded 1024-bit Random Access Memories organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A_0 to A_9.

The Chip Select input provides for memory array expansion. For large memories, the fast chip select access time permits the decoding of **Chip Select (CS) from the address without affecting system performance.**

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$, Pin 14). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at D_{OUT} and is non-inverted.

Uncommitted collector outputs are provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93415s or 93415As can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of R_L value must be used to provide a HIGH at the output when it is off. Any R_L value within the range specified below may be used.

$$\frac{V_{CC}\,(\mathrm{MIN})}{I_{OL} - \mathrm{FO}\,(1.6)} \leq R_L \leq \frac{V_{CC}\,(\mathrm{MIN}) - V_{OH}}{n\,(I_{CEX}) + \mathrm{FO}\,(0.04)}$$

R_L is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output HIGH Level at Output Node
I_{OL} = Output LOW Current

The minimum R_L value is limited by output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}. One Unit Load = 40 μA HIGH/1.6 mA LOW.

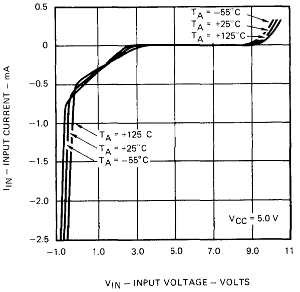
TABLE I – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	Open Collector	
H	X	X	H	NOT SELECTED
L	L	L	H	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

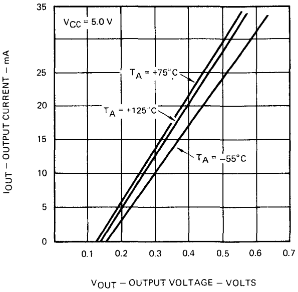
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5 V
Output Current (dc) (Output LOW)	+20 mA

*Either input voltage or input current limit is sufficient to protect the input.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE (T_A) (Note 4)
	MIN	TYP	MAX	
93415XC, 93415AXC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93415XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2, 4)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		MIN	TYP (Note 3)	MAX			
V_{OL}	Output LOW Voltage		0.3	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current		−250	−400	μA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
				1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
I_{CEX}	Output Leakage Current		1.0	100	μA	V_{CC} = MAX, V_{OUT} = 4.5 V	
V_{CD}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA	
I_{CC}	Power Supply Current		95	130	mA	$T_A \geqslant 75°C$	V_{CC} = MAX, All Inputs Grounded
				155	mA	$T_A = 0°C$	
				170	mA	$T_A = -55°C$	

AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

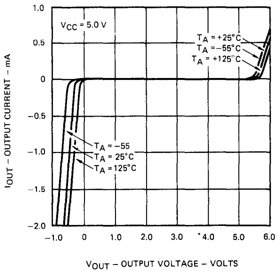
SYMBOL	CHARACTERISTIC	93415AXC			93415XC			93415XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES											
t_{ACS}	Chip Select Time		15	20		15	35		15	45	ns	See Test Circuit and Waveforms
t_{RCS}	Chip Select Recovery Time		15	20		20	35		20	50		
t_{AA}	Address Access Time		25	30		30	45		40	60		
WRITE MODE	DELAY TIMES											
t_{WS}	Write Disable Time		15	20		20	35		20	45	ns	See Test Circuit and Waveforms
t_{WR}	Write Recovery Time		20	25		25	40		45	50		
	INPUT TIMING REQUIREMENTS											
t_W	Write Pulse Width (to guarantee write)	20	15		30	25		40	25		ns	
t_{WSD}	Data Set-Up Time Prior to Write	5	0		5	0		5	0			
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0			
t_{WSA}	Address Set-Up Time	5	0		10	0		15	0			
t_{WHA}	Address Hold Time	5	0		5	0		5	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0		5	0			
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0			
C_I	Input Pin Capacitance		4	5		4	5		4	5	pF	
C_O	Output Pin Capacitance		7	8		7	8		7	8		

NOTES:

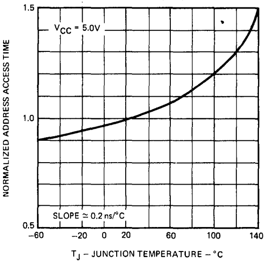
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.

TYPICAL ELECTRICAL CHARACTERISTICS

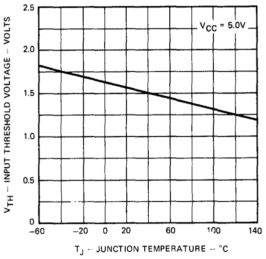
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



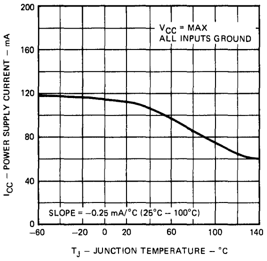
NORMALIZED ADDRESS ACCESS TIME VERSUS TEMPERATURE



INPUT THRESHOLD VOLTAGE VERSUS TEMPERATURE

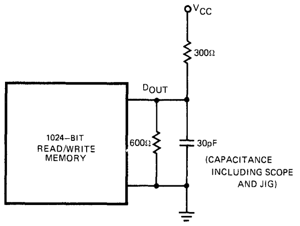


POWER SUPPLY CURRENT VERSUS TEMPERATURE

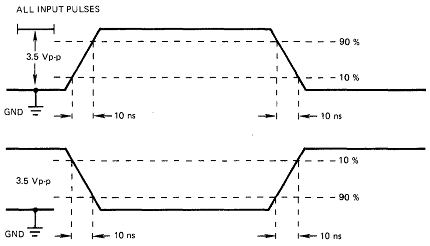


AC TEST LOAD AND WAVEFORM

LOADING CONDITION



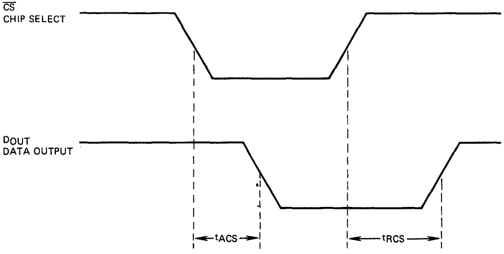
INPUT PULSES



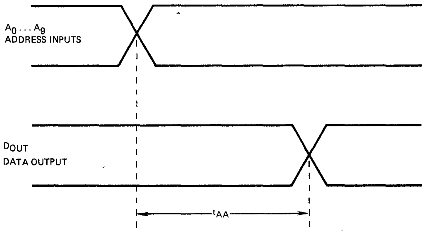
AC WAVEFORMS

READ MODE

PROPAGATION DELAY FROM CHIP SELECT



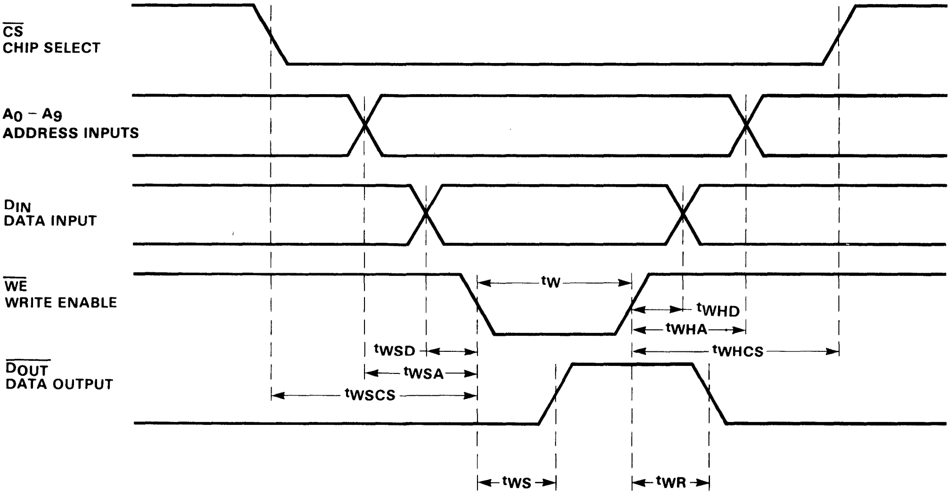
PROPAGATION DELAY FROM ADDRESS INPUTS



(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

AC WAVEFORMS (Cont'd)

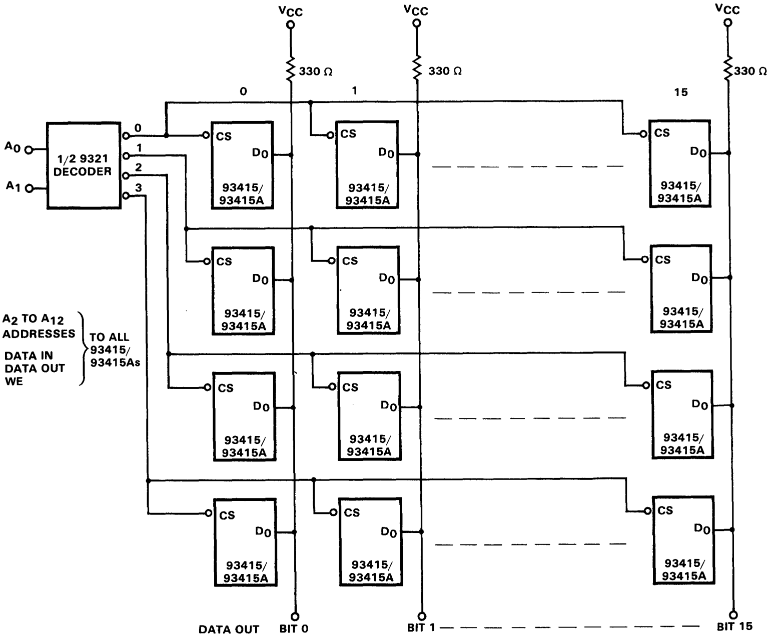
WRITE MODE



(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

APPLICATIONS



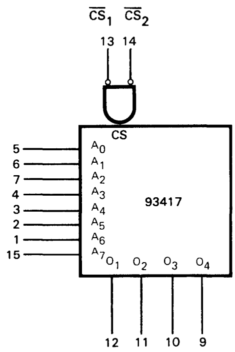
Addressing for a 4096-bit memory plane by 16 bits (4K by 16) requires only half of a 9321 1-of-4 decoder and any necessary buffers.

93417
ISOPLANAR SCHOTTKY TTL MEMORY
256×4-BIT PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION – The 93417 is a fully decoded high speed 1024-bit field Programmable ROM organized 256 words by four bits per word. The 93417 has uncommitted collector outputs. The outputs are disabled when either $\overline{CS}_1$ or $\overline{CS}_2$ are in the HIGH state. The 93417 is supplied with all bits stored as logic "1"s and can be programmed to logic "0"s by following the field programming procedure.

- **FULL MIL AND COMMERCIAL RANGES**
- **FIELD PROGRAMMABLE**
- **ORGANIZED 256 X 4 BITS PER WORD**
- **UNCOMMITTED COLLECTORS**
- **FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER**
- **CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION**
- **WIRED-OR CAPABILITY**
- **STANDARD 16-PIN DUAL IN-LINE PACKAGE**
- **NICHROME FUSE LINKS – FOR HIGH RELIABILITY**

LOGIC SYMBOL

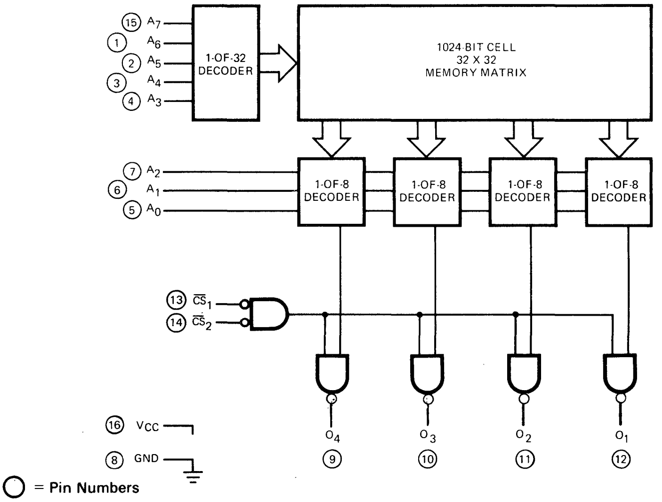


V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

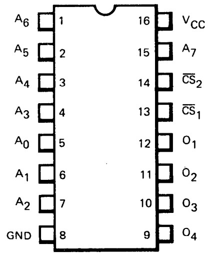
$A_0 - A_7$	Address Inputs
$\overline{CS}_1, \overline{CS}_2$	Chip Select Inputs (Active LOW)
$O_1 - O_4$	Data Outputs

LOGIC DIAGRAM



○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The 93417 is a bipolar field Programmable Read Only Memory (PROM) organized 256 words by four bits per word. Open collector outputs are provided for use in wired-OR systems. Chip Selects are active LOW; conversely, a HIGH (logic "1") on the $\overline{CS}_1$ or $\overline{CS}_2$ will disable all outputs.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_7 inputs, the chip is selected, and data is valid at the outputs after t_{AA} nanoseconds.

Programming (selectively opening nichrome fuse links) is accomplished by following the sequence outlined below.

PROGRAMMING – The 93417 is manufactured with all bits in the logic "1" state. Any desired bit (output) can be programmed to a logic "0" state by following the procedure shown in Chapter 6, page 6-16.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC}	−0.5 V to +7.0 V
Input Voltages	−0.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltages	−0.5 V to +5.5 V

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE
	MIN	TYP	MAX	
93417XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93417XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Package Information on this data sheet.

DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise noted.

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
I_{CEX}	Output Leakage Current			50	µA	V_{CC} = 5.25 V, V_{CEX} = 4.95 V, 0°C to +75°C Address any HIGH Output
I_{CEX}	Output Leakage Current			100	µA	V_{CC} = 5.5 V, V_{CEX} = 5.2 V, −55°C to +125°C Address any HIGH Output
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA, A_0 = +10.8 V A_1 through A_7 = HIGH
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
I_F	Input LOW Current					
	I_{FA} (Address Inputs)		−160	−250	µA	V_{CC} = MAX, V_F = 0.45 V
	I_{FCS} (Chip Select Inputs)		−160	−250	µA	
I_R	Input HIGH Current					
	I_{RA} (Address Inputs)			40	µA	V_{CC} = MAX, V_R = 2.4 V
	I_{RCS} (Chip Select Input)			40	µA	
I_{CC}	Power Supply Current		85	110	mA	V_{CC} = MAX, Outputs open Inputs Grounded and Chip Selected
C_O	Output Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
C_{IN}	Input Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
V_C	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_A = −18 mA

AC CHARACTERISTICS: T_A = 0°C to +75°C, V_{CC} = 5.0 V ± 5%.

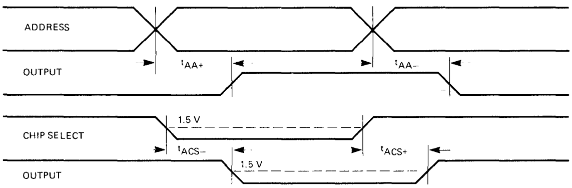
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-}	Address to Output Access Time		25	45	ns	See Figure 1
t_{AA+}			25	45	ns	
t_{ACS-}	Chip Select Access Time		12	20	ns	
t_{ACS+}			12	20	ns	

AC CHARACTERISTICS: T_A = −55°C to +125°C, V_{CC} = 5.0 V ± 10%.

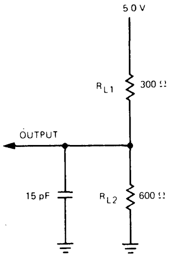
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-}	Address to Output Access Time		25	60	ns	See Figure 1
t_{AA+}			25	60	ns	
t_{ACS-}	Chip Select Access Time		12	30	ns	
t_{ACS+}			12	30	ns	

Note 1: Typical values are at V_{CC} = 5.0 V, +25°C and max loading.

AC WAVEFORMS



AC TEST OUTPUT LOAD



15 mA Load

Fig. 1

TTL ISOPLANAR MEMORY 93419

64×9-BIT FULLY DECODED RANDOM ACCESS MEMORY

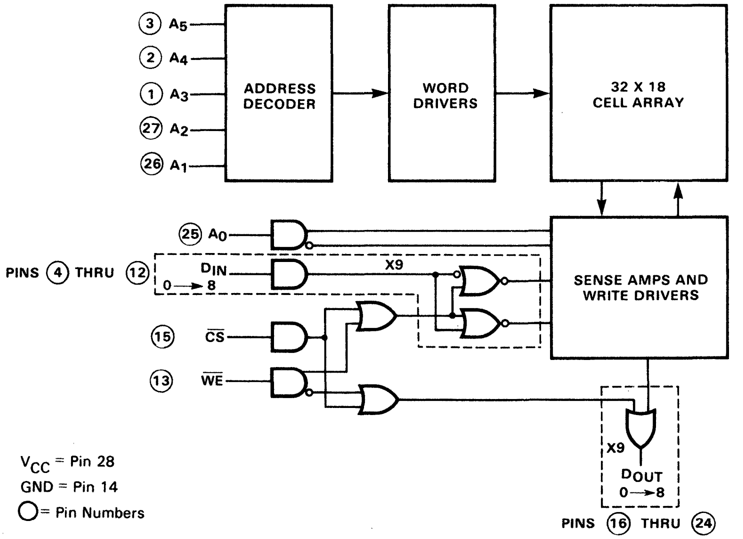
DESCRIPTION – The 93419 is a 576-bit Read/Write Random Access Memory organized 64 words by nine bits per word with uncommitted collector outputs. It is ideally suited for scratchpad, small buffer and other applications where the number of required words is small and where the number of required bits per word is relatively large. The ninth bit can provide parity for 8-bit word systems.

- **UNCOMMITTED COLLECTOR OUTPUTS**
- **TTL INPUTS AND OUTPUTS**
- **ISOPLANAR TECHNOLOGY**
- **ORGANIZATION – 64 WORDS X 9 BITS**
- **STANDARD 28-PIN DUAL IN-LINE PACKAGE**
- **DATA OUTPUT IS THE COMPLEMENT OF DATA INPUT**
- **POWER DISSIPATION – 1.3 mW/BIT**

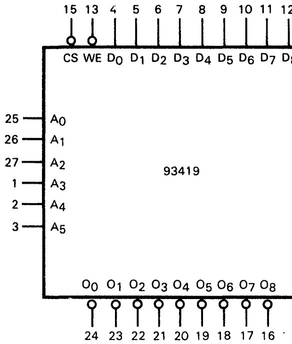
PIN NAMES

$A_0 - A_5$	Address Inputs
$D_0 - D_8$	Data Inputs
$\overline{O}_0 - \overline{O}_8$	Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input

LOGIC DIAGRAM

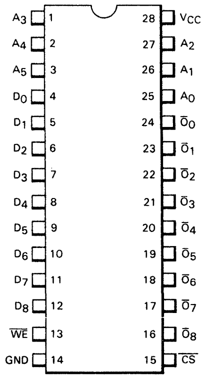


LOGIC SYMBOL



V_{CC} = Pin 28
GND = Pin 14

CONNECTION DIAGRAM
DIP (TOP VIEW)



FUNCTIONAL DESCRIPTION – The 93419 is a fully decoded 576-bit Random Access Memory organized 64 words by nine bits. Word selection is achieved by means of a 6-bit address, A_0 to A_5.

The Chip Select input provides for memory array expansion. For large memories, the fast chip select access time permits the decoding of chip select ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$, pin 13). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at $\overline{D_{OUT}}$ and is inverted from Data In to Data Out.

Uncommitted collector outputs are provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93419s can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of R_L value must be used to provide a HIGH at the output when it is off. Any R_L value within the range specified below may be used.

$$\frac{V_{CC}(MAX)}{I_{OL} - FO\,(1.6)} \leqslant R_L \leqslant \frac{V_{CC}\,(MIN) - V_{OH}}{n\,(I_{CEX}) + FO\,(0.04)}$$

R_L is in kΩ (limited to 8 mA)
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output HIGH Level at Output Node
I_{OL} = Output LOW Current

The minimum R_L value is limited by output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}. One Unit Load = 40 μA HIGH/1.6 mA LOW. FO_{MAX} = 5 UL.

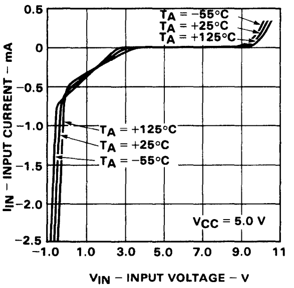
TABLE I – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	Open Collector	
H	X	X	H	NOT SELECTED
L	L	L	H	WRITE "0"*
L	L	H	H	WRITE "1"*
L	H	X	$\overline{D_{OUT}}$*	READ

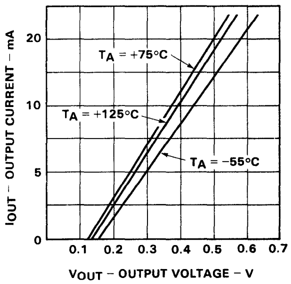
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)
* Memory inverts from Data In to Data Output

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5 V
Output Current (dc) (Output LOW)	+10 mA

*Either input voltage or input current limit is sufficient to protect the input.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE (Note 4)
	MIN	TYP	MAX	
93419XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93419XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2 and 4)

SYMBOL	PARAMETER	LIMITS MIN	TYP (Note 3)	MAX	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage		0.3	0.50	V	V_{CC} = MIN, I_{OL} = 8 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current		−250	−400	μA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
				1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
I_{CEX}	Output Leakage Current		1.0	100	μA	V_{CC} = MAX, V_{OUT} = 4.5 V	
V_{CD}	Input Clamp Diode Voltage		−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA	
I_{CC}	Power Supply Current			165	mA	T_A = 125°C	V_{CC} = MAX, All Inputs Grounded Outputs LOW
			145	200	mA	T_A = 25°C	
				210	mA	T_A = −55°C	

AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

SYMBOL	CHARACTERISTIC	93419XC MIN	93419XC TYP (Note 3)	93419XC MAX	93419XM MIN	93419XM TYP (Note 3)	93419XM MAX	UNITS	CONDITIONS
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Access Time		15	40		15	40	ns	See Test Circuit and Waveforms
t_{RCS}	Chip Select Recovery Time		20	40		20	40		
t_{AA}	Address Access Time		35	45		40	60		
WRITE MODE	DELAY TIMES								
t_{WS}	Write Disable Time		20	40		20	45	ns	
t_{WR}	Write Recovery Time		25	45		45	55		
	INPUT TIMING REQUIREMENTS								
t_W	Write Pulse Width (to guarantee write)	35	20		45	25		ns	See Test Circuit and Waveforms
t_{WSD}	Data Set-Up Time Prior to Write	5	0		5	0			
t_{WHD}	Data Hold Time After Write	5	0		5	0			
t_{WSA}	Address Set-Up Time	5	0		10	0			
t_{WHA}	Address Hold Time	5	0		5	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0			
t_{WHCS}	Chip Select Hold Time	5	0		5	0			
C_{IN}	Input Pin Capacitance		4	5		4	5	pF	
C_{OUT}	Output Pin Capacitance		7	8		7	8		

NOTES:

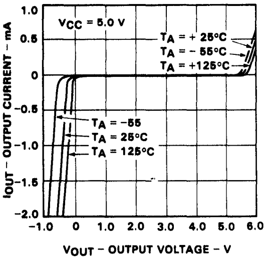
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°CC/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.

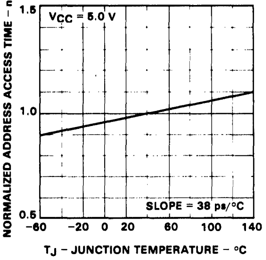
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.

TYPICAL ELECTRICAL CHARACTERISTICS

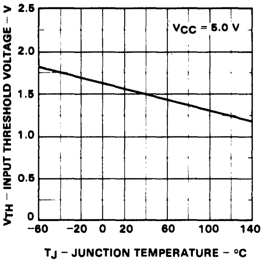
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



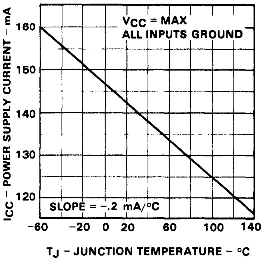
NORMALIZED ADDRESS ACCESS TIME VERSUS TEMPERATURE



INPUT THRESHOLD VOLTAGE VERSUS TEMPERATURE

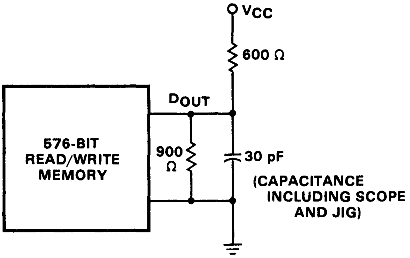


POWER SUPPLY CURRENT VERSUS TEMPERATURE

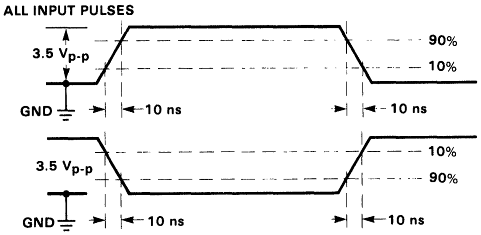


AC TEST LOAD AND WAVEFORM

LOADING CONDITION



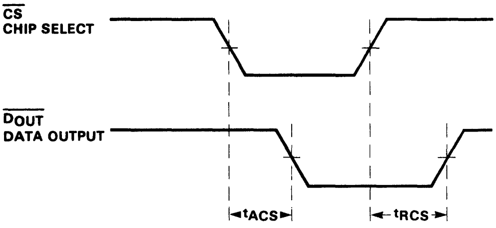
INPUT PULSES



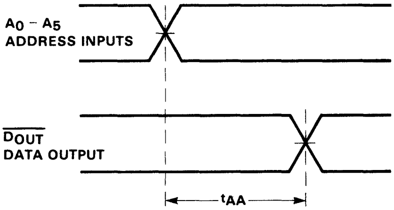
AC WAVEFORMS

READ MODE

PROPAGATION DELAY FROM CHIP SELECT



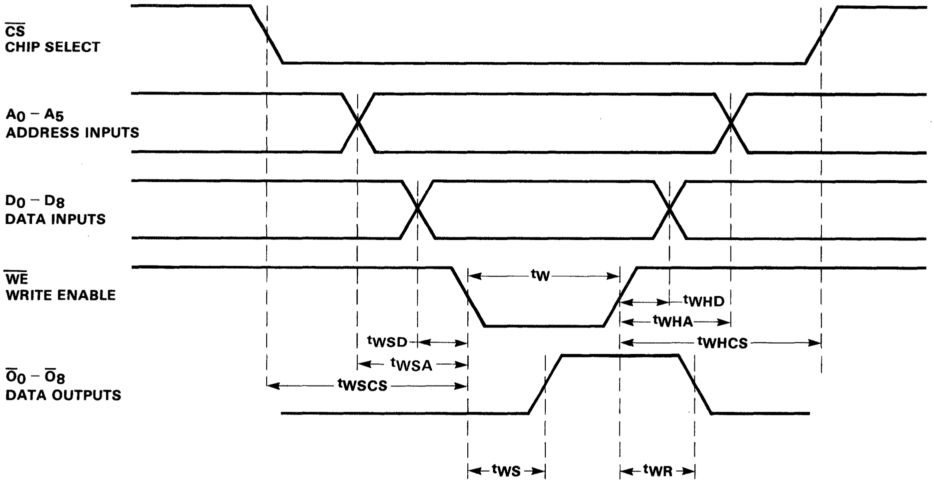
PROPAGATION DELAY FROM ADDRESS INPUTS



(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

AC WAVEFORMS (Cont'd)

WRITE MODE

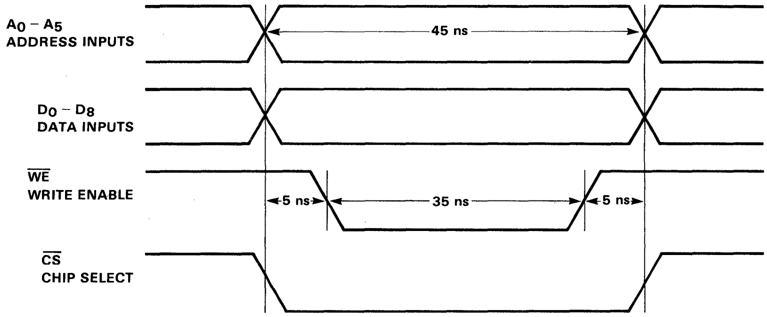


(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

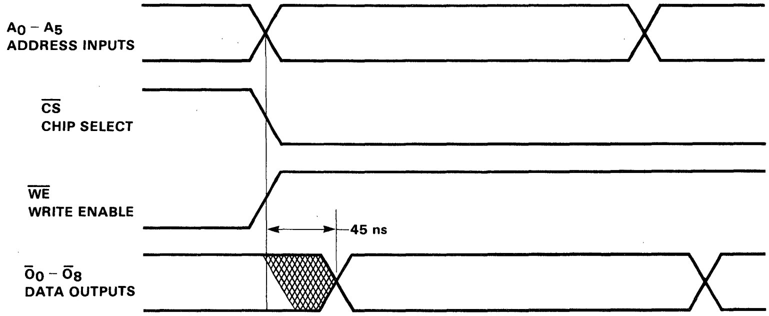
NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

TYPICAL SYSTEM TIMING

WRITE



READ



TTL ISOPLANAR MEMORY 93L420

256×1–BIT FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION – The 93L420 is a low power high speed 256-bit Read/Write Random Access Memory organized 256 words by one bit. It is designed for scratchpad, buffer and distributed main memory applications requiring low power. The device has three chip select lines to simplify its use in larger memory systems. Address input locations are specifically chosen to permit maximum packaging density and for ease of PC board layout. A 3-state output is provided to drive bus organized systems and/or highly capacitive loads.

- **3-STATE OUTPUT**
- **ORGANIZATION – 256 WORDS X 1 BIT**
- **THREE HIGH SPEED CHIP SELECT INPUTS**
- **TYPICAL READ ACCESS TIME – 40 ns**
- **ON-CHIP DECODING**
- **POWER DISSIPATION – 275 mW TYPICAL**
- **POWER DISSIPATION DECREASES WITH TEMPERATURE**
- **INVERTED DATA OUTPUT**

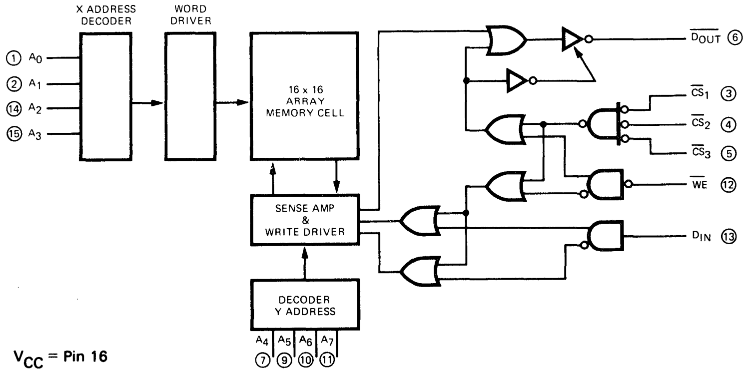
PIN NAMES		**LOADING (Notes a, b)**
$\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$	Chip Select Inputs	0.5 U.L.
$A_0 - A_7$	Address Inputs	0.5 U.L.
D_{IN}	Data Input	0.5 U.L.
$\overline{D}_{OUT}$	Data Output	10 U.L.
$\overline{WE}$	Write Enable	0.5 U.L.

NOTES:

a. 1 Unit Load (U.L.) = 40 μA HIGH / 1.6 mA LOW

b. 10 U.L. is the output LOW drive factor. This output will sink a maximum of 16 mA at V_{OUT} = 0.45 V, and will source a minimum of 10 mA at 2.4 V

LOGIC DIAGRAM

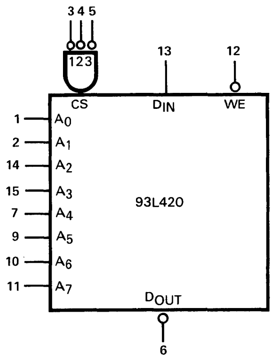


V_{CC} = Pin 16

GND = Pin 8

○ = Pin Numbers

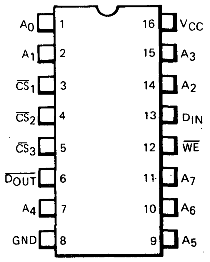
LOGIC SYMBOL



V_{CC} = Pin 16

GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The 93L420 is a fully decoded 256-bit Random Access Memory organized 256 words by one bit. Word selection is achieved by means of an 8-bit address, A_0 thru A_7.

Three Chip Select inputs are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of Chip Select, $\overline{CS}$, from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$, pin 12). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at $\overline{D}_{OUT}$.

The 3-state output provides drive capability for higher speeds with high capacitive load systems The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in the high impedance state.

TABLE I – TRUTH TABLE

INPUTS					OUTPUT	
$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_3$	$\overline{WE}$	D_{IN}	$\overline{D}_{OUT}$	MODE
H	X	X	X	X	HIGH Z	Not Selected
X	H	X	X	X	HIGH Z	Not Selected
X	X	H	X	X	HIGH Z	Not Selected
L	L	L	L	L	HIGH Z	Write "0"
L	L	L	L	H	HIGH Z	Write "1"
L	L	L	H	X	$\overline{D}_{OUT}$	Read inverted data from addressed location

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)
HIGH Z = HIGH Impedance

TABLE 2 – FUNCTION TABLE

FUNCTION	INPUTS		OUTPUT
	CHIP SELECT	WRITE ENABLE	
Write	L	L	HIGH Z
Read	L	H	Stored Data
Not Selected	H	X	HIGH Z

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
**Voltage Applied to Outputs (output HIGH)	−0.5 V to +5.50 V
Output Current (dc) (output LOW)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93L420XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93L420XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges. Notes 1, 2 and 4

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP (Note 3)	LIMITS MAX	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage			0.3	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage		2.0	1.6		V	Guaranteed Input Logical HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage			1.5	0.85	V	Guaranteed Input Logical LOW Voltage for all Inputs	
I_{IL}	Input LOW Current			−530	−800	μA	V_{CC} = MAX, V_{IN} = 0 V	
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
I_{OFF}	Output Current (HIGH Z)				50 −50	μA	V_{CC} = MAX, V_{OUT} = 2.4 V V_{CC} = MAX, V_{OUT} = 0.5 V	
V_{CD}	Input Clamp Diode Voltage			−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA	
I_{CC}	Power Supply Current	93L420XC		55	70	mA	T_A = 0°C to +75°C	V_{CC} = MAX, WE Grounded, all other inputs @ 4.5 V, see Power Supply vs Temp. Curve
		93L420XM		55	70		T_A = −55°C to +125°C	
V_{OH}	Output HIGH Voltage	93L420XC	2.4			V	I_{OH} = −10.3 mA	
		93L421XM	2.4			V	I_{OH} = −5.2 mA	
I_{OS}	Output Current Short Circuit to Ground				−100	mA	V_{CC} = MAX, Note 7	

AC CHARACTERISTICS: Over Guaranteed Operating Ranges. Notes 1, 2, 4, 5, 6

SYMBOL	CHARACTERISTIC	93L420XC MIN	93L420XC TYP (Note 3)	93L420XC MAX	93L420XM MIN	93L420XM TYP (Note 3)	93L420XM MAX	UNITS	CONDITIONS
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Access Time		20	25		20	40	ns	See Test Circuit and Waveforms Note 5
t_{ZRCS}	Chip Select to HIGH Z		25	30		25	40		
t_{AA}	Address Access Time		40	45		40	55		
WRITE MODE	DELAY TIMES								
t_{ZWS}	Write Disable to HIGH Z		25	30		25	40	ns	
t_{WR}	Write Recovery Time		45	50		45	55		
	INPUT TIMING REQUIREMENTS								
t_W	Minimum Write Pulse Width	35	15		40	15		ns	See Test Circuit and Waveforms Note 6
t_{WSD}	Data Set-Up Time Prior to Write	5	0		5	0			
t_{WHD}	Data Hold Time After Write	5	0		5	0			
t_{WSA}	Address Set-Up Time	5	0		10	0			
t_{WHA}	Address Hold Time	5	0		5	0			
t_{WSCS}	Chip Select Set-Up Time	0	0		0	0			
t_{WHCS}	Chip Select Hold Time	0	0		0	0			
C_{IN}	Input Capacitance		2.5	3.5		2.5	3.5	pF	Measured with a pulse technique
C_{OUT}	Output Capacitance		5	7		5	7		

NOTES:

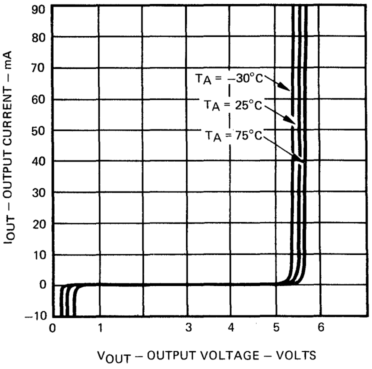
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.

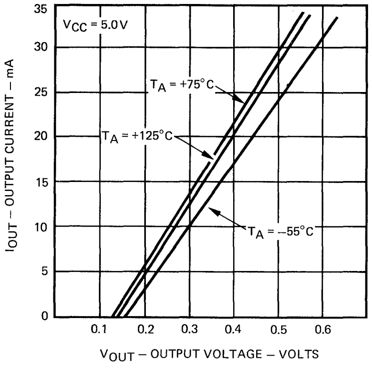
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.

TYPICAL ELECTRICAL CHARACTERISTIC CURVES

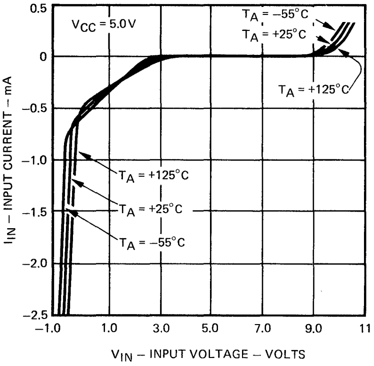
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH Z STATE)



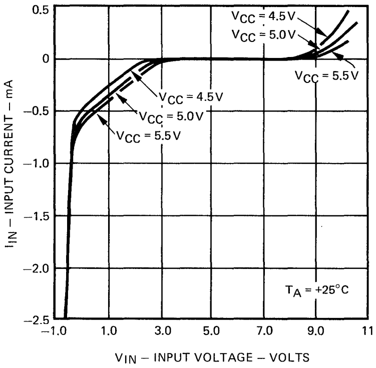
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS TEMPERATURE

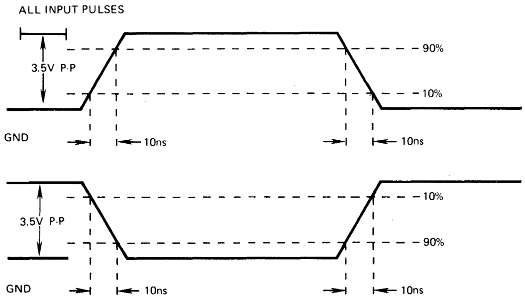


INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS SUPPLY VOLTAGE



AC TEST LOAD AND WAVEFORMS

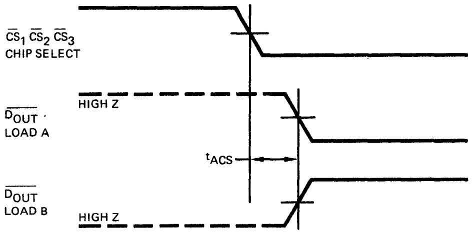
INPUT PULSES



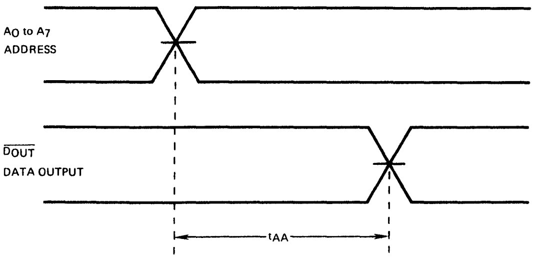
AC WAVEFORMS

READ MODE

PROPAGATION DELAY FROM CHIP SELECT

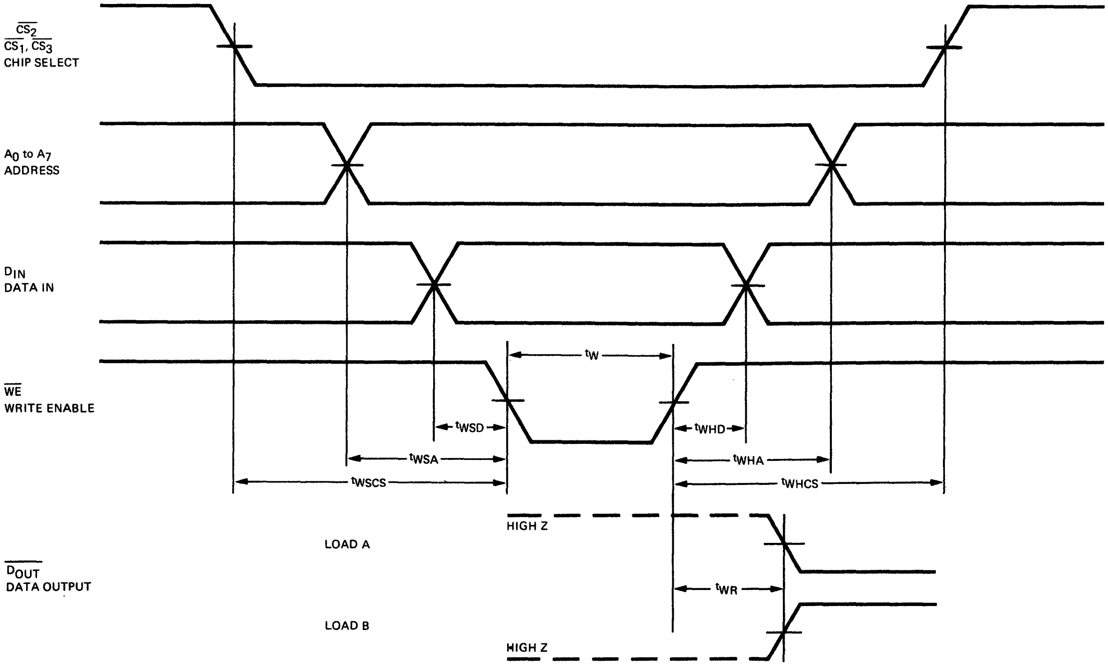


PROPAGATION DELAY FROM ADDRESS



(All time measurements referenced to 1.5 V)

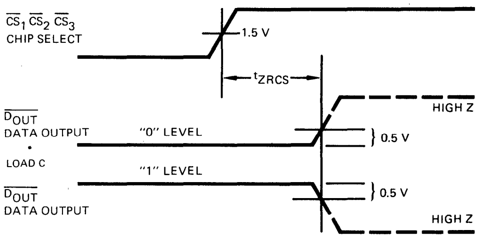
WRITE MODE



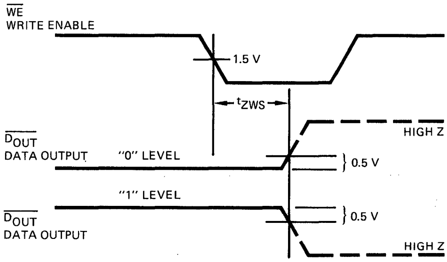
(All time measurements referenced to 1.5 V)

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z

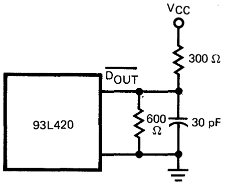


WRITE ENABLE TO HIGH Z DELAY

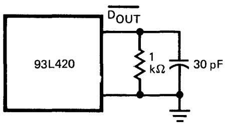


(All t_{ZXXX} parameters are measured at a delta of 0.5 V from the logic level and using Load C.)

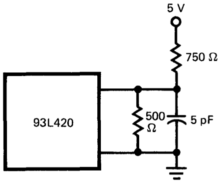
LOADING CONDITIONS



Load A



Load B



Load C

TTL ISOPLANAR MEMORY 93L421

256×1—BIT FULLY DECODED RANDOM ACCESS MEMORY

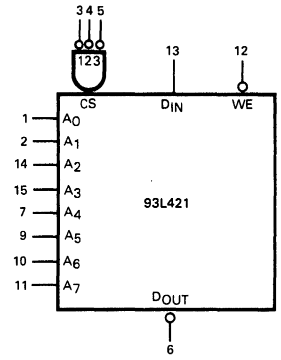
DESCRIPTION – The 93L421 is a low power 256-bit Read/Write Random Access Memory organized 256 words by one bit. It is designed for scratchpad, buffer and distributed main memory applications requiring low power. The device has three Chip Select lines to simplfy its use in larger memory systems. Address input locations are specifically chosen to permit maximum packaging density and for ease of PC board layout. A 3-state output is provided to drive bus organized systems and/or highly capacitive loads.

- **3-STATE OUTPUT**
- **ORGANIZATION – 256 WORDS X 1 BIT**
- **THREE HIGH SPEED CHIP SELECT INPUTS**
- **TYPICAL READ ACCESS TIME – 45 ns**
- **ON-CHIP DECODING**
- **POWER DISSIPATION – 275 mW TYPICAL**
- **POWER DISSIPATION DECREASES WITH TEMPERATURE**
- **INVERTED DATA OUTPUT**

PIN NAMES		**LOADING (Notes a, b)**
$\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$	Chip Select Inputs	0.5 U.L.
$A_0 - A_7$	Address Inputs	0.5 U.L.
D_{IN}	Data Input	0.5 U.L.
$\overline{D_{OUT}}$	Data Output	10 U.L.
$\overline{WE}$	Write Enable	0.5 U.L.

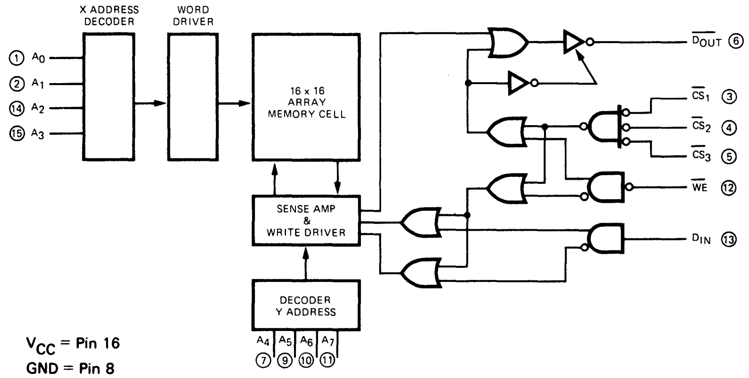
NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH / 1.6 mA LOW
b. 10 U.L. is the output LOW drive factor. This output will sink a maximum of 16 mA at $V_{OUT} = 0.45$ V, and will source a minimum of 10 mA at 2.4 V

LOGIC SYMBOL



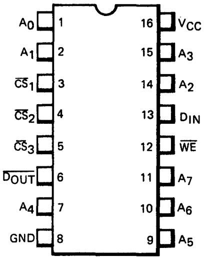
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The 93L421 is a fully decoded 256-bit Random Access Memory organized 256 words by one bit. Word selection is achieved by means of an 8-bit address, A_0 thru A_7.

Three Chip Select inputs are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of Chip Select, $\overline{CS}$, from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$, pin 12). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at $\overline{D_{OUT}}$.

The 3-state output provides drive capability for higher speeds with high capacitive load systems The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in the high impedance state.

TABLE I – TRUTH TABLE

INPUTS					OUTPUT	MODE
$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_3$	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	
H	X	X	X	X	HIGH Z	Not Selected
X	H	X	X	X	HIGH Z	Not Selected
X	X	H	X	X	HIGH Z	Not Selected
L	L	L	L	L	HIGH Z	Write "0"
L	L	L	L	H	HIGH Z	Write "1"
L	L	L	H	X	$\overline{D_{OUT}}$	Read inverted data from addressed location

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)
HIGH Z = HIGH Impedance

TABLE 2 – FUNCTION TABLE

FUNCTION	INPUTS		OUTPUT
	CHIP SELECT	WRITE ENABLE	
Write	L	L	HIGH Z
Read	L	H	Stored Data
Not Selected	H	X	HIGH Z

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
**Voltage Applied to Outputs (output HIGH)	−0.5 V to +5.50 V
Output Current (dc) (output LOW)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93L421XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93L421XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges. Notes 1, 2 and 4

SYMBOL	PARAMETER		LIMITS			UNITS	CONDITIONS
			MIN	TYP (Note 3)	MAX		
V_{OL}	Output LOW Voltage			0.3	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA
V_{IH}	Input HIGH Voltage		2.0	1.6		V	Guaranteed Input Logical HIGH Voltage for all Inputs
V_{IL}	Input LOW Voltage			1.5	0.85	V	Guaranteed Input Logical LOW Voltage for all Inputs
I_{IL}	Input LOW Current			−530	−800	μA	V_{CC} = MAX, V_{IN} = 0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 4.5 V
I_{OFF}	Output Current (HIGH Z)				50 −50	μA	V_{CC} = MAX, V_{OUT} = 2.4 V V_{CC} = MAX, V_{OUT} = 0.5 V
V_{CD}	Input Clamp Diode Voltage			−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA
I_{CC}	Power Supply Current	93L421XC		55	70	mA	T_A = 0°C to +75°C V_{CC} = MAX, WE Grounded, all other inputs @ 4.5 V, see Power Supply vs Temp. Curve
		93L421XM		55	70		T_A = −55°C to +125°C
V_{OH}	Output HIGH Voltage	93L421XC	2.4			V	I_{OH} = −10.3 mA
		93L421XM	2.4			V	I_{OH} = −5.2 mA
I_{OS}	Output Current Short Circuit to Ground				−100	mA	V_{CC} = MAX, Note 7

AC CHARACTERISTICS: Over Guaranteed Operating Ranges. Notes 1, 2, 4, 5, 6

SYMBOL	CHARACTERISTIC	93L421XC			93L421XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Access Time		30	40		35	50	ns	See Test Circuit and Waveforms Note 5
t_{ZRCS}	Chip Select to HIGH Z		30	40		30	50		
t_{AA}	Address Access Time		45	90		45	100		
WRITE MODE	DELAY TIMES								
t_{ZWS}	Write Disable to HIGH Z		30	45		30	55	ns	
t_{WR}	Write Recovery Time		50	60		65	70		
	INPUT TIMING REQUIREMENTS								
t_W	Minimum Write Pulse Width	60	20		70	20		ns	See Test Circuit and Waveforms Note 6
t_{WSD}	Data Set-Up Time Prior to Write	5	0		5	0			
t_{WHD}	Data Hold Time After Write	5	0		5	0			
t_{WSA}	Address Set-Up Time	10	0		15	0			
t_{WHA}	Address Hold Time	10	0		10	0			
t_{WSCS}	Chip Select Set-Up Time	0	0		0	0			
t_{WHCS}	Chip Select Hold Time	0	0		0	0			
C_{IN}	Input Capacitance		2.5	3.5		2.5	3.5	pF	Measured with a pulse technique
C_{OUT}	Output Capacitance		5	7		5	7		

NOTES:

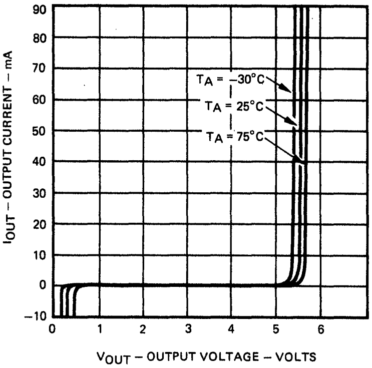
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.

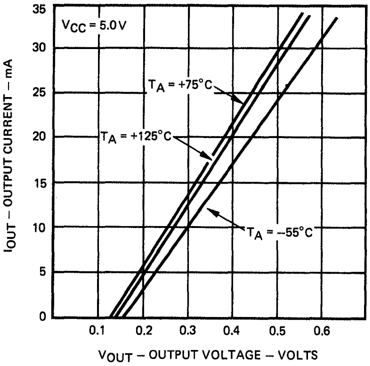
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.

TYPICAL ELECTRICAL CHARACTERISTICS

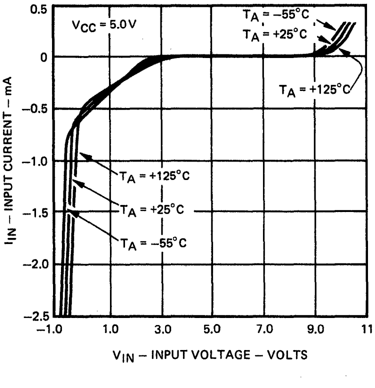
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH Z STATE)



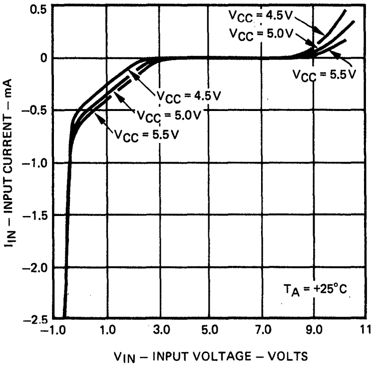
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS TEMPERATURE

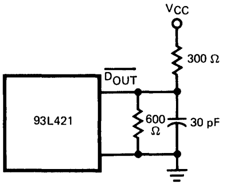


INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS SUPPLY VOLTAGE

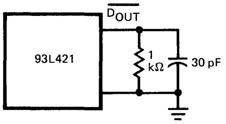


AC TEST LOAD AND WAVEFORM

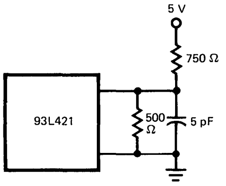
LOADING CONDITIONS



Load A

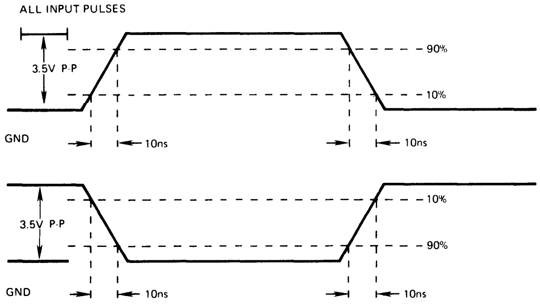


Load B



Load C

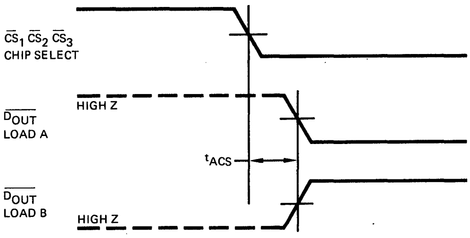
INPUT PULSES



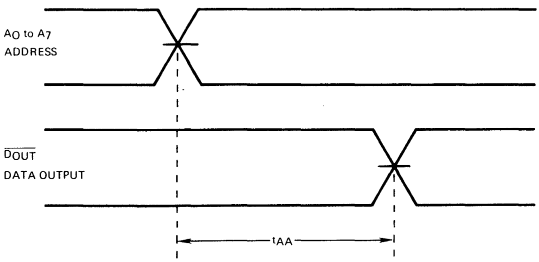
AC WAVEFORMS

READ MODE

PROPAGATION DELAY FROM CHIP SELECT



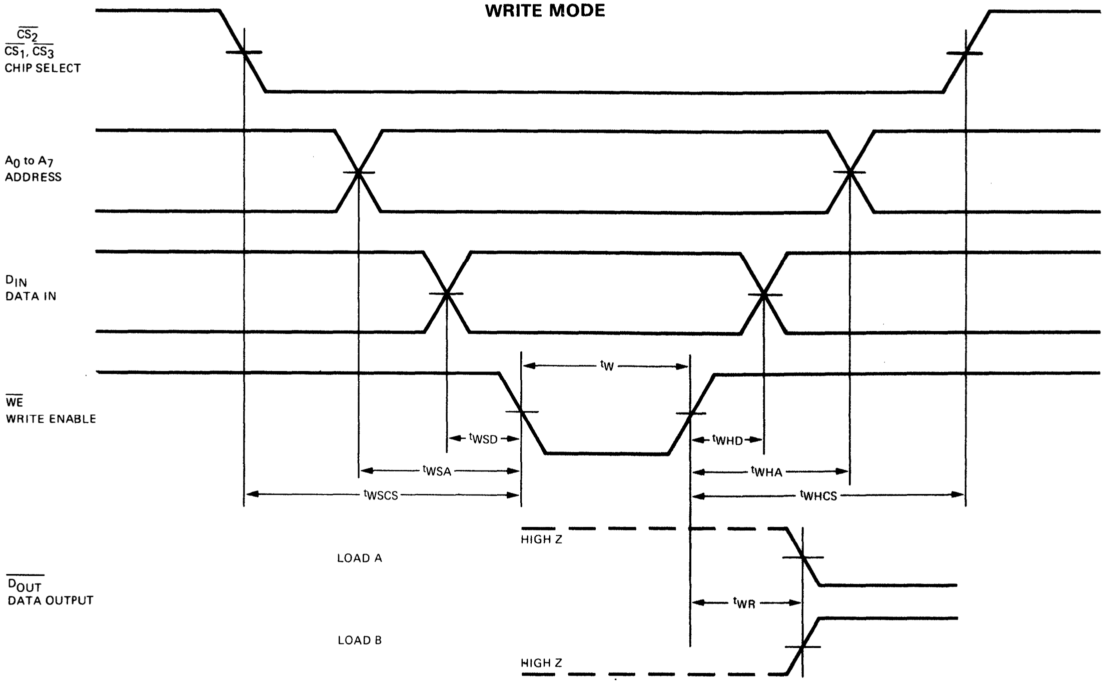
PROPAGATION DELAY FROM ADDRESS



(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

AC WAVEFORMS

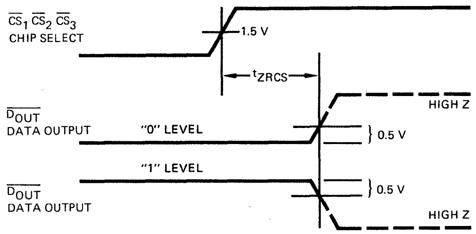
WRITE MODE



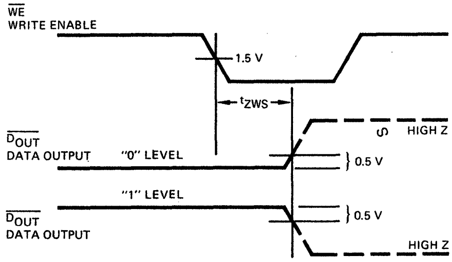
(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



WRITE ENABLE TO HIGH Z DELAY



(All t_{ZXXX} parameters are measured at a delta of 0.5 V from the logic level and using Load C.)

TTL ISOPLANAR MEMORY 93421/93421A

256×1—BIT FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION – The 93421 and 93421A are high speed 256-bit TTL Random Access Memories with full decoding on chip. They are organized 256 words by one bit and are designed for scratchpad, buffer and distributed main memory applications. The devices have three Chip Select lines to simplify their use in larger memory systems. Address input pin locations are specifically chosen to permit maximum packaging density and for ease of PC board layout. A 3-state output is provided to drive bus organized systems and/or highly capacitive loads.

- **3-STATE OUTPUT**
- **REPLACEMENT FOR 54/74S200 AND EQUIVALENT DEVICES**
- **ORGANIZATION – 256 WORDS X 1 BIT**
- **THREE HIGH SPEED CHIP SELECT INPUTS**
- **TYPICAL READ ACCESS TIME**

93421A	**Commercial**	**30 ns**
93421	**Commercial**	**35 ns**
93421	**Military**	**35 ns**

- **ON CHIP DECODING**
- **POWER DISSIPATION – 1.8 mW/BIT**
- **POWER DISSIPATION DECREASES WITH TEMPERATURE**
- **INVERTED DATA OUTPUT**

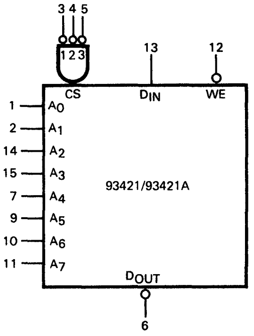
PIN NAMES		**LOADING (Notes a, b)**
$\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$	Chip Select Inputs	0.5 U.L.
$A_0 - A_7$	Address Inputs	0.5 U.L.
D_{IN}	Data Input	0.5 U.L.
$\overline{D_{OUT}}$	Data Output	10 U.L.
$\overline{WE}$	Write Enable	0.5 U.L.

NOTES:

a. 1 Unit Load (U.L.) = 40 μA HIGH / 1.6 mA LOW

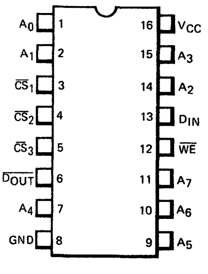
b. 10 U.L. is the output LOW drive factor. This output will sink a maximum of 16 mA at V_{OUT} = 0.45 V, and will source a minimum of 10 mA at 2.4 V.

LOGIC SYMBOL



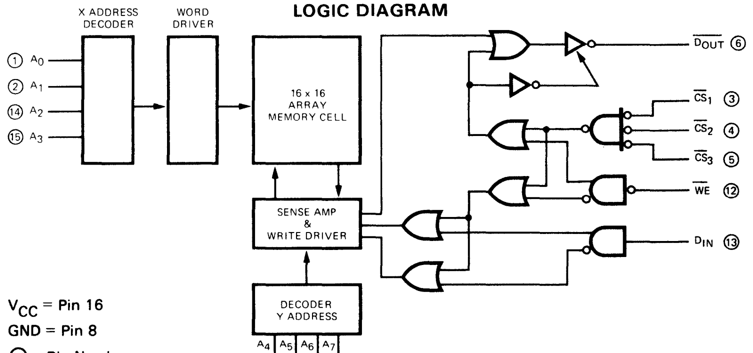
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The 93421/93421A are fully decoded 256-bit Random Access Memories organized 256 words by one bit. Word selection is achieved by means of an 8-bit address, A_0 thru A_7.

Three Chip Select inputs are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of Chip Select, $\overline{CS}$, from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$, pin 12). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at $\overline{D_{OUT}}$.

The 3-state output provides drive capability for higher speeds with high capacitive load systems. The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in the high impedance state.

TABLE I – TRUTH TABLE

INPUTS					OUTPUT	MODE
$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_3$	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	
H	X	X	X	X	HIGH Z	Not Selected
X	H	X	X	X	HIGH Z	Not Selected
X	X	H	X	X	HIGH Z	Not Selected
L	L	L	L	L	HIGH Z	Write "0"
L	L	L	L	H	HIGH Z	Write "1"
L	L	L	H	X	$\overline{D_{OUT}}$	Read inverted data from addressed location

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)
HIGH Z = HIGH Impedance

TABLE 2 – FUNCTION TABLE

FUNCTION	INPUTS		OUTPUT
	CHIP SELECT	WRITE ENABLE	
Write	L	L	HIGH Z
Read	L	H	$\overline{\text{Stored Data}}$
Not Selected	H	X	HIGH Z

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
**Voltage Applied to Outputs (output HIGH)	−0.5 V to +5.50 V
Output Current (dc) (output LOW)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93421AXC, 93421XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93421XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges. Notes 1, 2 and 4

SYMBOL	PARAMETER		LIMITS			UNITS	CONDITIONS	
			MIN	TYP (Note 3)	MAX			
V_{OL}	Output LOW Voltage			0.3	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage		2.0	1.6		V	Guaranteed Input Logical HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage			1.5	0.85	V	Guaranteed Input Logical LOW Voltage for all Inputs	
I_{IL}	Input LOW Current			−530	−800	μA	V_{CC} = MAX, V_{IN} = 0 V	
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
I_{OFF}	Output Current (HIGH Z)				50 −50	μA	V_{CC} = MAX, V_{OUT} = 2.4 V V_{CC} = MAX, V_{OUT} = 0.5 V	
V_{CD}	Input Clamp Diode Voltage			−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA	
I_{CC}	Power Supply Current	93421XC		90	124	mA	T_A = +75°C	V_{CC} = MAX, WE Grounded, all other inputs @ 4.5 V, see Power Supply vs Temp. Curve
		93421AXC		100	135		T_A = 0°C	
		93421XM		90	117		T_A = +125°C	
				100	143		T_A = −55°C	
V_{OH}	Output HIGH Voltage	93421XC,AXC	2.4			V	I_{OH} = −10.3 mA	
		93421XM	2.4			V	I_{OH} = −5.2 mA	
I_{OS}	Output Current Short Circuit to Ground				−100	mA	V_{CC} = MAX, Note 7	

AC CHARACTERISTICS: Over Guaranteed Operating Ranges. Notes 1, 2, 4, 5, 6

SYMBOL	CHARACTERISTIC	93421AXC			93421XC			93421XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES											
t_{ACS}	Chip Select Access Time		20	30		20	30		25	40	ns	See Test Circuit and Waveforms Note 5
t_{ZRCS}	Chip Select to HIGH Z		20	30		20	30		20	40		
t_{AA}	Address Access Time		30	40		35	50		35	60		
WRITE MODE	DELAY TIMES											
t_{ZWS}	Write Disable to HIGH Z	10	20	35	10	20	35	10	20	45	ns	
t_{WR}	Write Recovery Time		25	40		25	40		25	50		
	INPUT TIMING REQUIREMENTS											
t_W	Minimum Write Pulse Width	30	10		30	10		40	10		ns	See Test Circuit and Waveforms Note 6
t_{WSD}	Data Set-Up Time Prior to Write	0	0		0	0		0	0			
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0			
t_{WSA}	Address Set-Up Time	0	0		0	0		0	0			
t_{WHA}	Address Hold Time	5	0		5	0		5	0			
t_{WSCS}	Chip Select Set-Up Time	0	0		0	0		0	0			
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0			
C_I	Input Capacitance		2.5	3.5		2.5	3.5		2.5	3.5	pF	Measured with pulse technique
C_O	Output Capacitance		5	7		5	7		5	7		

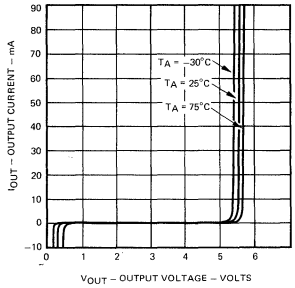
NOTES:

1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:

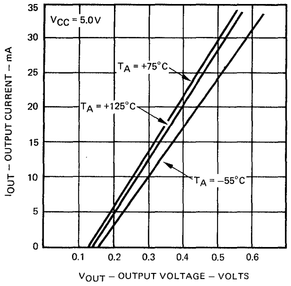
   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.

TYPICAL ELECTRICAL CHARACTERISTICS

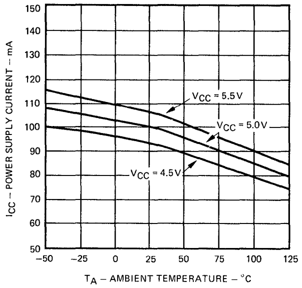
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH Z STATE)



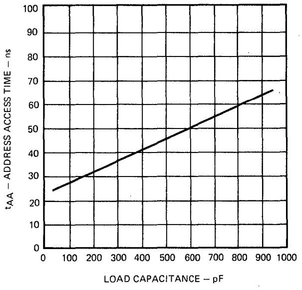
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



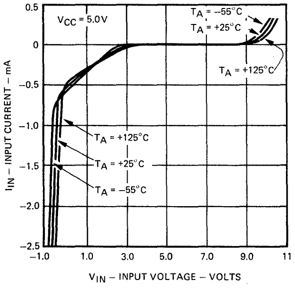
POWER SUPPLY CURRENT VERSUS TEMPERATURE



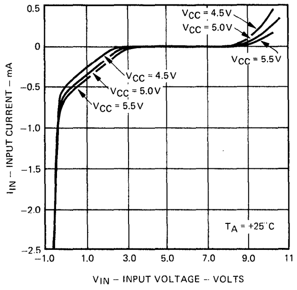
ADDRESS ACCESS TIME VERSUS LOAD CAPACITANCE



INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS TEMPERATURE

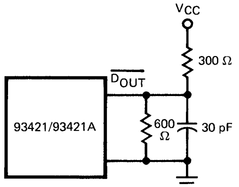


INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS SUPPLY VOLTAGE

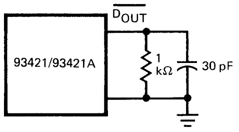


AC TEST LOAD AND WAVEFORM

LOADING CONDITION

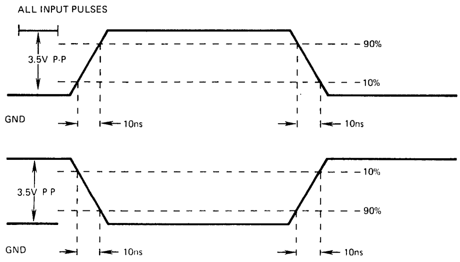


Load A



Load B

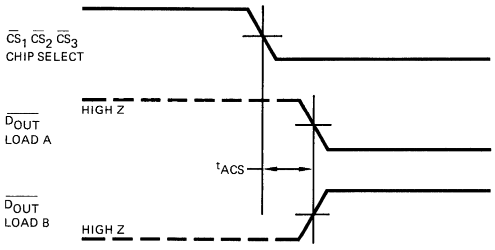
INPUT PULSES



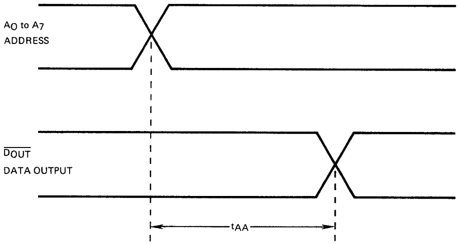
AC WAVEFORMS

READ MODE

PROPAGATION DELAY FROM CHIP SELECT

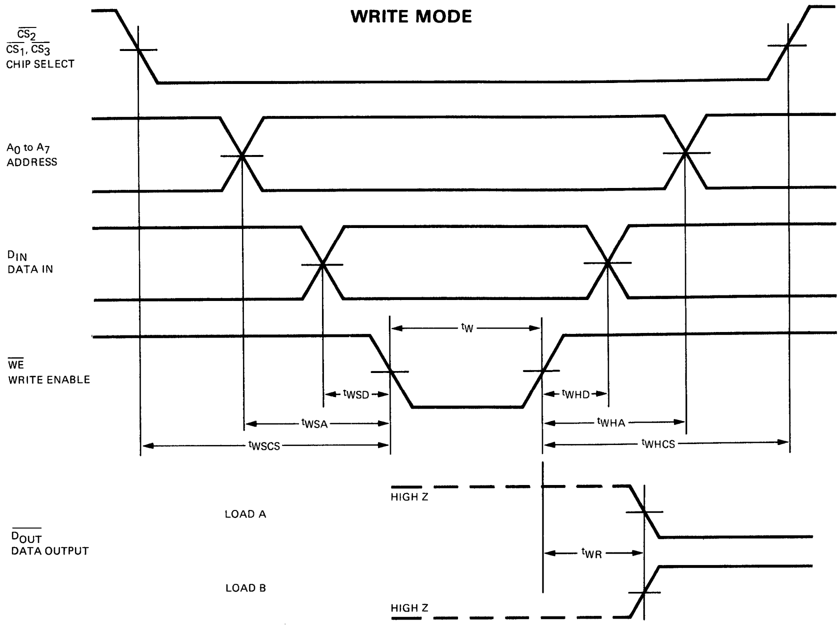


PROPAGATION DELAY FROM ADDRESS



(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

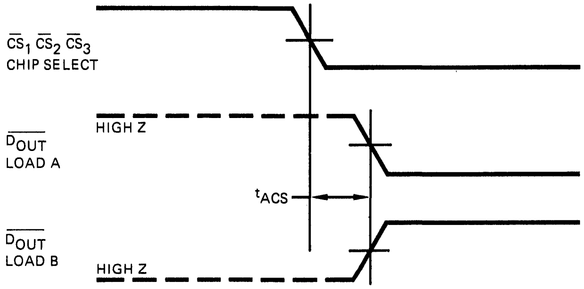
WRITE MODE

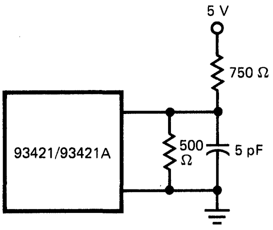


(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

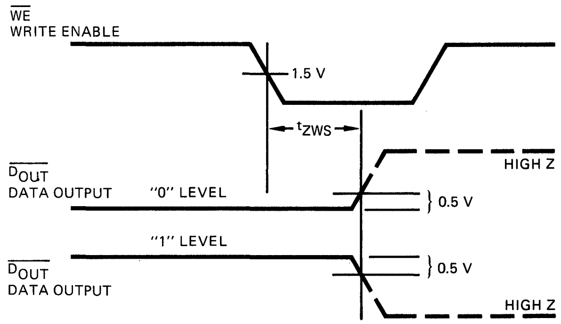
PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z





Load C

WRITE ENABLE TO HIGH Z DELAY



(All t_{ZXXX} parameters are measured at a delta of 0.5 V from the logic level and using Load C.)

TTL ISOPLANAR MEMORY 93L422

256×4-BIT FULLY DECODED RANDOM ACCESS MEMORY

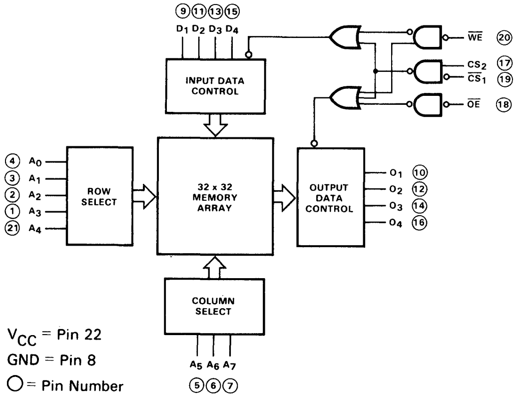
DESCRIPTION – The 93L422 is a 1024-bit Read/Write Random Access Memory organized 256 words by four bits per word. The 93L422 has 3-state outputs, and is designed primarily for buffer control storage and high performance main memory applications. The device has a typical address access time of 45 ns.

- **ISOPLANAR TECHNOLOGY**
- **ORGANIZATION – 256 WORDS X 4 BITS**
- **3-STATE OUTPUTS**
- **STANDARD 22-PIN DUAL IN-LINE PACKAGE**
- **TWO CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION**
- **LOW POWER DISSIPATION – 0.27 mW/BIT TYP**
- **TYPICAL READ ACCESS TIME – 45 ns**

PIN NAMES

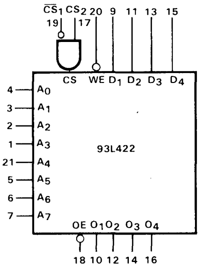
$A_0 - A_7$	Address Inputs
$D_1 - D_4$	Data Inputs
$\overline{CS}_1$, CS_2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
$O_1 - O_4$	Data Outputs
$\overline{OE}$	Output Enable

LOGIC DIAGRAM



V_{CC} = Pin 22
GND = Pin 8
○ = Pin Number

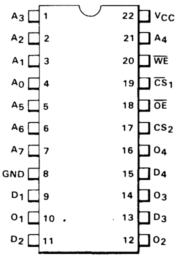
LOGIC SYMBOL



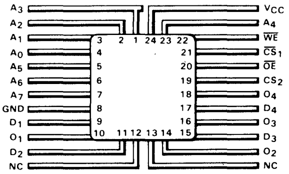
V_{CC} = Pin 22
GND = Pin 8

CONNECTION DIAGRAMS

DIP (TOP VIEW)



FLATPAK (TOP VIEW)



FUNCTIONAL DESCRIPTION – The 93L422 is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A_0 thru A_7.

Two Chip Select inputs are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of Chip Select, CS, from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable, WE (pin 20). With WE held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, WE is held HIGH and the chip selected. Data in the specified location is presented at D_{OUT}.

TRUTH TABLE

INPUTS					OUTPUTS	MODE
$\overline{OE}$ PIN 18	$\overline{CS}_1$ PIN 19	CS_2 PIN 17	$\overline{WE}$ PIN 20	$D_1 - D_4$ PINS 9, 11, 13 15	93L422 3-STATE	
X	H	X	X	X	HIGH Z	Not Selected
X	X	L	X	X	HIGH Z	Not Selected
L	L	H	H	X	$O_1 - O_4$	Read Stored Data
X	L	H	L	L	HIGH Z	Write "0"
X	L	H	L	H	HIGH Z	Write "1"
H	L	H	H	X	HIGH Z	Output Disabled
H	L	H	L	L	HIGH Z	Write "0" (Output Disabled)
H	L	H	L	H	HIGH Z	Write "1" (Output Disabled)

H = HIGH Voltage; L = LOW Voltage; X = Don't Care (HIGH or LOW); HIGH Z = HIgh Impedance.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Lead Potential to Ground Lead	−0.5 V to +7.0 V
Input Voltage (dc)*	−0.5 V to +5.5 V
Input Current (dc)*	−12 mA to +5.0 mA
Voltage Applied to Outputs (output HIGH)**	−0.5 V to +5.50 V
Output Current (dc)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93L422XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93L422XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2, 4)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		MIN	TYP (Note 3)	MAX			
V_{OL}	Output LOW Voltage		0.3	0.45	V	V_{CC} = MIN, I_{OL} = 8 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current		−150	−300	μA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
				1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
V_{CD}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = MAX, IN = −10 mA	
I_{OFF}	Output Current (HIGH Z)			50	μA	V_{CC} = MAX, V_{OUT} = 2.4 V	
				−50		V_{CC} = MAX, V_{OUT} = 0.5 V	
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = MIN, I_{OH} = −5.2 mA	
I_{OS}	Output Current Short Circuit to Ground			−70	mA	V_{CC} = MAX, Note 7	
I_{CC}	Power Supply Current 93L422XC		55	75	mA	T_A = +75°C	V_{CC} = MAX, All Inputs and Outputs Open
	93L422XC		60	80		T_A = 0°C	
	93L422XM		50	70		T_A = +125°C	
	93L422XM		65	90		T_A = −55°C	

AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

SYMBOL	CHARACTERISTIC	93L422XC*			93L422XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Time		20	35		20	45		
t_{ZRCS}	Chip Select to HIGH Z		20	35		20	45	ns	See Test Circuit and Waveforms
t_{AOS}	Output Enable Time		20	35		20	45		
t_{ZROS}	Output Enable to HIGH Z		20	35		20	45		
t_{AA}	Address Access Time		45	60		45	75		
WRITE MODE	DELAY TIMES								
t_{ZWS}	Write Disable to HIGH Z		20	40		20	45	ns	
t_{WR}	Write Recovery Time		25	45		25	50		
	INPUT TIMING REQUIREMENTS								See Test Circuit and Waveforms
t_W	Write Pulse Width (to guarantee write)	45	30		55	35			
t_{WSD}	Data Set-Up Time Prior to Write	5	0		5	0			
t_{WHD}	Data Hold Time After Write	5	0		5	0			
t_{WSA}	Address Set-Up Time	10	0		10	0		ns	
t_{WHA}	Address Hold Time	5	0		10	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0			
t_{WHCS}	Chip Select Hold Time	5	0		10	0			
C_I	Input Pin Capacitance		3	5		3	5	pF	Measure with Pulse Technique
C_O	Output Pin Capacitance		5	8		5	8		

NOTES:

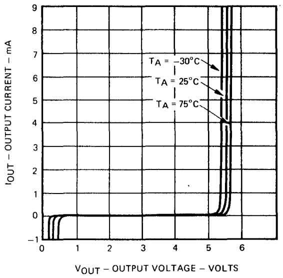
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°CC/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.

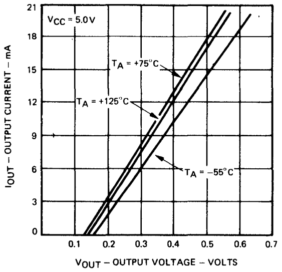
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.

TYPICAL ELECTRICAL CHARACTERISTIC CURVES

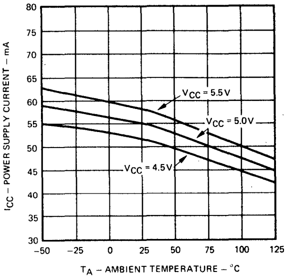
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH Z STATE)



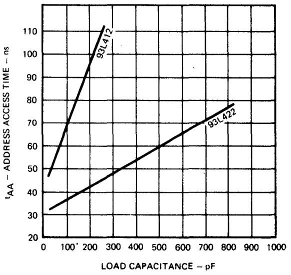
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



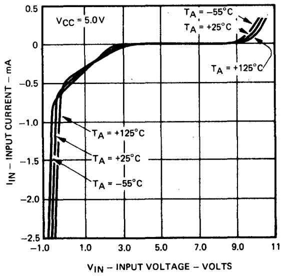
POWER SUPPLY CURRENT VERSUS TEMPERATURE



ADDRESS ACCESS TIME VERSUS LOAD CAPACITANCE

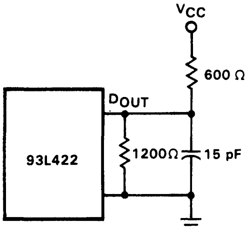


INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS TEMPERATURE

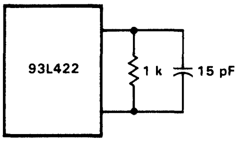


AC TEST LOAD AND WAVEFORM

LOADING CONDITIONS

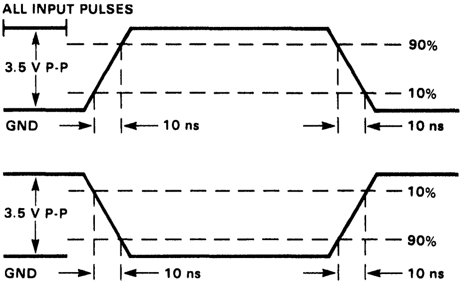


Load A

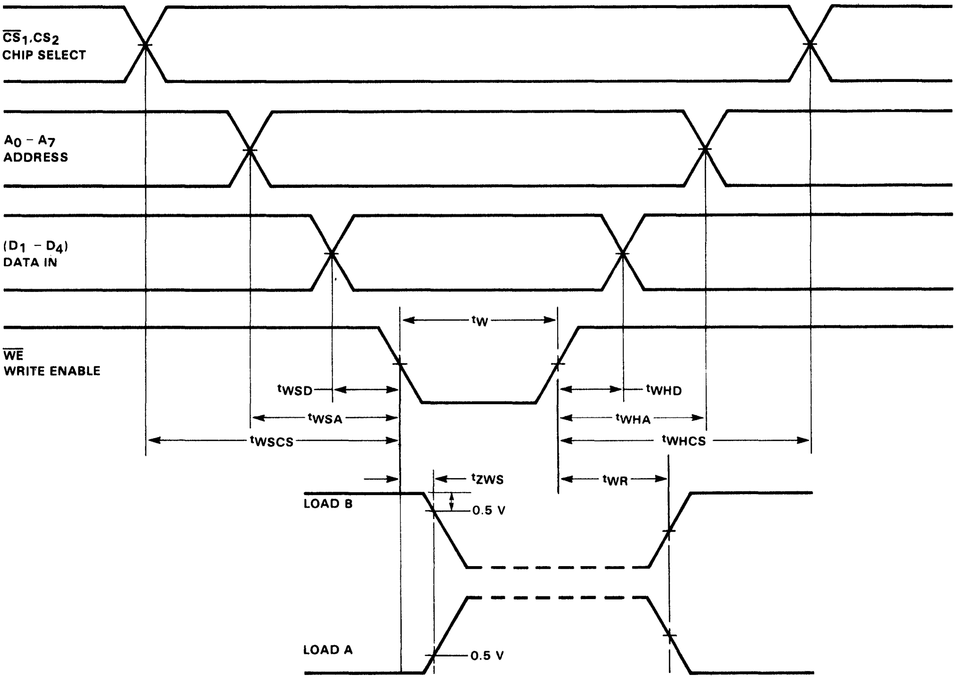


Load B

INPUT PULSES



WRITE MODE

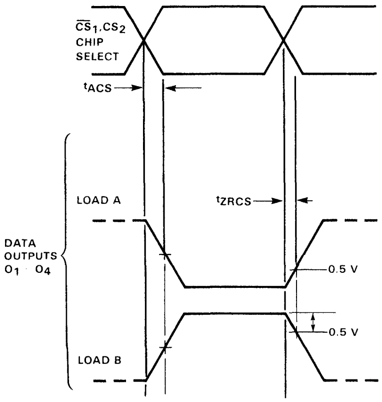


(All above measurements referenced to 1.5 V unless otherwise indicated)

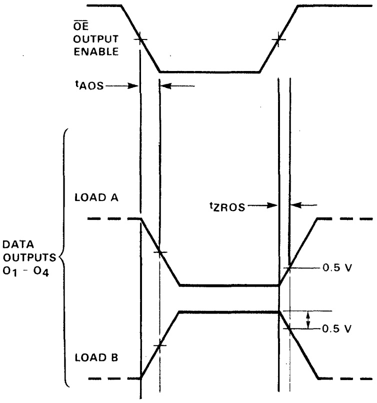
NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

READ MODE

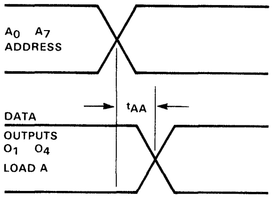
PROPAGATION DELAY FROM CHIP SELECT



PROPAGATION DELAY FROM OUTPUT ENABLE



PROPAGATION DELAY FROM ADDRESS INPUTS



93422

TTL ISOPLANAR MEMORY

256 × 4-BIT FULLY DECODED RANDOM ACCESS MEMORY

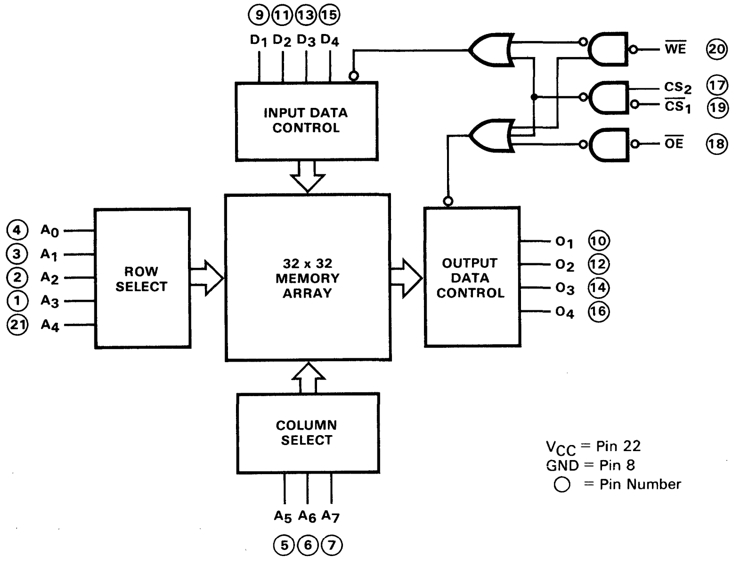
DESCRIPTION – The 93422 is a 1024-bit Read/Write Access Memory organized 256 words by four bits per word. The 93422 has 3-state outputs, and is designed primarily for buffer control storage and high performance main memory applications. The device has a typical address access time of 30 ns.

- **ISOPLANAR TECHNOLOGY**
- **ORGANIZATION – 256 WORDS X 4 BITS**
- **3-STATE OUTPUTS**
- **STANDARD 22-PIN DUAL IN-LINE PACKAGE**
- **TWO CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION**
- **POWER DISSIPATION – 0.475 mW/BIT TYPICAL**
- **TYPICAL READ ACCESS TIME – 30 ns**

PIN NAMES

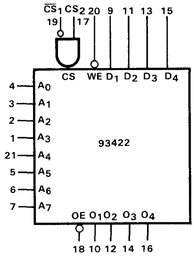
$A_0 - A_7$	Address Inputs
$D_1 - D_4$	Data Inputs
$\overline{CS_1}$, CS_2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
$O_1 - O_4$	Data Outputs
$\overline{O_E}$	Output Enable

LOGIC DIAGRAM



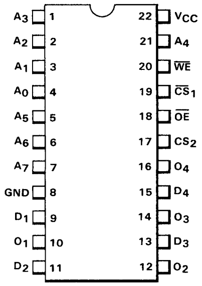
V_{CC} = Pin 22
GND = Pin 8
○ = Pin Number

LOGIC SYMBOL

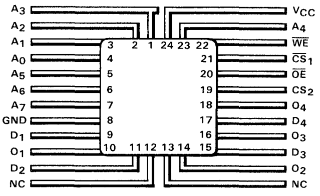


V_{CC} = Pin 22
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



FUNCTIONAL DESCRIPTION – The 93422 is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A_0 thru A_7.

Two Chip Select inputs are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of Chip Select, CS, from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable, WE (pin 20). With WE held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, WE is held HIGH and the chip selected. Data in the specified location is presented at D_{OUT}.

TRUTH TABLE

INPUTS					OUTPUTS	
$\overline{OE}$ PIN 18	$\overline{CS_1}$ PIN 19	CS_2 PIN 17	$\overline{WE}$ PIN 20	$D_1 - D_4$ PINS 9, 11,13, 15	93422 3-STATE	MODE
X	H	X	X	X	HIGH Z	Not Selected
X	X	L	X	X	HIGH Z	Not Selected
L	L	H	H	X	$O_1 - O_4$	Read Stored Data
X	L	H	L	L	HIGH Z	Write "0"
X	L	H	L	H	HIGH Z	Write "1"
H	L	H	H	X	HIGH Z	Output Disabled
H	L	H	L	L	HIGH Z	Write "0" (Output Disabled)
H	L	H	L	H	HIGH Z	Write "1" (Output Disabled)

H = HIGH Voltage, L = LOW Voltage, X = Don't Care (HIGH or LOW); HIGH Z = High Impedance.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
**Voltage Applied to Outputs (output HIGH)	−0.5 V to +5.50 V
Output Current (dc)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93422XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93422XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2, 4)

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 3)	LIMITS MAX	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage		0.3	0.45	V	V_{CC} = MIN, I_{OL} = 8 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current		−150	−300	µA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	40	µA	V_{CC} = MAX, V_{IN} = 4.5 V	
				1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
V_{CD}	Input Diode Clamp Voltage		−10	−1.5	V	V_{CC} = MAX, IN = −10 mA	
I_{OFF}	Output Current (HIGH Z)			50	µA	V_{CC} = MAX, V_{OUT} = 2.4 V	
				−50		V_{CC} = MAX, V_{OUT} = 0.5 V	
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = MIN, I_{OH} = −5.2 mA	
IOS	Output Current Short Circuit to Ground			−70	mA	V_{CC} = MAX, Note 7	
I_{CC}	Power Supply Current 93422XC		95	130	mA	T_A = +75°C	V_{CC} = MAX, All Inputs and Outputs Open
	93422XC			155		T_A = 0°C	
	93422XM			120		T_A = +125°C	
	93422XM			170		T_A = −55°C	

AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

SYMBOL	CHARACTERISTIC	93422XC MIN	93422XC TYP (Note 3)	93422XC MAX	93422XM MIN	93422XM TYP (Note 3)	93422XM MAX	UNITS	CONDITIONS
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Time		20	30		20	45	ns	See Test Circuit and Waveforms
t_{ZRCS}	Chip Select to HIGH Z		20	30		20	45		
t_{AOS}	Output Enable Time		20	30		20	45		
t_{ZROS}	Output Enable to HIGH Z		20	30		20	45		
t_{AA}	Address Access Time		30	45		40	60		
WRITE MODE	DELAY TIMES								
t_{ZWS}	Write Disable to HIGH Z		20	35		20	45	ns	See Test Circuit and Waveforms
t_{WR}	Write Recovery Time		25	40		25	50		
	INPUT TIMING REQUIREMENTS								
t_W	Write Pulse Width (to guarantee write)	30	20		40	30		ns	
t_{WSD}	Data Set-Up Time Prior to Write	5	0		5	0			
t_{WHD}	Data Hold Time After Write	5	0		5	0			
t_{WSA}	Address Set-Up Time	10	0		10	0			
t_{WHA}	Address Hold Time	5	0		10	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0			
t_{WHCS}	Chip Select Hold Time	5	0		10	0			
C_I	Input Pin Capacitance		3	5		3	5	pF	Measure with Pulse Technique
C_O	Output Pin Capacitance		5	8		5	8		

NOTES:

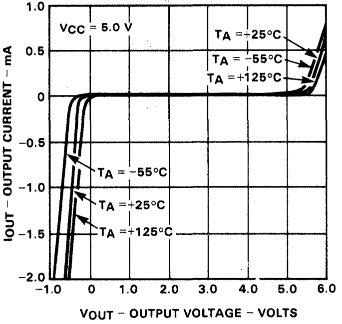
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.

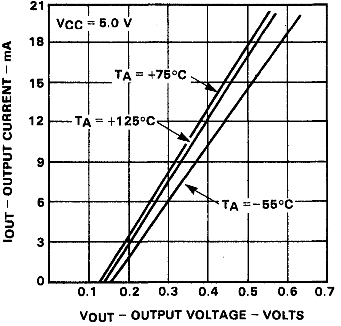
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.

TYPICAL ELECTRICAL CHARACTERISTIC CURVES

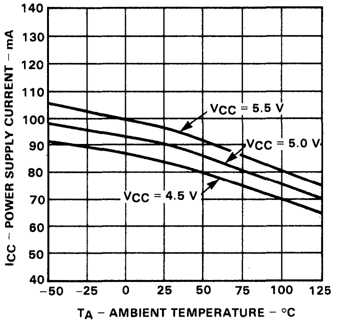
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH Z STATE)



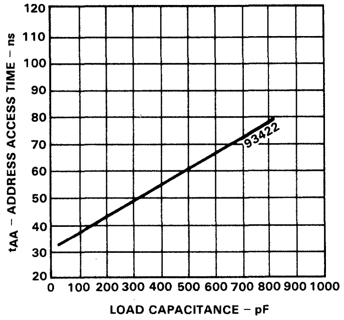
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



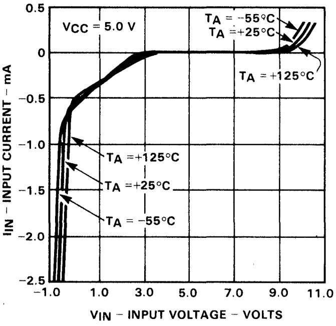
POWER SUPPLY CURRENT VERSUS TEMPERATURE



ADDRESS ACCESS TIME VERSUS LOAD CAPACITANCE

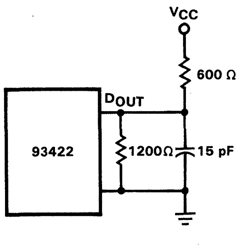


INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS TEMPERATURE

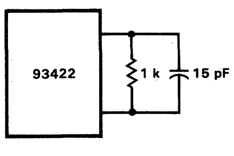


AC TEST LOAD AND WAVEFORM

LOADING CONDITIONS

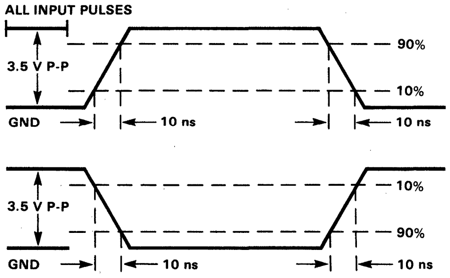


LOAD A



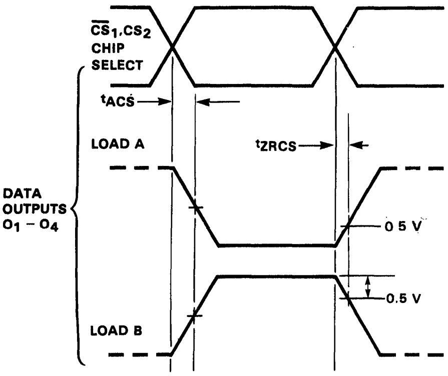
LOAD B

INPUT PULSES

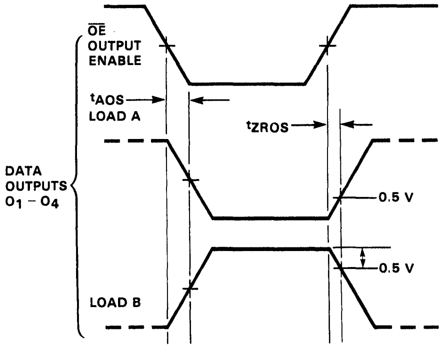


AC TEST WAVEFORMS (Cont'd)

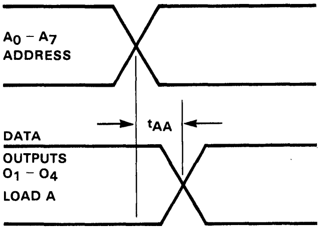
READ MODE
PROPAGATION DELAY FROM CHIP SELECT



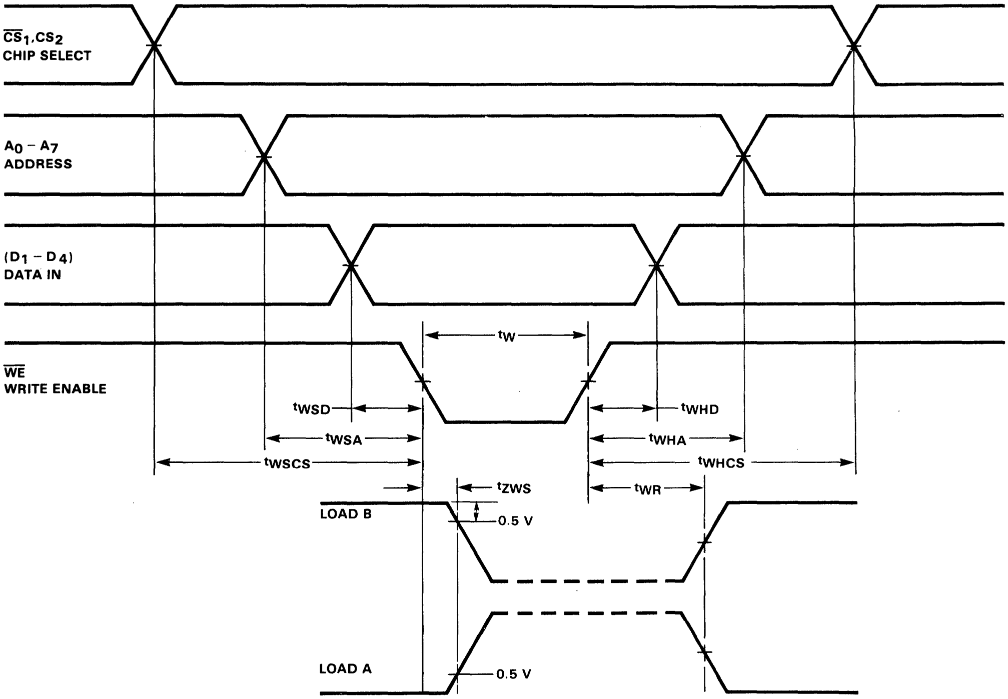
PROPAGATION DELAY FROM OUTPUT ENABLE



PROPAGATION DELAY FROM ADDRESS INPUTS



WRITE MODE



(All above measurements referenced to 1.5 V unless otherwise indicated)

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

TTL ISOPLANAR MEMORY 93L425

1024×1-BIT FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION – The 93L425 is a low power 1024-bit Read/Write Random Access Memory organized 1024 words by one bit. It has a typical access time of 35 ns and is designed for buffer and control storage and high performance main memory applications requiring low power.

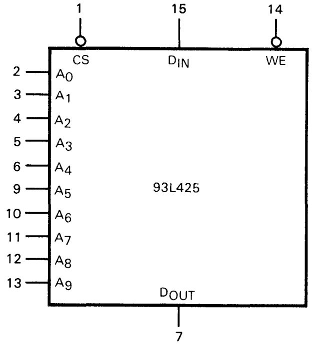
The 93L425 has full decoding on chip, separate Data Input and Data Output lines and an active LOW Chip Select line. A 3-state output is provided to drive bus organized systems and/or highly capacitive loads. The 93L425 is fully compatible with standard DTL and TTL logic families.

- **FULL MIL AND COMMERCIAL RANGES**
- **3-STATE OUTPUT**
- **NON-INVERTING DATA OUTPUT**
- **ORGANIZED 1024 WORDS X 1 BIT**
- **READ ACCESS TIME 35 ns TYPICAL**
- **CHIP SELECT ACCESS TIME 20 ns TYPICAL**
- **POWER DISSIPATION 250 mW TYPICAL**
- **TTL INPUTS AND OUTPUTS**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**

PIN NAMES

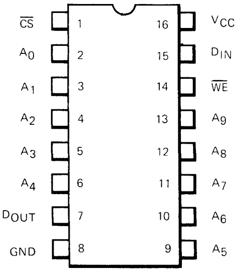
$\overline{CS}$	Chip Select Input
$A_0 - A_9$	Address Inputs
$\overline{WE}$	Write Enable Input
D_{IN}	Data Input
D_{OUT}	Data Output

LOGIC SYMBOL



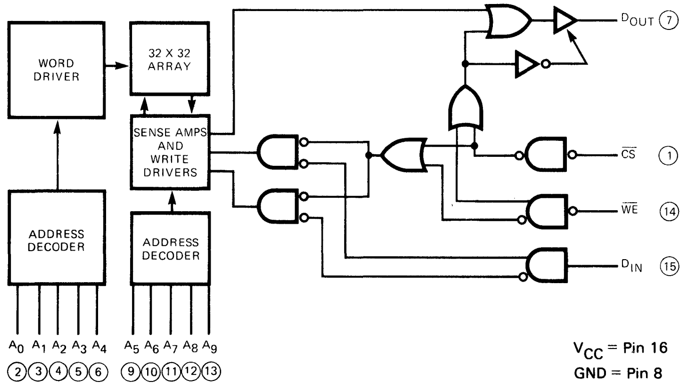
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Number

FUNCTIONAL DESCRIPTION – The 93L425 is a fully decoded 1024-Bit Random Access Memory organized 1024 words by one bit. Word selection is achieved by means of a 10-bit address, A_0 thru A_9.

The Chip Select input allows memory array expansion. For large memories, the fast chip select access time permits decoding of the Chip Select ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$, pin 14). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at D_{OUT} and is non-inverted. During writing, the output is held in the high impedance state.

The 3-state output provides drive capability for higher speeds with high capacitive load systems The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus.

TABLE 1 – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	
H	X	X	HIGH Z	Not Selected
L	L	L	HIGH Z	Write "0"
L	L	H	HIGH Z	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
**Voltage Applied to Outputs (output HIGH)	0.5 V to +5.50 V
Output Current (dc) (output LOW)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93L425XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93L425XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges. Notes 1, 2 and 4

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX		
V_{OL}	Output LOW Voltage		0.35	0.50	V	V_{CC} = MIN, I_{OL} = 16 mA
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guranteed Input LOW Voltage for all Inputs
I_{IL}	Input LOW Current		−150	−300	μA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V
				1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V
I_{OFF}	Output Current (HIGH Z)			50 −50	μA	V_{CC} = MAX, V_{OUT} = 2.4 V V_{CC} = MAX, V_{OUT} = 0.5 V
I_{OS}	Output Current Short Circuit to Ground			−100	mA	V_{CC} = MAX, Note 7
V_{OH}	Output HIGH Voltage 93L425XC	2.4			V	I_{OH} = −5.2 mA, V_{CC} = 5.0 V ±5%
	93L425XM	2.4			V	I_{OH} = −5.2 mA, V_{CC} = 5.0 V ±10%
V_{CD}	Input Clamp Diode Voltage		−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA
I_{CC}	Power Supply Current			55	mA	$T_A \geqslant 75$°C; V_{CC} = MAX, All Inputs Grounded
			45	65	mA	T_A = 0°C
				75	mA	T_A = −55°C

AC CHARACTERISTICS: Over Guaranteed Operating Ranges. Notes 1, 2, 4, 5, 6

SYMBOL	CHARACTERISTIC	93L425XC			93L425XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Access Time		20	40		20	45	ns	See Test Circuit and Waveforms
t_{ZRCS}	Chip Select to HIGH Z		20	40		20	50		
t_{AA}	Address Access Time		35	60		35	70		
WRITE MODE	DELAY TIMES								
t_{ZWS}	Write Disable to HIGH Z		20	45		20	45	ns	See Test Circuit and Waveforms
t_{WR}	Write Recovery Time		20	45		20	55		
	INPUT TIMING REQUIREMENTS								
t_W	Write Pulse Width (to guarantee write)	45	25		50	25			
t_{WSD}	Data Set-Up Time Prior to Write	5	0		10	0			
t_{WHD}	Data Hold Time After Write	5	0		10	0			
t_{WSA}	Address Set-Up Time	10	0		10	0			
t_{WHA}	Address Hold Time	5	0		10	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		10	0			
t_{WHCS}	Chip Select Hold Time	5	0		10	0			
C_I	Input Pin Capacitance		4	5		4	5	pF	
C_O	Output Pin Capacitance		7	8		7	8		

NOTES:

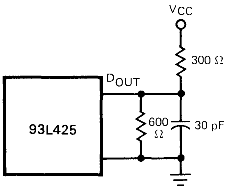
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°CC/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.

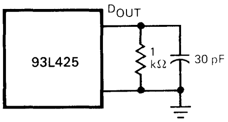
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.

AC TEST LOAD AND WAVEFORM

LOADING CONDITIONS

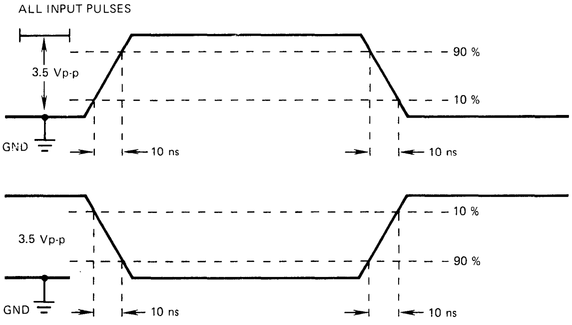


Load A



Load B

INPUT PULSES

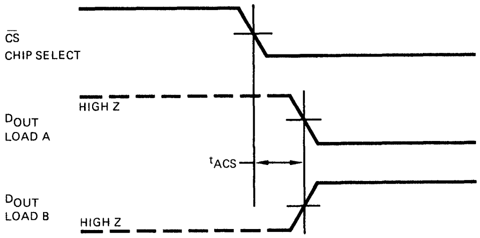


(All time measurements referenced to 1.5 V)

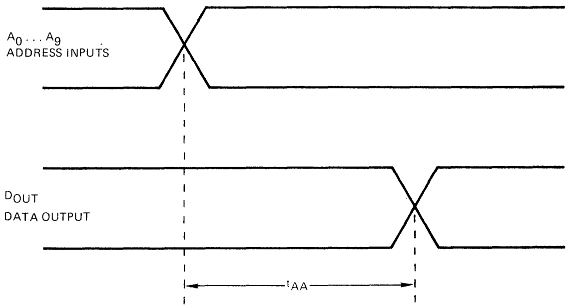
AC WAVEFORMS

READ MODE

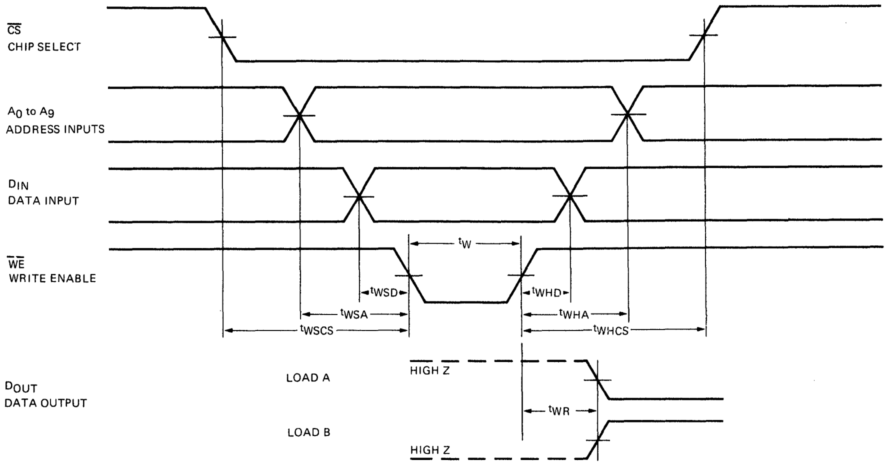
PROPAGATION DELAY FROM CHIP SELECT



PROPAGATION DELAY FROM ADDRESS INPUTS



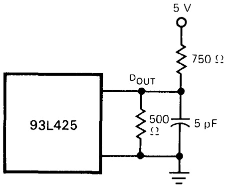
WRITE MODE



(All time measurements referenced to 1.5 V)

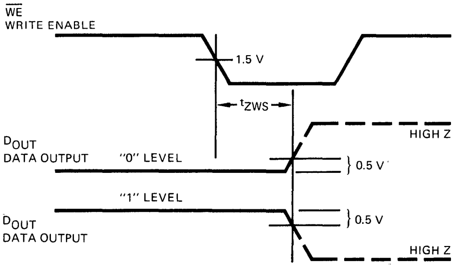
NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

AC TEST LOAD AND WAVEFORM

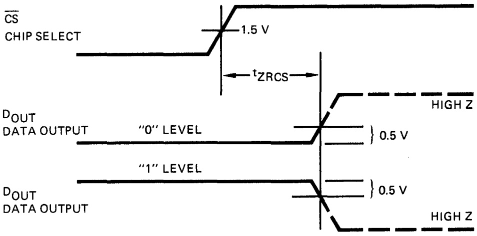


Load C

WRITE ENABLE TO HIGH Z DELAY



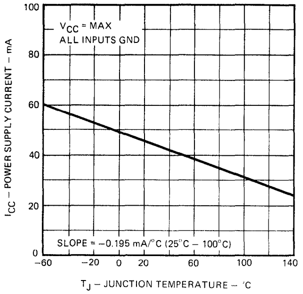
PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



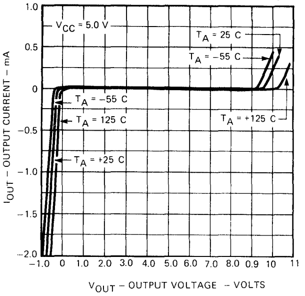
(All t_{ZXXX} parameters are measured at a delta of 0.5 V from the logic level and using Load C.)

TYPICAL ELECTRICAL CHARACTERISTIC CURVES

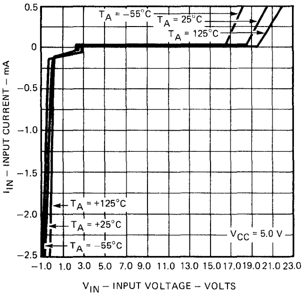
POWER SUPPLY CURRENT VERSUS TEMPERATURE



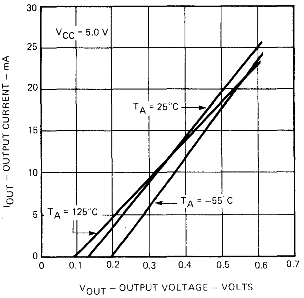
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



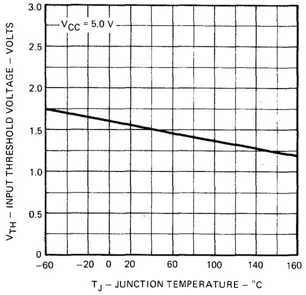
INPUT CURRENT VERSUS INPUT VOLTAGE



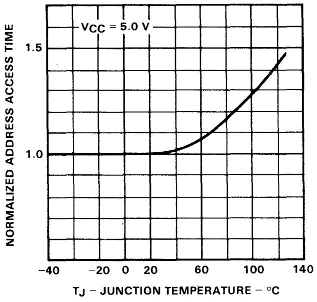
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



INPUT THRESHOLD VOLTAGE VERSUS TEMPERATURE



NORMALIZED ADDRESS ACCESS TIME VERSUS TEMPERATURE



TTL ISOPLANAR MEMORY 93425/93425A

1024×1-BIT FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION – The 93425 and 93425A are 1024-bit Read/Write Random Access Memories organized 1024 words by one bit. They are designed for buffer control storage and high performance main memory applications. The devices have typical address times of 30 ns for the 93425 and 25 ns for the 93425A.

The 93425 and 93425A include full decoding on chip, separate Data Input and Data Output lines and an active LOW Chip Select and Write Enable. They are fully compatible with standard DTL and TTL logic families. A 3-state output is provided to drive bus organized systems and/or highly capacitive loads.

- **3-STATE OUTPUT**
- **ORGANIZED 1024 WORDS X 1 BIT**
- **TTL INPUTS AND OUTPUT – FULL 16 mA DRIVE CAPABILITY**
- **TYPICAL READ ACCESS TIME**

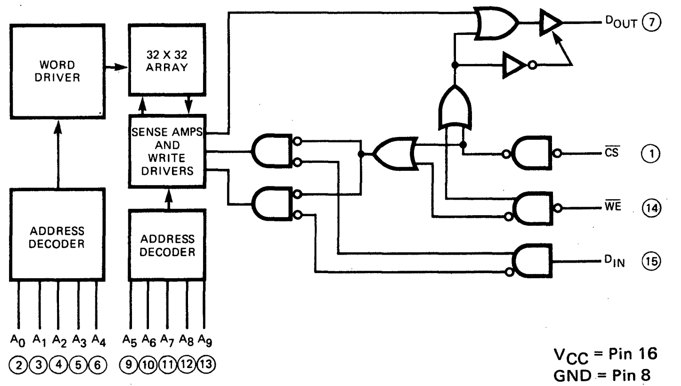
93425A	**Commercial**	**30 ns**
93425	**Commercial**	**40 ns**
93425	**Military**	**40 ns**

- **CHIP SELECT ACCESS TIME 15 ns TYPICAL**
- **NON-INVERTING DATA OUTPUT**
- **POWER DISSIPATION 0.5 mW/BIT TYPICAL**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**

PIN NAMES

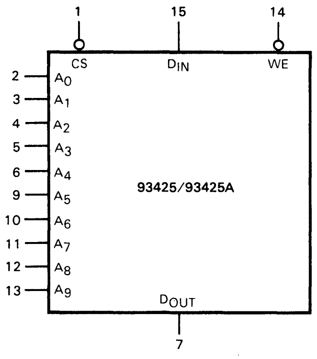
$\overline{CS}$	Chip Select
$A_0 - A_9$	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

LOGIC DIAGRAM



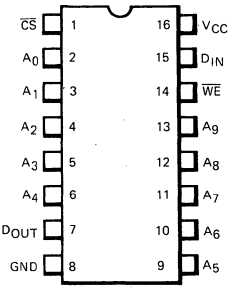
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The 93425/93425A are fully decoded 1024-bit Random Access Memories organized 1024 words by one bit. Word selection is achieved by means of a 10-bit address, A_0 to A_9.

The Chip Select ($\overline{CS}$) input provides for memory array expansion. For large memories, the fast chip select time permits the decoding of chip select from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$, Pin 14). With $\overline{WE}$ and $\overline{CS}$ held LOW, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and $\overline{CS}$ held LOW. Data in the specified location is presented at D_{OUT} and is non-inverted.

The 3-state output provides drive capability for higher speeds with high capacitive load systems. The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in the high impedance state.

TABLE 1 – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	
H	X	X	HIGH Z	NOT SELECTED
L	L	L	HIGH Z	WRITE "0"
L	L	H	HIGH Z	WRITE "1"
L	H	X	D_{OUT}	READ

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired.)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
**Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5 V
Output Current (dc) (Output LOW)	+20 mA

*Either input voltage or input current limit is sufficient to protect the input.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE (T_A) (Note 4)
	MIN	TYP	MAX	
93425XC, 93425AXC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93425XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2, 4)

SYMBOL	CHARACTERISTIC		LIMITS			UNITS	CONDITIONS	
			MIN	TYP (Note 3)	MAX			
V_{OL}	Output LOW Voltage			0.3	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage		2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage			1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current			−250	−400	μA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
I_{OFF}	Output Current (HIGH Z)				50 −50	μA	V_{CC} = MAX, V_{OUT} = 2.4 V V_{CC} = MAX, V_{OUT} = 0.5 V	
I_{OS}	Output Current Short Circuit to Ground				−100	mA	V_{CC} = MAX, Note 7	
V_{OH}	Output HIGH Voltage	93425XC	2.4			V	I_{OH} = −10.3 mA, V_{CC} = 5.0 V ±5%	
		93425XM	2.4			V	I_{OH} = −5.2 mA	
V_{CD}	Input Diode Clamp Voltage			−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA	
I_{CC}	Power Supply Current				130	mA	$T_A \geq 75°C$	V_{CC} = MAX, All Inputs Grounded
				95	155	mA	$T_A = 0°C$	
					170	mA	$T_A = -55°C$	

AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

SYMBOL	CHARACTERISTIC	93425AXC			93425XC			93425XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES											
t_{ACS}	Chip Select Time		15	20		15	35		15	45	ns	See Test Circuit and Waveforms
t_{ZRCS}	Chip Select to HIGH Z		15	20		20	35		20	50		
t_{AA}	Address Access Time		25	30		30	45		40	60		
WRITE MODE	DELAY TIMES											
t_{ZWS}	Write Disable to HIGH Z		15	20		20	35		20	45	ns	
t_{WR}	Write Recovery Time		20	25		25	40		45	50		
	INPUT TIMING REQUIREMENTS											
t_W	Write Pulse Width (to guarantee write)	20	15		30	25		40	25			See Test Circuit and Waveforms
t_{WSD}	Data Set-Up Time Prior to Write	5	0		5	0		5	0			
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0			
t_{WSA}	Address Set-Up Time	5	0		10	0		15	0		ns	
t_{WHA}	Address Hold Time	5	0		5	0		5	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0		5	0			
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0			
C_I	Input Pin Capacitance		4	5		4	5		4	5	pF	Measure with Pulse Technique
C_O	Output Pin Capacitance		7	8		7	8		7	8		

NOTES:

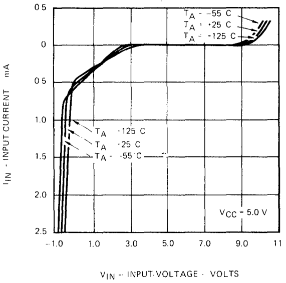
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°CC/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.

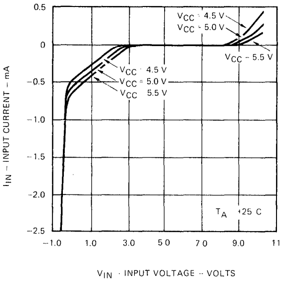
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.

TYPICAL ELECTRICAL CHARACTERISTICS

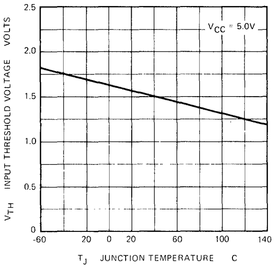
INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS TEMPERATURE



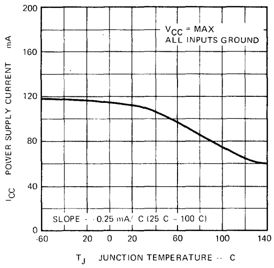
INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS SUPPLY VOLTAGE



INPUT THRESHOLD VOLTAGE VERSUS TEMPERATURE

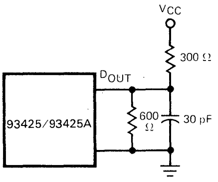


POWER SUPPLY CURRENT VERSUS TEMPERATURE

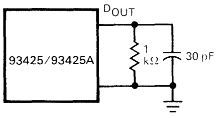


AC TEST LOAD AND WAVEFORMS

LOADING CONDITIONS

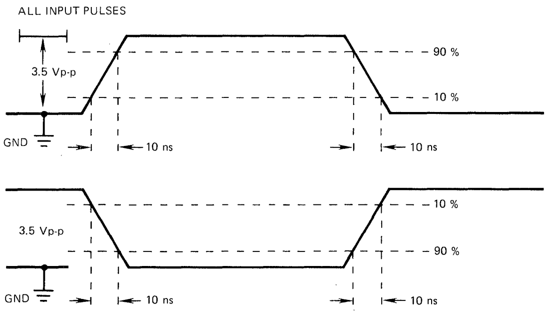


Load A



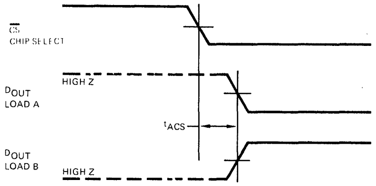
Load B

INPUT PULSES

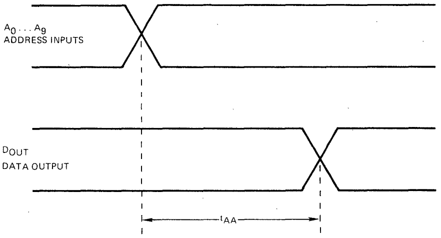


READ MODE

PROPAGATION DELAY FROM CHIP SELECT



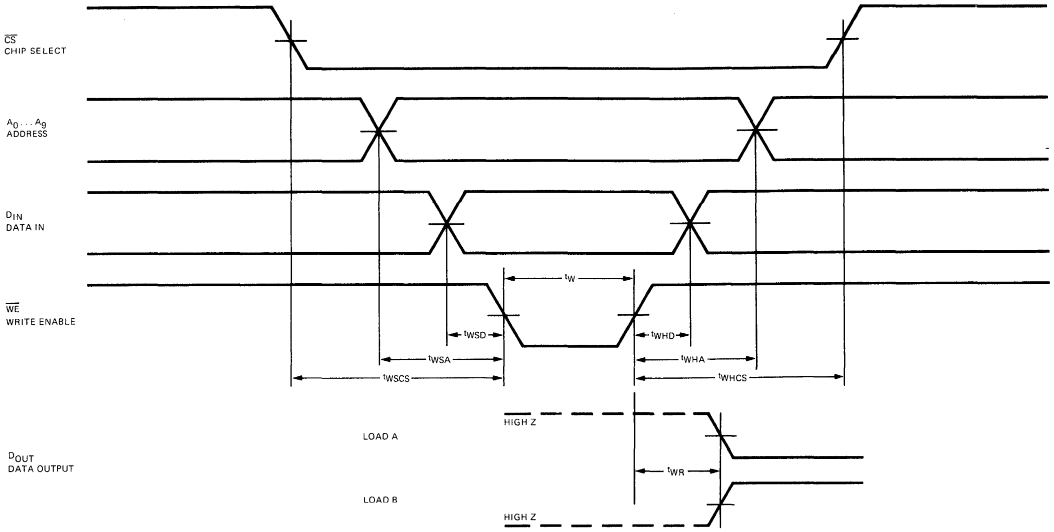
PROPAGATION DELAY FROM ADDRESS INPUTS



(All time measurements referenced to 1.5 V)

AC WAVEFORMS (Cont'd)

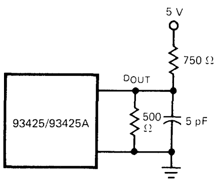
WRITE MODE



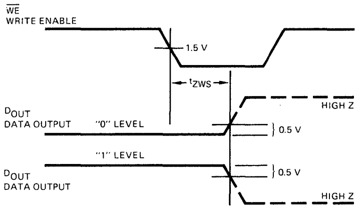
(All above measurements referenced to 1.5 V)

NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

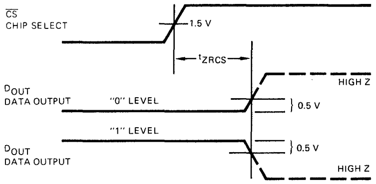
WRITE ENABLE TO HIGH Z DELAY



Load C



PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



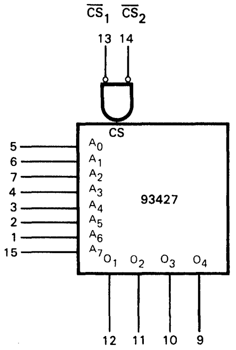
(All t_{ZXXX} parameters are measured at a delta of 0.5 V from the logic level and using Load C.)

93427
ISOPLANAR SCHOTTKY TTL MEMORY
256×4-BIT PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION – The 93427 is a fully decoded high speed 1024-bit field Programmable ROM organized 256 words by four bits per word. The 93427 has 3-state outputs. The outputs are disabled when either $\overline{CS}_1$ or $\overline{CS}_2$ are in the HIGH state. The 93427 is supplied with all bits stored as logic "1"s and can be programmed to logic "0"s by following the field programming procedure.

- FULL MIL AND COMMERCIAL RANGES
- FIELD PROGRAMMABLE
- ORGANIZED 256 X 4 BITS PER WORD
- 3-STATE OUTPUTS
- FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER
- CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION
- WIRED-OR CAPABILITY
- STANDARD 16-PIN DUAL IN-LINE PACKAGE
- NICHROME FUSE LINKS – FOR HIGH RELIABILITY

LOGIC SYMBOL

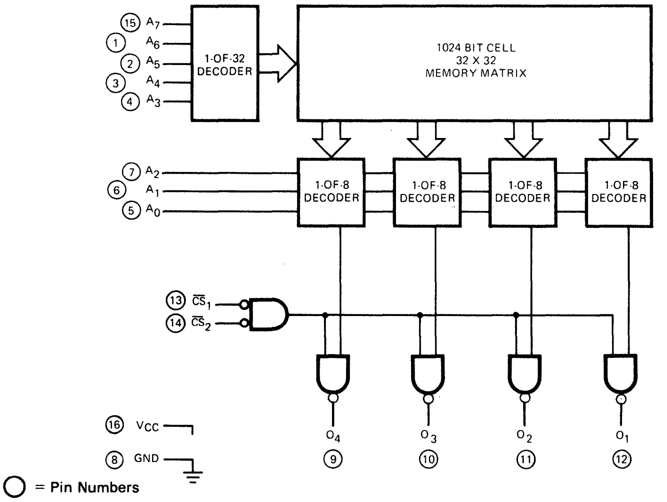


V_{CC} = Pin 16
GND = Pin 8

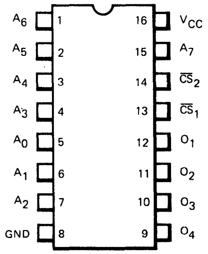
PIN NAMES

$A_0 - A_7$	Address Inputs
$\overline{CS}_1, \overline{CS}_2$	Chip Select Inputs (Active LOW)
$O_1 - O_4$	Data Outputs

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The 93427 is a bipolar field Programmable Read Only Memory (PROM) organized 256 words by four bits per word. The 93427 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. Chip Selects are active LOW; conversely, a HIGH (logic "1") on the $\overline{CS}_1$ or $\overline{CS}_2$ will disable all outputs.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_7 inputs, the chip is selected, and data is valid at the outputs after t_{AA} nanoseconds.

Programming (selectively opening nichrome fuse links) is accomplished by following the sequence outlined below.

PROGRAMMING – The 93427 is manufactured with all bits in the logic "1" state. Any desired bit (output) can be programmed to a logic "0" state by following the procedure shown in Chapter 6, page 6-16.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC}	−0.5 V to +7.0 V
Input Voltages	−0.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltages	−0.5 V to +5.5 V

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN	TYP	MAX	AMBIENT TEMPERATURE
93427XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93427XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Package Information on this data sheet.

DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise noted.

SYMBOL	CHARACTERISTIC	LIMITS MIN	TYP (Note 1)	MAX	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA, A_0 = +10.8 V A_1 through A_7 = HIGH	
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = MIN, I_{OH} = −2.0 mA	
I_{off}	Output Leakage Current for HIGH Impedance State			50 −50	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	0°C to +75°C
I_{off}	Output Leakage Current for HIGH Impedance State			100 −50	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	−55°C to +125°C
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
I_F	Input LOW Current I_{FA} (Address Inputs) I_{FCS} (Chip Select Inputs)		 −160 −160	 −250 −250	 μA μA	V_{CC} = MAX, V_F = 0.45 V	
I_R	Input HIGH Current I_{RA} (Address Inputs) I_{RCS} (Chip Select Input)			 40 40	 μA μA	V_{CC} = MAX, V_R = 2.4 V	
I_{CC}	Power Supply Current		85	110	mA	V_{CC} = MAX, Outputs open Inputs Grounded and Chip Selected	
C_O	Output Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz	
C_{IN}	Input Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz	
V_C	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_A = −18 mA	

AC CHARACTERISTICS: $T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$.

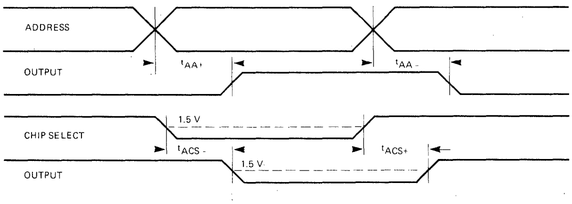
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-}	Address to Output Access Time		25	45	ns	See Figure 1
t_{AA+}			25	45	ns	
t_{ACS-}	Chip Select Access Time		12	20	ns	
t_{ACS+}			12	20	ns	

AC CHARACTERISTICS: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$.

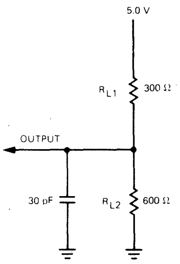
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-}	Address to Output Access Time		25	60	ns	See Figure 1
t_{AA+}			25	60	ns	
t_{ACS-}	Chip Select Access Time		12	30	ns	
t_{ACS+}			12	30	ns	

Note 1: Typical values are at $V_{CC} = 5.0\ V$, $+25°C$ and max loading.

AC WAVEFORMS



AC TEST OUTPUT LOAD



15 mA Load

Fig. 1

93431

ISOPLANAR SCHOTTKY TTL MEMORY

512 X 4-BIT READ ONLY MEMORY

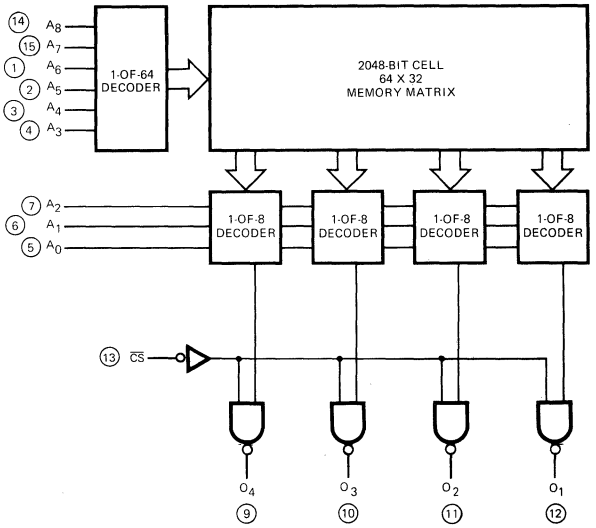
DESCRIPTION – The 93431 is a fully decoded high speed 2048-bit ROM organized 512 words by four bits per word. The 93431 has uncommitted collector outputs. The outputs are off when the $\overline{CS}$ input is in the HIGH state. Electrical characteristics are the same as the 93436.

- **FULL MIL AND COMMERCIAL RANGES**
- **FAST CYCLE TIME – 30 ns TYP**
- **ORGANIZATION 512 WORDS X 4 BITS**
- **UNCOMMITTED COLLECTORS**
- **SEE 93436 FOR ELECTRICALS**
- **FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER**
- **CHIP SELECT INPUT PROVIDES EASY MEMORY EXPANSION**
- **WIRED-OR CAPABILITY**
- **STANDARD 16-PIN DUAL IN-LINE PACKAGE**
- **REPLACES TWO 256 x 4 ROMs – DOUBLE DENSITY WITH SAME SPACE AND POWER**

PIN NAMES

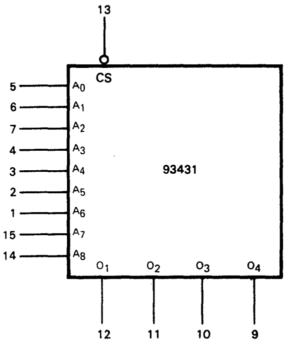
A_0 to A_8	Address Inputs
$\overline{CS}$	Chip Select Input
O_1 to O_4	Data Outputs

LOGIC DIAGRAM



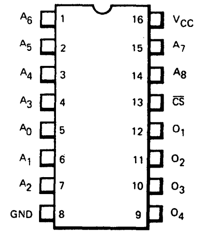
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

93432

ISOPLANAR SCHOTTKY TTL MEMORY

512 X 8-BIT READ ONLY MEMORY

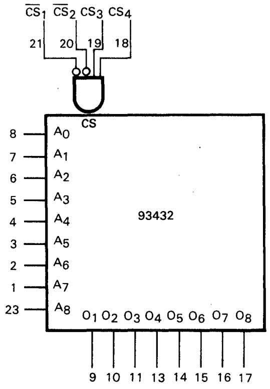
DESCRIPTION – The 93432 is a fully decoded 4096-bit Read Only Memory organized 512 words by eight bits per word. The 93432 has uncommitted collector outputs. The device is enabled when $\overline{CS}_1$ and $\overline{CS}_2$ are LOW and CS_3 and CS_4 are HIGH. Electrical characteristics are the same as the 93438.

- **ADVANCED ISOPLANAR SCHOTTKY**
- **ORGANIZATION – 512 WORDS X 8 BITS**
- **UNCOMMITTED COLLECTOR OUTPUTS**
- **SEE 93438 FOR ELECTRICALS**
- **STANDARD 24-PIN DUAL IN-LINE PACKAGE**
- **FULL ADDRESS DECODING ON CHIP**
- **FAST CYCLE TIME – 35 ns TYP**

PIN NAMES

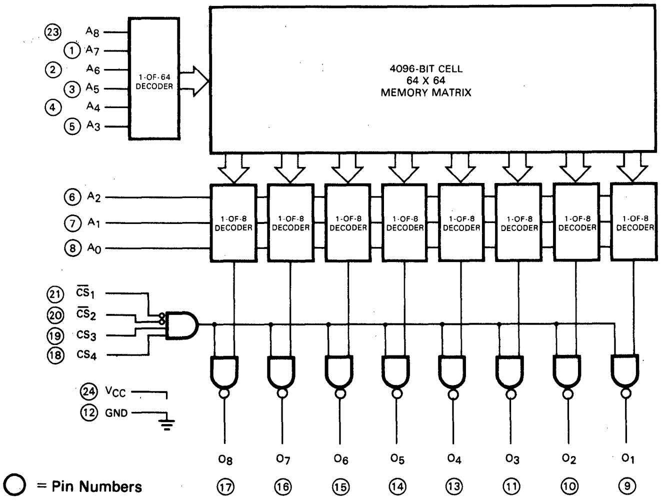
$\overline{CS}_1$, $\overline{CS}_2$, CS_3, CS_4	Chip Select Inputs
A_0 to A_8	Address Inputs
O_1 to O_8	Data Outputs

LOGIC SYMBOL

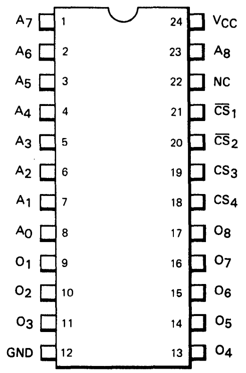


V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

93436
ISOPLANAR SCHOTTKY TTL MEMORY
512×4-BIT PROGRAMMABLE READ ONLY MEMORY

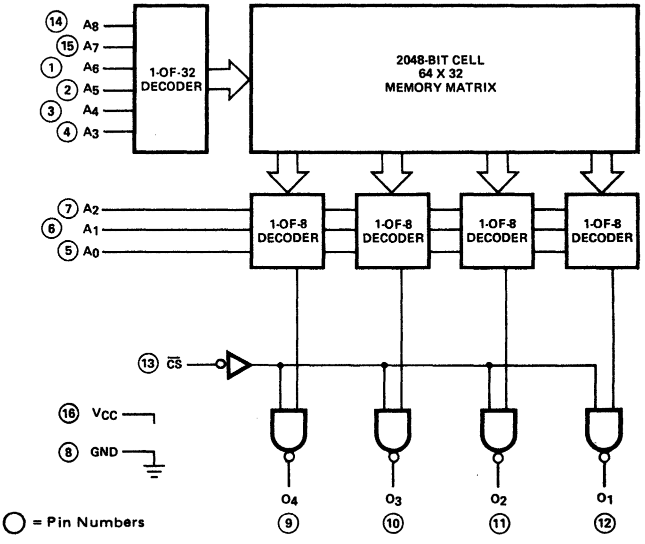
DESCRIPTION – The 93436 is a fully decoded high speed 2048-bit field Programmable ROM organized 512 words by four bits per word. The 93436 has uncommitted collector outputs. The outputs are off when the $\overline{CS}$ input is in the HIGH state. The 93436 is supplied with all bits stored as logic "1"s and can be programmed to logic "0"s by following the field programming procedure.

- FAST CYCLE TIME – 30 ns TYP.
- FULL MIL AND COMMERCIAL RANGES
- FIELD PROGRAMMABLE
- ORGANIZATION – 512 WORDS X 4 BITS
- UNCOMMITTED COLLECTORS – 93436
- FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER
- CHIP SELECT INPUT PROVIDES EASY MEMORY EXPANSION
- WIRED-OR CAPABILITY
- STANDARD 16-PIN DUAL IN-LINE PACKAGE
- NICHROME FUSE LINKS FOR HIGH RELIABILITY
- REPLACES TWO 256 x 4 PROMS – DOUBLE DENSITY WITH SAME SPACE AND POWER

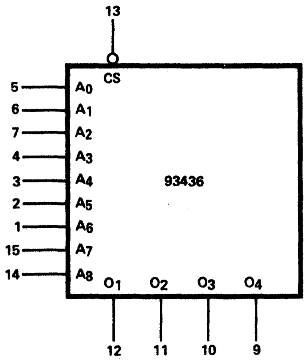
PIN NAMES

$A_0 - A_8$	Address Inputs
$\overline{CS}$	Chip Select Input
$O_1 - O_4$	Data Outputs

LOGIC DIAGRAM

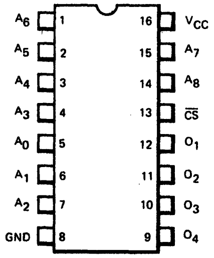


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP(TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The 93436 is a bipolar field Programmable Read Only Memory (PROM) organized 512 words by four bits per word. Open collector outputs are provided on the 93436 for use in wired-OR systems. Chip Select is active LOW; i.e., a HIGH (logic "1") on the $\overline{CS}$ pin will disable all outputs.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_8 inputs, the chip is selected, and data is valid at the outputs after t_{AA} nanoseconds.

Programming (selectively opening nichchrome fuse links) is accomplished by following the sequence outlined below.

PROGRAMMING – The 93436 is manufactured with all bits in the logic "1" state. Any desired bit (output) can be programmed to a logic "0" state by following the procedure shown in Chapter 6, page 6-16.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC}	−0.5 V to +7.0 V
Input Voltages	−0.5 V to +5.5 V
Current Into Output Terminal	100 mA
Output Voltages	−0.5 V to 4.0 V

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE
	MIN	TYP	MAX	
93436XC,	4.75 V	5.0 V	5.25 V	0°C to +75°C
93436XM,	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Package Information on this data sheet.

DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise noted.

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
I_{CEX}	Output Leakage Current			50	μA	V_{CC} = MAX, V_{CEX} = 4.0 V, 0°C to +75°C Address any HIGH Output
I_{CEX}	Output Leakage Current			100	μA	V_{CC} = MAX, V_{CEX} = 4.0 V, −55°C to +125°C Address any HIGH Output
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA, A_0 = +10.8 V A_1 through A_8 = HIGH
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
I_F	Input LOW Current I_{FA} (Address Inputs) I_{FCS} (Chip Select Inputs)		−160 −160	−250 −250	μA μA	V_{CC} = MAX, V_F = 0.45 V
I_R	Input HIGH Current I_{RA} (Address Inputs) I_{RCS} (Chip Select Input)			 40 40	 μA μA	V_{CC} = MAX, V_R = 2.4 V
I_{CC}	Power Supply Current		95	130	mA	V_{CC} = MAX, Outputs open Inputs Grounded and Chip Selected
C_O	Output Capacitance		7.0		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
C_{IN}	Input Capacitance		4.0		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
V_C	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_A = −18 mA

AC CHARACTERISTICS: T_A = 0°C to +75°C, V_{CC} = 5.0 V ± 5%.

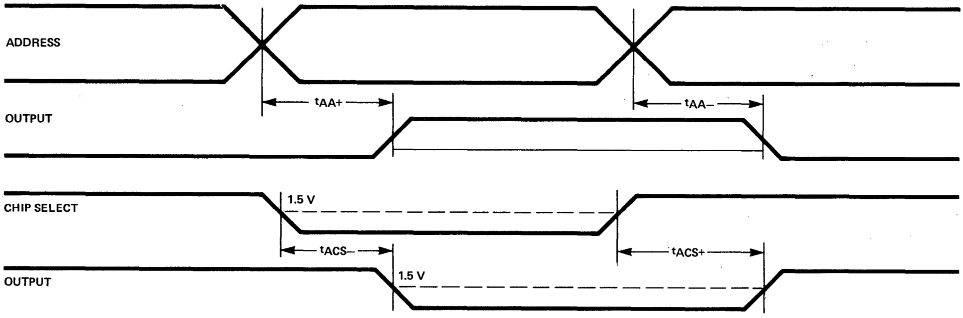
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-}	Address to Output Access Time		30	50	ns	See Figure 1
t_{AA+}			30	50	ns	
t_{ACS-}	Chip Select Access Time		15	25	ns	
t_{ACS+}			15	25	ns	

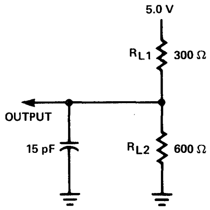
AC CHARACTERISTICS: T_A = −55°C to +125°C, V_{CC} = 5.0 V ± 10%.

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-}	Address to Output Access Time		30	60	ns	See Figure 1
t_{AA+}			30	60	ns	
t_{ACS-}	Chip Select Access Time		15	30	ns	
t_{ACS+}			15	30	ns	

Note 1: Typical values are at V_{CC} = 5.0 V, +25°C and max loading.

AC WAVEFORM AND TEST OUTPUT LOAD





15 mA Load

Fig. 1

93438
ISOPLANAR SCHOTTKY TTL MEMORY
512×8-BIT PROGRAMMABLE READ ONLY MEMORY

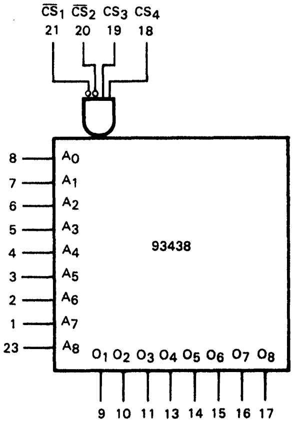
DESCRIPTION – The 93438 is a fully decoded 4096-bit field Programmable ROM organized 512 words by eight bits per word. The 93438 has uncommitted collector outputs. The device is enabled when $\overline{CS}_1$ and $\overline{CS}_2$ are LOW and CS_3 and CS_4 are HIGH. The 93438 is supplied with all bits stored as logic "1"s and may be programmed to logic "0"s by following the field programming procedure.

- **FULL MIL AND COMMERCIAL RANGES**
- **FIELD PROGRAMMABLE**
- **ORGANIZATION - 512 WORDS X 8 BITS**
- **UNCOMMITTED COLLECTORS**
- **FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER**
- **CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION**
- **WIRED-OR CAPABILITY**
- **STANDARD 24-PIN DUAL IN-LINE PACKAGE**
- **NICHROME FUSE LINKS FOR HIGH RELIABILITY**

PIN NAMES

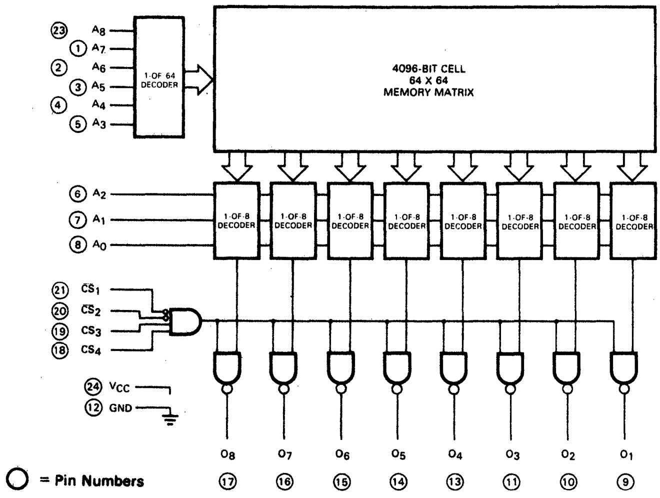
$A_0 - A_8$	Address Inputs
$\overline{CS}_1$, $\overline{CS}_2$, CS_3, CS_4	Chip Select Inputs
$O_1 - O_8$	Data Outputs

LOGIC SYMBOL

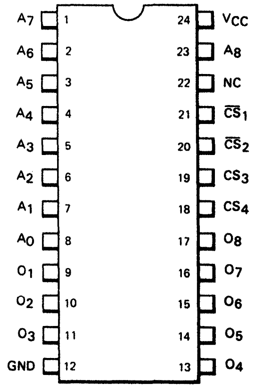


V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC}	−0.5 V to +7.0 V
Input Voltage	−0.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltages	−0.5 V to 4.0 V

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE
	MIN	TYP	MAX	
93438XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93438XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

FUNCTIONAL DESCRIPTION – The 93438 is a bipolar field Programmable Read Only Memory (PROM) organized 512 words by eight bits per word. Open collector outputs are provided on the 93438 for use in wired-OR systems. Chip Select follows the logic equation: $\overline{CS}_1 \bullet \overline{CS}_2 \bullet CS_3 \bullet CS_4 = CS$; i.e., if $\overline{CS}_1$ and $\overline{CS}_2$ are both active LOW and CS_3 and CS_4 are both active HIGH, all eight outputs are enabled; for any other condition all eight outputs are disabled.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_8 inputs, the chip is selected, and data is valid at the outputs after t_{AA} nanoseconds.

Programming (selectively opening nichrome fuse links) is accomplished by following the procedure in Chapter 6, page 6-16.

DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise note.

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
I_{CEX}	Output Leakage Current			50	μA	V_{CC} = MAX, V_{CEX} = 4.0 V, 0°C to +75°C Address any HIGH Output
I_{CEX}	Output Leakage Current			100	μA	V_{CC} = MAX, V_{CEX} = 4.0 V, −55°C to +125°C Address any HIGH Output
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA A_0 = +10.8 V, $A_1 - A_8$ = HIGH
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
I_F	Input LOW Current I_{FA} (Address Inputs) I_{FCS} (Chip Select Inputs)		 −160 −160	 −250 −250	 μA μA	V_{CC} = MAX, V_F = 0.45 V
I_R	Input HIGH Current I_{RA} (Address Inputs) I_{RCS} (Chip Select Input)			 40 40	 μA μA	V_{CC} = MAX, V_R = 2.4 V
I_{CC}	Power Supply Current		130	175	mA	V_{CC} = MAX, Outputs Open Inputs Grounded and Chip Selected
C_O	Output Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
C_{IN}	Input Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
V_C	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_A = −18 mA

AC CHARACTERISTICS: $T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$

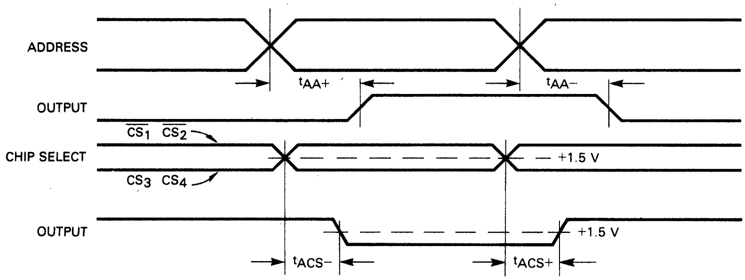
SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-} t_{AA+}	Address to Output Access Time		35 35	55 55	ns ns	See Figure 1
t_{ACS-} t_{ACS+}	Chip Select Access Time		15 15	25 25	ns ns	

AC CHARACTERISTICS: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$

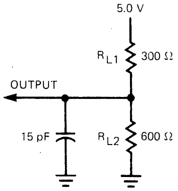
SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-} t_{AA+}	Address to Output Access Time		35 35	70 70	ns ns	See Figure 1
t_{ACS-} t_{ACS+}	Chip Select Access Time		15 15	30 30	ns ns	

Note (1): Typical values are at $V_{CC} = 5.0\ V$, $+25^oC$ and max loading.

AC WAVEFORM



AC TEST OUTPUT LOAD



15 mA Load

Fig. 1

93441

ISOPLANAR SCHOTTKY TTL MEMORY

512 X 4-BIT READ ONLY MEMORY

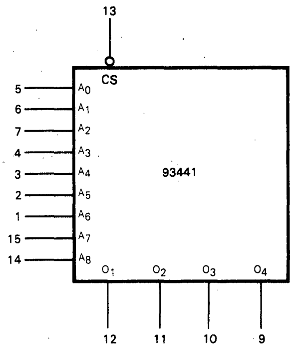
DESCRIPTION – The 93441 is a fully decoded high speed 2048-bit ROM organized 512 words by four bits per word. The 93441 has 3-state outputs. The outputs are off when The CS input is in the HIGH state. Electrical Characteristics are the same as the 93446. 93446.

- **FULL MIL AND COMMERCIAL RANGES**
- **FAST CYCLE TIME — 30 ns TYP**
- **ORGANIZATION – 512 WORDS X 4 BITS**
- **SEE 93446 FOR ELECTRICALS**
- **3-STATE OUTPUTS**
- **FULLY DECODED — ON-CHIP ADDRESS DECODER AND BUFFER**
- **CHIP SELECT INPUT PROVIDES EASY MEMORY EXPANSION**
- **WIRED-OR CAPABILITY**
- **STANDARD 16-PIN DUAL IN-LINE PACKAGE**
- **REPLACES TWO 256 x 4 ROMs — DOUBLE DENSITY WITH SAME SPACE AND POWER**

PIN NAMES

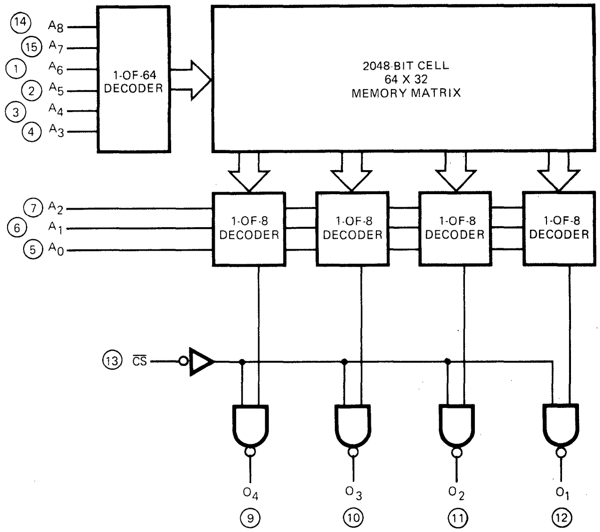
A_0 to A_8	Address Inputs
$\overline{CS}$	Chip Select Input
O_1 to O_4	Data Outputs

LOGIC SYMBOL



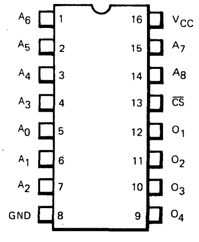
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

93442

ISOPLANAR SCHOTTKY TTL MEMORY

512 X 8-BIT READ ONLY MEMORY

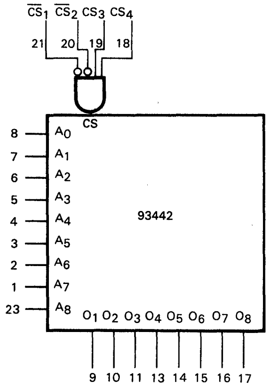
DESCRIPTION – The 93442 is a fully decoded 4096-bit Read Only Memory organized 512 words by eight bits per word. The 93442 has 3-state outputs. The devide is enabled when $\overline{CS}_1$ and $\overline{CS}_2$ are LOW and CS_3 and CS_4 are HIGH. Electrical characteristics are the same as the 93448.

- **FULL MIL AND COMMERCIAL RANGES**
- **ADVANCED ISOPLANAR SCHOTTKY**
- **ORGANIZATION – 512 WORDS X 8 BITS**
- **SEE 93448 FOR ELECTRICALS**
- **3-STATE OUTPUTS**
- **STANDARD 24-PIN DUAL IN-LINE PACKAGE**
- **FULL ADDRESS DECODING ON CHIP**
- **FAST CYCLE TIME – 35 ns TYP**

PIN NAMES

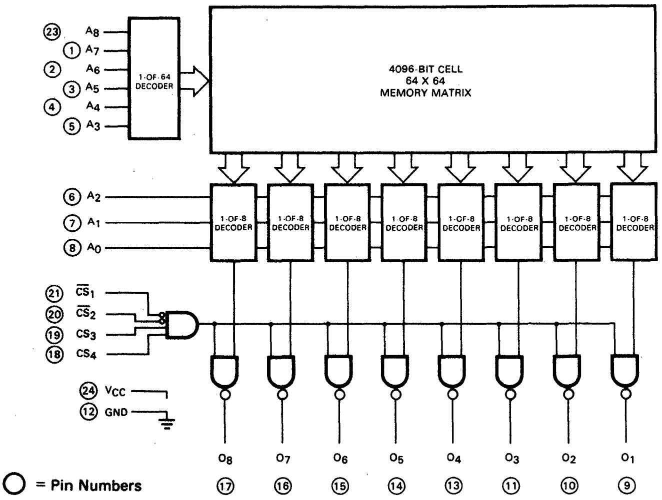
$\overline{CS}_1$, $\overline{CS}_2$, CS_3, CS_4	Chip Select Inputs
A_0 to A_8	Address Inputs
O_1 to O_8	Data Outputs

LOGIC SYMBOL

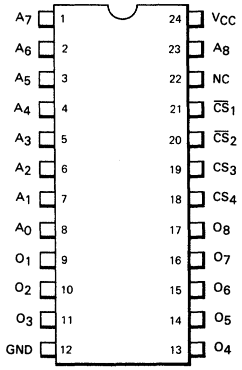


V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



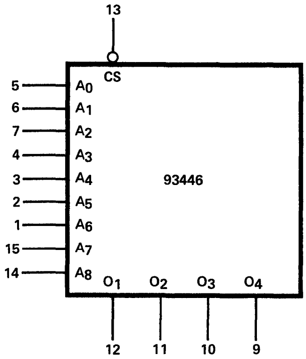
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

93446
ISOPLANAR SCHOTTKY TTL MEMORY
512×4-BIT PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION - The 93446 is a fully decoded high speed 2048-bit field Programmable ROM organized 512 words by four bits per word. The 93446 has 3-state outputs. The outputs are off when the $\overline{CS}$ input is in the HIGH state. The 93446 is supplied with all bits stored as logic "1"s and can be programmed to logic "0"s by following the field programming procedure.

- FAST CYCLE TIME – 30 ns TYP.
- FULL MIL AND COMMERCIAL RANGES
- FIELD PROGRAMMABLE
- ORGANIZATION – 512 WORDS X 4 BITS
- 3-STATE OUTPUTS
- FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER
- CHIP SELECT INPUT PROVIDES EASY MEMORY EXPANSION
- WIRED-OR CAPABILITY
- STANDARD 16-PIN DUAL IN-LINE PACKAGE
- NICHROME FUSE LINKS FOR HIGH RELIABILITY
- REPLACES TWO 256 x 4 PROMS – DOUBLE DENSITY WITH SAME SPACE AND POWER

LOGIC SYMBOL

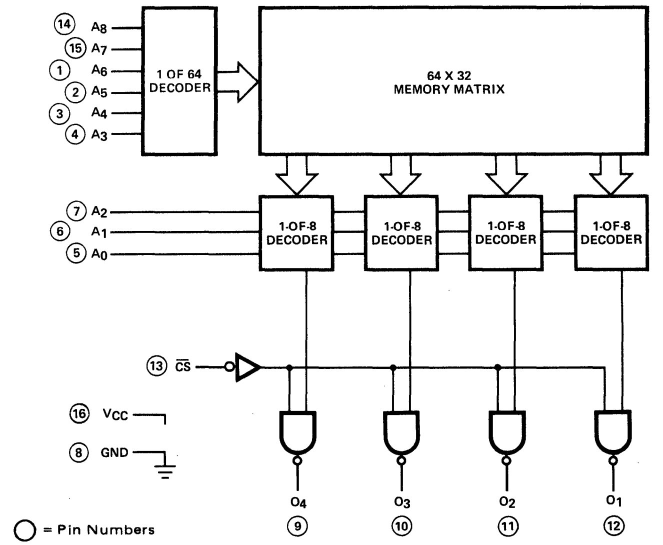


V_{CC} = Pin 16
GND = Pin 8

PIN NAMES

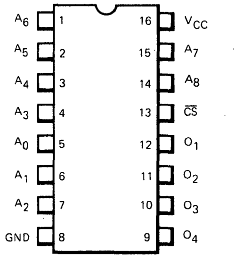
A_0 - A_8	Address Inputs
$\overline{CS}$	Chip Select Input
O_1 - O_4	Data Outputs

LOGIC DIAGRAM



○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION - The 93446 is a bipolar field Programmable Read Only Memory (PROM) organized 512 words by four bits per word. The 93446 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. Chip Select is active LOW; i.e., a HIGH (logic "1") on the $\overline{CS}$ pin will disable all outputs.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_8 inputs, the chip is selected, and data is valid at the outputs after t_{AA} nanoseconds.

Programming (selectively opening nichchrome fuse links) is accomplished by following the sequence outlined below.

PROGRAMMING - The 93446 is manufactured with all bits in the logic "1" state. Any desired bit (output) can be programmed to a logic "0" state by following the procedure shown in Chapter 6, page 6-16.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC}	−0.5 V to +7.0 V
Input Voltages	−0.5 V to +5.5 V
Current Into Output Terminal	100 mA
Output Voltages	−0.5 V to 4.0 V

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE
	MIN	TYP	MAX	
93446XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93446XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Package Information on this data sheet.

DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise noted.

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA, A_0 = +10.8 V A_1 through A_8 = HIGH
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = MIN, I_{OH} = −2.0 mA
I_{off}	Output Leakage Current for HIGH Impedance State			50	μA	V_{OH} = 2.4 V, 0°C to +75°C
				−50	μA	V_{OL} = 0.4 V
I_{off}	Output Leakage Current for HIGH Impedance State			100	μA	V_{OH} = 2.4 V, −55°C to +125°C
				−50	μA	V_{OL} = 0.4 V
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
I_F	Input LOW Current					
	I_{FA} (Address Inputs)		−160	−250	μA	V_{CC} = MAX, V_F = 0.45 V
	I_{FCS} (Chip Select Inputs)		−160	−250	μA	
I_R	Input HIGH Current					
	I_{RA} (Address Inputs)			40	μA	V_{CC} = MAX, V_R = 2.4 V
	I_{RCS} (Chip Select Input)			40	μA	
I_{CC}	Power Supply Current		95	130	mA	V_{CC} = MAX, Outputs open Inputs Grounded and Chip Selected
C_O	Output Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
C_{IN}	Input Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
V_C	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_A = −18 mA

AC CHARACTERISTICS: T_A = 0°C to +75°C, V_{CC} = 5.0 V ± 5%.

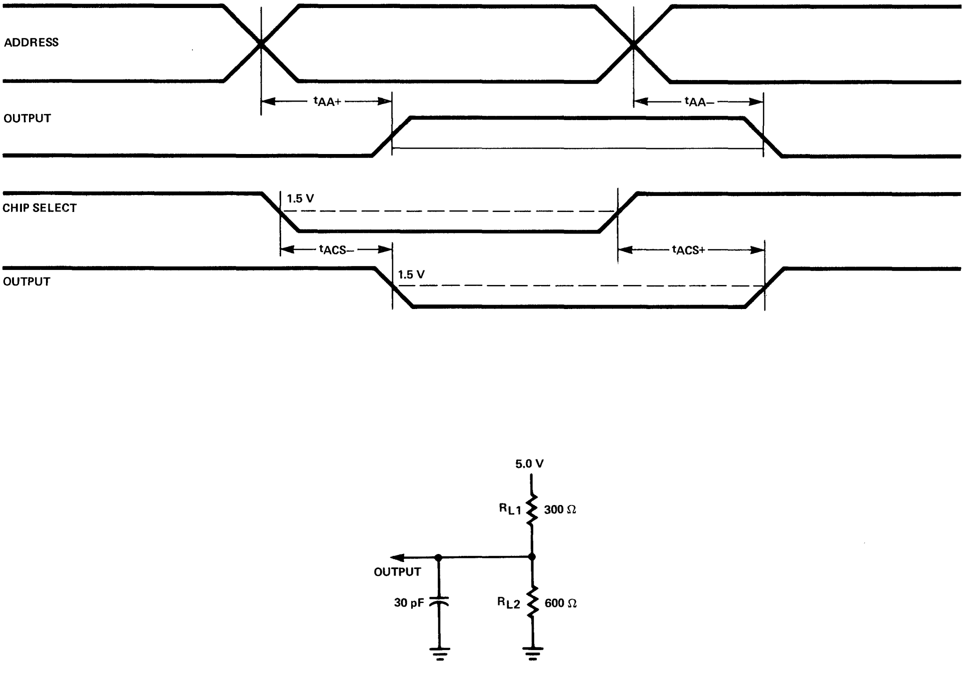
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-} t_{AA+}	Address to Output Access Time		30 30	50 50	ns ns	See Figure 1
t_{ACS-} t_{ACS+}	Chip Select Access Time		15 15	25 25	ns ns	

AC CHARACTERISTICS: T_A = −55°C to +125°C, V_{CC} = 5.0 V ± 10%.

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-} t_{AA+}	Address to Output Access Time		30 30	60 60	ns ns	See Figure 1
t_{ACS-} t_{ACS+}	Chip Select Access Time		15 15	30 30	ns ns	

Note 1: Typical values are at V_{CC} = 5.0 V, +25°C and max loading.

AC WAVEFORM AND TEST OUTPUT LOAD



15 mA Load

Fig. 1

93448
ISOPLANAR SCHOTTKY TTL MEMORY
512×8-BIT PROGRAMMABLE READ ONLY MEMORY

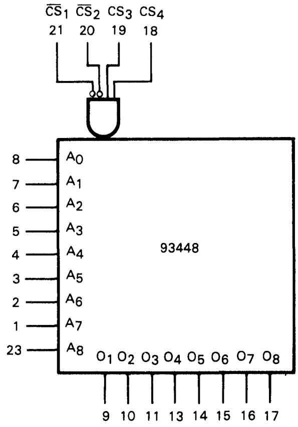
DESCRIPTION – The 93448 is a fully decoded 4096-bit field Programmable ROM organized 512 words by eight bits per word. The 93448 has 3-state outputs. The device is enabled when $\overline{CS}_1$ and $\overline{CS}_2$ are LOW and CS_3 and CS_4 are HIGH. The 93448 is supplied with all bits stored as logic "1"s and may be programmed to logic "0"s by following the field programming procedure.

- **FULL MIL AND COMMERCIAL RANGES**
- **FIELD PROGRAMMABLE**
- **ORGANIZATION – 512 WORDS X 8 BITS**
- **3-STATE OUTPUTS**
- **FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER**
- **CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION**
- **WIRED-OR CAPABILITY**
- **STANDARD 24-PIN DUAL IN-LINE PACKAGE**
- **NICHROME FUSE LINKS FOR HIGH RELIABILITY**
- **REPLACES TWO 256 X 8 PROMs – DOUBLE DENSITY WITH SAME SPACE AND POWER**

PIN NAMES

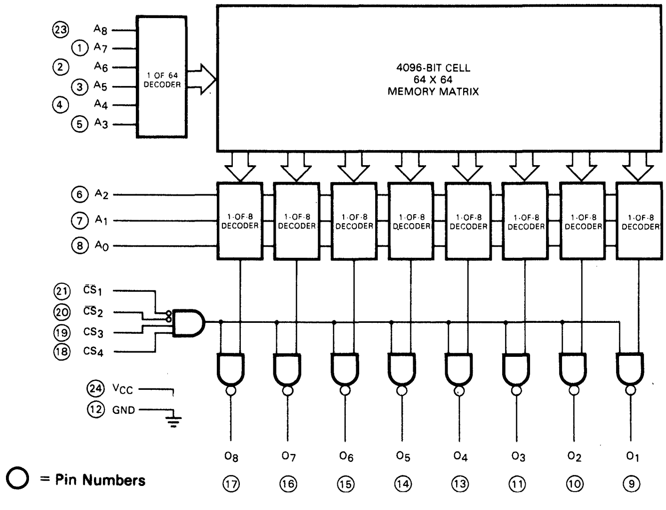
$A_0 - A_8$	Address Inputs
$\overline{CS}_1$, $\overline{CS}_2$, CS_3, CS_4	Chip Select Inputs
$O_1 - O_8$	Data Outputs

LOGIC SYMBOL

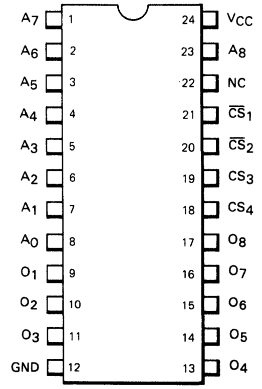


V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC}	−0.5 V to +7.0 V
Input Voltage	−0.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltages	−0.5 V to 4.0 V

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE
	MIN	TYP	MAX	
93448XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93448XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

FUNCTIONAL DESCRIPTION – The 93448 is a bipolar field Programmable Read Only Memory (PROM) organized 512 words by eight bits per word. The 93448 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. Chip Select for both devices follows the logic equation: $\overline{CS}_1 \bullet \overline{CS}_2 \bullet CS_3 \bullet CS_4 = CS$; i.e., if $\overline{CS}_1$ and $\overline{CS}_2$ are both active LOW and CS_3 and CS_4 are both active HIGH, all eight outputs are enabled; for any other condition all eight outputs are disabled.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_8 inputs, the chip is selected, and data is valid at the outputs after t_{AA} nanoseconds.

Programming (selectively opening nichrome fuse links) is accomplished by following the procedures in Chapter 6, page 6-16.

DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise note.

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		MIN	TYP (Note 1)	MAX			
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA A_0 = +10.8 V, $A_1 - A_8$ = HIGH	
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = MIN, I_{OH} = −2.0 mA	
I_{off}	Output Leakage Current for HIGH Impedance State			50 −50	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	0°C to +75°C
I_{off}	Output Leakage Current for HIGH Impedance State			100 −50	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	−55°C to +125°C
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
I_F	Input LOW Current I_{FA} (Address Inputs) I_{FCS} (Chip Select Inputs)		 −160 −160	 −250 −250	 μA μA	V_{CC} = MAX, V_F = 0.45 V	
I_R	Input HIGH Current I_{RA} (Address Inputs) I_{RCS} (Chip Select Input)			 40 40	 μA μA	V_{CC} = MAX, V_R = 2.4 V	
I_{CC}	Power Supply Current		130	175	mA	V_{CC} = MAX, Outputs Open Inputs Grounded and Chip Selected	
C_O	Output Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz	
C_{IN}	Input Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz	
V_C	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_A = −18 mA	

AC CHARACTERISTICS: $T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0$ V ±5%

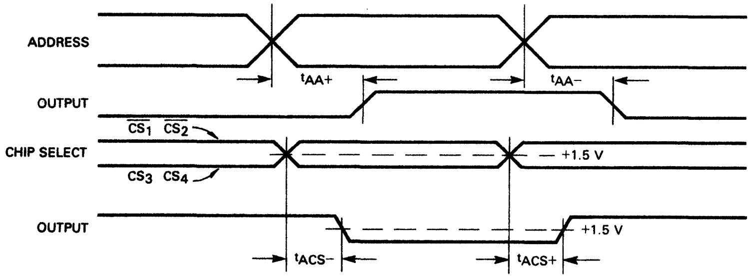
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-} t_{AA+}	Address to Output Access Time		35 35	55 55	ns ns	See Figure 1
t_{ACS-} t_{ACS+}	Chip Select Access Time		15 15	25 25	ns ns	

AC CHARACTERISTICS: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0$ V ±10%

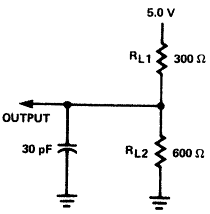
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-} t_{AA+}	Address to Output Access Time		35 35	70 70	ns ns	See Figure 1
t_{ACS-} t_{ACS+}	Chip Select Access Time		15 15	30 30	ns ns	

Note (1): Typical values are at V_{CC} = 5.0 V, 5.0 V, +25°C and max loading.

SWITCHING WAVEFORMS



SWITCHING TEST OUTPUT LOAD



15 mA Load

Fig. 1

93450/93451

ISOPLANAR SCHOTTKY TTL MEMORY

1024 × 8-BIT PROGRAMMABLE READ ONLY MEMORY

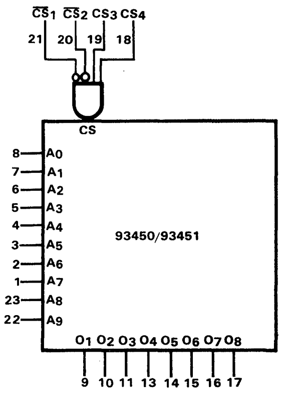
DESCRIPTION – The 93450 and 93451 are fully decoded 8192-bit Field Programmable ROMs organized 1024 words by eight bits per word. The devices are identical except for the output stage. The 93450 has uncommitted collector outputs, while the 93451 has 3-state outputs. Either device is enabled when $\overline{CS}_1$ and $\overline{CS}_2$ are LOW and CS_3 and CS_4 are HIGH. The 93450/51 is supplied with all bits stored as logic "1's" and may be programmed to logic "0's" by following the field programming procedure.

- **FAST CYCLE TIME – 40 ns TYPICAL**
- **FULL MIL AND COMMERCIAL RANGES**
- **FIELD PROGRAMMABLE**
- **ORGANIZATION – 1024 WORDS X 8 BITS**
- **UNCOMMITTED COLLECTORS – 93450**
- **3-STATE OUTPUTS – 93451**
- **FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER**
- **CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION**
- **WIRED-OR CAPABILITY**
- **STANDARD 24-PIN DUAL-IN-LINE PACKAGE**
- **NICHROME FUSE LINKS FOR HIGH RELIABILITY**

PIN NAMES

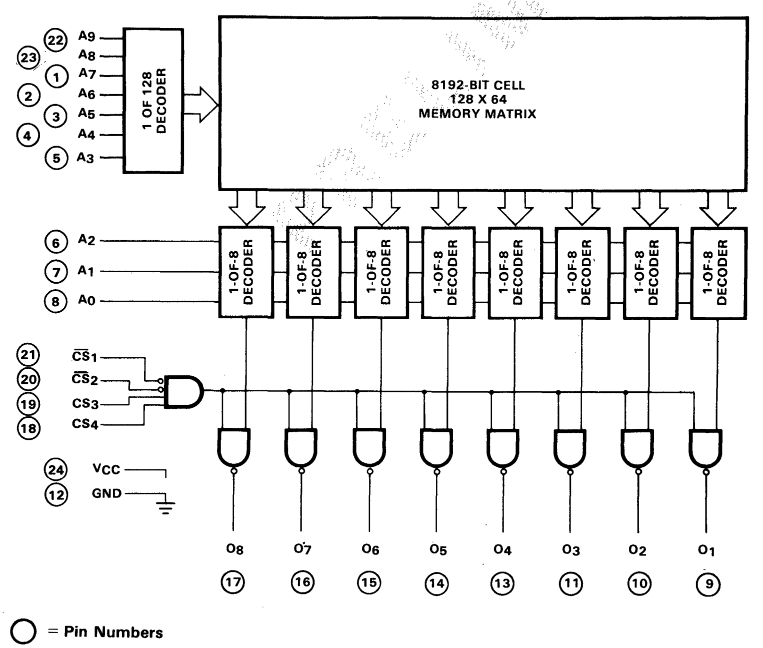
$A_0 - A_9$	Address Inputs
$\overline{CS}_1$, $\overline{CS}_2$, CS_3, CS_4	Chip Select Inputs
$O_1 - O_8$	Data Outputs

LOGIC SYMBOL

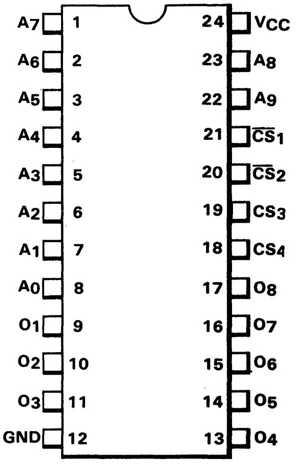


V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTES: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

93452 / 93453

ISOPLANAR SCHOTTKY TTL MEMORY

1024×4-BIT PROGRAMMABLE READ ONLY MEMORY

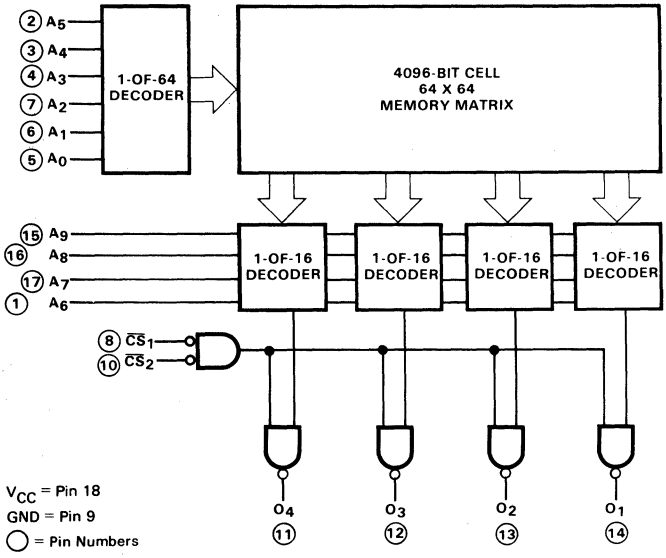
DESCRIPTION – The 93452 and 93453 are fully decoded high speed 4096-bit field Programmable Read Only Memories organized 1024 words by four bits per word. The devices are identical except for the output stages. The 93452 has uncommitted collector outputs, while the 93453 has 3-state outputs. In either case, the outputs are enabled when $\overline{CS}_1$ and $\overline{CS}_2$ are LOW.

- **FULL MIL AND COMMERCIAL RANGES**
- **FAST CYCLE TIME – 35 ns TYP**
- **ORGANIZATION – 1024 WORDS X 4 BITS**
- **UNCOMMITTED COLLECTOR OUTPUTS – 93452**
- **3-STATE OUTPUTS – 93453**
- **FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER**
- **CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION**
- **WIRED-OR CAPABILITY**
- **18-PIN DUAL IN-LINE PACKAGE**
- **REPLACES FOUR 256 X 4 PROMs**

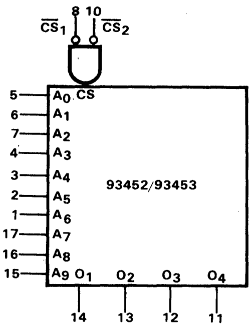
PIN NAMES

A_0 to A_9	Address Inputs
$\overline{CS}_1$, $\overline{CS}_2$	Chip Select Inputs
O_1 to O_4	Data Outputs

LOGIC DIAGRAM

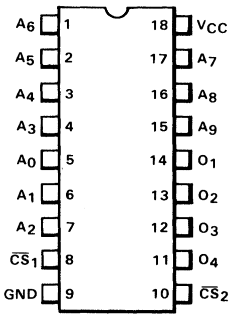


LOGIC SYMBOL



V_{CC} = Pin 18
GND = Pin 9

CONNECTION DIAGRAM
DIP (TOP VIEW)



FUNCTIONAL DESCRIPTION – The 93452 and 93453 are bipolar field Programmable Read Only Memories (PROMs) organized 1024 words by four bits per word. Open collector outputs are provided on the 93452 for use in wired-OR systems. The 93453 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. Chip Selects for both devices are active LOW; conversely, a HIGH (logic "1") on the $\overline{CS}_1$ or $\overline{CS}_2$ will disable all outputs.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_9 inputs, the chip is selected, and data is valid at the outputs after t_{AA} nanoseconds.

Programming (selectively opening nichrome fuse links) is accomplished by following the sequence outlined below.

PROGRAMMING – The 93452 and 93453 are manufactured with all bits in the logic "1" state. Any desired bit (output) can be programmed to a logic "0" state by following the procedure shown below. One may build a programmer to satisfy the specifications or buy any of the commercially available programmers which meet these specifications.

PROGRAMMING SPECIFICATIONS

CHARACTERISTIC	SYMBOL	MIN	RECOMMENDED VALUE	MAX	UNITS	COMMENTS
Address Input	V_{IH} V_{IL}	2.4 0	5.0 0	5.0 0.4	V V	Do not leave inputs open
Chip Select	$\overline{CS}_1,\overline{CS}_2$	2.4	5.0	5.0	V	Pin 8 or 10 or both
Programming Voltage Pulse	V_{OP}	20	21	21	V	Applied to output to be programmed
Programming Pulse Width	t_{pw}	0.05	0.18	50	ms	All bits can be programmed in $\leqslant$ 4.1 sec.
Duty Cycle, Programming Pulse			20	*	%	*Maximum duty cycle to maintain $T_C < 85°C$
Programming Pulse Rise Time	t_r	0.5	1.0	3.0	μs	
Number of Pulses Required		1	4	8		
Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Case Temperature	t_c		25	85	°C	
Programming Pulse Current Max.	I_{OP}			100	mA	If pulse generator is used, set current limit to this max value
Low V_{CC} Read	V_{CC}		4.4	5.0	V	Programming Read Verify

PROGRAMMING SEQUENCE – The Fairchild 93452/93453 may be programmed using the following method.

1. Apply the proper power, $V_{CC} = 5.0$ V, GND = 0 V.
2. Select the word to be programmed by applying the appropriate voltages to the address pins A_0 through A_9.
3. Enable the chip for programming by application of a HIGH (logic "1") to Chip Select ($\overline{CS}_1$), pin 8 or ($\overline{CS}_2$), pin 10 or both.
4. Apply the 21 V programming pulse to the output associated with the bit to be programmed. The other outputs may be left open or tied to any logic "1" (output HIGH), *i.e.,* 2.4 V to V_{CC}. Note that only one output may be programmed at a time.
5. To verify the logic "0" in the bit just programmed, remove the programming pulse from the output and sense it after applying logic "0"s to Chip Select inputs $\overline{CS}_1$ and $\overline{CS}_2$.
6. The above procedure is then repeated to program other bits on the chip.
7. See Chapter 6 for further details.

BOARD PROGRAMMING – To program a single PROM out of a group of "OR" tied memories the following procedure is required. (See Figure 1)

1. Connect all $\overline{CS}_2$ pins to ground.
2. Connect the outputs of a TTL Decoder (supplied by $V_{CC} = +12.6$ V, $V_{EE} = +7.6$ V) to the $\overline{CS}_1$ pins of the memories on the board.
3. Address the decoder such that the particular decoder output connected to the $\overline{CS}_1$ pin of the memory to be programmed will be LOW at +7.8 V. All the other decoder outputs will be HIGH at +10.6 V.
4. Apply the 21 V programming pulse to one group of "OR" tied outputs selected for programming; only the addressed bit in the +7.8 V selected memory will program, all other memories remain deselected (those with $\overline{CS}_1 = +10.6$ V).
5. To verify the logic "0" in the bit just programmed remove programming pulse and sense the "OR" tie after lowering the decoder supplies to the conventional $V_{CC} = +5.0$ V, $V_{EE} = 0$ V.

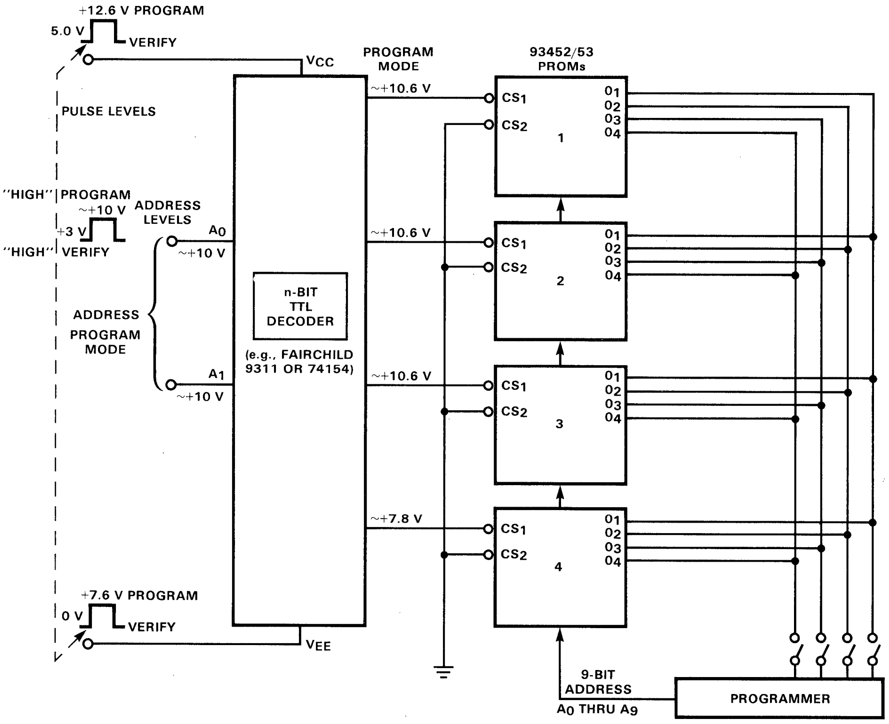


Figure 1

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC}	−0.5 V to +7.0 V
Input Voltages	−0.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltages	−0.5 V to +5.5 V

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
93452XC, 93453XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93452XM, 93453XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Package Information on this data sheet.

DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise noted.

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
I_{CEX}	Output Leakage Current (93452 only)			50	µA	V_{CC} = 5.25 V, V_{CEX} = 4.95 V, 0°C to +75°C Address any HIGH Output
I_{CEX}	Output Leakage Current (93452 only)			100	µA	V_{CC} = 5.5 V, V_{CEX} = 5.2 V, −55°C to +125°C Address any HIGH Output
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA A_9 = +10.8 V, A_2 = 10.8 V
V_{OH}	Output HIGH Voltage (93453 only)	2.4			V	V_{CC} = MIN, I_{OH} = −2.0 mA
I_{off}	Output Leakage Current for HIGH Impedance State (93453 only)			50 −50	µA µA	V_{OH} = 2.4 V V_{OL} = 0.4 V; 0°C to +75°C
I_{off}	Output Leakage Current for HIGH Impedance State (93453 only)			100 −50	µA µA	V_{OH} = 2.4 V V_{OL} = 0.4 V; −55°C to +125°C
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
I_F	Input LOW Current I_{FA} (Address Inputs) I_{FCS} (Chip Select Inputs)		 −160 −160	 −250 −250	 µA µA	V_{CC} = MAX, V_F = 0.45 V
I_R	Input HIGH Current I_{RA} (Address Inputs) I_{RCS} (Chip Select Input)			 40 40	 µA µA	V_{CC} = MAX, V_R = 2.4 V
I_{CC}	Power Supply Current		120	170	mA	V_{CC} = MAX, Outputs Open Inputs Grounded and Chip Selected
C_O	Output Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
C_{IN}	Input Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
V_C	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_A = −18 mA

AC CHARACTERISTICS: T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%

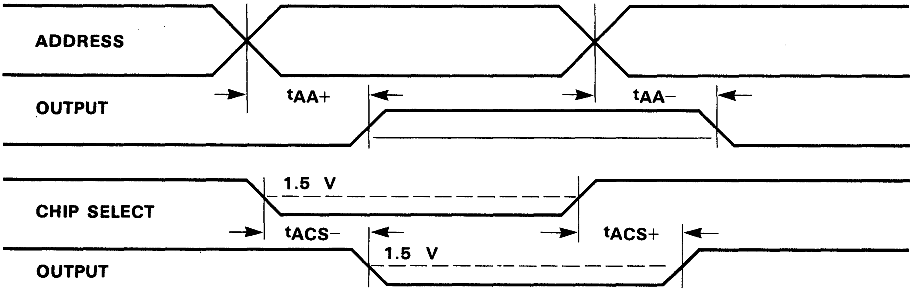
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-} t_{AA+}	Address to Output Access Time		30 30	55 55	ns ns	See Figure 1A and 1B
t_{ACS-} t_{ACS+}	Chip Select Access Time		15 15	25 25	ns ns	

AC CHARACTERISTICS: T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%

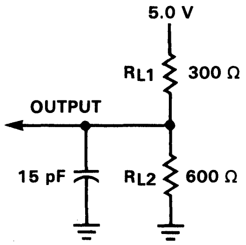
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-} t_{AA+}	Address to Output Access Time		30 30	70 70	ns ns	See Figure 1A and 1B
t_{ACS-} t_{ACS+}	Chip Select Access Time		15 15	30 30	ns ns	

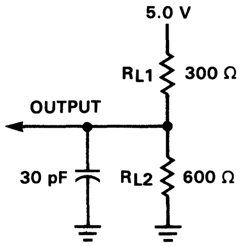
Note 1: Typical limits are at V_{CC} = 5.0 V, +25°C and max loading.

AC WAVEFORMS



AC TEST OUTPUT LOAD





93454
ISOPLANAR SCHOTTKY TTL MEMORY
1024×8-BIT READ ONLY MEMORY

DESCRIPTION – The 93454 is a fully decoded 8192-bit Read Only Memory organized 1024 words by eight bits per word. The 93454 has uncommitted collector outputs. The device is enabled when $\overline{CS}_1$ and $\overline{CS}_2$ are LOW and CS_3 and CS_4 are HIGH.

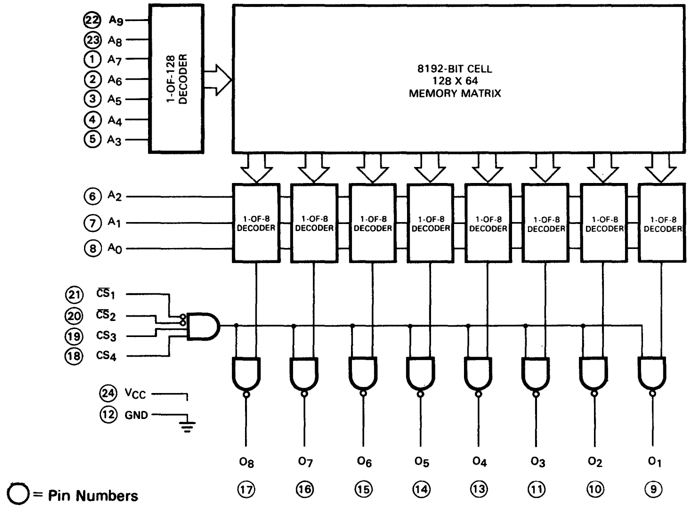
The contents of the memory are mask programmed to the customer's specifications. The customer can specify the desired ROM code on punched cards using the 93454 Data Card Format or on the 4K/8K-bit TTL ROM and PROM Customer Coding Form.

- **FULL MIL AND COMMERCIAL RANGES**
- **ADVANCED ISOPLANAR SCHOTTKY TECHNOLOGY**
- **ORGANIZATION – 1024 WORDS X 8 BITS**
- **UNCOMMITTED COLLECTOR OUTPUTS – 93454**
- **FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER**
- **FOUR CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION**
- **WIRED-OR CAPABILITY**
- **STANDARD 24-PIN DUAL IN-LINE PACKAGES**
- **ACCESS TIME – 45 ns MAX (0°C – 75°C)**

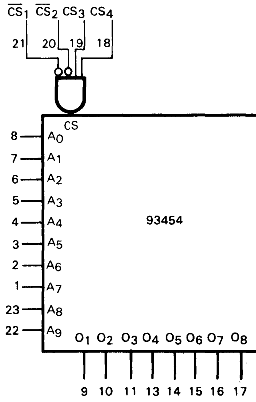
PIN NAMES

$\overline{CS}_1$, $\overline{CS}_2$, CS_3, CS_4	Chip Select Inputs
$A_0 - A_9$	Address Inputs
$O_1 - O_8$	Data Outputs

LOGIC DIAGRAM



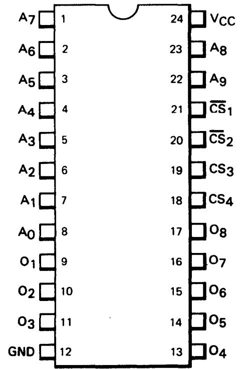
LOGIC SYMBOL



V_{CC} = Pin 24

GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC}	−0.5 V to +7.0 V
Input Voltage	−0.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltages	−0.5 V to V_{CC}

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
93454XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93454XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = Package type; D for Ceramic DIP, P for Plastic DIP, F for Flatpak. See Package Information on this data sheet.

FUNCTIONAL DESCRIPTION – The 93454 is a bipolar Read Only Memory (ROM) organized 1024 words by eight bits per word. Open collector outputs are provided on the 93454 for use in wired-OR systems. Chip Select follows the logic equation: $\overline{CS}_1 \bullet \overline{CS}_2 \bullet CS_3 \bullet CS_4 = CS$; *i.e.,* if $\overline{CS}_1$ and $\overline{CS}_2$ are both active LOW and CS_3 and CS_4 are both active HIGH, all eight outputs are enabled; for any other condition all eight outputs are disabled.

The read function is identical to that of any other conventional bipolar ROM. That is, a binary address is applied to the $A_0 - A_9$ inputs, the chip is selected, and data is valid at the outputs after t_{AA} nanoseconds.

DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise noted.

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
I_{CEX}	Output Leakage Current			50	μA	V_{CC} = MAX, $V_{CEX} = V_{CC}$, 0°C to +75°C Address any HIGH Output
I_{CEX}	Output Leakage Current			100	μA	V_{CC} = MAX, $V_{CEX} = V_{CC}$, −55°C to +125°C Address any HIGH Output
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA Address any LOW Output
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
I_F	Input LOW Current I_{FA} (Address Inputs) I_{FCS} (Chip Select Inputs)		 −160 −160	 −250 −250	 μA μA	V_{CC} = MAX, V_F = 0.45 V
I_R	Input HIGH Current I_{RA} (Address Inputs) I_{RCS} (Chip Select Input)			 40 40	 μA μA	V_{CC} = MAX, V_R = 2.4 V
I_{CC}	Power Supply Current		110	150	mA	V_{CC} = MAX, Outputs Open Inputs Grounded and Chip Selected
C_O	Output Pin Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
C_I	Input Pin Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
V_C	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_A = −18 mA

AC CHARACTERISTICS: $T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$

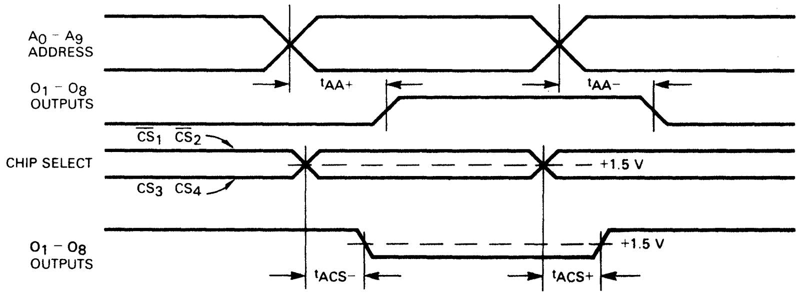
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-} t_{AA+}	Address to Output Access Time		30 30	45 45	ns ns	See Figure 1
t_{ACS-} t_{ACS+}	Chip Select Access Time		20 20	30 30	ns ns	

AC CHARACTERISTICS: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$

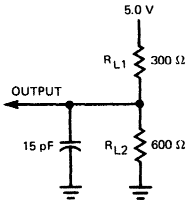
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-} t_{AA+}	Address to Output Access Time		30 30	60 60	ns ns	See Figure 1
t_{ACS-} t_{ACS+}	Chip Select Access Time		20 20	40 40	ns ns	

Note (1): Typical values are at $V_{CC} = 5.0\ V$, $T_A = +25°C$, and MAX loading.

AC WAVEFORM



AC TEST OUTPUT LOAD



15 mA Load

Fig. 1

93457
ISOPLANAR SCHOTTKY TTL MEMORY
256×4-BIT READ ONLY MEMORY

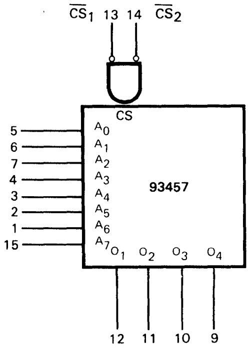
DESCRIPTION – The 93457 is a fully decoded high speed 1024-bit Read Only Memory organized 256 words by four bits per word. The 93457 has uncommitted collector outputs. The outputs are off when either of the CS inputs are in the HIGH state. The contents of the memory are mask programmed to the customers specification. The customer can specify the desired ROM code on the 4-bit/word Coding Form. Electrical characteristics are the same as the 93417.

- **FULL MIL AND COMMERCIAL RANGES**
- **512 x 4 BITS PER WORD**
- **UNCOMMITTED COLLECTOR OUTPUTS**
- **SEE 93417 FOR ELECTRICALS**
- **STANDARD 16-PIN DUAL IN-LINE PACKAGE**
- **FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER**
- **CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION**
- **WIRED-OR CAPABILITY**
- **FAST CYCLE TIME – 25 ns TYP**
- **POWER DISSIPATION – 425 mW TYP**

PIN NAMES

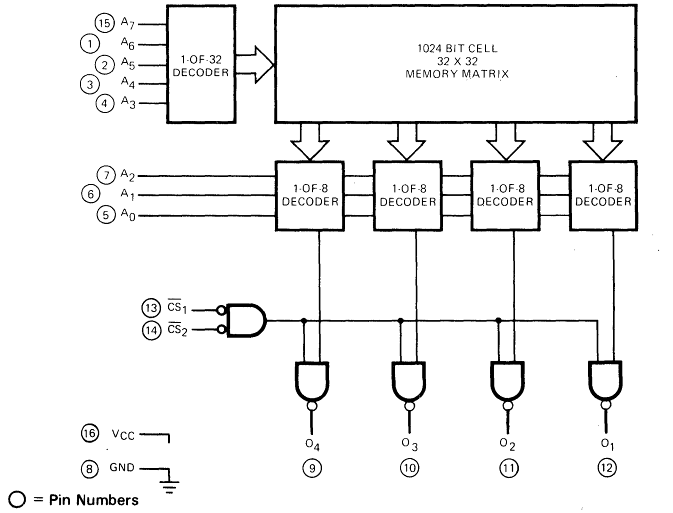
$A_0 - A_7$	Address Inputs
$\overline{CS}_1$, $\overline{CS}_2$	Chip Select Inputs
$O_1 - O_4$	Data Outputs

LOGIC SYMBOL

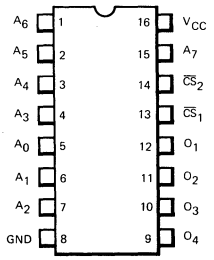


V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



CONNECTION DIAGRAM



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

93458/93459
ISOPLANAR SCHOTTKY TTL FPLA
16 × 48 × 8 FIELD PROGRAMMABLE LOGIC ARRAY

DESCRIPTION – The 93458 and 93459 are high-speed bipolar Field Programmable Logic Arrays organized with 16 inputs, 48 product terms and 8 outputs. The 16 inputs and their complements are fuse linked to the inputs of 48 AND gates (48 product terms). Each of the 48 AND gates are fuse linked to 8 48-input OR gates (8 summing terms). Each output may be programmed active HIGH or active LOW. The devices are identical except for the output stage. The 93458 has uncommitted collector outputs while the 93459 has 3-state outputs. In either case, the outputs are enabled when $\overline{CS}$ is LOW.

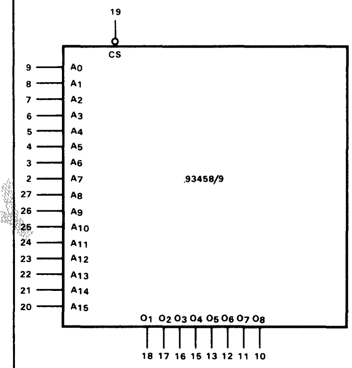
- **FIELD PROGRAMMABLE (NICHROME FUSE LINKS)**
- **FULL MIL AND COMMERCIAL RANGES**
- **FAST CYCLE TIME – 25 ns TYP**
- **ORGANIZATION – 16 INPUTS x 48 PRODUCT TERMS x 8 OUTPUTS**
- **UNCOMMITTED COLLECTOR OUTPUTS – 93458**
- **3-STATE OUTPUTS – 93459**
- **CHIP SELECT PROVIDES EASY MEMORY EXPANSION**
- **28-PIN PACKAGE**

PRELIMINARY

PIN NAMES

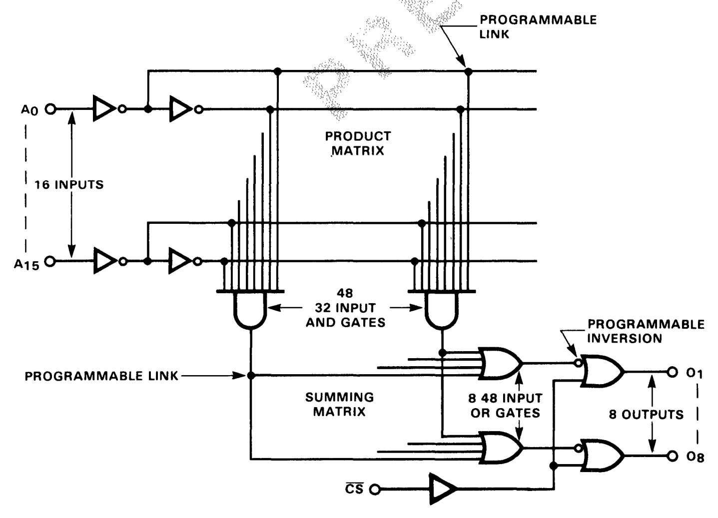
$A_0 - A_{15}$	Address Inputs
$\overline{CS}$	Chip Select Input
$O_1 - O_8$	Data Outputs

LOGIC SYMBOL

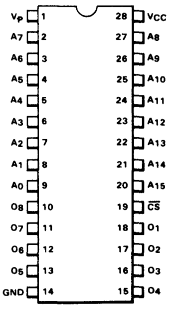


V_{CC} = Pin 28
GND = Pin 14
V_P = Pin 1

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



LOGIC RELATIONSHIPS

Input Term	A_n	$n = 0, \ldots, 15$, one of 16 inputs
Product Term	$P_m = \Pi_{0}^{15}(i_nA_n + j_n\overline{A_n})$	$m = 0, \ldots, 47$, one or 48 product terms where: a) $i_n = j_n = 0$ for unprogrammed input b) $i_n = \overline{j_n}$ for programmed input c) $i_n = j_n = 1$ for don't care input
	$F_r = \Sigma_{0}^{47} P_m$	$r = 1, \ldots, 8$, the OR function of the 48 products terms
Summing Term	$S_r = \Sigma_{0}^{47} k_mP_m$	where $k_m = 0$ for product term inactive (programmed) $k_m = 1$ for product term active (unprogrammed)

				OUTPUT	
MODE	$\overline{CS}$	F_r	S_r	ACTIVE HIGH	ACTIVE LOW
READ	0	1	0	0	1
	0	1	1	1	0
	0	0	X	0	1
DISABLE	1	X	X	1 (93458)	1 (93458)
	1	X	X	HI Z (93459)	HI Z (93459)

93464
ISOPLANAR SCHOTTKY TTL MEMORY
1024×8-BIT READ ONLY MEMORY

DESCRIPTION – The 93464 is a fully decoded 8192-bit Read Only Memory organized 1024 words by eight bits per word. The 93464 has 3-state outputs. The device is enabled when $\overline{CS}_1$ and $\overline{CS}_2$ are LOW and CS_3 and CS_4 are HIGH.

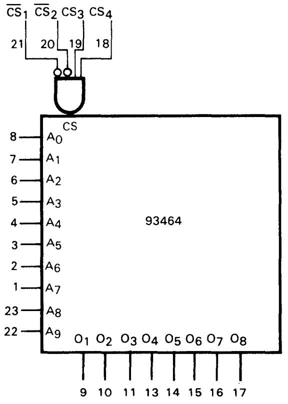
The contents of the memory are mask programmed to the customer's specification. The customer can specify the desired ROM code on punched cards using the 93464 Data Card Format or on the 4K/8K-bit TTL ROM and PROM Customer Coding Form.

- **FULL MIL AND COMMERCIAL RANGES**
- **ADVANCED ISOPLANAR SCHOTTKY TECHNOLOGY**
- **ORGANIZATION – 1024 WORDS X 8 BITS**
- **3-STATE OUTPUTS**
- **FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER**
- **FOUR CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION**
- **WIRED-OR CAPABILITY**
- **STANDARD 24-PIN DUAL IN-LINE PACKAGES**
- **ACCESS TIME – 45 ns MAX (0°C – 75°C)**

PIN NAMES

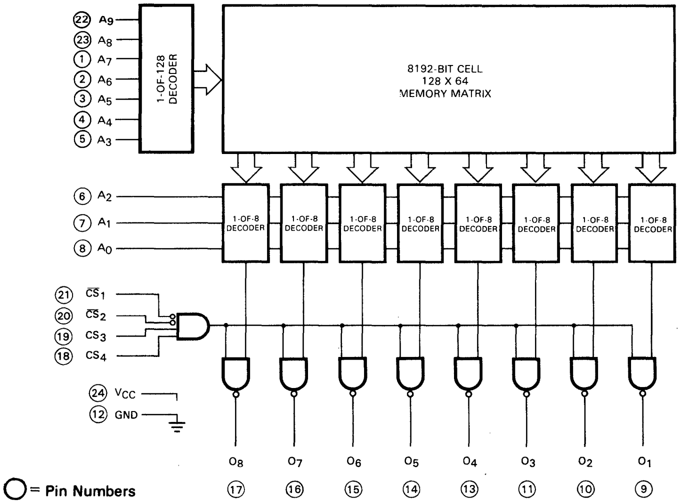
$\overline{CS}_1$, $\overline{CS}_2$, CS_3, CS_4	Chip Select Inputs
$A_0 - A_9$	Address Inputs
$O_1 - O_8$	Data Outputs

LOGIC SYMBOL

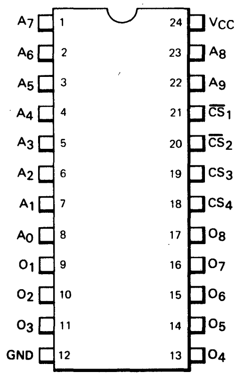


V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC}	−0.5 V to +7.0 V
Input Voltage	−0.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltages	−0.5 V to V_{CC}

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC}) MIN	SUPPLY VOLTAGE (V_{CC}) TYP	SUPPLY VOLTAGE (V_{CC}) MAX	TEMPERATURE
93464XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93464XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = Package type; D for Ceramic DIP, P for Plastic DIP, F for Flatpak. See Package Information on this data sheet.

FUNCTIONAL DESCRIPTION – The 93464 is a bipolar Read Only Memory (ROM) organized 1024 words by eight bits per word. The 93464 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. Chip Select follows the logic equation: $\overline{CS}_1 \bullet \overline{CS}_2 \bullet CS_3 \bullet CS_4 = CS$; *i.e.,* if $\overline{CS}_1$ and $\overline{CS}_2$ are both active LOW and CS_3 and CS_4 are both active HIGH, all eight outputs are enabled; for any other condition all eight outputs are disabled.

The read function is identical to that of any other conventional bipolar ROM. That is, a binary address is applied to the $A_0 - A_9$ inputs, the chip is selected, and data is valid at the outputs after t_{AA} nanoseconds.

DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise noted.

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA Address any LOW Output	
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = MIN, I_{OH} = −2.0 mA	
I_{off}	Output Leakage Current for HIGH Impedance State			50 −50	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	0°C to +75°C
I_{off}	Output Leakage Current for HIGH Impedance State			100 −50	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	−55°C to +125°C
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
I_F	Input LOW Current I_{FA} (Address Inputs) I_{FCS} (Chip Select Inputs)		 −160 −160	 −250 −250	 μA μA	V_{CC} = MAX, V_F = 0.45 V	
I_R	Input HIGH Current I_{RA} (Address Inputs) I_{RCS} (Chip Select Input)			 40 40	 μA μA	V_{CC} = MAX, V_R = 2.4 V	
I_{CC}	Power Supply Current		110	150	mA	V_{CC} = MAX, Outputs Open Inputs Grounded and Chip Selected	
C_O	Output Pin Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz	
C_I	Input Pin Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz	
V_C	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_A = −18 mA	

AC CHARACTERISTICS: T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%

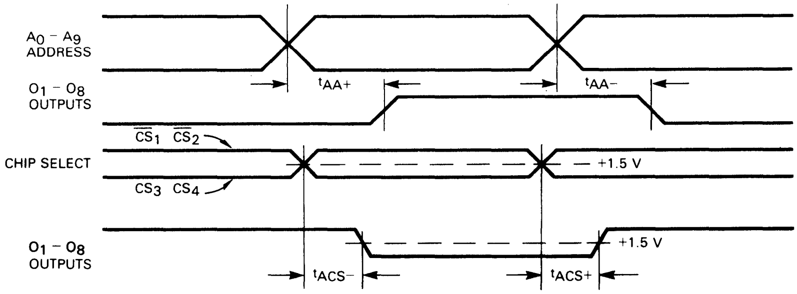
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-} t_{AA+}	Address to Output Access Time		30 30	45 45	ns ns	See Figure 1
t_{ACS-} t_{ACS+}	Chip Select Access Time		20 20	30 30	ns ns	

AC CHARACTERISTICS: T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%

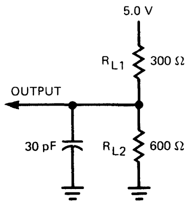
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 1)	MAX		
t_{AA-} t_{AA+}	Address to Output Access Time		30 30	60 60	ns ns	See Figure 1
t_{ACS-} t_{ACS+}	Chip Select Access Time		20 20	40 40	ns ns	

Note (1): Typical values are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.

AC WAVEFORM



AC TEST OUTPUT LOAD



15 mA Load

Fig. 1

93467
ISOPLANAR SCHOTTKY TTL MEMORY
256×4-BIT READ ONLY MEMORY

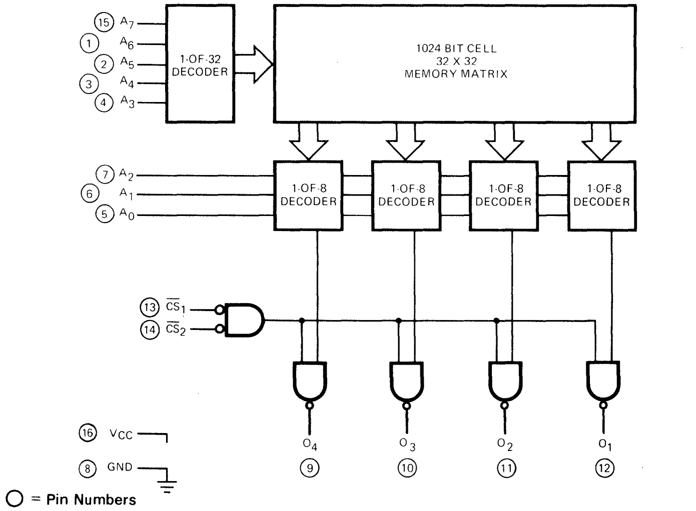
DESCRIPTION – The 93467 is a fully decoded high speed 1024-bit Read Only Memory organized 256 words by four bits per word. The 93467 has 3-state outputs. The outputs are off when either of the CS inputs are in the HIGH state. The contents of the memory are mask programmed to the customers specification. The customer can specify the desired ROM code on the 4-bit/word Coding Form. The electrical characteristics are the same as the 93427.

- **FULL MIL AND COMMERCIAL RANGES**
- **ORGANIZATION 512 x 4 BITS PER WORD**
- **SEE 93427 FOR ELECTRICALS**
- **3-STATE OUTPUTS**
- **STANDARD 16-PIN DUAL IN-LINE PACKAGE**
- **FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER**
- **CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION**
- **WIRED-OR CAPABILITY**
- **FAST CYCLE TIME – 25 ns TYP**
- **POWER DISSIPATION – 425 mW TYP**

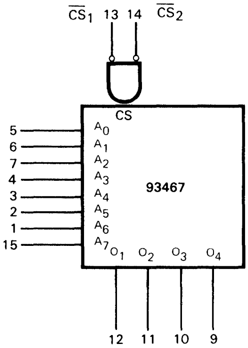
PIN NAMES

$A_0 - A_7$	Address Inputs
$\overline{CS}_1, \overline{CS}_2$	Chip Select Inputs
$O_1 - O_4$	Data Outputs

LOGIC DIAGRAM

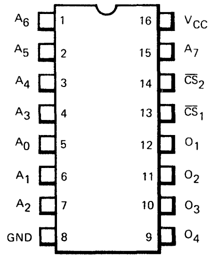


LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

TTL ISOPLANAR MEMORY 93470/93471

4096 × 1-BIT FULLY DECODED RANDOM ACCESS MEMORY

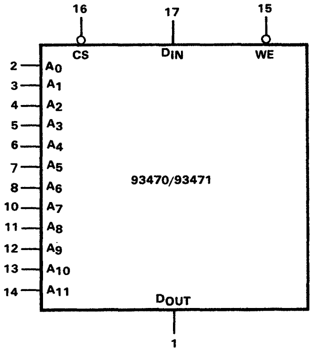
DESCRIPTION – The 93470 and 93471 are 4096-bit TTL Read/Write Random Access Memories organized 4096 words by one bit. The devices are identical except for the output stage. The 93470 has an uncommitted collector output, while the 93471 has a 3-state output. The devices have full decoding on chip, separate Data Input and Data Output lines and active LOW Chip Select lines. They are designed for high performance main memory application and can be used to replace four 1024-bit RAMs.

- **FULL MIL AND COMMERCIAL RANGES**
- **ORGANIZATION – 4096 WORDS X 1 BIT**
- **READ ACCESS TIME – 50 ns TYPICAL**
- **CHIP SELECT ACCESS TIME – 25 ns TYPICAL**
- **UNCOMMITTED COLLECTOR OUTPUT – 93470**
- **3-STATE OUTPUTS – 93471**
- **NON-INVERTING DATA OUTPUT**
- **POWER DISSIPATION – 0.22 mW/BIT TYPICAL**
- **REPLACES FOUR 1024 BY ONE RAMs**

PIN NAMES

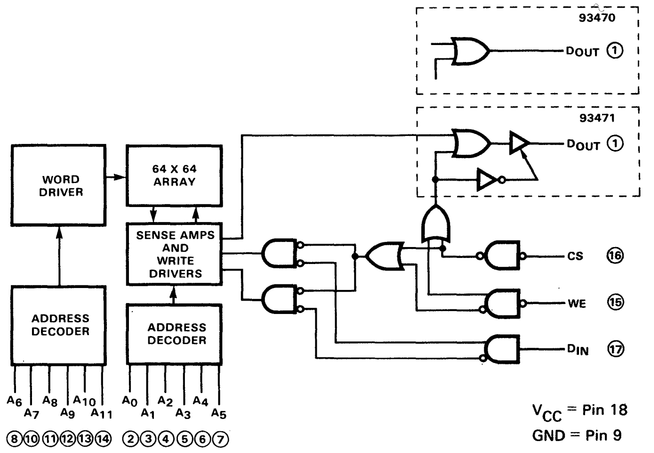
$\overline{CS}$	Chip Select Input
$A_0 - A_{11}$	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

LOGIC SYMBOL



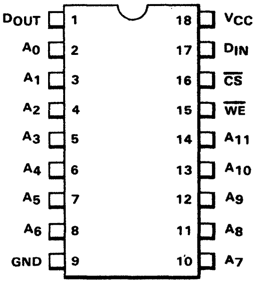
V_{CC} = Pin 18
GND = Pin 9

LOGIC DIAGRAM



V_{CC} = Pin 18
GND = Pin 9
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



FUNCTIONAL DESCRIPTION – The 93470 and 93471 are fully decoded 4096-bit Random Access Memories organized 4096 words by one bit. Word selection is achieved by means of a 12-bit address, A_0 thru A_{11}.

The Chip Select input is provided for logic flexibility. For larger memories, the fast Chip Select access time permits the decoding of Chip Select, $\overline{CS}$, from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable, $\overline{WE}$ (pin 5). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at the Data Outputs.

The 93471 has 3-state outputs which provide drive capability for higher speeds with high capacitive load systems. The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus.

The 93470 has uncommitted collector outputs to allow maximum flexibility in output connection. In many applications, such as memory expansion, the outputs of several 93470s can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of value R_L must be used to provide a HIGH at the output when it is off. Any value of R_L within the range specified below may be used.

$$\frac{V_{CC}(\max)}{8 - \text{F.O.}\ (1.6)} \leqslant R_L \leqslant \frac{V_{CC}(\min) - V_{OH}}{N\ (I_{CEX}) + \text{F.O.}\ (0.04)}$$

R_L is in kΩ
N = number of wired-OR outputs tied together
F.O. = number of TTL Unit Loads (U.L.) driven
I_{CEX} = Memory Output Leakage Current in mA
V_{OH} = Required Output HIGH level at Output Node

The minimum value of R_L is limited by output current sinking ability. The maximum value of R_L is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}.

TRUTH TABLE

INPUTS			OUTPUTS		MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	93470 O.C.	93471 3-STATE	
H	X	X	H	HIGH Z	Not Selected
L	L	L	H	HIGH Z	Write "0"
L	L	H	H	HIGH Z	Write "1"
L	H	X	D_{OUT}	D_{OUT}	Read

H = HIGH Voltage; L = LOW Voltage; X = Don't Care (HIGH or LOW)
HIGH Z = High Impedance; OC = Open Collector

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage (dc)*	−0.5 V to +5.5 V
Input Current (dc)*	−12 mA to +5.0 mA
Voltage Applied to Outputs (output HIGH)**	−0.5 V to +5.50 V
Output Current (dc)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93470XC, 93471XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93470XM, 93471XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type, F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2, 4)

SYMBOL	CHARACTERISTIC		LIMITS			UNITS	CONDITIONS	
			MIN	TYP (Note 3)	MAX			
V_{OL}	Output LOW Voltage			0.3	0.45	V	V_{CC} = MIN, I_{OL} = 8 mA	
V_{IH}	Input HIGH Voltage		2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage			1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current			−250	−400	μA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
V_{CD}	Input Diode Clamp Voltage			−1.0	−1.5	V	V_{CC} = MAX, V_{IN} = −10 mA	
I_{CEX}	Output Leakage Current	93470		1.0	100	μA	V_{CC} = MAX, V_{OUT} = 4.5 V	
I_{OFF}	Output Current (HIGH Z)	93471			50	μA	V_{CC} = MAX, V_{OUT} = 2.4 V	
					−50		V_{CC} = MAX, V_{OUT} = 0.5 V	
V_{OH}	Output HIGH Voltage	93471	2.4			V	V_{CC} = MIN, I_{OH} = −5.2 mA	
I_{OS}	Output Current Short Circuit to Ground	93471			−100	mA	V_{CC} = MAX, Note 7	
I_{CC}	Power Supply Current	93470/71XC		170		mA	T_A = +75°C	V_{CC} = MAX, All Inputs and Outputs Open
		93470/71XC		190			T_A = 0°C	
		93470/71XM		155			T_A = +125°C	
		93470/71XM		205			T_A = −55°C	

AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

SYMBOL	CHARACTERISTIC	93470/71XC			93470/71XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Time		25			25		ns	See Test Circuit and Waveforms
t_{RCS}	Chip Select Recovery Time (93470)		25			25			
t_{ZRCS}	Chip Select to HIGH Z (93471)		25			25			
t_{AOS}	Output Enable Time		25			25			
t_{ROS}	Output Enable Recovery Time (93470)		25			25			
t_{ZROS}	Output Enable to HIGH Z (93471)		25			25			
t_{AA}	Address Access Time		30			30			
WRITE MODE	DELAY TIMES								
t_{WS}	Write Disable Time (93470)		20			20		ns	See Test Circuit and Waveforms
t_{ZWS}	Write Disable to HIGH Z (93471)		20			20			
t_{WR}	Write Recovery Time		25			25			
	INPUT TIMING REQUIREMENTS								
t_W	Write Pulse Width (to guarantee write)		30			30		ns	
t_{WSD}	Data Set-Up Time Prior to Write		0			0			
t_{WHD}	Data Hold Time After Write		0			0			
t_{WSA}	Address Set-Up Time		0			0			
t_{WHA}	Address Hold Time		0			0			
t_{WSCS}	Chip Select Set-Up Time		0			0			
t_{WHCS}	Chip Select Hold Time		0			0			
C_I	Input Pin Capacitance		4			4		pF	Measure with Pulse Technique
C_O	Output Pin Capacitance		7			7			

NOTES:

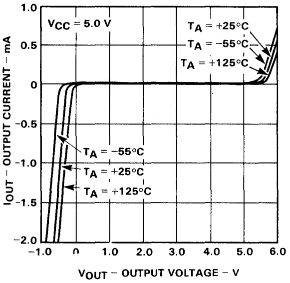
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 15°C/Watt, Flatpak.

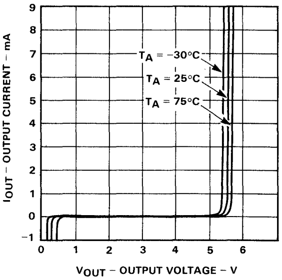
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.

TYPICAL ELECTRICAL CHARACTERISTIC CURVES

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH) (93470 ONLY)

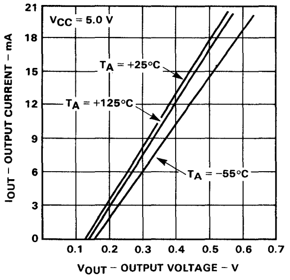


OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH Z STATE) (93471 ONLY)

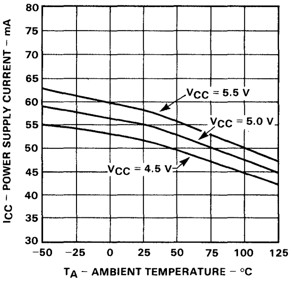


93470/93471

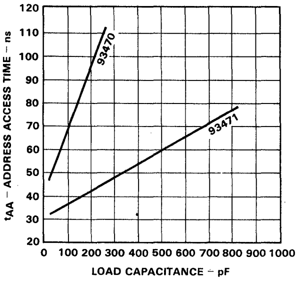
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



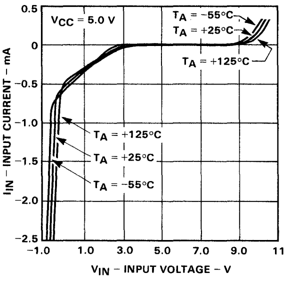
POWER SUPPLY CURRENT VERSUS TEMPERATURE



ADDRESS ACCESS TIME VERSUS LOAD CAPACITANCE

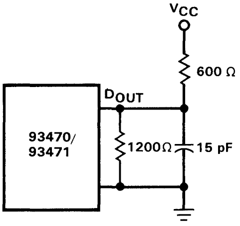


INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS TEMPERATURE

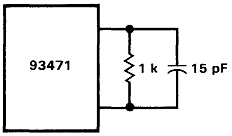


AC TEST LOAD AND WAVEFORM

LOADING CONDITIONS

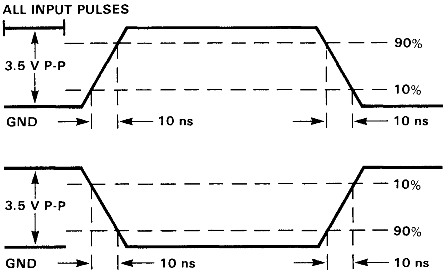


Load A

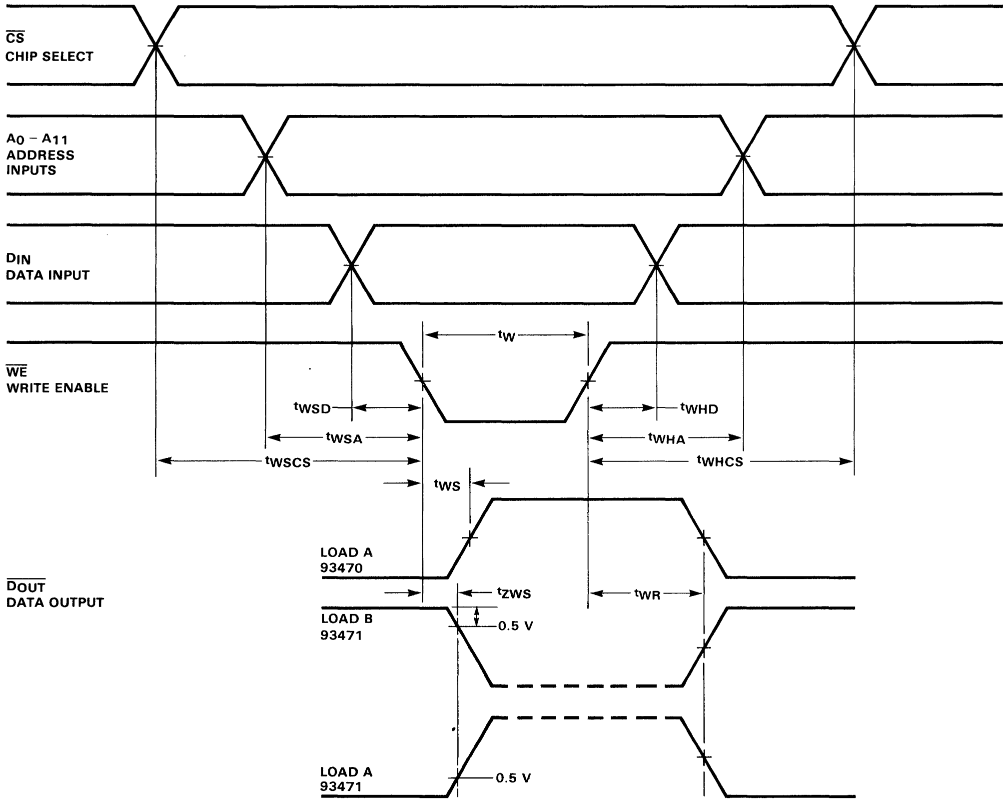


Load B

INPUT PULSES



WRITE MODE

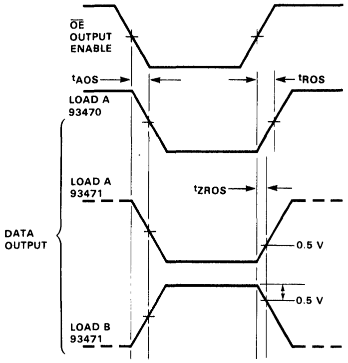


(All above measurements referenced to 1.5 V unless otherwise indicated)

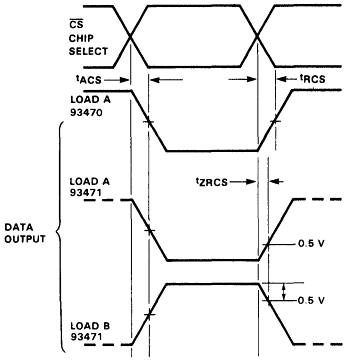
NOTE: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

READ MODE

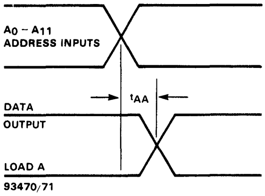
PROPAGATION DELAY FROM OUTPUT ENABLE



PROPAGATION DELAY FROM CHIP SELECT



PROPAGATION DELAY FROM ADDRESS INPUTS



93481/93481A

ISOPLANAR INTEGRATED INJECTION LOGIC MEMORY

4096 × 1-BIT DYNAMIC RANDOM ACCESS MEMORY

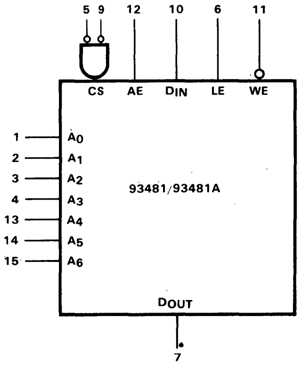
DESCRIPTION – The Fairchild 93481 and 93481A are address multiplexed fully decoded 4096 x 1 bipolar dynamic RAMs. The inputs and output are conventional TTL. The first five address inputs are latched with AE and the last seven are applied after AE and are used in conventional "ripple-through" fashion.

- **4096 X 1 BIT PER WORD**
- **FULLY TTL COMPATIBLE – NO SPECIAL CLOCK DRIVERS REQUIRED**
- **ADDRESS MULTIPLEXED**
- **ON-CHIP DATA LATCH**
- **STANDARD 16-PIN DUAL IN-LINE PACKAGE**
- **32-LINE REFRESH – 2 ms REFRESH INTERVAL**
- **ACCESS TIME 120 ns MAX (93481), 100 ns MAX (93481A)**
- **CYCLE TIME 280 ns MIN (93481), 240 ns MIN (93481A)**
- **POWER DISSIPATION 45 mW STANDBY, 350 mW TYPICAL AT MIN CYCLE TIME**
- **3-STATE OUTPUT**
- **TEMPERATURE RANGE 0°C – 70°C**

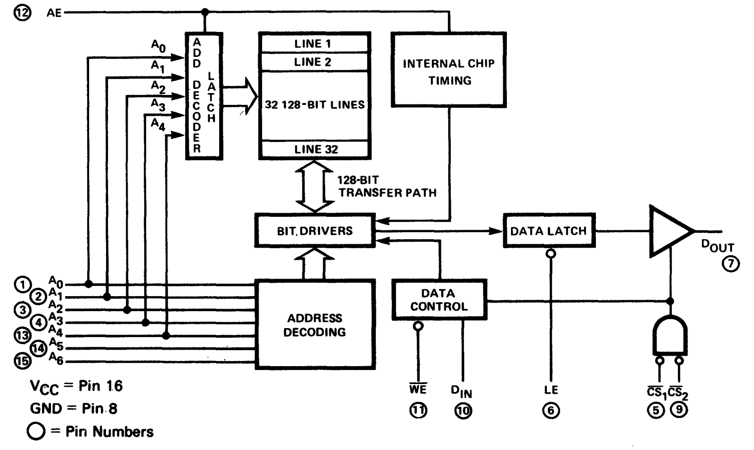
PIN NAMES

A_0-A_4	Multiplexed Address Inputs
A_5-A_6	Non-multiplexed Address Inputs
$\overline{CS}_1, \overline{CS}_2$	Chip Select Inputs
D_{OUT}	Data Output
LE	Output Latch Enable
D_{IN}	Data Input
AE	Address Enable
$\overline{WE}$	Write Enable

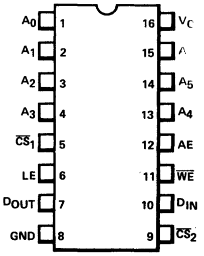
LOGIC SYMBOL



LOGIC DIAGRAM



CONNECTION DIAGRAM DIP(TOP VIEW)



FUNCTIONAL DESCRIPTION

Addressing — The storage array is organized in 32 rows of 128 cells. Twelve bits of address information are required to uniquely define one storage cell out of 4096. To accomplish this within the constraints of a 16-pin package, the 93481/93481A operates in conjunction with external addressing logic to examine sequentially five bits (ROW address) and then seven bits (COLUMN) of address information. Signals on the $A_0 - A_4$ inputs must be in the desired state at least a set-up time t_{AS} before the AE signal goes HIGH and must then remain fixed for at least the hold time t_{AH}. These timing requirements insure that the positive-going AE signal latches the $A_0 - A_4$ information into the internal row addressing logic. To complete the addressing operation, the AE signal must remain HIGH and the external addressing logic must present the final seven bits of the address on the $A_0 - A_6$ inputs.

Read Operation — The Write Enable input $\overline{WE}$ must be in the HIGH state for a read operation. After addressing a cell as outlined above, its content will exit via the output latch, which is transparent when the Latch Enable input LE is HIGH. The access delay t_{CAA} is measured from the time that the column address becomes valid, as is the latch input set-up time t_{ALS}. This latter parameter defines the earliest time that LE can go LOW and still insure that the desired data will be latched in. The latest time that LE can go LOW, for the purpose of retaining the data, is determined by two constraints. LE must go LOW no later than t_{ALH}, measured with respect to an address change. Also, LE must go LOW no later than t_{LH}, which is measured with respect to the negative-going edge of AE. If the LE signal timing satisfies these constraints, the latch will retain the data for as long as desired. A subsequent read or write operation will not affect the state of the latch so long as LE remains LOW. If LE subsequently goes HIGH while AE is LOW, the latch will no longer retain the data and its output will go to the high impedance state. It will then remain in this condition so long as AE remains LOW, regardless of the LE input signal.

If either or both Chip Select inputs are HIGH, D_{OUT} will be in the high impedance state.

Write Operation — After addressing a cell in the manner previously described, a LOW signal on $\overline{WE}$ will cause the data on the D_{IN} input to be stored, provided that both Chip Select inputs are LOW. To avoid writing in the wrong cell, $\overline{WE}$ should not go LOW before the column address set-up time t_{WSA}, and the address inputs should not be changed until after the address hold time t_{WHA}. Both the set-up time and hold time for D_{IN} are measured with respect to the trailing (i.e., positive-going) edge of the write pulse. If LE is HIGH during a write operation, D_{OUT} will go HIGH regardless of the state of D_{IN}. After $\overline{WE}$ goes HIGH at the end of a write pulse, the D_{OUT} signal will be the same as the data just stored, assuming that the address remains constant and both Chip Select inputs remain LOW.

Refresh — A normal read or write cycle causes all cells in the addressed row to be refreshed. Also, cycling AE such that the t_{TA} and t_{TR} requirements are met refreshes all cells in the addressed row, regardless of the $\overline{WE}$ and $\overline{CS}$ input signals. Each row must be refreshed at intervals of 2 ms or less.

Power Dissipation — There are three distinct power states in the 93481/93481A. When AE is HIGH the I_{CC} current is typically 100 mA. When AE is LOW, I_{CC} is typically 20 mA if the output latch is retaining data or 10 mA if the latch is not retaining data. When AE goes from LOW to HIGH the resultant increase in I_{CC} is not accompanied by any significant overshoot above the quiescent value. In a cyclical mode corresponding to minimum cycle time the average I_{CC} is 65 mA. No significant current transients occur when inputs other than AE change state.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage (dc)	−0.5 V to +5.5 V
Input Current (dc)	−12 mA to +5.0 mA
Voltage Applied to Output (Output High)	−0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA

GUARANTEED OPERATING RANGE

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE (T_A) (Note 4)
	MIN	TYP	MAX	
93481/93481A	4.75 V	5.0 V	5.25 V	0°C to +70°C

DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2, 4)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		MIN	TYP (Note 3)	MAX			
V_{OL}	Output LOW Voltage		0.3	0.5	V	V_{CC} = MIN, I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current		−100	−400	μA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		10	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
				1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
I_{OFF}	Output Current (HIGH Z)		10	100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V	
			−10	−50	μA	V_{CC} = MAX, V_{OUT} = 0.5 V	
I_{OS}	Output Current Short Circuit to Ground		−55	−100	mA	V_{CC} = MAX, Note 7	
V_{OH}	Output HIGH Voltage	2.4	3.0		V	I_{OH} = −5 mA, V_{CC} = MIN	
V_{CD}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA	
I_{CC}	Power Supply Current		65		mA	MIN CYCLE TIME	V_{CC} = MAX, All Remaining Inputs Grounded
			100		mA	AE = HIGH	
			9.0		mA	AE = LOW, LE = HIGH	

NOTES:

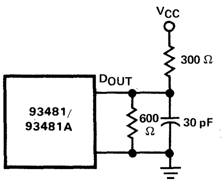
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Operating Ambient Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA}, t_{WSDE}, and t_{WHD} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.
8. Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

AC CHARACTERISTICS OVER GUARANTEED OPERATING RANGES (Notes 5, 6)

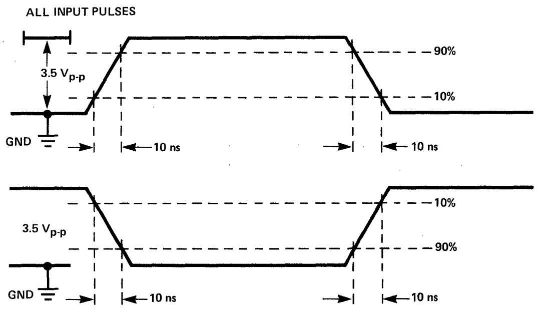
SYMBOL	CHARACTERISTICS	93481			UNITS
		MIN	TYP	MAX	
MULTIPLEX					
t_{AS}	Row Address Set-up Time	0			ns
t_{AH}	Row Address Hold Time	45			
t_{TA}	AE Active Time	150			
t_{TR}	AE Recovery Time	130			
READ CYCLE					
t_{CAA}	Column Address Access Time			75	ns
t_{CAH}	Output Valid Time After Column Address		10		
t_{CSA}	Chip Select Access Time		35		
t_{CSR}	Chip Select Recovery Time		30		
t_{TH}	Output Valid Time After AE		15		
DATA LATCH					
t_{ALS}	Address Set-up Time Before LE	75			ns
t_{ALH}	Address Hold Time After LE		0		
t_{LH}	AE Hold Time After LE		–10		
t_{LR}	Output Recovery from LE		35		
t_{DLA}	Output Valid Time After LE		10		
WRITE CYCLE					
t_{W}	Write Pulse Width	25			ns
t_{WSA}	Address Set-up Time	35			
t_{WHA}	Address Hold Time	5			
t_{WSCS}	Chip Select Set-up Time		0		
t_{WHCS}	Chip Select Hold Time		0		
t_{WHT}	AE Hold Time After $\overline{WE}$		40		
t_{WSDE}	Data In Set-up Time Before End of $\overline{WE}$	45			
t_{WHD}	Data In Hold Time After $\overline{WE}$	30			
t_{WS}	Output Disable Time After $\overline{WE}$		35		
t_{WR}	Output Recovery Time After $\overline{WE}$		40		
C_{IN}	Input Pin Capacitance		3.0		pF
C_{OUT}	Output Pin Capacitance		5.0		
USER TIMES					
t_{RC}	Row Column Address Change Time				
t_{MOD}	Data Modify Time				
t_{RFSH}	Refresh Period			2	ms

AC TEST LOAD AND WAVEFORMS

LOADING CONDITIONS



INPUT PULSES



AC CHARACTERISTICS OVER GUARANTEED OPERATING RANGES (Notes 5, 6)

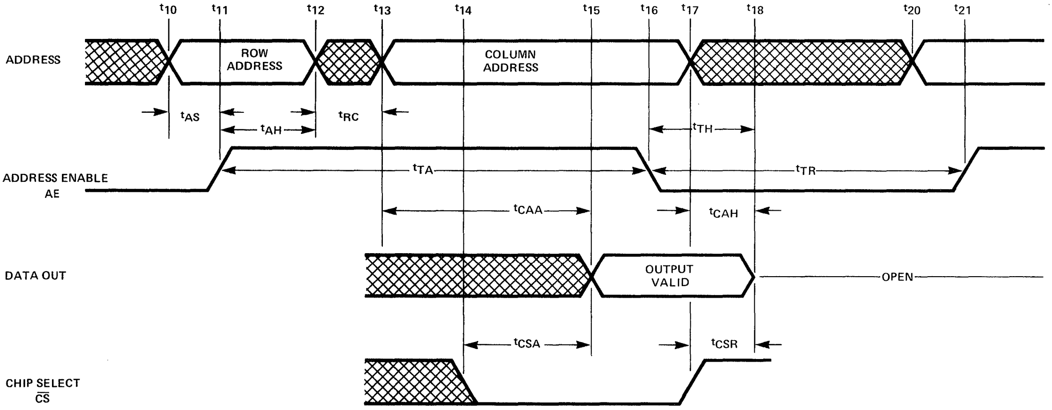
SYMBOL	CHARACTERISTICS	93481A			UNITS
		MIN	TYP	MAX	
MULTIPLEX					
t_{AS}	Row Address Set-up Time	0			ns
t_{AH}	Row Address Hold Time	35			
t_{TA}	AE Active Time	110			
t_{TR}	AE Recovery Time	130			
READ CYCLE					
t_{CAA}	Column Address Access Time			65	ns
t_{CAH}	Output Valid Time After Column Address		10		
t_{CSA}	Chip Select Access Time		35		
t_{CSR}	Chip Select Recovery Time		30		
t_{TH}	Output Valid Time After AE		15		
DATA LATCH					
t_{ALS}	Address Set-up Time Before LE	65			ns
t_{ALH}	Address Hold Time After LE		0		
t_{LH}	AE Hold Time After LE		–10		
t_{LR}	Output Recovery from LE		35		
t_{DLA}	Output Valid Time After LE		10		
WRITE CYCLE					
t_W	Write Pulse Width	25			ns
t_{WSA}	Address Set-up Time	35			
t_{WHA}	Address Hold Time	5			
t_{WSCS}	Chip Select Set-up Time		0		
t_{WHCS}	Chip Select Hold Time		0		
t_{WHT}	AE Hold Time After $\overline{WE}$		10		
t_{WSDE}	Data In Set-up Time Before End of $\overline{WE}$	35			
t_{WHD}	Data In Hold Time After $\overline{WE}$	30			
t_{WS}	Output Disable Time After $\overline{WE}$		35		
t_{WR}	Output Recovery Time After $\overline{WE}$		40		
C_{IN}	Input Pin Capacitance		3.0		pF
C_{OUT}	Output Pin Capacitance		5.0		
USER TIMES					
t_{RC}	Row Column Address Change Time				
t_{MOD}	Data Modify Time				
t_{RFSH}	Refresh Period			2	ms

READ-CYCLE – DATA NOT LATCHED

Addressing is accomplished by multiplexing the 5 bits of row address and 5 bits of the 7 bit column address on the same pins (A_0 through A_4, pins 1, 2, 3, 4 and 13). Assume the 5 bits of row address are stable at time t_{10} (the beginning of the cycle). At time t_{11} (t_{AS} after t_{10}) the address has been internally set up and the AE signal rise strobes the row address and latches it into the memory. The row address must be held stable until t_{12} (t_{AH} after the AE rise) to assure proper operation. At time t_{12}, the address input lines can change and the 7 bit column address can be switched on to the address input lines A_0 through A_6. The memory can tolerate an instantaneous change; however, the user circuitry will require some time (t_{RC}) to accomplish this change. Assuming this change is accomplished at t_{13}, the part now acts like a 128-bit static RAM. With the column address valid at t_{13} the output becomes valid at t_{15} with the data from the addressed cell. The time from t_{13} to t_{15} is t_{CAA} (column address access time). $\overline{CS}_1$ and $\overline{CS}_2$ must both be active low at t_{14} (t_{CSA} before t_{15}) for the output to be read at t_{15}. The chip selects can go low any time prior to t_{14}. The output will remain valid as long as the chip is selected, the column address is valid and AE remains high. The output will be in the high impedance state at time t_{CSR} after the chip select goes high. If the address is changed to a new column address with AE remaining high the same timing is applicable where the new address valid point corresponds to t_{13}.

If AE goes low at t_{16}, the output will remain valid until t_{18} (t_{TH} after t_{16}). The column address must be held valid until t_{17} (t_{CAH} prior to t_{18}) to guarantee the output is valid until t_{18}. AE goes low at t_{16} and is held low until t_{21} (at least t_{TR} after t_{16}). t_{21} corresponds to t_{11} in the first cycle.

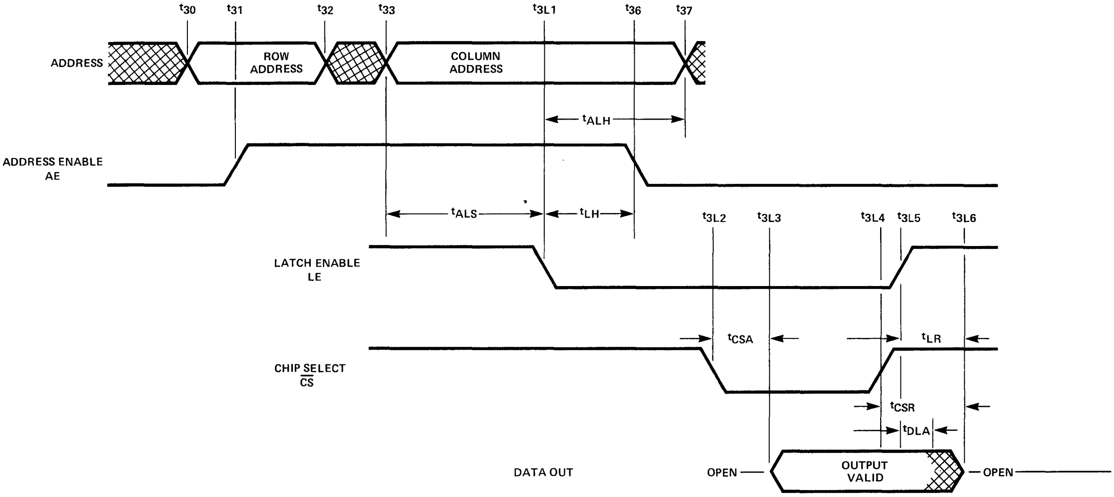
Full Cycle Address Access Time is $t_{AS} + t_{AH} + t_{CAA} + t_{RC}$.



DATA LATCH OPERATION

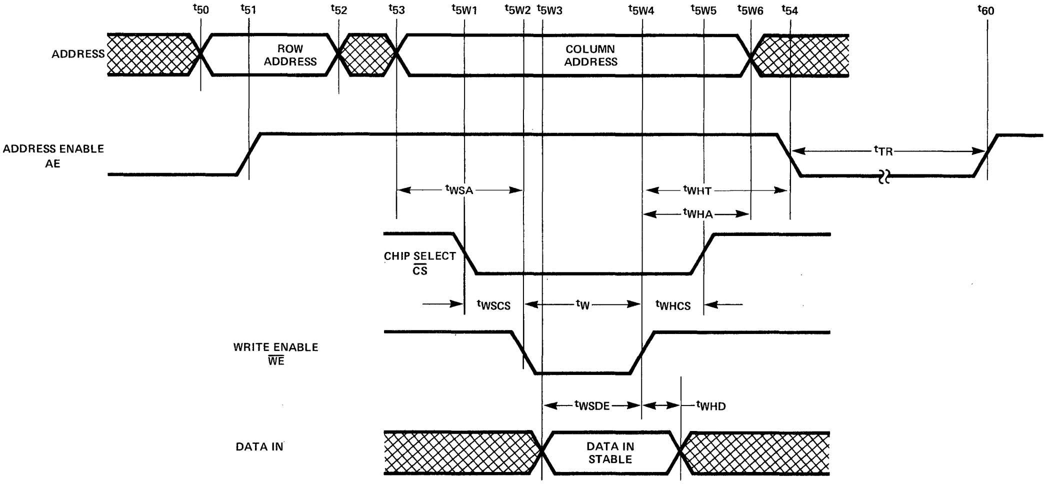
When a column address is valid (t_{33}) either after a row address, as illustrated, or after a previous column address, the Data Latch may be used to hold the data read from the addressed cell. LE may be activated low at t_{ALS} after t_{33} or later (t_{3L1}). The address may change no less than t_{ALH} after (t_{37}). The AE signal must be retained active high until t_{36} (defined by t_{3L1} + t_{LH}). t_{LH} is guaranteed negative meaning the AE signal may go low before LE goes low (i.e., t_{36} may be earlier than t_{3L1}). A useful mode of operation is for LE and AE to be tied together. The output is controlled by the state of the data latch circuit and the chip select signals which can be activated at any time. The output will appear on the output pin t_{CSA} after chip select signal goes low. If the chip select signal goes low earlier in the cycle, the output data will be read t_{CAA} after t_{33} as in the non-latched operation, but will remain valid until LE goes positive. If LE goes low while AE is low, an open is read at the output regardless of the state of $\overline{CS}_1$ and $\overline{CS}_2$.

When AE is low and Data has been latched the Data Output can be returned to the open state by either returning $\overline{CS}_1$, $\overline{CS}_2$ or LE to the high state. The output will be open at t_{3L6}, t_{CSR} after $\overline{CS}_1$ or $\overline{CS}_2$ is made high at t_{3L4} or t_{LR} after LE is made high at t_{3L5}. If AE is active high with data latched then $\overline{CS}_1$ or $\overline{CS}_2$ high will again cause the output to be open; or if LE alone is made high, the latched data will remain valid for time t_{DLA} on the output.



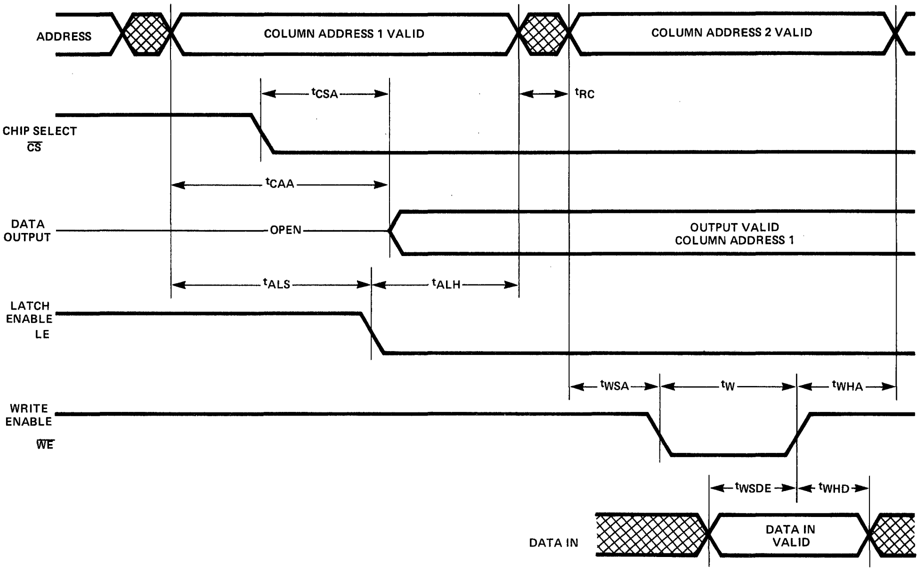
WRITE OPERATION

When a column address is valid (t_{53}) either after a row address as illustrated or after a previous column address, new data may be written into the addressed cell. The write signal may go low (t_{5W2}) t_{WSA} after the column address is valid (t_{53}). The write pulse must be at least t_W wide to assure writing. The $\overline{CS}_1$ and $\overline{CS}_2$ must both be low (t_{5W1}) at least t_{WSCS} before the fall of $\overline{WE}$ (t_{5W2}) and must remain low until at least t_{WHCS} after the rise of $\overline{WE}$ (t_{5W5}). AE must remain high until at least t_{WHT} after the rise of $\overline{WE}$ (t_{54}). The column address must remain valid until at least t_{WHA} after the rise of $\overline{WE}$ (t_{5W6}). Data In must be valid at least t_{WSDE} before the rise of $\overline{WE}$ and remain valid until at least t_{WHD} after the rise of $\overline{WE}$. Note that Data In timing is independent of the fall of $\overline{WE}$ (t_{5W2}).



EXAMPLE OF SUCCESSIVE COLUMN CYCLES

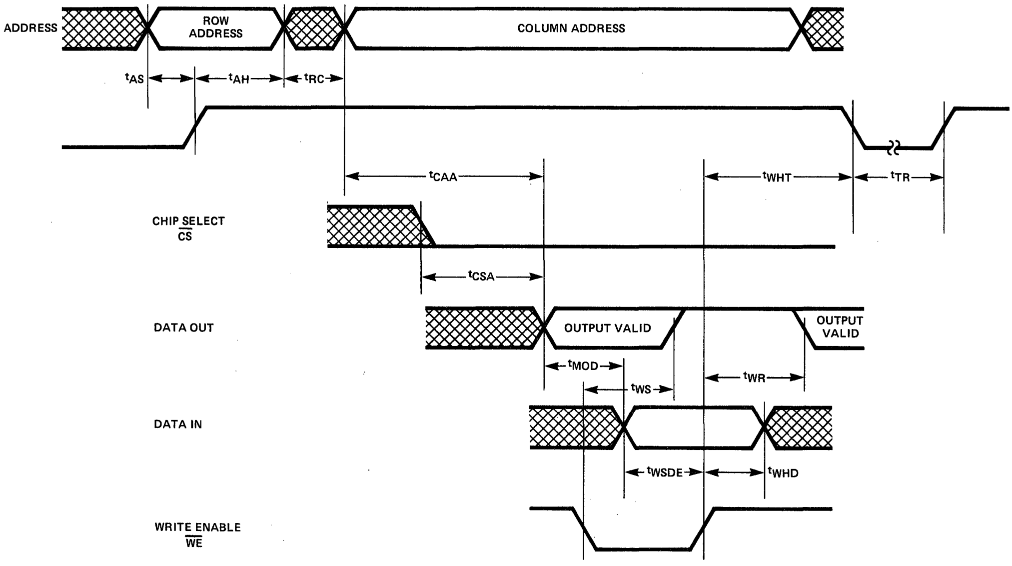
Successive operations at different column addresses on the same Row may be performed much more rapidly than a cycle requiring a new Row Address. This example illustrates a Read operation at Column Address 1 followed by a Write operation at Column Address 2. The Data Latch is used to hold the Output Data from Column Address 1 through the Write Cycle at Column Address 2. This kind of operation could be used to enter modified Data from Address 1 into the cell at Address 2.



READ-MODIFY-WRITE OPERATION

A Read-Modify-Write Cycle is performed by a normal Read followed by establishing D_{IN} and providing a $\overline{WE}$ signal. Since there are no special timing signals required for column operation this cycle is like a normal static Bipolar RAM. The Data Output from the read cycle remains valid until t_{WS} after the $\overline{WE}$ is brought low at which time it goes active high. If LE is high the output will again be valid t_{WR} after the $\overline{WE}$ is brought high. If LE is low the Data output will remain valid with the latched Data throughout the write portion of the cycle.

Read-Modify-Write cycle time is: $t_{AS} + t_{AH} + t_{RC} + t_{CAA} + t_{MOD} + t_{WSDE} + t_{WHT} + t_{TR}$



9403

FIRST-IN FIRST-OUT (FIFO) BUFFER MEMORY

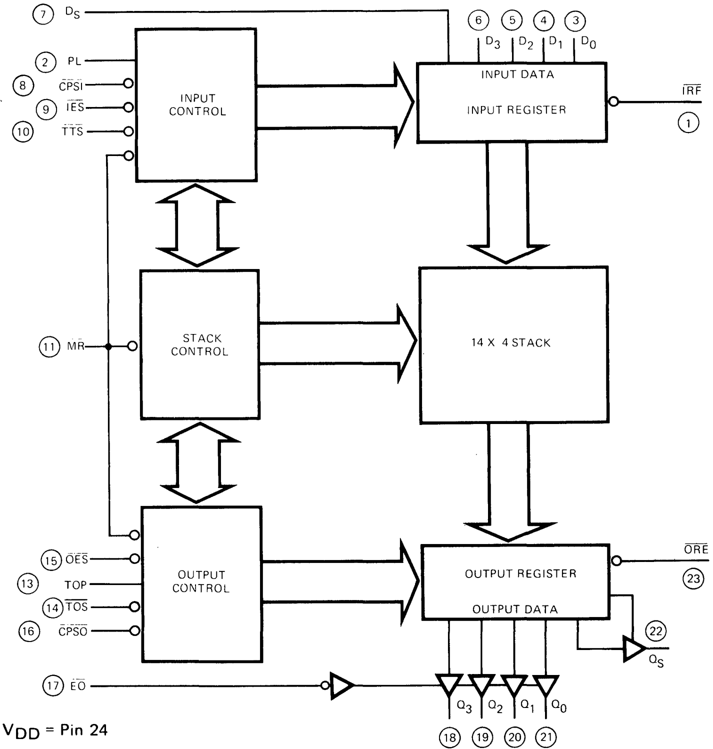
FAIRCHILD TTL MACROLOGIC

DESCRIPTION – The 9403 is an expandable fall-through type high-speed First-In First-Out (FIFO) Buffer Memory optimized for high speed disc or tape controllers and communication buffer applications. It is organized as 16 words by four bits and may be expanded to any number of words or any number of bits (in multiples of four). Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

The 9403 has 3-state outputs which provide added versatility and is fully compatible with all TTL families.

- **10 MHz SERIAL OR PARALLEL DATA RATE**
- **SERIAL OR PARALLEL INPUT**
- **SERIAL OR PARALLEL OUTPUT**
- **EXPANDABLE WITHOUT EXTERNAL LOGIC**
- **3-STATE OUTPUTS**
- **FULLY COMPATIBLE WITH ALL TTL FAMILIES**
- **SLIM 24-PIN PACKAGE**

BLOCK DIAGRAM

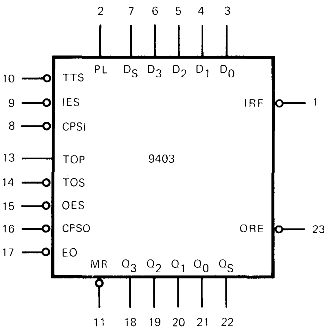


V_{DD} = Pin 24

V_{SS} = Pin 12

○ = Pin Numbers

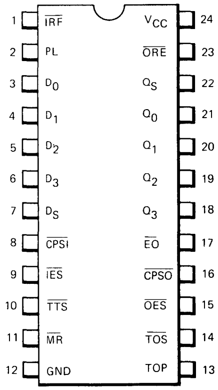
LOGIC SYMBOL



V_{CC} = Pin 24

GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

PIN NAME	DESCRIPTION	LOADING (Note a) HIGH	LOADING (Note a) LOW	COMMENTS
$D_0 - D_3$	Parallel Data Inputs	1.0 U.L.	0.23 U.L.	
D_S	Serial Data Input	1.0 U.L.	0.23 U.L.	
PL	Parallel Load Input	1.0 U.L.	0.23 U.L.	HIGH on PL enables $D_0 - D_3$. Not edge triggered. Ones catching.
$\overline{CPSI}$	Serial Input Clock	1.0 U.L.	0.23 U.L.	Edge triggered. Activates on falling edge.
$\overline{IES}$	Serial Input Enable	1.0 U.L.	0.23 U.L.	Enables serial and parallel input when LOW.
$\overline{TTS}$	Transfer to Stack Input	1.0 U.L.	0.23 U.L.	A LOW on this pin initiates fall through.
$\overline{OES}$	Serial Output Enable Input	1.0 U.L.	0.6 U.L.	Enables serial and parallel output when LOW.
$\overline{TOS}$	Transfer Out Serial Input	1.0 U.L.	0.23 U.L.	A LOW on this pin enables a word to be transferred from the stack to the output register. (TOP must be HIGH also for the transfer to occur). Not edge triggered.
TOP	Transfer Out Parallel Input	1.0 U.L.	0.23 U.L.	A HIGH on this pin enables a word to be transferred from the stack to the output register. ($\overline{TOS}$ must be LOW for the transfer to occur). Not edge triggered.
$\overline{MR}$	Master Reset	1.0 U.L.	0.23 U.L.	Active LOW.
$\overline{EO}$	Output Enable	1.0 U.L.	0.23 U.L.	Active LOW.
$\overline{CPSO}$	Serial Output Clock Input	1.0 U.L.	0.23 U.L.	Edge triggered. Activates on falling edge.
$Q_0 - Q_3$	Parallel Data Outputs	130 U.L.	10 U.L.	(Note b)
Q_S	Serial Data Output	10 U.L.	10 U.L.	(Note b)
$\overline{IRF}$	Input Register Full Output	10 U.L.	5 U.L.	LOW when input register is full (Note b).
$\overline{ORE}$	Output Register Empty Output	10 U.L.	5 U.L.	HIGH when output register contains valid data.

NOTE: a. 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW.
b. Output fan-out with $V_{OL} \leq 0.5$ V.

FUNCTIONAL DESCRIPTION – As shown in the block diagram the 9403 consists of three sections:

1. An Input Register with parallel and serial data inputs as well as control inputs and outputs for input handshaking and expansion.
2. A 4-bit wide, 14-word deep fall-through stack with self-contained control logic.
3. An Output Register with parallel and serial data outputs as well as control inputs and outputs for output handshaking and expansion.

Since these three sections operate asynchronously and almost independently, they will be described separately below:

Input Register (Data Entry):
The Input Register can receive data in either bit-serial or in 4-bit parallel form. It stores this data until it is sent to the fall-through stack and generates the necessary status and control signals.
Figure 1 is a conceptual logic diagram of the input section. As described later, this 5-bit register is initialized by setting the F3 flip-flop and resetting the other flip-flops. The Q-output of the last flip-flop (FC) is brought out as the "Input Register Full" output ($\overline{IRF}$). After initialization this output is HIGH.

Parallel Entry – A HIGH on the PL input loads the $D_0 - D_3$ inputs into the $F_0 - F_3$ flip-flops and sets the FC flip-flop. This forces the $\overline{IRF}$ output LOW indicating that the input register is full. During parallel entry, the $\overline{CPSI}$ input must be LOW.

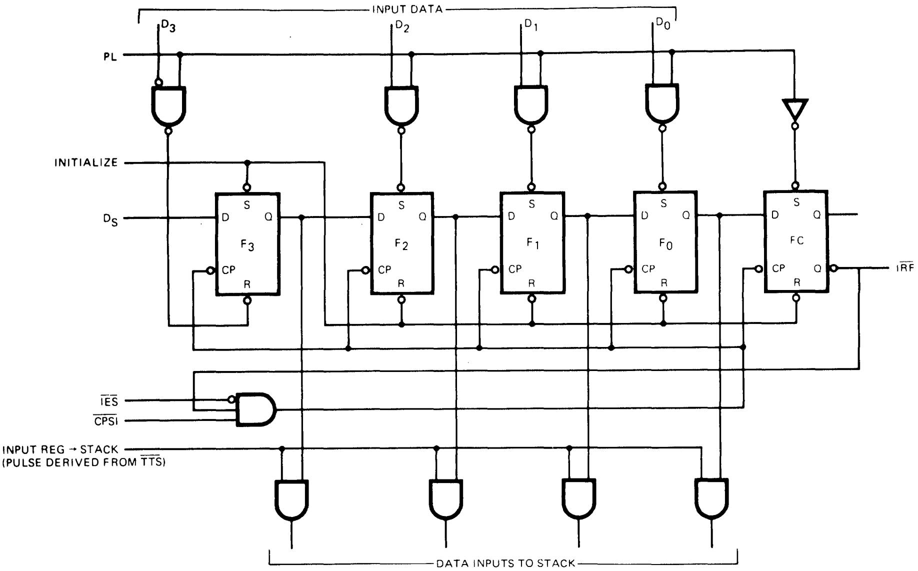


Fig. 1
CONCEPTUAL INPUT SECTION

Serial Entry – Data on the D_S input is serially entered into the F_3, F_2, F_1, F_0, FC shift register on each HIGH-to-LOW transition of the CPSI clock input, provided IES is LOW. During serial entry PL input should be LOW.

After the fourth clock transition, the four data bits located in the four flip-flops F_0 - F_3. The FC flip-flop is set, forcing the $\overline{IRF}$ output LOW and internally inhibiting $\overline{CPSI}$ clock pulses from effecting the register. ***Figure 2*** illustrates the final positions in a 9403 resulting from a 64-bit serial bit train. B_0 is the first bit, B_{63} the last bit.

Transfer to the Stack -The outputs of Flip-Flops F_0 - F_3 feed the stack. A LOW level on the $\overline{TTS}$ input initiates a "fall-through" action. If the top location of the stack is empty, data is loaded into the stack and the input register is re-initialized. Note that this initialization is postponed until PL is LOW again. Thus, automatic FIFO action is achieved by connecting the $\overline{IRF}$ output to the $\overline{TTS}$ input.

An RS Flip-Flop (the Request Initialization Flip-Flop shown in ***Figure 10***) in the control section records the fact that data has been transferred to the stack. This prevents multiple entry of the same word into the stack despite the fact the $\overline{IRF}$ and $\overline{TTS}$ may still be LOW. The Request Initialization Flip-Flop is not cleared until PL goes LOW. Once in the stack, data falls through the stack automatically, pausing only when it is necessary to wait for an empty next location. In the 9403, as in most modern FIFO designs, the $\overline{MR}$ input only initializes the stack control section and does not clear the data.

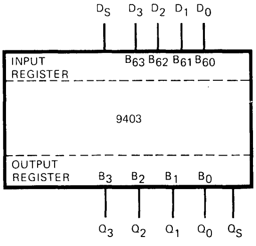


Fig. 2
FINAL POSITIONS IN A 9403 RESULTING FROM A 64-BIT SERIAL TRAIN

Output Register (Data Extraction) – The Output Register receives 4-bit data words from the bottom stack location, stores it and outputs data on a 3-state 4-bit parallel data bus or on a 3-state serial data bus. The output section generates and receives the necessary status and control signals. *Figure 3* is a conceptual logic diagram of the output section.

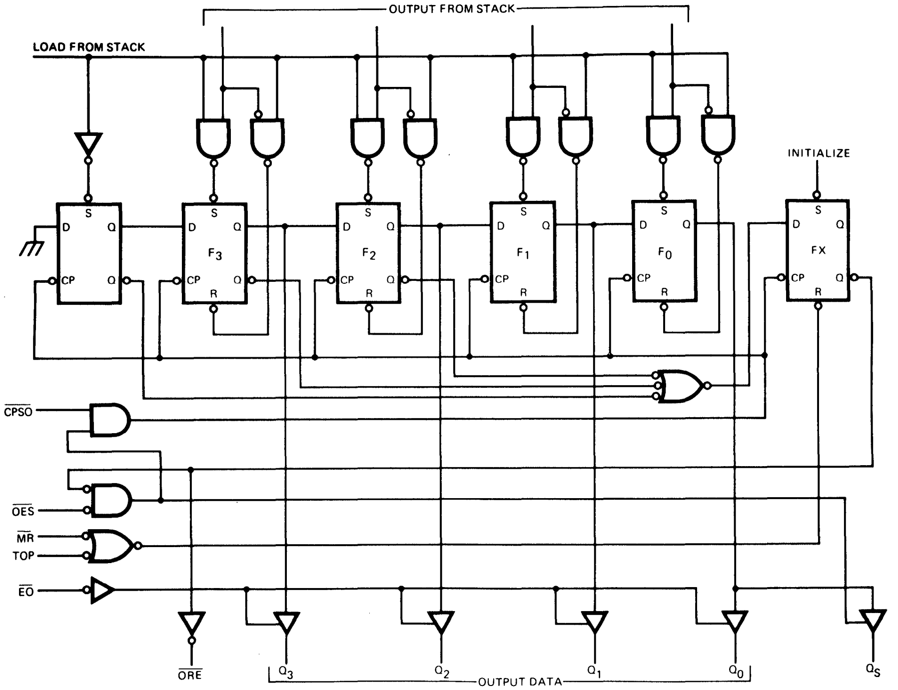


Fig. 3
CONCEPTUAL OUTPUT SECTION

Parallel Data Extraction – When the FIFO is empty after a LOW pulse is applied to $\overline{\text{MR}}$, the Output Register Empty ($\overline{\text{ORE}}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided the "Transfer Out Parallel" (TOP) input is HIGH. As a result of the data transfer $\overline{\text{ORE}}$ goes HIGH, indicating valid data on the data outputs (provided the 3-state buffer is enabled). TOP can now be used to clock out the next word. When TOP goes LOW, $\overline{\text{ORE}}$ will go LOW indicating that the output data has been extracted, but the data itself remains on the output bus until a HIGH level at TOP permits the transfer of the next word (if available into the Output Register. During parallel data extraction CPSO should be LOW. TOS should be grounded for single slice operation or connected to the appropriate ORE for expanded operation (see Expansion section).

TOP is not edge triggered. Therefore, if TOP goes HIGH before data is available from the stack, but data does become available before TOP goes LOW again, that data will be transferred into the Output Register. However, internal control circuitry prevents the same data from being transferred twice. If TOP goes HIGH and returns to LOW before data is available from the stack, $\overline{\text{ORE}}$ remains LOW indicating that there is no valid data at the outputs.

Serial Data Extraction – When the FIFO is empty after a LOW pulse is applied to $\overline{\text{MR}}$, the Output Register Empty ($\overline{\text{ORE}}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided $\overline{\text{TOS}}$ is LOW and TOP is HIGH. As a result of the data transfer $\overline{\text{ORE}}$ goes HIGH indicating valid data in the register. The 3-state Serial Data Output, Q_S, is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the HIGH-to-LOW transition of $\overline{\text{CPSO}}$. To prevent false shifting, $\overline{\text{CPSO}}$ should be LOW when the new word is being loaded into the Output Register. The fourth transition empties the shift register, forces $\overline{\text{ORE}}$ output LOW and disables the serial output, Q_S (refer to *Figure 3*). For serial operation the $\overline{\text{ORE}}$ output may be tied to the $\overline{\text{TOS}}$ input, requesting a new word from the stack as soon as the previous one has been shifted out.

EXPANSION -

Vertical Expansion - The 9403 may be vertically expanded to store more words without external parts. The interconnections necessary to form a 46-word by 4-bit FIFO are shown in *Figure 4.* Using the same technique, any FIFO of (15n + 1) words by four bits can be constructed, where n is the number of devices. Note that expansion does not sacrifice any of the 9403's flexibility for serial/parallel input and output. For other expansion schemes, refer to the Macrologic/Bipolar Microprocessor Data Book.

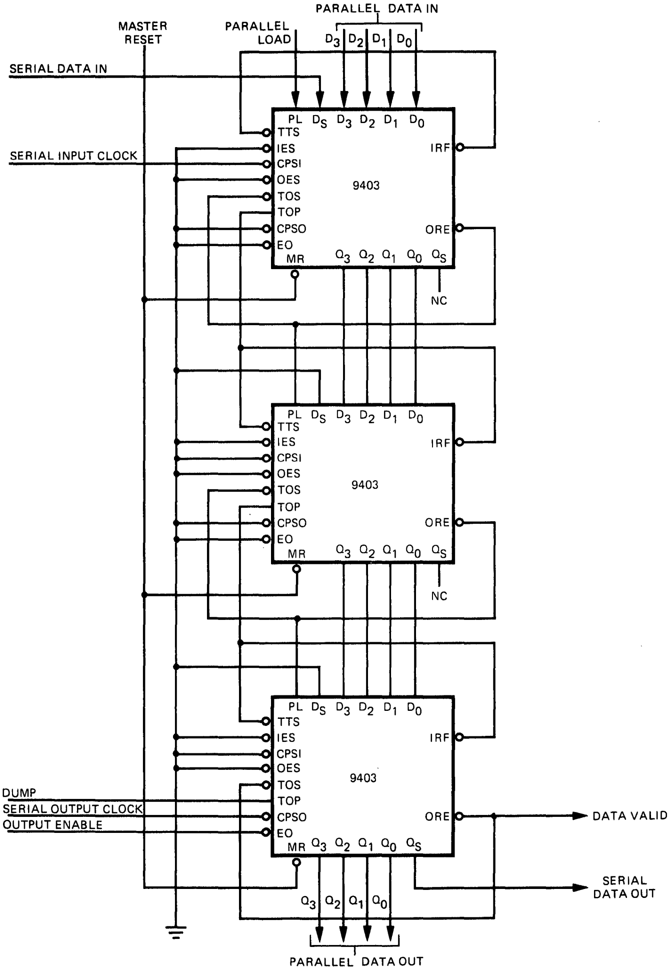


Fig. 4
A VERTICAL EXPANSION SCHEME

Horizontal Expansion – The 9403 can also be horizontally expanded to store long words (in multiples of four bits) without external logic. The interconnections necessary to form a 16-word by 12-bit FIFO are shown in *Figure 5.* Using the same technique, any FIFO of 16 words by 4n bits can be constructed, where n is the number of devices. The $\overline{IRF}$ output of the right most device (most significant device) is connected to the $\overline{TTS}$ inputs of all devices. Similarly, the $\overline{ORE}$ output of the most significant device is connected to the $\overline{TOS}$ inputs of all devices. As in the vertical expansion scheme, horizontal expansion does not sacrifice any of the 9403's flexibility for serial/parallel input and output.

It should be noted that this form of horizontal expansion extracts a penalty in speed. A single FIFO is guaranteed to operate at 10 MHz; an array of four FIFOs connected in the above manner is guaranteed at 4.3 MHz. An expansion scheme that provides higher speed but requires additional components is shown in the Applications section of the Macrologic/Bipolar Microprocessor Data Book.

Horizontal and Vertical Expansion – The 9403 can be expanded in both the horizontal and vertical directions without any external parts and without sacrificing any of its FIFO's flexibility for serial/parallel input and output. The interconnections necessary to form a 31-word by 16-bit FIFO are shown in *Figure 6.* Using the same technique, any FIFO of (15m + 1) words by (4n) bits can be constructed, where m is the number of devices in a column and n is the number of devices in a row.

Figures 7 and *8* show the timing diagrams for serial data entry and extraction for the 31-word by 16-bit FIFO shown in *Figure 6.* The final position of data after serial insertion of 496 bits into the FIFO array of *Figure 6* is shown in *Figure 9.*

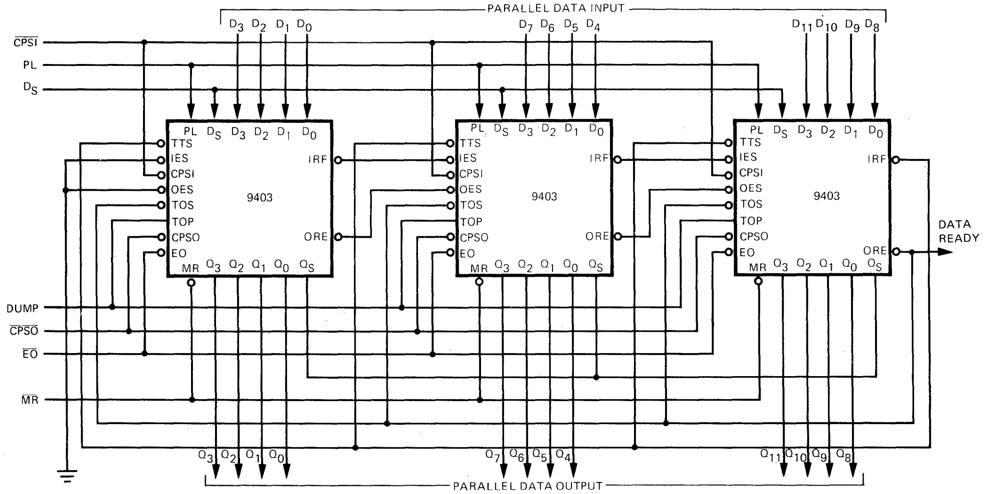


Fig. 5
A HORIZONTAL EXPANSION SCHEME

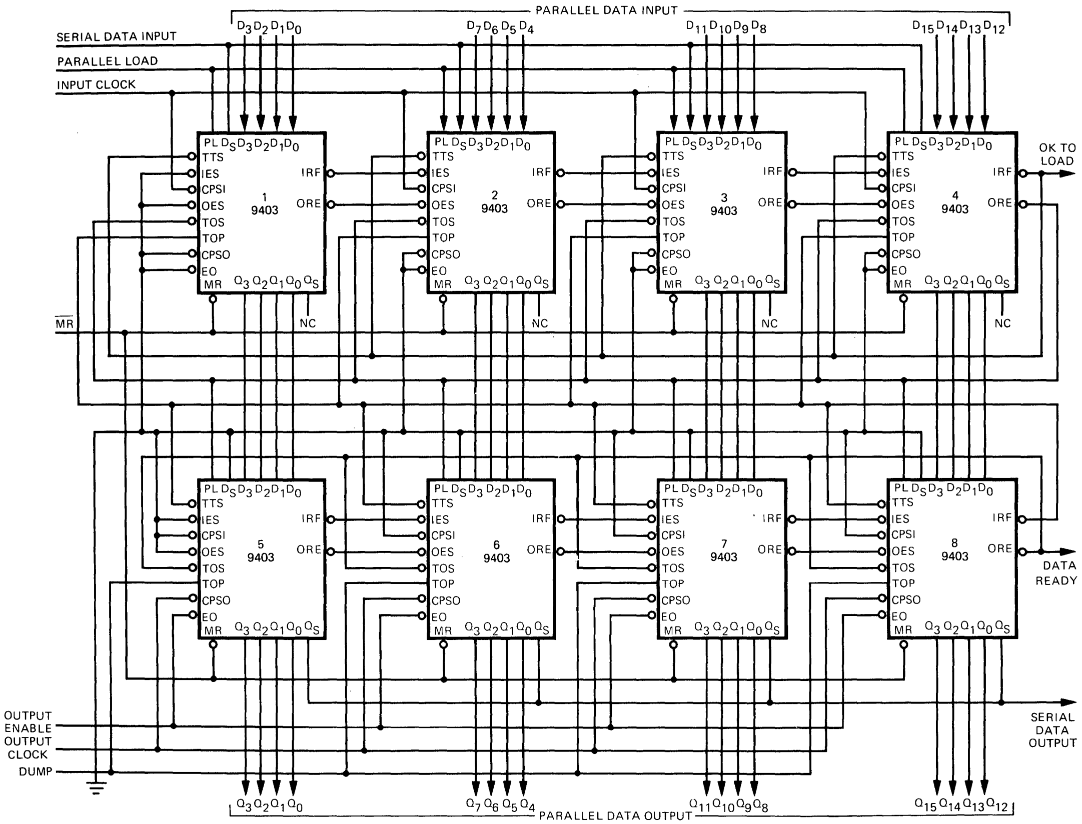


Fig. 6
A 31 X 16 FIFO ARRAY

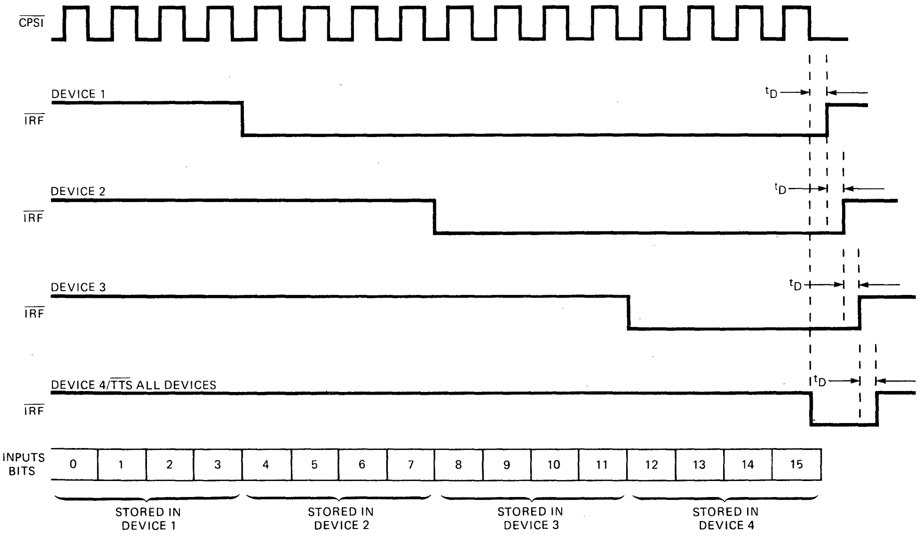


Fig. 7
SERIAL DATA ENTRY FOR ARRAY OF FIG. 6

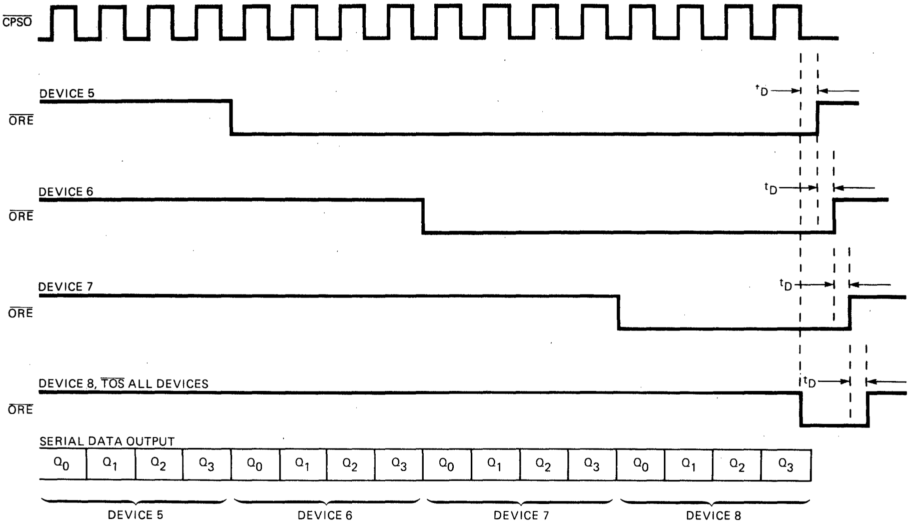


Fig. 8
SERIAL DATA EXTRACTION FOR ARRAY OF FIG. 6

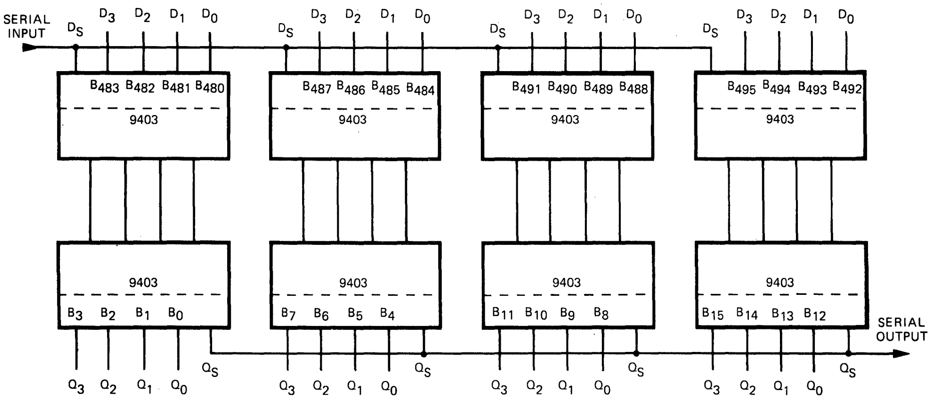


Fig. 9
FINAL POSITION OF A 496-BIT SERIAL INPUT

Interlocking Circuitry - Most conventional FIFO designs provide status signals analogous to $\overline{\text{IRF}}$ and $\overline{\text{ORE}}$. However, when these devices are operated in arrays, variations in unit to unit operating speed require external gating to assure all devices have completed an operation. The 9403 incorporates simple but effective "master/slave" interlocking circuitry to eliminate the need for external gating.

In the 9403 array of *Figure 6* devices 1 and 5 are defined as "row masters" and the other devices are slaves to the master in their row. No slave in a given row will initialize its Input Register until it has received LOW on its $\overline{\text{IES}}$ input from a row master or a slave of higher priority.

In a similar fashion, the $\overline{\text{ORE}}$ outputs of slaves will not go HIGH until their $\overline{\text{OES}}$ inputs have gone HIGH. This interlocking scheme ensures that new input data may be accepted by the array when the $\overline{\text{IRF}}$ output of the final slave in that row goes LOW and that output data for the array may be extracted when the $\overline{\text{ORE}}$ of the final slave in the output row goes HIGH.

The row master is established by connecting its $\overline{\text{IES}}$ input to ground while a slave receives its $\overline{\text{IES}}$ input from the $\overline{\text{IRF}}$ output of the next higher priority device. When an array of 9403 FIFOs is initialized with a LOW on the $\overline{\text{MR}}$ inputs of all devices, the $\overline{\text{IRF}}$ outputs of all devices will be HIGH. Thus, only the row master receives a LOW on the $\overline{\text{IES}}$ input during initialization. *Figure 10* is a conceptual logic diagram of the internal circuitry which determines master/slave operation. Whenever $\overline{\text{MR}}$ and $\overline{\text{IES}}$ are LOW, the Master Latch is set. Whenever $\overline{\text{TTS}}$ goes LOW the Request Initialization Flip-Flop will be set. If the Master Latch is HIGH, the Input Register will be immediately initialized and the Request Initialization Flip-Flop reset. If the Master Latch is reset, the Input Register is not initialized until $\overline{\text{IES}}$ goes LOW. In array operation, activating the $\overline{\text{TTS}}$ initiates a ripple input register initialization from the row master to the last slave.

A similar operation takes place for the output register. Either a $\overline{\text{TOS}}$ or TOP input initiates a load-from-stack operation and sets the ORE Request Flip-Flop. If the Master Latch is set, the last Output Register Flip-Flop is set and $\overline{\text{ORE}}$ goes HIGH. If the Master Latch is reset, the $\overline{\text{ORE}}$ output will be LOW until an $\overline{\text{OES}}$ input is received.

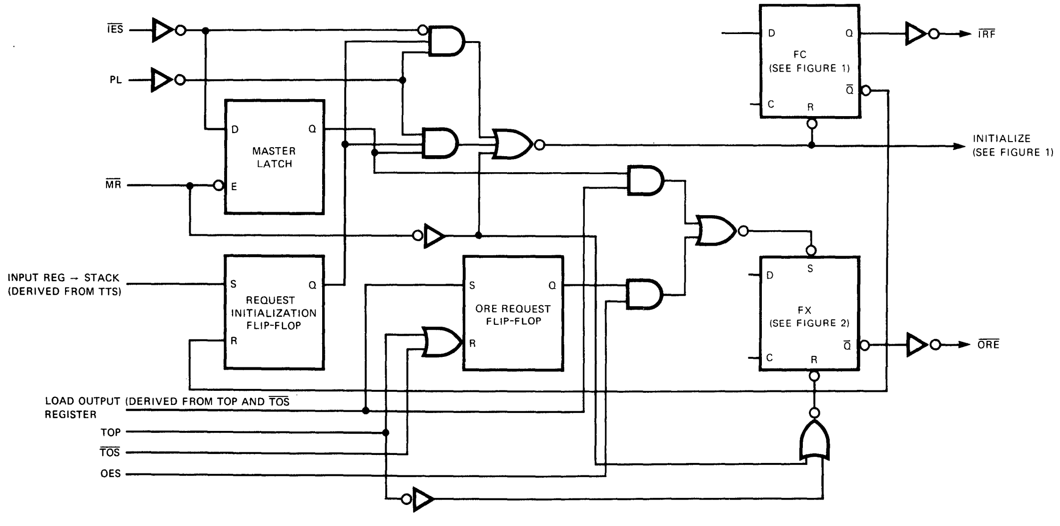


Fig. 10
CONCEPTUAL DIAGRAM, INTERLOCKING CIRCUITRY

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage, $\overline{\text{ORE}}$, $\overline{\text{IRF}}$	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 µA	
		XC	2.4	3.4				
V_{OH}	Output HIGH Voltage, Q_0–Q_3, Q_S	XM	2.4	3.4		V	I_{OH} = −2.0 mA	V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = −5.7 mA	
V_{OL}	Output LOW Voltage, Q_0–Q_3, Q_S	XM		0.25	0.4	V	I_{OL} = 8.0 mA	V_{CC} = MIN
		XC		0.35	0.5	V	I_{OL} = 16 mA	
V_{OL}	Output LOW Voltage, $\overline{\text{ORE}}$, $\overline{\text{IRF}}$	XM		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN
		XC		0.35	0.5		I_{OL} = 8.0 mA	
I_{OZH}	Output Off HIGH Current Q_0–Q_3, Q_S				100	µA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2.0 V	
I_{OZL}	Output Off LOW Current Q_0–Q_3, Q_S				−100	µA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 2.0 V	
I_{IH}	Input HIGH Current			1.0	40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current, all except $\overline{\text{OES}}$				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
	Input LOW Current, $\overline{\text{OES}}$				−0.96			
I_{OS}	Output Short Circuit Current Q_0–Q_3, Q_S, $\overline{\text{ORE}}$, $\overline{\text{OES}}$		−30		−130	mA	V_{CC} = MAX, V_{OUT} = 0, (Note 3)	
I_{CC}	Supply Current	XM		115	155	mA	V_{CC} = MAX, Inputs Open	
		XC		115	170			

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: V_{CC} = 5.0 V, C_L = 15 pF, T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{PHL}	Propagation Delay, Negative-Going CP to $\overline{\text{IRF}}$ Output		18	25	ns	Stack not Full, PL LOW, Figures 11 and 12
t_{PLH}	Propagation Delay, Negative-Going $\overline{\text{TTS}}$ to $\overline{\text{IRF}}$		48	64	ns	
t_{PLH},	Propagation Delay, Negative-Going $\overline{\text{CPSO}}$ to Q_S Output		30	40	ns	$\overline{\text{OES}}$ LOW, TOP HIGH, Figures 13 and 14
t_{PHL}			17	23	ns	
t_{PLH},	Propagation Delay, Positive-Going TOP to Outputs Q_0 – Q_3		40	56	ns	$\overline{\text{EO}}$, $\overline{\text{CPSO}}$ LOW, Figure 15
t_{PHL}			31	45	ns	
t_{PHL}	Propagation Delay, Negative-Going $\overline{\text{CPSO}}$ to $\overline{\text{ORE}}$		32	42	ns	$\overline{\text{OES}}$ LOW, TOP HIGH, Figures 13 and 14
t_{PHL}	Propagation Delay, Negative-Going TOP to $\overline{\text{ORE}}$		40	54	ns	Parallel Output, $\overline{\text{EO}}$, $\overline{\text{CPSO}}$ LOW, Figure 15
t_{PLH}	Propagation Delay, Positive-Going TOP to $\overline{\text{ORE}}$		51	68		
t_{DFT}	Fall Through Time		450	600	ns	$\overline{\text{TTS}}$ Connected to $\overline{\text{IRF}}$ $\overline{\text{TOS}}$ Connected to $\overline{\text{ORE}}$ $\overline{\text{IES}}$, $\overline{\text{OES}}$, $\overline{\text{EO}}$, $\overline{\text{CPSO}}$ LOW, TOP HIGH, Figure 16
t_{PLH}	Propagation Delay, Negative-Going $\overline{\text{TOS}}$ to Positive-Going $\overline{\text{ORE}}$		41	53	ns	Data in stack, TOP HIGH, Figures 13 and 14

AC CHARACTERISTICS (Cont'd): $V_{CC} = 5.0$ V, $C_L = 15$ pF, $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{PHL}	Propagation Delay, Positive-Going PL to Negative-Going $\overline{\mathrm{IRF}}$		33	44	ns	Stack not Full, Figures 17 and 18
t_{PLH}	Propagation Delay, Negative-Going PL to Positive-Going $\overline{\mathrm{IRF}}$		20	28	ns	
t_{PLH}	Propagation Delay, Positive-Going $\overline{\mathrm{OES}}$ to $\overline{\mathrm{ORE}}$		26	38	ns	
t_{PLH}	Propagation Delay, Positive-Going $\overline{\mathrm{IES}}$ to Positive-Going $\overline{\mathrm{IRF}}$		31	40	ns	Figure 18
t_{PZL}, t_{PZH}	Propagation Delay, $\overline{\mathrm{OE}}$ to Q_0, Q_1, Q_2, Q_3		9.0	14	ns	Propagation Delay Out of the High Impedance State
t_{PHZ}, t_{PLZ}	Propagation Delay, $\overline{\mathrm{OE}}$ to Q_0, Q_1, Q_2, Q_3		7.0	14	ns	Propagation Delay Into the High Impedance State
t_{PZL}, t_{PZH}	Propagation Delay, Negative-Going $\overline{\mathrm{OES}}$ to Q_S		13	18	ns	Propagation Delay Out of the High Impedance State
t_{PLZ}, t_{PHZ}	Propagation Delay, Negative-Going $\overline{\mathrm{OES}}$ to Q_S		7.0	14	ns	Propagation Delay Into the High Impedance State
t_{AP}	Parallel Appearance Time, $\overline{\mathrm{ORE}}$ to $Q_0 - Q_3$		−12	−5.0	ns	Time elapsed between $\overline{\mathrm{ORE}}$ going HIGH and valid data appearing at output. Negative number indicates data available before $\overline{\mathrm{ORE}}$ goes HIGH.
t_{AS}	Serial Appearance Time, $\overline{\mathrm{ORE}}$ to Q_S		6.0	10	ns	

AC SET-UP REQUIREMENTS: $V_{CC} = 5.0$ V, $C_L = 15$ pF, $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{PWH}	$\overline{\mathrm{CPSI}}$ Pulse Width (HIGH)	25	19		ns	Stack not full, PL LOW, Figures 11 and 12
t_{PWL}	$\overline{\mathrm{CPSI}}$ Pulse Width (LOW)	20	11		ns	
t_{PWH}	PL Pulse Width (HIGH)	40	29		ns	Stack not full, Figures 17 and 18
t_{PWL}	$\overline{\mathrm{TTS}}$ Pulse Width (LOW) Serial or Parallel Mode	20	9.0		ns	Stack not full, Figures 11, 12, 17, 18
t_{PWL}	$\overline{\mathrm{MR}}$ Pulse Width (LOW)	25	13		ns	Figure 16
t_{PWH}	TOP Pulse Width (High)	20	13		ns	$\overline{\mathrm{CPSO}}$ LOW, data available in stack, Figure 15
t_{PWL}	TOP Pulse Width (LOW)	30	17		ns	
t_{PWH}	$\overline{\mathrm{CPSO}}$ Pulse Width (HIGH)	32	18		ns	TOP HIGH, data in stack, Figures 13 and 14
t_{PWL}	$\overline{\mathrm{CPSO}}$ Pulse Width (LOW)	30	16		ns	
t_s	Set-up Time, D_S to Negative $\overline{\mathrm{CPSI}}$	28	17		ns	PL LOW, Figures 11 and 12
t_h	Hold Time, D_S to $\overline{\mathrm{CPSI}}$	0	−6.0		ns	PL LOW, Figures 11 and 12
t_s	Set-up Time, $\overline{\mathrm{TTS}}$ to $\overline{\mathrm{IRF}}$ Serial or Parallel Mode	0	−20		ns	Figures 11, 12, 17, 18
t_s	Set-up Time Negative-Going $\overline{\mathrm{ORE}}$ to Negative-Going $\overline{\mathrm{TOS}}$	0	−24		ns	TOP HIGH, Figures 13 and 14
t_{rec}	Recovery Time $\overline{\mathrm{MR}}$ to any Input	10	5.0		ns	Figure 16
t_s	Set-up Time, Negative-Going $\overline{\mathrm{IES}}$ to $\overline{\mathrm{CPSI}}$	32	23		ns	Figure 12
t_s	Set-up Time, Negative-Going $\overline{\mathrm{TTS}}$ to $\overline{\mathrm{CPSI}}$	76	58		ns	Figure 12
t_s	Set-up Time, Parallel Inputs to PL	0	−22		ns	Length of time parallel inputs must be applied prior to rising edge of PL.
t_h	Hold Time, Parallel Inputs to PL	0			ns	Length of time parallel inputs must reamin applied after falling edge of PL.

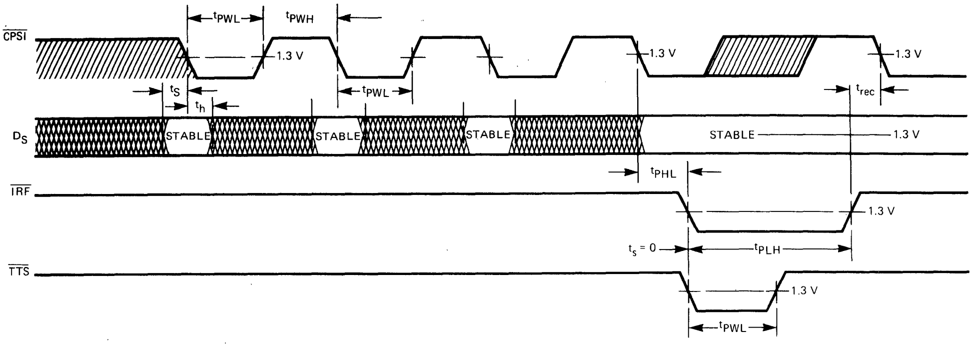


Fig. 11
SERIAL INPUT, UNEXPANDED OR MASTER OPERATION
Conditions: stack not full, $\overline{\text{IES}}$, PL LOW

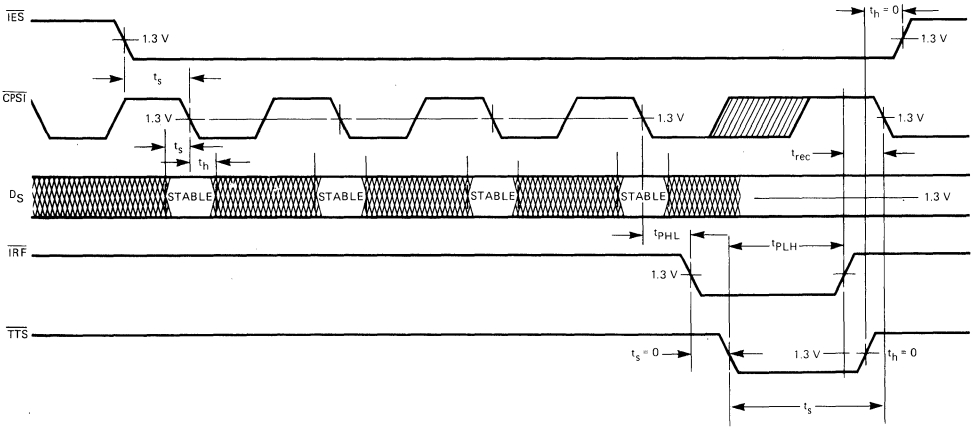


Fig. 12
SERIAL INPUT, EXPANDED SLAVE OPERATION
Conditions: stack not full, $\overline{\text{IES}}$ HIGH when initiated, PL LOW

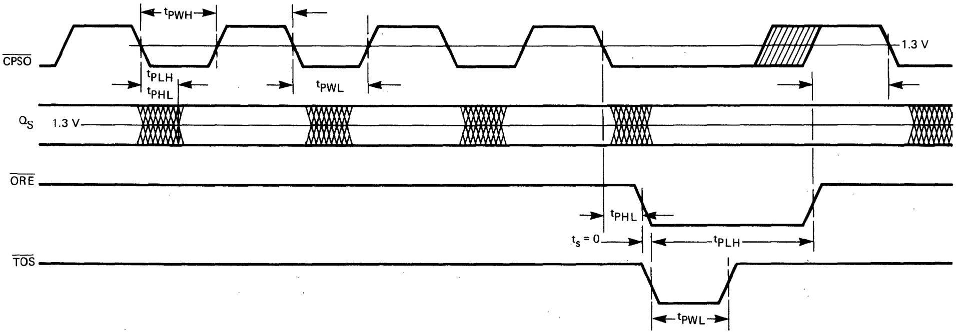


Fig. 13
SERIAL OUTPUT, UNEXPANDED OR MASTER OPERATION
Conditions: data in stack, TOP HIGH, $\overline{\text{IES}}$ LOW when initiated, $\overline{\text{OES}}$ LOW

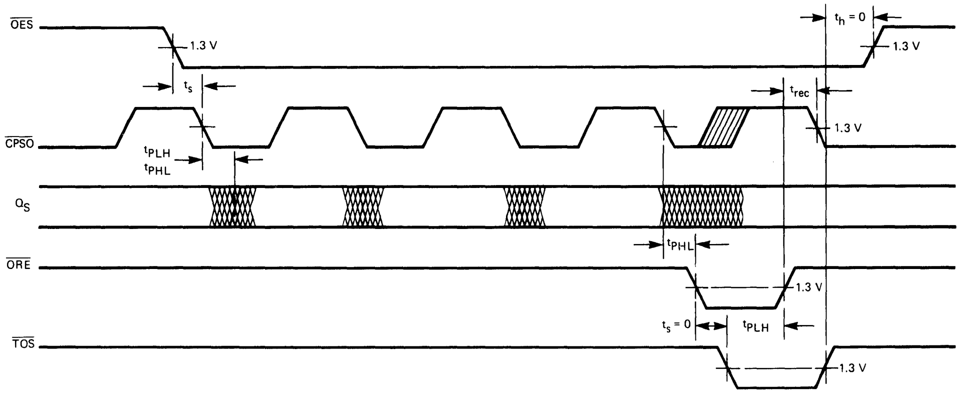


Fig. 14
SERIAL OUTPUT, SLAVE OPERATION
Conditions: data in stack, TOP HIGH, $\overline{\text{IES}}$ HIGH when initiated

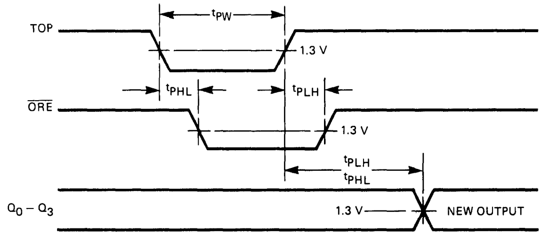


Fig. 15
PARALLEL OUTPUT, 4-BIT WORD OR MASTER IN PARALLEL EXPANSION
Conditions: $\overline{\text{IES}}$ LOW when initiated, $\overline{\text{EO}}$, $\overline{\text{CPSO}}$ LOW; data available in stack

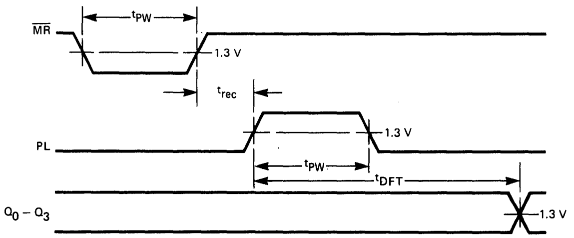


Fig. 16
FALL THROUGH TIME
Conditions: $\overline{\text{TTS}}$ connected to $\overline{\text{IRF}}$, $\overline{\text{TOS}}$ connected to $\overline{\text{ORE}}$, $\overline{\text{IES}}$, $\overline{\text{OES}}$, $\overline{\text{EO}}$, $\overline{\text{CPSO}}$ LOW, TOP HIGH

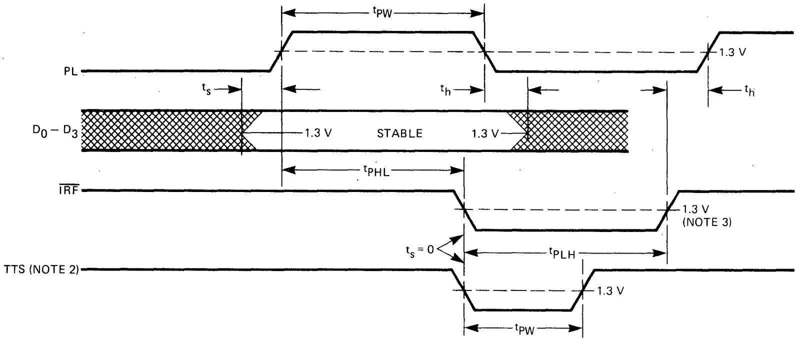


Fig. 17

PARALLEL LOAD MODE, 4-BIT WORD (UNEXPANDED) OR MASTER IN PARALLEL EXPANSION

Conditions: stack not full, $\overline{IES}$ LOW when initialized

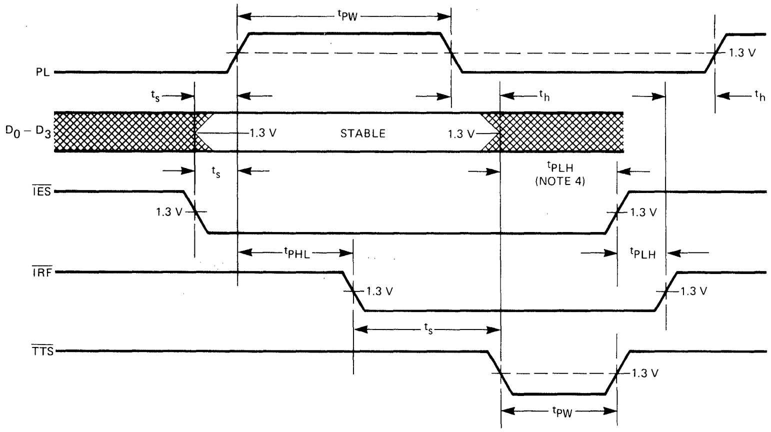


Fig. 18

PARALLEL LOAD, SLAVE MODE

Conditions: stack not full, device initialized (Note 1) with $\overline{IES}$ HIGH

NOTES:
1. Initialization requires a master reset to occur after power has been applied.
2. $\overline{TTS}$ normally connected to $\overline{IRF}$.
3. If stack is full, IRF will stay LOW.

9406

PROGRAM STACK

FAIRCHILD TTL MACROLOGIC

DESCRIPTION – The 9406 is a 16-word by 4-bit "push-down pop-up" Program Stack. It is designed to implement Program Counter (PC) and return address storage for nested subroutines in programmable digital systems. The 9406 executes 4 instructions: Return, Branch, Call and Fetch as specified by a 2-bit instruction. When the device is initialized, PC is in the top location of the stack. As a new PC value is "pushed" into the stack (Call operation), all previous PC values effectively move down one level. The top location of the stack is the current PC. Up to 16 new Program Counter values can be stored, which gives the 9406 a 15 level nesting capability. "Popping" the stack (Return operation) brings the most recent PC to the top of the stack. The remaining two instructions affect only the top location of the stack. In the Branch operation a new PC value is loaded into the top location of the stack from the $\overline{D}_0 - \overline{D}_3$ Inputs. In the Fetch operation, the contents of the top stack location (current PC value) are put on the $X_0 - X_3$ bus and the current PC value is incremented.

The 9406 may be expanded to any word length without additional logic. 3-state output drivers are provided on the 4-bit address outputs ($X_0 - X_3$) and data outputs ($\overline{O}_0 - \overline{O}_3$); the X-Bus outputs are enabled internally during the Fetch instruction while the O-Bus outputs are controlled by an Output Enable ($\overline{EO}_0$). Two status outputs, Stack Full ($\overline{SF}$) and Stack Empty ($\overline{SE}$) are provided. The 9406 is fully compatible with all TTL families.

- **16-WORD BY 4-BIT LIFO**
- **15-LEVEL NESTING CAPABILITY**
- **10 MHz MICROINSTRUCTION RATE**
- **PROGRAM COUNTER LOADS FROM DATA BUS**
- **OPTIONAL AUTOMATIC INCREMENT OF PROGRAM COUNTER**
- **STACK LIMIT STATUS INDICATORS**
- **SLIM 24-PIN PACKAGE**
- **3-STATE OUTPUTS**

PIN NAMES

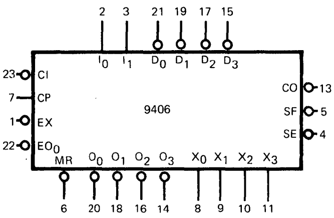
		LOADING (Note a)	
		HIGH	LOW
$\overline{D}_0 - \overline{D}_3$	Data Inputs (Active LOW)	1.0 U.L.	0.23 U.L.
I_0, I_1	Instruction Inputs	1.0 U.L.	0.23 U.L.
$\overline{EX}$	Execute Input (Active LOW)	1.0 U.L.	0.23 U.L.
CP	Clock Input	1.0 U.L.	0.23 U.L.
$\overline{MR}$	Master Reset Input (Active LOW)	1.0 U.L.	0.23 U.L.
$\overline{CI}$	Carry Input (Active LOW)	1.0 U.L.	0.23 U.L.
$\overline{EO}_0$	Output Enable Input (Active LOW)	1.0 U.L.	0.23 U.L.
$\overline{O}_0 - \overline{O}_3$	Output Data Outputs (Active LOW) (Note b)	130 U.L.	10 U.L.
$X_0 - X_3$	Address Outputs (Note b)	130 U.L.	10 U.L.
$\overline{CO}$	Carry Output (Active LOW) (Note b)	10 U.L.	5 U.L.
$\overline{SF}$	Stack Full Output (Active LOW) (Note b)	10 U.L.	5 U.L.
$\overline{SE}$	Stack Empty Output (Active LOW) (Note b)	10 U.L.	5 U.L.

NOTES:

a. 1 unit load (U.L.) = 40 μA HIGH, 1.6 mA LOW.

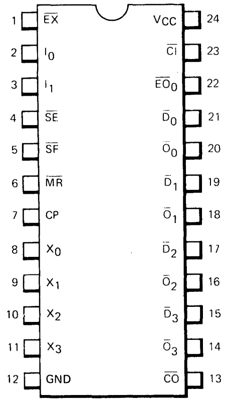
b. Output fan-out with $V_{OL} \leq 0.5$ V.

LOGIC SYMBOL



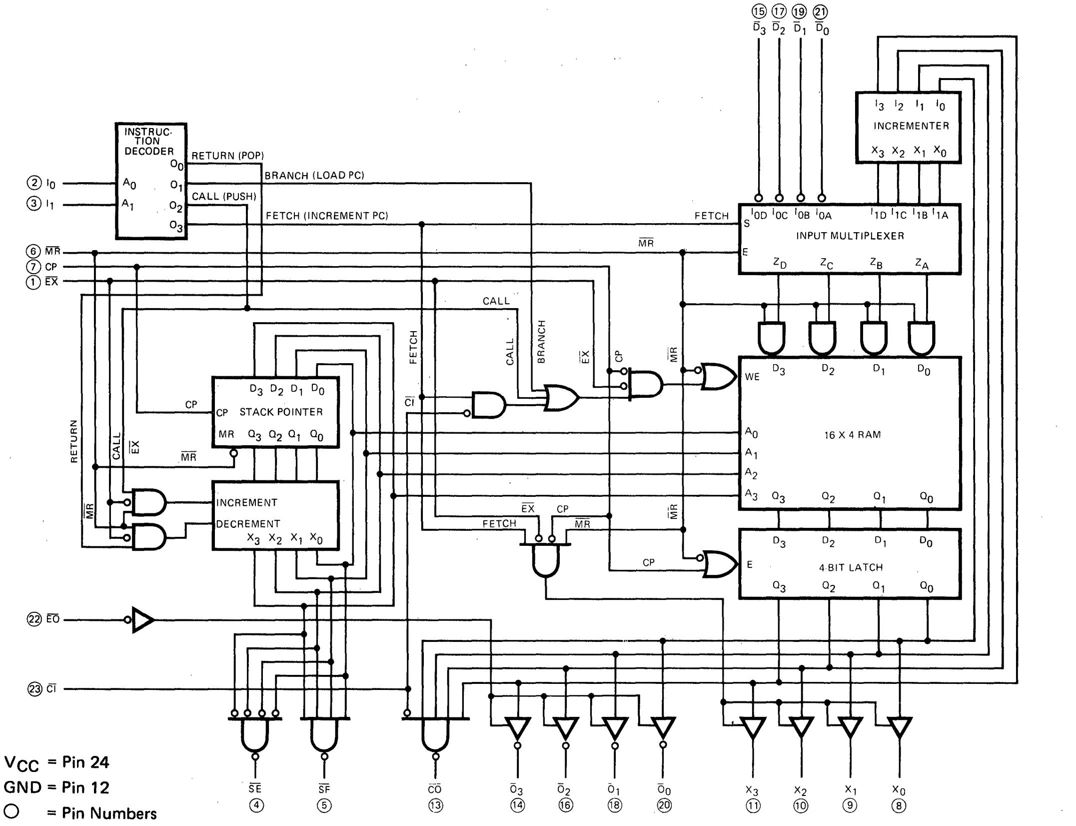
V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

BLOCK DIAGRAM



V_{CC} = Pin 24
GND = Pin 12
○ = Pin Numbers

TABLE 1
INSTRUCTION SET FOR THE 9406

I_1 I_0	INSTRUCTION	INTERNAL OPERATION	X-BUS	O-BUS (WITH EO_0 LOW)
L L	Return (Pop)	Decrement Stack Pointer	Disabled	Depending on the relative timing of $\overline{EX}$ and CP, the outputs will reflect the current program counter or the new value while CP is LOW. When CP goes HIGH again, the output will reflect the new value.
L H	Branch (Load PC)	Load D-Bus into Current Program Counter Location	Disabled	Current Program Counter until CP goes HIGH again, then updated with newly entered PC value.
H L	Call (Push)	Increment Stack Pointer and Load D-Bus into New Program Counter Location	Disabled	Depending on the relative timing of $\overline{EX}$ and CP, the outputs will reflect the current program counter or the previous contents of the incremented SP location. When CP goes HIGH again, the outputs will reflect the newly entered PC value. See Figure 9 for details.
H H	Fetch (Increment PC)	Increment Current Program Counter if $\overline{CI}$ is LOW	Current Program Counter while both CP and $\overline{EX}$ are LOW, disabled while CP or $\overline{EX}$ is HIGH	Current Program Counter until CP goes HIGH again, then updated with incremented PC value.

H = HIGH Level L = LOW Level

FUNCTIONAL DESCRIPTION – As shown in the block diagram, the 9406 consists of an Input Multiplexer, a 16 X 4 RAM with output latches addressed by the Stack Pointer (SP), an incrementor, control logic, and output buffers. The 9406 is organized around three 4-bit busses; the input data bus $(\overline{D}_0 - \overline{D}_3)$, output data bus $(\overline{O}_0 - \overline{O}_3)$ and the address bus $(X_0 - X_3)$. The 9406 implements four instructions as determined by Inputs I_0 and I_1 (see *Table 1*). The O-Bus is derived from the RAM output latches and enabled by a LOW on the Output Enable $(\overline{EO}_0)$ input. The X-Bus is also derived from the output latches; it is enabled internally during the Fetch instruction. Execution of instructions is controlled by the Execute $(\overline{EX})$ and Clock (CP) inputs.

Fetch Operation - The Fetch operation places the content of the current Program Counter (PC) on the X-Bus. If the Carry In (CI) is LOW, the current PC is incremented in preparation for the next Fetch. If CI is HIGH, the value of the current PC is unchanged, (Iterative Fetch).

The instruction code is set up on the I lines when CP is HIGH. The Execute $(\overline{EX})$ is normally LOW at this time. The control logic interprets I_0 and I_1 and selects the incrementor output as the data source to the RAM via the Input Multiplexer. The current PC value is loaded into the latches and is available on the O-Bus if $\overline{EO}_0$ is LOW. When CP is LOW the latches are disabled from following the RAM output, when both CP and $\overline{EX}$ are LOW, buffers are enabled, applying the current PC to the X-Bus. The output of the incrementor is written into the RAM during the period when CP and $\overline{EX}$ are LOW. If $\overline{CI}$ is LOW, the value stored in the current PC, plus one, is written into the RAM. If $\overline{CI}$ is HIGH, the current PC is not incremented. Carry Out $(\overline{CO})$ is LOW when the content of the current PC is at its maximum, i.e., all ones and the Carry In $(\overline{CI})$ is LOW. When CP or $\overline{EX}$ goes HIGH, writing into the RAM is inhibited and the address buffers $(X_0 - X_3)$ are disabled.

Branch Operation – During a Branch operation, the data inputs $(\overline{D}_0 - \overline{D}_3)$ are loaded into the current program counter.

The instruction code and the $\overline{EX}$ Input are set up when CP is HIGH. The Stack Pointer remains unchanged. When CP goes LOW (assuming $\overline{EX}$ is LOW) the D-Bus Inputs are written into the current PC. The X-Bus drivers are not enabled during a Branch operation.

Call Operation - During a Call operation the content of the data bus is loaded into the top location of the stack and all previous PC values are effectively moved down one level.

The instruction code and the $\overline{EX}$ input are set up when CP is HIGH. When $\overline{EX}$ is LOW, a "one" is added to the Stack Pointer value thus incrementing the RAM address. Since the output latches go to the nontransparent or store mode when CP is LOW, the O-Bus outputs will reflect the RAM output at the CP negative-going transition. If EX goes LOW considerably before CP goes LOW, the O-Bus will correspond to the previous contents of the incremented RAM address after CP goes LOW. If CP goes LOW a very short time after $\overline{EX}$, the O-Bus will remain unchanged until the LOW to HIGH transition of CP. When CP is LOW (assuming $\overline{EX}$ is LOW) the D-Bus inputs are written into this new RAM location. On the LOW-to-HIGH transition of CP, the incremented Stack Pointer value is loaded into the Stack Pointer and the O-Bus outputs reflect the newly entered data. When the RAM address is "1111" the Stack Full output $(\overline{SF})$ is LOW, indicating that no further Call operations should be initiated. If an additional Call operation is performed SP is incremented to (0000), the contents of that location will be written over, $\overline{SF}$ will go HIGH and the Stack Empty $(\overline{SE})$ will go LOW.

The X-Bus drivers are not enabled during a Call operation.

Return Operation – During the Return operation the previous PC is "popped" to become the current PC.

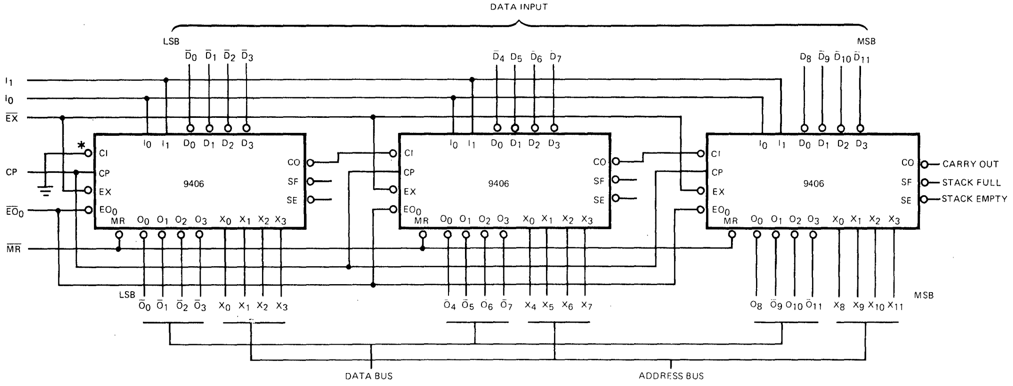
The instruction is set up when CP is HIGH. When $\overline{EX}$ is LOW, a "one" is subtracted from the Stack Pointer value, thus decrementing the RAM address. If $\overline{EX}$ goes LOW considerably before CP goes LOW, the O-Bus will correspond to the new value after $\overline{EX}$ goes LOW. If CP goes LOW a short time after $\overline{EX}$, the O-Bus will remain unchanged until the LOW-to-HIGH transition of CP.

On the LOW-to-HIGH transition of CP the decremented Stack Pointer value is loaded into the Stack Pointer and the O-Bus outputs correspond to the new "popped" value.

The X-Bus drivers are not enabled during a Return operation. When the RAM address is "0000", the Stack Empty output $(\overline{SE})$ is LOW, indicating that no further return operations should be initiated. If an additional Return operation is performed, SP is decremented to "1111", the $\overline{SE}$ will go HIGH and the Stack Full output $(\overline{SF})$ will go LOW. A LOW on the Master Reset $(\overline{MR})$ causes the SP to be reset and the contents of that RAM location (0000) to be cleared. The Stack Empty $(\overline{SE})$ output goes LOW. This operation overrides all other inputs.

EXPANSION – The 9406 may be expanded to any word length in multiples of four without external logic. The connection for expanded operation is shown in *Figure 1.* Carry In $(\overline{CI})$ and Carry Out $(\overline{CO})$ are connected to provide automatic increment of the current program counter during Fetch. The $\overline{CI}$ input of the least significant 9406 is tied LOW to ground.

If automatic increment during Fetch is not desired, the $\overline{CI}$ input of the least significant 9406 is held HIGH.



*Tie to V_{CC} to disable automatic increment.

Fig. 1
16 BY 12 PROGRAM STACK

DC CHARACTERISTICS OVER OPERATION TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage $\overline{CO}, \overline{SE}, \overline{SF}$	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 µA	
		XC	2.4	3.4				
V_{OH}	Output HIGH Voltage $X_0 - X_3, \overline{O}_0 - \overline{O}_3$	XM	2.4	3.4		V	I_{OH} = −2.0 mA	V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = −5.7 mA	
V_{OL}	Output LOW Voltage $\overline{CO}, \overline{SE}, \overline{SF}$			0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA	
				0.35	0.5		V_{CC} = MIN, I_{OL} = 8.0 mA	
V_{OL}	Output LOW Voltage $X_0 - X_3, \overline{O}_0 - \overline{O}_3$			0.25	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA	
				0.35	0.5		V_{CC} = MIN, I_{OL} = 16 mA	
I_{OZH}	Output Off HIGH Current				100	µA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2 V	
I_{OZL}	Output Off LOW Current				−100	µA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 2 V	
I_{IH}	Input HIGH Current			1.0	40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)	
I_{CCH}	Supply Current			100	160	mA	V_{CC} = MAX	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC SET-UP REQUIREMENTS – ALL MODES OF OPERATION: $V_{CC} = 5.0$ V, $T_A = 25°$C, $C_L = 15$ pF

SYMBOL	PARAMETERS	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{CW}	Clock Period	100	70		ns	
t_{PWH}	Clock Pulse Width (HIGH)	60	40		ns	
t_{PWL}	Clock Pulse Width (LOW)	40	25		ns	
$t_s\overline{EX}$	Set-Up Time, $\overline{EX}$ to CP		0		ns	
$t_h\overline{EX}$	Hold Time, $\overline{EX}$ to CP		0		ns	Figure 2
t_sI	Set-Up Time, I_0, I_1 to Negative-Going Clock		20		ns	
t_hI	Hold Time, I_0, I_1 to Positive-Going Clock		0		ns	
$t_s\overline{CI}$	Set-Up Time, $\overline{CI}$ to Negative-Going Clock		5		ns	
$t_h\overline{CI}$	Hold Time, $\overline{CI}$ to Positive-Going Clock		0		ns	
$t_s\overline{D}$	Set-Up Time, $\overline{D}_0$–$\overline{D}_3$ to Positive-Going Clock		20		ns	
$t_h\overline{D}$	Hold Time, $\overline{D}_0$ – $\overline{D}_3$ to Positive-Going Clock		0		ns	
$t_{PWL}\overline{MR}$	$\overline{MR}$ Pulse Width (LOW)	40	25		ns	Figure 3
t_{rec}	$\overline{MR}$ to Negative-Going Clock	45	30		ns	

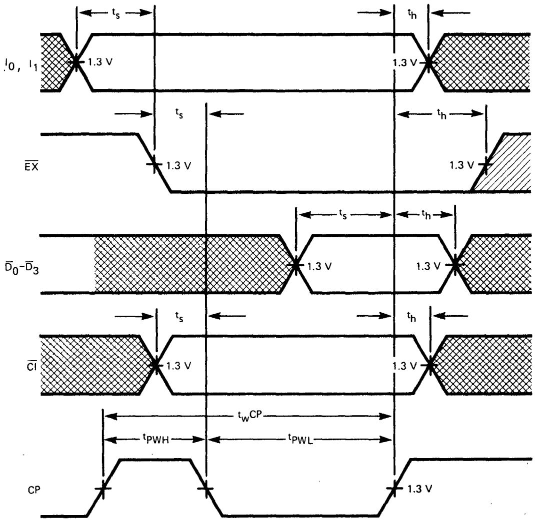


Fig. 2
WAVEFORMS FOR ALL OPERATIONS

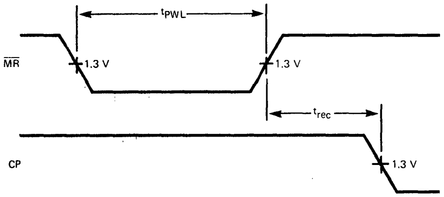


Fig. 3
RESET OPERATION

Refer to individual timing diagrams for each operation to determine output response.

AC CHARACTERISTICS - FETCH OPERATION: $V_{CC} = 5.0$ V, $T_A = 25^{\circ}$C, $C_L = 15$ pF

SYMBOL	PARAMETERS	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Carry In ($\overline{CI}$) to Carry Out ($\overline{CO}$)		11 7	16 12	ns	Figure 4
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going CP to Carry Out ($\overline{CO}$)		28 46	41 66	ns	Figure 5
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{EX}$ to Carry Out ($\overline{CO}$)		34 38	45 60	ns	Figure 6

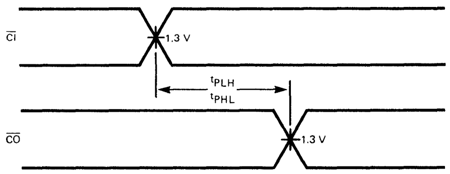


Fig. 4
CARRY-IN TO CARRY-OUT

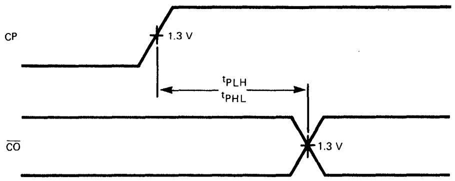


Fig. 5
CLOCK TO CARRY-OUT

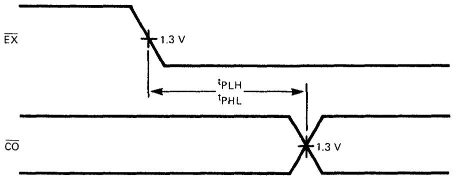


Fig. 6
EXECUTE TO CARRY-OUT

AC CHARACTERISTICS AND SET-UP REQUIREMENTS - BRANCH (LOAD PC) OPERATION: $V_{CC} = 5.0$ V, $T_A = 25^{\circ}$C, $C_L = 15$ pF

SYMBOL	PARAMETERS	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going CP to Outputs ($\overline{O}_0 - \overline{O}_3$)		28 45	41 66	ns	$\overline{EO}_0$ LOW Figures 7 and 8
t_s	Set-Up Time, I_0, I_1 to Negative-Going $\overline{EX}$	30	20		ns	
t_h	Hold Time I_0, I_1 to Positive-Going $\overline{EX}$	0	0		ns	$\overline{EX}$ goes HIGH before CP, Figure 8
t_h	Hold Time, I_0, I_1 to Positive-Going CP	0	0		ns	CP goes HIGH before $\overline{EX}$, Figure 7
t_s	Set-Up Time, $\overline{D}_0 - \overline{D}_3$ to Positive-Going CP	25	16		ns	Figures 7 and 8
t_h	Hold Time, $\overline{D}_0 - \overline{D}_3$ to Positive-Going CP	0	0		ns	
t_{PWL}	$\overline{EX}$ Pulse Width	45	30		ns	$\overline{EX}$ Goes HIGH Before CP, Figure 8

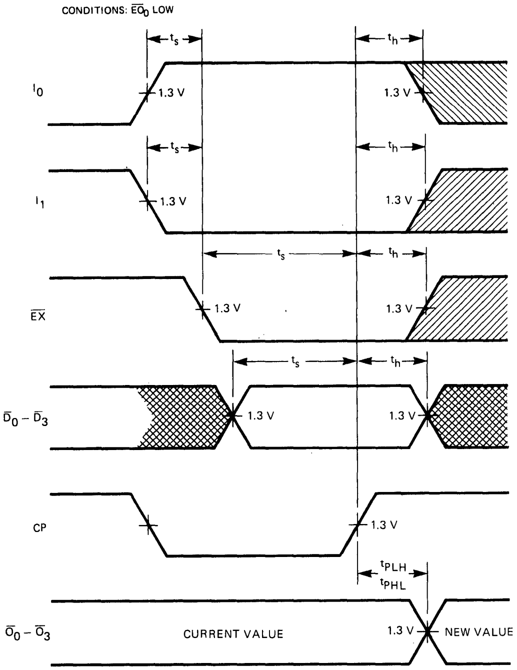


Fig. 7
BRANCH OPERATION, CP GOES HIGH BEFORE $\overline{EX}$

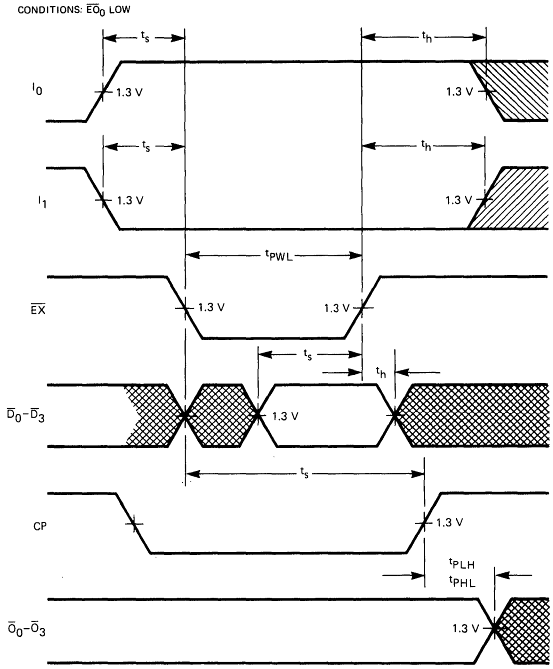


Fig. 8
BRANCH OPERATION, $\overline{EX}$ GOES HIGH BEFORE CP

AC CHARACTERISTICS AND SET-UP REQUIREMENTS - CALL (PUSH) OPERATION:

$V_{CC} = 5.0$ V, $T_A = 25°$C, $C_L = 15$ pF (Figure 9)

SYMBOL	PARAMETERS	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going CP to New Value of $\overline{O}_0 - \overline{O}_3$		25 75	40 130	ns	$\overline{EO}_0$ LOW
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{EX}$ to Intermediate Value of $\overline{O}_0 - \overline{O}_3$		22 64	35 85	ns	$\overline{EO}_0$ LOW, Set-Up Requirements $t_{s1}\overline{EX}$ must be met
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{EX}$ to $\overline{SE}$, $\overline{SF}$		18 43	28 59	ns	
t_s	Set-Up Time, Negative-Going $\overline{EX}$ to I_0, I_1	30	20		ns	
t_h	Hold Time, Positive-Going CP to I_0, I_1	0			ns	
$t_{s1}\overline{EX}$	Set-Up Time, $\overline{EX}$ to Negative-Going CP which Guarantees Intermediate Data on $\overline{O}_0 - \overline{O}_3$ while CP is LOW	65	45		ns	
$t_{s2}\overline{EX}$	Set-Up Time, $\overline{EX}$ to Negative-Going CP which Guarantees no Change in $\overline{O}_0 - \overline{O}_3$ While CP is LOW	0			ns	
$t_h\overline{EX}$	Hold Time, Positive-Going CP to Positive-Going $\overline{EX}$	0			ns	
t_s	Set-Up Time, $\overline{D}_0 - \overline{D}_3$ to Positive-Going CP	30	20		ns	
t_h	Hold Time, Positive-Going CP to $\overline{D}_0 - \overline{D}_3$	0			ns	

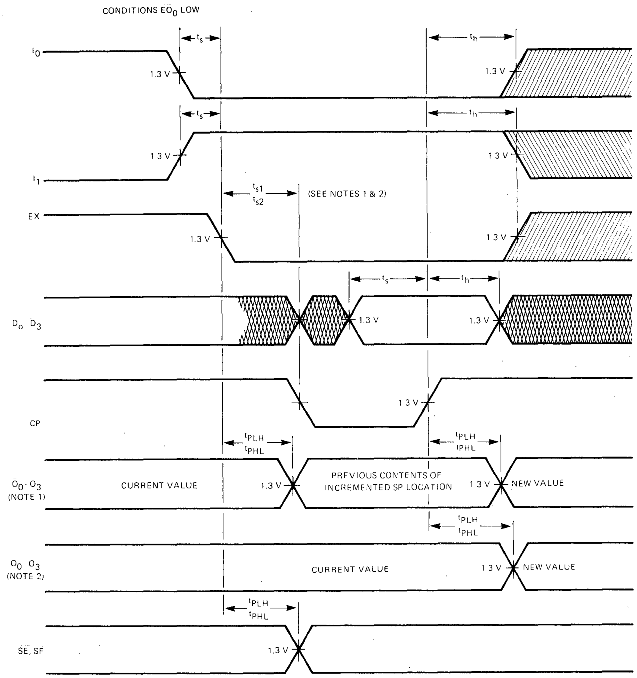


Fig. 9
CALL (PUSH) OPERATION

NOTES:
1. Condition which occurs when $\overline{EX}$ goes LOW considerably before CP goes LOW ($t_{s1}\overline{EX}$ is met).
2. Condition which occurs when $\overline{EX}$ goes LOW slightly before CP goes LOW ($t_{s2}\overline{EX}$ is met).

AC CHARACTERISTICS AND SET-UP REQUIREMENTS - RETURN (POP) OPERATION:

$V_{CC} = 5.0$ V, $T_A = 25°$C, $C_L = 15$ pF (Figure 10)

SYMBOL	PARAMETERS	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going CP to New Value of $\overline{O}_0 - \overline{O}_3$		25 103	40 130	ns	$\overline{EO}_0$ LOW
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{EX}$ to New Value of $\overline{O}_0 - \overline{O}_3$		23 101	40 130	ns	$\overline{EO}_0$ LOW, Set-Up Requirements $t_{s1}\overline{EX}$ must be met
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{EX}$ to $\overline{SE}$, $\overline{SF}$		18 43	28 59	ns	
t_s	Set-Up Time, Negative-Going $\overline{EX}$ to I_0, I_1	30	20		ns	
t_h	Hold Time, Positive-Going CP to I_0, I_1	0			ns	
$t_{s1}\overline{EX}$	Set-Up Time, $\overline{EX}$ to Negative-Going CP which Guarantees the New Value on $\overline{O}_0 - \overline{O}_3$ While CP is LOW	65	45		ns	
$t_{s2}\overline{EX}$	Set-Up Time, $\overline{EX}$ to Negative-Going CP. Either $t_{s2}\overline{EX}$ or $t_{s3}\overline{EX}$ must be met for Proper Operation	0			ns	
$t_{s3}\overline{EX}$	Set-Up Time, EX to Positive-Going CP. Either $t_{s3}\overline{EX}$ or $t_{s2}\overline{EX}$ (Above) must be met for Proper Operation.	45	30		ns	

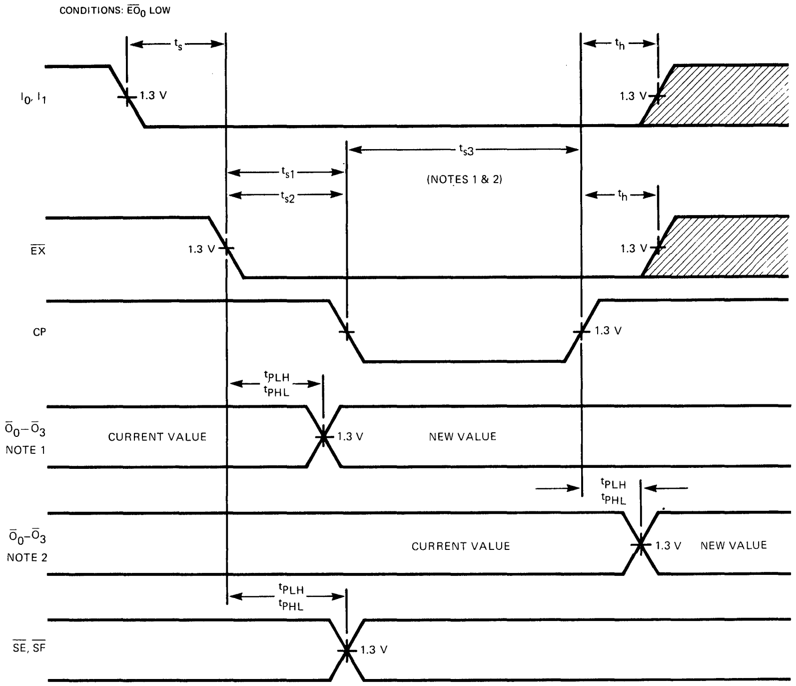


Fig. 10
RETURN (POP) OPERATION

NOTES:

1. Condition which occurs when $\overline{EX}$ goes LOW considerably before CP goes LOW ($t_{s1}\overline{EX}$ is met).
2. Condition which occurs when $\overline{EX}$ goes LOW slightly before or after CP goes LOW (either $t_{s2}\overline{EX}$ or $t_{s3}\overline{EX}$ are met).

AC CHARACTERISTICS AND SET-UP REQUIREMENTS - FETCH OPERATION:

$V_{CC} = 5.0$ V, $T_A = 25°$C, $C_L = 15$ pF

SYMBOL	PARAMETERS	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay Positive-Going CP to Incremented Value of $\overline{O}_0 - \overline{O}_3$		22 59	30 80	ns	$\overline{EO}_0$, $\overline{CI}$ LOW, Figures 13 and 14
t_{PZL} t_{PZH}	Turn-On Delay, from CP or $\overline{EX}$ Whichever goes LOW last to $X_0 - X_3$		13 12	18 17	ns	$\overline{EO}_X$ LOW, Figures 11, 12, 13 and 14
t_{PLZ} t_{PHZ}	Delay Going into HIGH Impedance State		7 10	12 16	ns	
t_s	Set-Up Time, I_0, I_1 to Negative-Going $\overline{EX}$	30	20		ns	Figures 11, 12, 13 and 14
t_h	Hold Time , I_0, I_1 to CP or $\overline{EX}$ whichever goes HIGH first	0			ns	
t_s	Set-Up Time, Negative Going $\overline{EX}$ to Positive-Going CP	40	25		ns	
t_s	Negative-Going $\overline{CI}$ to Positive-Going CP	30	20		ns	Fetch with Increment, Figures 13 and 14
t_h	Positive-Going $\overline{CI}$ to Negative-Going $\overline{EX}$	0				Iterative Fetch, Figures 11 and 12

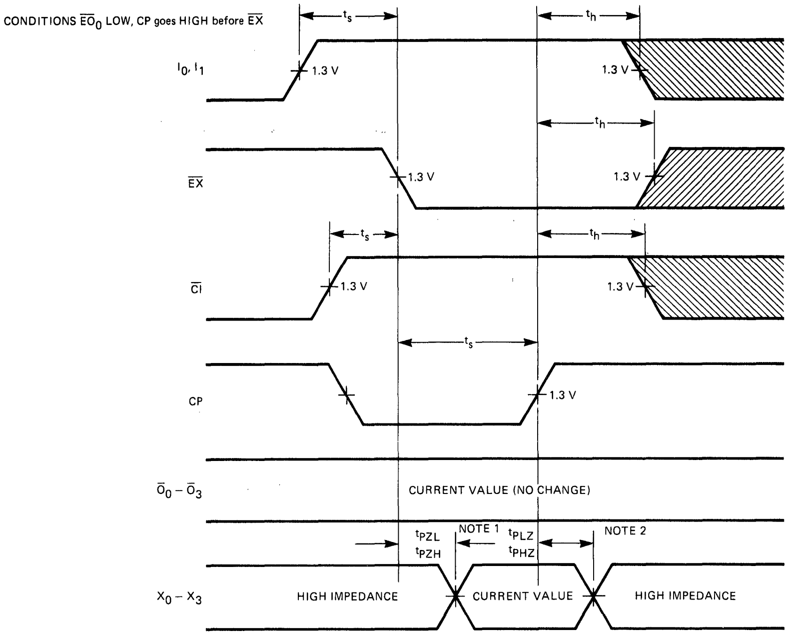


Fig. 11
ITERATIVE FETCH

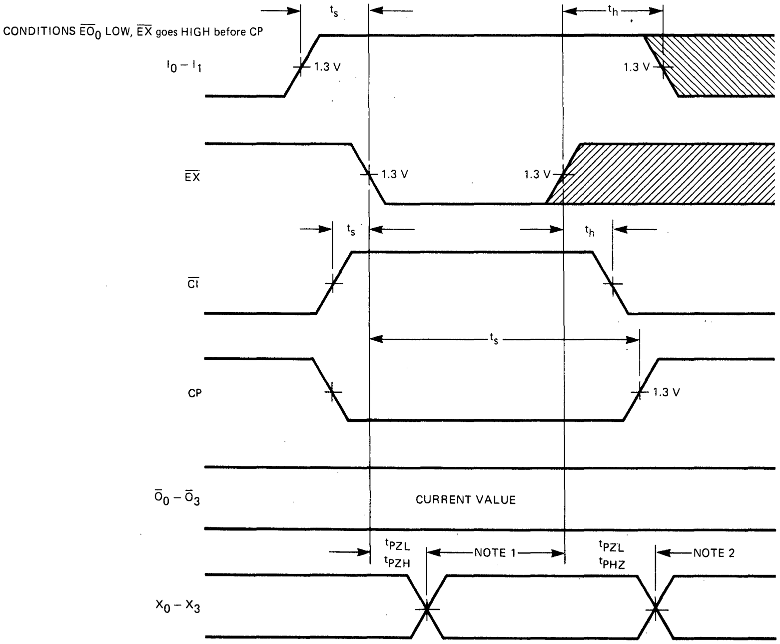


Fig. 12
ITERATIVE FETCH

NOTES:

1. $X_0 - X_3$ Turn-On Delay measured from the time both $\overline{EX}$ and CP go LOW.
2. $X_0 - X_3$ Turn-Off Delay measured from the time either $\overline{EX}$ or CP goes HIGH.

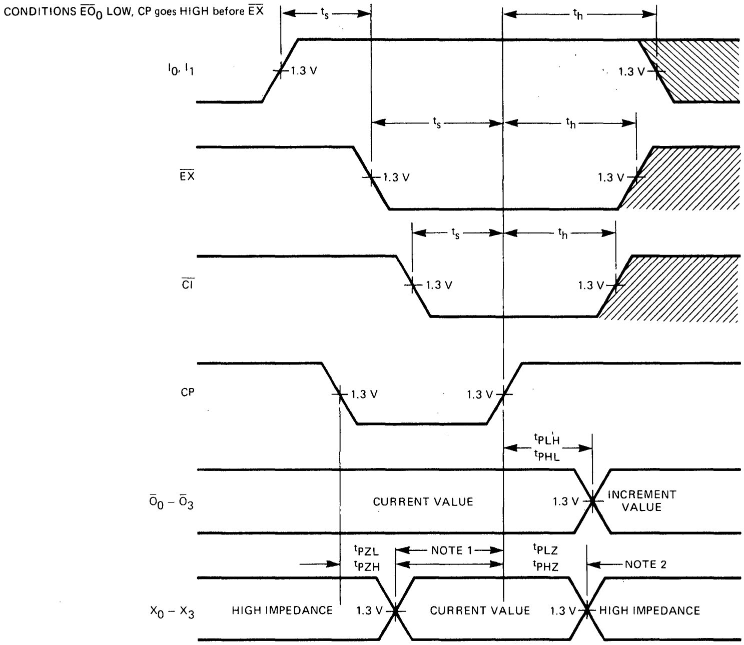


Fig. 13
FETCH WITH INCREMENT PC

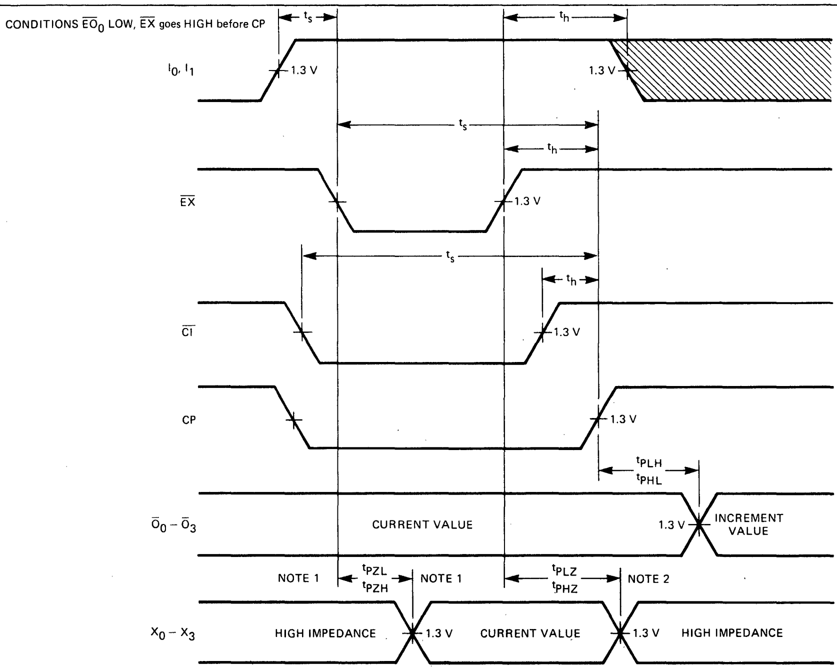


Fig. 14
FETCH OPERATION WITH INCREMENT PC

NOTES:
1. $X_0 - X_3$ Turn-On Delay measured from the time both $\overline{EX}$ and CP go LOW.
2. $X_0 - X_3$ Turn-Off Delay measured from the time either $\overline{EX}$ or CP goes HIGH.

9410

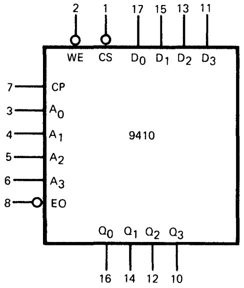
REGISTER STACK • 16×4 RAM WITH 3-STATE OUTPUT REGISTER

FAIRCHILD TTL MACROLOGIC

DESCRIPTION – The 9410 is a register oriented high speed 64-bit Read/Write Memory organized as 16-words by 4-bits. An edge triggered 4-bit output register allows new input data to be written while previous data is held. 3-state outputs are provided for maximum versatility. The 9410 is fully compatible with all TTL families.

- **EDGE-TRIGGERED OUTPUT REGISTER**
- **TYPICAL ACCESS TIME OF 35 ns**
- **3-STATE OUTPUTS**
- **OPTIMIZED FOR REGISTER STACK OPERATION**
- **TYPICAL POWER OF 375 mW**
- **18-PIN PACKAGE**

LOGIC SYMBOL



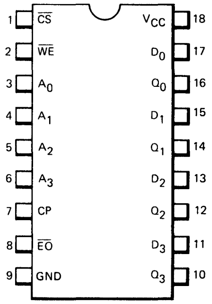
V_{CC} = Pin 18
GND = Pin 9

PIN NAMES

		LOADING (Note a) HIGH	LOADING (Note a) LOW
A_0–A_3	Address Inputs	1.0 U.L.	0.23 U.L.
D_0–D_3	Data Inputs	1.0 U.L.	0.23 U.L.
$\overline{CS}$	Chip Select Input (Active LOW)	1.0 U.L.	0.23 U.L.
$\overline{EO}$	Output Enable Input (Active LOW)	1.0 U.L.	0.23 U.L.
$\overline{WE}$	Write Enable Input (Active LOW)	1.0 U.L.	0.23 U.L.
CP	Clock Input (Outputs Change on LOW to HIGH Transition)	1.0 U.L.	0.23 U.L.
Q_0–Q_3	Outputs	130 U.L.	10 U.L. (Note b)

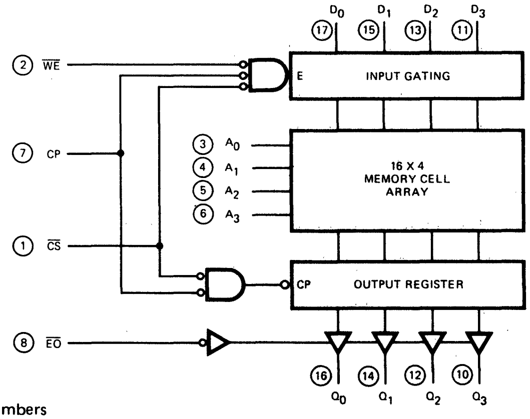
NOTES:
a) 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW.
b) 10 LOW Unit Loads measured at 0.5 V.

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

BLOCK DIAGRAM



V_{DD} = Pin 18
V_{SS} = Pin 9
○ = Pin Numbers

FUNCTIONAL DESCRIPTION

Write Operation - When the three control inputs: Write Enable (WE), Chip Select (CS), and Clock (CP), are LOW the information on the data inputs (D_0 - D_3) is written into the memory location selected by the address inputs (A_0 - A_3). If the input data changes while WE, CS, and CP are LOW, the contents of the selected memory location follows these changes, provided set-up time criteria are met.

Read Operation - Whenever CS is LOW and CP goes from LOW-to-HIGH, the contents of the memory location selected by the address inputs ($A_0 - A_3$) is edge-triggered into the Output Register.

A 3-State Output Enable (EO) controls the output buffers. When EO is HIGH the four outputs (Q_0 - Q_3) are in a high impedance or OFF state; when EO is LOW, the outputs are determined by the state of the Output Register.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4			I_{OH} = −2.0 mA	V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = −5.2 mA	
V_{OL}	Output LOW Voltage	XM & XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA	
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 16 mA	
I_{OZH}	Output Off HIGH Current				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 3 V	
I_{OZL}	Output Off LOW Current				−100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 3 V	
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)	
I_{CCH}	Supply Current			75	110	mA	V_{CC} = MAX, Inputs Open	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
READ MODE						
t_{PZH} t_{PZL}	Enable Delay, Output Enable to Output		9 9	15 15	ns ns	Figure 1
t_{PHZ} t_{PLZ}	Disable Time, Output Enable to Output		10 10	16 16	ns ns	Figure 1
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		14 14	20 20	ns ns	Figure 2
t_sAR	Set-up Time to Read from Address to Clock	38	25		ns	Figure 2
t_hAR	Hold Time to Read from Address to Clock	0			ns	Figure 2
WRITE MODE						
t_W	Write Enable, Chip Select, or Clock Pulse Width Required to Write (Note a)	21	12		ns	Figure 3
t_sAW	Set-up Time Address to Write Enable (Note b)	5			ns	Figure 3
t_hAW	Hold Time Address to Write Enable (Note b)	0			ns	Figure 3
t_sDW	Set-up Time Data to Write Enable (Note b)	16	9		ns	Figure 3
t_hDW	Hold Time Data to Write Enable	0			ns	Figure 3

NOTES:

a) Writing occurs when $\overline{WE}$, $\overline{CE}$ and CP are LOW.

b) Assuming $\overline{WE}$ is utilized as Writing Strobe.

READ MODE AC PARAMETERS

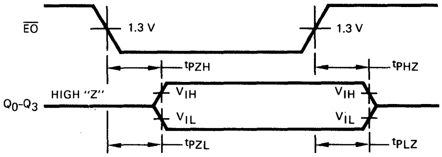
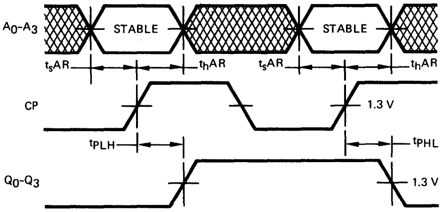


Fig. 1

PROPAGATION DELAY
OUTPUT ENABLE TO DATA OUTPUTS

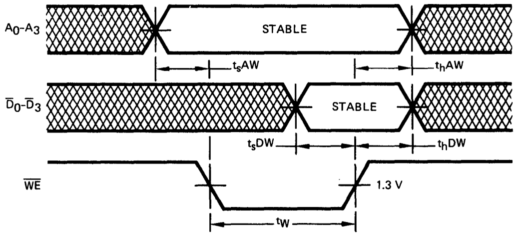


Other Conditions: $\overline{CS}$ = $\overline{OE}$ = LOW

Fig. 2

PROPAGATION DELAY CLOCK
TO DATA OUTPUTS, AND SET-UP
AND HOLD TIMES ADDRESS TO CLOCK TO READ

WRITE MODE AC PARAMETERS



Other Conditions: $\overline{CS}$ = CP = LOW

Fig. 3

WRITE ENABLE PULSE
WIDTH, SET-UP AND HOLD
TIMES ADDRESS AND DATA TO WRITE ENABLE

FUNCTIONAL DESCRIPTION

Write Operation - When the three control inputs: Write Enable (WE), Chip Select (CS), and Clock (CP), are LOW the information on the data inputs (D_0 - D_3) is written into the memory location selected by the address inputs (A_0 - A_3). If the input data changes while WE, CS, and CP are LOW, the contents of the selected memory location follows these changes, provided set-up time criteria are met.

Read Operation - Whenever CS is LOW and CP goes from LOW-to-HIGH, the contents of the memory location selected by the address inputs ($A_0 - A_3$) is edge-triggered into the Output Register.

A 3-State Output Enable (EO) controls the output buffers. When EO is HIGH the four outputs (Q_0 - Q_3) are in a high impedance or OFF state; when EO is LOW, the outputs are determined by the state of the Output Register.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	XM	2.4	3.4			I_{OH} = −2.0 mA	V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = −5.2 mA	
V_{OL}	Output LOW Voltage	XM & XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA	
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 16 mA	
I_{OZH}	Output Off HIGH Current				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 3 V	
I_{OZL}	Output Off LOW Current				−100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 3 V	
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)	
I_{CCH}	Supply Current			75	110	mA	V_{CC} = MAX, Inputs Open	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

9423

FIRST-IN FIRST-OUT (FIFO) BUFFER MEMORY

FAIRCHILD I³L™ MACROLOGIC

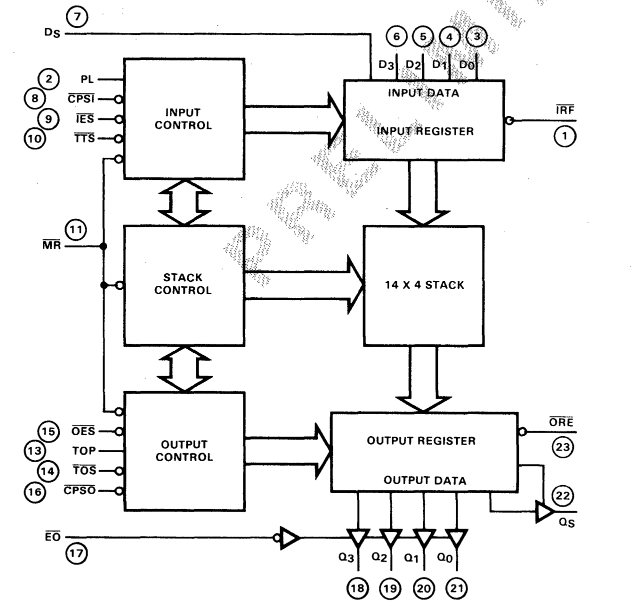
DESCRIPTION – The 9423 is an expandable fall-through type high-speed First-In First-Out (FIFO) Buffer Memory optimized for high speed disc or tape controllers and communication buffer applications. It is organized as 64 words by four bits and may be expanded to any number of words or any number of bits (in multiples of four). Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

The 9423 has 3-state outputs which provide added versatility and is fully compatible with all TTL families.

- **SERIAL OR PARALLEL INPUT**
- **SERIAL OR PARALLEL OUTPUT**
- **EXPANDABLE WITHOUT EXTERNAL LOGIC**
- **3-STATE OUTPUTS**
- **FULLY COMPATIBLE WITH ALL TTL FAMILIES**
- **SLIM 24-PIN PACKAGE**

PRELIMINARY

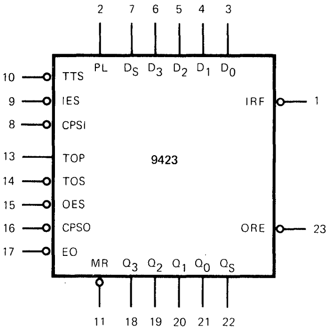
BLOCK DIAGRAM



V_{CC} = Pin 24
GND = Pin 12

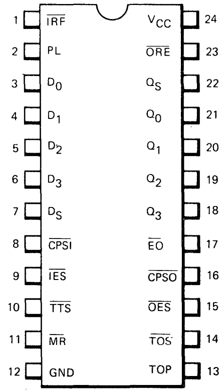
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the **Dual In-line Package.**

PIN NAMES

PIN NAME	DESCRIPTION	LOADING (Note a) HIGH	LOADING (Note a) LOW	COMMENTS
$D_0 - D_3$	Parallel Data Inputs	1.0 U.L.	0.23 U.L.	
D_S	Serial Data Input	1.0 U.L.	0.23 U.L.	
PL	Parallel Load Input	1.0 U.L.	0.23 U.L.	HIGH on PL enables $D_0 - D_3$. Not edge triggered. Ones catching.
$\overline{\text{CPSI}}$	Serial Input Clock	1.0 U.L.	0.23 U.L.	Edge triggered. Activates on falling edge.
$\overline{\text{IES}}$	Serial Input Enable	1.0 U.L.	0.23 U.L.	Enables serial and parallel input when LOW.
$\overline{\text{TTS}}$	Transfer to Stack Input	1.0 U.L.	0.23 U.L.	A LOW on this pin initiates fall through.
$\overline{\text{OES}}$	Serial Output Enable Input	1.0 U.L.	0.46 U.L.	Enables serial and parallel output when LOW.
$\overline{\text{TOS}}$	Transfer Out Serial Input	1.0 U.L.	0.23 U.L.	A LOW on this pin enables a word to be transferred from the stack to the output register. (TOP must be HIGH also for the transfer to occur). Not edge triggered.
TOP	Transfer Out Parallel Input	1.0 U.L.	0.23 U.L.	A HIGH on this pin enables a word to be transferred from the stack to the output register. ($\overline{\text{TOS}}$ must be LOW for the transfer to occur). Not edge triggered.
$\overline{\text{MR}}$	Master Reset	2.0 U.L.	0.46 U.L.	Active LOW.
$\overline{\text{EO}}$	Output Enable	1.0 U.L.	0.23 U.L.	Active LOW.
$\overline{\text{CPSO}}$	Serial Output Clock Input	1.0 U.L.	0.23 U.L.	Edge triggered. Activates on falling edge.
$Q_0 - Q_3$	Parallel Data Outputs	130 U.L.	10 U.L.	(Note b)
Q_S	Serial Data Output	10 U.L.	10 U.L.	(Note b)
$\overline{\text{IRF}}$	Input Register Full Output	10 U.L.	5 U.L.	LOW when input register is full (Note b).
$\overline{\text{ORE}}$	Output Register Empty Output	10 U.L.	5 U.L.	HIGH when output register contains valid data.

NOTE: a. 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW.
b. Output fan-out with $V_{OL} \leqslant 0.5$ V.

FUNCTIONAL DESCRIPTION – As shown in the block diagram the 9423 consists of three sections:

1. An Input Register with parallel and serial data inputs as well as control inputs and outputs for input handshaking and expansion.
2. A 4-bit wide, 62-word deep fall-through stack with self-contained control logic.
3. An Output Register with parallel and serial data outputs as well as control inputs and outputs for output handshaking and expansion.

Since these three sections operate asynchronously and almost independently, they will be described separately below:

Input Register (Data Entry):
The Input Register can receive data in either bit-serial or in 4-bit parallel form. It stores this data until it is sent to the fall-through stack and generates the necessary status and control signals.

Figure 1 is a conceptual logic diagram of the input section. As described later, this 5-bit register is initialized by setting the F3 flip-flop and resetting the other flip-flops. The Q-output of the last flip-flop (FC) is brought out as the "Input Register Full" output ($\overline{\text{IRF}}$). After initialization this output is HIGH.

Parallel Entry – A HIGH on the PL input loads the D_0 - D_3 inputs into the F_0 - F_3 flip-flops and sets the FC flip-flop. This forces the $\overline{\text{IRF}}$ output LOW indicating that the input register is full. During parallel entry, the $\overline{\text{CPSI}}$ input must be LOW.

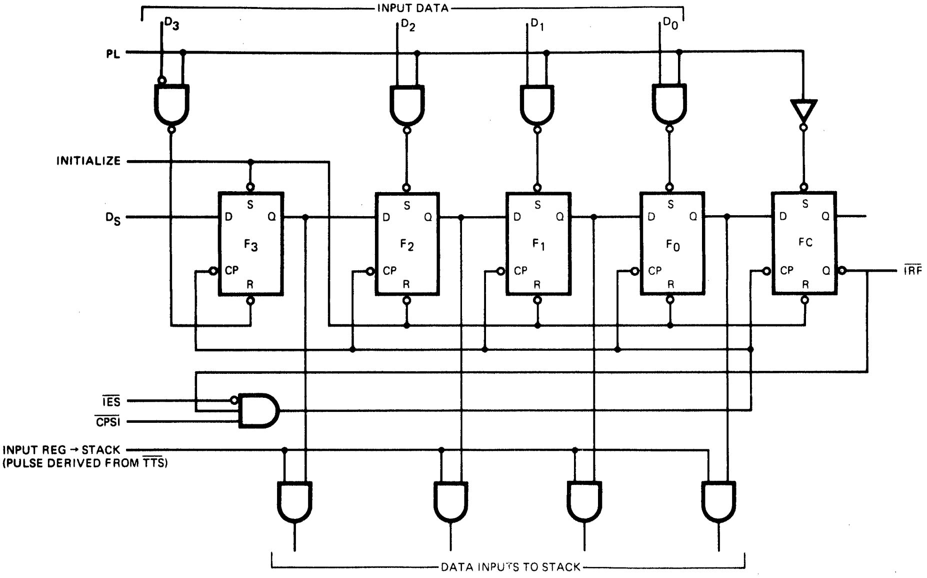


Fig. 1
CONCEPTUAL INPUT SECTION

Serial Entry - Data on the D_S input is serially entered into the F_3, F_2, F_1, F_0, FC shift register on each HIGH-to-LOW transition of the CPSI clock input, provided IES is LOW. During serial entry PL input should be LOW.

After the fourth clock transition, the four data bits are located in the four flip-flops F_0 - F_3. The FC flip-flop is set, forcing the $\overline{IRF}$ output LOW and internally inhibiting $\overline{CPSI}$ clock pulsed from effecting the register. *Figure 2* illustrates the final positions in a 9423 resulting from a 256-bit serial bit train. B_0 is the first bit, B_{255} the last bit.

Transfer to the Stack - The outputs of Flip-Flops F_0 - F_3 feed the stack. A LOW level on the $\overline{TTS}$ input initiates a "fall-through" action. If the top location of the stack is empty, data is loaded into the stack and the input register is re-initialized. Note that this initialization is postponed until PL is LOW. Thus, automatic FIFO action is achieved by connecting the $\overline{IRF}$ output to the $\overline{TTS}$ input.

An RS Flip-Flop (the Request Initialization Flip-Flop shown in *Figure 9)* in the control section records the fact that data has been transferred to the stack. This prevents multiple entry of the same word into the stack despite the fact the $\overline{IRF}$ and $\overline{TTS}$ may still be LOW. The Request Initialization Flip-Flop is not cleared until PL goes LOW. Once in the stack, data falls through the stack automatically, pausing only when it is necessary to wait for an empty next location. In the 9423, as in most modern FIFO designs, the $\overline{MR}$ input only initializes the stack control section and does not clear the data.

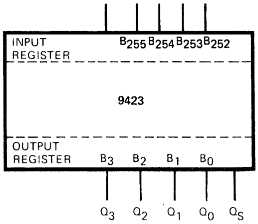


Fig. 2
FINAL POSITIONS IN A 9423 RESULTING
FROM A 256-BIT SERIAL TRAIN

Output Register (Data Extraction) - The Output Register receives 4-bit data words from the bottom stack location, stores it and outputs data on a 3-state 4-bit parallel data bus or on a 3-state serial data bus. The output section generates and receives the necessary status and control signals. *Figure 3* is a conceptual logic diagram of the output section.

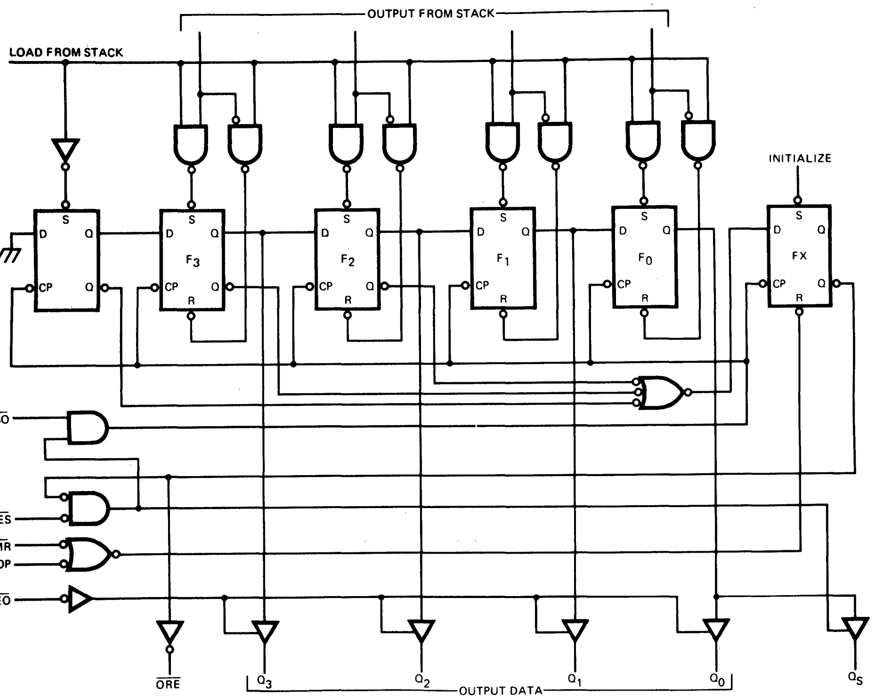


Fig. 3
CONCEPTUAL OUTPUT SECTION

Parallel Data Extraction - When the FIFO is empty after a LOW pulse is applied to $\overline{\text{MR}}$, the Output Register Empty ($\overline{\text{ORE}}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided the "Transfer Out Parallel" (TOP) input is HIGH. As a result of the data transfer $\overline{\text{ORE}}$ goes HIGH, indicating valid data on the data outputs (provided the 3-state buffer is enabled). TOP can now be used to clock out the next word. When TOP goes LOW, $\overline{\text{ORE}}$ will go LOW indicating that the output data has been extracted, but the data itself remains on the output bus until a HIGH level at TOP permits the transfer of the next word (if available) into the Output Register. During parallel data extraction $\overline{\text{CPSO}}$ should be LOW. $\overline{\text{TOS}}$ should be grounded for single slice operation or connected to the appropriate $\overline{\text{ORE}}$ for expanded operation (see Expansion section).

TOP is not edge triggered. Therefore, if TOP goes HIGH before data is available from the stack, but data does become available before TOP goes LOW again, that data will be transferred into the Output Register. However, internal control circuitry prevents the same data from being transferred twice. If TOP goes HIGH and returns to LOW before data is available from the stack, $\overline{\text{ORE}}$ remains LOW indicating that there is no valid data at the outputs.

Serial Data Extraction - When the FIFO is empty after a LOW pulse is applied to $\overline{\text{MR}}$, the Output Register Empty ($\overline{\text{ORE}}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided $\overline{\text{TOS}}$ is LOW and TOP is HIGH. As a result of the data transfer $\overline{\text{ORE}}$ goes HIGH indicating valid data in the register. The 3-state Serial Data Output, Q_S, is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the HIGH-to-LOW transition of $\overline{\text{CPSO}}$. To prevent false shifting, $\overline{\text{CPSO}}$ should be LOW when the new word is being loaded into the Output Register. The fourth transition empties the shift register, forces $\overline{\text{ORE}}$ output LOW and disables the serial output, Q_S (refer to *Figure 3*). For serial operation the $\overline{\text{ORE}}$ output may be tied to the $\overline{\text{TOS}}$ input, requesting a new word from the stack as soon as the previous one has been shifted out.

EXPANSION –

Vertical Expansion - The 9423 may be vertically expanded to store more words without external parts. The interconnections necessary to form a 190-word by 4-bit FIFO are shown in *Figure 4.* Using the same technique, any FIFO of (63 n+1) words by four bits can be constructed, where n is the number of devices. Note that expansion does not sacrifice any of the 9423's flexibility for serial/parallel input and output. For other expansion schemes, refer to the applications section of the Macrologic/Bipolar Microprocessor data book.

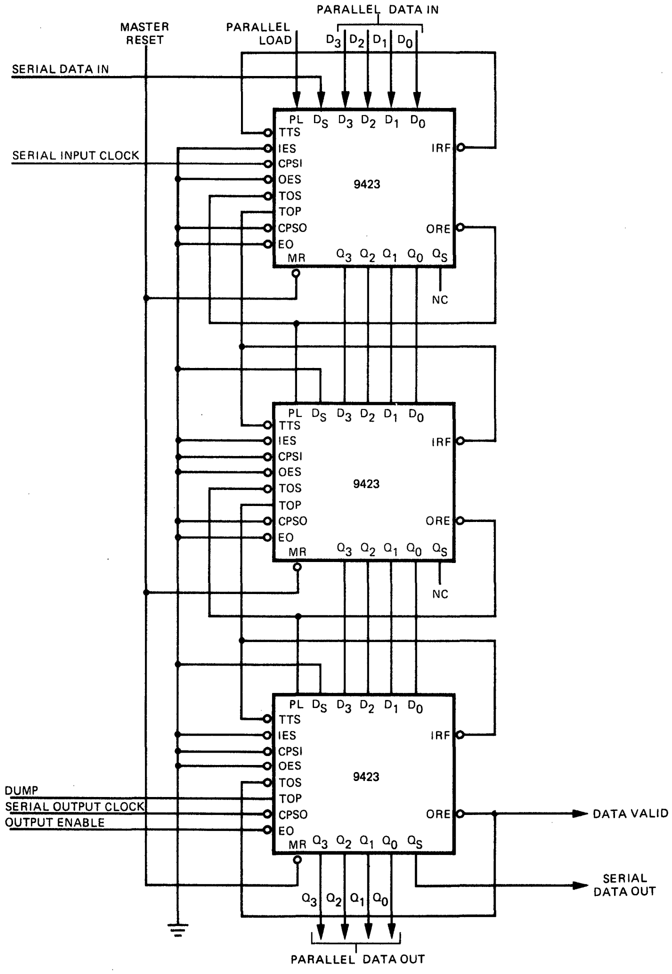


Fig. 4
A VERTICAL EXPANSION SCHEME

Horizontal Expansion - The 9423 can also be horizontally expanded to store long words (in multiples of four bits) without external logic. The interconnections necessary to form a 64-word by 12-bit FIFO are shown in *Figure 5.* Using the same technique, any FIFO of 64 words by 4n bits can be constructed, where n is the number of devices. The $\overline{IRF}$ output of the right most device (most significant device) is connected to the $\overline{TTS}$ inputs of all devices. Similarly, the $\overline{ORE}$ output of the most significant device is connected to the $\overline{TOS}$ inputs of all devices. As in the vertical expansion scheme, horizontal expansion does not sacrifice any of the 9423's flexibility for serial/parallel input and output.

It should be noted that this form of horizontal expansion extracts a penalty in speed. An expansion scheme that provides higher speed but requires additional components is shown in the Applications section of the Macrologic/Bipolar Microprocessor data book.

Horizontal and Vertical Expansion - The 9423 can be expanded in both the horizontal and vertical directions without any external parts and without sacrificing any of its FIFO's flexibility for serial/parallel input and output. The interconnections necessary to form a 127-word by 16-bit FIFO are shown in *Figure 6.* Using the same technique, any FIFO of (63m + 1) words by (4n) bits can be constructed, where m is the number of devices in a column and n is the number of devices in a row. *Figures 7* and *8* show the timing diagrams for serial data entry and extraction for the 127-word by 16-bit FIFO shown in *Figure 6.*

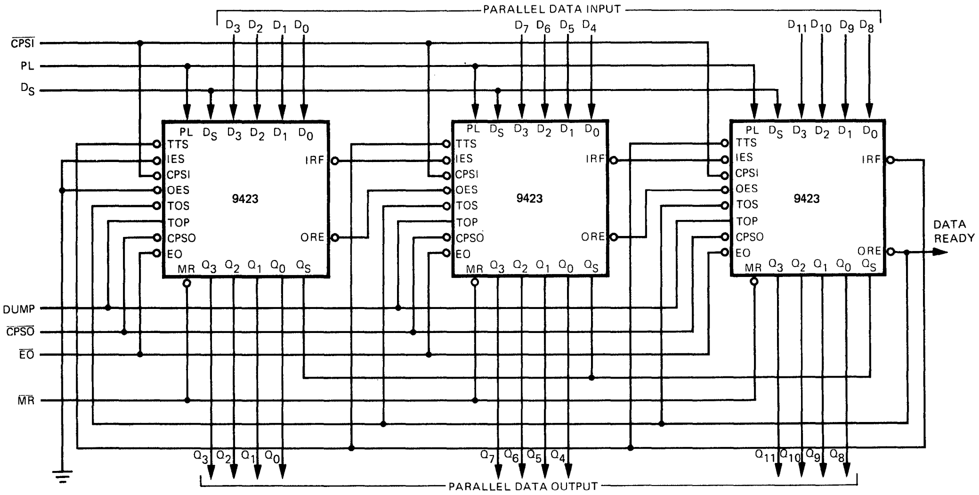


Fig. 5
A HORIZONTAL EXPANSION SCHEME

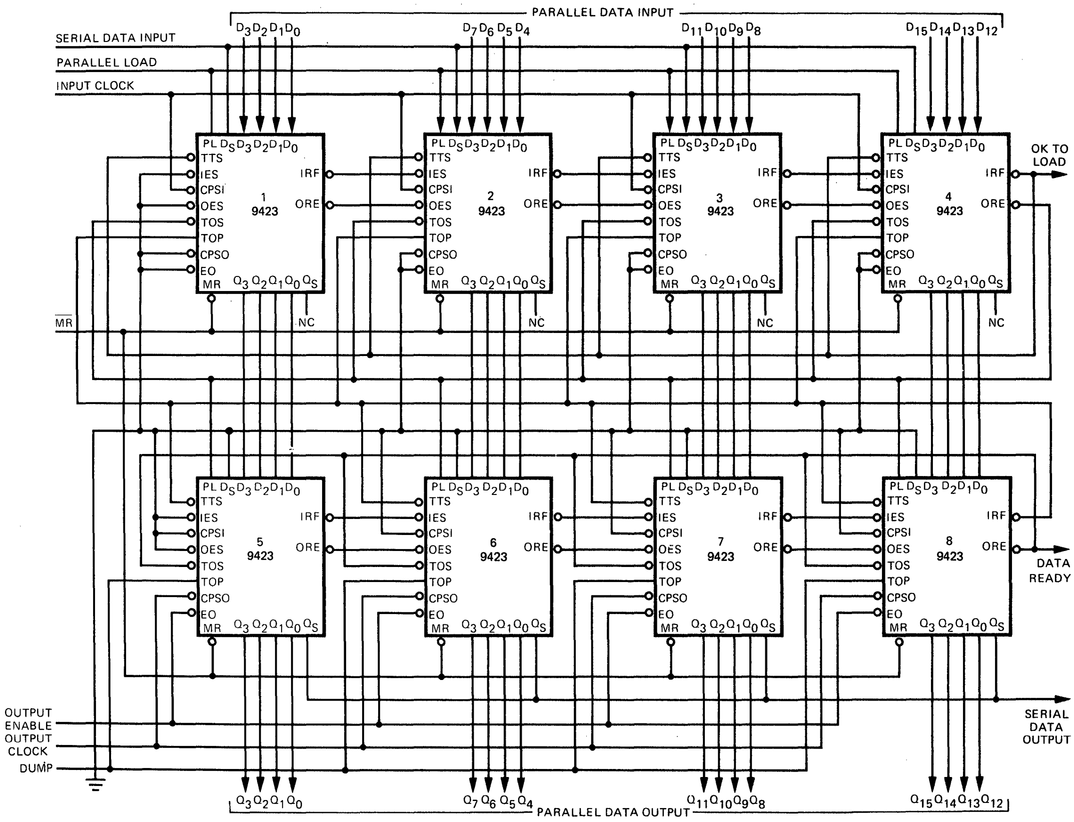


Fig. 6
A 127 X 16 FIFO ARRAY

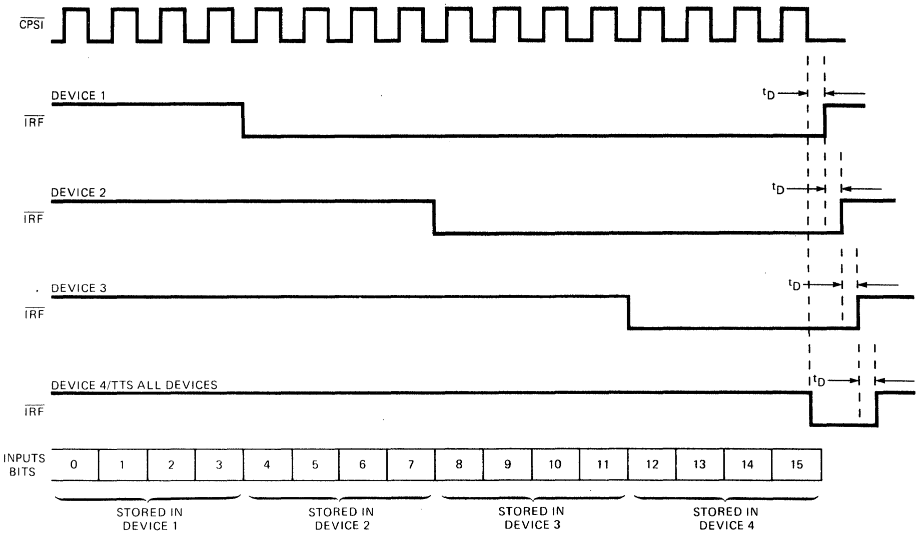


Fig. 7
SERIAL DATA ENTRY FOR ARRAY OF FIG. 6

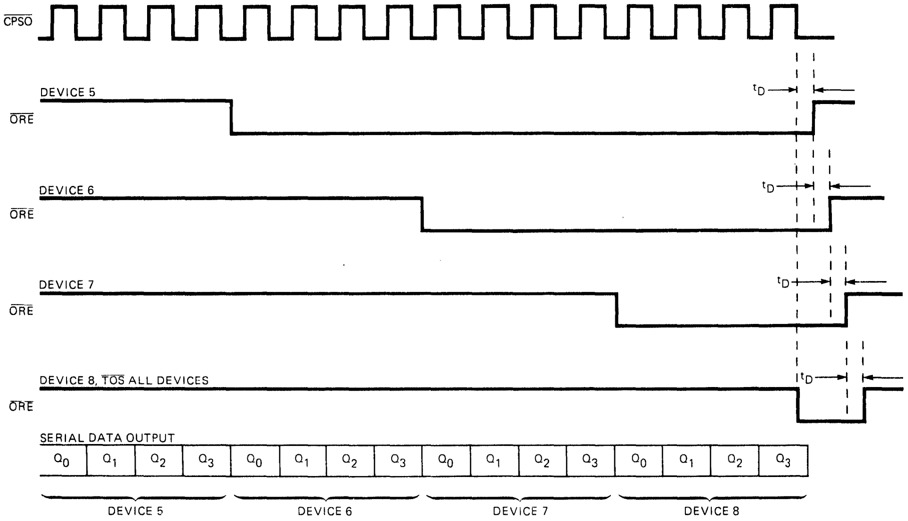


Fig. 8
SERIAL DATA EXTRACTION FOR ARRAY OF FIG. 6

Interlocking Circuitry - Most conventional FIFO designs provide status signals analogous to $\overline{\text{IRF}}$ and $\overline{\text{ORE}}$. However, when these devices are operated in arrays, variations in unit to unit operating speed require external gating to assure all devices have completed an operation. The 9423 incorporates simple but effective "master/slave" interlocking circuitry to eliminate the need for external gating.

In the 9423 array of *Figure 6* devices 1 and 5 are defined as "row masters" and the other devices are slaves to the master in their row. No slave in a given row will initialize its Input Register until it has received LOW on its $\overline{\text{IES}}$ input from a row master or a slave of higher priority.

In a similar fashion, the $\overline{\text{ORE}}$ outputs of slaves will not go HIGH until their $\overline{\text{OES}}$ inputs have gone HIGH. This interlocking scheme ensures that new input data may be accepted by the array when the $\overline{\text{IRF}}$ output of the final slave in that row goes HIGH and that output data for the array may be extracted when the $\overline{\text{ORE}}$ of the final slave in the output row goes HIGH.

The row master is established by connecting its $\overline{\text{IES}}$ input to ground while a slave receives its $\overline{\text{IES}}$ input from the $\overline{\text{IRF}}$ output of the next higher priority device. When an array of 9423 FIFOs is initialized with a LOW on the $\overline{\text{MR}}$ inputs of all devices, the $\overline{\text{IRF}}$ outputs of all devices will be HIGH. Thus, only the row master receives a LOW on the $\overline{\text{IES}}$ input during initialization. *Figure 9* is a conceptual logic diagram of the internal circuitry which determines master/slave operation. Whenever $\overline{\text{MR}}$ and $\overline{\text{IES}}$ are LOW, the Master Latch is set. Whenever $\overline{\text{TTS}}$ goes LOW the Request Initialization Flip-Flop will be set. If the Master Latch is HIGH, the Input Register will be immediately initialized and the Request Initialization Flip-Flop reset. If the Master Latch is reset, the Input Register is not initialized until $\overline{\text{IES}}$ goes LOW. In array operation, activating the $\overline{\text{TTS}}$ initiates a ripple input register initialization from the row master to the last slave.

A similar operation takes place for the output register. Either a $\overline{\text{TOS}}$ or TOP input initiates a load-from-stack operation and sets the ORE Request Flip-Flop. If the Master Latch is set, the last Output Register Flip-Flop is set and $\overline{\text{ORE}}$ goes HIGH. If the Master Latch is reset, the $\overline{\text{ORE}}$ output will be LOW until an $\overline{\text{OES}}$ input is received.

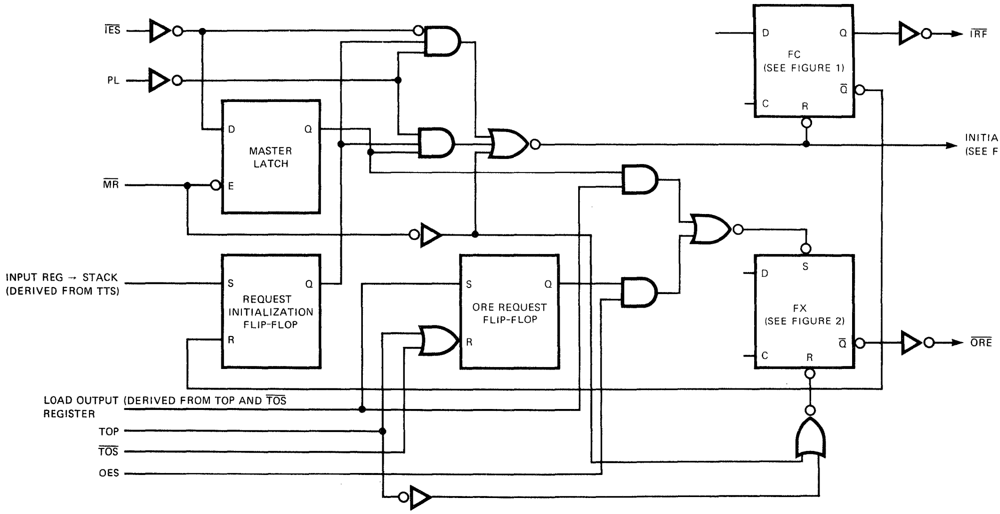


Fig. 9
CONCEPTUAL DIAGRAM, INTERLOCKING CIRCUITRY

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage	
		XC			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage, $\overline{ORE}$, $\overline{IRF}$	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 µA	
		XC	2.4	3.4				
V_{OH}	Output HIGH Voltage, Q_0–Q_3, Q_S	XM	2.4	3.4		V	I_{OH} = −2.0 mA	V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = −5.7 mA	
V_{OL}	Output LOW Voltage, Q_0–Q_3, Q_S	XM		0.25	0.4	V	I_{OL} = 8.0 mA	V_{CC} = MIN
		XC		0.35	0.5	V	I_{OL} = 16 mA	
V_{OL}	Output LOW Voltage, $\overline{ORE}$, $\overline{IRF}$	XM		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = MIN
		XC		0.35	0.5		I_{OL} = 8.0 mA	
I_{OZH}	Output Off HIGH Current Q_0–Q_3, Q_S				100	µA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2.0 V	
I_{OZL}	Output Off LOW Current Q_0–Q_3, Q_S				−100	µA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 2.0 V	
I_{IH}	Input HIGH Current			1.0	40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
I_{IL}	Input LOW Current, all except $\overline{OES}$, $\overline{MR}$				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
	Input LOW Current, $\overline{OES}$, $\overline{MR}$				−0.72			
I_{OS}	Output Short Circuit Current Q_0–Q_3, Q_S, $\overline{ORE}$, $\overline{OES}$		−30		−130	mA	V_{CC} = MAX, V_{OUT} = 0, (Note 3)	
I_{CC}	Supply Current	XM		150		mA	V_{CC} = MAX, Inputs Open	
		XC		150				

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: V_{CC} = 5.0 V, C_L = 15 pF, T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{PHL}	Propagation Delay, Negative-Going CP to $\overline{IRF}$ Output		28		ns	Stack not Full, PL LOW, Figures 11 and 12
t_{PLH}	Propagation Delay, Negative-Going $\overline{TTS}$ to $\overline{IRF}$		48		ns	
t_{PLH},	Propagation Delay, Negative-Going $\overline{CPSO}$ to Q_S Output		45		ns	$\overline{OES}$ LOW, TOP HIGH, Figures 13 and 14
t_{PHL}			30		ns	
t_{PLH},	Propagation Delay, Positive-Going TOP to Outputs Q_0 − Q_3		65		ns	$\overline{EO}$, $\overline{CPSO}$ LOW, Figure 15
t_{PHL}			40		ns	
t_{PHL}	Propagation Delay, Negative-Going $\overline{CPSO}$ to $\overline{ORE}$		30		ns	$\overline{OES}$ LOW, TOP HIGH, Figures 13 and 14
t_{PHL}	Propagation Delay, Negative-Going TOP to $\overline{ORE}$		35		ns	Parallel Output, $\overline{EO}$, $\overline{CPSO}$ LOW, Figure 15
t_{PLH}	Propagation Delay, Positive-Going TOP to $\overline{ORE}$		60			
t_{DFT}	Fall Through Time		2.5		µs	$\overline{TTS}$ Connected to $\overline{IRF}$ $\overline{TOS}$ Connected to $\overline{ORE}$ $\overline{IES}$, $\overline{OES}$, $\overline{EO}$, $\overline{CPSO}$ LOW, TOP HIGH, Figure 16
t_{PLH}	Propagation Delay, Negative-Going $\overline{TOS}$ to Positive-Going $\overline{ORE}$		60		ns	Data in stack, TOP HIGH, Figures 13 and 14

AC CHARACTERISTICS (Cont'd): V_{CC} = 5.0 V, C_L = 15 pF, T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{PHL}	Propagation Delay, Positive-Going PL to Negative-Going $\overline{IRF}$		30		ns	Stack not Full, Figures 17 and 18
t_{PLH}	Propagation Delay, Negative-Going PL to Positive-Going $\overline{IRF}$		30		ns	
t_{PLH}	Propagation Delay, Positive-Going $\overline{OES}$ to $\overline{ORE}$		26		ns	
t_{PLH}	Propagation Delay, Positive-Going $\overline{IES}$ to Positive-Going $\overline{IRF}$		30		ns	Figure 18
t_{PZL}, t_{PZH}	Propagation Delay, $\overline{OE}$ to Q_0, Q_1, Q_2, Q_3		10		ns	Propagation Delay Out of the High Impedance State
t_{PHZ}, t_{PLZ}	Propagation Delay, $\overline{OE}$ to Q_0, Q_1, Q_2, Q_3		10		ns	Propagation Delay Into the High Impedance State
t_{PZL}, t_{PZH}	Propagation Delay, Negative-Going $\overline{OES}$ to Q_S		13		ns	Propagation Delay Out of the High Impedance State
t_{PLZ}, t_{PHZ}	Propagation Delay, Negative-Going $\overline{OES}$ to Q_S		70		ns	Propagation Delay Into the High Impedance State
t_{AP}	Parallel Appearance Time, $\overline{ORE}$ to $Q_0 - Q_3$				ns	Time elapsed between $\overline{ORE}$ going HIGH and valid data appearing at output. Negative number indicates data available before $\overline{ORE}$ goes HIGH.
t_{AS}	Serial Appearance Time, $\overline{ORE}$ to Q_S		6.0		ns	

AC SET-UP REQUIREMENTS: V_{CC} = 5.0 V, C_L = 15 pF, T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{PWH}	$\overline{CPSI}$ Pulse Width (HIGH)				ns	Stack not full, PL LOW, Figures 11 and 12
t_{PWL}	$\overline{CPSI}$ Pulse Width (LOW)				ns	
t_{PWH}	PL Pulse Width (HIGH)				ns	Stack not full, Figures 17 and 18
t_{PWL}	$\overline{TTS}$ Pulse Width (LOW) Serial or Parallel Mode				ns	Stack not full, Figures 11, 12, 17, 18
t_{PWL}	$\overline{MR}$ Pulse Width (LOW)				ns	Figure 16
t_{PWH}	TOP Pulse Width (High)				ns	$\overline{CPSO}$ LOW, data available in stack, Figure 15
t_{PWL}	TOP Pulse Width (LOW)				ns	
t_{PWH}	$\overline{CPSO}$ Pulse Width (HIGH)				ns	TOP HIGH, data in stack, Figures 13 and 14
t_{PWL}	$\overline{CPSO}$ Pulse Width (LOW)				ns	
t_s	Set-up Time, D_S to Negative $\overline{CPSI}$				ns	PL LOW, Figures 11 and 12
t_h	Hold Time, D_S to $\overline{CPSI}$				ns	PL LOW, Figures 11 and 12
t_s	Set-up Time, $\overline{TTS}$ to $\overline{IRF}$ Serial or Parallel Mode				ns	Figures 11, 12, 17, 18
t_s	Set-up Time Negative-Going $\overline{ORE}$ to Negative-Going $\overline{TOS}$				ns	TOP HIGH, Figures 13 and 14
t_{rec}	Recovery Time $\overline{MR}$ to any Input				ns	Figure 16
t_s	Set-up Time, Negative-Going $\overline{IES}$ to $\overline{CPSI}$				ns	Figure 12
t_s	Set-up Time, Negative-Going $\overline{TTS}$ to $\overline{CPSI}$				ns	Figure 12
t_s	Set-up Time, Parallel Inputs to PL				ns	Length of time parallel inputs must be applied prior to rising edge of PL.
t_h	Hold Time, Parallel Inputs to PL				ns	Length of time parallel inputs must reamin applied after falling edge of PL.

Bipolar
Memory
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Memory

CHAPTER 8

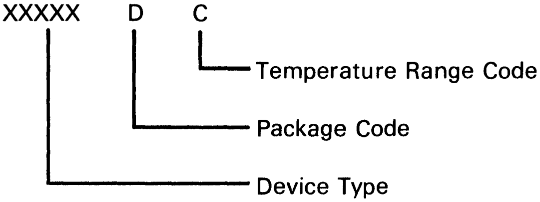
- Package Style
- Temperature Ranges
- Examples
- Device Identification/Marking Package Information
- Package Information
- Hi-Rel Processing
- Hi-Rel Processing Flows
- Package Outlines

ORDER AND PACKAGE INFORMATION

Fairchild bipolar memories may be ordered by using a simplified purchasing code where the package style and temperature range is defined as follows:

PACKAGE STYLE

D = Dual In-line – Ceramic (hermetic)
P = Dual In-line – Plastic
F = Flatpak



In order to accommodate varying die sizes and numbers of pins (16, 18, 24, etc.), a number of different package forms are required. The Package Information list on the following pages indicates the specific package codes currently used for each device type. The detailed package outline corresponding to each package code is shown at the end of this section.

TEMPERATURE RANGES

Two basic temperature grades are in common use: C = Commercial-Industrial, 0°C to +75°C; M = Military, −55°C to +125°C. Exact values and conditions are indicated on the data sheets.

EXAMPLES:

(a) 93415FM
This number code indicated a 93415 1024 x 1 RAM in a flatpak with military temperature rating.

(b) 93421DC
This number code indicates a 93421 256 x 1 RAM in a ceramic dual in-line package with commercial temperature rating.

(c) 93436PC
This number code indicates a 93436 512 x 4 PROM in a plastic package with a commercial temperature rating.

DEVICE IDENTIFICATION/MARKING

All Fairchild standard catalog bipolar memories will be marked as follows:

Device Type XX
Date Code

DEVICE	Military (M) −55°C to +125°C		DEVICE	Commercial (C)/Industrial 0°C to +75°C		
	Ceramic DIP (D)	Flatpak (F)		Ceramic DIP (D)	Plastic DIP (P)	Flatpak (F)
F10145A	-	-	F10145A	6B	9B	4L
F10405	-	-	F10405	6E	-	4B
F10410	-	-	F10410	6F	9B	4B
F10411	-	-	F10411	6F	9B	4B
F10414	-	-	F10414	6E	-	4B
F100414	-	-	F100414	6E	-	4B
F10415	-	-	F10415	6E	-	4B
F10415A	-	-	F10415A	6E	-	4B
F100415	-	-	F100415	6E	-	4B
F10416	-	-	F10416	6E	-	4B
F100416	-	-	F100416	6E	-	4B
F10470	-	-	F10470	7D	-	-
93410	6F	4B	93410	6F	9B	4B
93410A	-	-	93410A	6F	9B	4B
93411	6F	4B	93411	6F	9B	4B
93411A	-	-	93411A	6F	9B	4B
93L412	8T	4R	93L412	8T	-	4R
93412	8T	4R	93412	8T	-	4R
93L415	6J	4B	93L415	6J	9B	4B
93415	6J	4B	93415	6J	9B	4B
93415A	-	-	93415A	6J	9B	4B
93417	6E, 6J	3D, 4B	93417	6E, 6J	9B	3D, 4B
93419	7Y	-	93419	7Y	-	-
93L420	6F	4B	93L420	6F	9B	4B
93L421	6F	4B	93L421	6F	9B	4B
93421	6F	4B	93421	6F	9B	4B
93421A	-	-	93421A	6F	9B	4B
93L422	8T	4R	93L422	8T	-	4R
93422	8T	4R	93422	8T	-	4R
93L425	6J	4B	93L425	6J	9B	4B
93425	6J	4B	93425	6J	9B	4B
93425A	-	-	93425A	6J	9B	4B
93427	6E, 6J	3D, 4B	93427	6E, 6J	9B	3D, 4B
93431	6E, 6J	3D, 4B	93431	6E, 6J	9B	3D, 4B
93432	6M, 6N	4R	93442	6M, 6N	9N	4R
93436	6E, 6J	3D, 4B	93436	6E, 6J	9B	3D, 4B
93438	6M, 6N	4R	93438	6M, 6N	9N	4R
93441	6E, 6J	3D, 4B	93441	6E, 6J	9B	3D, 4B
93442	6M, 6N	4R	93442	6M, 6N	9N	4R
93446	6E, 6J	3D, 4B	93446	6E, 6J	9B	3D, 4B
93448	6M, 6N	4R	93448	6M, 6N	9N	4R
93450	6M, 6N	-	93450	6M, 6N	9N	4R
93451	6M, 6N	-	93451	6M, 6N	9N	4R
93452	7D, 4N	-	93452	7D, 4N	9M	-
93453	7D, 4N	-	93453	7D, 4N	9M	-
93454	6M, 6N	4R	93454	6M, 6N	9N	4R
93457	6E, 6J	3D, 4B	93457	6E, 6J	9B	3D, 4B
93458	7Y	-	93458	7Y	-	-
93459	7Y	-	93459	7Y	-	-
93464	6M	4R	93464	6E	9N	4R
93467	6E, 6J	3D, 4B	93467	6E, 6J	9B	3D, 4B
93470	7D	-	93470	7D	9M	-
93471	7D	-	93471	7D	9M	-
93481	-	-	93481	6E	9B	4B
93481A	-	-	93481A	6E	9B	4B
9403	6Q	4M	9403	6Q	9U	4M
9406	6Q	4M	9406	6Q	9U	4M
9410	7D		9410	7D	9M	-
9423	6Q	4M	9423	6Q	9U	4M

HI-REL PROCESSING

Fairchild's Bipolar Memory/ECL Products Division offers HI-REL processing for both military and commercial customers. Fairchild's UNIQUE 38510 program provides military customers an opportunity to purchase state-of-the-art LSI memory circuits processed to the latest version of MIL-M-38510/MIL-STD-883. The UNIQUE 38510 program is available for processing to specific customer drawings or may be ordered directly from the QB or QC processing flow.

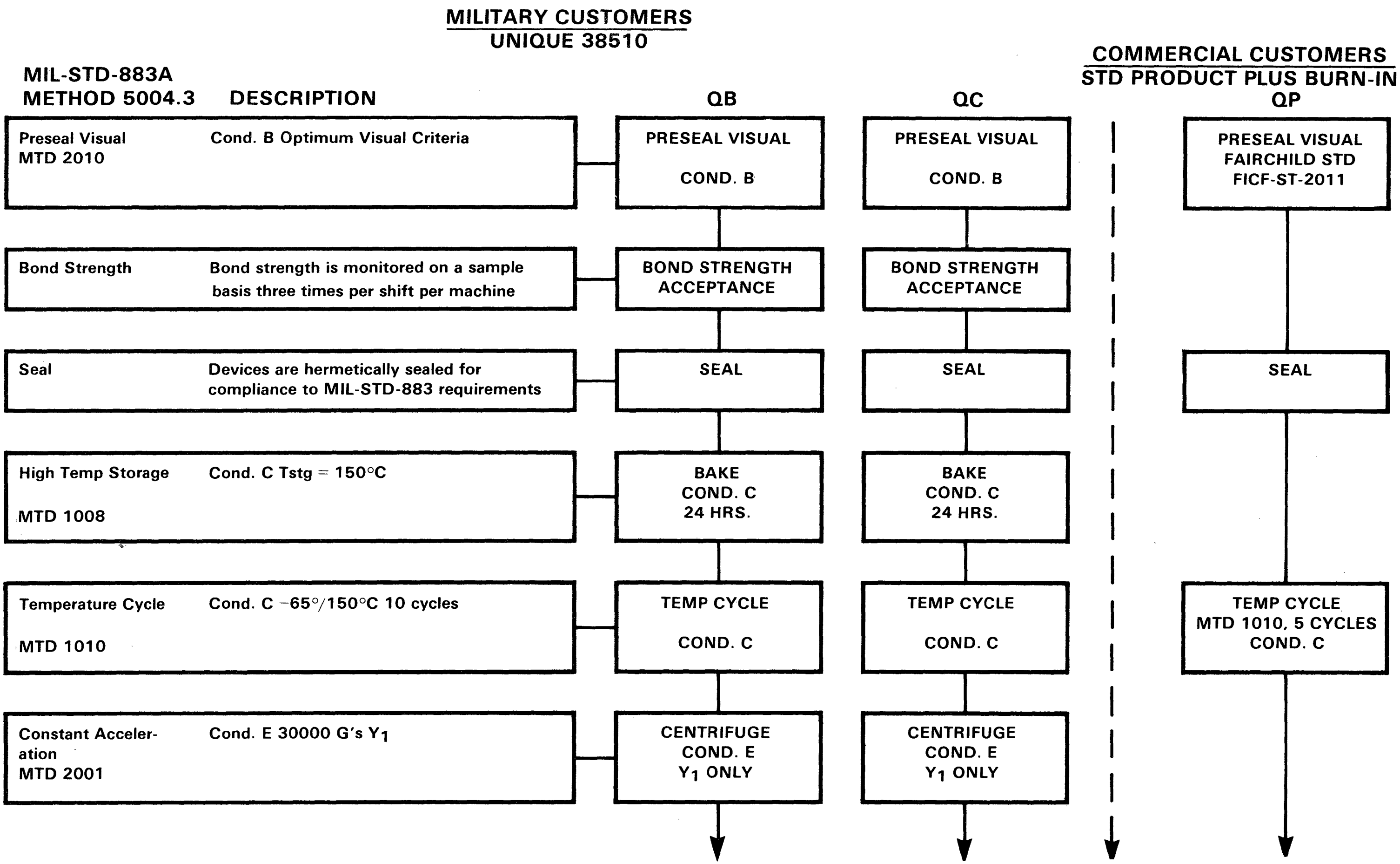
For commercial customers, the reliability of standard product can be improved by requiring burn-in on all devices with the QP process flow.

All HI-REL TTL RAMs and ROM/PROMs may be purchased in dual in-line and flatpak ceramic packages, with the exception of the 93419 which is only available in the dual in-line package.

In addition to the HI-REL processing flows shown, these additional HI-REL steps are available upon request:

- State-side assembly
- Radiography MTD 2012
- SEM Analysis
- PROM Programming (single or multiple pulse)
- Special lead form
- Read and record critical parameters before and after burn-in

HI-REL PROCESSING FLOWS

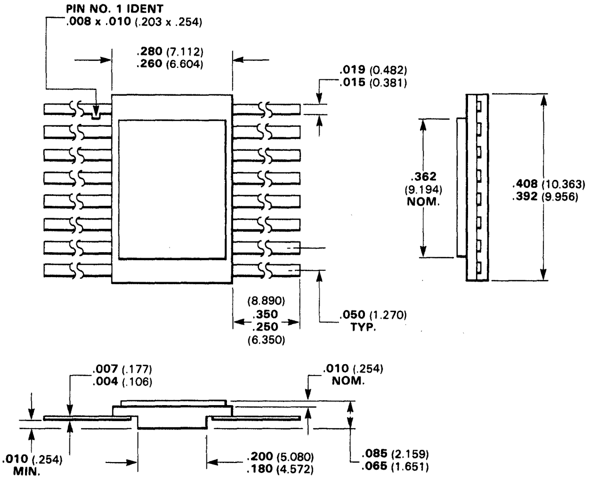


MIL-STD-883A METHOD 5004.3	DESCRIPTION	MILITARY CUSTOMERS UNIQUE 38510 QB	MILITARY CUSTOMERS UNIQUE 38510 QC	COMMERCIAL CUSTOMERS STD PRODUCT PLUS BURN-IN QP
Preseal Visual MTD 2010	Cond. B Optimum Visual Criteria	PRESEAL VISUAL COND. B	PRESEAL VISUAL COND. B	PRESEAL VISUAL FAIRCHILD STD FICF-ST-2011
Bond Strength	Bond strength is monitored on a sample basis three times per shift per machine	BOND STRENGTH ACCEPTANCE	BOND STRENGTH ACCEPTANCE	
Seal	Devices are hermetically sealed for compliance to MIL-STD-883 requirements	SEAL	SEAL	SEAL
High Temp Storage MTD 1008	Cond. C Tstg = 150°C	BAKE COND. C 24 HRS.	BAKE COND. C 24 HRS.	
Temperature Cycle MTD 1010	Cond. C −65°/150°C 10 cycles	TEMP CYCLE COND. C	TEMP CYCLE COND. C	TEMP CYCLE MTD 1010, 5 CYCLES COND. C
Constant Acceleration MTD 2001	Cond. E 30000 G's Y_1	CENTRIFUGE COND. E Y_1 ONLY	CENTRIFUGE COND. E Y_1 ONLY	

Hermetic Seal MTD 1014	Cond. A Fine-Helium 5x10^{-8} cc/sec Cond. B Fine-Radiflo 5x10^{-8} cc/sec Cond. C1 Gross-FC43/Hot 10^{-5} cc/sec Cond. C2 Gross-FC78/Vacuum 10^{-3} cc/sec	HERMETICITY COND. A/B COND. C2	HERMETICITY COND. A/B COND. C2	HERMETICITY COND. C1
Pre Burn-in Electrical 5004	25°C DC electrical testing to remove rejects prior to submission to burn-in screen	OPTIONAL PRE B/I ELECT 25°C DC		
Burn-in Screen MTD 1015		BURN-IN 168 HRS @ 125°C		BURN-IN 160 HRS @ 125°C
Post Burn-in Electrical 5004	Post Burn-in electrical screening to cull out devices which failed as a result of burn-in.	POST B/I ELECT 25°C DC +125°C DC −55°C DC 25°C AC 25°C FUNCTION	FINAL ELECT 25°C DC 25°C FUNCTION	FINAL ELECT 25°C DC 25°C FUNCTION
Quality Conformance Inspection MTD 5005	Group A: Electrical Characteristics Group B: Package oriented Tests Group C: Die-related Tests Group D: Package Tests	QUALITY CONFORMANCE GP A,B,C,D	QUALITY CONFORMANCE GP A,B,C,D	QA ACCEPTANCE GP A,B,C
External Visual MTD 2009	3X, 10X magnification: Verify dimensions, configuration, lead structure, marking and workmanship	EXTERNAL VISUAL MTD 2009	EXTERNAL VISUAL MTD 2009	EXTERNAL VISUAL 100%

PACKAGE OUTLINES

16-Pin Flatpak 3D



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

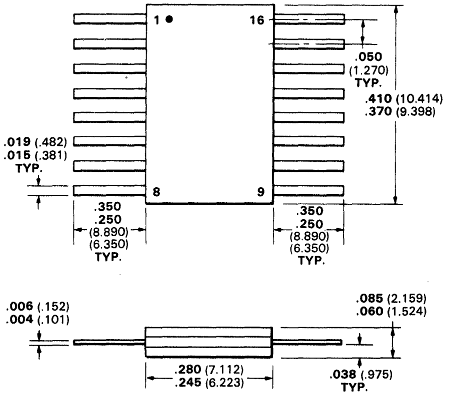
Pins are Ni Au plated kovar

Cap is kovar

Base is Al_2O_3

Package weight is 0.6 gram

16-Pin Cerpak 4B



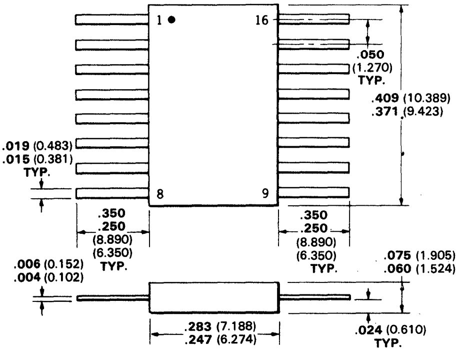
NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are tin-plated kovar or alloy 42

Package weight is 0.4 gram

16-Pin Cerpak 4L



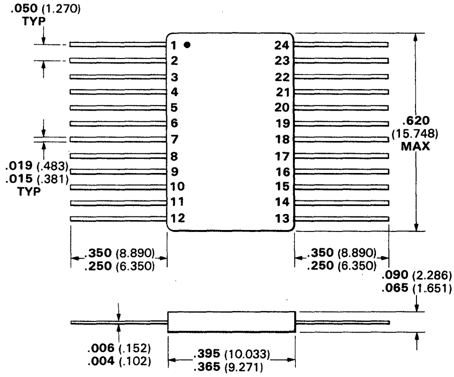
NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are tin-plated alloy 42

Package weight is 0.4 gram

24-Pin Cerpak 4M



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

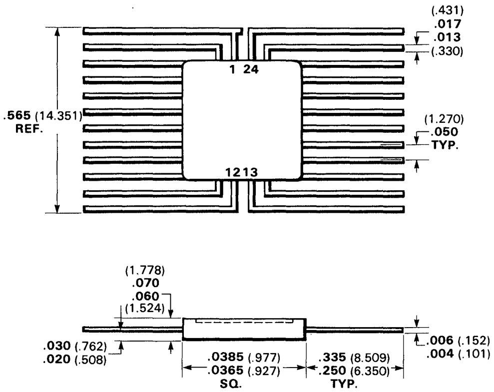
Pins are tin-plated alloy 42

Package weight is 0.8 gram

Pin numbers for reference only

PACKAGE OUTLINES

24-Pin Flatpak 4R



NOTES:

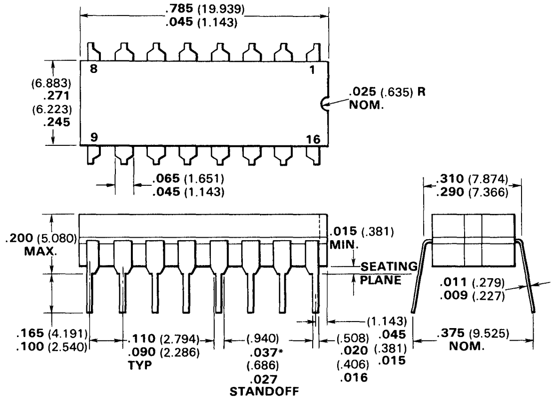
All dimensions in inches (bold) and millimeters (parentheses)

Metal cap and base

Pins are gold-plated kovar

Package weight is 0.6 gram

16-Pin Ceramic Dual In-line 6B



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are tin-plated alloy 42

Cap and Base is Al_2O_3

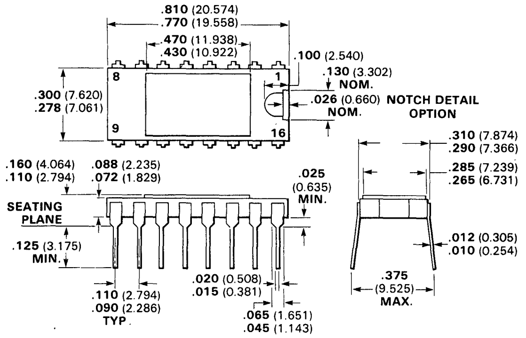
Pins are intended for insertion in hole rows on .300" (7.62) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal you practice for .020" (0.508) diameter pin

Package weight is 2.0 grams

16-Pin Ceramic Dual In-line (Metal Cap) 6E



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are gold-plated nickel alloy 42

Base is Al_2O_3

Cap is gold-plated kovar

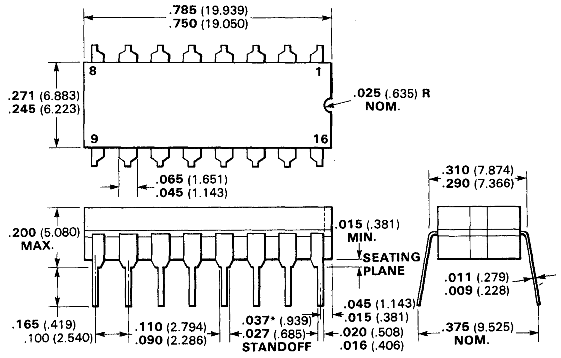
Pins are intended for insertion in hole rows on .300" (7.62) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal you practice for .020" (0.508) diameter pin

Package weight is 2.0 grams

16-Pin Ceramic Dual In-line 6F



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are tin-plated alloy 42

Cap and Base is Al_2O_3

Pins are intended for insertion in hole rows on .300" (7.62) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

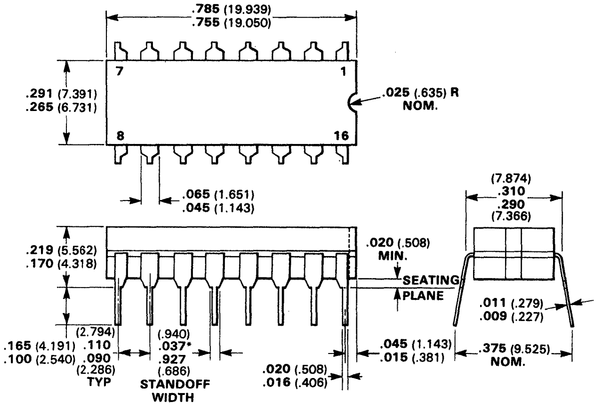
Board-drilling dimensions should equal you practice for .020" (0.508) diameter pin

Package weight is 2.0 grams

Pin numbers for reference only

PACKAGE OUTLINES

16-Pin Ceramic Dual In-line 6J



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are tin-plated alloy 42

Pins are intended for insertion in hole rows on .300" (7.62) centers

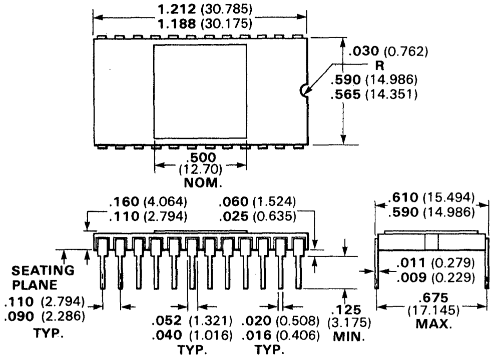
They are purposely shipped with positive misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for .020" (0.51) diameter pin

Package weight is 2.2 grams

*The .037/.027 dimensions does not apply to the corner pins

24-Pin Dual In-line Side Braze Package (BPM) 6M



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Cap is gold-plated kovar

Base is ceramic

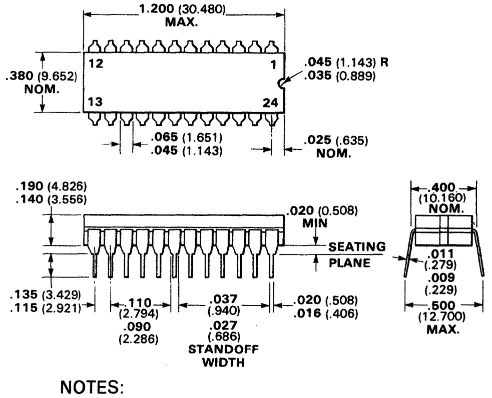
Pins are intended for insertion in hole rows on .600" (15.24) centers

Board-drilling dimensions should equal your practice for .020" (0.51) diameter pin

Pins are nickel-gold plated kovar

Package weight is 4.0 grams

24-Pin Ceramic Dual In-line 6Q



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

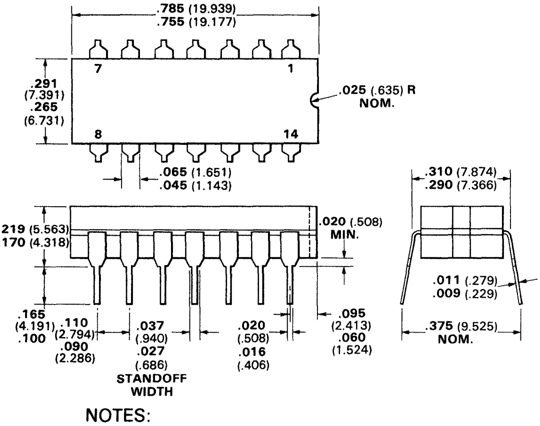
Pins are intended for insertion in hole rows on .400" (10.16) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling should equal your practice for .020" (0.51) diameter pin

Pins are tin-plated alloy 42

14-Pin Ceramic Dual In-line 7A



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are intended for insertion in hole rows on .300" (7.62) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for .020" (0.51) diameter pin

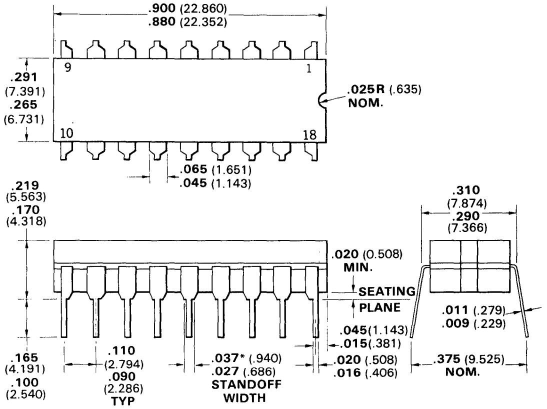
Pins are tin-plated alloy 42

Package weight is 2.0 grams

Pin numbers for reference only

PACKAGE OUTLINES

18-Pin Ceramic Dual In-line 7D



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are tin-plated kovar

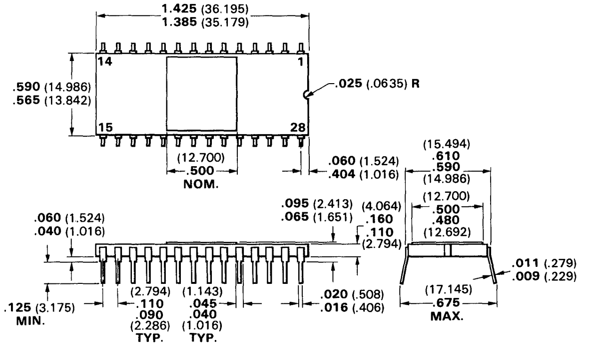
Pins are intended for insertion in hole rows on .300" (7.62) centers

They are purposely shipped with positive misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for .020" (0.51) diameter pin

*The .037/.027 dimensions does not apply to the corner pins

28-Pin Ceramic Dual In-line 7Y (Metal Cap)



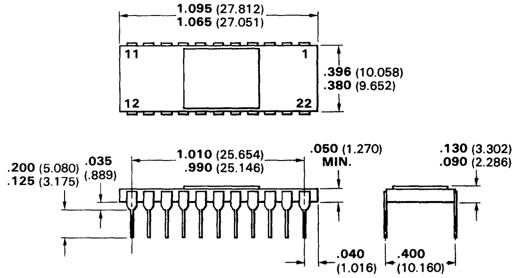
NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are gold-plated kovar

Package weight is 4.0 grams

22-Pin Ceramic Dual In-line 8T (Metal Cap)



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are intended for insertion in hole rows on .400" (10.16) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

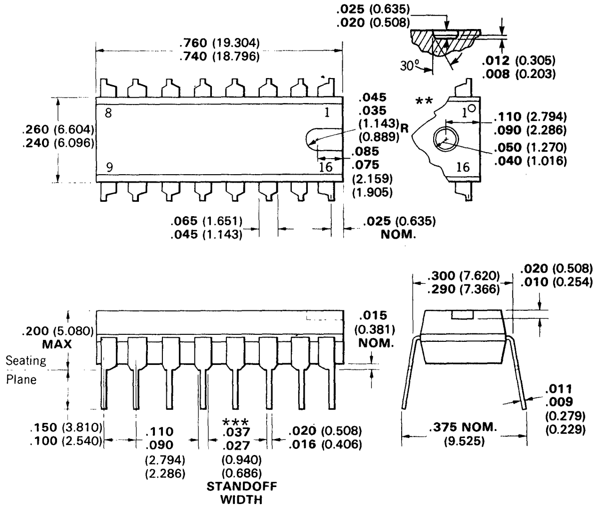
Board-drilling should equal your practice for .020" (0.51) diameter pin

Pins are gold-plated kovar

Pin numbers for reference only

16-Pin Plastic Dual In-line

9B



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are tin-plated alloy 42

*Package material varies depending on the product line

Pins are intended for insertion in hole rows on .300" (7.62) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for .020" (0.508) diameter pin

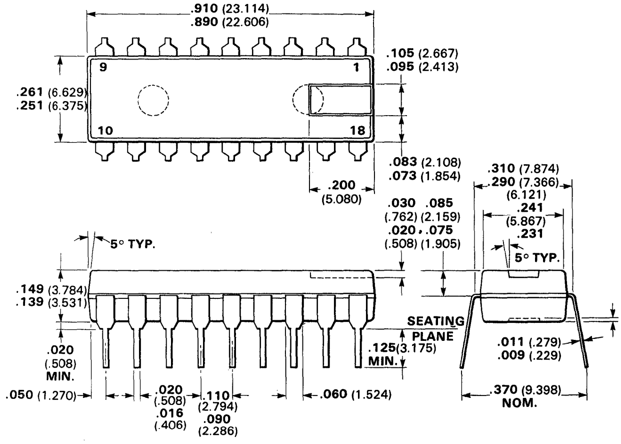
**Notch or ejector hole varies depending on the product line

***The .037/.027 dimension does not apply to the corner pins

Package weight is 0.9 gram

18-Pin Plastic Dual In-line

9M



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are intended for insertion in hole rows on .300" (7.62) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for .020" (0.51) diameter pin

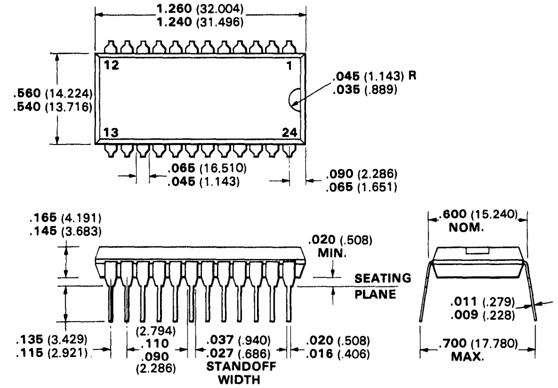
Pins are tin-plated kovar or alloy 42

Pin numbers for reference only

PACKAGE OUTLINES

24-Pin Plastic Dual In-line

9N



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are intended for insertion in hole rows on .600" (15.24) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

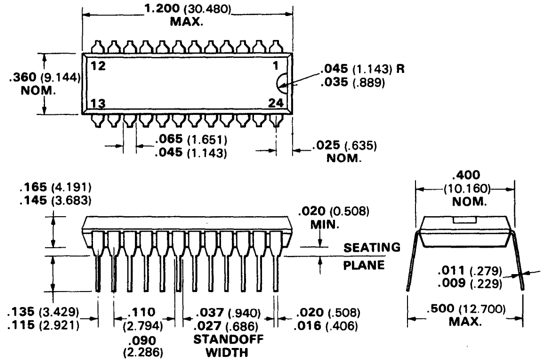
Board-drilling dimensions should equal your practice for .020" (0.508) diameter pin

Pins are tin-plated kovar or alloy 42

Package weight is 2.7 grams

24-Pin Plastic Dual In-line

9U



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are intended for insertion in hole rows on .400" (10.16) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling should equal your practice for .020" (0.51) diameter pin

Pins are tin-plated alloy 42

Pin numbers for reference only

Bipolar Memory Bipolar Memory

Bipolar
Memory
Bipolar
Memory

CHAPTER 9

- Fairchild Field Sales Offices, Representatives and Distributors

FAIRCHILD FRANCHISED DISTRIBUTORS
UNITED STATES AND CANADA

ALABAMA
HALLMARK ELECTRONICS
4739 Commercial Drive
Huntsville, Alabama 35805
Tel: 205-837-8700 TWX: 810-726-2187

HAMILTON/AVNET ELECTRONICS
805 Oster Drive, N.W.
Huntsville, Alabama 35805
Tel: 205-533-1170
Telex: None — use HAMAVLECB DAL 73-0511
(Regional Hq. in Dallas, Texas)

ARIZONA
HAMILTON/AVNET ELECTRONICS
2615 S. 21st Street
Phoenix, Arizona 85034
Tel: 602-275-7851 TWX: 910-951-1535

LIBERTY ELECTRONICS/ARIZONA
3130 N. 27th Avenue
Phoenix, Arizona 85016
Tel: 602-257-1272 TWX: 910-951-4282

MIRCO ELECTRONIC DISTRIBUTORS
2005 West Peoria Avenue
Phoenix, Arizona 85029
Tel: 602-944-2281
Telex: 668-403

STERLING ELECTRONICS
P.O. Drawer 20867 (zip code 85036)
2001 E. University Drive
Phoenix, Arizona 85034
Tel: 602-258-4531 Telex: 667317

CALIFORNIA
AVNET ELECTRONICS
350 McCormick Avenue
Costa Mesa, California 92626
Tel: 714-754-6111 (Orange County)
213-558-2345 (Los Angeles)
TWX: 910-595-1928

BELL INDUSTRIES
Electronic Distributor Division
1161 N. Fair Oaks Avenue
Sunnyvale, California 94086
Tel: 408-734-8570 TWX: 910-339-9378

ELMAR ELECTRONICS
2288 Charleston Rd.
Mountain View, California 94042
Tel: 415-961-3611 TWX: 910-379-6437

G.S. MARSHALL COMPANY
9674 Telstar Avenue
El Monte, California 91731
Tel: 213-686-0141 TWX: 910-587-1565

G.S. MARSHALL COMPANY
17975 Skypark Blvd.
Irvine, California 92707
Tel: 714-556-6400

G.S. MARSHALL COMPANY
8057 Raytheon Rd., Suite 1
San Diego, California 92111
Tel: 714-278-6350 TWX: 910-335-1191

HAMILTON ELECTRO SALES
10912 W. Washington Blvd.
Culver City, California 90230
Tel: 213-558-2121 TWX: 910-340-6364

HAMILTON/AVNET ELECTRONICS
575 E. Middlefield Road
Mountain View, California 94040
Tel: 415-961-7000 TWX: 910-379-6486

HAMILTON/AVNET ELECTRONICS
8917 Complex Drive
San Diego, California 92123
Tel: 714-279-2421
Telex: HAMAVELEC SDG 69-5415

LIBERTY ELECTRONICS
124 Maryland Street
El Segundo, California 90245
Tel: 213-322-8100 TWX: 910-348-7111

LIBERTY ELECTRONICS/SAN DIEGO
8248 Mercury Court
San Diego, California 92111
Tel: 714-565-9171 TWX: 910-335-1590

COLORADO
CENTURY ELECTRONICS
8155 West 48th Avenue
Wheatridge, Colorado 80033
Tel: 303-424-1985 TWX: 910-938-0393

CRAMER ELECTRONICS
5465 East Evans Place at Hudson
Denver, Colorado 80222
Tel: 303/758-2100

ELMAR ELECTRONICS
6777 E. 50th Avenue
Commerce City, Colorado 80022
Tel: 303-287-9611 TWX: 910-936-0770

G.S. MARSHALL COMPANY
5633 Kendall Court
Arvada, Colorado 80002
Tel: 303-423-9670 TWX: 910-938-2902

HAMILTON/AVNET ELECTRONICS
5921 N. Broadway
Denver, Colorado 80216
Tel: 303-534-1212 TWX: 910-931-0510

CONNECTICUT
CRAMER ELECTRONICS
35 Dodge Avenue
Wharton Brook Industrial Center
North Haven, Connecticut 06473
Tel: 203-239-5641

HAMILTON/AVNET ELECTRONICS
643 Danbury Road
Georgetown, Connecticut 06829
Tel: 203-762-0361
TWX: None — use 710-897-1405
(Regional Hq. in Mt. Laurel, N.J.)

HARVEY ELECTRONICS
112 Main Street
Norwalk, Connecticut 06851
Tel: 203-853-1515

SCHWEBER ELECTRONICS
Finance Drive
Commerce Industrial Park
Danbury, Connecticut 06810
Tel: 203-792-3500

FLORIDA
CRAMER ELECTRONICS
4035 N. 29th Avenue
Hollywood, Florida 33020
Tel: 305/923-8181

CRAMER ELECTRONICS
345 North Graham Avenue
Orlando, Florida 32814
Tel: 305-894-1511

HALLMARK ELECTRONICS
1302 W. McNab Road
Ft. Lauderdale, Florida 33309
Tel: 305-971-9280 TWX: 510-956-3092

HALLMARK ELECTRONICS
7233 Lake Ellenor Drive
Orlando, Florida 32809
Tel: 305-855-4020 TWX: 810-850-0183

HAMILTON/AVNET ELECTRONICS
6800 N.W. 20th Avenue
Ft. Lauderdale, Florida 33309
Tel: 305-971-2900 TWX: 510-954-9808

SCHWEBER ELECTRONICS
2830 North 28th Terrace
Hollywood, Florida 33020
Tel: 305-927-0511 TWX: 510-954-0304

GEORGIA
HAMILTON/AVNET ELECTRONICS
6700 Interstate 85 Access Road, Suite 1E
Norcross, Ga. 30071
Tel: 404-448-0800
Telex: None — use HAMAVLECB DAL 73 0511
(Regional Hq. in Dallas, Texas)

LYKES ELECTRONICS CORP.
6447 Atlantic Blvd.
Norcross, Georgia 30071
Tel: 404-449-9400

ILLINOIS
HALLMARK ELECTRONICS, INC.
180 Crossen Avenue
Elk Grove Village, Illinois 60007
Tel 312 437 8800

HAMILTON/AVNET ELECTRONICS
3901 N. 25th Avenue
Schiller Park, Illinois 60176
Tel: 312-678-6310 TWX: 910-227-0060

KIERULFF ELECTRONICS
85 Gordon Street
Elk Grove Village, Illinois 60007
Tel: 312-640-0200 TWX: 910-227-3166

SCHWEBER ELECTRONICS, INC.
1275 Brummel Avenue
Elk Grove Village, Ill. 60007
Tel: 312-593-2740 TWX: 910-222-3453

SEMICONDUCTOR SPECIALISTS, INC.
(mailing address)
O'Hare International Airport
P.O. Box 66125
Chicago, Illinois 60666

(shipping address)
195 Spangler Avenue
Elmhurst Industrial Park
Elmhurst, Illinois 60126
Tel: 312-279-1000 TWX: 910-254-0169

INDIANA
GRAHAM ELECTRONICS SUPPLY, INC.
133 So. Pennsylvania Street
Indianapolis, Indiana 46204
Tel: 317-634-8486 TWX: 810-341-3481

PIONEER INDIANA ELECTRONICS, INC.
6408 Castleplace Drive
Indianapolis, Indiana 46250
Tel: 317-849-7300 TWX: 810-260-1794

KANSAS
HALLMARK ELECTRONICS, INC.
11870 West 91st Street
Shawnee Mission, Kansas 66214
Tel: 913-888-4746

HAMILTON/AVNET ELECTRONICS
37 Lenexa Industrial Center
9900 Pflumm Road
Lenexa, Kansas 66215
Tel: 913-888-8900
Telex: None — use HAMAVLECB DAL 73-0511
(Regional Hq. in Dallas, Texas)

LOUISIANA
STERLING ELECTRONICS CORP.
4613 Fairfield
Metairie, Louisiana 70002
Tel: 504-887-7610
Telex: STERLE LEC MRIE 58-328

MARYLAND
HALLMARK ELECTRONICS, INC
6655 Amberton Drive
Baltimore, Maryland 21227
Tel, 301-796-9300

HAMILTON/AVNET ELECTRONICS
(mailing address)
Friendship International Airport
P O. Box 8647
Baltimore, Maryland 21240

7255 Standard Drive (shipping address)
Hanover, Maryland 21076
Tel: 301-796-5000 TWX: 710-862-1861
Telex: HAMAVLECA HNVE 87-968

PIONEER WASHINGTON ELECTRONICS, INC.
9100 Gaither Road
Gaithersburg, Maryland 20760
Tel: 301-948-0710 TWX. 710-828-9784

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5640 Fisher Lane
Rockville, Maryland 20852
Tel: 301-881-2970 TWX. 710-828-0536

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CRAMER ELECTRONICS
85 Wells Avenue
Newton Centre, Massachusetts 02159
Tel: 617-964-4000

GERBER ELECTRONICS
852 Providence Highway
U.S. Route 1
Dedham, Massachusetts 02026
Tel: 617-329-2400

HAMILTON/AVNET ELECTRONICS
100 E. Commerce Way
Woburn, Massachusetts 01801
Tel: 617-933-8000 TWX: 710-332-1201

HARVEY ELECTRONICS
44 Hartwell Ave.
Lexington, Massachusetts 02173
Tel: 617-861-9200 TWX: 710-326-6617

SCHWEBER ELECTRONICS
213 Third Avenue
Waltham, Massachusetts 02154
Tel: 617-890-8484

FAIRCHILD FRANCHISED DISTRIBUTORS (Cont'd)
UNITED STATES AND CANADA

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HAMILTON/AVNET ELECTRONICS
12870 Farmington Rd.
Livonia, Michigan 48150
Tel: 313-522-4700 TWX: 810-242-8775

PIONEER/DETROIT
13485 Stamford
Livonia, Michigan 48150
Tel: 313-525-1800

SCHWEBER ELECTRONICS
86 Executive Drive
Troy, Michigan 48084
Tel: 313-583-9242

SHERIDAN SALES CO.
24543 Indoplex Drive (P.O. Box 529)
Farmington, Mich. 48024
Tel: 313-477-3800

MINNESOTA

HAMILTON/AVNET ELECTRONICS
7683 Washington Ave. South
Edina, Minnesota 55435
Tel: 612-941-3801
TWX: None — use 910-227-0060
(Regional Hq. in Chicago, Ill.)

SCHWEBER ELECTRONICS
7402 Washington Ave. South
Eden Prairie, Minnesota 55343
Tel: 612-941-5280

SEMICONDUCTOR SPECIALISTS, INC.
8030 Cedar Avenue South
Minneapolis, Minnesota 55420
Tel: 612-854-8841 TWX: 910-576-2812

MISSOURI

HALLMARK ELECTRONICS, INC
13789 Rider Trail
Earth City, Missouri 63045
Tel 314-291-5350

HAMILTON/AVNET ELECTRONICS
364 Brookes Lane
Hazelwood, Missouri 63042
Tel: 314-731-1144 TWX: 910-762-0606

SEMICONDUCTOR SPECIALISTS, INC.
3805 N. Oak Trafficway
Kansas City, Mo. 64116
Tel: 816-452-3900 TWX: 910-771-2114

NEW JERSEY

HAMILTON/AVNET ELECTRONICS
218 Little Falls Road
Cedar Grove, New Jersey 07009
Tel: 201-239-0800 TWX: 710-994-5787

HAMILTON/AVNET ELECTRONICS
113 Gaither Drive
East Gate Industrial Park
Mt. Laurel, N.J. 08057
Tel: 609-234-2133 TWX: 710-897-1405

SCHWEBER ELECTRONICS
43 Belmont Drive
Somerset, N.J. 08873
Tel: 201-469-6008 TWX: 710-480-4733

STERLING ELECTRONICS
774 Pfeiffer Blvd.
Perth Amboy, N.J. 08861
Tel: 201-442-8000 Telex: 138-679

WILSHIRE ELECTRONICS
855 Industrial Highway, Unit #5
Cinnaninson, New Jersey 08077
Tel: 215-627-1920

WILSHIRE ELECTRONICS
1111 Paulison Avenue
Clifton, New Jersey 07011
Tel: 201-365-2600 TWX: 710-989-7052

NEW MEXICO

CENTURY ELECTRONICS
121 Elizabeth, N.E.
Albuquerque, New Mexico 87123
Tel: 505-292-2700 TWX: 910-989-0625

HAMILTON/AVNET ELECTRONICS
2450 Baylor Dr. S.E.
Albuquerque, New Mexico 87119
Tel: 505-765-1500
TWX: None — use 910-379-6486
(Regional Hq. in Mt. View, Ca.)

NEW YORK

CRAMER ELECTRONICS
129 Oser Avenue
Hauppauge, N.Y. 11787
Tel: 516/231-5682

CRAMER ELECTRONICS
6716 Joy Road
E. Syracuse, N.Y. 13057
Tel: 315/437-6671

COMPONENTS PLUS, INC.
40 Oser Avenue
Hauppauge, L.I., New York 11787
Tel: 516-231-9200 TWX: 510-227-9869

HAMILTON/AVNET ELECTRONICS
167 Clay Road
Rochester, New York 14623
Tel: 716-442-7820
TWX: None — use 710-332-1201
(Regional Hq. in Burlington, Mass.)

HAMILTON/AVNET ELECTRONICS
6500 Joy Road
E. Syracuse, New York 13057
Tel: 315-437-2642 TWX: 710-541-0959

HAMILTON/AVNET ELECTRONICS
70 State Street
Westbury, L.I., New York 11590
Tel: 516-333-5800 TWX: 510-222-8237

ROCHESTER RADIO SUPPLY CO., INC.
140 W. Main Street
(P.O. Box 1971)
Rochester, New York 14603
Tel: 716-454-7800

SCHWEBER ELECTRONICS
Jericho Turnpike
Westbury, L.I., New York 11590
Tel: 516-334-7474 TWX: 510-222-3660

SCHWEBER ELECTRONICS, INC.
2 Town Line Circle
Rochester, New York 14623
Tel: 716-461-4000

SEMICONDUCTOR CONCEPTS
145 Oser Ave.
Hauppauge, L.I., New York 11787
Tel: 516-273-1234 TWX: 510-227-6232

SUMMIT DISTRIBUTORS, INC.
916 Main Street
Buffalo, New York 14202
Tel: 716-884-3450 TWX: 710-522-1692

NORTH CAROLINA

CRAMER ELECTRONICS
938 Burke Street
Winston Salem, N.C. 27102
Tel: 919/725-8711

HALLMARK ELECTRONICS
1208 Front Street, Bldg K
Raleigh, North Carolina 27609
Tel 919-832-4465 TWX 510-928 1831

KIRKMAN ELECTRONICS, INC.
901 W. Second Street
Winston-Salem, North Carolina 27108
Tel: 919-722-9131

PIONEER/CAROLINA ELECTRONICS
2906 Baltic Avenue
Greensboro, North Carolina 27406
Tel: 919-273-4441

OHIO

HAMILTON/AVNET ELECTRONICS
761 Beta Drive, Suite "E"
Cleveland, Ohio 44143
Tel: 216-461-1400
TWX: None — use 910-227-0060
(Regional Hq. in Chicago, Ill.)

HAMILTON/AVNET ELECTRONICS
118 Westpark Road
Dayton, Ohio 45459
Tel: 513-433-0610 TWX: 810-450-2531

PIONEER/CLEVELAND
4800 East 131st Street
Cleveland, Ohio 44105
Tel: 216-587-3600

PIONEER/DAYTON
1900 Troy Street
Dayton, Ohio 45404
Tel: 513-236-9900 TWX: 810-459-1622

SCHWEBER ELECTRONICS
23880 Commerce Park Road
Beachwood, Ohio 44122
Tel: 216-464-2970 TWX: 810-427-9441

SHERIDAN SALES COMPANY
23224 Commerce Park Road
Beachwood Ohio 44122
Tel: 216-831-0130 TWX: 810-427-2957

SHERIDAN SALES CO.
(mailing address)
P.O. Box 37826
Cincinnati, Ohio 45222

(shipping address)
10 Knollcrest Drive
Reading, Ohio 45237
Tel: 513-761-5432 TWX: 810-461-2670

OKLAHOMA

HALLMARK ELECTRONICS
4846 South 83rd East Avenue
Tulsa, Oklahoma 74145
Tel: 918-835-8458 TWX: 910-845-2290

PENNSYLVANIA

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