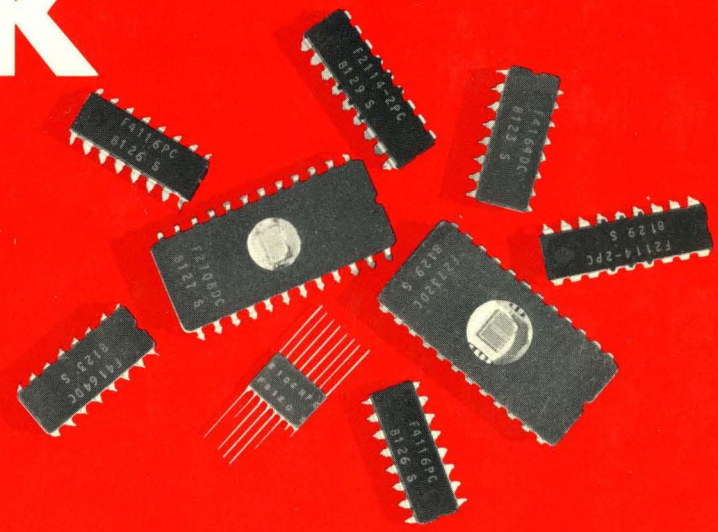
MOS MEMORY DATA BOOK



FAIRCHILD

A Schlumberger Company

MOS MEMORY DATA BOOK

464 Ellis Street • Mountain View, California 94042
415/962-5011 • TWX 910-379-6435

FAIRCHILD
A Schlumberger Company

Introduction

This data book presents a complete technical description of Fairchild's MOS Memory product line (excluding Read-Only Memories). The package outlines, electrical behavior, and ordering information are all included for this broad line of LSI and VLSI devices, manufactured using proven Isoplanar MOS processing techniques.

Complete technical data and ordering information on MOS ROMs can be obtained from Fairchild's Microprocessor Products Group.

Section 1 Product Index and Selection Guides
Handy tabulation of device numbers to assist in locating appropriate technical data.

Section 2 MOS Memory Technology Overview
Basic treatise covering the nature and history of MOS technology.

Section 3 RAM Data Sheets
Complete technical data on static and dynamic random access memories.

Section 4 EPROM Data Sheets
Complete technical data on UV EPROMs.

Section 5 Serial Memory Data Sheets
Complete technical data on static shift registers (including FIFOs).

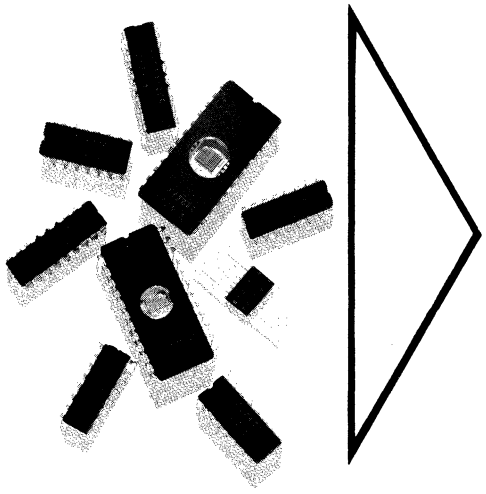
Section 6 Special Function Data Sheets
Complete technical data on several useful random logic devices.

Section 7 Extended Temperature Range Data Sheets
Complete technical data for extended temperature range operation of selected MOS devices.

Section 8 Ordering Information and Package Outlines
Detailed package drawings and ordering code information for standard parts, as well as Matrix VI and Unique 38510.

Section 9 Sales Offices, Representatives and Distributor Locations

Table of Contents



Section 1
Product Index and Selection Guides

Product Index

Random Access Memories

Organization	Part No.	Description	Access Time (ns)	Max Power Dissipation (mW)	Power Supply (V)	No. of Pins	Technology	Temperature Range (Note 1)	Package (Note 2)	Page No.
1024 x 1	2102-H	1K Static RAM	250	290	+5	16	NMOS	C,L,M	D,P,F	3-3, 7-3
	2102-F		350							3-3, 7-3
	2102-1		450							3-3, 7-3
	2102-2		650							3-3, 7-3
	2102L-H	1K Low-power Static RAM	250	160	+5	16	NMOS	C,L,M	D,P,F	3-3, 7-3
	2102L-F		350							3-3, 7-3
	2102L-1		450							3-3, 7-3
	2102L-2		650							3-3, 7-3
	21L02-H	1K Static RAM w/Power Down	250	160/25	+5	16	NMOS	C, L	D,P,F	3-3
	21L02-F		350							3-3
	21L02-1		450							3-3
	21L02-2		650							3-3
1024 x 4	F2114-2	4K Static RAM	200	530	+5	18	NMOS	C,M	D,P	3-8, 7-6
	F2114-3		300							3-8, 7-6
	F2114		450							3-8, 7-6
	F2114L-2	4K Low-power Static RAM	200	265	+5	18	NMOS	C,M	D,P	3-8, 7-6
	F2114L-3		300							3-8, 7-6
	F2114L		450							3-8, 7-6
2048 x 8	F3528-25	16K Static RAM w/Power Down	250	450/100	+5	24	Iso-H	C	D	3-12
	F3528-35		350							3-12
16,384 x 1	F3567-55	16K Static RAM w/Power Down	55	700/170	+5	20	Iso-H	C	D	3-14
16,384 x 1	F4116-2	16K Dynamic RAM	150	465/25	+12, ±5	16	NMOS	C,L,M*	D,P,F,L	3-15, 7-20
	F4116-3		200							3-15, 7-20
	F4116-4		250							3-15, 7-20
65,536 x 1	F4164-1	64K Dynamic RAM	120	250/20	+5	16	Iso-H	C	D	3-37
	F4164-2		150							3-37
	F4164-3		200							3-37

Notes

1. C = Commercial (T_A = 0°C to +70°C)
   L = Limited Military (T_A = −55°C to +85°C)
   M = Military (T_A = −55°C to +125°C)
   M* = Special Military (T_{Case} = −55°C to +110°C)
2. P = Plastic DIP
   D = Ceramic DIP
   F = Flatpak
   L = Leadless Chip Carrier

UV Erasable Programmable Read Only Memories

Organization	Part No.	Description	Access Time (ns)	Max Power Dissipation (mW)	Power Supply (V)	No. of Pins	Technology	Temperature Range (Note 1)	Package (Note 2)	Page No.
1024 x 8	F2708-1	8K EPROM	350	800	+12, ±5	24	NMOS	C	D	4-3
	F2708		450					C		4-3
4096 x 8	F2732	32K EPROM	450	790/160	+5	24	NMOS	C	D	4-10
8192 x 8	F2764	64K EPROM	200	750	+5	28	Iso-H	C	D	4-16

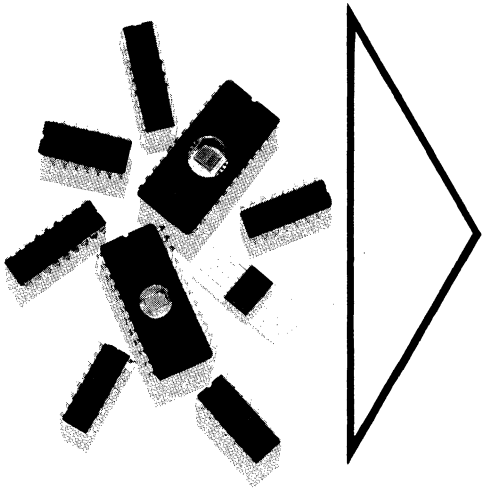
Serial Memories

Function	Organization	Part No.	Frequency Range (MHz)	Max Power Dissipation (mW)	Power Supply (V)	No. of Pins	Temperature Range (Note 1)	Technology	Package (Note 2)	Page No.
Static Shift Register	32 x 6	3348	dc to 1.0	500	−12, +5	24	C	PMOS	D	5-13
		3349				16			D,P	5-13
	64 x 4	3342	dc to 1.5	380	−12, +5	16	C	PMOS	D,P	5-9
	80 x 4	3357-1	dc to 4.0	375	−12, +5	16	C,L,M	PMOS	D,P	5-25, 7-15
		F2847	dc to 3.0	455			C		D,P	5-25
		F2847	dc to 2.5	600			L,M		D	7-15
		3357-2	dc to 2.0	285			C		D,P	5-25
Low Power Static Shift Register		F2847L	dc to 3.0	320			C		D,P	5-25
		F2847L	dc to 2.5	410			L,M		D	7-15
First-in First-out	64 x 4	3341A	dc to 1.0	450	−12, +5	16	C,L,M	PMOS	D	5-3, 7-8
		3341	dc to 0.7							5-3, 7-8
	40 x 9	3351-1	dc to 2.0	520	−12, +5	28	C,L,M	PMOS	D,P	5-16, 7-11
		3351-3	dc to 1.5	420						5-16, 7-11
		3351-2	dc to 1.0	420						5-16, 7-11

Special Function Products

Function	Part No.	Power Supply	Max Power Dissipation (mW)	Temperature Range	No. of Pins	Technology	Package	Page No.
TV Sync Generator	3262A	−12, +5	575	C	16	PMOS	D	6-3
TV Sync Generator with Gen-Lock	3262B	−12, +5	575	C	16	PMOS	D	6-9
8-Channel Multiplex Switch	3708	−19, +5.5	175	C,L,M	16	PMOS	D	6-15, 7-18

Notes on previous page.



Section 2
MOS Memory Technology Overview

To understand MOS circuitry, it is first necessary to become familiar with some of the physical characteristics of the metal-oxide-semiconductor structure. The MOS process involves the separation of a metal or other gate-material electrode from a semiconductor substrate by a thin insulator of silicon dioxide (oxide). The stand-alone band structures of the materials are pictured in *Figure 1.* The Fermi level, stated simply, is a reference energy level at which the probability of finding an electron is 1/2. The bands below it are mostly full, and those above are generally empty. Thus, since the conduction band in the metal is full, the Fermi level is situated within the conduction band. The *work function,* or the amount of energy needed to remove an electron from the Fermi level to a point outside the atom, is designated ϕ.

When these materials are together in an equilibrium state, electrons have been transferred from the metal to the silicon due to the lower work function of the metal. This equalizes the Fermi levels at the junctions and forms a potential across the non-conducting oxide (*Figure 2*). This structure, in effect, is a capacitor with charge stored on the gate and in the substrate, with a voltage equal to the difference in the work functions. In the particular case shown, if a negative voltage, with respect to the substrate, is applied to the gate, the voltage across the capacitor tends to decrease until it reaches the point shown in *Figure 3.* This applied voltage is then equal to the difference in work functions and is designated the *flat-band voltage* V_{FB}. Therefore, $V_{FB} = \phi$ metal $- \phi$ silicon in the ideal case. This voltage is useful when computing another important parameter, the threshold voltage, discussed later.

Figure 1

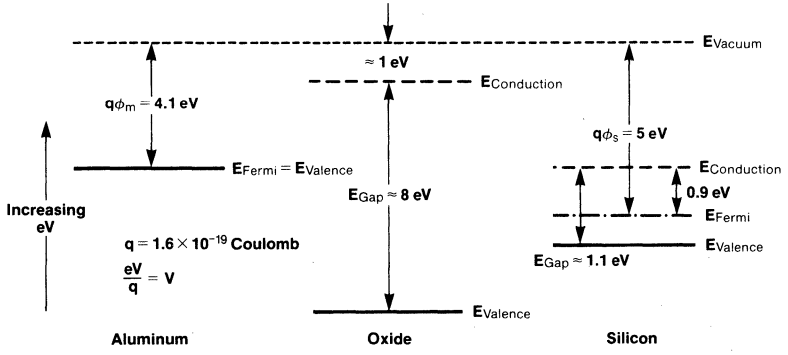


Figure 2

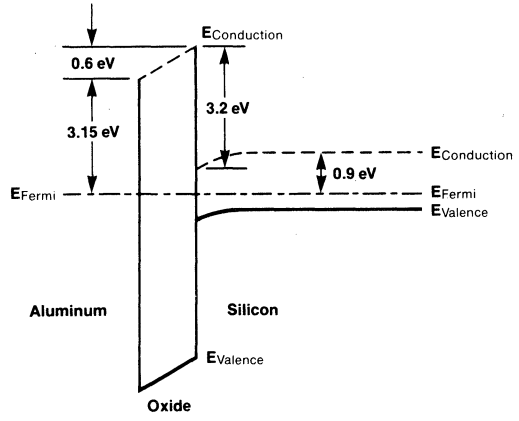
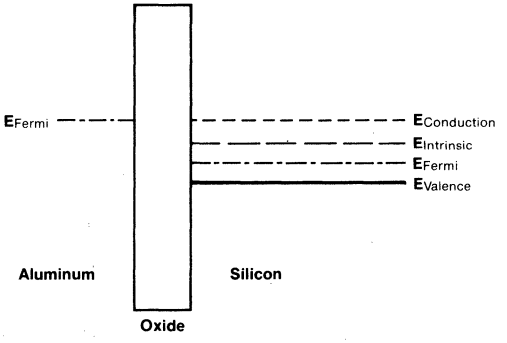


Figure 3



As the voltage on the gate becomes positive with respect to the substrate, it continues to repel the positive charge carriers in the surface below as well as build up a positive charge on the gate. When the substrate surface is nearly void of mobile carriers, the condition is called *surface depletion* (*Figure 4*). As the gate voltage becomes still more positive under equilibrium conditions, the Fermi level remains constant and the energy bands continue to bend downward. At the point where the actual Fermi level crosses the intrinsic (undoped) Fermi level, the substrate behaves like an n-type semiconductor. This forms a channel of n-type carriers (mobile electrons) between the source and drain called the *inversion layer* (*Figure 5*). The voltage at which this channel forms is known as the threshold voltage, and can be expressed as

$$V_T = V_{FB} + 2|\phi_p| + \frac{1}{C'_{ox}}\sqrt{2E_S\, qN_a\,(2\phi_p + V_C - V_B)} + V_C \quad (1)$$

where V_{FB} is the positive voltage needed to neutralize the charge between the gate and the substrate, and $2|\phi_p|$ is the voltage required to cause the bands to bend into the inverted condition. The third term results from the charge distribution within the substrate and depends on the permittivity of the silicon (E_S), the doping level N_a, the channel-to-substrate bias ($V_C - V_B$), and the oxide capacitance C'_{ox} (per square unit). V_C, the last term, is the channel voltage (typically zero when referenced to the source).

Figure 4

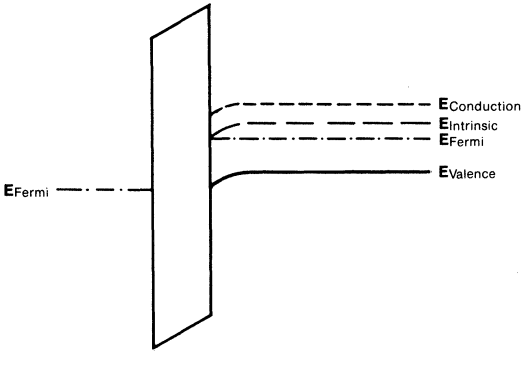
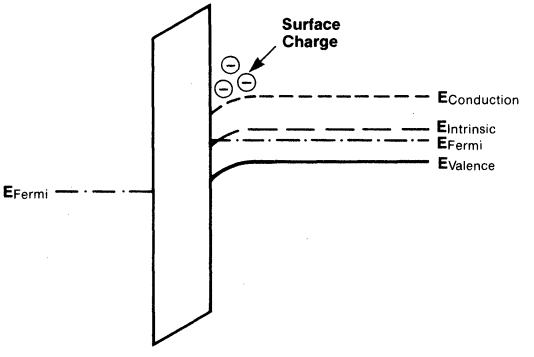
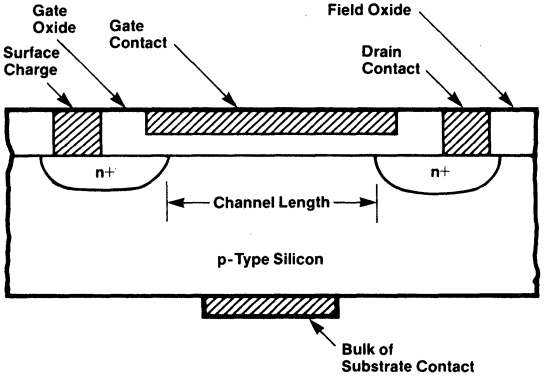


Figure 5



Since the channel forms because of the applied voltage, this device is said to conduct in the *enhancement* mode. *Depletion*-mode devices, on the other hand, are manufactured so that the channel exists without any external bias applied. The gate voltage must be applied to remove the channel and shut the transistor off. In fact, due to the internal positive charge contained in the oxide, an n-channel device may have an inverted substrate with no gate bias applied (*Figure 6*). Thus, it was not until special processing techniques were developed to reduce the oxide charge that enhancement NMOS devices became popular. Until that time, the majority of MOS devices were p-channel (PMOS). Although the previous discussion applies to NMOS technology, it is also applicable to PMOS with an n-type substrate and a negative gate-to-substrate voltage.

Figure 6



A brief history of MOS devices may prove enlightening. PMOS devices were originally constructed using <111>-oriented silicon with metal gates and had a typical threshold voltage of −4 V. Unfortunately, threshold voltages of −2 V or less were required for compatibility with TTL circuitry. This problem was solved by substituting a heavily doped, highly conductive layer of poly-crystalline silicon (poly) for the aluminum gate. This substitution brought about three major advantages. First, since the silicon gate material had a work function ϕ closer to that of the substrate, V_{FB} was reduced and V_T was correspondingly smaller. Secondly, since this type of silicon was stable at high temperatures, the source and drain could be diffused after the gate, thus yielding near perfect gate-channel alignment using the gate layer as a mask. And third, since another insulating layer could be deposited over the first poly, a second layer of metal or poly interconnections could be run over the top of the first (*Figure 7*).

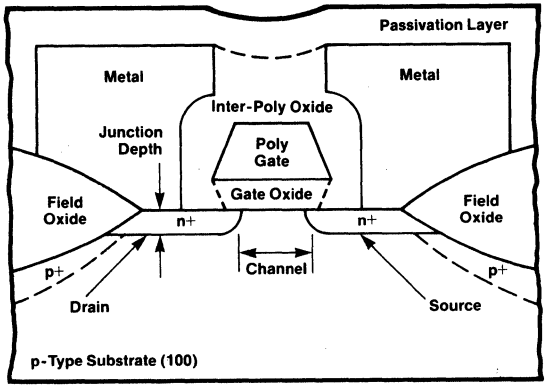
In addition to changing the gate material, it was also found that substituting <100>-oriented silicon for <111> type tended to lower threshold voltages and reduce surface state charge by a factor of three. Unfortunately, while the surface could be inverted under the gate with less voltage, it would also be inverted under the thicker field-oxide region, causing a lower field threshold V_{TF}. This limited the operating voltage, and to some extent the density, of the device.

Fairchild addressed this low-V_{TF} problem through the Isoplanar process. The field oxide is selectively grown to provide a thicker oxide layer where required (*Figure 7*). Since the oxide repels the p-type dopants, the substrate just below the field oxide becomes a p^+ or a more concentrated p region. As can be seen from *Equation 1*, the threshold voltage is higher where N_a is greater. In addition to raising the V_{TF}, this process also reduces vertical steps, making devices easier to manufacture.

Also to help overcome the V_{TF} problem and to aid in adjusting threshold voltages, the ion-implantation process was developed. This process consists of accelerating a pure beam of ionized dopant atoms and directing them onto the surface of the silicon. Typically, these ions are used to change the doping level of the channel area to lower the threshold properties with respect to the field or to effect more precise V_T control.

While the above advances are applicable to both P and NMOS, NMOS has received most of the attention due, in part, to its inherent speed advantages. Since

Figure 7



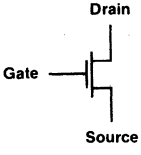
the mobility of carriers (electrons) is roughly two times that of holes, NMOS devices typically exhibit higher speed performance.

Transistor Operations

MOS transistors are a subset of a more general class of devices called insulated-gate field-effect transistors or IGFETs. While many of the properties discussed in the following section apply specifically to MOSFETs, most are analogous to the characteristics of other types of IGFETs. See *Figure 8* for the MOS transistor symbol and definition of terminals.

After the gate voltage exceeds V_T and the channel has formed, the magnitude of the current between the source and drain depends on the drain voltage V_D. Since the channel acts as a resistive element, V_D and V_T are typically specified with respect to the source.

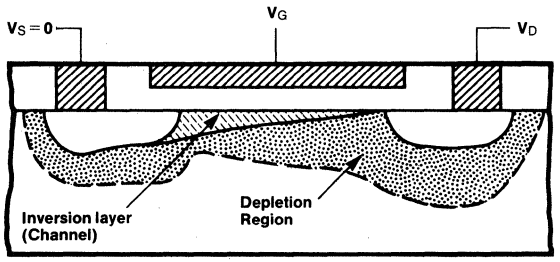
Figure 8



Thus when the channel first begins to form, $V_T = V_G - V_S$. As V_D continues to increase positively, the current increases linearly to a saturated condition (*Figure 9*), where further increases in V_D do not produce appreciable changes in drain current I_D. At this point,

$$V_{D(SAT)} = V_G - V_T \qquad (2)$$

Figure 9



When operated in the linear region, below $V_{D(SAT)}$, the MOSFET looks very much like a voltage-controlled resistor. MOSFET gain is typically measured by its transconductance, the rate of change of drain current with respect to gate voltage. The transconductance in the saturation region is given by

$$g_{msat} = \mu_n C'_{ox} W/L (V_G - V_S - V_T) \quad (3)$$

where μ_n is the mobility of electrons, C'_{ox} is the oxide capacitance (per unit area), and W/L is the channel width-to-length ratio, which will be discussed in greater detail later.

In a typical MOS integrated circuit, the substrate is common to many transistors. The substrate voltage can be varied with respect to the source and will affect the threshold voltage as indicated by *Equation 4.* In general, the change in V_T with substrate bias V_B is given by

$$V_T = K \sqrt{V_S - V_B} \quad (4)$$

where K is an empirical constant usually between 0.5 and 0.75.

In an MOS integrated circuit the source-substrate junction must be reverse biased to isolate the transistors from each other. Thus, the substrate voltage can be no greater than 0.6 V relative to the source. The negative voltage limit is the reverse breakdown voltage of this junction. Due to the charge distribution within the bulk, making V_B more negative causes V_T to become more positive. This effect is used in some devices to adjust V_T.

Threshold voltage V_T is a very important parameter since it affects input and output levels (noise margin), power-supply tolerance, power dissipation, speed, and output-drive current. Also, if the device design must allow for large variations in V_T, the speed-power product cannot be maximized. A substrate-bias generator can be used on-chip to control V_T such as in the case of the F4164 and F3528. This circuit compares the on-chip threshold voltages against a reference that is a fixed percentage of V_{CC}. The generator senses V_T variations and, using a *charge-pump* technique, adjusts the substrate bias to compensate. In addition to improving design, the bias generator eliminates the need for an external V_{BB} supply.

Memory-cell Design

The basic static read-write random access memory (RAM) cell (*Figure 10*) consists of two cross-coupled inverters used to latch the data as a '1' or '0'. The X (word) lines and the Y (bit) lines service other similar cells. Various types of cell pull-up devices have been employed, with the depletion-mode transistor shown or the poly resistor the most popular. These types are favored over enhancement-mode loads because the V_T drop required in an enhancement device lowers the cell's output-HIGH voltage below acceptable levels. Poly resistors have gained popularity over diffused resistors because of smaller size and higher resistance values. While fairly simple in structure, static cells have two main drawbacks—relatively large size and high power consumption, both critical parameters for high-density memories.

To overcome these limitations, the dynamic memory cell was devised. The most popular cells initially were the three-transistor types. Two major types were produced, differing mainly in the number of interconnections. The method of storage was the same, however.

Since the gates of MOS transistors are basically a capacitor, charge can be stored on the gate-to-source capacitance shown in *Figure 11.* This stored charge switches the transistor either on or off, storing the information. Unfortunately, since the charge eventually leaks off the gate, this cell needs to be refreshed at regular intervals; hence, the term *dynamic* memory is applied. Peripheral circuitry senses the data and rewrites it into the cell. This increased complexity can be shared among many cells in a multiplexed fashion, reducing the cell to three transistors with no direct power path between supplies. The resulting increase in density and reduction in power have made dynamic RAMs (DRAMs) very popular. The three-transistor cell was employed in DRAMs up through the 2K-bit density level.

Figure 10

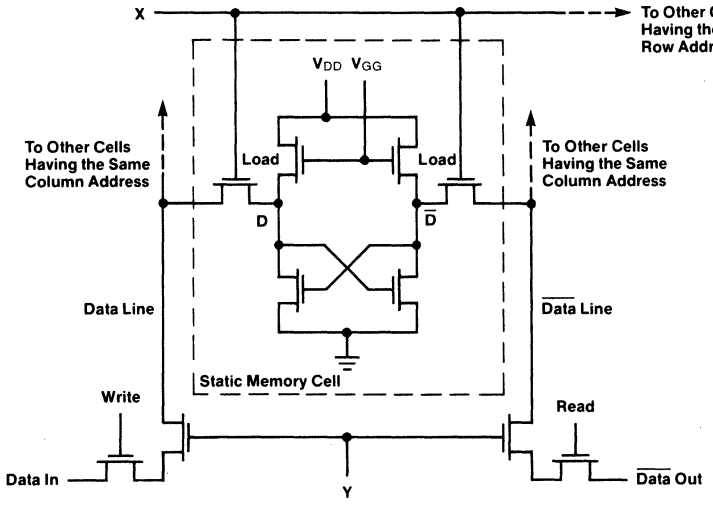
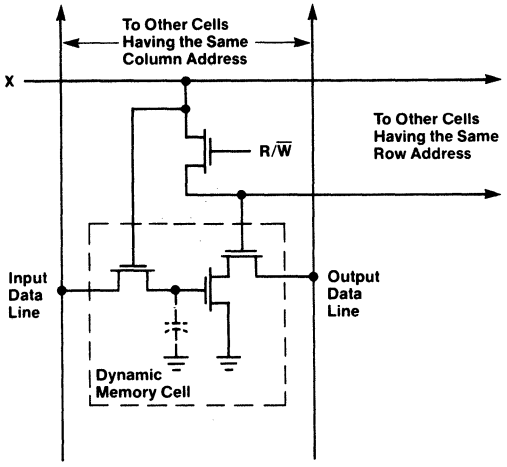
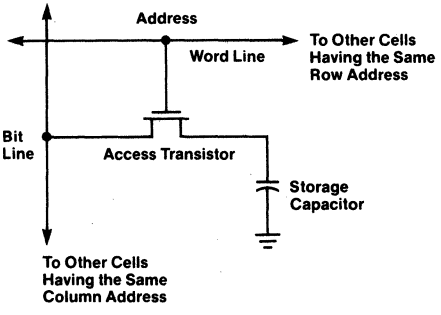


Figure 11



The 4K-bit DRAM generation and the following density levels (16K, 64K, etc.), incorporate the smaller one-transistor-cell design consisting of a capacitor and an access transistor (*Figure 12*). Because the one-transistor cell is much smaller than its predecessors, the amount of stored signal available for detection is also less. The one-transistor cell requires a more complex *balanced* sense amplifier, but the inherent density advantages make this cell viable.

Figure 12



RAM Architecture

The basic RAM organization can be word-wide (2K x 8, 1K x 4) or bit-wide (1K x 1, 16K x 1). Word-wide RAMs are generally used in applications requiring relatively small amounts of byte-organized memory, such as microprocessor-based systems. Accessing one 8-bit-wide device requires less power than enabling eight 1-bit-wide devices for the same amount of information.

In larger systems, the bit-wide device finds favor for two reasons. First, since the error-correction schemes employed in many large systems can correct single bit errors in a word, if one bit-wide device fails, the addressed word is correctable. Word-wide RAMs would be unsuitable for this application, because a general device failure would cause an uncorrectable 8- or 4-bit error in some words. Second, since output buffers required on a word-wide device are eliminated, the bit-wide memory-chip size is smaller. This is critical, for device cost is directly related to chip size and low-cost devices are necessary in cost-effective large memory systems.

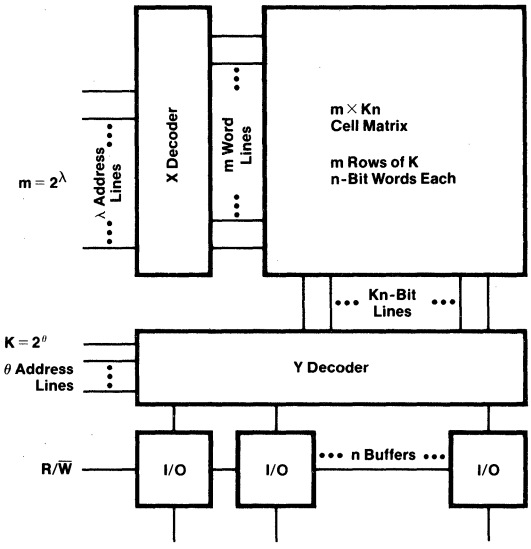
In a word-wide arrangement, some of the address lines (λ) are decoded to select a row of memory cells, as in *Figure 13.* The remaining address bits (θ) are decoded to determine which of the K sets of n cells within the row is being accessed. The entire n-bit word is then available at the I/O circuits.

In the bit-wide case, each word is one bit wide and the decoders are used to select any of the Y bit locations within the total X number of rows. In this configuration, the data lines may be connected in parallel to a single I/O buffer. These same matrix ideas are employed on both static and dynamic RAMs, although additional peripheral complexity is required for sensing and refreshing in the DRAM.

Due to the small amount of charge stored in DRAM memory cells, any loss of charge due to leakage or charge used during a read operation must be replaced by refreshing the location. Restoration is typically accomplished by the sense amp reading the information present in the cell, and then rewriting it immediately afterward. This function can be shared among all the cells in a given column. A block diagram of a sense amp and how it relates to the memory cells is shown in *Figure 14.*

There are many configurations of the sense-amp relationship to the storage-cell array; one of the most popular DRAM architectures is shown in *Figure 15.* It was not by accident that the sense amps are in the

Figure 13



center of the array. Since the small amount of stored charge must drive the bit-line capacitance, which is related to the bit-line length, the bit lines should be kept as short as possible. Thus, there is a tradeoff between the number of cells serviced by any one sense amp and the signal wasted to charge the bit line. This effect, coupled with the balanced nature of the sense amps, makes the middle of the array a good compromise. In addition, because the ratio of bit-line capacitance to storage capacitance can be 10:1 or more, the bit lines are sometimes precharged with a clocking circuit before the cell is connected.

Figure 14

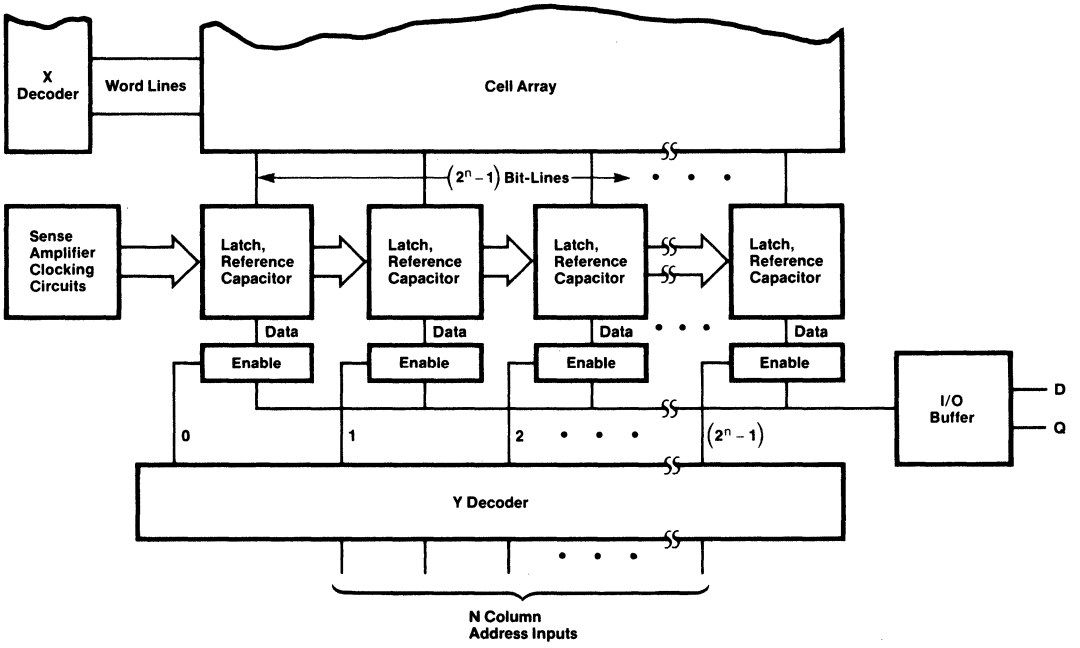
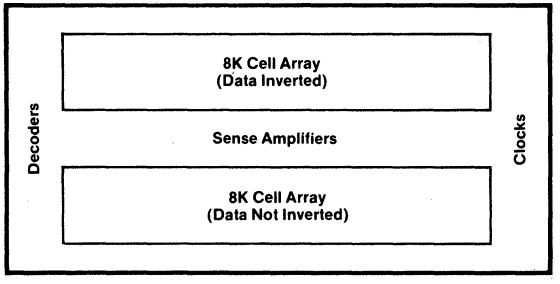


Figure 15



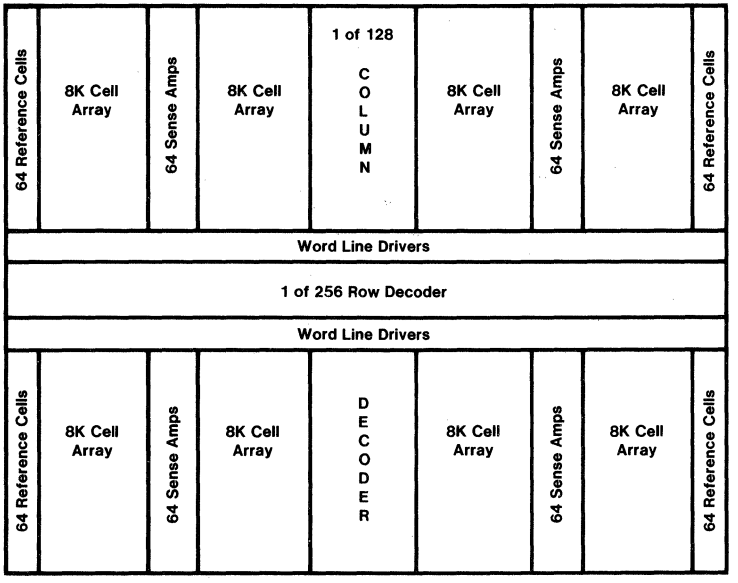
64K DRAM Architecture

With the advent of the 64K dynamic RAMs, the associated reduction in storage-cell charge has made the bit-line capacitance problem even more important. This problem is complicated for, as the array is further divided to effect shorter bit lines with less cells per line, the word lines become longer. Since layered interconnects are required and the word lines are fabricated with the less conductive polysilicon, the increased resistance adds RC time delays and slows access time. The F4164 is organized as eight 8K-bit blocks, with the word-line drivers located as shown in *Figure 16* to reduce word-line length. In addition, since the majority of the power is consumed by the sense amps, reducing the number of cells per sense amp by increasing the sense-amp count also increases the power.

Fairchild, by unique sense-amp design, has been able to double the effective service range of each sense amp of the F4164 without seriously affecting the signal available for sensing. Each of the 128 sense amps has 4 (not 2) bit lines, serving 64 cells per line. Each half bit line has an isolating transistor associated with it so only one bit-line half is connected to the desired cell.

In a balanced sense-amp design, the voltage on the bit-line half connected to the cell is compared against a reference voltage set up on another bit-line half connected to a *dummy* capacitor. Ideally, this dummy capacitor should be one half the capacitance of the storage cell. Unfortunately, if the storage capacitor is the minimum allowable size, there is obviously a problem making the dummy half that size. Fairchild

Figure 16



has overcome this problem in the F4164 sense amp by sharing one full-size dummy capacitor between the two halves of each bit line; thus, half the charge is supplied to each to establish the reference voltage. If the memory-cell capacitor has a HIGH charge, connecting it to a half bit line will cause that half to be more positive than the reference. If the cell has a LOW charge, the opposite occurs. This difference is sensed and latched by the sense amp.

Manufacturing Advances

With the advent of the one-transistor DRAM cell, it seems unlikely that further circuit evolution will bring about dramatic reductions in cell size. Further size reductions will come from process improvements, just as process modifications have already decreased the one-transistor cell from about 1 mil^2 to roughly 0.3 mil^2.

There are several ways to *shrink* an existing circuit without changing its basic design. A two-dimensional reduction in device geometries has already been successfully employed on several generations of MOS devices. At the transistor level, the length-to-width ratio of the channel determines its resistive properties, gain, speed performance, and relative size. Roughly, the higher the W/L, the lower the resistance, higher the gain and speed, and the larger the relative device area. Photographic size reduction can result in a smaller device that has similar properties to the original simply by keeping the W/L ratio constant.

A size reduction affecting all three dimensions is called *scaling.* Ideal scaling involves the reduction of each device dimension by a constant scale factor K. Since the field strength must generally be kept constant, the voltage at the device level is scaled by the same factor. In addition to the device area being reduced by the $1/K^2$ factor, there are also performance improvements. Speed is increased, since the smaller device area results in reduced capacitance and transit time. Also, because the voltage after scaling is 1/K times the voltage before and the post-scaling current is reduced by a like amount, power (V x I) is scaled by $1/K^2$. Since both power and voltage are lower in the scaled device, reliability is enhanced.

To ensure that a scaled design can be manufactured, the ideal scaling rules must be adjusted to provide process compatibility. The process parameters involved are dopant levels, oxide thickness, junction depths, and supply voltage. Isoplanar-H is Fairchild's proprietary Isoplanar scaled-MOS process. This scaled NMOS is characterized by optical lithography,

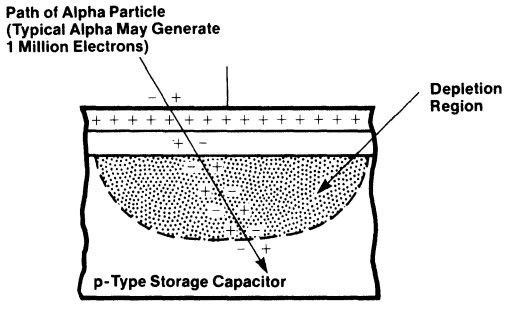
dry (plasma) etching, arsenic junctions, sub-500 Å oxides, and multiple levels of interconnect.

At present, scaling techniques are limited by the tolerances of existing photolithographic equipment. Contact printers with tolerances of ±0.75 microns, once acceptable when dealing with 10-micron line widths, are no longer useful at the 1-2 micron level. The advent of electron beam (E-beam) and step-and-repeat printers has demonstrated that this accuracy is possible for a price. The cost, just for the equipment, to set up a medium-size scaled-MOS line is around 30 million dollars.

Aside from the scaling limits imposed by equipment availability, there are physical limits as well. Reduced alpha immunity, short-channel effects, and reduced storage charge, are problems that increase significantly as device dimensions become smaller.

Alpha immunity is the relative resistance of a particular device to alpha-particle induced *soft errors*. Soft errors are defined as random bit errors not associated with physical defects on the chip. Alpha-induced soft errors occur when extra electron-hole pairs are generated by an alpha-particle collision with the chip, thus injecting extraneous charge that causes sensing malfunctions (*Figure 17*). The package material is the source of these alpha particles.

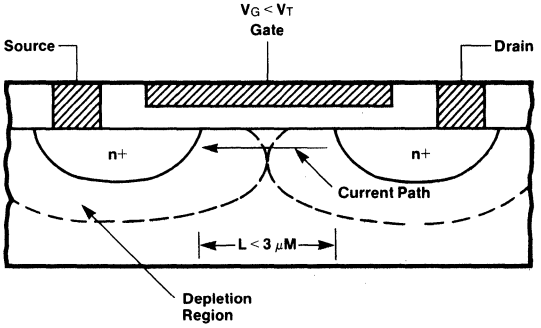
Figure 17



As device dimensions are further reduced, the amount of charge stored in each cell is decreased. Thus, the difference in the number of electrons sensed as a '1' and the number representing a '0' is also smaller. Therefore, since the number of electron-hole pairs produced within the silicon by an incident alpha particle is roughly constant, the probability of an error caused by this extra charge increases as device geometries and stored charge are scaled.

Other factors limiting the degree to which a device can be scaled are grouped into a category called *short-channel effects*. These characteristics become most pronounced when the channel length becomes less than about 3 microns. Although threshold voltage and several other parameters are affected, the largest problem is caused by the proximity of the source and drain regions. Since these two regions are now separated by a small distance, the relatively constant depletion regions that surround them may overlap, causing an unwanted current path between the source and drain (*Figure 18*). Research is underway to minimize these difficulties by varying process techniques, but short-channel effects remain a physical consideration when scaling.

Figure 18



Since vertical dimensions like oxide thickness also shrink during scaling, storage capacitance per unit area for future devices will remain roughly the same as for present-day NMOS. However, since the power supply voltage must be scaled to maintain a constant electric field, the charge written into a dynamic memory cell will be reduced since it is a product of the cell capacitance and writing voltage.

This reduction is fairly critical for a DRAM, because the charge in the cell is shared with a relatively large bit-line capacitance. Therefore, the signal voltage that the sense amplifier must correctly process is scaled in the same manner as the writing voltage.

The Future of MOS Memory

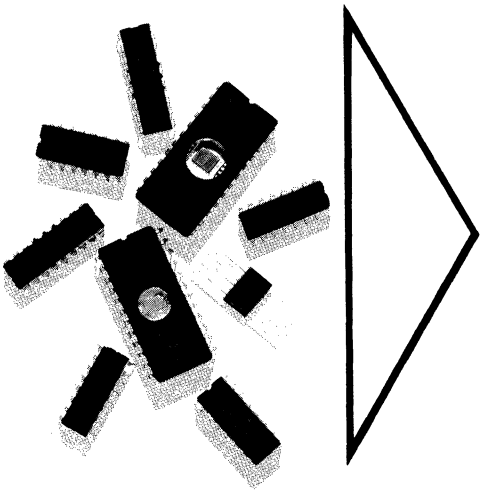
Future advances in very large scale integration will depend heavily on the ability of manufacturers to reduce device geometries beyond the current state of the art. Present geometries used for devices like the 64K DRAM, 16K fast static RAMs and the like are based on 3-micron design rules. Thus, MOS transistor

channel lengths are drawn to a 3-micron length. The finished effective channel length is 2–2.5 microns.

Future enhancements involve further shrinking of the design rules. At channel lengths below 1.5 micron, a new lithography technique such as X-ray or electron beam will be required. Using these mask-exposure techniques, sub-micron geometries will evolve to produce 1 megabit DRAMs in the late 1980s.

VLSI geometries will encounter a silicon-material limit at about the 0.5 micron level by the end of the decade. At this point, new substrate materials such as gallium arsenide may be required to continue the trend of increased integration. Materials development programs are presently investigating refractory metal-silicide gate structures. This approach significantly reduces the delays caused by interconnect resistivity while maintaining the relatively low work-function difference between the silicon substrate and the gate material. Thus, TTL compatibility can still be realized. Decreased RC delays will reduce the DRAM speed-related pattern sensitivities.

DRAMs will benefit from new types of materials, continued reduction of defect density, and increased automation of the production process. All of these factors will contribute to the increases in density, cost-effectiveness, reliability and performance that will appear in future generations of semiconductor memories.



2102/2102L/21L02
1024 x 1 Static RAM

MOS Memory Products

Description

The 2102 family consists of 1024-word by 1-bit static Random Access read/write Memories (RAM) that require a single 5 V supply, have fully TTL-compatible inputs and output, and require no clocking or refresh. Chip Select ($\overline{CS}$) permits a 3-state output allowing the outputs to be wired-OR. Special features include low power dissipation (2102L) and a power-down capability (21L02).

The 2102, 2102L and 21L02 are manufactured using the n-channel Isoplanar process and are available in a 16-pin dual in-line package or flatpak.

- **FAST ACCESS—250 ns**
- **SINGLE +5 V SUPPLY**
- **TTL-COMPATIBLE INPUTS AND OUTPUT**
- **TOTALLY STATIC—NO CLOCKS OR REFRESH**
- **3-STATE OUTPUT**
- **LOW POWER (2102L)**
- **POWER-DOWN CAPABILITY (21L02)**
- **FULLY EXPANDABLE**
- **FULLY DECODED**
- **16-PIN DUAL IN-LINE PACKAGE**

Pin Names

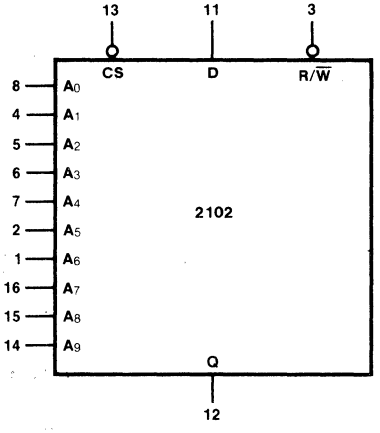
A_0-A_9	Address Inputs
D	Data Input
R/$\overline{W}$	Read/Write
$\overline{CS}$	Chip Select (active LOW)
Q	Data Output

Absolute Maximum Ratings

Voltage on Any Pin with Respect to V_{SS}	−0.5 V to +7.0 V
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +70°C

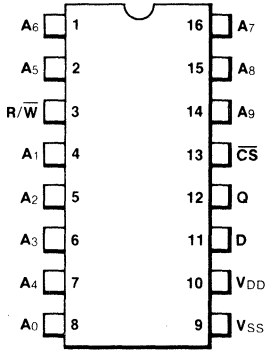
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliabiliy.

Logic Symbol



V_{SS} = Pin 9
V_{DD} = Pin 10

Connection Diagram
16-Pin DIP

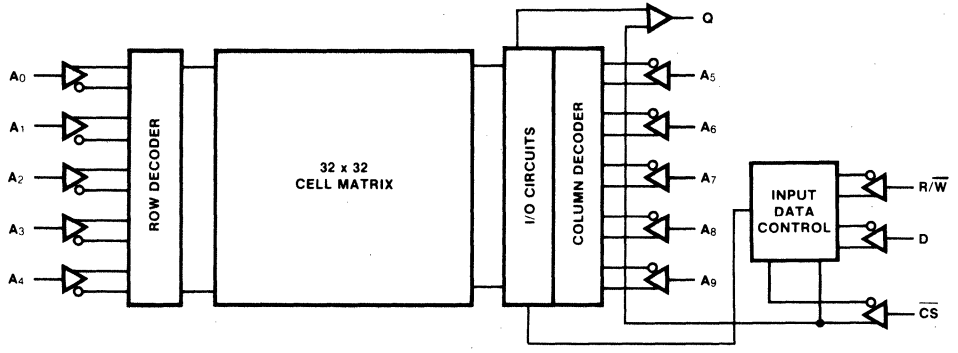


(Top View)

Package	Outline	Order Code
Ceramic DIP	6Z	D
Plastic DIP	UC	P
Flatpak	II	F

Note
The Flatpak has the same pin number-to-function correspondence as the DIP.

Block Diagram



Truth Table

$\overline{CS}$	R/$\overline{W}$	D	Q	Comments
H	X	X	•	Chip Deselected
L	L	H	H	Write "1"†
L	L	L	L	Write "0"†
L	H	X	D_n	Read†

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
• = Output High Impedance State
D_n = Data at Address Location
† = Chip Selected

Power/Access Time Guide

	Part Number	Access Time	$I_{DD(MAX)}$
Power Down	21L02H	250 ns	30 mA
	21L02F	350 ns	30 mA
	21L021	450 ns	30 mA
	21L022	650 ns	30 mA
Low Power	2102LH	250 ns	30 mA
	2102LF	350 ns	30 mA
	2102L1	450 ns	30 mA
	2102L2	650 ns	30 mA
Standard	2102H	250 ns	55 mA
	2102F	350 ns	55 mA
	21021	450 ns	55 mA
	21022	650 ns	55 mA

Functional Description

The 2102, 2102L and 21L02 are 1024 x 1 static RAMs. When the Chip Select ($\overline{CS}$) goes HIGH, the Read/Write (R/$\overline{W}$) input is disabled and the Data Output (Q) is forced into a high impedance state. When $\overline{CS}$ goes LOW, the Read/Write input is enabled.

When R/$\overline{W}$ goes LOW, data from the Data Input (D) is written at the location specified by the Address Inputs (A_n). The Data Output will be identical to the Data Input during a write command. When R/$\overline{W}$ goes HIGH, the contents of the addressed location will appear at Q. Q is not inverted from D in the 2102. (See Truth Table).

DC Requirements T_A = 0°C to +70°C

Symbol	Characteristic, Note		2102, 2102L Min	2102, 2102L Max	21L02 Min	21L02 Max	Unit	Condition
V_{IH}	Input HIGH Voltage	H,F,1	2.0	V_{DD}	2.0	V_{DD}	V	
		2	2.2	V_{DD}	2.2	V_{DD}		
V_{IL}	Input LOW Voltage	H,F,1	−0.5	0.8	−0.5	0.8	V	
		2	−0.5	0.65	−0.5	0.65		
V_{DD}	Power Supply Voltage		4.75	5.25	4.5	5.5	V	

DC Characteristics V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, T_A = 0°C to +70°C

Symbol	Characteristic, Note		2102, 2102L, 21L02 Min	2102, 2102L, 21L02 Max	Unit	Condition
V_{OH}	Output HIGH Voltage	H,F,1	2.4		V	I_{OH} = −100 μA
		2	2.2			
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 2.1 mA
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = V_{DD}$
I_{OH}	Output HIGH Current			5.0	μA	$V_{OUT} = V_{OH(Min)}$ $\overline{CS} = V_{IH(Min)}$
I_{OL}	Output LOW Current			−10	μA	$V_{OUT} = V_{OL(Max)}$ $\overline{CS} = V_{IH(Min)}$
I_{DD}	Power Supply Current 2102 2102L 21L02			 55 30 30	mA	Inputs = $V_{DD(Max)}$ D_{OUT} open, $T_A = T_{A(Min)}$

AC Requirements T_A = 0°C to +70°C

Symbol	Characteristic	2102H 2102LH 21L02H Min	2102F 2102LF 21L02F Min	21021 2102L1 21L021 Min	21022 2102L2 21L022 Min	Unit	Condition
t_{CYC}	Read or Write Cycle Time	250	350	450	650	ns	
t_{AW}	Address to Write Time	20	20	20	200	ns	
t_{WP}	Write Pulse Width	170	170	200	350	ns	V_{SS} = 0 V
t_{WR}	Write Recovery Time	0	0	0	50	ns	See DC Requirements
t_{DS}	Data Set-up Time	170	170	200	350	ns	for Conditions on V_{DD}
t_{DH}	Data Hold Time	0	0	0	20	ns	
t_{CW}	Chip Select to Write Time	170	170	200	400	ns	
t_{WC}	Write to Chip Select Time	0	0	0	50	ns	

Note
See Power/Access Time Guide and AC Characteristics for definitions of H, F, 1 and 2 speed grades.

AC Characteristics $T_A = 0°C$ to $+70°C$

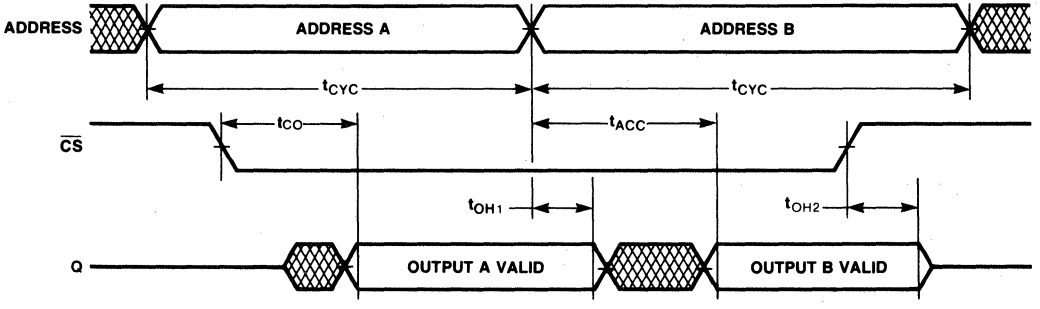
Symbol	Characteristic	2102H 2102LH 21L02H Min	2102H 2102LH 21L02H Max	2102F 2102LF 21L02F Min	2102F 2102LF 21L02F Max	21021 2102L1 21L021 Min	21021 2102L1 21L021 Max	21022 2102L2 21L022 Min	21022 2102L2 21L022 Max	Unit	Condition
t_{ACC}	Read Access Time		250		350		450		650	ns	
t_{CO}	Chip Select LOW to Output Valid Delay		130		170		200		400	ns	$V_{SS} = 0$ V
t_{OH1}	Data Valid after Address	40		50		50		50		ns	See DC Requirements for Conditions on V_{DD}
t_{OH2}	Previous Data Valid after Chip Deselect	0		0		0		0		ns	
C_{IN}	Input Capacitance		5.0		5.0		5.0		5.0	pF	$V_{IN} = 0$ V, $V_{SS} = 0$ V
C_{OUT}	Output Capacitance		10		10		10		10	pF	$f = 1$ MHz, $T_A = 25°C$

Power Down Characteristics (21L02 only) $T_A = 0°C$ to $+70°C$

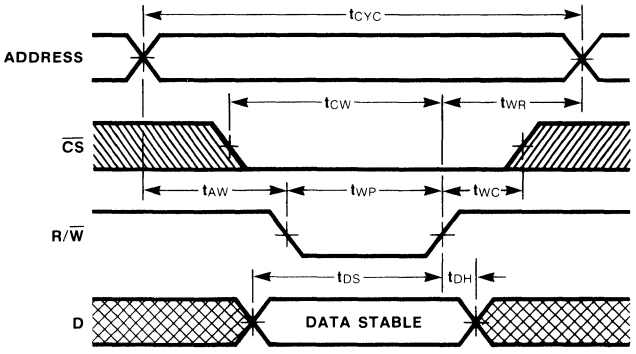
Symbol	Characteristic	21L02 Min	21L02 Max	Unit	Condition
$I_{DD(PD)}$	Power Supply Current		15	mA	$V_{DD} = 1.6$ V
$V_{DD(PD)}$	Power Supply Voltage	1.6		V	
t_{CSS}	Chip Select Set-up Time	100		ns	
t_{CSH}	Chip Select Hold Time	100		ns	
V_{CS}	Chip Select Voltage	2.0		V	
V'_{DD}	Power Supply Slew Rate		100	V/μs	

Timing Diagrams

Read Cycle Timing



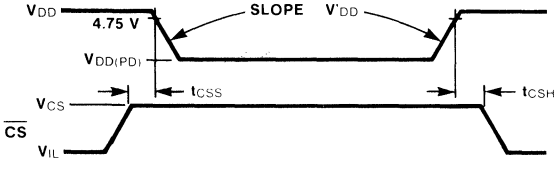
Write Cycle Timing



OUTPUT NOT VALID OR
INPUT IN HIGH OR LOW TRANSITION

HIGH-TO-LOW TRANSITION

LOW-TO-HIGH TRANSITION



AC Conditions

Input Levels: $V_{IL(Max)}$ to $V_{IH(Min)}$
Input Rise and Fall Times: 10 ns
Timing Measurement Reference Levels:
  Inputs: 1.5 V
  Output: 2.0 and 0.8 V
Output Load: 1 TTL Gate + 100 pF

F2114/2114L
1024 x 4 Static RAM

MOS Memory Products

Description

The F2114 is a 4096-bit static Random Access Memory (RAM) organized as 1024 words of four bits each. Since the operation of the F2114 is entirely static, there is no clocking or refreshing required. It operates from a single +5 V supply and is directly a TTL compatible at all inputs and outputs including the four bidirectional data I/O pins.

It is designed for memory applications in which static operation, large bit-capacity, and simple interfacing are important design considerations.

The F2114 is manufactured using Fairchild's n-channel silicon gate Isoplanar process. The innovative use of polysilicon resistors in the static memory cell permits a high bit packing density and insures low-power characteristics. It is available in a standard plastic or ceramic 18-pin dual in-line package.

- **1024 x 4-BIT ORGANIZATION**
- **SINGLE +5 V SUPPLY**
- **COMPLETELY STATIC—NO CLOCKS OR REFRESH**
- **TOTALLY TTL COMPATIBLE**
- **COMMON DATA I/O PINS WITH 3-STATE CAPABILITY**
- **IDENTICAL CYCLE AND ACCESS TIMES**
- **LOW POWER (2114L)**

Pin Names

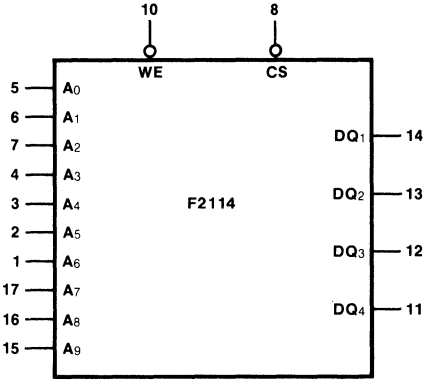
A_0-A_9	Address Inputs
$\overline{CS}$	Chip Select (Active LOW)
$\overline{WE}$	Write Enable (Active LOW)
DQ_1-DQ_4	Data Input/Output
V_{CC}	+5 V Power Supply
GND	Ground

Absolute Maximum Ratings

Voltage at Any Pin with Respect to GND	−0.5 V to +7.0 V
Operating Temperature (Ambient)	0°C to +70°C
Storage Temperature (Ambient)	−55°C to +150°C
Power Dissipation	1 W

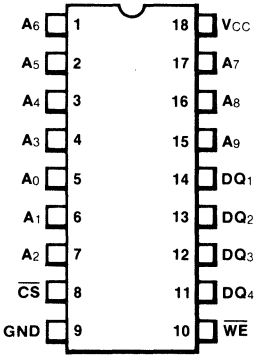
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

Logic Symbol



V_{CC} = Pin 18
GND = Pin 9

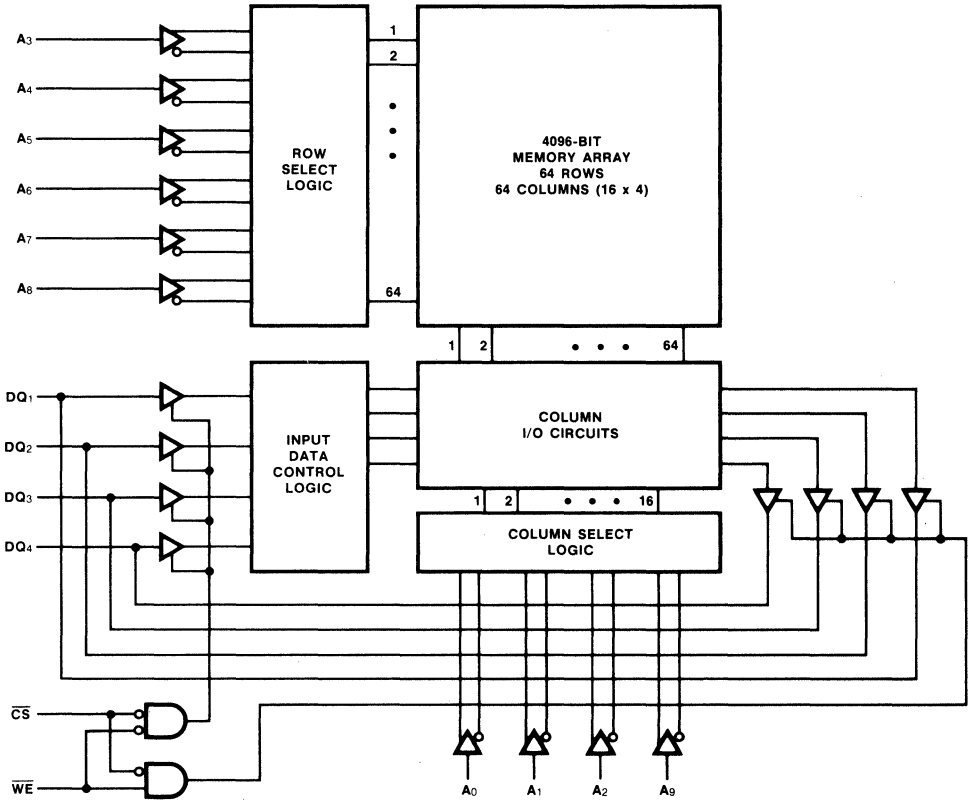
Connection Diagram
18-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	8D	D
Plastic DIP	8J	P

Block Diagram



Functional Description

The F2114, organized as 1024 words by four bits, is controlled by the Chip Select ($\overline{CS}$), Write Enable ($\overline{WE}$) and the ten address inputs. When $\overline{CS}$ goes HIGH the memory becomes deselected; the bidirectional input/output pins become high impedance, and the $\overline{WE}$ input is ignored. Therefore no read or write operations may occur. This feature allows the DQ pins to be OR-tied directly to a data bus. When the memory is selected ($\overline{CS}$ LOW), and the $\overline{WE}$ pin is in the HIGH state, the 4-bit word stored at the memory location specified by the address inputs is gated through to the DQ pins after a delay equal to the access time. If the $\overline{WE}$ is forced LOW, then the DQ pins become HIGH impedance inputs so that an externally supplied data word may be placed on them.

All inputs and bidirectional DQ pins are directly TTL compatible with data always being read out in the same polarity as it was written (i.e., not inverted).

Truth Table

$\overline{CS}$	$\overline{WE}$	DQ	Comments
H	X	High Z	Chip Deselected
L	L	H	Write "1"
L	L	L	Write "0"
L	H	Data	Read

DC Electrical Requirements and Characteristics T_A = 0 to 70°C, V_{CC} = 5.0 V ± 5%, all voltages are with respect to ground, Note 1

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{OH}	Output HIGH Voltage	2.4		V_{CC}	V	I_{OUT} = −1.2 mA
V_{OL}	Output LOW Voltage	0		0.4	V	I_{OUT} = 3.2 mA
I_{OS}	Output Short-Circuit Current, Note 2			65	mA	V_{OUT} = 0 V
I_{CC}	Average V_{CC} Supply Current F2114L2, F2114L3, F2114L			70	mA	V_{CC} = 5.25 V, T_A = 0°C,
	Average V_{CC} Supply Current F2114-2, F2114-3, F2114			100	mA	V_{IN} = 5.25 V, I/O current = 0 mA
I_{IN}	Input Leakage Current			10	μA	V_{IN} = 0 to 5.25 V
I_{DQ}	I/O Leakage Current	−10		10	μA	$\overline{CS}$ = 2.0 V, $V_{I/O}$ = 0.4 V to V_{CC}
C_{IN}	Input Capacitance			5.0	pF	T_A = 25°C, f = 1.0 MHz V_{IN} = 0 V
C_{DQ}	I/O Capacitance			5.0	pF	T_A = 25°C, f = 1.0 MHz $V_{I/O}$ = 0 V

AC Electrical Requirements And Characteristics T_A = 0°C to 70°C, V_{CC} = 5.0 V ± 5%, Notes 1 and 3

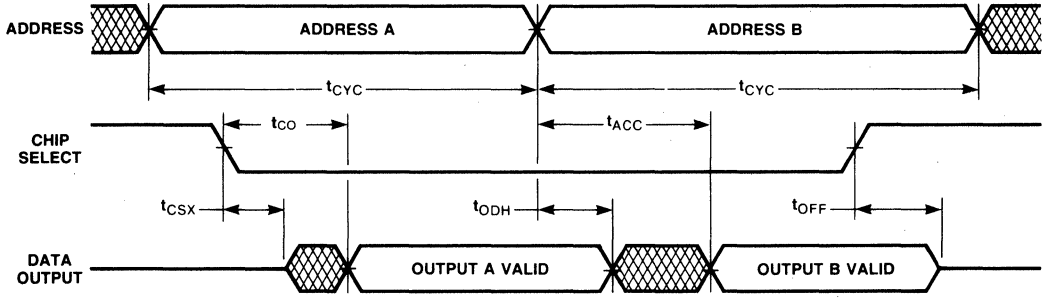
		F2114L-2 F2114-2		F2114L-3 F2114-3		F2114L F2114			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Note
t_{CYC}	Read or Write Cycle Time	200		300		450		ns	
t_{ACC}	Read Access Time		200		300		450	ns	
t_{CO}	$\overline{CS}$ LOW to Output Valid Delay		70		100		100	ns	
t_{CSX}	$\overline{CS}$ LOW to Output Active Delay	20		20		20		ns	
t_{ODH}	Output Data Hold Time After Address	50		50		50		ns	
t_{OFF}	Output Buffer Turn-Off Delay from $\overline{CS}$	0	60	0	80	0	100	ns	
t_{AW}	Address to Write Set-up Time	0		0		0		ns	
t_{WP}	$\overline{WE}$ Pulse Width	120		150		200		ns	
t_{WR}	Write Recovery Time	0		0		0		ns	
t_{DS}	Input Data Set-up Time	120		150		200		ns	
t_{DH}	Input Data Hold Time	0		0		0		ns	

Notes

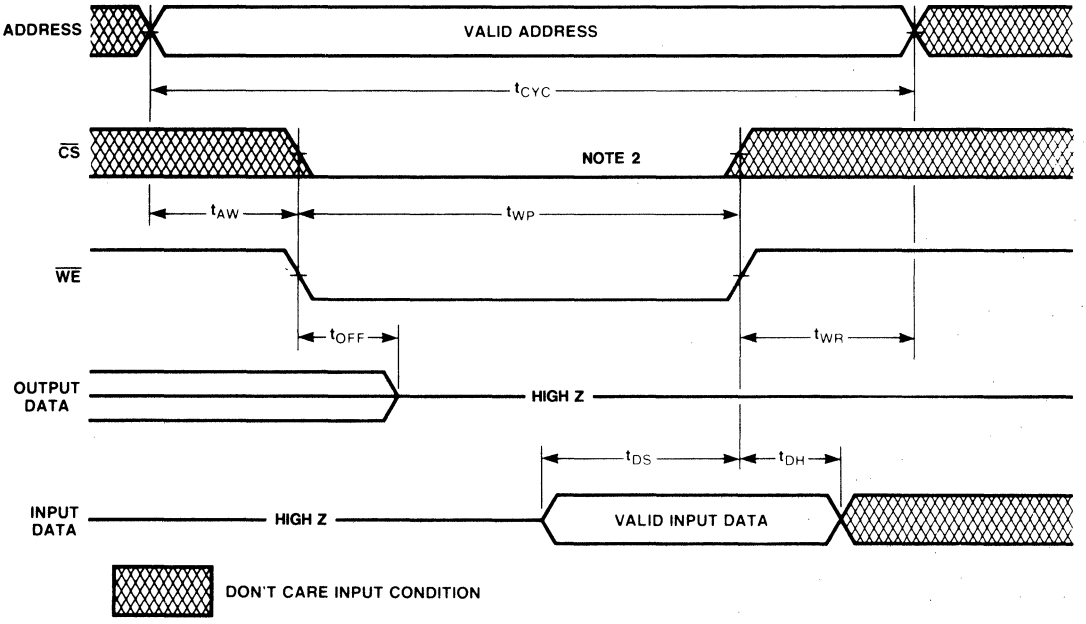
1. Test Note: The F2114 employs a self starting oscillator and a charge pump which require a start-up time of 500 μs after V_{CC} reaches at least 4.75 V.
2. Duration not to exceed 30 seconds.
3. AC Characteristic Test Conditions:

Input Levels	0.8 to 2.0 V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5 V
Output Load	1 TTL Gate, and CL = 100 pF

Read Mode Timing Diagram, Note 1



Write Mode Timing Diagram



Notes

1. $\overline{WE}$ must remain HIGH during READ cycles.
2. t_{WP} is measured from the falling edge of either $\overline{CS}$ or $\overline{WE}$ (whichever is the last to go LOW) to the rising edge of either $\overline{CS}$ or $\overline{WE}$ (whichever is the first to go HIGH).

F3528
2048 x 8 Static RAM

MOS Memory Products

Description

The F3528 is a 16,384-bit static Random Access Memory (RAM) organized as 2048 words of eight bits each. Since the operation of the F3528 is entirely static, no clocks or refresh are required. This device operates from a single +5 V supply and is directly TTL compatible at all inputs and outputs, including the eight bidirectional data DQ pins. The F3528 has an automatic power-down feature controlled by the Chip Enable function ($\overline{E}$ = active LOW). When not enabled, the F3528 is in standby mode; this reduces power dissipation by as much as 75% with no degradation of access time.

The F3528 is designed for memory applications where static operation, low cost, large bit-capacity and simple interfacing are important design considerations. It is manufactured using Fairchild's high performance, scaled NMOS technology, Isoplanar-H™. State-of-the-art design and process techniques ensure high density, lower power dissipation and excellent speed performance.

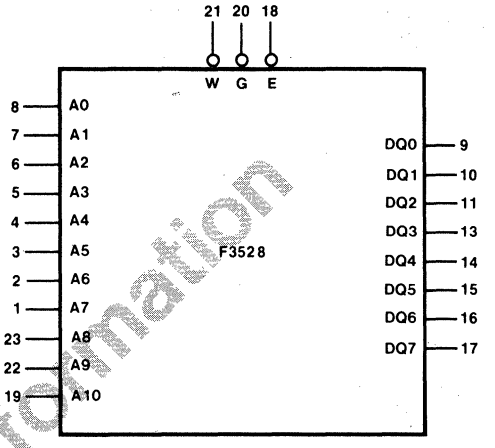
The F3528 is available in a standard 24-pin dual in-line package in a configuration that is pin and function compatible with the 2716 ultraviolet erasable PROM.

- **2048 x 8-BIT ORGANIZATION**
- **COMPLETELY STATIC—NO CLOCKS OR REFRESH**
- **SINGLE +5 V SUPPLY**
- **AUTOMATIC POWER DOWN WHEN CHIP NOT ENABLED ($\overline{E}$)**
- **ACCESS TIME—250 ns, 350 ns**
- **LOW POWER DISSIPATION**
  450 mW ACTIVE (MAX)
  100 mW STANDBY (MAX)
- **TOTALLY TTL COMPATIBLE WITH SIMPLE BUS CONTROL**
- **COMMON DATA I/O BUS WITH 3-STATE CAPABILITY**
- **PIN/FUNCTION COMPATIBLE WITH 2716**
- **STANDARD 24-PIN DIP**

Pin Names

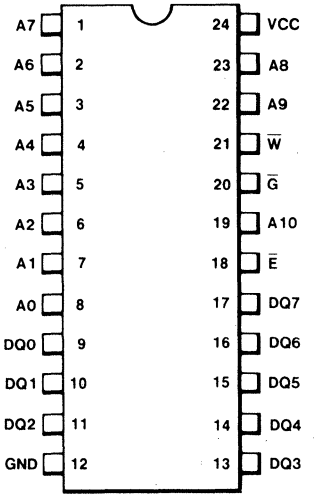
A0-A10	Address Inputs
$\overline{W}$	Write Enable Input
$\overline{G}$	Output Enable Input
$\overline{E}$	Chip Enable Input
DQ0-DQ7	Data Inputs/Outputs

Logic Symbol



V_{CC} = Pin 24
GND = Pin 12

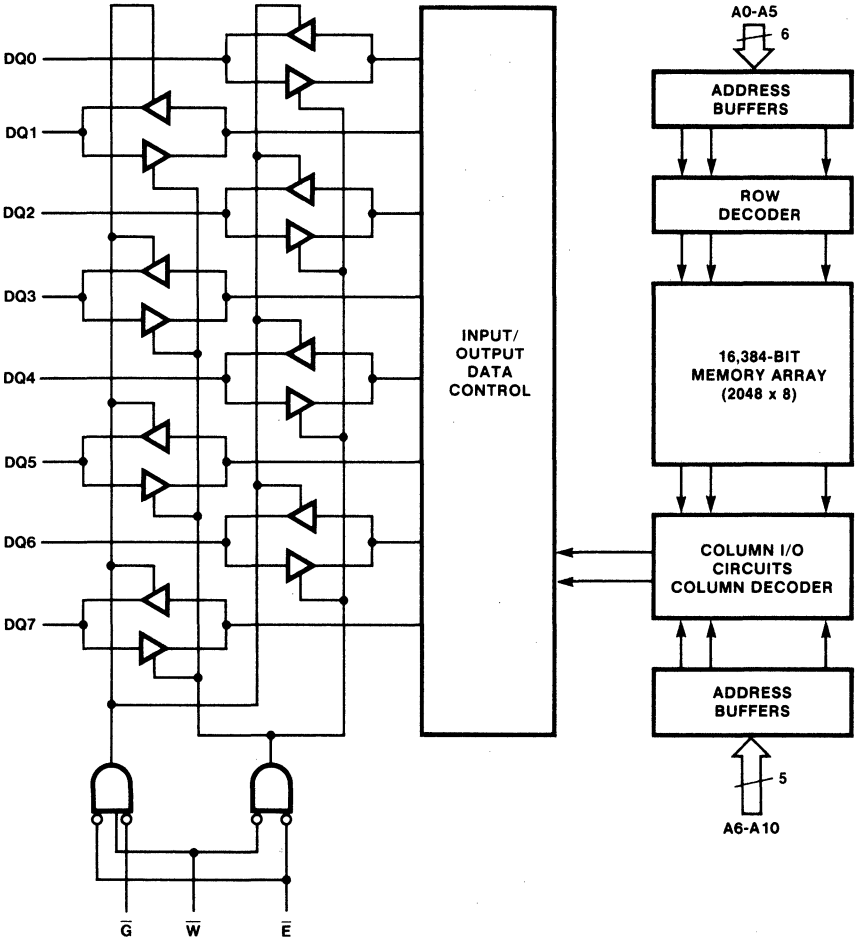
Connection Diagram
24-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	7R	D

Block Diagram



Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Chip Not Enabled	High Z	Standby
H	L	X	Output Not Enabled	High Z	Active
L	L	H	Read	Data	Active
L	L	L	Write	High Z	Active

F3567
16,384 x 1 Static RAM

MOS Memory Products

Description

The F3567 is a 16,384 x 1-bit Random Access Memory (RAM). Its operation is entirely static; therefore, no clocking or refreshing is required. The F3567 offers very fast access and cycle times, requires only a single +5 V power supply and is fully TTL compatible. D and Q functions are available on separate pins.

The F3567 has an automatic power-down feature controlled by the Enable function. When not enabled, the F3567 is in a standby mode which reduces power dissipation by as much as 75%. The F3567 is manufactured using Fairchild's high-performance, scaled NMOS technology, Isoplanar-H™, and is available in a 20-pin DIP.

- **16,384 x 1 ORGANIZATION**
- **COMPLETELY STATIC OPERATION**
- **SINGLE +5 V ± 10% POWER SUPPLY**
- **AUTOMATIC POWER-DOWN WHEN NOT ENABLED**
- **EQUAL ACCESS AND CYCLE TIMES—55 ns**
- **AVERAGE CURRENT**
  125 mA ACTIVE
  30 mA STANDBY
- **FULLY TTL COMPATIBLE**
- **3-STATE OUTPUT**
- **SEPARATE DATA INPUT AND OUTPUT**
- **STANDARD 20-PIN DIP**

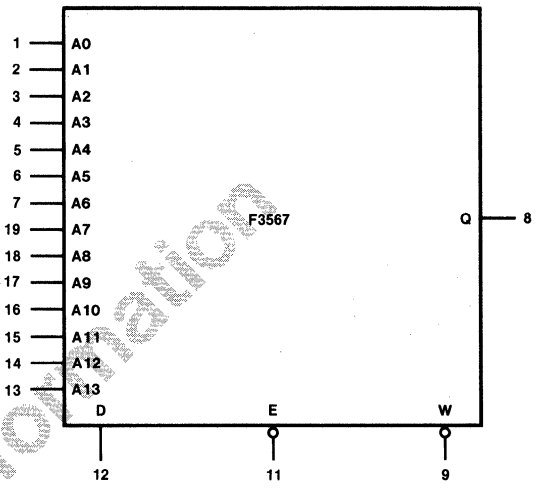
Pin Names

A0-A13	Address Inputs
$\overline{W}$	Write Enable Input
$\overline{E}$	Enable Input
D	Data Input
Q	Data Output
VCC	+5 V Power Supply

Truth Table

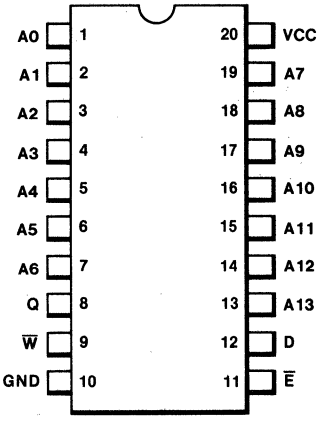
$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	Not Enabled	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	Data	Active

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

Connection Diagram
20-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	JD	D

F4116
16,384 x 1 Dynamic RAM

MOS Memory Products

Description

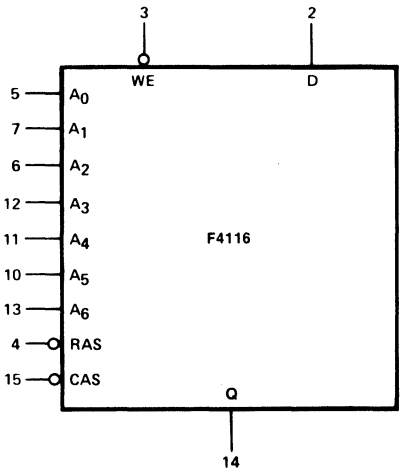
The F4116 is a 16,384-bit MOS dynamic Random Access Memory (RAM) configured as 16,384 one-bit words. It is manufactured using Fairchild's n-channel silicon gate, double-poly Isoplanar process. The use of the single-transistor memory cell along with address multiplexing techniques permits the packaging of the F4116 in a standard 16-pin dual in-line package. This package allows construction of highly dense memory systems utilizing widely available automated testing and insertion equipment.

- **INDUSTRY STANDARD 16-PIN DUAL IN-LINE PACKAGE**
- **LOW CAPACITANCE, TTL-COMPATIBLE INPUTS (INCLUDING CLOCKS)**
- **ON-CHIP ADDRESS AND INPUT DATA LATCHES**
- **3-STATE TTL-COMPATIBLE OUTPUT WITH DATA VALID TIME CONTROLLED BY $\overline{CAS}$**
- **COMMON I/O CAPABILITY**
- **TWO DIMENSIONAL SELECTION BY DECODING BOTH $\overline{RAS}$ AND $\overline{CAS}$**
- **STANDARD 10% SUPPLIES (+12 V, +5 V, AND −5 V)**
- **FLEXIBLE TIMING WITH PAGE-MODE AND EXTENDED PAGE BOUNDARIES**
- **128-CYCLE $\overline{RAS}$-ONLY REFRESH**

Pin Names

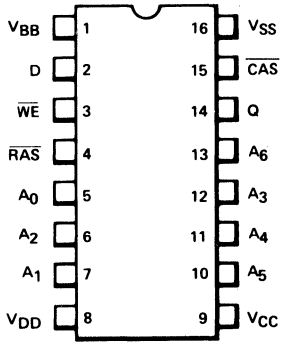
A_0-A_6	Address Inputs
D	Data Input
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{RAS}$	Row Address Strobe Input (Active LOW Clock)
$\overline{CAS}$	Column Address Strobe Input (Active LOW Clock)
Q	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	0 V Power Supply
V_{BB}	−5 V Power Supply
V_{DD}	+12 V Power Supply

Logic Symbol



V_{SS} = Pin 16
V_{CC} = Pin 9
V_{DD} = Pin 8
V_{BB} = Pin 1

Connection Diagram 16-Pin DIP



(Top View)

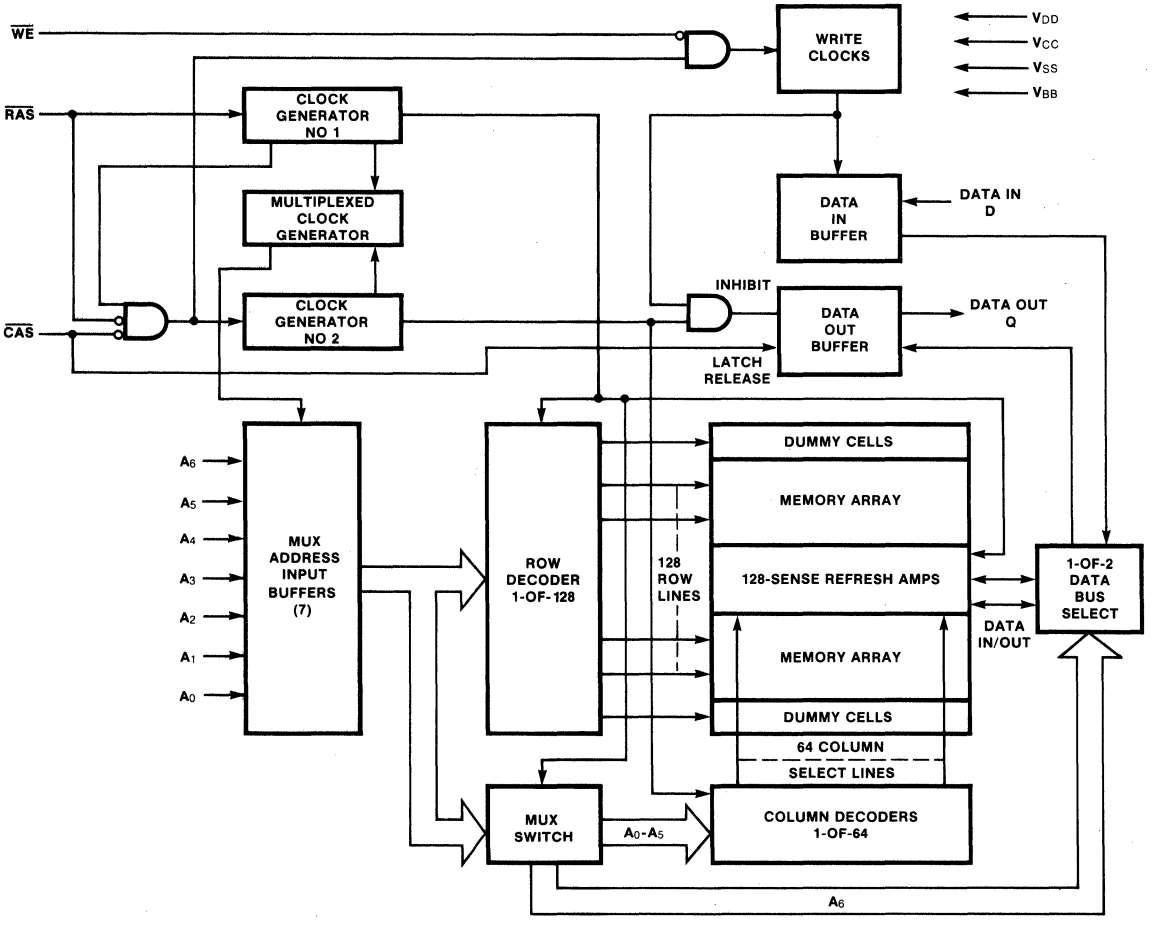
Package	Outline	Order Code
Ceramic DIP	2C	D
Plastic DIP	UB	P

Absolute Maximum Ratings

Voltage on Any Pin Relative to V_{BB} ($V_{SS} - V_{BB} \geq 4.5$ V)	−0.5 V to +20 V
Operating Temperature (Ambient)	0°C to 70°C
Storage Temperature (Ambient)	−65°C to +150°C
Power Dissipation	1 W
Voltage on V_{DD}, V_{CC} Supplies Relative to V_{SS}	−1.0 V to +15 V
Short-circuit Output Current	50 mA

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Functional Description

Addressing

The 14 address bits required to decode one-of-16,384 cell locations in the F4116 are entered using a 2-phase multiplexing operation; first, the 7-bit row address is entered followed by the 7-bit column address. First the 7-bit row address is applied to the seven address inputs of the F4116 and latched into the chip by Row Address Strobe ($\overline{RAS}$) which is the first of two externally applied TTL-level clocks. The second clock, Column Address Strobe ($\overline{CAS}$), subsequently latches the seven column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, trigger on-chip clock generators which control the internal sequencing of events on the chip. Advanced techniques used in handling the row and column address information allow the address multiplexing operation to be performed without lengthening the critical timing path governing the access time. The activation of $\overline{CAS}$ strobes the column address latch but this event as well as other internal events governed by the $\overline{CAS}$ clock generator may be inhibited until certain prerequisite events controlled by the $\overline{RAS}$ clock generator have occurred.

More specifically, a window of time exists, extending from $t_{RCD(min)}$ to $t_{RCD(max)}$ during which $\overline{CAS}$ may become active without impacting the access time. Stated another way, as long as $\overline{CAS}$ occurs during this window, the access time will be specified by t_{RAC}. If $\overline{CAS}$ occurs a certain delay after this window of time, the $\overline{RAS}$ clock generator no longer inhibits the $\overline{CAS}$ clock generator and the magnitude of this delay will add directly to the overall access time. This lengthened access time is now referenced to $\overline{CAS}$ rather than $\overline{RAS}$ and is lengthened by the amount of time that t_{RCD} exceeds the $t_{RCD(max)}$ limit. This gated-$\overline{CAS}$ feature allows greater flexibility since the $\overline{CAS}$ clock may be externally activated as soon as the hold time for the row address has been met and the address inputs have been changed from row address to column address information.

Page Mode Operation

The page-mode feature of the F4116 allows successive memory cycles accessing the same row in the memory matrix to be concatenated together in such a way that the common row address need be supplied only once. The result is faster access times with no corresponding increase in power. The page-mode option may be used in conjunction with any of the defined memory operations, and is accomplished by supplying the row address to the chip and holding $\overline{RAS}$ LOW throughout all subsequent memory cycles for which the row address is common.

Since $\overline{RAS}$ makes its initial negative transition only once, no additional dynamic power is dissipated due to $\overline{RAS}$ on any subsequent cycles performed within that row. The access and cycle times are also shortened since the time required to supply a row address is eliminated.

Data Input

In a write operation, the data to be input into memory is strobed into an on-chip register during $\overline{RAS}$ by a combination of $\overline{CAS}$ and Write Enable ($\overline{WE}$). The strobe is formed by the last of these two signals to make its negative transition. This presents several possibilities in how a write cycle may be performed. In an "early-write" cycle ($\overline{WE}$ active LOW before $\overline{CAS}$ goes LOW), Data In (D) is strobed by $\overline{CAS}$ and thus the set-up and hold times are referenced to this signal edge. If D is not yet valid at the time $\overline{CAS}$ becomes active (or if the cycle is a read-write or read-modify-write) then $\overline{WE}$ must be delayed. In this delayed-write mode, the D set-up and hold times are referenced to $\overline{WE}$ rather than $\overline{CAS}$. (See the timing diagrams.)

Data Output

The Data Out (Q) latch and buffer unconditionally assume the high-impedance state whenever $\overline{CAS}$ is HIGH, i.e., inactive. If the cycle being performed is a read, read-modify-write, or a delayed write cycle, then the Q latch and buffer will remain high impedance until the access time, after which Q will assume the value of the data read from the selected cell. This output data is of the same polarity (not inverted) as the input data and will remain valid as long as $\overline{CAS}$ is kept active, i.e., LOW. However, if the cycle is an "early-write" cycle or if the chip fails to receive both $\overline{RAS}$ and $\overline{CAS}$, then Q will remain high impedance throughout the cycle. This feature allows systems which write exclusively in the early-write mode to connect D and Q directly together.

Another advantage of this "unlatched output" feature is that OR-tied outputs in a memory matrix require no special action to be turned off. Unlike other types of RAMs which require a negative transition of $\overline{CAS}$ to become high impedance, the F4116's output is already high impedance whenever $\overline{CAS}$ is HIGH, i.e., inactive. This means that $\overline{CAS}$ need not be supplied to unused devices and therefore may be used for device selection. Thus a reduction in external decoding logic is possible by using both $\overline{RAS}$ and $\overline{CAS}$ in a 2-dimensional decoding/selection scheme.

$\overline{RAS}$ and $\overline{CAS}$ Clock Conditions

$\overline{RAS}$ and $\overline{CAS}$ cycle	Device active
$\overline{RAS}$ only cycle	Device deselected, refresh
$\overline{CAS}$ only cycle	Device deselected
Neither $\overline{RAS}$ nor $\overline{CAS}$	Device deselected, standby

Extended Page Boundary

A further implication of using both $\overline{RAS}$ and $\overline{CAS}$ for device decoding/selection is in extending page boundaries for page-mode operation. If only $\overline{RAS}$ is decoded, then any given page is limited to only 128 different column addresses within that page (i.e., seven column address bits correspond to $2^7 = 128$ column addresses). Therefore, for memory systems using more than 16K words of data, page boundaries may be extended from 128 addresses per page up to any multiple of 128 addresses merely by decoding which 16K memory bank also gets a $\overline{CAS}$ (subject to $t_{RAS(max)}$ limitation). This is accomplished by supplying $\overline{RAS}$ to all devices in order to latch in the row address information and then decoding which bank of 16K words also gets $\overline{CAS}$. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ will respond with a valid memory cycle.

Input/Output Levels

All inputs, including the two address strobes, interface directly with TTL. The high-impedance, low-capacitance input characteristics simplify input driver selection by allowing use of standard logic elements rather than specially designed driver elements. Termination resistors are normally required in a system to prevent ringing due to line inductance and reflections. In high-speed memory systems, transmission line techniques must be employed on the signal lines to achieve optimum system speeds. Series termination may by employed at some degradation of system speed. The 3-state output buffer is a low impedance to V_{CC} for logic "1" and low impedance to V_{SS} for logic "0". The effective resistance to V_{CC} is 420 Ω maximum and 135 Ω typically. The effective resistance to V_{SS} is 95 Ω maximum and 35 Ω typically.

Refresh

The matrix of 128 x 128 memory cells in the F4116 is refreshed by executing a memory cycle at each of the 128 row addresses within each interval of 2 ms or less. Although any cycle in which $\overline{RAS}$ occurs accomplishes a refresh operation, the refresh is most easily accomplished in the $\overline{RAS}$-only-refresh mode. This type of refresh operation results in decreased power dissipation, since $\overline{CAS}$ remains inactive.

Power Dissipation/Standby

Since the F4116 uses dynamic memory cells, this means that most of the dissipated power is a result of an address strobe edge. There is, however, a small dc component of dissipated power that is associated with the precharging of the sense amplifiers. Thus, the total power dissipated is a function of both operating frequency and duty cycle. Typically, the power is 350 mW at 1 μs cycle time with a worst case power of less than 462 mW at 375 ns cycle time. To reduce overall system power during standby, $\overline{RAS}$-only-refresh cycles should be performed with $\overline{CAS}$ held HIGH.

The V_{CC} supply is not used in the internal memory operations of the F4116, but rather is used only at the output buffer and thus, for some applications, may be powered from the supply voltage of the logic to which the chip's output is interfaced. This means that I_{CC}, the current drawn from the V_{CC} supply, is a function of output loading. During battery standby operation, the V_{CC} pin may be unpowered, if desired, without affecting the refresh operation. This allows all system logic, except the $\overline{RAS}$ timing circuitry and the refresh address logic, to be turned off during battery standby to conserve power.

Memory Power Up

The F4116 requires no particular power supply sequencing as long as the absolute maximum rating conditions are observed. However, in order to insure compliance with the absolute maximum ratings, by providing larger voltage margins, it is recommended that power supplies be sequenced at power-up such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

Under system failure conditions in which one or more supplies exceed the specified limits, significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and $\overline{CAS}$ to the inactive state.

After power is applied to the device, the F4116 requires several cycles before proper device operation is achieved. Any eight cycles which perform refresh are adequate for this purpose.

DC Requirements T_A = 0°C to +70°C (See Notes 1 and 2)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{DD}	Supply Voltage	10.8	12	13.2	V	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	Note 5
V_{SS}	Supply Voltage	0	0	0	V	
V_{BB}	Supply Voltage	−5.7	−5.0	−4.5	V	
V_{IHC}	Input HIGH Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	2.4		7.0	V	
V_{IH}	Input HIGH Voltage, All Inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	2.2		7.0	V	
V_{IL}	Input LOW Voltage, All Inputs	−1.0		0.8	V	

DC Characteristics Over full range of voltage and temperature

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{OH}	Output HIGH Voltage		2.4			V	I_{OUT} = −5.0 mA, Note 5
V_{OL}	Output LOW Voltage				0.4	V	I_{OUT} = 4.2 mA, Note 5
I_{DD}	Average V_{DD} Current	Normal Operation			35	mA	For F4116-4 Refresh I_{DD} = 27 mA Max. Note 3
		Standby			1.5	mA	
		Refresh			25	mA	
		Page Mode			27	mA	
I_{CC}	Average V_{CC} Current	Normal Operation/ Page Mode					Note 4
		Standby/Refresh	−10		10	μA	
I_{BB}	Average V_{BB} Current	Normal Operation/ Refresh/Page Mode			200	μA	
		Standby			100	μA	
I_{IN}	Input Leakage Current (Any Input)		−10		10	μA	
I_{OUT}	Output Leakage Current		−10		10	μA	
C_{IN1}	Input Capacitance, A_0-A_6, D			4.0	5.0	pF	Note 6
C_{IN2}	Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$			8.0	10	pF	Note 6
C_{OUT}	Output Capacitance, Q			5.0	7.0	pF	$\overline{CAS}$ = V_{IHC}

Notes on following pages.

Recommended ac Operating Conditions Over full range of voltage and temperature

Symbol	Characteristic	F4116-2		F4116-3		F4116-4		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	320		375		410		ns	7
t_{RWC}	Read-Write Cycle Time	320		375		425		ns	7
t_{RMW}	Read Modify Write Cycle Time	320		405		500		ns	7
t_{PC}	Page Mode Cycle Time	170		225		275		ns	7
t_{RAC}	Access Time from $\overline{RAS}$		150		200		250	ns	8, 10
t_{CAC}	Access Time from $\overline{CAS}$		100		135		165	ns	9, 10
t_{OFF}	Output Buffer Turn-off Delay	0	40	0	50	0	60	ns	11
t_{RP}	$\overline{RAS}$ Precharge Time	100		120		150		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10,000	200	10,000	250	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	100		135		165		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	150		200		250		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	100	10,000	135	10,000	165	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	65	35	85	ns	12
t_{ASR}	Row Address Set-up Time	0		0		0			
t_{RAH}	Row Address Hold Time	20		25		35		ns	
t_{ASC}	Column Address Set-up Time	−10		−10		−10		ns	
t_{CAH}	Column Address Hold Time	45		55		75		ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_T	Transition Time (Rise and Fall)	3.0	35	3.0	50	3.0	50	ns	13
t_{RCS}	Read Command Set-up Time (RMW)	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{WCH}	Write Command Hold Time	45		55		75		ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{WCS}	Write Command Set-up Time	−20		−20		−20		ns	14
t_{WP}	Write Command Pulse Width	45		55		75		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	50		70		85		ns	15
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	50		70		85		ns	15
t_{DS}	Data In Set-up Time	0		0		0		ns	16
t_{DH}	Data In Hold Time	45		55		75		ns	16
t_{DHR}	Data In Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	−20		−20		−20		ns	

Notes on following page.

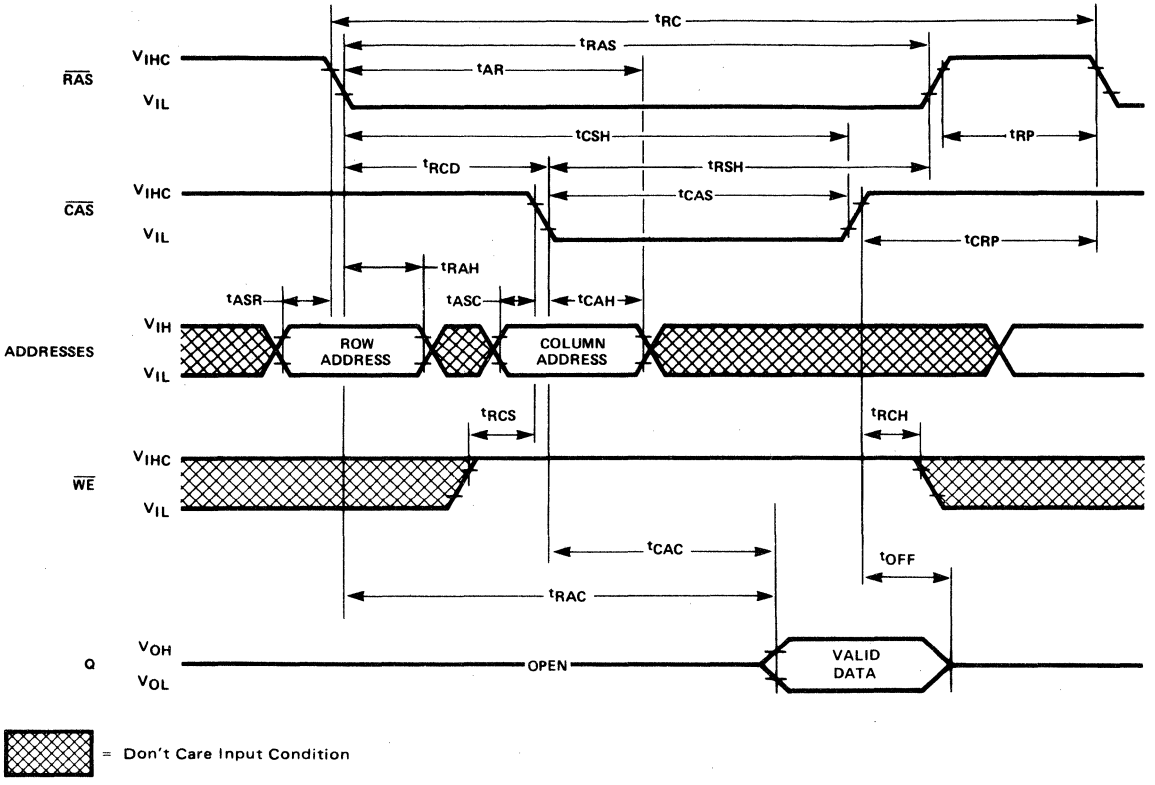
Recommended ac Operating Conditions (Cont'd)

Symbol	Characteristic	F4116-2		F4116-3		F4116-4		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{CP}	$\overline{CAS}$ Precharge Time (Page-Mode)	60		80		100		ns	
t_{RF}	Refresh Period		2.0		2.0		2.0	ms	
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	60		80		90		ns	17
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	110		145		175		ns	17

Notes

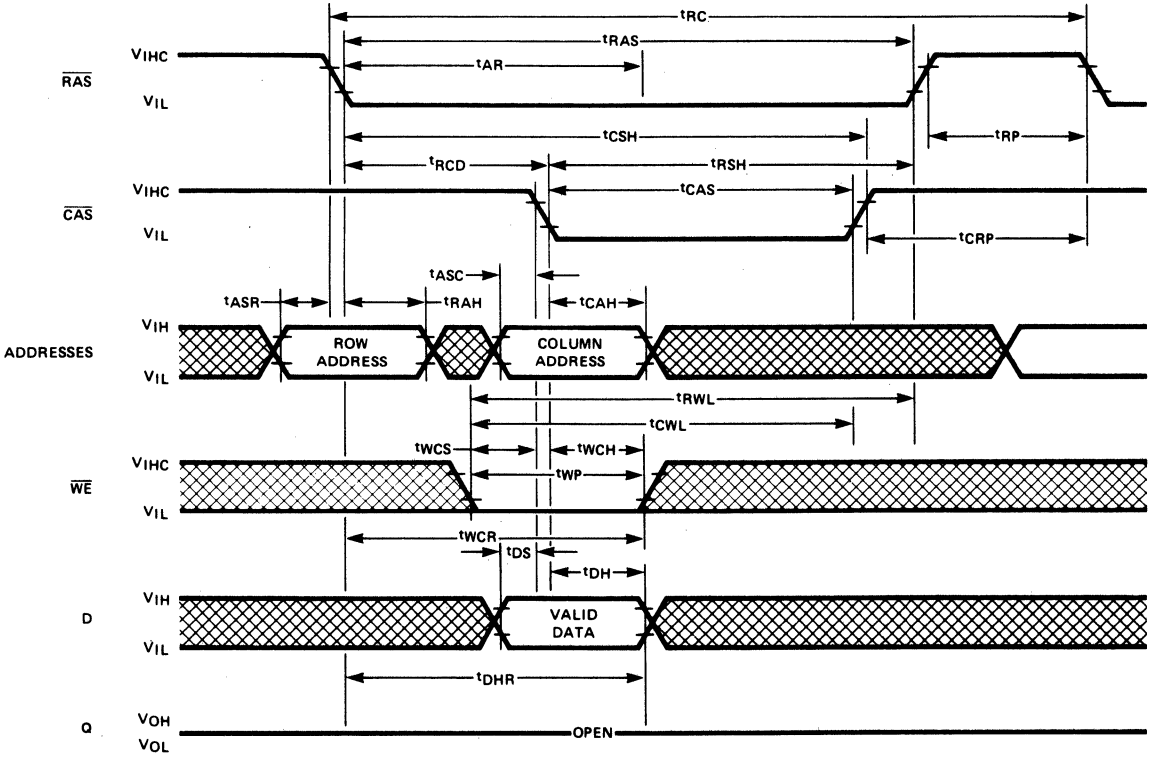
1. The ambient temperature (T_A) is specified here for operation at frequencies up to that frequency determined by the minimum cycle time. Operation at high cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided ac operating parameters are met.
2. All voltages are referenced to V_{SS} = 0 V.
3. I_{DD} depends on frequency of operation. Maximum current is measured at the fastest cycle rate.
4. I_{CC} depends upon output loading. The V_{CC} is connected to the output buffer only. During readout of HIGH level data, V_{CC} is connected through a low impedance (135 Ω typ) to Data Out. At other times I_{CC} consists of leakage currents only.
5. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of reducing power in the standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the $V_{OH(min)}$ specification is not guaranteed in this mode.
6. Effective capacitance calculated from the equation $C = I\frac{\Delta t}{\Delta V}$ with ΔV = 3 V and power supplies at normal levels.
7. The specifications for $t_{RC(min)}$, $t_{RWC(min)}$, $t_{RMW(min)}$ and $t_{PC(min)}$ are used only to indicate cycle time at which proper operation over full temperature range (0°C ≤ T_A ≤ 70°C) is assured. All transition times, t_T, are assumed to be 5 ns.
8. Assumes that $t_{RCD} \leq t_{RCD(max)}$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
10. Measured with a load equivalent to two TTL loads and 100 pF.
11. $t_{OFF(max)}$ defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.
12. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
13. $V_{IHC(min)}$ or $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}. Composite timing parameters (such as cycle times) assume 5 ns transition times.
14. t_{WCS} is a restrictive operating parameter. If $t_{WCS} \geq t_{WCS(min)}$, the cycle is an early write cycle and the Data Out pin will remain open circuit (high impedance) throughout the entire cycle, otherwise the cycle is a delayed write cycle.
15. The parameters t_{RWL} and t_{CWL} reference $\overline{WE}$ (for a read-modify-write cycle) to either $\overline{RAS}$ or $\overline{CAS}$ respectively, whichever is the first to go HIGH.
16. t_{DS} and t_{DH} are referenced to the leading edge of $\overline{CAS}$ in early write cycles, and to the leading edge of $\overline{WE}$ in delayed write or read-modify-write cycles.
17. t_{RWD} and t_{CWD} are restrictive operating parameters due to the following characteristics:
    If $t_{CWD} < t_{CWD(min)}$, the Data Out will be indeterminate.
    If $t_{CWD} \geq t_{CWD(min)}$, the Data Out will contain the data read from the selected cell.

Timing Diagrams
Read Cycle

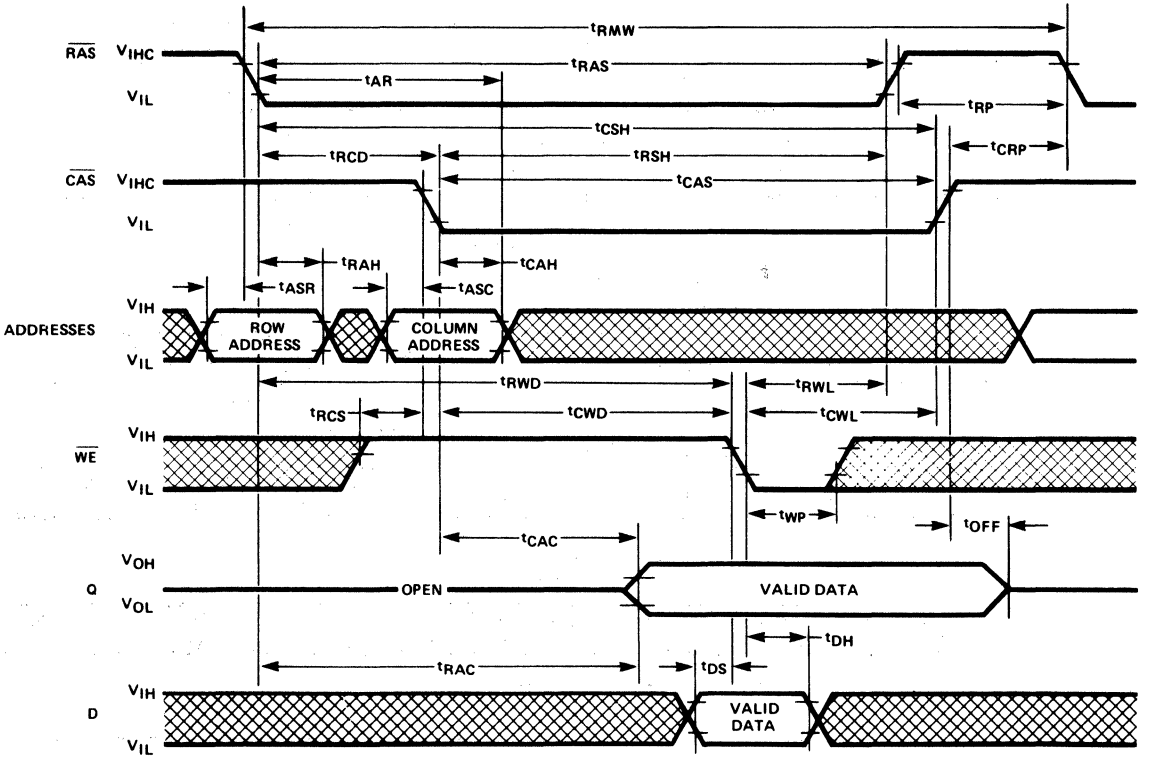


= Don't Care Input Condition

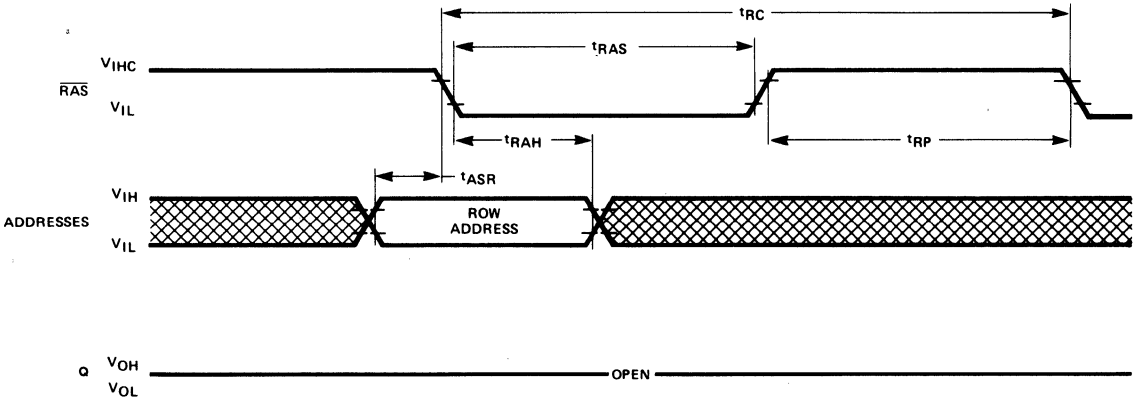
Write Cycle (Early Write)



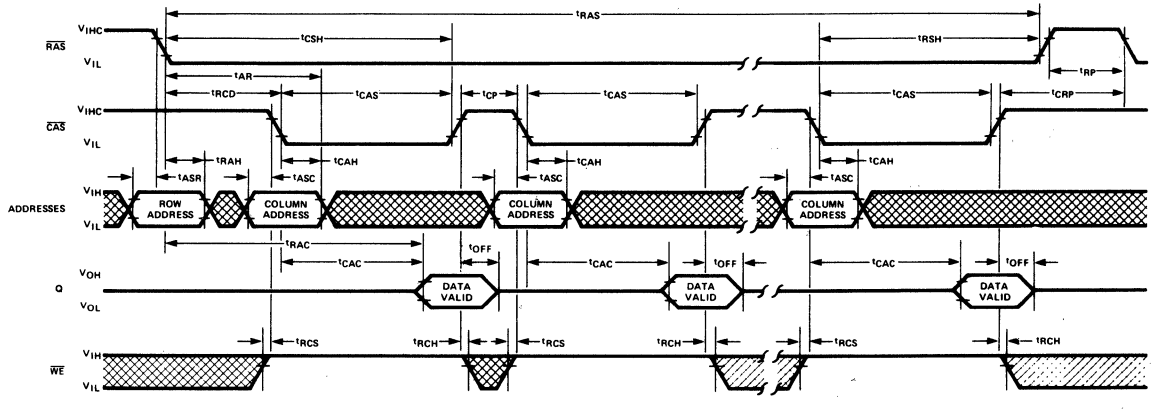
Read-Write/Read-Modify-Write Cycle



"$\overline{RAS}$ ONLY" Refresh Cycle

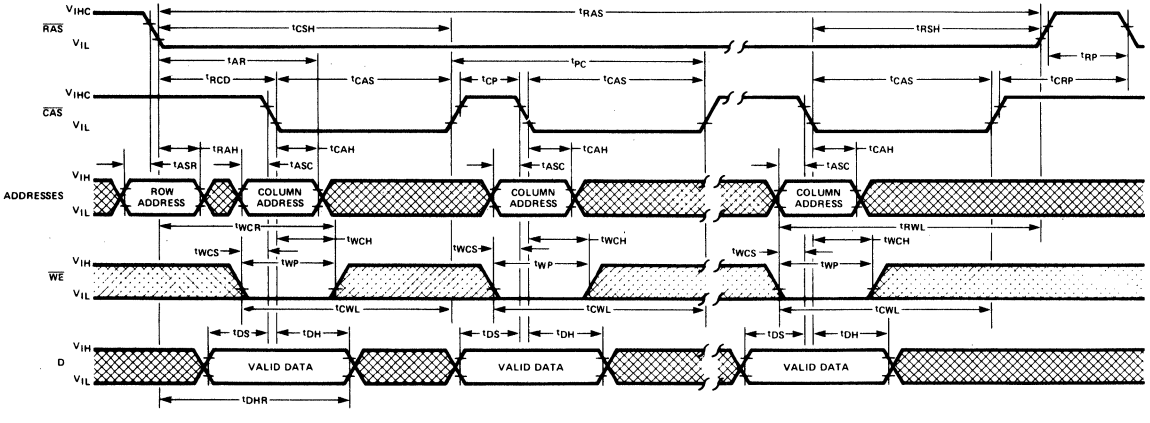


Page Mode Read Cycle

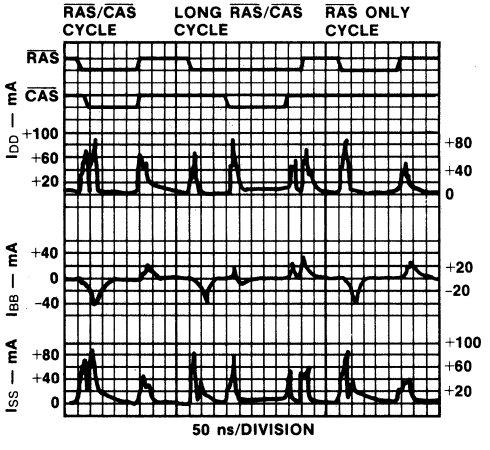


= Don't Care Input Condition

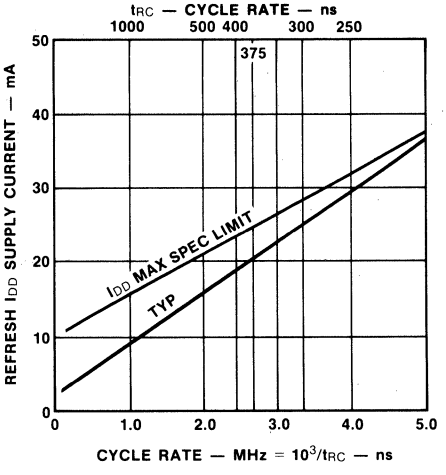
Page Mode Write Cycle (Early Write)



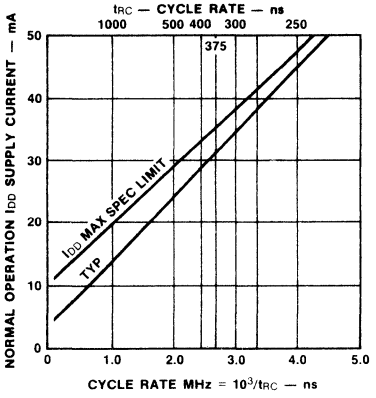
Typical Current Waveforms



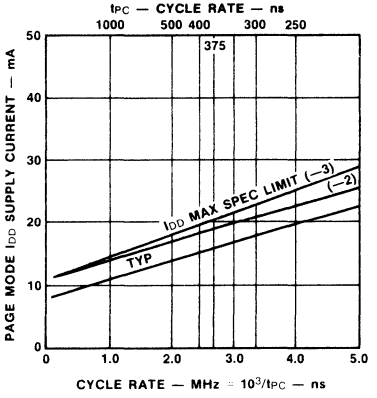
Refresh I_{DD} vs Cycle Rate



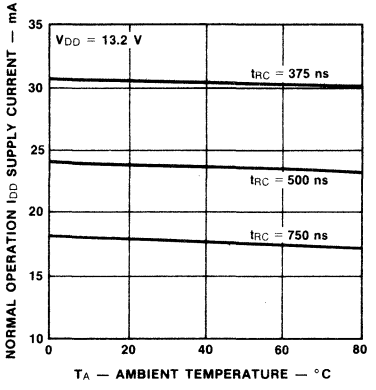
Normal Operation I_{DD} vs Cycle Rate



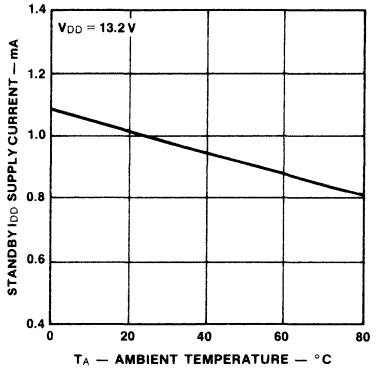
Page Mode I_{DD} vs Cycle Rate



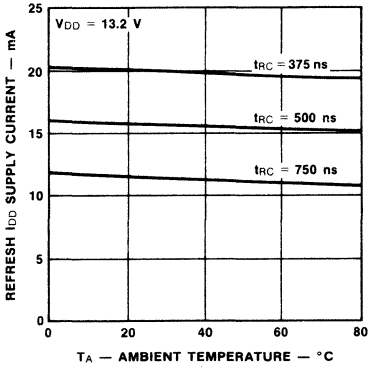
Normal Operation I_{DD} vs Ambient Temperature



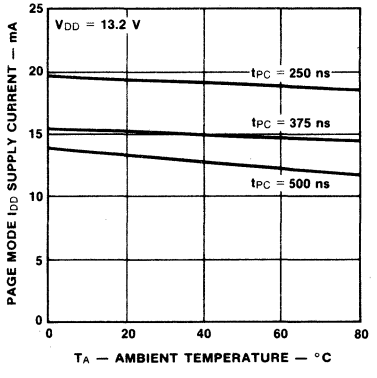
Standby I_{DD} vs Ambient Temperature



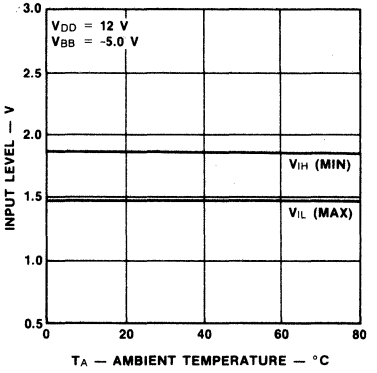
Refresh I_{DD} vs Ambient Temperature



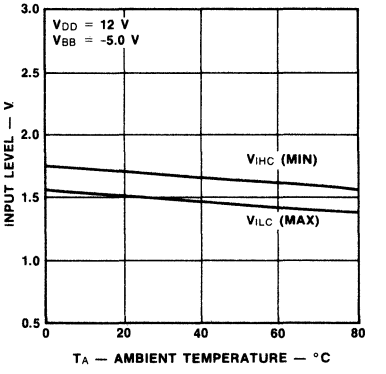
Page Mode I_{DD} vs Ambient Temperature



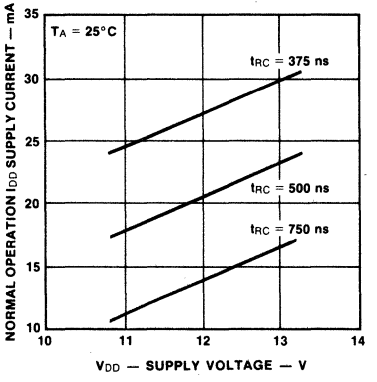
Address Data Input Levels vs T_A



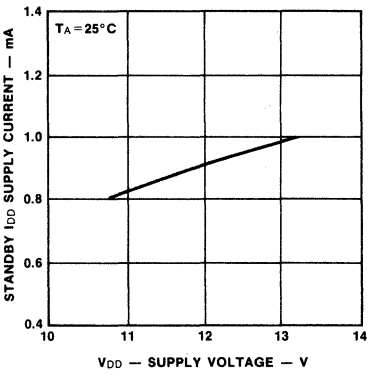
Clock Input Levels vs T_A



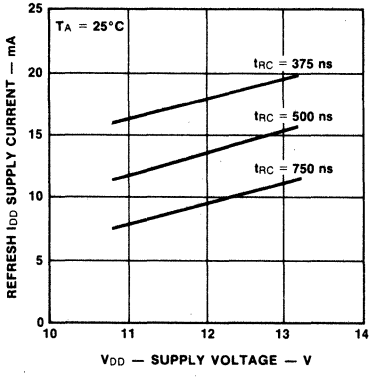
Normal Operation I_{DD} vs V_{DD}



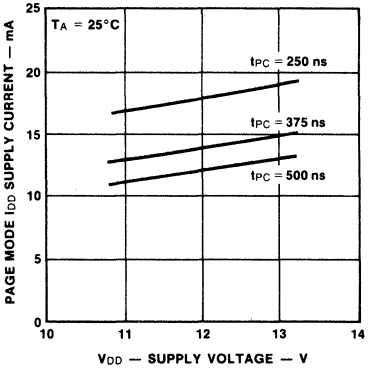
Standby I_{DD} vs V_{DD}



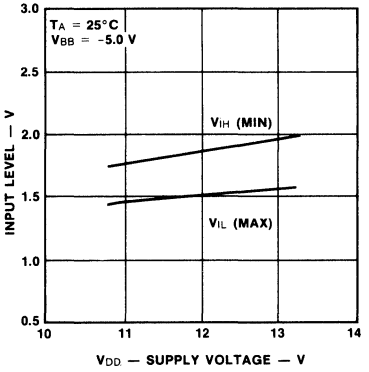
Refresh I_{DD} vs V_{DD}



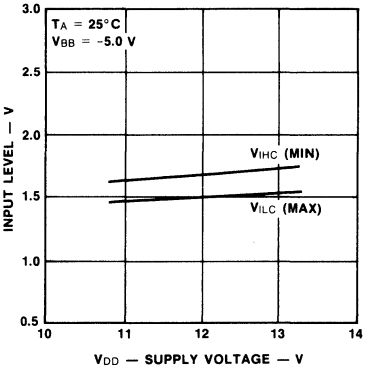
Page Mode I_{DD} vs V_{DD}



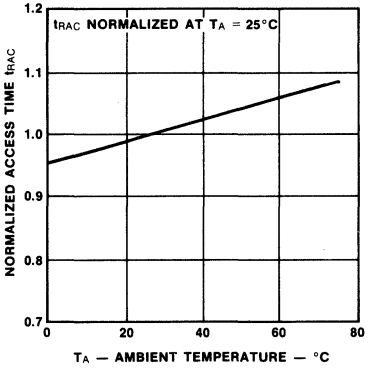
Address Data Input Levels vs V_{DD}



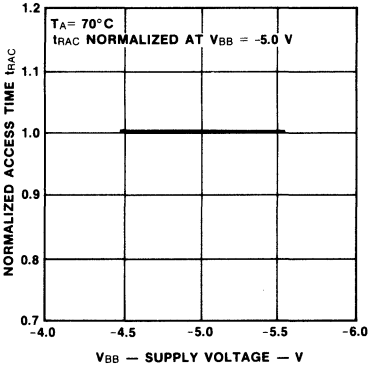
Clock Input Level vs V_{DD}



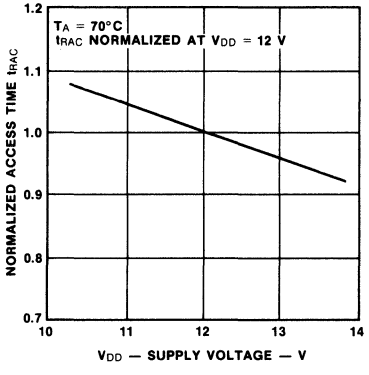
Access Time (Normalized) vs T_A



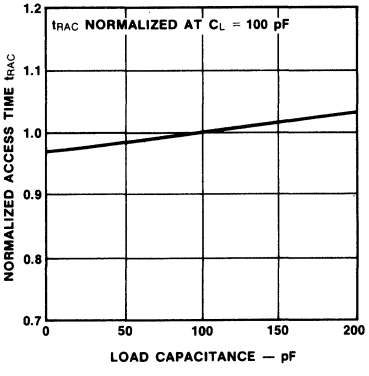
Access Time (Normalized) vs V_{BB}



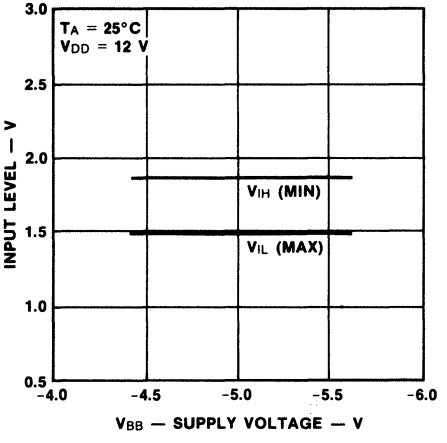
Access Time (Normalized) vs V_{DD}



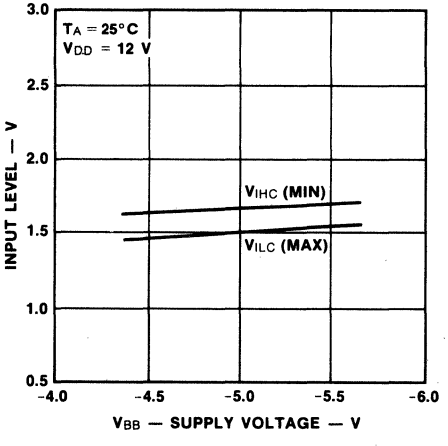
Normalized Access Time vs Load Capacitance



Address and Data Input Levels vs V_{BB}



Clock Input Level vs V_{BB}



Applications and Testing

F4116 Data Scramble

In order to assist engineers in testing the F4116 16,384 x 1-bit dynamic Random Access Memory, information concerning the internal polarity and location of the stored data is provided as follows. *Figure 1* shows a block diagram of the various figures and how they relate to each other.

Address Scrambling

The relationship of the external (data sheet) address to the actual internal row or column address is shown in *Figure 2*. This information may be required to locate a specific location on the chip, when only its external pin address is known. The actual chip addresses (converted to decimal) are shown in *Figure 3*.

Figure 4 shows the external logic necessary to descramble the F4116 internal logic shown in *Figure 2*. For example, addressing column "0", via the system address inputs (A_0-A_6 = LOW), selects the actual chip column 0 shown in *Figure 3*. Setting a "1" on the system column address inputs (0000001), selects the adjacent actual column "1" on the chip. This correspondence holds for all rows and columns when using the transformation supplied in *Figure 4*.

The tables provided in *Figures 5* and *6* show the relationship of the system address (decimal) to the external (data sheet) address converted to octal. In other words, *Figures 5* and *6* are simply truth tables for the logic shown in *Figure 4*.

Data Inversion

Since the F4116 employs balanced sense amps, it is necessary to store some of the data in inverted form. This is decoded internally so it does not appear to the user, and need only be considered when testing. The input and output EXOR gates shown in *Figure 1* provide the proper inversions necessary to have all data written in the same polarity. It should be noted that A_6, shown in *Figure 1*, is referenced to the most significant bit of the system row address. This is because the inversion is only related to the row address and must be independent of the multiplexing operation.

Fig. 1 Relationship of various scrambling and inversion networks

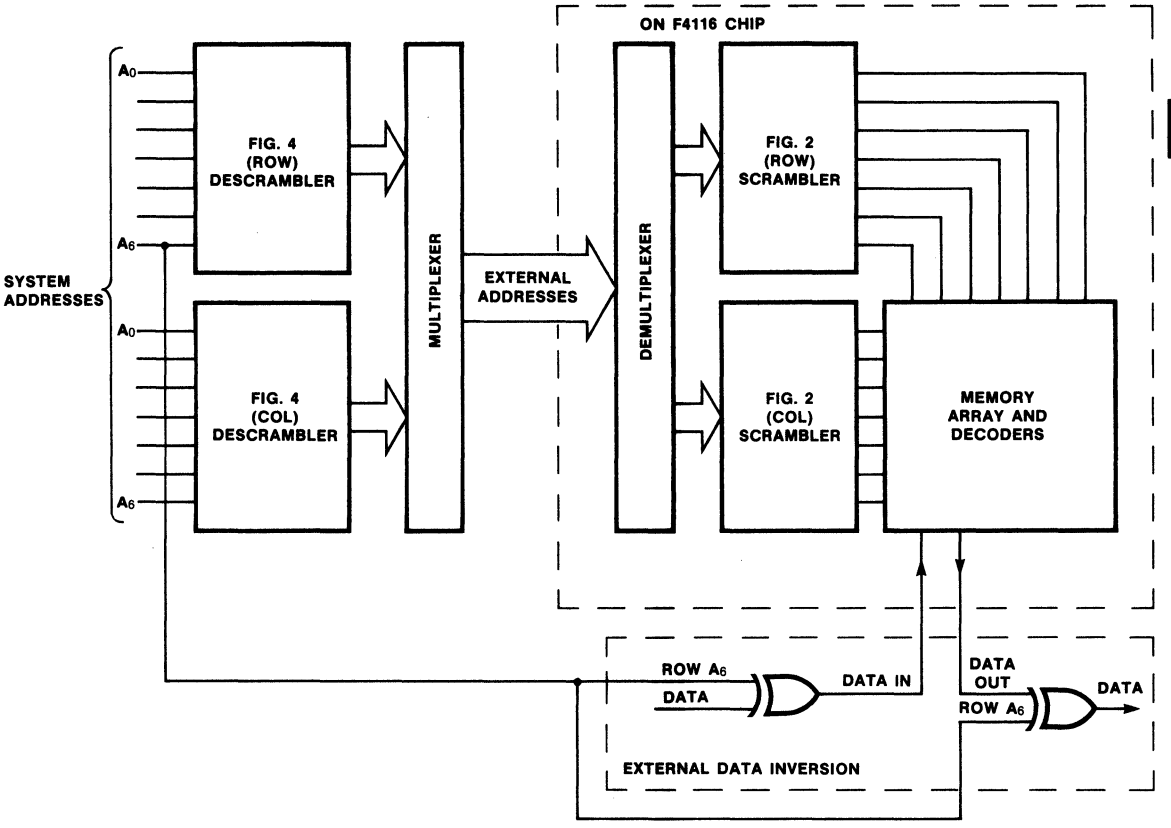


Fig. 2 Relationship of external addresses to actual row and column positions (multiplexer not shown). Refer to *Figure 3* for actual positions converted to decimal.

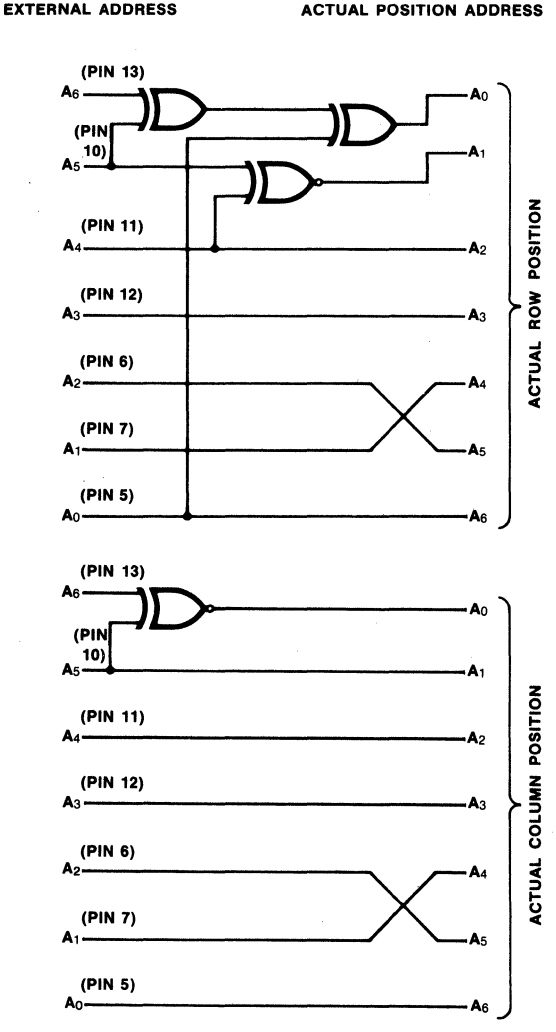
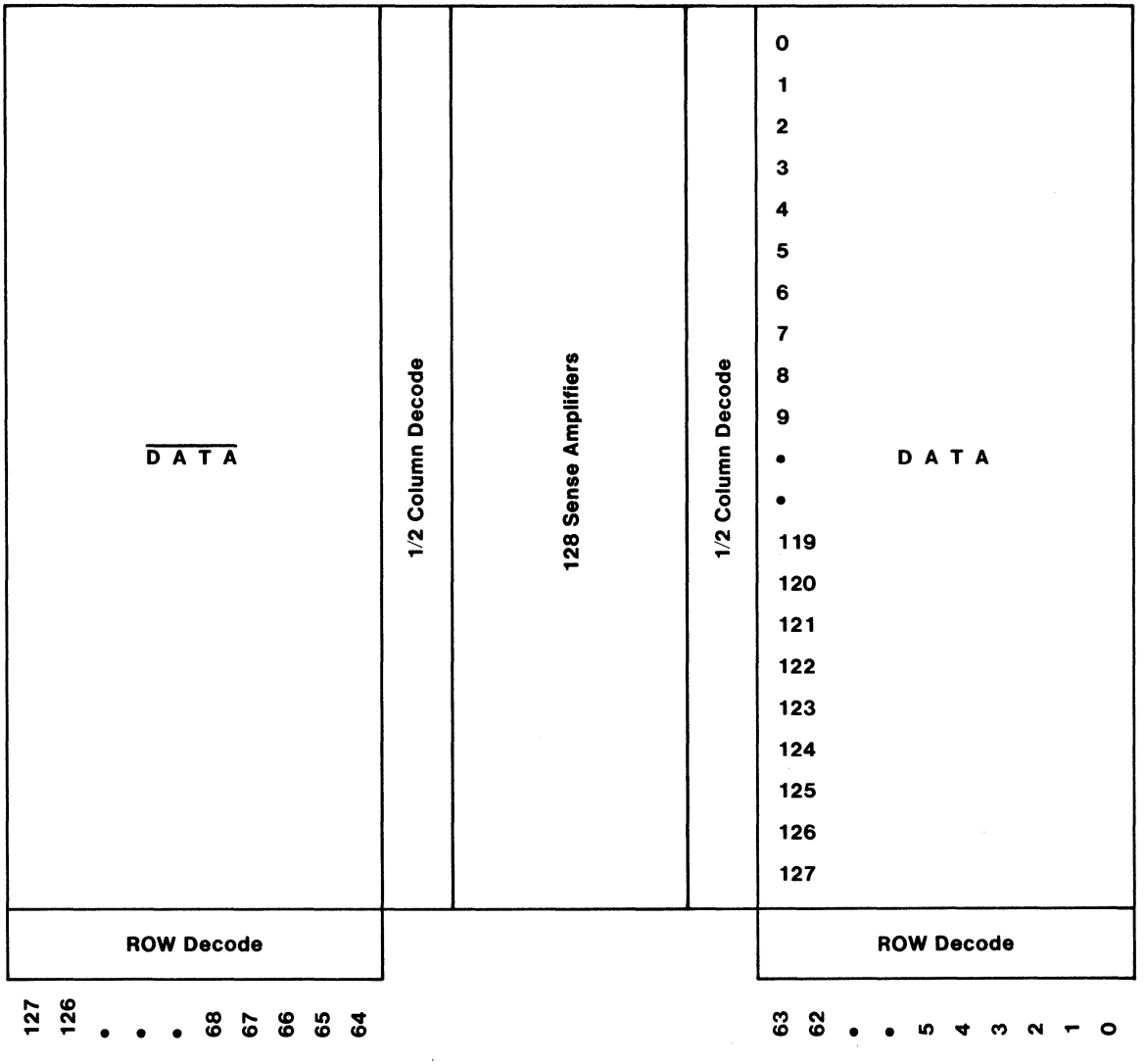
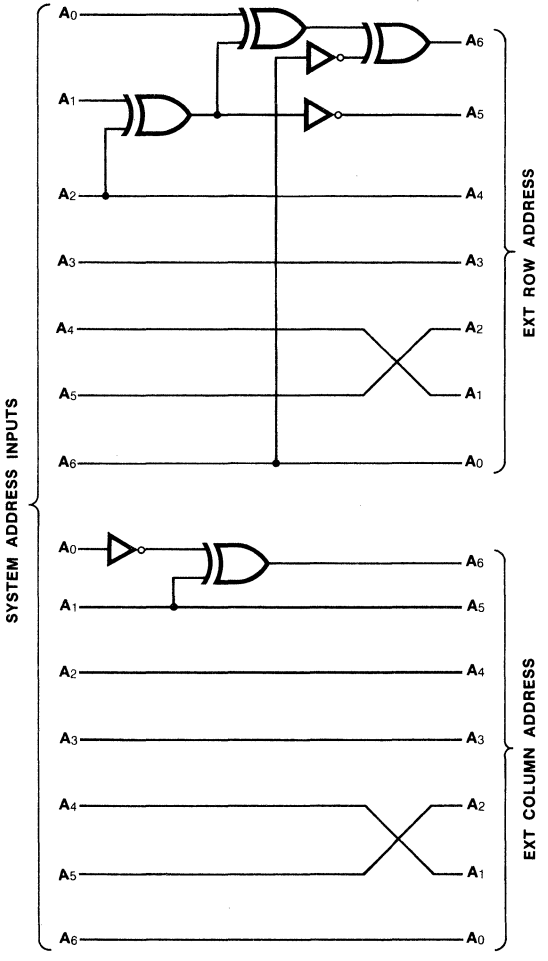


Fig. 3 F4116 Bit Map



Actual column and row position addresses converted to decimal. Conversion to the external address is explained in the text.

Fig. 4 External address transformation required to descramble F4116 internal decoder shown in *Figure 1* (multiplexer not shown).



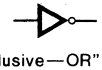
Note
The logic symbols  and  are used solely to indicate the logic function "Exclusive—OR" and "NOT", respectively. The above figure is not a suggested implementation of logic.

Fig. 5 System Row Address (Decimal) To External Address (Octal) Conversion Table

System Row Address	External Address	System Row Address	External Address	System Row Address	External Address	System Row Address	External Address
0	1 4 0	32	1 4 4	64	0 4 1	96	0 4 5
1	0 4 0	33	0 4 4	65	1 4 1	97	1 4 5
2	0 0 0	34	0 0 4	66	1 0 1	98	1 0 5
3	1 0 0	35	1 0 4	67	0 0 1	99	0 0 5
4	0 2 0	36	0 2 4	68	1 2 1	100	1 2 5
5	1 2 0	37	1 2 4	69	0 2 1	101	0 2 5
6	1 6 0	38	1 6 4	70	0 6 1	102	0 6 5
7	0 6 0	39	0 6 4	71	1 6 1	103	1 6 5
8	1 5 0	40	1 5 4	72	0 5 1	104	0 5 5
9	0 5 0	41	0 5 4	73	1 5 1	105	1 5 5
10	0 1 0	42	0 1 4	74	1 1 1	106	1 1 5
11	1 1 0	43	1 1 4	75	0 1 1	107	0 1 5
12	0 3 0	44	0 3 4	76	1 3 1	108	1 3 5
13	1 3 0	45	1 3 4	77	0 3 1	109	0 3 5
14	1 7 0	46	1 7 4	78	0 7 1	110	0 7 5
15	0 7 0	47	0 7 4	79	1 7 1	111	1 7 5
16	1 4 2	48	1 4 6	80	0 4 3	112	0 4 7
17	0 4 2	49	0 4 6	81	1 4 3	113	1 4 7
18	0 0 2	50	0 0 6	82	1 0 3	114	1 0 7
19	1 0 2	51	1 0 0	83	0 0 3	115	0 0 7
20	0 2 2	52	0 2 6	84	1 2 3	116	1 2 7
21	1 2 2	53	1 2 6	85	0 2 3	117	0 2 7
22	1 6 2	54	1 6 6	86	0 6 3	118	0 6 7
23	0 6 2	55	0 6 6	87	1 6 3	119	1 6 7
24	1 5 2	56	1 5 6	88	0 5 3	120	0 5 7
25	0 5 2	57	0 5 6	89	1 5 3	121	1 5 7
26	0 1 2	58	0 1 6	90	1 1 3	122	1 1 7
27	1 1 2	59	1 1 6	91	0 1 3	123	0 1 7
28	0 3 2	60	0 3 6	92	1 3 3	124	1 3 7
29	1 3 2	61	1 3 6	93	0 3 3	125	0 3 7
30	1 7 2	62	1 7 6	94	0 7 3	126	0 7 7
31	0 7 2	63	0 7 6	95	1 7 3	127	1 7 7

Fig. 6 System Column Address (Decimal) To External Address (Octal) Conversion Table

System Column Address	External Address	System Column Address	External Address	System Column Address	External Address	System Column Address	External Address
0	1 0 0	32	1 0 4	64	1 0 1	96	1 0 5
1	0 0 0	33	0 0 4	65	0 0 1	97	0 0 5
2	0 4 0	34	0 4 4	66	0 4 1	98	0 4 5
3	1 4 0	35	1 4 4	67	1 4 1	99	1 4 5
4	1 2 0	36	1 2 4	68	1 2 1	100	1 2 5
5	0 2 0	37	0 2 4	69	0 2 1	101	0 2 5
6	0 6 0	38	0 6 4	70	0 6 1	102	0 6 5
7	1 6 0	39	1 6 4	71	1 6 1	103	1 6 5
8	1 1 0	40	1 1 4	72	1 1 1	104	1 1 5
9	0 1 0	41	0 1 4	73	0 1 1	105	0 1 5
10	0 5 0	42	0 5 4	74	0 5 1	106	0 5 5
11	1 5 0	43	1 5 4	75	1 5 1	107	1 5 5
12	1 3 0	44	1 3 4	76	1 3 1	108	1 3 5
13	0 3 0	45	0 3 4	77	0 3 1	109	0 3 5
14	0 7 0	46	0 7 4	78	0 7 1	110	0 7 5
15	1 7 0	47	1 7 4	79	1 7 1	111	1 7 5
16	1 0 2	48	1 0 6	80	1 0 3	112	1 0 7
17	0 0 2	49	0 0 6	81	0 0 3	113	0 0 7
18	0 4 2	50	0 4 6	82	0 4 3	114	0 4 7
19	1 4 2	51	1 4 6	83	1 4 3	115	1 4 7
20	1 2 2	52	1 2 6	84	1 2 3	116	1 2 7
21	0 2 2	53	0 2 6	85	0 2 3	117	0 2 7
22	0 6 2	54	0 6 6	86	0 6 3	118	0 6 7
23	1 6 2	55	1 6 6	87	1 6 3	119	1 6 7
24	1 1 2	56	1 1 6	88	1 1 3	120	1 1 7
25	0 1 2	57	0 1 6	89	0 1 3	121	0 1 7
26	0 5 2	58	0 5 6	90	0 5 3	122	0 5 7
27	1 5 2	59	1 5 6	91	1 5 3	123	1 5 7
28	1 3 2	60	1 3 6	92	1 3 3	124	1 3 7
29	0 3 2	61	0 3 6	93	0 3 3	125	0 3 7
30	0 7 2	62	0 7 6	94	0 7 3	126	0 7 7
31	1 7 2	63	1 7 6	95	1 7 3	127	1 7 7

F4164
65,536 x 1
Dynamic RAM

MOS Memory Products

Description

The F4164 is a dynamic Random Access Memory (RAM) circuit organized as 65,536 single-bit words. This memory uses the Fairchild advanced double poly NMOS, Isoplanar-H™ process which allows volume manufacture of reliable, high density memory products.

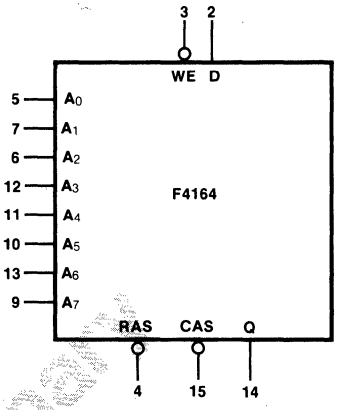
Innovative architecture and circuit design provide significant user benefits including wide operating margins, low power dissipation and excellent noise characteristics. Double cruciform architecture minimizes signal path lengths to improve noise margin and reduce propagation delays. A multiplexed sense amplifier scheme halves the number of sense amplifiers and the bit-line to cell capacitance ratio; this simultaneously reduces power consumption and improves signal sensing margins. Full-sized reference cells provide good margins and control. Low capacitance TTL-compatible inputs with overshoot and anti-static protection insure data and address input integrity.

- **INDUSTRY STANDARD 16-PIN DIP WITH PIN 1 NOT CONNECTED (NC)**
- **LOW CAPACITANCE TTL-COMPATIBLE INPUTS WITH OVERSHOOT AND ANTI-STATIC PROTECTION**
- **COMMON I/O CAPABILITY**
- **STANDARD 5 V ±10% SINGLE POWER SUPPLY REQUIREMENT**
- **LOW POWER**
  209 mW ACTIVE (MAX)
  19.3 mW STANDBY (MAX)
- **FAST ACCESS TIME — 120 ns, 150 ns or 200 ns**
- **READ-MODIFY-WRITE, RAS-ONLY REFRESH AND PAGE MODE CAPABILITY**
- **OUTPUT UNLATCHED AT CYCLE END ALLOWS FOR PAGE BOUNDARY EXTENSION AND TWO-DIMENSIONAL CHIP SELECTION**

Pin Names

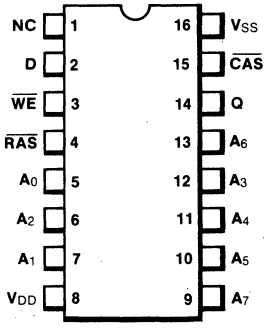
A_0-A_7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D	Data Input
Q	Data Output

Logic Symbol



V_{SS} = Pin 16
V_{DD} = Pin 8

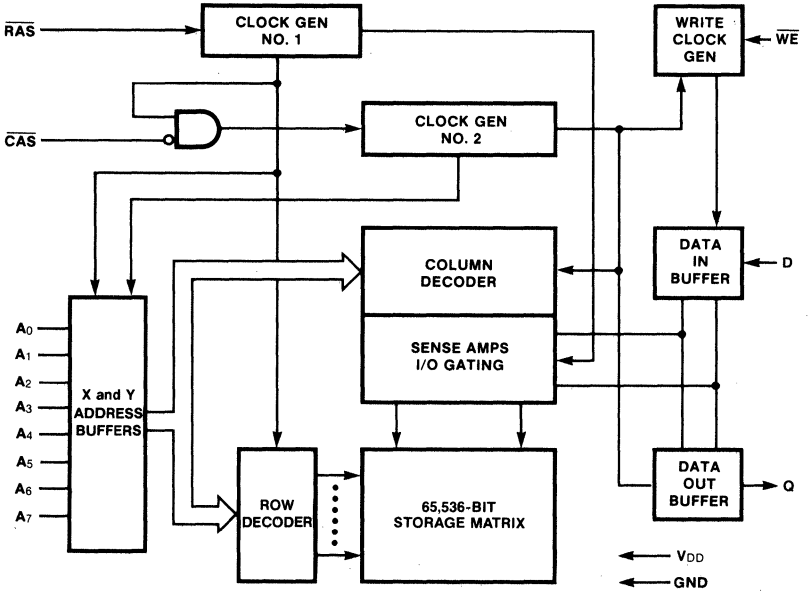
Connection Diagram 16-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	WC	D

Block Diagram



Functional Description

Memory Cycles

The F4164 operates in several modes which reflect various application considerations, some examples of which follow.

Random Read or Write Cycle

This mode implements standard Read or Write operation. Addresses are entered in two consecutive 8-bit bytes synchronized with $\overline{RAS}$ and $\overline{CAS}$. In the Read case, $\overline{WE}$ should be HIGH before the falling edge of $\overline{CAS}$. During Early-Write operations, $\overline{WE}$ falls before $\overline{CAS}$, causing the output to remain in the high impedance state. This output mode is useful if the RAM Data input (D) and Data output (Q) pins are to be wired in common as a bidirectional data bus.

Read-Write Cycle

The Read-Write mode is used when new data is to be written into the same cell location from which the content is currently being read. Since no address change is required, this mode provides a much faster Read-Write cycle by allowing the overhead associated with the address decoder and precharge to be amortized over two operations. In general, t_{RWC} is significantly less than twice t_{RC}. In this mode the new input data is not a function of the currently stored data. For that reason the cycle time is not limited by access time (t_{RAC}), but by Write considerations such as t_{RWD} and t_{RWL}.

Read-Modify-Write Cycle

The Read-Modify-Write cycle is used when the data from the cell at the current address is used to derive new data for writing back into that cell, such as in error correction schemes. In this mode, cycle time is dependent upon both read access time and write-related parameters.

Addressing

The 16 address bits required to decode one-of-65,536 storage cell locations in the F4164 are entered using a two-phase multiplexing operation. First, the 8-bit row address is applied to the eight Address inputs of the F4164 and latched into the chip by Row Address Strobe ($\overline{RAS}$). Next, the 8-bit column address is presented to the Address inputs and latched by the Column Address Strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edge of $\overline{RAS}$ or $\overline{CAS}$.

$\overline{CAS}$ is internally inhibited by a signal derived from $\overline{RAS}$. This feature prevents column addresses from being strobed onto the chip before row address dependent operations have been completed.

The gated-$\overline{CAS}$ feature allows $\overline{CAS}$ to occur any time before $t_{RCD(max)}$ with no effect on the worst-case access time (t_{RAC}). No errors will result if $\overline{CAS}$ is applied to the F4164 after the $t_{RCD(max)}$ limit, but access time will then be determined from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}).

Page Mode Operation
Higher speed and lower power operations can be performed in Page Mode on bits sharing a Row Address. In this mode $\overline{RAS}$ strobes in the common Row Address and is then kept LOW (active) while successive $\overline{CAS}$ cycles allow the required Column Addresses to be strobed in for subsequent Read or Write operations. Data from the first bit addressed is accessed within t_{RAC} (or $t_{RCD} + t_{CAC}$ if $t_{RCD} > t_{RCD(max)}$) and subsequent Column Addresses are accessed within t_{CAC} only.

Both the delays and the dynamic power dissipation associated with row selection and sensing occur only once with the initial $\overline{RAS}$ transition. Thereafter, delays and dynamic power dissipation are incurred only in the column select and data path. The delay and power in the row and sensing circuitry are amortized over 256 different Column Addresses offering improved speed and lower power per bit.

Page Mode address boundaries may be extended by multiplexing $\overline{CAS}$ to several devices which share a common Data output (Q) bus.

Data Input
In a Write operation, the data to be written is latched into the chip while $\overline{RAS}$ is LOW by a combination of $\overline{CAS}$ and Write Enable ($\overline{WE}$). The strobe is enabled by the last of these two signals to go LOW. This allows several types of write cycles to be performed. In an Early-Write cycle ($\overline{WE}$ LOW before $\overline{CAS}$ goes LOW), the Data input (D) is strobed by $\overline{CAS}$. Here data set-up and hold times are referenced to $\overline{CAS}$. If D is not yet valid at the time $\overline{CAS}$ becomes active, or if a Read-Write or Read-Modify-Write cycle is desired, then $\overline{WE}$ must be delayed. In this "late-write" mode, the data set-up and hold times are referenced to $\overline{WE}$ rather than $\overline{CAS}$.

Data Output
The Data output (Q) buffer assumes a high impedance state whenever $\overline{CAS}$ is HIGH (inactive) subject to $t_{OFF(max)}$. If the cycle being performed is a Read, Read-Modify-Write, or a "late-write" cycle, then the Q latch and buffer will remain high impedance until the access time, after which Q will assume the value of the data read from the selected cell. This output data is of the same polarity as the input data and will remain valid as long as $\overline{CAS}$ is kept LOW (active). However, if the operation is an Early-Write, or if the chip does not receive both $\overline{RAS}$ and $\overline{CAS}$, then Q will remain high impedance throughout the cycle. This feature allows systems which write exclusively in the Early-Write mode to connect D and Q directly together.

Since both $\overline{RAS}$ and $\overline{CAS}$ must be supplied for a device to be "active", a reduction in external decoding logic can be realized by using $\overline{RAS}$ and $\overline{CAS}$ in a 2-dimensional decoding/selection scheme. An analogous method can be used to extend the page boundary to beyond 256 locations by decoding which device receives a $\overline{CAS}$ in addition to the $\overline{RAS}$ already latched into the chips. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ will respond with a valid memory cycle (see Table 1).

Table 1 $\overline{RAS}$ and $\overline{CAS}$ Clock Conditions

$\overline{RAS}$ and $\overline{CAS}$ cycle	Device active
$\overline{RAS}$-only cycle	Device deselected, refresh
$\overline{CAS}$-only cycle	Device deselected
Neither $\overline{RAS}$ nor $\overline{CAS}$	Device deselected, standby

Refresh
Refresh of the data stored in the dynamic cell matrix of the F4164 is accomplished by performing a memory cycle at each of the 256 row addresses at least every 4 ms. Performing a $\overline{RAS}$-only Refresh with $\overline{CAS}$ held HIGH causes the output buffer to remain in the high-impendence state throughout the cycle.

The F4164 256-cycle, 4 ms refresh timing requirement is compatible with distributed refresh techniques currently utilized for 128-cycle, 2 ms refresh 16K dynamic RAMs.

Absolute Maximum Ratings

Voltage on Any Pin with Respect to V_{SS}	−1.0 V to +7.0 V
V_{DD} Supply with Respect to V_{SS}	−1.0 V to +7.0 V
Storage Temperature	−65°C to +150°C
Power Dissipation	1.0 W
Short-Circuit Output Current	50 mA
Operating Temperature	0°C to +70°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (Note)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	4.5		5.5	V
V_{SS}		0		0	V
V_{IH}	Input HIGH Voltage	2.4		6.5	V
V_{IL}	Input LOW Voltage, All Inputs	−1.0		0.8	V

DC Characteristics Recommended operating conditions unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 4.2 mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −5.0 mA
I_{DD1}	Operating Current Average Power Supply Current		27	38	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min; Q = no connection
I_{DD2}	Standby Current Power Supply Current			3.5	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}
I_{DD3}	Refresh Current Average Power Supply Current		21	32	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = Min, Q = no connection
I_{DD4}	Page Mode Current Average Power Supply Current		15	30	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{CP} = Min, Q = no connection
I_{IL}	Input Leakage Current	−10		10	μA	Any Input, 0 V ≤ V_{IN} ≤ 6.5 V; all other pins not under test = 0 V
I_{OL}	Output Leakage Current	−10		10	μA	Data Out is disabled, 0 V ≤ V_{OUT} ≤ 6.5 V

Capacitance T_A = +25°C

Symbol	Characteristic	Min	Typ	Max	Unit
C_{IN1}	Input Capacitance A_0-A_7, D			5.0	pF
C_{IN2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$			10	pF
C_{OUT}	Output Capacitance Q			7.0	pF

Note

All Voltages are referenced to V_{SS}. Conditions apply over the entire operating temperature range.

AC Characteristics Recommended operating conditions unless otherwise noted (Notes 1, 2, and 3)

IEEE Symbol[9]	Symbol	Characteristic	F4164-1		F4164-2		F4164-3		Unit	Note
			Min	Max	Min	Max	Min	Max		
TRVRV	t_{REF}	Time between Refresh		4.0		4.0		4.0	ms	
TRELREL	t_{RC}	Random Read/Write Cycle Time	300		320		330		ns	
TRELREL	t_{RWC}	Read-Write Cycle Time	315		335		375		ns	
TCELCEL	t_{PC}	Page Mode Cycle Time	160		170		225		ns	
TRELQV	t_{RAC}	Access Time from $\overline{RAS}$		120		150		200	ns	4, 6
TCEHQV	t_{CAC}	Access Time from $\overline{CAS}$		80		100		135	ns	5, 6
TCEHQZ	t_{OFF}	Output Buffer Turn-Off Delay	0	35	0	40	0	50	ns	
TT	t_T	Transition Time	3.0	35	3.0	35	3.0	50	ns	
TREHREL	t_{RP}	$\overline{RAS}$ Precharge Time	80		100		120		ns	
TRELREH	t_{RAS}	$\overline{RAS}$ Pulse Width	120	10K	150	10K	200	10K	ns	
TCELREH	t_{RSH}	$\overline{RAS}$ Hold Time	80		100		135		ns	
TCEHCEL	t_{CP}	$\overline{CAS}$ Precharge Time	60		60		80		ns	
TCELCEH	t_{CAS}	$\overline{CAS}$ Pulse Width	80	10K	100	10K	135	10K	ns	
TRELCEH	t_{CSH}	$\overline{CAS}$ Hold Time	120		150		200		ns	
TRELCEL	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	40	30	50	35	65	ns	7
TCEHREL	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		0		ns	
TARVREL	t_{ASR}	Row Address Set-up Time	0		0		0		ns	
TRELARX	t_{RAH}	Row Address Hold Time	15		20		25		ns	
TACVCEL	t_{ASC}	Column Address Set-up Time	0		0		0		ns	
TCELACX	t_{CAH}	Column Address Hold Time	40		45		55		ns	
TRELACX	t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	80		95		120		ns	
TWHCEL	t_{RCS}	Read Command Set-up Time	0		0		0		ns	
TCEHWL	t_{RCH}	Read Command Hold Time	0		0		0		ns	
TWLCEL	t_{WCS}	Write Command Set-up Time	0		−10		−10		ns	8
TCELWH	t_{WCH}	Write Command Hold Time	40		45		55		ns	
TRELWH	t_{WCR}	Write Command Hold Time Reference to $\overline{RAS}$	80		95		120		ns	
TWLWH	t_{WP}	Write Command Pulse Width	40		45		55		ns	
TWLREH	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	60		70		80		ns	
TWLCEH	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	60		70		80		ns	

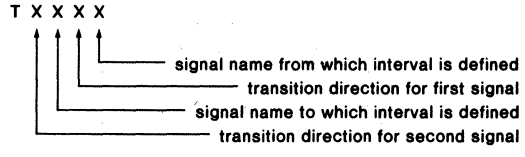
Notes on following page.

AC Characteristics (Continued)

IEEE Symbol[9]	Symbol	Characteristic	F4164-1		F4164-2		F4164-3		Unit	Note
			Min	Max	Min	Max	Min	Max		
TDVREL	t_{DS}	Data In Set-up Time	0		0		0		ns	
TCELDX	t_{DH}	Data In Hold Time	40		45		55		ns	
TRELDX	t_{DHR}	Data In Hold Time Referenced to $\overline{RAS}$	80		95		120		ns	
TCELWL	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	60		70		95		ns	8
TRELWL	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	100		120		160		ns	8

Notes

1. Several cycles are required after power up before proper device operation is achieved. Any eight cycles which perform refresh are adequate for this purpose.
2. Dynamic measurements assume $t_T = 5$ ns.
3. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leq t_{RCD(max)}$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. Refer to test conditions.
7. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating characteristics due to the following. If $t_{WCS} \geq t_{WCS(min)}$, the cycle is an early write cycle and the Data output pin will be open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$, the cycle is a read-write cycle and Data output will contain data read from the selected cell. If neither of the conditions is satisfied the condition of the Data output is indeterminate.
9. **Timing Parameter Abbreviations**
   All timing abbreviations in this format use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a 'from-to' sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:



The signal definitions used in this data sheet are:

RE = $\overline{RAS}$, CE = $\overline{CAS}$
AR = Row Address
AC = Column Address

A = Address
D = Data In
Q = Data Out
W = Write Enable

The transition definitions used in this data sheet are:

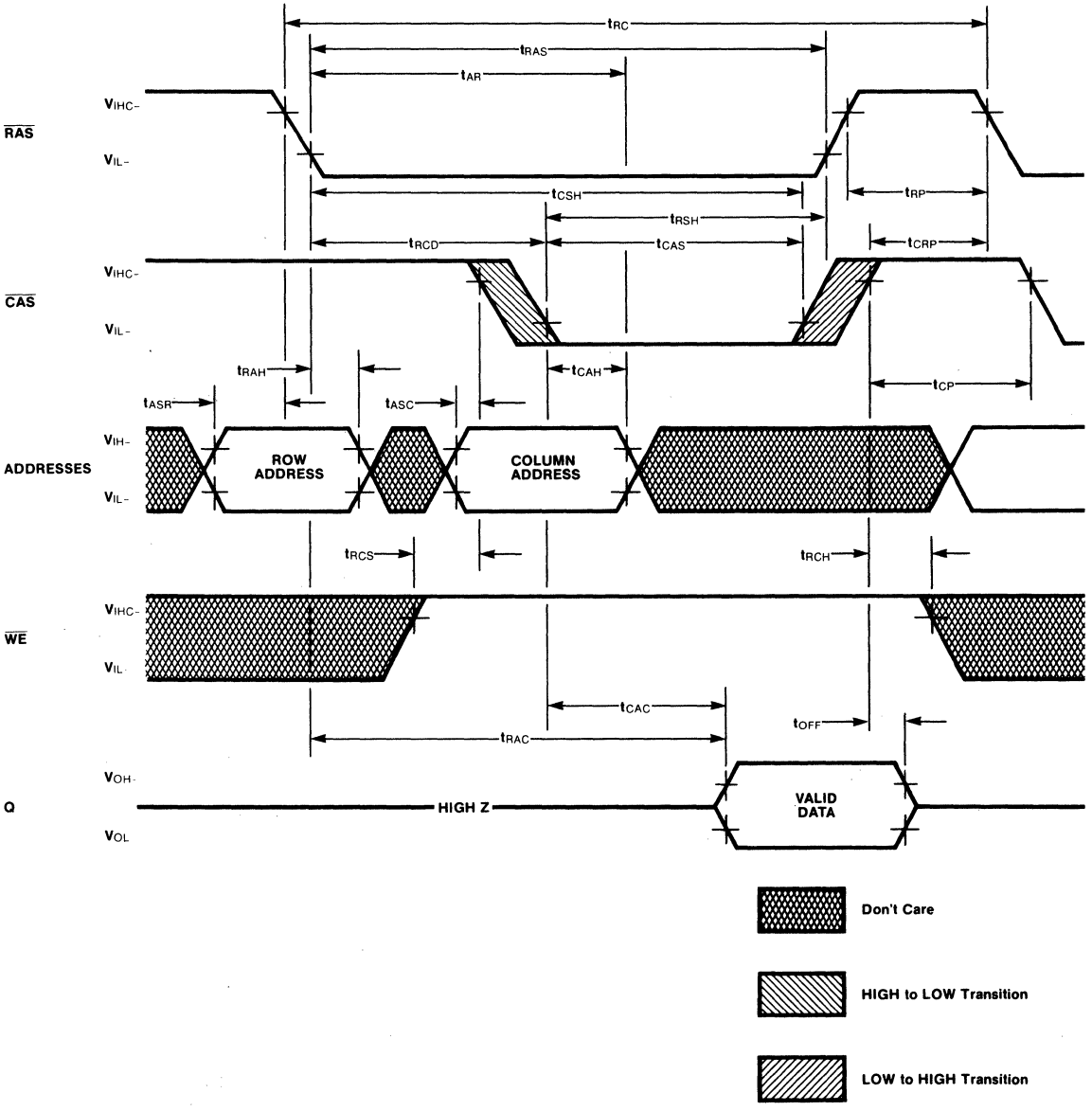
H = transition to HIGH
L = transition to LOW
V = transition to valid
X = transition to invalid or don't care
Z = transition to off (high impedance)

Timing Limits

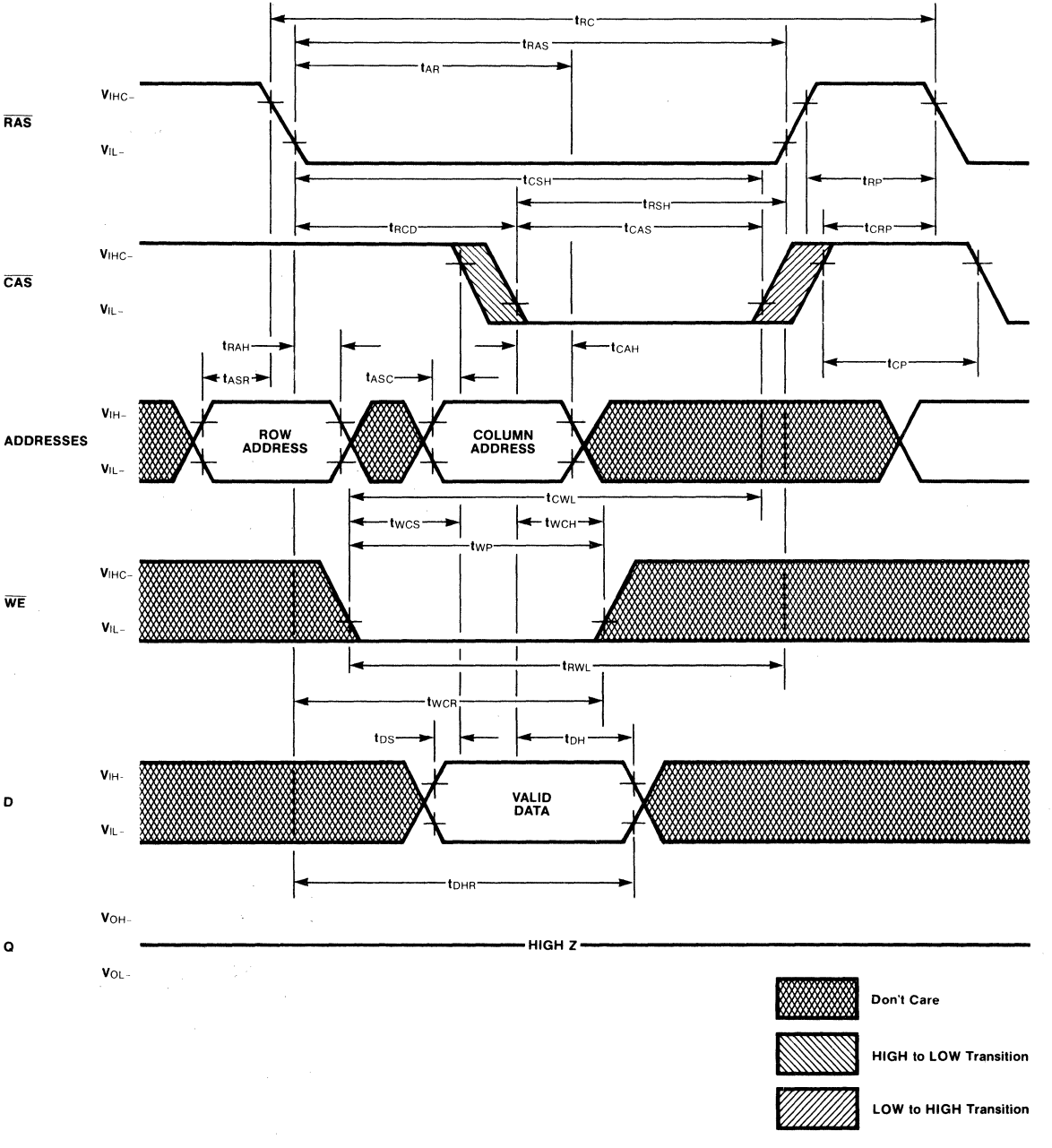
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Timing Diagrams

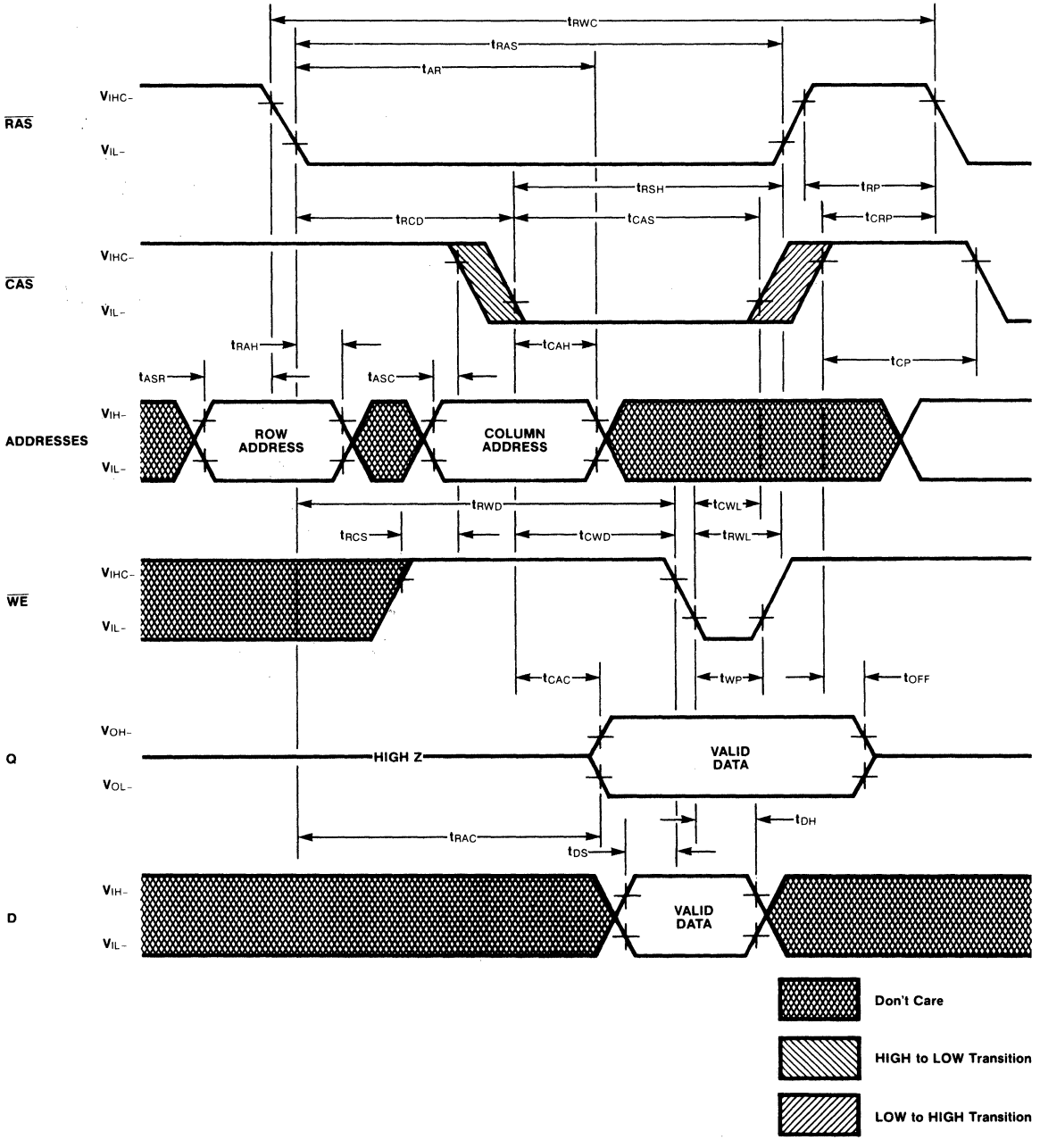
Read Cycle Timing Diagram



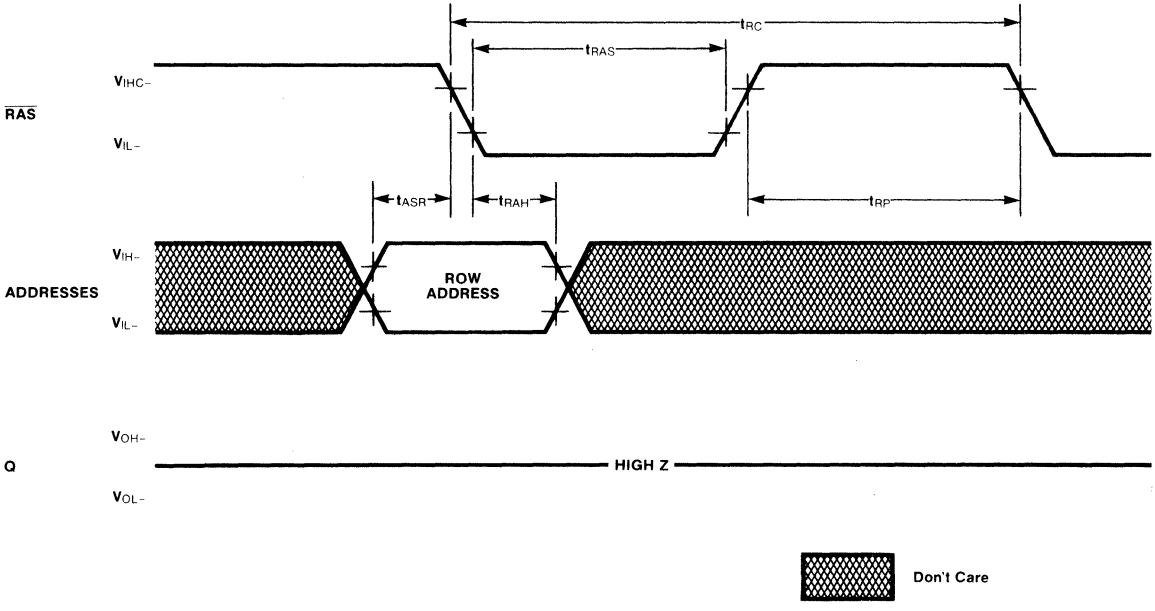
Write Cycle (Early Write)



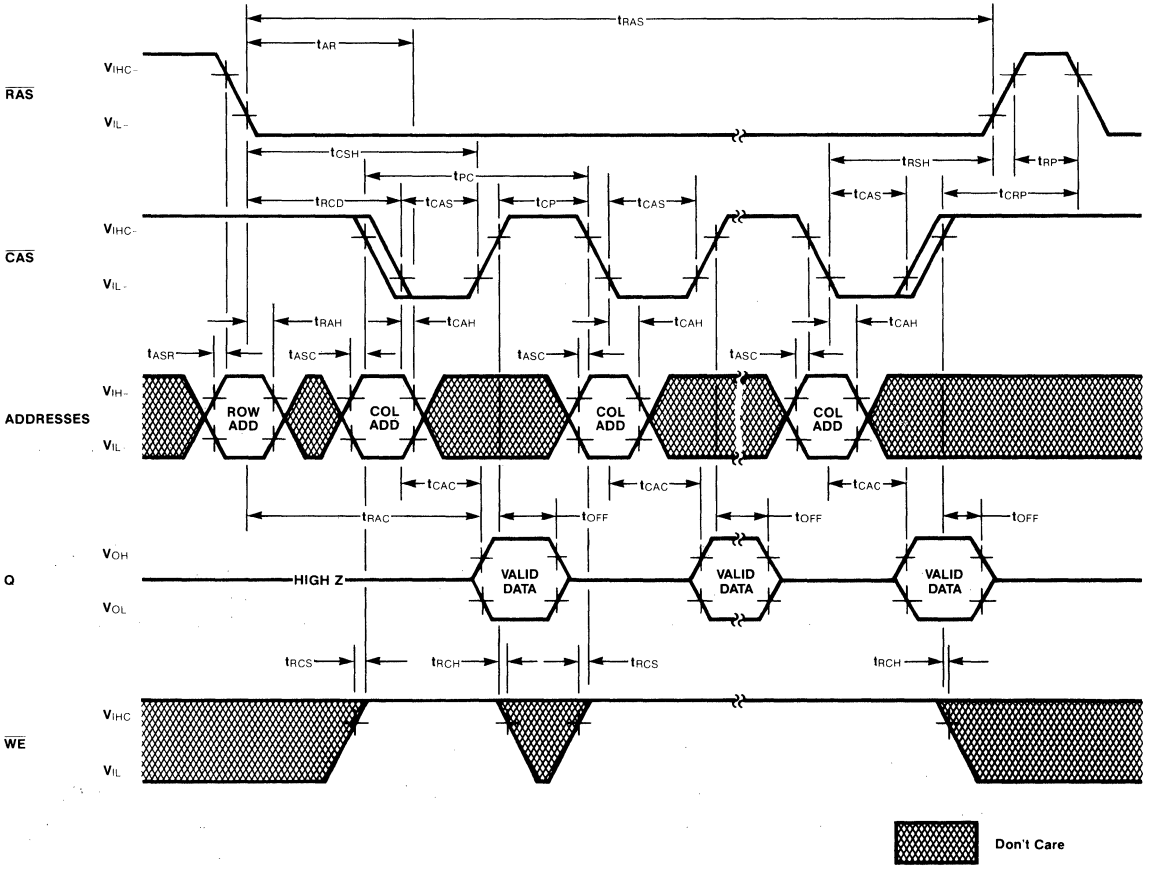
Read-Write/Read-Modify-Write Cycle



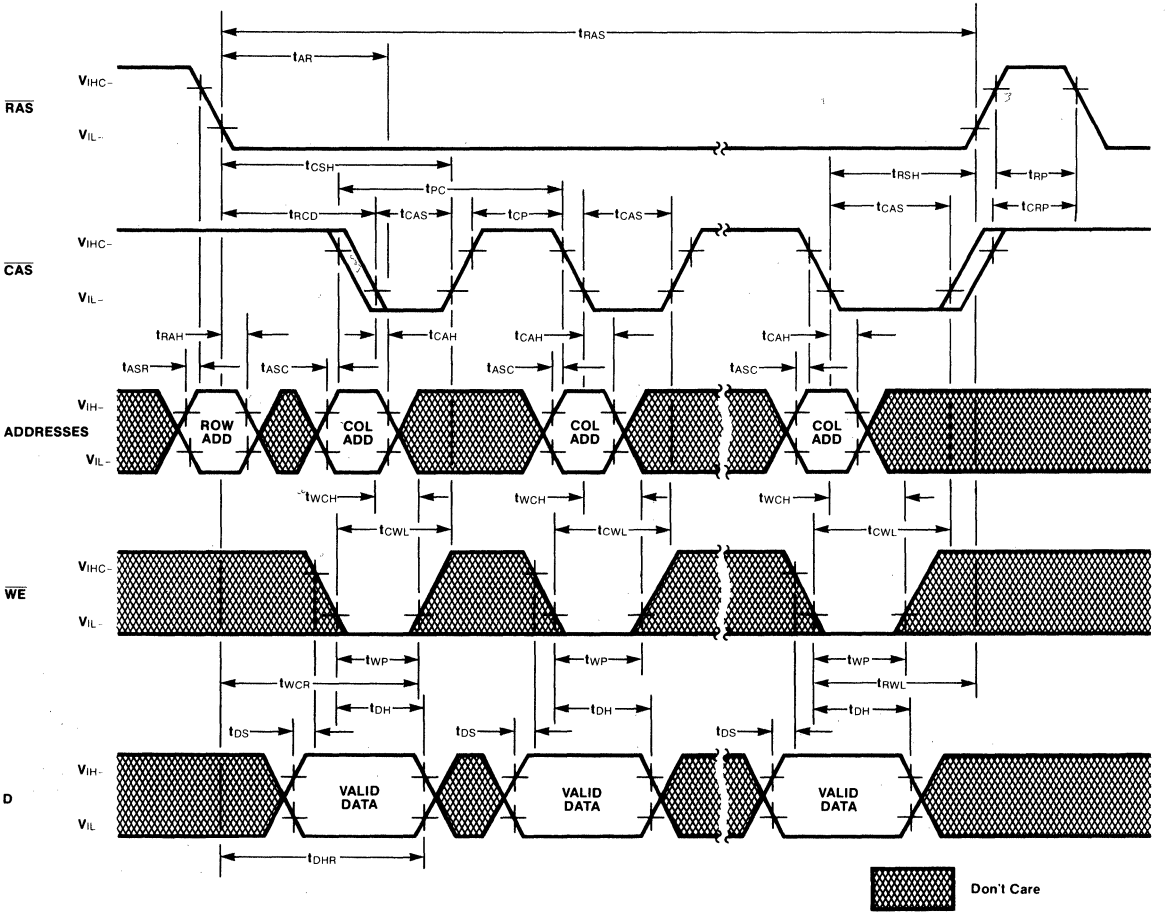
"$\overline{\text{RAS}}$-only" Refresh Cycle

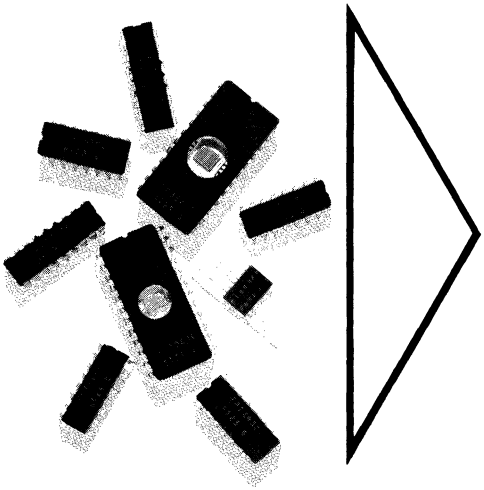


Page Mode Read Cycle



Page Mode Write Cycle





F2708
1024 x 8 UV Erasable PROM

MOS Memory Products

Description

The F2708 is an 8,192-bit ultraviolet light Erasable and electrically Programmable Read Only Memory (EPROM) manufactured using the Isoplanar n-channel silicon gate technology. Organized 1024 x 8, the F2708 is ideally suited for non-volatile data storage in applications such as 8-bit microprocessor systems, where reprogrammability, high bit-density, maximum performance and simple interfacing are essential parameters. All inputs and outputs are TTL compatible. The 3-state outputs become high impedance when the F2708 is deselected, allowing a direct interface capability which is useful in many computer bus structures.

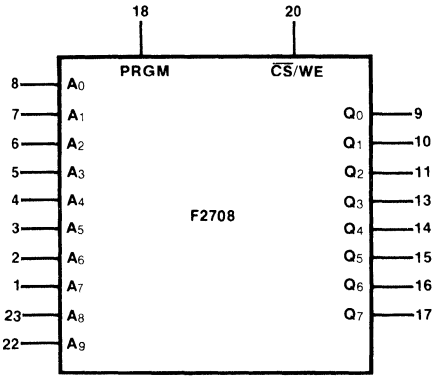
The F2708 provides inexpensive, non-volatile storage of data/program code in applications where fast turn-around and experimentation are important requirements.

- **1024 x 8-BITS ORGANIZATION**
- **FAST ACCESS TIME—350 ns MAX (F2708-1)**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **3-STATE OUTPUTS**
- **STANDARD POWER SUPPLIES +12 V, +5 V, −5 V**
- **CHIP SELECT INPUT FOR MEMORY EXPANSION**
- **STATIC OPERATION**
- **PIN COMPATIBLE TO 8K AND 16K ROMs FOR LOW-COST PRODUCTION**
- **LOW POWER DURING PROGRAMMING**
- **CONTENTS ERASABLE WITH ULTRAVIOLET LIGHT**

Pin Names

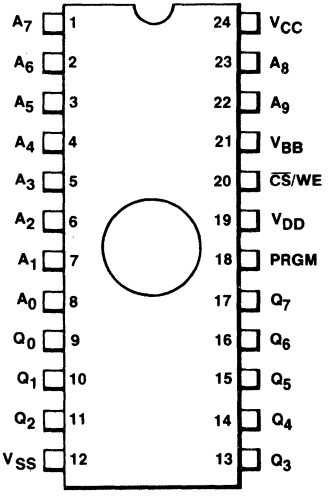
A_0-A_9	Address Inputs
PRGM	Program Pulse Input
$\overline{CS}$/WE	Chip Select/Write Enable
Q_0-Q_7	Data Outputs/Programming Inputs
V_{DD}	+12 V Supply
V_{CC}	+5 V Supply
V_{SS}	Ground
V_{BB}	−5 V Supply

Logic Symbol



V_{DD} = Pin 19
V_{CC} = Pin 24
V_{BB} = Pin 21
V_{SS} = Pin 12

Connection Diagram
24-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	7C	D

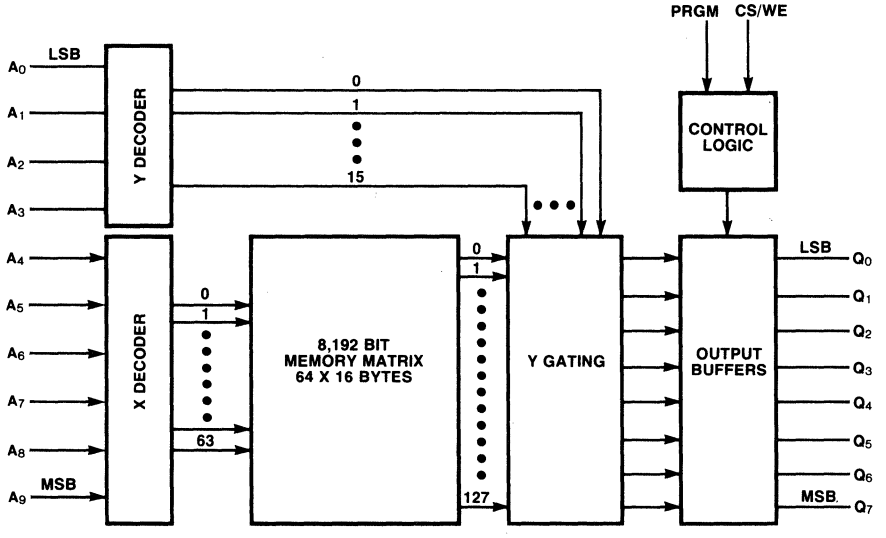
Absolute Maximum Ratings

V_{DD} Supply Voltage	−0.3 V to +20 V
V_{CC} or V_{SS} Supply Voltage	−0.3 V to +15 V
PRGM Input Voltage During Programming	−0.3 V to +35 V
$\overline{CS}$/WE Input Voltage During Programming	−0.3 V to +20 V
Any Other Input During Programming	−0.3 V to +15 V
Any Input or Output During Read	−0.3 V to +15 V
Operating Temperature (Ambient)	0°C to 70°C
Storage Temperature (Ambient)	−65°C to +125°C
Power Dissipation	1.8 W

All voltages with respect to V_{BB}.

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Connections During Read or Programming Modes

Mode	Data I/O	V_{SS} Supply	PRGM	V_{DD} Supply	$\overline{CS}$/WE	V_{BB} Supply	V_{CC} Supply
	9-11, 13-17	12	18	19	20	21	24
Read	Output Data	GND	GND	+12 V	V_{IL}	−5 V	+5 V
Program	Input Data	GND	Pulsed 26 V	+12 V	+12 V	−5 V	+5 V
Deselect	High Impedance	GND	GND	+12 V	V_{IH}	−5 V	+5 V

4

Read Mode dc Electrical Requirements
T_A = 0°C to 70°C unless otherwise indicated. All voltages referenced to V_{SS}

Symbol	Characteristic	Min	Typ	Max	Unit	Note
V_{DD}	Supply Voltage	11.4	12.0	12.6	V	
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	
V_{SS}	Supply Voltage	0	0	0	V	1
V_{BB}	Supply Voltage	−5.25	−5.0	−4.75	V	
V_{IH}	Input HIGH Voltage	3.0		V_{CC} +1.0	V	
V_{IL}	Input LOW Voltage	V_{SS}		0.65	V	

Read Mode dc Electrical Characteristics
Over full range of voltage and temperature unless otherwise indicated

Symbol	Characteristic (1)	Min	Typ	Max	Unit	Note
I_{DD}	Average V_{DD} Current		50	65	mA	2
I_{CC}	Average V_{CC} Current		7.5	10	mA	2
I_{BB}	Average V_{BB} Current		30	45	mA	2
I_{IN}	Input Leakage Current		1.0	10	μA	3
I_{OUT}	Output Leakage Current		1.0	10	μA	4
V_{OH}	Output HIGH Voltage I_{OH} = −1.0 mA	2.4			V	
	Output HIGH Voltage I_{OH} = −100 μA	3.7			V	
V_{OL}	Output LOW Voltage I_{OL} = 1.6 mA			0.45	V	
P_D	Power Dissipation T_A = 70°C			800	mW	5
C_{IN}	Input Capacitance		4.0	6.0	pF	6
C_{OUT}	Output Capacitance		8.0	12	pF	7

Notes on following page.

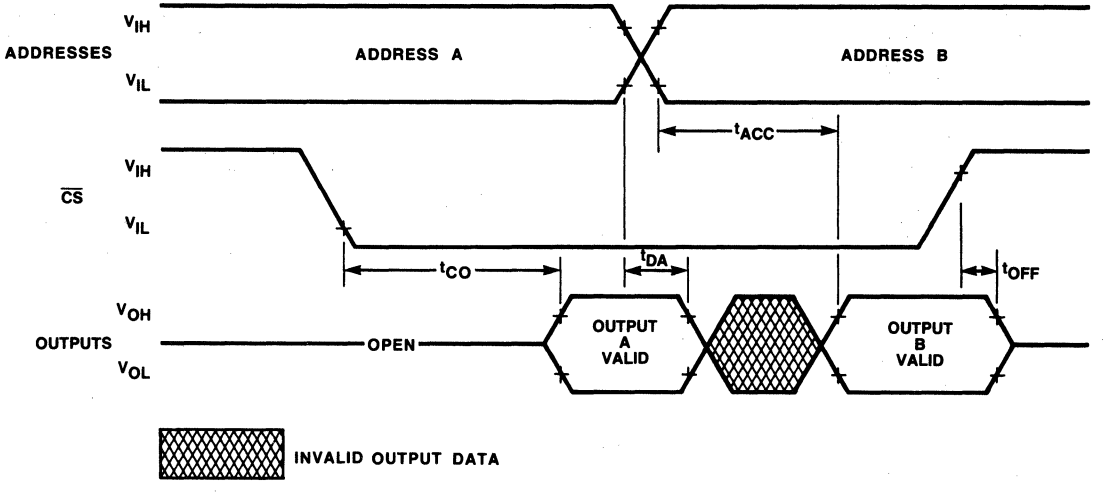
Read Mode ac Electrical Characteristics

Symbol	Characteristic (Note 8)	F2708-1		F2708		Unit	Note
		Min	Max	Min	Max		
t_{ACC}	Address to Output Delay Time		350		450	ns	
t_{CO}	Chip Select to Output Delay Time		120		120	ns	
t_{OFF}	Chip Deselect to Output High Impedance		120		120	ns	
t_{DA}	Data Valid After Address Time	0		0		ns	

Notes

1. All voltage levels are referenced to V_{SS} = 0 V.
2. Supply current limits are measured with all inputs HIGH (including $\overline{CS}$/WE = 5.0 V) and ambient temperature at T_A = 0°C.
3. Measured both with V_{IN} = 5.25 V and V_{IN} = $V_{IL(min)}$ = V_{SS}.
4. Measured both with V_{OUT} = 5.5 V and $\overline{CS}$/WE = 5.0 V.
5. The total power dissipation of the 2708 is specified at 800 mW. It is not calculable by summing the various currents (I_{DD}, I_{CC} and I_{BB}) multiplied by their respective voltages, since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC} and I_{BB} currents should be used to determine power supply capacity only.
6. Measured with V_{IN} = 0 V, T_A = 25°C and f = 1.0 MHz.
7. Measured with V_{OUT} = 0 V, T_A = 25°C and f = 1.0 MHz.
8. Timing parameters are measured with input logic levels of $V_{IL(max)}$ = 0.65 V and $V_{IH(min)}$ = 3.0 V. Timing measurement reference levels are 0.8 V and 2.8 V for inputs and 0.8 V and 2.4 V for outputs. An output load of 1 TTL gate plus 100 pF is assumed.

Read Mode Timing Diagram



Programming Instructions
After the completion of an erase operation, every memory cell in the F2708 is in the logic "1" state (as indicated by a HIGH level at the data outputs). An 8-bit byte of data is entered into the memory by programming logic "0s" into the appropriate cell locations at some given address. Word locations in the memory are addressed in the same way as in read operations. Once a cell is programmed to a logic "0", it can be altered only through ultraviolet light erasure.

In order to program the F2708, the $\overline{CS}$/WE input must first be set to 12 V. Data to be programmed is entered in 8-bit bytes through the output data terminals (Q_0 through Q_7). Input logic levels for the data lines, addresses, and supply voltages are the same as in a read operation.

Programming is accomplished by executing a number (n) of passes through a programming loop, each of which involves sequencing through all 1024 locations in the address space. In each pass through the loop, a single, high-voltage (26 V) pulse is applied to the PRGM input, once at each address. Logic "0s" applied to the Data outputs (Q_0 through Q_7) are written into the proper bit positions at the location specified by the Address inputs (A_0 through A_7). There must be n successive passes through the programming loop in order to guarantee reliable programming of information. The required number of passes through the programming loop (n) is a function of the pulse width (t_{PW}) of the high-voltage programming pulse applied to the PRGM input. Total programming time is given by the relationship:

$$t_{TOTAL} = n \times t_{PW} \geq 100 \text{ ms} \qquad (1)$$

The allowed range of pulse widths is from 0.1 ms to 1.0 ms. This implies that the minimum value of n must be in the range of 100 to 1000. WARNING: Applying more than one programming pulse in succession to the same address is not permitted since it will result in damage to the device. At the end of a program sequence, the $\overline{CS}$/WE falling edge transition must occur before the first address transition when changing from the program mode to the read mode. The PRGM pin should be pulled down to approximately V_{SS}, (i.e., ground) with a low impedance device since this pin sources several milliamps of current when $\overline{CS}$/WE is at 12 V and the PRGM pin is LOW.

Programming Examples
The programming relationship in Equation 1 above should always be used in determining values of t_{PW} and n.

Example 1
The full capacity of 1024 bytes could be programmed using 0.2 ms programming pulse widths. In this case, the minimum number of passes through the programming loop would be

$$n = \frac{t_{TOTAL}}{t_{PW}} = \frac{100 \text{ ms}}{0.2 \text{ ms}} = 500 \text{ passes} \qquad (2)$$

Each of the 500 passes through the programming loop must sequence through address locations 0 through 1023.

Example 2
Word locations 0 to 200 and 300 to 700 are to be programmed. All other bits are "don't care". The programmed pulses are 0.5 ms wide. Thus, the minimum number of passes through the program loop is

$$n = \frac{100 \text{ ms}}{0.5 \text{ ms}} = 200 \text{ passes} \qquad (3)$$

The data entered into the "don't care" locations should consist of all logic "1s". Even though portions of the address space are not used (or "don't care"), the programming loop should still sequence through all 1024 addresses on each pass.

Example 3
Extending the case of Example 2, the F2708 is now to be updated to include new data at locations 850 to 880 which previously were programmed as "don't care"; in this case, logic "1s". The mimimum number of passes through the programming loop is the same as in Example 2, n = 200 passes. Address locations 0 to 200 and 300 to 700 must be reprogrammed with their original data pattern. The remaining unused addresses should again be programmed as logic "1s".

Erasing Instructions

The contents of the F2708 EPROM can be erased by exposure to high-intensity short-wave ultraviolet (UV) light with a wavelength of 2537 Angstroms (Å). This can be accomplished with ultraviolet light EPROM erasure devices which are available from several U.S. manufacturers. These erasure devices contain a UV light source which is usually placed approximately one or two inches from the EPROM to illuminate the transparent window on top of the device. The minimum required integrated dose (intensity x exposure time) of UV light energy incident on the window of the device in order to reliably insure complete erasure is 12.5 W-s/cm^2. The UV erasure unit should be periodically calibrated if minimum exposure times are to be used. (Minimum exposure times range from 10 to 45 minutes, depending on model type and age of UV lamp). If longer exposure times are possible, variations in the output light intensity of the UV light source are not critical.

Program Mode dc Electrical Requirements $T_A = 25°C \pm 5°C$ unless otherwise indicated

Symbol	Characteristic		Min	Typ	Max	Unit	Note
V_{DD}	Supply Voltage		11.4	12.0	12.6	V	
V_{CC}	Supply Voltage		4.75	5.0	5.25	V	
V_{SS}	Supply Voltage		0	0	0	V	1
V_{BB}	Supply Voltage		−5.25	−5.0	−4.75	V	
V_{IHP}	Input HIGH Voltage During Programming	Address and Data	3.0		V_{CC} + 1.0	V	
		$\overline{CS}$/WE Input	11.4	12.0	12.6	V	
		PRGM Input	25		27	V	2
V_{IL}	Input LOW Voltage	PRGM Input	V_{SS}		1.0	V	2
		All Other Inputs	V_{SS}		0.65	V	

Program Mode dc Electrical Characteristics $T_A = 25°C \pm 5°C$ unless otherwise indicated

Symbol	Characteristic		Min	Typ	Max	Unit	Note
I_{DD}	Average V_{DD} Current			50	65	mA	3
I_{CC}	Average V_{CC} Current			6.0	10	mA	3
I_{BB}	Average V_{BB} Current			30	45	mA	3
I_{IN}	Input Leakage Current, Addresses and $\overline{CS}$/WE		−10		10	μA	4
I_{PRGM}	PRGM Input Current	HIGH			20	mA	
		LOW			3.0	mA	5

Notes

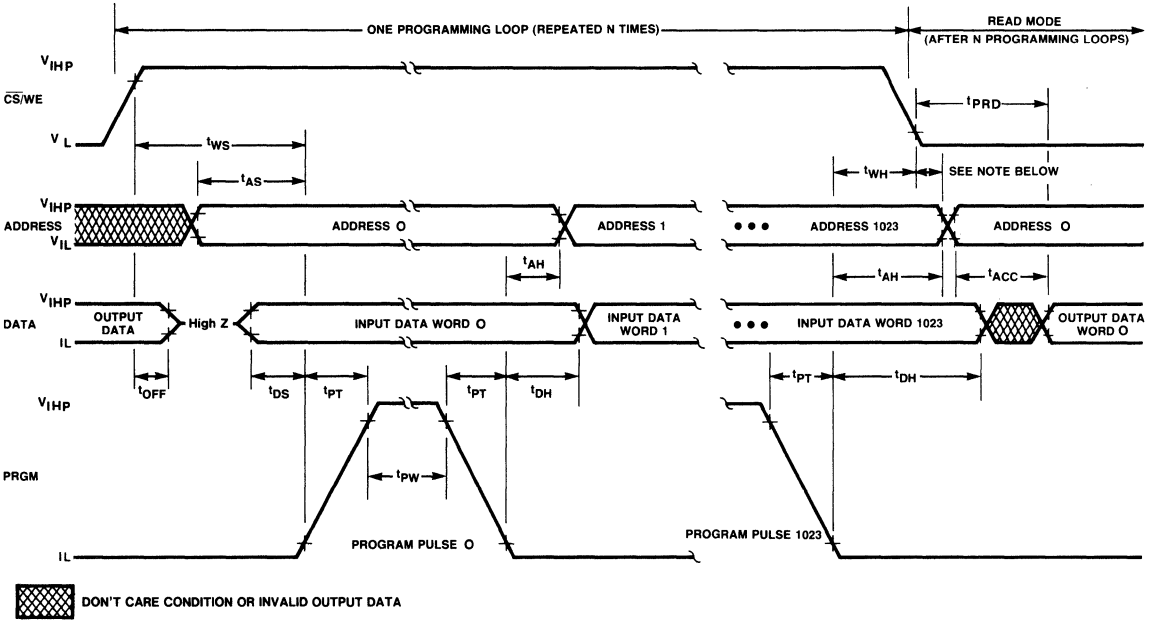
1. All voltage levels are referenced to V_{SS} = 0 V.
2. The voltage differential between V_{IHP} and V_{IL} at the PRGM input pin should be greater than or equal to 25 V.
3. Supply current limits are measured with all inputs HIGH (including $\overline{CS}$/WE = 5.0 V) and ambient temperature at $T_A = 0°C$.
4. Measured both with V_{IN} = 5.25 V and $V_{IN} = V_{IL(min)} = V_{SS}$.
5. This is a current sourced by the PRGM pin when it is in the LOW state and when $\overline{CS}$/WE = 12 V.

Program Mode ac Electrical Requirements and Characteristics $T_A = 25°C \pm 5°C$ unless otherwise indicated

Symbol	Characteristic		Min	Max	Unit	Note
t_{AS}	Address Set-up Time		10		μs	
t_{AH}	Address Hold Time		1.0		μs	
t_{WS}	Write Enable Set-up Time		10		μs	
t_{WH}	Write Enable Hold Time		0.5		μs	
t_{DS}	Data Set-up Time		10		μs	
t_{DH}	Data Hold Time		1.0		μs	
t_{PW}	Program Pulse Width		0.1	1.0	ms	
t_{PT}	Program Pulse Transition Time	Rise	0.5	2.0	μs	
		Fall	0.5	2.0	μs	
t_{PRD}	Program to Read Delay			10	μs	
t_{OFF}	Output Buffer Turn-off Delay		0	120	ns	

4

Program Mode Timing Diagram



Note

The falling edge of $\overline{CS}$/WE must occur after the falling edge of the program pulse and before the address transition.

F2732
32K (4K x 8)
UV Erasable PROM

MOS Memory Products

Description

The F2732 is a 32,768-bit ultraviolet light Erasable and electrically Programmable Read Only Memory (EPROM) manufactured using the Isoplanar n-channel silicon gate technology. Organized 4096 × 8, the F2732 is ideally suited for non-volatile data storage in applications such as 8-bit microprocessor systems, where reprogrammability, high bit-density, maximum performance, and simple interfacing are essential parameters. All inputs and outputs are TTL-compatible. The 3-state outputs become high impedance when the F2732 is deselected, allowing a direct interface capability which is useful in many computer bus structures.

The F2732 operates from a single standard +5 V power supply during reading, making it compatible with the latest generations of microprocessors.

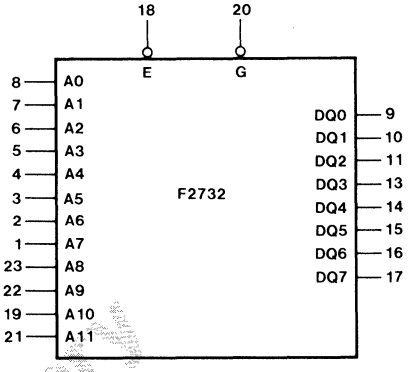
The F2732 programming technique is the simplest available. All data and address inputs are at TTL levels during programming. A +25 V power supply is connected to the $\overline{G}$/VPP pin and only those addresses to be programmed need be selected; therefore total programming time is short and field corrections straight forward. The technique is compatible with board-level programming making large systems simple to program.

- **4096 x 8-BIT ORGANIZATION**
- **FAST ACCESS TIME—450 ns MAX**
- **TTL-COMPATIBLE INPUTS AND OUTPUTS**
- **3-STATE OUTPUTS FOR WIRED-OR CAPABILITY**
- **SINGLE +5 V POWER SUPPLY FOR READ OPERATION**
- **REDUCED POWER STANDBY MODE**
- **SIMPLEST, FASTEST EPROM PROGRAMMING TECHNIQUE AVAILABLE**
- **OUTPUT ENABLE CONTROL FOR MEMORY EXPANSION**
- **STATIC OPERATION**
- **PIN COMPATIBLE WITH 32K AND 64K ROMs FOR LOW COST PRODUCTION**
- **LOW POWER DURING PROGRAMMING**
- **CONTENTS ERASABLE WITH ULTRAVIOLET LIGHT**

Pin Names

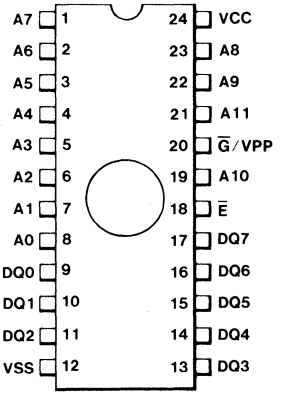
A0-A11	Address Inputs
$\overline{E}$	Chip Enable (Power Down) Input
$\overline{G}$/VPP	Output Enable/+25 V Program Input
DQ0-DQ7	Data Output/Programming Inputs
VCC	+5 V Supply
VSS	Ground

Logic Symbol



VCC = Pin 24
VPP = Pin 20
VSS = Pin 12

Connection Diagram 24-Pin DIP



(Top View)

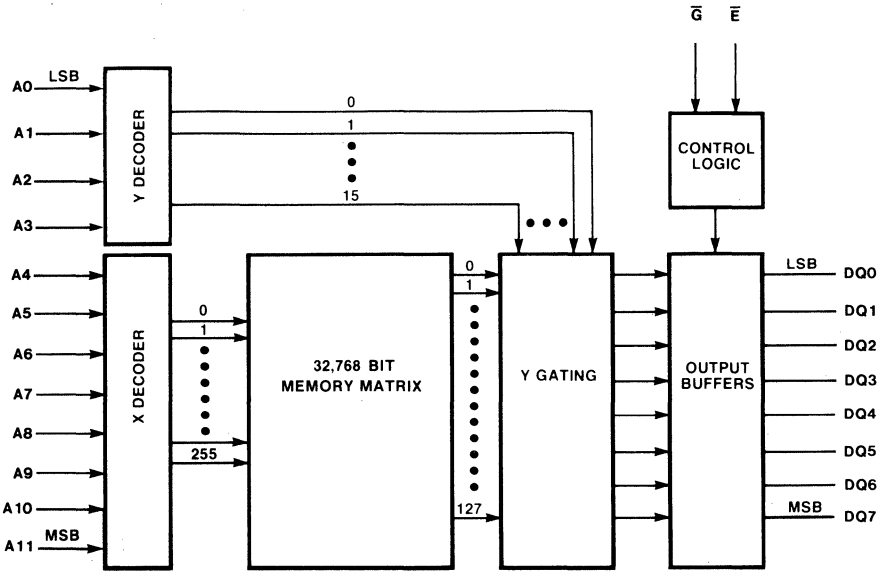
Package	Outline	Order Code
Ceramic DIP	7W	D

Absolute Maximum Ratings

VCC Supply Voltage	−0.3 V to +6 V
Any Input or Output	−0.3 V to +6 V
Operating Temperature (Ambient)	0°C to 70°C
Storage Temperature (Ambient)	−65°C to + 125°C

All voltages with respect to VSS.
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

Block Diagram



Mode Selection All voltages referenced to ground

Mode	Outputs	Address Inputs	$\overline{E}$	$\overline{G}$/VPP	VCC	Note
Read	V_{OL} or V_{OH}	V_{IL} or V_{IH}	V_{IL}	V_{IL}	+5 V	1
Deselect/ Active	High Z	V_{IL} or V_{IH}	V_{IL}	V_{IH}	+5 V	1
Deselect/ Power Down	High Z	V_{IL} or V_{IH}	V_{IH}	V_{IH} or V_{IL}	+5 V	1
Program	V_{IH} or V_{IL}	V_{IL} or V_{IH}	Pulse V_{IH} to V_{IL}	V_{PP}	+5 V	1,2
Verify During Program	V_{OL} or V_{OH}	V_{IL} or V_{IH}	V_{IL}	V_{IL}	+5 V	1
Inhibit Program	High Z	V_{IL} or V_{IH}	V_{IH}	V_{PP}	+5 V	1

Read Mode dc Electrical Requirements
T_A = 0°C to 70°C unless otherwise indicated; all voltages referenced to ground

Symbol	Characteristic	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
V_{IH}	Input HIGH Voltage	2.0		V_{CC} + 1.0	V
V_{IL}	Input LOW Voltage	−0.1		0.8	V

Read Mode dc Electrical Characteristics Over full range of operating voltage and temperature unless otherwise indicated; typical values are for T_A = 25°C and nominal supply voltages

Symbol	Characteristic (Note 3)	Min	Typ	Max	Unit	Note
I_{CC}	Average V_{CC} Current Active		85	150	mA	4
	Average V_{CC} Current Power Down		15	30	mA	4
I_{IN1}	Input Leakage Current (Except $\overline{G}$/VPP)			10	μA	5
I_{IN2}	$\overline{G}$/VPP Input Leakage Current			10	μA	5
I_{OUT}	Output Leakage Current			10	μA	6
V_{OH}	Output HIGH Voltage I_{OH} = −400 μA	2.4			V	
V_{OL}	Output LOW Voltage I_{OL} = 2.1 mA			0.45	V	
C_{IN1}	Input Capacitance (Except $\overline{G}$/VPP)		4.0	6.0	pF	7
C_{IN2}	$\overline{G}$/VPP Input Capacitance			20	pF	7
C_{OUT}	Output Capacitance		8.0	12	pF	8

Notes on following page.

Read Mode ac Electrical Characteristics

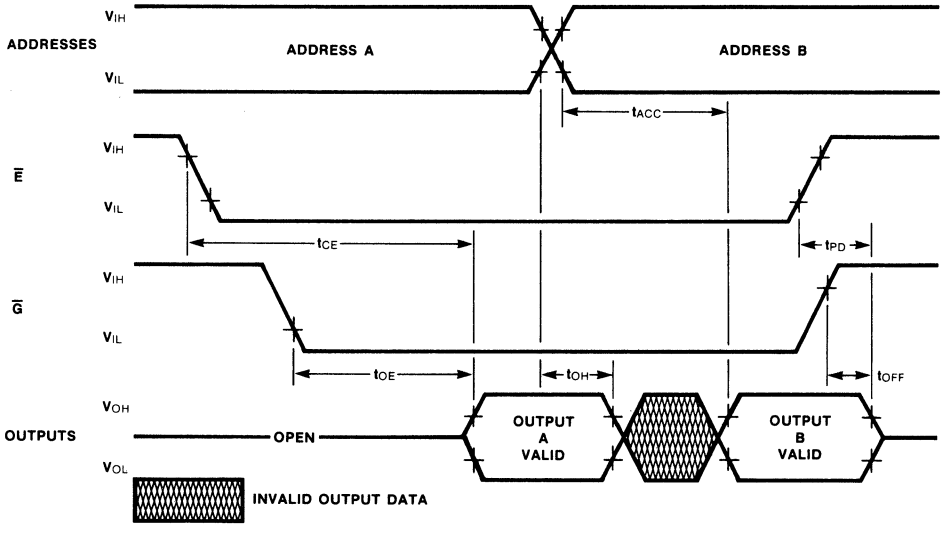
Over full range of operating voltage and temperature unless otherwise indicated

Symbol	Characteristic	Min	Max	Unit	Note
t_{ACC}	Address to Output Delay Time		450	ns	9
t_{OE}	Output Enable to Output Delay Time		120	ns	9
t_{OFF}	Output Disable to Output High Impedance		100	ns	
t_{OH}	Address to Output Hold Time	0		ns	
t_{CE}	Power-up Delay from $\overline{E}$ to Outputs Active		450	ns	
t_{PD}	Power-down Delay from $\overline{E}$ to Outputs OFF		100	ns	

Notes

1. V_{IL} or V_{IH} should be selected on Address and Data inputs as desired.
2. Outputs are in the HIGH state allowing Data In to be applied with TTL drivers.
3. All voltage levels are referenced to VSS.
4. Worst case supply currents occur when all inputs are HIGH (including $\overline{G}$ = 5.0 V) and the ambient temperature is T_A = 0°C.
5. Measured both with V_{IN} = 5.25 V and V_{IN} = 0 V.
6. Measured both with V_{OUT} = 5.25 V and $\overline{G}$ = 5.0 V.
7. Measured with V_{IN} = 0 V, T_A = 25°C and f = 1.0 MHz.
8. Measured with V_{OUT} = 0 V, T_A = 25°C and f = 1.0 MHz.
9. Timing parameters are measured with input logic levels of $V_{IL(max)}$ = 0.8 V and $V_{IH(min)}$ = 2.2 V. Timing measurement reference levels are 1.0 V and 2.0 V for inputs and 0.8 V and 2 V for outputs. An output load of 1 TTL gate plus 100 pF is assumed.

Read Mode Timing Diagram



Erasing Instructions
The contents of the F2732 EPROM can be erased by exposure to high intensity short-wave ultraviolet (UV) light with a wavelength of 2537 Angstroms (Å). This can be accomplished with ultraviolet light EPROM erasure devices which are available from several U.S. manufacturers. These erasure devices contain a UV light source which is usually placed approximately one or two inches from the EPROM to illuminate the transparent window on top of the device. The minimum required integrated dose (intensity x exposure time) of UV light energy incident on the window of the device in order to reliably insure complete erasure is 15 W-s/cm^2. The UV erasure unit should be periodically calibrated if minimum exposure times are to be used. (Minimum exposure times range from 10 to 45 minutes, depending on model type and age of UV lamp.) If longer exposure times are possible, variations in the output light intensity of the UV light source are not critical.

Programming
After erasure with a UV source all bits of the memory will be sensed as V_{OH} levels. Any word of the memory may have V_{OL} levels programmed into it. All eight outputs are programmed at one time for any selected address. Words may be programmed in any order. Programming time for any word regardless of the number of bits to be programmed is 50 ms; maximum programming time for all addresses is 205 s. Once programmed to a V_{OL} level a bit of the array can be changed back to a V_{OH} level by exposing the entire array to a UV source.

The programming procedure is as follows:
1. Apply V_{CC} and V_{SS} with $\overline{E}$ at V_{IH}.
2. Apply V_{PP} to the $\overline{G}$/VPP Input.
3. Apply V_{IL} and V_{IH} to the Address inputs and outputs to select the data combination to be programmed.
4. Apply a 50 ms wide V_{IL} pulse to $\overline{E}$.
5. Apply V_{IL} to $\overline{G}$/VPP and remove the drivers from the output. Read out the contents of the memory (this verification step is optional).
6. Repeat steps 3 through 5 until all desired data has been programmed.
7. Reduce the $\overline{G}$/VPP voltage to V_{IL} to change to the normal read mode.

Caution
It is recommended that a 0.1 μF capacitor be connected between $\overline{G}$/VPP and ground to prevent voltage transients that may damage the device.

Program Mode dc Electrical Requirements and Characteristics $T_A = 25°C \pm 5°C$

Symbol	Characteristic	Min	Typ	Max	Unit	Note
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	
V_{PP}	Programming Input Voltage	24	25	26	V	1
V_{IL}	Input LOW Voltage	−0.1		0.8	V	
V_{IH}	Input HIGH Voltage (Except $\overline{G}$/VPP)	2.0		V_{CC} + 1	V	
I_{IN}	Input Leakage Current (for any input)			10	μA	2
I_{PP}	V_{PP} Supply Current			30	mA	3
I_{CC}	V_{CC} Supply Current		85	150	mA	

Notes on following page.

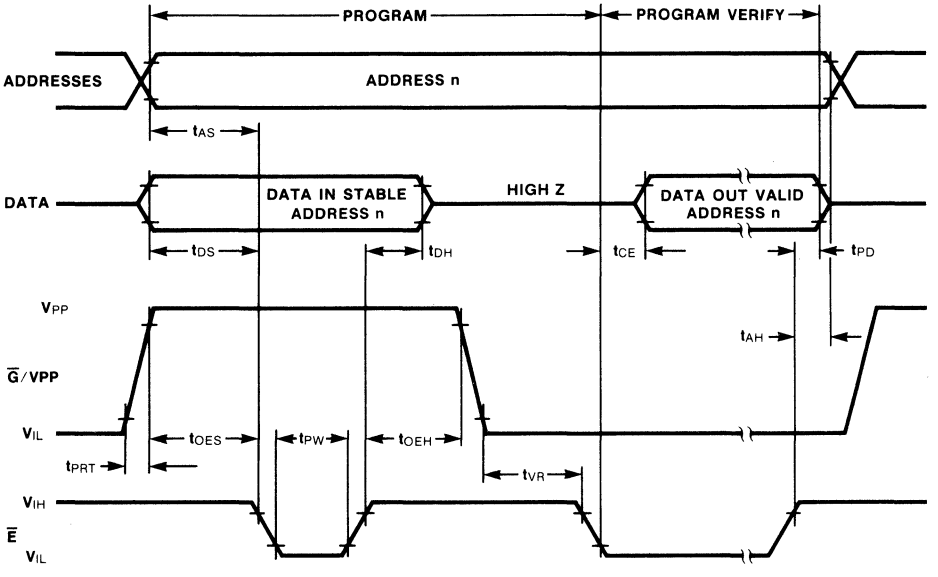
Program Mode ac Electrical Characteristics and Requirements $T_A = 25°C \pm 5°C$ (Note 1)

Symbol	Characteristic	Min	Typ	Max	Unit	Note
t_{AS}	Address Set-up Time	2			μs	
t_{OES}	$\overline{G}$ Set-up Time	2			μs	
t_{DS}	Data Set-up Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{OEH}	$\overline{G}$ Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{PD}	Power-down Delay from $\overline{E}$ to Outputs OFF	0		120	ns	3
t_{CE}	Chip Enable to Data Valid			1	μs	4
t_{PW}	Program Pulse Width	45	50	55	ms	
t_{PR}	$\overline{G}$ Pulse Rise Time During Programming	50			ns	
t_{VR}	V_{PP} Recovery Time	2			μs	

Notes

1. A 0.1 μF capacitor must be connected between $\overline{G}/V_{PP}$ and ground to prevent voltage transients which may damage the device.
2. V_{IN} = 5.25 V to 0 V.
3. $\overline{E} = V_{IL}$.
4. $\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$.

Program Mode Timing Diagram



F2764
64K (8K x 8)
UV Erasable PROM

MOS Memory Products

Description

The F2764 is a 65,536-bit ultraviolet light Erasable and electrically Programmable Read Only Memory (EPROM) manufactured using the Fairchild advanced NMOS, Isoplanar-H™ technology. Organized 8192 x 8, the F2764 is ideally suited for non-volatile data storage in applications such as 8-bit microprocessor systems, where reprogrammability, high bit-density, maximum performance, and simple interfacing are essential parameters. The 3-state outputs become high impedance when the F2764 is deselected, allowing a direct interface capability which is useful in many computer bus structures.

The F2764 operates from a single standard +5 V power supply during reading, making it compatible with the latest generations of microprocessors.

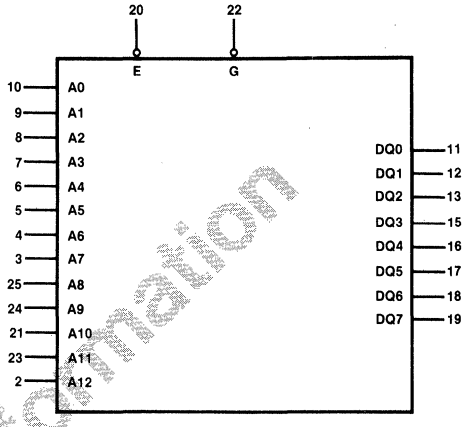
The F2764 programming technique is the simplest available. All data and address inputs are at TTL levels during programming. A +21 V power supply is connected to the VPP pin and only those addresses to be programmed need be selected; therefore total programming time is short and field corrections straight forward. The technique is compatible with board-level programming making large systems simple to program.

- **8192 x 8-BIT ORGANIZATION**
- **FAST ACCESS TIME—200 ns MAX**
- **TTL-COMPATIBLE INPUTS AND OUTPUTS**
- **3-STATE OUTPUTS FOR WIRED-OR CAPABILITY**
- **SINGLE +5 V POWER SUPPLY FOR READ OPERATION**
- **REDUCED POWER STANDBY MODE**
- **SIMPLEST, FASTEST EPROM PROGRAMMING TECHNIQUE AVAILABLE**
- **OUTPUT ENABLE CONTROL FOR MEMORY EXPANSION**
- **STATIC OPERATION**
- **UNIVERSAL BYTE WIDE PINOUT**
- **LOW POWER DURING PROGRAMMING**
- **CONTENTS ERASABLE WITH ULTRAVIOLET LIGHT**

Pin Names

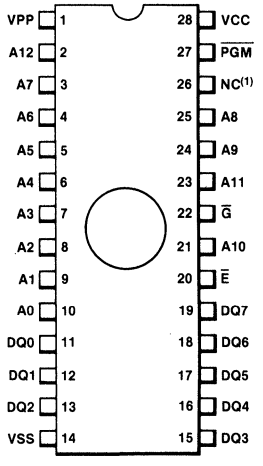
A0-A12	Address Inputs
$\overline{E}$	Chip Enable (Power Down) Input
$\overline{G}$	Output Enable Input
VPP	+21 V Program Input
DQ0-DQ7	Data Output/Programming Inputs
$\overline{PGM}$	Program
VCC	+5 V Supply
VSS	Ground

Logic Symbol



VCC = Pin 28
VSS = Pin 14
VPP = Pin 1
$\overline{PGM}$ = Pin 27

Connection Diagram
28-Pin DIP



(Top View)

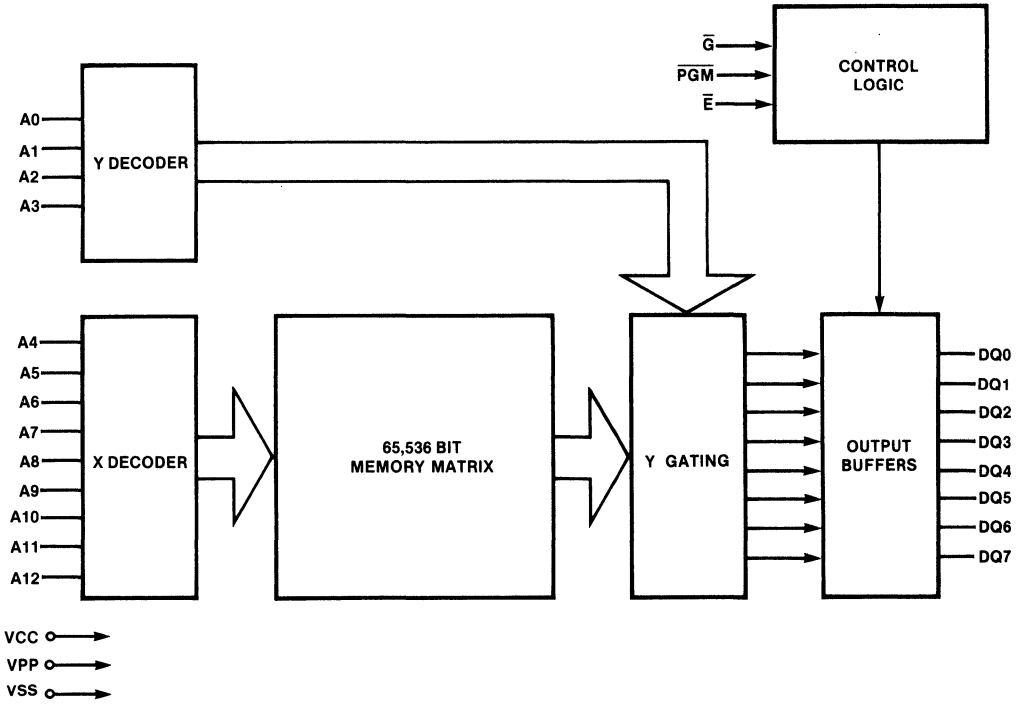
(1) For total compatibility and upgradability from the F2732 and ROMs provide a trace to Pin 26

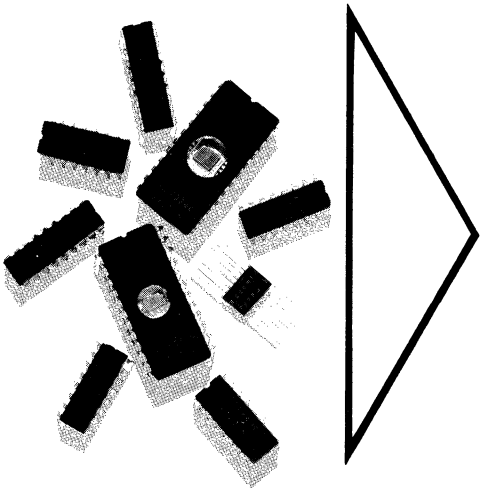
Absolute Maximum Ratings

VCC Supply Voltage	−1.0 V to +7.0 V
Any Input or Output	−1.0 V to +7.0 V
VPP Supply During Programming	−1.0 V to +22 V
Operating Temperature (Ambient)	0°C to 70°C
Storage Temperature (Ambient)	−65°C to +150°C

All voltages with respect to VSS.
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

Block Diagram





3341/3341A 64 x 4 FIFO Serial Memory

MOS Memory Products

Description

The 3341 or 3341A is a 64-word x 4-bit First-In First-Out (FIFO) Serial Memory. Inputs and the outputs are completely independent (no common clocks) making the 3341/3341A ideal for asynchronous buffer applications.

Special on-chip input pull-up circuits and bipolar-compatible output buffers provide direct bipolar interfacing with no external components required. Control signals are provided for both vertical and horizontal cascading.

The 3341 and 3341A are manufactured using the p-channel Isoplanar silicon gate process and are available in both ceramic and plastic packages.

- **1 MHz (3341A) AND 700 kHz (3341) DATA RATES**
- **INDEPENDENT ASYNCHRONOUS INPUTS AND OUTPUTS**
- **FULLY TTL COMPATIBLE**
- **EXPANDABLE IN EITHER DIRECTION**
- **ACTIVE PULL-UP ON INPUTS**
- **16-PIN DUAL IN-LINE PACKAGE**

Pin Names

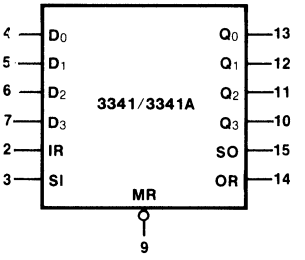
IR	Input Ready
SI	Shift In
D_0-D_3	Data Inputs
$\overline{MR}$	Master Reset
OR	Output Ready
SO	Shift Out
Q_0-Q_3	Data Outputs
V_{SS}	+5 V Power Supply
V_{DD}	0 V Power Supply
V_{GG}	−12 V Power Supply

Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Voltage on All Pins Except V_{DD} with Respect to V_{SS}	−20 V to +0.3 V
Voltage on V_{DD}	−7.0 V to +0.3 V

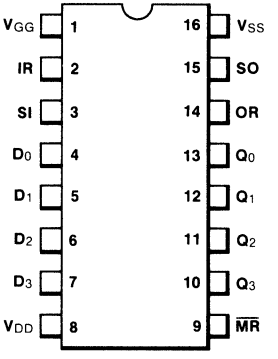
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Symbol



V_{SS} = Pin 16
V_{DD} = Pin 8
V_{GG} = Pin 1

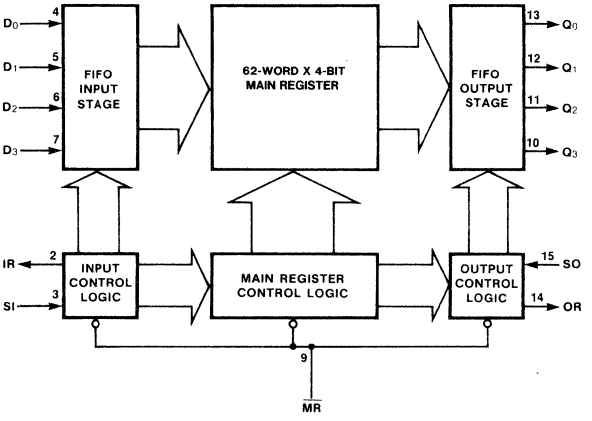
Connection Diagram 16-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	6Z	D
Plastic DIP	8K	P

Block Diagram



Functional Description

Data Input

The four bits of data on the D_0 through D_3 inputs are entered into the first bit location when both Input Ready (IR) and Shift In (SI) are HIGH ($\approx V_{SS}$). This causes IR to go LOW ($\approx V_{DD}$), but data will stay locked in the first bit location until both IR and SI are LOW. Then data will propagate to the second bit location, provided the location is empty. When data is transferred, IR will go HIGH indicating that the device is ready to accept new data. If the memory is full, IR will stay LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{BT} defines the time required for the first data to travel from the input to the output of a previously empty device, or for the first empty space to travel from the output to the input of a previously full device.

Data Output

When data has been transferred into the last cell, Output Ready (OR) goes HIGH, indicating the presence of valid data at the output pins Q_0 through Q_3. The transfer of data is initiated when both the Output Ready output from the device and the Shift Out (SO) input to the device are HIGH. This causes OR to go LOW; output data, however, is maintained until both OR and SO are LOW. Then the content of the adjacent (upstream) cell (provided it is full) will be transferred into the last cell, causing OR to go HIGH again. If the memory has been emptied, OR will stay LOW.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{BT}) or completely empty (Output Ready stays LOW for at least t_{BT}).

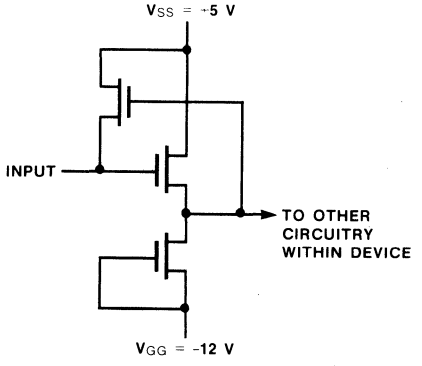
Reset

When Master Reset ($\overline{MR}$) goes LOW, the control logic is cleared. When $\overline{MR}$ returns HIGH, Output Ready (OR) stays LOW, and Input Ready (IR) goes HIGH if Shift In (SI) was LOW. Since the Data Outputs (Q_0 through Q_3) are unaffected by $\overline{MR}$, Data on Q_0 through Q_3 should be considered valid only while OR is HIGH.

Active Pull-up Description

TTL compatibility on each input is achieved through the use of active pull-up circuits that raise the input voltage to a value meeting the V_{IH} specification, i.e., $V_{IH} \geq V_{SS} - 1.0$ V. Each of these pull-up circuits may be thought of as a switched variable impedance between the input and V_{SS} with its state being dependent upon the input voltage, V_{IN}. When V_{IN} is LOW, the input impedance is on the order of several megohms, causing the input current to look like a leakage current. As V_{IN} swings toward a TTL HIGH value, the impedance decreases, providing a low-impedance path to V_{SS}, pulling V_{IN} up to the proper V_{IH} level. Furthermore, at $V_{IN} \geq V_{IH}$, the input characteristics resemble those of a TTL device making it look like a normal TTL load.

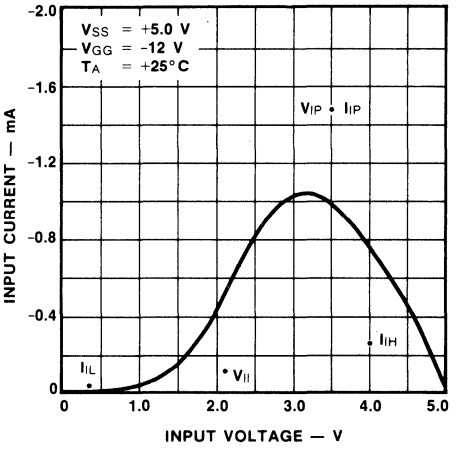
Input Buffer Stage With Active Pull-up

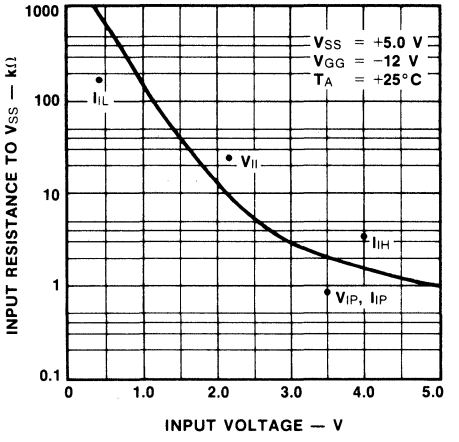


More specifically, the input current increases significantly when V_{IN} starts to exceed V_{II} (the pull-up initiation voltage). This current reaches a peak value of I_{IP} (the input barrier current) when $V_{IN} = V_{IP}$ (the peak input current voltage point) after which it decreases as V_{IN} rises to its V_{IH} value.

Although not usually necessary under low fan-out conditions, the active pull-up circuit on each input guarantees that the V_{IH} specification is met under all conditions where the 3341 is driven by a TTL-like structure.

Typical Input Characteristics





5

DC Characteristics V_{SS} = +5 V ± 5%, V_{GG} = −12 V ± 5%, V_{DD} = 0 V, T_A = 0°C to +70°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	V_{SS} −1.0			V	Notes 1 and 2
V_{IL}	Input LOW Voltage			0.8	V	Note 1
V_{OH}	Output HIGH Voltage	V_{SS} − 1.0			V	I_{OH} = −0.3 mA
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 1.6 mA
V_{II}	Input Pull-up Initiation Voltage			2.0	V	V_{SS} = 4.75 V
				2.2	V	V_{SS} = 5.25 V
V_{IP}	Peak Input Current Voltage Point			V_{SS} − 1.5	V	
I_{IH}	Input HIGH Current	−200			μA	Note 1, V_{IN} = V_{SS} − 1.0 V
I_{IL}	Input Leakage Current			−30	μA	Note 1, V_{IN} = 0 V
I_{IP}	Input Barrier Current			−1.6	mA	Note 1
I_{GG}	V_{GG} Current			−12	mA	
I_{DD}	V_{DD} Current			−45	mA	
P_D	Power Dissipation			450	mW	

Notes

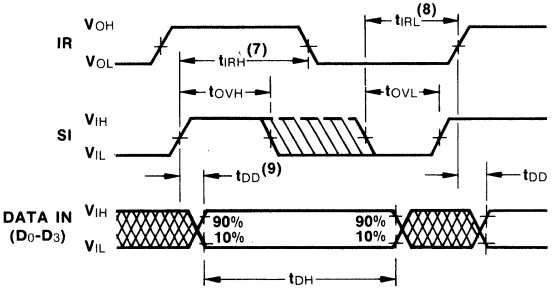
1. Inputs include D_0-D_3. Master Reset, Shift In, and Shift Out.
2. Internal pull-up circuits are provided on all inputs to insure proper HIGH level.
3. Control signals include Input Ready, Shift In, Output Ready, and Shift Out.
4. This parameter defines total time from the time data is loaded into the first word location to the time it is available at Q_0-Q_3 with the FIFO initially empty. Conversely, t_{BT} also defines the time required for an empty space to propagate from the last word location back to the first word location. When the FIFO is full, this is the time from the HIGH-to-LOW transition of OR to the LOW-to-HIGH transition of IR.
5. 1 TTL load +20 pF.
6. The $\overline{MR}$ input overrides all other control functions. It resets the control register and the input and output control logic while disabling any SI or SO inputs.
7. t_{IRH} is referenced to the positive going edge of IR or SI, whichever occurs later.
8. t_{IRL} is referenced to the negative going edge of IR or SI, whichever occurs later.
9. t_{DD} is referenced to the positive going edge of IR or SI, whichever occurs later.
10. t_{OVH} is referenced to the positive going edge of IR or SI, whichever occurs later.
11. t_{OVL} is referenced to the negative going edge of IR or SI whichever occurs later.
12. Data must be stable for t_{DH} or t_{IRH}, whichever is shorter.
13. t_{ORH} is referenced to the positive going edge of OR or SO, whichever occurs later.
14. t_{ORL} is referenced to the negative going edge of OR or SO, whichever occurs later.
15. t_{DV} is referenced to the negative going edge of OR or SO, whichever occurs later.
16. t_{OVH} is referenced to the positive going edge of IR or SI, whichever occurs later.
17. t_{OVL} is referenced to the negative going edge of IR or SI, whichever occurs later.

AC Characteristics V_{CC} = +5 V ± 5%, V_{DD} = 0 V, V_{GG} = −12 V ± 5%, T_A = 0°C to +70°C

		3341A			3341				
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Condition**
t_{IRH}	Input Ready HIGH Time	80		400	100	300	550	ns	*Figure 1*, Notes 7, 12
t_{IRL}	Input Ready LOW Time	100		550	138	300	550	ns	*Figure 1*, Note 8
t_{OVH}	Control Overlap HIGH Time	80			100			ns	*Figures 1, 2* and Notes 3, 16
t_{OVL}	Control Overlap LOW Time	80			100			ns	*Figures 1, 2* and Notes 3, 17
t_{DH}	Data Input Stable Time	200			400			ns	*Figure 1*
t_{DD}	Data Input Delay Time			0			25	ns	*Figure 1*, Note 9
t_{ORH}	Output Ready HIGH Time	80		450	100	300	500	ns	*Figure 2*, Note 13
t_{ORL}	Output Ready LOW Time	80		550	170	450	850	ns	*Figure 2*, Note 14
t_{BT}	Data Bubble-through Time			16			32	μs	Note 4
t_{DV}	Data Valid After SO or OR	75			75			ns	*Figure 2*, Note 15
t_{MRW}	Master Reset Pulse Width	400			400			ns	Note 6
t_{DA}	Data Output Available Time	0			0			ns	*Figure 2*
C_{IN}	Input Capacitance of Data and Control Lines			7.0			7.0	pF	f = 1 MHz, V_{IN} = V_{SS}
C_{MR}	Input Capacitance of $\overline{MR}$			7.0			15	pF	f = 1 MHz, V_{MR} = V_{SS}
f	Operating Frequency			1000			700	kHz	Note 5

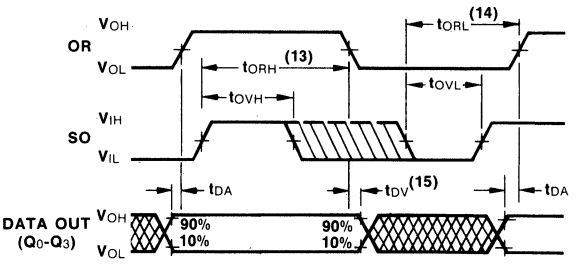
Timing Diagrams

Fig. 1 Input Timing



Input data must remain stable during timing window t_{DH}. Both SI and IR must be HIGH for t_{OVH}. Similarly, both SI and IR must be LOW for t_{OVL}.

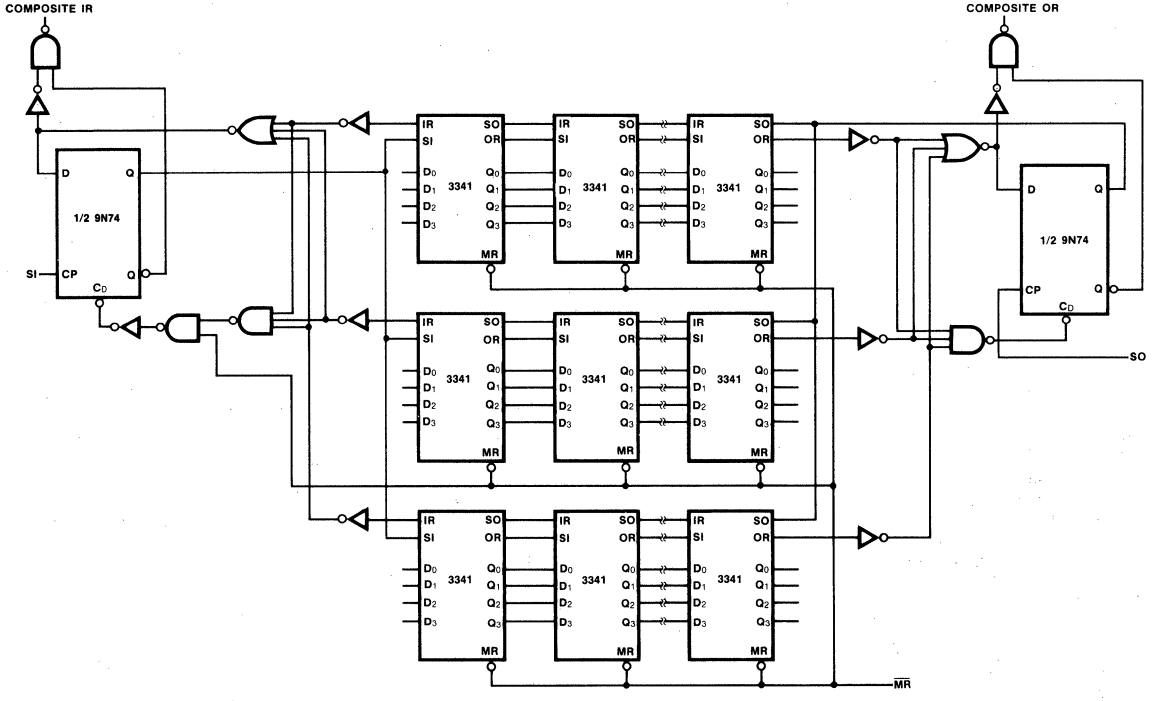
Fig. 2 Output Timing



Both SO and OR must be HIGH for t_{OVH}. Similarly both SO and OR must be LOW for t_{OVL}. Data will remain stable for t_{DV} after both SO and OR are LOW.

Application

Expansion of 3341 to n-Word by 12-Bit FIFO



Note

Composite Shift In should be LOW when Master Reset goes HIGH.
Input data may be changed after Composite IR goes LOW.
Composite IR will not go HIGH until Composite Shift In goes LOW.
When Composite IR goes HIGH, FIFOs will accept new data.
3341s will operate at full speed if these rules are followed.

3342
Quad 64-Bit Static Shift Register

MOS Memory Products

Description

The 3342 is a static shift register in quad 64-bit organization. An on-chip clock generator provides appropriate internal clock phases from a single external TTL-level clock input. Passive on-chip input pull-up resistors allow direct TTL compatibility on all inputs. The outputs are capable of driving a single TTL load directly without the need for external components. The 3342 is manufactured with p-channel silicon gate technology. It is available in ceramic or plastic 16-pin dual in-line packages in the commercial temperature range, 0°C to +70°C.

- **SINGLE TTL-COMPATIBLE EXTERNAL CLOCK**
- **DIRECT TTL COMPATIBILITY**
- **1.5 MHz OPERATION GUARANTEED**
- **LOW CLOCK CAPACITANCE**
- **INPUT OVERVOLTAGE PROTECTION**
- **EXTERNAL RECIRCULATE CONTROL**
- **16-PIN CERAMIC OR PLASTIC DUAL IN-LINE PACKAGE**

Pin Names

D_1-D_4	Data Inputs
REC_1-REC_4	Recirculate Inputs
CP	Clock Pulse Input
Q_1-Q_4	Data Outputs
V_{SS}	+5 V Power Supply
V_{DD}	0 V Power Supply
V_{GG}	−12 V Power Supply

Absolute Maximum Ratings

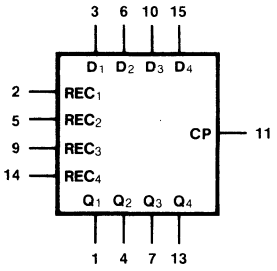
All Inputs Including Clock (Note 1)	−20 V to +0.3 V
V_{GG} (Note 1)	−20 V to +0.3 V
V_{DD} and Outputs (Note 1)	−7.0 V to +0.3 V
Output Current when Output is LOW (Note 2)	10 mA
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +70°C

Notes

1. All voltages with respect to V_{SS}
2. LOW logic level is the most negative level and HIGH logic level is the most positive.

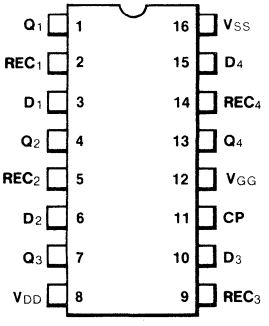
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Symbol



V_{SS} = Pin 16
V_{DD} = Pin 8
V_{GG} = Pin 12

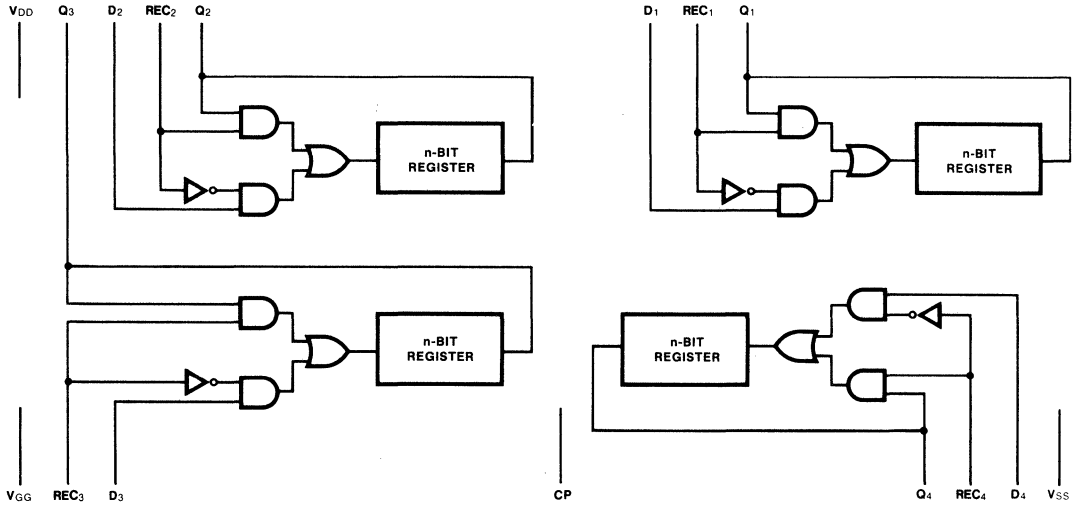
Connection Diagram 16-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	6Z	D
Plastic DIP	9B	P

Logic Diagram



Functional Description

The 3342 is a single phase static shift register. Data is accepted at the inputs when the external clock is HIGH. Data is available at the outputs after the negative clock transition as illustrated in the Timing Diagram. All inputs are connected by an MOS transistor to V_{SS} allowing complete TTL compatibility. The recirculate inputs allow data to be entered externally (LOW logic level) or internally recirculated in the registers (HIGH logic level). The output stages are push/pull amplifiers and can drive one TTL load.

DC Requirements V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, T_A = 0°C to +70°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	V_{SS} −1.0			V	Notes 1 and 2
V_{IL}	Input LOW Voltage	V_{GG}		0.80	V	Note 1

DC Characteristics V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, T_A = 0°C to +70°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{OH}	Output HIGH Voltage	2.4		V_{SS}	V	I_{OH} = −0.5 mA
V_{OL}	Output LOW Voltage	0		0.4	V	I_{OL} = −1.6 mA
I_{IH}	Input HIGH Current	−0.10			mA	V_{IN} = V_{SS} −1.0 V, Note 1
I_{IL}	Input LOW Current			−1.6	mA	V_{IN} = 0.4 V, Note 1
I_{IN}	Input Leakage Current			1.0	μA	V_{IN} = −5.0 V, Note 1 V_{GG} = V_{SS}
I_{DD}	V_{DD} Current			28	mA	
I_{GG}	V_{GG} Current			12	mA	
I_{SS}	V_{SS} Current			40	mA	
P_D	Power Dissipation			380	mW	t_{PWH} = 265 ns, f = 1.5 MHz

AC Requirements V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, T_A = 0°C to +70°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f	Operating Frequency	0		1.5	MHz	Note 4
t_{PWH}	Clock Pulse Width HIGH	0.265		10	μs	Note 3
t_{PWL}	Clock Pulse Width LOW	0.320			μs	
t_r, t_f	Clock Rise and Fall Times (10% to 90%)			1.0	μs	
t_{DS}	Data Input Set-up Time	200			ns	
t_{DH}	Data Input Hold Time	100			ns	
t_{RS}	Recirculate Set-up Time	200			ns	
t_{RH}	Recirculate Hold Time	130			ns	

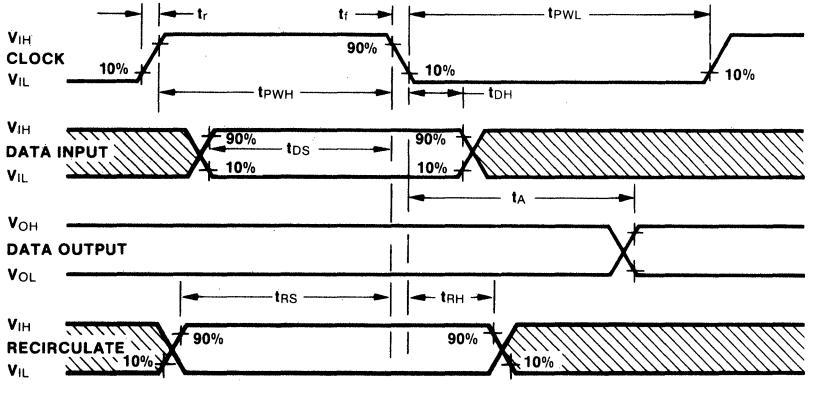
Notes

1. These parameters apply to all data, recirculate, and clock inputs.
2. On-chip pull-up resistors are provided on all inputs to effect the proper logic level when driving with TTL/DTL.
3. Outputs remain valid until negative-going edge of next clock pulse.
4. $1/f = t_{PWH} + t_{PWL} + t_r + t_f$.

AC Characteristics V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, T_A = 0°C to +70°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_A	Clock to Output Delay			265	ns	C_L = 10 pF Load = 1 TTL Input
C_{IN}	Capacitance All Inputs Including Clock			5.0	pF	V_{IN} = V_{SS}, f = 1.0 MHz

Timing Diagram



3348/3349
Hex 32-Bit
Static Shift Register

MOS Memory Products

Description

The 3348/3349 contains six separate 32-bit static shift registers constructed on a single chip using p-channel enhancement mode silicon gate MOS technology. Only two power pins, V_{SS} and V_{GG}, are needed for circuit operation. An on-chip clock generator provides all internal clock phases from a single TTL clock pulse. Each output is a bare drain, and therefore requires a 7.5 kΩ load resistor to V_{GG}. A recirculate data input allows the user to either enter data from the outside (LOW logic level) or to internally recirculate the contents of the registers (HIGH logic level).

The 3348 is available in a 24-pin ceramic dual in-line package and the 3349 is available in a 16-pin plastic or ceramic dual in-line package. The 3348 option provides an output enable pin for wired-OR operation. The outputs are enabled when Output Enable is LOW.

- **SINGLE TTL EXTERNAL CLOCK**
- **INPUT OVERVOLTAGE PROTECTION**
- **LOW CLOCKLINE CAPACITANCE**
- **TTL COMPATIBLE INPUTS**
- **CASCADE CAPABILITY**
- **SINGLE POWER SUPPLY OPERATION**
- **INTERNAL RECIRCULATION CONTROL**
- **DC TO 1 MHz OPERATION GUARANTEED**
- **OUTPUT ENABLE CONTROL (3348 ONLY)**
- **SINGLE-ENDED (BARE DRAIN) BUFFERS**

Pin Names

D_1-D_6	Data Inputs
$\overline{REC}$	Recirculate Input
$\overline{CP}$	Clock Pulse
$\overline{OE}$	Output Enable (3348 only)
Q_1-Q_6	Data Outputs

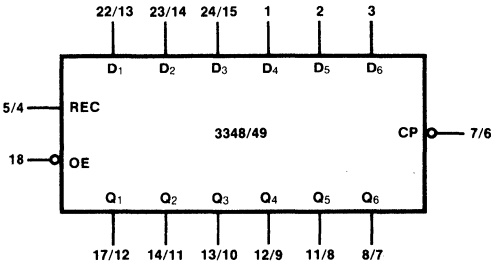
Absolute Maximum Ratings

All Inputs, V_{GG}	−22 V to +0.3 V
All Outputs	−19 V to +0.3 V
Output Current	+10 mA
Storage Temperature	−55° C to +150° C
Operating Temperature	0°C to 70°C

All voltages with respect to V_{SS}.

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Symbol

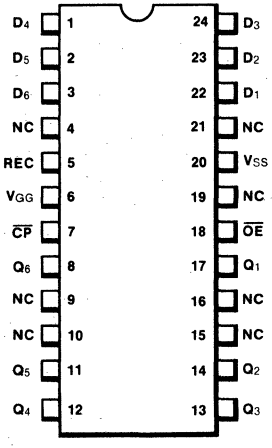


V_{SS} = Pin 20 (24-Pin DIP), Pin 16 (16-Pin DIP)
V_{GG} = Pin 6 (24-Pin DIP), Pin 5 (16-Pin DIP)

Connection Diagrams

24-Pin DIP

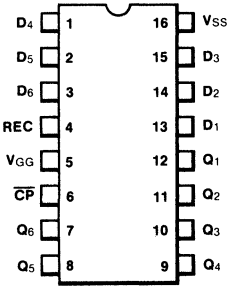
3348



(Top View)

16-Pin DIP

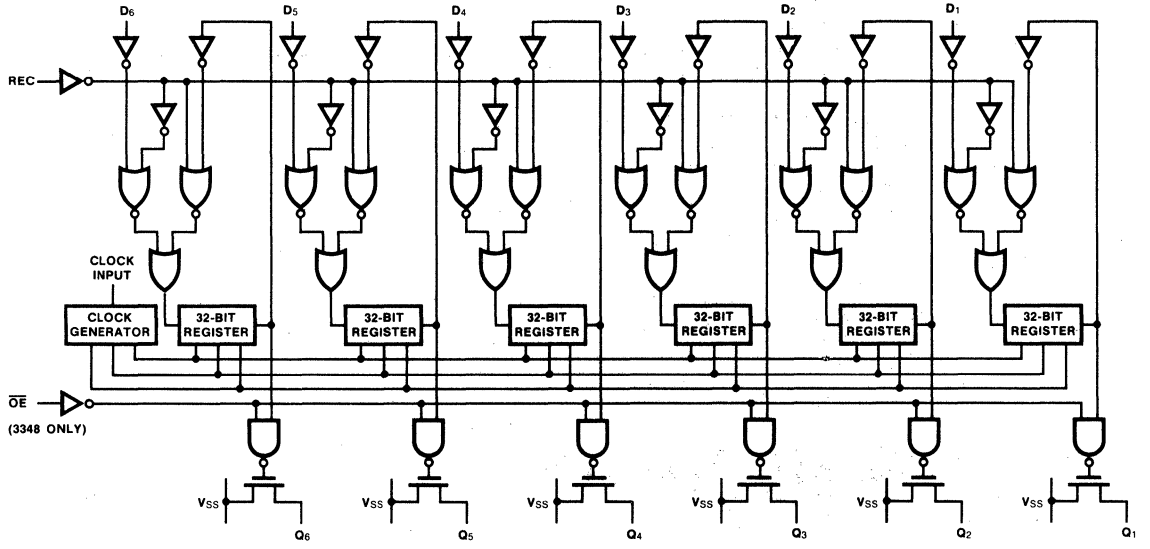
3349



(Top View)

	Package	Outline	Order Code
3348	Ceramic DIP	7M	D
3349	Ceramic DIP	6Z	D
	Plastic DIP	9B	P

Block Diagram



Functional Description

The 3348/3349 is a two-phase Static Shift Register. The single external clock phase generates two shift phases as well as a static operation phase via the on-chip clock generator. Data is accepted at the inputs after the negative-going transition of the external clock. Output information is available after the positive clock transition as illustrated in Timing Diagram. For long-term storage, the external clock should be held HIGH.

DC Requirements V_{SS} = 5 V ±5%, V_{GG} = −12 ±1 V, T_A = 0° C to 70° C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	V_{SS} − 1.5			V	All Inputs Including Clocks
V_{IL}	Input LOW Voltage			0.6	V	All Inputs Including Clocks
R_L	Output Load Resistor to V_{GG}	7.5			kΩ	

DC Characteristics V_{SS} = 5 V ±5%, V_{GG} = −12 ±1 V, T_A = 0° C to 70° C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{OH}	Output HIGH Voltage	V_{SS} − 1.2			V	7500 Ω Load to V_{GG} V_{SS} = 4.75 V, V_{GG} = −11 V
I_{IN}	Input Leakage Current			1.0	μA	V_{IN} = 0 V
I_{GG}	V_{GG} Current			27	mA	V_{GG} = −12 V, V_{SS} = 5.0 V

AC Requirements V_{SS} = 5 V ±5%, V_{GG} = −12 ±1 V, T_A = 0° C to 70° C

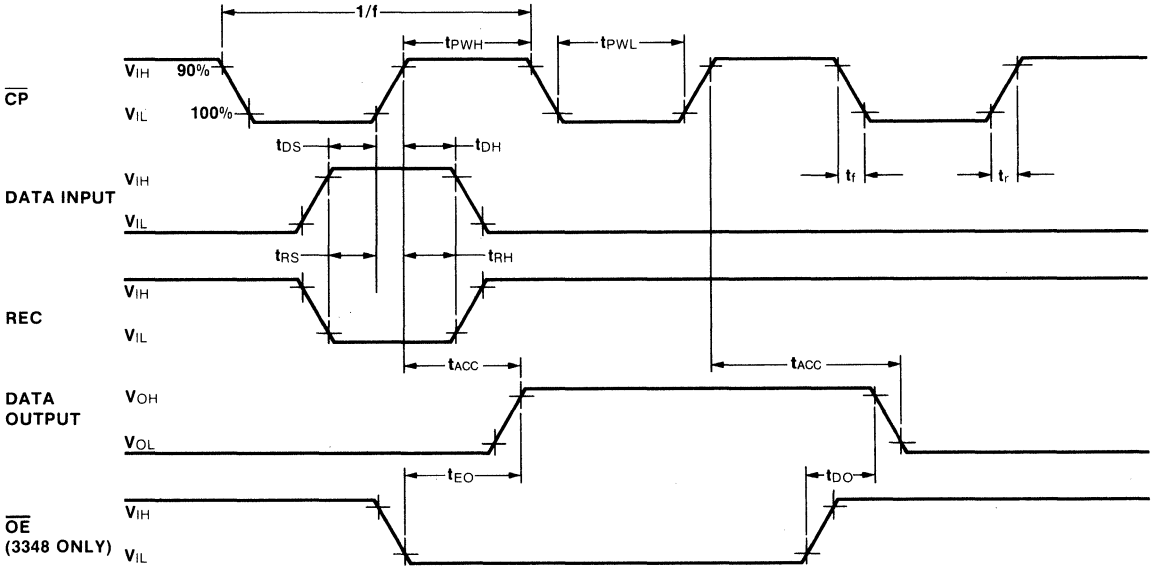
Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f	Operating Frequency			1.0	MHz	
t_{PWL}	Clock Pulse Width LOW	0.35		50	μs	
t_{PWH}	Clock Pulse Width HIGH	0.6			μs	
t_r, t_f	Clock Rise Time and Fall Time			0.5	μs	
t_{DS}	Input Data Set-up Time	180			ns	
t_{DH}	Input Data Hold Time	40			ns	
t_{RPW}	Recirculate Pulse Width	350			ns	
t_{RS}	Recirculate Set-up Time	225			ns	
t_{RH}	Recirculate Hold Time	100			ns	

5

AC Characteristics V_{SS} = 5 V ±5%, V_{GG} = −12 ±1 V, T_A = 0° C to 70° C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_{ACC}	Clock to Output Delay Time	125		520	ns	C_L = 0 to 20 pF, R_L = 7.5 kΩ
t_{EO}	Output Enable Delay Time (3348 Only)			350	ns	C_L = 20 pF, R_L = 7.5 kΩ to V_{GG}
t_{DO}	Output Disable Delay Time (3348 Only)			350	ns	

Timing Diagram



3351
40 x 9 FIFO Memory

MOS Memory Products

Description

The 3351 is a First-In First-Out (FIFO) memory used in data rate buffering applications. The 3351 has a capacity of 40 9-bit words. The words are accepted at the input, automatically shifted towards the output, and removed at any rate in the same sequence in which they were entered.

The 3351 has status indicators on both the input and output to signal an available empty input or a valid data word at the output. It also has separate input and output enable lines, in addition to a master reset line. A unique input stage interfaces to TTL without external components. The 3351 is manufactured using the p-channel Isoplanar silicon gate process with ion-implantation.

- **2 MHz (3351-1), 1.5 MHz (3351-3), AND 1 MHz (3351-2) DATA RATES**
- **INDEPENDENT ASYNCHRONOUS INPUTS AND OUTPUTS**
- **FULLY TTL COMPATIBLE**
- **3-STATE OUTPUTS**
- **INPUT AND OUTPUT ENABLE CONTROLS**
- **EXPANDABLE IN EITHER DIRECTION**
- **STATUS INDICATORS ON INPUT AND OUTPUT**
- **28-PIN CERAMIC DUAL IN-LINE PACKAGE**

Pin Names

D_0-D_8	Data Inputs
$\overline{MR}$	Master Reset
$\overline{IE}$	Input Enable
IR	Input Ready
SI	Shift In
$\overline{SO}$	Shift Out
$\overline{OE}$	Output Enable
OR	Output Ready
Q_0-Q_8	Data Outputs

Absolute Maximum Ratings

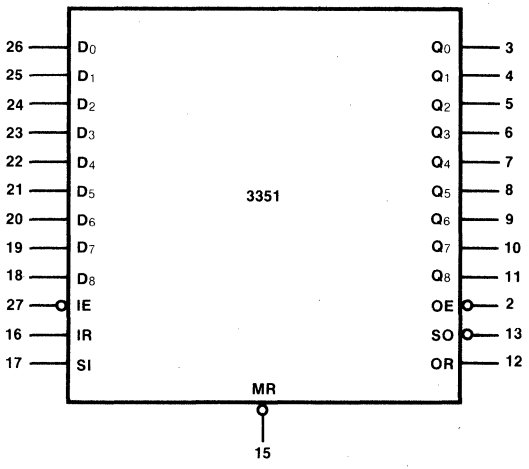
V_{GG} and Inputs	−20 V to +0.3 V
V_{DD} and Outputs	−7.0 V to +0.3 V
Output Sink Current	5.0 mA
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +70°C

Note

All Voltages with respect to V_{SS}.

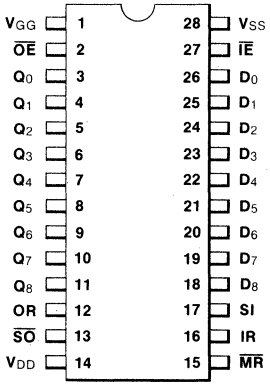
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Symbol



V_{SS} = Pin 28
V_{DD} = Pin 14
V_{GG} = Pin 1

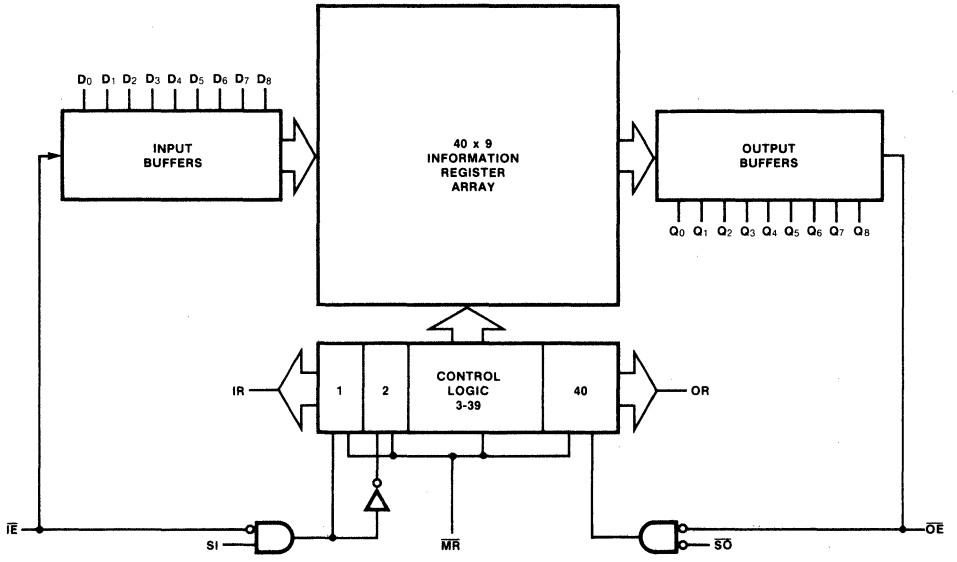
Connection Diagram 28-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	8E	D

Block Diagram

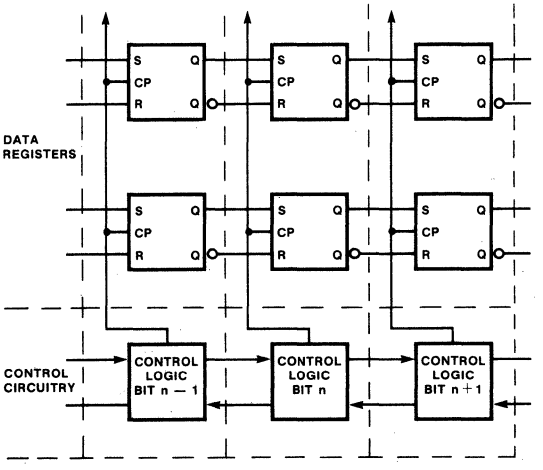


Functional Description

The 40 by 9 memory array is under the constant control of a control logic network. Each word position in the array is clocked by a control register, which also stores a marker bit; a "1" signifies that the position is filled and a "0" indicates a vacancy at that location. Each control register clocks data from the preceding nine data flip-flops to its own set of nine data flip-flops. The register logic detects the status of the preceding and succeeding registers' marker bits to determine when to clock its data flip-flops. When data has been transferred from location n to location n+1, the n+1 control circuitry changes the marker bit at control register n from a "1" to a "0", indicating that the data at location n has been transferred elsewhere in the array. This "0" will then propagate back to the first control register signifying that the FIFO is capable of accepting more data.

The 3351 buffers the first and last control registers and uses them as input/output status indicators. Since all status marker "0s" propagate toward the first control register, a "0" at the first register indicates the FIFO is ready to clock in more data.

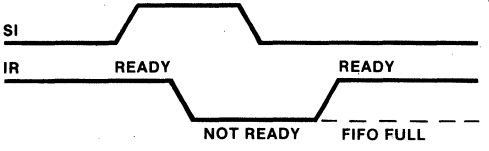
Likewise, all "1s" propagate towards the last control register, and a "1" here means that data is valid at the outputs.



A Master Reset control is provided to set all the control registers' status markers to "0". Note that the data registers are not reset by $\overline{MR}$.

Shift In (SI), Input Ready (IR)
A LOW-to-HIGH transition of the Shift In command does two things: 1) the first control register is enabled, permitting input data to be loaded into the first set of data registers and setting the first marker bit to a "1", and 2) the second control register is locked out by means of an inverted SI command. At this point, data from the first data register cannot be transferred to the second data register. The Input Ready signal indicates the status of the first marker bit and accordingly goes LOW (not ready).

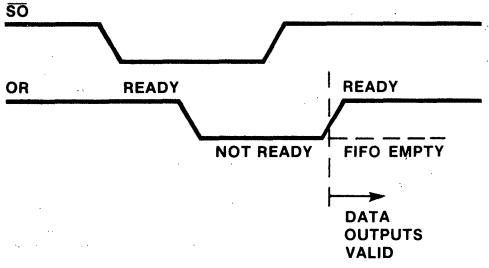
The HIGH-to-LOW transition of the SI locks out the first control register and causes data from the first data registers to propagate down the FIFO under the control of the control logic. This action sets the first marker bit to a "0" and the Input Ready returns HIGH (input ready). When the FIFO becomes full, the IR will stay LOW after SI returns LOW and any further SI commands will be ignored by the circuit. When a "0" ripples back from the last to the first control register the Input Ready (IR) will return to HIGH (if SI is LOW).



Input Enable ($\overline{IE}$)
A HIGH on the Input Enable disables the SI input and the current-sourcing capability of the special TTL pull-up networks of the data inputs and the SI. A LOW enables these inputs.

Shift Out ($\overline{SO}$), Output Ready (OR)
The HIGH-to-LOW transition of Shift Out command disables the clocking line of the last control register and changes the 40th bit marker to a "0". The Output Ready is then forced LOW. Note that data is not transferred from the 39th position to the 40th position on this edge. When $\overline{SO}$ makes the LOW-to-HIGH transition, the FIFO is again under control of its control logic circuitry, new data is transferred to the 40th location and the 40th marker bit is reset to a "1". The Output Ready returns to HIGH, signifying the new data at the output leads is now valid.

When the FIFO is empty, the OR remains LOW after $\overline{SO}$ goes HIGH. $\overline{SO}$ commands will be ignored until a "1" marker ripples down to the last control register, after which the OR goes HIGH (if $\overline{SO}$ is HIGH).



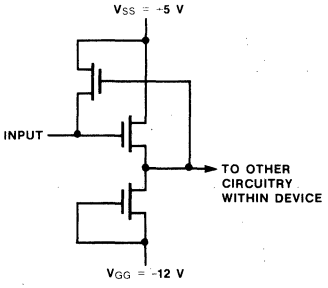
Output Enable ($\overline{OE}$)
A HIGH on Output Enable forces the nine outputs to a high impedance state, disables the shift out command, and disables the current-sourcing capability of the special TTL pull-up network of $\overline{SO}$. A LOW again enables $\overline{SO}$, and the outputs revert back to their normal TTL states.

Master Reset ($\overline{MR}$)
A LOW on Master Reset sets all the control logic marker bits to "0". Consequently, IR will go HIGH (if SI is LOW) and OR will go LOW, indicating that the FIFO is now empty.

Active Pull-up Description

TTL compatibility on each input is achieved through the use of active pull-up circuits which raise the input voltage to a value meeting the V_{IH} specification, i.e., $V_{IH} \geq V_{SS} - 1.0$ V. Each of these pull-up circuits may be thought of as a switched variable impedance between the input and V_{SS} with a state dependent upon the input voltage, V_{IN}. When V_{IN} is LOW, the input impedance is on the order of several megohms, causing the input current to look like a leakage current. As V_{IN} swings toward a TTL HIGH value, the input impedance decreases, providing a low impedance path to V_{SS}, pulling V_{IN} up to the proper V_{IH} level. Furthermore, at $V_{IN} \geq V_{IH}$, the input characteristics resemble those of a TTL device making it look like a normal TTL load.

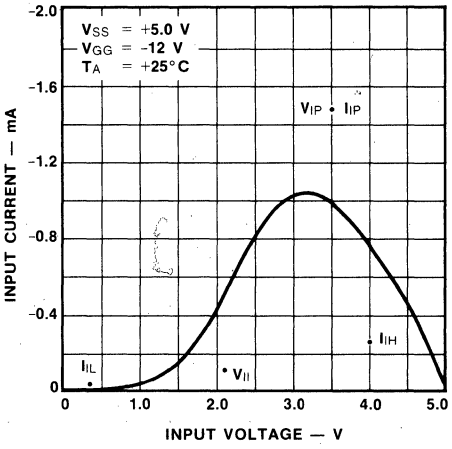
Input Buffer Stage With Active Pull-Up

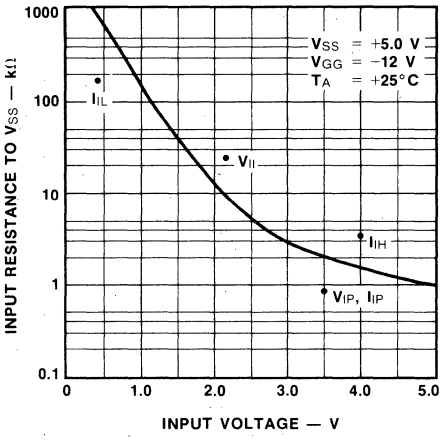


More specifically, the input current increases significantly when V_{IN} starts to exceed V_{II} (the pull-up initiation voltage). This current reaches a peak value of I_{IP} (the input barrier current) when $V_{IN} = V_{IP}$ (the peak input current voltage point) after which it decreases as V_{IN} rises to its V_{IH} value.

Although not usually necessary under low fan-out conditions, the active pull-up circuit on each input guarantees that the V_{IH} specification is met under all conditions where the 3351 is driven by a TTL-like structure.

Typical Input Characteristics





DC Requirements V_{SS} = 5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, T_A = 0°C to 70°C

		3351-1		3351-2		3351-3			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Condition**
V_{IH}	Input HIGH Voltage	V_{SS}−1.0	V_{SS}+0.3	V_{SS}−1.0	V_{SS}+0.3	V_{SS}−1.0	V_{SS}+0.3	V	Note
V_{IL}	Input LOW Voltage	V_{GG}	0.8	V_{GG}	0.8	V_{GG}	0.8	V	Note

DC Characteristics V_{SS} = 5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%

		3351-1		3351-2		3351-3			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Condition**
V_{OH1}	Output HIGH Voltage	V_{SS}−0.5		V_{SS}−0.5		V_{SS}−0.5		V	I_{OH} = 50 μA
V_{OH2}	Output HIGH Voltage	2.4		2.4		2.4		V	I_{OH} = −0.2 mA
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	V	I_{OL} = 1.6 mA
V_{II}	Pull-up Initiation Voltage		2.2		2.2		2.2	V	Note I_{IN} = −0.12 mA
V_{IP}	Peak Current Voltage		V_{SS}−1.5		V_{SS}−1.5		V_{SS}−1.5	V	Note
I_{IP}	Peak Current		−1.6		−1.6		−1.6	mA	Note
I_{IH}	Input HIGH Current	−0.22		−0.22		−0.22		mA	Note V_{IN} = V_{SS} −1.0 V
I_{IL}	Input LOW Current		−50		−50		−50	μA	Note V_{IN} = 0.4 V
I_{DD}	V_{DD} Current		65		50		50	mA	
I_{GG}	V_{GG} Current		10		8.0		8.0	mA	
P_D	Power Dissipation		520		420		420	mW	

Note
Includes all Data inputs, $\overline{IE}$, $\overline{OE}$, SI, $\overline{SO}$ and $\overline{MR}$. (See Active Pull-up description.)

AC Requirements V_{SS} = 5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, T_A = 0°C to 70°C. See Notes 1 and 2

Symbol	Characteristic	3351-1		3351-2		3351-3		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{IDS}	$\overline{IE}$ Disable Set-Up Time	20		20		20		ns	*Fig. 1*
t_{IDH}	$\overline{IE}$ Disable Hold Time	20		20		20		ns	
t_{IES}	$\overline{IE}$ Enable Set-Up Time	0		0		0		ns	
t_{IEH}	$\overline{IE}$ Enable Hold Time	0		0		0		ns	
t_{DS}	Input Data Set-Up Time	0		0		0		ns	
t_{DH}	Input Data Hold Time	220		440		330		ns	
t_{SIH}	SI HIGH Time	220		440		300		ns	
t_{SIL}	SI LOW Time	280		560		370		ns	
t_{ODS}	$\overline{OE}$ Disable Set-Up Time	20		20		20		ns	*Fig. 2*
t_{ODH}	$\overline{OE}$ Disable Hold Time	20		20		20		ns	
t_{OES}	$\overline{OE}$ Enable Set-Up Time	0		0		0		ns	
t_{OEH}	$\overline{OE}$ Enable Hold Time	0		0		0		ns	
t_{SOL}	$\overline{SO}$ LOW Time	200		400		260		ns	
t_{SOH}	$\overline{SO}$ HIGH Time	300		600		410		ns	
t_{RPW}	$\overline{MR}$ Pulse Width	100		200		150		ns	*Fig. 3*
t_{RS}	$\overline{MR}$ to SI Set-Up Time	0		0		0		ns	

Notes

1. All input t_r and t_f: 10 ns.
2. All time measurements referenced to 50% level.

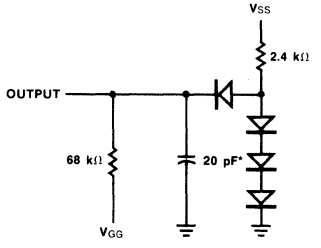
AC Characteristics V_{SS} = 5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%. See Notes 3, 4 and Output Loading

		3351-1		3351-2		3351-3			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Condition**
$t_{SI-IRHL}$	SI to IR Delay Time		220		440		300	ns	*Fig. 1* (Note 1)
$t_{SI-IRLH}$	SI to IR Delay Time		280		560		370	ns	
$t_{SO-ORLL}$	$\overline{SO}$ to OR Delay Time		200		400		300	ns	(Note 1)
$t_{SO-ORHH}$	$\overline{SO}$ to OR Delay Time		300		600		410	ns	
t_{MR-IR}	$\overline{MR}$ to IR Delay Time		300		480		480	ns	*Fig. 2*
t_{MR-OR}	$\overline{MR}$ to OR Delay Time		300		480		480	ns	
t_{BT}	Bubble-Through Time		9.0		15		15	μs	(Note 2)
t_E	Output Enable Time		300		600		480	ns	*Fig. 3*
t_D	Output Disable Time		300		600		480	ns	
f	Operating Frequency		2.0		1.0		1.5	MHz	

Notes

1. HL means positive-going edge of first signal to negative-going edge of second signal, etc.
2. Forward and reverse.
3. All input t_r and t_f: 10 ns.
4. All time measurements referenced to 50% level.

Output Loading



All Diodes 1N4152
*Includes Scope and Jig Capacitance

Timing Diagrams

Fig. 1 Input Timing

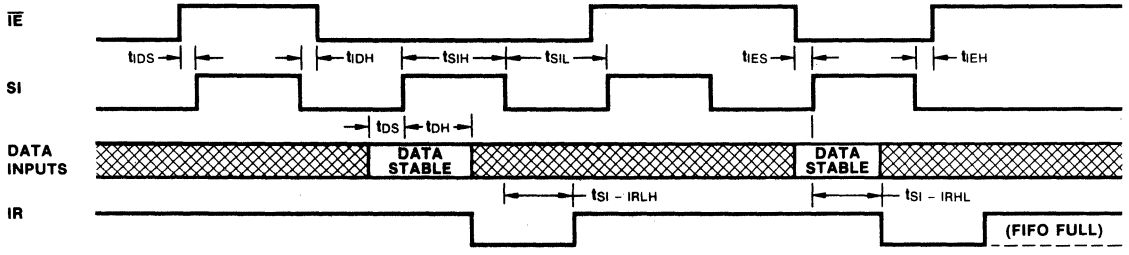


Fig. 2 Output Timing

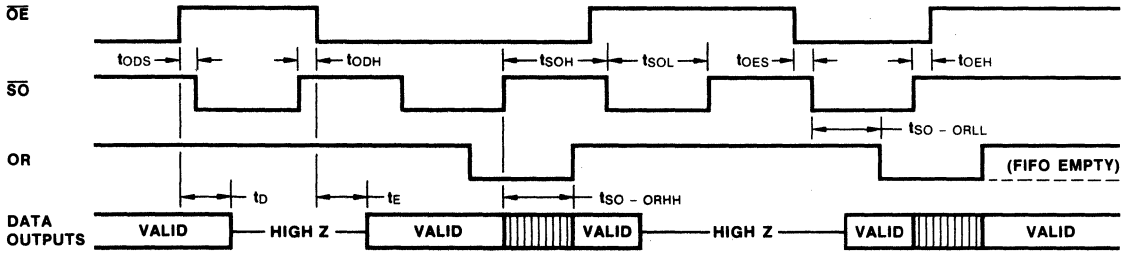
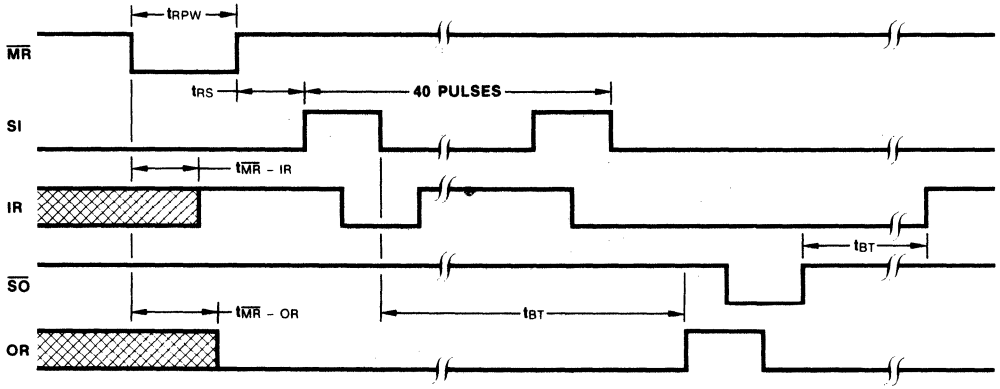


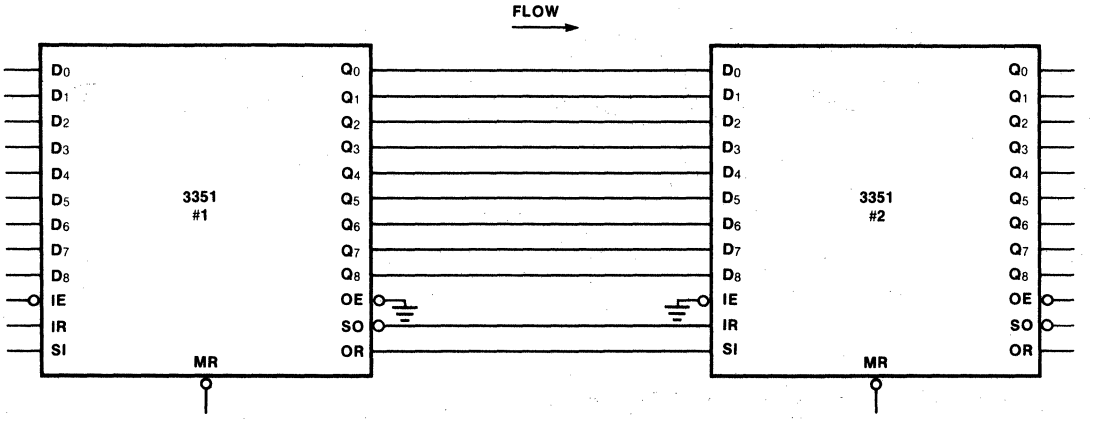
Fig. 3 Bubble-through Timing



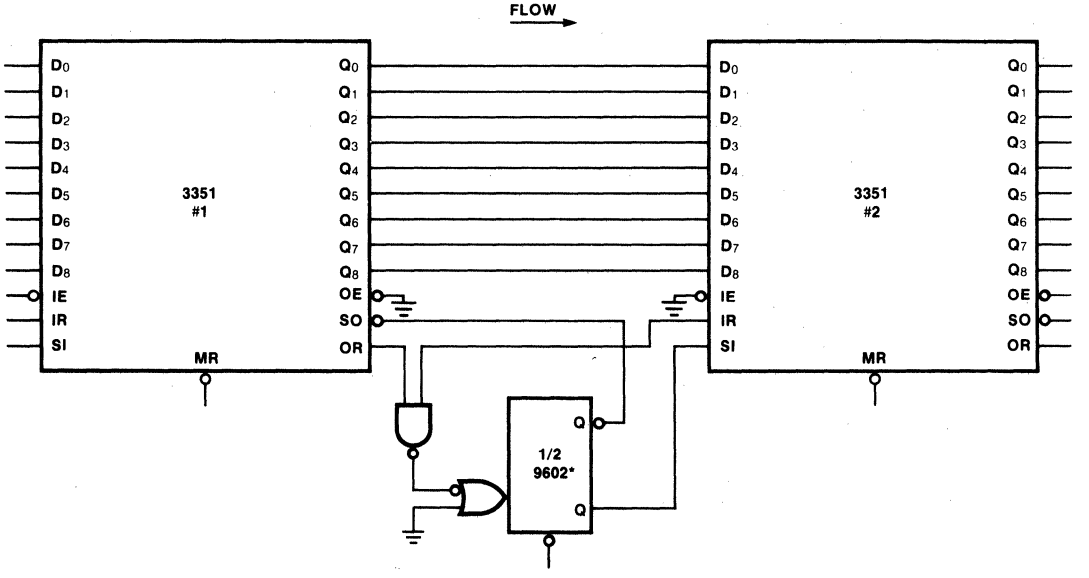
KEY:
HIGH Z — HIGH IMPEDANCE STATE
OUTPUT TRANSITION
DON'T CARE

Applications

Simple Word Expansion (39 n + 1) Words



High Speed-Word Expansion



*Adjust pulse width for t_{SIH}

3357/F2847
Quad 80-Bit Static Shift Register

MOS Memory Products

Description

The 3357 and F2847 are single phase quad 80-bit static shift registers. Both have an on-chip clock generator that is driven by a single phase TTL clock. A multiplexer is provided to allow data to be entered from the input or recirculated from the output. A unique on-chip input pull-up circuit allows interfacing directly from TTL to all inputs without external components.

The 3357 and F2847 are manufactured with the p-channel Isoplanar process and are available in 16-pin ceramic or plastic dual in-line packages in the commercial temperature range.

- **4.0 MHz (33571), 3.0 MHz (F2847) AND 2.0 MHz (33572) GUARANTEED OPERATION**
- **ZERO DATA HOLD TIME**
- **TTL COMPATIBILITY**
- **SINGLE PHASE TTL CLOCK**
- **LOW CLOCK CAPACITANCE**
- **INPUT MULTIPLEXER**
- **16-PIN CERAMIC OR PLASTIC DUAL IN-LINE PACKAGE**
- **LOW POWER VERSION (F2847L)**

Pin Names

D_1-D_4	Data Inputs
REC_1-REC_4	Recirculate Inputs
CP	Clock Input
Q_1-Q_4	Data Outputs

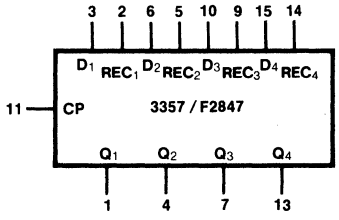
Absolute Maximum Ratings

V_{GG} and Inputs	−20 V to +0.3 V
V_{DD} and Outputs	−7.0 V to +0.3 V
Output Sink Current	10 mA
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +70°C

All voltages with respect to V_{SS}.

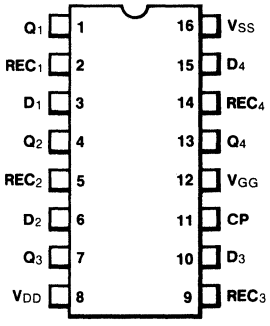
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Symbol



V_{SS} = Pin 16
V_{DD} = Pin 8
V_{GG} = Pin 12

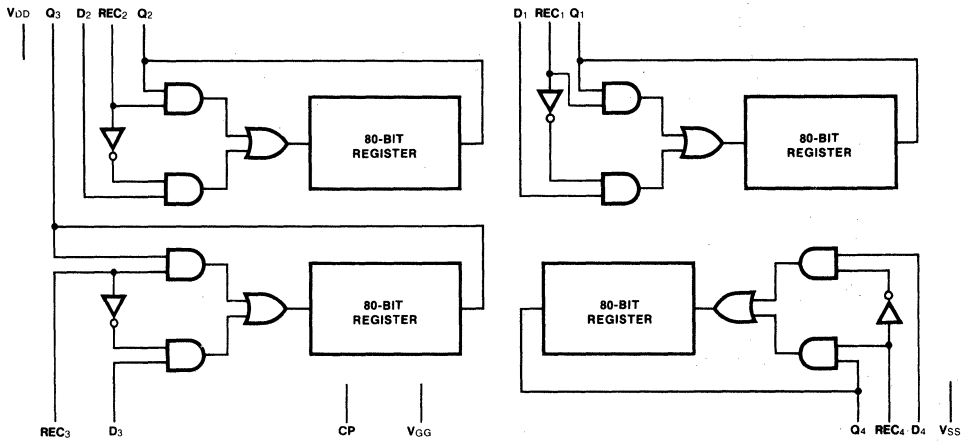
Connection Diagram 16-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	6Z	D
Plastic DIP	9B	P

Block Diagram



Functional Description

The 3357 and F2847 are single phase quad 80-bit static shift registers. Data is loaded into the register on the negative transition of the external clock. The Recirculate input loads new data from the input or recirculates old data from the output. A LOW on Recirculate loads data from the input, and a HIGH loads data from the output.

Output Characteristics

Each output will drive one unit TTL load (1.6 mA at 0.4 V) directly or another unit Shift Register load without any external components.

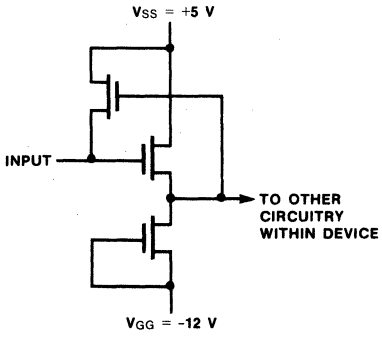
Active Pull-up Description

TTL compatibility on each input is achieved through the use of active pull-up circuits which raise the input voltage to a value meeting the V_{IH} specification, i.e., $V_{IH} \geq V_{SS} - 1.0$ V. Each of these pull-up circuits may be thought of as a switched variable impedance between the input and V_{SS} whose state is dependent upon the input voltage, V_{IN}. When V_{IN} is LOW, the input impedance is on the order of several megohms, causing the input current to look like a leakage current. As V_{IN} swings toward a TTL HIGH value, the input impedance decreases, providing a low impedance path to V_{SS}, pulling V_{IN} up to the proper V_{IH} level. Furthermore, at $V_{IN} \geq V_{IH}$, the input characteristics resemble those of a TTL device making it look like a normal TTL load.

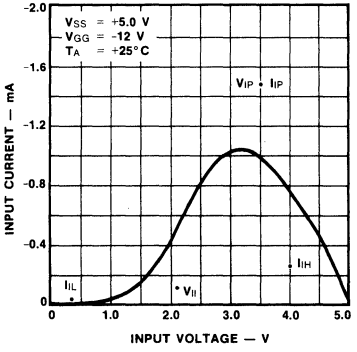
More specifically, the input current increases significantly when V_{IN} starts to exceed V_{II} (the Pull-up Initiation voltage). This current reaches a peak value of I_{IP} (the Input Barrier current) when $V_{IN} = V_{IP}$ (the Peak Input Current Voltage Point) after which it decreases as V_{IN} rises to its V_{IH} value. See Typical Input Characteristics.

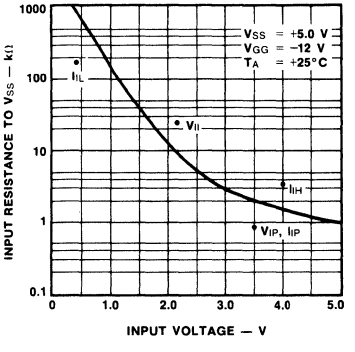
Although not usually necessary under low fan-out conditions, the active pull-up circuit on each input guarantees that the V_{IH} specification is met under all conditions where the 3357 or F2847 is driven by a TTL-like structure.

Input Buffer Stage With Active Pull-up



Typical Input Characteristics





5

DC Requirements T_A = 0°C to +70°C, V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%

Symbol	Characteristic	Min	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	V_{SS} − 1	V_{SS} + 0.3	V	Note
V_{IL}	Input LOW Voltage	V_{GG}	+0.8	V	Note

DC Characteristics T_A = 0°C to +70°C, V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%

Symbol	Characteristic		Min	Max	Unit	Condition
V_{OH}	Output HIGH Voltage		V_{SS} − 1		V	I_{OH} = −0.1 mA
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 1.6 mA
V_{II}	Input Pull-up Initiation Voltage			2.2	V	Note, I_{IN} < −0.12 mA
V_{IP}	Input Peak Current Voltage			V_{SS} − 1.5	V	Note
I_{IP}	Input Peak Current			−1.6	mA	Note
I_{IH}	Input HIGH Current		−0.22		mA	Note, V_{IN} = V_{SS} − 1.0 V
I_{IL}	Input LOW Current			−30	μA	Note, V_{IN} = 0.4 V
I_{DD}	V_{DD} Current	3357-1		−20	mA	Max Operating Frequency
		3357-2		−18	mA	
		F2847L		−20	mA	
		F2847		−35	mA	
I_{GG}	V_{GG} Current	3357-1		−15	mA	
		3357-2		−10.5	mA	
		F2847L		−12	mA	
		F2847		−15	mA	
P_D	Power Dissipation	3357-1		375	mW	
		3357-2		285	mW	
		F2847L		320	mW	
		F2847		455	mW	

Note
Applies to all inputs including Clock.

AC Requirements $T_A = 0°C$ to $+70°C$, $V_{SS} = +5.0\ V \pm 5\%$, $V_{DD} = 0\ V$, $V_{GG} = -12\ V \pm 5\%$

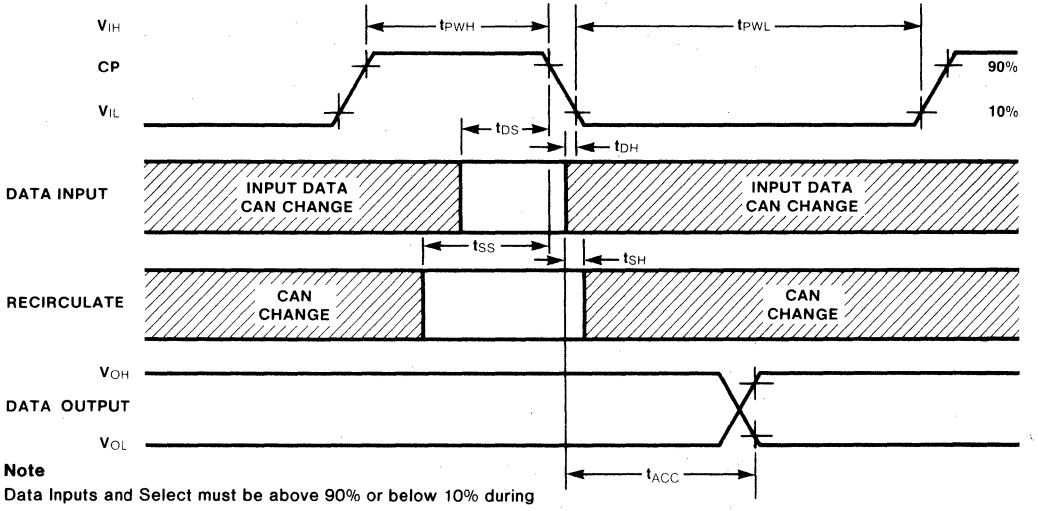
Symbol	Characteristic	3357-1		F2847-F2847L		3357-2		Unit	Condition
		Min	Max	Min	Max	Min	Max		
f	Operating Frequency	0	4.0	0	3.0	0	2.0	MHz	
t_{PWH}	Clock Pulse Width HIGH	0.095	100	0.14	100	0.25	100	μs	See Timing Diagram, Note
t_{PWL}	Clock Pulse Width LOW	0.135		0.14		0.25		μs	
t_{DS}	Data Set-up Time	25		120		40		ns	
t_{DH}	Data Hold Time	30		40		30		ns	
t_{SS}	Select Set-up Time	40		70		70		ns	
t_{SH}	Select Hold Time	10		10		10		ns	

AC Characteristics $T_A = 0°C$ to $+70°C$, $V_{SS} = +5.0\ V \pm 5\%$, $V_{DD} = 0\ V$, $V_{GG} = -12\ V \pm 5\%$

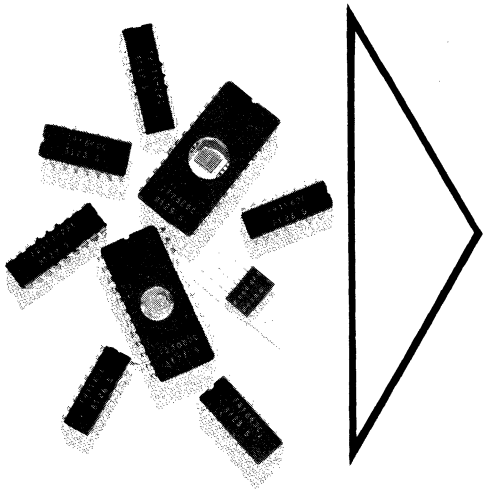
Symbol	Parameter		Min	Max	Unit	Condition
C_{IN}	Input Capacitance			5.0	pF	All inputs
C_{OUT}	Output Capacitance			5.0	pF	
t_{ACC}	Clock to Output Delay Time	3357-1		215	ns	See Timing Diagram
		3357-2		260		
		F2847L		200		
		F2847		200		

Note
t_r, t_f = Clock Transition Time = 0.5 μs.

Timing Diagram



Note
Data Inputs and Select must be above 90% or below 10% during valid time.



3262A
TV Sync Generator

MOS Memory Products

Description

The 3262A is a sync pulse generator that produces the necessary outputs for synchronizing television broadcast information. These outputs include Horizontal Drive, Vertical Drive, Composite Sync, Composite Blanking, and Even and Odd Fields, all of which are provided in the format specified by RS170EIA Standard Output Signals. The Color Subcarrier (3.58 MHz) and the Color Burst Flag outputs are provided for color operation. All waveforms are derived from a low-voltage two-phase clock (for color operation) or a single-phase clock (for black and white operation). All outputs except the Color Subcarrier are capable of driving a TTL load directly. The Color Subcarrier is designed to drive a capacitive load. The 3262A is a monolithic integrated circuit manufactured with Isoplanar p-channel silicon gate technology.

- **COLOR OR BLACK/WHITE OPERATION**
- **ALL COUNTERS SYNCHRONOUS**
- **PULSE WIDTHS DERIVED DIGITALLY**
- **OUTPUTS DRIVE TTL DIRECTLY (EXCEPT COLOR SUBCARRIER)**
- **SEPARATE VERTICAL AND HORIZONTAL RESET**

Applications

- **CAMERA LOGIC REPLACEMENT**
- **HOME TV GAMES**
- **VIDEO TAPE RECORDS**
- **VIDEO TERMINALS**

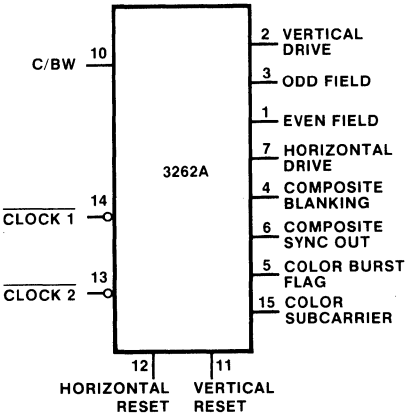
Absolute Maximum Ratings

All Inputs (Note)	−20 V to +0.3 V
V_{GG}	−20 V to +0.3 V
V_{DD} and Outputs	−6 V to +0.3 V
DC Output Current (output LOW)	<10 mA
Storage Temperature	−55°C to 150°C
Operating Temperature	0°C to 70°C
Maximum Power Dissipation	750 mW

All Voltages with respect to V_{SS}

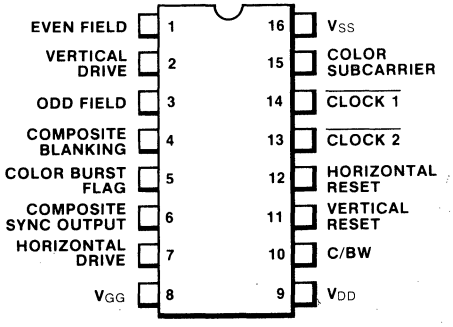
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Symbol



V_{SS} = Pin 16
V_{DD} = Pin 9
V_{GG} = Pin 8

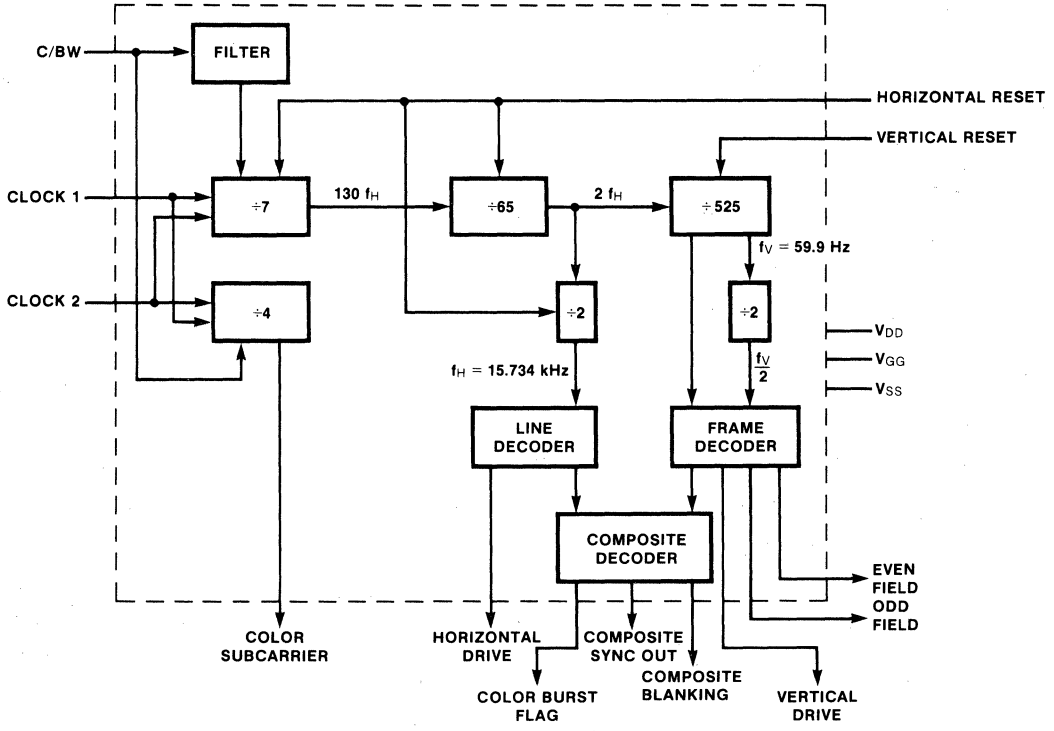
Connection Diagram
16-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	6Z	D

Block Diagram



Functional Description

The 3262A block diagram shows the counting and decoding scheme used to generate all output waveforms. The clock frequency is divided down in three steps (÷7, ÷65, ÷2) and decoded to generate the horizontal drive. A signal at twice the horizontal frequency is divided by 525 to generate the vertical drive. The Color Subcarrier is generated by a ÷4 Johnson counter driven directly from the input clock. This is approximately a sinusodial signal. Pulses at the horizontal and vertical frequencies are combined in the composite decoder to generate the outputs Composite Sync, Composite Blanking, and Color Burst Flag.

For use in special applications, the 3262A provides a 30 Hz pulse at the start of the field (Odd Field) and again at the start of the next field (Even Field).

Separate Horizontal and Vertical Reset input pins are provided to allow the 3262A to be used in systems requiring gen-lock operation. Tie Horizontal and Vertical Resets to V_{SS} when they are not used.

The C/BW input is used to select either color or black and white operation. A logic HIGH applied to C/BW will select color operation; if C/BW is LOW, the ÷4 and ÷7 counters will be bypassed for black and white operation. In addition, the only clock needed for black and white operation is Clock 1; Clock 2 should be tied to V_{SS}. The input frequency should be 2.0475 MHz for normal operation.

C/BW when LOW also resets the Color Subcarrier. If the LOW pulse on C/BW is within the specification for t_{RS} — Color Subcarrier Reset Pulse — the color operation for the 3262A will be unaffected.

DC Characteristics V_{SS} = 5.1 V ±0.25 V, V_{GG} = −12 V ± 5%, V_{DD} = 0 V, T_A = 0°C to + 70°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	V_{SS} −0.8		V_{SS} +0.3	V	
V_{IL}	Input LOW Voltage	−5.0		V_{SS} −4.35	V	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −0.1 mA
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 1.6 mA
V_{IHC}	Clock Input HIGH Voltage	V_{SS} −1.0		V_{SS} +0.3	V	
V_{ILC}	Clock Input LOW Voltage	−5.0 V		V_{SS} −4.35	V	
$V_{SUBCARRIER}$	Subcarrier Output Voltage Approximate Sine wave	0.5			$V_{pk\text{-}pk}$	C = 10 pF to V_{DD} R = 10 kΩ to V_{DD}, Note 1
I_{IN}	Input Leakage Current		1.0		μA	V_{IN} = 0 V
I_{DD}	V_{DD} Current		14		mA	
I_{GG}	V_{GG} Current		40		mA	

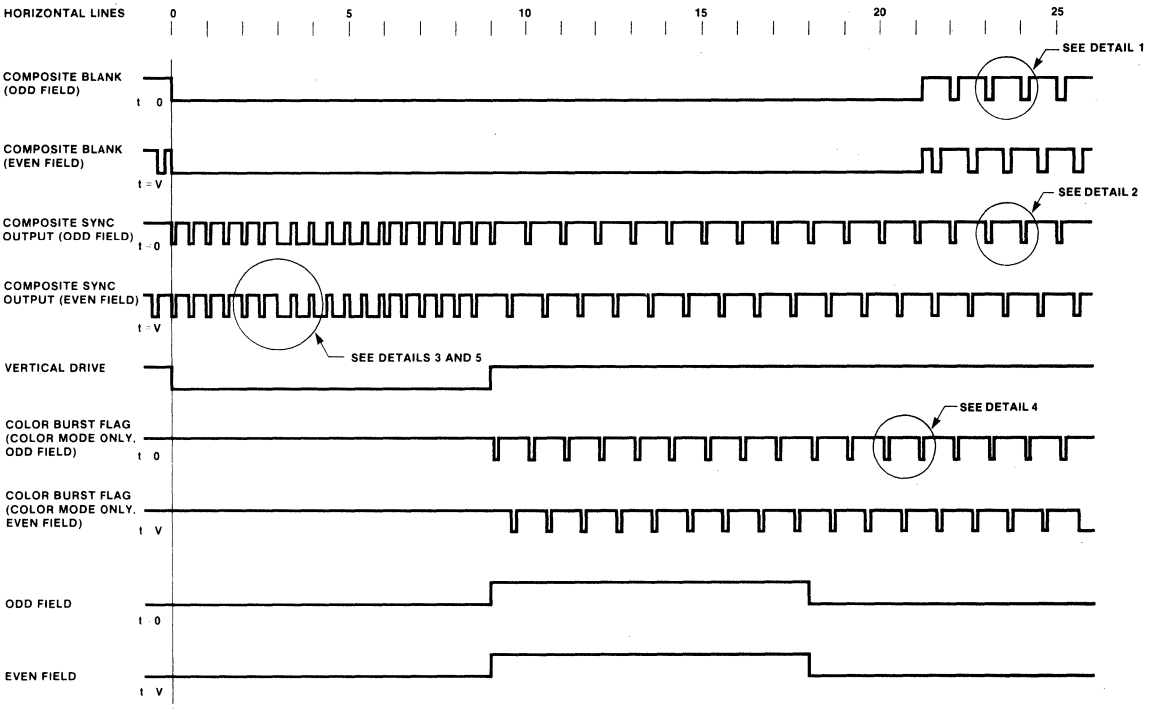
AC Characteristics V_{SS} = 5.1 V ±0.25 V, V_{GG} = −12 V ± 5%, V_{DD} = 0 V, C_L = 10 pF, 1 TTL Load (1.6 mA), T_A = 0°C to + 70°C (See Timing Diagrams)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f	Input Frequency Color	13.3	14.31818	15.4	MHz	t_r, $t_f \leq$ 5 ns
f_1	Input Frequency Black/White	1.5	2.0475	2.2	MHz	t_r, $t_f \leq$ 20 ns
t_{PW1}	B/W Clock LOW Time	200	215	230	ns	t_r, $t_f \leq$ 20 ns
$t_{\overline{PW1}}$	B/W Clock HIGH Time	200	215		ns	t_r, $t_f \leq$ 20 ns
t_{PW2}	Color Clock LOW Time	30	35	40	ns	t_r, $t_f \leq$ 5 ns
$t_{\overline{PW2}}$	Color Clock HIGH Time	30	35		ns	t_r, $t_f \leq$ 5 ns
t_{OV}	Color Clock Overlap Time			5	ns	
$t_{HR\ PW}$	Horizontal Reset Pulse Width	200			ns	t_r, $t_f \leq$ 20 ns
$t_{VR\ PW}$	Vertical Reset Pulse Width	200			ns	t_r, $t_f \leq$ 20 ns, Note 2
t_{CSR}	Color Subcarrier Reset Pulse Width	130		200	ns	t_r, $t_f \leq$ 20 ns

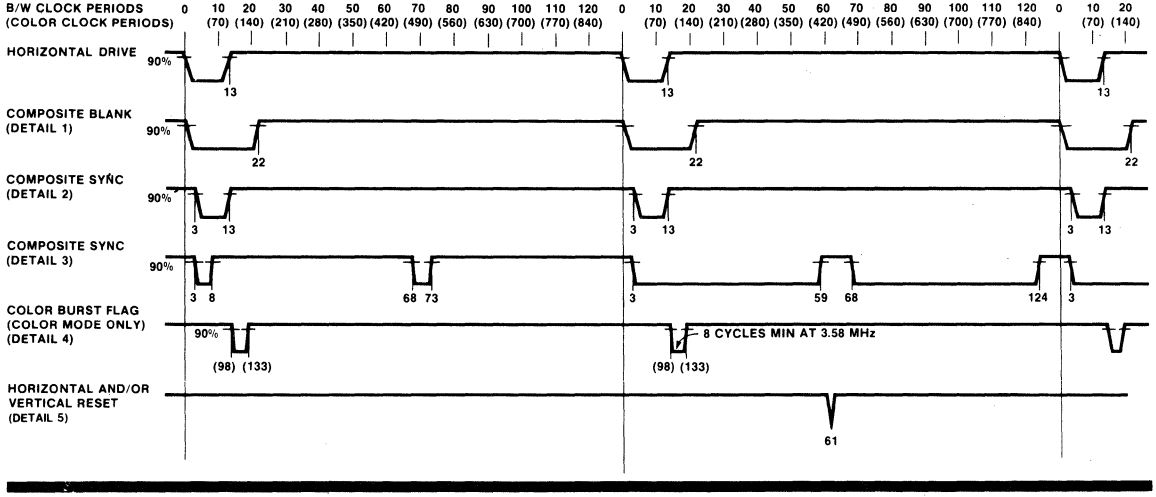
Notes

1. Subcarrier Output should be dc blocked with .01 μF before loading.
2. If t_{HR} occurs simultaneously; if t_{HR} does not occur, t_{VR} = 400 ns min.

RS170EIA Timing Diagram

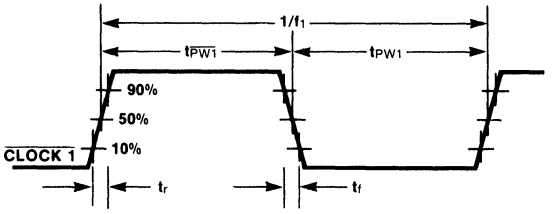


RS170EIA Timing Detail

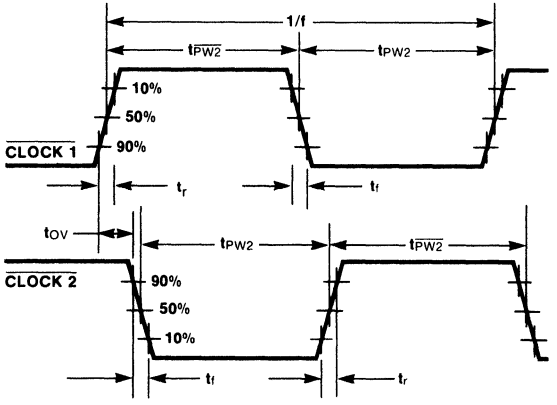


Clock Timing Diagrams

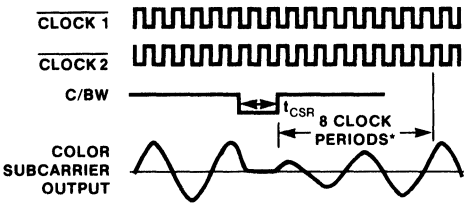
a) Black and White Clock



b) Color Clocks



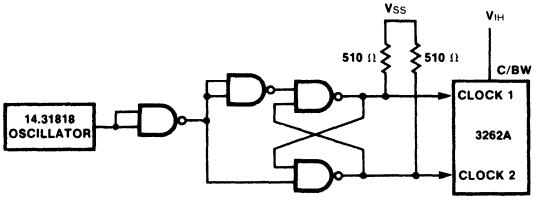
c) Color Subcarrier Timing and Reset Detail



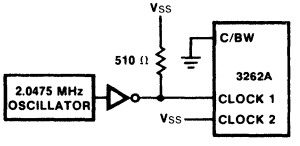
*Maximum subcarrier amplitude attained within 8 color clock periods following rising edge of C/BW.

Clock Generator Circuitry

a) Color Clocks

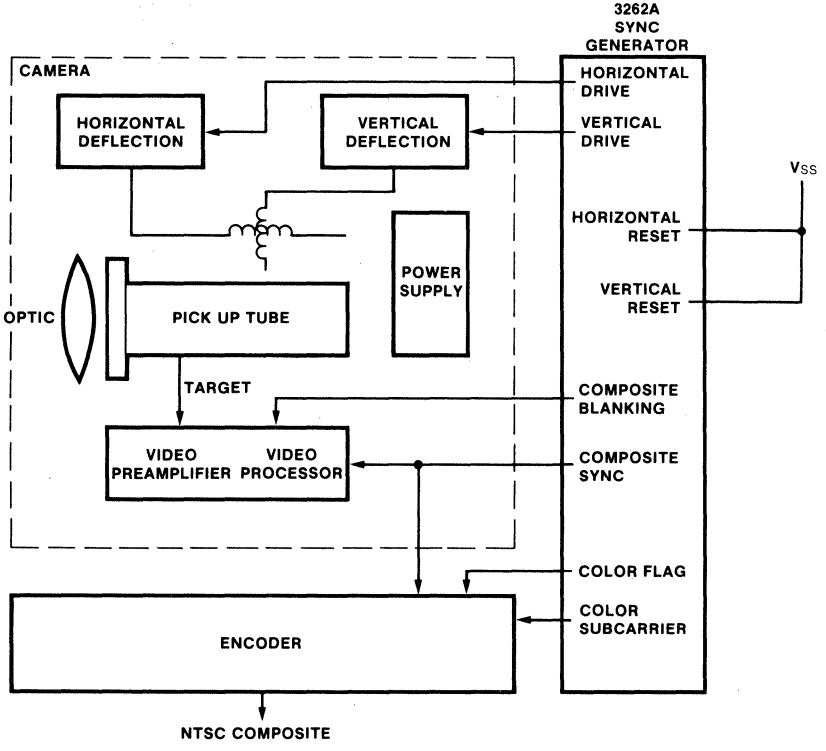


b) Black and White Clock



Applications

TV Camera System



3262B
TV Sync Generator for Generator Lock

MOS Memory Products

Description

The 3262B is a sync pulse generator that produces the necessary outputs for synchronizing television broadcast information. These outputs include Horizontal Drive, Vertical Drive, Composite Sync, Composite Blanking, and Even and Odd Fields, all of which are provided in the format specified by RS170EIA Standard Output Signals. The Color Subcarrier (3.58 MHz) and the Color Burst Flag outputs are provided for color operation. All waveforms are derived from a low-voltage two-phase clock (for color operation) or a single-phase clock (for black and white operation). All outputs except the Color Subcarrier are capable of driving a TTL load directly. The Color Subcarrier is designed to drive a capacitive load. The 3262B is a monolithic integrated circuit manufactured with Isoplanar p-channel silicon gate technology.

- **COLOR OR BLACK WHITE OPERATION**
- **ALL COUNTERS SYNCHRONOUS**
- **PULSE WIDTHS DERIVED DIGITALLY**
- **OUTPUTS DRIVE TTL DIRECTLY (EXCEPT COLOR SUBCARRIER)**
- **IDEAL FOR GENERATOR LOCK OPERATION—SYNCHRONIZES TO COMPOSITE SYNC INPUT**

Applications

- Camera Logic Replacement
- Home TV Games
- Video Tape Recorders
- Video Terminals

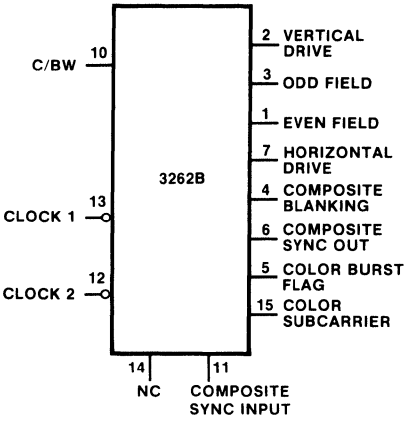
Absolute Maximum Ratings

All Inputs (Note)	−20 V to + 0.3 V
V_{GG}	−20 V to +0.3 V
V_{DD} and Outputs	−6 V to +0.3 V
DC Output Current (output LOW)	<10 mA
Storage Temperature	−55°C to 150°C
Operating Temperature	0°C to 70°C
Maximum Power Dissipation	750 mW

Note
All Voltages with respect to V_{SS}

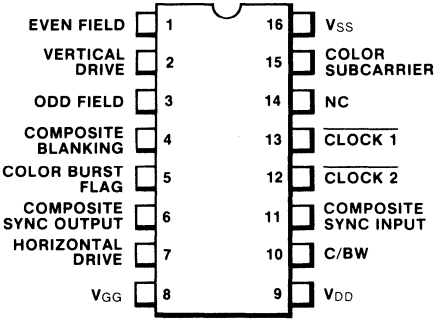
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Diagram



V_{SS} = Pin 16
V_{DD} = Pin 9
V_{GG} = Pin 8

Connection Diagram
16-Pin DIP

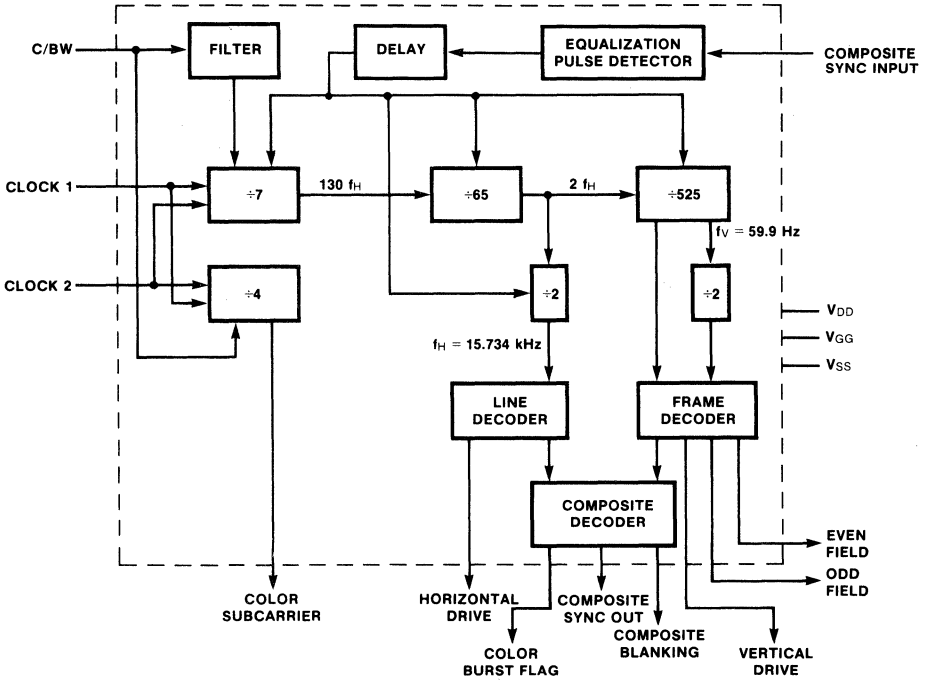


(Top View)

NC = No Connection

Package	Outline	Order Code
Ceramic DIP	6Z	D

Block Diagram



Functional Description

The 3262B block diagram shows the counting and decoding scheme used to generate all output waveforms. The clock frequency is divided down in three steps (÷7, ÷65, ÷2) and decoded to generate the horizontal drive. A signal at twice the horizontal frequency is divided by 525 to generate the vertical drive. The Color Subcarrier is generated by a ÷4 Johnson counter driven directly from the input clock. This is approximately a sinusoidal signal. Pulses at the horizontal and vertical frequencies are combined in the composite decoder to generate the outputs Composite Sync, Composite Blanking, and Color Burst Flag.

For use in special applications, the 3262B provides a 30 Hz pulse at the start of the field (Odd Field) and again at the start of the next field (Even Field).

The Composite Sync input is provided for gen-lock operation. The detection circuit shown in the block diagram detects the first equalizing pulse in the Odd Field and, as a result, generates a reset. This causes the Composite Sync output and Composite Sync input to synchronize such that Composite Sync output occurs before Composite Sync input (see Timing Diagrams). For gen-lock application the input clock must be locked to master generator clock in order to provide stable operation.

The C/BW input is used to select either color or black and white operation. A logic HIGH applied to C/BW will select color operation; if C/BW is LOW, the ÷4 and ÷7 counters will be bypassed for black and white operation. In addition, the only clock needed for black and white operation is Clock 1; Clock 2 should be tied to V_{SS}. The input frequency should be 2.0475 MHz for normal operation.

C/BW when LOW also resets the Color Subcarrier. If the LOW pulse on C/BW is within the specification for t_{RS}—Color Subcarrier Reset Pulse—the color operation for the 3262B will be unaffected.

DC Characteristics V_{SS} = 5.1 V ±0.25 V, V_{GG} = −12 V ± 5%, V_{DD} = 0 V, T_A = 0°C to +70°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	V_{SS} −1.0		V_{SS} −0.3	V	
V_{IL}	Input LOW Voltage	−5.0		V_{SS} −4.35	V	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −0.1 mA
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 1.6 mA
V_{IHC}	Clock Input HIGH Voltage	V_{SS} −1.0		V_{SS} +0.3	V	
V_{ILC}	Clock Input LOW Voltage	−5.0 V		V_{SS} −4.35	V	
$V_{SUBCARRIER}$	Subcarrier Output Voltage Approximate Sine Wave	0.5			V_{pk-pk}	C = 10 pF to V_{DD} R = 10 kΩ to V_{DD} Note 1
I_{IN}	Input Leakage Current		1.0		μA	V_{IN} = 0 V
I_{DD}	V_{DD} Current		14		mA	
I_{GG}	V_{GG} Current		40		mA	

6

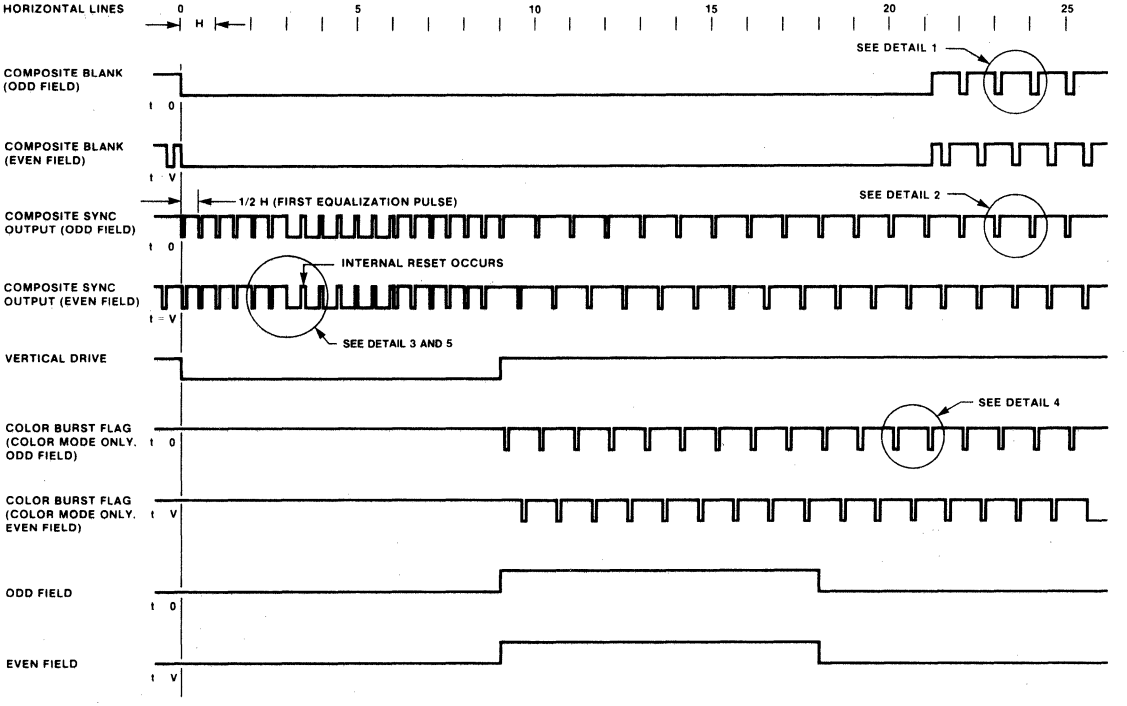
AC Characteristics V_{SS} = 5.1 V ±0.25 V, V_{GG} = −12 V ± 5%, V_{DD} = 0 V, C_L = 10 pF, 1 TTL Load (1.6 mA), T_A = 0°C to +70°C (See Timing Diagrams)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f	Input Frequency Color	13.3	14.31818	15.4	MHz	t_r, $t_f \leq$ 5 ns
f_1	Input Frequency Black/White	1.5	2.0475	2.2	MHz	t_r, $t_f \leq$ 20 ns
t_{PW1}	B/W Clock LOW Time	200	215	230	ns	t_r, $t_f \leq$ 20 ns
$t_{\overline{PW1}}$	B/W Clock HIGH Time	200	215		ns	t_r, $t_f \leq$ 20 ns
t_{PW2}	Color Clock LOW Time	30	35	40	ns	t_r, $t_f \leq$ 5 ns
$t_{\overline{PW2}}$	Color Clock HIGH Time	30	35		ns	t_r, $t_f \leq$ 5 ns
t_{OV}	Color Clock Overlap Time			5	ns	
t_{CA}	Time by which Composite Sync Output precedes Composite Sync Input		2.0		μs	Black/White, Note 2
			500		ns	Color, Note 2
t_s	Synchronization Time for Composite Sync Input			34	ms	Note 3
t_{CSR}	Color Subcarrier Reset Pulse	130		200	ns	t_r, $t_f \leq$ 20 ns

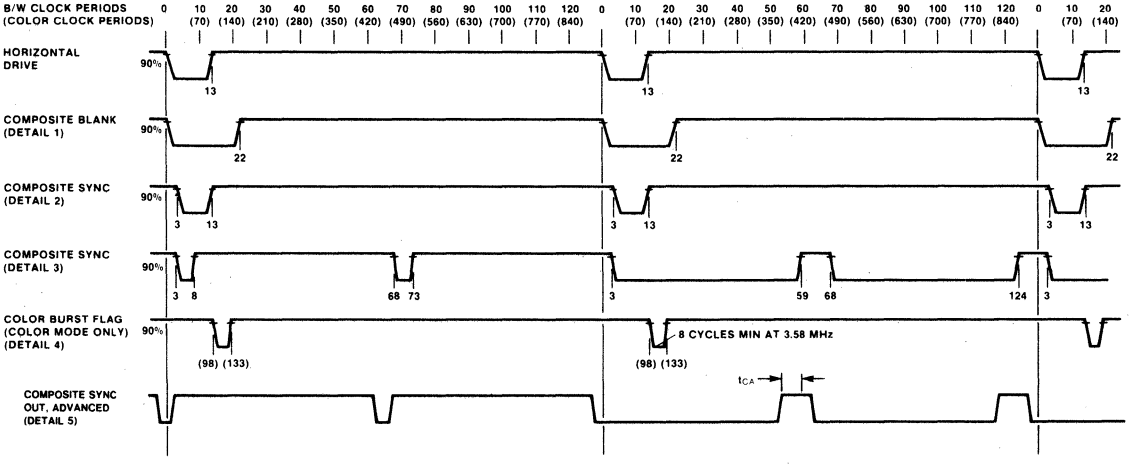
Notes

1. Subcarrier output should be dc blocked with 0.01 μF before loading.
2. t_{CA} is derived digitally from the input clock. t_{CA} = 4 black and white clock periods (7 color clock periods) + skew between Composite Sync Input and negative clock transition + 250 ns propagation delay.
3. One full frame is the maximum. This synchronizes as a result of the region detected in Composite Sync input as shown in RS170EIA Timing Details. The minimum time is the width of the region.

RS170EIA Timing Diagram

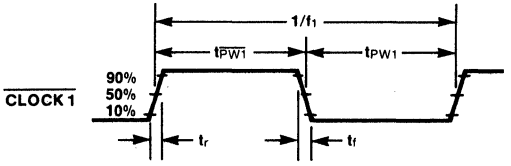


RS170EIA Timing Details

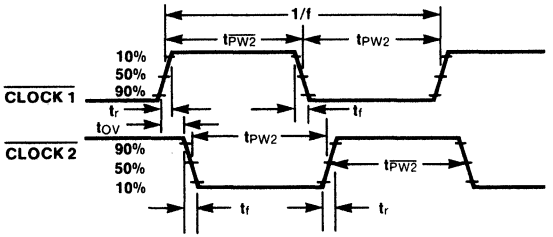


Clock Timing Diagrams

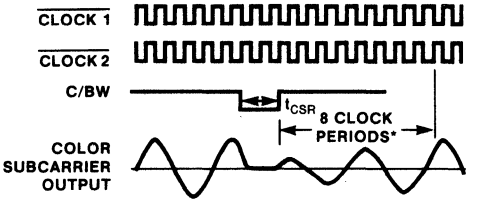
a) Black and White Clock



b) Color Clocks



c) Color Subcarrier Timing and Reset Detail

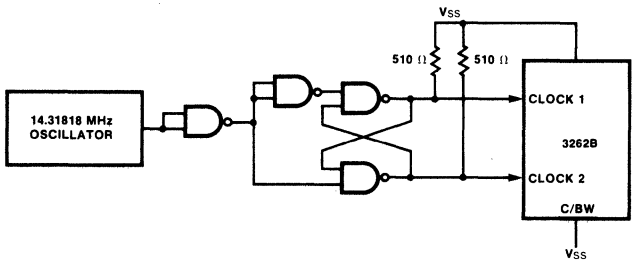


*Maximum subcarrier amplitude attained within 8 color clock periods following rising edge of C/BW.

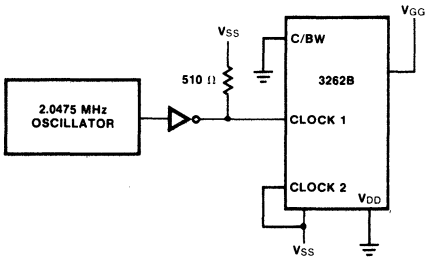
6

Clock Generator Circuitry

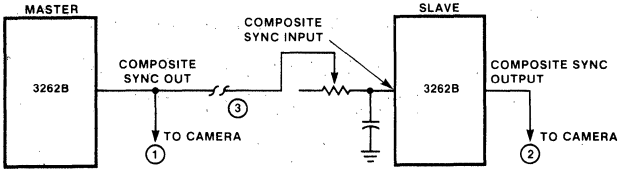
(a) Color Clock

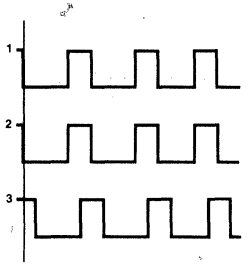


(b) Black and White Clock



Generator-Lock Operation





Note

Due to propagation delay associated with distance, Composite Sync at (3) is delayed from (1). Since Composite Sync Out from the Slave camera is advanced by t_{CA} from (3), the RC network can be adjusted so the (1) and (2) are exactly in sync.

3708
8-Channel Multiplex Switch

MOS Memory Products

Description

The 3708 is an 8-channel multiplex switch with an Output Enable control and 1-of-8 decoder included on-chip. It is manufactured using p-channel enhancement mode silicon gate technology. The logic input lines are npn bipolar compatible and can be used directly with TTL 5.0 V logic levels with no level shifting interface required. This device is intended for use in a/d converters, multiplexing in analog or digital data transmission systems, and other airborne or ground instrumentation signal routing applications.

- **1-of-8 DECODER ON-CHIP**
- **HIGH OFF-RESISTANCE TO ON-RESISTANCE RATIO**
- **OUTPUT ENABLE CONTROL**
- **LOW LEAKAGE CURRENT**
- **ZERO OFFSET VOLTAGE**
- **FAST SWITCHING TIME—1.5 μs (MAX)**
- **TTL COMPATIBLE INPUT LOGIC LEVELS**

Pin Names

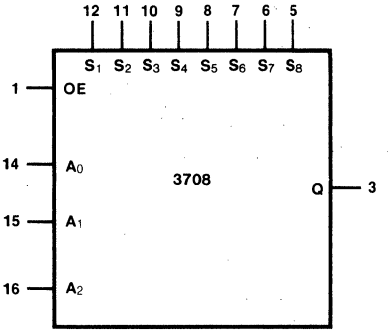
A_0-A_2	Address Inputs
S_1-S_8	Switch Inputs
OE	Output Enable
Q	Data Output

Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Positive Voltage on any Pin	+0.3 V
Negative Voltage on Digital and Analog Input Pins	−30 V
Negative Voltage on Digital and Analog Output Pins	−30 V
Negative Voltage on V_{DD}	−30 V
Total Power Dissipation in Package (T_A = 25°C)	200 mW

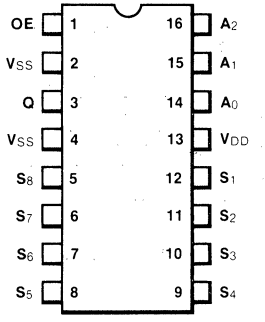
Voltage ratings are all referenced to pins 2 and 4 (V_{SS}). Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress raany other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Symbol



V_{SS} = Pins 2 and 4
V_{DD} = Pin 13

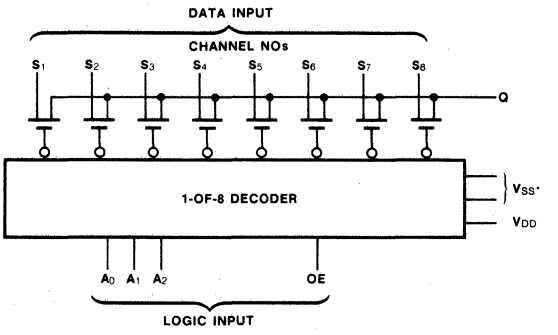
Connection Diagram 16-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	6Z	D

Block Diagram



*Both V_{SS} lines are internally connected; either one or both may be used.

Truth Table

Logic Inputs				Channel
A_0	A_1	A_2	OE	ON
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

DC and AC Characteristics

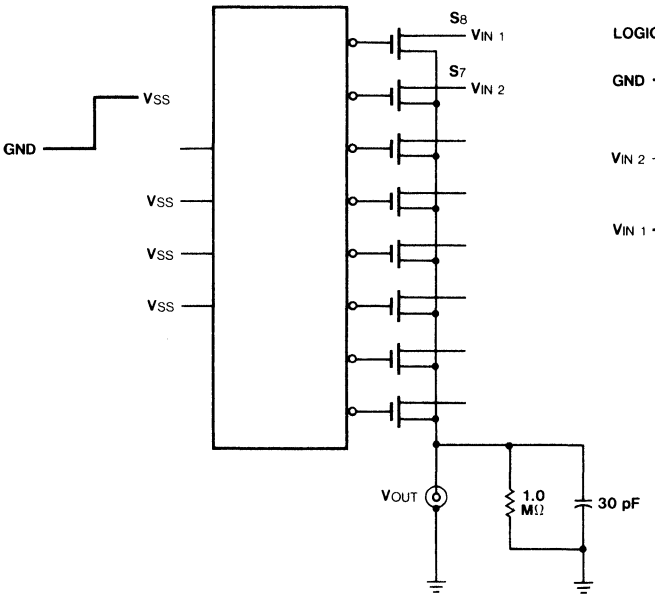
V_{OUT} = −5.0 V to +5.0 V, V_{DD} = −19 V ±1 V, V_{SS} = 5.5 V ± 0.5 V, T_A = 0°C to +70°C

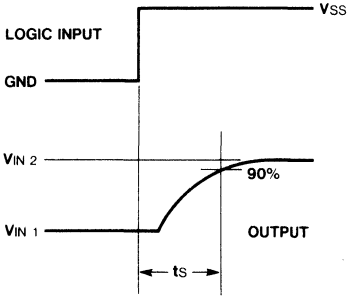
Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	$V_{SS}-1.5$		V_{SS}	V	Note
V_{IL}	Input LOW Voltage	V_{DD}		0.8	V	Note
I_{IN}	Logic Input Leakage Current			10	μA	$V_{SS} - V_{LOGIC\text{-}IN}$ = 15 V
I_{LD}	Data Input Leakage Current			500	nA	$V_{SS} - V_{IN}$ = 15 V
I_{OUT}	Output Leakage Current			500	nA	$V_{SS} - V_{OUT}$ = 15 V
R_{ON}	Data Channel "ON" Resistance			450	Ω	V_{OUT} = −5.0 V, I_{OUT} = −100 μA
P_D	Power Dissipation			175	mW	V_{DD} = −26 V, V_{SS} = 0 V @ 25°C
t_S	Channel Switching Time			1.5	μs	See Test Circuit

Note

When driven by TTL elements, avoid excessive dc loading of TTL elements to insure 3708 logic levels under maximum fanout conditions. Analog input signal swing should not exceed V_{SS} (= V_{CC}).

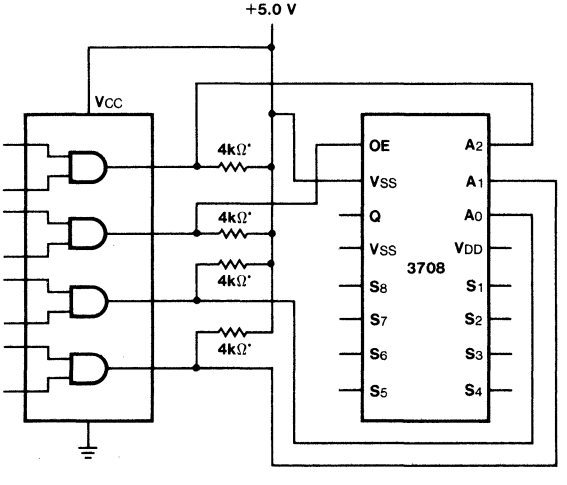
Switching Time Test Circuit





Application

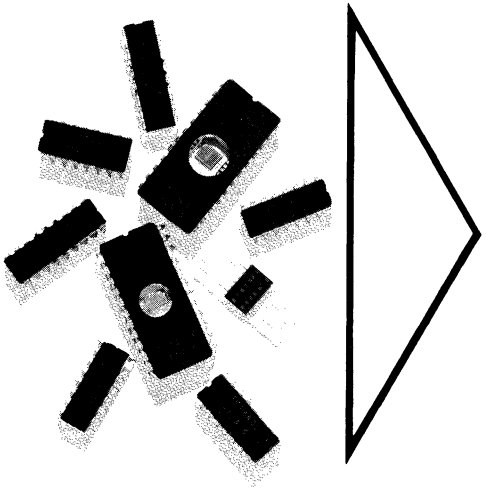
Typical Control Circuit



ANY TTL OR DTL INTEGRATED CIRCUIT

Note

*Optional Components — not needed if TTL fan-out is limited to 1.



Extended Temperature Range Supplement

2102/2102L 1024 x 1 Static RAM

MOS Memory Products

Description

The 2102 family consists of 1024-word by 1-bit static Random Access read/write Memories (RAM) that require a single 5 V supply, have fully TTL-compatible inputs and output, and require no clocking or refresh. Chip Select ($\overline{CS}$) permits a 3-state output allowing the outputs to be wired-OR.

The 2102 and 2102L are manufactured using the n-channel Isoplanar process and are available in a 16-pin dual in-line package or flatpak.

- **FAST ACCESS—250 ns**
- **SINGLE +5 V SUPPLY**
- **TTL-COMPATIBLE INPUTS AND OUTPUT**
- **TOTALLY STATIC—NO CLOCKS OR REFRESH**
- **3-STATE OUTPUT**
- **LOW POWER (2102L)**
- **FULLY EXPANDABLE**
- **FULLY DECODED**
- **16-PIN DUAL IN-LINE PACKAGE**
- **TWO TEMPERATURE RANGES**

Pin Names

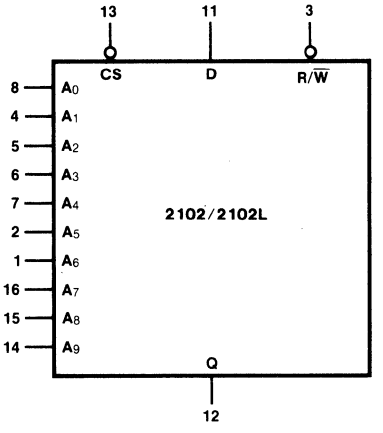
A_0-A_9	Address Inputs
D	Data Input
$R/\overline{W}$	Read/Write
$\overline{CS}$	Chip Select (active LOW)
Q	Data Output

Absolute Maximum Ratings

Any Pin with Respect to V_{SS}	−0.5 V to +7.0 V
Storage Temperature	−55°C to +150°C
Operating Temperature	DL: −55°C to +85°C DM: −55°C to +125°C

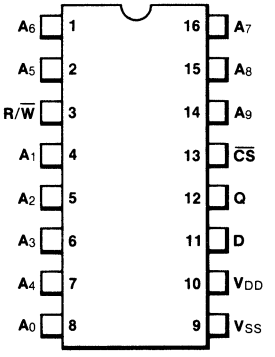
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliabiliy.

Logic Symbol



V_{SS} = Pin 9
V_{DD} = Pin 10

Connection Diagram 16-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	6Z	D
Flatpak	II	F

Note
The Flatpak has the same Pin number to function correspondence as the DIP.

DC Requirements Over full operating temperature range unless otherwise specified

Symbol	Characteristic, Note		2102 DL/DM, 2102L DL/DM C Min	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	H,F,1	2.0	V_{DD}	V	
		2	2.2	V_{DD}		
V_{IL}	Input LOW Voltage	H,F,1	−0.5	0.8	V	
		2	−0.5	0.65		
V_{DD}	Power Supply Voltage		4.5	5.5	V	

DC Characteristics V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, over full operating temperature range unless otherwise specified

Symbol	Characteristic	2102 DL/DM, 2102L DL/DM Min	Max	Unit	Condition
V_{OH}	Output HIGH Voltage	2.2		V	I_{OH} = −100 μA
V_{OL}	Output LOW Voltage		0.45	V	I_{OL} = 2.1 mA
I_{IN}	Input Leakage Current		10		V_{IN} = 5.5 V
I_{OH}	Output HIGH Leakage Current		10	μA	$V_{OUT} = V_{OH(Min)}$ $\overline{CS} = V_{IH(Min)}$
I_{OL}	Output LOW Leakage Current		−50	μA	$V_{OUT} = V_{OL(Max)}$ $\overline{CS} = V_{IH(Min)}$
I_{DD}	Power Supply Current 2102 2102L		60 30	mA	Inputs = 5.5 V D_{OUT} open, T_A = −55°C

AC Requirements Over full operating temperature range unless otherwise specified

Symbol	Characteristic	2102H 2102LH DL/DM Min	2102F 2102LF DL/DM Min	21021 2102L1 DL/DM Min	21022 2102L2 DL/DM Min	Unit	Condition
t_{CYC}	Read or Write Cycle Time	250	350	450	650	ns	
t_{AW}	Address to Write Time	20	20	20	200	ns	
t_{WP}	Write Pulse Width	170	170	200	350	ns	V_{SS} = 0 V
t_{WR}	Write Recovery Time	0	0	0	50	ns	See DC Requirements
t_{DS}	Data Set-up Time	170	170	200	350	ns	for Conditions on V_{DD}
t_{DH}	Data Hold Time	0	0	0	20	ns	
t_{CW}	Chip Select to Write Time	170	170	200	400	ns	
t_{WC}	Write to Chip Select Time	0	0	0	50	ns	

AC Characteristics Over full operating temperature range unless otherwise specified

Symbol	Characteristic	2102H 2102LH DL/DM		2102F 2102LF DL/DM		21021 2102L1 DL/DM		21022 2102L2 DL/DM		Unit	Condition
		Min	Max	Min	Max	Min	Max	Min	Max		
t_A	Read Access Time		250		350		450		650	ns	V_{SS} = 0 V See DC Requirements for Conditions on V_{DD}
t_{CO}	Chip Select to Output Time		130		170		200		400	ns	
t_{OH1}	Data Valid after Address	40		50		50		50		ns	
t_{OH2}	Previous Data Valid after Chip Deselect	0		0		0		0		ns	
C_{IN}	Input Capacitance		5		5		5		5	pF	V_{IN} = 0 V, V_{SS} = 0 V f = 1 MHz, T_A = 25°C
C_{OUT}	Output Capacitance		10		10		10		10	pF	

For block diagram, functional description and timing diagrams refer to standard 2102 data sheet, Section 3.

7

Extended Temperature Range Supplement

F2114/F2114L 1024 x 4 Static RAM

MOS Memory Products

Description

The F2114 is a 4096-bit static Random Access Memory (RAM) organized as 1024 words of four bits each. Since the operation of the F2114 is entirely static, there is no clocking or refreshing required. It operates from a single +5 V supply and is directly a TTL compatible at all inputs and outputs including the four bidirectional data I/O pins.

It is designed for memory applications in which static operation, large bit-capacity, and simple interfacing are important design considerations.

The F2114 is manufactured using Fairchild's n-channel silicon gate Isoplanar process. The innovative use of polysilicon resistors in the static memory cell permits a high bit packing density and insures low-power characteristics. It is available in a standard ceramic 18-pin dual in-line package.

- **1024 x 4-BIT ORGANIZATION**
- **SINGLE +5 V SUPPLY**
- **COMPLETELY STATIC—NO CLOCKS OR REFRESH**
- **TOTALLY TTL COMPATIBLE**
- **COMMON DATA I/O PINS WITH 3-STATE CAPABILITY**
- **IDENTICAL CYCLE AND ACCESS TIMES**
- **LOW POWER (2114L)**

Pin Names

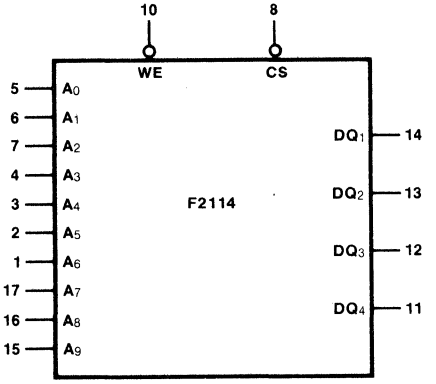
A_0-A_9	Address Inputs
$\overline{CS}$	Chip Select (Active LOW)
$\overline{WE}$	Write Enable (Active LOW)
DQ_1-DQ_4	Data Input/Output
V_{CC}	+5 V Power Supply
GND	Ground

Absolute Maximum Ratings

Voltage at Any Pin with Respect to GND	−0.5 V to +7.0 V
Operating Temperature (Ambient)	−55 to +125°C
Storage Temperature (Ambient)	−55°C to +150°C
Power Dissipation	1 W

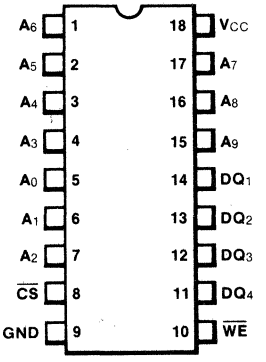
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

Logic Symbol



V_{CC} = Pin 18
GND = Pin 9

Connection Diagram 18-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	8D	D

DC Electrical Requirements and Characteristics $T_A = -55$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$, all voltages are with respect to ground, Note 1

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{OH}	Output HIGH Voltage	2.4		V_{CC}	V	$I_{OUT} = -1.0$ mA
V_{OL}	Output LOW Voltage	0		0.4	V	$I_{OUT} = 2.1$ mA
I_{OS}	Output Short-Circuit Current[2]			65	mA	$V_{OUT} = 0$ V
I_{CC}	Average V_{CC} Supply Current F2114L2, F2114L3, F2114L			70	mA	$V_{CC} = 5.5$ V, $T_A = 0°C$,
	Average V_{CC} Supply Current F2114-2, F2114-3, F2114			100	mA	$V_{IN} = 5.5$ V, I/O current = 0 mA
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = 0$ to 5.5 V
I_{DQ}	I/O Leakage Current	−10		10	μA	$\overline{CS} = 2.0$ V, $V_{I/O} = 0.4$ V to V_{CC}
C_{IN}	Input Capacitance			5.0	pF	$T_A = 25°C$, f = 1.0 MHz $V_{IN} = 0$ V
C_{DQ}	I/O Capacitance			5.0	pF	$T_A = 25°C$, f = 1.0 MHz $V_{I/O} = 0$ V

AC Electrical Requirements and Characteristics $T_A = -55$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$, Notes 1 and 3

		F2114-2/L-2		F2114-3/L-3		F2114/L			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Note
t_{CYC}	Read or Write Cycle Time	200		300		450		ns	
t_{ACC}	Read Access Time		200		300		450	ns	
t_{CO}	$\overline{CS}$ LOW to Output Valid Delay		70		100		100	ns	
t_{CSX}	$\overline{CS}$ LOW to Output Active Delay	20		20		20		ns	
t_{ODH}	Output Data Hold Time after Address	50		50		50		ns	
t_{OFF}	Output OFF Delay from $\overline{CS}$	0	60	0	80	0	100	ns	
t_{AW}	Address to Write Set-up Time	0		0		0		ns	
t_{WP}	$\overline{WE}$ Pulse Width	120		150		200		ns	
t_{WR}	Write Recovery Time	0		0		0		ns	
t_{DS}	Input Data Set-up Time	120		150		200		ns	
t_{DH}	Input Data Hold Time	0		0		0		ns	

Notes

1. Test Note: The F2114 employs a self starting oscillator and a charge pump which require a start-up time of 500 μs after V_{CC} reaches at least 4.75 V.
2. Duration not to exceed 30 seconds.
3. AC Characteristic Test Conditions:

Input Levels	0.8 to 2.0 V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5 V
Output Load	1 TTL Gate, CL = 100 pF

For block diagram, functional description and timing diagrams refer to standard 2114 data sheet, Section 3.

Extended Temperature Range Supplement

3341/3341A 64 x 4 FIFO Serial Memory

MOS Memory Products

Description

The 3341 or 3341A is a 64-word x 4-bit First-In First-Out (FIFO) serial memory. Inputs and the outputs are completely independent (no common clocks) making the 3341/3341A ideal for asynchronous buffer applications.

Special on-chip input pull-up circuits and bipolar-compatible output buffers provide direct bipolar interfacing with no external components required. Control signals are provided for both vertical and horizontal cascading.

The 3341 and 3341A are manufactured using the p-channel Isoplanar silicon gate process and are available in both ceramic and plastic packages.

- **1 MHz (3341A) AND 700 kHz (3341) DATA RATES**
- **INDEPENDENT ASYNCHRONOUS INPUTS AND OUTPUTS**
- **FULLY TTL COMPATIBLE**
- **EXPANDABLE IN EITHER DIRECTION**
- **ACTIVE PULL-UP ON INPUTS**
- **TWO TEMPERATURE RANGES**
- **16-PIN DUAL IN-LINE PACKAGE**

Pin Names

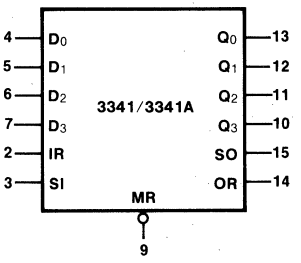
IR	Input Ready
SI	Shift In
D_0-D_3	Data Inputs
$\overline{MR}$	Master Reset
OR	Output Ready
SO	Shift Out
Q_0-Q_3	Data Outputs
V_{SS}	+5 V Power Supply
V_{DD}	0 V Power Supply
V_{GG}	−12 V Power Supply

Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Operating Temperature	DL: −55°C to +85°C DM: −55°C to +125°C
Voltage on All Pins Except V_{DD} with Respect to V_{SS}	−20 V to +0.3 V
Voltage on V_{DD}	−7.0 V to +0.3 V

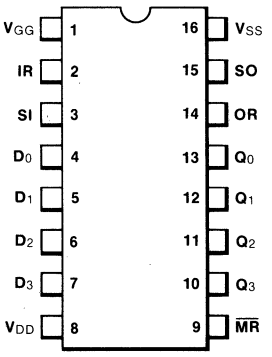
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Symbol



V_{SS} = Pin 16
V_{DD} = Pin 8
V_{GG} = Pin 1

Connection Diagram 16-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	6Z	D

DC Characteristics V_{SS} = +5 V ± 5%, V_{GG} = −12 V ± 5%, V_{DD} = 0 V
over full operating temperature range unless otherwise indicated

Symbol	Characteristic	F3341DL/DM, 3341ADL/DM Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	V_{SS} −1.0			V	Notes 1 and 2
V_{IL}	Input LOW Voltage			0.8	V	Note 1
V_{OH}	Output HIGH Voltage	V_{SS} − 1.0			V	I_{OH} = −0.3 mA
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 1.6 mA
V_{II}	Input Pull-up Initiation Voltage			2.0	V	V_{SS} = 4.75 V
				2.2	V	V_{SS} = 5.25 V
V_{IP}	Peak Input Current Voltage Point			V_{SS} − 1.5	V	
I_{IH}	Input HIGH Current	−200			μA	Note 1, V_{IN} = V_{SS} − 1.0 V
I_{IL}	Input Leakage Current			−50	μA	Note 1, V_{IN} = 0 V
I_{IP}	Input Barrier Current			−2.0	mA	Note 1
I_{GG}	V_{GG} Current			−16	mA	
I_{DD}	V_{DD} Current			−60	mA	

Notes

1. Inputs include D_0-D_3. Master Reset, Shift In, and Shift Out.
2. Internal pull-up circuits are provided on all inputs to insure proper HIGH level.
3. Control signals include Input Ready, Shift In, Output Ready, and Shift Out.
4. This parameter defines total time from the time data is loaded into the first word location to the time it is available at Q_0-Q_3 with the FIFO initially empty. Conversely, t_{BT} also defines the time required for an empty space to propagate from the last word location back to the first word location. When the FIFO is full, this is the time from the HIGH-to-LOW transition of OR to the LOW-to-HIGH transition of IR.
5. 1 TTL load +20 pF.
6. The $\overline{MR}$ input overrides all other control functions. It resets the control register and the input and output control logic while disabling any SI or SO inputs.
7. t_{IRH} is referenced to the positive going edge of IR or SI, whichever occurs later.
8. t_{IRL} is referenced to the negative going edge of IR or SI, whichever occurs later.
9. t_{DD} is referenced to the positive going edge of IR or SI, whichever occurs later.
10. t_{OVH} is referenced to the positive going edge of IR or SI, whichever occurs later.
11. t_{OVL} is referenced to the negative going edge of IR or SI whichever occurs later.
12. Data must be stable for t_{DH} or t_{IRH}, whichever is shorter.
13. t_{ORH} is referenced to the positive going edge of OR or SO, whichever occurs later.
14. t_{ORL} is referenced to the negative going edge of OR or SO, whichever occurs later.
15. t_{DV} is referenced to the negative going edge of OR or SO, whichever occurs later.
16. t_{OVH} is referenced to the positive going edge of IR or SI, whichever occurs later.
17. t_{OVL} is referenced to the negative going edge of IR or SI, whichever occurs later.

AC Characteristics V_{CC} = +5 V ± 5%, V_{DD} = 0 V, V_{GG} = −12 V ± 5%
over full operating temperature range unless otherwise indicated

		3341A DL/DM			3341 DL/DM				
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Condition**
t_{IRH}	Input Ready HIGH Time	80		400	100	300	550	ns	Notes 7, 12
t_{IRL}	Input Ready LOW Time	100		550	138	300	550	ns	Note 8
t_{OVH}	Control Overlap HIGH Time	80			100			ns	Notes 3, 16
t_{OVL}	Control Overlap LOW Time	80			100			ns	Notes 3, 17
t_{DH}	Data Input Stable Time	200			400			ns	
t_{DD}	Data Input Delay Time			0			25	ns	Note 9
t_{ORH}	Output Ready HIGH Time	80		450	100	300	500	ns	Note 13
t_{ORL}	Output Ready LOW Time	80		550	170	450	850	ns	Note 14
t_{BT}	Data Bubble-through Time			16			32	μs	Note 4
t_{DV}	Data Valid After SO or OR	75			75			ns	Note 15
t_{MRW}	Master Reset Pulse Width	400			400			ns	Note 6
t_{DA}	Data Output Available Time	0			0			ns	
C_{IN}	Input Capacitance of Data and Control Lines			7.0			7.0	pF	f = 1 MHz, V_{IN} = V_{SS}
C_{MR}	Input Capacitance of $\overline{MR}$			7.0			15	pF	f = 1 MHz, V_{MR} = V_{SS}
f	Operating Frequency			1000			700	kHz	Note 5

Notes on previous page

For block diagram, functional description, timing diagrams and applications refer to standard 3341/3341A data sheet, Section 5.

Extended Temperature Range Supplement

3351 40 x 9 FIFO Memory

MOS Memory Products

Description

The 3351 is a First-In First-Out (FIFO) memory used in data rate buffering applications. The 3351 has a capacity of 40 9-bit words. The words are accepted at the input, automatically shifted towards the output, and removed at any rate in the same sequence in which they were entered.

The 3351 has status indicators on both the input and output to signal an available empty input or a valid data word at the output. It also has separate input and output enable lines, in addition to a master reset line. A unique input stage interfaces to TTL without external components. The 3351 is manufactured using the p-channel Isoplanar silicon gate process with ion-implantation.

- **2 MHz (3351-1), 1.5 MHz (3351-3), AND 1 MHz (3351-2) DATA RATES**
- **INDEPENDENT ASYNCHRONOUS INPUTS AND OUTPUTS**
- **FULLY TTL COMPATIBLE**
- **3-STATE OUTPUTS**
- **INPUT AND OUTPUT ENABLE CONTROLS**
- **EXPANDABLE IN EITHER DIRECTION**
- **STATUS INDICATORS ON INPUT AND OUTPUT**
- **28-PIN CERAMIC DUAL IN-LINE PACKAGE**
- **TWO TEMPERATURE RANGES**

Pin Names

D_0-D_8	Data Inputs
$\overline{MR}$	Master Reset
$\overline{IE}$	Input Enable
IR	Input Ready
SI	Shift In
$\overline{SO}$	Shift Out
$\overline{OE}$	Output Enable
OR	Output Ready
Q_0-Q_8	Data Outputs

Absolute Maximum Ratings

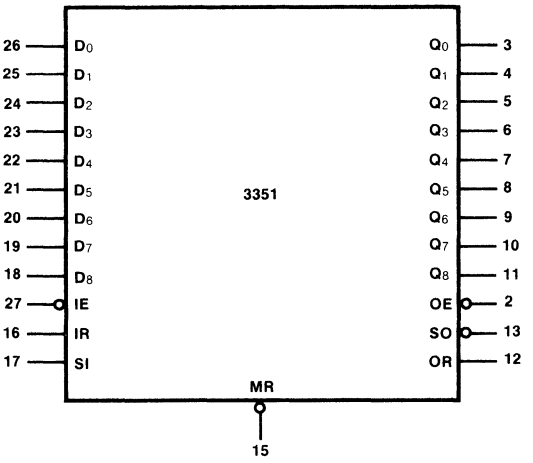
V_{GG} and Inputs	−20 V to +0.3 V
V_{DD} and Outputs	−7.0 V to +0.3 V
Output Sink Current	5.0 mA
Storage Temperature	−55°C to +150°C
Operating Temperature	DL: −55°C to +85°C
	DM: −55°C to +125°C

Note

All Voltages with respect to V_{SS}.

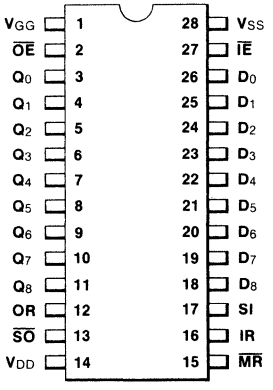
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Symbol



V_{SS} = Pin 28
V_{DD} = Pin 14
V_{GG} = Pin 1

Connection Diagram 28-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	8E	D

DC Requirements V_{SS} = 5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, over full operating temperature range unless otherwise specified.

Symbol	Characteristic	3351-1DL/DM		3351-2DL/DM		3351-3DL/DM		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH}	Input HIGH Voltage	$V_{SS}-1.0$	$V_{SS}+0.3$	$V_{SS}-1.0$	$V_{SS}+0.3$	$V_{SS}-1.0$	$V_{SS}+0.3$	V	Note
V_{IL}	Input LOW Voltage	V_{GG}	0.8	V_{GG}	0.8	V_{GG}	0.8	V	Note

DC Characteristics V_{SS} = 5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%

Symbol	Characteristic	3351-1DL/DM		3351-2DL/DM		3351-3DL/DM		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{OH1}	Output HIGH Voltage	$V_{SS}-0.5$		$V_{SS}-0.5$		$V_{SS}-0.5$		V	I_{OH} = 50 μA
V_{OH2}	Output HIGH Voltage	2.4		2.4		2.4		V	I_{OH} = −0.2 mA
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	V	I_{OL} = 1.6 mA
V_{II}	Pull-up Initiation Voltage		2.2		2.2		2.2	V	Note I_{IN} = −0.12 mA
V_{IP}	Peak Current Voltage		$V_{SS}-1.5$		$V_{SS}-1.5$		$V_{SS}-1.5$	V	Note
I_{IP}	Peak Current		−2.0		−2.0		−2.0	mA	Note
I_{IH}	Input HIGH Current	−0.22		−0.22		−0.22		mA	Note $V_{IN} = V_{SS} - 1.0$ V
I_{IL}	Input LOW Current		−70		−70		−70	μA	Note V_{IN} = 0.4 V
I_{DD}	V_{DD} Current		65		50		50	mA	
I_{GG}	V_{GG} Current		−12		−10		−10	mA	

Note
Includes all Data inputs, $\overline{IE}$, $\overline{OE}$, SI, $\overline{SO}$ and $\overline{MR}$. (See Active Pull-up description.)

AC Requirements V_{SS} = 5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, over full operating temperature range unless otherwise specified.

Symbol	Characteristic	3351-1DL/DM		3351-2DL/DM		3351-3DL/DM		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{IDS}	$\overline{IE}$ Disable Set-Up Time	20		20		20		ns	
t_{IDH}	$\overline{IE}$ Disable Hold Time	20		20		20		ns	
t_{IES}	$\overline{IE}$ Enable Set-Up Time	0		0		0		ns	
t_{IEH}	$\overline{IE}$ Enable Hold Time	0		0		0		ns	
t_{DS}	Input Data Set-Up Time	0		0		0		ns	
t_{DH}	Input Data Hold Time	220		440		300		ns	
t_{SIH}	SI HIGH Time	220		440		300		ns	
t_{SIL}	SI LOW Time	280		560		370		ns	
t_{ODS}	$\overline{OE}$ Disable Set-Up Time	20		20		20		ns	
t_{ODH}	$\overline{OE}$ Disable Hold Time	20		20		20		ns	
t_{OES}	$\overline{OE}$ Enable Set-Up Time	0		0		0		ns	
t_{OEH}	$\overline{OE}$ Enable Hold Time	0		0		0		ns	
t_{SOL}	$\overline{SO}$ LOW Time	200		400		260		ns	
t_{SOH}	$\overline{SO}$ HIGH Time	300		600		450		ns	
t_{RPW}	$\overline{MR}$ Pulse Width	100		200		150		ns	
t_{RS}	$\overline{MR}$ to SI Set-Up Time	0		0		0		ns	

Notes

1. All input t_r and t_f: 10 ns.
2. All time measurements referenced to 50% level.

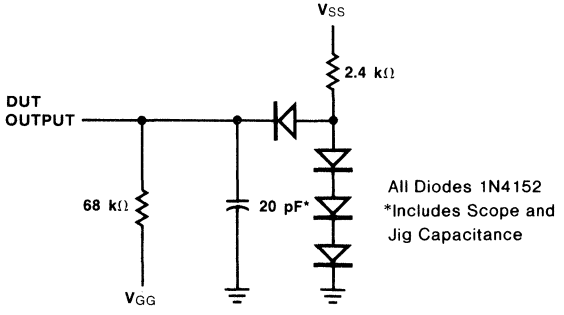
AC Characteristics V_{SS} = 5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, over full operating temperature range unless otherwise specified. See Notes 3, 4 and Output Loading

Symbol	Characteristic	3351-1DL/DM		3351-2DL/DM		3351-3DL/DM		Unit	Condition
		Min	Max	Min	Max	Min	Max		
$t_{SI\text{-}IRHL}$	SI to IR Delay Time		220		440		300	ns	Note 1
$t_{SI\text{-}IRLH}$	SI to IR Delay Time		280		560		370	ns	
$t_{SO\text{-}ORLL}$	$\overline{SO}$ to OR Delay Time		200		400		300	ns	Note 1
$t_{SO\text{-}ORHH}$	$\overline{SO}$ to OR Delay Time		300		600		410	ns	
$t_{MR\text{-}IR}$	$\overline{MR}$ to IR Delay Time		300		480		480	ns	
$t_{MR\text{-}OR}$	$\overline{MR}$ to OR Delay Time		240		480		480	ns	
t_{BT}	Bubble-Through Time		9.0		15		15	μs	Note 2
t_E	Output Enable Time		300		600		480	ns	
t_D	Output Disable Time		300		600		480	ns	
f	Operating Frequency		2.0		1.0		1.5	MHz	

Notes

1. HL means positive-going edge of first signal to negative-going edge of second signal, etc.
2. Forward and reverse.
3. All input t_r and t_f: 10 ns.
4. All time measurements referenced to 50% level.

Output Loading



For block diagram, functional description, timing diagrams and applications information refer to standard 3351 data sheet, Section 5.

Extended Temperature Range Supplement

3357/F2847 Quad 80-Bit Static Shift Register

MOS Memory Products

Description

The 3357 and F2847 are single phase quad 80-bit static shift registers. Both have an on-chip clock generator that is driven by a single phase TTL clock. A multiplexer is provided to allow data to be entered from the input or recirculated from the output. A unique on-chip input pull-up circuit allows interfacing directly from TTL to all inputs without external components.

The 3357 and F2847 are manufactured with the p-channel Isoplanar process and are available in 16-pin ceramic or plastic dual in-line packages in two temperature ranges.

- **4.0 MHz (3357), 2.5 MHz (F2847)**
- **TTL COMPATIBILITY**
- **SINGLE PHASE TTL CLOCK**
- **LOW CLOCK CAPACITANCE**
- **INPUT MULTIPLEXER**
- **16-PIN CERAMIC DUAL IN-LINE PACKAGE**
- **LOW POWER VERSION (F2847L)**
- **TWO TEMPERATURE RANGES**

Pin Names

D_1-D_4	Data Inputs
REC_1-REC_4	Recirculate Inputs
CP	Clock Input
Q_1-Q_4	Data Outputs

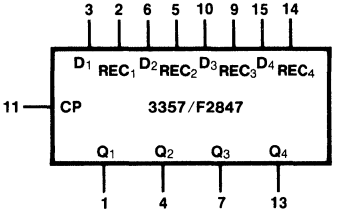
Absolute Maximum Ratings

V_{GG} and Inputs	−20 V to +0.3 V
V_{DD} and Outputs	−7.0 V to +0.3 V
Output Sink Current	10 mA
Storage Temperature	−55°C to +150°C
Operating Temperature	DL: −55°C to +85°C DM: −55°C to +125°C

All voltages with respect to V_{SS}.

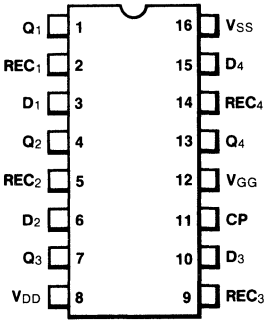
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Symbol



V_{SS} = Pin 16
V_{DD} = Pin 8
V_{GG} = Pin 12

Connection Diagram 16-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	6Z	D

7

DC Requirements V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, over full operating temperature range unless otherwise indicated

Symbol	Characteristic	3357 DL/DM, F2847 DL/DM Min	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	V_{SS} − 1	V_{SS} + 0.3	V	Note 1
V_{IL}	Input LOW Voltage	V_{GG}	+0.8	V	Note 1

DC Characteristics V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, over full operating temeprature range unless otherwise indicated

Symbol	Characteristic		Min	Max	Unit	Condition
V_{OH}	Output HIGH Voltage		V_{SS} − 1		V	I_{OH} = −0.1 mA
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 1.6 mA
V_{II}	Input Pull-up Initiation Voltage			2.2	V	Note 1, $I_{IN} < -0.12$ mA
V_{IP}	Input Peak Current Voltage			V_{SS} − 1.5	V	Note 1
I_{IP}	Input Peak Current			−2.0	mA	Note 1
I_{IH}	Input HIGH Current		−0.22		mA	Note 1, $V_{IN} = V_{SS} - 1.0$ V
I_{IL}	Input LOW Current			−50	μA	Note 1, V_{IN} = 0.4 V
I_{DD}	V_{DD} Current	3357 DL/DM		−25	mA	Max Operating Frequency
		F2847L DL/DM		−25	mA	
		F2847 DL/DM		−45	mA	
I_{GG}	V_{GG} Current	3357 DL/DM		−18	mA	
		F2847L DL/DM		−15	mA	
		F2847 DL/DM		−20	mA	

AC Requirements V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, over full operating temperature range unless otherwise indicated

Symbol	Characteristic	3357 DL/DM Min	3357 DL/DM Max	F2847 DL/DM, F2847L DL/DM Min	F2847 DL/DM, F2847L DL/DM Max	Unit	Condition
f	Operating Frequency	0	4.0	0	2.5	MHz	
t_{PWH}	Clock Pulse Width HIGH	0.095	100	0.15	10	μs	See Timing Diagram, Note 2
t_{PWL}	Clock Pulse Width LOW	0.135		0.18		μs	
t_{DS}	Data Set-up Time	40		120		ns	
t_{DH}	Data Hold Time	30		60		ns	
t_{SS}	Select Set-up Time	40		70		ns	
t_{SH}	Select Hold Time	40		40		ns	

Notes

1. Applies to all inputs including Clock.
2. t_r, t_f = Clock Transition Time = 0.5 μs.

AC Characteristics V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, over full operating temperature range unless otherwise indicated.

Symbol	Parameter		Min	Max	Unit	Condition
C_{IN}	Input Capacitance			5.0	pF	All Inputs
C_{OUT}	Output Capacitance			5.0	pF	
t_{ACC}	Clock to Output Delay Time	3357 DL/DM		185	ns	See Timing Diagram
		F2847L DL/DM		280		
		F2847 DL/DM		280		

For block diagram, functional description and timing diagram refer to standard 3357/F2847 data sheet, Section 5.

Extended Temperature Range Supplement

3708 8-Channel Multiplex Switch

MOS Memory Products

Description

The 3708 is an 8-channel multiplex switch with an Output Enable control and 1-of-8 decoder included on-chip. It is manufactured using p-channel enhancement mode silicon gate technology. The logic input lines are npn bipolar compatible and can be used directly with TTL 5.0 V logic levels with no level shifting interface required. This device is intended for use in a/d converters, multiplexing in analog or digital data transmission systems, and other airborne or ground instrumentation signal routing applications.

- **1-of-8 DECODER ON CHIP**
- **HIGH OFF-RESISTANCE TO ON-RESISTANCE RATIO**
- **OUTPUT ENABLE CONTROL**
- **LOW LEAKAGE CURRENT**
- **ZERO OFFSET VOLTAGE**
- **FAST SWITCHING TIME—1.5 μs (MAX)**
- **TTL COMPATIBLE INPUT LOGIC LEVELS**
- **TWO TEMPERATURE RANGES**

Pin Names

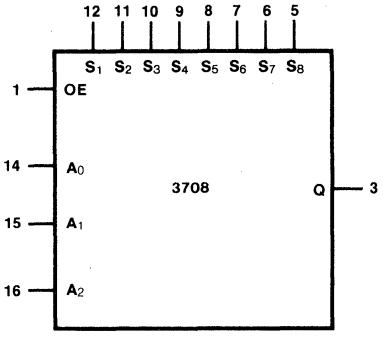
A_0-A_2	Address Inputs
S_1-S_8	Switch Inputs
OE	Output Enable
Q	Data Output

Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Operating Temperature	DL: −55°C to +85°C DM: −55°C to +125°C
Positive Voltage on any Pin	+0.3 V
Negative Voltage on Digital and Analog Input Pins	−30 V
Negative Voltage on Digital and Analog Output Pins	−30 V
Negative Voltage on V_{DD}	−30 V

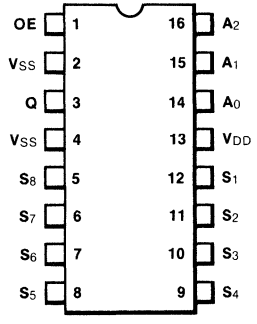
Voltage ratings are all referenced to pins 2 and 4 (V_{SS}). Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Symbol



V_{SS} = Pins 2 and 4
V_{DD} = Pin 13

Connection Diagram 16-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	6Z	D

DC and AC Characteristics V_{OUT} = −5.0 V to +5.0 V, V_{DD} = −19 V ± 1 V, V_{SS} = 5.5 V ± 0.5 V, over full operating temperature range unless otherwise indicated

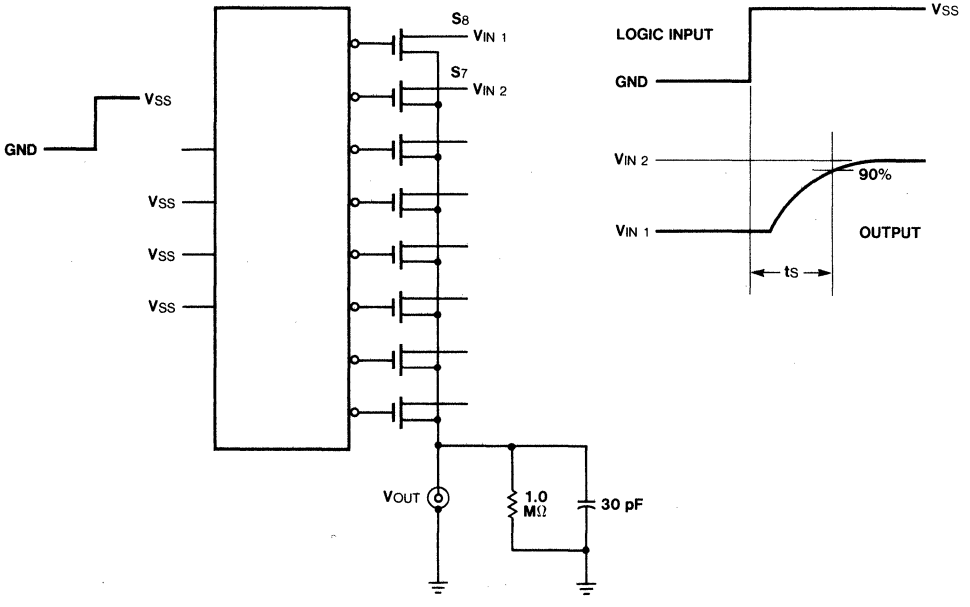
		3708DL/DM				
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**	**Condition**
V_{IH}	Input HIGH Voltage	V_{SS}−1.5		V_{SS}	V	Note
V_{IL}	Input LOW Voltage	V_{DD}		0.8	V	Note
I_{IN}	Logic Input Leakage Current			10	μA	$V_{SS} - V_{LOGIC\text{-}IN}$ = 15 V
I_{LD}	Data Input Leakage Current			500	nA	$V_{SS} - V_{IN}$ = 15 V
I_{OUT}	Output Leakage Current			500	nA	$V_{SS} - V_{OUT}$ = 15 V
R_{ON}	Data Channel "ON" Resistance			450	Ω	V_{OUT} = −5.0 V, I_{OUT} = −100 μA
P_D	Power Dissipation			200	mW	V_{DD} = −26 V, V_{SS} = 0 V @ 25°C
t_S	Channel Switching Time			1.5	μs	See Test Circuit

Note

When driven by TTL elements, avoid excessive dc loading of TTL elements to insure 3708 logic levels under maximum fanout conditions. Analog input signal swing should not exceed V_{SS} (= V_{CC}).

7

Switching Time Test Circuit



For block diagram, truth table and application refer to standard 3708 data sheet, Section 6.

Extended Temperature Range Supplement

F4116 • F4116/240 16,384 x 1 Dynamic RAM

MOS Memory Products

Description

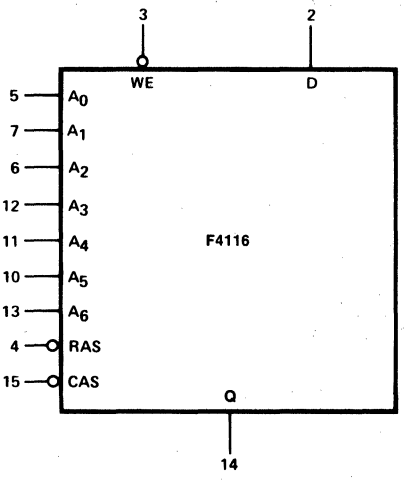
The F4116 and F4116/240 are 16,384-bit MOS dynamic Random Access Memories (RAM) configured as 16,384 one-bit words. They are manufactured using Fairchild's n-channel silicon gate, double-poly Isoplanar process. The use of the single-transistor memory cell along with address multiplexing techniques permits the packaging of the F4116 in a standard 16-pin dual in-line package. This package allows construction of highly dense memory systems utilizing widely available automated testing and insertion equipment.

- **TWO TEMPERATURE RANGES**
- **LOW CAPACITANCE, TTL-COMPATIBLE INPUTS (INCLUDING CLOCKS)**
- **ON-CHIP ADDRESS AND INPUT DATA LATCHES**
- **3-STATE TTL-COMPATIBLE OUTPUT WITH DATA VALID TIME CONTROLLED BY $\overline{CAS}$**
- **COMMON I/O CAPABILITY**
- **TWO DIMENSIONAL SELECTION BY DECODING BOTH $\overline{RAS}$ AND $\overline{CAS}$**
- **STANDARD 10% SUPPLIES (+12 V, +5 V, AND −5 V)**
- **FLEXIBLE TIMING WITH PAGE-MODE AND EXTENDED PAGE BOUNDARIES**
- **128-CYCLE $\overline{RAS}$-ONLY REFRESH**
- **AVAILABLE IN 16-PIN CERAMIC DIP AND FLATPAK**

Pin Names

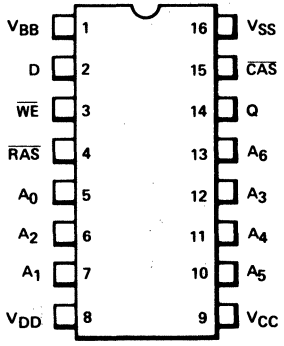
A_0-A_6	Address Inputs
$\overline{D}$	Data Input
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{RAS}$	Row Address Strobe Input (Active LOW Clock)
$\overline{CAS}$	Column Address Strobe Input (Active LOW Clock)
Q	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	0 V Power Supply
V_{BB}	−5 V Power Supply
V_{DD}	+12 V Power Supply

Logic Symbol



V_{SS} = Pin 16
V_{CC} = Pin 9
V_{DD} = Pin 8
V_{BB} = Pin 1

Connection Diagram 16-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	2C	D
Flatpak	2R	F

Absolute Maximum Ratings

Voltage on Any Pin Relative to V_{BB} ($V_{SS} - V_{BB} \geq 4.5$ V)	−0.5 V to +20 V
Ambient Operating Temperature F4116	−55°C to +85°C
Case Operating Temperature F4116/240	−55°C to +110°C
Storage Temperature (Ambient)	−65°C to +150°C
Power Dissipation	1 W
$V_{BB} - V_{SS}$ ($V_{DD} - V_{SS} > 0$ V)	0 V
Voltage on V_{DD}, V_{CC} Supplies Relative to V_{SS}	−1.0 V to +15 V
Short-circuit Output Current	50 mA

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7

DC Requirements (F4116) $T_A = -55°C$ to +85°C, Notes 1 and 2

Symbol	Characteristic	F4116-2, -3, -4 Min	Typ	Max	Unit	Condition
V_{DD}	Supply Voltage	10.8	12	13.2	V	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	Note 5
V_{SS}	Supply Voltage	0	0	0	V	
V_{BB}	Supply Voltage	−5.5	−5.0	−4.5	V	
V_{IHC}	Input HIGH Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	2.7		7.0	V	
V_{IH}	Input HIGH Voltage, All Inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	2.4		7.0	V	
V_{IL}	Input LOW Voltage, All Inputs	−1.0		0.8	V	

Notes on final page.

DC Characteristics (F4116) Over full range of voltage and T_A = −55°C to +85°C

Symbol	Characteristic		F4116-2, -3, -4 Min	Typ	Max	Unit	Condition
V_{OH}	Output HIGH Voltage		2.4			V	I_{OUT} = −5.0 mA Note 5
V_{OL}	Output LOW Voltage				0.4	V	I_{OUT} = 4.2 mA, Note 5
I_{DD}	Average V_{DD} Current	Normal Operation			35	mA	
		Standby			2.25	mA	
		Refresh			27	mA	
		Page Mode			27	mA	Note 3
I_{CC}	Average V_{CC} Current	Normal Operation/ Page Mode				mA	
		Standby/Refresh	−10		10	μA	Note 3, 4
I_{BB}	Average V_{BB} Current	Normal Operation/ Refresh/Page Mode			400	μA	
		Standby			200	μA	
I_{IN}	Input Leakage Current (Any Input)		−10		10	μA	
I_{OUT}	Output Leakage Current		−10		10	μA	
C_{IN1}	Input Capacitance, A_0-A_6, D_{IN}			4.0	5.0	pF	Note 6
C_{IN2}	Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$			8.0	10	pF	Note 6
C_{OUT}	Output Capacitance, D_{OUT}			5.0	7.0	pF	$\overline{CAS}$ = V_{IHC}

Recommended ac Operating Conditions (F4116) Over full range of voltage and T_A = −55°C to +85°C

Symbol	Characteristic	F4116-2 Min	F4116-2 Max	F4116-3 Min	F4116-3 Max	F4116-4 Min	F4116-4 Max	Unit	Note
t_{RC}	Random Read or Write Cycle Time	320		375		410		ns	7
t_{RWC}	Read-Write Cycle Time	320		375		425		ns	7
t_{RMW}	Read Modify Write Cycle Time	320		405		500		ns	7
t_{PC}	Page Mode Cycle Time	170		225		275		ns	7
t_{RAC}	Access Time from $\overline{RAS}$		150		200		250	ns	8, 10
t_{CAC}	Access Time from $\overline{CAS}$		100		135		165	ns	9, 10
t_{OFF}	Output Buffer Turn-off Delay	0	40	0	50	0	60	ns	11
t_{RP}	$\overline{RAS}$ Precharge Time	100		120		150		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	150	5000	200	5000	250	5000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	100		135		165		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	150		200		250		ns	

Notes on final page.

Recommended ac Operating Conditions (F4116) (Cont'd)

Symbol	Characteristic	F4116-2		F4116-3		F4116-4		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CAS}	$\overline{CAS}$ Pulse Width	100	5000	135	5000	165	5000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	65	35	85	ns	12
t_{ASR}	Row Address Set-up Time	0		0		0		ns	
t_{RAH}	Row Address Hold Time	20		25		35		ns	
t_{ASC}	Column Address Set-up Time	0		0		0		ns	
t_{CAH}	Column Address Hold Time	45		55		75		ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_T	Transition Time (rise and fall)	3.0	35	3.0	50	3.0	50	ns	13
t_{RCS}	Read Command Set-up Time (RMW)	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{WCH}	Write Command Hold Time	45		55		75		ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{WCS}	Write Command Set-up Time	0		0		0		ns	14
t_{WP}	Write Command Pulse Width	45		55		75		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	50		70		85		ns	15
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	50		70		85		ns	15
t_{DS}	Data In Set-up Time	0		0		0		ns	16
t_{DH}	Data In Hold Time	45		55		75		ns	16
t_{DHR}	Data In Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		0		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Page-mode)	60		80		100		ns	
t_{RF}	Refresh Period		2.0		2.0		2.0	ms	
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	60		80		90		ns	17
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	110		145		175		ns	17

Notes on final page.

DC Requirements (F4116/240) T_C = −55°C to +110°C, Notes 1 and 2

Symbol	Characteristic	F4116/240 Min	Typ	Max	Unit	Condition
V_{DD}	Supply Voltage	10.8	12	13.2	V	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	Note 5
V_{SS}	Supply Voltage	0	0	0	V	
V_{BB}	Supply Voltage	−5.5	−5.0	−4.5	V	
V_{IHC}	Input HIGH Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	2.7		7.0	V	
V_{IH}	Input HIGH Voltage, All Inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	2.4		7.0	V	
V_{IL}	Input LOW Voltage, All Inputs	−1.0		0.8	V	

DC Characteristics (F4116/240) Over full range of voltage and T_C = −55°C to +110°C

Symbol	Characteristic		F4116/240 Min	Typ	Max	Unit	Condition
V_{OH}	Output HIGH Voltage		2.4			V	I_{OUT} = −5.0 mA, V_{CC} = 4.5 V Note 5
V_{OL}	Output LOW Voltage				0.4	V	I_{OUT} = 4.2 mA, V_{CC} = 4.5 V Note 5
I_{DD}	Average V_{DD} Current	Normal Operation			35	mA	
		Standby			1.75	mA	
		Refresh			27	mA	
		Page Mode			27	mA	Note 3
I_{CC}	Average V_{CC} Current	Normal Operation			600	μA	
		Page Mode			1000	μA	
		Standby/Refresh	−10		10	μA	Notes 3 and 4
I_{BB}	Average V_{BB} Current	Normal Operation/ Refresh/Page Mode			400	μA	
		Standby			200	μA	
I_{IN}	Input Leakage Current (Any Input)		−10		10	μA	V_{IN} = 0 to 7.0 V
I_{OUT}	Output Leakage Current		−10		10	μA	$\overline{RAS}$ and $\overline{CAS}$ = V_{IHC} V_{OUT} = 0 to 5.5 V
C_{IN1}	Input Capacitance, A_0-A_6, D_{IN}			4.0	5.0	pF	Note 6
C_{IN2}	Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$			8.0	10	pF	Note 6
C_{OUT}	Output Capacitance, D_{OUT}			5.0	7.0	pF	$\overline{CAS}$ = V_{IHC}

Notes on final page.

Recommended ac Operating Conditions (F4116/240) Over full range of voltage and T_C = −55°C to +110°C

Symbol	Characteristic	F4116/240-01 F4116/240-03* Min	F4116/240-01 F4116/240-03* Max	F4116/240-02 Min	F4116/240-02 Max	Unit	Note
t_{RC}	Random Read or Write Cycle Time	375	10120	410	10120	ns	7
t_{RWC}	Read-Write Cycle Time	375	10120	425	10120	ns	7
t_{PC}	Page Mode Cycle Time	225		275		ns	
t_{RAC}	Access Time from $\overline{RAS}$		200		250	ns	8, 10
t_{CAC}	Access Time from $\overline{CAS}$		135		165	ns	9, 10
t_{OFF}	Output Buffer Turn-off Delay		50		60	ns	11
t_{RP}	$\overline{RAS}$ Precharge Time	120	1000	150	1000	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	200	10,000	250	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	135		165		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	200		250		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	135	10,000	165	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	30	65	35	85	ns	12
t_{ASR}	Row Address Set-up Time	0		0		ns	
t_{RAH}	Row Address Hold Time	30		35		ns	
t_{ASC}	Column Address Set-up Time	0		0		ns	
t_{CAH}	Column Address Hold Time	60		75		ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	125		160		ns	
t_T	Transition Time (Rise and Fall)	3.0	50	3.0	50	ns	13
t_{RCS}	Read Command Set-up Time (RMW)	0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		ns	
t_{WCH}	Write Command Hold Time	60		75		ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	125		160		ns	
t_{WCS}	Write Command Set-up Time	0		0		ns	14
t_{WP}	Write Command Pulse Width	60		75		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	80		100		ns	15
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	80		100		ns	15
$t_{DS(C)}$	Data In Set-up Time	0		0		ns	16
$t_{DS(W)}$	Data In Set-up Time (Late Write)	10		10		ns	16
t_{DH}	Data In Hold Time	60		75		ns	16
t_{DHR}	Data In Hold Time Referenced to $\overline{RAS}$	125		160		ns	

*03 (200 ns Page Mode Operation Guaranteed)

Notes on final page.

7

Recommended ac Operating Conditions (F4116/240) (Cont'd)

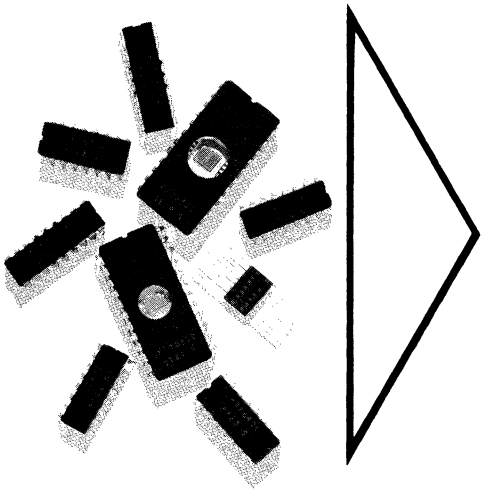
Symbol	Characteristic	F4116/240-01 F4116/240-03*		F4116/240-02		Unit	Note
		Min	Max	Min	Max		
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Page-mode)	80		100		ns	
t_{RF}	Refresh Period		1.0		1.0	ms	
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	95		125		ns	17
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	160		200		ns	17

*03 (200 ns Page Mode Operation Guaranteed)

Notes

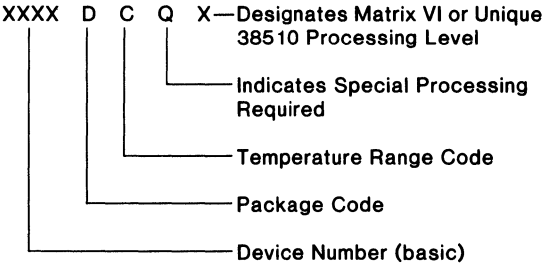
1. The ambient temperature (T_A) is specified here for operation at frequencies up to that frequency determined by the minimum cycle time. Operation at high cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided ac operating parameters are met.
2. All voltages are referenced to V_{SS} = 0 V.
3. I_{DD} depends on frequency of operation. Maximum current is measured at the fastest cycle rate.
   Normal Operation: $\overline{RAS}$ and $\overline{CAS}$ cycling
   Standby: $\overline{RAS}$ and $\overline{CAS}$ = V_{IHC}, D_{OUT}, = High Z
   Refresh $\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}
   Page Mode: $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling
4. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only. During readout of HIGH level data, V_{CC} is connected through a low impedance (135 Ω typ) to Data Out. At other times I_{CC} consists of leakage currents only.
5. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of reducing power in the standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the $V_{OH(min)}$ specification is not guaranteed in this mode.
6. Effective capacitance calculated from the equation $C = I \frac{\Delta t}{\Delta V}$ with ΔV = 3 V and power supplies at normal levels.
7. The specifications for $t_{RC(min)}$, $t_{RWC(min)}$, $t_{RMW(min)}$ and $t_{PC(min)}$ are used only to indicate cycle time at which proper operation over full temperature range (0°C ≤ T_A ≤ 70°C) is assured. All transition times, t_T, are assumed to be 5 ns.
8. Assumes that $t_{RCD} \leq t_{RCD(max)}$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
10. Measured with a load equivalent to two TTL loads and 100 pF.
11. $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
13. $V_{IHC(min)}$ or $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}. Composite timing parameters (such as cycle times) assume 5 ns transition times.
14. t_{WCS} is a restrictive operating parameter. If $t_{WCS} \geq t_{WCS(min)}$, the cycle is an early write cycle and the Data Out pin will remain open circuit (high impedance) throughout the entire cycle, otherwise the cycle is a delayed write cycle.
15. The parameters t_{RWL} and t_{CWL} reference $\overline{WE}$ (for a read-modify-write cycle) to either $\overline{RAS}$ or $\overline{CAS}$ respectively, whichever is the first to go HIGH.
16. t_{DS} and t_{DH} are referenced to the leading edge of $\overline{CAS}$ in early write cycles, and to the leading edge of $\overline{WE}$ in delayed write or read-modify-write cycles.
17. t_{RWD} and t_{CWD} are restrictive operating parameters due to the following characteristics:
    If $t_{CWD} < t_{CWD(min)}$, the Data Out will be indeterminate
    If $t_{CWD} \geq t_{CWD(min)}$, the Data Out will contain the data read from the selected cell.

For block diagram, functional description, timing diagrams and characteristic curves refer to standard F4116 data sheet, Section 3.



Section 8
Ordering Information and Package Outlines

Specific ordering codes, as well as the temperature ranges and package types available, are listed on each data sheet in Sections 3 through 7. The Product Index and Selection Guides given in Section 1 list only the *basic device numbers*. This basic number is used to form part of a simplified purchasing code where the package type, temperature range and processing level are defined as follows:



Package Code—One letter represents the basic package type. Different package outlines exist within each package type to accommodate varying die sizes and number of pins, as indicated below:

D— Ceramic (Hermetic) Dual In-line
Side-braze—WC, 7R
Ceramic DIP—JD, 2C, 6Z, 7C, 7M, 7W, 8D, 8E

P— Plastic Dual In-line
UB, UC, 8J, 8K, 9B

F— Flatpak
II, 2R, 4A

Package Outlines—The package outlines indicated by the codes above are shown in the detailed outline drawings in this section.

Temperature Range—Three basic temperature grades are in common use:

C = Commercial
0°C to +70°C

L = Limited Military
−55°C to +85°C

M = Military
−55°C to +125°C

Unique 38510

The Fairchild Unique 38510 program is written in accordance with MIL-M-38510 and MIL-STD-883 to meet the need for improved reliability in the military market. Devices ordered to this program are subjected to 100% screening as outlined in *Table 1.*

Customer procurement documents should specify the following:

1. Fairchild Product Code indicating the basic device number, package code letter and temperature range code letter;
2. the Unique 38510 device class (B or S);
3. Number or Letter Options required;
4. special marking requirements if Number Option 6 was specified.

Unique 38510 Ordering Code Examples

21021FMQB	Device number 21021, packaged in ceramic flatpak (F), in military temperature range (M) and processed to Unique 38510 Class B.
21021DMQS	Device number 21021, packaged in ceramic Dual In-line (D), in military temperature range (M) and processed to Unique 38510 Class S.

Number Options (apply to operations performed on each unit delivered)

Option 1	Lead form to dimensions in detail specifications, followed by hermetic seal tests.
Option 2	Hot solder dip finish.
Option 3	Read and record critical parameters before and after burn-in.
Option 4	Initial qualification, Group B, C and D quality conformance not required.
Option 5	Radiographic inspection shall be performed on all devices.
Option 6	Special marking required.
Option 7	Non-conforming variation—refer to procurement documents for details (must be negotiated with factory).

Letter Options (apply once per Purchase Order or line item and are considered test charges)

Option A	Group C testing shall be performed.
Option B	Group D testing shall be performed.
Option C	Generic data to be supplied from the latest completed lot.
Option D	Unique 38510 program plan, pertinent to the device family being purchased, shall be supplied.

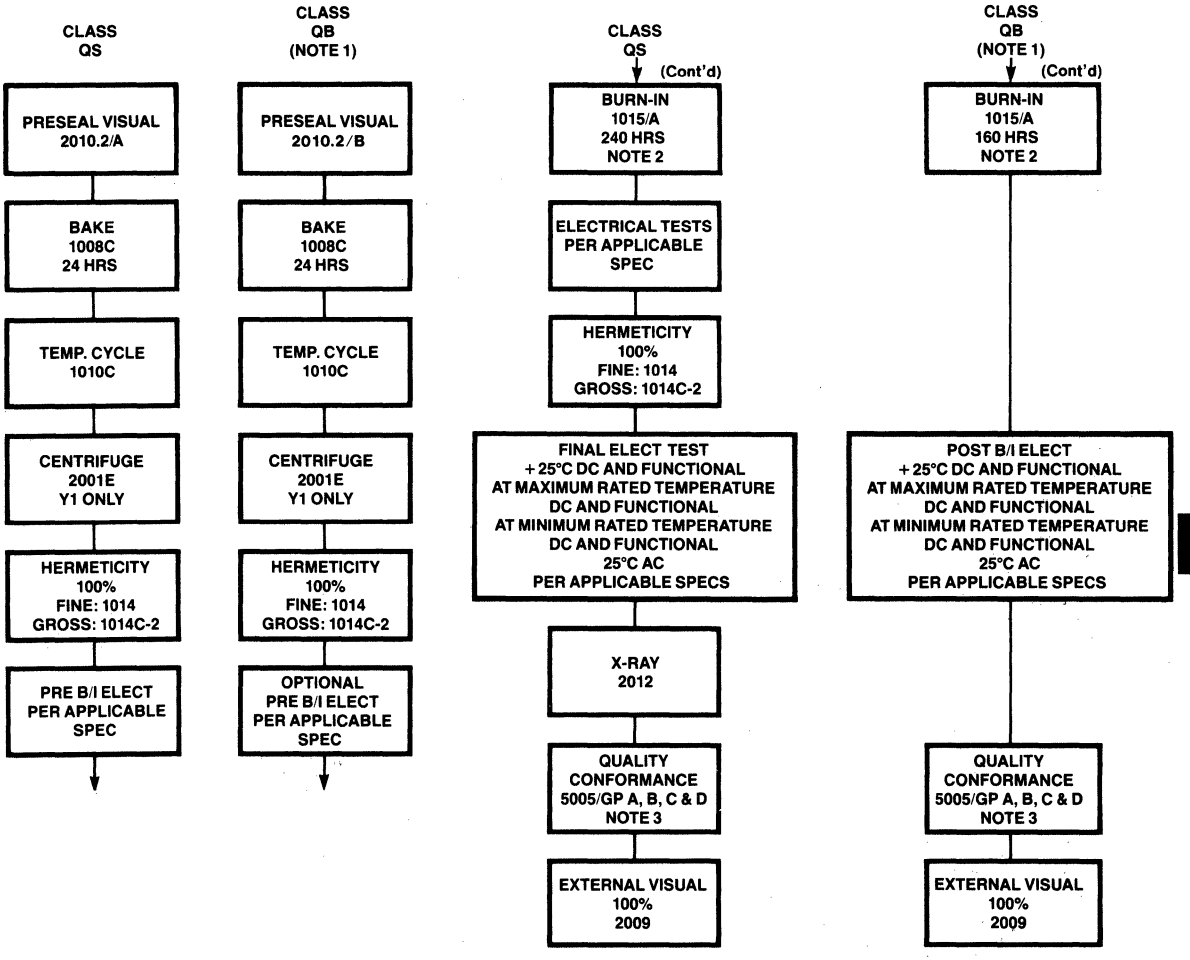
Matrix VI

Matrix VI is a full spectrum, cost effective reliability and quality program for commercial or industrial integrated circuits only. This program features six levels of flow screening, each tailored to a user's field application environment and incoming quality and equipment reliability requirements. A Matrix VI part number consists of the device number followed by the package code letter, the temperature range code letter, the special processing indicator (Q) and the Matrix VI code letter as shown in the following examples. See *Table 2* for processing level definition.

Matrix VI Ordering Code Examples

21021PC	Device number 21021, packaged in plastic Dual In-line (P), in commercial temperature range (C) and processed to Matrix VI Level 1.
21021DC	Device number 21021, packaged in ceramic Dual In-line (D), in commercial temperature range and processed to Matrix VI Level 3.
21021PCQR	Device number 21021, packaged in plastic Dual In-line (P), in commercial temperature range (C) with supplemental Matrix VI Level 5 screening, including 100% thermal shock, "hot rail" test, 168 hours +125°C burn-in and 0.1% AQL functional testing.
21021DCQR	Device number 21021, packaged in ceramic Dual In-line (D), in commercial temperature range (C) with supplemental Matrix VI Level 6 screening, including burn-in, three 100% dc/functional tests and 0.1% AQL functional testing.

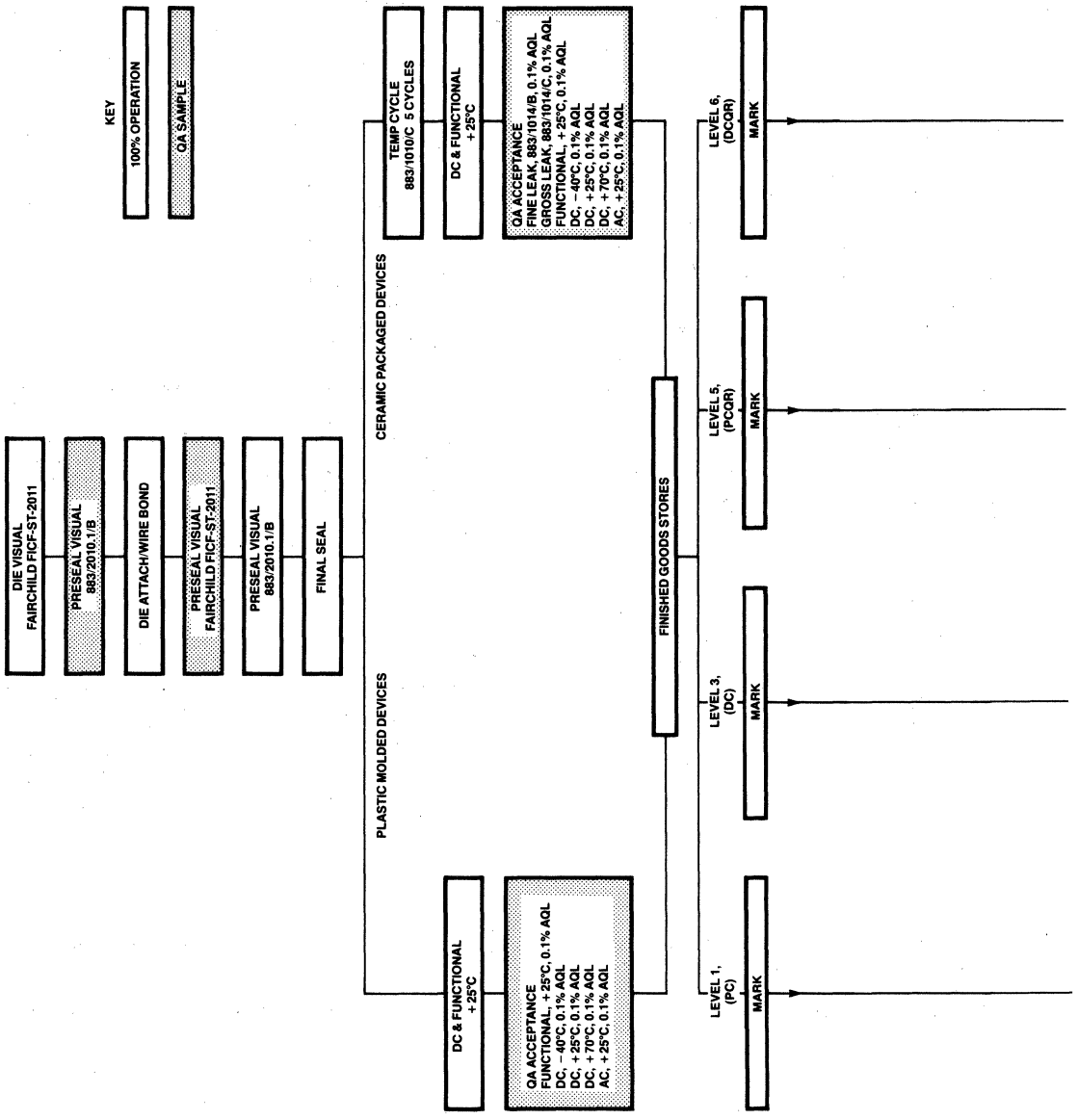
Table 1 Unique 38510 Process Flow

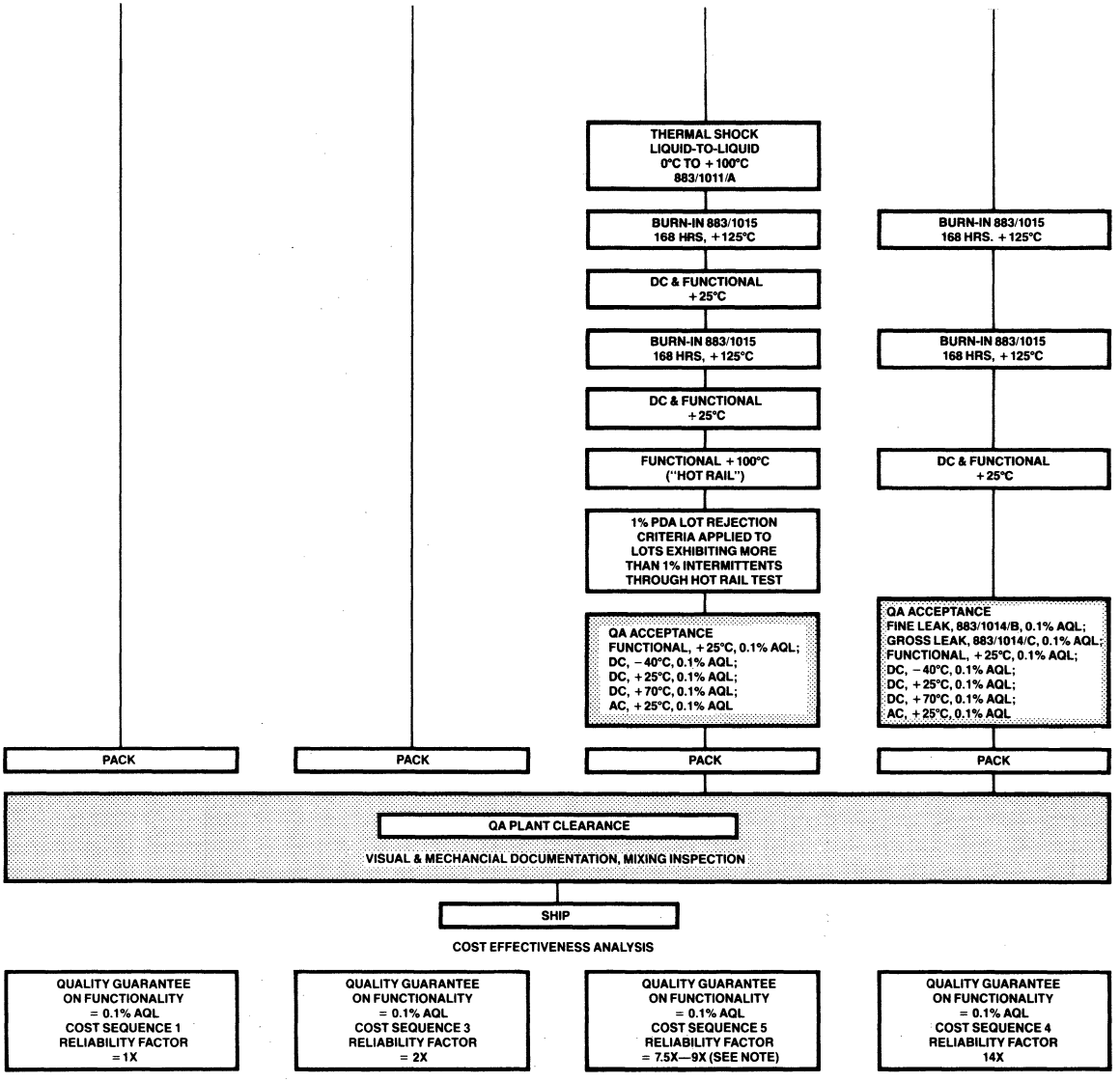


Notes

1. Class B processing in this case includes adding 100% post burn-in testing: dc testing at maximum and minimum rated temperatures (See data sheet for rating.); ac testing at +25°C.
2. Any burn-in condition other than MTD 1015 Condition A is at customer request only.
3. Qualification testing per groups B, C and D on a customer's parts require additional lot charges and an added minimum of two months to the schedules deliveries.

Table 2 Matrix VI Process Flow Options & Cost Effectiveness

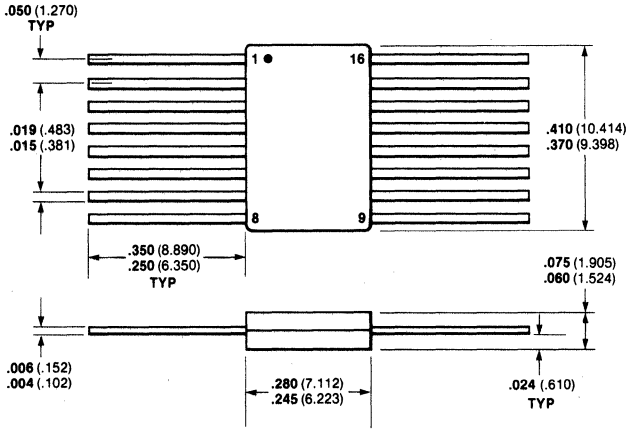




Note

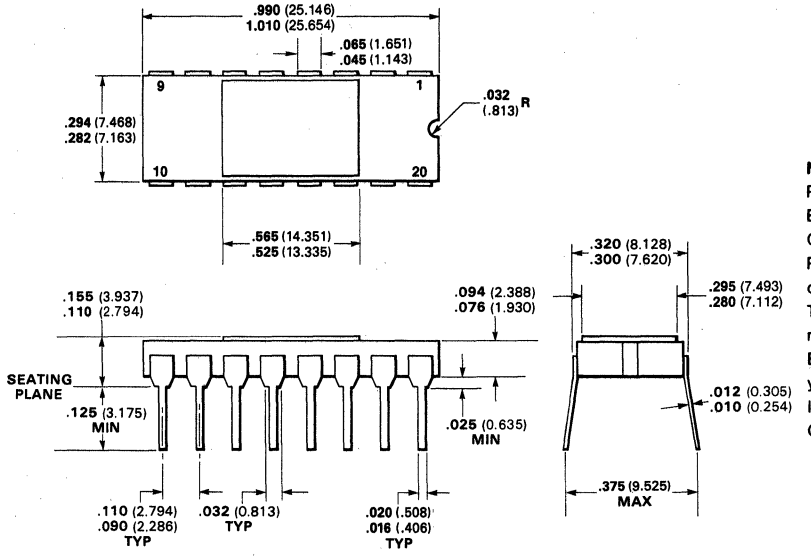
Burn-In has the same relative effectiveness for plastic molded devices as for ceramic/hermetic packaged devices. Assuming a controlled (air conditioned and constant power) field application/environment, the reliability factor would be approximately 9X. But should the field application be in a less controlled and power ON/OFF application, the reliability factor would be approximately 7.5X.

16-Pin Ceramic Flatpak — II



Notes
Pins are tin-plated 42 alloy
Cap and base are alumina
Cavity size is **.140** x **.200** (3.556 x 5.080), silver plated
Package weight is 0.4 gram

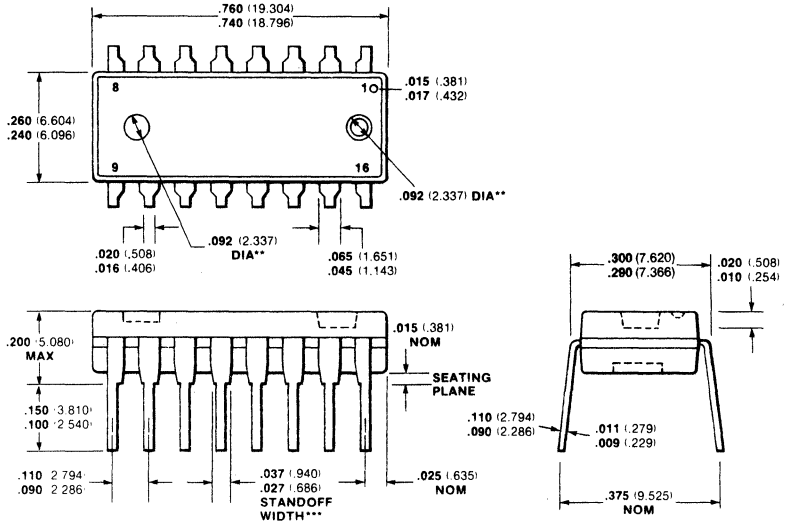
20-Pin Ceramic DIP (Metal Cap) — JD



Notes
Pins are gold-plated kovar
Base is Al_2O_3
Cap is kovar
Pins are intended for insertion in hole rows on **.300**" (7.620) centers
They are purposely shipped with positive misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.020**" (5.080) diameter lead
Cavity size is **.200** x **.375** (5.08 x 9.52)

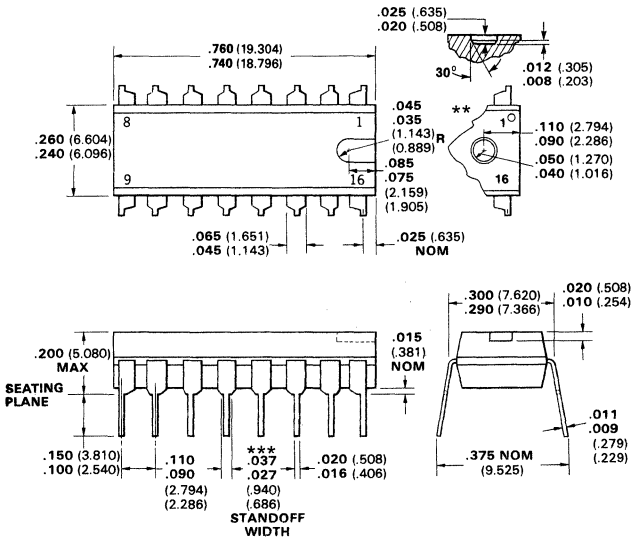
All dimensions in inches bold and millimeters (parentheses)

16-Pin Plastic DIP — UB



Notes
Pins are tin-plated OLIN 195 copper
Package material varies depending on the product line
Leads are intended for insertion in hole rows on **.300**" (7.620) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.020**" (.510) diameter lead
***The **.037-.027** (.940-.686) dimension does not apply to the corner leads
**Notch or ejector hole varies depending on the product line
Package weight is 0.9 gram
Polyimide die attach

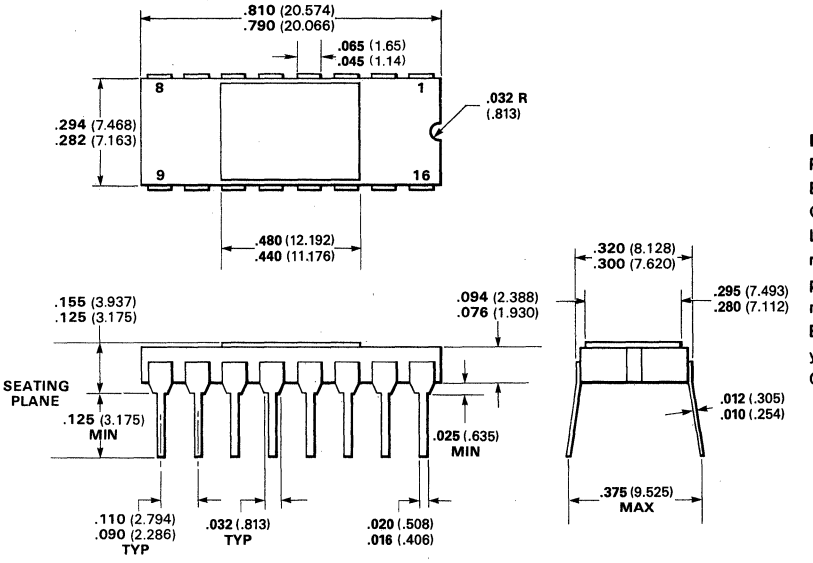
16-Pin Plastic DIP — UC



Notes
Pins are tin-plated copper
Package material varies depending on the product line
Pins are intended for insertion in hole rows on **.300**" (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.020** inch (0.51) diameter pin
***The **.037-.027** (.940-.686) dimension does not apply to the corner pins
**Notch or ejector hole varies depending on the product line
Package weight is 0.9 gram

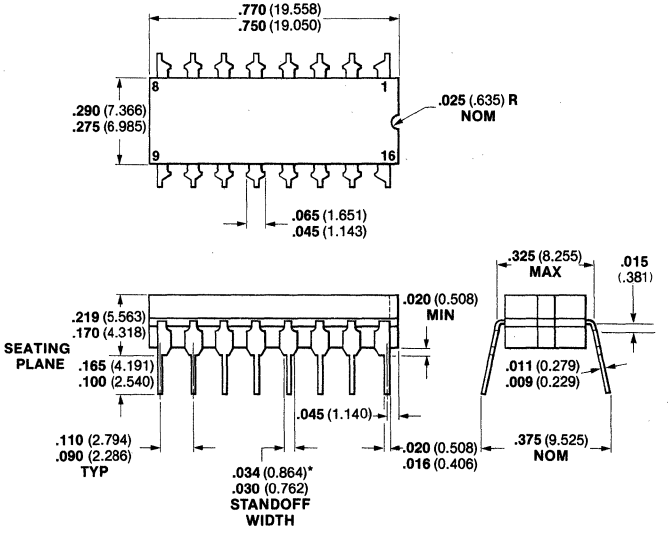
All dimensions in inches bold and millimeters (parentheses)

16-Pin Side-Brazed DIP (Metal Cap) WC



Notes
Pins are gold-plated kovar or alloy 42
Base is Al_2O_3
Cap is kovar
Leads are intended for insertion in hole rows on **.300"** (7.620) centers. They are purposely shipped with positive misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.020"** (5.080)
Cavity size is **.170** x **.320** (4.318 x 8.128)

16-Pin Ceramic DIP 2C

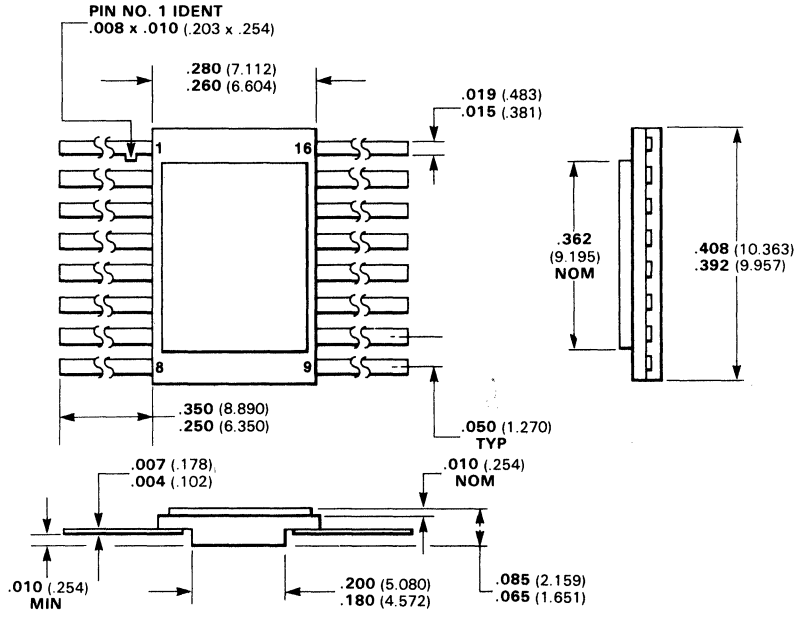


Notes
Pins are tin-plated alloy 42
Pins are intended for insertion in hole rows on **.300"** (7.620) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.020** inch (5.080) diameter pin
Hermetically sealed alumina package
Cavity size is **.160** x **.310** (4.064 x 7.874)
*The **.034-.030** (.864-.762) dimension does not apply to the corner pins
Package weight is 2.2 grams

All dimensions in inches bold and millimeters (parentheses)

16-Pin Side-Brazed Flatpak

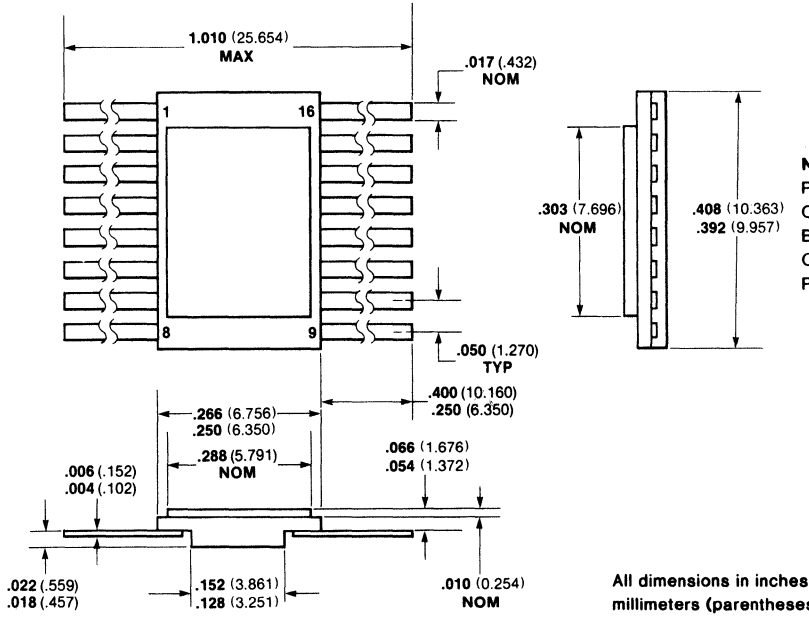
2R



Notes
Package body is black ceramic
Pins are gold plated kovar or alloy 42
Lid is gold plated kovar
Package is hermetic
Package weight is 1.1 grams

16-Pin Ceramic Flatpak

4A

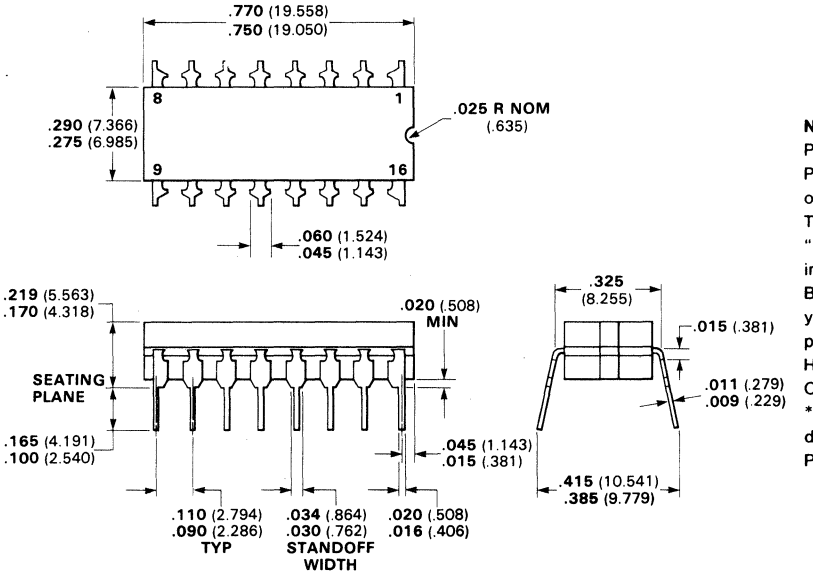


Notes
Pins are Ni Au plated kovar
Cap is kovar
Base is Al_2O_3
Cavity size is **.110** x **.180** (2.794 x 4.572)
Package weight is approximately 0.6 gram

All dimensions in inches bold and millimeters (parentheses)

16-Pin Ceramic DIP

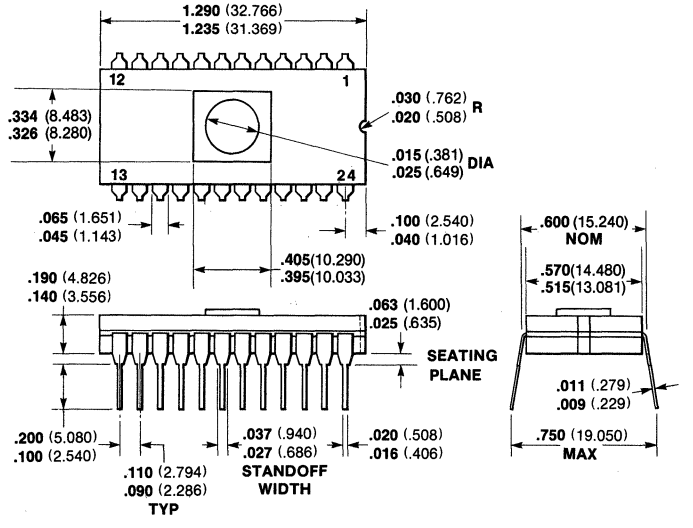
6Z



Notes
Pins are tin-plated alloy 42
Pins are intended for insertion in hole rows on **.300**" (7.620) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.020** inch (.508) diameter pin
Hermetically sealed alumina package
Cavity size is **.160** x **.250** (4.064 x 6.350)
*The **.034-.030** (.864-.762) dimension does not apply to the corner pins
Package weight is 2.2 grams

24-Pin Ceramic DIP

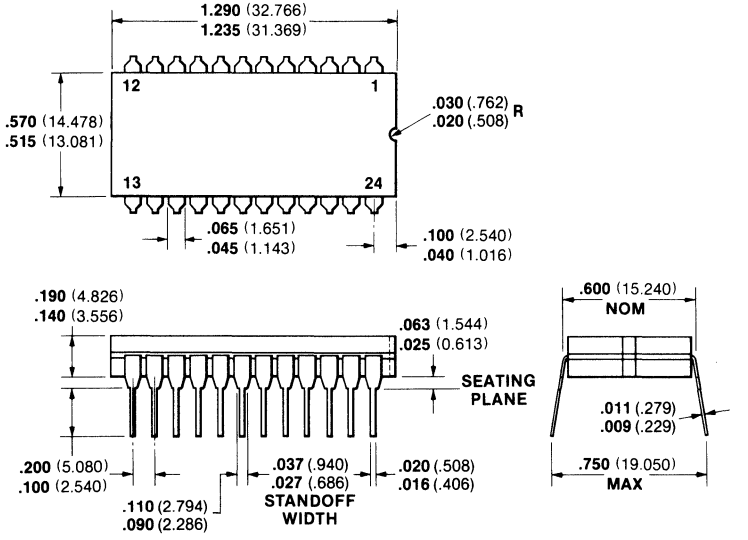
7C



Notes
Pins are tin-plated alloy 42
Package material is alumina
Pins are intended for insertion in hole rows on **.600** (15.240) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Cavity size is **.260** x **.260** (6.604 x 6.604)
Package weight is 6.5 grams
Window—UV transmission glass

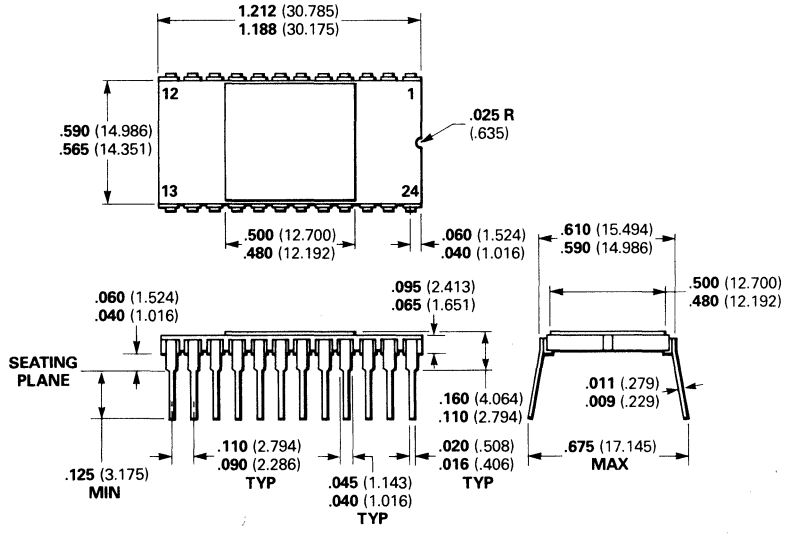
All dimensions in inches **bold** and millimeters (parentheses)

24-Pin Ceramic DIP 7M



Notes
Pins are tin-plated alloy 42
Package material is alumina
Pins are intended for insertion in hole rows on **.600** (15.240) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Cavity size is **.250** x **.250** (6.350 x 6.350)
Package weight is 6.5 grams

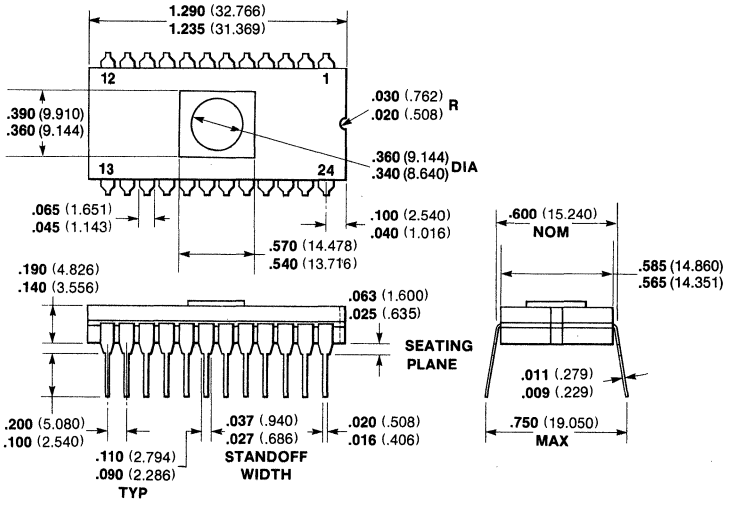
24-Pin Side-Brazed DIP 7R



Notes
Pins are nickel gold-plated kovar or alloy 42
Cap is kovar
Base is Ceramic
Cavity size is **.250** x **.250** (6.350 x 6.350)
Package weight is 3.85 grams

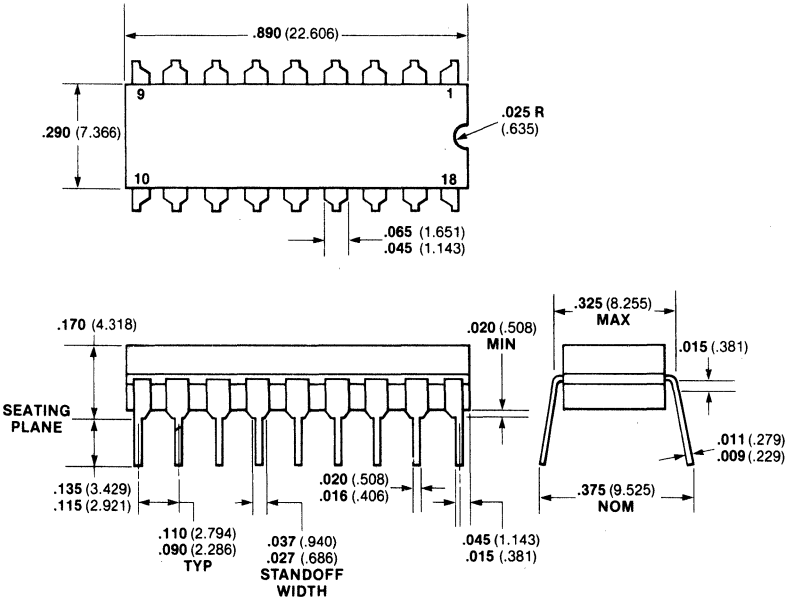
All dimensions in inches **bold** and millimeters (parentheses)

24-Pin Ceramic DIP — 7W



Notes
Pins are tin-plated alloy 42
Package material is alumina
Pins are intended for insertion in hole rows on **.600** (15.240) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Cavity size is **.260** x **.260** (6.604 x 6.604)
Package weight is 6.5 grams

24-Pin Ceramic DIP — 8D

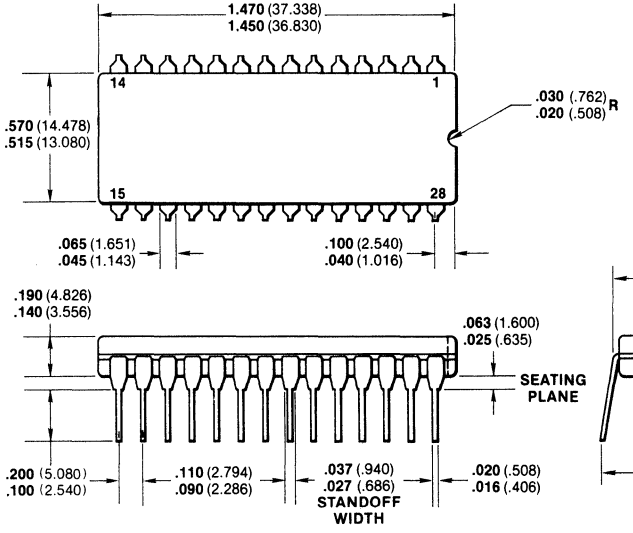


Notes
Pins are tin-plated alloy 42
Package material is alumina
Pins are intended for insertion in hole rows on **.300** (7.620) centers
They are purposely shipped with positive misalignment to facilitate insertion
Package weight is 3.0 grams

All dimensions in inches **bold** and millimeters (parentheses)

28-Pin Ceramic DIP

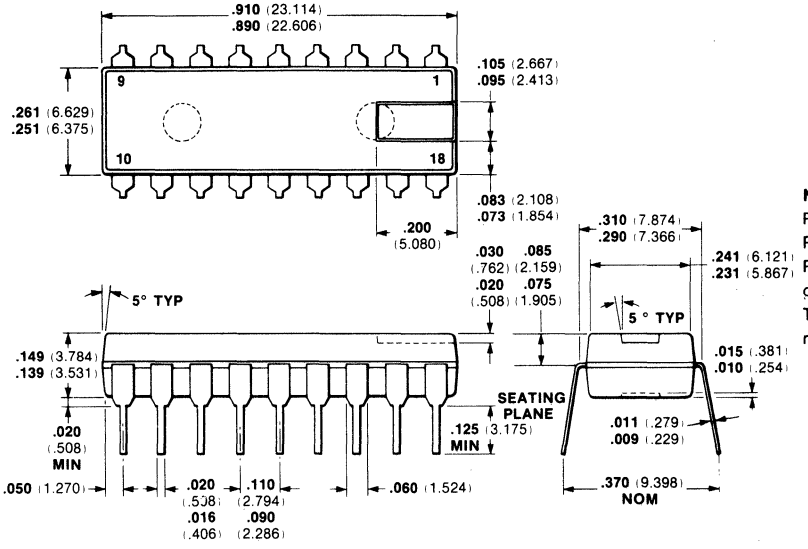
8E



Notes
Pins are tin-plated alloy 42
Package material is alumina
Pins are intended for insertion in hole rows on **.600** (15.240) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Cavity size is **.240** x **.240** (6.096 x 6.096)
Package weight is 7.5 grams

18-Pin Plastic DIP

8J

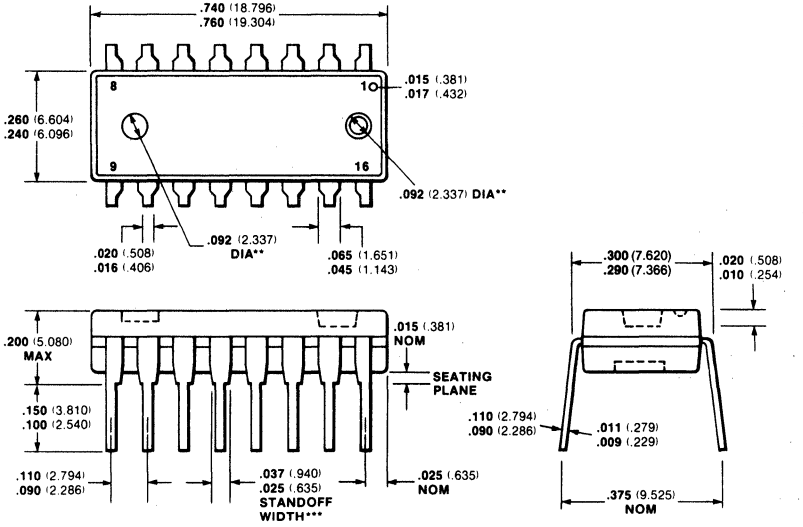


Notes
Pins are tin-plated alloy 42
Package material is plastic
Pins are intended for insertion in hole rows on **.300** (7.620) centers
They are purposely shipped with positive misalignment to facilitate insertion

All dimensions in inches **bold** and millimeters (parentheses)

Ordering Information and Package Outlines

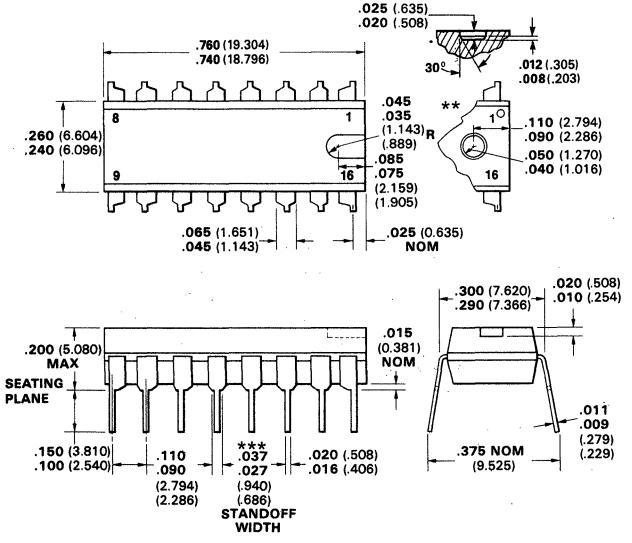
16-Pin Plastic DIP 8K



Notes

Pins are tin-plated kovar or alloy 42 nickel
Package material varies depending on the product line
Pins are intended for insertion in hole rows on **.300**" (7.620) centers
They are purposely shipped with positive misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.020**" (0.510) diameter pin
***The **.037-.027** (.940-.690) dimension does not apply to the corner leads
**Notch or ejector hole varies depending on the product line
Package weight is 0.9 gram

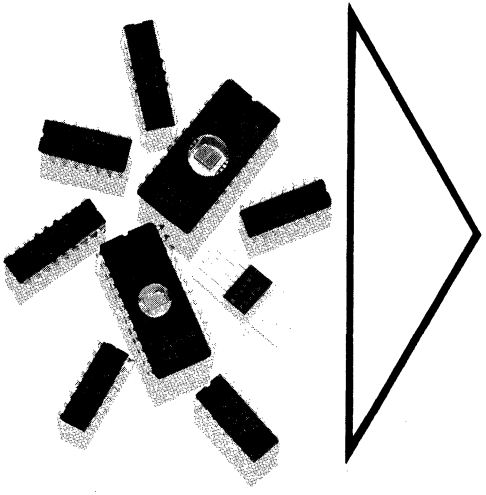
16-Pin Plastic DIP 9B



Notes

Pins are tin-plated kovar or alloy 42 nickel
Package material varies depending on the product line
Pins are intended for insertion in hole rows on **.300**" (7.620) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.020**" (0.508) diameter pin
***The **.037-.027** (.940-.686) dimension does not apply to the corner pins
**Notch or ejector hole varies depending on the product line
Package weight is 0.9 gram

All dimensions in inches bold and millimeters (parentheses)



Fairchild Semiconductor

Alabama
Hall Mark Electronics
4900 Bradford Drive
Huntsville, Alabama 35807
Tel: 205-837-8700 TWX: 810-726-2187

Hamilton/Avnet Electronics
4692 Commercial Drive
Huntsville, Alabama 35805
Tel: 205-837-7210
Telex: None — use HAMAVLECB DAL 73-0511
(Regional Hq. in Dallas, Texas)

Arizona
Hamilton/Avnet Electronics
505 South Madison Drive
Tempe, Arizona 85281
Tel: 602-231-5100 TWX: 910-951-1535

Kierulff Electronics
4134 East Wood Street
Phoenix, Arizona 85040
Tel: 602-243-4101

Wyle Distribution Group
8155 North 24th Avenue
Phoenix, Arizona 85021
Tel: 602-249-2232 TWX: 910-951-4282

California
Anthem Electronics, Inc.
21730 Nordhoff Street
Chatsworth, California 91311
Tel: 213-700-1000 TWX: 910-493-2083

Anthem Electronics, Inc.
4125 Sorrento Valley Blvd.
San Diego, California 92121
Tel: 714-279-5200

Anthem Electronics, Inc.
174 Component Drive
San Jose, California 95131
Tel: 408-946-8000

Anthem Electronics, Inc.
2661 Dow Avenue
Tustin, California 92680
Tel: 714-730-8000

Arrow Electronics
9511 Ridge Haven Court
San Diego, California 92123
Tel: 714-565-4800

Arrow Electronics
521 Weddell Avenue
Sunnyvale, California 94086
Tel: 408-745-6600 TWX: 910-339-9371

Avnet Electronics
350 McCormick Avenue
Costa Mesa, California 92626
Tel: 714-754-6111 (Orange County)
213-558-2345 (Los Angeles)
TWX: 910-595-1928

Bell Industries
Electronic Distributor Division
1161 N. Fair Oaks Avenue
Sunnyvale, California 94086
Tel: 408-734-8570 TWX: 910-339-9378

Franchised Distributors

Hamilton/Avnet Electronics
3170 Pullman Avenue
Costa Mesa, California 92626
Tel: 714-641-1850

Hamilton Electro Sales
10912 West Washington Blvd.
Culver City, California 90230
Tel: 213-558-2121 TWX: 910-340-6364

Hamilton/Avnet Electronics
4545 Viewridge Avenue
San Diego, California 92123
Tel: 714-571-7527
Telex: HAMAVELEC SDG 69-5415

Hamilton/Avnet Electronics
1175 Bordeaux Drive
Sunnyvale, California 94086
Tel: 408-743-3355 TWX: 910-379-6486

**Sertech Laboratories
2120 Main Street, Suite 190
Huntington Beach, California 92647
Tel: 714-960-1403

Wyle Electronics
124 Maryland Street
El Segundo, California 90245
Tel: 213-322-8100 TWX: 910-348-7111

Wyle Distributor Group
17872 Cowan Avenue
Irvine, California 92714
Tel: 714-641-1600
Telex: 910-595-1572

Wyle Distribution Group
9525 Chesapeake
San Diego, California 92123
Tel: 714-565-9171 TWX: 910-335-1590

Wyle Distribution Group
3000 Bowers Avenue
Santa Clara, California 95051
Tel: 408-727-2500 TWX: 910-338-0541

Colorado
Arrow Electronics
2121 South Hudson
Denver, Colorado 80222
Tel: 303-758-2100

Bell Industries
8155 West 48th Avenue
Wheatridge, Colorado 80033
Tel: 303-424-1985 TWX: 910-938-0393

Hamilton/Avnet Electronics
8765 E. Orchard Rd., Suite 708
Englewood, Colorado 80111
Tel: 303-740-1000 TWX: 910-935-0787

Wyle Distribution Group
451 East 124th Avenue
Thornton, Colorado 80241
Tel: 303-457-9953 TWX: 910-936-0770

Connecticut
Arrow Electronics
12 Beaumont Road
Wallingford, Connecticut 06492
Tel: 203-265-7741 TWX: 203-265-7741

United States and Canada

Hamilton/Avnet Electronics
Commerce Drive, Commerce Park
Danbury, Connecticut 06810
Tel: 203-797-2800
TWX: None — use 710-897-1405
(Regional Hq. in Mt. Laurel, N.J.

Harvey Electronics
112 Main Street
Norwalk, Connecticut 06851
Tel: 203-853-1515

Schweber Electronics
Finance Drive
Commerce Industrial Park
Danbury, Connecticut 06810
Tel: 203-792-3500

Florida
Arrow Electronics
1001 Northwest 62nd Street
Suite 108
Ft. Lauderdale, Florida 33309
Tel: 305-776-7790

Arrow Electronics
50 Woodlake Drive West
Building B
Palm Bay, Florida 32905
Tel: 305-725-1480

Hall Mark Electronics
1671 West McNab Road
Ft. Lauderdale, Florida 33309
Tel: 305-971-9280 TWX: 510-956-3092

Hall Mark Electronics
7233 Lake Ellenor Drive
Orlando, Florida 32809
Tel: 305-855-4020 TWX: 810-850-0183

Hamilton/Avnet Electronics
6801 N.W. 15th Way
Ft. Lauderdale, Florida 33309
Tel: 305-971-2900 TWX: 510-954-9808

Hamilton/Avnet Electronics
3197 Tech Drive, North
St. Petersburg, Florida 33702
Tel: 813-576-3930

Schweber Electronics
2830 North 28th Terrace
Hollywood, Florida 33020
Tel: 305-927-0511 TWX: 510-954-0304

Georgia
Arrow Electronics
2979 Pacific Drive
Norcross, Georgia 30071
Tel: 404-449-8252
Telex: 810-766-0439

Hall Mark Electronics
6410 Atlantic Blvd., Suite 115
Norcross, Georgia 30071
Tel: 404-447-8000 TWX: 810-766-4510

Hamilton/Avnet Electronics
5825-D Peachtree Corners East
Norcross, Georgia 30092
Tel: 404-447-7500
Telex: None — use HAMAVLECB DAL 73-0511
(Regional Hq. in Dallas, Texas)

**This distributor carries Fairchild *die* products only.

Fairchild Semiconductor

Franchised Distributors

United States and Canada

Illinois
Arrow Electronics
492 Lunt Avenue
Schaumburg, Illinois 60193
Tel: 312-893-9420

Hall Mark Electronics
1177 Industrial Drive
Bensenville, Illinois 60106
Tel: 312-860-3800

Hamilton/Avnet Electronics
1130 Thorndale Avenue
Bensenville, Illinois 60106
Tel: 312-860-7780 TWX: 910-227-0060

Kierulff Electronics
1536 Landmeier Road
Elk Grove Village, Illinois 60007
Tel: 312-640-0200 TWX: 910-227-3166

Schweber Electronics
1275 Brummel Avenue
Elk Grove Village, Illinois 60007
Tel: 312-364-3750 TWX: 910-222-3453

Indiana
Arrow Electronics
2718 Rand Road
Indianapolis, Indiana 46241
Tel: 317-243-9353

Graham Electronics Supply, Inc.
133 S. Pennsylvania Street
Indianapolis, Indiana 46204
Tel: 317-634-8486 TWX: 810-341-3481

Hamilton/Avnet Electronics
485 Gradle Drive
Carmel, Indiana 46032
Tel: 317-844-9333

Pioneer Electronics
6408 Castle Place Drive
Indianapolis, Indiana 46250
Tel: 317-849-7300 TWX: 810-260-1794

Kansas
Hall Mark Electronics
10815 Lakeview Drive
Lenexa, Kansas 66215
Tel: 913-888-4747

Hamilton/Avnet Electronics
9219 Quivira Road
Overland Park, Kansas 66215
Tel: 913-888-8900
Telex: None — use HAMAVLECB DAL 73-0511
(Regional Hq. in Dallas, Texas)

Maryland
Hall Mark Electronics
6655 Amberton Drive
Baltimore, Maryland 21227
Tel: 301-796-9300

Hamilton/Avnet Electronics
6822 Oak Hall Lane
Columbia, Maryland 21045
Tel: 301-995-3500 TWX: 710-862-1861

Pioneer Electronics
9100 Gaither Road
Gaithersburg, Maryland 20760
Tel: 301-948-0710 TWX: 710-828-9784

Schweber Electronics
9218 Gaither Road
Gaithersburg, Maryland 20760
Tel: 301-840-5900 TWX: 710-828-0536

Massachusetts
Arrow Electronics
Arrow Drive
Woburn, Massachusetts 01801
Tel: 617-933-8130 TWX: 710-393-6770

Gerber Electronics
128 Carnegie Row
Norwood, Massachusetts 02026
Tel: 617-329-2400

Hamilton/Avnet Electronics
50 Tower Office Park
Woburn, Massachusetts 01801
Tel: 617-273-7500 TWX: 710-393-0382

Harvey Electronics
44 Hartwell Avenue
Lexington, Massachusetts 02173
Tel: 617-861-9200 TWX: 710-326-6617

Schweber Electronics
25 Wiggins Avenue
Bedford, Massachusetts 01730
Tel: 617-275-5100

**Sertech Laboratories
1 Peabody Street
Salem, Massachusetts 01970
Tel: 617-745-2450

Michigan
Arrow Electronics
3810 Varsity Drive
Ann Arbor, Michigan 48104
Tel: 313-971-8220

Hamilton/Avnet Electronics
2215 29th Street S.E.
Space A5
Grand Rapids, Michigan 49508
Tel: 616-243-8805 TWX: 810-273-6921

Hamilton/Avnet Electronics
32487 Schoolcraft
Livonia, Michigan 48150
Tel: 313-522-4700 TWX: 810-242-8775

Pioneer Electronics
13485 Stamford
Livonia, Michigan 48150
Tel: 313-525-1800

Schweber Electronics
33540 Schoolcraft
Livonia, Michigan 48150
Tel: 313-525-8100

Minnesota
Arrow Electronics
5230 West 73rd Street
Edina, Minnesota 55435
Tel: 612-830-1800

Hamilton/Avnet Electronics
10300 Bren Road East
Minnetonka, Minnesota 55343
Tel: 612-932-0600
TWX: None — use 910-227-0060
(Regional Hq. in Chicago, Illinois)

Schweber Electronics
7422 Washington Avenue S.
Eden Prairie, Minnesota 55344
Tel: 612-941-5280

Missouri
Hall Mark Electronics
13789 Rider Trail
Earth City, Missouri 63045
Tel: 314-291-5350

Hamilton/Avnet Electronics
13743 Shoreline Court, East
Earth City, Missouri 63045
Tel: 314-344-1200 TWX: 910-762-0684

New Hampshire
Arrow Electronics
1 Perimeter Road
Manchester, New Hampshire 03103
Tel: 603-668-6968

New Jersey
Arrow Electronics
Pleasant Valley Avenue
Moorestown, New Jersey 08057
Tel: 609-235-1900

Arrow Electronics
285 Midland Avenue
Saddle Brook, New Jersey 07662
Tel: 201-797-5800

Hall Mark Electronics
Springdale Business Center
2091 Springdale Road
Cherry Hill, New Jersey 08003
Tel: 609-424-0880

Hamilton/Avnet Electronics
10 Industrial Road
Fairfield, New Jersey 07006
Tel: 201-575-3390 TWX: 710-994-5787

Hamilton/Avnet Electronics
#1 Keystone Avenue
Cherry Hill, New Jersey 08003
Tel: 609-424-0100 TWX: 710-940-0262

Harvey Electronics
45 Route 46
Pinebrook, New Jersey 07058
Tel: 201-575-3510 TWX: 710-734-4382

Schweber Electronics
18 Madison Road
Fairfield, New Jersey 07006
Tel: 201-227-7880 TWX: 710-480-4733

Sterling Electronics
774 Pfeiffer Blvd.
Perth Amboy, New Jersey 08861
Tel: 201-442-8000 Telex: 138-679

New Mexico
Arrow Electronics
2460 Alamo Avenue S.E.
Albuquerque, New Mexico 87106
Tel: 505-243-4566

Bell Industries
11728 Linn Avenue N.E.
Albuquerque, New Mexico 87123
Tel: 505-292-2700 TWX: 910-989-0625

**This distributor carries Fairchild *die* products only.

Fairchild Semiconductor

Franchised Distributors

United States and Canada

Hamilton/Avnet Electronics
2524 Baylor Drive, S.E.
Albuquerque, New Mexico 87106
Tel: 505-765-1500
TWX: None — use 910-379-6486
(Regional Hq. in Mt. View, California)

New York
Arrow Electronics
900 Broadhollow Road
Farmingdale, New York 11735
Tel: 516-694-6800
TWX: 510-224-6155 & 510-224-6126

Arrow Electronics
20 Oser Avenue
Hauppauge, New York 11787
Tel: 516-231-1000

Arrow Electronics
P.O. Box 370
7705 Maltlage Drive
Liverpool, New York 13088
Tel: 315-652-1000 TWX: 710-545-0230

*Cadence Electronics
40-17 Oser Avenue
Hauppauge, New York 11787
Tel: 516-231-6722

Components Plus, Inc.
40 Oser Avenue
Hauppauge, New York 11787
Tel: 516-231-9200 TWX: 510-227-9869

Hamilton/Avnet Electronics
5 Hub Drive
Melville, New York 11746
Tel: 516-454-6000 TWX: 510-224-6166

Hamilton/Avnet Electronics
333 Metro Park
Rochester, New York 14623
Tel: 716-475-9130
TWX: None — use 710-332-1201
(Regional Hq. in Burlington, Ma.)

Hamilton/Avnet Electronics
16 Corporate Circle
E. Syracuse, New York 13057
Tel: 315-437-2642 TWX: 710-541-0959

Harvey Electronics
(mailing address)
P.O. Box 1208
Binghampton, New York 13902
(shipping address)
1911 Vestal Parkway East
Vestal, New York 13850
Tel: 607-748-8211

Harvey Electronics
60 Crossways Park West
Woodbury, New York 11797
Tel: 516-921-8920 TWX: 510-221-2184

Schweber Electronics
Jericho Turnpike
Westbury, L.I., New York 11590
Tel: 516-334-7474 TWX: 510-222-3660

Summit Distributors, Inc.
916 Main Street
Buffalo, New York 14202
Tel: 716-884-3450 TWX: 710-522-1692

*Minority Distributor

North Carolina
Arrow Electronics
938 Burke Street
Winston Salem, North Carolina 27102
Tel: 919-725-8711 TWX: 510-922-4765

Hamilton/Avnet Electronics
2803 Industrial Drive
Raleigh, North Carolina 27609
Tel: 919-829-8030

Hall Mark Electronics
1208 Front Street, Bldg. K
Raleigh, North Carolina 27609
Tel: 919-823-4465 TWX: 510-928-1831

Pioneer Electronics
103 Industrial Drive
Greensboro, North Carolina 27406
Tel: 919-273-4441

Ohio
Arrow Electronics
7620 McEwen Road
Centerville, Ohio 45459
Tel: 513-435-5563

Arrow Electronics
6238 Cochran Road
Solon, Ohio 44139
Tel: 216-248-3990 TWX: 810-427-9409

Hamilton/Avnet Electronics
954 Senate Drive
Dayton, Ohio 45459
Tel: 513-433-0610 TWX: 810-450-2531

Hamilton/Avnet Electronics
4588 Emery Industrial Parkway
Warrensville Heights, Ohio 44128
Tel: 216-831-3500
TWX: None — use 910-227-0060
(Regional Hq. in Chicago, Ill.)

Pioneer Electronics
4800 E. 131st Street
Cleveland, Ohio 44105
Tel: 216-587-3600

Pioneer Electronics
4433 Interpoint Blvd.
Dayton, Ohio 45424
Tel: 513-236-9900 TWX: 810-459-1622

Schweber Electronics
23880 Commerce Park Road
Beachwood, Ohio 44122
Tel: 216-464-2970 TWX: 810-427-9441

Oklahoma
Hall Mark Electronics
5460 S. 103rd East Avenue
Tulsa, Oklahoma 74145
Tel: 918-835-8458 TWX: 910-845-2290

Oregon
Hamilton/Avnet Electronics
6024 S.W. Jean Road
Building C, Suite 10
Lake Oswego, Oregon 97034
Tel: 503-635-8157

Pennsylvania
Arrow Electronics
650 Seco Road
Monroeville, Pennsylvania 15146
Tel: 412-856-7000

Pioneer Electronics
261 Gibraltar Road
Horsham, Pennsylvania 19044
Tel: 215-674-4000 TWX: 510-665-6778

Pioneer Electronics
259 Kappa Drive
Pittsburgh, Pennsylvania 15238
Tel: 412-782-2300 TWX: 710-795-3122

Schweber Electronics
101 Rock Road
Horsham, Pennsylvania 19044
Tel: 215-441-0600

Texas
Arrow Electronics
13715 Gamma Road
Dallas, Texas 75234
Tel: 214-386-7500 TWX: 910-860-5377

Arrow Electronics
10700 Corporate Drive, Suite 100
Stafford, Texas 77477
Tel: 713-491-4100 TWX: 910-880-4439

Hall Mark Electronics
12211 Technology Blvd.
Austin, Texas 78759
Tel: 512-258-8848

Hall Mark Electronics
11333 Page Mill Drive
Dallas, Texas 75243
Tel: 214-343-5000 TWX: 910-867-4721

Hall Mark Electronics
8000 Westglen
Houston, Texas 77063
Tel: 713-781-6100

Hamilton/Avnet Electronics
2401 Rutland Drive
Austin, Texas 78758
Tel: 512-837-8911 TWX: 910-874-1319

Hamilton/Avnet Electronics
8750 Westpark
Houston, Texas 77063
Tel: 713-780-1771
Telex: HAMAVLECB HOU 76-2589

Hamilton/Avnet Electronics
2111 W. Walnut Hill Lane
Irving, Texas 75062
Tel: 214-659-4111
TWX: 910-860-5929 HAVDLAS IRVG

Schweber Electronics, Inc.
4202 Beltway Drive
Dallas, Texas 75234
Tel: 214-661-5010 TWX: 910-860-5493

Schweber Electronics, Inc.
10625 Richmond, Suite 100
Houston, Texas 77042
Tel: 713-784-3600 TWX: 910-881-1109

Sterling Electronics
4201 Southwest Freeway
Houston, Texas 77027
Tel: 713-627-9800 TWX: 910-881-5042
Telex: STELECO HOUA 77-5299

Utah
Bell Industries
3639 West 2150 South
Salt Lake City, Utah 84120
Tel: 801-972-6969 TWX: 910-925-5686

Hamilton/Avnet Electronics
1585 West 2100 South
Salt Lake City, Utah 84119
Tel: 801-972-2800
TWX: None — use 910-379-6486
Regional Hq. in Mt. View, Ca.

Washington
Arrow Electronics
14320 N.E. 21st Street
Bellevue, Washington 98005
Tel: 206-643-4800 TWX: 910-443-3033

Hamilton/Avnet Electronics
14212 N.E. 21st Street
Bellevue, Washington 98005
Tel: 206-453-5844 TWX: 910-443-2449

Radar Electronic Co., Inc.
168 Western Avenue W.
Seattle, Washington 98119
Tel: 206-282-2511 TWX: 910-444-2052

Wyle Distribution Group
1750 132nd Avenue N.E.
Bellevue, Washington 98005
Tel: 206-453-8300 TWX: 910-444-1379

Wisconsin
Hall Mark Electronics
9657 South 20th Street
Oakcreek, Wisconsin 53154
Tel: 414-761-3000

Hamilton/Avnet Electronics
2975 South Moorland Road
New Berlin, Wisconsin 53151
Tel: 414-784-4510 TWX: 910-262-1182

Canada
Future Electronics Inc.
4800 Dufferin Street
Downsview, Ontario, M3H 5S8, Canada
Tel: 416-663-5563

Future Electronics Inc.
Baxter Center
1050 Baxter Road
Ottawa, Ontario, K2C 3P2, Canada
Tel: 613-820-8313

Future Electronics Inc.
237 Hymus Blvd.
Pointe Clare (Montreal), Quebec, H9R 5C7, Canada
Tel: 514-694-7710 TWX: 610-421-3251

Hamilton/Avnet Canada Ltd.
6845 Rexwood Road, Units 3-4-5
Mississauga, Ontario, L4V 1R2, Canada
Tel: 416-677-7432 TWX: 610-492-8867

Hamilton/Avnet Canada Ltd.
210 Colonnade Road
Nepean, Ontario, K2E 7L5, Canada
Tel: 613-226-1700

Hamilton/Avnet Canada Ltd.
2670 Sabourin Street
St. Laurent, Quebec, H4S 1M2, Canada
Tel: 514-331-6443 TWX: 610-421-3731

Semad Electronics Ltd.
620 Meloche Avenue
Dorval, Quebec, H9P 2P4, Canada
Tel: 604-299-8866 TWX: 610-422-3048

Semad Electronics Ltd.
105 Brisbane Avenue
Downsview, Ontario, M3J 2K6, Canada
Tel: 416-663-5670 TWX: 610-492-2510

Semad Electronics Ltd.
864 Lady Ellen Place
Ottawa, Ontario K1Z 5M2, Canada
Tel: 613-722-6571 TWX: 610-562-1923

Fairchild Semiconductor Sales Representatives United States and Canada

California
Magna Sales, Inc.
3333 Bowers Avenue, Suite 295
Santa Clara, California 95051
Tel: 408-727-8753 TWX: 910-338-0241

Colorado
Simpson Associates, Inc.
2552 Ridge Road
Littleton, Colorado 80120
Tel: 303-794-8381 TWX: 910-935-0719

Illinois
Micro Sales, Inc.
54 W. Seegers Road
Arlington Heights, Illinois 60005
Tel: 312-956-1000 TWX: 910-222-1833

Maryland
Delta III Associates
1000 Century Plaza, Suite 224
Columbia, Maryland 21044
Tel: 301-730-4700 TWX: 710-826-9654

Massachusetts
Spectrum Associates, Inc.
109 Highland Avenue
Needham, Massachusetts 02192
Tel: 617-444-8600 TWX: 710-325-6665

Minnesota
PSI Company
5315 West 74th Street
Edina, Minnesota 55435
Tel: 612-835-1777 TWX: 910-576-3483

Missouri
Micro Sales, Inc.
514 Earth City Plaza, Suite 314
Earth City, Missouri 63045
Tel: 314-739-7446

Nevada
Magna Sales, Inc.
4560 Wagon Wheel Road
Carson City, Nevada 89701
Tel: 702-883-1471

New York
Lorac Sales, Inc.
550 Old Country Road, Room 410
Hicksville, New York 11801
Tel: 516-681-8746 TWX: 510-224-6480

Tri-Tech Electronics, Inc.
3215 E. Main Street
Endwell, New York 13760
Tel: 607-754-1094 TWX: 510-252-0891

Tri-Tech Electronics, Inc.
590 Perinton Hills Office Park
Fairport, New York 14450
Tel: 716-223-5720 TWX: 510-253-6356

Tri-Tech Electronics, Inc.
6836 E. Genesee Street
Fayetteville, New York 13066
Tel: 315-446-2881 TWX: 710-541-0604

Tri-Tech Electronics, Inc.
19 Davis Avenue
Poughkeepsie, New York 12603
Tel: 914-473-3880 TWX: 510-253-6356

Ohio
The Lyons Corporation
4812 Frederick Road, Suite 101
Dayton, Ohio 45414
Tel: 513-278-0714 TWX: 810-459-1803

The Lyons Corporation
4615 West Streetsboro, Suite 203
Richfield, Ohio 44286
Tel: 216-659-9224 TWX: 810-459-1803

Oregon
Magna Sales, Inc.
8285 S.W. Nimbus Avenue, Suite 138
Beaverton, Oregon 97005
Tel: 503-641-7045 TWX: 910-467-8742

Utah
Simpson Associates, Inc.
7324 South 1300 East, Suite 350
Midvale, Utah 84047
Tel: 801-566-3691 TWX: 910-925-4031

Washington
Magna Sales, Inc.
Benaroya Business Park
Building 3, Suite 115
300 120th Avenue, N.E.
Bellevue, Washington 98004
Tel: 206-455-3190

Wisconsin
Larsen Associates
10855 West Potter Road
Wauwatosa, Wisconsin 53226
Tel: 414-258-0529 TWX: 910-262-3160

Canada
R.N. Longman Sales, Inc. - L.S.I.
1715 Meyerside Drive, Suite 1
Mississauga, Ontario, L5T 1C5 Canada
Tel: 416-677-8100 TWX: 610-492-8976

R.N. Longman Sales, Inc. - L.S.I.
16891 Hymus Blvd.
Kirkland, Quebec, H9H 3L4 Canada
Tel: 514-694-3911 TWX: 610-422-3028

Fairchild Semiconductor Sales Offices United States and Canada

Alabama
Huntsville Office
500 Wynn Drive, Suite 511
Huntsville, Alabama 35805
Tel: 205-837-8960

Arizona
Phoenix Office
2255 West Northern Road, Suite B112
Phoenix, Arizona 85021
Tel: 602-864-1000 TWX: 910-951-1544

California
Los Angeles Office*
Crocker Bank Bldg.
15760 Ventura Blvd., Suite 1027
Encino, California 91436
Tel: 213-990-9800 TWX: 910-495-1776

San Diego Office*
7867 Convoy Court, Suite 312
San Diego, California 92111
Tel: 714-279-7961 TWX: 910-335-1512

Santa Ana Office*
1570 Brookhollow Drive, Suite 206
Santa Ana, California 92705
Tel: 714-557-7350 TWX: 910-595-1109

Santa Clara Office*
3333 Bowers Avenue, Suite 299
Santa Clara, California 95051
Tel: 408-987-9530 TWX: 910-338-0241

Colorado
Denver Office
7200 East Hampden Avenue, Suite 206
Denver, Colorado 80224
Tel: 303-758-7924

Connecticut
Danbury Office
57 North Street, #206
Danbury, Connecticut 06810
Tel: 203-744-4010

Florida
Ft. Lauderdale Office
Executive Plaza, Suite 112
1001 Northwest 62nd Street
Ft. Lauderdale, Florida 33309
Tel: 305-771-0320 TWX: 510-955-4098

Orlando Office*
Crane's Roost Office Park
399 Whooping Loop
Altamonte Springs, Florida 32701
Tel: 305-834-7000 TWX: 810-850-0152

Georgia
Atlanta Sales Office
Interchange Park, Bldg. 2
4183 N.E. Expressway
Atlanta, Georgia 30340
Tel: 404-939-7683

Illinois
Itasca Office
500 Park Blvd., Suite 575
Itasca, Illinois 60143
Tel: 312-773-3300

Indiana
Ft. Wayne Office
2118 Inwood Drive, Suite 111
Ft. Wayne, Indiana 46815
Tel: 219-483-6453 TWX: 810-332-1507

Indianapolis Office
7202 N. Shadeland, Room 205
Castle Point
Indianapolis, Indiana 46250
Tel: 317-849-5412 TWX: 810-260-1793

Kansas
Kansas City Office
8600 West 110th Street, Suite 209
Overland Park, Kansas 66210
Tel: 913-649-3974

Maryland
Columbia Office
1000 Century Plaza, Suite 225
Columbia, Maryland 21044
Tel: 301-730-1510 TWX: 710-826-9654

Massachusetts
Framingham Office
5 Speen Street
Framingham, Massachusetts 01701
Tel: 617-872-4900 TWX: 710-380-0599

Michigan
Detroit Office*
21999 Farmington Road
Farmington Hills, Michigan 48024
Tel: 313-478-7400 TWX: 810-242-2973

Minnesota
Minneapolis Office*
4570 West 77th Street, Room 356
Minneapolis, Minnesota 55435
Tel: 612-835-3322 TWX: 910-576-2944

New Jersey
Wayne Office*
580 Valley Road
Wayne, New Jersey 07470
Tel: 201-696-7070 TWX: 710-988-5846

New Mexico
Albuquerque Office
North Building
2900 Louisiana N.E. South G2
Albuquerque, New Mexico 87110
Tel: 505-884-5601 TWX: 910-379-6435

New York
Fairport Office
815 Ayrault Road
Fairport, New York 14450
Tel: 716-223-7700

Melville Office
275 Broadhollow Road, Suite 219
Melville, New York 11747
Tel: 516-293-2900 TWX: 510-224-6480

Poughkeepsie Office
19 Davis Avenue
Poughkeepsie, New York 12603
Tel: 914-473-5730 TWX: 510-248-0030

North Carolina
Raleigh Office
1100 Navaho Drive, Suite 112
Raleigh, North Carolina 27609
Tel: 919-876-9643

Ohio
Dayton Office
5045 North Main Street, Suite 105
Dayton, Ohio 45414
Tel: 513-278-8278 TWX: 810-459-1803

Oklahoma
Tulsa Office
9810 East 42nd Street, Suite 127
Tulsa, Oklahoma 74145
Tel: 918-627-1591

Oregon
Portland Office
8285 S.W. Nimbus Avenue, Suite 138
Beaverton, Oregon 97005
Tel: 503-641-7871 TWX: 910-467-7842

Pennsylvania
Philadelphia Office*
2500 Office Center
2500 Maryland Road
Willow Grove, Pennsylvania 19090
Tel: 215-657-2711

Tennessee
Knoxville Office
Executive Square II
9051 Executive Park Drive, Suite 502
Knoxville, Tennessee 37923
Tel: 615-691-4011

Texas
Austin Office
9027 North Gate Blvd., Suite 124
Austin, Texas 78758
Tel: 512-837-8931

Dallas Office
1702 North Collins Street, Suite 101
Richardson, Texas 75081
Tel: 214-234-3391 TWX: 910-867-4757

Houston Office
9896 Bissonnet-2,, Suite 470
Houston, Texas 77036
Tel: 713-771-3547 TWX: 910-881-8278

Canada
Toronto Regional Office
1590 Matheson Blvd., Unit 26
Mississauga, Ontario L4W 1J1, Canada
Tel: 416-625-7070 TWX: 610-492-4311

* Field Application Engineer

Australlia
Fairchild Australia Pty Ltd.
Branch Office Third Floor
F.A.I. Insurance Building
619 Pacific Highway
St. Leonards 2065
New South Wales, Australia
Tel: (02) 439-5911
Telex: AA20053

Austria and Eastern Europe
Fairchild Electronics
A-1010 Wien
Schwedenplatz 2
Tel: 0222 635821 Telex: 75096

Benelux
Fairchild Semiconductor
Ruysdaelbaan 35
5613 Dx Eindhoven
The Netherlands
Tel: 00-31-40-446909 Telex: 00-1451024

Brazil
Fairchild Semiconductores Ltda.
Caixa Postal 30407
Rua Alagoas, 663
01242 Sao Paulo, Brazil
Tel: 66-9092 Telex: 011-23831
Cable: FAIRLEC

France
Fairchild Camera & Instrument S.A.
121, Avenue d'Italie
75013 Paris, France
Tel: 331-584-55 66
Telex: 0042 200614 or 260937

Germany
Fairchild Camera and Instrument GmBH
Daimlerstrasse 15
8046 Garching Hochbruck
Munich, Germany
Tel: (089) 320031 Telex: 52 4831 fair d

Fairchild Camera and Instrument GmBH
Oeltzenstrasse 15
3000 Hannover
W. Germany
Tel: 0511 17844 Telex: 09 22922

Fairchild Camera and Instrument GmBH
Poststrasse 37
7251 Leonberg
W. Germany
Tel: 07152 41026 Telex: 07 245711

Hong Kong
Fairchild Semiconductor (HK) Ltd.
135 Hoi Bun Road
Kwun Tong
Kowloon, Hong Kong
Tel: 3-440233 and 3-890271
Telex: HKG-531

Italy
Fairchild Semiconducttori, S.P.A.
Via Flamenia Vecchia 653
00191 Roma, Italy
Tel: 06 327 4006 Telex: 63046 (FAIR ROM

Fairchild Semiconducttori S.P.A.
Viale Corsica 7
20133 Milano, Italy
Tel: 296001-5 Telex: 843-330522

Japan
Fairchild Japan Corporation
Pola Bldg.
1-15-21, Shibuva
Shibuya-Ku, Tokyo 150, Japan
Tel: 03 400 8351 Telex: 242173

Fairchild Japan Corporation
Yotsubashi Chuo Bldg.
1-4-26, Shinmachi
Nishi-Ku, Osaka 550, Japan
Tel: 06-541-6138/9

Korea
Fairchild Semikor Ltd.
K2 219-6 Gari Bong Dong
Young Dung Po-Ku
Seoul 150-06, Korea
Tel: 85-0067 Telex: FAIRKOR 22705

mailing address
Central P.O. Box 2806

Mexico
Fairchild Mexicana S.A.
Blvd. Adolofo Lopez Mateos No. 163
Mexico 19, D.F.
Tel: 905-563-5411 Telex: 017-71-038

Scandinavia
Fairchild Semiconductor AB
Svartengsgatan 6
S-11620 Stockholm
Sweden
Tel: 8-449255 Telex: 17759

Singapore
Fairchild Semiconductor Pty. Ltd.
No. 11, Lorong 3
Toa Payoh
Singapore 12
Tel: 531-066 Telex: FAIRSIN-RS 21376

Taiwan
Fairchild Semiconductor Ltd.
Hsietsu Bldg., Room 502
47 Chung Shan North Road
Sec. 3 Taipei, Taiwan
Tel: 573205 thru 573207

United Kingdom
Fairchild Camera and Instrument Ltd.
Semiconductor Division
230 High Street
Potters Bar
Hertfordshire EN6 5BU
England
Tel: 0707 51111 Telex: 262835

Fairchild Semiconductor Ltd.
17 Victoria Street
Craigshill
Livingston
West Lothian, Scotland-EH54 5BG
Tel: Livingston 0506 32891 Telex: 72629

GEC-Fairchild Ltd.
Chester High Road
Neston
South Wirral L64 3UE
Cheshire, England
Tel: 051-336-3975 Telex: 629701

FAIRCHILD

A Schlumberger Company

Printed in U.S.A./2020-287-A-22-050 60M October, 1981