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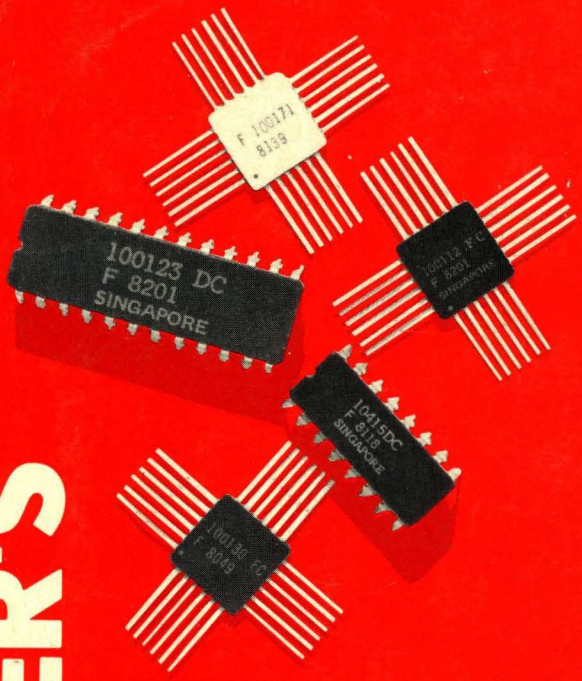
F100K ECL USER'S HANDBOOK



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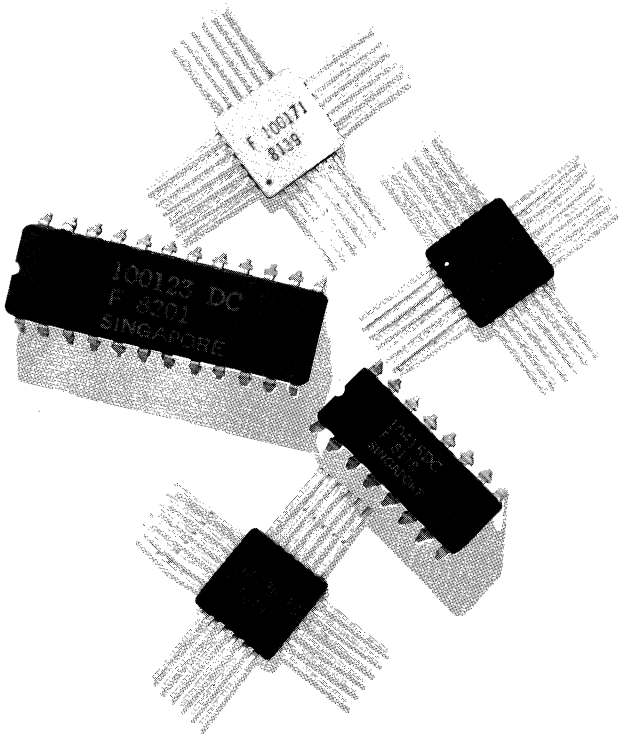

F100K ECL DATA BOOK

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Introduction

Fairchild's F100K ECL family has gained acceptance as the industry's performance leader. Before publishing this book, additional characterization data was taken that enabled the parametric specifications to be greatly expanded. DC parameters are now specified at 0°C to 85°C case temperature *and* over a −4.2 V to −4.8 V V_{EE} instead of only at −4.5 V. AC parameters are also specified over the same ranges of V_{EE} and temperature instead of only at −4.5 V and 25°C.

Future characterization efforts will be aimed at expanding the V_{EE} range and the temperature range.

For the user's convenience, the F10K memory products are also included in this databook.

Additionally, Fairchild's *F100K ECL User's Handbook* is available for more information concerning design considerations.

Chapter 1 Product Index, Selection Guide and Definitions
The Product Index is a numerical list of all device types contained in this book. The Selection Guide groups the products by function. Also included are definitions of commonly used terms.

Chapter 2 Family Overview
Discusses F100K design philosophy and actualization and summarizes the key F100K features and advantages in high speed systems.

Chapter 3 F100K Data Sheets
Contains a DC family data sheet for the F100K family and individual data sheets for the F100K devices.

Chapter 4 F10K Data Sheets
Contains a DC family data sheet for the F10K family and individual data sheets for the F10K memory devices.

Chapter 5 Ordering Information and Package Outlines

Chapter 6 Field Sales Offices, Distributor Locations

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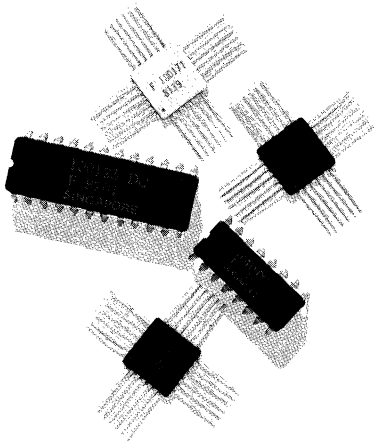

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AC Switching Parameters

f_{COUNT} (Count Frequency/Toggle Frequency/Operating Frequency) — The maximum repetition rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

t_{AA} (Address Access Time) — 50% points of address input pulse to data output pulse.

t_{ACS} (Chip Select Access Time) — 50% points of select pulse to data output pulse/leading edges.

t_h (Hold Time) — The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which the data to be recognized must be maintained at the input to ensure its continued recognition.

t_{PLH} (Propagation Delay Time) — The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} (Propagation Delay Time) — The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined HIGH level to the defined LOW level.

t_{RCS} (Chip Select Recovery Time) — Data output pulse/trailing edges.

t_S (Setup Time) — The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which the data to be recognized must be maintained at the input to ensure its recognition.

t_S (Release Time) — The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which the master set or reset must be released (inactive) to ensure valid data is recognized.

t_{TLH} (Transition Time, LOW to HIGH) — The time between two specified reference points on a waveform which is changing from LOW to HIGH.

t_{THL} (Transition Time, HIGH to LOW) — The time between two specified reference points on a waveform which is changing from HIGH to LOW.

t_W (Pulse Width) — The time between 50 percent amplitude points on the leading and trailing edges of a pulse.

t_W (Write Pulse Width) — 50% points of write enable input pulse.

t_{WHA} (Address Hold Time) — 50% points of address pulse to trailing edge of write enable pulse.

t_{WHCS} (Chip Select Hold Time) — 50% points of trailing edges of chip select pulse to write enable pulse.

t_{WHD} (Data Hold Time After Write) — 50% points of trailing edges of data input pulse to write enable pulse.

t_{WR} (Write Recovery Time) — 50% points of trailing edges of write enable pulse to data output pulse.

t_{WS} (Write Disable Time) — 50% points of leading edges of write enable pulse to data output pulse.

t_{WSA} (Address Setup Time) — 50% points of address pulse to leading edge of write enable pulse.

t_{WSCS} (Chip Select Setup Time) — 50% points of leading edges of chip select pulse to write enable pulse.

t_{WSD} (Data Setup Time Prior to Write) — 50% points of leading edges of data input pulse to write enable pulse.

TTL Loading

U.L. (Unit Loads) — One unit load in the HIGH state is defined as 40 μA; thus both the input HIGH leakage current, I_{IH}, and the output HIGH current sourcing capability, I_{OH}, are normalized to 40 μA. Similarly, one unit load in the LOW state is defined as 1.6 mA and both the input LOW current, I_{IL}, and the output LOW current sinking capability, I_{OL}, are normalized to 1.6 mA.

Currents

Positive current is defined as conventional current flow *into* a device lead. Negative current is defined as conventional current flow *out of* a device lead.

I_{EE} (Power Supply Current) — The current required by each device from the V_{EE} supply. This value represents only the internal current required by the specified device, and does not include the current required for loads or terminations.

I_{IH} (Input Current HIGH) — The current flowing into a device lead with the specified V_{IH} applied to the input. This value represents the worst case dc input load that a device presents to a driving element.

I_{IL} (Input Current LOW) — The current flowing into a device lead with the specified V_{IL} applied to the input.

Voltages

All voltage values are referenced to V_{CC} (or ground) which is the most positive potential in an ECL system.

V_{BB} (Bias Voltage) — The internally generated reference voltage which is used to set the input and output threshold levels.

V_{CC} (Circuit Ground) — This is the most positive potential in the ECL system and it is used as the reference level for other voltages.

V_{CS} (Current Source Voltage) — The internally generated potential used to control the level of the active current source.

V_{EE} (Power Supply Voltage) — This potential is the system power supply voltage and it is the most negative potential in the system.

V_{IH} (Input Voltage HIGH) — The range of input voltages that represents a logic HIGH level in the system.

$V_{IH(max)}$ — The most positive V_{IH}.

$V_{IH(min)}$ — The most negative V_{IH}. This value represents the guaranteed input HIGH threshold for the device.

V_{IL} (Input Voltage LOW) — The range of input voltages that represents a logic LOW level in the system.

$V_{IL(max)}$ — The most positive V_{IL}. This value represents the guaranteed input LOW threshold for the device.

$V_{IL(min)}$ — The most negative V_{IL}.

V_{OH} (Output Voltage HIGH) — The range of voltages at an output terminal with the specified output loading and with the inputs conditioned to establish a HIGH level at the output.

$V_{OH(max)}$ — The most positive V_{OH} under the specified input and loading conditions.

$V_{OH(min)}$ — The most negative V_{OH} under the specified input and loading conditions.

V_{OHC} — The output HIGH corner point or guaranteed HIGH threshold voltage with the inputs set to their respective threshold levels.

V_{OL} (Output Voltage LOW) — The range of voltages at an output terminal with the specified output loading and with the inputs conditioned to establish a LOW level at the output.

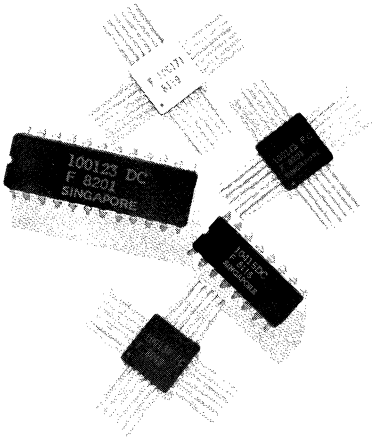
$V_{OL(max)}$ — The most positive V_{OL} under the specified input and loading conditions.

$V_{OL(min)}$ — The most negative V_{OL} under the specified input and loading conditions.

V_{OLC} — The output LOW corner point or guaranteed LOW threshold voltage with the inputs set to their respective threshold levels.

V_{NH} (HIGH Level Noise Margin) — Noise margin between the output HIGH level of a driving circuit and the input HIGH threshold level of its driven load. A conservative value for V_{NH} is the difference between V_{OHC} and $V_{IH(min)}$.

V_{NL} (LOW Level Noise Margin) — Noise margin between the output LOW level of a driving circuit and the input LOW threshold level of its driven load. A conservative value for V_{NL} is the difference between $V_{IL(max)}$ and V_{OLC}.



Chapter 2
Family Overview

- Introduction
- Design Philosophy
- Process Technology
- Compensation Network
- Characteristics
- System Aspects
- Features
- System Benefits
- Process Benefits
- Radiation Tolerance
- Packaging
- References

Introduction

Systems designers have found that Emitter Coupled Logic (ECL) circuits offer significant advantages to high-speed systems. These advantages include high switching rates with moderate power consumption, low propagation delays with moderate edge rates, and the ability to drive low impedance transmission lines.

The F100K ECL family is the realization of refinements made on ECL design to produce a family of logic components which are not only capable of providing ultimate performance for packaged SSI/MSI but which are easy to use and cost effective.

F100K ECL has been accepted as the standard subnanosecond logic family used in high-speed, next generation systems. The advance into complex LSI and gate arrays is fully supported by the F100K SSI/MSI parts.

Design Philosophy

F100K was designed to meet four key requirements: high speed at reduced power, high level of on-chip integration, flexible logic functions, and optimum I/O pin assignment.

Subnanosecond Gate Delays

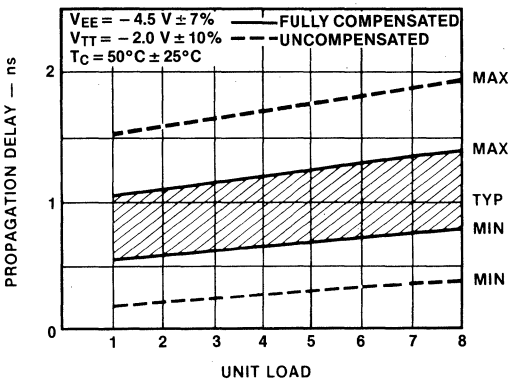
The subnanosecond internal gate delays of F100K are obtained by the use of ECL design techniques and the advanced Isoplanar II process. Many circuit approaches were carefully considered prior to selecting the optimum gate configuration for the F100K family. The emitter-follower current-switch (E^2CL) and current-mode logic (CML) gates were eliminated mainly because of poor capacitive drive and lack of output wired-OR capability; the CML gate has low noise margins. The 2-1/2D, EFL, DCTTL and hysteresis gates were eliminated due to the lack of simultaneous complementary outputs along with difficult temperature and voltage compensation characteristics that lead to the loss of system noise immunity.

The choice narrowed down to the current-switch emitter-follower ECL gate which offers the following characteristics:

- High fan-out capability
- Simultaneous complementary outputs
- Excellent ac characteristics
- Compatibility with existing ECL logic and memories
- Internal series gating capability
- Good noise immunity
- Amenable full compensation and extended temperature characteristics
- External wired-OR capability

In order to ease drive requirements all circuit inputs were designed to have similar loading characteristics; *i.e.,* buffers are incorporated where an input pin would normally drive more than one on-chip gate. The on-chip delay incurred by buffering is less than the system delay caused by an output which drives a capacitance of higher than three unit loads. Full compensation was selected for the F100K family to provide improved switching characteristics. Full compensation results in relatively constant signal levels and thresholds and in improved noise margins over temperature and voltage variations from chip to chip, and thus a tighter ac window in the system environment. A comparison of fully compensated ECL to conventional ECL shows a 2:1 improvement in system ac performance due solely to full compensation *(Figure 1-1).* And, the improved speed has been achieved at reduced power. This power reduction is accomplished by the use of advanced process technology that reduces parasitic capacitances and improves tolerances, by optimum circuit designs using series gating and collector and emitter dotting, and by designing for the use of a −4.5 V V_{EE} power supply. While a −5.2 V ± 10% power supply can be used to interface with 2 ns ECL families, F100K is only specified at a V_{EE} power supply of −4.2 V to −4.8 V.

Fig. 2-1 Comparison of Propagation Delays



High On-Chip Integration
Higher on-chip integration is made possible by using the 24-pin package to increase the number of signal pins by 62% over the conventional 16-pin package. The emphasis in F100K is to minimize the number of SSI functions and maximuze the use of MSI and LSI to reduce wiring delays and thus make more efficient use of the fast on-chip switching technology. Only 10 SSI functions are needed to serve the system needs presently requiring 25 functions in the ECL 10K family.

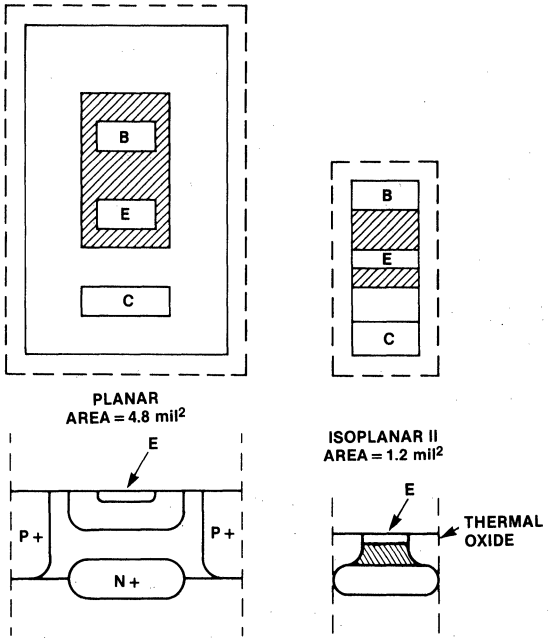
Flexibility and Pin Assignment
F100K was planned to minimize the total number of logic functions by increasing the flexibility of each function and by making use of more I/O pins. Since next-generation system performance and ease of system designs are major F100K goals, pin assignment is important and was planned to minimize crosstalk, noise coupling and feedthrough, to facilitate OR-ties and to ease power-bus routing. Some of the key considerations in selecting the F100K pin assignments were:

- Locate power pins in the center on opposite sides of the DIP package to ease system design and to provide low-inductance connections to the chip.
- Provide two V_{CC} pins, one for the internal circuit and one for the output buffers, to minimize noise coupling.
- Locate inverting outputs of logically independent gates adjacent to each other. This provides the ability to wire AND-OR-Invert functions with ease.
- Locate common pins such as common Reset and common Clock at pin number 22 and Address or control inputs at pins 19 and 20 for flatpaks. This is to maximize use of Computer Aided Design (CAD) for board layouts.
- When feasible, mode control pins are used to create multipurpose devices.

Process Technology
The F100K family is fabricated using the advanced Isoplanar II process, which provides transistors with very-high, well-controlled switching speeds, extremely small parasitic capacitances and f_T in excess of 5 GHz.

The technology can best be described by comparing the integrated circuit transistor structures of the conventional Planar process and that of the Isoplanar II process *(Figure 1-2)*. The top view shows the area needed for each structure; the dashed area is the center of the isolation area.

Fig. 2-2 Transistor Structures



In the Isoplanar process, a thick oxide is selectively grown between devices, instead of the P^+ region which is present in the Planar process. Since this oxide needs no separation from the base-collector regions, a substantial reduction in device and chip size can be realized. The base and emitter ends terminate in the oxide wall; therefore, the masks can overlap into the isolation oxide. This overlap feature means that base and emitter masking does not have to meet the extremely close tolerances that might otherwise be necessary, and standard photolithographic processes can be used.

The "walled emitter" structure allows over a 70% reduction of the transistor silicon area compared to that of a conventional Planar transistor. For a given emitter size, the collector-base area is also reduced by more than 60%. The reduced junction areas result in corresponding reductions in collector-base and collector-substrate capacitances, thereby allowing higher speeds.

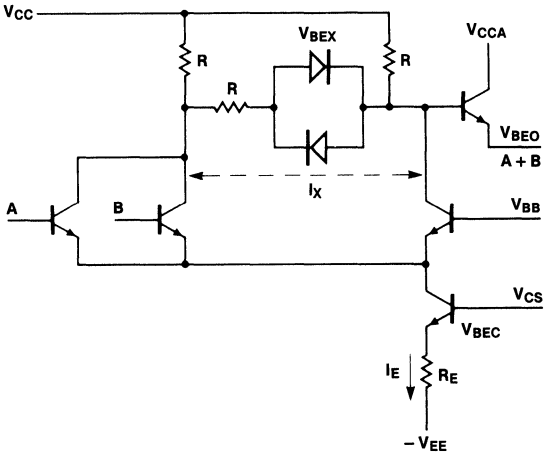
Since the active transistor area is only under the emitter, all capacitance and resistance values outside this area are reduced. Parasitic values are further reduced by taking advantage of the masking alignment latitude resulting from the self-aligning nature of the structure.

As is the case with other modern LSI processes, the shallower diffusions and thinner oxides make ECL devices more susceptible to damage from electrostatic discharge than are devices of earlier TTL families. Users should take the usual precautions when handling ECL devices: avoid placing them on non-conductive plastic surfaces or in plastic bags, make sure test equipment and fixtures are grounded, individuals should be grounded before handling the devices, etc.

Compensation Network

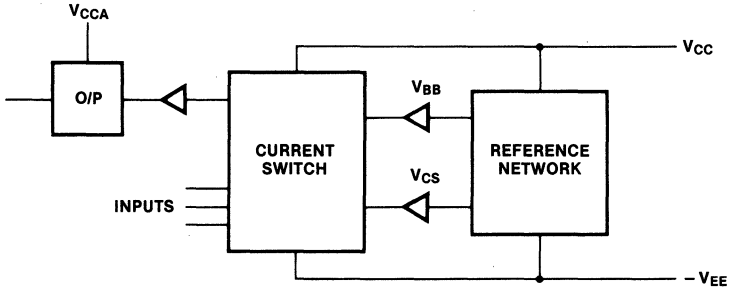
The heart of F100K is fully compensated ECL.[1] The basic gate consists of three blocks — the current switch, the output emitter-followers, and the reference or bias network *(Figure 1-3).* The current switch allows both conjunctive and disjunctive logic. The output emitter-followers provide high drive capability through impedance transformation and allows for increased logic swing. The bias network sets dc thresholds and current-source bias voltages. Temperature compensation at the gate output is achieved by incorporating a cross-connect branch between the complementary collector nodes of the current switch and driving the current source with a temperature insensitive bias network[2] *(Figure 1-4).*

Fig. 2-4 Temperature Compensation



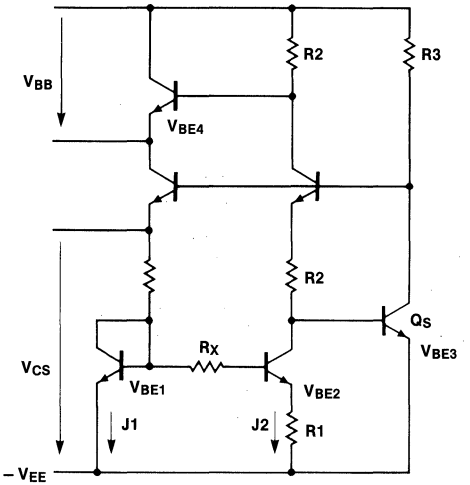
As junction temperature increases and the forward base-emitter voltage of the output emitter-follower decreases, the collector node of the current switch must become more negative. Since the current-source bias voltage, V_{CS}, is independent of temperature, the switch current increases with temperature due to the temperature dependence of V_{BEC}. The combination of temperature controlled current, I_E, and the cross-connect branch current, I_X, forces the proper temperature coefficient at the collector node of the current switch to null out the V_{BEO} tracking coefficient.[3]

Fig. 2-3 ECL Gate



The schematic for the reference network displays a V_{BE1} amplifier in the bottom left corner *(Figure 1-5)*. Two base-emitter junctions are operated at different current densities, J1 and J2. The resulting voltage difference, V_{BE1} minus V_{BE2}, appears across R1 and is amplified by the ratio R2/R1. Note that R2 is used twice, once to generate V_{CS} and once to generate V_{BB}. The different current densities, J1 and J2, result in a positive temperature tracking coefficient across R2, which cancels the negative diode-tracking coefficient of V_{BE3} and V_{BE4}. The V_{CS} and the V_{BB} thus generated are temperature insensitive at the extrapolated bandgap voltage of silicon[1,2] (approximately 1300 mV).[4] R_X in the V_{BE} amplifier compensates for process variations of β and ΔV_{BE}.[5] Voltage regulation is achieved through a shunt regulator shown at the right side of the schematic.

Fig. 2-5 Reference Network



Characteristics

F100K compatibility with existing ECL logic families and memories permits direct interface with slower logic families and ensures immediate memory availability. The typical logic swing is 800 mV *(Figure 1-6)* and all voltage levels are specified with a 50 Ω load to –2 V at all outputs to provide transmission line drive capability. However, the inherently low output impedance *(Figure 1-7)* and maximum specified output current, 50 mA, make 25 Ω drive possible at any or all outputs. Alternately, of course, higher termination impedances or other termination schemes are also useful.

Fig. 2-6 Transfer Characteristics

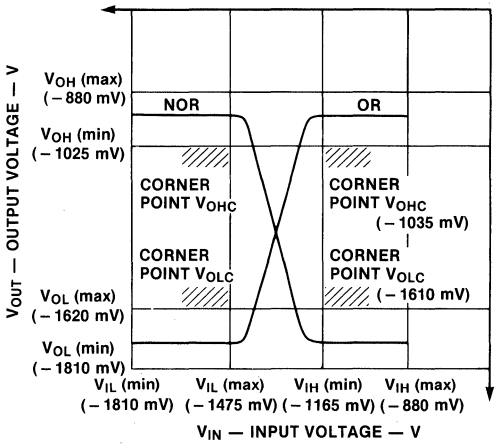
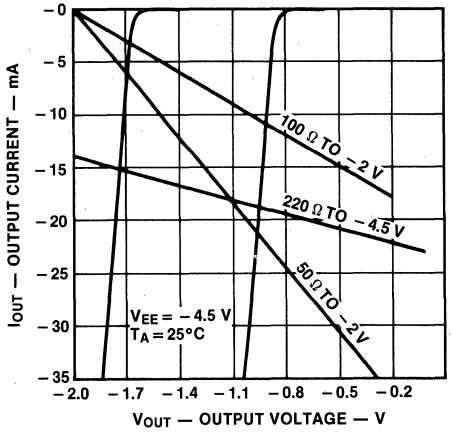
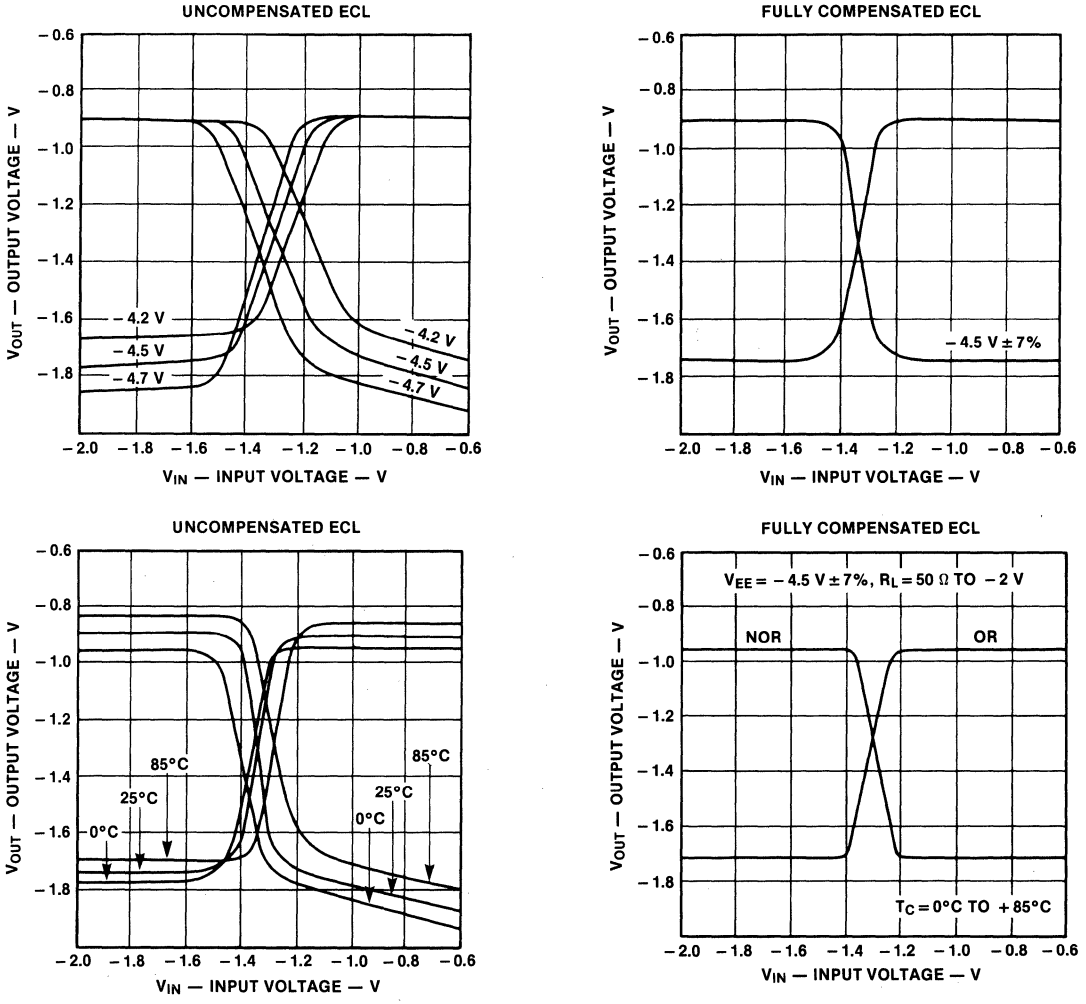


Fig. 2-7 Output Characteristic vs Output Terminations



F100K exhibits relatively constant output levels and thresholds over the 0°C to +85°C specified temperature range and –4.2 V to –4.8 V specified voltage range *(Figure 1-8)*. V_{EE} power supply current is also constant over the specified voltage range *(Figure 1-9)*; therefore:

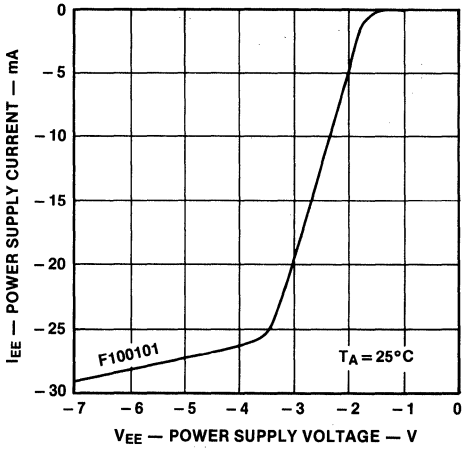
Fig. 2-8 Transfer Characteristics



- Propagation delay is relatively constant versus power supply voltage variations thus tightening the ac window.
- Power dissipation is a linear function of the supply voltage, reducing worst-case power consumption.

The typical propagation delay of an SSI gate function driving a 50 Ω transmission line is 0.75 ns, including package, with a power dissipation of 40 mW resulting in a speed-power product of 3 pJ. For optimized MSI functions, the internal gates can dissipate < 10 mW with average propagation delay of < 0.5 ns, giving a power-speed product of < 5 pJ.

Fig. 2-9 Change In I_{EE} vs Change In V_{EE}



F100K has a tighter ac window over the wide range of environmental conditions; thus, the system timing requirements are eased and maximum system clock rates are increased. At the sacrifice of ac performance, the small-signal input impedance was conservatively designed to be positive-real over the frequency range encountered by any circuit input. This provides adequate damping to insure ac stability within the system.

System Aspects

F100K provides high-density digital functions that outperform all other families on the market today. How does this increased circuit performance and higher on-chip density improve system performance?

Propagation delay and transition times vary (ac windows) when functions are operated at the extremes of the specified environmental ranges. With F100K, these variations are reduced and more predictable system timing is achieved. For synchronous machines and very high speed asynchronous systems, timing and its predictability are of utmost importance. Due to F100K constant supply current versus power supply voltage and because of nearly constant levels and thresholds with respect to temperature, voltage variations and gradients, speed skews are minimized.

Not only timing but also maximum system clock rate is affected by the tighter ac window. Thus, with F100K the system designer can use a higher speed value in his worst-case calculations. This can be translated into higher possible system clock rates. Therefore, a machine can perform at up to twice the frequency, solely due to the F100K compensation features. Noise immunity will be of utmost importance in next generation computers, since much of the noise generated within the system is inversely proportional to the switching transition time of the circuits. The F100K transition time is typically 0.7 ns as compared to 2.0 ns in other ECL families and should therefore increase system crosstalk by the same ratio.

F100K combats the increased system noise by maintaining a virtually invariant noise immunity with variations and gradients in power supply voltage, ambient and junction temperatures. The variation in junction temperatures is much larger than in earlier computer systems because of the mixture of LSI and SSI functions on the same boards.

Features

F100K ECL logic components are designed to be used in high-speed, low-noise systems and offer significant advantages over other logic families. Some of the important features and advantages are summarized below:

Low Propagation Delay

F100K ECL features gate delays which are typically 0.75 ns (750 picoseconds) with counters, registers and flip-flops operating in the 400 - 500 MHz range. When compared to other logic families such as Schottky TTL or slower ECL families, system performance can be doubled or tripled.

Moderate Edge Rates

Because of the nature of current mode switching which uses differential comparison techniques and avoids transistor storage delays, rise times can be controlled by internal time constants without sacrificing throughput delays. Slower rise times minimize ringing and reflections on interconnection wiring and simplify physical design. The typical edge rate for F100K ECL is 1 V/ns, only about 80% of the edge rate of Schottky TTL. It can be shown that for ECL circuits, the natural rise and fall times are approximately equal to the propagation delay. This relationship is considered optimum for use in high-speed systems.

Wired-OR Capability
ECL outputs can be wired together where wiring rules permit, to form the positive logic-OR function, thus achieving an extra level of gating at no parts count expense. Data bussing and party line operations are facilitated by this feature.

Complementary Outputs
A majority of F100K ECL logic elements have complementary outputs, providing numerous opportunities for reduction of package count and power consumption when mechanizing logic equations. Further, the system incurs no extra penalty in time delay since the complementary ECL outputs switch simultaneously.

A significant advantage to complementary outputs is that, since both the true and complement logic functions are available, I_{CC} imbalance can be minimized either by using both outputs in the design or merely terminating unused outputs. In this way, the constant current characteristic of ECL is not compromised and power supply noise is minimized.

Low Output Impedance, High Current Capacity
As operating speeds are increased to achieve the higher performance levels demanded of digital systems, ordinary wiring begins to exhibit distributed parameter characteristics, as opposed to a lumped capacitance nature at low speeds.

Characteristic impedances of normal wiring and printed circuit interconnections generally fall in the 50 to 250 Ω range. With these low impedance lines and fast transitions, the signals are attenuated by the voltage divider action between the circuit output impedance and the characteristic impedance of the interconnection.

Voltage mode circuits have a HIGH state output impedance of from 50 to 150 Ω and thus exhibit an output *stepped* characteristic, first reaching about 50% of final value and later reaching the final value in another *step.* F100K ECL output impedances under 10 Ω insure a complete, full valued, signal into a transmission line. Also, F100K ECL outputs are specified to drive a 50 Ω load (some devices are specified to drive a 25 Ω load). Outputs are capable of supplying 50 mA or more and can thus support the quiescent current required for passive terminations.

Convenient Data Transmission
The complementary high-current outputs of F100K ECL elements are well suited for driving twisted pair or other balanced lines in a differential mode, thereby enhancing field cancellation and minimizing crosstalk between subsystems.

High Common-Mode Noise Rejection
Differential line receivers provide common-mode noise rejection of 1 V or more for induced and ground noise. Differential receiving requires less signal swing than single ended and thus allows more reliable interpretation of low signal swings.

Constant Supply Current
The supply current drain of F100K ECL elements is governed by one or more internal constant current sources supplying operating current for differential switches and level shifting networks. Since the current drain is the same regardless of the state of the switches, F100K ECL circuits present constant current loads to power supplies *(see Complementary Outputs).*

Low Power Loss in Stray Capacitance
Energy is consumed each time a capacitor is charged or discharged so the energy loss rate, or power, goes up with switching frequency. Since the energy stored in a capacitor is proportional to the square of the voltage and F100K ECL signal swings are four to five times less than those of TTL, power loss in stray capacitance may be an order of magnitude less than that of TTL.

Low Noise Generation
In ECL systems, power supply lines are not subjected to the large current spikes common with TTL designs. Inherently, ECL is a constant current family without the totem-pole structures found in TTL circuits which generate the large current spikes. Since ECL voltage swings are much smaller than TTL, the current spikes caused by charging and discharging stray capacitances are much smaller with ECL than with TTL of comparable edge rates.

Low Crosstalk
Induced noise signals are proportional to signal swings and edge rates. The lower swing and slower edge rate of F100K ECL result in low levels of crosstalk.

System Benefits

The Fairchild F100K family offers improvements over other ECL families such as voltage and temperature compensation, higher integration levels, improved packaging, planned pinouts, lower propagation delay and more complementary outputs. These improvements cause measurable advantages to accrue to the design(er) of high-performance systems.

Easier Engineering

Designers have increased confidence that designs realized in F100K will operate with good margins over voltage and temperature variations in prototypes, production models and field installations. Less effort need be expended doing detailed voltage and temperature calculations and testing. With noncompensated ECL, noise margins cannot be guaranteed unless both the receiving and transmitting circuit operate at the same temperature and V_{EE}. This can cause a problem when attempting to transfer a breadboard or prototype system to production.

Since output swings and input thresholds remain almost constant over temperature and V_{EE} variations, complex control systems for power supply levels and more-than-adequate cooling are not necessary with F100K. This results in a more economical and better operating system.

Circuit Design

F100K ECL benefits from sound, well-engineered circuit designs. All input pins exhibit *positive/real* input impedance to eliminate system oscillations. Input buffering is used to reduce loads on lines which drive multiple internal gates.

High Performance

The regulation and control of dc and ac parameters achieved by F100K ECL assures that signal timing and propagation delays in critical paths are relatively insensitive to changes or gradients of temperature and supply voltage. Guardbands can be narrower, yet provide a higher degree of confidence due to the elimination of skew between output levels at one location and input thresholds at another.

The consistency of response and security of noise margins permit operation at higher clock rates and thus increase system performance.

Easier Debugging

With F100K, debugging of systems can proceed more rapidly than with uncompensated ECL. When a cabinet or enclosure is opened for access in debugging, the resultant change in thermal conditions has almost no effect on F100K signal swings, propagation delays, edge rates or noise margins.

Flexibility

F100K is designed to operate at −4.5 V for reduced power dissipation. If compatibility with other ECL families is a requirement, F100K will operate between −4.2 and −5.7 V due to the unique voltage compensation features. When operating at voltages other than −4.5 V, ac and dc parameters will vary slightly from specified values.

Fan-In/Fan-Out

All F100K ECL outputs are specified to drive 50 Ω transmission lines; this makes them suitable for driving very-high fan-out loads. In addition, some F100K outputs are specified to drive 25 Ω lines, which would be the case if a 50 Ω party-line bus terminated at both ends were being driven.

System Design

F100K ECL was designed to be the ultimate standard packaged IC logic family. System design constraints were considered and the F100K family was designed for overall ease of system design and use while making the maximum use of the very fast propagation delays available.

Process Benefits

F100K ECL SSI/MSI parts are made using the Isoplanar II process. This process makes possible subnanosecond logic delays and very tightly controlled switching characteristics.

Expansion of the F100K family will take place by moving into LSI functions of 500 to 4000 gates. The evolution of the Isoplanar II process will enable such growth and give much increased performance.

It is by moving into LSI that subnanosecond delays can be fully utilized and overall system performance increased with decreased power consumption and parts count.

Radiation Tolerance

F100K ECL manufactured using Isoplanar II processes is one of the most radiation-hard integrated circuit families in production. Radiation hardness can extend system lifetimes up to 50% in some applications requiring radiation tolerance. *(Reference Table 1.)*

Packaging

The initial package selected for the F100K is a 24-pin Flatpak, 0.375 inches square, with leads on 50-mil centers, 6 leads per side. This package was chosen because it offers minimum performance degradations of circuit and system and uses a somewhat conventional packaging technology. More common packaging such as the dual in-line packages, while available, do not provide optimum performance due to the loss in speed entering and leaving the package as well as a decrease in system density. With the F100K packaging technique and higher chip complexities within the family, the system density is two to three times higher than that possible with other available ECL families.

Table 1 Summary of Semiconductor Vulnerability Assessment

Radiation Environment	Bipolar Trans. & J-FET. Discretes	SCR	TTL	LSTTL	Analog IC	CMOS	NMOS	LED	ISO II ECL
Neutrons n/cm^2	10^{10}-10^{12}	10^{10}-10^{12}	10^{14}	10^{14}	10^{13}	10^{15}	10^{15}	10^{13}	$> 10^{15}$
Ionizing Total Dose Rads (Si)	$> 10^4$	10^4	10^6	10^6	5×10^4 10^5	10^3 10^4	10^3	$> 10^5$	10^7
Transient Dose Rate Rads (Si)/seconds (Upset or Saturation)		10^3	10^7	5×10^7	10^6	10^7	10^5		$> 10^8$
Transient Dose Rate Rads (Si)/seconds (Survival)	10^{10}	10^{10}	$> 10^{10}$	$> 10^{10}$	$> 10^{10}$	10^9	10^{10}	$> 10^{10}$	$> 10^{11}$
Dormant Total Dose (Zero Bias)	$> 10^4$	10^4	10^6	10^6	10^5	10^6	10^4	$> 10^5$	$> 10^7$

References

1. H.H. Muller, W.K. Owens, and P.W.J. Verhofstadt, "Fully Compensated Emitter-Coupled Logic: Eliminating the Drawbacks of Conventional ECL", *IEEE Journal of Solid-State Circuits,* October 1973, pp. 362-367.
2. R.R. Marley, "On-chip Temperature Compensation for ECL", *Electronic Products,* March 1, 1971.
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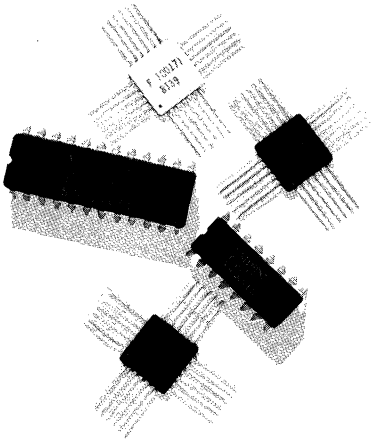
4. R.J. Widlar, "New Developments in IC Voltage Regulators", *ISSCC Digital Technical Papers,* February 1970, pp. 157-159.
5. W.K. Owens, "Temperature Compensated Voltage Regulator Having Beta Compensating Means", United States Patent, No. 3,731,648, December 25, 1973.



F100K DC Family Specification

DC characteristics for the F100K series family parametric limits listed below are guaranteed for the entire F100K ECL family unless specified on the individual data sheet.

Absolute Maximum Ratings: Above which the useful life may be impaired[1]

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	0°C to +150°C
Case Temperature Under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	−50 mA
Operating Range[2]	−5.7 V to −4.2 V

DC Characteristics: V_{EE} = −4.5 V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, Note 3

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions[4]	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mv	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(min)}$	

DC Characteristics: V_{EE} = −4.2 V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, Note 3

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions[4]	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1810		−1605	mV		
V_{OHC}	Output HIGH Voltage	−1030			mv	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage			−1595	mV		
V_{IH}	Input HIGH Voltage	−1150		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(min)}$	

DC Characteristics: V_{EE} = −4.8 V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, Note 3

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions[4]	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1830		−1620	mV		
V_{OHC}	Output HIGH Voltage	−1045			mv	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(min)}$	

1. Unless specified otherwise on individual data sheet.
2. Parametric values specified at −4.2 V to −4.8 V.
3. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

F100101
Triple 5-Input OR/NOR Gate

F100K ECL Product

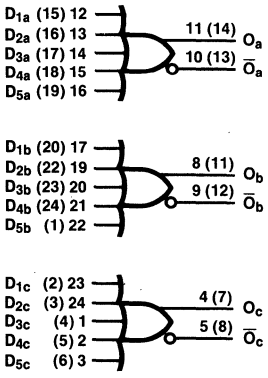
Description

The F100101 is a monolithic triple 5-input OR/NOR gate. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Pin Names

D_{na}, D_{nb}, D_{nc}	Data Inputs
O_a, O_b, O_c	Data Outputs
$\overline{O}_a$, $\overline{O}_b$, $\overline{O}_c$	Complementary Data Outputs

Logic Symbol



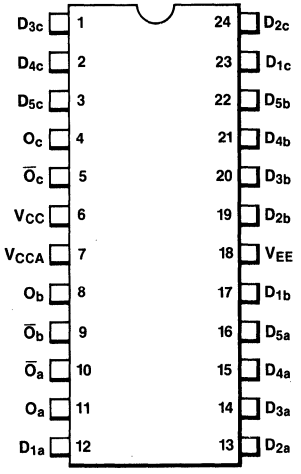
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

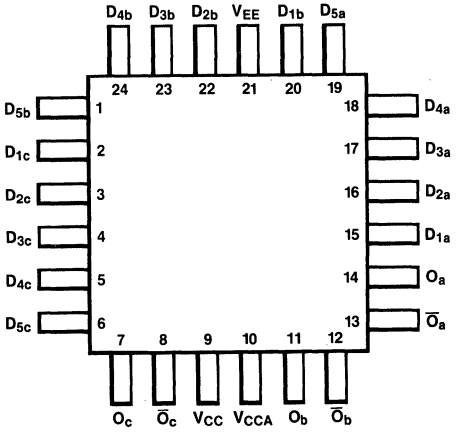
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Connection Diagrams

24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			350	μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	−38	−26	−18	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

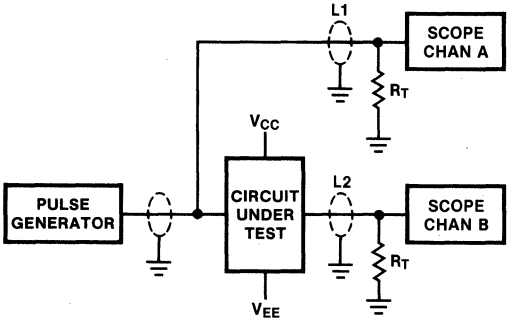
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.50	1.15	0.50	1.15	0.55	1.30	ns	*Figures 1 and 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.30	0.45	1.20	0.45	1.20	ns	

Flatpak AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.50	0.95	0.50	0.95	0.55	1.10	ns	*Figures 1 and 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.20	0.45	1.10	0.45	1.10	ns	

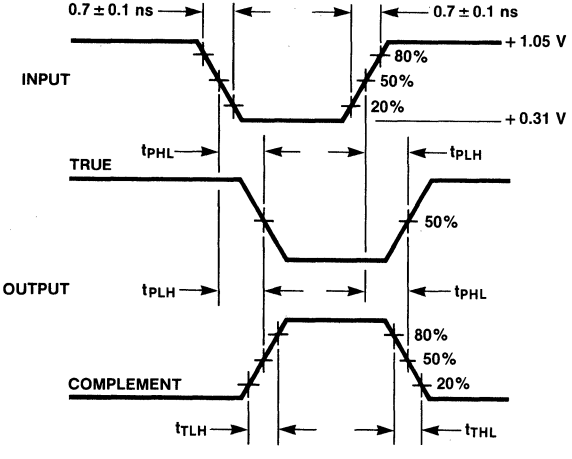
*See Family Characteristics for other dc specifications.

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = −2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Fig. 2 Propagation Delay and Transition Times



F100102
Quint 2-Input OR/NOR Gate

F100K ECL Product

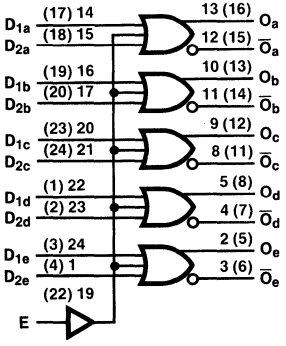
Description

The F100102 is a monolithic quint 2-input OR/NOR gate with common enable. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Pin Names

D_{na}–D_{ne}	Data Inputs
E	Enable Input
O_a–O_e	Data Outputs
$\overline{O}_a$–$\overline{O}_e$	Complementary Data Outputs

Logic Symbol



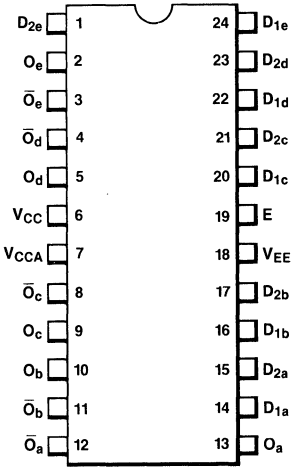
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

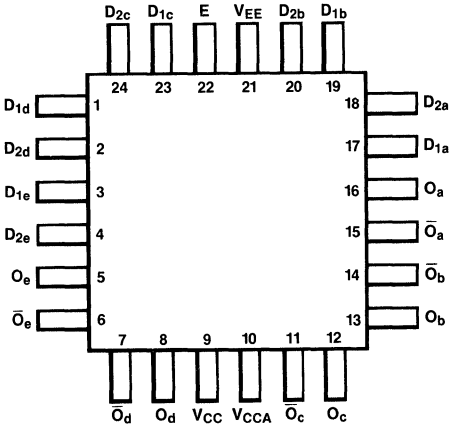
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Connection Diagrams

24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current Data Enable			 350 300	 μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−80	−55	−38	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

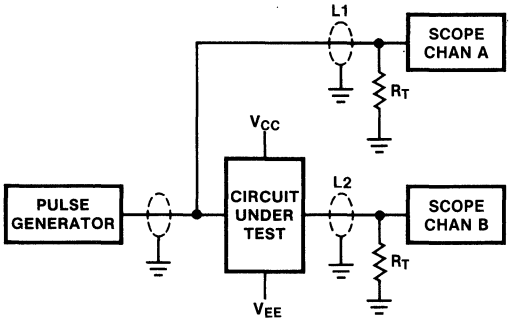
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.35	0.45	1.15	0.45	1.40	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.95	2.15	0.95	2.15	0.95	2.20	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.30	0.45	1.20	0.45	1.20	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.15	0.45	0.95	0.45	1.20	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.95	1.95	0.95	1.95	0.95	2.00	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.20	0.45	1.10	0.45	1.10	ns	

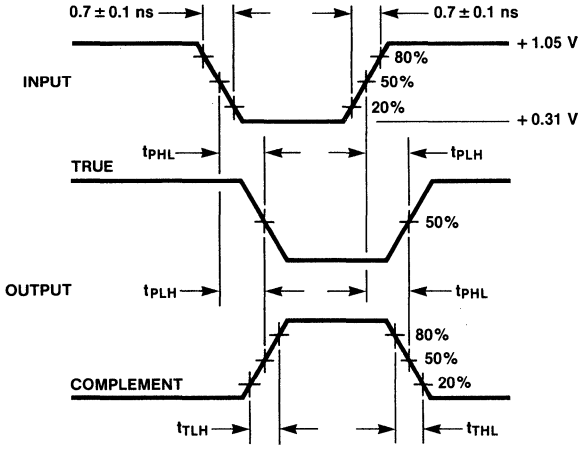
*See Family Characteristics for other dc specifications.

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Fig. 2 Propagation Delay and Transition Times



F100107
Quint Exclusive OR/NOR Gate

F100K ECL Product

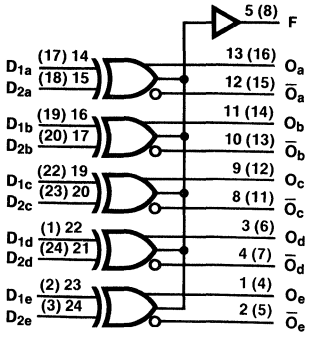
Description

The F100107 is a monolithic quint exclusive-OR/NOR gate. The Function output is the wire-OR of all five exclusive-OR outputs: $F = (D_{1a} \oplus D_{2a}) + (D_{1b} \oplus D_{2b}) + (D_{1c} \oplus D_{2c}) + (D_{1d} \oplus D_{2d}) + (D_{1e} \oplus D_{2e})$.

Pin Names

D_{na}–D_{ne}	Data Inputs
F	Function Input
O_a–O_e	Data Outputs
$\overline{O}_a$–$\overline{O}_e$	Complementary Data Outputs

Logic Symbol



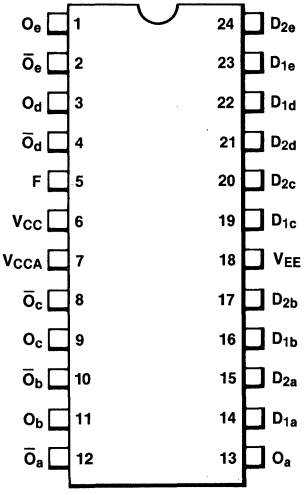
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

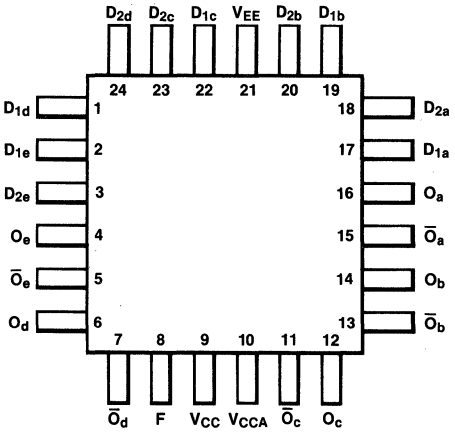
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Connection Diagrams

24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current D_{2a} - D_{2e} D_{1a} - D_{1e}			 250 350	 μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−96	−66	−46	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

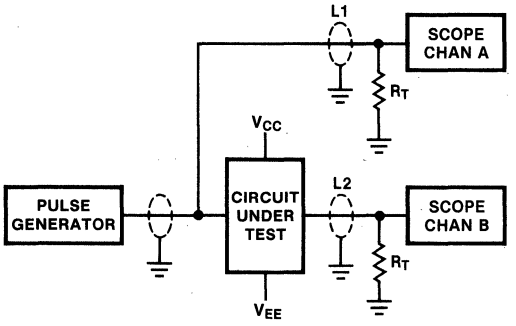
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay D_{2a}-D_{2e} to O, $\overline{O}$	0.55	1.90	0.55	1.80	0.55	1.90	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay D_{1a}-D_{1e} to O, $\overline{O}$	0.55	1.70	0.55	1.60	0.55	1.70	ns	
t_{PLH} t_{PHL}	Propagation Delay Data to F	1.15	2.75	1.15	2.75	1.15	3.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.65	0.45	1.80	ns	

Flatpak AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay D_{2a}-D_{2e} to O, $\overline{O}$	0.55	1.70	0.55	1.60	0.55	1.70	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay D_{1a}-D_{1e} to O, $\overline{O}$	0.55	1.50	0.55	1.40	0.55	1.50	ns	
t_{PLH} t_{PHL}	Propagation Delay Data to F	1.15	2.55	1.15	2.55	1.15	2.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.55	0.45	1.70	ns	

*See Family Characteristics for other dc specifications.

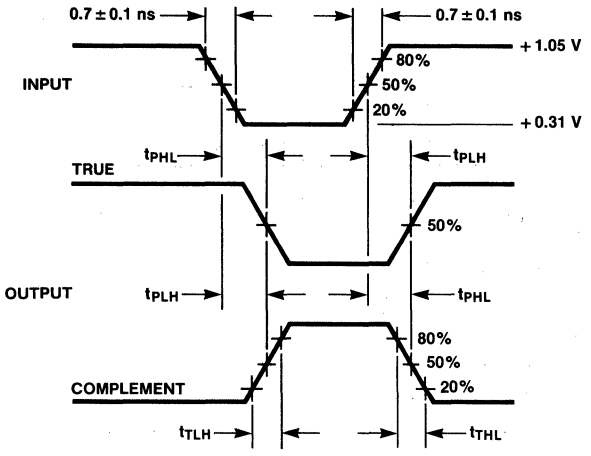
Fig. 1 AC Test Circuit



Notes

V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Fig. 2 Propagation Delay and Transition Times



F100112
Quad Driver

F100K ECL Product

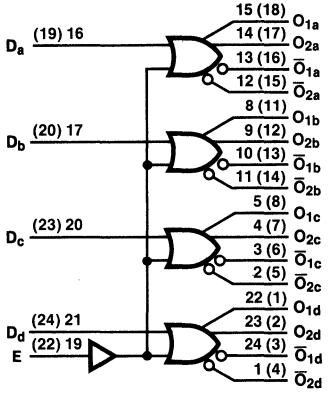
Description

The F100112 is a monolithic quad driver with two OR and two NOR outputs and common enable. The common input is buffered to minimize input loading. If the D inputs are not used the Enable can be used to drive sixteen 50 Ω lines. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Pin Names

D_a–D_d	Data Inputs
E	Enable Input
O_{na}–O_{nd}	Data Outputs
$\overline{O}_{na}$–$\overline{O}_{nd}$	Complementary Data Outputs

Logic Symbol



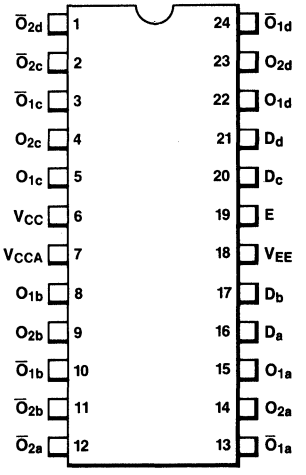
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

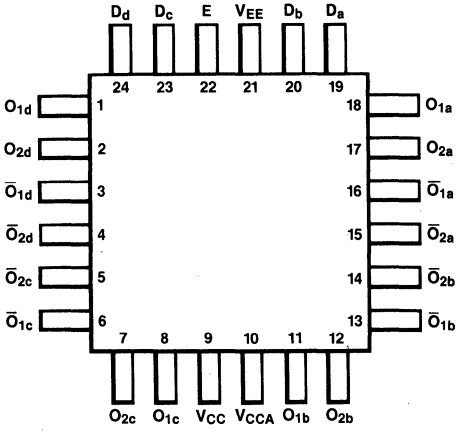
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Connection Diagrams

24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current Data Enable			 550 450	 μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	−106	−73	−51	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

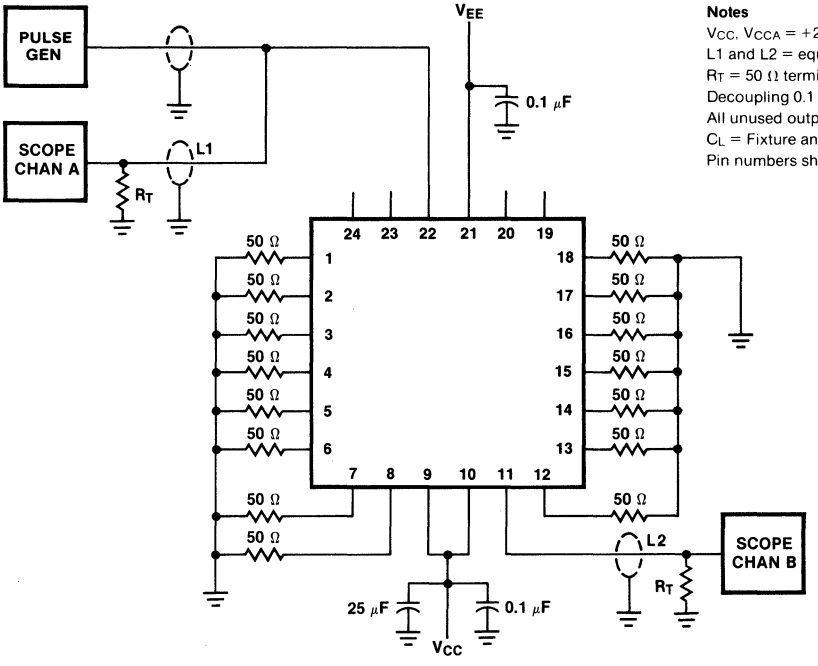
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Condition**
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.55	1.50	0.55	1.40	0.45	1.60	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.65	2.00	0.65	1.90	0.65	2.00	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.50	0.45	1.60	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Condition**
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.55	1.30	0.55	1.20	0.45	1.40	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.65	1.80	0.65	1.70	0.65	1.80	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.50	ns	

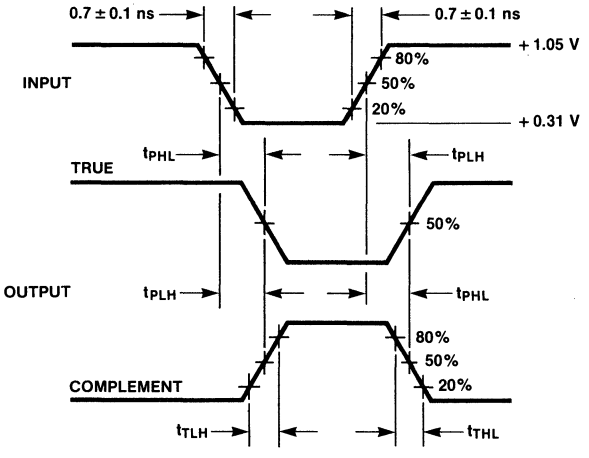
*See Family Characteristics for other dc specifications.

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = −2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Fig. 2 Propagation Delay and Transition Times



F100113
Quad Driver

F100K ECL Product

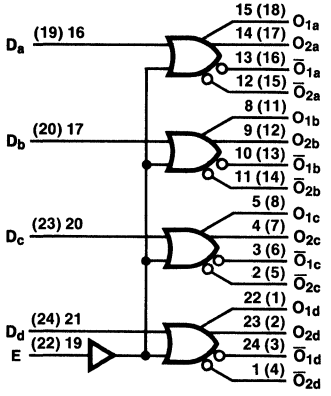
Description

The F100113 is a monolithic quad driver with two OR and two NOR outputs and common enable. The common input is buffered to minimize input loading. If the D inputs are not used the Enable can be used to drive sixteen 50 Ω lines. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Pin Names

D_a - D_d	Data Inputs
E	Enable Input
O_{na} - O_{nd}	Data Outputs
$\overline{O}_{na}$ - $\overline{O}_{nd}$	Complementary Data Outputs

Logic Symbol



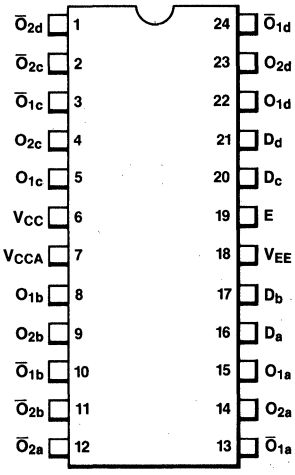
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

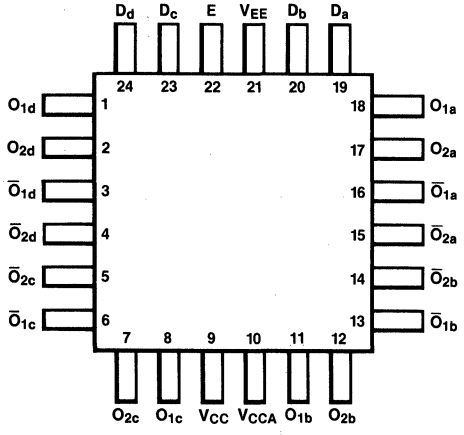
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Connection Diagrams

24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current Data Enable			 550 350	 μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−116	−80	−56	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

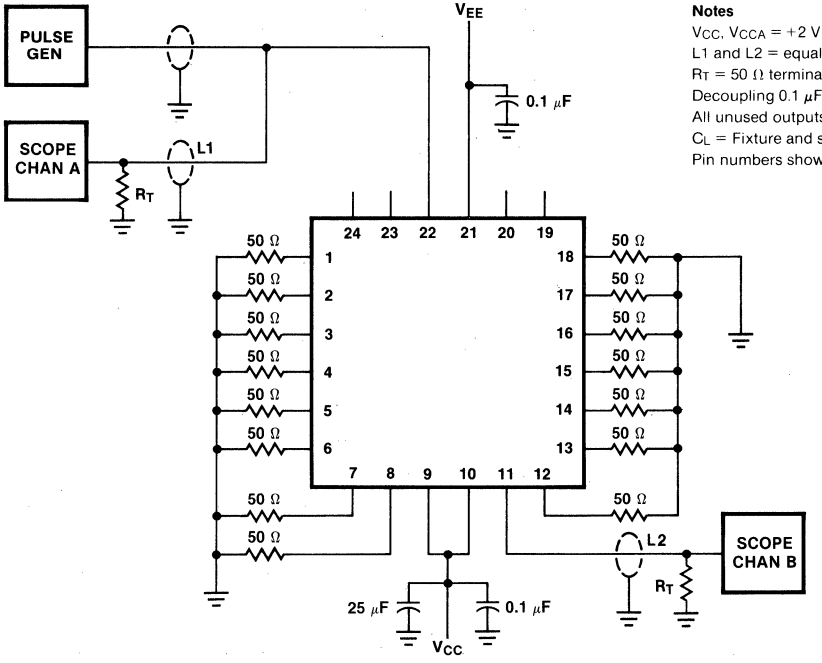
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Condition**
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.40	0.45	1.35	0.45	1.40	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.55	1.90	0.55	1.90	0.55	1.90	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.50	0.45	1.60	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Condition**
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.20	0.45	1.15	0.45	1.20	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.55	1.70	0.55	1.70	0.55	1.70	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.50	ns	

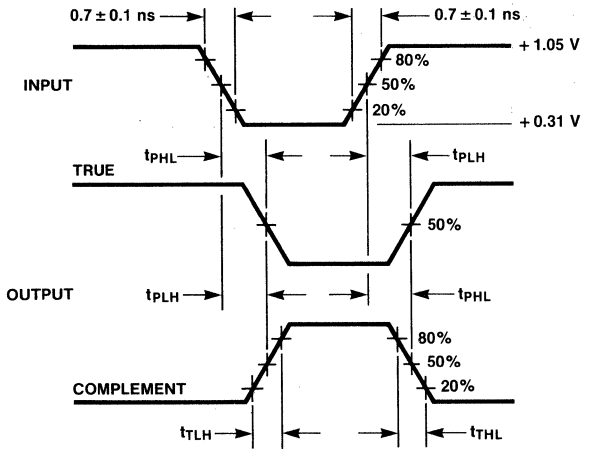
*See Family Characteristics for other dc specifications.

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Fig. 2 Propagation Delay and Transition Times



F100114
Quint Differential Line Receiver

F100K ECL Product

Description

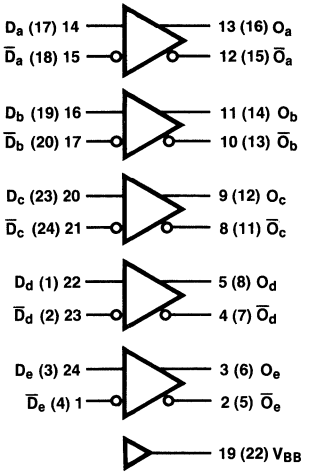
The F100114 is a monolithic quint differential line receiver with emitter-follower outputs. An internal reference supply (V_{BB}) is available for single-ended reception. When used in single-ended operation the apparent input threshold of the true inputs is 25 to 30 mV higher (positive) than the threshold of the complementary inputs. Unlike other F100K ECL devices, the inputs do not have input pull-down resistors.

Active current sources provide common-mode rejection of 1.0 V in either the positive or negative direction. A defined output state exists if both inverting and non-inverting inputs are at the same potential between V_{EE} and V_{CC}. The defined state is logic HIGH on the $\overline{O}_a$-$\overline{O}_e$ outputs.

Pin Names

D_a-D_e	Data Inputs
$\overline{D}_a$-$\overline{D}_e$	Inverting Data Inputs
O_a-O_e	Data Outputs
$\overline{O}_a$-$\overline{O}_e$	Complementary Data Outputs

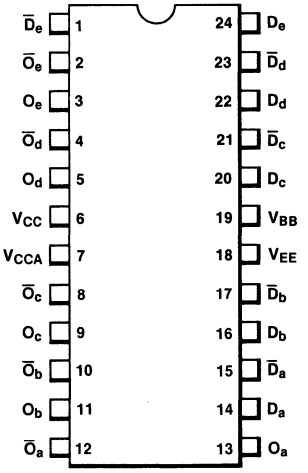
Logic Symbol



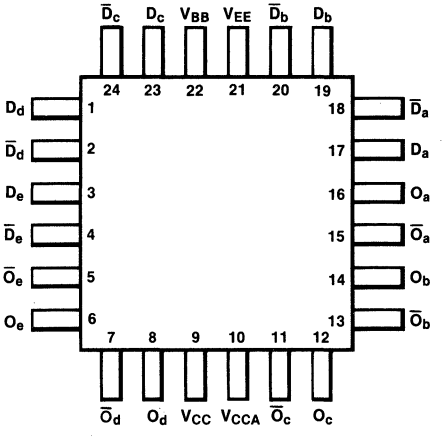
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Connection Diagrams

24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
V_{IH}	Single-ended Input HIGH Voltage	−1165			mV	V_{EE} = −4.5 V	Guaranteed HIGH Signal for All Inputs*
		−1149			mV	V_{EE} = −4.2 V to −4.8 V	
V_{IL}	Single-ended Input LOW Voltage			−1475	mV	V_{EE} = −4.5 V	Guaranteed LOW Signal for All Inputs*
				−1491	mV	V_{EE} = −4.2 V to −4.8 V	
V_{BB}	Output Reference Voltage	−1380	−1320	−1260	mV	V_{EE} = −4.5 V	Tie Pins 22 (1), 24 (3), 14 (17), 16 (19), 20 (23) to Pin 19 (22)
		−1396	−1320	−1244	mV	V_{EE} = −4.2 V to −4.8 V	
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage			1.0	V	Permissible ±V_{CM} with Respect to V_{BB}	
I_{IH}	Input HIGH Current			50	μA	V_{IN} = $V_{IH(max)}$, D_a-D_e = V_{BB}, $\overline{D_a}$-$\overline{D_e}$ = $V_{IL(min)}$	
I_{CBO}	Input Leakage Current	−10			μA	V_{IN} = V_{EE}, D_a-D_e = V_{BB}, $\overline{D_a}$-$\overline{D_e}$ = $V_{IL(min)}$	
I_{EE}	Power Supply Current	−106	−73	−51	mA	D_a-D_e = V_{BB}, $\overline{D_a}$-$\overline{D_e}$ = $V_{IL(min)}$	

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

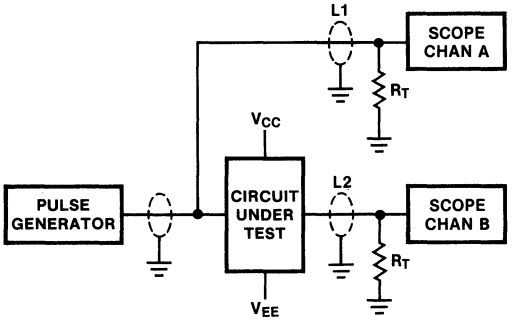
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.55	1.90	0.60	2.00	0.70	2.40	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.55	1.30	0.45	1.20	0.45	1.40	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.55	1.70	0.60	1.80	0.70	2.20	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.55	1.20	0.45	1.10	0.45	1.30	ns	

*One input tied to V_{BB}

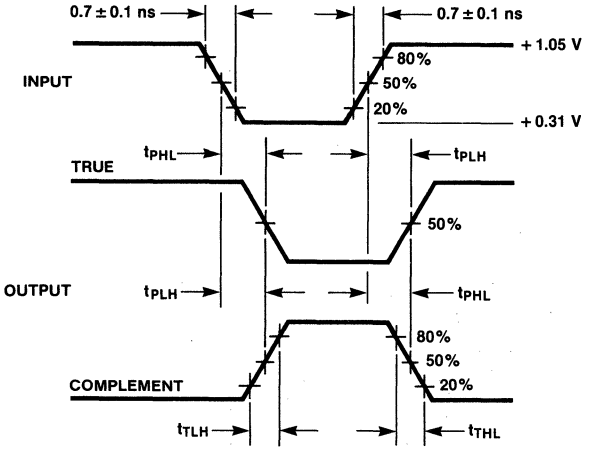
Fig. 1 AC Test Circuit



Notes

V_{CC}, V_{CCA} = +2 V, V_{EE} = −2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Fig. 2 Propagation Delay and Transition Times



F100117
Triple 2-Wide OA/OAI Gate

F100K ECL Product

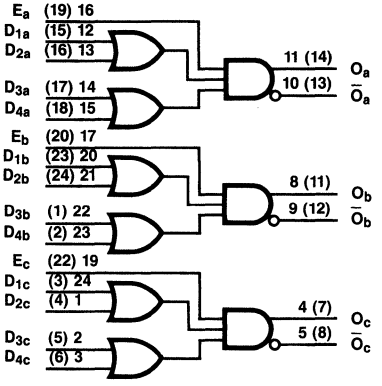
Description

The F100117 is a monolithic triple 2-wide OR/AND gate with true and complement outputs. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Pin Names

D_{na}–D_{nc}	Data Inputs
E_a–E_c	Enable Inputs
O_a–O_c	Data Outputs
$\overline{O}_a$–$\overline{O}_c$	Complementary Data Outputs

Logic Symbol



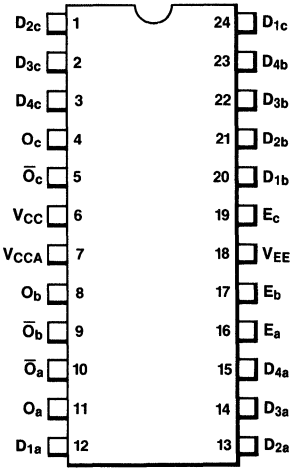
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

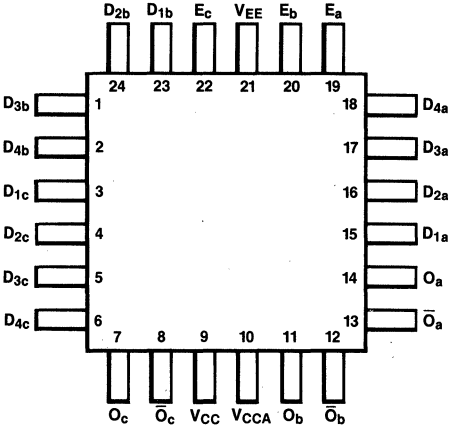
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Connection Diagrams

24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current All Inputs			260	μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	−79	−54	−37	mA	Inputs Open

3

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

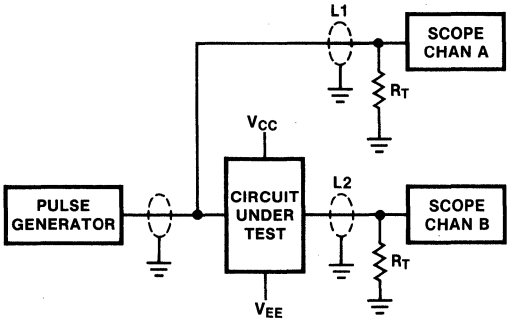
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Condition**
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.90	2.60	0.90	2.50	0.90	2.60	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.45	1.40	0.45	1.30	0.45	1.40	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.30	0.45	1.20	0.45	1.30	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Condition**
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.90	2.40	0.90	2.30	0.90	2.40	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.45	1.20	0.45	1.10	0.45	1.20	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.20	0.45	1.10	0.45	1.20	ns	

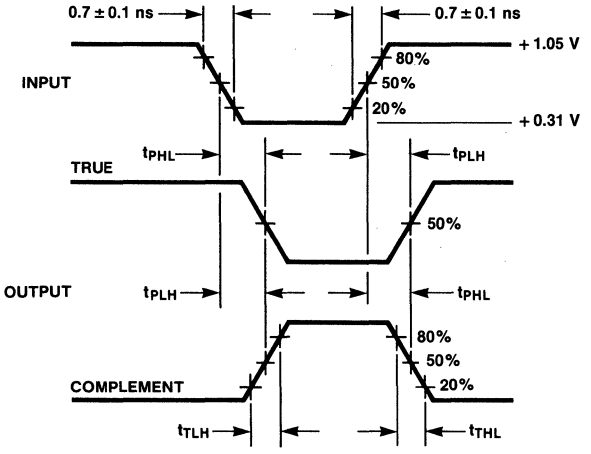
*See Family Characteristics for other dc specifications.

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = −2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Fig. 2 Propagation Delay and Transition Times



F100118
5-Wide 5, 4, 4, 4, 2 OA/OAI Gate

F100K ECL Product

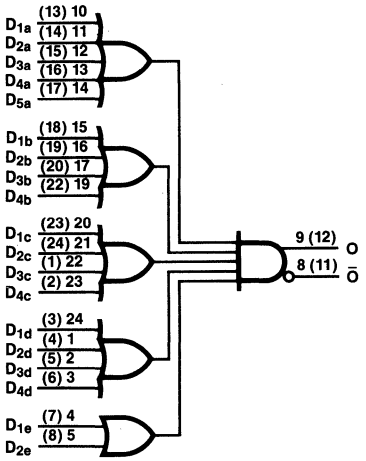
Description

The F100118 is a monolithic 5-wide 5, 4, 4, 4, 2 OR/AND gate with true and complementary outputs. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Pin Names

D_{na}–D_{ne}	Data Inputs
O, $\overline{O}$	Data Outputs

Logic Symbol



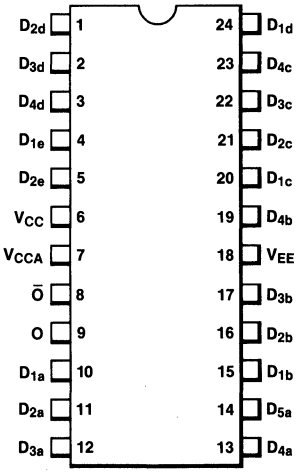
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

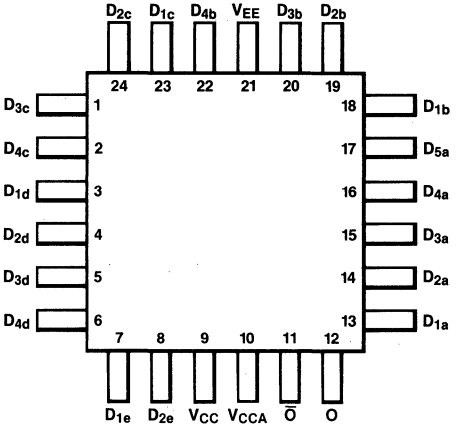
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Connection Diagrams

24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current All Inputs			350	μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	−92	−69	−42	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

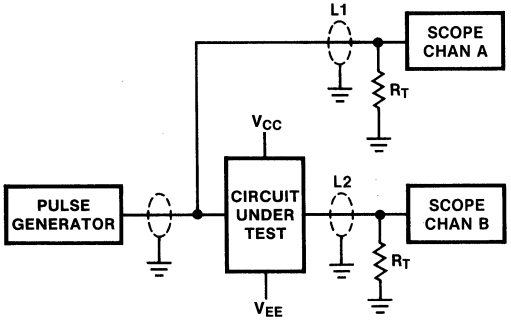
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.85	3.20	0.95	3.20	0.95	3.40	ns	*Figures 1 and 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.50	0.45	1.60	ns	

Flatpak AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.85	3.00	0.95	3.00	0.95	3.20	ns	*Figures 1 and 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.50	ns	

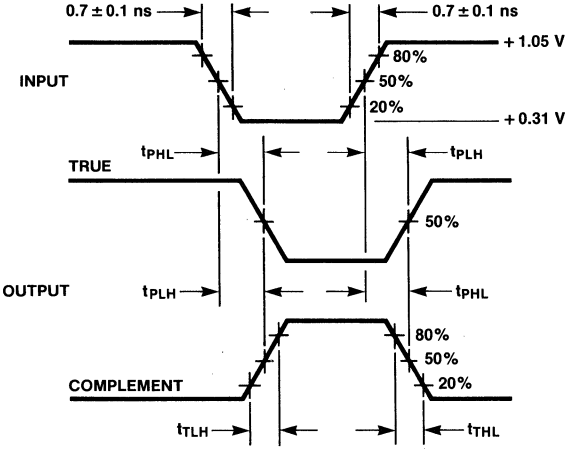
*See Family Characteristics for other dc specifications.

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Fig. 2 Propagation Delay and Transition Times



F100122
9-Bit Buffer

F100K ECL Product

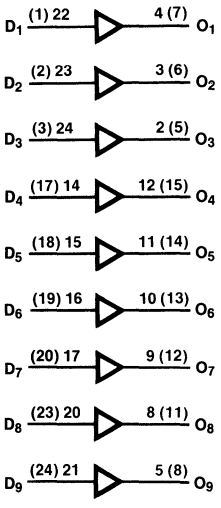
Description

The F100122 is a monolithic 9-bit buffer. The device contains nine non-inverting buffer gates with single input and output. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Pin Names

D_1–D_9	Data Inputs
O_1–O_9	Data Outputs

Logic Symbol



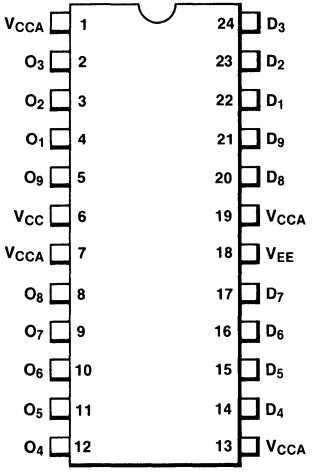
V_{CC} = Pin 6 (9)
V_{CCA} = Pins 1 (4), 7 (10), 13 (16), 19 (22)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

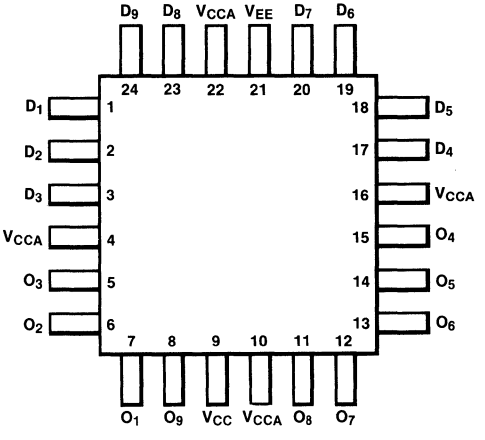
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Connection Diagrams

24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			350	μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	−96	−70	−46	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

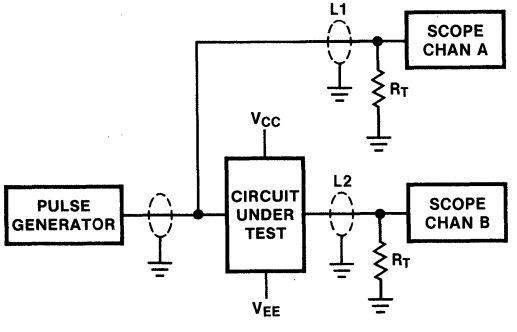
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.60	0.45	1.45	0.45	1.60	ns	*Figures 1 and 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.40	ns	

Flatpak AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.40	0.45	1.25	0.45	1.40	ns	*Figures 1 and 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.40	0.45	1.30	0.45	1.30	ns	

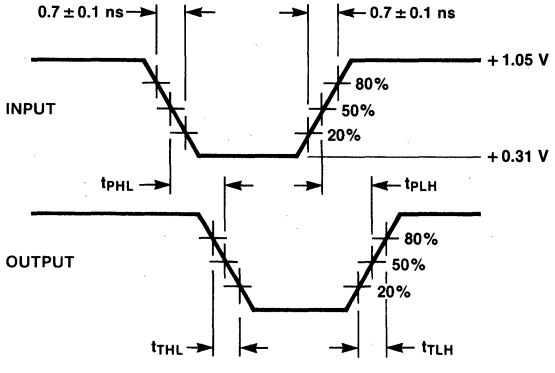
*See Family Characteristics for other dc specifications

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Fig. 2 Propagation Delay and Transition Times



F100123
Hex Bus Driver

F100K ECL Product

Description

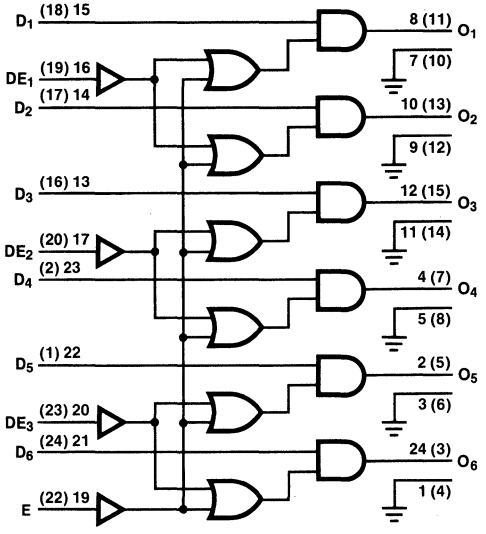
The F100123 is a monolithic device containing six bus drivers capable of driving terminated lines with terminations as low as 25 Ω. To reduce crosstalk, each output has its respective ground connection. Transition times were designed to be longer than on other F100K devices. The driver itself performs the positive logic AND of a data input (D_1-D_6) and the OR of two select inputs (E and either DE_1, DE_2, or DE_3). Enabling of data is possible in multiples of two, *i.e.*, 2, 4, or all 6 paths.

The output voltage LOW level is designed to be more negative than normal ECL outputs (cut off state). This allows an emitter-follower output transistor to turn off when the termination supply is −2.0 V and thus present a high impedance to the data bus.

Pin Names

D_1-D_6	Data Inputs
DE_1-DE_3	Dual Enable Inputs
E	Common Enable Input
O_1-O_6	Data Outputs

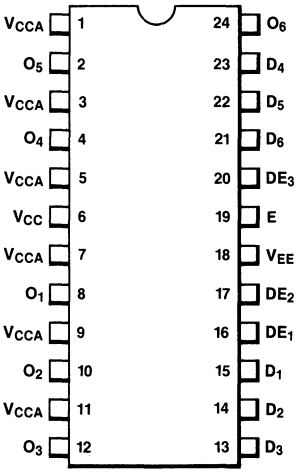
Logic Symbol



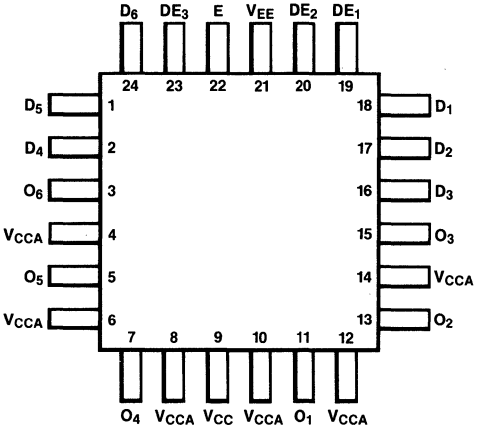
V_{CC} = Pin 6 (9)
V_{CCA} = Pins 1 (4), 3 (6), 5 (8), 7 (10), 9 (12), 11 (14)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Connection Diagrams

24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4Q	FC

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{EE} = −4.5 V	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$, Loaded with 25 Ω to −2.0 V
		−1035		−870	mV	V_{EE} = −4.2 V to −4.8 V	
V_{OHC}	Output HIGH Corner Voltage	−1035			mV	V_{EE} = −4.5 V	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$, Loaded with 25 Ω to −2.3 V
		−1045			mV	V_{EE} = −4.2 V to −4.8 V	
V_{OL}	Output LOW Voltage Cut-off State			−2200	mV	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$ Loaded with 25 Ω to −2.3 V	
I_{IH}	Input HIGH Current Common Enable Data and Dual Enable			330 260	μA	V_{IN} = $V_{IH(max)}$	
I_{EE}	Power Supply Current	−235	−170	−113	mA	Inputs Open	

*See Family Characteristics for other dc specifications.

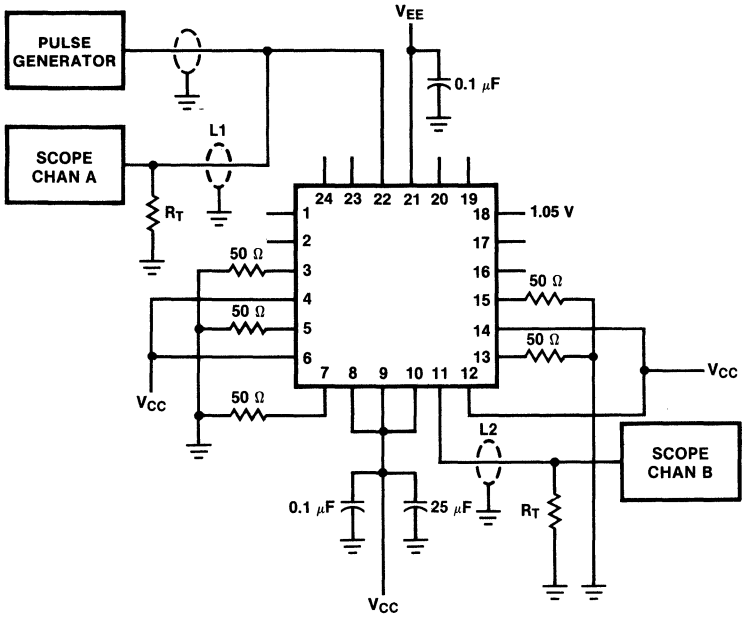
Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.00 1.00	4.30 2.40	1.95 1.00	4.30 2.40	2.00 1.10	4.60 2.60	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Dual Enable to Output	2.30 1.40	4.70 3.00	2.00 1.40	4.70 3.00	2.30 1.40	5.10 3.40	ns	
t_{PLH} t_{PHL}	Propagation Delay Common Enable to Output	2.60 1.50	5.40 3.20	2.50 1.50	5.30 3.30	2.80 1.50	5.80 3.60	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.70 0.45	2.10 1.40	0.70 0.45	1.80 1.30	0.70 0.45	2.20 1.40	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.00 1.00	4.10 2.20	1.95 1.00	4.10 2.20	2.00 1.10	4.40 2.40	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Dual Enable to Output	2.30 1.40	4.50 2.80	2.00 1.40	4.50 2.80	2.30 1.40	4.90 3.20	ns	
t_{PLH} t_{PHL}	Propagation Delay Common Enable to Output	2.60 1.50	5.20 3.00	2.50 1.50	5.10 3.10	2.80 1.50	5.60 3.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.70 0.45	2.00 1.30	0.70 0.45	1.70 1.20	0.70 0.45	2.10 1.30	ns	

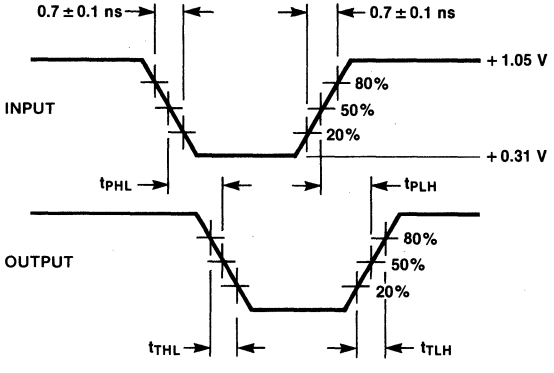
Fig. 1 AC Test Circuit



Notes

V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Fig. 2 Propagation Delay and Transition Times



F100124
Hex TTL-to-ECL Translator

F100K ECL Product

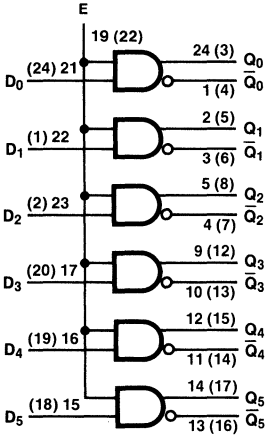
Description

The F100124 is a hex translator, designed to convert TTL logic levels to 100K ECL logic levels. The inputs are compatible with standard or Schottky TTL. A common Enable input (E), when LOW, holds all inverting outputs HIGH and holds all true outputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator or as a differential line driver. The output levels are voltage compensated.

When the circuit is used in the differential mode, the F100124, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems. The V_{EE} and V_{TTL} power may be applied in either order.

Pin Names	Description	TTL Unit Load (U.L.) HIGH/LOW
D_0-D_5	Data Inputs	0.5/1.0
E	Enable Input	3.0/6.0
Q_0-Q_5	Data Outputs	—
$\overline{Q}_0$-$\overline{Q}_5$	Complementary Data Outputs	—

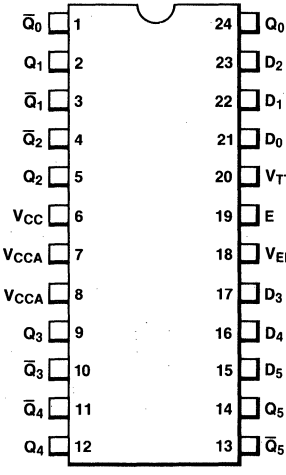
Logic Symbol



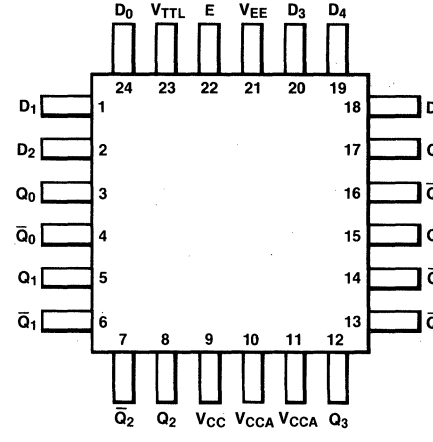
V_{CC} = Pin 6 (9)
V_{CCA} = Pins 7 (10), 8 (11)
V_{EE} = Pin 18 (21)
V_{TTL} = Pin 20 (23)
( ) = Flatpak

Connection Diagrams

24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Absolute Maximum Ratings* Above which the useful life may be impaired

V_{TTL} Pin Potential to Ground Pin	+6.0 V to −0.5 V
Input Voltage (dc)	−0.5 V to V_{TTL}

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5 V to +5.5 V, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		5.0	V	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	0		0.8	V	Guaranteed LOW Signal for All Inputs
V_{CD}	Input Clamp Diode Voltage	−1.5			V	I_{IN} = −10 mA
I_{IH}	Input HIGH Current Data Enable			20 120	μA	V_{IN} = +2.4 V, All Other Inputs V_{IN} = GND
	Input HIGH Current Breakdown Test, All Inputs			1.0	mA	V_{IN} = +5.5 V, All Other Inputs = GND
I_{IL}	Input LOW Current Data Enable	 −1.6 −9.6			mA	V_{IN} = +0.4 V, All Other Inputs V_{IN} = GND
I_{EE}	V_{EE} Power Supply Current	−140	−96	−52	mA	All Inputs V_{IN} = +4.0 V
I_{TTL}	V_{TTL} Power Supply Current		44	75	mA	All Inputs V_{IN} = GND

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5 V to +5.5 V

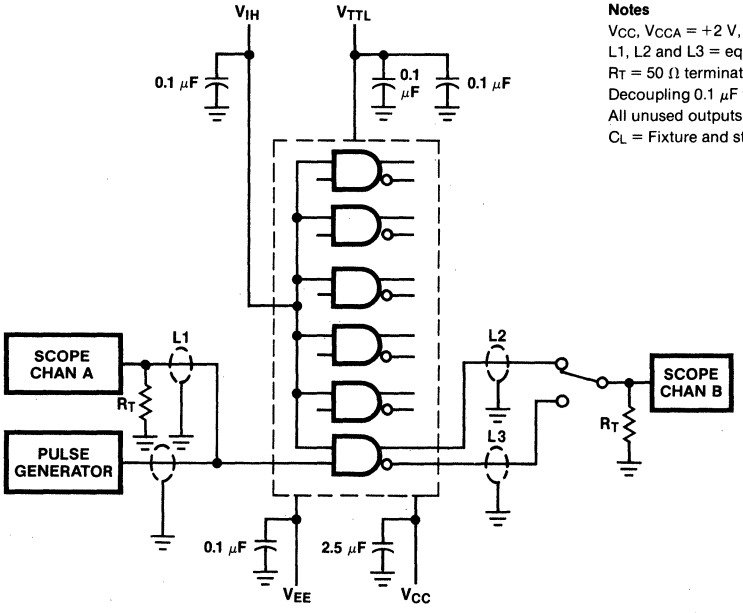
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.50	3.00	0.50	2.90	0.50	3.00	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.80	0.45	1.80	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5 V to +5.5 V

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.50	2.80	0.50	2.70	0.50	2.80	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.70	ns	

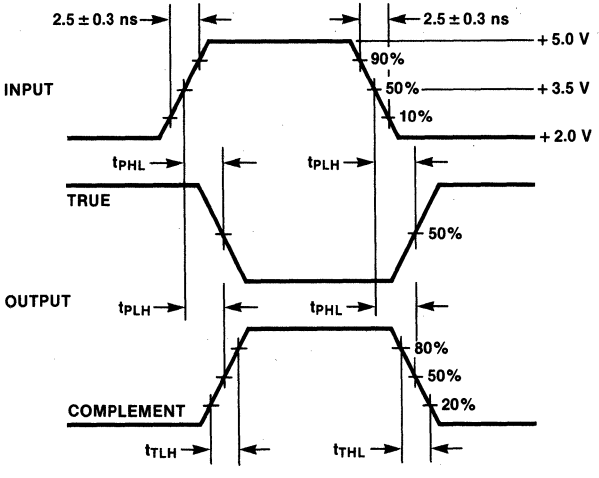
*See Family Characteristics for other absolute maximum ratings and dc specifications.

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = −2.5 V, V_{TTL} = +7.0 V, V_{IH} = +6.0 V
L1, L2 and L3 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC}, V_{EE} and V_{TTL}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Fig. 2 Propagation Delay and Transition Times



F100125
Hex ECL-to-TTL Translator

F100K ECL Product

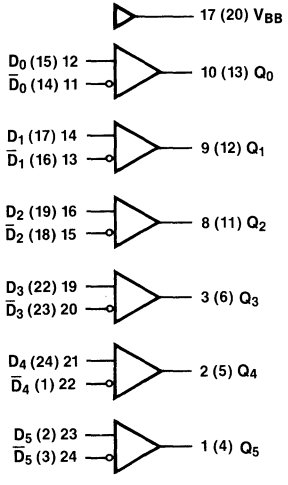
Description

The F100125 is a hex translator for converting F100K logic levels to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non-inverting or differential receiver. An internal reference voltage generator provides V_{BB} for single-ended operation or for use in Schmitt trigger applications. All inputs have 50 kΩ pull-down resistors; therefore, the outputs will go LOW when the inputs are left unconnected.

When used in the differential mode, the inputs have a common mode rejection of +1 V, making this device tolerant of ground offsets and transients between the signal source and the translator. The V_{EE} and V_{TTL} power may be applied in either order.

Pin Names	Description	TTL Unit Load (U.L.) HIGH/LOW
D_0-D_5	Data Inputs	—
$\overline{D_0}$-$\overline{D_5}$	Inverting Data Inputs	—
Q_0-Q_5	Data Outputs	50/12.5

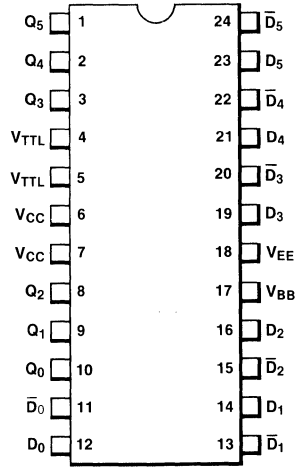
Logic Symbol



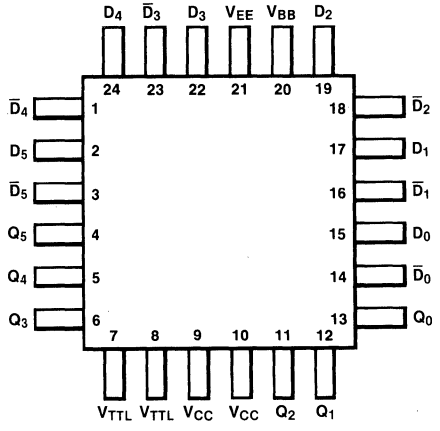
V_{TTL} = Pins 4 (7), 5 (8)
V_{CC} = Pins 6 (9), 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Connection Diagrams

24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Truth Table

Inputs		Outputs
D_n	$\overline{D_n}$	Q_n
L	H	L
H	L	H
L	L	U
H	H	U
Open	Open	L
V_{EE}	V_{EE}	L
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	L	H
V_{BB}	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
U = Undefined

Absolute Maximum Ratings[1] Above which the useful life may be impaired

V_{TTL} Pin Potential to Ground Pin +6.0 V to −0.5 V

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = GND, V_{TTL} = +4.5 to +5.5 V, T_C = 0°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
V_{OH}	Output HIGH Voltage	2.5			V	I_{OH} = −2.0 mA	$V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 20 mA	
V_{IH}	Single-ended Input HIGH Voltage	−1165		−880	mV	V_{EE} = −4.5 V	Guaranteed HIGH Signal for All Inputs[2]
		−1150		−880	mV	V_{EE} = −4.2 V to −4.8 V	
V_{IL}	Single-ended Input LOW Voltage	−1810		−1475	mV	V_{EE} = −4.5 V	Guaranteed LOW Signal for All Inputs[2]
		−1810		−1490	mV	V_{EE} = −4.2 V to −4.8 V	
V_{BB}	Output Reference Voltage	−1380	−1320	−1260	mV	V_{EE} = −4.5 V	Tie Pins 12 (15), 14 (17), 19 (22), 21 (24), 23 (2) to Pin 17 (20)
		−1396	−1320	−1244	mV	V_{EE} = −4.2 V to −4.8 V	

Notes
1. See Family Characteristics for other absolute maximum ratings
2. One input tied to V_{BB}

DC Characteristics (Cont'd): V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = GND, V_{TTL} = +4.5 to +5.5 V, T_C = 0°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing
V_{CM}	Common Mode Voltage			1.0	V	Permissible $\pm V_{CM}$ with Respect to V_{BB}
I_{IH}	Input HIGH Current			350	μA	$V_{IN} = V_{IH(max)}$, D_0-$D_5 = V_{BB}$, $\overline{D_0}$-$\overline{D_5} = V_{IL(min)}$
I_{IL}	Input LOW Current	0.5			μA	$V_{IN} = V_{IL(min)}$, D_0-$D_5 = V_{BB}$
I_{OS}	Output Short-circuit Current	−100		−40	mA	V_{OUT} = GND*
I_{EE}	V_{EE} Power Supply Current	−85	−60	−40	mA	D_0-$D_5 = V_{BB}$
I_{TTL}	V_{TTL} Power Supply Current		75	115	mA	D_0-$D_5 = V_{BB}$

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = GND, V_{TTL} = +4.5 V to +5.5 V

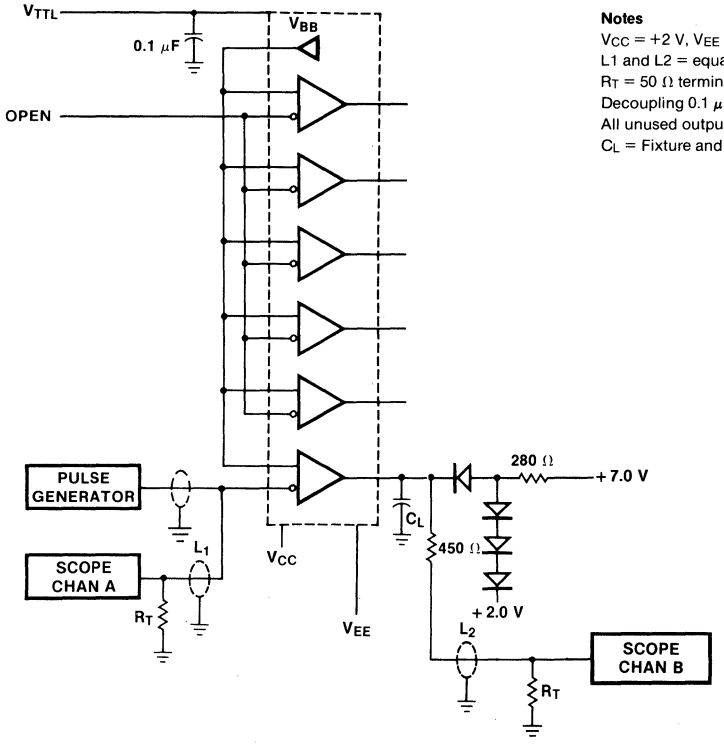
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.80	3.50	0.90	3.70	1.00	4.00	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 10% to 90%, 90% to 10%	0.50	2.60	0.50	2.60	0.50	2.60	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = GND, V_{TTL} = +4.5 V to +5.5 V

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.80	3.30	0.90	3.50	1.00	3.80	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 10% to 90%, 90% to 10%	0.50	2.50	0.50	2.50	0.50	2.50	ns	

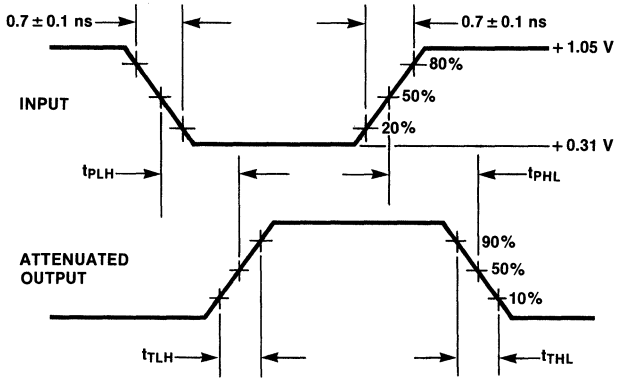
*Test one output at a time.

Fig. 1 AC Test Circuit



Notes
V_{CC} = +2 V, V_{EE} = −2.5 V, V_{TTL} = +7 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC}, V_{EE} and V_{TTL}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Fig. 2 Propagation Delay and Transition Times



F100126
9-Bit Backplane Driver

F100K ECL Product

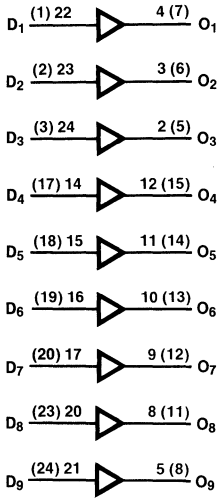
Description

The F100126 contains nine independent, high-speed, buffer gates each with a single input and a single output. The gates are non-inverting. These buffers are useful in bus-oriented systems where minimal output loading or bus isolation is desired. The output transition times are longer to minimize noise when used as a backplane driver.

Pin Names

D_1–D_9	Data Inputs
O_1–O_9	Data Outputs

Logic Symbol



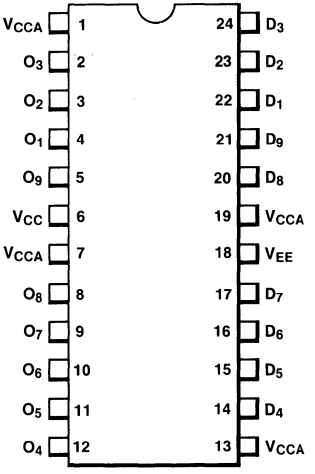
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 1 (4), 7 (10), 13 (16), 19 (22)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

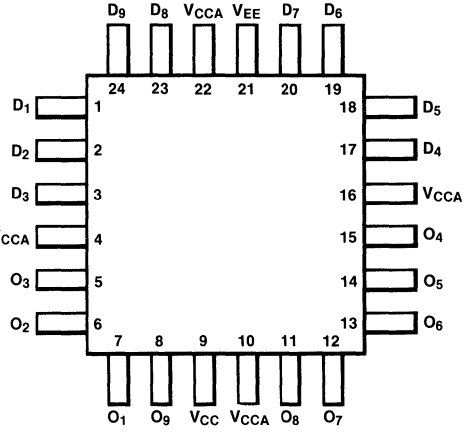
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Connection Diagrams

24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			350	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−96	−70	−46	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

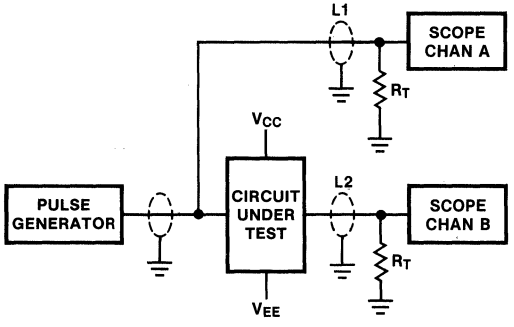
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.05	2.75	1.05	2.75	1.05	2.75	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	1.15	3.40	1.15	3.40	1.05	3.40	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.05	2.55	1.05	2.55	1.05	2.55	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	1.15	3.30	1.15	3.30	1.05	3.30	ns	

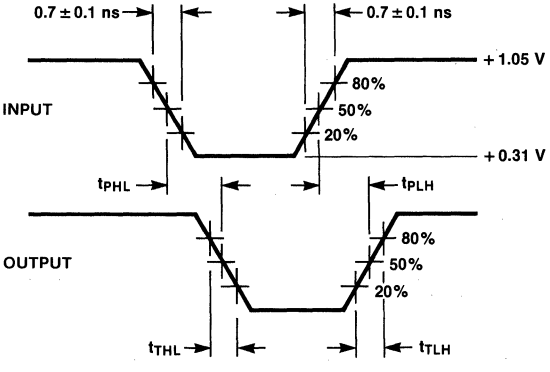
*See Family Characteristics for other dc specifications.

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = −2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Fig. 2 Propagation Delay and Transition Times



F100130
Triple D Latch

F100K ECL Product

Description

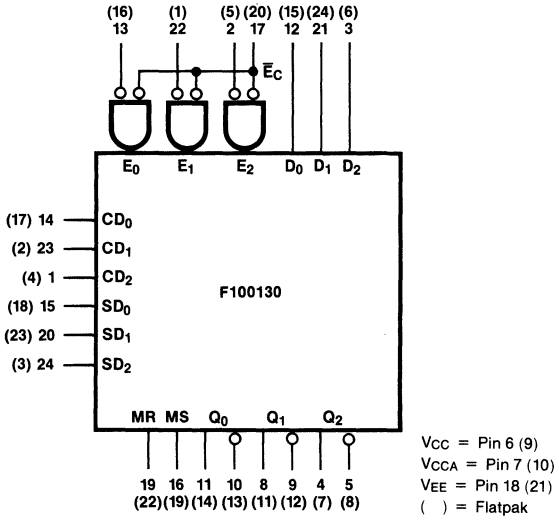
The F100130 contains three D-type latches with true and complement outputs and with Common Enable ($\overline{E}_C$), Master Set (MS) and Master Reset (MR) inputs. Each latch has its own Enable ($\overline{E}_n$), Direct Set (SD_n) and Direct Clear (CD_n) inputs. The Q output follows its Data (D) input when both $\overline{E}_n$ and $\overline{E}_C$ are LOW (transparent mode). When either $\overline{E}_n$ or $\overline{E}_C$ (or both) are HIGH, a latch stores the last valid data present on its D_n input before $\overline{E}_n$ or $\overline{E}_C$ goes HIGH.

Both Master Reset (MR) and Master Set (MS) inputs override the Enable inputs. The individual CD_n and SD_n also override the Enable inputs.

Pin Names

CD_0-CD_2	Individual Direct Clear Inputs
SD_0-SD_2	Individual Direct Set Inputs
$\overline{E}_0$-$\overline{E}_2$	Individual Enable Inputs (Active LOW)
$\overline{E}_C$	Common Enable Input (Active LOW)
D_0-D_2	Data Inputs
MR	Master Reset Input
MS	Master Set Input
Q_0-Q_2	Data Outputs
$\overline{Q}_0$-$\overline{Q}_2$	Complementary Data Outputs

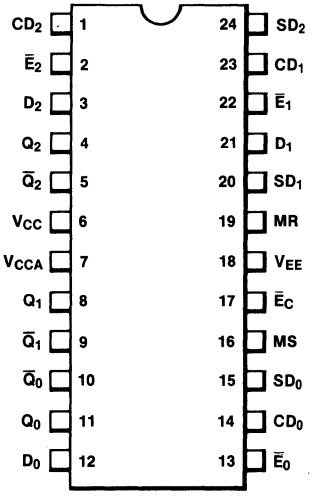
Logic Symbol



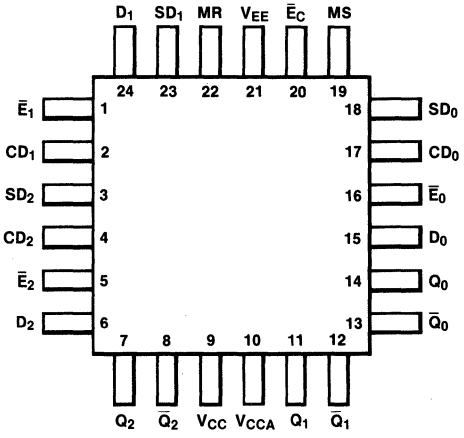
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Connection Diagrams

24-Pin DIP (Top View)



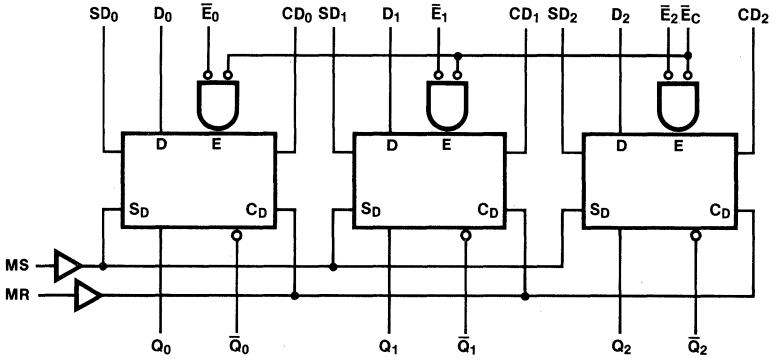
24-Pin Flatpak (Top View)



Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Logic Diagram



Truth Tables (Each Latch)

Latch Operation

Inputs					Outputs
D_n	$\overline{E}_n$	$\overline{E}_C$	MS SD_n	MR CD_n	Q_n
L	L	L	L	L	L
H	L	L	L	L	H
X	H	X	L	L	Latched*
X	X	H	L	L	Latched*

Asynchronous Operation

Inputs					Outputs
D_n	$\overline{E}_n$	$\overline{E}_C$	MS SD_n	MR CD_n	Q_n
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

*Retains data presented before $\overline{E}$ positive transition
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
U = Undefined

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current D_n CD_n, SD_n $\overline{E}_n$ $\overline{E}_C$, MR, MS			 350 530 240 450	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−149	−106	−74	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

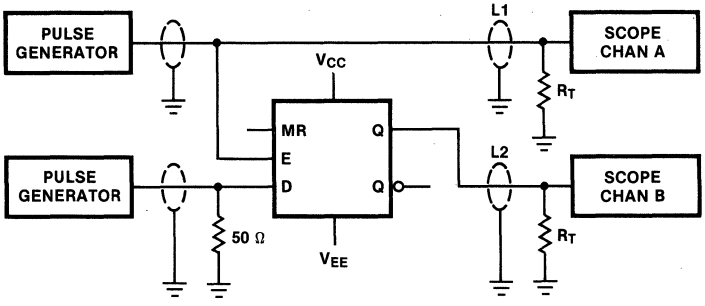
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay D_n to Output (Transparent Mode)	0.50	1.80	0.50	1.70	0.50	1.90	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_C$ to Output	0.65	2.10	0.75	2.00	0.75	2.10	ns	
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n, $\overline{E}_n$ to Output	0.50	2.00	0.60	1.75	0.60	2.00	ns	*Figures 1, 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.50	1.10	2.40	1.10	2.60	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.60	0.45	1.60	ns	*Figures 1* and *2*
t_s	Setup Time D_0-D_2 CD_n, SD_n (Release Time) MR, MS (Release Time)	 0.90 1.20 1.90		 0.70 1.10 1.90		 0.90 1.40 2.00		ns	*Figures 3* and *4*
t_h	Hold Time D_0-D_2	0.60		0.60		0.80		ns	*Figure 4*
t_{pw}(L)	Pulse Width LOW $\overline{E}_n$, $\overline{E}_C$	2.00		2.00		2.00		ns	*Figure 2*
t_{pw}(H)	Pulse Width HIGH CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	*Figure 3*

*See Family Characteristics for other dc specifications.

Flatpak AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output (Transparent Mode)	0.50	1.60	0.50	1.50	0.50	1.70	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_C$ to Output	0.65	1.90	0.75	1.80	0.75	1.90	ns	
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n, $\overline{E}_n$ to Output	0.50	1.80	0.60	1.55	0.60	1.80	ns	*Figures 1, 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.30	1.10	2.20	1.10	2.40	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.50	0.45	1.50	ns	*Figures 1* and *2*
t_s	Setup Time D_0-D_2 CD_n, SD_n (Release Time) MR, MS (Release Time)	0.80 1.10 1.80		0.60 1.00 1.80		0.80 1.30 2.00		ns	*Figures 3* and *4*
t_h	Hold Time D_0-D_2	0.50		0.50		0.70		ns	*Figure 4*
$t_{pw}(L)$	Pulse Width LOW $\overline{E}_n$, $\overline{E}_C$	2.00		2.00		2.00		ns	*Figure 2*
$t_{pw}(H)$	Pulse Width HIGH CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	*Figure 3*

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Fig. 2 Enable Timing

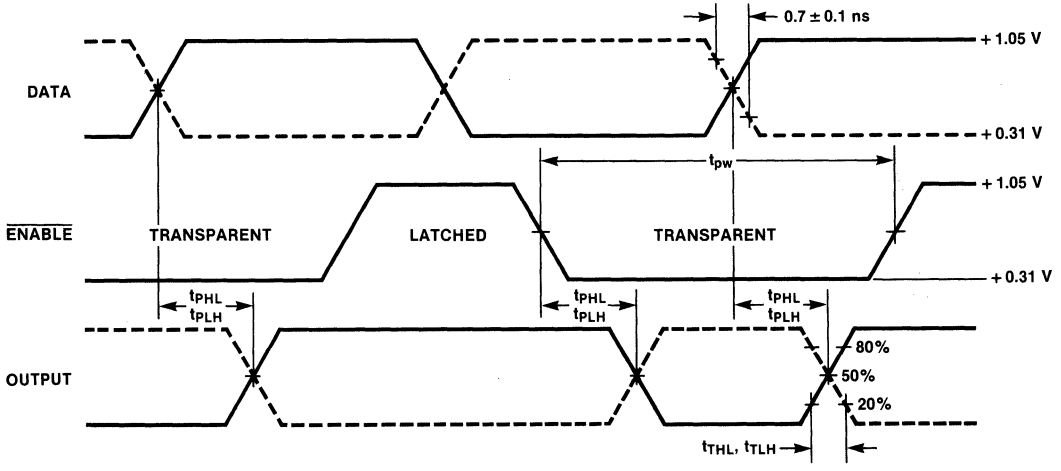


Fig. 3 Reset Timing

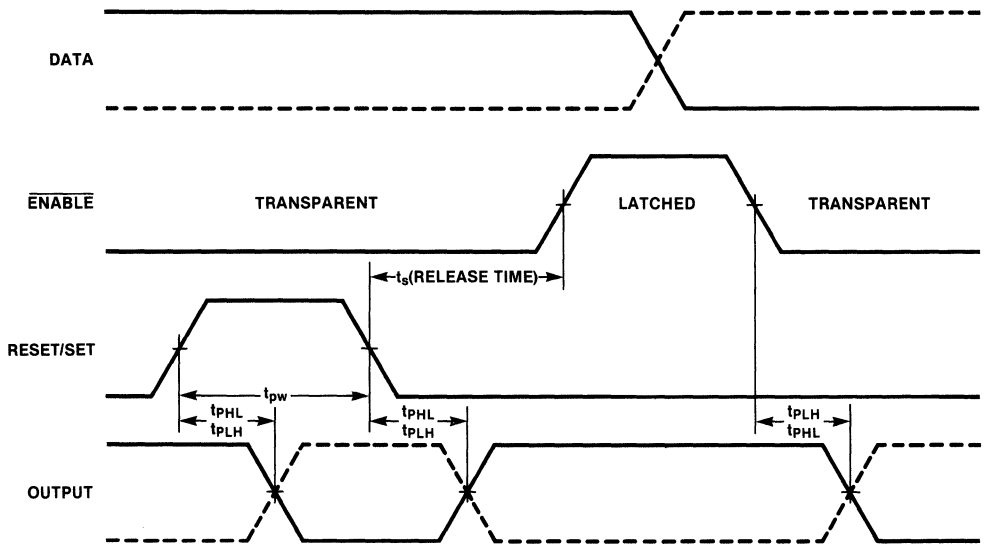
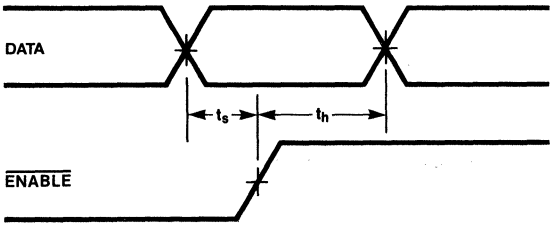


Fig. 4 Data Setup and Hold Time



Notes

t_s is the minimum time before the transition of the enable that information must be present at the data input

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input

F100131
Triple D Flip-Flop

F100K ECL Product

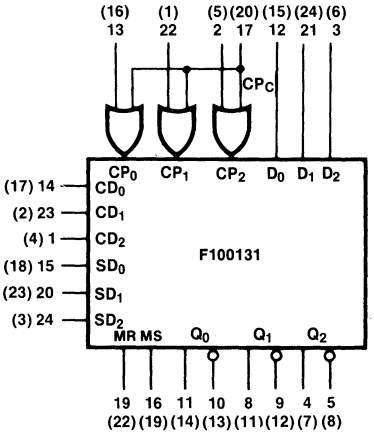
Description

The F100131 contains three D-type, edge-triggered master/slave flip-flops with true and complement outputs, a Common Clock (CP_C), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual Clock (CP_n), Direct Set (SD_n) and Direct Clear (CD_n) inputs. Data enters a master when both CP_n and CP_C are LOW and transfers to a slave when CP_n or CP_C (or both) go HIGH. The Master Set, Master Reset and individual CD_n and SD_n inputs override the Clock inputs.

Pin Names

CP_0–CP_2	Individual Clock Inputs
CP_C	Common Clock Input
D_0–D_2	Data Inputs
CD_0–CD_2	Individual Direct Clear Inputs
SD_n	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
Q_0–Q_2	Data Outputs
$\overline{Q}_0$–$\overline{Q}_2$	Complementary Data Outputs

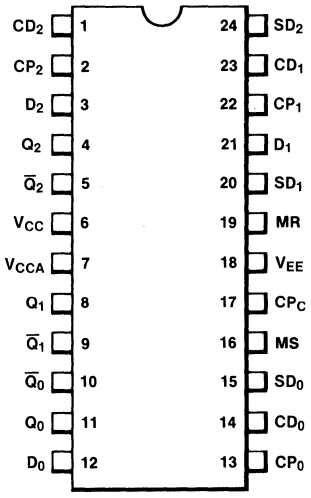
Logic Symbol



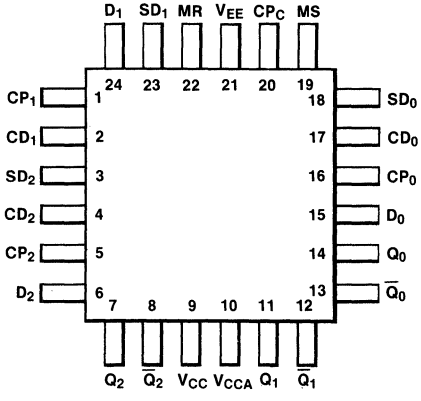
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Connection Diagrams

24-Pin DIP (Top View)



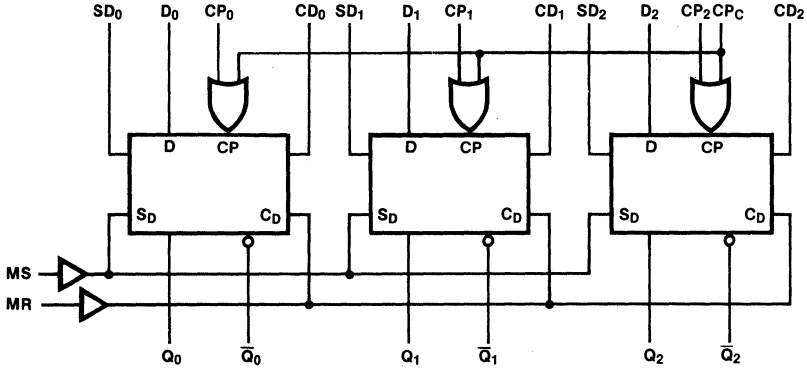
24-Pin Flatpak (Top View)



Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Logic Diagram



Truth Tables (Each Flip Flop)

Synchronous Operation

Inputs					Outputs
D_n	CP_n	CP_C	MS SD_n	MR CD_n	$Q_n(t+1)$
L	⌐¬	L	L	L	L
H	⌐¬	L	L	L	H
L	L	⌐¬	L	L	L
H	L	⌐¬	L	L	H
X	L	L	L	L	$Q_n(t)$
X	H	X	L	L	$Q_n(t)$
X	X	H	L	L	$Q_n(t)$

Asynchronous Operation

Inputs					Outputs
D_n	CP_n	CP_C	MS SD_n	MR CD_n	$Q_n(t+1)$
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
U = Undefined
t = Time before CP positive transition
t+1 = Time after CP positive transition
⌐¬ = LOW to HIGH transition

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current CP_n, D_n MS, MR, CP_C CD_n, SD_n			 240 450 530	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−149	−106	−74	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C				
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition	
f_{max}	Toggle Frequency	325		325		325		MHz	*Figures 2* and *3*	
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	0.75	2.40	0.75	2.15	0.70	2.30	ns	*Figures 1* and *3*	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.70	2.20	0.70	2.00	0.70	2.20	ns		
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	0.70	1.90	0.70	1.70	0.70	1.80	ns	CP_n, CP_C = L	*Figures 1* and *4*
t_{PLH} t_{PHL}		0.70	2.10	0.70	2.00	0.70	2.20		CP_n, CP_C = H	
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.70	1.10	2.60	1.10	2.70	ns	CP_n, CP_C = L	
t_{PLH} t_{PHL}		1.05	3.05	1.05	2.95	1.05	3.05		CP_n, CP_C = H	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.20	0.45	1.80	0.45	1.90	ns	*Figures 1, 3* and *4*	
t_s	Setup Time D_n CD_n, SD_n (Release Time) MS, MR (Release Time)	 0.90 1.50 2.50		 0.70 1.30 2.30		 0.90 1.50 2.50		ns	*Figure 5* *Figure 4*	
t_h	Hold Time D_n	0.60		0.60		0.80		ns	*Figure 5*	
t_{pw}(H)	Pulse Width HIGH CP_n, CP_C, CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	*Figures 3* and *4*	

*See Family Characteristics for other dc specifications.

Flatpak AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition	
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	350		350		350		MHz	*Figures 2* and *3*	
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	0.75	2.20	0.75	1.95	0.70	2.10	ns	*Figures 1* and *3*	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.70	2.00	0.70	1.80	0.70	2.00	ns		
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	0.70	1.70	0.70	1.50	0.70	1.60	ns	CP_n, CP_C = L	*Figures 1* and *4*
t_{PLH} t_{PHL}		0.70	1.90	0.70	1.80	0.70	2.00		CP_n, CP_C = H	
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.50	1.10	2.40	1.10	2.50	ns	CP_n, CP_C = L	
t_{PLH} t_{PHL}		1.05	2.85	1.05	2.75	1.05	2.85		CP_n, CP_C = H	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.00	0.45	1.60	0.45	1.70	ns	*Figures 1, 3* and *4*	
t_s	Setup Time D_n	0.80		0.60		0.80		ns	*Figure 5*	
	CD_n, SD_n (Release Time)	1.40		1.20		1.40			*Figure 4*	
	MS, MR (Release Time)	2.40		2.20		2.40				
t_h	Hold Time D_n	0.50		0.50		0.70		ns	*Figure 5*	
$t_{pw}(H)$	Pulse Width HIGH CP_n, CP_C, CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	*Figures 3* and *4*	

Fig. 1 AC Test Circuit

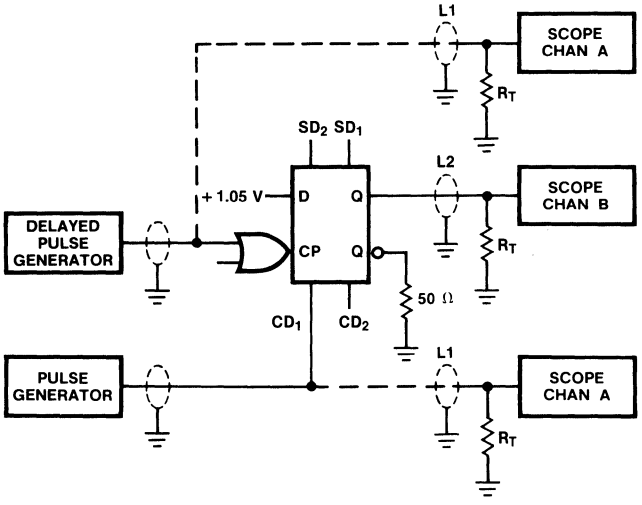
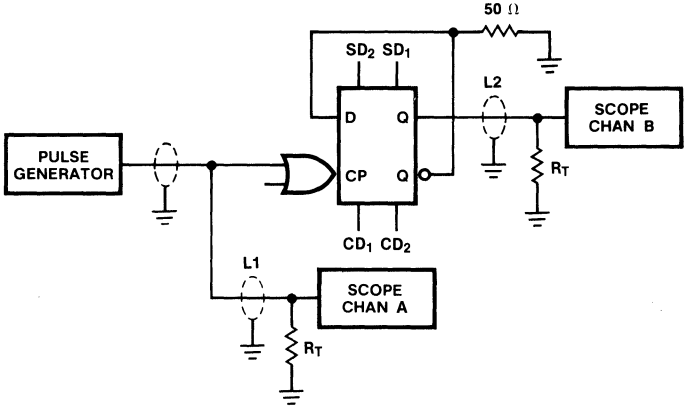


Fig. 2 Toggle Frequency Test Circuit



Notes

V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Fig. 3 Propagation Delay (Clock) and Transition Times

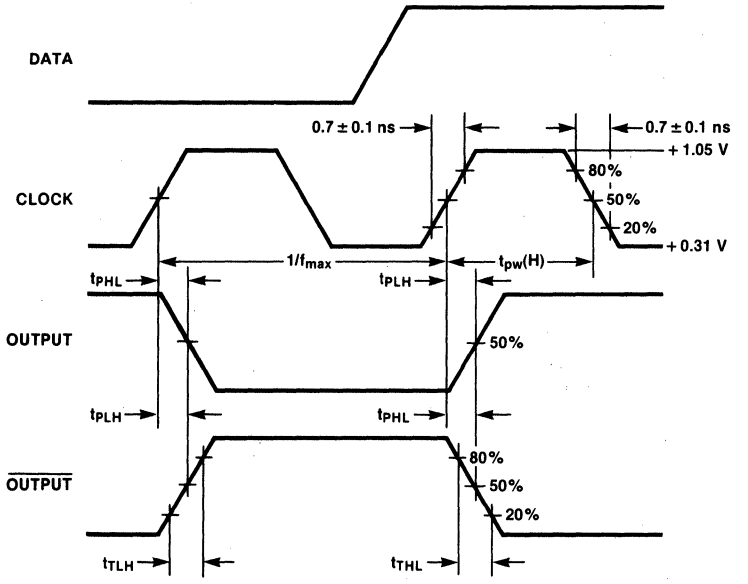


Fig. 4 Propagation Delay (Resets)

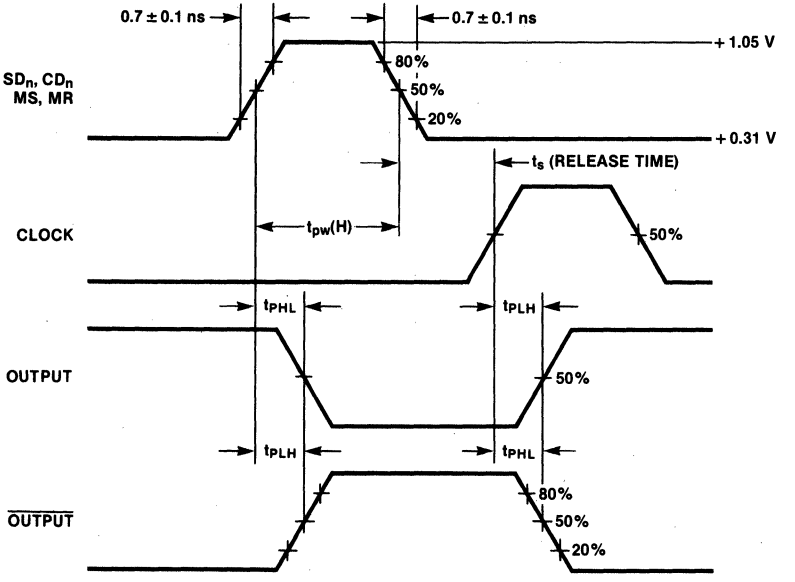
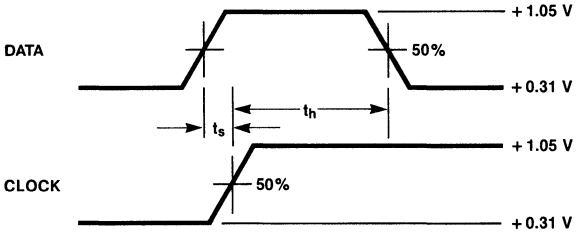


Fig. 5 Data Setup and Hold Time



Notes

t_s is the minimum time before the transition of the clock that information must be present at the data input

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input

F100136
4-Stage Counter/ Shift Register

F100K ECL Product

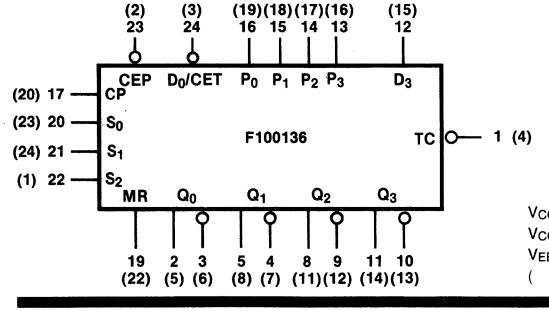
Description

The F100136 operates as either a modulo-16 up/down counter or as a 4-bit bidirectional shift register. Three Select (S_n) inputs determine the mode of operation, as shown in the Function Select table. Two Count Enable ($\overline{CEP}$, $\overline{CET}$) inputs are provided for ease of cascading in multistage counters. One Count Enable ($\overline{CET}$) input also doubles as a Serial Data (D_0) input for shift-up operation. For shift-down operation D_3 is the Serial Data input. In counting operations the Terminal Count ($\overline{TC}$) output goes LOW when the counter reaches 15 in the count/up mode or 0 (zero) in the count/down mode. In the shift modes, the $\overline{TC}$ output repeats the Q_3 output. The dual nature of this $\overline{TC}/Q_3$ output and the $D_0/\overline{CET}$ input means that one interconnection from one stage to the next higher stage serves as the link for multistage counting or shift-up operation. The individual Preset (P_n) inputs are used to enter data in parallel or to preset the counter in programmable counter applications. A HIGH signal on the Master Reset (MR) input overrides all other inputs and asynchronously clears the flip-flops. In addition, a synchronous clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops.

Pin Names

CP	Clock Pulse Input
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)
$D_0/\overline{CET}$	Serial Data Input/Count Enable Trickle Input (Active LOW)
S_0-S_2	Select Inputs
MR	Master Reset Input
P_0-P_3	Preset Inputs
D_3	Serial Data Input
$\overline{TC}$	Terminal Count Output
Q_0-Q_3	Data Outputs
$\overline{Q}_0$-$\overline{Q}_3$	Complementary Data Outputs

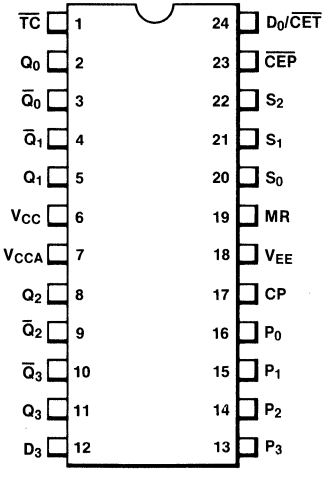
Logic Symbol



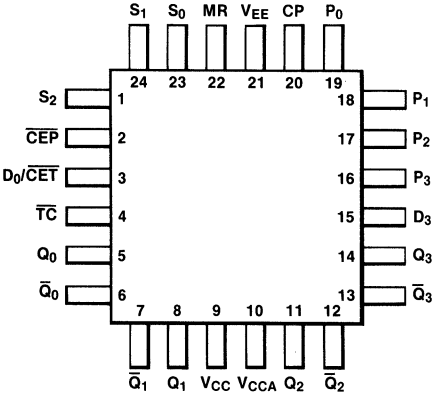
VCC = Pin 6 (9)
VCCA = Pin 7 (10)
VEE = Pin 18 (21)
( ) = Flatpak

Connection Diagrams

24-Pin DIP (Top View)



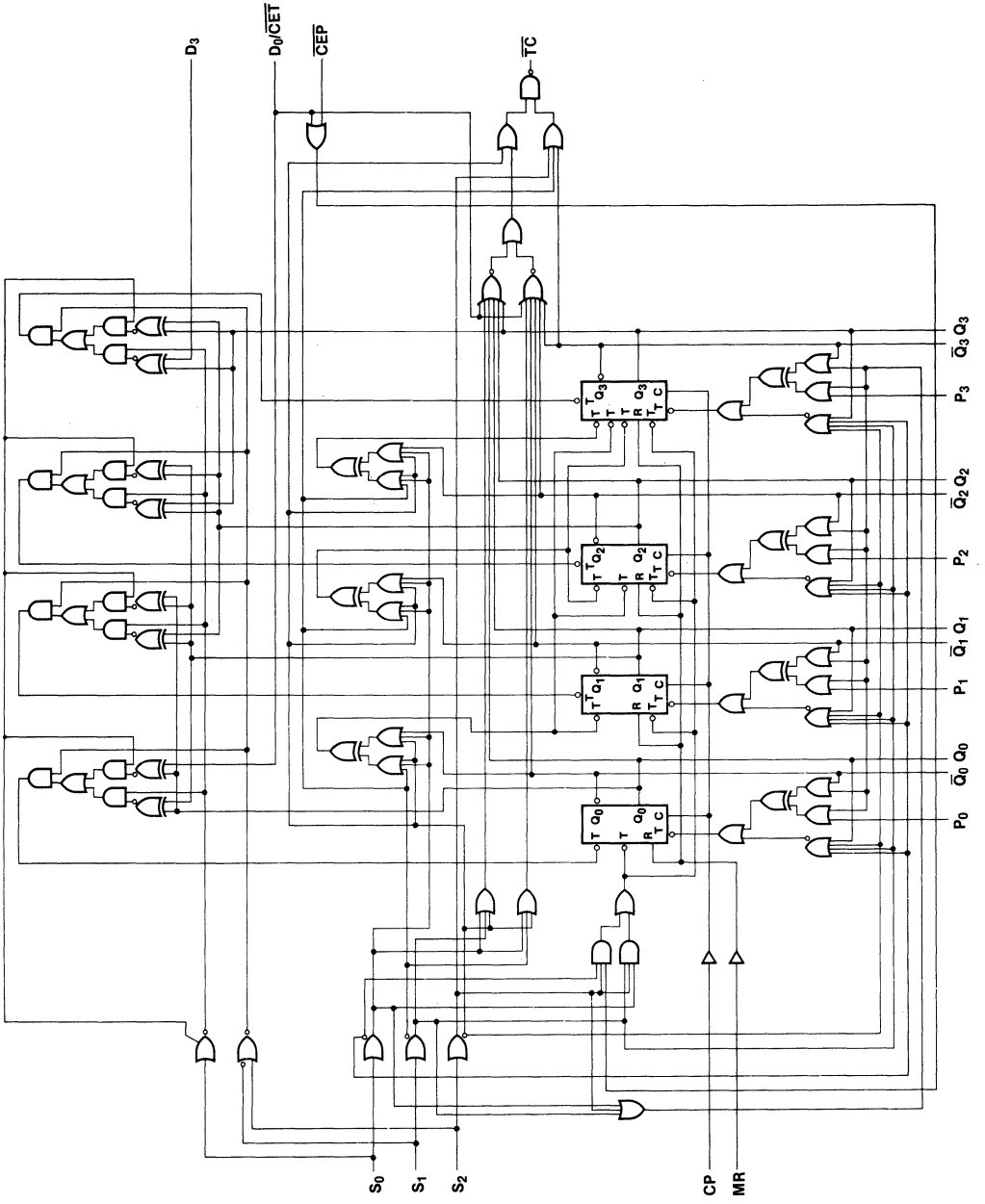
24-Pin Flatpak (Top View)



Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4Q	FC

Logic Diagram



Function Select Table

S_0	S_1	S_2	Function
L	L	L	Parallel load
L	L	H	Count Down
L	H	L	Shift Left
L	H	H	Count Up
H	L	L	Complement
H	L	H	Clear
H	H	L	Shift Right
H	H	H	Hold

Truth Table

Inputs								Outputs					
MR	S_0	S_1	S_2	$\overline{CEP}$	$D_0/\overline{CET}$	D_3	CP	Q_0	Q_1	Q_2	Q_3	$\overline{TC}$	Mode
L	L	L	L	X	X	X	⎍	P_0	P_1	P_2	P_3	L	Preset (Parallel Load)
L	L	L	H	L	L	X	⎍	(Q_{0-3}) minus 1				①	Count Down
L	L	L	H	H	L	X	X	Q_0	Q_1	Q_2	Q_3	①	Count Down with $\overline{CEP}$ not active
L	L	L	H	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Down with $\overline{CET}$ not active
L	L	H	L	X	X	X	⎍	Q_1	Q_2	Q_3	D_3	D_3	Shift Left
L	L	H	H	L	L	X	⎍	(Q_{0-3}) plus 1				②	Count Up
L	L	H	H	H	L	X	X	Q_0	Q_1	Q_2	Q_3	②	Count Up with $\overline{CEP}$ not active
L	L	H	H	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Up with $\overline{CET}$ not active
L	H	L	L	X	X	X	⎍	$\overline{Q_0}$	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	L	Invert
L	H	L	H	X	X	X	⎍	L	L	L	L	H	Clear
L	H	H	L	X	X	X	⎍	D_0	Q_0	Q_1	Q_2	Q_3	Shift Right
L	H	H	H	X	X	X	X	Q_0	Q_1	Q_2	Q_3	H	Hold
H	L	L	L	X	X	X	X	L	L	L	L	L	Asynchronous Master Reset
H	L	L	H	X	L	X	X	L	L	L	L	L	
H	L	L	H	X	H	X	X	L	L	L	L	H	
H	L	H	L	X	X	X	X	L	L	L	L	L	
H	L	H	H	X	X	X	X	L	L	L	L	H	
H	H	L	L	X	X	X	X	L	L	L	L	L	
H	H	L	H	X	X	X	X	L	L	L	L	H	
H	H	H	L	X	X	X	X	L	L	L	L	L	
H	H	H	H	X	X	X	X	L	L	L	L	H	

① = L if Q_0-Q_3 = LLLL
H if Q_0-$Q_3 \neq$ LLLL
② = L if Q_0-Q_3 = HHHH
H if Q_0-$Q_3 \neq$ HHHH
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
⎍ = LOW-to-HIGH Transition

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current P_n, S_n $\overline{CEP}$ MR D_3 CP $D_0/\overline{CET}$			 180 200 240 280 390 530	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−283	−195	−136	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

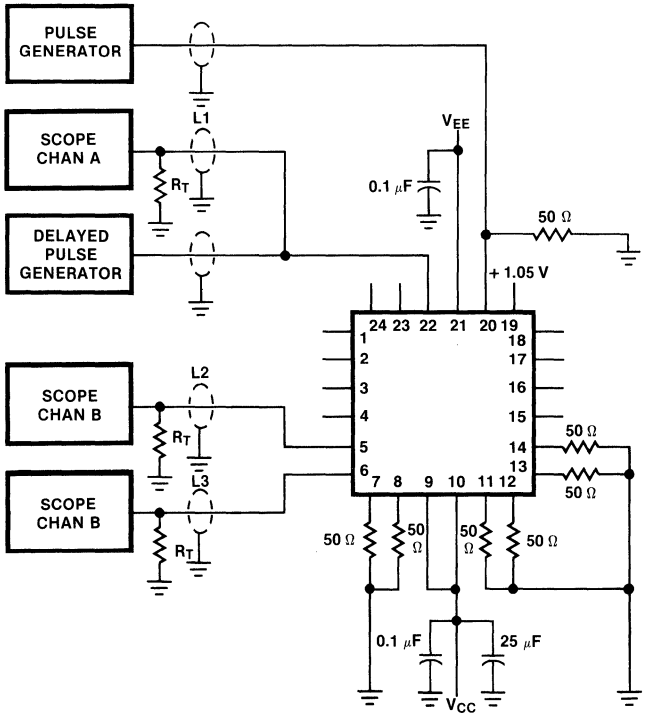
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
f_{shift}	Shift Frequency	250		250		250		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	0.85	2.10	0.85	2.10	0.85	2.25	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	1.90	4.80	1.90	4.60	1.90	5.20	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q}_n$	1.20	2.95	1.35	2.95	1.20	3.10	ns	*Figures 1* and *4*
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$	2.20	4.80	2.20	4.80	2.20	5.30	ns	
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	1.40	3.20	1.40	3.20	1.40	3.50	ns	*Figures 1* and *5*
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	1.70	4.60	1.80	4.60	1.80	5.10	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.80	0.45	1.80	ns	*Figures 1* and *3*
t_s	Setup Time D_3 P_n $D_0/\overline{CET}$, $\overline{CEP}$ S_n MR (Release Time)	 1.20 1.70 1.45 3.30 2.60		 1.20 1.70 1.45 3.30 2.60		 1.20 1.70 1.45 3.30 2.60		ns	*Figure 6*
t_h	Hold Time D_3 P_n $D_0/\overline{CET}$, $\overline{CEP}$ S_n	 0.20 0.10 0.20 −0.90		 0.20 0.10 0.20 −0.90		 0.20 0.10 0.20 −0.90		ns	*Figure 6*
$t_{pw}(H)$	Pulse Width HIGH CP, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*

*See Family Characteristics for other dc specifications.

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
f_{shift}	Shift Frequency	250		250		250		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	0.85	1.90	0.85	1.90	0.85	2.05	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	1.90	4.60	1.90	4.40	1.90	5.00	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q}_n$	1.20	2.75	1.35	2.75	1.20	2.90	ns	*Figures 1* and *4*
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$	2.20	4.60	2.20	4.60	2.20	5.10	ns	
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	1.40	3.00	1.40	3.00	1.40	3.30	ns	*Figures 1* and *5*
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	1.70	4.40	1.80	4.40	1.80	4.90	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.70	ns	*Figures 1* and *3*
t_s	Setup Time D_3 P_n $D_0/\overline{CET}$, $\overline{CEP}$ S_n MR (Release Time)	 1.10 1.60 1.35 3.20 2.50		 1.10 1.60 1.35 3.20 2.50		 1.10 1.60 1.35 3.20 2.50		ns	*Figure 6*
t_h	Hold Time D_3 P_n $D_0/\overline{CET}$, $\overline{CEP}$ S_n	 0.10 0 0.10 −1.00		 0.10 0 0.10 −1.00		 0.10 0 0.10 −1.00		ns	*Figure 6*
$t_{pw}(H)$	Pulse Width HIGH CP, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*

Fig. 1 AC Test Circuit

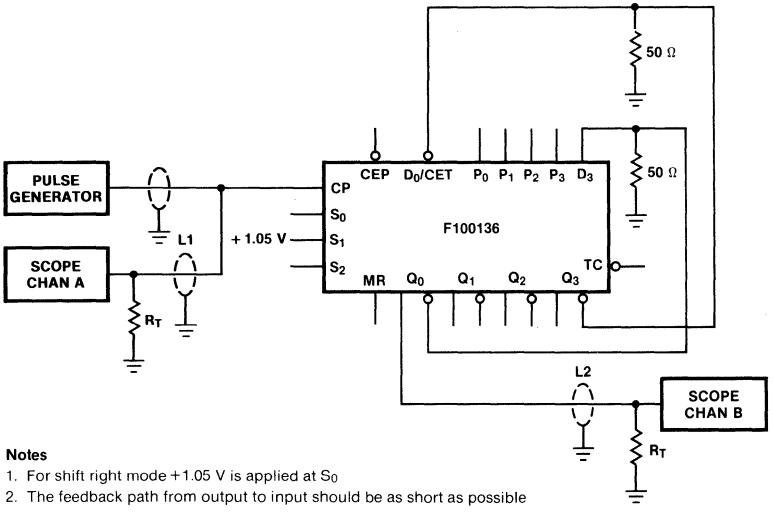


Notes

V_{CC}, V_{CCA} = +2 V, V_{EE} = −2.5 V
L1, L2 and L3 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

3

Fig. 2 Shift Frequency Test Circuit (Shift Left)



Notes

1. For shift right mode +1.05 V is applied at S_0
2. The feedback path from output to input should be as short as possible

Fig. 3 Propagation Delay (Clock) and Transition Times

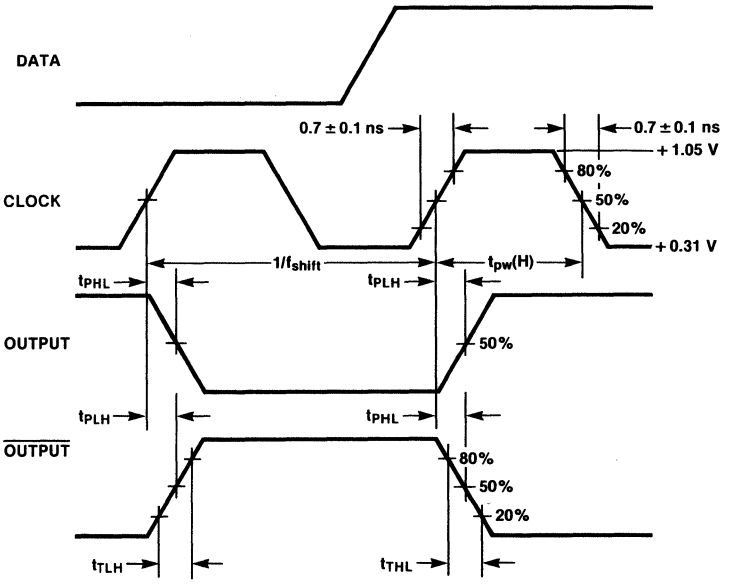


Fig. 4 Propagation Delay (Reset)

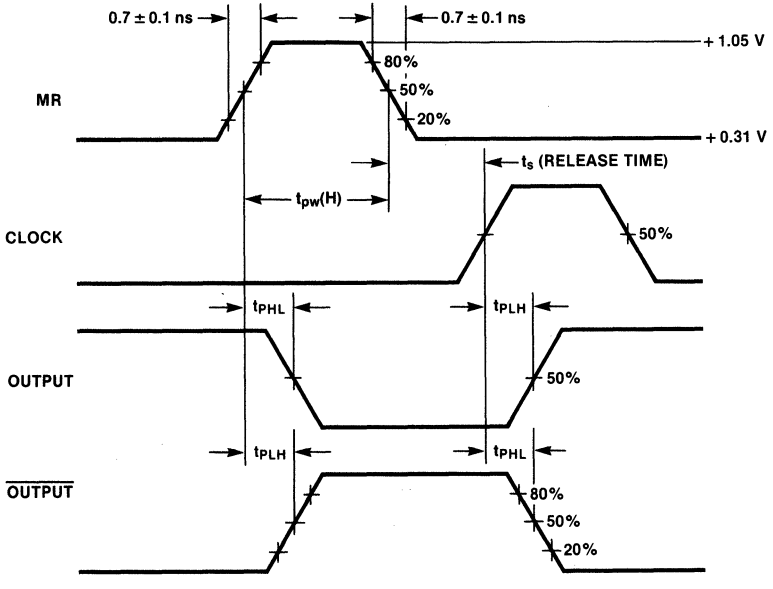


Fig. 5 Propagation Delay (Serial Data, Selects)

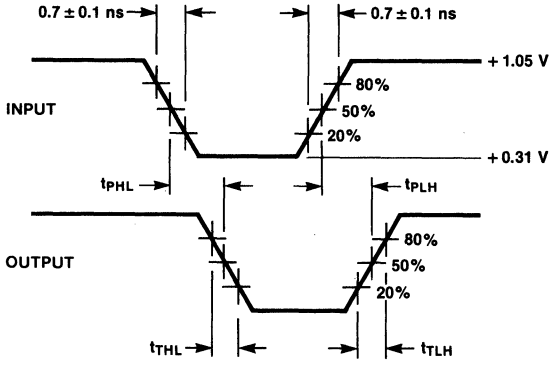
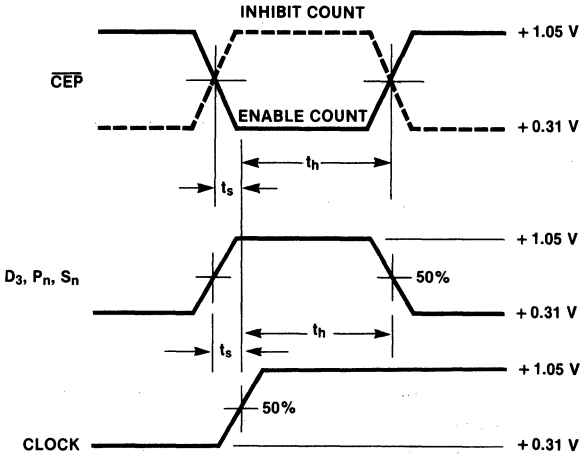


Fig. 6 Setup and Hold Time



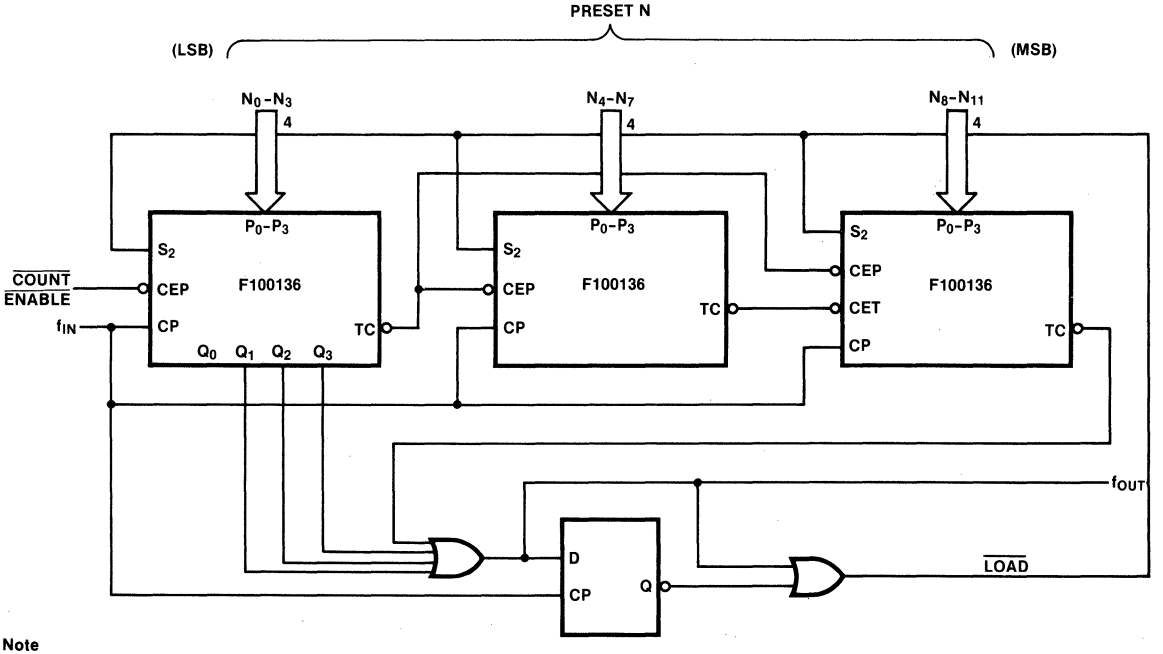
Notes

t_s is the minimum time before the transition of the clock that information must be present at the data input

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input

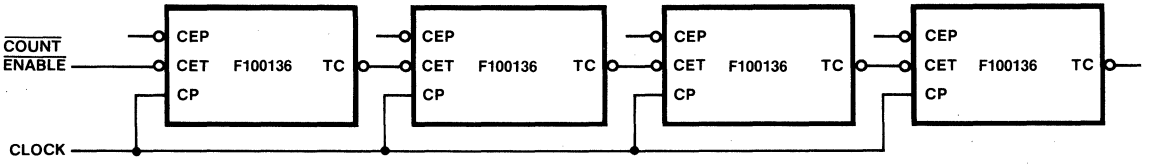
Application

3-Stage Divider, Preset Count Down Mode

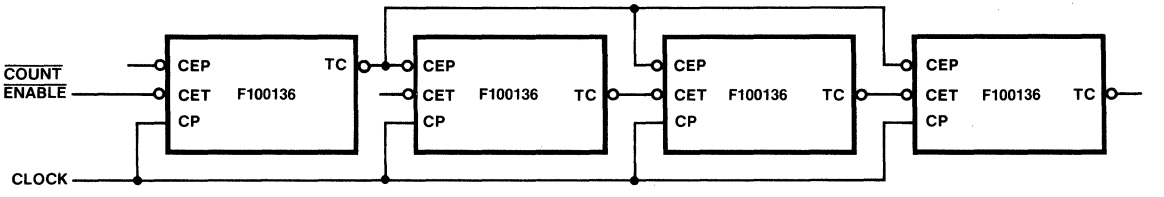


Note
If $S_0 = S_1 = S_2 =$ LOW, then $T_C =$ LOW

Slow Expansion Scheme



Fast Expansion Scheme



F100141
8-Bit Shift Register

F100K ECL Product

Description

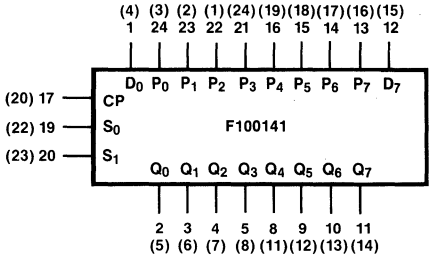
The F100141 contains eight edge-triggered, D-type flip-flops with individual inputs (P_n) and outputs (Q_n) for parallel operation, and with serial inputs (D_n) and steering logic for bidirectional shifting. The flip-flops accept input data a setup time before the positive-going transition of the clock pulse and their outputs respond a propagation delay after this rising clock edge.

The circuit operating mode is determined by the Select inputs S_0 and S_1, which are internally decoded to select either "parallel entry", "hold", "shift left" or "shift right" as described in the Truth Table.

Pin Names

CP	Clock Input
S_0, S_1	Select Inputs
D_0, D_7	Serial Inputs
P_0–P_7	Parallel Inputs
Q_0–Q_7	Data Outputs

Logic Symbol



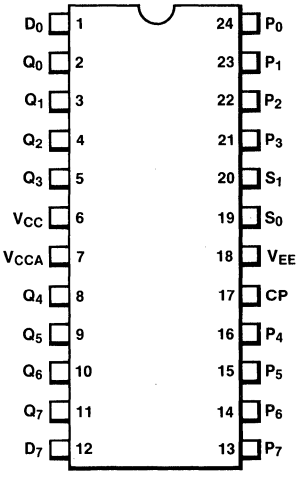
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

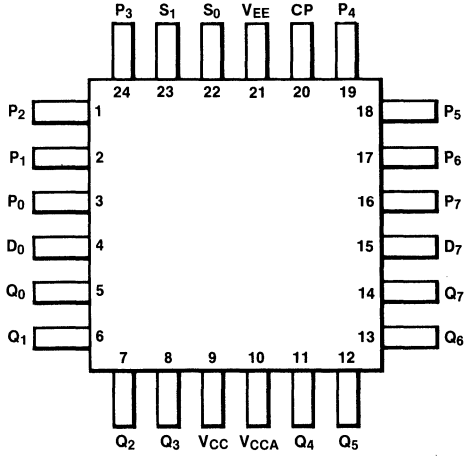
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4Q	FC

Connection Diagrams

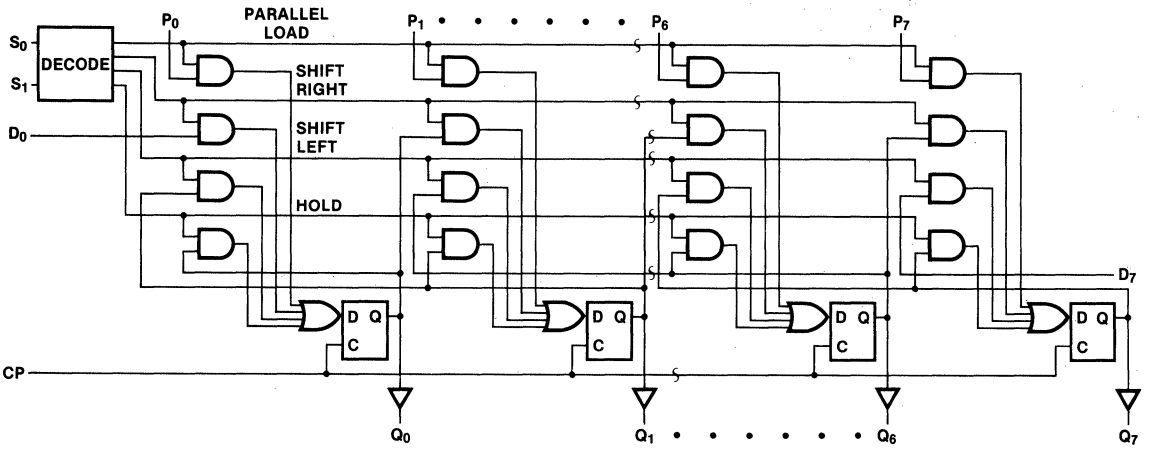
24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Logic Diagram



Truth Table

Function	Inputs					Outputs							
	D_7	D_0	S_1	S_0	CP	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
Load Register	X	X	L	L	⌐¬	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
Shift Left	X	L	L	H	⌐¬	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	L
Shift Left	X	H	L	H	⌐¬	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	H
Shift Right	L	X	H	L	⌐¬	L	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Shift Right	H	X	H	L	⌐¬	H	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Hold	X	X	H	H	X	← No Change →							
Hold	X	X	X	X	H	← No Change →							
Hold	X	X	X	X	L	← No Change →							

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
⌐¬ = LOW-to-HIGH transition

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current D_n, P_n, S_n CP			 220 550	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−238	−170	−119	mA	Inputs Open

*See Family Characteristics for other dc specifications.

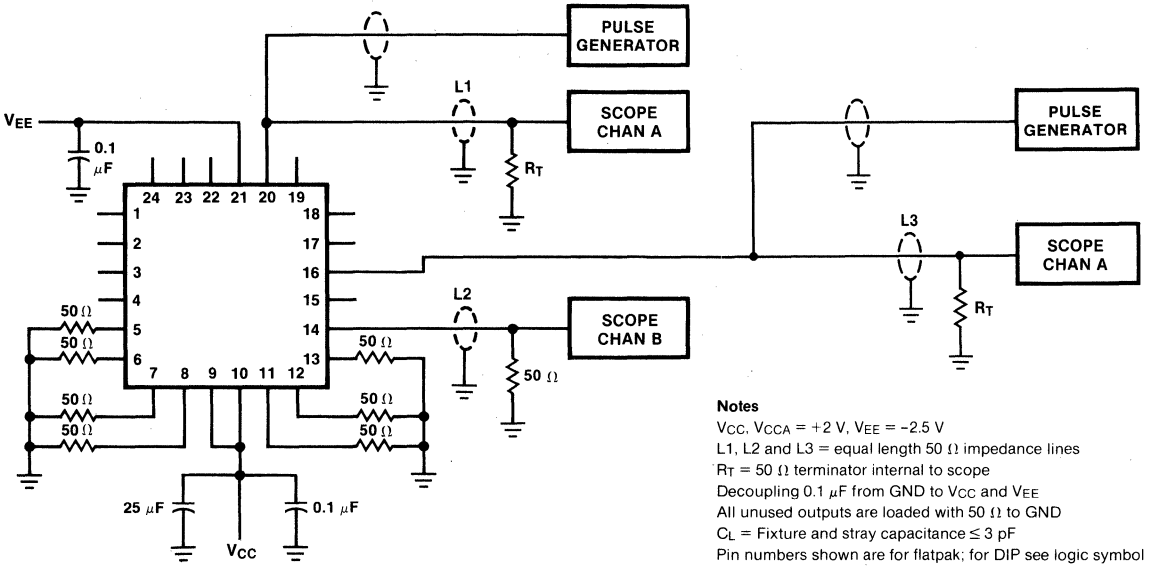
Ceramic Dual In-line Package AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Condition**
f_{shift}	Shift Frequency	275		275		255		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.90	2.40	1.10	2.30	1.10	2.50	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.50	ns	
t_s	Setup Time D_n, P_n S_n	 0.85 2.20		 0.85 2.20		 0.85 2.20		ns	*Figure 4*
t_h	Hold Time D_n, P_n S_n	 0.60 0.10		 0.60 0.10		 0.60 0.10		ns	
$t_{pw}(H)$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figure 3*

Flatpak AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

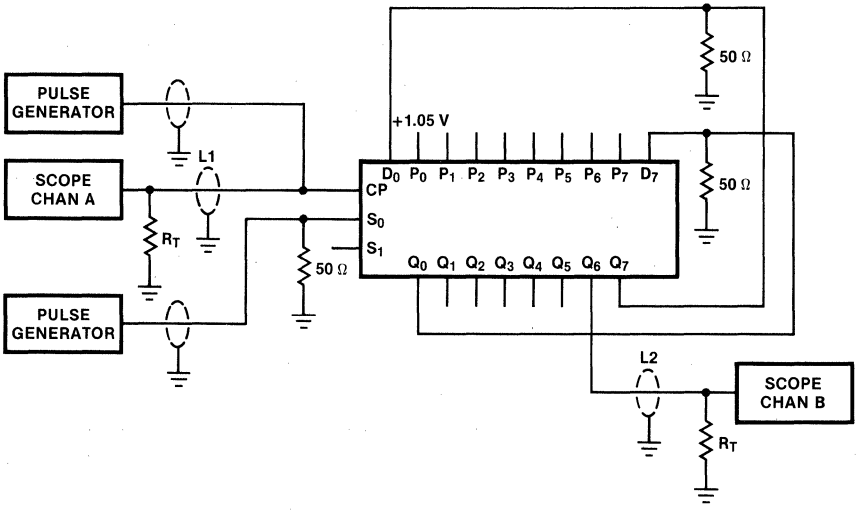
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Condition**
f_{shift}	Shift Frequency	300		300		280		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.90	2.20	1.10	2.10	1.10	2.30	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.40	0.45	1.30	0.45	1.40	ns	
t_s	Setup Time D_n, P_n S_n	 0.75 2.10		 0.75 2.10		 0.75 2.10		ns	*Figure 4*
t_h	Hold Time D_n, P_n S_n	 0.50 0		 0.50 0		 0.50 0		ns	
$t_{pw}(H)$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figure 3*

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = −2.5 V
L1, L2 and L3 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Fig. 2 Shift Frequency Test Circuit (Shift Left)



Notes
1. For shift right mode pulse generator connected to S_0 is moved to S_1.
2. Pulse generator connected to S_1 has a LOW frequency 99% duty cycle, which allows occasional parallel load.
3. The feedback path from output to input should be as short as possible.

Fig. 3 Propagation Delay and Transition Times

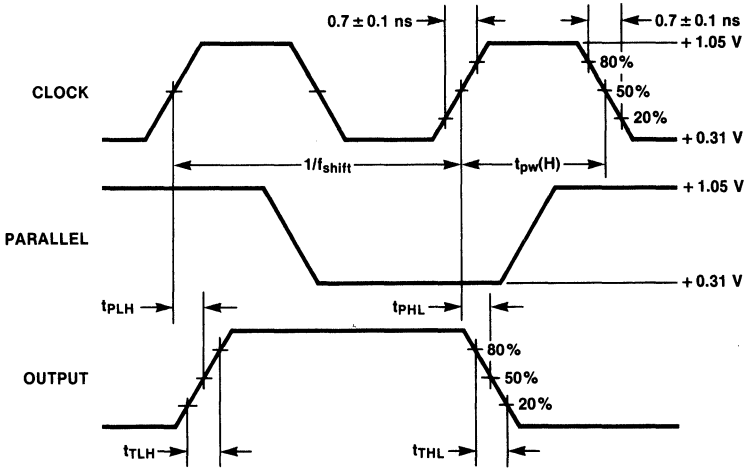
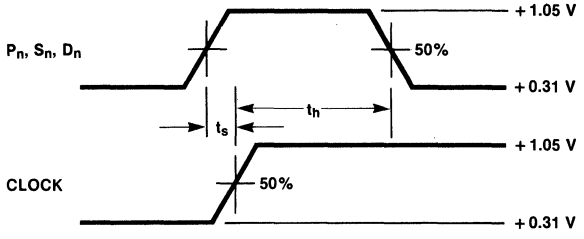


Fig. 4 Setup and Hold Times



Notes

t_s is the minimum time before the transition of the clock that information must be present at the data input

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input

F100142
4 x 4-Bit Content Addressable Memory

F100K ECL Product

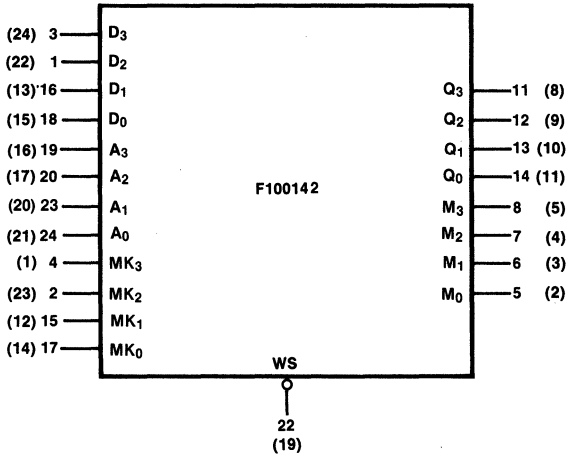
Description

The F100142 is a 4 word x 4-bit Content Addressable Memory (CAM). Each word location has its own address select line. Reading or writing is accomplished when the address select line is LOW. In the Read mode, data from the addressed location appears at the Data (Q_n) outputs. In the Write mode, data is stored in the addressed location. A LOW Write Strobe selects the Read mode. Each Data input has its own Mask input that blocks data storage when the Mask is HIGH. The Data input word is simultaneously compared with each of four memory words. If a search compare results in a match, then the match output will go LOW. A HIGH Mask input on any bit forces a match of that bit. Each input has a 50 k Ω (typical) pull-down resistor tied to V_{EE}.

Pin Names

MK_0–MK_3	Data Mask Inputs
A_0–A_3	Address Inputs
D_0–D_3	Data Inputs
$\overline{WS}$	Write Strobe Input
M_0–M_3	Match Outputs
Q_0–Q_3	Data Outputs

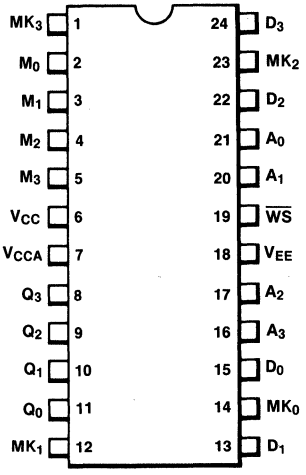
Logic Symbol



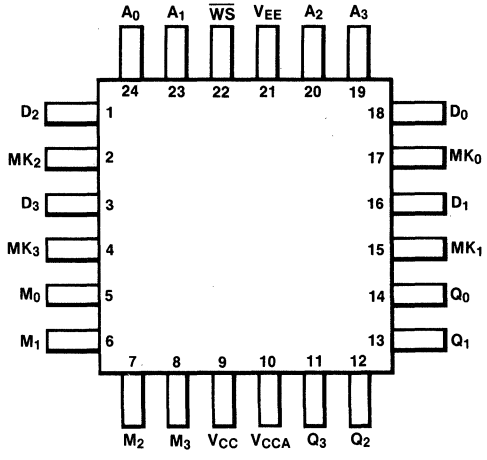
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Connection Diagrams

24-Pin DIP (Top View)



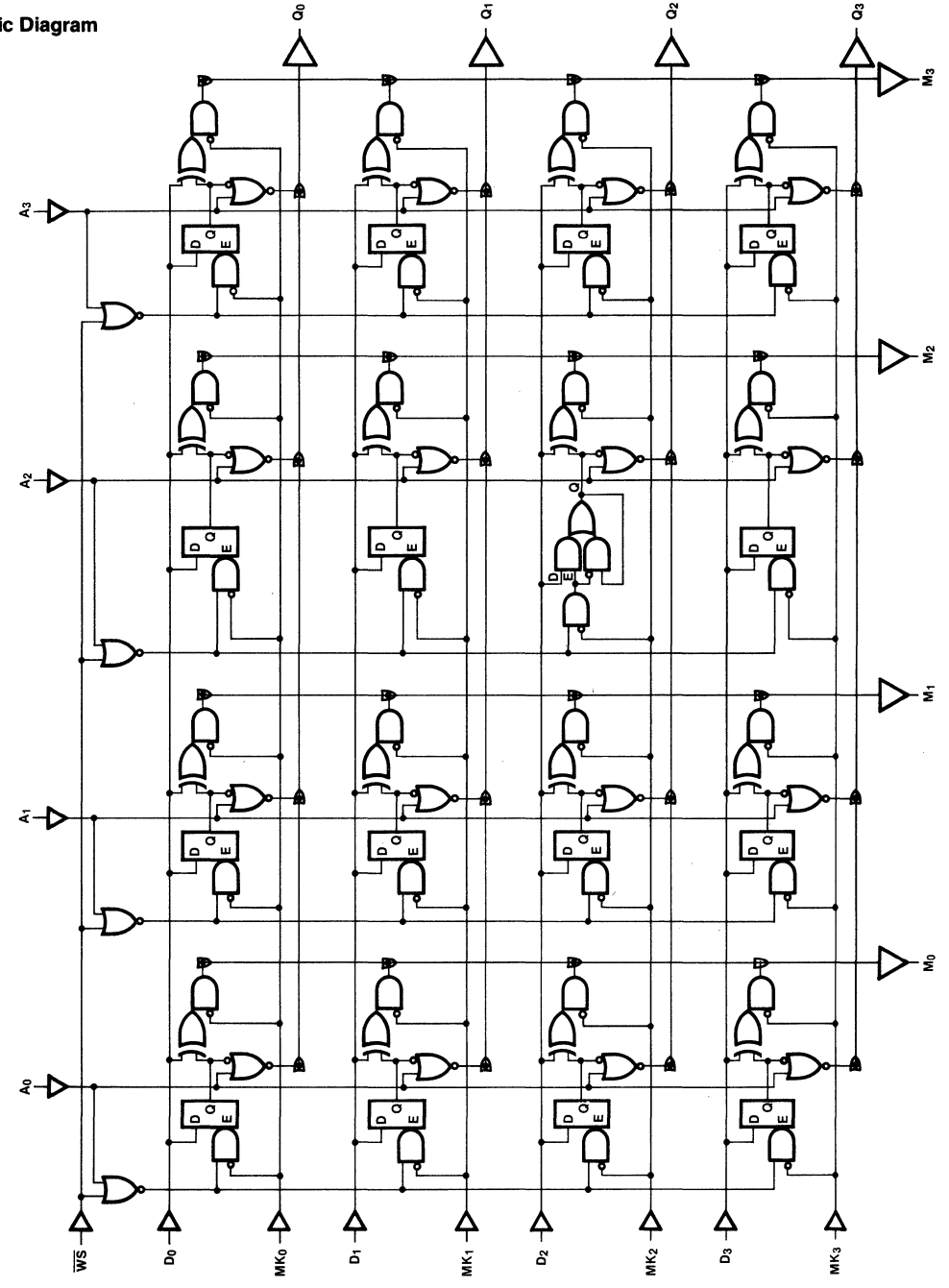
24-Pin Flatpak (Top View)



Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4Q	FC

Logic Diagram



Truth Table

Operation	Inputs				Flip-Flop	Outputs	
	$\overline{WS}$	A_i	D_j	MK_j	Q_{ij}	M_i	Q_j
	$\overline{WS}$	A_0 A_1 A_2 A_3	D_0 D_1 D_2 D_3	MK_0 MK_1 MK_2 MK_3		M_0 M_1 M_2 M_3	Q_0 Q_1 Q_2 Q_3
Write Disabled	X X H	H L L	X X X	X H X	NC NC NC	X L X	L $Q_{ij}n-1$ $Q_{ij}n-1$
Write	L L	L L	H L	L L	H L	L L	H L
Read	H H	L L	X X	X X	H L	X X	H L
Match Masked	H	X	X	H	NC	L	X
Match Not Satisfied	H H H H	L H H L	H H L L	L L L L	L L H H	H H H H	L L L H
Match Satisfied	H H H H	L H H L	H H L L	L L L L	H H L L	L L L L	H L L L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change from Previous State
$\overline{WS}$ = Write Strobe
A_i = Address for ith Word
D_j = Data for jth Bit
MK_j = Data Mask for jth Bit
H = Mask
Q_{ij} = Cell State for ith Word, jth Bit
M_i = Match Output of ith Word
L = True
Q_j = Data Output of jth Bit
Q_{n-1} = Previous Cell State

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current All Inputs			200	μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	−288	−190	−114	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Condition**
t_{AD}	Address to Data Out	1.20	4.40	1.20	4.30	1.20	4.50	ns	*Figures 2* and *3*
t_{DM}	Data In to Match Out Time	1.60	3.70	1.60	3.60	1.60	3.80	ns	*Figure 5*
t_{MM}	Mask In to "Enable Partial" Match Out Time	1.20	3.90	1.20	3.90	1.20	4.00	ns	
t_{DD}	Data In to New Data Out	1.70	4.40	1.70	4.40	1.70	4.60	ns	*Figure 2*
t_{WD}	Write to New Data Out	2.50	5.40	2.50	5.20	2.30	5.10	ns	
t_{AM}	Address to Match	2.50	4.60	2.50	4.60	2.50	4.90	ns	
t_{MD}	Mask to Data	2.20	4.90	2.20	4.80	2.20	5.00	ns	
t_{WSM}	$\overline{WS}$ to Match	2.80	4.90	2.80	4.80	2.80	5.10	ns	
t_W	Write Pulse Width	1.30		1.30		1.30		ns	*Figure 1*
t_{AS}	Address Setup before Write Time	1.40		1.40		1.40		ns	
t_{AH}	Address Hold after Write Time	1.40		1.40		1.40		ns	
t_{DS}	Data In Setup before Write Time	0.60		0.60		0.60		ns	
t_{DH}	Data In Hold after Write Time	1.10		1.10		1.10		ns	
t_{MH}	Mask In Hold Write Time	2.50		2.50		2.50		ns	
t_{MS}	Mask In Setup Write Time	1.10		1.10		1.10		ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	2.30	0.50	2.30	0.50	2.30	ns	*Figure 2*

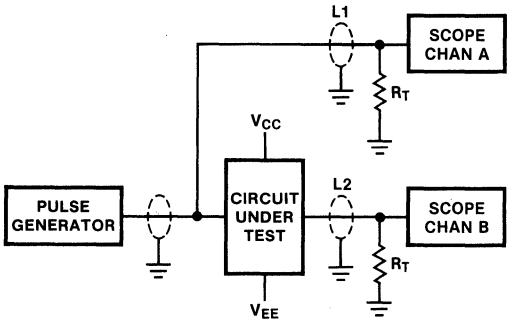
*See Family Characteristics for other dc specifications.

Flatpak AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{AD}	Address to Data Out	1.20	4.20	1.20	4.10	1.20	4.30	ns	*Figures 2* and *3*
t_{DM}	Data In to Match Out Time	1.60	3.50	1.60	3.40	1.60	3.60	ns	*Figure 5*
t_{MM}	Mask In to "Enable Partial" Match Out Time	1.20	3.70	1.20	3.70	1.20	3.80	ns	
t_{DD}	Data In to New Data Out	1.70	4.20	1.70	4.20	1.70	4.40	ns	*Figure 2*
t_{WD}	Write to New Data Out	2.50	5.20	2.50	5.00	2.30	4.90	ns	
t_{AM}	Address to Match	2.50	4.40	2.50	4.40	2.50	4.70	ns	
t_{MD}	Mask to Data	2.20	4.70	2.20	4.60	2.20	4.80	ns	
t_{WSM}	$\overline{WS}$ to Match	2.80	4.70	2.80	4.60	2.80	4.90	ns	
t_W	Write Pulse Width	1.20		1.20		1.20		ns	*Figure 1*
t_{AS}	Address Setup before Write Time	1.30		1.30		1.30		ns	
t_{AH}	Address Hold after Write Time	1.30		1.30		1.30		ns	
t_{DS}	Data In Setup before Write Time	0.50		0.50		0.50		ns	
t_{DH}	Data In Hold after Write Time	1.00		1.00		1.00		ns	
t_{MH}	Mask In Hold Write Time	2.40		2.40		2.40		ns	
t_{MS}	Mask In Setup Write Time	1.00		1.00		1.00		ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	2.20	0.50	2.20	0.50	2.20	ns	*Figure 2*

Switching Waveforms

Fig. 1 AC Test Circuit



Notes

V_{CC}, V_{CCA} = +2 V, V_{EE} = −2.5 V
L1, L2 and L3 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Fig. 2 Output Rise and Fall Times and Waveforms

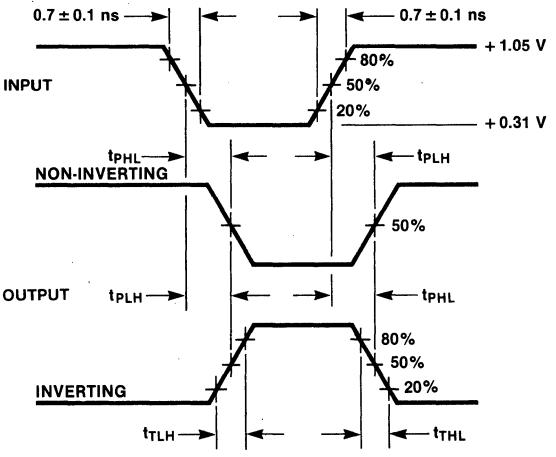


Fig. 3 Write Mode and Read/Write Mode Waveforms

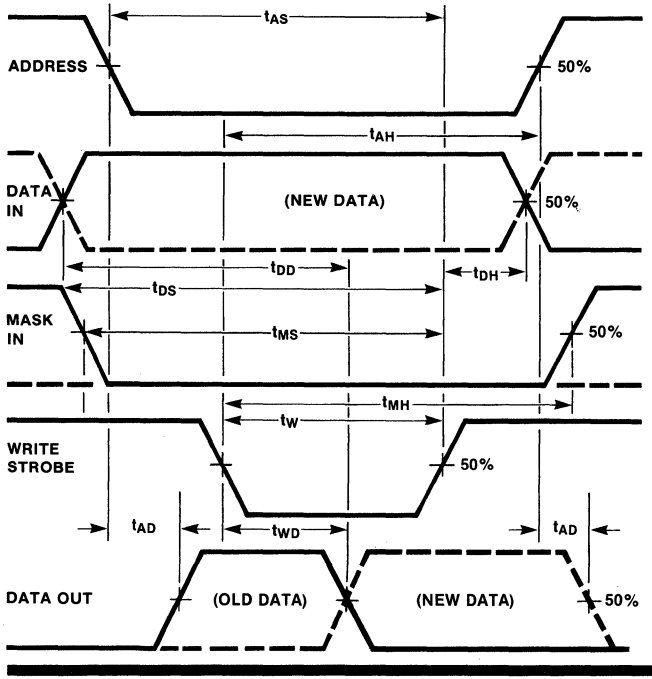


Fig. 4 Read Mode Waveforms

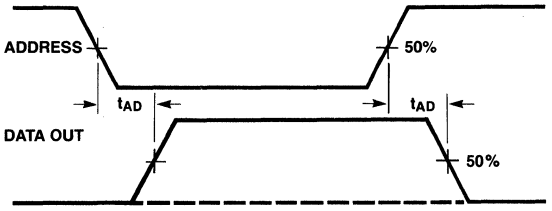
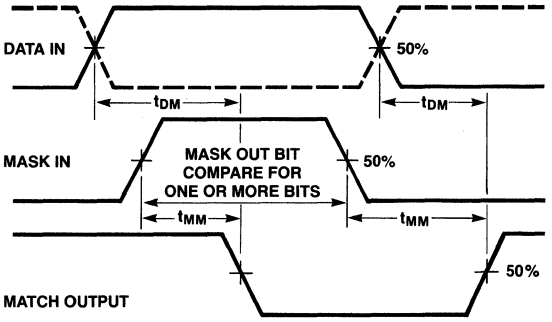


Fig. 5 Search Mode Waveforms



F100145
16 x 4-Bit Read/Write Register File

F100K ECL Product

Description

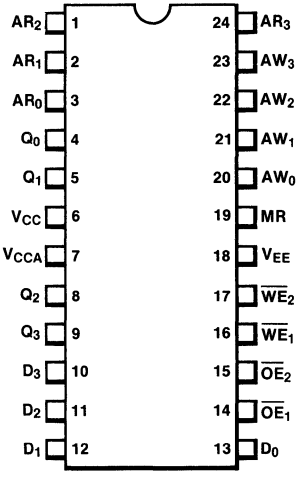
The F100145 is a 64-bit register file organized as 16 words of four bits each. Separate address inputs for Read (AR_n) and Write (AW_n) operations reduce overall cycle time by allowing one address to be setting up while the other is being executed. Operating speed is also enhanced by four output latches which store data from the previous read operation while writing is in progress. When both Write Enable ($\overline{WE}$) inputs are LOW, the circuit is in the Write mode and the latches are in a Hold mode. When either $\overline{WE}$ input is HIGH, the circuit is in the Read mode, but the outputs can be forced LOW by a HIGH signal on either of the Output Enable ($\overline{OE}$) inputs. This makes it possible to tie one $\overline{WE}$ input and one $\overline{OE}$ input together to serve as an active-LOW Chip Select ($\overline{CS}$) input. When this wired $\overline{CS}$ input is HIGH, reading will still take place internally and the resulting data will enter the latches and become available as soon as the $\overline{CS}$ signal goes LOW, provided that the other $\overline{OE}$ input is LOW. A HIGH signal on the Master Reset (MR) input overrides all other inputs, clears all cells in the memory, resets the output latches, and forces the outputs LOW.

Pin Names

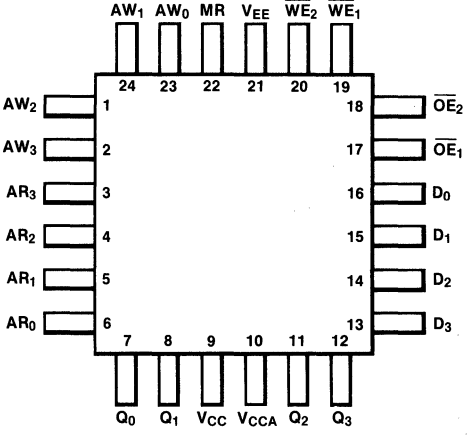
AR_0-AR_3	Read Address Inputs
AW_0-AW_3	Write Address Inputs (Active LOW)
$\overline{WE_1}$, $\overline{WE_2}$	Read Enable Inputs (Active LOW)
$\overline{OE_1}$, $\overline{OE_2}$	Output Enable Inputs (Active LOW)
D_0-D_3	Data Inputs
MR	Master Reset Input
Q_0-Q_3	Data Outputs

Connection Diagrams

24-Pin DIP (Top View)



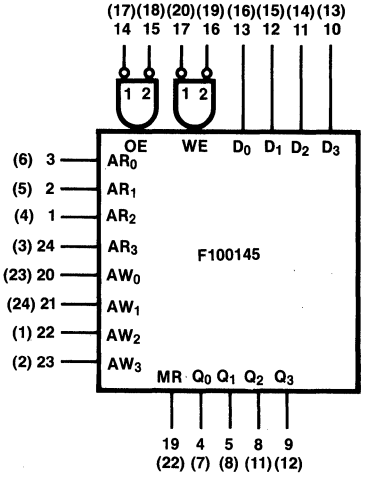
24-Pin Flatpak (Top View)



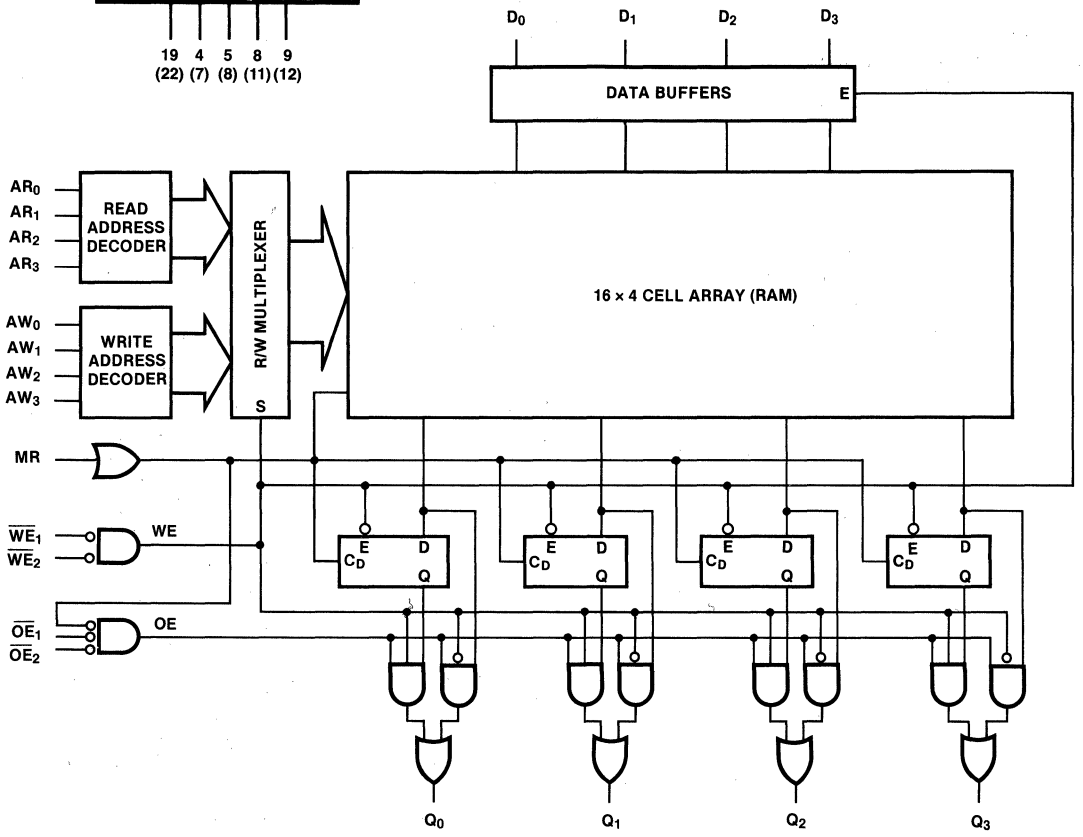
Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Logic Symbol and Logic Diagram



V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many internal functions are achieved more efficiently than indicated.

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current All Inputs			240	μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	−247	−170	−119	mA	Inputs Open

*See Family Characteristics for other dc specifications.

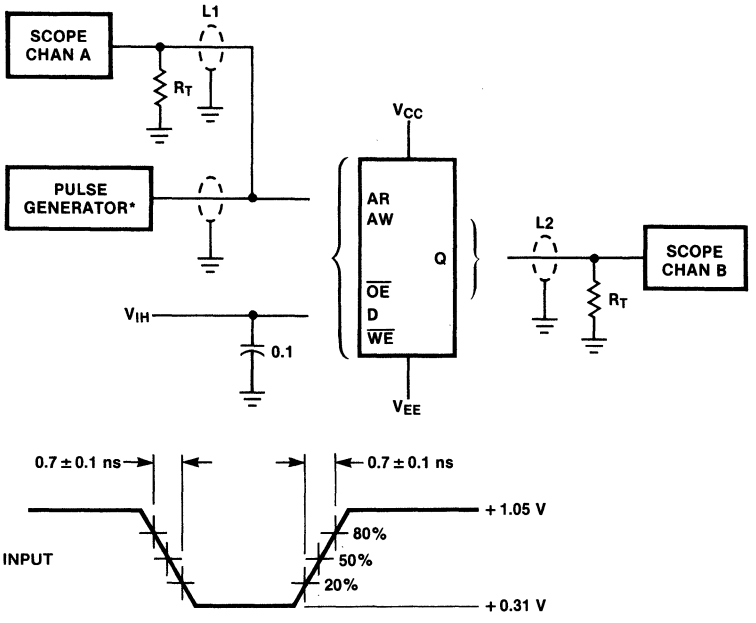
Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Condition**
	Access/Recovery Timing								
t_{AA}	Address Access	2.20	6.70	2.20	6.70	2.20	7.40	ns	*Figures 1* and *2a*
t_{OR}	Output Recivery	1.00	2.90	1.10	2.90	1.10	3.20	ns	*Figures 1* and *2e*
t_{OD}	Output Disable	1.00	2.90	1.10	2.90	1.10	3.20	ns	
	Read Timing								
t_{RSA1}	Address Setup	1.10		1.10		1.10		ns	*Figures 1* and *2b*
t_{WEQ}	Output Delay	2.00	6.10	2.00	6.10	2.00	6.60	ns	
	Output Latch Timing								
t_{RSA2}	Address Setup	4.10		4.10		5.60		ns	*Figures 1* and *2c*
t_{RHA}	Address Hold	0.10		0.10		0.10		ns	*Figures 1* and *2d*
	Write Timing								
t_{WSA}	Address Setup	0.10		0.10		0.10		ns	
t_{WHA}	Address Hold	1.10		1.60		1.60		ns	
t_{WSD}	Data Setup	4.10		5.60		8.30		ns	t_W = 6.0 ns
t_{WHD}	Data Hold	1.10		1.60		1.90		ns	*Figures 1* and *3*
t_W	Write Pulse Width, LOW	4.60		6.60		11.60		ns	
	Master Reset Timing								
t_M	Reset Pulse Width, LOW	5.60		5.60		7.60		ns	*Figures 1* and *4a*
t_{MHW}	$\overline{WE}$ Hold to Write	6.30		7.10		10.50		ns	
t_{MQ}	Output Disable	2.80		2.80		3.20		ns	*Figures 1* and *4b*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	2.30	0.50	2.30	0.50	2.30	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
	Access/Recovery Timing								
t_{AA}	Address Access	2.20	6.50	2.20	6.50	2.20	7.20	ns	*Figures 1* and *2a*
t_{OR}	Output Recivery	1.00	2.70	1.10	2.70	1.10	3.00	ns	*Figures 1* and *2e*
t_{OD}	Output Disable	1.00	2.70	1.10	2.70	1.10	3.00	ns	
	Read Timing								
t_{RSA1}	Address Setup	1.00		1.00		1.00		ns	*Figures 1* and *2b*
t_{WEQ}	Output Delay	2.00	5.90	2.00	5.90	2.00	6.40	ns	
	Output Latch Timing								
t_{RSA2}	Address Setup	4.00		4.00		5.50		ns	*Figures 1* and *2c*
t_{RHA}	Address Hold	0		0		0		ns	*Figures 1* and *2d*
	Write Timing								
t_{WSA}	Address Setup	0		0		0		ns	
t_{WHA}	Address Hold	1.00		1.50		1.50		ns	
t_{WSD}	Data Setup	4.00		5.50		8.20		ns	t_W = 6.0 ns
t_{WHD}	Data Hold	1.00		1.50		1.80		ns	*Figures 1* and *3*
t_W	Write Pulse Width, LOW	4.50		6.50		11.50		ns	
	Master Reset Timing								
t_M	Reset Pulse Width, LOW	5.50		5.50		7.50		ns	*Figures 1* and *4a*
t_{MHW}	$\overline{WE}$ Hold to Write	6.20		7.00		10.40		ns	
t_{MQ}	Output Disable	2.60		2.60		3.00		ns	*Figures 1* and *4b*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	2.20	0.50	2.20	0.50	2.20	ns	

Fig. 1 AC Test Circuit

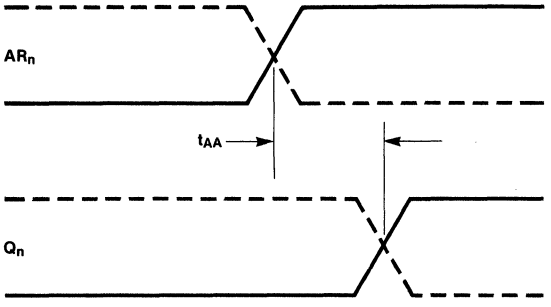


Notes

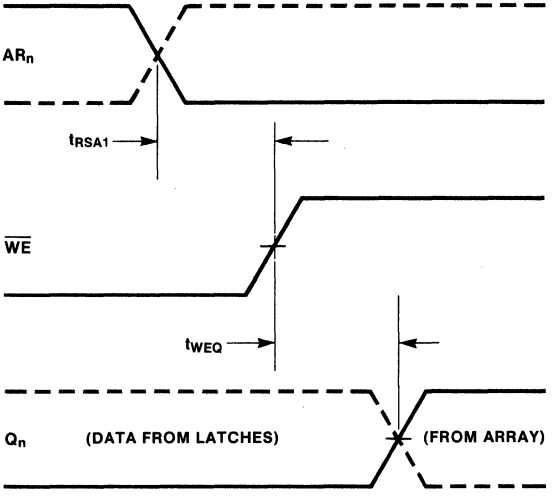
V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Fig. 2 Read Timing

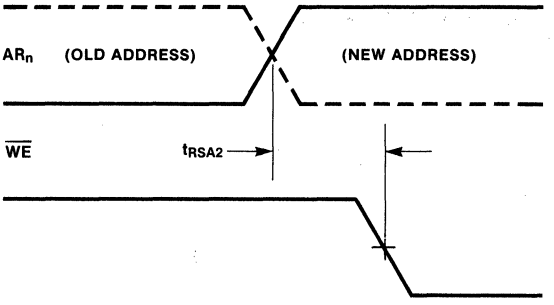
2a Address Access Time ($\overline{WE_1}$ or $\overline{WE_2}$ = HIGH; $\overline{OE_1}$ = $\overline{OE_2}$ = LOW)



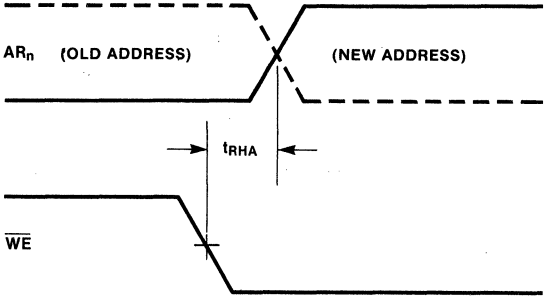
2b Address Setup Time before $\overline{WE}$, to Ensure Minimum Delay (unpulsed $\overline{WE}$= $\overline{OE_1}$ = $\overline{OE_2}$ = LOW)



2c Address Setup Time to Ensure Latching Data from New Address (unpulsed $\overline{WE}$ = LOW)



2d Address Hold Time to Ensure Latching Data from Old Address (unpulsed $\overline{WE}$ = LOW)



2e Output Recovery/Disable Times, $\overline{OE}$ to Qn (unpulsed $\overline{OE}$ = LOW)

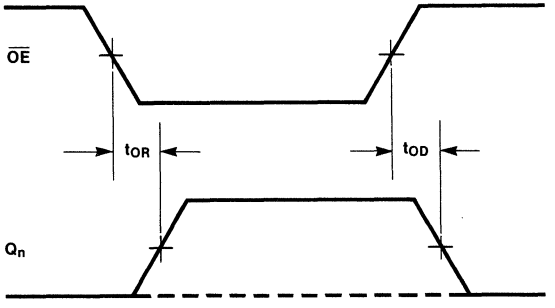


Fig. 3 Write Timing

Address and Data Setup and Hold Times; Write pulse Width (unpulsed $\overline{WE}$ = LOW)

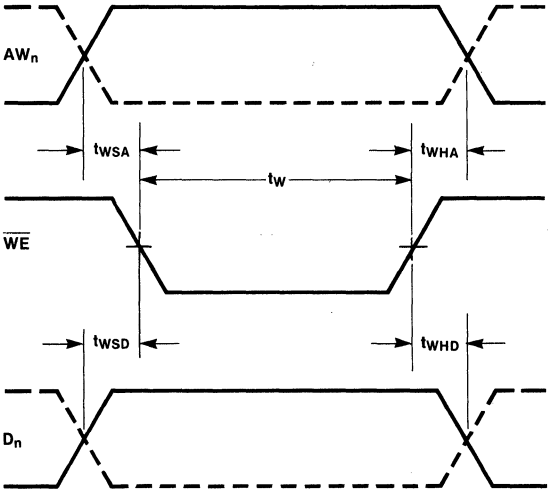
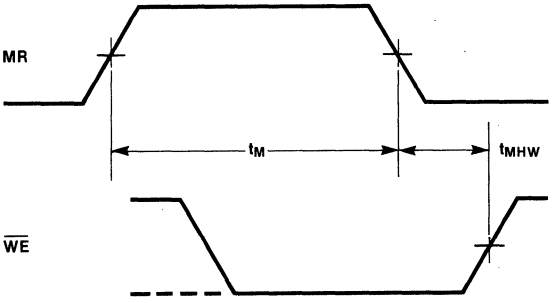
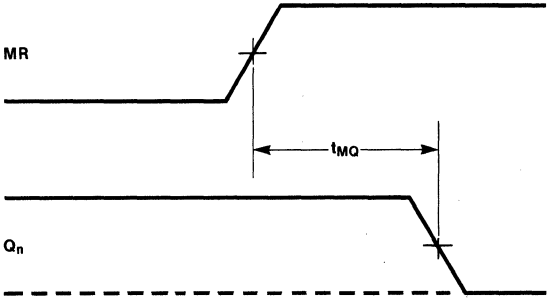


Fig. 4 Master Reset Timing

4a Reset Pulse Width; $\overline{WE}$ Hold Time for Subsequent Writing (address already setup, unpulsed $\overline{WE}$ = LOW)



4b Output Reset Delay, MR to Q_n



F100150
Hex D Latch

F100K ECL Product

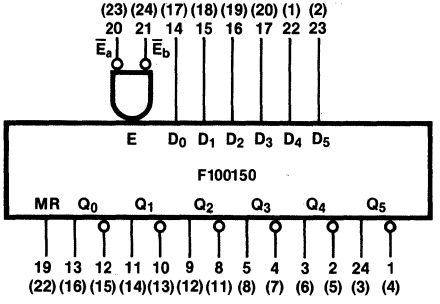
Description

The F100150 contains six D-type latches with true and complement outputs, a pair of Common Enables ($\overline{E}_a$ and $\overline{E}_b$), and a common Master Reset (MR). A Q output follows its D input when both $\overline{E}_a$ and $\overline{E}_b$ are LOW. When either $\overline{E}_a$ or $\overline{E}_b$ (or both) are HIGH, a latch stores the last valid data present on its D input before $\overline{E}_a$ or $\overline{E}_b$ went HIGH. The MR input overrides all other inputs and makes the Q outputs LOW.

Pin Names

D_0–D_5	Data Inputs
$\overline{E}_a$, $\overline{E}_b$	Common Enable Inputs (Active LOW)
MR	Asynchronous Master Reset Input
Q_0–Q_5	Data Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Complementary Data Outputs

Logic Symbol



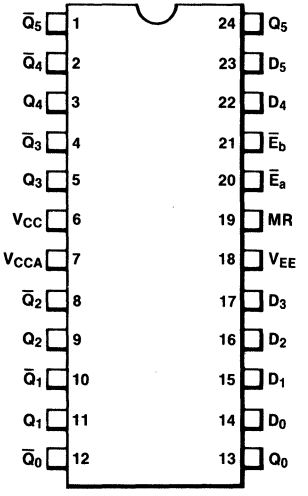
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

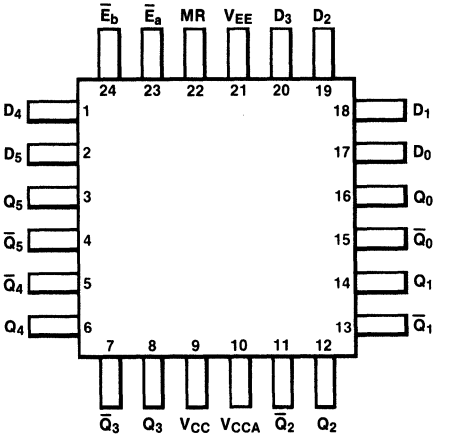
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4Q	FC

Connection Diagrams

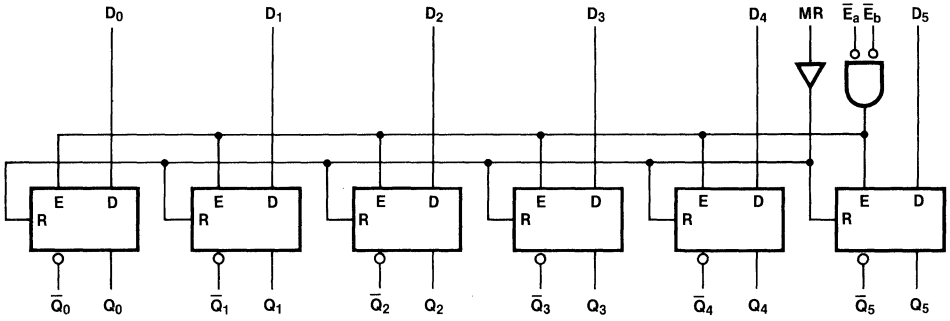
24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Logic Diagram



Truth Tables (Each Latch)

Latch Operation

Inputs				Outputs
D_n	$\overline{E}_a$	$\overline{E}_b$	MR	Q_n
L	L	L	L	L
H	L	L	L	H
X	H	X	L	Latched*
X	X	H	L	Latched*

Asynchronous Operation

Inputs				Outputs
D_n	$\overline{E}_a$	$\overline{E}_b$	MR	Q_n
X	X	X	H	L

*Retains data present before $\overline{E}$ positive transition
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current MR D_n $\overline{E}_a$, $\overline{E}_b$			 450 340 520	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−159	−113	−79	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

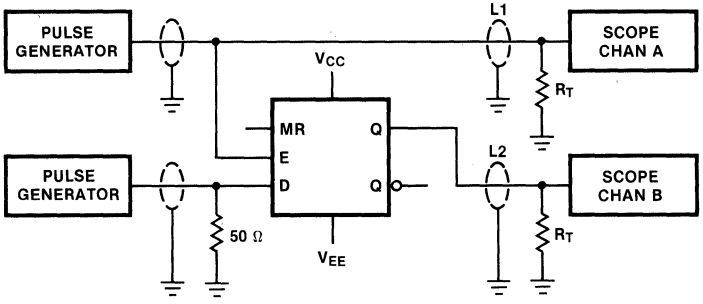
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay D_n to Output (Transparent Mode)	0.45	1.50	0.50	1.40	0.50	1.50	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_a$, $\overline{E}_b$ to Output	0.75	2.05	0.75	1.85	0.75	2.05	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.80	2.40	0.90	2.40	0.90	2.60	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.60	0.45	1.60	ns	*Figures 1* and *2*
t_s	Setup Time D_0-D_5 MR (Release Time)	 0.70 2.10		 0.70 2.10		 0.70 2.10		ns	*Figures 3* and *4*
t_h	Hold Time D_0-D_5	0.70		0.70		0.70		ns	*Figure 4*
$t_{pw}(L)$	Pulse Width LOW $\overline{E}_a$, $\overline{E}_b$	2.00		2.00		2.00		ns	*Figure 2*
$t_{pw}(H)$	Pulse Width HIGH MR	2.00		2.00		2.00		ns	*Figure 3*

*See Family Characteristics for other dc specifications.

Flatpak AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output (Transparent Mode)	0.45	1.30	0.50	1.20	0.50	1.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_a$, $\overline{E}_b$ to Output	0.75	1.85	0.75	1.65	0.75	1.85	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.80	2.20	0.90	2.20	0.90	2.40	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.50	0.45	1.50	ns	*Figures 1* and *2*
t_s	Setup Time D_0-D_5 MR (Release Time)	0.60 2.00		0.60 2.00		0.60 2.00		ns	*Figures 3* and *4*
t_h	Hold Time D_0-D_5	0.60		0.60		0.60		ns	*Figure 4*
$t_{pw}(L)$	Pulse Width LOW $\overline{E}_a$, $\overline{E}_b$	2.00		2.00		2.00		ns	*Figure 2*
$t_{pw}(H)$	Pulse Width HIGH MR	2.00		2.00		2.00		ns	*Figure 3*

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Fig. 2 Enable Timing

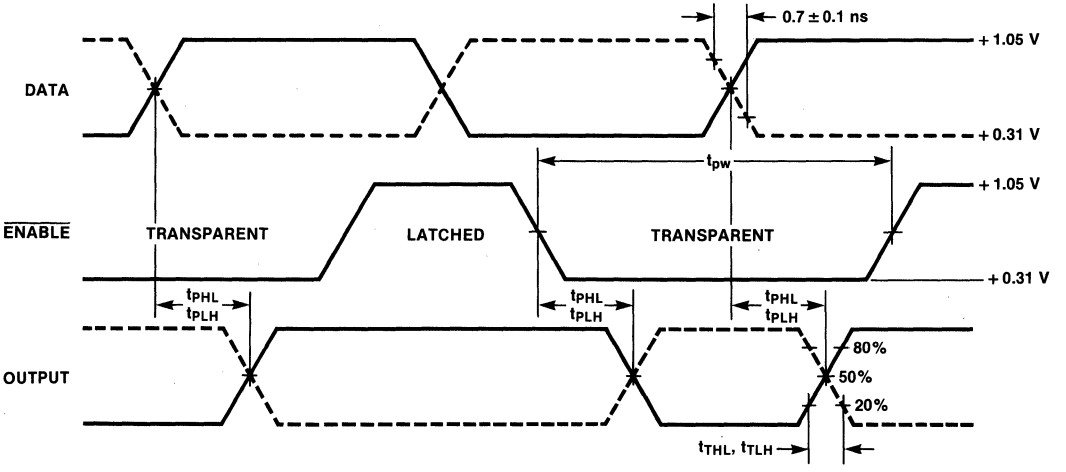


Fig. 3 Reset Timing

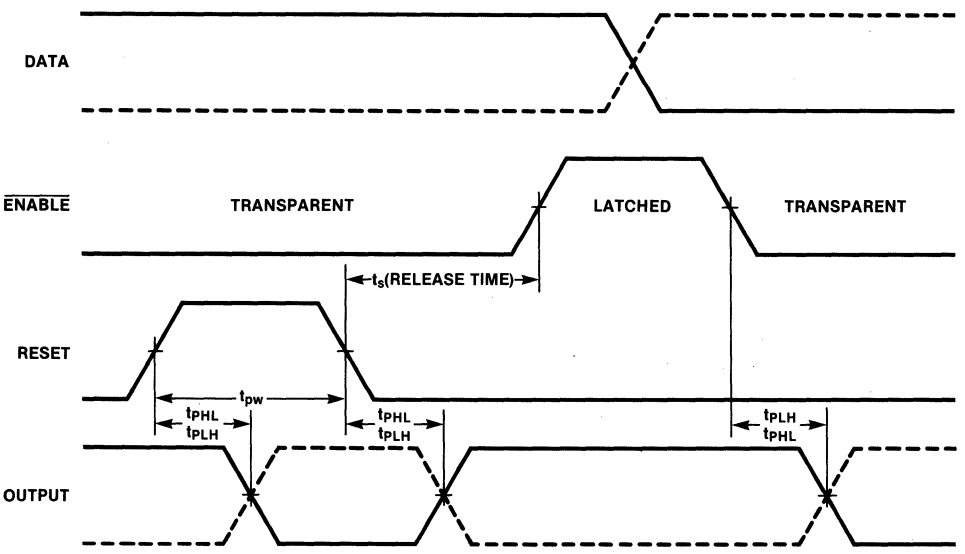
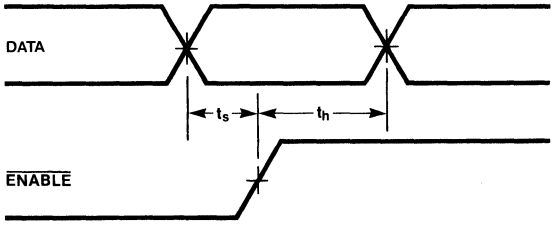


Fig. 4 Data Setup and Hold Time



Notes

t_s is the minimum time before the transition of the enable that information must be present at the data input.

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

F100151
Hex D Flip-Flop

F100K ECL Product

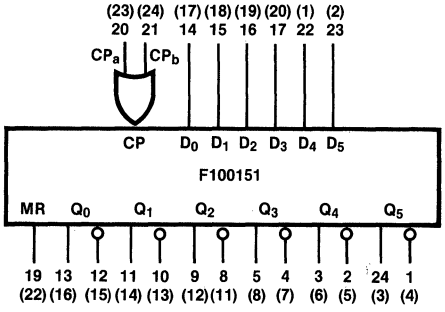
Description

The F100151 contains six D-type edge-triggered, master/slave flip-flops with true and complement outputs, a pair of Common Clock inputs (CP_a and CP_b) and common Master Reset (MR) input. Data enters a master when both CP_a and CP_b are LOW and transfers to the slave when CP_a and CP_b (or both) go HIGH. The MR input overrides all other inputs and makes the Q outputs LOW.

Pin Names

D_0–D_5	Data Inputs
CP_a, CP_b	Common Clock Inputs
MR	Asynchronous Master Reset Input
Q_0–Q_5	Data Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Complementary Data Outputs

Logic Symbol



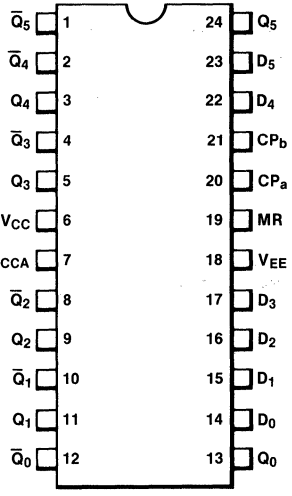
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

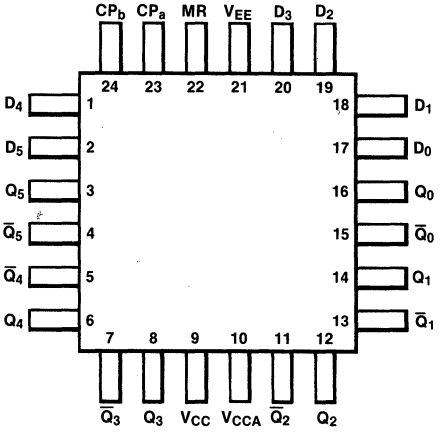
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4Q	FC

Connection Diagrams

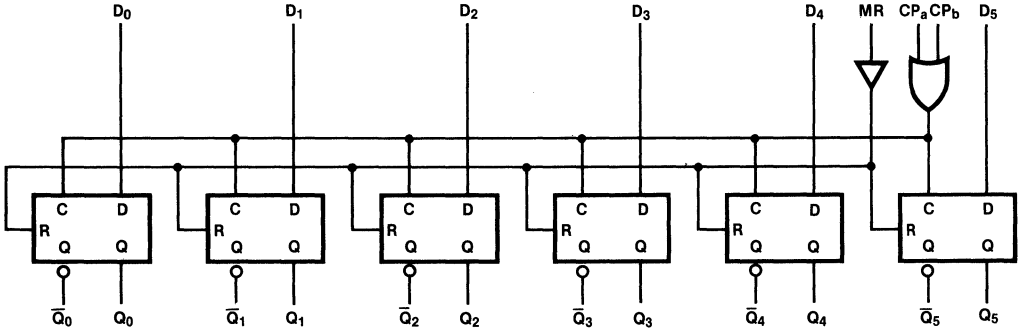
24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Logic Diagram



Truth Tables (Each Flip-flop)

Synchronous Operation

Inputs				Outputs
D_n	CP_a	CP_b	MR	$Q_n(t+1)$
L	⌐	L	L	L
H	⌐	L	L	H
L	L	⌐	L	L
H	L	⌐	L	H
X	H	⌐	L	$Q_n(t)$
X	⌐	H	L	$Q_n(t)$
X	L	L	L	$Q_n(t)$

Asynchronous Operation

Inputs				Outputs
D_n	CP_a	CP_b	MR	$Q_n(t+1)$
X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
t = Time before CP positive transition
t+1 = Time after CP positive transition
⌐ = LOW-to-HIGH transition

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current MR D_0–D_5 CP_a, CP_b			 450 225 520	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−210	−155	−98	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
f_{max}	Toggle Frequency	375		375		375		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	0.80	2.20	0.80	2.20	0.90	2.40	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay MR to Output	1.20	2.90	1.30	3.00	1.20	3.10	ns	*Figures 1* and *4*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.70	0.45	1.80	ns	*Figures 1* and *3*
t_s	Setup Time D_0–D_5 MR (Release Time)	 0.70 2.30		 0.70 2.30		 0.70 2.60		ns	*Figure 5* *Figure 4*
t_h	Hold Time D_0–D_5	0.70		0.70		0.70		ns	*Figure 5*
t_{pw}(H)	Pulse Width HIGH CP_a, CP_b, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*

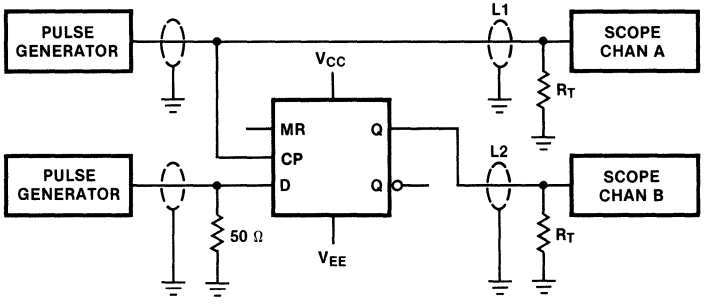
*See Family Characteristics for other dc specifications.

Flatpak AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	375		375		375		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	0.80	2.00	0.80	2.00	0.90	2.20	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay MR to Output	1.20	2.70	1.30	2.80	1.20	2.90	ns	*Figures 1* and *4*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.60	0.45	1.70	ns	*Figures 1* and *3*
t_s	Setup Time D_0-D_5 MR (Release Time)	0.60 2.20		0.60 2.20		0.60 2.50		ns	*Figure 5* *Figure 4*
t_h	Hold Time D_0-D_5	0.60		0.60		0.60		ns	*Figure 5*
$t_{pw}(H)$	Pulse Width HIGH CP_a, CP_b, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*

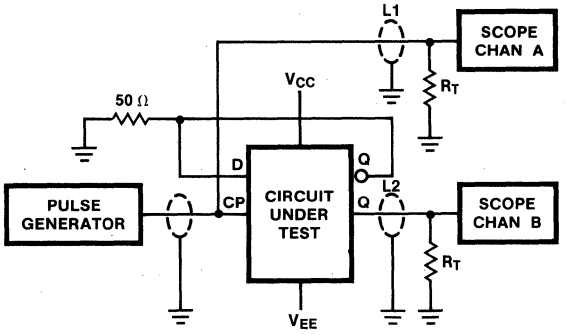
*See Family Characteristics for other dc specifications.

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Fig. 2 Toggle Frequency Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = −2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Jig and stray capacitance ≤ 3 pF

Fig. 3 Propagation Delay (Clock) and Transition Times

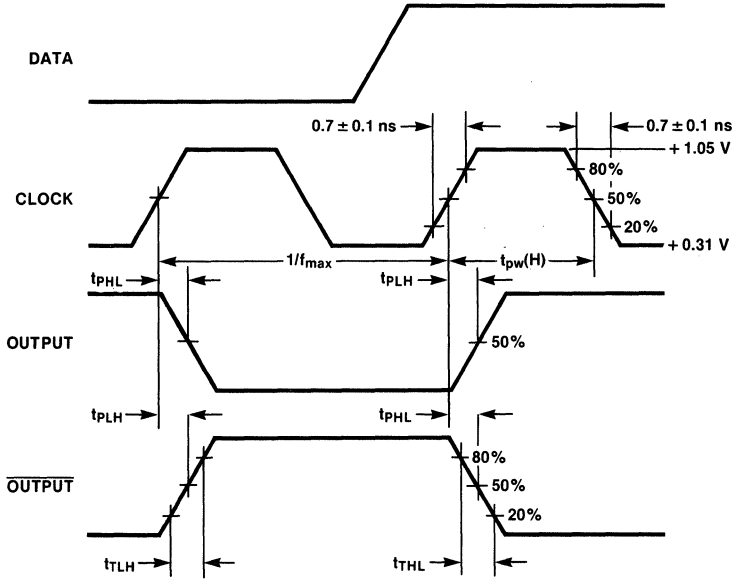


Fig. 4 Propagation Delay (Reset)

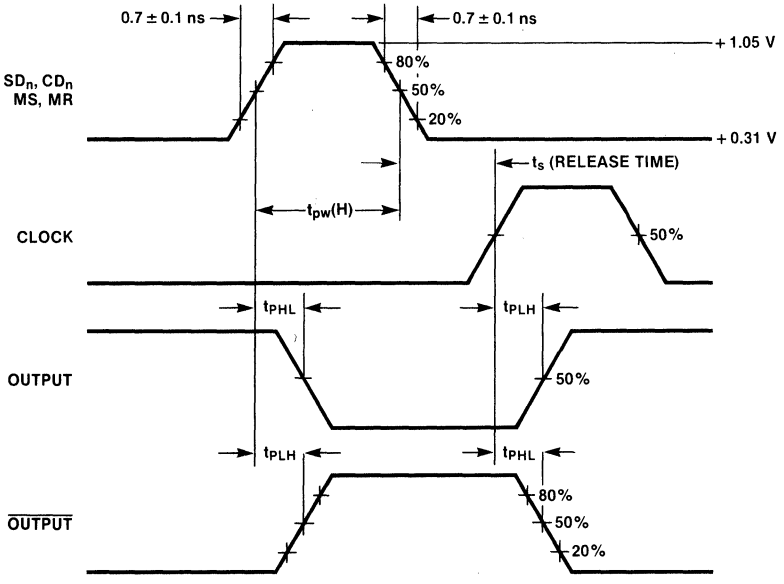
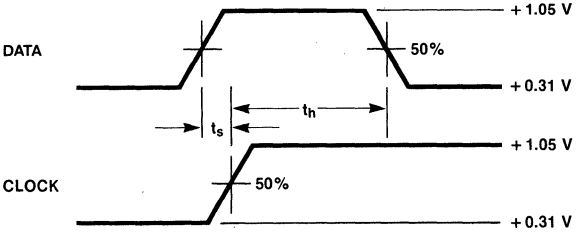


Fig. 5 Setup and Hold Time



Notes

t_s is the minimum time before the transition of the clock that information must be present at the data input

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input

F100155
Quad Multiplexer/Latch

F100K ECL Product

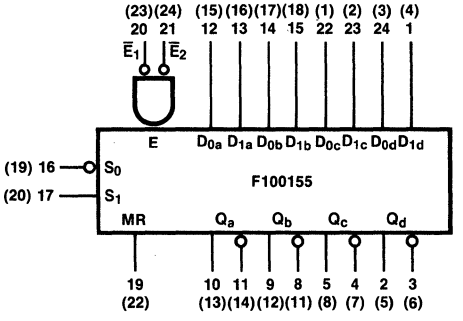
Description

The F100155 contains four transparent latches, each of which can accept and store data from two sources. When both Enable ($\overline{E}_n$) inputs are LOW, the data that appears at an output is controlled by the Select (S_n) inputs, as shown in the Operating Mode table. In addition to routing data from either D_0 or D_1, the Select inputs can force the outputs LOW for the case where the latch is transparent (both Enables are LOW) and can steer a HIGH signal from either D_0 or D_1 to an output. The Select inputs can be tied together for applications requiring only that data be steered from either D_0 or D_1. A positive-going signal on either Enable input latches the outputs. A HIGH signal on the Master Reset (MR) input overrides all the other inputs and forces the Q outputs LOW.

Pin Names

$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)
$\overline{S}_0$, S_1	Select Inputs
MR	Master Reset
D_{na}–D_{nd}	Data Inputs
Q_a–Q_d	Data Outputs
$\overline{Q}_a$–$\overline{Q}_d$	Complementary Data Outputs

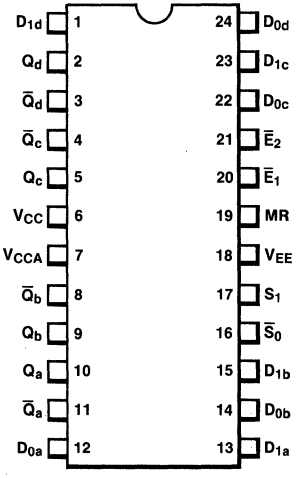
Logic Symbol



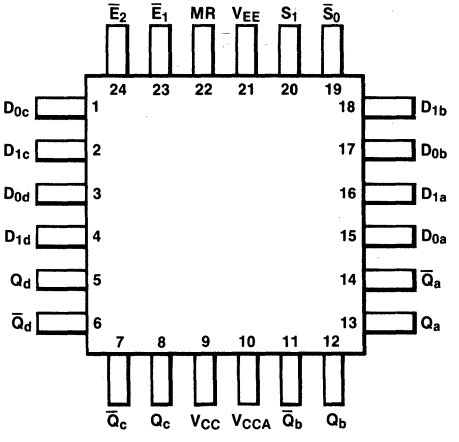
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Connection Diagrams

24-Pin DIP (Top View)



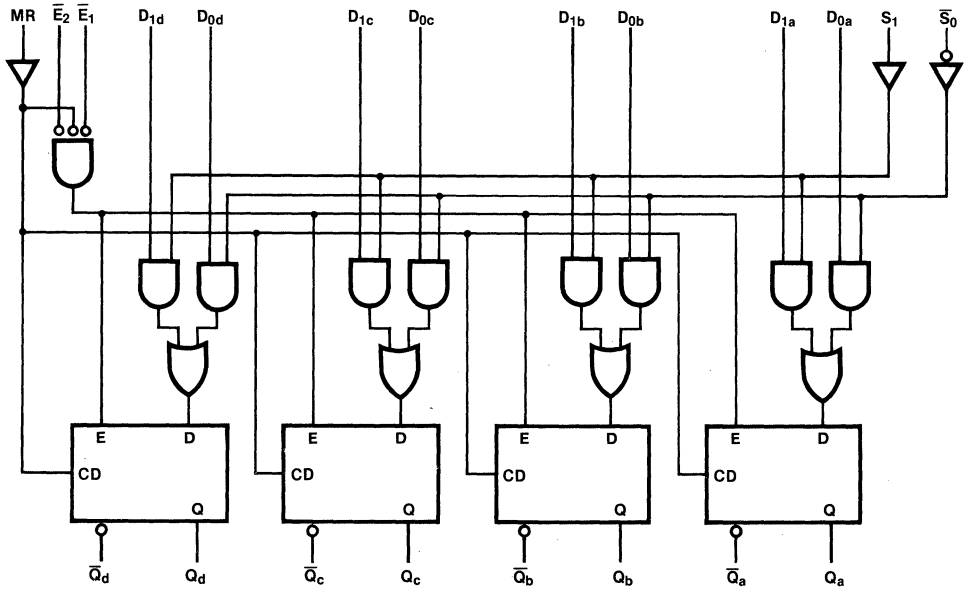
24-Pin Flatpak (Top View)



Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Logic Diagram



Operating Mode Table

Controls				Outputs
$\overline{E}_1$	$\overline{E}_2$	S_1	$\overline{S}_0$	Q_n
H	X	X	X	Latched*
X	H	X	X	Latched*
L	L	L	L	D_{0x}
L	L	H	L	$D_{0x} + D_{1x}$
L	L	L	H	L
L	L	H	H	D_{1x}

*Stores data present before $\overline{E}$ went HIGH
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Truth Table

Inputs							Outputs	
MR	$\overline{E}_1$	$\overline{E}_2$	S_1	$\overline{S}_0$	D_{1x}	D_{0x}	$\overline{Q}_x$	Q_x
H	X	X	X	X	X	X	H	L
L	L	L	H	H	H	X	L	H
L	L	L	H	H	L	X	H	L
L	L	L	L	L	X	H	L	H
L	L	L	L	L	X	L	H	L
L	L	L	L	H	X	X	H	L
L	L	L	H	L	H	X	L	H
L	L	L	H	L	X	H	L	H
L	L	L	H	L	L	L	H	L
L	H	X	X	X	X	X	Latched*	
L	X	H	X	X	X	X	Latched*	

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current $\overline{S_0}$, S_1 $\overline{E_1}$, $\overline{E_2}$ D_{na}–D_{nd} MR			 220 350 340 430	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−133	−95	−66	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

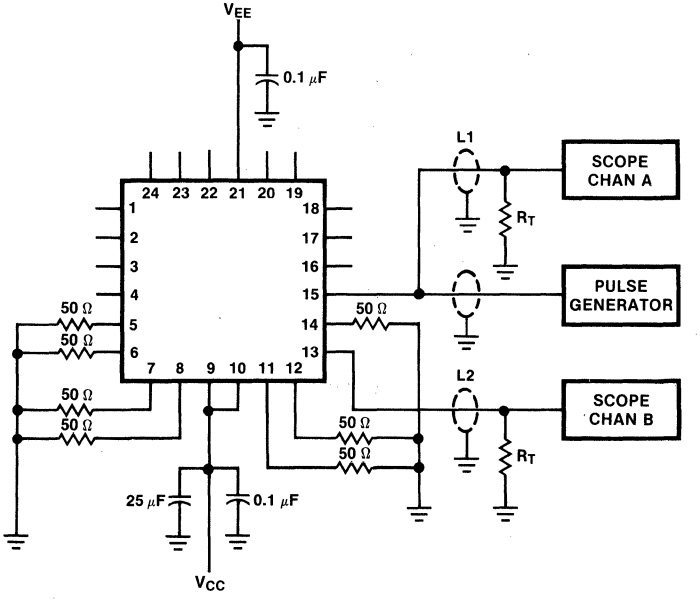
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay D_{na}–D_{nd} to Output (Transparent Mode)	0.50	1.90	0.60	1.85	0.50	1.90	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{S_0}$, S_1 to Output (Transparent Mode)	1.50	3.50	1.50	3.40	1.50	3.50	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E_1}$, $\overline{E_2}$ to Output	0.90	2.50	1.00	2.40	1.00	2.50	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.90	3.00	0.90	2.90	0.90	3.00	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.60	2.30	0.60	2.20	0.45	2.30	ns	*Figures 1* and *2*
t_s	Setup Time D_{na}–D_{nd} $\overline{S_0}$, S_1 MR (Release Time)	 0.90 2.40 1.50		 0.90 2.40 1.50		 0.90 2.70 1.50		ns	 *Figure 4* *Figure 3*
t_h	Hold Time D_{na}–D_{nd} $\overline{S_0}$, S_1	 0.40 −0.70		 0.40 −0.70		 0.40 −0.70		ns	*Figure 4*
t_{pw}(L)	Pulse Width LOW $\overline{E_1}$, $\overline{E_2}$	2.00		2.00		2.00		ns	*Figure 2*
t_{pw}(H)	Pulse Width HIGH MR	2.00		2.00		2.00		ns	*Figure 3*

*See Family characteristics for other dc specifications

Flatpak AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{na}-D_{nd} to Output (Transparent Mode)	0.50	1.70	0.60	1.65	0.50	1.70	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{S_0}$, S_1 to Output (Transparent Mode)	1.50	3.30	1.50	3.20	1.50	3.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E_1}$, $\overline{E_2}$ to Output	0.90	2.30	1.00	2.20	1.00	2.30	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.90	2.80	0.90	2.70	0.90	2.80	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.60	2.20	0.60	2.10	0.45	2.20	ns	*Figures 1* and *2*
t_s	Setup Time D_{na}-D_{nd} $\overline{S_0}$, S_1 MR (Release Time)	0.80 2.30 1.40		0.80 2.30 1.40		0.80 2.60 1.40		ns	*Figure 4* *Figure 3*
t_h	Hold Time D_{na}-D_{nd} $\overline{S_0}$, S_1	0.30 −0.80		0.30 −0.80		0.30 −0.80		ns	*Figure 4*
$t_{pw}(L)$	Pulse Width LOW $\overline{E_1}$, $\overline{E_2}$	2.00		2.00		2.00		ns	*Figure 2*
$t_{pw}(H)$	Pulse Width HIGH MR	2.00		2.00		2.00		ns	*Figure 3*

Fig. 1 AC Test Circuit



Notes

V_{CC}, V_{CCA} = +2 V, V_{EE} = −2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Fig. 2 Enable Timing

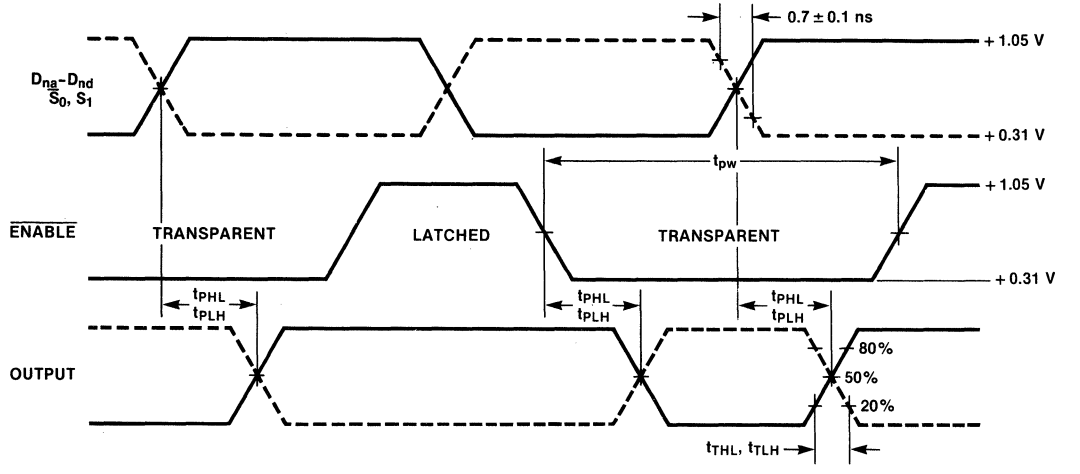


Fig. 3 Reset Timing

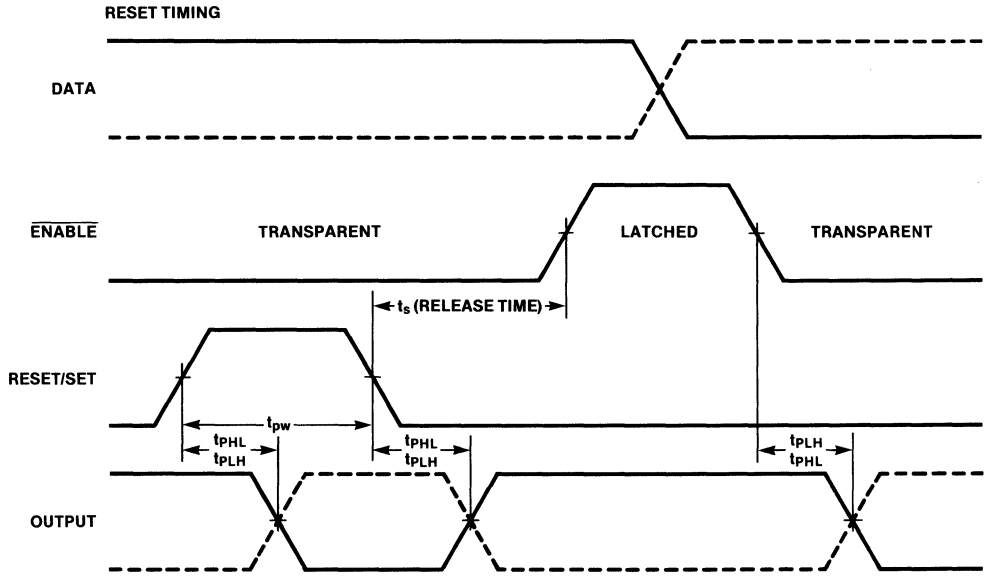
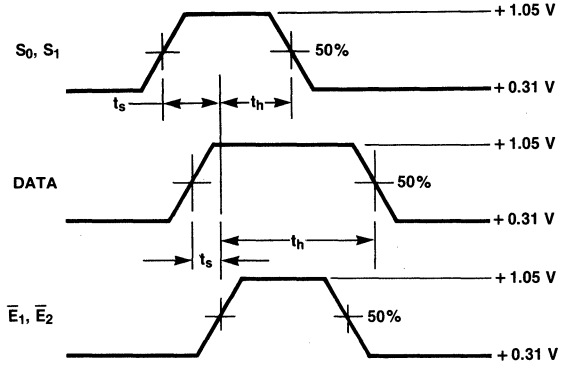


Fig. 4 Setup and Hold Times



Notes

t_s is the minimum time before the transition of the enable that information must be present at the data input

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input

F100156
Mask-Merge/Latch

F100K ECL Product

Description

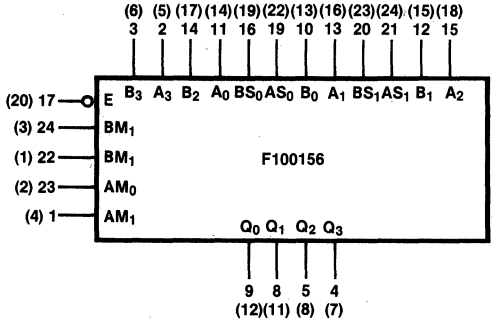
The F100156 merges two 4-bit words to form a 4-bit output word. The AM_n enable allows the merge of A into B by one, two or three places (per the AS_n value) from the left. The BM_n enable similarly allows the merge of B into A from the left (per the BS_n value). The B merge overrides the A merge when both are enabled. This means A first merges into B and B then merges into the A merge. If the B address is equal to or greater than the A address, then outputs are forced to B.

The merge outputs feed four latches, which have a common enable ($\overline{E}$) input. All inputs have a 50 kΩ (typical) pull-down resistor tied to V_{EE}. All four outputs do not have pull-down resistors; they have wired-OR capability and will require external resistors.

Pin Names

$\overline{E}$	Latch Enable Input (Active LOW)
A_0–A_3	A Data Inputs
B_0–B_3	B Data Inputs
AM_0, AM_1	A Merge Enable Inputs
BM_0, BM_1	B Merge Enable Inputs
AS_0, AS_1	A Address Inputs
BS_0, BS_1	B Address Inputs
Q_0–Q_3	Data Outputs

Logic Symbol

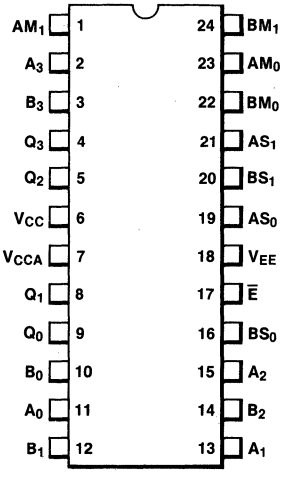


V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

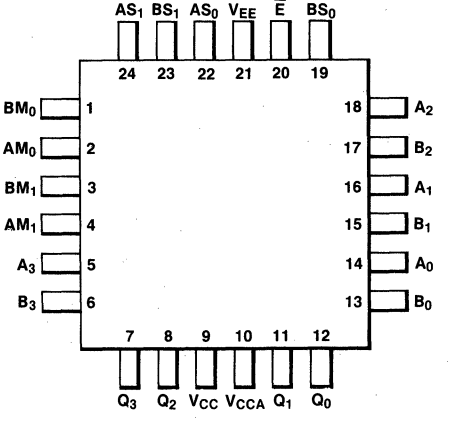
Note
When $\overline{E}$ is HIGH, Q_n outputs do not change.
When $\overline{E}$ is LOW, Q_n = A or B depending on which is selected.

Connection Diagrams

24-Pin DIP (Top View)



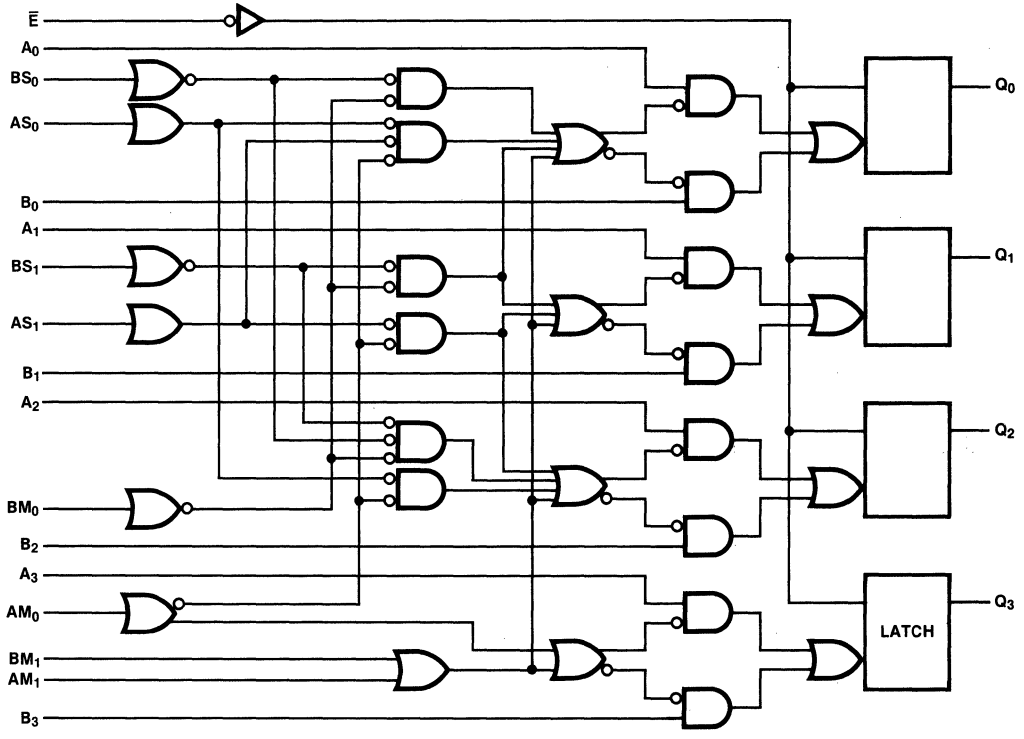
24-Pin Flatpak (Top View)



Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4Q	FC

Logic Diagram



Truth Table

Inputs									Outputs				Remarks
Merge Enables				Addresses									
BM_1	BM_0	AM_1	AM_0	BS_1	BS_0	AS_1	AS_0	$\overline{E}$	Q_0	Q_1	Q_2	Q_3	
X	X	H	X	X	X	X	X	L	B_0	B_1	B_2	B_3	Select B
H	X	X	X	X	X	X	X	L	B_0	B_1	B_2	B_3	
L	L	L	L	X	X	X	X	L	A_0	A_1	A_2	A_3	Select A
L	L	L	H	X	X	L	L	L	B_0	B_1	B_2	B_3	
L	L	L	H	X	X	L	H	L	A_0	B_1	B_2	B_3	Merge A→B
L	L	L	H	X	X	H	L	L	A_0	A_1	B_2	B_3	
L	L	L	H	X	X	H	H	L	A_0	A_1	A_2	B_3	
L	H	L	L	L	L	X	X	L	A_0	A_1	A_2	A_3	
L	H	L	L	L	H	X	X	L	B_0	A_1	A_2	A_3	Merge B→A
L	H	L	L	H	L	X	X	L	B_0	B_1	A_2	A_3	
L	H	L	L	H	H	X	X	L	B_0	B_1	B_2	A_3	
L	H	L	H	L	L	L	H	L	A_0	B_1	B_2	B_3	
L	H	L	H	L	L	H	L	L	A_0	A_1	B_2	B_3	Merge A→B
L	H	L	H	L	L	H	H	L	A_0	A_1	A_2	B_3	
L	H	L	H	L	H	H	L	L	B_0	A_1	B_2	B_3	Merge A→B
L	H	L	H	L	H	H	H	L	B_0	A_1	A_2	B_3	then
L	H	L	H	H	L	H	H	L	B_0	B_1	A_2	B_3	Merge B→A
L	H	L	H	H	H	H	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	H	H	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	H	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	H	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	H	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	L	H	L	B_0	B_1	B_2	B_3	B Address ≥ A Address
L	H	L	H	H	L	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	H	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	H	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	L	L	L	L	B_0	B_1	B_2	B_3	
X	X	X	X	X	X	X	X	H	Q_0	Q_1	Q_2	Q_3	Latch
Before Start	At Start	After End	At End										

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current A_n, B_n BM_n, AM_n, BS_n, AS_n, $\overline{E}$			265	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−235	−161	−107	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

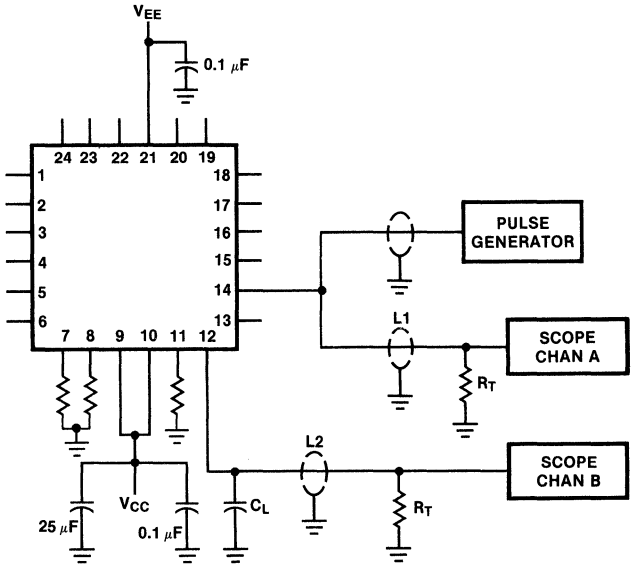
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to Outputs (Transparent Mode)	0.45	1.90	0.50	1.80	0.50	2.00	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Outputs	1.00	2.50	1.00	2.40	1.00	2.50	ns	
t_{PLH} t_{PHL}	Propagation Delay AM_n, BM_n, AS_n, BS_n to Outputs (Transparent Mode)	1.20	3.70	1.20	3.70	1.20	3.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.90	0.45	1.80	0.45	1.90	ns	
t_s	Setup Time A_n, B_n AM_n, BM_n, AS_n, BS_n	0.80 2.90		0.80 2.90		0.80 2.90		ns	*Figure 3*
t_h	Hold Time A_n, B_n AM_n, BM_n, AS_n, BS_n	2.10 0.80		2.10 0.80		2.10 0.80		ns	
$t_{pw}(L)$	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 2*

*See Family Characteristics for other dc specifications

Flatpak AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to Outputs (Transparent Mode)	0.45	1.70	0.50	1.60	0.50	1.80	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Outputs	1.00	2.30	1.00	2.20	1.00	2.30	ns	
t_{PLH} t_{PHL}	Propagation Delay AM_n, BM_n, AS_n, BS_n to Outputs (Transparent Mode)	1.20	3.50	1.20	3.50	1.20	3.60	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.70	0.45	1.80	ns	
t_s	Setup Time A_n, B_n AM_n, BM_n, AS_n, BS_n	0.70 2.80		0.70 2.80		0.70 2.80		ns	*Figure 3*
t_h	Hold Time A_n, B_n AM_n, BM_n, AS_n, BS_n	2.00 0.70		2.00 0.70		2.00 0.70		ns	
$t_{pw}(L)$	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 2*

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Fig. 2 Enable Timing

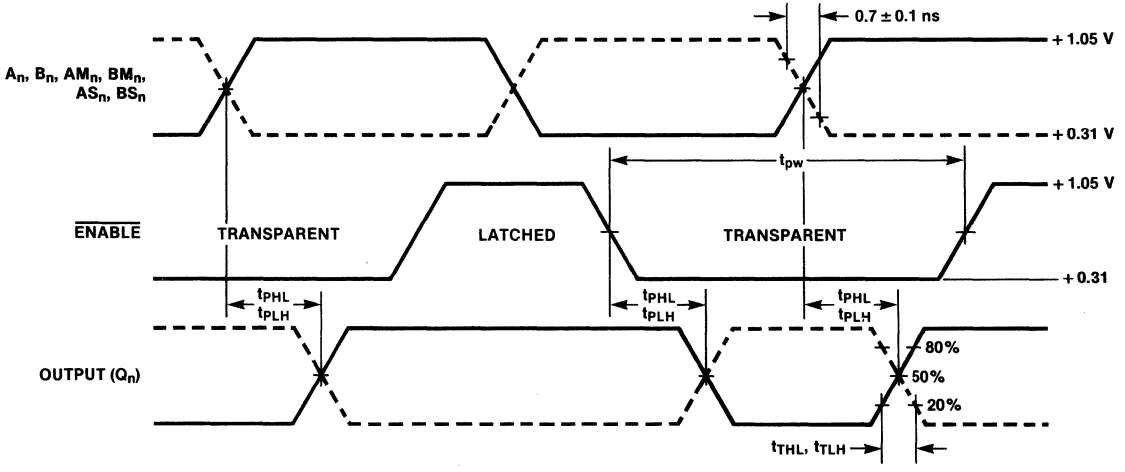
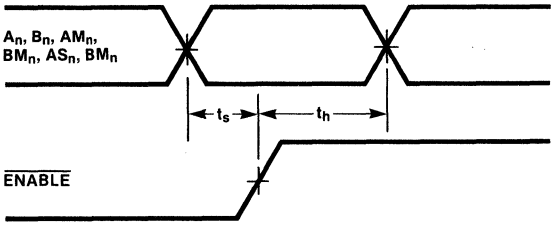


Fig. 3 Data Setup and Hold Times



Notes

t_s is the minimum time before the transition of the enable that information must be present at the designated input

t_h is the minimum time after the transition of the enable that information must remain unchanged at the designated input

F100158
8-Bit Shift Matrix

F100K ECL Product

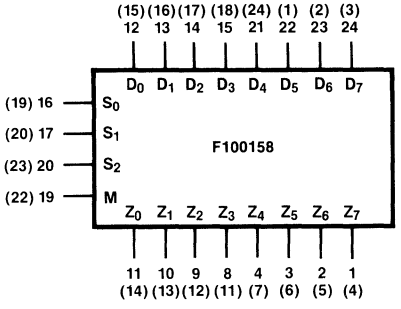
Description

The F100158 contains a combinatorial network which performs the function of an 8-bit shift matrix. Three control lines (S_n) are internally decoded and define the number of places which an 8-bit word present at the inputs (D_n) is shifted to the left and presented at the outputs (Z_n). A Mode Control input (M) is provided which, if LOW, forces LOW all outputs to the right of the one that contains D_7. This operation is sometimes referred to as *LOW backfill.* If M is HIGH, an end-around shift is performed such that D_0 appears at the output to the right of the one that contains D_7. This operation is commonly referred to as *barrel shifting.*

Pin Names

D_0-D_7	Data Inputs
S_0-S_2	Select Inputs
M	Mode Control Input
Z_0-Z_7	Data Outputs

Logic Symbol



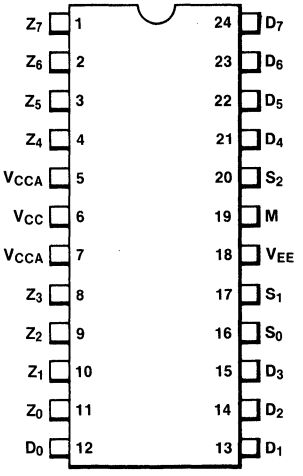
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 5 (8), 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

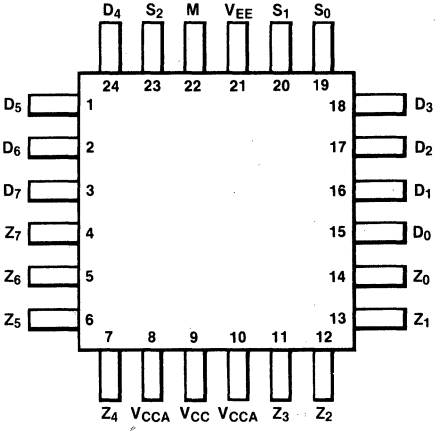
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4Q	FC

Connection Diagrams

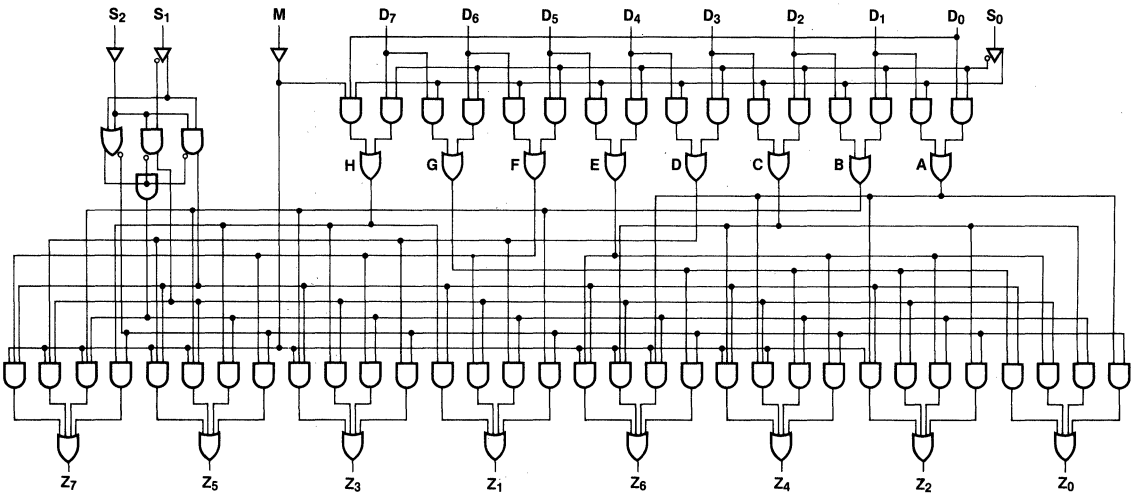
24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Logic Diagram



Truth Table

Inputs				Outputs							
M	**S_0**	**S_1**	**S_2**	**Z_0**	**Z_1**	**Z_2**	**Z_3**	**Z_4**	**Z_5**	**Z_6**	**Z_7**
X	L	L	L	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
L	H	L	L	D_1	D_2	D_3	D_4	D_5	D_6	D_7	L
L	L	H	L	D_2	D_3	D_4	D_5	D_6	D_7	L	L
L	H	H	L	D_3	D_4	D_5	D_6	D_7	L	L	L
L	L	L	H	D_4	D_5	D_6	D_7	L	L	L	L
L	H	L	H	D_5	D_6	D_7	L	L	L	L	L
L	L	H	H	D_6	D_7	L	L	L	L	L	L
L	H	H	H	D_7	L	L	L	L	L	L	L
H	H	L	L	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0
H	L	H	L	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_1
H	H	H	L	D_3	D_4	D_5	D_6	D_7	D_0	D_1	D_2
H	L	L	H	D_4	D_5	D_6	D_7	D_0	D_1	D_2	D_3
H	H	L	H	D_5	D_6	D_7	D_0	D_1	D_2	D_3	D_4
H	L	H	H	D_6	D_7	D_0	D_1	D_2	D_3	D_4	D_5
H	H	H	H	D_7	D_0	D_1	D_2	D_3	D_4	D_5	D_6

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current All Inputs			220	μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	−205	−140	−95	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

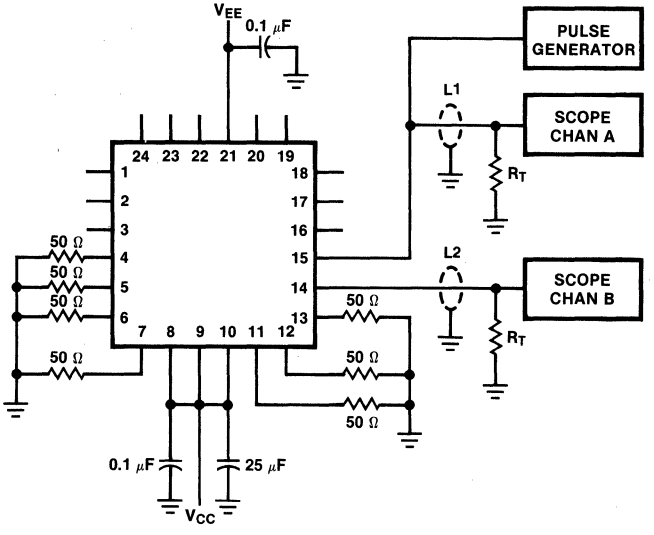
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	1.10	2.80	1.10	2.70	1.10	2.80	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay M to Output	1.15	4.20	1.25	4.20	1.15	4.20	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to Output	1.70	4.20	1.70	4.20	1.70	4.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	2.30	0.50	2.30	0.50	2.30	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	1.10	2.60	1.10	2.50	1.10	2.60	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay M to Output	1.15	4.00	1.25	4.00	1.15	4.00	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to Output	1.70	4.00	1.70	4.00	1.70	4.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	2.20	0.50	2.20	0.50	2.20	ns	

*See Family Characteristics for other dc specifications.

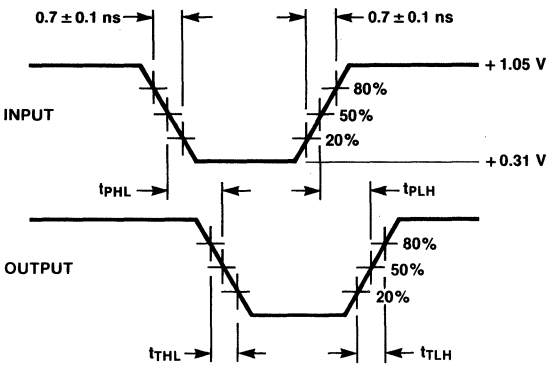
Fig. 1 AC Test Circuit



Notes

V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP refer to logic symbol

Fig. 2 Propagation Delay and Transition Times



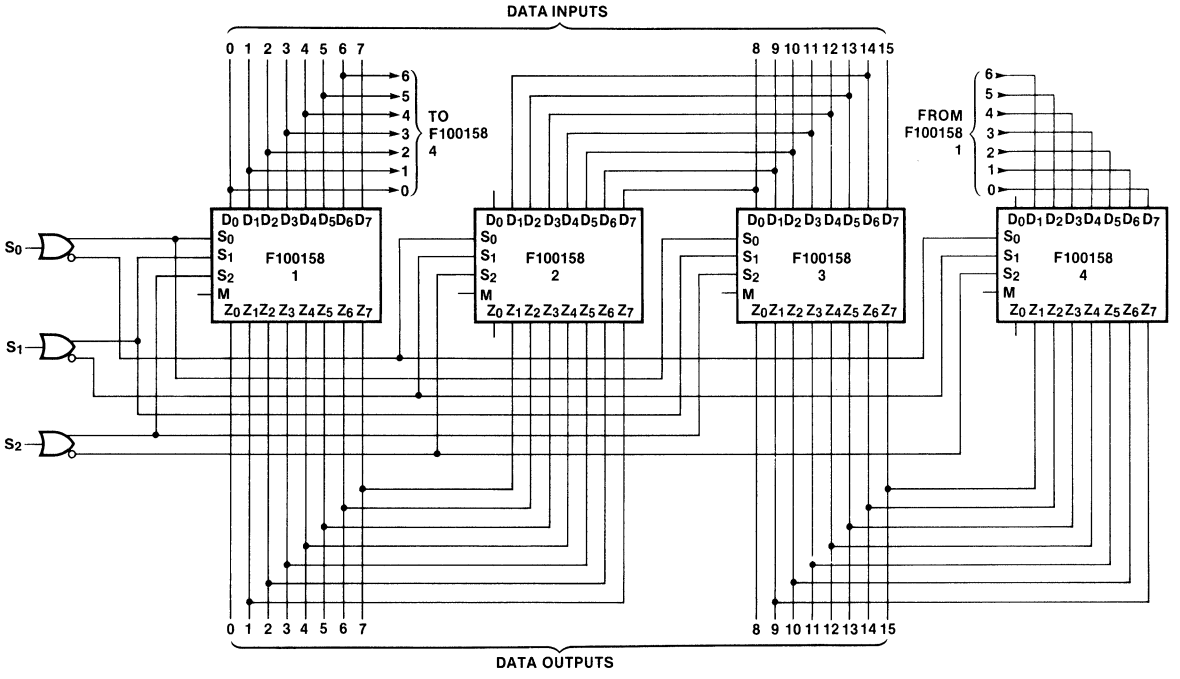
Applications

The following technique uses two ranks of F100158s to shift a 64-bit word from 0 to 63 places. Although two stage delays are required (one for each rank), the total shift takes only about 4 ns. This technique performs a bit shift on each 8-bit byte in the first rank and then a modulo-8 byte shift on the 64 bit word in the second rank.

Basic 16-Bit 0-7 Place Shifter

Figure 3 shows the basic 0-7 place shift technique which can be expanded to accommodate any word length. Each 8-bit byte requires a pair of F100158s operating in the LOW backfill mode. The address lines for each pair of ICs are driven out of phase by three OR gates. Inputs for the two ICs are taken from two bytes transposed in order; outputs are transposed and emitter-OR tied. One device shifts right from location 0 and the other shifts left from location 7. The bits shifted off one pair are picked up by the next pair of F100158s or — in the case of the last one in the rank — returned to the first device. The net result is a 0-7 place shift of the entire word.

Fig. 3 Basic 16-Bit 0-7 Place Shifter



Expanding to 64-Bit Word and 64-Place Shift

The basic 0-7 place shift technique can be expanded to accommodate a 64-bit word shifted from 0 to 63 places, however, two ranks of F100158s are required *(Figure 4)*. The first rank is identical to the one illustrated in *Figure 3* except it contains a total of 16 devices. The second rank consists of eight additional F100158s connected in the modulo-8 configuration shown in *Figure 5*.

The modulo-8 rank is used to simulate an 8-bit simultaneous shift since the F100158 cannot shift in 8-bit jumps. The modulo-8 configuration is achieved by wiring the first rank and the output device to the second rank as illustrated in *Figure 5*. The LSB of each output byte in the first rank is wired to one of the eight inputs of the first F100158 in the second rank. The next least significant bit of each first-rank F100158 pair, however, is connected to the inputs of the second F100158 in the second rank. The other first-ranked outputs are connected in a similar fashion to the remainder of the second-rank inputs. Ultimately, the outputs of the second rank must then be connected to reform the final usable 64-bit word so that the bits are again ordered from 0-63.

The effect is that each single-location shift in the second rank appears to be an eight place shift in the final word due to the way the inputs and outputs of the second rank are connected. The combination of the two ranks produces the 64-place shift of the entire word.

Fig. 4 64-Bit 0 — Place Barrel Shifter

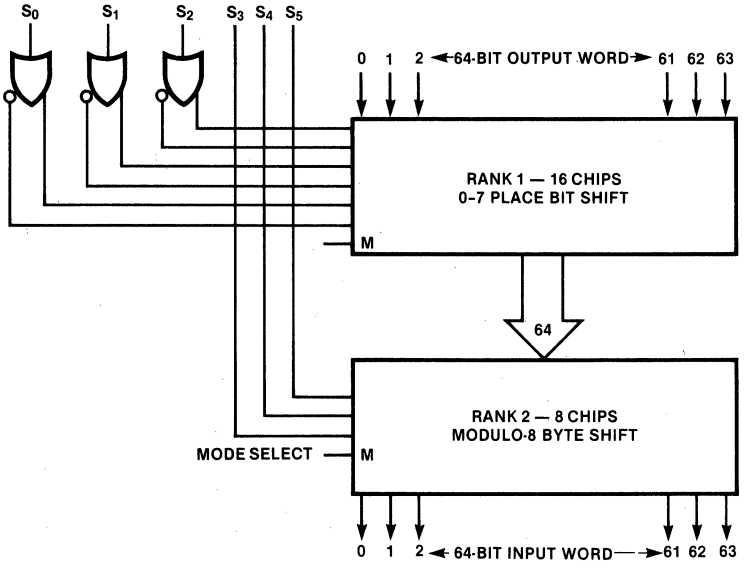
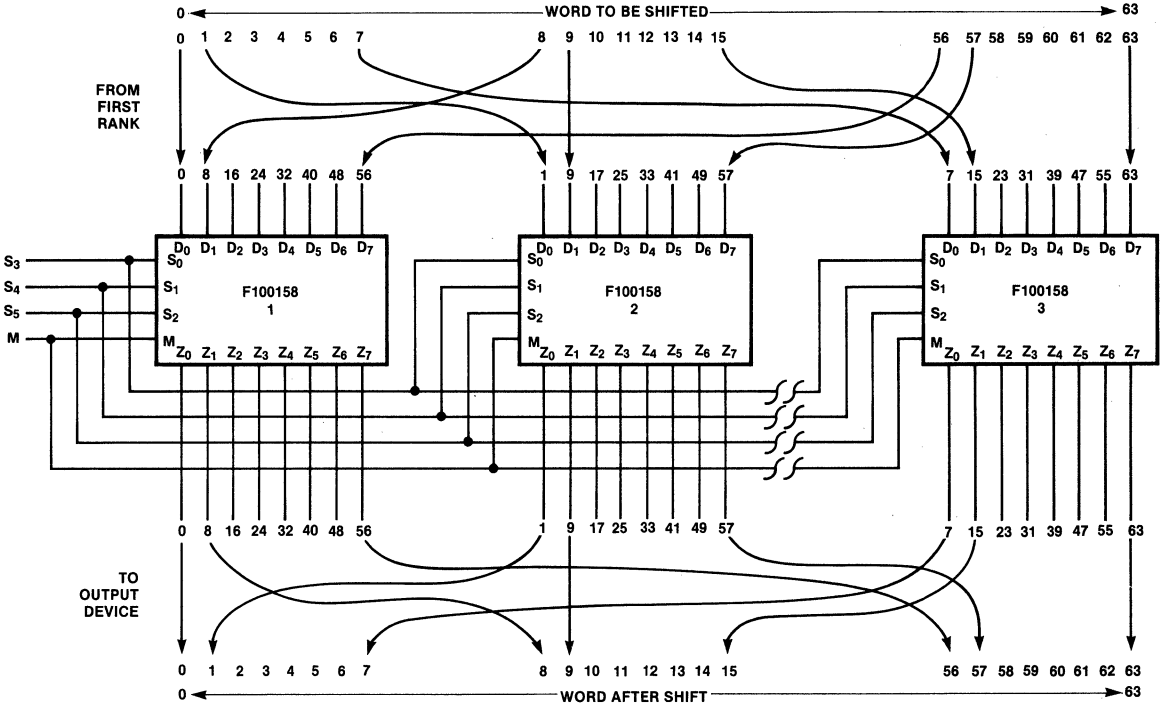


Fig. 5 Modulo-8 Shift



F100160
Dual Parity Checker/Generator

F100K ECL Product

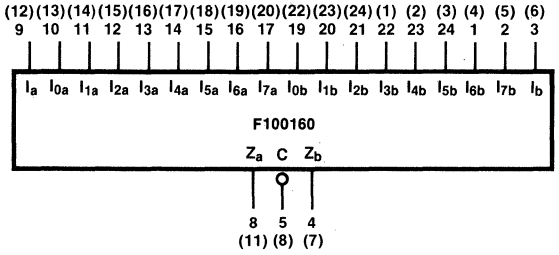
Description

The F100160 is a dual parity checker/generator. Each half has nine inputs; the output is HIGH when an even number of inputs are HIGH. One of the nine inputs (I_a or I_b) has the shorter through-put delay and is therefore preferred as the expansion input for generating parity for 16 or more bits. The F100160 also has a Compare ($\overline{C}$) output which allows the circuit to compare two 8-bit words. The $\overline{C}$ output is LOW when the two words match, bit for bit.

Pin Names

I_a, I_b, I_{na}, I_{nb}	Data Inputs
Z_a, Z_b	Parity Odd Outputs
$\overline{C}$	Compare Output

Logic Symbol



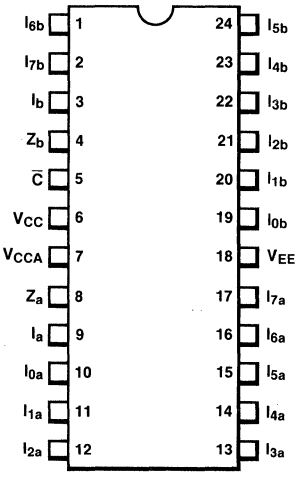
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

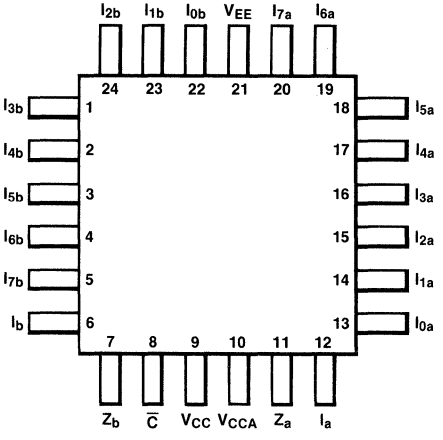
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Connection Diagrams

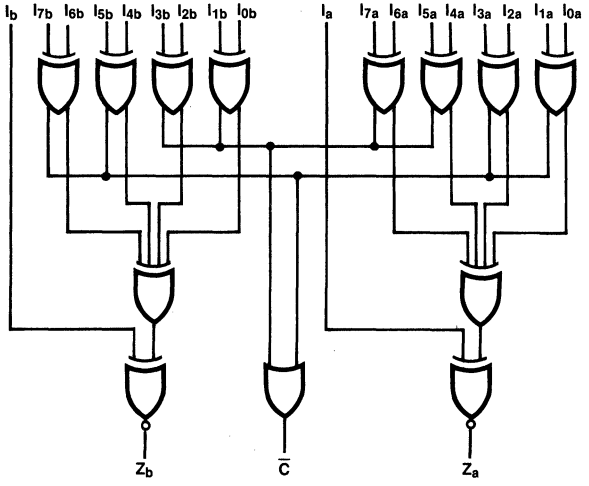
24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Logic Diagram



Truth Table (Each Half)

Sum of HIGH Inputs	Output Z
Even	HIGH
Odd	LOW

Comparator Function

$$\overline{C} = (I_{0a} \oplus I_{1a}) + (I_{2a} \oplus I_{3a}) + (I_{4a} \oplus I_{5a}) + (I_{6a} \oplus I_{7a}) + (I_{0b} \oplus I_{1b}) + (I_{2b} \oplus I_{3b}) + (I_{4b} \oplus I_{5b}) + (I_{6b} \oplus I_{7b})$$

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current I_a, I_b I_{na}, I_{nb}			340 240	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−115	−82	−57	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

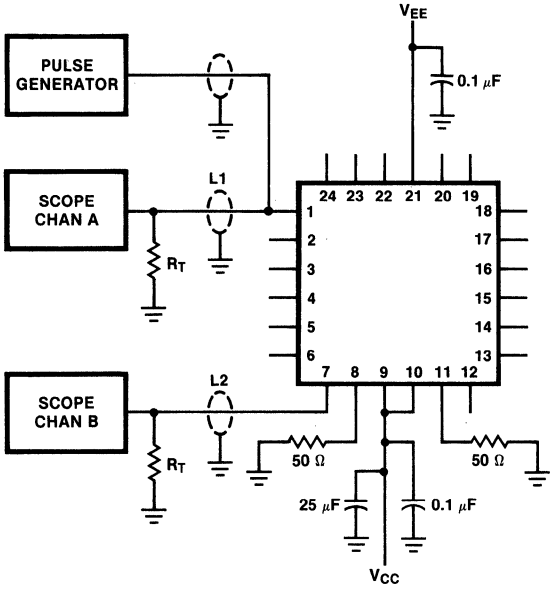
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to Z_a, Z_b	1.30	4.30	1.30	4.10	1.30	4.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to $\overline{C}$	1.20	3.30	1.20	3.10	1.20	3.30	ns	
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to Z_a, Z_b	0.50	1.60	0.50	1.50	0.50	1.60	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.50	0.45	1.60	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to Z_a, Z_b	1.30	4.10	1.30	3.90	1.30	4.10	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to $\overline{C}$	1.20	3.10	1.20	2.90	1.20	3.10	ns	
t_{PLH} t_{PHL}	Propagation Delay I_a, I_b to Z_a, Z_b	0.50	1.40	0.50	1.30	0.50	1.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.50	ns	

*See Family Characteristics for other dc specifications.

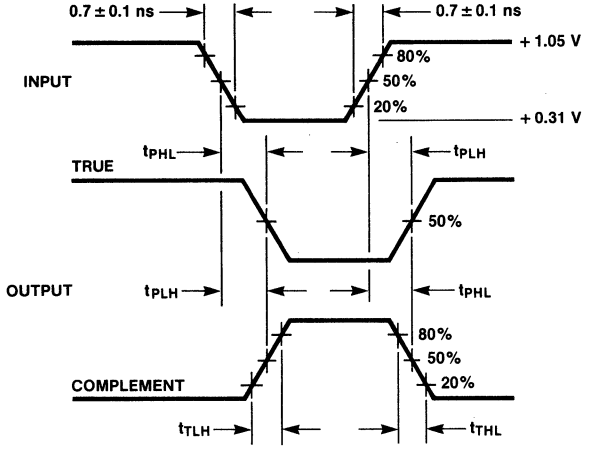
Fig. 1 AC Test Circuit



Notes

V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Fig. 2 Propagation Delay and Transition Times



F100163
Dual 8-Input Multiplexer

F100K ECL Product

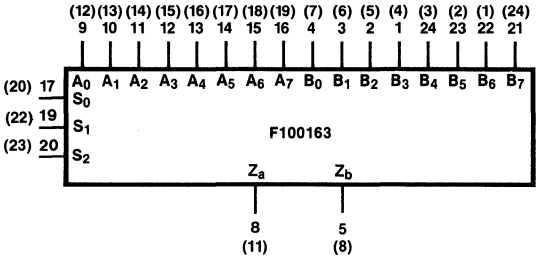
Description

The F100163 is a dual 8-input multiplexer. The Data Select (S_n) inputs determine which bit (A_n and B_n) will be presented at the outputs (Z_a and Z_b respectively). The same bit (0-7) will be selected for both the Z_a and Z_b output.

Pin Names

$S_0 - S_2$	Data Select Inputs
$A_0 - A_7$	A Data Inputs
$B_0 - B_7$	B Data Inputs
Z_a, Z_b	Data Outputs

Logic Symbol



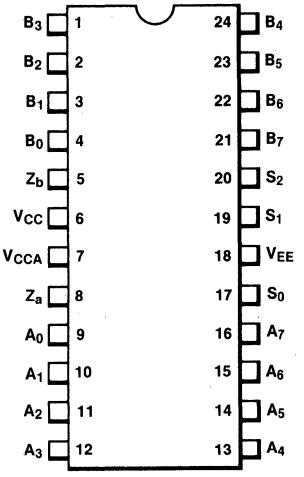
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

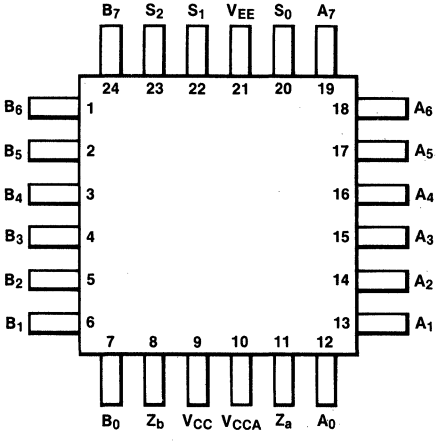
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Connection Diagrams

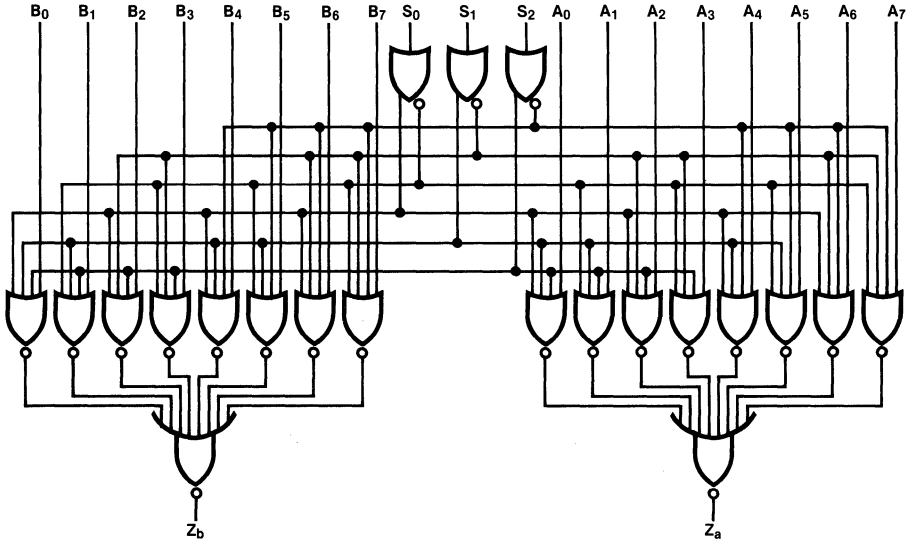
24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Logic Diagram



Truth Table

Inputs											Outputs
Select			Data								
S_2	S_1	S_0	A_7 B_7	A_6 B_6	A_5 B_5	A_4 B_4	A_3 B_3	A_2 B_2	A_1 B_1	A_0 B_0	Z_a Z_b
L L	L L	L L								L H	L H
L L	L L	H H							L H		L H
L L	H H	L L						L H			L H
L L	H H	H H					L H				L H
H H	L L	L L				L H					L H
H H	L L	H H			L H						L H
H H	H H	L L		L H							L H
H H	H H	H H	L H								L H

H = HIGH Voltage Level
L = LOW Voltage Level
Blank = X = Don't Care

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current S_n A_n, B_n			 265 340	 μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−153	−110	−76	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

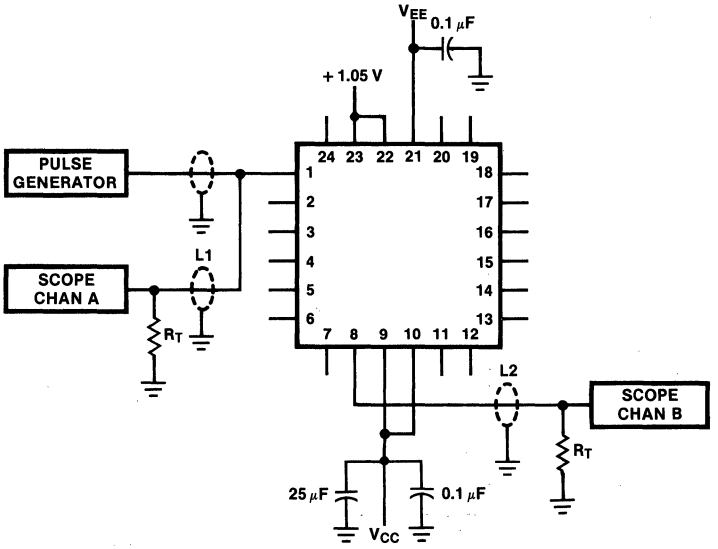
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Condition**
t_{PLH} t_{PHL}	Propagation Delay A_0–A_7, B_0–B_7 to Output	0.55	1.65	0.60	1.70	0.65	1.80	ns	
t_{PLH} t_{PHL}	Propagation Delay S_0–S_2 to Output	1.10	2.80	1.10	2.80	1.20	3.10	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	1.85	0.55	1.80	0.50	1.80	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Condition**
t_{PLH} t_{PHL}	Propagation Delay A_0–A_7, B_0–B_7 to Output	0.55	1.45	0.60	1.50	0.65	1.60	ns	
t_{PLH} t_{PHL}	Propagation Delay S_0–S_2 to Output	1.10	2.60	1.10	2.60	1.20	2.90	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	1.75	0.55	1.70	0.50	1.70	ns	

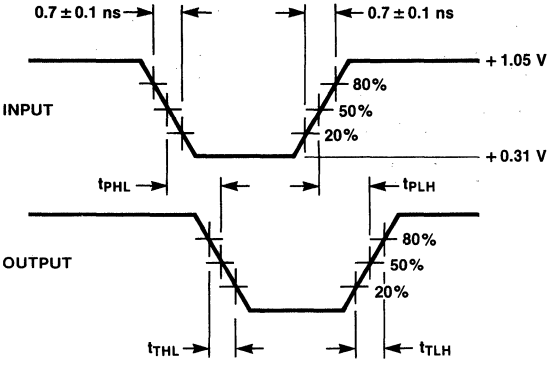
*See Family Characteristics for other dc specifications.

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = −2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Fig. 2 Propagation Delay and Transition Times



F100164
16-Input Multiplexer

F100K ECL Product

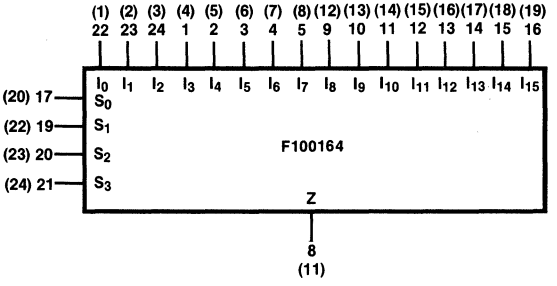
Description

The F100164 is a 16-input multiplexer. Data paths are controlled by four Select lines (S_0-S_3). Their decoding is shown in the truth table. Output data polarity is the same as the selected input data.

Pin Names

I_0-I_{15}	Data Inputs
S_0-S_3	Select Inputs
Z	Data Output

Logic Symbol



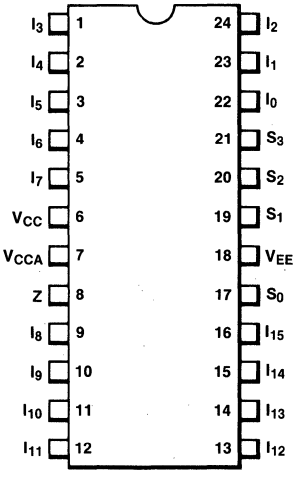
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

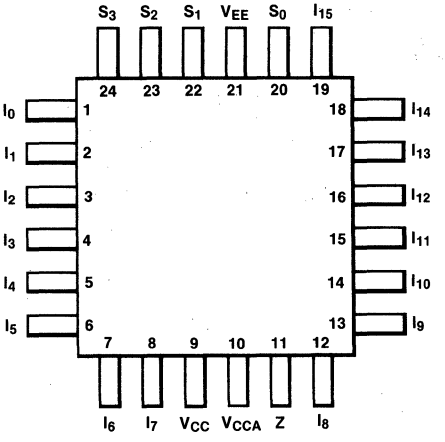
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Connection Diagrams

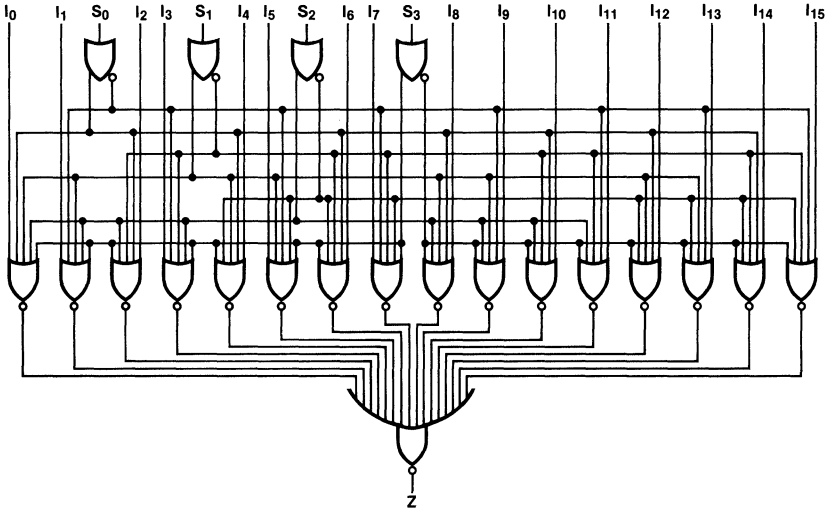
24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Logic Diagram



Truth Table

Select Inputs				Output
S_0	S_1	S_2	S_3	Z
L	L	L	L	I_0
H	L	L	L	I_1
L	H	L	L	I_2
H	H	L	L	I_3
L	L	H	L	I_4
H	L	H	L	I_5
L	H	H	L	I_6
H	H	H	L	I_7
L	L	L	H	I_8
H	L	L	H	I_9
L	H	L	H	I_{10}
H	H	L	H	I_{11}
L	L	H	H	I_{12}
H	L	H	H	I_{13}
L	H	H	H	I_{14}
H	H	H	H	I_{15}

H = HIGH Voltage Level
L = LOW Voltage Level

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current I_n S_0, S_1 S_2, S_3			 280 240 200	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−105	−70	−49	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

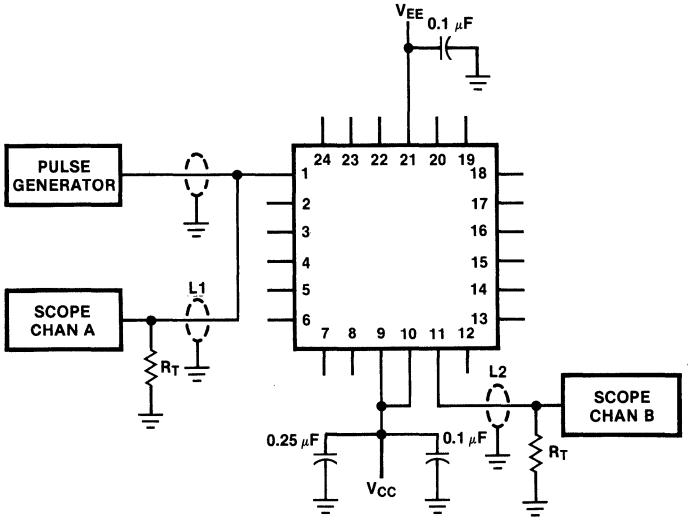
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay I_0–I_{15} to Output	0.80	2.20	0.90	2.35	0.90	2.55	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	1.45	3.10	1.45	3.20	1.55	3.60	ns	
t_{PLH} t_{PHL}	Propagation Delay S_2, S_3 to Output	1.10	2.45	1.10	2.50	1.20	2.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.70	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay I_0–I_{15} to Output	0.80	2.00	0.90	2.15	0.90	2.35	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	1.45	2.90	1.45	3.00	1.55	3.40	ns	
t_{PLH} t_{PHL}	Propagation Delay S_2, S_3 to Output	1.10	2.25	1.10	2.30	1.20	2.60	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.60	0.45	1.60	ns	

*See Family Characteristics for other dc specifications.

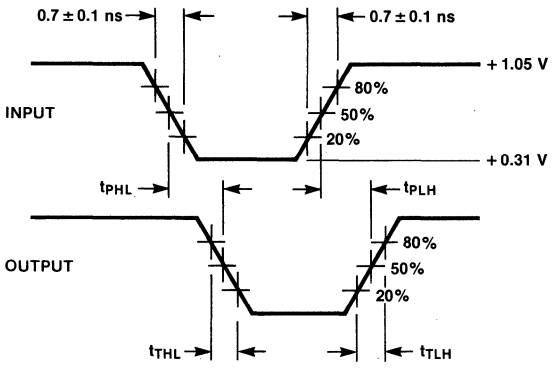
Fig. 1 AC Test Circuit



Notes

V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Fig. 2 Propagation Delay and Transition Times



F100165
Universal Priority Encoder

F100K ECL Product

Description

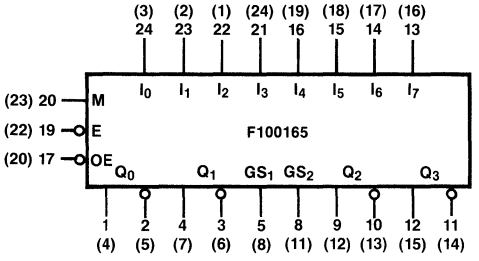
The F100165 contains eight input latches with a common Enable ($\overline{E}$) followed by encoding logic which generates the binary address of the highest priority input having a HIGH signal. The circuit operates as a dual 4-input encoder when the Mode Control (M) input is LOW, and as a signal 8-input encoder when M is HIGH. In the 8-input mode, Q_0, Q_1 and Q_2 are the relevant outputs, I_0 is the highest priority input and GS_1 is the relevant Group Signal output. In the dual mode, Q_0, Q_1 and GS_1 operate with I_0–I_3. Q_2, Q_3 and GS_2 operate with I_4–I_7. A GS output goes LOW when its pertinent inputs are all LOW.

Inputs are latched when $\overline{E}$ goes HIGH. A HIGH signal on the Output Enable ($\overline{OE}$) input forces all Q outputs LOW and GS outputs HIGH. Expansion to accommodate more inputs can be done by connecting the GS output of a higher priority group to the $\overline{OE}$ input of the next lower priority group.

Pin Names

I_0 – I_7	Data Inputs
$\overline{E}$	Enable Input (Active LOW)
$\overline{OE}$	Output Enable Input (Active LOW)
M	Mode Control Input
GS_1 – GS_2	Group Signal Outputs
Q_0 – Q_3	Data Outputs
$\overline{Q_0}$ – $\overline{Q_3}$	Complementary Data Outputs

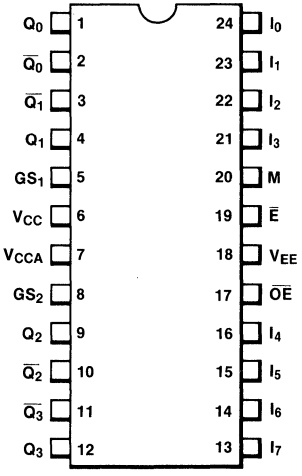
Logic Symbol



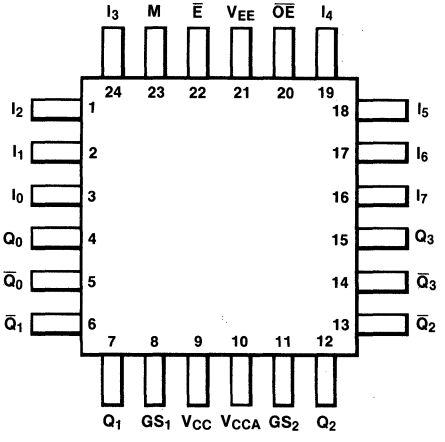
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Connection Diagrams

24-Pin DIP (Top View)



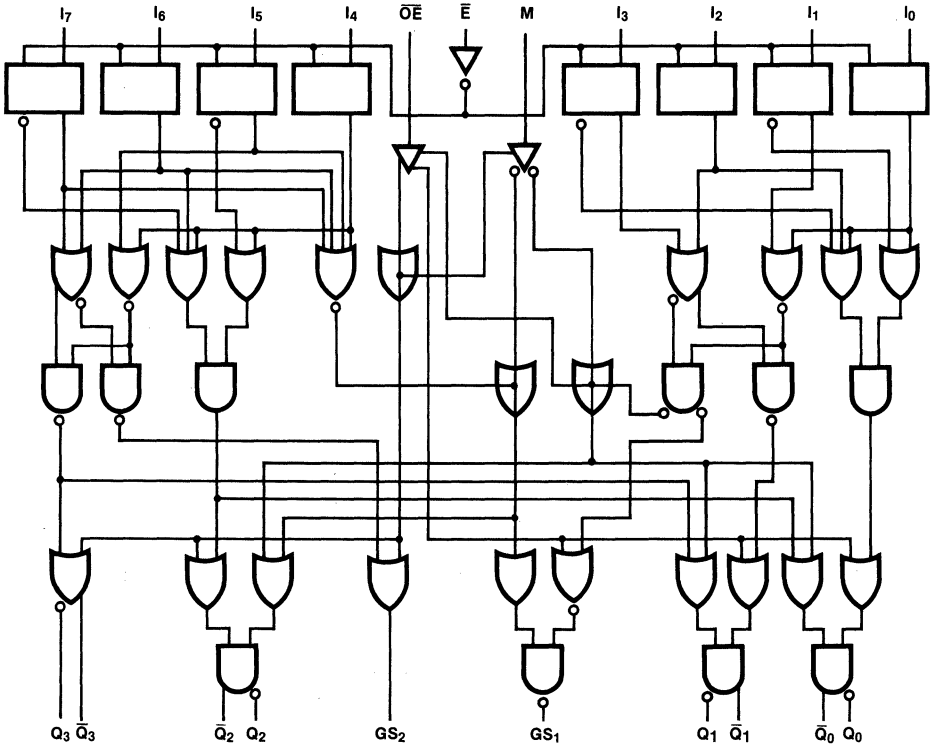
24-Pin Flatpak (Top View)



Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Logic Diagram



Truth Table

Inputs											Outputs					
$\overline{E}$	$\overline{OE}$	M	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Q_0	Q_1	Q_2	Q_3	GS_1	GS_2
L	L	L	H	X	X	X					L	L			H	
L	L	L	L	H	X	X					H	L			H	
L	L	L	L	L	H	X					L	H			H	
L	L	L	L	L	L	H					H	H			H	
L	L	L	L	L	L	L					L	L			L	
L	L	L					H	X	X	X			L	L		H
L	L	L					L	H	X	X			H	L		H
L	L	L					L	L	H	X			L	H		H
L	L	L					L	L	L	H			H	H		H
L	L	L					L	L	L	L			L	L		L
L	L	H	H	X	X	X	X	X	X	X	L	L	L	L	H	H
L	L	H	L	H	X	X	X	X	X	X	H	L	L	L	H	H
L	L	H	L	L	H	X	X	X	X	X	L	H	L	L	H	H
L	L	H	L	L	L	H	X	X	X	X	H	H	L	L	H	H
L	L	H	L	L	L	L	H	X	X	X	L	L	H	L	H	H
L	L	H	L	L	L	L	L	H	X	X	H	L	H	L	H	H
L	L	H	L	L	L	L	L	L	H	X	L	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	H	H	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H
X	H	X	X	X	X	X	X	X	X	X	L	L	L	L	H	H
H	L	L	X	X	X	X	X	X	X	X	Given by I_0-I_7 when $\overline{E}$ was LOW and M = L					
H	L	H	X	X	X	X	X	X	X	X	Given by I_0-I_7 when $\overline{E}$ was LOW and M = H					

H = HIGH Voltage Level
L = LOW Voltage Level
Blank = X = Don't Care

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current All Inputs			230	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−200	−140	−77	mA	Inputs Open

*See Family Characteristics for other dc specifications.

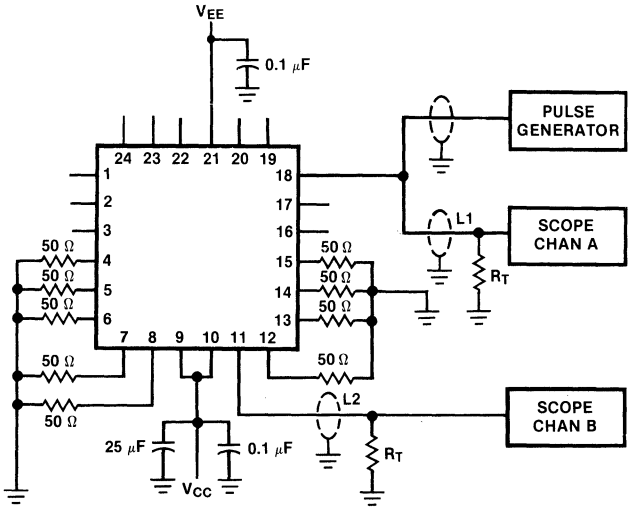
Ceramic Dual In-line Package AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Condition**
t_{PLH} t_{PHL}	Propagation Delay I_0-I_7 to Q_0-Q_3, $\overline{Q}_0$-$\overline{Q}_3$ (Transparent Mode)	1.10	4.10	1.10	4.10	1.10	4.60	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay I_0-I_7 to GS_1-GS_2 (Transparent Mode)	1.30	3.90	1.30	3.90	1.30	4.20	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}$ to Q_0-Q_3, $\overline{Q}_0$-$\overline{Q}_3$	1.00	3.00	1.00	3.00	1.10	3.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}$ to GS_1-GS_2	1.10	2.60	1.10	2.60	1.20	2.80	ns	
t_{PLH} t_{PHL}	Propagation Delay M to Q_0-Q_3, $\overline{Q}_0$-$\overline{Q}_3$	0.90	3.60	1.00	3.60	1.00	3.80	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_0-Q_3, $\overline{Q}_0$-$\overline{Q}_3$	1.50	4.70	1.50	4.60	1.50	5.00	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.50	ns	*Figures 1, 2* and *3*
t_s	Setup Time I_0-I_7	1.00		0.90		1.00		ns	*Figure 4*
t_h	Hold Time I_0-I_7	1.20		1.20		1.20		ns	

Flatpak AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_0-I_7 to Q_0-Q_3, $\overline{Q}_0$-$\overline{Q}_3$ (Transparent Mode)	1.10	3.90	1.10	3.90	1.10	4.40	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay I_0-I_7 to GS_1-GS_2 (Transparent Mode)	1.30	3.70	1.30	3.70	1.30	4.00	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}$ to Q_0-Q_3, $\overline{Q}_0$-$\overline{Q}_3$	1.00	2.80	1.00	2.80	1.10	3.10	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}$ to GS_1-GS_2	1.10	2.40	1.10	2.40	1.20	2.60	ns	
t_{PLH} t_{PHL}	Propagation Delay M to Q_0-Q_3, $\overline{Q}_0$-$\overline{Q}_3$	0.90	3.40	1.00	3.40	1.00	3.60	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_0-Q_3, $\overline{Q}_0$-$\overline{Q}_3$	1.50	4.50	1.50	4.40	1.50	4.80	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.40	0.45	1.30	0.45	1.40	ns	*Figures 1, 2* and *3*
t_s	Setup Time I_0-I_7	0.90		0.80		0.90		ns	*Figure 4*
t_h	Hold Time I_0-I_7	1.10		1.10		1.10		ns	

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Fig. 2 Propagation Delay (M, $\overline{OE}$) and Transition Times

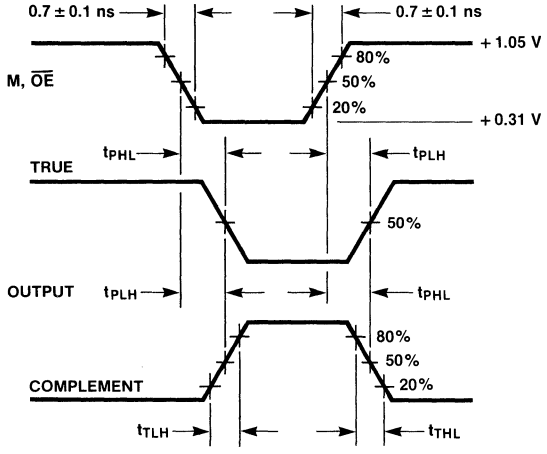


Fig. 3 Enable Timing

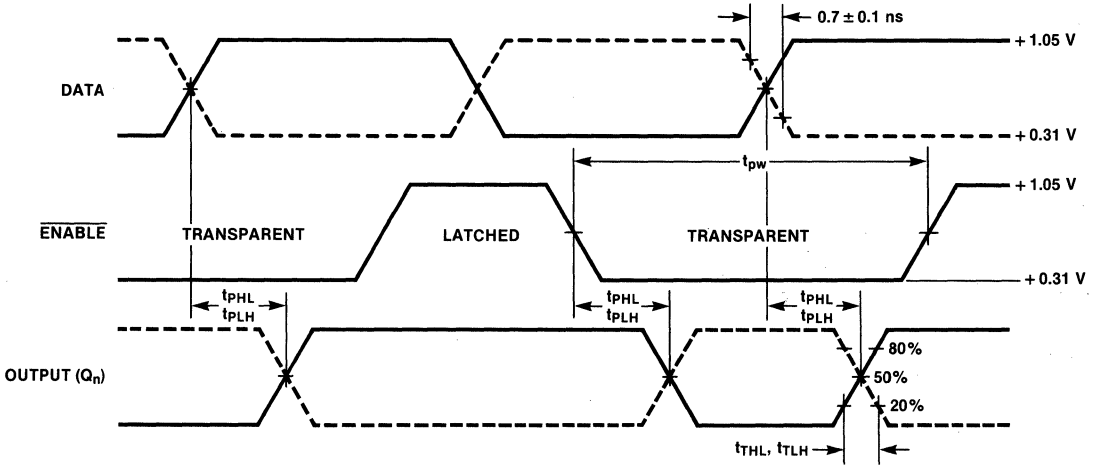
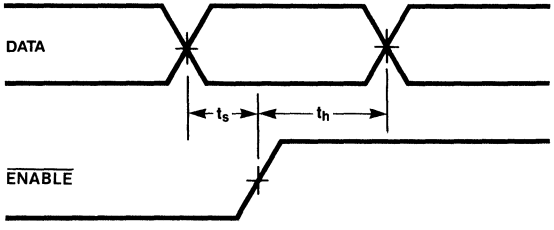


Fig. 4 Setup and Hold Times



Notes

t_s is the minimum time before the transition of the enable that information must be present at the data input

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input

F100166
9-Bit Comparator

F100K ECL Product

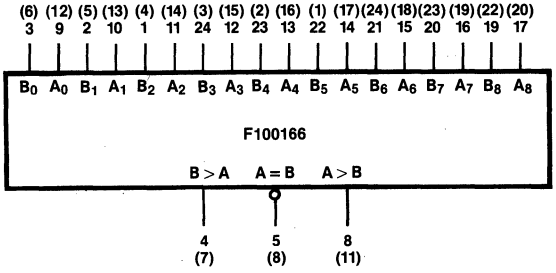
Description

The F100166 is a 9-bit magnitude comparator which compares the arithmetic value of two 9-bit words and indicates whether one word is greater than, or equal to, the other. Other functions can be generated by the wire-OR of the outputs.

Pin Names

$A_0 - A_8$	A Data Inputs
$B_0 - B_8$	B Data Inputs
A > B	A Greater than B Output
$\overline{B > A}$	B Greater than A Output
$\overline{A = B}$	Complement A Equal to B Output (Active LOW)

Logic Symbol



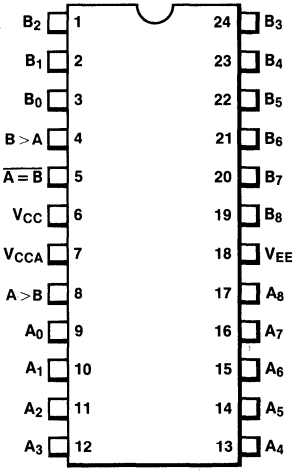
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

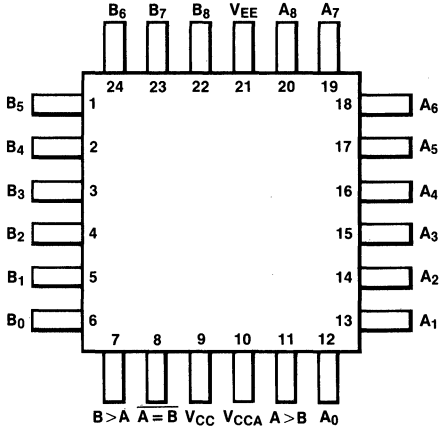
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4Q	FC

Connection Diagrams

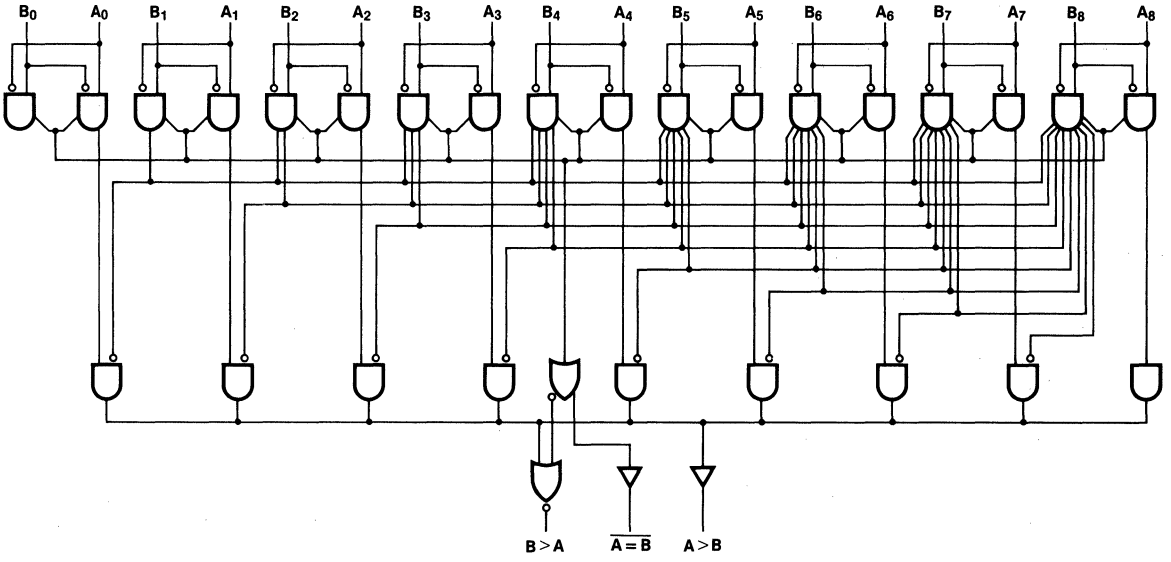
24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Logic Diagram



Truth Table

Inputs									Outputs		
A_8B_8	A_7B_7	A_6B_6	A_5B_5	A_4B_4	A_3B_3	A_2B_2	A_1B_1	A_0B_0	A > B	B > A	$\overline{A = B}$
H L									H	L	H
L H									L	H	H
$A_8 = B_8$	H L								H	L	H
$A_8 = B_8$	L H								L	H	H
$A_8 = B_8$	$A_7 = B_7$	H L							H	L	H
$A_8 = B_8$	$A_7 = B_7$	L H							L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	H L						H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	L H						L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	H L					H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	L H					L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	H L				H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	L H				L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	H L			H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	L H			L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	H L		H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	L H		L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	H L	H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	L H	L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L

H = HIGH Voltage Level L = LOW Voltage Level Blank = Don't Care

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current All Inputs			250	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−238	−170	−119	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

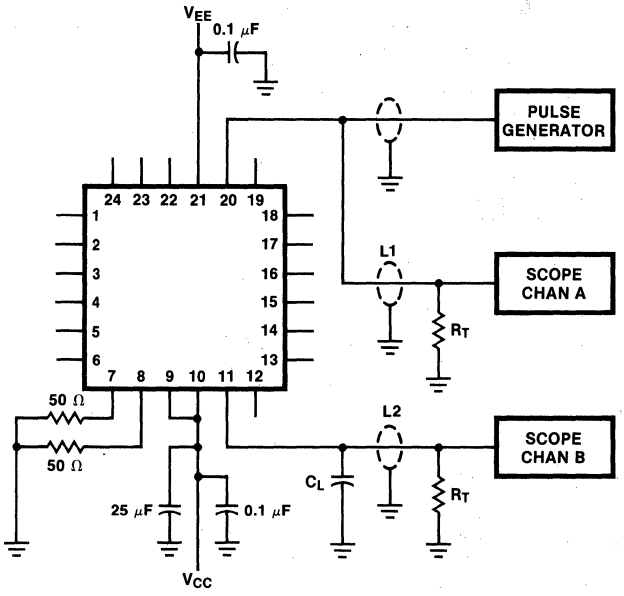
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.40	3.50	1.40	3.50	1.40	3.90	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.55	0.45	1.50	0.45	1.50	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.40	3.30	1.40	3.30	1.40	3.70	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.45	0.45	1.40	0.45	1.40	ns	

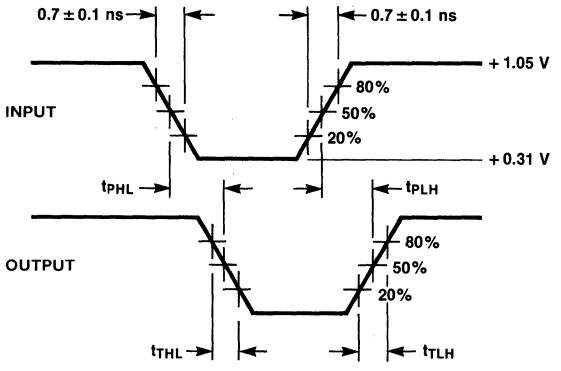
*See Family Characteristics for other dc specifications.

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Fig. 2 Propagation Delay and Transition Times



F100170
Universal Demultiplexer/ Decoder

F100K ECL Product

Description

The F100170 universal demultiplexer/decoder functions as either a dual 1-of-4 decoder or as a single 1-of-8 decoder, depending on the signal applied to the Mode Control (M) input. In the dual mode, each half has a pair of active-LOW Enable ($\overline{E}$) inputs. Pin assignments for the $\overline{E}$ inputs are such that in the 1-of-8 mode they can easily be tied together in pairs to provide two active-LOW enables ($\overline{E}_{1a}$ to $\overline{E}_{1b}$, $\overline{E}_{2a}$ to $\overline{E}_{2b}$). Signals applied to auxiliary inputs H_a, H_b and H_c determine whether the outputs are active HIGH or active LOW. In the dual 1-of-4 mode the Address inputs are A_{0a}, A_{1a} and A_{0b}, A_{1b} with A_{2a} unused (*i.e.*, left open, tied to V_{EE} or with LOW signal applied). In the 1-of-8 mode, the Address inputs are A_{0a}, A_{1a}, A_{2a} with A_{0b} and A_{1b} LOW or open.

Pin Names

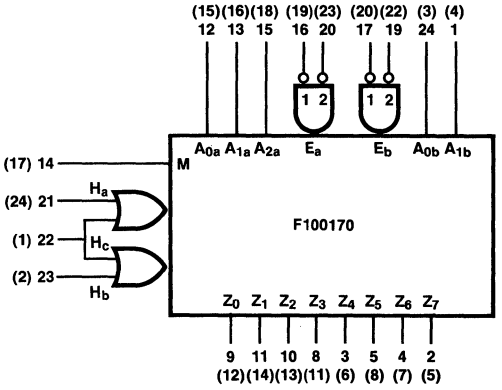
A_{na}, A_{nb}	Address Inputs
$\overline{E}_{na}$, $\overline{E}_{nb}$	Enable Inputs
M	Mode Control Input
H_a	Z_0–Z_3 ($\overline{Z}_{0a}$–$\overline{Z}_{3a}$) Polarity Select Input
H_b	Z_4–Z_7 ($\overline{Z}_{0b}$–$\overline{Z}_{03}$) Polarity Select Input
H_c	Common Polarity Select Input
Z_0–Z_7	Single 1-of-8 Data Outputs
Z_{na}, Z_{nb}	Dual 1-of-4 Data Outputs

Ordering Information (See Section 5)

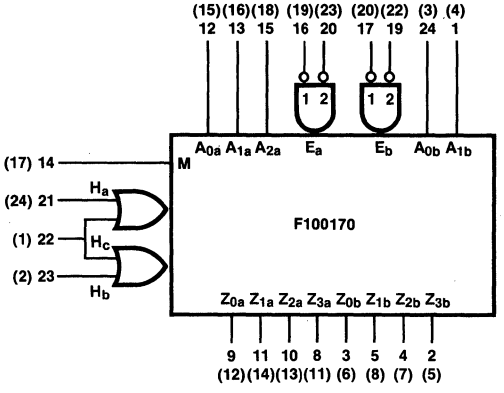
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Logic Symbols

Single 1-of-8 Application



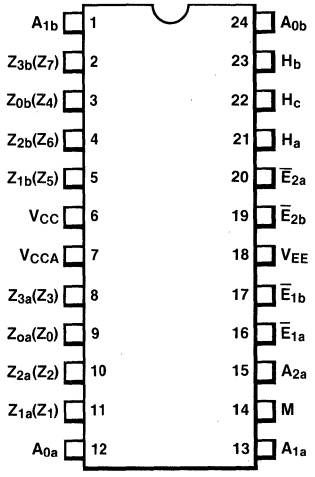
Dual 1-of-4 Application



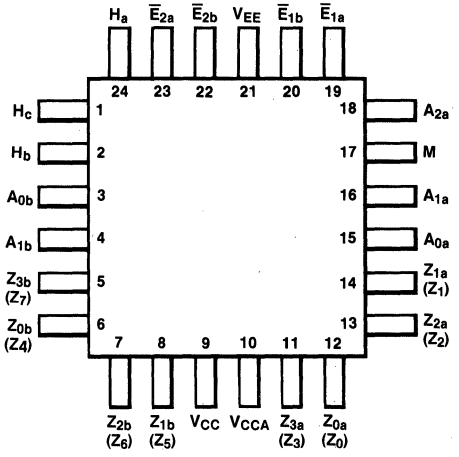
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Connection Diagrams

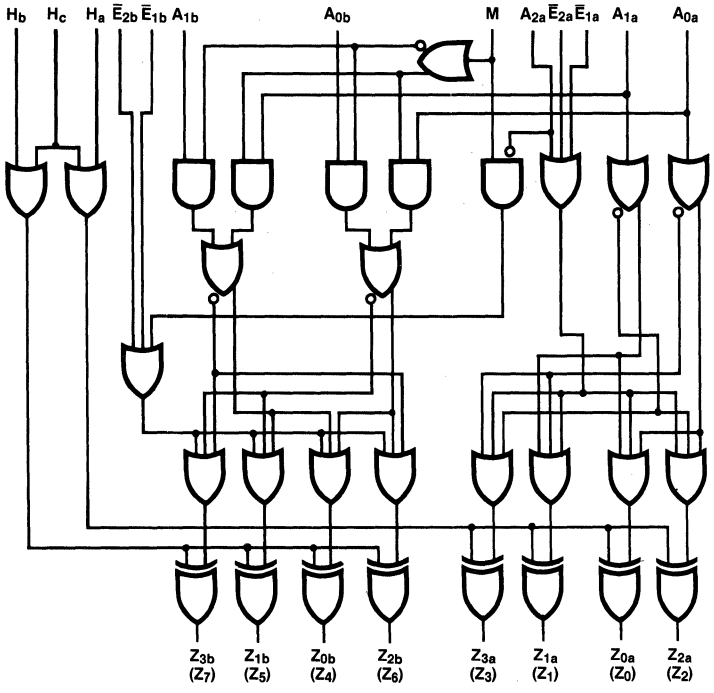
24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Logic Diagram



Note
(Z_n) for 1-of-4 applications

Truth Tables

Dual 1-of-4 Mode ($M = A_{2a} = H_c$ = LOW)

Inputs				Active HIGH Outputs (H_a and H_b inputs HIGH)				Active LOW Outputs (H_a and H_b inputs LOW)			
$\overline{E}_{1a}$ $\overline{E}_{1b}$	$\overline{E}_{2a}$ $\overline{E}_{2b}$	A_{1a} A_{1b}	A_{0a} A_{0b}	Z_{0a} Z_{0b}	Z_{1a} Z_{1b}	Z_{2a} Z_{2b}	Z_{3a} Z_{3b}	Z_{0a} Z_{0b}	Z_{1a} Z_{1b}	Z_{2a} Z_{2b}	Z_{3a} Z_{3b}
H	X	X	X	L	L	L	L	H	H	H	H
X	H	X	X	L	L	L	L	H	H	H	H
L	L	L	L	H	L	L	L	L	H	H	H
L	L	L	H	L	H	L	L	H	L	H	H
L	L	H	L	L	L	H	L	H	H	L	H
L	L	H	H	L	L	L	H	H	H	H	L

Single 1-of-8 Mode (M = HIGH; $A_{0b} = A_{1b} = H_a = H_b$ = LOW)

Inputs					Active HIGH Outputs* (H_c Input HIGH)							
$\overline{E}_1$	$\overline{E}_2$	A_{2a}	A_{1a}	A_{0a}	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
*for H_c = LOW, output states are complemented
$\overline{E}_1 = \overline{E}_{1a}$ and $\overline{E}_{1b}$ wired; $\overline{E}_2 = \overline{E}_{2a}$ and $\overline{E}_{2b}$ wired

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current H_c, A_{0a}, A_{1a}, A_{2a} All Others			310 250	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−153	−109	−76	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

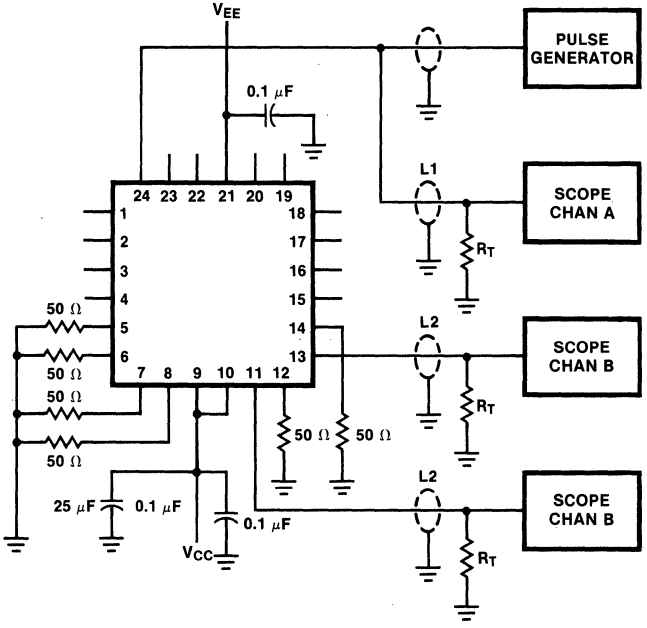
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_{na}$, $\overline{E}_{nb}$ to Output	0.90	2.30	0.90	2.20	0.90	2.30	ns	
t_{PLH} t_{PHL}	Propagation Delay A_{na}, A_{nb} to Output	1.00	2.80	1.00	2.70	1.00	2.90	ns	
t_{PLH} t_{PHL}	Propagation Delay H_a, H_b, H_c to Output	1.00	3.00	1.00	2.90	1.00	3.00	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay M to Output	1.50	3.90	1.60	3.80	1.60	3.90	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.80	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_{na}$, $\overline{E}_{nb}$ to Output	0.90	2.10	0.90	2.00	0.90	2.10	ns	
t_{PLH} t_{PHL}	Propagation Delay A_{na}, A_{nb} to Output	1.00	2.60	1.00	2.50	1.00	2.70	ns	
t_{PLH} t_{PHL}	Propagation Delay H_a, H_b, H_c to Output	1.00	2.80	1.00	2.70	1.00	2.80	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay M to Output	1.50	3.70	1.60	3.60	1.60	3.70	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.60	0.45	1.70	ns	

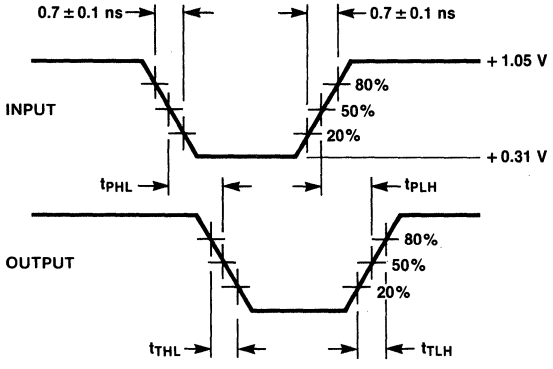
*See Family Characteristics for other dc specifications.

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Fig. 2 Propagation Delay and Transition Times



F100171
Triple 4-Input Multiplexer with Enable

F100K ECL Product

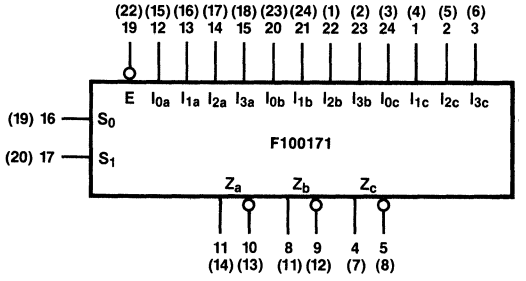
Description

The F100171 contains three 4-input multiplexers which share a common decoder (inputs S_0 and S_1). Output buffer gates provide true and complement outputs. A HIGH on the Enable input ($\overline{E}$) forces all true outputs LOW (see Truth Table).

Pin Names

$I_{0x} - I_{3x}$	Data Inputs
S_0, S_1	Select Inputs
$\overline{E}$	Enable Input (Active LOW)
$Z_a - Z_c$	Data Outputs
$\overline{Z}_a - \overline{Z}_c$	Complementary Data Outputs

Logic Symbol



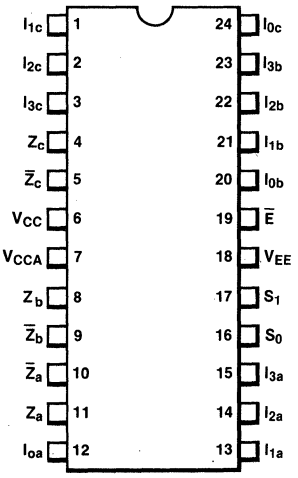
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

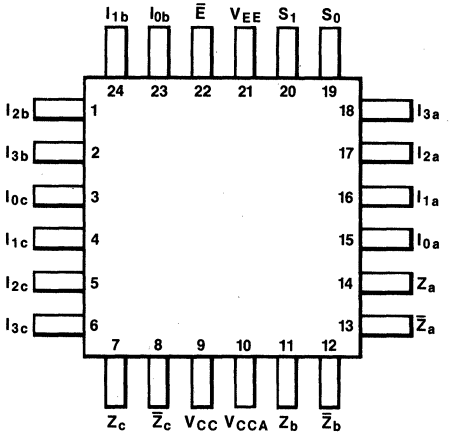
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Connection Diagrams

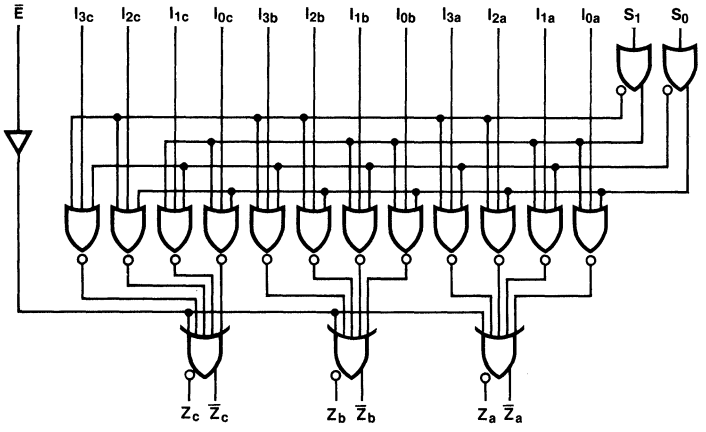
24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Logic Diagram



Truth Table

Inputs			Outputs
$\overline{E}$	S_0	S_1	Z_n
L	L	L	I_{0x}
L	H	L	I_{1x}
L	L	H	I_{2x}
L	H	H	I_{3x}
H	X	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current I_{0x}–I_{3x} S_0, S_1, $\overline{E}$			340 300	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−114	−80	−56	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

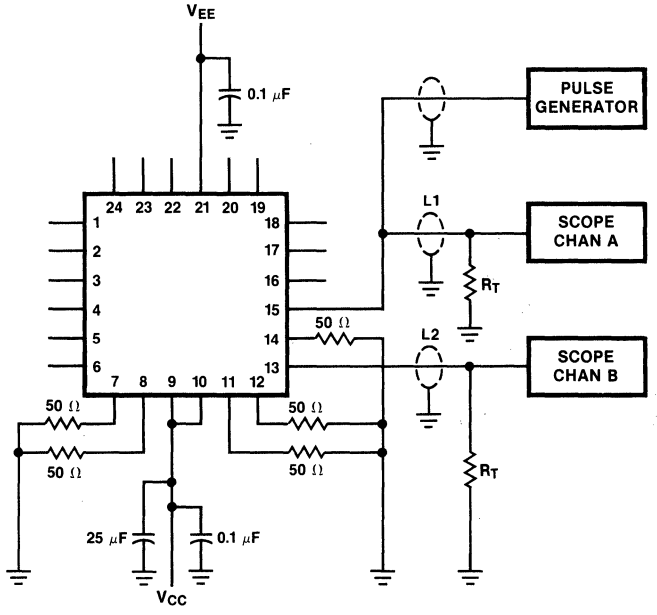
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay I_{0x}–I_{3x} to Output	0.45	1.70	0.45	1.60	0.50	1.70	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	0.90	2.40	0.90	2.60	1.00	3.00	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Output	0.65	2.40	0.65	2.30	0.75	2.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.60	0.45	1.60	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay I_{0x}–I_{3x} to Output	0.45	1.50	0.45	1.40	0.50	1.50	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	0.90	2.20	0.90	2.40	1.00	2.80	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Output	0.65	2.20	0.65	2.10	0.75	2.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.50	0.45	1.50	ns	

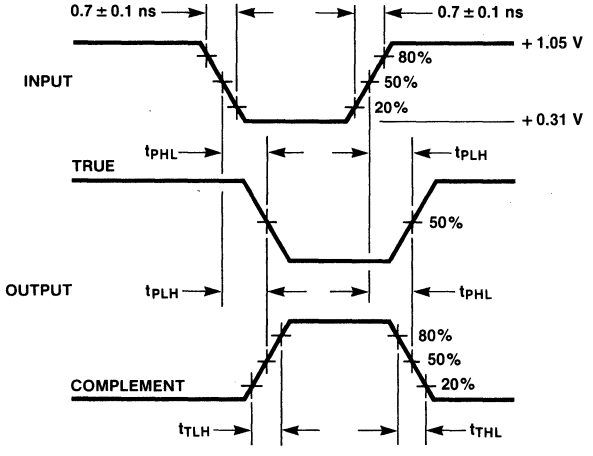
*See Family Characteristics for other dc specifications.

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Fig. 2 Propagation Delay and Transition Times



F100179
Carry Lookahead Generator

F100K ECL Product

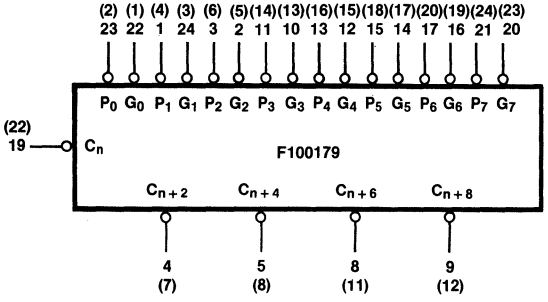
Description

The F100179 is a high-speed Carry Lookahead Generator intended for use with the F100180 6-bit fast Adder and the F100181 4-bit ALU.

Pin Names

$\overline{C}_n$	Carry Input (Active LOW)
$\overline{P}_0$–$\overline{P}_7$	Carry Propagate Inputs (Active LOW)
$\overline{G}_0$–$\overline{G}_7$	Carry Generate Inputs (Active LOW)
$\overline{C}_{n+2}$, $\overline{C}_{n+4}$ $\overline{C}_{n+6}$, $\overline{C}_{n+8}$	Carry Outputs

Logic Symbol



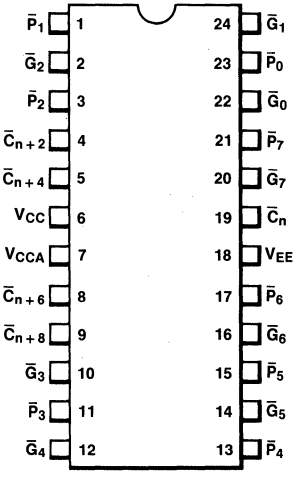
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

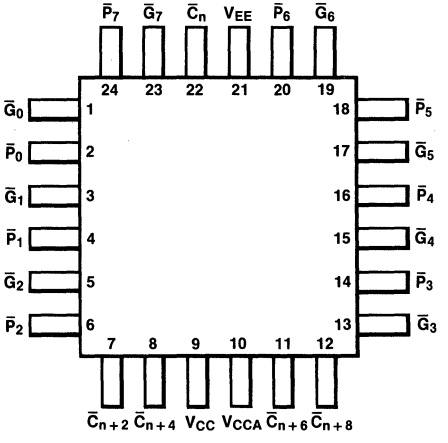
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4Q	FC

Connection Diagrams

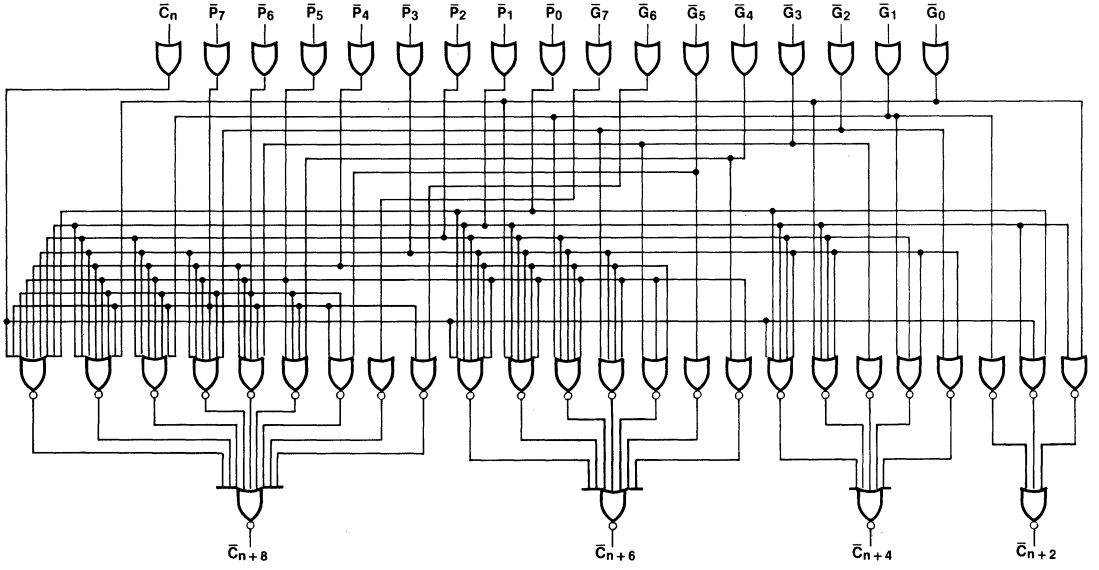
24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Logic Diagram



Truth Tables

$\overline{C}_{n+2}$ Output

Inputs					Output
$\overline{C}_n$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{C}_{n+2}$
X	X	X	L	X	L
X	L	X	X	L	L
L	X	L	X	L	L
All other combinations					H

$\overline{C}_{n+2} = \overline{G}_1 \bullet (\overline{P}_1 + \overline{G}_0) \bullet (\overline{P}_1 + \overline{P}_0 + \overline{C}_n)$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

$\overline{C}_{n+4}$ Output

Inputs									Output
$\overline{C}_n$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	$\overline{C}_{n+4}$
X	X	X	X	X	X	X	L	X	L
X	X	X	X	X	L	X	X	L	L
X	X	X	L	X	X	L	X	L	L
X	L	X	X	L	X	L	X	L	L
L	X	L	X	L	X	L	X	L	L
All other combinations									H

$\overline{C}_{n+4} = \overline{G}_3 \bullet (\overline{P}_3 + \overline{G}_2) \bullet (\overline{P}_3 + \overline{P}_2 + \overline{G}_1) \bullet (\overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0)$
$\bullet (\overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_n)$

Truth Tables (Cont'd)

$\overline{C}_{n+6}$ Output

Inputs												Output
$\overline{C}_n$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	$\overline{G}_4$	$\overline{P}_4$	$\overline{G}_5$	$\overline{P}_5$	$\overline{C}_{n+6}$
X	X	X	X	X	X	X	X	X	X	X	L	X	L
X	X	X	X	X	X	X	X	X	L	X	X	L	L
X	X	X	X	X	X	X	L	X	X	L	X	L	L
X	X	X	X	X	L	X	X	L	X	L	X	L	L
X	X	X	L	X	X	L	X	L	X	L	X	L	L
X	L	X	X	L	X	L	X	L	X	L	X	L	L
L	X	L	X	L	X	L	X	L	X	L	X	L	L
All other combinations													H

$$\overline{C}_{n+6} = \overline{G}_5 \bullet (\overline{P}_5 + \overline{G}_4) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{G}_3) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{G}_2) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{G}_1) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_n)$$

$\overline{C}_{n+8}$ Output

Inputs																Output
$\overline{C}_n$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	$\overline{G}_4$	$\overline{P}_4$	$\overline{G}_5$	$\overline{P}_5$	$\overline{G}_6$	$\overline{P}_6$	$\overline{G}_7$	$\overline{P}_7$	$\overline{C}_{n+8}$
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	L
X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	L	L
X	X	X	X	X	X	X	X	X	X	X	L	X	X	L	X	L	L
X	X	X	X	X	X	X	X	X	L	X	X	L	X	L	X	L	L
X	X	X	X	X	X	X	L	X	X	L	X	L	X	L	X	L	L
X	X	X	X	X	L	X	X	L	X	L	X	L	X	L	X	L	L
X	X	X	L	X	X	L	X	L	X	L	X	L	X	L	X	L	L
X	L	X	X	L	X	L	X	L	X	L	X	L	X	L	X	L	L
L	X	L	X	L	X	L	X	L	X	L	X	L	X	L	X	L	L
All other combinations																	H

$$\overline{C}_{n+8} = \overline{G}_7 \bullet (\overline{P}_7 + \overline{G}_6) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{G}_5) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{G}_4) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{G}_3) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{G}_2) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{G}_1) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_n)$$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current $\overline{C}_n$, $\overline{G}_0$–$\overline{G}_7$ $\overline{P}_0$–$\overline{P}_7$			250 340	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−220	−150	−100	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

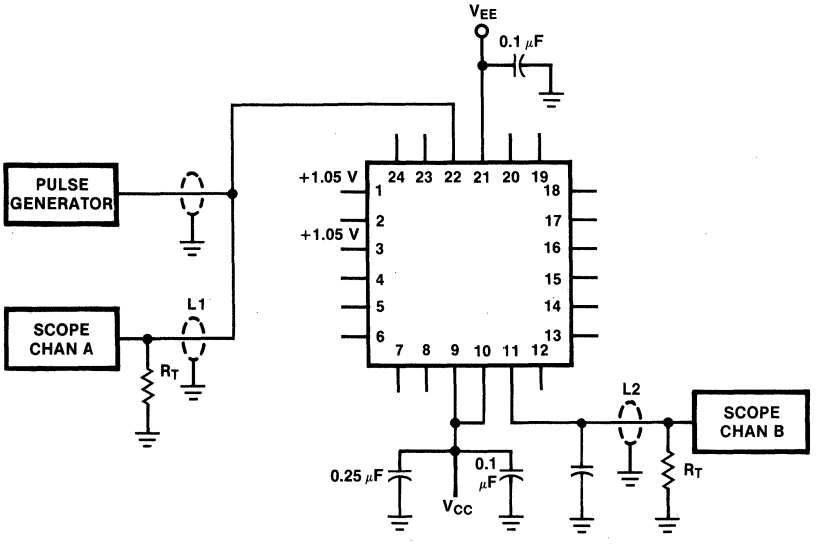
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$, $\overline{G}_0$–$\overline{G}_7$, $\overline{P}_0$–$\overline{P}_7$ to $\overline{C}_{n+x}$	1.10	2.90	1.10	2.90	1.10	3.00	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.80	0.45	1.80	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$, $\overline{G}_0$–$\overline{G}_7$, $\overline{P}_0$–$\overline{P}_7$ to $\overline{C}_{n+x}$	1.10	2.70	1.10	2.70	1.10	2.80	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.70	ns	

*See Family Characteristics for other dc specifications.

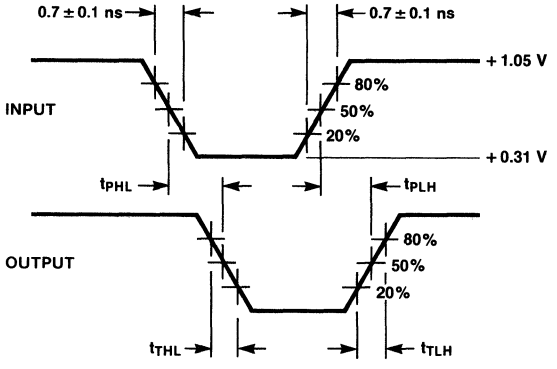
Fig. 1 AC Test Circuit



Notes

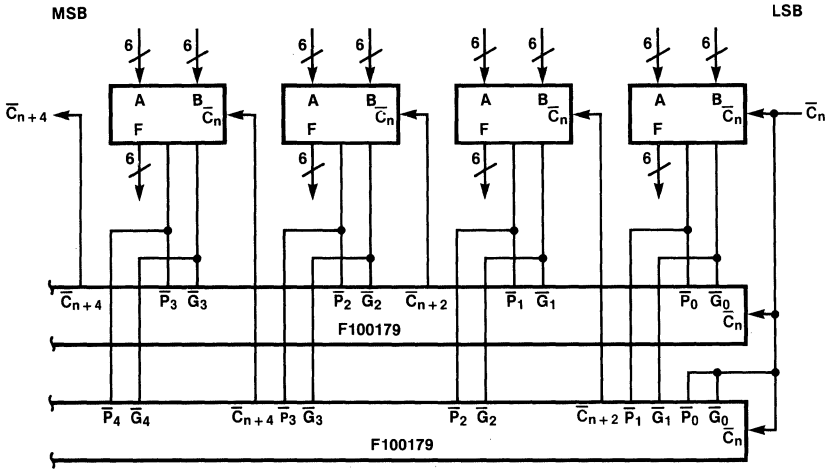
V_{CC}, V_{CCA} = +2 V, V_{EE} = −2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Fig. 2 Propagation Delay and Transition Times

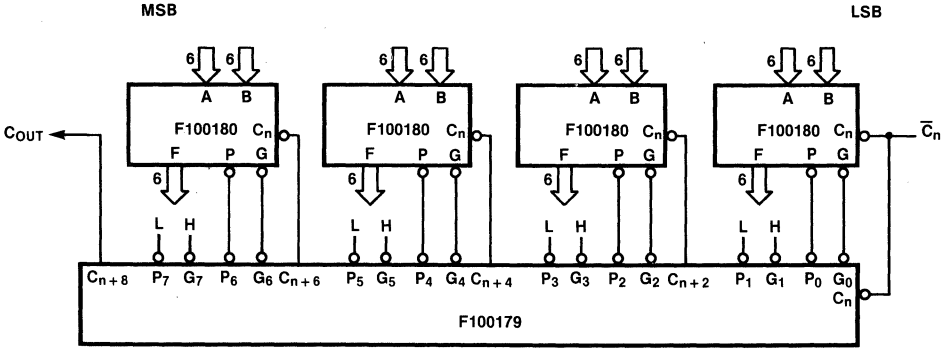


Applications

Fast Adder and Carry Lookahead



24-Bit Adder Using One Carry Lookahead



F100180
High-Speed 6-Bit Adder

F100K ECL Product

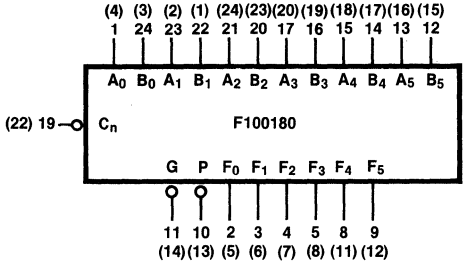
Description

The F100180 is a high-speed 6-bit adder capable of performing a full 6-bit addition of two operands. Inputs for the adder are active-LOW Carry, Operand A, and Operand B; outputs are Function, active-LOW Carry Generate, and active-LOW Carry Propagate. When used with the F100179 Full Carry Lookahead as a second order lookahead block, the F100180 provides high-speed addition of very long words.

Pin Names

A_0–A_5	Operand A Inputs
B_0–B_5	Operand B Inputs
$\overline{C}_n$	Carry Input (Active LOW)
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)
F_0–F_5	Function Outputs

Logic Symbol



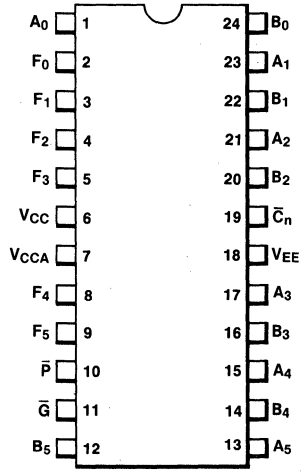
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

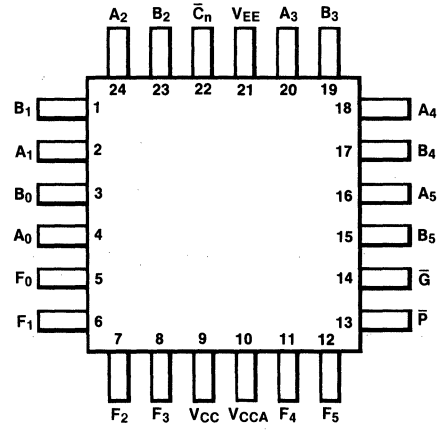
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4Q	FC

Connection Diagrams

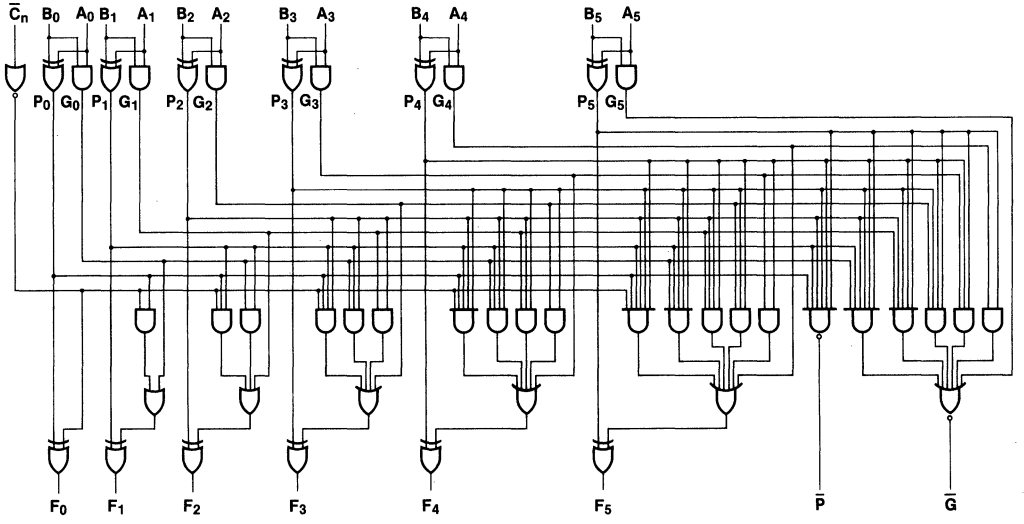
24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Logic Diagram



Logic Equations

$P_i = A_i \oplus B_i$

$G_i = A_i B_i$

$i = 0, 1, 2, 3, 4, 5$

$F_0 = P_0 \oplus C_n$

$F_1 = P_1 \oplus (G_0 + P_0 C_n)$

$F_2 = P_2 \oplus (G_1 + P_1 G_0 + P_1 P_0 C_n)$

$F_3 = P_3 \oplus (G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n)$

$F_4 = P_4 \oplus (G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_n)$

$F_5 = P_5 \oplus (G_4 + P_4 G_3 + P_4 P_3 G_2 + P_4 P_3 P_2 G_1 + P_4 P_3 P_2 P_1 G_0 + P_4 P_3 P_2 P_1 P_0 C_n)$

$\overline{P} = \overline{P_0 P_1 P_2 P_3 P_4 P_5}$

$\overline{G} = \overline{G_5 + P_5 G_4 + P_5 P_4 G_3 + P_5 P_4 P_3 G_2 + P_5 P_4 P_3 P_2 G_1 + P_5 P_4 P_3 P_2 P_1 G_0}$

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current All Inputs			220	μA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	−290	−195	−135	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

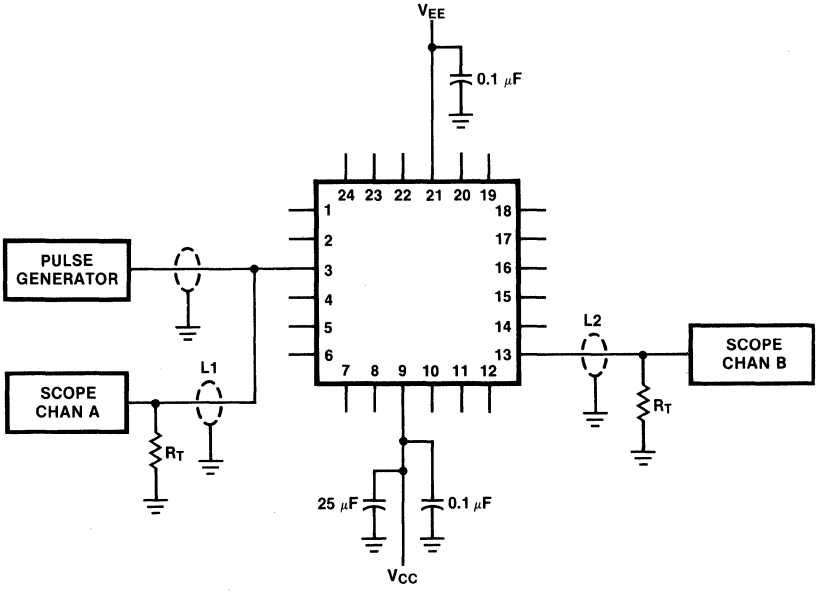
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to F_n	1.10	4.70	1.10	4.60	1.10	4.70	ns	
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{P}$	1.00	3.00	1.00	3.00	1.00	3.30	ns	
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{G}$	1.40	3.90	1.40	3.80	1.40	3.90	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to F_n	1.10	4.00	1.10	3.90	1.10	4.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.40	0.45	2.30	0.45	2.40	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to F_n	1.10	4.50	1.10	4.40	1.10	4.50	ns	
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{P}$	1.00	2.80	1.00	2.80	1.00	3.10	ns	
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{G}$	1.40	3.70	1.40	3.60	1.40	3.70	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to F_n	1.10	3.80	1.10	3.70	1.10	3.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.30	0.45	2.20	0.45	2.30	ns	

*See Family Characteristics for other dc specifications.

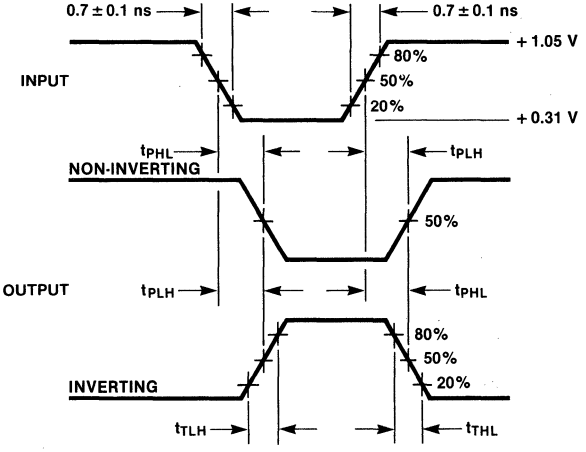
Fig. 1 AC Test Circuit



Notes

V_{CC}, V_{CCA} = +2 V, V_{EE} = −2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Fig. 2 Propagation Delay and Transition Times



F100181
4-Bit Binary/BCD Arithmetic Logic Unit

F100K ECL Product

Description

The F100181 performs eight logic operations and eight arithmetic operations on a pair of 4-bit words. The operating mode is determined by signals applied to the Select (S_n) inputs, as shown in the Function Select table. In addition to performing binary arithmetic, the circuit contains the necessary correction logic to perform BCD addition and subtraction. Output latches are provided to reduce overall package count and increase system operating speed. When the latches are not required, leaving the Enable ($\overline{E}$) input LOW makes the latches transparent.

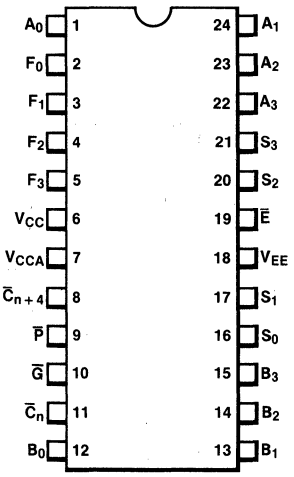
The circuit uses internal lookahead carry to minimize delay to the F_n outputs and to the ripple Carry output, $\overline{C}_{n+4}$. Group Carry Lookahead Propagate ($\overline{P}$) and Generate ($\overline{G}$) outputs are also provided, which are independent of the Carry input $\overline{C}_n$. The $\overline{P}$ output goes LOW when a plus operation produces fifteen (nine for BCD) or when a minus operation produces zero. Similarly, $\overline{G}$ goes LOW when the sum of A and B is greater than fifteen (nine for BCD) in a plus mode, or when their difference is greater than zero in a minus mode.

Pin Names

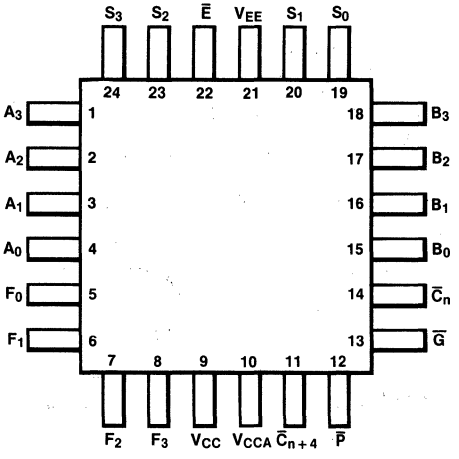
A_0–A_3	Word A Operand Inputs
B_0–B_3	Word B Operand Inputs
$\overline{C}_n$	Carry Input (Active LOW)
S_0–S_3	Function Select Inputs
$\overline{E}$	Latch Enable Input (Active LOW)
$\overline{P}$	Carry Lookahead Propagate Output (Active Low)
$\overline{G}$	Carry Lookahead Generate Output (Active LOW)
$\overline{C}_{n+4}$	Carry Output
F_0–F_3	Function Outputs

Connection Diagrams

24-Pin DIP (Top View)



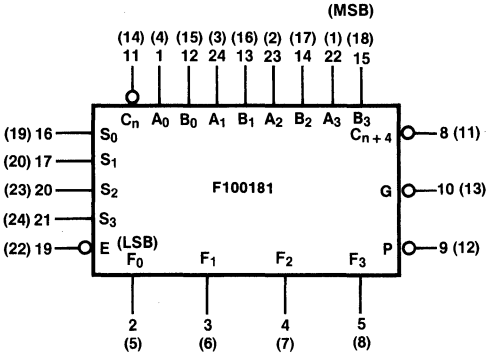
24-Pin Flatpak (Top View)



Ordering Information (See Section 5)

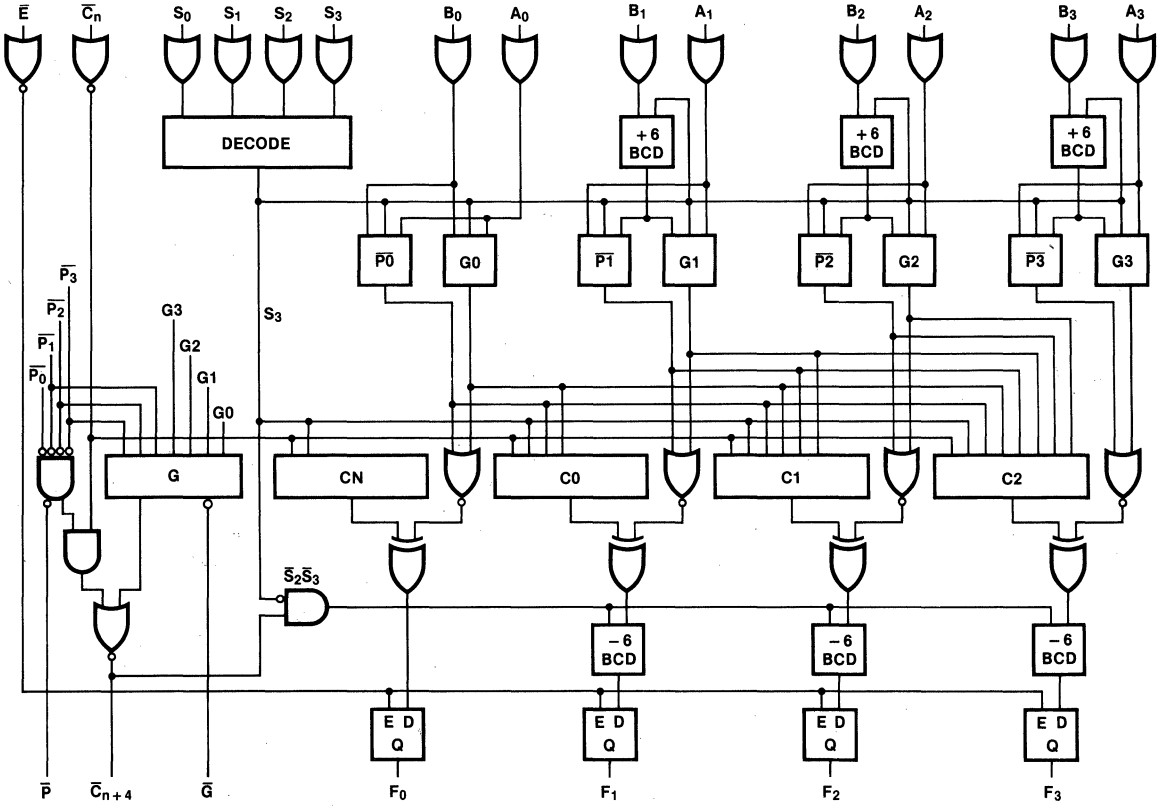
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4Q	FC

Logic Symbol

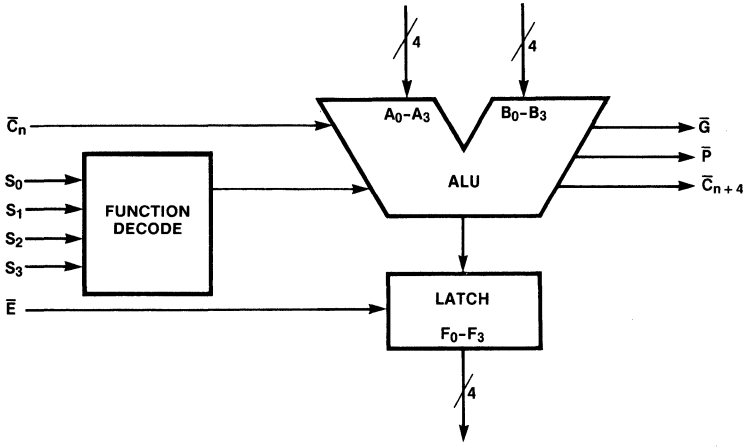


V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Logic Diagram



Block Diagram



Functional Description

There are two modes of operation: Arithmetic and Logic. The S_3 input controls these two modes:

S_3 = LOW for Arithmetic mode
S_3 = HIGH for Logic mode

The arithmetic mode includes decimal and binary arithmetic operations. S_2 is the control input: with S_3 = LOW,

S_2 = LOW for Decimal Arithmetic (BCD)
S_2 = HIGH for Binary Arithmetic

Decimal Arithmetic Operation

Addition
F = A plus B plus C_n. Arguments A and B are directly applied to the inputs. The circuit automatically performs the "+6" and "−6" logic correction internally.

Subtraction
F = A minus B plus C_n. Arguments A and B are directly applied to the inputs. The circuit automatically takes the nines complement of B and adds "+6". A "−6" adjustment is made if the subtraction algorithm calls for it. If there is a carry out, the result is a positive number. With no carry out, the result is a negative number expressed in its nines complement form. Therefore, to perform a subtraction with results in the tens complement form, an initial carry should be forced into the lowest order bit, *i.e.*, set $\overline{C}_n$ = LOW.

(tens complement of B) = (nines complement of B) + 1

F = B minus A plus C_n. Operation is similar to and results are the same as F = A minus B plus C_n.

Binary Arithmetic Operation

Addition
F = A minus B plus C_n. Arguments A and B are directly applied to the inputs.

Subtraction
F = A minus B plus C_n. Arguments A and B are directly applied to the inputs. The circuit automatically takes the ones complement of B (by inverting B internally). If there is a carry out the result is a positive number. With no carry out, the result is a negative number expressed in its ones complement form. Therefore, to perform a subtraction with results in the twos complement form, an initial carry should be forced into the lowest order bit, *i.e.*, set $\overline{C}_n$ = LOW.

(twos complement of B) = (ones complement of B) + 1

F = B minus A plus C_n. Operation is similar and results are the same as F = A minus B plus C_n.

Function Table

S_3	S_2	S_1	S_0	F_n Function	G_n (n = 0 to 3)	P_n (n = 0 to 3)	Outputs		
					Internal Signals		$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	L	L	L	F_n = A plus B plus C_n (BCD)	A_nD_n	$A_n + D_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	L	L	H	F_n = A minus B plus C_n (BCD)	$A_n\overline{B}_n$	$A_n + \overline{B}_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	L	H	L	F_n = B minus A plus C_n (BCD)	$\overline{A}_nB_n$	$\overline{A}_n + B_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	L	H	H	F_n = 0 minus B plus C_n (BCD)	L	$\overline{B}_n$	$\overline{C}_{n+4}$	H	$\overline{P}$
L	H	L	L	F_n = A plus B plus C_n (Binary)	A_nB_n	$A_n + B_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	H	L	H	F_n = A minus B plus C_n (Binary)	$A_n\overline{B}_n$	$A_n + \overline{B}_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	H	H	L	F_n = B minus A plus C_n (Binary)	$\overline{A}_nB_n$	$\overline{A}_n + B_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	H	H	H	F_n = 0 minus B plus C_n (Binary)	L	$\overline{B}_n$	$\overline{C}_{n+4}$	H	$\overline{P}$
H	L	L	L	$F_n = A_nB_n + \overline{A}_n\overline{B}_n$	A_nB_n	$A_n + B_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
H	L	L	H	$F_n = A_n\overline{B}_n + \overline{A}_nB_n$	$A_n\overline{B}_n$	$A_n + \overline{B}_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
H	L	H	L	$F_n = A_n + B_n$	A_n	$\overline{B}_n$	$\overline{C}_{n+4}$	$\overline{G}_x$	$\overline{P}$
H	L	H	H	$F_n = A_n$	A_n	H	$\overline{C}_{n+4}$	$\overline{G}$	L
H	H	L	L	$F_n = \overline{B}_n$	L	B_n	L	H	$\overline{P}$
H	H	L	H	$F_n = B_n$	L	$\overline{B}_n$	L	H	$\overline{P}$
H	H	H	L	$F_n = A_nB_n$	L	$\overline{A}_n + \overline{B}_n$	L	H	$\overline{P}$
H	H	H	H	F_n = LOW	L	H	L	H	L

H = HIGH Voltage Level
L = LOW Voltage Level

$$\overline{P} = \overline{P}_0 + \overline{P}_1 + \overline{P}_2 + \overline{P}_3$$
$$\overline{G} = G_3 + P_3G_2 + P_3P_2P_1 + P_3P_2P_1G_0$$
$$\overline{C}_{n+4} = \overline{G} \cdot (\overline{P} + \overline{C}_n)$$

Arithmetic Operations

$$F_n = \overline{G_n + \overline{P}_n} \oplus C_i \qquad i = 0 \text{ to } 3$$

Logic Operations

$$F_n = G_n + \overline{P}_n$$

Internal Equations for Carry Lookahead

(i = 0, 1, 2, 3)

$$C_0 = C_n + S_3$$
$$C_1 = G_0 + P_0C_n + S_3$$
$$C_2 = G_1 + P_1G_0 + P_1P_0C_n + S_3$$
$$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n + S_3$$

Internal Equations for +6 Logic

$$D_0 = B_0$$
$$D_1 = \overline{B}_1$$
$$D_2 = B_1B_2 + \overline{B}_1\overline{B}_2$$
$$D_3 = B_1 + B_2 + B_3$$
$$\overline{G}_x = \overline{G_3P_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current S_n, $\overline{E}$ All Others			 350 250	μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	−300	−210	−130	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

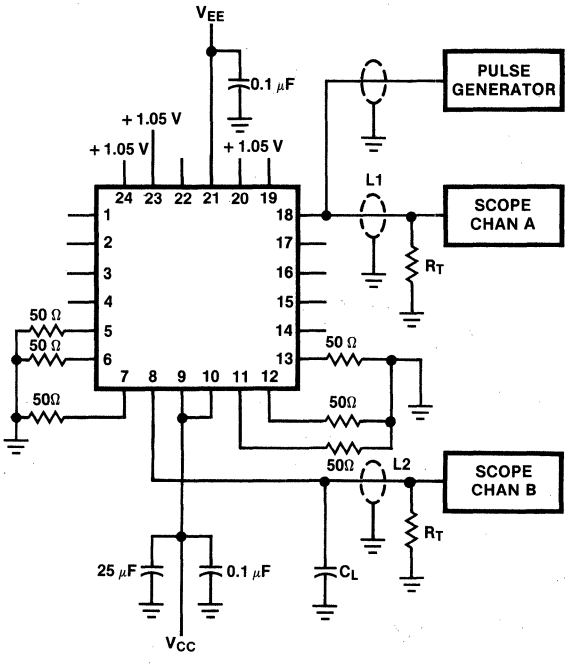
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to F_n	2.00	6.90	2.10	6.80	2.30	7.40	ns	
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{P}$, $\overline{G}$	1.40	4.70	1.40	4.40	1.40	4.70	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{C}_{n+4}$	2.00	6.50	2.00	6.50	2.10	6.80	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to F_n	1.60	5.10	1.60	5.20	1.60	5.50	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to $\overline{C}_{n+4}$	1.30	3.00	1.40	3.00	1.40	3.10	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to F_n	1.40	8.80	1.50	8.60	1.50	9.00	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{P}$, $\overline{G}$	1.70	7.40	2.00	5.90	2.00	6.50	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{C}_{n+4}$	2.70	10.10	2.80	8.50	2.90	8.70	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to F_n	1.00	3.40	0.90	3.60	1.10	3.80	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.70	0.45	2.60	0.45	2.70	ns	*Figures 1* and *2*
t_s	Setup Time A_n, B_n S_n $\overline{C}_n$	 7.60 8.70 4.80		 7.60 8.50 5.00		 8.10 9.60 5.30		ns	*Figure 3*
t_h	Hold Time A_n, B_n S_n $\overline{C}_n$	 0.10 0.60 0.60		 0.10 0.60 0.60		 0.10 0.60 0.60		ns	
$t_{pw}(L)$	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 2*

*See Family Characteristics for other dc specifications.

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to F_n	2.00	6.70	2.10	6.60	2.30	7.20	ns	
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{P}$, $\overline{G}$	1.40	4.50	1.40	4.20	1.40	4.50	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{C}_{n+4}$	2.00	6.30	2.00	6.30	2.10	6.60	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to F_n	1.60	4.90	1.60	5.00	1.60	5.30	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to $\overline{C}_{n+4}$	1.30	2.80	1.40	2.80	1.40	2.90	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_n to F_n	1.40	8.60	1.50	8.40	1.50	8.80	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{P}$, $\overline{G}$	1.70	7.20	2.00	5.70	2.00	6.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{C}_{n+4}$	2.70	9.90	2.80	8.30	2.90	8.50	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to F_n	1.00	3.20	0.90	3.40	1.10	3.60	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.60	0.45	2.50	0.45	2.60	ns	*Figures 1* and *2*
t_s	Setup Time A_n, B_n S_n $\overline{C}_n$	 7.50 8.60 4.70		 7.50 8.40 4.90		 8.00 9.50 5.20		ns	*Figure 3*
t_h	Hold Time A_n, B_n S_n $\overline{C}_n$	 0 0.50 0.50		 0 0.50 0.50		 0 0.50 0.50		ns	
$t_{pw}(L)$	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 2*

Fig. 1 AC Test Circuit



Notes

V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Fig. 2 Enable Timing

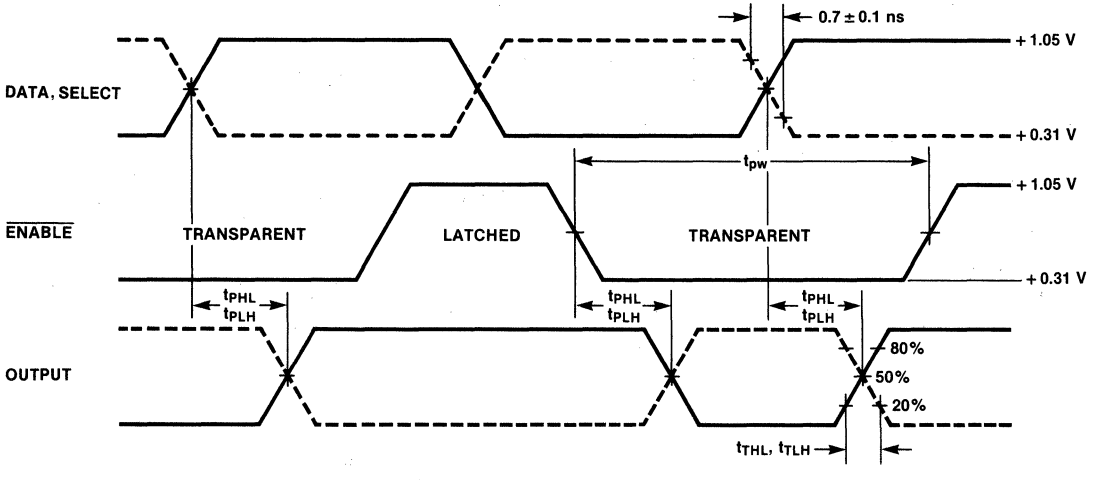
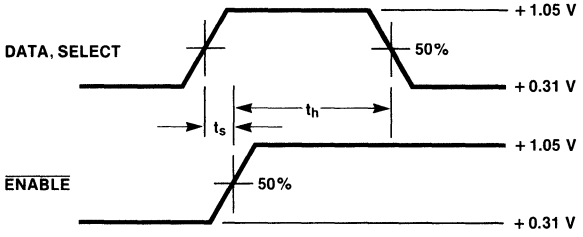


Fig. 3 Setup and Hold Times



Notes

t_s is the minimum time before the transition of the enable that information must be present at the data input

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input

F100182
9-Bit Wallace Tree Adder

F100K ECL Product

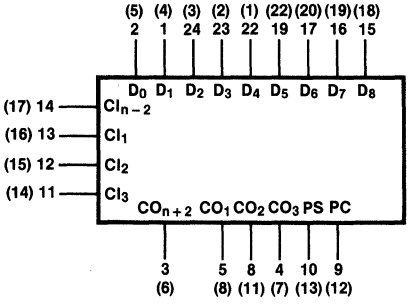
Description

The F100182 is a 9-bit Wallace tree adder. It is designed to assist in performing high-speed hardware multiplication. The device is designed to add 9-bits of data 1-bit-slice wide and handle the carry-ins from the previous slices. The F100182 is easily expanded and still maintains four levels of delay regardless of input string length. In conjunction with the F100183 Recode Multiplier, the F100179 Carry Lookahead, and the F100180 High-speed Adder, the F100182 assists in performing parallel multiplication of two signed numbers to produce a signed twos complement product. See F100183 data sheet for additional information.

Pin Names

D_0–D_8	Data Inputs
CI_1–CI_3, CI_{n-2}	Carry Inputs
CO_1–CO_3, CO_{n+2}	Carry Outputs
PS	Partial Sum Output
PC	Partial Carry Output

Logic Symbol



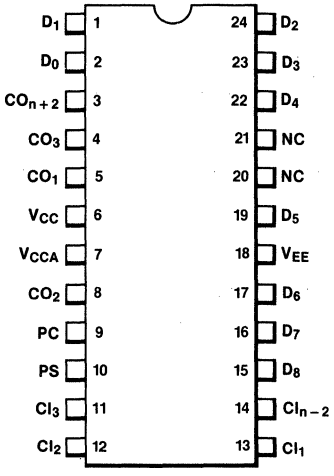
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
NC = Pins 20 (23), 21 (24)
( ) = Flatpak

Ordering Information (See Section 5)

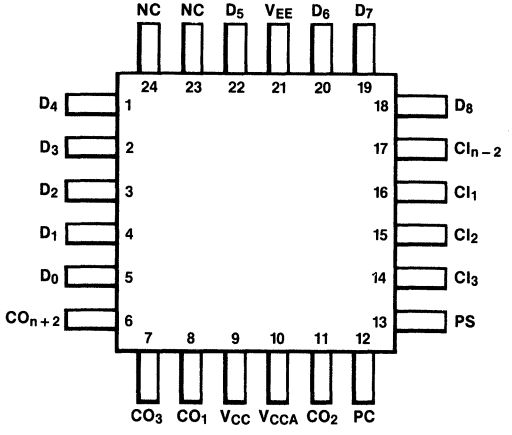
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4Q	FC

Connection Diagrams

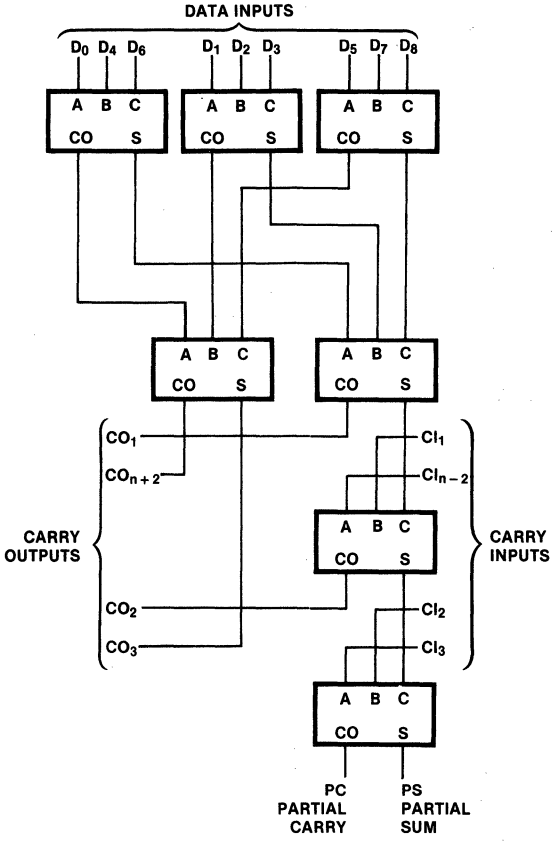
24-Pin DIP (Top View)



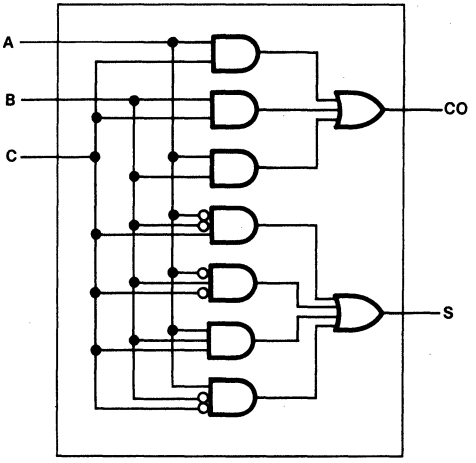
24-Pin Flatpak (Top View)



Logic Diagram



Adder Logic Diagram



Adder Truth Table

Inputs			Outputs	
A	B	C	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current CI_1–CI_3, CI_{n-2} D_1, D_3, D_4, D_5, D_6, D_8			300	μA	V_{IN} = $V_{IH(max)}$
	D_0, D_2, D_7			250		
I_{EE}	Power Supply Current	−260	−180	−125	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

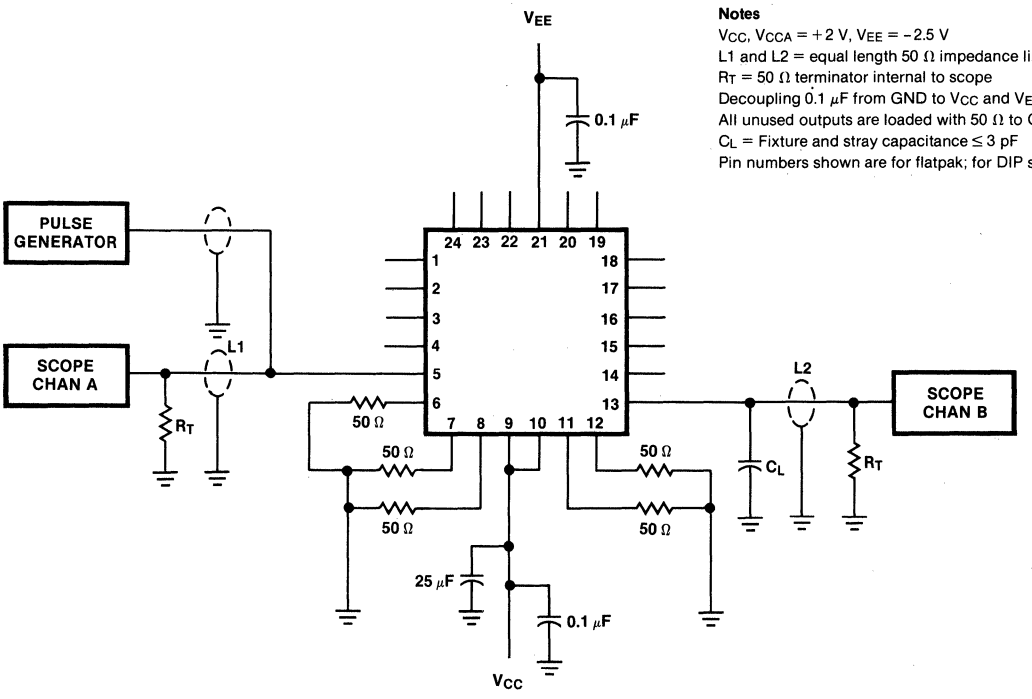
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_{n+2}	1.40	4.50	1.40	4.50	1.50	4.70	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_1	1.30	4.80	1.30	4.70	1.50	5.00	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_2	2.20	6.20	2.20	6.10	2.30	6.40	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_3	1.30	4.70	1.40	4.70	1.50	5.00	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to PS, PC	2.50	7.20	2.50	7.20	2.70	7.40	ns	
t_{PLH} t_{PHL}	Propagation Delay CI_{n-2}, CI_1 to CO_2	1.00	3.50	1.00	3.40	1.10	3.70	ns	
t_{PLH} t_{PHL}	Propagation Delay CI_{n-2}, CI_1 to PS, PC	1.50	4.50	1.50	4.45	1.60	4.60	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay CI_3, CI_2 to PS, PC	0.80	3.30	0.80	3.20	0.90	3.60	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.60	0.45	1.60	ns	*Figures 1* and *2*

*See Family Characteristics for other dc specifications.

Flatpak AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

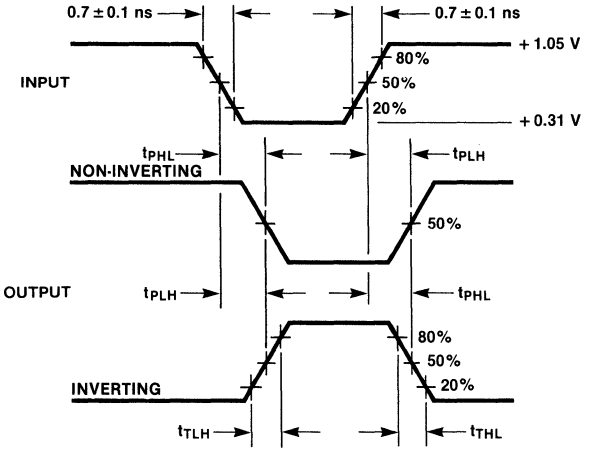
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Condition**
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_{n+2}	1.40	4.30	1.40	4.30	1.50	4.50	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_1	1.30	4.60	1.30	4.50	1.50	4.80	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_2	2.20	6.00	2.20	5.90	2.30	6.20	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_3	1.30	4.50	1.40	4.50	1.50	4.80	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to PS, PC	2.50	7.00	2.50	7.00	2.70	7.20	ns	
t_{PLH} t_{PHL}	Propagation Delay CI_{n-2}, CI_1 to CO_2	1.00	3.30	1.00	3.20	1.10	3.50	ns	
t_{PLH} t_{PHL}	Propagation Delay CI_{n-2}, CI_1 to PS, PC	1.50	4.30	1.50	4.25	1.60	4.40	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay CI_3, CI_2 to PS, PC	0.80	3.10	0.80	3.00	0.90	3.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.50	0.45	1.50	ns	*Figures 1* and *2*

Fig. 1 AC Test Circuit



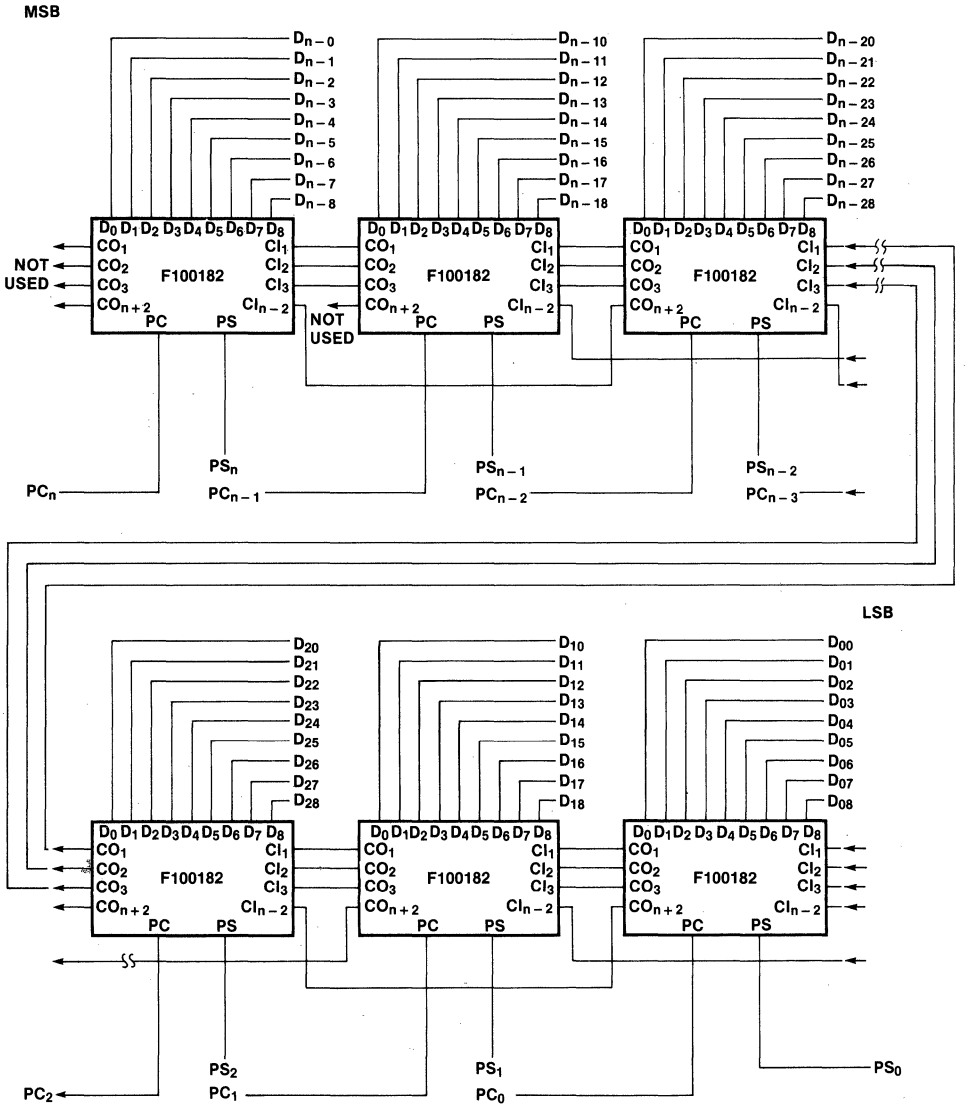
Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = −2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Fig. 2 Propagation Delay and Transition Times

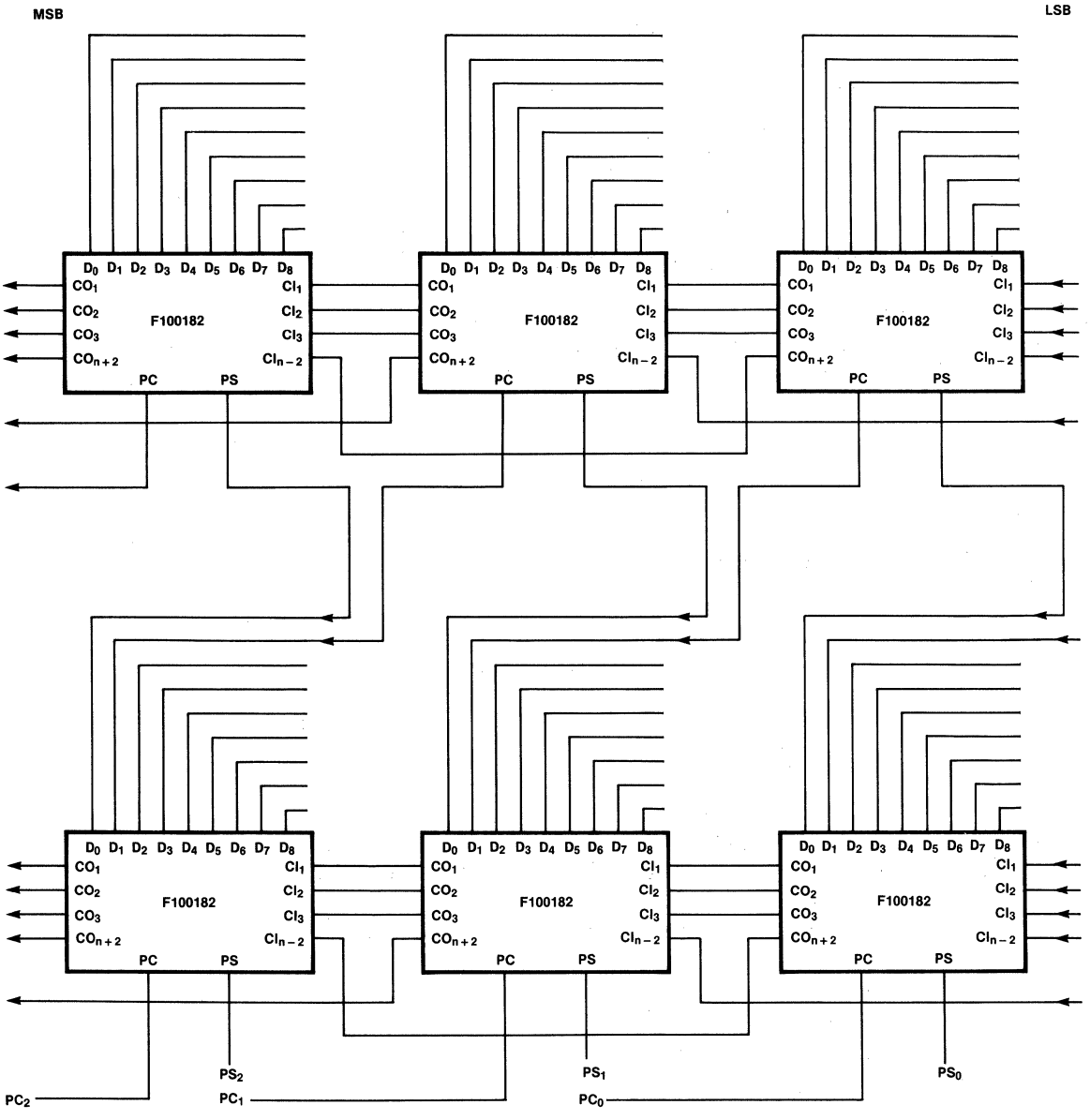


Application

Typical Horizontal interconnection of 9-Bit Wallace Tree Adders F100182



16-Bit Vertical Expansion of Wallace Tree Adders



F100183
2 x 8-Bit
Recode Multiplier

F100K ECL Product

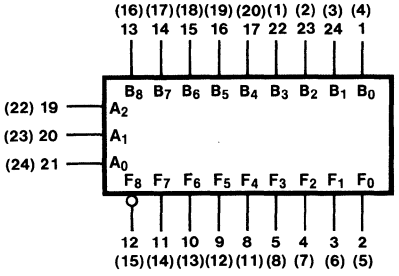
Description

The F100183 is a 2 x 8-bit recode multiplier designed to perform high-speed hardware multiplication. In conjunction with the F100182 Wallace Tree Adder, the F100179 Carry Lookahead, and the F100180 High-speed Adder, the F100183 performs parallel multiplication of two signed numbers in twos complement form to produce a signed twos complement product.

Pin Names

A_0–A_2	Multiplier (Recode) Inputs
B_0–B_8	Multiplicand Inputs
F_0–F_7	Partial Product Outputs
$\overline{F}_8$	Sign Extension Output

Logic Symbol



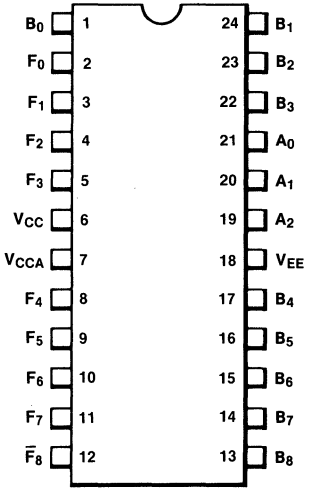
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

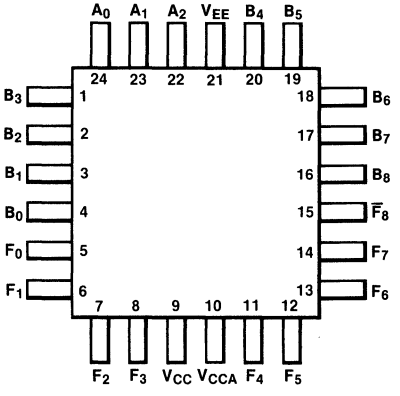
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4Q	FC

Connection Diagrams

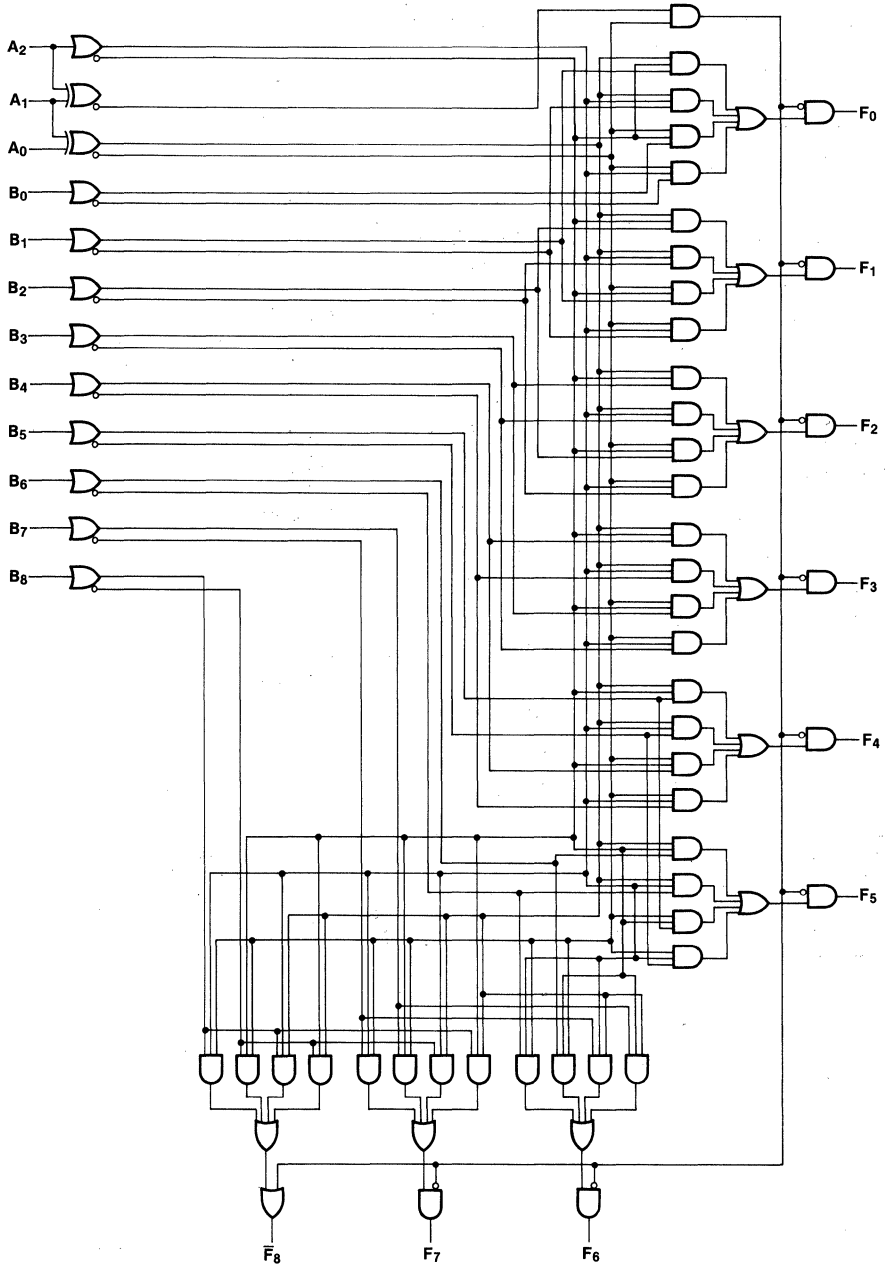
24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Logic Diagram



Truth Table

Inputs			Recode Mode	Outputs								
A_2	A_1	A_0		$\overline{F_8}$	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0
L	L	L	0	H	L	L	L	L	L	L	L	L
L	L	H	+1	$\overline{B_8}$	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
L	H	L	+1	$\overline{B_8}$	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
L	H	H	+2	$\overline{B_8}$	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
H	L	L	−2	B_8	$\overline{B_7}$	$\overline{B_6}$	$\overline{B_5}$	$\overline{B_4}$	$\overline{B_3}$	$\overline{B_2}$	$\overline{B_1}$	$\overline{B_0}$
H	L	H	−1	B_8	$\overline{B_8}$	$\overline{B_7}$	$\overline{B_6}$	$\overline{B_5}$	$\overline{B_4}$	$\overline{B_3}$	$\overline{B_2}$	$\overline{B_1}$
H	H	L	−1	B_8	$\overline{B_8}$	$\overline{B_7}$	$\overline{B_6}$	$\overline{B_5}$	$\overline{B_4}$	$\overline{B_3}$	$\overline{B_2}$	$\overline{B_1}$
H	H	H	0	H	L	L	L	L	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current B_0-B_8 A_0 A_1 A_2			 215 215 285 310	μA	V_{IN}=$V_{IH(max)}$
I_{EE}	Power Supply Current	−250	−170	−115	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

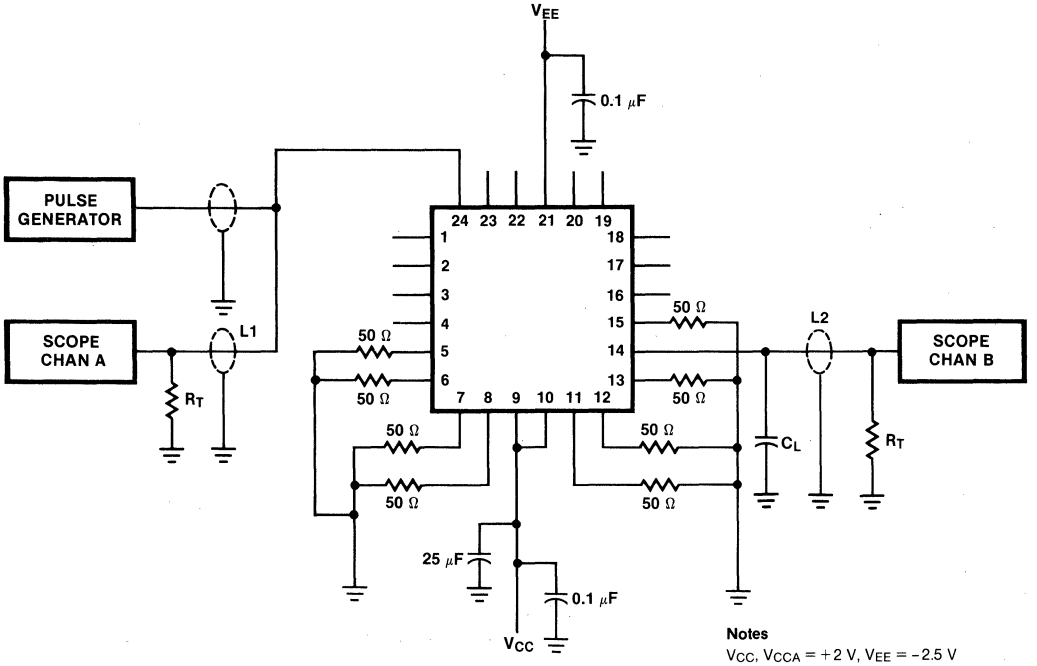
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay A_0-A_2 to F_0-F_7	1.10	3.90	1.10	3.80	1.10	4.20	ns	*Figure 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay A_0-A_2 to $\overline{F_8}$	0.90	3.20	1.00	3.10	1.00	3.60	ns	
t_{PLH} t_{PHL}	Propagation Delay B_0-B_8 to F_0-F_7	0.80	2.20	0.90	2.15	0.90	2.50	ns	*Figure 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay B_8 to $\overline{F_8}$	0.80	2.00	0.90	2.00	0.90	2.50	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.50	0.45	2.40	0.45	2.60	ns	*Figures 1* and *2*

*See Family Characteristics for other dc specifications.

Flatpak AC Characteristics: V_{EE} = -4.2 V to -4.8 V, V_{CC} = V_{CCA} = GND

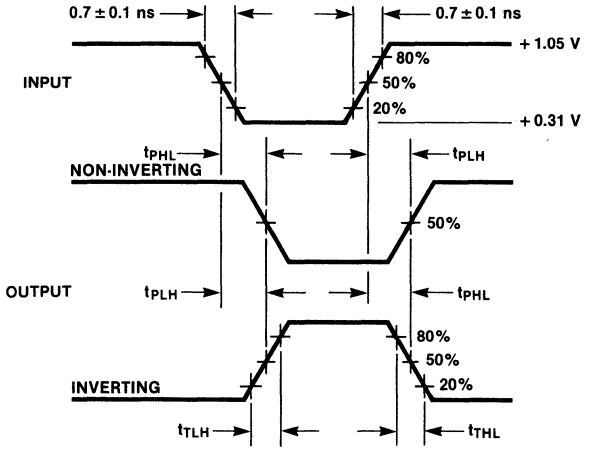
Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_0-A_2 to F_0-F_7	1.10	3.70	1.10	3.60	1.10	4.00	ns	*Figure 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay A_0-A_2 to $\overline{F_8}$	0.90	3.00	1.00	2.90	1.00	3.40	ns	
t_{PLH} t_{PHL}	Propagation Delay B_0-B_8 to F_0-F_7	0.80	2.00	0.90	1.95	0.90	2.30	ns	*Figure 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay B_8 to $\overline{F_8}$	0.80	1.80	0.90	1.80	0.90	2.30	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.40	0.45	2.30	0.45	2.50	ns	*Figures 1* and *2*

Fig. 1 AC Test Circuit



Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Fig. 2 Propagation Delay and Transition Times



Application

F100183 is a 2 x 8-bit recode multiplier that performs parallel multiplication using twos complement arithmetic. In multiplying, the multiplier is partitioned into recode groups, then each recode group operates on the multiplicand to provide a partial product at the same time. The F100183, 2 x 8-bit recode multiplier provides partial products in 3.6 ns.

The F100182, 9-Bit Wallace Tree Adder combines the partial products to obtain the partial sum and partial carries in an additional 10.7 ns. Then the Carry Look-ahead generator and 6-bit adder combine the results of a 16 x 16-bit multiply for a total of 24.3 ns. The propagation delays and package count for implementing various size multipliers are listed in *Tables 1* and *2*.

Multiplication of twos complement binary numbers is accomplished by first obtaining all the partial products. Then the weighted partial products are added together to yield the final result. In the Wallace Tree method of multiplication the sign bit is treated the same as the rest of the bits to obtain a signed result.

Table 1 Propagation Delay Summation*

Array Size	Recode Multiplier 100183	Wallace Tree Adder 100182	High-speed Adder 100180	Carry Lookahead 100179		Total (Max) Delay
16 x 16	3.6	10.7	7.3	2.7	=	24.3 ns
17 x 17	↕	21.4	↕	↕	=	35.0 ns
24 x 24		↕		2.7	=	35.0 ns
25 x 25	↕	↕	↕	5.4	=	37.7 ns
48 x 48		↕		5.4	=	37.7 ns
49 x 49	↕	↕	↕	8.1	=	40.4 ns
72 x 72		21.4		8.1	=	40.4 ns
73 x 73	3.6	32.1	7.3	10.8	=	53.8 ns

Table 2 Package Count

	100102 100117	100183	100182	100180	100179		Total
16 x 16	6	16	32	6	2	=	62
18 x 18	7	27	38	6	2	=	70
24 x 24	9	36	60	8	2	=	115
32 x 32	11	64	96	11	4	=	186
36 x 36	13	80	116	12	4	=	225
64 x 64	24	256	328	22	6	=	634

*Worst case, Flatpak

For a quick review of the twos complement number format see *Table 3*. Note that subtraction is accomplished by adding the negative number. An example of changing from a positive number to a negative number is shown.

1011	negative number-5
0100	bits inverted
+ 0001	add one
0101	Results 5

Table 3 Twos Complement Format

Sign Bit	Magnitude 2^2	2^1	2^0	Decimal Number
0	1	1	1	+7
0	1	1	0	+6
0	1	0	1	+5
0	1	0	0	+4
0	0	1	1	+3
0	0	1	0	+2
0	0	0	1	+1
0	0	0	0	0
1	1	1	1	−1
1	1	1	0	−2
1	1	0	1	−3
1	1	0	0	−4
1	0	1	1	−5
1	0	1	0	−6
1	0	0	1	−7
1	0	0	0	−8

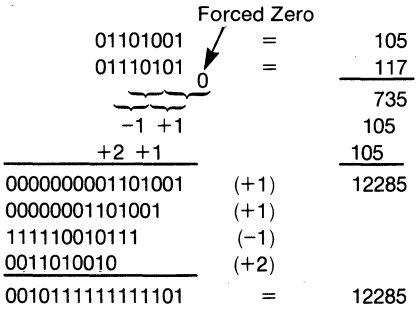
Multiplication Algorithm

In the multiplication algorithm used, the multiplier ($Y_n...Y_0$) is partitioned into recode groups and each recode group operates on the multiplicand ($X_n...X_0$) as in *Figure 4*. The F100183, 2 x 8-bit recode multiplier partitions the multiplier ($X_n...X_0$) into groups of eight and the multiplicand ($Y_n...Y_0$) into groups of two. Each recode group is two bits wide but requires three bits to determine the partial products. *Table 4* lists the significance of the various recode groups. The partial product is ±0, ± multiplicand, or ± two times the multiplicand. A forced zero is required to establish the least significant bit of the first recode group. By connecting recode multipliers in parallel the partial products are available at the same time. The weighted partial products ($A_n...A_0$, $B_n...B_0$)... are added together using F100182, 9-bit Wallace Tree Adders. The results of the partial sum and partial carry are combined together using Carry Look-ahead generators and 6-bit adders. An example of using recode multiplication is shown in *Figure 3:* multiplier (117_{10}) 01110101 times multiplicand (105_{10}) 01101001. The first recode group 010 requires adding the multiplicand; the second recode group 010 also requires adding the multiplicand; the third group 110 requires subtracting the multiplicand (the same as inverting each digit and adding 1); the fourth group 011 requires adding twice the multiplicand. Combining the results of four groups, 12285_{10}, we have the correct answer.

Table 4 Recode Product

Recode Group Y_{i+1}	Y_i	Y_{i-1}	Recode Value	Partial Product
0	0	0	+0	Add zero
0	0	1	+1	Add multiplicand
0	1	0	+1	Add multiplicand
0	1	1	+2	Add twice the multiplicand
1	0	0	−2	Subtract twice the multiplicand
1	0	1	−1	Subtract the multiplicand
1	1	0	−1	Subtract the multiplicand
1	1	1	−0	Subtract zero

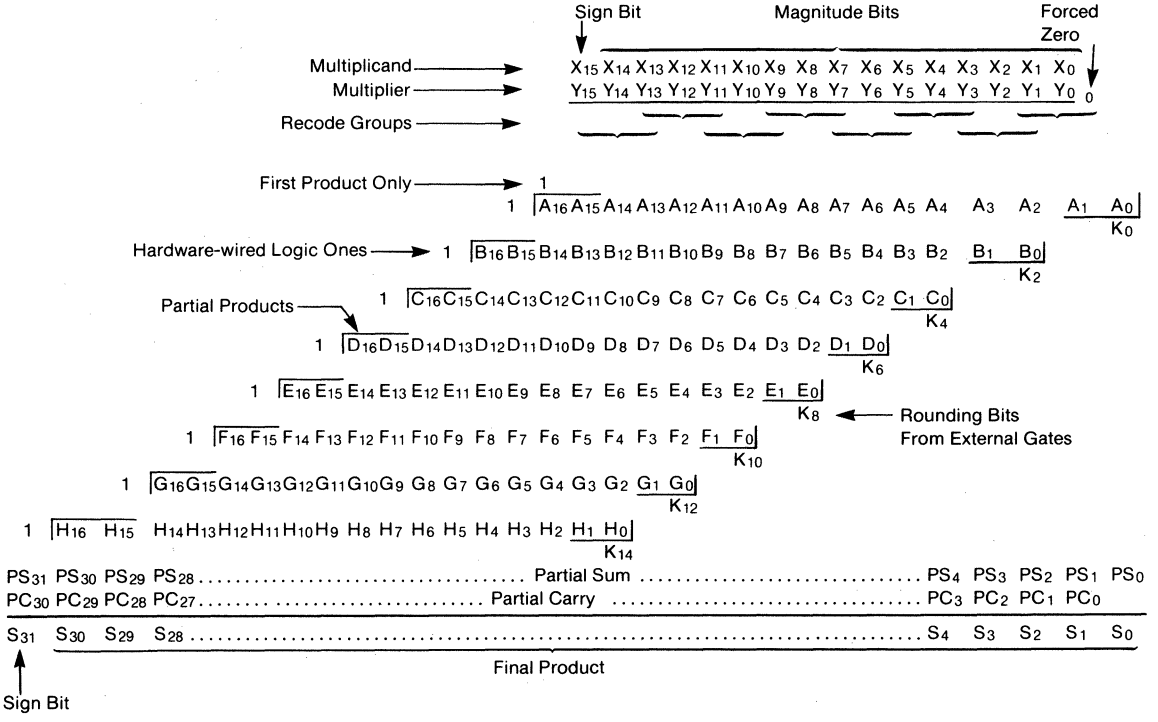
Fig. 3 Recode Multiplication Example



Hardware Implementation

For the hardware implementation of the F100183 recode multiplier the sign bit is connected to the B_8 input, and B_7 through B_0 are the magnitude bits. To extend the word length greater than eight bits, the B_0 and B_8 inputs of adjacent devices are connected together (see *Figure 7*). The device outputs F_0 through F_7 are used as the partial products; these correspond to A_0 through A_7, or A_8 through A_{15}, or B_0 through B_7 etc. To reduce the hardware, the $\overline{F}_8$ bit (A_{16} in *Figure 7*) is used as the sign bit of the partial product. The sign bits are extended by using hardware wired logic "1s." The ones are located in front of each partial product with an extra "1" at the sign bit of the first partial product as in *Figure 4.* The logic "1s" are wired as inputs into the Wallace Tree Adders as shown in *Figure 6.* If the recode group requires the multiplicand to be added, then the F100183 outputs

Fig. 4 16 x 16 Multiply



the correct partial products to be added. But when the recode group requires that the multiplicand be subtracted then the F100183 outputs the ones complement. External gates are required to generate a "1" to be added to the ones complement to complete the twos complement for the partial product *(Figure 7)*. These external gates generate the rounding bits, $K_0 \ldots K_n$, which are input to the Wallace Tree Adder. *Figures 4, 6* and *7* show the location. An example of multiplication which has the rounding bits and the hardware wired logic "1s" is shown in *Figure 5*.

The weighted partial products are added together using F100182, 9-bit Wallace Tree Adders as shown in *Figure 6*. The output is a partial sum and partial carry which can be reduced to the final product using Carry Lookahead and 6-bit adders. See *Figure 8*.

Fig. 5 Example of Multiplication Using Rounding Bits

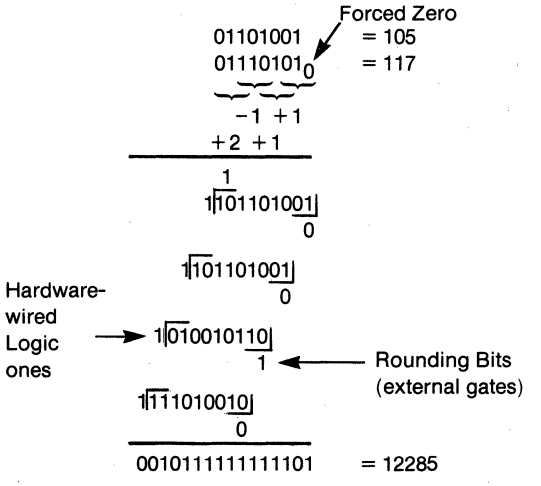


Fig. 6 F100182 Hook-up for 16 x 16 Multiplier

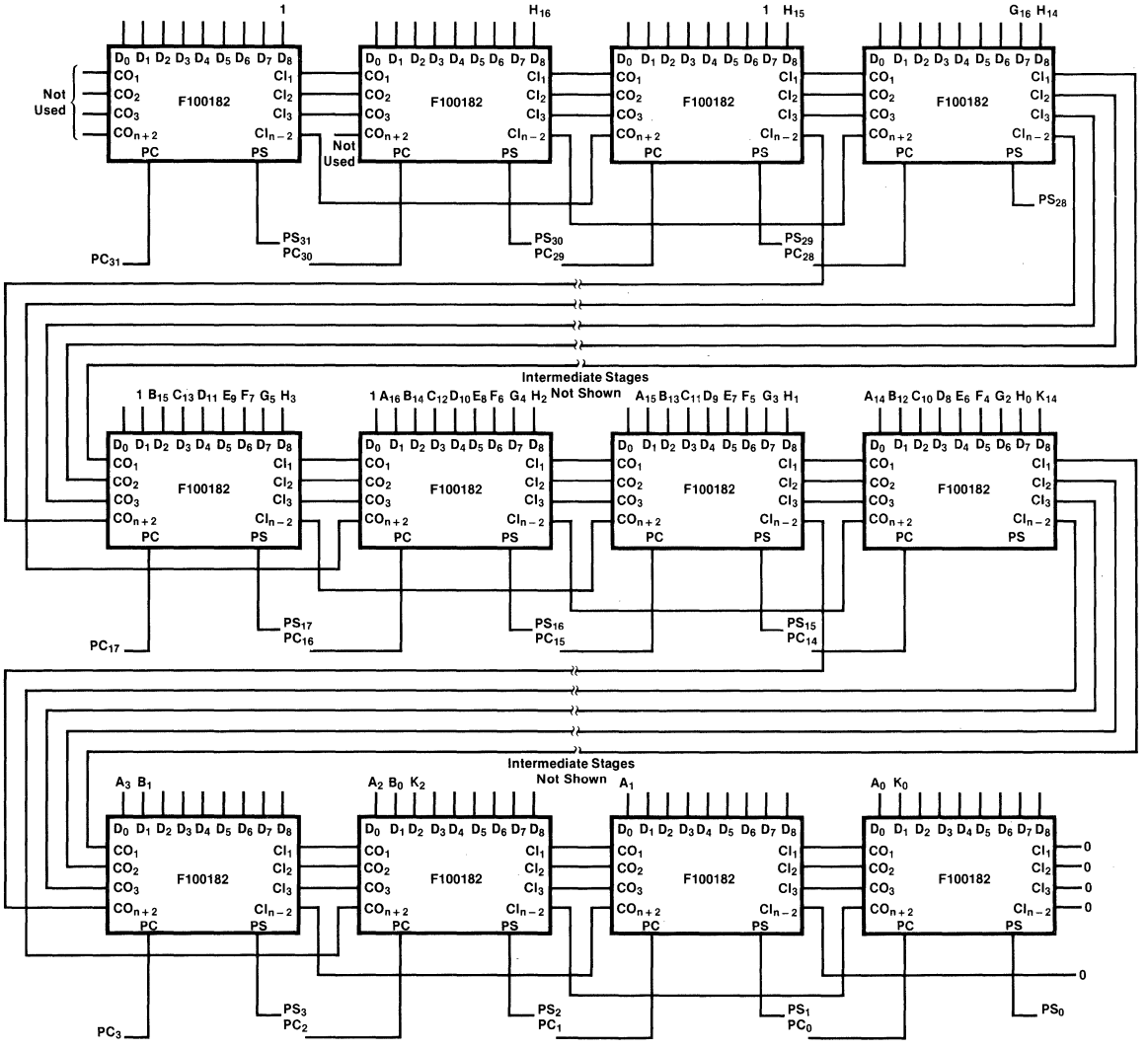


Fig. 7 F100183 Hook-up for 16 x 16 Multiplier

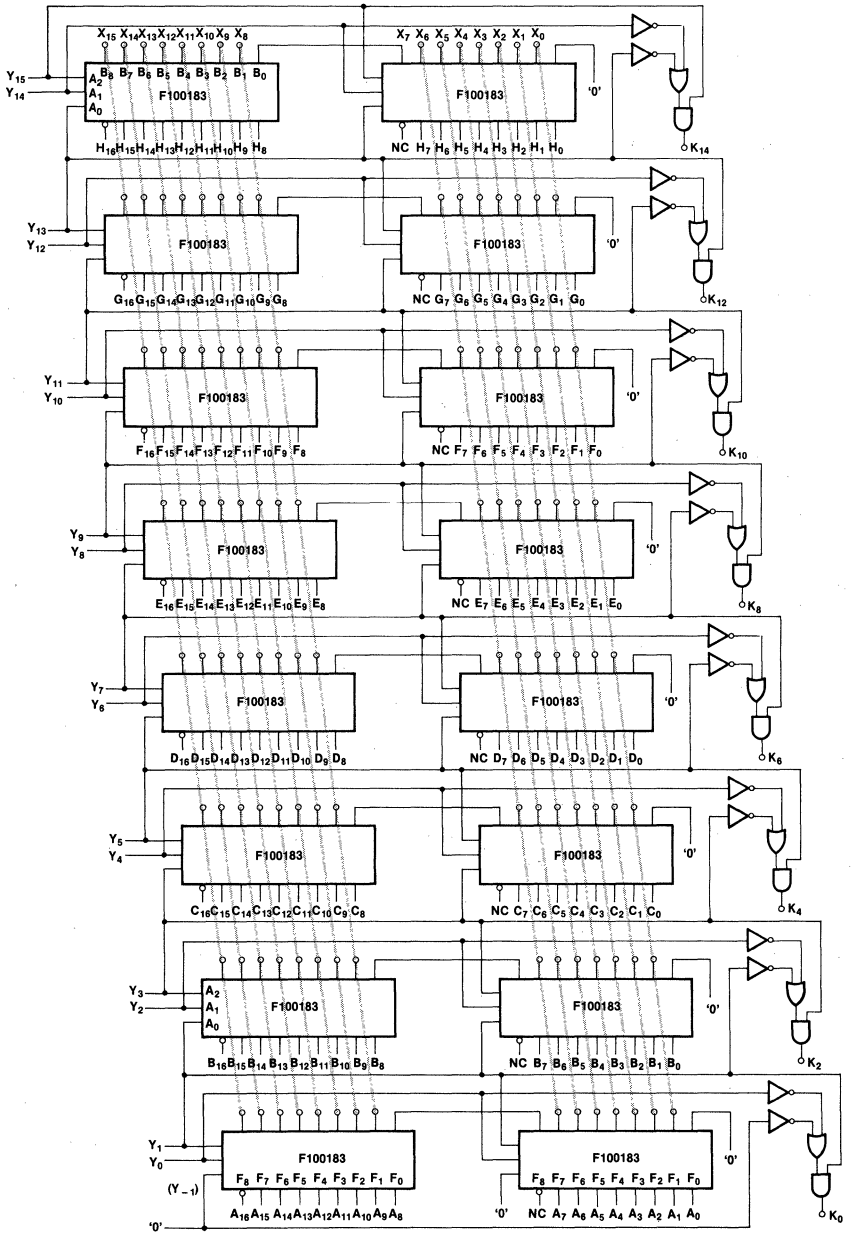
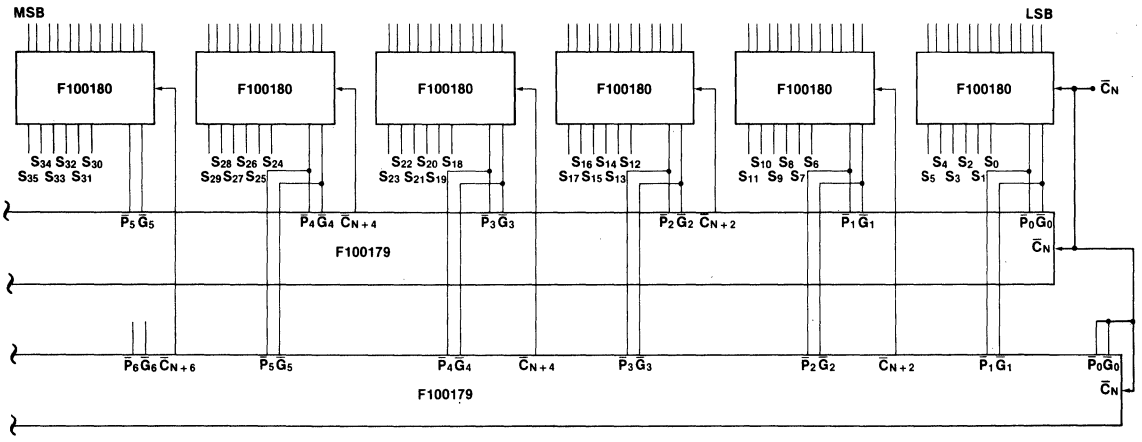


Fig. 8 Final Summation for 16 x 16 Multiplier



F100194
Quint Duplex Bus Driver (Transceiver)

F100K ECL Product

Description

The F100194 is a quint line driver/receiver capable of transmitting and receiving full duplex digital signals on a high-speed bus line. Because of the current source line driver, two independent messages may be transmitted on one line at the same time.

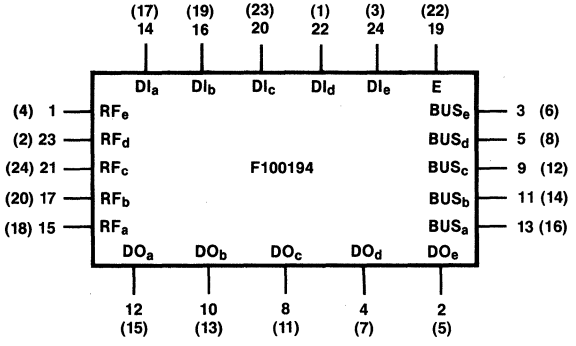
The F100194 is designed to work with a wide line impedance range by connecting a resistor equal to one half the line impedance between RF_n inputs and V_{EE}. Each driver is capable of driving a double terminated 50 Ω impedance line, where each R_{BUS} is 25 Ω.

The Enable (E) can be used to take all the devices off the line by putting all the outputs into a high-impedance state.

Pin Names

E	Enable Input
DI_a-DI_e	Data Inputs
RF_a-RF_e	Reference Resistor Inputs
BUS_a-BUS_e	Bus Inputs/Outputs
DO_a-DO_e	Data Outputs

Logic Symbol



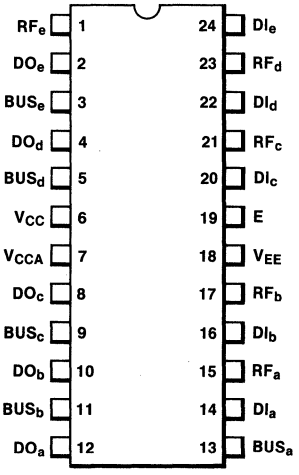
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

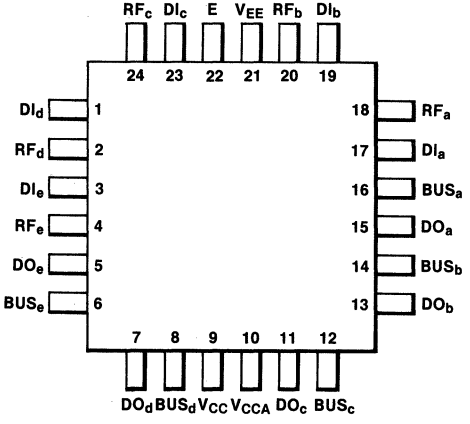
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4Q	FC

Connection Diagrams

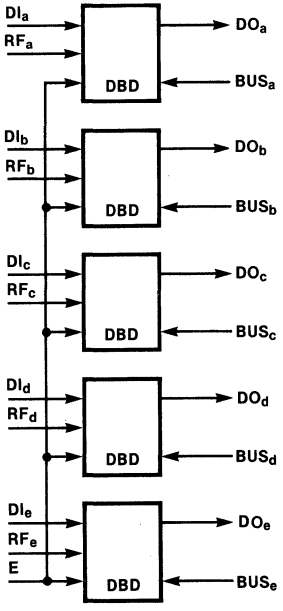
24-Pin DIP (Top View)

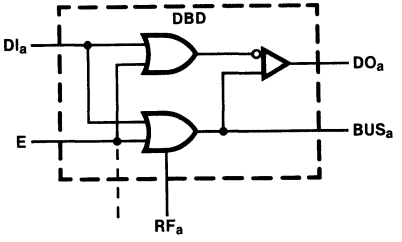


24-Pin Flatpak (Top View)



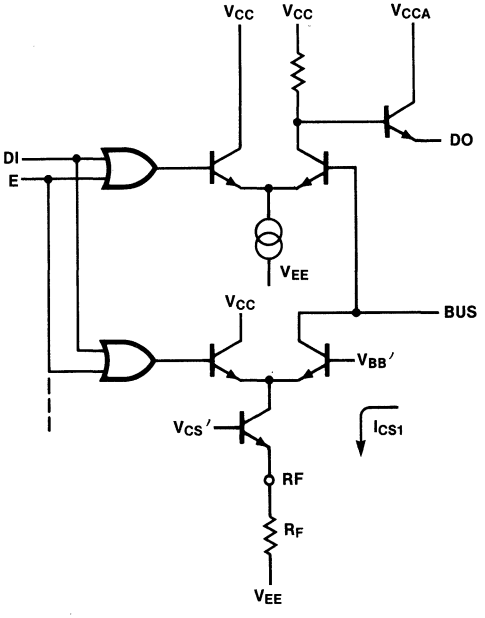
Logic Diagram





DBD = Duplex Bus Driver
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Output Equivalent Circuit



DC Logic Level Description

The bus terminal (*i.e.*, BUS_a) can be at any one of three possible levels, V_{OHBH}, V_{OLBL} or a third level, depending upon the combination of inputs applied. The third level is between V_{OLBH} and V_{OHBL}, typically −800 mV. The inputs DI_x and E cause the bus terminal to switch between two levels, V_{OHBH} and V_{OLBH}, when the external current source I_{CS2} is OFF and V_{OHBL} and V_{OLBL} when the external current source is ON. The bus output threshold voltage levels caused by applying input threshold voltages $V_{IL(max)}$ and $V_{IH(min)}$ at E and DI_x are also translated depending upon the state of I_{CS2}. These threshold levels are V_{OHBHC} and V_{OLBHC} when I_{CS2} is OFF and V_{OHBLC} and V_{OLBLC} when I_{CS2} is ON. These relative voltage levels are shown in *Figure 1.*

The BUS_x output is an open collector in current sinking configuration. The current I_{CS1} provided to the R_{BUS} resistor depends upon the reference resistor R_F. The following applies:

$$I_{CS1} = \frac{800\ mV}{R_F};$$

therefore the voltage swing at the BUS_x output is

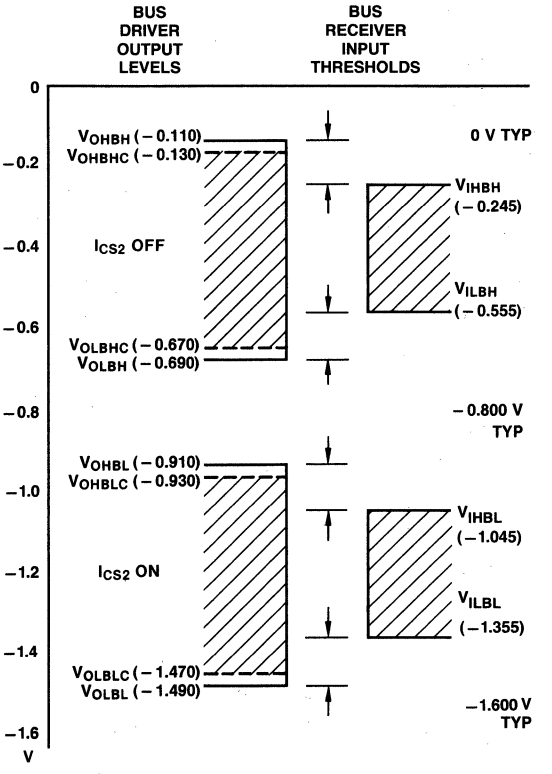
$$\frac{R_{BUS}}{R_F} \times 800\ mV.$$

Truth Table

Inputs				Outputs
E_x	DI_x	I_{CS2}	BUS_x	DO_x
L	L	ON	V_{OLBL}	H
L	L	OFF	V_{OLBH}	L
L	H	ON	V_{OHBL}	H
L	H	OFF	V_{OHBH}	L
H	X	ON	V_{OHBL}	H
H	X	OFF	V_{OHBH}	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Fig. 1 Bus Driver and Receiver Voltage Levels



DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
V_{OHBH}	Output HIGH Voltage Bus HIGH	−110		0	mV	I_{CS2} = OFF = 0 mA	$V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$
V_{OLBH}	Output LOW Voltage Bus HIGH	−910		−690	mV		
V_{OHBL}	Output HIGH Voltage Bus LOW	−910		−690	mV	I_{CS2} = ON = 32.0 mA	
V_{OLBL}	Output LOW Voltage Bus LOW	−1710		−1490	mv		
V_{OHBHC}	Output HIGH Corner Voltage Bus HIGH	−130			mV	I_{CS2} = OFF = 0 mA	$V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$
V_{OLBHC}	Output LOW Corner Voltage Bus HIGH			−670	mV		
V_{OHBLC}	Output HIGH Corner Voltage Bus LOW	−930			mV	I_{CS2} = ON = 32.0 mA	
V_{OLBLC}	Output LOW Corner Voltage Bus LOW			−1470	mv		
V_{IHBH}	Input HIGH Voltage Bus HIGH	−245		0	mV	Guaranteed HIGH Signal for BUS_x Inputs	I_{CS1} = OFF E or $DI_x = V_{IH}$
V_{ILBH}	Input LOW Voltage Bus HIGH	−800		−555	mV	Guaranteed LOW Signal for BUS_x Inputs	
V_{IHBL}	Input HIGH Voltage Bus LOW	−1045		−800	mV	Guaranteed HIGH Signal for BUS_x Inputs	I_{CS2} = ON E, $DI_x = V_{IL}$
V_{ILBL}	Input LOW Voltage Bus LOW	−1600		−1355	mV	Guaranteed LOW Signal for BUS_x Inputs	

DC Characteristics (Cont'd.): V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
I_{IH}	Input HIGH Current Data Enable			220 440	μA	$V_{IN} = V_{IH(max)}$	
I_{IL}	Input LOW Current Data, Enable	0.5			μA	$V_{IN} = V_{IL(min)}$	
I_{IHBH}	Input HIGH Current Bus HIGH			60	μA	$V_{IN} = V_{IHBH(max)}$ E or $DI_x = V_{IH}$	R_F = 25 Ω
I_{ILBH}	Input LOW Current Bus HIGH	0.5			μA	$V_{IN} = V_{ILBH(min)}$ E, $DI_x = V_{IL}$	
I_{IHBL}	Input HIGH Current Bus LOW (I_{CS1})		32	27.6	mA	$V_{IN} = V_{IHBH(max)}$ E, $DI_x = V_{IL}$	
I_{ILBL}	Input LOW Current Bus LOW (I_{CS1})	36.4	32		mA	$V_{IN} = V_{ILBL(min)}$ E, $DI_x = V_{IL}$	
I_{EE}	Power Supply Current	−160	−110	−72	mA	Inputs Open, R_F = Open	

*See Family Characteristics for other dc specifications.

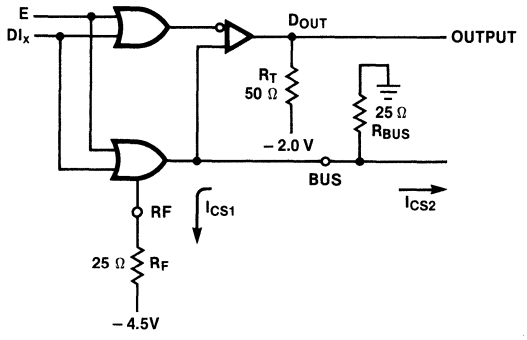
Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Bus	0.45	1.50	0.45	1.40	0.45	1.50	ns	*Figures 3* and *5*
t_{PLH} t_{PHL}	Propagation Delay Enable to Bus	0.70	1.90	0.70	1.80	0.70	1.90	ns	
t_{PLH} t_{PHL}	Propagation Delay Bus to Output	0.45	1.50	0.45	1.40	0.45	1.40	ns	*Figures 4* and *6*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20% BUS_a-BUS_e	0.30	1.00	0.30	1.00	0.30	1.00	ns	*Figures 3* and *5*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20% DO_a-DO_e	0.45	1.60	0.45	1.50	0.45	1.60	ns	*Figures 4* and *6*

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Bus	0.45	1.30	0.45	1.20	0.45	1.30	ns	*Figures 3* and *5*
t_{PLH} t_{PHL}	Propagation Delay Enable to Bus	0.70	1.70	0.70	1.60	0.70	1.70	ns	
t_{PLH} t_{PHL}	Propagation Delay Bus to Output	0.45	1.30	0.45	1.20	0.45	1.20	ns	*Figures 4* and *6*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20% BUS_a-BUS_e	0.30	0.90	0.30	0.90	0.30	0.90	ns	*Figures 3* and *5*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20% DO_a-DO_e	0.45	1.50	0.45	1.40	0.45	1.50	ns	*Figures 4* and *6*

Fig. 2 DC Test Circuit

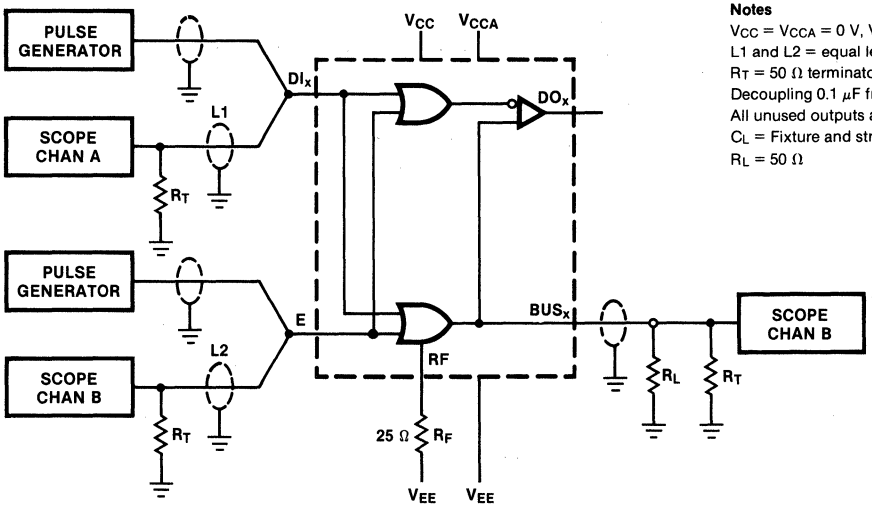


Notes

I_{CS2} is used to represent second transceiver on bus.

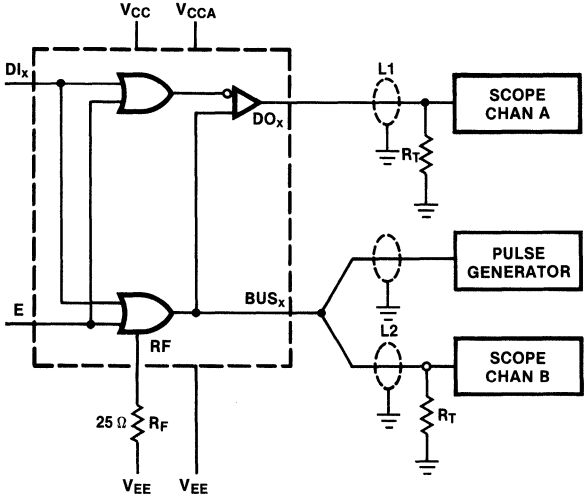
Resistors ± 1%

Fig. 3 AC Test Circuit (DI_X, E to BUS_X)



Notes
$V_{CC} = V_{CCA} = 0$ V, $V_{EE} = -4.5$ V
L1 and L2 = equal length 50 Ω impedance lines
$R_T = 50\ \Omega$ terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
$R_L = 50\ \Omega$

Fig. 4 AC Test Circuit (BUS_X to DO_X)



Notes
V_{CC}, $V_{CCA} = +2$ V, $V_{EE} = -2.5$ V
L1 and L2 = equal length 50 Ω impedance lines
$R_T = 50\ \Omega$ terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

Fig. 5 DI_x, E to BUS_x Timing

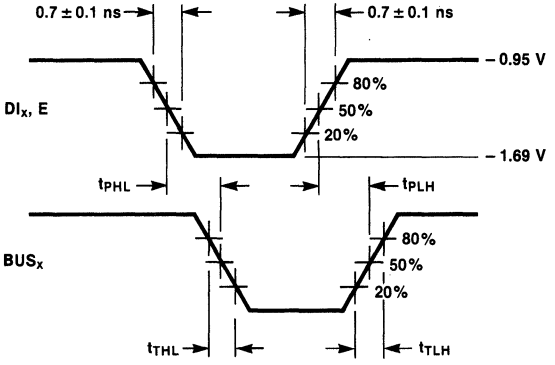
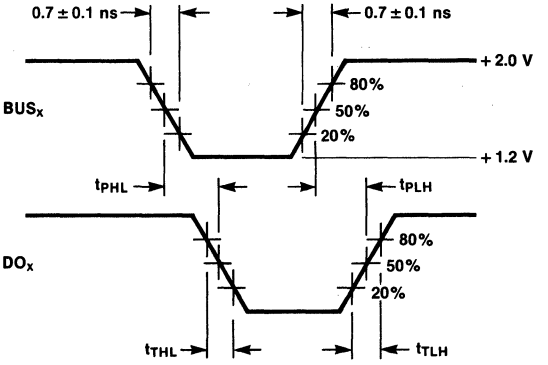


Fig. 6 BUS_x to DO_x Timing



3

Application

Two Transceiver System Operation

When a signal is transmitted through DI_a, the bus follows and $DO_b = \overline{DI_a}$; however, DO_a does not respond to the signal. Likewise, a signal transmitted through DI_b causes the bus to follow the signal with no response at DO_b, and $DO_a = \overline{DI_b}$. Since the bus has three logic levels, transmission and reception of two simultaneous signals is possible.

The common Enable, when HIGH, disables transmission from the five transceivers in the package but does not interfere with reception from an external transceiver.

Transceiver Truth Table

Input						Bus Output	Output	
Transceiver 1			Transceiver 2				Transceiver 1	Transceiver 2
E_1	DI_1	I_{CS1}	E_2	DI_2	I_{CS2}	Bus	DO_1	DO_2
L	L	ON	L	L	ON	V_{OLBL}	H	H
L	L	ON	L	H	OFF	V_{OLBH}	L	H
L	H	OFF	L	L	ON	V_{OHBL}	H	L
L	H	OFF	L	H	OFF	V_{OHBH}	L	L
H	X	OFF	L	L	ON	V_{OHBL}	H	L
H	X	OFF	L	H	OFF	V_{OHBH}	L	L
L	L	ON	H	X	OFF	V_{OLBH}	L	H
L	H	OFF	H	X	OFF	V_{OHBH}	L	L
H	X	OFF	H	X	OFF	V_{OHBH}	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Fig. 7 50 Ω Configuration

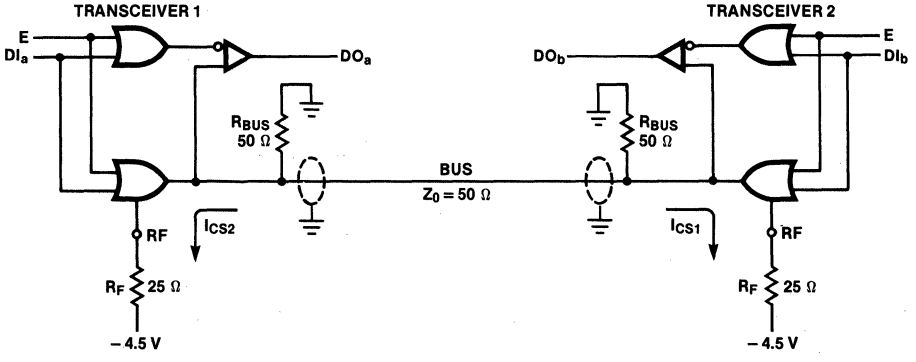
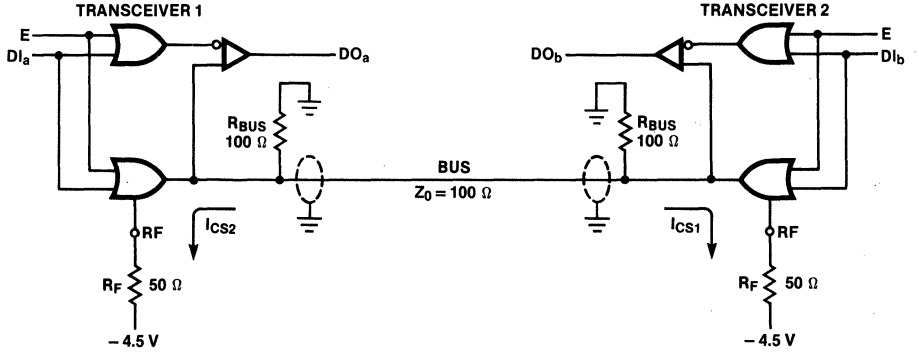


Fig. 8 100 Ω Configuration



F100402
16 x 4 Register File (RAM)

F100K ECL Product

Description

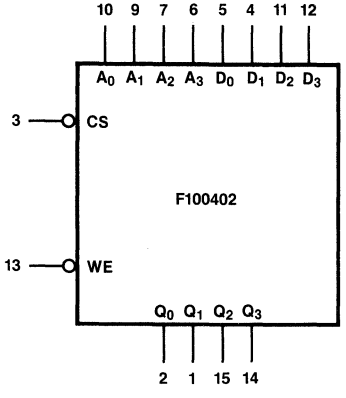
The F100402 is a high-speed 64-bit Random Access Memory (RAM) organized as a 16-word by 4-bit array. External logic requirements are minimized by internal address decoding, while memory expansion and data busing are facilitated by the output disabling features of the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs.

A HIGH signal on $\overline{CS}$ prevents read and write operations and forces the outputs to the LOW state. When $\overline{CS}$ is LOW, the $\overline{WE}$ input controls chip operations. A HIGH signal on $\overline{WE}$ disables the Data input (D_n) buffers and enables readout from the memory location determined by the Address (A_n) inputs. A LOW signal on $\overline{WE}$ forces the Q_n outputs LOW and allows data on the D_n inputs to be stored in the addressed location. Data exists in the same logical sense as presented at the data inputs, *i.e.*, the memory is non-inverting.

Pin Names

$\overline{CS}$	Chip Select Input
A_0-A_3	Address Inputs
D_0-D_3	Data Inputs
$\overline{WE}$	Write Enable Input
Q_0-Q_3	Data Outputs

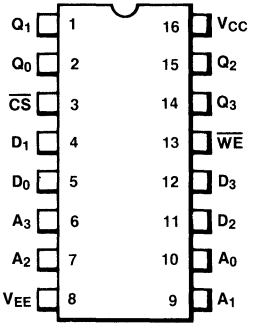
Logic Symbol



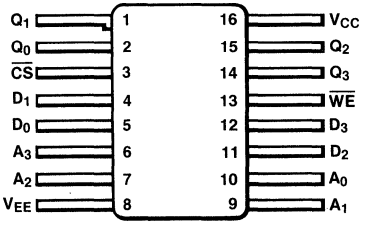
V_{CC} = Pin 16
V_{EE} = Pin 8

Connection Diagrams

16-Pin DIP (Top View)



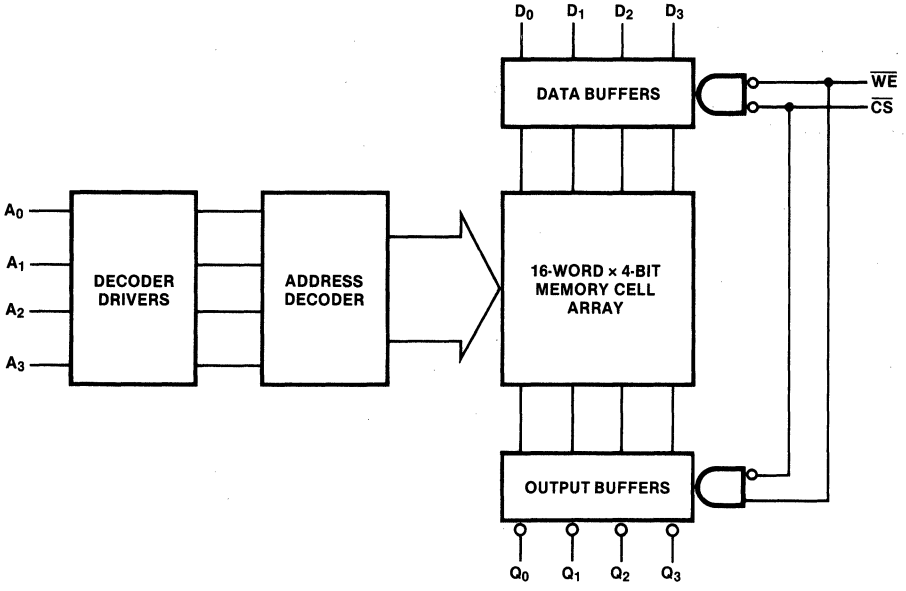
16-Pin Flatpak (Top View)



Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	4J	DC
Flatpak	3L	FC

Logic Diagram



DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = GND, T_C = 0°C to +85°C*

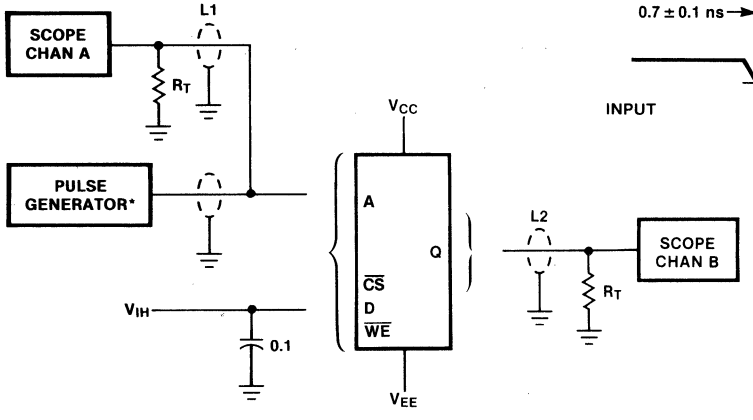
Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current All Inputs			300	μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	−170	−110	−70	mA	Inputs Open

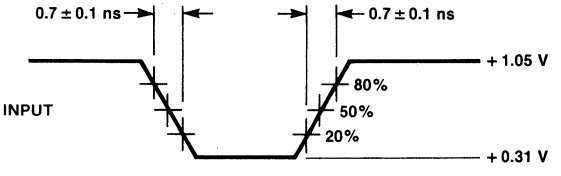
*See Family Characteristics for other dc specifications.

AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = GND, Applies to Flatpak and DIP Packages

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
	Access/Recovery Timing								
t_{ACS}	Chip Select Access		3.30		3.50		3.80	ns	
t_{RCS}	Chip Select Recovery		3.30		3.50		3.80	ns	*Figures 1* and *3*
t_{AA}	Address Access	3.00	5.00	3.00	5.30	3.50	6.00	ns	
	Write Timing, Setup								
t_{WSD}	Data	0.50		0.50		0.80		ns	
t_{WSCS}	Chip Select	1.50		1.50		1.50		ns	
t_{WSA}	Address	1.00		1.00		1.00		ns	*Figures 1* and *2*
	Write Timing, Hold								t_W = 6 ns
t_{WHD}	Data	0.50		0.50		0.50		ns	
t_{WHCS}	Chip Select	0.50		0.50		0.50		ns	
t_{WHA}	Address	2.50		2.50		2.50		ns	
t_{WR}	Write Recovery Time	4.00		4.00		4.50		ns	*Figures 1* and *3*
t_{WS}	Write Disable Time	3.00		3.00		3.50		ns	
t_W	Write Pulse Width, (LOW)	2.50		2.50		3.00		ns	*Figures 1* and *2*
t_{CS}	Chip Select Pulse Width, (LOW)	2.50		2.50		3.00		ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	1.70	0.50	1.70	0.50	1.70	ns	*Figures 1* and *3*

Fig. 1 AC Test Circuit and Waveforms



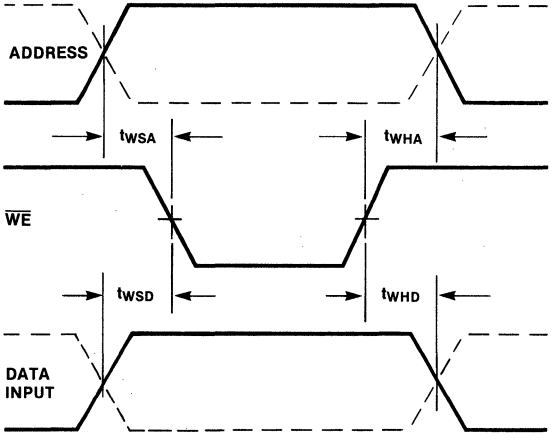


Notes
V_{CC} = +2 V, V_{EE} = −2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
*One or more generators, as required

Fig. 2 Write Modes

Write Enable Strobe

ADDRESS AND DATA INPUT SET-UP AND HOLD TIMES
(CS = LOW)



CHIP SELECT SET-UP AND HOLD TIMES

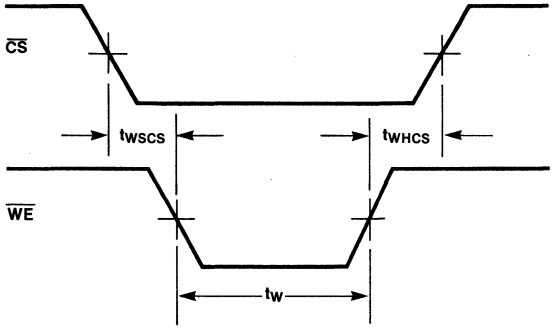
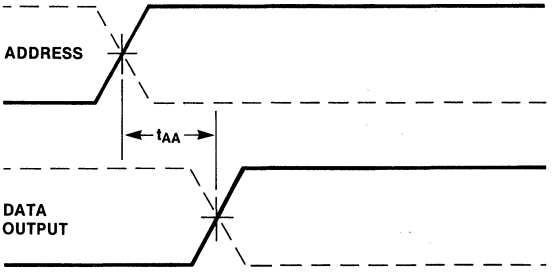


Fig. 3 Read Modes

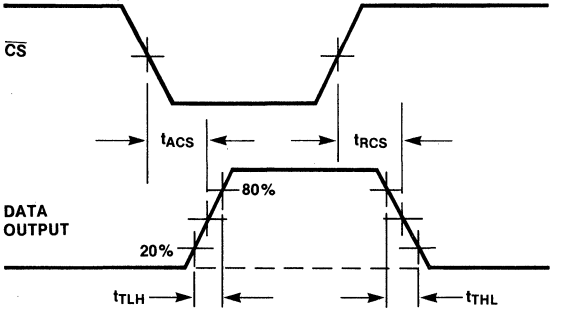
Address Input to Data Output ($\overline{WE}$ = HIGH, $\overline{CS}$ = LOW)

ADDRESS ACCESS TIME



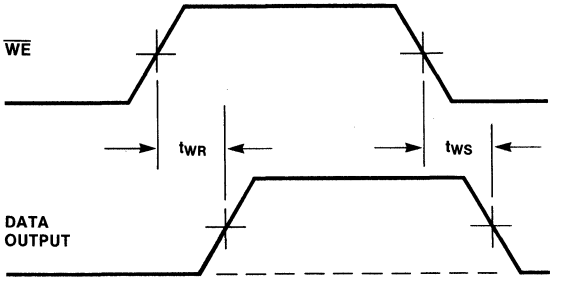
Chip Select Input to Data Output ($\overline{WE}$ = HIGH)

CHIP SELECT ACCESS AND RECOVERY TIMES



Write Enable Input to Data Output ($\overline{CS}$ = LOW)

WRITE RECOVERY, DISABLE TIMES



F100414
256 x 1-Bit Static Random Access Memory

F100K ECL Product

Description

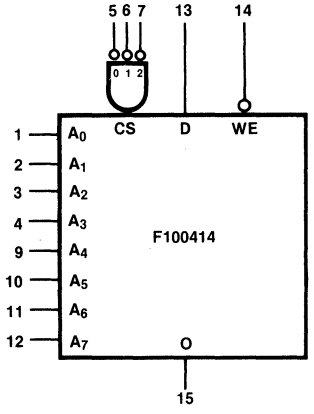
The F100414 is a 256-bit read/write Random Access Memory (RAM), organized 256 words by one bit. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as three active-LOW Chip Select lines.

- **Address Access Time–10 ns Max**
- **Chip Select Access Time–6.0 ns Max**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation–1.8 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}_0$–$\overline{CS}_2$	Chip Select Inputs (Active LOW)
A_0–A_7	Address Inputs
D	Data Input
O	Data Output

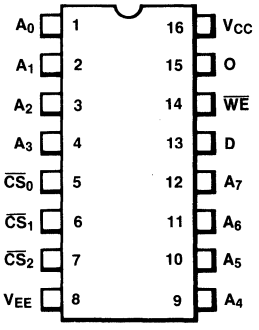
Logic Symbol



V_{CC} = Pin 16
V_{EE} = Pin 8

Connection Diagram

16-Pin DIP (Top View)

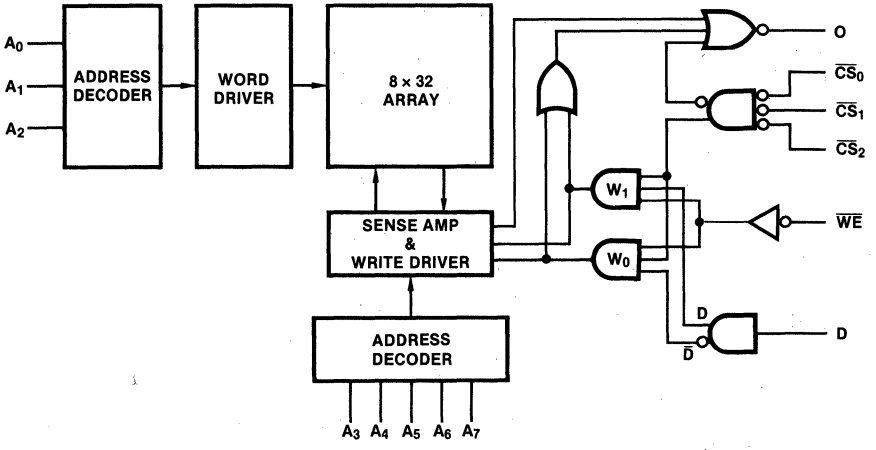


Note
The 16-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6D	DC
Plastic DIP	9B	PC
Flatpak	3L	FC

Logic Diagram



Functional Description

The F100414 is a fully decoded 256-bit read/write random access memory, organized 256 words by one bit. Bit selection is achieved by means of an 8-bit address, A_0 through A_7.

Three active-LOW Chip Select inputs are provided for increased logic flexibility. This permits memory array expansion up to 2048 words with the F100170 decoder. For larger memories, the fast chip select access time permits the decoding of Chip Select, $\overline{CS}$, from the address without affecting system performance.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the output (O).

The output of the F100414 is an unterminated emitter follower, which allows maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F100414 devices together to allow easy expansion. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output.

Truth Table

Inputs					Output	Mode
$\overline{CS_0}$	$\overline{CS_1}$	$\overline{CS_2}$	$\overline{WE}$	D	O	
X	X	H*	X	X	L	Not Selected
L	L	L	L	L	L	Write "0"
L	L	L	L	H	L	Write "1"
L	L	L	H	X	Data	Read

L = LOW Voltage Levels = −1.7 V (Nominal)
H = HIGH Voltage Levels = −0.9 V (Nominal)
X = Don't Care
Data = Previously stored data
*One or more Chip Selects HIGH

DC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = GND, T_C = 0°C to +85°C unless otherwise specified[1]

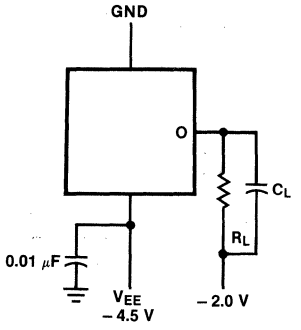
Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			220	μA	$V_{IN} = V_{IH(max)}$
I_{IL}	Input LOW Current, $\overline{CS}$ $\overline{WE}$, A_0-A_{11}, D	0.5 −50		170	μA	$V_{IN} = V_{IL(min)}$
I_{EE}	Power Supply Current	−140	−100		mA	Inputs and Outputs Open

AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = GND, Output Load = 50 Ω and 30 pF to −2.0 V, T_C = 0°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
	Read Timing						
t_{ACS}	Chip Select Access Time		4.0	6.0	ns		
t_{RCS}	Chip Select Recovery Time		4.0	6.0	ns	*Figures 3a, 3b*	
t_{AA}	Address Access Time[2]		7.0	10	ns		
	Write Timing						
t_W	Write Pulse Width to Guarantee Writing	7.0	5.0		ns	t_{WSA} = 1 ns	Measured at 50% of Input to Valid Output ($V_{IL(max)}$ for V_{OL} or $V_{IH(min)}$ for V_{OH})
t_{WSD}	Data Setup Time prior to Write	1.0	0		ns	*Figure 4*	
t_{WHD}	Data Hold Time after Write	2.0	0		ns		
t_{WSA}	Address Setup Time prior to Write	1.0	0		ns		
t_{WHA}	Address Hold Time after Write	2.0	0		ns		
t_{WSCS}	Chip Select Setup Time prior to Write	1.0	0		ns	t_W = 7 ns	
t_{WHCS}	Chip Select Hold Time after Write	2.0	0		ns	*Figure 4*	
t_{WS}	Write Disable Time		4.0	8.0	ns		
t_{WR}	Write Recovery Time		5.0	10	ns		
t_r	Output Rise Time		3.0		ns	Measured between 20% and 80% or 80% and 20%, *Figure 2*	
t_f	Output Fall Time		3.0		ns		
C_{IN}	Input Pin Capacitance		4.0	5.0	pF	Measured with a Pulse Technique	
C_{OUT}	Output Pin Capacitance		7.0	8.0	pF		

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Fig. 1 AC Test Circuit



Notes
All Timing Measurements Referenced to 50% of Input Levels
C_L = 30 pF including Fixture and Stray Capacitance
R_L = 50 Ω to – 2.0 V.

Fig. 2 Input Levels

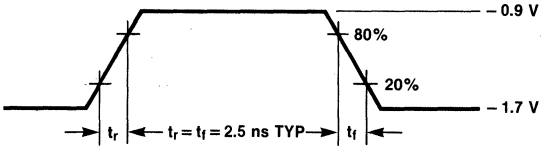
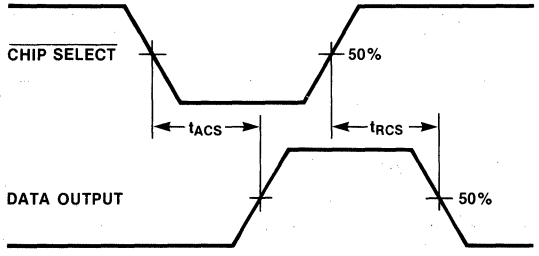


Fig. 3 Read Mode Timing

a Read Mode Propagation Delay from Chip Select



b Read Mode Propagation Delay from Address

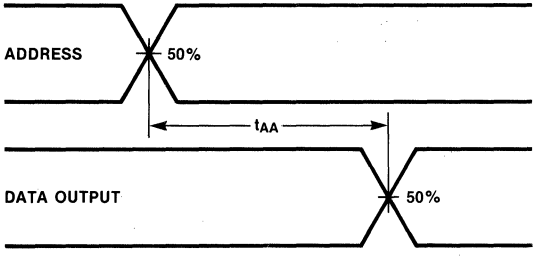
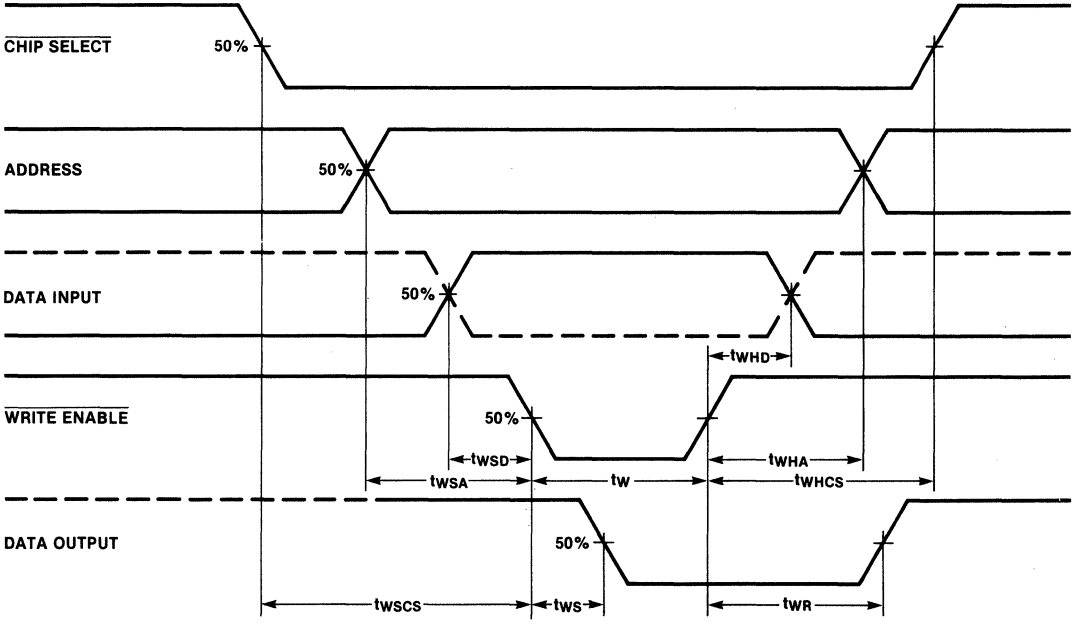


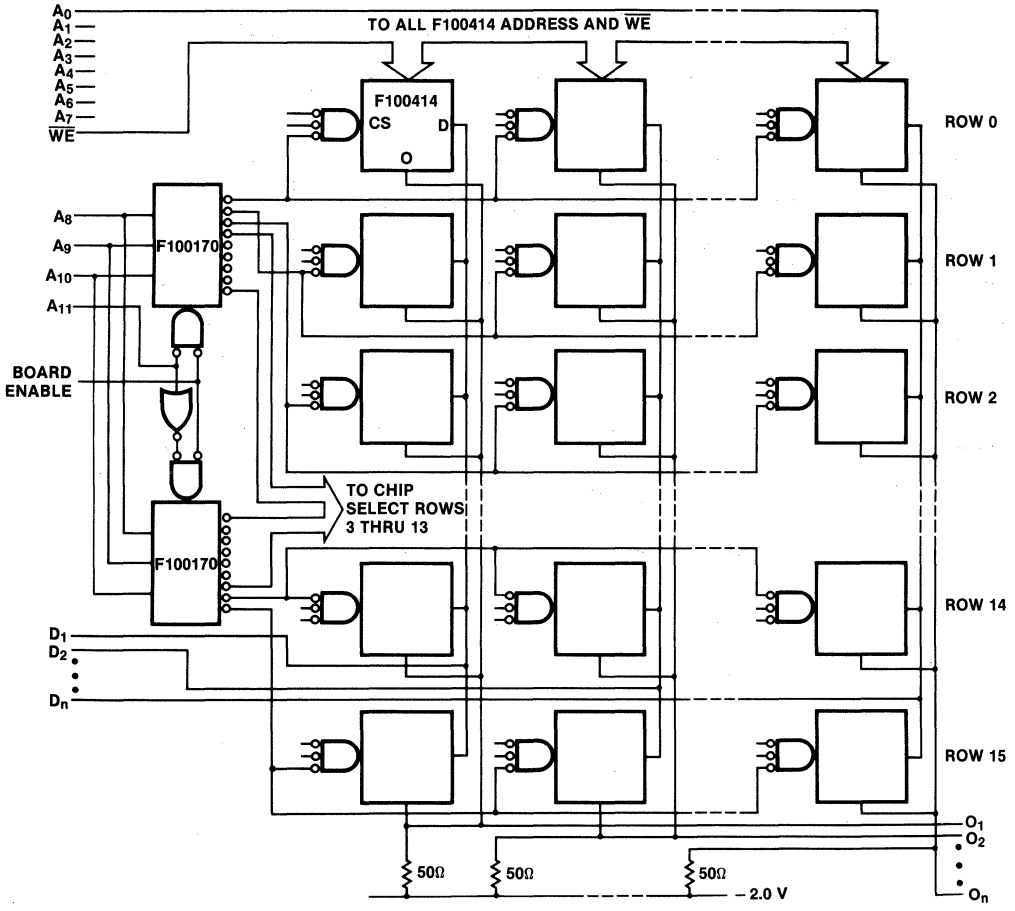
Fig. 4 Write Mode Timing



Note
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Typical Application

4096-Word x n-Bit System



F100415
1024 x 1-Bit Static Random Access Memory

F100K ECL Product

Description

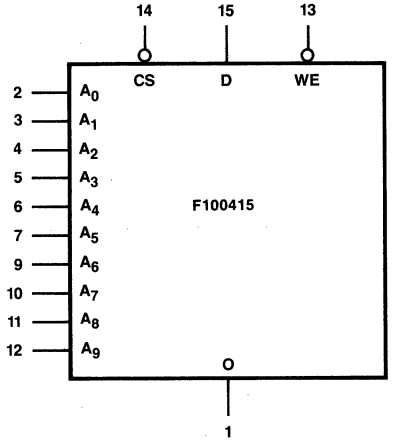
The F100415 is a 1024-bit read/write Random Access Memory (RAM), organized as 1024 words by one bit per word and designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as three active-LOW Chip Select line.

- **Address Access Time — 20 ns Max**
- **Chip Select Access Time — 8.0 ns Max**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation–0.5 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Inputs (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
A_0–A_9	Address Inputs
D	Data Input
O	Data Output

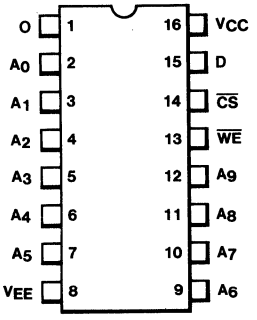
Logic Symbol



V_{CC} = Pin 16
V_{EE} = Pin 8

Connection Diagram

16-Pin DIP (Top View)

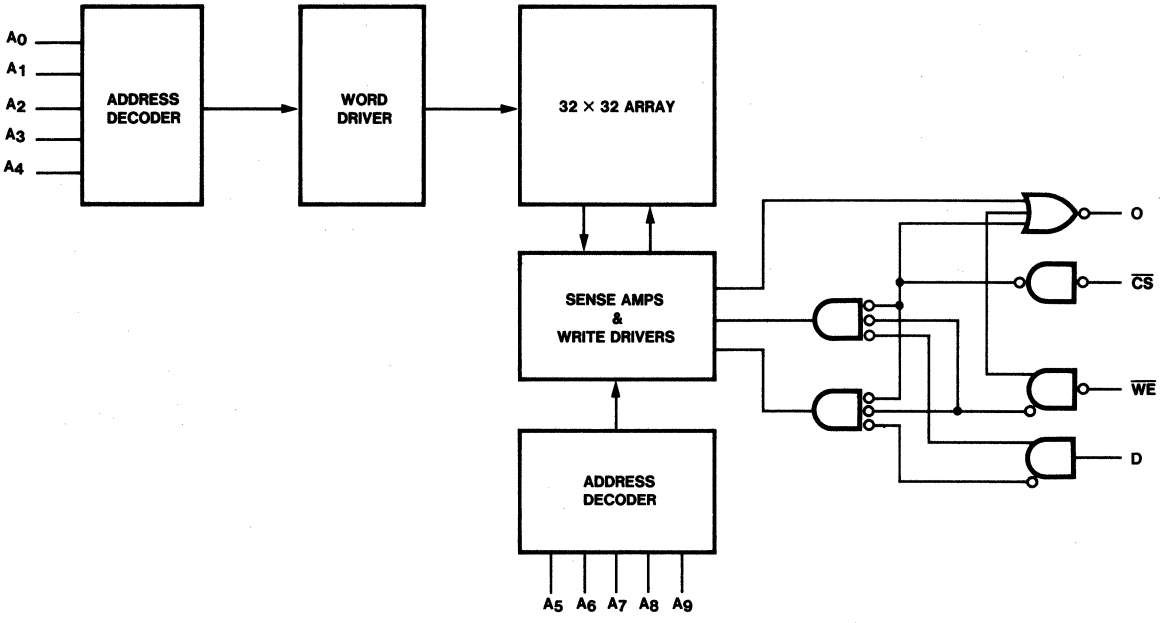


Note
The 16-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6D	DC
Plastic DIP	9B	PC
Flatpak	3L	FC

Logic Diagram



Functional Description

The F100415 is a fully decoded 1024-bit read/write random access memory, organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A_0 through A_9.

One Chip Select input is provided for memory array expansion up to 2048 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of Chip Select, ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the output (O).

The output of the F100415 is an unterminated emitter follower, which allows maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F100415 devices together to allow easy expansion. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output.

Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D	O	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

L = LOW Voltage Levels = −1.7 V (Nominal)
H = HIGH Voltage Levels = −0.9 V (Nominal)
X = Don't Care
Data = Previously stored data

DC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = GND, T_C = 0°C to +85°C unless otherwise specified[1]

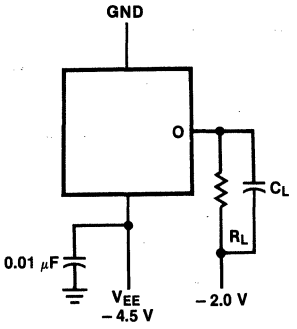
Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			220	μA	$V_{IN} = V_{IH(max)}$
I_{IL}	Input LOW Current, $\overline{CS}$ $\overline{WE}$, A_0-A_9, D	0.5 −50		170	μA	$V_{IN} = V_{IL(min)}$
I_{EE}	Power Supply Current	−150	−105		mA	Inputs and Outputs Open

AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = GND, Output Load = 50 Ω and 30 pF to −2.0 V, T_C = 0°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
	Read Timing						
t_{ACS}	Chip Select Access Time		5.0	8.0	ns		
t_{RCS}	Chip Select Recovery Time		5.0	8.0	ns	*Figures 3a, 3b*	
t_{AA}	Address Access Time[2]		13	20	ns		
	Write Timing						
t_W	Write Pulse Width to Guarantee Writing	14	9.0		ns	t_{WSA} = 5 ns	
t_{WSD}	Data Setup Time prior to Write	4.0	0		ns	*Figure 4*	Measured at 50% of Input to Valid Output ($V_{IL(max)}$ for V_{OL} or $V_{IH(min)}$ for V_{OH})
t_{WHD}	Data Hold Time after Write	4.0	0		ns		
t_{WSA}	Address Setup Time prior to Write	5.0	3.0		ns		
t_{WHA}	Address Hold Time after Write	3.0	0		ns		
t_{WSCS}	Chip Select Setup Time prior to Write	4.0	0		ns	t_W =14 ns	
t_{WHCS}	Chip Select Hold Time after Write	4.0	0		ns	*Figure 4*	
t_{WS}	Write Disable Time		5.0	10	ns		
t_{WR}	Write Recovery Time		7.0	15	ns		
t_r	Output Rise Time		5.0		ns	Measured between 20% and 80% or 80% and 20%, *Figure 2*	
t_f	Output Fall Time		5.0		ns		
C_{IN}	Input Pin Capacitance		4.0	5.0	pF	Measured with a Pulse Technique	
C_{OUT}	Output Pin Capacitance		7.0	8.0	pF		

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Fig. 1 AC Test Circuit



Notes
All Timing Measurements Referenced to 50% of Input Levels
C_L = 30 pF including Fixture and Stray Capacitance
R_L = 50 Ω to −2.0 V.

Fig. 2 Input Levels

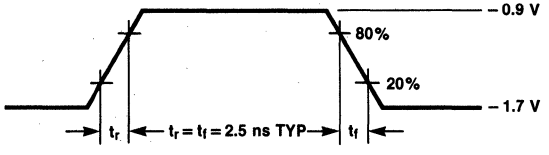
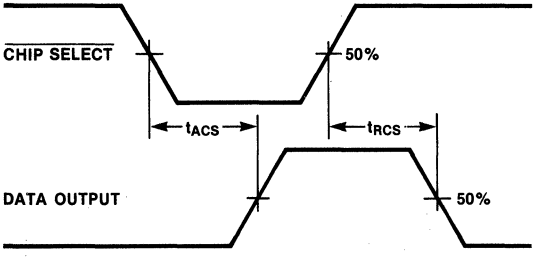


Fig. 3 Read Mode Timing

a Read Mode Propagation Delay from Chip Select



b Read Mode Propagation Delay from Address

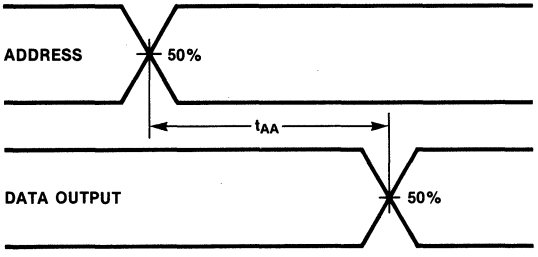
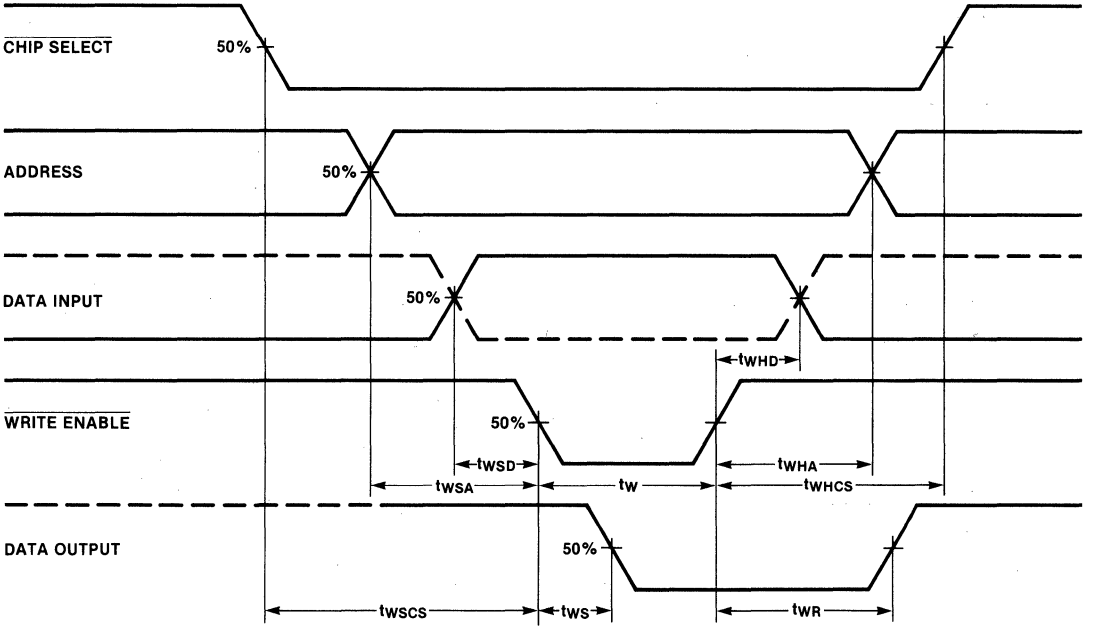


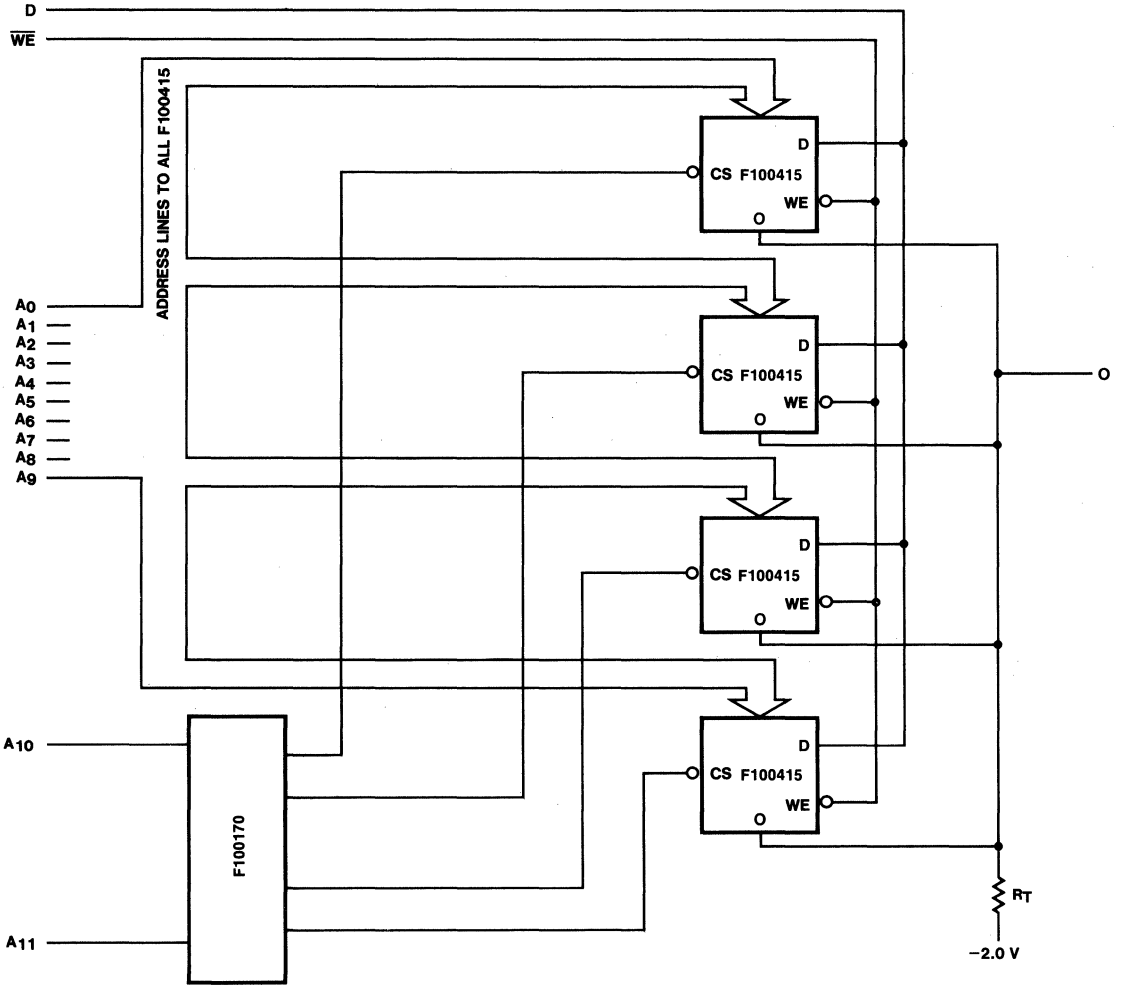
Fig. 4 Write Mode Timing



Note
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Typical Application

4096-Word x n-Bit System



F100416
256 x 4-Bit Programmable Read Only Memory

F100K ECL Product

Description

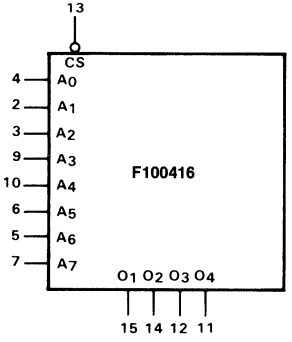
The F100416 is a 1024-bit field Programmable Read Only Memory (PROM), organized 256 words by four bits per word. It is designed for high-speed control, mapping, code conversion, and logic replacement. The device includes full on-chip address decoding, non-inverting Data output lines, and an active-LOW Chip Select line for easy memory expansion. The device is manufactured with all bits in the logic-HIGH state. Programmed bits will furnish LOW levels at corresponding outputs.

- **Address Access Time - 20 ns Max**
- **Chip Select Access Time - 8.0 ns Max**
- **Chip Select Input and Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation - 0.46 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{CS}$	Chip Select Input (Active LOW)
A_0-A_7	Address Inputs
O_1-O_4	Data Outputs

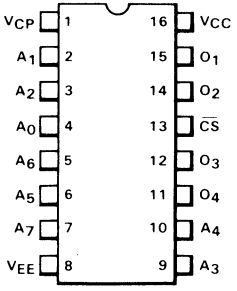
Logic Symbol



V_{CP} = Pin 1
V_{CC} = Pin 16
V_{EE} = Pin 8

Connection Diagram

16-Pin DIP (Top View)

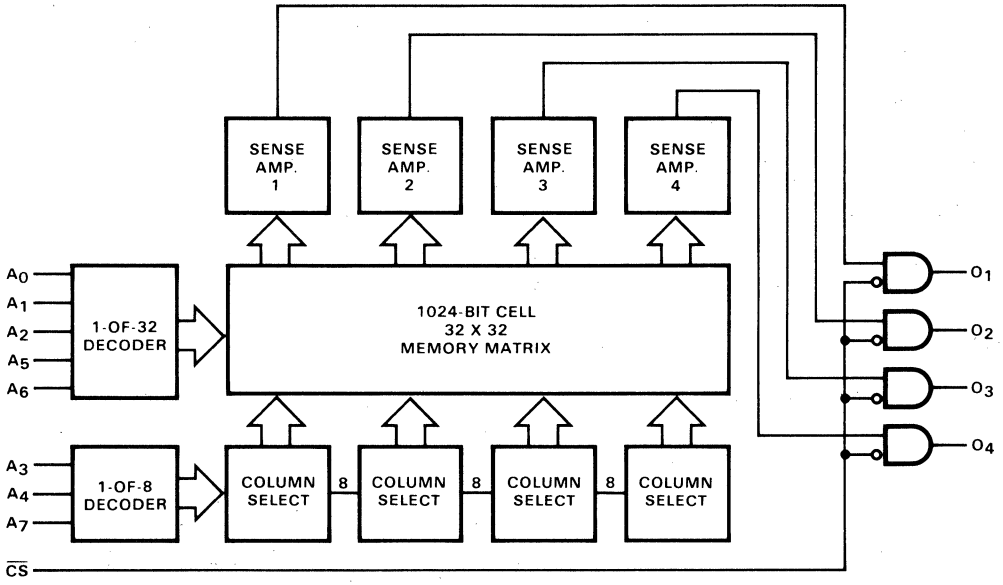


Notes
V_{CP} (Pin 1) is connected to the Programmer (+10.5 V) during programming only; otherwise, it should be grounded.
The Flatpak version has the same pinout (Connection Diagram) as the Dual In-line Package.

Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6D	DC
Plastic DIP	9B	PC
Flatpak	3L	FC

Logic Diagram



Functional Description

The F100416 is a fully decoded bipolar field programmable read only memory organized 256 words by four bits per word. An unterminated emitter-follower output is provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many F100416 devices can be tied together. An external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is off.

One Chip Select ($\overline{CS}$) input is provided for memory array expansion up to 512 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of $\overline{CS}$ from the address without increasing address access time. The device is enabled when $\overline{CS}$ is LOW. When the device is disabled ($\overline{CS}$ = HIGH), all outputs are forced LOW.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_7 inputs, the chip is selected and data is valid at the outputs after t_{AA}.

In the unprogrammed state the outputs are HIGH. To program LOW levels follow the procedure outlined in the *Programming Specifications* table.

Programming

The F100416 is manufactured with all bits in the logic "1" state. Any desired bit (output) can be programmed to a logic "0" state by following the procedure shown below. One may build a programmer to satisfy the specifications or purchase any of the commercially available programmers which meet these specifications.

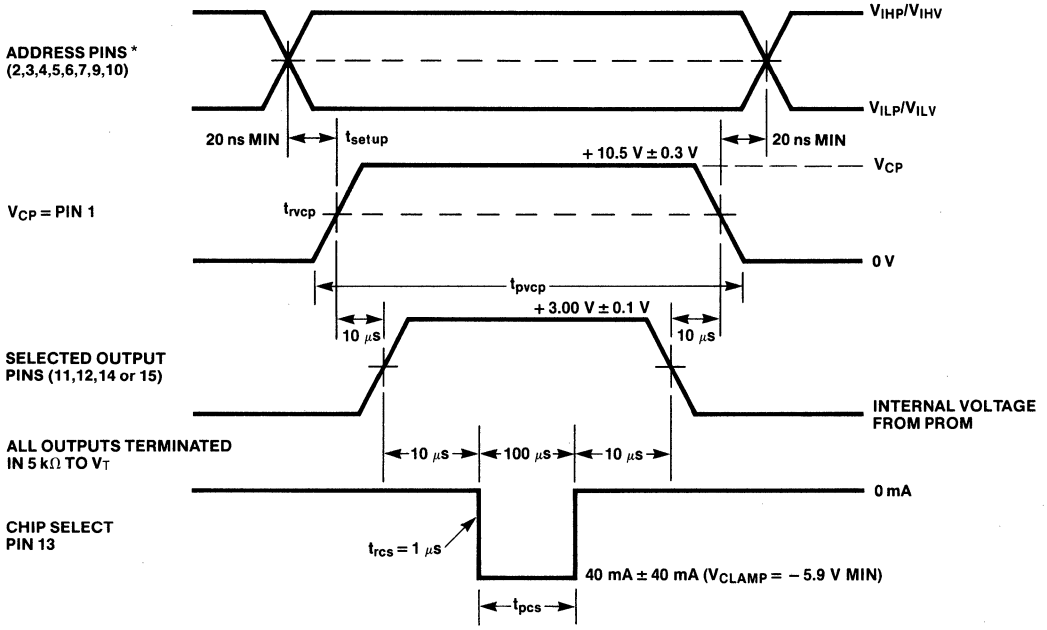
Programming Sequence

1. Apply power to the part: V_{CC} = pin 16 = GND; V_{EE} = pin 8 = −5.2 V ± 5%.
2. Terminate all outputs (pins 11, 12, 14 and 15) with 5 kΩ resistors to V_{TT} = −2.0 V. Note: all input pins, including $\overline{CS}$, have internal 50 kΩ pull-down resistors to V_{EE}.
3. Select the word to be programmed by applying the appropriate voltage levels, as shown in the *Programming Specifications* table, to the Address pins (2, 3, 4, 5, 6, 7, 9 and 10).
4. After the address levels are set raise V_{CP} = Pin 1 from 0 V to +10.5 V ± 0.3 V.

5. After V_{CP} has reached its HIGH level, select the bit to be programmed by applying a HIGH level of +3.0 V ± 0.1 V to the output associated with it, *i.e.*, pins 11, 12, 14 or 15. Only one bit (output) at a time may be selected for programming. Uncommitted outputs are terminated as outlined in 2.
6. After the HIGH level (+3.0 V) has been established at the selected output pin, source a current of −40 mA ± 4 mA out of the Chip Select input (pin 13) to program the selected bit; this applied current pulse which is 100 μs wide and has an approximate rise time of 1 μs is to be furnished by a current sink which clamps at V_{CLAMP} = −5.9 V.
7. To verify a LOW in the bit just programmed follow this sequence:
   (a) Remove current pulse from $\overline{CS}$ pin.
   (b) Remove applied voltage from selected output pin.
   (c) Lower V_{CP} from HIGH level to GND.
   (d) Keep same address but change its levels to normal ECL levels as outlined in the *Programming Specifications* table.
   (e) Enable the chip by applying a LOW level (V_{IL}) to $\overline{CS}$ (pin 13), or leave it open.
   (f) Sense the level at the selected output pin; a LOW level indicates successful programming whereas a HIGH level is a fail indication; in the latter case reprogramming of the bit can be attempted up to a maximum of eight times.
8. To program other bits in the memory repeat steps 3 through 7.

3

Programming Timing Sequence



*Input pins A_1 and A_7 cannot be lower than $V_{IL(min)}$.

Programming Specifications

Symbol	Characteristic	Min	Recommended Value	Max	Unit	Comments
V_{CC}	Power Supply		0		V	
V_{EE}		−5.46	−5.2	−4.94	V	
V_{TT}	Termination Voltage		−2.0		V	Applied to all outputs
V_{IH}	Chip Select (V_{CLAMP})	−0.1	0	+0.1	V	Max Current is 40 mA during programming
V_{IL}		−5.9	−5.2		V	
V_{IHP}	Address Input Threshold	−0.1	0	+0.1	V	Programming levels
V_{ILP}		−3.1	−3.0	−2.9	V	
V_{IHV}	Address Input Threshold	−0.88	−0.87	−0.86	V	Verify levels
V_{ILV}		−1.76	−1.75	−1.74	V	
V_{CP}	Program Setup Pulse	10.2	10.5	10.8	V	
V_{OP}	Programming Pulse	2.9	3.0	3.1	V	Applied to output to be programmed
I_{CS}	Chip Select Programming Current	36	40	44	mA	At V_{CLAMP} = −5.9 V Min on the Chip Select pin
t_{pcs}	Chip Select Programming Pulse	50	100	180	μs	
t_{rcs}	Chip Select Programming Pulse Rise Time	0.5	1.0	2.0	μs	
t_{pvcp}	V_{CP} Programming Pulse	90	140	220	μs	
t_{rvcp}	V_{CP} Programming Rise Time	0.5	1.0	2.0	μs	
t_{setup}	Setup Time	20			ns	Start time of V_{CP} pulse after address is selected

DC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = GND, T_C = 0°C to +85°C unless otherwise specified[1]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			200	μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	−140	−105		mA	Inputs and Outputs Open

AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = GND, Output Load 50 Ω to −2.0 V, T_C = 0°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_{AA}	Address Access Time[2]		11	20	ns	Measured at 50% Points of both Input and Output
t_{ACS}	Chip Select Access Time		4.0	8.0	ns	Measured at 50% Points of both Input and Output

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

F100422
256 x 4-Bit Static Random Access Memory

F100K ECL Product

Description

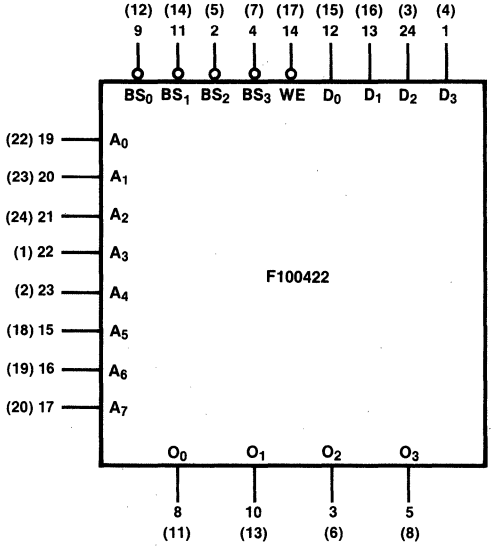
The F100422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits per word. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as four active-LOW Bit Select lines.

- **Address Access Time–10 ns Max**
- **Bit Select Access Time–5.0 ns Max**
- **Four Bits Can be Independently Selected**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{BS_0}$–$\overline{BS_3}$	Bit Select Inputs (Active LOW)
A_0–A_7	Address Inputs
D_0–D_3	Data Inputs
O_0–O_3	Data Outputs

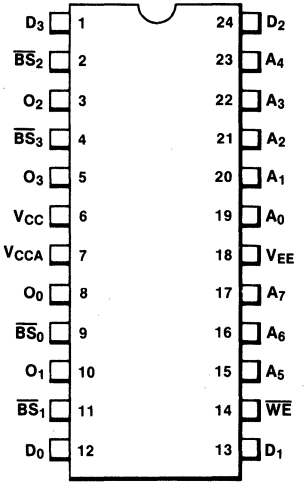
Logic Symbol



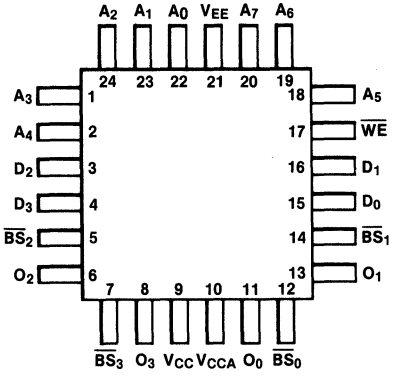
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Connection Diagrams

24-Pin DIP (Top View)



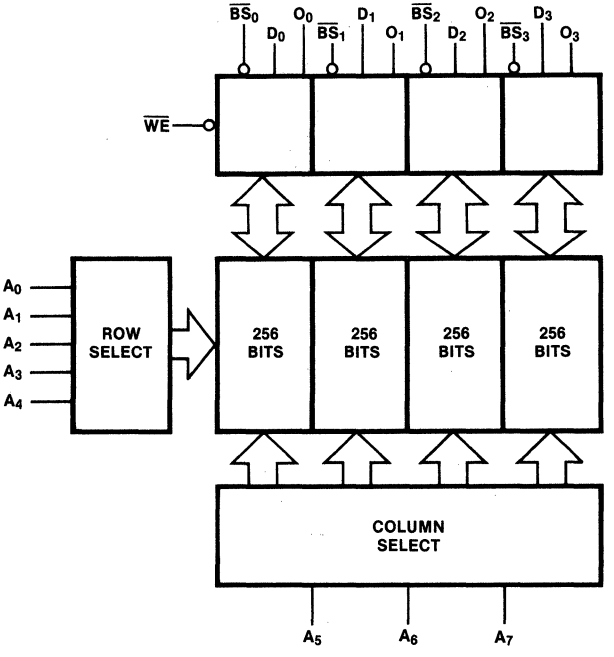
24-Pin Flatpak (Top View)



Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Logic Diagram



Functional Description

The F100422 is a fully decoded 1024-bit read/write random access memory, organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A_0 through A_7.

Four Bit Select inputs are provided for logic flexibility. For larger memories, the fast bit select access time permits the decoding of individual bit selects from the address without increasing address access time.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the bit selected, the data at D_0 - D_3 is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the bits selected. Non-inverted data is then presented at the outputs (O_0-O_3).

The outputs of the F100422 are unterminated emitter followers, which allow maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F100422 devices together to allow easy expansion. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output.

Truth Table

Inputs			Outputs	Mode
$\overline{BS_n}$	$\overline{WE}$	D_n	O_n	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

Each bit has independent $\overline{BS}$, D, and O, but all have common $\overline{WE}$.
L = LOW Voltage Levels = −1.7 V (Nominal)
H = HIGH Voltage Levels = −0.9 V (Nominal)
X = Don't Care
Data = Previously stored data

DC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C unless otherwise specified[1]

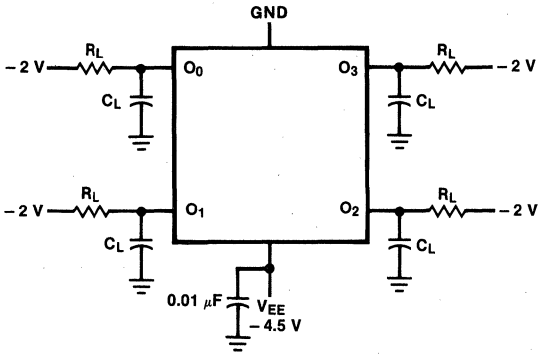
Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			220	μA	$V_{IN} = V_{IH(max)}$
I_{IL}	Input LOW Current, $\overline{CS}$ $\overline{WE}$, A_0–A_{11}, D	0.5 −50		170	μA	$V_{IN} = V_{IL(min)}$
I_{EE}	Power Supply Current	−230	−180		mA	Inputs and Outputs Open

AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND, Output Load = 50 Ω and 30 pF to −2.0 V, T_C = 0°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
	Read Timing						
t_{ABS}	Bit Select Access Time		3.0	5.0	ns		
t_{RBS}	Bit Select Recovery Time		3.0	5.0	ns	*Figures 3a, 3b*	
t_{AA}	Address Access Time[2]		7.0	10	ns		
	Write Timing						
t_W	Write Pulse Width to Guarantee Writing	7.0	5.0		ns	t_{WSA} = 1 ns	Measured at 50% of Input to Valid Output ($V_{IL(max)}$ for V_{OL} or $V_{IH(min)}$ for V_{OH})
t_{WSD}	Data Setup Time prior to Write	1.0	0		ns	*Figure 4*	
t_{WHD}	Data Hold Time after Write	2.0	0		ns		
t_{WSA}	Address Setup Time prior to Write	1.0	0		ns		
t_{WHA}	Address Hold Time after Write	2.0	0		ns		
t_{WSBS}	Bit Select Setup Time prior to Write	1.0	0		ns		
t_{WHBS}	Bit Select Hold Time after Write	2.0	0		ns	t_W = 7 ns *Figure 4*	
t_{WS}	Write Disable Time		3.0	5.0	ns		
t_{WR}	Write Recovery Time		6.0	12	ns		
t_r	Output Rise Time		3.0		ns	Measured between 20% and 80% or 80% and 20%, *Figure 2*	
t_f	Output Fall Time		3.0		ns		
C_{IN}	Input Pin Capacitance		4.0	5.0	pF	Measured with a Pulse Technique	
C_{OUT}	Output Pin Capacitance		7.0	8.0	pF		

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Fig. 1 AC Test Circuit



Notes
All Timing Measurements Referenced to 50% of Input Levels
C_L = 30 pF including Fixture and Stray Capacitance
R_L = 50 Ω to –2.0 V.

Fig. 2 Input Levels

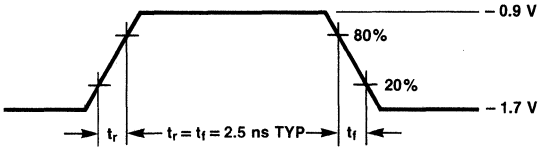
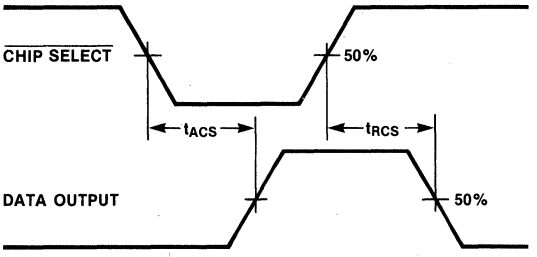


Fig. 3 Read Mode Timing

a Read Mode Propagation Delay from Bit Select



b Read Mode Propagation Delay from Address

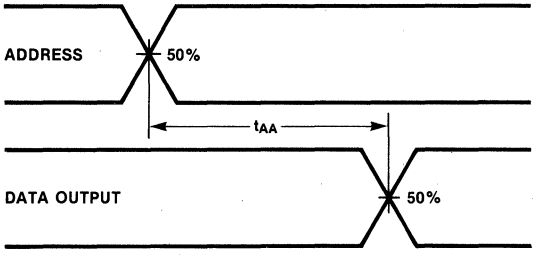
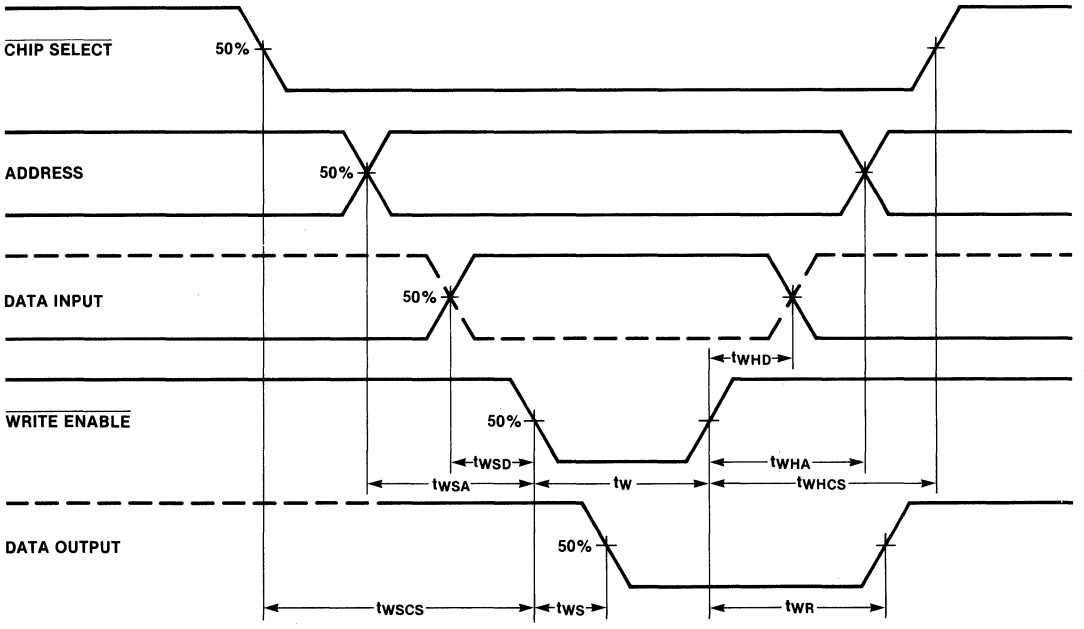


Fig. 4 Write Mode Timing



Note
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

F100470
4096 x 1-Bit Static Random Access Memory

F100K ECL Product

Description

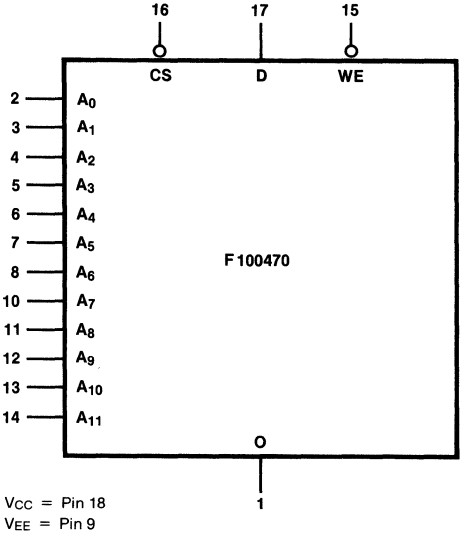
The F100470 is a 4096-bit read/write Random Access Memory (RAM), organized 4096 words by one bit per word and designed for high-speed scratchpad, control and buffer storage applications. It is available in two speed versions, the F100470 and F100470A. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

- **Address Access Time**
  F100470-35 ns Max
  F100470A-25 ns Max
- **Chip Select Access Time**
  F100470-15 ns Max
  F100470A-10 ns Max
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation-0.70 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
A_0-A_{11}	Address Inputs
D	Data Input
O	Data Output

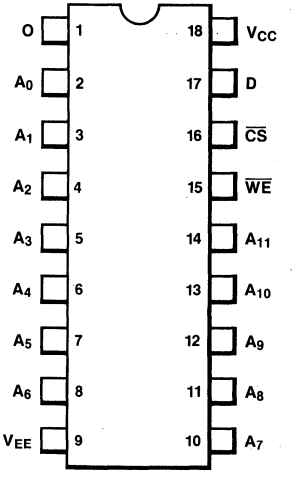
Logic Symbol



V_{CC} = Pin 18
V_{EE} = Pin 9

Connection Diagram

18-Pin DIP (Top View)

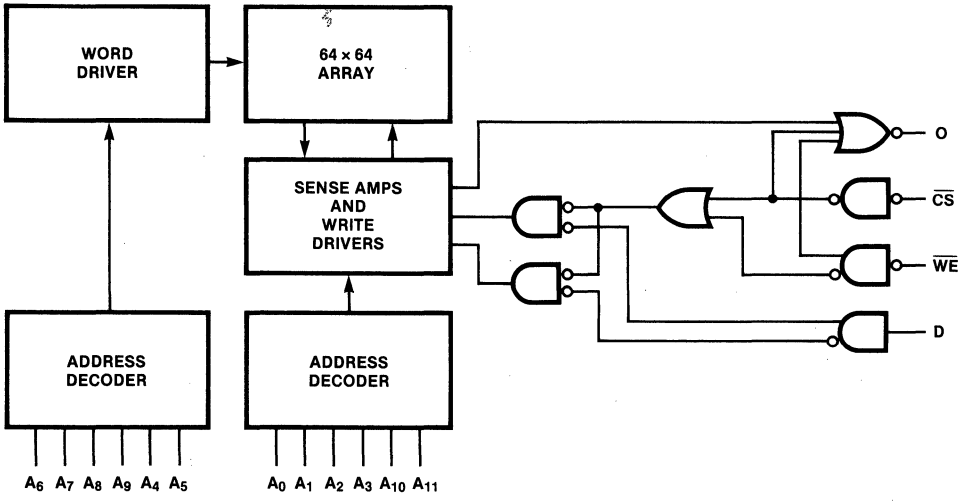


Note
The 18-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	8F	DC
Flatpak	3E	FC

Logic Diagram



Functional Description

The F100470 is a fully decoded 4096-bit read/write random access memory, organized 4096 words by one bit. Bit selection is achieved by means of a 12-bit address, A_0 through A_{11}.

One Chip Select input is provided for memory array expansion up to 8196 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of Chip Select, ($\overline{CS}$) from the address without increasing address access time.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the output (O).

The output of the F100470 is an unterminated emitter follower, which allows maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F100470 devices together. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is OFF.

Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D	O	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

L = LOW Voltage Levels = −1.7 V (Nominal)
H = HIGH Voltage Levels = −0.9 V (Nominal)
X = Don't Care
Data = Previously stored data

DC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = GND, T_C = 0°C to +85°C unless otherwise specified[1]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			220	μA	$V_{IN} = V_{IH(max)}$
I_{IL}	Input LOW Current, $\overline{CS}$ $\overline{WE}$, A_0–A_{11}, D	0.5 −50		170	μA	$V_{IN} = V_{IL(min)}$
I_{EE}	Power Supply Current	−195	−160		mA	Inputs and Outputs Open

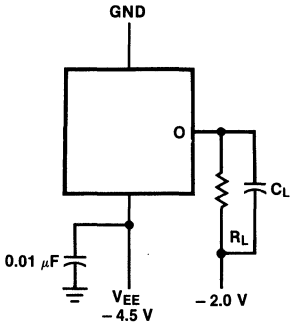
AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = GND, Output Load = 50 Ω and 30 pF to −2.0 V, T_C = 0°C to +85°C

Symbol	Characteristic	F100470 Min	F100470 Max	F100470A Min	F100470A Max	Unit	Condition	
	Read Timing							
t_{ACS}	Chip Select Access Time		15		10	ns		
t_{RCS}	Chip Select Recovery Time		15		10	ns	*Figures 3a, 3b*	
t_{AA}	Address Access Time[2]		35		25	ns		
	Write Timing							
t_W	Write Pulse Width to Guarantee Writing	25		15		ns	t_{WSA} = 10 ns (F100470 and F100470A), *Figure 4*	Measured at 50% of Input to Valid Output ($V_{IL(max)}$ for V_{OL} or $V_{IH(min)}$ for V_{OH})
t_{WSD}	Data Setup Time prior to Write	5.0		5.0		ns		
t_{WHD}	Data Hold Time after Write	5.0		5.0		ns		
t_{WSA}	Address Setup Time prior to Write	10		10		ns		
t_{WHA}	Address Hold Time after Write	5.0		5.0		ns	t_W = 25 ns (F100470), 15 ns (F100470A), *Figure 4*	
t_{WSCS}	Chip Select Setup Time prior to Write	5.0		5.0		ns		
t_{WHCS}	Chip Select Hold Time after Write	5.0		5.0		ns		
t_{WS}	Write Disable Time		15		15	ns		
t_{WR}	Write Recovery Time		20		20	ns		

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r	Output Rise Time		5.0		ns	Measured between 20% and
t_f	Output Fall Time		5.0		ns	80% or 80% and 20% *Figure 2*
C_{IN}	Input Pin Capacitance		4.0	5.0	pF	Measured with a Pulse
C_{OUT}	Output Pin Capacitance		7.0	8.0	pF	Technique

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a psuedorandom testing pattern.

Fig. 1 AC Test Circuit



Notes
All Timing Measurements Referenced to 50% of Input Levels
C_L = 30 pF including Fixture and Stray Capacitance
R_L = 50 Ω to −2.0 V.

Fig. 2 Input Levels

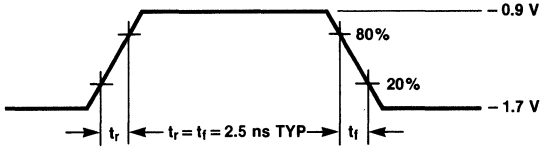
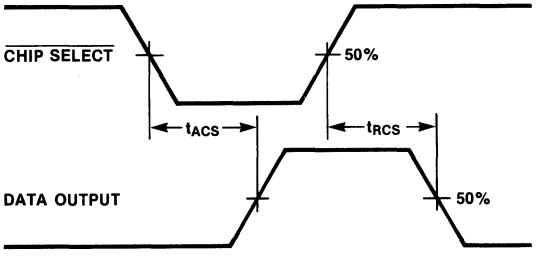
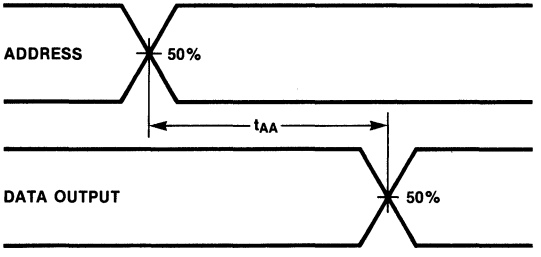


Fig. 3 Read Mode Timing

a Read Mode Propagation Delay from Chip Select

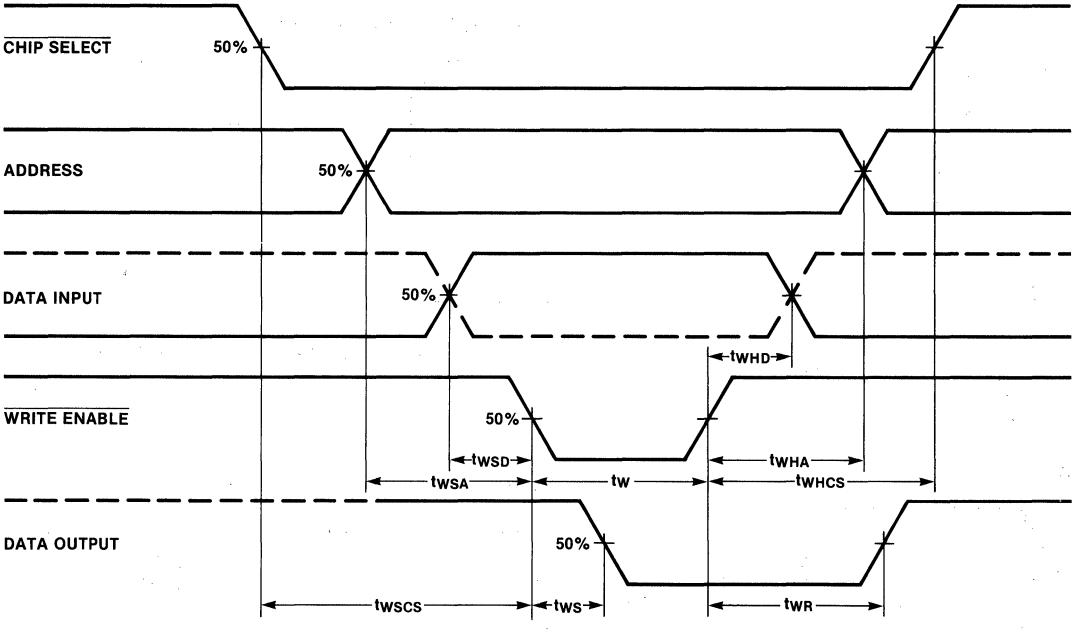


b Read Mode Propagation Delay from Address



3

Fig. 4 Write Mode Timing



Note
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

F100474
1024 x 4-Bit Static Random Access Memory

F100K ECL Product

Description

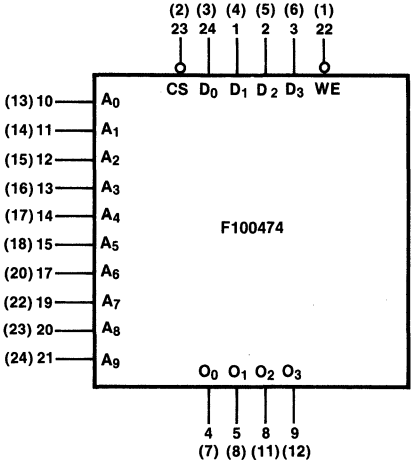
The F100474 is a 4096-bit read/write Random Access Memory (RAM), organized 1024 words by four bits per word. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

- **Address Access Time–25 ns Max**
- **Chip Select Access Time–15 ns Max**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation–0.70 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
A_0–A_9	Address Inputs
D_0–D_3	Data Inputs
O_0–O_3	Data Outputs

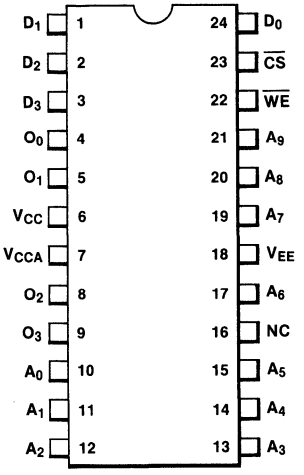
Logic Symbol



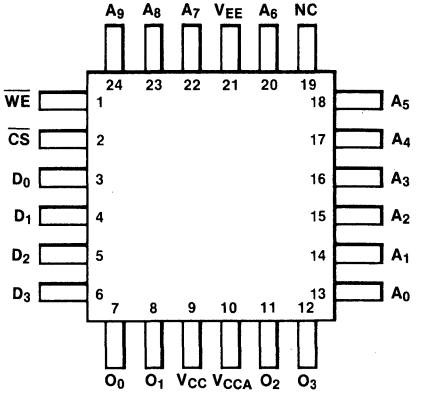
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Connection Diagrams

24-Pin DIP (Top View)



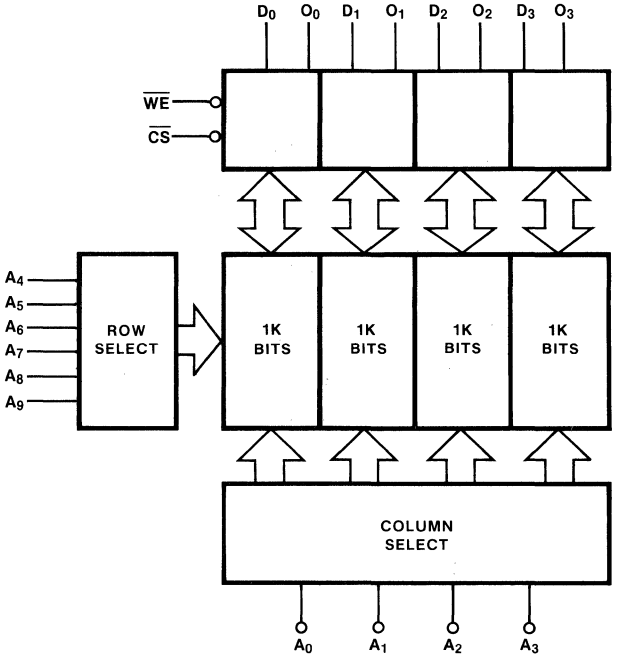
24-Pin Flatpak (Top View)



Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Logic Diagram



Functional Description

The F100474 is a fully decoded 4096-bit read/write random access memory, organized 1024 words by four bits. Word selection is achieved by means of a 10-bit address, A_0 through A_9.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D_0–D_3 is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the outputs (O_0–O_3).

The outputs of the F100474 are unterminated emitter followers, which allow maximum flexibility in output connection configurations. In many applications such as memory expansion, the outputs of many F100474 devices can be tied together. In other applicatons the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is OFF.

Truth Table

Inputs			Outputs	Mode
$\overline{CS}$	$\overline{WE}$	D_n	O_n	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

L = LOW Voltage Levels = −1.7 V (Nominal)
H = HIGH Voltage Levels = −0.9 V (Nominal)
X = Don't Care
Data = Previously stored data

DC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C unless otherwise specified[1]

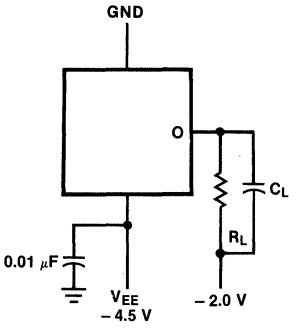
Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			220	μA	$V_{IN} = V_{IH(max)}$
I_{IL}	Input LOW Current, $\overline{CS}$ $\overline{WE}$, A_0–A_{11}, D	0.5 −50		170	μA	$V_{IN} = V_{IL(min)}$
I_{EE}	Power Supply Current	−195	−160		mA	Inputs and Outputs Open

AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND, Output Load = 50 Ω and 30 pF to −2.0 V, T_C = 0°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
	Read Timing						
t_{ACS}	Chip Select Access Time		10	15	ns		
t_{RCS}	Chip Select Recovery Time		10	15	ns	*Figures 3a, 3b*	
t_{AA}	Address Access Time[2]		20	25	ns		
	Write Timing						
t_W	Write Pulse Width to Guarantee Writing	16	10		ns	t_{WSA} = 10 ns	Measured at 50% of Input to Valid Output ($V_{IL(max)}$ for V_{OL} or $V_{IH(min)}$ for V_{OH})
t_{WSD}	Data Setup Time prior to Write	5.0	1.0		ns	*Figure 4*	
t_{WHD}	Data Hold Time after Write	5.0	1.0		ns		
t_{WSA}	Address Setup Time prior to Write	10	3.0		ns		
t_{WHA}	Address Hold Time after Write	4.0	1.0		ns		
t_{WSCS}	Chip Select Setup Time prior to Write	5.0	1.0		ns		
t_{WHCS}	Chip Select Hold Time after Write	5.0	1.0		ns	t_W = 16 ns *Figure 4*	
t_{WS}	Write Disable Time		6.0	15	ns		
t_{WR}	Write Recovery Time		8.0	20	ns		
t_r	Output Rise Time		5.0		ns	Measured between 20% and 80% or 80% and 20%, *Figure 2*	
t_f	Output Fall Time		5.0		ns		
C_{IN}	Input Pin Capacitance		4.0	5.0	pF	Measured with a Pulse Technique	
C_{OUT}	Output Pin Capacitance		7.0	8.0	pF		

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Fig. 1 AC Test Circuit



Notes
All Timing Measurements Referenced to 50% of Input Levels
C_L = 30 pF including Fixture and Stray Capacitance
R_L = 50 Ω to –2.0 V.

Fig. 2 Input Levels

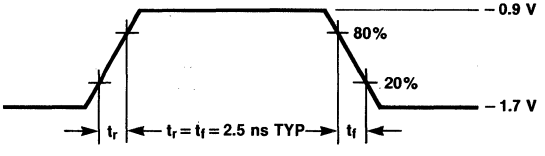
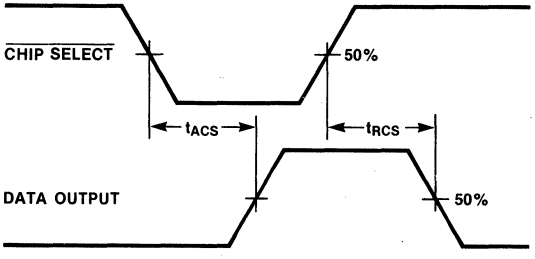


Fig. 3 Read Mode Timing

a Read Mode Propagation Delay from Chip Select



b Read Mode Propagation Delay from Address

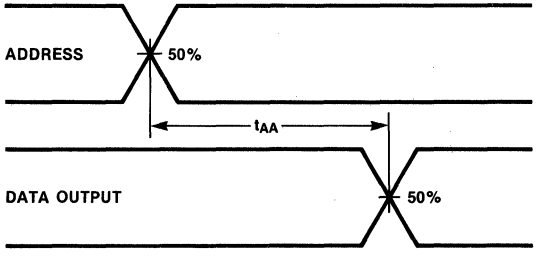
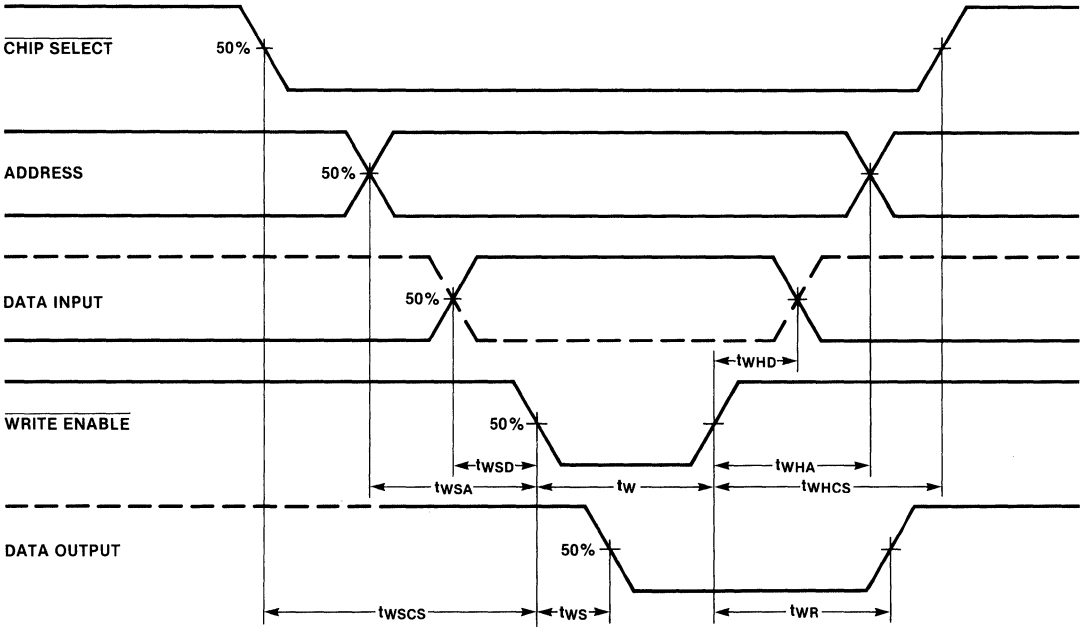
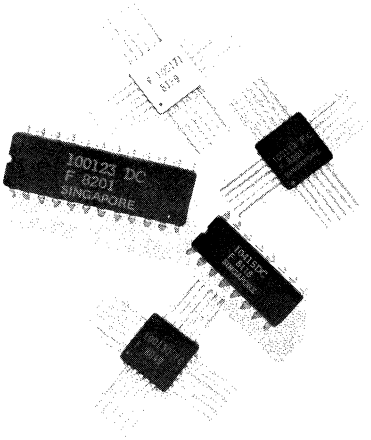


Fig. 4 Write Mode Timing



Note
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.



F10K DC Family Specifications

DC characteristics for the F10K series memories. Parametric limits listed below are guaranteed for all F10K memories, except where noted on individual data sheets.

Absolute Maximum Ratings: Above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{EE} Pin Potential to Ground Pin	−7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	−30 mA to +0.1 mA

Guaranteed Operating Ranges

Supply Voltage (V_{EE})			Ambient Temperature
Min	Typ	Max	T_A
−5.46 V	−5.2 V	−4.94 V	0°C to +75°C

4

DC Characteristics: V_{EE} = −5.2 V, Output Load = 50 Ω and 30 pF to −2.0 V, T_A = 0°C to 75°C[1]

Symbol	Characteristic	Min	Typ	Max	Unit	T_A	Conditions[2]	
V_{OH}	Output HIGH Voltage	−1000 −960 −900		−840 −810 −720	mV	0°C +25°C +75°C	$V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$	Loading is 50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1870 −1850 −1830		−1665 −1650 −1625	mV	0°C +25°C +75°C		
V_{OHC}	Output HIGH Voltage	−1020 −980 −920			mv	0°C +25°C +75°C	$V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage			−1645 −1630 −1605	mV	0°C +25°C +75°C		
V_{IH}	Input HIGH Voltage	−1145 −1105 −1045		−840 −810 −720	mV	0°C +25°C +75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input LOW Voltage	−1870 −1850 −1830		−1490 −1475 −1450	mV	0°C +25°C +75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IL}	Input LOW Current	0.5		170	μA	+25°C	$V_{IN} = V_{IL(min)}$	

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

F10145A
16 x 4 Register File (RAM)

F10K Voltage Compensated ECL

Description

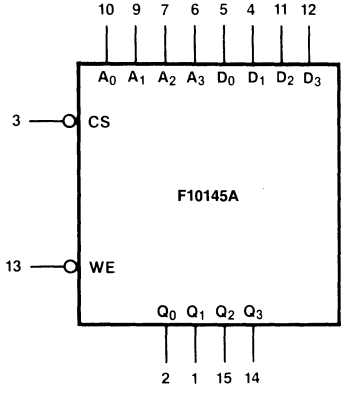
The F10145A and F10545A are high-speed 64-bit Random Access Memories organized as a 16-word by 4-bit array. External logic requirements are minimized by internal address decoding, while memory expansion and data bussing are facilitated by the output disabling features of the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs.

A HIGH signal on $\overline{CS}$ prevents read and write operations and forces the outputs to the LOW state. When $\overline{CS}$ is LOW, the $\overline{WE}$ input controls chip operations. A HIGH signal on $\overline{WE}$ disables the Data input (D_n) buffers and enables readout from the memory location determined by the Address (A_n) inputs. A LOW signal on $\overline{WE}$ forces the Q_n outputs LOW and allows data on the D_n inputs to be stored in the addressed location. Data exists in the same logical sense as presented at the data inputs, *i.e.*, the memory is non-inverting.

Pin Names

$\overline{CS}$	Chip Select
A_0-A_3	Address
D_0-D_3	Data Inputs
$\overline{WE}$	Write Enables
Q_0-Q_3	Data Outputs

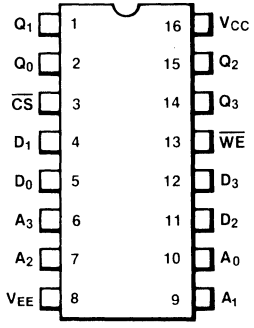
Logic Symbol



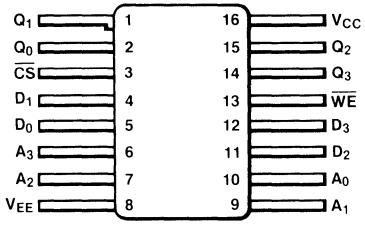
V_{CC} = Pin 16
V_{EE} = Pin 8

Connection Diagrams

16-Pin DIP (Top View)



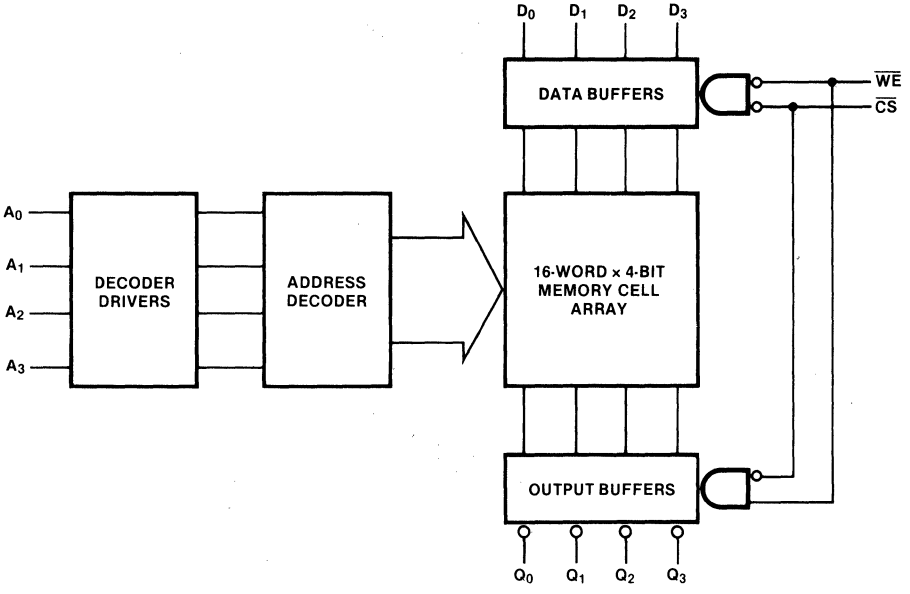
16-Pin Flatpak (Top View)



Ordering Information (See Section 5)

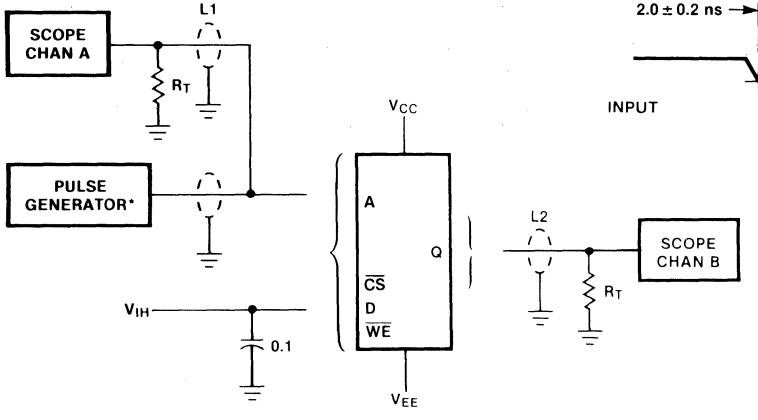
Package	Outline	Order Code
Ceramic DIP	4J	DC
Flatpak	3L	FC

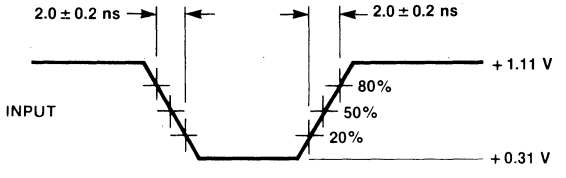
Logic Diagram



V_{CC} = Pin 16
V_{EE} = Pin 8

Fig. 1 Switching Circuit and Waveforms





Notes
V_{CC} = +2 V, V_{EE} = −3.2 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 5 pF

DC Characteristics: V_{EE} = −5.2 V, V_{CC} = GND, T_A = 25°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current $\overline{CS}$, A_0-A_3 $\overline{WE}$, D_0-D_3			200 220	μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	−150	−100		mA	Inputs and Outputs Open

AC Characteristics: V_{EE} = −5.2 V, V_{CC} = GND, T_A = 25°C

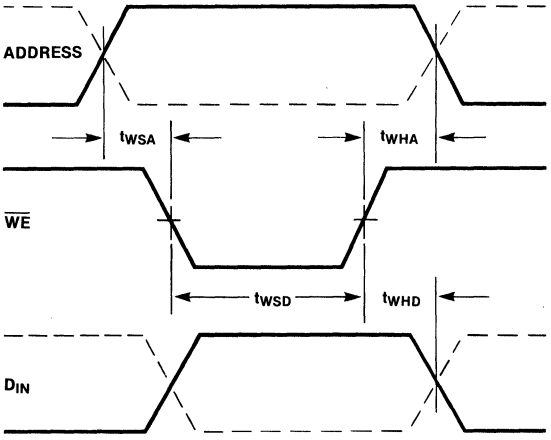
Symbol	Characteristic	Min	Typ	Max	Unit	Condition
	Access/Recovery Times					
t_{ACS}	Chip Select Access	3.0	4.5	6.0	ns	
t_{RCS}	Chip Select Recovery	3.0	4.5	6.0	ns	*Figures 1* and *3*
t_{AA}	Address Access	4.5	6.5	9.0	ns	
	Write Setup Times					
t_{WSD}	Data	4.5	3.0		ns	
t_{WSCS}	Chip Select	4.5	2.5		ns	
t_{WSA}	Address	3.5	1.5		ns	
	Write Hold Times					*Figures 1* and *2*
t_{WHD}	Data	−1.0	−2.5		ns	
t_{WHCS}	Chip Select	0.5	0		ns	
t_{WHA}	Address	1.0	−1.0		ns	
t_{WR}	Write Recovery Time	3.0	4.5	6.0	ns	*Figures 1* and *3*
t_{WS}	Write Disable Time	3.0	4.5	6.0	ns	
t_W	Write Pulse Width, Min	4.0	2.5		ns	*Figures 1* and *2*
t_{CS}	Chip Select Pulse Width, Min	4.0	2.5		ns	
	Select Setup Times					
t_{CSD}	Data	4.5	3.0		ns	
t_{CSW}	Write Enable	4.5	2.5		ns	
t_{CSA}	Address	3.5	1.5		ns	*Figures 1* and *2*
	Write Hold Times					
t_{CHD}	Data	−1.0	−2.5		ns	
t_{CHW}	Write Enable	0.5	0		ns	
t_{CHA}	Address	1.0	−1.0		ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	1.5	2.5	3.9	ns	*Figures 1* and *3*

*See Family Characteristics for other dc specifications.

Fig. 2 Write Modes

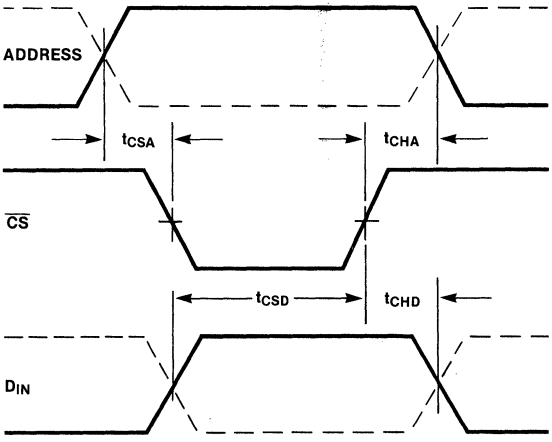
Write Enable Strobe

ADDRESS AND D_{IN} SET UP AND HOLD TIMES ($\overline{CS}$ = LOW)

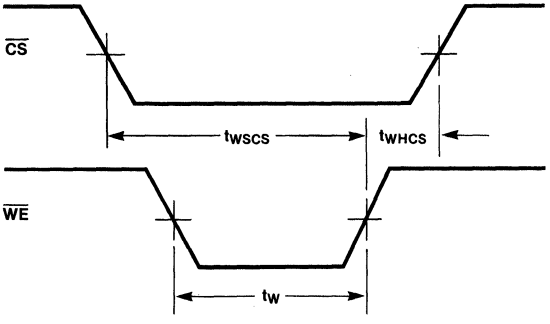


Chip Select Strobe

ADDRESS AND D_{IN} SET UP AND HOLD TIMES ($\overline{WE}$ = LOW)



CHIP SELECT SET-UP AND HOLD TIMES



WRITE ENABLE SET-UP AND HOLD TIMES, $\overline{CS}$ PULSE WIDTH[2]

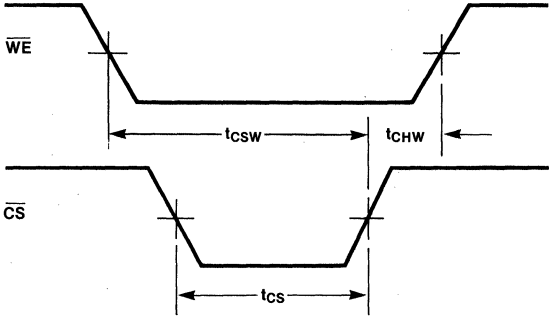
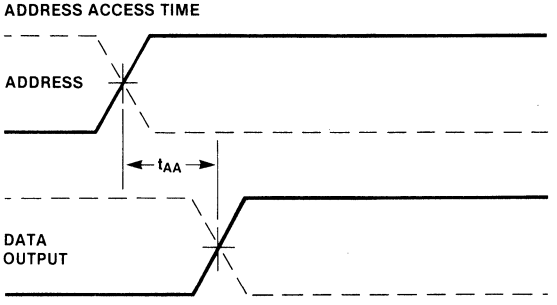
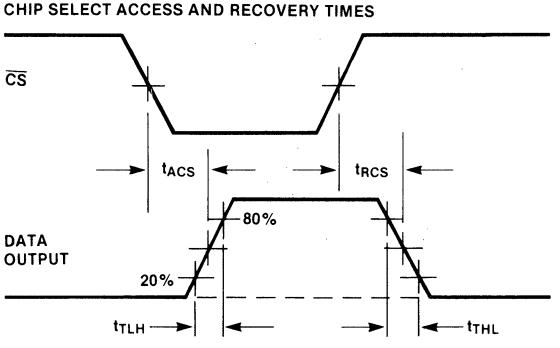


Fig. 3 Read Modes

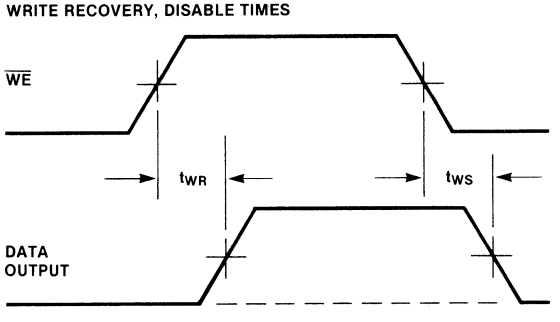
Address Input to Data Output ($\overline{WE}$ = HIGH, $\overline{CS}$ = LOW)



Chip Select Input to Data Output ($\overline{WE}$ = HIGH)



Write Enable Input to Data Output ($\overline{CS}$ = LOW)



F10402
16 x 4 Register File (RAM)

F10K ECL Product

Description

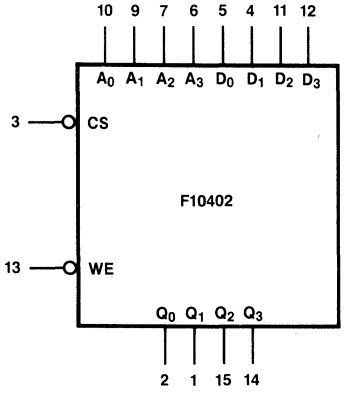
The F10402 is a high-speed 64-bit Random Access Memory (RAM) organized as a 16-word by 4-bit array. External logic requirements are minimized by internal address decoding, while memory expansion and data busing are facilitated by the output disabling features of the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs.

A HIGH signal on $\overline{CS}$ prevents read and write operations and forces the outputs to the LOW state. When $\overline{CS}$ is LOW, the $\overline{WE}$ input controls chip operations. A HIGH signal on $\overline{WE}$ disables the Data input (D_n) buffers and enables readout from the memory location determined by the Address (A_n) inputs. A LOW signal on $\overline{WE}$ forces the Q_n outputs LOW and allows data on the D_n inputs to be stored in the addressed location. Data exists in the same logical sense as presented at the data inputs, *i.e.*, the memory is non-inverting.

Pin Names

$\overline{CS}$	Chip Select Input
A_0-A_3	Address Inputs
D_0-D_3	Data Inputs
$\overline{WE}$	Write Enable Input
Q_0-Q_3	Data Outputs

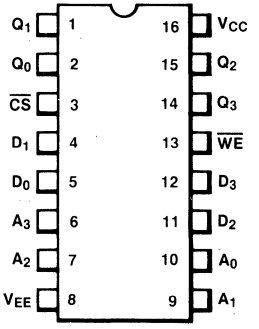
Logic Symbol



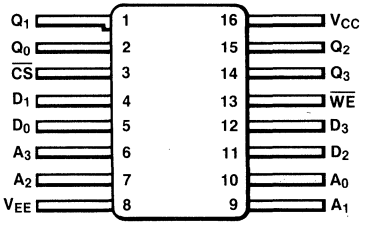
V_{CC} = Pin 16
V_{EE} = Pin 8

Connection Diagrams

16-Pin DIP (Top View)



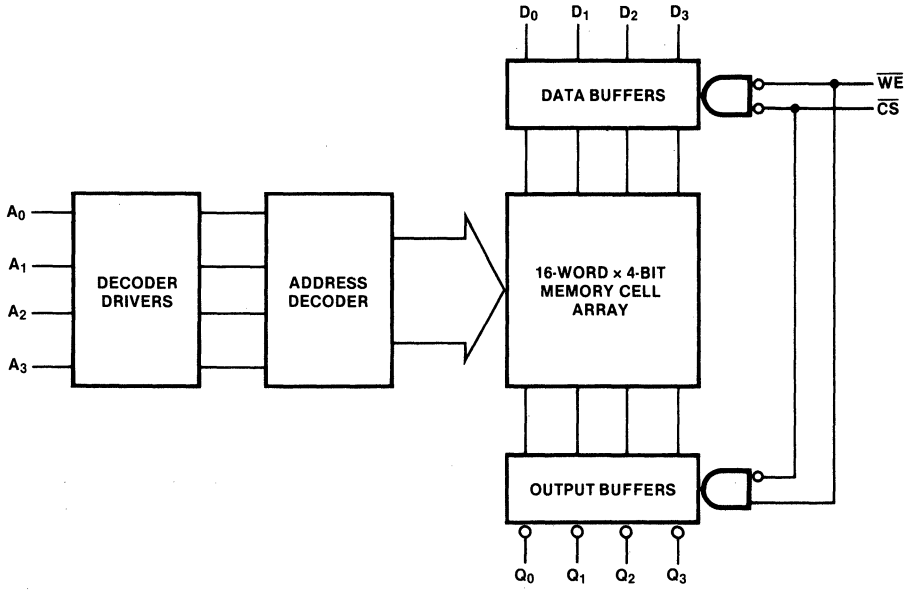
16-Pin Flatpak (Top View)



Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	4J	DC
Flatpak	3L	FC

Logic Diagram



DC Characteristics: $V_{EE} = -5.2\ V \pm 5\%$, $V_{CC} = V_{CCA} = GND$, $T_A = 0°C$ to $+75°C$ unless otherwise specified*

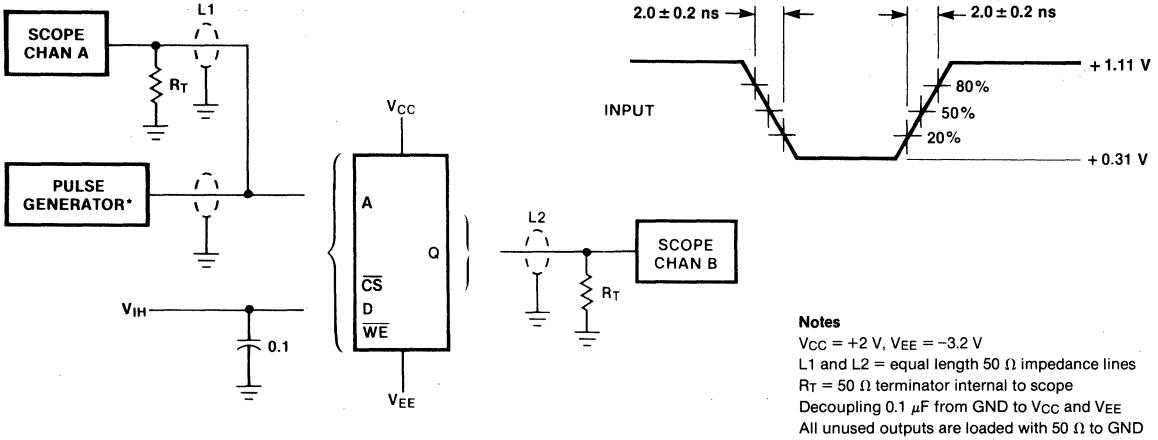
Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current All Inputs			300	μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	−170	−110	−70	mA	Inputs Open

*See Family Characteristics for other dc specifications.

AC Characteristics: V_{EE} = −5.2 V, V_{CC} = GND, Applies to Flatpak and DIP Packages

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
	Access/Recovery Timing								
t_{ACS}	Chip Select Access		3.30		3.50		3.80	ns	
t_{RCS}	Chip Select Recovery		3.30		3.50		3.80	ns	*Figures 1* and *3*
t_{AA}	Address Access	3.00	5.00	3.00	5.30	3.50	6.00	ns	
	Write Timing, Setup								
t_{WSD}	Data	0.50		0.50		0.80		ns	
t_{WSCS}	Chip Select	1.50		1.50		1.50		ns	
t_{WSA}	Address	1.00		1.00		1.00		ns	*Figures 1* and *2*
	Write Timing, Hold								t_W = 6 ns
t_{WHD}	Data	0.50		0.50		0.50		ns	
t_{WHCS}	Chip Select	0.50		0.50		0.50		ns	
t_{WHA}	Address	2.50		2.50		2.50		ns	
t_{WR}	Write Recovery Time	4.00		4.00		4.50		ns	*Figures 1* and *3*
t_{WS}	Write Disable Time	3.00		3.00		3.50		ns	
t_W	Write Pulse Width, (LOW)	2.50		2.50		3.00		ns	*Figures 1* and *2*
t_{CS}	Chip Select Pulse Width, (LOW)	2.50		2.50		3.00		ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	1.70	0.50	1.70	0.50	1.70	ns	*Figures 1* and *3*

Fig. 1 AC Test Circuit and Waveforms

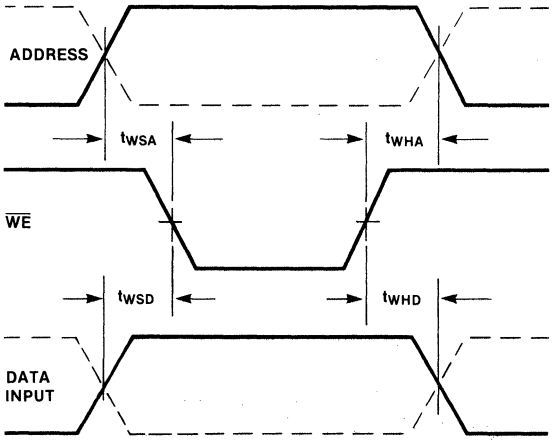


Notes
V_{CC} = +2 V, V_{EE} = −3.2 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 5 pF
*One or more generators as required

Fig. 2 Write Modes

Write Enable Strobe

ADDRESS AND DATA INPUT SET-UP AND HOLD TIMES
($\overline{CS}$ = LOW)



CHIP SELECT SET-UP AND HOLD TIMES

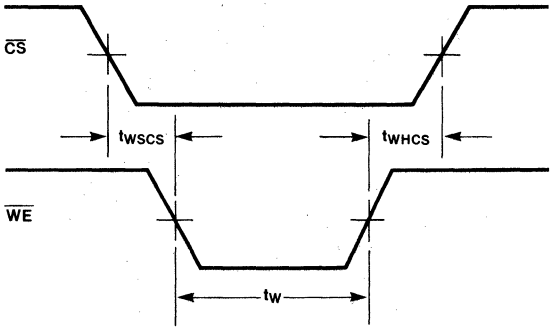
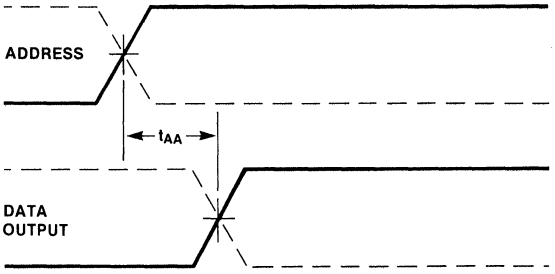


Fig. 3 Read Modes

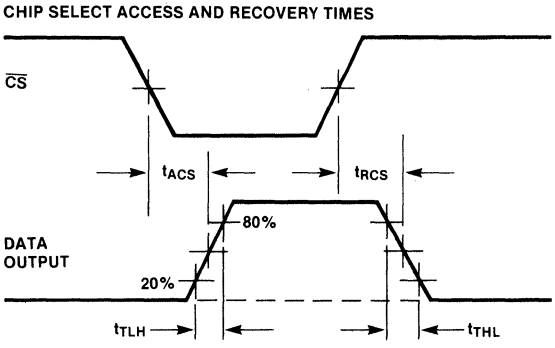
Address Input to Data Output ($\overline{WE}$ = HIGH, $\overline{CS}$ = LOW)

ADDRESS ACCESS TIME



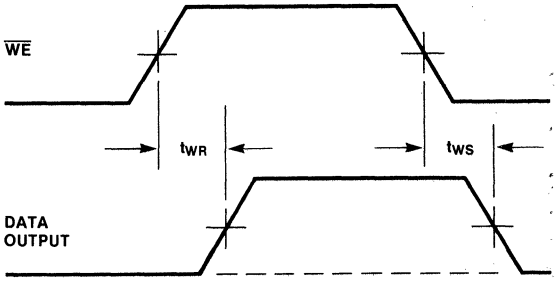
Chip Select Input to Data Output ($\overline{WE}$ = HIGH)

CHIP SELECT ACCESS AND RECOVERY TIMES



Write Enable Input to Data Output ($\overline{CS}$ = LOW)

WRITE RECOVERY, DISABLE TIMES



F10414
256 x 1-Bit Static Random Access Memory

F10K ECL Product

Description

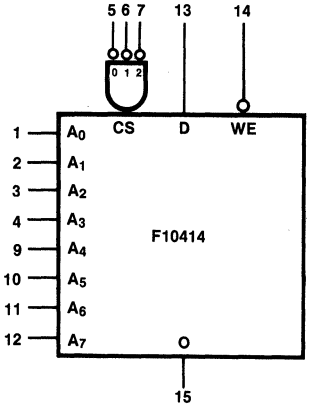
The F10414 is a 256-bit read/write Random Access Memory (RAM), organized 256 words by one bit. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as three active-LOW Chip Select lines.

- **Address Access Time–10 ns Max**
- **Chip Select Access Time–6.0 ns Max**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation–1.8 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}_0$–$\overline{CS}_2$	Chip Select Inputs (Active LOW)
A_0–A_7	Address Inputs
D	Data Input
O	Data Output

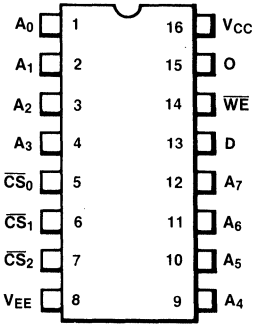
Logic Symbol



V_{CC} = Pin 16
V_{EE} = Pin 8

Connection Diagram

16-Pin DIP (Top View)

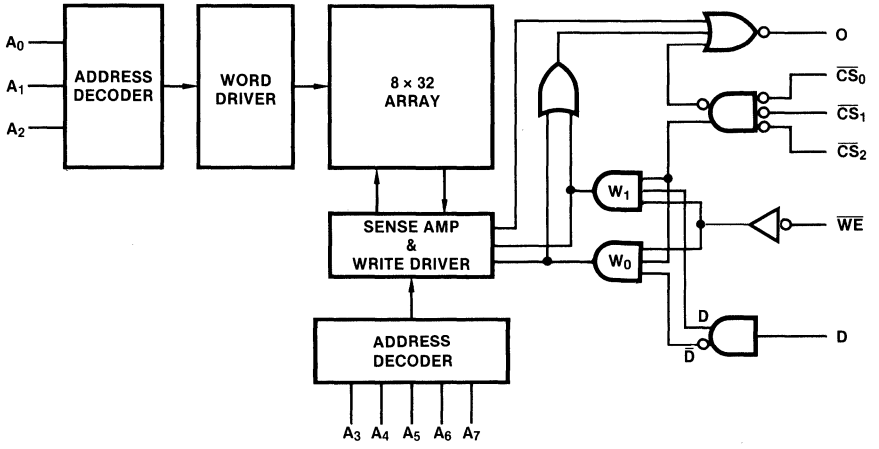


Note
The 16-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6D	DC
Plastic DIP	9B	PC
Flatpak	3L	FC

Logic Diagram



Functional Description

The F10414 is a fully decoded 256-bit read/write random access memory, organized 256 words by one bit. Bit selection is achieved by means of an 8-bit address, A_0 through A_7.

Three active-LOW Chip Select inputs are provided for increased logic flexibility. This permits memory array expansion up to 2048 words with the F10170 decoder. For larger memories, the fast chip select access time permits the decoding of Chip Select, $\overline{CS}$, from the address without affecting system performance.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the output (O).

The output of the F10414 is an unterminated emitter follower, which allows maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F10414 devices together to allow easy expansion. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output.

Truth Table

Inputs					Output	Mode
$\overline{CS_0}$	$\overline{CS_1}$	$\overline{CS_2}$	$\overline{WE}$	D	O	
X	X	H*	X	X	L	Not Selected
L	L	L	L	L	L	Write "0"
L	L	L	L	H	L	Write "1"
L	L	L	H	X	Data	Read

L = LOW Voltage Levels = −1.7 V (Nominal)
H = HIGH Voltage Levels = −0.9 V (Nominal)
X = Don't Care
Data = Previously stored data
*One or more Chip Selects HIGH

DC Characteristics: $V_{EE} = -5.2$ V, V_{CC} = GND, $T_A = 0°C$ to $+75°C$ unless otherwise specified[1]

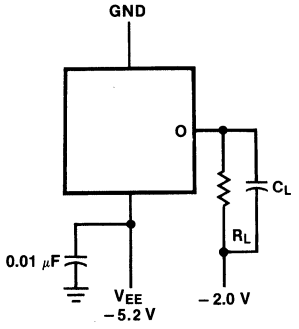
Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
I_{IH}	Input HIGH Current			220	μA	$V_{IN} = V_{IH(max)}$	
I_{IL}	Input LOW Current, $\overline{CS}$ $\overline{WE}$, A_0-A_{11}, D	0.5 −50		170	μA	$V_{IN} = V_{IL(min)}$	
I_{EE}	Power Supply Current		−90		mA	$T_A = +75°C$	Inputs and Outputs Open
		−140	−100			$T_A = 0°C$	

AC Characteristics: $V_{EE} = -5.2$ V ±5%, V_{CC} = GND, Output Load = 50 Ω and 30 pF to −2.0 V, $T_A = 0°C$ to $+75°C$

Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
	Read Timing						
t_{ACS}	Chip Select Access Time		4.0	6.0	ns		
t_{RCS}	Chip Select Recovery Time		4.0	6.0	ns	*Figures 3a, 3b*	
t_{AA}	Address Access Time[2]		7.0	10	ns		
	Write Timing						
t_W	Write Pulse Width to Guarantee Writing	7.0	4.0		ns	t_{WSA} = 1 ns	Measured at 50% of Input to Valid Output ($V_{IL(max)}$ for V_{OL} or $V_{IH(min)}$ for V_{OH})
t_{WSD}	Data Setup Time prior to Write	1.0	0		ns	*Figure 4*	
t_{WHD}	Data Hold Time after Write	2.0	0		ns		
t_{WSA}	Address Setup Time prior to Write	1.0	0		ns		
t_{WHA}	Address Hold Time after Write	2.0	0		ns		
t_{WSCS}	Chip Select Setup Time prior to Write	1.0	0		ns	t_W = 7 ns	
t_{WHCS}	Chip Select Hold Time after Write	2.0	0		ns	*Figure 4*	
t_{WS}	Write Disable Time		4.0	8.0	ns		
t_{WR}	Write Recovery Time		5.0	10	ns		
t_r	Output Rise Time		3.0		ns	Measured between 20% and 80% or 80% and 20%, *Figure 2*	
t_f	Output Fall Time		3.0		ns		
C_{IN}	Input Pin Capacitance		4.0	5.0	pF	Measured with a Pulse Technique	
C_{OUT}	Output Pin Capacitance		7.0	8.0	pF		

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Fig. 1 AC Test Circuit



Notes
All Timing Measurements Referenced to 50% of Input Levels
C_L = 30 pF including Fixture and Stray Capacitance
R_L = 50 Ω to −2.0 V.

Fig. 2 Input Levels

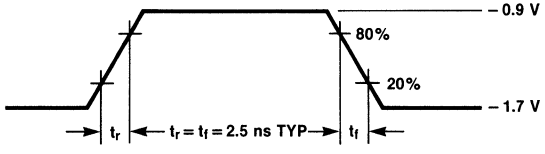
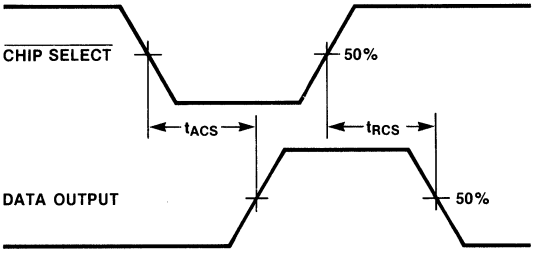


Fig. 3 Read Mode Timing

a Read Mode Propagation Delay from Chip Select



b Read Mode Propagation Delay from Address

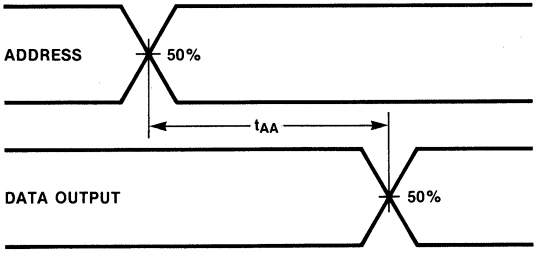


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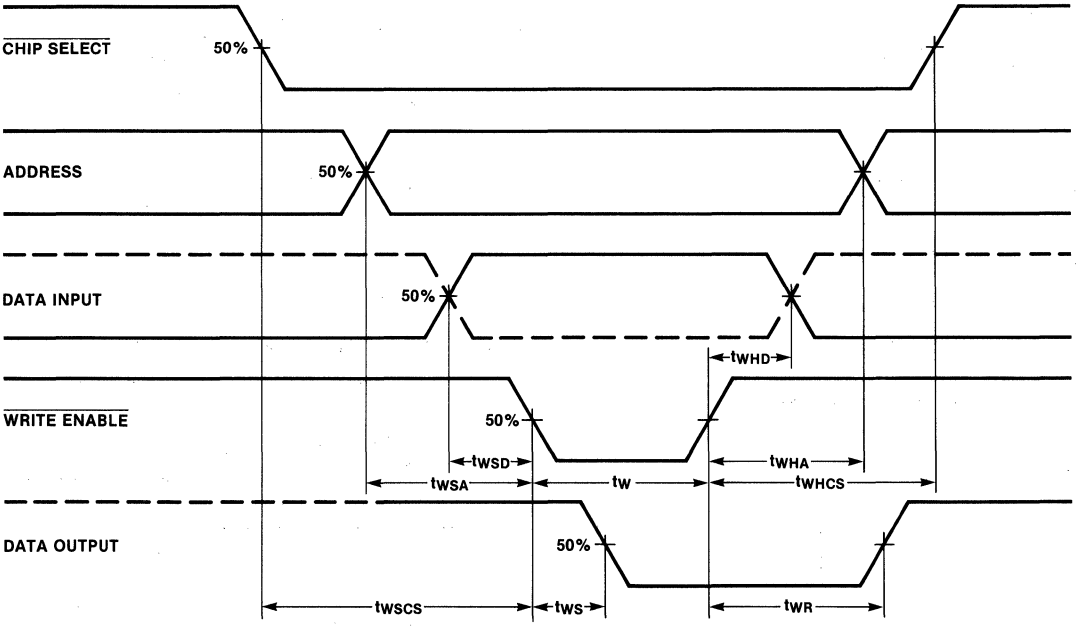
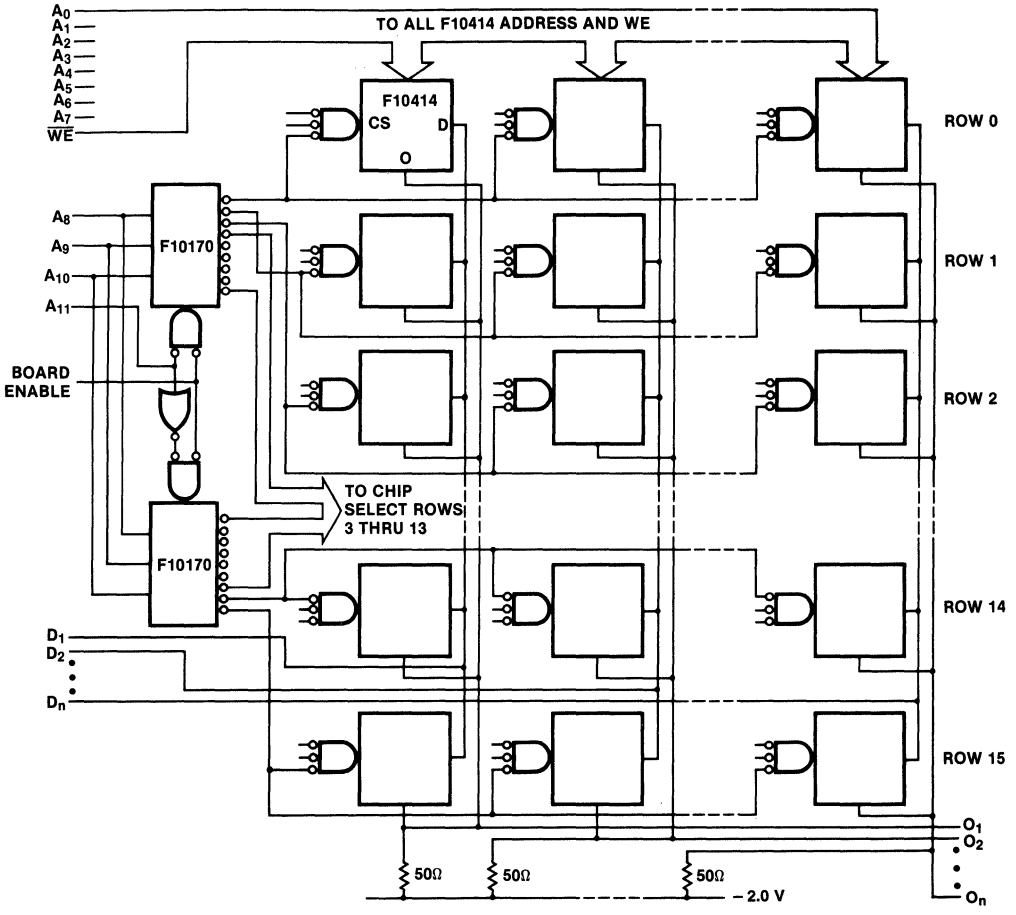
Fig. 4 Write Mode Timing



Note
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Typical Application

4096-Word x n-Bit System



F10415
1024 x 1-Bit Static Random Access Memory

F10K ECL Product

Description

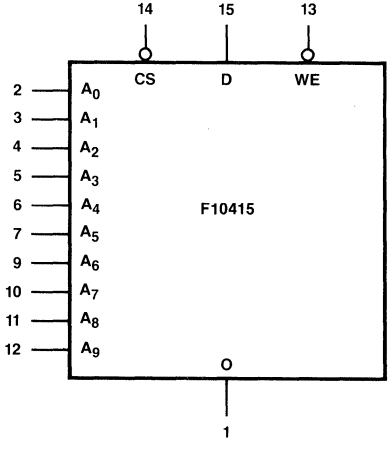
The F10415 is a 1024-bit read/write Random Access Memory (RAM), organized as 1024 words by one bit per word and designed for high-speed scratchpad, control and buffer storage applications. It is available in two speed versions, the F10415 and F10415A. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

- **Address Access Time**
  F10415-35 ns Max
  F10415A-20 ns Max
- **Chip Select Access Time**
  F10415-10 ns Max
  F10415A-8.0 ns Max
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation-0.5 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
A_0-A_9	Address Inputs
D	Data Input
O	Data Output

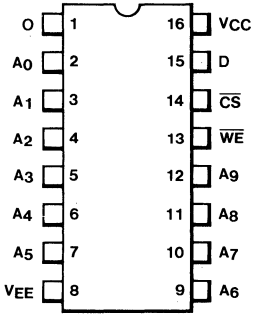
Logic Symbol



V_{CC} = Pin 16
V_{EE} = Pin 8

Connection Diagram

16-Pin DIP (Top View)

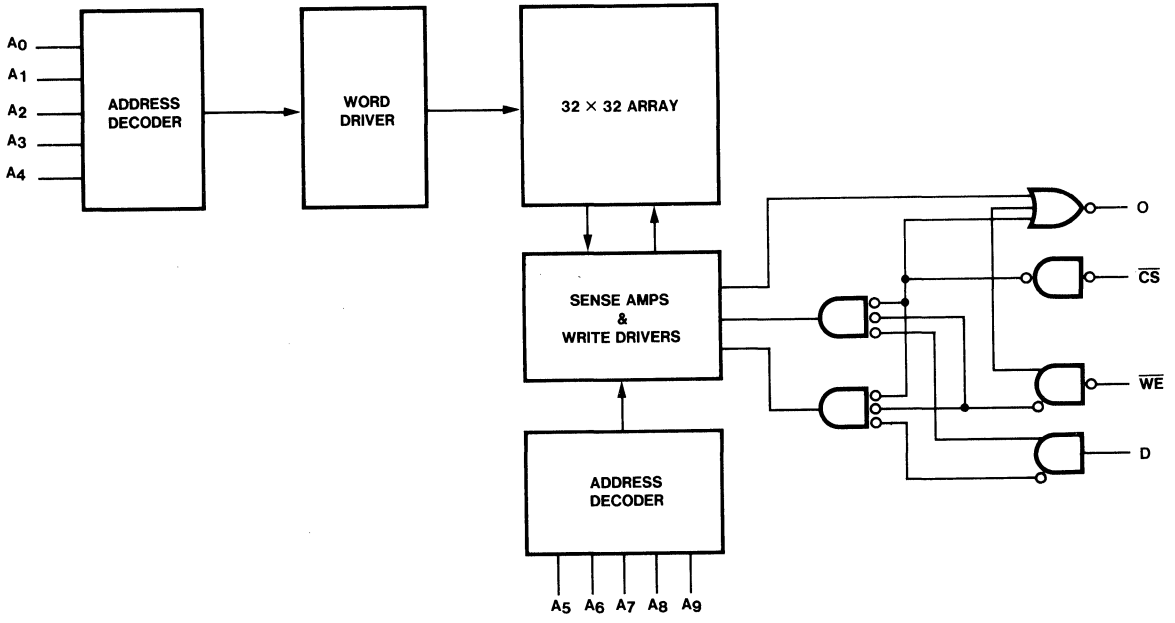


Note
The 16-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6D	DC
Plastic DIP	9B	PC
Flatpak	3L	FC

Logic Diagram



Functional Description

The F10415 is a fully decoded 1024-bit read/write random access memory, organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A_0 through A_9.

One Chip Select input is provided for memory array expansion up to 2048 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of Chip Select, ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the output (O).

The output of the F10415 is an unterminated emitter follower, which allows maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F10415 devices together to allow easy expansion. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output.

Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D	O	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

L = LOW Voltage Levels = −1.7 V (Nominal)
H = HIGH Voltage Levels = −0.9 V (Nominal)
X = Don't Care
Data = Previously stored data

DC Characteristics: V_{EE} = −5.2 V, V_{CC} = GND, T_A = 0°C to +75°C unless otherwise specified[1]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
I_{IH}	Input HIGH Current			220	μA	$V_{IN} = V_{IH(max)}$	
I_{IL}	Input LOW Current, $\overline{CS}$ $\overline{WE}$, A_0–A_9, D	0.5		170	μA	$V_{IN} = V_{IL(min)}$	
I_{EE}	Power Supply Current	−150	−105		mA	T_A = +75°C	Inputs and Output Open
			−90			T_A = 0° C	

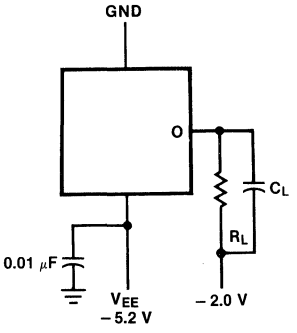
AC Characteristics: V_{EE} = −5.2 V ±5%, V_{CC} = GND, Output Load = 50 Ω and 30 pF to −2.0 V, T_A = 0°C to +75°C

Symbol	Characteristic	F10415 Min	F10415 Max	F10415A Min	F10415A Max	Unit	Condition	
	Read Timing							
t_{ACS}	Chip Select Access Time		10		8.0	ns		
t_{RCS}	Chip Select Recovery Time		10		8.0	ns	*Figures 3a, 3b*	
t_{AA}	Address Access Time[2]		35		20	ns		
	Write Timing							
t_W	Write Pulse Width to Guarantee Writing	25		14		ns	t_{WSA} = 8 ns (F10415), 5 ns (F10415A), *Figure 4*	Measured at 50% of Input to Valid Output ($V_{IL(max)}$ for V_{OL} or $V_{IH(min)}$ for V_{OH})
t_{WSD}	Data Setup Time prior to Write	5.0		4.0		ns		
t_{WHD}	Data Hold Time after Write	5.0		4.0		ns		
t_{WSA}	Address Setup Time prior to Write	8.0		5.0		ns	t_W = 25 ns (F10415), 14 ns (F10415A), *Figure 4*	
t_{WHA}	Address Hold Time after Write	4.0		3.0		ns		
t_{WSCS}	Chip Select Setup Time prior to Write	5.0		4.0		ns		
t_{WHCS}	Chip Select Hold Time after Write	5.0		4.0		ns		
t_{WS}	Write Disable Time		10		10	ns		
t_{WR}	Write Recovery Time		20		20	ns		

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r	Output Rise Time		5.0		ns	Measured between 20% and
t_f	Output Fall Time		5.0		ns	80% or 80% and 20%, *Figure 2*
C_{IN}	Input Pin Capacitance		4.0	5.0	pF	Measured with a Pulse
C_{OUT}	Output Pin Capacitance		7.0	8.0	pF	Technique

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Fig. 1 AC Test Circuit



Notes
All Timing Measurements Referenced to 50% of Input Levels
C_L = 30 pF including Fixture and Stray Capacitance
R_L = 50 Ω to −2.0 V.

Fig. 2 Input Levels

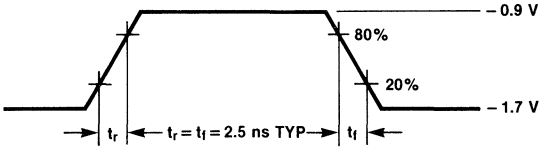
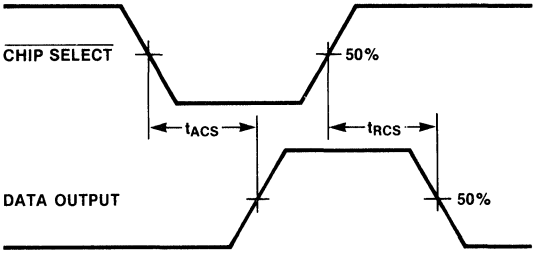


Fig. 3 Read Mode Timing

a Read Mode Propagation Delay from Chip Select



b Read Mode Propagation Delay from Address

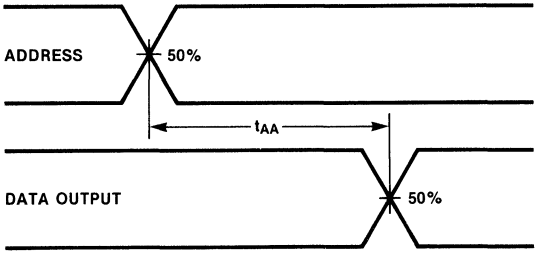


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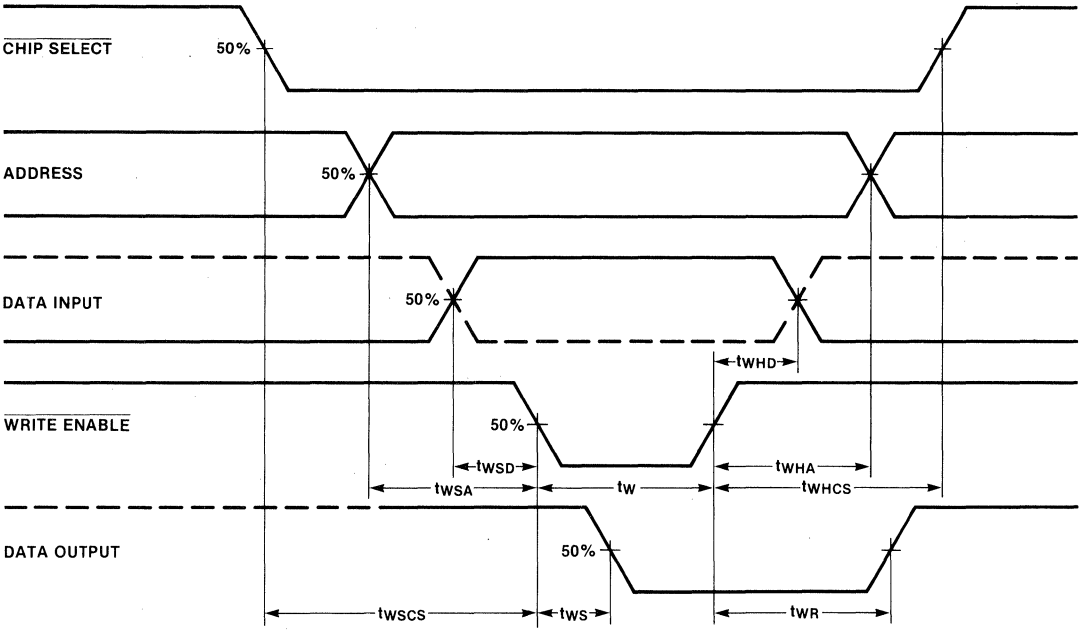
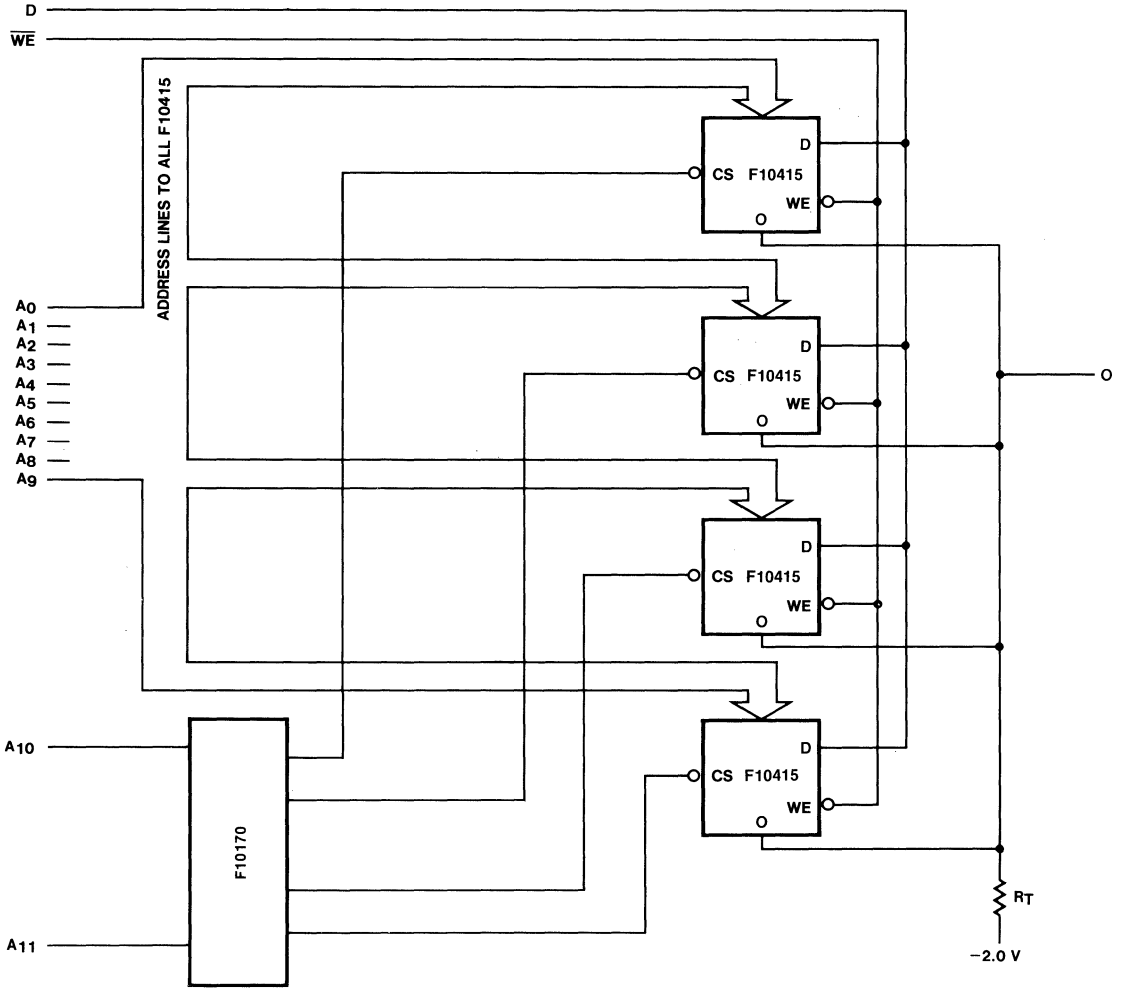
Fig. 4 Write Mode Timing



Note
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Typical Application

4096-Word x n-Bit System



F10416
256 x 4-Bit Programmable Read Only Memory

F10K ECL Product

Description

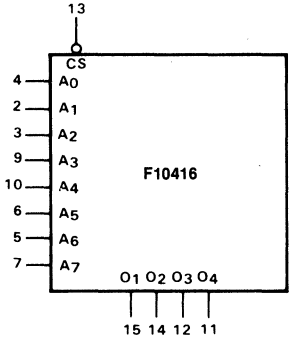
The F10416 is a 1024-bit field Programmable Read Only Memory (PROM), organized 256 words by four bits per word. It is designed for high-speed control, mapping, code conversion, and logic replacement. The device includes full on-chip address decoding, non-inverting Data output lines, and an active-LOW Chip Select line for easy memory expansion. The device is manufactured with all bits in the logic-HIGH state. Programmed bits will furnish LOW levels at corresponding outputs.

- **Address Access Time - 20 ns Max**
- **Chip Select Access Time - 8.0 ns Max**
- **Chip Select Input and Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation - 0.56 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{CS}$	Chip Select Input (Active LOW)
A_0-A_7	Address Inputs
O_1-O_4	Data Outputs

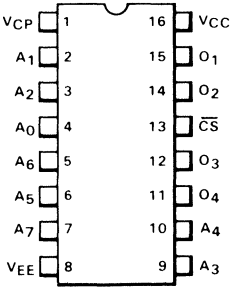
Logic Symbol



V_{CP} = Pin 1
V_{CC} = Pin 16
V_{EE} = Pin 8

Connection Diagram

16-Pin DIP (Top View)



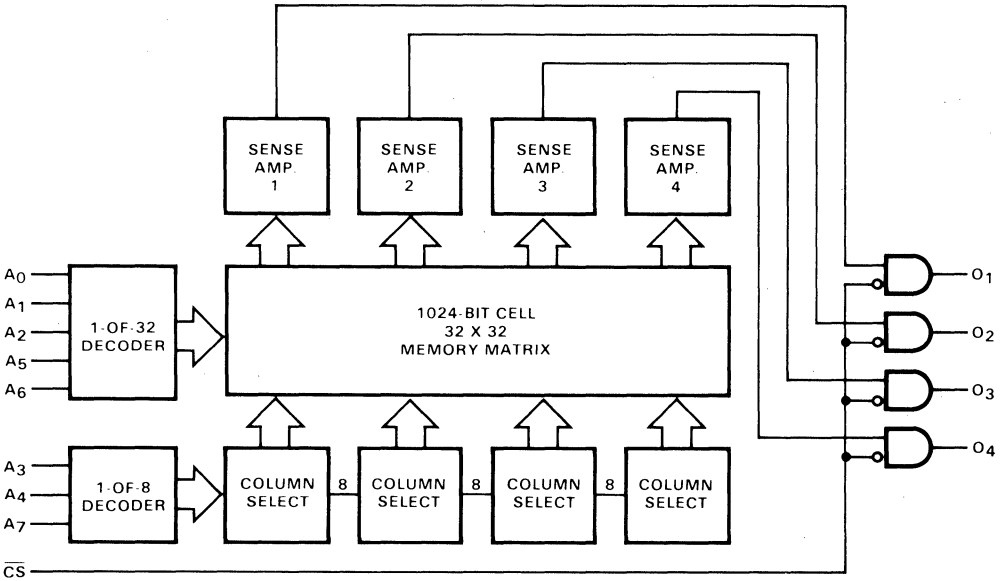
Notes

V_{CP} (Pin 1) is connected to the Programmer (+10.5 V) during programming only; otherwise, it should be grounded.
The Flatpak version has the same pinout (Connection Diagram) as the Dual In-line Package.

Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6D	DC
Plastic DIP	9B	PC
Flatpak	3L	FC

Logic Diagram



Functional Description

The F10416 is a fully decoded bipolar field programmable read only memory organized 256 words by four bits per word. An unterminated emitter-follower output is provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many F10416 devices can be tied together. An external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is off.

One Chip Select ($\overline{CS}$) input is provided for memory array expansion up to 512 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of $\overline{CS}$ from the address without increasing address access time. The device is enabled when $\overline{CS}$ is LOW. When the device is disabled ($\overline{CS}$ = HIGH), all outputs are forced LOW.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_7 inputs, the chip is selected and data is valid at the outputs after t_{AA}.

In the unprogrammed state the outputs are HIGH. To program LOW levels follow the procedure outlined in the *Programming Specifications* table.

Programming

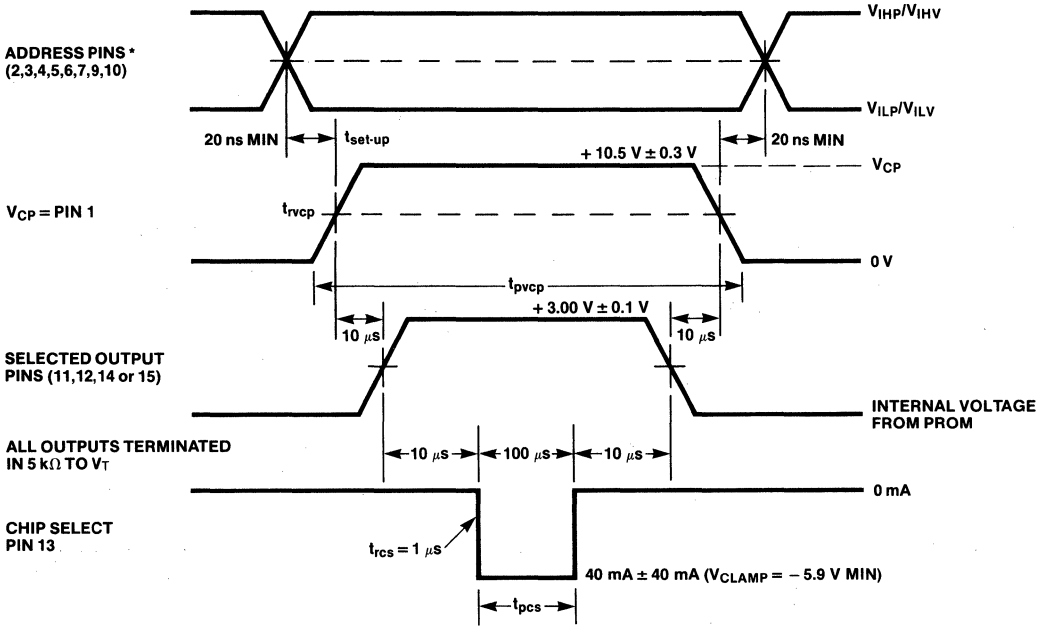
The F10416 is manufactured with all bits in the logic "1" state. Any desired bit (output) can be programmed to a logic "0" state by following the procedure shown below. One may build a programmer to satisfy the specifications or purchase any of the commercially available programmers which meet these specifications.

Programming Sequence

1. Apply power to the part: V_{CC} = pin 16 = GND; V_{EE} = pin 8 = −5.2 V ± 5%.
2. Terminate all outputs (pins 11, 12, 14 and 15) with 5 kΩ resistors to V_{TT} = −2.0 V. Note: all input pins, including $\overline{CS}$, have internal 50 kΩ pull-down resistors to V_{EE}.

3. Select the word to be programmed by applying the appropriate voltage levels, as shown in the *Programming Specifications* table, to the Address pins (2, 3, 4, 5, 6, 7, 9 and 10).
4. After the address levels are set raise V_{CP} = Pin 1 from 0 V to +10.5 V ± 0.3 V.
5. After V_{CP} has reached its HIGH level, select the bit to be programmed by applying a HIGH level of +3.0 V ± 0.1 V to the output associated with it, *i.e.,* pins 11, 12, 14 or 15. Only one bit (output) at a time may be selected for programming. Uncommitted outputs are terminated as outlined in 2.
6. After the HIGH level (+3.0 V) has been established at the selected output pin, source a current of −40 mA ± 4 mA out of the Chip Select input (pin 13) to program the selected bit; this applied current pulse which is 100 μs wide and has an approximate rise time of 1 μs is to be furnished by a current sink which clamps at V_{CLAMP} = −5.9 V.
7. To verify a LOW in the bit just programmed follow this sequence:
   (a) Remove current pulse from $\overline{CS}$ pin.
   (b) Remove applied voltage from selected output pin.
   (c) Lower V_{CP} from HIGH level to GND.
   (d) Keep same address but change its levels to normal ECL levels as outlined in the *Programming Specifications* table.
   (e) Enable the chip by applying a LOW level (V_{IL}) to $\overline{CS}$ (pin 13), or leave it open.
   (f) Sense the level at the selected output pin; a LOW level indicates successful programming whereas a HIGH level is a fail indication; in the latter case reprogramming of the bit can be attempted up to a maximum of eight times.
8. To program other bits in the memory repeat steps 3 through 7.

Programming Timing Sequence



*Input pins A_1 and A_7 cannot be lower than $V_{IL(min)}$.

Programming Specifications

Symbol	Characteristic	Min	Recommended Value	Max	Unit	Comment
V_{CC}	Power Supply		0		V	
V_{EE}		−5.46	−5.2	−4.94	V	
V_{TT}	Termination Voltage		−2.0		V	Applied to all outputs
V_{IH}	Chip Select (V_{CLAMP})	−0.1	0	+0.1	V	Max Current is 40 mA during programming
V_{IL}		−5.9	−5.2		V	
V_{IHP}	Address Input Threshold	−0.1	0	+0.1	V	Programming levels
V_{ILP}		−3.1	−3.0	−2.9	V	
V_{IHV}	Address Input Threshold	−0.88	−0.87	−0.86	V	Verify levels
V_{ILV}		−1.76	−1.75	−1.74	V	
V_{CP}	Program Setup Pulse	10.2	10.5	10.8	V	
V_{OP}	Programming Pulse	2.9	3.0	3.1	V	Applied to output to be programmed
I_{CS}	Chip Select Programming Current	36	40	44	mA	At V_{CLAMP} = −5.9 V Min on the Chip Select pin
t_{pcs}	Chip Select Programming Pulse	50	100	180	μs	
t_{rcs}	Chip Select Programming Pulse Rise Time	0.5	1.0	2.0	μs	
t_{pvcp}	V_{CP} Programming Pulse	90	140	220	μs	
t_{rvcp}	V_{CP} Programming Rise Time	0.5	1.0	2.0	μs	
t_{setup}	Setup Time	20			ns	Start time of V_{CP} pulse after address is selected

Guaranteed Operating Ranges

Part Number	Supply Voltage (V_{EE}) Min	Typ	Max	Ambient Temperature T_A
F10416XC	−5.46 V	−5.2 V	−4.94 V	−30°C to +85°C

X = Package Type

DC Characteristics: V_{EE} = −5.2 V, V_{CC} = GND, T_A = −30°C to +85°C unless otherwise specified[1]

Symbol	Characteristic	Min	Typ	Max	Unit	T_A	Condition	
V_{OH}	Output HIGH Voltage	−1060 −960 −890		−890 −810 −700	mV	−30°C +25°C +85°C	$V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$	Loading is 50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1890 −1850 −1825		−1675 −1650 −1615	mV	−30°C +25°C +85°C		
V_{OHC}	Output HIGH Voltage	−1080 −980 −910			mv	−30°C +25°C +85°C	$V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage			−1655 −1630 −1595	mV	−30°C +25°C +85°C		
V_{IH}	Input HIGH Voltage	−1205 −1105 −1035		890 810 700	mV	−30°C +25°C +85°C	Guaranteed HIGH signal for All Inputs	
V_{IL}	Input LOW Voltage	−1890 −1850 −1825		−1500 −1475 −1440	mV	−30°C +25°C +85°C	Guaranteed LOW signal for All Inputs	
I_{IH}	Input HIGH Current			200	μA	−30°C to +85°C	$V_{IN} = V_{IH(max)}$	
I_{IL}	Input LOW Current, $\overline{CS}$	0.5		150	μA	+25°C	$V_{IN} = V_{IL(min)}$	
I_{EE}	Power Supply Current	−140	−110		mA	+25°C	All Inputs and Outputs Open	

AC Characteristics: V_{EE} = −5.2 V ± 5%, V_{CC} = GND, Output Load 50 Ω to −2.0 V, T_A = −30°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_{AA}	Address Access Time[2]		11	20	ns	Measured at 50% Points of both Input and Output
t_{ACS}	Chip Select Access Time		4.0	8.0	ns	Measured at 50% Points of both Input and Output

1. See 10K Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

F10422
256 x 4-Bit Static Random Access Memory

F10K ECL Product

Description

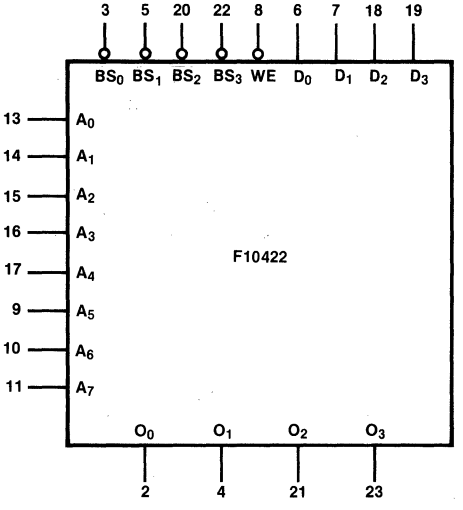
The F10422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits per word. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as four active-LOW Bit Select lines.

- **Address Access Time–10 ns Max**
- **Bit Select Access Time–5.0 ns Max**
- **Four Bits Can be Independently Selected**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation–0.92 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{BS_0}$–$\overline{BS_3}$	Bit Select Inputs (Active LOW)
A_0–A_7	Address Inputs
D_0–D_3	Data Inputs
O_0–O_3	Data Outputs

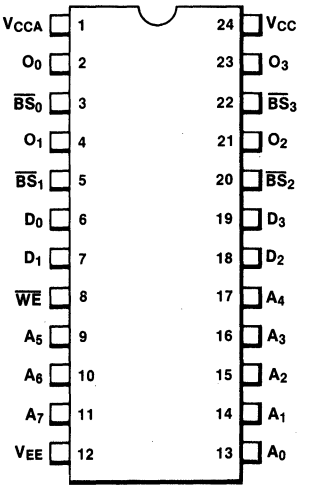
Logic Symbol



V_{CC} = Pin 24
V_{CCA} = Pin 1
V_{EE} = Pin 12

Connection Diagrams

24-Pin DIP (Top View)

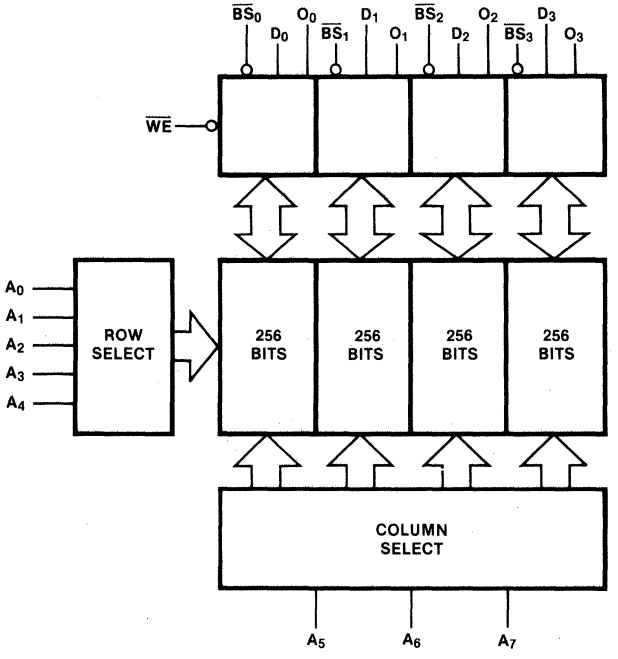


Note
The 24-pin flatpak version has the same pinout connections as the Dual In-Line package.

Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Logic Diagram



Functional Description

The F10422 is a fully decoded 1024-bit read/write random access memory, organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A_0 through A_7.

Four Bit Select inputs are provided for logic flexibility. For larger memories, the fast bit select access time permits the decoding of individual bit selects from the address without increasing address access time.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the bit selected, the data at $D_0 - D_3$ is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the bit selected. Non-inverted data is then presented at the output (O).

The outputs of the F10422 are unterminated emitter followers, which allow maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F10422 devices together to allow easy expansion. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output.

Truth Table

Inputs			Outputs	Mode
$\overline{BS_n}$	$\overline{WE}$	D_n	O_n	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

Each bit has independent $\overline{BS}$, D, and O, but all have common $\overline{WE}$.
L = LOW Voltage Levels = −1.7 V (Nominal)
H = HIGH Voltage Levels = −0.9 V (Nominal)
X = Don't Care
Data = Previously stored data

DC Characteristics: $V_{EE} = -5.2$ V, $V_{CC} = V_{CCA} = GND$, $T_A = 0°C$ to $+75°C$ unless otherwise specified[1]

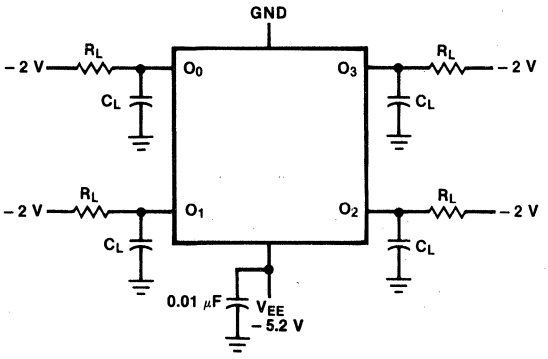
Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			220	μA	$V_{IN} = V_{IH(max)}$
I_{IL}	Input LOW Current, $\overline{BS_0}$-$\overline{BS_3}$ $\overline{WE}$, A_0-A_7, D_0-D_3	0.5 −50		170	μA	$V_{IN} = V_{IL(min)}$
I_{EE}	Power Supply Current	−230	−180		mA	All Inputs and Outputs Open

AC Characteristics: $V_{EE} = -5.2$ V ±5%, $V_{CC} = V_{CCA} = GND$, Output Load = 50 Ω and 30 pF to −2.0 V, $T_A = 0°C$ to $+75°C$

Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
	Read Timing						
t_{ABS}	Bit Select Access Time		3.0	5.0	ns		
t_{RBS}	Bit Select Recovery Time		3.0	5.0	ns	*Figures 3a, 3b*	
t_{AA}	Address Access Time[2]		7.0	10	ns		
	Write Timing						
t_W	Write Pulse Width to Guarantee Writing	7.0	5.0		ns	t_{WSA} = 1 ns	Measured at 50% of Input to Valid Output ($V_{IL(max)}$ for V_{OL} or $V_{IH(min)}$ for V_{OH})
t_{WSD}	Data Setup Time prior to Write	1.0	0		ns	*Figure 4*	
t_{WHD}	Data Hold Time after Write	2.0	0		ns		
t_{WSA}	Address Setup Time prior to Write	1.0	0		ns		
t_{WHA}	Address Hold Time after Write	2.0	0		ns		
t_{WSBS}	Bit Select Setup Time prior to Write	1.0	0		ns		
t_{WHBS}	Bit Select Hold Time after Write	2.0	0		ns	t_W = 7 ns *Figure 4*	
t_{WS}	Write Disable Time		3.0	5.0	ns		
t_{WR}	Write Recovery Time		6.0	12	ns		
t_r	Output Rise Time		3.0		ns	Measured between 20% and 80% or 80% and 20%, *Figure 2*	
t_f	Output Fall Time		3.0		ns		
C_{IN}	Input Pin Capacitance		4.0	5.0	pF	Measured with a Pulse Technique	
C_{OUT}	Output Pin Capacitance		7.0	8.0	pF		

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Fig. 1 AC Test Circuit



Notes
All Timing Measurements Referenced to 50% of Input Levels
C_L = 30 pF including Fixture and Stray Capacitance
R_L = 50 Ω to – 2.0 V.

Fig. 2 Input Levels

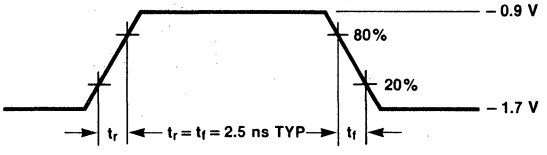
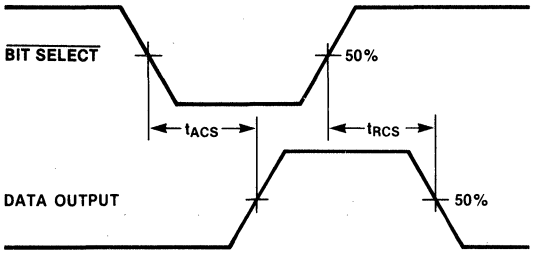


Fig. 3 Read Mode Timing

a Read Mode Propagation Delay from Bit Select



b Read Mode Propagation Delay from Address

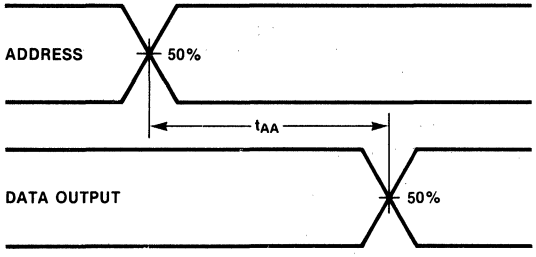
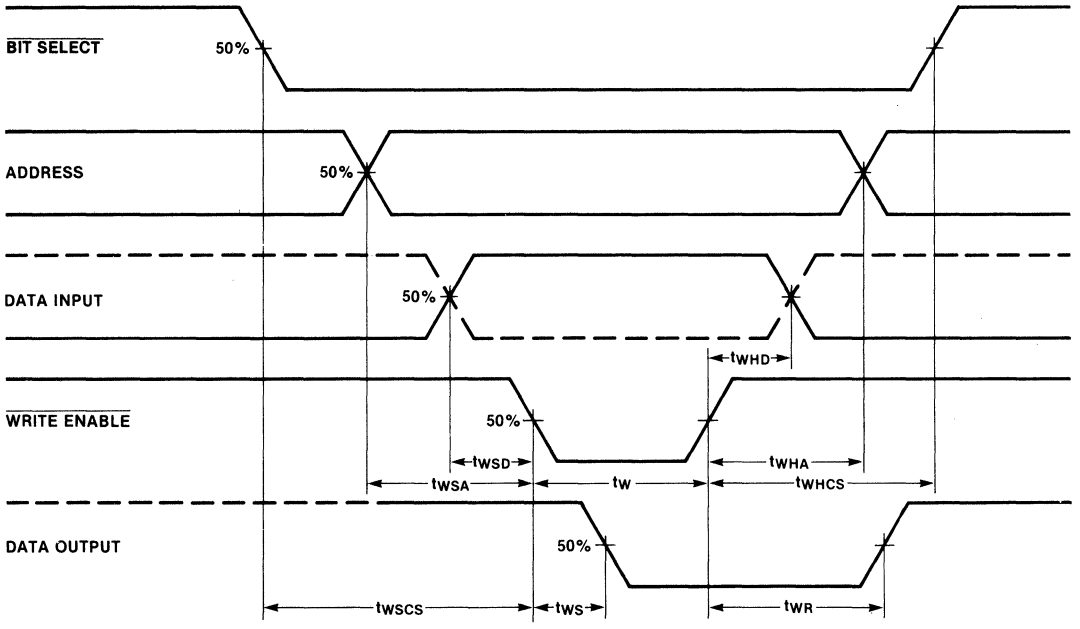


Fig. 4 Write Mode Timing



Note
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

F10470
4096 x 1-Bit Static Random Access Memory

F10K ECL Product

Description

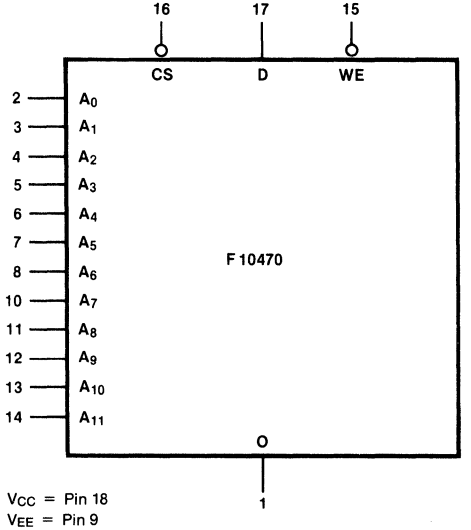
The F10470 is a 4096-bit read/write Random Access Memory (RAM), organized 4096 words by one bit per word and designed for high-speed scratchpad, control and buffer storage applications. It is available in two speed versions, the F10470 and F10470A. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

- **Address Access Time**
  F10470-35 ns Max
  F10470A-25 ns Max
- **Chip Select Access Time**
  F10470-15 ns Max
  F10470A-10 ns Max
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation-0.20 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
A_0-A_{11}	Address Inputs
D	Data Input
O	Data Output

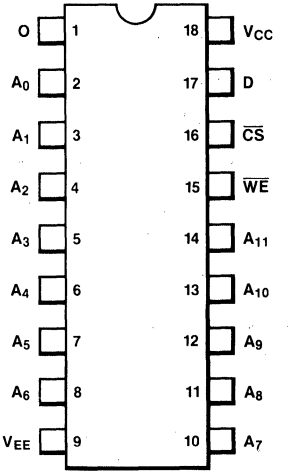
Logic Symbol



V_{CC} = Pin 18
V_{EE} = Pin 9

Connection Diagram

18-Pin DIP (Top View)

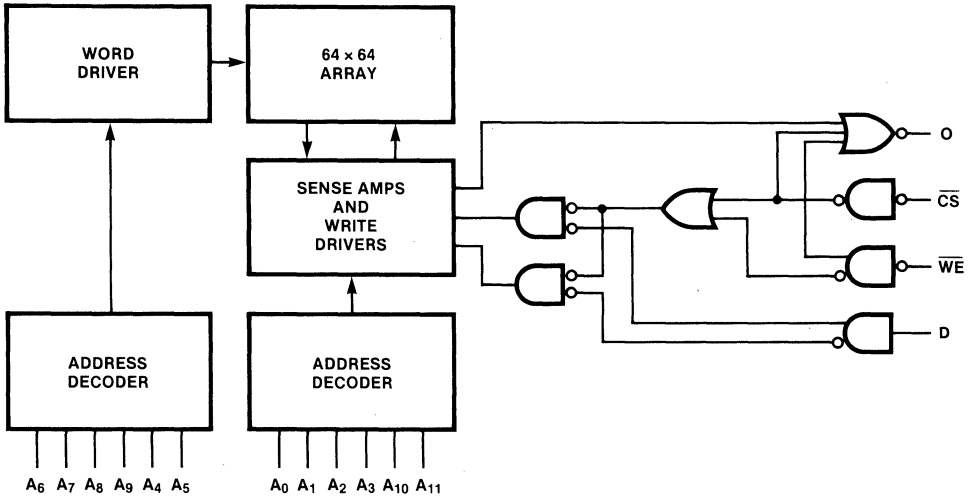


Note
The 18-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	8F	DC
Flatpak	3E	FC

Logic Diagram



Functional Description

The F10470 is a fully decoded 4096-bit read/write random access memory, organized 4096 words by one bit. Bit selection is achieved by means of a 12-bit address, A_0 through A_{11}.

One Chip Select input is provided for memory array expansion up to 8196 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of Chip Select, ($\overline{CS}$) from the address without increasing address access time.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the output (O).

The output of the F10470 is an unterminated emitter follower, which allows maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F10470 devices together. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is OFF.

Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D	O	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

L = LOW Voltage Levels = −1.7 V (Nominal)
H = HIGH Voltage Levels = −0.9 V (Nominal)
X = Don't Care
Data = Previously stored data

DC Characteristics: V_{EE} = −5.2 V, V_{CC} = GND, T_A = 0°C to +75°C unless otherwise specified[1]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
I_{IH}	Input HIGH Current			220	μA	$V_{IN} = V_{IH(max)}$	
I_{IL}	Input LOW Current, $\overline{CS}$ $\overline{WE}$, A_0-A_{11}, D	0.5 −50		170	μA	$V_{IN} = V_{IL(min)}$	
I_{EE}	Power Supply Current		−145		mA	T_A = 75°C	All Inputs and Output Open
		−200	−160			T_A = 0°C	

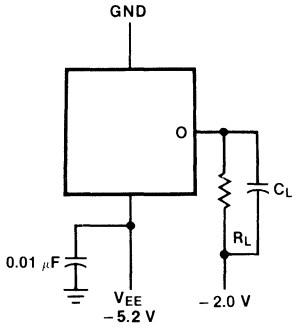
AC Characteristics: V_{EE} = −5.2 V ± 5%, V_{CC} = GND, Output Load = 50 Ω and 30 pF to −2.0 V, T_A = 0°C to +75°C

Symbol	Characteristic	F10470 Min	F10470 Max	F10470A Min	F10470A Max	Unit	Condition	
	Read Timing							
t_{ACS}	Chip Select Access Time		15		10	ns		
t_{RCS}	Chip Select Recovery Time		15		10	ns	*Figures 3a, 3b*	
t_{AA}	Address Access Time[2]		35		25	ns		
	Write Timing							
t_W	Write Pulse Width to Guarantee Writing	25		15		ns	t_{WSA} = 10 ns (F10470) and (F10470A), *Figure 4*	Measured at 50% of Input to Valid Output ($V_{IL(max)}$ for V_{OL} or $V_{IH(min)}$ for V_{OH})
t_{WSD}	Data Setup Time prior to Write	5.0		5.0		ns		
t_{WHD}	Data Hold Time after Write	5.0		5.0		ns		
t_{WSA}	Address Setup Time prior to Write	10		10		ns	t_W = 25 ns (F10470), 15 ns (F10470A), *Figure 4*	
t_{WHA}	Address Hold Time after Write	5.0		5.0		ns		
t_{WSCS}	Chip Select Setup Time prior to Write	5.0		5.0		ns		
t_{WHCS}	Chip Select Hold Time after Write	5.0		5.0		ns		
t_{WS}	Write Disable Time		15		15	ns		
t_{WR}	Write Recovery Time		20		20	ns		

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r	Output Rise Time		5.0		ns	Measured between 20% and
t_f	Output Fall Time		5.0		ns	80% or 80% and 20% *Figure 2*
C_{IN}	Input Pin Capacitance		4.0	5.0	pF	Measured with a Pulse
C_{OUT}	Output Pin Capacitance		7.0	8.0	pF	Technique

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a psuedorandom testing pattern.

Fig. 1 AC Test Circuit



Notes
All Timing Measurements Referenced to 50% of Input Levels
C_L = 30 pF including Fixture and Stray Capacitance
R_L = 50 Ω to −2.0 V.

Fig. 2 Input Levels

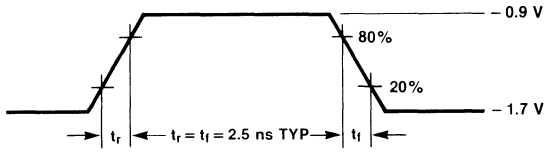
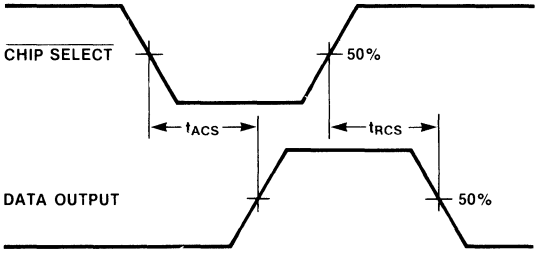
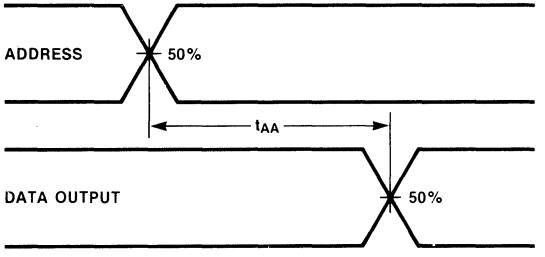


Fig. 3 Read Mode Timing

a Read Mode Propagation Delay from Chip Select

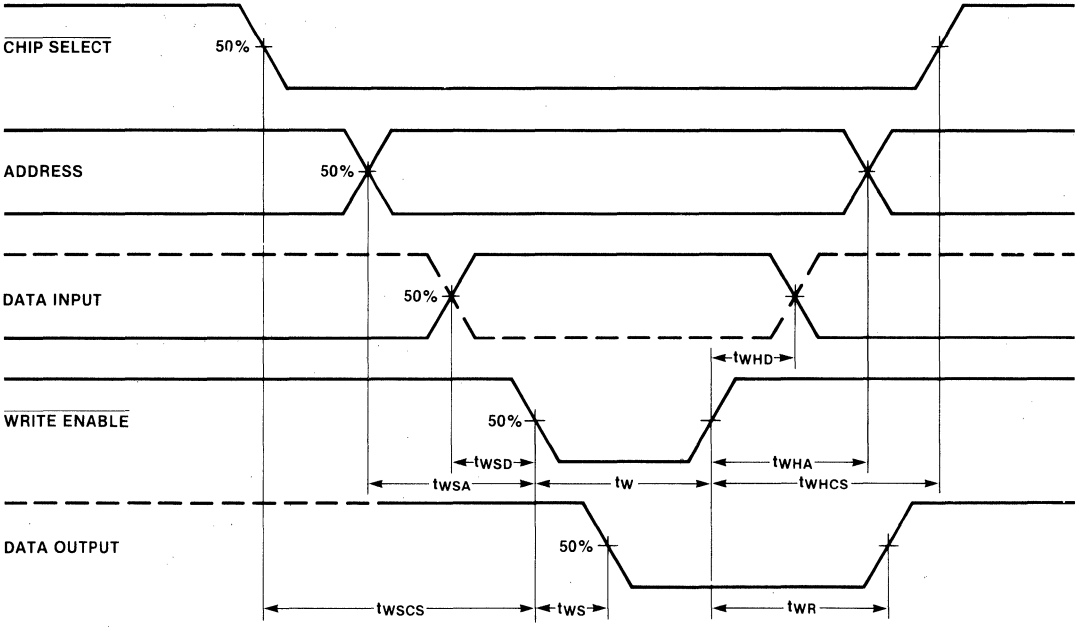


b Read Mode Propagation Delay from Address



4

Fig. 4 Write Mode Timing



Note
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

F10474
1024 x 4-Bit Static Random Access Memory

F10K ECL Product

Description

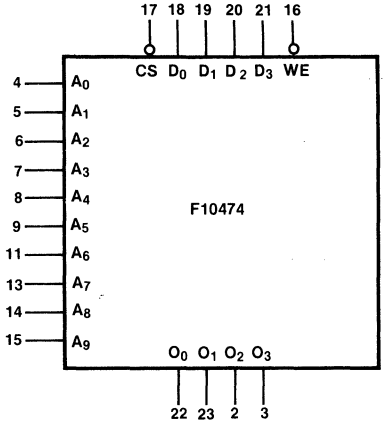
The F10474 is a 4096-bit read/write Random Access Memory (RAM), organized 1024 words by four bits per word. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

- **Address Access Time–25 ns Max**
- **Chip Select Access Time–15 ns Max**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation–0.20 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
A_0–A_9	Address Inputs
D_0–D_3	Data Inputs
O_0–O_3	Data Outputs

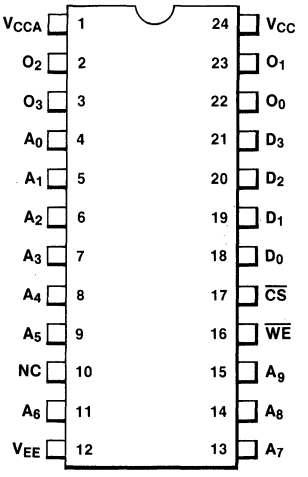
Logic Symbol



V_{CC} = Pin 24
V_{CCA} = Pin 1
V_{EE} = Pin 12
NC = Pin 10

Connection Diagram

24-Pin DIP (Top View)

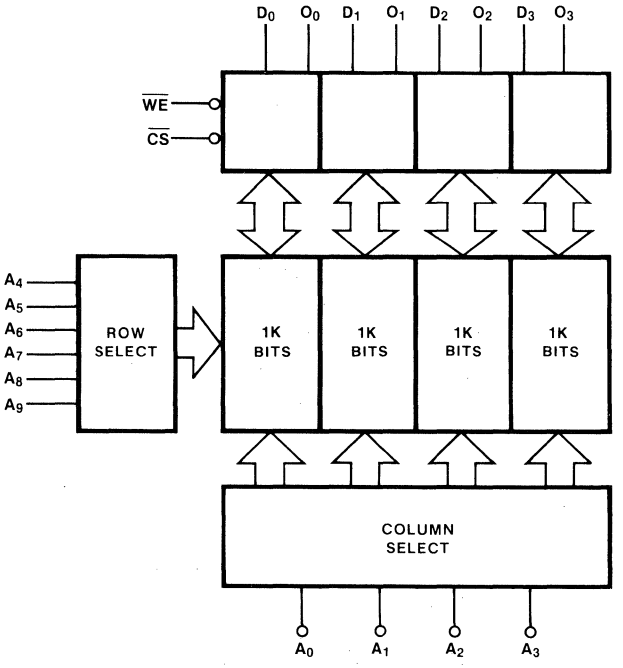


Note
The 24-pin flatpak version has the same pinout connections as the Dual In-Line package.

Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Logic Diagram



Functional Description

The F10474 is a fully decoded 4096-bit read/write random access memory, organized 1024 words by four bits. Word selection is achieved by means of a 10-bit address, A_0 through A_9.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D_0-D_3 is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the outputs (O_0-O_3).

The outputs of the F10474 are unterminated emitter followers, which allow maximum flexibility in output connection configurations. In many applications such as memory expansion, the outputs of many F10474 devices can be tied together. In other applicatons the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is OFF.

Truth Table

Inputs			Outputs	Mode
$\overline{CS}$	$\overline{WE}$	D_n	O_n	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

L = LOW Voltage Levels = −1.7 V (Nominal)
H = HIGH Voltage Levels = −0.9 V (Nominal)
X = Don't Care
Data = Previously stored data

DC Characteristics: $V_{EE} = -5.2\ V \pm 5\%$, $V_{CC} = V_{CCA} = GND$, $T_A = 0°C$ to $+75°C$ unless otherwise specified[1]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			220	μA	$V_{IN} = V_{IH(max)}$
I_{IL}	Input LOW Current, $\overline{CS}$ $\overline{WE}$, A_0-A_{11}, D	0.5 −50		170	μA	$V_{IN} = V_{IL(min)}$
I_{EE}	Power Supply Current	−200	−160		mA	Inputs and Outputs Open

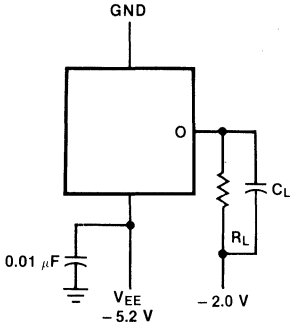
4

AC Characteristics: $V_{EE} = -5.2\ V \pm 5\ V$, $V_{CC} = V_{CCA} = GND$, Output Load = 50 Ω and 30 pF to −2.0 V, $T_A = 0°C$ to 75°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
	Read Timing						
t_{ACS}	Chip Select Access Time		10	15	ns		
t_{RCS}	Chip Select Recovery Time		10	15	ns	*Figures 3a, 3b*	
t_{AA}	Address Access Time[2]		20	25	ns		
	Write Timing						
t_W	Write Pulse Width to Guarantee Writing	16	10		ns	t_{WSA} = 10 ns	Measured at 50% of Input to Valid Output ($V_{IL(max)}$ for V_{OL} or $V_{IH(min)}$ for V_{OH})
t_{WSD}	Data Setup Time prior to Write	5.0	1.0		ns	*Figure 4*	
t_{WHD}	Data Hold Time after Write	5.0	1.0		ns		
t_{WSA}	Address Setup Time prior to Write	10	3.0		ns	t_W = 16 ns	
t_{WHA}	Address Hold Time after Write	4.0	1.0		ns		
t_{WSCS}	Chip Select Setup Time prior to Write	5.0	1.0		ns		
t_{WHCS}	Chip Select Hold Time after Write	5.0	1.0		ns	*Figure 4*	
t_{WS}	Write Disable Time		6.0	15	ns		
t_{WR}	Write Recovery Time		8.0	20	ns		
t_r	Output Rise Time		5.0		ns	Measured between 20% and 80% or 80% and 20%, *Figure 2*	
t_f	Output Fall Time		5.0		ns		
C_{IN}	Input Pin Capacitance		4.0	5.0	pF	Measured with a Pulse Technique	
C_{OUT}	Output Pin Capacitance		7.0	8.0	pF		

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Fig. 1 AC Test Circuit



Notes
All Timing Measurements Referenced to 50% of Input Levels
C_L = 30 pF including Fixture and Stray Capacitance
R_L = 50 Ω to –2.0 V.

Fig. 2 Input Levels

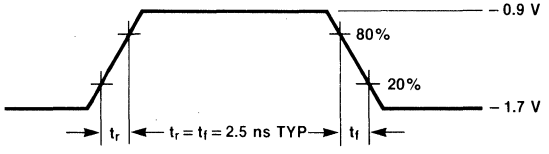
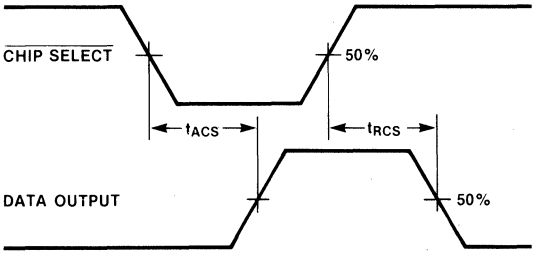


Fig. 3 Read Mode Timing

a Read Mode Propagation Delay from Chip Select



b Read Mode Propagation Delay from Address

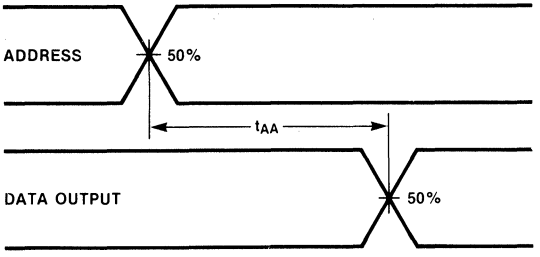
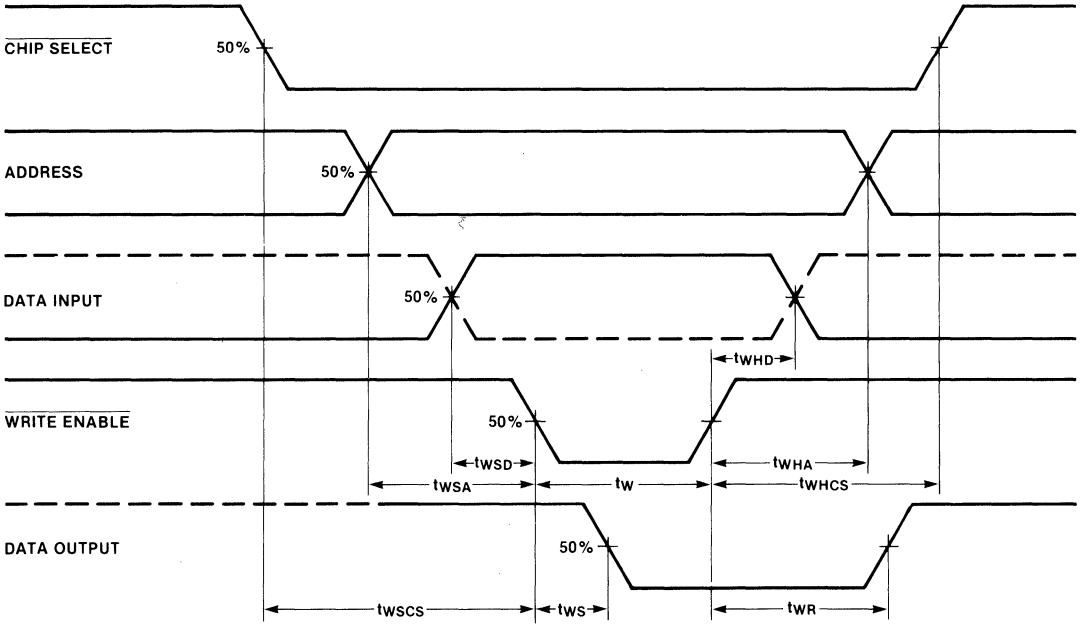
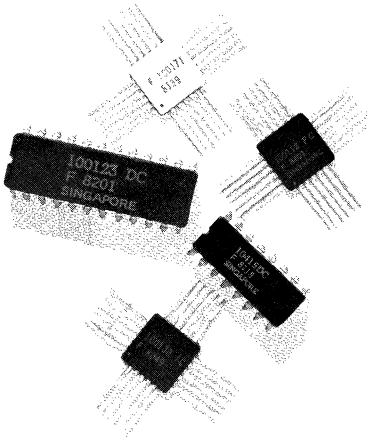


Fig. 4 Write Mode Timing



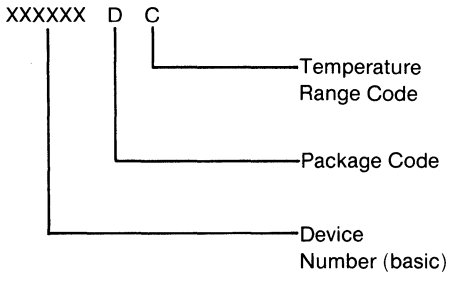
Note
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.



Chapter 5

Ordering Information/ Package Outlines

Specific ordering codes are listed on each data sheet in Chapters 3 and 4. The Product Index and Selection Guide given in Chapter 1 list only the "basic device numbers." This basic number is used to form part of a simplified purchasing code where the package type is defined as follows:



Temperature Range — One basic temperature grade is specified in this databook:

C = Commercial
0°C to +85°C

Package Code — One letter represents the basic package type. Different package outlines exist within each package type to accommodate varying die sizes and number of pins, as indicated below:

D — Ceramic/Hermetic Dual In-line
4J, 6D, 6Y, 8F

F — Flatpak
3E, 3L, 4Q, 4V

P — Plastic Dual In-line
9B

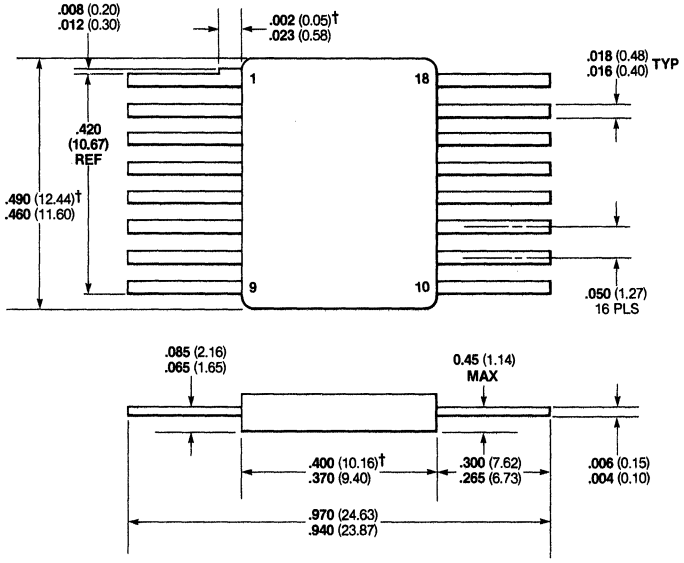
Package Outlines — The package outlines indicated by the codes above are shown in the detailed outline drawings in this section.

Thermal Resistance (Typical)

Package Styles	θ_{JC} (°C/W) Fluid Bath	θ_{JA} (°C/W) Still Air
3L	18	164
4J	14	78
4Q	8	140
4V	35	190
6D	15	82
6Y	25	75
9B	41	118

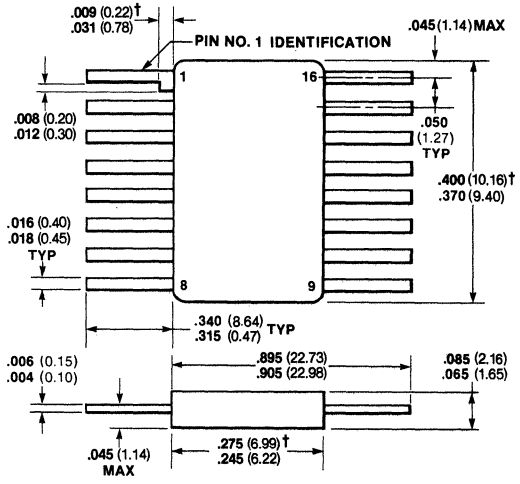
5

3E 18-Pin Cerpak



Notes
Pins are tin-plated alloy 42 or equivalent
Cap and base are black alumina (AL_2O_3).
Package weight is 0.9 Grams.
†These dimensions include misalignment, glass overrun, *etc.*...

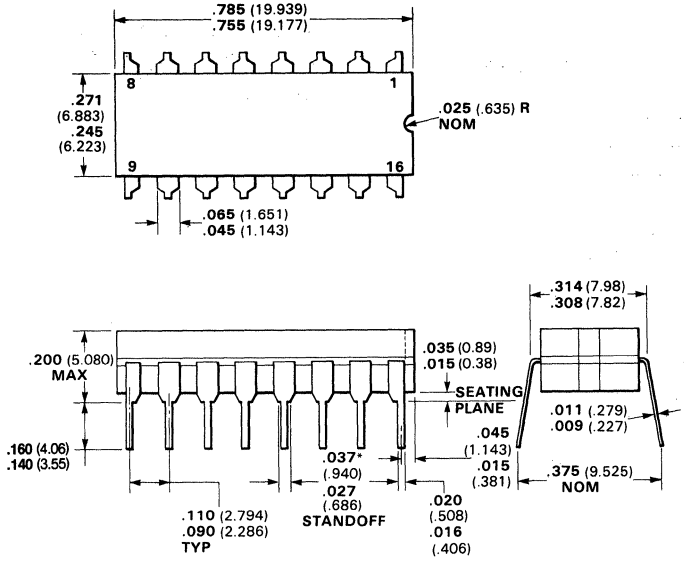
3L 16-Pin Cerpak



Notes
Pins are tin-plated alloy 42 or equivalent
Cap and base are black alumina (AL_2O_3).
Package weight is 0.5 Grams.
†These dimensions include misalignment, glass over-run, *etc.*...

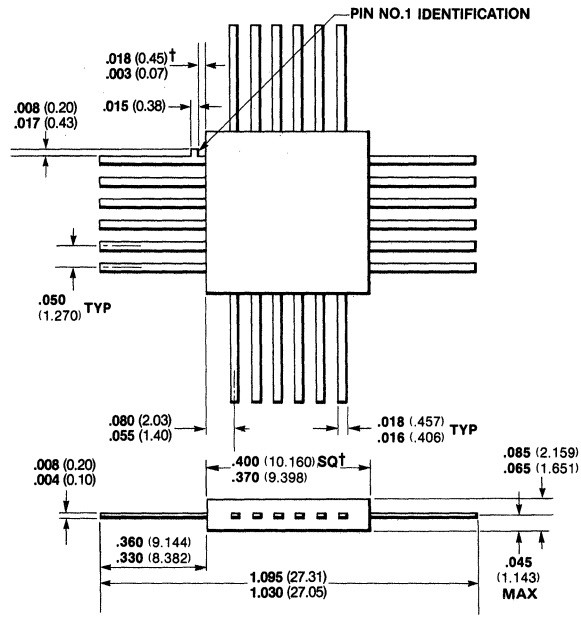
All dimensions in inches **bold** and millimeters (parentheses).

4J 16-Pin Ceramic DIP



Notes
Pins are tin-plated alloy 42 or equivalent.
Pins are intended for insertion in hole rows on **.300** (7.62) centers.
Pins are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for **.020** (0.51) diameter pin.
Hermetically sealed alumina package.
*The **.037**–**.027** (0.94–0.69) dimension does not apply to the corner pins.
Package weight is 1.0 grams.

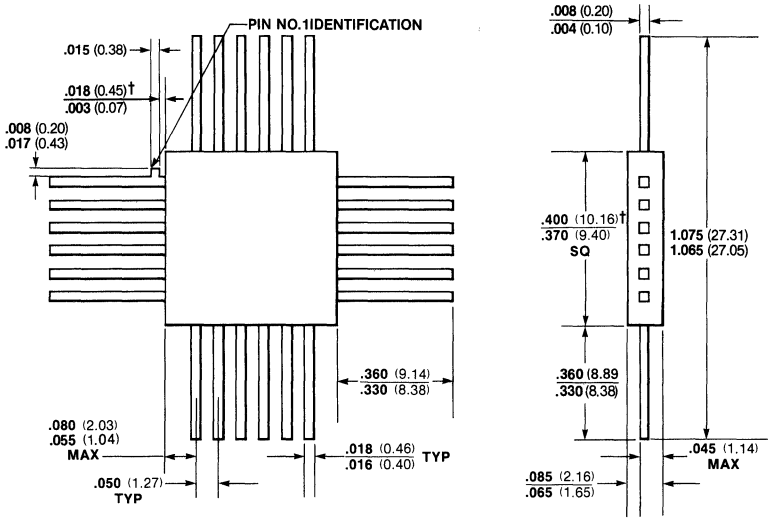
4Q 24-Pin Quad Cerpak



Notes
Pins are tin-plated alloy 42 or equivalent.
Base is BeO and cap is alumina (white).
Package weight is 0.7 grams.
†This dimension includes misalignment, glass over-run, etc....

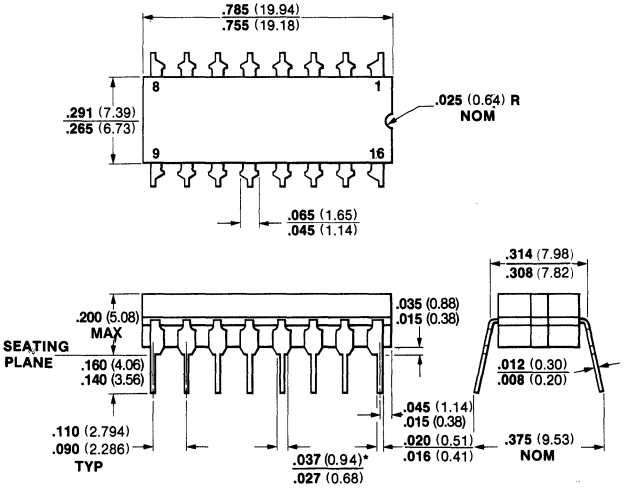
All dimensions in inches **bold** and millimeters (parentheses).

4V 24-Pin Quad Cerpak



Notes
Pins are tin-plated alloy 42 or equivalent.
Base and cap is alumina (black).
Package weight is 0.7 grams.
†This dimension includes misalignment, glass over-run, etc....

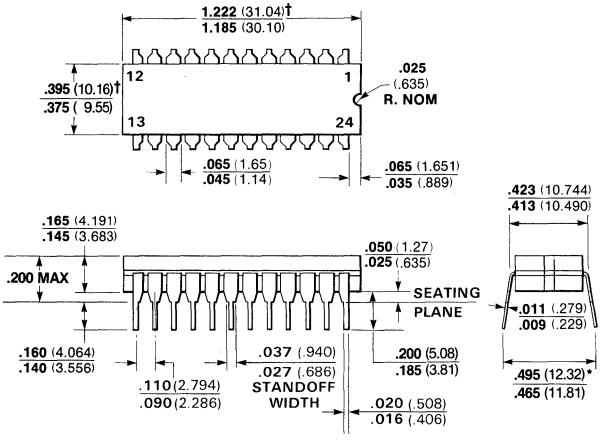
6D 16-Pin Vitreous Glass MSI DIP



Notes
Pins are tin-plated kovar or nickel alloy 42.
Pins are intended for insertion in hole rows on **.300** (7.62) centers.
Pins are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for **.030** (0.76) diameter pins.
Hermetically sealed alumina package (black).
*The **.037-.027** (0.94-0.68) dimension does not apply to the corner pins.
Package weight is 2.2 grams.

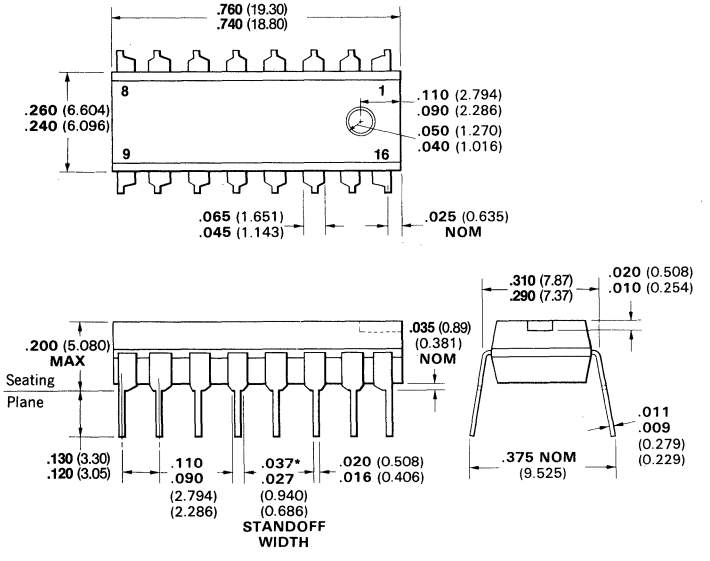
All dimensions in inches **bold** and millimeters (parentheses).

6Y 24-Pin Ceramic DIP



Notes
Pins are tin-plated alloy 42 or equivalent.
Package material is alumina.
Pins are intended for insertion in rows on **.400** (10.16) centers.
Pins are purposely shipped with "positive" misalignment to facilitate insertion.
Package weight is 5.0 grams.
†*These dimensions include misalignment, glass over-run, etc....*
††This dimension is measured from CL to CL of pins.

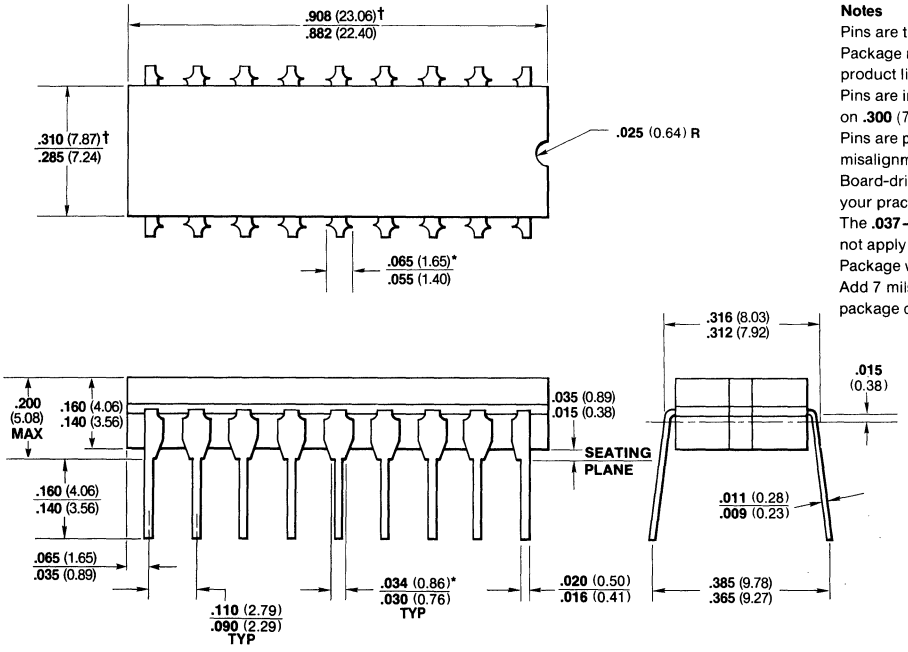
8F 18-Pin Ceramic DIP (LSI)



Notes
Pins are tin-plated alloy 42 or equivalent.
Pins are intended for insertion in hole rows on **.300** (7.62) centers.
Pins are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimeensions should equal your practice for **.030** (.762) diameter holes.
Hermetically sealed alumina package.
*Does not apply to the corner pins.
Package weight is 2.7 grams.
†This dimension includes misalignment, glass over-run, etc....

All dimensions in inches **bold** and millimeters (parentheses).

9B 16-Pin Plastic DIP

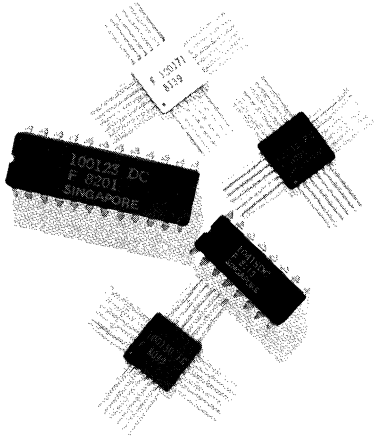


Notes

Pins are tin-plated alloy 42 or equivalent.
Package material varies depending on the product line.
Pins are intended for insertion in hole rows on **.300** (7.62) centers.
Pins are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for **.020** (0.51) diameter pin.
The **.037-.027** (0.94-0.69) dimension does not apply to the corner pins.
Package weight is 1.0 grams.
Add 7 mils flash on all sides to maximum package dimensions.

5

All dimensions in inches **bold** and millimeters (parentheses).



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*Field Application Engineer

F100K DC Family Specification

DC Characteristics: V_{EE} = −4.5 V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, Note 3

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions[4]	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mv	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(min)}$	

DC Characteristics: V_{EE} = −4.2 V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, Note 3

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions[4]	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1810		−1605	mV		
V_{OHC}	Output HIGH Voltage	−1030			mv	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage			−1595	mV		
V_{IH}	Input HIGH Voltage	−1150		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(min)}$	

DC Characteristics: V_{EE} = −4.8 V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, Note 3

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions[4]	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50 Ω to −2.0 V
V_{OL}	Output LOW Voltage	−1830		−1620	mV		
V_{OHC}	Output HIGH Voltage	−1045			mv	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(min)}$	

1. Unless specified otherwise on individual data sheet.
2. Parametric values specified at −4.2 V to −4.8 V.
3. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

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