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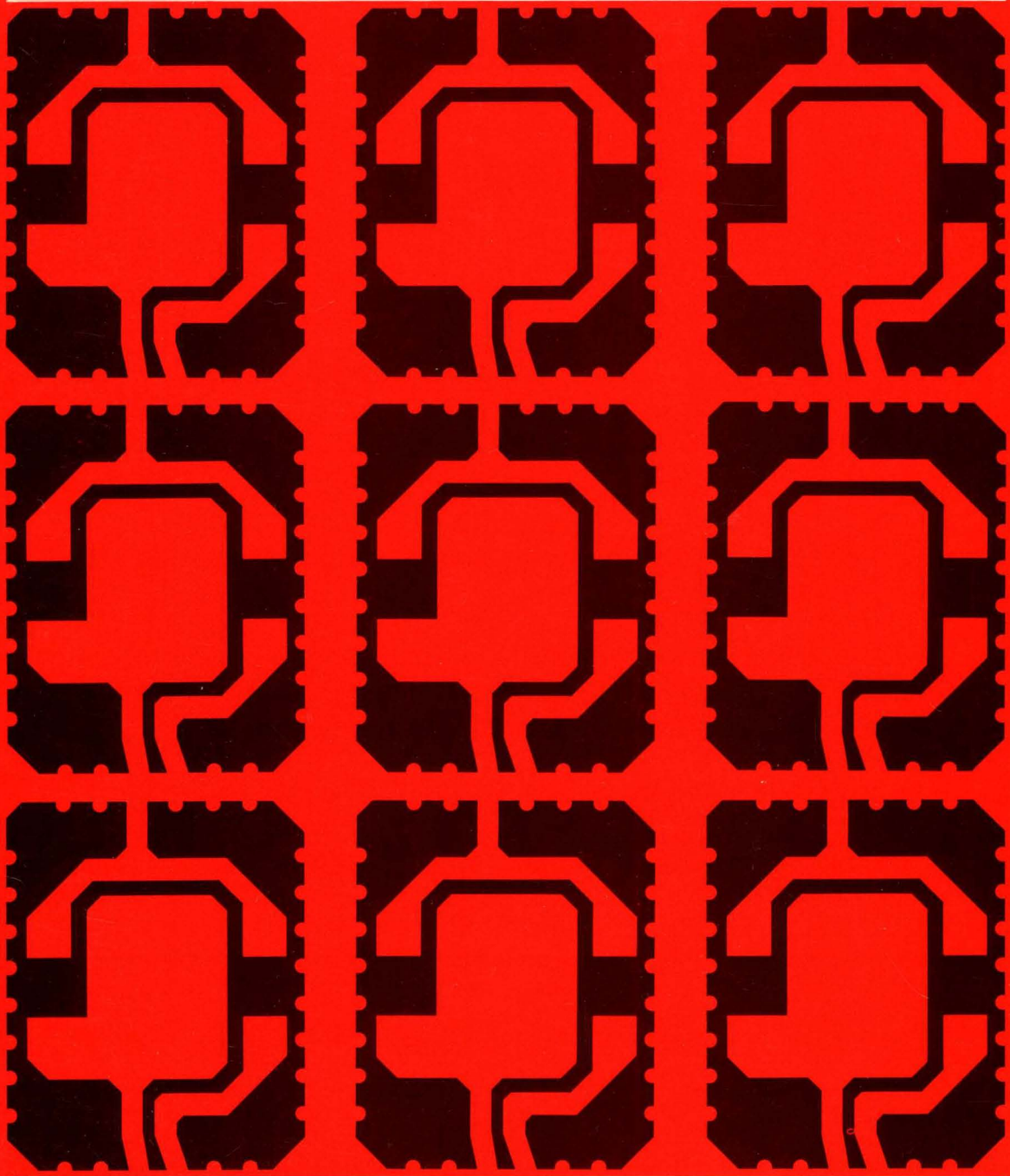
# Bipolar Memory Data Book

1983

Bipolar Division



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# Bipolar Memory Data Book

Bipolar Division


Bipolar Division
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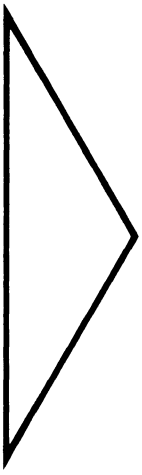


# Numerical Index of Devices

# Selection Guide

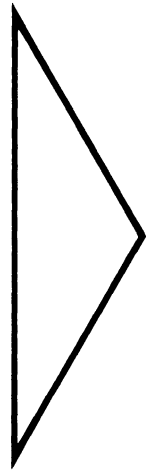
**ECL PROM/Programmable Logic Cross Reference**

| ECL PROMS | Size | Organization | $T_{AA}$ Max | Motorola | National | Signetics |
|---|---|---|---|---|---|---|
| **Ni Cr Fuses** | | | | | | |
| F10416 | 1024 | 256 x 4 | 20 | 10149 | 10416 | 10149 |
| F100416 | 1024 | 256 x 4 | 20 | | | 100149 |
| **ISO-Z Fuses** | | | | | | |
| F10Z416 | 1024 | 256 x 4 | 9 Typ | | | |
| F100Z416 | 1024 | 256 x 4 | 9 Typ | | | |
| **ECL Programmable Logic** | | | | | | |
| **ISO-Z Fuses** | | | | | | |
| F10Z459 | — | 16 x 24 x (8 + $\overline{8}$) FPLA | 4.0 | | | |
| F100Z459 | — | 16 x 24 x (8 + $\overline{8}$) FPLA | 4.0 | | | |

**TTL PROM/Programmable Logic Availability Guide and Cross Reference**

| TTL PROMS | Size | Organization | Output | $T_{AA}$ Max Comm/Mil | AMD | Fujitsu |
|---|---|---|---|---|---|---|
| **Ni Cr Fuse** | | | | | | |
| 93453 | 4096 | 1K x 4 | TS | 40/55 | Am27S33 | MB7122 |
| **ISO-Z Fuses** | | | | | | |
| 93Z450 | 8192 | 1K x 8 | OC | 40/55 | Am27S180 | |
| 93Z450A | 8192 | 1K x 8 | OC | 35/45 | | |
| 93Z451 | 8192 | 1K x 8 | TS | 40/55 | Am27S181 | MB7132 |
| 93Z451A | 8192 | 1K x 8 | TS | 35/45 | | |
| 93Z510 | 16,384 | 2K x 8 | OC | 45/55 | Am27S190 | |
| 93Z510 | 16,384 | 2K x 8 | TS | 45/55 | Am27S191 | MB7138 |
| 93Z564 | 65,536 | 8K x 8 | OC | 55/65 | | MB7143 |
| 93Z564A | 65,536 | 8K x 8 | OC | 45/55 | | |
| 93Z565 | 65,536 | 8K x 8 | TS | 55/65 | | MB7144 |
| 93Z565A | 65,536 | 8K x 8 | TS | 45/55 | | |
| **TTL Programmable Logic** | | | | | | |
| **Ni Cr Fuses** | | | | | | |
| 93458 | — | 16 x 48 x 8 FPLA | OC | 45/65 | | |
| 93459 | — | 16 x 48 x 8 FPLA | TS | 45/65 | | |

| Harris | Intel | MMI | National | Raytheon | Signetics | TI |
|---|---|---|---|---|---|---|
| HM7643 | 3625 | 53/6353 | DM54/74S573 | 29641 | N/S82S137 | TBP24S41 |
| HM7680 | 3608 | 53/6380 | DM77/87S180 | 29630 | N/S82S180 | TBP285SA86 |
| HM7681 | 3628<br>3628B | 53/6381 | DM77/87S181 | 29631 | N/S82S181 | TBP28S86 |
| HM76160 | 3616 | | DM77/87S190 | 29680 | N/S82S190 | |
| HM76161 | 3636 | | DM77/87S191 | 29681 | N/S82S191 | TBP28S166 |
| HM76641 | | | | | | |
| | | | | | N/S82S101<br>N/S82S100 | |



# Quality Assurance and Reliability

**Introduction**
All Fairchild Bipolar Division Products are manufactured to strict quality and reliability standards. Product conformance to these standards is insured by careful monitoring of the following functions: (1) incoming quality inspection, (2) process quality control, (3) quality assurance, and (4) reliability.

**Incoming Quality Inspection**
Purchased piece parts and raw materials must conform to purchase specifications. Major monitoring programs are the inspection of package piece parts, inspection of raw silicon wafers, and inspection of bulk chemicals and materials. Two other important functions of incoming quality inspection are to provide real-time feedback to vendors and in-house engineering, and to define and initiate quality improvement programs.

*Package Piece Parts Inspection*
Each shipment of package piece parts is inspected and accepted or rejected based on AQL sampling plans. Inspection tests include both inherent characteristics and functional use tests. Inherent characteristics include physical dimensions, color, plating quality, material purity, and material density. Functional use tests for various package piece parts include die attach, bond pull, seal, lid torque, salt atmosphere, lead fatigue, solderability, and mechanical strength. In these tests, the piece parts are sent through process steps that simulate package assembly. The units are then destructively tested to determine whether or not they meet the required quality and reliability levels.

*Silicon Wafer Inspection*
Each shipment of raw silicon wafers is accepted or rejected based on AQL sampling plans. Raw silicon wafers are subjected to non-destructive and destructive tests. Included in the testing are flatness, physical dimensions, resistivity, oxygen and carbon content, and defect densities. The test results are used to accept or reject the lot.

*Bulk Chemical and material Inspection*
Bulk chemicals and materials play an important role in any semiconductor process. To insure that the bulk chemicals and materials used in processing Fairchild wafers are the highest quality, they are stringently tested for trace impurities and particulate or organic contamination. Mixtures are also analized to verify their chemical make-up.

Incoming inspection is only the first step in determining the acceptability of bulk chemicals and materials. After acceptance, detailed documentation is maintained to correlate process results to various vendors and to any variations found in mixture consistency.

**Process Quality Control**
Process quality is maintained by establishing and maintaining effective controls for monitoring the wafer fabrication process, reporting the results of the monitors, and initiating valid measurement techniques for improving quality and reliability levels.

*Methods of Control*
The process quality control program utilizes the following methods of control: (1) process audits, (2) environmental monitors, (3) process monitors, (4) lot acceptance inspections, (5) process qualifications, and (6) process integrity audits. These methods of control, defined below, characterize visually and electrically the wafer fabrication operation.

Process Audit — Audits concerning manufacturing operator conformance to specification. These are performed on all operations critical to product quality and reliability.

Environmental Monitor — Monitors concernig the process environment, *i.e.*, water purity, air temperature/humidity, and particulate count.

Process Monitor — Periodic inspection at designated process steps for verification of manufacturing inspection and maintenance of process average. These inspections provide both attribute and variables data.

Lot Acceptance — Lot by lot sampling. This sampling method is reserved for those operations deemed as critical and, as such, requiring special attention.

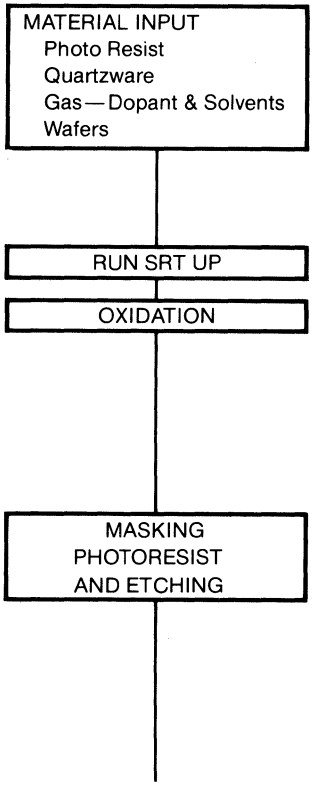
Process Qualification — Complete distributional analysis is run to specified tolerance averages and standard deviations. These qualifications are typically conducted on deposition and evaporation processes, *i.e.*, epi, aluminum, vapox, and backside gold.

Process Integrity Audit — Special audits conducted on oxidation and metal evaporation processes (CV drift—oxidation; SEM evaluation — metal evaporation).

*Data Reporting*
Process quality control data is recorded on an attribute or variable basis as required; control charts are maintained on a regular basis. This data is reviewed at periodic intervals and serves as the basis for judging the acceptability of specific processes. Summary data from the various process quality control operations are relayed to cognizant line, engineering and management personnel in real time so that, if appropriate, the necessary corrective actions can be immediately taken.

*Process Flow*
*Figure 2-1* shows the integration of the various methods of control into the wafer fabrication process flow. The process flow chart contains examples of the process quality controls and inspections utilized in the manufacturing operation.

**Fig. 2-1 Process Flow Chart**




**Process Controls (Examples)**

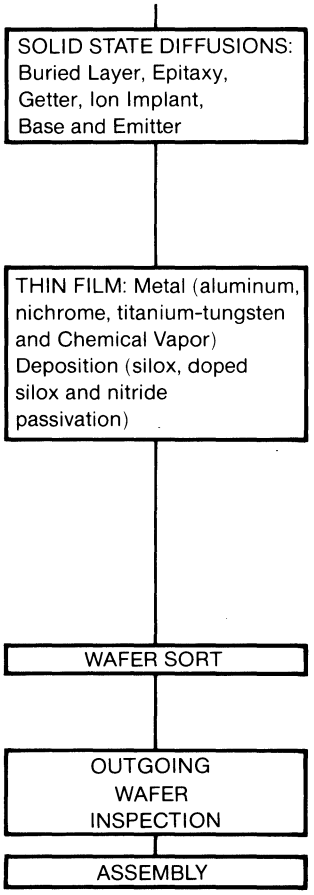
A. Environmental
B. Chemical supplies
C. Substrate exam. (resistivity, flatness, thickness, crystal perfection, etc.)
D. Photoresist evaluation
E. Mask inspections

A. Process audit

A. Process audit/qualification
B. Environmental
C. Process monitors (thickness, pinhole and crack measurements)
E. C V Plotting
F. Calibration

A. Process audits
B. Environmental
C. Visual examinations
D. Photoresist evaluation (preparation, storage, application, baking, development and removal),
E. Etchant controls
F. Exposure controls (intensity, uniformity)

**Fig. 2-1 Process Flow Chart** (cont'd.)




A. Process audits/qualification
B. Environmental
C. Temperature profiling
D. Quartz cleaning
E. Calibration
F. Electrical tests (resistivity, breakdown voltages, etc.)

A. Process audits/qualification
B. Environmental
C. Visual examinations
D. Epitaxy controls (thickness, resistivity cleaning, visual examination)
E. Metallization controls (thickness, temperature cleaning, SEM, C V plotting)
F. Glassivation controls (thickness, dopant concentraton, pinhole and crack measurements)

A. Process audit
B. Environments
C. Visual examinations

A. Process audit
B. Inspection

**Quality Assurance**

To assure that all product shipped meets both internal Fairchild specifications for standard product and customer specifications in the case of negotiated specs, a number of QA inspections throughout the assembly process flow (*Figure 2-2*) are required.

Many of the assembly operations follow the requirements of MIL-M-38510 (General Specification for Microcircuits). The test methods employed and listed are described in MIL-STD-883 (Test Methods and Procedures for Microelectronics). Most of the internal specifications, as a result, closely follow the procedures of the military specifications.

For ease of reference, and for clearer understanding of the operations performed, the MIL-STD-883 methods are listed to indicate the equivalent generic type of testing being performed. A flow, much more detailed than the one presented in *Figure 2-2*, governs the assembly of the devices and the performance of the environmental, mechanical, and electrical tests to Fairchild specifications.

**Fig. 2-2 Generalized Process Flow**

| **Operation** | **Method** |
|---|---|
| Die Forming/Scribe | |
| Die Attach | |
| QA — Die Shear Strength | 2019 |
| Ultrasonic Bonding | |
| QA — Ultrasonic Bond Strength | 2011 |
| Internal Visual (3rd OPT) | 2010 |
| QA — Internal Visual (3rd OPT) | 2010 |
| Seal — Solder or Glass | |
| External Visual (4th OPT) | 2009 |
| QA — External Visual (4th OPT) | 2009 |
| High Temperature Storage | 1008/C, E |
| Temperature Cycling | 1010/C |
| Plating (Tin/Gold) — Lead Finish | |
| QA — Plating Inspection/ Solderability | 2003 |

| **Operation** (cont'd.) | **Method** (cont'd.) |
|---|---|
| Lead Clip and Form | |
| Seal, Fine (Hermeticity Check) | 1014<br>$5 \times 10^{-8}$<br>cc/sec |
| Seal, Gross (Hermeticity Check) | Bubble Test — Fluorocarbon |
| Mark and Pack | |
| QA — External Visual | 2009 |
| QA — Seal, Fine (Hermeticity Check) | 1014<br>$5 \times 10^{-8}$<br>cc/sec |
| QA — Seal, Gross (Hermeticity Check) | Bubble Test — Fluorocarbon |
| Electrical Test | |
| Quality Conformance (Group A) | 5005 |
| QA — Plant Clearance | |
| Distribution Store | |

**Reliability**

A number of programs, among them qualification testing, reliability monitoring, failure analysis, and reliability data collection and presentation, are maintained.

*Qualification Programs*

All products receive reliability qualification prior to the product being released for shipment. Qualification is required for (1) new product designs, (2) new fabrication processes or (3) new packages or assembly processes. Stress tests are run in accordance to test methods described in MIL-STD-883B. Test results are evaluated against existing reliability levels, and must be better than or equal to current product for the new product to receive qualification.

New Product Designs — Receive, as a minimum, +125°C operating life tests. Readouts are normally scheduled at 168 hours, 1168 hours and 2168 hours. The samples stressed are electrically good units from initial wafer runs. Additional life testing, consisting of high-temperature operating life test, 85/85 humidity bias tests and bias pressure pot (BPTH) tests, may be run as deemed necessary. Redesigns of existing device layouts are considered to be new product designs, and full qualification is necessary.

New Fabrication Processes — Qualifications are designed to evaluate the new process against the current process. Stress tests consist of operating life test, high-temperature operating life test, 85/85 humidity bias test and/or biased pressure pot (BPTH) test. In addition, package environment tests may be performed. Evaluations are performed on various products throughout the development stages of the new process. Units stressed are generally from split wafer runs. All processing is performed as a single wafer lot up to the new process steps, where the lot is split for the new and the current process steps. Then the wafers are recombined, and again processed as a single wafer lot. This allows for controlled evaluation of the new process against the standard process. Both significant modifications to existing process and transferring existing products to new fabrication plants are treated as a new process.

New Packages or Assembly Processes — Qualifications are performed for new package designs, changes to existing piece parts, changes in piece part vendors, and significant modification to assembly process methods. In general, samples from three assembly runs are stressed to a matrix in accordance to MIL-STD-883B, Method 5005, group B, group C, subgroup 2, and group D (*Table 2-1*). In addition, +100°C operating life tests, 85/85 humidity bias tests, biased pressure pot (BPTH) tests and unbiased pressure pot tests are performed.

*Reliability Monitors*

Reliability testing of mature products is performed to establish device failure rates, and to identify problems occuring in production. Samples are obtained on a regular basis from production. These units are stressed with operating life tests or package environmental tests. The results of these tests are summarized and reported on a monthly basis. When a problem is identified, the respective engineering group is notified, and production is stopped until corrective action is taken.

Current testing levels are in excess of 14,000 units per year stressed with operating life tests, and 23,000 units per year stressed with package environmental tests.

*Failure Analysis*

Failure analysis is performed on all units failing reliability stress tests. Failure analysis is offered as a service to support manufacturing and engineering, and to support customer returns and customer requested failure studies. The failure analysis procedure used has been established to provide a technique of sequential analysis. This technique is based on the premise that each step of analysis will provide information of the failure without destroying information to be obtained from subsequent steps. The ultimate purpose is to uncover all underlying failure mechanisms through complete, in-depth, defect analysis. The procedure places great emphasis on electrical analysis, both external before decapsulation, and internal micro-probing. Visual examinations with high magnification microscopes or SEM analysis are used to confirm failure mechanisms. Results of the failure analysis are recorded and, if abnormalities are found, reported to engineering and/or manufacturing.

*Data Collection and Presentation*

Product reliability is controlled by first stressing the product, and then feeding back results to manufacturing and engineering. This feedback takes two forms. There is a formal monthly Reliability Summary distributed to all groups. The summary shows current product failure

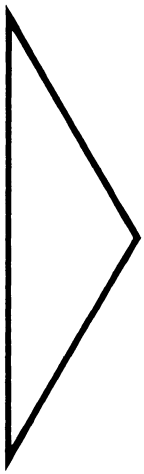
rates, highlights problem areas, and shows the status of qualification and corrective action programs. Less formal feedback is obtained by including reliability personnel at all product meetings, which gives high visibility to the reliability aspects of various products. As a customer service, product reliability data is compiled and made available upon request.

**Table 2-1 Package Environmental Stress Matrix**

| | MIL-STD-883 | |
|---|---|---|
| **Test** | **Method** | **Condition** |
| **Group B** | | |
| *Subgroup 1* | | |
| Physical dimensions | 2016 | |
| *Subgroup 2* | | |
| Resistance to solvents | 2015 | |
| *Subgroup 3* | | |
| Solderability | 2003 | Soldering temperature of 260 ± 10°C |
| *Subgroup 5* | | |
| Bond strength | 2011 | |
| (1) Thermocompression | | (1) Test condition C or D |
| (2) Ultrasonic or wedge | | (2) Test condition C or D |
| **Group C** | | |
| *Subgroup 2* | | |
| Temperature cycling | 1010 | Test condition C (−65°C to ±150°C) |
| Constant acceleration | 2001 | Test condition E (30 Kg), $Y_1$ orientation and $X_1$ orientation<br>Test condition D (20K g) for packages over 5 gram weight or with seal ring greater than 2 inches |
| Seal | 1014 | |
| (a) Fine | | |
| (b) Gross | | |
| Visual examination | | |
| End-point electrical parameters | | |
| **Group D** | | |
| *Subgroup 1* | | |
| Physical dimensions | 2016 | |
| *Subgroup 2* | | |
| Lead integrity | 2004 | Test condition B2 (lead fatigue) |
| Seal | 1014 | As applicable |
| (a) Fine | | |
| (b) Gross | | |
| Lid torque | 2024 | As applicable |

**Table 2-1 Package Environmental Stress Matrix** (cont'd.)

| Test | Method | MIL-STD-883 Condition |
|---|---|---|
| *Subgroup 3* | | |
| Thermal shock | 1011 | Test condition B (−55°C to ±125°C) 15 cycles minimum |
| Temperature cycling | 1010 | Test condition C, (−65°C to ±150°C) 100 cycles minimum. |
| Moisture resistance | 1004 | |
| Seal | 1014 | |
| (a) Fine | | |
| (b) Gross | | |
| Visual examination | | |
| End-point electrical parameters | | |
| *Subgroup 4* | | |
| Mechanical shock | 2002 | Test condition B (1500g, 0.5 ms) |
| Vibration, variable frequency | 2007 | Test condition A (20g) |
| Constant acceleration | 2001 | Same as group C, subgroup 2 |
| Seal | | |
| (a) Fine | | |
| (b) Gross | | |
| Visual examination | | |
| End-point electrical parameters | | |
| *Subgroup 5* | | |
| Salt atmosphere | 1009 | Test condition A minimum (24 hours) |
| Seal | 1014 | As applicable |
| (a) Fine | | |
| (b) Gross | | |
| Visual examination | | |
| *Subgroup 6* | | |
| Internal water-vapor content | 1018 | |
| *Subgroup 7* | | |
| Adhesion of lead finish | 2025 | |



# F100K DC Family Specifications

DC characteristics for the F100K series family parametric limits listed below are guaranteed for the entire F100K ECL family unless specified on the individual data sheet.

**Absolute Maximum Ratings:** Above which the useful life may be impaired[1]

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Maximum Junction Temperature ($T_J$) | 0°C to +150°C |
| Case Temperature Under Bias ($T_C$) | 0°C to +85°C |
| $V_{EE}$ Pin Potential to Ground Pin | −7.0 V to +0.5 V |
| Input Voltage (dc) | $V_{EE}$ to +0.5 V |
| Output Current (dc Output HIGH) | −50 mA |
| Operating Range[2] | −5.7 V to −4.2 V |



**DC Characteristics:** $V_{EE}$ = −4.5 V, $V_{CC}$ = $V_{CCA}$ = GND, $T_C$ = 0°C to +85°C, Note 3

| Symbol | Characteristic | Min | Typ | Max | Unit | Conditions[4] | |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | −1025 | −955 | −880 | mV | $V_{IN}$ = $V_{IH(max)}$ or $V_{IL(min)}$ | Loading with 50 Ω to −2.0 V |
| $V_{OL}$ | Output LOW Voltage | −1810 | −1705 | −1620 | mV | | |
| $V_{OHC}$ | Output HIGH Voltage | −1035 | | | mv | $V_{IN}$ = $V_{IH(min)}$ or $V_{IL(max)}$ | |
| $V_{OLC}$ | Output LOW Voltage | | | −1610 | mV | | |
| $V_{IH}$ | Input HIGH Voltage | −1165 | | −880 | mV | Guaranteed HIGH Signal for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | −1810 | | −1475 | mV | Guaranteed LOW Signal for All Inputs | |
| $I_{IL}$ | Input LOW Current | 0.50 | | | μA | $V_{IN}$ = $V_{IL(min)}$ | |

1. Unless specified otherwise on individual data sheet.
2. Parametric values specified at −4.2 V to −4.8 V.
3. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute, conformance testing performed instantaneously where $T_A$ = $T_J$= $T_C$. Correlated temperatures, typically 25°C and 100°C, and limits may be used to guarantee device operating performance.

**DC Characteristics:** $V_{EE} = -4.2$ V, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$, Note 3

| Symbol | Characteristic | Min | Typ | Max | Unit | Conditions[4] | |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | −1020 | | −870 | mV | $V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$ | Loading with 50 Ω to −2.0 V |
| $V_{OL}$ | Output LOW Voltage | −1810 | | −1605 | mV | | |
| $V_{OHC}$ | Output HIGH Voltage | −1030 | | | mv | $V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$ | |
| $V_{OLC}$ | Output LOW Voltage | | | −1595 | mV | | |
| $V_{IH}$ | Input HIGH Voltage | −1150 | | −880 | mV | Guaranteed HIGH Signal for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | −1810 | | −1475 | mV | Guaranteed LOW Signal for All Inputs | |
| $I_{IL}$ | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL(min)}$ | |

**DC Characteristics:** $V_{EE} = -4.8$ V, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$, Note 3

| Symbol | Characteristic | Min | Typ | Max | Unit | Conditions[4] | |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | −1035 | | −880 | mV | $V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$ | Loading with 50 Ω to −2.0 V |
| $V_{OL}$ | Output LOW Voltage | −1830 | | −1620 | mV | | |
| $V_{OHC}$ | Output HIGH Voltage | −1045 | | | mv | $V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$ | |
| $V_{OLC}$ | Output LOW Voltage | | | −1610 | mV | | |
| $V_{IH}$ | Input HIGH Voltage | −1165 | | −880 | mV | Guaranteed HIGH Signal for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | −1810 | | −1490 | mV | Guaranteed LOW Signal for All Inputs | |
| $I_{IL}$ | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL(min)}$ | |

Notes on preceding page

# F10K DC Family Specifications

DC characteristics for the F10K series memories. Parametric limits listed below are guaranteed for all F10K memories, except where noted on individual data sheets.

**Absolute Maximum Ratings:** Above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| $V_{EE}$ Pin Potential to Ground Pin | −7.0 V to +0.5 V |
| Input Voltage (dc) | $V_{EE}$ to +0.5 V |
| Output Current (dc Output HIGH) | −30 mA to +0.1 mA |

**Guaranteed Operating Ranges**

| Supply Voltage ($V_{CC}$) | | | Ambient Temperature ($T_A$) Note 1 |
|---|---|---|---|
| **Min** | **Typ** | **Max** | |
| −5.46 V | −5.2 V | −4.94 V | 0°C to +75°C |

3

**DC Characteristics:** $V_{EE}$ = −5.2 V, Output Load = 50 Ω and 30 pF to −2.0 V, $T_A$ = 0°C to 75°C[1]

| Symbol | Characteristic | Min | Typ | Max | Unit | $T_A$ | Conditions[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | −1000<br>−960<br>−900 | | −840<br>−810<br>−720 | mV | 0°C<br>+25°C<br>+75°C | $V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$ | Loading is 50 Ω to −2.0 V |
| $V_{OL}$ | Output LOW Voltage | −1870<br>−1850<br>−1830 | | −1665<br>−1650<br>−1625 | mV | 0°C<br>+25°C<br>+75°C | | |
| $V_{OHC}$ | Output HIGH Voltage | −1020<br>−980<br>−920 | | | mv | 0°C<br>+25°C<br>+75°C | $V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$ | |
| $V_{OLC}$ | Output LOW Voltage | | | −1645<br>−1630<br>−1605 | mV | 0°C<br>+25°C<br>+75°C | | |
| $V_{IH}$ | Input HIGH Voltage | −1145<br>−1105<br>−1045 | | −840<br>−810<br>−720 | mV | 0°C<br>+25°C<br>+75°C | Guaranteed Input Voltage HIGH for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | −1870<br>−1850<br>−1830 | | −1490<br>−1475<br>−1450 | mV | 0°C<br>+25°C<br>+75°C | Guaranteed Input Voltage LOW for All Inputs | |
| $I_{IL}$ | Input LOW Current | 0.5 | | 170 | μA | +25°C | $V_{IN} = V_{IL(min)}$ | |

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute, conformance testing performed instantaneously where $T_A = T_J = T_C$. Correlated temperatures, typically 25°C and 100°C, and limits may be used to guarantee device operating performance.

FAIRCHILD
A Schlumberger Company

# F100414
# 256 x 1-Bit Static Random Access Memory

Bipolar Division

F100K ECL Product

## Description

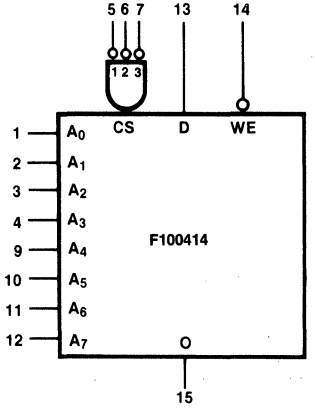
The F100414 is a 256-bit read/write Random Access Memory (RAM), organized 256 words by one bit. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as three active-LOW Chip Select lines.

- **Address Access Time — 10 ns Max**
- **Chip Select Access Time — 6.0 ns Max**
- **Open-emitter Output for Easy Memory Expansion**
- **Power Dissipation — 1.8 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $\overline{WE}$ | Write Enable Input (Active LOW) |
| $\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$ | Chip Select Inputs (Active LOW) |
| $A_0$–$A_7$ | Address Inputs |
| D | Data Input |
| O | Data Output |

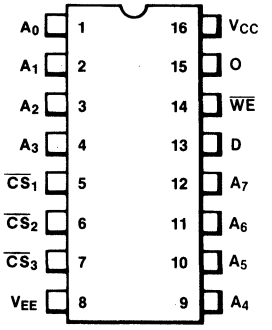
## Logic Symbol




$V_{CC}$ = Pin 16
$V_{EE}$ = Pin 8

## Connection Diagram

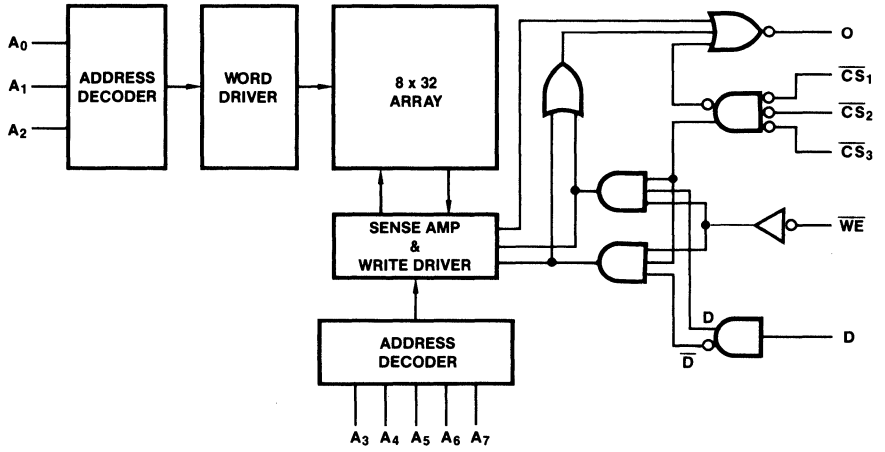
**16-Pin DIP** (Top View)




**Note**

The 16-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

## Logic Diagram




### Functional Description

The F100414 is a fully decoded 256-bit read/write random access memory, organized 256 words by one bit. Bit selection is achieved by means of an 8-bit address, $A_0$ through $A_7$.

Three active-LOW Chip Select inputs are provided for increased logic flexibility. This permits memory array expansion up to 2048 words with the F100170 decoder. For larger memories, the fast chip select access time permits the decoding of Chip Select, $\overline{CS}$, from the address without affecting system performance.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the output (O).

The output of the F100414 is an unterminated emitter follower, which allows maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F100414 devices together to allow easy expansion. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output.

### Truth Table

| Inputs | | | | | Output | |
|---|---|---|---|---|---|---|
| $\overline{CS_1}$ | $\overline{CS_2}$ | $\overline{CS_3}$ | $\overline{WE}$ | D | O | Mode |
| X | X | H* | X | X | L | Not Selected |
| L | L | L | L | L | L | Write "0" |
| L | L | L | L | H | L | Write "1" |
| L | L | L | H | X | Data | Read |

H = HIGH Voltage Levels = −0.9 V (Nominal)
L = LOW Voltage Levels = −1.7 V (Nominal)
X = Don't Care
Data = Previously stored data
*One or more Chip Selects HIGH

**DC Characteristics:** $V_{EE}$ = −4.2 V to −4.8 V, $V_{CC}$ = GND, $T_C$ = 0°C to +85°C unless otherwise specified[1]

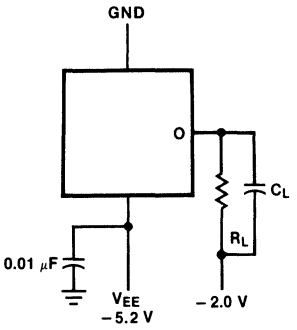
| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input HIGH Current | | | 220 | μA | $V_{IN} = V_{IH(max)}$ |
| $I_{IL}$ | Input LOW Current, $\overline{CS}_n$<br>$\overline{WE}$, $A_0$-$A_7$, D | 0.5<br>−50 | | 170 | μA | $V_{IN} = V_{IL(min)}$ |
| $I_{EE}$ | Power Supply Current | −140 | −100 | | mA | Inputs and Output Open |

**AC Characteristics:** $V_{EE}$ = −4.2 V to −4.8 V, $V_{CC}$ = GND, Output Load = 50 Ω and 30 pF to −2.0 V, $T_C$ = 0°C to +85°C

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| | **Read Timing** | | | | | |
| $t_{ACS}$ | Chip Select Access Time | | | 6.0 | ns | |
| $t_{RCS}$ | Chip Select Recovery Time | | | 6.0 | ns | *Figures 3a, 3b* |
| $t_{AA}$ | Address Access Time[2] | | | 10 | ns | |
| | **Write Timing** | | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[3] | 7.0 | | | ns | |
| $t_{WSD}$ | Data Setup Time prior to Write | 1.0 | | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 2.0 | | | ns | |
| $t_{WSA}$ | Address Setup Time prior to Write[3] | 1.0 | | | ns | *Figure 4* |
| $t_{WHA}$ | Address Hold Time after Write | 2.0 | | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time prior to Write | 1.0 | | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 2.0 | | | ns | |
| $t_{WS}$ | Write Disable Time | | | 8.0 | ns | |
| $t_{WR}$ | Write Recovery Time | | | 10 | ns | |
| $t_r$ | Output Rise Time | | 3.0 | | ns | Measured between 20% and |
| $t_f$ | Output Fall Time | | 3.0 | | ns | 80% or 80% and 20% |
| $C_{IN}$ | Input Pin Capacitance | | 4.0 | 5.0 | pF | Measured with a Pulse |
| $C_{OUT}$ | Output Pin Capacitance | | 7.0 | 8.0 | pF | Technique |

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. $T_W$ measured at $t_{WSA}$ = Min, $t_{WSA}$ measured at $t_W$ = Min.

**Fig. 1 AC Test Circuit**




**Notes**
All Timing Measurements Referenced to 50% of Input Levels
$C_L$ = 30 pF including Fixture and Stray Capacitance
$R_L$ = 50 Ω to −2.0 V

**Fig. 2 Input Levels**

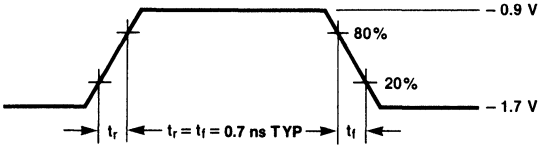
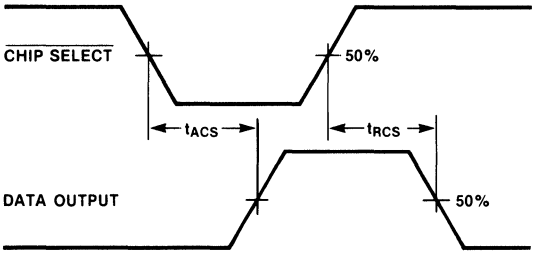
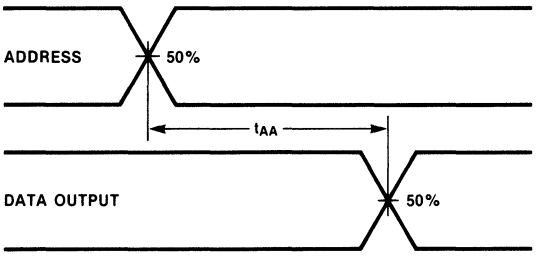



**Fig. 3 Read Mode Timing**

**a Read Mode Propagation Delay from Chip Select**

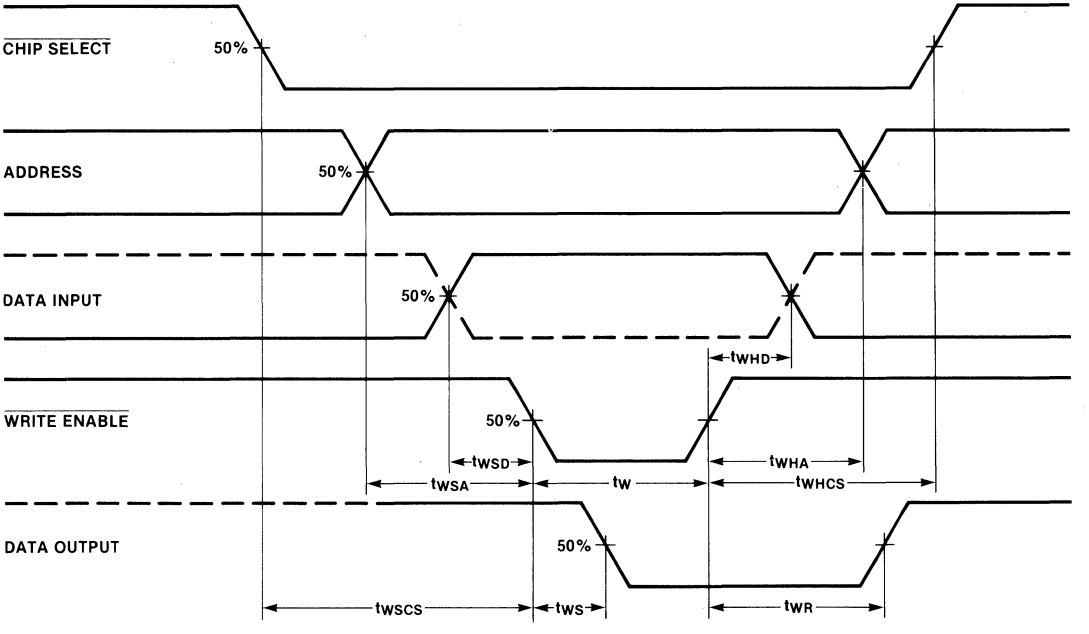



**b Read Mode Propagation Delay from Address**



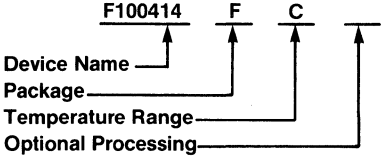

3

**Fig. 4 Write Mode Timing**




**Note**
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

## Ordering Information



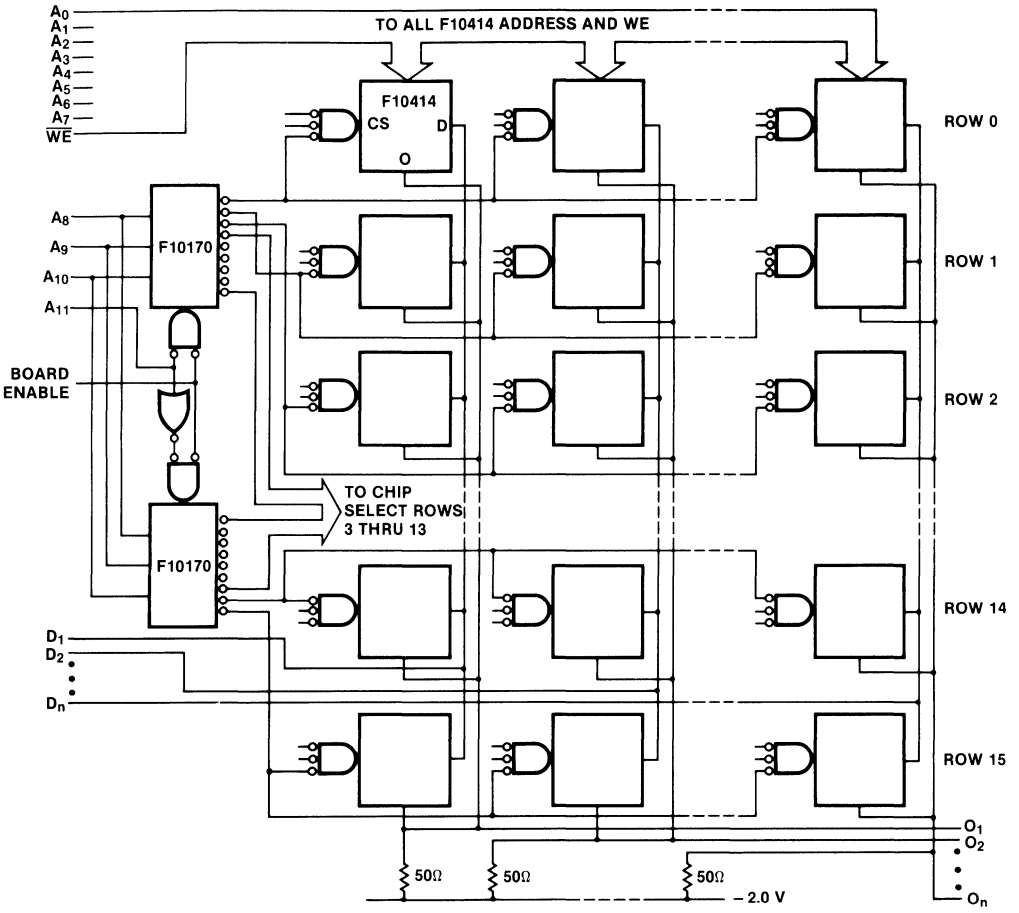

**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak
P = Plastic DIP

**Temperature Range**
C = 0°C to +85°C, Case

**Optional Processing**
QR = 160 Hour Burn In

## Typical Application

### 4096-Word x n-Bit System



FAIRCHILD
A Schlumberger Company

# F100415
# 1024 x 1-Bit Static Random Access Memory

Bipolar Division

F100K ECL Product

## Description

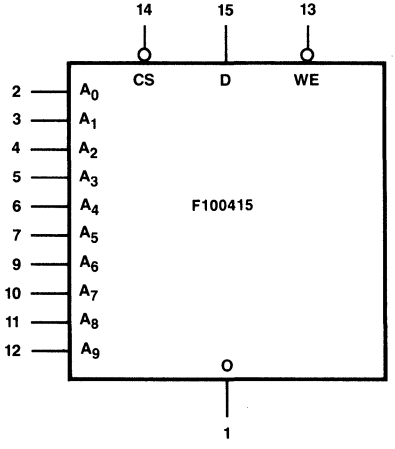
The F100415 is a 1024-bit read/write Random Access Memory (RAM), organized as 1024 words by one bit per word and designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

- **Address Access Time — 20 ns Max**
- **Chip Select Access Time — 8.0 ns Max**
- **Open-emitter Output for Easy Memory Expansion**
- **Power Dissipation — 0.5 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $\overline{WE}$ | Write Enable Input (Active LOW) |
| $\overline{CS}$ | Chip Select Input (Active LOW) |
| $A_0$–$A_9$ | Address Inputs |
| D | Data Input |
| O | Data Output |

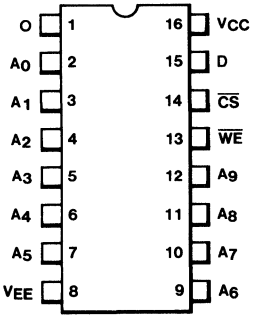
## Logic Symbol




$V_{CC}$ = Pin 16
$V_{EE}$ = Pin 8

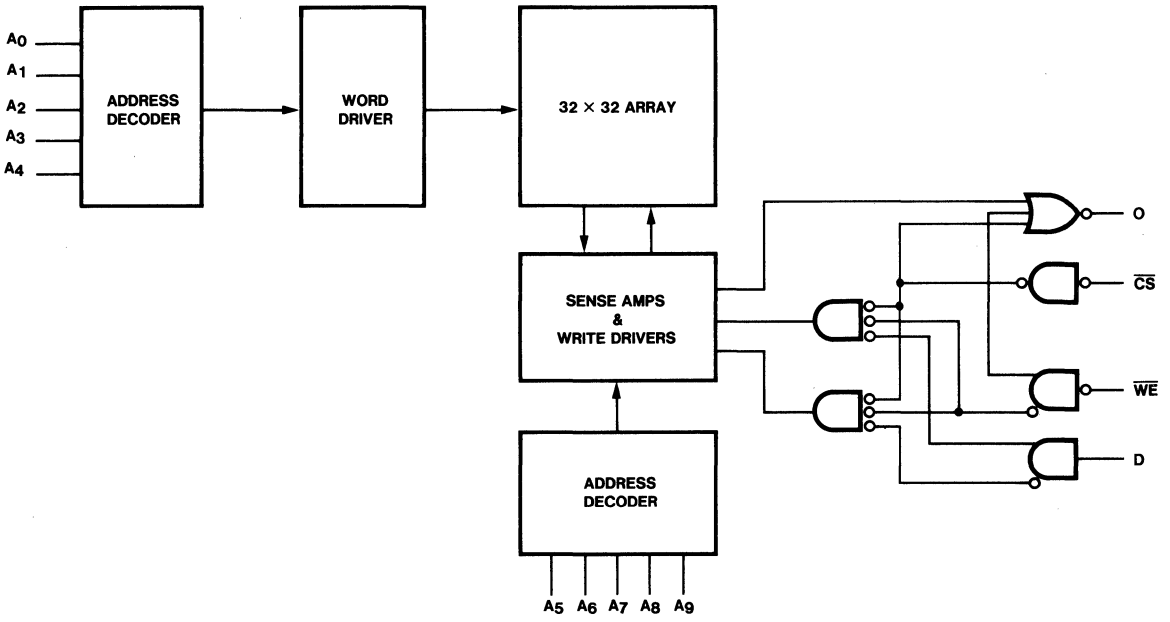
## Connection Diagram

**16-Pin DIP** (Top View)




**Note**
The 16-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package

## Logic Diagram






**Functional Description**

The F100415 is a fully decoded 1024-bit read/write random access memory, organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, $A_0$ through $A_9$.

One Chip Select input is provided for memory array expansion up to 2048 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of Chip Select, ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the output (O).

The output of the F100415 is an unterminated emitter follower, which allows maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F100415 devices together to allow easy expansion. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output.

**Truth Table**

| Inputs | | | Output | Mode |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | D | O | |
| H | X | X | L | Not Selected |
| L | L | L | L | Write "0" |
| L | L | H | L | Write "1" |
| L | H | X | Data | Read |

H = HIGH Voltage Levels = −0.9 V (Nominal)
L = LOW Voltage Levels = −1.7 V (Nominal)
X = Don't Care
Data = Previously stored data

**DC Characteristics:** $V_{EE}$ = −4.2 V to −4.8 V, $V_{CC}$ = GND, $T_C$ = 0°C to +85°C unless otherwise specified[1]

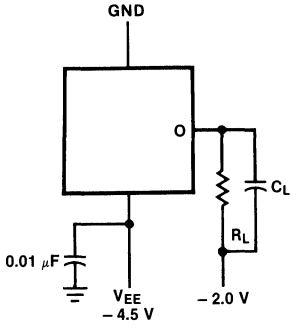
| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input HIGH Current | | | 220 | μA | $V_{IN} = V_{IH(max)}$ |
| $I_{IL}$ | Input LOW Current, $\overline{CS}$<br>$\overline{WE}$, $A_0$-$A_9$, D | 0.5<br>−50 | | 170 | μA | $V_{IN} = V_{IL(min)}$ |
| $I_{EE}$ | Power Supply Current | −150 | −105 | | mA | Inputs and Output Open |

**AC Characteristics:** $V_{EE}$ = −4.2 V to −4.8 V, $V_{CC}$ = GND, Output Load = 50 Ω and 30 pF to −2.0 V, $T_C$ = 0°C to +85°C

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| | **Read Timing** | | | | | |
| $t_{ACS}$ | Chip Select Access Time | | | 8.0 | ns | |
| $t_{RCS}$ | Chip Select Recovery Time | | | 8.0 | ns | *Figures 3a, 3b* |
| $t_{AA}$ | Address Access Time[2] | | | 20 | ns | |
| | **Write Timing** | | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[3] | 14 | | | ns | |
| $t_{WSD}$ | Data Setup Time prior to Write | 4.0 | | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 4.0 | | | ns | |
| $t_{WSA}$ | Address Setup Time prior to Write[3] | 5.0 | | | ns | *Figure 4* |
| $t_{WHA}$ | Address Hold Time after Write | 3.0 | | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time prior to Write | 4.0 | | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 4.0 | | | ns | |
| $t_{WS}$ | Write Disable Time | | | 10 | ns | |
| $t_{WR}$ | Write Recovery Time | | | 15 | ns | |
| $t_r$ | Output Rise Time | | 5.0 | | ns | Measured between 20% and |
| $t_f$ | Output Fall Time | | 5.0 | | ns | 80% or 80% and 20% |
| $C_{IN}$ | Input Pin Capacitance | | 4.0 | 5.0 | pF | Measured with a Pulse |
| $C_{OUT}$ | Output Pin Capacitance | | 7.0 | 8.0 | pF | Technique |

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. $T_W$ measured at $t_{WSA}$ = Min, $t_{WSA}$ measured at $t_W$ = Min.

**Fig. 1 AC Test Circuit**




**Notes**
All Timing Measurements Referenced to 50% of Input Levels
$C_L$ = 30 pF including Fixture and Stray Capacitance
$R_L$ = 50 Ω to – 2.0 V.

**Fig. 2 Input Levels**

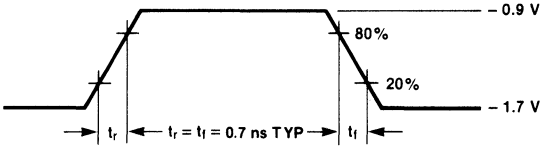
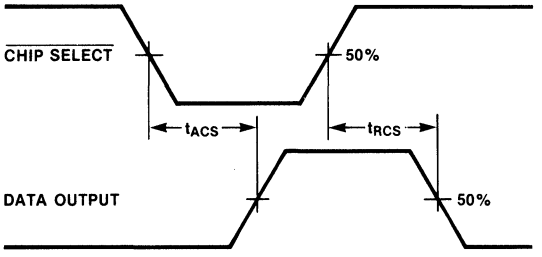
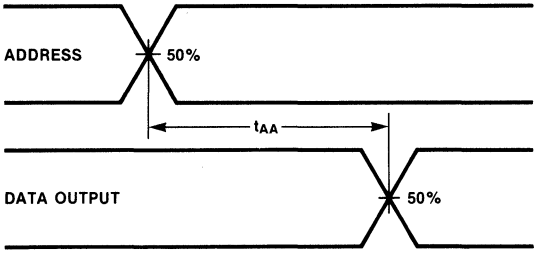



**Fig. 3 Read Mode Timing**

**a Read Mode Propagation Delay from Chip Select**

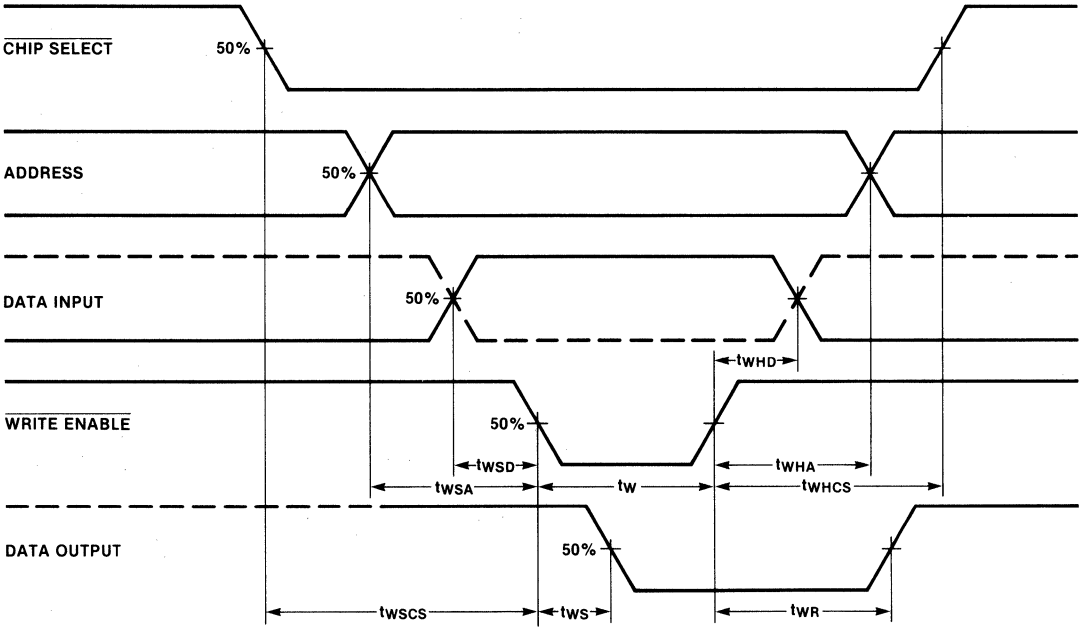



**b Read Mode Propagation Delay from Address**



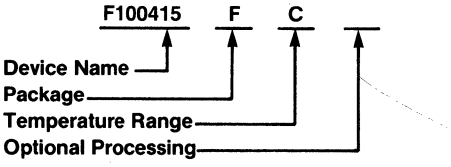

3

**Fig. 4 Write Mode Timing**




**Note**
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

## Ordering Information



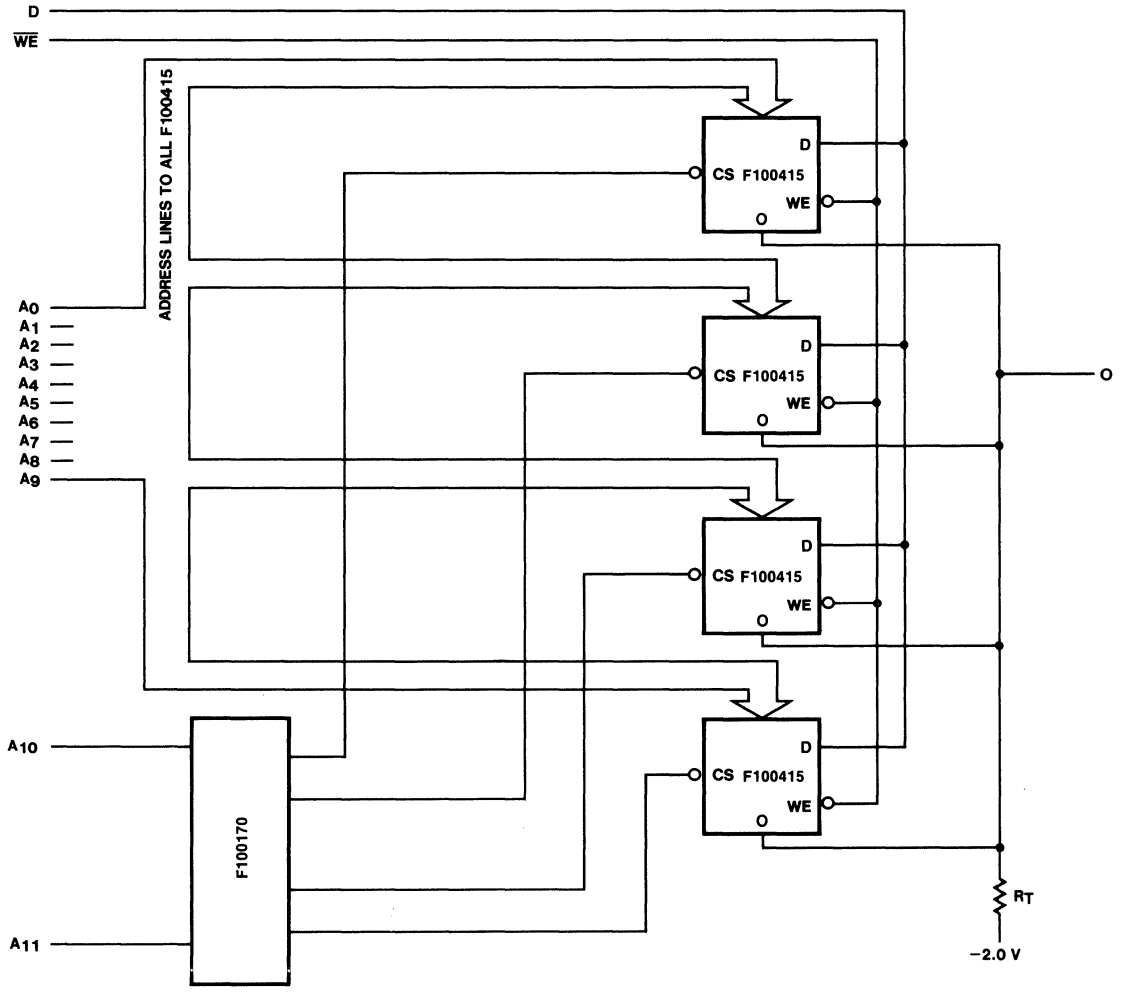

**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak
P = Plastic DIP

**Temperature Range**
C = 0°C to +85°C, Case

**Optional Processing**
QR = 160 Hour Burn In

## Typical Application

### 4096-Word x n-Bit System



FAIRCHILD
A Schlumberger Company

# F100422
# 256 x 4-Bit Static Random Access Memory

Bipolar Division

F100K ECL Product

## Description

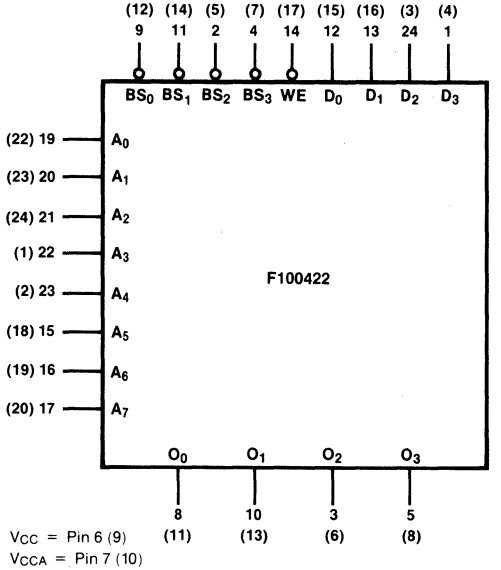
The F100422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits per word. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as four active-LOW Bit Select lines.

- **Address Access Time — 10 ns Max**
- **Bit Select Access Time — 5.0 ns Max**
- **Four Bits Can be Independently Selected**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation — 0.79 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $\overline{WE}$ | Write Enable Input (Active LOW) |
| $\overline{BS}_0 - \overline{BS}_3$ | Bit Select Inputs (Active LOW) |
| $A_0 - A_7$ | Address Inputs |
| $D_0 - D_3$ | Data Inputs |
| $O_0 - O_3$ | Data Outputs |

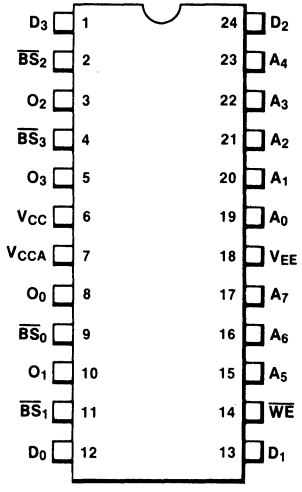
## Logic Symbol



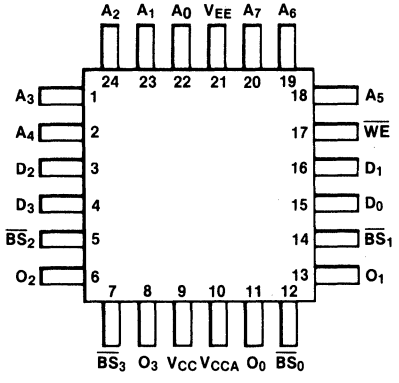

VCC = Pin 6 (9)
VCCA = Pin 7 (10)
VEE = Pin 18 (21)
( ) = Flatpak

## Connection Diagrams

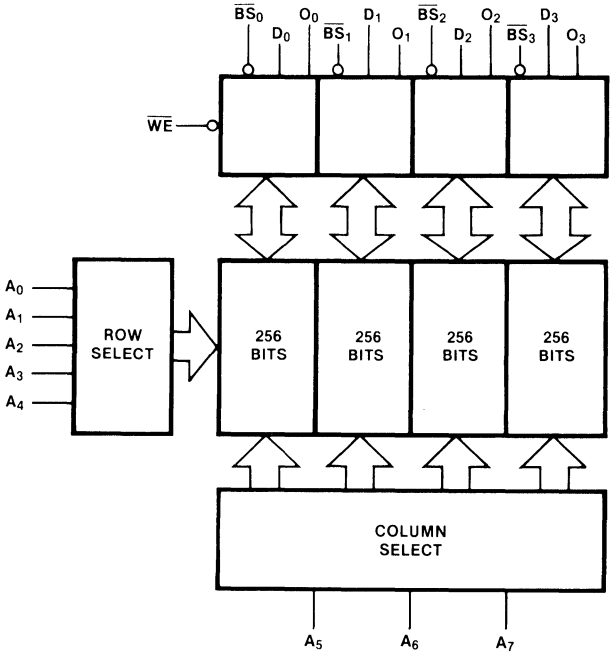
**24-Pin DIP** (Top View)




**24-Pin Flatpak** (Top View)



### Logic Diagram




### Functional Description

The F100422 is a fully decoded 1024-bit read/write random access memory, organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, $A_0$ through $A_7$.

Four Bit Select inputs are provided for logic flexibility. For larger memories, the fast bit select access time permits the decoding of individual bit selects from the address without increasing address access time.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the bit selected, the data at $D_0$-$D_3$ is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the bit selected. Non-inverted data is then presented at the output ($O_0$-$O_3$).

The outputs of the F100422 are unterminated emitter followers, which allow maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F100422 devices together to allow easy expansion. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output.

### Truth Table

| Inputs | | | Outputs | |
|---|---|---|---|---|
| $\overline{BS}_n$ | $\overline{WE}$ | $D_n$ | $O_n$ | Mode |
| H | X | X | L | Not Selected |
| L | L | L | L | Write "0" |
| L | L | H | L | Write "1" |
| L | H | X | Data | Read |

Each bit has independent $\overline{BS}$, D, and O, but all have common $\overline{WE}$
H = HIGH Voltage Levels = −0.9 V (Nominal)
L = LOW Voltage Levels = −1.7 V (Nominal)
X = Don't Care
Data = Previously stored data

**DC Characteristics:** $V_{EE}$ = −4.2 to −4.8 V, $V_{CC}$ = $V_{CCA}$ = GND, $T_C$ = 0°C to +85°C unless otherwise specified[1]

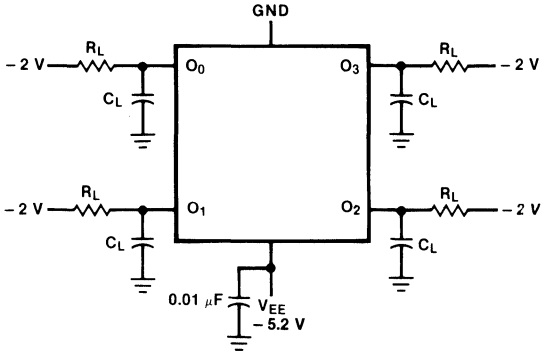
| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input HIGH Current | | | 220 | μA | $V_{IN}$ = $V_{IH(max)}$ |
| $I_{IL}$ | Input LOW Current, $\overline{BS_0}$-$\overline{BS_3}$<br>$\overline{WE}$, $A_0$-$A_7$, $D_0$-$D_3$ | 0.5<br>−50 | | 170 | μA | $V_{IN}$ = $V_{IL(min)}$ |
| $I_{EE}$ | Power Supply Current | −200 | −180 | | mA | All Inputs and Outputs Open |

**AC Characteristics:** $V_{EE}$ = −4.2 to −4.8 V, $V_{CC}$ = $V_{CCA}$ = GND, Output Load = 50 Ω and 30 pF to −2.0 V,
$T_C$ = 0°C to +85°C

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| | **Read Timing** | | | | | |
| $t_{ACS}$ | Chip Select Access Time | | | 5.0 | ns | |
| $t_{RCS}$ | Chip Select Recovery Time | | | 5.0 | ns | *Figures 3a, 3b* |
| $t_{AA}$ | Address Access Time[2] | | | 10 | ns | |
| | **Write Timing** | | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[3] | 7.0 | | | ns | |
| $t_{WSD}$ | Data Setup Time prior to Write | 1.0 | | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 2.0 | | | ns | |
| $t_{WSA}$ | Address Setup Time prior to Write[3] | 1.0 | | | ns | *Figure 4* |
| $t_{WHA}$ | Address Hold Time after Write | 2.0 | | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time prior to Write | 1.0 | | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 2.0 | | | ns | |
| $t_{WS}$ | Write Disable Time | | | 5.0 | ns | |
| $t_{WR}$ | Write Recovery Time | | | 12 | ns | |
| $t_r$ | Output Rise Time | | 3.0 | | ns | Measured between 20% and |
| $t_f$ | Output Fall Time | | 3.0 | | ns | 80% or 80% and 20% |
| $C_{IN}$ | Input Pin Capacitance | | 4.0 | 5.0 | pF | Measured with a Pulse |
| $C_{OUT}$ | Output Pin Capacitance | | 7.0 | 8.0 | pF | Technique |

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. $T_W$ measured at $t_{WSA}$ = Min, $t_{WSA}$ measured at $t_W$ = Min.

**Fig. 1 AC Test Circuit**




**Notes**
All Timing Measurements Referenced to 50% of Input Levels
$C_L$ = 30 pF including Fixture and Stray Capacitance
$R_L$ = 50 Ω to –2.0 V

**Fig. 2 Input Levels**

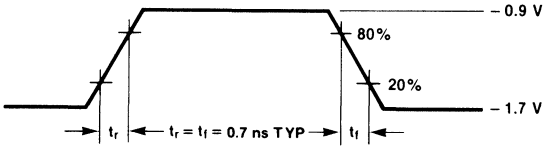
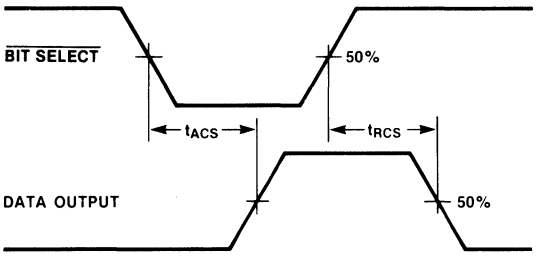
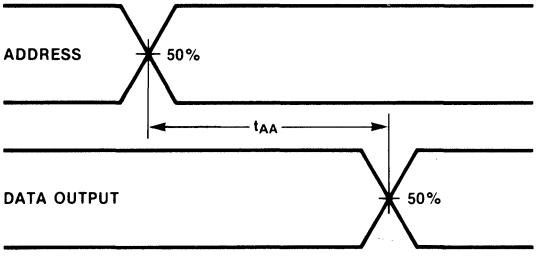



**Fig. 3 Read Mode Timing**

**a Read Mode Propagation Delay from Bit Select**

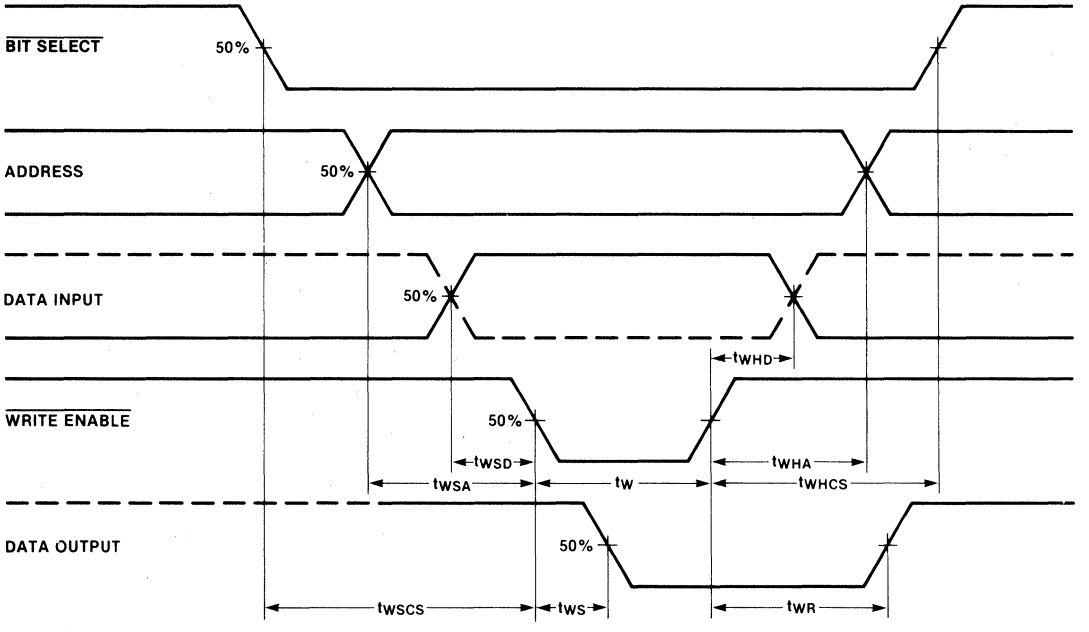



**b Read Mode Propagation Delay from Address**



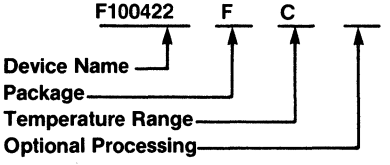

3

**Fig. 4 Write Mode Timing**




**Note**
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

## Ordering Information




**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak

**Temperature Ranges**
C = 0°C to +85°C, Case

**Optional Processing**
QR = 160 Hour Burn In

FAIRCHILD
A Schlumberger Company

# F100470
# 4096 x 1-Bit Static Random Access Memory

Bipolar Division

F100K ECL Product

## Description

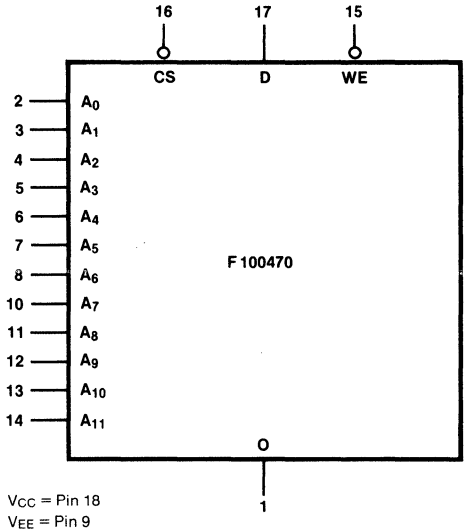
The F100470 is a 4096-bit read/write Random Access Memory (RAM), organized 4096 words by one bit per word and designed for high-speed scratchpad, control and buffer storage applications. It is available in two speed versions, the F100470 and F100470A. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

- **Address Access Time**
  **F100470 — 35 ns Max**
  **F100470A — 25 ns Max**
- **Chip Select Access Time**
  **F100470 — 15 ns Max**
  **F100470A — 10 ns Max**
- **Open-emitter Output for Easy Memory Expansion**
- **Power Dissipation — 0.17 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $\overline{WE}$ | Write Enable Input (Active LOW) |
| $\overline{CS}$ | Chip Select Input (Active LOW) |
| $A_0$-$A_{11}$ | Address Inputs |
| D | Data Input |
| O | Data Output |

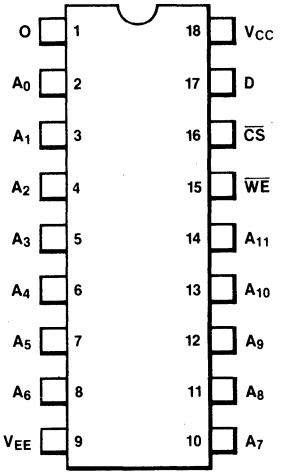
## Logic Symbol




$V_{CC}$ = Pin 18
$V_{EE}$ = Pin 9

## Connection Diagram

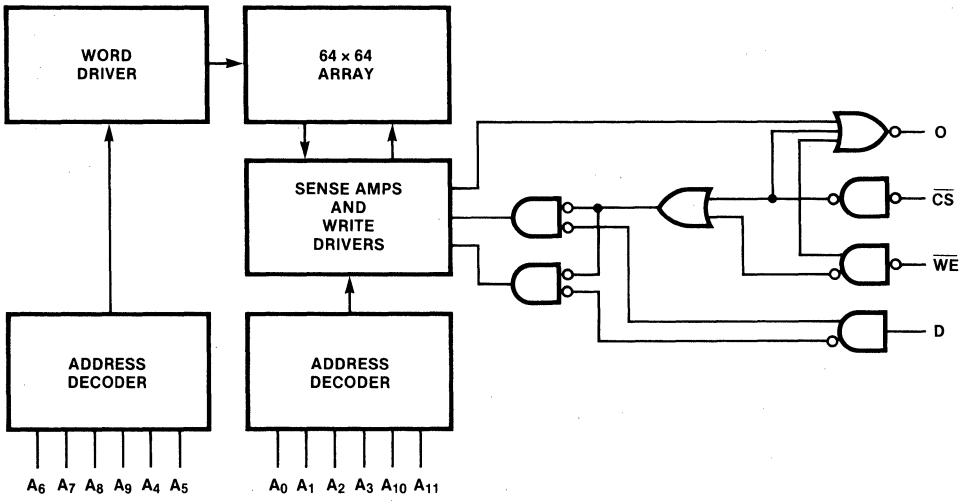
**18-Pin DIP** (Top View)




**Note**
The 18-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

3

**Logic Diagram**




**Functional Description**

The F100470 is a fully decoded 4096-bit read/write random access memory, organized 4096 words by one bit. Bit selection is achieved by means of a 12-bit address, $A_0$ through $A_{11}$.

One Chip Select input is provided for memory array expansion up to 8196 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of Chip Select, ($\overline{CS}$) from the address without increasing address access time.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the output (O).

The output of the F100470 is an unterminated emitter follower, which allows maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F100470 devices together. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is OFF.

**Truth Table**

| Inputs | | | Output | |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | D | O | Mode |
| H | X | X | L | Not Selected |
| L | L | L | L | Write "0" |
| L | L | H | L | Write "1" |
| L | H | X | Data | Read |

H = HIGH Voltage Levels = −0.9 V (Nominal)
L = LOW Voltage Levels = −1.7 V (Nominal)
X = Don't Care
Data = Previously stored data

**DC Characteristics:** $V_{EE}$ = −4.2 V to −4.8 V, $V_{CC}$ = GND, $T_C$ = 0°C to +85°C unless otherwise specified[1]

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input HIGH Current | | | 220 | μA | $V_{IN} = V_{IH(max)}$ |
| $I_{IL}$ | Input LOW Current, $\overline{CS}$<br>$\overline{WE}$, $A_0$-$A_{11}$, D | 0.5<br>−50 | | 170 | μA | $V_{IN} = V_{IL(min)}$ |
| $I_{EE}$ | Power Supply Current | −195 | −160 | | mA | Inputs and Output Open |

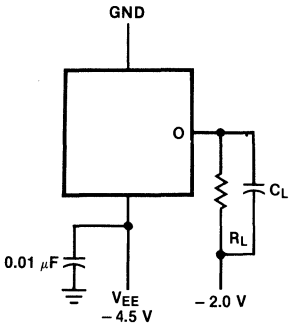
**AC Characteristics:** $V_{EE}$ = −4.2 V to −4.8 V, $V_{CC}$ = GND, Output Load = 50 Ω and 30 pF to −2.0 V, $T_C$ = 0°C to +85°C

| Symbol | Characteristic | F100470 Min | F100470 Max | F100470A Min | F100470A Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | **Read Timing** | | | | | | |
| $t_{ACS}$ | Chip Select Access Time | | 15 | | 10 | ns | |
| $t_{RCS}$ | Chip Select Recovery Time | | 15 | | 10 | ns | *Figures 3a, 3b* |
| $t_{AA}$ | Address Access Time[2] | | 35 | | 25 | ns | |
| | **Write Timing** | | | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[3] | 25 | | 15 | | ns | |
| $t_{WSD}$ | Data Setup Time prior to Write | 5.0 | | 5.0 | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 5.0 | | 5.0 | | ns | |
| $t_{WSA}$ | Address Setup Time prior to Write[3] | 10 | | 10 | | ns | *Figure 4* |
| $t_{WHA}$ | Address Hold Time after Write | 5.0 | | 5.0 | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time prior to Write | 5.0 | | 5.0 | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 5.0 | | 5.0 | | ns | |
| $t_{WS}$ | Write Disable Time | | 15 | | 15 | ns | |
| $t_{WR}$ | Write Recovery Time | | 20 | | 20 | ns | |

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $t_r$ | Output Rise Time | | 5.0 | | ns | Measured between 20% and |
| $t_f$ | Output Fall Time | | 5.0 | | ns | 80% or 80% and 20% |
| $C_{IN}$ | Input Pin Capacitance | | 4.0 | 5.0 | pF | Measured with a Pulse |
| $C_{OUT}$ | Output Pin Capacitance | | 7.0 | 8.0 | pF | Technique |

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. $T_W$ measured at $t_{WSA}$ = Min, $t_{WSA}$ measured at $t_W$ = Min.

**Fig. 1 AC Test Circuit**




**Notes**
All Timing Measurements Referenced to 50% of Input Levels
$C_L$ = 30 pF including Fixture and Stray Capacitance
$R_L$ = 50 Ω to – 2.0 V.

**Fig. 2 Input Levels**

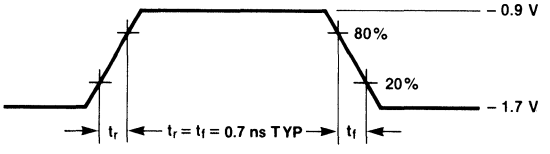
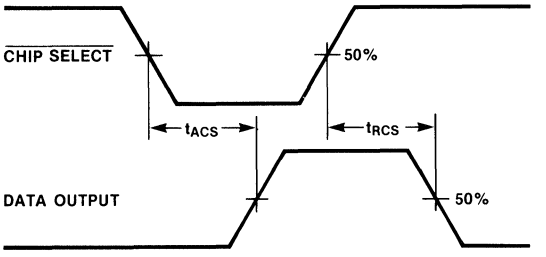



**Fig. 3 Read Mode Timing**

**a Read Mode Propagation Delay from Chip Select**




**b Read Mode Propagation Delay from Address**

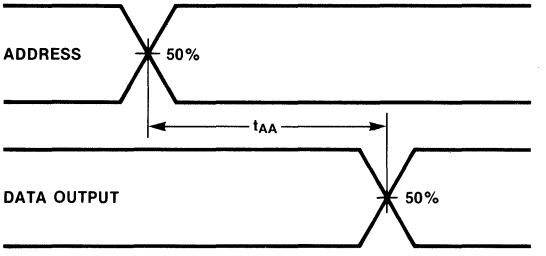
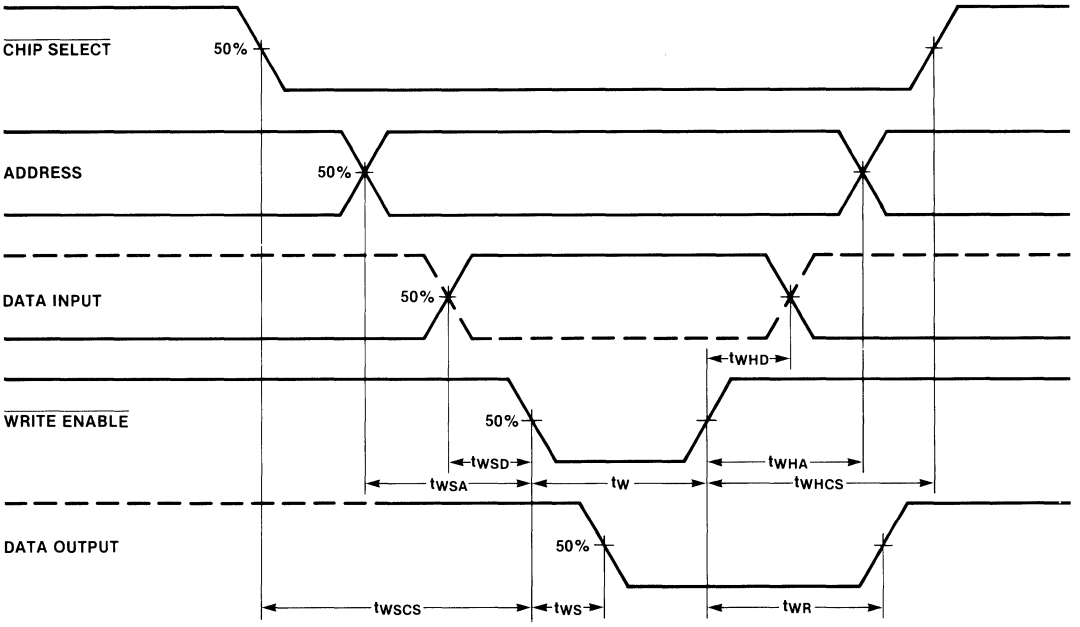
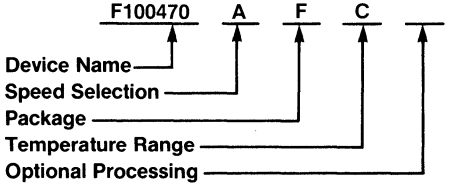


**Fig. 4 Write Mode Timing**




**Note**
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

## Ordering Information




**Speed Selection**
Blank = Standard Speed
A = 'A' Grade

**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak

**Temperature Range**
C = 0°C to +85°C, Case

**Optional Processing**
QR = 160 Hour Burn In

FAIRCHILD
A Schlumberger Company

# F100474
# 1024 x 4-Bit Static Random Access Memory

Bipolar Division

F100K ECL Product

## Description

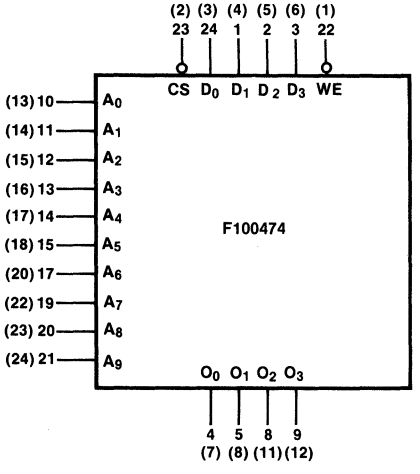
The F100474 is a 4096-bit read/write Random Access Memory (RAM), organized 1024 words by four bits per word. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

- **Address Access Time — 25 ns Max**
- **Chip Select Access Time — 15 ns Max**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation — 0.17 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $\overline{WE}$ | Write Enable Input (Active LOW) |
| $\overline{CS}$ | Chip Select Input (Active LOW) |
| $A_0$–$A_9$ | Address Inputs |
| $D_0$–$D_3$ | Data Inputs |
| $O_0$–$O_3$ | Data Outputs |

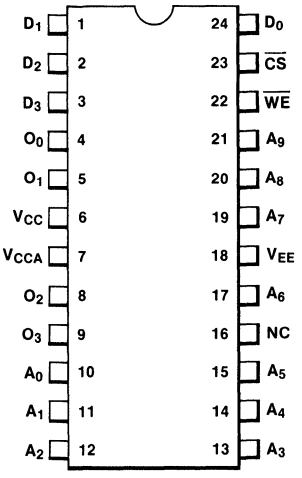
## Logic Symbol



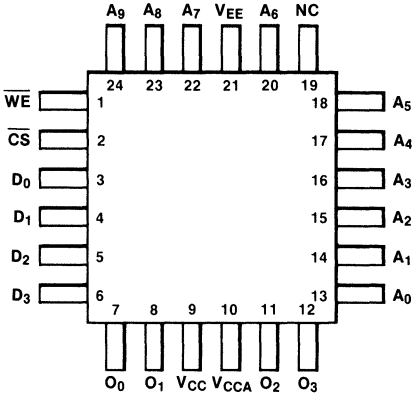

$V_{CC}$ = Pin 6 (9)
$V_{CCA}$ = Pin 7 (10)
$V_{EE}$ = Pin 18 (21)
( ) = Flatpak

## Connection Diagrams

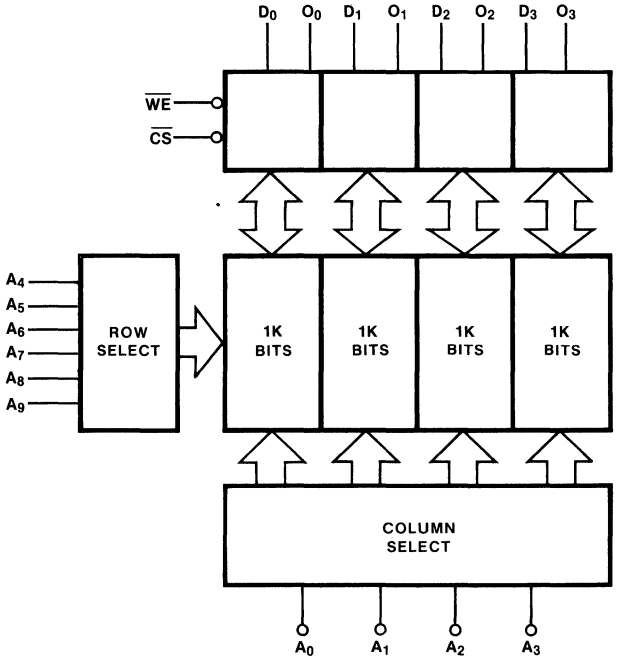
**24-Pin DIP** (Top View)




**24-Pin Flatpak** (Top View)



## Logic Diagram




### Functional Description

The F100474 is a fully decoded 4096-bit read/write random access memory, organized 1024 words by four bits. Word selection is achieved by means of a 10-bit address, $A_0$ through $A_9$.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at $D_0$–$D_3$ is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the outputs ($O_0$–$O_3$).

The output of the F100474 is an unterminated emitter follower, which allows maximum flexibility in choosing connection configurations. In many applications such as memory expansion, the outputs of many F100474 devices can be tied together. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is OFF.

### Truth Table

| Inputs | | | Outputs | |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | $D_n$ | $O_n$ | Mode |
| H | X | X | L | Not Selected |
| L | L | L | L | Write "0" |
| L | L | H | L | Write "1" |
| L | H | X | Data | Read |

H = HIGH Voltage Levels = −0.9 V (Nominal)
L = LOW Voltage Levels = −1.7 V (Nominal)
X = Don't Care
Data = Previously stored data

**DC Characteristics:** $V_{EE}$ = −4.2 V to −4.8 V, $V_{CC}$ = $V_{CCA}$ = GND, $T_C$ = 0°C to +85°C unless otherwise specified[1]

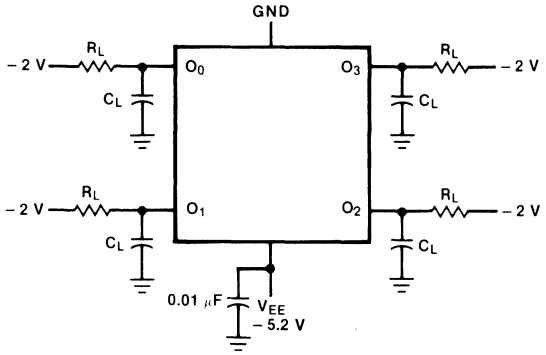
| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input HIGH Current | | | 220 | μA | $V_{IN} = V_{IH(max)}$ |
| $I_{IL}$ | Input LOW Current, $\overline{CS}$<br>$\overline{WE}$, $A_0$-$A_9$, D | 0.5<br>−50 | | 170 | μA | $V_{IN} = V_{IL(min)}$ |
| $I_{EE}$ | Power Supply Current | −195 | −160 | | mA | Inputs and Outputs Open |

**AC Characteristics:** $V_{EE}$ = −4.2 V to −4.8 V, $V_{CC}$ = $V_{CCA}$ = GND, Output Load = 50 Ω and 30 pF to −2.0 V, $T_C$ = 0°C to +85°C

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| | **Read Timing** | | | | | |
| $t_{ACS}$ | Chip Select Access Time | | | 15 | ns | |
| $t_{RCS}$ | Chip Select Recovery Time | | | 15 | ns | *Figures 3a, 3b* |
| $t_{AA}$ | Address Access Time[2] | | | 25 | ns | |
| | **Write Timing** | | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[3] | 16 | | | ns | |
| $t_{WSD}$ | Data Setup Time prior to Write | 5.0 | | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 5.0 | | | ns | |
| $t_{WSA}$ | Address Setup Time prior to Write[3] | 10 | | | ns | *Figure 4* |
| $t_{WHA}$ | Address Hold Time after Write | 4.0 | | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time prior to Write | 5.0 | | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 5.0 | | | ns | |
| $t_{WS}$ | Write Disable Time | | | 15 | ns | |
| $t_{WR}$ | Write Recovery Time | | | 20 | ns | |
| $t_r$ | Output Rise Time | | 5.0 | | ns | Measured between 20% and |
| $t_f$ | Output Fall Time | | 5.0 | | ns | 80% or 80% and 20% |
| $C_{IN}$ | Input Pin Capacitance | | 4.0 | 5.0 | pF | Measured with a Pulse |
| $C_{OUT}$ | Output Pin Capacitance | | 7.0 | 8.0 | pF | Technique |

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. $T_W$ measured at $t_{WSA}$ = Min, $t_{WSA}$ measured at $t_W$ = Min.

**Fig. 1 AC Test Circuit**




**Notes**
All Timing Measurements Referenced to 50% of Input Levels
$C_L$ = 30 pF including Fixture and Stray Capacitance
$R_L$ = 50 Ω to –2.0 V

**Fig. 2 Input Levels**

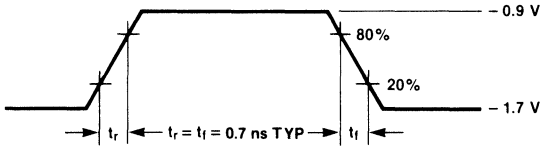
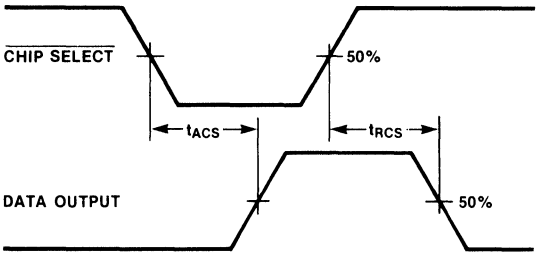
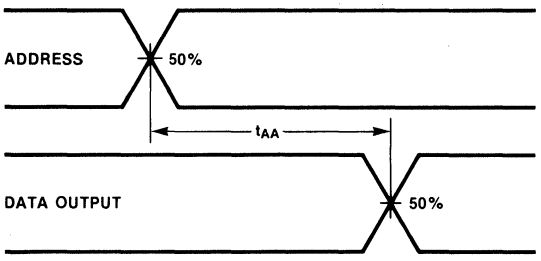



**Fig. 3 Read Mode Timing**

**a Read Mode Propagation Delay from Chip Select**

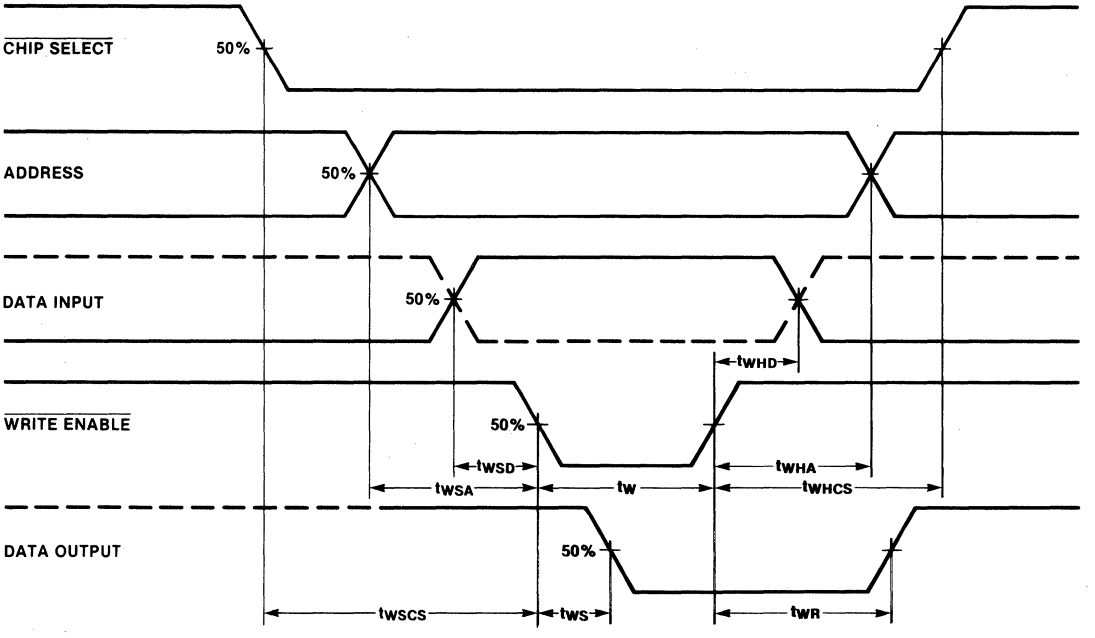



**b Read Mode Propagation Delay from Address**



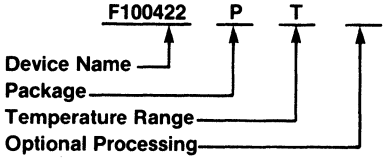

3

**Fig. 4 Write Mode Timing**




**Note**
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

## Ordering Information




**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak

**Temperature Ranges**
C = 0°C to +85°C, Case

**Optional Processing**
QR = 160 Hour Burn In

FAIRCHILD
A Schlumberger Company

# F100480
# 16,384 x 1-Bit Static Random Access Memory

Bipolar Division

F100K ECL Product



## Description

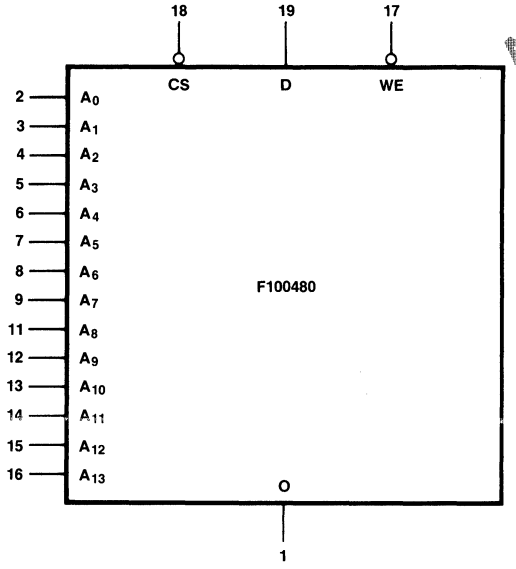
The F100480 is a 16,384-bit read/write Random Access Memory (RAM), organized 16,384 words by one bit per word and designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

- **Address Access Time — 25 ns Max**
- **Open-emitter Output for Easy Memory Expansion**
- **Power Dissipation — 0.043 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $\overline{WE}$ | Write Enable Input (Active LOW) |
| $\overline{CS}$ | Chip Select Input (Active LOW) |
| $A_0$-$A_{13}$ | Address Inputs |
| D | Data Input |
| O | Data Output |

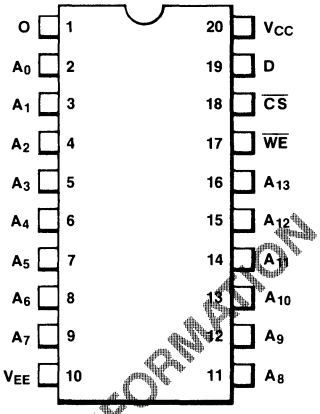
## Logic Symbol




$V_{CC}$ = Pin 20
$V_{EE}$ = Pin 10

## Connection Diagram

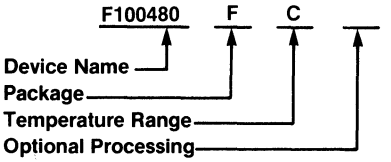
**20-Pin DIP** (Top View)




**Note**
The 20-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.



## Ordering Information

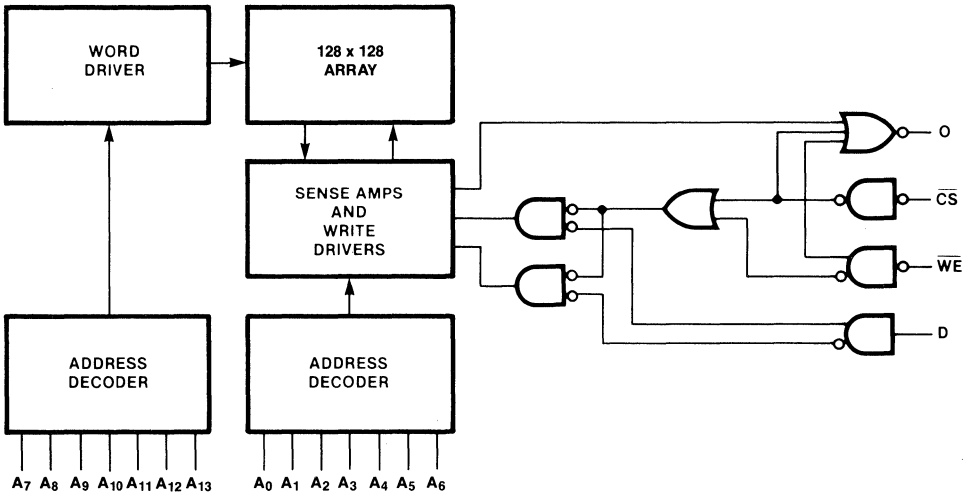



**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak

**Temperature Range**
C = 0°C to +85°C, Case

**Optional Processing**
QR = 160 Hour Burn In

## Logic Diagram




### Functional Description

The F100480 is a fully decoded 16,384-bit read/write random access memory, organized 16,384 words by one bit. Bit selection is achieved by means of a 14-bit address, $A_0$ through $A_{13}$.

One Chip Select input is provided for memory array expansion up to 32,768 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of Chip Select, ($\overline{CS}$) from the address without increasing address access time.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the output (O).

The output of the F100480 is an unterminated emitter follower, which allows maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F100480 devices together. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is OFF.

**Truth Table**

| Inputs | | | Output | |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | D | O | Mode |
| H | X | X | L | Not Selected |
| L | L | L | L | Write "0" |
| L | L | H | L | Write "1" |
| L | H | X | Data | Read |

H = HIGH Voltage Levels = −0.9 V (Nominal)
L = LOW Voltage Levels = −1.7 V (Nominal)
X = Don't Care
Data = Previously stored data

FAIRCHILD
A Schlumberger Company

# F10414
# 256 x 1-Bit Static Random Access Memory

Bipolar Division

F10K ECL Product

## Description

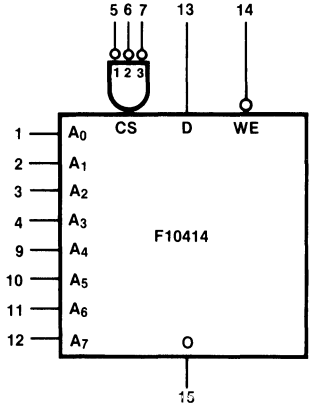
The F10414 is a 256-bit read/write Random Access Memory (RAM), organized 256 words by one bit. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as three active-LOW Chip Select lines.

- **Address Access Time — 10 ns Max**
- **Chip Select Access Time — 6.0 ns Max**
- **Open-emitter Output for Easy Memory Expansion**
- **Power Dissipation — 1.8 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $\overline{WE}$ | Write Enable Input (Active LOW) |
| $\overline{CS_1}$, $\overline{CS_2}$, $\overline{CS_3}$ | Chip Select Inputs (Active LOW) |
| $A_0$–$A_7$ | Address Inputs |
| D | Data Input |
| O | Data Output |

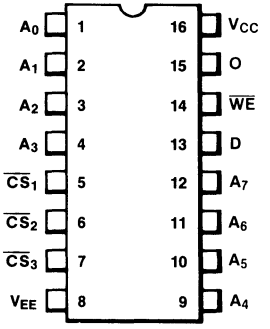
## Logic Symbol




$V_{CC}$ = Pin 16
$V_{EE}$ = Pin 8

## Connection Diagram

**16-Pin DIP** (Top View)

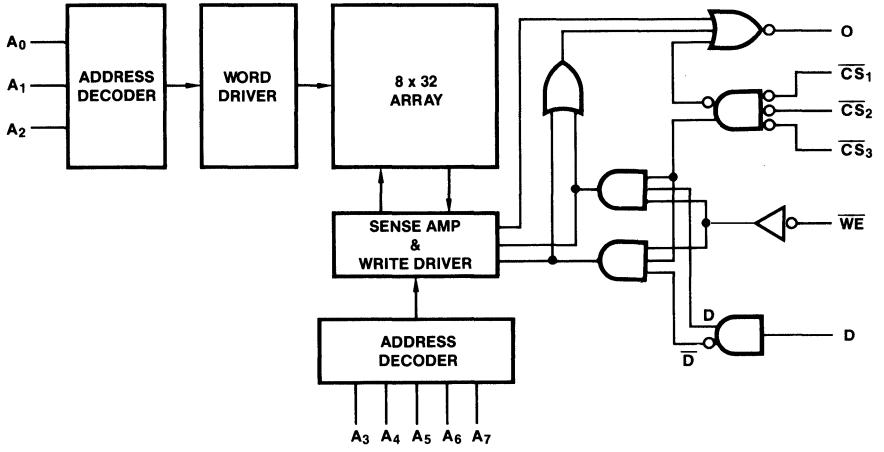



**Note**

The 16-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

3

## Logic Diagram




### Functional Description

The F10414 is a fully decoded 256-bit read/write random access memory, organized 256 words by one bit. Bit selection is achieved by means of an 8-bit address, $A_0$ through $A_7$.

Three active-LOW Chip Select inputs are provided for increased logic flexibility. This permits memory array expansion up to 2048 words with the F10170 decoder. For larger memories, the fast chip select access time permits the decoding of Chip Select, $\overline{CS}$, from the address without affecting system performance.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the output (O).

The output of the F10414 is an unterminated emitter follower, which allows maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F10414 devices together to allow easy expansion. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output.

### Truth Table

| Inputs | | | | | Output | |
|---|---|---|---|---|---|---|
| $\overline{CS_1}$ | $\overline{CS_2}$ | $\overline{CS_3}$ | $\overline{WE}$ | D | O | Mode |
| X | X | H* | X | X | L | Not Selected |
| L | L | L | L | L | L | Write "0" |
| L | L | L | L | H | L | Write "1" |
| L | L | L | H | X | Data | Read |

H = HIGH Voltage Levels = −0.9 V (Nominal)
L = LOW Voltage Levels = −1.7 V (Nominal)
X = Don't Care
Data = Previously stored data
*One or more Chip Selects HIGH

**DC Characteristics:** $V_{EE} = -5.2$ V, $V_{CC}$ = GND, $T_A = 0°C$ to $+75°C$ unless otherwise specified[1]

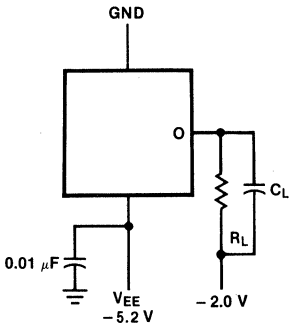
| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input HIGH Current | | | 220 | μA | $V_{IN} = V_{IH(max)}$ |
| $I_{IL}$ | Input LOW Current, $\overline{CS}_n$<br>$\overline{WE}$, $A_0$-$A_7$, D | 0.5<br>−50 | | 170 | μA | $V_{IN} = V_{IL(min)}$ |
| $I_{EE}$ | Power Supply Current | −140 | −100 | | mA | Inputs and Output Open |

**AC Characteristics:** $V_{EE} = -5.2$ V ±5%, $V_{CC}$ = GND, Output Load = 50 Ω and 30 pF to −2.0 V, $T_A = 0°C$ to $+75°C$

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| | **Read Timing** | | | | | |
| $t_{ACS}$ | Chip Select Access Time | | | 6.0 | ns | |
| $t_{RCS}$ | Chip Select Recovery Time | | | 6.0 | ns | *Figures 3a, 3b* |
| $t_{AA}$ | Address Access Time[2] | | | 10 | ns | |
| | **Write Timing** | | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[3] | 7.0 | | | ns | |
| $t_{WSD}$ | Data Setup Time prior to Write | 1.0 | | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 2.0 | | | ns | |
| $t_{WSA}$ | Address Setup Time[3] prior to Write | 1.0 | | | ns | *Figure 4* |
| $t_{WHA}$ | Address Hold Time after Write | 2.0 | | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time prior to Write | 1.0 | | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 2.0 | | | ns | |
| $t_{WS}$ | Write Disable Time | | | 8.0 | ns | |
| $t_{WR}$ | Write Recovery Time | | | 10 | ns | |
| $t_r$ | Output Rise Time | | 3.0 | | ns | Measured between 20% and |
| $t_f$ | Output Fall Time | | 3.0 | | ns | 80% or 80% and 20% |
| $C_{IN}$ | Input Pin Capacitance | | 4.0 | 5.0 | pF | Measured with a Pulse |
| $C_{OUT}$ | Output Pin Capacitance | | 7.0 | 8.0 | pF | Technique |

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. $T_W$ measured at $t_{WSA}$ = Min, $t_{WSA}$ measured at $t_W$ = Min.

**Fig. 1 AC Test Circuit**




**Notes**
All Timing Measurements Referenced to 50% of Input Levels
$C_L$ = 30 pF including Fixture and Stray Capacitance
$R_L$ = 50 Ω to −2.0 V.

**Fig. 2 Input Levels**

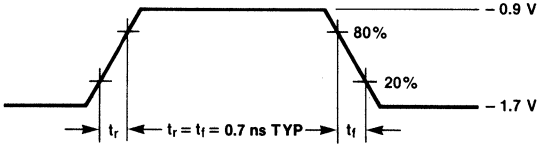
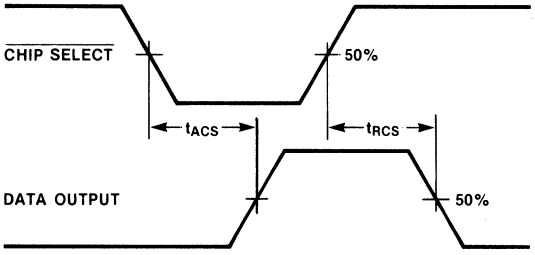



**Fig. 3 Read Mode Timing**

**a Read Mode Propagation Delay from Chip Select**




**b Read Mode Propagation Delay from Address**

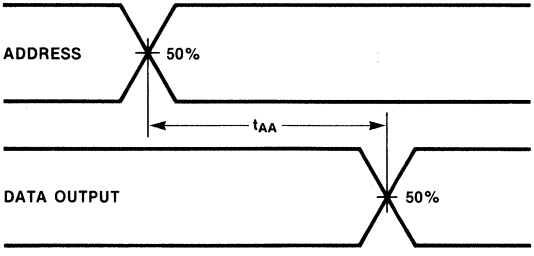
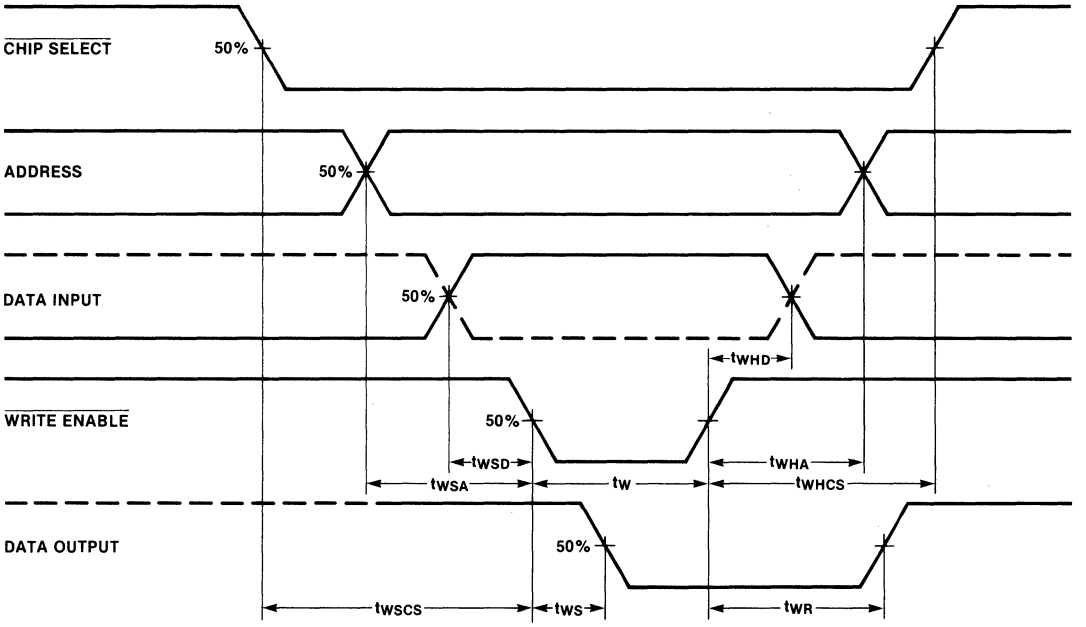
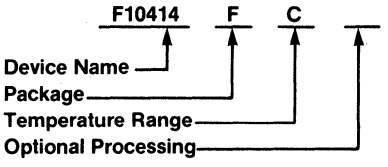


**Fig. 4 Write Mode Timing**




**Note**
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

## Ordering Information



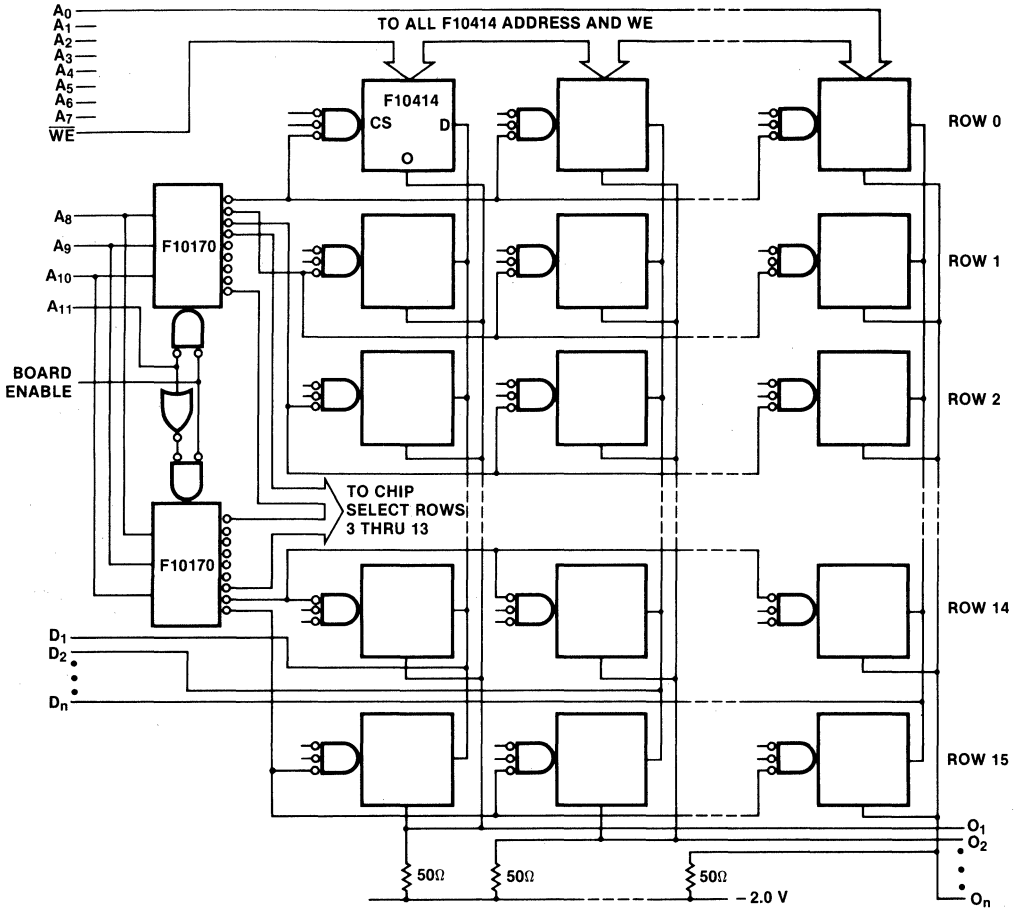

**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak
P = Plastic DIP

**Temperature Ranges**
C = 0°C to +75°C, Ambient

**Optional Processing**
QR = 160 Hour Burn In

## Typical Application

### 4096-Word x n-Bit System



FAIRCHILD
A Schlumberger Company

# F10415
# 1024 x 1-Bit Static Random Access Memory

Advanced Bipolar Division

F10K ECL Product

## Description

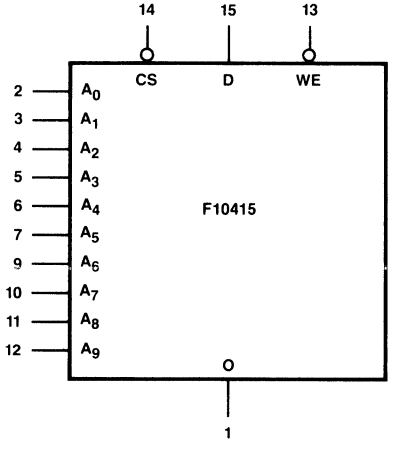
The F10415 is a 1024-bit read/write Random Access Memory (RAM), organized as 1024 words by one bit per word and designed for high-speed scratchpad, control and buffer storage applications. It is available in two speed versions, the F10415 and F10415A. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

- **Address Access Time**
  **F10415 — 35 ns Max**
  **F10415A — 20 ns Max**
- **Chip Select Access Time**
  **F10415 — 10 ns Max**
  **F10415A — 8.0 ns Max**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation — 0.5 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $\overline{WE}$ | Write Enable Input (Active LOW) |
| $\overline{CS}$ | Chip Select Input (Active LOW) |
| $A_0$–$A_9$ | Address Inputs |
| D | Data Input |
| O | Data Output |

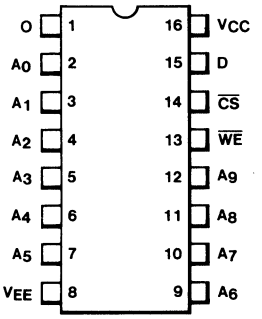
## Logic Symbol




$V_{CC}$ = Pin 16
$V_{EE}$ = Pin 8

## Connection Diagram

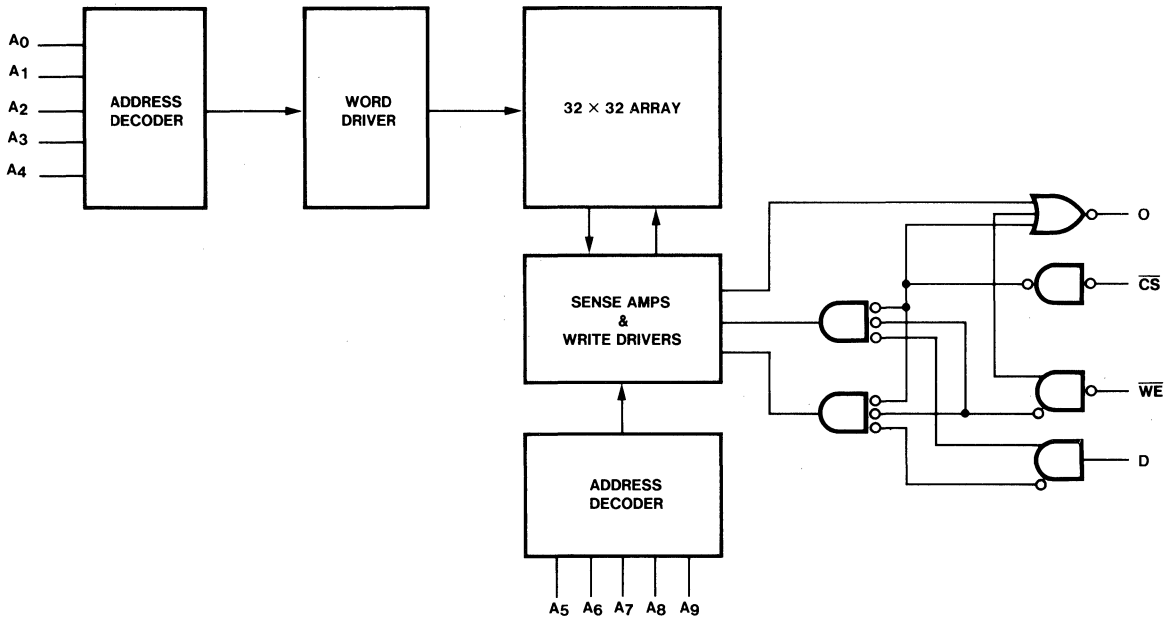
**16-Pin DIP** (Top View)




**Note**
The 16-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package

3

## Logic Diagram




### Functional Description

The F10415 is a fully decoded 1024-bit read/write random access memory, organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, $A_0$ through $A_9$.

One Chip Select input is provided for memory array expansion up to 2048 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of Chip Select, ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the output (O).

The output of the F10415 is an unterminated emitter follower, which allows maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F10415 devices together to allow easy expansion. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output.

**Truth Table**

| Inputs | | | Output | Mode |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | D | O | |
| H | X | X | L | Not Selected |
| L | L | L | L | Write "0" |
| L | L | H | L | Write "1" |
| L | H | X | Data | Read |

H = HIGH Voltage Levels = −0.9 V (Nominal)
L = LOW Voltage Levels = −1.7 V (Nominal)
X = Don't Care
Data = Previously stored data

**DC Characteristics:** $V_{EE} = -5.2$ V, $V_{CC}$ = GND, $T_A = 0°C$ to $+75°C$ unless otherwise specified[1]

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input HIGH Current | | | 220 | μA | $V_{IN} = V_{IH(max)}$ |
| $I_{IL}$ | Input LOW Current, $\overline{CS}$<br>$\overline{WE}$, $A_0$-$A_9$, D | 0.5<br>−50 | | 170 | μA | $V_{IN} = V_{IL(min)}$ |
| $I_{EE}$ | Power Supply Current | −150 | −105 | | mA | Inputs and Output Open |

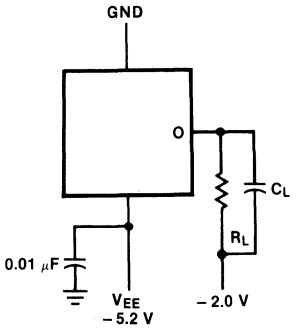
**AC Characteristics:** $V_{EE} = -5.2$ V ±5%, $V_{CC}$ = GND, Output Load = 50 Ω and 30 pF to −2.0 V, $T_A = 0°C$ to $+75°C$

| Symbol | Characteristic | F10415 Min | F10415 Max | F10415A Min | F10415A Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | **Read Timing** | | | | | | |
| $t_{ACS}$ | Chip Select Access Time | | 10 | | 8.0 | ns | |
| $t_{RCS}$ | Chip Select Recovery Time | | 10 | | 8.0 | ns | *Figures 3a, 3b* |
| $t_{AA}$ | Address Access Time[2] | | 35 | | 20 | ns | |
| | **Write Timing** | | | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[3] | 25 | | 14 | | ns | |
| $t_{WSD}$ | Data Setup Time prior to Write | 5.0 | | 4.0 | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 5.0 | | 4.0 | | ns | |
| $t_{WSA}$ | Address Setup Time prior to Write[3] | 8.0 | | 5.0 | | ns | *Figure 4* |
| $t_{WHA}$ | Address Hold Time after Write | 4.0 | | 3.0 | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time prior to Write | 5.0 | | 4.0 | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 5.0 | | 4.0 | | ns | |
| $t_{WS}$ | Write Disable Time | | 10 | | 10 | ns | |
| $t_{WR}$ | Write Recovery Time | | 20 | | 20 | ns | |

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $t_r$ | Output Rise Time | | 5.0 | | ns | Measured between 20% and |
| $t_f$ | Output Fall Time | | 5.0 | | ns | 80% or 80% and 20% |
| $C_{IN}$ | Input Pin Capacitance | | 4.0 | 5.0 | pF | Measured with a Pulse |
| $C_{OUT}$ | Output Pin Capacitance | | 7.0 | 8.0 | pF | Technique |

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. $T_W$ measured at $t_{WSA}$ = Min, $t_{WSA}$ measured at $t_W$ = Min.

**Fig. 1 AC Test Circuit**




**Notes**
All Timing Measurements Referenced to 50% of Input Levels
$C_L$ = 30 pF including Fixture and Stray Capacitance
$R_L$ = 50 Ω to –2.0 V

**Fig. 2 Input Levels**

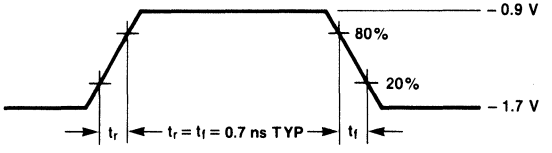
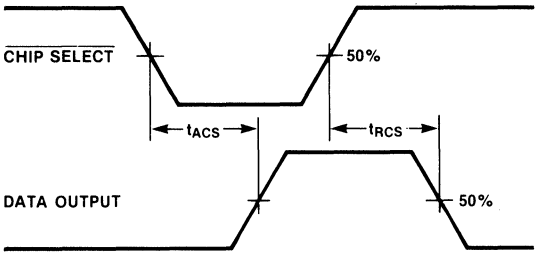



**Fig. 3 Read Mode Timing**

**a Read Mode Propagation Delay from Chip Select**




**b Read Mode Propagation Delay from Address**

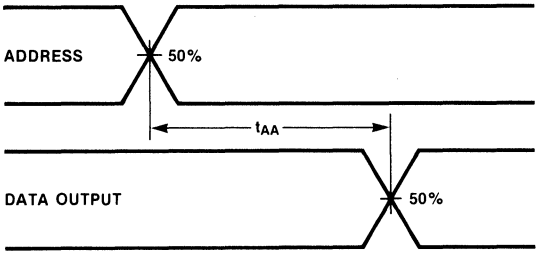
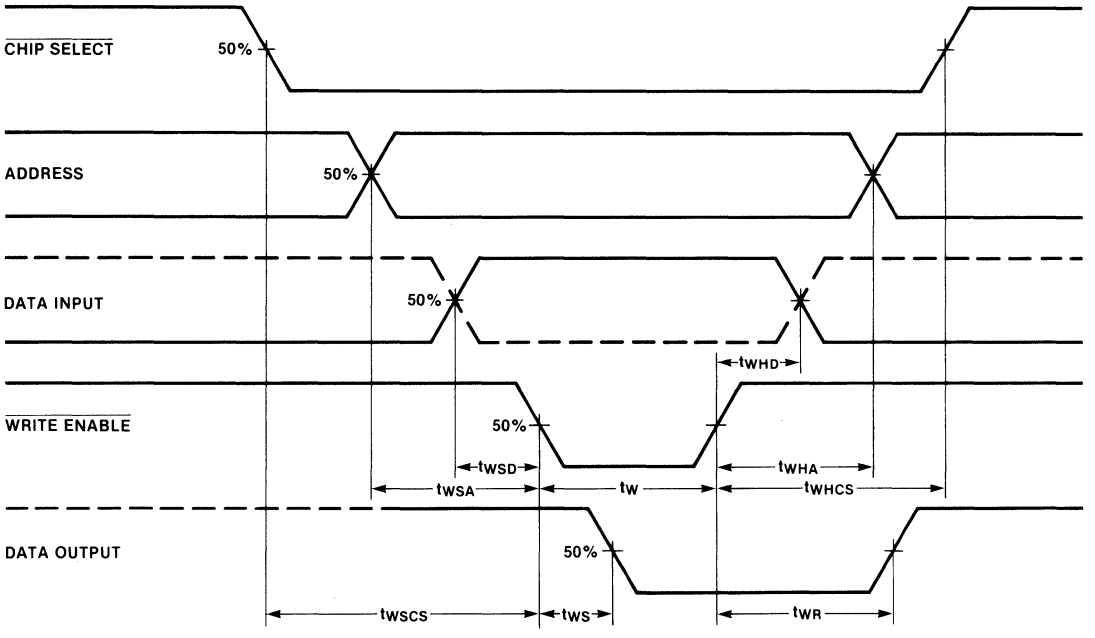
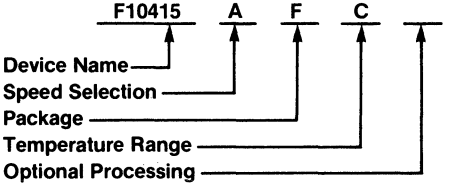


**Fig. 4 Write Mode Timing**




**Note**
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

## Ordering Information




**Speed Selection**
Blank = Standard Speed
A = 'A' Grade

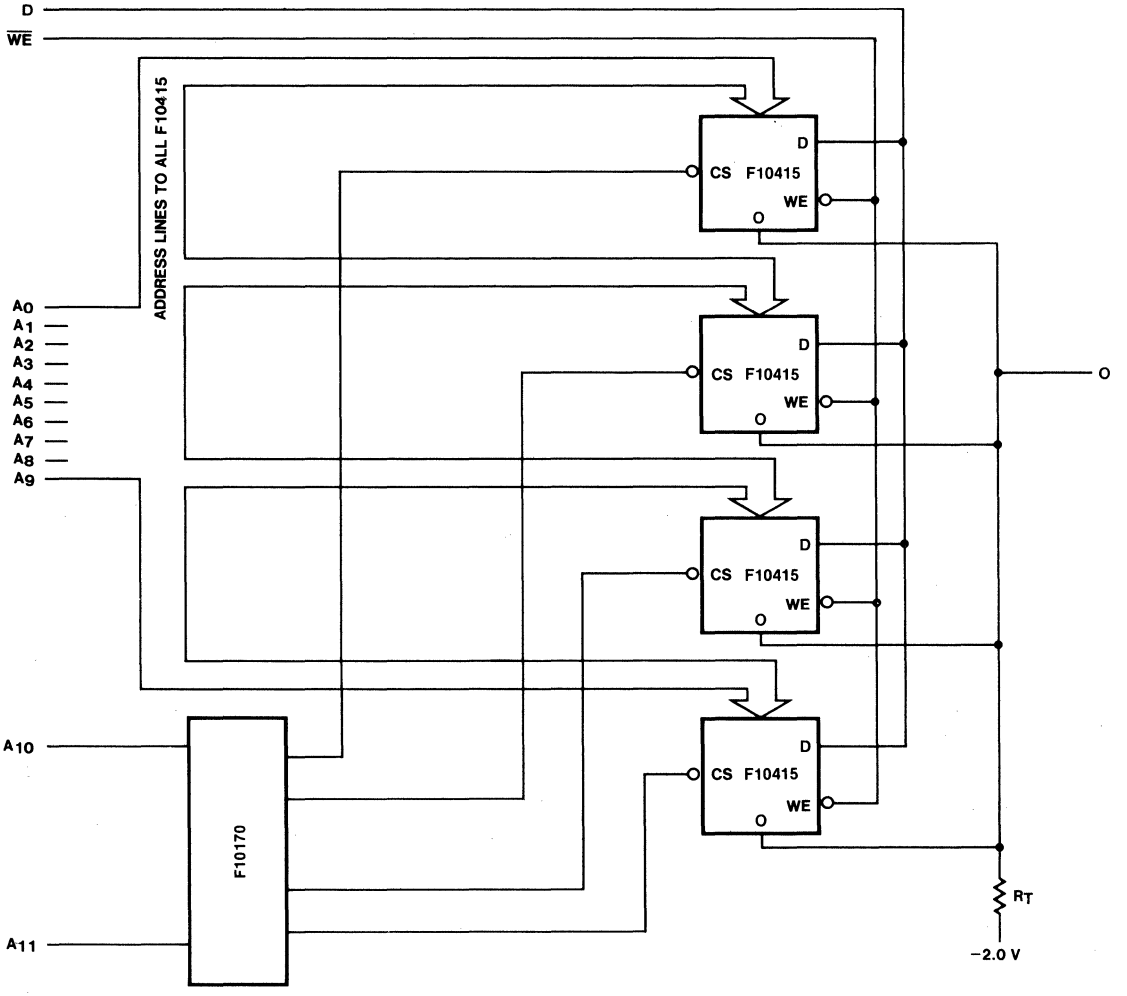
**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak
P = Plastic DIP

**Temperature Range**
C = 0°C to +75°C, Ambient

**Optional Processing**
QR = 160 Hour Burn In

## Typical Application

### 4096-Word x n-Bit System



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# F10422
# 256 x 4-Bit Static Random Access Memory

Bipolar Division

F10K ECL Product

## Description

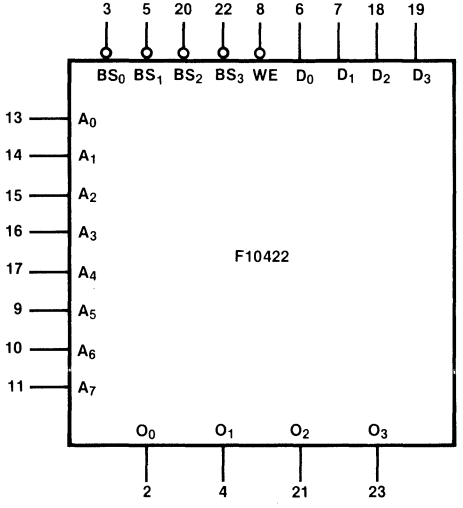
The F10422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits per word. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as four active-LOW Bit Select lines.

- **Address Access Time — 10 ns Max**
- **Bit Select Access Time — 5.0 ns Max**
- **Four Bits Can be Independently Selected**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation — 0.92 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $\overline{WE}$ | Write Enable Input (Active LOW) |
| $\overline{BS}_0 - \overline{BS}_3$ | Bit Select Inputs (Active LOW) |
| $A_0 - A_7$ | Address Inputs |
| $D_0 - D_3$ | Data Inputs |
| $O_0 - O_3$ | Data Outputs |

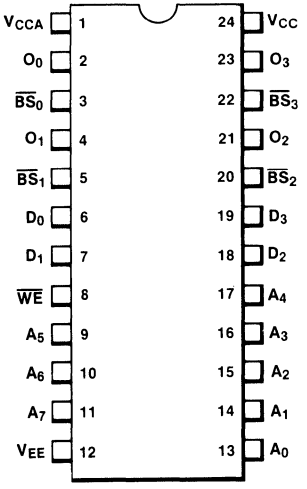
## Logic Symbol




$V_{CC}$ = Pin 24
$V_{CCA}$ = Pin 1
$V_{EE}$ = Pin 12

## Connection Diagram

**24-Pin DIP** (Top View)

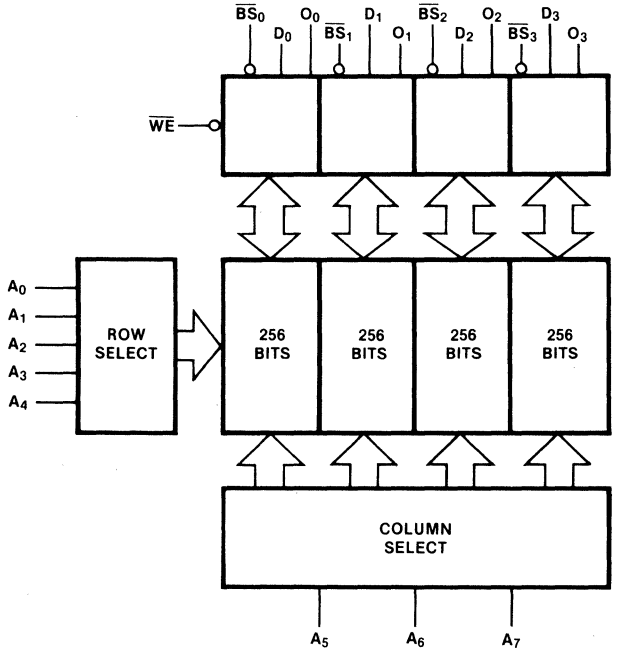



**Note**

The 24-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

3

## Logic Diagram




### Functional Description

The F10422 is a fully decoded 1024-bit read/write random access memory, organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, $A_0$ through $A_7$.

Four Bit Select inputs are provided for logic flexibility. For larger memories, the fast bit select access time permits the decoding of individual bit selects from the address without increasing address access time.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the bit selected, the data at $D_0$-$D_3$ is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the bit selected. Non-inverted data is then presented at the output ($O_0$-$O_3$).

The output of the F10422 is an unterminated emitter follower, which allows maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F10422 devices together to allow easy expansion. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output.

### Truth Table

| Inputs | | | Outputs | |
|---|---|---|---|---|
| $\overline{BS}_n$ | $\overline{WE}$ | $D_n$ | $O_n$ | Mode |
| H | X | X | L | Not Selected |
| L | L | L | L | Write "0" |
| L | L | H | L | Write "1" |
| L | H | X | Data | Read |

Each bit has independent $\overline{BS}$, D, and O, but all have common $\overline{WE}$
H = HIGH Voltage Levels = −0.9 V (Nominal)
L = LOW Voltage Levels = −1.7 V (Nominal)
X = Don't Care
Data = Previously stored data

**DC Characteristics:** $V_{EE} = -5.2$ V, $V_{CC} = V_{CCA} = GND$, $T_A = 0°C$ to $+75°C$ unless otherwise specified[1]

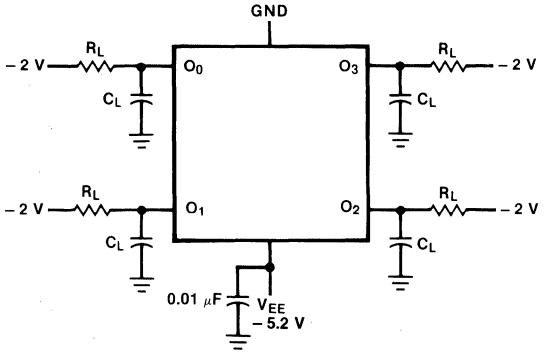
| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input HIGH Current | | | 220 | μA | $V_{IN} = V_{IH(max)}$ |
| $I_{IL}$ | Input LOW Current, $\overline{BS_0}$-$\overline{BS_3}$<br>$\overline{WE}$, $A_0$-$A_7$, $D_0$-$D_3$ | 0.5<br>−50 | | 170 | μA | $V_{IN} = V_{IL(min)}$ |
| $I_{EE}$ | Power Supply Current | −200 | −180 | | mA | All Inputs and Outputs Open |

**AC Characteristics:** $V_{EE} = -5.2$ V ±5%, $V_{CC} = V_{CCA} = GND$, Output Load = 50 Ω and 30 pF to −2.0 V, $T_A = 0°C$ to $+75°C$

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| | **Read Timing** | | | | | |
| $t_{ACS}$ | Chip Select Access Time | | | 5.0 | ns | |
| $t_{RCS}$ | Chip Select Recovery Time | | | 5.0 | ns | *Figures 3a, 3b* |
| $t_{AA}$ | Address Access Time[2] | | | 10 | ns | |
| | **Write Timing** | | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[3] | 7.0 | | | ns | |
| $t_{WSD}$ | Data Setup Time prior to Write | 1.0 | | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 2.0 | | | ns | |
| $t_{WSA}$ | Address Setup Time prior to Write[3] | 1.0 | | | ns | *Figure 4* |
| $t_{WHA}$ | Address Hold Time after Write | 2.0 | | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time prior to Write | 1.0 | | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 2.0 | | | ns | |
| $t_{WS}$ | Write Disable Time | | | 5.0 | ns | |
| $t_{WR}$ | Write Recovery Time | | | 12 | ns | |
| $t_r$ | Output Rise Time | | 3.0 | | ns | Measured between 20% and |
| $t_f$ | Output Fall Time | | 3.0 | | ns | 80% or 80% and 20% |
| $C_{IN}$ | Input Pin Capacitance | | 4.0 | 5.0 | pF | Measured with a Pulse |
| $C_{OUT}$ | Output Pin Capacitance | | 7.0 | 8.0 | pF | Technique |

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. $T_W$ measured at $t_{WSA}$ = Min, $t_{WSA}$ measured at $t_W$ = Min.

**Fig. 1 AC Test Circuit**




**Notes**
All Timing Measurements Referenced to 50% of Input Levels
$C_L$ = 30 pF including Fixture and Stray Capacitance
$R_L$ = 50 Ω to –2.0 V

**Fig. 2 Input Levels**

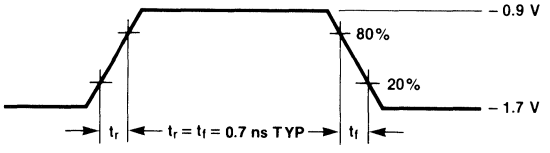
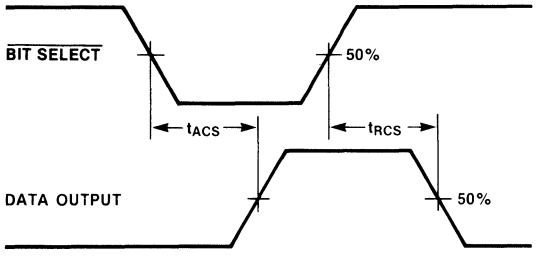



**Fig. 3 Read Mode Timing**

**a Read Mode Propagation Delay from Bit Select**




**b Read Mode Propagation Delay from Address**

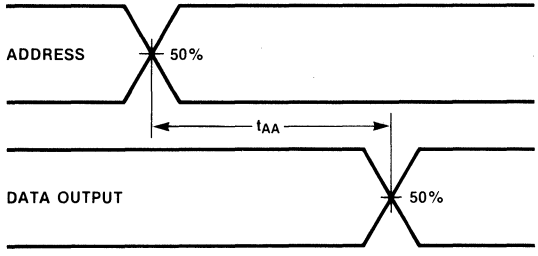
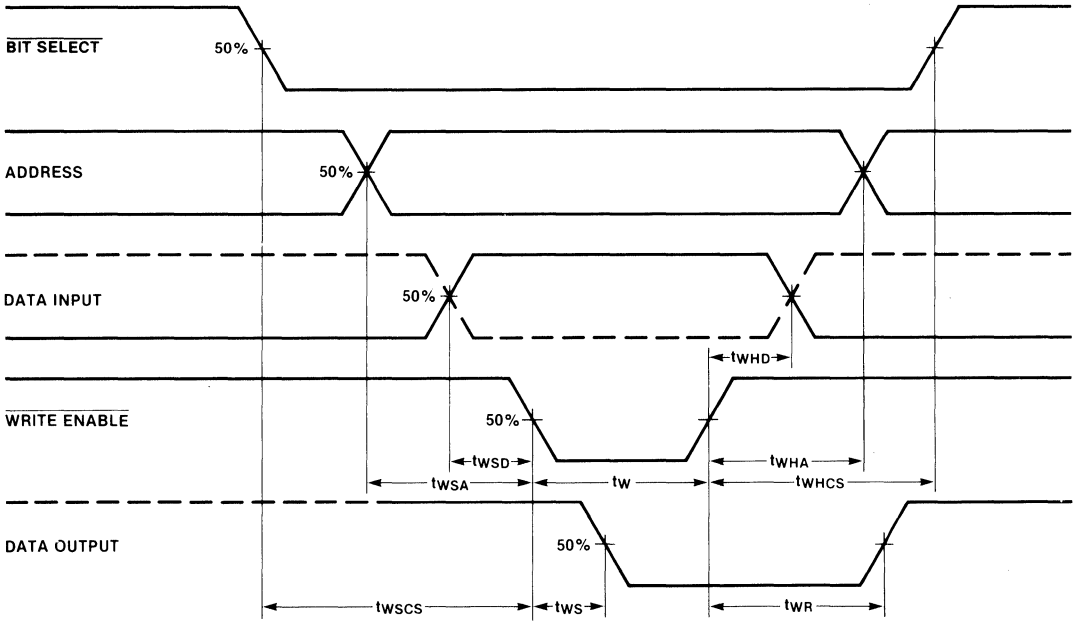
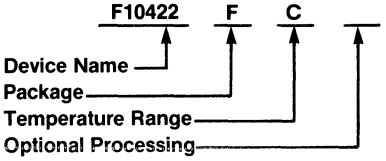


**Fig. 4 Write Mode Timing**




**Note**
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

## Ordering Information




**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak

**Temperature Ranges**
C = 0°C to +75°C, Ambient

**Optional Processing**
QR = 160 Hour Burn In

FAIRCHILD
A Schlumberger Company

# F10470
# 4096 x 1-Bit Static Random Access Memory

Bipolar Division

F10K ECL Product

## Description

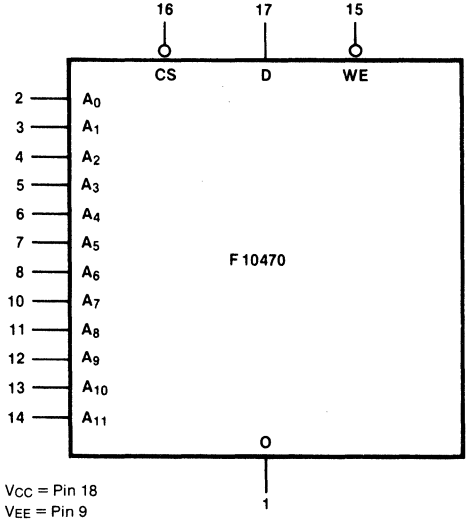
The F10470 is a 4096-bit read/write Random Access Memory (RAM), organized 4096 words by one bit per word and designed for high-speed scratchpad, control and buffer storage applications. It is available in two speed versions, the F10470 and F10470A. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

- **Address Access Time**
  - **F10470 — 35 ns Max**
  - **F10470A — 25 ns Max**
- **Chip Select Access Time**
  - **F10470 — 15 ns Max**
  - **F10470A — 10 ns Max**
- **Open-emitter Output for Easy Memory Expansion**
- **Power Dissipation — 0.20 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $\overline{WE}$ | Write Enable Input (Active LOW) |
| $\overline{CS}$ | Chip Select Input (Active LOW) |
| $A_0$–$A_{11}$ | Address Inputs |
| D | Data Input |
| O | Data Output |

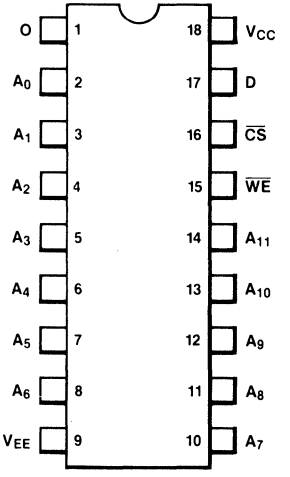
## Logic Symbol




$V_{CC}$ = Pin 18
$V_{EE}$ = Pin 9

## Connection Diagram

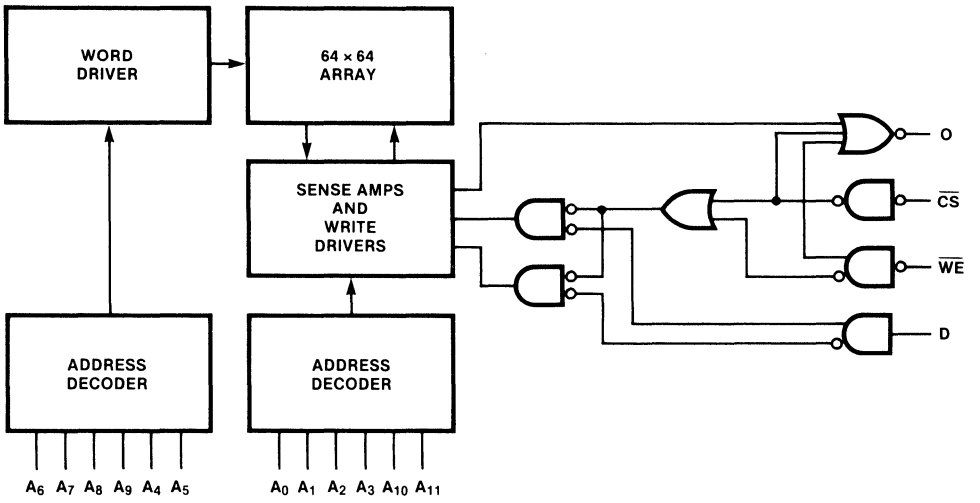
**18-Pin DIP** (Top View)




**Note**

The 18-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

**Logic Diagram**




**Functional Description**

The F10470 is a fully decoded 4096-bit read/write random access memory, organized 4096 words by one bit. Bit selection is achieved by means of a 12-bit address, $A_0$ through $A_{11}$.

One Chip Select input is provided for memory array expansion up to 8196 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of Chip Select, ($\overline{CS}$) from the address without increasing address access time.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the output (O).

The output of the F10470 is an unterminated emitter follower, which allows maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F10470 devices together. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is OFF.

**Truth Table**

| Inputs | | | Output | |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | D | O | Mode |
| H | X | X | L | Not Selected |
| L | L | L | L | Write "0" |
| L | L | H | L | Write "1" |
| L | H | X | Data | Read |

H = HIGH Voltage Levels = −0.9 V (Nominal)
L = LOW Voltage Levels = −1.7 V (Nominal)
X = Don't Care
Data = Previously stored data

**DC Characteristics:** $V_{EE} = -5.2$ V, $V_{CC}$ = GND, $T_A = 0°C$ to $+75°C$ unless otherwise specified[1]

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input HIGH Current | | | 220 | μA | $V_{IN} = V_{IH(max)}$ |
| $I_{IL}$ | Input LOW Current, $\overline{CS}$<br>$\overline{WE}$, $A_0$-$A_{11}$, D | 0.5<br>−50 | | 170 | μA | $V_{IN} = V_{IL(min)}$ |
| $I_{EE}$ | Power Supply Current | −200 | −160 | | mA | Inputs and Output Open |

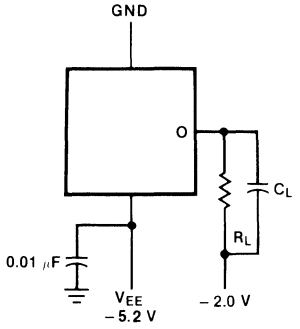
**AC Characteristics:** $V_{EE} = -5.2$ V ±5%, $V_{CC}$ = GND, Output Load = 50 Ω and 30 pF to −2.0 V, $T_A = 0°C$ to $+75°C$

| Symbol | Characteristic | F10470 Min | F10470 Max | F10470A Min | F10470A Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | **Read Timing** | | | | | | |
| $t_{ACS}$ | Chip Select Access Time | | 15 | | 10 | ns | |
| $t_{RCS}$ | Chip Select Recovery Time | | 15 | | 10 | ns | *Figures 3a, 3b* |
| $t_{AA}$ | Address Access Time[2] | | 35 | | 25 | ns | |
| | **Write Timing** | | | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[3] | 25 | | 15 | | ns | |
| $t_{WSD}$ | Data Setup Time prior to Write | 5.0 | | 5.0 | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 5.0 | | 5.0 | | ns | |
| $t_{WSA}$ | Address Setup Time prior to Write[3] | 10 | | 10 | | ns | *Figure 4* |
| $t_{WHA}$ | Address Hold Time after Write | 5.0 | | 5.0 | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time prior to Write | 5.0 | | 5.0 | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 5.0 | | 5.0 | | ns | |
| $t_{WS}$ | Write Disable Time | | 15 | | 15 | ns | |
| $t_{WR}$ | Write Recovery Time | | 20 | | 20 | ns | |

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $t_r$ | Output Rise Time | | 5.0 | | ns | Measured between 20% and |
| $t_f$ | Output Fall Time | | 5.0 | | ns | 80% or 80% and 20% |
| $C_{IN}$ | Input Pin Capacitance | | 4.0 | 5.0 | pF | Measured with a Pulse |
| $C_{OUT}$ | Output Pin Capacitance | | 7.0 | 8.0 | pF | Technique |

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. $T_W$ measured at $t_{WSA}$ = Min, $t_{WSA}$ measured at $t_W$ = Min.

**Fig. 1 AC Test Circuit**




**Notes**
All Timing Measurements Referenced to 50% of Input Levels
$C_L$ = 30 pF including Fixture and Stray Capacitance
$R_L$ = 50 Ω to −2.0 V.

**Fig. 2 Input Levels**

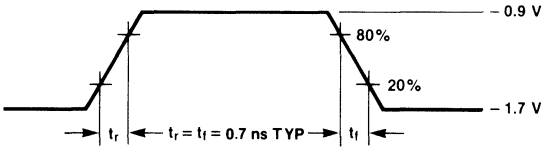
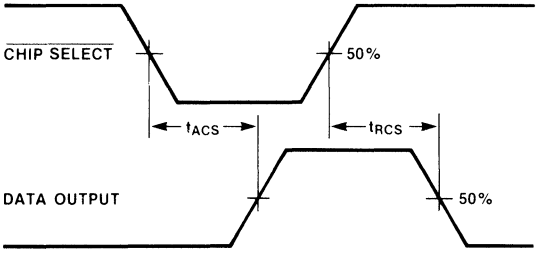
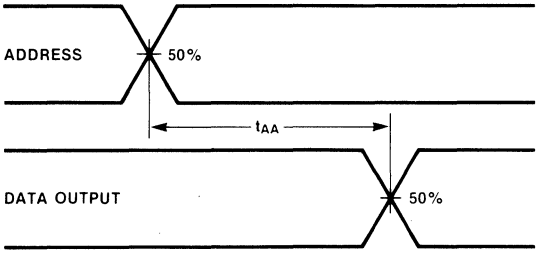



**Fig. 3 Read Mode Timing**

**a Read Mode Propagation Delay from Chip Select**

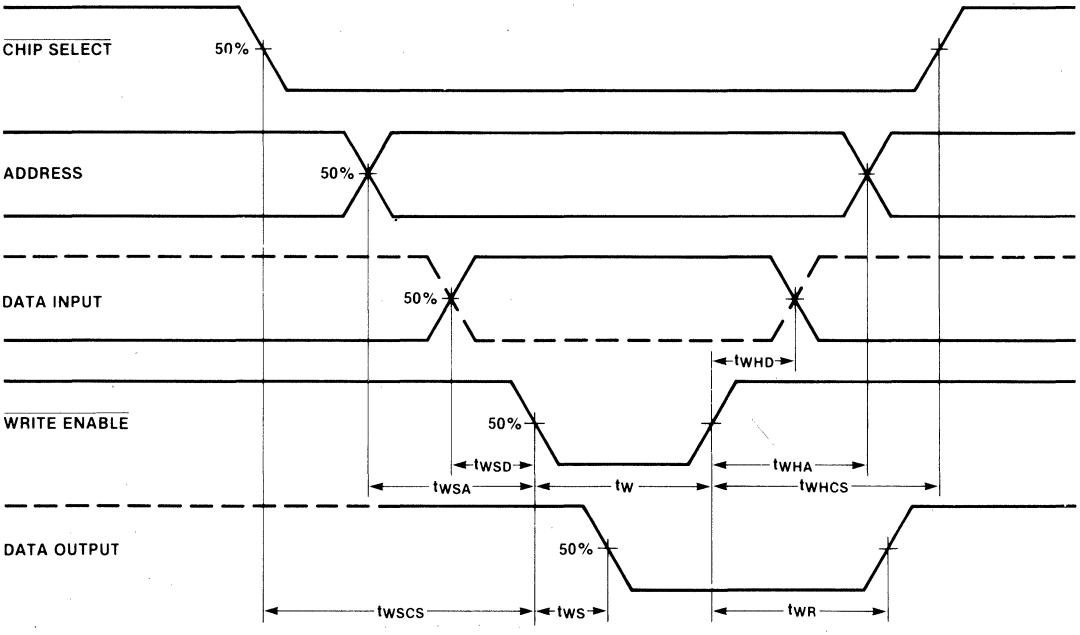



**b Read Mode Propagation Delay from Address**



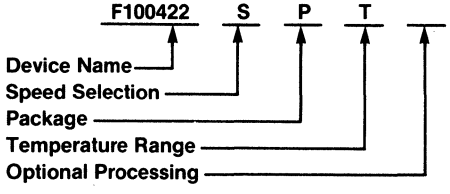

3

**Fig. 4 Write Mode Timing**




**Note**
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

## Ordering Information




**Speed Selection**
Blank = Standard Speed
A = 'A' Grade

**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak

**Temperature Range**
C = 0°C to +75°C, Ambient

**Optional Processing**
QR = 160 Hour Burn In

FAIRCHILD
A Schlumberger Company

# F10474
# 1024 x 4-Bit Static Random Access Memory

Bipolar Division

F10K ECL Product

## Description

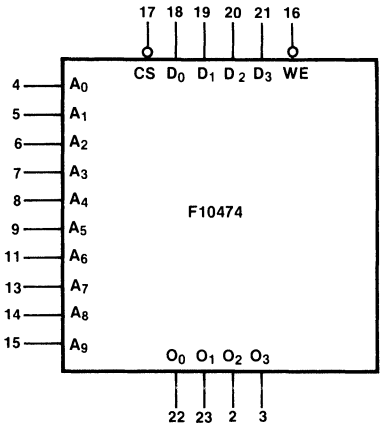
The F10474 is a 4096-bit read/write Random Access Memory (RAM), organized 1024 words by four bits per word. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

- **Address Access Time — 25 ns Max**
- **Chip Select Access Time — 15 ns Max**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation — 0.20 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $\overline{WE}$ | Write Enable Input (Active LOW) |
| $\overline{CS}$ | Chip Select Input (Active LOW) |
| $A_0$-$A_9$ | Address Inputs |
| $D_0$-$D_3$ | Data Inputs |
| $O_0$-$O_3$ | Data Outputs |

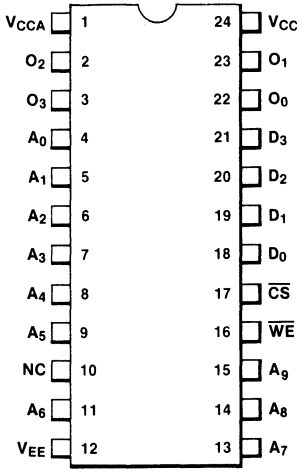
## Logic Symbol




$V_{CC}$ = Pin 24
$V_{CCA}$ = Pin 1
$V_{EE}$ = Pin 12
NC = Pin 10

## Connection Diagram

**24-Pin DIP** (Top View)

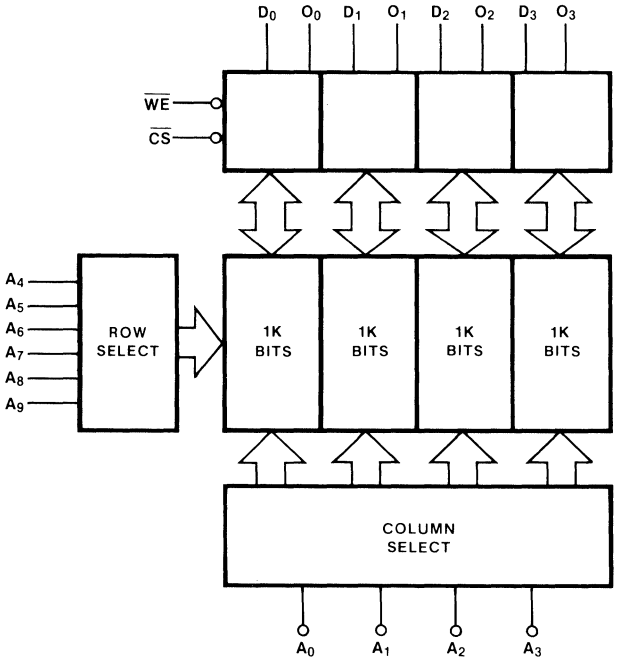



**Note**

The 24-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

3

## Logic Diagram




### Functional Description

The F10474 is a fully decoded 4096-bit read/write random access memory, organized 1024 words by four bits. Word selection is achieved by means of a 10-bit address, $A_0$ through $A_9$.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at $D_0$-$D_3$ is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the outputs ($O_0$-$O_3$).

The output of the F10474 is an unterminated emitter follower, which allows maximum flexibility in choosing connection configurations. In many applications such as memory expansion, the outputs of many F10474 devices can be tied together. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is OFF.

### Truth Table

| Inputs | | | Outputs | |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | $D_n$ | $O_n$ | Mode |
| H | X | X | L | Not Selected |
| L | L | L | L | Write "0" |
| L | L | H | L | Write "1" |
| L | H | X | Data | Read |

H = HIGH Voltage Levels = −0.9 V (Nominal)
L = LOW Voltage Levels = −1.7 V (Nominal)
X = Don't Care
Data = Previously stored data

**DC Characteristics:** $V_{EE} = -5.2$ V, $V_{CC} = V_{CCA} = GND$, $T_A = 0°C$ to $+75°C$ unless otherwise specified[1]

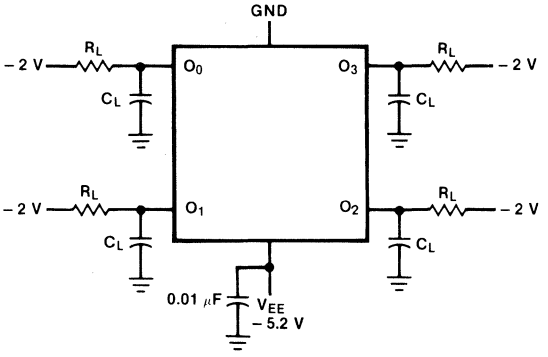
| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input HIGH Current | | | 220 | μA | $V_{IN} = V_{IH(max)}$ |
| $I_{IL}$ | Input LOW Current, $\overline{CS}$<br>$\overline{WE}$, $A_0$-$A_9$, D | 0.5<br>−50 | | 170 | μA | $V_{IN} = V_{IL(min)}$ |
| $I_{EE}$ | Power Supply Current | −200 | −160 | | mA | Inputs and Outputs Open |

**AC Characteristics:** $V_{EE} = -5.2$ V ±5%, $V_{CC} = V_{CCA} = GND$, Output Load = 50 Ω and 30 pF to −2.0 V, $T_A = 0°C$ to $+75°C$

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| | **Read Timing** | | | | | |
| $t_{ACS}$ | Chip Select Access Time | | | 15 | ns | |
| $t_{RCS}$ | Chip Select Recovery Time | | | 15 | ns | *Figures 3a, 3b* |
| $t_{AA}$ | Address Access Time[2] | | | 25 | ns | |
| | **Write Timing** | | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[3] | 16 | | | ns | |
| $t_{WSD}$ | Data Setup Time prior to Write | 5.0 | | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 5.0 | | | ns | |
| $t_{WSA}$ | Address Setup Time prior to Write[3] | 10 | | | ns | *Figure 4* |
| $t_{WHA}$ | Address Hold Time after Write | 4.0 | | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time prior to Write | 5.0 | | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 5.0 | | | ns | |
| $t_{WS}$ | Write Disable Time | | | 15 | ns | |
| $t_{WR}$ | Write Recovery Time | | | 20 | ns | |
| $t_r$ | Output Rise Time | | 5.0 | | ns | Measured between 20% and |
| $t_f$ | Output Fall Time | | 5.0 | | ns | 80% or 80% and 20% |
| $C_{IN}$ | Input Pin Capacitance | | 4.0 | 5.0 | pF | Measured with a Pulse |
| $C_{OUT}$ | Output Pin Capacitance | | 7.0 | 8.0 | pF | Technique |

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
3. $T_W$ measured at $t_{WSA}$ = Min, $t_{WSA}$ measured at $t_W$ = Min.

**Fig. 1 AC Test Circuit**




**Notes**
All Timing Measurements Referenced to 50% of Input Levels
$C_L$ = 30 pF including Fixture and Stray Capacitance
$R_L$ = 50 Ω to –2.0 V

**Fig. 2 Input Levels**

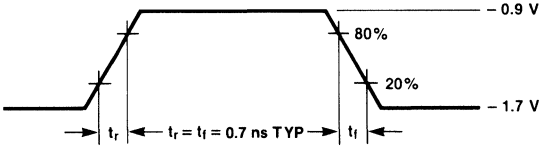
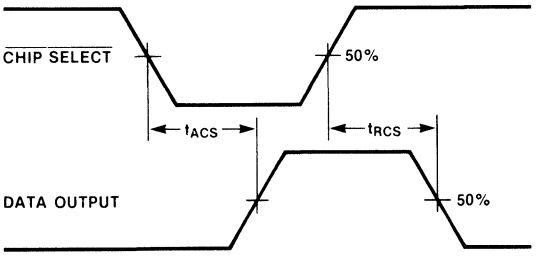



**Fig. 3 Read Mode Timing**

**a Read Mode Propagation Delay from Chip Select**




**b Read Mode Propagation Delay from Address**

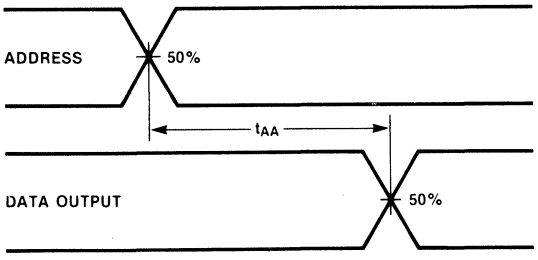
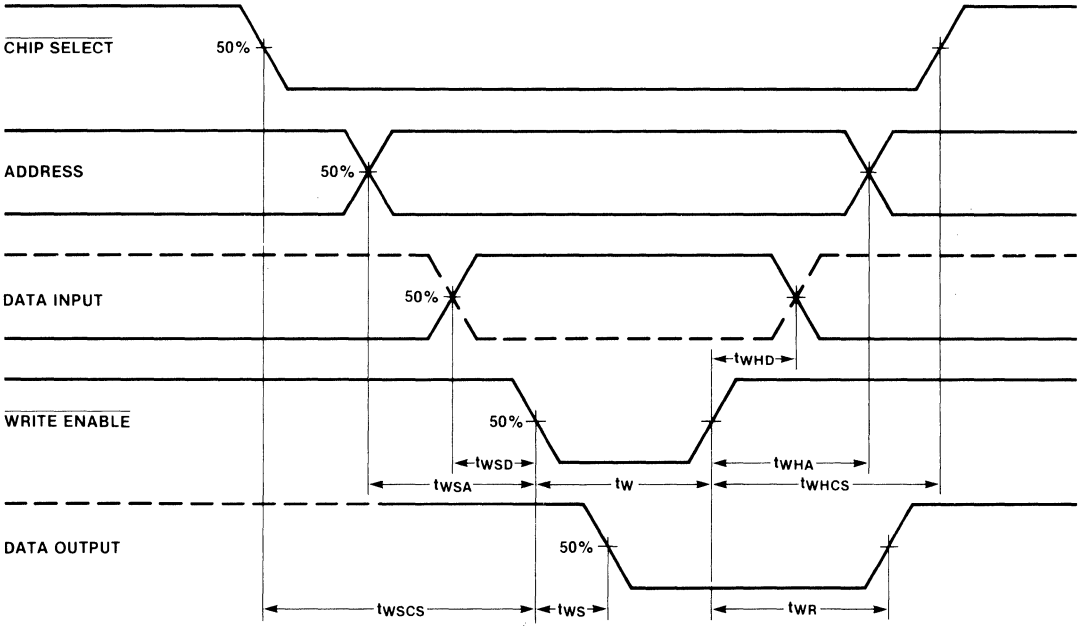
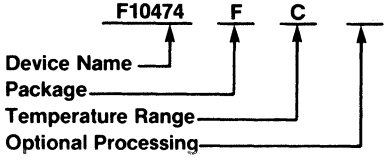


**Fig. 4 Write Mode Timing**




**Note**
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

## Ordering Information




**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak

**Temperature Ranges**
C = 0°C to +75°C, Ambient

**Optional Processing**
QR = 160 Hour Burn In

FAIRCHILD
A Schlumberger Company

# F10480
# 16,384 x 1-Bit Static Random Access Memory

Bipolar Division

F10K ECL Product

## Description

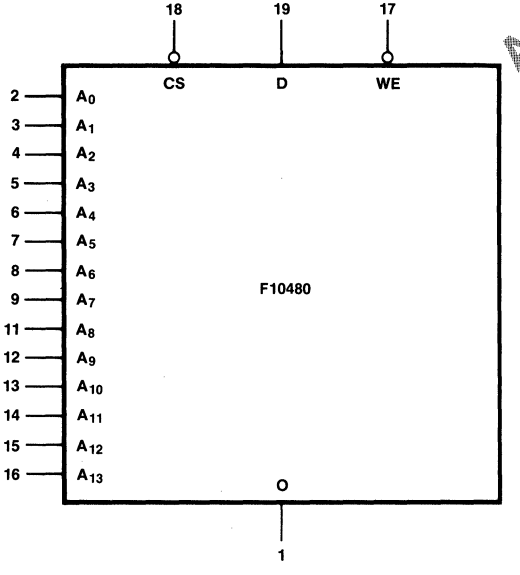
The F10480 is a 16,384-bit read/write Random Access Memory (RAM), organized 16,384 words by one bit per word and designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

- **Address Access Time — 25 ns Max**
- **Open-emitter Output for Easy Memory Expansion**
- **Power Dissipation — 0.05 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $\overline{WE}$ | Write Enable Input (Active LOW) |
| $\overline{CS}$ | Chip Select Input (Active LOW) |
| $A_0$–$A_{13}$ | Address Inputs |
| D | Data Input |
| O | Data Output |

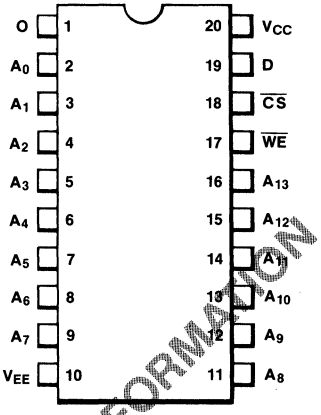
## Logic Symbol




$V_{CC}$ = Pin 20
$V_{EE}$ = Pin 10

## Connection Diagram

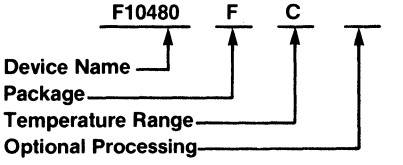
**20-Pin DIP** (Top View)




**Note**
The 20-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.



## Ordering Information

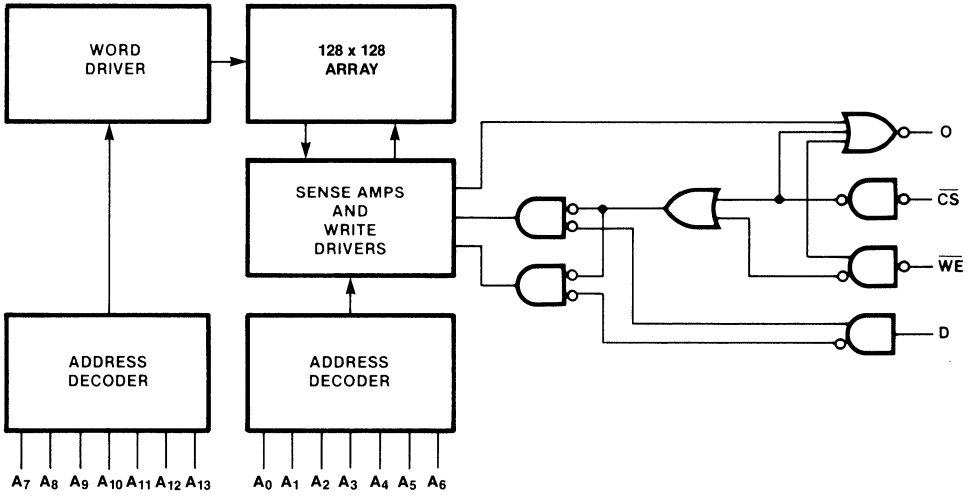



**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak

**Temperature Range**
C = 0°C to +75°C, Ambient

**Optional Processing**
QR = 160 Hour Burn In

## Logic Diagram






### Functional Description

The F10480 is a fully decoded 16,384-bit read/write random access memory, organized 16,384 words by one bit. Bit selection is achieved by means of a 14-bit address, $A_0$ through $A_{13}$.

One Chip Select input is provided for memory array expansion up to 32,768 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of Chip Select, ($\overline{CS}$) from the address without increasing address access time.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the output (O).

The output of the F10480 is an unterminated emitter follower, which allows maximum flexibility in choosing output connection configurations. In many applications it is desirable to tie the outputs of several F10480 devices together. In other applications the wired-OR need not be used. In either case an external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is OFF.

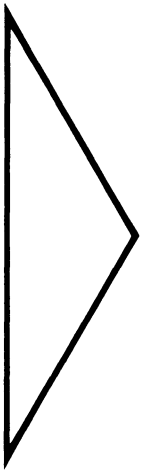
**Truth Table**

| Inputs | | | Output | |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | D | O | Mode |
| H | X | X | L | Not Selected |
| L | L | L | L | Write "0" |
| L | L | H | L | Write "1" |
| L | H | X | Data | Read |

H = HIGH Voltage Levels = −0.9 V (Nominal)
L = LOW Voltage Levels = −1.7 V (Nominal)
X = Don't Care
Data = Previously stored data

# Notes

# Notes



**Absolute Maximum Ratings:** Above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| $V_{CC}$ Pin Potential to Ground Pin | −0.5 V to +7.0 V |
| *Input Voltage (dc) | −0.5 V to +5.5 V |
| *Input Current (dc) | −12 mA to +5.0 mA |
| **Voltage Applied to Outputs (output HIGH) | −0.5 V to +5.50 V |
| Output Current (dc) | +20 mA |

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required



**Guaranteed Operating Ranges**

| | Supply Voltage ($V_{CC}$) | | | Ambient Temperature ($T_A$) Note 1 |
|---|---|---|---|---|
| | Min | Typ | Max | |
| Commercial | 4.75 V | 5.0 V | 5.25 V | 0°C to +75°C |
| Military | 4.50 V | 5.0 V | 5.50 V | −55°C to +125°C |

1. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute, conformance testing performed instantaneously where $T_A = T_J = T_C$. Correlated temperatures, typically 25°C and 100°C, and limits may be used to guarantee device operating performance.
2. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

| Symbol | Characteristic | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Pin Capacitance | 4.0 | 5.0 | pF | Measured with a Pulse |
| $C_{OUT}$ | Output Pin Capacitance | 7.0 | 8.0 | pF | Technique |

DC specifications listed with each device

FAIRCHILD
A Schlumberger Company

# 93415
# 1024 x 1-Bit Static Random Access Memory

Bipolar Division

TTL Bipolar Memory

## Description

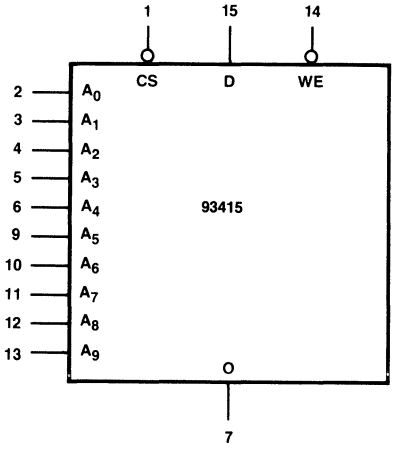
The 93415 is a 1024-bit read/write Random Access Memory (RAM), organized 1024 words by one bit. It is designed for high speed cache, control and buffer storage applications. The device includes full on-chip decoding, separate Data input and non-inverting Data output, as well as an active LOW Chip Select line.

- **Commercial Address Access Time**
  **93415 — 45 ns Max**
  **93415A — 30 ns Max**
- **Military Address Access Time — 60 ns Max**
- **Features Open Collector Output**
- **Power Dissipation — 0.46 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $\overline{CS}$ | Chip Select Input (Active LOW) |
| $A_0$–$A_9$ | Address Inputs |
| $\overline{WE}$ | Write Enable Input (Active LOW) |
| D | Data Input |
| O | Data Output |

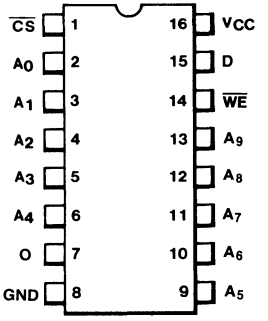
## Logic Symbol




$V_{CC}$ = Pin 16
GND = Pin 8

## Connection Diagram

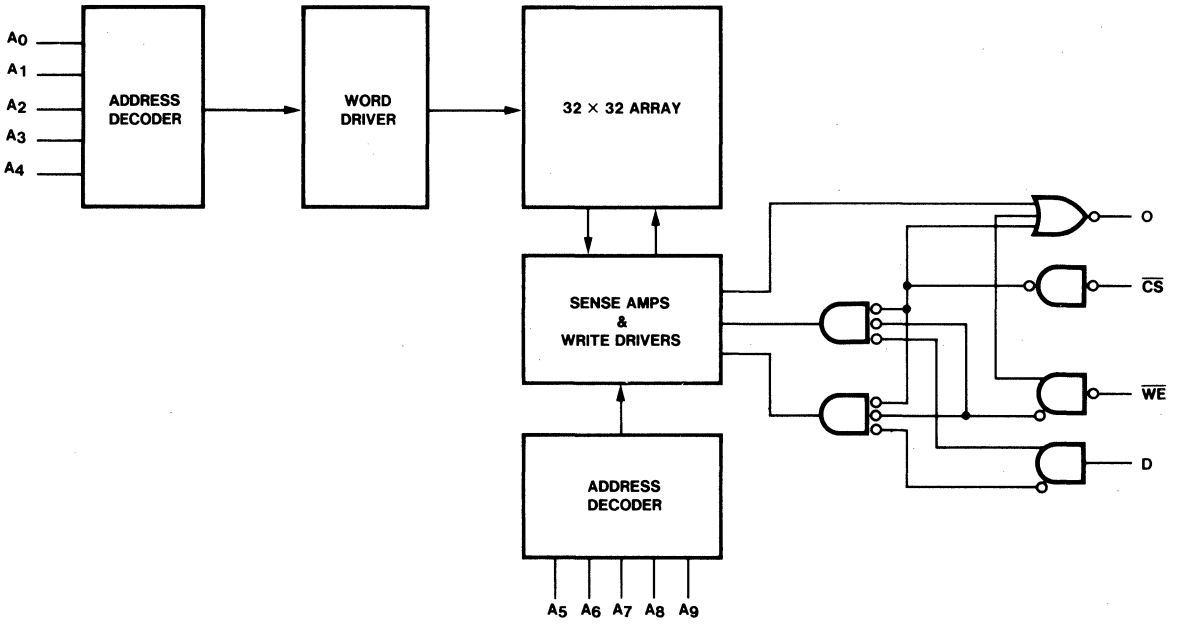
**16-Pin DIP** (Top View)




**Note:**
The 16-pin Flatpak version has the same pinout connections as the Dual In-line package.

4

## Logic Diagram




### Functional Description

The 93415 is a fully decoded 1024-bit read/write Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, $A_0$ through $A_9$.

One Chip Select input is provided for easy memory array expansion of up to 2048 bits without the need for external decoding. For larger memories, the fast chip select access time permits direct address decoding without an increase in overall memory access time.

The read and write functions of the 93415 are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. When $\overline{WE}$ is held LOW and the chip is selected, the data at D is written into the location specified by the binary address present at $A_0$ through $A_9$. Since the write function is level triggered, data must be held stable at the data input for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. When $\overline{WE}$ is held HIGH and the chip selected, data is read from the addressed location and presented at the output (O).

An open collector output is provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93415s can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of $R_L$ value must be used to provide a HIGH at the output

when it is off. Any $R_L$ value within the range specified below may be used.

$$\frac{V_{CC}(Max)}{I_{OL} - FO(1.6)} \leq R_L \leq \frac{V_{CC}(Min) - V_{OH}}{n(I_{CEX}) + FO(0.04)}$$

$R_L$ is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
$I_{CEX}$ = Memory Output Leakage Current
$V_{OH}$ = Required Output HIGH Level at Output Node
$I_{OL}$ = Output LOW Current

The minimum $R_L$ value is limited by the output current sinking ability. The maximum $R_L$ value is determined by the output and input leakage current which must be supplied to hold the output at $V_{OH}$.
One Unit Load = 40 $\mu$A HIGH/1.6 mA LOW.
$FO_{MAX}$ = 5 UL.

**Truth Table**

| Inputs | | | Output | |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | D | O | Mode |
| H | X | X | H | Not Selected |
| L | L | L | H | Write "0" |
| L | L | H | H | Write "1" |
| L | H | X | $D_{OUT}$ | Read |

H = HIGH Voltage Level (2.4 V)
L = LOW Voltage Level (.5 V)
X = Don't Care (HIGH or LOW)

**DC Characteristics:** Over operating temperature ranges (Notes 1, 2)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition | |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Output LOW Voltage | | 0.3 | 0.45 | V | $V_{CC}$ = Min, $I_{OL}$ = 16 mA | |
| $V_{IH}$ | Input HIGH Voltage | 2.1 | 1.6 | | V | Guaranteed Input HIGH Voltage for All Inputs[6] | |
| $V_{IL}$ | Input LOW Voltage | | 1.5 | 0.8 | V | Guaranteed Input LOW Voltage for All Inputs[6] | |
| $I_{IL}$ | Input LOW Current | | −250 | −400 | $\mu$A | $V_{CC}$ = Max, $V_{IN}$ = 0.4 V | |
| $I_{IH}$ | Input HIGH Current | | 1.0 | 40<br>1.0 | $\mu$A<br>mA | $V_{CC}$ = Max, $V_{IN}$ = 4.5 V<br>$V_{CC}$ = Max, $V_{IN}$ = 5.25 V | |
| $V_{IC}$ | Input Diode Clamp Voltage | | −1.0 | −1.5 | V | $V_{CC}$ = Max, $I_{IN}$ = −10 mA | |
| $I_{CEX}$ | Output Leakage Current | | 1.0 | 100 | $\mu$A | $V_{CC}$ = Max, $V_{OUT}$ = 4.5 V | |
| $I_{CC}$ | Power Supply Current | | 95 | 155<br>170 | mA | Commercial<br>Military | $V_{CC}$ = Max<br>All Inputs GND |

**Notes**
1. Operating specification with adequate time for temperature stabilization and transverse airflow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where $T_A = T_J = T_C$. Correlated temperatures, typically 25°C and 100°C, and limits may be used to guarantee performance.
2. Typical values are at $V_{CC}$ = 5.0 V, $T_A$ = +25°C and maximum loading.
3. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
4. Short circuit to ground not to exceed one second.
5. $T_W$ measured at $t_{WSA}$ = Min, $t_{WSA}$ measured at $t_W$ = Min.
6. Static condition only.

**Commercial**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 5%, GND = 0 V, $T_A$ = 0°C to +75°C (Notes 1, 3)

| Symbol | Characteristic | "A" Min | "A" Max | Std Min | Std Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | **Read Timing** | | | | | | |
| $t_{ACS}$ | Chip Select Access Time | | 20 | | 35 | ns | |
| $t_{ZRCS}$ | Chip Select to HIGH Z | | 20 | | 35 | ns | *Figures 3a, 3b* |
| $t_{AA}$ | Address Access Time | | 30 | | 45 | ns | |
| | **Write Timing** | | | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[5] | 20 | | 35 | | ns | |
| $t_{WSD}$ | Data Setup Time Prior to Write | 5 | | 5 | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 5 | | 5 | | ns | |
| $t_{WSA}$ | Address Setup Time Prior to Write[5] | 5 | | 5 | | ns | *Figure 4* |
| $t_{WHA}$ | Address Hold Time after Write | 5 | | 5 | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time Prior to Write | 5 | | 5 | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 5 | | 5 | | ns | |
| $t_{ZWS}$ | Write Disable to HIGH Z | | 20 | | 35 | ns | |
| $t_{WR}$ | Write Recovery Time | | 25 | | 40 | ns | |

**Military**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 10%, GND = 0 V, $T_A$ = −55°C to +125°C (Notes 1, 3)

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| | **Read Timing** | | | | |
| $t_{ACS}$ | Chip Select Access Time | | 45 | ns | |
| $t_{ZRCS}$ | Chip Select to HIGH Z | | 50 | ns | *Figures 3a, 3b* |
| $t_{AA}$ | Address Access Time | | 60 | ns | |
| | **Write Timing** | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[5] | 40 | | ns | |
| $t_{WSD}$ | Data Setup Time Prior to Write | 5 | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 5 | | ns | |
| $t_{WSA}$ | Address Setup Time Prior to Write[5] | 15 | | ns | *Figure 4* |
| $t_{WHA}$ | Address Hold Time after Write | 5 | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time Prior to Write | 5 | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 5 | | ns | |
| $t_{ZWS}$ | Write Disable to HIGH Z | | 45 | ns | |
| $t_{WR}$ | Write Recovery Time | | 50 | ns | |

Notes on preceeding page

**Fig. 1 AC Test Circuit**

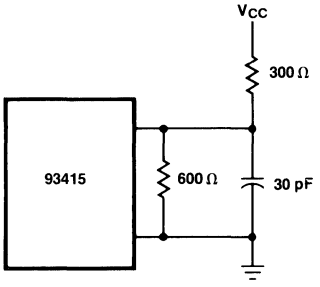



**Fig. 2 Input Levels**

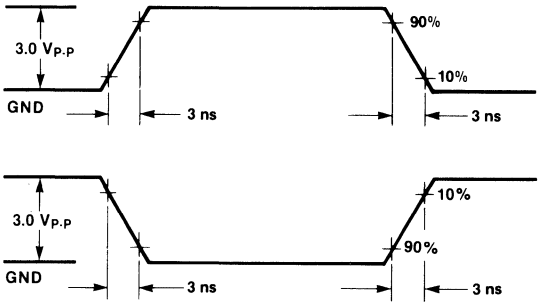
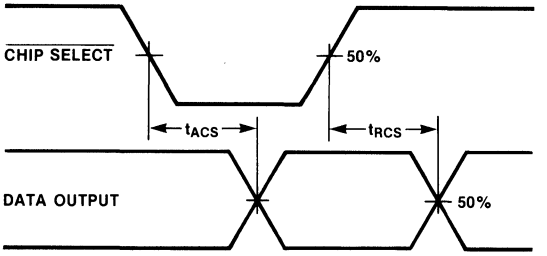



**Fig. 3 Read Mode Timing**

**a Read Mode Propagation Delay from Chip Select**




**b Read Mode Propagation Delay from Address**

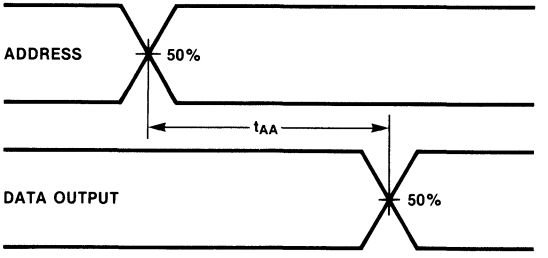



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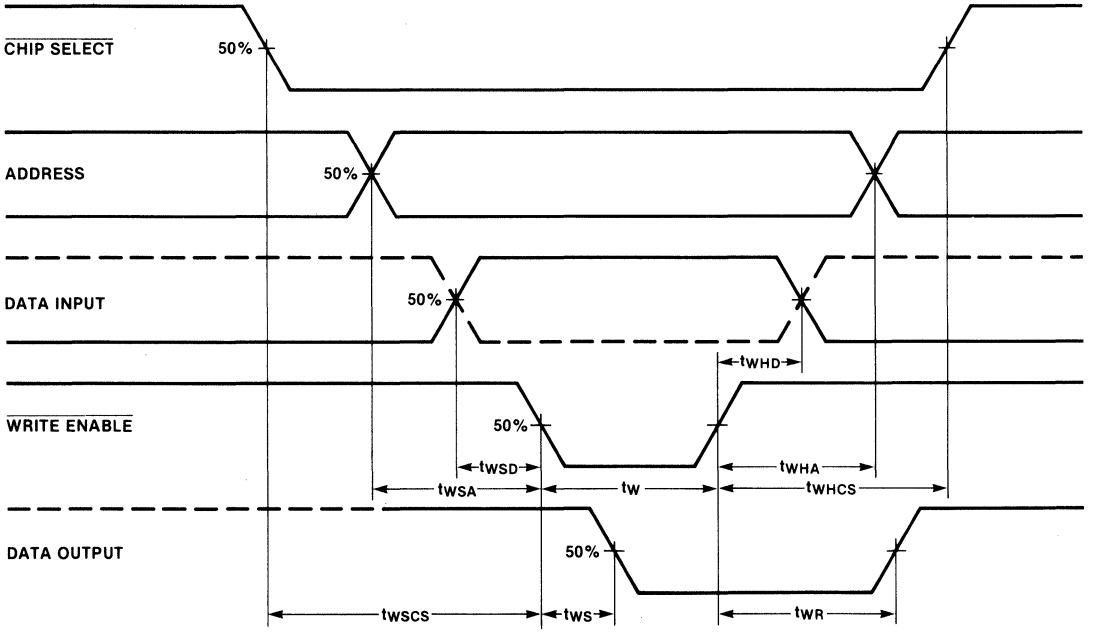
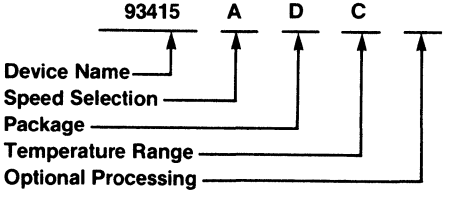
**Fig. 4 Write Mode Timing**




**Note**
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

## Ordering Information




**Speed Selection**
Blank = Standard Speed
A = 'A' Grade (Commercial Only)

**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier
P = Plastic DIP

**Temperature Range**
C = 0°C to +75°C
M = −55°C to +125°C

**Optional Processing**
QB = Mil Std 883
Method 5004 and 5005, Level B
QC = Mil Std 883
Method 5004 and 5005, Level C
QR = Commercial Device with
160 Hour Burn In

FAIRCHILD
A Schlumberger Company

# 93L415
# 1024 x 1-Bit Static Random Access Memory

Bipolar Division

TTL Bipolar Memory

## Description

The 93L415 is a 1024-bit read/write Random Access Memory (RAM), organized 1024 words by one bit. It is designed for high speed cache, control and buffer storage applications. The device includes full on-chip decoding, separate Data input and non-inverting Data output, as well as an active LOW Chip Select line.

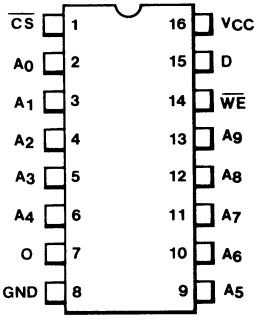
- **Commercial Address Access Time — 60 ns Max**
- **Military Address Access Time — 70 ns Max**
- **Features Open Collector Output**
- **Power Dissipation — 0.22 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $\overline{CS}$ | Chip Select Input (Active LOW) |
| $A_0$–$A_9$ | Address Inputs |
| $\overline{WE}$ | Write Enable Input (Active LOW) |
| D | Data Input |
| O | Data Output |

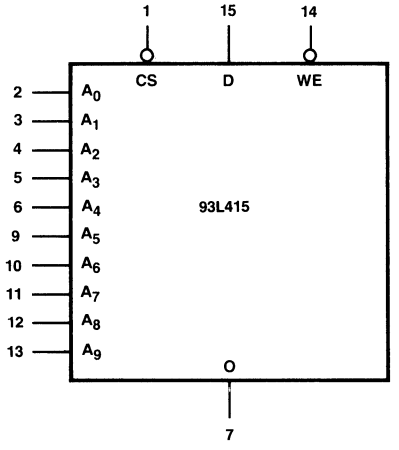
## Connection Diagram

**16-Pin DIP** (Top View)




**Note:**
The 16-pin Flatpak version has the same pinout connections as the Dual In-line package.

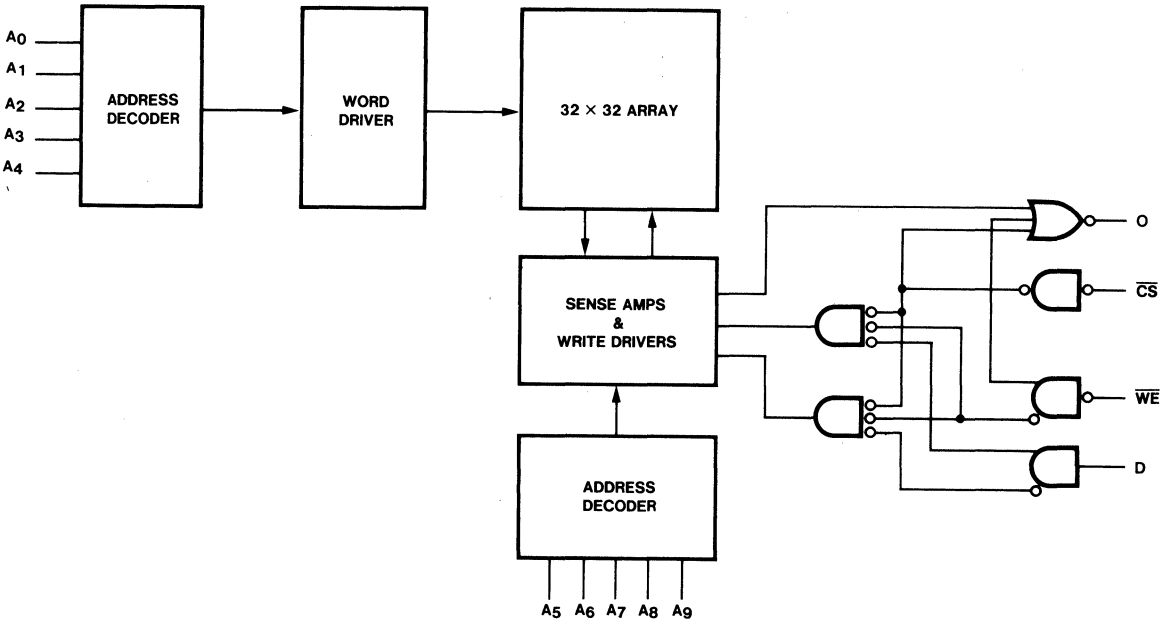
## Logic Symbol




$V_{CC}$ = Pin 16
GND = Pin 8

4

## Logic Diagram




### Functional Description

The 93L415 is a fully decoded 1024-bit read/write Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, $A_0$ through $A_9$.

One Chip Select input is provided for easy memory array expansion of up to 2048 bits without the need for external decoding. For larger memories, the fast chip select access time permits direct address decoding without an increase in overall memory access time.

The read and write functions of the 93L415 are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. When $\overline{WE}$ is held LOW and the chip is selected, the data at D is written into the location specified by the binary address present at $A_0$ through $A_9$. Since the write function is level triggered, data must be held stable at the data input for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. When $\overline{WE}$ is held HIGH and the chip selected, data is read from the addressed location and presented at the output (O).

An open collector output is provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93L415s can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of $R_L$ value must be used to provide a HIGH at the output when it is off. Any $R_L$ value within the range specified below may be used.

$$\frac{V_{CC}\,(Max)}{I_{OL} - FO\,(1.6)} \leq R_L \leq \frac{V_{CC}\,(Min) - V_{OH}}{n\,(I_{CEX}) + FO\,(0.04)}$$

$R_L$ is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
$I_{CEX}$ = Memory Output Leakage Current
$V_{OH}$ = Required Output HIGH Level at Output Node
$I_{OL}$ = Output LOW Current

The minimum $R_L$ value is limited by the output current sinking ability. The maximum $R_L$ value is determined by the output and input leakage current which must be supplied to hold the output at $V_{OH}$.
One Unit Load = 40 $\mu$A HIGH/1.6 mA LOW.

**Truth Table**

| Inputs | | | Output | |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | D | O | Mode |
| H | X | X | H | Not Selected |
| L | L | L | H | Write "0" |
| L | L | H | H | Write "1" |
| L | H | X | $D_{OUT}$ | Read |

H = HIGH Voltage Level (2.4 V)
L = LOW Voltage Level (.5 V)
X = Don't Care (HIGH or LOW)



**DC Characteristics:** Over operating temperature ranges (Notes 1, 2)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition | |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Output LOW Voltage | | 0.3 | 0.45 | V | $V_{CC}$ = Min, $I_{OL}$ = 16 mA | |
| $V_{IH}$ | Input HIGH Voltage | 2.1 | 1.6 | | V | Guaranteed Input HIGH Voltage for All Inputs[6] | |
| $V_{IL}$ | Input LOW Voltage | | 1.5 | 0.8 | V | Guaranteed Input LOW Voltage for All Inputs[6] | |
| $I_{IL}$ | Input LOW Current | | −150 | −300 | $\mu$A | $V_{CC}$ = Max, $V_{IN}$ = 0.4 V | |
| $I_{IH}$ | Input HIGH Current | | 1.0 | 40<br>1.0 | $\mu$A<br>mA | $V_{CC}$ = Max, $V_{IN}$ = 4.5 V<br>$V_{CC}$ = Max, $V_{IN}$ = 5.25 V | |
| $V_{IC}$ | Input Diode Clamp Voltage | | −1.0 | −1.5 | V | $V_{CC}$ = Max, $I_{IN}$ = −10 mA | |
| $I_{CEX}$ | Output Leakage Current | | 1.0 | 100 | $\mu$A | $V_{CC}$ = Max, $V_{OUT}$ = 4.5 V | |
| $I_{CC}$ | Power Supply Current | | 45 | 65<br>75 | mA | Commercial<br>Military | $V_{CC}$ = Max<br>All Inputs GND |

**Notes**

1. Operating specification with adequate time for temperature stabilization and transverse airflow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where $T_A = T_J = T_C$. Correlated temperatures, typically 25°C and 100°C, and limits may be used to guarantee performance.
2. Typical values are at $V_{CC}$ = 5.0 V, $T_A$ = +25°C and maximum loading.
3. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
4. Short circuit to ground not to exceed one second.
5. $t_W$ measured at $t_{WSA}$ = Min, $t_{WSA}$ measured at $t_W$ = Min.
6. Static condition only.

**Commercial**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 5%, GND = 0 V, $T_A$ = 0°C to +75°C (Notes 1, 3)

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| | **Read Timing** | | | | |
| $t_{ACS}$ | Chip Select Access Time | | 40 | ns | |
| $t_{ZRCS}$ | Chip Select to HIGH Z | | 40 | ns | *Figures 3a, 3b* |
| $t_{AA}$ | Address Access Time | | 60 | ns | |
| | **Write Timing** | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[5] | 45 | | ns | |
| $t_{WSD}$ | Data Setup Time Prior to Write | 5 | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 5 | | ns | |
| $t_{WSA}$ | Address Setup Time Prior to Write[5] | 10 | | ns | *Figure 4* |
| $t_{WHA}$ | Address Hold Time after Write | 5 | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time Prior to Write | 5 | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 5 | | ns | |
| $t_{ZWS}$ | Write Disable to HIGH Z | | 45 | ns | |
| $t_{WR}$ | Write Recovery Time | | 45 | ns | |

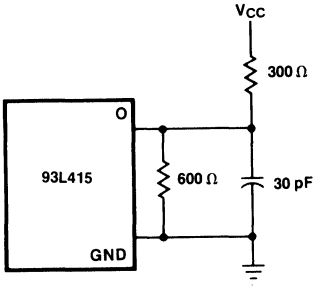
**Military**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 10%, GND = 0 V, $T_A$ = −55°C to +125°C (Notes 1, 3)

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| | **Read Timing** | | | | |
| $t_{ACS}$ | Chip Select Access Time | | 45 | ns | |
| $t_{ZRCS}$ | Chip Select to HIGH Z | | 50 | ns | *Figures 3a, 3b* |
| $t_{AA}$ | Address Access Time | | 70 | ns | |
| | **Write Timing** | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[5] | 50 | | ns | |
| $t_{WSD}$ | Data Setup Time Prior to Write | 10 | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 10 | | ns | |
| $t_{WSA}$ | Address Setup Time Prior to Write[5] | 10 | | ns | *Figure 4* |
| $t_{WHA}$ | Address Hold Time after Write | 10 | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time Prior to Write | 10 | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 10 | | ns | |
| $t_{ZWS}$ | Write Disable to HIGH Z | | 45 | ns | |
| $t_{WR}$ | Write Recovery Time | | 55 | ns | |

Notes on preceeding page

**Fig. 1 AC Test Circuit**




**Load A**

**Fig. 2 Input Levels**

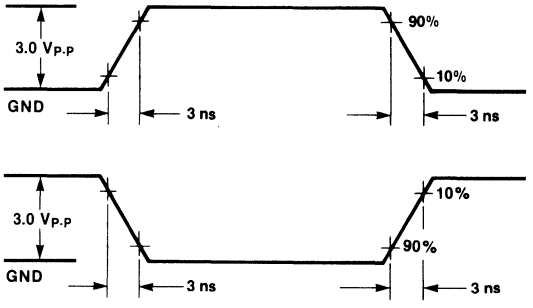
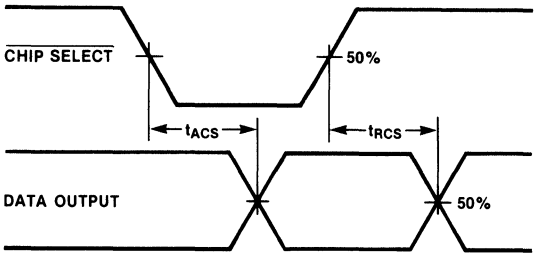
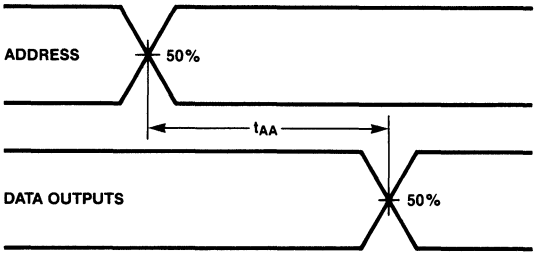



**Fig. 3 Read Mode Timing**

**a Read Mode Propagation Delay from Chip Select**

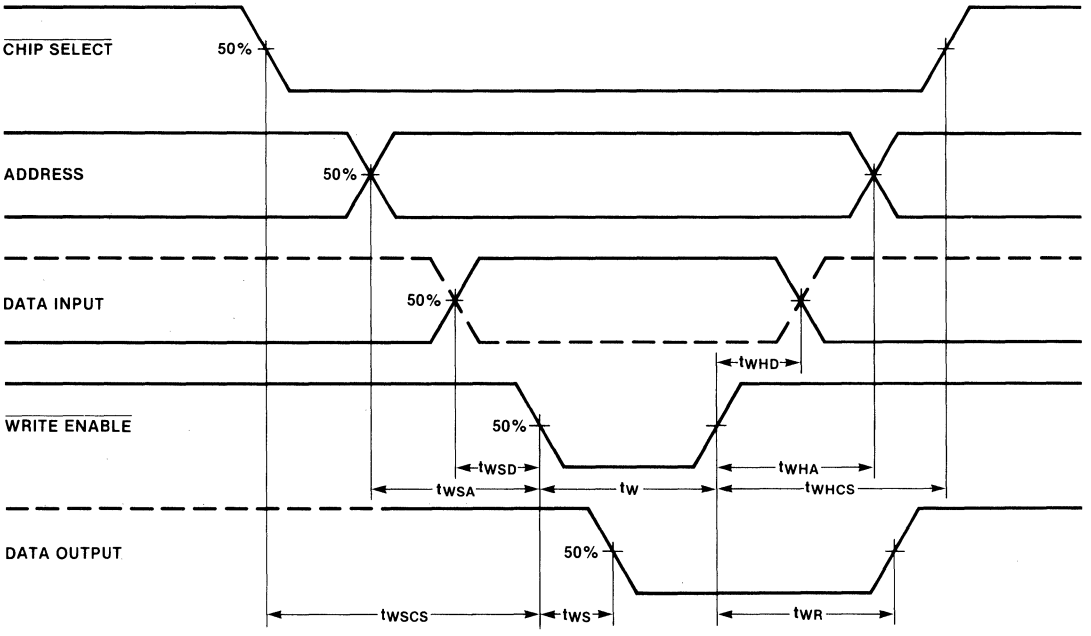



**b Read Mode Propagation Delay from Address**




4

**Fig. 4 Write Mode Timing**




**Note:**
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

## Ordering Information

93L415 D C

Device Name
Package
Temperature Range
Optional Processing

**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier
P = Plastic DIP

**Temperature Range**
C = 0°C to +75°C
M = −55°C to +125°C

**Optional Processing**
QB = Mil Std 883
Method 5004 and 5005, Level B
QC = Mil Std 883
Method 5004 and 5005, Level C
QR = Commercial Device with
160 Hour Burn In

FAIRCHILD
A Schlumberger Company

# 93419
# 64 x 9-Bit Static Random Access Memory

Bipolar Division

TTL Bipolar Memory

## Description

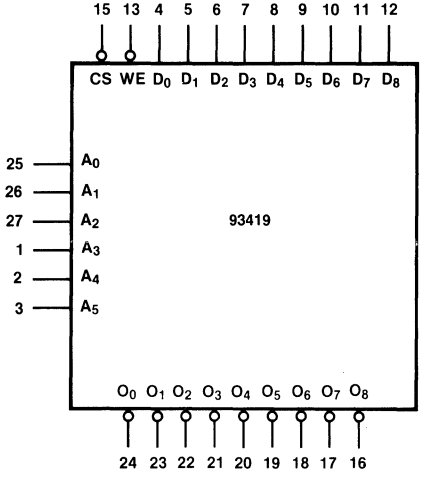
The 93419 is a 576-bit read/write Random Access Memory (RAM), organized 64 words by nine bits per word with open collector outputs. It is ideally suited for scratchpad, small buffer and other applications where the number of required words is small and where the number of required bits per word is relatively large. The ninth bit can provide parity for 8-bit word systems. The commercial version of the 93419 is available in two speeds "standard" speed and an 'A' grade.

- **Commercial Address Access Time**
  **93419 — 45 ns Max**
  **93419A — 35 ns Max**
- **Military Address Access Time — 60 ns Max**
- **Fully TTL Compatible**
- **Features Open Collector Outputs**
- **Data Output is the Complement of Data Input**
- **Power Dissipation — 0.87 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $A_0$-$A_5$ | Address Inputs |
| $D_0$-$D_8$ | Data Inputs |
| $\overline{O}_0$-$\overline{O}_8$ | Inverting Data Outputs |
| $\overline{WE}$ | Write Enable Input (Active LOW) |
| $\overline{CS}$ | Chip Select Input (Active LOW) |

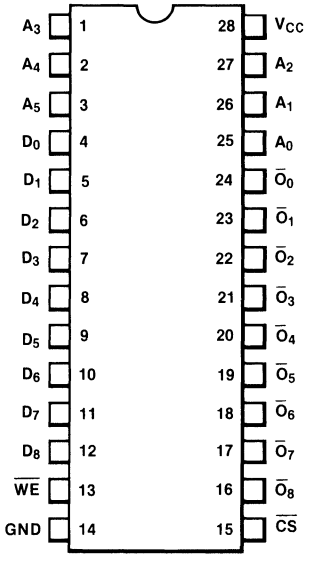
## Logic Symbol




$V_{CC}$ = Pin 28
GND = Pin 14

## Connection Diagram

**28-Pin DIP** (Top View)

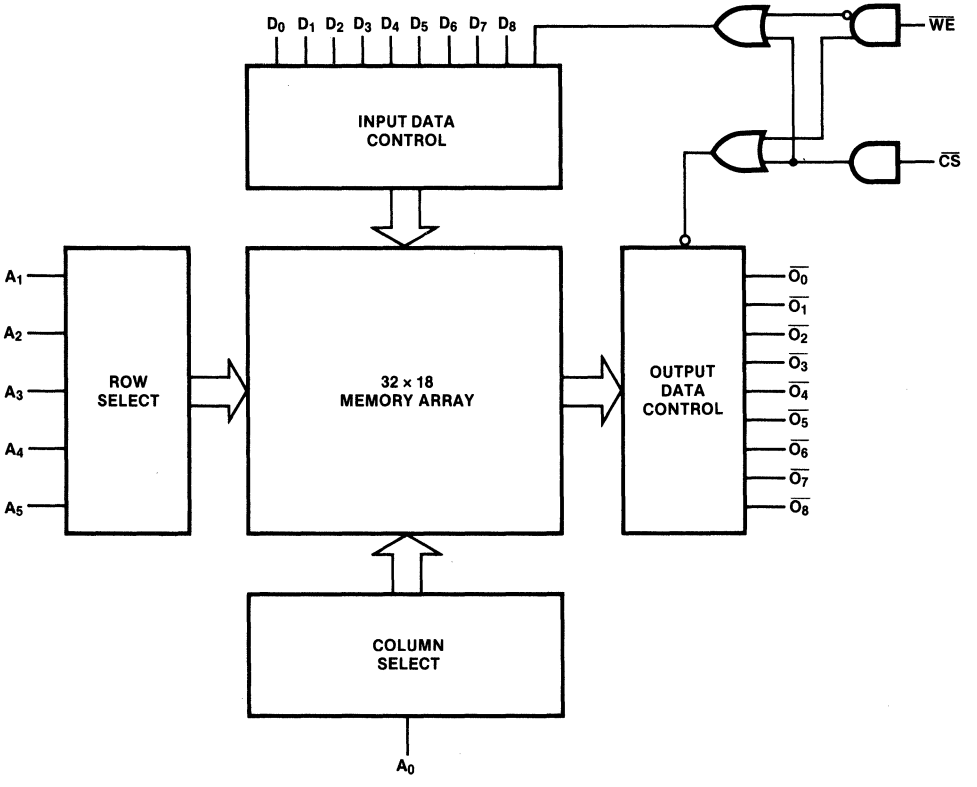



(Top View)

**Note:**
The 28-Pin Flatpak and the 28-Pin Leadless Chip Carrier have the same pinout as the 28-Pin DIP.

4

## Logic Diagram




### Functional Description

The 93419 is a fully decoded 576-bit random access memory organized 64 words by nine bits. Word selection is achieved by means of a 6-bit address, $A_0$ through $A_5$.

One Chip Select input is provided for easy memory array expansion of up to 128 words without the need for external decoding. For larger memories, the fast chip select access time permits decoding without an increase in overall memory access time.

The read and write functions of the 93419 are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. When $\overline{WE}$ is held LOW and the chip is selected, the data $D_0 - D_5$ is written into the location specified by the binary address present at $A_0$ through $A_5$. Since the write function is level triggered, data must be held stable at the data input for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. When $\overline{WE}$ is held HIGH and the chip selected, inverted data is read from the addressed location and presented at the outputs ($\overline{O_0} - \overline{O_8}$).

Open collector outputs are provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93419s can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of $R_L$ value must be used to provide a HIGH at the output when it is off. Any $R_L$ value within the range specified below may be used.

$$\frac{V_{CC}(Max)}{I_{OL} - FO(1.6)} \leq R_L \leq \frac{V_{CC}(Min) - V_{OH}}{n(I_{CEX}) + FO(0.04)}$$

$R_L$ is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
$I_{CEX}$ = Memory Output Leakage Current
$V_{OH}$ = Required Output HIGH Level at Output Node
$I_{OL}$ = Output LOW Current

The minimum $R_L$ value is limited by the output current sinking ability. The maximum $R_L$ value is determined by the output and input leakage current which must be supplied to hold the output at $V_{OH}$.
One Unit Load = 40 μA HIGH/1.6 mA LOW.

**Truth Table**

| Inputs | | | Output | |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | D | Open Collector | Mode |
| H | X | X | H | Not Selected |
| L | L | L | H | Write "0"* |
| L | L | H | H | Write "1"* |
| L | H | X | $\overline{D_{OUT}}$* | Read |

H = HIGH Voltage Level (2.4 V)
L = LOW Voltage Level (.5 V)
X = Don't Care (HIGH or LOW)
*Memory inverts from Data In to Data Out

**DC Characteristics:** Over operating temperature ranges (Notes 1, 2)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition | |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Output LOW Voltage | | 0.3 | 0.5 | V | $V_{CC}$ = Min, $I_{OL}$ = 12 mA | |
| $V_{IH}$ | Input HIGH Voltage | 2.1 | 1.6 | | V | Guaranteed Input HIGH Voltage for All Inputs[6] | |
| $V_{IL}$ | Input LOW Voltage | | 1.5 | 0.8 | V | Guaranteed Input LOW Voltage for All Inputs[6] | |
| $I_{IL}$ | Input LOW Current | | −200 | −400 | μA | $V_{CC}$ = Max, $V_{IN}$ = 0.4 V | |
| $I_{IH}$ | Input HIGH Current | | 1.0 | 40<br>1.0 | μA<br>mA | $V_{CC}$ = Max, $V_{IN}$ = 4.5 V<br>$V_{CC}$ = Max, $V_{IN}$ = 5.25 V | |
| $I_{CEX}$ | Output Leakage Current | | 1.0 | −100 | μA | $V_{CC}$ = Max, $V_{OUT}$ = 4.5 V | |
| $V_{IC}$ | Input Clamp Diode Voltage | | −1.0 | −1.5 | V | $V_{CC}$ = Max, $I_{IN}$ = −10 mA, *Note 4* | |
| $I_{CC}$ | Power Supply Current | | 100 | 150<br>170 | mA<br>mA | Commercial<br>Military | $V_{CC}$ = Max<br>All Inputs Grounded |

**Notes**
1. Operating specification with adequate time for temperature stabilization and transverse airflow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where $T_A = T_J = T_C$. Correlated temperatures, typically 25°C and 100°C, and limits may be used to guarantee performance.
2. Typical values are at $V_{CC}$ = 5.0 V, $T_A$ = +25°C and maximum loading.
3. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
4. Short circuit to ground not to exceed one second.
5. $T_W$ measured at $t_{WSA}$ = Min, $t_{WSA}$ measured at $t_W$ = Min.
6. Static condition only.

**Commercial**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 5%, GND = 0 V, $T_A$ = 0°C to +75°C (Notes 1, 3)

| Symbol | Characteristic | "A" Min | "A" Max | Std Min | Std Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | **Read Timing** | | | | | | |
| $t_{ACS}$ | Chip Select Access Time | | 30 | | 40 | ns | |
| $t_{ZRCS}$ | Chip Select to HIGH Z | | 30 | | 40 | ns | *Figures 3a, 3b* |
| $t_{AA}$ | Address Access Time | | 35 | | 45 | ns | |
| | **Write Timing** | | | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[5] | 25 | | 35 | | ns | |
| $t_{WSD}$ | Data Setup Time Prior to Write | 5 | | 5 | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 5 | | 5 | | ns | |
| $t_{WSA}$ | Address Setup Time Prior to Write[5] | 5 | | 5 | | ns | *Figure 4* |
| $t_{WHA}$ | Address Hold Time after Write | 5 | | 5 | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time Prior to Write | 5 | | 5 | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 5 | | 5 | | ns | |
| $t_{ZWS}$ | Write Disable to HIGH Z | | 30 | | 40 | ns | |
| $t_{WR}$ | Write Recovery Time | | 35 | | 40 | ns | |

**Military**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 10%, GND = 0 V, $T_A$ = −55°C to +125°C (Notes 1, 3)

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| | **Read Timing** | | | | |
| $t_{ACS}$ | Chip Select Access Time | | 40 | ns | |
| $t_{ZRCS}$ | Chip Select to HIGH Z | | 40 | ns | *Figures 3a, 3b* |
| $t_{AA}$ | Address Access Time | | 60 | ns | |
| | **Write Timing** | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[5] | 45 | | ns | |
| $t_{WSD}$ | Data Setup Time Prior to Write | 5 | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 5 | | ns | |
| $t_{WSA}$ | Address Setup Time Prior to Write[5] | 10 | | ns | *Figure 4* |
| $t_{WHA}$ | Address Hold Time after Write | 5 | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time Prior to Write | 5 | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 5 | | ns | |
| $t_{ZWS}$ | Write Disable to HIGH Z | | 45 | ns | |
| $t_{WR}$ | Write Recovery Time | | 55 | ns | |

Notes on preceeding page

**Fig. 1 AC Test Load**

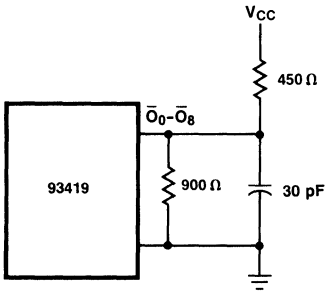



**Fig. 2 Input Levels**

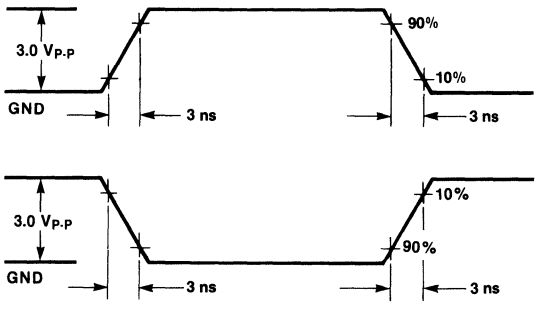
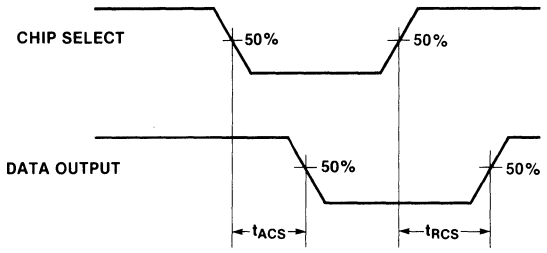
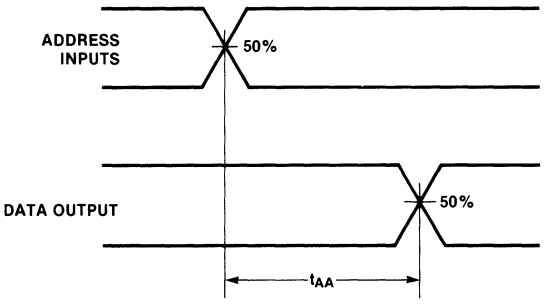



**Fig. 3 Read Mode Timing**

**a. Read Mode Propagation Delay from Chip Select**

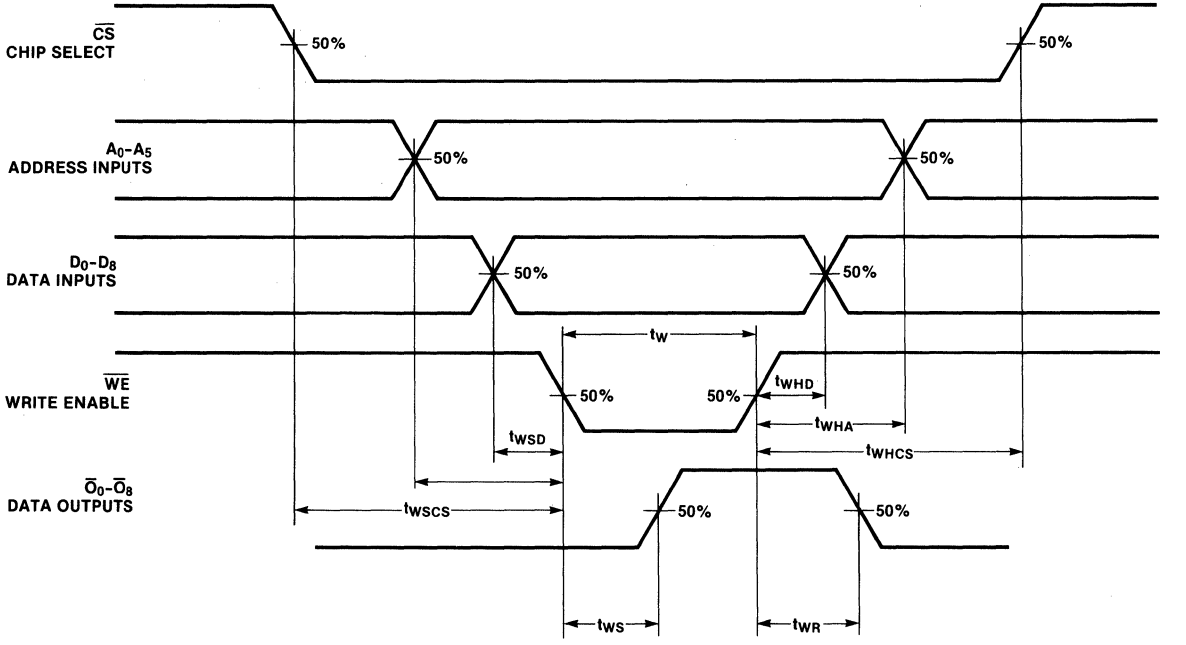



**b. Read Mode Propagation Delay from Address Inputs**



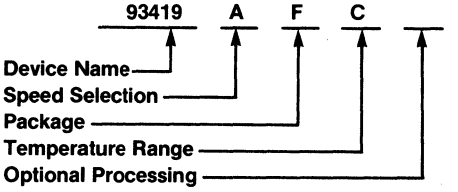

4

**Fig. 4 Write Mode Timing**




**Note:**
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

## Ordering Information




**Speed Selection**
Blank = Standard Speed
A = 'A' Grade (Commercial Only)

**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier
P = Plastic DIP

**Temperature Range**
C = 0°C to +75°C
M = −55°C to +125°C

**Optional Processing**
QB = Mil Std 883
Method 5004 and 5005, Level B
QC = Mil Std 883
Method 5004 and 5005, Level C
QR = Commercial Device with
160 Hour Burn In

FAIRCHILD
A Schlumberger Company

# 93422
# 256 x 4-Bit Static Random Access Memory

Bipolar Division

TTL Bipolar Memory

## Description

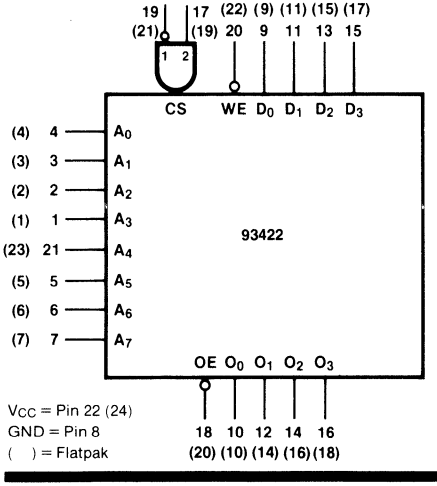
The 93422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits. It is designed for high speed cache, control and buffer storage applications. The 93422 is available in two speeds, "standard" speed and an "A" grade. The device includes full on-chip decoding, separate Data inputs and non-inverting Data outputs, as well as two Chip Select lines.

- **Commercial Address Access Time**
  - **93422 — 45 ns Max**
  - **93422A — 35 ns Max**
- **Military Address Access Time**
  - **93422 — 60 ns Max**
  - **93422A — 45 ns Max**
- **Fully TTL Compatible**
- **Features Three State Outputs**
- **Power Dissipation — 0.46 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $A_0$-$A_7$ | Address Inputs |
| $D_0$-$D_3$ | Data Inputs |
| $\overline{CS}_1$ | Chip Select Input (Active LOW) |
| $CS_2$ | Chip Select Input (Active HIGH) |
| $\overline{WE}$ | Write Enable Input (Active LOW) |
| $\overline{OE}$ | Output Enable Input (Active LOW) |
| $O_0$-$O_3$ | Data Outputs |

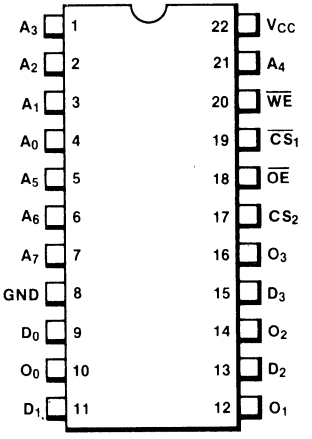
## Logic Symbol



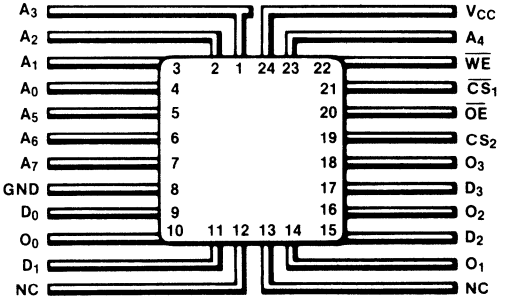

VCC = Pin 22 (24)
GND = Pin 8
( ) = Flatpak

## Connection Diagrams

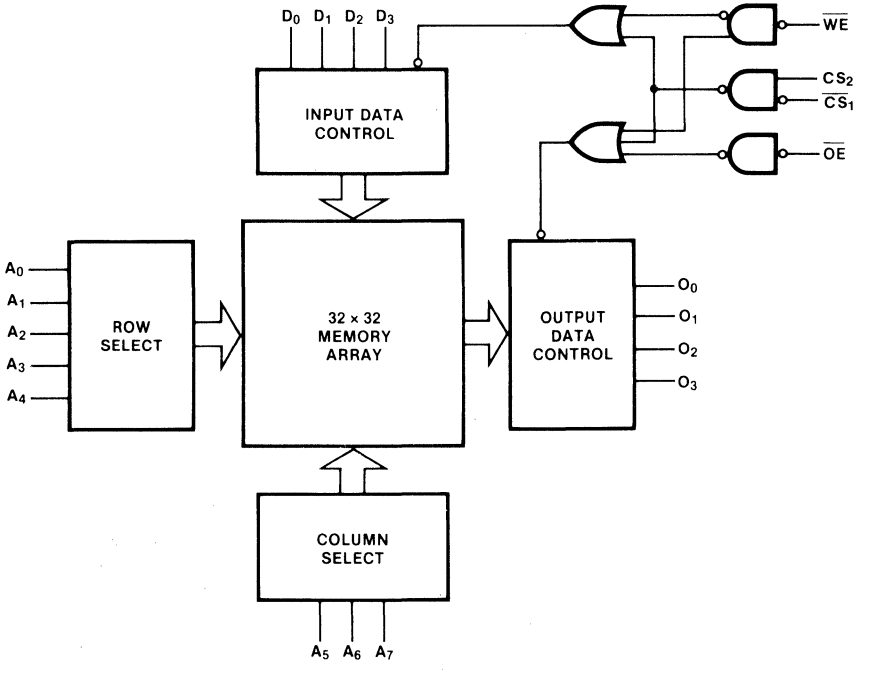
**22-Pin DIP** (Top View)




**24-Pin Flatpak** (Top View)



## Logic Diagram




### Functional Description

The 93422 is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, $A_0$ through $A_7$.

Two Chip Select inputs, inverting and non-inverting, are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of the chip selects from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. When $\overline{WE}$ is held LOW and the chip is selected, the data at $D_0$–$D_3$ is written into the addressed location. Since the write function is level-triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the outputs ($O_0$–$O_3$).

The 93422 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.

**Truth Table**

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| $\overline{OE}$ | $\overline{CS_1}$ | $CS_2$ | $\overline{WE}$ | $D_0$-$D_3$ | 3-State | Mode |
| X | H | X | X | X | HIGH Z | Not Selected |
| X | X | L | X | X | HIGH Z | Not Selected |
| L | L | H | H | X | $O_0$-$O_3$ | Read Stored Data |
| L | L | H | L | L | HIGH Z | Write "0" |
| L | L | H | L | H | HIGH Z | Write "1" |
| H | L | H | H | X | HIGH Z | Output Disabled |
| H | L | H | L | L | HIGH Z | Write "0" (Output Disabled) |
| H | L | H | L | H | HIGH Z | Write "1" (Output Disabled) |

H = HIGH Voltage Level (2.4 V)
L = LOW Voltage Level (.5 V)
X = Don't Care (HIGH or LOW)
High Z = High-Impedance

4

**DC Characteristics:** Over operating temperature ranges (Notes 1, 2)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition | |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Output LOW Voltage | | 0.3 | 0.45 | V | $V_{CC}$ = Min, $I_{OL}$ = 8 mA | |
| $V_{IH}$ | Input HIGH Voltage | 2.1 | 1.6 | | V | Guaranteed Input HIGH Voltage for All Inputs[6] | |
| $V_{IL}$ | Input LOW Voltage | | 1.5 | 0.8 | V | Guaranteed Input LOW Voltage for All Inputs[6] | |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $V_{CC}$ = Min, $I_{OH}$ = −5.2 mA | |
| $I_{IL}$ | Input LOW Current | | −150 | −300 | μA | $V_{CC}$ = Max, $V_{IN}$ = 0.4 V | |
| $I_{IH}$ | Input HIGH Current | | 1.0 | 40<br>1.0 | μA<br>mA | $V_{CC}$ = Max, $V_{IN}$ = 4.5 V<br>$V_{CC}$ = Max, $V_{IN}$ = 5.25 V | |
| $V_{IC}$ | Input Diode Clamp Voltage | | −1.0 | −1.5 | V | $V_{CC}$ = Max, $I_{IN}$ = −10 mA | |
| $I_{OFF}$ | Output Current (HIGH Z) | | | 50<br>−50 | μA | $V_{CC}$ = Max, $V_{OUT}$ = 2.4 V<br>$V_{CC}$ = Max, $V_{OUT}$ = 0.5 V | |
| $I_{OS}$ | Output Current Short Circuit to Ground | | | −70 | mA | $V_{CC}$ = Max, Note 4 | |
| $I_{CC}$ | Power Supply Current | | 95<br>95 | 150<br>170 | mA | Commercial<br>Military | $V_{CC}$ = Max<br>All Inputs GND |

**Notes**

1. Operating specification with adequate time for temperature stabilization and transverse airflow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where $T_A = T_J = T_C$. Correlated temperatures, typically 25°C and 100°C, and limits may be used to guarantee performance.
2. Typical values are at $V_{CC}$ = 5.0 V, $T_A$ = +25°C and maximum loading.
3. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
4. Short circuit to ground not to exceed one second.
5. $T_W$ measured at $t_{WSA}$ = Min, $t_{WSA}$ measured at $t_W$ = Min.
6. Static condition only.

**Commercial**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 5%, GND = 0 V, $T_A$ = 0°C to +75°C (Notes 1, 3)

| Symbol | Characteristic | "A" Min | "A" Max | Std Min | Std Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | **Read Timing** | | | | | | |
| $t_{ACS}$ | Chip Select Access Time | | 30 | | 30 | ns | |
| $t_{ZRCS}$ | Chip Select to HIGH Z | | 30 | | 30 | ns | |
| $t_{AOS}$ | Output Enable Access Time | | 30 | | 30 | ns | *Figures 3a, 3b, 3c* |
| $t_{ZROS}$ | Output Enable to HIGH Z | | 30 | | 30 | ns | |
| $t_{AA}$ | Address Access Time | | 35 | | 45 | ns | |
| | **Write Timing** | | | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[5] | 25 | | 30 | | ns | |
| $t_{WSD}$ | Data Setup Time Prior to Write | 5 | | 5 | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 5 | | 5 | | ns | |
| $t_{WSA}$ | Address Setup Time Prior to Write[5] | 5 | | 10 | | ns | *Figure 4* |
| $t_{WHA}$ | Address Hold Time after Write | 5 | | 5 | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time Prior to Write | 5 | | 5 | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 5 | | 5 | | ns | |
| $t_{ZWS}$ | Write Disable to HIGH Z | | 35 | | 35 | ns | |
| $t_{WR}$ | Write Recovery Time | | 35 | | 40 | ns | |

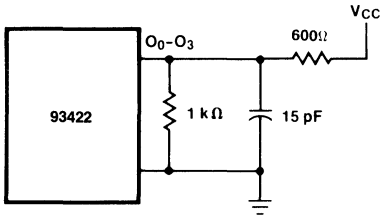
**Military**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 10%, GND = 0 V, $T_A$ = −55°C to +125°C (Notes 1, 3)

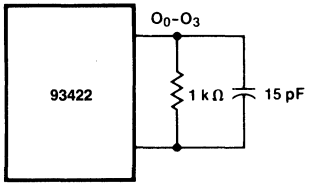
| Symbol | Characteristic | "A" Min | "A" Max | Std Min | Std Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | **Read Timing** | | | | | | |
| $t_{ACS}$ | Chip Select Access Time | | 35 | | 45 | ns | |
| $t_{ZRCS}$ | Chip Select to HIGH Z | | 35 | | 45 | ns | |
| $t_{AOS}$ | Output Enable Access Time | | 35 | | 45 | ns | *Figures 3a, 3b, 3c* |
| $t_{ZROS}$ | Output Enable to HIGH Z | | 35 | | 45 | ns | |
| $t_{AA}$ | Address Access Time | | 45 | | 60 | ns | |
| | **Write Timing** | | | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[5] | 35 | | 40 | | ns | |
| $t_{WSD}$ | Data Setup Time Prior to Write | 5 | | 5 | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 5 | | 5 | | ns | |
| $t_{WSA}$ | Address Setup Time Prior to Write[5] | 5 | | 10 | | ns | *Figure 4* |
| $t_{WHA}$ | Address Hold Time after Write | 5 | | 10 | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time Prior to Write | 5 | | 5 | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 5 | | 10 | | ns | |
| $t_{ZWS}$ | Write Disable to HIGH Z | | 40 | | 45 | ns | |
| $t_{WR}$ | Write Recovery Time | | 40 | | 50 | ns | |

Notes on preceeding page

**Fig. 1 AC Test Load**




LOAD A




LOAD B

**Fig. 2 Input Levels**

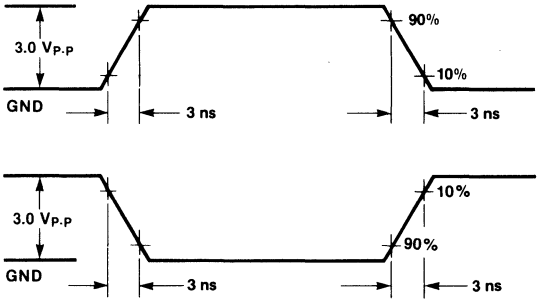
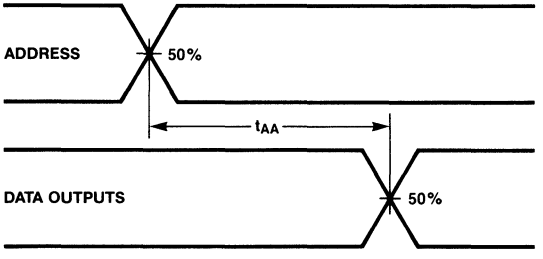
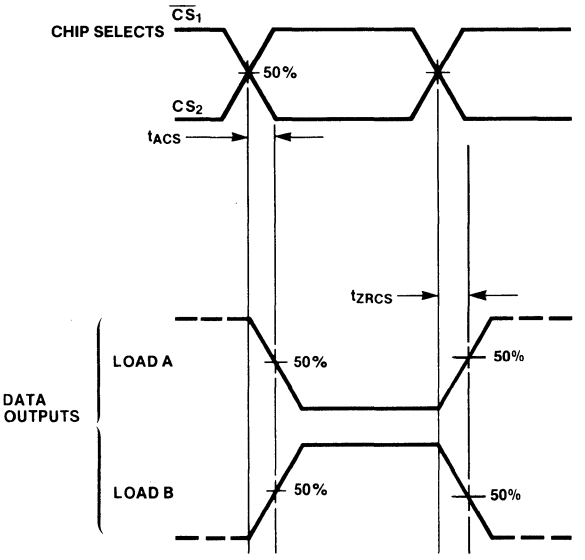



**Fig. 3 Read Mode Timing**

**a Read Mode Propagation Delay from Address**




**b Read Mode Propagation Delay from Chip Select**




**c Read Mode Propagation Delay From Output Enable**

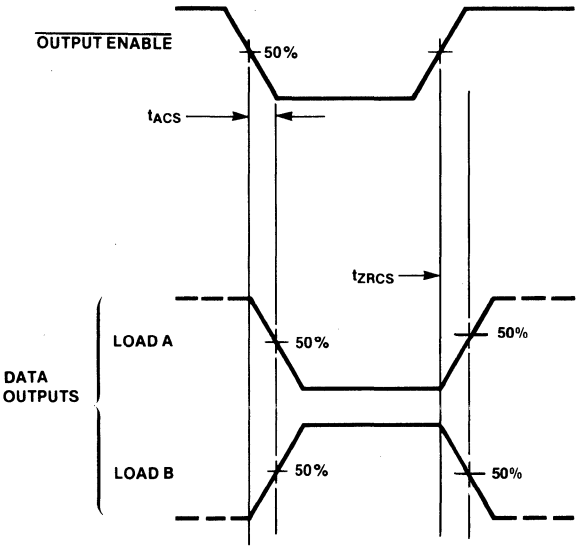



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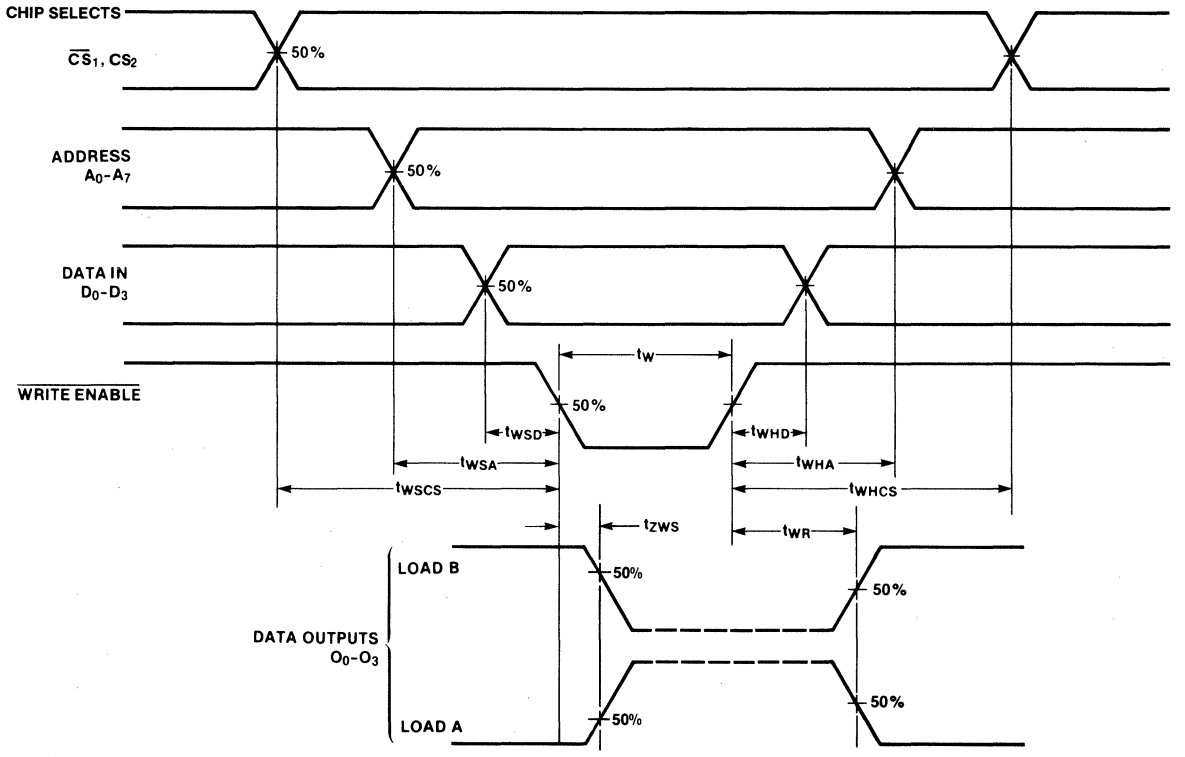
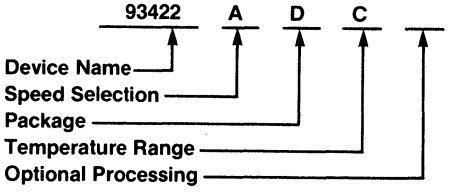
**Fig. 4 Write Mode Timing**




**Note**
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

## Ordering Information




**Speed Selection**
Blank = Standard Speed
A = 'A' Grade

**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier
P = Plastic DIP

**Temperature Range**
C = 0°C to +75°C
M = −55°C to +125°C

**Optional Processing**
QB = Mil Std 883
Method 5004 and 5005, Level B
QC = Mil Std 883
Method 5004 and 5005, Level C
QR = Commercial Device with
160 Hour Burn In

FAIRCHILD
A Schlumberger Company

# 93L422
# 256 x 4-Bit Static Random Access Memory

Bipolar Division

TTL Bipolar Memory

## Description

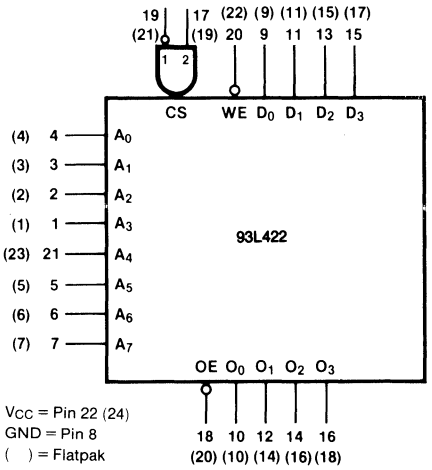
The 93L422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits. It is designed for high speed cache, control and buffer storage applications. The 93L422 is available in two speeds, "standard" speed and an "A" grade. The device includes full on-chip decoding, separate Data inputs and non-inverting Data outputs, as well as two Chip Select lines.

- **Commercial Address Access Time**
  - **93L422 — 60 ns Max**
  - **93L422A — 45 ns Max**
- **Military Address Access Time**
  - **93L422 — 75 ns Max**
  - **93L422A — 55 ns Max**
- **Fully TTL Compatible**
- **Features Three State Outputs**
- **Power Dissipation — 0.25 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $A_0$-$A_7$ | Address Inputs |
| $D_0$-$D_3$ | Data Inputs |
| $\overline{CS}_1$ | Chip Select Input (Active LOW) |
| $CS_2$ | Chip Select Input (Active HIGH) |
| $\overline{WE}$ | Write Enable Input (Active LOW) |
| $\overline{OE}$ | Output Enable Input (Active LOW) |
| $O_0$-$O_3$ | Data Outputs |

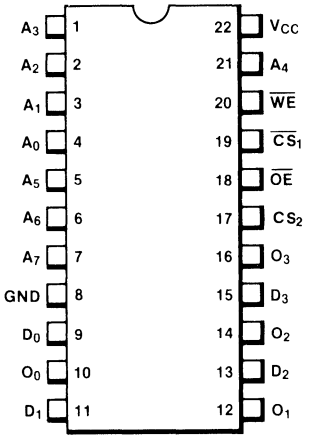
## Logic Symbol



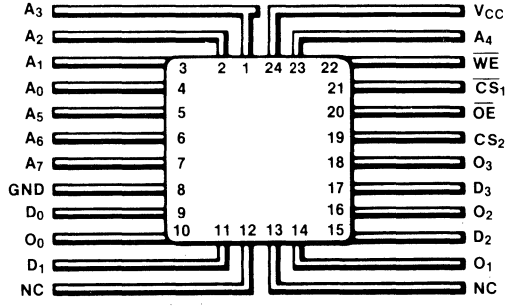

VCC = Pin 22 (24)
GND = Pin 8
( ) = Flatpak

## Connection Diagrams

**22-Pin DIP** (Top View)

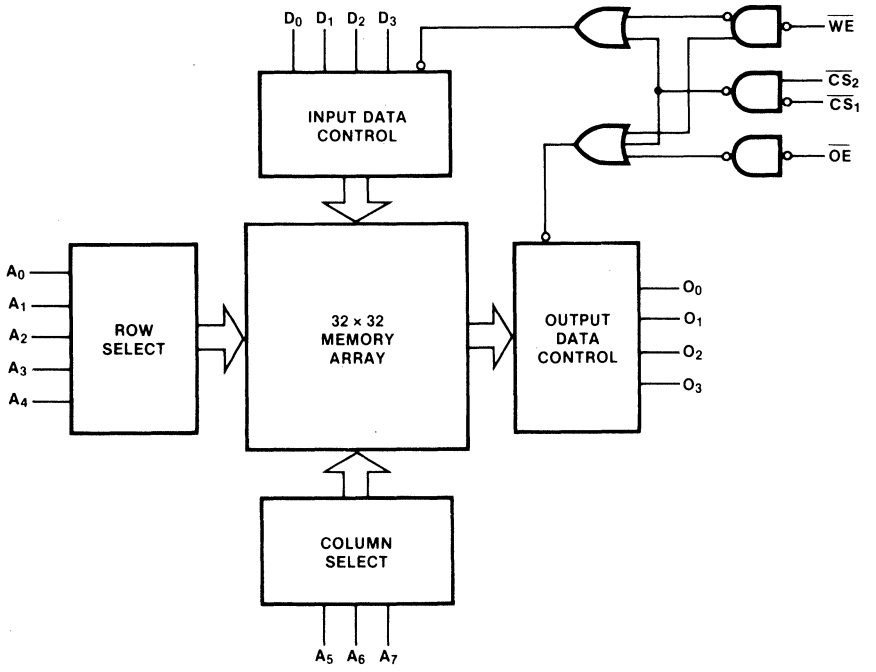



**24-Pin Flatpak** (Top View)




4

**Logic Diagram**




**Functional Description**

The 93L422 is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, $A_0$ through $A_7$.

Two Chip Select inputs, inverting and non-inverting, are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of the chip selects from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. When $\overline{WE}$ is held LOW and the chip is selected, the data at $D_0$-$D_3$ is written into the addressed location. Since the write function is level-triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the outputs ($O_0$-$O_3$).

The 93L422 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.

**Truth Table**

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| $\overline{OE}$ | $\overline{CS_1}$ | $CS_2$ | $\overline{WE}$ | $D_0$-$D_3$ | 3-State | Mode |
| X | H | X | X | X | HIGH Z | Not Selected |
| X | X | L | X | X | HIGH Z | Not Selected |
| L | L | H | H | X | $O_0$-$O_3$ | Read Stored Data |
| L | L | H | L | L | HIGH Z | Write "0" |
| L | L | H | L | H | HIGH Z | Write "1" |
| H | L | H | H | X | HIGH Z | Output Disabled |
| H | L | H | L | L | HIGH Z | Write "0" (Output Disabled) |
| H | L | H | L | H | HIGH Z | Write "1" (Output Disabled) |

H = HIGH Voltage Level (2.4 V)
L = LOW Voltage Level (.5 V)
X = Don't Care (HIGH or LOW)
High Z = High-Impedance

4

**DC Characteristics:** Over operating temperature ranges (Notes 1, 2)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition | |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Output LOW Voltage | | 0.3 | 0.45 | V | $V_{CC}$ = Min, $I_{OL}$ = 8 mA | |
| $V_{IH}$ | Input HIGH Voltage | 2.1 | 1.6 | | V | Guaranteed Input HIGH Voltage for All Inputs[6] | |
| $V_{IL}$ | Input LOW Voltage | | 1.5 | 0.8 | V | Guaranteed Input LOW Voltage for All Inputs[6] | |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $V_{CC}$ = Min, $I_{OH}$ = −5.2 mA | |
| $I_{IL}$ | Input LOW Current | | −150 | −300 | μA | $V_{CC}$ = Max, $V_{IN}$ = 0.4 V | |
| $I_{IH}$ | Input HIGH Current | | 1.0<br>— | 40<br>1.0 | μA<br>mA | $V_{CC}$ = Max, $V_{IN}$ = 4.5 V<br>$V_{CC}$ = Max, $V_{IN}$ = 5.25 V | |
| $V_{IC}$ | Input Diode Clamp Voltage | | −1.0 | −1.5 | V | $V_{CC}$ = Max, $I_{IN}$ = −10 mA | |
| $I_{OFF}$ | Output Current (HIGH Z) | | | 50<br>−50 | μA | $V_{CC}$ = Max, $V_{OUT}$ = 2.4 V<br>$V_{CC}$ = Max, $V_{OUT}$ = 0.5 V | |
| $I_{OS}$ | Output Current Short Circuit to Ground | | | −70 | mA | $V_{CC}$ = Max, Note 4 | |
| $I_{CC}$ | Power Supply Current | | 60<br>69 | 80<br>90 | mA | Commercial<br>Military | $V_{CC}$ = Max<br>All Inputs GND |

**Notes**

1. Operating specification with adequate time for temperature stabilization and transverse airflow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where $T_A = T_J = T_C$. Correlated temperatures, typically 25°C and 100°C, and limits may be used to guarantee performance.
2. Typical values are at $V_{CC}$ = 5.0 V, $T_A$ = +25°C and maximum loading.
3. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
4. Short circuit to ground not to exceed one second.
5. $T_W$ measured at $t_{WSA}$ = Min, $t_{WSA}$ measured at $t_W$ = Min.
6. Static condition only.

**Commercial**
**AC Characteristics:** $V_{CC}$ = 5.0 V ± 5%, GND = 0 V, $T_A$ = 0°C to +75°C (Notes 1, 3)

| Symbol | Characteristic | "A" Min | "A" Max | Std Min | Std Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | **Read Timing** | | | | | | |
| $t_{ACS}$ | Chip Select Access Time | | 30 | | 35 | ns | |
| $t_{ZRCS}$ | Chip Select to HIGH Z | | 30 | | 35 | ns | |
| $t_{AOS}$ | Output Enable Access Time | | 30 | | 35 | ns | *Figures 3a, 3b, 3c* |
| $t_{ZROS}$ | Output Enable to HIGH Z | | 30 | | 35 | ns | |
| $t_{AA}$ | Address Access Time | | 45 | | 60 | ns | |
| | **Write Timing** | | | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[5] | 30 | | 45 | | ns | |
| $t_{WSD}$ | Data Setup Time Prior to Write | 5 | | 5 | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 5 | | 5 | | ns | |
| $t_{WSA}$ | Address Setup Time Prior to Write[5] | 10 | | 10 | | ns | *Figure 4* |
| $t_{WHA}$ | Address Hold Time after Write | 5 | | 5 | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time Prior to Write | 5 | | 5 | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 5 | | 5 | | ns | |
| $t_{ZWS}$ | Write Disable to HIGH Z | | 35 | | 40 | ns | |
| $t_{WR}$ | Write Recovery Time | | 40 | | 45 | ns | |

**Military**
**AC Characteristics:** $V_{CC}$ = 5.0 V ± 10%, GND = 0 V, $T_A$ = −55°C to +125°C (Notes 1, 3)

| Symbol | Characteristic | "A" Min | "A" Max | Std Min | Std Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | **Read Timing** | | | | | | |
| $t_{ACS}$ | Chip Select Access Time | | 40 | | 45 | ns | |
| $t_{ZRCS}$ | Chip Select to HIGH Z | | 40 | | 45 | ns | |
| $t_{AOS}$ | Output Enable Access Time | | 40 | | 45 | ns | *Figures 3a, 3b, 3c* |
| $t_{ZROS}$ | Output Enable to HIGH Z | | 40 | | 45 | ns | |
| $t_{AA}$ | Address Access Time | | 55 | | 75 | ns | |
| | **Write Timing** | | | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[5] | 40 | | 55 | | ns | |
| $t_{WSD}$ | Data Setup Time Prior to Write | 5 | | 5 | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 5 | | 5 | | ns | |
| $t_{WSA}$ | Address Setup Time Prior to Write[5] | 10 | | 10 | | ns | *Figure 4* |
| $t_{WHA}$ | Address Hold Time after Write | 5 | | 10 | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time Prior to Write | 10 | | 5 | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 5 | | 10 | | ns | |
| $t_{ZWS}$ | Write Disable to HIGH Z | | 45 | | 45 | ns | |
| $t_{WR}$ | Write Recovery Time | | 50 | | 50 | ns | |

Notes on preceeding page

**Fig. 1 AC Test Load**

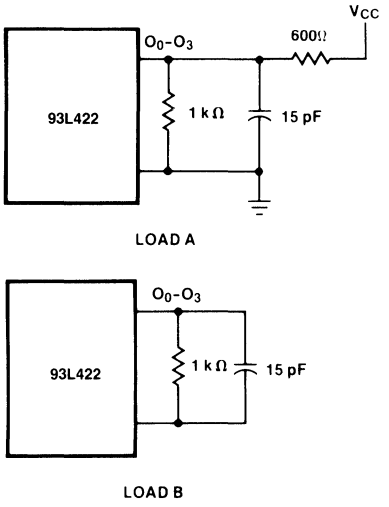



**Fig. 2 Input Levels**

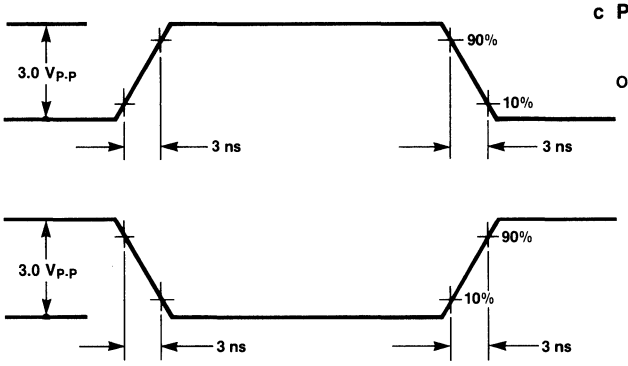
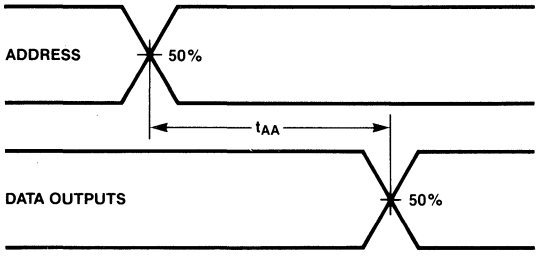
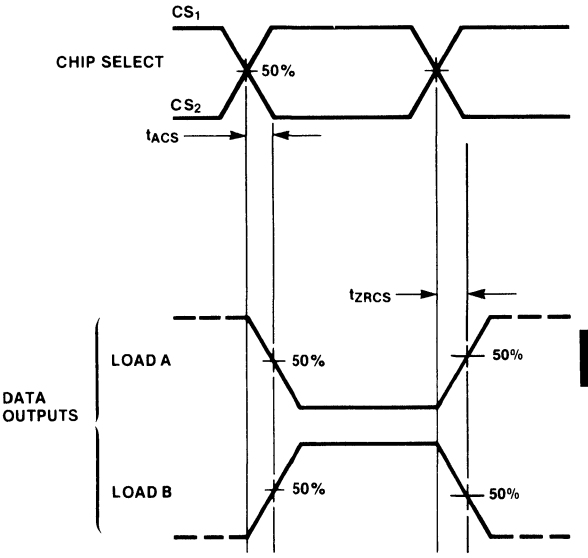



**Fig. 3 Read Mode Timing**

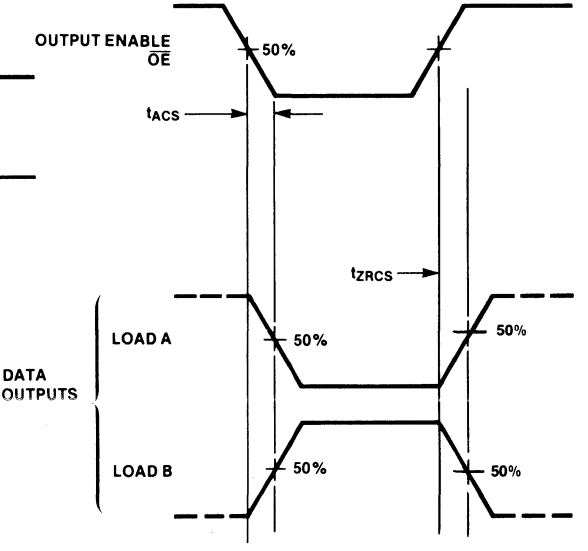
**b Read Mode Propagation Delay from Address**




**b Propagation Delay from Chip Select**

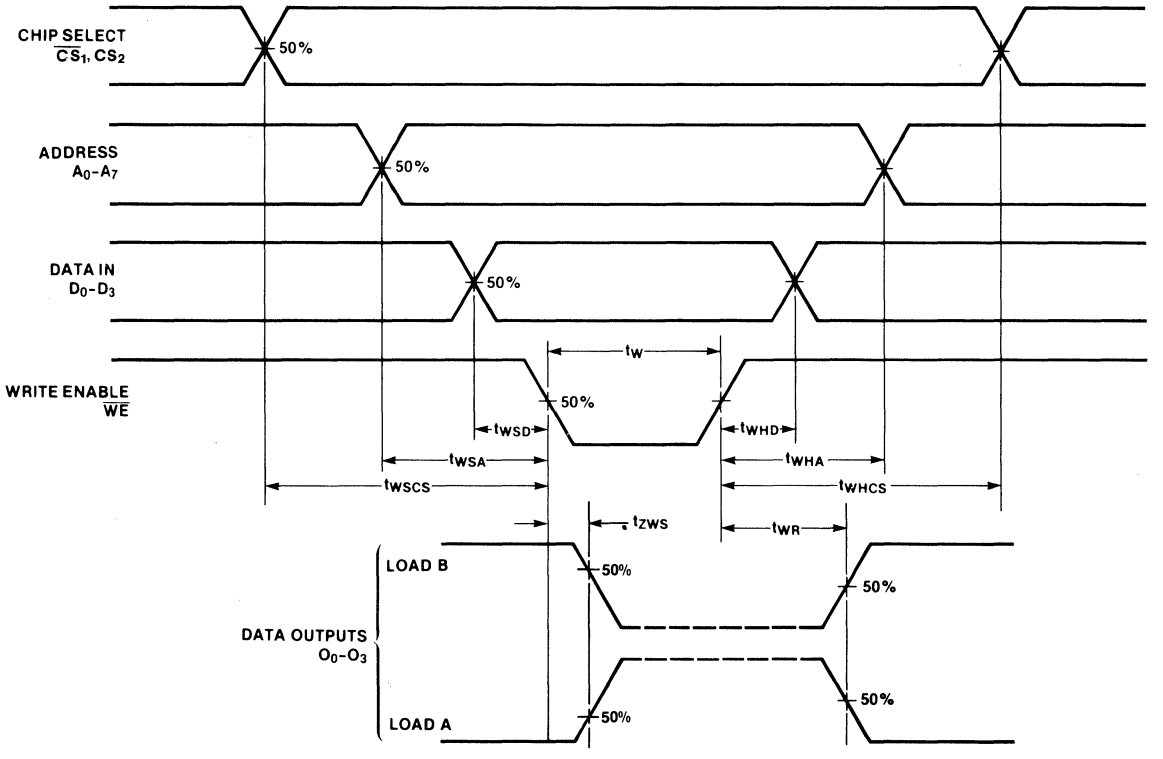



**c Propagation Delay From Output Enable**



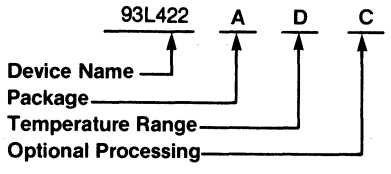

4

**Fig. 4 Write Mode Timing**




**Note:**
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

## Ordering Information




**Speed Selection**
Blank = Standard Speed
A = 'A' Grade (Commercial Only)

**Packages and Outlines** (See Section 10)

| | |
|---|---|
| D = Ceramic DIP | 6S |
| F = Flatpak | 4P |
| L = Leadless Chip Carrier | 2J |
| P = Plastic DIP | 4K |

**Temperature Range**
C = 0°C to +75°C
M = −55°C to +125°C

**Optional Processing**
QB = Mil Std 883
Method 5004 and 5005, Level B
QC = Mil Std 883
Method 5004 and 5005, Level C
QR = Commercial Device with
160 Hour Burn In

FAIRCHILD
A Schlumberger Company

Bipolar Division

# 93425
# 1024 x 1-Bit Static Random Access Memory

TTL Bipolar Memory

## Description

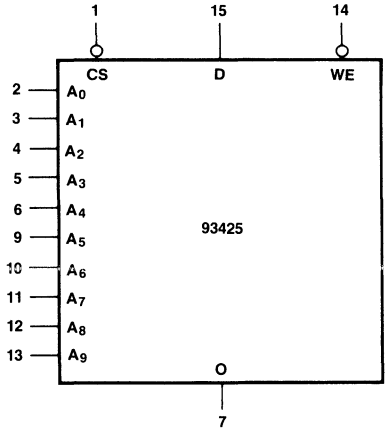
The 93425 is a 1024-bit read/write Random Access Memory (RAM), organized 1024 words by one bit. It is designed for high speed cache, control and buffer storage applications. The commercial version of the 93425 is available in two speeds, "standard" speed and an "A" grade. The device includes full on-chip decoding, separate Data input and non-inverting Data output, as well as an active LOW Chip Select line.

- **Commercial Address Access Time**
  - **93425 — 45 ns Max**
  - **93425A — 30 ns Max**
- **Military Address Access Time**
  - **93425 — 60 ns Max**
  - **93425A — 45 ns Max**
- **Features Three State Output**
- **Power Dissipation — 0.46 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $\overline{CS}$ | Chip Select (Active LOW) |
| $A_0$-$A_9$ | Address Inputs |
| $\overline{WE}$ | Write Enable (Active LOW) |
| D | Data Input |
| O | Data Output |

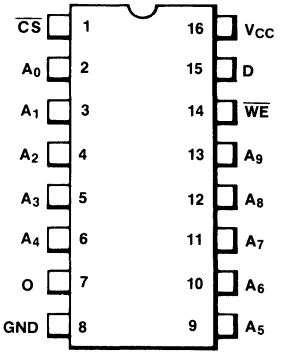
## Logic Symbol




$V_{CC}$ = Pin 16
GND = Pin 8

## Connection Diagram

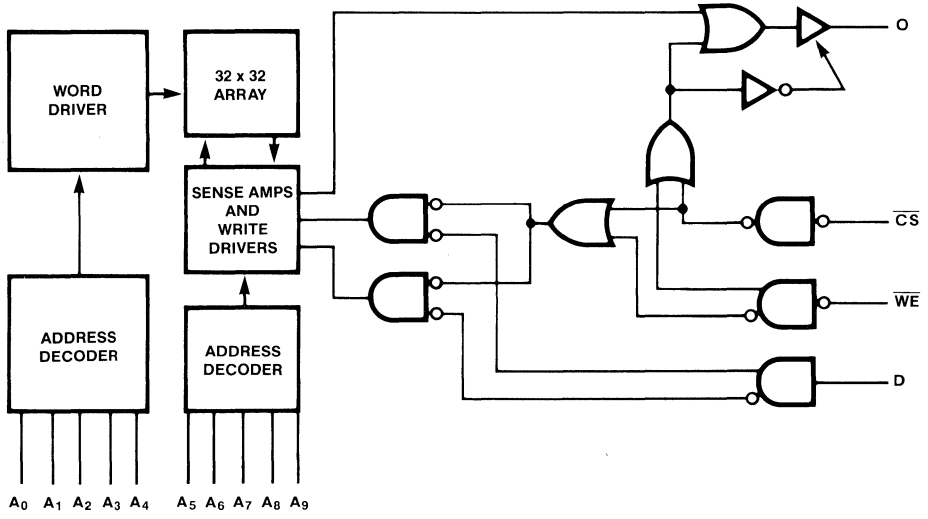
**16-Pin DIP** (Top View)




**Note:**
The 16 pin Flatpak version has the same pinout connections as the Dual In-line package.

4

## Logic Diagram




### Functional Description

The 93425 is a fully decoded 1024-bit read/write Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, $A_0$ through $A_9$.

One Chip Select input is provided for easy memory array expansion of up to 2048 bits without the need for external decoding. For larger memories, the fast chip select access time permits direct address decoding without an increase in overall memory access time.

The read and write functions of the 93425 are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. When $\overline{WE}$ is held LOW and the chip is selected, the data at D is written into the location specified by the binary address present at $A_0$ through $A_9$. Since the write function is level triggered, data must be held stable at the data input for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. When $\overline{WE}$ is held HIGH and the chip selected, data is read from the addressed location and presented at the output (O).

The 93425 has a three-state output which provides an active pull-up or pull-down when enabled and a high impedance (HIGH Z) state when disabled. The active pull-up provides drive capability for high capacative loads while the high impedance state allows optimization of word expansion in bus organized systems.

### Truth Table

| Inputs | | | Output | |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | D | O | Mode |
| H | X | X | HIGH Z | Not Selected |
| L | L | L | HIGH Z | Write "0" |
| L | L | H | HIGH Z | Write "1" |
| L | H | X | $D_{OUT}$ | Read |

H = HIGH Voltage Level (2.4 V)
L = LOW Voltage Level (.5 V)
X = Don't Care (HIGH or LOW)

**DC Characteristics:** Over operating temperature ranges (Notes 1, 2)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition | |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Output LOW Voltage | | 0.3 | 0.45 | V | $V_{CC}$ = Min, $I_{OL}$ = 16 mA | |
| $V_{IH}$ | Input HIGH Voltage | 2.1 | 1.6 | | V | Guaranteed Input HIGH Voltage for All Inputs[6] | |
| $V_{IL}$ | Input LOW Voltage | | 1.5 | 0.8 | V | Guaranteed Input LOW Voltage for All Inputs[6] | |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $V_{CC}$ = Min, $I_{OH}$ = −5.2 mA | |
| $I_{IL}$ | Input LOW Current | | −250 | −400 | μA | $V_{CC}$ = Max, $V_{IN}$ = 0.4 V | |
| $I_{IH}$ | Input HIGH Current | | 1.0 | 40<br>1.0 | μA<br>mA | $V_{CC}$ = Max, $V_{IN}$ = 4.5 V<br>$V_{CC}$ = Max, $V_{IN}$ = 5.25 V | |
| $V_{IC}$ | Input Diode Clamp Voltage | | −1.0 | −1.5 | V | $V_{CC}$ = Max, $I_{IN}$ = −10 mA | |
| $I_{OFF}$ | Output Current (HIGH Z) | | | 50<br>−50 | μA | $V_{CC}$ = Max, $V_{OUT}$ = 2.4 V<br>$V_{CC}$ = Max, $V_{OUT}$ = 0.5 V | |
| $I_{OS}$ | Output Current Short Circuit to Ground | | | −100 | mA | $V_{CC}$ = Max, *Note 4* | |
| $I_{CC}$ | Power Supply Current | | 95 | 155<br>170 | mA | Commercial<br>Military | $V_{CC}$ = Max<br>All Inputs GND |

**Notes**

1. Operating specification with adequate time for temperature stabilization and transverse airflow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where $T_A = T_J = T_C$. Correlated temperatures, typically 25°C and 100°C, and limits may be used to guarantee performance.
2. Typical values are at $V_{CC}$ = 5.0 V, $T_A$ = +25°C and maximum loading.
3. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
4. Short circuit to ground not to exceed one second.
5. $t_W$ measured at $t_{WSA}$ = Min, $t_{WSA}$ measured at $t_W$ = Min.
6. Static condition only.

**Commercial**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 5%, GND = 0 V, $T_A$ = 0°C to +75°C (Notes 1, 3)

| Symbol | Characteristic | "A" Min | "A" Max | Std Min | Std Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | **Read Timing** | | | | | | |
| $t_{ACS}$ | Chip Select Access Time | | 20 | | 35 | ns | |
| $t_{ZRCS}$ | Chip Select to HIGH Z | | 20 | | 35 | ns | *Figures 3a, 3b* |
| $t_{AA}$ | Address Access Time | | 30 | | 45 | ns | |
| | **Write Timing** | | | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[5] | 20 | | 35 | | ns | |
| $t_{WSD}$ | Data Setup Time Prior to Write | 5 | | 5 | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 5 | | 5 | | ns | |
| $t_{WSA}$ | Address Setup Time Prior to Write[5] | 5 | | 5 | | ns | *Figures 4a, 4b* |
| $t_{WHA}$ | Address Hold Time after Write | 5 | | 5 | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time Prior to Write | 5 | | 5 | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 5 | | 5 | | ns | |
| $t_{ZWS}$ | Write Disable to HIGH Z | | 20 | | 35 | ns | |
| $t_{WR}$ | Write Recovery Time | | 25 | | 40 | ns | |

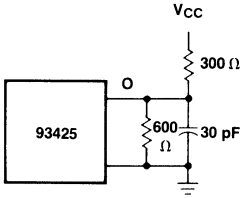
**Military**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 10%, GND = 0 V, $T_A$ = −55°C to +125°C (Notes 1, 3)

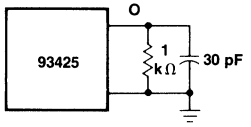
| Symbol | Characteristic | "A" Min | "A" Max | Std Min | Std Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | **Read Timing** | | | | | | |
| $t_{ACS}$ | Chip Select Access Time | | 35 | | 45 | ns | |
| $t_{ZRCS}$ | Chip Select to HIGH Z | | 35 | | 50 | ns | *Figures 3a, 3b* |
| $t_{AA}$ | Address Access Time | | 45 | | 60 | ns | |
| | **Write Timing** | | | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[5] | 35 | | 40 | | ns | |
| $t_{WSD}$ | Data Setup Time Prior to Write | 5 | | 5 | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 5 | | 5 | | ns | |
| $t_{WSA}$ | Address Setup Time Prior to Write[5] | 5 | | 15 | | ns | *Figures 4a, 4b* |
| $t_{WHA}$ | Address Hold Time after Write | 5 | | 5 | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time Prior to Write | 5 | | 5 | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 5 | | 5 | | ns | |
| $t_{ZWS}$ | Write Disable to HIGH Z | | 35 | | 45 | ns | |
| $t_{WR}$ | Write Recovery Time | | 40 | | 50 | ns | |

Notes on preceeding page

Fig. 1 AC Test Output Load




LOAD A




LOAD B

Fig. 2 Input Levels

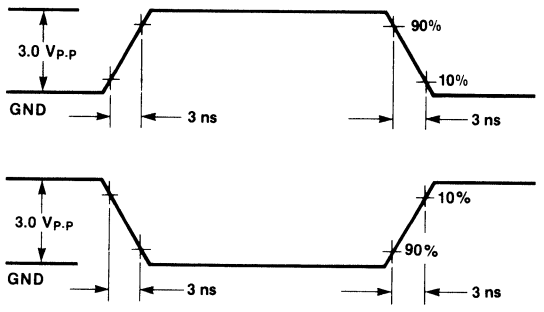
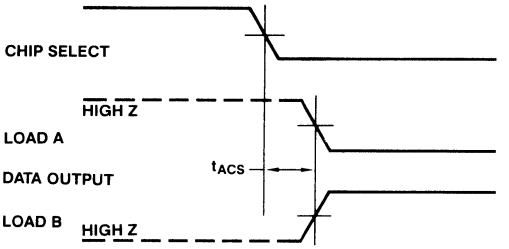
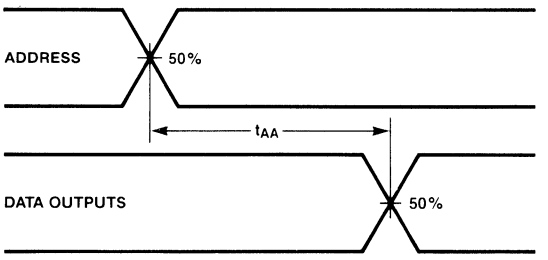



Fig. 3 Read Mode Timing

a Read Mode Propagation Delay from Address




b Read Mode Propagation Delay from Address




4

**Fig. 4a Write Mode Timing**

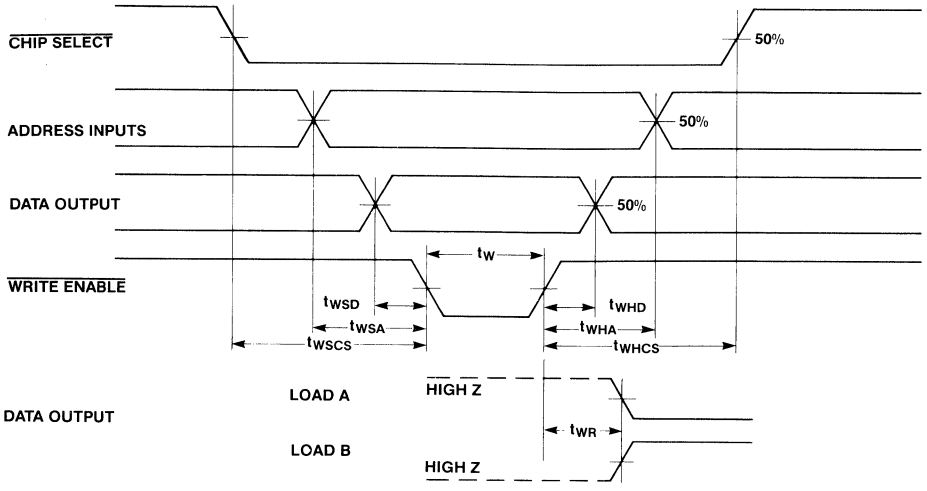
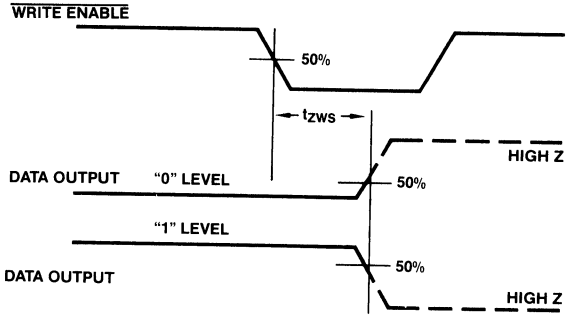
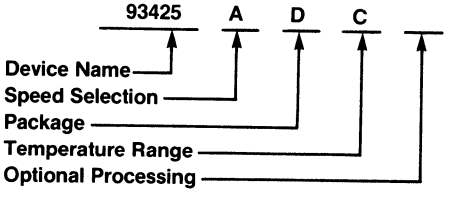


**Fig. 4b Write Enable to HIGH Z Delay**






## Ordering Information




**Speed Selection**
Blank = Standard Speed
A = 'A' Grade

**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier
P = Plastic DIP

**Temperature Range**
C = 0°C to +75°C
M = −55°C to +125°C

**Optional Processing**
QB = Mil Std 883
Method 5004 and 5005, Level B
QC = Mil Std 883
Method 5004 and 5005, Level C
QR = Commercial Device with
160 Hour Burn In

FAIRCHILD
A Schlumberger Company

# 93L425
# 1024 x 1-Bit Static Random Access Memory

**Advanced Bipolar Division** | **TTL Bipolar Memory**

## Description

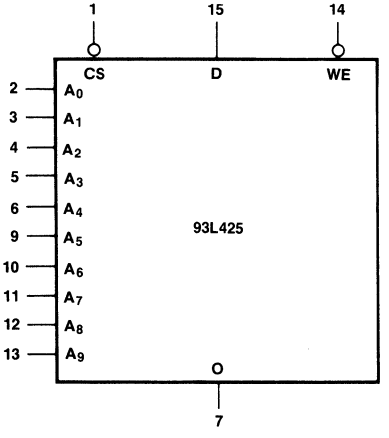
The 93L425 is a 1024-bit read/write Random Access Memory (RAM), organized 1024 words by one bit. It is designed for high speed cache, control and buffer storage applications. The commercial version of the 93L425 is available in two speeds, "standard" speed and an "A" grade. The device includes full on-chip decoding, separate Data input and non-inverting Data output, as well as an active LOW Chip Select line.

- **Commercial Address Access Time — 60 ns Max**
- **Military Address Access Time — 70 ns Max**
- **Features Three State Output**
- **Power Dissipation — 0.22 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $\overline{CS}$ | Chip Select (Active LOW) |
| $A_0 - A_9$ | Address Inputs |
| $\overline{WE}$ | Write Enable (Active LOW) |
| D | Data Input |
| O | Data Output |

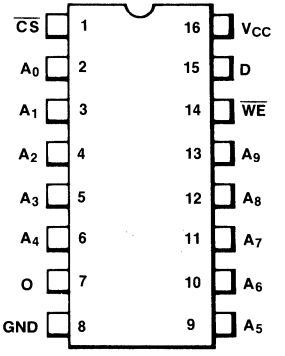
## Logic Symbol




$V_{CC}$ = Pin 16
GND = Pin 8

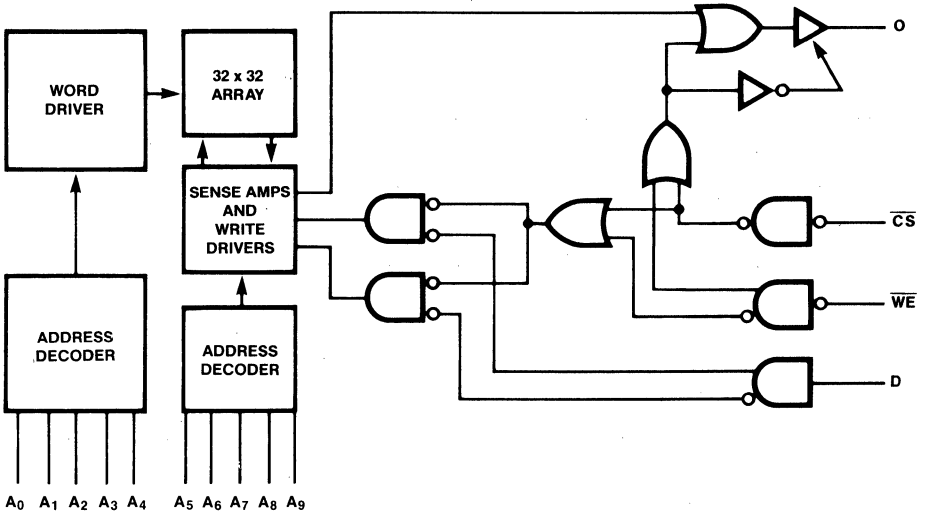
## Connection Diagram

**16 Pin DIP** (Top View)




**Note:**
The 16-pin Flatpak version has the same pinout connections as the Dual In-line package.

## Logic Symbol






### Functional Description

The 93L425 is a fully decoded 1024-bit read/write Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, $A_0$ through $A_9$.

One Chip Select input is provided for easy memory array expansion of up to 2048 bits without the need for external decoding. For larger memories, the fast chip select access time permits direct address decoding without an increase in overall memory access time.

The read and write functions of the 93L425 are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. When $\overline{WE}$ is held LOW and the chip is selected, the data at D is written into the location specified by the binary address present at $A_0$ through $A_9$. Since the write function is level triggered, data must be held stable at the data input for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. When $\overline{WE}$ is held HIGH and the chip selected, data is read from the addressed location and presented at the output (O).

The 93L425 has a three-state output which provides an active pull-up or pull-down when enabled and a high impedance (HIGH Z) state when disabled. The active pull-up provides drive capability for high capacative loads while the high impedance state allows optimization of word expansion in bus organized systems.

### Truth Table

| Inputs | | | Output | |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | D | O | Mode |
| H | X | X | HIGH Z | Not Selected |
| L | L | L | HIGH Z | Write "0" |
| L | L | H | HIGH Z | Write "1" |
| L | H | X | $D_{OUT}$ | Read |

H = HIGH Voltage Level (2.4 V)
L = LOW Voltage Level (.5 V)
X = Don't Care (HIGH or LOW)

**DC Characteristics:** Over operating temperature ranges (Notes 1, 2)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition | |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Output LOW Voltage | | 0.35 | 0.45 | V | $V_{CC}$ = Min, $I_{OL}$ = 16 mA | |
| $V_{IH}$ | Input HIGH Voltage | 2.1 | 1.6 | | V | Guaranteed Input HIGH Voltage for All Inputs[6] | |
| $V_{IL}$ | Input LOW Voltage | | 1.5 | 0.8 | V | Guaranteed Input LOW Voltage for All Inputs[6] | |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $V_{CC}$ = Min, $I_{OH}$ = −5.2 mA | |
| $I_{IL}$ | Input LOW Current | | −150 | −300 | μA | $V_{CC}$ = Max, $V_{IN}$ = 0.4 V | |
| $I_{IH}$ | Input HIGH Current | | 1.0 | 40<br>1.0 | μA<br>mA | $V_{CC}$ = Max, $V_{IN}$ = 4.5 V<br>$V_{CC}$ = Max, $V_{IN}$ = 5.25 V | |
| $V_{IC}$ | Input Diode Clamp Voltage | | −1.0 | −1.5 | V | $V_{CC}$ = Max, $I_{IN}$ = −10 mA | |
| $I_{OFF}$ | Output Current (HIGH Z) | | | 50<br>−50 | μA | $V_{CC}$ = Max, $V_{OUT}$ = 2.4 V<br>$V_{CC}$ = Max, $V_{OUT}$ = 0.5 V | |
| $I_{OS}$ | Output Current Short Circuit to Ground | | | −100 | mA | $V_{CC}$ = Max, *Note 4* | |
| $I_{CC}$ | Power Supply Current | | 45 | 65<br>75 | mA | Commercial<br>Military | $V_{CC}$ = Max<br>All Inputs GND |

**Notes**

1. Operating specification with adequate time for temperature stabilization and transverse airflow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where $T_A = T_J = T_C$. Correlated temperatures, typically 25°C and 100°C, and limits may be used to guarantee performance.
2. Typical values are at $V_{CC}$ = 5.0 V, $T_A$ = +25°C and maximum loading.
3. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
4. Short circuit to ground not to exceed one second.
5. $T_W$ measured at $t_{WSA}$ = Min, $t_{WSA}$ measured at $t_W$ = Min.
6. Static condition only.

**Commercial**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 5%, GND = 0 V, $T_A$ = 0°C to +75°C (Notes 1, 3)

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| | **Read Timing** | | | | |
| $t_{ACS}$ | Chip Select Access Time | | 40 | ns | |
| $t_{ZRCS}$ | Chip Select to HIGH Z | | 40 | ns | *Figures 3a, 3b* |
| $t_{AA}$ | Address Access Time | | 60 | ns | |
| | **Write Timing** | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[5] | 45 | | ns | |
| $t_{WSD}$ | Data Setup Time Prior to Write | 5 | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 5 | | ns | |
| $t_{WSA}$ | Address Setup Time Prior to Write[5] | 10 | | ns | *Figure 4a, 4b* |
| $t_{WHA}$ | Address Hold Time after Write | 5 | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time Prior to Write | 5 | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 5 | | ns | |
| $t_{ZWS}$ | Write Disable to HIGH Z | | 45 | ns | |
| $t_{WR}$ | Write Recovery Time | | 45 | ns | |

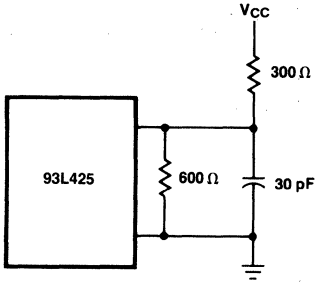
**Military**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 10%, GND = 0 V, $T_A$ = −55°C to +125°C (Notes 1, 3)

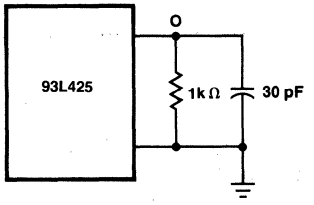
| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| | **Read Timing** | | | | |
| $t_{ACS}$ | Chip Select Access Time | | 45 | ns | |
| $t_{ZRCS}$ | Chip Select to HIGH Z | | 50 | ns | *Figures 3a, 3b* |
| $t_{AA}$ | Address Access Time | | 70 | ns | |
| | **Write Timing** | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[5] | 50 | | ns | |
| $t_{WSD}$ | Data Setup Time Prior to Write | 10 | | ns | |
| $t_{WHD}$ | Data Hold Time after Write | 10 | | ns | |
| $t_{WSA}$ | Address Setup Time Prior to Write[5] | 10 | | ns | *Figure 4a, 4b* |
| $t_{WHA}$ | Address Hold Time after Write | 10 | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time Prior to Write | 10 | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 5 | | ns | |
| $t_{ZWS}$ | Write Disable to HIGH Z | | 45 | ns | |
| $t_{WR}$ | Write Recovery Time | | 55 | ns | |

Notes on preceeding page

Fig. 4 AC Test Output Load




LOAD A




LOAD B

Fig. 2 Input Levels

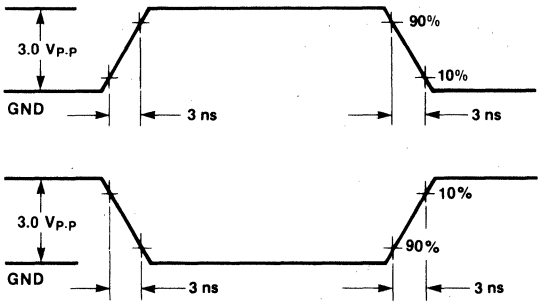
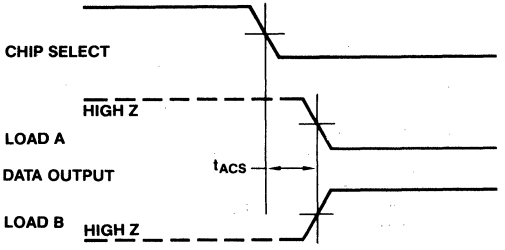



Fig. 3 Read Mode Timing

a Read Mode Propagation Delay from Chip Select




b Read Mode Propagation Delay from Address

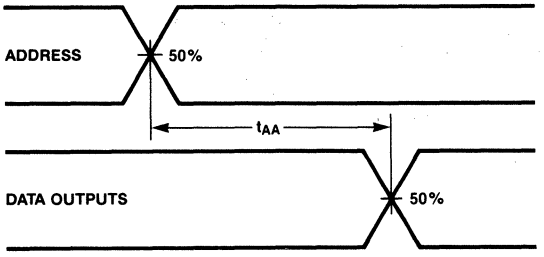


Fig. 4 Write Mode Timing

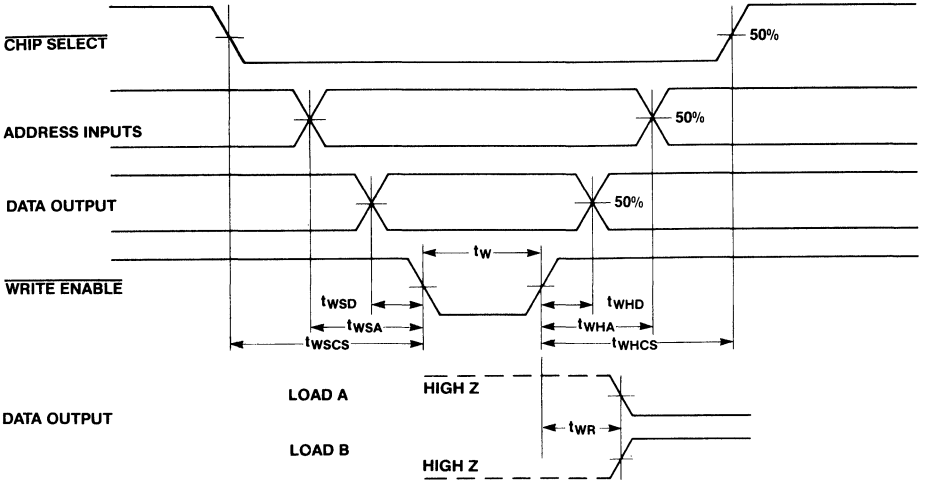
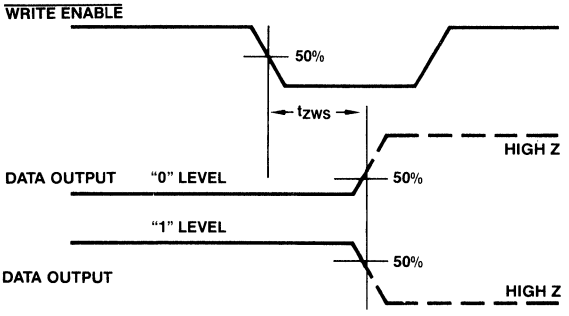
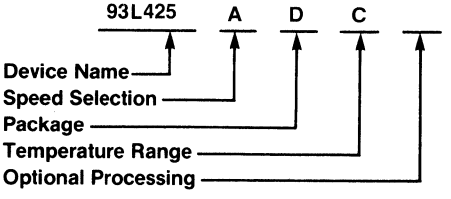


**Fig. 4b Write Enable to HIGH Z Delay**




**Speed Selection**
Blank = High Speed
A = 'A' Grade

**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier
P = Plastic DIP

**Temperature Ranges**
C = 0°C to +75°C
M = −55°C to +125°C

**Optional Processing**
QB = Mil Std 883
Method 5004 & 5005, Level B
QC = Mil Std 883
Method 5004 & 5005, Level C
QR = Commercial Device with
160 Hour Burn In

FAIRCHILD
A Schlumberger Company

# 93475
# 1024 x 4-Bit Static Random Access Memory

Bipolar Division

TTL Bipolar Memory

## Description

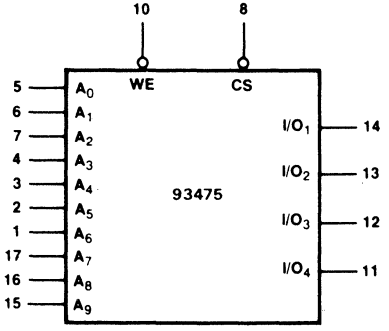
The 93475 is a 4096-bit read/write Random Access Memory (RAM), organized 1024 words by four bits per word. It is designed for high speed cache, control and buffer torage applications. The military version of the 93475 is available in two speeds, "standard" speed and an "A" grade. The device includes full on-chip decoding and an active LOW Chip Select line.

- **Address Access Time — 45 ns Max**
- **Chip Select Access Time — 35 ns Max**
- **Features Three State Outputs**
- **Common Data I/O's**
- **Industry Standard 2114 Pinout**
- **Power Dissipation — 0.16 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $A_0$-$A_9$ | Address Inputs |
| $\overline{CS}$ | Chip Select Input (Active LOW) |
| $\overline{WE}$ | Write Enable Input (Active LOW) |
| $I/O_1$-$I/O_4$ | Data Input/Data Outputs |

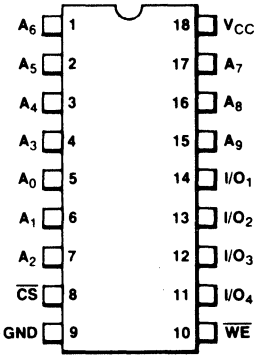
## Logic Symbol




$V_{CC}$ = Pin 18
GND = Pin 9

## Connection Diagram

**18-Pin DIP** (Top View)

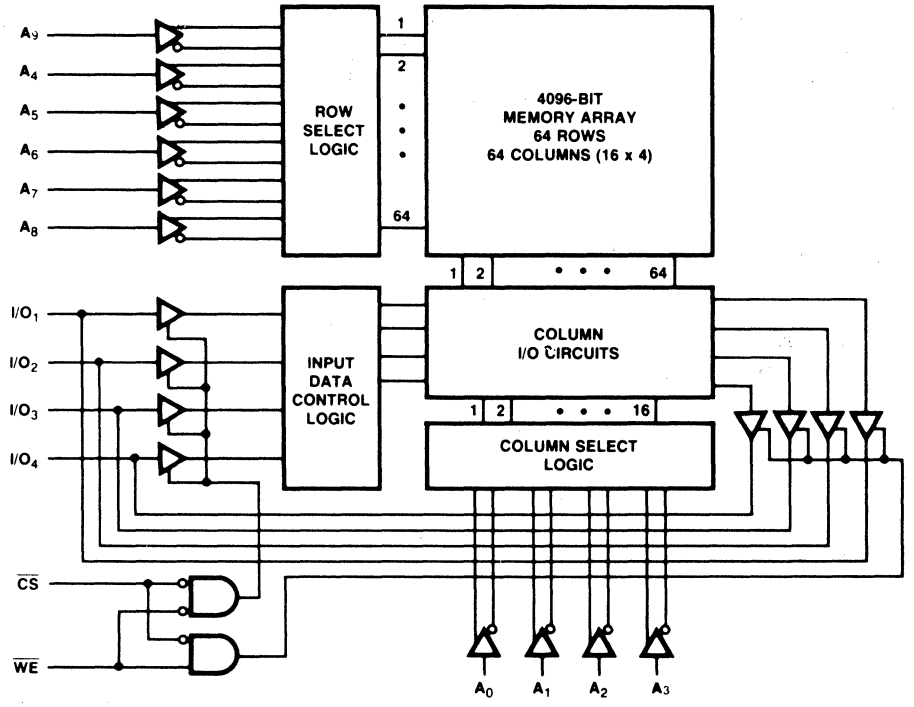



**Note:**
The 18-pin Flatpak version has the same pinout connections as the Dual In-line package.



4

## Logic Diagram




### Functional Description

The 93475 is a fully decoded 4096-bit read/write Random Access Memory organized 1024 words by four bits per word. Word selection is achieved by means of a 10-bit address, $A_0$ through $A_9$.

One Chip Select input is provided for logic flexibility or for memory array expansion of up to 8196 bits without the need for external decoding. For larger memories, the fast chip select access time permits the decoding of Chip Select, ($\overline{CS}$) from the address without affecting system performance.

The read and write functions of the 93475 are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. When $\overline{WE}$ is held LOW and the chip is selected, the data at $I/O_1$ through $I/O_4$ is written into the addressed locations. Since the write function is level triggered, data must be held stable at the data input for at least $t_{WSD(min)}$ plus $t_{W(min)}$ to insure a valid write.

When $\overline{WE}$ is held HIGH and the chip selected, data is read from the addressed location and presented at the outputs ($I/O_1$-$I/O_4$).

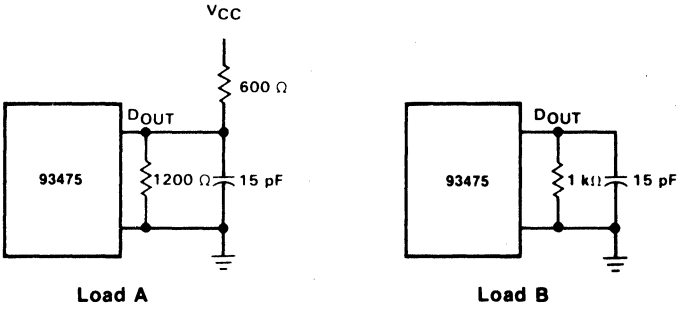
The 93475 has three-state outputs for use in bus organized systems.

### Truth Table

| Inputs | | | |
|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | $I/O_1$-$I/O_4$ | Mode |
| H | X | HIGH Z | Not Selected |
| L | H | $D_{OUT}$ | Read |
| L | L | $D_{IN}$ HIGH Z | Write |

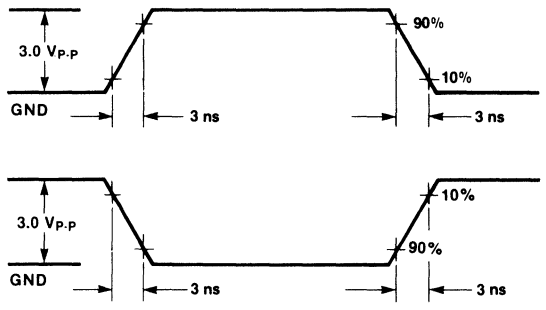
H = HIGH Voltage Level (2.4 V)
L = LOW Voltage Level (.5 V)
X = Don't Care (HIGH or LOW)

**Fig. 1 AC Test Load Output Load**




**Loading Conditions**

**Fig. 2 Input Levels**



FAIRCHILD
A Schlumberger Company

# 93479
# 256 x 9-Bit Static Random Access Memory

Bipolar Division

TTL Bipolar Memory

## Description

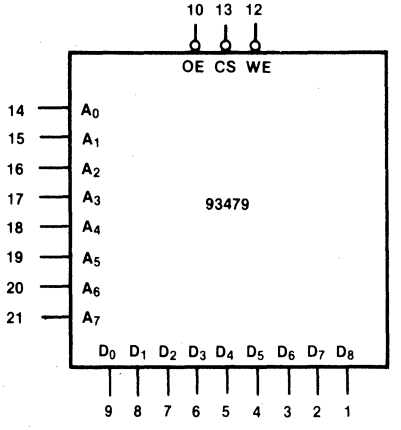
The 93479 is a 2304-bit read/write Random Access Memory (RAM), organized as 256 words by nine bits per word. It is ideally suited for scratchpad, small buffer and other applications where the number of required words is small and where the number of required bits per word is relatively large. The ninth bit can be used to provide parity for 8-bit word systems.

- **Commercial Address Access Time — 45 ns Max**
- **Military Address Access Time — 60 ns Max**
- **Common Data Input/Outputs**
- **Features Three State Outputs**
- **Power Dissipation — 0.29 mW/Bit Typ**

## Pin Names

| | |
|---|---|
| $A_0$-$A_7$ | Address Inputs |
| $D_0$-$D_8$ | Data Input/Outputs |
| $\overline{OE}$ | Output Enable Input (Active LOW) |
| $\overline{WE}$ | Write Enable Input (Active LOW) |
| $\overline{CS}$ | Chip Select Input (Active LOW) |

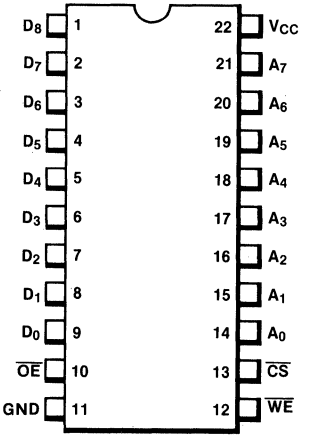
## Logic Symbol



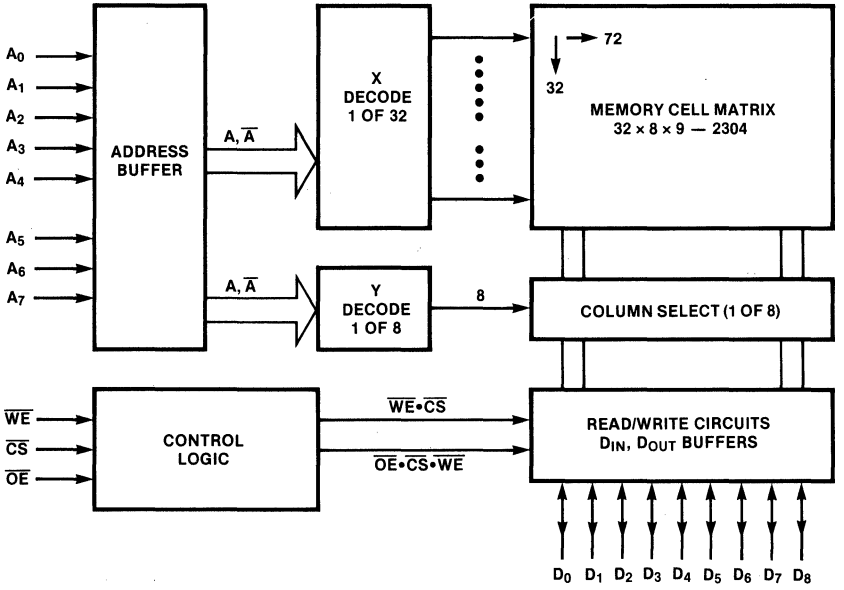

$V_{CC}$ = Pin 22
GND = Pin 11

## Connection Diagram

**22-Pin DIP** (Top View)



## Logic Diagram




### Functional Description

The 93479 is a fully decoded 2304-bit random access memory organized 256 words by nine bits. Word selection is achieved by means of an 8-bit address, $A_0$ to $A_7$.

The Chip Select input provides for memory array expansion. For larger memories, the fast chip select access time permits decoding without an increase in overall memory access time.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW, the chip selected, and the output disabled, the data at $D_0$-$D_8$ is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH, the chip selected and the outputs enabled. Non-inverted data is then presented at the outputs ($D_0$-$D_8$).

The 93479 has three-state outputs which provides an active pull-up or pull-down when enabled and a high impedance (HIGH Z) state when disabled. The active pull-ups provide drive capability for high capacative loads while the high impedance state allows optimization of word expansion in bus organized systems. During writing, the output is held in the high impedance state.

### Truth Table

| Inputs | | | Data In/Out | |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | $D_0$-$D_8$ | Mode |
| X | H | X | HIGH Z | Output Disabled |
| H | X | X | HIGH Z | R/W Disabled |
| L | L | H | Data Out | Read |
| L | L | L | Data In | Write |

H = HIGH Voltage Level (2.4 V)
L = LOW Voltage Level (.5 V)
X = Don't Care (HIGH or LOW)
HIGH Z = High Impedance State

**DC Characteristics:** Over operating temperature ranges (Notes 1, 2)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition | |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Output LOW Voltage | | 0.3 | 0.5 | V | $V_{CC}$ = Min, $I_{OL}$ = 8.0 mA | |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $V_{CC}$ = Min, $I_{OH}$ = −5.2 mA | |
| $V_{IH}$ | Input HIGH Voltage | 2.1 | 1.6 | | V | Guaranteed Input HIGH Voltage for All Inputs[6] | |
| $V_{IL}$ | Input LOW Voltage | | 1.5 | 0.8 | V | Guaranteed Input LOW Voltage for All Inputs[6] | |
| $I_{IL}$ | Input LOW Current | | −250 | −400 | μA | $V_{CC}$ = Max, $V_{IN}$ = 0.4 V | |
| $I_{IH}$ | Input HIGH Current | | 1.0 | 40<br>1.0 | μA<br>mA | $V_{CC}$ = Max, $V_{IN}$ = 4.5 V<br>$V_{CC}$ = Max, $V_{IN}$ = 5.25 V | |
| $I_{OFF}$ | Output Current (HIGH Z) | | <br>−50 | 50<br>−400 | μA<br>μA | $V_{CC}$ = Max, $V_{OUT}$ = 2.4 V<br>$V_{CC}$ = Max, $V_{OUT}$ = 0.5 V | |
| $V_{IC}$ | Input Diode Clamp Voltage | | −1.0 | −1.5 | V | $V_{CC}$ = Max, $I_{IN}$ = −10 mA | |
| $I_{OS}$ | Output Current Short Circuit to Ground | | | −70 | mA | $V_{CC}$ = Max, Note 4 | |
| $I_{CC}$ | Power Supply Current | | 135<br>135 | 185<br>200 | mA | Commercial<br>Military | $V_{CC}$ = Max<br>All Inputs GND |

**Notes**

1. Operating specification with adequate time for temperature stabilization and transverse airflow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where $T_A = T_J = T_C$. Correlated temperatures, typically 25°C and 100°C, and limits may be used to guarantee performance.
2. Typical values are at $V_{CC}$ = 5.0 V, $T_A$ = +25°C and maximum loading.
3. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
4. Short circuit to ground not to exceed one second.
5. $T_W$ measured at $t_{WSA}$ = Min, $t_{WSA}$ measured at $t_W$ = Min.
6. Static condition only.

**Commercial**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 5%, GND = 0 V, $T_A$ = 0°C to +75°C (Notes 1, 3)

| Symbol | Characteristic | "A" Min | "A" Max | Std Min | Std Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | **Read Timing** | | | | | | |
| $t_{ACS}$ | Chip Select Access Time | | 25 | | 25 | ns | |
| $t_{ZRCS}$ | Chip Select to HIGH Z | | 25 | | 25 | ns | |
| $t_{AOS}$ | Output Enable Access Time | | 25 | | 25 | ns | *Figures 3a, 3b, 3c* |
| $t_{ZROS}$ | Output Enable to HIGH Z | | 25 | | 25 | ns | |
| $t_{AA}$ | Address Access Time | | 35 | | 45 | ns | |
| | **Write Timing** | | | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[5] | 25 | | 25 | | ns | |
| $t_{SO}$ | Output Enable Setup Time | 5 | | 5 | | ns | |
| $t_{HO}$ | Data Enable Hold Time | 5 | | 5 | | ns | |
| $t_{WSD}$ | Data Setup Time Prior to Write | 25 | | 25 | | ns | *Figure 4* |
| $t_{WHD}$ | Data Hold Time after Write | 5 | | 5 | | ns | |
| $t_{WSA}$ | Address Setup Time Prior to Write[5] | 5 | | 5 | | ns | |
| $t_{WHA}$ | Address Hold Time after Write | 5 | | 5 | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time Prior to Write | 5 | | 5 | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 5 | | 5 | | ns | |

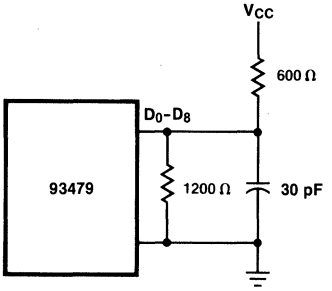
**Military**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 10%, GND = 0 V, $T_A$ = −55°C to +125°C (Notes 1, 3)

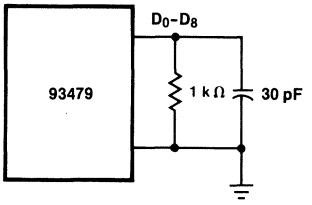
| Symbol | Characteristic | "A" Min | "A" Max | Std Min | Std Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | **Read Timing** | | | | | | |
| $t_{ACS}$ | Chip Select Access Time | | 30 | | 40 | ns | |
| $t_{ZRCS}$ | Chip Select to HIGH Z | | 30 | | 40 | ns | |
| $t_{AOS}$ | Output Enable Access Time | | 30 | | 40 | ns | *Figures 3a, 3b, 3c* |
| $t_{ZROS}$ | Output Enable to HIGH Z | | 30 | | 40 | ns | |
| $t_{AA}$ | Address Access Time | | 45 | | 60 | ns | |
| | **Write Timing** | | | | | | |
| $t_W$ | Write Pulse Width to Guarantee Writing[5] | 40 | | 40 | | ns | |
| $t_{SO}$ | Output Enable Setup Time | 5 | | 5 | | ns | |
| $t_{HO}$ | Data Enable Hold Time | 5 | | 5 | | ns | |
| $t_{WSD}$ | Data Setup Time Prior to Write | 50 | | 50 | | ns | *Figure 4* |
| $t_{WHD}$ | Data Hold Time after Write | 10 | | 10 | | ns | |
| $t_{WSA}$ | Address Setup Time Prior to Write[5] | 10 | | 10 | | ns | |
| $t_{WHA}$ | Address Hold Time after Write | 10 | | 10 | | ns | |
| $t_{WSCS}$ | Chip Select Setup Time Prior to Write | 10 | | 10 | | ns | |
| $t_{WHCS}$ | Chip Select Hold Time after Write | 10 | | 10 | | ns | |

Notes on preceeding page

**Fig. 1 AC Test Load Output Load**




LOAD A




LOAD B

**Fig. 2 Input Levels**

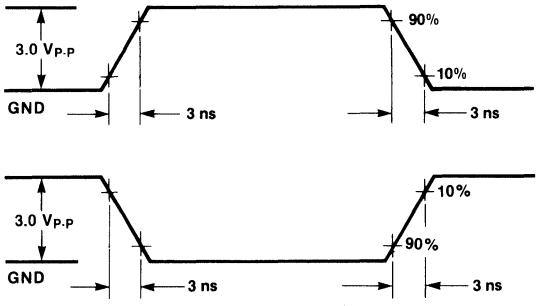
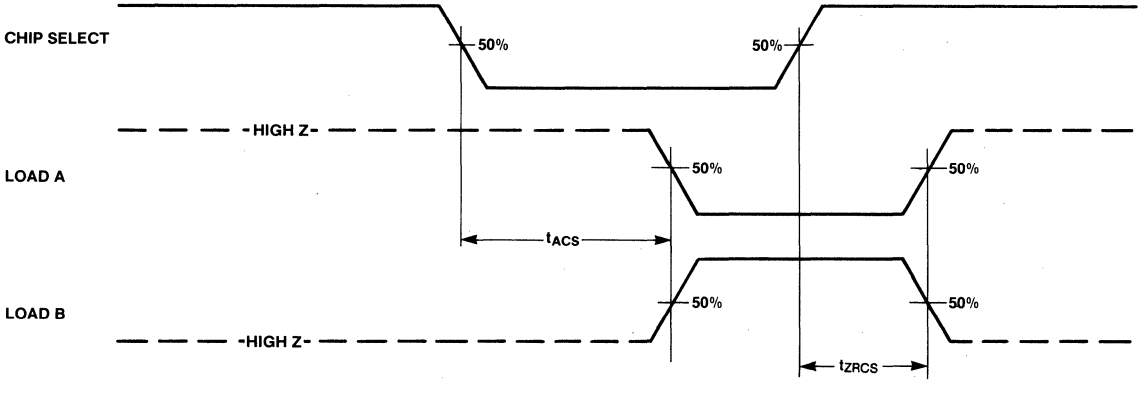
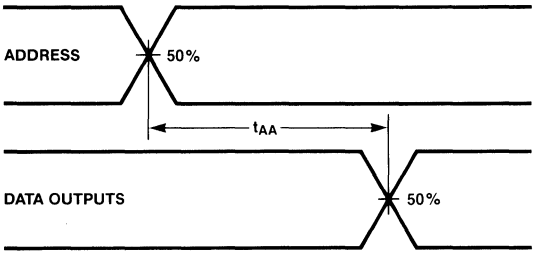



**Fig. 3 Read Mode Timing**

**a Read Mode Propagation Delay from Chip Select to Output**



b Read Mode Propagation Delay from Address to Output






c Read Mode Propagation Delay from Output Enable

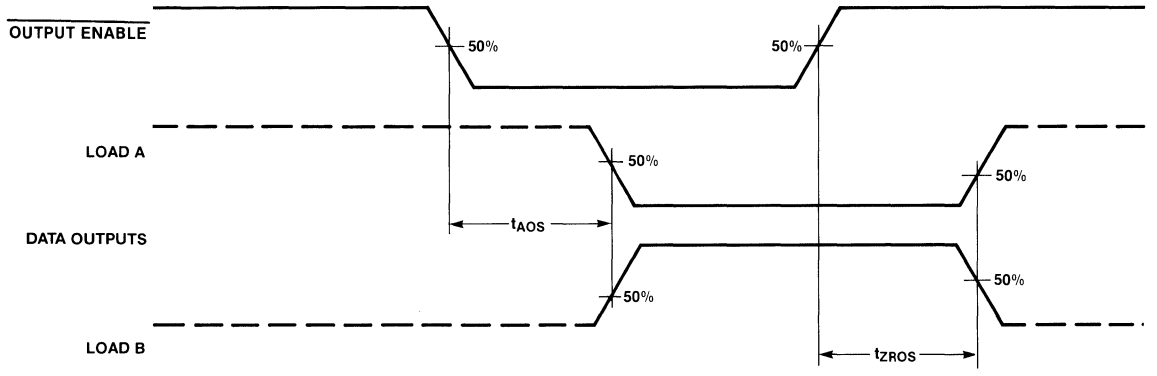
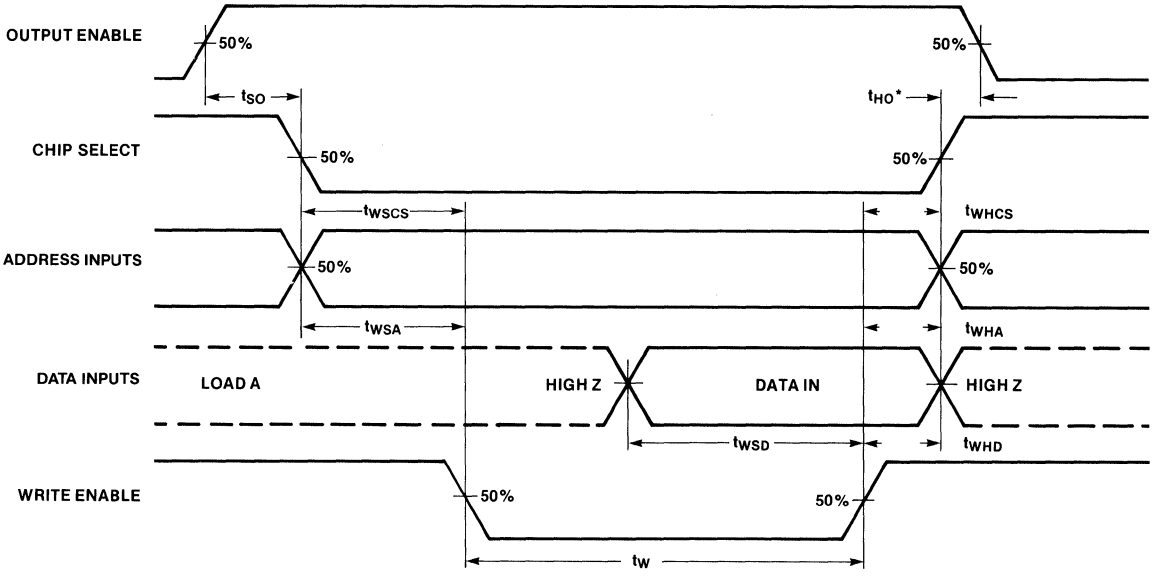


**Fig. 4 Write Mode Timing**




* These timing parameters are only necessary to guarantee High Z state during the entire write cycle

## Ordering Information

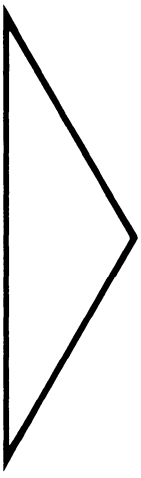
93479 D M

Device Name
Package
Temperature Range
Optional Processing

**Packages and Outlines** (See Section 10)
D = Ceramic DIP

**Temperature Range**
C = 0°C to +75°C
M = −55°C to +125°C

**Optional Processing**
QB = Mil Std 883
Method 5004 and 5005, Level B
QC = Mil Std 883
Method 5004 and 5005, Level C
QR = Commercial Device with
160 Hour Burn In



# F100K DC Family Specifications

DC characteristics for the F100K series family parametric limits listed below are guaranteed for the entire F100K ECL family unless specified on the individual data sheet.

**Absolute Maximum Ratings:** Above which the useful life may be impaired[1]

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Maximum Junction Temperature ($T_J$) | 0°C to +150°C |
| Case Temperature Under Bias ($T_C$) | 0°C to +85°C |
| $V_{EE}$ Pin Potential to Ground Pin | −7.0 V to +0.5 V |
| Input Voltage (dc) | $V_{EE}$ to +0.5 V |
| Output Current (dc Output HIGH) | −50 mA |
| Operating Range[2] | −5.7 V to −4.2 V |

5

**DC Characteristics:** $V_{EE}$ = −4.5 V, $V_{CC}$ = $V_{CCA}$ = GND, $T_C$ = 0°C to +85°C, Note 3

| Symbol | Characteristic | Min | Typ | Max | Unit | Conditions[4] | |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | −1025 | −955 | −880 | mV | $V_{IN}$ = $V_{IH(max)}$ or $V_{IL(min)}$ | Loading with 50 Ω to −2.0 V |
| $V_{OL}$ | Output LOW Voltage | −1810 | −1705 | −1620 | mV | | |
| $V_{OHC}$ | Output HIGH Voltage | −1035 | | | mv | $V_{IN}$ = $V_{IH(min)}$ or $V_{IL(max)}$ | |
| $V_{OLC}$ | Output LOW Voltage | | | −1610 | mV | | |
| $V_{IH}$ | Input HIGH Voltage | −1165 | | −880 | mV | Guaranteed HIGH Signal for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | −1810 | | −1475 | mV | Guaranteed LOW Signal for All Inputs | |
| $I_{IL}$ | Input LOW Current | 0.50 | | | μA | $V_{IN}$ = $V_{IL(min)}$ | |

1. Unless specified otherwise on individual data sheet.
2. Parametric values specified at −4.2 V to −4.8 V.
3. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute, conformance testing performed instantaneously where $T_A$ = $T_J$= $T_C$. Correlated temperatures, typically 25°C and 100°C, and limits may be used to guarantee device operating performance.

**DC Characteristics:** $V_{EE} = -4.2$ V, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$, Note 3

| Symbol | Characteristic | Min | Typ | Max | Unit | Conditions[4] | |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | −1020 | | −870 | mV | $V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$ | Loading with 50 Ω to −2.0 V |
| $V_{OL}$ | Output LOW Voltage | −1810 | | −1605 | mV | | |
| $V_{OHC}$ | Output HIGH Voltage | −1030 | | | mv | $V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$ | |
| $V_{OLC}$ | Output LOW Voltage | | | −1595 | mV | | |
| $V_{IH}$ | Input HIGH Voltage | −1150 | | −880 | mV | Guaranteed HIGH Signal for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | −1810 | | −1475 | mV | Guaranteed LOW Signal for All Inputs | |
| $I_{IL}$ | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL(min)}$ | |

**DC Characteristics:** $V_{EE} = -4.8$ V, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$, Note 3

| Symbol | Characteristic | Min | Typ | Max | Unit | Conditions[4] | |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | −1035 | | −880 | mV | $V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$ | Loading with 50 Ω to −2.0 V |
| $V_{OL}$ | Output LOW Voltage | −1830 | | −1620 | mV | | |
| $V_{OHC}$ | Output HIGH Voltage | −1045 | | | mv | $V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$ | |
| $V_{OLC}$ | Output LOW Voltage | | | −1610 | mV | | |
| $V_{IH}$ | Input HIGH Voltage | −1165 | | −880 | mV | Guaranteed HIGH Signal for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | −1810 | | −1490 | mV | Guaranteed LOW Signal for All Inputs | |
| $I_{IL}$ | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL(min)}$ | |

Notes on preceding page

# F10K DC Family Specifications

DC characteristics for the F10K series memories. Parametric limits listed below are guaranteed for all F10K memories, except where noted on individual data sheets.

**Absolute Maximum Ratings:** Above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| $V_{EE}$ Pin Potential to Ground Pin | −7.0 V to +0.5 V |
| Input Voltage (dc) | $V_{EE}$ to +0.5 V |
| Output Current (dc Output HIGH) | −30 mA to +0.1 mA |

**Guaranteed Operating Ranges**

| Supply Voltage ($V_{CC}$) | | | Ambient Temperature ($T_A$) Note 1 |
|---|---|---|---|
| Min | Typ | Max | |
| −5.46 V | −5.2 V | −4.94 V | 0°C to +75°C |

**DC Characteristics:** $V_{EE}$ = −5.2 V, Output Load = 50 Ω and 30 pF to −2.0 V, $T_A$ = 0°C to 75°C[1]

| Symbol | Characteristic | Min | Typ | Max | Unit | $T_A$ | Conditions[2] | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | −1000<br>−960<br>−900 | | −840<br>−810<br>−720 | mV | 0°C<br>+25°C<br>+75°C | $V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$ | Loading is 50 Ω to −2.0 V |
| $V_{OL}$ | Output LOW Voltage | −1870<br>−1850<br>−1830 | | −1665<br>−1650<br>−1625 | mV | 0°C<br>+25°C<br>+75°C | | |
| $V_{OHC}$ | Output HIGH Voltage | −1020<br>−980<br>−920 | | | mv | 0°C<br>+25°C<br>+75°C | $V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$ | |
| $V_{OLC}$ | Output LOW Voltage | | | −1645<br>−1630<br>−1605 | mV | 0°C<br>+25°C<br>+75°C | | |
| $V_{IH}$ | Input HIGH Voltage | −1145<br>−1105<br>−1045 | | −840<br>−810<br>−720 | mV | 0°C<br>+25°C<br>+75°C | Guaranteed Input Voltage HIGH for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | −1870<br>−1850<br>−1830 | | −1490<br>−1475<br>−1450 | mV | 0°C<br>+25°C<br>+75°C | Guaranteed Input Voltage LOW for All Inputs | |
| $I_{IL}$ | Input LOW Current | 0.5 | | 170 | μA | +25°C | $V_{IN} = V_{IL(min)}$ | |

1. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
2. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute, conformance testing performed instantaneously where $T_A = T_J = T_C$. Correlated temperatures, typically 25°C and 100°C, and limits may be used to guarantee device operating performance.

FAIRCHILD
A Schlumberger Company

# F100416
# 256 x 4-Bit Programmable Read Only Memory

Bipolar Division

F100K ECL Product

## Description

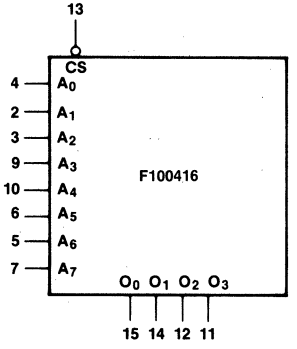
The F100416 is a 1024-bit field Programmable Read Only Memory (PROM), organized 256 words by four bits per word. It is designed for high-speed control, mapping, code conversion, and logic replacement. The device includes full on-chip address decoding, non-inverting Data output lines, and an active-LOW Chip Select line for easy memory expansion. The device is manufactured with all bits in the logic-HIGH state. Programmed bits will furnish LOW levels at corresponding outputs.

- **Address Access Time — 20 ns Max**
- **Chip Select Access Time — 8.0 ns Max**
- **Chip Select Input and Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation — 0.46 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $\overline{CS}$ | Chip Select Input (Active LOW) |
| $A_0$–$A_7$ | Address Inputs |
| $O_0$–$O_3$ | Data Outputs |

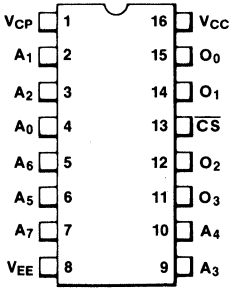
## Logic Symbol




$V_{CP}$ = Pin 1
$V_{CC}$ = Pin 16
$V_{EE}$ = Pin 8

## Connection Diagram

**16-Pin DIP** (Top View)

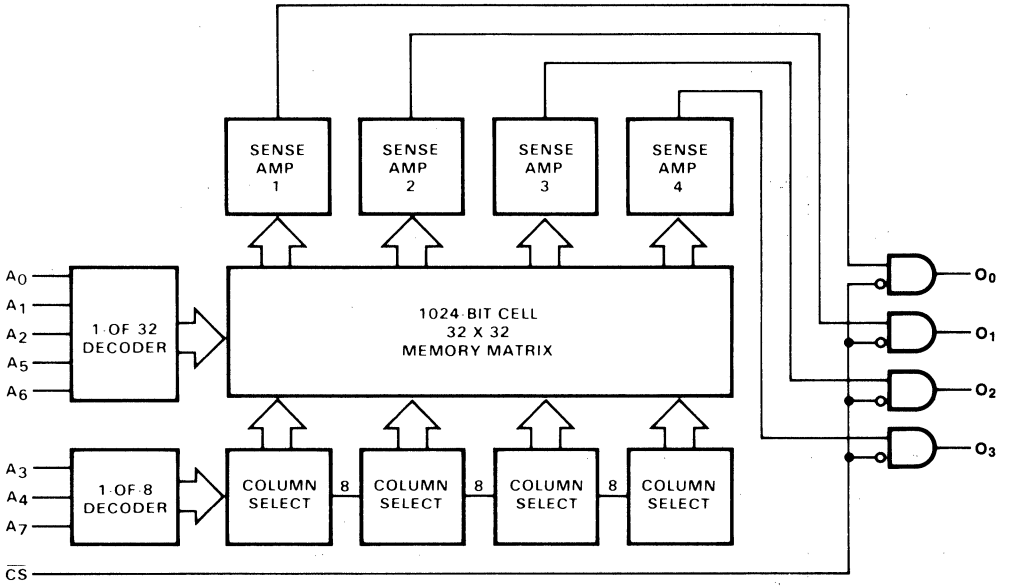



**Notes**

$V_{CP}$ (Pin 1) is connected to the Programmer (+10.5 V) during programming only; otherwise, it should be grounded

The Flatpak version has the same pinout (Connection Diagram) as the Dual In-line Package

**Logic Diagram**




**Functional Description**

The F100416 is a fully decoded bipolar field programmable read only memory organized 256 words by four bits per word. An unterminated emitter-follower output is provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many F100416 devices can be tied together. An external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is off.

One Chip Select ($\overline{CS}$) input is provided for memory array expansion up to 512 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of $\overline{CS}$ from the address without increasing address access time. The device is enabled when $\overline{CS}$ is LOW. When the device is disabled ($\overline{CS}$ = HIGH), all outputs are forced LOW.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the $A_0$ through $A_7$ inputs, the chip is selected and data is valid at the outputs after $t_{AA}$.

In the unprogrammed state the outputs are HIGH. To program LOW levels follow the procedure outlined in the *Programming Specifications* table.

**Programming**

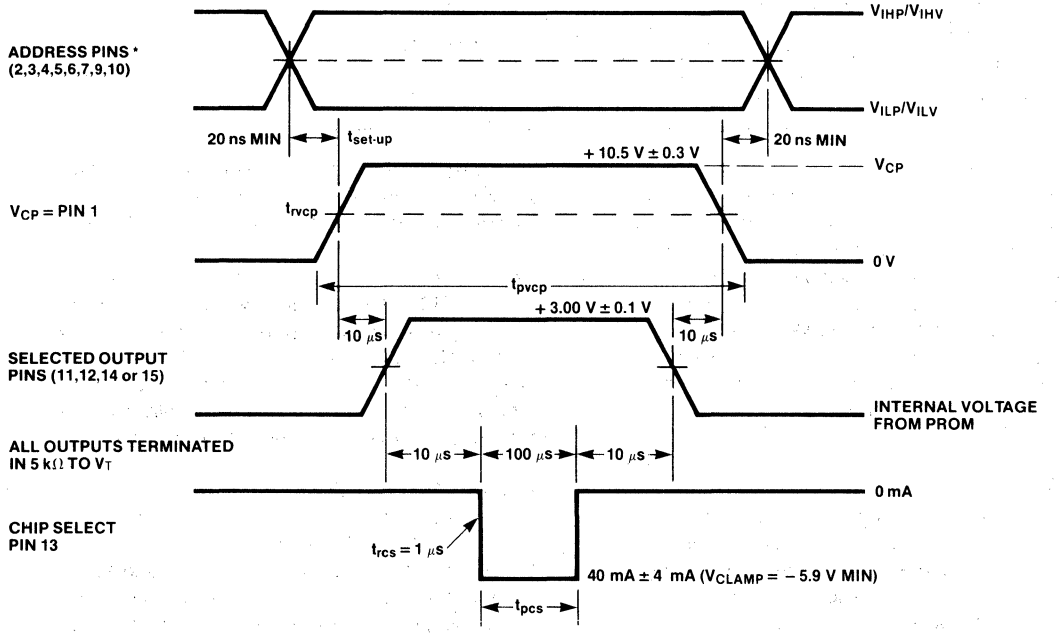
The F100416 is manufactured with all bits in the logic "1" state. Any desired bit (output) can be programmed to a logic "0" state by following the procedure shown below. One may build a programmer to satisfy the specifications or purchase any of the commercially available programmers which meet these specifications.

**Programming Sequence**

1. Apply power to the part: $V_{CC}$ = pin 16 = GND; $V_{EE}$ = pin 8 = −5.2 V ± 5%.
2. Terminate all outputs (pins 11, 12, 14 and 15) with 5 kΩ resistors to $V_{TT}$ = −2.0 V. Note: all input pins, including $\overline{CS}$, have internal 50 kΩ pull-down resistors to $V_{EE}$.
3. Select the word to be programmed by applying the appropriate voltage levels, as shown in the *Programming Specifications* table, to the Address pins (2, 3, 4, 5, 6, 7, 9 and 10).
4. After the address levels are set raise $V_{CP}$ = Pin 1 from 0 V to +10.5 V ±0.3 V.

5. After $V_{CP}$ has reached its HIGH level, select the bit to be programmed by applying a HIGH level of +3.0 V ±0.1 V to the output associated with it, *i.e.*, pins 11, 12, 14 or 15. Only one bit (output) at a time may be selected for programming. Uncommitted outputs are terminated as outlined in 2.
6. After the HIGH level (+3.0 V) has been established at the selected output pin, source a current of −40 mA ± 4 mA out of the Chip Select input (pin 13) to program the selected bit; this applied current pulse which is 100 μs wide and has an approximate rise time of 1 μs is to be furnished by a current sink which clamps at $V_{CLAMP}$ = −5.9 V.
7. To verify a LOW in the bit just programmed follow this sequence:
   (a) Remove current pulse from $\overline{CS}$ pin.
   (b) Remove applied voltage from selected output pin.
   (c) Lower $V_{CP}$ from HIGH level to GND.
   (d) Keep same address but change its levels to normal ECL levels as outlined in the *Programming Specifications* table.
   (e) Enable the chip by applying a LOW level ($V_{IL}$) to $\overline{CS}$ (pin 13), or leave it open.
   (f) Sense the level at the selected output pin; a LOW level indicates successful programming whereas a HIGH level is a fail indication; in the latter case reprogramming of the bit can be attempted up to a maximum of eight times.
8. To program other bits in the memory repeat steps 3 through 7.

**Programming Timing Sequence**




*Input pins $A_1$ and $A_7$ cannot be lower than $V_{IL(min)}$

**Programming Specifications**

| Symbol | Characteristic | Min | Recommended Value | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply | | 0 | | V | |
| $V_{EE}$ | | −5.46 | −5.2 | −4.94 | V | |
| $V_{TT}$ | Termination Voltage | | −2.0 | | V | Applied to all outputs |
| $V_{IH}$ | Chip Select ($V_{CLAMP}$) | −0.1 | 0 | +0.1 | V | Max Current is 40 mA during programming |
| $V_{IL}$ | | −5.9 | −5.2 | | V | |
| $V_{IHP}$ | Address Input Threshold | −0.1 | 0 | +0.1 | V | Programming levels |
| $V_{ILP}$ | | −3.1 | −3.0 | −2.9 | V | |
| $V_{IHV}$ | Address Input Threshold | −0.88 | −0.87 | −0.86 | V | Verify levels |
| $V_{ILV}$ | | −1.76 | −1.75 | −1.74 | V | |
| $V_{CP}$ | Program Setup Pulse | 10.2 | 10.5 | 10.8 | V | |
| $V_{OP}$ | Programming Pulse | 2.9 | 3.0 | 3.1 | V | Applied to output to be programmed |
| $I_{CS}$ | Chip Select Programming Current | 36 | 40 | 44 | mA | At $V_{CLAMP}$ = −5.9 V Min on the Chip Select pin |
| $t_{pcs}$ | Chip Select Programming Pulse | 50 | 100 | 180 | μs | |
| $t_{rcs}$ | Chip Select Programming Pulse Rise Time | 0.5 | 1.0 | 2.0 | μs | |
| $t_{pvcp}$ | $V_{CP}$ Programming Pulse | 90 | 140 | 220 | μs | |
| $t_{rvcp}$ | $V_{CP}$ Programming Rise Time | 0.5 | 1.0 | 2.0 | μs | |
| $t_{setup}$ | Setup Time | 20 | | | ns | Start time of $V_{CP}$ pulse after address is selected |

**DC Characteristics:** $V_{EE}$ = −4.2 V to −4.8 V, $V_{CC}$ = GND, $T_C$ = 0°C to +85°C unless otherwise specified[1]

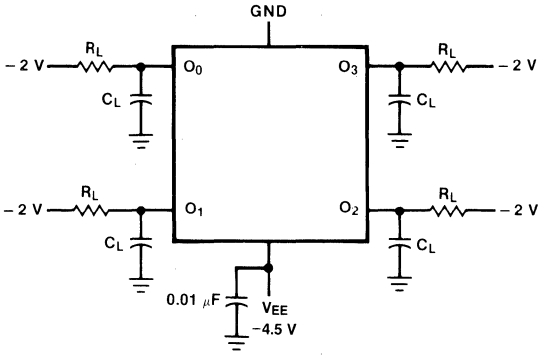
| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input HIGH Current | | | 200 | μA | $V_{IN} = V_{IH(max)}$ |
| $I_{EE}$ | Power Supply Current | −140 | −105 | | mA | Inputs and Outputs Open |

**AC Characteristics:** $V_{EE}$ = −4.2 V to −4.8 V, $V_{CC}$ = GND, Output Load 50 Ω to −2.0 V, $T_C$ = 0°C to +85°C

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $t_{AA}$ | Address Access Time[2] | | 20 | ns | *Figure 3a, 3b* |
| $t_{ACS}$ | Chip Select Access Time | | 8.0 | ns | |

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

**Fig. 1 AC Test Circuit**




**Notes**
All Timing Measurements Referenced to 50% of Input Levels
$C_L$ = 30 pF including Fixture and Stray Capacitance
$R_L$ = 30 Ω to –2.0 V

**Fig. 2 Input Levels**

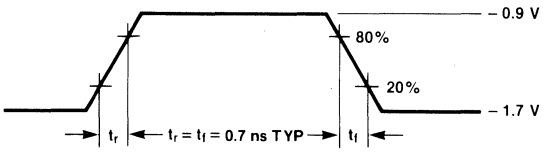
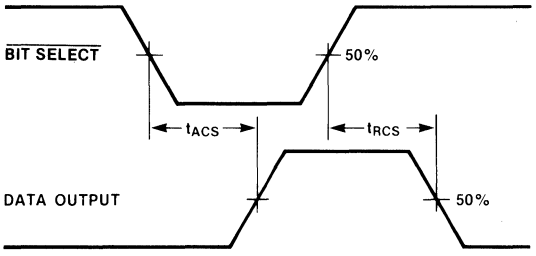
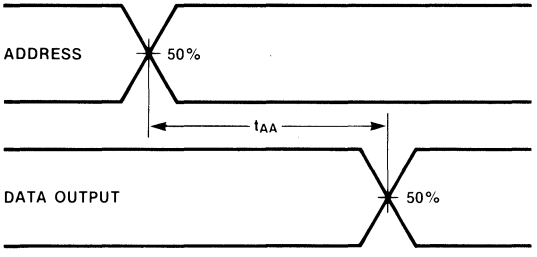



**Fig. 3 Read Mode Timing**

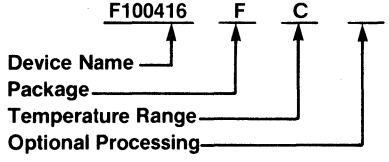
**a Read Mode Propagation Delay from Bit Select**




**b Read Mode Propagation Delay from Address**




## Ordering Information




**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak
P = Plastic DIP

**Temperature Ranges**
C = –30°C to +85°C, Ambient

**Optional Processing**
QR = 160 Hour Burn In

FAIRCHILD
A Schlumberger Company

# F100Z416
# 256 x 4-Bit Programmable Read Only Memory

Bipolar Division

F100K ECL Product

## Description

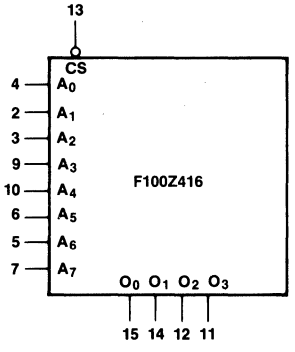
The F100Z416 is a 1024-bit field Programmable Read Only Memory (PROM), organized 256 words by four bits per word. It is designed for high-speed control, mapping, code conversion, and logic replacement. The device includes full on-chip address decoding, non-inverting Data output lines, and an active-LOW Chip Select line for easy memory expansion.

- **Address Access Time — 8.0 ns Typ**
- **Chip Select Input and Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $\overline{CS}$ | Chip Select Input (Active LOW) |
| $A_0$-$A_7$ | Address Inputs |
| $O_0$-$O_3$ | Data Outputs |

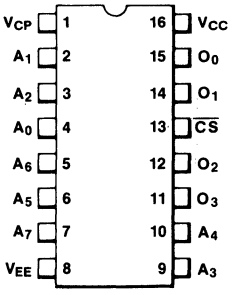
## Logic Symbol




$V_{CP}$ = Pin 1
$V_{CC}$ = Pin 16
$V_{EE}$ = Pin 8

## Connection Diagram

**16-Pin DIP** (Top View)

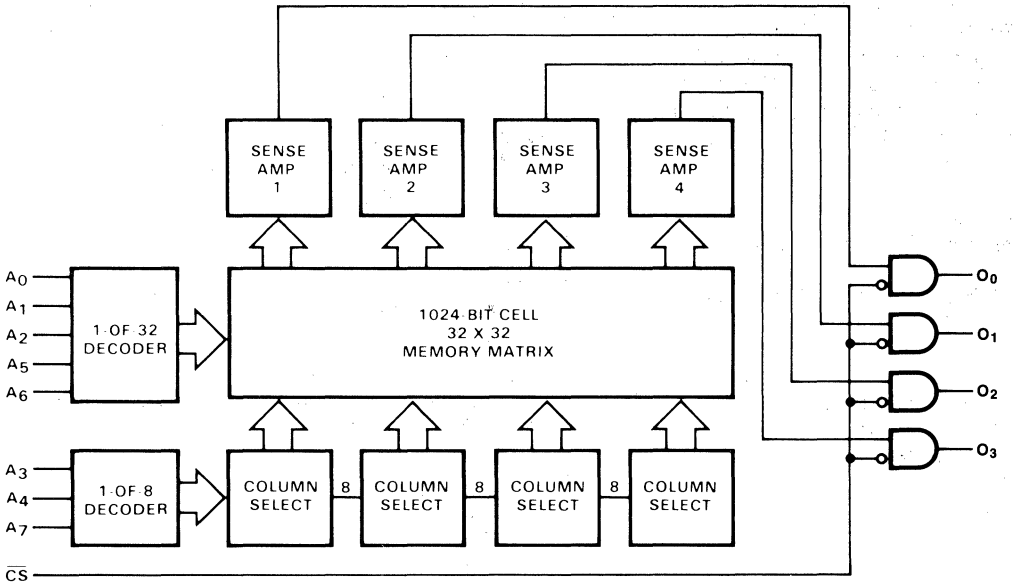



**Note**
The Flatpak version has the same pinout (Connection Diagram) as the Dual In-line Package.



5

**Logic Diagram**




**Functional Description**

The F100Z416 is a fully decoded bipolar field programmable read only memory organized 256 words by four bits per word. An unterminated emitter-follower output is provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many F100Z416 devices can be tied together. An external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is off.

One Chip Select ($\overline{CS}$) input is provided for memory array expansion up to 512 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of $\overline{CS}$ from the address without increasing address access time. The device is enabled when $\overline{CS}$ is LOW. When the device is disabled ($\overline{CS}$ = HIGH), all outputs are forced LOW.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the $A_0$ through $A_7$ inputs, the chip is selected and data is valid at the outputs after $t_{AA}$.

The F100Z416 uses open base transistor vertical (junction) fuse cells. Initially, an unprogrammed cell is in the logic '0' state. Cells can selectively be programmed to a logic '1' state by following a specified procedure which fuses aluminum through the emitter-base junction of the cell transistor.

FAIRCHILD
A Schlumberger Company

# F10416
# 256 x 4-Bit Programmable Read Only Memory

Bipolar Division

F10K ECL Product

## Description

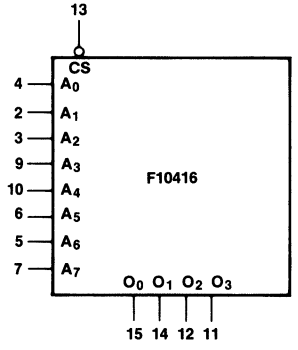
The F10416 is a 1024-bit field Programmable Read Only Memory (PROM), organized 256 words by four bits per word. It is designed for high-speed control, mapping, code conversion, and logic replacement. The device includes full on-chip address decoding, non-inverting Data output lines, and an active-LOW Chip Select line for easy memory expansion. The device is manufactured with all bits in the logic-HIGH state. Programmed bits will furnish LOW levels at corresponding outputs.

- **Address Access Time — 20 ns Max**
- **Chip Select Access Time — 8.0 ns Max**
- **Chip Select Input and Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation — 0.56 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $\overline{CS}$ | Chip Select Input (Active LOW) |
| $A_0$-$A_7$ | Address Inputs |
| $O_0$-$O_3$ | Data Outputs |

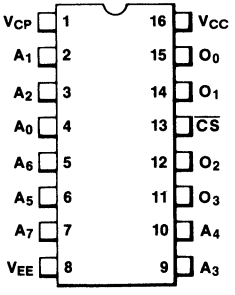
## Logic Symbol




$V_{CP}$ = Pin 1
$V_{CC}$ = Pin 16
$V_{EE}$ = Pin 8

## Connection Diagram

**16-Pin DIP** (Top View)



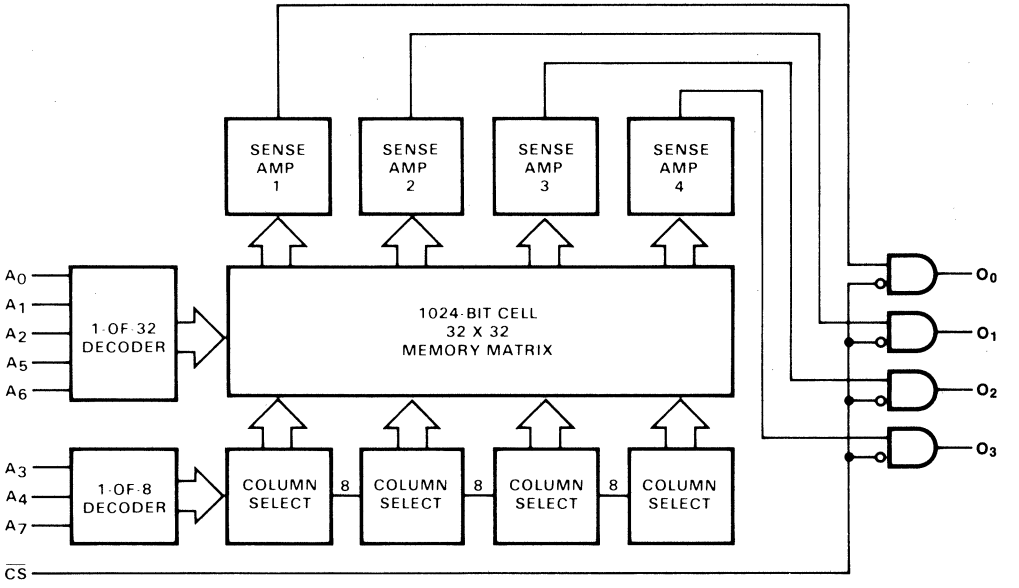

**Notes**

$V_{CP}$ (Pin 1) is connected to the Programmer (+10.5 V) during programming only; otherwise, it should be grounded

The Flatpak version has the same pinout (Connection Diagram) as the Dual In-line Package

5

**Logic Diagram**




**Functional Description**

The F10416 is a fully decoded bipolar field programmable read only memory organized 256 words by four bits per word. An unterminated emitter-follower output is provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many F10416 devices can be tied together. An external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is off.

One Chip Select ($\overline{CS}$) input is provided for memory array expansion up to 512 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of $\overline{CS}$ from the address without increasing address access time. The device is enabled when $\overline{CS}$ is LOW. When the device is disabled ($\overline{CS}$ = HIGH), all outputs are forced LOW.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the $A_0$ through $A_7$ inputs, the chip is selected and data is valid at the outputs after $t_{AA}$.

In the unprogrammed state the outputs are HIGH. To program LOW levels follow the procedure outlined in the *Programming Specifications* table.

**Programming**

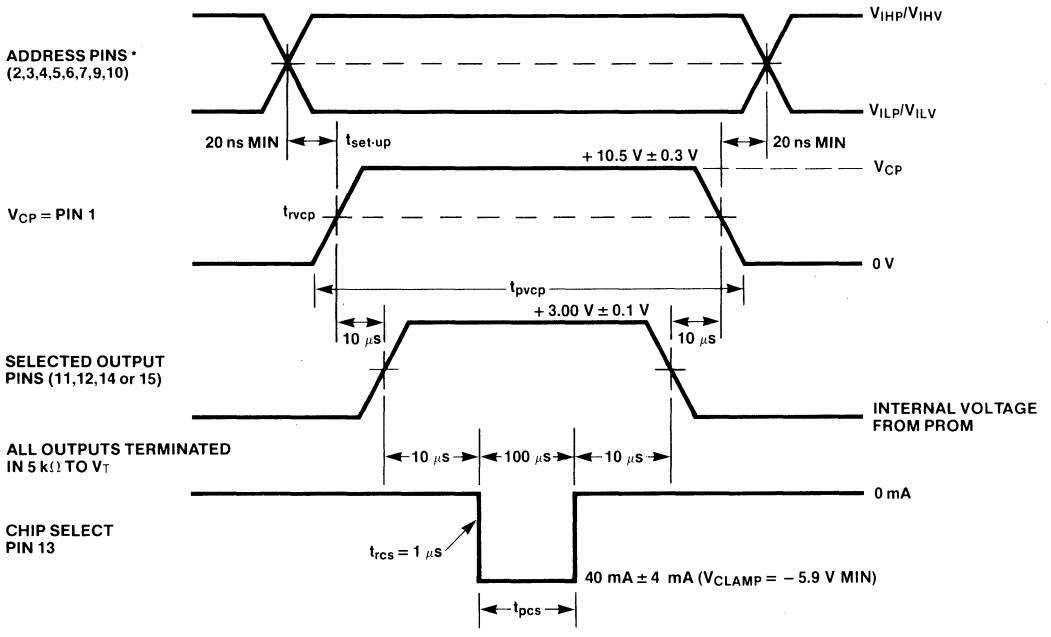
The F10416 is manufactured with all bits in the logic "1" state. Any desired bit (output) can be programmed to a logic "0" state by following the procedure shown below. One may build a programmer to satisfy the specifications or purchase any of the commercially available programmers which meet these specifications.

**Programming Sequence**

1. Apply power to the part: $V_{CC}$ = pin 16 = GND; $V_{EE}$ = pin 8 = −5.2 V ± 5%.
2. Terminate all outputs (pins 11, 12, 14 and 15) with 5 kΩ resistors to $V_{TT}$ = −2.0 V. Note: all input pins, including $\overline{CS}$, have internal 50 kΩ pull-down resistors to $V_{EE}$.
3. Select the word to be programmed by applying the appropriate voltage levels, as shown in the *Programming Specifications* table, to the Address pins (2, 3, 4, 5, 6, 7, 9 and 10).
4. After the address levels are set raise $V_{CP}$ = Pin 1 from 0 V to +10.5 V ±0.3 V.

5. After $V_{CP}$ has reached its HIGH level, select the bit to be programmed by applying a HIGH level of +3.0 V ±0.1 V to the output associated with it, *i.e.*, pins 11, 12, 14 or 15. Only one bit (output) at a time may be selected for programming. Uncommitted outputs are terminated as outlined in 2.
6. After the HIGH level (+3.0 V) has been established at the selected output pin, source a current of −40 mA ± 4 mA out of the Chip Select input (pin 13) to program the selected bit; this applied current pulse which is 100 μs wide and has an approximate rise time of 1 μs is to be furnished by a current sink which clamps at $V_{CLAMP} = -5.9$ V.
7. To verify a LOW in the bit just programmed follow this sequence:
   (a) Remove current pulse from $\overline{CS}$ pin.
   (b) Remove applied voltage from selected output pin.
   (c) Lower $V_{CP}$ from HIGH level to GND.
   (d) Keep same address but change its levels to normal ECL levels as outlined in the *Programming Specifications* table.
   (e) Enable the chip by applying a LOW level ($V_{IL}$) to $\overline{CS}$ (pin 13), or leave it open.
   (f) Sense the level at the selected output pin; a LOW level indicates successful programming whereas a HIGH level is a fail indication; in the latter case reprogramming of the bit can be attempted up to a maximum of eight times.
8. To program other bits in the memory repeat steps 3 through 7.

**Programming Timing Sequence**




*Input pins $A_1$ and $A_7$ cannot be lower than $V_{IL(min)}$

**Programming Specifications**

| Symbol | Characteristic | Min | Recommended Value | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply | | 0 | | V | |
| $V_{EE}$ | | −5.46 | −5.2 | −4.94 | V | |
| $V_{TT}$ | Termination Voltage | | −2.0 | | V | Applied to all outputs |
| $V_{IH}$ | Chip Select ($V_{CLAMP}$) | −0.1 | 0 | +0.1 | V | Max Current is 40 mA during programming |
| $V_{IL}$ | | −5.9 | −5.2 | | V | |
| $V_{IHP}$ | Address Input Threshold | −0.1 | 0 | +0.1 | V | Programming levels |
| $V_{ILP}$ | | −3.1 | −3.0 | −2.9 | V | |
| $V_{IHV}$ | Address Input Threshold | −0.88 | −0.87 | −0.86 | V | Verify levels |
| $V_{ILV}$ | | −1.76 | −1.75 | −1.74 | V | |
| $V_{CP}$ | Program Setup Pulse | 10.2 | 10.5 | 10.8 | V | |
| $V_{OP}$ | Programming Pulse | 2.9 | 3.0 | 3.1 | V | Applied to output to be programmed |
| $I_{CS}$ | Chip Select Programming Current | 36 | 40 | 44 | mA | At $V_{CLAMP}$ = −5.9 V Min on the Chip Select pin |
| $t_{pcs}$ | Chip Select Programming Pulse | 50 | 100 | 180 | μs | |
| $t_{rcs}$ | Chip Select Programming Pulse Rise Time | 0.5 | 1.0 | 2.0 | μs | |
| $t_{pvcp}$ | $V_{CP}$ Programming Pulse | 90 | 140 | 220 | μs | |
| $t_{rvcp}$ | $V_{CP}$ Programming Rise Time | 0.5 | 1.0 | 2.0 | μs | |
| $t_{setup}$ | Setup Time | 20 | | | ns | Start time of $V_{CP}$ pulse after address is selected |

**Guaranteed Operating Range**

| | Supply Voltage ($V_{EE}$) | | | Ambient Temperature |
|---|---|---|---|---|
| | Min | Typ | Max | $T_A$ |
| Commercial | −5.46 V | −5.2 V | −4.94 V | −30°C to +85°C |

**DC Characteristics:** $V_{EE}$ = −5.2 V, $V_{CC}$ = GND, $T_A$ = −30°C to +85°C unless otherwise specified[1]

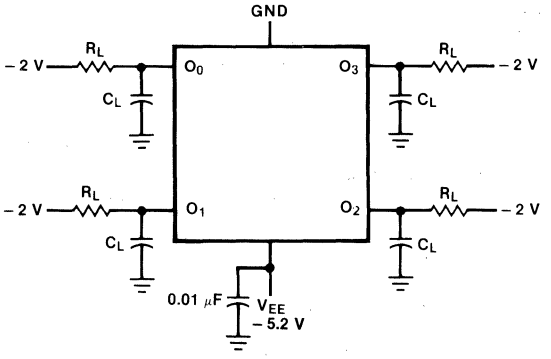
| Symbol | Characteristic | Min | Typ | Max | Unit | $T_A$ | Condition | |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | −1060<br>−960<br>−890 | | −890<br>−810<br>−700 | mV | −30°C<br>+25°C<br>+85°C | $V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$ | Loading is 50 Ω to −2.0 V |
| $V_{OL}$ | Output LOW Voltage | −1890<br>−1850<br>−1825 | | −1675<br>−1650<br>−1615 | mV | −30°C<br>+25°C<br>+85°C | | |
| $V_{OHC}$ | Output HIGH Voltage | −1080<br>−980<br>−910 | | | mv | −30°C<br>+25°C<br>+85°C | $V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$ | |
| $V_{OLC}$ | Output LOW Voltage | | | −1655<br>−1630<br>−1595 | mV | −30°C<br>+25°C<br>+85°C | | |
| $V_{IH}$ | Input HIGH Voltage | −1205<br>−1105<br>−1035 | | 890<br>810<br>700 | mV | −30°C<br>+25°C<br>+85°C | Guaranteed HIGH signal for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | −1890<br>−1850<br>−1825 | | −1500<br>−1475<br>−1440 | mV | −30°C<br>+25°C<br>+85°C | Guaranteed LOW signal for All Inputs | |
| $I_{IH}$ | Input HIGH Current | | | 200 | μA | −30°C to +85°C | $V_{IN} = V_{IH(max)}$ | |
| $I_{IL}$ | Input LOW Current, $\overline{CS}$ | 0.5 | | 150 | μA | +25°C | $V_{IN} = V_{IL(min)}$ | |
| $I_{EE}$ | Power Supply Current | −140 | −110 | | mA | +25°C | All Inputs and Outputs Open | |

**AC Characteristics:** $V_{EE}$ = −4.2 V to −4.8 V, $V_{CC}$ = GND, Output Load 50 Ω to −2.0 V, $T_C$ = 0°C to +85°C

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $t_{AA}$ | Address Access Time[2] | | 20 | ns | *Figure 3a, 3b* |
| $t_{ACS}$ | Chip Select Access Time | | 8.0 | ns | |

1. See Family Characteristics for other dc specifications.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

**Fig. 1 AC Test Circuit**




**Notes**
All Timing Measurements Referenced to 50% of Input Levels
$C_L$ = 30 pF including Fixture and Stray Capacitance
$R_L$ = 50 Ω to –2.0 V

**Fig. 2 Input Levels**

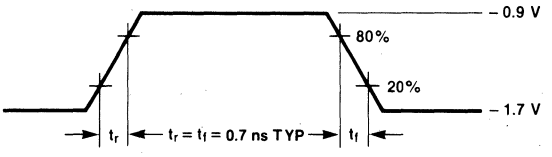
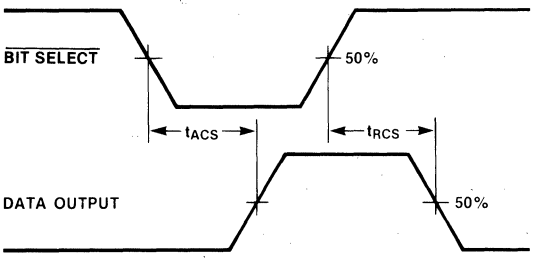
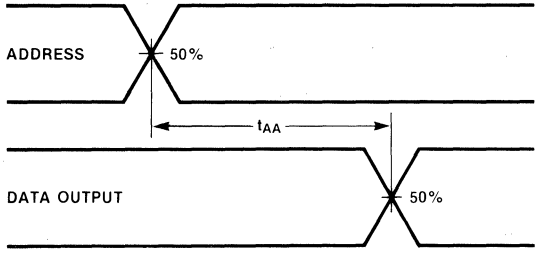



**Fig. 3 Read Mode Timing**

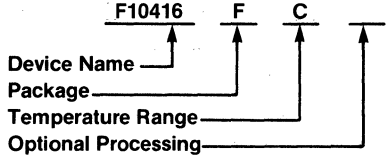
**a Read Mode Propagation Delay from Bit Select**




**b Read Mode Propagation Delay from Address**




## Ordering Information




**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak
P = Plastic DIP

**Temperature Ranges**
C = –30°C to +85°C, Ambient

**Optional Processing**
QR = 160 Hour Burn In

FAIRCHILD
A Schlumberger Company

# F10Z416
# 256 x 4-Bit Programmable Read Only Memory

Bipolar Division

F10K ECL Product

## Description

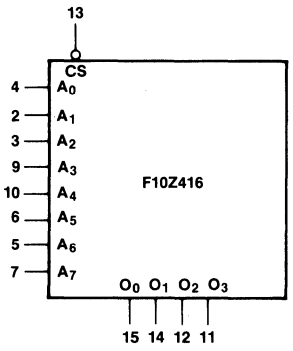
The F10Z416 is a 1024-bit field Programmable Read Only Memory (PROM), organized 256 words by four bits per word. It is designed for high-speed control, mapping, code conversion, and logic replacement. The device includes full on-chip address decoding, non-inverting Data output lines, and an active-LOW Chip Select line for easy memory expansion.

- **Address Access Time — 8.0 ns Typ**
- **Chip Select Input and Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation Decreases with Increasing Temperature**

## Pin Names

| | |
|---|---|
| $\overline{CS}$ | Chip Select Input (Active LOW) |
| $A_0$-$A_7$ | Address Inputs |
| $O_0$-$O_3$ | Data Outputs |

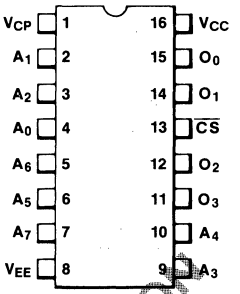
## Logic Symbol




$V_{CP}$ = Pin 1
$V_{CC}$ = Pin 16
$V_{EE}$ = Pin 8

## Connection Diagram

**16-Pin DIP** (Top View)

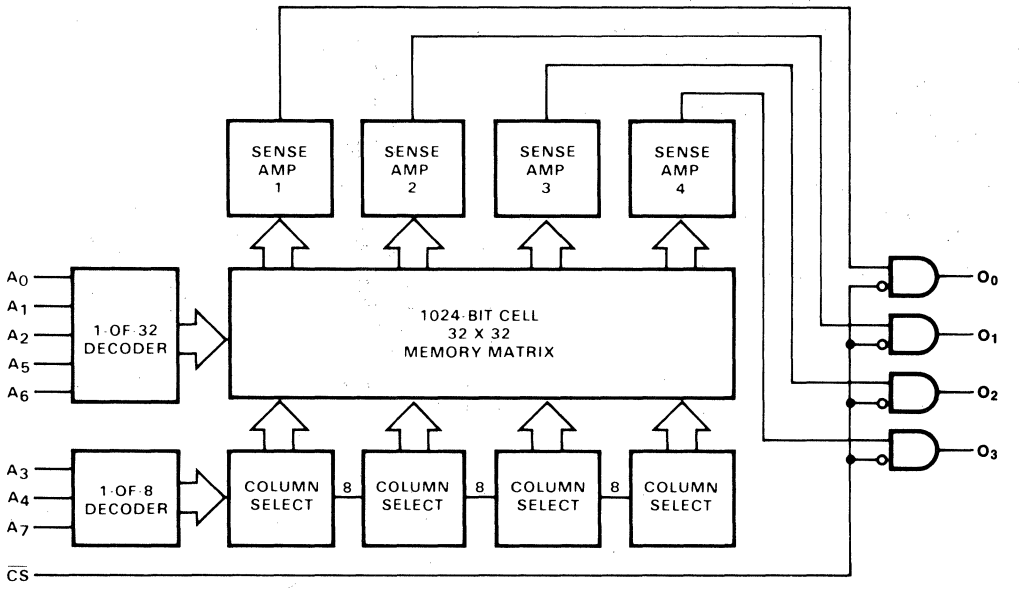



**Note**
The Flatpak version has the same pinout (Connection Diagram) as the Dual In-line Package.



5

## Logic Diagram



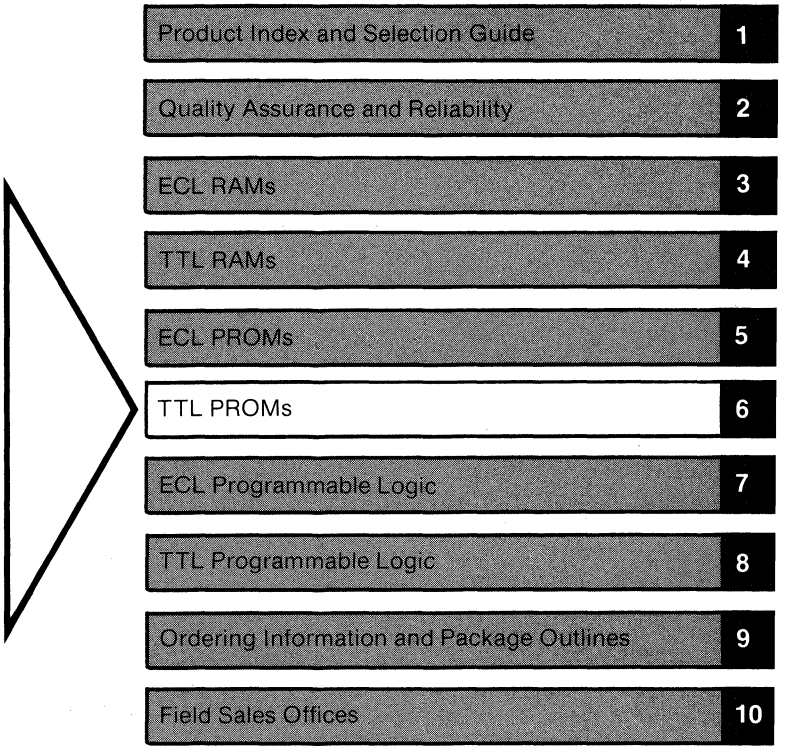

### Functional Description

The F10Z416 is a fully decoded bipolar field programmable read only memory organized 256 words by four bits per word. An unterminated emitter-follower output is provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many F10Z416 devices can be tied together. An external 50 Ω pull-down resistor to −2 V or an equivalent network must be used to provide a LOW at the output when it is off.

One Chip Select ($\overline{CS}$) input is provided for memory array expansion up to 512 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of $\overline{CS}$ from the address without increasing address access time. The device is enabled when $\overline{CS}$ is LOW. When the device is disabled ($\overline{CS}$ = HIGH), all outputs are forced LOW.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the $A_0$ through $A_7$ inputs, the chip is selected and data is valid at the outputs after $t_{AA}$.

The F10Z416 uses open base transistor vertical (junction) fuse cells. Initially, an unprogrammed cell is in the logic '0' state. Cells can selectively be programmed to a logic '1' state by following a specified procedure which fuses aluminum through the emitter-base junction of the cell transistor.


Product Index and Selection Guide 1
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**Absolute Maximum Ratings:** Above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| $V_{CC}$ Pin Potential to Ground Pin | −0.5 V to +7.0 V |
| *Input Voltage (dc) | −0.5 V to +5.5 V |
| *Input Current (dc) | −12 mA to +5.0 mA |
| **Voltage Applied to Outputs (output HIGH) | −0.5 V to +5.50 V |
| Output Current (dc) | +20 mA |

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required

**Guaranteed Operating Ranges**

| | Supply Voltage ($V_{CC}$) | | | Ambient Temperature ($T_A$) Note 1 |
|---|---|---|---|---|
| | Min | Typ | Max | |
| Commercial | 4.75 V | 5.0 V | 5.25 V | 0°C to +75°C |
| Military | 4.50 V | 5.0 V | 5.50 V | −55°C to +125°C |

1. Operating specification with adequate time for temperature stabilization and transverse air flow exceeding 400 linear feet per minute, conformance testing performed instantaneously where $T_A = T_J = T_C$. Correlated temperatures, typically 25°C and 100°C, and limits may be used to guarantee device operating performance.
2. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

| Symbol | Characteristic | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Pin Capacitance | 4.0 | 5.0 | pF | Measured with a Pulse |
| $C_{OUT}$ | Output Pin Capacitance | 7.0 | 8.0 | pF | Technique |

DC specifications listed with each device

FAIRCHILD
A Schlumberger Company

# 93Z450/93Z451
# 1024 x 8-Bit Programmable Read Only Memory

Bipolar Division

Isoplanar-Z Vertical Fuse TTL Memory

## Description

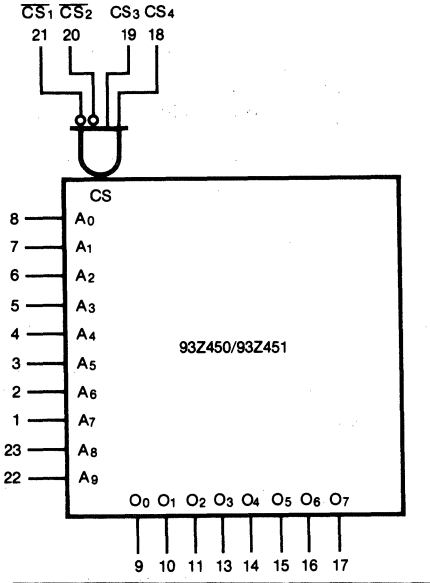
The 93Z450 and 93Z451 are fully decoded 8,192-bit Programmable Read Only Memories (PROMs), organized 1024 words by eight bits per word. The two devices are identical except the 93Z450 has open collector outputs while the 93Z451 has three state outputs. Both devices are available in two speed versions, standard speed and 'A' grade.

- **Commercial Address Access Time**
  **93Z450/93Z451 — 40 ns Max**
  **93Z450A/93Z451A — 35 ns Max**
- **Military Address Access Time**
  **93Z450/93Z451 — 55 ns Max**
  **93Z450A/93Z451A — 45 ns Max**
- **Highly Reliable Vertical Fuses Ensure High Programming Yields**
- **Available with Open Collector (93Z450) or Three State (93Z451) Outputs**
- **Low Current PNP Inputs**

## Pin Names

| | |
|---|---|
| $A_0$–$A_9$ | Address Inputs |
| $\overline{CS_1}$, $\overline{CS_2}$ | Chip Select Inputs (Active LOW) |
| $CS_3$, $CS_4$ | Chip Select Inputs (Active HIGH) |
| $O_0$–$O_7$ | Data Outputs |

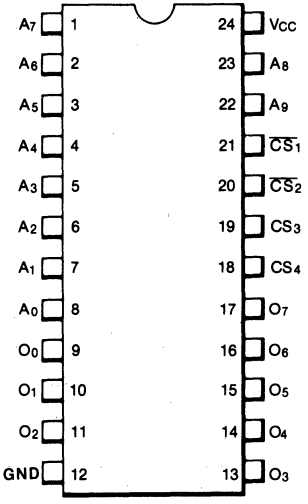
## Logic Symbol




$V_{CC}$ = Pin 24
GND = Pin 12

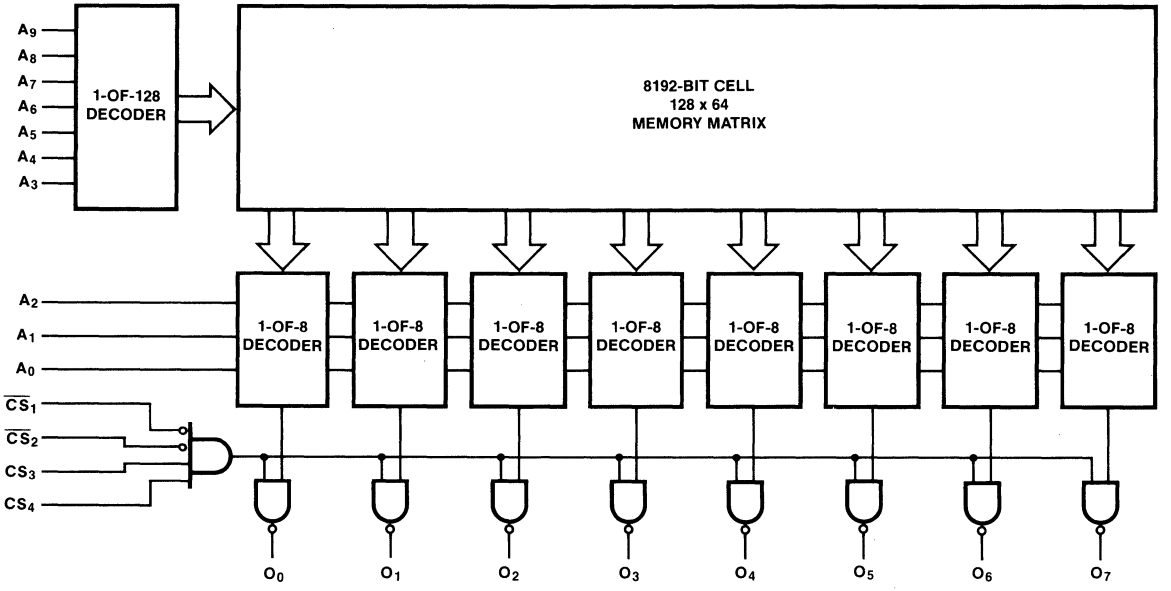
## Connection Diagrams

**24-pin DIP** (Top View)




**Note:**
The 24-pin Flatpak has the same pinout (Connection Diagram) as the 24-pin DIP.

## Logic Diagram




### Functional Description

The 93Z450 and 93Z451 are TTL bipolar field Programmable Read Only Memories (PROMs) organized 1024 words by eight bits per word. Open-collector outputs are provided on the 93Z450 for use in wired-OR applications. The 93Z451 has 3-state outputs which provide active pull ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.

Four Chip Select inputs are provided for logic flexibility and for memory array expansion of up to 128K without the need for external decoding. The fast Chip Select access time permits direct address decoding without increasing overall memory access times. Both devices are enabled only when $\overline{CS_1}$ and $\overline{CS_2}$ are LOW and $CS_3$ and $CS_4$ are HIGH.

The devices contain an internal test row and test column which are accessed and programmed during both wafer sort and final test. These test fuses are used to assure high programmability and to guarantee AC performance and DC parameters.

The 93Z450 and 93Z451 use open base vertical transistor (junction) fuse cells. Initially an unprogrammed cell is in the logic '0' state. Cells can be programmed to a logic '1' state by following the specified programming procedure which fuses aluminum through the emitter base junction of the cell transistor.

The read function is identical to that of a conventional Read Only Memory (ROM). A binary address is applied to the address pins $A_0$ through $A_9$ and the chip is selected. Data is then available at the outputs after $t_{AA}$.

### Programming

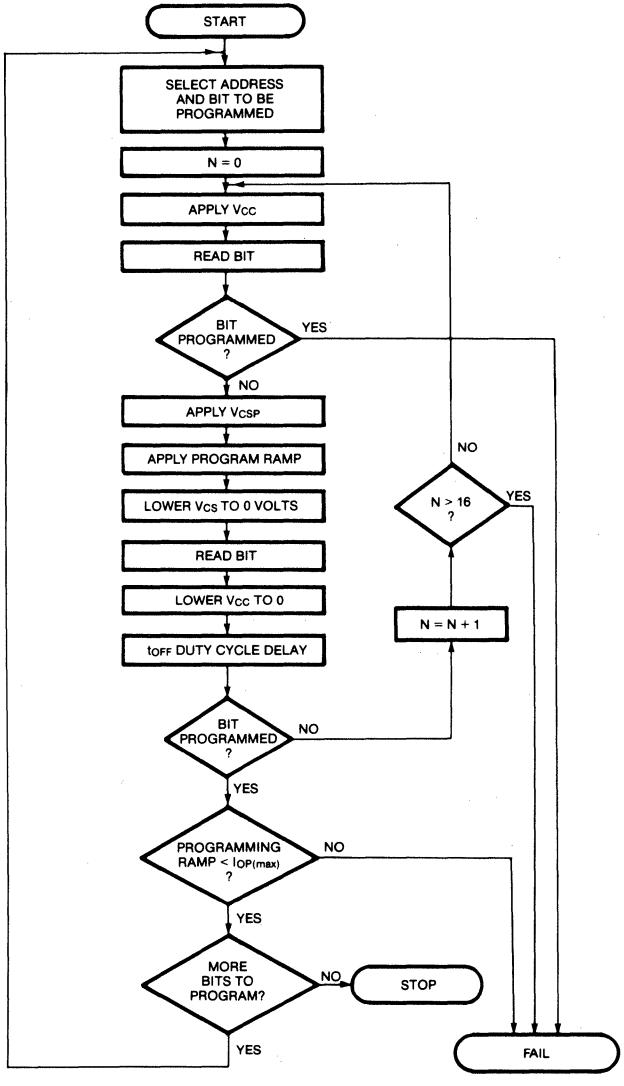
The 93Z450 and 93Z451 are manufactured with all bits in the logic "0" state. Any desired bit (output) can be programmed to a logic "1" state by following the Isoplanar-Z Generic Programming Specifications found at the back of this section.

### Programming Sequence

The 93Z450 and 93Z451 are both programmed using the following method:

1. Address the word to be programmed by applying the appropriate voltages to address pins $A_0$ through $A_9$. Select the PROM by applying a LOW to $\overline{CS_1}$ and $\overline{CS_2}$ and a HIGH to $CS_3$ and $CS_4$.
2. Apply the proper power for a High $V_{CC}$ read. $V_{CC}$ = 6.5 V, GND = 0 V.
3. Read the output to be programmed and verify it is in the unprogrammed logic '0' state.
4. Enable the chip for programming by application of the Chip Select Programming Voltage ($V_{CSP}$ = 20.0 V) to $\overline{CS_2}$. $\overline{CS_1}$ should remain LOW and $CS_3$ and $CS_4$ HIGH.
5. a. To program the bit apply $I_{OP}$, the programming current ramp to the output. NOTE: Only one output may be programmed at a time. The other outputs must be left open.
   b. During the rise of the current ramp, a drop in voltage ($V_{PS}$) at the output may be sensed. This indicates that the current needed to program the junction has been reached and the bit has programmed.
   c. Upon detection of the voltage drop ($V_{PS}$), the current ramp should be held at a constant current for a time ($t_{hAP}$) and then shut off.
6. Once the current ramp has been shut off, lower $V_{CSP}$ to 0 V and read the output.
7. Lower $V_{CC}$ to 0 V. The power supply duty cycle must be less than or equal to 50%.
8. If the read performed in step 6 indicates that the bit has not programmed then go to step 1 and repeat the programming sequence (up to a maximum of 16 attempts total.)
9. If the read performed in step 6 indicates that the bit has programmed then one of the two following conditions exist:
   a. If the required programming current was less than $I_{OP(max)}$ then go to step 10.
   b. If the required programming current was equal to $I_{OP(max)}$ then the device is considered a failure and no future attempts at programming should be made.
10. Repeat the above procedure from step 1 until all the desired bits in the memory have been programmed.

### Programming Flow Chart



**DC Characteristics:** Over guaranteed operating ranges unless otherwise noted

| Symbol | Characteristic | Min | Typ(1) | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | Guaranteed Input LOW Voltage for All Inputs |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs |
| $V_{IC}$ | Input Clamp Diode Voltage | | | −1.2 | V | $V_{CC}$ = Min, $I_{IN}$ = −18 mA |
| $V_{OL}$ | Output LOW Voltage | | 0.30 | 0.45 | V | $V_{CC}$ = Min, $I_{OL}$ = 16 mA |
| $V_{OH}$ | Output HIGH Voltage (three state only) | 2.4 | | | V | $V_{CC}$ = Min, $I_{OH}$ = −2.0 mA Address Any '1' |
| $I_{IL}$ | Input LOW Current | | −10 | −100 | μA | $V_{CC}$ = Max, $V_{IL}$ = 0.45 V to $V_{CC}$ |
| $I_{IH}$ | Input HIGH Current | −40 | | 40 | μA | $V_{CC}$ = Max, $V_{IH}$ = 2.4 V to $V_{CC}$ |
| $I_{OHZ}$ | Output Leakage Current for High Impedance State (three state only) | | | 40<br>−40 | μA<br>μA | $V_{OH}$ = 2.4 V<br>$V_{OL}$ = 0.4 V |
| $I_{CEX}$ | Output Leakage Current (open collector only) | | | 40 | μA | $V_{CEX}$ = $V_{CC}$, Chip Deselected |
| $I_{OS}$ | Output Short-Circuit Current (three state only) | −20 | −45 | −90 | mA | $V_{CC}$ = Max, $V_O$ = 0 V, Note 2 Address Any '1' |
| $I_{CC}$ | Power Supply Current | | 110 | 135 | mA | $V_{CC}$ = Max, Inputs and Outputs Open |

**Commercial**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 5%, GND = 0 V, $T_A$ = 0°C to +75°C

| Symbol | Characteristic | 'A' | Std | Unit | Condition |
|---|---|---|---|---|---|
| $t_{AA}$ | Address to Output Access Time | 35 | 40 | ns | See AC Output Load |
| $t_{ACS}$ | Chip Select to Output Access Time | 25 | 30 | ns | See AC Output Load |

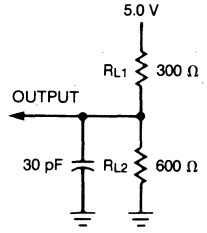
**Military**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 10%, GND = 0 V, $T_A$ = 55°C to +125°C

| Symbol | Characteristic | 'A' | Std | Unit | Condition |
|---|---|---|---|---|---|
| $t_{AA}$ | Address to Output Access Time | 45 | 55 | ns | See AC Output Load |
| $t_{ACS}$ | Chip Select to Output Access Time | 30 | 35 | ns | See AC Output Load |

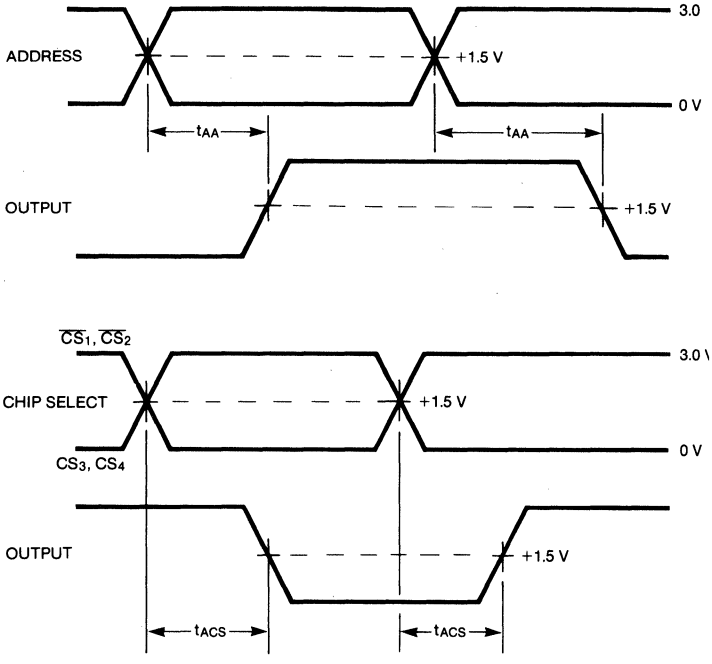
1. Typical values are at $V_{CC}$ = 5.0 V, $T_A$ = +25°C and maximum loading.
2. Not more than one output to be shorted at a time. Duration of the short circuit should not exceed one second.

**Fig. 1 AC Test Output Load**

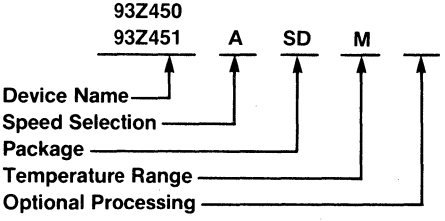



**Test Conditions**
Input pulse: 0 V to 3.0 V
Input pulse rise and fall times: 5 ns between 1 V and 2 V
Measurements made at 1.5 V level

**Fig. 2 AC Waveforms**




## Ordering Information




**Speed Selection**
Blank = Standard Speed
A = 'A' Grade

**Packages and Outlines** (See Section 10)
D = 24-pin Ceramic DIP
P = 24-pin Plastic DIP (Commercial only)
SD = 24-pin Slim Ceramic DIP
F = 24-pin Flatpak
L = 28-pin Square Leadless Chip Carrier

**Temperature Range**
C = 0°C to +75°C
M = −55°C to +125°C

**Optional Processing**
QB = Mil Std 883
Method 5004 and 5005, Level B
QC = Mil Std 883
Method 5004 and 5005, Level C
QR = Commercial Device with
160 Hour Burn In

FAIRCHILD
A Schlumberger Company

# 93453
# 1024 x 4-Bit Programmable Read Only Memory

Bipolar Division

TTL NiChrome Fuse Memory

## Description

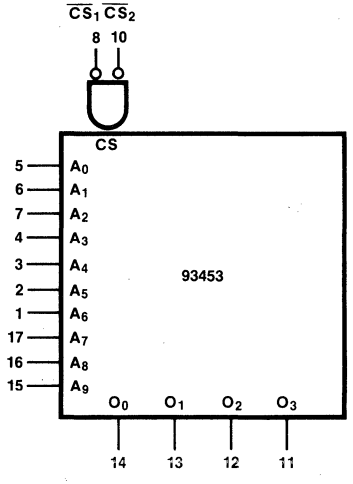
The 93453 is a 4096-bit field Programmable Read Only Memory (PROM) organized 1024 words by four bits per word. The device features full on-chip address decoding, two active LOW Chip Select lines and three state outputs.

- **Commercial Address Access Time — 40 ns Max**
- **Military Address Access Time — 55 ns Max**
- **Fully TTL Compatible**
- **Proven Nichrome Fuse Technology**
- **Features Three State Outputs**
- **Power Dissipation — 135μW/Bit Typ**
- **JEDEC Standard Pinout**

## Pin Names

| | |
|---|---|
| $A_0$-$A_9$ | Address Inputs |
| $\overline{CS}_1$, $\overline{CS}_2$ | Chip Select Inputs (Active LOW) |
| $O_0$-$O_3$ | Data Outputs |

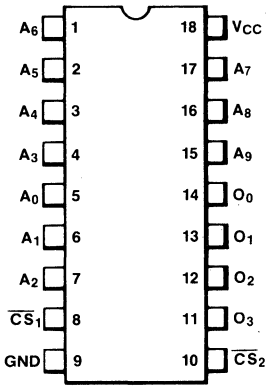
## Logic Symbol




$V_{CC}$ = Pin 18
GND = Pin 9

## Connection Diagram

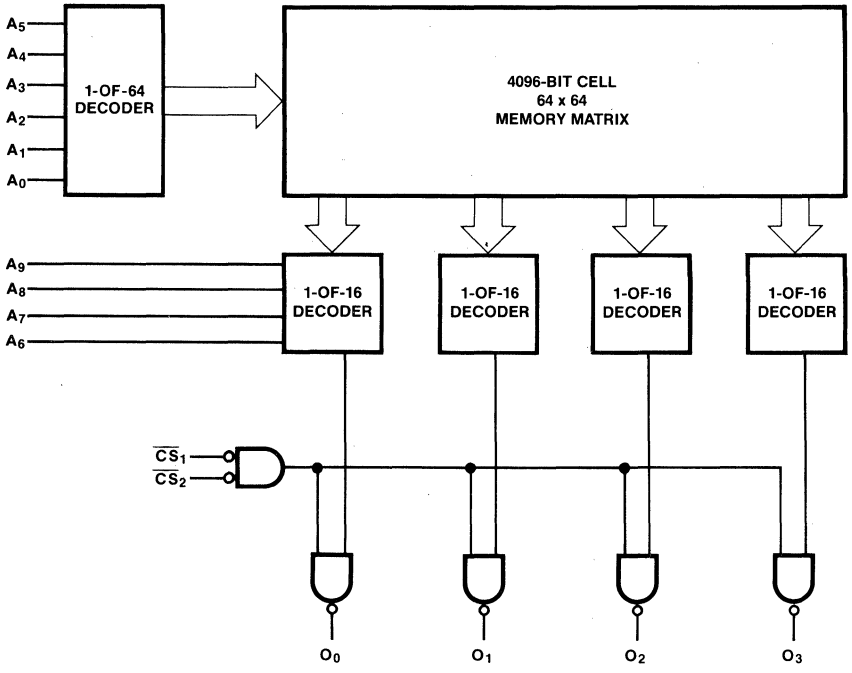
**18-Pin DIP** (Top View)




**Note:**
The 18-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

6

## Logic Diagram




### Functional Description

The 93453 is a TTL bipolar field Programmable Read Only Memory (PROM) organized 1024 words by four bits per word.

Two active LOW Chip Select inputs are provided for logic flexibility and for memory array expansion of up to 16,384 bits without affecting system performance, eliminating the need for external decoding. The device is enabled only when $\overline{CS}_1$ and $\overline{CS}_2$ are LOW, otherwise the outputs are disabled.

The 93453 uses industry proven nichrome fuses. An unprogrammed device is supplied with all bits in the logic '1' (HIGH) state. Bits can be selectively programmed to the logic '0' (LOW) state by following the specified procedure for programming nichrome fuses.

The device contains an internal test row and test column which are accessed and programmed during testing of the device. These fuses are used to assure high programmability and to guarantee AC and DC performance.

The read function is identical to that of a conventional Read Only Memory (ROM). A binary address is applied to the address pins $A_0$ through $A_9$ and the chip selected. Data is then available at the outputs after $t_{AA}$.

**DC Characteristics:** Over guaranteed operating ranges unless otherwise noted

| Symbol | Characteristic | Min | Typ(1) | Max | Unit | Condition | |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | Guaranteed Input LOW Voltage for All Inputs | |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs | |
| $V_{IC}$ | Input Clamp Diode Voltage | | | −1.2 | V | $V_{CC}$ = Min, $I_{IN}$ = −18 mA | |
| $V_{OL}$ | Output LOW Voltage | | 0.30 | 0.45 | V | $V_{CC}$ = Min, $I_{OL}$ = 16 mA | |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $V_{CC}$ = Min, $I_{OH}$ = −2.0 mA | |
| $I_{IL}$ | Input LOW Current | | −160 | −250 | μA | $V_{CC}$ = Max, $V_{IL}$ = 0.45 V | |
| $I_{IH}$ | Input HIGH Current | | | 40 | μA | $V_{CC}$ = Max, $V_{IH}$ = 2.4 V | |
| $I_{OHZ}$ | Output Leakage Current for High Impedance State | | | 50<br>−50 | μA<br>μA | $V_{OH}$ = 2.4 V<br>$V_{OL}$ = 0.4 V | 0°C to +75°C |
| $I_{OHZ}$ | Output Leakage Current for High Impedance State | | | 100<br>−100 | μA<br>μA | $V_{OH}$ = 2.4 V<br>$V_{OL}$ = 0.4 V | −55°C to +125°C |
| $I_{OS}$ | Output Short-Circuit Current | −15 | −35 | −90 | mA | $V_{CC}$ = Max, $V_O$ = 0 V, Note 2 | |
| $I_{CC}$ | Power Supply Current | | 110 | 140 | mA | $V_{CC}$ = Max | |

**Commercial**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 5%, GND = 0 V, $T_A$ = 0°C to +75°C

| Symbol | Characteristic | Max | Unit | Condition |
|---|---|---|---|---|
| $t_{AA}$ | Address to Output Access Time | 40 | ns | See AC Test Output Load |
| $t_{ACS}$ | Chip Select to Output Access Time | 25 | ns | See AC Test Output Load |

**Military**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 10%, GND = 0 V, $T_A$ = 55°C to +125°C

| Symbol | Characteristic | Max | Unit | Condition |
|---|---|---|---|---|
| $t_{AA}$ | Address to Output Access Time | 55 | ns | See AC Test Output Load |
| $t_{ACS}$ | Chip Select to Output Access Time | 30 | ns | See AC Test Output Load |

1. Typical values are at $V_{CC}$ = 5.0 V, $T_A$ = +25°C and maximum loading.
2. Not more than one output to be shorted at a time. Duration of the short circuit should not exceed one second.

**Programming**

The 93453 is manufactured with all bits in the logic "1" state. Any desired bit (output) can be programmed to a logic "0" state by following the procedure shown below. One may build a programmer to satisfy the specifications or buy any of the commercially available programmers which meet these specifications.

**Programming Sequence**

The 93453 is programmed using the following method.

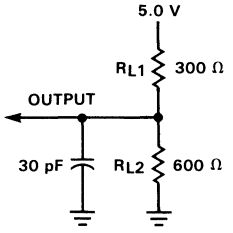
1. Apply the proper power, $V_{CC}$ = 5.0 V, GND = 0 V.
2. Select the word to be programmed by applying the appropriate voltages to the Address pins $A_0$ through $A_9$.
3. Enable the chip for programming by application of $V_{IH}$ (logic "1") to Chip Select ($\overline{CS}_1$), or ($\overline{CS}_2$), or both.
4. Apply the $V_{OP}$ programming to the output associated with the bit to be programmed. The other outputs may be left open or tied to any logic "1" (output HIGH), *i.e.*, 2.4 V to 5.0 V. Note that only one output may be programmed at a time.
5. To verify the logic "0" in the bit just programmed, remove the programming pulse from the output, lower $V_{CC}$ to the Low $V_{CC}$ Read recommended value and sense the output after applying a logic "0" to Chip Selects $\overline{CS}_1$ and $\overline{CS}_2$.
6. The above procedure is then repeated to program other bits on the chip.

**Programming Specifications**

| Symbol | Characteristic | Min | Recommended Value | Max | Unit | Comment |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Address Input | 2.4 | 5.0 | 5.0 | V | Do not leave input open |
| $V_{IL}$ | | 0 | 0 | 0.4 | V | |
| $\overline{CS}_1$, $\overline{CS}_2$ | Chip Select | 2.4 | 5.0 | 5.0 | V | $\overline{CS}_1$, $\overline{CS}_2$ or both |
| $V_{OP}$ | Programming Voltage Pulse | 20 | 20.5 | 21 | V | Applied to output to be programmed |
| $t_{pw}$ | Programming Pulse Width | 0.05 | 0.18 | 50 | ms | All bits can be programmed in ≤ 4.1 seconds |
| | Duty Cycle, Programming Pulse | | 20 | * | % | *Maximum duty cycle to maintain $T_C$ < 85°C |
| $t_r$ | Programming Pulse Rise Time | 0.5 | 1.0 | 3.0 | μs | |
| | Number of Pulses Required | 1 | 4 | 8 | | |
| $V_{CC}$ | Power Supply Voltage | 4.9 | 5.0 | 5.1 | V | |
| $T_C$ | Case Temperature | | 25 | 85 | °C | |
| $I_{OP}$ | Programming Pulse Current Limit | | | 100 | mA | If pulse generator is used, set current limit to this maximum value |
| $LV_{CC}$ | Low $V_{CC}$ Read | 4.2 | 4.2 or 4.4 | 4.4 | V | Programming Read Verify** |

**4.2 V simulates −55°C operation, 4.4 V simulates 0°C operation.

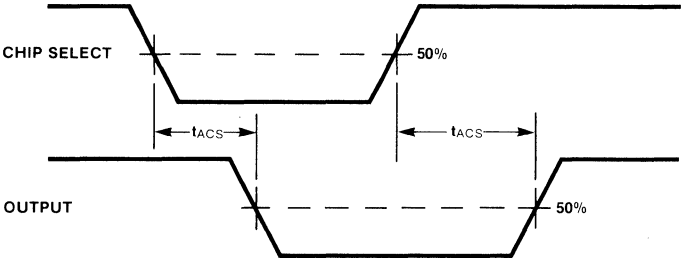
## Fig. 1 AC Test Output Load



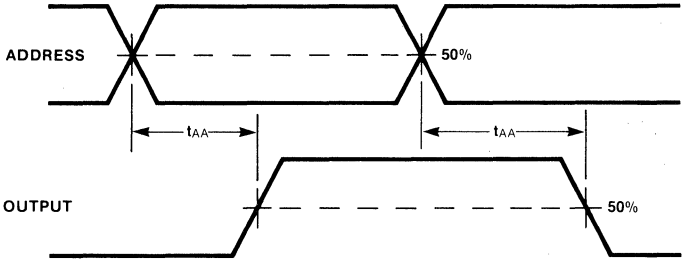

**Test Conditions**
Input Pulse: 0 V to 3.0 V
Input Pulse Rise and Fall Times: 5 ns between 1 V and 2 V
Measurements made at 1.5 V Level

## Fig. 2 AC Waveforms

### a Propagation Delay from Chip Select to Outputs




### b Propagation Delay from Address to Outputs

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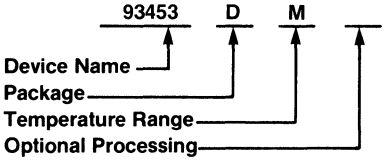
## Ordering Information




**Packages and Outlines** (See Section 10)
D = Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier
P = Plastic DIP

**Temperature Range**
C = 0°C to +75°C
M = −55°C to +125°C

**Optional Processing**
QB = Mil Std 883
Method 5004 and 5005, Level B
QC = Mil Std 883
Method 5004 and 5005, Level C
QR = Commercial Device with
160 Hour Burn In

FAIRCHILD
A Schlumberger Company

Bipolar Division

# 93Z510/93Z511
# 2048 X 8-Bit Programmable Read Only Memory

Isoplanar-Z Vertical Fuse TTL Memory

## Description

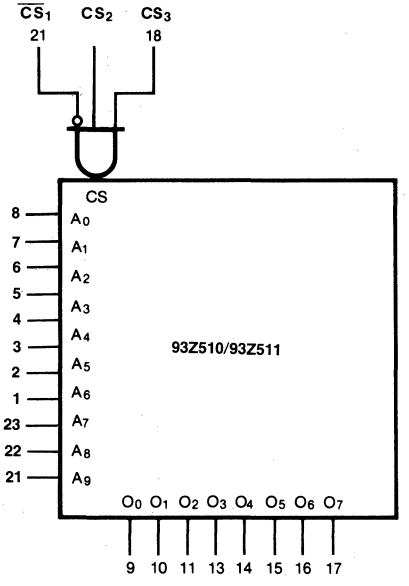
The 93Z510 and 93Z511 are fully decoded 16,384-bit Programmable Read Only Memories (PROMs), organized 2048 words by eight bits per word. The two devices are identical except the 93Z510 has open collector outputs while the 93Z511 has three state outputs.

- **Commercial Address Access Time — 45 ns Max**
- **Military Address Access Time — 55 ns Max**
- **Highly Reliable Vertical Fuses Ensure High Programming Yields**
- **Available with Open Collector (93Z510) or Three State (93Z511) Outputs**
- **Low Current PNP Inputs**

## Pin Names

| | |
|---|---|
| $A_0$–$A_{10}$ | Address Inputs |
| $\overline{CS}_1$ | Chip Select Input (Active LOW) |
| $CS_2$, $CS_3$ | Chip Select Inputs (Active HIGH) |
| $O_0$–$O_7$ | Data Outputs |

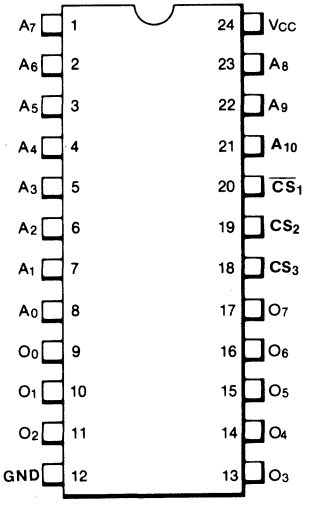
## Logic Symbol




$V_{CC}$ = Pin 24
GND = Pin 12

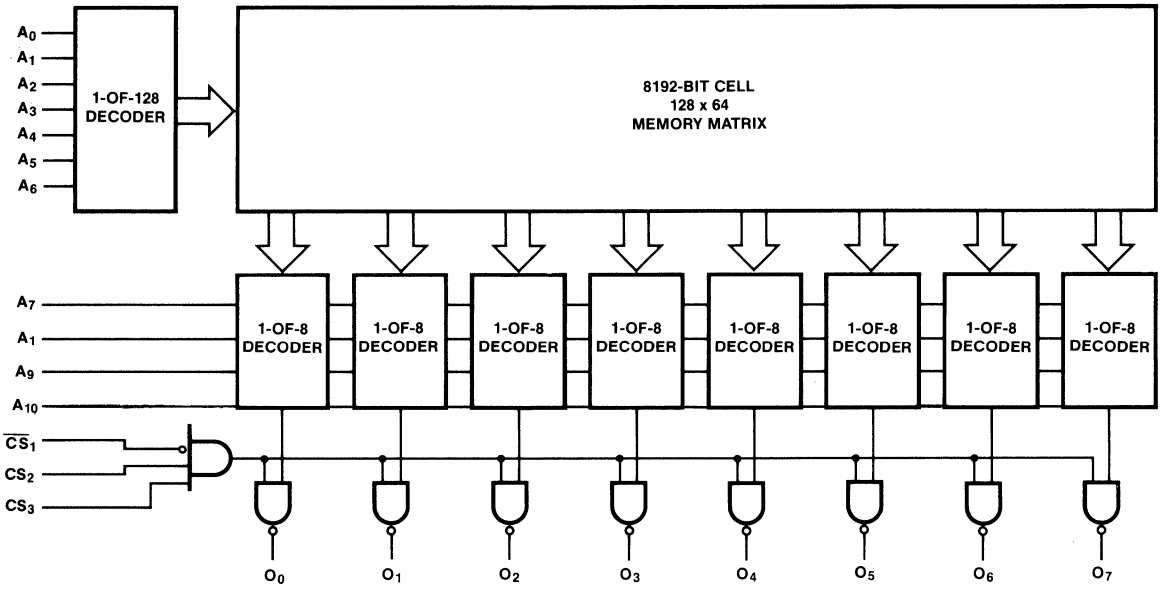
## Connection Diagrams

**24-pin DIP** (Top View)




**Note:**
The 24-pin Flatpak has the same pinout (Connection Diagram) as the 24-pin DIP.

## Logic Diagram

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### Functional Description

The 93Z510 and 93Z511 are TTL bipolar field Programmable Read Only Memories (PROMs) organized 2048 words by eight bits per word. Open-collector outputs are provided on the 93Z510 for use in wired-OR applications. The 93Z511 has 3-state outputs which provide active pull ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.

Three Chip Select inputs are provided for logic flexibility and for memory array expansion of up to 128K without the need for external decoding. The fast Chip Select access time permits direct address decoding without increasing overall memory access times. Both devices are enabled only when $\overline{CS}_1$ is LOW and $CS_2$ and $CS_3$ are HIGH.

The devices contain an internal test row and test column which are accessed and programmed during both wafer sort and final test. These test fuses are used to assure high programmability and to guarantee AC performance and DC parameters.

The 93Z510 and 93Z511 use open base vertical transistor (junction) fuse cells. Initially an unprogrammed cell is in the logic '0' state. Cells can be programmed to a logic '1' state by following the specified programming procedure which fuses aluminum through the emitter base junction of the cell transistor.

The read function is identical to that of a conventional Read Only Memory (ROM). A binary address is applied to the address pins $A_0$ through $A_{10}$ and the chip is selected. Data is then available at the outputs after $t_{AA}$.

## Programming

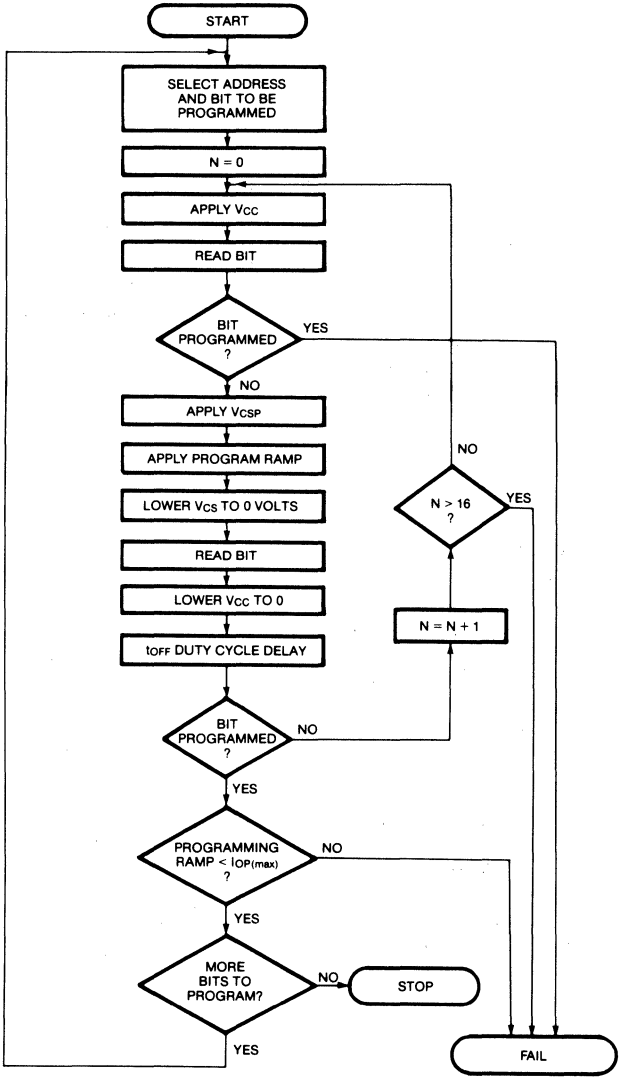
The 93Z510 and 93Z511 are manufactured with all bits in the logic "0" state. Any desired bit (output) can be programmed to a logic "1" state by following the Isoplanar-Z Generic Programming Specifications found at the back of this section.

## Programming Sequence

The 93Z510 and 93Z511 are both programmed using the following method:

1. Address the word to be programmed by applying the appropriate voltages to address pins $A_0$ through $A_{10}$.
2. Apply the proper power for a High $V_{CC}$ read. $V_{CC}$ = 6.5 V, GND = 0 V.
3. Read the output to be programmed and verify it is in the unprogrammed logic '0' state.
4. Enable the chip for programming by application of the Chip Select Programming Voltage ($V_{CSP}$ = 20.0 V) to $\overline{CS}_1$. $CS_2$ and $CS_3$ should remain HIGH.
5. a. To program the bit apply $I_{OP}$, the programming current ramp to the output. NOTE: Only one output may be programmed at a time. The other outputs must be left open.
   b. During the rise of the current ramp, a drop in voltage ($V_{ps}$) at the output may be sensed. This indicates that the current needed to program the junction has been reached and the bit has programmed.
   c. Upon detection of the voltage drop ($V_{ps}$), the current ramp should be held at a constant current for a time ($t_{hAP}$) and then shut off.
6. Once the current ramp has been shut off, lower $V_{CSP}$ to 0 V and read the output.
7. Lower $V_{CC}$ to 0 V. The power supply duty cycle must be less than or equal to 50%.
8. If the read performed in step 6 indicates that the bit has not programmed then go to step 1 and repeat the programming sequence (up to a maximum of 16 attempts total.)
9. If the read performed in step 6 indicates that the bit has programmed then one of the two following conditions exist:
   a. If the required programming current was less than $I_{OP(max)}$ then go to step 10.
   b. If the required programming current was equal to $I_{OP(max)}$ then the device is considered a failure and no future attempts at programming should be made.
10. Repeat the above procedure from step 1 until all the desired bits in the memory have been programmed.

### Programming Flow Chart



**DC Characteristics:** Over guaranteed operating ranges unless otherwise noted

| Symbol | Characteristic | Min | Typ(1) | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | Guaranteed Input LOW Voltage for All Inputs |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs |
| $V_{IC}$ | Input Clamp Diode Voltage | | | −1.2 | V | $V_{CC}$ = Min, $I_{IN}$ = −18 mA |
| $V_{OL}$ | Output LOW Voltage | | 0.30 | 0.45 | V | $V_{CC}$ = Min, $I_{OL}$ = 16 mA |
| $V_{OH}$ | Output HIGH Voltage (93Z511 only) | 2.4 | | | V | $V_{CC}$ = Min, $I_{OH}$ = −2.0 mA |
| $I_{IL}$ | Input LOW Current | | −10 | −100 | μA | $V_{CC}$ = Max, $V_{IL}$ = 0.45 V |
| $I_{IH}$ | Input HIGH Current | −40 | | 40 | μA | $V_{CC}$ = Max, $V_{IH}$ = 2.4 V |
| $I_{OHZ}$ | Output Leakage Current for High Impedance State (93Z511 only) | | | 40<br>−40 | μA | $V_{OH}$ = 2.4 V<br>$V_{OL}$ = 0.4 V |
| $I_{CEX}$ | Output Leakage Current (93Z510 only) | | | 40 | μA | $V_{CEX}$ = $V_{CC}$<br>Chip Deselected |
| $I_{OS}$ | Output Short-Circuit Current (93Z511 only) | −15 | −35 | −90 | mA | $V_{CC}$ = Max, $V_O$ = 0 V, Note 2 |
| $I_{CC}$ | Power Supply Current | | 120 | 175 | mA | $V_{CC}$ = Max |

**Commercial**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 5%, GND = 0 V, $T_A$ = 0°C to +75°C

| Symbol | Characteristic | Max | Unit | Condition |
|---|---|---|---|---|
| $t_{AA}$ | Address to Output Access Time | 45 | ns | See AC Output Load |
| $t_{ACS}$ | Chip Select to Output Access Time | 25 | ns | See AC Output Load |

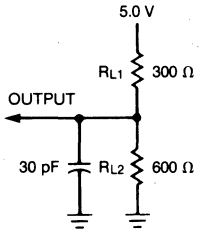
**Military**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 10%, GND = 0 V, $T_A$ = 55°C to +125°C

| Symbol | Characteristic | Max | Unit | Condition |
|---|---|---|---|---|
| $t_{AA}$ | Address to Output Access Time | 55 | ns | See AC Test Output Load |
| $t_{ACS}$ | Chip Select to Output Access Time | 25 | ns | See AC Test Output Load |

1. Typical values are at $V_{CC}$ = 5.0 V, $T_A$ = +25°C and maximum loading.
2. Not more than one output to be shorted at a time. Duration of the short circuit should not exceed one second.

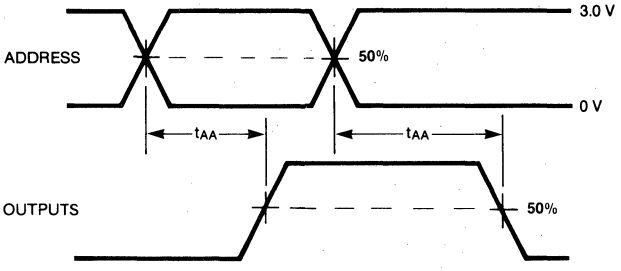
**Fig. 1 AC Test Load**



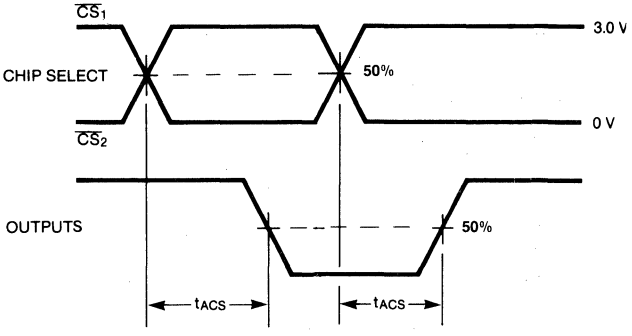

**Test Conditions**
Input pulse: 0 V to 3.0 V
Input pulse rise and fall times: 5 ns between 1 V and 2 V
Measurements made at 1.5 V level

**Fig. 2 AC Waveforms**

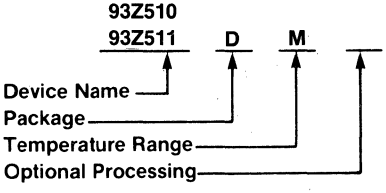
**a Propagation Delay from Address Inputs**




**b Propagation Delay from Chip Select**




## Ordering Information




**Packages**
D = Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier
P = Plastic DIP

**Temperature Ranges**
C = 0°C to +75°C
M = −55°C to +125°C

**Optional Processing**
QB = Mil Std 883
Method 5004 & 5005, Level B
QC = Mil Std 883
Method 5004 & 5005, Level C
QR = Commercial Device with
160 Hour Burn In

FAIRCHILD
A Schlumberger Company

# 93Z564/93Z565
# 8192 x 8-Bit Programmable Read Only Memory

Bipolar Division

Isoplanar-Z Vertical Fuse TTL Memory

## Description

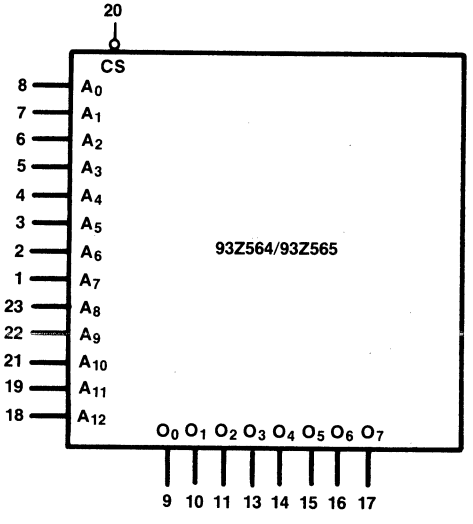
The 93Z564 and 93Z565 are fully decoded 65,536-bit Programmable Read Only Memories (PROMs), organized 8192 words by eight bits per word. The two devices are identical except the 93Z564 has open collector outputs while the 93Z565 has three state outputs. Both devices are available in two speed versions, standard speed and 'A' grade.

- **Commercial Address Access Time**
  **93Z564/93Z565 — 55 ns Max**
  **93Z564A/93Z565A — 45 ns Max**
- **Military Address Access Time**
  **93Z564/93Z565 — 65 ns Max**
  **93Z564A/93Z565A — 55 ns Max**
- **Highly Reliable Vertical Fuses Ensure High Programming Yields**
- **Available with Open Collector (93Z564) or Three State (93Z565) Outputs**
- **Low Current PNP Inputs**

## Pin Names

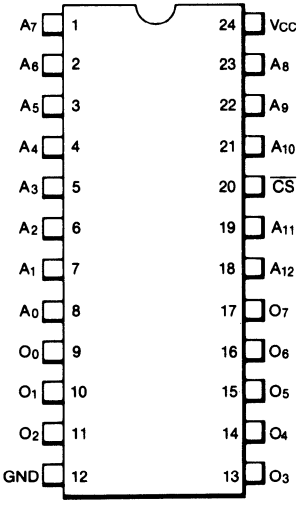
| | |
|---|---|
| $A_0$–$A_{12}$ | Address Inputs |
| $\overline{CS}$ | Chip Select Input (Active LOW) |
| $O_0$–$O_7$ | Data Outputs |

## Logic Symbol




## Connection Diagrams

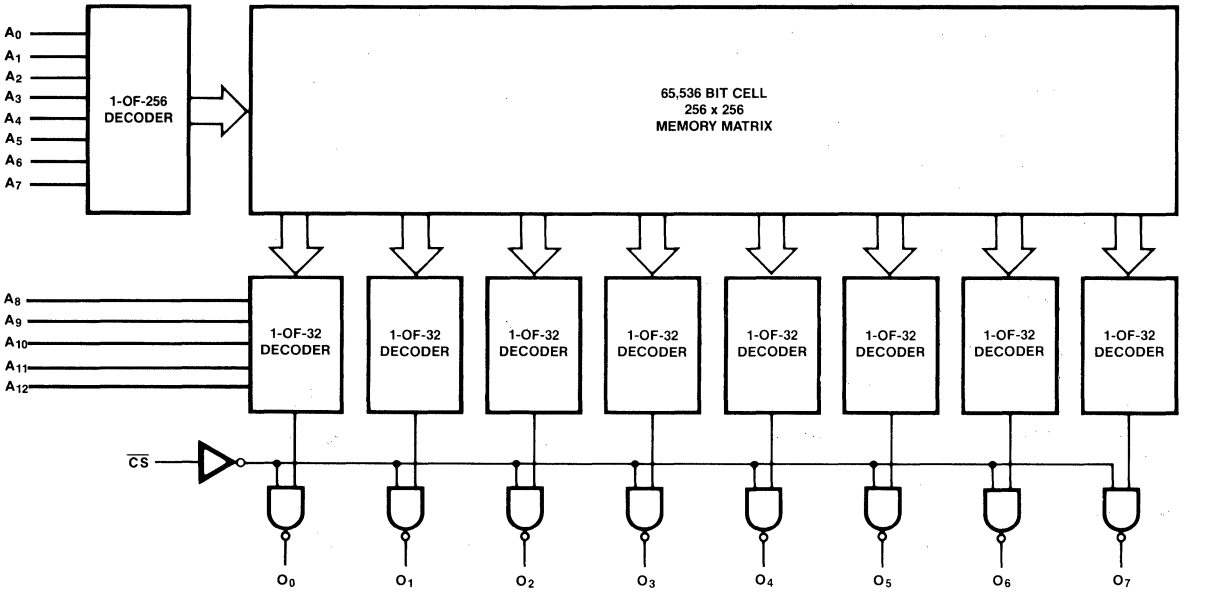
**24-pin DIP** (Top View)




**Note:**
The 24-pin Flatpak has the same pinout (Connection Diagram) as the 24 pin DIP.

6

## Logic Diagram




**Functional Description**

The 93Z564 and 93Z565 are TTL bipolar field Programmable Read Only Memories (PROMs) organized 8192 words by eight bits per word. Open-collector outputs are provided on the 93Z564 for use in wired-OR applications. The 93Z565 has 3-state outputs which provide active pull ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.

One Chip Select input is provided for logic flexibility and for memory array expansion of up to 128K without the need for external decoding. The fast Chip Select access time permits direct address decoding without increasing overall memory access times. Both devices are enabled only when $\overline{CS}$ is LOW.

The 93Z564 and 93Z565 use open base vertical transistor (junction) fuse cells. Initially an unprogrammed cell is in the logic '0' state. Cells can be programmed to a logic '1' state by following the specified programming procedure which fuses aluminum through the emitter base junction of the cell transistor.

The devices contain an internal test row and test column which are accessed and programmed during both wafer sort and final test. These test fuses are used to assure high programmability and to guarantee AC performance and DC parameters.

The read function is identical to that of a conventional Read Only Memory (ROM). A binary address is applied to the address pins $A_0$ through $A_{12}$ and the chip is selected. Data is then available at the outputs after $t_{AA}$.

**Programming**

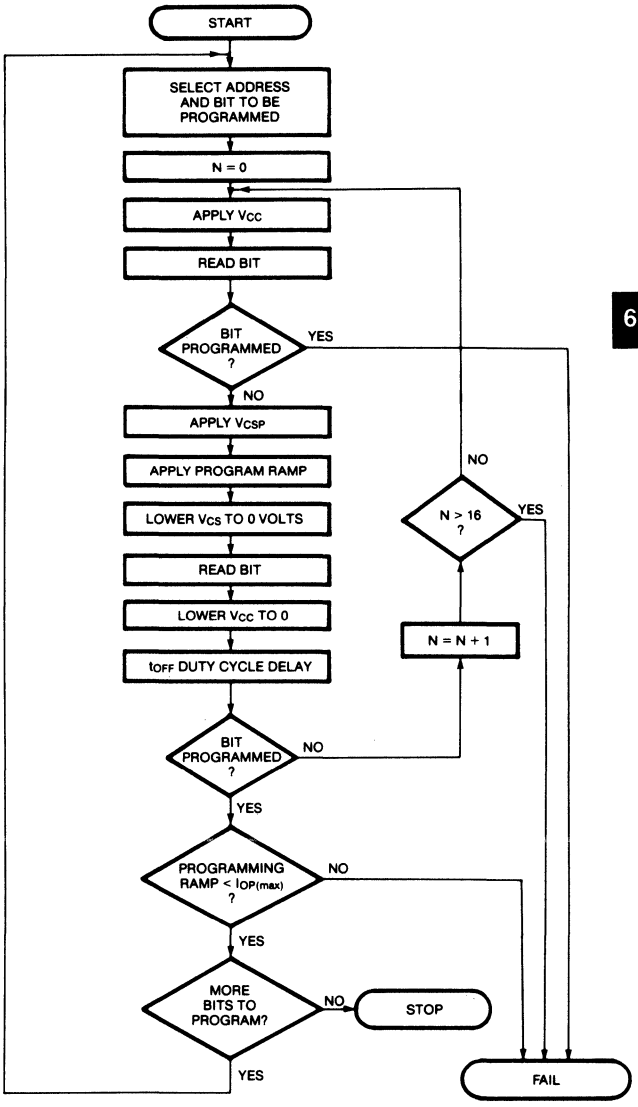
The 93Z564 and 93Z565 are manufactured with all bits in the logic "0" state. Any desired bit (output) can be programmed to a logic "1" state by following the Isoplanar-Z Generic Programming Specifications found at the back of this section.

**Programming Sequence**

The 93Z564 and 93Z565 are both programmed using the following method:

1. Address the word to be programmed by applying the appropriate voltages to address pins $A_0$ through $A_{12}$. Select the PROM by applying a LOW to $\overline{CS}$.
2. Apply the proper power for a High $V_{CC}$ read. $V_{CC}$ = 6.5 V, GND = 0 V.
3. Read the output to be programmed and verify it is in the unprogrammed logic '0' state.
4. Enable the chip for programming by application of the Chip Select Programming Voltage ($V_{CSP}$ = 20.0 V) to $\overline{CS}$.
5. a. To program the bit apply $I_{OP}$, the programming current ramp to the output. NOTE: Only one output may be programmed at a time. The other outputs must be left open.
   b. During the rise of the current ramp, a drop in voltage ($V_{ps}$) at the output may be sensed. This indicates that the current needed to program the junction has been reached and the bit has programmed.
   c. Upon detection of the voltage drop ($V_{ps}$), the current ramp should be held at a constant current for a time ($t_{hAP}$) and then shut off.
6. Once the current ramp has been shut off, lower $V_{CSP}$ to 0 V and read the output.
7. Lower $V_{CC}$ to 0 V. The power supply duty cycle must be less than or equal to 50%.
8. If the read performed in step 6 indicates that the bit has not programmed then go to step 1 and repeat the programming sequence (up to a maximum of 16 attempts total.)
9. If the read performed in step 6 indicates that the bit has programmed then one of the two following conditions exist:
   a. If the required programming current was less than $I_{OP(max)}$ then go to step 10.
   b. If the required programming current was equal to $I_{OP(max)}$ then the device is considered a failure and no future attempts at programming should be made.
10. Repeat the above procedure from step 1 until all the desired bits in the memory have been programmed.

**Programming Flow Chart**



**DC Characteristics:** Over guaranteed operating ranges unless otherwise noted

| Symbol | Characteristic | Min | Typ(1) | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | Guaranteed Input LOW Voltage for All Inputs |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs |
| $V_{IC}$ | Input Clamp Diode Voltage | | | −1.2 | V | $V_{CC}$ = Min, $I_{IN}$ = −18 mA |
| $V_{OL}$ | Output LOW Voltage | | 0.30 | 0.45 | V | $V_{CC}$ = Min, $I_{OL}$ = 16 mA |
| $V_{OH}$ | Output HIGH Voltage (93Z565 only) | 2.4 | | | V | $V_{CC}$ = Min, $I_{OH}$ = −2.0 mA Address Any '1' |
| $I_{IL}$ | Input LOW Current | | −10 | −100 | μA | $V_{CC}$ = Max, $V_{IL}$ = 0.45 V |
| $I_{IH}$ | Input HIGH Current | −40 | | 40 | μA | $V_{CC}$ = Max, $V_{IH}$ = 2.4 V |
| $I_{OHZ}$ | Output Leakage Current for High Impedance State (93Z565 only) | | | 40<br>−40 | μA<br>μA | $V_{OH}$ = 2.4 V<br>$V_{OL}$ = 0.4 V |
| $I_{CEX}$ | Output Leakage Current (93Z564 only) | | | 40 | μA | $V_{CEX}$ = $V_{CC}$ Chip Deselected |
| $I_{OS}$ | Output Short-Circuit Current (93Z565 only) | −15 | −35 | −90 | mA | $V_{CC}$ = Max, $V_O$ = 0 V, Note 2 Address Any '1' |
| $I_{CC}$ | Power Supply Current | | 120 | 180 | mA | $V_{CC}$ = Max |
| $C_{IN}$ | Input Pin Capacitance | | 4.0 | | pF | $V_{CC}$ = 5.0 V, $V_{IN}$ = 4.0 V, f = 1.0 MHz |
| $C_O$ | Output Pin Capacitance | | 7.0 | | pF | $V_{CC}$ = 5.0 V, $V_O$ = 4.0 V, f = 1.0 MHz |

**Commercial**

**AC Characteristics:** $V_{CC}$ = 5.0 V ±5%, GND = 0 V, $T_A$ = 0°C to +75°C

| Symbol | Characteristic | 'A' | Std | Unit | Condition |
|---|---|---|---|---|---|
| $t_{AA}$ | Address to Output Access Time | 45 | 55 | ns | See AC Output Load |
| $t_{ACS}$ | Chip Select to Output Access Time | 25 | 30 | ns | See AC Output Load |

**Military**

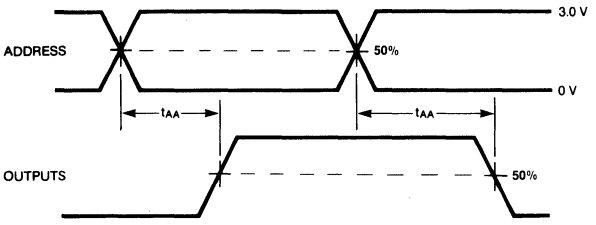
**AC Characteristics:** $V_{CC}$ = 5.0 V ±10%, GND = 0 V, $T_A$ = 55°C to +125°C

| Symbol | Characteristic | 'A' | Std | Unit | Condition |
|---|---|---|---|---|---|
| $t_{AA}$ | Address to Output Access Time | 55 | 65 | ns | See AC Output Load |
| $t_{ACS}$ | Chip Select to Output Access Time | 30 | 35 | ns | See AC Output Load |

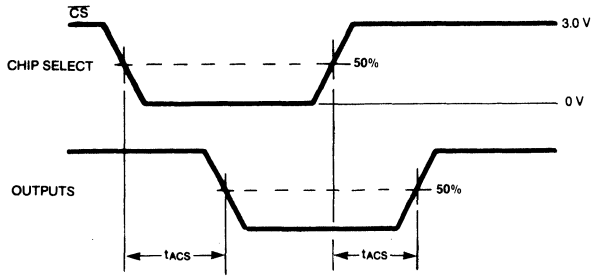
1. Typical values are at $V_{CC}$ = 5.0 V, $T_A$ = +25°C and maximum loading.
2. Not more than one output to be shorted at a time. Duration of the short circuit should not exceed one second.

## Fig. 1 Read Mode Timing

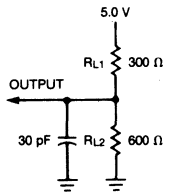
### a Propagation Delay from Address to Output




### b Propagation Delay from Chip Select to Output

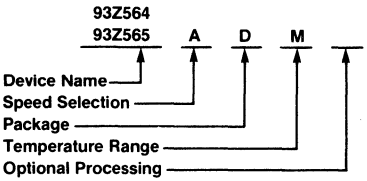



## Fig. 2 AC Test Output Load




**Test Conditions**
Input Pulse: 0 V to 3.0 V
Input Pulse Rise and Fall Times: 5 ns between 1 V and 2 V
Measurements made at 1.5 V Level

## Ordering Information




**Speed Selection**
Blank = High Speed
A = A Grade

**Packages**
D = Ceramic DIP
L = Leadless Chip Carrier

**Temperature Ranges**
C = 0°C to +75°C
M = −55°C to +125°C

**Optional Processing**
QB = Mil Std 883
Method 5004 & 5005, Level B
QC = Mil Std 883
Method 5004 & 5005, Level C
QR = Commercial Device with
160 Hour Burn In

# Isoplanar-Z Junction Fuse Principles and Programming

Conventional fusible link bipolar PROMs and programmable logic devices are based upon two dimensional matrices of electrically conductive thin film fusible elements of materials such as nichrome, titanium tungsten, platinum silicide or polysilicon. Each of these thin film technologies has its own unique advantages and disadvantages but all have in common the fact that fuses lie flat on the surface of the silicon and therefore occupy a significant portion of silicon area. Cell area has become increasingly important as device densities have grown from 4K to 64K. Manufacturing cost, yields and performance are all directly related to die size which is a strong function of cell area. Previously, reductions in cell area have been accomplished primarily through improvements in photolithographic techniques. Such techniques have been pushed to their limits to produce high density, cost effective programmable memories and logic. The need to shrink cell sizes, especially in higher density devices, is placing severe strains on the manufacturability of thin film fuses.

Junction fuses are the emerging solution to the inherent problems posed by thin film fuses. A junction fuse is simply a PN junction programmable cell. The emitter-base junction of a floating base NPN transistor acts as the fuse element. Because fuses are single vertical transistors (hence the often used name of vertical fuses), they occupy minimal silicon area. The entire fuse structure can essentially be modeled as two diodes connected back-to-back. Before programming, a high impedence (open) path exists between the emitter and collector. The emitter-base diode is reverse biased, preventing read currents from passing through the fuse. During programming, the emitter-base junction is shorted out, leaving a forward biased base-collector (B-C) diode. This diode now appears as a low impedence (closed) path. The fuse has been programmed from a logic 0 to a logic 1. The fuse junction lies beneath the surface of the silicon so all of the potential thin film fuse related failure modes such as metal migration (growback), freeze out, corrosion, marginally opened fuses and passivation scattering have been eliminated.

The major problem encountered in early P-N junction programmable junction fuse development was the requirement of a large cell programming current (typically 200 mA per cell). This large current meant that large transistors were needed in the peripheral programming circuitry. The gain in array size reduction due to small cells was offset by the need for a larger peripheral programming circuitry which, in turn, translated to larger overall die size and higher die cost. The costs were such that, despite their reliability advantages, these devices were never widely commercially accepted.

The most straightforward method to achieve reductions in cell programming current is to use small emitter cells. A small emitter cell increases the effective current density at the emitter-base junction therefore decreasing the overall energy required to program the cell. To reduce emitter size and programming currents without the use of advanced photolithographic equipment, Fairchild adopted a simple solution, use a walled emitter cell and an oxide isolated Isoplanar process. With oxide isolation, emitter sizes are defined by the oxide opening and as a result are self aligned, easing manufacturing tolerances.

The main advantages of the Isoplanar-Z process are due to the use of oxide encroachment. The cell emitter is defined using standard photolithography. The surrounding oxide is then laterally grown, shrinking the emitter area and decreasing the effective cell size. Very small self aligned emitter-base junction areas can be achieved quite easily with the encroachment technique. An added benefit of oxide encroachment is that the higher thermal resistivity of the silicon dioxide which surrounds the cells, as compared to silicon, reduces heat loss during programming. This thermal insulation effect further reduces the current required to program a cell. Typical programming currents of 60 mA or below are easily achieved using the Isoplanar-Z process.

Results of reliability and programming yield testing have been excellent. Data have demonstrated typical programming yields in excess of 97% on a 16,384 bit PROM and no cell related failures in over 63 billion cell hours of life test.

*Programming a Junction Fuse*

Programming a junction fuse is accomplished by driving a controlled current through the emitter of the cell, inducing avalanche breakdown of the emitter-base junction. Heat locally generated at the reverse biased junction causes the Aluminum-Silicon interface to reach the

Al-Si eutectic solidus (melting) temperature of approximately 575°C. The electrically conductive aluminum eutectic then diffuses down through the emitter to the emitter-base junction, forming a permanent short.

Once a junction fuse has been programmed, achieving a uniform cell resistance is necessary to insure proper device operation. Due to RC time constant considerations, uniform resistance is especially important in high speed devices. The resistance of the cell is largely determined by the depth of the aluminum eutectic "spike" down into the base depletion layer of the fuse transistor. This depth is determined by the amount of energy applied to the cell after the aluminum spike contacts the emitter-base junction. Too little current is undesireable as the fuse may not remain properly programmed. Too much current is also undesirable since the aluminum eutectic spike may be driven too deep, shorting out both the emitter-base and the base-collector junctions, destroying the fuse and rendering the entire device useless.

Different methods have been used to control the current needed to program a junction fuse. One method is a pulse-read technique, whereby a series of current pulses of uniform magnitude and duration are applied to the cell. Each pulse applies a specific amount of energy to the cell's emitter-base junction, successively heating the junction until the cell emitter reaches the Aluminum-Silicon eutectic temperature. Once this temperature is reached, migration occurs and the junction shorts. A read is performed after each pulse to detect if the fuse has blown. If additional energy is needed to program any cell, more pulses are applied until the cell blows. Once the emitter-base junction has been shorted, a fixed number of additional current pulses are applied to the fuse to attain uniform cell resistance.

However, the fixed number of additional pulses will insure uniform cell resistance accross the array only if cell sizes are uniform across the array. Thus stringent controls must be maintained to produce devices with uniform cell sizes throughout. The amount of current required to program a cell can also change due to process variation or other factors such as array leakages. Any changes in cell programming current requirements will alter the effective energy which reaches the area around the aluminum spike. A difference in the effective energy can change the depth of the spike and therefore affect the cell resistance. In addition, if cell sizes were changed by design to take advantage of process advances or photolithography refinements, the energy needed to guarantee uniform cell resistance would change. A change in the designed cell size requires that either the number of extra pulses or the pulse width must be changed.

To solve all of the problems posed by varying cell size, Fairchild developed a self adjusting current ramp programming technique which delivers the optimum current needed to program each individual cell. With the self adjusting technique a steadily increasing current ramp is applied to a cell until a shorted junction is detected. The exact moment when the junction actually shorts can be sensed by a sharp drop in the voltage across the cell. This voltage drop occurs because the reverse biased E-B diode is no longer in series with the programming path.

Once the moment of programming has been detected, Fairchild incorporates the use of a programming ramp "post hold time". The rise in programming current is halted at the level which was required to cause a blow, held for a precise time interval, and then turned off. This means that the amount of additional energy applied to a cell is totally governed by the amount of current required to program that cell, which is in turn dependent upon cell size. Therefore each cell's additional energy pulse is custom tailored for that specific cell. Experimental data shows that a carefully chosen post hold time can insure a very uniform cell resistance regardless of cell size. The self adjusting current ramp programming scheme allows consistent, repeatable programming and uniform cell resistance, overcoming any effects of process variations on a particular product or differences in cell sizes across product lines. The same self adaptive programming algorithm can be applied to all future products independent of cell size and total memory density.

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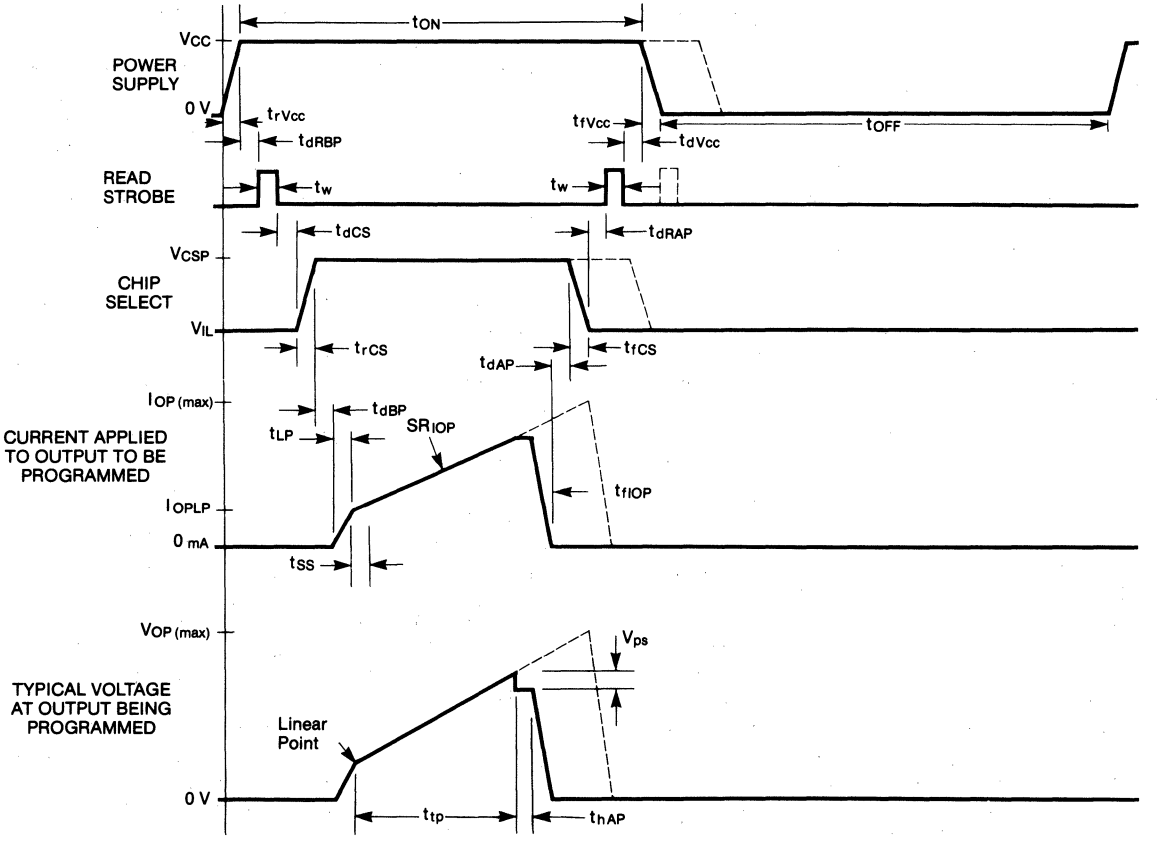
# Isoplanar-Z TTL PROM Generic Programming Specifications

## Programming Timing Diagram




## Programming Specifications(4)

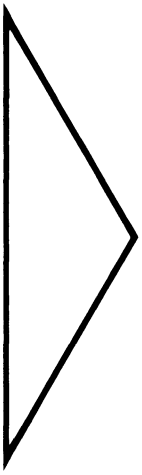
| Symbol | Parameter | Min | Recommended Value | Max | Units | Comments |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| $V_{CC}$ | Power Supply Voltage | 6.3 | 6.5 | 6.7 | V | Typical $I_{CC}$ at 6.5 V = 250 mA |
| $t_{rVcc}$ | Power Supply Rise Time(3) | 0.2 | 2.0 | | μs | |
| $t_{fVcc}$ | Power Supply Fall Time | 0.2 | 2.0 | | μs | |
| $t_{ON}$ | $V_{CC}$ On Time | (1) | | | | See Programming Timing Diagram |
| $t_{OFF}$ | $V_{CC}$ Off Time | (2) | | | | |
| | Duty Cycle for $V_{CC}$ | | | 50 | % | $t_{ON}/(t_{OFF} + t_{ON})$ |

**Programming Specifications**(4) (Cont'd)

| Symbol | Parameter | Min | Recommended Value | Max | Units | Comments |
|---|---|---|---|---|---|---|
| **Read Strobe** | | | | | | |
| $t_{dRBP}$ | Read Delay before Programming | 2.0 | 3.0 | | μs | Initial Check |
| $t_w$ | Fuse Read Time | | 1.0 | | μs | |
| $t_{dVcc}$ | Delay to $V_{CC}$ Off | | 1.0 | | μs | |
| $t_{dRAP}$ | Delay to Read after Programming | 2.0 | 3.0 | | μs | Verify |
| **Chip Select** | | | | | | |
| $V_{CSP}$ | Chip Select Programming Voltage | 19.5 | 20.0 | 20.5 | V | |
| $I_{CSP}$ | Chip Select Program Current Limit | 175 | 180 | 185 | mA | |
| $V_{IL}$ | Input Voltage LOW | 0 | 0 | 0.4 | V | |
| $V_{IH}$ | Input Voltage HIGH | 2.4 | 5.0 | 5.0 | V | |
| $t_{dCS}$ | Delay to Chip Deselect | | 1.0 | | μs | |
| $t_{rCS}$ | Chip Select Pulse Rise Time | 3.0 | 4.0 | | μs | |
| $t_{dAP}$ | Delay to Chip Select Time | 2.0 | 3.0 | | μs | |
| $t_{fCS}$ | Chip Select Pulse Fall Time | 0.2 | 4.0 | | μs | |
| **Current Ramp** | | | | | | |
| $I_{OPLP}$ | Programming Current Linear Point | | 10 | 11 | mA | Point after which the programming current ramp must rise at a linear slew rate |
| $I_{OP(max)}$ | Output Programming Current Limit | 155 | 160 | 165 | mA | Apply current ramp to selected output |
| $V_{OP(max)}$ | Output Programming Voltage Limit | 24 | 25 | 26 | V | |
| $SR_{IOP}$ | Current Slew Rate | 0.9 | 1.0 | 1.1 | mA/μs | Constant after Linear Point |
| $V_{PS}$ | Blow Sense Voltage | 0.7 | | | V | |
| $t_{dBP}$ | Delay to Programming Ramp | 2.0 | 3.0 | | μs | |
| $t_{LP}$ | Time to Reach Linear Point | 0.2 | 1.0 | 10 | μs | |
| $t_{SS}$ | Program Sense Inhibit | 2.0 | 3.0 | 4.0 | μs | |
| $t_{tp}$ | Time to Program Fuse | 3.0 | | 137 | μs | |
| $t_{hAP}$ | Programming Ramp Hold Time | 1.4 | 1.5 | 1.6 | μs | After fuse programs |
| $t_{fIOP}$ | Program Ramp Fall Time | | 0.1 | 0.2 | μs | |

**Notes**
1. Total time $V_{CC}$ is on to program fuse is equal to or greater than the sum of all the specified delays, pulse widths and rise/fall times.
2. $t_{OFF}$ is equal to or greater than $t_{ON}$.
3. Rise and fall times are from 10% to 90%.
4. Recommended programming temp. $T_A = 25°C \pm 10°C$.

# Notes



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# F100Z459
# 16 x 24 x (8 + $\overline{8}$) Field Programmable Logic Array

Bipolar Division

F100K Programmable Logic Array

## Description

The F100Z459 is a high speed bipolar Field Programmable Logic Array (FPLA), organized with 16 inputs, 24 product terms and eight outputs. The 16 inputs are fuse linked to the inputs of 24 AND gates (24 product terms). Each of the 24 AND gates are fuse linked to eight 24-input OR gates (eight summing terms). Each summing term is fed into an output register where the outputs are available in both true and complement form. The output registers are operable in either edge triggered or transparent modes determined by the state of the register enable pins $E_a$ or $E_b$. In the edge triggered mode, the registers operate as a negative edge triggered D flip-flops controlled by the common clock CP. The device also contains two clock enables, a Master Set, three Set Direct inputs and a Set Enable.

The F100Z459 on-chip maintenance circuit is an 11-bit shift register which is outside the data path. Various test points within the FPLA can be loaded in parallel and then shifted out for external diagnostics. One of these test points is the output of an interconnect integrity monitor which detects signal pin faults such as an open or a short to $V_{CC}$. The other test points monitor the state of the output registers and the common clock CP.

- **Output Latches Operable in Edge or Level Enable Modes**
- **Transparent Input to Output Time — 4 ns Max**
- **Synchronous Clock Rate — 125 MHz Max**
- **Both True and Complement Outputs Available**
- **Highly Reliable Junction Fuses Ensure High Programming Yields**
- **On Chip Maintenance Circuit for In-System Monitoring and Checkout**
- **Interconnect Integrity Monitor Detects Signal Pin Faults**
- **Power Dissipation — 2.8 W Typ**

## Connection Diagram
## 64-Pin Pin Grid Array

**TO BE DETERMINED**

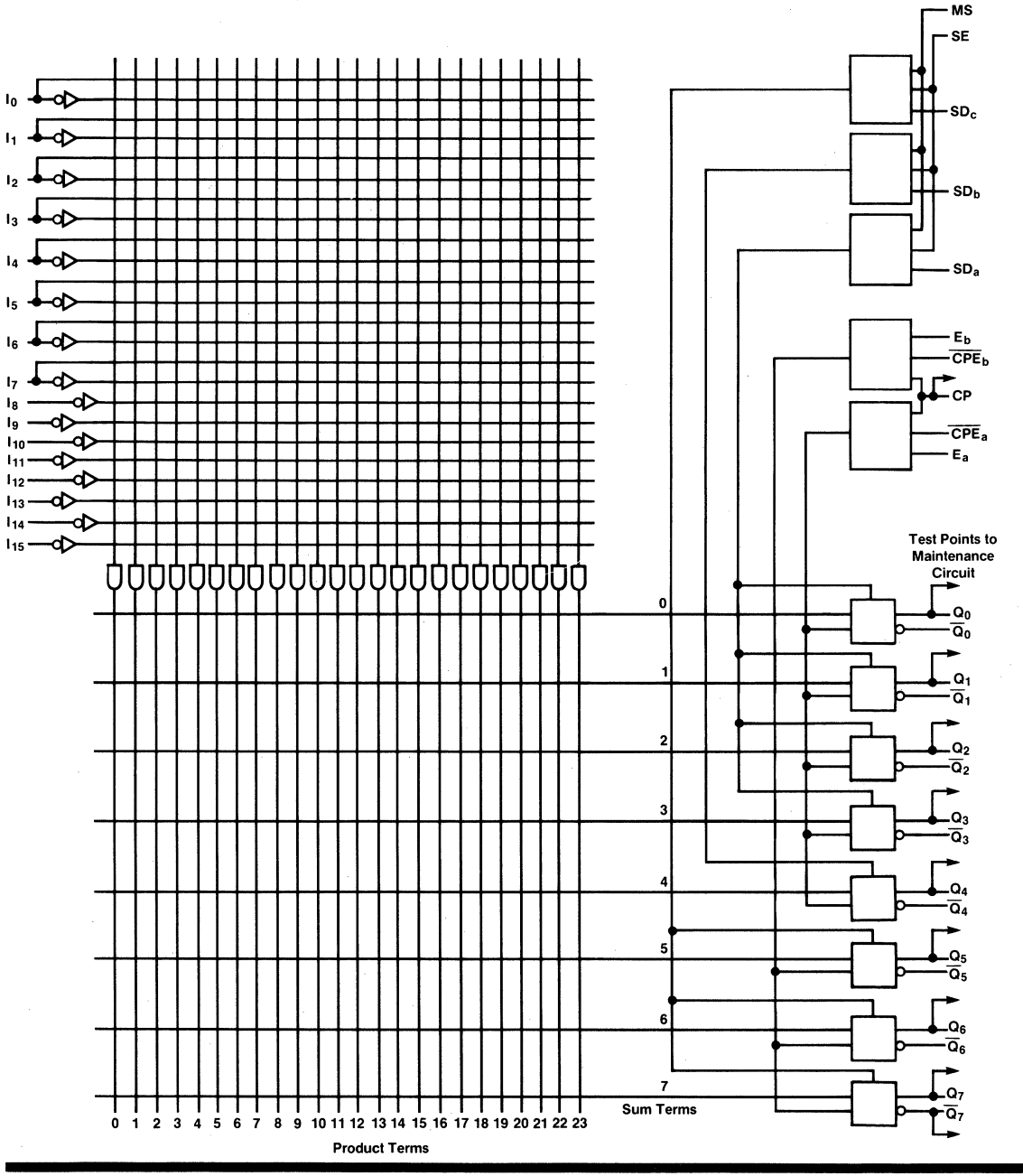


**Pin Names**

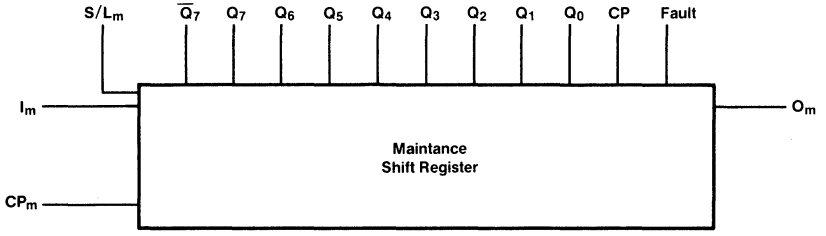
| | |
|---|---|
| $I_0$-$I_{15}$ | Inputs |
| $Q_0$-$Q_7$ | True Outputs |
| $\overline{Q_0}$-$\overline{Q_7}$ | Complement Outputs |
| CP | Common Clock |
| $E_a$, $E_b$ | Register Enables |
| $\overline{CPE_a}$, $\overline{CPE_b}$ | Clock Enables (Active LOW) |
| $SD_a$, $SD_b$, $SD_c$ | Set Direct Inputs |
| SE | Set Enable |
| MS | Master Set |
| $I_m$ | Maintenance Serial Data Input |
| $O_m$ | Maintenance Serial Data Output |
| $CP_m$ | Maintenance Clock |
| $L/S_m$ | Maintenance Load/Shift |

7

## Logic Diagram



**Maintenance Circuit Logic Diagram**




**Functional Description**

The F100Z459 is a high speed ECL Field Programmable Logic Array (FPLA) organized 16 x 24 x (8+$\overline{8}$). A common clock CP can be used to latch data into the negative edge triggered registers. $\overline{CPE}_a$ and $\overline{CPE}_b$ are separate clock enables which control the clocking operations of $Q_0$-$Q_4$ and $Q_5$-$Q_7$ and their complements respectively. These clock enables mask out the clock when in a HIGH state. Two register enables ($E_a$ and $E_b$) override the internal clock generation circuit and make the registers transparent. If either $E_a$ or $E_b$ are HIGH then the corresponding registers become transparent, *i.e.,* the outputs of the registers follow their inputs independent of the clock. When a register enable is LOW the output stores the data which was present on its inputs before that enable went LOW. Master Set (MS) Set Enable (SE), and individual Set Direct controls ($SD_a$, $SD_b$ and $SD_c$) are available for the output registers. Three Set Direct inputs $SD_a$, $SD_b$ and $SD_c$ set outputs $Q_0$ through $Q_3$, $Q_4$ and $Q_5$ through $Q_7$ and reset their complements respectively.

An on-chip maintenance circuit, which is not in the data path, provides the capabilities of monitoring various test points in the device. The shift register is parallel loaded with the status of the output latches, the status of CP and the status of an interconnection integrity monitor. $CP_m$ is an independent clock which is used to shift the maintenance data out. Maintenance Serial Data Input ($I_m$) and Maintenance Serial Data Output ($O_m$) are provided for expansion. The interconnect integrity monitor is a zero's catching flip-flop with input circuitry which detects faults such as an open or a short to $V_{CC}$ on any of the signal pins.

### Output Latch, Asynchronous Set Operation

| Inputs | | | | | Outputs | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| SE | MS | $SD_a$ | $SD_b$ | $SD_c$ | $Q_{0-3}$ | $\overline{Q}_{0-3}$ | $Q_4$ | $\overline{Q}_4$ | $Q_{5-7}$ | $\overline{Q}_{5-7}$ |
| L | X | X | X | X | $Q_n(t)$ | $\overline{Q}_n(t)$ | $Q_n(t)$ | $\overline{Q}_n(t)$ | $Q_n(t)$ | $\overline{Q}_n(t)$ |
| H | L | L | L | L | $Q_n(t)$ | $\overline{Q}_n(t)$ | $Q_n(t)$ | $\overline{Q}_n(t)$ | $Q_n(t)$ | $\overline{Q}_n(t)$ |
| H | L | H | L | L | H | L | $Q_n(t)$ | $\overline{Q}_n(t)$ | $Q_n(t)$ | $\overline{Q}_n(t)$ |
| H | L | L | H | L | $Q_n(t)$ | $\overline{Q}_n(t)$ | H | L | $Q_n(t)$ | $\overline{Q}_n(t)$ |
| H | L | L | L | H | $Q_n(t)$ | $\overline{Q}_n(t)$ | $Q_n(t)$ | $\overline{Q}_n(t)$ | H | L |
| H | H | X | X | X | H | L | H | L | H | L |

t = Time Before Input Transition
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)

### Output Latch, Enable Operation

| Inputs at t | | | | | Outputs at t + 1 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $E_a$ | $E_b$ | $\overline{CPE}_a$ | $\overline{CPE}_b$ | CP | $Q_{0-4}$ | $\overline{Q}_{0-4}$ | $Q_{5-7}$ | $\overline{Q}_{5-7}$ | Comments |
| L | L | L | L | | $D_n(t)$ | $\overline{D}_n(t)$ | $D_n(t)$ | $\overline{D}_n(t)$ | $Q_{0-7}$ Latch new data |
| L | L | L | H | | $D_n(t)$ | $\overline{D}_n(t)$ | $Q_n(t)$ | $\overline{Q}_n(t)$ | $Q_{0-4}$ Latch new data<br>$Q_{5-7}$ Latched, no change |
| L | L | H | L | | $Q_n(t)$ | $\overline{Q}_n(t)$ | $D_n(t)$ | $\overline{D}_n(t)$ | $Q_{0-4}$ Latched, no change<br>$Q_{5-7}$ Latch new data |
| L | L | H | H | X | $Q_n(t)$ | $\overline{Q}_n(t)$ | $Q_n(t)$ | $\overline{Q}_n(t)$ | Latched, no change |
| H | L | X | H | X | $D_n$ | $\overline{D}_n$ | $Q_n(t)$ | $\overline{Q}_n(t)$ | $Q_{0-4}$ Transparent<br>$Q_{5-7}$ Latched, no change |
| L | H | H | X | X | $Q_n(t)$ | $\overline{Q}_n(t)$ | $D_n$ | $\overline{D}_n$ | $Q_{0-4}$ Latched, no change<br>$Q_{5-7}$ Transparent |
| H | H | X | X | X | $D_n$ | $\overline{D}_n$ | $D_n$ | $\overline{D}_n$ | $Q_{0-7}$ Transparent |
| | L | H | H | X | $D_n(t)$ | $\overline{D}_n(t)$ | $Q_n(t)$ | $\overline{Q}_n(t)$ | $Q_{0-4}$ Latch new data<br>$Q_{5-7}$ Latched, no change |
| L | | H | H | X | $Q_n(t)$ | $\overline{Q}_n(t)$ | $D_n(t)$ | $\overline{D}_n(t)$ | $Q_{0-4}$ Latched, no change<br>$Q_{5-7}$ Latch new data |

$D_n$ = Input to Latch from Summing Array
t = Time Before Input Transition
t+1 = Time After Input Transition
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)

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A Schlumberger Company

# 93458/93459
# 16 x 48 x 8 Field Programmable Logic Array

Bipolar Division

Isoplanar Schottky TTL Logic Array

## Description

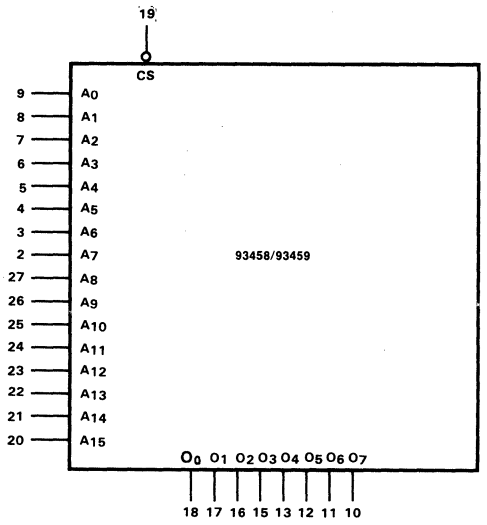
The 93458 and 93459 are bipolar Field Programmable Logic Arrays (FPLAs) organized with 16 inputs, 48 product terms and eight outputs. The 16 inputs and their complements are fuse linked to the inputs of 48 AND gates (48 product terms). Each of the 48 AND gates are fuse linked to eight 48-input OR gates (eight summing terms). Each output may be programmed active HIGH or active LOW. The devices are identical except for the output stage. The 93458 has open-collector outputs; the 93459 has 3-state outputs. In either case, the outputs are enabled when $\overline{CS}$ is LOW.

- **Commercial Address Access Time — 45 ns Max**
- **Military Address Access Time — 65 ns Max**
- **Fully Programmable Product Array, Summing Array and Output Polarity**
- **Available with Open Collector (93458) or Three State (93459) Outputs**
- **Industry Proven Nichrome Fuses**

## Pin Names

| | |
|---|---|
| $\underline{A_0}$-$A_{15}$ | Address Inputs |
| $\overline{CS}$ | Chip Select Inputs |
| $O_0$-$O_7$ | Data Outputs |
| $V_P$ | Programming Pin |

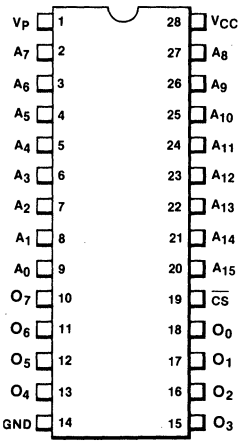
## Logic Symbol




$V_{CC}$ = Pin 28
GND = Pin 14

## Connection Diagram

**28-Pin DIP** (Top View)




**Note**

The 28-pin Flatpak and the 28-pin Leadless Chip Carrier have the same pinout (Connection Diagram) as the 28-pin DIP.

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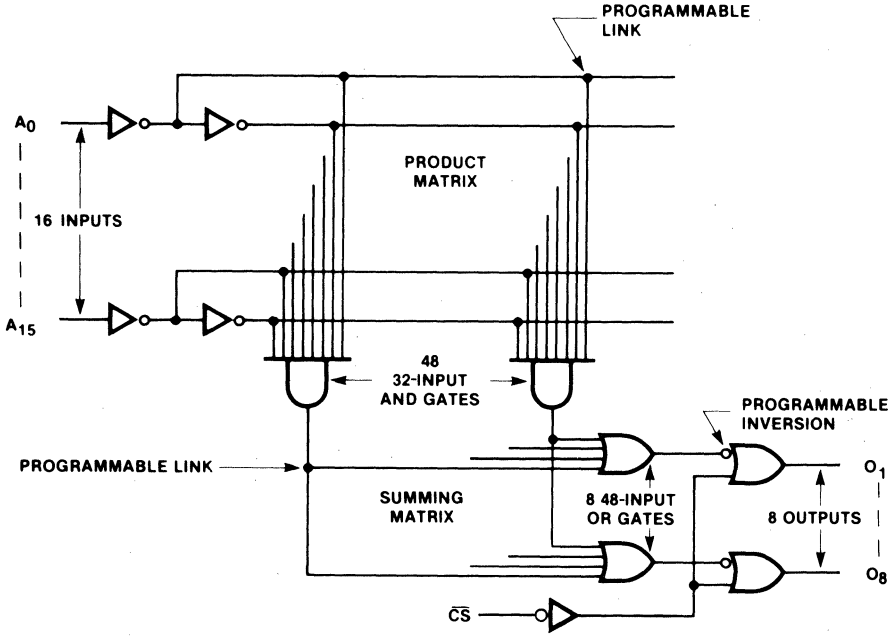
## Logic Diagram




### Functional Description

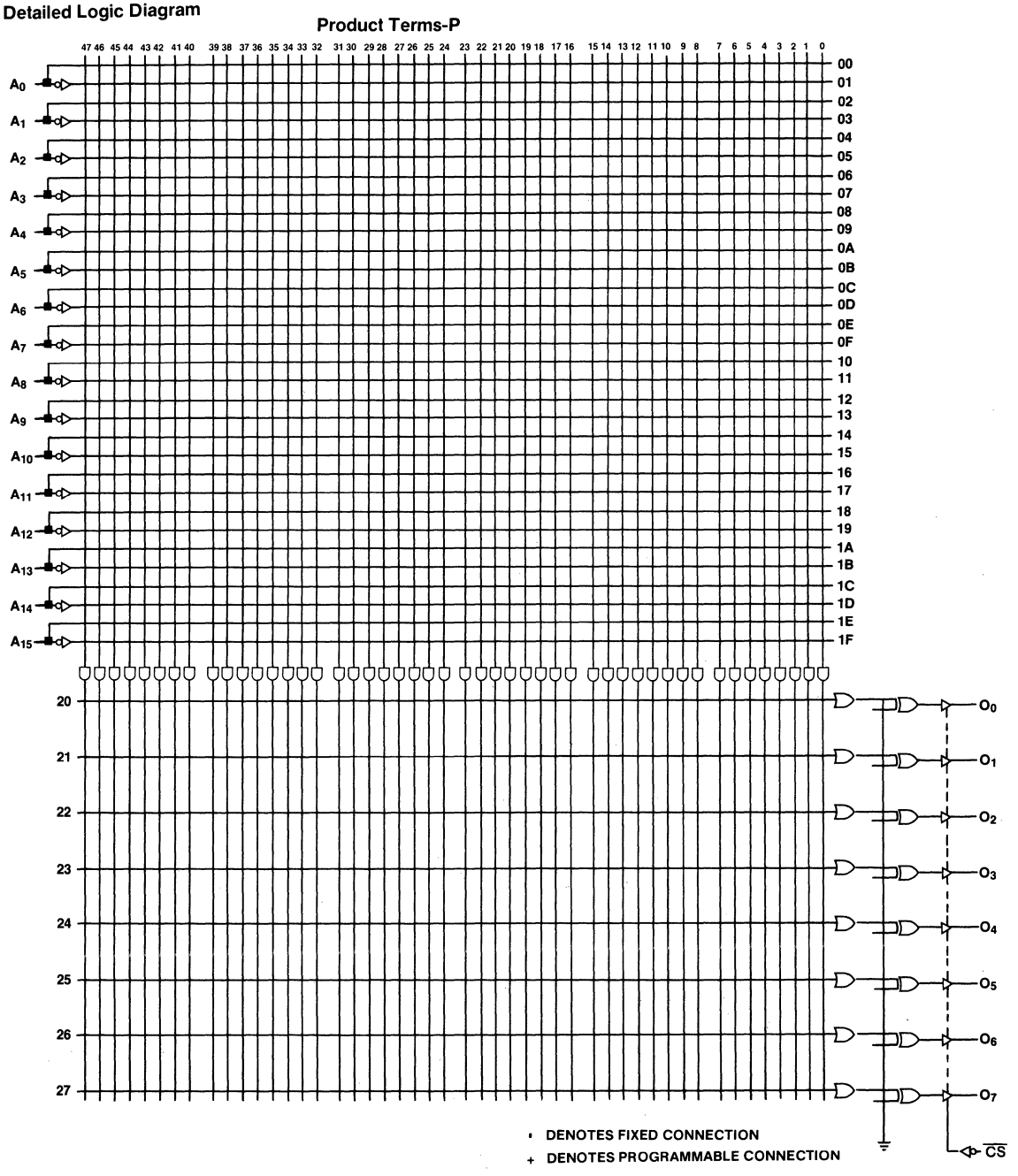
The 93458 and 93459 are bipolar Field Programmable Logic Arrays (FPLAs) organized 16 inputs by 48 product terms by eight outputs. Open-collector outputs are provided on the 93458 for use in wired-OR systems. The 93459 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. Chip Select for both devices is active LOW; i.e., a HIGH (logic "1") on the $\overline{CS}$ pin will disable all outputs.

The 93458 and 93459 both contain a test input line, two test product term lines and a test output line. These test fuses are accessed during both wafer sort and final test and used to assure high programmability and to guarantee DC parameters and AC performance.

The read function is identical to that of a conventional bipolar PLA. That is, a binary address is applied to inputs $A_0$ through $A_{15}$, the chip is selected, and data is valid at the outputs after $t_{AA}$.

Programming (selectively opening nichrome fuse links) is accomplished by following the sequence outlined in the *Programming Specifications* table.

## Detailed Logic Diagram

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**Logic Relationships**

Input Term

$A_n$ — n = 0, . . ., 15, one of 16 inputs

Product Term

$P_m = \pi_0^{15} (i_n A_n + j_n \overline{A}_n)$ — m = 0, . . ., 47, one of 48 product terms where:

a) $i_n = j_n = 0$ for unprogrammed input
b) $i_n \neq j_n$ for programmed input
c) $i_n = j_n = 1$ for Don't Care input

$F_r = \Sigma_0^{47} P_m$ — r = 0, . . ., 7, the OR function of the 48 product terms

Summing Term

$S_r = \Sigma_0^{47} k_m P_m$ — where $k_m = 0$ for product term inactive (programmed)
$k_m = 1$ for product term active (unprogrammed)

| | | | | Output | |
|---|---|---|---|---|---|
| **Mode** | $\overline{CS}$ | $F_r$ | $S_r$ | **Active HIGH** | **Active LOW** |
| Read | L | H | L | L | H |
| | L | H | H | H | L |
| | L | L | X | L | H |
| Disable | H | X | X | H (93458) | H (93458) |
| | H | X | X | High-Z (93459) | High-Z (93459) |

H = HIGH Voltage Levels
L = LOW Voltage Levels
X = Don't Care

By programming, the eight outputs of an FPLA can be made to relate to the 16 inputs as given by the following example:

8 outputs total

$O_1 = A_0 \overline{A}_6 A_{14} + \overline{A}_2 \overline{A}_{15} + \underbrace{\overline{A}_0 A_1 \ldots A_{15}}_{\text{One Product Term, 16 input terms max}} + \overline{A}_8 A_{10} \overline{A}_{13}$

One Output, 48 product terms max

$O_2 = A_0 \overline{A}_6 A_{14} + \overline{A}_2 \overline{A}_{15}$
(Output polarity programmed, active HIGH)

$O_7 = \overline{(\overline{A}_8 A_{10} \overline{A}_{13} + A_4 \overline{A}_7 \overline{A}_9 A_{11} \overline{A}_{12})}$
(Output polarity not programmed, active LOW)

## Programming

The 93458 and 93459 are delivered in an unprogrammed state, characterized by:

- All fuses intact
- All 8 output buffers in active LOW state
- All outputs read HIGH

Programming and verifying the Product Matrix, the Summing Matrix, and the Output Polarity are outlined below.

### Program Product Matrix

All 48 AND gates of the product matrix are fuse linked to both the true and false lines of every input buffer in the initial unprogrammed state. The initial logic expression for the 48 unprogrammed AND gates is $A_0\overline{A_0}A_1\overline{A_1}\ldots A_{15}\overline{A_{15}}$ (where $A_n$ or $\overline{A_n}$ is defined to be an input term). Programming the fuse located by the selection of an input line, $A_n$, and the mth AND gate replaces the input term $A_n$ with '1' in the logic expression for the mth AND gate.

- Program one input at a time.
- All unused inputs of programmed product terms must be programmed as Don't Care.
- Inputs of unused product lines are not required to be programmed.
- Pin 18 ($O_0$) is in the read mode (open collector). Care must be taken so that this pin is either left open, grounded, or loaded such that the current flowing into the pin does not exceed 16 mA.

1. Connect pin 28 ($V_{CC}$) to 5.0 V.
2. Connect pin 14 (GND) to ground.
3. Connect pin 19 ($\overline{CS}$) to a TTL HIGH level.
4. Apply TTL levels to pins 10 through 13, 15, and 16 ($O_7$ through $O_2$) to address an on-chip 1-of-48 decoder to select the AND gate to be programmed ($O_7$ = LSB and $O_2$ = MSB).
5. Apply +12.0 V to all input pins ($A_0$ through $A_{15}$).
6. Apply the proper TTL level to an $A_n$ input pin as follows (program one input at a time):
   a. If the product term to be programmed contains the input term $A_n$ (where n = 0 through 15), lower the $A_n$ pin to a TTL HIGH level.
   b. If the product term to be programmed contains the input term $\overline{A_n}$, lower the $A_n$ to a TTL LOW level.
   c. If the product term does not contain the input terms $A_n$ or $\overline{A_n}$ (i.e., $A_n$ is a "Don't Care" input), perform steps 6a, 7, 6b, and 7.
7. Apply a 15.0 V programming pulse to pin 1 ($V_P$) according to the *Programming Specifications* table.
8. Repeat steps 5 through 7 for each input of the selected product term.
9. Repeat steps 4 through 8 for all other product terms to be programmed.

### Verify Product Matrix

1. Connect pin 28 ($V_{CC}$) to 5.0 V.
2. Connect pin 14 (GND) to ground.
3. Connect pin 19 ($\overline{CS}$) to a TTL HIGH level.
4. Apply TTL levels to pins 10 through 13, 15, and 16 ($O_7$ through $O_2$) to address an on-chip 1-of-48 decoder to select the AND gate to be verified ($O_7$ = LSB and $O_2$ = MSB).
5. Apply +12.0 V to all input pins ($A_0$ through $A_{15}$).
6. Test the state of the $A_n$ input as follows:
   a. Lower the $A_n$ pin to a TTL HIGH level and sense the voltage on pin 18 ($O_0$).
   b. Lower the $A_n$ pin to a TTL LOW level and sense the voltage on pin 18 ($O_0$).
7. The state of the $A_n$ input is determined as follows:

| | $A_n$ = TTL HIGH | $A_n$ = TTL LOW | Condition of $A_n$ for Selected Product Term |
|---|---|---|---|
| | H | H | Don't Care |
| **Level at** | H | L | $A_n$ in P-Term |
| **Output 0** | L | H | $\overline{A_n}$ in P-Term |
| (Notes 1, 2, 3) | L | L | Unprogrammed |

8. Repeat steps 5 through 7 for each input of the selected product term.
9. Repeat steps 4 through 8 for all other product terms.
10. Repeat steps 4 through 9 with $V_{CC}$ at the Low $V_{CC}$ Read recommended value.

**Notes**

1. $O_0$ in this mode functions as an open-collector output.
2. The table above is valid regardless of the polarity (active HIGH or active LOW) of $O_0$.
3. Pin 1 ($V_P$) should be either floating or grounded.

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**Programming Summing Matrix**

All eight OR gates of the summing matrix are fuse linked to the outputs of the AND gates in the initial unprogrammed state. The initial logic expression (sum of products) of the eight unprogrammed OR gates is $P_0 + P_1 + P_2 + \ldots + P_{47}$ where Pm is the product term programmed into the mth AND gate. Programming the fuse located by the selection of the mth AND gate and the nth summing line replaces the product term Pm with '0' in the logic expression of the nth OR gate. The nth summing line is selected by the selection of the nth output buffer where n = 0 through seven.

- Program one input at a time.
- All unused product lines are not required to be programmed.

1. Connect pin 28 ($V_{CC}$) to 5.0 V.
2. Connect pin 14 (GND) to ground.
3. Connect pin 19 ($\overline{CS}$) to a TTL HIGH level.
4. Apply TTL levels to pins 4 through 9 ($A_5$ through $A_0$) to address an on-chip 1-of-48 decoder to select the AND gate to be programmed ($A_0$ = LSB and $A_5$ = MSB).
5. Apply a TTL HIGH level to pins 20 and 21 ($A_{15}$ and $A_{14}$).
6. Connect the remaining input pins to +12.0 V.
7. Apply an 18 V programming pulse (see *Programming Specifications* table) at the pin of the output to be programmed. Other output pins should be either left open or tied to a TTL HIGH level.

**Verify Summing Matrix**

1. Connect pin 28 ($V_{CC}$) to 5 V.
2. Connect pin 14 (GND) to ground.
3. Connect pin 19 ($\overline{CS}$) to a TTL LOW level.
4. Apply TTL levels to pins 4 through 9 ($A_5$ through $A_0$) to address an on-chip 1-of-48 decoder to select the AND gate to be verified ($A_0$ = LSB and $A_5$ = MSB).
5. Apply a TTL HIGH level to pins 20 and 22 ($A_{15}$ and $A_{13}$).
6. Connect the remaining input pins to +12.0 V.
7. Sense the voltage on the output pin to be verified. The programming of the selected product line to the output line can be determined as follows:

| Output Reads (Note) | Fuse Link |
|---|---|
| L | Blown (Inactive) |
| H | Unblown (Active) |

**Note**
The condition of the fuse link can be determined from the table above regardless of the polarity (active HIGH or active LOW) of the output buffer being verified.

8. Repeat steps 4 through 7 with $V_{CC}$ at the Low $V_{CC}$ Read recommended value.

**Program Output Polarity**

The initial unprogrammed state of all eight output buffers is active LOW or inverting. To program an output buffer into the active HIGH or non-inverting state follow the steps shown below:

- Program one output at a time.

1. Connect pin 28 ($V_{CC}$) to 5.0 V.
2. Connect pin 14 (GND) to ground.
3. Connect pin 19 ($\overline{CS}$) to a TTL HIGH level.
4. Apply a TTL level to pins 4 through 9 ($A_5$ through $A_0$).
5. Apply a TTL HIGH level to pin 20 ($A_{15}$).
6. Connect the remaining input pins to +12.0 V.
7. Apply an 18 V programming pulse (see *Programming Specifications* table) to the pin of the output to be programmed. Other output pins should be either left open or tied to a TTL HIGH level.

**Verify Output Polarity**

1. Connect pin 28 ($V_{CC}$) to 5 V.
2. Connect pin 14 (GND) to ground.
3. Connect pin 19 ($\overline{CS}$) to a TTL LOW level.
4. Apply a TTL level to pins 4 through 9 ($A_5$ through $A_0$).
5. Apply a TTL HIGH level to pins 21 and 22 ($A_{14}$ and $A_{13}$).
6. Connect the remaining input pins to +12.0 V.
7. Sense the voltage on the pin of the output buffer to be verified. The condition of the output can be determined as follows:

| Output Reads | Output State |
|---|---|
| H | Active LOW |
| L | Active HIGH |

8. Repeat step 7 with $V_{CC}$ at the Low $V_{CC}$ Read recommended value.

The table given below summarizes the full programming and verifying procedures.

**Summary of Pin Voltages** (Volts)

| | Read | Program Product Matrix | Verify Product Matrix | Program Summing Matrix | Verify Summing Matrix | Program Output Polarity | Verify Output Polarity |
|---|---|---|---|---|---|---|---|
| Pin 1 ($V_P$) | *** | 15.0 | *** | *** | *** | *** | *** |
| Pin 2 ($A_7$) | TTL | 12.0* | 12.0* | 12.0 | 12.0 | 12.0 | 12.0 |
| Pin 3 ($A_6$) | TTL | 12.0* | 12.0* | 12.0 | 12.0 | 12.0 | 12.0 |
| Pin 4 ($A_5$) | TTL | 12.0* | 12.0* | TTL | TTL | TTL HIGH | TTL HIGH |
| Pin 5 ($A_4$) | TTL | 12.0* | 12.0* | TTL | TTL | TTL HIGH | TTL HIGH |
| Pin 6 ($A_3$) | TTL | 12.0* | 12.0* | TTL | TTL | TTL HIGH | TTL HIGH |
| Pin 7 ($A_2$) | TTL | 12.0* | 12.0* | TTL | TTL | TTL HIGH | TTL HIGH |
| Pin 8 ($A_1$) | TTL | 12.0* | 12.0* | TTL | TTL | TTL HIGH | TTL HIGH |
| Pin 9 ($A_0$) | TTL | 12.0* | 12.0* | TTL | TTL | TTL HIGH | TTL HIGH |
| Pin 10 ($O_7$) | READ | TTL | TTL | **** | READ | **** | READ |
| Pin 11 ($O_6$) | READ | TTL | TTL | **** | READ | **** | READ |
| Pin 12 ($O_5$) | READ | TTL | TTL | **** | READ | **** | READ |
| Pin 13 ($O_4$) | READ | TTL | TTL | **** | READ | **** | READ |
| Pin 14 (GND) | GND | GND | GND | GND | GND | GND | GND |
| Pin 15 ($O_3$) | READ | TTL | TTL | **** | READ | **** | READ |
| Pin 16 ($O_2$) | READ | TTL | TTL | **** | READ | **** | READ |
| Pin 17 ($O_1$) | READ | ** | ** | **** | READ | **** | READ |
| Pin 18 ($O_0$) | READ | READ | READ | **** | READ | **** | READ |
| Pin 19 ($\overline{CS}$) | TTL LOW | TTL HIGH | TTL HIGH | TTL HIGH | TTL LOW | TTL HIGH | TTL LOW |
| Pin 20 ($A_{15}$) | TTL | 12.0* | 12.0* | TTL HIGH | TTL HIGH | TTL HIGH | 12.0 |
| Pin 21 ($A_{14}$) | TTL | 12.0* | 12.0* | TTL HIGH | 12.0 | 12.0 | TTL HIGH |
| Pin 22 ($A_{13}$) | TTL | 12.0* | 12.0* | 12.0 | TTL HIGH | 12.0 | TTL HIGH |
| Pin 23 ($A_{12}$) | TTL | 12.0* | 12.0* | 12.0 | 12.0 | 12.0 | 12.0 |
| Pin 24 ($A_{11}$) | TTL | 12.0* | 12.0* | 12.0 | 12.0 | 12.0 | 12.0 |
| Pin 25 ($A_{10}$) | TTL | 12.0* | 12.0* | 12.0 | 12.0 | 12.0 | 12.0 |
| Pin 26 ($A_9$) | TTL | 12.0* | 12.0* | 12.0 | 12.0 | 12.0 | 12.0 |
| Pin 27 ($A_8$) | TTL | 12.0* | 12.0* | 12.0 | 12.0 | 12.0 | 12.0 |
| Pin 28 ($V_{CC}$) | 5.0 | 5.0 | 5.0 | 5.0 | 5.0 | 5.0 | 5.0 |

*For selection of input apply TTL HIGH or TTL LOW
**Left open or TTL HIGH
***Left open or grounded
****Left open, TTL HIGH, or programming pulse

**Programming Specifications**

| Symbol | Characteristic | Min | Recommended Value | Max | Unit | Comment |
|---|---|---|---|---|---|---|
| $V_{IH}$ | TTL Levels | 2.4 | 5.0 | 5.0 | V | Apply to appropriate address and output pins. Do not leave pins open |
| $V_{IL}$ | | 0 | 0 | 0.4 | V | |
| $\overline{CS}$ | Chip Select | 2.4 | 5.0 | 5.0 | V | |
| $V_{OP}$ | Programming Voltage Pulse | 17.5 | 18.0 | 18.5 | V | Applied to appropriate output pin |
| $V_P$ | Programming Voltage Pulse | 14.5 | 15.0 | 15.5 | V | Apply to $V_P$ pin |
| $t_{pw}$ | Programming Pulse Width | | 0.18 | 50 | ms | |
| | Duty Cycle, Programming Pulse | | 20 | * | % | *Maximum duty cycle to maintain $T_C < 85°C$ |
| $t_r$ | Programming Pulse Rise Time | 0.5 | 1.0 | 3.0 | $\mu$s | |
| | Number of Pulses Required | 1 | 4 | 8 | | |
| $V_{CC}$ | Power Supply Voltage | 4.9 | 5.0 | 5.1 | V | |
| $T_C$ | Case Temperature | | 25 | 85 | °C | |
| $I_{VP}$ | Programming Pulse Current Limit ($V_P$ Pin) | | | 200 | mA | If pulse generator is used, set current limit to this maximum value |
| $I_{OP}$ | Programming Pulse Current Limit (Any Output Pin) | | | 100 | mA | If pulse generator is used, set current limit to this maximum value |
| $LV_{CC}$ | Low $V_{CC}$ Read | 4.2 | 4.2 or 4.4 | 4.4 | V | Programming Read Verify** |

**4.2 V simulates −55°C operation, 4.4 V simulates 0°C operation.

## 16 x 48 x 8 FPLA Program Table

**This Portion to be Completed by Fairchild**

Customer Name _____ CF (XXXX) _____

Purchase Order # _____ Customer Symbolized Part # _____

Fairchild Device # _____ Date Received _____

Total Number of Parts _____ Comments _____

Program Table # _____ Rev _____ Date _____

| Program Table Entries | | | | | | |
|---|---|---|---|---|---|---|
| Input Variable | | | Output Function | | Output Active Level | |
| $A_n$ | $\overline{A}_n$ | Immaterial | Product Term Present in $F_r$ | Product Term Not Present in $F_r$ | Active HIGH | Active LOW |
| H | L | - (dash) | A | · (period) | H | L |
| **Note** Enter (—) for *unused* inputs of *used* P terms | | | **Notes** 1) Entries independent of output polarity 2) Enter (A) for *unused* outputs of *used* P terms | | **Notes** 1) Polarity programmed once only 2) Enter (L) for all *unused* outputs | |

| | Product Term* | | | | | | | | | | | | | | | | Active Level | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Input Variable | | | | | | | | | | | | | | | | | | | | | | | |
| No. | 1 5 | 1 4 | 1 3 | 1 2 | 1 1 | 1 0 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Output Function* | | | | | | | |
| | | | | | | | | | | | | | | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | | | | | | | | | | | | | | | | | | | | | | | | |
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*Input and Output fields of *unused* P-terms can be left blank

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**DC Characteristics:** Over guaranteed operating ranges unless otherwise noted

| Symbol | Characteristic | Min | Typ(1) | Max | Unit | Condition | |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | Guaranteed Input LOW Voltage for All Inputs | |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs | |
| $V_{IC}$ | Input Clamp Diode Voltage | | | −1.2 | V | $V_{CC}$ = Min, $I_{IN}$ = −18 mA | |
| $V_{OL}$ | Output LOW Voltage | | 0.30 | 0.45 | V | $V_{CC}$ = Min, $I_{OL}$ = 16 mA | |
| $V_{OH}$ | Output HIGH Voltage (93459 only) | 2.4 | | | V | $V_{CC}$ = Min, $I_{OH}$ = −2.0 mA | |
| $I_{IL}$ | Input LOW Current | | −160 | −250 | μA | $V_{CC}$ = Max, $V_{IL}$ = 0.45 V | |
| $I_{IH}$ | Input HIGH Current | | | 40 | μA | $V_{CC}$ = Max, $V_{IH}$ = 2.4 V | |
| $I_{OHZ}$ | Output Leakage Current for High Impedance State (93459 only) | | | 50<br>−50 | μA | $V_{OH}$ = 2.4 V<br>$V_{OL}$ = 0.4 V | 0°C to +75°C |
| $I_{OHZ}$ | Output Leakage Current for High Impedance State (93459 only) | | | 100<br>−100 | μA | $V_{OH}$ = 2.4 V<br>$V_{OL}$ = 0.4 V | −55°C to +125°C |
| $I_{CEX}$ | Output Leakage Current (93458 only) | | | 50 | μA | $V_{CC}$ = 5.25 V, $V_{CEX}$ = 4.95 V, −0°C to +75°C Chip Deselected | |
| $I_{CEX}$ | Output Leakage Current (93458 only) | | | 150 | μA | $V_{CC}$ = 5.5 V, $V_{CEX}$ = 5.2 V, −55°C to +125°C Chip Deselected | |
| $I_{OS}$ | Output Short-Circuit Current (93459 only) | −15 | −35 | −90 | mA | $V_{CC}$ = Max, $V_O$ = 0 V, Note 2 | |
| $I_{CC}$ | Power Supply Current | | 105 | 170 | mA | $V_{CC}$ = Max, Chip Selected, Note 3 | |
| $C_{IN}$ | Input Pin Capacitance | | 4.0 | | pF | $V_{CC}$ = 5.0 V, $V_{IN}$ = 4.0 V, f = 1.0 MHz | |
| $C_O$ | Output Pin Capacitance | | 7.0 | | pF | $V_{CC}$ 5.0 = V, $V_O$ = 4.0 V, f = 1.0 MHz | |

**Commercial**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 5%, GND = 0 V, $T_A$ = 0°C to +75°C

| Symbol | Characteristic | Max | Unit | Condition |
|---|---|---|---|---|
| $t_{AA}$ | Address to Output Access Time | 45 | ns | See AC Output Load |
| $t_{ACS}$ | Chip Select to Output Access Time | 30 | ns | See AC Output Load |

**Military**

**AC Characteristics:** $V_{CC}$ = 5.0 V ± 10%, GND = 0 V, $T_A$ = 55°C to +125°C

| Symbol | Characteristic | Max | Unit | Condition |
|---|---|---|---|---|
| $t_{AA}$ | Address to Output Access Time | 65 | ns | See AC Test Output Load |
| $t_{ACS}$ | Chip Select to Output Access Time | 30 | ns | See AC Test Output Load |

1. Typical values are at $V_{CC}$ = 5.0 V, $T_A$ = +25°C and maximum loading.
2. Not more than one output to be shorted at a time. Duration of the short circuit should not exceed one second.
3. For programmed part, add 0.45 mA typical, 0.60 mA maximum per selected programmed product terms and add 2.9 mA typical, 3.9 mA maximum per enabled low output or 33 mA typical, 44 mA maximum for disabled states.

**Fig. 1 AC Test Loads**

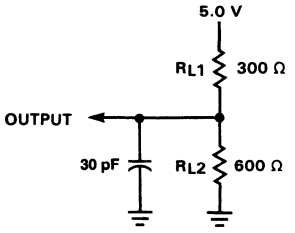



**Fig. 3 Read Mode Timing**

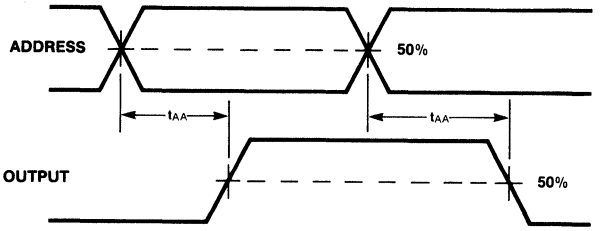
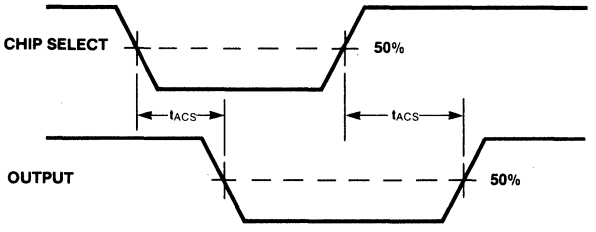
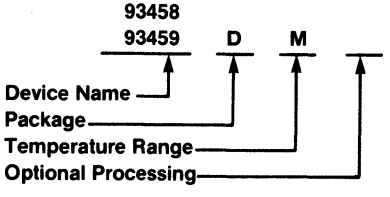



**Fig. 2 Input Levels**




8

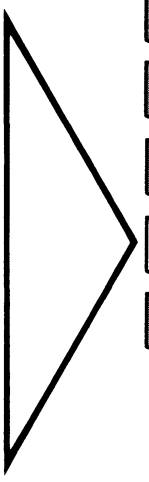
## Ordering Information



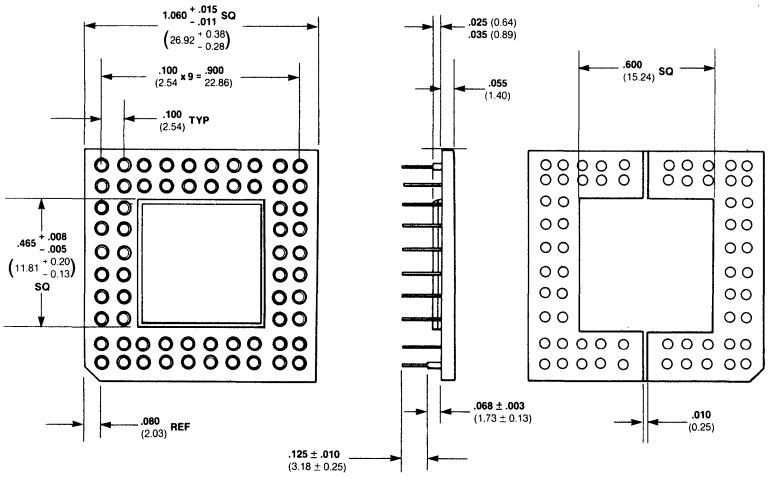

**Packages**
- D = Ceramic DIP
- F = Flatpak
- L = Leadless Chip Carrier
- P = Plastic DIP

**Temperature Ranges**
- C = 0°C to +75°C
- M = −55°C to +125°C

**Optional Processing**
- QB = Mil Std 883 Method 5004 & 5005, Level B
- QC = Mil Std 883 Method 5004 & 5005, Level C
- QR = Commercial Device with 160 Hour Burn In

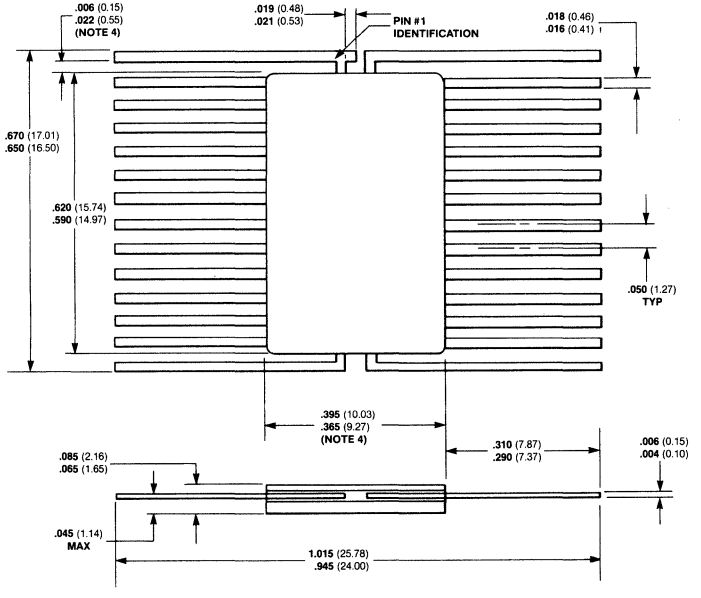


## 1F 64-Pin Plug In Package




**Notes**
Body is 92% min. alumina
Lid is nickel/gold-plated kovar or equivalent
Assembled weight is 4.7 grams

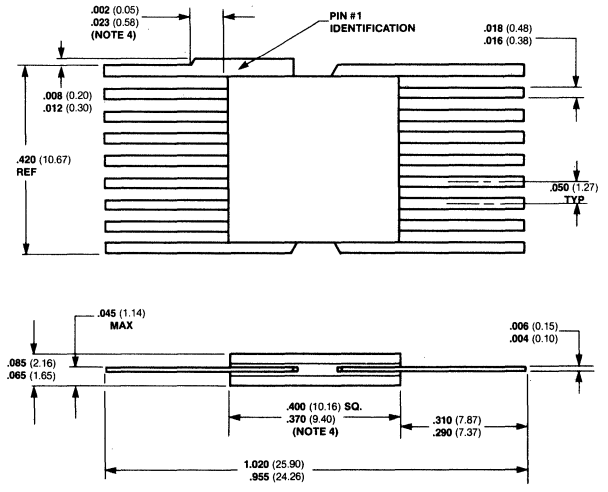
## 2E 28-Pin Cerpak




**Notes**
Pins are tin-plated alloy 42 or equivalent
Base and cap are black alumina
Package weight is 1.0 grams
These dimensions include misalignment, glass over-run etc. . . .

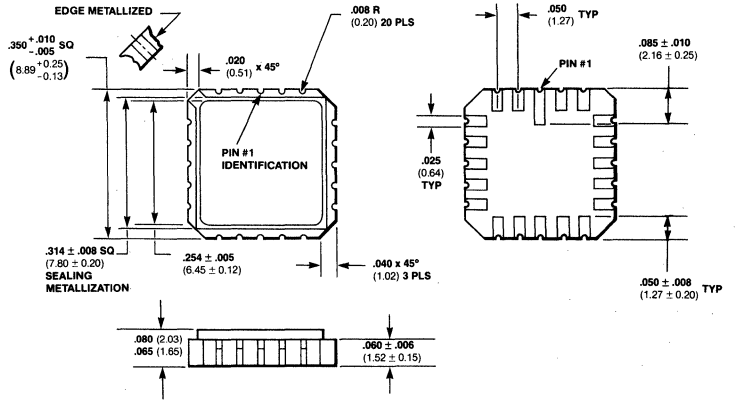
9

## 2F 18-Pin Cerpak



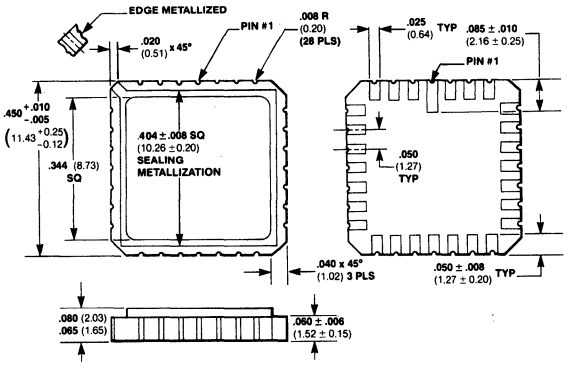

**Notes**
Pins are tin-plated alloy 42 or equivalent
Base and cap are black alumina
Package weight is 0.7 grams
These dimensions include misalignment, glass over-run etc. . . .

## 2H 20-Pin Leadless Chip Carrier



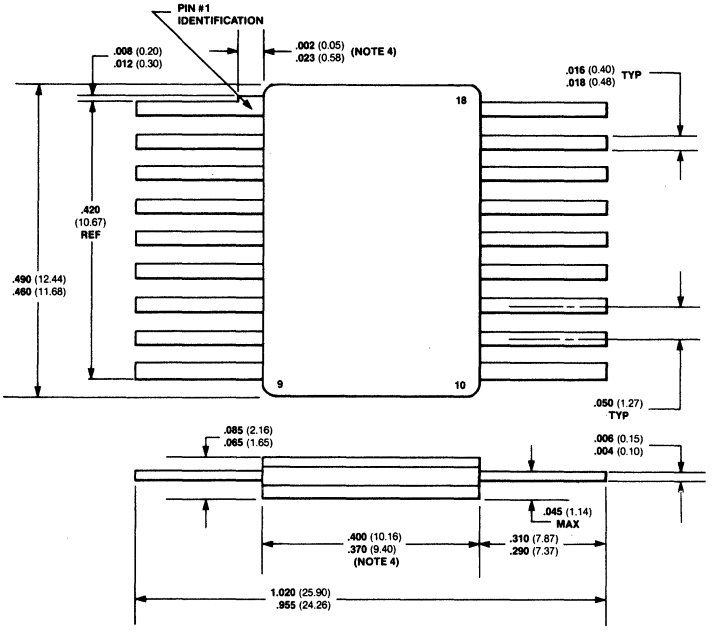

**Notes**
Chip carrier is 92% min. black alumina
Cap is nickel/gold-plated kovar or equivalent
All edge notches (except corners) are gold-plated to connect to bottom gold lead plating
Package weight is 2.5 grams

## 2J 28-Pin Leadless Chip Carrier




**Notes**
Chip carrier is 92% min. black alumina
Cap is nickel/gold-plated kovar or equivalent
All edge notches (except corners) are gold-plated to connect to bottom gold lead plating
Package weight is 2.7 grams

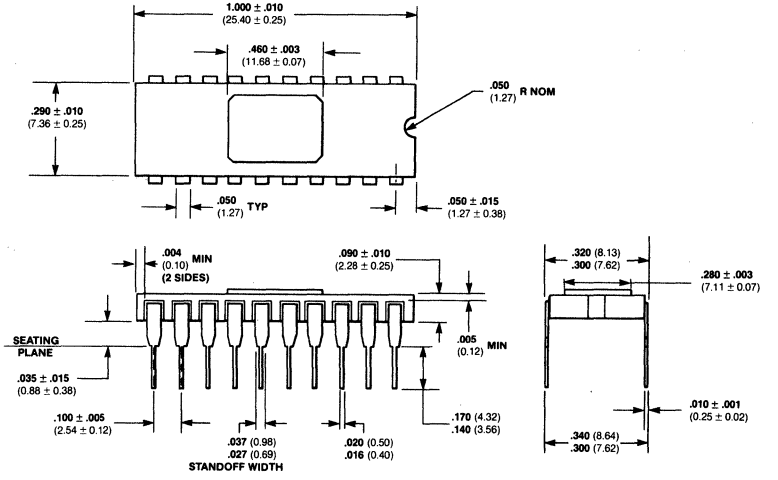
## 3E 18-Pin Lead Cerpak




**Notes**
Pins are tin-plated alloy 42 or equivalent
Base and cap are black alumina
Package weight is 0.9 grams
These dimensions include misalignment, glass over-run etc. . . .

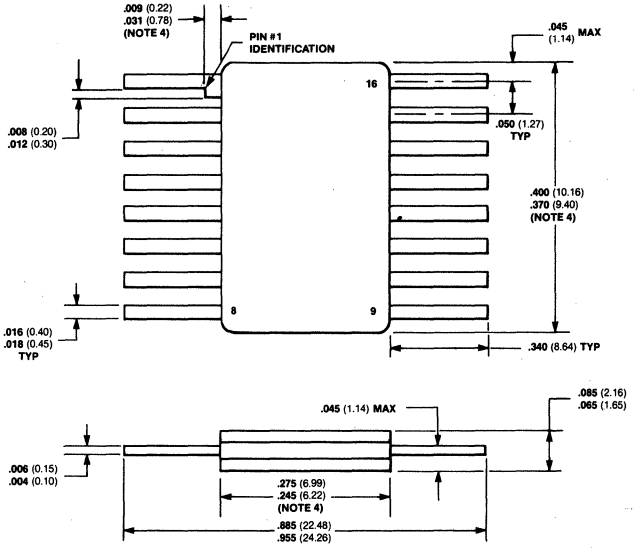
9

## 3G 20-Pin Side-Brazed Package



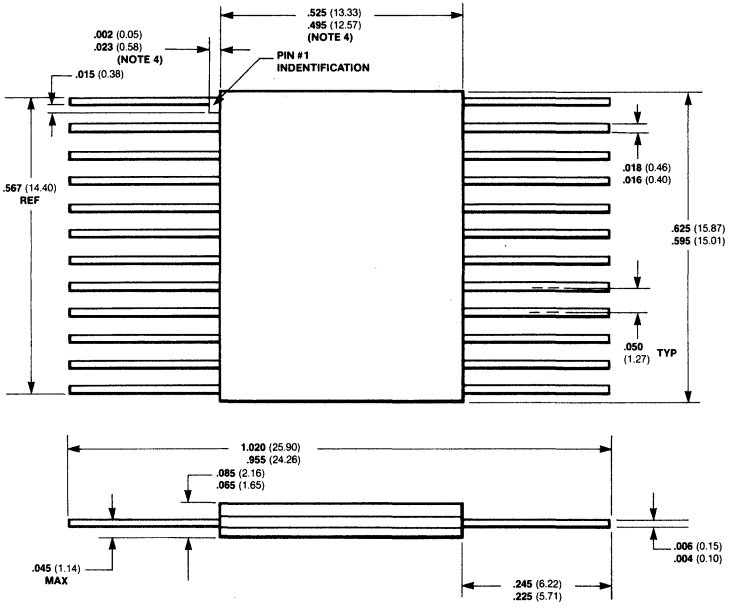

**Notes**
Pins are nickel/gold-plated alloy 42 or equivalent
Package material is alumina, 92% min.
Cap is Ni/Au-plated kovar or equivalent
Board-drilling dimensions should equal your practice for **.030** (0.76) dia holes
Pins are intended for insertion in hole rows on **.300** (7.62) centers
Pins are purposely shipped with "positive" misalignment to facilitate insertion
Package weight is 1.8 grams

## 3L 16-Pin Cerpak



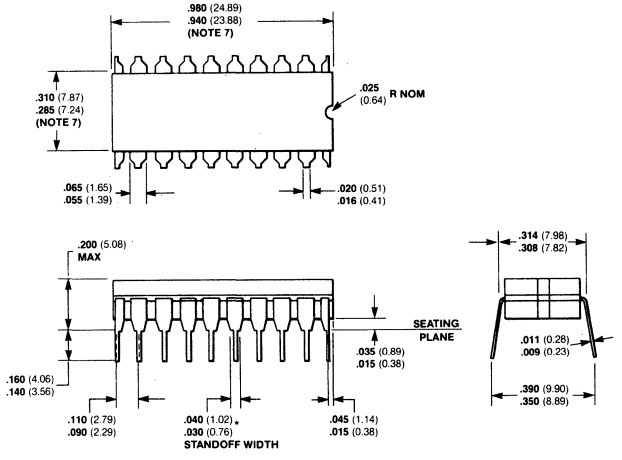

**Notes**
Pins are tin-plated alloy 42 or equivalent
Base and cap are black alumina
Package weight is 0.5 grams
These dimensions include misalignment, glass over-run etc. . . .

## 3M 24-pin Cerpak




**Notes**
Pins are tin-plated alloy 42 or equivalent
Base and cap are black aiumina
Package weight is 1.0 gram
These dimensions include misalignment, glass over-run etc. . . .

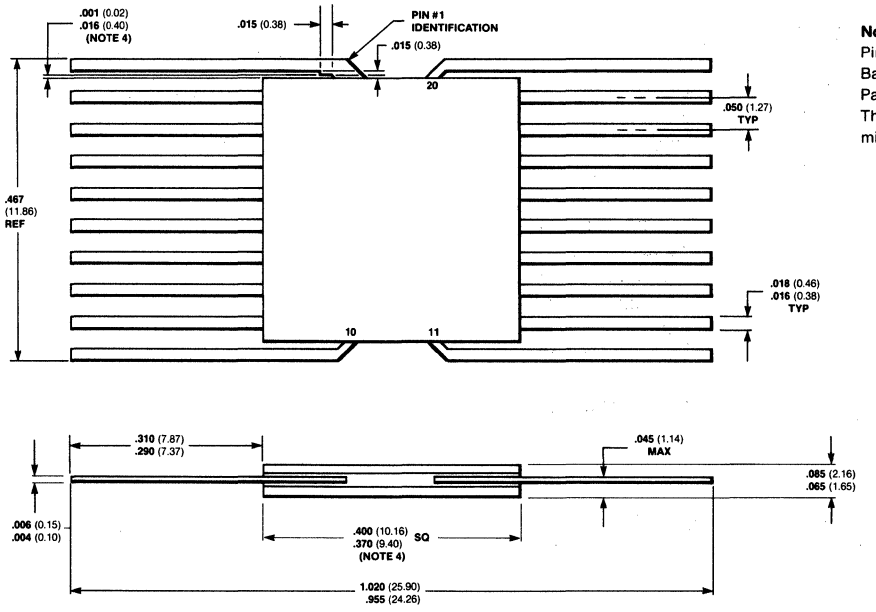
## 4E 20-Pin Package, Cerdip




**Notes**
Pins are tin-plated alloy 42 or equivalent
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.030** (0.76) inch diameter holes
Hermetically sealed alumina package
Package weight is 2.9 grams
These dimensions include misalignment, glass over-run etc. . . .
* The **.040-.030** dimension does not apply to the corner pins

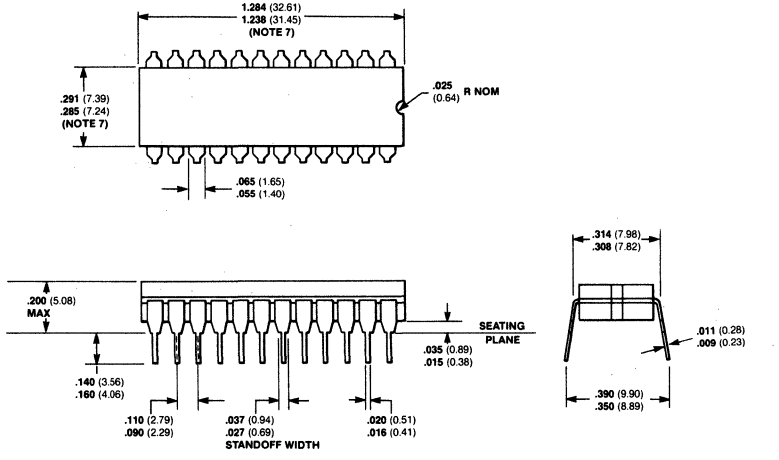
9

## 4F 20-Pin Cerpak



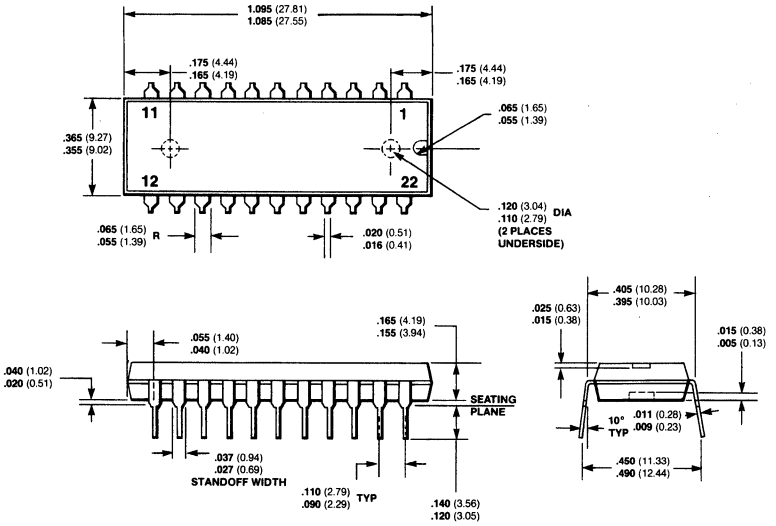

**Notes**
Pins are tin-plated alloy 42 or equivalent
Base and cap are black alumina
Package weight is 0.8 grams
These dimensions include misalignment, glass over-run etc. . . .

## 4H 24-Pin Cerdip Package



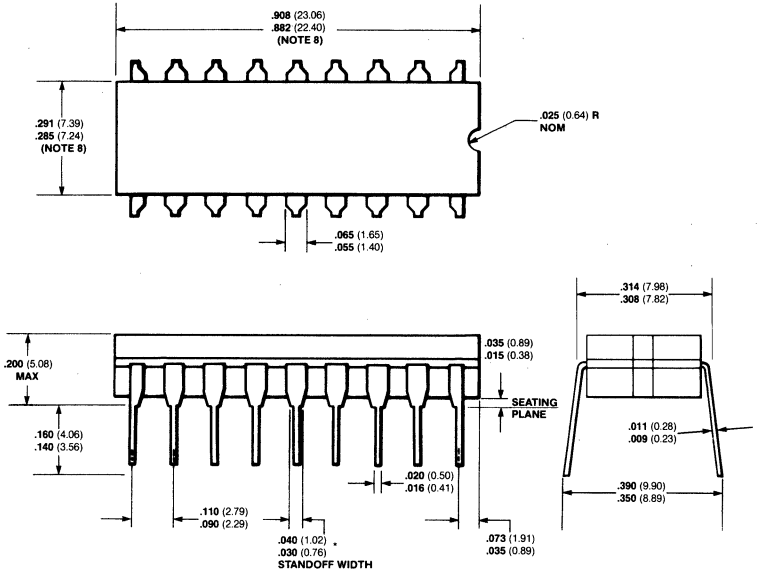

**Notes**
Pins are tin-plated alloy 42 or equivalent
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.030** (0.76) inch diameter pins
Hermetically sealed alumina package
Package weight is 6.7 grams
These dimensions include misalignment, glass over-run etc. . . .

## 4K/4K-L 22-Pin Plastic Dip




**Notes**
Pins are tin-plated alloy 42 or equivalent
Package material is plastic
Pins are intended for insertion in hole rows on **.400** (10.16) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Package weight is 2.1 grams
Package dimensions do not include permissible flash

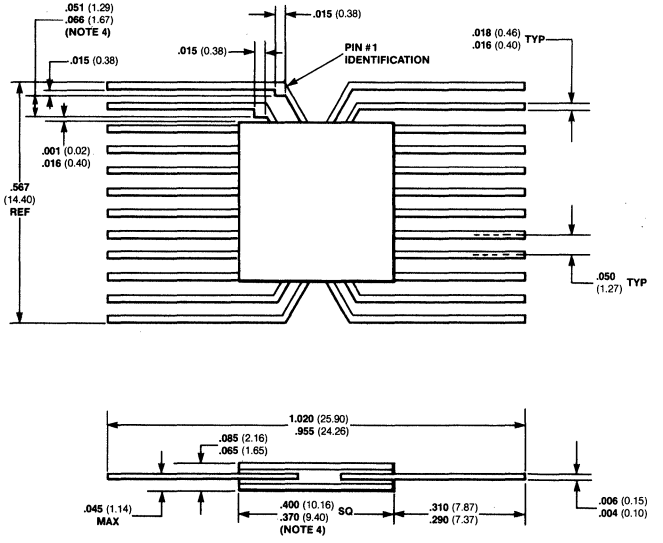
## 4N/8F 18-Pin Package, Cerdip




**Notes**
Pins are tin-plated alloy 42 or equivalent
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.030** (0.76) inch diameter holes
Hermetically sealed alumina package
*Does not apply to the corner leads
Package weight is 2.7 grams
These dimensions include misalignment, glass over-run etc. . . .

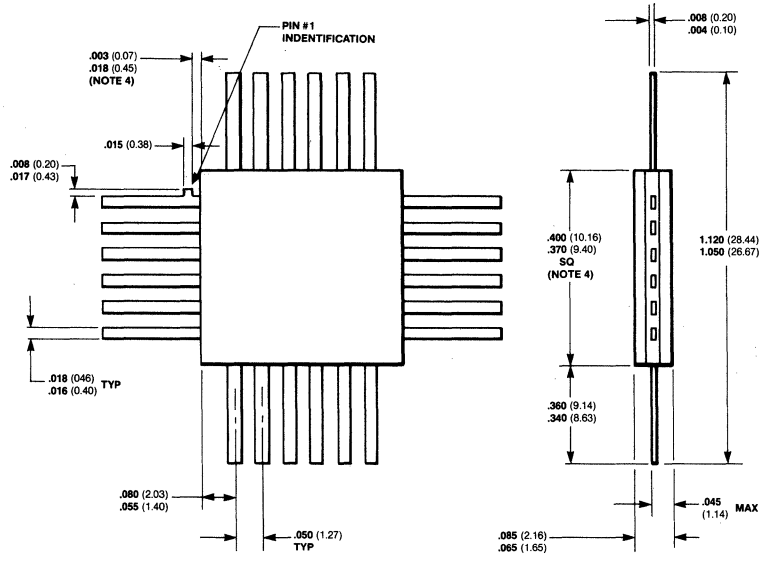
9

## 4P 24-Pin Cerpak



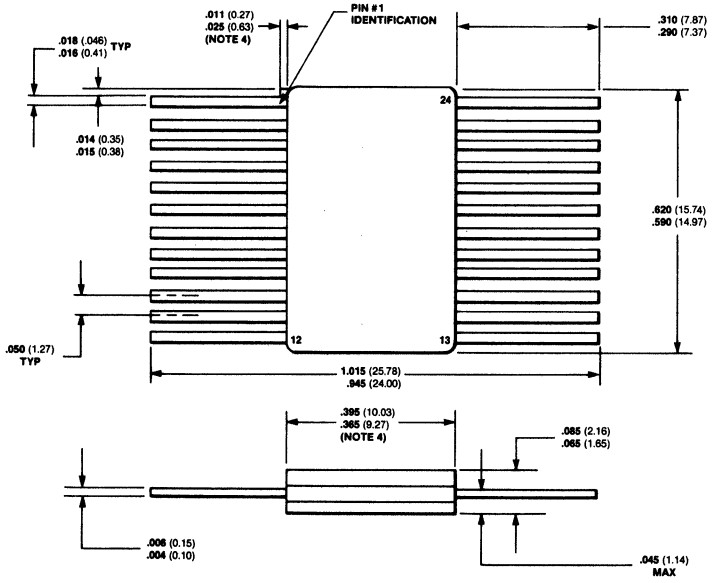

**Notes**
Pins are tin-plated alloy 42 or equivalent
Base and cap are black alumina
Package weight is 0.8 grams
These dimensions include misalignment, glass over-run etc. . . .

## 4V 24-Pin Quad Cerpak



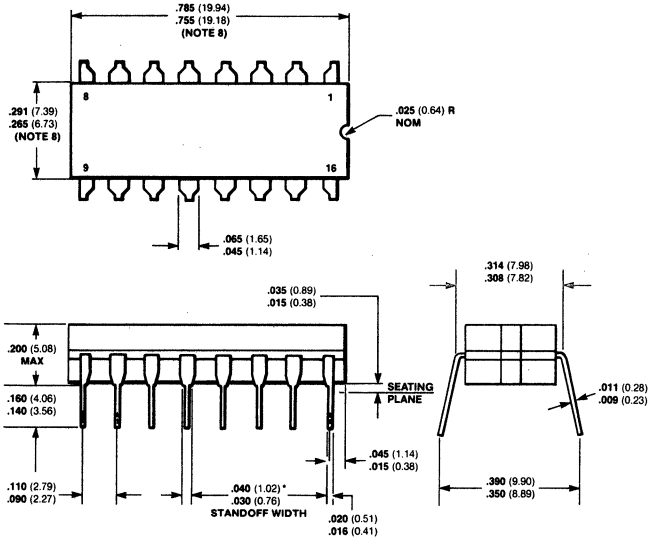

**Notes**
Pins are tin-plated alloy 42 or equivalent
Cavity size is **.200 SQ.** (5.08 SQ.)
Package weight is 0.7 grams
These dimensions include misalignment, glass over-run etc. . . .

## 4X 24-Pin Cerpak




**Notes**
Pins are tin-plated alloy 42 or equivalent
Base and cap are black alumina
Package weight is 1.0 gram
These dimensions include misalignment, glass over-run etc. . . .

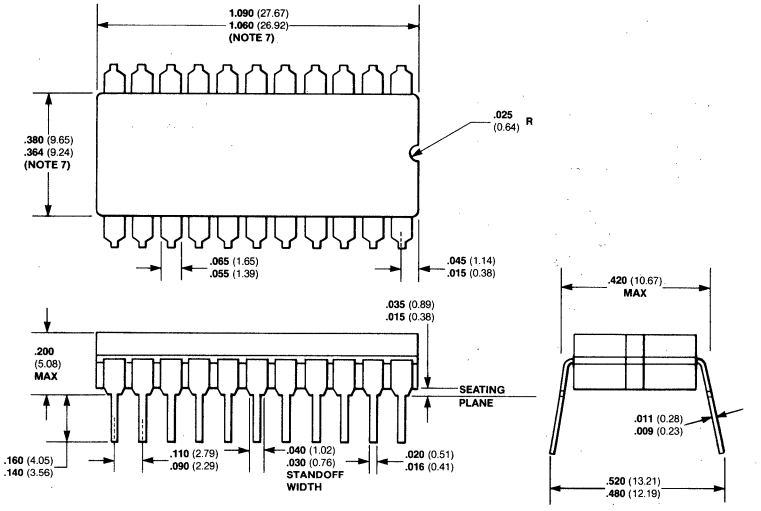
## 6D 16-Pin Package, Cerdip




**Notes**
Pins are tin-plated alloy 42 or equivalent
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.030** (0.76) inch dia holes
Hermetically sealed alumina package
The **.040-.030** dimension does not apply to the corner pins
Package weight is 2.2 grams
These dimensions include misalignment, glass over-run etc. . . .

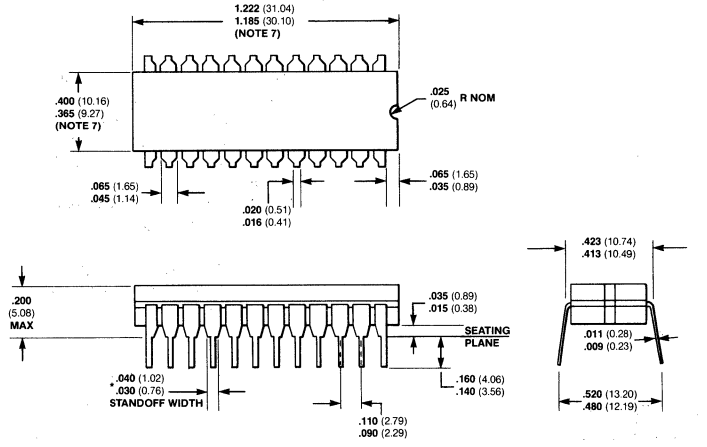
9

## 6S 22-Pin Package, Cerdip



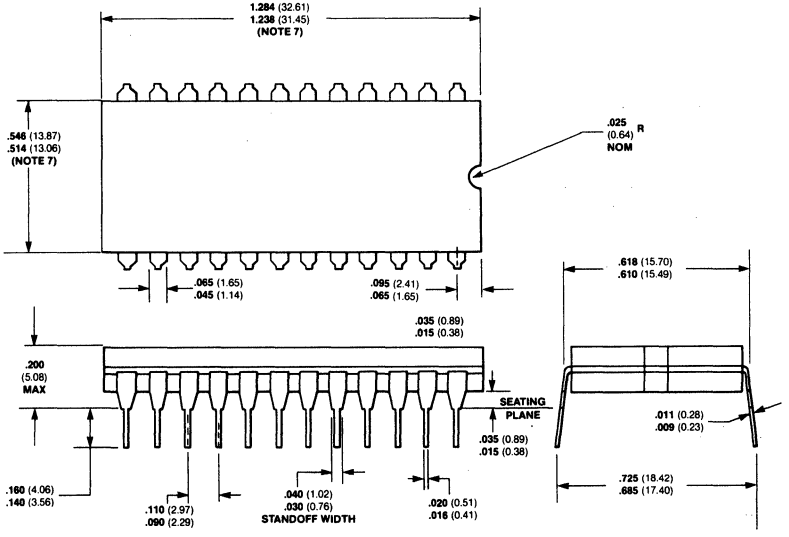

**Notes**
Pins are tin-plated alloy 42 or equivalent
Hermetically sealed alumina package
Pins are intended for insertion in hole rows on **.400** (10.16) centers
They are purposely shipped "positive" misalignment to facilitate insertion
Package weight is 2.2 grams
Board-drilling dimensions should equal your practice for **.030** (0.76) inch diameter holes
These dimensions include misalignment, glass over-run etc. . . .

## 6Y 24-Pin Package, Cerdip



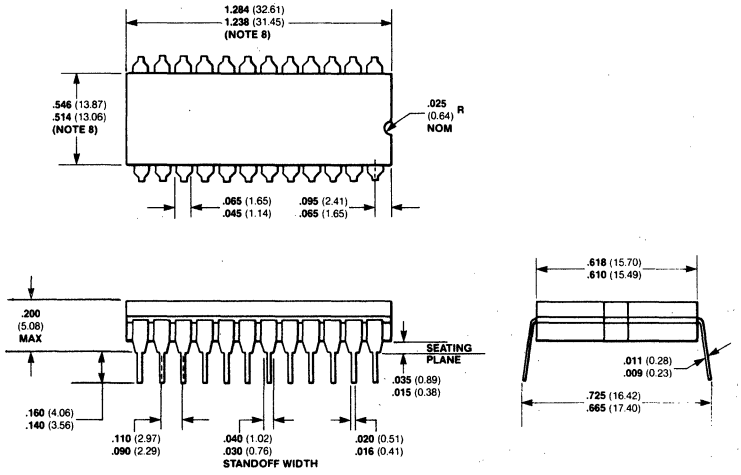

**Notes**
Pins are tin-plated alloy 42 or equivalent
Hermetically sealed alumina package
Pins are intended for insertion in hole rows on **.400** (10.16) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Package weight is 6.0 grams
Board-drilling dimensions should equal your practice for **.030** (0.76) inch diameter holes
These dimensions include misalignment, glass over-run etc. . . .

## 7L 24-Pin Package, Cerdip




**Notes**
Pins are tin-plated alloy 42 or equivalent
Hermetically sealed alumina package
Pins are intended for insertion in hole rows on **.600** (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.030** (0.76) inch diameter holes
Package weight is 7.1 grams
These dimensions include misalignment, glass over-run etc. . . .

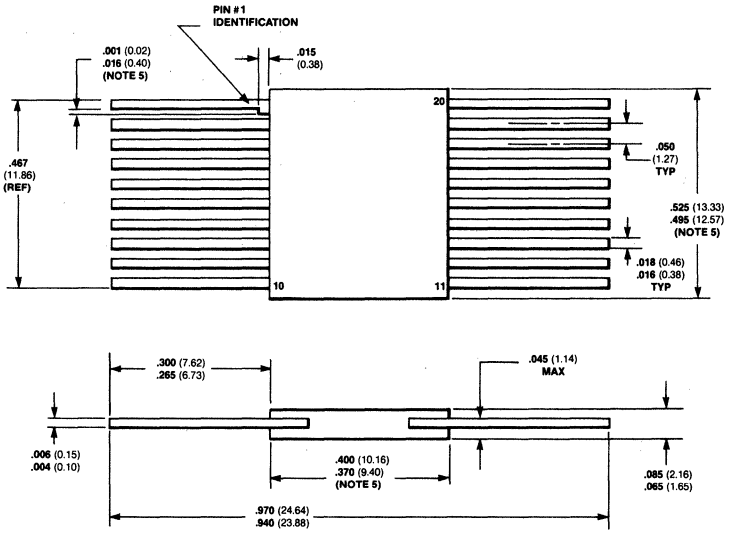
## 7W 24-Pin MSI Dual In-line, Cerdip




**Notes**
Pins are tin-plated alloy 42 or equivalent
Hermetically sealed alumina package
Pins are intended for insertion in hole rows on **.600** (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.030** (0.76) inch diameter holes
Cavity size is **.320 x .320** (8.13 x 8.13)
Package weight is 7.1 grams
These dimensions include misalignment, glass over-run etc. . . .

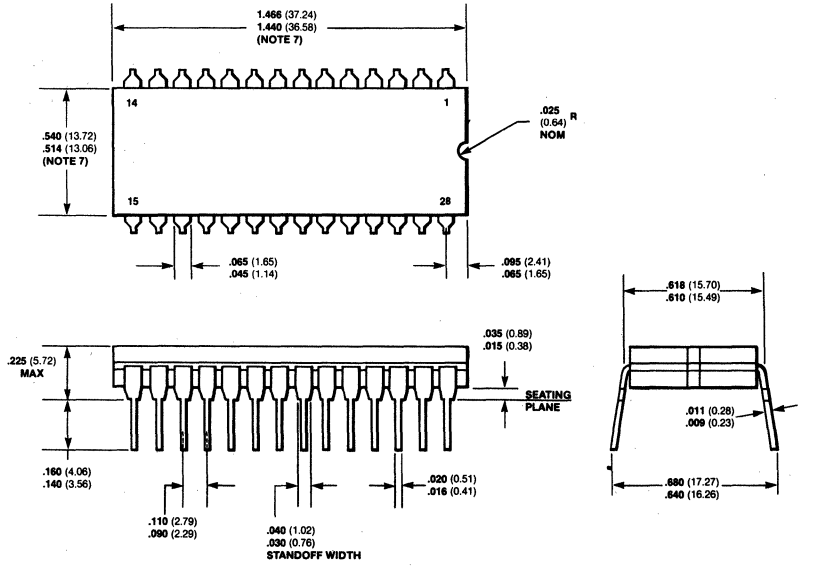
9

## 8H 20-Pin Cerpak



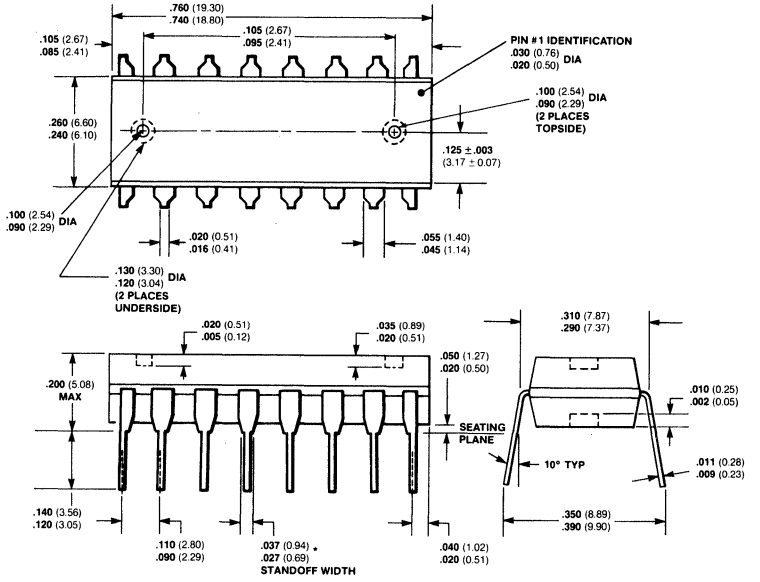

**Notes**
Pins are tin-plated alloy 42 or equivalent
Base and cap are black alumina
Cavity size is **.300 x .375** (7.62 x 9.52)
Package weight is 1.0 gram
These dimensions include misalignment, glass over-run etc. . . .

## 8S 28-Pin Package, Cerdip



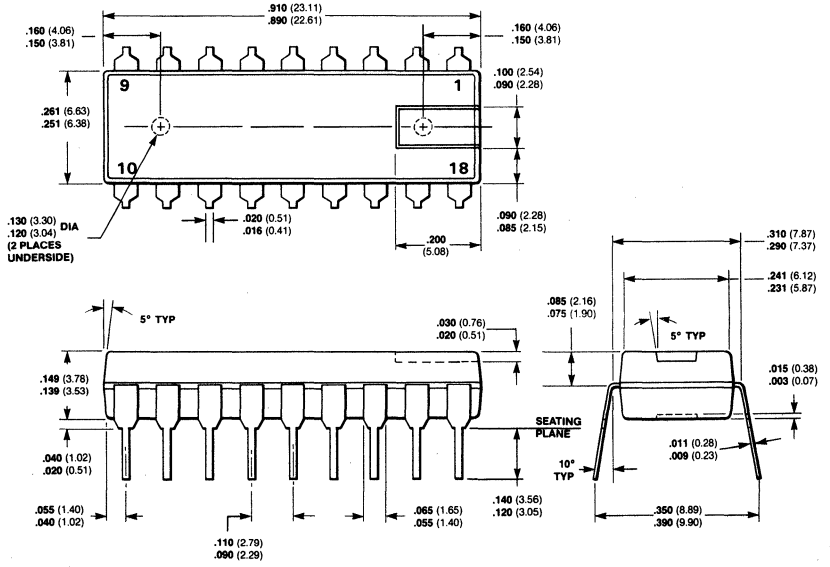

**Notes**
Pins are tin-plated alloy 42 or equivalent
Hermetically sealed alumina package
Pins are intended for insertion in hole rows on **.600** (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.030** (0.76) inch diameter holes
Package weight is 8.6 grams
These dimensions include misalignment, glass over-run etc. . . .

## 9B 16-Pin Plastic Dip



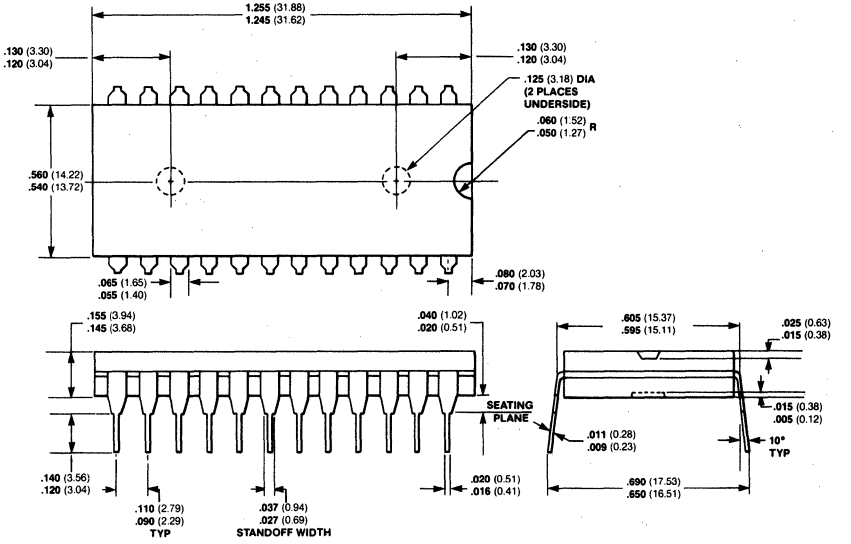

**Notes**
Pins are tin-plated alloy 42 or equivalent
Package material is plastic
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
*The **.037-.027** dimension does not apply to the corner pins
Package weight is 1.0 gram
Package dimensions do not include permissible flash

## 9M/9M-L 18-Pin Plastic Dip



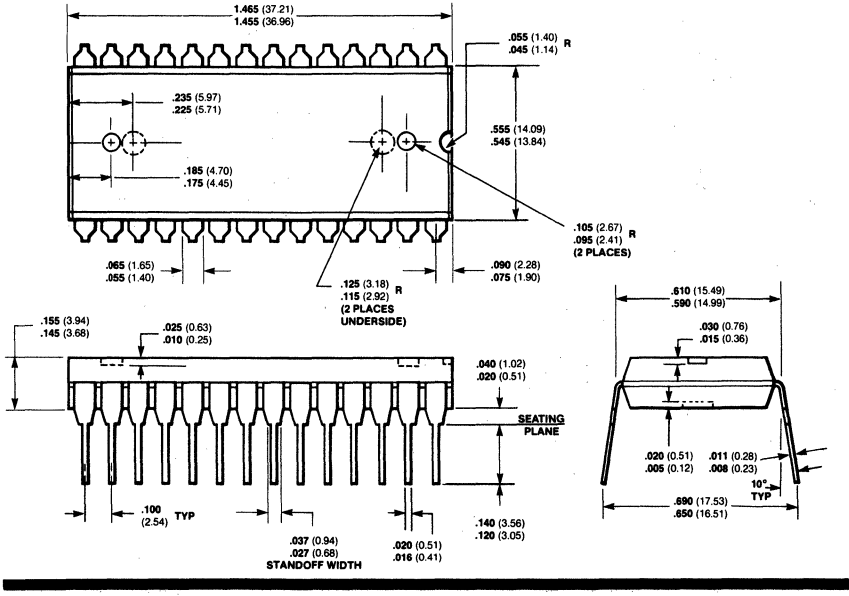

**Notes**
Pins are tin-plated alloy 42 or equivalent
Package material is plastic
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Package weight is 1.3 grams
Package dimensions do not include permissible flash

## 9N/9N-L 24-Pin Plastic Dip

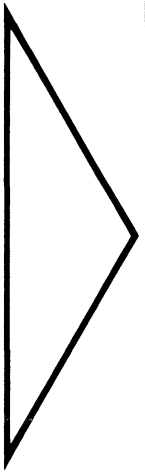



**Notes**
Pins are tin-plated alloy 42 or equivalent
Package material is plastic
Pins are intended for insertion in hole rows on **.600** (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Package weight is 3.5 grams
Package dimensions do not include permissible flash

## 9Y 28-Pin Plastic Dip




**Notes**
Pins are tin-plated alloy 42 or equivalent
Package material is plastic
Pins are intended for insertion in hole rows on **.600** (15.24) centers
They are purposely shipped "positive" misalignment to facilitate insertion
Package weight is 4.5 grams
Package dimensions do not include permissible flash



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Costa Mesa, California 92626
Tel: 714-641-1850 TWX: 910-595-2638

Hamilton Electro Sales
10912 West Washington Blvd.
Culver City, California 90230
Tel: 213-558-2121 TWX: 910-340-6364

Hamilton/Avnet Electronics
4103 North Gate Blvd.
Sacramento, California 95348
Tel: 916-920-3150

Hamilton/Avnet Electronics
4545 Viewridge Avenue
San Diego, California 92123
Tel: 714-571-7527 TWX: 910-335-1216

Hamilton/Avnet Electronics
1175 Bordeaux Drive
Sunnyvale, California 94086
Tel: 408-743-3355 TWX: 910-339-9332

Schweber Electronics
17811 Gillette Avenue
Irvine, California 92714
Tel: 714-556-3880

Sertech Laboratories**
3170 Pullman Dr.
Costa Mesa, California 92626
Tel: 714-754-0666

Wyle Distribution Group
124 Maryland Street
El Segundo, California 90245
Tel: 213-322-8100 TWX: 910-348-7140

Wyle Distribution Group
17872 Cowan Avenue
Irvine, California 92714
Tel: 714-641-1600 Telex: 910-595-1572

Wyle Distribution Group
Military Product Division
18910 Teller Avenue
Irvine, California 92715
Tel: 714-851-9953

Wyle Distribution Group
9525 Chesapeake
San Diego, California 92123
Tel: 714-565-9171 TWX: 910-335-1590

Wyle Distribution Group
3000 Bowers Avenue
Santa Clara, California 95051
Tel: 408-727-2500 TWX: 910-338-0541

Zeus Components, Inc.
1130 Hawk Circle
Anaheim, California 92807
Tel: 714-632-6880

Zeus Components, Inc.
3350 Scott Blvd., Bldg. 6402
Santa Clara, California 95051
Tel: 408-727-0714 TWX: 910-338-2121

**Colorado**
Arrow Electronics
1390 S. Potomac Street, Suite 136
Aurora, Colorado 80012
Tel: 303-696-1111

Bell Industries
8155 West 48th Avenue
Wheatridge, Colorado 80033
Tel: 303-424-1985 TWX: 910-938-0393

Hamilton/Avnet Electronics
8765 E. Orchard Rd., Suite 708
Englewood, Colorado 80111
Tel: 303-740-1000 TWX: 910-935-0787

Wyle Distribution Group
451 East 124th Avenue
Thornton, Colorado 80241
Tel: 303-457-9953 TWX: 910-936-0770

**Connecticut**
Arrow Electronics
12 Beaumont Road
Wallingford, Connecticut 06492
Tel: 203-265-7741 TWX: 710-476-0162

Hamilton/Avnet Electronics
Commerce Drive, Commerce Park
Danbury, Connecticut 06810
Tel: 203-797-2800 TWX: 710-546-9974

Schweber Electronics
Finance Drive
Commerce Industrial Park
Danbury, Connecticut 06810
Tel: 203-792-3500 TWX: 710-456-9405

**Florida**
Arrow Electronics
1001 Northwest 62nd Street
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Ft. Lauderdale, Florida 33309
Tel: 305-776-7790 TWX: 510-955-9456

Arrow Electronics
50 Woodlake Drive West
Building B
Palm Bay, Florida 32905
Tel: 305-725-1480 TWX: 510-959-6337

Chip Supply**
1607 Forsyth Road
Orlando, Florida 32807
Tel: 305-275-3810

Hall Mark Electronics
1671 West McNab Road
Ft. Lauderdale, Florida 33309
Tel: 305-971-9280 TWX: 510-956-3092

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# Fairchild Semiconductor Franchised Distributors United States and Canada

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7233 Lake Ellenor Drive
Orlando, Florida 32809
Tel: 305-855-4020 TWX: 810-850-0183

Hamilton/Avnet Electronics
6801 N.W. 15th Way
Ft. Lauderdale, Florida 33309
Tel: 305-971-2900 TWX: 510-956-3097

Hamilton/Avnet Electronics
3197 Tech Drive, North
St. Petersburg, Florida 33702
Tel: 813-576-3930 TWX: 810-863-0374

Schweber Electronics
181 Whooping Loop
Altamonte Springs, Florida 32701
Tel: 305-331-7555

Schweber Electronics
2830 North 28th Terrace
Hollywood, Florida 33020
Tel: 305-927-0511 TWX: 510-954-0304

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Arrow Electronics
2979 Pacific Drive
Norcross, Georgia 30071
Tel: 404-449-8252 TWX: 810-766-0439

Hall Mark Electronics
6410 Atlantic Blvd., Suite 115
Norcross, Georgia 30071
Tel: 404-447-8000 TWX: 810-766-4510

Hamilton/Avnet Electronics
5825-D Peachtree Corners East
Norcross, Georgia 30092
Tel: 404-447-7500 TWX: 810-766-0432

Schweber Electronics
303 Research Drive
Norcross, Georgia 30092
Tel: 404-449-9170

**Illinois**
Arrow Electronics
2000 Algonquin Road
Schaumburg, Illinois 60195
Tel: 312-397-3440 TWX: 910-291-3544

Hall Mark Electronics
1177 Industrial Drive
Bensenville, Illinois 60106
Tel: 312-860-3800 TWX: 910-651-0185

Hamilton/Avnet Electronics
1130 Thorndale Avenue
Bensenville, Illinois 60106
Tel: 312-860-7780 TWX: 910-227-0060

Kierulff Electronics
1536 Landmeier Road
Elk Grove Village, Illinois 60007
Tel: 312-640-0200 TWX: 910-227-3166

Schweber Electronics
904 Cambridge Avenue
Elk Grove Village, Illinois 60007
Tel: 312-364-3750 TWX: 910-222-3453

**Indiana**
Arrow Electronics
2718 Rand Road
Indianapolis, Indiana 46241
Tel: 317-243-9353 TWX: 810-341-3119

Graham Electronics Supply, Inc.
133 S. Pennsylvania Street
Indianapolis, Indiana 46204
Tel: 317-634-8202 TWX: 810-341-3481

Hamilton/Avnet Electronics
485 Gradle Drive
Carmel, Indiana 46032
Tel: 317-844-9333 TWX: 810-260-3966

Pioneer Electronics
6408 Castle Place Drive
Indianapolis, Indiana 46250
Tel: 317-849-7300 TWX: 810-260-1794

**Iowa**
Arrow Electronics
1930 St. Andrews N.E.
Cedar Rapids, Iowa 52402
Tel: 319-395-7230

Schweber Electronics
5270 N. Park Place N.E.
Cedar Rapids, Iowa 52402
Tel: 319-373-1417

**Kansas**
Hall Mark Electronics
10815 Lakeview Drive
Lenexa, Kansas 66215
Tel: 913-888-4747 TWX: 910-749-6620

Hamilton/Avnet Electronics
9219 Quivira Road
Overland Park, Kansas 66215
Tel: 913-888-8900 TWX: 910-743-0005

Schweber Electronics
10300 W. 103rd St., Suite 103
Overland Park, Kansas 66214
Tel: 913-492-2921

**Maryland**
Arrow Electronics
4801 Benson Avenue
Baltimore, Maryland 21227
Tel: 301-247-5200 TWX: 710-236-9005

Hall Mark Electronics
6655 Amberton Drive
Baltimore, Maryland 21227
Tel: 301-796-9300 TWX: 710-862-1942

Hamilton/Avnet Electronics
6822 Oak Hall Lane
Columbia, Maryland 21045
Tel: 301-995-3500 TWX: 710-862-1861

Schweber Electronics
9218 Gaither Road
Gaithersburg, Maryland 20760
Tel: 301-840-5900 TWX: 710-828-9749

**Massachusetts**
Arrow Electronics
One Arrow Drive
Woburn, Massachusetts 01801
Tel: 617-933-8130 TWX: 710-392-6770

Gerber Electronics
128 Carnegie Row
Norwood, Massachusetts 02062
Tel: 617-329-2400 TWX: 710-336-1987

Hamilton/Avnet Electronics
50 Tower Office Park
Woburn, Massachusetts 01801
Tel: 617-273-7500 TWX: 710-393-0382

Schweber Electronics
25 Wiggins Avenue
Bedford, Massachusetts 01730
Tel: 617-275-5100 TWX: 710-326-0268

Sertech Laboratories**
1 Peabody Street
Salem, Massachusetts 01970
Tel: 617-745-2450 TWX: 710-347-0223

Zeus Components, Inc.
25 Adams Street
Burlington, Massachusetts 01803
Tel: 617-273-0750 TWX: 710-332-0716

**Michigan**
Arrow Electronics
3810 Varsity Drive
Ann Arbor, Michigan 48104
Tel: 313-971-8220 TWX: 810-223-6020

Arrow Electronics
3510 Roger B. Chafee, S.E.
Grand Rapids, Michigan 49508
Tel: 616-243-0912

Hamilton/Avnet Electronics
2215 29th Street S.E., Space A5
Grand Rapids, Michigan 49508
Tel: 616-243-8805 TWX: 810-273-6921

Hamilton/Avnet Electronics
32487 Schoolcraft
Livonia, Michigan 48150
Tel: 313-522-4700 TWX: 810-242-8775

Pioneer Electronics
13485 Stamford
Livonia, Michigan 48150
Tel: 313-525-1800 TWX: 810-242-3271

Schweber Electronics
12060 Hubbard Avenue
Livonia, Michigan 48150
Tel: 313-525-8100 TWX: 810-242-2983

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Arrow Electronics
5230 West 73rd Street
Edina, Minnesota 55435
Tel: 612-830-1800 TWX: 910-576-3125

Hall Mark Electronics
7838 12th Avenue South
Bloomington, Minnesota 55420
Tel: 612-854-3233

Hamilton/Avnet Electronics
10300 Bren Road East
Minnetonka, Minnesota 55343
Tel: 612-932-0600 TWX: 910-576-2720

Schweber Electronics
7422 Washington Avenue S.
Eden Prairie, Minnesota 55344
Tel: 612-941-5280 TWX: 910-576-3167

**Missouri**
Arrow Electronics
2380 Schuetz Road
St. Louis, Missouri 63141
Tel: 314-567-6888 TWX: 910-764-0882

Hall Mark Electronics
2662 Metro Blvd.
Maryland Heights, Missouri 63043
Tel: 314-291-5350 Telex: 910-762-0672

Hamilton/Avnet Electronics
13743 Shoreline Court, East
Earth City, Missouri 63045
Tel: 314-344-1200 TWX: 910-762-0684

Schweber Electronics
502 Earth City Expressway
Earth City, Missouri 63045
Tel: 314-739-0526

**New Hampshire**
Arrow Electronics
1 Perimeter Road
Manchester, New Hampshire 03103
Tel: 603-668-6968 TWX: 710-220-1684

Schweber Electronics
Bedford Farms Building 2
Kilton and South River Roads
Manchester, New Hampshire 03102
Tel: 603-625-2250

**New Jersey**
Arrow Electronics
Pleasant Valley Avenue
Moorestown, New Jersey 08057
Tel: 609-235-1900 TWX: 710-897-0829

Arrow Electronics
2 Industrial Road
Fairfield, New Jersey 07006
Tel: 201-575-5300

Hall Mark Electronics
Springdale Business Center
2091 Springdale Road
Cherry Hill, New Jersey 08003
Tel: 609-424-0880 TWX: 710-940-0660

Hall Mark Electronics
107 Fairfield Road
Fairfield, New Jersey 07006
Tel: 201-575-4415

Hamilton/Avnet Electronics
10 Industrial Road
Fairfield, New Jersey 07006
Tel: 201-575-3390 TWX: 710-734-4388

Hamilton/Avnet Electronics
#1 Keystone Avenue
Cherry Hill, New Jersey 08003
Tel: 609-424-0100 TWX: 710-940-0262

Schweber Electronics
18 Madison Road
Fairfield, New Jersey 07006
Tel: 201-227-7880 TWX: 710-734-4305

**New Mexico**
Arrow Electronics
2460 Alamo Avenue S.E.
Albuquerque, New Mexico 87106
Tel: 505-243-4566 TWX: 910-989-1679

Bell Industries
11728 Linn Avenue N.E.
Albuquerque, New Mexico 87123
Tel: 505-292-2700 TWX: 910-989-0625

Hamilton/Avnet Electronics
2524 Baylor Drive, S.E.
Albuquerque, New Mexico 87106
Tel: 505-765-1500 TWX: 910-989-0614

**New York**
Arrow Electronics
900 Broadhollow Road
Farmingdale, New York 11735
Tel: 516-694-6800
TWX: 510-224-6155 & 510-224-6126

Arrow Electronics
20 Oser Avenue
Hauppauge, New York 11787
Tel: 516-231-1000 TWX: 510-227-6623

Arrow Electronics
P.O. Box 370
7705 Maltlage Drive
Liverpool, New York 13088
Tel: 315-652-1000 TWX: 710-545-0230

Arrow Electronics
3000 Winton Road South
Rochester, New York 14623
Tel: 716-275-0300 TWX: 510-253-4766

Hamilton/Avnet Electronics
5 Hub Drive
Melville, New York 11746
Tel: 516-454-6000 TWX: 510-224-6166

Hamilton/Avnet Electronics
333 Metro Park
Rochester, New York 14623
Tel: 716-475-9130 TWX: 510-253-5470

Hamilton/Avnet Electronics
16 Corporate Circle
E. Syracuse, New York 13057
Tel: 315-437-2642 TWX: 710-541-1560

Schweber Electronics
Jericho Turnpike
Westbury, L.I., New York 11590
Tel: 516-334-7474 TWX: 510-222-3660

Schweber Electronics
3 Town Line Circle
Rochester, New York 14623
Tel: 716-424-2222

Summit Distributors, Inc.
916 Main Street
Buffalo, New York 14202
Tel: 716-884-3450 TWX: 710-522-1692

Zeus Components, Inc.
100 Midland Avenue
Port Chester, New York 10573
Tel: 914-937-7400 TWX: 710-567-1248

**North Carolina**
Arrow Electronics
938 Burke Street
Winston Salem, North Carolina 27102
Tel: 919-725-8711 TWX: 510-931-3169

Arrow Electronics
3117 Poplarwood Court, Suite 123
Raleigh, North Carolina 27625
Tel: 919-876-3132 TWX: 510: 928-1856

Hall Mark Electronics
5237 North Blvd.
Raleigh, North Carolina 27604
Tel: 919-872-0712 TWX: 510-928-1831

Hamilton/Avnet Electronics
3510 Spring Forrest Road
Raleigh, North Carolina 27604
Tel: 919-878-0819

Schweber Electronics
5285 North Blvd.
Raleigh, North Carolina 27604
Tel: 919-876-0000

**Ohio**
Arrow Electronics
7620 McEwen Road
Centerville, Ohio 45459
Tel: 513-435-5563 TWX: 810-459-1611

Arrow Electronics
6238 Cochran Road
Solon, Ohio 44139
Tel: 216-248-3990 TWX: 810-427-9409

Hall Mark Electronics
175 Alpha Park
Highland Heights, Ohio 44143
Tel: 216-473-2907

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Hall Mark Electronics
6130 Sundbury Road, Suite B
Westerville, Ohio 43081
Tel: 614-891-4555

Hamilton/Avnet Electronics
954 Senate Drive
Dayton, Ohio 45459
Tel: 513-433-0610 TWX: 810-450-2531

Hamilton/Avnet Electronics
4588 Emery Industrial Parkway
Warrensville Heights, Ohio 44128
Tel: 216-831-3500 TWX: 810-427-9452

Pioneer Electronics
4800 E. 131st Street
Cleveland, Ohio 44105
Tel: 216-587-3600 TWX: 810-422-2211

Pioneer Electronics
4433 Interpoint Blvd.
Dayton, Ohio 45424
Tel: 513-236-9900 TWX: 810-459-1622

Schweber Electronics
23880 Commerce Park Road
Beachwood, Ohio 44122
Tel: 216-464-2970 TWX: 810-427-9441

Schweber Electronics
7865 Paragon Road
Dayton, Ohio 45459
Tel: 513-439-1800

**Oklahoma**
Arrow Electronics
4719 S. Memorial
Tulsa, Oklahoma 74145
Tel: 918-665-7700

Hall Mark Electronics
5460 S. 103rd East Avenue
Tulsa, Oklahoma 74145
Tel: 918-665-3200 TWX: 910-845-2290

Schweber Electronics
4815 S. Sheridan Road
Tulsa, Oklahoma 74145
Tel: 918-622-8000

**Oregon**
Hamilton/Avnet Electronics
6024 S.W. Jean Road
Building C, Suite 10
Lake Oswego, Oregon 97034
Tel: 503-635-8157 TWX: 910-455-8179

**Pennsylvania**
Arrow Electronics
650 Seco Road
Monroeville, Pennsylvania 15146
Tel: 412-856-7000 TWX: 710-797-3894

Pioneer Electronics
259 Kappa Drive
Pittsburgh, Pennsylvania 15238
Tel: 412-782-2300 TWX: 710-795-3122

Schweber Electronics
101 Rock Road
Horsham, Pennsylvania 19044
Tel: 215-441-0600 TWX: 510-665-6540

**Texas**
Arrow Electronics
10125 Metropolitan Drive
Austin, Texas 78758
Tel: 512-835-4180 TWX: 910-874-1348

Arrow Electronics
13715 Gamma Road
Dallas, Texas 75234
Tel: 214-386-7500 TWX: 910-860-5377

Arrow Electronics
10899 Kinghurst, Suite 100
Houstin, Texas 77099
Tel: 713-530-4700 TWX: 910-880-4439

Hall Mark Electronics
12211 Technology Blvd.
Austin, Texas 78759
Tel: 512-258-8848 TWX: 910-874-2031

Hall Mark Electronics
11333 Page Mill Drive
Dallas, Texas 75243
Tel: 214-343-5000 TWX: 910-867-4721

Hall Mark Electronics
8000 Westglen
Houston, Texas 77063
Tel: 713-781-6100 TWX: 910-881-2711

Hamilton/Avnet Electronics
2401 Rutland Drive
Austin, Texas 78758
Tel: 512-837-8911 TWX: 910-874-1319

Hamilton/Avnet Electronics
8750 Westpark
Houston, Texas 77063
Tel: 713-780-1771 TWX: 910-881-5523

Hamilton/Avnet Electronics
2111 W. Walnut Hill Lane
Irving, Texas 75062
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Schweber Electronics
111 W. Anderson Lane
Austin, Texas 78752
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Schweber Electronics
4202 Beltway Drive
Dallas, Texas 75234
Tel: 214-661-5010 TWX: 910-860-5493

Schweber Electronics
10625 Richmond, Suite 100
Houston, Texas 77042
Tel: 713-784-3600 TWX: 910-881-4836

Sterling Electronics
23358 Kramer Lane
Austin, Texas 78758
Tel: 512-836-1341

Sterling Electronics
11090 Stemmons Freeway
Dallas, Texas 75229

Sterling Electronics
4201 Southwest Freeway
Houston, Texas 77027
Tel: 713-627-9800 TWX: 910-881-5042
Telex: STELECO HOUA 77-5299

Zeus Components, Inc.
14001 Goldmark, Suite 250
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**Utah**
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4980 Amelia Earhart Drive
Salt Lake City, Utah 84116
Tel: 801-539-1135

Bell Industries
3639 West 2150 South
Salt Lake City, Utah 84120
Tel: 801-972-6969 TWX: 910-925-5686

Hamilton/Avnet Electronics
1585 West 2100 South
Salt Lake City, Utah 04119
Tel: 801-972-2800 TWX: 910-925-4018

Wyle Distribution Group
1959 South 4130 West, Unit B
Salt Lake City, Utah 84104
Tel: 801-974-9953

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Arrow Electronics
8002 Discovery Drive
Richmond, Virginia 23285
Tel: 804-0413 TWX: 710-956-0169

**Washington**
Arrow Electronics
14320 N.E. 21st Street
Bellevue, Washington 98005
Tel: 206-643-4800 TWX: 910-443-3033

Hamilton/Avnet Electronics
14212 N.E. 21st Street
Bellevue, Washington 98005
Tel: 206-453-5844 TWX: 910-443-2469

Radar Electronic Co., Inc.
168 Western Avenue W.
Seattle, Washington 98119
Tel: 206-282-2511 TWX: 910-444-2052

Wyle Distribution Group
1750 132nd Avenue N.E.
Bellevue, Washington 98005
Tel: 206-453-8300 TWX: 910-443-2526

**Wisconsin**
Arrow Electronics
430 W. Rawson Avenue
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2975 South Moorland Road
New Berlin, Wisconsin 53151
Tel: 414-784-4510 TWX: 910-262-1182

Schweber Electronics
150 Synnyslope Road, Suite 120
Brookfield, Wisconsin 53005
Tel: 414-784-9020

**Canada**

Future Electronics Corporation
5809 MacLeod Trail S. Unit 109
Calgary, Alberta T23 0J9
Tel: 403-259-6437

Future Electronics Inc.
4800 Dufferin Street
Downsview, Ontario, M3H 5S8, Canada
Tel: 416-663-5563

Future Electronics Inc.
Baxter Center
1050 Baxter Road
Ottawa, Ontario, K2C 3P2, Canada
Tel: 613-820-8313

Future Electronics Inc.
237 Hymus Blvd.
Pointe Claire (Montreal), Quebec, H9R 5C7, Canada
Tel: 514-694-7710 TWX: 610-421-3251

Future Electronics Corporation
3070 Kingsway
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Hamilton/Avnet Canada Ltd.
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Tel: 613-226-1700 Telex: 0534-971

Hamilton/Avnet Canada Ltd.
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St. Laurent, Quebec, H4S 1M2, Canada
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Semad Electronics Ltd.
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Dorval, Quebec, H9P 2P4, Canada
Tel: 604-299-8866 TWX: 610-422-3048

Semad Electronics Ltd.
864 Lady Ellen Place
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Phoenix, Arizona 85021
Tel: 602-864-1905 TWX: 910-951-1544

**California**
Los Angeles Office*
Crocker Bank Bldg.
15760 Ventura Blvd., Suite 1027
Encino, California 91436
Tel: 213-990-9800 TWX: 910-495-1776

San Diego Office
4355 Ruffin Road, Suite 100
San Diego, California 92123
Tel: 714-560-1332

Santa Ana Office
1570 Brookhollow Drive, Suite 206
Santa Ana, California 92705
Tel: 714-557-7350 TWX: 910-595-1109

Santa Clara Office*
3333 Bowers Avenue, Suite 299
Santa Clara, California 95051
Tel: 408-980-9990 TWX: 910-338-0241

**Colorado**
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Tel: 303-695-4950

**Connecticut**
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250 Pomeroy Avenue
Meriden, Connecticut 06450
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Ft. Lauderdale Office
5237 N.W. 33rd Avenue Suite 2D
Ft. Lauderdale, Florida 33309
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Orlando Office
Crane's Roost Office Park
399 Whooping Loop
Altamonte Springs, Florida 32701
Tel: 305-834-7000 TWX: 810-850-0152

**Georgia**
Norcross Office*
3220 Pointe Parkway, Suite 1200
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500 Park Blvd., Suite 575
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**Iowa**
Cedar Rapids Office
373 Collin Road N.E., Suite 200
Cedar Rapids, Iowa 52402
Tel: 319-395-0090

**Indiana**
Indianapolis Office
7202 N. Shadeland, Room 205
Castle Point
Indianapolis, Indiana 46250
Tel: 317-849-5412 TWX: 810-260-1793

**Kansas**
Kansas City Office
8600 West 110th Street, Suite 209
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Wichita Office
2424 N. Woodlawn
Wichita, Kansas 67220
Tel: 316-687-1111 TWX: 710-826-9654

**Maryland**
Columbia Office
2000 Century Plaza, Suite 114
Columbia, Maryland 21044
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**Massachusetts**
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Framingham, Massachusetts 01701
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21999 Farmington Road
Farmington Hills, Michigan 48024
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Minneapolis Office
4570 West 77th Street, Room 356
Edina, Minnesota 55435
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**New Jersey**
New Jersey Office
Vreeland Plaza
41 Vreeland Avenue
Totowa, New Jersey 07511
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**New Mexico**
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Fairport Office
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Fairport, New York 14450
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Hauppauge Office*
300 Wheeler Road
Hauppauge, New York 11788
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Cleveland Office
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Columbus Office
960 West Henderson Road
Columbus, Ohio 43220
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# Notes

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A Schlumberger Company



Manufactured under one or more of the following U.S. Patents: 3,562,721, 3,586,922, 3,590,274, 3,639,781, 3,648,125, 3,772,660; other patents pending.

Printed in U.S.A. 605050 30M