FAIRCHILD

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Fairchild Advanced CMOS Technology

Logic Data Book

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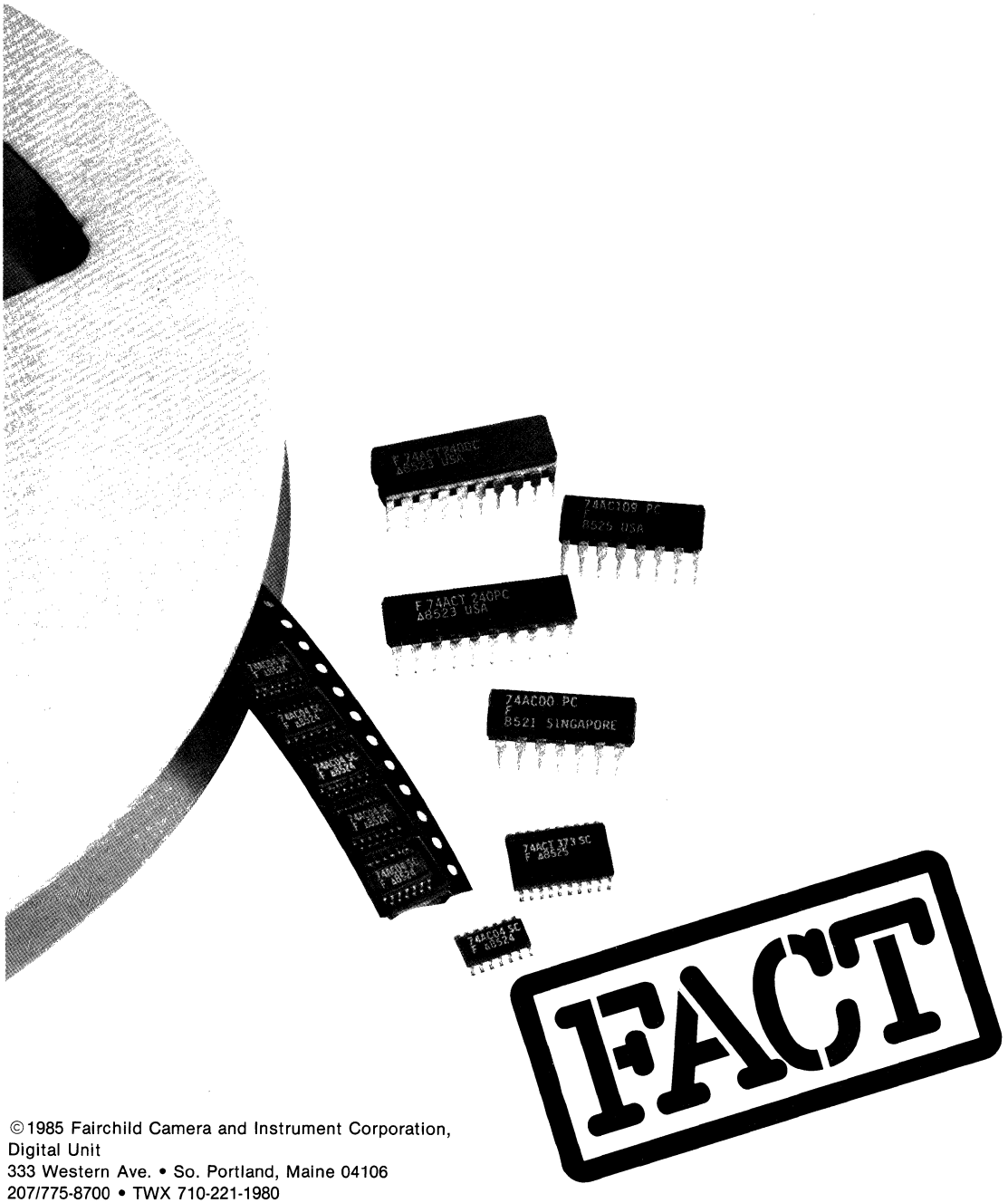

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Introduction

This data book presents advanced information on Fairchild's very high-speed, low-power CMOS logic family, fabricated with Fairchild's state-of-the-art CMOS process.

FACT (Fairchild Advanced CMOS Technology) utilizes Fairchild's 2 μm Isoplanar silicon gate CMOS process to attain speeds similar to that of Advanced Low Power Schottky while retaining the advantages of CMOS logic, namely, ultra low power and high noise immunity. As an added benefit, FACT offers the system designer superior line driving characteristics and excellent ESD and latch-up immunity.

The FACT family consists of devices in two categories:

1. **AC**, standard logic functions with CMOS compatible inputs and TTL and MOS compatible outputs;
2. **ACT**, standard logic functions with TTL compatible inputs and TTL and MOS compatible outputs.

Section 1 Literature Classification, Product Index, and Selection Guide
Tabulation of device numbers to assist in locating appropriate technical data.

Section 2 FACT Description and Family Characteristics
Basic information on FACT including performance comparisons with competitive technologies.

Section 3 Design Considerations
Information to assist both TTL and CMOS designers to get the most out of Fairchild's FACT.

Section 4 Data Sheets

Section 5 Package Outlines and Ordering Information

Section 6 Field Sales Offices and Distributor Locations

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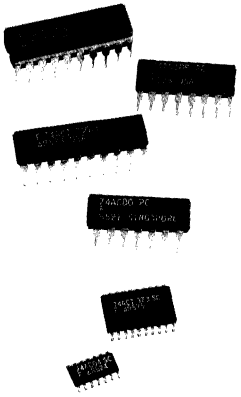

Literature Classification

PRELIMINARY

Preliminary: This product is in sampling or preproduction stage. This document contains advanced information and specifications that are subject to change without notice. Fairchild reserves the right to make changes at any time in order to improve design and provide the best product possible.

ADVANCE INFORMATION

Advance Information: The material described is in the formative or design phase. Specifications may be changed in any manner without notice.

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Product Index and Selection Guide

Product Index

*Full data sheet for this device will be available upon product release.

Product Index (Cont'd)

*Full data sheet for this device will be available upon product release.

Selection Guide

Gates

Function	Device	Page No.
Quad 2-Input NAND	54AC/74AC00	4-3
Triple 3-Input NAND	54AC/74AC10	*
Dual 4-Input NAND	54AC/74AC20	*
Quad 2-Input AND	54AC/74AC08	*
Triple 3-Input AND	54AC/74AC11	*
Quad 2-Input NOR	54AC/74AC02	*
Hex Inverter	54AC/74AC04	*
Hex Schmitt Trigger Inverter	54AC/74AC14	*
Quad 2-Input OR	54AC/74AC32	*
Quad 2-Input Exclusive-OR	54AC/74AC86	*

Flip-Flops

Function	Device	3-State Outputs	Master Reset	Page No.
Dual D	54AC/74AC74	No	No	4-4
Dual $J\overline{K}$	54AC/74AC109	No	No	4-7
Quad D Flip-Flop	54AC/74AC175	No	Yes	*
Quad D Flip-Flop	54AC/74AC379	No	No	*
Hex D Flip-Flop	54AC/74AC174	No	Yes	*
Hex D Flip-Flop	54AC/74AC378	No	No	*
Octal D Flip-Flop	54AC/74AC273	No	Yes	*
Octal D Flip-Flop	54AC/74AC374	Yes	No	4-42
Octal D Flip-Flop	54ACT/74ACT374	Yes	No	*
Octal D Flip-Flop	54AC/74AC377	No	No	*
Octal D Flip-Flop	54AC/74AC564	Yes	No	*
Octal D Flip-Flop	54ACT/74ACT564	Yes	No	*
Octal D Flip-Flop	54AC/74AC574	Yes	No	*
Octal D Flip-Flop	54ACT/74ACT574	Yes	No	*

Latches

Function	Device	3-State Outputs	Broadside Pinout	Page No.
Octal Latch	54AC/74AC373	Yes	No	4-38
Octal Latch	54ACT/74ACT373	Yes	No	*
Octal D Latch	54AC/74AC563	Yes	Yes	*
Octal D Latch	54ACT/74ACT563	Yes	Yes	*
Octal D Latch	54AC/74AC573	Yes	Yes	*
Octal D Latch	54ACT/74ACT573	Yes	Yes	*

*Full data sheet for this device will be available upon product release.

Counters

Function	Device	Parallel Entry	Reset	U/D	3-State Outputs	Page No.
4-Bit BCD Decade	54AC/74AC160	S	A	No	No	*
4-Bit Binary	54AC/74AC161	S	A	No	No	*
4-Bit Binary	54AC/74AC163	S	S	No	No	*
4-Bit Binary	54AC/74AC169	S	S/A	Yes	No	*
4-Bit Binary	54AC/74AC191	A	No	Yes	No	*
4-Bit Binary	54AC/74AC569	S	S/A	Yes	Yes	*

S = Synchronous
A = Asynchronous

Shift Registers

Function	Device	No. of Bits	Reset	Serial Inputs	3-State Outputs	Page No.
Octal Shift/Storage Register	54AC/74AC299	8	A	2	Yes	*
Octal Shift/Storage Register	54AC/74AC323	8	S	2	Yes	*

S = Synchronous
A = Asynchronous

Buffers/Line Drivers

Function	Device	Enable Inputs (Level)	Inverting/ Noninverting	Broadside Pinout	Page No.
Octal Buffer/Line Driver	54AC/74AC240	2(L)	I		4-20
Octal Buffer/Line Driver	54ACT/74ACT240	2(L)	I		4-22
Octal Buffer/Line Driver	54AC/74AC241	1(L) & 1(H)	N		4-24
Octal Buffer/Line Driver	54ACT/74ACT241	1(L) & 1(H)	N		4-26
Octal Buffer/Line Driver	54AC/74AC244	2(L)	N		4-28
Octal Buffer/Line Driver	54ACT/74ACT244	2(L)	N		4-30
Octal Buffer/Line Driver	54AC/74AC540	2(L)	I	Yes	*
Octal Buffer/Line Driver	54AC/74AC541	1(L) & 1(H)	N	Yes	*

*Full data sheet for this device will be available upon product release.

Multiplexers

Function	Device	Enable Inputs (Level)	True Output	Complement Output	Page No.
8-Input	54AC/74AC151	1(L)	Yes	Yes	*
Dual 4-Input	54AC/74AC153	2(L)	Yes	No	4-17
Quad 2-Input	54AC/74AC157	1(L)	Yes	No	*
Quad 2-Input	54AC/74AC158	1(L)	No	Yes	*
8-Input	54AC/74AC251	1(L)	Yes	Yes	*
Dual 4-Input	54AC/74AC253	2(L)	Yes	No	4-34
Quad 2-Input	54AC/74AC257	1(L)	Yes	No	*
Quad 2-Input	54AC/74AC258	1(L)	No	Yes	*

Decoders/Demultiplexers

Function	Device	LOW Enable	Active-HIGH Enable	Active-LOW Outputs	Active-Address Inputs	Page No.
1-of-8 Decoder/Demultiplexer	54AC/74AC138	2	1	8	3	4-10
1-of-8 Decoder/Demultiplexer	54ACT/74ACT138	2	1	8	3	*
Dual 1-of-4 Decoder	54AC/74AC139	1 & 1	No	4 & 4	2 & 2	4-14

Comparators

Function	Device	Features	Page No.
Octal Comparator	54AC/74AC520	Expandable	*
Octal Comparator	54AC/74AC521	Expandable	*

Transceivers/Registered Transceivers

Function	Device	Registered	Enable Inputs (Level)	3-State Output	Page No.
Octal Bus Transceiver	54AC/74AC245	No	1(L)	Yes	4-32
Octal Bus Transceiver	54ACT/74ACT245	No	1(L)	Yes	*
Octal Bus Transceiver	54AC/74AC646	Yes	1(L) & 1(H)	Yes	*
Octal Bus Transceiver	54AC/74AC648	Yes	1(L) & 1(H)	Yes	*

*Full data sheet for this device will be available upon product release.

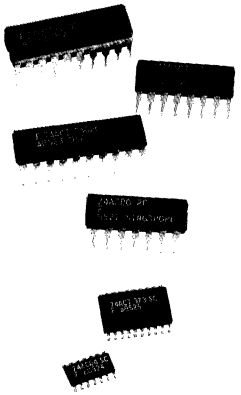
FIFOs

Function	Device	Input	Output	3-State Output	Page No.
64 X 9 FIFO	54AC/74AC708	Parallel	Parallel	Yes	*
64 X 9 FIFO	54ACT/74ACT708	Parallel	Parallel	Yes	*

Arithmetic Functions

Function	Device	Features	Page No.
16 X 16 Multiplier/Accumulator	54AC/74AC1010	2's Complement & unsigned arith.	*
16 X 16 Multiplier/Accumulator	54ACT/74ACT1010	2's Complement & unsigned arith.	*
16 X 16 Multiplier	54AC/74AC1016	2's Complement & unsigned arith.	*
16 X 16 Multiplier	54ACT/74ACT1016	2's Complement & unsigned arith.	*
16 X 16 Multiplier	54AC/74AC1017	Common Clock	*
16 X 16 Multiplier	54ACT/74ACT1017	Common Clock	*

*Full data sheet for this device will be available upon product release.



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FACT Description and Family Characteristics

Fairchild Digital's Advanced CMOS Logic

Fairchild Digital is pleased to announce FACT (Fairchild Advanced CMOS Technology), a family of high-speed ADVANCED CMOS logic circuits.

This versatile new family promises to be the product family for future logic systems, offering a unique combination of high-speed, low-power dissipation, high noise immunity, wide fanout capability, extended power supply range and high reliability. This data book describes the initial product line scheduled for introduction during 1985. All device specifications are included for these products as well as a section on designing with this family and its comparison to predecessor technologies.

The two micron, silicon gate CMOS process utilized in this family has been proven in the field of high performance gate arrays for the last two years and has been further enhanced to meet and exceed the JEDEC standards for 74HCXX logic.

For direct replacement of LS and ALS devices, the ACT circuits with TTL-type input thresholds are included in the FACT family. These include the more popular bus drivers/transceivers as well as many other 54ACT/74ACTXXX devices.

Characteristics

- Full Logic Product Line
- Industry Standard Functions and Pinouts for SSI and MSI
- Meets or Exceeds JEDEC Standards for 74HCXX Family
- TTL Inputs on Selected Circuits
- High Performance Outputs
  - Common Output Structure For Standard and Buffer Drivers
  - Output Sink/Source Current of 24 mA
  - Transmission Line Driving 50 Ω (Comm)/ 75 Ω (Mil) Guaranteed
- Operation from 2-6 Volts
- Temperature Range −40°C to +85°C (Comm), −55°C to +125°C (Mil)
- Improved Gate Protection Network
- High Current Latch Up Immunity

Low Power CMOS Operation

If there is one single characteristic that justifies the existence of CMOS, it is low power dissipation. In the quiescent state, FACT draws three orders of magnitude less power than the equivalent LS or ALS TTL device. This feature can only enhance system reliability while eliminating costly regulated high current power supplies, heat sinks, fans and the like.

Operating power is also very low for FACT. Power consumption of various technologies, with a clock frequency of 1 MHz, is shown below.

FACT = 0.1 mW/Gate
ALS = 1.2 mW/Gate
LS = 2.0 mW/Gate
HC = 0.1 mW/Gate

These are typical values measured at 1 MHz.

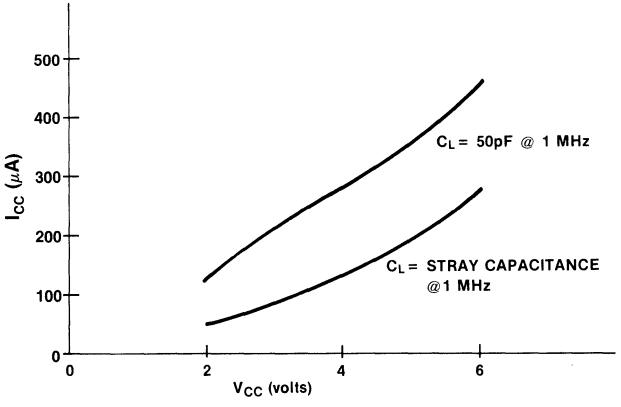


Figure 2-1 I_{CC} vs V_{CC}

Figure 2-1 shows the effects of I_{CC} vs. power supply voltage (V_{CC}) with two load capacitance values, 50 pF and stray capacitance. The clock frequency is measured at 1 MHz.

AC Performance

In comparison to LS, ALS, and HC families, FACT devices exceed the internal gate delays as well as the basic gate delays, and as the level of integration increases, FACT leads the way to very high-speed systems.

The example below describes averaged typical values for a 74XX138, 3-to-8 line decoder.

FACT = 8 ns @ C_L = 50 pF
ALS = 8.5 ns @ C_L = 50 pF
LS = 22 ns @ C_L = 15 pF
HC = 17.5 ns @ C_L = 50 pF

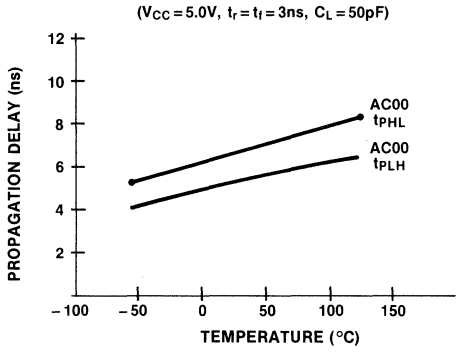


Figure 2-2 Propagation Delay vs. Temperature

Figure 2-2 describes the effects of temperature on the LOW-to-HIGH and HIGH-to-LOW transitions for propagation delays on a FACT quad NAND gate. The plot shows approximately 2 ns deviation over the entire operating temperature range.

AC performance specifications are guaranteed at 5.0 V ± 10% and 3.3 V ± 0.3V. For worst case design at 2.0 V V_{CC} on all device types, derating values are provided. The formula below can be used to determine AC performance at 2.0 V V_{CC}.

AC performance at 2.0 V V_{CC} = 1.9 x AC specification at 3.0 V.

Propagation delay is affected by the number of outputs switching simultaneously. Typically, devices with more than one output will follow the rule: for each output switching, derate the databook specification by 250 pS. This effect typically is not significant on an octal device unless more than four outputs are switching simultaneously. This derating is valid for the entire temperature range and 5.0 V ± 10% V_{CC}.

Noise Immunity

The noise immunity of a logic family is also an important equipment cost factor in terms of decoupling components, power supply dynamic resistance and regulation as well as layout rules for PC boards and signal cables.

The comparisons shown describe the difference between the input threshold of a device and the output voltage, $V_{IL} - V_{OL} / | V_{IH} - V_{OH} |$ @ 4.5 V V_{CC}.

FACT = 1.25/1.25 V
ALS = 0.4/0.7 V
LS = 0.3/0.7 V @ 4.75 V V_{CC}
HC = 0.8/1.25 V

Output Drive

As mentioned before, all devices (AC or ACT) have the same output stages and are all guaranteed to source or sink 24 mA, still outperforming HC buffer drivers in speed and power. Furthermore, 74AC/74ACT devices are capable of driving 50 Ω transmission lines while for 54AC/54ACT 75 Ω lines can be driven.

I_{OL}/I_{OH} Characteristics

FACT = 24/ – 24 mA
ALS = 24/ – 15 mA
LS = 8/ – 0.4 mA @ 4.75 V V_{CC}
HC = 4/ – 4 mA

Choice of Voltage Specifications

To obtain better performance and higher density, semiconductor technologists are reducing the vertical and horizontal dimensions of integrated device structures. Due to a number of electrical limitations in the manufacture of VLSI devices and the need for low voltage operation in memory cards, it was decided by the JEDEC committee to establish interface standards for devices operating at 3.3 V ± 0.3 V. To this end Fairchild Digital guarantees all of its devices operational at 3.3 V ± 0.3 V. Note also that AC and DC specifications are guaranteed between 4.5 and 5.5 V. Operation of FACT devices is also guaranteed from 2.0 V to 6.0 V on V_{CC}.

Operating Voltage Ranges

FACT = 2.0 to 6.0 V
ALS = 5.0 V ± 10%
LS = 5.0 V ± 5%
HC = 2.0 to 6.0 V

Replacement For LS, ALS, HCMOS

Fairchild's Advanced CMOS family is specifically designed to outperform the LS, ALS and HCMOS families. The graph (Figure 2-3) shows the relative position of various logic families in speed/power performance. FACT exhibits 1 ns internal propagation delays while consuming 1μW of power.

The Logic Family Comparisons table below summarizes the key performance specifications for various competitive technology logic families.

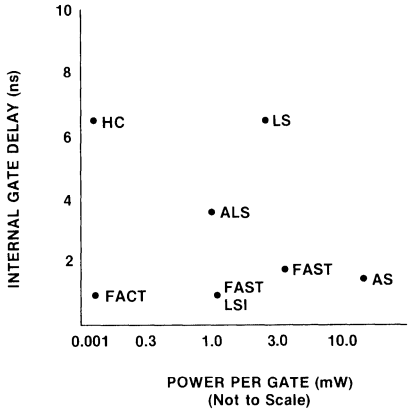


Figure 2-3 Internal Gate Delays

Logic Family Comparisons

General Characteristics (All Max Ratings)

Characteristics	Symbol	LS	ALS	HCMOS	FACT	Unit
Operating Voltage Range	$V_{CC/EE/DD}$	5 ± 5%	5 ± 10%	2.0 to 6.0	2.0 to 6.0	V
Operating Temperature Range	t_A 74 Series	0 to +70	0 to +70	−40 to +85	−40 to +85	°C
Input Voltage (limits)	V_{IH} (min)	2.0	2.0	3.15	3.15	V
	V_{IL} (max)	0.8	0.8	0.9	1.35	V
Output Voltage (limits)	V_{OH} (min)	2.7	2.7	V_{CC} − 0.1	V_{CC} − 0.1	V
	V_{OL} (max)	0.5	0.5	0.1	0.1	V
Input Current	I_{IH}	20	20	+1.0	+1.0	μA
	I_{IL}	−400	−200	−1.0	−1.0	μA
Output Current @ V_0(limit)	I_{OH}	−0.4	−0.4	−4.0@V_{CC} − 0.8	−24@V_{CC} − 0.8	mA
	I_{OL}	8.0	8.0	4.0 @ 0.4 V	24 @ 0.4 V	mA
DC Noise Margin LOW/HIGH	DCM	0.3/0.7	0.4/0.7	0.8/1.25	1.25/1.25	V
DC Fanout (LSTTL)		20	20	10	60	

Logic Family Comparisons (cont'd)

Speed/Power Characteristics (All Typical Ratings)

Characteristics	Symbol	LS	ALS	HCMOS	FACT	Unit
Quiescent Supply Current/Gate	I_G	0.4	0.2	0.0005	0.0005	mA
Power/Gate (Quiescent)	P_G	2.0	1.2	0.0025	0.0025	mW
Propagation Delay	t_P	7.0	5.0	8.0	5.0	ns
Speed Power Product	-	14	6.0	0.02	0.01	pJ
Clock Frequency D/FF	f_{max}	33	50	50	125	MHz

Propagation Delay (Commercial Temperature Range)

	Product		LS	ALS	HCMOS	FACT	Unit
t_{PLH}/t_{PHL}	74XX00	Typ	10.0	5.0	8.0	5.0	ns
		Max	15.0	11.0	23.0	9.5	ns
t_{PLH}/t_{PHL} (Clock to Q)	74XX74	Typ	25.0	12.0	23.0	8.0	ns
		Max	40.0	18.0	44.0	11.0	ns
t_{PLH}/t_{PHL} (Clock to Q)	74XX163	Typ	18.0	10.0	20.0	10.0	ns
		Max	27.0	17.0	52.0	17.0	ns

Conditions: (LS) $V_{CC} = 5.0$ V ± 5%, $C_L = 15$ pF, 25°C;
(ALS/HC/FACT) $V_{CC} = 5.0$ V ± 10%, $C_L = 50$ pF, Typ values at 25°C, Max values at 0 to 70°C for ALS, −40 to +85°C for HC/FACT.

Circuit Characteristics

Power Dissipation

Power consumption for FACT is dependent on the supply voltage, frequency of operation, internal capacitance and load. The power consumption may be calculated for each package by summing the quiescent power consumption, I_{CC}, V_{CC}, and the switching power required by each device within the package. The device dynamic power requirements can be calculated by the equation:

$$P_D = (C_L + C_{PD})V_{CC}^2 f$$

In this equation f is the frequency in Hertz, C_L is the total load capacitance present at the output under test, and C_{PD}, power dissipation capacitance, is a measure of internal capacitances given specifically for power consumption calculations. C_{PD} is calculated in the following manner:

1. The power supply voltage is set to $V_{CC} = 5.5\ V_{DC}$.
2. Signal inputs are set up so that as many outputs as possible are switching, giving a worst case situation.
3. The power supply current is measured and recorded at input frequencies of 200 KHz and 1 MHz.
4. The power dissipation capacitance is calculated by solving the two simultaneous equations:

$$P_{01} = C_{PD}\ V_{CC}^2\ f_1 + I_{CC}\ V_{CC}$$
$$P_{02} = C_{PD}\ V_{CC}^2\ f_2 + I_{CC}\ V_{CC}$$

giving

$$C_{PD} = (P_{01} - P_{02})/V_{CC}^2\ (f_1 - f_2)$$

or

$$C_{PD} = (I_{01} - I_{02})/V_{CC}\ (f_1 - f_2)$$

where
I_{01} = supply current at $f_1 = 200$ KHz
I_{02} = supply current at $f_2 = 1$ MHz

On FACT data sheets, C_{PD} is a typical value and is given either for the package or for the individual device (i.e., gates, flip-flops, etc.) within the package.

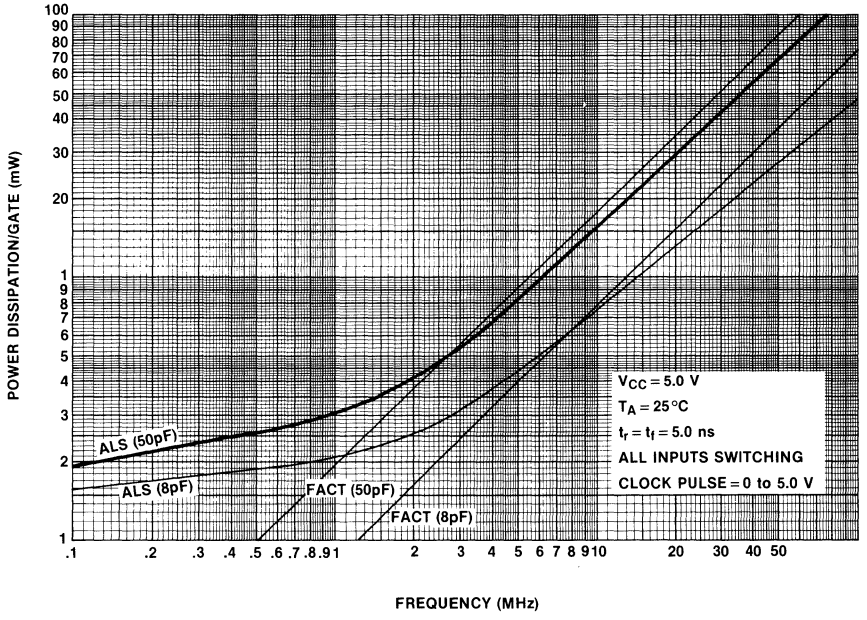


Figure 2-4 Power Dissipation per Gate vs. Frequency

Power Dissipation (Test Philosophy)

In an effort to reduce confusion about measuring C_{PD}, a de facto standard test procedure has been adopted which specifies the test setup for each type of device. This allows a device to be exercised in a consistent manner for the purpose of specification comparison. All device measurements are made with $V_{CC} = 5.0$ V at 25°C, with 3-state outputs both enabled and disabled.

Gates:	Switch one input. Bias the remaining inputs such that the output switches.
Latches:	Switch the enable and D inputs such that the latch toggles.
Flip-Flops:	Switch the clock pin while changing D (or bias J and K) such that the output(s) change each clock cycle. For parts with common clock, exercise only one flip-flop.
Decoders:	Switch one address pin which changes two outputs.
Multiplexers:	Switch one address input with the corresponding data inputs at opposite logic levels so that the output switches.
Counters:	Switch the clock pin with other inputs biased such that the device counts.
Shift Registers:	Switch the clock, adjust the data inputs such that the register fills with alternate 1s and 0s.
Transceivers:	Switch one data input. For bidirectional devices enable only one direction.
Parity Generators:	Switch one input.
Priority Encoders:	Switch the lowest priority input.
Load Capacitance:	Each output which is switching should be loaded with the standard 50 pF. The equivalent load capacitance, based upon the number of outputs switching and their respective frequency, is then subtracted from the measured gross C_{PD} number to obtain the device's actual C_{PD} value.

If the device is tested at a high enough frequency, the static supply current can be ignored. Thus at 1 MHz the following formula can be used to calculate C_{PD}:

$C_{PD} = I_{CC}/(V_{CC})(1 \times 10^6) - (\text{Equivalent load capacitance})$

Capacitive Loading Effects

In addition to temperature and power supply effects, capacitive loading effects should be taken into account for propagation delays of FACT devices. Minimum delay numbers may be determined from the table below. Propagation delays are measured to the 50% point of the output waveform.

	Voltage			
	3.0V	**4.5V**	**5.5V**	
t_{PLH}/pF	31	22	19	**Output Drive (ps/pF)**
t_{PHL}/pF	18	13	12.5	

Condition = 25°C

The two graphs following (Figures 2-5 and 2-6) describe propagation delays on FACT devices as affected by variations in power supply voltage (V_{CC}) and lumped load capacitance (C_L). Figures 2-7 and 2-8 show the effects of lumped load capacitance on rise and fall times for FACT devices.

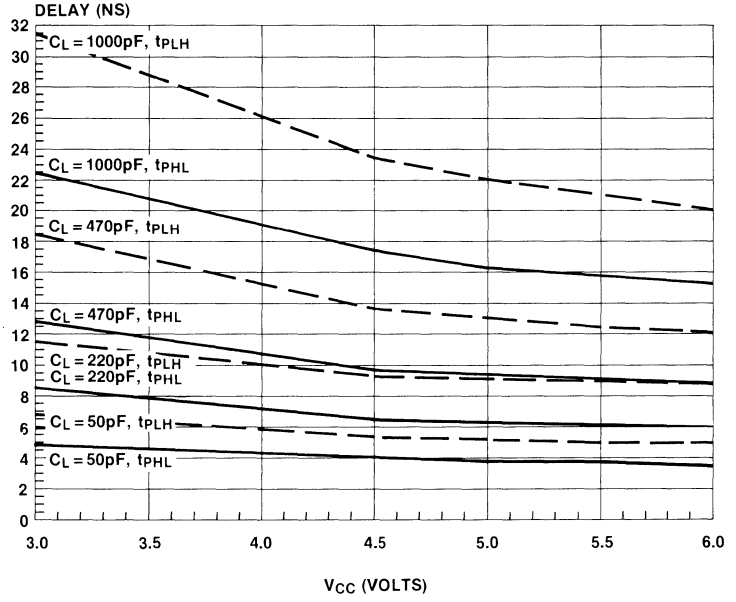


Figure 2-5 Propagation Delay vs. V_{CC} ('AC00)

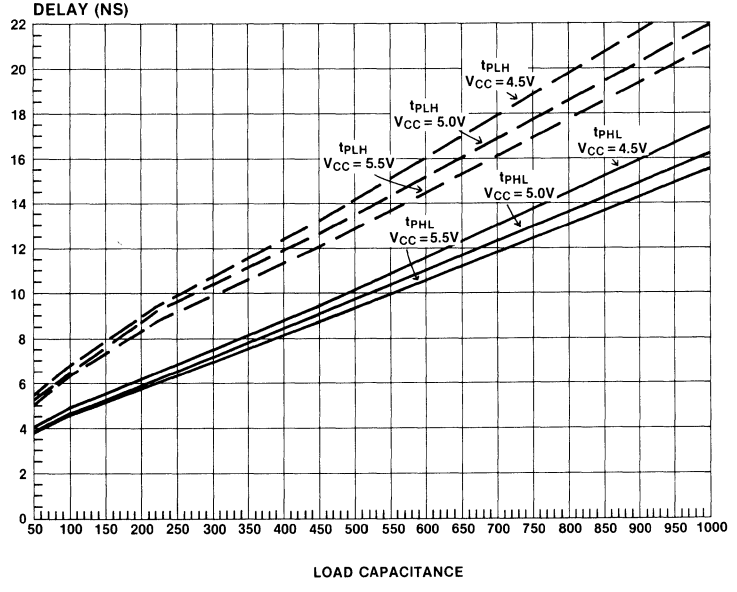


Figure 2-6 Propagation Delay vs. C_L ('AC00)

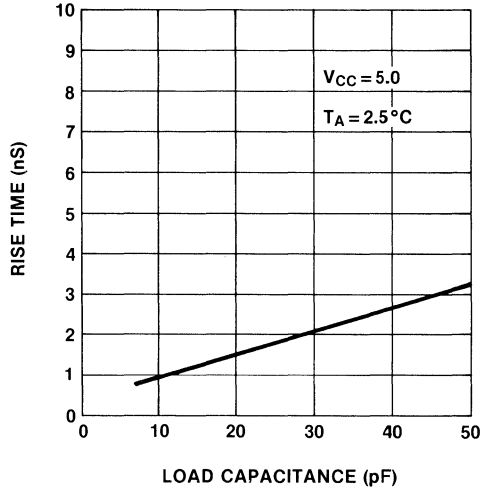


Figure 2-7 t_r vs. Capacitance

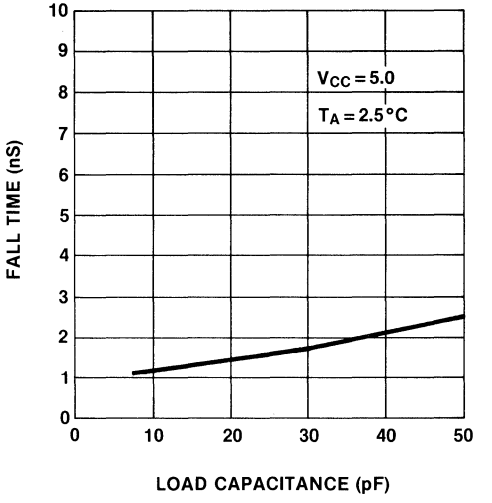


Figure 2-8 t_f vs. Capacitance

Latch Up

Latch up immunity in FACT devices is greatly improved over the standard metal gate CMOS family. These devices will not latch up with dynamic currents of 100 mA forced into or out of the inputs or 100 mA for the outputs under worst case conditions ($T_A = 125°C$ and $V_{CC} = 6\ V_{DC}$). At room temperatures the parts can typically withstand dynamic current forced into or out of the outputs of over 450 mA. For most designs, latch up will not be a problem, but the designer should be aware of it, what causes it and how to prevent it.

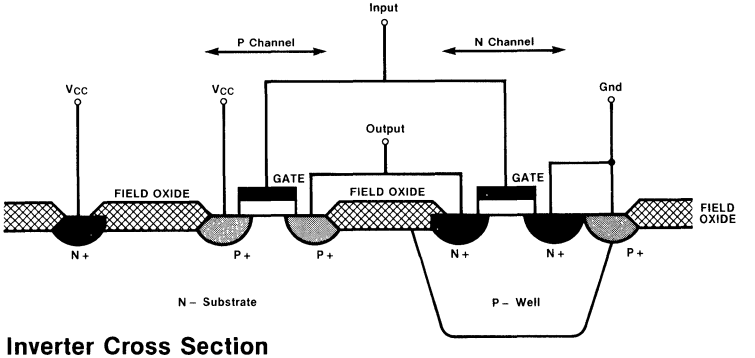


Figure 2-9 CMOS Inverter Cross Section

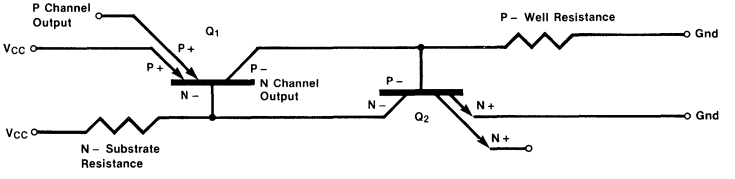


Figure 2-10 Latch Up Circuit Schematic

Electrostatic Discharge (ESD) Sensitivity

Fairchild's FACT devices are classified as standard 'B' of MIL STD-883, test method 3015, and therefore do not require any special handling procedures. However, normal handling precautions should be observed as in the case of any semiconductor device. Figure 2-11 shows the ESD test circuit used in the sensitivity analysis for this specification. Figure 2-12 shows the pulse waveform required to perform the sensitivity test. The test procedure is as follows: five pulses, each of 2000 V, are applied to every combination of pin with a five second cool-down period between each pulse. Reverse the polarity and use the same procedure, pulse and same pin combination for an additional five discharges. Continue until all pins have been tested.

If none of the devices from the sample population fails the DC and AC test characteristics, the device shall be classified as standard B of MIL STD-883, test procedure 3015. For further specifications of TP-3015 the reader should follow up the relevant standard.

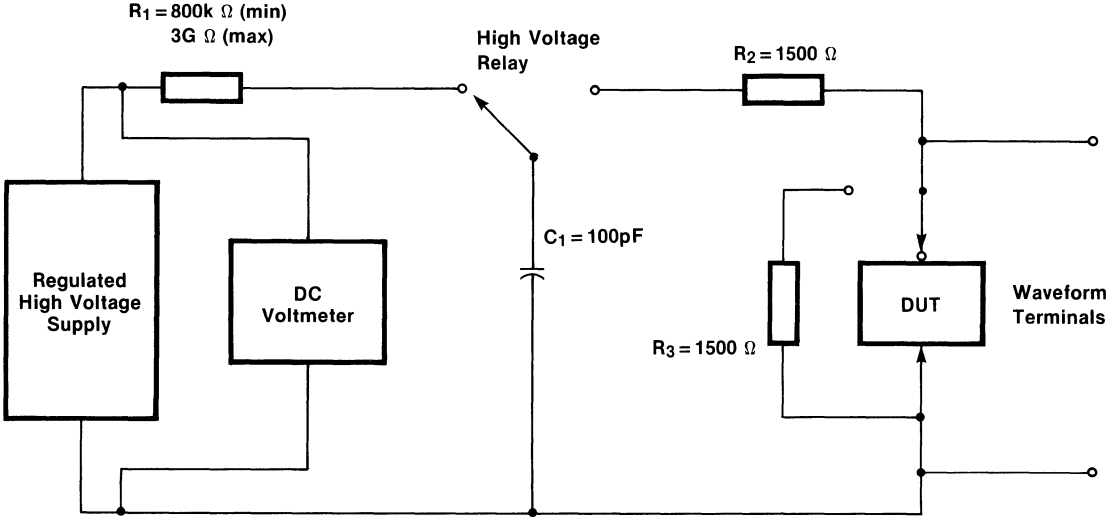


Figure 2-11 ESD Test Circuit

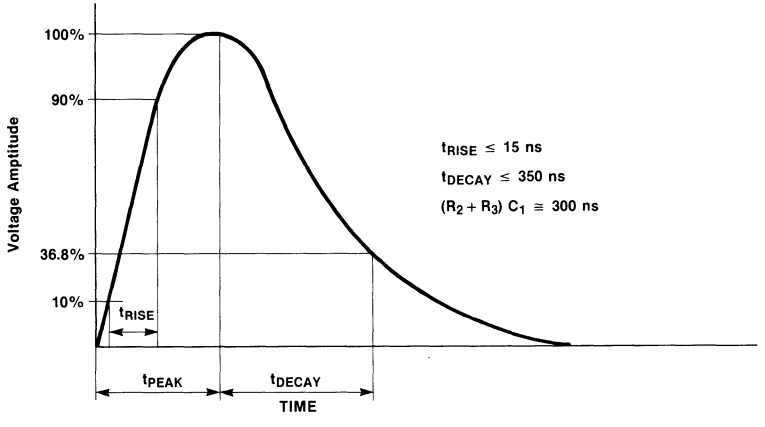


Figure 2-12 ESD Pulse Waveform

Output Characteristics

All FACT outputs are buffered to ensure consistent output voltage and current specifications across the family. Both 74ACXX and 74ACTXX device types have the same output structures. Two clamp diodes are internally connected to the output pin to improve impedance matching with other FACT device inputs and to suppress voltage overshoot and undershoot in noisy system applications. The balanced output design allows for controlled edge rates and equal rise and fall times.

Dynamic Output Current

54 Series Parts
$I_{OL} = 57$ mA @ $V_{CC} = 5.5$ V, $V_{OUT} = 1.1$ V, $T_A = 125°C$
$I_{OH} = 50$ mA @ $V_{CC} = 5.5$ V, $V_{OUT} = 3.85$ V, $T_A = 125°C$

74 Series Parts
$I_{OL} = 86$ mA @ $V_{CC} = 5.5$ V, $V_{OUT} = 1.1$ V, $T_A = 85°C$
$I_{OH} = 75$ mA @ $V_{CC} = 5.5$ V, $V_{OUT} = 3.85$ V, $T_A = 85°C$

The following performance charts are provided in order to aid the designer in determining dynamic output current drive of FACT devices with various power supply voltages.

Interfacing

FACT devices have a wide operating voltage range ($V_{CC} = 2$ to 6 V_{DC}) and sufficient current drive to interface with most other logic families available today.

Device designators are as follows:

AC—This is a high-speed CMOS device with CMOS input switching levels and buffered CMOS outputs that can drive ± 24 mA of I_{OH} and I_{OL} current. AC nomenclature and pinouts are equivalent to standard TTL functions.

ACT—This is a high-speed CMOS device with a TTL-to-CMOS input buffer stage. These devices are designed to interface with TTL outputs operating with a $V_{CC} = 5$ V ± 10%, but are functional over the entire FACT operating voltage range of 2.0 to 6.0 V_{DC}. These devices have buffered outputs that will drive CMOS or TTL devices with no additional interface circuitry. ACT devices have the same output structures as AC devices.

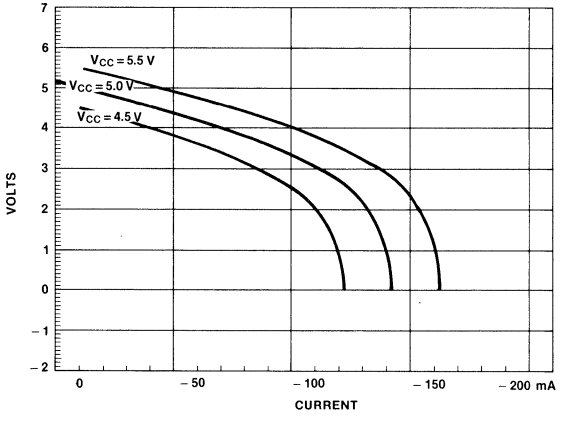


Figure 2-13 Output Characteristics V_{OH}/I_{OH}, 'AC00DC

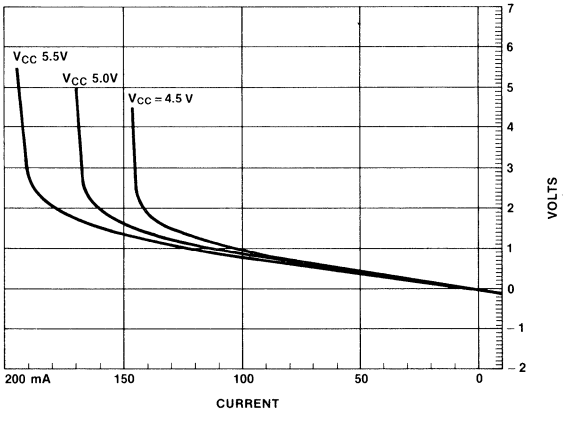


Figure 2-14 Output Characteristics V_{OL}/I_{OL}, 'AC00DC

Ratings, Specifications and Waveforms

Absolute Maximum Ratings*

Parameter	Symbol	Conditions	Limits	Units
Supply Voltage	V_{CC}		−0.5 to 7.0	V
DC Input Diode Current or DC Input Voltage	I_{IK} V_I	$V_I = -0.5$ $V_I = V_{CC} + 0.5$	−20 20 −0.5 to V_{CC} +0.5	mA mA V
DC Output Diode Current or DC Output Voltage	I_{OK} V_O	$V_O = -0.5$ $V_O = V_{CC} + 0.5$	−20 20 −0.5 to V_{CC} +0.5	mA mA V
DC Output Source or Sink Current, Per Output Pin	I_O		±50	mA
DC V_{CC} or Ground Current	I_{CC} or I_{GND}		±200	mA
Storage Temperature	T_{STG}		−65 to 150	°C

*Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Recommended Operating Conditions

Parameter		Symbol	Conditions	Limits	Units
Supply Voltage (unless otherwise specified)		V_{CC}		2.0 to 6.0	V
Input Voltage		V_I		0 to V_{CC}	V
Output Voltage		V_O		0 to V_{CC}	V
Operating Temperature	74AC 54AC	T_A		−40 to +85 −55 to +125	°C °C
Input Rise and Fall Time (except for Schmitt inputs)		t_r, t_f	V_{CC} @ 2.0 V V_{CC} @ 4.5 V V_{CC} @ 6.0 V	0 to 1000 0 to 500 0 to 400	ns ns ns

DC Characteristics for AC Family Devices

Symbol	Parameter	Conditions	V_{CC}	54AC/74AC $T_A = 25°$		54AC $T_A =$ $-55°$ to $+125°C$	74AC $T_A =$ $-40°$ to $+85°C$	Units
				Typ	Guaranteed Maximum			
V_{IH}	Minimum High Level Input Voltage	$V_{OUT} = 0.1$ V or $V_{CC} - 0.1$ V	3.0 4.5 5.5		2.1 3.15 3.85	2.1 3.15 3.85	2.1 3.15 3.85	V
V_{IL}	Maximum Low Level Input Voltage	$V_{OUT} = 0.1$ V or $V_{CC} - 0.1$ V	3.0 4.5 5.5		0.9 1.35 1.65	0.9 1.35 1.65	0.9 1.35 1.65	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IL}$ or V_{IH} $I_{OUT} = -20\mu A$	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	2.9 4.4 5.4	V
		I_{OH} -4 mA -24 mA -24 mA	3.0 4.5 5.5		2.56 3.86 4.86	2.4 3.7 4.7	2.46 3.76 4.76	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IL}$ or V_{IH} $I_{OUT} = 20\ \mu A$	3.0 4.5 5.5	.002 .001 .001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		I_{OL} 4 mA 24 mA 24 mA	3.0 4.5 5.5		0.32 0.32 0.32	0.4 0.4 0.4	0.37 0.37 0.37	V
I_{IN}	Maximum Input Leakage Current	$V_I = V_{CC}$,GND	5.5		± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum 3-State Current	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$,GND	5.5		± 0.5	± 10.0	± 5.0	μA

DC Characteristics for ACT Family Devices

Symbol	Parameter	Conditions	V_{CC}	54AC/74AC $T_A = 25°C$		54AC $T_A =$ $-55°$ to $+125°C$	74AC $T_A =$ $-40°$ to $+85°C$	Units
				Typ	Guaranteed Maximum			
V_{IH}	Minimum High Level Input Voltage	$V_{OUT} = 0.1$ V or $V_{CC} - 0.1$ V	4.5 5.5		2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Minimum Low Level Input Voltage	$V_{OUT} = 0.1$ V or $V_{CC} - 0.1$ V	4.5 5.5		0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IL}$ or V_{IH} $I_{OUT} = -20$ μA	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V
		I_{OH} -24 mA -24 mA	4.5 5.5		3.86 4.86	3.7 4.7	3.76 4.76	V
V_{OL}	Minimum Low Level Output Voltage	$V_I = V_{IL}$ or V_{IH} $I_{OUT} = 20$ μA	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V
		I_{OL} 24 mA 24 mA	4.5 5.5		0.32 0.32	0.4 0.4	0.37 0.37	V
I_{IN}	Maximum Input	$V_I = V_{CC}$,GND	5.5		± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum 3-State Current	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$,GND	5.5		± 0.5	± 10.0	± 5.0	μA
I_{CC}	Maximum I_{CC}/Input	$V_I = 2.4$ V/0.4 V	5.5	0.600	2.0	3.0	2.9	mA

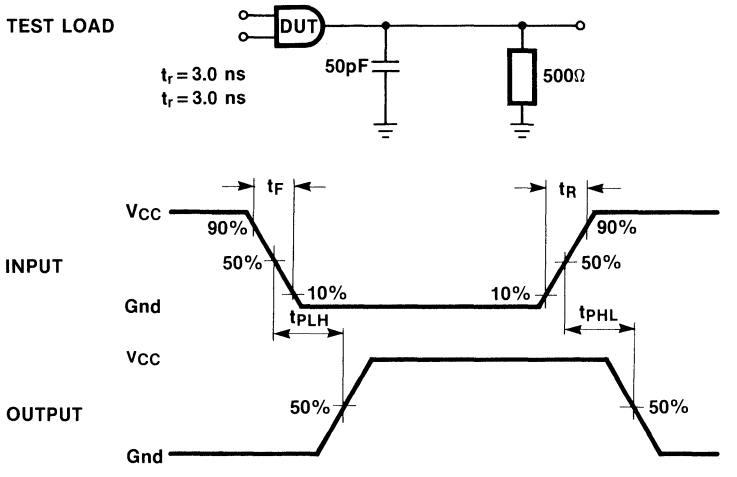


Figure 2-15 AC Measurement Conditions (Standard Outputs)

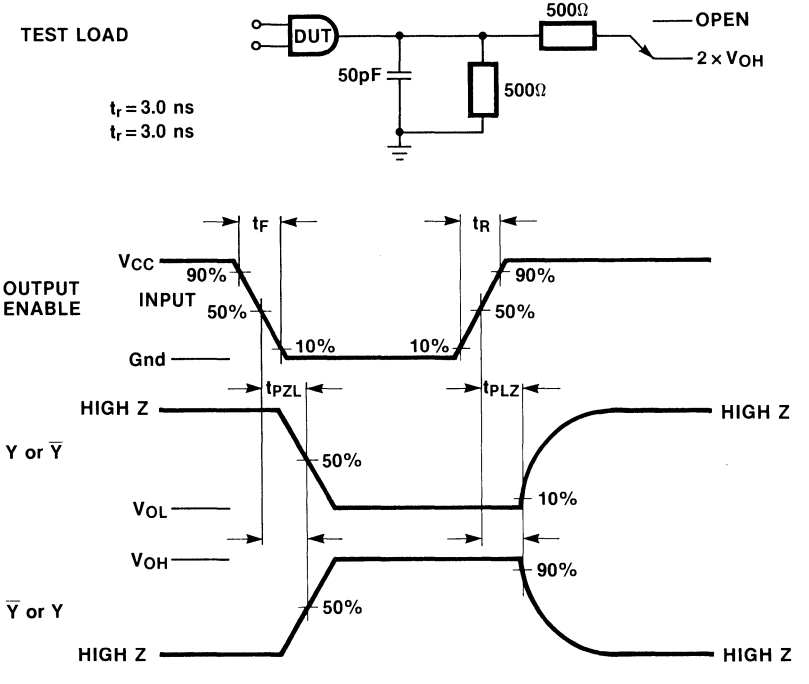
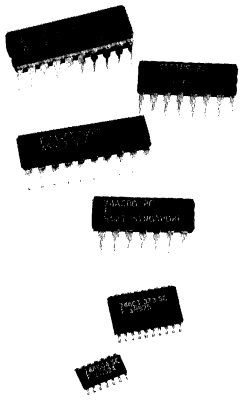


Figure 2-16 AC Measurement Conditions (3-State Outputs)



FAIRCHILD
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Design Considerations

From its conception, FACT was designed to alleviate many of the drawbacks that are common to current technology logic circuits. Performance features such as Schottky speeds at CMOS power levels, Schottky drive, excellent noise, ESD, and latch-up immunity are characteristics that designers of state-of-the-art systems require. FACT answers all of these concerns in one family of logic products. To fully utilize the advantages provided by FACT, the system designer should have an understanding of the flexibility as well as the trade-offs of CMOS design. The following section discusses common design concerns relative to the performance and requirements of FACT.

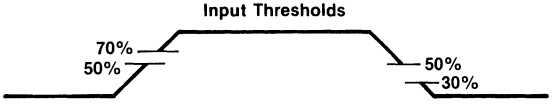


Figure 3-1 Input Thresholds

Line Driving with Fairchild Advanced CMOS

The output structure of FACT has been designed to drive 50 Ω transmission lines over the commercial temperature range, and 75 Ω lines over the military temperature range. This line driving capability is guaranteed over 4.5 to 5.5 V V_{CC} and full temperature range. Balanced 24 mA DC sink and source output currents give controlled edge rates and equal rise and fall times. The logic HIGH and LOW levels are guaranteed to be 70% and 30% of V_{CC} with a minimum of 20% V_{CC} noise margin (Figure 3-1).

Advanced CMOS outputs are specified at 24 mA sink at 0.37 V (4.5 V_{CC}) DC and 24 mA source at 3.76 V (4.5 V_{CC}) DC. Dynamic I_{OH} and I_{OL} performance is guaranteed over commercial and military temperature range and specified at $V_{CC} = 5.5$ V as shown below.

74AC	$I_{OL} = 86$ mA @ $V_{OL} = 1.1$ V $I_{OH} = -75$ mA @ $V_{OH} = 3.85$ V
54AC	$I_{OL} = 57$ mA @ $V_{OL} = 1.1$ V $I_{OH} = -50$ mA @ $V_{OH} = 3.85$ V

Figures 3-2 and 3-3 show V_{OH}/I_{OH} and V_{OL}/I_{OL} at 4.5, 5.0 and 5.5 volts V_{CC}.

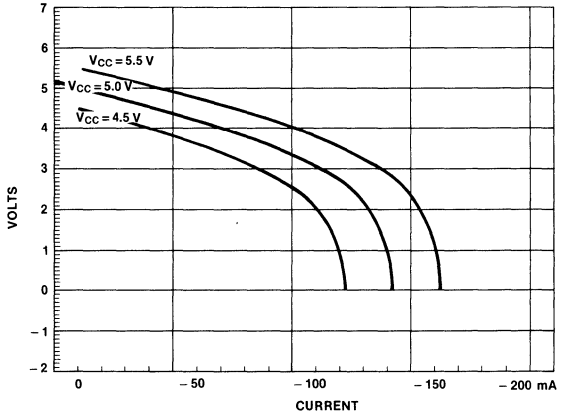


Figure 3-2 Output Characteristics (V_{OH}, I_{OH})

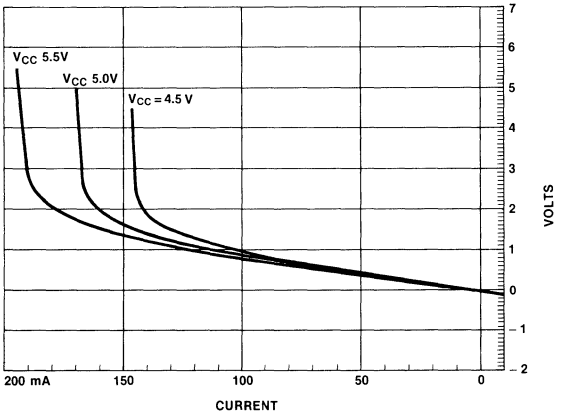


Figure 3-3 Output Characteristics (V_{OL}, I_{OL})

The input and output diode clamps to V_{CC} and ground on a FACT device will match most transmission line impedances. However, it is advisable to terminate any signal line that exceeds 20 inches in length with either the series termination resistor as shown in Figure 3-4 or the AC termination to ground shown in Figure 3-5. Both of these termination schemes consume zero DC power and thus are ideal for low-power applications while optimizing high-speed performance. The AC termination works well with 3-state bus lines and will typically hold the last bus state for a few milliseconds; alternatively, the bus can be forced HIGH or LOW with high value resistors connected to the appropriate power rail.

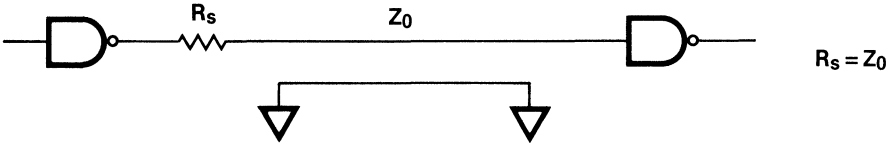
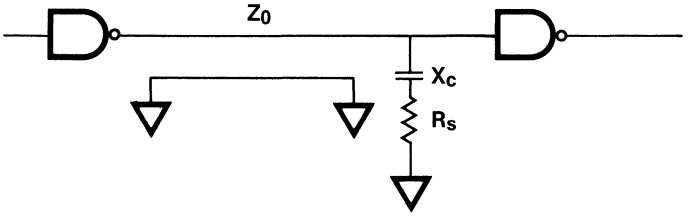


Figure 3-4



$$X_C < 2\ \Omega @\ f = \frac{1}{2\ tpd}$$

$$R_S = Z_0$$

Figure 3-5

When designing high speed systems with FACT, interconnect propagation delays must be considered in the system timing budget.

Most power distribution layouts exhibit an impedance between 50 and 100Ω. The impedance of the power distribution system appears in series with the load, reducing the resultant dynamic voltage swing at the output. When the device outputs are switching, local decoupling capacitors supply the current to the device. An example of an 'AC240 driving a point along a 100 Ω bus is shown in Figure 3-6. The impedance seen by the driver is equivalent to both arms of the bus in parallel at the drive point, in this case 100||100 = 50 Ω. The output will switch between the supply rails at 94 mA of output current. If all outputs switch from LOW to HIGH, the load to V_{CC} would be eight 50Ω impedances in parallel = 6.25Ω. Approximately half the supply impedance would be in series with this load, dropping the V_{CC} to the chip and limiting the output drive. Slow rise and fall times would result provided decoupling is not used.

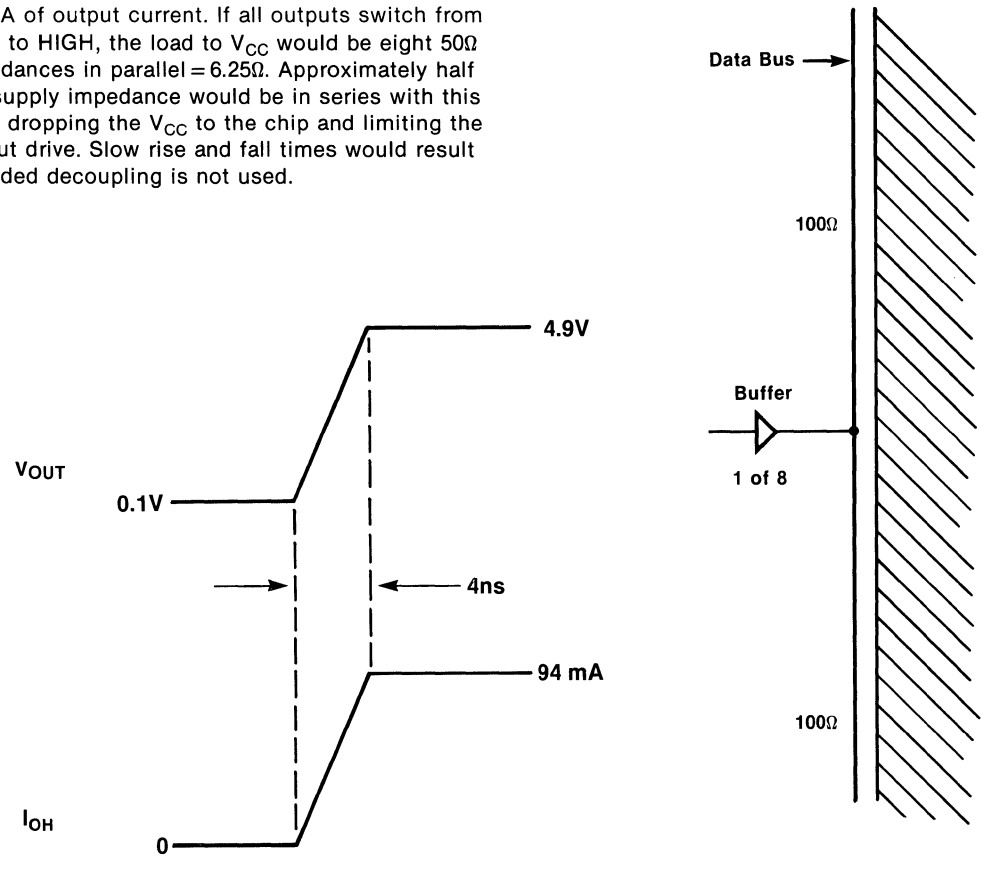


Figure 3-6

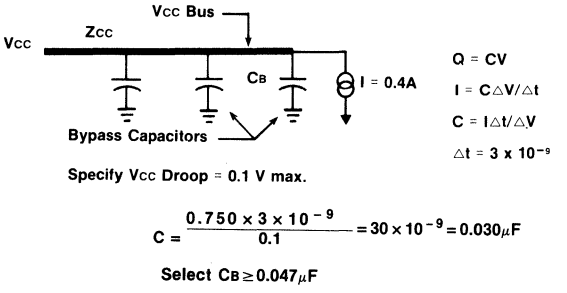
Worst-Case Octal Drain = 8 x 94 mA = 0.750 Amp.

Buffer Output Sees Net 50Ω Load.
50Ω Load Line on I_{OH}-V_{OH} Characteristic
Shows LOW-to-HIGH Step of Approx. 4.8V

Decoupling

Local high frequency decoupling is required to supply power to the chip during the LOW-to-HIGH transition, to charge the load capacitance or drive the load impedance.

A local decoupling capacitor may be used to supply the current to the load and maintain the voltage at the chip. The decoupling capacitor value can be calculated from the formula in Figure 3-7.



Good practice is to place one decoupling capacitor adjacent to each package driving any transmission line and distribute other capacitors evenly throughout the logic, one capacitor per three packages.

Figure 3-7

Capacitor Types

Decoupling capacitors for high-speed logic circuits should be of the high K ceramic type with a low ESR (equivalent series resistance), which is primarily made up of series inductance and series resistance internal to the capacitor. Capacitors using 5 ZU dielectric are a good choice for decoupling capacitors, thus giving minimum cost coupled with effective performance.

The high noise immunity of FACT insures that noise originating from ground is not a problem when interconnecting FACT packages; however, when interfacing to other logic families (e.g., Low Power Schottky), this will still be a problem and good ground layout is essential.

Interfacing Fairchild Advanced CMOS

Figure 3-8 AC to Bipolar

No special interface is required, provided both devices are operating with the same power supply.

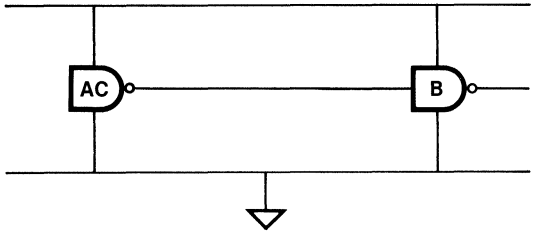


Figure 3-9 Bipolar to ACT

No special interface is required, provided both devices are operating with the same power supply.

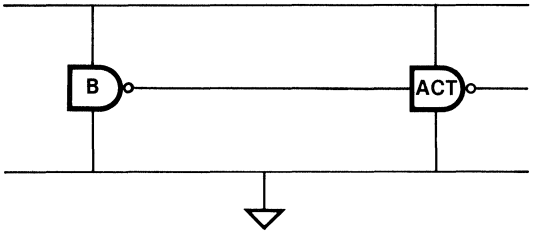


Figure 3-10 Bipolar to AC

A pull up resistor to V_{CC} of 4.7K Ω is required to establish V_{IH}.

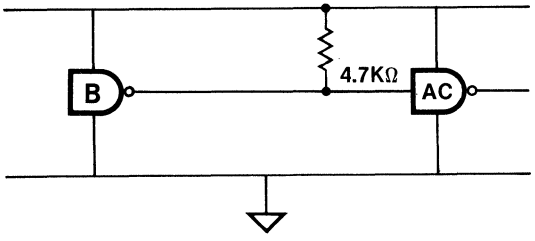


Figure 3-11 MOS to AC
No special interface is required, provided both devices are operating with the same power supply.

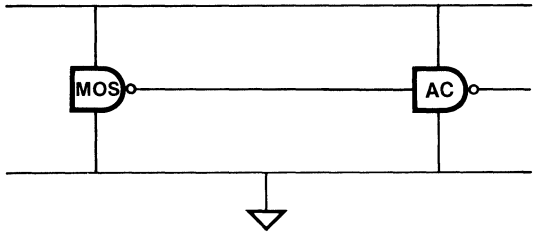


Figure 3-12 AC to MOS
No special interface is required, provided both devices are operating with the same power supply.

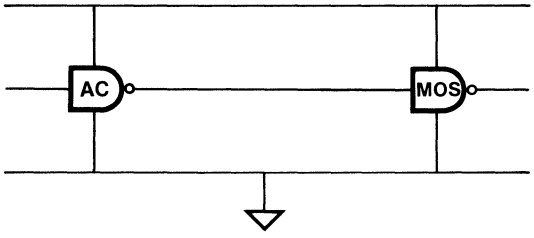


Figure 3-13 AC to 10K ECL
In this interfacing application the FACT power supply is 5 V. ECL power supply is −5.2 V, and the values for resistors are: R_1, 560 Ω; R_2, 510 Ω; R_3, 470 Ω.

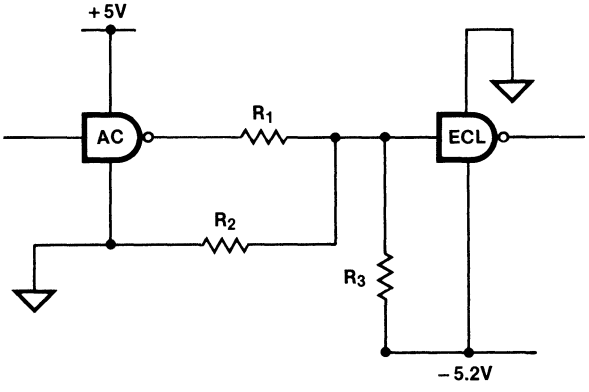
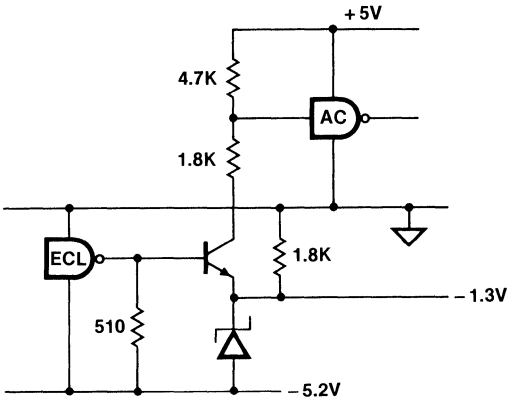
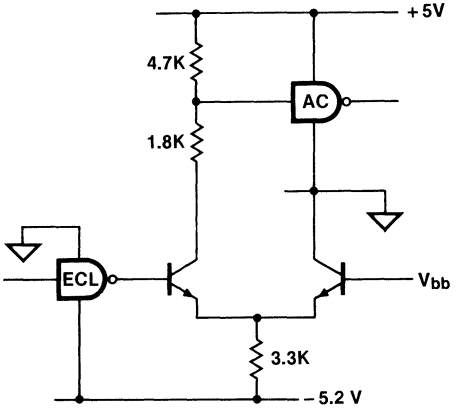


Figure 3-14 10K ECL to AC
Interfacing 10K ECL to ACMOS using +5 V and −5.2 V power rails requires the use of an ECL to TTL translator, 10125 (refer to Figure 3-10), or one of the two circuits shown below.





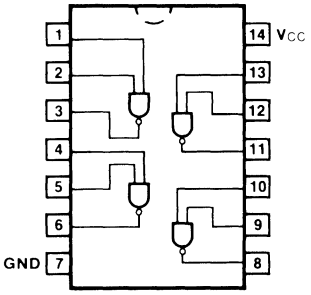
54AC/74AC00

Quad 2-Input NAND Gate

- **Outputs Source/Sink 24 mA**

Ordering Code: See Section 5

Connection Diagram



Pin Assignment for DIP and SOIC

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Quiescent Supply Current	100	50	μA	$V_{IN} = V_{CC}$ or Ground $V_{CC} = 5.5$ V

AC Characteristics

Symbol	Parameter	V_{CC}	54AC/74AC	54AC/74AC		54AC	74AC	Units
			Worst Case	$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°$ to $+85°C$ $C_L = 50$ pF	
			Min	Typ	Guaranteed Maximum			
t_{PLH}	Propagation Delay	3.0	1.0	6.0	9.5	11.0	10.0	ns
		4.5	1.0	5.0	8.0	8.5	8.5	
		5.5	1.0	5.0	8.0	8.5	8.5	
t_{PHL}	Propagation Delay	3.0	1.0	5.0	8.5	10.0	9.0	ns
		4.5	1.0	4.0	7.0	8.0	7.5	
		5.5	1.0	4.0	7.0	8.0	7.5	
C_{IN}	Input Capacitance	5.5		4.5				pF
C_{PD}	Power Dissipation Capacitance	5.5		20.0				pF

54AC/74AC74

Dual D-Type Positive Edge-Triggered Flip-Flop

Description

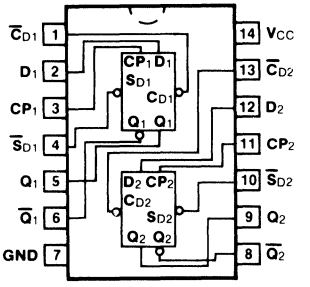
The 'AC74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:
- LOW input to $\overline{S}_D$ sets Q to HIGH level
- LOW input to $\overline{C}_D$ sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

•Outputs Source/Sink 24 mA

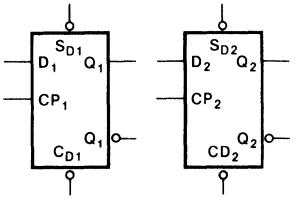
Ordering Code: See Section 5

Connection Diagram



Pin Assignment for DIP and SOIC

Logic Symbol



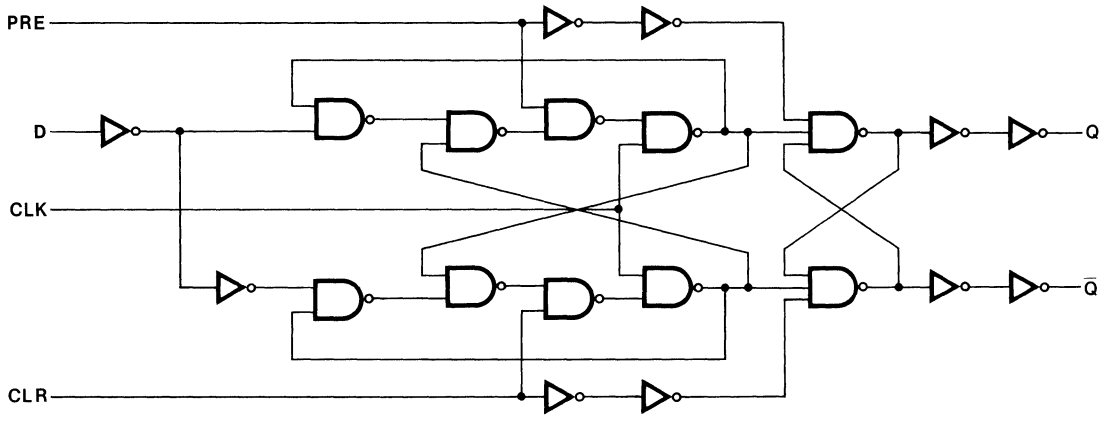
Truth Table

(Each Half)

Input	Outputs	
@ t_n	@ t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit Time before Clock Pulse
t_{n+1} = Bit Time after Clock Pulse

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Quiescent Supply Current	100	50	μA	$V_{IN} = V_{CC}$ or Ground $V_{CC} = 5.5$ V

AC Characteristics

Symbol	Parameter	V_{CC}	54AC/74AC	54AC/74AC		54AC	74AC	Units
			Worst Case	$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°$ to $+85°C$ $C_L = 50$ pF	
			Min	Typ	Guaranteed Maximum			
f_{max}	Maximum Clock Frequency	3.0 4.5 5.5	60.0 100.0 100.0	75.0 125.0 125.0				MHz
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.0 4.5 5.5	1.0 1.0 1.0	8.5 6.5 6.5	13.0 10.0 10.0	15.5 11.0 11.0	13.5 10.0 10.0	ns
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.0 4.5 5.5	1.0 1.0 1.0	8.5 6.5 6.5	14.0 10.0 10.0	16.0 11.5 11.5	14.5 10.5 10.5	ns

AC Characteristics (cont'd)

Symbol	Parameter	V_{CC}	54AC/74AC	54AC/74AC		54AC	74AC	Units
			Worst Case	$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°$ to $+85°C$ $C_L = 50$ pF	
			Min	Typ	Guaranteed Maximum			
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.0 4.5 5.5	1.0 1.0 1.0	8.0 6.0 6.0	12.0 9.0 9.0	14.5 10.5 10.5	13.0 10.0 10.0	ns
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.0 4.5 5.5	1.0 1.0 1.0	11.0 8.0 8.0	16.0 11.5 11.5	20.0 14.5 14.5	18.5 13.5 13.5	ns
C_{IN}	Input Capacitance			4.5				pF
C_{PD}	Power Dissipation Capacitance			25.0				pF

AC Operating Requirements

Symbol	Parameter	V_{CC}	54AC/74AC		54AC	74AC	Units
			$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°$ to $+85°C$ $C_L = 50$ pF	
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP_n	3.0 4.5 5.5	2.5 1.5 1.5	4.0 3.0 3.0	5.0 3.5 3.5	4.5 3.0 3.0	ns
t_h	Hold Time, HIGH or LOW D_n to CP_n	3.0 4.5 5.5	−2.0 −1.5 −1.5	0 0 0	0 0 0	0 0 0	ns
t_w	CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	3.0 4.5 5.5	3.0 2.5 2.5	5.5 4.5 4.5	8.0 5.5 5.5	7.0 5.0 5.0	ns
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	3.0 4.5 5.5	−3.0 −2.0 −2.0	0 0 0	0 0 0	0 0 0	ns

54AC/74AC109

Dual J$\overline{K}$ Positive Edge-Triggered Flip-Flop

Description

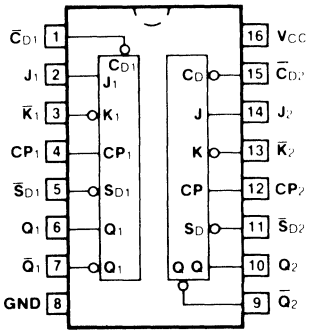
The 'AC109 consists of two high-speed, completely independent transition clocked J$\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The J$\overline{K}$ design allows operation as a D flip-flop (refer to 'AC74 data sheet) by connecting the J and $\overline{K}$ inputs together.

Asynchronous Inputs:
- LOW input to $\overline{S}_D$ sets Q to HIGH level
- LOW input to $\overline{C}_D$ sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

•Outputs Source/Sink 24 mA

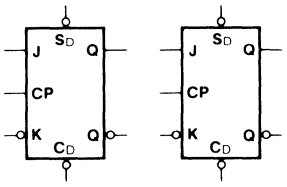
Ordering Code: See Section 5

Connection Diagram



Pin Assignment for DIP and SOIC

Logic Symbol

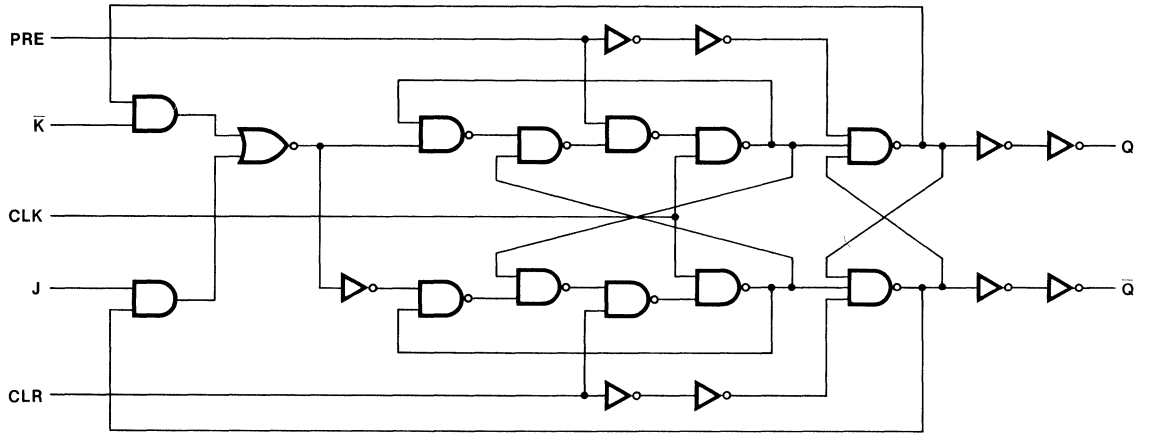


Truth Table

Inputs		Outputs	
@ t_n		@ t_{n+1}	
J	$\overline{K}$	Q	$\overline{Q}$
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit Time before Clock Pulse
t_{n+1} = Bit Time after Clock Pulse

Logic Diagram (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Quiescent Supply Current	100	50	μA	$V_{IN} = V_{CC}$ or Ground $V_{CC} = 5.5$ V

AC Characteristics

Symbol	Parameter	V_{CC}	54AC/74AC	54AC/74AC		54AC	74AC	Units
			Worst Case	$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°$ to $+85°C$ $C_L = 50$ pF	
			Min	Typ	Guaranteed Maximum			
f_{max}	Maximum Clock Frequency	3.0 4.5 5.5	30.0 50.0 50.0	50.0 75.0 75.0				MHz
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.0 4.5 5.5	1.0 1.0 1.0	8.5 6.5 6.5	13.0 10.0 10.0	15.5 11.0 11.0	13.5 10.0 10.0	ns
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.0 4.5 5.5	1.0 1.0 1.0	8.5 6.5 6.5	14.0 10.0 10.0	16.5 11.5 11.5	14.5 10.5 10.5	ns
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.0 4.5 5.5	1.0 1.0 1.0	8.0 6.0 6.0	12.0 9.0 9.0	14.5 10.5 10.5	13.0 10.0 10.0	ns

AC Characteristics (cont'd)

Symbol	Parameter	V_{CC}	54AC/74AC	54AC/74AC		54AC	74AC	Units
			Worst Case	$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°$ to $+85°C$ $C_L = 50$ pF	
			Min	Typ	Guaranteed Maximum			
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.0 4.5 5.5	1.0 1.0 1.0	11.0 8.0 8.0	16.0 11.5 11.5	20.0 14.5 14.5	18.5 13.5 13.5	ns
C_{IN}	Input Capacitance			4.5				pF
C_{PD}	Power Dissipation Capacitance			25.0				pF

AC Operating Requirements

Symbol	Parameter	V_{CC}	54AC/74AC		54AC	74AC	Units
			$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°$ to $+85°C$ $C_L = 50$ pF	
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.0 4.5 5.5	3.5 2.5 2.5	5.5 4.5 4.5	6.5 4.5 4.5	6.5 4.5 4.5	ns
t_h	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.0 4.5 5.5	−2.0 −1.5 −1.5	0 0 0	0 0 0	0 0 0	ns
t_w	CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	3.0 4.5 5.5	3.0 2.5 2.5	5.5 4.5 4.5	8.0 5.5 5.5	7.0 5.0 5.0	ns
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	3.0 4.5 5.5	−3.0 −2.0 −2.0	0 0 0	0 0 0	0 0 0	ns

54AC/74AC138

1-of-8 Decoder/Demultiplexer

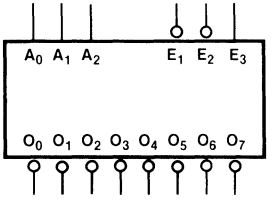
Description

The 'AC138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 'AC138 devices or a 1-of-32 decoder using four 'AC138 devices and one inverter.

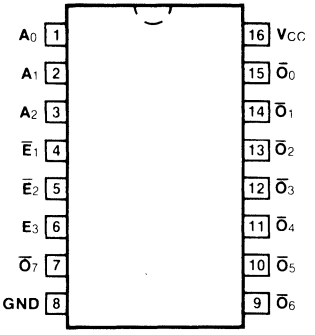
- **FACT Process for High Speed and Ultra Low Power**
- **Demultiplexing Capability**
- **Multiple Input Enable for Easy Expansion**
- **Active LOW Mutually Exclusive Outputs**
- **Outputs Source/Sink 24 mA**

Ordering Code: See Section 5

Logic Symbol



Connection Diagram



Pin Assignment for DIP and SOIC

Truth Table

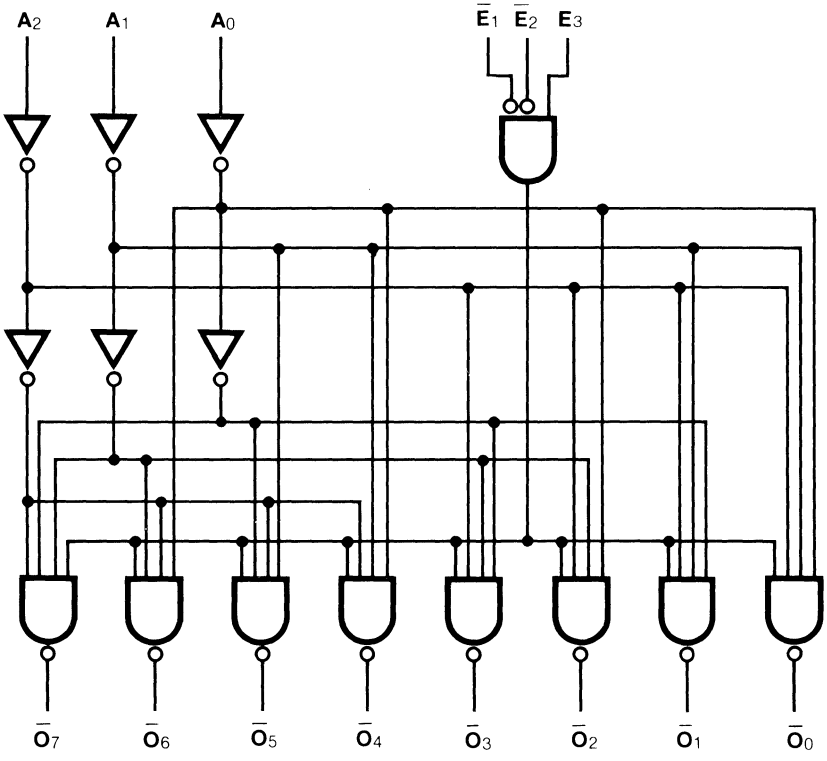
Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Functional Description

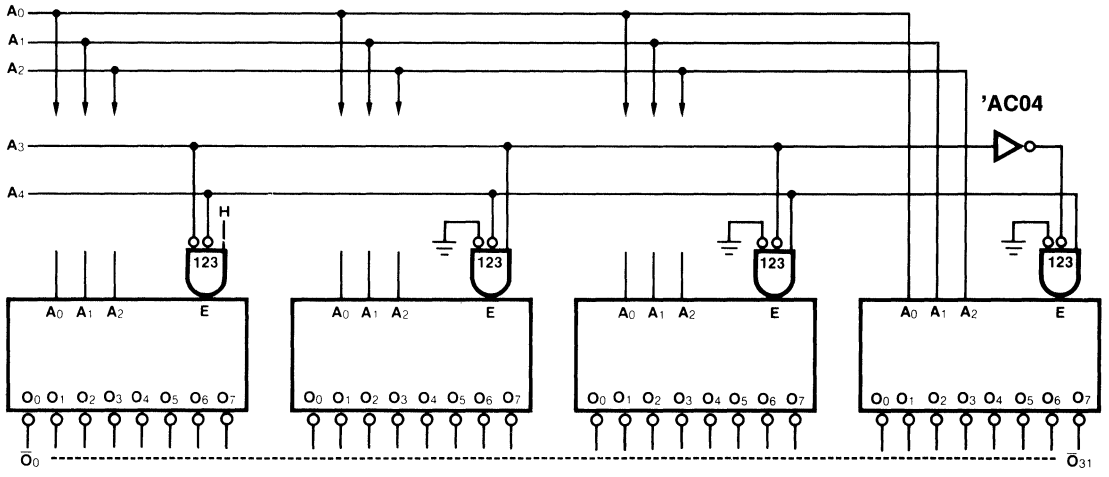
The 'AC138 high-speed 1-of-8 decoder/multiplexer accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_7$). The 'AC138 features three Enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 'AC138 devices and one inverter (See Figure a). The 'AC138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure a Expansion to 1-of-32 Decoding



DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Quiescent Supply Current	100	50	μA	$V_{IN} = V_{CC}$ or Ground $V_{CC} = 5.5$ V

AC Characteristics

Symbol	Parameter	V_{CC}	54AC/74AC	54AC/74AC		54AC	74AC	Units
			Worst Case	$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°$ to $+85°C$ $C_L = 50$ pF	
			Min	Typ	Guaranteed Maximum			
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	3.0 4.5 5.5	1.0 1.0 1.0	11.0 8.0 8.0	18.0 14.0 14.0	21.5 16.0 16.0	20.0 15.0 15.0	ns
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	3.0 4.5 5.5	1.0 1.0 1.0	9.5 7.0 7.0	16.5 12.5 12.5	19.5 14.5 14.5	18.0 13.5 13.5	ns
t_{PLH}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	3.0 4.5 5.5	1.0 1.0 1.0	12.5 9.5 9.5	20.0 15.0 15.0	24.5 18.0 18.0	22.5 16.5 16.5	ns
t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	3.0 4.5 5.5	1.0 1.0 1.0	11.0 8.0 8.0	17.0 12.5 12.5	20.0 14.5 14.5	18.5 13.5 13.5	ns
t_{PLH}	Propagation Delay $\overline{E}_3$ to $\overline{O}_n$	3.0 4.5 5.5	1.0 1.0 1.0	12.0 9.0 9.0	19.0 14.0 14.0	23.0 17.0 17.0	21.0 16.0 16.0	ns
t_{PHL}	Propagation Delay $\overline{E}_3$ to $\overline{O}_n$	3.0 4.5 5.5	1.0 1.0 1.0	10.0 7.0 7.0	15.5 11.0 11.0	18.5 13.5 13.5	17.5 12.5 12.5	ns
C_{IN}	Input Capacitance			4.5				pF
C_{PD}	Power Dissipation Capacitance			25.0				pF

54AC/74AC139

Dual 1-of-4 Decoder/Demultiplexer

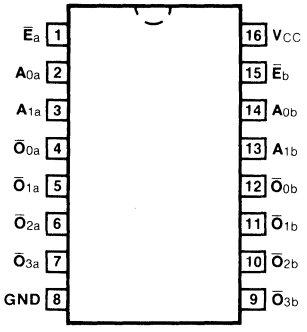
Description

The 'AC139 is a high-speed, dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the 'AC139 can be used as a function generator providing all four minterms of two variables.

- **Multifunction Capability**
- **Two Completely Independent 1-of-4 Decoders**
- **Active LOW Mutually Exclusive Outputs**
- **Outputs Source/Sink 24 mA**

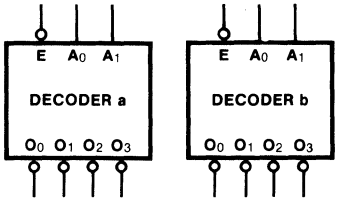
Ordering Code: See Section 5

Connection Diagram



Pin Assignment for DIP and SOIC

Logic Symbol



Truth Table

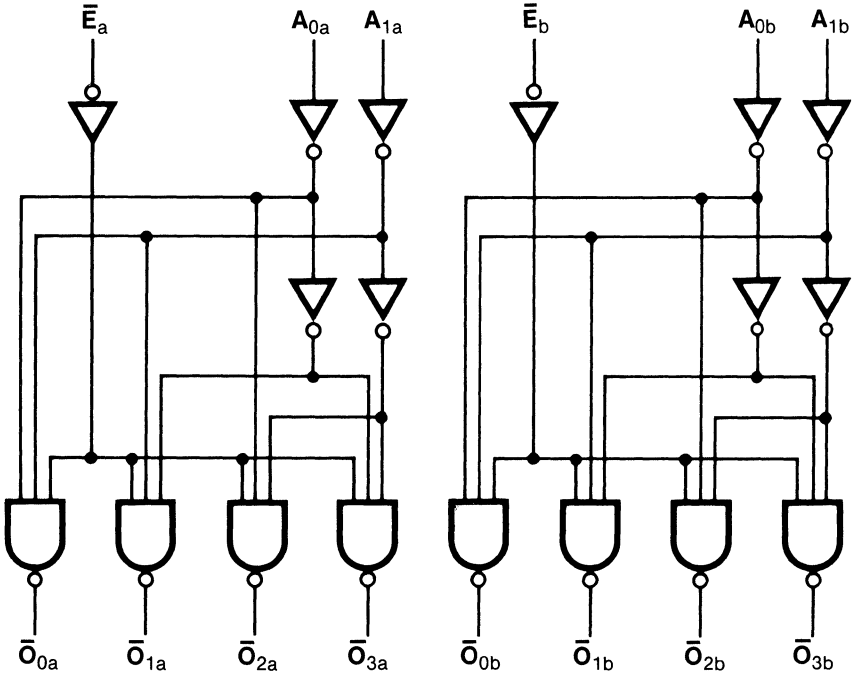
Inputs			Outputs			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Functional Description

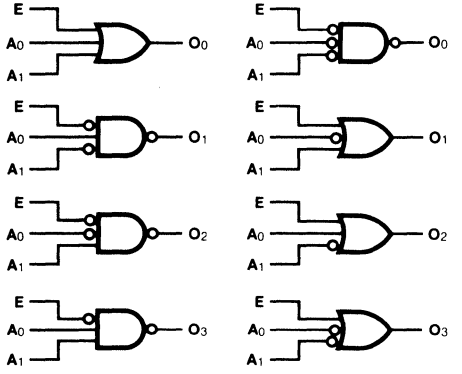
The 'AC139 is a high-speed dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each of which accepts two binary weighed inputs (A_0-A_1) and provides four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application. Each half of the 'AC139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Figure a, and thereby reducing the number of packages required in a logic network.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure a Gate Functions (each half)



DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Quiescent Supply Current	100	50	μA	$V_{IN} = V_{CC}$ or Ground $V_{CC} = 5.5$ V

AC Characteristics

Symbol	Parameter	V_{CC}	54AC/74AC	54AC/74AC		54AC	74AC	Units
			Worst Case	$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°$ to $+85°C$ $C_L = 50$ pF	
			Min	Typ	Guaranteed Maximum			
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	3.0 4.5 5.5	1.0 1.0 1.0	10.5 8.0 8.0	18.0 13.0 13.0	21.0 15.5 15.5	19.5 14.5 14.5	ns
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	3.0 4.5 5.5	1.0 1.0 1.0	8.5 6.5 6.5	14.5 11.5 11.5	17.5 13.5 13.5	16.0 12.5 12.5	ns
t_{PLH}	Propagation Delay $\overline{E}_n$ to $\overline{O}_n$	3.0 4.5 5.5	1.0 1.0 1.0	11.5 8.0 8.0	18.5 13.5 13.5	22.5 16.5 16.5	20.5 15.0 15.0	ns
t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{O}_n$	3.0 4.5 5.5	1.0 1.0 1.0	9.5 7.0 7.0	14.5 11.0 11.0	17.5 13.0 13.0	16.5 12.5 12.5	ns
C_{IN}	Input Capacitance			4.5				pF
C_{PD}	Power Dissipation Capacitance			25.0				pF

54AC/74AC153

Dual 4-Input Multiplexer

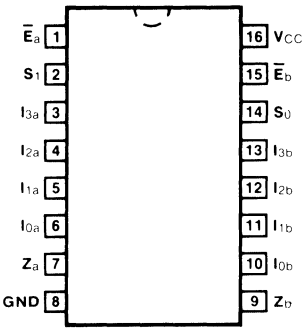
Description

The 'AC153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the 'AC153 can generate any two functions of three variables.

- **Outputs Source/Sink 24 mA**

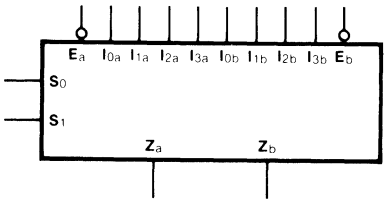
Ordering Code: See Section 5

Connection Diagram



Pin Assignment for DIP and SOIC

Logic Symbol



Truth Table

Select Inputs		Inputs (a or b)					Output
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Functional Description

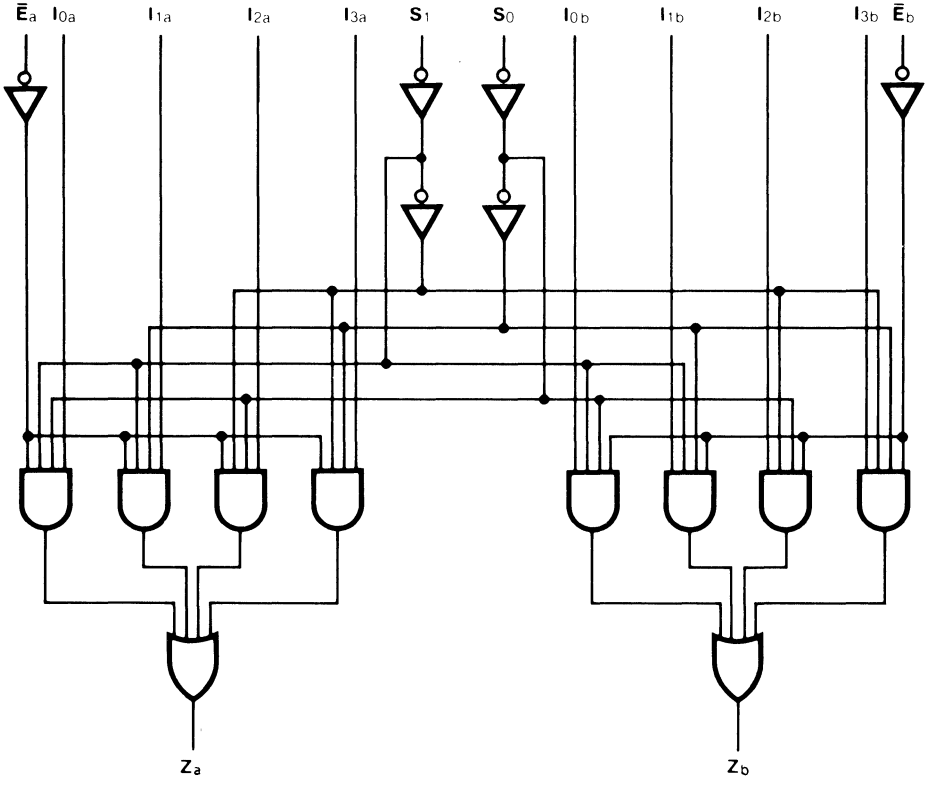
The 'AC153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW. The 'AC153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$Z_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

The 'AC153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is as a function generator. The 'AC153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Quiescent Supply Current	100	50	μA	$V_{IN} = V_{CC}$ or Ground $V_{CC} = 5.5$ V

AC Characteristics

Symbol	Parameter	V_{CC}	54AC/74AC	54AC/74AC		54AC	74AC	Units
			Worst Case	$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°$ to $+85°C$ $C_L = 50$ pF	
			Min	Typ	Guaranteed Maximum			
t_{PLH}	Propagation Delay S_n to Z_n	3.0 4.5 5.5	1.0 1.0 1.0	13.5 10.0 10.0	21.0 15.5 15.5	25.0 18.5 18.5	23.0 17.0 17.0	ns
t_{PHL}	Propagation Delay S_n to Z_n	3.0 4.5 5.5	1.0 1.0 1.0	18.5 13.5 13.5	28.0 20.5 20.5	33.5 24.5 24.5	31.0 23.0 23.0	ns
t_{PLH}	Propagation Delay $\overline{E}_n$ to Z_n	3.0 4.5 5.5	1.0 1.0 1.0	13.5 10.0 10.0	21.0 15.5 15.5	25.0 18.5 18.5	23.0 17.0 17.0	ns
t_{PHL}	Propagation Delay $\overline{E}_n$ to Z_n	3.0 4.5 5.5	1.0 1.0 1.0	22.0 16.0 16.0	33.0 24.5 24.5	40.0 29.0 29.0	37.0 27.0 27.0	ns
t_{PLH}	Propagation Delay I_n to Z_n	3.0 4.5 5.5	1.0 1.0 1.0	13.5 10.0 10.0	21.0 15.5 15.5	25.0 18.5 18.5	23.0 17.0 17.0	ns
t_{PHL}	Propagation Delay I_n to Z_n	3.0 4.5 5.5	1.0 1.0 1.0	13.0 9.5 9.5	20.0 14.5 14.5	23.5 17.5 17.5	22.0 16.0 16.0	ns
C_{IN}	Input Capacitance			4.5				pF
C_{PD}	Power Dissipation Capacitance			25.0				pF

54AC/74AC240

Octal Buffer/Line Driver With 3-State Outputs

Description

The 'AC240 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which provides improved PC board density.

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Outputs Source/Sink 24 mA**
- **Input Clamp Diodes Limit High-Speed Termination Effects**

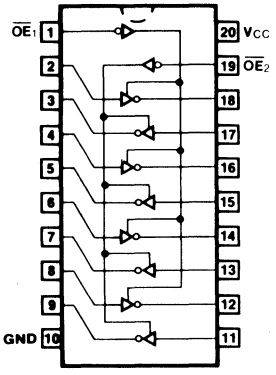
Ordering Code: See Section 5

Truth Table

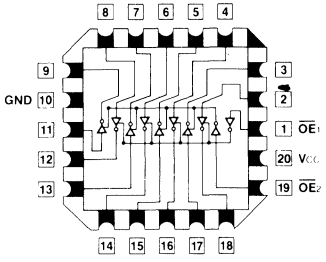
Inputs		Output
$\overline{OE}_1$, $\overline{OE}_2$	D	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Quiescent Supply Current	100	50	μA	$V_{IN} = V_{CC}$ or Ground $V_{CC} = 5.5$ V

AC Characteristics

Symbol	Parameter	V_{CC}	54AC/74AC	54AC/74AC		54AC	74AC	Units
			Worst Case	$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°$ to $+85°C$ $C_L = 50$ pF	
			Min	Typ	Guaranteed Maximum			
t_{PLH}	Propagation Delay Data to Output	3.0	1.0	8.0	12.5	15.0	14.0	ns
		4.5	1.0	6.0	9.5	11.0	10.5	
		5.5	1.0	6.0	9.5	11.0	10.5	
t_{PHL}	Propagation Delay Data to Output	3.0	1.0	7.5	11.5	14.0	13.0	ns
		4.5	1.0	5.5	8.5	10.0	9.5	
		5.5	1.0	5.5	8.5	10.0	9.5	
t_{PZH}	Output Enable Time	3.0	1.0	9.5	14.5	17.5	16.5	ns
		4.5	1.0	7.0	11.0	13.0	12.0	
		5.5	1.0	7.0	11.0	13.0	12.0	
t_{PZL}	Output Enable Time	3.0	1.0	9.5	14.5	17.5	16.5	ns
		4.5	1.0	7.0	11.0	13.0	12.0	
		5.5	1.0	7.0	11.0	13.0	12.0	
t_{PHZ}	Output Disable Time	3.0	1.0	11.0	16.5	20.0	18.5	ns
		4.5	1.0	8.0	12.5	14.5	13.5	
		5.5	1.0	8.0	12.5	14.5	13.5	
t_{PLZ}	Output Disable Time	3.0	1.0	9.0	13.5	16.5	15.0	ns
		4.5	1.0	6.5	10.0	12.0	11.0	
		5.5	1.0	6.5	10.0	12.0	11.0	
C_{IN}	Input Capacitance			4.5				pF
C_{PD}	Power Dissipation Capacitance			50.0				pF

54ACT/74ACT240

Octal Buffer/Line Driver With 3-State Outputs

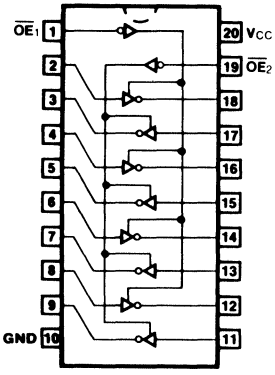
Description

The 'ACT240 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which provides improved PC board density.

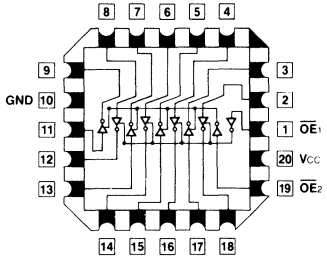
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Outputs Source/Sink 24 mA**
- **Input Clamp Diodes Limit High-Speed Termination Effects**
- **TTL Compatible Inputs**

Ordering Code: See Section 5

Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Truth Table

Inputs		Output
$\overline{OE}_1$, $\overline{OE}_2$	D	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54ACT	74ACT	Units	Conditions
I_{CC}	Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground $V_{CC} = 5.5$ V
ΔI_{CC}	I_{CC}/Input	3.0	2.9	mA	$V_{IN} = 2.4$ V or 0.4 V $V_{CC} = 5.5$ V

AC Characteristics

Symbol	Parameter	V_{CC}	54ACT/74ACT	54ACT/74ACT		54ACT	74ACT	Units
			Worst Case	$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°$ to $+85°C$ $C_L = 50$ pF	
			Min	Typ	Guaranteed Maximum			
t_{PLH}	Propagation Delay Data to Output	4.5 5.5	1.0 1.0	8.0 8.0	12.5 12.5	14.5 14.5	13.5 13.5	ns
t_{PHL}	Propagation Delay Data to Output	4.5 5.5	1.0 1.0	7.5 7.5	11.5 11.5	14.0 14.0	13.0 13.0	ns
t_{PZH}	Output Enable Time	4.5 5.5	1.0 1.0	9.0 9.0	14.0 14.0	16.5 16.5	15.5 15.5	ns
t_{PZL}	Output Enable Time	4.5 5.5	1.0 1.0	9.0 9.0	14.0 14.0	16.5 16.5	15.5 15.5	ns
t_{PHZ}	Output Disable Time	4.5 5.5	1.0 1.0	10.0 10.0	15.5 15.5	18.5 18.5	17.0 17.0	ns
t_{PLZ}	Output Disable Time	4.5 5.5	1.0 1.0	8.5 8.5	13.0 13.0	15.5 15.5	14.5 14.5	ns
C_{IN}	Input Capacitance			4.5				pF
C_{PD}	Power Dissipation Capacitance			50.0				pF

54AC/74AC241

Octal Buffer/Line Driver With 3-State Outputs

Description

The 'AC241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which provides improved PC board density.

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Outputs Source/Sink 24 mA**
- **Input Clamp Diodes Limit High-Speed Termination Effects**

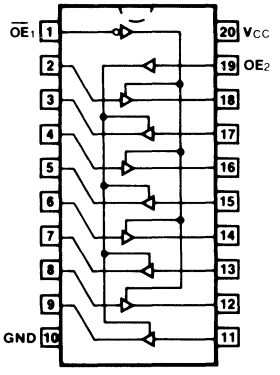
Ordering Code: See Section 5

Truth Table

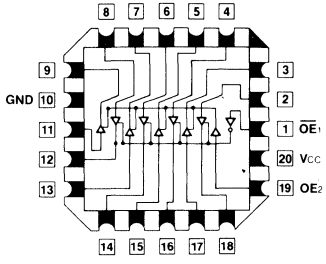
Inputs			Output
$\overline{OE}_1$	OE_2	D	
L	H	L	L
L	H	H	H
H	L	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Quiescent Supply Current	100	50	μA	$V_{IN} = V_{CC}$ or Ground $V_{CC} = 5.5$ V

AC Characteristics

Symbol	Parameter	V_{CC}	54AC/74AC	54AC/74AC		54AC	74AC	Units
			Worst Case	$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°$ to $+85°C$ $C_L = 50$ pF	
			Min	Typ	Guaranteed Maximum			
t_{PLH}	Propagation Delay Data to Output	3.0 4.5 5.5	1.0 1.0 1.0	8.0 6.0 6.0	12.5 9.5 9.5	15.0 11.0 11.0	14.0 10.5 10.5	ns
t_{PHL}	Propagation Delay Data to Output	3.0 4.5 5.5	1.0 1.0 1.0	7.5 5.5 5.5	11.5 8.5 8.5	14.0 10.0 10.0	13.0 9.5 9.5	ns
t_{PZH}	Output Enable Time	3.0 4.5 5.5	1.0 1.0 1.0	9.5 7.0 7.0	14.5 11.0 11.0	17.5 13.0 13.0	16.5 12.0 12.0	ns
t_{PZL}	Output Enable Time	3.0 4.5 5.5	1.0 1.0 1.0	9.5 7.0 7.0	14.5 11.0 11.0	17.5 13.0 13.0	16.5 12.0 12.0	ns
t_{PHZ}	Output Disable Time	3.0 4.5 5.5	1.0 1.0 1.0	11.0 8.0 8.0	16.5 12.5 12.5	20.0 14.5 14.5	18.5 13.5 13.5	ns
t_{PLZ}	Output Disable Time	3.0 4.5 5.5	1.0 1.0 1.0	9.0 6.5 6.5	13.5 10.0 10.0	16.5 12.0 12.0	15.0 11.0 11.0	ns
C_{IN}	Input Capacitance			4.5				pF
C_{PD}	Power Dissipation Capacitance			50.0				pF

54ACT/74ACT241

Octal Buffer/Line Driver With 3-State Outputs

Description

The 'ACT241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which provides improved PC board density.

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Outputs Source/Sink 24 mA**
- **Input Clamp Diodes Limit High-Speed Termination Effects**
- **TTL Compatible Inputs**

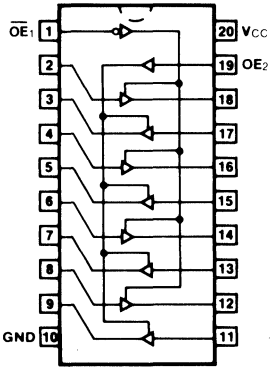
Ordering Code: See Section 5

Truth Table

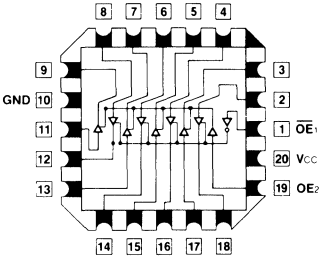
Inputs			Output
$\overline{OE}_1$	OE_2	D	
L	H	L	L
L	H	H	H
H	L	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54ACT	74ACT	Units	Conditions
I_{CC}	Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground $V_{CC} = 5.5$ V
ΔI_{CC}	I_{CC}/Input	3.0	2.9	mA	$V_{IN} = 2.4$ V or 0.4 V $V_{CC} = 5.5$ V

AC Characteristics

Symbol	Parameter	V_{CC}	54ACT/74ACT	54ACT/74ACT		54ACT	74ACT	Units
			Worst Case	$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°$ to $+85°C$ $C_L = 50$ pF	
			Min	Typ	Guaranteed Maximum			
t_{PLH}	Propagation Delay Data to Output	4.5 5.5	1.0 1.0	8.0 8.0	12.5 12.5	14.5 14.5	13.5 13.5	ns
t_{PHL}	Propagation Delay Data to Output	4.5 5.5	1.0 1.0	7.5 7.5	11.5 11.5	14.0 14.0	13.0 13.0	ns
t_{PZH}	Output Enable Time	4.5 5.5	1.0 1.0	9.0 9.0	14.0 14.0	16.5 16.5	15.5 15.5	ns
t_{PZL}	Output Enable Time	4.5 5.5	1.0 1.0	9.0 9.0	14.0 14.0	16.5 16.5	15.5 15.5	ns
t_{PHZ}	Output Disable Time	4.5 5.5	1.0 1.0	10.0 10.0	15.5 15.5	18.5 18.5	17.0 17.0	ns
t_{PLZ}	Output Disable Time	4.5 5.5	1.0 1.0	8.5 8.5	13.0 13.0	15.5 15.5	14.5 14.5	ns
C_{IN}	Input Capacitance			4.5				pF
C_{PD}	Power Dissipation Capacitance			50.0				pF

54AC/74AC244

Octal Buffer/Line Driver With 3-State Outputs

Description

The 'AC244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which provides improved PC board density.

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Outputs Source/Sink 24 mA**
- **Input Clamp Diodes Limit High-Speed Termination Effects**

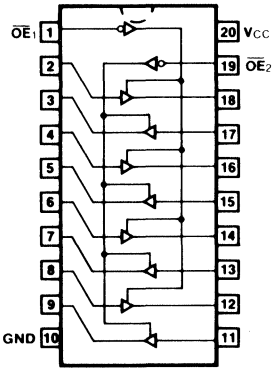
Ordering Code: See Section 5

Truth Table

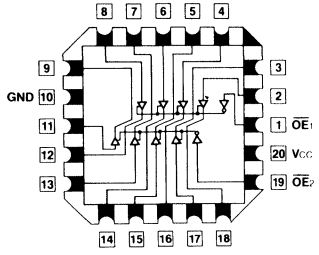
Inputs		Output
$\overline{OE}_1$, $\overline{OE}_2$	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Quiescent Supply Current	100	50	μA	$V_{IN} = V_{CC}$ or Ground $V_{CC} = 5.5$ V

AC Characteristics

Symbol	Parameter	V_{CC}	54AC/74AC	54AC/74AC		54AC	74AC	Units
			Worst Case	$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°$ to $+85°C$ $C_L = 50$ pF	
			Min	Typ	Guaranteed Maximum			
t_{PLH}	Propagation Delay Data to Output	3.0 4.5 5.5	1.0 1.0 1.0	8.0 6.0 6.0	12.5 9.5 9.5	15.5 11.0 11.0	14.0 10.5 10.5	ns
t_{PHL}	Propagation Delay Data to Output	3.0 4.5 5.5	1.0 1.0 1.0	7.5 5.5 5.5	11.5 8.5 8.5	14.0 10.0 10.0	13.0 9.5 9.5	ns
t_{PZH}	Output Enable Time	3.0 4.5 5.5	1.0 1.0 1.0	9.5 7.0 7.0	14.5 11.0 11.0	17.5 13.0 13.0	16.5 12.0 12.0	ns
t_{PZL}	Output Enable Time	3.0 4.5 5.5	1.0 1.0 1.0	9.5 7.0 7.0	14.5 11.0 11.0	17.5 13.0 13.0	16.5 12.0 12.0	ns
t_{PHZ}	Output Disable Time	3.0 4.5 5.5	1.0 1.0 1.0	11.0 8.0 8.0	16.5 12.5 12.5	20.0 14.5 14.5	18.5 13.5 13.5	ns
t_{PLZ}	Output Disable Time	3.0 4.5 5.5	1.0 1.0 1.0	9.0 6.5 6.5	13.5 10.0 10.0	16.5 12.0 12.0	15.0 11.0 11.0	ns
C_{IN}	Input Capacitance			4.5				pF
C_{PD}	Power Dissipation Capacitance			50.0				pF

54ACT/74ACT244

Octal Buffer/Line Driver With 3-State Outputs

Description

The 'ACT244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which provides improved PC board density.

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Outputs Source/Sink 24 mA**
- **Input Clamp Diodes Limit High-Speed Termination Effects**
- **TTL Compatible Inputs**

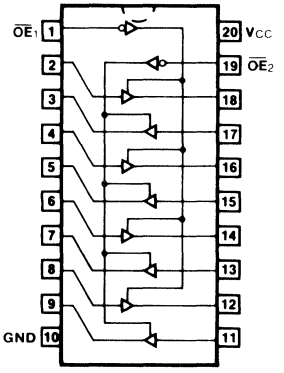
Ordering Code: See Section 5

Truth Table

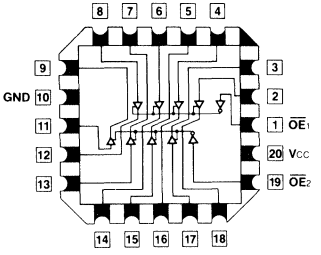
Inputs		Output
$\overline{OE}_1$, $\overline{OE}_2$	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54ACT	74ACT	Units	Conditions
I_{CC}	Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground $V_{CC} = 5.5$ V
ΔI_{CC}	I_{CC}/Input	3.0	2.9	mA	$V_{IN} = 2.4$ V or 0.4 V $V_{CC} = 5.5$ V

AC Characteristics

Symbol	Parameter	V_{CC}	54ACT/74ACT	54ACT/74ACT		54ACT	74ACT	Units
			Worst Case	$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°$ to $+85°C$ $C_L = 50$ pF	
			Min	Typ	Guaranteed Maximum			
t_{PLH}	Propagation Delay Data to Output	4.5 5.5	1.0 1.0	8.0 8.0	12.5 12.5	14.5 14.5	13.5 13.5	ns
t_{PHL}	Propagation Delay Data to Output	4.5 5.5	1.0 1.0	7.5 7.5	11.5 11.5	14.0 14.0	13.0 13.0	ns
t_{PZH}	Output Enable Time	4.5 5.5	1.0 1.0	9.0 9.0	14.0 14.0	16.5 16.5	15.5 15.5	ns
t_{PZL}	Output Enable Time	4.5 5.5	1.0 1.0	9.0 9.0	14.0 14.0	16.5 16.5	15.5 15.5	ns
t_{PHZ}	Output Disable Time	4.5 5.5	1.0 1.0	10.0 10.0	15.5 15.5	18.5 18.5	17.0 17.0	ns
t_{PLZ}	Output Disable Time	4.5 5.5	1.0 1.0	8.5 8.5	13.0 13.0	15.5 15.5	14.5 14.5	ns
C_{IN}	Input Capacitance			4.5				pF
C_{PD}	Power Dissipation Capacitance			50.0				pF

4

54AC/74AC245

Octal Bidirectional Transceiver With 3-State Inputs/Outputs

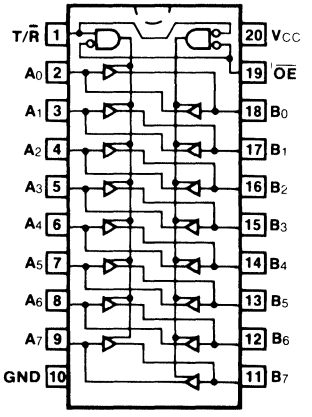
Description

The 'AC245 contains eight non-inverting bidirectional buffers with 3-state outputs and is intended for bus oriented applications. Current sinking capability is 24 mA at the A ports and 24 mA at the B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a High Z condition.

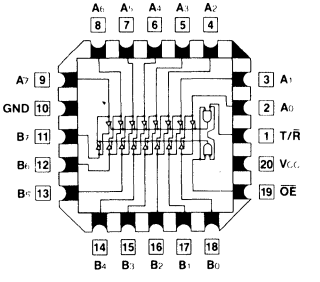
- **Non-Inverting Buffers**
- **Bidirectional Data Path**
- **A and B Outputs Sink 24 mA/Source −24 mA**

Ordering Code: See Section 5

Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Truth Table

Inputs		Output
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Quiescent Supply Current	100	50	μA	$V_{IN} = V_{CC}$ or Ground $V_{CC} = 5.5$ V

AC Characteristics

Symbol	Parameter	V_{CC}	54AC/74AC	54AC/74AC		54AC	74AC	Units
			Worst Case	$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°$ to $+85°C$ $C_L = 50$ pF	
			Min	Typ	Guaranteed Maximum			
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	3.0 4.5 5.5	1.0 1.0 1.0	8.0 6.0 6.0	12.5 9.5 9.5	15.0 11.0 11.0	14.0 10.5 10.5	ns
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	3.0 4.5 5.5	1.0 1.0 1.0	7.5 5.5 5.5	11.5 8.5 8.5	14.0 10.0 10.0	13.0 9.5 9.5	ns
t_{PZH}	Output Enable Time	3.0 4.5 5.5	1.0 1.0 1.0	9.5 7.0 7.0	14.5 11.0 11.0	17.5 13.0 13.0	16.5 12.0 12.0	ns
t_{PZL}	Output Enable Time	3.0 4.5 5.5	1.0 1.0 1.0	9.5 7.0 7.0	14.5 11.0 11.0	17.5 13.0 13.0	16.5 12.0 12.0	ns
t_{PHZ}	Output Disable Time	3.0 4.5 5.5	1.0 1.0 1.0	11.0 8.0 8.0	16.5 12.5 12.5	20.0 14.5 14.5	18.5 13.5 13.5	ns
t_{PLZ}	Output Disable Time	3.0 4.5 5.5	1.0 1.0 1.0	9.0 6.5 6.5	13.5 10.0 10.0	16.5 12.0 12.0	15.0 11.0 11.0	ns
C_{IN}	Input Capacitance			4.5				pF
$C_{I/O}$	Input/Output Capacitance			15.0				pF
C_{PD}	Power Dissipation Capacitance			50.0				pF

54AC/74AC253

Dual 4-Input Multiplexer With 3-State Outputs

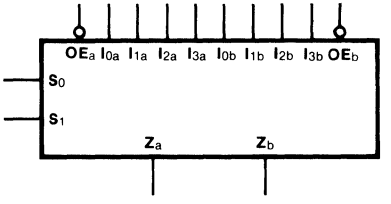
Description

The 'AC253 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

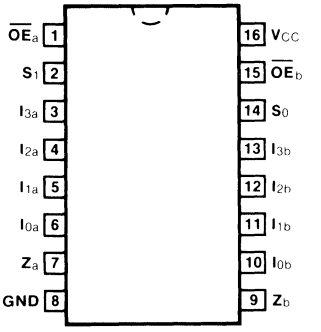
- **FACT Process for High Speed and Ultra Low Power**
- **Multifunction Capability**
- **Non-Inverting 3-State Outputs**
- **Outputs Source/Sink 24 mA**

Ordering Code: See Section 5

Logic Symbol



Connection Diagram



Pin Assignment for DIP and SOIC

Functional Description

This device contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$Z_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

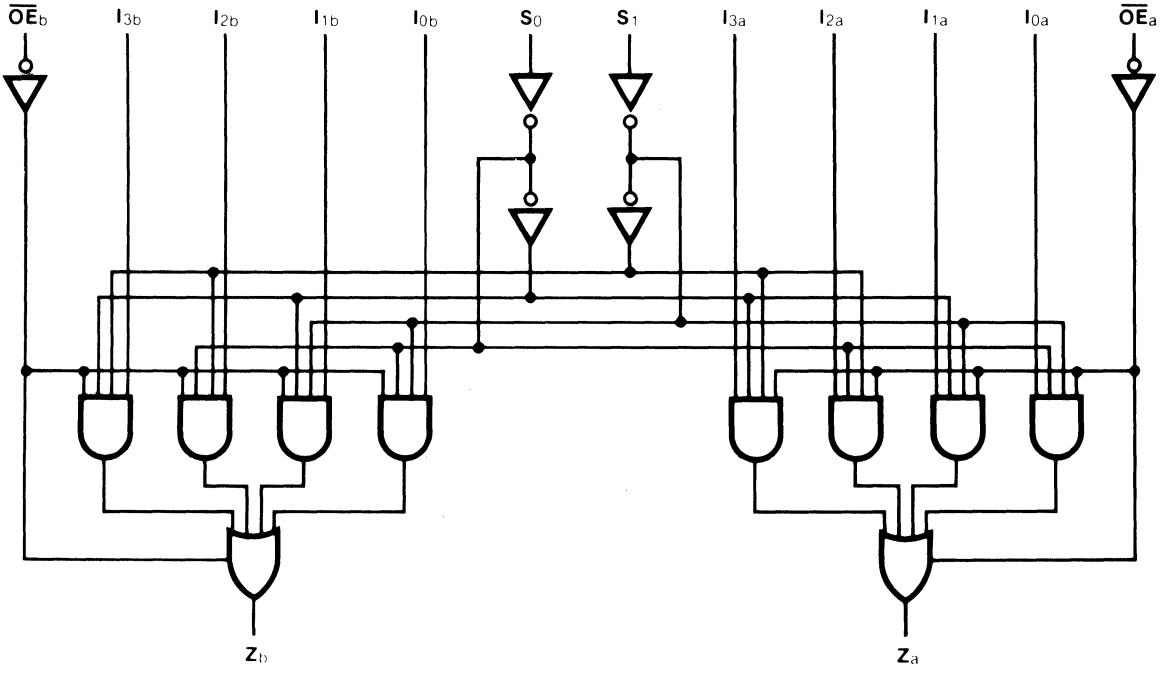
If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

Truth Table

Select Inputs		Data Inputs				Output Enable	Output
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs S_0 and S_1 are common to both sections.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Quiescent Supply Current	100	50	μA	$V_{IN} = V_{CC}$ or Ground $V_{CC} = 5.5$ V

AC Characteristics

Symbol	Parameter	V_{CC}	54AC/74AC	54AC/74AC		54AC	74AC	Units
			Worst Case	$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°$ to $+85°C$ $C_L = 50$ pF	
			Min	Typ	Guaranteed Maximum			
t_{PLH}	Propagation Delay S_n to Z_n	3.0	1.0	16.5	25.0	30.0	27.5	ns
		4.5	1.0	12.0	18.5	22.0	20.5	
		5.5	1.0	12.0	18.5	22.0	20.5	
t_{PHL}	Propagation Delay S_n to Z_n	3.0	1.0	20.5	31.0	37.5	34.5	ns
		4.5	1.0	15.0	23.0	27.5	25.5	
		5.5	1.0	15.0	23.0	27.5	25.5	
t_{PLH}	Propagation Delay I_n to Z_n	3.0	1.0	14.5	22.0	26.0	24.5	ns
		4.5	1.0	10.5	16.0	19.0	18.0	
		5.5	1.0	10.5	16.0	19.0	18.0	
t_{PHL}	Propagation Delay I_n to Z_n	3.0	1.0	16.0	24.0	28.5	26.5	ns
		4.5	1.0	11.5	17.5	21.0	19.5	
		5.5	1.0	11.5	17.5	21.0	19.5	
t_{PZL}	Output Enable Time	3.0	1.0	7.0	10.5	12.5	11.5	ns
		4.5	1.0	5.0	8.0	9.5	8.5	
		5.5	1.0	5.0	8.0	9.5	8.5	
t_{PZH}	Output Enable Time	3.0	1.0	9.0	13.5	16.5	15.0	ns
		4.5	1.0	6.5	10.0	12.0	11.0	
		5.5	1.0	6.5	10.0	12.0	11.0	
t_{PHZ}	Output Disable Time	3.0	1.0	9.0	13.5	16.5	15.0	ns
		4.5	1.0	6.5	10.0	12.0	11.0	
		5.5	1.0	6.5	10.0	12.0	11.0	
t_{PLZ}	Output Disable Time	3.0	1.0	7.0	10.5	12.5	11.5	ns
		4.5	1.0	5.0	8.0	9.5	8.5	
		5.5	1.0	5.0	8.0	9.5	8.5	
C_{IN}	Input Capacitance			4.5				pF
C_{PD}	Power Dissipation Capacitance			25.0				pF

54AC/74AC373

Octal Transparent Latch With 3-State Outputs

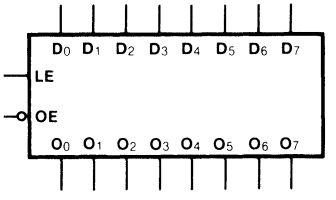
Description

The 'AC373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

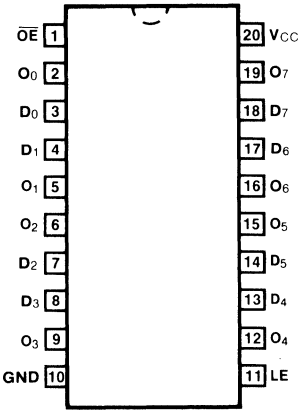
- **Eight Latches in a Single Package**
- **3-State Outputs for Bus Interfacing**
- **Outputs Source/Sink 24 mA**

Ordering Code: See Section 5

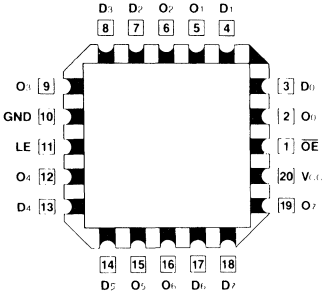
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

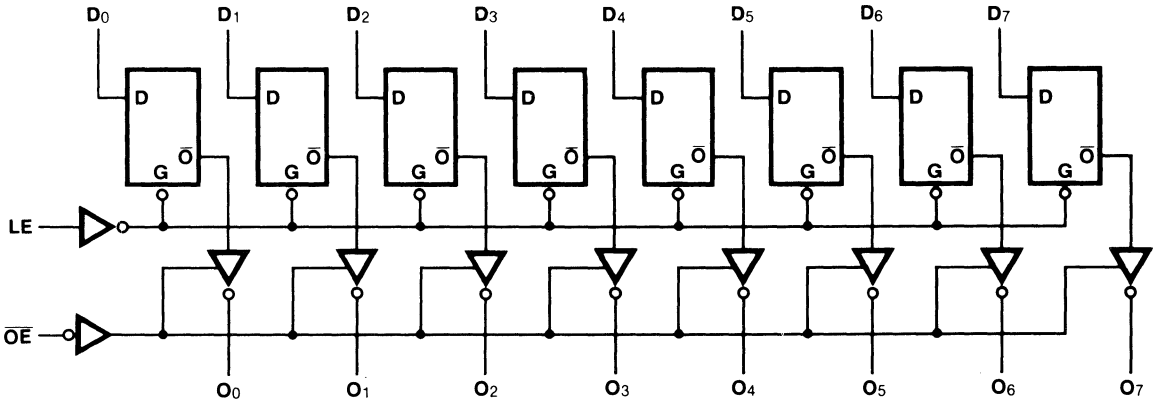


Pin Assignment for LCC and PCC

Functional Description

The 'AC373 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the 2-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Quiescent Supply Current	100	50	μA	$V_{IN} = V_{CC}$ or Ground $V_{CC} = 5.5$ V

AC Characteristics

Symbol	Parameter	V_{CC}	54AC/74AC	54AC/74AC		54AC	74AC	Units
			Worst Case	$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°$ to $+85°C$ $C_L = 50$ pF	
			Min	Typ	Guaranteed Maximum			
t_{PLH}	Propagation Delay D_n to O_n	3.0 4.5 5.5	1.0 1.0 1.0	9.0 6.5 6.5	13.5 10.0 10.0	16.5 12.0 12.0	15.0 11.0 11.0	ns
t_{PHL}	Propagation Delay D_n to O_n	3.0 4.5 5.5	1.0 1.0 1.0	8.0 6.0 6.0	12.5 9.5 9.5	15.0 11.0 11.0	14.0 10.5 10.5	ns
t_{PLH}	Propagation Delay LE to O_n	3.0 4.5 5.5	1.0 1.0 1.0	9.0 6.5 6.5	13.5 10.0 10.0	16.5 12.0 12.0	15.0 11.0 11.0	ns
t_{PHL}	Propagation Delay LE to O_n	3.0 4.5 5.5	1.0 1.0 1.0	8.0 6.0 6.0	12.5 9.5 9.5	15.0 11.0 11.0	14.0 10.5 10.5	ns
t_{PZH}	Output Enable Time	3.0 4.5 5.5	1.0 1.0 1.0	9.5 7.0 7.0	14.5 11.0 11.0	17.5 13.0 13.0	16.5 12.0 12.0	ns
t_{PZL}	Output Enable Time	3.0 4.5 5.5	1.0 1.0 1.0	9.5 7.0 7.0	14.5 11.0 11.0	17.5 13.0 13.0	16.5 12.0 12.0	ns
t_{PHZ}	Output Disable Time	3.0 4.5 5.5	1.0 1.0 1.0	12.5 9.0 9.0	19.0 14.0 14.0	22.5 16.5 16.5	21.0 15.5 15.5	ns
t_{PLZ}	Output Disable Time	3.0 4.5 5.5	1.0 1.0 1.0	9.5 7.0 7.0	14.5 11.0 11.0	17.5 13.0 13.0	16.5 12.0 12.0	ns
C_{IN}	Input Capacitance			4.5				pF
C_{PD}	Power Dissipation Capacitance			30.0				pF

AC Operating Requirements

Symbol	Parameter	V_{CC}	54AC/74AC		54AC	74AC	Units
			$T_A = +25°C$, $C_L = 50$ pF		$T_A = -55°$ to $+125°C$, $C_L = 50$ pF	$T_A = -40°$ to $+85°C$, $C_L = 50$ pF	
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	3.0	3.5	5.5	6.5	6.0	ns
		4.5	2.5	4.0	5.0	4.5	
		5.5	2.5	4.0	5.0	4.5	
t_h	Hold Time, HIGH or LOW D_n to LE	3.0	0	0	0	0	ns
		4.5	0	0	0	0	
		5.5	0	0	0	0	
$t_w(H)$	LE Pulse Width, HIGH	3.0	3.5	5.5	6.5	6.0	ns
		4.5	2.5	4.0	5.0	4.5	
		5.5	2.5	4.0	5.0	4.5	

54AC/74AC374

Octal D-Type Flip-Flop With 3-State Outputs

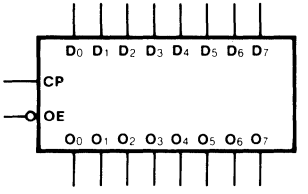
Description

The 'AC374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

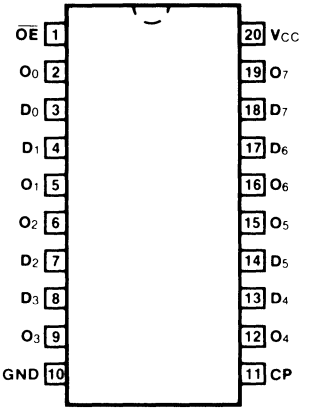
- **Edge-Triggered D-Type Inputs**
- **Buffered Positive Edge-Triggered Clock**
- **3-State Outputs for Bus Oriented Applications**
- **Outputs Source/Sink 24 mA**

Ordering Code: See Section 5

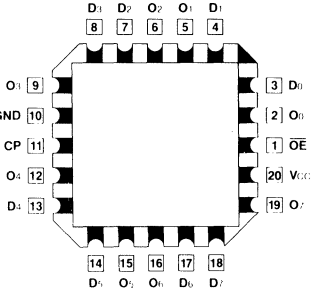
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Functional Description

The 'AC374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

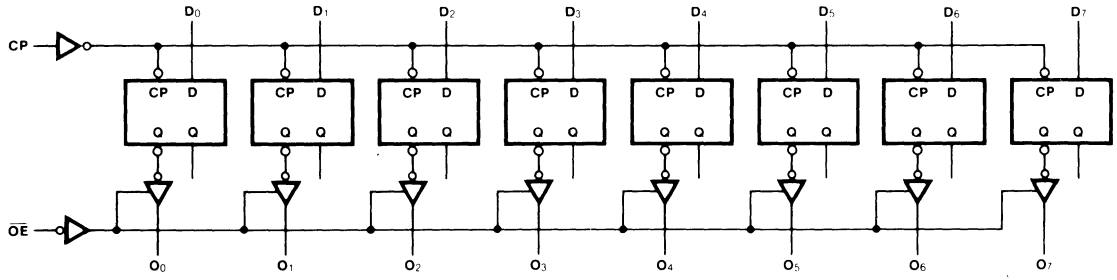
Truth Table

Inputs		Outputs	
D_n	CP	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

4

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Quiescent Supply Current	100	50	μA	$V_{IN} = V_{CC}$ or Ground $V_{CC} = 5.5$ V

AC Characteristics

Symbol	Parameter	V_{CC}	54AC/74AC	54AC/74AC		54AC	74AC	Units
			Worst Case	$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°$ to $+85°C$ $C_L = 50$ pF	
			Min	Typ	Guaranteed Maximum			
f_{max}	Maximum Clock Frequency	3.0 4.5 5.5	60.0 100.0	75.0 125.0 125.0				MHz
t_{PLH}	Propagation Delay CP to O_n	3.0 4.5 5.5	1.0 1.0 1.0	9.0 6.5 6.5	13.5 10.0 10.0	16.5 12.0 12.0	15.0 11.0 11.0	ns
t_{PHL}	Propagation Delay CP to O_n	3.0 4.5 5.5	1.0 1.0 1.0	8.0 6.0 6.0	12.5 9.5 9.5	15.0 11.0 11.0	14.0 10.5 10.5	ns
t_{PZH}	Output Enable Time	3.0 4.5 5.5	1.0 1.0 1.0	9.5 7.0 7.0	14.5 11.0 11.0	17.5 13.0 13.0	16.5 12.0 12.0	ns
t_{PZL}	Output Enable Time	3.0 4.5 5.5	1.0 1.0 1.0	9.5 7.0 7.0	14.5 11.0 11.0	17.5 13.0 13.0	16.5 12.0 12.0	ns
t_{PHZ}	Output Disable Time	3.0 4.5 5.5	1.0 1.0 1.0	12.5 9.0 9.0	19.0 14.0 14.0	22.5 16.5 16.5	21.0 15.5 15.5	ns
t_{PLZ}	Output Disable Time	3.0 4.5 5.5	1.0 1.0 1.0	9.5 7.0 7.0	14.5 11.0 11.0	17.5 13.0 13.0	16.5 12.0 12.0	ns
C_{IN}	Input Capacitance			4.5				pF
C_{PD}	Power Dissipation Capacitance			30.0				pF

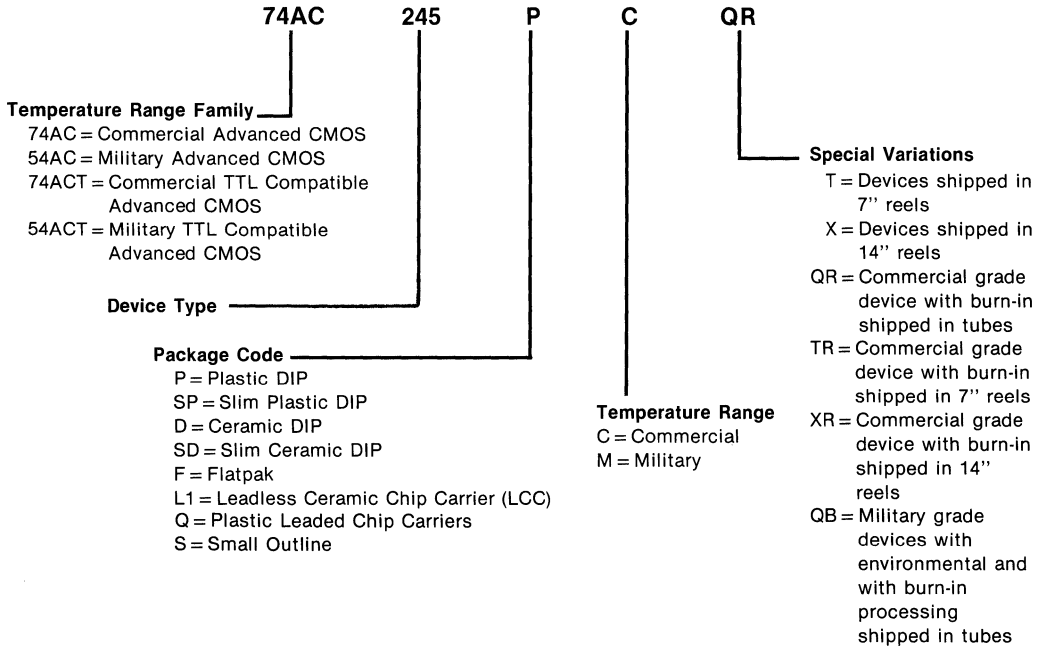
AC Operating Requirements

Symbol	Parameter	V_{CC}	54AC/74AC		54AC	74AC	Units
			$T_A = +25°C$, $C_L = 50$ pF		$T_A = -55°$ to $+125°C$, $C_L = 50$ pF	$T_A = -40°$ to $+85°C$, $C_L = 50$ pF	
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	3.0	3.5	5.5	6.5	6.0	ns
		4.5	2.5	4.0	5.0	4.5	
		5.5	2.5	4.0	5.0	4.5	
t_h	Hold Time, HIGH or LOW D_n to CP	3.0	0	0	0	0	ns
		4.5	0	0	0	0	
		5.5	0	0	0	0	
t_w	CP Pulse Width HIGH or LOW	3.0	3.5	5.5	6.5	6.0	ns
		4.5	2.5	4.0	5.0	4.5	
		5.5	2.5	4.0	5.0	4.5	

FAIRCHILD
A Schlumberger Company

Ordering Information/ Package Outlines

The Product Index and Selection Guide in Section 1 lists only the basic device numbers. This basic number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Package	Package Code
Plastic DIP	P
Slim Plastic DIP	SP
Ceramic DIP	D
Slim Ceramic DIP	SD
Flatpak	F
Leadless Ceramic Chip Carrier (LCC)	L1
Plastic Chip Carrier (PCC)	Q
Small Outline	S

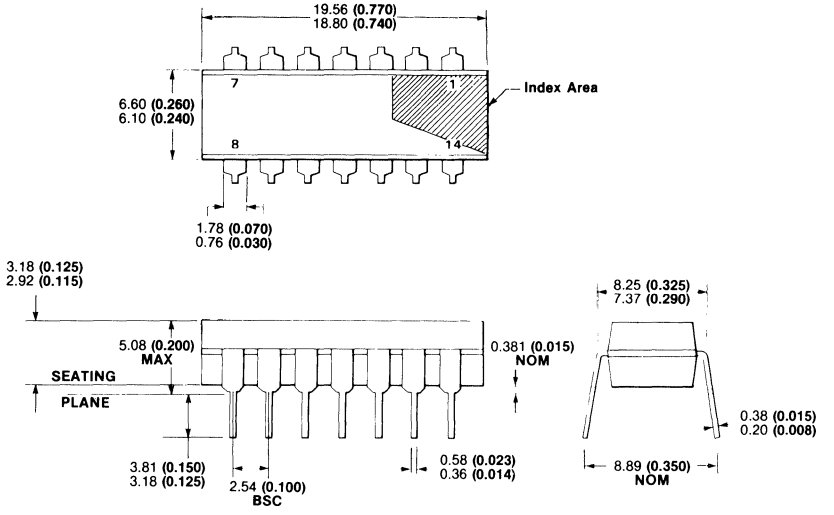
Temperature Range	Temperature Code
Commercial −40°C to +85°C	C
Military −55°C to +125°C	M

Package Outlines

The package outlines indicated above are shown in the detailed outline drawings in this section.

14 Lead Plastic Dual In-Line

Ordering Code: 74ACXXXPC
74ACTXXXPC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 7.620 **(0.300)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Package weight is 0.9 gram.

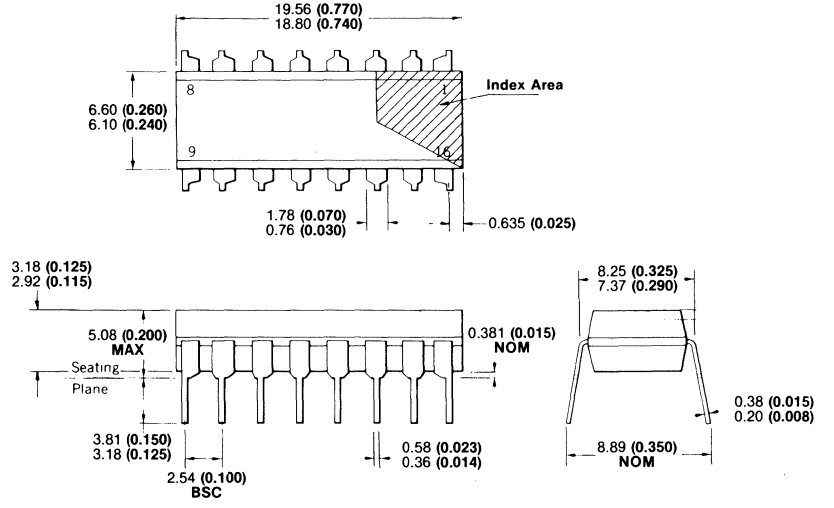
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

16 Lead Plastic Dual In-Line

Ordering Code: 74ACXXXPC
74ACTXXXPC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 7.620 **(0.300)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Package weight is 0.9 gram.

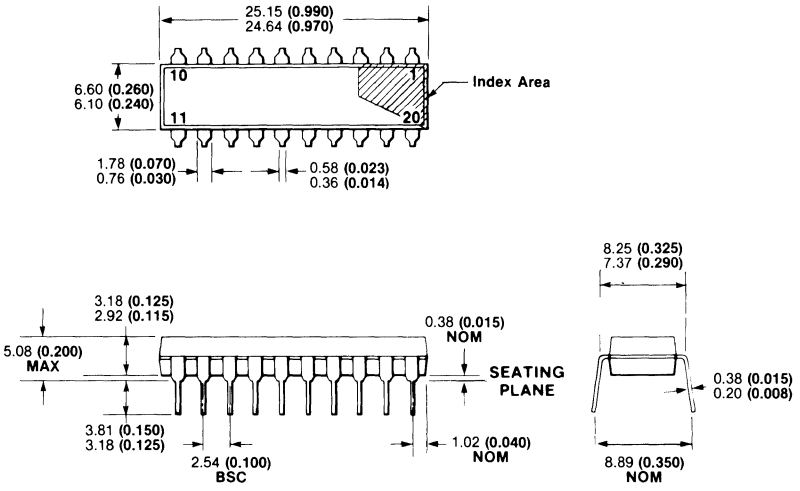
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

20 Lead Plastic Dual In-Line

Ordering Code: 74ACXXXPC
74ACTXXXPC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 7.620 **(0.300)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

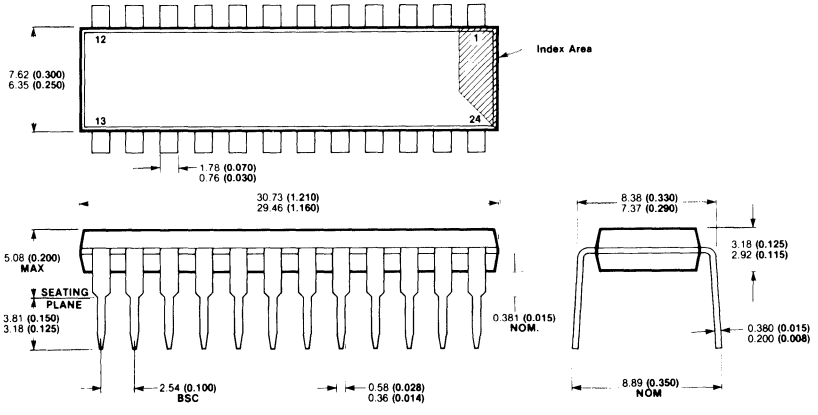
Package weight is 1.2 grams.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

24 Lead Slim (0.300" Wide) Plastic Dual In-Line

Ordering Code: 74ACXXXSPC
74ACTXXXSPC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 7.620 **(0.300)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

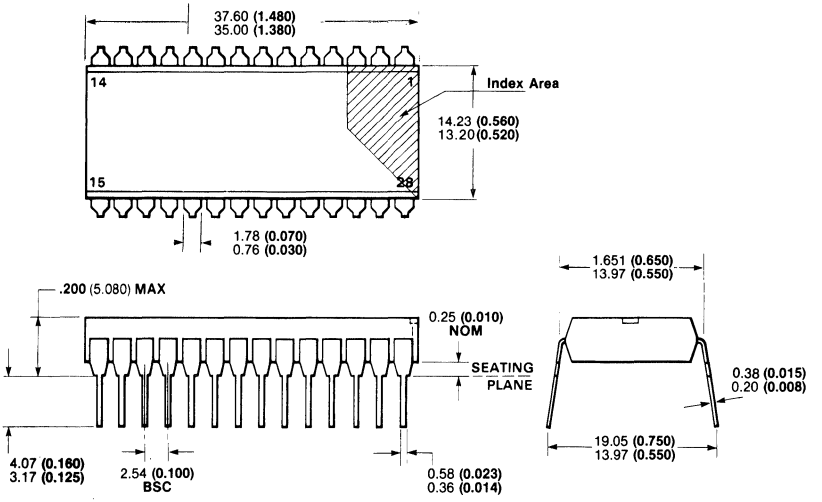
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

28 Lead Plastic Dual In-Line

Ordering Code: 74ACXXXPC
74ACTXXXPC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 15.400 **(0.600)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

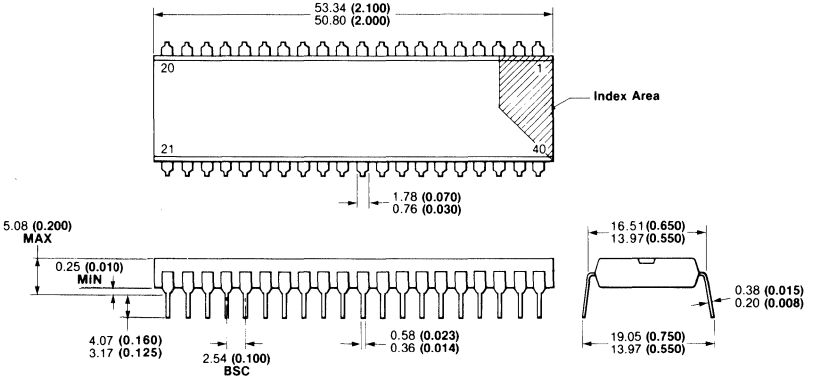
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

40 Lead Plastic Dual In-Line

Ordering Code: 74ACXXXPC
74ACTXXXPC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 15.240 **(0.600)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

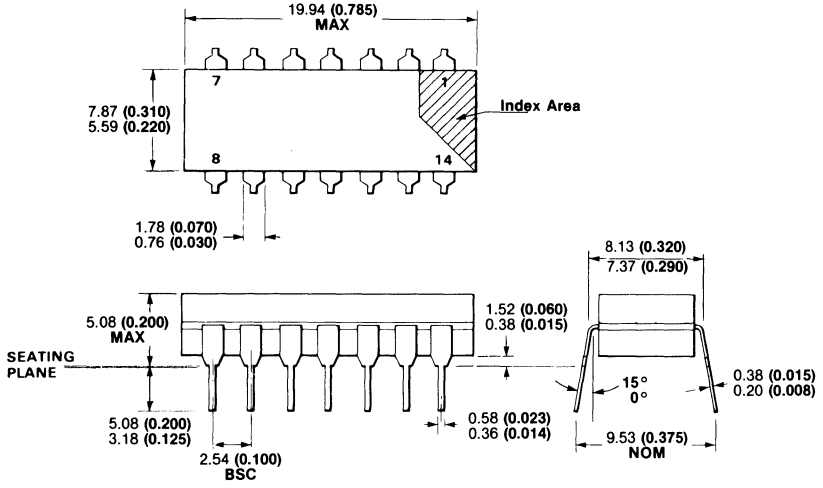
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

14 Lead Ceramic Dual In-Line

Ordering Codes: 74ACXXXDC
74ACTXXXDC
54ACXXXDM
54ACTXXXDM



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 7.620 **(0.300)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are alloy 42, either tin plated or solder coated.

Package is hermetically sealed alumina (black).

Package weight is 2.0 grams.

All dimensions are typical unless otherwise specified.

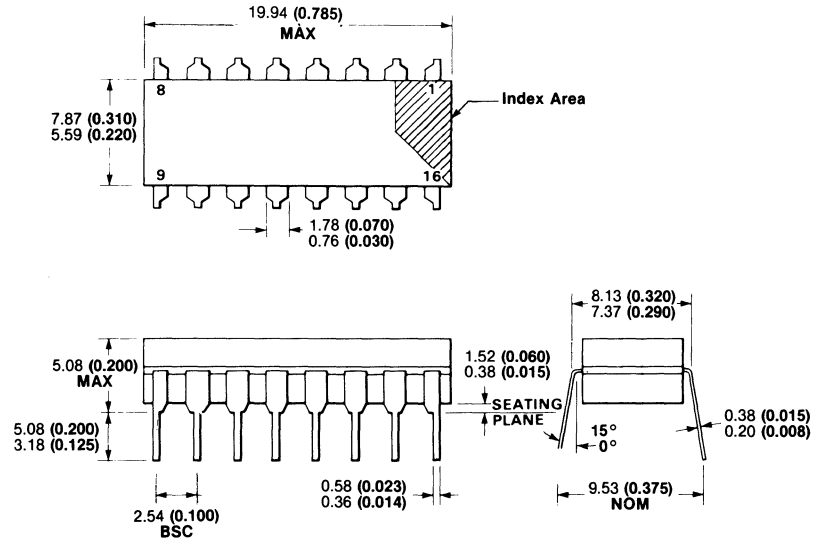
Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

5

16 Lead Ceramic Dual In-Line

Ordering Codes: 74ACXXXDC
74ACTXXXDC
54ACXXXDM
54ACTXXXDM



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 7.620 **(0.300)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are alloy 42, either tin plated or solder coated.

Package is hermetically sealed alumina (black).

Package weight is 2.2 grams.

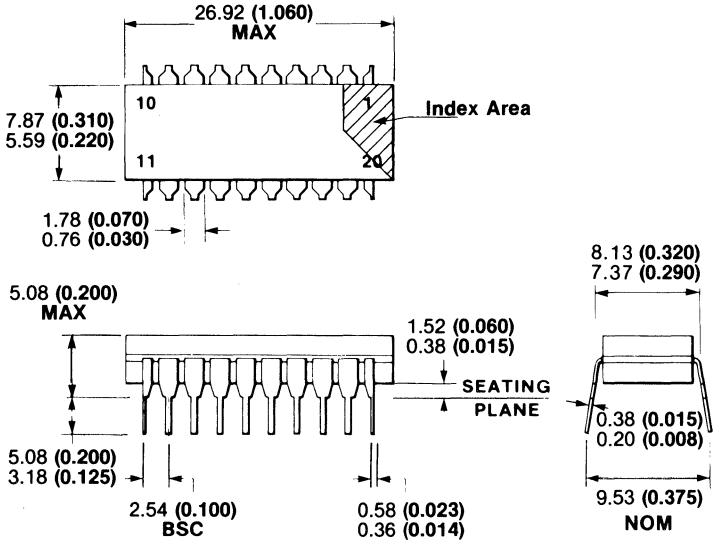
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

20 Lead Ceramic Dual In-Line

Ordering Codes: 74ACXXXDC
74ACTXXXDC
54ACXXXDM
54ACTXXXDM



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 7.620 **(0.300)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are alloy 42, either tin plated or solder coated.

Package is hermetically sealed alumina (black).

Package weight is 2.4 grams.

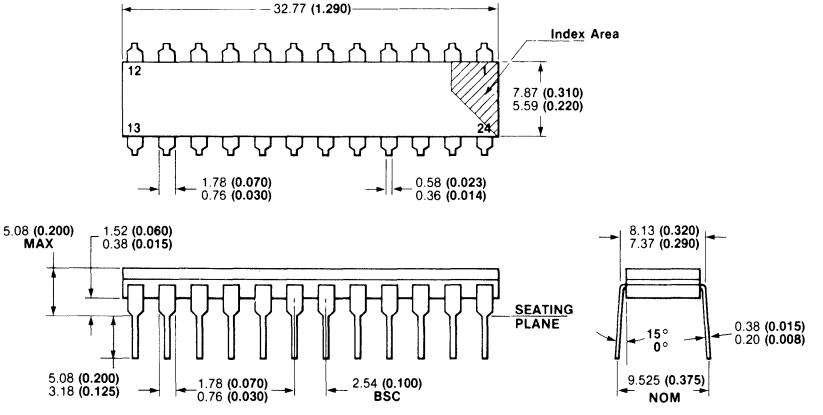
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

24 Lead Slim (0.300" Wide) Ceramic Dual In-Line

Ordering Codes: 74ACXXXSDC
74ACTXXXSDC
54ACXXXSDM
54ACTXXXSDM



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 7.620 **(0.300)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are alloy 42, either tin plated or solder coated.

Package is hermetically sealed alumina (black).

Package weight is 3.9 grams.

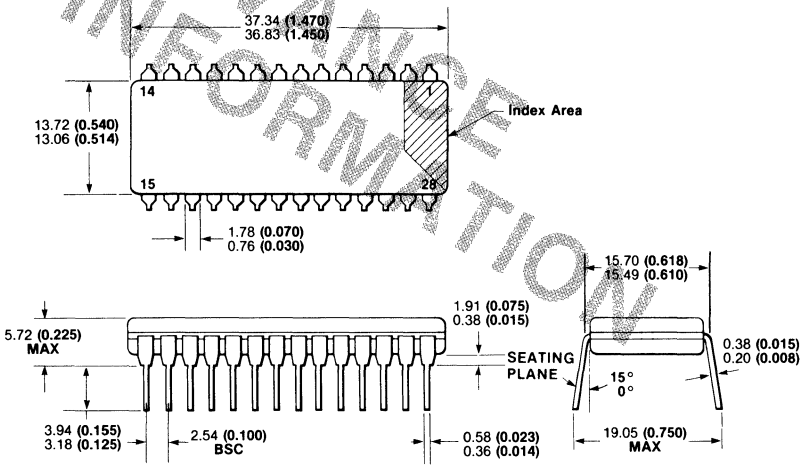
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

28 Lead Ceramic Dual In-Line

Ordering Codes: 74ACXXXDC
74ACTXXXDC
54ACXXXDM
54ACTXXXDM



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 15.240 **(0.600)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are alloy 42, either tin plated or solder coated.

Package is hermetically sealed alumina (black).

Package weight is 7.5 grams.

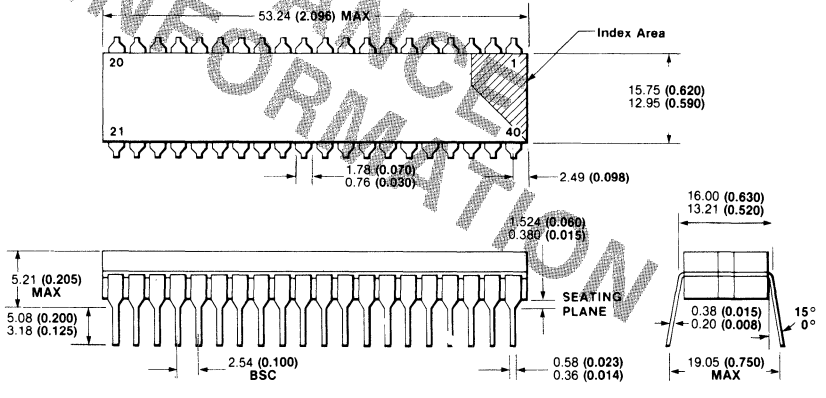
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

40 Lead Ceramic Dual In-Line

Ordering Codes: 74ACXXXDC
74ACTXXXDC
54ACXXXDM
54ACTXXXDM



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are intended for insertion in hole rows on 15.240 **(0.600)** centers. They are purposely shipped with positive misalignment to facilitate insertion.

Leads are alloy 42, either tin plated or solder coated.

Package is hermetically sealed alumina (black).

Package weight is 12.0 grams.

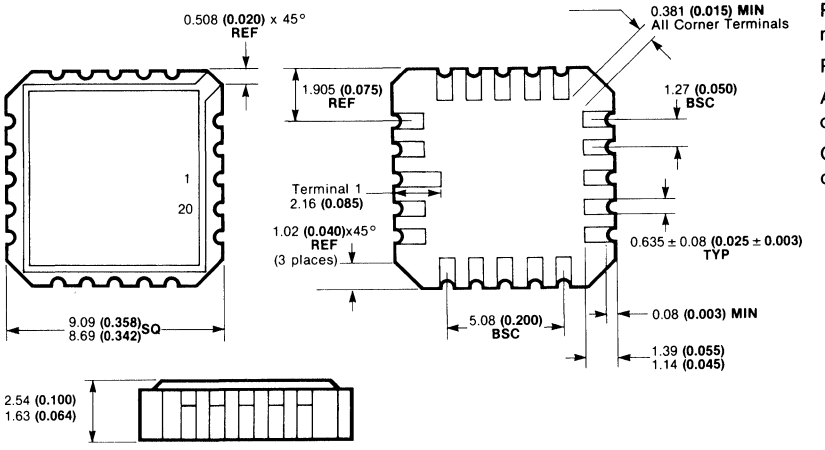
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

20 Terminal Ceramic Leadless Chip Carrier

Ordering Codes: 74ACXXXL1C
74ACTXXXL1C
54ACXXXL1M
54ACTXXXL1M



Notes

Package construction is multilayer refractory metal (gold plated) and alumina (black).

Package is hermetic—solder seal metal lid.

Package weight is 0.5 gram.

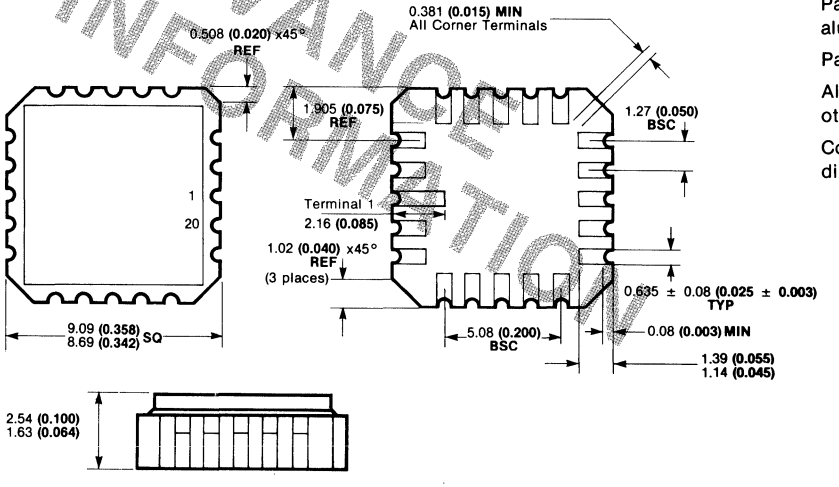
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

20 Terminal Ceramic Leadless Chip Carrier

Ordering Codes: 74ACXXXL1C
74ACTXXXL1C
54ACXXXL1M
54ACTXXXL1M



Notes

Package construction is multilayer refractory metal (gold plated) and alumina (black).

Package is hermetic—glass seal alumina lid (black).

Package weight is 0.5 gram.

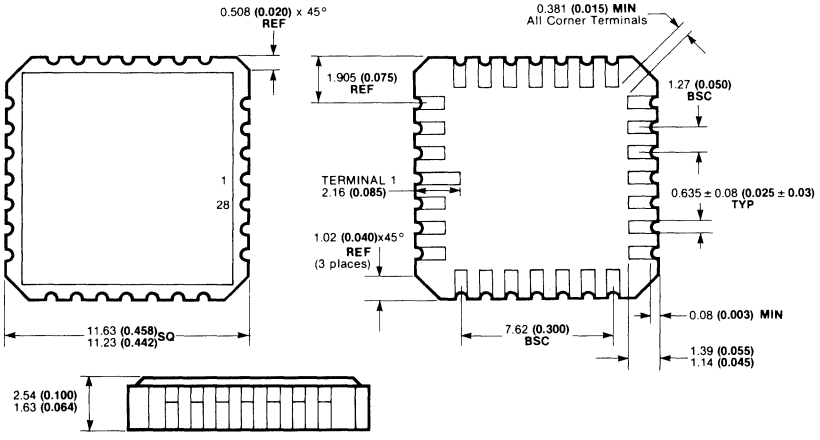
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

28 Terminal Ceramic Leadless Chip Carrier

Ordering Codes: 74ACXXXL1C
74ACTXXXL1C
54ACXXXL1M
54ACTXXXL1M



Notes

Package construction is multilayer refractory metal (gold plated) and alumina (black).

Package is hermetic—solder seal metal lid.

Package weight is 0.8 gram.

All dimensions are typical unless otherwise specified.

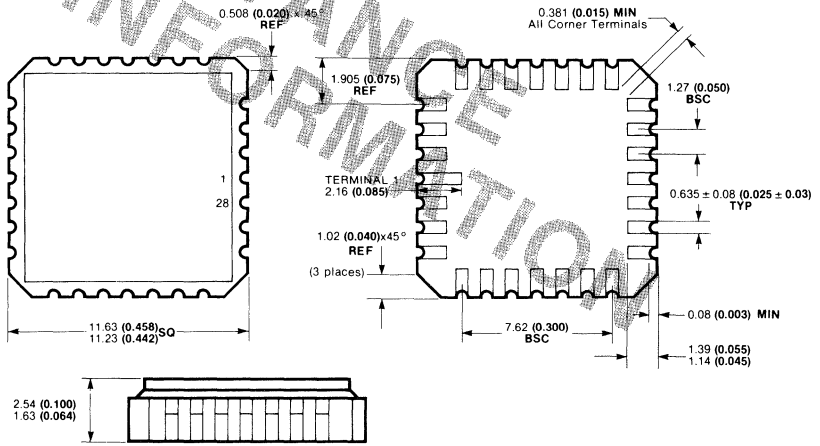
Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

5

28 Terminal Ceramic Leadless Chip Carrier

Ordering Codes: 74ACXXXL1C
74ACTXXXL1C
54ACXXXL1M
54ACTXXXL1M



Notes

Package construction is multilayer refractory metal (gold plated) and alumina (black).

Package is hermetic—glass seal alumina lid (black).

Package weight is 0.9 gram.

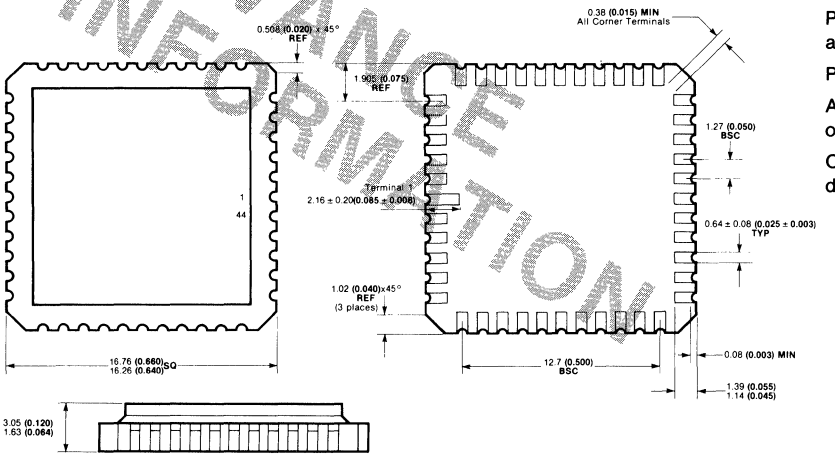
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

44 Terminal Ceramic Leadless Chip Carrier

Ordering Codes: 74ACXXXL1C
74ACTXXXL1C
54ACXXXL1M
54ACTXXXL1M



Notes

Package construction is multilayer refractory metal (gold plated) and alumina (black).

Package is hermetic—glass seal alumina lid (black).

Package weight is 1.7 grams.

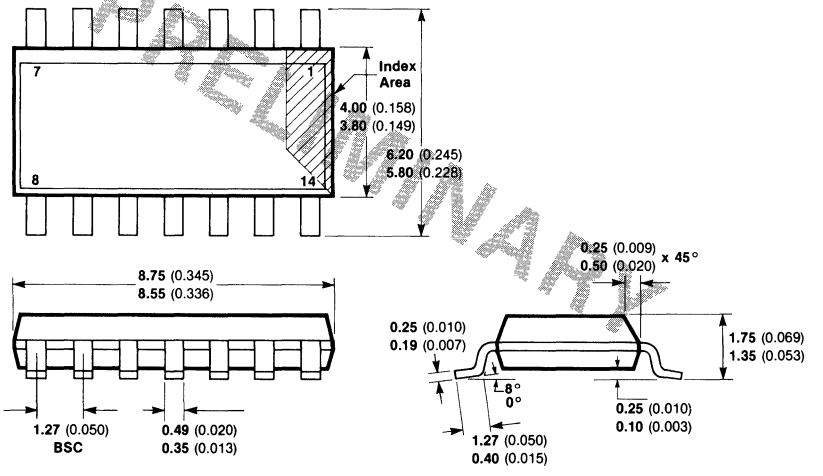
All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

Metric dimensions appear first, followed by **inch** dimensions.

14 Lead Small Outline Integrated Circuit (SOIC)

Ordering Code: 74ACXXXSC
74ACTXXXSC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Package weight is 0.14 grams.

Total flash not to exceed **0.15** (0.006) over body dimensions.

Conforms to variation AB of JEDEC Standard Outline MS-012 for **3.75** (0.150) body width small outline (SO) family.

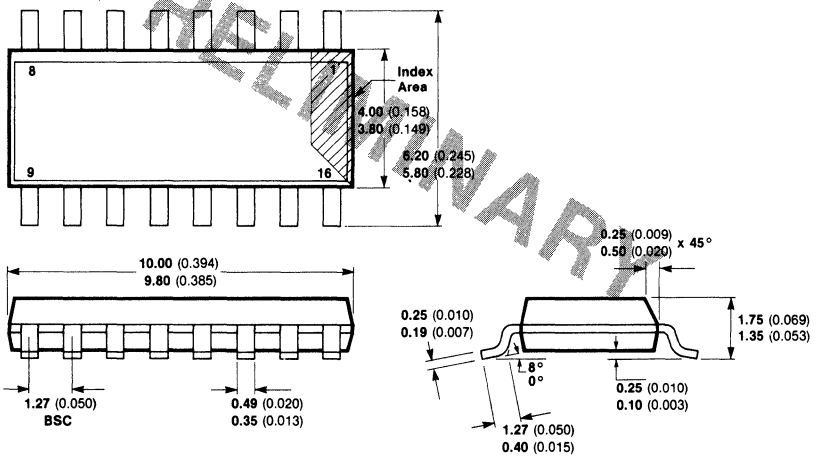
All dimensions are typical unless otherwise specified.

Controlling dimensions are metric dimensions.

Metric dimensions appear first, followed by inch dimensions.

16 Lead Small Outline Integrated Circuit (SOIC)

Ordering Code: 74ACXXXSC
74ACTXXXSC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Package weight is 0.16 grams.

Total flash not to exceed **0.15** (0.006) over body dimensions.

Conforms to variation AC of JEDEC Standard Outline MS-012 for **3.75** (0.150) body width small outline (SO) family.

All dimensions are typical unless otherwise specified.

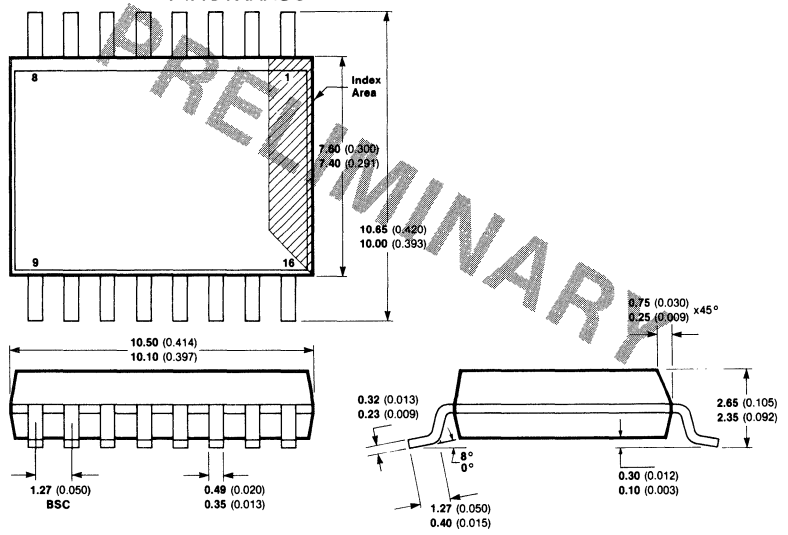
Controlling dimensions are metric dimensions.

Metric dimensions appear first, followed by inch dimensions.

5

16 Lead (0.300" Wide) Small Outline Integrated Circuit (SOIC)

Ordering Code: 74ACXXXSC
74ACTXXXSC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Package weight is 0.46 grams.

Total flash not to exceed **0.15** (0.006) over body dimensions.

Conforms to variation AA of JEDEC Standard Outline MS-013 for **7.50** (0.300) body width small outline (SO) family.

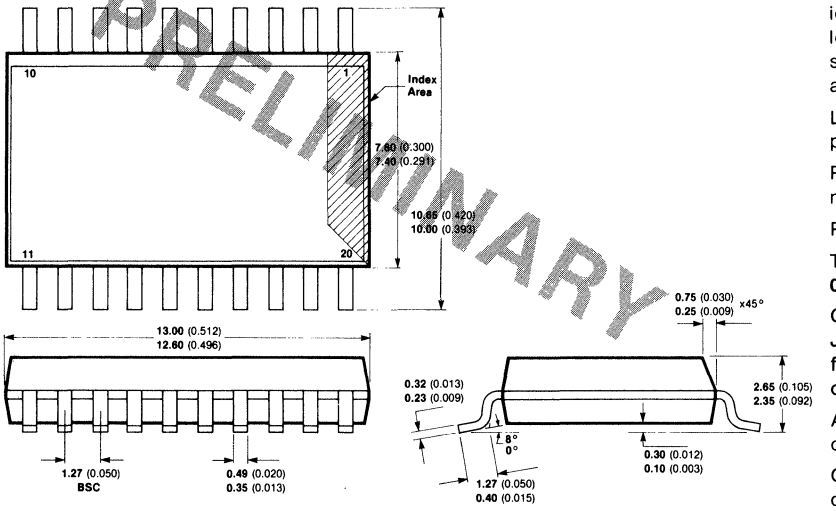
All dimensions are typical unless otherwise specified.

Controlling dimensions are metric dimensions.

Metric dimensions appear first, followed by inch dimensions.

20 Lead Small Outline Integrated Circuit (SOIC)

Ordering Code: 74ACXXXSC
74ACTXXXSC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Package weight is 0.55 grams.

Total flash not to exceed **0.15** (0.006) over body dimensions.

Conforms to variation AC of JEDEC Registered Outline MS-013 for **7.50** (0.300) body width small outline (SO) family.

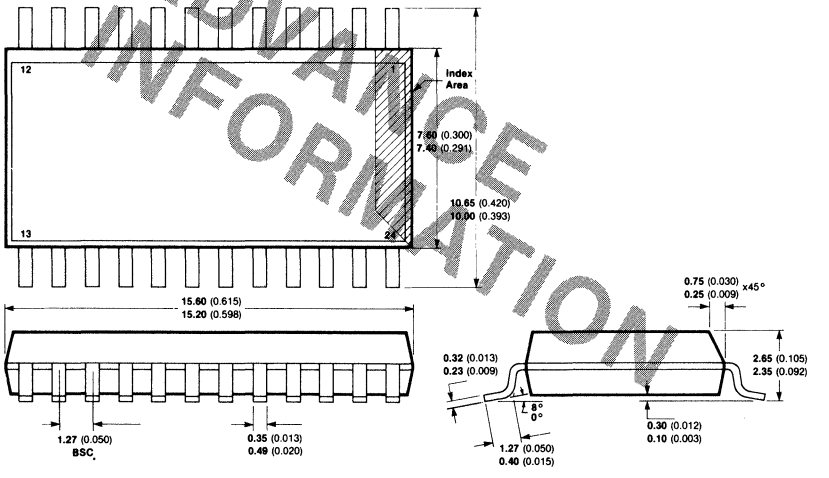
All dimensions are typical unless otherwise specified.

Controlling dimensions are metric dimensions.

Metric dimensions appear first, followed by inch dimensions.

24 Lead Small Outline Integrated Circuit (SOIC)

Ordering Code: 74ACXXXSC
74ACTXXXSC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Package weight is 0.66 grams.

Total flash not to exceed **0.15** (0.006) over body dimensions.

Conforms to variation AD of JEDEC Standard Outline MS-013 for **7.50** (0.300) body width small outline (SO) family.

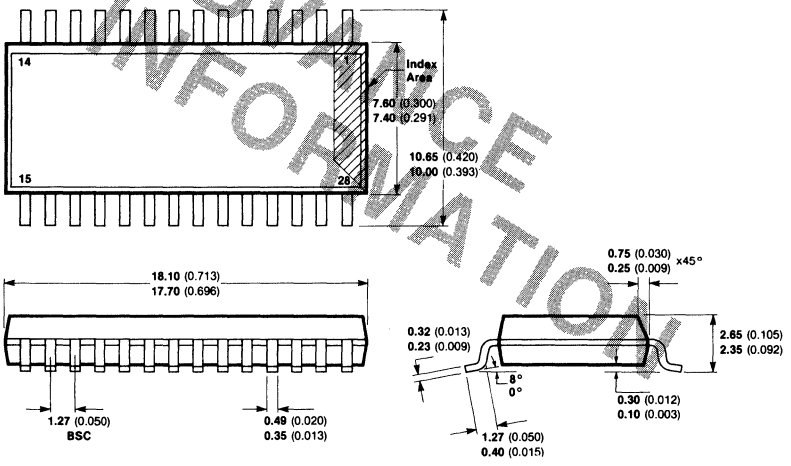
All dimensions are typical unless otherwise specified.

Controlling dimensions are metric dimensions.

Metric dimensions appear first, followed by inch dimensions.

28 Lead Small Outline Integrated Circuit (SOIC)

Ordering Code: 74ACXXXSC
74ACTXXXSC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Package weight is 0.77 grams.

Total flash not to exceed **0.15** (0.006) over body dimensions.

Conforms to variation AE of JEDEC Standard Outline MS-013 for **7.50** (0.300) body width small outline (SO) family.

All dimensions are typical unless otherwise specified.

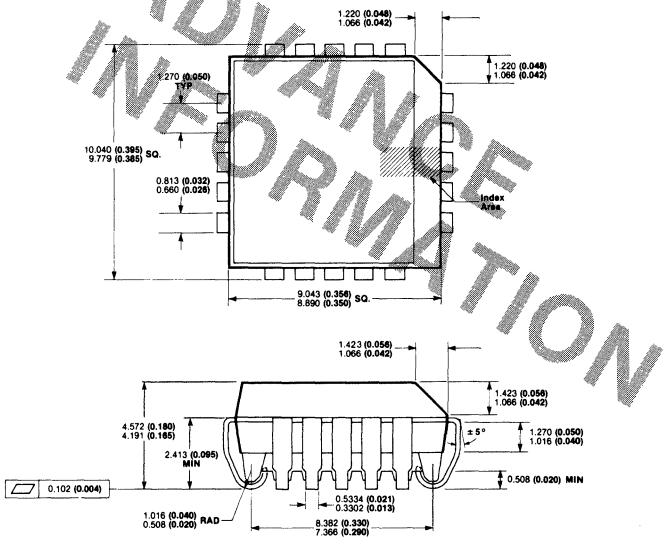
Controlling dimensions are metric dimensions.

Metric dimensions appear first, followed by inch dimensions.

5

20 Lead Plastic Chip Carrier (PCC)

Ordering Code: 74ACXXXQC
74ACTXXXQC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Total flash not to exceed 0.016 **(0.006)** over body dimensions.

Conforms to variation AA of JEDEC Registered Outline MO-047 for Plastic Chip Carrier package.

All dimensions are typical unless otherwise specified.

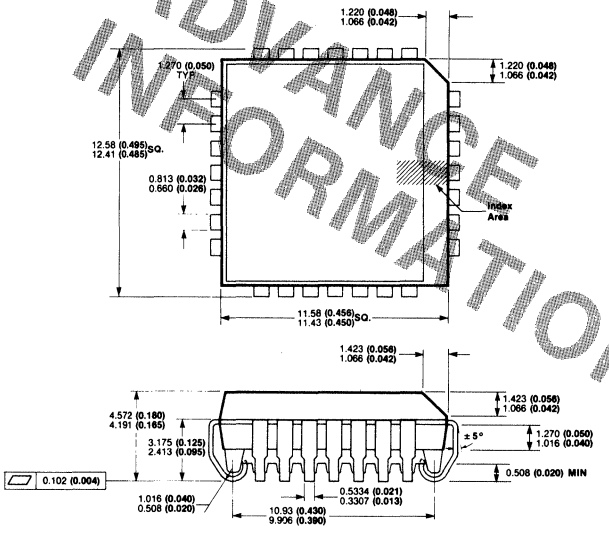
Controlling dimensions are inch dimensions.

This package is also referred to as a Plastic Leaded Chip Carrier (PLCC) or Plastic Quadpak.

Metric dimensions appear first, followed by **inch** dimensions.

28 Lead Plastic Chip Carrier (PCC)

Ordering Code: 74ACXXXQC
74ACTXXXQC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Total flash not to exceed 0.016 **(0.006)** over body dimensions.

Conforms to variation AB of JEDEC Registered Outline MO-047 for Plastic Chip Carrier package.

All dimensions are typical unless otherwise specified.

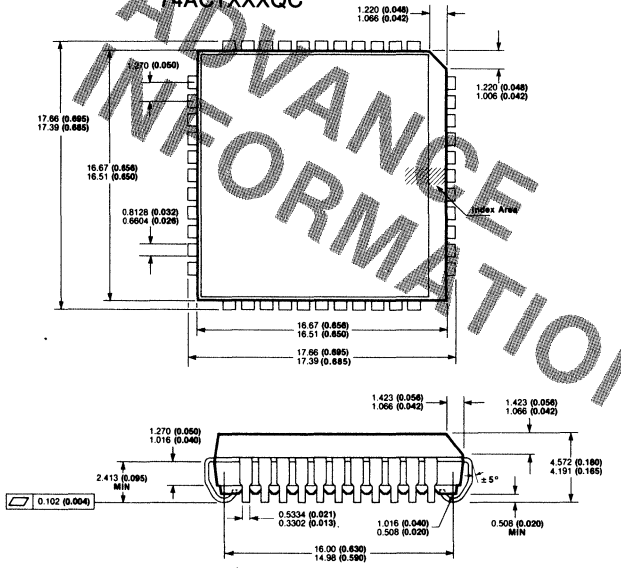
Controlling dimensions are inch dimensions.

This package is also referred to as a Plastic Leaded Chip Carrier (PLCC) or Plastic Quadpak.

Metric dimensions appear first, followed by **inch** dimensions.

44 Lead Plastic Chip Carrier (PCC)

Ordering Code: 74ACXXXQC
74ACTXXXQC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Total flash not to exceed 0.16 **(0.006)** over body dimensions.

Conforms to variation AC of JEDEC Registered Outline MO-047 for Plastic Chip Carrier package.

All dimensions are typical unless otherwise specified.

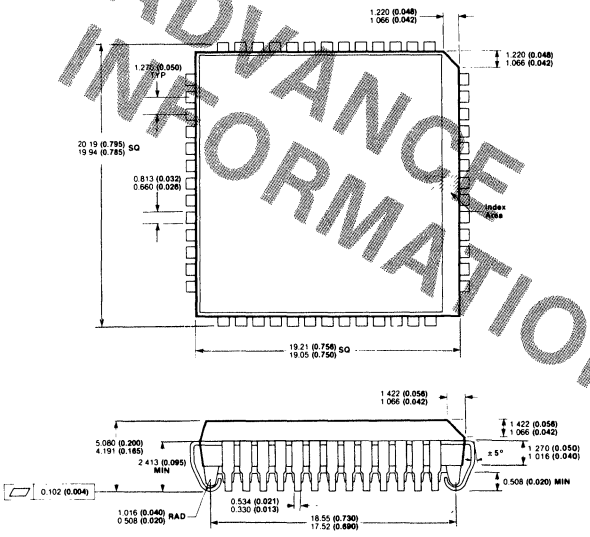
Controlling dimensions are inch dimensions.

This package is also referred to as a Plastic Leaded Chip Carrier (PLCC) or Plastic Quadpak.

Metric dimensions appear first, followed by **inch** dimensions.

52 Lead Plastic Chip Carrier (PCC)

Ordering Code: 74ACXXXQC
74ACTXXXQC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Total flash not to exceed 0.16 **(0.006)** over body dimensions.

Conforms to variation AD of JEDEC Registered Outline MO-047 for Plastic Chip Carrier package.

All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

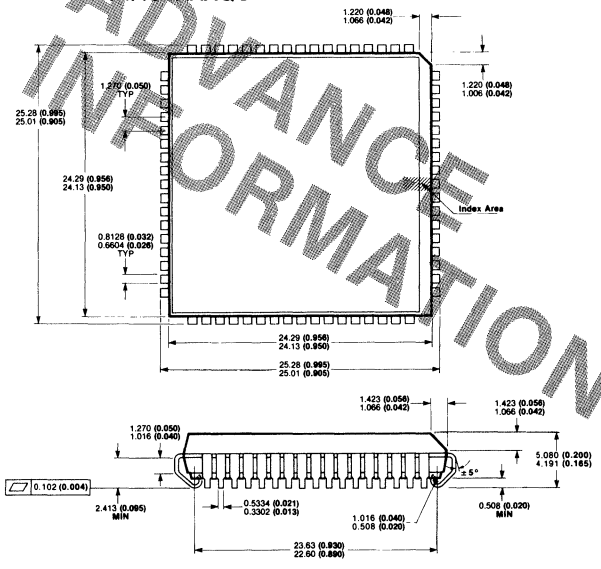
This package is also referred to as a Plastic Leaded Chip Carrier (PLCC) or Plastic Quadpak.

Metric dimensions appear first, followed by **inch** dimensions.

5

68 Lead Plastic Chip Carrier (PCC)

Ordering Code: 74ACXXXQC
74ACTXXXQC



Notes

Index area: a notch or Lead One identification mark shall be located adjacent to Lead One and shall be located within the shaded area shown.

Leads are copper alloy, either tin plated or solder coated.

Package plastic material is novolac epoxy.

Total flash not to exceed 0.016 **(0.006)** over body dimensions.

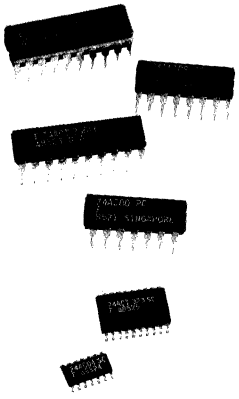
Conforms to variation AE of JEDEC Registered Outline MO-047 for Plastic Chip Carrier package.

All dimensions are typical unless otherwise specified.

Controlling dimensions are inch dimensions.

This package is also referred to as a Plastic Leaded Chip Carrier (PLCC) or Plastic Quadpak.

Metric dimensions appear first, followed by **inch** dimensions.



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Rochester, New York 14623
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Hamilton/Avnet Electronics
16 Corporate Circle
East Syracuse, New York 13057
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Schweber Electronics
Jericho Turnpike
Westbury, New York 11590
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Schweber Electronics
3 Town Line Circle
Rochester, New York 14623
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Summit Distributors, Inc.
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Tel: 716-884-3450

Zeus Components, Inc.
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Tel: 914-937-7400

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Winston-Salem, North Carolina 27101
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Arrow Electronics
5240 Greens Dairy Road
Raleigh, North Carolina 27604
Tel: 919-876-3132

Hall-Mark Electronics
5237 North Blvd.
Raleigh, North Carolina 27604
Tel: 919-872-0712

Hamilton/Avnet Electronics
3510 Spring Forest Road
Raleigh, North Carolina 27604
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5285 North Blvd.
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Tel: 919-876-0000

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7620 McEwen Road
Centerville, Ohio 45459
Tel: 513-435-5563

Arrow Electronics
1040 Crupper Avenue
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Tel: 614-885-8362

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6238 Cochran Road
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Tel: 216-248-3990

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Tulsa, Oklahoma 74145
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Hall-Mark Electronics
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Santurce, Puerto Rico 00911
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Austin, Texas 78758
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1585 West 2100 South
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