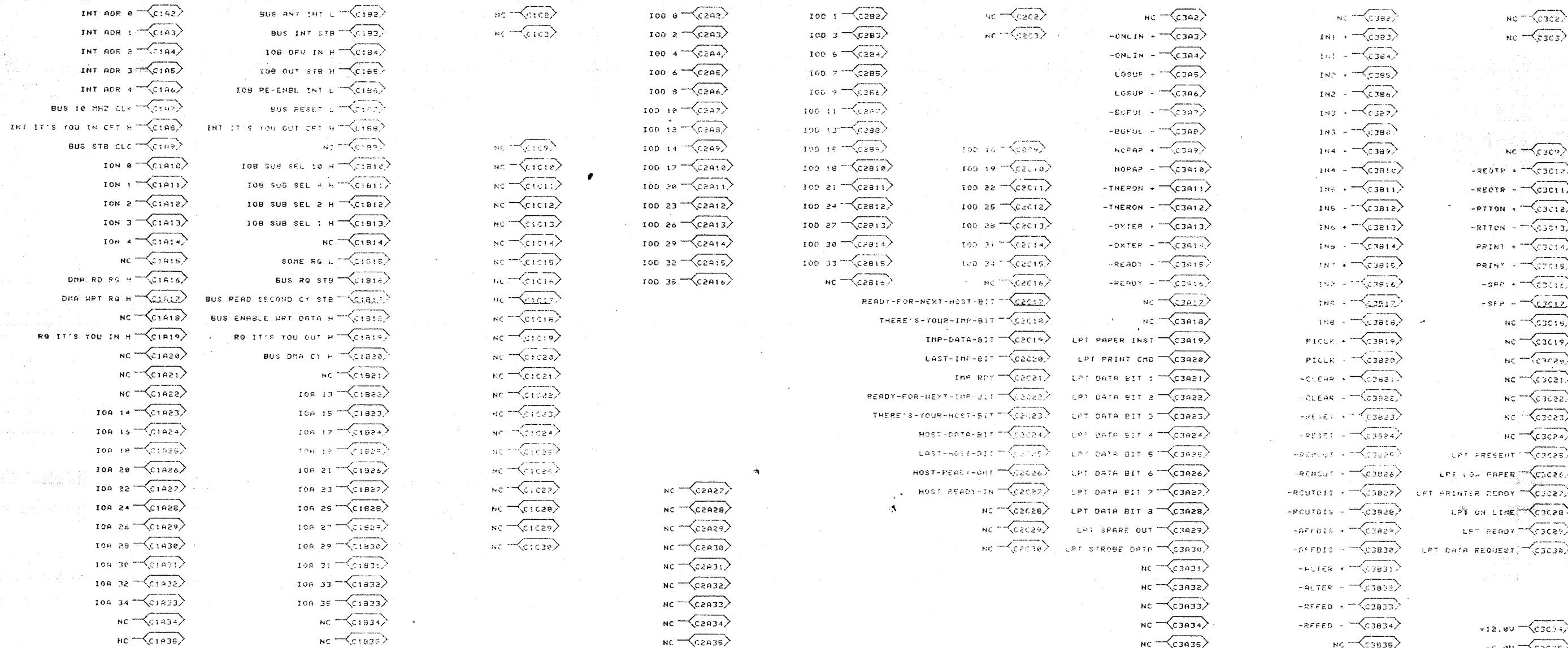
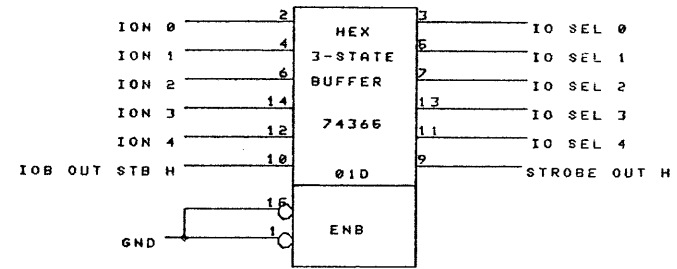


NOTE: SIGNALS "INT IT'S YOU" AND "RW IT'S YOU" ARE NOT BUSSED!!!! -- THEY ARE DAISY-CHAINED (IN TO OUT)!!!!!!

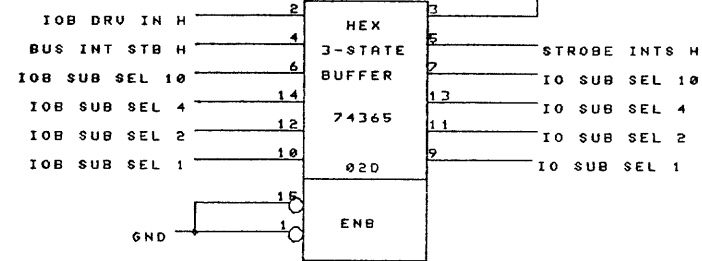
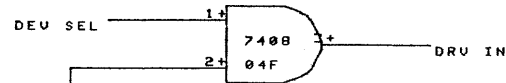
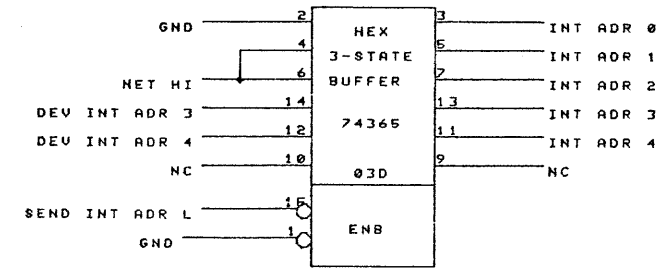


Foonly, Inc.		LPT/NET Interface Backpanel Pins		24-JUN-80 03:21
DRAWN BY:		PAGE 1 OF 17	NUMBER	NETCON.DRW [46,646662]
APPROVED BY: <i>S. Foonly</i>		PROJECT:	L P T	REV. A

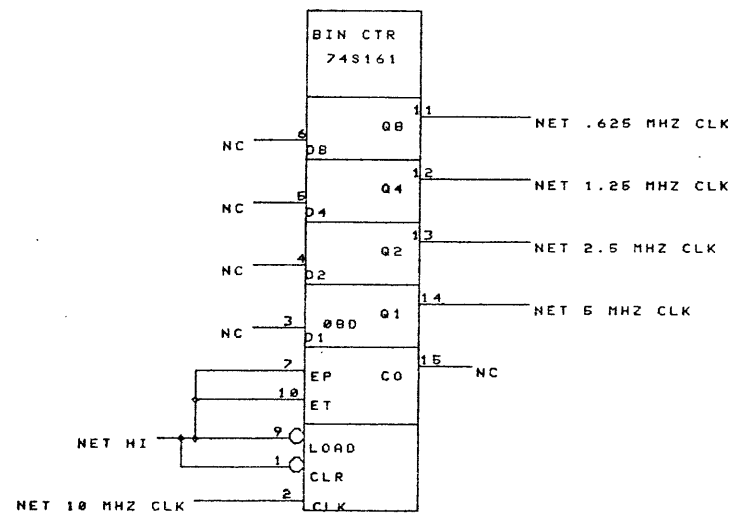
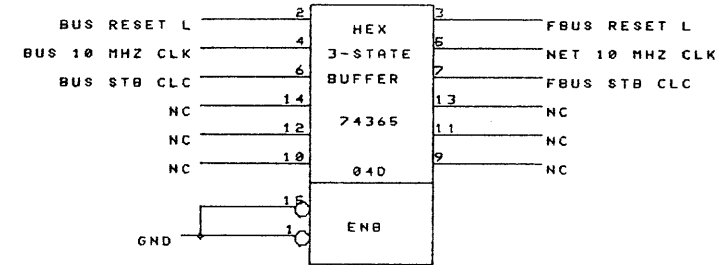
These two buffers receive the device select and control signals from the CPU



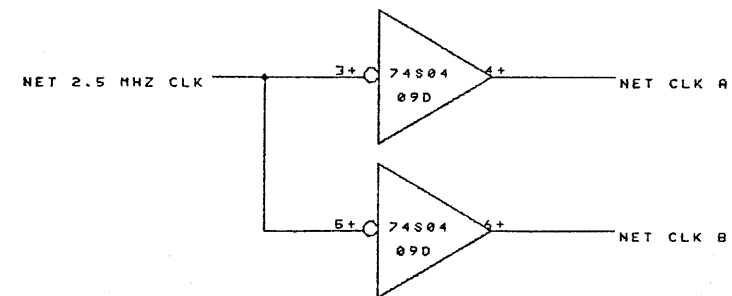
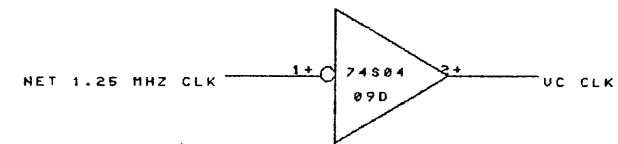
This drives the device number onto the FBUS when this device's micro-interrupt is acknowledged by the bus control logic.



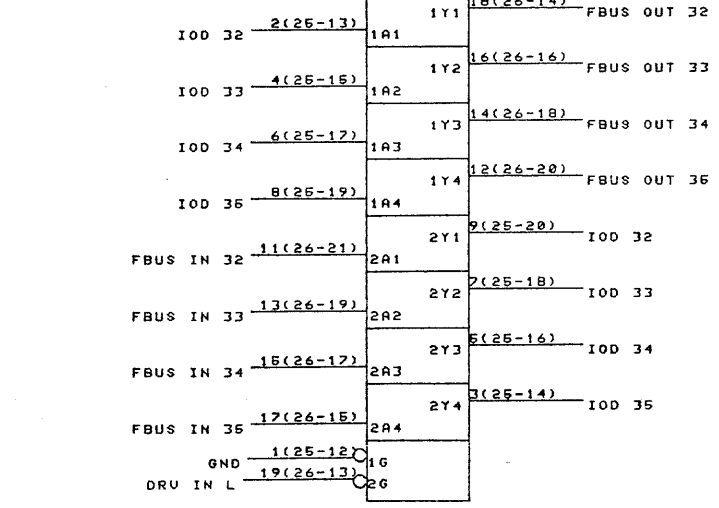
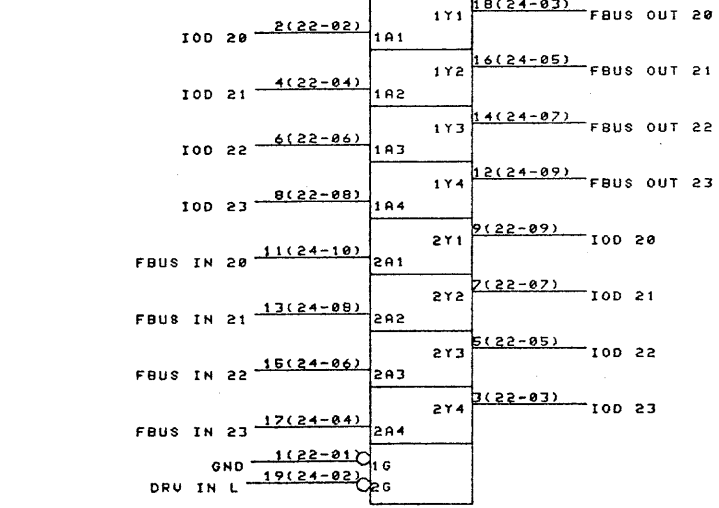
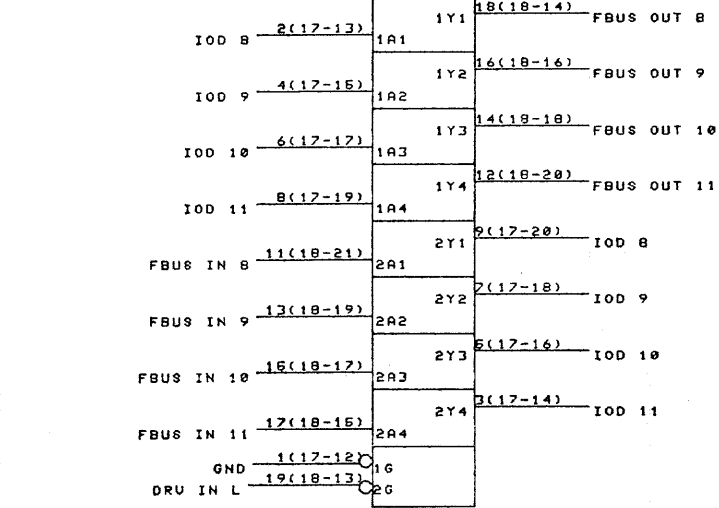
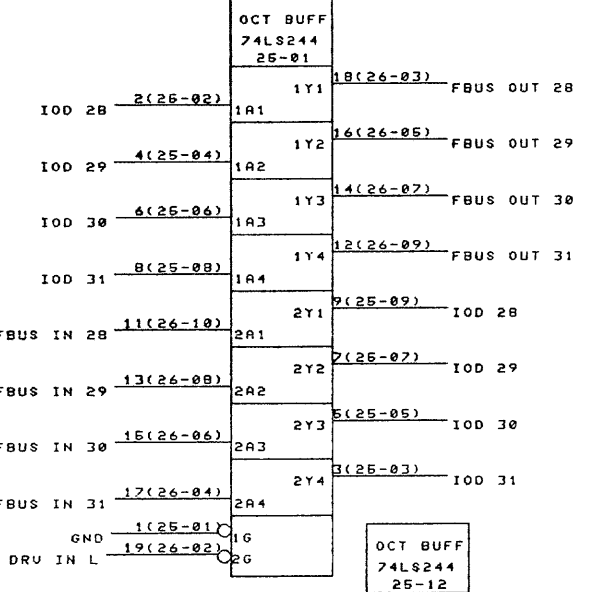
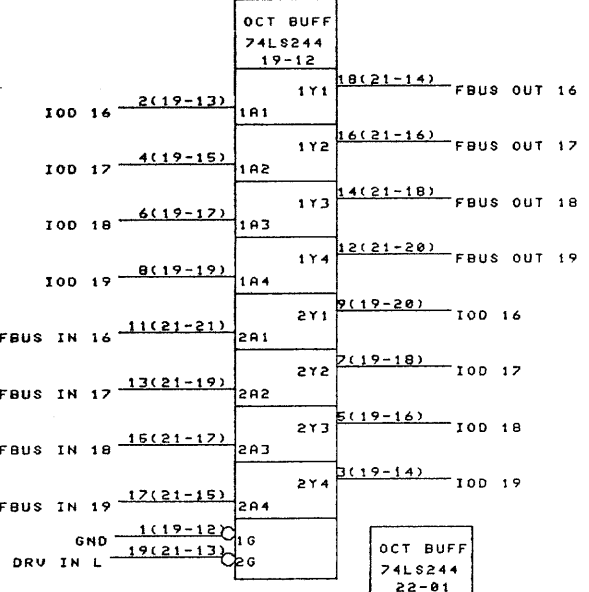
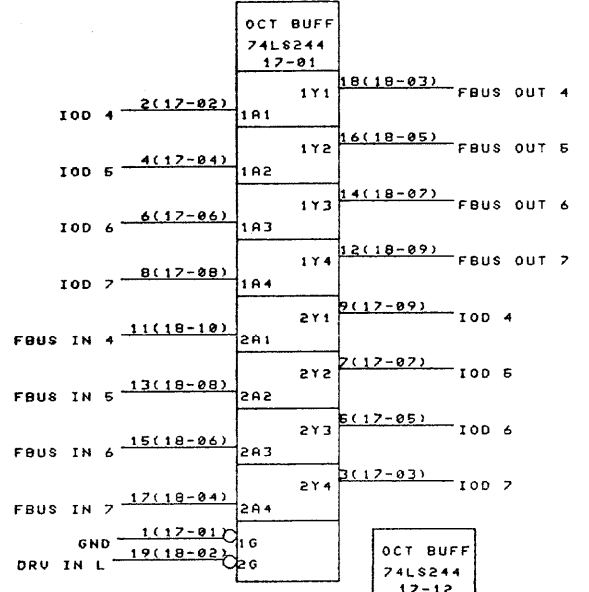
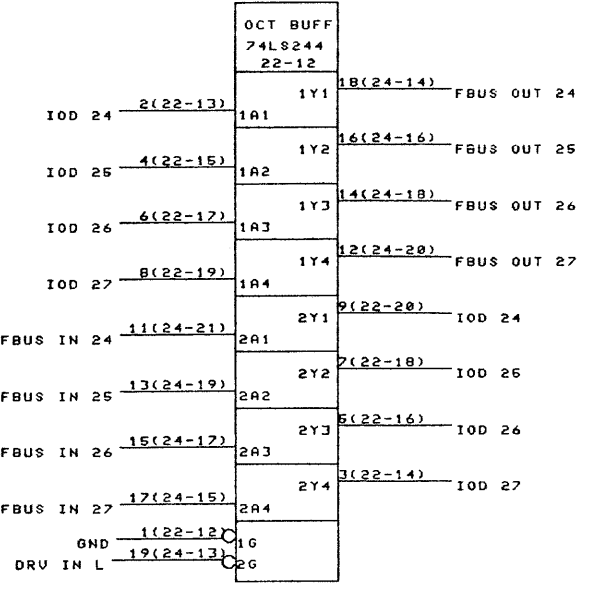
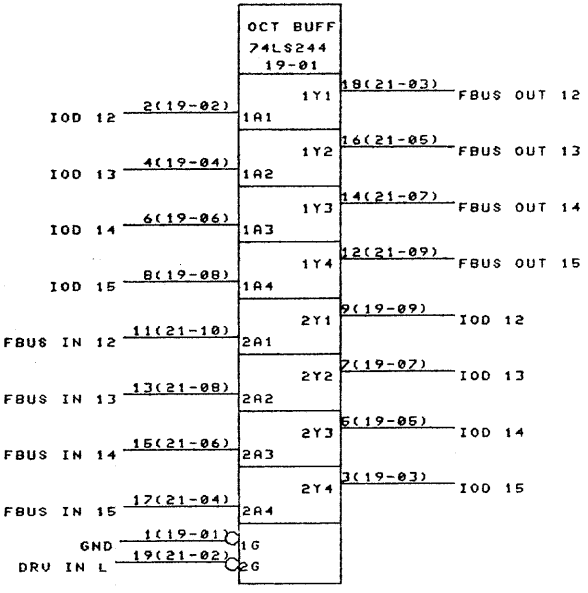
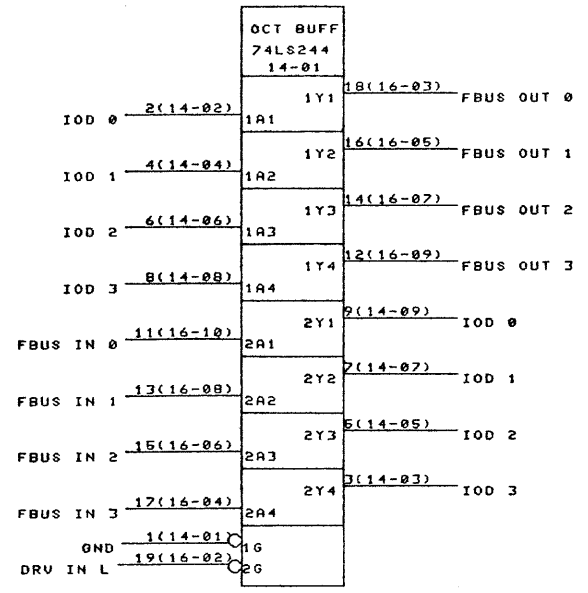
Here FBUS receivers



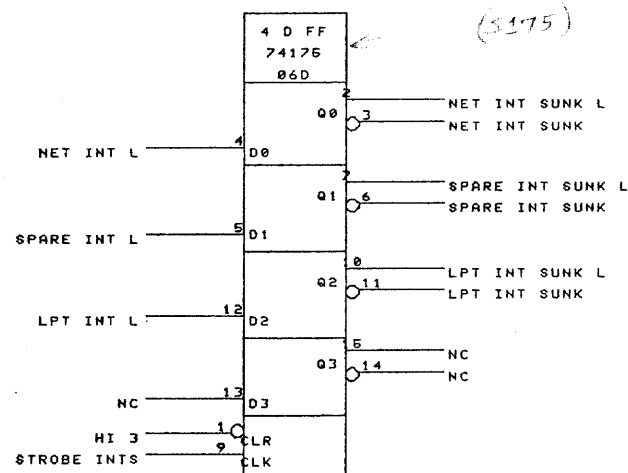
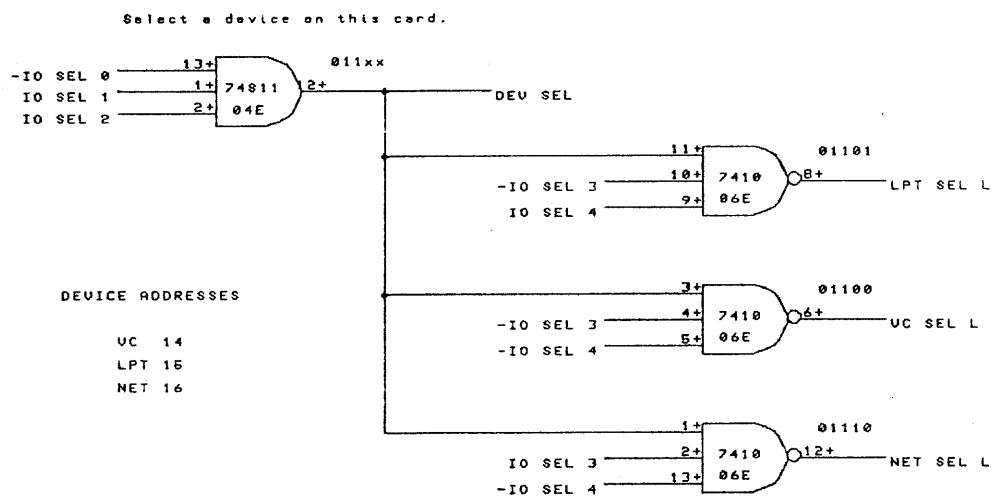
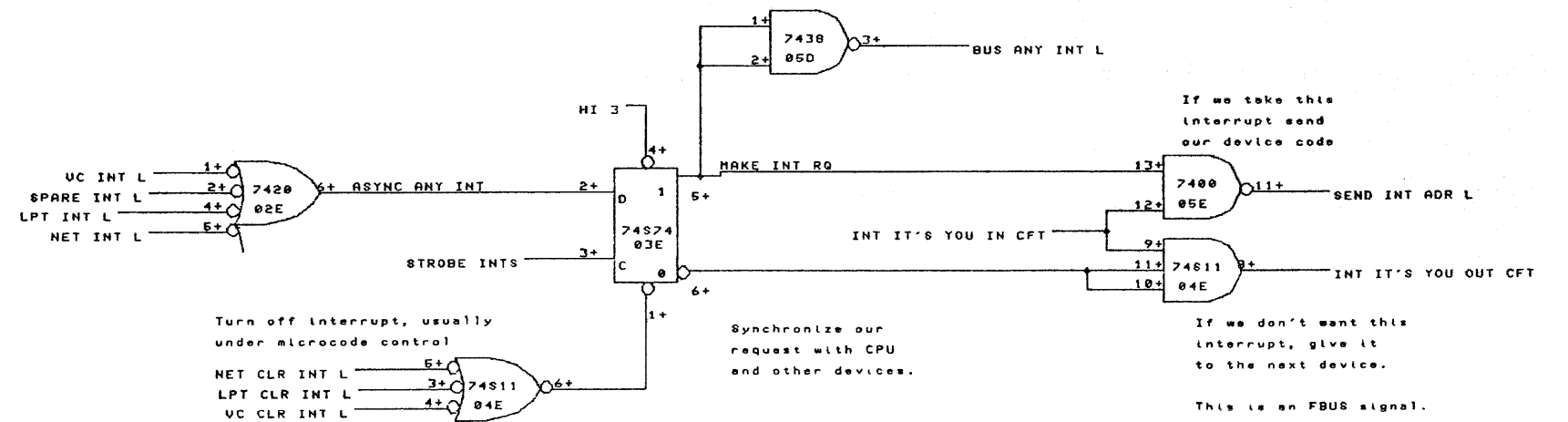
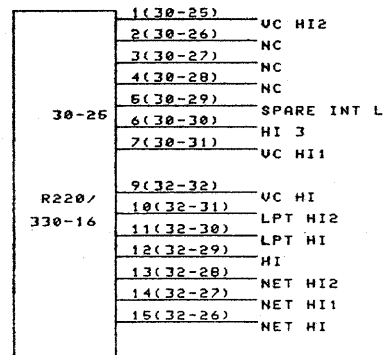
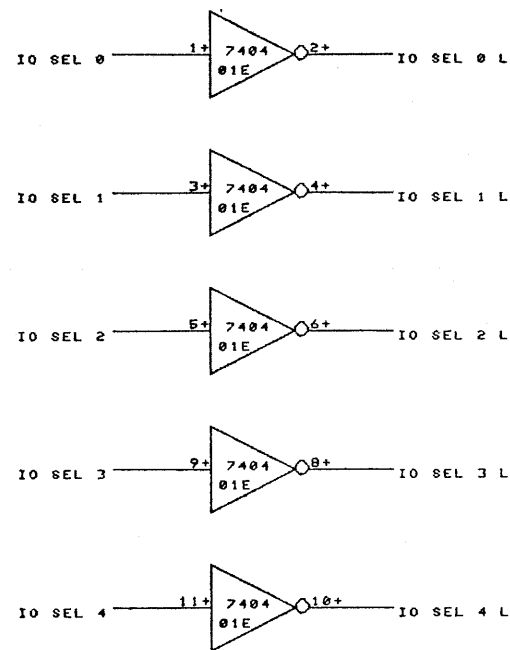
Divide down system clock for local use



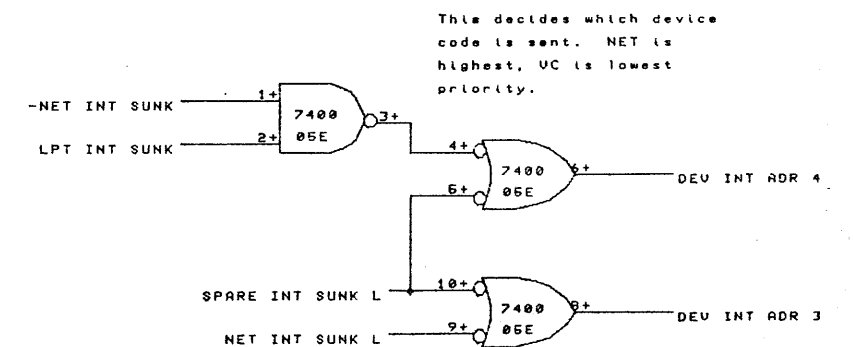
Foonly, Inc.		LPT/NET Interface FBUS Buffers		24-JUN-80 03:06	
DRAWN BY:		PAGE 2 OF 17	NUMBER	REV.	
APPROVED BY: <i>S. Foonly</i>		PROJECT:	L P T	A	
				NETBF.DRW [46,646662]	



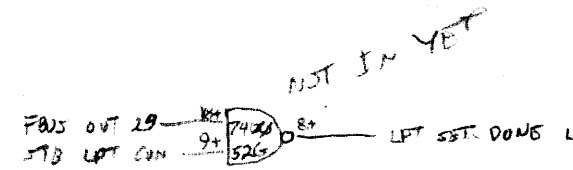
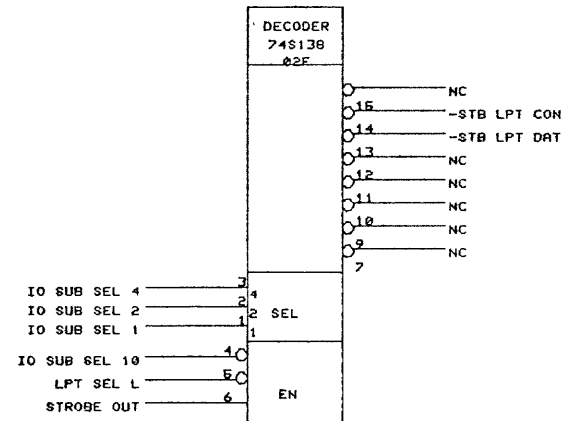
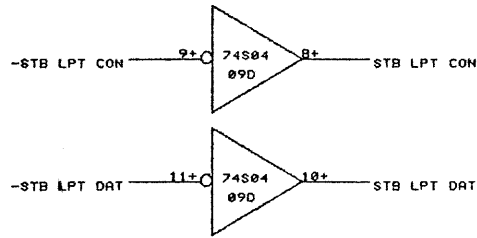
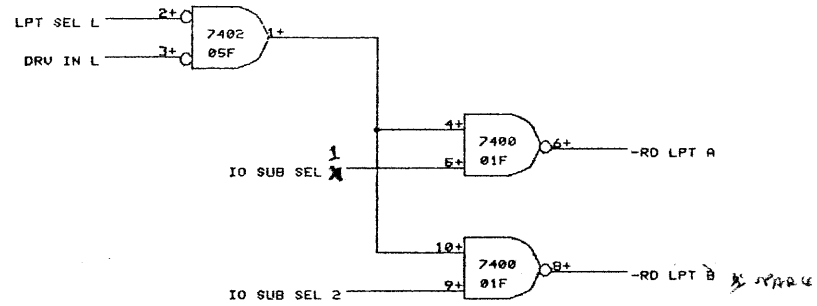
Foonly, Inc.		LPT/NET Interface Data Buffers		24-JUN-80 03:06	
DRAWN BY:		PAGE 3 OF 17		NUMBER	
APPROVED BY: <i>J. Foonly</i>		PROJECT:		L P T	
				REV. A	
NETBF1.DRW [46,646662]					



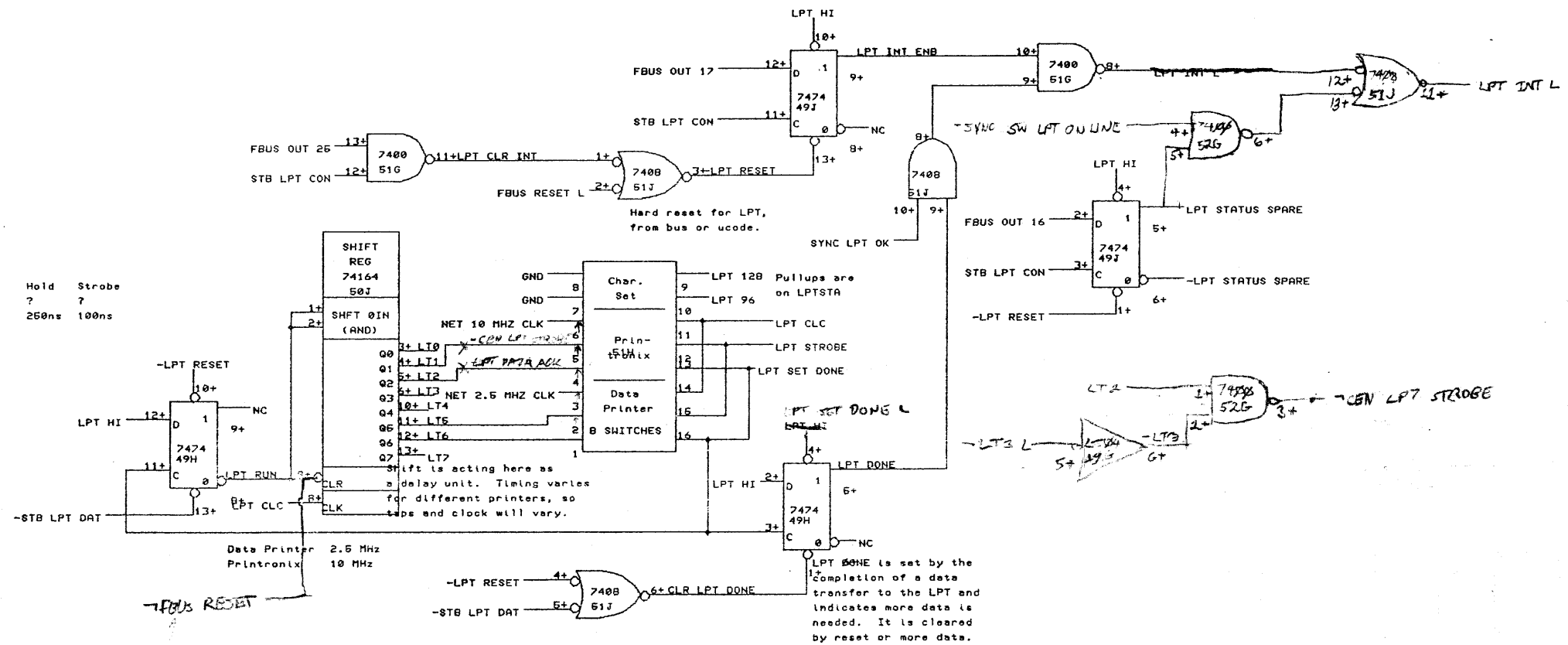
The address of the interrupting device must be synchronized with the CPU.



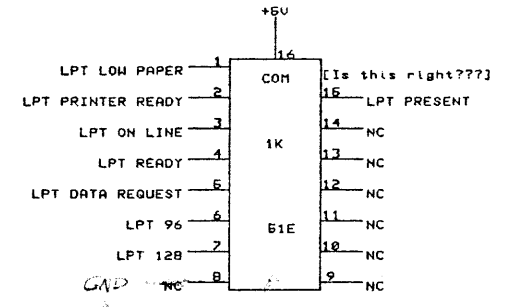
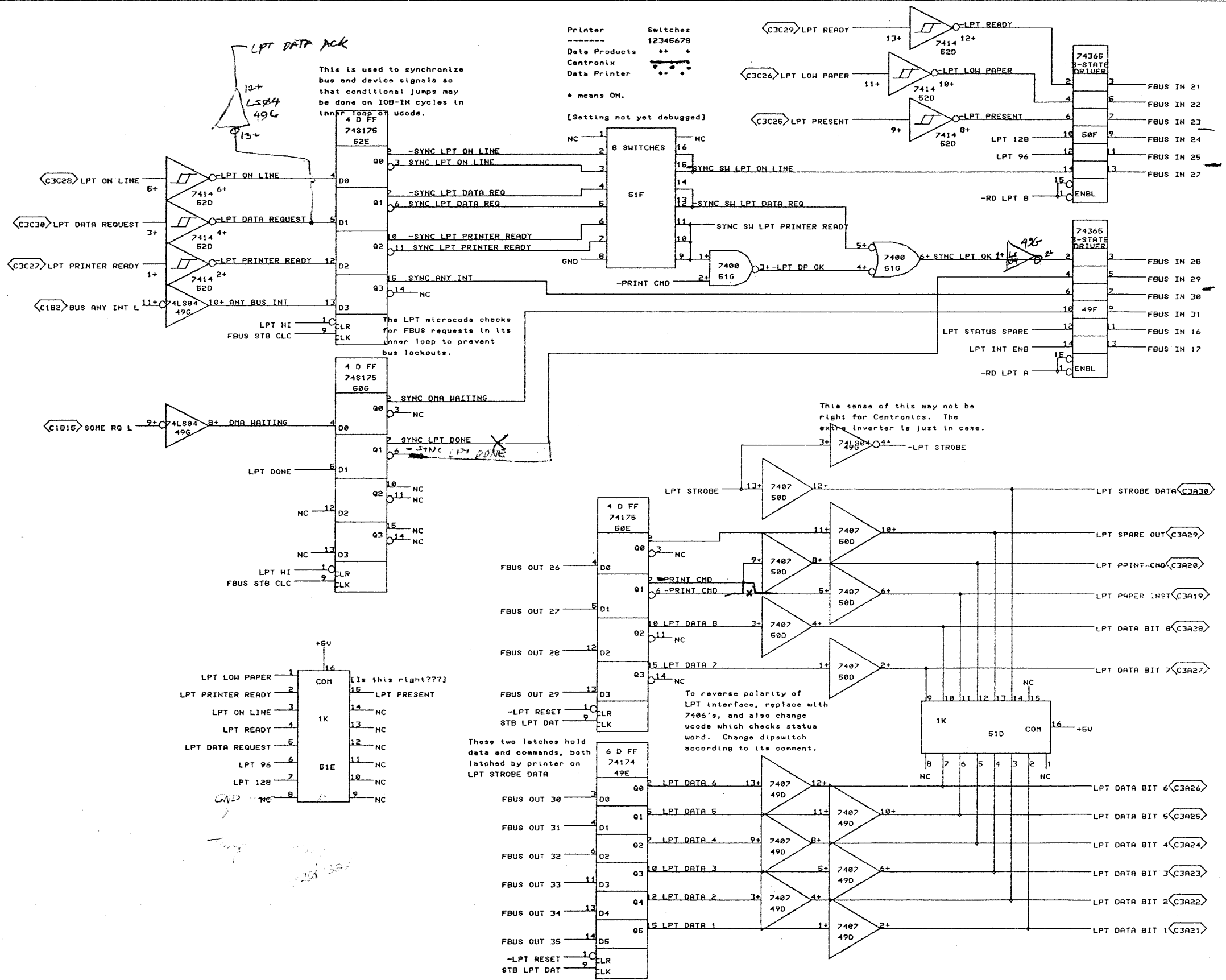
Foonly, Inc.		LPT/NET Interface Device Select		24-JUN-80 03:06	
DRAWN BY: Jovar		PAGE 4 OF 17		LPTINT.DRW [46,646662]	
APPROVED BY: S. Foonly		PROJECT:		NUMBER	REV. A
		L P T			



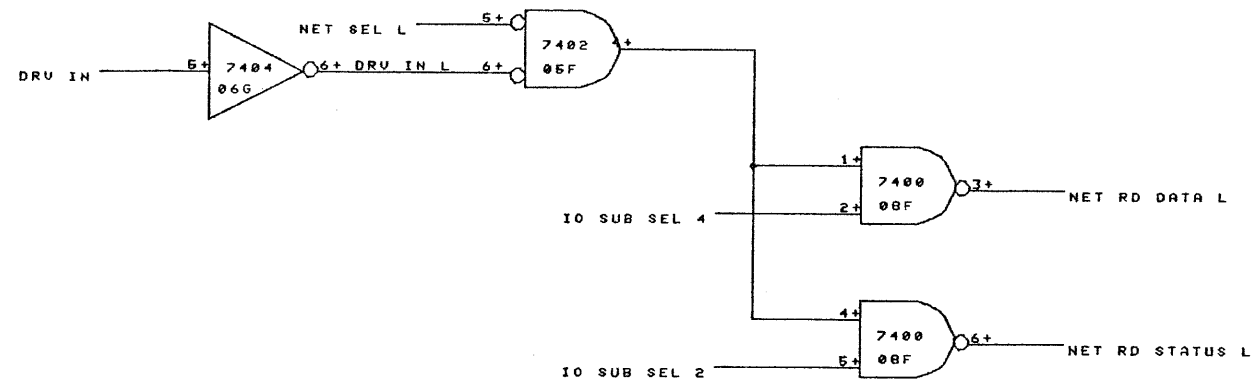
Printer Timing:
 Type Setup Hold Strobe
 Data Printer 2usec ? 7
 Printronix 50 ns 250ns 100ns
 (either interface)



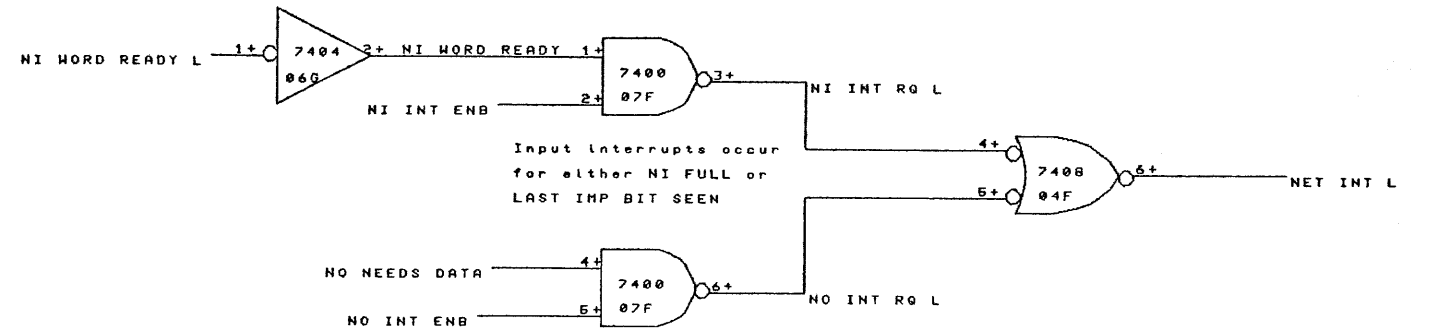
Foonly, Inc.		LPT/NET Interface Control logic		24-JUN-80 03:07
DRAWN BY: S. Fovar		PAGE 5 OF 17	NUMBER	REV. A
APPROVED BY: S. Foonly		PROJECT:	LPT	



Foonly, Inc.		LPT/NET Interface LPT Data		24-JUN-80 03:07	
DRAWN BY: S. Foonly		PAGE 6 OF 17		LPTDAT.DRW [46,646662]	
APPROVED BY: S. Foonly		PROJECT: LPT		NUMBER	REV. A

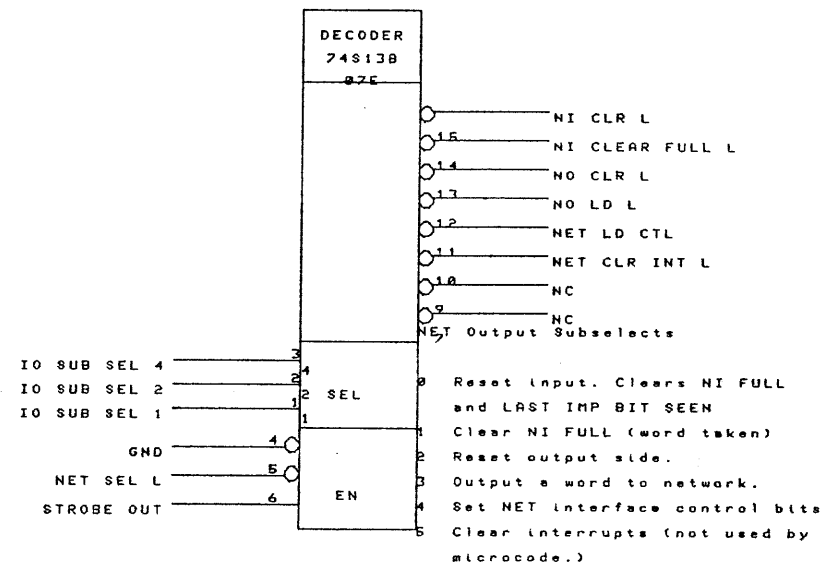


NET Input Subselects
 2 Status
 4 Data (shift register)

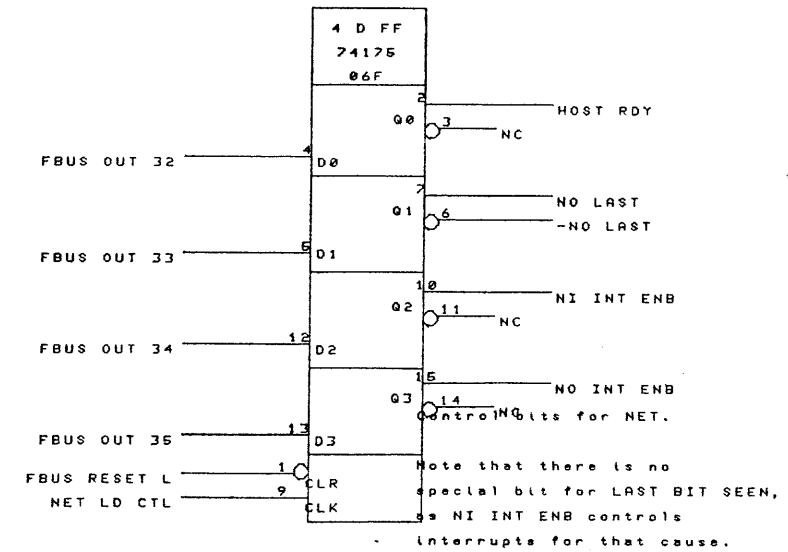


Input Interrupts occur for either NI FULL or LAST IMP BIT SEEN

Output Interrupts occur on NO EMPTY and -NO LAST, or on last bit taken.



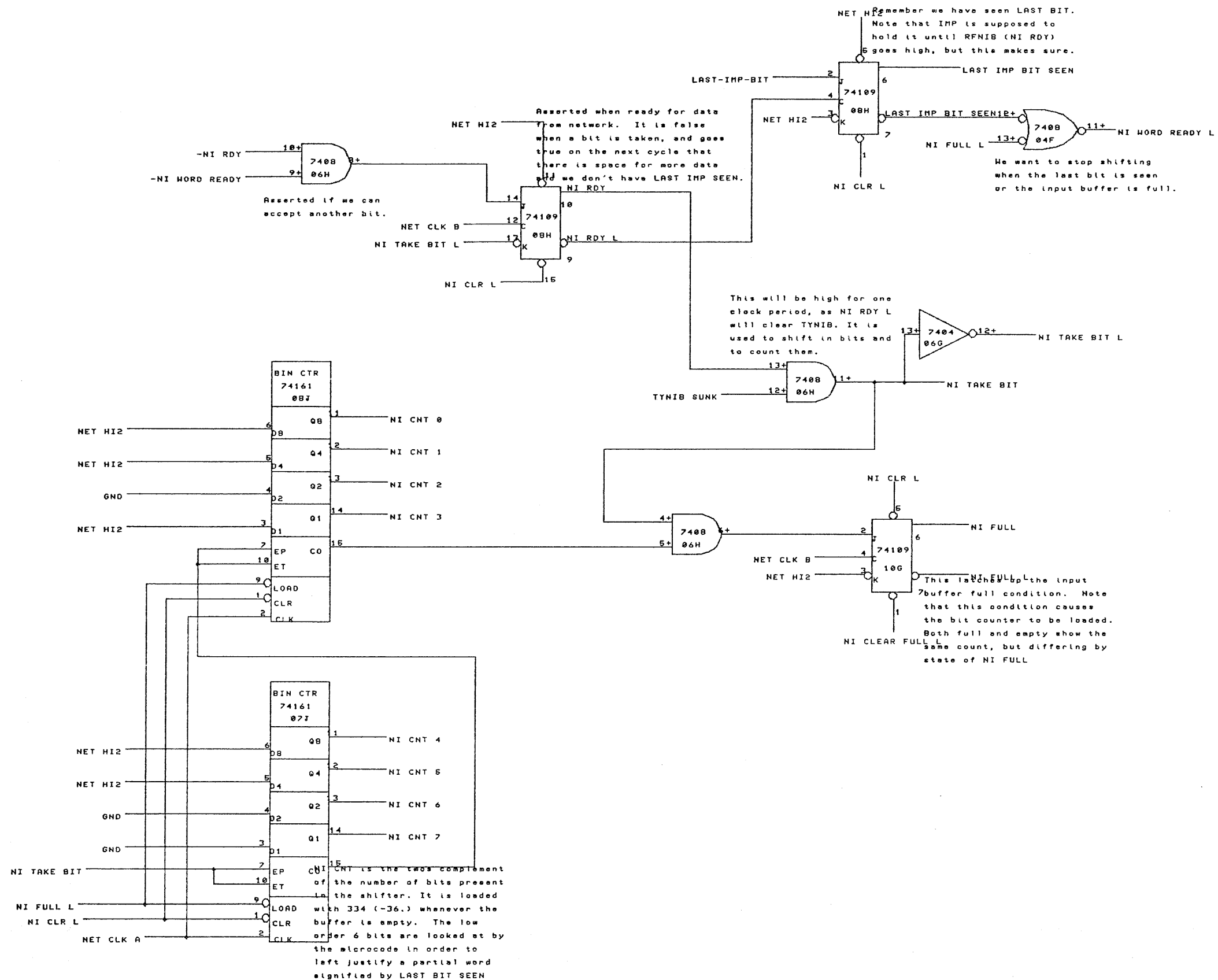
NET Output Subselects
 8 Reset input. Clears NI FULL and LAST IMP BIT SEEN
 1 Clear NI FULL (word taken)
 2 Reset output side.
 3 Output a word to network.
 4 Set NET interface control bits
 5 Clear interrupts (not used by microcode.)



Note that there is no special bit for LAST BIT SEEN, as NI INT ENB controls interrupts for that cause.

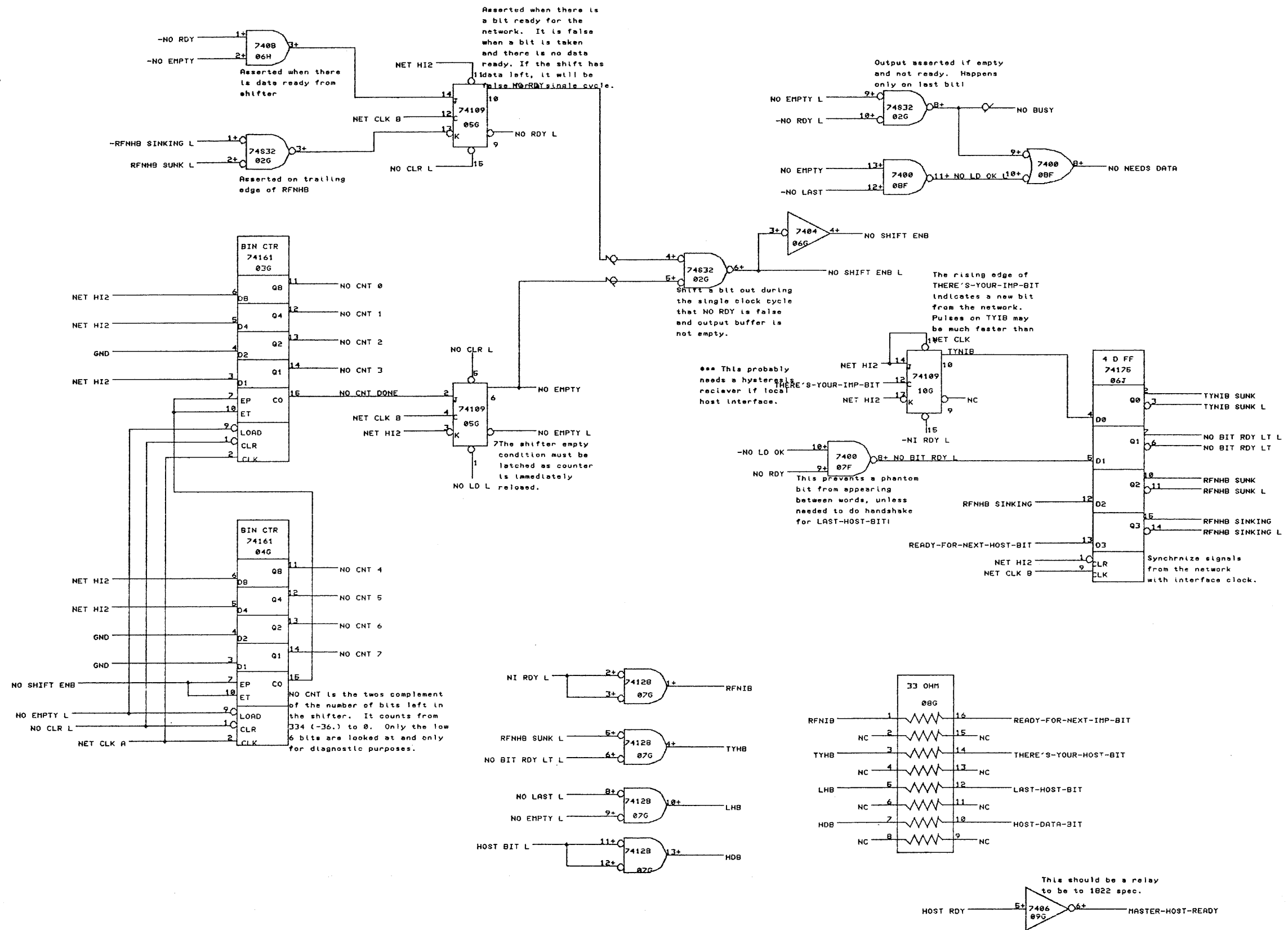
Caution: After setting NO LAST, do not load shifter until NO NEEDS DATA is true.

Foonly, Inc.		LPT/NET Interface Net Control		24-JUN-80 03:07
DRAWN BY: J. Fovar		PAGE 7 OF 17	NUMBER	REV.
APPROVED BY: J. Foonly		PROJECT:	L P T	A
				NETCT1.DRW [46,646662]

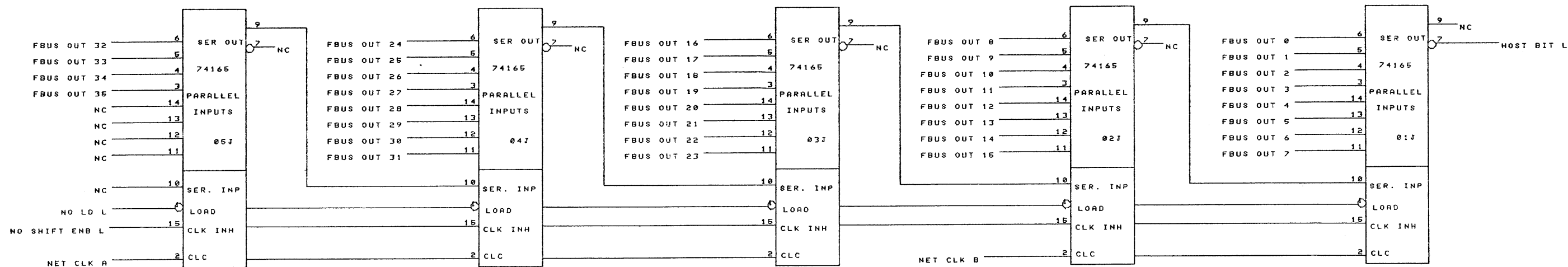


Foonly, Inc.		LPT/NET Interface Net Input		24-JUN-80 03:08
DRAWN BY: <i>S. Foonly</i>		PAGE 8 OF 17	NUMBER	REV. A
APPROVED BY: <i>S. Foonly</i>		PROJECT:	L P T	

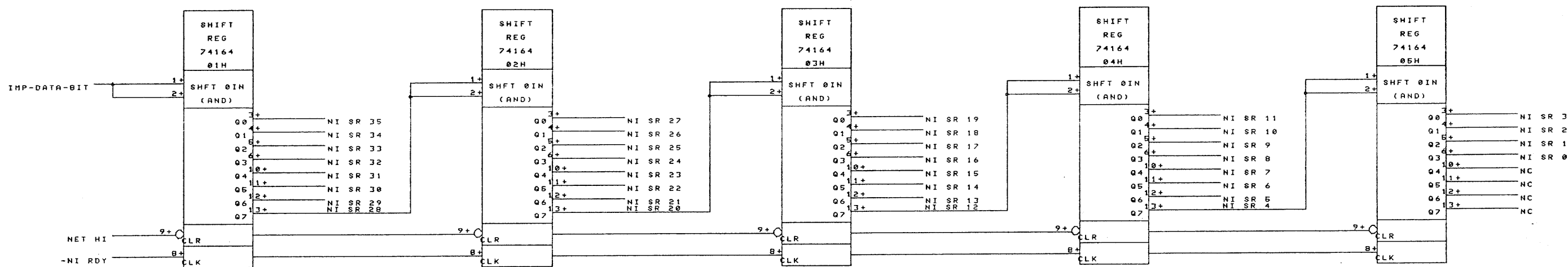
NETICT.DRW[46,646662]



Foonly, Inc.		LPT/NET Interface Net Output		24-JUN-80 03:09
DRAWN BY: <i>S. Foonly</i>		PAGE 9 OF 17	NUMBER	REV.
APPROVED BY: <i>S. Foonly</i>		PROJECT:	L P T	A
				NETOCT.DRW [46, 646662]

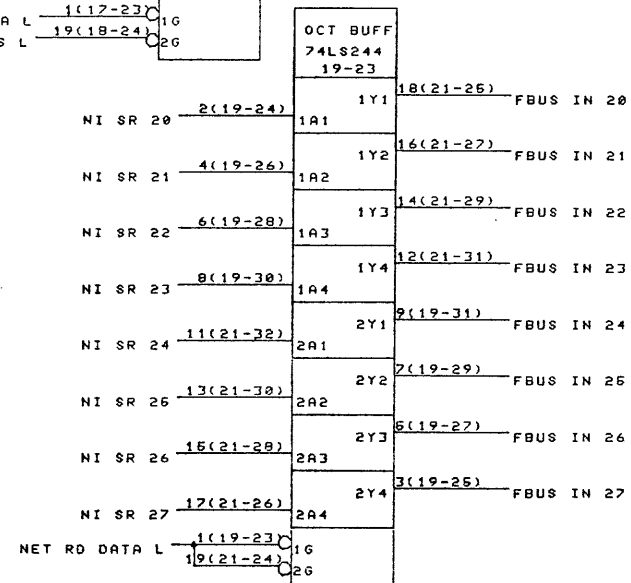
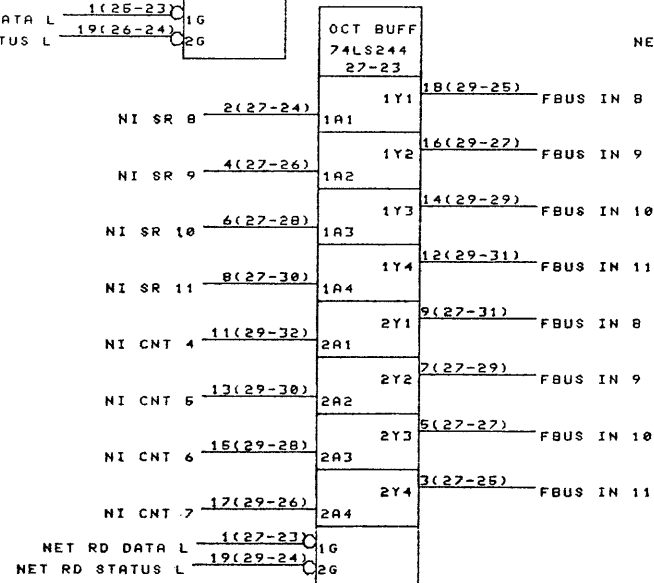
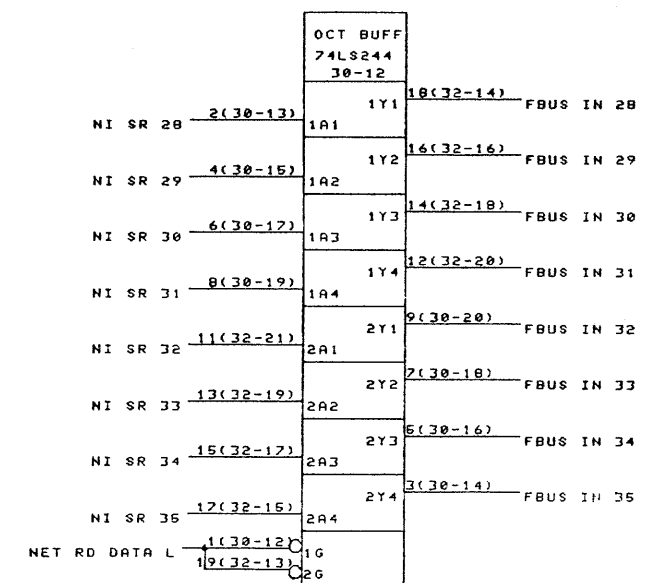
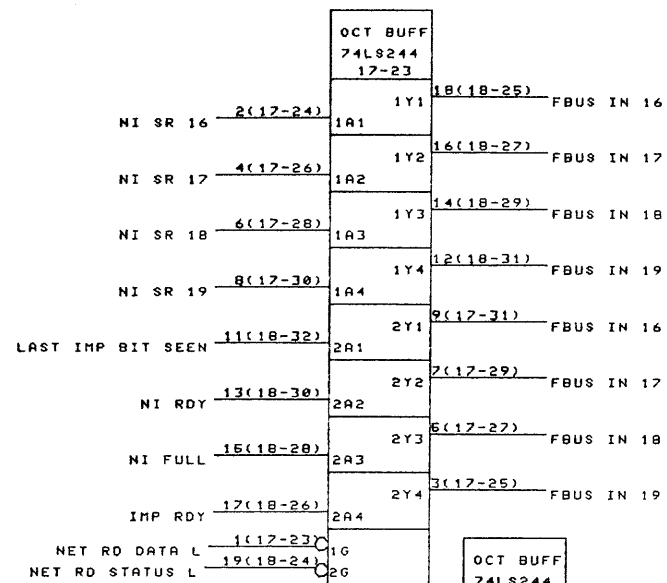
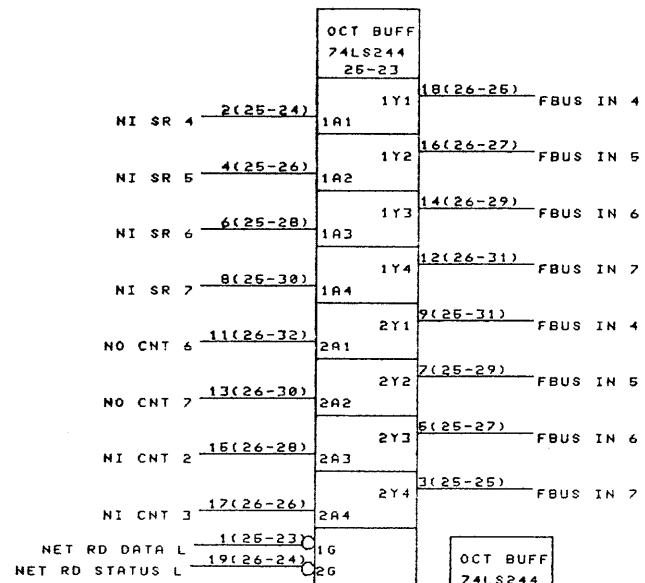
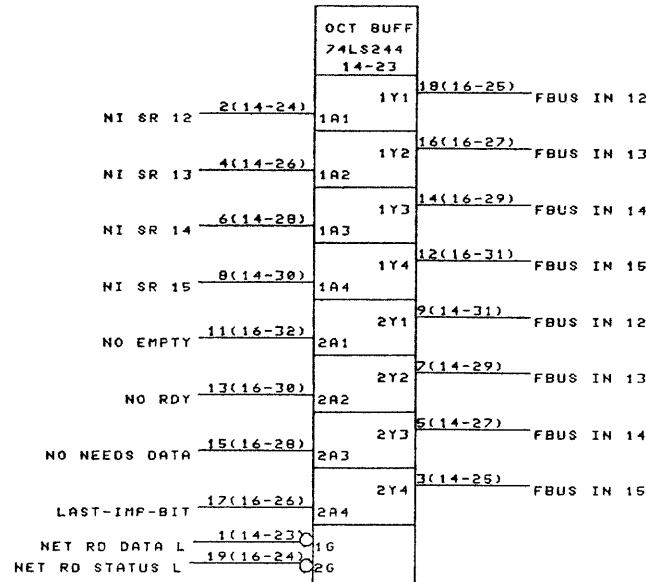
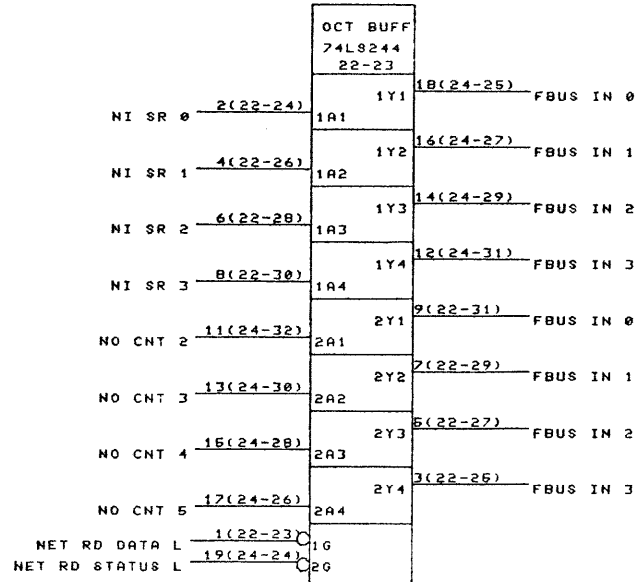


Words are loaded by CPU and shifted out on each clock tic when SHIFT ENB is true.



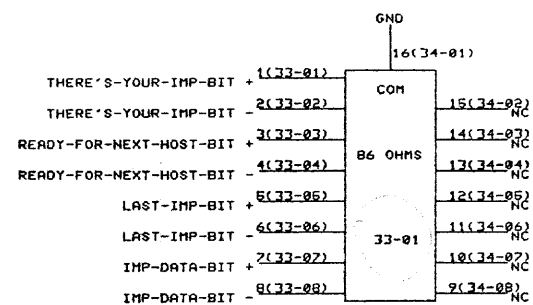
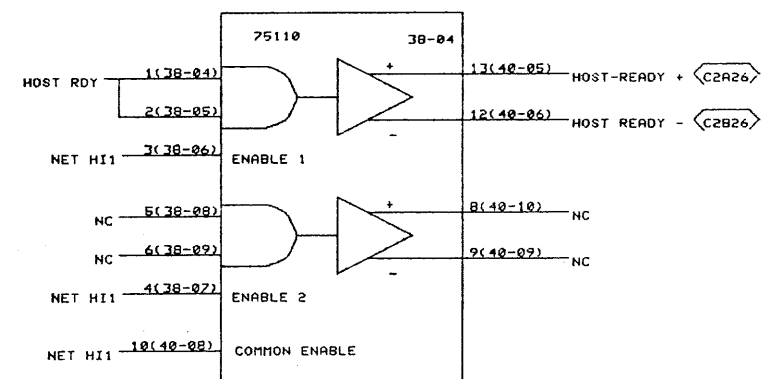
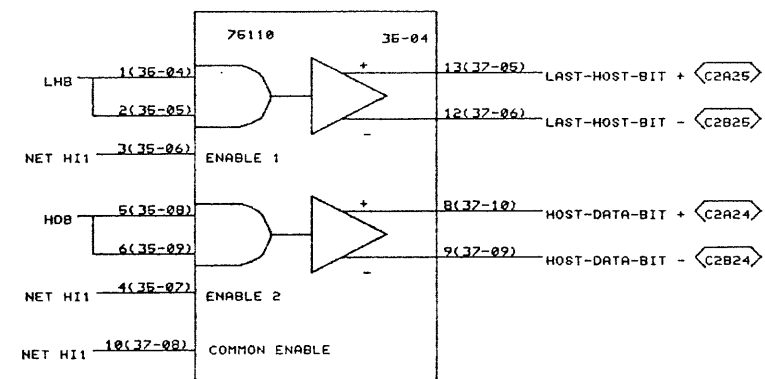
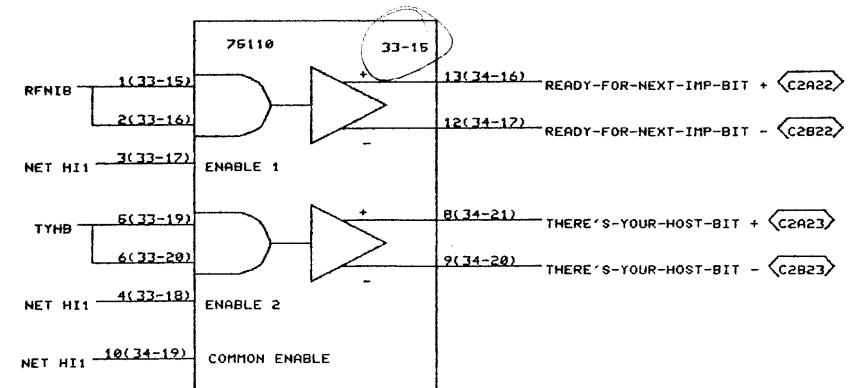
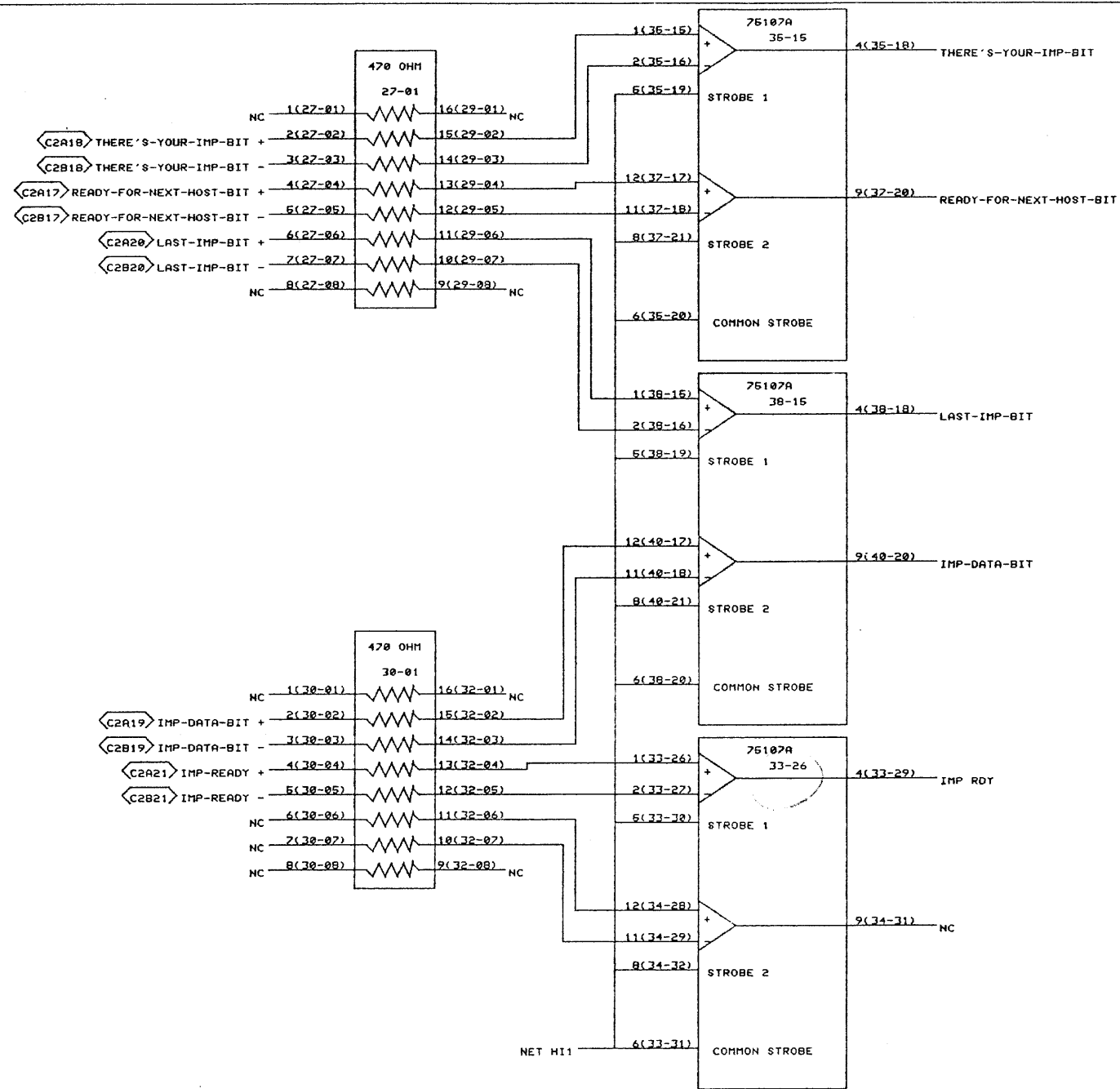
Data from NET is shifted in on the trailing edge of NI RDY and read as a word by the CPU

Foonly, Inc.		LPT/NET Interface NET Shifters		24-JUN-80 03:09	
DRAWN BY: J. Foonly		PAGE 10 OF 17	NUMBER	NETSR.DRW [46,646662]	
APPROVED BY: J. Foonly		PROJECT:	LPT	REV. A	

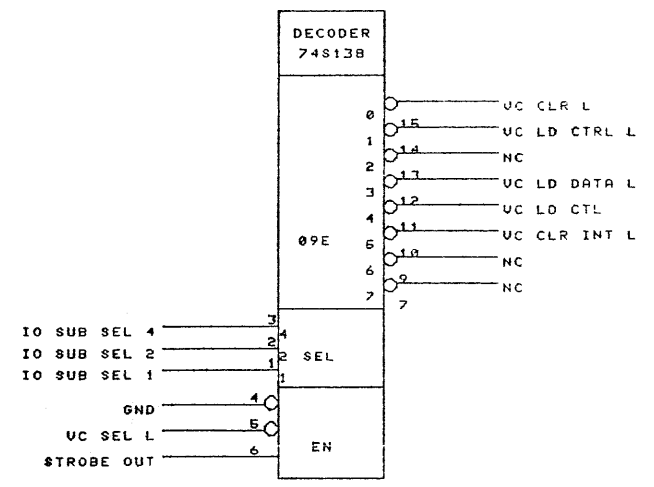
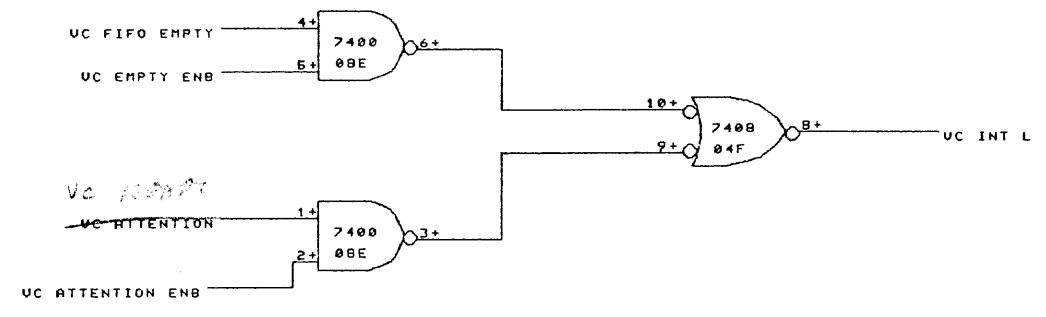
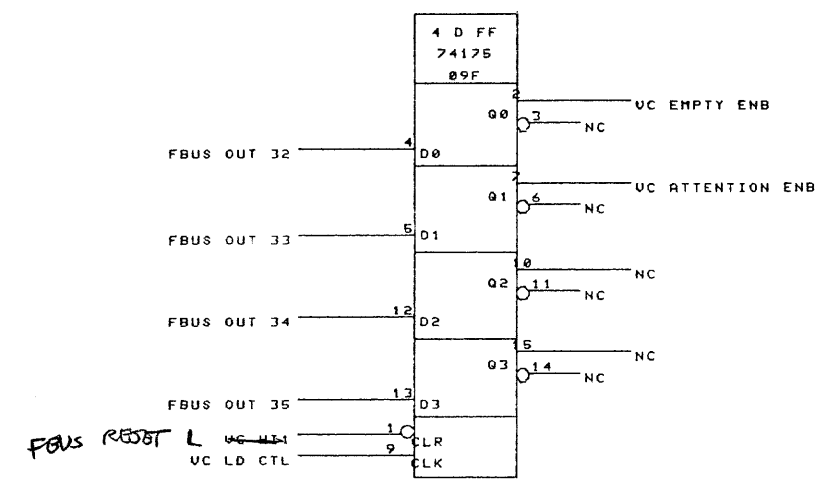
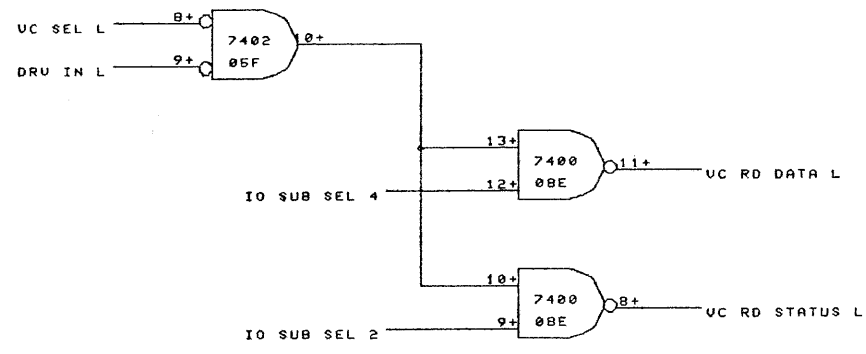


Foonly, Inc.		LPT/NET Interface Net Input Mux		24-JUN-80 03:09
DRAWN BY: <i>S. Foonly</i>		PAGE 11 OF 17	NUMBER	REV. A
APPROVED BY: <i>S. Foonly</i>		PROJECT:	L P T	

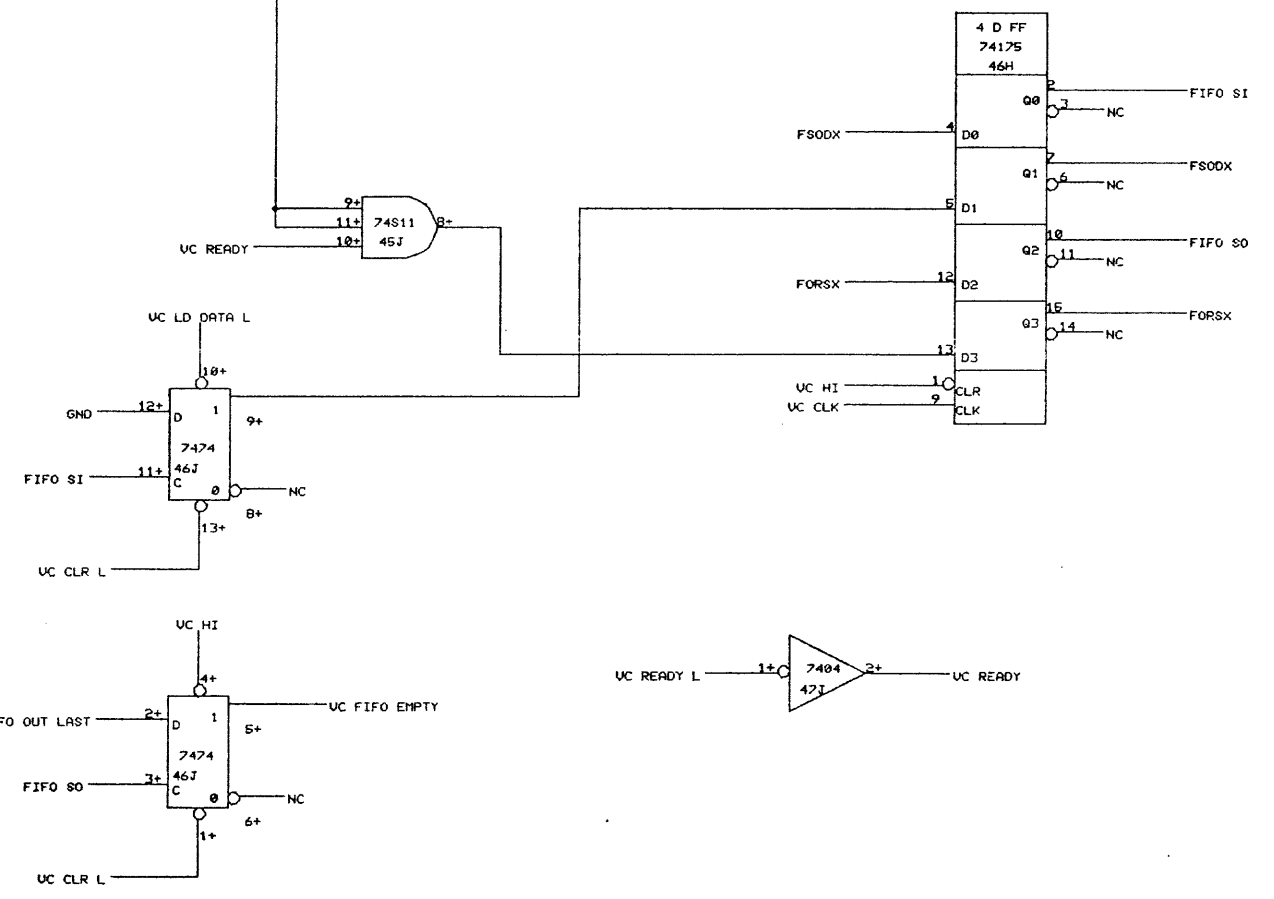
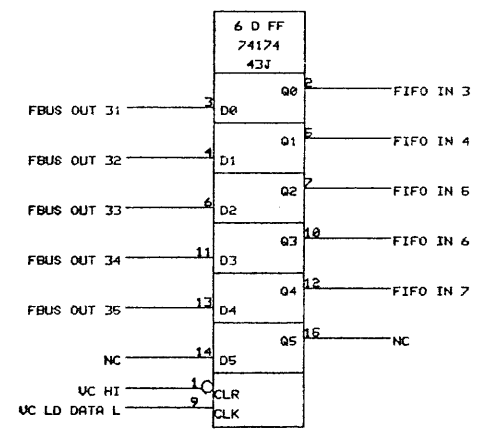
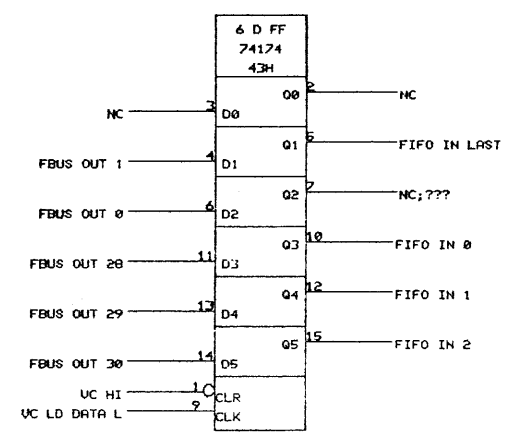
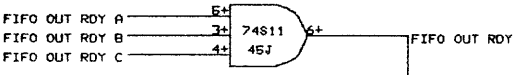
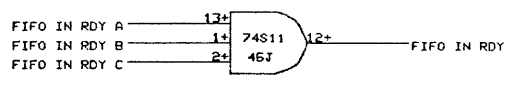
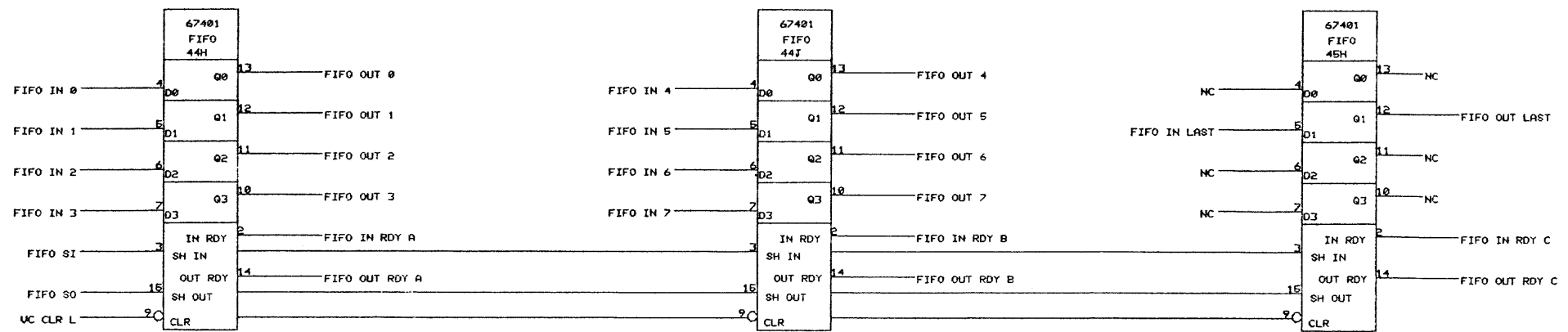
NETIMX.DRW [46,646662]



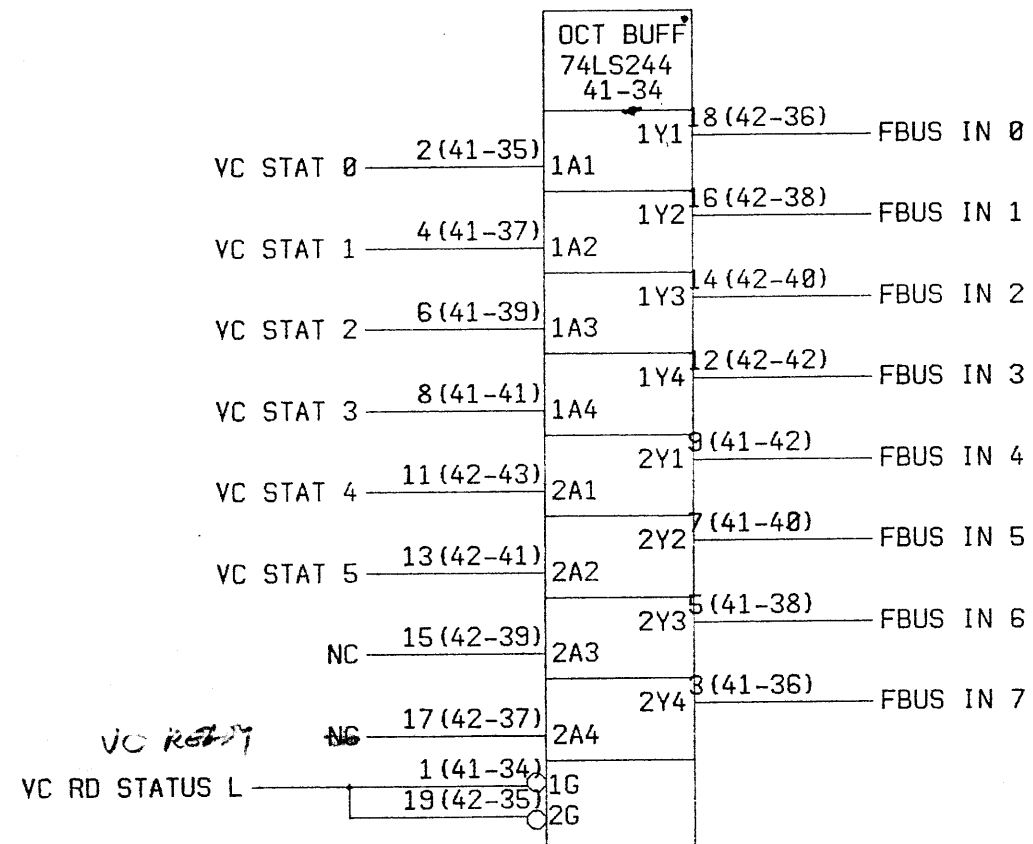
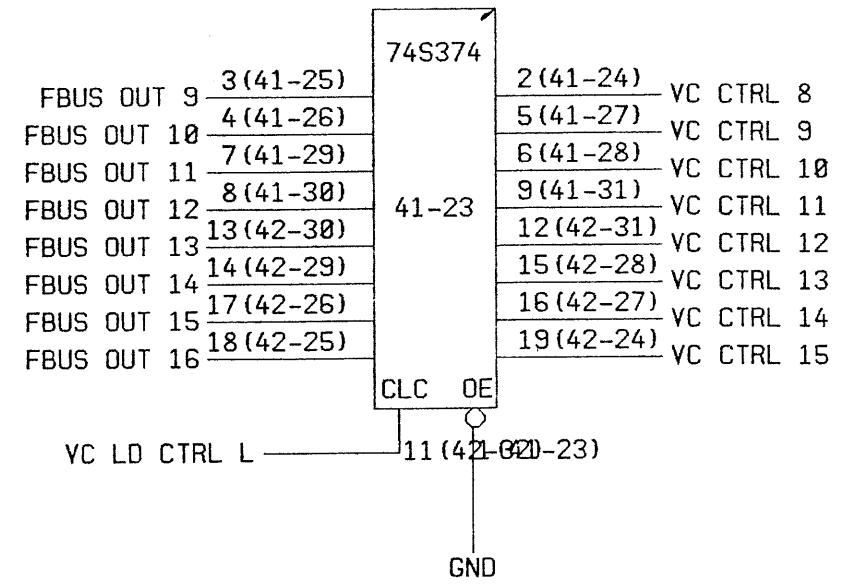
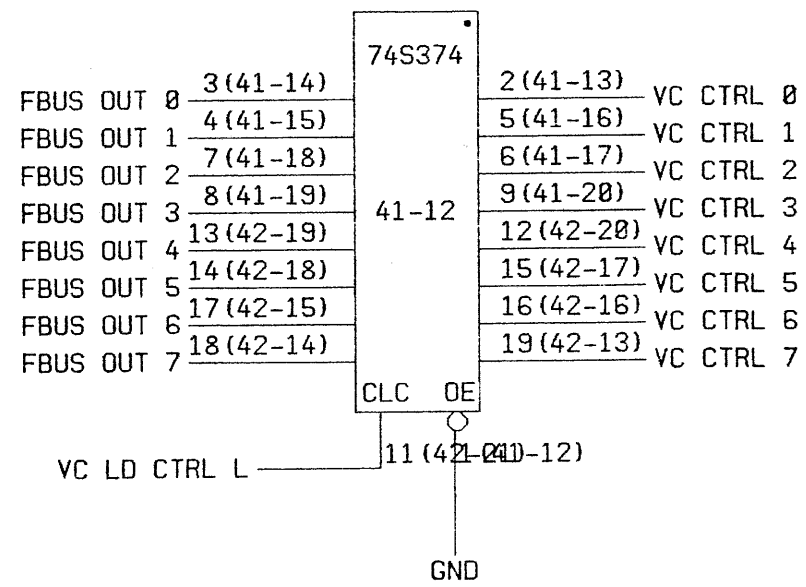
Foonly, Inc.		LPT/NET Interface Level Converters		25-JUN-80 06:40
DRAWN BY: Tovar		PAGE 12 OF 17	NUMBER	REV.
APPROVED BY:		PROJECT:	L P T	A



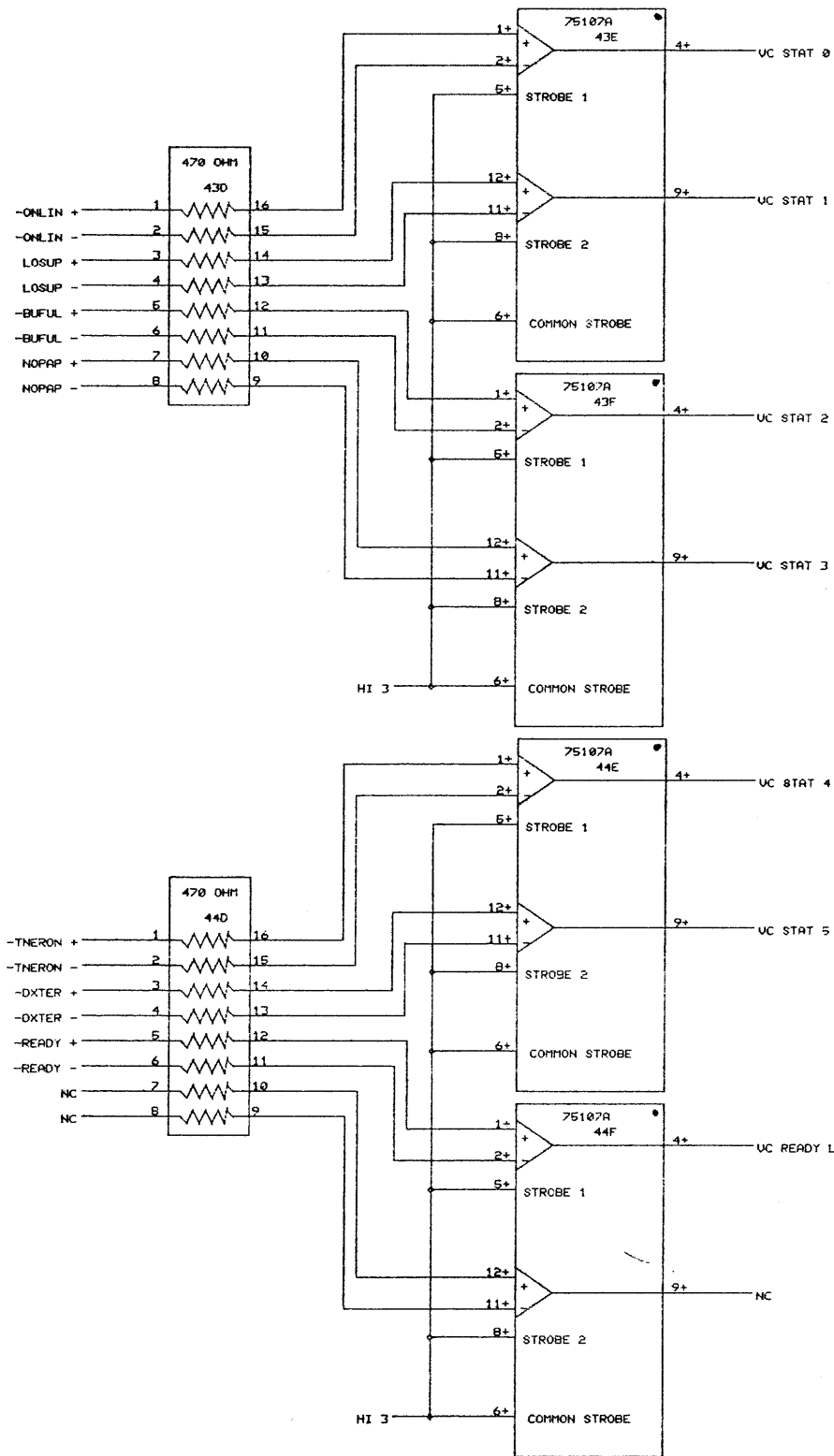
Foonly, Inc.		Versatec/Varian Interface Device Control		24-JUN-80 03:10
DRAWN BY:		PAGE 13 OF 17	NUMBER	REV.
APPROVED BY: <i>J. Foonly</i>		PROJECT:	L P T	A
				VCCT1.DRW [46,646662]



Foonly, Inc.		Versatec/Varian Interface FIFO and control		24-JUN-80 03:11
DRAWN BY:		PAGE 14 OF 17	NUMBER	REV.
APPROVED BY: <i>S. Foonly</i>		PROJECT:	L P T	A

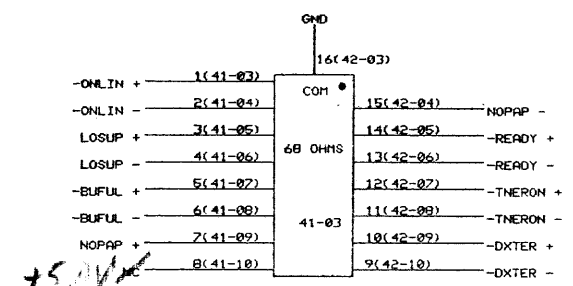


Foonly, Inc.		Versatec/Varian Interface Local buffers		24-JUN-80 03:12	
DRAWN BY:		PAGE 15 OF 17	NUMBER		REV.
APPROVED BY: <i>J. Foonly</i>		PROJECT:	L P T		A
VCLBF.DRW [46,646662]					



garbage

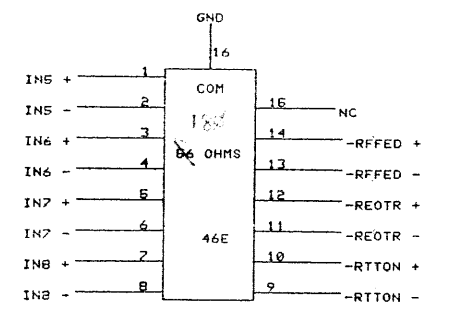
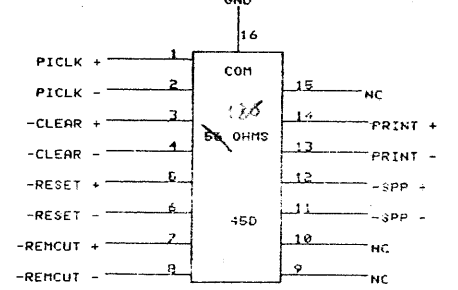
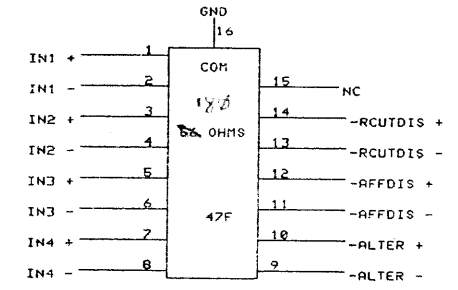
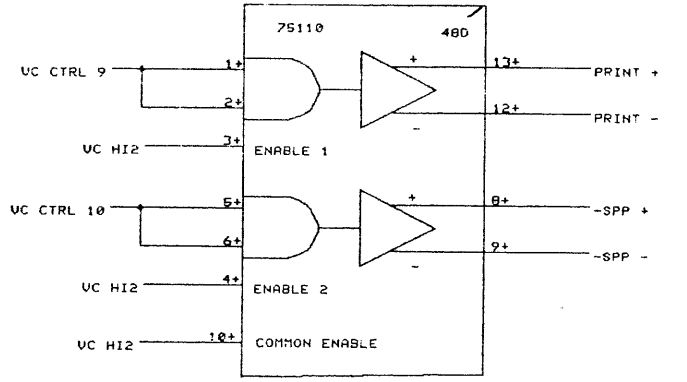
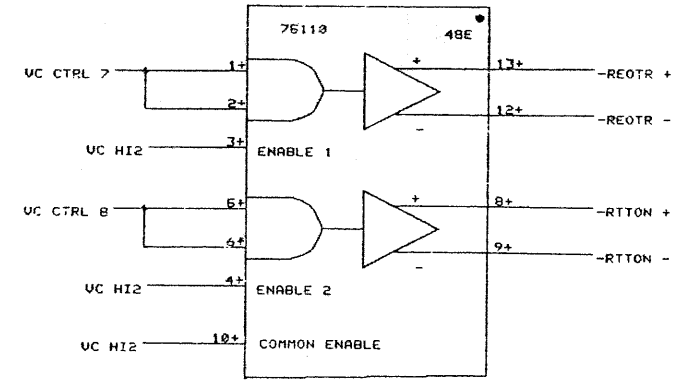
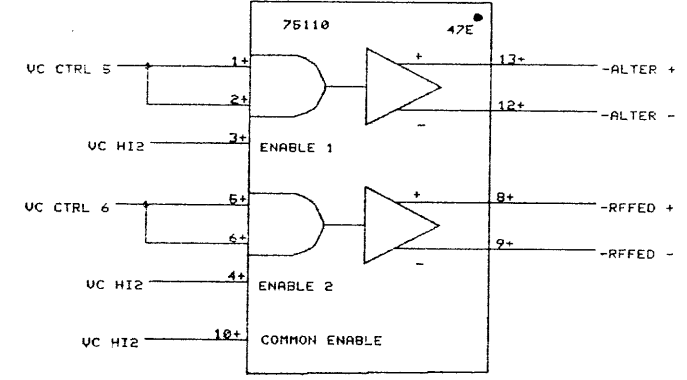
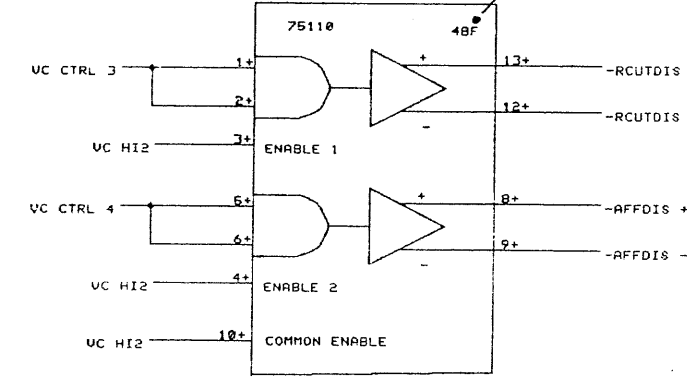
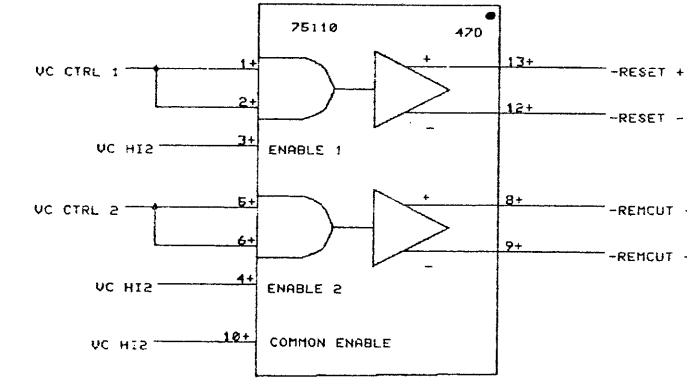
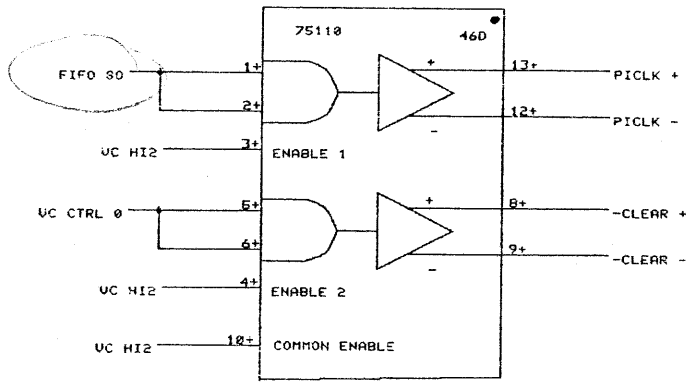
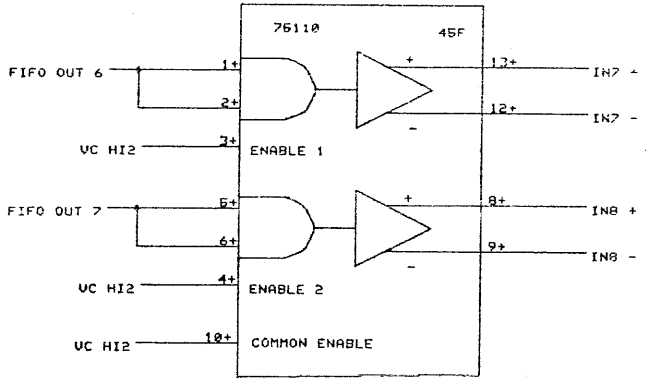
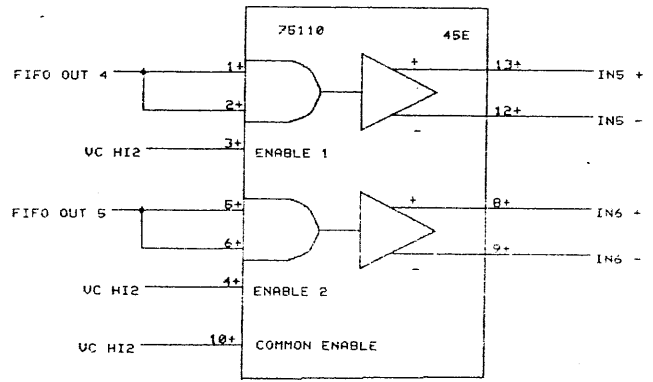
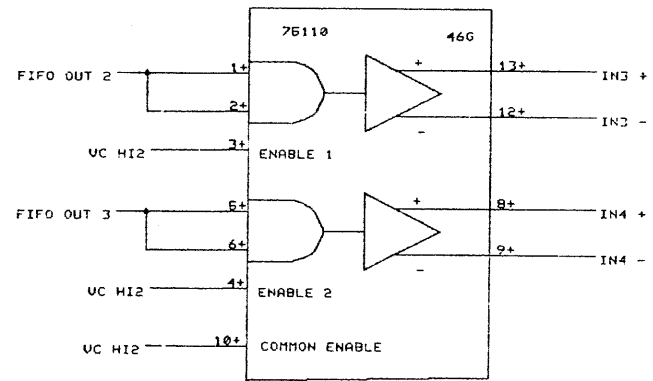
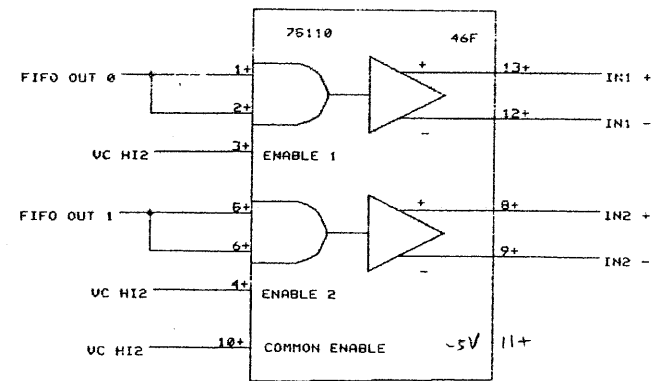
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APPROVED BY: <i>J. Foonly</i>		PROJECT:	L P T	VCLC2.DRW [46, 646662]