SYS68K / ASCU-1/2

HARDWARE USER'S MANUAL

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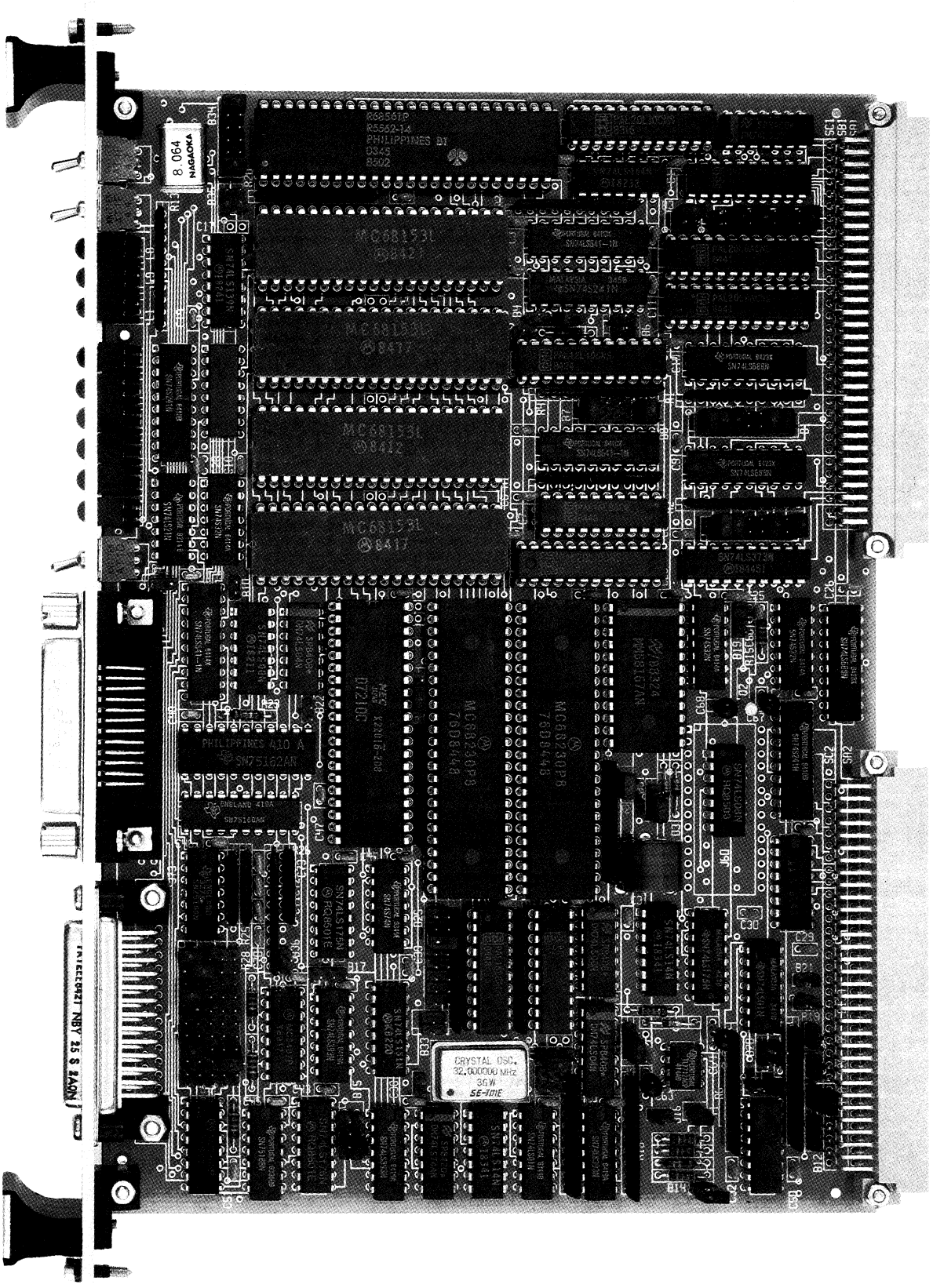


1. General Description SYS68K/ASCU-1/2

The SYS68K/ASCU-1 board is a high performance system controller which handles all exception signals on the VMEbus and contains powerful I/O devices such as a serial interface (RS232 and RS422 compatible), a centronics parallel interface, a real time clock with battery backup, and a 4 level bus arbiter.

The SYS68K/ASCU-2 board provides all the features of the ASCU-1 board as well as a IEEE 488 GPIB interface with Talker, Listener, and Controller functions and powerful interrupt capabilities for multiprocessor environments.

The two block diagrams show the different building blocks in detail.

1.1 Features of the SYS68K/ASCU-1

- 4 level Bus ARBITER with prioritized, round robin, and prioritized round robin operating mode.

- LEDs show the current bus master level (Ø-3)

- High speed serial I/O channel with 68561 Multi-Protocol Communications Controller, RS232 and RS422 driver/receiver circuitries.

- Centronics Parallel Interface for printer connection

- 58167A Real Time Clock with on-board battery back-up

- POWER MONITOR provides automatic power-up/power-down and ACFAIL/SYSRESET handling through power fail detection. A Reset function switch generates a SYSRESET to the VMEbus.

- SYSTEM CLOCK driver (16MHz)

- BUS TIMER with software selectable time-outs for Bus Error generation

- Timer Interrupt can be used for time measurements or as a watch dog

- Software selectable option for generating an interrupt on ACFAIL detection

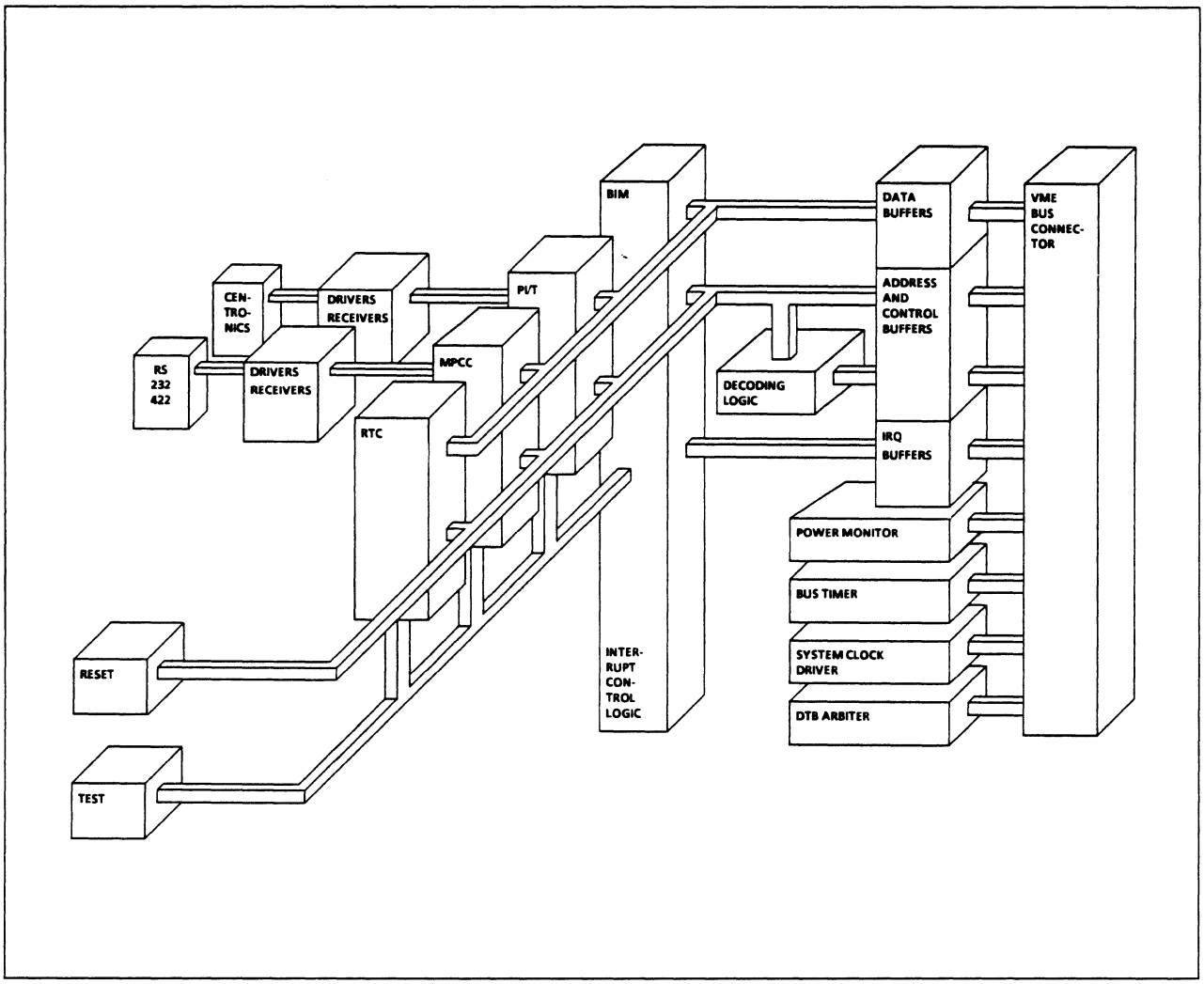
- TEST function switch generates an interrupt to the VMEbus on a software programmable level

- Every I/O device can be programmed to generate an interrupt on one of the 7 IRQ levels on the Priority Interrupt Bus

- Jumper selectable access address and address modifier code(s)

- DTB slave bus interface

Figure 2: Block Diagram of the SYS68K/ASCU-1



1.2 Additional Features of the SYS68K/ASCU-2

- All of the features contained in the SYS68K/ASCU-1 description

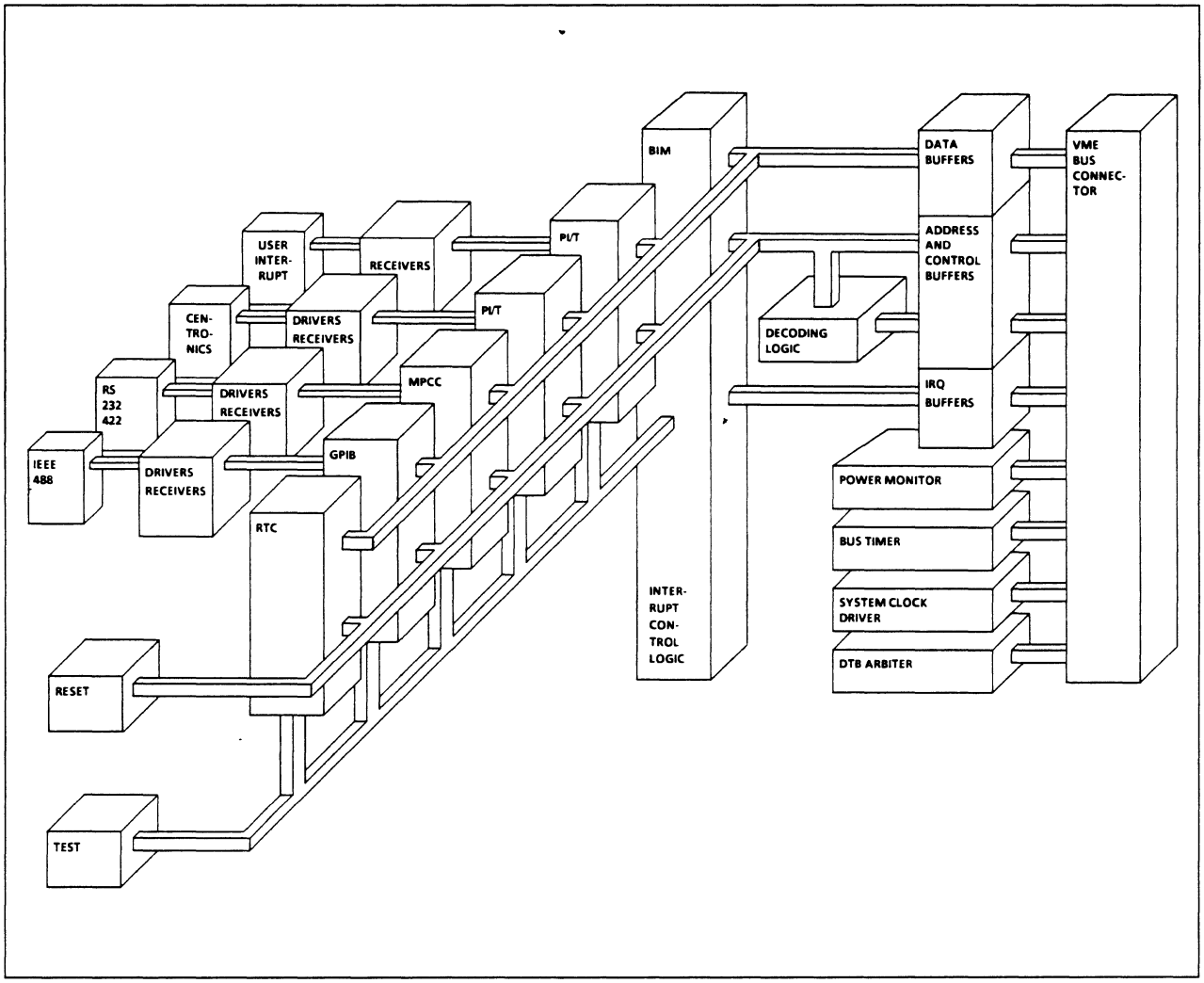
- General Purpose Interface Bus (IEEE488)
  Talker, Listener, and Controller functions

- 8 different fully software programmable interrupts to the VMEbus

- 5 user interrupts (buffered inputs through P2 connector)

- Software programmable time-out for bus mastership of the current bus master

Figure 3: Block Diagram of the SYS68K/ASCU-2



2. Access to the SYS68K/ASCU-1/2

The SYS68K/ASCU-1/2 is accessible under a user defined address and Address Modifier Code.

The decoding includes the Standard Decoding Mode, with an address range of 16Mbytes and short I/O range with 64 Kbytes address range.

To access the board, the jumper settings for the Board Base Address and the Address Modifier Code must match the valid address and Address Modifier Code on the VMEbus. The board is delivered with a default Board Base Address of $B02000. The default jumper setting for the Address Modifier Code is the mode in which the SYS68K/ASCU-1/2 responds to any defined Address Modifier Code.

The SYS68K/ASCU-1/2 occupies an Address Range of 512 bytes, beginning at the Board Base Address. However, within this Address Range, not all locations can be accessed. An access to a non-specified location (no I/O device) will cause a bus trap error. For legal access, please refer to the ASCU-1/2 Device Address Assignment and the Register Map Table of the particular devices.

2.1 Board Base Address Selection

The Base Address of the SYS68K/ASCU-1/2 is jumper selectable in the 16Mbyte address space, in steps of 512 bytes. To select the board, the address on the address lines A9-A23 must match the base address jumper settings at jumper fields B1 and B2.

B1 is the jumper field which defines the bit pattern of the address lines A23-A16. B2 is the jumper field for the address lines A15-A9.

Fig. 4 shows the location of the jumper fields B1 and B2 on the PC board.

Fig. 5 shows the pinout of the jumper fields B1 and B2.

Table 1 points out the connection assignment:

"IN" stands for a connection of the associated pins by a plugged-in jumper,

"OUT" means that the pins are disconnected and the jumper is removed.

Figure 4: Jumper Location Diagram for the Board Base Address Selection

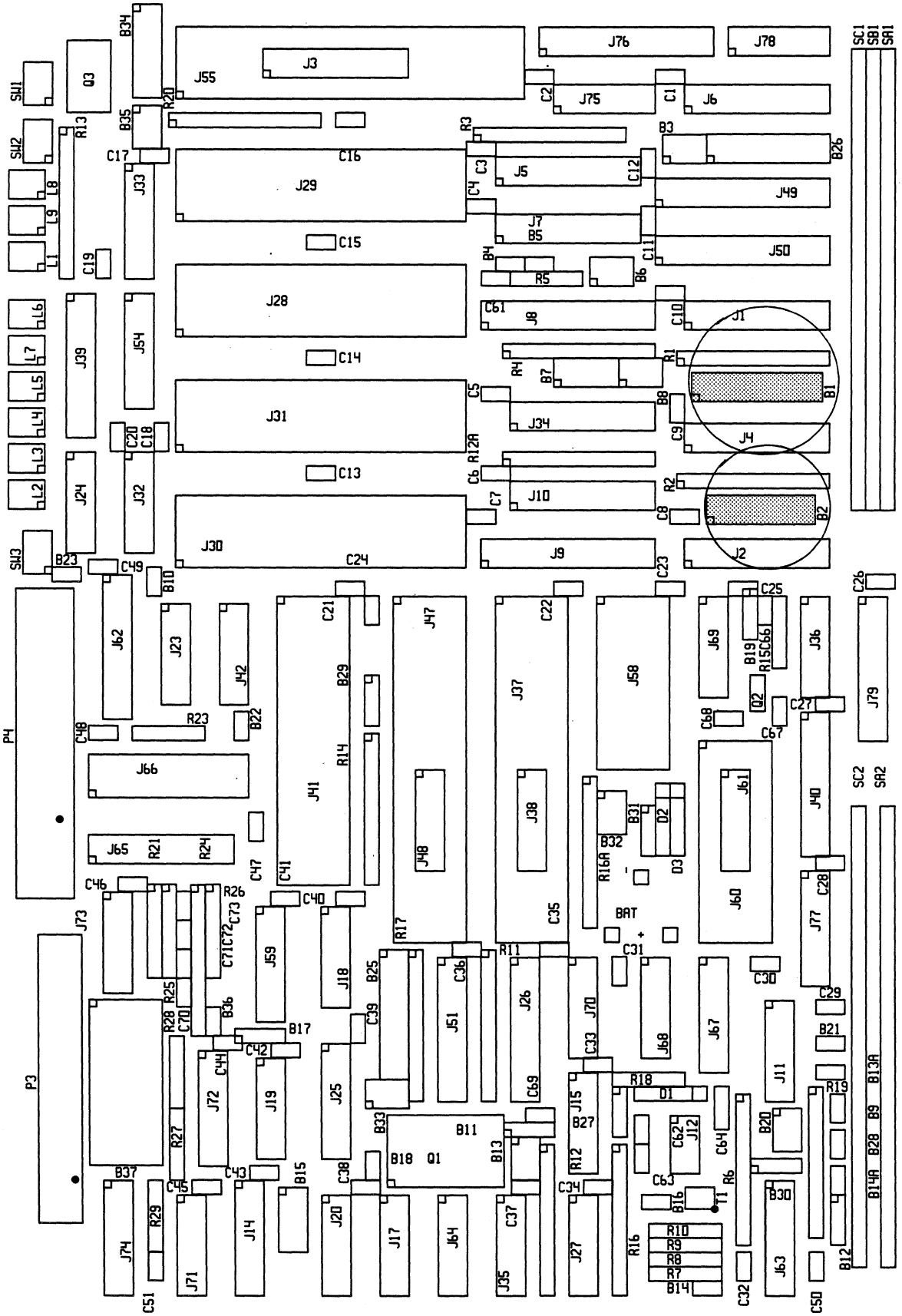


Figure 5: Board Base Address Selection

Jumper Field Pin-out:

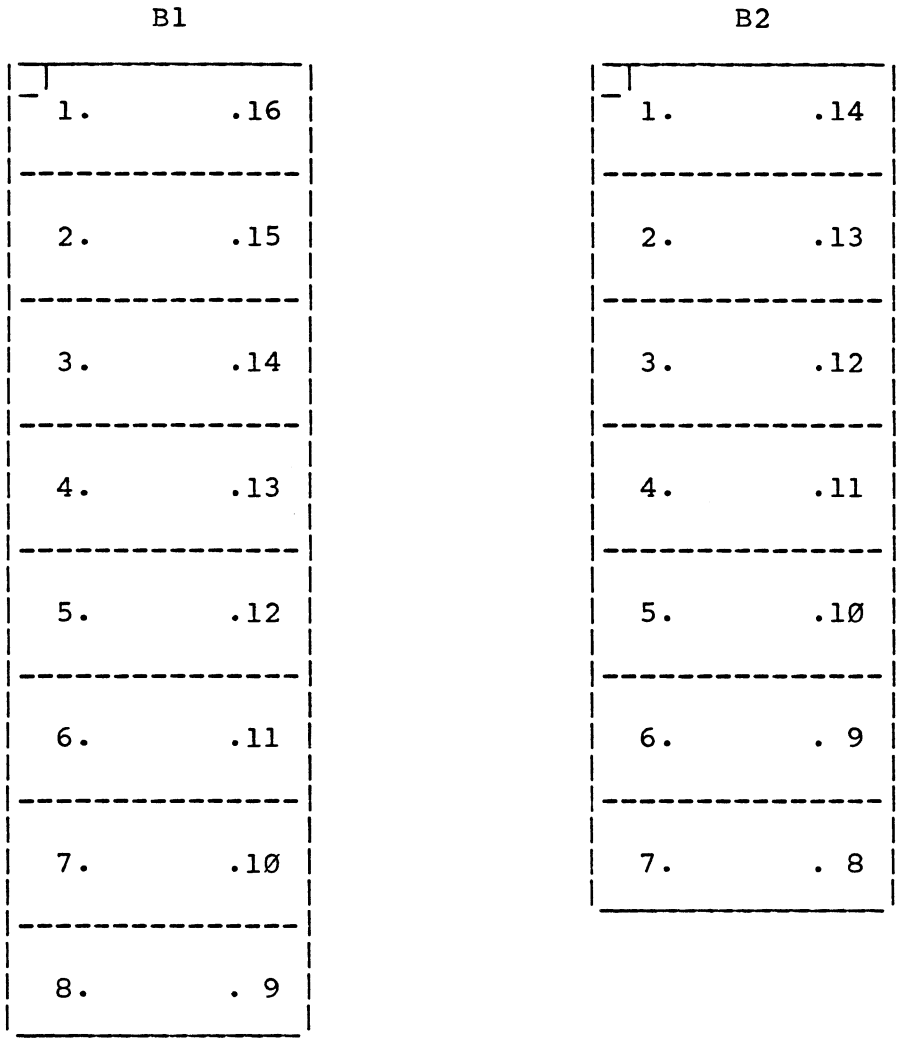


Table 1: Board Base Address Selection

Default Base Address : $BØ2ØØØ

Address Line	Corresponding PINs	Default Jumper Setting	Selection Ø=Jumper IN, 1=OUT
JUMPER FIELD B1			
A23	1 - 16	OUT	1
A22	2 - 15	IN	Ø
A21	3 - 14	OUT	1
A2Ø	4 - 13	OUT	1
A19	5 - 12	IN	Ø
A18	6 - 11	IN	Ø
A17	7 - 1Ø	IN	Ø
A16	8 - 9	IN	Ø
JUMPER FIELD B2			
A15	1 - 14	IN	Ø
A14	2 - 13	IN	Ø
A13	3 - 12	OUT	1
A12	4 - 11	IN	Ø
A11	5 - 1Ø	IN	Ø
A1Ø	6 - 9	IN	Ø
A 9	7 - 8	IN	Ø

2.2 Address Modifier Decoding

The VMEbus has 6 signal lines (AMØ-AM5) carrying the Address Modifier Code which is generated by the bus master together with the address signals. The definition of the AM codes is given in table 2.

The SYS68K/ASCU-1/2 can be accessed with several AM codes, according to the jumper settings in the field B7 and B8. The following AM codes are decoded and selectable as described in table 3. At least one jumper must be inserted, and any combination is allowed. Therefore, the board is able to respond to several AM codes without changing the jumper settings.

Figure 6 outlines the jumper location diagram of the AM jumper field B7 and B8.

Figure 7 shows the pin numbering of B7 and B8.

The default setting in the AM jumper field during manufacturing is as shown in table 3, which causes the board to ignore the AM code.

When selecting the AM code Short Supervisory I/O Access (AM Code, $2D) or Short Non-privileged I/O Access, the decoding is limited to the Address Lines A1 - A15.

Table 2: Address Modifier Codes

HEX Code	Address Modifier 5	4	3	2	1	Ø	Function
3F	H	H	H	H	H	H	Standard Supervisory Block Transfer
3E	H	H	H	H	H	L	Standard Supervisory Program Access
3D	H	H	H	H	L	H	Standard Supervisory Data Access
3C	H	H	H	H	L	L	Reserved
3B	H	H	H	L	H	H	Standard Non-Privileged Block Transfer
3A	H	H	H	L	H	L	Standard Non-Privileged Program Access
39	H	H	H	L	L	H	Standard Non-Privileged Data Access
38	H	H	H	L	L	L	Reserved
37	H	H	L	H	H	H	Reserved
36	H	H	L	H	H	L	Reserved
35	H	H	L	H	L	H	Reserved
34	H	H	L	H	L	L	Reserved
33	H	H	L	L	H	H	Reserved
32	H	H	L	L	H	L	Reserved
31	H	H	L	L	L	H	Reserved
3Ø	H	H	L	L	L	L	Reserved
2F	H	L	H	H	H	H	Reserved
2E	H	L	H	H	H	L	Reserved
2D	H	L	H	H	L	H	Short Supervisory Access
2C	H	L	H	H	L	L	Reserved
2B	H	L	H	L	H	H	Reserved
2A	H	L	H	L	H	L	Reserved
29	H	L	H	L	L	H	Short Non-Privileged Access
28	H	L	H	L	L	L	Reserved
27	H	L	L	H	H	H	Reserved
26	H	L	L	H	H	L	Reserved
25	H	L	L	H	L	H	Reserved
24	H	L	L	H	L	L	Reserved
23	H	L	L	L	H	H	Reserved
22	H	L	L	L	H	L	Reserved
21	H	L	L	L	L	H	Reserved
2Ø	H	L	L	L	L	L	Reserved

L = low signal level
H = high signal level

Table 2 cont'd

HEX Code	Address Modifier 5	4	3	2	1	Ø	Function
1F	L	H	H	H	H	H	User defined
1E	L	H	H	H	H	L	User defined
1D	L	H	H	H	L	H	User defined
1C	L	H	H	H	L	L	User defined
1B	L	H	H	L	H	H	User defined
1A	L	H	H	L	H	L	User defined
19	L	H	H	L	L	H	User defined
18	L	H	H	L	L	L	User defined
17	L	H	L	H	H	H	User defined
16	L	H	L	H	H	L	User defined
15	L	H	L	H	L	H	User defined
14	L	H	L	H	L	L	User defined
13	L	H	L	L	H	H	User defined
12	L	H	L	L	H	L	User defined
11	L	H	L	L	L	H	User defined
1Ø	L	H	L	L	L	L	User defined
ØF	L	L	H	H	H	H	Extended Supervisory Block Transfer
ØE	L	L	H	H	H	L	Extended Supervisory Block Transfer
ØD	L	L	H	H	L	H	Extended Supervisory Block Transfer
ØC	L	L	H	H	L	L	Reserved
ØB	L	L	H	L	H	H	Extended Non-Privileged Block Transfer
ØA	L	L	H	L	H	L	Extended Non-Privileged Program Access
Ø9	L	L	H	L	L	H	Extended Non-Privileged Data Access
Ø8	L	L	H	L	L	L	Reserved
Ø7	L	L	L	H	H	H	Reserved
Ø6	L	L	L	H	H	L	Reserved
Ø5	L	L	L	H	L	H	Reserved
Ø4	L	L	L	H	L	L	Reserved
Ø3	L	L	L	L	H	H	Reserved
Ø2	L	L	L	L	H	L	Reserved
Ø1	L	L	L	L	L	H	Reserved
ØØ	L	L	L	L	L	L	Reserved

L = low signal level
H = high signal level

Table 3: Address Modifier Code Selection

AM Code HEX	Function	Jumper-field	PINS	Decoded Address Lines
3D	Standard Supervisory Data Access	B7	1-8	A1-A23
39	Standard Non-privileged Data Access	B7	2-7	A1-A23
2D	Short Supervisory I/O Access	B7	3-6	A1-A15
29	Short Non-privileged I/O Access	B7	4-5	A1-A15
XX *	Ignore any code	B8	1-4	A1-A23
3F	Standard Access Mode for CPU boards which do not drive the AM signal lines. This AM code is not decoded in the sense of the P1Ø14 Block Transfer Definition.	B8	2-3	A1-A23

* Default setting

Figure 6: Jumper Location Diagram for the Address Modifier Code Selection

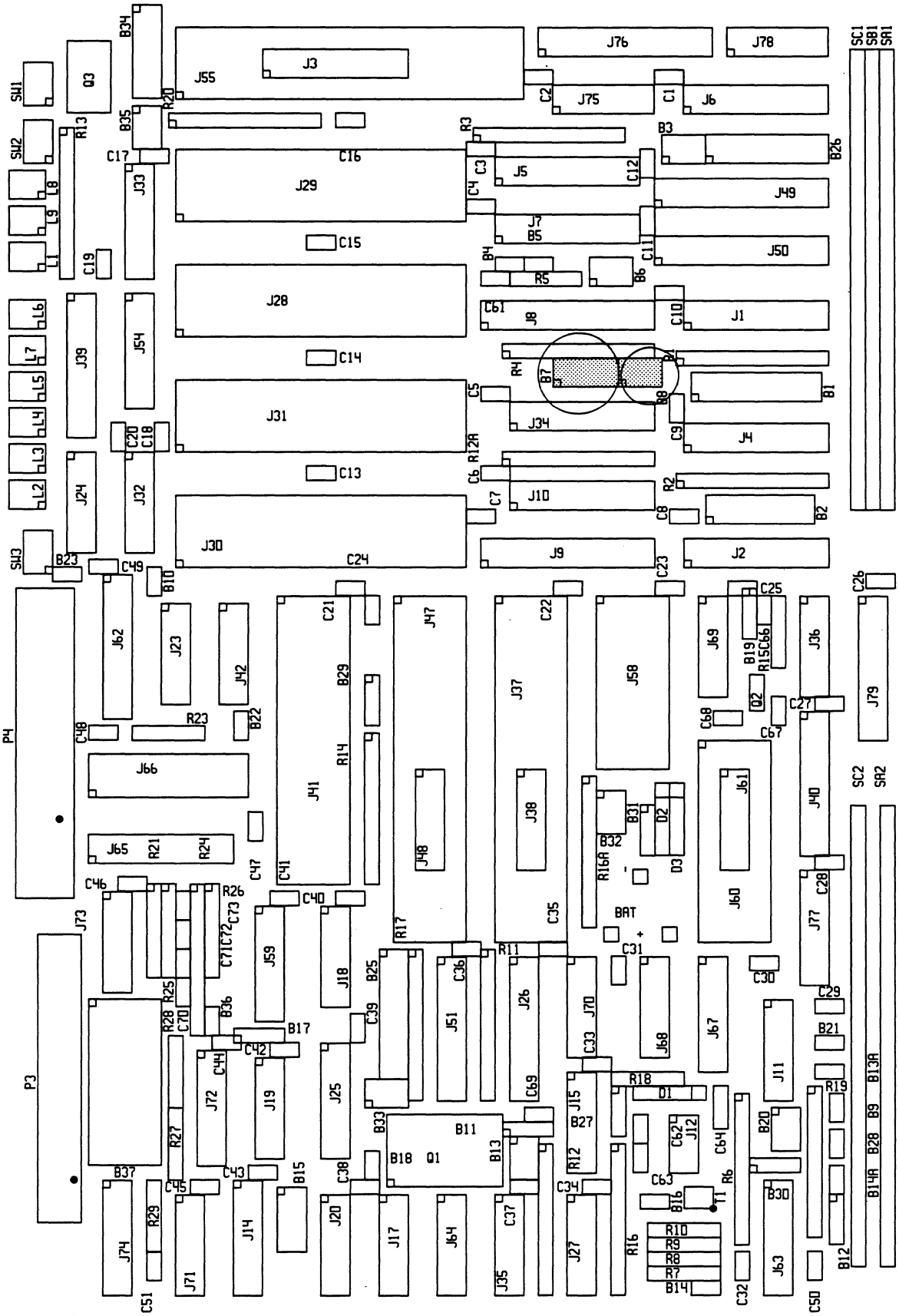
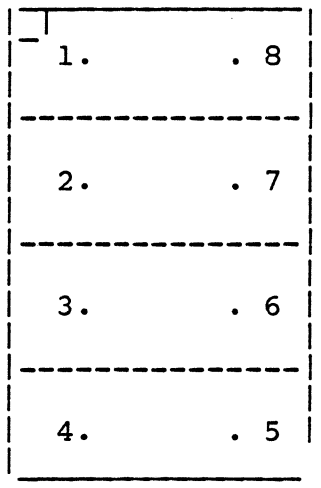


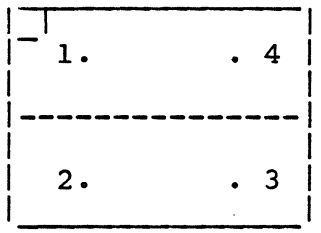
Figure 7: Address Modifier Code Selection

Jumper Field Pin-out:

B7:



B8:



2.3 Application Examples

Example 1):

If the Board Base Address has to be changed to $A574ØØ and the board should operate with the Standard Supervisory Data Access (AM Code: $3D) as well as the Standard Non-Privileged Data Access (AM Code: $39), then the following jumper settings have to be provided:

	Address Line	Jumper Setting	Selection
Jumper Field B1:	A23	OUT	1
	A22	IN	Ø
	A21	OUT	1
	A2Ø	IN	Ø
	A19	IN	Ø
	A18	OUT	1
	A17	IN	Ø
	A16	OUT	1
Jumper Field B2:	A15	IN	Ø
	A14	OUT	1
	A13	OUT	1
	A12	OUT	1
	A11	IN	Ø
	A1Ø	OUT	1
	A 9	IN	Ø

	AM-Code (HEX)	Connected PINs
Jumper Field B7:	3D	1-8
	39	2-7

Example 2):

In this example, the Short Board Base Address $1600 with the AM-Code for Short Non-Privileged I/O access ($29) is selected. It is irrelevant, in this case, which jumper settings are made in the field B1, because the address lines A16-A23 will not be decoded.

The following jumper connections have to be installed:

	Address Line	Jumper Setting	Selection
Jumper Field B2:	A15	IN	Ø
	A14	IN	Ø
	A13	IN	Ø
	A12	OUT	1
	A19	IN	Ø
	A1Ø	OUT	1
	A 9	OUT	1

	AM-Code (HEX)	Connected PINs
Jumper Field B7:	29	4-5

3. The Front Panel

3.1 RESET Function Switch

The switch on the top of the SYS68K/ASCU-1/2 front panel is the RESET function switch. Pushing this switch can generate a SYSRESET* signal to the VMEbus, and resets all devices on the SYS68K/ASCU-1/2. The SYSRESET* signal is signaled by the red RESET LED on the front panel (Figure 8). For further information, please refer to chapter 8 - "Utility Signal Handling" and "Power Monitor Module".

3.2 TEST Function Switch

The second switch on the front panel is the TEST function switch. It generates an interrupt request to the VMEbus. The interrupt level and vector is software programmable. The TEST function is inactive after the power-up procedure. For correct operation please refer to chapter 15 - "TEST Interrupt".

3.3 The SYSFAIL LED

The red SYSFAIL LED signals the status of the corresponding Utility Bus Signal Line SYSFAIL*.

This signal line is used to indicate that a local selftest of a board is in progress, or a system test has been started by an intelligent master board. During this test procedure the signal line is driven low.

The SYSFAIL* line may be driven by any module in the system that is able to detect faults.

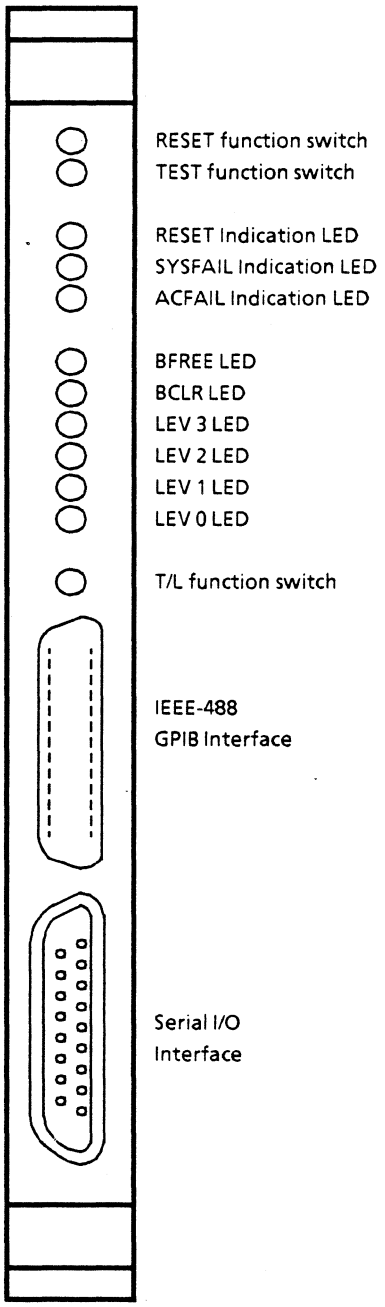
It may also be driven low at any time during normal operation to indicate that some kind of failure has occurred. Further details can be found in chapter 5.

3.4 The ACFAIL LED

The red ACFAIL LED is built onto the SYS68K/ASCU-1/2 board as a visual indicator of power failures. The LED will signal a power failure when the ACFAIL* signal line is asserted.

The signal handling of the ACFAIL* signal is described in chapter 5 "Utility Signal Handling".

Figure 8: The Front Panel of the SYS68K/ASCU-2



3.5 BUS ARBITRATION STATUS LEDs

The SYS68K/ASCU-1/2 is equipped with six Bus Arbitration Status LEDs which show the activity of the Bus Arbiter and the bus load.

The LEDs are designated on the front panel as follows:

BFREE	(green)
BCLR	(red)
LEV 3	(yellow)
LEV 2	(yellow)
LEV 1	(yellow)
LEV Ø	(yellow)

The BUSFREE LED turns on after the power-up procedure is terminated, when the SYSRESET* signal line has been cleared. Further on, the BUSFREE LED is controlled by the BBSY* signal line.

This signal line is driven to a high level if no Bus Master has control of the Data Transfer Bus. On this condition, the BUSFREE LED will light up.

The asserted BBSY* signal line indicates that a Bus Master has control of the Data Transfer Bus and the BUSFREE LED will turn off.

The BUSFREE LED will also turn off if the SYSRESET* signal line is asserted.

The BCLR (Bus Clear) LED signals the asserted BCLR* signal which is either generated by the on-board ARBITER or the BCLR-Timer. (The BCLR-Timer is installed only on the SYS68K/ASCU-2).

The red BCLR LED provides the visual information that the current Bus Master is requested to release the Data Transfer Bus.

To monitor the level on which the current Bus Master is operating, the SYS68K/ASCU-1/2 provides four yellow LEDs, (LEV 3 to LEV Ø).

These LEDs are attached to four daisy-chained Bus lines which are defined in the VMEbus and P1Ø14* specification as Bus Grant (Ø-3) OUT lines (BGx OUT).

The relation of the LEDs to the Bus Grant lines are as follows:

LEV 3	->	BG 3 OUT
LEV 2	->	BG 2 OUT
LEV 1	->	BG 1 OUT
LEV Ø	->	BG Ø OUT

When the Arbiter grants the Data Transfer Bus to a requesting board by asserting the BGx OUT line, the LEV(x) LED will turn on (where x is a number Ø, 1, 2 or 3).

For a detailed description of the Bus Arbitration function, please refer to chapter 1Ø - "The 4-Level Bus ARBITER", and chapter 11 - "The BCLR-TIMER".

3.6 The T/L Switch (included only on the ASCU-2)

The T/L toggle switch (only provided on the ASCU-2) provides a status signal, readable via the Port C of the second PI/T device.

* P1Ø14 - Bus Specification (VMEbus) of the IEEE Computer Society TC.

3.7 IEEE-488 GPIB Connector (included only on the ASCU-2)

The ASCU-2 provides a high performance IEEE-488 Interface (also called GPIB, HPIB, or IEC bus interface) with a 24 pin microribbon connector mounted on the front panel (see figure 8).

The mechanical construction and the mounting of the connector meets fully the IEEE-488 specification and allows stacked connection of interface cables.

The pin assignment of the connector is given in table 4.

Table 4: IEEE 488 Connector Pin Assignment

Contact	Signal Line	Contact	Signal Line
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EOI (24)	17	REN (24)
6	DAV	18	Gnd,(6)
7	NRFD	19	Gnd,(7)
8	NDAC	2Ø	Gnd,(8)
9	IFC	21	Gnd,(9)
1Ø	SRQ	22	Gnd,(1Ø)
11	ATN	23	Gnd,(11)
12	SHIELD	24	Gnd,LOGIC

NOTE: Gnd,(n) refers to the signal ground return of the referenced contact. EOI and REN return on contact 24.

A comprehensive description of the interface is given in chapter 17 - "The IEEE-488 GPIB Interface".

3.8 Serial Interface Connector

The 25-pin female D-sub connector is available on the front panel (see figure 8), and provides the connection to the RS232 and RS422-compatible Serial Interface.

The pin assignment to the connector of the two interfaces is completely jumper selectable.

The default pin assignment during manufacturing is given in table 5, using the RS232 interface.

This allows the connection of a standard terminal after initialization of the MPCC device.

For further information, please refer to chapter 12 - "The Serial I/O".

Table 5: The Default I/O Signal Assignment to the D-Sub-Connector

Terminal Signal	D-Sub-Connector
DTR	20
CTS	5
RX DATA	3
TX DATA	2
GND	1
GND	7

All other signals are not connected by default during manufacturing.

4. Interrupt Structure of the SYS68K/ASCU-1/2

This chapter describes the Interrupt Structure of the SYS68K/ASCU-1/2.

A short description of the following terms is given in Appendix G (Glossary of P1Ø14 Terms) at the end of this manual.

Terms:

- INTERRUPT HANDLER
- INTERRUPTER
- INTERRUPT BUS
- INTERRUPT ACKNOWLEDGE CYCLE
- DAISY CHAIN

For a detailed description please refer to the IEEE P1Ø14/VMEbus Specification.

Introduction:

The P1Ø14 Standard Specification defines a Priority Interrupt Bus with seven interrupt request lines (IRQ1-IRQ7). Each interrupt request line is assigned one interrupt level.

In a Single Handler System, where one Interrupt Handler services all interrupt requests, the signal line IRQ7 has the highest priority, and IRQ1 the lowest. Interrupters drive the interrupt request line low when requesting an interrupt. The Interrupt Handler honours the request by asserting the IACK* line, putting the level code on the address lines AØ-A3, and driving AS* low. The Interrupter then terminates the Interrupt Acknowledge Cycle providing the Interrupt Vector on the data bus lines DØ-D7 and drives DTACK* low. More than one Interrupt Request Line can be driven simultaneously, and the same Interrupt Request Line can be asserted by several boards.

If more than one Interrupt Request Line is asserted at the same time, the Interrupt Handler prioritizes the requests and services them in order of priority.

If two or more Interrupter Modules request an interrupt at the same IRQ level, the Interrupter Modules themselves decide in which order the Interrupt Handler will acknowledge the interrupts.

To make sure that only one Interrupt responds to the interrupt acknowledge cycle, the VMEbus/P1Ø14 specification defines an Interrupt Acknowledge Daisy Chain structure with the Interrupt Acknowledge Daisy Chain line IACKIN*/IACKOUT*.

This line passes through each board on the system, whereby the IACKOUT* pin of each Interrupter Module is connected to the IACKIN* pin of the next Interrupter Module.

After leaving the board at slot n with the IACKOUT* line, this line enters the next board at slot n+1 with the IACKIN* line.

Each interrupter having a pending Interrupt Request only responds to the cycle when it receives a falling edge on the IACKIN* daisy chain input. It puts the Interrupt Vector onto the data bus and drives the DTACK* line low. This interrupter does not assert the IACKOUT* pin, preventing other interrupters from responding to the interrupt acknowledge cycle.

An interrupter asserts its IACKOUT* output when it has no Interrupt Request pending or when its pending Interrupt Request level differs from the one being acknowledged in the current cycle.

The Interrupt Acknowledge daisy chain operates from the left side to the right side of the backplane, giving priority to boards further left.

The IACKIN* line starts at the first slot and has to be connected to the IACK* bus line.

For this purpose the jumperfield B4 is provided on the board. An inserted jumper in this field connects the bus lines IACK* with the IACKIN* line of the board.

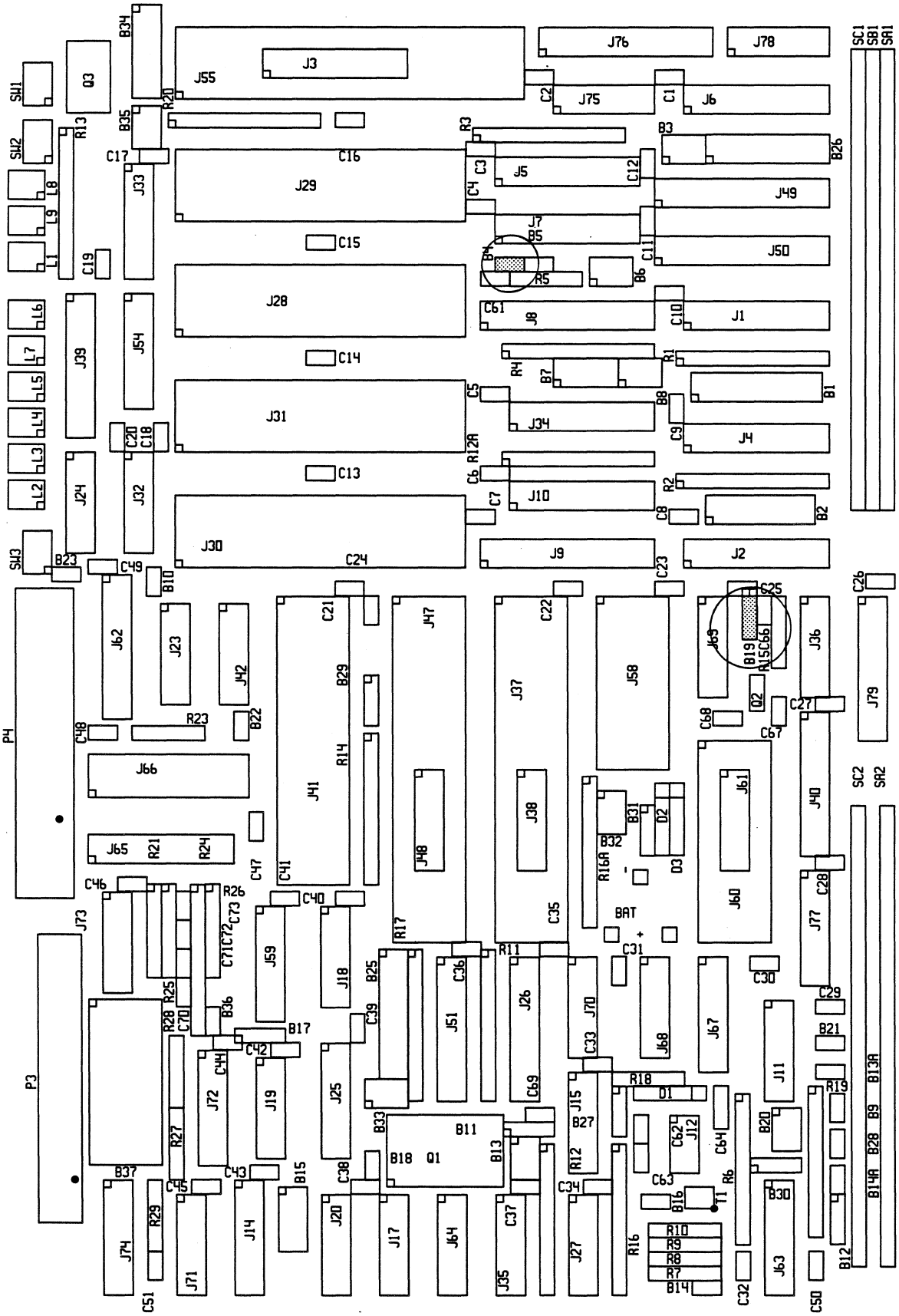
This jumper has to be inserted if the SYS68K/ASCU-1/2 is located at slot 1, but must be removed when the board is plugged into other slot positions. The default condition during manufacturing is a plugged-in jumper.

The jumper on jumperfield B19 connects the on-board Interrupt Acknowledge daisy chain line to the IACKOUT* bus line. This jumper is not user selectable.

In the default condition on the SYS68K/ASCU-1 the jumper connects pins 2 and 3 of B19, and on the SYS68K/ASCU-2, pins 1 and 2 are connected.

Figure 9 outlines the location of the jumperfields B4 and B19.

Figure 9: Jumperfield Location Diagram of B4 and B19



4.1 Programming of the BIM on the ASCU-1/2

The SYS68K/ASCU-1/2 contains Bus Interrupter Modules (BIM 68153) to transmit the Interrupt Request Signals of peripheral devices (also called Interrupt Sources) to the VMEbus and the Interrupt Acknowledge Signal from the VMEbus to the interrupt sources. All interrupt sources are arbitrated by the BIMs.

The SYS68K/ASCU-1 has two BIMs on the board serving seven interrupt sources.

The SYS68K/ASCU-2 board is equipped with four BIM devices supporting sixteen interrupt sources.

Each Bus Interrupter Module has the capability to drive each Interrupt Request line on the VMEbus. It also provides a vector if the Interrupter does not support the vectored protocol. Both functions, the selection of the Interrupt Request Level as well as the supplied interrupt vector are fully under software control.

The BIM contains two types of registers: The Control Register, and the Vector Register.

Programming the Control Register allows the selection of the Interrupt Request Level as well as to enable or disable this function. If the interrupting source does not provide the interrupt vector, the Control Register can be programmed to give out the contents of the associated Vector Register as the required Interrupt Vector.

When the BIM device is reset, it prevents the interrupt generation from the board to the VMEbus.

For detailed information, please refer to the data sheet of the BIM 68153 in Appendix H.

4.2 Interrupt Sources and IACK Daisy Chain Structure of the SYS68K/ASCU-1/2

For easier comprehension of the interrupt structure of the SYS68K/ASCU-1/2 it is helpful to consider all Bus Interrupter Modules on the board as a single device providing several interrupt channels.

Each interrupt source is assigned one interrupt channel. Every interrupt channel has an associated software programmable Control Register and Vector Register and can be programmed to generate an Interrupt Request on every IRQ-level of the VMEbus. It depends on the interrupting device, whether the Vector Register of the interrupt channel or the interrupt source by itself supplies the vector.

The following interrupt sources are provided on the SYS68K/ASCU-1/2. The list also shows the assigned interrupt channel number.

		Interrupt Channel Number	
- PORT INTERRUPT OF PI/T 1		1	
- TIMER INTERRUPT OF PI/T 1		2	
- ACFAIL		3	
- SYSFAIL		4	
- TEST INTERRUPT		5	
- RTC		6	
- MPCC		7	
- GPIB CONTROLLER		8	*
- 8 PROGRAMMABLE INTERRUPTS	BIM J3Ø	9-12	*
	BIM J31	13-16	*

* available only on ASCU-2

The on-board daisy chain structure is hardware defined and operates in the order given in Table 6.

When all interrupt sources are working on the same IRQ-level, the SYSFAIL interrupt source has the highest priority. The lowest priority on the ASCU-1 has the TEST INTERRUPT source, on the ASCU-2 the PROGRAMMABLE INTERRUPT source with Interrupt Channel number 13.

Table 6: Sequence of the On-Board IACK Daisy Chain

Interrupt Source	Channel No.	Comment
SYSFAIL	4	highest priority
ACFAIL	3	
TIMER INTERRUPT OF PI/T 1	2	
PORT INTERRUPT OF PI/T 1	1	|| decreasing || \/ priority
GPIB CONTROLLER	8	
MPCC	7	
RTC	6	
TEST INTERRUPT	5	
PROGRAMMABLE INTERRUPT PA3	12	
PA2	11	
PA1	10	
PA0	9	
PROGRAMMABLE INTERRUPT PA7	16	
PA6	15	
PA5	14	
PA4	13	lowest priority

A summary of the interrupt sources and the assigned channel numbers and register addresses is shown in table 55 "Interrupt Channel Addressing".

4.3 Interrupt Vector Structure

All interrupt sources on the SYS68K/ASCU-1/2 are arbitrated by the Bus Interrupter Modules which provide one interrupt vector for each interrupt source.

The BIM can be programmed to honour an Interrupt Acknowledge with the content of its vector register or to send the acknowledge signal to the interrupt source.

The SYS68K/ASCU-1/2 has three different groups of interrupt sources:

The first group are interrupt sources, which do not supply an interrupt vector.

This group must be supported by the BIM which must provide the interrupt vector. The BIM Control Register has to be programmed appropriately. Table 7 lists the affected interrupt sources with interrupt channel and BIM register address offset related to the Board Base Address.

Table 7: Non-vectorized Interrupt Sources

Interrupt Source	Interrupt Channel Number	Interrupter Device	Offset- Board Base Address BIM Control Register	BIM Vector Register	
ACFAIL	3	BIM 1	$105	$10D	
SYSFAIL	4	BIM 1	$107	$10F	
TEST INTERRUPT	5	BIM 2	$111	$119	
REAL TIME CLOCK	6	BIM 2	$113	$11B	
GPIB CONTROLLER	8	BIM 2	$117	$11F	*
PROGRAM. INTERRUPT	9	BIM 3	$121	$129	*
PROGRAM. INTERRUPT	10	BIM 3	$123	$12B	*
PROGRAM. INTERRUPT	11	BIM 3	$125	$12D	*
PROGRAM. INTERRUPT	12	BIM 3	$127	$12F	*
PROGRAM. INTERRUPT	13	BIM 4	$131	$139	*
PROGRAM. INTERRUPT	14	BIM 4	$133	$13B	*
PROGRAM. INTERRUPT	15	BIM 4	$135	$13D	*
PROGRAM. INTERRUPT	16	BIM 4	$137	$13F	*

* ONLY INCLUDED ON THE ASCU-2

The second group is an Interrupt Source, which always supplies its own vector when it honours an Interrupt Acknowledge Cycle.

This interrupt source is the Multi Protocol Communication Controller (MPCC 68561).

The MPCC has three vector registers:

- Receiver Interrupt Vector Number Register (RIVNR)
- Transmitter Interrupt Vector Number Register (TIVNR)
- Serial Interrupt Vector Number Register (SIVNR)

As the MPCC always serves an interrupt acknowledge cycle with one of its own vectors, the BIM has to be programmed for an external interrupt acknowledge response.

The register address assignment of the MPCC interrupt source is shown in the table below:

Table 8: Vectorized Interrupt Source

Interrupt Source	Interrupt Channel Number	Offset to Board Base Address BIM 2		MPCC		
		Control Register	Vector Register	Vector Register	Byte Mode	Word Mode
MPCC	7	$115	not used	RIVNR:	$ØØ5	$Ø25
				TIVNR:	$ØØD	$Ø2D
				SIVNR:	$Ø15	$Ø35

The third group of interrupt sources can be enabled or disabled of providing the interrupt vector. The user can therefore choose whether the interrupt source or the BIM provides the vector.

The two independent interrupt sources belonging to this group reside in the Parallel Interface/Timer Module PI/T 1 (6823Ø).

The timer has one interrupt vector available which is programmable in the 8-bit wide Timer Interrupt Vector Register of the PI/T 1 device. If the timer is enabled to support the vectored interrupt, the BIM must not provide the interrupt vector.

Table 9 shows the timer interrupt channel address assignment (offset to Board Base Address)

Table 9: Optional Vectorized Interrupt Source 1

Interrupt Source	Interrupt Channel Number	Offset to Board Base Address: BIM 1 Control Reg.	Offset to Board Base Address: BIM 1 Vector Reg.	Offset to Board Base Address: PI/T 1 Timer Interrupt Vector Register
TIMER	2	$1Ø3	$1ØB	not used
	2	$1Ø3	not used	TIVR:$Ø63

The Port Interrupt of the PI/T 1 device has one associated vector register, but it represents four consecutive vector numbers. As the BIM can only provide one vector for the Port Interrupt, it is recommendable to handle the BIM transparent, always selecting the external vector generation of the PI/T 1 device.

Table 1Ø shows the Port Interrupt channel address assignment (offsets to Board Base Address).

Table 1Ø: Optional Vectorized Interrupt Source 2

Interrupt Source	Interrupt Channel Number	Offset to Board Base Address: BIM 1 Control Reg.	Offset to Board Base Address: BIM 1 Vector Reg.	Offset to Board Base Address: PI/T 1 Port Interrupt Vector Register
PORT INTERRUPT	1	$1Ø1	$1Ø9	not used
	1	$1Ø1	not used	PIVR: $Ø4B

5. Utility Signal Handling

The SYS68K/ASCU-1/2 handles the utility signals SYSRESET*, SYSFAIL* and ACFAIL* which are provided by the Utility Bus, and supply initialization and diagnostic capabilities for a VME/P1Ø14 standard system.

5.1 The SYSRESET* Signal

The SYS68K/ASCU-1/2 board can be configured to drive the SYSRESET* signal line or not to drive it. Figure 1Ø outlines the jumper location diagram B16 with which the function can be selected.

Jumper B16 inserted -> SYSRESET* is driven to the VMEbus

removed -> SYSRESET* is not driven to the VMEbus

The SYSRESET* signal is driven to the VMEbus by default during manufacturing.

The SYSRESET* Bus signal is always received by the board and resets each of the devices described in the following table.

Table 11: RESET on the ASCU-1/2

	Abbreviation	Device	
BUS INTERRUPTER MODULE 1	BIM 1	68153	
BUS INTERRUPTER MODULE 2	BIM 2	68153	
BUS INTERRUPTER MODULE 3	BIM 3	68153	*
BUS INTERRUPTER MODULE 4	BIM 4	68153	*
PARALLEL INTERFACE/TIMER MODULE 1	PI/T 1	6823Ø	
PARALLEL INTERFACE/TIMER MODULE 2	PI/T 2	6823Ø	*
MULTI PROTOCOL COMMUNICATION CONTROLLER	MPCC	68561	
GENERAL PURPOSE INTERFACE BUS CONTROLLER	GPIB	721Ø	*
REAL TIME CLOCK	RTC	58167A	

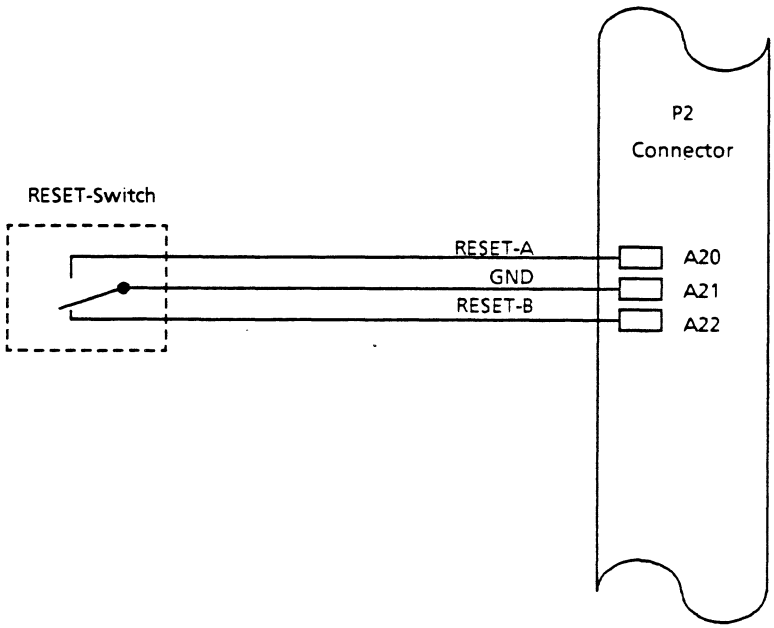
* included only on the SYS68K/ASCU-2.

The whole SYSRESET* exception signal handling is performed by the POWER MONITOR MODULE. It generates a SYSRESET signal during power-up sequence, and monitors five reset sources. If any of the five sources becomes active, the Power Monitor Module asserts the SYSRESET* signal line (providing that Jumper B16 is inserted).

The five reset sources are:

1) The RESET switch on the FRONT PANEL,

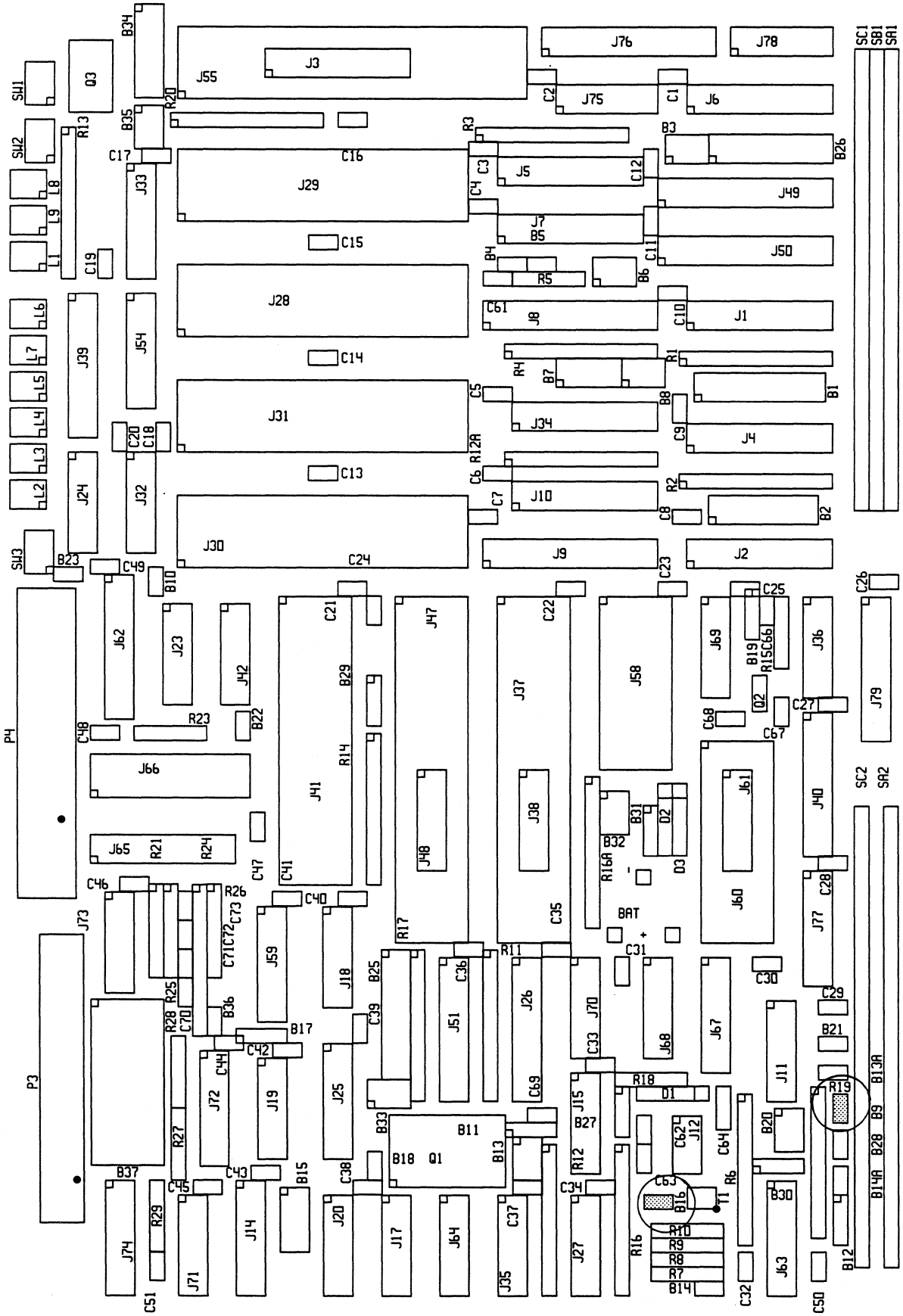
2) An optional switch connected to the P2 connector pins A2Ø, A21, A22. This switch should be connected in the following way:



To enable the function switch, the jumper B9 has to be removed. If there is no switch connected, the jumper must be plugged in. This is the default condition during manufacturing.

Figure 1Ø outlines the location diagram of the jumperfield B9 on the board.

Figure 1Ø: The SYSRESET Jumperfield B16 and the Jumperfield B9 for the External Reset Switch Connection

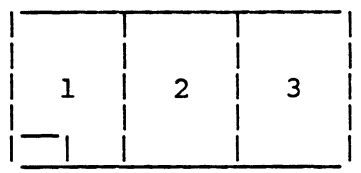


3) A second optional RESET switch can be connected to the P2 connector - PIN A2. This pin is a TTL-compatible input and generates a reset execution if the switch closes the pin to ground.

This pin is a double function pin also providing a signal ground for the Data 1 line of the CENTRONICS Interface, which is installed on the board. Therefore, selecting the function of the second optional RESET switch or the Centronics Interface, the jumper B3Ø has to be changed according to the following table.

Figure 11 shows the location diagram for Jumperfield B3Ø.

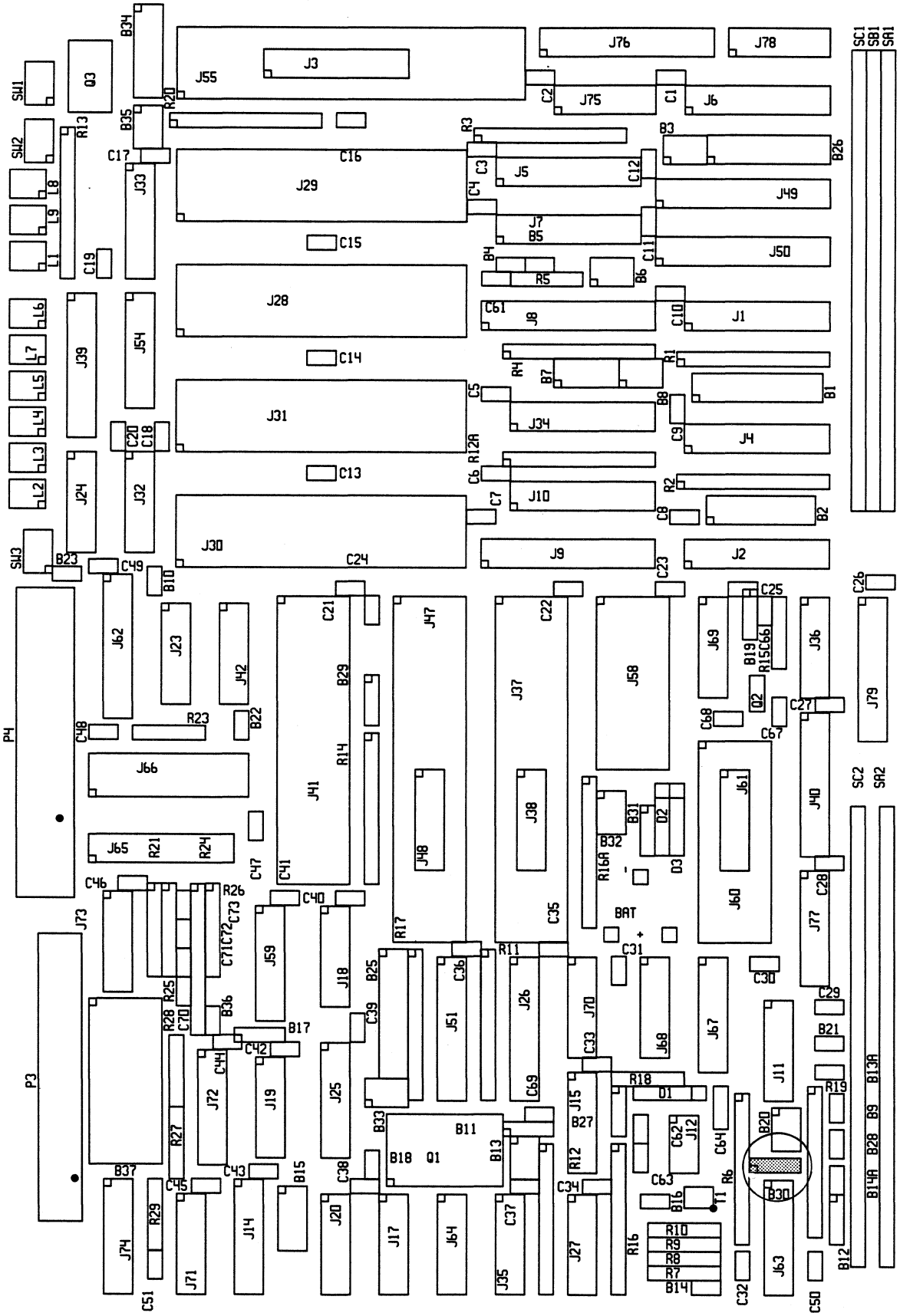
Jumperfield B3Ø



	Jumperfield B3Ø Connected Pins
Centronics Interface *	1 - 2
Optional Reset Switch	2 - 3

* default condition

Figure 11: Jumperfield B30 for Selection of the Centronics Interface/second Optional RESET Switch



4) A software programmable SYSRESET* execution is provided by the SYS68K/ASCU-1/2.

The function is directed by the signal PB7 of the PI/T 1 Parallel Interface, and can be activated if the PB7 signal is set to a logical Ø (low state).

This function becomes inactive after the SYS68K/ASCU-1/2 board has been reset.

If the board does not drive the SYSRESET* signal to the VMEbus, the programmable reset function has no effect on the on-board devices.

More information about the programming of this function is available in chapter 7 "Software Control".

5) Reset after ACFAIL* detection.

This function can be enabled or disabled by inserting or removing the jumper B1Ø.

In default, the Reset after ACFAIL* detection function is enabled with an inserted B1Ø jumper.

Figure 12 shows the location diagram of the jumper B1Ø.

Detailed information about reset after ACFAIL* detection is given in section 5.3, "ACFAIL* Signal", and chapter 8, "Power Monitor Module".

5.2 The SYSFAIL* Signal

The SYSFAIL* signal line is monitored by the SYS68K/ASCU-1/2 and the status of the line is shown by the red SYSFAIL LED, mounted on the Front Panel. Additionally, a second LED can be connected to the P2 Connector Pin C23 and Pin C24.

Pin C24 provides the signal level for the second LED and Pin C23 sources the supply current. The LED is directly connectable without using an external resistor.

The SYSFAIL* signal line is used for system diagnostics and may be driven by any system module able to detect faults.

The SYS68K/ASCU-1/2 provides an Interrupt Request generation to the VMEbus after the board has received the signal line at low-state.

The interrupt level and the vector is fully software programmable through the control register and the vector register of a Bus Interrupter Module (BIM).

The following table shows the offset of the two BIM registers to the Board Base Address.

Interrupt Source	Interrupt Channel Number	Interrupter Device	Offset to Board Base Address	
			Control Reg.	Vector Reg.
SYSFAIL*	4	BIM 1	$1Ø7	$1ØF

For the initialization of the registers, please refer to section 4.1 "Programming of the BIM on the ASCU-1/2" and section 4.3 "Interrupt Vector Structure".

5.3 The ACFAIL* Signal

The SYS68K/ASCU-1/2 provides the connection of an external power fail signal on two pins of the P2 Connector. This power fail signal is typically driven by the System Power Supply to indicate AC power failure.

The board drives the power fail signal to the VMEbus ACFAIL* line and receives the signal from this open collector bus line.

The ACFAIL* line is always received by the ASCU-1/2 board, therefore, the line can also be driven by another board in the system.

The external power fail signal can be connected to the ASCU-1/2 board at the following pins on Connector P2:

Connector P2 - Pin A1
Pin A27

The Pin A1 of the P2 Connector is a double function pin and also provides the signal ground for the DATA STROBE signal of the Centronics Interface.

A jumper on the Jumperfield B12 selects the A1 pin either as a power fail input pin or a signal ground for the Centronics Interface Data Strobe line.

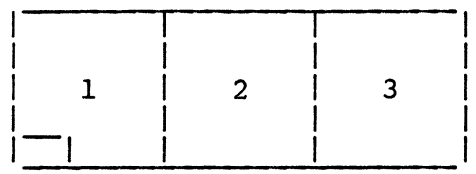
In the default jumper setting during manufacturing the A1 pin functions as signal ground.

The following table lists the B12 jumper settings for these two functions.

	PIN A1 Function	Jumperfield B12 Connected PINs
Connector P2 PIN A1 -->	Centronics I.F. Data Strobe Signal GND	2 - 3 *
-->	Power Fail Input-Pin	1 - 2

* Default jumper setting.

Pin-Out of Jumperfield B12



To adjust a Power Fail signal which is either true on low state (Ø) or on high state (1), jumperfield B13 is provided on the board. The possible jumper settings given in Table 12 determine the active level of the two power fail input pins at Connector P2 Pins A1 and A27.

If there is no Power Fail signal attached to the board, the jumper settings on B13 has to be either the default one, or the jumper has to be removed. A removed jumper will hinder the board from reacting on the external Power Fail signal.

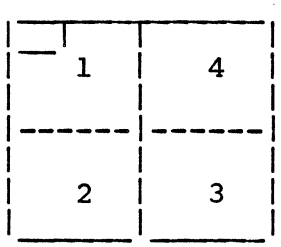
The location of B13 is shown in Figure 12.

Table 12: The Power Fail Signal Level

Power Fail Signal	Jumperfield B13 Connected Pins
Active low	1 - 2 *
Active high	2 - 3
Disabled function	Jumper removed

* default jumper setting.

Pin-Out of Jumperfield B13:



When the ASCU-1/2 board receives the ACFAIL* line asserted, it will latch the signal and execute the following functions:

- turning on the red ACFAIL LED on the front panel
- requesting an interrupt to the VMEbus (if programmed)
- triggering a time-out counter which drives the SYSRESET* line low after a selectable delay.

The latched ACFAIL* signal is readable via the PB5 Port terminal of the Parallel Interface Timer Module 1/Port B (PI/T 1, location J37). The latch can be cleared if the PB6 terminal of the PI/T 1 device is programmed as a low status output, providing that the ACFAIL* signal line is not still asserted.

This feature allows the system software to distinguish between occurring short AC-power drop-outs and longer power failure periods, which require an appropriate data saving reaction.

After the power-up sequence, both terminals PB6 and PB7 of the PI/T 1 are programmed as inputs and carry high level.

If the latched ACFAIL* signal is cleared, the ACFAIL LED on the front panel will also turn off.

A second external LED for an ACFAIL display is connectable on the P2 connector Pin C26 and C25. Pin C26 provides the signal level and C25 the LED supply voltage. The circuitry includes a pre-register which supplies a source current of 50mA.

The Interrupt Request caused by the latched ACFAIL* signal is handled by the BIM 1 device and has to be enabled by programming the appropriate Control and Vector register of the BIM (please refer to chapter 4.1 and the Data Sheet of the Bus Interrupter Module).

Table 13 outlines the offset of the corresponding BIM Register to the Board Base Address.

Table 13: ACFAIL* Interrupt Channel Address Assignment

Interrupt Source	Interrupt Channel Number	Interrupt Device	Offset to Board Base Address	
			Control Reg.	Vector Reg.
ACFAIL*	3	BIM 1	$105	$10D

If the ASCU-1/2 detects the ACFAIL* line to be asserted, it will drive the SYSRESET* signal line low after a defined time.

This feature is enabled with an inserted jumper at B1Ø.

The delay between the ACFAIL* and the SYSRESET* transition is jumper selectable in the range of 2ms to 16ms. The selection is made by an inserted jumper in jumperfield B15.

Figure 12 shows the location of the jumperfield B1Ø and B15.

Table 14: Delay of SYSRESET*/Generation after ACFAIL* Detection

Delays	Jumperfield B15 corresponding Pins
2ms	1 - 8
4ms	2 - 7
8ms	3 - 6 *
16ms	4 - 5

* default jumper setting

Pin-Out of Jumperfield B15:

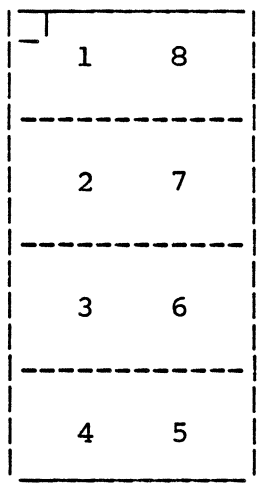
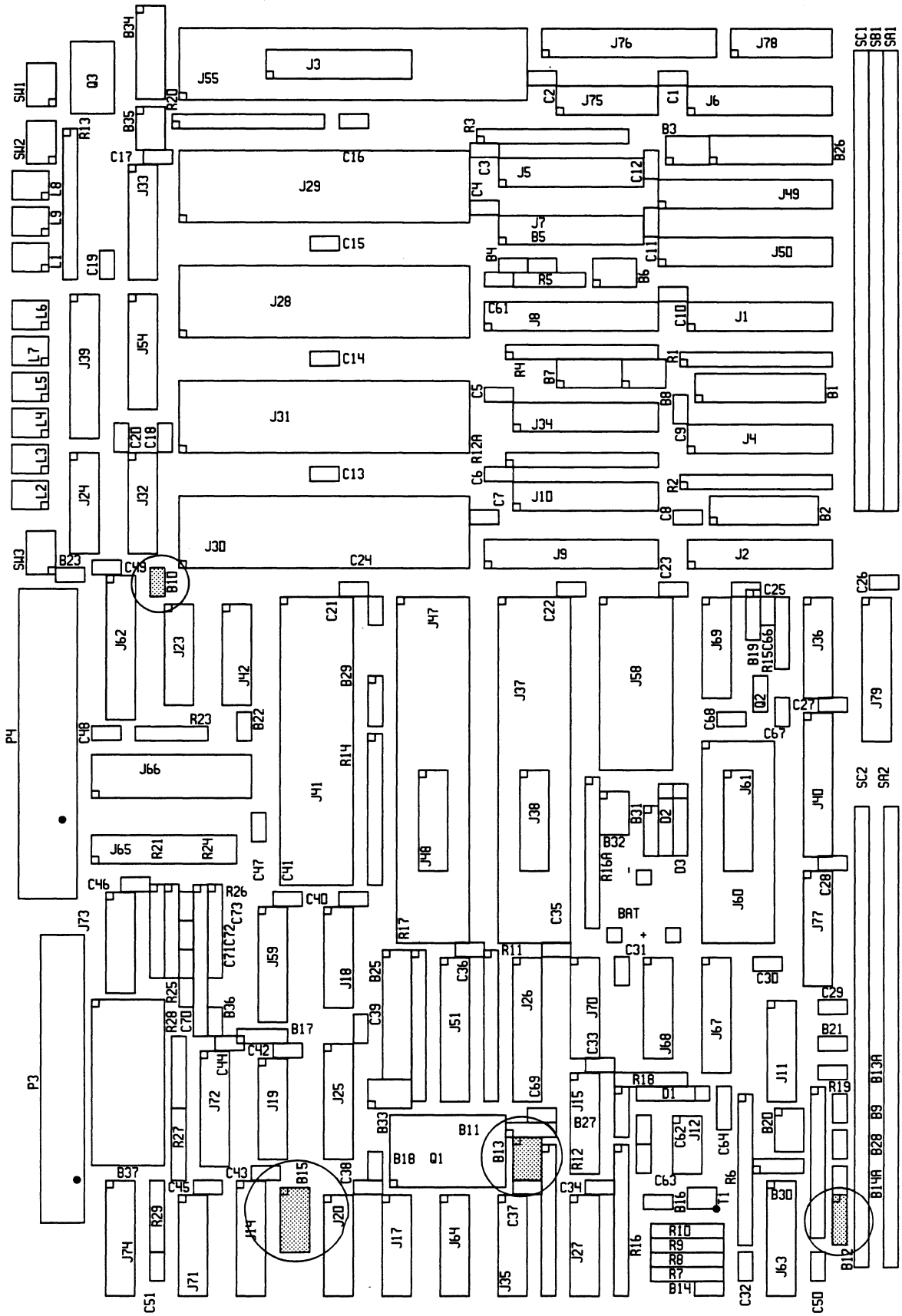


Figure 12: Jumper Location of the ACFAIL* Signal Handling

B1Ø, B12, B13, and B15



6. Functional Groups on the SYS68K/ASCU-1/2

The SYS68K/ASCU-1/2 can be considered to consist of the following functional groups:

- Software Control of Board Features
- Power Monitor Module
- SYSCLOCK DRIVER
- Bus Arbiter
- Bus Timer
- Serial Interface
- Centronics Interface
- Real Timer Clock
- Test Interrupt
- User Interrupt 1
- Timer Interrupt
- IEEE-488 GPIB Interface (only on ASCU-2)
- User Interrupts 2-5 (only on ASCU-2)
- Programmable Interrupts (only on ASCU-2)
- Bus Clear Timer (only on ASCU-2)

Some of the functional groups consist of one device while others are distributed to several devices e.g. the IEEE-Interface.

Table 15 shows this distribution of the Functional Groups realized in conjunction with the devices on the board.

The SOFTWARE CONTROL of BOARD FEATURES is provided by two Parallel Interface/Timer Modules (6823Ø) PI/T 1 and PI/T 2. The port terminals are used to control and steer functional groups on the board.

The POWER MONITOR MODULE handles the SYSRESET*, ACFAIL* and SYSFAIL* utility bus lines. It is assigned two interrupt channels of the BIM device (Channel 4 and Channel 3). Channel 4 is driven by the SYSFAIL* line, Channel 3 is assigned to the ACFAIL* function. Two port terminals of the PI/T 1 device have control of the latched ACFAIL* signal, which can be read as well as cleared. The programmable SYSRESET* generation is performed by another port terminal.

The SYSCLOCK DRIVER MODULE provides a 16MHz frequency which can be used as a known system time base. It can be considered as an autonomous module as well as the BUS ARBITER, which provides an efficient allocation method of the Data Transfer Bus to several bus masters.

The BUS TIMER functional group is controlled by the PI/T 1 device. Five signal lines of Port B (PBØ-4) select the desired bus time-out.

The same Parallel Interface/Timer Module PI/T 1 provides the standard CENTRONICS INTERFACE for printer connection. Interrupt generation is supported by the H1 handshake input, which is connected to the Data Acknowledge signal line of the Centronics Interface. The assigned Interrupt Channel is Channel 1.

The REAL TIME CLOCK can force an interrupt to the VMEbus via the Interrupt Channel 6.

The TEST INTERRUPT function can be enabled by the initialization of Interrupt Channel 5.

The USER INTERRUPT 1 line is connected to the H3 input of the PI/T 1 device and uses the same interrupt channel (Channel 1) as the Centronics Interface and the USER INTERRUPTS 2-5. A distinction between the Centronics Interface interrupt request and the Peripheral User Interrupt 1 request can be made by using the vector generating mode of the Port Interrupt. The source of the Peripheral User Interrupt 2-5 has to be identified by a polling software routine.

The TIMER INTERRUPT function is a part of the PI/T 1 device and generates the interrupt request over Channel 2.

The IEEE-488 GPIB INTERFACE is supported by the 2nd PI/T device. The talker/listener address is jumper selectable and can be read via Port B pins PBØ to PB4 of PI/T 2. If the signal pin of PC7 is programmed as an input, the status of T/L switch 3 is readable.

Port A of the PI/T 2 device provides eight independent software **PROGRAMMABLE INTERRUPTS.** Each of these interrupt sources is assigned a unique interrupt channel.

The **BUS CLEAR TIMER** function consists of the timer module on the PI/T 2 device. The input pin PC2 triggers the counter to generate the Bus Clear signal on PC3 after a software programmable time.

Table 15 gives detailed information on how each of the functional groups is distributed over PI/T 1, PI/T 2, the 16 Interrupt Channels and individual parts.

Table 15: Functional Groups Distribution

FUNCTIONAL GROUPS	DEVICES					
	PI/T 1 (J37)		PI/T 2 (J47)		Bus Interrupter Module Channel No.	Other Device
	PIN	I/O	PIN	I/O		
SOFTWARE CONTROL						
Programmable Interrupt			PAØ	O	CH 9	
Programmable Interrupt			PA1	O	CH1Ø	
Programmable Interrupt			PA2	O	CH11	
Programmable Interrupt			PA3	O	CH12	
Programmable Interrupt			PA4	O	CH13	
Programmable Interrupt			PA5	O	CH14	
Programmable Interrupt			PA6	O	CH15	
Programmable Interrupt			PA7	O	CH16	
GPIB Address Bit D1			PBØ	I		
GPIB Address Bit D2			PB1	I		
GPIB Address Bit D3			PB2	I		
GPIB Address Bit D4			PB3	I		
GPIB Address Bit D5			PB4	I		
BCLR* Timer			PCØ	O		
BCLR* Timer			PC1	O		
BCLR* Timer			PC2	I		
BCLR* Timer			PC3	O		
BCLR* Timer			PC4	O		
GPIB Direction Control			PC6	O		
Status T/L Switch			PC7	I		
Bus Timer Out Data Cycle	PBØ	O				
Bus Timer Out Data Cycle	PB1	O				
Bus Timer Out Data Cycle	PB2	O				
Bus Timer Out IACK Cycle	PB3	O				
Bus Timer enable/disable	PB4	O				
ACFAIL* latched	PB5	I				
ACFAIL* IRQ cleared	PB6	O				
RESET programmable	PB7	O				
POWER MONITOR MODULE						
ACFAIL* latched	PB5	I				
ACFAIL* IRQ cleared	PB6	O				
RESET programmable	PB7	O				
ACFAIL* Interrupt Req.					CH 3	
SYSFAIL* Interrupt Req.					CH 4	
SYSCLOCK DRIVER						Individual Parts
ARBITER						Individual Parts

Table 15 cont'd

FUNCTIONAL GROUPS	DEVICES					
	PI/T 1 (J37)		PI/T 2 (J47)		Bus Interrupter Module Channel No.	Other Device
	PIN	I/O	PIN	I/O		
BUS TIMER						Individual Parts
Bus Time-Out Data Cycle	PBØ	O				
Bus Time-Out Data Cycle	PB1	O				
Bus Time-Out Data Cycle	PB2	O				
Bus Time-Out IACK Cycle	PB3	O				
BUS Time enabled/disabld	PB4	O				
SERIAL INTERFACE						
Interrupt Request					CH 7	MPCC (J55)
CENTRONICS INTERFACE						
Interrupt Request	PC5				CH 1	
Data 1	PAØ	O				
Data 2	PA1	O				
Data 3	PA2	O				
Data 4	PA3	O				
Data 5	PA4	O				
Data 6	PA5	O				
Data 7	PA6	O				
Data 8	PA7	O				
ACKNLG	H1	I				
DATA STROBE	H2	O				
BUSY	PCØ	I				
PE	PC1	I				
SLCT	PC2	I				
ERROR	PC4	I				
REAL TIME CLOCK						
Interrupt Request					CH 6	RTC 58167A (J58)
TEST INTERRUPT						Individual Parts
Interrupt Request					CH 5	
USER INTERRUPT 1						
Interrupt Request	PC5				CH 1	
USER Interrupt 1	H3					
TIMER INTERRUPT						
Interrupt Request	PC3				CH 2	

Table 15 cont'd

FUNCTIONAL GROUPS	DEVICES					
	PI/T 1 (J37)		PI/T 2 (J47)		Bus Interrupter Module Channel No.	Other Device
	PIN	I/O	PIN	I/O		
IEEE-488 GPIB INTERFACE (only on ASCU-2)						7210
Interrupt Request					CH 8	(J41)
GPIB Address Bit D1			PB0	I		
GPIB Address Bit D2			PB1	I		
GPIB Address Bit D3			PB2	I		
GPIB Address Bit D4			PB3	I		
GPIB Address Bit D5			PB4	I		
GPIB Direction Control			PC6	O		
Status T/L Switch			PC7	I		
USER INTERRUPT 2-5 (only on ASCU-2)						
Interrupt Request	PC5	O	PC5	O	CH 1	
User Interrupt 2			H1	I		
User Interrupt 3			H2	I		
User Interrupt 4			H3	I		
User Interrupt 5			H4	I		
PROGRAMMABLE INTERRUPTS (only on ASCU-2)						
			PA0	O	CH 9	
			PA1	O	CH10	
			PA2	O	CH11	
			PA3	O	CH12	
			PA4	O	CH13	
			PA5	O	CH14	
			PA6	O	CH15	
			PA7	O	CH16	
BUS CLEAR TIMER						
BCLR* Mode Select			PC0	O		
BCLR* Mode Select			PC1	O		
BCLR* Mode Select			PC4	O		
Trigger input			PC2	I		
BCLR* signal			PC3	O		

7. Software Control

Powerful software control of the functional groups on the ASCU-1/2 is provided by the two Parallel Interface/Timer Modules (68230) PI/T 1 and PI/T 2.

The software control function is performed by programming I/O pins of the PI/T devices to be output and to drive them to a logical 1 or Ø. The reset situation is that all I/O pins of the pit devices are in the high independence state (Input Mode), and internal or external pull-up registers grant a logical 1 (high level).

The PI/T device consists of two logically independent parts: the parallel ports and the timer.

The timers of the PI/T 1 and PI/T 2 represent the functional groups "TIMER INTERRUPT" and BUS CLEAR TIMER". A description of these groups follows in the corresponding chapters. The program example which initializes the software control in this chapter will also activate the timers.

7.1 Addressing of the PI/T devices

The two parallel interface/timer modules allow only byte transfers on the lower data bus (DØ-D7). The register access to the PI/T can only be performed at odd addresses.

The devices have the following offset related to the Board Base Address:

PI/T 1 : $Ø4Ø

PI/T 2 : $Ø8Ø

Provided that the Board Base Address is $BØ2ØØØ (default condition during manufacturing), the first register of the PI/T 1 device has the absolute access address $BØ2Ø41 and PI/T 2 $BØ2Ø81 (Port General Control Register).

All registers are readable and writeable and can be accessed directly. The PI/T device features a flexible port mode structure which is selectable by writing to the control registers of the PI/T.

The Bit I/O Mode allows all port terminals to be programmed and controlled independently. The software control function is performed by writing Ø or 1 to the corresponding bit locations of the PI/T data registers.

For further information, please refer to the programming example at the end of this chapter as well as the chapter entitled "Board Register Summary", and the data sheet.
Table 16 gives all the I/O pins involved in the software control function. A detailed description of the control can be found in the chapters for the appropriate functional groups.

Table 16: Software Controlled I/O Pins

Device	Port I/O Pin	In/Out Function	Affected Functional Group / Signal
PI/T 1	PB Ø	OUT	BUS TIMER / Time Out for Data Cycle
	PB 1	OUT	BUS TIMER / Time Out for Data Cycle
	PB 2	OUT	BUS TIMER / Time Out for Data Cycle
	PB 3	OUT	BUS TIMER / Time Out for IACK Cycle
	PB 4	OUT	BUS TIMER / enabled - disabled
	PB 5	IN	POWER MONITOR MODULE/ACFAIL* SIGNAL
	PB 6	OUT	POWER MONITOR MODULE/ACFAIL* SIGNAL
	PB 7	OUT	POWER MONITOR MODULE/SYSRESET* SIGNAL
PI/T 2	PA Ø	OUT	PROGRAMMABLE INTERRUPT / CHANNEL 9
	PA 1	OUT	PROGRAMMABLE INTERRUPT / CHANNEL 1Ø
	PA 2	OUT	PROGRAMMABLE INTERRUPT / CHANNEL 11
	PA 3	OUT	PROGRAMMABLE INTERRUPT / CHANNEL 12
	PA 4	OUT	PROGRAMMABLE INTERRUPT / CHANNEL 13
	PA 5	OUT	PROGRAMMABLE INTERRUPT / CHANNEL 14
	PA 6	OUT	PROGRAMMABLE INTERRUPT / CHANNEL 15
	PA 7	OUT	PROGRAMMABLE INTERRUPT / CHANNEL 16
	PC Ø	OUT	BUS CLEAR Mode Select / MODE 1
	PC 1	OUT	BUS CLEAR Mode Select / MODE 2
	PC 4	OUT	BUS CLEAR Mode Select / MODE 3
	PC 2	IN	BUS CLEAR TIMER /Trigger Input Signal
	PC 3	OUT	BUS CLEAR TIMER /BCLR* Signal Genera.
	PB Ø	IN	IEEE-488 GPIB I.F./Address Bit D1
	PB 1	IN	IEEE-488 GPIB I.F./Address Bit D2
	PB 2	IN	IEEE-488 GPIB I.F./Address Bit D3
	PB 3	IN	IEEE-488 GPIB I.F./Address Bit D4
	PB 4	IN	IEEE-488 GPIB I.F./Address Bit D5
	PC 6	OUT	IEEE-488 GPIB I.F./Direction Control
	PC 7	IN	IEEE-488 GPIB I.F./Status T/L Switch

Programming Example

```
*************************************************************************
*
*       PROGRAMMING EXAMPLE
*
*************************************************************************
*
*       The example contains the following subroutines:
*       - INITASCU2     Initializes Functional Modules:
*                       BUS TIMER       32 us for DATA and IACK cycles
*
*                       BCLR*Generation mode: Arbiter or Timer output
*                       BCLR*Timer      functions as watchdog counter
*
*       - TIMERIRQ      periodical Interrupt Generation through Timer
*                       Interrupt
*
*       - PIRQINIT      Initializes PI/T 2 to Bit I/O-mode for
*                       Programmable Interrupt Generation
*
*       - PROGIRQ       Programmable Interrupt subroutine
*-----------------------------------------------------------------------


ASCUBASE:       EQU     $B02000         ;BASE ADDRESS OF ASCU-2
*
*
*PI/T Register offsets:
*
*Parallel I/O section
PGCR:   EQU     $01
PSRR:   EQU     $03
PADDR:  EQU     $05
PBDDR:  EQU     $07
PCDDR:  EQU     $09
PIVR:   EQU     $0B
PACR:   EQU     $0D
PBCR:   EQU     $0F
PADR:   EQU     $11
PBDR:   EQU     $13
PAAR:   EQU     $15
PBAR:   EQU     $17
PCDR:   EQU     $19
PSR:    EQU     $1B
*Timer section
TCR:    EQU     $21
TIVR:   EQU     $23
CPR:    EQU     $25
CNTR:   EQU     $2D
TSR:    EQU     $35
*
*
*Offsets for BIM register address calculation
*
BIMCONTR:       DC.W    $121
                DC.W    $123
                DC.W    $125
                DC.W    $127
                DC.W    $131
                DC.W    $133
                DC.W    $135
                DC.W    $137
*
VECTOR:         EQU     $40                     ;Timer Interrupt Vector
                EVEN
```

Programming Example cont'd.

```
*-------------------------------------------------------------------------
*
*               Initialisation Routine
*               ======================
*
INITASCU2:      MOVEM.L A0-A3/D0,-(A7)          ;push registers to save
                LEA.L   ASCUBASE,A0             ;Board Base Address->A0
                LEA.L   $40(A0),A1              ;Device Base Address PI/T 1
                LEA.L   $80(A0),A2              ;Device Base Address PI/T 2
                BCLR.B  #7,PGCR(A1)             ;Bit 7 of PGCR cleared
                BCLR.B  #6,PGCR(A1)             ;Bit 6 of PGCR cleared
                BSET.B  #7,PACR(A1)             ;Set PI/T 1 to the Bit I/O -
                BSET.B  #6,PBCR(A1)             ;mode
*
                MOVE.B  #$EE,PBDR(A1)           ;BUS TIMER set to 32 us DATA-
                MOVE.B  #$DF,PBDDR(A1)          ;and IACK-cycle
*
                MOVE.L  #$1000,D0               ;WATCHDOG counter
                MOVEP.L D0,CPR(A2)              ;for
                MOVE.B  #$F3,TCR(A2)            ;BCLR* Timer
*
                MOVE.B  #$FD,PCDR(A2)           ;BCLR-Mode
                MOVE.B  #$5B,PCDDR(A2)          ;selection
*
                MOVEM.L (A7)+,A0-A3/D0          ;pop saved registers
*
                BSR.S   PIRQINIT                ;Subroutine to initialize
*                                               ;PI/T 2 for programmable
*                                               ;IRQ-generation
                RTS

*-------------------------------------------------------------------------
*
PIRQINIT:       MOVEM.L A0-A2,-(A7)             ;push registers to save
                LEA.L   ASCUBASE,A0             ;ASCU-2 Board Base Address->A0
                LEA.L   $80(A0),A2              ;PI/T 2 Device address ->A2
                BCLR.B  #7,PGCR(A2)             ;Set PI/T 2 to
                BCLR.B  #6,PGCR(A2)             ;Bit I/O mode
                BSET.B  #7,PACR(A2)             ;
                MOVE.B  #00,PADR(A2)            ;Port A pins -> output
                MOVE.B  #$FF,PADDR(A2)          ;Port A pins -> low
                MOVEM.L (A7)+,A0-A2             ;pop saved registers
                RTS
```

Programming Example cont'd.

```
*-------------------------------------------------------------------------
*       Subroutine for periodical TIMER-INTERRUPTS and IRQ-CHANNEL-2
*       Initialisation: TIMERIRQ
*
*
TIMERIRQ:       PEA.L   SERVICE(PC)
                MOVE.L  (A7)+,VECTOR*4
*
                MOVEM.L A0-A1/D0-D1,-(A7)       ;PUSH REGISTERS TO SAVE
                LEA.L   ASCUBASE,A0             ;BOARD BASE ADDRESS -> A0
                LEA.L   ASCUBASE+$40,A1         ;PI/T1 DEVICE BASE ADDRESS ->A1
                MOVE.B  #VECTOR,D1              ;INTERRUPT VECTOR NUMBER -> D1
                MOVE.B  D1,TIVR(A1)             ;VECTOR -> TIMER INT.VECT.REG
                MOVE.L  #$600,D0                ;COUNT VALUE
                MOVEP.L D0,CPR(A1)              ;LOAD COUNT PRELOAD REGISTER
                MOVE.B  #$A1,TCR(A1)            ;PERIODIC INTERRUPT GENERATOR
                MOVE.B  #$1,TSR(A1)             ;
                MOVE.B  #$36,$103(A0)           ;BIM INIT: EXTERNAL VECTOR
*                                               ;IRQ-LEVEL 6
                MOVEM.L (A7)+,A0-A1/D0-D1       ;POP SAVED REGISTERS
                RTS


*               TIMER INTERRUPT SERVICE ROUTINE: SERVICE
*               ========================================
*
SERVICE:        MOVEM.L A1/D0,-(A7)             ;SAVE REGISTERS
                LEA.L   ASCUBASE+$40,A1         ;PI/T1 DEVICE BASE ADDRESS ->A1
                MOVE.B  #$A1,TCR(A1)
                MOVE.B  #$01,TSR(A1)            ;CLEAR ZDS STATUS BIT
*
                MOVEM.L (A7)+,A1/D0
                RTE



*-------------------------------------------------------------------------
*       SUBROUTINE: PROGIRQ
*       This subroutine initiates an Interrupt Request to the VMEbus by
*       searching a free IRQ channel (channel 9 - 16).
*       The interrupt vector must be stored in D0 (00-FF), the desired
*       interrupt level must be stored in D1 (1-7).
*       Before this Subroutine can be called, the SYS68K/ASCU-2 has to be
*       initialized by the INITASCU2 subroutine.
*
*
PROGIRQ:        MOVEM.L D2-D3/A0-A5,-(A7)       ;push registers to save
                LEA.L   ASCUBASE,A0             ;Board Base Address ->A0
LOOP:           LEA.L   BIMCONTR(PC),A4         ;BIM IRQ channel table
                LEA.L   $10(A4),A5              ;End of IRQ channel table
NEXT:           MOVE.W  (A4)+,D3                ;Read Offset
                BSET.B  #7,0(A0,D3)             ;Test and Set BIM channel
                BEQ.S   IRQCHAN                 ;Free channel found
                CMPA.L  A4,A5                   ;compare if last channel
                BNE.S   NEXT                    ;next channel
                BRA.S   LOOP                    ;unfinite loop to wait for
*                                               ;free channel
IRQCHAN:        MOVE.B  D0,8(A0,D3)             ;write vector
                MOVE.B  #$D8,D2                 ;control byte construction
                OR.B    D1,D2                   ;
                MOVE.B  D2,0(A0,D3)             ;write control byte
                MOVEM.L (A7)+,D2-D3/A0-A5       ;pop saved registers
                RTS
```

8. Power Monitor Module

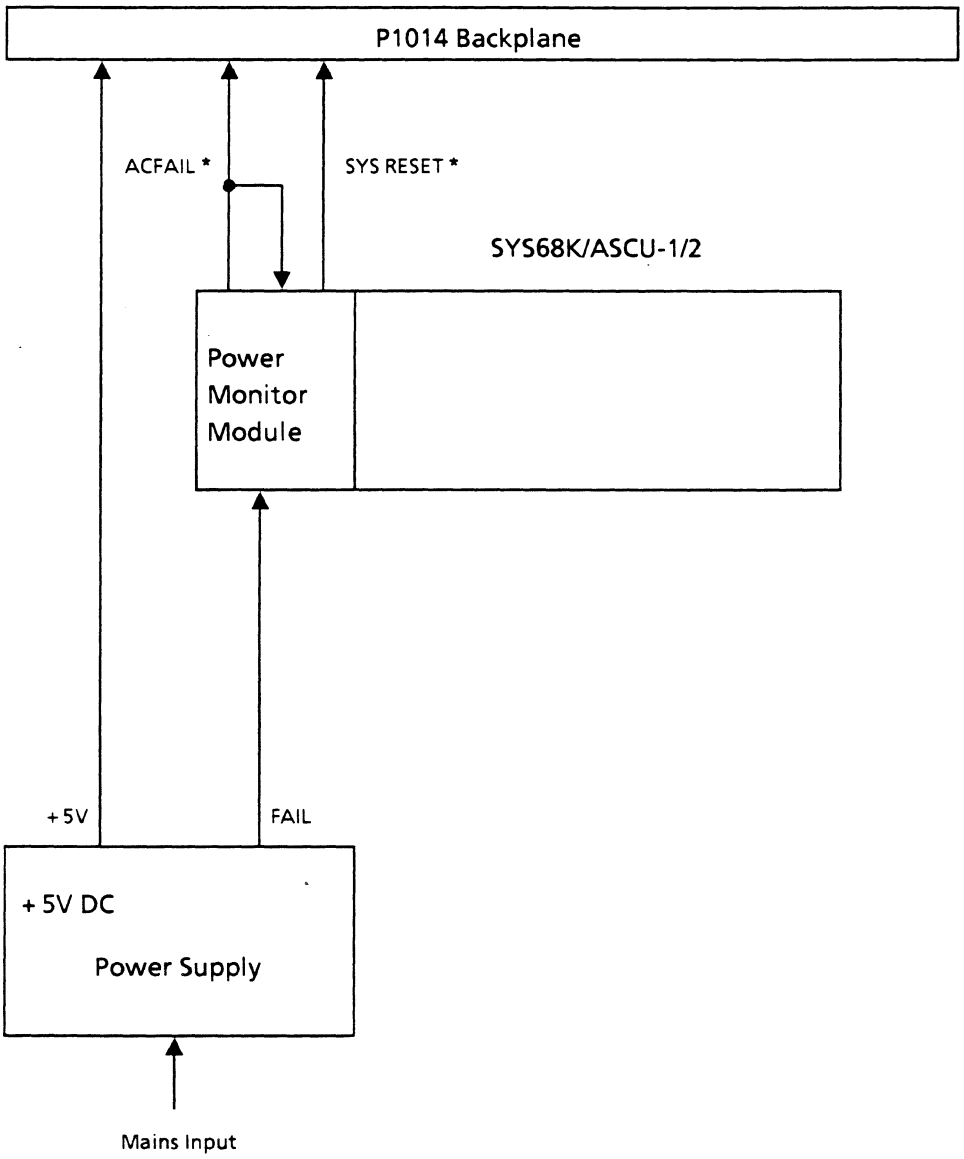
The SYS68K/ASCU-1/2 board is equipped with a Power Monitor Module which executes an orderly shut-down of a system after an AC power failure has been indicated by an asserted ACFAIL* bus line.

The indication of a power failure may be provided by the system power supply whose Power Fail signal line can be attached to the P2 connector of the ASCU-1/2.

Figure 13 shows this arrangement in a system block diagram.

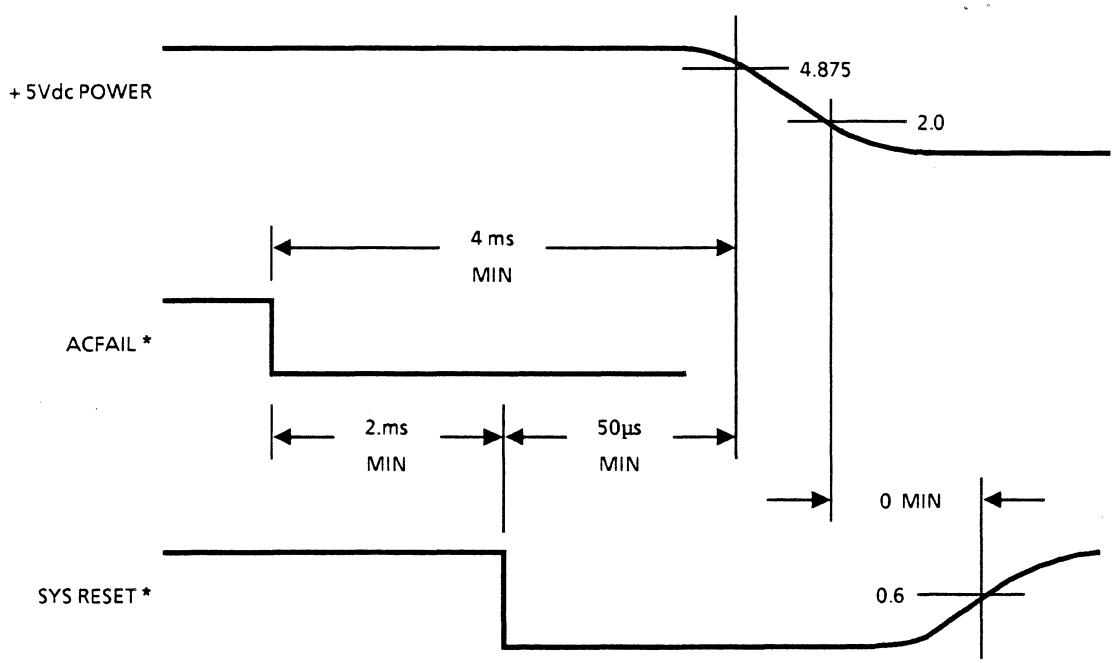
The connection of the Power Fail signal of an external source and the P2 connector is described in section 5.3 "The ACFAIL* Signal".

Figure 13: System Block Diagram



The Power Monitor Module guarantees a VME/PlØ14 compatible active low SYSRESET* signal according to the timing relationship given in Figure 14.

Figure 14: Power Fail Timing Diagram



The delay of the ACFAIL* signal transition to the active SYSRESET* signal is selectable in the range between 2ms and 16ms. Please refer to chapter 5.3, "The ACFAIL* Signal".

8.1 The Reset Generator

The SYSRESET* signal is carried out by an on-board reset generator circuitry which operates above 3V supply voltage. The SYSRESET line is driven by the board if the jumper B16 is inserted (default condition = jumper B16 inserted).

Figure 15 shows a block diagram of the reset structure.

The reset generator will assert its output signal by any of the following conditions:

a) detection of an ACFAIL* signal transition to low state,
b) closing one of the reset keys,
c) generating a programmable reset,
d) sensing the system supply voltage out of specified range.

N.B. points a) - c) are described in chapter 5 "Utility Signal Handling".

The reset source of condition d) is provided by the reset generator itself, containing a precision voltage sensor.

During the power-up procedure the circuit checks the supply voltage and asserts its output as long as VCC has not reached the value of the sense voltage.

After VCC has exceeded the threshold voltage, an internal timer assures that the SYSRESET* line will remain asserted for at least 200 milliseconds. That delay is also provided for all other reset conditions after they have been removed.

Figure 16 shows the corresponding timing.

Also, when the supply voltage drops under the sense voltage, the reset generator output becomes active and the SYSRESET* signal line will be pulled down to low state.

Figure 15: Block Diagram of the RESET Structure

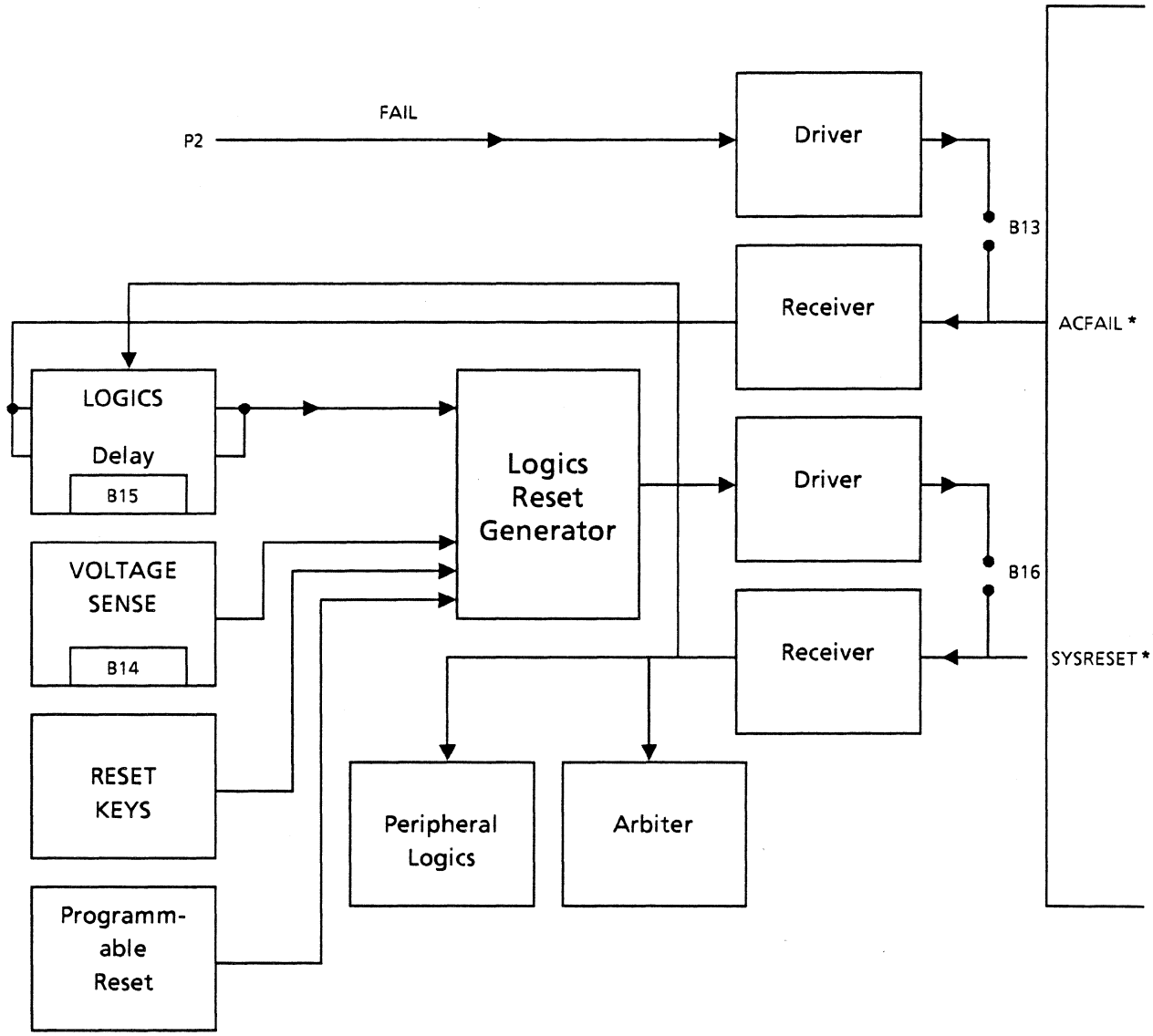
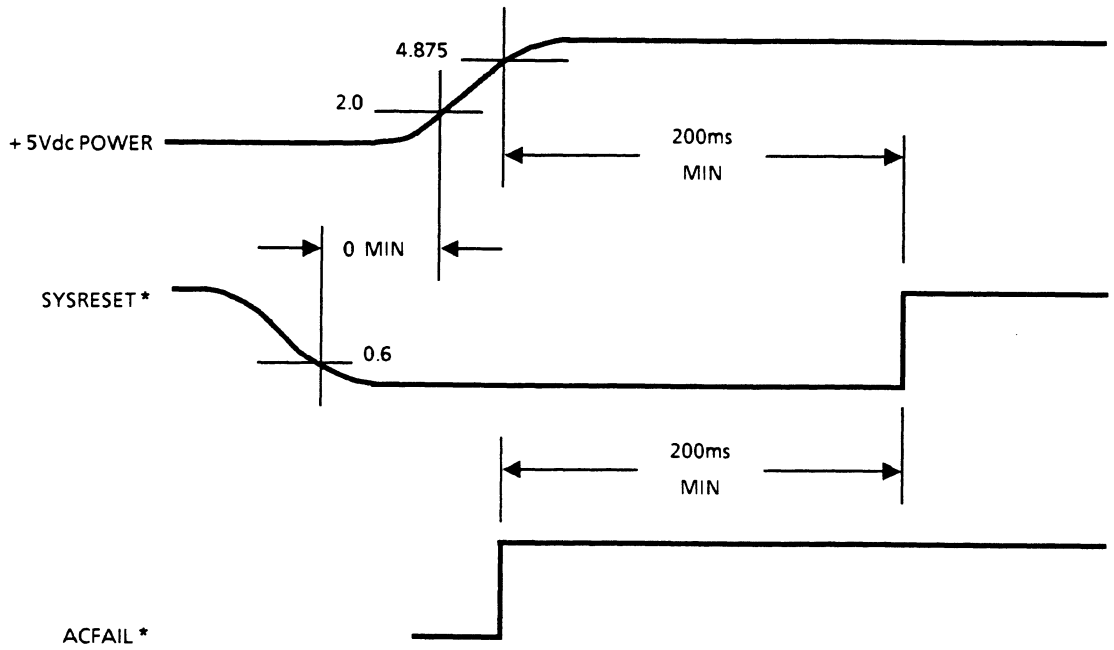


Figure 16: Power Monitor System Restart Timing

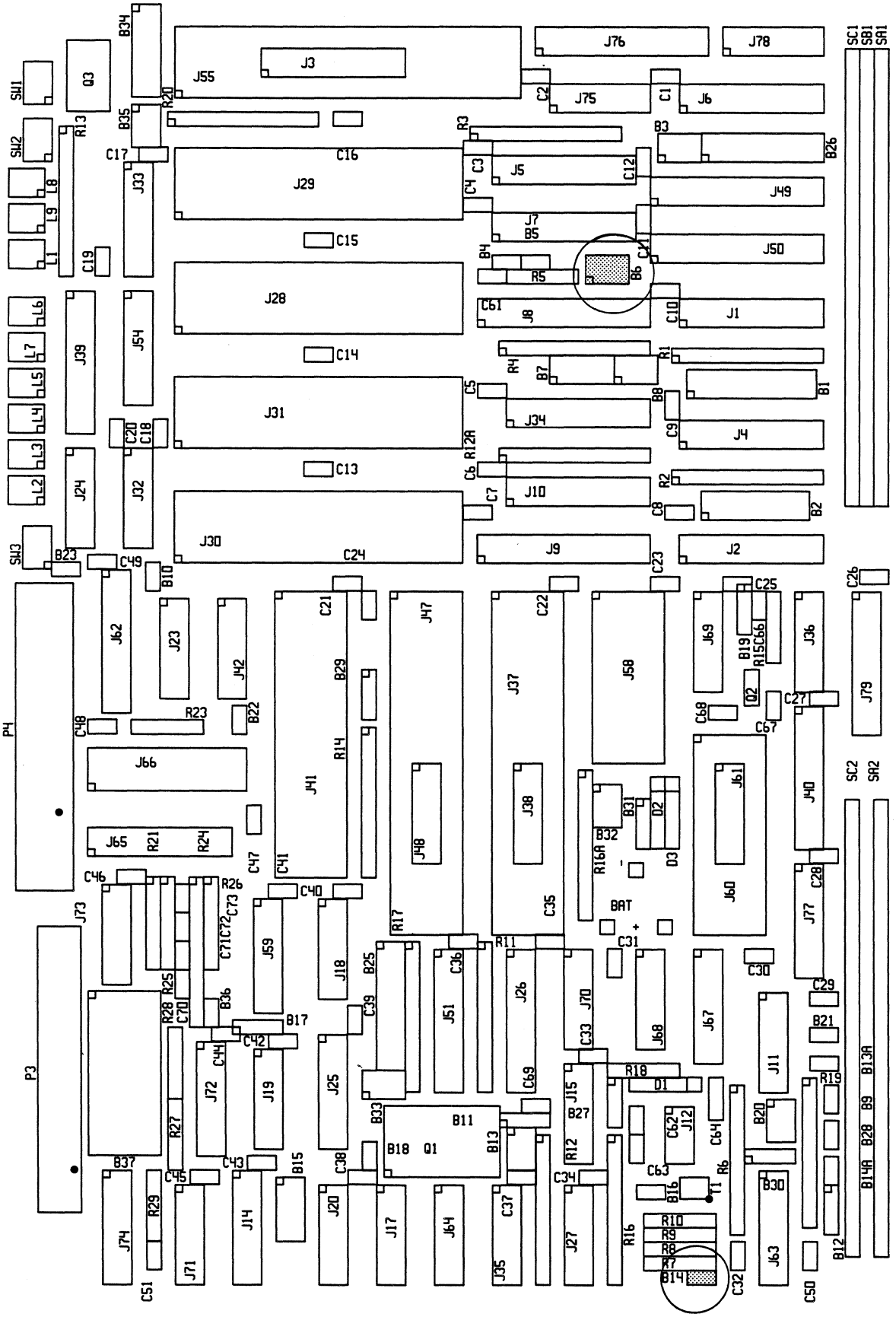


The sense voltage is jumper selectable for two values.

If jumper B14 is removed (default condition), the sense voltage is fixed at 4.8V. Inserting the jumper selects a sense voltage of 4.5V, which should ensue for test purposes only.

The location diagram of jumper B14 is shown in Figure 17.

Figure 17: Location Diagram of the Jumperfields B14 and B6



9. The SYSCLOCK Driver

The SYS68K/ASCU-1/2 is equipped with a SYSCLOCK DRIVER Module that provides a fully asynchronous 16MHz timing signal on the utility bus according to the VMEbus/P1Ø14 specification. The signal has no fixed phase relationship to/with other timings.

The SYSCLOCK signal is a divided clock-frequency which is generated by a quarz oscillator module.

The signal is connected to the backplane via jumperfield B6. If there is a jumper installed connecting pins 1 and 4, the signal is driven to the bus. (Default condition during manufacturing.) Removing this jumper disables the driving of this signal.

Fig. 17 outlines the position of the jumperfield B6.

Caution: According to the VMEbus/P1Ø14 specification, if the SYS68K/ASCU-1/2 sources the SYSCLOCK signal, the board has to be installed in slot 1 of the backplane.

Pin-Out of the Jumperfield B6:

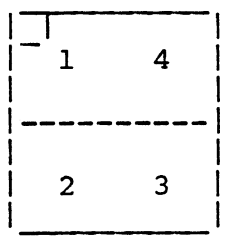
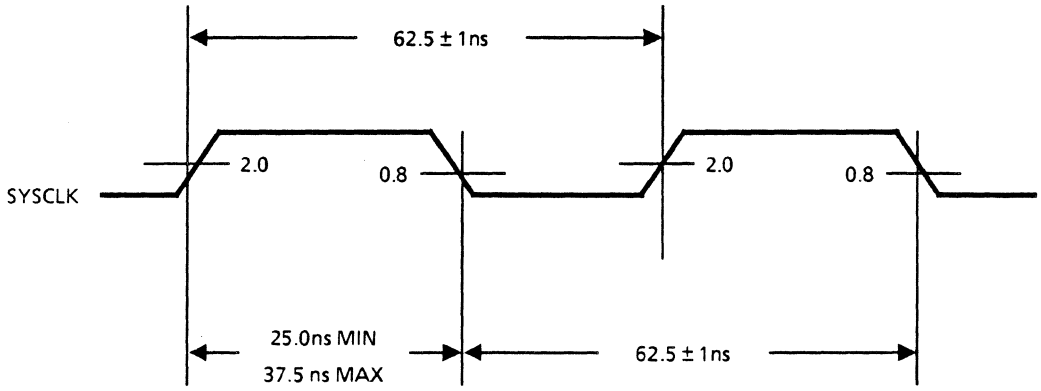


Figure 18: The SYSCLK Timing Diagram



1Ø. The 4-Level Bus Arbiter

The SYS68K/ASCU-1/2 is equipped with a functional module for Data Transfer Bus Arbitration according to the VMEbus/IEEE-P1Ø14 specification.

The VMEbus is defined to support multiple bus masters that can initiate data transfer cycles. Only one board can be Bus Master at any one time. No other board can become Bus Master before the current Bus Master has relinquished Bus Mastership.

The VMEbus specification defines a four-level Bus Request - Bus Grant - Bus Busy handshake mechanism, with an arbitration module to be located in slot 1 of the VMEbus backplane. The number of possible bus masters is not limited to the four levels, because the VMEbus backplane supports a daisy chain for the four Bus Grant signals.

The four level Bus Arbiter installed on the SYS68K/ASCU-1/2 supports three jumper selectable types of arbitration:

The Prioritization	PRI
Round Robin	RRS
Prioritized Round Robin	PRR

The selection of the arbitration types is done by different jumper settings at jumperfield B33, according to table 17.

Pin-out of Jumperfield B33

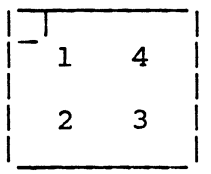


Table 17: Selection of the Arbitration Type

Arbitration Type	Jumperfield B33 Connected Pins
PRI	1 - 4
RRS	2 - 3
PRR	1 - 2 *

* default condition

If the SYS68K/ASCU-1/2 is inserted in slot 1 of the VMEbus backplane, then the Bus Arbiter must be operational. This is the default jumper configuration on delivery. If the SYS68K/ASCU-1/2 is inserted in any other slot, then the Bus Arbiter must not drive the Bus Grant signals, and the jumper configuration has to be changed.

Figure 19 shows the pin-out of Jumperfield B26, which determines the enabled or disabled Bus Arbiter function. The required jumper settings on B26 are given in Tables 18 and 19.

Figure 19:

Pin-out of Jumperfield B26

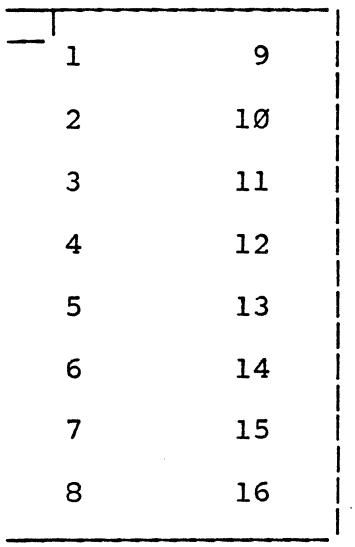


Table 18: Jumper Settings for Enabled Bus Arbiter Function

	Jumperfield B26 Connected Pins	Default Configuration
Enabled Bus Arbiter Function	2 - 1Ø	x
	4 - 12	x
	6 - 14	x
	8 - 16	x

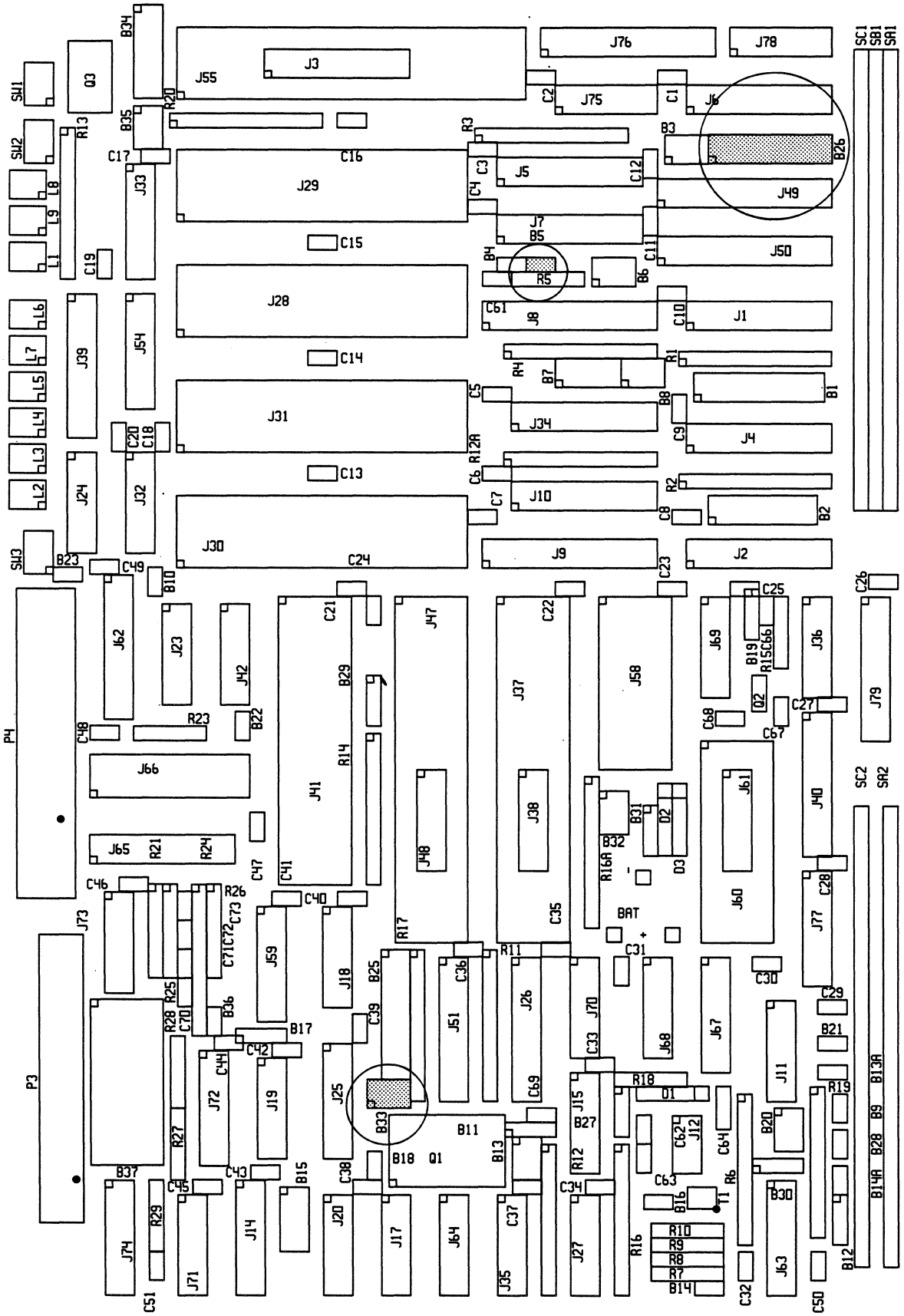
Table 19: Jumper Settings for Disabled Bus Arbiter Function

	Jumperfield B26 Connected Pins	Default Configuration
Disabled Bus Arbiter Function	9 - 1Ø 11 - 12 13 - 14 15 - 16	

Figure 2Ø shows the locations of the jumperfields assigned to the Arbiter function.

Note: Jumperfield B32 is not user selectable, but provided for test purposes only. No jumpers are inserted by default.

Figure 20: The Location Diagram of the Arbiter Jumperfields



The VMEbus includes the signal BCLR*.It is the arbiter that drives this signal and the current Bus Master can monitor it. Asserting the BCLR* signal means that the Bus Arbiter wishes the current Bus Master to relinquish Bus Mastership. However, despite this signal, the Bus Master will relinquish Bus Mastership only when it wishes to do so itself.

The BCLR* output of the SYS68K/ASCU-2 is equipped with software programmable timing for more flexibility. Please refer to chapter 19 "Bus Clear Timer". The BCLR* signal line is driven if jumper B5 is inserted. This is the default condition.

Caution: The B5 jumper must be removed if the board resides in any other slot of the rack than slot 1.

Table 2Ø describes the BCLR* generation of the SYS68K/ASCU-1. The BCLR* generation in the various arbitration modes on the SYS68K/ASCU-2 are described in chapter 19 "Bus Clear Timer".

Table 2Ø: BCLR* Generation on the SYS68K/ASCU-1

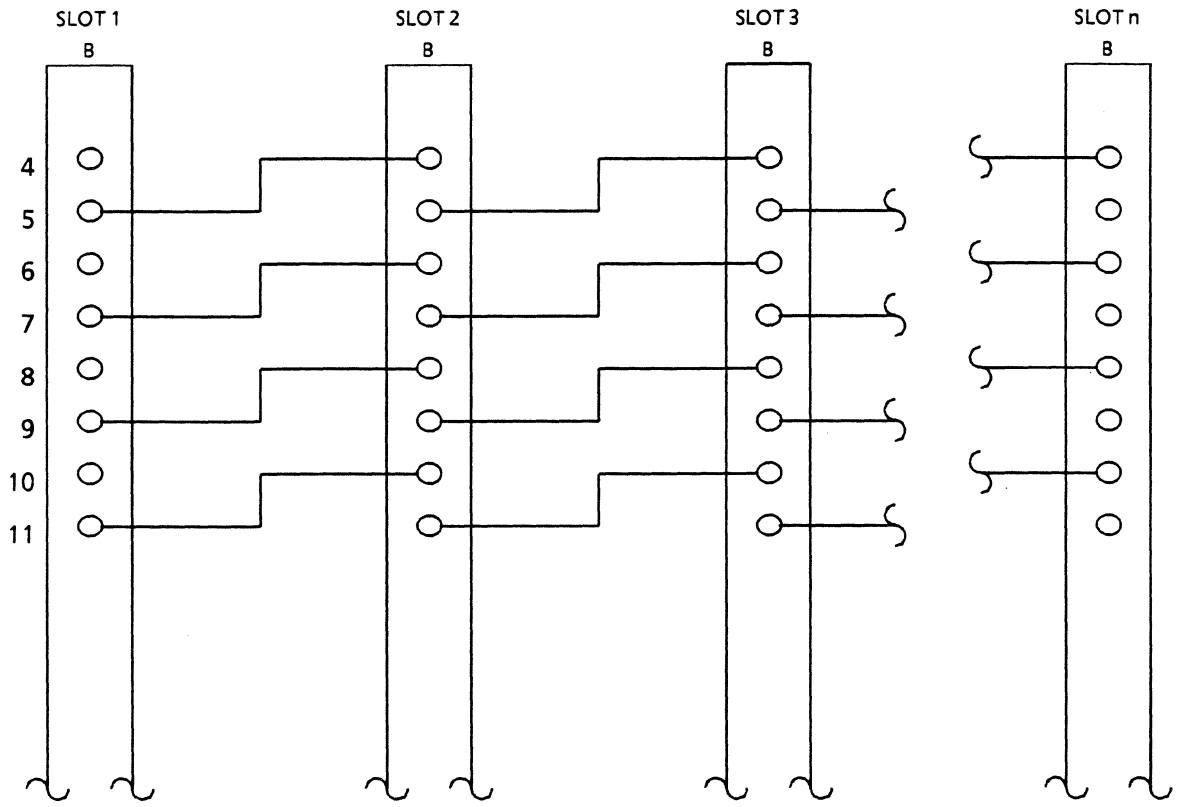
Arbitration Mode	D e s c r i p t i o n BCLR* is asserted if ...
PRI	a higher prioritized Bus Request is pending
PRR (default)	a level 3 Bus Request is pending
RRS	any Bus Request is pending

There are six LEDs installed on the front panel of the SYS68K/ASCU-1/2 for visual information about the bus load situation. They are described in more detail in chapter 3.5, "Bus Arbitration Status LEDs", as well as in the rest of this chapter.

Caution: No master can be removed from being master on the VMEbus. The master should release the bus by itself sometime. Even if all masters periodically release the bus, it can happen that some requesters never receive a grant. This is not a malfunction of the arbiter, but a logical consequence of the priority structure and of the daisy chain, if high bus load is accomplished.

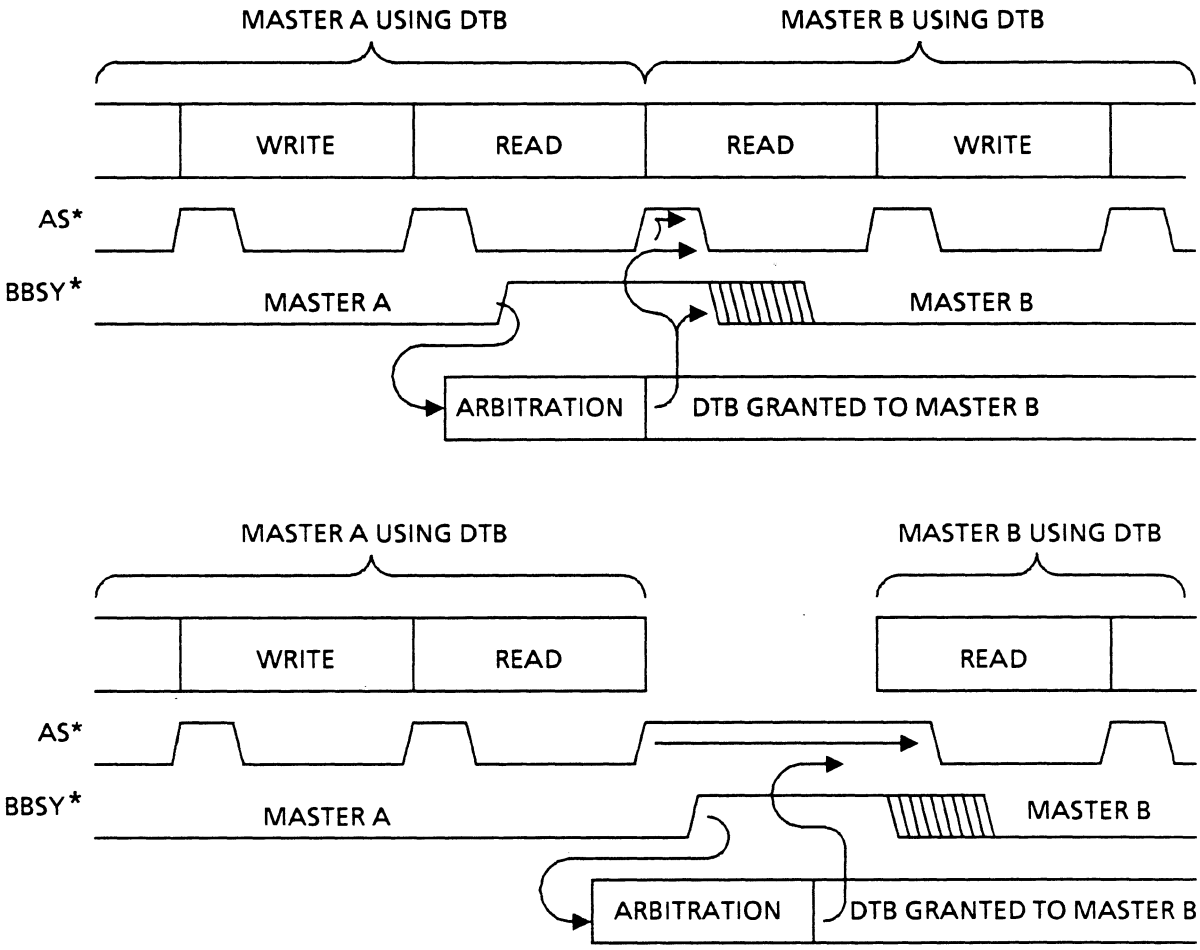
Figure 21 shows the Bus Grant Daisy Chain structure on the VMEbus backplane, and figure 22 outlines the global DTB arbitration timings.

Figure 21: The Bus Grant Daisy Chain



PIN 4 = BG 0 IN*
PIN 5 = BG 0 OUT*
PIN 6 = BG 1 IN *
PIN 7 = BG 1 OUT*
PIN 8 = BG 2 IN*
PIN 9 = BG 2 OUT*
PIN 10 = BG 3 IN*
PIN 11 = BG 3 OUT*

Figure 22: Global DTB Arbitration Timing



10.1 The PRI Arbiter

The VMEbus/IEEE-P1014 specifications define the prioritization algorithm of arbitration. The sequence of priority is as follows:

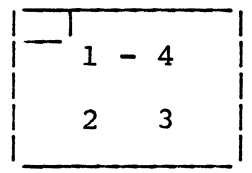
BR3* has priority over BR2*, BR1*, BR0*
BR2* has priority over BR1*, BR0*
BR1* has priority over BR0*.

Whenever the bus is not occupied by a master, or the bus is released by a master and there is a Bus Request pending, the arbiter will grant the bus to the master requesting on the bus request level with the highest priority.

If there is a Bus Request pending on a bus request level which has higher priority than the current Bus Master, then the arbiter asserts the BCLR* output to signal this situation to the current Bus Master.

To select the PRI Arbiter, the following jumper configuration has to be installed at jumperfield B33:

Jumperfield B33:



Connected pins: 1 - 4

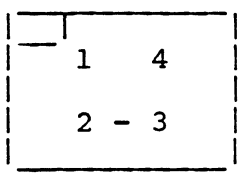
10.2 The RRS Arbiter

The VMEbus/IEEE-P1014 specifications define the Round Robin arbitration scheme. If this type of arbitration is selected, then all bus request levels appear to be of equal preference.

The BCLR* signal is driven by the SYS68K/ASCU-1/2 on any bus request in this type of arbitration. The BCLR* can be disconnected from the bus line by removing jumper B5.

To select the RRS arbiter, the following jumper configuration has to be installed:

Jumperfield B33:



Connected Pins: 2 - 3

10.3 The PRR Arbiter

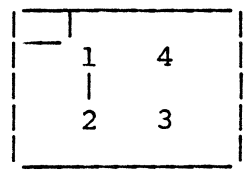
The IEEE-P1014 specification allows 4-level arbiters other than PRI or RRS. The PRR Arbiter which is jumper selectable on the SYS68K/ASCU-1/2 is a realization of what is described in section 3-1 of IEEE-P1014.

BR3* has priority over BR2*, BR1*, BR0*
BR2*, BR1*, and BR0* are of equal preference.

If there is a Bus Request pending on BR3* and the bus is occupied, then the arbiter asserts the BCLR* signal. With this arbiter, the BCLR* operation is correct with only one master requesting on BR3*.

To select the RRS Arbiter, the following jumper configuration has to be installed:

Jumperfield B33:



Connected Pins: 1 - 2

The PRR Arbitration Mode is selected during manufacturing for the SYS68K/ASCU-1 as well as for the SYS68K/ASCU-2.

The yellow LEDs LEV3, LEV2, LEV1, LEV0 light up according to the bus request level of the current Bus Master. If the bus is free and no master is active, then these LEDs are not lit, while the green Bus Free LED lights up. The pattern in which these different lights are lit gives visual information on the bus load situation. The red LED BCLR lights up if the BCLR* signal line is asserted. All of these lights can only be observed if the corresponding even is long enough and occurs often enough to be perceived. If the SYS68K/ASCU-1/2 is inserted in any slot other than slot 1, then the front panel LEDs light up on a random basis.

11. The Bus Timer

VME/P1Ø14 systems contain the BERR* signal line which is used to indicate an unsuccessful data transfer.

The SYS68K/ASCU-1/2 board provides the supervision of data transfers on the bus through a BUS TIMER module. It drives the BERR* line low if an accessed slave board does not respond to the master within a specified time.

The Bus Timer can be selected to work in various modes. When its function has been enabled, eight different time-out periods can be selected for the data transfer cycle. Independent from this selection is the time-out value for Interrupt Acknowledge (IACK) cycles which may take more time than normal cycles. Two different time-out values are provided for the IACK cycle.

The Bus Timer functions are software selectable and can be performed by programming several Port B I/O pins of the PI/T 2 device to be output carrying logical Ø or 1. After reset, all pins are on high level and the Bus Timer is disabled.

Description of the Port B I/O Pins

PBØ, PB1 and PB2: These three output signals select the time-out value for data transfer cycles according to table 21.

Table 21: Bus Time-out Values

Time-out(us)	PB2	PB1	PBØ
8ØØØ	Ø	Ø	Ø
1	Ø	Ø	1
2	Ø	1	Ø
4	Ø	1	1
8	1	Ø	Ø
16	1	Ø	1
32	1	1	Ø
64	1	1	1

PB3: This pin selects the time-out values for Interrupt Acknowledge cycles.

PB3 = Ø	128us
PB3 = 1	32us

PB4: The PB4 output enables or disables the Bus Timer function.

PB4 = Ø	Bus Timer enabled
PB4 = 1	Bus Timer disabled (default conditions after reset and power-up)

The BERR* signal line is driven by the board if a jumper connects the pins 2 and 3 of the jumperfield B3. This jumper is inserted by default.

12. The Serial I/O Interface

For serial communications a Multi-Protocol Communications Controller (MPCC 68561) is provided on the ASCU-1/2 board.

The MPCC interfaces a single serial communications channel using either asynchronous or synchronous protocol. High speed bit rate, separate interrupt vectoring and eight character buffering optimize the MPCC performance to take full advantage of the asynchronous bus structure.

Control, status and data are transferred between the MPCC and the on-board CPU via 22 directly addressable registers. Two First-In/First-Out (FIFO) registers, for receive and transmit data, buffer a maximum of 8 characters at a time. This allows more MPU processing throughput and data security.

The on-chip oscillator drives the internal baud rate generator (BRG). The BRG in conjunction with two selectable prescalers and a 16-bit programmable divider, provides a data bit rate up to 4MHz.

The 48 pin 68561 supports word length (16 bit) or byte length (8 bit) operations.

The mode is controlled by the Protocol Select Register two, bit 7.

After reset the MPCC is initialized in the byte mode. The address signal A5 of the VMEbus and the upper data strobe signal DS1* are combined to provide both operations on the board without any hardware presetting.

The register layout for the byte and word modes is given in tables 22 and 23.

The relative offset to the Board Base Address ($BØ2ØØØ) of the MPCC is $ØØØ.

Table 22: The MPCC Address Map in the Byte Mode of Addressing

Default Board Base Address: $BØ2ØØØ
Device Offset: $ ØØØ

Default Addr.HEX	Regis. Offset	Reset Value	Label	Description
BØ2ØØ1	Ø1	ØØ	MPCRSR	Receiver Status Register
BØ2ØØ3	Ø3	--	MPCRDR	Receiver Data Register
BØ2ØØ5	Ø5	ØF	MPCRIVNR	Receiver Interrupt Vector Number Register
BØ2ØØ9	Ø9	8Ø	MPCTSR	Transmitter Status Register
BØ2ØØB	ØB	--	MPCTDR	Transmitter Data Register
BØ2ØØD	ØD	ØF	MPCTIVNR	Transmitter Interrupt Vector Number Register
BØ2Ø11	11	ØØ	MPCSISR	Serial Interface Status Reg.
BØ2Ø15	15	ØF	MPCSIVNR	Serial Interrupt Vector Number Register
BØ2Ø19	19	ØØ	MPCPSR1	Protocol Select Register 1
BØ2Ø1B	1B	ØØ	MPCAR1	Address Register 1
BØ2Ø1D	1D	Ø1	MPCBRDR1	Baud Rate Divider 1
BØ2Ø1F	1F	ØØ	MPCCCR	Clock Control Register
BØ2Ø21	21	Ø1	MPCRCR	Receiver Control Register
BØ2Ø25	25	ØØ	MPCRIER	Receiver Interrupt Enable Reg.
BØ2Ø29	29	Ø1	MPCTCR	Transmitter Control Register
BØ2Ø2D	2D	ØØ	MPCTIER	Transmitter Interrupt Enable Register
BØ2Ø31	31	ØØ	MPCSICR	Serial Interface Control Reg.
BØ2Ø35	35	ØØ	MPCSIER	Serial Interrupt Enable Reg.
BØ2Ø39	39	ØØ	MPCPSR2	Protocol Select Register 2
BØ2Ø3B	3B	ØØ	MPCAR2	Address Register 2
BØ2Ø3D	3D	ØØ	MPCBRDR2	Baud Rate Divider 2
BØ2Ø3F	3F	Ø4	MPCECR	Error Control Register

Table 23: The MPCC Address Map in the Word Mode of Addressing

Default Board Base Address : $B02000
Device Offset : $ 000 only word accesses allowed

Default Addr.HEX	Regis. Offset	Reset Value	Label	Description
B02020	20	01	MPCRCR	Receiver Control Register
B02021	21	00	MPCRSR	Receiver Status Register
B02022	22	--	MPCRDR	Receiver Data Register
B02023	23	--		
B02024	24	00	MPCRIER	Receiver Interrupt Enable Reg
B02025	25	0F	MPCRIVNR	Receiver Int. Vector No. Reg
B02028	28	01	MPCTCR	Transmitter Control Register
B02029	29	80	MPCTSR	Transmitter Status Register
B0202A	2A	--	MPCTDR	Transmitter Data Register
B0202B	2B	--		
B0202C	2C	00	MPCTIER	Transmitter Int. Enable Reg
B0202D	2D	0F	MPCTIVNR	Trans. Int. Vector No. Reg
B02030	30	00	MPCSICR	Serial Interface Control Reg
B02031	31	00	MPCSISR	Serial Interface Status Reg
B02034	34	00	MPCSIER	Serial Interrupt Enable Reg
B02035	35	0F	MPCSIVNR	Serial Int. Vector No. Reg
B02038	38	00	MPCPSR2	Protocol Select Register 2
B02039	39	00	MPCPSR1	Protocol Select Register 1
B0203A	3A	00	MPCAR2	Address Register 2
B0203B	3B	00	MPCAR1	Address Register 1
B0203C	3C	00	MPCBRDR2	Baud Rate Divider Register 2
B0203D	3D	01	MPCBRDR1	Baud Rate Divider Register 1
B0203E	3E	04	MPCECR	Error Control Register
B0203F	3F	00	MPCCCR	Clock Control Register

Features of the MPCC

- Full duplex synchronous/asynchronous receiver and transmitter
- Fully implements IBM Binary Synchronous Communications (BSC) in two coding formats: ASCII and EBCDIC
- Supports other synchronous character-oriented protocols (COP), such as six-bit BSC, DDCMP, X3.28, X.21, ISO, IS1745, ECMA-16, etc.
- Supports synchronous bit-oriented protocols (BOP), such as SDLC, HDLC/ADCCP, X.25, etc.
- Asynchronous and isochronous modes
- Modem handshake interface
- High speed serial data rate (DC to 4 MHz)
- Internal oscillator and Baud Rate Generator (BRG) with programmable data rate (up to 38.400 Baud)
- Direct interface to 68000/68010/68020 asynchronous bus
- Eight-character receiver and transmitter buffer registers
- 22 directly addressable registers for flexible option selection, complete status reporting, and data transfer
- Three separate programmable interrupt vector numbers for receiver, transmitter and serial interface
- Maskable interrupt conditions for receiver, transmitter and serial interface
- Programmable microprocessor bus data transfer polled or via interrupt
- Selectable full/halt duplex, autoecho and local loop-back modes
- Selectable parity (enable, odd, even) and CRC (control field enable, CRC-16, CCITT V.41, VRC/LRC)

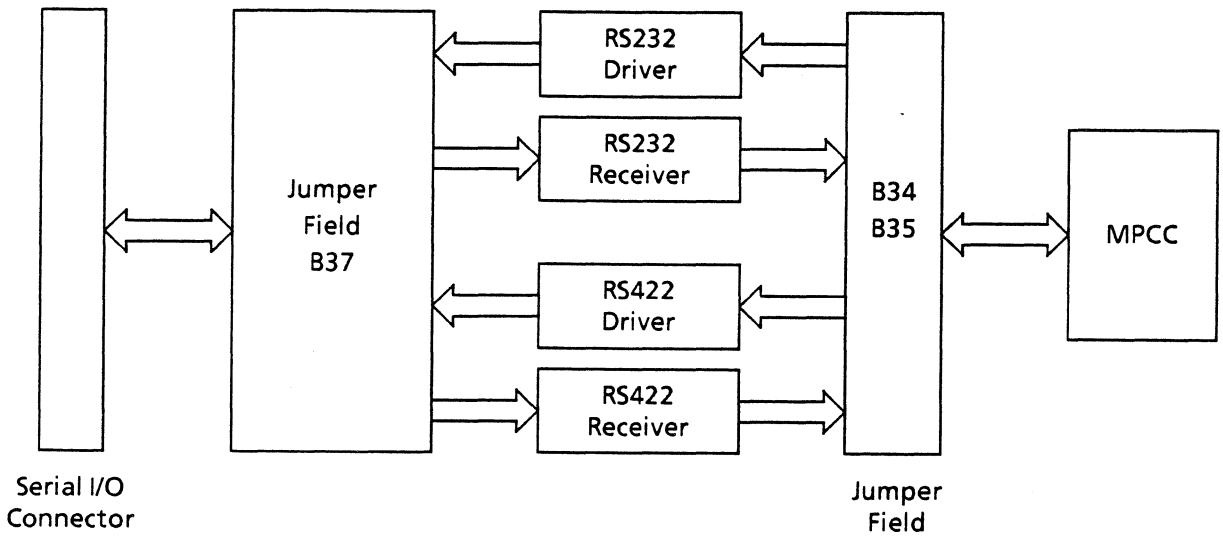
The Serial I/O Hardware Interface

The MPCC requires driver and receiver circuits to communicate via standard voltage levels to other equipment. The SYS68K/ASCU-1/2 board contains RS232 and RS422-compatible interface devices to provide maximum flexibility.

The RS232 interface is realized with one driver IC (1488) and one receiver IC (1489). The driver IC 3487 and the receiver IC 3486 are installed for the RS422 interface.

Figure 23 shows the complete serial I/O interface in a Block Diagram.

Figure 23: Block Diagram of the Serial I/O Interface



The following handshake/control signals are available on the MPCC:

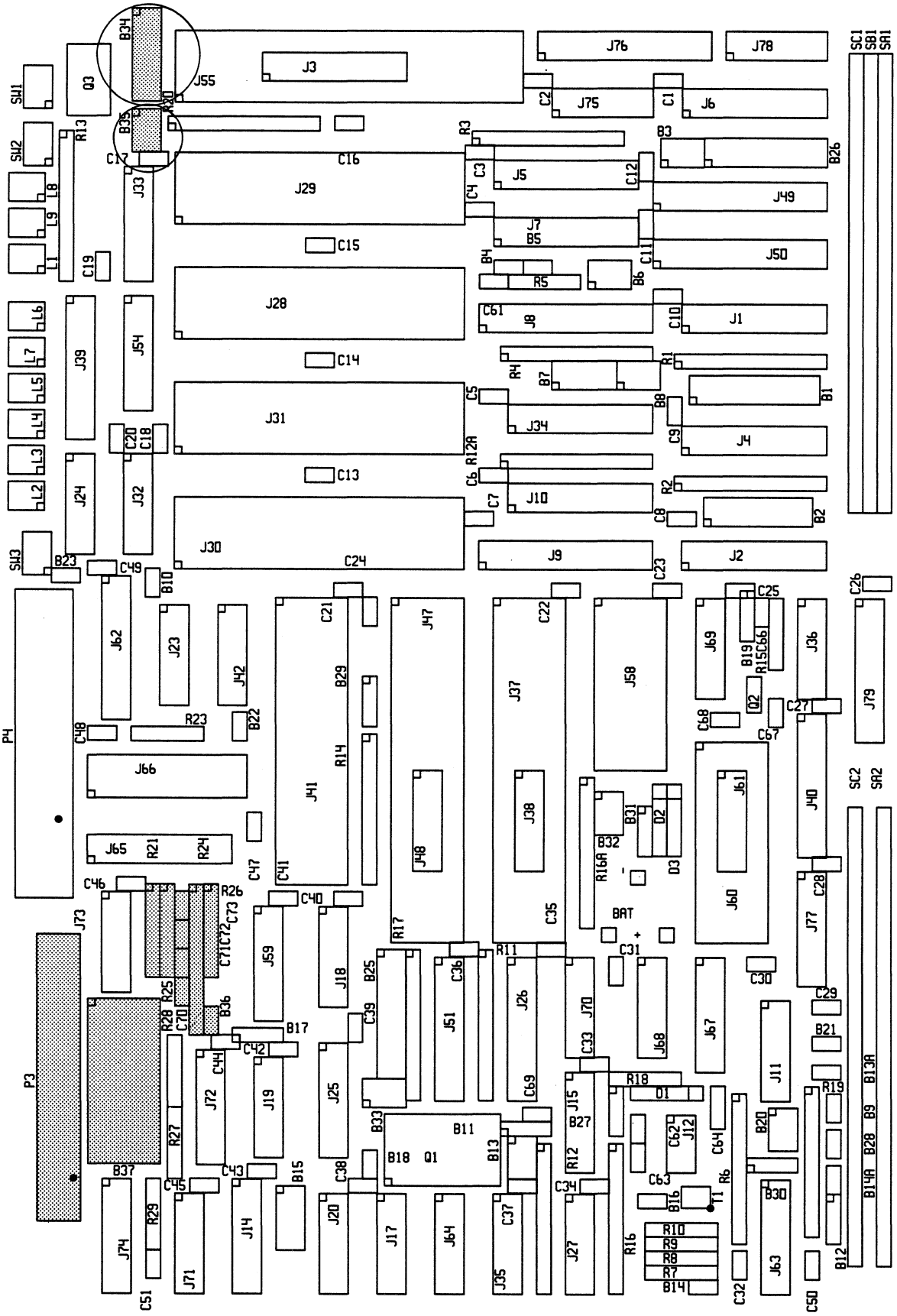
Table 24: The Signal Assignment of the MPCC Serial Interface

MPCC Signal	MPCC Pin	Description		Input	Output
TXD	26	Transmitted Data			x
RXD	3	Received Data		x	
RTS	24	Request to Send			x
CTS	30	Clear to Send		x	
DTR	5	Data Terminal Ready			x
DCD	7	Data Carrier Detect		x	
DSR	6	Data Set Ready	*	x	x
RXC	15	Receiver Clock		x	
TXC	17	Transmitter Clock	*	x	x

* These signals can be used either as input or output.

With the exception of the RXD and TXD signals, all handshake/control signals of the MPCC can be connected to the RS232/422 drivers and receivers by jumpers installed in the jumperfields B34 and B35.

Figure 24: Location Diagram of the Serial I/O Interface Parts



All I/O signals are jumper selectable to the 25 pin female D-Sub connector (P3), located on the front panel.

The jumperfield B37 defines the I/O signal assignment to the connector and provides the selection of the RS232 or the RS422 compatible interface circuits.

Figure 25 outlines the pin-out of the jumperfield B37 with the signal assignment to each pin.

The detailed hardware drawing of the RS232/422 interface is shown in Figure 26.

When the RS232 interface is selected, jumper B36 must be inserted. To enable the RS422 drivers and receivers, remove jumper B36.

Figure 24 shows the location of the serial I/O parts.

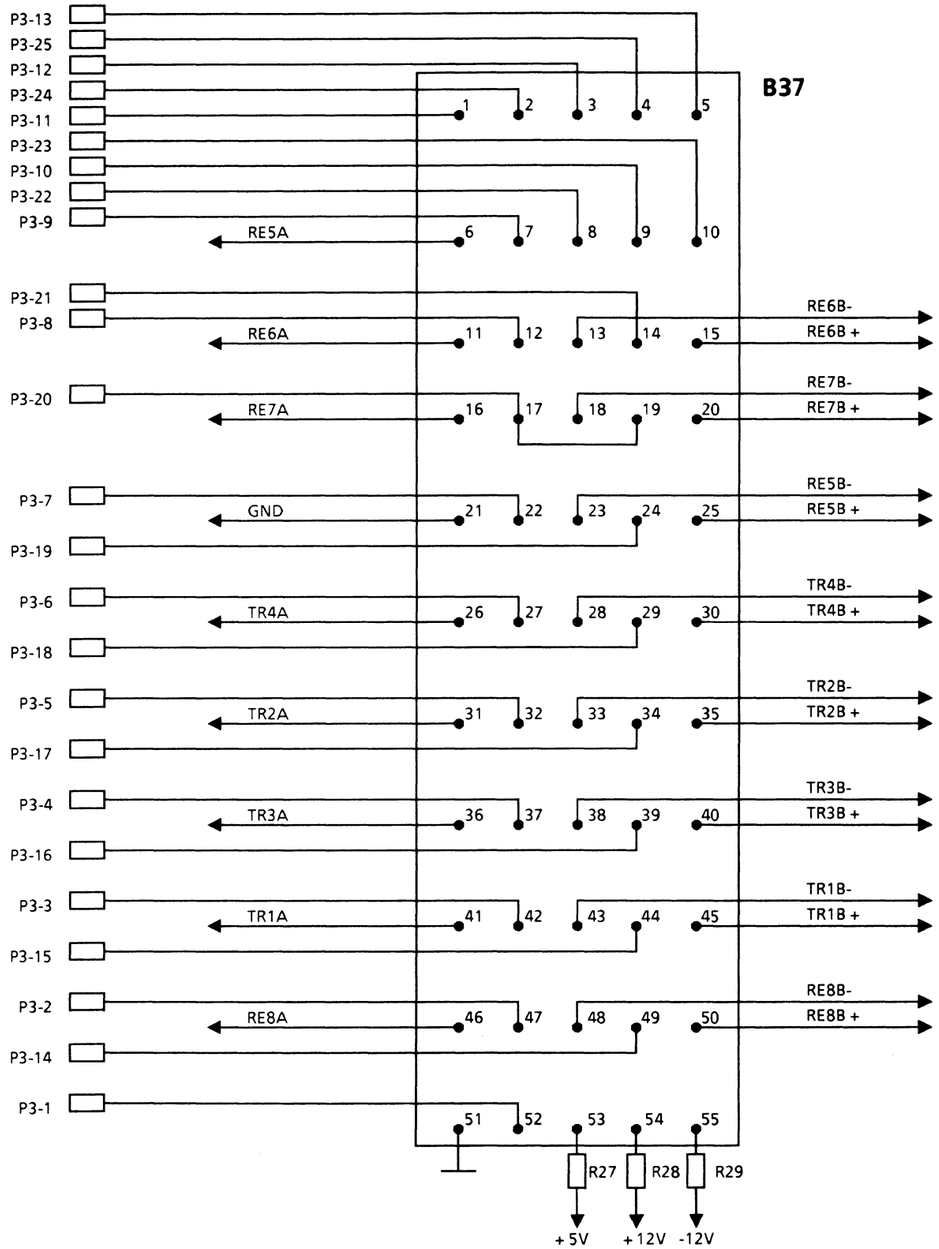
The RS422 input lines can be supplied with additional resistors and capacitors by the user to eliminate spikes and glitches. The locations R24, R25, R26, C7Ø-C73 are therefore provided on the board for this purpose.

Figure 27 shows the optional R/C implementation.

Figure 25: Signal Assignment of Jumperfield B37

1	2	3	4	5
#11	#24	#12	#25	#13
6	7	8	9	10
RE5A	#9	#22	#10	#23
11	12	13	14	15
RE6A	#8	RE6B-	#21	RE6B+
16	17	18	19	20
RE7A	#20	RE7B-	#20	RE7B+
21	22	23	24	25
GND	#7	RE5B-	#19	RE5B+
26	27	28	29	30
TR4A	#6	TR4B-	#18	TR4B+
31	32	33	34	35
TR2A	#5	TR2B-	#17	TR2B+
36	37	38	39	40
TR3A	#4	TR3B-	#16	TR3B+
41	42	43	44	45
TR1A	#3	TR1B-	#15	TR1B+
46	47	48	49	50
RE8A	#2	RE8B-	#14	RE8B+
51	52	53	54	55
GND	#1	+5V	+12V	-12v

Figure 26: Serial I/O Hardware Lay-Out



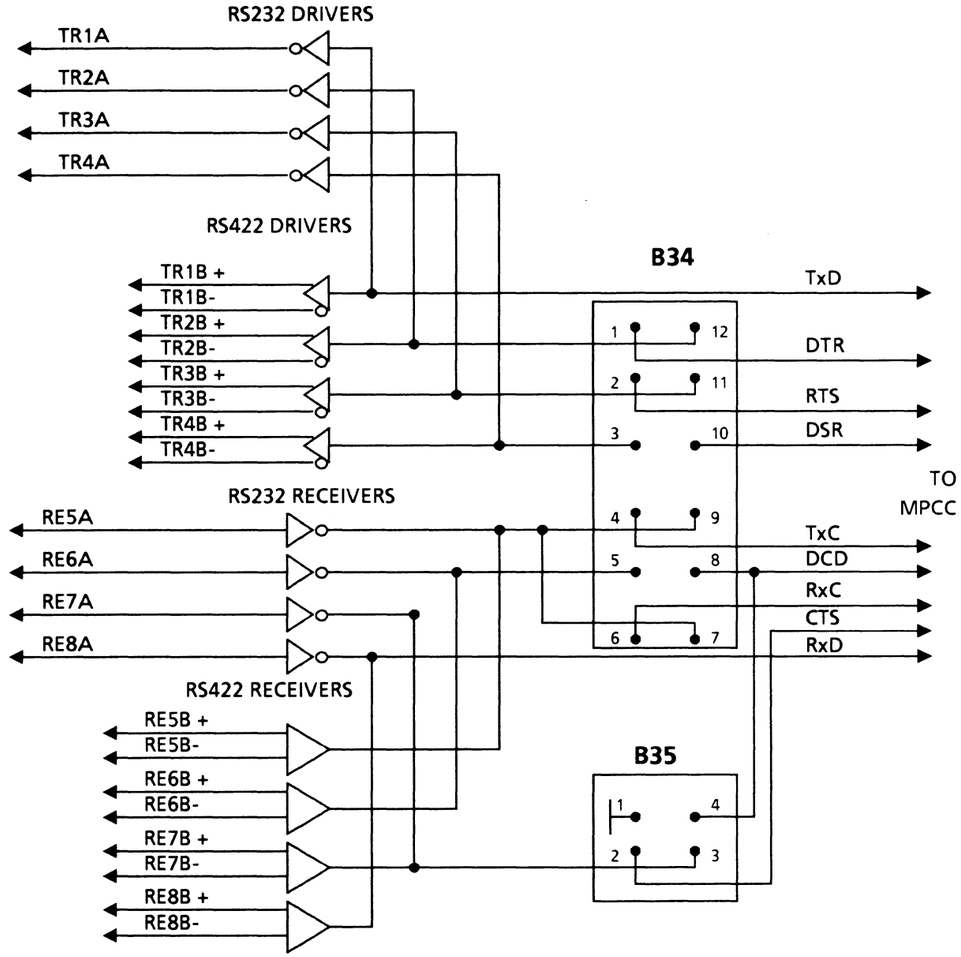
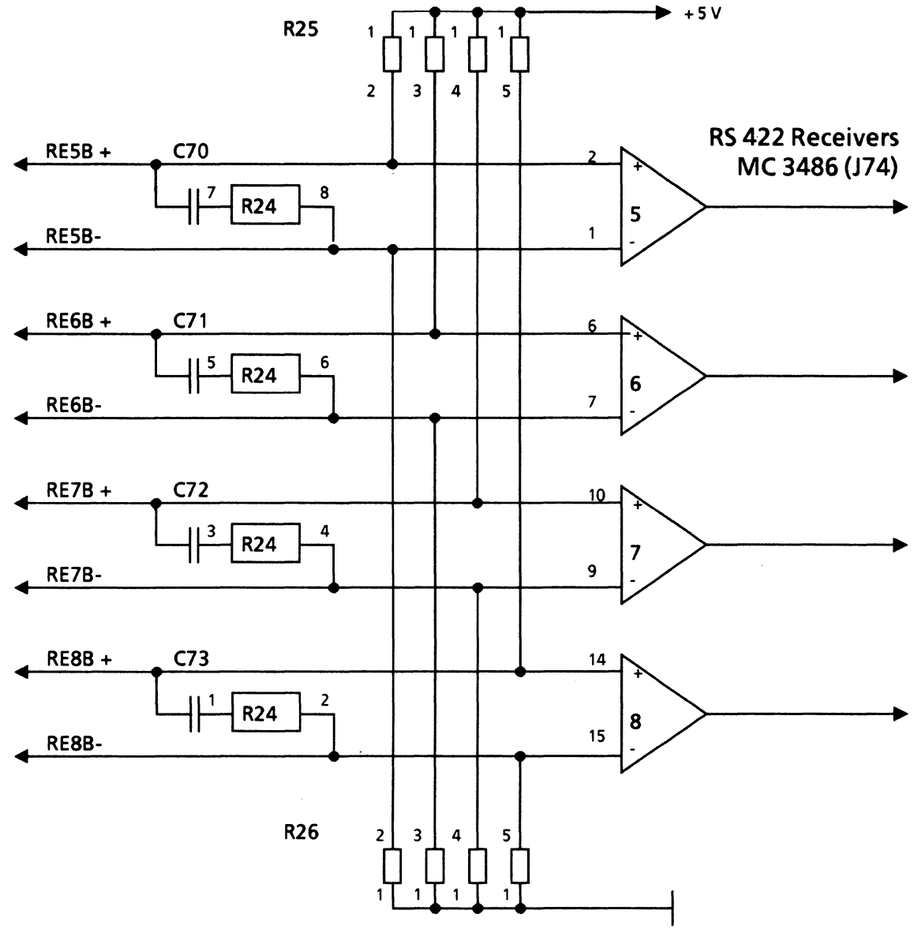


Figure 27: The Optional R/C Implementation



The default jumper settings on the jumperfields B34, B35 and B37 (shown in table 25) allow the connection of a standard terminal by using the following signals from the RS232 interface.

CTS
DTR
TXD
RXD

The terminal interface cable is directly connectable to the 25 pin D-sub connector on the front panel and to the female connector of the terminal. Figure 28 outlines the connection example.

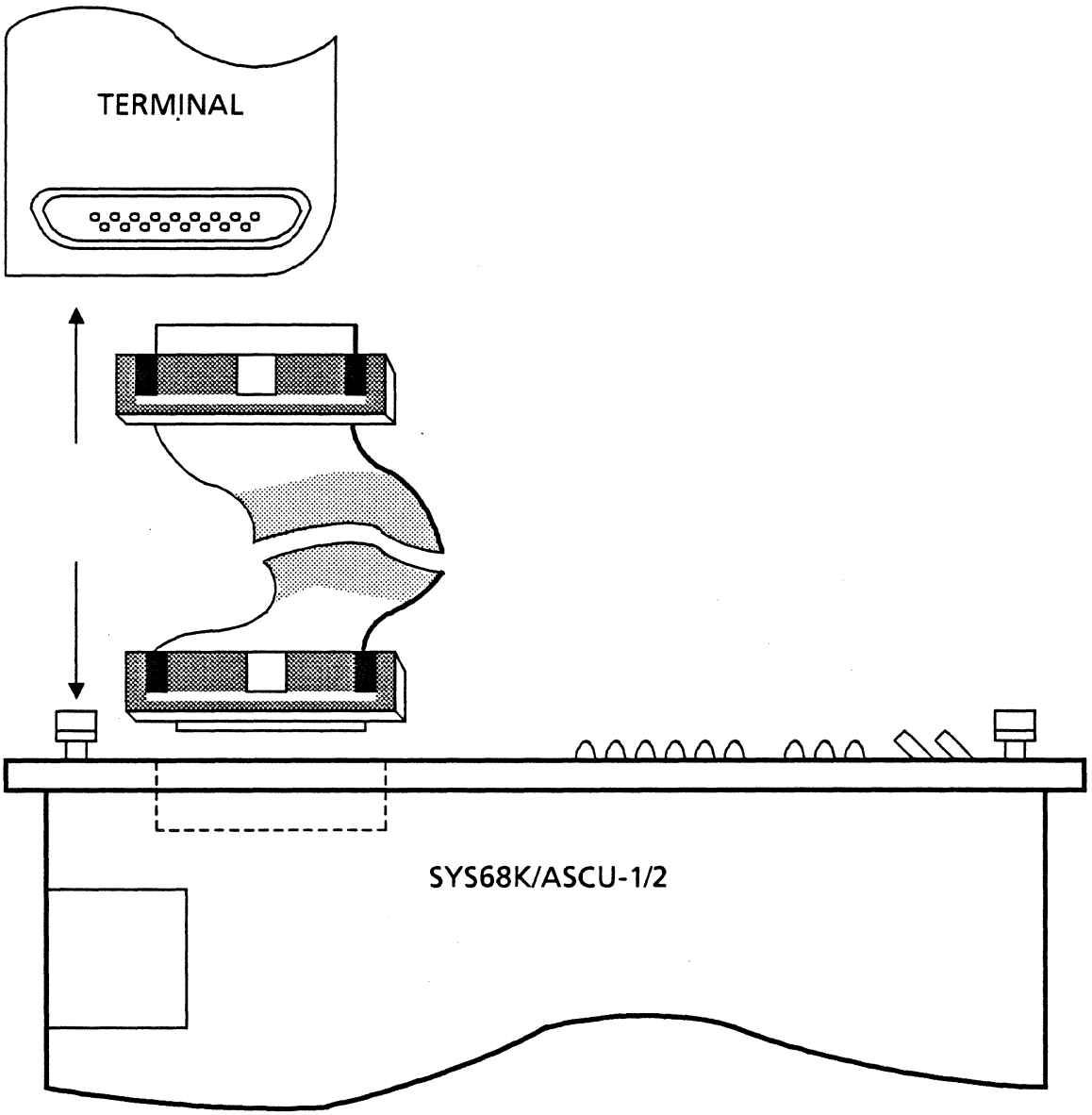
The following program example shows how to initialize the MPCC.

Table 25: Default Jumper Settings for RS232 I/O Signals

Terminal Signal	In <-- --> Out	D-Sub-Connector Pin #	Connected Pins of Jumperfield B37	Connected Pins of Jumperfield B35	Connected Pins of Jumperfield B34	In --> <-- Out	MPCC Signal
DTR	-->	20	16 - 17	2-3		-->	CTS
CTS	<--	5	31 - 32		1-12	<--	DTR
RX Data	<--	3	41 - 42			<--	TXD
TX Data	-->	2	46 - 47			-->	RXD
GND		1	51 - 52				
GND		7	21 - 22				
				1-4		(GND)	DCD

All other signals are not connected by default during manufacturing.

Figure 28:Connection between the SYS68K/ASCU-1/2 Board and a Terminal



12.1 The MPCC Interrupt Scheme

The MPCC can force an interrupt to the VMEbus via the interrupt channel 7 which is provided by a Bus Interrupter Module. Two BIM 2 registers are associated to the interrupt channel 7: The Control Register, and the Vector Register.

The level, on which the interrupt will be generated to the VMEbus is selectable by the Control Register (bits Ø-2). Bit 5 of the Control Register (X/IN) selects whether either the BIM will respond to the interrupt handler supplying the interrupt vector of the associated vector register, or the interrupt source with its own vector.

The MPCC always responds to the interrupt acknowledge cycle with one of its own vectors. Therefore, the external/internal (X/In) list of the BIM Control Register must be set (1) to disable the response from the BIM device.

If the MPCC asserts its IRQ output, causing the BIM to generate an interrupt request to the VMEbus, one of three vectors may be provided by the MPCC to honour the acknowledge cycle. These three vectors are stored in the following MPCC registers:

- Receiver Interrupt Vector Number Register (RIVNR)
- Transmitter Interrupt Vector Number Register (TIVNR)
- Serial Interrupt Vector Number Register (SIVNR)

Corresponding to each register is a status bit which enables/disables the interrupt generating status of the MPCC.

Highest priority is given to the Receiver Interrupt status, followed by the Transmitter Interrupt status and the Serial Interrupt status with the lowest priority.

If the three interrupt states occur simultaneously, they will be handled in order of prioritization and the IRQ output of the MPCC will stay asserted until the last state is removed or disabled. Table 25a lists the register address assignment of interrupt channel 7.

Table 25a: MPCC Interrupt Channel Address Assignment

Interrupt Source	Interrupt Channel Number	Offset to Board Base Address				
		BIM 2		MPCC Vector Register		
		Control Register	Vector Register		Byte Mode	Word Mode
MPCC	7	$115	not used	RIVNR: TIVNR: SIVNR:	$ØØ5 $ØØD $Ø15	$Ø25 $Ø2D $Ø35

12.2 Programming Example

```
*******************************************************************************
*
*       12.2    MPCC PROGRAMMING EXAMPLE
*
*
*       SUBROUTINES INCLUDED:   INITIALIZE THE MPCC:    INITMPCC
*                               INPUT ONE CHARACTER:    CHARIN
*                               OUTPUT A STRING     :   STRINGOUT
*
*
*       The code starting at TEST causes an
*       infinite string out to the connected
*       terminal (Xon/Xoff Protocol)
*
*------------------------------------------------------------------------------
*
*
MPCCBASE:       EQU     $B02000                 ;BASE ADDRESS OF MPCC
*
RSR:            EQU     $01                     ;RECEIVER STATUS REGISTER
RDR:            EQU     $03                     ;RECEIVER DATA REGISTER
RIVNR:          EQU     $05                     ;REC.INT.VECT.NR.REG
TSR:            EQU     $09                     ;TRANSMITTER STATUS REG.
TDR:            EQU     $0B                     ;TRANSMITTER DATA REGISTER
TIVNR:          EQU     $0D                     ;TRANSMITTER INT.VECT.NR.REG.
SISR:           EQU     $11                     ;SERIAL INTERFACE STATUS REG.
SIVNR:          EQU     $15                     ;SERIAL INTERR. VECT.NR.REG.
PSR1:           EQU     $19                     ;PROTOCOL SELECT REG.1
AR1:            EQU     $1B                     ;ADDRESS REGISTER 1
BRDR1:          EQU     $1D                     ;BAUD RATE DIVIDER 1
CCR:            EQU     $1F                     ;CLOCK CONTROL REGISTER
RCR:            EQU     $21                     ;RECEIVER CONTROL REGISTER
RIER:           EQU     $25                     ;RECEIV.INTERR.ENABLE REG.
TCR:            EQU     $29                     ;TRANSMITTER CONTROL REG.
TIER:           EQU     $2D                     ;TRANSM.INTERR.ENABLE REG
SICR:           EQU     $31                     ;SERIAL INTERFACE CONTR.REG.
SIER:           EQU     $35                     ;SERIAL INTERRUPT ENABLE REG.
PSR2:           EQU     $39                     ;PROTOCOL SELECT REGISTER 2
AR2:            EQU     $3B                     ;ADDRESS REGISTER 2
BRDR2:          EQU     $3D                     ;BAUD RATE DIVIDER 2
ECR:            EQU     $3F                     ;ERROR CONTROL REGISTER
*
*------------------------------------------------------------------------------
*
*
*       INPUT ONE CHARACTER INTO D0
*
CHARIN:         MOVEM.L A0,-(A7)                ;PUSH REGISTER TO SAVE
WAITRDA:        MOVE.L  #MPCCBASE,A0            ;LOAD MPCC BASE ADDRESS
                BTST.B  #$07,RSR(A0)            ;TEST RDA BIT
                BEQ.S   WAITRDA
                MOVE.B  RDR(A0),D0              ;READ DATA MPCC -> D0
                MOVEM.L (A7)+,A0                ;POP SAVED REGISTER
                RTS
```

Programming Example cont'd.

```
*-------------------------------------------------------------------------
*
*       INITIALIZE FOR POLLING RECEIVE AND TRANSMIT
*
*
INITMPCC:       MOVEM.L A0,-(A7)                ;PUSH REGISTER TO SAVE
                MOVE.L  #MPCCBASE,A0            ;LOAD MPCC BASE ADDRESS
                MOVE.B  #$01,RCR(A0)            ;RESET RECEIVER
                MOVE.B  #$01,TCR(A0)            ;RESET TRANSMITTER
                MOVE.B  #$00,PSR1(A0)           ;ASYNCHR,8 BIT
                MOVE.B  #$5E,PSR2(A0)           ;2 STOP BITS
                MOVE.B  #$8C,BRDR1(A0)          ;9600
                MOVE.B  #$00,BRDR2(A0)          ;BAUD
                MOVE.B  #$1C,CCR(A0)            ;INTERNAL CLOCK SELECT
                MOVE.B  #$00,ECR(A0)            ;NO PARITY
                MOVE.B  #$00,RIER(A0)           ;DISABLE RECEIVER INTERRUPT
                MOVE.B  #$00,TIER(A0)           ;DISABLE TRANSMITTER INTERRUPT
                MOVE.B  #$00,SIER(A0)           ;DISABLE SER.INTERF. INTERRUPT
                MOVE.B  #$C0,SICR(A0)           ;ASSERT RTS AND DTR OUTPUT
                MOVE.B  #$00,RCR(A0)            ;RECEIVER INTERFACE ENABLE
                MOVE.B  #$80,TCR(A0)            ;TRANSMIT INTERFACE ENABLE
                MOVEM.L (A7)+,A0                ;POP SAVED REGISTER
                RTS
*
*-------------------------------------------------------------------------
*
TEST:           BSR.L   INITMPCC
TESTLOOP:       LEA.L   STRING1(PC),A1
                LEA.L   STRING2(PC),A2
                BSR.L   STRINGOUT
                BRA.S   TESTLOOP
*
STRING1:        DC.B    $0A,$0D,'SYS68K/ASCU-1/2  SERIAL I/O TEST',$0A,$0D
STRING2:        DC.B    $00
                EVEN
*
*-------------------------------------------------------------------------
*
*       SUBROUTINE TO DUMP A STRING
*
*       STOP TRANSMISSION:      XOFF  ($13)
*       RESTART           :     XON   ($11)
*
*       START:  (A1)
*       END   :  (A2)
*
STRINGOUT:      MOVEM.L A0,-(A7)                ;PUSH REGISTER TO SAVE
                MOVE.L  #MPCCBASE,A0            ;LOAD MPCC BASE ADDRESS
NEXTCHAR:       CMP.L   A1,A2                   ;COMPARE IF COMPLETED
                BEQ.S   STRINGEND
BUFFERFUL:      BTST.B  #$07,TSR(A0)            ;TEST TDRA FLAG
                BEQ.S   BUFFERFUL               ;BRANCH IF BUFFER FULL
                BTST.B  #$07,RSR(A0)            ;TEST RDA FLAG
                BEQ.S   OUTPUT                  ;BRANCH IF NO CHARACTER REC.
                CMPI.B  #$13,RDR(A0)            ;TEST RECEIVED DATA
                BNE.S   OUTPUT                  ;BRANCH IF NO XOFF
XOFFLOOP:       BTST.B  #$07,RSR(A0)            ;TEST RDA FLAG
                BEQ.S   XOFFLOOP                ;BRANCH TO WAIT XON CHAR
                CMPI.B  #$11,RDR(A0)            ;TEST RECEIVED DATA
                BNE.S   XOFFLOOP                ;BRANCH TO WAIT XON CHAR
OUTPUT:         MOVE.B  (A1)+,TDR(A0)           ;TRANSMIT CHAR
                BRA.L   NEXTCHAR                ;CONTINUE WITH NEXT CHAR
STRINGEND:      MOVEM.L (A7)+,A0                ;POP SAVED REGISTER
                RTS
```

13. Centronics Interface

The SYS68K/ASCU-1/2 includes a Centronics Parallel Interface for printer connection. This standard centronics interface allows parallel transfer of byte-wide data under control of the DATA STROBE and ACKNLG handshake lines. The handshake protocol is fully under software control. A timing diagram for the Centronics Interface is shown in Figure 29.

The implemented interface supports eight data lines, two handshake lines and several printer status lines, as listed below.

Data Lines	D1 - D8		Output
Handshake Lines	DATA STROBE		Output
	ACKNOWLEDGE	(ACKNLG)	Input
Printer Status Lines	BUSY		Input
	PAPER END/OUT	(PE)	Input
	SELECT	(SLCT)	Input
	ERROR		Input

The hardware realization of the centronics interface is performed by the PI/T 1 device with buffer and inverter devices. A detailed hardware description is given in Figure 30.

The output signals D1-D8 and DATA STROBE are driven from a 74S241 device which has a drive capacity of 64mA. This allows a cable length to the printer of approximately 5 meters. All inputs such as the ACKNLG signal and the printer status signals are received by a 74LS14 device, which provides Schmitt-Trigger inputs for improved noise immunity on these signal lines. The jumperfield B20 enables the user to exchange the connection of the ACKNLG and the BUSY line on the receiver circuit by wire wrap if this should be required.

During manufacturing, jumpers are inserted to connect pin 1-4 and 2-3 of the B20 jumperfield.

Jumper B21 connects the chassis GROUND of the printer to the logic ground of the board. The jumpers on the jumperfields B12 and B3Ø select the function of the P2 connector pins A1 and A2. These pins provide the signal ground for the DATA STROBE and the Data 1 signal and have to be connected to ground. Therefore, the jumpers on B12 and B3Ø have to be installed in the following way:

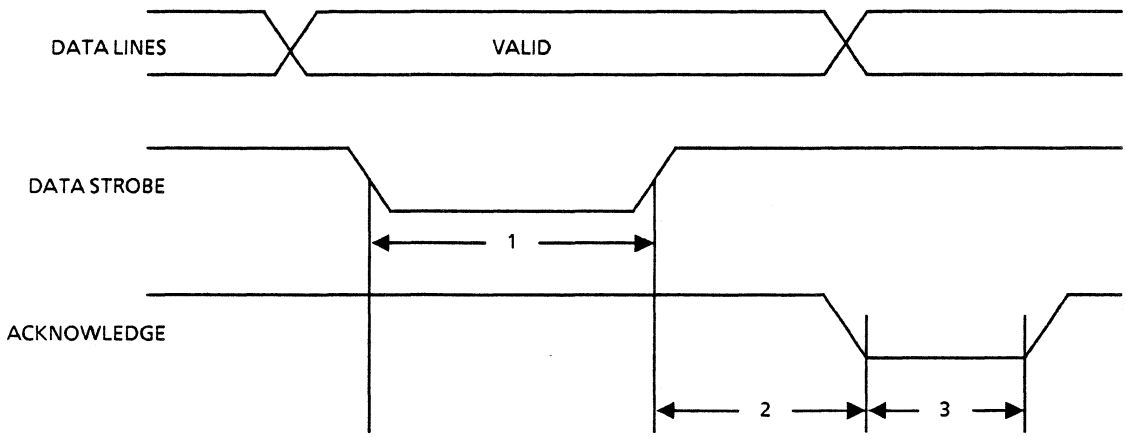
Jumperfield	Connected Pins
B12	2 - 3
B3Ø	1 - 2

Please refer to chapter 5.1 "Utility Signal Handling", sections 5.1 and 5.3 where pins A1 and A2 are described in their capacity as ACFAIL and Reset inputs.

Easy 1:1 signal transmission of the installed Centronics Interface to the printer connector pins as outlined in Table 26 is provided by using a flat cable for interconnection.

Figure 31 shows a connection example and the pin orientation of the connectors and Figure 32 outlines the location diagram of all Centronics Interface parts.

Figure 29: Timing Diagram of the Centronics Parallel Interface



Time Values

No.		MIN	MAX
1	Data Strobe active	0.50µs	
2	TOLY Delay Time	50µs	1.0ms
3	ACK Acknowledge Time	4µs	50µs

Figure 30: Hardware Realization of the Centronics Interface

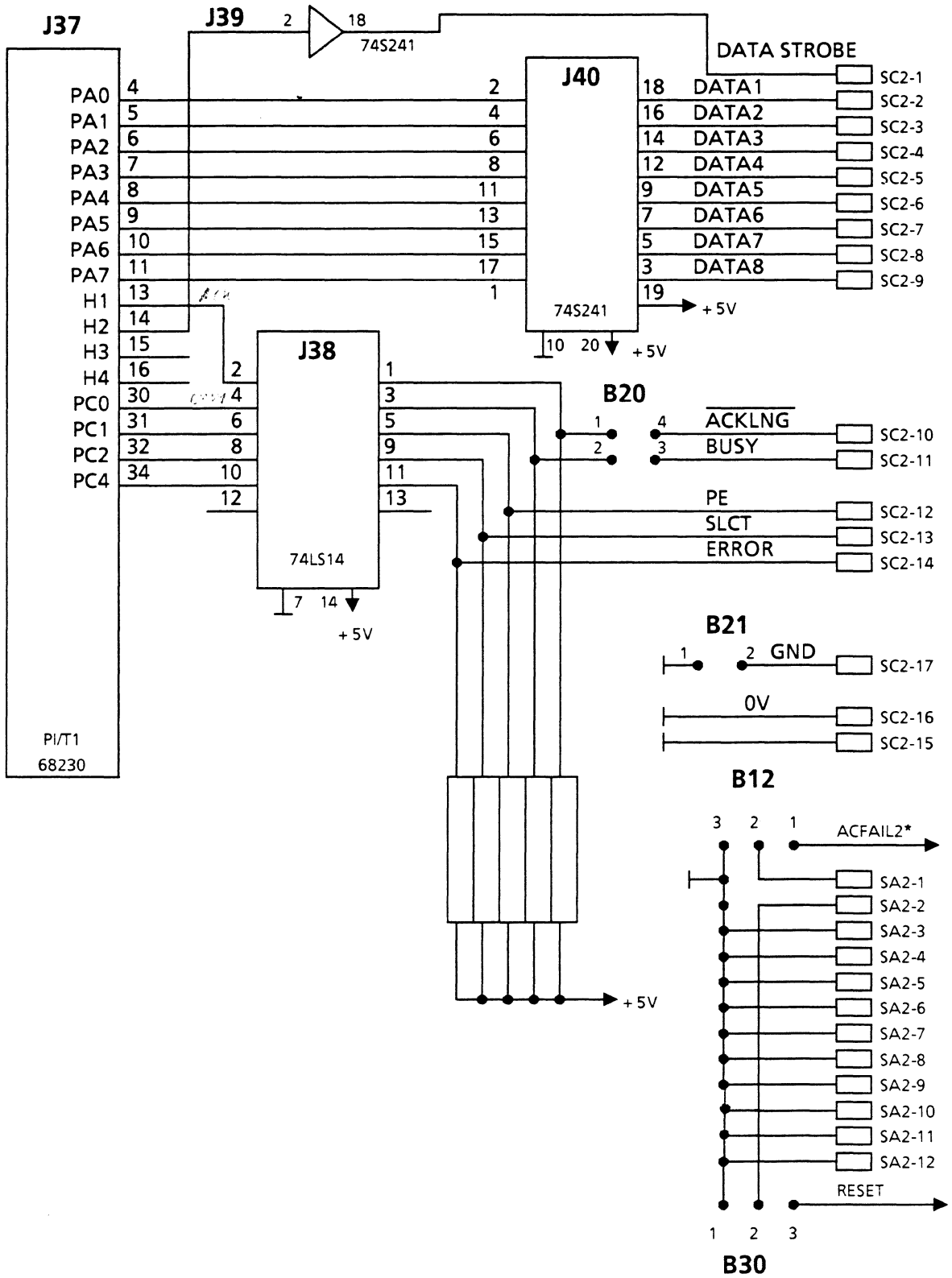


Table 26 shows the signal assignment of the Centronics Interface to the P2-connector and to the Centronics printer connector.

Table 26: Signal Assignment of the Centronics Printer Interface

Signal Name	P2 Connector Pins	Centronics Printer Connector Pins
DATA STROBE	C1	1
GND	A1	19
DATA 1	C2	2
GND	A2	20
DATA 2	C3	3
GND	A3	21
DATA 3	C4	4
GND	A4	22
DATA 4	C5	5
GND	A5	23
DATA 5	C6	6
GND	A6	24
DATA 6	C7	7
GND	A7	25
DATA 7	C8	8
GND	A8	26
DATA 8	C9	9
GND	A9	27
ACKNLG	C10	10
GND	A10	28
BUSY	C11	11
GND	A11	29
PE	C12	12
GND	A12	30
SLCT	C13	13
ERROR	A14	32
GND	A15	33
LOGIC GND	C16	16
CHASSIS GND	C17	17

Figure 31: Connection Example for the Centronics Interface

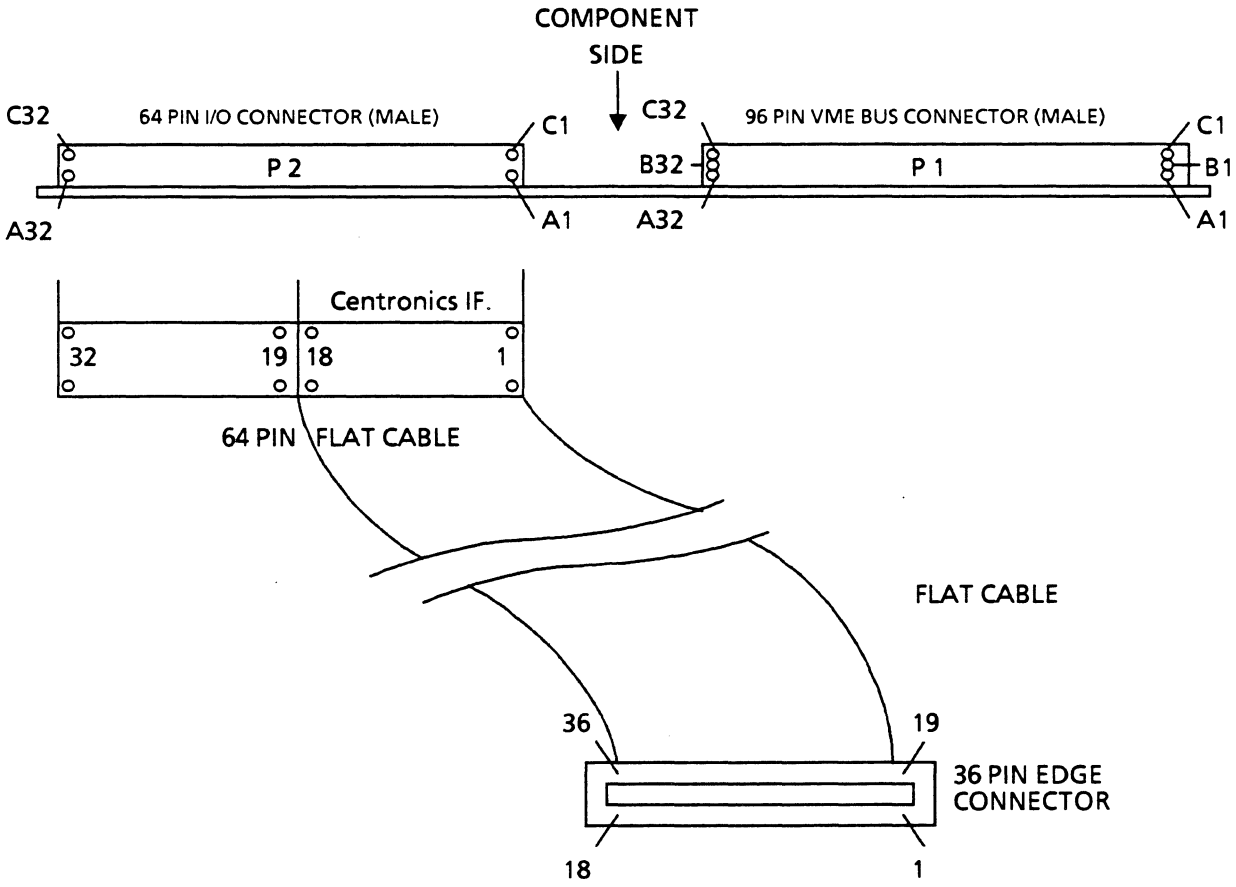
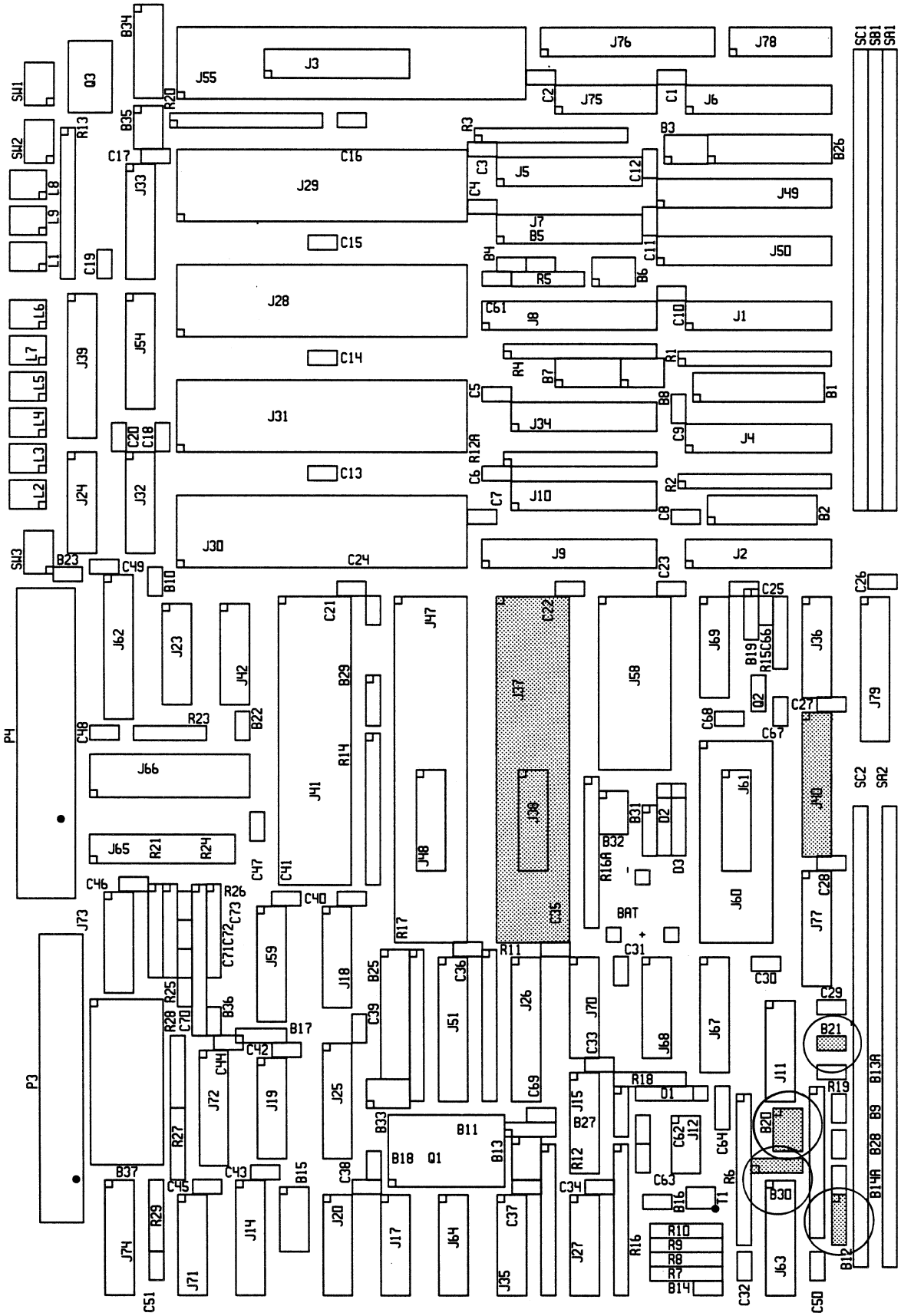


Figure 32: Location Diagram of the Centronics Interface Components



13.1 Interrupt Scheme of the Centronics Interface

An interrupt request of the Centronics Interface to the VMEbus can be forced when the H1 handshake line of the PI/T 1 device, which is assigned the ACKNLG signal, is asserted.

The edge sensitive handshake pin may be programmed as either active high or active low input (printer type dependent).

When the PI/T is enabled to supply the interrupt vector, it will provide a vector set together by the upper six bits of the Port Interrupt Vector Register (PIVR Bit 2-7), and the 2 bit value ØØ, assigned to the H1 interrupt source.

The Port Interrupt of the PI/T 1 device is transmitted to the VMEbus via the interrupt channel no. 1. This channel assigns two registers of the BIM 1 device.

The Control Register (offset address $1Ø1) and

the Vector Register (offset address $1Ø9).

The Control Register can be programmed to let the interrupt vector be supplied either by the interrupt source (PI/T device) or by the BIM itself with the content of the associated vector register.

The initialization of the PI/T and the BIM device must insure than only one interrupt vector is provided during the interrupt acknowledge cycle. Table 27 shows the registers associated to the interrupt channel 1 with its register addresses.

Table 27: Centronics Interrupt Assignment

Interrupt Source	Interrupt Channel Number	Offset to Board Base Address: BIM 1 Control Register	BIM 1 Vector Register	PI/T 1 Port Interrupt Vector Register
Centronics Interface (H1 pin)	1	$1Ø1	$1Ø9	not used
	1	$1Ø1	not used	$Ø4B

A programming example for the Centronics Interface is listed on the next page.

Centronics Interface Programming Example

```
*******************************************************************************
*
*       PROGRAMMING EXAMPLE
*
*       68230 PARALLEL INTERFACE/TIMER
*       USED AS A CENTRONICS INTERFACE
*
*       PRINTER:
*       TANDBERG DATA PRINTER
*
*------------------------------------------------------------------------------
*
PIT     EQU     $B02040                 ;BASE ADDRESS FOR PI/T
PGCR    EQU     PIT+1                   ;PORT GENERAL CONTROL REGISTER
PADDR   EQU     PIT+5                   ;PORT A DATA DIRECTION REGISTER
PACR    EQU     PIT+$D                  ;PORT A CONTROL REGISTER
PADR    EQU     PIT+$11                 ;PORT A DATA REGISTER
PSR     EQU     PIT+$1B                 ;PORT STATUS REGISTER
*
*------------------------------------------------------------------------------
*
*       MAIN PROGRAM
*
        BSR     INIT
        LEA.L MES(PC),A2
@0010   MOVE.B (A2)+,D0
        CMPI.B #4,D0
        BEQ.S EXIT
        BSR     WRITE
        BSR DELAY
        BRA.S @0010
EXIT    XEXT                            ;Return to monitor
*------------------------------------------------------------------------------
*
*       INIT---INITIALISATION OF PI/T   UNIDIRECTIONAL 8-BIT MODE 0 SUBMODE 1X
*                                       PORT A OUTPUT  8 BIT
*                                       H2 => DATA STROBE
*                                       H1 => ACKNLG
*
INIT:   MOVE.B  #$FF,PADDR              ;8 BITS OUT
        MOVE.B  #$A8,PACR               ;SUBMODE 1X, H2=HIGH,
        MOVE.B  #$13,PGCR               ;MODE 0, H12 ENABLE, H2 INVERS
        RTS
*------------------------------------------------------------------------------
*
*       ROUTINE FOR CENTRONICS HANDSHAKE: WRITE
*
WRITE:  BTST    #1,PSR
        BNE     WRITE
        MOVE.B  D0,PADR                 ;CHAR IN D0, OUT ON PORT A
        MOVE.B  #$A0,PACR               ;H2=DATA STROBE => LOW
        MOVE.B  #$A8,PACR               ;H2=DATA STROBE => HIGH
        RTS
*
*------------------------------------------------------------------------------
DELAY:  MOVE.L #$1000,D0
@0010   SUBQ.L #1,D0
        BNE.S @0010
        RTS
*
MES     DC.B $0D,'ABCDEFGHIJKLMNOPQRSTUVWXYZ',$0D,$0A,4
*
        EVEN
        END
```

14. The Real Time Clock

The SYS68K/ASCU-1/2 contains a real time clock (RTC 58167A) with battery backup. This guarantees the operation of the RTC even when the board is powered down or in transit. The lithium battery included in the shipment is packed separately to prevent discharging by the aluminium foil.

A jumper on the jumperfield B31 selects the main power sources for the RTC. Table 28 lists the possible settings.

Table 28: Power Connection for the RTC

Supply Source	Jumperfield B31 Connected Pins
+5V System VCC	1 - 2 *
+5V System Standby	2 - 3

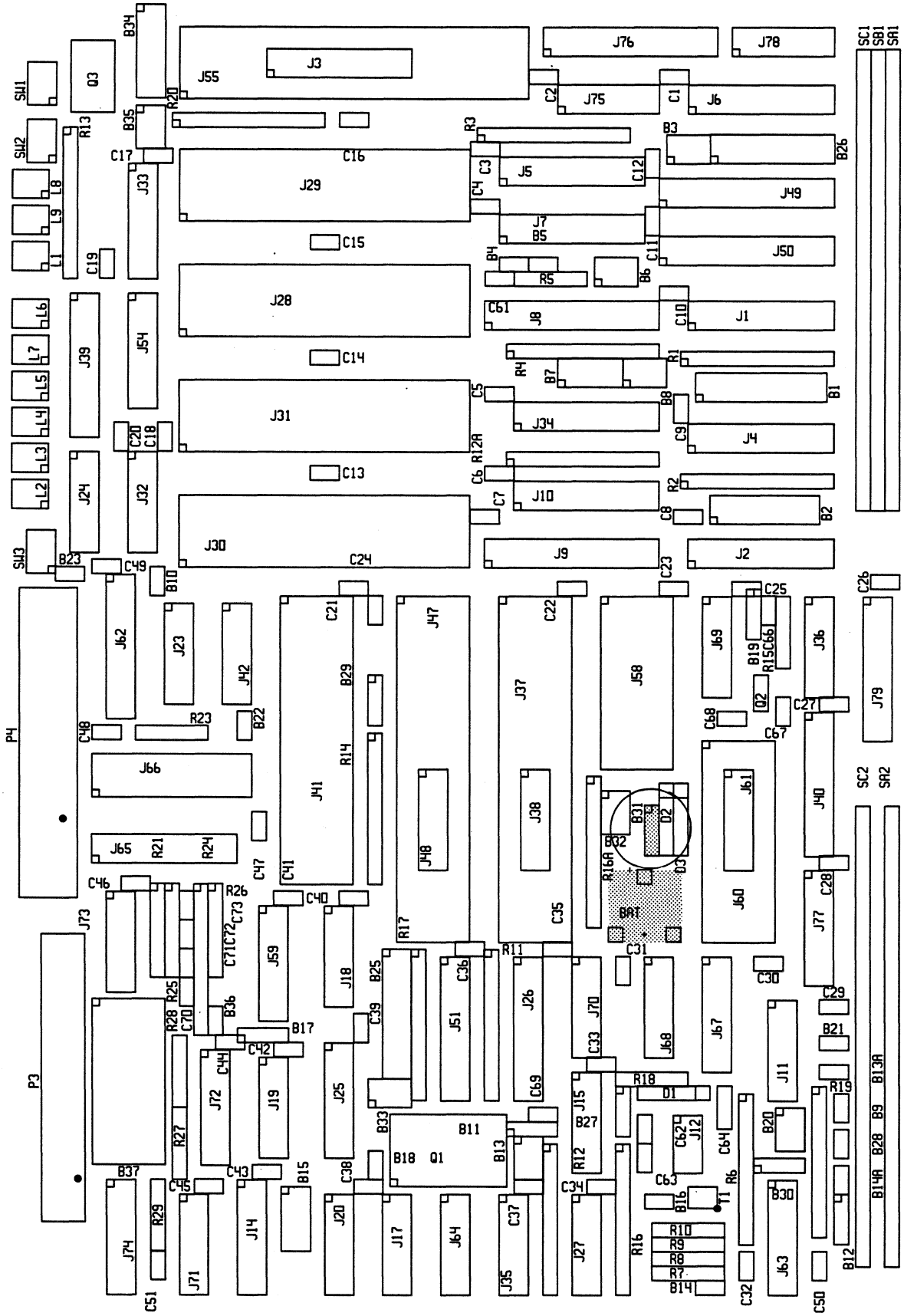
* default during manufacturing

Figure 33 shows the location of the battery position and the jumperfield B31.

Battery backup is provided through soldering the lithium battery on to the board. This has to be done carefully.

Caution: The power to the RTC device has to be disconnected before the battery can be soldered onto the board (see Figure 33).

Figure 33: Location Diagram of the Jumperfield B31 and the Battery Position



14.1 Features of the RTC

The RTC has the following features:

- 1/10000 of a second through month counter
- 56 bits of RAM with comparator to compare the real time counter to the RAM data
- Interrupt output with 8 possible interrupt signals
- Power-down mechanism disables all input and output signals
- Status register to indicate rollover during a read cycle
- 32.768Hz crystal oscillator
- Four year calendar (no leap year)
- 24 hour clock

Addressing of the RTC

Provided that the Board Base Address is $B02000, the access address of the first register of the RTC is $B020C1. The device offset $0C0 is related to the selected board base address.

Only single byte data transfers to/from the RTC are allowed on the data bits D0-D7. Therefore, all accesses to the RTC registers must be performed on odd addresses.

Table 29 lists RTC registers and the corresponding access address.

Table 29: Register Table of the RTC

Default Board Base Address: $BØ2ØØØ
Device Offset: $ ØCØ

Default Address HEX	Register Offset	Reset Value	Label	Description
BØ2ØC1	Ø1	--	RTCCTTS	Counter - ten thousands of secs
BØ2ØC3	Ø3	--	RTCCHTS	Counter - hundredths + tenths of secs
BØ2ØC5	Ø5	--	RTCCSEC	Counter - seconds
BØ2ØC7	Ø7	--	RTCCMIN	Counter - minutes
BØ2ØC9	Ø9	--	RTCCHRS	Counter - hours
BØ2ØCB	ØB	--	RTCCDOW	Counter - day of week
BØ2ØCD	ØD	--	RTCCDOM	Counter - day of month
BØ2ØCF	ØF	--	RTCCMON	Counter - month
BØ2ØDØ	11	--	RTCRTTS	RAM - ten thousandths of secs
BØ2ØD3	13	--	RTCRHTS	RAM - hundredths + tenths of secs
BØ2ØD5	15	--	RTCRSEC	RAM - seconds
BØ2ØD7	17	--	RTCRMIN	RAM - minutes
BØ2ØD9	19	--	RTCRHRS	RAM - hours
BØ2ØDB	1B	--	RTCRDOW	RAM - day of week
BØ2ØDD	1D	--	RTCRDOM	RAM - day of month
BØ2ØDF	1F	--	RTCRMON	RAM - month
BØ2ØE1	21	--	RTCISR	Interrupt Status Register
BØ2ØE3	23	--	RTCICR	Interrupt Control Register
BØ2ØE5	25	--	RTCCRES	Counters reset
BØ2ØE7	27	--	RTCRRES	RAM reset
BØ2ØE9	29	--	RTCSTAT	Status bit
BØ2ØEB	2B	--	RTCGO	GO command
BØ2ØED	2D	--	RTCSINT	Standby interrupt
BØ2ØFF	3F	--	RTCTEST	Test mode

14.2 Timing of the RTC

The read/write timing diagram and the time values are given in Figures 34 and 35 and in Table 30/31.

The RTC is a metal gate CMOS circuit which has an access time of approximately 1100ns. This requires a special delay of the DTACK* signal by accesses to/from the RTC.

Table 30: RTC Write Time Values

Number	Parameter	(Note A) Min.	Max
1	Axx valid and IACK* high to AS* low	10	
3	AS* high	30	
4	AS* low to CSRTC active	0	
5	AS* active	0	
6	AS* invalid to UDS* high	0	40
7	AS* inactive to CSRTC inactive	0	40
8	AS* low to LDS* low (WRITE)	10	130
9	AS* low to DTACK* low	1800	2500
11	AS* inactive to DTACK inactive	15	45
12	AS* active to WRITE* low	10	150
13	AS* inactive to WRITE* inactive	10	70
14	Data valid to Data Strobes active	10	
15	AS* inactive to Data invalid	10	45

Figure 34: RTC Write Cycle Timing Diagram

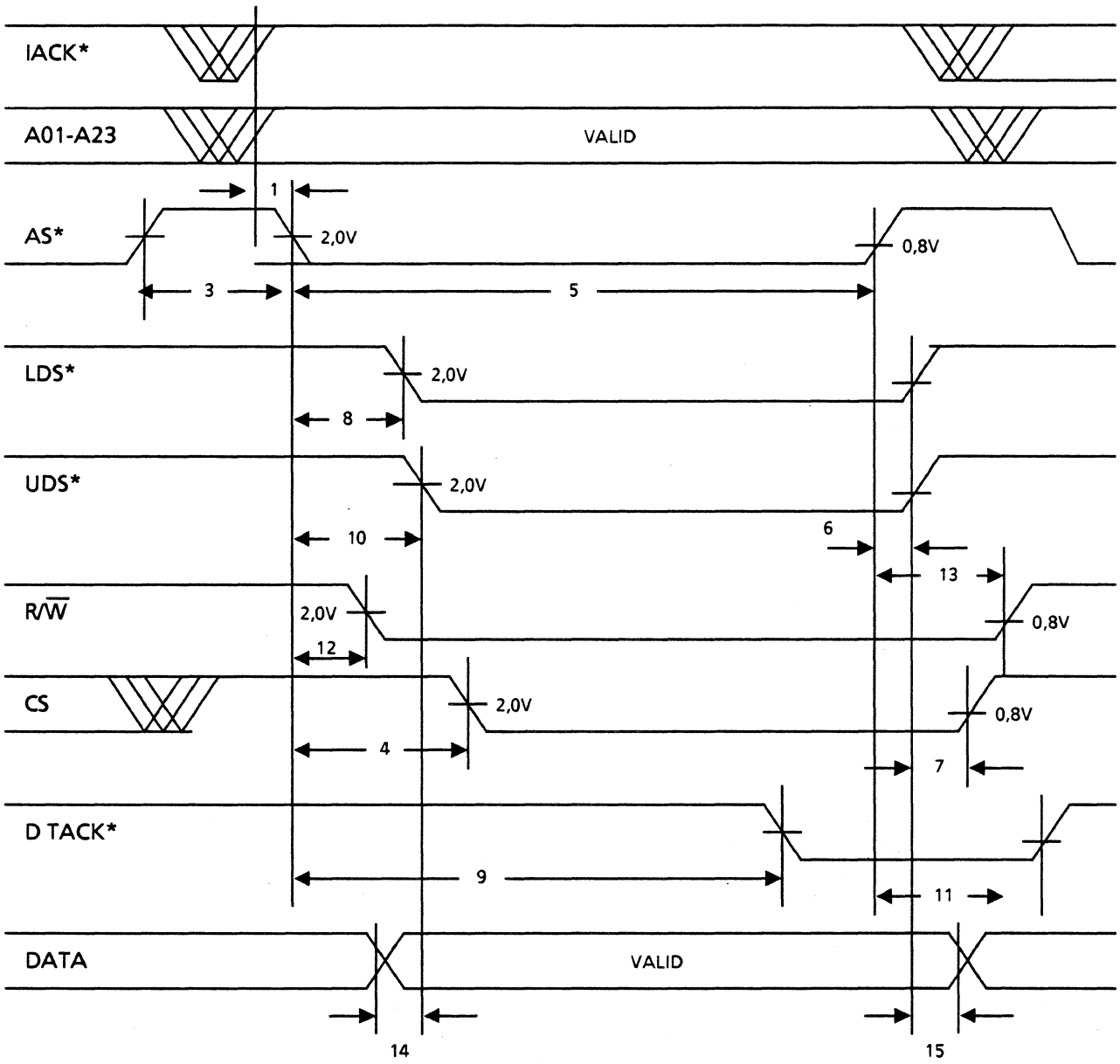
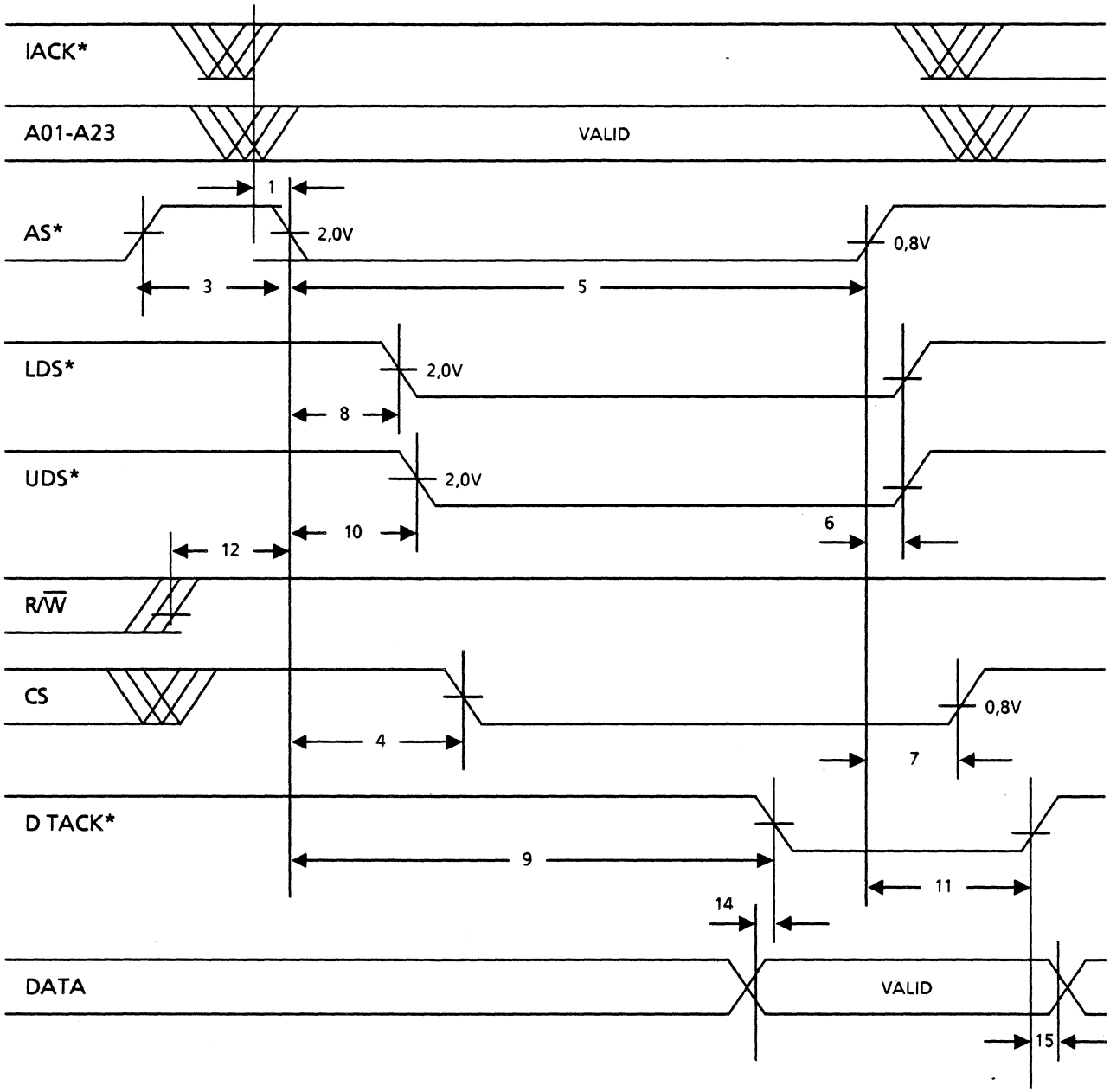


Table 31: RTC Read Time Values

Number	Parameter	(Note A) Min.	Max
1	Axx valid and IACK* high to AS* low	10	
3	AS* high	30	
4	AS* active to CSRTC low	30	60
5	AS* low	1800	2500
6	AS* inactive to UDS* inactive	10	60
7	AS* inactive to CSRTC inactive	0	40
8	AS* active to LDS* valid	10	130
9	AS* low to DTACK low	1800	2500
11	AS* inactive to DTACK inactive	15	45
12	WRITE* high to AS* active	10	
14	Data valid to DTACK active	10	
15	DTACK inactive to Data invalid	10	60

Figure 35: RTC Read Cycle Timing Diagram



14.3 The RTC Interrupt Scheme

The RTC can be used to force an interrupt request to the VMEbus. Since the interrupt request is transmitted from the RTC to the bus by a BIM device, every interrupt request level can be used.

The RTC is assigned the interrupt channel number 6 with the associated BIM registers given in Table 32.

Table 32: RTC Interrupt Channel Address Assignment

Interrupt Source	Interrupt Channel Number	Interrupter Device	Offset to Board Base Addr.	
			BIM Control Reg.	BIM Vector Reg.
RTC	6	BIM 2	$113	$11B

If the BIM device is initialized to enable the RTC interrupt request it also has to provide the interrupt vector stored in the BIM vector register, because the RTC does not supply the vectorized protocol.

15.Ø Special Interrupts

15.1 The Test Interrupt

An interrupt generation to the VMEbus is provided by the Test Interrupt switch which is located on the front panel (see Figure 8).

A second switch can be connected in parallel on connector P2. To enable the function of this switch, the jumper B28 has to be removed. If there is no switch connected, jumper B28 must be installed. This is the default condition. The location of jumperfield B28 is outlined in Figure 36.

The external interrupt switch should be connected to the P2 connector according to Figure 37.

The Test Interrupt switch on the front panel and the optional connectable external switch share one interrupt channel provided by the BIM2 device. Pushing one of the TEST switches causes an interrupt.

Using the test switch requires the initialization of the BIM's control register and vector register in the way that the interrupt vector is supplied by the BIM device.

The access address of the associated BIM registers are shown in the following table.

Table 33: TEST Interrupt Channel Address Assignment

Interrupt Source	Interrupt Channel Number	Interrupter Device	Offset to Board Base Addr.	
			BIM Control Reg.	BIM Vector Reg.
Test Interrupt	6	BIM 2	$111	$119

The Test Interrupt function provides a VME compatible interrupt if a jumper on the jumperfield B27 connects the pins 2-3 (this is the default condition).

The jumper setting connecting the pins 1-2 of B27 can be used to support non-VME compatible edge-sensitive interrupts (e.g. level 7 of a 68ØØØ processor).

Figure 36: Location Diagram of the TEST Interrupt Jumperfield

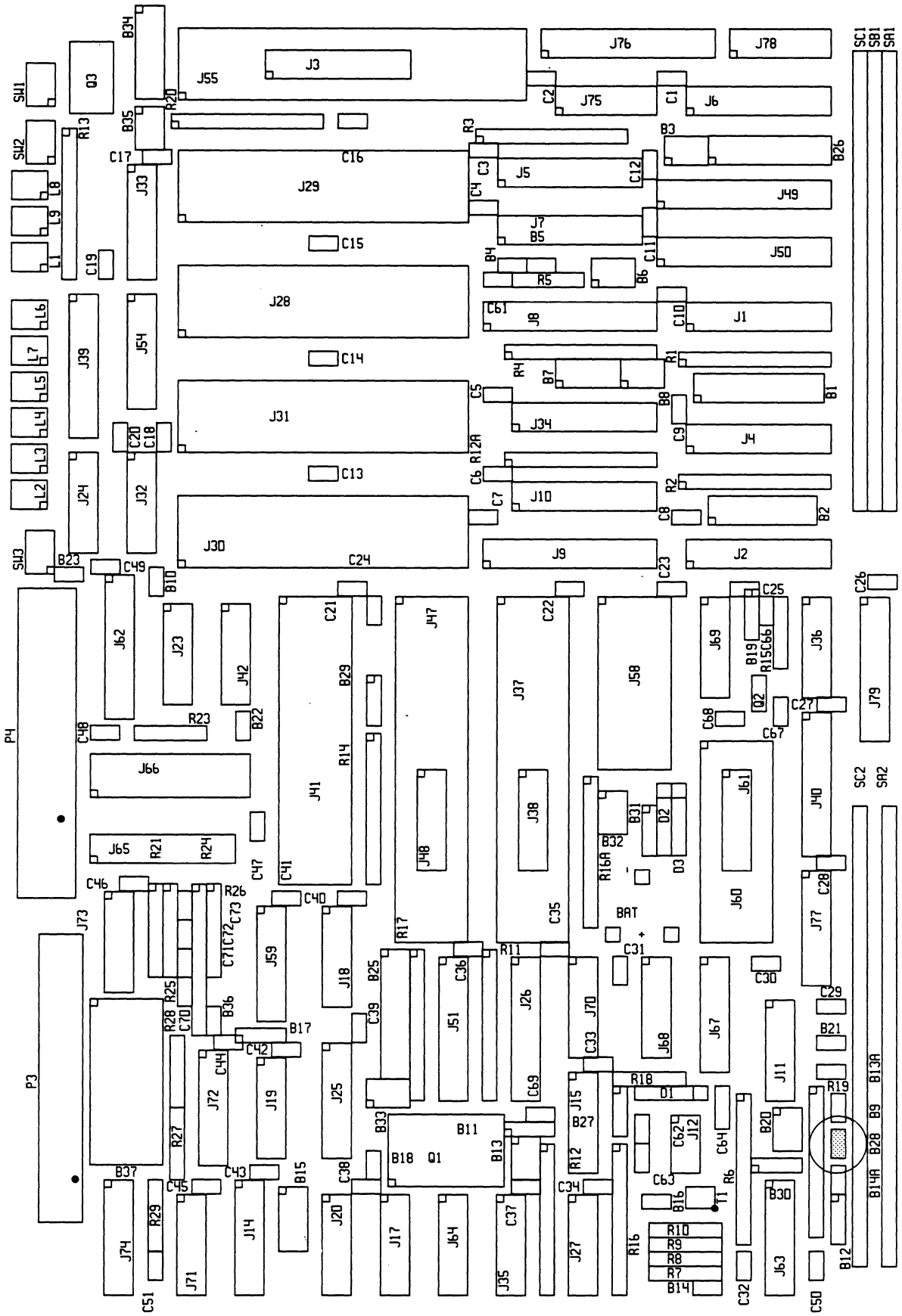
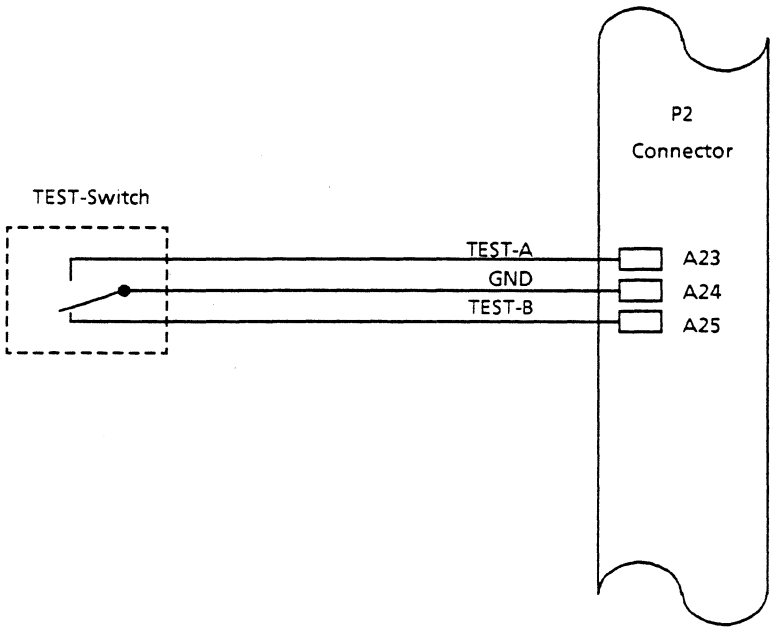


Figure 37: Connection of an External TEST Switch



15.2 The User Interrupt 1

The SYS68K/ASCU-1/2 is able to let external devices or another system generate an interrupt to the VMEbus. One external interrupt can be connected to the ASCU-1 and has to be attached to the P2 connector pin A28. The designation USINT1 is given to this input line on the hardware schematics.

The input is buffered with a 74LS14 device and uses the H3 handshake line of the PI/T 1 (J37) device for an interrupt request generation. The H3 input may be programmed as either active high or active low and has associated its own interrupt vector (stored in the Port Interrupt Vector Register PIVR).

The User Interrupt 1 is transmitted to the VMEbus via the Interrupt Channel 1 which is provided by the BIM 1 device. The Interrupt Channel 1 is assigned the two BIM 1 registers.:

Control Register (Offset to Board Base Address: $1Ø1)

Vector Register (Offset to Board Base Address: $1Ø9)

When the Control Register is programmed for an external response during the IACK cycle, the BIM vector register is not used. In this case the content of the PIVR with the associated H3 interrupt vector is supplied to honour the Interrupt Acknowledge.

15.3 User Interrupts 2-5

The SYS68K/ASCU-2 provides in addition to the User Interrupt 1 input the four User Interrupts 2, 3, 4 and 5 to let peripheral interrupt sources generate interrupts to the VMEbus.

These input lines are available at the P2 connector pins A29, A30, A31, A32, and are assigned to the handshake pins H1, H2, H3 and H4 of the second Parallel Interface/Timer Module (PI/T 2, J47) according to the following list:

User Interrupt 2	->	A29	->	Handshake pin H1
User Interrupt 3	->	A30	->	Handshake pin H2
User Interrupt 4	->	A31	->	Handshake pin H3
User Interrupt 5	->	A32	->	Handshake pin H4

All four User Interrupt inputs are buffered with Schmitt-Trigger devices 74LS14. The handshake pins H1-H4 can be programmed independently as either active high or active low.

Interrupt Scheme

The User Interrupts 2-5 are transmitted to the VMEbus through Interrupt Channel 1. This IRQ channel is assigned to Port Interrupt of PI/T 1 and is shared by the interrupts of the H1-H4 handshake inputs (PI/T 1).

The interrupt sources of PI/T 1 can be identified by the interrupt vector which is associated to the appropriate handshake pin.

The H4 handshake pin of PI/T 1 is connected to the PI/T 2 device on the PC5 pin, transmitting the User Interrupts 2-5. The PC5 pin of PI/T 2 is asserted if a User Interrupt 2-5 becomes active. A polling software routine has to find out which one of the User Interrupts 2-5 is requesting service.

16. The Timer Interrupt

The TIMER INTERRUPT function is performed by the timer module of the PI/T 1 device. This independent part of the PI/T contains a 24-bit-wide counter and a 5-bit prescaler.

The timer may generate periodic interrupts or a single interrupt after a programmable time period. It may be used as a watchdog timer or for elapsed time measurements. The timer is clocked by the 8MHz frequency of the PI/T clock input.

Interrupt generation is executed via the interrupt channel 2. The timer supports vectorized interrupt. Table 34 lists the associated registers and their addresses related to the default Board Base Address $B02000.

Table 34: TIMER Interrupt Channel Address Assignment

Interrupt Source	Interrupt Channel	Offset to Board Base Address		
		B I M 1 Control Register	Vector Register	PI/T 1 Timer Interrupt Vector Register
TIMER	2	$103	$10B	not used
	2	$103	not used	TIVR:$063

The programming example given in chapter 7 "Software Control" includes a subroutine which initializes the Timer to generate interrupts periodically using the interrupt vector stored in the Timer Interrupt Vector Register (TIVR).

17. The IEEE-488 GPIB Interface

(included only on the SYS68K/ASCU-2)

The SYS68K/ASCU-2 has a GPIB Interface (General Purpose Interface Bus) installed which conforms to the IEEE Standard 488-1978.

This interface allows the transference of data between the VMEbus and the GPIB, making it possible to control various remotely programmable test and measurement devices by a VMEbus system.

The IEEE-488 standard defines the GPIB structure as a 16 transmission line bus, consisting of 8 data lines, 3 handshake lines and 5 interface management lines.

The bus works with an asynchronous handshake protocol transferring the data in bit parallel, byte serial manner. Data and programming instructions can be transferred bidirectionally between the connected peripherals.

The devices connected to the GPIB can be classified into three groups: Talker, Listener and Controller. Some devices may perform a combination of the three functions such as Controller/Talker or Talker/Listener.

Figure 38 shows the bus structure of the GPIB and an example for the bus configuration and Figure 39 outlines the interface used on the SYS68K/ASCU-2.

Figure 38: GPIB Structure and Possible Bus Configurations

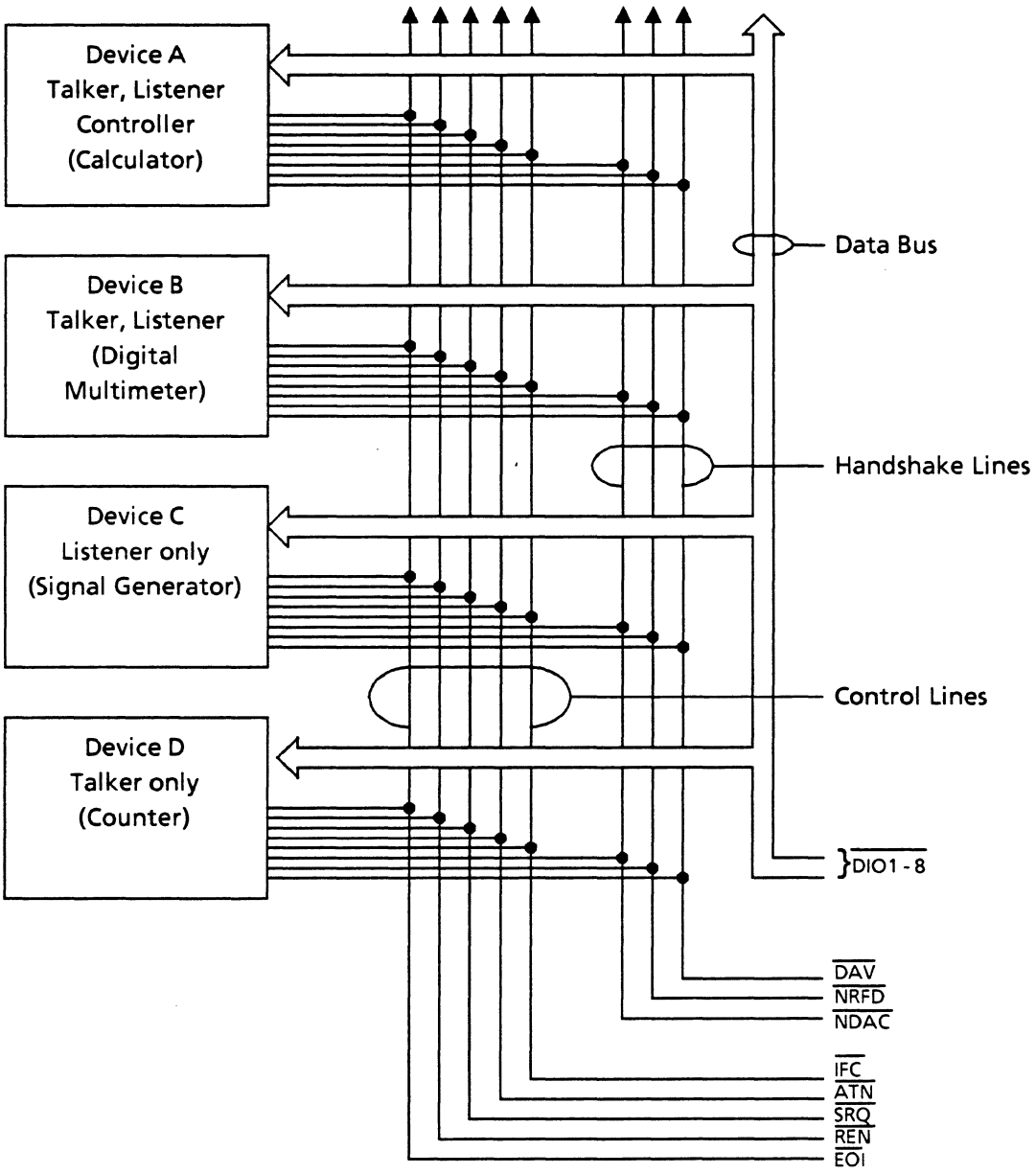
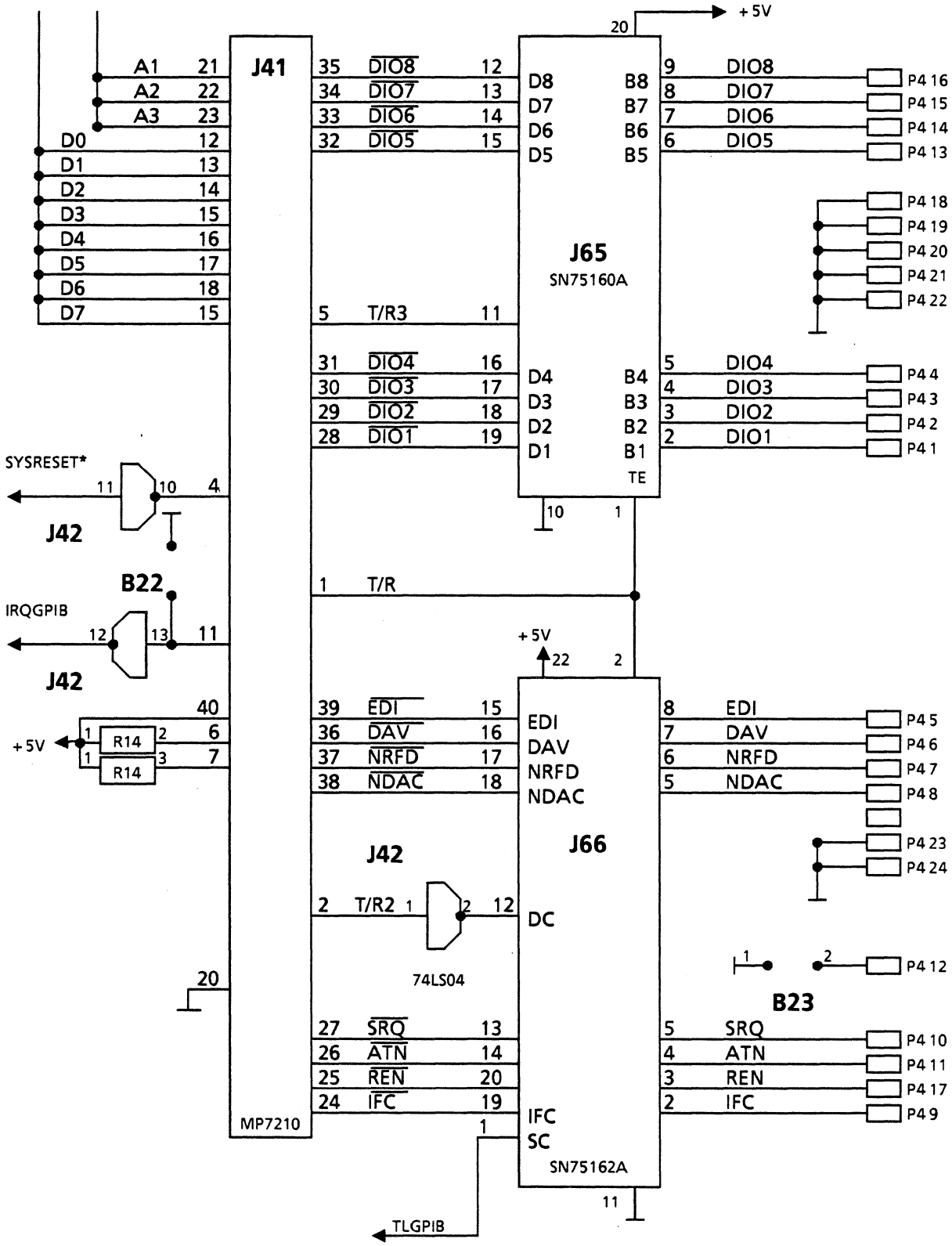


Figure 39: Hardware Schematics of the GPIB Interface



The GPIB interface implemented on the ASCU-2 has the functional interface capabilities listed in table 35. All capabilities have the complete option of the allowable subsets, defined in the IEEE-488 standard.

Table 35: GPIB Interface Capabilities

Capability Identification Code	Interface Function
SH 1	Source Handshake
AH 1	Accepter Handshake
T5, TE5	Talker, Extended Talker
L3, LE3	Listener, Extended Listener
SR 1	Service Request
RL	Relocate Local
PP1, PP2	Parallel Poll
DC 1	Device Clear
DT 1	Device Trigger
C1-C5	All Controller functions

17.1 Features of the NEC 7210

- Interface capability that meets IEEE Standard 488-1978

- Programmable Data Transfer Rate

- 16 accessible registers - 8 read / 8 write

- 2 Address Registers
  Detection of MTA, MLA, MSA
  Two device addresses

- EOS Message automatic detection

- Automatic command processing and undefined command read capability

- Programmable Bus Transceiver I/O Specification

- 1-8MHz clock range

- TTL compatible

17.2 Hardware Realization of the GPIB Interface

Full control of the General Purpose Interface Bus is provided by the Advanced Interface Controller Chip 7210. The device features all of the interface functions for Talker, Listener and Controller defined in the IEEE-488 standard.

The sixteen internal registers enable software control of all interface functions.

A detailed hardware schematics diagram of the interface is given in Figure 39.

The GPIB controller operates with a clock frequency of 8MHz. The T/R1, T/R2 and T/R3 lines are transceiver control lines whose operation is steered by software.

Two non-inverting Bus Driver/Receiver circuits (75160A, 75162A) attach the controller chip to the GPIB.

The transceivers meet all the requirements of the IEEE-488 specification and have a drive capacity of 48mA sink current. They can work with either open collector outputs or three state outputs. This allows high speed data transfer if the three state output mode is selected.

The SYSTEM CONTROL (SC) input of the 75162A device controls the direction for the REN and the IFC signals transmission independently.

The determination of the SC level is software programmable and is carried out by the PC6 pin of the PI/T 2.

When the interface functions as a controller, the REN and IFC signals must be driven to the GPIB I/O port. For this, the SC input has to be set to a logical 1. If the interface function is required to receive the REN and IFC signal from the GPIB, the SC input must be set to 0.

The default situation after reset is that PC6 as well as the SC input is on high level and the REN and IFC signals will be driven to the GPIB.

The T/L switch on the front panel provides a hardware selectable status signal which may be used to determine the direction of the REN and the IFC signal transmission. The T/L switch status is readable via pin PC7 of the PI/T 2 device.

Jumperfield B25 provides a jumper selectable 5-bit device address for the GPIB interface which is readable via the Port B of PI/T 2. An inserted jumper connecting the corresponding jumper pins provides a low level (0) at the port input and a removed jumper a high level (1).

Three input pins on Port B are spare for user applications. Table 36 lists the assignment of Port B pins to the jumperfield B25.

Table 36: GPIB Address Selection

	Jumperfield B25		
PI/T 2 Port B	Corresponding Pins	Default Jumper Settings	Comments
PBØ	1 - 16	IN	GPIB Address bit D1
PB1	2 - 15	IN	GPIB Address bit D2
PB2	3 - 14	IN	GPIB Address bit D3
PB3	4 - 13	IN	GPIB Address bit D4
PB4	5 - 12	IN	GPIB Address bit D5
PB5	6 - 11	OUT	spare
PB6	7 - 1Ø	OUT	spare
PB7	8 - 9	OUT	spare

The jumper B23 selects the connection of the cable shield to logic ground (inserted by default).

Figure 4Ø shows the pinout of the jumperfield B25 and Figure 41 the location of B25 and B23.

Figure 4Ø: Pin-Out of the Jumperfield B25

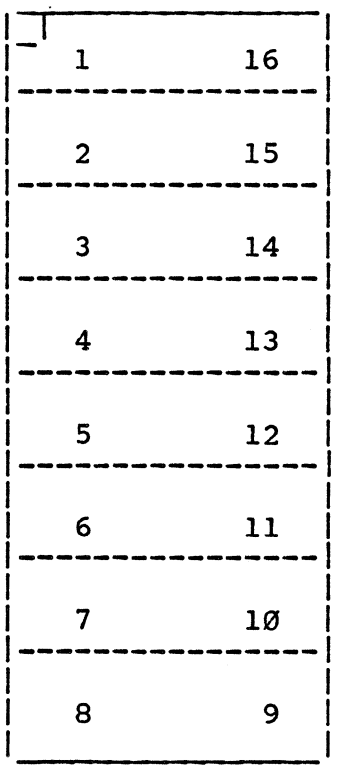
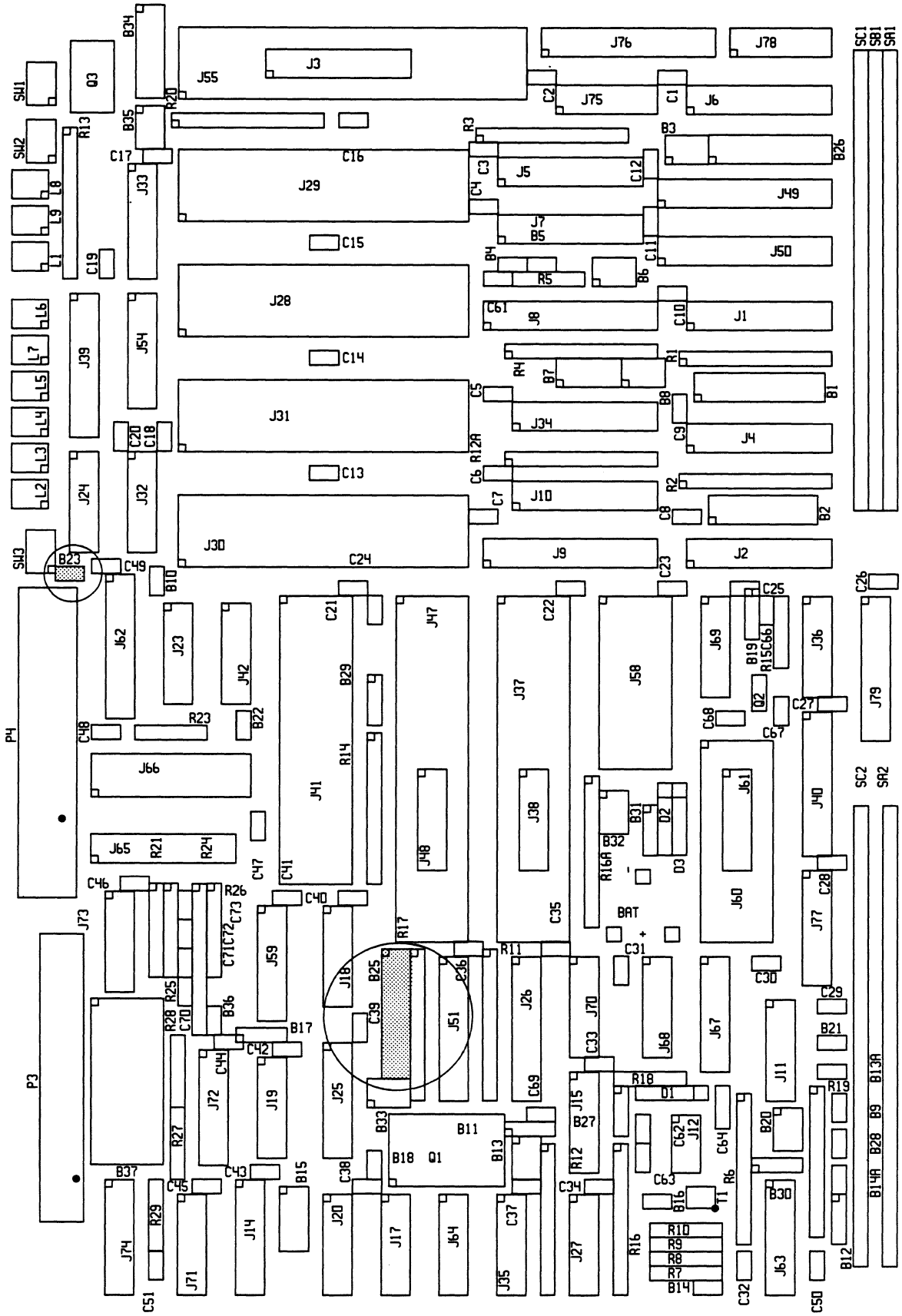


Figure 41: Location Diagram of the Jumperfields B23 and B25



The GPIB Interface I/O signals are available at the 24 pin microribbon connector located on the front panel. Table 37 shows the signal assignment of the connector.

Table 37: IEEE 488 Connector Pin Assignment

Contact	Signal Line	Contact	Signal Line
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EOI (24)	17	REN (24)
6	DAV	18	Gnd,(6)
7	NRFD	19	Gnd,(7)
8	NDAC	20	Gnd,(8)
9	IFC	21	Gnd,(9)
10	SRQ	22	Gnd,(10)
11	ATN	23	Gnd,(11)
12	SHIELD	24	Gnd,LOGIC

Note: Gnd,(n) refers to the signal ground return of the referenced contact. EOI and REN return on contact 24.

17.3 Addressing of the GPIB Controller

Communication between the system bus and the General Purpose Interface Bus is performed by the register set of the GPIB Controller. The sixteen internal registers - eight read registers and eight write registers - are directly addressable and used for data transfer and control of the interface functions. These registers occupy 8 consecutive byte locations. One location is shared by a read register and a write register.

The GPIB controller chip works on the lower data bus (DØ-7) and is therefore accessible only at odd addresses.

The access address of the first register under the default Board Base Address ($BØ2ØØØ) is $BØ2141. Table 38 lists the register address assignment of the GPIB controller.

Table 38: Register Table of the GPIB Controller

Default Address HEX	Register Offset	R/W	Description
Default Board Base Address: $BØ2ØØØ			
Device Offset:		$ 14Ø	
Read Registers			
BØ2141	Ø1	R	Data In
BØ2143	Ø3	R	Interrupt Status 1
BØ2145	Ø5	R	Interrupt Status 2
BØ2147	Ø7	R	Serial Poll Status
BØ2149	Ø9	R	Address Status
BØ214B	ØB	R	Command Pass Through
BØ214D	ØD	R	Address Ø
BØ214F	ØF	R	Address 1
Write Registers			
BØ2141	Ø1	W	Byte Out
BØ2143	Ø3	W	Interrupt Mask 1
BØ2145	Ø5	W	Interrupt Mask 2
BØ2147	Ø7	W	Serial Poll Mask
BØ2149	Ø9	W	Address Mode
BØ214B	ØB	W	Auxiliary Mode
BØ214D	ØD	W	Address Ø/1
BØ214F	ØF	W	End of String

17.4 The GPIB Interrupt Scheme

To provide a fully asynchronous system structure the GPIB controller is able to force an interrupt request on one level of the 7 VMEbus interrupt request lines. This is made possible by a Bus Interrupter Module (BIM 2) that transmits the interrupt request of the GPIB Controller to the VMEbus. The level on which an interrupt is requested is programmable by the BIM control register.

The BIM device will also supply the interrupt vector during an interrupt acknowledge cycle if it is programmed to do so.

Since the GPIB Controller has no interrupt vector, the BIM must be initialized to honour an acknowledge with the contents of its vector register.

The GPIB interrupt is performed via Interrupt Channel 8.

Table 39 shows the addresses of the assigned BIM registers.

Table 39: GPIB Controller Interrupt Channel Address Assignment

Interrupt Source	Interrupt Channel Number	Interrupter Device	Offset to Board Base Addr.	
			BIM Control Reg.	BIM Vector Reg.
GPIB Controller	8	BIM 2	$117	$11F

There are thirteen possible interrupt events which may cause the GPIB Controller to assert its interrupt request output. Each interrupt event has its own status bit and mask bit.

Providing that the interrupt mask bit enables an interrupt condition, the interrupt output of the controller gets active if this condition is met.

To ensure a correct interrupt generation by the GPIB controller device, its interrupt pin has to be active low. The active level of the interrupt pin is software selectable and can be specified to be active low by writing a logical 1 to bit 3 of the Auxiliary Register B.

Table 40 lists the possible events for the controllers interrupt execution.

Table 40: GPIB Interrupt Events

Interrupt Status Bit	Description
INT	OR of All Unmasked Interrupt Status Bits
CPT	Command Pass Through
APT	Address Pass Through
DET	Device Trigger
END	End (END or EOS Message Received)
DEC	Device Clear
ERR	Error
DO	Data Out
DI	Data In
SRQI	Service Request Input
LOKC	Lockout Change
REMC	Remote Change
ADSC	Address Status Change
CO	Command Output

17.5 Programming Example of the GPIB Controller

17.5. PROGRAMMING EXAMPLE

```
*************************************************************************
*       GPIB CONTROLLER 7210
*
*       Programming the Power Supply
*       Manufacturer:   FARNELL INSTRUMENTS LTD.
*       Type:           AP60/50
*
*       Set output voltage =>  4.5 V
*       Set current limit  =>  2.5 A
*
*       This program example initializes the uPD 7210 as CONTROLLER/
*       TALKER. After specifying the Talker (TA=0) and the Listener
*       (LA=1)  DATA is sent to the GPIB bus. The data stream sets the
*       output voltage of the Power Supply to 4.5 V and the current
*       limit to 2.5 A.
*-----------------------------------------------------------------------
*
*       DEFINITION OF WRITE REGISTERS
*
GPIB:   EQU     $B02140                 ;BASE ADDRESS OF GPIB CONTROLLER
BOUT:   EQU     GPIB+1                  ;BYTE OUT REGISTER
INTM1:  EQU     GPIB+3                  ;INTERRUPT MASK 1
INTM2:  EQU     GPIB+5                  ;INTERRUPT MASK 5
SPM:    EQU     GPIB+7                  ;SERIALPOLL MODE
ADRM:   EQU     GPIB+9                  ;ADDRESS MODE
AUXM:   EQU     GPIB+$B                 ;AUXILARY MODE
ADR01:  EQU     GPIB+$D                 ;ADDRESS 0/1
EOS:    EQU     GPIB+$F                 ;END OF STRING
*
*-----------------------------------------------------------------------
*       MAIN Routine
*
*       -initializes uPD 7210
*       -sends IFC (interface clear)
*       -calls send routine
*
        BSR     INIT
        MOVE.B  #$1E,AUXM               ;set IFC (interface clear)
        MOVE.B  #25,D1
IFCWAIT:SUBI.B  #1,D1                   ;wait 100us
        BNE.S   IFCWAIT
        MOVE.B  #$16,AUXM               ;clear IFC
        BSR     SEND
        XEXT                            ;Return to monitor
*-----------------------------------------------------------------------
*       INITIALIZATION
*
INIT:   MOVE.B  #$02,AUXM               ;AUX-C REGISTER;CHIP RESET
        MOVE.B  #$00,INTM1              ;DISABLE INTERRUPT MASK 1
        MOVE.B  #$00,INTM2              ;DISABLE INTERRUPT MASK 2
        MOVE.B  #$31,ADRM               ;ADDRESS-MODE 1;T/R MODE 3
*                                       ;75160/75162 DRIVERS
        MOVE.B  #$00,ADR01              ;My talker address = 0
*                                       ;in ADDRESS-0 REGISTER
        MOVE.B  #$E0,ADR01              ;DISABLE ADDRESS-1 REGISTER
        MOVE.B  #$04,EOS                ;CONTENT END OF STRING = <EOT>
        MOVE.B  #$AC,AUXM               ;AUX-B REGISTER:  HIGH SPEED TRANSFER
*                                       ;Tri-State-Driver;INT-Pin is activ low
        MOVE.B  #$28,AUXM               ;AUX-F REGISTER;NF = 8 MHz
        MOVE.B  #$9C,AUXM               ;AUX-A REGISTER;normal handshake mode,
*                                       ;8-bit word EOS
        MOVE.B  #$00,AUXM               ;AUX-C REGISTER: immediate execute
*                                       ;power on
        RTS                             ;END OF INITIALISATION
```

Programming Example cont'd

```
*-------------------------------------------------------------------
*
*       SEND ROUTINE
*
SEND:   MOVE.B  #$98,AUXM               ;AUX-A REGISTER: 8 bit EOS;normal
*                                       ;handshake mode;output EOI on EOS sent
        BSR     COCHECK                 ;CO Bit check
        MOVE.B  #$3F,BOUT               ;send UNLISTEN=$3F
        BSR     COCHECK
        MOVE.B  #$21,BOUT               ;send listener address Ø1
        BSR     COCHECK
        MOVE.B  #$4Ø,BOUT               ;send talker address $ØØ
        MOVE.B  #$1Ø,AUXM               ;local message; gts
*
*
        LEA.L   DATA(PC),AØ
        LEA.L   DATAE(PC),A1
@ØØ1Ø    BSR     DOCHECK
        MOVE.B  (AØ)+,BOUT
        CMPA.L  A1,AØ
        BNE.S   @ØØ1Ø
        RTS
*
*-------------------------------------------------------------------
*
COCHECK:MOVE.B  INTM2,DØ                ;CO bit check
        ANDI.B  #$Ø8,DØ
        BEQ.S   COCHECK
        RTS
*-------------------------------------------------------------------
*
DOCHECK:MOVE.B  INTM1,DØ                ;DO bit check
        ANDI.B  #$Ø6,DØ
        BEQ.S   DOCHECK
        ANDI.B  #$Ø4,DØ                 ;ERROR bit check
        BNE     ERROR
        RTS
*-------------------------------------------------------------------
*
DATA    DC.B    'VØ45 IØ25 S',$ØD,$ØA,$Ø4,'Ø'   ;DATA sent to the GPIB
DATAE   DC.B '0'
        EVEN
*-------------------------------------------------------------------
ERROR:  XRDM                                    ;individual error routine
        XPMC ERRMSG
        XEXT
*
ERRMSG  DC.B $ØD,$ØA,'DOCHECK FAILED',$ØD,$ØA,Ø
        EVEN
```

18. Software Programmable Interrupts

The SYS68K/ASCU-2 contains 4 Bus Interrupter Modules (BIM 68153). Two BIMs can be used to generate software triggered interrupts to the VMEbus. The second PI/T device on the ASCU-2 is used to drive the interrupt inputs of the two BIMs (J3Ø, J31).

Therefore, multiprocessor intercommunication is performed because every processor board on the VMEbus may send an interrupt to any other processor board.

The level and the interrupt vector of each interrupt channel (8 channels are implemented) are software programmable through the BIM. Therefore, processor A (which handles IRQs from the VMEbus on level 1-4) can send an interrupt to processor B (which handles IRQs from level 5-7) on level 5, 6 or 7, and processor B can send an interrupt to processor A on level 1, 2, 3 or 4. A maximum of 7 different assignments for processor intercommunication are possible through the 7 VMEbus IRQs. If more than 7 processor boards are installed a special software handling of each IRQ level must be performed.

The assignment of the channels to the IRQ level is fully under software control to allow a dynamic change of the IRQ assignments in the used operating system.

Table 41 lists the assignment of each interrupt channel to the interrupt trigger (port A of the 2nd PI/T).

Table 41: The Software Programmable Interrupts of the SYS68K/ASCU-2

PI/T2 (J47) Port A	Interrupter Device	Interrupt Channel Number	Offset to Board Base Address	
			BIM Control Register	BIM Vector Register
PA Ø	BIM 3	9	$121	$129
PA 1	BIM 3	1Ø	$123	$12B
PA 2	BIM 3	11	$125	$12D
PA 3	BIM 3	12	$127	$12F
PA 4	BIM 4	13	$131	$139
PA 5	BIM 4	14	$133	$13B
PA 6	BIM 4	15	$135	$13D
PA 7	BIM 4	16	$137	$13F

Caution: If more than one processor is used in the VMEbus environment, a read modify write cycle to a common available memory (8 bit wide) must be used to avoid the problem that the bus mastership changes during the SEND routine (A or B). In this case the read data may be wrong because the following changes may occur:

1) Processor A reads data on Port A of PI/T 2 (J47).
   Data: 1111 1111

2) Bus mastership changes.

3) Processor Ø reads data on Port A of PI/T 2 (J47).
   Data: 1111 1111

4) Processor writes modified data into Port A of PI/T J47.
   Data: 11Ø1 1111

5) Bus mastership changes.

6) Data at PI/T 2 (J47).
   Data 11Ø1 1111

7) Processor B writes modified data into Port A of PI/T 2 (J47).
   Data 1Ø11 1111

This failure (change of bus mastership on points 2 and 5) is avoided if the Read Modify Write intercommunication is used. The correct data stored in PI/T 2 (J47) would then be:
Data: 1ØØ1 1111

A programming example for the Software Programmable Interrupts is given at the end of chapter 7 "Software Control".

19. The BCLR* Timing Function

The BCLR* Timing Function is performed by the Parallel Interface/Timer Module PI/T 2 (J47) and is available only on the SYS68K/ASCU-2 board.

The BCLR* Timing Function has associated five pins of the PI/T 2 device: PCØ, PC1, PC4,
PC2/TIN, PC3/TOUT

The PCØ, PC1 and PC4 pins belong to the Parallel Interface Module of PI/T 2 and are used to select the different BCLR* generation modes provided by the board. These BCLR* generation modes are listed in chapters 1Ø.1, 1Ø.2 and 1Ø.3 depending on the arbitration type, PRI, RRS or PRR.

The PC2/TIN pin and the PC3/TOUT pin are double function pins, applied to the Timer Module of the PI/T 2 device. After reset all pins function as input pins carrying high level. The default condition for the BCLR* generation is that BCLR* is asserted if a Bus Request on level 3 is pending. (Arbiter function is the PRR arbitration type. See Table 44.)

19.1 BCLR* Signal Generation Structure

The SYS68K/ASCU-2 has two sources which may generate the BCLR* bus signal. It is generated either by the on-board BUS ARBITER (ABCLR* signal) or by the BCLR*-Timer (TOUTBCLR* signal). The two signals are gated by a PAL device (J51) and can be mixed for various generation modes.

The generation of the BCLR* bus signal depends on the following setup:

- the arbitration type of the arbiter,
- the BCLR* generation mode (selected by PCØ, PC1, PC4),
- the BCLR-Timer configuration.

19.2 The BCLR*-Timer

The additional BCLR-Timer of the SYS68K/ASCU-2 can be configured to operate in several modes providing a flexible BCLR* bus signal generation. The BCLR-Timer is assigned to the two double function pins PC2/TIN and PC3/TOUT.

The function of the pins is software selectable by the Timer Control Register (TCR) which also determines all other operations of the BCLR-Timer. Please refer to the timer description of the PI/T Data Sheet to select its programmable options and capabilities.

When the BCLR-Timer is selected to operate, the dual function pins work as TOUT and TIN. The TOUT pin is an output and provides the TOUTBCLR signal. The TIN pin operates as a trigger input and can be used to enable the watchdog timer which allows the generation of a BCLR* if a programmed time is over.

This mode allows all bus masters to transfer their data for a minimum time before the Bus Clear is generated (arbitration time overheads are reduced).

The counter operates as a retriggerable multivibrator with a software programmable timeout. An internal trigger/retrigger/preset signal starts the PI/T watchdog counter every time the arbiter has granted the bus to a bus master.

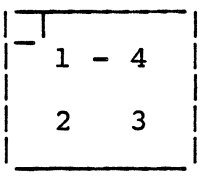
If the PC2/PC3 pin function is selected, (port C function), the PC2 pin must not be programmed to be output. This may damage the circuitry.

The default condition of these pins after reset is that they function as input and carry high level.

Table 42: BCLR* Generation Modes in the PRI Arbitration Type

B33

B33 Jumper setting for PRI mode: Connected pins 1-4

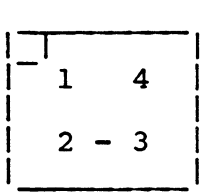


BCLR* driven to the bus if B5 inserted.

Software Control PI/T 2 Port C Pins			Description of BCLR* Generation Modes
PCØ	PC1	PC4	BCLR* is asserted if
1	1	1	Higher prioritized Bus Request is pending
Ø	Ø	1	The Bus Clear Timer asserts its output
1	Ø	1	Higher prioritized Bus Request is pending or The Bus Clear Timer asserts its output
Ø	1	Ø	Higher prioritized Bus Request is pending and The Bus Clear Timer asserts its output
Ø	Ø	Ø	never
Ø	1	1	not allowed
1	Ø	Ø	not allowed
1	1	Ø	not allowed

Table 43: BCLR* Generation Modes in the RRS Arbitration Type

B33 Jumper setting for RRS mode: Connected pins 2-3

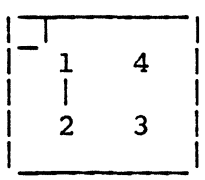


BCLR* driven to the bus if B5 inserted.

Software Control PI/T 2 Port C Pins			Description of BCLR* Generation Modes
PCØ	PC1	PC4	BCLR* is asserted if
1	1	1	Any Bus Request is pending
Ø	Ø	1	The Bus Clear Timer asserts its output
1	Ø	1	Any Bus Request is pending or The Bus Clear Timer asserts its output
Ø	1	Ø	Any Bus Request is pending and The Bus Clear Timer asserts its output
Ø	Ø	Ø	never
Ø	1	1	not allowed
1	Ø	Ø	not allowed
1	1	Ø	not allowed

Table 44: BCLR* Generation Modes in the PRR Arbitration Type

B33 Jumper setting for PRR mode: Connected pins 1-2



BCLR* driven to the bus if B5 inserted.

Software Control PI/T 2 Port C Pins			Description of BCLR* Generation Modes
			BCLR* is asserted if
PCØ	PC1	PC4	
1	1	1	A Bus Request on level 3 is pending *
Ø	Ø	1	The Bus Clear Timer asserts its output
1	Ø	1	A Bus Request on level 3 is pending or The Bus Clear Timer asserts its output
Ø	1	Ø	A Bus Request on level 3 is pending and The Bus Clear Timer asserts its output
Ø	Ø	Ø	never
Ø	1	1	not allowed
1	Ø	Ø	not allowed
1	1	Ø	not allowed

* Default BCLR Generation

20. Board Register Summary

The SYS68K/ASCU-1 contains the following devices:

- Multi Protocol Serial I/O	(J55)	MPCC	68561
- Parallel Interface/Timer 1	(J37)	PI/T 1	68230
- Real Time Clock	(J58)	RTC	58167A
- Bus Interrupter Module 1	(J28)	BIM 1	68153
- Bus Interrupter Module 2	(J29)	BIM 2	68153

The SYS68K/ASCU-2 contains all the devices of the ASCU-1 and the following additional devices:

- Parallel Interface/Timer 2	(J47)	PI/T 2	68230
- Bus Interrupter Module 3	(J30)	BIM 3	68153
- Bus Interrupter Module 4	(J31)	BIM 4	68153
- IEEE-488 GPIB Controller	(J41)	GPIB-C	7210

On the SYS68K/ASCU-2 all I/O devices and the 4 BIM devices reside in a contiguous memory map. The different I/O functions are described in chapters 3 to 19.

All device registers of the board are directly addressable.

Read, write and read-modify-write accesses are possible.

An overview of the addressing of the board devices is given below:

Device	Offset to Board Base Address	Access Mode	Usable Data Bits
MPCC	$000	Byte, Word	D0-D7 or D0-D15
PI/T 1	$040	Byte	D0-D7
PI/T 2	$080	Byte	D0-D7
RTC	$0C0	Byte	D0-D7
BIM 1	$100	Byte	D0-D7
BIM 2	$110	Byte	D0-D7
BIM 3	$120	Byte	D0-D7
BIM 4	$130	Byte	D0-D7
GPIB-C	$140	Byte	D0-D7

MPCC Summary

Default Board Base Address	$BØ2ØØØ
Relative Offset to the Board Base Address	$ ØØØ
Default Access Address	$BØ2ØØ1 - $BØ2Ø3F (Byte Mode) $BØ2Ø2Ø - $BØ2Ø3F (Word Mode)
Access Mode	Byte Mode (default) Word Mode
Usable Data Bits	DØ-D7 Byte Mode (default) DØ-D15 Word Mode
Interrupt Capabilities	3 software programmable interrupt vectors. Interrupt generation via Channel 7.

Table 45: The MPCC Address Map in the Byte Mode of Addressing

Default Board Base Address: $B02000
Device Offset: $ 000

Default Addr.HEX	Regis. Offset	Reset Value	Label	Description
B02001	01	00	MPCRSR	Receiver Status Register
B02003	03	--	MPCRDR	Receiver Data Register
B02005	05	0F	MPCRIVNR	Receiver Interrupt Vector Number Register
B02009	09	80	MPCTSR	Transmitter Status Register
B0200B	0B	--	MPCTDR	Transmitter Data Register
B0200D	0D	0F	MPCTIVNR	Transmitter Interrupt Vector Number Register
B02011	11	00	MPCSISR	Serial Interface Status Reg.
B02015	15	0F	MPCSIVNR	Serial Interrupt Vector Number Register
B02019	19	00	MPCPSR1	Protocol Select Register 1
B0201B	1B	00	MPCAR1	Address Register 1
B0201D	1D	01	MPCBRDR1	Baud Rate Divider 1
B0201F	1F	00	MPCCCR	Clock Control Register
B02021	21	01	MPCRCR	Receiver Control Register
B02025	25	00	MPCRIER	Receiver Interrupt Enable Reg.
B02029	29	01	MPCTCR	Transmitter Control Register
B0202D	2D	00	MPCTIER	Transmitter Interrupt Enable Register
B02031	31	00	MPCSICR	Serial Interface Control Reg.
B02035	35	00	MPCSIER	Serial Interrupt Enable Reg.
B02039	39	00	MPCPSR2	Protocol Select Register 2
B0203B	3B	00	MPCAR2	Address Register 2
B0203D	3D	00	MPCBRDR2	Baud Rate Divider 2
B0203F	3F	04	MPCECR	Error Control Register

Table 46: The MPCC Address Map in the Word Mode of Addressing

Default Board Base Address : $BØ2ØØØ
Device Offset : $ ØØØ only word accesses allowed

Default Addr.HEX	Regis. Offset	Reset Value	Label	Description
BØ2Ø2Ø	2Ø	Ø1	MPCRCR	Receiver Control Register
BØ2Ø21	21	ØØ	MPCRSR	Receiver Status Register
BØ2Ø22	22	--	MPCRDR	Receiver Data Register
BØ2Ø23	23	--		
BØ2Ø24	24	ØØ	MPCRIER	Receiver Interrupt Enable Reg
BØ2Ø25	25	ØF	MPCRIVNR	Receiver Int. Vector No. Reg
BØ2Ø28	28	Ø1	MPCTCR	Transmitter Control Register
BØ2Ø29	29	8Ø	MPCTSR	Transmitter Status Register
BØ2Ø2A	2A	--	MPCTDR	Transmitter Data Register
BØ2Ø2B	2B	--		
BØ2Ø2C	2C	ØØ	MPCTIER	Transmitter Int. Enable Reg
BØ2Ø2D	2D	ØF	MPCTIVNR	Trans. Int. Vector No. Reg
BØ2Ø3Ø	3Ø	ØØ	MPCSICR	Serial Interface Control Reg
BØ2Ø31	31	ØØ	MPCSISR	Serial Interface Status Reg
BØ2Ø34	34	ØØ	MPCSIER	Serial Interrupt Enable Reg
BØ2Ø35	35	ØF	MPCSIVNR	Serial Int. Vector No. Reg
BØ2Ø38	38	ØØ	MPCPSR2	Protocol Select Register 2
BØ2Ø39	39	ØØ	MPCPSR1	Protocol Select Register 1
BØ2Ø3A	3A	ØØ	MPCAR2	Address Register 2
BØ2Ø3B	3B	ØØ	MPCAR1	Address Register 1
BØ2Ø3C	3C	ØØ	MPCBRDR2	Baud Rate Divider Register 2
BØ2Ø3D	3D	Ø1	MPCBRDR1	Baud Rate Divider Register 1
BØ2Ø3E	3E	Ø4	MPCECR	Error Control Register
BØ2Ø3F	3F	ØØ	MPCCCR	Clock Control Register

PI/T 1 Summary

Default Board Base Address	$B02000
Relative Offset to the Board Base Address	$ 040
Default Access Address	$B02041 - $B0207F
Access Mode	Byte Mode (odd only)
Usable Data Bits	D0-D7
Interrupt Capabilities	Parallel Interface: 4 vectors Vector Address: $B0204B (PIVR) Interrupt generation via Channel 1. Timer: 1 vector Vector Address: $B02063 (TIVR) Interrupt generation via Channel 2.

Table 47: The PI/T 1 Address Map

Default Board Base Address: $B02000
Device Offset: $ 040

Default Address HEX	Regis. Offset	Reset Value	Label	Description
B02041	01	00	PITPGCR	Port General Control Register
B02043	03	00	PITPSRR	Port Service Request Register
B02045	05	00	PITPADDR	Port A Data Direction Register
B02047	07	00	PITPBDDR	Port B Data Direction Register
B02049	09	00	PITPCDDR	Port C Data Direction Register
B0204B	0B	0F	PITPIVR	Port Interrupt Vector Register
B0204D	0D	00	PITPACR	Port A Control Register
B0204F	0F	00	PITPBCR	Port B Control Register
B02051	11	--	PITPADR	Port A Data Register
B02053	13	--	PITPBDR	Port B Data Register
B02055	15	--	PITPAAR	Port A Alternate Register
B02057	17	--	PITPBAR	Port B Alternate Register
B02059	19	--	PITPCDR	Port C Data Register
B0205B	1B	--	PITPSR	Port Status Register
B02061	21	00	PITTCR	Timer Control Register
B02063	23	0F	PITTIVR	Timer Interrupt Vector Reg.
B02065	25	--	PITCPR	Counter Preload Register
B02067	27	--		
B02069	29	--		
B0206B	2B	--		
B0206D	2D	--	PITCNTR	Count Register
B0206F	2F	--		
B02071	31	--		
B02073	33	--		
B02075	35	00	PITTSR	Timer Status Register

PI/T 2 Summary

Default Board Base Address	$B02000
Relative Offset to the Board Base Address	$ 080
Default Access Address	$B02081 - $B020BF
Access Mode	Byte Mode (odd only)
Usable Data Bits	D0-D7
Interrupt Capabilities	Parallel Interface Interrupt via PI/T 1 Vector Address: $B0208B (PIVR) Timer: not Interrupt capable

Table 48: The PI/T 2 Address Map

Default Board Base Address: $BØ2ØØØ
Device Offset: $ Ø8Ø

Default Address HEX	Regis. Offset	Reset Value	Label	Description
BØ2Ø81	Ø1	ØØ	PITPGCR	Port General Control Register
BØ2Ø83	Ø3	ØØ	PITPSRR	Port Service Request Register
BØ2Ø85	Ø5	ØØ	PITPADDR	Port A Data Direction Register
BØ2Ø87	Ø7	ØØ	PITPBDDR	Port B Data Direction Register
BØ2Ø89	Ø9	ØØ	PITPCDDR	Port C Data Direction Register
BØ208B	ØB	ØF	PITPIVR	Port Interrupt Vector Register
BØ208D	ØD	ØØ	PITPACR	Port A Control Register
BØ208F	ØF	ØØ	PITPBCR	Port B Control Register
BØ2Ø91	11	--	PITPADR	Port A Data Register
BØ2Ø93	13	--	PITPBDR	Port B Data Register
BØ2Ø95	15	--	PITPAAR	Port A Alternate Register
BØ2Ø97	17	--	PITPBAR	Port B Alternate Register
BØ2Ø99	19	--	PITPCDR	Port C Data Register
BØ209B	1B	--	PITPSR	Port Status Register
BØ2ØA1	21	ØØ	PITTCR	Timer Control Register
BØ2ØA3	23	ØF	PITTIVR	Timer Interrupt Vector Reg.
BØ2ØA5	25	--	PITCPR	Counter Preload Register
BØ2ØA7	27	--		
BØ2ØA9	29	--		
BØ2ØAB	2B	--		
BØ2ØAD	2D	--	PITCNTR	Count Register
BØ2ØAF	2F	--		
BØ2ØB1	31	--		
BØ2ØB3	33	--		
BØ2ØB5	35	ØØ	PITTSR	Timer Status Register

RTC Summary

Default Board Base Address	$BØ2ØØØ
Relative Offset to the Board Base Address	$ ØCØ
Default Access Address	$BØ2ØC1 - $BØ2ØFF
Access Mode	Byte Mode (odd only)
Usable Data Bits	DØ-D7
Interrupt Capabilities	No Interrupt Vector Interrupt generation via Channel 6

Table 49: The RTC Address Map

Default Board Base Address: $BØ2ØØØ
Device Offset: $ ØCØ

Default Address HEX	Register Offset	Reset Value	Label	Description
BØ2ØC1	Ø1	--	RTCCTTS	Counter - ten thousands of secs
BØ2ØC3	Ø3	--	RTCCHTS	Counter - hundredths + tenths of secs
BØ2ØC5	Ø5	--	RTCCSEC	Counter - seconds
BØ2ØC7	Ø7	--	RTCCMIN	Counter - minutes
BØ2ØC9	Ø9	--	RTCCHRS	Counter - hours
BØ2ØCB	ØB	--	RTCCDOW	Counter - day of week
BØ2ØCD	ØD	--	RTCCDOM	Counter - day of month
BØ2ØCF	ØF	--	RTCCMON	Counter - month
BØ2ØDØ	1Ø	--	RTCRTTS	RAM - ten thousandths of secs
BØ2ØD3	13	--	RTCRHTS	RAM - hundredths + tenths of secs
BØ2ØD5	15	--	RTCRSEC	RAM - seconds
BØ2ØD7	17	--	RTCRMIN	RAM - minutes
BØ2ØD9	19	--	RTCRHRS	RAM - hours
BØ2ØDB	1B	--	RTCRDOW	RAM - day of week
BØ2ØDD	1D	--	RTCRDOM	RAM - day of month
BØ2ØDF	1F	--	RTCRMON	RAM - month
BØ2ØE1	21	--	RTCISR	Interrupt Status Register
BØ2ØE3	23	--	RTCICR	Interrupt Control Register
BØ2ØE5	25	--	RTCCRES	Counters reset
BØ2ØE7	27	--	RTCRRES	RAM reset
BØ2ØE9	29	--	RTCSTAT	Status bit
BØ2ØEB	2B	--	RTCGO	GO command
BØ2ØED	2D	--	RTCSINT	Standby interrupt
BØ2ØFF	3F	--	RTCTEST	Test mode

GPIB-Controller Summary

Default Board Base Address	$B02000
Relative Offset to the Board Base Address	$000140
Default Access Address	$B02141 - $B0214F
Access Mode	Byte Mode (odd only)
Usable Data Bits	D0-D7
Interrupt Capabilities	No Interrupt Vector Interrupt generation via Channel 8

Table 50: The GPIB-Controller Address Map

Default Address HEX	Register Offset	R/W	Description
Default Board Base Address: $B02000			
Device Offset:			$ 140
Read Registers			
B02141	01	R	Data In
B02143	03	R	Interrupt Status 1
B02145	05	R	Interrupt Status 2
B02147	07	R	Serial Poll Status
B02149	09	R	Address Status
B0214B	0B	R	Command Pass Through
B0214D	0D	R	Address 0
B0214F	0F	R	Address 1
Write Registers			
B02141	01	W	Byte Out
B02143	03	W	Interrupt Mask 1
B02145	05	W	Interrupt Mask 2
B02147	07	W	Serial Poll Mask
B02149	09	W	Address Mode
B0214B	0B	W	Auxiliary Mode
B0214D	0D	W	Address 0/1
B0214F	0F	W	End of String

BIM 1 Summary

Default Board Base Address	$BØ2ØØØ
Relative Offset to the Board Base Address	$ØØØ1ØØ
Default Access Address	$BØ21Ø1 - $BØ21ØF
Access Mode	Byte Mode (odd only)
Usable Data Bits	DØ-D7
Assigned Interrupt Channels	No. 1 Parallel Interface (PIRQ) No. 2 Timer (TIRQ) No. 3 ACFAIL No. 4 SYSFAIL

Table 51: Register Table of the BIM 1

Default Board Base Address: $BØ2ØØØ
Device Offset: $ 1ØØ

Default Address HEX	Register Offset	Reset Value	Label	Description
BØ21Ø1	Ø1	ØØ	BIMCR1	Control Register 1
BØ21Ø3	Ø3	ØØ	BIMCR2	Control Register 2
BØ21Ø5	Ø5	ØØ	BIMCR3	Control Register 3
BØ21Ø7	Ø7	ØØ	BIMCR4	Control Register 4
BØ21Ø9	Ø9	ØF	BIMVR1	Vector Register 1
BØ21ØB	ØB	ØF	BIMVR2	Vector Register 2
BØ21ØD	ØD	ØF	BIMVR3	Vector Register 3
BØ21ØF	ØF	ØF	BIMVR4	Vector Register 4

BIM 2 Summary

Default Board Base Address	$B02000
Relative Offset to the Board Base Address	$000110
Default Access Address	$B02111 - $B0211F
Access Mode	Byte Mode (odd only)
Usable Data Bits	D0-D7
Assigned Interrupt Channels	No. 5 Test IRQ No. 6 RTC No. 7 MPCC No. 8 GPIB-C

Table 52: Register Table of the BIM 2

Default Board Base Address: $B02000
Device Offset: $ 110

Default Address HEX	Register Offset	Reset Value	Label	Description
B02111	01	00	BIMCR1	Control Register 1
B02113	03	00	BIMCR2	Control Register 2
B02115	05	00	BIMCR3	Control Register 3
B02117	07	00	BIMCR4	Control Register 4
B02119	09	0F	BIMVR1	Vector Register 1
B0211B	0B	0F	BIMVR2	Vector Register 2
B0211D	0D	0F	BIMVR3	Vector Register 3
B0211F	0F	0F	BIMVR4	Vector Register 4

BIM 3 Summary

Default Board Base Address	$BØ2ØØØ
Relative Offset to the Board Base Address	$ØØØ12Ø
Default Access Address	$BØ2124 - $BØ212F
Access Mode	Byte Mode (odd only)
Usable Data Bits	DØ-D7
Assigned Interrupt Channels	No. 9 PAØ No. 1Ø PA1 No. 11 PA2 No. 12 PA3

Table 53: Register Table of the BIM 3

Default Board Base Address: $BØ2ØØØ
Device Offset: $ 12Ø

Default Address HEX	Register Offset	Reset Value	Label	Description
BØ2121	Ø1	ØØ	BIMCR1	Control Register 1
BØ2123	Ø3	ØØ	BIMCR2	Control Register 2
BØ2125	Ø5	ØØ	BIMCR3	Control Register 3
BØ2127	Ø7	ØØ	BIMCR4	Control Register 4
BØ2129	Ø9	FF	BIMVR1	Vector Register 1
BØ212B	ØB	FF	BIMVR2	Vector Register 2
BØ212D	ØD	FF	BIMVR3	Vector Register 3
BØ212F	ØF	FF	BIMVR4	Vector Register 4

BIM 4 Summary

Default Board Base Address	$BØ2ØØØ
Relative Offset to the Board Base Address	$ØØØ13Ø
Default Access Address	$BØ2131 - $BØ213F
Access Mode	Byte Mode (odd only)
Usable Data Bits	DØ-D7
Assigned Interrupt Channels	No. 13 PA4 No. 14 PA5 No. 15 PA6 No. 16 PA7

Table 54: Register Table of the BIM 4

Default Board Base Address: $BØ2ØØØ
Device Offset: $ 131

Default Address HEX	Register Offset	Reset Value	Label	Description
BØ2131	Ø1	ØØ	BIMCR1	Control Register 1
BØ2133	Ø3	ØØ	BIMCR2	Control Register 2
BØ2135	Ø5	ØØ	BIMCR3	Control Register 3
BØ2137	Ø7	ØØ	BIMCR4	Control Register 4
BØ2139	Ø9	FF	BIMVR1	Vector Register 1
BØ213B	ØB	FF	BIMVR2	Vector Register 2
BØ213D	ØD	FF	BIMVR3	Vector Register 3
BØ213F	ØF	FF	BIMVR4	Vector Register 4

Table 55: Interrupt Channel Addressing

Device	Interrupt Channel Number	Offset to Board Base Address		Interrupt Source	Interrupt Vector Source	Address Offset of the Vector Source
		BIM Control Register	BIM Vector Register			
BIM 1 (J28)	1	$1Ø1	$1Ø9 (1)	Port Interrupt of PI/T 1 (J37)	PIVR :	$04B
	2	$1Ø3	$1ØB (1)	Timer Interrupt of PI/T 1 (J37)	TIVR :	$063
	3	$1Ø5	$1ØD	ACFAIL*	BIM 1 :	$1ØD
	4	$1Ø7	$1ØF	SYSFAIL*	BIM 1 :	$1ØF
BIM 2 (J29)	5	$111	$119	Test Interrupt	BIM 2 :	$119
	6	$113	$11B	Real Time Clock	BIM 2 :	$11B
	7	$115	$11D (2)	MPCC		Byte mode / Word mode
					RIVNR :	$ØØ5 / $Ø25
					TIVNR :	$ØØD / $Ø2D
					SIVNR :	$Ø15 / $Ø35
	8	$117	$11F	IEEE-GPIB Controller	BIM 2 :	$11F
BIM 3 (J3Ø)	9	$121	$129	PAØ : PI/T 2 (J47)	BIM 3 :	$129
	1Ø	$123	$12B	PA1 : PI/T 2 (J47)	BIM 3 :	$12B
(ASCU-2 only)	11	$125	$12D	PA2 : PI/T 2 (J47)	BIM 3 :	$12D
	12	$127	$12F	PA3 : PI/T 2 (J47)	BIM 3 :	$12F
BIM 4 (J31)	13	$131	$139	PA4 : PI/T 2 (J47)	BIM 4 :	$139
	14	$133	$13B	PA5 : PI/T 2 (J47)	BIM 4 :	$13B
(ASCU-2 only)	15	$135	$13D	PA6 : PI/T 2 (J47)	BIM 4 :	$13D
	16	$137	$13F	PA7 : PI/T 2 (J47)	BIM 4 :	$13F

(1) It is possible to let the BIM vector register supply the interrupt vector. In most cases it is better to prefer the interrupt vectors supplied by the interrupt source devices.

(2) BIM must not be programmed to supply vector, because the vector will be supplied by the Interrupt Source device.

21. General Information

The board is configured as SYSTEM CONTROLLER and has to be installed in slot 1 of a VMEbus system.

The following configuration is made during manufacturing:

The SYSCLOCK DRIVER module is enabled and drives the SYSCLK* bus line. (Ensure that other system boards do not drive the SYSCLK* bus line!)

The 4-level BUS ARBITER is enabled and drives the Bus Grant out lines BGØOUT-BG3OUT as well as the Bus Clear line BCLR*.

The BUS TIMER is disabled after Rest and Power-up.

The board drives and receives the SYSRESET* bus signal line.

The SYSFAIL* signal and the ACFAIL* signal are received by the board.

The Board Base Address is selected as $BØ2ØØØ.

22. Installation

Please read the complete manual for easy and correct board handling. Install the board in slot 1 of a VMEbus environment.

Use power supply with sufficient drive capacity.

After power-on the red RESET LED should turn off after approximately half a second and the green BCLR LED turns on. Now normal access can be forced to the default set address range of the devices.

Note: If the SYS68K/ASCU-1/2 is not to be used as System Controller and is not plugged into slot 1, the 4-level Bus ARBITER and the SYSCLOCK Driver must be disabled before the board is installed.

Caution: Please follow manufacturer's instructions for use and trouble shooting.

APPENDIX A

Specification of the SYS68K/ASCU-1/2

Description	ASCU-1	ASCU-2
IEEE488 (GPIB) Interface	-	x
Serial I/O Interface RS422	x	x
RS232	x	x
Centronics Parallel Interface	x	x
Real Time Clock	x	x
Battery Backup	x	x
SW-Programmable Bus Timer (2 to 12000us)	x	x
ACFAIL Handling	x	x
SYSFAIL Handling	x	x
TEST/RESET Switches	x	x
IACK Daisy Chain Driver	x	x
Interrupts to Priority Interrupt Bus	7	16
SW-Programmable Interrupts	-	8
User Interrupts on P2	1	5
RORA/ROAK Interrupt Release	x	x
4 Level Bus Arbiter	x	x
SW-Programmable Time for Bus Mastership	-	x
Address Selection A24:D16 / A16:D16	x	x
Power Requirements +5V (max)	2.5A	2.9A
+12V (max)	200mA	200mA
-12V (max)	200mA	200mA
Operating Temperature 0 to 60 degrees C	x	x
Storage Temperature -55 to +85 degrees C	x	x
Relative Humidity 0 - 95% (non-condensing)	x	x
Dimensions Double Eurocard 233x160mm (9.2x6.3")	x	x

APPENDIX B

Address Assignment of the SYS68K/ASCU-1/2 Devices

The devices are accessible only on odd addresses!

Start Address	End Address	Devices	
$B02001	$B0203F	MPCC 68561	
$B02041	$B0207F	PI/T 1 68230	
$B02081	$B020BF	PI/T 2 68230	*
$B020C1	$B020FF	RTC 58167A	
$B02101	$B0210F	BIM 1 68153	
$B02111	$B0211F	BIM 2 68153	
$B02121	$B0212F	BIM 3 68153	*
$B02131	$B0213F	BIM 4 68153	*
$B02141	$B0214F	GPIB CONTROLLER 7210	*

* included only on the SYS68K/ASCU-2

APPENDIX C

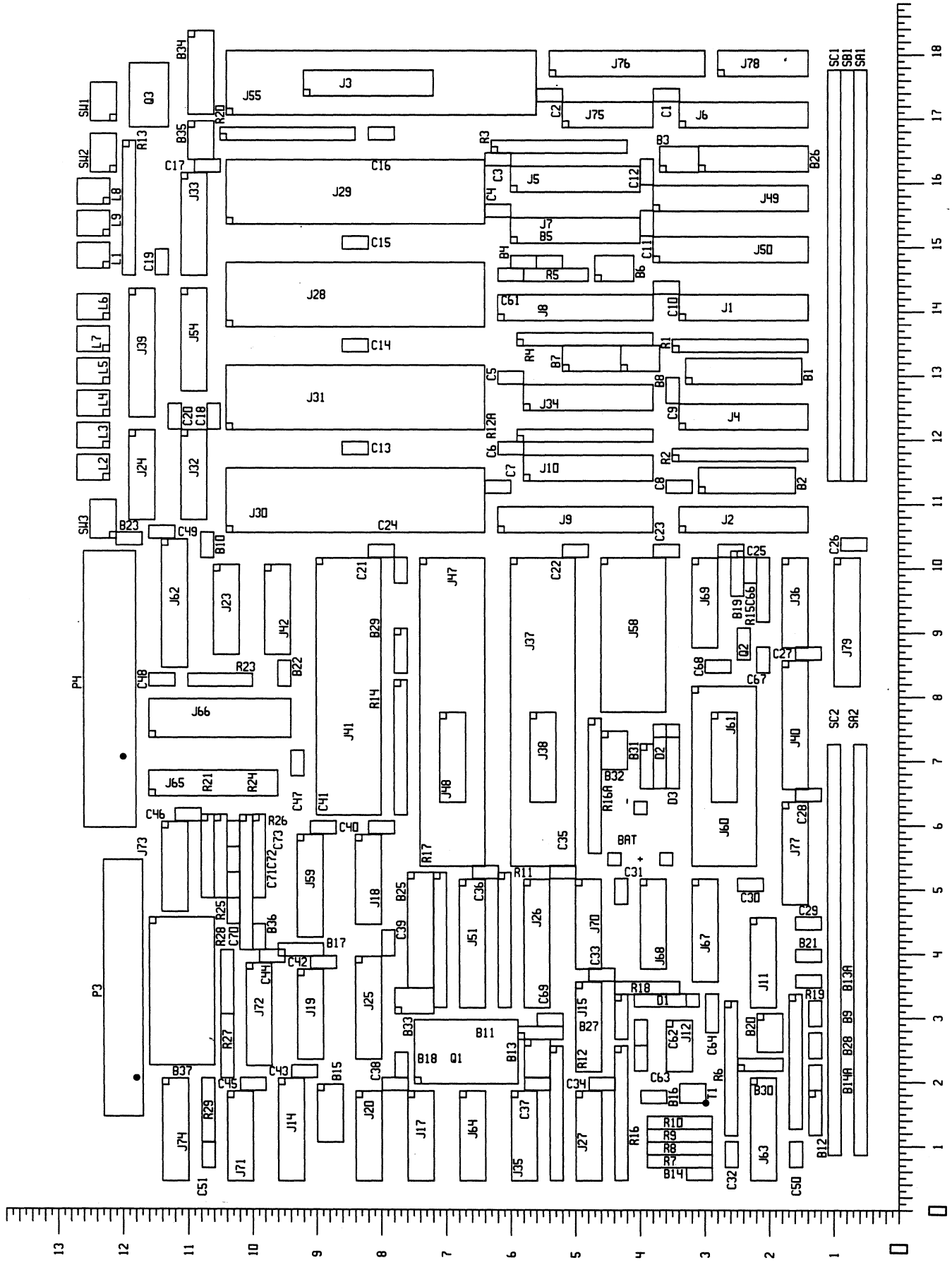
Description of the Jumperfields

Jumper-Field	Description	Default Cond.	Schematics	Location Coord. x y	see pg.
B1	Board Base Address selection for Address Lines A23-A16	2 - 15 5 - 12 6 - 11 7 - 10 8 - 9	1-B1	129/30	19
B2	Board Base Address selection for Address Lines A15-A9	1 - 14 2 - 13 4 - 11 5 - 10 6 - 9 7 - 8	1-B2	112/28	19
B3	BUS Timer enable jumper	2 - 3	1-B2	162/34	90
B4	IACK* - IACKIN* connection	1 - 2	1-A4	147/58	39
B5	BCLR* enable jumper	1 - 2	1-A4	147/54	83
B6	SYSCLOCK enable jumper	1 - 4	1-A4	145/44	77
B7	Address Modifier Code		1-B3	131/49	23
+ B8	Selection	1 - 4	1-B4	131/40	23
B9	Enables reset switch connected at P2 pins A20, A21, A22	1 - 2	2-A1	31/12	49
B10	Reset generation on ACFAIL detection	1 - 2	2-B1	104/106	53/ 58
B12	Selects ACFAIL signal connected at P2-PIN A1 or ground potential for the Centronics Interface	2 - 3	2-A3	16/12	55/ 109

Jumper -Field	Description	Default Cond.	Schematics	Location Coord. x y	see pg.
B13	Selection of ACFAIL* signal high or low active	1 - 2	2-A3	24/56	56
B13A	Connection of P2-PIN A19 to GND	1 - 2	2-A2	35/14	--
B14	Sense voltage selection	removed	2-B1	5/31	75
B14A	Connection of P2-PIN A26 to VCC	1 - 2	2-A3	21/12	--
B15	Selection of Reset delay after ACFAIL* detection	3 - 6	2-B2	17/88	58
B16	Selection of driven/not driven SYSRESET* signal	1 - 2	2-C1	17/36	48/ 73
B17	Not user selectable	2 - 3	2-C2	40/93	--
B18	Not user selectable	1 - 2	2-C1	23/76	--
B19	Not user selectable Default on ASCU-1 Default on ASCU-2	 2 - 3 1 - 2	3-C3	100/24	39
B20	Centronics I.F Configuration	1 - 4 2 - 3	4-B2	28/20	108
B21	Centronics I.F Configuration	1 - 2	4-B2	39/14	109
B22	Not user selectable Default on ASCU-1 Default on ASCU-2	 1 - 2 not con	4-C2	84/94	--
B23	IEEE-488 I.F ground for cable shield	1 - 2	4-D3	104/119	138
B25	IEEE-488 I.F Device Address selection	1 - 16 2 - 15 3 - 14 4 - 13 5 - 12	4-A4	50/74	137
B26	Enables/disables Bus Arbiter	2 - 10 4 - 12 6 - 14 8 - 16	5-B1	162/28	80

Jumper-Field	Description	Default Cond.	Schematics	Location Coord. x y	see pg.
B27	Test Interrupt / (limited selection)	2 - 3	3-B2	31/42	126
B28	Enables optional Test Interrupt switch connected at P2 connector	1 - 2	3-B4	26/12	126
B29	Only for test purposes	1 - 2	4-B3	88/76	--
B30	Selects reset switch connected at P2-PIN A2 or ground potential for Centronics I.F	1 - 2	4-B3	22/22	51/109
B31	Standby power for RTC	1 - 2	6-B4	70/38	117
B32	Only for test purposes	removed	5-C3	72/44	81
B33	Bus arbiter/arbitration type selection	1 - 2	5-D1	31/75	79
B34	Serial I/O signal configur.	1 - 12	6-B2 -3	181/108	97/103
B35	Serial I/O signal configur.	1 - 4 2 - 3	6-B4	167/108	97/103
B36	Enables/disables RS422 drivers	1 - 2	6-D4	43/98	99
B37	I/O configuration RS232 and RS422	16-17 31-32 41-42 46-47 51-52 21-22	7-AB -1-4	43/114	99

Coordinate Diagram



APPENDIX D

P1 Connector PIN Assignments

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	DØØ	BBSY*	DØ8
2	DØ1	BCLR*	DØ9
3	DØ2	ACFAIL*	D1Ø
4	DØ3	BGØIN*	D11
5	DØ4	BGØOUT*	D12
6	DØ5	BG1IN*	D13
7	DØ6	BG1OUT*	D14
8	DØ7	BG2IN*	D15
9	GND	BG2OUT*	GND
1Ø	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BRØ*	SYSRESET*
13	DSØ*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AMØ	A22
17	GND	AM1	A21
18	AS*	AM2	A2Ø
19	GND	AM3	A19
2Ø	IACK*	GND	A18
21	IACKIN*		A17
22	IACKOUT*		A16
23	AM4	GND	A15
24	AØ7	IRQ7*	A14
25	AØ6	IRQ6*	A13
26	AØ5	IRQ5*	A12
27	AØ4	IRQ4*	A11
28	AØ3	IRQ3*	A1Ø
29	AØ2	IRQ2*	AØ9
3Ø	AØ1	IRQ1*	AØ8
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+ 5V

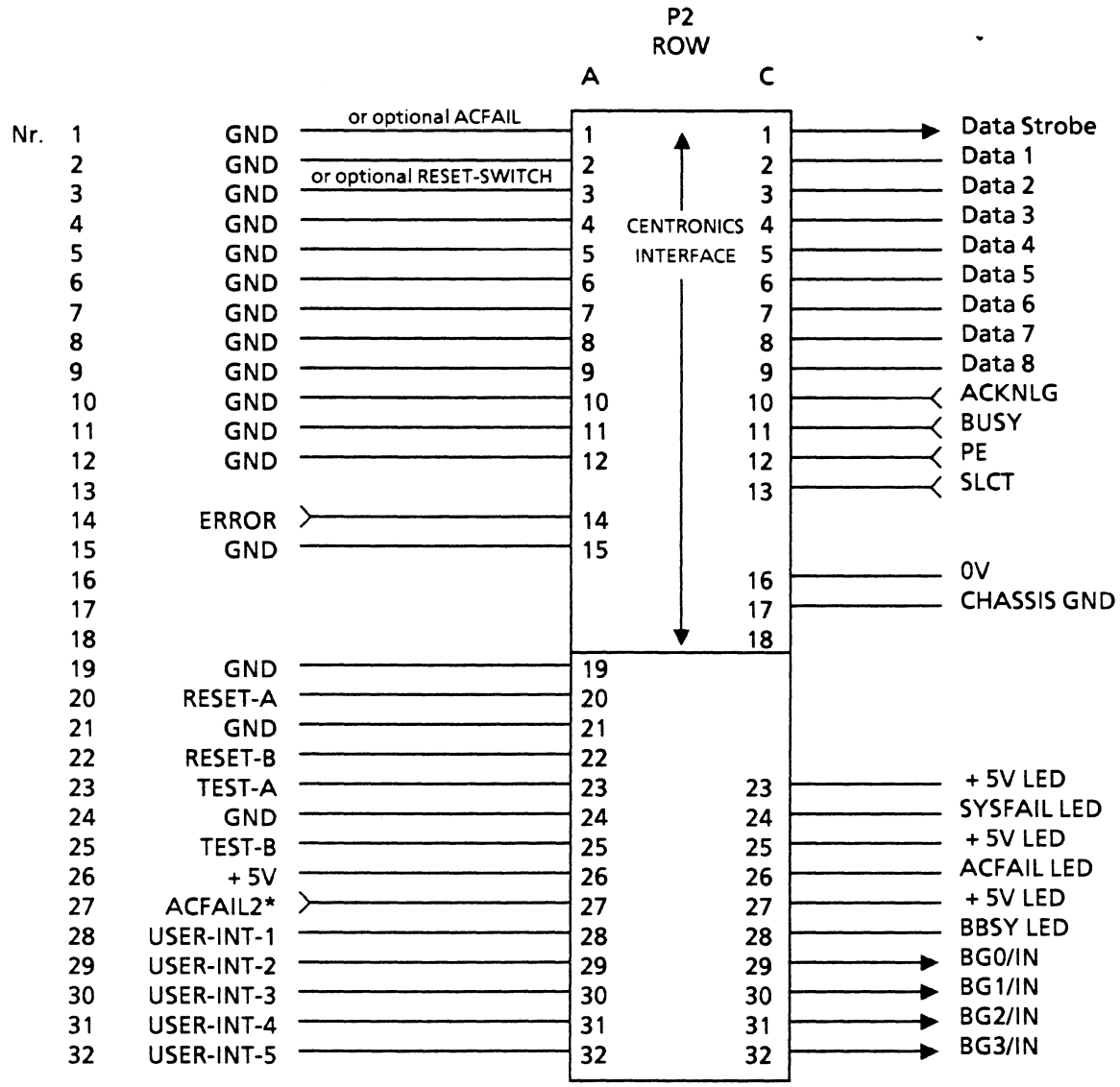
APPENDIX D

P2 Connector PIN Assignments

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	GND/ACFAIL 2*		DATA STROBE
2	GND/RESET		DATA 1
3	GND		DATA 2
4	GND		DATA 3
5	GND		DATA 4
6	GND		DATA 5
7	GND		DATA 6
8	GND		DATA 7
9	GND		DATA 8
10	GND		ACKNLG
11	GND		BUSY
12	GND		PE
13			SLCT
14	ERROR		
15	GND		
16			ØV
17			CHASSIS GND
18			
19	GND		
20	RESET-A		
21	GND		
22	RESET-B		
23	TEST-A		+5V LED
24	GND		SYSFAIL-LED
25	TEST-B		+5V LED
26	+5V		ACFAIL-LED
27	ACFAIL 2*		+5V LED
28	USER-INT 1		BBSY-LED
29	USER-INT 2		BGØ/IN
30	USER-INT 3		BG1/IN
31	USER-INT 4		BG2/IN
32	USER-INT 5		BG3/IN

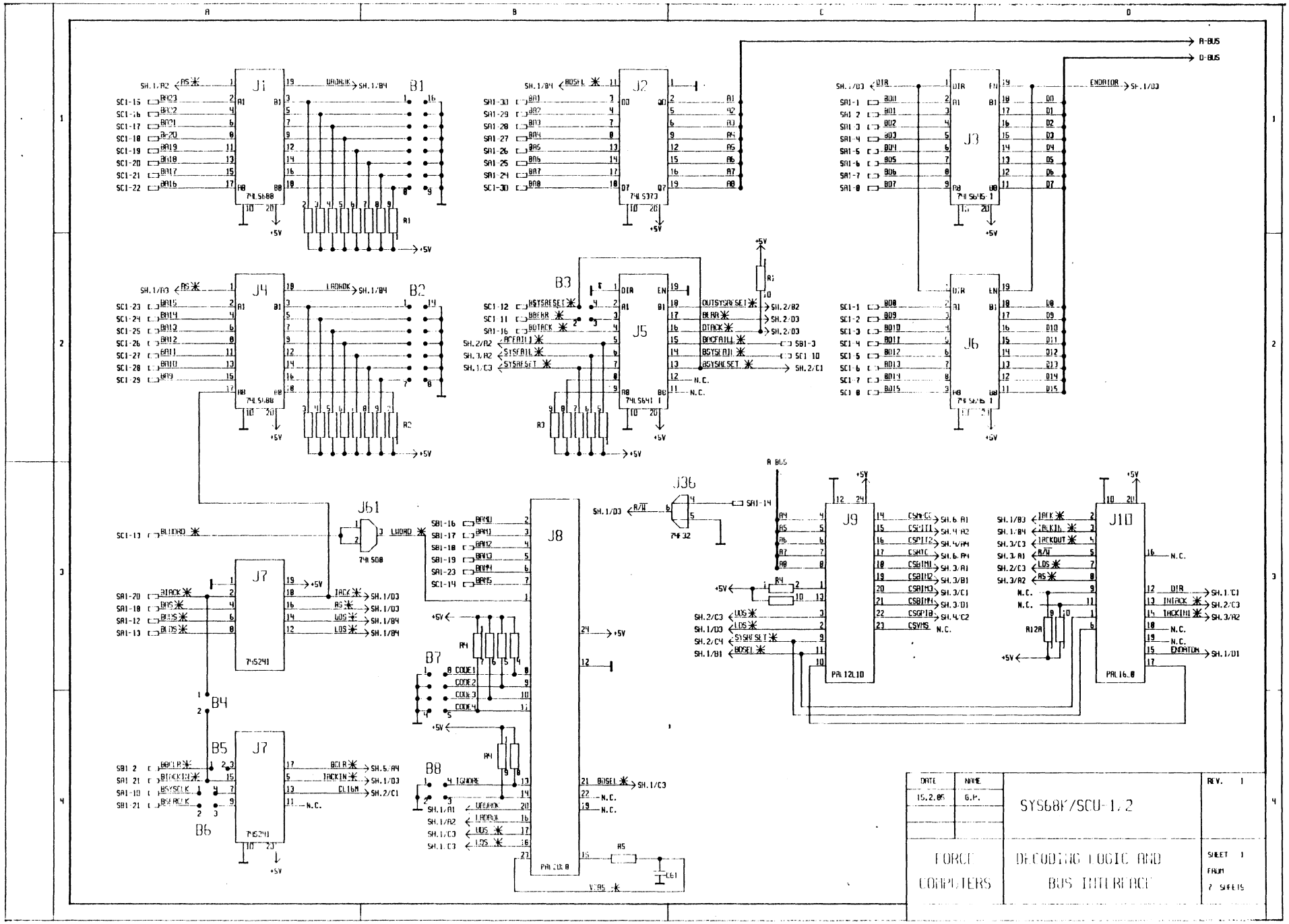
APPENDIX D

P2 Connector Pin - Assignments on the SYS68K/ASCU-1/2

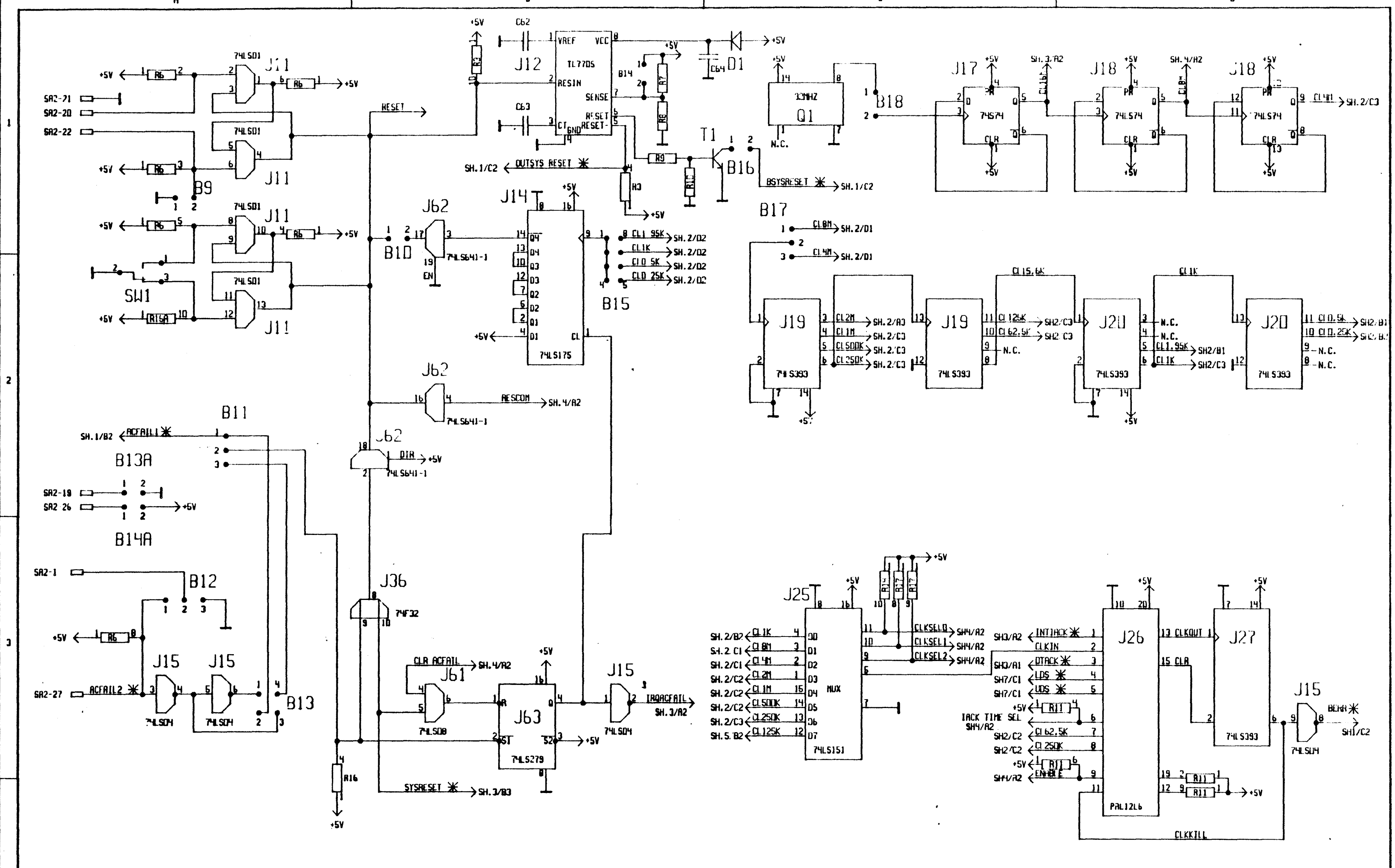


APPENDIX E

Circuit Schematics



DATE	NAME		REV. 1
15.2.85	G.P.	SYS68K/SCU-1.2	
FORCE COMPUTERS		DECODING LOGIC AND BUS INTERFACE	SHEET 1 FROM 7 SHEETS



DATE	NAME		REV. 1
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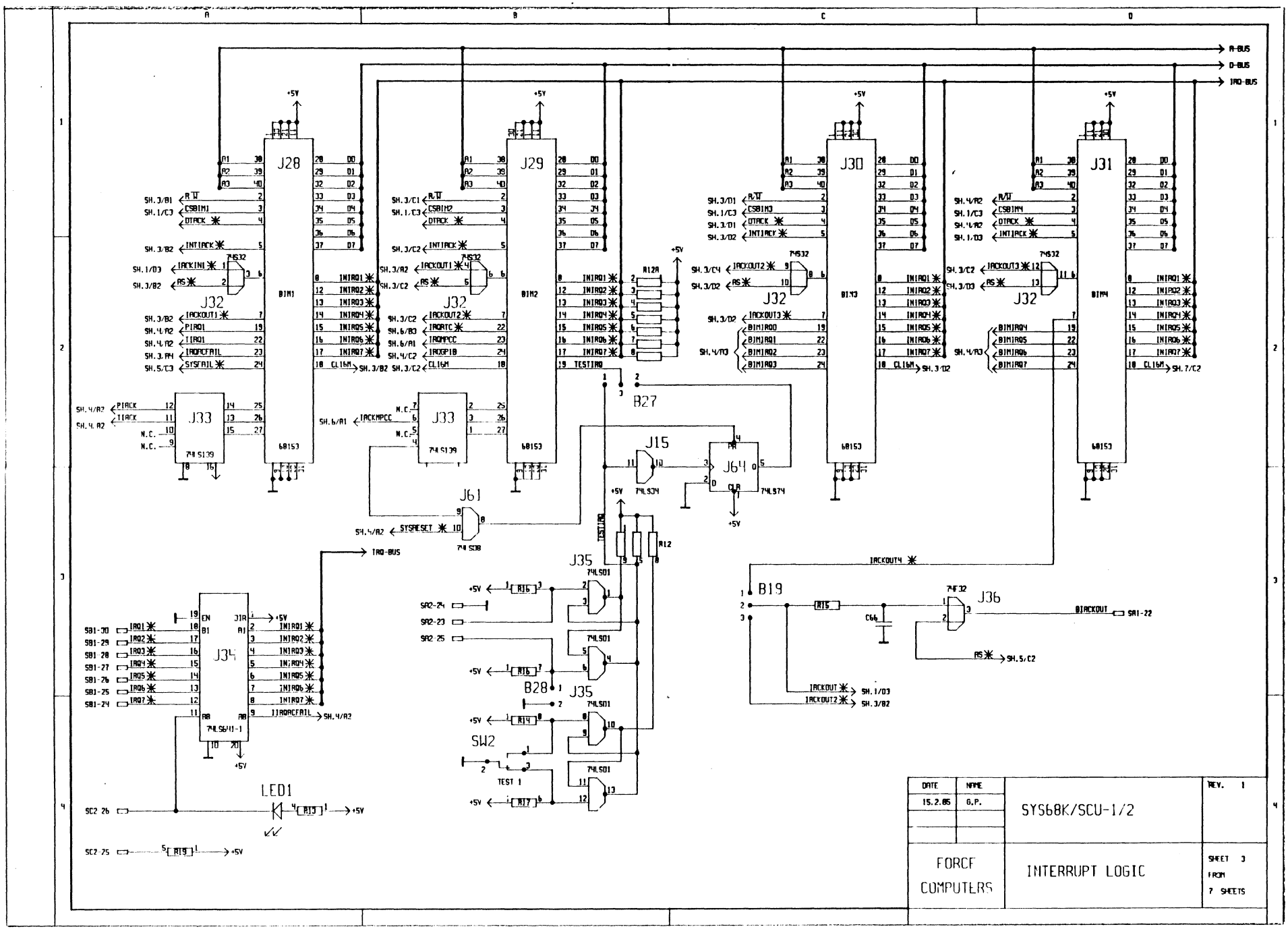
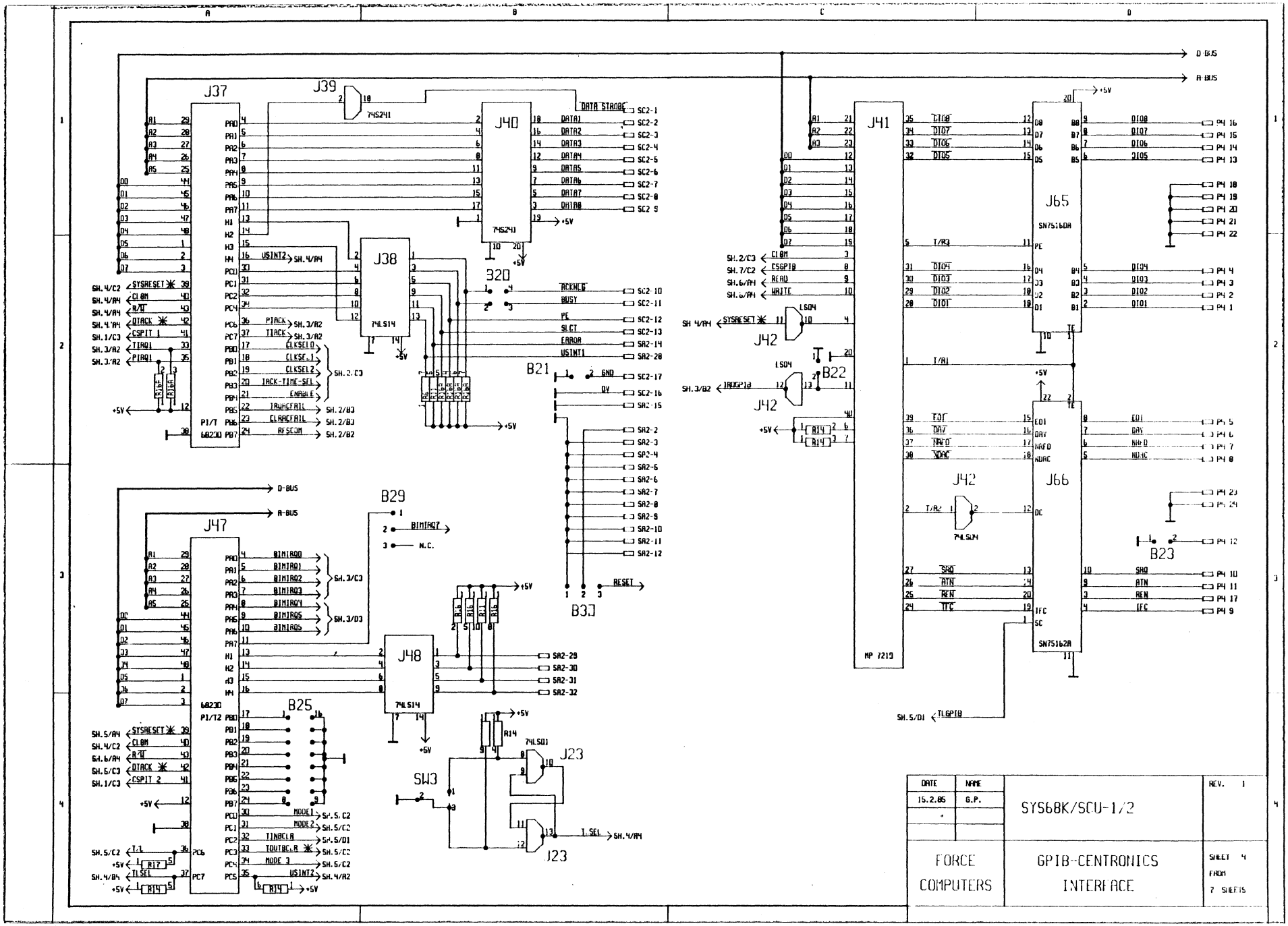
FORCE COMPUTERS		CLOCK/RESET/DTACK/ BERR-GENERATION	SHEET 2 FROM 7 SHEETS


A-BUS
D-BUS
IRQ-BUS
J28
J29
J30
J31
BIM1
BIM2
BIM3
BIM4
68153
J32
74S32
J33
74S139
J34
74LS641-1
J35
74LS01
J36
74F32
J61
74S08
J15
74LS74
J64
B27
B28
B19
SW2
TEST 1
LED1
R12A
R12
R15
R16
R17
R19
C66
+5V
IRQ-BUS
IACKOUT4
BIACKOUT
SA1-22
AS
SH.5/C2
SYSRESET
SH.4/A2
SH.3/B2
SH.1/D3
SH.3/C2
SH.3/A2
SH.3/C1
SH.1/C3
SH.3/B1
SH.3/D1
SH.1/C3
SH.3/D2
SH.3/C4
SH.3/D2
SH.4/A2
SH.1/C3
SH.1/D3
SH.3/C2
SH.3/D3
SH.4/B3
SH.7/C2
SH.3/D2
SH.4/B3
SH.6/A1
SH.4/A2
SH.4/A2
SH.4/B2
SH.5/C3
SH.1/D3
SH.3/B2
SH.4/A2
SH.4/B2
SH.3/A4
SH.5/C3
SH.3/B2
SH.3/C2
SH.6/B3
SH.6/A1
SH.4/C2
SH.3/C2
SH.3/C2
SH.3/D2
SH.1/D3
SH.3/B2
SA2-24
SA2-23
SA2-25
SC2-26
SC2-25
SB1-30
SB1-29
SB1-28
SB1-27
SB1-26
SB1-25
SB1-24
IRQ1
IRQ2
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
IRQACFAIL
SH.4/A2
IACKOUT
IACKOUT2
SH.1/D3
SH.3/B2
TESTIRQ
TEST 1
DATE
NAME
15.2.85
G.P.
SYS68K/SCU-1/2
REV. 1
FORCE COMPUTERS
INTERRUPT LOGIC
SHEET 3 FROM 7 SHEETS



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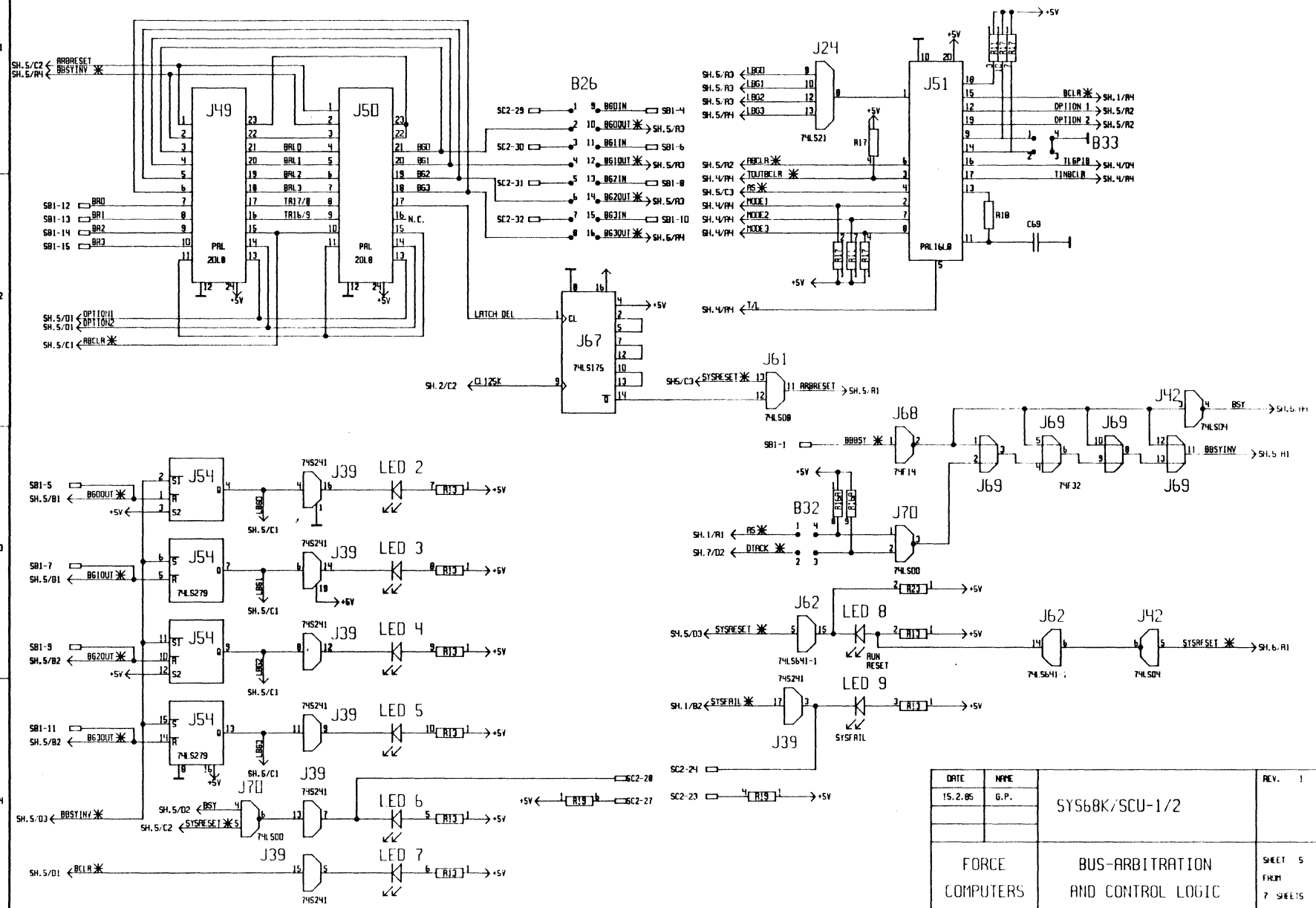
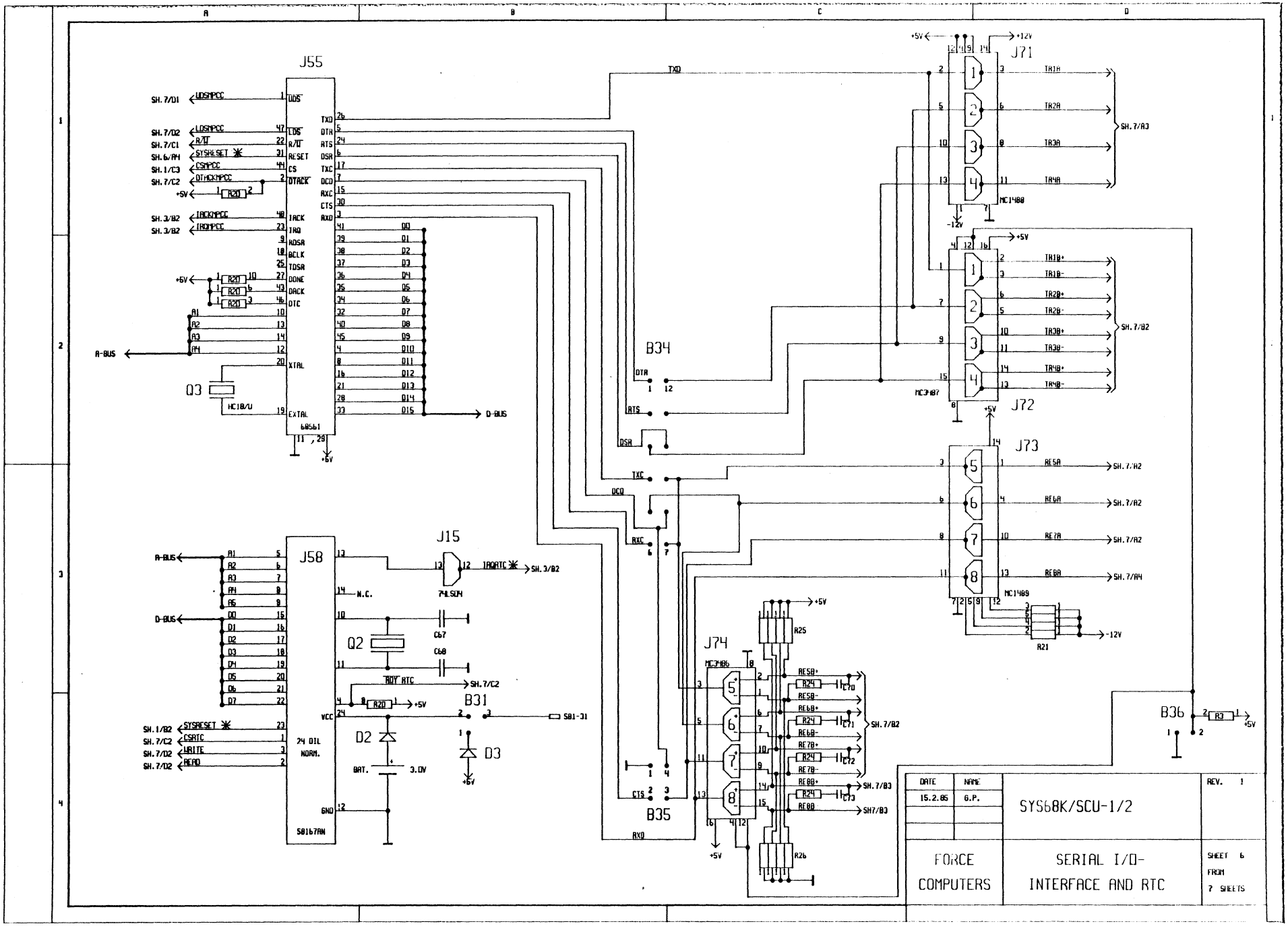
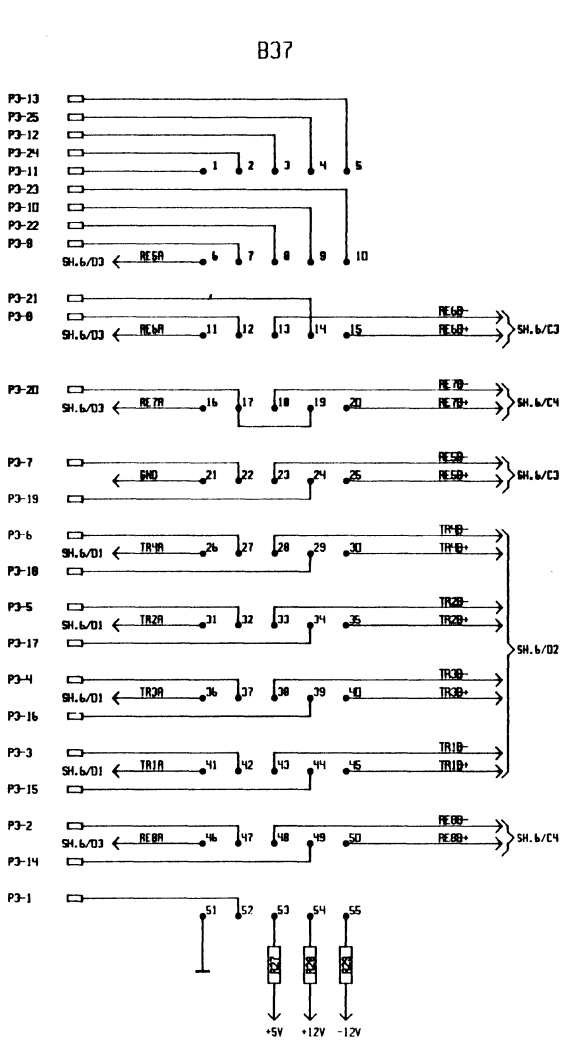
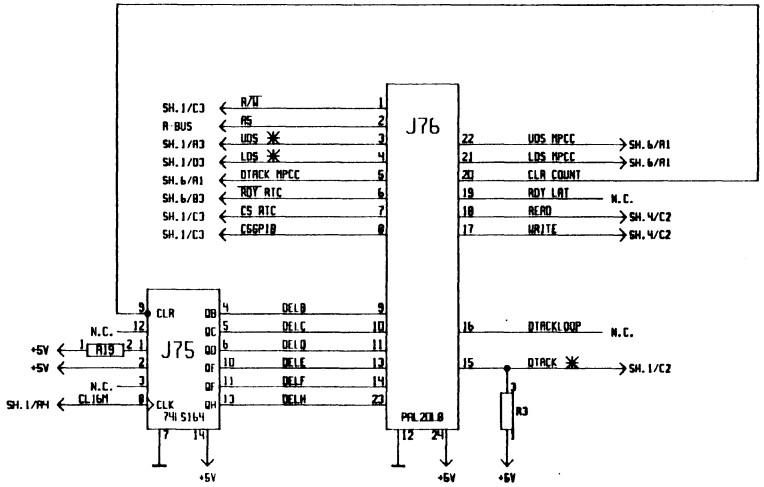
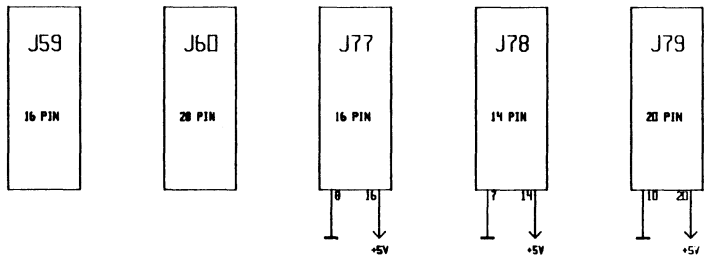
FORCE COMPUTERS		GPIB-CENTRONICS INTERFACE	SHEET 4 FROM 7 SHEETS


J49
J50
PAL 20L8
B26
J24
J51
74LS21
PAL16L8
J67
74LS175
J61
74LS08
J68
74F14
J69
74F32
J42
74LS04
J70
74LS00
J62
74LS641-1
J54
74LS279
J39
74S241
B32
B33
LED 2
LED 3
LED 4
LED 5
LED 6
LED 7
LED 8
LED 9
RUN RESET
SYSFAIL
SYSRESET
BBSY
BBSYINV
ABBRESET
BCLR
+5V
SYS68K/SCU-1/2
FORCE COMPUTERS
BUS-ARBITRATION AND CONTROL LOGIC
DATE 15.2.85
NAME G.P.
REV. 1
SHEET 5 FROM 7 SHEETS


J55
J58
J15
J71
J72
J73
J74
B34
B35
B36
B31
Q3
Q2
D2
D3
A-BUS
D-BUS
SH.7/D1
SH.7/D2
SH.7/C1
SH.6/A4
SH.1/C3
SH.7/C2
SH.3/B2
SH.7/B3
SH.7/A3
SH.7/B2
SH.7/A2
SH.7/A4
SH.7/C2
SH.3/B2
SH.1/B2
SH.7/D2
SH.7/D2
SYSRESET
LDSMPCC
R/W
CSMPCC
DTACKMPCC
IACKMPCC
IRQMPCC
XTAL
EXTAL
68561
MC1488
MC1489
MC1486
74LS14
5817AM
24 DIL NORM.
BAT.
3.0V
TXD
DTR
RTS
DSR
TXC
DCD
RXC
CTS
RXD
IRQRTC
RDY RTC
N.C.
GND
VCC
+5V
-12V
C67
C68
C69
C70
C71
C72
C73
R20
R21
R24
R25
R26
R3
DATE
NAME
15.2.85
G.P.
SYS68K/SCU-1/2
REV. 1
FORCE COMPUTERS
SERIAL I/O-INTERFACE AND RTC
SHEET 6 FROM 7 SHEETS







DATE	NAME		REV.
15.2.85	G.P.	SYS68K/SCU-1/2	!
FORCE COMPUTERS		CONTROL LOGIC AND SERIAL I/O CONNECTOR	SHEET 7 FROM 7 SHEETS

APPENDIX F

COMPONENT PART LIST / SYS68K/ASCU-1/2

IC's

Location	Type	Manufacturer	Package	Function
J1	74LS688	VARIOUS		Octal Comparator
J2	74LS373	VARIOUS		Octal D-type Latch
J3	74LS645-1	VARIOUS		Octal Bus Transceiver
J4	74LS688	VARIOUS		Octal Comparator
J5	74LS641-1	VARIOUS		O.C. Bus Transceiver
J6	74LS645-1	VARIOUS		Octal Bus Transceiver
J7	74S241	VARIOUS		Octal Buffer
J8	FRC 84	FORCE		PAL 20L8A
J9	FRC 85/92	FORCE		PAL 12L10
J10	FRC 86	FORCE		PAL 16L8A
J11	74LS01	VARIOUS		Quad NAND Gate O.C
J12	TL7705	T.I.		Voltage Supervisor
J14	74LS175	VARIOUS		Quad D-type Flip Flop
J15	74LS04	VARIOUS		Hex Inverter
J17	74S74	VARIOUS		Dual D-type Flip Flop
J18	74LS74	VARIOUS		Dual D-type Flip Flop
J19	74LS393	VARIOUS		Dual 4-bit Binary Counter
J20	74LS393	VARIOUS		Dual 4-bit Binary Counter
* J23	74LS01	VARIOUS		Quad NAND Gate O.C
J24	74LS21	VARIOUS		Dual 4-input AND Gates
J25	74LS151	VARIOUS		1 of 8 Multiplexer
J26	FRC 87	FORCE		PAL 12L6
J27	74LS393	VARIOUS		Dual 4-bit Binary

* included on the ASCU-2 only

APPENDIX F

COMPONENT PART LIST / SYS68K/ASCU-1/2

IC's

Location	Type	Manufacturer	Package	Function
J28	68153	MOTOROLA		BIM
J29	68153	MOTOROLA		BIM
* J30	68153	MOTOROLA		BIM
* J31	68153	MOTOROLA		BIM
J32	74S32	VARIOUS		Quad OR Gate
J33	74LS139	VARIOUS		Dual 2-to-4 Decoder
J34	74LS641-1	VARIOUS		O.C. Bus Transceiver
J35	74LS01	VARIOUS		Quad NAND Gate O.C
J36	74F32	VARIOUS		Quad OR Gate
J37	68230	MOTOROLA		PI/T
J38	74LS14	VARIOUS		Hex Inverters
J39	74S241	VARIOUS		Octal Buffer
J40	74S241	VARIOUS		Octal Buffer
* J41	7210	NEC		GPIB Controller
J42	74LS04	VARIOUS		Hex Inverters
* J47	68230	MOTOROLA		PI/T
* J48	74LS14	VARIOUS		Hex Inverters
J49	FRC 88	FORCE		PAL 20L8A
J50	FRC 89	FORCE		PAL 20L8A
J51	FRC 90	FORCE		PAL 16L8A
J54	74LS279	VARIOUS		Quad Latches
J55	68561	ROCKWELL,MOT		MPCC
J58	58167	NSC		Real Time Clock

* included on the ASCU-2 only

APPENDIX F

COMPONENT PART LIST / SYS68K/ASCU-1/2

IC's

Location	Type	Manufacturer	Package	Function
J59				SPARE
J60				SPARE
J61	74LS08	VARIOUS		Quad AND Gate
J62	74LS641-1	VARIOUS		O.C. Bus Transceiver
J63	74LS279	VARIOUS		Quad Latches
J64	74LS74	VARIOUS		Dual D-Type Flip Flop
* J65	75160A	T.I.		GPIB Bus Transceiver
* J66	75162A	T.I.		GPIB Bus Transceiver
J67	74LS175	VARIOUS		Quad D-type Flip Flop
J68	74F14	VARIOUS		Hex Inverters
J69	74F32	VARIOUS		Quad OR Gate
J70	74LS00	VARIOUS		Quad NAND Gate
J71	1488	MOTOROLA,NSC		RS232 Transmitter
J72	3487	MOTOROLA,NSC		RS422 Transmitter
J73	1489	MOTOROLA,NSC		RS232 Receiver
J74	3486	MOTOROLA,NSC		RS422 Receiver
J75	74LS164	VARIOUS		Shift Register
J76	FRC 91/93	FORCE		PAL 20L8A
J77				SPARE
J78				SPARE
J79				SPARE

* included on the ASCU-2 only

APPENDIX F

COMPONENT PART LIST / SYS68K/ASCU-1/2

DIODES

Location	Type	Manufacturer	Package	Function
D1	1N4148	VARIOUS		Diode
D2	1N4148	VARIOUS		Diode
D3	1N4148	VARIOUS		Diode
L1	24Ø6	DIALIGHT		LED Red
L2	23Ø6	DIALIGHT		LED Yellow
L3	23Ø6	DIALIGHT		LED Yellow
L4	23Ø6	DIALIGHT		LED Yellow
L5	23Ø6	DIALIGHT		LED Yellow
L6	22Ø6	DIALIGHT		LED Green
L7	24Ø6	DIALIGHT		LED Red
L8	24Ø6	DIALIGHT		LED Red
L9	24Ø6	DIALIGHT		LED Red

Crystals

Location	Type	Manufacturer	Package	Function
Q1	32.Ø MHz	VARIOUS		Quarz Oscillator Module
Q2	32.678KHz	VARIOUS		Quarz Oscillator
Q3	8.Ø64MHz	VARIOUS		Quarz Oscillator

Transistor

Location	Type	Manufacturer	Package	Function
T1	BC237	VARIOUS		Transistor

APPENDIX F

COMPONENT PART LIST / SYS68K/ASCU-1/2

Resistors (in Ohm)

Location	Type	Manufacturer	Package	Function
R1	9*4.7K	VARIOUS		
R2	9*4.7K	VARIOUS		
R3	9*68Ø	VARIOUS		
R4	9*4.7K	VARIOUS		
R6	9*4.7K	VARIOUS		
R7	68Ø	VARIOUS		
R9	1.5K	VARIOUS		
R1Ø	3.3K	VARIOUS		
R11	9*4.7K	VARIOUS		
R12	9*4.7K	VARIOUS		
R12A	9*4.7K	VARIOUS		
R13	9*1ØØ	VARIOUS		
R14	9*4.7K	VARIOUS		
R15	1ØØ	VARIOUS		
R16	9*4.7K	VARIOUS		
R16A	9*4.7K	VARIOUS		
R17	9*4.7K	VARIOUS		
R19	9*68Ø	VARIOUS		
R2Ø	9*4.7K	VARIOUS		
R21	5*27K	VARIOUS		

APPENDIX F

COMPONENT PART LIST / SYS68K/ASCU-1/2

Resistors (in Ohm)

Location	Type	Manufacturer	Package	Function
R24		VARIOUS		OPTIONAL FOR USER
R25		VARIOUS		OPTIONAL FOR USER
R26		VARIOUS		OPTIONAL FOR USER
R27	100	VARIOUS		
R28	100	VARIOUS		
R29	100	VARIOUS		

APPENDIX F

COMPONENT PART LIST / SYS68K/ASCU-1/2

CAPACITORS

Location	Type	Manufacturer	Package	Function
C1-C51	100nF	VARIOUS		CAPACITOR
C62	100nF	VARIOUS		CAPACITOR
C63	47uF/6.3V	VARIOUS		CAPACITOR (Tantal)
C64	47uF/6.3V	VARIOUS		CAPACITOR (Tantal)
C66	680pF	VARIOUS		CAPACITOR
C67	22pF	VARIOUS		CAPACITOR
C68	22pF	VARIOUS		CAPACITOR
C70		VARIOUS		OPTIONAL FOR USER
C71		VARIOUS		OPTIONAL FOR USER
C72		VARIOUS		OPTIONAL FOR USER
C73		VARIOUS		OPTIONAL FOR USER

APPENDIX F

COMPONENT PART LIST / SYS68K/ASCU-1/2

Mechanical Parts

Location	Type	Manufacturer	Package	Function
B1	DW16	VARIOUS		HEADER
B2	DW14	VARIOUS		HEADER
B3	DW4	VARIOUS		HEADER
B4	EW2	VARIOUS		HEADER
B5	EW2	VARIOUS		HEADER
B6	DW4	VARIOUS		HEADER
B7	DW8	VARIOUS		HEADER
B8	DW4	VARIOUS		HEADER
B9	EW2	VARIOUS		HEADER
B1Ø	EW2	VARIOUS		HEADER
B12	EW3	VARIOUS		HEADER
B13	DW4	VARIOUS		HEADER
B13A	EW2	VARIOUS		HEADER
B14	EW2	VARIOUS		HEADER
B14A	EW2	VARIOUS		HEADER
B15	DW8	VARIOUS		HEADER
B16	EW2	VARIOUS		HEADER
B17	EW3	VARIOUS		HEADER
B18	EW2	VARIOUS		HEADER
B19	EW3	VARIOUS		HEADER
B2Ø	DW4	VARIOUS		HEADER

APPENDIX F

COMPONENT PART LIST / SYS68K/ASCU-1/2

Mechanical Parts

Location	Type	Manufacturer	Package	Function
B21	EW2	VARIOUS		HEADER
B22	EW2	VARIOUS		HEADER
* B23	EW2	VARIOUS		HEADER
* B25	DW16	VARIOUS		HEADER
B26	DW16	VARIOUS		HEADER
B27	EW3	VARIOUS		HEADER
B28	EW2	VARIOUS		HEADER
* B29	EW3	VARIOUS		HEADER
B3Ø	EW3	VARIOUS		HEADER
B31	EW3	VARIOUS		HEADER
B32	DW4	VARIOUS		HEADER
B33	DW4	VARIOUS		HEADER
B34	DW12	VARIOUS		HEADER
B35	DW4	VARIOUS		HEADER
B36	EW2	VARIOUS		HEADER
B37	PW55	VARIOUS		HEADER

* included only on the ASCU-2

APPENDIX F

COMPONENT PART LIST / SYS68K/ASCU-1/2

Mechanical Parts

Location	Type	Manufacturer	Package	Function
J8		VARIOUS		24 PIN SLIM SOCKET
J9		VARIOUS		24 PIN SLIM SOCKET
J10		VARIOUS		20 PIN SOCKET
J26		VARIOUS		20 PIN SOCKET
J28		VARIOUS		40 PIN SOCKET
J29		VARIOUS		40 PIN SOCKET
* J30		VARIOUS		40 PIN SOCKET
* J31		VARIOUS		40 PIN SOCKET
J37		VARIOUS		2*24 PIN SIL SOCKET
* J41		VARIOUS		40 PIN SOCKET
* J47		VARIOUS		2*24 PIN SIL SOCKET
J49		VARIOUS		24 PIN SLIM SOCKET
J50		VARIOUS		24 PIN SLIM SOCKET
J51		VARIOUS		20 PIN SOCKET
J55		VARIOUS		2*24 PIN SIL SOCKET
J58		VARIOUS		24 PIN SOCKET
J76		VARIOUS		24 PIN SLIM SOCKET
SW1	AT-1F	KNITTER		SWITCH
SW2	AT-1F	KNITTER		SWITCH
* SW3	ATE-1D	KNITTER		SWITCH
P1				VG MALE CONNECTOR 96 PIN 90 DEGREES
P2				VG MALE CONNECTOR 64 PIN 90 DEGREES
P3				DSUB FEMALE CONNECT 25 PIN 90 DEGREES
* P4				MICRORIBBON FEMALE CONNECTOR 24 PIN 90 DEGREES
	JUMPERS-A			JUMPERS FOR HEADERS ASCU-1 (51) ASCU-2 (56)
	SCU-2-F			FRONT PANEL
	SCU-2-PC			PC-BOARD

* included on the ASCU-2 only

APPENDIX F

COMPONENT PART LIST / SYS68K/ASCU-1/2

Attached Components

	Attached Components SYS68K/ASCU-1/2
1	Lithium Battery CR1/3N (3.ØV)
2	Hardware User's Manual
3	Product Release Note

APPENDIX G

Glossary of P1Ø14 Terms

A16
A type of module that provides or decodes an address on address line AØ1 through A15.

A24
A type of module that provides or decodes an address on address lines AØ1 through A23.

A32
A type of module that provides or decodes an address on address lines AØ1 through A31.

ARBITRATION
The process of assigning control of the DTB to a REQUESTER.

ADDRESS-ONLY CYCLE
A DTB cycle that consists of an address broadcast, but no data transfer. SLAVES do not acknowledge ADDRESS-ONLY cycles and MASTERS terminate the cycle without waiting for an acknowledgment.

ARBITER
A functional module that accepts bus requests from REQUESTER modules and grants control of the DTB to one REQUESTER at a time.

ARBITRATION BUS
One of the four buses provided by the P1Ø14 backplane This bus allows an ARBITER module and several REQUESTER modules to coordinate use of the DTB.

ARBITRATION CYCLE
An ARBITRATION CYCLE begins when the ARBITER senses a bus request. The ARBITER grants the bus to a REQUESTER, which signals that the DTB is busy. The REQUESTER terminates the cycle by taking away the bus busy signal which causes the ARBITER to sample the bus requests again.

BACKPLANE (P1Ø14)
A printed circuit (PC) board with 96 pin connectors and signal paths that bus the connector pins. Some P1Ø14 systems have a single PC board, called the J1 backplane. It provides the signal paths needed for basic operation. Other P1Ø14 systems also have an optional second PC board called a J2 backplane. It provides the additional 96 pin connectors and signal paths needed for wider data and address transfers. Still others have a single PC board that provides the signal conductors and connectors of both the J1 and J2 backplanes.

BACKPLANE INTERFACE LOGIC

Special interface logic that takes into account the characteristics of the backplane: its signal line impedance, propagation time, termination values, etc. The P1Ø14 specification prescribes certain rules for the design of this logic based on the maximum length of the backplane and its maximum number of board slots.

BLOCK READ CYCLE

A DTB is cycle used to transfer a block of 1 to 256 bytes from a SLAVE to a MASTER. This transfer is done using a string of 1, 2, or 4 byte data transfers. Once the block transfer is started, the MASTER does not release the DTB until all of the bytes have been transferred. It differs from a string of read cycles in that the MASTER broadcasts only one address and address modifier (at the beginning of the cycle). Then the SLAVE increments this address on each transfer so that the data for the next cycle is retrieved from the next higher location.

BLOCK WRITE CYCLE

A DTB cycle used to transfer a block of 1 to 256 bytes from a MASTER to a SLAVE. The block write cycle is very similar to the block read cycle. It uses a string of 1, 2, or 4 byte data transfers and the MASTER does not release the DTB until all of the bytes have been transferred. It differs from a string of write cycles in that the MASTER broadcasts only one address and address modifier (at the beginning of the cycle). Then the SLAVE increments this address on each transfer so that the next transfer is stored on the next higher location.

BOARD

A printed circuit (PC) board, its collection or electronic components, and either one or two 96 pin connectors that can be plugged into P1Ø14 backplane connectors.

BUS TIMER

A functional module that measures how long each data transfer takes on the DTB and terminates the DTB cycle if a transfer takes too long. If the MASTER tries to transfer data to or from a non-existent SLAVE location it might wait forever. The BUS TIMER prevents this by terminating the cycle.

DØ8(Ø)

A SLAVE that sends and receives data 8 bits at a time over DØØ-DØ7,

or

an INTERRUPT HANDLER that receives 8 bit STATUS/IDs over DØØ-DØ7,

or

an INTERRUPTER that sends 8 bit STATUS/IDs over DØØ-DØ7.

D08(E0)

A MASTER that sends or receives data 8 bits at a time over either D00-D07 or D08-D15,

or

A SLAVE that sends and receives data 8 bits at a time over either D00-D07 or D08-D15,

or

an INTERRUPT HANDLER that receives 8 bit STATUS/IDs over D00-D07,

or

an INTERRUPTER that sends 8 bit STATUS/IDs over D00-D07.

D16

A MASTER that sends and receives data 16 bits at a time over D00-D15,

or

A SLAVE that sends and receives data 16 bits at a time over D00-D15,

or

an INTERRUPT HANDLER that receives 16 bit STATUS/IDs over D00-D15,

or

an INTERRUPTER that sends 16 bit STATUS/IDs over D00-D15.

D32

A MASTER that sends and receives data 32 bits at a time over D00-D31,

or

A SLAVE that sends and receives data 32 bits at a time over D00-D31,

or

an INTERRUPT HANDLER that receives 32 bit STATUS/IDs over D00-D31,

or

an INTERRUPTER that sends 32 bit STATUS/IDs over D00-D31.

DAISY-CHAIN

A special type of P1014 signal line that is used to propagate a signal level from board to board, starting with the first slot and ending with the last slot. There are four bus grant daisy-chains and one interrupt acknowledge daisy-chain on the P1014.

DATA TRANSFER BUS

One of the four buses provided by the P1014 backplane. The DATA TRANSFER BUS allows MASTERS to direct the transfer of binary data between themselves and SLAVES. (DATA TRANSFER BUS is often abbreviated to DTB).

DATA TRANSFER BUS CYCLE

A sequence of level transitions on the signal lines of the DTB that result in the transfer of an address or an address and data between a MASTER and a SLAVE. There are seven types of data transfer bus cycles.

DTB

An acronym for DATA TRANSFER BUS.

FUNCTIONAL MODULE

A collection of electronic circuitry that resides on one P1Ø14 board and works together to accomplish a task.

IACK DAISY-CHAIN DRIVER

A functional module which activates the interrupt acknowledge daisy-chain whenever an INTERRUPT HANDLER acknowledges an interrupt request. This daisy-chain ensures that only one INTERRUPTER will respond with its STATUS/ID when more than one has generated an interrupt request.

INTERRUPT ACKNOWLEDGE CYCLE

A DTB cycle, initiated by an INTERRUPT HANDLER that reads a "STATUS/ID" from an INTERRUPTER. An INTERRUPT HANDLER generates this cycle when it detects an interrupt request from an INTERRUPTER and it has control of the DTB.

INTERRUPT BUS

One of the four buses provided by the P1Ø14 backplane. The INTERRUPT BUS allows INTERRUPTER modules to send interrupt requests to INTERRUPT HANDLER modules.

INTERRUPTER

A functional module that generates an interrupt request on the INTERRUPT BUS and then provides STATUS/ID information when the INTERRUPT HANDLER requests it.

INTERRUPT HANDLER

A functional module that detects interrupt requests generated by INTERRUPTERS and responds to those requests by asking for STATUS/ID information.

LOCATION MONITOR

A functional module that monitors data transfers over the DTB in order to detect accesses to the locations it has been assigned to watch. When an access occurs to one of these assigned locations, the LOCATION MONITOR generates an on-board signal.

MASTER

A functional module that initiates DTB cycles in order to transfer data between itself and a SLAVE module.

OBO

A SLAVE that sends and receives data 8 bits at a time over DØØ-DØ7.

POWER MONITOR MODULE

A functional module that monitors the status of the primary power source to the P1Ø14 system and signals when that power has strayed outside the limits required for reliable system operation. Since most systems are powered by an AC source, the power monitor is typically designed to detect drop-out or brown-out conditions on AC lines.

READ CYCLE

A DTB cycle used to transfer 1, 2, or 4 bytes from a SLAVE to a MASTER. The cycle begins when the MASTER broadcasts and address and an address modifier. Each SLAVE captures this address and address modifier, and checks to see of it is to respond to the cycle. If so, it retrieves the data from its internal storage, places it on the data bus and acknowledges the transfer. Then the MASTER terminates the cycle.

READ-MODIFY-WRITE CYCLE

A DTB cycle that is used to both read from, and write to, a SLAVE location without permitting any other MASTER to access that location. This cycle is most useful in multiprocessing systems where certain memory locations are used to control access to certain systems resources. (For example, semaphore locations.)

REQUESTER

A functional module that resides on the same board as a MASTER or INTERRUPT HANDLER and requests use of the DTB whenever its MASTER or INTERRUPT HANDLER needs it.

SERIAL CLOCK DRIVER

A functional module that provides a periodic timing signal that synchronizes operation of the VMSbus. (Although the P1Ø14 specification defines a SERIAL CLOCK DRIVER for use with the VMSbus, and although it reserves two backplane signal lines for use by that bus, the VMSbus protocol is completely independent of the P1Ø14.)

SLAVE

A functional module that detects DTB cycles initiated by a MASTER and, when those cycles specify its participation, transfers data between itself and the MASTER.

SLOT

A position where a board can be inserted into a P1Ø14 backplane. If the P1Ø14 system has both a J1 and a J2 backplane (or a combination J1/J2 backplane) each slot provides a pair of 96 pin connectors. If the system has only a J1 backplane, then each slot provides a single 96 pin connector.

SUBRACK

A rigid framework that provides mechanical support for boards inserted into the backplane, ensuring that the connectors mate properly and that adjacent boards do not contact each other. It also guides the cooling airflow through the system, and ensures that inserted boards do not disengage themselves from the backplane due to vibration or shock.

SYSTEM CLOCK DRIVER

A functional module that provides a 16 MHz timing signal on the UTILITY BUS.

SYSTEM CONTROLLER BOARD

A board which resides in slot 1 of a P1Ø14 backplane and has a SYSTEM CLOCK DRIVER, a DTB ARBITER, an IACK DAISY CHAIN DRIVER, and a BUS TIMER. Some also have a SERIAL CLOCK DRIVER, a POWER MONITOR or both.

UAT

A MASTER that sends or receives data in an unaligned fashion,

or

a SLAVE that sends and receives data in an unaligned fashion.

UTILITY BUS

One of the four buses provided by the P1Ø14 backplane. This bus includes signals that provide periodic timing and coordinate the power-up and power-down of P1Ø14 systems.

WRITE CYCLE

A DTB cycle used to transfer 1, 2, or 4 bytes from a MASTER to a SLAVE. The cycle begins when the MASTER broadcasts an address and address modifier and places data on the DTB. Each SLAVE captures this address and address modifier, and checks to see if it is to respond to the cycle. If so, it stores the data and then acknowledges the transfer. The MASTER then terminates the cycle.

APPENDIX H

Data Sheets

MOTOROLA
SEMICONDUCTORS

P.O. BOX 20912 • PHOENIX, ARIZONA 85036

MC68153

Advance Information

BUS INTERRUPTER MODULE

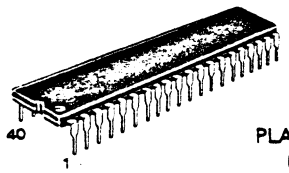
The bipolar LSI MC68153 Bus Interrupter interfaces a microcomputer system bus to multiple slave devices requiring interrupt capabilities. It handles up to 4 independent sources of interrupt requests and is fully programmable.

- VERSAbus/VMEbus Compatible
- MC68000 Compatible
- Handles 4 Independent Interrupt Sources
- 8 Programmable Read/Write Registers
- Programmable Interrupt Request Levels
- Programmable Interrupt Vectors
- Supports Interrupt Acknowledge Daisy Chain
- Control Registers Contain Flag Bits
- Single +5.0 Volt Supply
- Total Power Dissipation = 1.5 W Typical
- Temperature Range of 0°C to 70°C
- Chip Access Time = 200 ns Typical with 16 MHz Clock
- 40-Pin Dual-In-Line Package

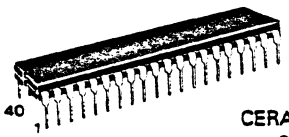
TTL

BUS INTERRUPTER MODULE

ADVANCED LOW POWER SCHOTTKY

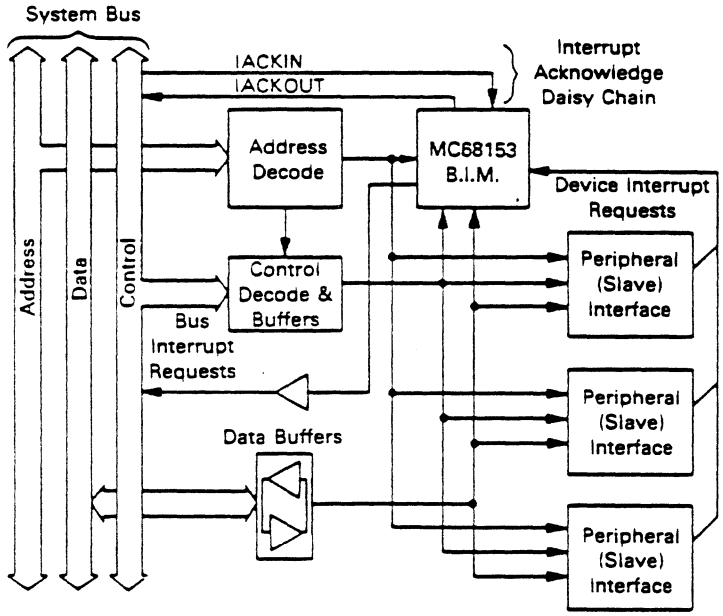


P SUFFIX
PLASTIC PACKAGE
CASE 711-03



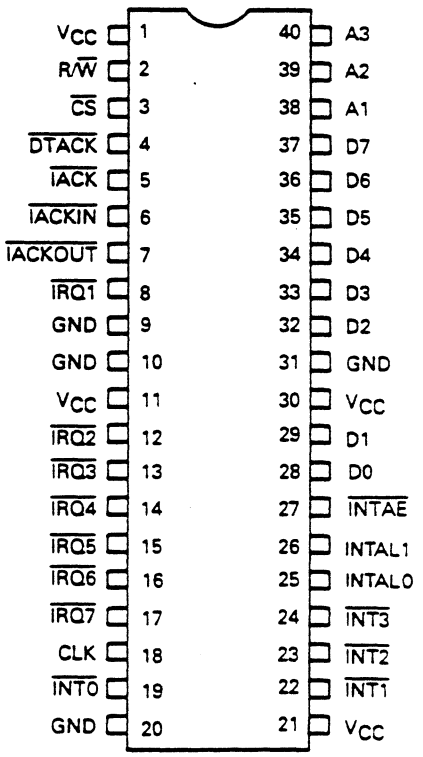
L SUFFIX
CERAMIC PACKAGE
CASE 734-04

FIGURE 1 — MC68153 SYSTEM BLOCK DIAGRAM



VERSAbus is a trademark of Motorola.

PIN ASSIGNMENTS



This document contains information on a new product. Specifications and information herein are subject to change without notice

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ADI-1057
(Replacing NP-151)

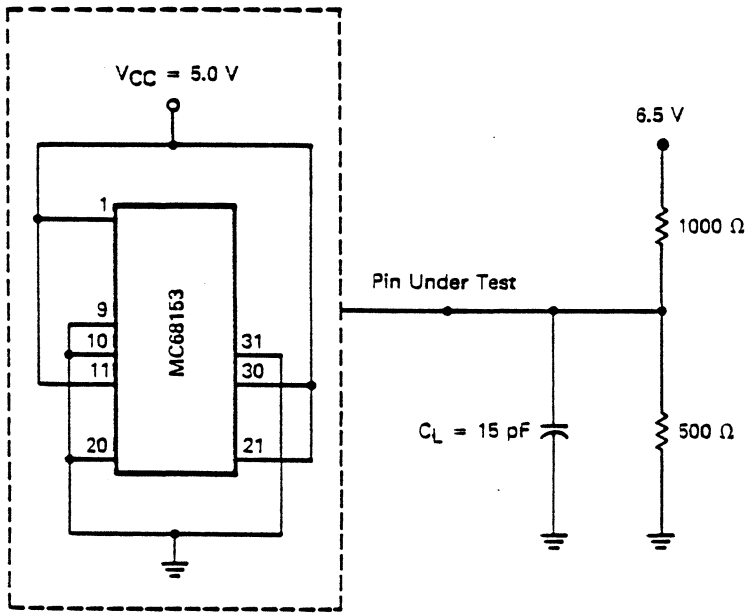
ABSOLUTE MAXIMUM RATINGS (Beyond which useful life may be impaired.)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{in}	−0.5 to +7.0	V
Input Current	I_{in}	−30 to +5.0	mA
Output Voltage	V_{out}	−0.5 to +5.5	V
Output Current	I_{OL}	Twice Rated I_{OL}	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Junction Operating Temperature	T_J	−55 to +175	°C

DC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 V ±5%, T_A = 0°C to 70°C)

Parameter	Symbol	Min	Max	Unit	Test Conditions
High Level Input Voltage	V_{IH}	2.0	—	V	
Low Level Input Voltage	V_{IL}	—	0.8	V	
Input Clamp Voltage	V_{IK}	—	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
High Level Output Voltage(1)	V_{OH}	2.7	—	V	V_{CC} = MIN, I_{OH} = −400 μA
Low Level Output Voltage	V_{OL}	—	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
Output Short Circuit Current(2)	I_{OS}	−15	−130	mA	V_{CC} = MAX, V_{OUT} = 0 V
High Level Input Current	I_{IH}	—	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
Low Level Input Current	I_{IL}	—	−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
Supply Current	I_{CC}	225	385	mA	V_{CC} = MAX
Output Off Current (High)	I_{OZH}	—	20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V
Output Off Current (Low)	I_{OZL}	—	−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V

AC TEST CIRCUIT — AC Testing of All Outputs



NOTES:
1. Not applicable to open-collector outputs.
2. Not more than one output should be shorted at a time for longer than one second.
3. $\overline{CS}$ Low to CLK High (Setup Time) of 15 ns Min must be observed.
4. $\overline{IACK}$ Low to CLK High and $\overline{IACKIN}$ Low to CLK High (Setup Times) of 15 ns Min must be observed.
5. See Table 1 for additional performance guidelines.

AC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 V ±5%, T_A = 0°C to 70°C)

Parameter	Test Number(5)	Max (ns)
CLK High to Data Out Valid (Delay)(3)	1	55
CLK High to $\overline{\text{DTACK}}$ Low (Delay)(3)	2	40
$\overline{\text{CS}}$ High to $\overline{\text{DTACK}}$ High (Delay)	3	35
CLK High to Data Out Valid (Delay)(4)	4	55
CLK High to $\overline{\text{INTAE}}$ Low (Delay)(4)	5	40
$\overline{\text{IACK}}$ High to Data Out High Impedance (Delay)	6	60
$\overline{\text{IACK}}$ High to $\overline{\text{DTACK}}$ High (Delay)	7	45
$\overline{\text{CS}}$ High to Data Out High (Delay)	8	45
CS High to IRQ High (Delay)	9	60
$\overline{\text{IACK}}$ High to $\overline{\text{INTAE}}$ High (Delay)	10	35

GENERAL DESCRIPTION

The MC68153 Bus Interrupter Module (BIM) is designed to serve as an interrupt requester for peripheral devices in a microcomputer system. Up to 4 independent devices can be interfaced to the system bus by the MC68153. Intended for asynchronous master/slave bus operation, the BIM is compatible with VERSAbus, VMEbus, MC68000 device bus, and other system buses. Figure 1 shows a block diagram of a typical configuration. In this example, three peripheral devices (bus slaves) are connected to the system data bus. Each of these devices could be parallel I/O, serial I/O, or some other function. An interrupt request from any device is routed to the MC68153, and the BIM handles all interface to the system bus. It generates a bus interrupt request as a result of the device interrupt request. When the system interrupt handler or processor responds with an interrupt acknowledge cycle, the MC68153 can answer supplying an interrupt vector and handling all timing.

The functional block diagram of the MC68153 is shown in Figure 2. The device contains circuitry to accept four separate interrupt sources ($\overline{\text{INT0}}$ – $\overline{\text{INT3}}$). Interface to the system bus includes generation of bus interrupt requests ($\overline{\text{IRQ1}}$ – $\overline{\text{IRQ7}}$), response to a bus interrupt acknowledge cycle (either supplying a vector or passing on a daisy chain signal), and releasing the bus interrupt request signal at the proper time. The BIM has flexibility provided by eight programmable read/write registers. Four 8-bit vector registers (VR0 – VR3) contain status/address information and supply a byte vector in response to an interrupt acknowledge cycle for the corresponding interrupt source. Four other 8-bit control registers (CR0 – CR3) contain information that oversees operation of the interrupt circuitry. The control information is programmable and includes interrupt request level and interrupt enable and disable. Also contained in the control registers are flag-bits. These flags are useful for task coordination, resource management, and interprocessor communication.

SIGNAL DESCRIPTION

Throughout the data sheet, signals are presented using the terms asserted and negated independent of whether the signal is asserted in the high voltage or low voltage state. Active low signals are denoted by a superscript bar.

BIDIRECTIONAL DATA BUS — D0 – D7

Pins D0 – D7 form an 8-bit bidirectional data bus to/from the system bus. These are active high, 3-state pins.

ADDRESS INPUTS — A1 – A3

These active high inputs serve two functions. One function is to select one of the eight possible registers during a read or write cycle. Secondly, during an interrupt acknowledge A1 – A3 show the level of interrupt being acknowledged, and the BIM uses these to determine if a match exists with an internal level.

CHIP SELECT — $\overline{\text{CS}}$

$\overline{\text{CS}}$ is an active low input used to select the BIM's registers for the current bus cycle. Address strobe, data strobe, and appropriate address bits must be included in the chip select equation.

READ/WRITE — R/$\overline{\text{W}}$

The R/$\overline{\text{W}}$ input is a signal from the system bus used to determine if the current bus cycle is a read (high) or write (low).

DATA TRANSFER ACKNOWLEDGE — $\overline{\text{DTACK}}$

$\overline{\text{DTACK}}$ is an open-collector, active low output that signals the completion of a read, write, or interrupt acknowledge cycle. During read or interrupt acknowledge cycles, $\overline{\text{DTACK}}$ is asserted by the MC68153 after data has been provided on the data bus; during write cycles it is asserted after data has been accepted from the data bus. A pullup resistor is required to maintain $\overline{\text{DTACK}}$ high between bus cycles.

FIGURE 2 — MC68153 FUNCTIONAL BLOCK DIAGRAM

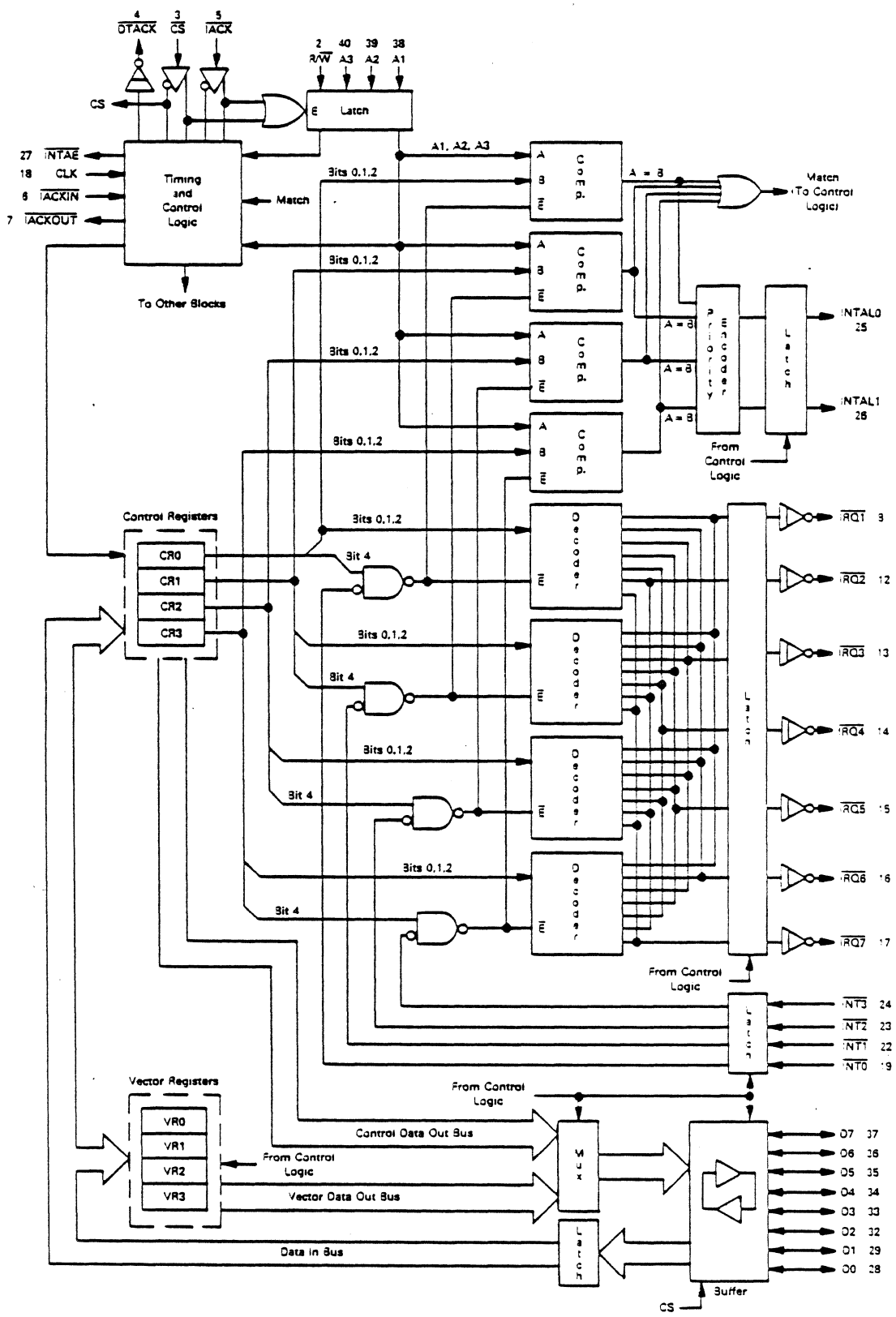
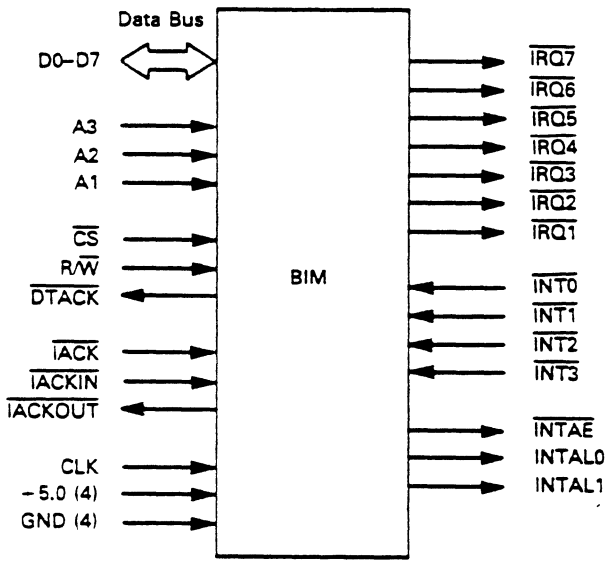


FIGURE 3 — LOGICAL PIN ASSIGNMENT



INTERRUPT ACKNOWLEDGE SIGNALS — $\overline{IACK}$, $\overline{IACKIN}$, $\overline{IACKOUT}$

These three pins support the interrupt acknowledge cycle. A low level on the $\overline{IACK}$ input indicates an interrupt acknowledge cycle has been initiated. This signal is conditioned externally with Address Strobe and the lower data strobe of an MC68000 type bus. After $\overline{IACK}$ is asserted the BIM compares the interrupt level presented on address lines A1, A2, and A3 with the current levels generated internally and determines if a match exists. Then, if input $\overline{IACKIN}$ is asserted (driven low), the BIM will either complete the interrupt acknowledge cycle if a match exists or assert output $\overline{IACKOUT}$ if *no* match exists.

$\overline{IACKIN}$ and $\overline{IACKOUT}$ form part of a prioritized interrupt acknowledge daisy chain. The daisy chain prioritizes interrupters and guarantees that two or more devices requesting an interrupt on the same level will not respond to the same cycle. The requesting device (or interrupter) must wait until $\overline{IACKIN}$ is asserted and not pass the signal on (assert $\overline{IACKOUT}$) if it is to complete the interrupt acknowledge cycle.

BUS INTERRUPT REQUEST SIGNALS — $\overline{IRQ1}$ – $\overline{IRQ7}$

These open-collector outputs are low when asserted, indicating a bus interrupt is requested at the corresponding level. An open-collector buffer is normally required for sufficient drive when interfacing to a system bus. A pullup resistor is required to maintain $\overline{IRQ1}$ – $\overline{IRQ7}$ high between interrupt requests.

DEVICE INTERRUPT REQUEST SIGNALS — $\overline{INT0}$ – $\overline{INT3}$

$\overline{INT0}$ – $\overline{INT3}$ are active low inputs used to indicate to the BIM that a device wants a bus interrupt.

INTERRUPT ACKNOWLEDGE ENABLE — $\overline{INTAE}$

During an interrupt acknowledge cycle, this output pin is asserted low to indicate that outputs INTAL0 and INTAL1 are valid. These two outputs contain an encoded number (x) corresponding to the interrupt ($\overline{INTx}$) being acknowledged. This feature can be used to signal interrupting devices, which supply their own vector, when to respond to the interrupt acknowledge cycle with the vector and a $\overline{DTACK}$ signal.

INTERRUPT ACKNOWLEDGE LEVEL — INTAL0, INTAL1

These active high outputs contain an encoded number corresponding to the interrupt level being acknowledged. They are valid only when $\overline{INTAE}$ is asserted low.

CLOCK — CLK

The CLK input is used to supply the clock for internal operations of the MC68153.

RESET — $\overline{CS}$, $\overline{IACK}$

Although a reset input is not supplied, an on-board reset is performed if $\overline{CS}$ and $\overline{IACK}$ are asserted simultaneously.

FIGURE 4 — MC68153 REGISTER MODEL

ADDRESS BIT A3	A2	A1	FLAG	FLAG AUTO-CLEAR	EXTERNAL/INTERNAL	INTERRUPT ENABLE	INTERRUPT AUTO-CLEAR	INTERRUPT LEVEL			REGISTER NAME
0	0	0	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 0
0	0	1	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 1
0	1	0	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 2
1	1	1	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 3
1	0	0	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 0
1	0	1	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 1
1	1	0	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 2
1	1	1	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 3
			7	6	5	4	3	2	1	0	REGISTER NAME
			REGISTER BIT								

REGISTER DESCRIPTION

The MC68153 contains 8 programmable read/write registers. There are four control registers (CR0 – CR3) that govern operation of the device. The other four (VR0 – VR3) are vector registers that contain the vector data used during an interrupt acknowledge cycle. Figure 4 illustrates the device register model.

CONTROL REGISTERS

There is a control register for each interrupt source, i.e., CR0 controls $\overline{INT0}$, CR1 controls $\overline{INT1}$, etc. The control registers are divided into several fields:

1. Interrupt level (L2, L1, L0) — The least significant 3-bit field of the register determines the level at which an interrupt will be generated:

L2	L1	L0	IRQ LEVEL
0	0	0	DISABLED
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

   A value of zero in the field disables the interrupt.

2. Interrupt Enable (IRE) — This field (Bit 4) must be set (high level) to enable the bus interrupt request associated with the control register. Thus, if the $\overline{INTX}$ line is asserted and IRE is cleared, *no* interrupt request ($\overline{IRQX}$) will be asserted.
3. Interrupt Auto-Clear (IRAC) — If the IRAC is set (Bit 3), IRE (Bit 4) is cleared during an interrupt acknowledge cycle responding to this request. This action of clearing IRE disables the interrupt request. To re-enable the interrupt associated with this register, IRE must be set again by writing to the control register.
4. External/Internal (X/$\overline{IN}$) — Bit 5 of the control register determines the response of the MC68153 during an interrupt acknowledge cycle. If the X/$\overline{IN}$ bit is clear (low level) the BIM will respond with vector data and a $\overline{DTACK}$ signal, i.e., an internal response. If X/$\overline{IN}$ is set, the vector is not supplied and no $\overline{DTACK}$ is given by the BIM, i.e., an external device should respond.
5. Flag (F) — Bit 7 is a flag that can be used in conjunction with the test and set instruction of the MC68000. It can be changed without affecting chip operation. It is useful for processor-to-processor communication and resource allocation.
6. Flag Auto-Clear (FAC) — If FAC (Bit 6) is set, the Flag bit is automatically cleared during an interrupt acknowledge cycle.

VECTOR REGISTERS

Each interrupt input has its own associated vector register. Each register is 8 bits wide and supplies a data byte during its interrupt acknowledge cycle if the associated External/Internal (X/$\overline{IN}$) control register bit is clear. This data can be status, identification, or address information depending on system usage. The information is programmed by the system user.

DEVICE RESET

When the MC68153 is reset, the registers are set to a known condition. The control registers are set to all zeros (low). The vector registers are set to $0F. This value is the MC68000 vector for an uninitialized interrupt vector.

FUNCTIONAL DESCRIPTION

SYSTEM OVERVIEW

The MC68153 is compatible with many system buses, however, it is primarily intended for VMEbus, VERSAbus and MC68000 applications. Figure 5 shows a system configuration similar to VMEbus. In the figure only one system Data Transfer Bus (DTB) master is used. The Priority Interrupt structure provides a means for peripheral slave devices to ask for an interrupt of other processor (DTB master) activity and receive service from the processor. The MC68153 BIM acts as an interface device requesting and responding to interrupt acknowledge cycles for up to 4 independent slaves.

In Figure 5, functional modules are identified as Interrupters and an Interrupt Handler. An Interrupter (such as the MC68153) receives slave requests for an interrupt and handles all interface to the system bus required to ask for and respond to interrupt requests. The Interrupt Handler receives the bus interrupt requests, determines when an interrupt acknowledge will occur and at which level, and finally either performs the interrupt acknowledge (IACK) cycle or tells the DTB master to execute the IACK cycle.

The signal lines in the Priority Interrupt structure include (* — indicates active low):

1. IRQ1*–IRQ7* — seven prioritized interrupt request lines.
2. IACK* — signal line that indicates an interrupt acknowledge cycle is occurring.
3. IACKIN*/IACKOUT* — two signals that form part of a daisy chain that prioritizes interrupters.

In addition Data Transfer Bus control signals are involved in the IACK bus cycle:

1. AS* — the Address Strobe asserted low indicates a valid address is on the bus.
2. DSO* — the lower Data Strobe asserted low indicates a data transfer will occur on bus bits D00–D07.
3. WRITE* — the Read/Write is negated indicating the data is to be read from the Interrupter.
4. A01–A03 — Address lines A01–A03 contain the encoded priority level of the IACK cycle.
5. D00–D07 — Data bus lines D00–D07 are used to pass the interrupt vector from the responding Interrupter to the Interrupt Handler.
6. DTACK* — Data Transfer Acknowledge asserted low signals that the Interrupter has put the vector on the data bus.

FIGURE 5 — SIMPLE VMEbus CONFIGURATION

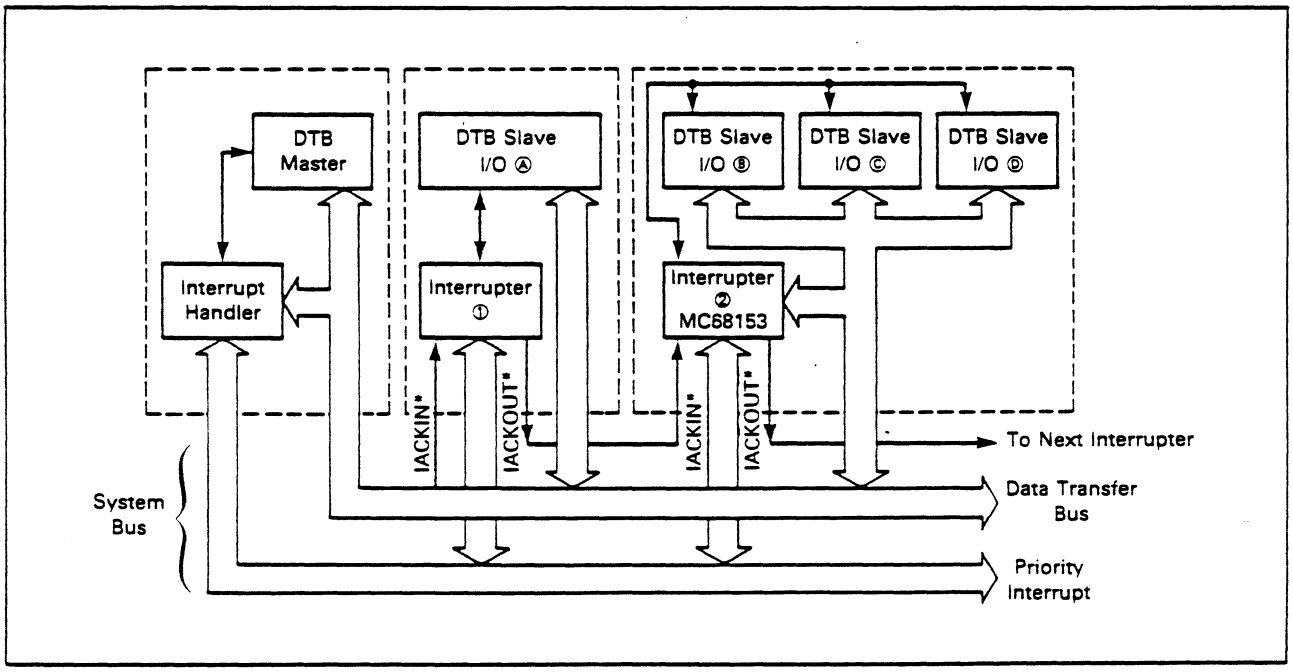
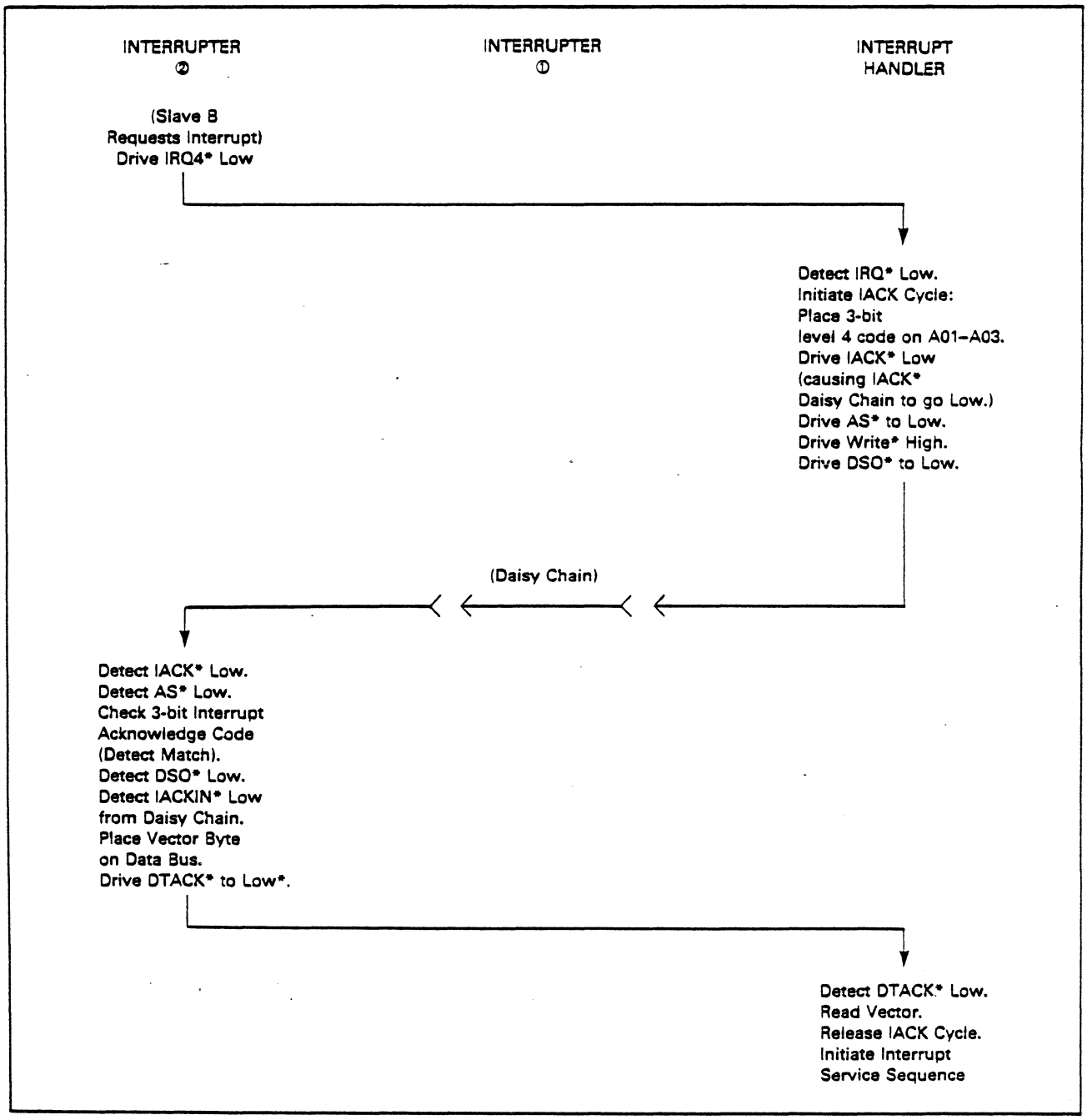


Figure 6 shows a flow diagram of a typical interrupt request and acknowledge operation. Briefly, the sequence of events is first, an Interrupter makes a request, next the Handler responds with an IACK cycle, then the Interrupter passes a vector to the Handler completing the IACK cycle, and finally the Handler uses the vector to determine additional action. Typically, an interrupt service routine is stored in software and the vector points to its starting address.

Note the daisy chain operation. If the IACK level (on A01–A03) does not match the Interrupter's request level or if no request is pending, the Interrupter passes the IACKIN* signal on and asserts IACKOUT*. This sequential action automatically prioritizes Requesters on the same level (first one in line with a request pending gets serviced) and prevents two or more Interrupters from responding simultaneously.

FIGURE 6 — INTERRUPT REQUEST AND ACKNOWLEDGE OPERATION FLOW DIAGRAM



This discussion is a very cursory look at the bus operation. For more details including situations with multiple bus masters, the user is directed to the VMEbus Specification MVMEBS or VERSAbus Specification M68KVBS. Also, the MC68153 can be used with other buses having similar interrupt structures.

BIM BUS INTERFACE

Figure 7 shows a simplified block diagram of the MC68153 interface to VERSAbus or VMEbus. Address Decode and Control Decode are dependent on the application and must be designed to guarantee BIM ac specifications. It is possible in most cases that the decode logic can be shared with the slave devices. Buffers are provided where shown to comply with bus loading and drive specifications. It is also possible that buffers can be shared with the slave bus interface.

READ/WRITE OPERATION

All eight BIM registers can be accessed from the system bus in both read and write modes. The BIM has an asynchronous bus interface, primarily designed for MC68000-like buses. The following signals generate read and write cycles: Chip Select ($\overline{CS}$), Read/Write (R/$\overline{W}$), Address Inputs (A1–A3), Data Bus (D0–D7), and Data Transfer Acknowledge ($\overline{DTACK}$). During read and write cycles the internal registers are selected by A1, A2, and A3 in compliance with the Figure 4 Truth Table.

Figure 8 shows the device timing for a read cycle. R/$\overline{W}$ and A1–A3 are latched on the falling edge of $\overline{CS}$ and must meet specified setup and hold times. Chip access time for valid data and $\overline{DTACK}$ are dependent on the clock frequency as shown in the figure.

Figure 9 shows the device timing for a write cycle. R/$\overline{W}$, A1–A3, and D0–D7 are latched on the falling edge of $\overline{CS}$ and must meet specified setup and hold times. Chip access time for $\overline{DTACK}$ is dependent on the clock frequency as shown in the figure.

FIGURE 7 — VMEbus/VERSAbus INTERFACE BLOCK DIAGRAM

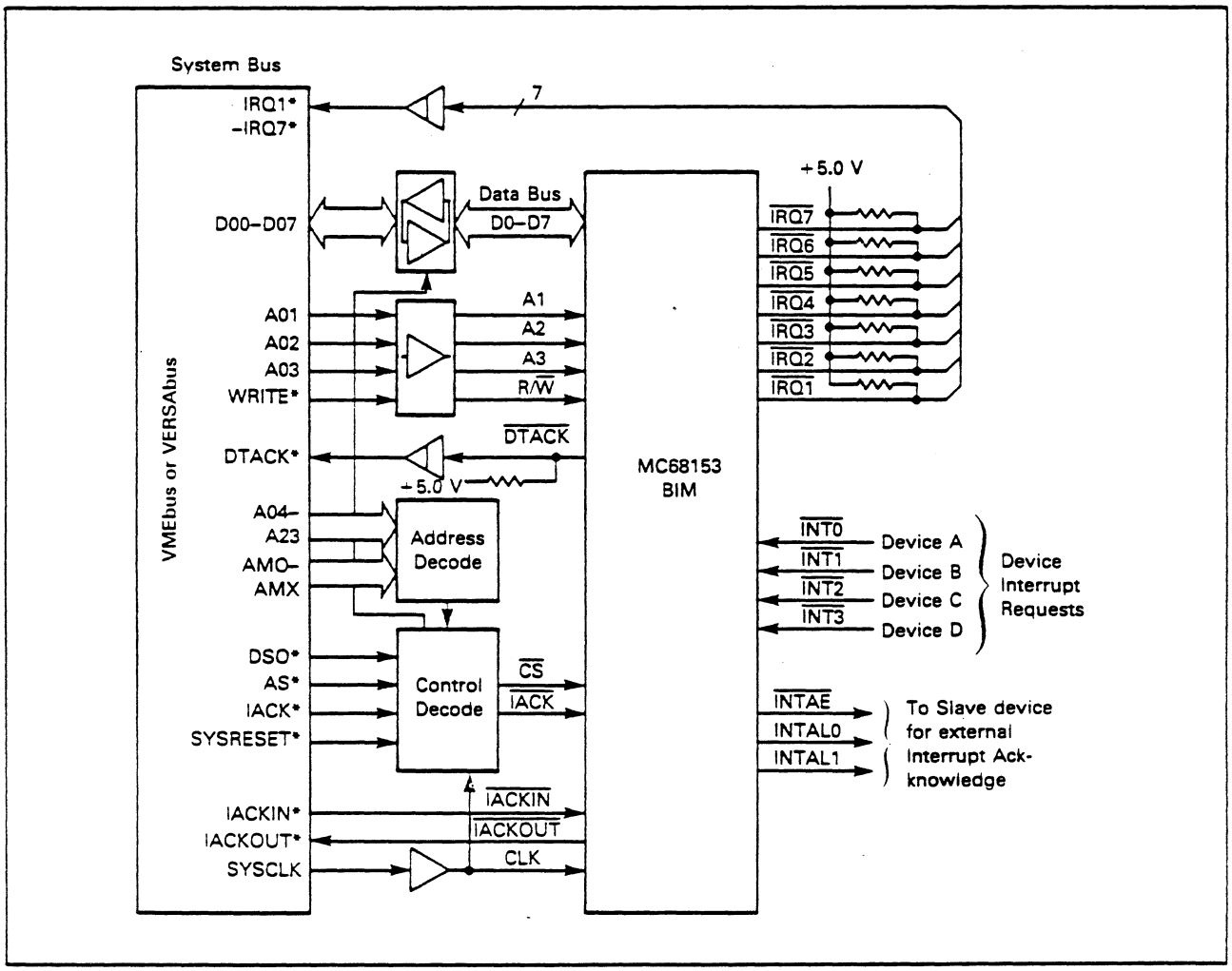


FIGURE 8 — READ CYCLE

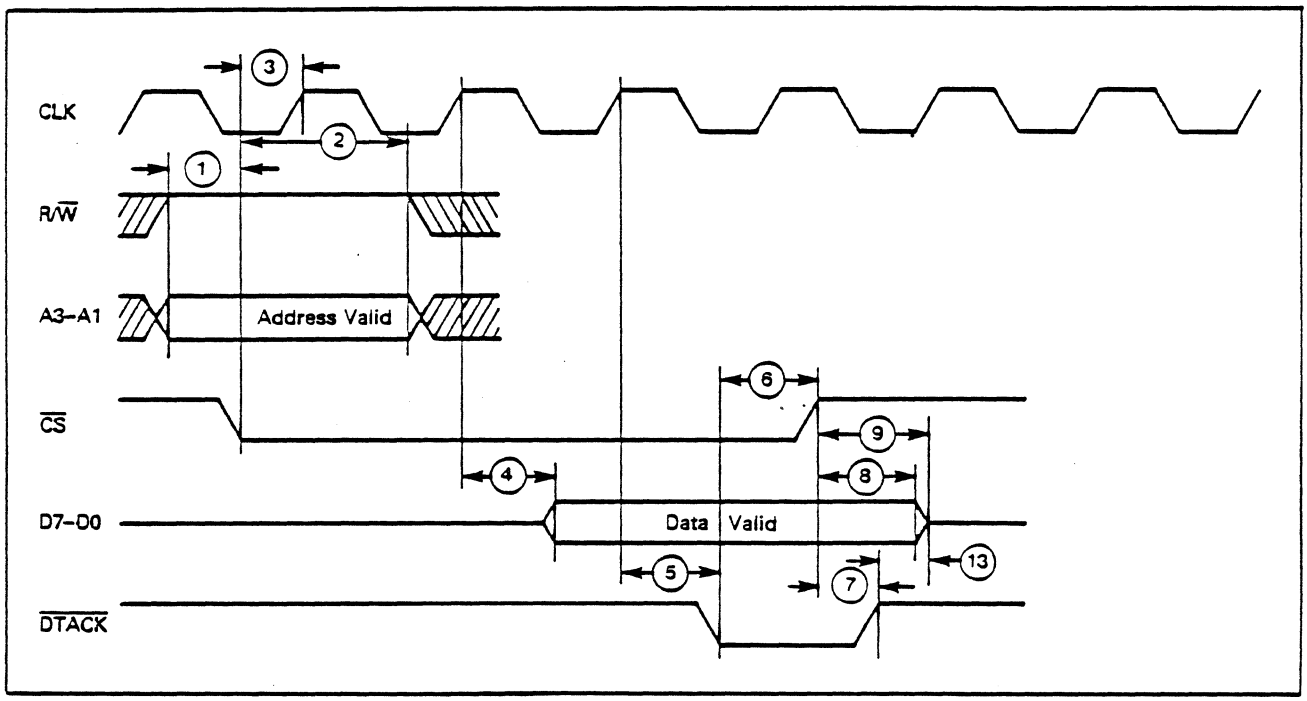
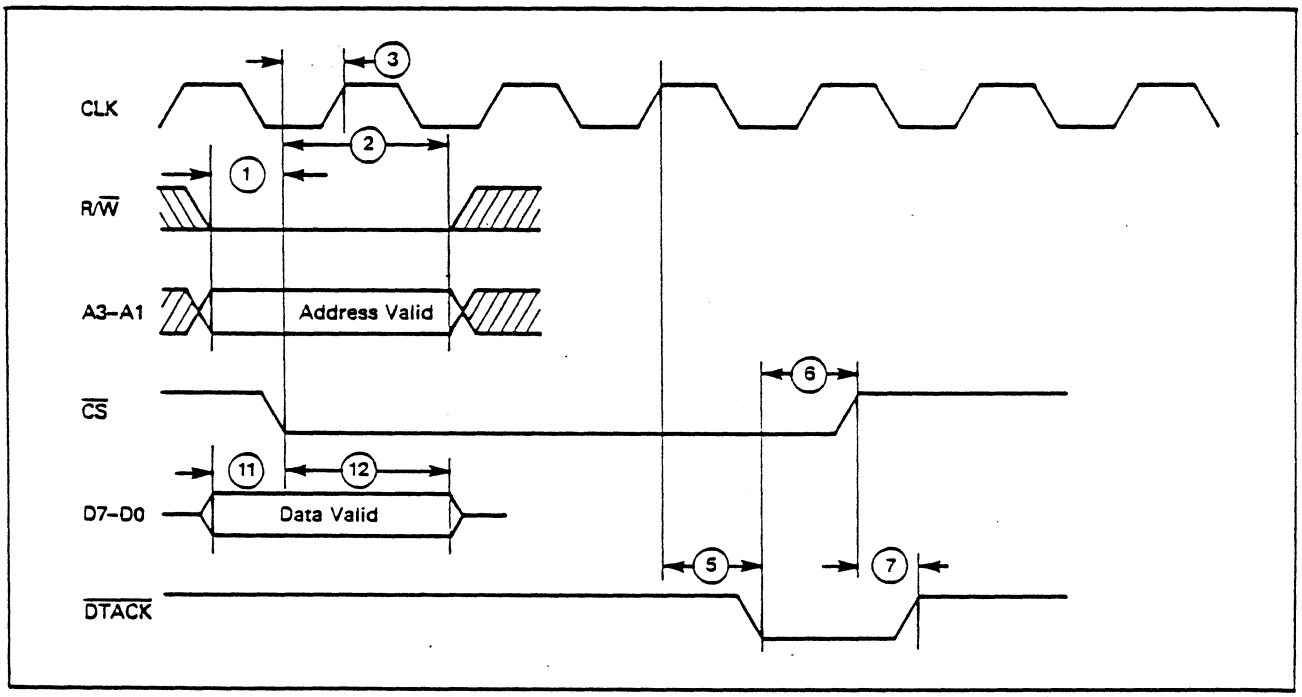


FIGURE 9 — WRITE CYCLE



INTERRUPT REQUESTS

The MC68153 accepts device interrupt requests on inputs $\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, and $\overline{INT3}$. Each input is regulated by Bit 4 (IRE) of the associated control register (CR0 controls $\overline{INT0}$, CR1 controls $\overline{INT1}$, etc). If IRE (Interrupt Enable) is set and a device input is asserted, an Interrupt Request open-collector output ($\overline{IRQ1}$–$\overline{IRQ7}$) is asserted. The asserted $\overline{IRQX}$ output is selected by the value programmed in Bits 0, 1, and 2 of the control register (L0, L1, and L2). This 3-bit field determines the interrupt request level as set by software.

Two or more interrupt sources can be programmed to the same request level. That $\overline{IRQX}$ output will remain asserted until multiple interrupt acknowledge cycles respond to all requests.

If the interrupt request level is set to zero, the interrupt is disabled because there is no corresponding IRQ output.

INTERRUPT ACKNOWLEDGE

The response of an Interrupt Handler to a bus interrupt request is an interrupt acknowledge cycle. The IACK cycle is initiated in the MC68153 by receiving $\overline{IACK}$ low. R/$\overline{W}$, A1, A2, A3 are latched, and the interrupt level on line A1–A3 is compared with any interrupt requests pending in the chip. Further activity can be one of four cases:

1. No further action required — This occurs if $\overline{IACKIN}$ is **not** asserted. Asserting $\overline{IACK}$ only starts the BIM activity. If the daisy chain signal never reaches the MC68153 ($\overline{IACKIN}$ is not asserted), another Interrupter has responded to the $\overline{IACK}$ cycle. The cycle will end, the chip $\overline{IACK}$ is negated, and no additional action is required.

2. Pass on the interrupt acknowledge daisy chain — For this case, $\overline{IACKIN}$ input is asserted by the preceding daisy chain Interrupter, and $\overline{IACKOUT}$ output is in turn asserted. The daisy chain signal is passed on when no interrupts are pending on a matching level or when any possible interrupts are disabled. The Interrupt Enable (IRE) bit of a control register can disable any interrupt requests, and in turn, any possible matches.

3. Respond internally — For this case, $\overline{IACKIN}$ is asserted and a match is found. The MC68153 completes the IACK cycle by supplying an interrupt vector from the proper vector register followed by a $\overline{DTACK}$ signal asserted. $\overline{IACKOUT}$ is not asserted because the interrupt acknowledge cycle is completed by this device.

   For the MC68153 to respond in this mode of operation, the EXTERNAL/$\overline{INTERNAL}$ control register bit (X/$\overline{IN}$) must be zero. For each source of interrupt request, the associated control register determines the BIM response to an IACK cycle, and the X/$\overline{IN}$ bit sets this response either internally (X/$\overline{IN}$ = 0) or externally (X/$\overline{IN}$ = 1).

4. Respond externally — For the final case, $\overline{IACKIN}$ is also asserted, a match is found and the associated control register has X/$\overline{IN}$ bit set to one. The MC68153 does not assert $\overline{IACKOUT}$ and does assert $\overline{INTAE}$ low. $\overline{INTAE}$ signals that the requesting device must complete the IACK cycle (supplying a vector and $\overline{DTACK}$) and that the 2-bit code contained on outputs INTAL0 and INTAL1 shows which interrupt source is being acknowledged.

These cases are discussed in more detail in the following paragraphs.

Internal Interrupt Acknowledge

For an internal interrupt acknowledge to occur, the following conditions must be met:

1. One or more device interrupt inputs ($\overline{INT0}$–$\overline{INT3}$) has been asserted and corresponding control bit IRE value is one.

2. $\overline{IACK}$ asserted.

3. A match exists between [A3, A2, A1] and the [L2, L1, L0] field of an enabled, requesting control register. If two or more devices are requesting at the same interrupt level, preference is given to the highest number requester, that is, $\overline{INT3}$ has highest priority and $\overline{INT0}$ has lowest.

4. Control register bit X/$\overline{IN}$ of matching interrupt source must be zero.

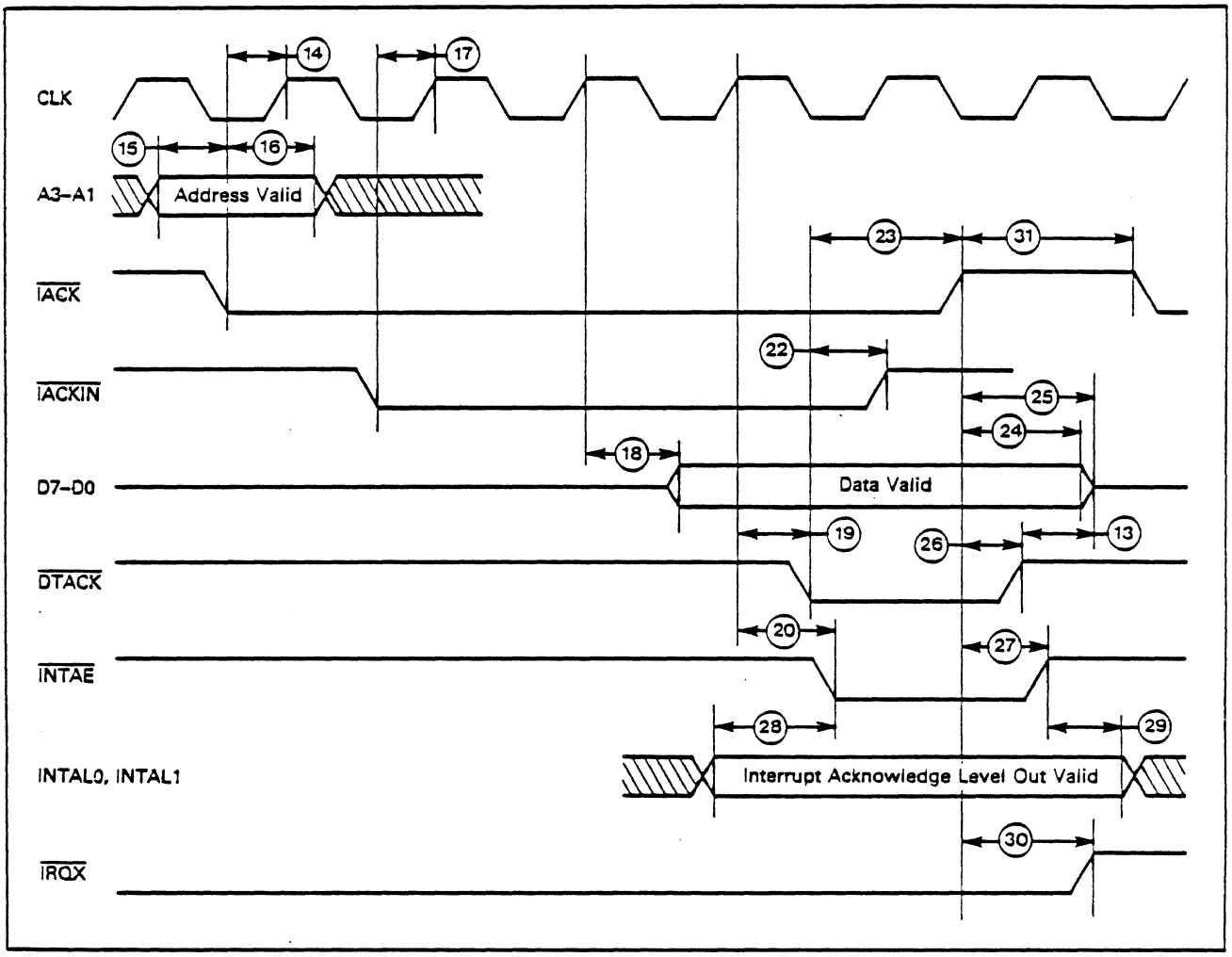
5. $\overline{IACKIN}$ asserted.

The internal interrupt acknowledge cycle timing is shown in Figure 10. The 8-bit interrupt acknowledge vector is presented to the data bus and $\overline{DTACK}$ is asserted. Note also that INTAL0 and INTAL1 are valid and $\overline{INTAE}$ is asserted during this cycle although they would normally not be used. The cycle is terminated (data and $\overline{DTACK}$ released) after $\overline{IACK}$ is negated.

During the IACK cycle, the INTERRUPT AUTO-CLEAR control bit (IRAC) comes into play. If the IRAC = one for the responding interrupt source, the INTERRUPT ENABLE (IRE) bit is automatically cleared during the IACK cycle, thus disabling the associated interrupt input and any $\overline{IRQX}$ output asserted due to this interrupt input. Before another interrupt can be requested from this source, IRE must be set to one by writing to the control register.

Note that $\overline{IACKOUT}$ is not asserted because this device is responding to the IACK and does not pass the daisy chain signal on. Also, new device interrupt requests occurring on $\overline{INT0}$–$\overline{INT3}$ after $\overline{IACK}$ is asserted are locked out to prevent any race conditions on the daisy chain.

FIGURE 10 — INTERRUPT ACKNOWLEDGE CYCLE — INTERNAL VECTOR



External Interrupt Acknowledge

For an external interrupt acknowledge, the same conditions as listed above are met with one exception. Control register bit X/$\overline{IN}$ of matching interrupt source must be set to one. The timing is shown in Figure 11. For this cycle, the interrupt vector and $\overline{DTACK}$ must be supplied by an external device. $\overline{INTAE}$ is asserted indicating that INTAL0 and INTAL1 are valid. The external device can use these signals to enable the vector and $\overline{DTACK}$. The cycle is terminated after $\overline{IACK}$ is negated.

The IRAC control bit acts in the external interrupt acknowledge the same as described for the internal response (see above). Also, $\overline{IACKOUT}$ is not asserted and new device interrupts are disabled for reasons discussed above.

Pass On IACK Daisy Chain

If the MC68153 has no interrupt request pending at the same level as the interrupt acknowledge, the IACK daisy chain signal is passed on to the next device if $\overline{IACKIN}$ is asserted. The following conditions are thus met:

1. $\overline{IACK}$ asserted.
2. No match exists between [A3, A2, A1] and the [L2, L1, L0] field of an enabled, requesting control register.
3. $\overline{IACKIN}$ is asserted.

$\overline{IACKOUT}$ is asserted if these conditions are valid. This output drives $\overline{IACKIN}$ of the next Interrupter on the daisy chain, passing the signal along. Figure 12 shows the timing for this case. $\overline{IACKOUT}$ is negated after $\overline{IACK}$ is negated.

FIGURE 11 — INTERRUPT ACKNOWLEDGE CYCLE — EXTERNAL VECTOR

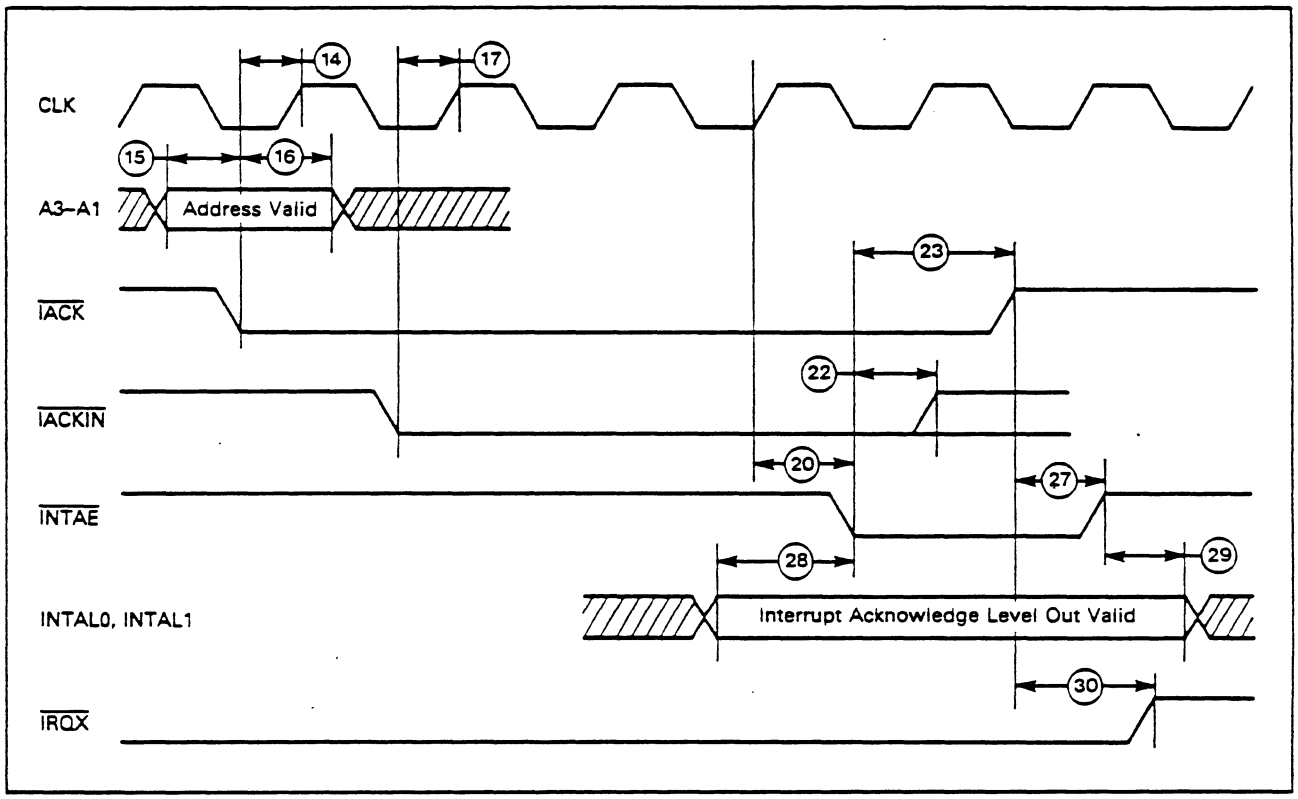
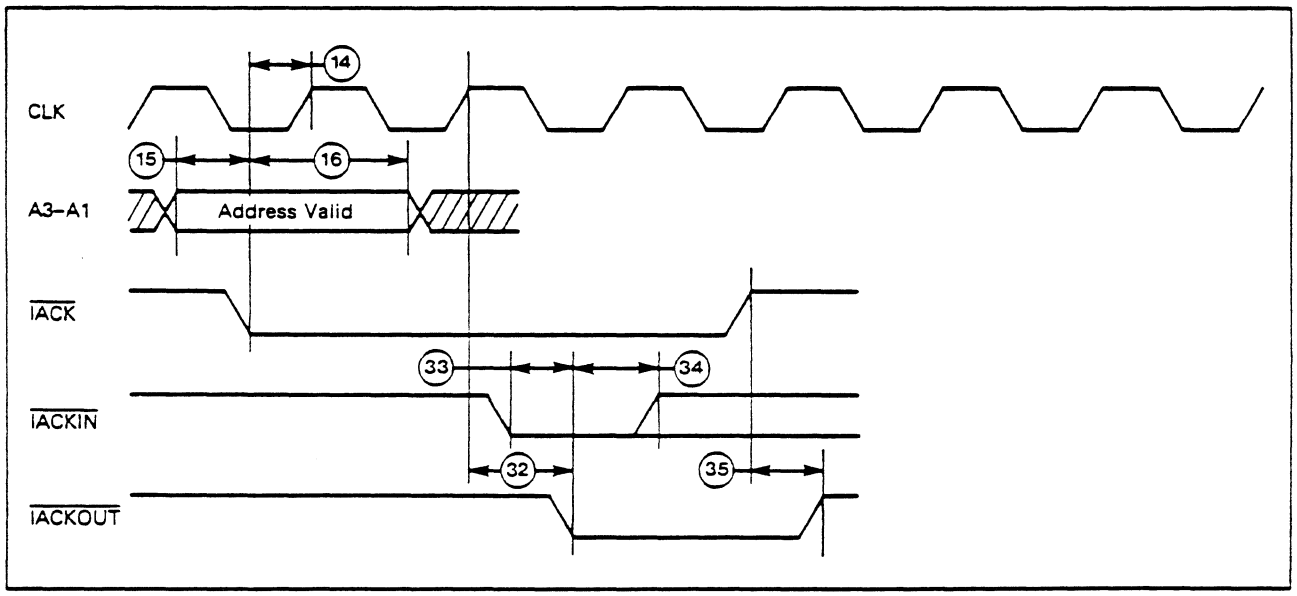


FIGURE 12 — INTERRUPT ACKNOWLEDGE CYCLE — $\overline{\text{IACKOUT}}$



CONTROL REGISTER FLAGS

Each control register contains a Flag bit (F) and a Flag Auto-Clear bit (FAC). Both bits can be read or altered via a register write without affecting the interrupt operation of the device. The Flag is useful as a status indicator for resource management and as a semaphor in multitasking or multiprocessor systems. Flag (F) is located in bit position 7 and can be used with the MC68000 Test and Set (TAS) instruction.

The Flag Auto-Clear (FAC) is used to manipulate the Flag bit. If the Flag is set to one and the FAC is also one, an interrupt acknowledge cycle to the associated interrupt source clears the Flag bit. This feature is useful in determining the interrupt status and passing messages.

RESET

There is no reset input, however, a chip reset is activated by asserting both $\overline{CS}$ and $\overline{IACK}$ simultaneously (Figure 13). These inputs should be held low for a minimum of two clock cycles for a full reset function. The control registers are reset to all zeroes and the Vector Registers are set to a value of $0F. This vector value is the uninitialized vector for the MC68000. See the MC68000 Users Manual for more details on this vector.

CLOCK

The chip clock is required for internal operation to occur. Typical frequency is 16 MHz in VMEbus and VERSAbus applications derived from the system clock. Any frequency can be used, however, up to 25 MHz (Figure 14).

FIGURE 13 — RESET

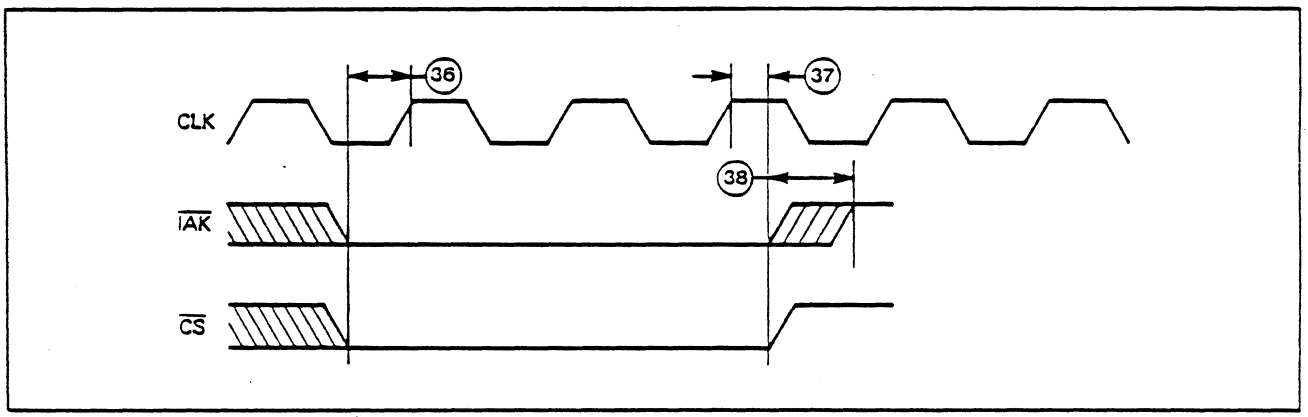


FIGURE 14 — CLOCK WAVEFORM

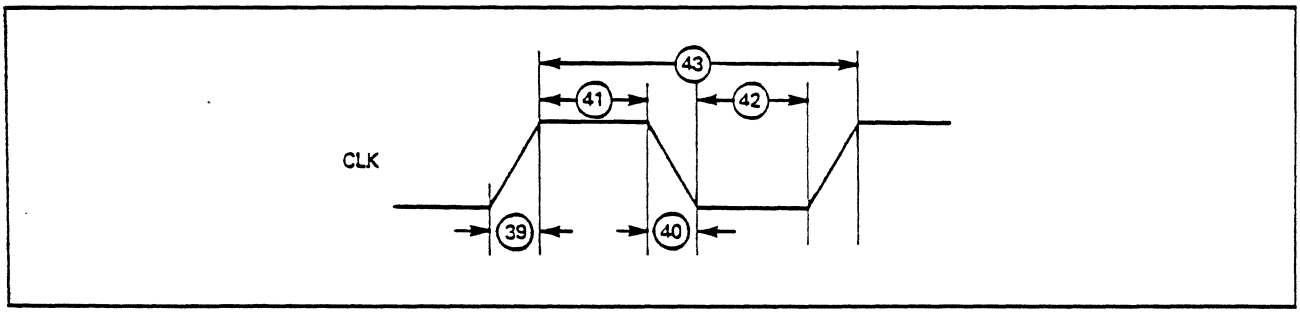


TABLE 1
AC PERFORMANCE SPECIFICATIONS
(V_{CC} = 5.0 V ±5%, T_A = 0°C to 70°C)

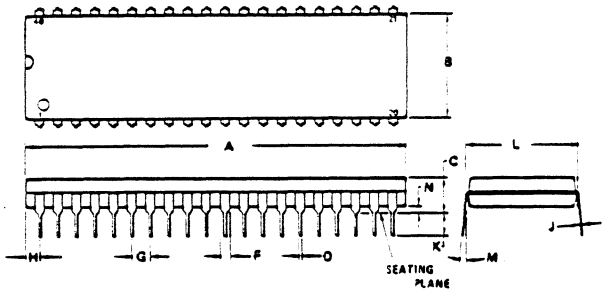
Number	Characteristic	Min	Max	Units	Notes
1	R/$\overline{W}$, A1–A3 Valid to $\overline{CS}$ Low (Setup Time)	10	—	ns	
2	$\overline{CS}$ Low to R/$\overline{W}$, A1–A3 Invalid (Hold Time)	5.0	—	ns	
3	$\overline{CS}$ Low to CLK High (Setup Time)	15	—	ns	1
4	CLK High to Data Out Valid (Delay)	—	55	ns	2
5	CLK High to $\overline{DTACK}$ Low (Delay)	—	40	ns	2
6	$\overline{DTACK}$ Low to $\overline{CS}$ High	0		ns	
7	$\overline{CS}$ High to $\overline{DTACK}$ High (Delay)	—	35	ns	10
8	$\overline{CS}$ High to Data Out Invalid (Hold Time)	0	—	ns	
9	$\overline{CS}$ High to Data Out High-Impedance (Hold Time)	—	50	ns	
10	$\overline{CS}$ High to $\overline{CS}$ or $\overline{IACK}$ Low	20	—	ns	
11	Data In Valid to $\overline{CS}$ Low (Setup Time)	10	—	ns	
12	$\overline{CS}$ Low to Data In Invalid (Hold Time)	5.0	—	ns	
13	$\overline{DTACK}$ High to Data Out High-Impedance	—	25	ns	10
14	$\overline{IACK}$ Low to CLK High (Setup Time)	15	—	ns	1
15	A1–A3 Valid to $\overline{IACK}$ Low (Setup Time)	10	—	ns	
16	$\overline{IACK}$ Low to A1–A3 Invalid (Hold Time)	5.0	—	ns	
17	$\overline{IACKIN}$ Low to CLK High (Setup Time)	15	—	ns	1, 8
18	CLK High to Data Out Valid (Delay)	—	55	ns	3
19	CLK High to $\overline{DTACK}$ Low (Delay)	—	40	ns	3
20	CLK High to $\overline{INTAE}$ Low (Delay)	—	40	ns	3
22	$\overline{DTACK}$ Low to $\overline{IACKIN}$ High	0	—	ns	8
23	$\overline{DTACK}$ Low to $\overline{IACK}$ High	0	—	ns	
24	$\overline{IACK}$ High to Data Out Invalid (Hold Time)	0	—	ns	
25	$\overline{IACK}$ High to Data Out High Impedance (Delay)	—	60	ns	
26	$\overline{IACK}$ High to $\overline{DTACK}$ High (Delay)	—	45	ns	10
27	$\overline{IACK}$ High to $\overline{INTAE}$ High (Delay)	—	35	ns	
28	INTAL0, INTAL1 Valid to $\overline{INTAE}$ Low (Setup Time)	1.0	2.0	CLK Per	
29	$\overline{INTAE}$ High to INTAL0, INTAL1 Invalid (Hold Time)	1.0	2.0	CLK Per	
30	$\overline{IACK}$ High to $\overline{IRQx}$ High (Delay)	—	50	ns	7, 10
31	$\overline{IACK}$ High to $\overline{IACK}$ or $\overline{CS}$ Low	20	—	ns	
32	CLK High to $\overline{IACKOUT}$ Low (Delay)	—	40	ns	5
33	$\overline{IACKIN}$ Low to $\overline{IACKOUT}$ Low (Delay)	—	30	ns	4, 8
34	$\overline{IACKOUT}$ Low to $\overline{IACKIN}$, $\overline{IACK}$ High	0	—	ns	8
35	$\overline{IACK}$ High to $\overline{IACKOUT}$ High (Delay)	—	35	ns	
36	$\overline{IACK}$ and $\overline{CS}$ both Low to CLK High (Setup Time)	15	—	ns	9
37	CLK High to $\overline{IACK}$ or $\overline{CS}$ High (Hold Time)	0	—	ns	
38	$\overline{IACK}$ or $\overline{CS}$ High to $\overline{IACK}$ and $\overline{CS}$ High (Skew)	—	1.0	CLK Per	6
39	Clock Rise Time	—	10	ns	
40	Clock Fall Time	—	10	ns	
41	Clock High Time	20	—	ns	
42	Clock Low Time	20	—	ns	
43	Clock Period	40	—	ns	

NOTES:

1. This specification only applies if the VBIM had completed all operations initiated by the previous bus cycle when $\overline{CS}$ or $\overline{IACK}$ was asserted. Following a normal bus cycle, all operations are completed within 2 clock cycles after $\overline{CS}$ or $\overline{IACK}$ have been negated. If $\overline{IACK}$ or $\overline{CS}$ is asserted prior to completion of these operations, the new cycle, and hence, $\overline{DTACK}$ is postponed.

   If the $\overline{IACK}$, $\overline{IACKIN}$ or $\overline{CS}$ setup time is violated, $\overline{DTACK}$ may be asserted as shown, or may be asserted one clock cycle later (i.e. $\overline{IACK}$ will not be recognized until the next rising edge of the clock).
2. Assumes that 3 has been met.
3. Assumes that 14 and 17 have both been met.
4. Assumes that 14 has been met. ($\overline{IACKOUT}$ cannot go low prior to $\overline{IACKIN}$ going low).
5. Assumes that 14 has been met and $\overline{IACKIN}$ has been low for at least the amount of time specified by 33.
6. 38 is the minimum skew between the last moment when both $\overline{IACK}$ and $\overline{CS}$ are asserted to when both are negated, to insure that an access cycle is not unintentionally started.
7. Assumes no other $\overline{INTx}$ input is causing $\overline{IRQx}$ to be driven low.
8. In non-daisy chain systems, $\overline{IACKIN}$ may be tied low.
9. Failure to meet this spec. causes RESET to be ignored for 1 clock period. It is then necessary to keep these signals low for 3 clock periods instead of 2.
10. Delay time is specified from input signal to Open-Collector Output pulled High thru 1.0 kΩ resistor to +6.5 V.

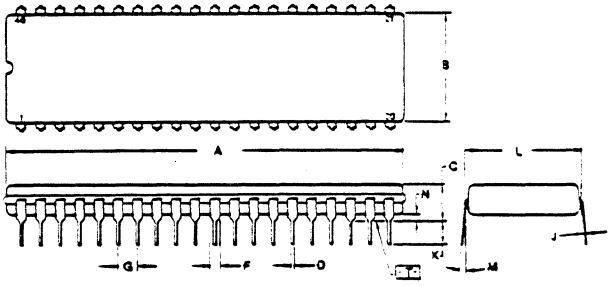
OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

CASE 711-03
PLASTIC PACKAGE



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.31	53.24	2.020	2.096
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS: ⌖ Ø 0.25(0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONS A AND B INCLUDE MENISCUS.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

CASE 734-04
CERAMIC PACKAGE

TYPICAL THERMAL CHARACTERISTICS

Package	θ_{JA} (Junction to Ambient) Still Air	Junction Temperature Still Air @ 70°C Ambient
L Suffix	40°C/W	147°C
P Suffix	35°C/W	137°C

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SEMICONDUCTORS
5001 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MC68230L8
MC68230L10

Advance Information

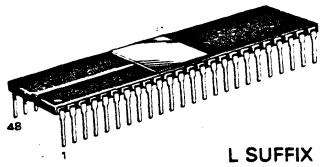
HMOS
(HIGH-DENSITY N-CHANNEL SILICON-GATE)

PARALLEL INTERFACE/TIMER

MC68230 PARALLEL INTERFACE/TIMER

The MC68230 Parallel Interface/Timer provides versatile double buffered parallel interfaces and an operating system oriented timer to MC68000 systems. The parallel interfaces operate in unidirectional or bidirectional modes, either 8 or 16 bits wide. In the unidirectional modes, an associated data direction register determines whether the port pins are inputs or outputs. In the bidirectional modes the data direction registers are ignored and the direction is determined dynamically by the state of four handshake pins. These programmable handshake pins provide an interface flexible enough for connection to a wide variety of low, medium, or high speed peripherals or other computer systems. The PI/T ports allow use of vectored or autovectored interrupts, and also provide a DMA Request pin for connection to the MC68450 Direct Memory Access Controller or a similar circuit. The PI/T timer contains a 24-bit wide counter and a 5-bit prescaler. The timer may be clocked by the system clock (PI/T CLK pin) or by an external clock (TIN pin), and a 5-bit prescaler can be used. It can generate periodic interrupts, a square wave, or a single interrupt after a programmed time period. Also it can be used for elapsed time measurement or as a device watchdog.

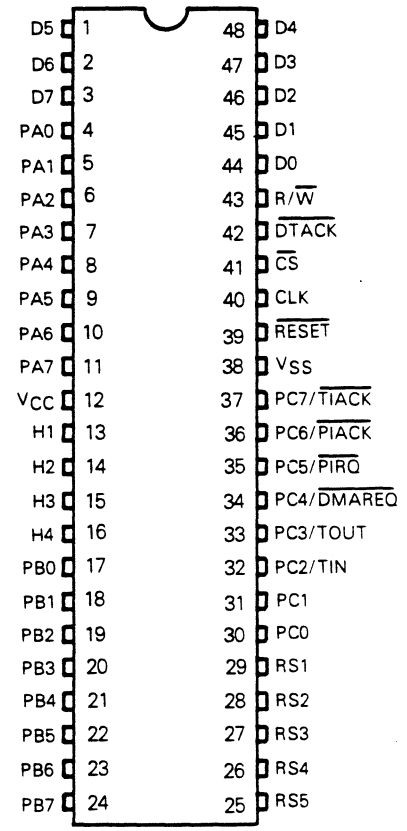
- MC68000 Bus Compatible
- Port Modes Include:
  - Bit I/O
  - Unidirectonal 8-Bit and 16-Bit
  - Bidirectional 8-Bit and 16-Bit
- Selectable Handshaking Options
- 24-Bit Programmable Timer
- Software Programmable Timer Modes
- Contains Interrupt Vector Generation Logic
- Separate Port and Timer Interrupt Service Requests
- Registers are Read/Write and Directly Addressable
- Registers are Addressed for MOVEP (Move Peripheral) and DMAC Compatibility



L SUFFIX
CERAMIC PACKAGE
CASE 740

P SUFFIX
PLASTIC PACKAGE
AVAILABLE 2Q82

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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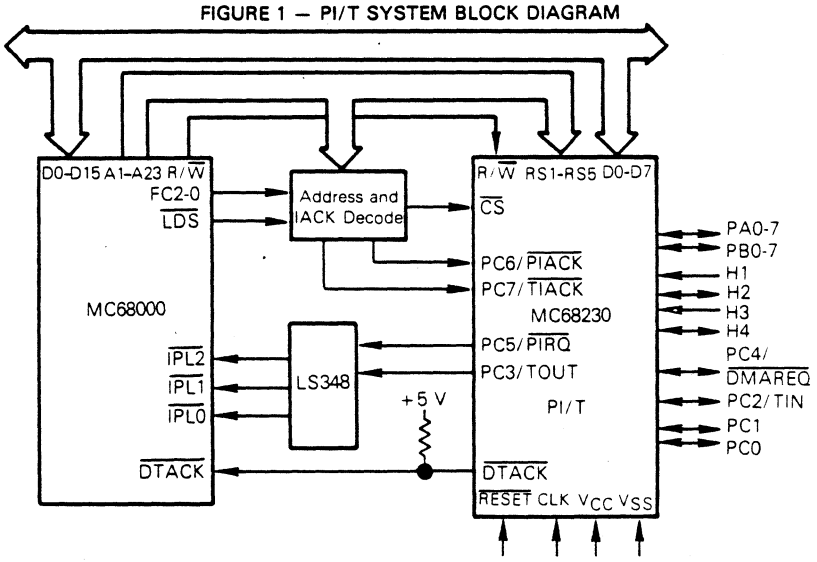
FIGURE 1 — PI/T SYSTEM BLOCK DIAGRAM



POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A ≡ Ambient Temperature, °C

θ_{JA} ≡ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{PORT}$

$P_{INT} \equiv I_{CC} \times V_{CC}$, Watts — Chip Internal Power

P_{PORT} ≡ Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Rating
Thermal Resistance Ceramic	θ_{JA}	50	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precuations be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

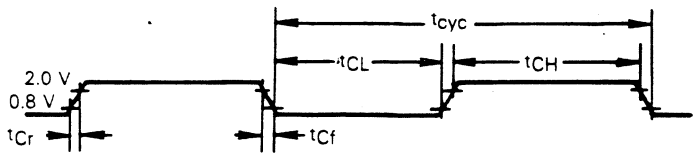
DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5%, T_A = 0 to 70°C unless otherwise noted)

Characteristics		Symbol	Min	Max	Unit
Input High Voltage	All Inputs	V_{IH}	V_{SS}+2.0	V_{CC}	V
Input Low Voltage	All Inputs	V_{IL}	V_{SS}−0.3	V_{SS}+0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V)	H1, H3, R/$\overline{W}$, $\overline{RESET}$, CLK, RS1-RS5, $\overline{CS}$	I_{in}	–	10.0	μA
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4)	$\overline{DTACK}$, PC0-PC7, D0-D7 H2, H4, PA0-PA7, PB0-PB7	I_{TSI}	– −0.1	20 −1.0	μA mA
Output High Voltage (I_{Load} = −400 μA, V_{CC} = min) (I_{Load} = −150 μA, V_{CC} = min) (I_{Load} = −100 μA, V_{CC} = min)	$\overline{DTACK}$, D0-D7 H2, H4, PB0-PB7, PA0-PA7 PC0-PC7	V_{OH}	V_{SS}+2.4	–	V
Output Low Voltage (I_{Load} = 8.8 mA, V_{CC} = min) (I_{Load} = 5.3 mA, V_{CC} = min) (I_{Load} = 2.4 mA, V_{CC} = min)	PC3/TOUT, PC5/$\overline{PIRQ}$ D0-D7, $\overline{DTACK}$ PA0-PA7, PB0-PB7, H2, H4, PC0-PC2, PC4, PC6, PC7	V_{OL}	–	0.5	V
Internal Power Dissipation (Measured at T_A = 0°C)		P_{INT}	–	500	mW
Input Capacitance (V_{in} = 0, T_A = 25°C, f = 1 MHz)		C_{in}	–	15	pF

CLOCK TIMING (See Figure 2)

Characteristic	Symbol	8 MHz MC68230L8		10 MHz MC68230L10		Unit
		Min	Max	Min	Max	
Frequency of Operation	f	2.0	8.0	2.0	10.0	MHz
Cycle Time	t_{cyc}	125	500	100	500	ns
Clock Pulse Width	t_{CL} t_{CH}	55 55	250 250	45 45	250 250	ns
Clock Rise and Fall Times	t_{Cr} t_{Cf}	– –	10 10	– –	10 10	ns

FIGURE 2 — INPUT CLOCK WAVEFORM



AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5%, V_S = 0 Vdc, T_A = 0°C to 70°C)

Number	Characteristic	8 MHz MC68230L8		10 MHz MC68230L10		Unit
		Min	Max	Min	Max	
1	R/$\overline{W}$, RS1-RS5 Valid to $\overline{CS}$ Low (Setup Time)	0	–	0	–	ns
2(10)	$\overline{CS}$ Low to R/$\overline{W}$ and RS1-RS5 Invalid (Hold Time)	100	–	65	–	ns
3(1)	$\overline{CS}$ Low to CLK Low (Setup Time)	30	–	20	–	ns
4(2)	$\overline{CS}$ Low to data Out Valid (Delay)	–	75	–	60	ns
5	RS1-RS5 Valid to Data Out Valid (Delay)	–	140	–	100	ns
6	CLK Low to $\overline{DTACK}$ Low (Read/Write Cycle) (Delay)	0	70	0	60	ns
7(3)	DTACK Low to $\overline{CS}$ High (Hold Time)	0	–	0	–	ns
8	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to Data Out Invalid (Hold Time)	0	–	0	–	ns
9	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to D0-D7 High-Impedance (Delay)	–	50	–	45	ns
10	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to DTACK High (Delay)	–	50	–	30	ns
11	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to $\overline{DTACK}$ High Impedance (Delay)	–	100	–	55	ns
12	Data Invalid to $\overline{CS}$ Low (Setup Time)	0	–	0	–	ns
13	$\overline{CS}$ Low to Data In INvalid (Hold Time)	100	–	65	–	ns
14	Input Data Valid to H1(H3) Asserted (Setup Time)	100	–	60	–	ns
15	H1(H3) Asserted to Input Data Invalid (Hold Time)	20	–	20	–	ns
16	Handshake Input H1(H4) Pulse Width Asserted	40	–	40	–	ns
17	Handshake Input (H1-H4) Pulse Width Negated	40	–	40	–	ns
18	H1(H3) Asserted to H2(H4) Negated (Delay)	–	150	–	120	ns
19	CLK Low to H2(H4) Asserted (Delay)	–	100	–	100	ns
20(4)	H2(H4) Asserted to H1(H3) Asserted	0	–	0	–	ns
21(5)	CLK Low to H2(H4) Pulse Negated (Delay)	–	125	–	125	ns
22(9, 11)	Synchronized H1(H3) to CLK Low on which $\overline{DMAREQ}$ is Asserted (See Figures 13 and 14)	2.5	3.5	2.5	3.5	CLK Per
23	CLK Low $\overline{DMAREQ}$ is Asserted to CLK Low on which $\overline{DMAREQ}$ is Negated	3	3	3	3	CLK Per
24	CLK Low to Output Data Valid (Delay) (Modes 0, 1)	–	150	–	120	ns
25(9, 11)	Synchronized H1(H3) to Output Data Invalid (Modes 0, 1)	1.5	2.5	1.5	2.5	CLK Per
26	H1 Negated to Output Data Valid (Modes 2, 3)	–	70	–	50	ns
27	H1 Asserted to Output Data High Impedance (Modes 2, 3)	0	70	0	70	ns
28	Read Data Valid to $\overline{DTACK}$ Low (Setup Time)	0	–	0	–	ns
29	CLK Low to Data Output Valid (Interrupt Acknowledge Cycle)	–	120	–	100	ns
30(7)	H1(H3) Asserted to CLK High (Setup Time)	50	–	40	–	ns
31	$\overline{PIACK}$ or $\overline{TIACK}$ Low to CLK Low (Setup Time)	50	–	40	–	ns
32(11)	Synchronized $\overline{CS}$ to CLK Low on which $\overline{DMAREQ}$ is Asserted (See Figures 13 and 14)	3	3	3	3	CLK Per
33(9, 11)	Synchronized H1(H3) to CLK Low on which H2(H4) is Asserted	3.5	4.5	3.5	4.5	CLK Per
34	CLK Low to $\overline{DTACK}$ Low (Interrupt Acknowledge Cycle (Delay)	–	75	–	60	ns
35	CLK Low to $\overline{DMAREQ}$ Low (Delay)	0	120	0	100	ns
36	CLK Low to $\overline{DMAREQ}$ High (Delay)	0	120	0	100	ns
–	CLK Low to $\overline{PIRQ}$ Low or High Impedance	–	200	–	150	ns
–(8)	TIN Frequency (External Clock) – Prescaler Used	0	1	0	1	Fclk(Hz)(6)
–	TIN Frequency (External Clock) – Prescaler Not used	0	1/32	0	1/32	Fclk(Hz)(6)
–	TIN Pulse Width High or Low (External Clock)	55	–	45	–	ns
–	TIN Pulse Width Low (Run/Halt Control)	1	–	1	–	CLK
–	CLK Low to TOUT High, Low, or High Impedance	0	200	0	150	ns
–	$\overline{CS}$, $\overline{PIACK}$, or $\overline{TIACK}$ High to $\overline{CS}$, $\overline{PIACK}$, or $\overline{TIACK}$ Low	50	–	30	–	ns

NOTES:

1. This specification only applies if the PI/T had completed all operations initiated by the previous bus cycle when $\overline{CS}$ was asserted. Following a normal read or write bus cycle, all operations are complete within three CLKs after the falling edge of the CLK pin on which $\overline{DTACK}$ was asserted. If $\overline{CS}$ is asserted prior to completion of these operations, the new bus cycle, and hence, $\overline{DTACK}$ is postponed.

   If all operations of the previous bus cycle were complete when $\overline{CS}$ was asserted, this specification is made only to insure that $\overline{DTACK}$ is asserted with respect to the falling edge of the CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the $\overline{CS}$ setup time is violated, $\overline{DTACK}$ may be asserted as shown, or may be asserted one clock cycle later.

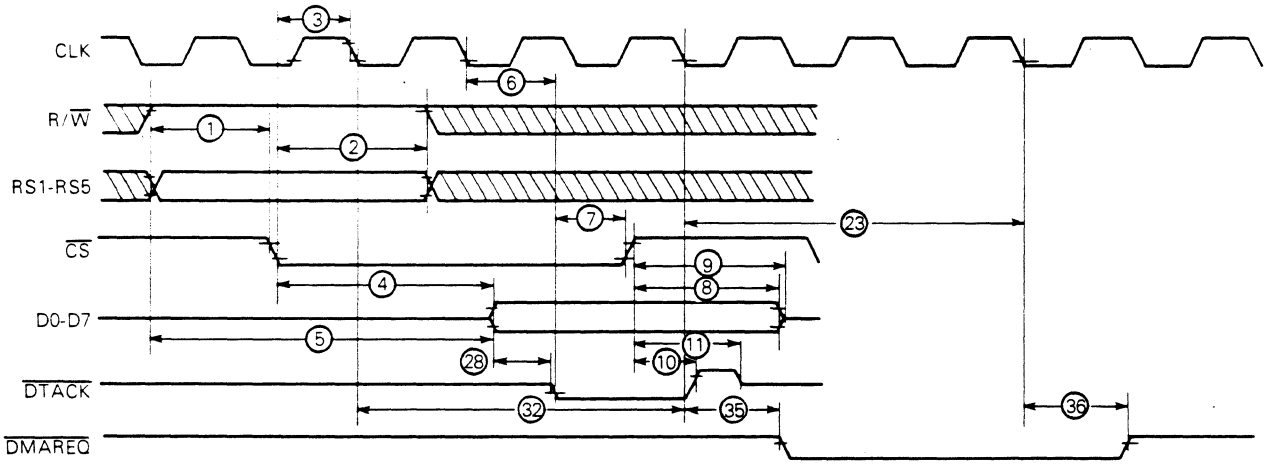
2. Assuming the RS1-RS5 to Data Valid time has also expired.

3. This specification imposes a lower bound on $\overline{CS}$ low time, guaranteeing that $\overline{CS}$ will be low for at least 1 CLK period.
4. This specification assures recognition of the asserted edge of H1(H3).
5. This specification applies only when a pulsed handshake option is chosen and the pulse is not shortened due to an early asserted edge of H1(H3).
6. CLK refers to the actual frequency of the CLK pin, not the maximum allowable CLK frequency.
7. If the setup time on the rising edge of the clock is violated, H1(H3) may not be recognized until the next rising of the clock.
8. This limit applies to the frequency of the signal at TIN compared to the frequency of the CLK signal during each clock cycle. If any period of the waveform at TIN is smaller than the period of the CLK signal at that instant, then it is likely that the timer circuit will completely ignore one cycle of the TIN signal.

   If these two signals are derived from different sources they will have different instantaneous frequency variations. In this case the frequency applied to the TIN pin must be distinctly less than the frequency at the CLK pin to avoid lost cycles of the TIN signal. With signals derived from different crystal oscillators applied to the TIN and CLK pins with fast rise and fall times, the TIN frequency can approach 80 to 90% of the frequency of the CLK signal without a loss of a cycle of the TIN signal.

   If these two signals are derived from the same frequency source then the frequency of the signal applied to TIN can be 100% of the frequency at the CLK pin. They may be generated by different buffers from the same signal or one may be an inverted version of the other. The TIN signal may be generated by an 'AND' function of the clock and a control signal.
9. The maximum value is caused by a peripheral access (H1(H3) asserted) and bus access ($\overline{CS}$ asserted) occurring at the same time.
10. See BUS INTERFACE CONNECTION section for exception.
11. Synchronized means that the input signal has been seen by the PI/T on the appropriate edge of the clock (rising edge for H1(H3) and falling edge for $\overline{CS}$). (Refer to the BUS INTERFACE CONNECTION section for the exception concerning $\overline{CS}$.)

FIGURE 3 — BUS READ CYCLE TIMING



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 4 — BUS WRITE CYCLE TIMING

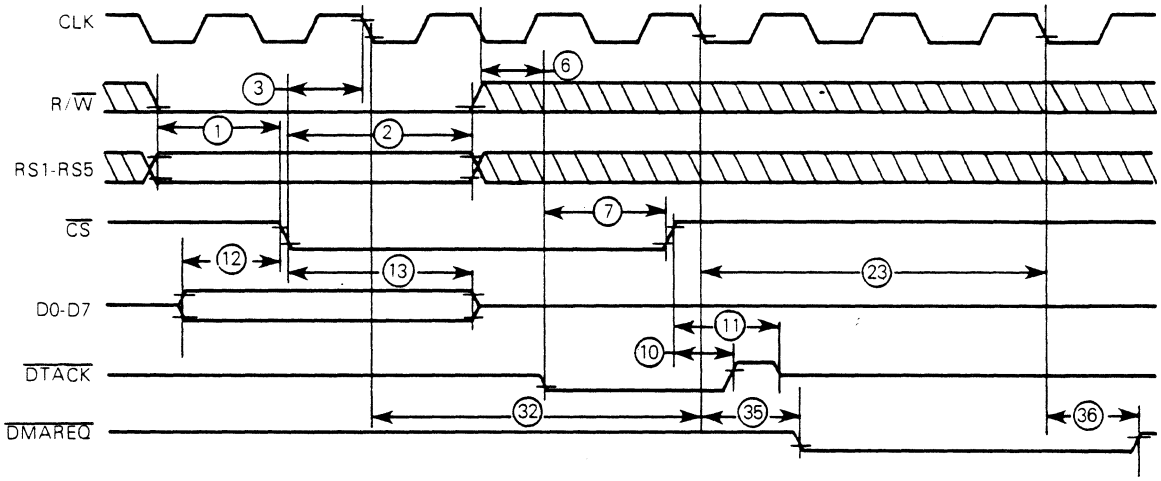
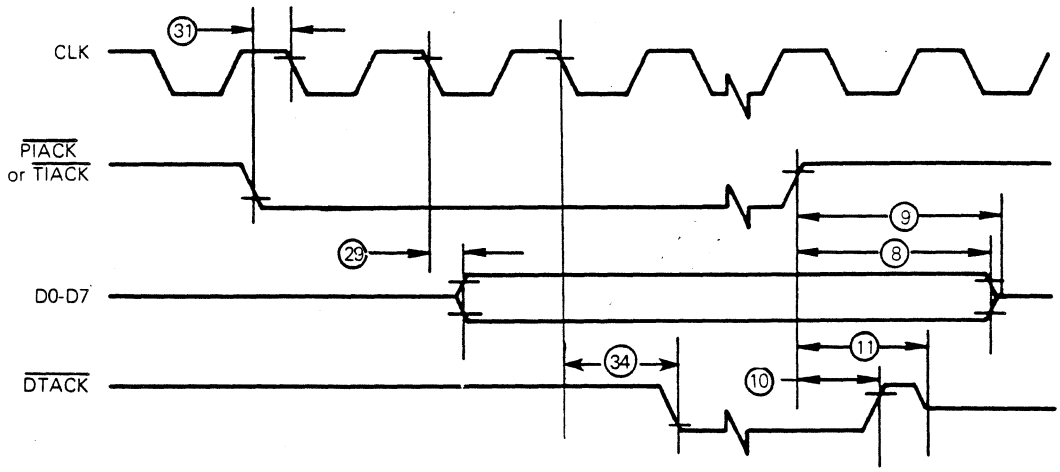
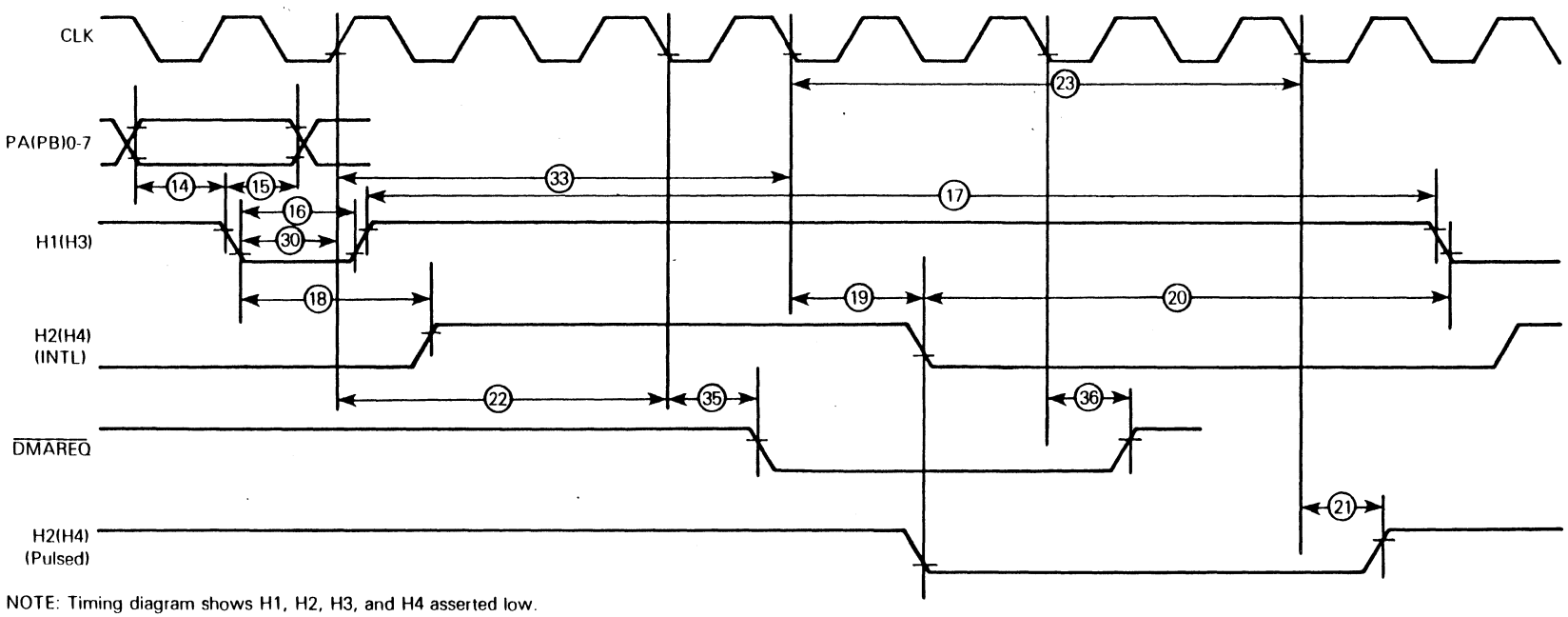


FIGURE 5 — INTERRUPT ACKNOWLEDGE
FUNCTIONAL TIMING DIAGRAM



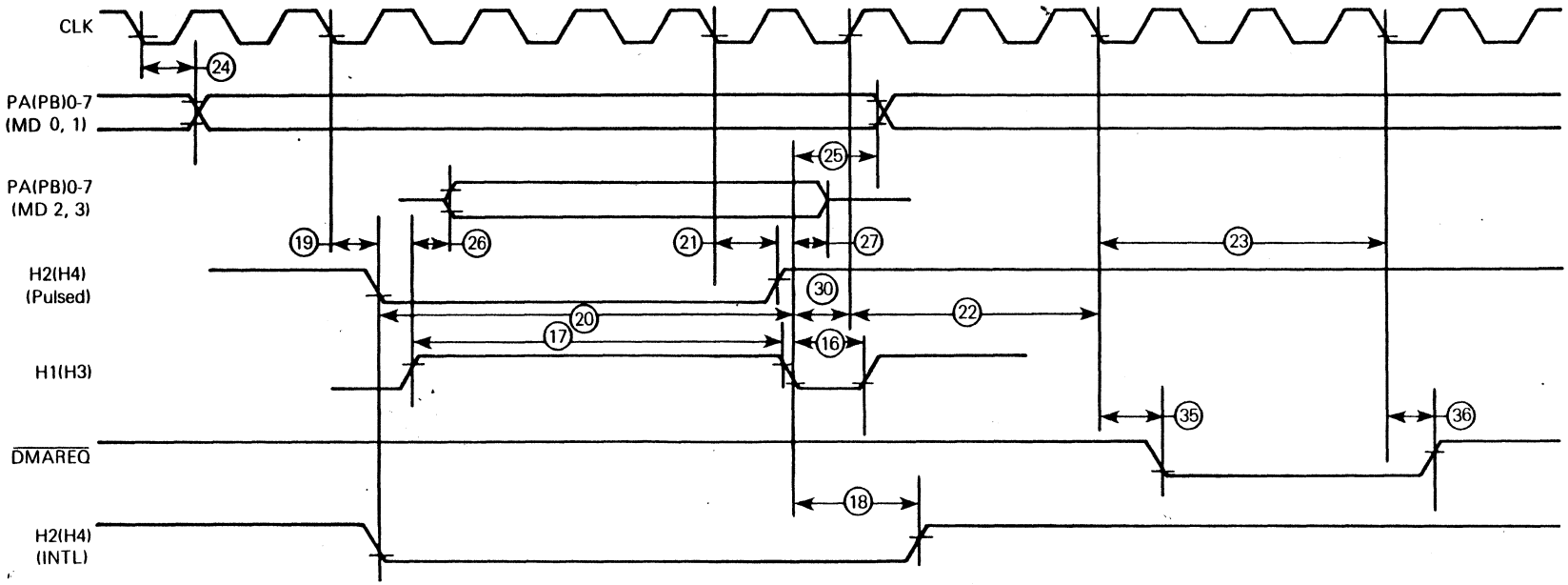
Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 6 – PERIPHERAL INTERFACE INPUT TIMING



NOTE: Timing diagram shows H1, H2, H3, and H4 asserted low.

FIGURE 7 — PERIPHERAL INTERFACE OUTPUT TIMING



NOTE: Timing diagram shows H1, H2, H3, and H4 asserted low.

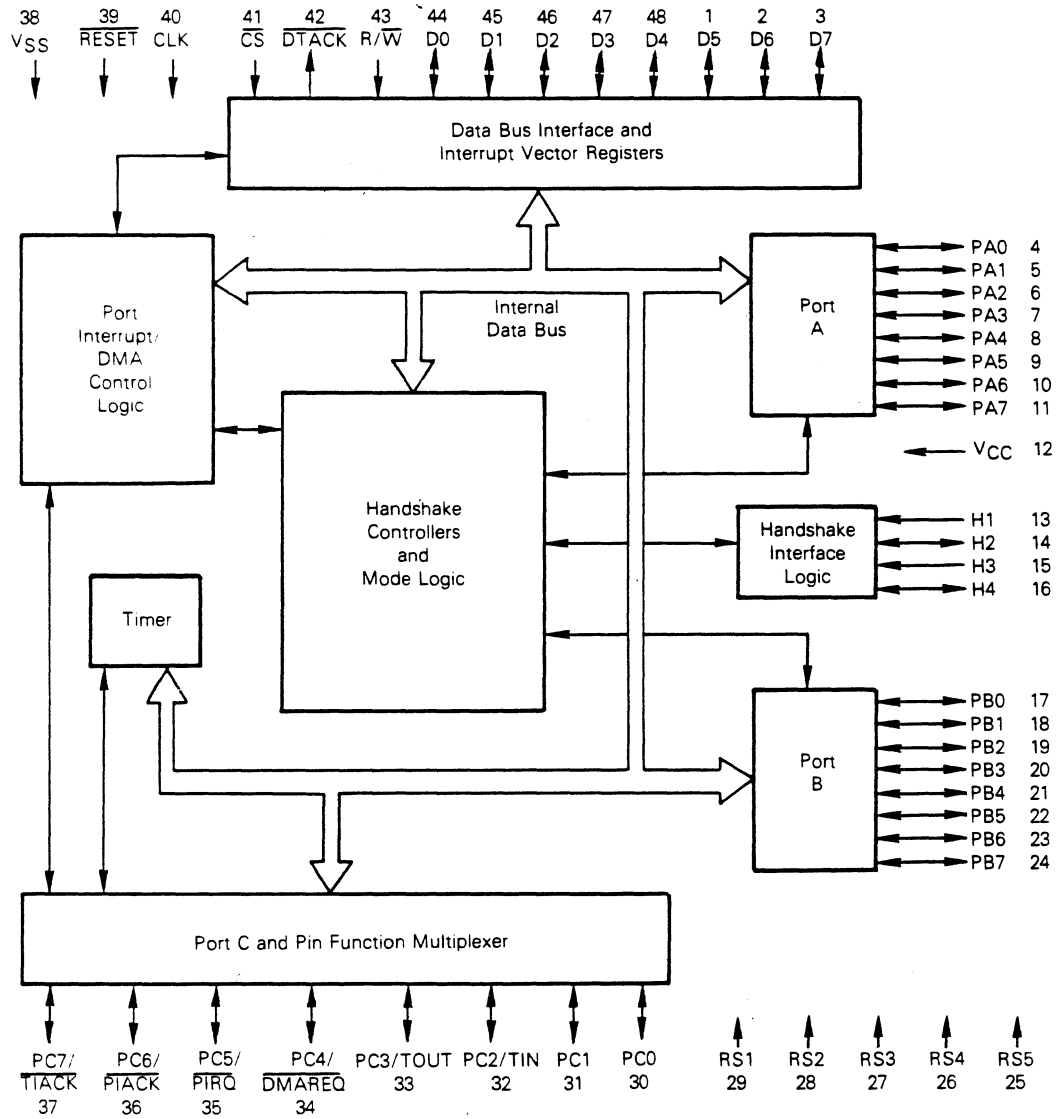
GENERAL DESCRIPTION

The PI/T consists of two logically independent sections: the ports and the timer. The port section consists of Port A (PA0-7), Port B (PB0-7), four handshake pins (H1, H2, H3, and H4), two general I/O pins, and six dual-function pins. The dual-function pins can individually operate as a third port (Port C) or an alternate function related to either Ports A and B, or the timer. The four programmable handshake pins, depending on the mode, can control data transfer to and from the ports, or can be used as interrupt generating inputs, or I/O pins.

The timer consists of a 24-bit counter, optionally clocked by a 5-bit prescaler. Three pins provide complete timer I/O: PC2/TIN, PC3/TOUT, and PC7/$\overline{\text{TIACK}}$. Of course, only the ones needed for the given configuration perform the timer function, while the others remain Port C I/O.

The system bus interface provides for asynchronous transfer of data from the PI/T to a bus master over the data bus (D0-D7). Data transfer acknowledge ($\overline{\text{DTACK}}$), register selects (RS1-RS5), chip select, the read/write line (R/$\overline{\text{W}}$), and Port Interrup Acknowledge ($\overline{\text{PIACK}}$) or Timer Interrupt Acknowledge ($\overline{\text{TIACK}}$) control data transfer between the PI/T and the MC68000.

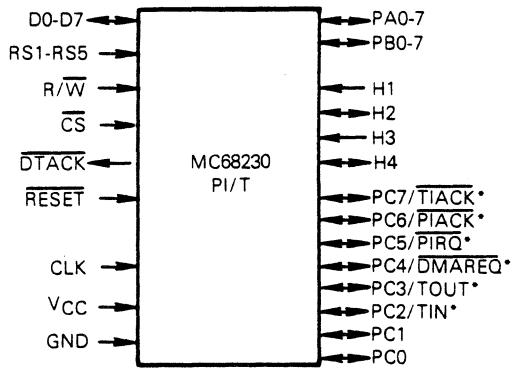
FIGURE 8 — MC68230 BLOCK DIAGRAM



PI/T PIN DESCRIPTION

Throughout the data sheet, signals are presented using the terms active and inactive or asserted and negated independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is given below.) Active low signals are denoted by a superscript bar. R/$\overline{W}$ indicates a write is active low and a read active high.

FIGURE 9 — LOGICAL PIN ASSIGNMENT



*Individually Programmable Dual-Function Pin

D0-D7 — Bidirectional Data Bus. The data bus pins D0-D7 form an 8-bit bidirectional data bus to/from the MC68000 or other bus master. These pins are active high.

RS1-RS5 — Register Selects. RS1-RS5 are active high high-impedance inputs that determine which of the 25 possible registers is being addressed. They are provided by the MC68000 or other bus master.

R/$\overline{W}$ — Read/Write Input — R/$\overline{W}$ is the high-impedance Read/Write signal from the MC68000 or bus master, indicating whether the current bus cycle is a read (high) or write (low) cycle.

$\overline{CS}$ — Chip Select Input. $\overline{CS}$ is a high-impedance input that selects the PI/T registers for the current bus cycle. Address strobe and the data strobe (upper or lower) of the bus master, along with the appropriate address bits, must be included in the chip select equation. A low level corresponds to an asserted chip select.

$\overline{DTACK}$ — Data Transfer Acknowledge Output. $\overline{DTACK}$ is an active low output that signals the completion of the bus cycle. During read or interrupt acknowledge cycles, $\overline{DTACK}$ is asserted by the MC68230 after data has been provided on the data bus; during write cycles it is asserted after data has been accepted at the data bus. Data transfer acknowledge is compatible with the MC68000 and with other Motorola bus masters such as the MC68450 DMA controller. A holding resistor is required to maintain $\overline{DTACK}$ high between bus cycles.

$\overline{RESET}$ — Reset Input. $\overline{RESET}$ is a high-impedance input used to initialize all PI/T functions. All control and data direction registers are cleared and most internal operations are disabled by the assertion of $\overline{RESET}$ (low).

CLK — Clock Input. The clock pin is a high-impedance TTL-compatible signal with the same specifications as the MC68000. The PI/T contains dynamic logic throughout, and hence this clock must not be gated off at any time. It is not necessary that this clock maintain any particular phase relationship with the MC68000 clock. It may be connected to an independent frequency source (faster or slower) as long as all bus specifications are met.

PA0-PA7 and PB0-PB7 — Port A and Port B. Ports A and B are 8-bit ports that may be concatenated to form a 16-bit port in certain modes. The ports may be controlled in conjunction with the handshake pins H1-H4. For stabilization during system power-up, Ports A and B have internal pullup resistors to V_{CC}. All port pins are active high.

H1-H4 — Handshake pins (I/O depending on the Mode and Submode). Handshake pins H1-H4 are multi-purpose pins that (depending on the operational mode) may provide an interlocked handshake, a pulsed handshake, an interrupt input (independent of data transfers), or simple I/O pins. For stabilization during system power-up, H2 and H4 have internal pullup resistors to V_{CC}. Their sense (active high or low) may be programmed in the Port General Control Register bits 3-0. Independent of the mode, the instantaneous level of the handshake pins can be read from the Port Status Register.

Port C — (PC0-PC7/Alternate function). This port can be used as eight general purpose I/O pins (PC0-PC7) or any combination of six special function pins and two general purpose I/O pins (PC0-PC1). (Each dual function pin can be standard I/O or a special function independent of the other port C pins.) The dual function pins are defined in the following paragraphs. When used as a port C pin, these pins are active high. They may be individually programmed as inputs or outputs by the Port C Data Direction Register.

The alternate functions (TIN, TOUT, and $\overline{TIACK}$) are timer I/O pins. TIN may be used as a rising-edge triggered external clock input or an external run/halt control pin (the timer is in the run state if run/halt is high and in the halt state if run/halt is low). TOUT may provide an active low timer interrupt request output or a general-purpose square-wave output, initially high. $\overline{TIACK}$ is an active low high-impedance input used for timer interrupt acknowledge.

Port A and B functions have an independent pair of active low interrupt request ($\overline{PIRQ}$) and interrupt acknowledge ($\overline{PIACK}$) pins.

The $\overline{DMAREQ}$ (Direct Memory Access Request) pin provides an active low Direct Memory Access Controller (DMAC) request pulse of 3 clock cycles, completely compatible with the MC68450 DMAC.

REGISTER MODEL

A register model that includes the corresponding Register Selects is shown in Table 1.

TABLE 1 — REGISTER MODEL

Register Select Bits 5	4	3	2	1	7	6	5	4	3	2	1	0	
0	0	0	0	0	Port Mode Control		H34 Enable	H12 Enable	H4 Sense	H3 Sense	H2 Sense	H1 Sense	Port General Control Register
0	0	0	0	1	*	SVCRQ Select		Interrupt PFS		Port Interrupt Priority Control			Port Service Request Register
0	0	0	1	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Port A Data Direction Register
0	0	0	1	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Port B Data Direction Register
0	0	1	0	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Port C Data Direction Register
0	0	1	0	1	Interrupt Vector Number						*	*	Port Interrupt Vector Register
0	0	1	1	0	Port A Submode		H2 Control			H2 Int Enable	H1 SVCRQ Enable	H1 Stat Ctrl.	Port A Control Register
0	0	1	1	1	Port B Submode		H4 Control			H4 Int Enable	H3 SVCRQ Enable	H3 Stat Ctrl.	Port B Control Register
0	1	0	0	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Port A Data Register
0	1	0	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Port B Data Register
0	1	0	1	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Port A Alternate Register
0	1	0	1	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Port B Alternate Register
0	1	1	0	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Port C Data Register
0	1	1	0	1	H4 Level	H3 Level	H2 Level	H1 Level	H4S	H3S	H2S	H1S	Port Status Register
0	1	1	1	0	*	*	*	*	*	*	*	*	(null)
0	1	1	1	1	*	*	*	*	*	*	*	*	(null)
1	0	0	0	0	TOUT/$\overline{\text{TIACK}}$ Control			Z D Ctrl	*	Clock Control		Timer Enable	Timer Control Register
1	0	0	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Timer Interrupt Vector Register
1	0	0	1	0	*	*	*	*	*	*	*	*	(null)
1	0	0	1	1	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	Counter Preload Register (High)
1	0	1	0	0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	(Mid)
1	0	1	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	(Low)
1	0	1	1	0	*	*	*	*	*	*	*	*	(null)
1	0	1	1	1	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	Count Register (High)
1	1	0	0	0	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	(Mid)
1	1	0	0	1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	(Low)
1	1	0	1	0	*	*	*	*	*	*	*	ZDS	Timer Status Register
1	1	0	1	1	*	*	*	*	*	*	*	*	(null)
1	1	1	0	0	*	*	*	*	*	*	*	*	(null)
1	1	1	0	1	*	*	*	*	*	*	*	*	(null)
1	1	1	1	0	*	*	*	*	*	*	*	*	(null)
1	1	1	1	1	*	*	*	*	*	*	*	*	(null)

*Unused, read as zero.

PORT CONTROL STRUCTURE

The primary focus of most applications will be on Ports A and B, the handshake pins, the port interrupt pins, and the DMA request pin. They are controlled in the following way: the Port General Control Register contains a 2-bit field that specifies a set of four operation modes. These govern the overall operation of the ports and determine their interrelationships. Some modes require additional information from each port's control register to further define its operation. In each port control register, there is a 2-bit submode field that serves this purpose. Each port mode/submode combination specifies a set of programmable characteristics that fully define the behavior of that port and two of the handshake pins. This structure is summarized in Table 2 and Figure 10.

FIGURE 10 — PORT MODE LAYOUT

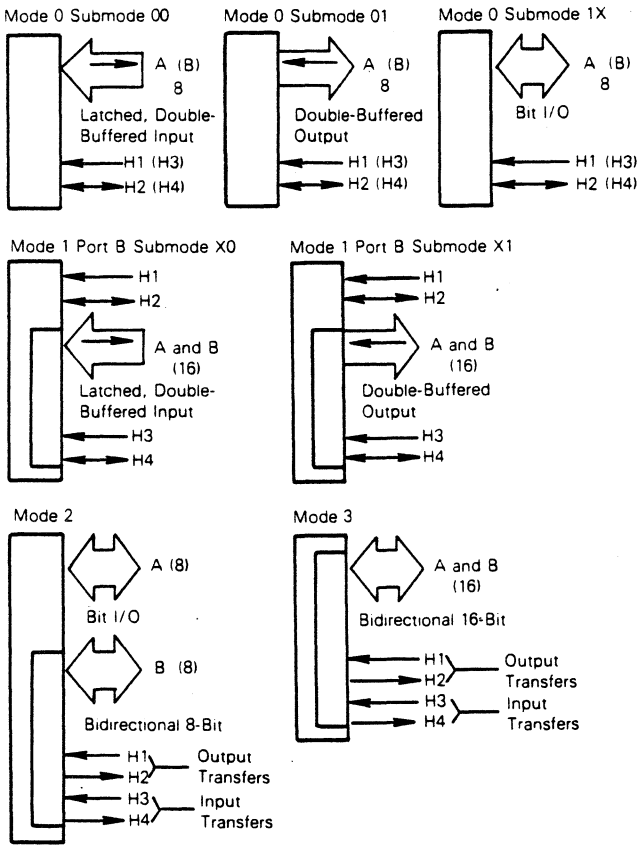


TABLE 2 — PORT MODE CONTROL SUMMARY

Mode 0 (Unidirectional 8-Bit Mode)
- Port A
  - Submode 00 — Double-Buffered Input
    - H1 — Latches input data
    - H2 — Status/interrupt generating input, general-purpose output, or operation with H1 in the interlocked or pulsed input handshake protocols
  - Submode 01 — Double-Buffered Output
    - H1 — Indicates data received by peripheral
    - H2 — Status/interrupt generating input, general-purpose output, or operation with H1 in the interlocked or pulsed output handshake protocols
  - Submode 1X — Bit I/O
    - H1 — Status/interrupt generating input
    - H2 — Status/interrupt generating input or general-purpose output
- Port B, H3 and H4 — Identical to Port A, H1 and H2

Mode 1 (Unidirectional 16-Bit Mode)
- Port A — Double-Buffered Data (Most significant)
  - Submode XX (not used)
    - H1 — Status/interrupt generating input
    - H2 — Status/interrupt generating input or general-purpose output
- Port B — Double-Buffered Data (Least significant)
  - Submode X0 — Unidirectional 16-Bit Input
    - H3 — Latches input data
    - H4 — Status/interrupt generating input, general-purpose output, or operation with H3 in the interlocked or pulsed input handshake protocols
  - Submode X1 — Unidirectional 16-Bit Output
    - H3 — Indicates data received by peripheral
    - H4 — Status/interrupt generating input, general-purpose output, or operation with H3 in the interlocked or pulsed output handshake protocols

Mode 2 (Bidirectional 8-Bit Mode)
- Port A — Bit I/O (with no handshaking pins)
  - Submode XX (not used)
- Port B — Bidirectional 8-Bit Data (Double-Buffered)
  - Submode XX (not used)
    - H1 — Indicates output data received by peripheral
    - H2 — Operation with H1 in the interlocked or pulsed output handshake protocols
    - H3 — Latches input data
    - H4 — Operation with H3 in the interlocked or pulsed input handshake protocols

Mode 3 (Bidirectional 16-Bit Mode)
- Port A — Double-Buffered Data (Most significant)
  - Submode XX (not used)
- Port B — Double-Buffered Data (Least significant)
  - Submode XX (not used)
    - H1 — Indicates output data received by peripheral
    - H2 — Operation with H1 in the interlocked or pulsed output handshake protocols
    - H3 — Latches input data
    - H4 — Operation with H3 in the interlocked or pulsed input handshake protocols

PORT GENERAL INFORMATION AND CONVENTIONS

The following paragraphs introduce concepts that are generally applicable to the PI/T ports independent of the chosen mode and submode. For this reason, no particular port or handshake pins are mentioned; the notation H1 (H3) indicates that, depending on the chosen mode and submode, the statement given may be true for either the H1 or H3 handshake pin.

Unidirectional vs Bidirectional — Figure 10 shows the configuration of Ports A and B and each of the handshake pins in each port mode and submode. In Modes 0 and 1, a data direction register is associated with each of the ports. These registers contain one bit for each port pin to determine whether that pin is an input or an output. Modes 0 and 1 are, thus, called unidirectional modes because each pin assumes a constant direction, changeable only by a reset condition or a programming change. These modes allow double-buffered data transfers in one direction. This direction, determined by the mode and submode definition, is known as the primary direction. Data transfers in the primary direction are controlled by the handshake pins. Data transfers not in the primary direction are generally unrelated, and single or unbuffered data paths exist.

In Modes 2 and 3 there is no concept of primary direction as in Modes 0 and 1. Except for Port A in Mode 2 (Bit I/O), the data direction registers have no effect. These modes are bidirectional, in that the direction of each transfer (always 8 or 16 bits, double-buffered) is determined dynamically by the state of the handshake pins. Thus, for example, data may be transferred out of the ports, followed very shortly by a transfer into the same port pins. Transfers to and from the ports are independent and may occur in any sequence. Since the instantaneous direction is always determined by the external system, a small amount of arbitration logic may be required.

Control of Double-Buffered Data Paths — Generally speaking, the PI/T is a double-buffered device. In the primary direction, double-buffering allows orderly transfers by using the handshake pins in any of several programmable protocols. (When Bit I/O is used, double-buffering is not available and the handshake pins are used as outputs or status/interrupt inputs.)

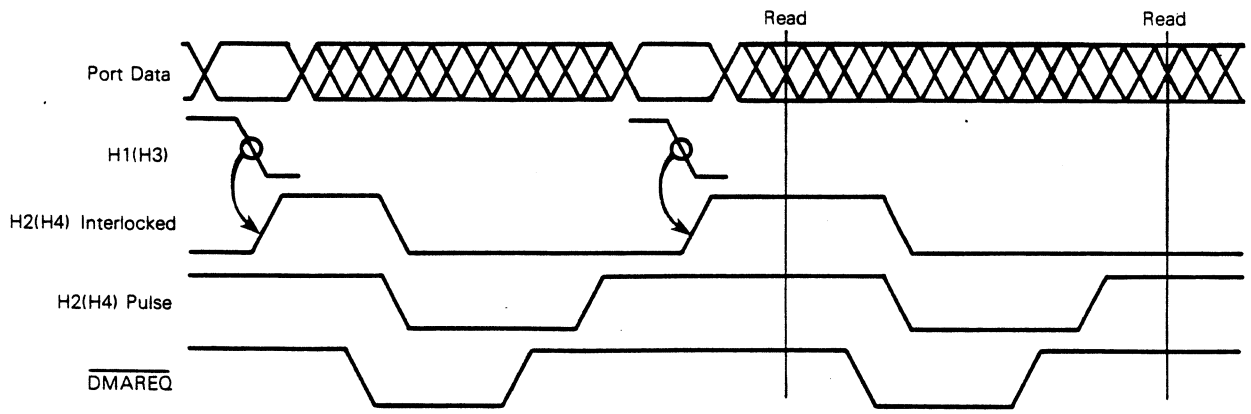
Use of double-buffering is most beneficial in situations where a peripheral device and the computer system are capable of transferring data at roughly the same speed. Double-buffering allows the fetch operation of the data transmitter to be overlapped with the store operation of the data receiver. Thus, throughput measured in bytes or words-per-second may be greatly enhanced. if there is a large mismatch in transfer capability between the computer and the peripheral, little or no benefit is obtained. In these cases there is no penalty in using double-buffering.

Double-Buffered Input Transfers — In all modes, the PI/T supports double-buffered input transfers. Data that meets the port setup and hold times is latched on the asserted edge of H1(H3). H1(H3) is edge-sensitive, and may assume any duty-cycle as long as both high and low minimum times are observed. The PI/T contains a Port Status Register whose H1S(H3S) status bit is set anytime any input data is present in the double-buffered latches that has not been read by the bus master. The action of H2(H4) is programmable; it may indicate whether there is room for more data in the PI/T latches or it may serve other purposes. The following options are available, depending on the mode.

1. H2(H4) may be an edge-sensitive input that is independent of H1(H3) and the transfer of port data. On the asserted edge of H2(H4), the H2S(H4S) status bit is set. It is cleared by the direct method (refer to Direct Method of Resetting Status), the $\overline{\text{RESET}}$ pin being asserted, or when the H12 Enable (H34 Enable) bit of the Port General Control Register is 0.
2. H2(H4) may be a general purpose output pin that is always negated. The H2S(H4S) status bit is always 0.
3. H2(H4) may be a general purpose output pin that is always asserted. The H2S(H4S) status bit is always 0.
4. H2(H4) may be an output pin in the interlocked input handshake protocol. It is asserted when the port input latches are ready to accept new data. It is negated asynchronously following the asserted edge of the H1(H3) input. As soon as the input latches become ready, H2(H4) is again asserted. When the input double-buffered latches are full, H2(H4) remains negated until data is removed. Thus, anytime the H2(H4) output is asserted, new input data may be entered by asserting H1(H3). At other times transitions on H1(H3) are ignored. The H2S(H4S) status bit is always 0. When H12 Enable (H34 Enable) is 0, H2(H4) is held negated.
5. H2(H4) may be an output pin in the pulsed input handshake protocol. It is asserted exactly as in the interlocked input protocol, but never remains asserted longer than 4 clock cycles. Typically, a four clock cycle pulse is generated. But in the case that a subsequent H1(H3) asserted edge occurs before termination of the pulse, H2(H4) is negated asynchronously. Thus, anytime after the leading edge of the H2(H4) pulse, new data may be entered in the PI/T double-buffered input latches. The H2S(H4S) status bit is always 0. When H12 Enable (H34 Enable) is 0, H2(H4) is held negated.

A sample timing diagram is shown in Figure 11. The H2(H4) interlocked and pulsed input handshake protocols are shown. The $\overline{\text{DMAREQ}}$ pin is also shown assuming it is enabled. All handshake pin sense bits are assumed to be 0 (refer to Port General Control Register); thus, the pins are in the low state when asserted. Due to the great similarity between modes, this timing diagram is applicable to all double-buffered input transfers.

FIGURE 11 — DOUBLE-BUFFERED INPUT TRANSFERS

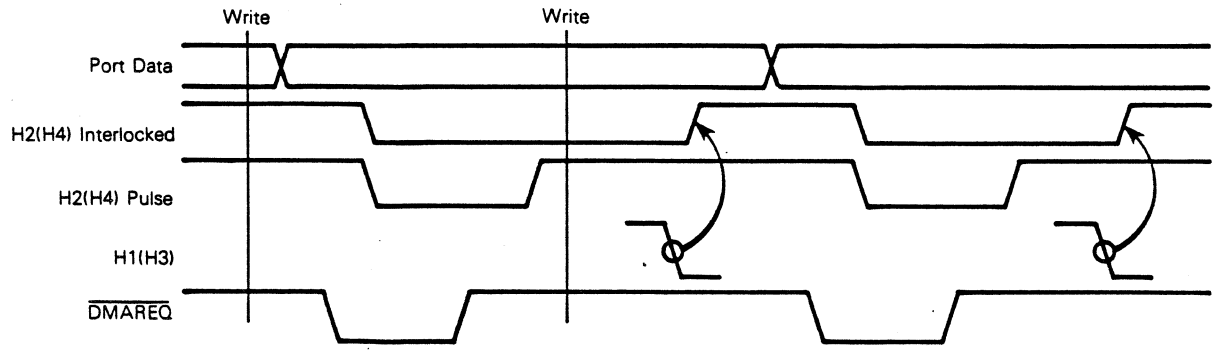


Double-Buffered Output Transfers — The PI/T supports double-buffered output transfers in all modes. Data, written by the bus master to the PI/T, is stored in the port's output latch. The peripheral accepts the data by asserting H1(H3), which causes the next data to be moved to the port's output latch as soon as it is available. The function of H2(H4) is programmable; it may indicate whether new data has been moved to the output latch or it may serve other purposes. The H1S(H3S) status bit may be programmed for two interpretations. Normally the status bit is a 1 when there is at least one latch in the double-buffered data path that can accept new data. After writing one byte/word of data to the ports, an interrupt service routine could check this bit to determine if it could store another byte/word; thus, filling both latches. When the bus master is finished, it is often useful to be able to check whether all of the data has been transferred to the peripheral. The H1S(H3S) Status Control bit of the Port A and B Control Registers provide this flexibility. The programmable options of the H2(H4) pin are given below, depending on the mode.

1. H2(H4) may be an edge-sensitive input pin independent of H1(H3) and the transfer of port data. On the asserted edge of H2(H4), the H2S(H4S) status bit is set. It is reset by the direct method (refer to Direct Method of Resetting Status), the $\overline{\text{RESET}}$ pin being asserted, or when the H12 Enable (H34 Enable) bit of the Port General Control Register is 0.
2. H2(H4) may be a general-purpose output pin that is always negated. The H2S(H4S) status bit is always 0.
3. H2(H4) may be a general-purpose output pin that is always asserted. The H2S(H4S) status bit is always 0.
4. H2(H4) may be an output pin in the interlocked output handshake protocol. H2(H4) is asserted two clock cycles after data is transferred to the double-buffered output latches. The data remains stable and H2(H4) remains asserted until the next asserted edge of the H1(H3) input. At that time, H2(H4) is asynchronously negated. As soon as the next data is available, it is transferred to the output latches. When H2(H4) is negated, asserted transitions on H1(H3) have no effect on the data paths. As is explained later, however, in Modes 2 and 3 they do control the three-state output buffers of the bidirectional port(s). The H2S(H4S) status bit is always 0. When H12 Enable (H34 Enable) is 0, H2(H4) is held negated.
5. H2(H4) may be an output pin in the pulsed output handshake protocol. It is asserted exactly as in the interlocked output protocol above, but never remains asserted longer than four clock cycles. Typically, a four clock pulse is generated. But in the case that a subsequent H1(H3) asserted edge occurs before termination of the pulse, H2(H4) is negated asynchronously shortening the pulse. The H2S(H4S) status bit is always 0. When H12 Enable (H34 Enable) is 0 H2(H4) is held negated.

A sample timing diagram is shown in Figure 12. The H2(H4) interlocked and pulsed output handshake protocols are shown. The $\overline{\text{DMAREQ}}$ pin is also shown assuming it is enabled. All handshake pin sense bits are assumed to be 0; thus, the pins are in the low state when asserted. Due to the great similarity between modes, this timing diagram is applicable to all double-buffered output transfer.

FIGURE 12 — DOUBLE-BUFFERED OUTPUT TRANSFERS



Requesting Bus Master Service — The PI/T has several means of indicating a need for service by a bus master. First, the processor may poll the Port Status Register. It contains a status bit for each handshake pin, plus a level bit that always reflects the instantaneous state of that handshake pin. A status bit is 1 when the PI/T needs servicing, i.e., generally when the bus master needs to read or write data to the ports, or when a handshake pin used as a simple status input has been asserted. The interpretation of these bits is dependent on the chosen mode and submode.

Second, the PI/T may be placed in the processor's interrupt structure. As mentioned previously, the PI/T contains Port A and B Control Registers that configure the handshake pins. Other bits in these registers enable an interrupt associated with each handshake pin. This interrupt is made available through the PC5/$\overline{\text{PIRQ}}$ pin, if the PIRQ function is selected. Three additional conditions are required for $\overline{\text{PIRQ}}$ to be asserted: (1) the handshake pin status bit set, (2) the corresponding interrupt (service request) enable bit is set, (3) and DMA requests are not associated with that data transfer (H1 and H3 only). The conditions from each of the four handshake pins and corresponding status bits are ORed to determine $\overline{\text{PIRQ}}$.

The third method of requesting service is via the PC4/$\overline{\text{DMAREQ}}$ pin. This pin can be associated with double-buffered transfers in each mode. If it is used as a DMA controller request, it can initiate requests to keep the PI/T's input/output double-buffering empty/full as much as possible. It will not overrun the DMA controller. The pin is compatible with the MC68450 Direct Memory Access Controller (DMAC).

Vectored, Prioritized Port Interrupts — Use of MC68000-compatible vectored interrupts with the PI/T requires the $\overline{\text{PIRQ}}$ and $\overline{\text{PIACK}}$ pins. When $\overline{\text{PIACK}}$ is asserted, the PI/T places an 8-bit vector on the data pins D0-D7. Under normal conditions, this vector corresponds to highest priority, enabled, active port interrupt source with which the $\overline{\text{DMAREQ}}$ pin is not currently associated. The most-significant six bits are provided by the Port Interrupt Vector Register (PIVR), with the lower two bits supplied by prioritization logic according to conditions present when $\overline{\text{PIACK}}$ is asserted. It is important to note that the only affect on the PI/T caused by interrupt acknowledge cycles is that the vector is placed on the data bus. Specifically, no registers, data, status, or other internal states of the PI/T are affected by the cycle.

Several conditions may be present when the $\overline{\text{PIACK}}$ input is asserted to the PI/T. These conditions affect the PI/T's response and the termination of the bus cycle. If the PI/T has no interrupt function selected, or is not asserting $\overline{\text{PIRQ}}$, the PI/T will make no response to $\overline{\text{PIACK}}$ ($\overline{\text{DTACK}}$ will not be asserted). If the PI/T is asserting $\overline{\text{PIRQ}}$ when $\overline{\text{PIACK}}$ is received, the PI/T will output the contents of the Port Interrupt Vector Register and the prioritization bits. If the PIVR has not been initialized, $0F will be read from this register. These conditions are summarized in Table 3.

TABLE 3 — RESPONSE TO PORT INTERRUPT ACKNOWLEDGE

Conditions	$\overline{\text{PIRQ}}$ negated OR interrupt request function not selected	$\overline{\text{PIRQ}}$ asserted
PIVR has not been initialized since $\overline{\text{RESET}}$	No response from PI/T. No $\overline{\text{DTACK}}$.	PI/T provides $0F, the Uninitialized Vector.*
PIVR has been initialized since $\overline{\text{RESET}}$	No response from PI/T. No $\overline{\text{DTACK}}$.	PI/T provides PIVR contents with prioritization bits.

*The uninitialized vector is the value returned from an interrupt vector register before it has been initialized.

The vector table entries for the PI/T appear as a contiguous block of four vector numbers whose common upper six bits are programmed in the PIVR. The following table pairs each interrupt source with the 2-bit value provided by the prioritization logic, when interrupt acknowledge is asserted.

H1 source — 00
H2 source — 01
H3 source — 10
H4 source — 11

Autovectored Port Interrupts — Autovecored interrupts use only the $\overline{\text{PIRQ}}$ pin. The operation of the PI/T with vectored and autovectored interrupts is identical except that no vectors are supplied and the PC6/$\overline{\text{PIACK}}$ pin can be used as a Port C pin.

Direct Method of Resetting Status — In certain modes one or more handshake pins can be used as edge-sensitive inputs for sole purpose of setting bits in the Port Status Register. These bits consist of simple flip-flops. They are set (to 1) by the occurrence of the asserted edge of the handshake pin input. Resetting a handshake status bit can be done by writing an 8-bit mask to the Port Status Register. This is called the direct method of resetting. To reset a status bit that is resettable by the direct method, the mask must contain a 1 in the bit position of the Port Status Register corresponding to the desired bit. Other positions must contain 0's. For status bits that are not resettable by the direct method in the chosen mode, the data written to the port status register has no effect. For status bits that are resettable by the direct method in the chosen mode, a 0 in the mask has no effect.

Handshake Pin Sense Control — The PI/T contains exclusive-OR gates to control the sense of each of the handshake pins, whether used as inputs or outputs. Four bits in the Port General Control Register may be programmed to determine whether the pins are asserted in the low or high voltage state. As with other control registers, these bits are reset to 0 when the $\overline{\text{RESET}}$ pin is asserted, defaulting the asserted level to be low.

Enabling Ports A and B — Certain functions involved with double-buffered data transfers, the handshake pins, and the status bits, may be disabled by the external system or by the

programmer during initialization. The Port General Control Register contains two bits, H12 Enable and H34 Enable, which control these functions. These bits are cleared to the o state when the $\overline{\text{RESET}}$ pin is asserted, and the functions are disabled. The functions are the following:

1. Independent of other actions by the bus master or peripheral (via the handshake pins), the PI/T's disabled handshake controller is held to the "empty" state, i.e., no data is present in the double-buffered data path.
2. When any handshake pin is used to set a simple status flip-flop, unrelated to double-buffered transfers, these flip-flops are held reset to 0. (See Table 2.)
3. When H2(H4) is used in an interlocked or pulsed handshake with H1(H3), H2(H4) is held negated, regardless of the chosen mode, submode, and primary direction. Thus, for double-buffered input transfers, the programmer may signal a peripheral when the PI/T is ready to begin transfers by setting the associated handshake enable bit to 1.

The Port A and B Alternate Registers — In addition to the Port A and B Data Registers, the PI/T contains Port A and B Alternate Registers. These registers are read-only, and simply provide the instantaneous level of each port pin. They have no effect on the operation of the handshake pins, double-buffered transfers, status bits, or any other aspect of the PI/T, and they are mode/submode independent.

PORT MODES

This section contains information that distinguishes the various port modes and submodes. General characteristics, common to all modes, have been defined previously.

MODE 0 — UNIDIRECTIONAL 8-BIT MODE

In Mode 0, Ports A and B operate independently. Each may be configured in any of its three possible submodes:

Submode 00 — Double-Buffered Input
Submode 01 — Double-Buffered Output
Submode 1X — Bit I/O

Handshake pins H1 and H2 are associated with Port A and configured by programming the Port A Control Register. (The H12 Enable bit of the Port General Control Register enables Port A transfers.) Handshake pins H3 and H4 are associated with Port B and configured by programming the Port B Control Register. (The H34 Enable bit of the Port General Control Register enables Port B transfers.) The Port A and B Data Direction Registers operate in all three submodes. Along with the submode, they affect the data read and written at the associated data register according to Table 4. They also enable the output buffer associated with each port pin. The $\overline{\text{DMAREQ}}$ pin may be associated with either (not both) Port A or Port B, but does not function if the Bit I/O submode is programmed for the chosen port.

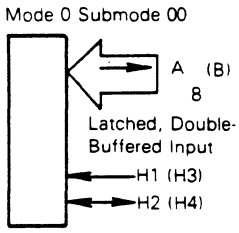
TABLE 4 — MODE 0 PORT DATA PATHS

Mode	Read Port A/B Data Register		Write Port A/B Data Register	
	DDR = 0	DDR = 1	DDR = X	
0 Submode 00	FIL, D.B.	FOL Note 3	FOL, S.B.	Note 1
0 Submode 01	Pin	FOL Note 3	IOL/FOL, D.B.	Note 2
0 Submode 1X	Pin	FOL Note 3	FOL, S.B.	Note 1

Abbreviations:
IOL — Initial Output Latch
FOL — Final Output Latch
FIL — Final Input Latch
S.B. — Single Buffered
D.B. — Double Buffered
DDR — Data Direction Register

Note 1: Data is latched in the output data registers (final output latch) and will be single buffered at the pin if the DDR is 1. The output buffers will be turned off if the DDR is 0.
Note 2: Data is latched in the double-buffered output data registers. The data in the final output latch will appear on the port pin if the DDR is a 1.
Note 3: The output drivers that connect the final output latch to the pins are turned on.

Port A or B Submode 00 (8-Bit Double-Buffered Input) —

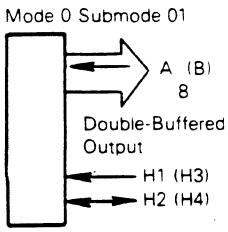


In Mode 0, double-buffered input transfers of up to 8-bits are available by programming Submode 00 in the desired port's control register. The operation of H2 and H4 may be selected by programming the Port A and Port B Control Registers, respectively. All five double-buffered input handshake options, previously mentioned in the Port General Information and Conventions section, are available.

For pins used as outputs, the data path consists of a single latch driving the output buffer. Data written to the port's data register does not affect the operation of any handshake pin, status bit, or any other aspect of the PI/T. Output pins may be used independently of the input transfer. However, read bus cycles to the data register do remove data from the port. Therefore, care should be taken to avoid processor instructions that perform unwanted read cycles.

Refer to PARALLEL PORTS Double-Buffered Input Transfers for a sample timing diagram (Figure 11).

Port A or B Submode 01 (8-Bit Double-Buffered Output) —

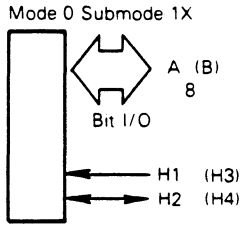


In Mode 0, double-buffered output transfers of up to 8 bits are available by programming submode 01 in the desired port's control register. The operation of H2 and H4 may be selected by programming the Port A and Port B Control Registers, respectively. All five double-buffered output handshake options, previously mentioned in the Port General Information and Conventions section, are available.

For pins used as inputs, data written to the associated data register is double-buffered and passed to the initial or final output latch, as usual, but the output buffer is disabled.

Refer to PARALLEL PORTS Double-Buffered Output Transfers for a sample timing diagram (Figure 12).

Port A or B Submode 1X (Bit I/O) —



In Mode 0, simple Bit I/O is available by programming Submode 1X in the desired port's control register. This submode is intended for applications in which several independent devices must be controlled or monitored. Data written to the associated data register is single-buffered. If the data direction register bit for that pin is a 1 (output), the output buffer is enabled. If it is 0 (input), data written is still latched, but is not available at the pin. Data read from the data register is the instantaneous value of the pin or what was written to the data register, depending on the contents of the data direction register. H1(H3) is an edge-sensitive status input pin only and it controls no data-related function. The H1S(H3S) status bit is set following the asserted edge of the input waveform. It is reset by the direct method, the $\overline{\text{RESET}}$ pin being asserted, or when the H12 Enable (H34 Enable) bit is 0.

H2(H4) can be programmed as a simple status input (identical to H1(H3)), or as an asserted or negated output. The interlocked or pulsed handshake configurations are not available.

MODE 1 — UNIDIRECTIONAL 16-BIT MODE

In Mode 1, Ports A and B are concatenated to form a single 16-bit port. The Port B Submode field controls the configuration of both ports. The possible submodes are:

Port B Submode X0 — Double-Buffered Input
Port B Submode X1 — Double-Buffered Output

Handshake pins H3 and H4, configured by programming the Port B Control Register, are associated with the 16-bit double-buffered transfer. These 16-bit transfers, are enabled by the H34 Enable bit of the Port General Control Register. Handshake pins H1 and H2 may be used as simple status inputs not related to the 16-bit data transfer or H2 may be an output. Enabling of the H1 and H2 handshake pins is done by the H12 Enable bit of the Port General Control Register. The Port A and B Data Direction Registers operate in each submode. Along with the submode, they affect the data read and written at the data register according to Table 5. They also enable the output buffer associated with each port pin. The $\overline{\text{DMAREQ}}$ pin may be associated only with H3.

Mode 1 can provide convenient, high-speed 16-bit transfers. The Port A and B data registers are addressed for compatibility with the MC68000 Move Peripheral (MOVEP) instruction and with the MC68450 DMAC. To take advantage of this, Port A should contain the most-significant byte of data and always be read or written by the bus master first. The interlocked and pulsed handshake protocols are keyed to accesses to the Port B Data Register in Mode 1. If it is accessed last, the 16-bit double-buffered transfers proceed smoothly.

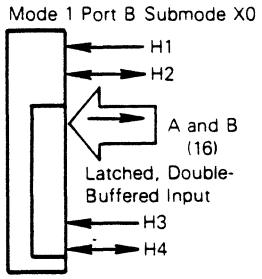
TABLE 5 — MODE 1 PORT DATA PATHS

Mode	Read Port A/B Register		Write Port A/B Register	
	DDR = 0	DDR = 1	DDR = 0	DDR = 1
1, Port B Submode X0	FIL, D.B.	FOL Note 3	FOL, S.B. Note 2	FOL, S.B. Note 2
1, Port B Submode X1	Pin	FOL Note 3	IOL/FOL, D.B., Note 1	IOL/FOL, D.B., Note 1

Note 1: Data written to Port A goes to a temporary latch. When the Port B data register is later written, Port A data is transferred to IOL/FOL.
Note 2: Data is latched in the output data registers (final output latch) and will be single buffered at the pin if the DDR is 1. The output buffers will be turned off if the DDR is 0.
Note 3: The output drivers that connect the final output latch to the pins are turned on.

Abbreviations:
IOL — Initial Output Latch
FOL — Final Output Latch
FIL — Final Input Latch
S.B. — Single Buffered
D.B. — Double Buffered
DDR — Data Direction Register

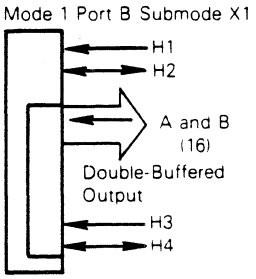
Port B Submode X0 (16-Bit Double-Buffered Input) —



In Mode 1 Port B Submode X0, double-buffered input transfers of up to 16 bits may be obtained. The level of all 16 pins is asynchronously latched with the asserted edge of H3. The processor may check H3S status bit to determine if new data is present. The $\overline{\text{DMAREQ}}$ pin may be used to signal a DMA controller to empty the input buffers. Regardless of the bus master, Port A data should be read first. (Actually, Port A data need not be read at all.) Port B data should be read last. The operation of the internal handshake controller, the H3S bit, and $\overline{\text{DMAREQ}}$ are keyed to the reading of the Port B data register. (The MC68450 DMAC can be programmed to perform the exact transfers needed for compatibility with the PI/T.) H4 may be programmed for all five of the handshake options mentioned in the Port General Information and Conventions section.

For pins used as outputs, the data path consists of a single latch driving the output buffer. Data written to the port's data register does not affect the operation of any handshake pin, status bit, or any other aspect of the PI/T. Thus, output pins may be used independently of the input transfer. However, read bus cycles to the Port B Data Register do remove data, so care should be taken to avoid unwanted read cycles.

Port B Submode X1 (16-Bit Double-Buffered Output) —



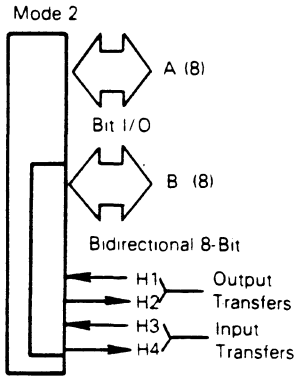
Refer to PARALLEL PORTS Double-Buffered Input Transfers for a sample timing diagram (Figure 11).

In Mode 1 Port B Submode X1, double-buffered output transfers of up to 16 bits may be obtained. Data is written by the bus master (processor or DMA controller) in two bytes. The first byte (most-significant) is written to the Port A Data Register. It is stored in a temporary latch until the next byte is written to the Port B Data Register. Then all 16 bits are transferred to the final output latches of Ports A and B. Both options for interpretation of the H3S status bit, mentioned in Port General Information and Comments section, are available and apply to the 16-bit port as a whole. The $\overline{\text{DMAREQ}}$ pin may be used to signal a DMA controller to transfer another word to the port output latches. (The MC68450 DMAC can be programmed to perform the exact transfers needed for compatibility with the PI/T.) H4 may be programmed for all five of the handshake options mentioned in the Port General Information and Comments section.

For pins used as inputs, data written to either data register is double-buffered and passed to the initial or final output latch, as usual, but the output buffer is disabled.

Refer to PARALLEL PORTS Double-Buffered Input/Output Transfer for a sample timing diagram (Figure 12).

MODE 2 — BIDIRECTIONAL 8-BIT MODE

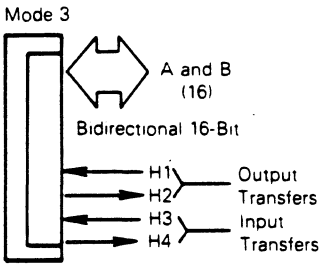


In Mode 2, Port A is used for simple bit I/O with no associated handshake pins. Port B is used for bidirectional 8-bit double-buffered transfers. H1 and H2, enabled by the H12 Enable bit in the Port General Control Register, control output transfers, while H3 and H4, enabled by the Port General Control Register bit H34 Enable, control input transfers. The instantaneous direction of the data is determined by the H1 handshake pin. The Port B Data Direction Register is not used. The Port A and Port B submode fields do not affect PI/T operation in Mode 2.

Double-Buffered I/O (Port B) — The only aspect of bidirectional double-buffered transfers that differs from the unidirectional modes lies in controlling the Port B output buffers. They are controlled by the level of H1. When H1 is negated, the Port B output buffers (all 8) are enabled and the pins drive the bidirectional bus. Generally, H1 is negated in response to an asserted H2, which indicates that new output data is present in the double-buffered latches. Following acceptance of the data, the peripheral asserts H1, disabling the Port B output buffers. Other than controlling the output buffer, H1 is edge-sensitive as in other modes. Input transfers proceed identically to the double-buffered input protocol described in the Port General Information and Conventions Section. In Mode 2, only the interlocked and pulsed handshake pin options are available on H2 and H4. The $\overline{\text{DMAREQ}}$ pin may be associated with either input transfers (H3) or output transfers (H1), but not both. Refer to Table 6 for a summary of the Port B Data Register responses in Mode 2.

Bit I/O (Port A) — Mode 2, Port A performs simple bit I/O with no associated handshake pins. This configuration is intended for applications in which several independent devices must be controlled or monitored. Data written to the Port A data register is single-buffered. If the Port A Data Direction Register bit for that pin is 1 (output), the output buffer is enabled. If it is 0, data written is still latched but not available at the pin. Data read from the data register is either the instantaneous value of the pin or what was written to the data register, depending on the contents of the Port A Data Direction Register. This is summarized in Table 7.

MODE 3 — BIDIRECTIONAL 16-BIT DOUBLE-BUFFERED I/O



In Mode 3, Ports A and B are used for bidirectional 16-bit double-buffered transfers. H1 and H2 control output transfers, while H3 and H4 control input transfers. (H1 and H2 are enabled by the H12 Enable bit while H3 and H4 are enabled by the H34 Enable bit of the Port General Control Register.) The instantaneous direction of the data is determined by the H1 handshake pin, and thus, the data direction registers are not used. The Port A and Port B submode fields do not affect PI/T operation in Mode 3.

The only aspect of bidirectional double-buffered transfers that differs from the unidirectional modes lies in controlling the Port A and B output buffers. They are controlled by the level of H1. When H1 is negated, the output buffers (all 16) are enabled and the pins drive the bidirectional bus. General-

TABLE 6 — MODE 2 PORT B DATA PATHS

Mode	Read Port B Data Register	Write Port B Data Register
2	FIL, D.B.	IOL/FOL, D.B.

Abbreviations:
IOL — Initial Output Latch
FOL — Final Output Latch
FIL — Final Input Latch
D.B. — Double Buffered

TABLE 7 — MODE 2 PORT A DATA PATHS

Mode	Read Port A Data Register		Write Port A Data Register	
	DDR = 0	DDR = 1	DDR = 0	DDR = 1
2	Pin	FOL	FOL	FOL, S.B.

Abbreviations:
S.B. — Single Buffered
FOL — Final Output Latch
DDR — Data Direction Register

ly, H1 is negated in response to an asserted H2, which indicates that new output data is present in the double-buffered latches. Following acceptance of the data, the peripheral asserts H1, disabling the output buffers. Other than controlling the output buffers, H1 is edge-sensitive as in other modes. Input transfers proceed identicaliy to the double-buffered input protocol described in the Port General Information and Conventions section. Port A and B data is latched with the asserted edge of H3. In Mode 3, only the interlocked and pulsed handshake pin options are available to H2 and H4. The $\overline{\text{DMAREQ}}$ pin may be associated with either input transfers (H3) or output transfers (H1), but not both. H2 indicates when new data is available in the Port B (and implicitly Port A) output latches, but unless the buffer is enabled by H1, the data is not driving the pins.

Mode 3 can provide convenient high-speed 16-bit transfers. The Port A and B Data Registers are addressed for compatibility with the MC68000's Move Peripheral (MOVEP) instruction and with the MC68450 DMAC. To take advantage of this, Port A should contain the most-significant data and always be read or written by the bus master first. The interlocked and pulsed handshake protocols are keyed to accesses to the Port B Data Register in Mode 3. If it is accessed last, the 16-bit double-buffered transfer proceed smoothly. Refer to Table 8 for a summary of the Port A and B data paths in Mode 3.

DMA REQUEST OPERATION

The Direct Memory Access Request ($\overline{\text{DMAREQ}}$) pulse (when enabled) is associated with output or input transfers to keep the initial and final output latches full or initial and final input latches empty, respectively. Figures 13 and 14 show all the possible paths in generating DMA requests.

$\overline{\text{DMAREQ}}$ is generated on the bus side of the MC68230 by the synchronized* Chip Select. If the conditions of Figures 13 and 14 are met, an access of the bus (assertion of $\overline{\text{CS}}$) will cause $\overline{\text{DMAREQ}}$ to be asserted 3 PI/T clocks (plus the delay time from the clock edge) after $\overline{\text{CS}}$ is synchronized.* $\overline{\text{DMAREQ}}$ remains asserted 3 clock cycles (plus the delay time from the clock edge) and is then negated.

The $\overline{\text{DMAREQ}}$ pulse associated with a peripheral or port side of the PI/T is caused by the synchronized* H1(H3) input. If the conditions of Figures 13 and 14 are met, a port access (assertion of the H1(H3) input) will cause $\overline{\text{DMAREQ}}$ to be asserted 2.5 PI/T clock cycles (plus the delay time from clock edge) after H1(H3) is sycnhronized.* $\overline{\text{DMAREQ}}$ remains asserted 3 clock cycles (plus the delay time from the clock edge) and is then negated.

TABLE 8 — MODE 3 PORT A AND B DATA PATHS

Mode	Read Port A and B Data Register	Write Port A and B Data Register
3	FIL, D.B.	IOL/FOL, D.B., Note 1
Note 1: Data written to Port A goes to a temporary latch. When the Port B data register is later written, Port A data is transferred to IOL/FOL.		
Abbreviations: IOL — Initial Output Latch FOL — Final Output Latch FIL — Final Input Latch		S.B. — Single Buffered D.B. — Double Buffered

FIGURE 13 — $\overline{\text{DMAREQ}}$ ASSOCIATED WITH OUTPUT TRANSFERS
Data in Output Latches

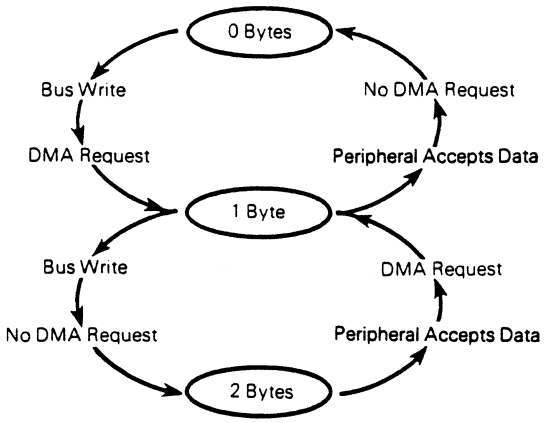
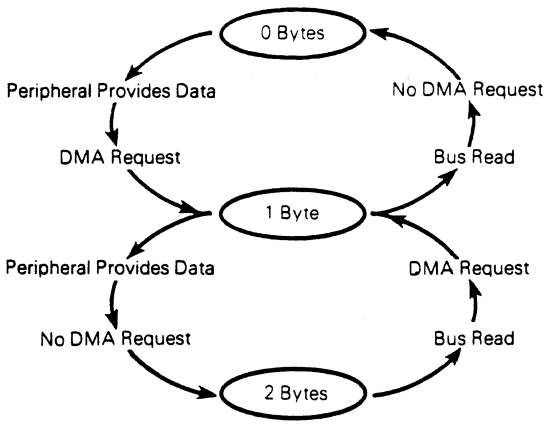


FIGURE 14 — $\overline{\text{DMAREQ}}$ ASSOCIATED WITH INPUT TRANSFERS
Data in Input Latches



*Synchronized means that the input signal has been seen by the PI/T on the appropriate edge of the clock (rising edge for H1(H3) and falling edge for $\overline{\text{CS}}$). (Refer to the BUS INTERFACE CONNECTION section for the exception concerning $\overline{\text{CS}}$.) If a bus access (assertion of $\overline{\text{CS}}$) and a port access (assertion of H1(H3)) occur at the same time, $\overline{\text{CS}}$ will be recognized without any delay. H1(H3) will be recognized one clock cycle later.

TIMER

The MC68230 timer can provide several facilities needed by MC68000 operating systems. It can generate periodic interrupts, a square wave, or a single interrupt after a programmed time period. Also, it can be used for elapsed time measurement or as a device watchdog. This section describes the programmable options available, capabilities, and restrictions that apply to the timer.

The PI/T timer contains a 24-bit synchronous down counter that is loaded from three 8-bit Counter Preload Registers. The 24-bit counter may be clocked by the output of a 5-bit (divide-by-32) prescaler or by an external timer input TIN. If the prescaler is used, it may be clocked by the system clock (CLK pin) or by the TIN external input. The counter signals the occurrence of an event primarily through zero detection. (A zero is when the counter of the 24-bit timer is equal to zero.) This sets the zero detect status (ZDS) bit in the Timer Status Register. It may be checked by the processor or may be used to generate a timer interrupt. The ZDS bit is reset by writing a 1 to the Timer Status Register in that bit position.

The general operation of the timer is flexible and easily programmable. The timer is fully configured and controlled by programming the 8-bit Timer Control Register. It controls: (1) the choice between the Port C operation and the timer operation of three timer pins, (2) whether the counter is loaded from the Counter Preload Register or rolls over when zero detect is reach, (3) the clock input, (4) whether the prescaler is used, and (5) whether the timer is enabled.

RUN/HALT DEFINITION

The overall operation of the timer is described in terms of the run or halt states. The control of the current state is determined by programming the Timer Control Register. When in the halt state, all of the following occur:

1. The prior contents of the counter is not altered and is reliably readable via the Count Registers.
2. The prescaler is forced to $1F whether or not it is used.
3. The ZDS status bit is forced to 0, regardless of the possible zero contents of the 24-bit counter.

The run state is characterized by:

1. The counter is clocked by the source programmed in the Timer Control Register.
2. The counter is not reliably readable.
3. The prescaler is allowed to decrement if programmed for use.
4. The ZDS status bit is set when the 24-bit counter transitions from $000001 to $000000.

TIMER RULES

This section provides a set of rules that allow easy application of the timer.

1. Refer to the Run/Halt Definition above.
2. When the $\overline{\text{RESET}}$ pin is asserted, all bits of the Timer Control Register go to 0, configuring the dual function pins as Port C inputs.
3. The contents of the Counter Preload Registers and counter are not affected by the $\overline{\text{RESET}}$ pin.
4. The Count Registers provide a direct read data path from each portion of the 24-bit counter, but data written to their addresses is ignored. (This results in a normal bus cycle.) These registers are readable at any time, but their contents are never latched. Unreliable data may be read when the timer is in the run state.
5. The Counter Preload Registers are readable and writable at any time and this occurs independently of any timer operation. No protection mechanisms are provided against ill-timed writes.
6. The input frequency to the 24-bit counter from the TIN pin or prescaler output, must be between 0 and the input frequency at CLK pin divided by 32 regardless of the configuration chosen.
7. For configurations in which the prescaler is used (with the CLK pin or TIN pin as an input), the contents of the Counter Preload Register (CPR) is transferred to the counter the first time that the prescaler passes from $00 to $1F (rolls over) after entering the run state. Thereafter, the counter decrements or is loaded from the Counter Preload Register when the prescaler rolls over.
8. For configurations in which the prescaler is not used, the contents of the Counter Preload Registers are transferred to the counter on the first asserted edge of the TIN input after entering the run state. On subsequent asserted edges the counter decrements or is loaded from the Counter Preload Registers.
9. The lowest value allowed in the Counter Preload Register for use with the counter is $000001.

TIMER INTERRUPT ACKNOWLEDGE CYCLES

Several conditions may be present when the timer interrupt acknowledge pin ($\overline{\text{TIACK}}$) is asserted. These conditions affect the PI/T's response and the termination of the bus cycle. (See Table 9.)

TABLE 9 — RESPONSE TO TIMER INTERRUPT ACKNOWLEDGE

PC3/TOUT Function	Response to Asserted $\overline{\text{TIACK}}$
PC3 — Port C Pin	No response. No $\overline{\text{DTACK}}$.
TOUT — Square Wave	No response. No $\overline{\text{DTACK}}$.
TOUT — Negated Timer Interrupt Request	No response. No $\overline{\text{DTACK}}$.
TOUT — Asserted Timer Interrupt Request	Timer Interrupt Vector Contents. $\overline{\text{DTACK}}$ Asserted.

PROGRAMMER'S MODEL

The internal accessible register organization is represented in Table 10. Address space within the address map is reserved for future expansion. Throughout the PI/T data sheet the following conventions are maintained:

1. A read from a reserved location in the map results in a read from the "null register." The null register returns all zeros for data and results in a normal bus cycle. A write to one of these locations results in a normal bus cycle but no write occurs.
2. Unused bits of a defined register are denoted by "•" and are read as zeroes.
3. Bits that are unused in the chosen mode/submode but are used in others, are denoted by "X", and are readable and writeable. Their content, however, is ignored in the chosen mode/submode.
4. All registers are addressable as 8-bit quantities. To facilitate operation with the MOVEP instruction and the DMAC, addresses are ordered such that certain sets of registers may also be accessed as words (2 bytes) or long words (4 bytes).

TABLE 10 — PI/T REGISTER ADDRESSING ASSIGNMENTS

Register	Register Select Bits 5	4	3	2	1	Accessible	Affected by Reset	Affected by Read Cycle
Port General Control Register (PGCR)	0	0	0	0	0	R W	Yes	No
Port Service Request Register (PSRR)	0	0	0	0	1	R W	Yes	No
Port A Data Direction Register (PADDR)	0	0	0	1	0	R W	Yes	No
Port B Data Direction Register (PBDDR)	0	0	0	1	1	R W	Yes	No
Port C Data Direction Register (PCDDR)	0	0	1	0	0	R W	Yes	No
Port Interrupt Vector Register (PIVR)	0	0	1	0	1	R W	Yes	No
Port A Control Register (PACR)	0	0	1	1	0	R W	Yes	No
Port B Control Register (PBCR)	0	0	1	1	1	R W	Yes	No
Port A Data Register (PADR)	0	1	0	0	0	R W	No	**
Port B Data Register (PBDR)	0	1	0	0	1	R W	No	**
Port A Alternate Register (PAAR)	0	1	0	1	0	R	No	No
Port B Alternate Register (PBAR)	0	1	0	1	1	R	No	No
Port C Data Register (PCDR)	0	1	1	0	0	R W	No	No
Port Status Register (PSR)	0	1	1	0	1	R W*	Yes	No
Timer Control Register (TCR)	1	0	0	0	0	R W	Yes	No
Timer Interrupt Vector Register (TIVR)	1	0	0	0	1	R W	Yes	No
Counter Preload Register High (CPRH)	1	0	0	1	1	R W	No	No
Counter Preload Register Middle (CPRM)	1	0	1	0	0	R W	No	No
Counter Preload Register Low (CPRL)	1	0	1	0	1	R W	No	No
Count Register High (CNTRH)	1	0	1	1	1	R	No	No
Count Register Middle (CNTRM)	1	1	0	0	0	R	No	No
Count Register Low (CNTRL)	1	1	0	0	1	R	No	No
Timer Status Register (TSR)	1	1	0	1	0	R W*	Yes	No

* A write to this register may perform a special status resetting operation.
** Mode dependent.

R = Read
W = Write

Port General Control Register (PGCR) —

7	6	5	4	3	2	1	0
Port Mode Control		H34 Enable	H12 Enable	H4 Sense	H3 Sense	H2 Sense	H1 Sense

The Port General Control Register controls many of the functions that are common to the overall operation of the ports. The PGCR is composed of three major fields: bits 7 and 6 define the operational mode of Ports A and B and affect operation of the handshake pins and status bits; bits 5 and 4 allow a software controlled disabling of particular hardware associated with the handshake pins of each port; and bits 3-0 define the sense of the handshake pins. The PGCR is always readable and writeable.

All bits are reset to 0 when the RESET pin is asserted.

The Port Mode Control field should be altered only when the H12 Enable and H34 Enable bits are 0. Except when Mode 0 is desired, the Port General Control register must be written once to establish the mode, and again to enable the respective operation(s).

PGCR

7	6	Port Mode Control
0	0	Mode 0 (Unidirectional 8-Bit Mode)
0	1	Mode 1 (Unidirectional 16-Bit Mode)
1	0	Mode 2 (Bidirectional 8-Bit Mode)
1	1	Mode 3 (Bidirectional 16-Bit Mode)

PGCR

5	H34 Enable
0	Disabled
1	Enabled

PGCR

4	H12 Enable
0	Disabled
1	Enabled

PGCR

3-0	Handshake Pin Sense
0	The associated pin is at the high-voltage level when negated and at the low-voltage level when asserted.
1	The associated pin is at the low-voltage level when negated and at the high-voltage level when asserted.

Port Service Request Register (PSRR) –

7	6	5	4	3	2	1	0
*	SVCRQ Select		Interrupt PFS		Port Interrupt Priority Control		

The Port Service Request Register controls other functions that are common to the overall operation to the ports. It is composed of four major fields: bit 7 is unused and is always read as 0; bits 6 and 5 define whether interrupt or DMA requests are generated from activity on the H1 and H3 handshake pins; bits 4 and 3 determine whether two dual function pins operate as Port C or port interrupt request/-acknowledge pins; and bits 2, 1, and 0 control the priority among all port interrupt sources. Since bits 2, 1, and 0 affect interrupt operation, it is recommended that they be changed only when the affected interrupt(s) is (are) disabled or known to remain inactive. The PSRR is always readable and writeable.

All bits are reset to 0 when the $\overline{\text{RESET}}$ pin is asserted.

PSRR

6	5	SVCRQ Select
0	X	The PC4/$\overline{\text{DMAREQ}}$ pin carries the PC4 function; DMA is not used.
1	0	The PC4/$\overline{\text{DMAREQ}}$ pin carries the $\overline{\text{DMAREQ}}$ function and is associated with double-buffered transfers controlled by H1. H1 is removed from the PI/T's interrupt structure, and thus, does not cause interrupt requests to be generated. To obtain $\overline{\text{DMAREQ}}$ pulses, Port A Control Register bit 1 (H1 SVCRQ Enable) must be a 1.
1	1	The PC4/$\overline{\text{DMAREQ}}$ pin carries the $\overline{\text{DMAREQ}}$ function and is associated with double-buffered transfers controlled by H3. H3 is removed from the PI/T's interrupt structure, and thus, does not cause interrupt requests to be generated. To obtain $\overline{\text{DMAREQ}}$ pulses, Port B Control Register bit 1 (H3 SVCRQ Enable) must be 1.

PSRR

4	3	Interrupt Pin Function Select
0	0	The PC5/$\overline{\text{PIRQ}}$ pin carries the PC5 function. The PC6/$\overline{\text{PIACK}}$ pin carries the PC6 function.
0	1	The PC5/$\overline{\text{PIRQ}}$ pin carries the $\overline{\text{PIRQ}}$ function. The PC6/$\overline{\text{PIACK}}$ pin carries the PC6 function.
1	0	The PC5/$\overline{\text{PIRQ}}$ pin carries the PC5 function. The PC6/$\overline{\text{PIACK}}$ pin carries the $\overline{\text{PIACK}}$ function.
1	1	The PC5/$\overline{\text{PIRQ}}$ pin carries the $\overline{\text{PIRQ}}$ function. The PC6/$\overline{\text{PIACK}}$ pin carries the $\overline{\text{PIACK}}$ function.

Bits 2, 1, and 0 determine port interrupt priority. The priority is shown in descending order left to right.

PSRR 2	1	0	Port Interrupt Priority Control Highest ..... Lowest			
0	0	0	H1S	H2S	H3S	H4S
0	0	1	H2S	H1S	H3S	H4S
0	1	0	H1S	H2S	H4S	H3S
0	1	1	H2S	H1S	H4S	H3S
1	0	0	H3S	H4S	H1S	H2S
1	0	1	H3S	H4S	H2S	H1S
1	1	0	H4S	H3S	H1S	H2S
1	1	1	H4S	H3S	H2S	H1S

Port A Data Direction Register (PADDR) – The Port A Data Direction Register determines the direction and buffering characteristics of each of the Port A pins. One bit in the PADDR is assigned to each pin. A 0 indicates that the pin is used as an input, while a 1 indicates it is used as an output. The PADDR is always readable and writeable. This register is ignored in Mode 3.

All bits are reset to the 0 (input) state when the $\overline{\text{RESET}}$ pin is asserted.

Port B Data Direction Register (PBDDR) – The PBDDR is identical to the PADDR for the Port B pins and the Port B Data Register, except that this register is ignored in Modes 2 and 3.

Port C Data Direction Register (PCDDR) – The Port C Data Direction Register specifies whether each dual-function pin that is chosen for Port C operation is an input (0) or an output (1) pin. The PCDDR, along with bits that determine the respective pin's function, also specify the exact hardware to be accessed at the Port C Data Register address. (See the Port C Data Register description for more details.) The PCDDR is an 8-bit register that is readable and writeable at all times. Its operation is independent of the chosen PI/T mode.

These bits are cleared to 0 when the $\overline{\text{RESET}}$ pin is asserted.

Port Interrupt Vector Register (PIVR) –

7	6	5	4	3	2	1	0
Interrupt Vector Number						*	*

The Port Interrupt Vector Register contains the upper order six bits of the four port interrupt vectors. The contents of this register may be read two ways: by an ordinary read cycle, or by a port interrupt acknowledge bus cycle. The exact data read depends on how the cycle was initiated and other factors. Behavior during a port interrupt acknowledge cycle is summarized above in Table 3.

From a normal read cycle (CS), there is never a consequence to reading this register. Following negation of the RESET pin, but prior to writing to the PIVR, a $0F will be read. After writing to the register, the upper 6 bits may be read and the lower 2 bits are forced to 0. No prioritization computation is performed.

Port A Control Register (PACR) –

7	6	5	4	3	2	1	0
Port A Submode		H2 Control			H2 Int. Enable	H1 SVCRQ Enable	H1 Stat. Ctrl.

The Port A Control Register, in conjunction with the programmed mode and the Port B submode, control the operation of Port A and the handshake pins H1 and H2. The Port A Control Register contains five fields: bits 7 and 6 specify the Port A submode; bits 5, 4, and 3 control the operation of the H2 handshake pin and H2S status bit; bit 2 determines whether an interrupt will be generated when the H2S status bit goes to 1; bit 1 determines whether a service request (interrupt request or DMA request) will occur; bit 0 controls the operation of the H1S status bit. The PACR is always readable and writeable.

All bits are cleared to 0 when the RESET pin is asserted.

When the Port A submode field is relevant in a mode/submode definition, it must not be altered unless the H12 Enable bit in the Port General Control Register is 0. (See Table 2.)

The operation of H1 and H2 and their related status bits is given below, for each of the modes specified by Port General Control Register bits 7 and 6. This description is organized such that for each mode/submode all programmable options of each pin and status bit are given.

Bits 2 and 1 carry the same meaning in each mode/submode, and thus are specified only once.

PACR

2	H2 Interrupt Enable
0	The H2 interrupt is disabled.
1	The H2 interrupt is enabled.

PACR

1	H1 SVCRQ Enable
0	The H1 interrupt and DMA request are disabled.
1	The H1 interrupt and DMA request are enabled.

PACR Mode 0 Port A Submode 00

PACR

5	4	3	H2 Control
0	X	X	Input pin – status only.
1	0	0	Output pin – always negated.
1	0	1	Output pin – always asserted.
1	1	0	Output pin – interlocked input handshake protocol.
1	1	1	Output pin – pulsed input handshake protocol.

PACR

0	H1 Status Control
X	Not Used

PACR Mode 0 Port a Submode 01

PACR

5	4	3	H2 Control
0	X	X	Input pin – status only.
1	0	0	Output pin – always negated.
1	0	1	Output pin – always asserted.
1	1	0	Output pin – interlocked output handshake protocol.
1	1	1	Output pin – pulsed output handshake protocol.

PACR

0	H1 Status Control
0	The H1S status bit is 1 when either the Port A initial or final output latch can accept new data. It is 0 when both latches are full and cannot accept new data.
1	The H1S status bit is 1 when both of the Port A output latches are empty. It is 0 when at least one latch is full.

PACR Mode 0 Port A Submode 1X

PCR

5	4	3	H2 Control
0	X	X	Input pin – status only.
1	X	0	Output pin – always negated.
1	X	1	Output pin – always asserted.

PACR

0	H1 Status Control
X	Not used.

PACR Mode 1 Port A Submode XX Port B Submode X0

PACR

5	4	3	H2 Control
0	X	X	Input pin – status only.
1	X	0	Output pin – always negated.
1	X	1	Output pin – always asserted.

PACR

0	H1 Status Control
X	Not used.

PACR Mode 1 Port A Submode XX Port B Submode X1

PACR

5	4	3	H2 Control
0	X	X	Input pin – status only.
1	X	0	Output pin – always negated.
1	X	1	Output pin – always asserted.

PACR

0	H1 Status Control
X	Not used.

PACR Mode 2

PACR

5	4	3	H2 Control
X	X	0	Output pin — interlocked output handshake protocol.
X	X	1	Output pin — pulsed output handshake protocol.

PACR

0	H1 Status Control
0	The H1S status bit is 1 when either the Port B initial or final output latch can accept new data. It is 0 when both latches are full and cannot accept new data.
1	The H1S status bit is 1 when both of the Port B output latches are empty. It is 0 when at least one latch is full.

PACR Mode 3

PACR

5	4	3	H2 Control
X	X	0	Output pin — interlocked output handshake protocol.
X	X	1	Output pin — pulsed output handshake protocol.

PACR

0	H1 Status Control
0	The H1S status bit is 1 when either the initial or final output latch of Port A and B can accept new data. It is 0 when both latches are full and cannot accept new data.
1	The H1S status bit is 1 when both the initial and final output latches of Ports A and B are empty. It is 0 when either the initial or final latch of Ports A and B is full.

Port B Control Register (PBCR) —

7	6	5	4	3	2	1	0
Port B Submode		H4 Control			H4 Int. Enable	H3 SVCRQ Enable	H3 Stat. Ctrl.

The Port B Control Register specifies the operation of Port B and the handshake pins H3 and H4. The Port B control register contains five fields: bits 7 and 6 specify the Port B submode; bits 5, 4, and 3 control the operation of the H4 handshake pin and H4S status bit; bit 2 determines whether an interrupt will be generated when the H4S status bit goes to 1; bit 1 determines whether a service request (interrupt request or DMA request) will occur; bit 0 controls the operation of the H3S status bit. The PACR is always readable and writeable. There is never a consequence to reading the register.

All bits are cleared to 0 when the $\overline{\text{RESET}}$ pin is asserted.

When the Port B submode field is relevant in a mode/submode definition, it must not be altered unless the H34 Enable bit in the Port General Control Register is 0. (See Table 2.)

The operation of H3 and H4 and their related status bits is given below, for each of the modes specified by Port General Control Register bits 7 and 6. This description is organized such that for each mode/submode all programmable options of each pin and status bit are given.

Bits 2 and 1 carry the same meaning in each mode/submode, and thus are specified only once.

PBCR

2	H4 Interrupt Enable
0	The H4 interrupt is disabled.
1	The H4 interrupt is enabled.

PBCR

1	H3 SVCRQ Enable
0	The H3 interrupt and DMA request are disabled.
1	The H3 interrupt and DMA request are enabled.

PBCR Mode 0 Port B Submode 00

PBCR

5	4	3	H4 Control
0	X	X	Input pin — status only.
1	0	0	Output pin — always negated.
1	0	1	Output pin — always asserted.
1	1	0	Output pin — interlocked input handshake protocol.
1	1	1	Output pin — pulsed input handshake protocol.

PBCR

0	H3 Status Control
X	Not used.

PBCR Mode 0 Port B Submode 01

PBCR

5	4	3	H4 Control
0	X	X	Input pin — status only.
1	0	0	Output pin — always negated.
1	0	1	Output pin — always asserted.
1	1	0	Output pin — interlocked output handshake protocol.
1	1	1	Output pin — pulsed output handshake protocol.

PBCR

0	H3 Status Control
0	The H3S status bit is 1 when either the Port B initial or final output latch can accept new data. It is 0 when both latches are full and cannot accept new data.
1	The H3S status bit is 1 when both of the Port B output latches are empty. It is 0 when at least one latch is full.

PBCR Mode 0 Port B Submode 1X

PBCR

5	4	3	H4 Control
0	X	X	Input Pin — status only.
1	X	0	Output pin — always negated.
1	X	1	Output pin — always asserted.

PBCR

0	H3 Status Control
X	Not used.

PBCR Mode 1 Port B Submode X0

PBCR

5	4	3	H4 Control
0	X	X	Input pin — status only.
1	0	0	Output pin — always negated.
1	0	1	Output pin — always asserted.
1	1	0	Output pin — interlocked input handshake protocol.
1	1	1	Output pin — pulsed input handshake protocol.

PBCR

0	H3 Status Control
X	Not used.

PBCR Mode 1 Port B Submode X1

PBCR

5	4	3	H4 Control
0	X	X	Input pin — status only.
1	0	0	Output pin — always negated.
1	0	1	Output pin — always asserted.
1	1	0	Output pin — interlocked output handshake protocol.
1	1	1	Output pin — pulsed output handshake protocol.

PBCR

0	H3 Status Control
0	The H3S status bit is 1 when either the initial or final output latch of Port A and B can accept new data. It is 0 when both latches are full and cannot accept new data.
1	The H3S status bit is 1 when both the initial and final output latches of Ports A and B are empty. It is 0 when neither the initial or final latch of Ports A and B is full.

PBCR Mode 2

PBCR

5	4	3	H4 Control
X	X	0	Output pin — interlocked input handshake protocol.
X	X	1	Output pin — pulsed input handshake protocol.

PBCR

0	H3 Status Control
X	Not used.

PBCR Mode 3

PBCR

5	4	3	H4 Control
X	X	0	Output pin — interlocked input handshake protocol.
X	X	1	Output pin — pulsed input handshake protocol.

PBCR

0	H3 Status Control
X	Not used.

Port A Data Register (PADR) — The Port A Data Register is an address for moving data to and from the Port A pins. The Port A Data Direction Register determines whether each pin is an input (0) or an output (1), and is used in configuring the actual data paths. This is mode dependent and is described with the modes above.

This register is readable and writeable at all times. Depending on the chosen mode/submode, reading or writing may affect the double-buffered handshake mechanism. The Port A Data Register is not affected by the assertion of the $\overline{\text{RESET}}$ pin.

Port B Data Register (PBDR) — The Port B Data Register is an address for moving data to and from the Port B pins. The Port B Data Direction Register determines whether each pin is an input (0)or an output (1), and is used in configuring the actual data paths. This is mode dependent and is described with the modes, above.

This register is readable and writeable at all times. Depending on the chosen mode/submode, reading or writing may affect the double-buffered handshake mechanism. The Port B Data Register is not affected by the assertion of the $\overline{\text{RESET}}$ pin.

Port A Alternate Register (PAAR) — The Port A Alternate Register is an alternate address for reading the Port A pins. It is a read-only address and no other PI/T condition is affected. In all modes and the instantaneous pin level is read and no input latching is performed except at the data bus interface (see Bus Interface Connection). Writes to this address are answered with $\overline{\text{DTACK}}$, but the data is ignored.

Port B Alternate Register (PBAR) — The Port B Alternate Register is an alternate address for reading the Port B pins. It is a read-only address and no other PI/T condition is affected. In all modes the instantaneous pin level is read and no input latching is performed except at the data bus interface (see Bus Interface Connection). Writes to this address are answered with $\overline{\text{DTACK}}$, but the data is ignored.

Port C Data Register (PCDR) — The Port C Data Register is an address for moving data to and from each of the eight Port C/alternate-function pins. The exact hardware accessed is determined by the type of bus cycle (read or write) and individual conditions affecting each pin. These conditions are (1) whether the pin is used for the Port C or alternate function, and (2) whether the Port C Data Direction Register indicates the input or output direction. The Port C Data Register is single buffered for output pins and not buffered for input pins. These conditions are summarized in Table 11.

The Port C Data Register is not affected by the assertion of the $\overline{\text{RESET}}$ pin.

The operation of the PCDR is independent of the chosen PI/T mode.

TABLE 11 — PCDR HARDWARE ACCESSES

Read Port C Data Register			
Port C function PCDDR = 0	**Port C function PCDDR = 1**	**Alternate function PCDDR = 0**	**Alternate function PCDDR = 1**
pin	Port C output register	pin	Port C output register
Write Port C Data Register			
Port C Function PCDDR = 0	**Port C Function PCDDR = 1**	**Alternate function PCDDR = 0**	**Alternate function PCDDR = 1**
Port C output register, buffer disabled	Port C output register, buffer enabled	Port C output register	Port C output register

Note that two additional useful benefits result from this structure. First, it is possible to directly read the state of a dual-function pin while used for the non-Port C function. Second, it is possible to generate program controlled transitions on alternate-function pins by switching back to the Port C function, and writing to the PCDR.

This register is readable and writeable at all times.

Port Status Register (PSR) –

7	6	5	4	3	2	1	0
H4 Level	H3 Level	H2 Level	H1 Level	H4S	H3S	H2S	H1S

The Port Status Register contains information about handshake pin activity. Bits 7-4 show the instantaneous level of the respective handshake pin, and is independent of the handshake pin sense bits in the Port General Control Register. Bit 3-0 are the respective status bits referred to throughout this data sheet. Their interpretation depends on the programmed mode/submode of the PI/T. For Bits 3-0 a 1 is the active or asserted state.

Timer Control Register (TCR) –

7	6	5	4	3	2	1	0
TOUT/$\overline{\text{TIACK}}$ Control			Z.D. Ctrl.	*	Clock Control		Timer Enable

The Timer Control Register (TCR) determines all operations of the timer. Bits 7-5 configure the PC3/TOUT and PC7/$\overline{\text{TIACK}}$ pins for Port C, square wave, vectored interrupt, or autovectored interrupt operation; bit 4 specifies whether the counter receives data from the Counter Preload Register or continues counting when zero detect is reached; bit 3 is unused and is read as 0; bits 2 and 1 configure the path from the CLK and TIN pins to the counter controller; bit 0 enables the timer. This register is readable and writeable at all times.

All bits are cleared to 0 when the $\overline{\text{RESET}}$ pin is asserted.

TCR 7 6 5 — TOUT/$\overline{\text{TIACK}}$ Control

0 0 X The dual-function pins PC3/TOUT and PC7/$\overline{\text{TIACK}}$ carry the Port C function.

0 1 X The dual-function pin PC3/TOUT carries the TOUT function. In the run state it is used as a square wave output and is toggled on zero detect. The TOUT pin is high while in the halt state. The dual-function pin PC7/$\overline{\text{TIACK}}$ carries the PC7 function.

1 0 0 The dual-function pin PC3/TOUT carries the TOUT function. In the run or halt state it is used as a timer interrupt request output. The timer interrupt is disabled; thus, the pin is always three-stated. The dual-function pin PC7/$\overline{\text{TIACK}}$ carries the $\overline{\text{TIACK}}$ function; however, since interrupt request is negated, the PI/T produces no response, i.e., no data or $\overline{\text{DTACK}}$, to an asserted $\overline{\text{TIACK}}$. Refer to Timer Interrupt Cycle section for details. This combination and the 101 state below support vectored timer interrupts.

1 0 1 The dual-function pin PC3/TOUT carries the TOUT function and is used as a timer interrupt request output. The timer interrupt is enabled; thus, the pin is low when the timer ZDS status bit is 1. The dual function pin PC7/$\overline{\text{TIACK}}$ carries the $\overline{\text{TIACK}}$ function and is used as a timer interrupt acknowledge input. Refer to the Timer Interrupt Acknowledge Cycle section for details. This combination and the 100 state above support vectored timer interrupts.

1 1 0 The dual-function pin PC3/TOUT carries the TOUT function. In the run or halt state it is used as a timer interrupt request output. The timer interrupt is disabled; thus, the pin is always three-stated. The dual-function pin PC7/$\overline{\text{TIACK}}$ carries the PC7 function.

1 1 1 The dual-function pin PC3/TOUT carries the TOUT function and is used as a timer interrupt request output. The timer interrupt is enabled; thus, the pin is low when the timer ZDS status bit is 1. The dual-function pin PC7/$\overline{\text{TIACK}}$ carries the PC7 function and autovectored interrupts are supported.

TCR 4 — Zero Detect Control

0 The counter is loaded from the Counter Preload Register on the first clock to the 24-bit counter after zero detect, and resumes counting.

1 The counter rolls over on zero detect, then continues counting.

Bit 3 is unused and is always read as 0.

TCR 2 1 — Clock Control

0 0 The PC2/TIN input pin carries the Port C function and the CLK pin and prescaler are used. The prescaler is decremented on the falling transition of the CLK pin; the 24-bit counter is decremented or loaded from the Counter Preload Registers when the prescaler rolls over from $00 to $1F. The Timer Enable bit determines whether the timer is in the run or halt state.

0 1 The PC2/TIN pin serves as a timer input and the CLK pin and prescaler are used. The prescaler is decremented on the falling transition of the CLK pin; the 24-bit counter is decremented or loaded from the Counter Preload Registers when the prescaler rolls over from $00 to $1F. The timer is in the run state when the Timer Enable bit is 1 and the TIN pin is high; otherwise the timer is in the halt state.

1 0 The PC2/TIN pin serves as a timer input and the prescaler is used. The prescaler is decremented following the rising transition of the TIN pin after syncing with the internal clock. The 24-bit counter is decremented or loaded from the counter preload registers when the prescaler rolls over from $00 to $1F. The Timer Enable bit determines whether the timer is in the run or halt state.

1 1 The PC2/TIN pin serves as a timer input and the prescaler is unused. The 24-bit counter is decremented or loaded from the Counter Preload Registers following the rising edge of the TIN pin after syncing with the internal clock. The Timer Enable bit determines whether the timer is in the run or halt state.

TCR

0	Timer Enable
0	Disabled.
1	Enabled.

Timer Interrupt Vector Register (TIVR) — The timer interrupt vector register contains the 8-bit vector supplied when the timer interrupt acknowledge pin $\overline{TIACK}$ is asserted. The register is readable and writeable at all times, and the same value is always obtained from a normal read cycle and a timer interrupt acknowledge bus cycle ($\overline{TIACK}$). When the $\overline{RESET}$ pin is asserted the value of $0F is automatically loaded into the register. Refer to Timer Interrupt Acknowledge Cycle section for more details.

Counter Preload Register H, M, L (CPRH-L)

7	6	5	4	3	2	1	0	
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	CPRH
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	CPRM
Bit 7	Bit 6	Bit 5	Bir 4	Bit 3	Bit 2	Bit 1	Bit 0	CPRL

The Counter Preload Registers are a group of three 8-bit registers used for storing data to be transferred to the counter. Each of the registers is individually addressable, or the group may be accessed with the MOVEP .L or the MOVEP.W instructions. The address one less than the address of CPRH is the null register, and is reserved so that zeros are read in the upper 8 bits of the destination data register when a MOVEP.L is used. Data written to this address is ignored.

The registers are readable and writeable at all times. A read cycle proceeds independently of any transfer to the counter, which may be occuring simultaneously.

To insure proper operation of the PI/T Timer, a value of $000000 may not be stored in the Counter Preload Registers for use with the counter.

The $\overline{RESET}$ pin does not affect the contents of these registers.

Count Register H, M, L (CNTRH-L) —

7	6	5	4	3	2	1	0	
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	CNTRH
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	CNTRM
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	CNTRL

The count registers are a group of three 8-bit addresses at which the counter can be read. The contents of the counter are not latched during a read bus cycle; thus, the data read at these addresses is not guaranteed if the timer is in the run state. (Bits 2, 1, and 0 of the Timer Control Register specify the state.) Write operations to these addresses result in a normal bus cycle but the data is ignored.

Each of the registers is individually addressable, or the group may be accessed with the MOVEP.L or the MOVEP.W instructions. The address one less than the address of CNTRH is the null register, and is reserved so that zeros are read in the upper 8 bits of the destination data register when a MOVEP.L is used. Data written to this address is ignored.

Timer Status Register (TSR) —

7	6	5	4	3	2	1	0
*	*	*	*	*	*	*	ZDS

The Timer Status Register contains one bit from which the zero detect status can be determined. The ZDS status bit (bit 0) is an edge-sensitive flip-flop that is set to 1 when the 24-bit counter decrements from $000001 to $000000. The ZDS status bit is cleared to 0 following the direct clear operation (similar to that of the ports), or when the timer is halted. Note also that when the RESET pin is asserted the timer is disabled, and thus enters the halt state.

This register is always readable without consequence. A write access performs a direct clear operation if bit 0 in the written data is 1. Following that, the ZDS bit is 0.

This register is constructed with a reset dominant S-R flip-flop so that all clearing conditions prevail over the possible zero detect condition.

Bits 7-1 are unused and are read as 0.

TIMER APPLICATIONS SUMMARY

This section outlines programming of the Timer Control Register for several typical examples.

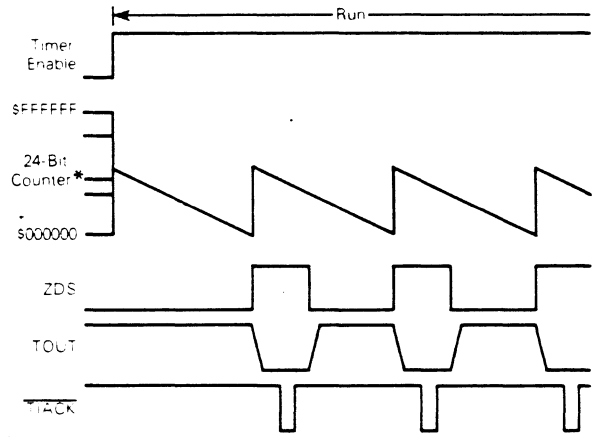
Periodic Interrupt Generator

7	6	5	4	3	2	1	0
TOUT $\overline{TIACK}$ Control			Z D Ctrl	*	Clock Control		Timer Enable
1	X	1	0	0	00 or 1X		changed

In this configuration the timer generates a periodic interrupt. The TOUT pin is connected to the system's interrupt request circuitry and the $\overline{TIACK}$ pin may be used as an interrupt acknowledge input to the timer. The TIN pin may be used as a clock input.

The processor loads the Counter Preload Registers and Timer Control Register, and then enables the timer. When the 24-bit counter passes from $000001 to $000000 the ZDS status bit is set and the TOUT (interrupt request) pin is asserted. At the next clock to the 24-bit counter it is again loaded with the contents of the CPR's, and thereafter decrements. In normal operation, the processor must direct clear the status bit to negate the interrupt request (see Figure 15).

FIGURE 15 — PERIODIC INTERRUPT GENERATOR



* Analog representation of counter value

Square Wave Generator

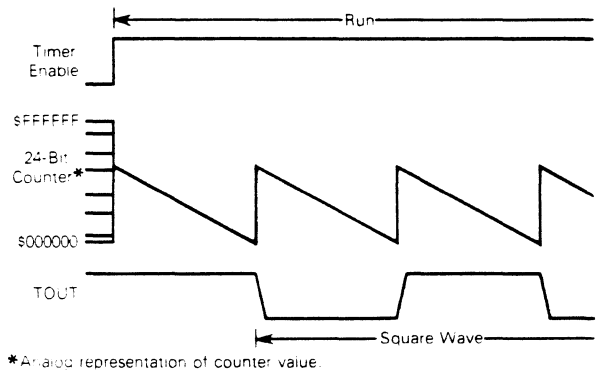
7	6	5	4	3	2	1	0
TOUT/TIACK Control			Z. D. Ctrl.	*	Clock Control		Timer Enable
0	1	X	1	0	00 or 1X		changed

In this configuration the timer produces a square wave at the TOUT pin. The TOUT pin is connected to the user's circuitry and the TIACK pin is not used. The TIN pin may be used as a clock input.

The processor loads the Counter Preload Registers and Timer Control Register, and then enables the timer. When the 24-bit counter passes from $000001 to $000000 the ZDS status bit is set and the TOUT (square wave output) pin is toggled. At the next clock to the 24-bit counter it is again loaded with the contents of the CPRs, and thereafter decrements. In this application there is no need for the processor to direct clear the ZDS status bit; however, it is possible for the processor to sync itself with the square wave by clearing the ZDS status bit, then polling it. The processor may also read the TOUT level at the Port C address.

Note that the PC3/TOUT pin functions as PC3 following the negation of RESET. If used in the square wave configuration a pullup resistor may be required to keep a known level prior to programming. Prior to enabling the timer, TOUT is high (see Figure 16).

FIGURE 16 — SQUARE WAVE GENERATOR



* Analog representation of counter value.

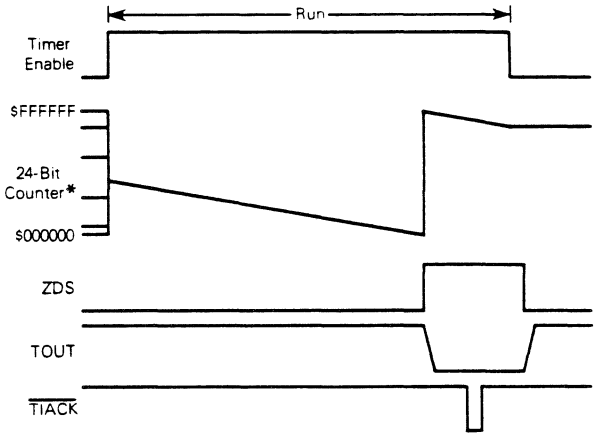
Interrupt After Timeout

7	6	5	4	3	2	1	0
TOUT/TIACK Control			Z. D. Ctrl.	*	Clock Control		Timer En.
1	X	1	1	0	00 or 1X		changed

In this configuration the timer generates an interrupt after a programmed time period has expired. The TOUT pin is connected to the system's interrupt request circuitry and the TIACK pin may be an interrupt acknowledge input to the timer. The TIN pin may be used as a clock input.

This configuration is similar to the periodic interrupt generator except that the Zero Detect Control bit is set. This forces the counter roll over after Zero Detect is reached, rather than reloading from the CPRs. When the processor takes the interrupt it can halt the timer and read the counter. This allows the processor to measure the delay time from Zero Detect (interrupt request) to entering the service routine. Accurate knowledge of the interrupt latency may be useful in some applications (see Figure 17).

FIGURE 17 — SINGLE INTERRUPT AFTER TIMEOUT



* Analog representation of counter value.

Elapsed Time Measurement

Elapsed time measurement takes several forms; two are described below.

System Clock

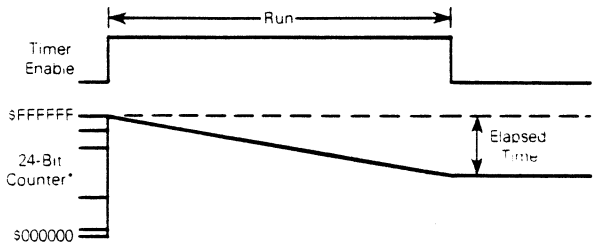
7	6	5	4	3	2	1	0
TOUT/TIACK Control			Z. D. Ctrl.	*	Clock Control		Timer Enable
0	0	X	1	0	0	0	changed

This configuration allows time interval measurement by software. No timer pins are used.

The processor loads the Counter Preload Registers (generally with all 1s) and Timer Control Register, and then enables the timer. The counter decrements until the ending event takes place. When it is desired to read the time interval, the processor must halt the timer, then read the counter.

For applications in which the interval could have exceeded that programmable in this timer, interrupts can be counted to provide the equivalent of additional timer bits. At the end, the timer can be halted and read (see Figure 18).

FIGURE 18 — ELAPSED TIME MEASUREMENT



*Analog representation of counter values.

External Clock

7	6	5	4	3	2	1	0
TOUT/$\overline{\text{TIACK}}$ Control			Z. D Ctrl.	*	Clock Control		Timer Enable
0	0	X	1	0	1	X	changed

This configuration allows measurement (counting) of the number of input pulses occurring in an interval in which the counter is enabled. The TIN input pin provides the input pulses. Generally the TOUT and $\overline{\text{TIACK}}$ pins are not used.

This configuration is identical to the Elapsed Time Measurement/System Clock configuration except that the TIN pin is used to provide the input frequency. It can be connected to a simple oscillator, and the same methods could be used. Alternately, it could be gated off and on externally and the number of cycles occurring while in the run state can be counted. However, minimum pulse width high and low specifications must be met.

Device Watchdog

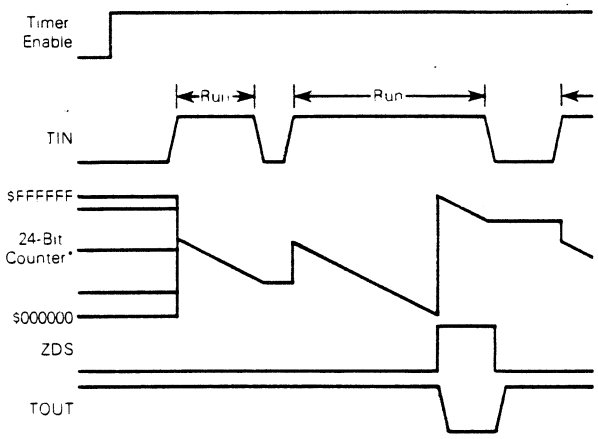
7	6	5	4	3	2	1	0
TOUT/$\overline{\text{TIACK}}$ Control			Z. D Ctrl.	*	Clock Control		Timer Enable
1	X	1	1	0	0	1	changed

This configuration provides the watchdog function needed in many systems. The TIN pin is the timer input whose period at the high (1) level is to be checked. Once allowed by the processor, the TIN input pin controls the run/halt mode. The TOUT pin is connected to external circuitry requiring notification when the TIN pin has been asserted longer than the programmed time. The $\overline{\text{TIACK}}$ pin (interrupt acknowledge) is only needed if the TOUT pin is connected to interrupt circuitry.

The processor loads the Counter Preload Register and Timer Control Register, and then enables the timer. When the TIN input is asserted (1, high) the timer transfers the contents of the Counter Preload Register to the counter and begins counting. If the TIN input is negated before Zero Detect is reached, the TOUT output and the ZDS status bit remain negated. If Zero Detect is reached while the TIN input is still asserted the ZDS status bit is set and the TOUT output is asserted. (The counter rolls over and keeps on counting.)

In either case, when the TIN input is negated the ZDS status bit is 0, the TOUT output is negated, the counting stops, and the prescaler is forced to all 1s (see Figure 19).

FIGURE 19 — DEVICE WATCHDOG



*Analog representation of counter value.

BUS INTERFACE CONNECTION

The PI/T has an asynchronous bus interface, primarily designed for use with the MC68000 microprocessor. With care, however, it can be connected to synchronous microprocessor buses. This section completely describes the PI/T's bus interface, and is intended for the asynchronous bus designer unless otherwise mentioned.

In an asynchronous system the PI/T CLK may operate at a significantly different frequency, either higher or lower, than the bus master and other system components, as long as all bus specifications are met. The MC68230 CLK pin has the same specifications as the MC68000 CLK, and must not be gated off at any time.

The following signals generate normal read and write cycles to the PI/T: $\overline{\text{CS}}$ (Chip Select), R/$\overline{\text{W}}$ (Read/Write), RS1-RS5 (five Register Select bits), D0-D7 (the 8-bit bidirectional data bus), and $\overline{\text{DTACK}}$ (Data Transfer Acknowledge). To generate interrupt acknowledge cycles PC6/$\overline{\text{PIACK}}$ or PC7/$\overline{\text{TIACK}}$ is used instead of $\overline{\text{CS}}$, and the Register Select pins are ignored. No combination of the following pins may be asserted simultaneously: $\overline{\text{CS}}$, $\overline{\text{PIACK}}$, or $\overline{\text{TIACK}}$.

READ CYCLES VIA CHIP SELECT

This catagory includes all register reads, except port or timer interrupt acknowledge cycles. When $\overline{\text{CS}}$ is asserted, the Register Select and R/$\overline{\text{W}}$ inputs are latched internallly. They must meet small setup and hold time requirements with respect to the asserted edge of $\overline{\text{CS}}$. (See the AC ELECTRICAL CHARACTERISTICS table.) The PI/T is *not* protected against aborted (shortened) bus cycles generated by an Address Error or Bus Error exception in which it is addressed.

Certain operations triggered by normal read (or write) bus cycles are not complete within the time allotted to the bus cycle. One example is transfers to/from the double-buffered latches that occur as a result of the bus cycle. If the bus master's CLK is significantly faster than the PI/T's the possibility exists that, following the bus cycle, $\overline{\text{CS}}$ can be

negated then re-asserted before completion of these internal operations. In this situation the PI/T does not recognize the re-assertion of $\overline{CS}$ until these operations are complete. Only at that time does it begin the internal sequencing necessary to react to the asserted $\overline{CS}$. Since $\overline{CS}$ also controls the $\overline{DTACK}$ response, this "bus cycle recovery time" can be related to the CLK edge on which $\overline{DTACK}$ is asserted for that cycle. The PI/T will recognize the subsequent assertion of $\overline{CS}$ three (3) CLK periods after the CLK edge on which $\overline{DTACK}$ was previously asserted.

The Register Select and R/$\overline{W}$ inputs pass through an internal latch that is transparent when the PI/T can recognize a new $\overline{CS}$ pulse (see above paragraph). Since the internal data bus of the PI/T is continuously enabled for read transfers, the read access time (to the data bus buffers) begins when the Register Selects are stabilized internally. Also, when the PI/T is ready to begin a new bus cycle, the assertion of $\overline{CS}$ enables the data bus buffers within a short propagation delay. This does not contribute to the overall read access time unless $\overline{CS}$ is asserted significantly after the Register Select and R/$\overline{W}$ inputs are stabilized (as may occur with synchronous bus microprocessors).

In addition to Chip Select's previously mentioned duties, it controls the assertion of $\overline{DTACK}$ and latching of read data at the data bus interface. Except for controlling input latches and enabling the data bus buffers, all of these functions occur only after $\overline{CS}$ has been recognized internally and synchronized with the internal clock. Chip Select is recognized on the falling edge of the CLK if the setup time is met, $\overline{DTACK}$ is asserted (low) on the next falling edge of the CLK. Read data is latched at the PI/T's data bus interface at the same time $\overline{DTACK}$ is asserted. It is stable as long as Chip Select remains asserted independent of other external conditions.

From the above discussion it is clear that if the $\overline{CS}$ setup time prior to the falling edge of the CLK is met, the PI/T can consistently respond to a new read or write bus cycle every four (4) CLK cycles. This fact is especially useful in designing the PI/T's clock in synchronous bus systems not using $\overline{DTACK}$. (An extra CLK period is required in interrupt acknowledge cycles, see Read Cycles via Interrupt Acknowledge.)

In asynchronous bus systems in which the PI/T's CLK differs from that of the bus master, generally there is no way to guarantee that the $\overline{CS}$ setup time with respect to the PI/T CLK is met. Thus, the only way to determine that the PI/T recognized the assertion of $\overline{CS}$ is to wait for the assertion of $\overline{DTACK}$. In this situation, all latched bus inputs to the PI/T must be held stable until $\overline{DTACK}$ is asserted. These include Register Select, R/$\overline{W}$, and write data inputs (see below).

System specifications impose a maximum delay from the trailing (negated) edge of Chip Select to the negated edge of $\overline{DTACK}$. As system speeds increase this becomes more difficult to meet with a simple pullup resistor tied to the $\overline{DTACK}$ line. Therefore, the PI/T provides an internal active pullup device to reduce the rise time, and a level-sensitive circuit that later turns this device off. $\overline{DTACK}$ is negated asynchronously as fast as possible following the rising edge of Chip Select, then three-stated to avoid interference with the next bus cycle.

The system designer must take care that $\overline{DTACK}$ is negated and three-stated quickly enough after each bus cycle to avoid interference with the next one. With the MC68000 this necessitates a relatively fast external path from the data strobe to $\overline{CS}$ going negated.

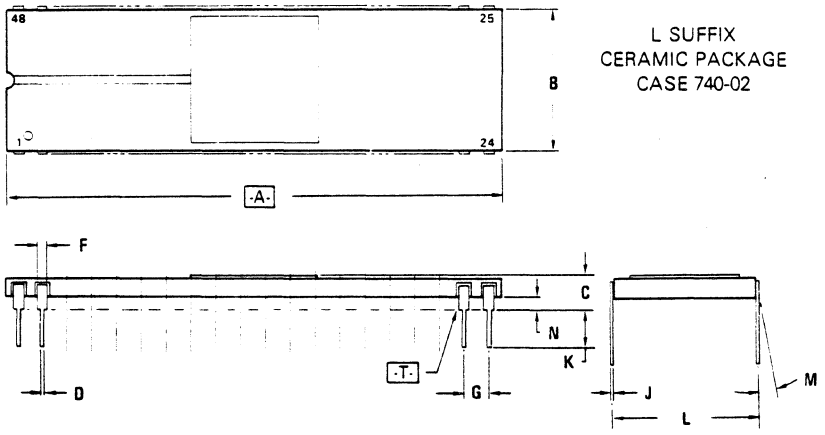
WRITE CYCLES

In many ways write cycles are similar to normal read cycles (see above). On write cycles, data at the D0-D7 pins must meet the same setup specifications as the Register Select and R/$\overline{W}$ lines. Like these signals, write data is latched on the asserted edge of $\overline{CS}$, and must meet small setup and hold time requirements with respect to that edge. The same bus cycle recovery conditions exist as for normal read cycles. No other differences exist.

READ CYCLES VIA INTERRUPT ACKNOWLEDGE

Special internal operations take place on PI/T interrupt acknowledge cycles. The Port Interrupt Vector Register or the Timer Interrupt Vector Register are implicitly addressed by the assertion of PC6/$\overline{PIACK}$ or PC7/$\overline{TIACK}$, respectively. The signals are first synchronized with the falling edge of the CLK. One clock period after they are recognized the data bus buffers are enabled and the vector is driven onto the bus. $\overline{DTACK}$ is asserted after another clock period to allow the vector some setup time prior to $\overline{DTACK}$. $\overline{DTACK}$ is negated, then three-stated as with normal read or write cycle, when $\overline{PIACK}$ or $\overline{TIACK}$ is negated.

PACKAGE DIMENSIONS



L SUFFIX
CERAMIC PACKAGE
CASE 740-02

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	60.35	61.57	2.376	2.424
B	14.63	15.34	0.576	0.604
C	3.05	4.32	0.120	0.160
D	0.381	0.533	0.015	0.021
F	0.762	1.397	0.030	0.055
G	2.54 BSC		0.100 BSC	
J	0.203	0.330	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.99	15.65	0.590	0.616
M	0°	10°	0°	10°
N	1.016	1.524	0.040	0.060

NOTES:
1. DIMENSION -A- IS DATUM.
2. POSTIONAL TOLERANCE FOR LEADS:
   ⌖ Ø 0.25 (0.010) Ⓜ T A Ⓜ
3. -T- IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

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ADI-660

R68560, R68561
MULTI-PROTOCOL COMMUNICATIONS CONTROLLER (MPCC)

PRELIMINARY

DESCRIPTION

The R68560, R68561 Multi-Protocol Communications Controller (MPCC) interfaces a single serial communications channel to a 68008/68000 microcomputer-based system using either asynchronous or synchronous protocol. High speed bit rate, automatic formatting, low overhead programming, eight character buffering, two channel DMA interface and three separate interrupt vector numbers optimize MPCC performance to take full advantage of the 68008/68000 processing capabilities and asynchronous bus structure.

In synchronous operation, the MPCC supports bit-oriented protocols (BOP), such as SDLC/HDLC, and character-oriented protocols (COP), such as IBM Bisync (BSC) in either ASCII or EBCDIC coding. Formatting, synchronizing, validation and error detection is performed automatically in accordance with protocol requirements and selected options. Asynchronous (ASYNC) and isochronous (ISOC) modes are also supported. In addition, modem interface handshake signals are available for general use.

Control, status and data are transferred between the MPCC and the microcomputer bus via 22 directly addressable registers and a DMA interface. Two first-in first-out (FIFO) registers, addressable through separate receiver and transmitter data registers, each buffer up to eight characters at a time to allow more MPU processing time to service data received or to be transmitted and to maximize bus throughput, especially during DMA operation. The two-channel Direct Memory Access (DMA) interface operates with the MC68440/MC68450 DMA Controller. Three prioritized interrupt vector numbers separately support receiver, transmitter and modem interface operation.

An on-chip oscillator drives the internal baud rate generator (BRG) and an external clock output with an 8 MHz input crystal or clock frequency. The BRG, in conjunction with two selectable prescalers and 16-bit programmable divisor, provides a data bit rate of DC to 4 MHz.

The 48-pin R68561 supports word-length (16-bit) operation when connected to the 68000 16-bit asynchronous bus, as well as byte-length (8-bit) operation when connected to the 68008 8-bit bus. The 40-pin R68560 supports byte-length operation on the 68008 bus.

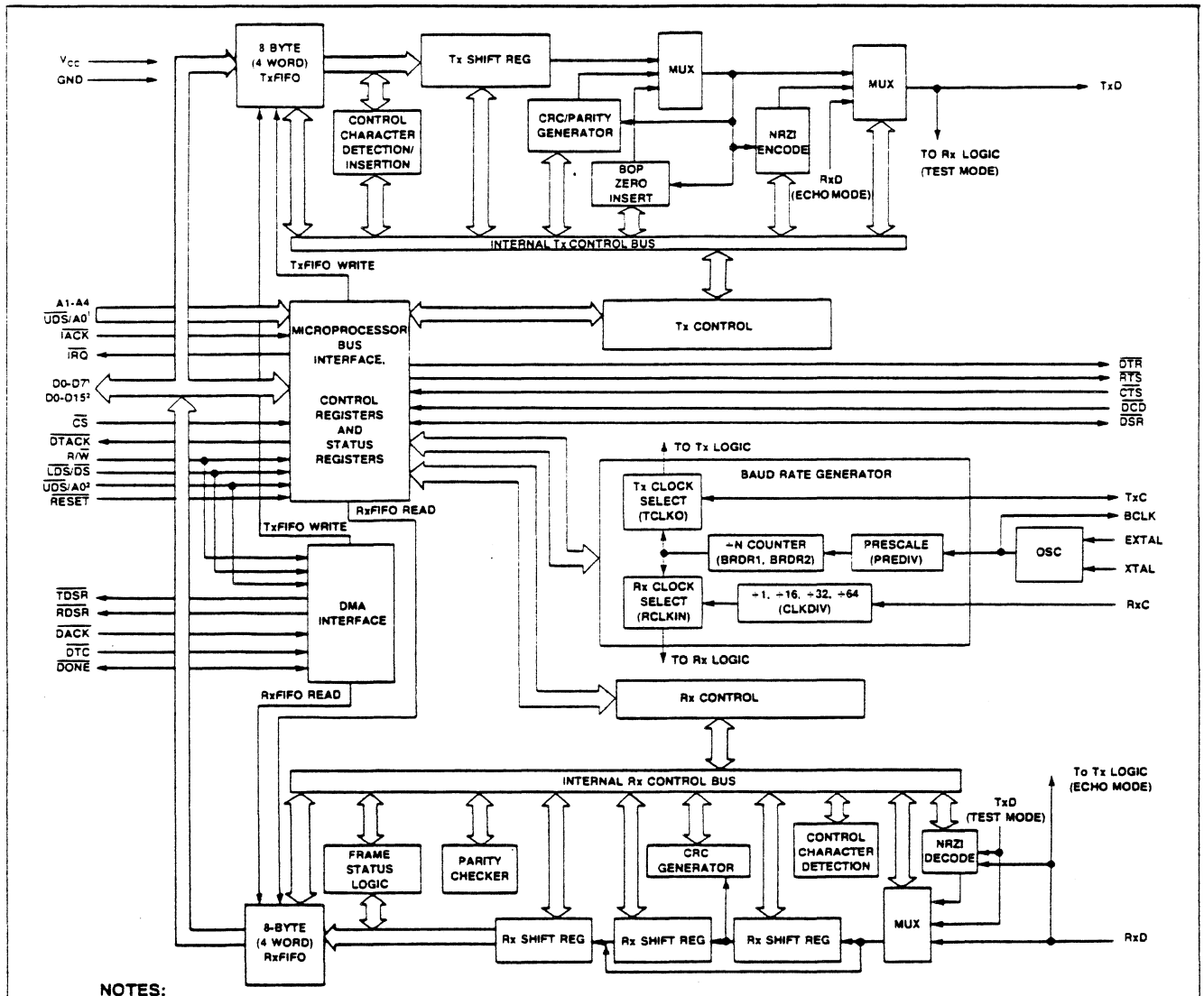
FEATURES

- Full duplex synchronous/asynchronous receiver and transmitter
- Fully implements IBM Binary Synchronous Communications (BSC) in two coding formats: ASCII and EBCDIC
- Supports other synchronous character-oriented protocols (COP), such as six-bit BSC, DDCMP, X3.28, ISO IS1745, ECMA-16, etc.
- Supports synchronous bit-oriented protocols (BOP), such as SDLC, HDLC/ADCCP, X.25, etc.
- Asynchronous and isochronous modes
- Modem handshake interface
- High speed serial data rate (DC to 4 MHz)
- Internal oscillator and Baud Rate Generator (BRG) with programmable data rate
- Crystal or TTL level clock input and buffered clock output (8 MHz)
- Direct interface to 68008/68000 asynchronous bus
- Eight-character receiver and transmitter buffer registers
- 22 directly addressable registers for flexible option selection, complete status reporting, and data transfer
- Three separate programmable interrupt vector numbers for receiver, transmitter and serial interface
- Maskable interrupt conditions for receiver, transmitter and serial interface.
- Programmable microprocessor bus data transfer: polled, interrupt and two-channel DMA transfer compatible with MC68440/MC68450
- Clock control register for receiver clock divisor and receiver and transmitter clock routing
- Selectable full/half duplex, autoecho and local loop-back modes
- Selectable parity (enable, odd, even) and CRC (control field enable, CRC-16, CCITT V.41, VRC/LRC)

ORDERING INFORMATION

Part Number	Frequency	Temperature Range
R6856_ _	4 MHz	0°C to 70°C

R6856_ _
- Package: C = Ceramic, P = Plastic
- Number of pins: 0 = 40, 1 = 48



NOTES:
1. Byte mode on 68008 bus.
2. Word mode on 68000 bus.

FIGURE 1. MPCC Block Diagram

PIN DESCRIPTION

Throughout the data sheet, signals are presented using the terms active and inactive or asserted and negated independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is described below.) Active low signals are denoted by a superscript bar. R/$\overline{W}$ indicates a write is active low and a read active high.

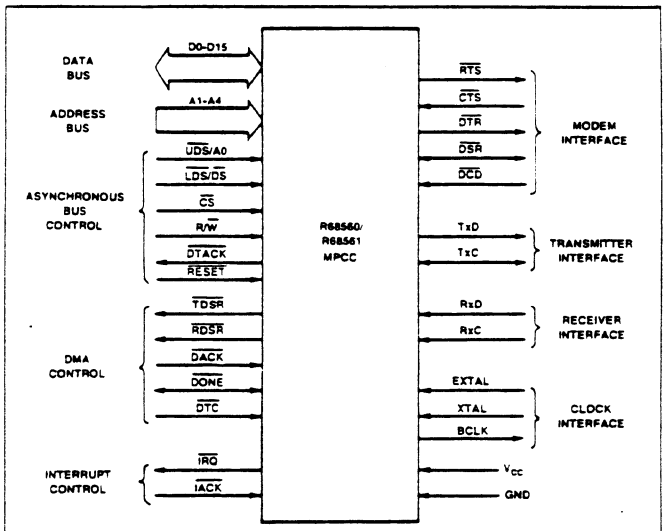


FIGURE 2. MPCC Input and Output Signals

A1-A4—Address Lines. A1-A4 are active high inputs used in conjunction with the $\overline{CS}$ input to access the internal registers. The address map for these registers is shown in Table 1. A0 is valid only in byte mode. For 68000 asynchronous bus interface A0 = $\overline{UDS}$.

D0-D15—Data Lines. The bidirectional data lines transfer data between the MPCC and the MPU, memory or other peripheral device. D0-D15 are used when connected to the 16-bit 68000 bus and operating in the MPCC word mode. D0-D7 are used when connected to the 16-bit 68000 bus or the 8-bit 68008 bus and operating in the MPCC byte mode. The data bus is three-stated when $\overline{CS}$ is inactive. (See exceptions in DMA mode.)

$\overline{CS}$—Chip Select. $\overline{CS}$ low selects the MPCC for programmed transfers with the host. The MPCC is deselected when the $\overline{CS}$ input is inactive in non-DMA mode. $\overline{CS}$ must be decoded from the address bus and gated with address strobe ($\overline{AS}$).

R/$\overline{W}$—Read/Write. R/$\overline{W}$ controls the direction of data flow through the bidirectional data bus by indicating that the current bus cycle is a read (high) or write (low) cycle.

$\overline{DTACK}$—Data Transfer Acknowledge. $\overline{DTACK}$ is an active low output that signals the completion of the bus cycle. During read or interrupt acknowledge cycles, $\overline{DTACK}$ is asserted by the MPCC after data has been provided on the data bus; during write cycles it is asserted after data has been accepted at the data bus. $\overline{DTACK}$ is driven high after assertion prior to being tri-stated. A holding resistor is required to maintain $\overline{DTACK}$ high between bus cycles.

$\overline{LDS}$/$\overline{DS}$—Lower Data Strobe/Data Strobe. During a write (R/$\overline{W}$ low), the $\overline{LDS}$ positive transition latches data on data bus lines D0-D7 into the MPCC. During a read (R/$\overline{W}$ high), $\overline{LDS}$ low enables data from the MPCC to data bus lines D0-D7.

$\overline{UDS}$/A0—Upper Data Strobe/Address Line A0. When interfacing the R68561 to the 68000 16-bit bus, the data bus UDS signal is connected to the $\overline{UDS}$/A0 input. During a write (R/$\overline{W}$ low), the $\overline{UDS}$ positive transition latches data on data lines D8-D15 into the MPCC (word mode only). During a read (R/$\overline{W}$ high), $\overline{UDS}$ low enables data from the MPCC to data bus lines D8-D15 (word mode only). In the byte mode, $\overline{UDS}$ is used internally by the MPCC as A0 to address a register byte (see Table 1).

When interfacing the R68560 to the 68008 8-bit bus, data bus A0 line is connected to the $\overline{UDS}$/A0 input and is used to access an internal register byte (see Table 1).

$\overline{IRQ}$—Interrupt Request. The active low $\overline{IRQ}$ output requests interrupt service by the MPU. $\overline{IRQ}$ is driven high after assertion prior to being tri-stated.

$\overline{IACK}$—Interrupt Acknowledge. The active low $\overline{IACK}$ input indicates that the current bus cycle is an interrupt acknowledge cycle. When $\overline{IACK}$ is asserted the MPCC places an interrupt vector on the lower byte (D0-D7) of the data bus.

$\overline{TDSR}$—Transmitter Data Service Request. When Transmitter DMA mode is active, the low $\overline{TDSR}$ output requests DMA service.

$\overline{RDSR}$—Receiver Data Service Request. When receiver DMA mode is active, the low $\overline{RDSR}$ output requests DMA service.

$\overline{DACK}$—DMA Acknowledge. The $\overline{DACK}$ low input indicates that the data bus has been acquired by the DMAC and that the requested bus cycle is beginning.

$\overline{DTC}$—Data Transfer Complete. The $\overline{DTC}$ low input indicates that a DMA data transfer is complete. $\overline{DTC}$ in response to a $\overline{RDSR}$ indicates that the data has been successfully stored in memory. $\overline{DTC}$ in response to a $\overline{TDSR}$ indicates that the data is present on the data bus for strobing into the MPCC. $\overline{DTC}$ is used in conjunction with R/$\overline{W}$ to increment the TxFIFO or RxFIFO pointer.

$\overline{DONE}$—Done. $\overline{DONE}$ is a bidirectional active low signal. The $\overline{DONE}$ signal is asserted by the DMAC when the DMA transfer count is exhausted and there is no more data to be transferred, or asserted by the MPCC when the status byte following the last character of a frame (block) is being transferred in response to a $\overline{RDSR}$. The $\overline{DONE}$ signal asserted by the DMAC in response to a $\overline{TDSR}$ will be stored to track with the data byte (lower byte for word transfer) through the TxFIFO.

$\overline{RESET}$—Reset. $\overline{RESET}$ is an active low, high impedance input that initializes all MPCC functions. $\overline{RESET}$ must be asserted for at least 500 ns to initialize the MPCC.

$\overline{DTR}$—Data Terminal Ready. The $\overline{DTR}$ active low output is general purpose in nature, and is controlled by the DTRLVL bit in the Serial Interface Control Register (SICR).

$\overline{RTS}$—Request to Send. The $\overline{RTS}$ active low output is general purpose in nature, and is controlled by the RTSLVL bit in the SICR.

$\overline{CTS}$—Clear to Send. The $\overline{CTS}$ active low input positive transition and level are reported in the CTS and CTSLVL bits in the Serial Interface Status Register (SISR), respectively.

$\overline{DSR}$—Data Set Ready. The $\overline{DSR}$ active low input negative transition and level are reported in the DSR and DSRLVL bits in the SISR, respectively.

$\overline{DCD}$—Data Carrier Detect. The $\overline{DCD}$ active low input positive transition and level are reported in the DCD and DCDLVL bits in the SISR, respectively.

TxD—Transmitted Data. The MPCC transmits serial data on the TxD output. The TxD output changes on the negative going edge of TxC.

RxD—Received Data. The MPCC receives serial data on the RxD input. The RxD input is shifted into the receiver with the positive going edge of RxC.

TxC—Transmitter Clock. TxC can be programmed to be an input or an output. When TxC is selected to be an input, the transmitter clock must be provided externally. When TxC is programmed to be an output, a clock is generated by the MPCC's internal baud rate generator. The low-to-high transition of the clock signal nominally indicates the center of a serial data bit present on the TxD output.

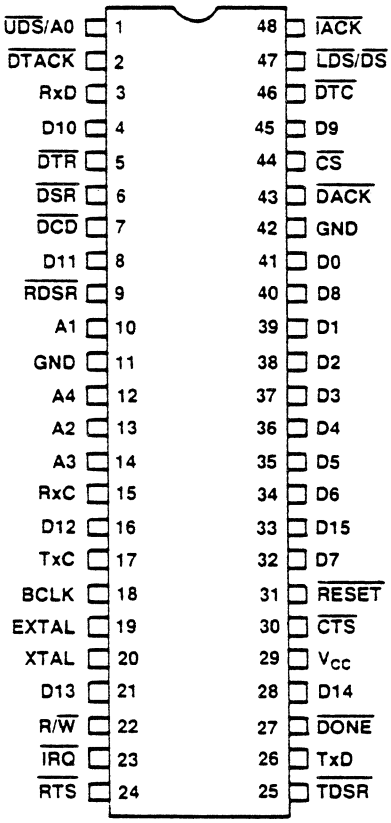
RxC—Receiver Clock. RxC provides the MPCC receiver with received data timing information. The clock transition from low-to-high nominally indicates the center of each serial data bit on the RxD input.

EXTAL—Crystal/External Clock Input.
XTAL Crystal Return. EXTAL and XTAL connect an 8 MHz external crystal to the MPCC internal oscillator. The pin EXTAL may also be used as a TTL level input to supply a DC to 8 MHz reference timing from an external clock source. XTAL must be tied to ground when applying an external clock to the EXTAL input.

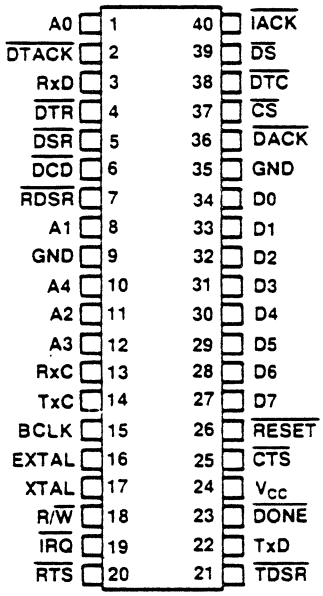
BCLK—Buffered Clock. BCLK is the internal oscillator buffered output available to other MPCC devices eliminating the need for additional crystals.

Vcc—Power. 5 V ± 5%.

GND—Ground. Ground (V_{SS}).



R68561 Pin Configuration



R68560 Pin Configuration

MPCC REGISTERS

Twenty-four 8-bit registers define, control and monitor the data communications process. These registers and their addresses are listed in Table 1.

In the word mode, two registers are read or written at a time starting at an even boundary (A0 is not used in the word mode and is implied to be 0). In the byte mode, each register is explicitly addressed based on A0.

Table 2 summarizes the MPCC register bit assignments. A read from an unassigned location results in a read from the "null register." The null register returns all ones for data and results in a normal bus cycle. Unused bits of a defined register are read as zeros unless otherwise noted.

TABLE 1. MPCC Accessible Registers

Register	Hex Addr	Address Bits					Access	Initialized by $\overline{\text{RESET}}$
		A4	A3	A2	A1	A0		
Receiver Status Register (RSR)	00	0	0	0	0	0	R/W	Yes
Receiver Control Register (RCR)	01	0	0	0	0	1	R/W	Yes
Receiver Data Register (RDR)	02	0	0	0	1	0	R	No*
Receiver Interrupt Vector Number Register (RIVNR)	04	0	0	1	0	0	R/W	Yes
Receiver Interrupt Enable Register (RIER)	05	0	0	1	0	1	R/W	Yes
Transmitter Status Register (TSR)	08	0	1	0	0	0	R/W	Yes
Transmitter Control Register (TCR)	09	0	1	0	0	1	R/W	Yes
Transmitter Data Register (TDR)	0A	0	1	0	1	0	W	No*
Transmitter Interrupt Vector Number Register (TIVNR)	0C	0	1	1	0	0	R/W	Yes
Transmitter Interrupt Enable Register (TIER)	0D	0	1	1	0	1	R/W	Yes
Serial Interface Status Register (SISR)	10	1	0	0	0	0	R/W	Yes
Serial Interface Control Register (SICR)	11	1	0	0	0	1	R/W	Yes
Serial Interrupt Vector Number Register (SIVNR)	14	1	0	1	0	0	R/W	Yes
Serial Interrupt Enable Register (SIER)	15	1	0	1	0	1	R/W	Yes
Protocol Select Register 1 (PSR1)	18	1	1	0	0	0	R/W	Yes
Protocol Select Register 2 (PSR2)	19	1	1	0	0	1	R/W	Yes
Address Register 1 (AR1)	1A	1	1	0	1	0	R/W	Yes
Address Register 2 (AR2)	1B	1	1	0	1	1	R/W	Yes
Baud Rate Divider Register 1 (BRDR1)	1C	1	1	1	0	0	R/W	Yes
Baud Rate Divider Register 2 (BRDR2)	1D	1	1	1	0	1	R/W	Yes
Clock Control Register (CCR)	1E	1	1	1	1	0	R/W	Yes
Error Control Register (ECR)	1F	1	1	1	1	1	R/W	Yes

*The data in the registers is not initialized, however, the FIFO pointers are reset to point to the top.
R = Read, W = Write

TABLE 2. MPCC Register Bit Assignments

HEX ADDRESS	BIT NUMBER 7	6	5	4	3	2	1	0	RESET[1] VALUE	
00	RDA	EOF	0	C/PERR	FRERR	ROVRN	RA/B	RIDLE	00	Receiver Status Register (RSR)
01	—	RDSREN	DONEEN	RSYNEN	STRSYN	2ADCMP	RABTEN	RRES	01	Receiver Control Register (RCR)
02	RECEIVED DATA (RxFIFO)								— —	Receiver Data Register (RDR)
03[3]	1	1	1	1	1	1	1	1		(null)
04	RECEIVER INTERRUPT VECTOR NUMBER (RIVN)								0F	Receiver Interrupt Vector Number Register (RIVNR)
05	RDA IE	EOF IE	—	C/PERR IE	FRERR IE	ROVRN IE	RA/B IE	—	00	Receiver Interrupt Enable Register (RIER)
06	1	1	1	1	1	1	1	1		(null)
07	1	1	1	1	1	1	1	1		(null)
08	TDRA	TFC	0	0	0	TUNRN	TFERR	0	80	Transmitter Status Register (TSR)
09	TEN	TDSREN	TICS	THW	TLAST	TSYN	TABT	TRES	01	Transmitter Control Register (TCR)
0A	TRANSMITTED DATA (TxFIFO)								— —	Transmitter Data Register (TDR)
0B[3]	1	1	1	1	1	1	1	1		(null)
0C	TRANSMITTER INTERRUPT VECTOR NUMBER (TIVN)								0F	Transmitter Interrupt Vector Number Register (TIVNR)
0D	TDRA IE	TFC IE	—	—	—	TUNRN IE	TFERR IE	—	00	Transmitter Interrupt Enable Register (TIER)
0E	1	1	1	1	1	1	1	1		(null)
0F	1	1	1	1	1	1	1	1		(null)
10	CTS	DSR	DCD	CTSLVL	DSRLVL	DCDLVL	0	0	00	Serial Interface Status Register (SISR)
11	RTSLVL	DTRLVL	—	—	—	ECHO	TEST	NRZI	00	Serial Interface Control Register (SICR)
12	(NOT USED**)									(reserved)
13	(NOT USED**)									(reserved)
14	SERIAL INTERRUPT VECTOR NUMBER (SIVN)								0F	Serial Interrupt Vector Number Register (SIVNR)
15	CTS IE	DSR IE	DCD IE	—	—	—	—	—	00	Serial Interrupt Enable Register (SIER)
16	1	1	1	1	1	1	1	1		(null)
17	1	1	1	1	1	1	1	1		(null)
18	—	—	—	—	—	—	CTLEX	ADDEX	00	Protocol Select Register 1 (PSR1)
19	WD/BYT	STOP BIT SEL		CHAR LEN SEL		PROTOCOL SEL			00	Protocol Select Register 2 (PSR2)
		SB2	SB1	CL2	CL1	PS3	PS2	PS1		
1A	BOP ADDRESS/BSC & COP PAD								00	Address Register 1 (AR1)
1B	BOP ADDRESS/BSC & COP SYN								00	Address Register 2 (AR2)
1C	BAUD RATE DIVIDER (LSH)								01	Baud Rate Divider Register 1 (BRDR1)
1D	BAUD RATE DIVIDER (MSH)								00	Baud Rate Divider Register 2 (BRDR2)
1E	—	—	—	PSCDIV	TCLKO	RCLKIN	CLK SEL		00	Clock Control Register (CCR)
							CK2	CK1		
1F	PAREN	ODDPAR	—	—	CTLCRC	CRCPRE	CRC SEL		04	Error Control Register (ECR)
							CR2	CR1		

NOTES:
1. RESET = Register contents upon power up or $\overline{\text{RESET}}$ (— — = undefined).
2. In the word mode, two bytes are addressed with each word access starting with the even address (R68561 only).
3. When address 03 or 0B is addressed in the word mode, the second byte of the RxFIFO or TxFIFO is accessed, respectively.

** Unused registers may contain random bit values.
— = Read as zero.

REGISTER DEFINITIONS

RECEIVER REGISTERS

Receiver Status Register (RSR)

7	6	5	4	3	2	1	0
RDA	EOF	0	C/PERR	FRERR	ROVRN	RA/B	RIDLE

The Receiver Status Register (RSR) contains the status of the receiver including error conditions. Status bits are cleared by writing a 1 into respective positions, by writing a 1 into the RCR RRES bit or by $\overline{\text{RESET}}$. If an EOF, C/PERR, or FRERR is set in the RSR, the data reflecting the error (the first byte or word in the RxFIFO) must be read prior to resetting the corresponding status bit in the RSR. The $\overline{\text{IRQ}}$ output is asserted if any of the conditions reported by the status bits occur and the corresponding interrupt enable bit in the RIER is set.

The RSR format is the same as the frame status format (see below) except as noted.

RSR
7 **RDA —Receiver Data Available.** (RSR only).
0 The RxFIFO is empty (i.e., no received data is available).
1 Received data is available in the RxFIFO and can be read via the RDR.

RSR
6 **EOF —End of Frame.**
0 No end of frame or block detected.
1 End of frame or block detected (BOP and BSC).

RSR
5 **RHW —Receive Half Word.** (Frame Status only).
0 The last word of the frame contains data on the upper half (D8-D15) and frame status on the lower half (D0-D7) of the data bus.
1 The lower half of the data bus (D0-D7) contains the frame status but the upper half (D8-D15) is blank or invalid.

RSR
4 **C/PERR —CRC/Parity Error.**
0 No CRC or parity error detected.
1 CRC error detected (BOP, BSC), Parity error detected (ASYNC, ISOC and COP).

RSR
3 **FRERR —Frame Error.**
0 No frame error detected.
1 Short Frame or a closing FLAG detected off boundary (BOP), Frame error (ASYNC, ISOC) or receiver overrun.

RSR
2 **ROVRN —Receiver Overrun.**
0 No receiver overrun detected.
1 Receiver overrun detected. Indicates that receiver data was attempted to be transferred into the RxFIFO when it was full, resulting in loss of received data. The data that is already in RxFIFO are not affected and may be read by the processor.

RSR
1 **RA/B —Receiver Abort/Break.**
0 Normal Operation.
1 ABORT detected after an opening flag (BOP), ENQ detected in a block of text data (BSC), or BREAK detected (ASYNC).

RSR
0 **RIDLE —Receiver Idle.** (RSR only).
0 Receiver not idle.
1 15 or more consecutive "1's" have been received and the receiver is in an inactive idle state.

Frame Status

For the BSC and BOP protocols which have defined message blocks or frames, a "frame status" byte will be loaded into the RxFIFO following the last data byte of each block. If the MPCC is in word mode and the last data byte was on an even byte boundary (i.e., there was an even number of bytes in the message), a blank byte will be loaded into the RxFIFO prior to loading the frame status byte in order to force the "frame status" byte and the next frame to be on an even boundary. In the byte mode, the status byte will always immediately follow the last data byte of the block/frame (see Figure 3). The EOF status in the RSR is then set when the byte/word containing the frame status is the next byte/word to be read from the RxFIFO.

In the receiver DMA mode, when the EOF status in the RSR is set, DONE is asserted to the DMAC. Thus the last byte accessed by the DMAC is always a status byte, which the processor may read to check the validity of entire frame.

The frame status contains all the status contained within the RSR with the exception of RDA and RIDLE. But, in addition to the RSR contents, the frame status byte has a RHW status in bit 5 which indicates either an even or odd boundary (applicable to word mode only). When RHW = 0, the last word of the frame contains data on the upper half and status on the lower half of the data bus. If RHW = 1, the lower half of the bus contains status but the upper half is a blank or invalid byte.

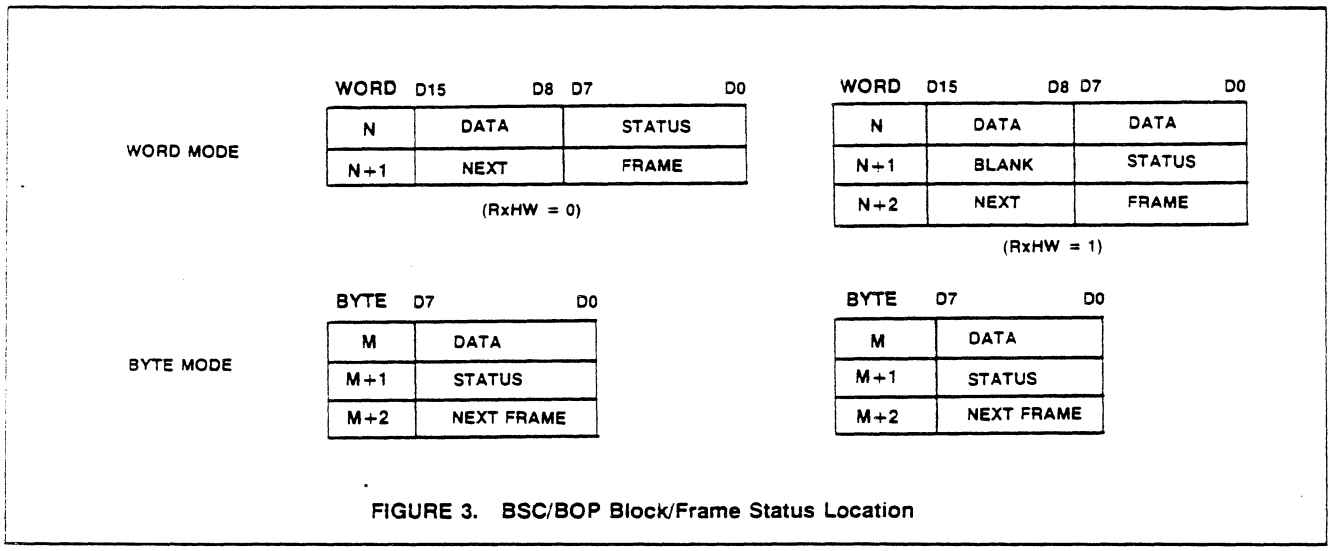


FIGURE 3. BSC/BOP Block/Frame Status Location

Receiver Control Register (RCR)

7	6	5	4	3	2	1	0
—	RDSREN	DONEEN	RSYNEN	STRSYN	2ADCMP	RABEN	RRES

The Receiver Control Register (RCR) selects receiver control options.

RCR
7 —**Not used.**

RCR
6 **RDSREN —Receiver Data Service Request Enable.**
0 Disable receiver DMA mode.
1 Enable receiver DMA mode.

RCR
5 **DONEEN —$\overline{\text{DONE}}$ Output Enable.**
0 Disable $\overline{\text{DONE}}$ output.
1 Enable $\overline{\text{DONE}}$ output. (When the receiver is in the DMA mode, i.e., RDSREN = 1).

RCR
4 **RSYNEN —RSYNEN Output Enable.** Selects the DSR signal input or the RSYN SYNC signal output on the $\overline{\text{DSR}}$ pin.
0 Input DSR on $\overline{\text{DSR}}$.
1 Output RSYN on $\overline{\text{DSR}}$.

RCR
3 **STRSYN —Strip SYN Character (COP only).**
0 Do not strip SYN character.
1 Strip SYN character.

RCR
2 **2ADCMP —One/Two Address Compare (BOP only).**
0 Compare one address byte with the contents of AR1.
1 Compare two address bytes with the contents of AR1 and AR2.

RCR
1 **RABTEN —Receiver Abort Enable (BOP only).**
0 Do not abort frame upon error detection.
1 Abort frame upon RxFIFO overrun (ROVRN bit = 1 in the RSR) or CFCRC error detection (C/PERR bit = 1 in the RSR). If either error occurs, the MPCC ignores the remainder of the current frame and searches for the beginning of the next frame.

RCR
0 **RRES —Receiver Reset Command.**
0 Enable normal receiver operation.
1 Reset receiver. Resets the receiver section including the RxFIFO and the RSR (but not the RCR). RRES is set by $\overline{\text{RESET}}$ or by writing a 1 into this bit for one write cycle and is cleared by writing a 0 into this bit. RRES requires clearing after $\overline{\text{RESET}}$.

Receiver Data Register (RDR)

7	6	5	4	3	2	1	0
MSB	Received Data (RxFIFO)						LSB

The receiver has an 8-byte (or 4-word) First In First Out (FIFO) register file (RxFIFO) where received data are stored before being transferred to the bus. The received data is transferred out of the RxFIFO via the RDR in 8-bit bytes or 16-bit words depending on the WD/BYT bit setting in PSR2. When the RxFIFO has a data byte/word ready to be transferred, the RDA status bit in the RSR is set to 1.

Receiver Interrupt Vector Number Register (RIVNR)

7	6	5	4	3	2	1	0
Receiver Interrupt Vector Number (RIVN)							

If a receiver interrupt condition occurs (as reported by status bits in the RSR that correspond to interrupt enable bits in the RIER) and the corresponding bit is set in the RIER, $\overline{\text{IRQ}}$ output is asserted to request MPU receiver interrupt service. When the $\overline{\text{IACK}}$ input is asserted from the bus, the Receiver Interrupt Vector Number (RIVN) from the Receiver Interrupt Vector Number Register (RIVNR) is placed on the data bus. The RIVN is set to $0F upon $\overline{\text{RESET}}$.

Receiver Interrupt Enable Register (RIER)

7	6	5	4	3	2	1	0
RDA IE	EOF IE	—	C/PERR IE	FRERR IE	ROVRN IE	RA/B IE	—

The Receiver Interrupt Enable Register (RIER) contains interrupt enable bits for the Receiver Status Register (RSR). When enabled, the $\overline{IRQ}$ output is asserted when the corresponding condition is detected and reported in the RSR.

RIER
7 **RDA IE —Receiver Data Available Interrupt Enable.**
0 Disable RDA Interrupt.
1 Enable RDA Interrupt.

RIER
6 **EOF IE —End of Frame Interrupt Enable.**
0 Disable EOF Interrupt.
1 Enable EOF Interrupt.

RIER
5 **—Not used.**

RIER
4 **C/PERR IE —CRC/Parity Error Interrupt Enable.**
0 Disable C/PERR Interrupt.
1 Enable C/PERR Interrupt.

RIER
3 **FRERR IE —Frame Error Interrupt Enable.**
0 Disable FRERR Interrupt.
1 Enable FRERR Interrupt.

RIER
2 **ROVRN IE —Receiver Overrun Interrupt Enable.**
0 Disable ROVRN Interrupt.
1 Enable ROVRN Interrupt

RIER
1 **RA/B IE —Receiver Abort/Break Interrupt Enable.**
0 Disable RA/B Interrupt.
1 Enable RA/B Interrupt.

RIER
0 **—Not used.**

TRANSMITTER REGISTERS

Transmitter Status Register (TSR)

7	6	5	4	3	2	1	0
TDRA	TFC	0	0	0	TUNRN	TFERR	0

The Transmitter Status Register (TSR) contains the transmitter status including error conditions. The transmitter status bits are cleared by writing a 1 into their respective positions, by writing a 1 into the TCR TRES bit, or by $\overline{RESET}$. The $\overline{IRQ}$ output is asserted if any of the conditions reported by the status bits occur and the corresponding interrupt enable bit in the TIER is set.

TSR
7 **TDRA —Transmitter Data Register Available.**
0 The TxFIFO is full.
1 The TxFIFO is not full (i.e., available) and data to transmit can be loaded via the TDR.

TSR
6 **TFC —Transmitted Frame Complete.** (BOP, BSC and COP only).
0 Frame not complete.
1 Closing FLAG or ABORT character has been transmitted (BOP), Trailing PAD has been transmitted (BSC), or the last character of a frame or block as defined by TLAST (TCR bit 3) has been transmitted (COP).

TSR
5-3 **—Not used.**

TSR
2 **TUNRN —Transmitter Underrun** (BOP, BSC and COP only). A transmitter underrun occurs when the transmitter runs out of data during a transmission. For BOP, the underrun condition is treated as an abort. For BSC and COP, SYN characters are transmitted until more data is available in the TxFIFO.
0 No transmitter underrun occurred.
1 Transmitter underrun occurred.

TSR
1 **TFERR —Transmit Frame Error** (BOP only).
0 No frame error has occurred.
1 No control field was present (short frame).

Transmitter Control Register (TCR)

7	6	5	4	3	2	1	0
TEN	TDSREN	TICS	THW	TLAST	TSYN	TABT	TRES

The Transmitter Control Register (TCR) selects transmitter control functions.

TCR
7 **TEN —Transmitter Enable.**
0 Disable transmitter. TxD output is idled. The TxFIFO may be loaded while the transmitter is disabled.
1 Enable transmitter.

TCR
6 **TDSREN —Transmitter Data Service Request Enable.**
0 Disable transmitter DMA mode.
1 Enable transmitter DMA mode.

TCR
5 **TICS —Transmitter Idle Character Select.** Selects the idle character to be transmitted when the transmitter is in an active idle mode (transmitter enabled or disabled).
0 Mark Idle (TxD output is held high).
1 Content of AR2 (BSC and COP), BREAK condition (ASYNC and ISOC), or FLAG character (BOP).

TCR
4 **THW —Transmit Half Word.** (word mode only). This bit is used when the frame or block ends on an odd boundary in conjunction with the TLAST bit and indicates that the last word in the TxFIFO contains valid data in the upper byte only. This bit must always be 0 in byte mode.
0 Transmit full word (16 bits) from the TxFIFO.
1 Transmit upper byte (8 bits) from the TxFIFO.

TCR
3 **TLAST —Transmit Last Character** (BOP, BSC and COP only).
0 The next character is not the last character in a frame or block.
1 The next character to be written into the TDR is the last character of the message. The TLAST bit automatically returns to a 0 when the associated word/byte is written to the TxFIFO. If the transmitter DMA mode is enabled, TLAST is set to a 1 by $\overline{DONE}$ from the DMAC. In this case the character written into the TDR in the current cycle is the last character.

TCR
2 **TSYN —Transmit SYN** (BSC and COP only).
0 Do not transmit SYN characters.
1 Transmit SYN characters. Causes a pair of SYN characters to be transmitted immediately following the current character. If BSC transparent mode is active, a DLE SYN sequence is transmitted. The TSYN bit automatically returns to a 0 when the SYN character is loaded into the Transmitter Shift Register.

TCR
1 **TABT —Transmit ABORT** (BOP only).
0 Enable normal transmitter operation.
1 Causes an abort by sending eight consecutive 1's. A data word/byte must be loaded into the TxFIFO after setting this bit in order to complete the command. The TABT bit clears automatically when the subsequent data word/byte is loaded into the TxFIFO.

TCR
0 **TRES —Transmitter Reset Command.**
0 Enable normal transmitter operation.
1 Reset transmitter. Clears the transmitter section including the TxFIFO and the TSR (but not the TCR). The TxD output is held in "Mark" condition. TRES is set by $\overline{RESET}$ or by writing a 1 into this bit for one write cycle and is cleared by writing a 0 into this bit. TRES requires clearing after $\overline{RESET}$.

Transmit Data Register (TDR)

7	6	5	4	3	2	1	0
MSB	TRANSMITTED DATA (TxFIFO)						LSB

The transmitter has an 8-byte (or 4-word) FIFO register file (TxFIFO). Data to be transmitted is transferred from the bus into the TxFIFO via the TDR in 8-bit bytes or 16-bit words depending on the WD/BYT bit setting in PSR2. The TDRA status bit in the TSR is set to 1 when the TxFIFO is ready to accept another data word/byte.

Transmitter Interrupt Vector Number Register (TIVNR)

7	6	5	4	3	2	1	0
Transmitter Interrupt Vector Number (TIVN)							

If a transmitter interrupt condition occurs (as reported by status bits in the TSR that correspond to interrupt enable bits in the TIER) and the corresponding bit in the TIER is set, the $\overline{IRQ}$ output is asserted to request MPU transmitter interrupt service. When the $\overline{IACK}$ input is asserted from the bus, the Transmitter Interrupt Vector Number (TIVN) from the Transmitter Interrupt Vector Number Register (TIVNR) is placed on the data bus. The TIVN is set to $0F upon $\overline{RESET}$.

Transmitter Interrupt Enable Register (TIER)

7	6	5	4	3	2	1	0
TDRA IE	TFC IE	—	—	—	TUNRN IE	TFERR IE	—

The Transmitter Interrupt Enable Register (TIER) contains interrupt enable bits for the Transmitter Status Register. When enabled, the $\overline{IRQ}$ output is asserted when the corresponding condition is detected and reported in the TSR.

TIER
7 **TDRA IE —Transmitter Data Register (TDR) Available Interrupt Enable.**
0 Disable TDRA Interrupt.
1 Enable TDRA Interrupt.

TIER
6 **TFC IE —Transmit Frame Complete (TFC) Interrupt Enable.**
0 Disable TFC Interrupt.
1 Enable TFC Interrupt.

TIER
5-3 **—Not used.**

TIER
2 **TUNRN IE—Transmitter Underrun (TUNRN) Interrupt Enable.**
0 Disable TUNRN Interrupt.
1 Enable TUNRN Interrupt.

TIER
1 **TFERR IE—Transmit Frame Error (TFERR) Interrupt Enable.**
0 Disable TFERR Interrupt.
1 Enable TFERR Interrupt.

TIER
0 **—Not used**

SERIAL INTERFACE REGISTERS

Serial Interface Status Register (SISR)

7	6	5	4	3	2	1	0
CTS	DSR	DCD	CTSLVL	DSRLVL	DCDLVL	0	0

The Serial Interface Status Register (SISR) contains the serial interface status information. The transition status bits (CTS, DSR and DCD) are cleared by writing a 1 into their respective positions, or by $\overline{\text{RESET}}$. The level status bits (CTSLVL, DSRLVL and DCDLVL) reflect the state of their respective inputs and cannot be cleared internally. The $\overline{\text{IRQ}}$ output is asserted if any of the conditions reported by the transition status bits occur and the corresponding interrupt enable bit in the SIER is set.

SISR
7 **CTS —Clear to Send Transition Status.**
1 $\overline{\text{CTS}}$ has transitioned positive (from active to inactive).
0 $\overline{\text{CTS}}$ has not transitioned positive.

SISR
6 **DSR —Data Set Ready Transition Status.**
1 $\overline{\text{DSR}}$ has transitioned negative (from inactive to active).
0 $\overline{\text{DSR}}$ has not transitioned negative.

SISR
5 **DCD —Data Carrier Detect Transition Status.**
1 $\overline{\text{DCD}}$ has transitioned positive (from active to inactive).
0 $\overline{\text{DCD}}$ has not transitioned positive.

SISR
4 **CTSLVL —Clear to Send Level.**
0 $\overline{\text{CTS}}$ input level is negated (high).
1 $\overline{\text{CTS}}$ input level is asserted (low).

SISR
3 **DSRLVL —Data Set Ready Level.**
0 $\overline{\text{DSR}}$ input level is negated (high).
1 $\overline{\text{DSR}}$ input level is asserted (low).

SISR
2 **DCDLVL —Data Carrier Detect Level.**
0 $\overline{\text{DCD}}$ input level is negated (high).
1 $\overline{\text{DCD}}$ input level is asserted (low).

SISR
1-0 **—Not used.**

Serial Interface Control Register (SICR)

7	6	5	4	3	2	1	0
RTSLVL	DTRLVL	—	—	—	ECHO	TEST	NRZI

The Serial Interface Control Register (SICR) controls various serial interface signals and test functions.

SICR
7 **RTSLVL —Request to Send Level.**
0 Negate $\overline{\text{RTS}}$ output (high).
1 Assert $\overline{\text{RTS}}$ output (low).

NOTE

In BOP, BSC, or COP, when the $\overline{\text{RTS}}$ bit is cleared in the middle of data transmission, the $\overline{\text{RTS}}$ output remains asserted until the end of the current frame or block has been transmitted. In ASYNC or ISOC, the $\overline{\text{RTS}}$ output is negated when the TxFIFO is empty. If the transmitter is idling when the $\overline{\text{RTS}}$ bit is reset, the $\overline{\text{RTS}}$ output is negated within two bit times.

SICR
6 **DTRLVL —Data Terminal Ready Level.**
0 Negate $\overline{\text{DTR}}$ output (high).
1 Assert $\overline{\text{DTR}}$ output (low).

SICR
5-3 **—Not used.** These bits are initialized to 0 by $\overline{\text{RESET}}$ and must not be set to 1.

SICR
2 **ECHO —Echo Mode Enable.**
0 Disable Echo mode (enable normal operation).
1 Enable Echo mode. Received data (RxD) and clock (RxC) are routed back through the transmitter to TxD and TxC, respectively. The contents of the TxFIFO is undisturbed. This mode may be used for remote test purposes.

SICR
1 **TEST —Self-test Enable.**
0 Disable self-test (enable normal operation).
1 Enable self-test, the transmitted data (TxD) and clock (TxC) are routed back through to the receiver through RxD and RxC, respectively ($\overline{\text{DCD}}$ and $\overline{\text{CTS}}$ are ignored). This "loop-back" self-test may be used for all protocols.

SICR
0 **NRZI —NRZI Data Format Select.** Selects the transmit and receive data format to be NRZ or NRZI.
0 Select NRZ data format. NRZ coding—high = 1 and low = 0.
1 Select NRZI data format. The serial data remains in the same state to send a binary 1 and switches to the opposite state to send a binary 0. A 1 bit delay is added to the TxD output to allow for encoding.

Serial Interrupt Vector Register (SIVR)

7	6	5	4	3	2	1	0
Serial Interrupt Vector Number (SIVN)							

If a serial interface interrupt condition occurs (as reported by status bits in the SISR that correspond to interrupt enable bits in the SIER) and the corresponding bit in the SIER is set, the $\overline{\text{IRQ}}$ output is asserted to request MPU serial interface interrupt service. When the $\overline{\text{IACK}}$ input asserted from the bus, the Serial Interrupt Vector Number (SIVN) from the Serial Interrupt Vector Number Register (SIVNR) is placed on the data bus. The SIVN is set to $0F upon $\overline{\text{RESET}}$.

Serial Interrupt Enable Register (SIER)

7	6	5	4	3	2	1	0
CTS IE	DSR IE	DCD IE	—	—	—	—	—

The Serial Interrupt Enable Register (SIER) contains interrupt enable bits for the Serial Interface Status Register. When an interrupt enable bit is set, the IRQ output is asserted when the corresponding condition occurs as reported in the SISR.

SIER
7 **CTS IE —Clear to Send (CTS) Interrupt Enable.**
0 Disable CTS Interrupt.
1 Enable CTS Interrupt.

SIER
6 **DSR IE —Data Set Ready (DSR) Interrupt Enable.**
0 Disable DSR Interrupt.
1 Enable DSR Interrupt.

SIER
5 **DCD IE —Data Carrier Detect (DCD) Interrupt Enable.**
0 Disable DCD Interrupt.
1 Enable DCD Interrupt.

SIER
4-0 **—Not used.**

GLOBAL REGISTERS

The global registers contain command information applying to different modes of operation and protocols. After changing global register data, TRES and RRES should be set then cleared prior to performing normal mode processing.

Protocol Select Register 1 (PSR1)

7	6	5	4	3	2	1	0
—	—	—	—	—	—	CTLEX	ADDEX

Protocol Select Register 1 (PSR1) selects BOP protocol related options.

PSR1
7-2 **—Not used.**

PSR1
1 **CTLEX —Control Field Extend (BOP only).**
0 Select 8-bit control field.
1 Select 16-bit control field.

PSR1
0 **ADDEX —Address Extend (BOP only).**
0 Disable address extension. All eight bits of the address byte are utilized for addressing.
1 Enable address extension. When bit 0 in the address byte is a 0 the address field is extended by one byte. An exception to the address field extension occurs when the first address byte is all 0's (null address).

Protocol Select Register 2 (PSR2)

7	6	5	4	3	2	1	0
WD/BYT	STOP BIT SEL		CHAR LEN SEL		PROTOCOL SEL		
	SB2	SB1	CL2	CL1	PS3	PS2	PS1

Protocol Select Register 2 (PSR2) selects protocols, character size, the number of stop bits, and word/byte mode.

PSR2
7 **WD/BYT —Data Bus Word/Byte Mode.**
0 Select byte mode. Selects the number of data bits to be transferred from the RxFIFO and the registers to the data bus and to be transferred from the data bus to the TxFIFO and the registers. The MPCC is initialized by $\overline{\text{RESET}}$ to the byte mode. Reset processing for operation with the 16-bit bus should select the word mode by sending $80 on the lower data bus to address $19 prior to transferring subsequent data between the MPCC and the data bus.
1 Select word mode.

PSR2
6-5 **STOP BIT SEL —Number of Stop Bits Select.** Selects the number of stop bits transmitted at the end of the data bits in ASYNC and ISOC modes.

		No. of Stop Bits	
SB2	SB1	ASYNC	ISOC
0	0	1	1
0	1	1-1/2	2
1	0	2	2

PSR2
4-3 **CHAR LEN SEL —Character Length Select.** Selects the character length except in BOP and BSC where the character length is always eight bits. Parity is not included in the character length.

CL2	CL1	Character Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

PSR2
2-0 **PROTOCOL SEL —Protocol Select.** Selects protocol and defines the protocol dependent control bits.

PS3	PS2	PS1	Protocol
0	0	0	BOP (Primary)
0	0	1	BOP (Secondary)
0	1	0	Reserved
0	1	1	COP
1	0	0	BSC EBCDIC
1	0	1	BSC ASCII
1	1	0	ASYNC
1	1	1	ISOC

Address Register 1 (AR1)

7	6	5	4	3	2	1	0
BOP ADDRESS/BSC & COP PAD							

Address Register 2 (AR2)

7	6	5	4	3	2	1	0
BOP ADDRESS/BSC & COP SYN							

The protocol selected in PSR2 (BOP, BSC and COP only) determines the function of the two 8-bit Address Registers (AR1 and AR2). As a secondary station in BOP, the contents of the address registers are used for address matching depending on the 2ADCMP selection in the RCR. In BSC and COP, AR1 and AR2 contain programmable leading PAD and programmable SYN characters, respectively.

Address Register (AR) Contents

Protocol Selected	2ADCMP	AR1	AR2
BOP (Primary)	X	X	X
BOP (Secondary)	0	Address	X
	1	Address	Address
BSC EBCDIC	X	Leading PAD	SYN
BSC ASCII	X	Leading PAD	SYN
COP	X	Leading PAD	SYN
*X = Not used			

Baud Rate Divider Register 1 (BRDR1)

7	6	5	4	3	2	1	0
BAUD RATE DIVIDER (LSH)							

Baud Rate Divider Register 2 (BRDR2)

7	6	5	4	3	2	1	0
BAUD RATE DIVIDER (MSH)							

The two 8-bit Baud Rate Divider Registers (BRDR1 and BRDR2) hold the divisor of the Baud Rate Divider circuit. BRDR1 contains the least significant half (LSH) and BRDR2 contains the most significant half (MSH). With an 8.064 MHz EXTAL input, standard bit rates can be selected using the combination of Prescaler Divider (in the CCR) and Baud Rate Divider values shown in Table 3. For isochronous or synchronous protocols, the Baud Rate Divider value must be multiplied by two for the same Prescaler Divider value.

The Baud Rate Divider (BRD) value can be computed for other crystal frequency, prescaler divider and desired baud rate values as follows:

$$BRD = \frac{\text{Crystal Frequency}}{\text{(Prescaler Divider) (Baud Rate) (K)}}$$

where:

K = 1 for isochronous or synchronous
2 for asynchronous

TABLE 3. Standard Baud Selection (8.064 MHz Crystal)

Desired Baud Rate (Bit Rate)	Prescaler Divider		Baud Rate Divider					
			Asynchronous			Isochronous and Synchronous		
				Hexadecimal Value			Hexadecimal Value	
	Decimal Value	PSCDIV (0 or 1)	Decimal Value	BRDR2 (MSH)	BRDR1 (LSH)	Decimal Value	BRDR2 (MSH)	BRDR1 (LSH)
50	3	1	26,880	69	00	53,760	D2	00
75	2	0	26,880	69	00	53,760	D2	00
110	3	1	12,218	2F	BA	24,436	5F	74
135	2	0	14,933	3A	55	29,866	74	AA
150	3	1	8,960	23	00	17,920	46	00
300	2	0	6,720	1A	40	13,440	34	80
1200	3	1	1,120	04	60	2,240	08	C0
1800	2	0	1,120	04	60	2,240	08	C0
2400	2	0	840	03	48	1,680	06	90
3600	2	0	560	02	30	1,120	04	60
4800	3	1	280	01	18	560	02	30
7200	2	0	280	01	18	560	02	30
9600	3	1	140	00	8C	280	01	18
19200	3	1	70	00	46	140	00	8C
38400	3	1	35	00	23	70	00	46

Clock Control Register (CCR)

7	6	5	4	3	2	1	0
—	—	—	PSCDIV	TCLKO	RCLKIN	CLK SEL	
						CK2	CK1

The CCR selects various clock options.

CCR
7-5 —**Not used.**

CCR
4 **PSCDIV —Prescaler Divider.** The Prescaler Divider network reduces the external/oscillator frequency to a value for use by the internal Baud Rate Generator.
0 Divide by 2.
1 Divide by 3.

CCR
3 **TCLKO —Transmitter Clock Output Select.**
0 Select TxC to be an input.
1 Select TxC to be an output.

CCR
2 **RCLKIN —Receiver Clock Internal Select** (ASYNC only).
0 Select External RxC.
1 Select Internal RxC.

CCR
1-0 **CLK DIV —External Receiver Clock Divider.** Selects the divider of the external RxC to determine the receiver data rate.

CK2	CK1	Divider
0	0	1 (ISOC)
0	1	16
1	0	32
1	1	64

Error Control Register (ECR)

7	6	5	4	3	2	1	0
PAREN	ODDPAR	—	—	CRCCTL	CRCPRE	CRCSEL	
						CR2	CR1

The Error Control Register (ECR) selects the error detection method used by the MPCC.

ECR
7 **PAREN —Parity Enable.** (ASYNC, ISOC and COP only)
0 Disable parity generation/checking.
1 Enable parity generation/checking.

ECR
6 **ODDPAR—Odd/Even Parity Select** (Effective only when PAREN=1).
0 Generate/check even parity.
1 Generate/check odd parity.

ECR
5-4 —**Not used.**

ECR
3 **CFCRC —Control Field CRC Enable.**
0 Disable control field CRC.
1 Enable control field CRC. Enables an intermediate CRC remainder to be appended after the address/control field in transmitted BOP frames and checked in received frames. The CRC generator is reset after control field CRC calculation.

ECR
2 **CRCPRE —CRC Generator Preset Select.**
0 Preset CRC Generator to 0.
1 Preset CRC Generator to 1 and transmit the 1's complement of the resulting remainder.

ECR
1-0 **CRCSEL —CRC Polynomial Select.** Selects one of the CRC polynominals.

CR2	CR1	Polynominal
0	0	$x^{16} + x^{12} + x^5 + 1$ (CCITT V.41)
0	1	$x^{16} + x^{15} + x^2 + 1$ (CRC-16)
1	0	$x^8 + 1$ (VRC/LRC)*
1	1	Not used.

*VRC: Odd-parity check is performed on each character including the LRC character.

INPUT/OUTPUT FUNCTIONS

MPU INTERFACE

Transfer of data between the MPCC and the system bus involves the following signals: Address lines A1 through A4, Data Bus D0 through D15, and control signals consisting of R/$\overline{W}$, $\overline{DTACK}$, $\overline{CS}$, $\overline{UDS}$/A0, and $\overline{LDS}$/$\overline{DS}$. When the MPCC is connected to the 16-bit 68000 bus, $\overline{UDS}$/A0 is connected to the $\overline{UDS}$ bus signal and $\overline{LDS}$/$\overline{DS}$ is connected to the $\overline{LDS}$ bus signal. When the MPCC is connected to the 8-bit 68008, $\overline{UDS}$/A0 is connected to the A0 bus signal and $\overline{LDS}$/DS is connected to the $\overline{DS}$ bus signal. Figures 9 & 10 show typical interface connections.

Read/Write Operation

The R/$\overline{W}$ input controls the direction of data flow on the data bus. $\overline{CS}$ (Chip Select) enables the MPCC for access to the internal registers and other operations. When $\overline{CS}$ is asserted the data I/O buffer acts as an output driver during a read operation, and as an input buffer during a write operation. $\overline{CS}$ must be decoded from the address bus and gated with address strobe ($\overline{AS}$).

When connected to the 16-bit 68000 bus for operation in the word mode (WD/BYT = 1 in the PSR2), address lines A1-A4 select the internal register(s) (the 8-bit control/status registers are accessed two at a time and the 16-bit data registers are accessed on even address boundaries). When the MPCC is selected ($\overline{CS}$ low) during a read (R/$\overline{W}$ high), 16 bits of register data are placed on the data bus when the data strobes ($\overline{LDS}$ and $\overline{UDS}$) are asserted. $\overline{LDS}$ strobes the lower eight data bits (D0-D7) and $\overline{UDS}$ strobes the upper eight data bits (D8-D15). The MPCC asserts Data Transfer Acknowledge ($\overline{DTACK}$) prior to placing data on the data bus. Conversely, when the MPCC is selected ($\overline{CS}$ low) during a write (R/$\overline{W}$ low), $\overline{LDS}$ and $\overline{UDS}$ strobe data from the D0-D7 and D8-D15 data bus lines into the selected register(s) and the MPCC asserts $\overline{DTACK}$. $\overline{DTACK}$ is negated when $\overline{CS}$ is negated. Figures 11 and 12 show the read and write timing relationships.

When connected to the 8-bit 68008 bus for operation in the byte mode (WD/BYT = 0 in the PSR2), address lines A0-A4 select one internal 8-bit register. When the MPCC is selected ($\overline{CS}$ low) during a read (R/$\overline{W}$ high), eight bits of register data are placed on data bus lines D0-D7 when the data strobe ($\overline{DS}$) is asserted. When the MPCC is selected ($\overline{CS}$ low) for a write (R/$\overline{W}$ low), $\overline{DS}$ strobes data from the D0-D7 data lines into the selected register.

DMA INTERFACE

The MPCC is capable of providing DMA data transfers up to 2 Mbytes per second when used with the MC68440 or MC68450 DMAC in the single address mode. Based on 4 Mb/s serial data rate and 5 bits/character, the maximum DMA required transfer rate is 800 Kbytes per second.

The MPCC has separate DMA enable bits for the transmitter and receiver, each of which occupies a DMA channel. Both the transmitter and receiver data are implicitly addressed (TDR or RDR) therefore addressing of the data register is not required before data may be transferred. Communication between the MPCC and the DMAC is accomplished by a two-signal request/acknowledge handshake. Since the MPCC has only one acknowledge input ($\overline{DACK}$) for its two DMA request lines, an external OR function must be provided to combine the two DMA acknowledge signals. The MPCC uses the R/$\overline{W}$ input to distinguish between the Transmitter Data Service Request ($\overline{TDSR}$) acknowledge and the Receiver Data Service Request ($\overline{RDSR}$) acknowledge.

Receiver DMA Mode

The receiver DMA mode is enabled when the RDSREN bit in the RCR is set to 1. When data is available in the RxFIFO, Receiver Data Service Request ($\overline{RDSR}$) is asserted for one receiver clock period to initiate the MPCC to memory DMA transfer. The next $\overline{RDSR}$ cycle may be initiated as soon as the current $\overline{RDSR}$ cycle is completed.

In response to $\overline{RDSR}$ assertion, the DMAC sets the R/$\overline{W}$ line to write, asserts the memory address, address strobe, and DMA acknowledge. The MPCC outputs data from the RxFIFO to the data bus and the DMAC asserts the data strobes. The memory latches the data and asserts $\overline{DTACK}$ to complete the data transfer. The DMAC asserts $\overline{DTC}$ to indicate to the MPCC that data transfer is complete. Figure 13 shows the timing relationships for the receiver DMA mode.

$\overline{RDSR}$ is inhibited when either RDSREN is reset to 0 or RRES is set to 1 (both in the RCR), or when $\overline{RESET}$ is asserted.

Transmitter DMA Mode

The transmitter DMA mode is enabled when the TDSREN bit in the TCR is set to 1. When the TxFIFO is available, Transmitter Data Service Request ($\overline{TDSR}$) is asserted for one transmitter clock period to initiate the memory to MPCC DMA transfer. The next $\overline{TDSR}$ cycle may be initiated as soon as the current $\overline{TDSR}$ cycle is completed.

In the transmitter DMA mode, the TxFIFO is implicitly addressed. That is, when the transfer is from memory to the TxFIFO, only the memory is addressed. In response to $\overline{TDSR}$ assertion, the DMAC sets the R/$\overline{W}$ line to read, asserts the memory address, the address strobe, the data strobes and DMA acknowledge. The memory places data on the data bus and asserts $\overline{DTACK}$. Data is valid at this time and will remain valid until the data strobes are negated. The DMAC asserts $\overline{DTC}$ to indicate to the MPCC that data is available. The MPCC now loads the data into the TxFIFO and the transfer is complete. A timing diagram for the transmitter DMA mode is shown in Figure 14.

$\overline{TDSR}$ is inhibited when either TDSREN is reset to 0 or TRES is set to 1 (both in the TCR), or when $\overline{RESET}$ is asserted.

$\overline{\text{DONE}}$

When the DMA transfer count is exhausted in transmitter DMA mode, the DMAC asserts $\overline{\text{DONE}}$ which sets the TLAST bit in the TCR to indicate that the last word/byte has been transferred. In the receiver DMA mode, $\overline{\text{DONE}}$ is asserted by the MPCC when the last character of the frame/block is being transferred from the RxFIFO to the data bus if the DONEEN bit is set to a 1 in the RCR.

INTERRUPTS

If an interrupt generating status occurs and the interrupt is enabled, the MPCC asserts the $\overline{\text{IRQ}}$ output. Upon receiving $\overline{\text{IACK}}$ for the pending interrupt request, the MPCC places an interrupt vector on D0-D7 data bus and asserts $\overline{\text{DTACK}}$.

The MPCC has three vector registers: Receiver Interrupt Vector Number Register (RIVNR), Transmitter Interrupt Vector Number Register (TIVNR), and Serial Interrupt Vector Number Register (SIVNR). The receiver interrupt has higher priority over the transmitter interrupt, and the transmitter interrupt has priority over the serial interface interrupt. For example, if a pending interrupt request has been generated simultaneously by the receiver and the transmitter, the Receiver Interrupt Vector Number (RIVN) is placed on D0-D7 when acknowledged by the MPU. Upon completion of the first interrupt request cycle (which clears the receiver interrupt), $\overline{\text{IRQ}}$ will remain low to start the transmitter interrupt cycle.

A timing diagram for the interrupt acknowledge sequence is shown in Figure 15.

DCE/MODEM INTERFACE

The following section describes the handshake/control signals provided on the MPCC for interfacing to a modem or RS-232C-type Data Communication Equipment (DCE).

$\overline{\text{RTS}}$ (Request to Send) Output

The $\overline{\text{RTS}}$ output is controlled by the RTSLVL bit in the SICR in conjunction with the state of the transmitter section. When the RTSLVL bit is set to 1, the $\overline{\text{RTS}}$ output is asserted. When the RTSLVL bit is reset to 0, the $\overline{\text{RTS}}$ output remains asserted until the TxFIFO becomes empty or the end of the message (or frame), complete with CRC code if any, has been transmitted. $\overline{\text{RTS}}$ also is negated when the RTSLVL bit is reset during transmitter idle, or when the $\overline{\text{RESET}}$ input is asserted.

$\overline{\text{CTS}}$ (Clear to Send) Input

The $\overline{\text{CTS}}$ input signal is normally generated by the DCE to indicate whether or not the data set is ready to transmit data. The $\overline{\text{CTS}}$ bit in the SISR reflects the transition status of the $\overline{\text{CTS}}$ input while the CTSLVL bit in the SISR reflects the current level. A positive transition on the $\overline{\text{CTS}}$ pin asserts $\overline{\text{IRQ}}$ if the CTS IE bit in the SIER is set. The $\overline{\text{CTS}}$ input in an inactive state disables the start of transmission.

$\overline{\text{DCD}}$ (Data Carrier Detect) Input

The $\overline{\text{DCD}}$ input signal is normally generated by the DCE and indicates that the DCE is receiving a data carrier signal suitable for demodulation. The $\overline{\text{DCD}}$ bit in the SISR reports the transition status of the $\overline{\text{DCD}}$ input while the DCDLVL bit in the SISR contains the current level. A positive transition on the $\overline{\text{DCD}}$ pin asserts the $\overline{\text{IRQ}}$ output if the DCD IE bit in the SIER is set. A negated $\overline{\text{DCD}}$ input disables the start of the receiver.

$\overline{\text{DSR}}$ (Data Set Ready) Input

The $\overline{\text{DSR}}$ input from the DCE indicates the status of the local data set. The $\overline{\text{DSR}}$ bit in the SISR contains the transition status of the $\overline{\text{DSR}}$ input while the DSRLVL bit in the SISR reports the current level. A negative transition on the $\overline{\text{DSR}}$ pin asserts the $\overline{\text{IRQ}}$ output if the DSR IE bit in the SIER is set.

When the RSYN bit in the RCR is set to 1, the frame synchronization signal (RSYN) in the receiver is output on the $\overline{\text{DSR}}$ pin. In this mode, $\overline{\text{DSR}}$ output low indicates detection of SYN in BSC or COP, or an address match in BOP.

$\overline{\text{DTR}}$ (Data Terminal Ready) Output

The $\overline{\text{DTR}}$ output is general purpose in nature and can be used to control switching of the DCE. The $\overline{\text{DTR}}$ output is controlled by the DTRLVL bit in the SICR.

TxC (Transmitter Clock) Input/Output

The transmitter clock (TxC) may be programmed to be input or an output. When the TCLKO control bit in the CCR is set to a 1, the TxC pin becomes an output and provides the DCE with a clock whose frequency is determined by the internal baud rate generator. When the TCLKO control bit is reset, TxC is an input and the transmitter shift timing must be provided externally. The TxD output changes state on the negative-going edge of the transmitter clock, i.e., the low-to-high transition of the clock signal nominally indicates the center of a serial data bit on the TxD output. In the asynchronous mode when TCLKO = 0 in the CCR, the TxC frequency must be two times the desired baud rate.

TxD (Transmitted Data) Output

The serial data transmitted from the MPCC is coded in NRZ or NRZI (zero compliment) data format as selected by the NRZI control bit in the SICR.

RxC (Receiver Clock) Input

The receiver latches data on the negative transition of the RxC, i.e., the positive transition of the external clock indicates the nominal center of each serial data bit on the RxD input.

RxD (Received Data) Input

The serial data received by the MPCC can be coded in NRZ or NRZI data format. The MPCC will decode the received data in accordance with the NRZI control bit setting in the SICR.

SERIAL COMMUNICATION MODES AND PROTOCOLS

ASYNCHRONOUS AND ISOCHRONOUS MODES

Asynchronous and isochronous data are transferred in frames. Each frame consists of a start bit, 5 to 8 data bits plus optional even or odd parity, and 1, 1½, or 2 stop bits. The data character is transmitted with the least significant bit (LSB) first. The data line is normally held high (MARK) between frames, however, a BREAK (minimum of one frame length for which the line is held low) is used for control purposes. Figure 3 illustrates the frame format supported by the MPCC.

Asynchronous Receive

In the asynchronous (ASYNC) mode, data received on RxD occurs in three phases: (1) detection of the start bit and bit synchronization, (2) character assembly and optional parity check, and (3) stop bit detection. The receiver bit stream may be synchronized by the internal baud rate generator clock or by an external clock on RxC. When RCLKIN in the CCR is set to 0, an external clock with a frequency of 16, 32, or 64 times the data rate establishes the data bit midpoint and maintains bit synchronization. The character assembly process does not start if the start bit is less than one-half bit time. Framing and parity errors are detected and buffered along with the character on which errors occurred. They are passed on to the RxFIFO and set appropriate status bits in the RSR when the character with an error reaches the last RxFIFO register where it is ready to be transferred onto the data bus via the RDR.

Isochronous Receive

In the isochronous (ISOC) mode, a 1 times clock on RxC is provided with the data on RxD and the serial data bit is latched on the falling edge of each clock pulse. The requirement for the detection of a valid start bit, or the beginning of a break, is satisfied by the detection of a high-to-low transition on the serial data input line. Error detection and status indication are the same as the asynchronous mode.

Asynchronous and Isochronous Transmit

In asynchronous and isochronous transmit modes, output data transmission on TxD begins with the start bit. This is followed by the data character which is transmitted LSB first. If parity generation is enabled, the parity bit is transmitted after the MSB of the character.

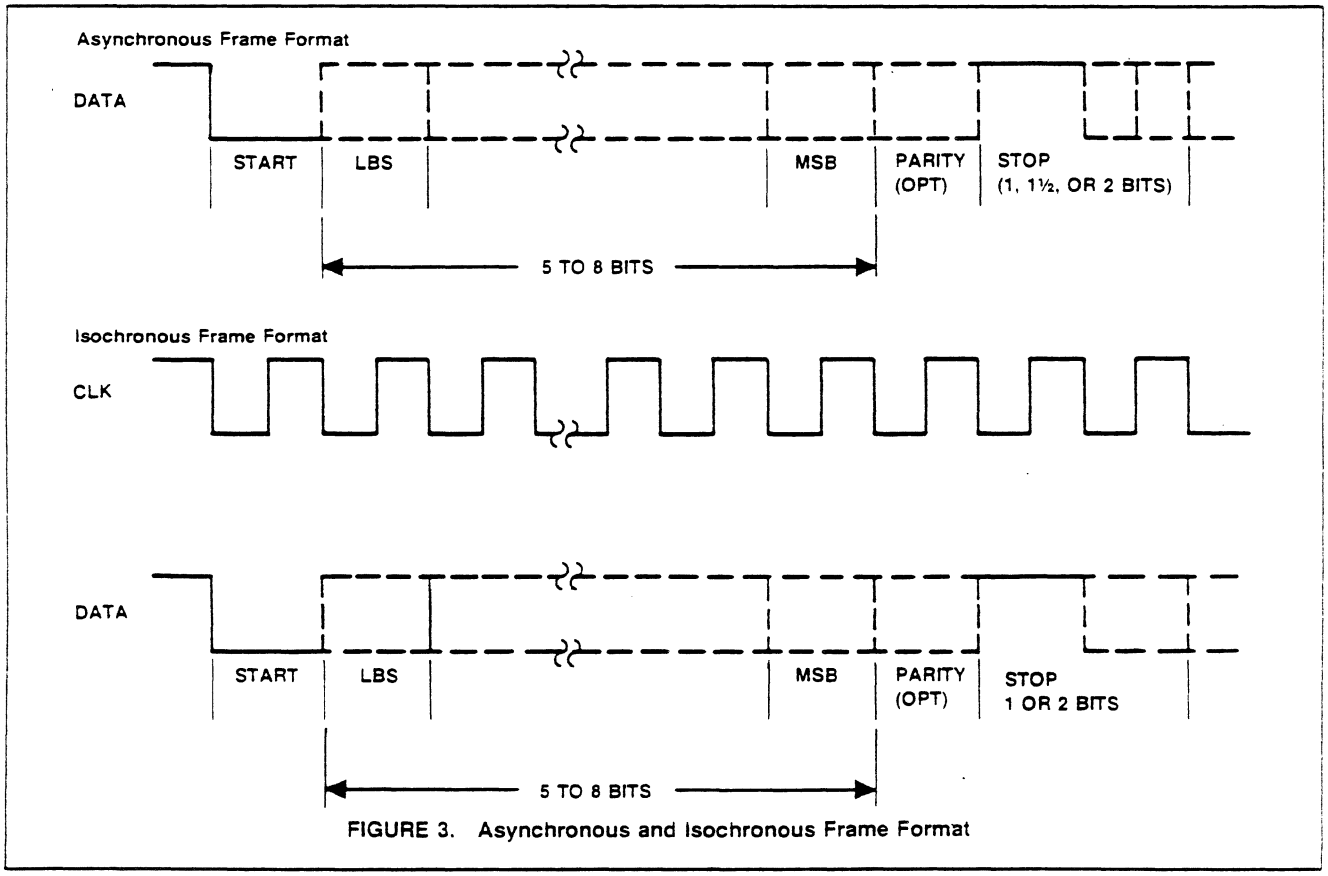


FIGURE 3. Asynchronous and Isochronous Frame Format

SYNCHRONOUS MODES

In synchronous modes, a clock is provided along with the data. Serial output data is shifted out and input data is latched on the falling edge of the clock.

BIT ORIENTED PROTOCOLS (BOP)

In bit oriented protocols (BOP), messages (data) are transmitted and received in frames. Each frame contains an opening flag, address field, control field, frame check sequence, and a closing flag. A frame may also contain an information field. (See Figure 4).

The opening flag is a special character whose bit pattern is 01111110. It marks the frame boundaries and is the interframe fill character. The address field of a frame contains the address of the secondary station which is receiving or responding to a command. The address field may be one or more bytes long. The address field can be extended by setting the ADDEX bit to a 1 in PSR1. In this case, the address field will be extended until the occurrence of an address byte with a 1 in bit 0. Up to two bytes of the address field may be automatically checked when the MPCC is programmed to be a secondary station in BOP. An automatic check for global (11111111) or null (00000000) address is also made.

The optional information field consists of 8-bit characters. Cyclic redundancy checking is used for error detection and the CRC remainder resulting from the calculation is transmitted as the frame check sequence field. For BOP, the polynomial $X^{16} - X^{12} - X^5 - 1$ (CRC-CCITT) should be used, i.e., selected in the CRC SEL bits in the ECR. The registers representing the CRC-CCITT polynomial are generally preset to all 1's and the 1's complement of the resulting remainder is transmitted. (See X.25 Recommendation).

Zero insertion/deletion is employed to prevent valid frame data from being confused with the special characters. A 0 is inserted by the transmitter after every fifth consecutive 1 in the data stream. These inserted zeros are removed by the receiver to restore the data to its original form. The inserted zeros are not included in the CRC calculation.

With the control options offered by the MPCC, commonly used bit oriented protocols such as SDLC, HDLC, ADCCP, and X.25 standards can be supported. Figure 5 compares the requirements of these options.

FLAG 01111110	ADDRESS 1 OR N BYTES	CONTROL 1 OR 2 BYTES	INFORMATION N BYTES (OPTIONAL)	FCS 2 BYTES	FLAG 01111110

FIGURE 4. Bit Oriented Protocol (BOP) Frame Format

IBM SDLC FRAME FORMAT

FLAG 01111110	ADDRESS 1 BYTE	CONTROL 1 BYTE	INFORMATION N BYTES	FCS 2 BYTES	FLAG 01111110

ADCCP/HDLC FRAME FORMAT

FLAG 01111110	ADDRESS N BYTES	CONTROL 1 OR 2 BYTES	INFORMATION N BYTES	FCS 2 BYTES	FLAG 01111110

FIGURE 5. Implemented Bit Oriented Protocols

BOP Receiver Operation

In BOP, the receiver starts assembling characters and accumulating CRC immediately after the detection of a FLAG. The receiver also continues to search for additional FLAG, or ABORT, characters on a bit-by-bit basis. Zero deletion is implemented in the Receiver Shift Register after the FLAG detection logic and before the CRC circuitry. The receiver recognizes the shared flag (the closing flag for one frame serves as the opening flag for the next frame) and the shared zero (the ending 0 of a closing flag serves as the beginning 0 of an opening flag forming the pattern "011111101111110."

Character assembly and CRC accumulation are stopped when a closing FLAG or ABORT is detected. The CRC accumulation includes all the characters between the opening FLAG and the closing FLAG. The contents of the CRC register are checked at the close of a frame and the C/PERR bit in the RSR is updated. The FCS and the FLAG are not passed on to the RxFIFO.

If the FLAG is a closing flag, a check for short frame (no control field) and CRC error conditions are made and the appropriate status is updated. When an ABORT (seven 1's) is detected, the remaining frame is discarded and the RA/B bit is set in the RSR. When a link idle (15 or more consecutive 1's) is detected, the RIDLE status bit is set in the RSR. The zeros that have been inserted to distinguish data from special characters are detected and deleted from the data stream before characters are assembled. The MPCC programmed as a secondary station provides automatic address matching of up to two bytes. If there is no address match, the receiver (secondary station) ignores the remainder of the frame by searching for the flag. If there is a match, the address bytes are transferred to the RxFIFO as they are assembled.

For the control field, one or two bytes are assembled and passed on to the RxFIFO depending on the state of the extended control field bit.

If the CTLCRC bit in the ECR is set to 1, an intermediate CRC check will be made after the address and control field. The Frame Check Sequence is still calculated over the remainder of the frame.

BOP Transmitter Operation

In BOP, the TxFIFO can be preloaded through the TDR while the transmitter is disabled (TEN = 0 in the TCR). When the transmitter is enabled (TEN = 1 in the TCR), the leading FLAG is automatically sent prior to transmitting data from the TxFIFO. The TDRA bit is set to 1 in the TSR as long as TxFIFO is not full. If an underrun occurs, the TUNRN bit in the TSR is set to a 1 and an ABORT (11111111) is transmitted followed by continuous FLAGs or marks until a new sequence is initiated.

The TLAST bit in the TCR must be set prior to loading the last character of the message to signal the transmitter to append the two-byte Frame Check Sequence (FCS) following the last character. If the transmitter DMA mode is selected (the TDSREN bit set to 1 in the TCR) the TLAST bit is set by the DONE signal from the DMAC.

A message may be terminated at any time by setting the TABT bit in the TCR to 1. This causes the transmitter to send an ABORT character followed by the remainder of the current frame data in the TxFIFO.

The serial data from the Transmitter Shift Register is continuously monitored for five consecutive 1's, and a 0 is inserted in the data stream each time this condition occurs (excluding FLAG and ABORT characters).

CRC accumulation begins with the first non-FLAG character and includes all subsequent characters. The CRC remainder is transmitted as the FCS following the last data character. If the CTLCRC bit in the ECR is set to 1, an intermediate CRC remainder is appended after the Address and Control Field. The final frame check sequence is calculated over the balance of the frame.

BISYNC (BSC)

The structure of messages utilizing the IBM Binary Synchronous Communications (BSC) protocol, commonly called Bisync, is shown in Figure 6. The MPCC can process both transparent and non-transparent messages using either the EBCDIC or the ASCII codes. The CRC-16 polynomial should be selected by setting the appropriate CRCSEL bits in the ECR for both transparent and non-transparent EBCDIC and for transparent ASCII coded messages. VRC/LRC should be selected for non-transparent ASCII coded messages. BSC messages are formatted using defined data-link control characters. Data-link control characters generated and recognized by the MPCC are listed in Table 3.

TABLE 3. BSC Data-Link Control Characters

ASCII			EBCDIC		
Command	Byte 1	Byte 2	Command	Byte 1	Byte 2
SYN	16*	—	SYN	32*	—
SOH	01	—	SOH	01	—
STX	02	—	STX	02	—
ETB	17	—	EOB (ETB)	26	—
ETX	03	—	ETX	03	—
ENQ	05	—	ENQ	2D	—
DLE	10	—	DLE	10	—
ITB	1F	—	ITB	1F	—
EOT	04	—	EOT	37	—
ACK N*	10	30-37	ACK 0	10	70
NAK	15	—	ACK 1	10	61
WACK	10	3B	NAK	3D	—
RVI	10	3C	WACK	10	6B
			RVI	10	7C

NOTE: *Programmable

A heading is a block of data starting with an SOH and containing one or more characters that are used for message control (e.g., message identification, routing, and priority). The SOH initiates the block-check-character (BCC) accumulation, but is not included in the accumulation. The heading is terminated by STX when it is part of a block containing both heading and text. A block containing only a heading is terminated with an ITB or an ETB followed by the BCC. Only the first SOH or STX in a transmission block following a line turnaround causes the BCC to reset. All succeeding STX or SOH characters are included in the BCC. This permits the entire transmission (excluding the first SOH or STX) to be block-checked.

The text data is transmitted in complete units called messages, which are initiated by STX and concluded with ETX. A message can be subdivided into smaller blocks for ease in processing and more efficient error control. Each block starts with STX and ends with ETB (except for the last block of a message, which ends with ETX). A single transmission can contain any number of blocks (ending with ETB) or messages (ending with ETX). An EOT following the last ETX block indicates a normal end of transmission. Message blocking without line turnaround can be accomplished by using ITB (see the Additional Data Link Capabilities section, IBM GA 27-3004-2).

Two modes of data transfers are used in BSC. In non-transparent mode, data link control characters may not appear as text data. In transparent mode, each control character is preceded by a data link escape (DLE) character to differentiate it from the text data. Table 4 indicates which control characters are excluded in the CRC generation. All characters not shown in the table are included in the CRC generation. Figure 7 shows various formats for Control/Response Blocks and Heading and Text Blocks.

TABLE 4. BSC Control Sequences—Inclusion in CRC Accumulation

Character of Sequence	Included in CRC Accumulation	
	Yes	No
TSYN	—	DLESYN
TSOH	—	DLESOH
TSTX*	—	DLESTX
TETB	ETB	DLE
TETX	ETX	DLE
TDLE	(DLE)DLE	DLE(DLE)

*If not preceded within the same block by transparent heading information.

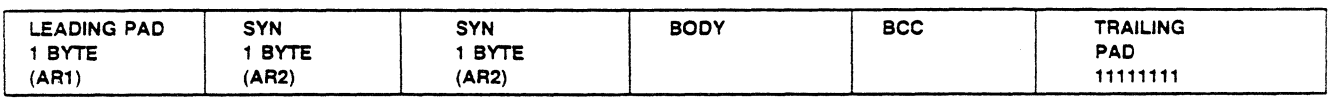


FIGURE 6. BSC Block Format

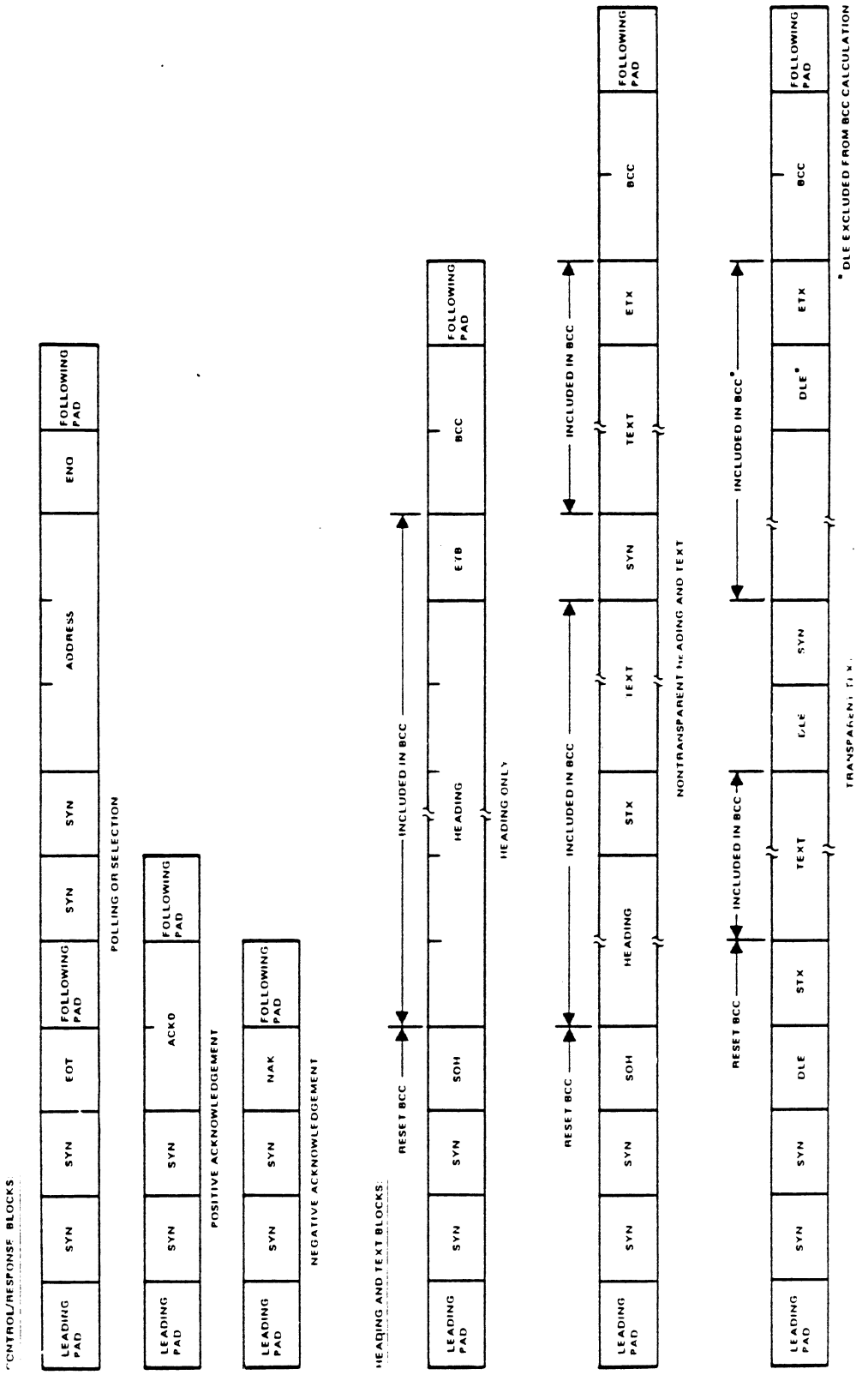


FIGURE 7. BSC Message Format Examples

BSC Receiver Operation

Character length defaults to eight bits in BSC mode. When ASCII is selected, the eighth bit is used for parity provided the VRC LRC polynomial is selected. Character assembly starts after the receipt of two consecutive SYN characters. Serial data bits are shifted through the Receiver Shift Register into the Serial-to-Parallel Register and transferred to the RxFIFO. The RDA status bit in the RSR is set to 1 each time data is transferred to the RxFIFO. The SYN character in non-transparent mode and DLE-SYN pairs in transparent mode are discarded.

The receiver starts each block in the non-transparent mode. It switches to transparent mode if a block begins with a DLE-SOH or DLE-STX pair. The receiver remains in transparent mode until a DLE-ITB, DLE-ETB, DLE-ETX or DLE-ENQ pair is received. BCC accumulation begins after an opening SOH, STX, or DLE-STX. SYN characters in non-transparent mode or DLE-SYN pairs in transparent mode are excluded from the BCC accumulation. The first DLE of a DLE-DLE sequence is not included in the BCC accumulation. The BCC is checked after receipt of an ITB, ETB, or ETX in non-transparent mode or DLE-ITB, DLE-ETB, DLE-ETX in transparent mode. If a CRC error is detected, the C/PERR and EOF bits in the RSR are set to 1. If no error is detected only the EOF bit is set. If the closing character was an ITB, BCC accumulation and character assembly starts again on the first character following the BCC.

BSC Transmitter Operation

BSC transmission begins with the sending of an opening pad (PAD) and two sync (SYN) characters. These characters are programmable and stored in AR1(PAD) and AR2(SYN). SOH or STX initiates the block-check-character (BCC) accumulation. An initial SOH or STX is not included in the BCC accumulation. Should an underrun condition occur, the content of AR2 (normally SYN character) is transmitted until new characters become available. The message is terminated by the transmission of the BCC followed by a closing pad when an ETB, ITB, or ETX is fetched from the TxFIFO. The closing PAD is generated by the MPCC.

In transparent mode, the BCC accumulation is initiated by DLE-STX and is terminated by the sequences DLE-ETX, DLE-ETB, or DLE-ITB. See Table 4 for character sequence and inclusion in CRC accumulation. If an underrun occurs, DLE-SYN characters will be transmitted until new characters are available in the TxFIFO. ETB, ETX, ITB, or ENQ with a TLAST tag is treated as a control character and the MPCC automatically inserts a DLE immediately preceding these characters. DLE-ETB, DLE-ETX, DLE-ITB, or DLE-ENQ terminates a block of transparent text, and returns the data link to normal mode. BCC generation is not used for messages beginning with characters other than SOH, STX, DLE-SOH, or DLE-STX. On all message types, if the TSYN bit is set to 1 in the TCR, a SYN-SYN (DLE-SYN sequence on transparent messages) sequence is transmitted before the next character is fetched from the TxFIFO.

CHARACTER ORIENTED PROTOCOLS

The character oriented protocol (COP) option uses the format shown in Figure 8. It may be used for various character oriented protocols with 5-8 bit character sizes and optional parity checking. The input data is checked on a bit-by-bit basis for a pair of consecutive SYN characters to establish character synchronization. These SYN characters are discarded after detection. The PAD and SYN characters may be 5-8 bits long and are user programmable as stored in AR1 and AR2, respectively.

If parity checking is enabled the characters assembled after character sync are checked for parity errors. If STRSYN is set in the RCR, all SYN characters detected within the message will be discarded and will not be passed on to the RxFIFO. If STRSYN is reset, SYNs detected within the message will be treated as data.

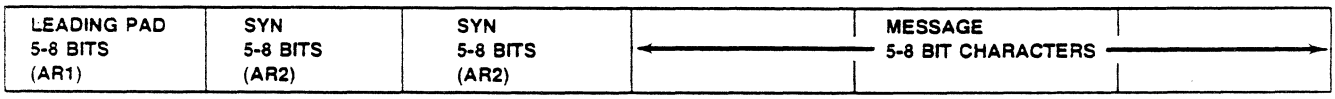


FIGURE 8. Character Oriented Protocol Format

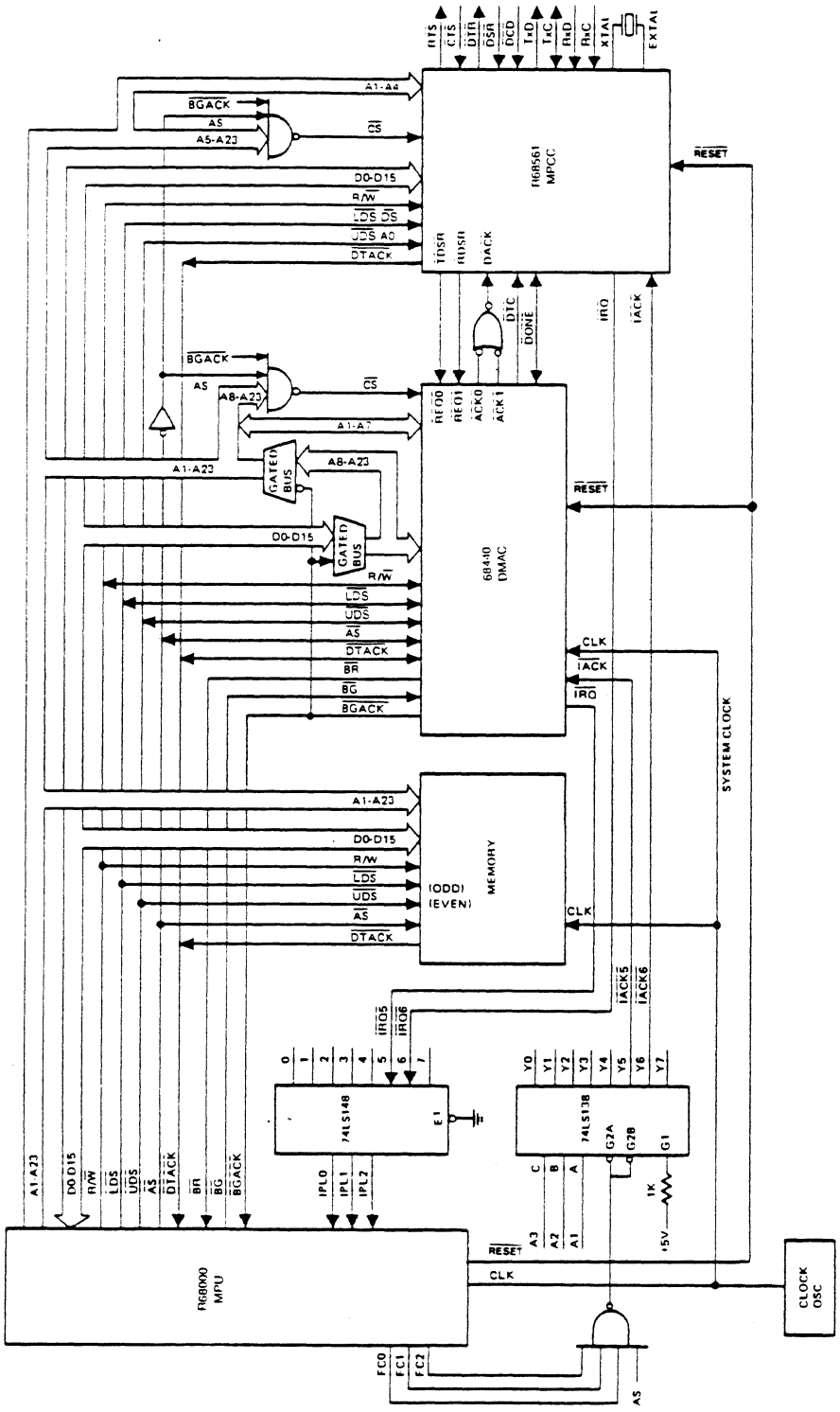


FIGURE 9. Typical Interface to 68000-Based System

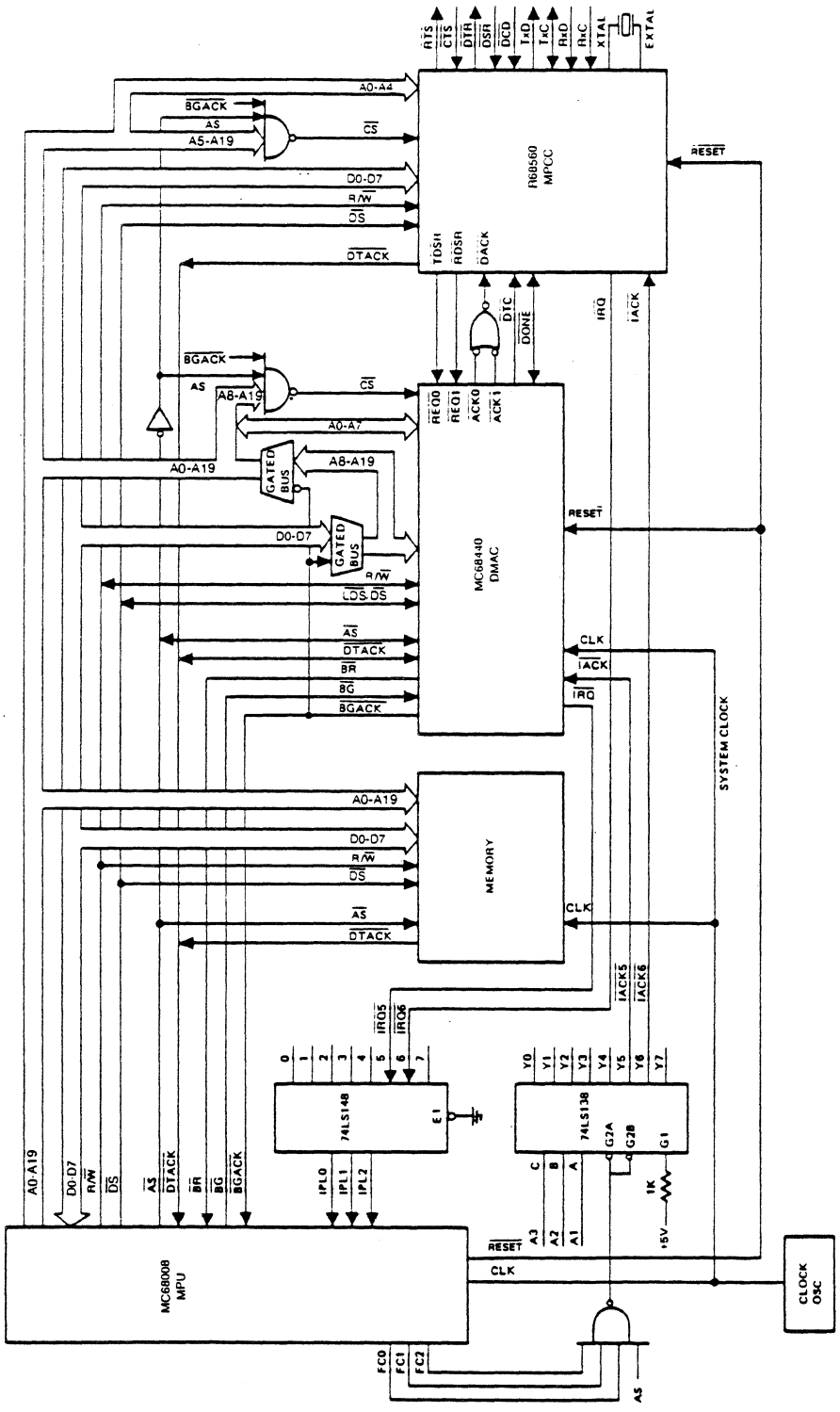
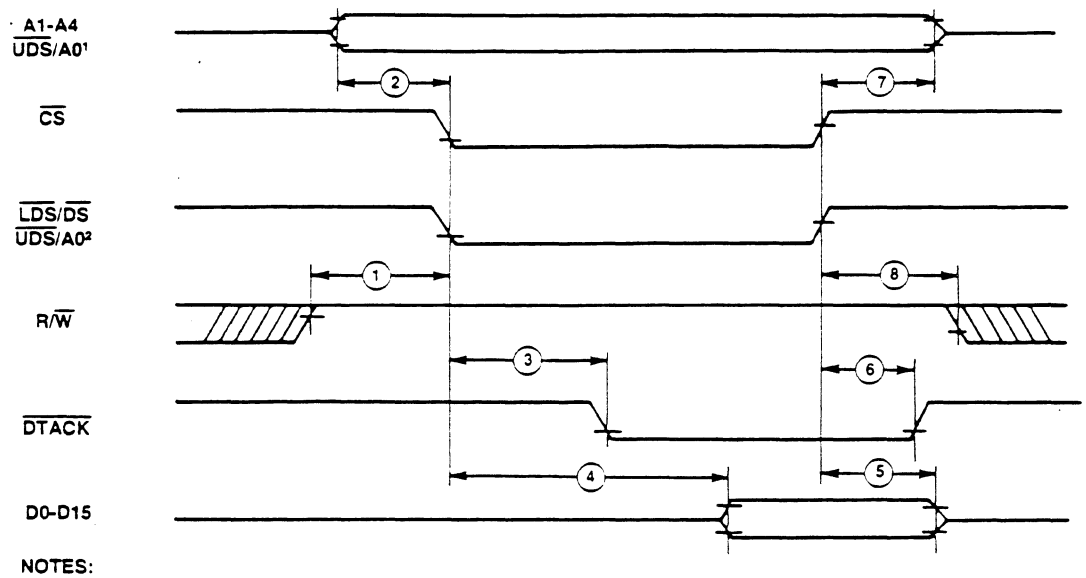
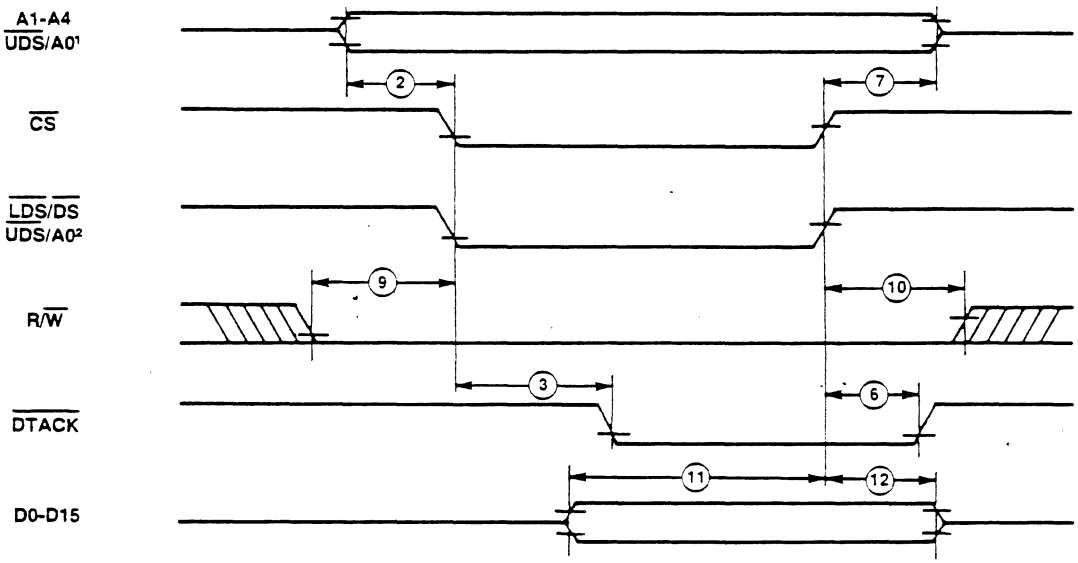


FIGURE 10. Typical Interface to 68008-Based System



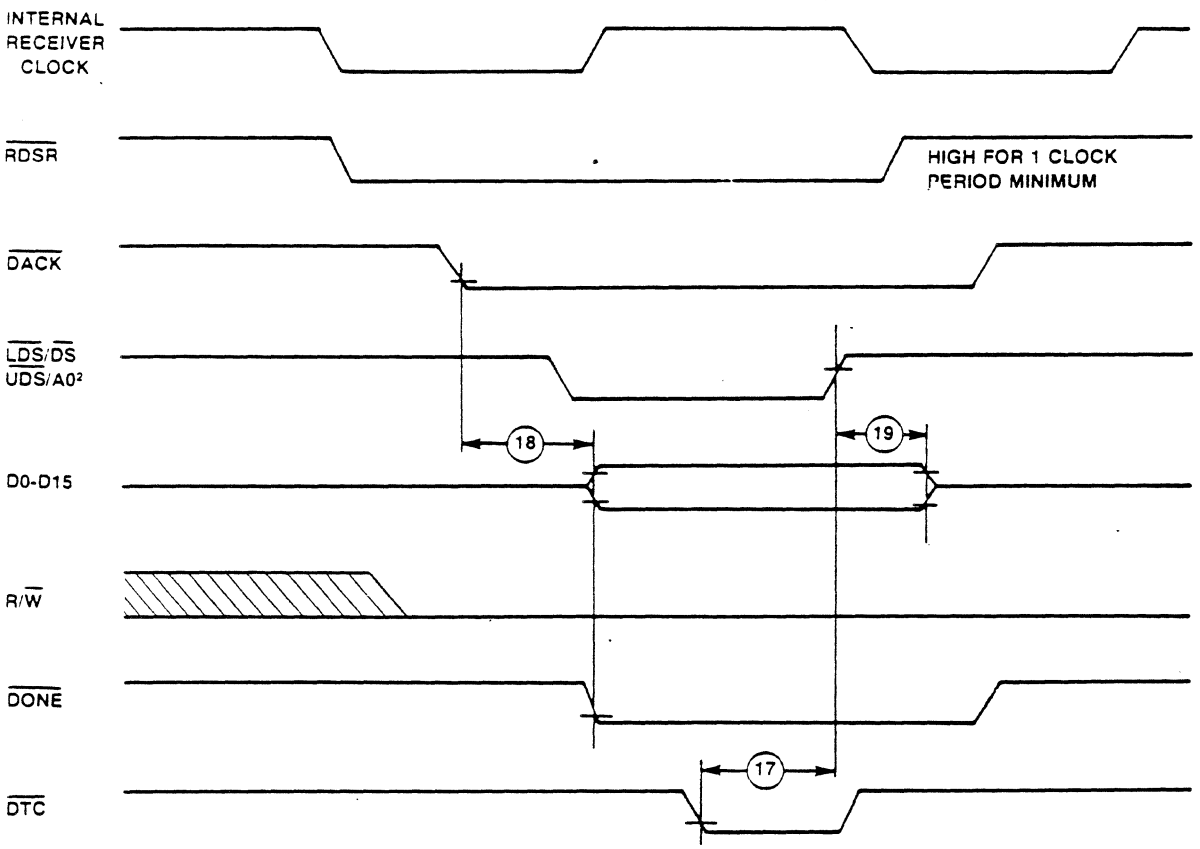
NOTES:
1. Byte mode when connected to A0 on 68008 bus.
2. Word mode when connected to UDS on 68000 bus.
3. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 11. MPCC Read Cycle Timing



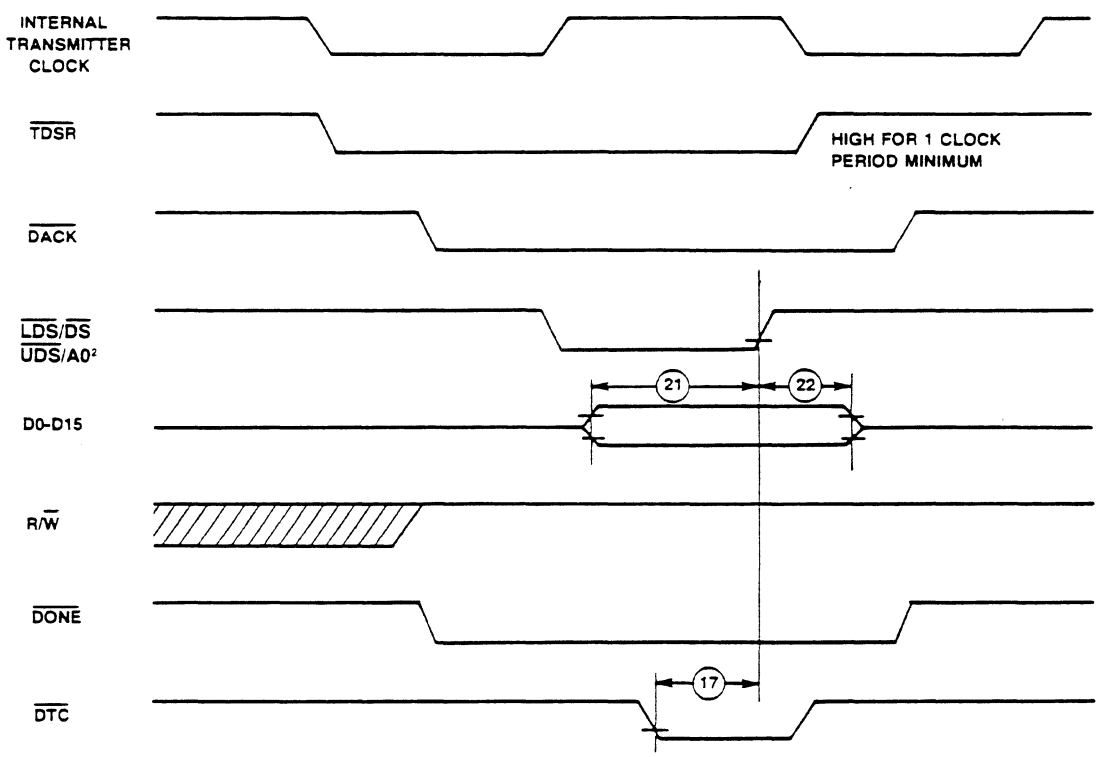
NOTES:
1. Byte mode when connected to A0 on 68008 bus.
2. Word mode when connected to UDS on 68000 bus.
3. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 12. MPCC Write Cycle Timing



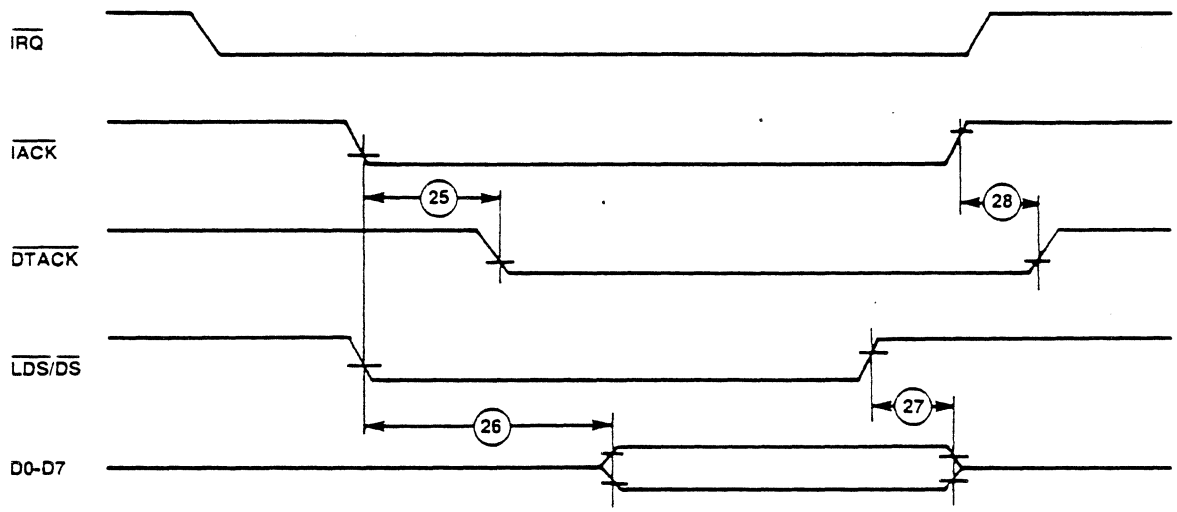
NOTES: 1. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts unless otherwise noted.
2. Word mode only.

FIGURE 13. MPCC to Memory DMA Transfer Cycle Timing (Receiver DMA Mode).



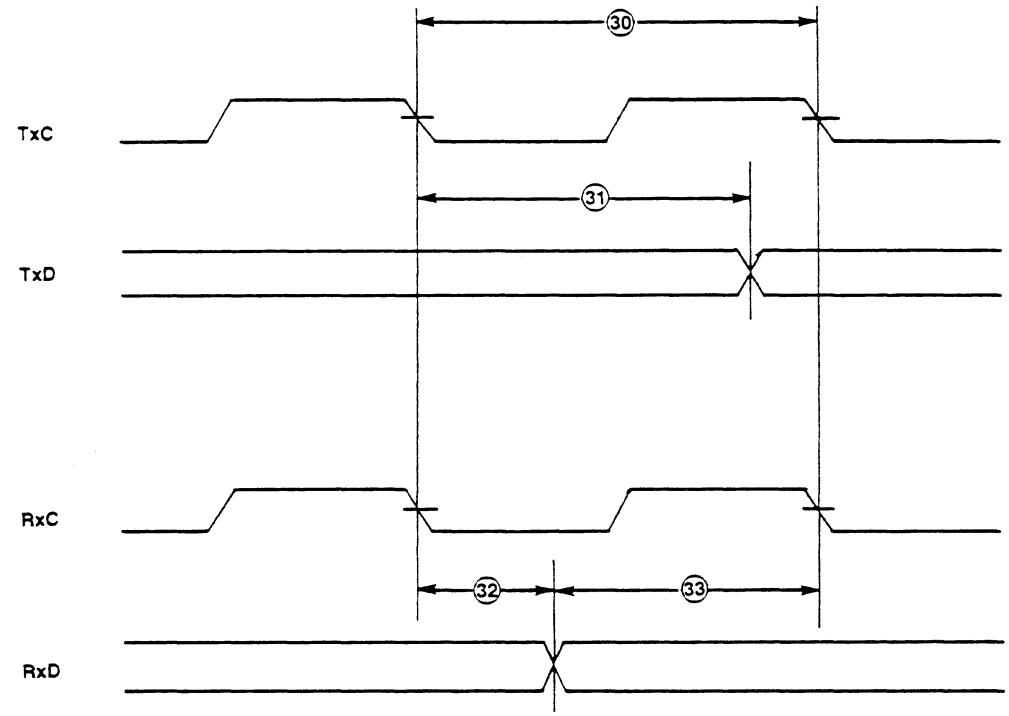
NOTES: 1. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts unless otherwise noted.
2. Word mode only.

FIGURE 14. Memory to MPCC DMA Transfer Cycle Timing (Transmitter DMA Mode).



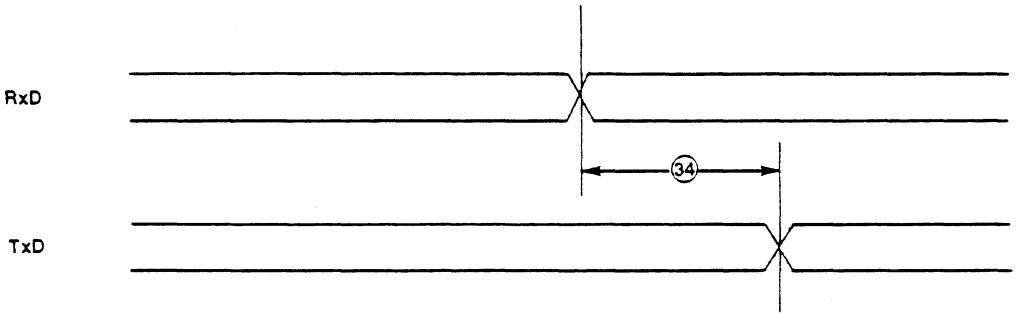
NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 15. Interrupt Request Cycle Timing



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted

FIGURE 16. Serial Interface Timing



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted

FIGURE 17. Serial Interface Echo Mode Timing

SPECIFICATIONS

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 5%, V_{SS}= 0 Vdc, T_A = 0°C to 70°C)

Number	Characteristic	Symbol	Min	Max	Unit
1	R/$\overline{W}$ High to $\overline{CS}$, $\overline{DS}$ Low	t_{RHSL}	0	—	ns
2	Address Valid to $\overline{CS}$, $\overline{DS}$ Low	t_{AVSL}	30	—	ns
3	$\overline{CS}$ Low to $\overline{DTACK}$ Low	t_{CLDAL}	0	40	ns
4	$\overline{CS}$, $\overline{DS}$ Low to Data Valid	t_{SLDV}	0	140	ns
5	$\overline{CS}$, $\overline{DS}$ High to Data Invalid	t_{SHDI}	10	150	ns
6	$\overline{CS}$, $\overline{DS}$ High to $\overline{DTACK}$ High	t_{SHDAT}	0	40	ns
7	$\overline{CS}$, $\overline{DS}$ High to Address Invalid	t_{SHAI}	20	—	ns
8	$\overline{CS}$, $\overline{DS}$ High to R/$\overline{W}$ Low	t_{SHRL}	20	—	ns
9	R/$\overline{W}$ Low to $\overline{CS}$, $\overline{DS}$ Low	t_{RLSL}	0	—	ns
10	$\overline{CS}$ High, $\overline{DS}$ High to R/$\overline{W}$ High	t_{SHRH}	20	—	ns
11	Data Valid to $\overline{CS}$, $\overline{DS}$ High	t_{DVSH}	60	—	ns
12	$\overline{CS}$, $\overline{DS}$ High to Data Invalid	t_{SHDI}	0	—	ns
17	$\overline{DTC}$ Low to $\overline{DS}$ High	t_{CLSH}	60	—	ns
18	$\overline{DACK}$ Low to Data Valid, $\overline{DONE}$ Low	t_{ALDV}	0	140	ns
19	$\overline{DS}$ High to Data Invalid	t_{SHDI}	10	150	ns
21	Data Valid to $\overline{DS}$ High	t_{DVSH}	60	—	ns
22	$\overline{DS}$ High to Data Invalid	t_{SHDI}	0	—	ns
25	$\overline{IACK}$ Low to $\overline{DTACK}$ Low	t_{IALAL}	0	40	ns
26	$\overline{IACK}$, $\overline{DS}$ Low to Data Valid	t_{IALDV}	0	140	ns
27	$\overline{DS}$ High to Data Invalid	t_{ISHDI}	10	150	ns
28	$\overline{IACK}$ High to $\overline{DTACK}$ High	t_{IAHDAT}	0	40	ns
30	RxC and TxC Period	t_{CP}	250	—	ns
31	TxC Low to TxD Delay	t_{TCLTD}	0	200	ns
32	RxC Low to RxD Transition (Hold)	t_{RCLRD}	0	—	ns
33	RxD Transition to RxC Low (Setup)	t_{RDRCL}	30	—	ns
34	RxD to TxD Delay (Echo Mode)	t_{RDTD}	—	200	ns

Note.
1. For read cycle timing, the MPCC asserts $\overline{DTACK}$ within the MPU S4 clock low setup time requirement and establishes valid data (Data In) within the MPU S6 clock low setup time requirement.

MAXIMUM RATINGS

Characteristics	Symbol	Value
Supply Voltage	V_{CC}	−0.3 to −7.0V
Input Voltage	V_{in}	−0.3 to +7.0V
Operating Temperatures	T_A	0 to 70°C
Storage Temperatures	T_{stg}	−55 to +150°C

Note:
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, normal precautions should be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Rating
Thermal Resistance	θ_{JA}		°C/W
Ceramic		50	
Plastic		68	

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C unless otherwise noted)

Characteristics		Symbol	Min	Max	Unit
Input High Voltage	All Inputs	V_{IH}	V_{SS} + 2.0	V_{CC}	V
Input Low Voltage	All Inputs	V_{IL}	V_{SS} − 0.3	V_{SS} + 0.8	V
Input Leakage Current (V_{in} = 0 to 5.25V)	R/$\overline{W}$, $\overline{RESET}$, $\overline{CS}$	I_{in}	—	10.0	μA
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4)	$\overline{IRQ}$, $\overline{DTACK}$, D0-D15	I_{TSI}	—	10.0	μA
Output High Voltage (I_{LOAD} = −400 μA, C_{LOAD} = 130 pf, V_{CC} = min) (I_{LOAD} = 0, C_{LOAD} = 30 pf, V_{CC} = min)	$\overline{RDSR}$, $\overline{TDSR}$, $\overline{IRQ}$, $\overline{DTACK}$, D0-D15 $\overline{DTR}$, $\overline{RTS}$, TxD, TxC BCLK	V_{OH}	V_{SS} + 2.4	—	V
Output Low Voltage (I_{LOAD} = 3.2 mA, V_{CC} = min) (I_{LOAD} = 8.8 mA, V_{CC} = min)	$\overline{RDSR}$, $\overline{TDSR}$, $\overline{IRQ}$, $\overline{DTACK}$, D0-D15 $\overline{DTR}$, $\overline{RTS}$, $\overline{TxD}$, $\overline{TxC}$, $\overline{BCLK}$ $\overline{DONE}$	V_{OL}	—	0.5	V
Internal Power Dissipation (Measured at T_A = 25°C)		P_{INT}	—	1	W
Input Capacitance (V_{in} = 0, T_A = 25°C, f = 1 MHz)		C_{in}	—	13	pF

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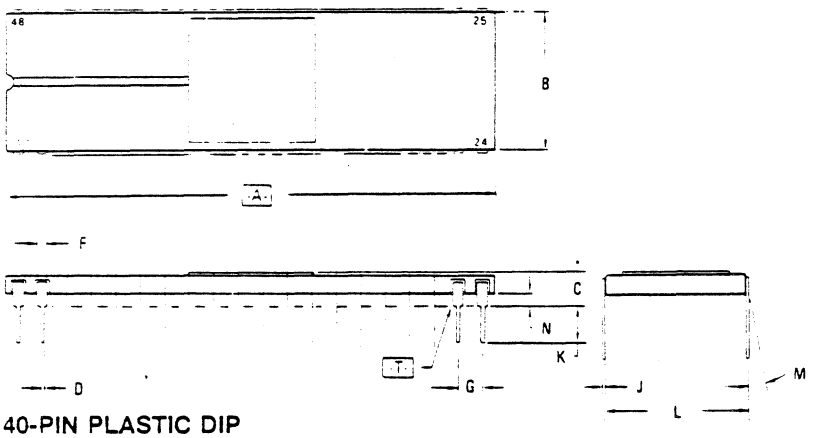
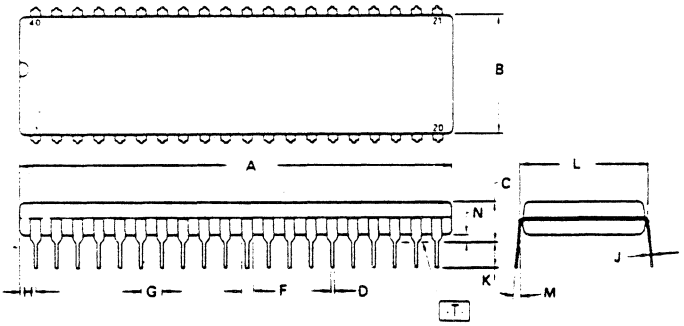
PACKAGE DIMENSIONS

48-PIN CERAMIC DIP



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	60.35	61.57	2.376	2.424
B	14.63	15.04	0.576	0.604
C	3.05	4.32	0.120	0.160
D	0.381	0.533	0.015	0.021
F	0.762	1.397	0.030	0.055
G	2.54 BSC		0.100 BSC	
J	0.203	0.330	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.99	15.65	0.590	0.616
M	0°	10°	0°	10°
N	1.016	1.524	0.040	0.606

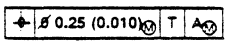
40-PIN PLASTIC DIP



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040

NOTES:

1. **DIMENSION -A- IS DATUM.**
2. **POSTIONAL TOLERANCE FOR LEADS:**



3. **-T- IS SEATING PLANE.**
4. **DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.**
5. **DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.**

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National Semiconductor

April 1982

MM58167A Microprocessor Real Time Clock

General Description

The MM58167A is a low threshold metal gate CMOS circuit that functions as a real time clock in bus oriented microprocessor systems. The device includes an addressable real time counter, 56 bits of RAM, and two interrupt outputs. A $\overline{\text{POWER DOWN}}$ input allows the chip to be disabled from the rest of the system for standby low power operation. The time base is a 32.768 Hz crystal oscillator.

Features

- Microprocessor compatible (8-bit data bus)
- 1/10,000 of a second through month counters
- 56 bits of RAM with comparator to compare the real time counter to the RAM data
- 2 INTERRUPT OUTPUTS with 8 possible interrupt signals
- $\overline{\text{POWER DOWN}}$ input that disables all inputs and outputs except for one of the interrupts
- Status bit to indicate rollover during a read
- 32.768 Hz crystal oscillator
- Four-year calendar (no leap year)
- 24-hour clock

Functional Description

Real Time Counter

The real time counter is divided into 4-bit digits with 2 digits being accessed during any read or write cycle. Each digit represents a BCD number and is defined in Table I. Any unused bits are held at a logical zero during a read and ignored during a write. An unused bit is any bit not necessary to provide a full BCD number. For example tens of hours cannot legally exceed the number 2, thus only 2 bits are necessary to define the tens of hours. The other 2 bits in the tens of hours digit are unused. The unused bits are designated in Table I as dashes.

The addressable portion of the counter is from 1/10,000 of a second to months. The counter itself is a ripple counter. The ripple delay is less than 60 μs above 4.0V and 300 μs at 2.0V.

RAM

56 bits of RAM are contained on-chip. These can be used for any necessary power down storage or as an alarm latch for comparison to the real time counter. The data in the RAM can be compared to the real time counter on a digit basis. The only digits that are not compared are the unit ten thousandths of seconds and tens of days of the week (these are unused in the real time counter). If the two most significant bits of any RAM digit are ones, then this RAM location will always compare.

The RAM is formatted the same as the real time counter, 4 bits per digit, 14 digits, however there are no unused bits. The unused bits in the real time counter will compare only to zeros in the RAM.

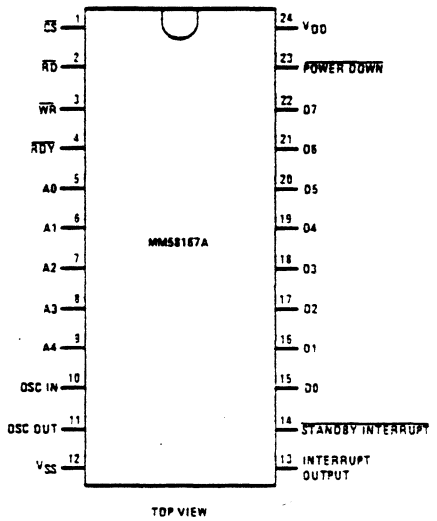
Interrupts and Comparator

There are two interrupt outputs. The first and most flexible is the INTERRUPT OUTPUT (a true high signal). This output can be programmed to provide 8 different output signals. They are: 10 Hz, 1 Hz, once per minute, once per hour, once a day, once a week, once a month, and when a RAM/real time counter comparison occurs. To enable the output a one is written into the interrupt control register at the bit location corresponding to the desired output frequency *(Figure 1)*. Once one or more bits have been set in the interrupt control register, the corresponding counter's rollover to its reset state will clock the interrupt status register and cause the interrupt output to go high. To reset the interrupt and to identify which frequency caused the interrupt, the interrupt status register is read. Reading this register places the contents of the status register on the data bus. The interrupting frequency will be identified by a one in the respective bit position. Removing the read will reset the interrupt.

The second interrupt is the $\overline{\text{STANDBY INTERRUPT}}$ (open drain output, active low). This interrupt occurs when enabled and when a RAM/real time counter comparison occurs. The $\overline{\text{STANDBY INTERRUPT}}$ is enabled by writing a one on the D0 line at address 16_H or disabled by writing a zero on the D0 line. This interrupt is not triggered by the edge of the compare signal, but rather by the level. Thus if the compare is enabled when the $\overline{\text{STANDBY INTERRUPT}}$ is enabled, the interrupt will turn on immediately.

Connection Diagram

Dual-In-Line Package



TOP VIEW

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Absolute Maximum Ratings

Voltage at All Pins	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature	− 40°C to 85°C
Storage Temperature	− 65°C to 150°C
V_{DD}−V_{SS}	6.0V
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics V_{SS} = 0V, − 40°C ≤ T_A ≤ 85°C

Parameter	Conditions	Min	Max	Units
Supply Voltage				
V_{DD}	Outputs Enabled	4.0	5.5	V
V_{DD}	$\overline{\text{POWER DOWN}}$ Mode	2.0	5.5	V
Supply Current				
I_{DD}, Static	Outputs TRI-STATE®			
	f_{IN} = DC, V_{DD} = 5.5V		10	μA
I_{DD}, Dynamic	Outputs TRI-STATE			
	f_{IN} = 32 kHz, V_{DD} = 5.5V			
	$V_{IH} \geq V_{DD} - 0.3V$			
	$V_{IL} \leq V_{SS} + 0.3V$		20	μA
I_{DD}, Dynamic	Outputs TRI-STATE			
	f_{IN} = 32 kHz, V_{DD} = 5.5V			
	V_{IH} = 2.0V, V_{IL} = 0.8V		5	mA
Input Voltage				
Logical Low		0.0	0.8	V
Logical High		2.0	V_{DD}	V
Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{DD}$	− 1	1	μA
Output Impedance	I/O and INTERRUPT OUT			
Logical Low	V_{DD} = 4.5V, I_{OL} = 1.6 mA		0.4	V
Logical High	V_{DD} = 4.5V, I_{OH} = − 400 μA	2.4		V
	I_{OH} = − 10 μA	0.8 V_{DD}		V
TRI-STATE	$V_{SS} \leq V_{OUT} \leq V_{DD}$	− 1	1	μA
Output Impedance	$\overline{\text{RDY}}$ and $\overline{\text{STANDBY}}$ $\overline{\text{INTERRUPT}}$			
Logical Low, Sink	V_{DD} = 4.5V, I_{OL} = 1.6 mA		0.4	V
Logical High, Leakage	$V_{OUT} \leq V_{DD}$		10	μA

Functional Description (Continued)

TABLE I. REAL TIME COUNTER FORMAT

Counter Addressed		Units D0	D1	D2	D3	Max BCD Code	Tens D4	D5	D6	D7	Max BCD Code
1/10,000 of Seconds	(00_H)	-	-	-	-	0	D4	D5	D6	D7	9
Hundredths and Tenths Sec	(01_H)	D0	D1	D2	D3	9	D4	D5	D6	D7	9
Seconds	(02_H)	D0	D1	D2	D3	9	D4	D5	D6	-	5
Minutes	(03_H)	D0	D1	D2	D3	9	D4	D5	D6	-	5
Hours	(04_H)	D0	D1	D2	D3	9	D4	D5	-	-	2
Day of the Week	(05_H)	D0	D1	D2	-	7	-	-	-	-	0
Day of the Month	(06_H)	D0	D1	D2	D3	9	D4	D5	-	-	3
Month	(07_H)	D0	D1	D2	D3	9	D4	-	-	-	1

(-) indicates unused bits

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Functional Description (Continued)

TABLE II. ADDRESS CODES AND FUNCTIONS

A4	A3	A2	A1	A0	Function
0	0	0	0	0	Counter—Ten Thousandths of Seconds
0	0	0	0	1	Counter—Hundredths and Tenths of Seconds
0	0	0	1	0	Counter—Seconds
0	0	0	1	1	Counter—Minutes
0	0	1	0	0	Counter—Hours
0	0	1	0	1	Counter—Day of Week
0	0	1	1	0	Counter—Day of Month
0	0	1	1	1	Counter—Month
0	1	0	0	0	RAM—Ten Thousandths of Seconds
0	1	0	0	1	RAM—Hundredths and Tenths of Seconds
0	1	0	1	0	RAM—Seconds
0	1	0	1	1	RAM—Minutes
0	1	1	0	0	RAM—Hours
0	1	1	0	1	RAM—Day of Week
0	1	1	1	0	RAM—Day of Month
0	1	1	1	1	RAM—Months
1	0	0	0	0	Interrupt Status Register
1	0	0	0	1	Interrupt Control Register
1	0	0	1	0	Counters Reset
1	0	0	1	1	RAM Reset
1	0	1	0	0	Status Bit
1	0	1	0	1	GO Command
1	0	1	1	0	$\overline{\text{STANDBY}}$ $\overline{\text{INTERRUPT}}$
1	1	1	1	1	Test Mode

All others unused

Functional Description (Continued)

The comparator is a cascaded exclusive NOR. Its output is latched 61 μs after the rising edge of the 1 kHz clock signal (input to the ten thousandths of seconds counter). This allows the counter to ripple through before looking at the comparator. For operation at less than 4.0V, the thousandths of seconds counter should not be included in a compare because of the possibility of having a ripple delay greater than 61 μs. (For output timing see Interrupt Timing.)

Power Down Mode

The $\overline{\text{POWER DOWN}}$ input is essentially a second chip select. It disables all inputs and outputs except for the $\overline{\text{STANDBY INTERRUPT}}$. When this input is at a logical zero, the device will not respond to any external signals. It will, however, maintain timekeeping and turn on the $\overline{\text{STANDBY INTERRUPT}}$ if programmed to do so. (The programming must be done before the $\overline{\text{POWER DOWN}}$ input goes to a logical zero.) When switching V_{DD} to the standby or power down mode, the $\overline{\text{POWER DOWN}}$ input should go to a logical zero at least 1 μs before V_{DD} is switched. When switching V_{DD} all other inputs must remain between $V_{SS} - 0.3V$ and $V_{DD} + 0.3V$. When restoring V_{DD} to the normal operating mode, it is necessary to insure that all other inputs are at valid levels before switching the $\overline{\text{POWER DOWN}}$ input back to a logical one. These precautions are necessary to insure that no data is lost or altered when changing to or from the power down mode.

Counter and RAM Resets; GO Command

The counters and RAM can be reset by writing all 1's (FF) at address 12_H or 13_H respectively.

A write pulse at address 15_H will reset the thousandths, hundredths, tenths, units, and tens of seconds counters. This GO command is used for precise starting of the clock. The data on the data bus is ignored during the write. If the seconds counter is at a value greater than 40 when the GO is issued, the minute counter will increment; otherwise the minute counter is unaffected. This command is not necessary to start the clock, but merely a convenient way to start precisely at a given minute. (See Table III for reset format.)

Status Bit

The status bit is provided to inform the user that the clock is in the process of rolling over when a counter is read. The 1 kHz clock into the thousandths of seconds counter has a pulse width of 61 μs. If a read of the real time counter (any digits) is done during this 61 μs period the status bit will be set. This tells the user that the clock is rippling through the real time counter. Because the clock is rippling, invalid data may be read from the counter. If the status bit is set following a counter read, the counter should be reread.

The status bit appears on D0 when address 14_H is read. All the other data lines will be zero. The bit is set when a logical one appears. This bit should be read every time a counter read or series of counter reads are done. The trailing edge of the read at address 14_H will reset the status bit.

Oscillator

The oscillator used is the standard Pierce oscillator. Externally only 2 capacitors and the crystal are required. For micropower crystals a resistor in series with the oscillator output may be necessary to insure the crystal is not overdriven. This resistor should be approximately 200 kΩ. The capacitor values should be typically 20 pF-25 pF. The crystal frequency is 32.768 Hz.

The oscillator input can be externally driven, if desired. In this case the output should be left floating and the input levels should be within 0.3V of the supplies.

A ground line or ground plane between pins 9 and 10 may be necessary to prevent interference of the oscillator by the A4 address.

Control Lines

The $\overline{\text{READ}}$, $\overline{\text{WRITE}}$, and $\overline{\text{CHIP SELECT}}$ signals are active low inputs. The $\overline{\text{READY}}$ signal is an open drain output. At the start of each read or write cycle the $\overline{\text{READY}}$ line (open drain) will pull low and will remain low until valid data from a chip read appears on the bus or data on the bus is latched in during a write. $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$ must be accompanied by a $\overline{\text{CHIP SELECT}}$ (see *Figures 3 and 4* for read and write cycle timing).

Test Mode

The test mode is merely a mode for production testing. It allows the counters to count at a higher than normal rate. In this mode the 32 kHz oscillator input is connected directly to the ten thousandths of seconds counter. The chip select and write lines must be low and the address must be held at $1F_H$.

Functional Description (Continued)

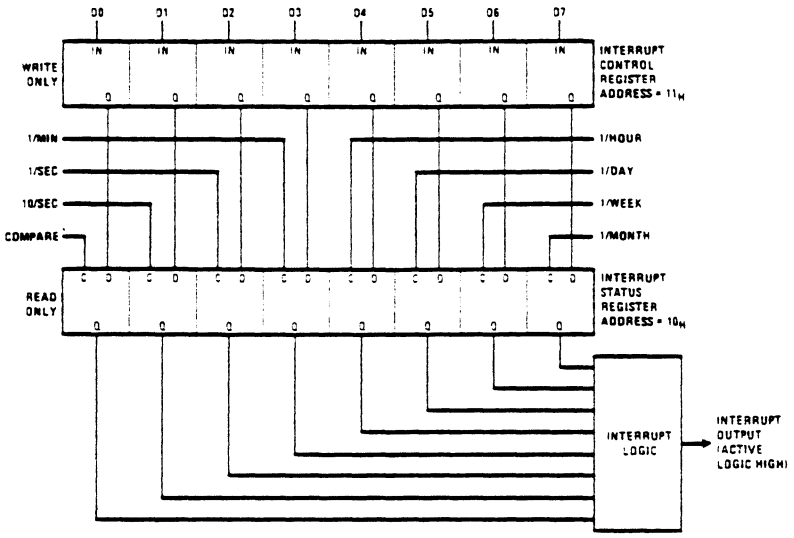


FIGURE 1. Interrupt Register Format

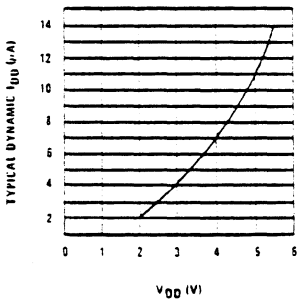


FIGURE 2. Typical Supply Current vs Supply Voltage

Interrupt Timing $-40°C \le T_A \le 85°C$, $4.5V \le V_{DD} \le 5.5V$, $V_{SS} = 0V$

	Parameter	Min	Max	Units
t_{INTON}	Status Register Clock to INTERRUPT OUTPUT (Pin 13) High (Note 1)		5	μS
t_{SBYON}	Compare Valid to $\overline{\text{STANDBY INTERRUPT}}$ (Pin 14) Low (Note 1)		5	μS
t_{INTOFF}	Trailing Edge of Status Register Read to INTERRUPT OUTPUT Low		5	μS
t_{SBYOFF}	Trailing Edge of Write Cycle (D0 = 0; Address = 16_H) to $\overline{\text{STANDBY INTERRUPT}}$ Off (High Impedance State)		5	μS

Note 1: The status register clocks are: the corresponding counter's rollover to its reset state or the compare becoming valid. The compare becomes valid 61 μs after the 1/10,000 of a second counter is clocked, if the real time counter data matches the RAM data.

Read Cycle Timing $-40°C \le T_A \le 85°C$, $4.5V \le V_{DD} \le 5.5V$, $V_{SS} = 0V$

	Parameter	Min	Max	Units
t_{AR}	Address Bus Valid to Read Strobe	100		ns
t_{CSR}	Chip Select to Read Strobe	0		ns
t_{RRY}	Read Strobe to Ready Strobe		150	ns
t_{RYD}	Ready Strobe to Data Valid		800	ns
t_{AD}	Address Bus Valid to Data Valid		1050	ns
t_{RH}	Data Hold Time From Trailing Edge of Read Strobe	0		ns
t_{HZ}	Trailing Edge of Read Strobe to TRI-STATE Mode		250	ns
t_{RYH}	Read Hold Time after Ready Strobe	0		ns
t_{RA}	Address Bus Hold Time from Trailing Edge of Read Strobe	50		ns

Note 2: If $t_{AR} = 0$ or $t_{DW} = 0$ and Chip Select, Address Valid, Read or Write are coincident then they must exist for 1050 ns.

Write Cycle Timing $-40°C \le T_A \le 85°C$, $4.5V \le V_{DD} \le 5.5V$, $V_{SS} = 0V$

	Parameter	Min	Max	Units
t_{AW}	Address Valid to Write Strobe	100		ns
t_{CSW}	Chip Select to Write Strobe	0		ns
t_{DW}	Data Valid before Write Strobe	100		ns
t_{WRY}	Write Strobe to Ready Strobe		150	ns
t_{RY}	Ready Strobe Width		800	ns
t_{RYH}	Write Hold Time after Ready Strobe	0		ns
t_{WD}	Data Hold Time after Write Strobe	110		ns
t_{WA}	Address Hold Time after Write Strobe	50		ns

Data bus loading is 100 pF.
Ready output loading is 50 pF and 20 kΩ pull-up.
Input and output AC timing levels:
Logical one = 2.0V
Logical zero = 0.8V

Read and Write Cycle Timing Diagrams

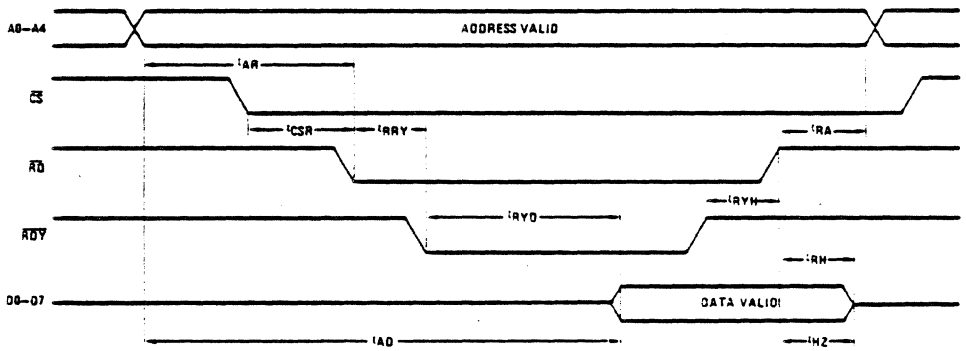


FIGURE 3. Read Cycle Timing

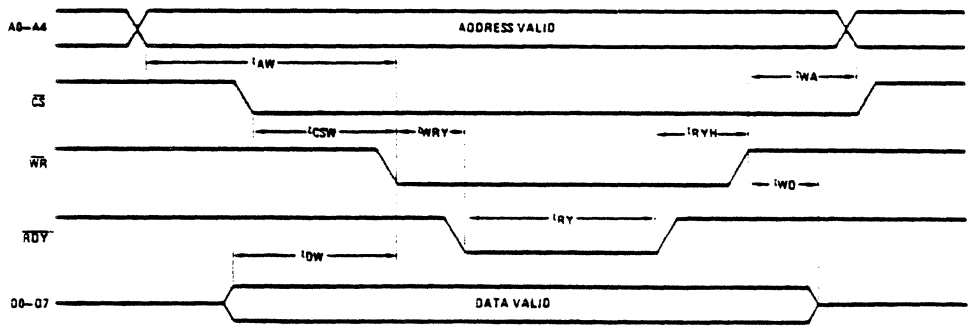
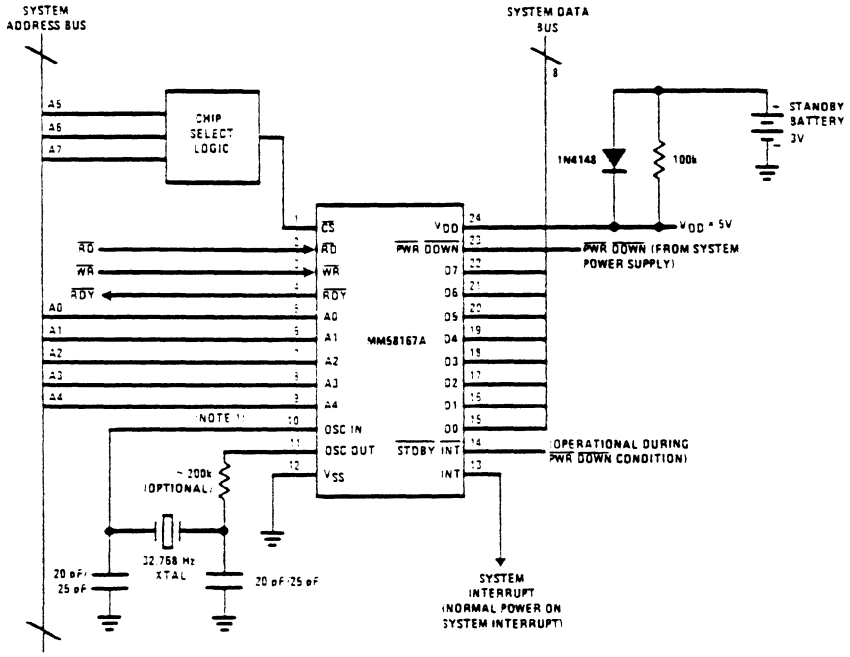


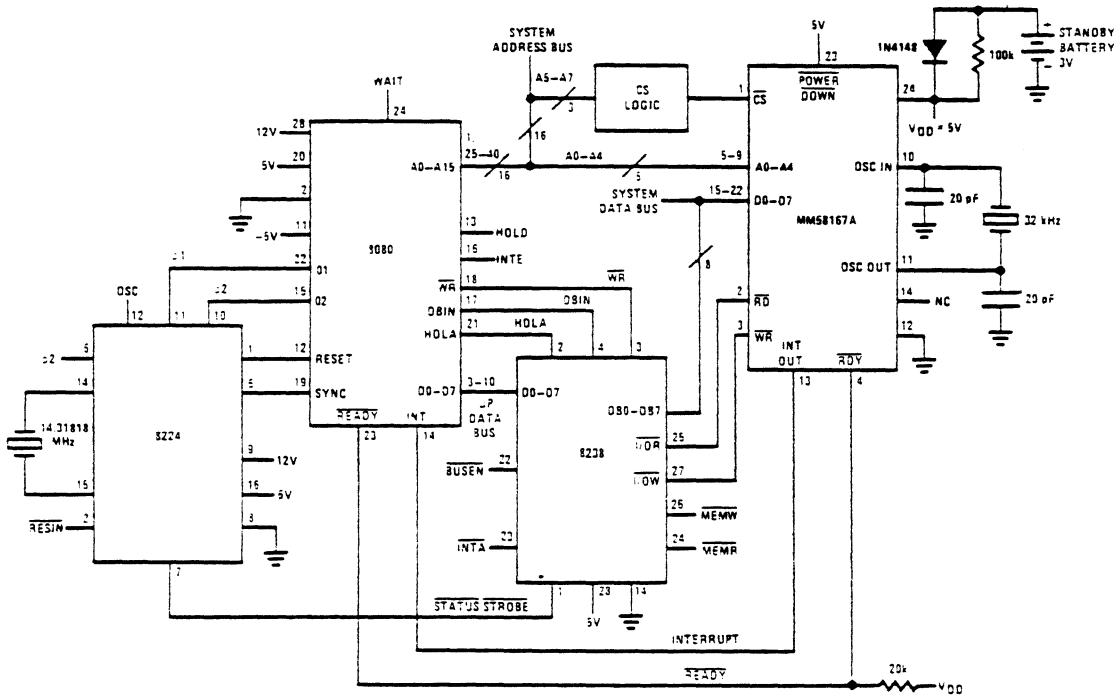
FIGURE 4. Write Cycle Timing

Typical Applications



Note 1: A ground line or ground plane guard trace should be included between pins 9 and 10 to insure the oscillator is not disturbed by the address line.

FIGURE 5. Typical Connection Diagram



Note 1: Must use 8238 or equivalent logic to insure advanced IOW pulse; so that the ready output of the MM58167A is valid by the end of ϕ_2 during the T3 microcycle.

Note 2: $t_{\phi 2} \geq t_{PS8080} + t_{DL8238} + t_{WRY58167A}$

FIGURE 6. 8080 System Interface with Battery Backup

Block Diagram

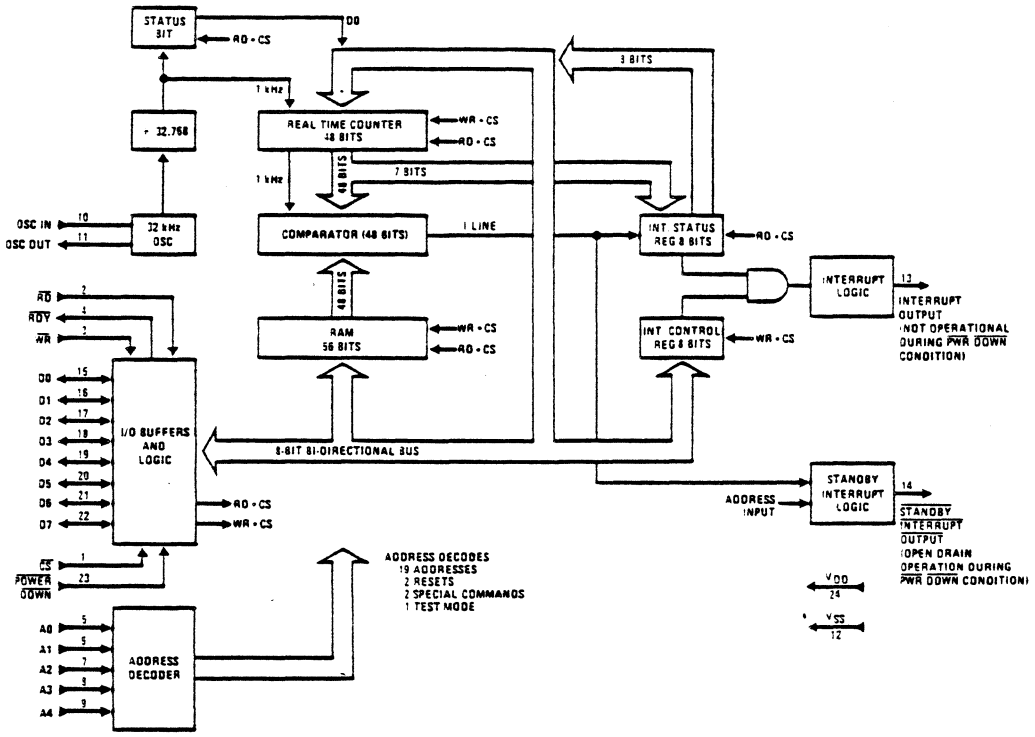


FIGURE 7

Physical Dimensions inches (millimeters)

Molded Dual-In-Line Package (N)
Order Number MM58167AN
NS Package Number N24A

LIFE SUPPORT POLICY

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INTELLIGENT GPIB INTERFACE CONTROLLER

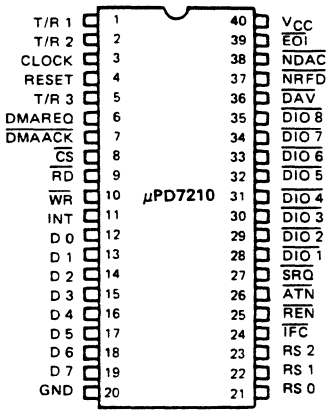
DESCRIPTION

The μPD7210 TLC is an intelligent GPIB Interface Controller designed to meet all of the functional requirements for Talkers, Listeners, and Controllers as specified by the IEEE Standard 488-1978. Connected between a processor bus and the GPIB, the TLC provides high level management of the GPIB to unburden the processor and to simplify both hardware and software design. Fully compatible with most processor architectures, Bus Driver/Receivers are the only additional components required to implement any type of GPIB interface.

FEATURES

- All Functional Interface Capability Meeting IEEE Standard
  - SH 1 (Source Handshake)
  - AH 1 (Acceptor Handshake)
  - T5 or TE5 (Talker or Extended Talker)
  - L3 or LE3 (Listener or Extended Listener)
  - SR1 (Service Request)
  - RL1 (Remote Local)
  - PP1 or PP2 (Parallel Port [Remote or Local Configuration])
  - DC 1(Device Clear)
  - DT1 (Device Trigger)
  - C1-5 (Controller [All Functions])
- Programmable Data Transfer Rate
- 16 MPU Accessible Registers – 8 Read/8 Write
- 2 Address Registers
  - Detection of MTA, MLA, MSA (My Talk/Listen/Secondary Address)
  - 2 Device Addresses
- EOS Message Automatic Detection
- Command (IEEE Standard 488-78) Automatic Processing and Undefined Command Read Capability
- DMA Capability
- Programmable Bus Transceiver I/O Specification (Works with T.I./Motorola/Intel)
- 1 to 8 MHz Clock Range
- TTL Compatible
- N Channel MOS
- +5V Single Power Supply
- 40-Pin Plastic DIP
- 8080/85/86 Compatible

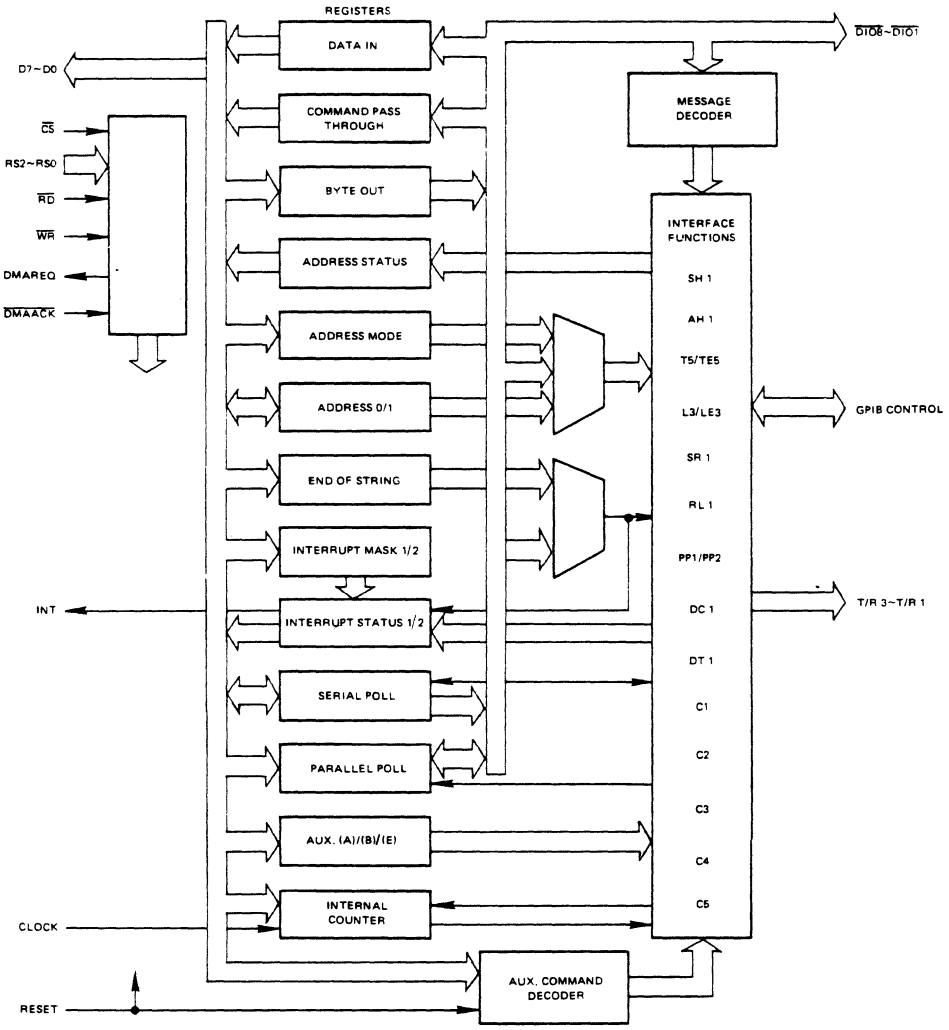
PIN CONFIGURATION



PIN IDENTIFICATION

PIN	NAME	I/O	DESCRIPTION
1	T/R1	O	Transmit/Receive Control – Input/Output Control Signal for the GPIB Bus Transceivers.
2	T/R2	O	Transmit/Receive Control – The function of T/R2, T/R3 are determined by the value of TRM1, TRM0 of the address mode register.
3	CLK	I	Clock – (1-8 MHz) Reference Clock for generating the state change prohibit times T1, T6, T7, T9 specified in IEEE Standard 488-1978.
4	RST	I	Reset – Resets 7210 to an idle state when high (active high).
5	T/R3	O	Transmit/Receive Control – Function determined by TRM1 and TRM0 of address mode register (See T/R2).
6	DRQ	O	DMA Request – 7210 requests data transfer to the computer system, becomes low on input of DMA acknowledge signal $\overline{DACK}$.
7	$\overline{DACK}$	I	DMA Acknowledge – (Active Low) Signal connects the computer system data bus to the data register of the 7210.
8	$\overline{CS}$	I	Chip Select – (Active Low) Enables access to the register selected by RS0-2 (read or write operation).
9	$\overline{RD}$	I	Read – (Active Low) Places contents of read register specified by RS0-2 – on D0-7 (Computer Bus).
10	$\overline{WR}$	I	Write – (Active Low) writes data on D0-7 into the write register specified by RS0-2.
11	INT / $\overline{INT}$	O	Interrupt Request – (Active High/Low) Becomes active due to any 1 of 13 internal interrupt factors (unmasked) active state software configurable, active high on chip reset.
12-19	D0-7	I/O	Data Bus – 8 bit bidirectional data bus, for interface to computer system.
20	GND		Ground.
21-23	RS0-2	I	Register Select – These lines select one of eight read (write) registers during a read (write) operation.
24	$\overline{IFC}$	I/O	Interface Clear – Control line used for clearing the interface functions.
25	$\overline{REN}$	I/O	Remote Enable – Control line used to select remote or local control of the devices.
26	$\overline{ATN}$	I/O	Attention – Control line which indicates whether data on DIO lines is an interface message or device dependent message.
27	$\overline{SRQ}$	I/O	Service Request – Control line used to request the controller for service.
28-35	$\overline{DIO1\text{-}8}$	I/O	Data Input/Output – 8 bit bidirectional bus for transfer of message on the GPIB.
36	$\overline{DAV}$	I/O	Data Valid – Handshake line indicating that data on DIO lines is valid.
37	$\overline{NRFD}$	I/O	Ready for Data – Handshake line indicating that device is ready for data.
38	$\overline{NDAC}$	I/O	Data Accepted – Handshake line indicating completion of message reception.
39	$\overline{EOI}$	I/O	End or Identify – Control line used to indicate the end of multiple byte transfer sequence or to execute a parallel polling in conjunction with ATN.
40	V_{CC}		+5V DC – Technical Specifications: +5V; NMOS; 500 MW; 40 Pins; TTL Compatible; 1-8 MHz.

BLOCK DIAGRAM



μPD7210

INTRODUCTION

The IEEE Standard 488 describes a "Standard Digital Interface for Programmable Instrumentation" which, since its introduction in 1975, has become the most popular means of interconnecting instruments and controllers in laboratory, automatic test and even industrial applications. Refined over several years, the 488-1978 standard, also known as the General Purpose Interface Bus (GPIB), is a highly sophisticated standard providing a high degree of flexibility to meet virtually most all instrumentation requirements. The μPD7210 TLC implements all of the functions that are required to interface to the GPIB. While it is beyond the scope of this document to provide a complete explanation of the IEEE 488 Standard, a basic description follows:

The GPIB interconnects up to 15 devices over a common set of data control lines. Three types of devices are defined by the standard: Talkers, Listeners, and Controllers, although some devices may combine functions such as Talker/Listener or Talker/Controller.

Data on the GPIB is transferred in a bit parallel, byte serial fashion over 8 Data I/O lines (D101 – D108). A 3 wire handshake is used to ensure synchronization of transmission and reception. In order to permit more than one device to receive data at the same time, these control lines are "Open Collector" so that the slowest device controls the data rate. A number of other control lines perform a variety of functions such as device addressing, interrupt generation, etc.

The μPD7210 TLC implements all functional aspects of Talker, Listener and Controller functions ad defined by the 488-1978 Standard, and on a single chip.

GENERAL

The μPD7210 TLC is an intelligent controller designed to provide high level protocol management of the GPIB, freeing the host processor for other tasks. Control of the TLC is accomplished via 16 internal registers. Data may be transferred either under program control or via DMA using the TLC's DMA control facilities to further reduce processor overhead. The processor interface of the TLC is general in nature and may be readily interfaced to most processor lines.

In addition to providing all control and data lines necessary for a complete GPIB implementation, the TLC also provides a unique set of bus transceiver controls permitting the use of a variety of different transceiver configurations for maximum flexibility.

INTERNAL REGISTERS

The TLC has 16 registers, eight of which are read and 8 write.

REGISTER NAME	ADDRESSING					SPECIFICATION							
	R	R	R	WR	CS								
	S	S	S	WR	CS								
	2	1	0	WR	CS								
Data In [0R]	0	0	0	WR	CS	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
Interrupt Status 1 [1R]	0	0	1	WR	CS	CPT	APT	DET	END	DEC	ERR	DO	DI
Interrupt Status 2 [2R]	0	1	0	WR	CS	INT	SRQI	LOK	REM	CO	LOKC	REMC	ADSC
Serial Poll Status [3R]	0	1	1	WR	CS	S8	PEND	S6	S5	S4	S3	S2	S1
Address Status [4R]	1	0	0	WR	CS	CIC	ATN	SPMS	LPAS	TPAS	LA	TA	MJMN
Command Pass Through [5R]	1	0	1	WR	CS	CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0
Address 0 [6R]	1	1	0	WR	CS	X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0
Address 1 [7R]	1	1	1	WR	CS	EOI	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1
Byte Out [0W]	0	0	0	WR	CS	BO7	BO6	BO5	BO4	BO3	BO2	BO1	BO0
Interrupt Mask 1 [1W]	0	0	1	WR	CS	CPT	APT	DET	END	DEC	ERR	DO	DI
Interrupt Mask 2 [2W]	0	1	0	WR	CS	0	SRQI	DMAO	DMAI	CO	LOKC	REMC	ADSC
Serial Poll Mode [3W]	0	1	1	WR	CS	S8	rsv	S6	S5	S4	S3	S2	S1
Address Mode [4W]	1	0	0	WR	CS	ton	lon	TRM1	TRM0	0	0	ADM1	ADM0
Auxiliary Mode [5W]	1	0	1	WR	CS	CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0
Address 0/1 [6W]	1	1	0	WR	CS	ARS	DT	DL	AD5	AD4	AD3	AD2	AD1
End of String [7W]	1	1	1	WR	CS	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

DATA REGISTERS

The data registers are used for data and command transfers between the GPIB and the microcomputer system.

DATA IN (0R)

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

Holds data sent from the GPIB to the computer

BYTE OUT (0W)

BO7	BO6	BO5	BO4	BO3	BO2	BO1	BO0

Holds information written into it for transfer to the GPIB

INTERRUPT REGISTERS

The interrupt registers are composed of interrupt status bits, interrupt mask bits, and some other noninterrupt related status bits.

READ

INTERRUPT STATUS 1 (1R)	CPT	APT	DET	END	DEC	ERR	DO	DI
INTERRUPT STATUS 2 (2R)	INT	SRQI	LOK	REM	CO	LOKC	REMC	ADSC

WRITE

INTERRUPT MASK 1 (1W)	CPT	APT	DET	END	DEC	ERR	DO	DI
INTERRUPT MASK 2 (2W)	0	SRQI	DMAO	DMAI	CO	LOKC	REMC	ADSC

There are thirteen factors which can generate an interrupt from the μPD7210, each with their own status bit and mask bit.

The interrupt status bits are always set to one if the interrupt condition is met. The interrupt mask bits decide whether the INT bit and the interrupt pin will be active for that condition.

Interrupt Status Bits

INT	OR of All Unmasked Interrupt Status Bits
CPT	Command Pass Through
APT	Address Pass Through
DET	Device Trigger
END	End (END or EOS Message Received)
DEC	Device Clear
ERR	Error
DO	Data Out
DI	Data In
SRQI	Service Request Input
LOKC	Lockout Change
REMC	Remote Change
ADSC	Address Status Change
CO	Command Output

Non Interrupt Status Bits

LOK	Lockout
REM	Remote/Local
DMAO	Enable/Disable DMA Out
DMAI	Enable/Disable DMA In

SERIAL POLL REGISTERS

READ

SERIAL POLL STATUS [3R]	S8	PEND	S6	S5	S4	S3	S2	S1

WRITE

SERIAL POLL MODE [3W]	S8	rsv	S6	S5	S4	S3	S2	S1

The Serial Poll Mode register holds the STB (status byte: S8, S6-S1) sent over the GPIB and the local message rsv (request service). The Serial Poll Mode register may be read through the Serial Poll Status register. The PEND is set by rsv = 1, and cleared by NPRS • $\overline{rsv}$ = 1 (NPRS = Negative Poll Response State).

ADDRESS MODE/STATUS REGISTERS

ADDRESS STATUS [4R]	CIC	$\overline{ATN}$	SPMS	LPAS	TPAS	LA	TA	MJMN
ADDRESS MODE [4W]	ton	lon	TRM1	TRM0	0	0	ADM1	ADM0

The Address Mode register selects the address mode of the device and also sets the mode for T/R3 and T/R2 the transceiver control lines.

The TLC is able to automatically detect two types of addresses which are held in address registers 0 and 1. The addressing modes are outlined below.

ADDRESS MODES

ton	lon	ADM1	ADM0	ADDRESS MODE	CONTENTS OF ADDRESS (0) REGISTER	CONTENTS OF ADDRESS (1) REGISTER
1	0	0	0	Talk only mode	Address Identification Not Necessary	
0	1	0	0	Listen only mode	Not Used	
0	0	0	1	Address mode 1	Major talk address or Major listen address	Minor talk address or Minor listen address
0	0	1	0	Address mode 2	Primary address (talk or listen)	Secondary address (talk or listen)
0	0	1	1	Address mode 3	Primary address (major talk or major listen)	Primary address (minor talk or minor listen)
Combinations other than above indicated Prohibited.						

Notes: A1 – Either MTA or MLA reception is indicated by coincidence of either address with the received address. Interface function T or L.

A2 – Address register 0 = primary, Address register 1 = secondary, interface function TC or LC.

A3 – CPU must read secondary address via Command Pass Through Register. TE or LC Command.

ADDRESS STATUS BITS

$\overline{ATN}$	Data Transfer Cycle (device in CSBS)
LPAS	Listener Primary Addressed State
TPAS	Talker Primary Addressed State
CIC	Controller Active
LA	Listener Addressed
TA	Talker Addressed
MJMN	Sets minor T/L address Reset = Major T/L address
SPMS	Serial Poll Mode State

ADDRESS REGISTERS

ADDRESS 0 [6R]	X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0
ADDRESS 1 [7R]	EOI	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1
ADDRESS 0/1 [6W]	ARS	DT	DL	AD5	AD4	AD3	AD2	AD1

Address settings are made by writing into the address 0/1 register. The function of each bit is described below.

ADDRESS 0/1 REGISTER BIT SELECTIONS

ARS – Selects which address register 0 or 1
DT – Permits or Prohibits address to be detected as Talk
DL – Permits or Prohibits address to be detected as Listen
AD5 – AD1 – Device address value
EOI – Holds the value of EOI line when data is received

COMMAND PASS THROUGH REGISTER

COMMAND PASS THROUGH [5R]	CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0

The CPT register is used such that the CPU may read the DIO lines in the cases of undefined command, secondary address, or parallel poll response.

END OF STRING REGISTER

END OF STRING [7W]	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

This register holds either a 7 or 8 bit EOS message byte used in the GPIB system to detect the end of a data block. Aux Mode Register A controls the specific use of this register.

AUXILIARY MODE REGISTER

AUXILIARY MODE [5W]	CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0

This is a multipurpose register. A write to this register generates one of the following operations according to the values of the CNT bits.

CNT 2	CNT 1	CNT 0	COM 4	COM 3	COM 2	COM 1	COM 0	OPERATION
0	0	0	C_4	C_3	C_2	C_1	C_0	Issues an auxiliary command specified by C_4 to C_0.
0	0	1	0	F_3	F_2	F_1	F_0	The reference clock frequency is specified and T_1, T_6, T_7, T_9 are determined as a result.
0	1	1	U	S	P_3	P_2	P_1	Makes write operation to the parallel poll register.
1	0	0	A_4	A_3	A_2	A_1	A_0	Makes write operation to the aux. (A) register.
1	0	1	B_4	B_3	B_2	B_1	B_0	Makes write operation to the aux. (B) register.
1	1	0	0	0	0	E_1	E_0	Makes write operation to the aux. (E) register.

AUXILIARY COMMANDS 0 0 0 C_4 C_3 C_2 C_1 C_0

COM 43210			
00000	iepon	–	Immediate Execute pon – Generate local pon Message
00010	crst	–	Chip Reset – Same as External Reset
00011	rrfd	–	Release RFD
00100	trig	–	Trigger
00101	rtl	–	Return to Local Message Generation
00110	seoi	–	Send EOI Message
00111	nvld	–	Non Valid (OSA reception) – Release DAC Holdoff
01111	vld	–	Valid (MSA reception, CPT, DEC, DET) – Release DAC Holdoff
0X001	sppf	–	Set/Reset Parallel Poll Flag
10000	gts	–	Go To Standby
10001	tca	–	Take Control Asynchronously
10010	tcs	–	Take Control Synchronously
11010	tcse	–	Take Control Synchronously on End
10011	ltn	–	Listen
11011	ltnc	–	Listen with Continuous Mode
11100	lun	–	Local Unlisten
11101	epp	–	Execute Parallel Poll
1X110	sifc	–	Set/Reset IFC
1X111	sren	–	Set/Reset REN
10100	dsc	–	Disable System Control

INTERNAL COUNTER 0 0 1 0 F_3 F_2 F_1 F_0

The internal counter generates the state change prohibit times (T_1, T_6, T_7, T_9) specified in the IEEE std 488-1978 with reference to the clock frequency.

AUXILIARY A REGISTER 1 0 0 A_4 A_3 A_2 A_1 A_0

Of the 5 bits that may be specified as part of its access word, two bits control the GPIB data receiving modes of the 7210 and 3 bits control how the EOS message is used.

A_1	A_0	DATA RECEIVING MODE
0	0	Normal Handshake Mode
0	1	RFD Holdoff on all Data Mode
1	0	RFD Holdoff on End Mode
1	1	Continuous Mode

BIT NAME			FUNCTION
A_2	0	Prohibit	Permits (prohibits) the setting of the END bit by reception of the EOS message.
	1	Permit	
A_3	0	Prohibit	Permits (prohibits) automatic transmission of END message simultaneously with the transmission of EOS message TACS.
	1	Permit	
A_4	0	7 bit EOS	Makes the 8 bits/7 bits of EOS register the valid EOS message.
	1	8 bit EOS	

AUXILIARY B REGISTER 1 0 1 B_4 B_3 B_2 B_1 B_0

The Auxiliary B Register is much like the A Register in that it controls the special operating features of the device.

BIT NAME			FUNCTION
B_0	1	Permit	Permits (prohibits) the detection of undefined command. In other words, it permits (prohibits) the setting of the CPT bit on reception of an undefined command.
	0	Prohibit	
B_1	1	Permit	Permits (prohibits) the transmission of the END message when in serial poll active state (SPAS).
	0	Prohibit	
B_2	1	T_1 (high-speed)	T_1 (high speed) as T_1 of handshake after transmission of 2nd byte following data transmission.
	0	T_1 (low-speed)	
B_3	1	INT	Specifies the active level of INT pin.
	0	INT	
B_4	1	1st = SRQS	SRQS indicates the value of 1st level local message (the value of the parallel poll flag is ignored). SRQS = 1 . . . 1st = 1. SRQS = 0 . . . 1st = 0.
	0	1st = Parallel Poll Flag	The value of the parallel poll flag is taken as the 1st local message.

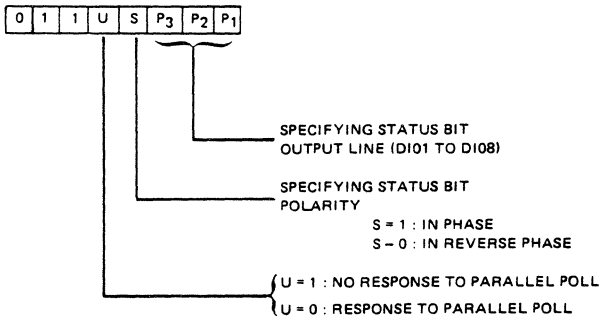
AUXILIARY E REGISTER 1 1 0 0 0 0 E_1 E_0

This register controls the Data Acceptance Modes of the TLC.

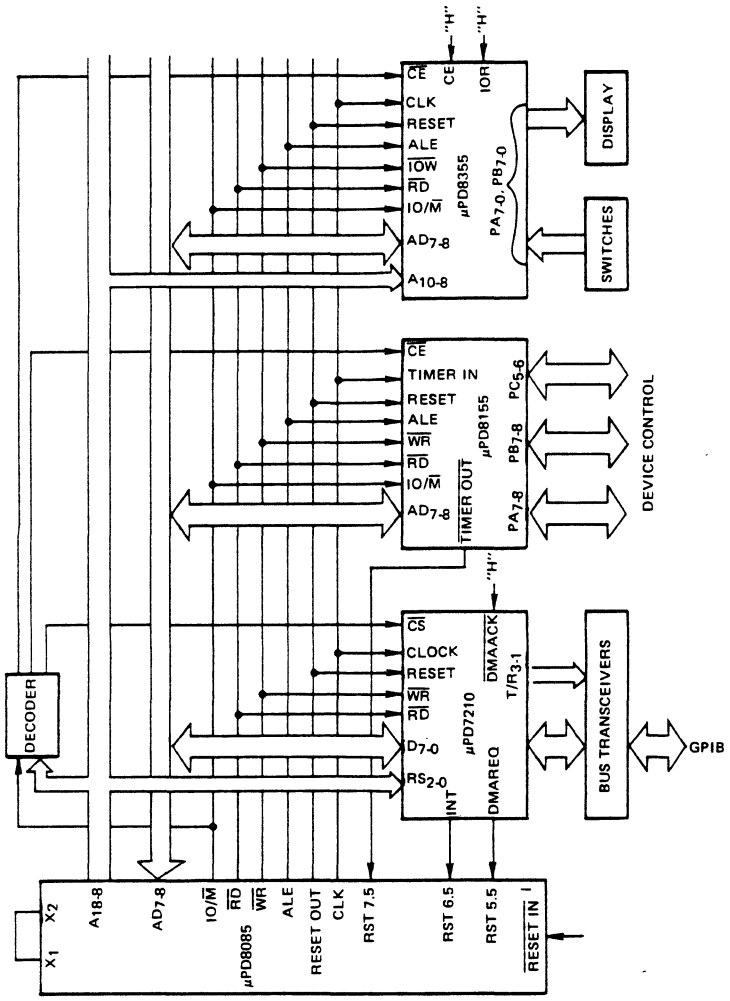
BIT	FUNCTION		
E_0	1	Enable	DAC Holdoff by initiation of DCAS
	0	Disable	
E_1	1	Enable	DAC Holdoff by initiation of DTAS
	0	Disable	

Parallel Poll Register → 0 1 1 U S P_3 P_2 P_1

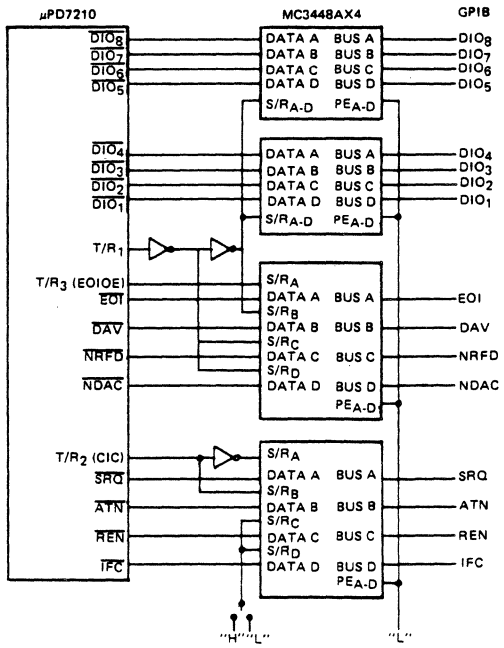
The Parallel Poll Register defines the parallel poll response of the μPD7210.



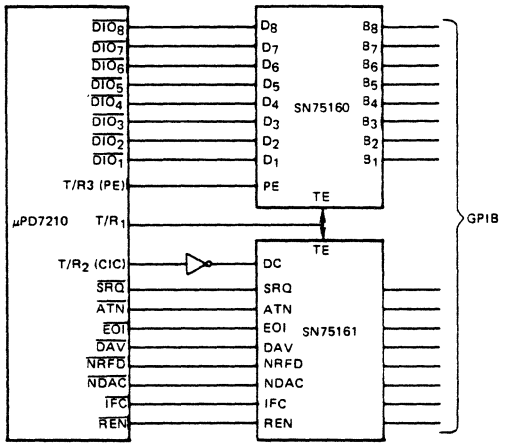
MINIMUM 8085 SYSTEM
WITH μPD7210



MINIMUM 8085 SYSTEM
WITH μPD7210 (CONT.)



Note: In this example, high-speed data transfer cannot be made since the bus transceiver is of the open collector type (Set $B_2 = 0$).



Note: In the case of low-speed data transfer ($B_2 = 0$), the T/R_3 pin can be used as a TRIG output. The PE input of SN75160 should be cleared to "0." Using this conction, pass-control operation cannot be used.

ABSOLUTE MAXIMUM RATINGS

T_a = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNITS
Supply Voltage	V_{CC}		−0.5 ∼ +7.0	V
Input Voltage	V_I		−0.5 ∼ +7.0	V
Output Voltage	V_O		−0.5 ∼ +7.0	V
Operating Temperature	T_{opt}		0 ∼ +70	°C
Strage Temperature	T_{stg}		−65 ∼ + 125	°C

DC CHARACTERISTICS

T_a = 0 ∼ +70°C, V_{CC} = 5V ± 10%

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Input Low Voltage	V_{IL}		−0.5		+0.8	V
Input High Voltage	V_{IH}		+ 2.0		V_{CC} +0.5	V
Low Level Output Voltage	V_{OL}	I_{OL} = 2mA (4mA : T/R1 Pin)			+0.45	V
High Level Output Voltage	V_{OH1}	I_{OH} = −400uA, Except INT	+ 2.4			V
	V_{OH2}	I_{OH} = −400uA, INT Pin	+ 2.4			V
		I_{OH} = −50uA, INT Pin	+ 3.5			V
Input Leakage Current	I_{IL}	I_{IN} = 0V ∼ V_{CC}	−10		+10	uA
Output Leakage Current	I_{OL}	I_{OUT} = 0.45V ∼ V_{CC}	−10		+10	uA
Supply Current	I_{CC}				+180	mA

CAPACITANCE

T_a = 25°C, V_{CC} = GND = 0V

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Input Capacitance	C_{IN}	f = 1 MHz, All Pins Except Pin Under Test Tied to AC Ground			10	pF
Output Capacitance	C_{OUT}				15	pF
I/O Capacitance	$C_{I/O}$				20	pF

AC CHARACTERISTICS

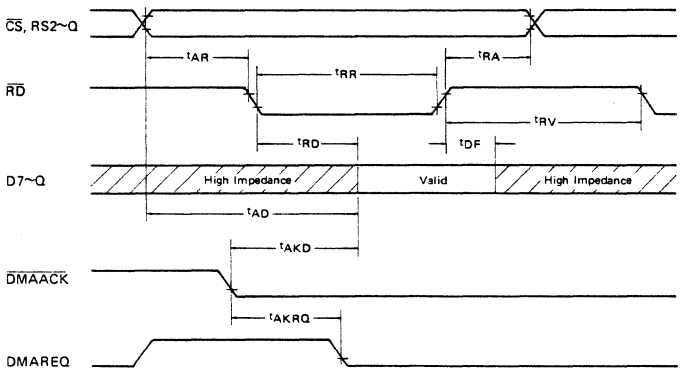
T_a = 0 ∼ +70°C, V_{CC} = 5V ± 10%

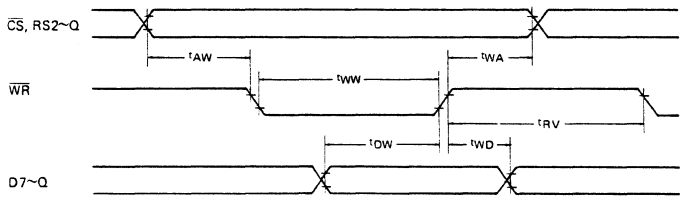
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Address Setup to $\overline{RD}$	t_{AR}	$RS_{2\text{-}0}$	85			ns
		$\overline{CS}$	0			
Address Hold from $\overline{RD}$	t_{RA}		0			ns
$\overline{RD}$ Pulse Width	t_{RR}		170			ns
Data Delay from Address	t_{AD}				250	ns
Data Delay from $\overline{RD}$ ↓	t_{RD}				150	ns
Output Float Delay from $\overline{RD}$ ↑	t_{DF}		0		80	ns
$\overline{RD}$ Recovery Time	t_{RV}		250			ns
Address Setup to $\overline{WR}$	t_{AW}		0			ns
Address Hold from $\overline{WR}$	t_{WA}		0			ns
$\overline{WR}$ Pulse Width	t_{WW}		170			ns
Data Setup to $\overline{WR}$	t_{DW}		150			ns
Data Hold from $\overline{WR}$	t_{WD}		0			ns
$\overline{WR}$ Recovery Time	t_{RV}		250			ns
DMAREQ ↓ Delay from $\overline{DMAACK}$	t_{AKRQ}				130	ns
Data Delay from $\overline{DMAACK}$	t_{AKD}				200	ns

AC CHARACTERISTICS

T_a = 0 ~ + 70°C, V_{CC} = 5V ± 10%

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
$\overline{EOI}$ ↓ → $\overline{DIO}$	t_{EOD1}	PPSS → PPAS, ATN = True			250	ns
$\overline{EOI}$ ↓ → T/$\overline{R1}$ ↑	t_{EOT11}	PPSS → PPAS, ATN = True			155	ns
$\overline{EOI}$ ↑ → T/$\overline{R1}$ ↓	t_{EOT12}	PPAS → PPSS, ATN = False			200	ns
$\overline{ATN}$ ↓ → $\overline{NDAC}$ ↓	t_{ATND}	AIDS → ANRS, LIDS			155	ns
$\overline{ATN}$ ↓ → T/$\overline{R1}$ ↓	t_{ATT1}	TACS + SPAS → TADS, CIDS			155	ns
$\overline{ATN}$ ↓ → T/$\overline{R2}$ ↓	t_{ATT2}	TACS + SPAS → TADS, CIDS			200	ns
$\overline{DAV}$ ↓ → DMAREQ ↑	t_{DVRQ}	ACRS → ACDS, LACS			600	ns
$\overline{DAV}$ ↓ → $\overline{NRFD}$ ↓	t_{DVNR1}	ACRS → ACDS			350	ns
$\overline{DAV}$ ↓ → $\overline{NDAC}$ ↑	t_{DVND1}	ACRS → ACDS → AWNS			650	ns
$\overline{DAV}$ ↑ → $\overline{NDAC}$ ↓	t_{DVND2}	AWNS → ANRS			350	ns
$\overline{DAV}$ ↑ → $\overline{NRFD}$ ↑	t_{DVNR2}	AWNS → ANRS → ACRS			350	ns
$\overline{RD}$ ↓ → $\overline{NRFD}$ ↑	t_{RNR}	ANRS → ACRS LACS, DI reg. selected			500	ns
$\overline{NDAC}$ ↑ → DMAREQ ↑	t_{NDRQ}	STRS → SWNS → SGNS, TACS			400	ns
$\overline{NDAC}$ ↑ → $\overline{DAV}$ ↑	t_{NDDV}	STRS → SWNS → SGNS			350	ns
$\overline{WR}$ ↑ → $\overline{DIO}$	t_{WDI}	SGNS → SDYS, BO reg. selected			250	ns
$\overline{NRFD}$ ↑ → $\overline{DAV}$ ↓	t_{NRDV}	SDYS → STRS, T_1 = True			350	ns
$\overline{WR}$ ↑ → $\overline{DAV}$ ↓	t_{WDV}	SGNS → SDYS → STRS BO reg. selected, RFD = True $N_F = f_C$ = 8 MHz, T_1 (High Speed)			830 +t_{SYNC}	ns
TRIG Pulse Width	t_{TRIG}		50			ns





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NEC reserves the right to make changes any time without notice in order to improve design and supply the best product possible.

APPENDIX I

Product Error Report

DEAR CUSTOMER,

WHILE FORCE COMPUTERS HAS ACHIEVED A VERY HIGH STANDARD OF QUALITY IN OUR PRODUCTS AND DOCUMENTATION, WE CONTINUALLY SEEK SUGGESTIONS FOR IMPROVEMENTS.

WE WOULD APPRECIATE ANY FEEDBACK YOU CARE TO OFFER.

PLEASE USE ATTACHED "PRODUCT ERROR REPORT" FORM FOR YOUR COMMENTS AND RETURN IT TO ONE OF OUR FORCE COMPUTERS OFFICES.

SINCERELY

FORCE COMPUTERS

P R O D U C T E R R O R R E P O R T

HARDWARE/SOFTWARE/SYSTEMS

PRODUCT : _____

SERIAL NO. : _____

DATE OF PURCHASE : _____

ORIGINATOR : _____

COMPANY : _____

ADDRESS : _____

_____

_____

DATE : _____

TELEPHONE : ( ) _____ EXT _____

CONTACT : _____

This box to be completed by FORCE
DATE : _____
PR# : _____
ACTION BY :
Engineering ( )
Marketing ( )
Production ( )

AFFECTED PRODUCT: ( ) SOFTWARE ( ) HARDWARE ( ) SYSTEM

AFFECTED DOCUMENTATION: ( ) SOFTWARE ( ) HARDWARE ( ) SYSTEM

ERROR DESCRIPTION : _____

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SEND TO :

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Marketing
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Los Gatos, CA 95030
U.S.A.

FORCE Computers GmbH
Marketing
Daimlerstrasse 9
8012 Ottobrunn/Munich
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FORCE Computers FRANCE
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