

M2611T#D, M2612ET/M2613ET/M2614ET

INTELLIGENT DISK DRIVES

OEM MANUAL

| REVISION RECORD | | |
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PREFACE

This manual describes the M2612ET, M2613ET, M2614ET, and M2611T (D version) intelligent disk drives. This manual provides a detailed explanation of the intelligent disk drives, including specifications and functions.

This manual consists of the following:

CHAPTER 1 GENERAL DESCRIPTION

CHAPTER 2 CONFIGURATION

CHAPTER 3 INSTALLATION

CHAPTER 4 HOST INTERFACE

CHAPTER 5 DATA FORMAT

CHAPTER 6 OTHER

In this manual, the M2611T (D version), M2612ET, M2613ET, and M2614ET intelligent disk drives are abbreviated as M261xET, drive, device or IDD unless otherwise specified.

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CHAPTER 1 GENERAL DESCRIPTION

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| 1.2 | Features |
| 1.3 | Specifications |
| 1.4 | Environmental Conditions |
| 1.5 | Power Requirements |
| 1.6 | Reliability |
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| 1.8 | Media Defect |

1.1 Introduction

The M261xET are compact and highly reliable 3.5" fixed disk drives containing a disk controller. The M261xT can be connected to the IBM PC-AT interface.

1.2 Features

(1) Compact size

The M261xET has one or more magnetic disks (95 mm in diameter) which are driven by a DC motor directly connected to the spindle. The controller is built in to the PCA of the M261xET.

(2) Large storage capacity

Each magnetic disk can store data of up to 45 MB due to employment of the 1/7 RLL data recording method. The M2611T, M2612ET, M2613ET, and M2614ET store 45 MB, 90 MB, 135 MB, and 180 MB respectively.

(3) Connectable to IBM PC-AT interface

The embedded PC-AT interface controller enables the M261xET to be connected to the IBM PC-AT interface via a simple adaptor board. This board consists of address decoder and driver/receiver (74LS244/245 or equivalent).

(4) **56 KB ring buffer and 6 KB write buffer**

The M261xET supports a look-ahead cache to increase system throughput. The M261xET uses 56 KB of the cache to read and 6 KB to write.

(5) **High transfer rate**

A maximum transfer rate of 3.7 MW/s is accomplished with a 30-MHz clock signal and high-speed buffer management. When the data transfer rate becomes near 3.7 MW/s or more, the host must receive IOCHRDY signal and maintain the transfer synchronization by setting a wait state.

(6) **Error correction and retry functions by ECC**

When a recoverable error is found, the M261xET tries to correct it internally. Correction of recoverable data errors is accomplished with a 7-bit or 4-bit ECC.

(7) **Built-in self-diagnosis**

The M261xET tests itself with diagnostic commands.

(8) **High reliability**

The components of the M261xET (e. g., disks, read/write heads, and positioners) are sealed in a disk enclosure which has a circulation filter and a breather filter to prevent contamination.

(9) **High-speed head positioning**

A rotary voice coil motor positions the read/write heads at high speed.

(10) **Maintenance-free mechanism**

The M261xET does not require preventive or periodic maintenance operations.

(11) **Vertical or horizontal installation**

The M261xET can be installed on the vertical or horizontal orientation.

(12) **Low power consumption in ready status**

Typical power consumption is 5.5 watts for the M2611T and 6.4 watts for the M2612ET to M2614ET including seek, write and read operation.

(13) Low operating noise (Ready condition)

Approximately 40 dB for the M2611 (A-scale weighting) and approximately 43 dB for the M2612ET to M2614ET (A-scale weighting)

(14) Low vibration

The M261xET stands on four rubber vibration isolators for absorption of operating vibrations.

(15) Power save mode

When the M261xET will not be operated for a long time, power consumption can be reduced by using the power save mode.

(16) DC power supply

DC voltages of +5 V and +12 V are available. M2611T has two types of power connectors, the one is big type (4 pins), the other is small type (CN6 : 3 pins).

(17) Reliable LSI chips

The controller mechanism and the drive mechanism are made smaller by means of a custom LSI and two microprocessor chips. The read/write head IC is mounted on the head positioning arm to improve the signal-to-noise ratio and to eliminate read errors.

1.3 Specifications

1.3.1 Functional specifications

Table 1.1 M2612ET/13ET/14ET functional specifications

| Model | | M2612ET | M2613ET | M2614ET |
|--|----------------|---------------------------------------|------------|------------|
| Specifications | | | | |
| Total storage capacity (Formatted) * | | 90.1 (MB) | 135.2 (MB) | 180.3 (MB) |
| Number of heads (physical) | | 4 | 6 | 8 |
| Number of cylinders (physical) | | 1,334 | | |
| Storage capacity/track (Formatted) | | 16,896 (B) | | |
| Recording method | | 1/7 RLL | | |
| Recording density | | 29,571 (BPI) | | |
| Track density | | 1,681 (TPI) | | |
| Rotational Speed | | 3,490 (rpm) | | |
| Average latency time | | 8.6 (ms) | | |
| Positioning time | Minimum | 8 (ms) | | |
| | Average | 20 (ms) | | |
| | Maximum | 36 (ms) | | |
| Start/stop time | Start | Typ. 8 (s) [Max. 15 (s)] | | |
| | Stop | Type. 17 (s) [Max. 25 (s)] | | |
| Interface | | PC-AT Cable length: 0.5 (m) Max. | | |
| Data transfer rate | To/From Media | 1.25 (MB/s) | | |
| | To/From Buffer | 3.7 (MW/s) Max. | | |
| Bytes per block (Fixed) | | 512 (B) | | |
| PC-AT command specifications | | PC-AT command compatibility supported | | |
| Data buffer | | 56-KB FIFO ring buffer | | |
| External size (Height × Depth × Width) | | 41.3 (mm) × 146.0 (mm) × 101.6 (mm) | | |
| Weight | | 1.0 (kg) | | |

* In case of bad track free

Table 1.2 M2611T (D version) specifications

| Specifications | Model | M2611T (D version) |
|--|-----------------------|---------------------------------------|
| Total storage capacity (Formatted)* | | 45.0 (MB) |
| Number of heads (physical) | | 2 |
| Number of cylinders (physical) | | 1,334 |
| Storage capacity per track (Formatted) | | 16,896 (B) |
| Recording method | | 1/7 RLL |
| Recording density | | 29,571 (BPI) |
| Track density | | 1,681 (TPI) |
| Rotational Speed | | 3,490 (rpm) |
| Average latency time | | 8.6 (ms) |
| Positioning time | Minimum | 10 (ms) |
| | Average | 25 (ms) |
| | Maximum | 42 (ms) |
| Start/stop time | Start | Typ. 6 (s) [Max. 15 (s)] |
| | Stop | Typ. 8 (s) [Max. 25 (s)] |
| Interface | | PC-AT Cable length: 0.5 (m) Max. |
| Data transfer rate | To/From Storage Media | 1.25 (MB/s) |
| | To/From Buffer | 3.7 (MW/s) Max. |
| Bytes per block (Fixed) | | 512 (B) |
| PC-AT command specifications | | PC-AT command compatibility supported |
| Data buffer | | 56-KB FIFO ring buffer |
| External size (Height × Depth × Width) | | 25.4 (mm) × 146.0 (mm) × 101.6 (mm) |
| Weight | | 0.6 (kg) |

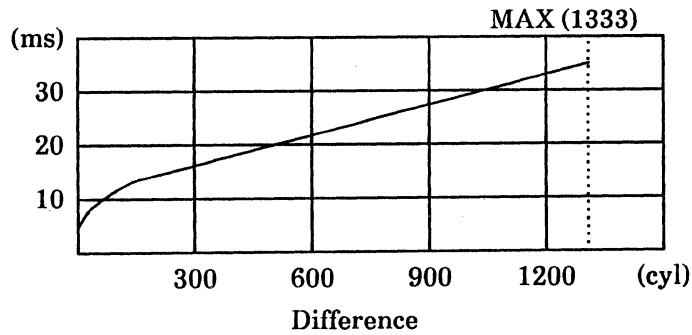
* In case of bad track free

1.3.2 Ordering specifications

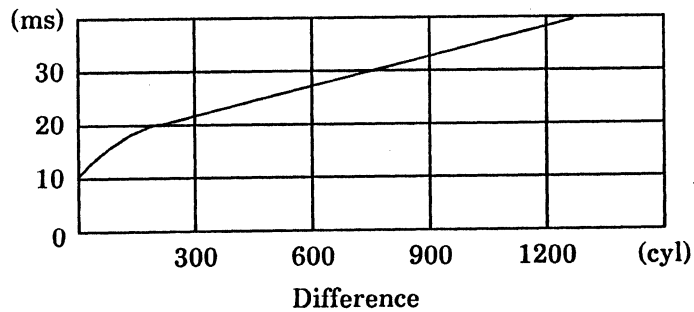
The following table lists models and part numbers to be used when placing orders.

| Model name | Storage capacity | Part number | Mounting screw |
|------------|------------------|-------------------|----------------|
| M2611T | 45 MB | B03B-7065-B301A#D | M3 |
| M2612ET | 90 MB | B03B-7055-B304A | M3 |
| M2613ET | 135 MB | B03B-7055-B305A | M3 |
| M2614ET | 180 MB | B03B-7055-B306A | M3 |

1.3.3 Positioning time (M2612ET to M2614ET)



Positioning time (M2611T)



1.3.4 Start and stop time

Typical start time (time from when power is turned on until the IDD is ready) is 6 seconds or less (M2611T), 8 seconds or less (M2612ET ~ 14ET), and typical stop time (time to completely stop when power is turned off) is 8 seconds or less (M2611T), 17 seconds or less (M2612ET ~ 14ET).

1.4 Environmental Conditions

| | | |
|-----------------------|---|---|
| Temperature | Operating | 5°C to 45°C (5°C to 58° on disk enclosure base) |
| | Nonoperating Temperature change | – 45°C to 60°C 15°C or less per hour |
| Relative humidity | Operating | 20% to 80% (Maximum wet bulb temperature : 29°C) |
| | Nonoperating | 5% to 95% (Maximum wet bulb temperature : 29°C) There must be no condensation. |
| Vibration | Operating (*1) | 0.3G (5 to 150 Hz) 0.5G (150 to 250 Hz) Test condition : Frequency cycles between 5 and 250 Hz every two minutes. Test length is one hour. (except for resonance points) |
| | Nonoperating | 0.5G (5 to 150 Hz) 1.0G (150 to 250 Hz) Test condition : Frequency cycles between 5 and 250 Hz every two minutes. Test length is one hour. (Power-off after installation) |
| Shock resistance (*2) | Operating Power-off, shipping, storage | 5.0G (10 ms maximum) 50G (10 ms maximum) |
| Altitude | Operating | – 60 to 3,000 m |
| | Nonoperating | 12,000 m (maximum) |

*1 Tested on a solid structure

*2 Tested on a solid frame

1.5 Power Requirements

(1) Input voltage and allowable variation

| | Input voltage |
|-------|----------------|
| +12 V | +12 V \pm 5% |
| +5 V | +5 V \pm 5% |

The above values are measured at the power input pin.

(2) Power Supply Current

| Voltage \ Current | M2611T | | M2612ET/M2613ET/M2614ET | |
|-------------------|--------------|--------------|-------------------------|--------------|
| | Peak current | Steady-state | Peak current | Steady-state |
| +12 V | 1.5 A max. | 0.3 A | 2.0 A max. | 0.4 A |
| +5 V | — | 0.6 A | — | 0.6 A |

(3) Ripple

+5 V: maximum 50 mVp-p, +12 V: maximum 100 mVp-p

High frequency noise: maximum 100 mVp-p

(4) Power consumption

| Mode | M2612ET/M2613ET/M2614ET | M2611T |
|------------------|-------------------------|------------|
| Steady state | Typ. 6.4 W | Typ. 5.5 W |
| Power save state | 3.5 W | 2.5 W |

Steady state includes SEEK, WRITE and READ operation.
See Subsection 4.4.8 for explanation of POWER COMMANDS.

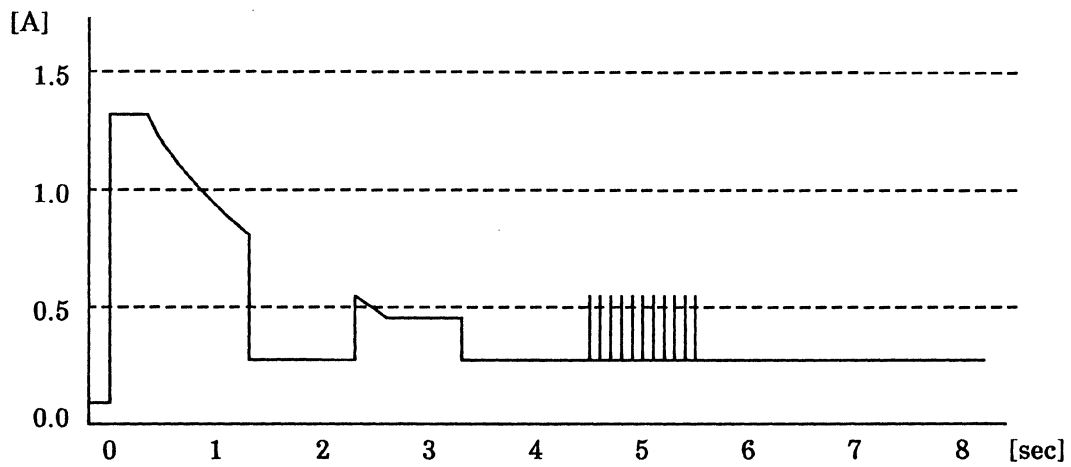
(5) Current consumption (Typ.)

| | M2611T | | |
|------|--------|--------|--------|
| | Seek | W/R | Ready |
| +12V | 0.25 A | 0.25 A | 0.25 A |
| +5V | 0.5 A | 0.5 A | 0.5 A |

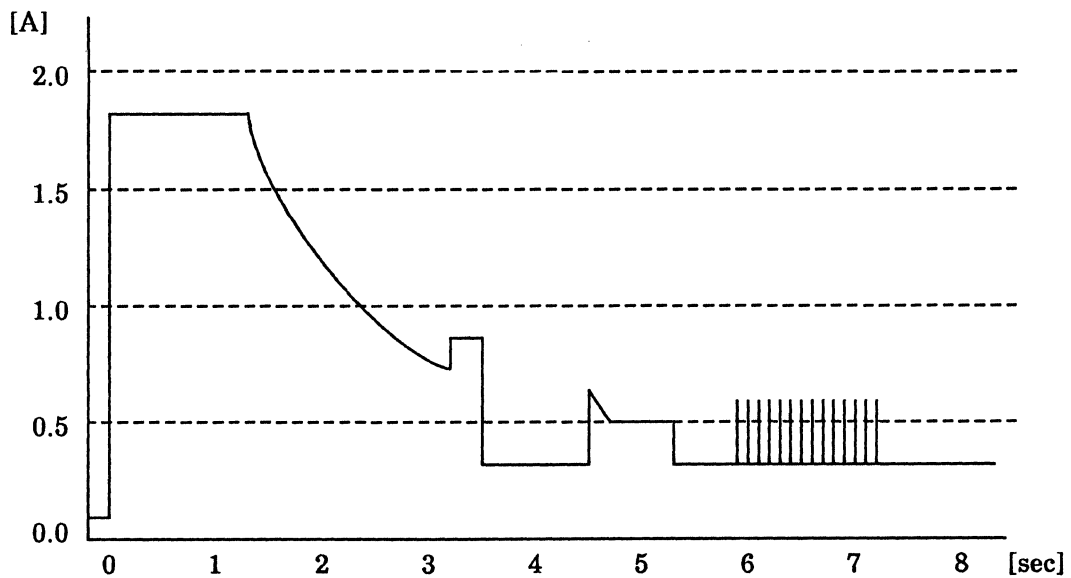
| | M2612ET/13ET/14ET | | |
|------|-------------------|--------|--------|
| | Seek | W/R | Ready |
| +12V | 0.3 A | 0.3 A | 0.3 A |
| +5V | 0.56 A | 0.56 A | 0.56 A |

(6) +12V Start Current (Typ.)

① M2611T



② M2612ET/13ET/14ET



(7) **Power on/off sequence**

The +5 V and +12 V power supplies are monitored by the voltage check circuit. The circuit allows a write current to flow only when both voltages are normal. Accordingly, no power sequence is required. This is for protection of the content of the medium.

However, in case the supply of +12V is after +5V, the delay time of +12V should be less than about 3 seconds.

If not, the drive regards it as abnormal and sets the diagnostic code in the error register. This code is X '02' means "The controller is abnormal".

1.6 Reliability

(1) **Mean time between failures (MTBF)**

The MTBF of the IDD during its life time is estimated at 50,000 hours. The MTBF is defined as follows:

$$MTBF = \frac{\text{Operating time}}{\text{Number of equipment failures in the field}}$$

Operating time is the total time duration during which the power is on, excluding preventive maintenance.

Failure of the equipment means a failure that requires repair, adjustment, or replacement, excluding preventive maintenance. Errors by the operator, failures due to power failures, controller faults, cable faults, bad environmental conditions, or other failures not caused by the equipment itself are not included.

(2) **Mean time to repair (MTTR)**

MTTR is the average time taken by a well-trained service engineer to diagnose and repair a unit malfunction. The IDD is designed for an MTTR of 30 minutes or less.

(3) **Service life**

Overhaul of the drive is not required for the first five years or 20,000 hours.

(4) **Data protection at power failure**

Integrity of the data on the disk is guaranteed against all forms of abnormal DC power except a power failure during writing.

1.7 Error Rate

Errors detected upon initialization and replaced by an alternate record are not included in the error rate.

(1) Non-recoverable error rate

Errors which cannot be recovered within 16 retries should not exceed 10 errors per 10^{15} bits.

(2) Seek error rate

The rate of seek errors recoverable by one retry should be 10 or less per 10^7 seeks.

1.8 Media Defect

When a physical track contains two or more bad sectors, all sectors in the track are given BAD flags in formatting before the M261xET is shipped. It is called "bad track" (see Section 6.2).

As regards media defect, it defines with number of bad tracks as follows. (provided that CYL0 is defect free)

Number of bad tracks per drive : 12 max (M2611T)
 24 max (M2612ET)
 36 max (M2613ET)
 48 max (M2614ET)

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CHAPTER 2 CONFIGURATION

2.1 Mechanical Configuration

2.2 Circuit Configuration

2.3 System Configuration

2.1 Mechanical Configuration

The following figure shows the outer view of the IDD.

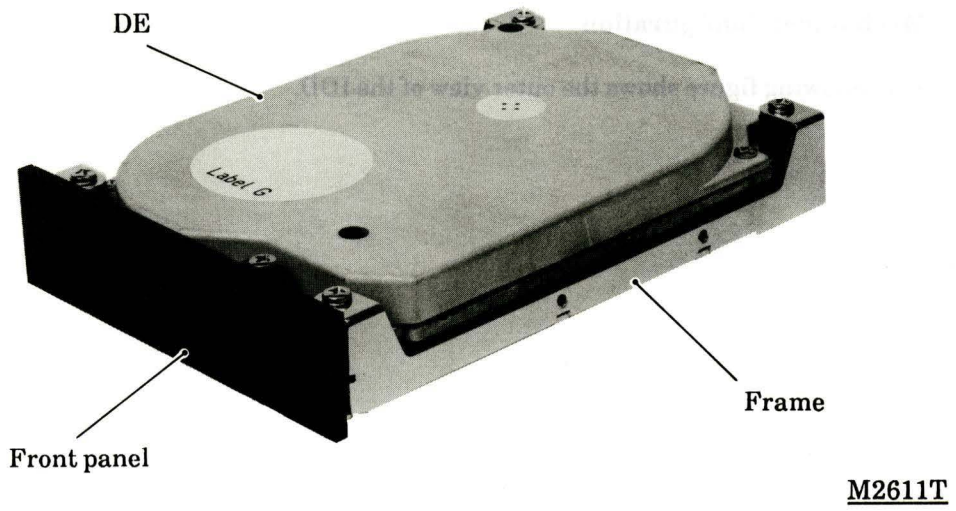
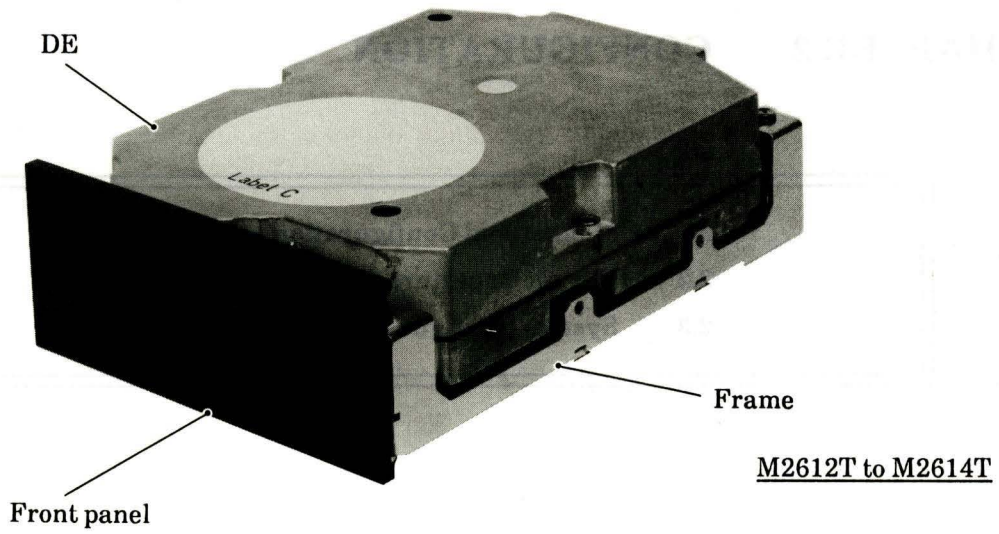


Figure 2.1 Outer view

(1) Disks

The disks have an outer diameter of 95 mm and inner diameter of 25 mm. They are sputtered storage media coated with a special lubricant. The M2611T uses one disk; the M2612ET, two; the M2613ET, three; and the M2614ET, four. The disks are good for at least 10,000 starts and stops.

(2) Heads

The heads are in contact with the disks when the disks are not moving, but automatically float when the rotation reaches the nominal speed. There are 2 read/write heads in the M2611T, 4 in the M2612ET, 6 in the M2613ET, and 8 in the M2614ET.

(3) Spindle motor

The disks are turned by a direct-drive DC motor. The motor attains a very precise rotational speed of 3490 rpm, $\pm 0.5\%$. This precision is achieved through a feedback circuit which includes Hall-effect elements mounted within the motor assembly.

(4) Actuator

The actuator consists of a rotary voice coil motor (VCM) and in-line type head actuator to achieve high-speed access. The actuator is controlled by electrical feedback from sector servo information read out through the head.

(5) Air circulation

Heads, disks, and actuator are sealed inside a cover to keep out dust. This head assembly has an air recirculation system using the blower effect of the rotating disks to continuously cycle air through the recirculation filter. This filter traps any dust generated inside the enclosure.

To prevent dust from entering due to air going in and out in the enclosure, the breather filter is attached. This breather filter equalizes the internal air pressure with the atmospheric pressure; external air can enter only through this filter.

2.2 Circuit Configuration

Figure 2.2 shows the IDD circuit configuration.

(1) 2 microprocessors (MPU)

One microprocessor is installed in the controller section and another in the drive section in the PCA. The former is used for interface control and the latter mainly for servo control, which supports fine control.

(2) Controller circuit

Important functions are listed below :

a. PC-AT interface control

This block controls interfacing with the expansion bus of the host via a simple adaptor board.

b. 64-KB buffer

This block consists of three areas ; a 56-KB area as a lock-ahead cache, a 6-KB area to write, and a 2-KB area to download sequencer programs.

c. ECC mechanism

This block can perform 4- or 7-bit error check and correction (ECC) which is selectable by jumper setting.

d. Error recovery and self-diagnostic function

This block retries for recovery on detecting an error in the execution of a SEEK, READ, or WRITE command and also self-diagnostics the M261xET with the DIAGNOSTIC command.

e. Power saving circuit

The M261xET supports two power modes which are selectable by the POWER command: idle mode and power save mode. In the power save mode, power is supplied only to the controller circuit, the spindle motor circuit, and the drive control IC. Power to the other components is shut off by the power FET. Thus low power consumption is accomplished. In this mode, the spindle keeps rotating for hot restart.

(3) Read/write circuit

The 1/7 (RLL) system is used for high recording density.

- ① The read/write circuit is a single-chip circuit containing a VFO and an RLL modulation/demodulation circuit.
- ② The pulse detector consists of an AGC amplifier, a filter circuit, a differential circuit and a pulse shaper.
- ③ The equalizer circuit is connected to AGC circuit to improve the read margin.
- ④ The head IC circuit contains a write amplifier, read preamplifier, and a head selection circuit to improve the signal-to-noise ratio.

(4) Servo circuit

The positioning and speed is controlled by the closed loop servo method. The MPU fetches a position signal from the sector servo information on each disk through the ADC and executes all control items ; the control signal is sent from DAC to the VCM, which supports high-speed access and high-precision positioning.

(5) Spindle motor control circuit

This circuit controls the rotational speed by comparing the output frequency of the Hall elements in the motor with the standard frequency generated by the crystal oscillator, so the rotational variation is very low.

For optimum motor speed control, the control filter constant for the M2611T is different from that for the M2612ET, M2613ET and M2614ET.

(6) Sample hold circuit

This circuit holds sector servo information on the data surface of the disk. This circuit produces the difference between the odd and even signals on the data surface and send it to ADC. The drive MPV receives positional information from the ADC output.

(7) Drive control circuit

This circuit consists of a circuit for decoding cylinder information (which is written with gray code in sector servo information) and a circuit (ESDI) for interfacing with the controller section.

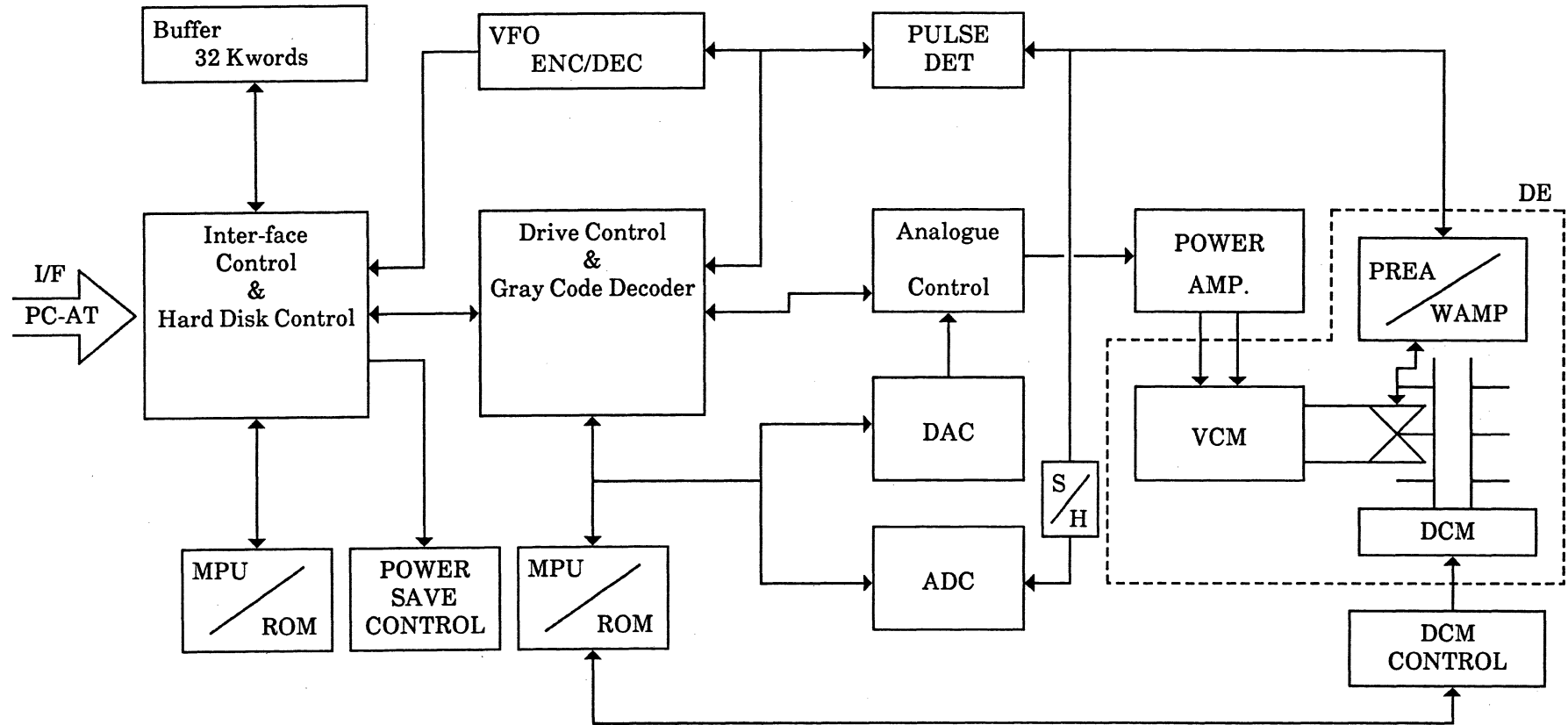


Figure 2.2 IDD circuit configuration

2.3 System Configuration

Figure 2.3 shows a system configuration example.

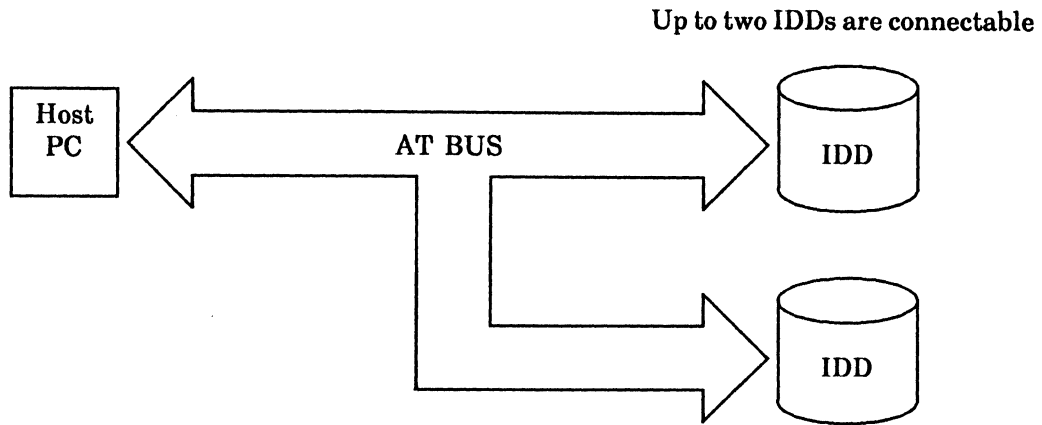


Figure 2.3 System configuration

Note:

In principle, perfect operation cannot be guaranteed in case of daisy-chained combination (2-drive system) of M261xET drive and other manufacturer's drive.

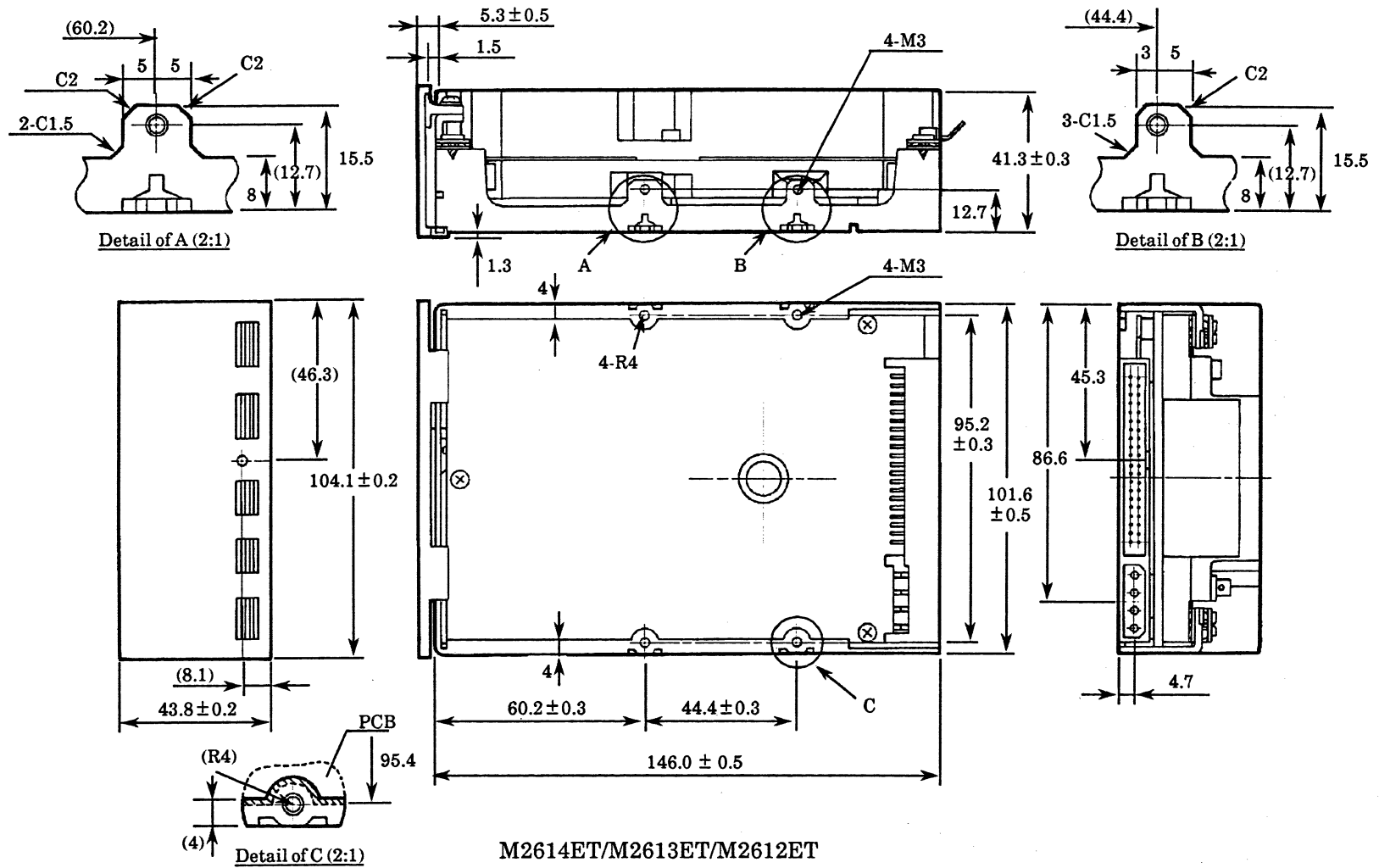
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CHAPTER 3 INSTALLATION

| | |
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| 3.1 | Outer Dimensions |
| 3.2 | Notes On Installation |
| 3.3 | Cable Connection |
| 3.4 | DC Grounding |
| 3.5 | Setting Switches |

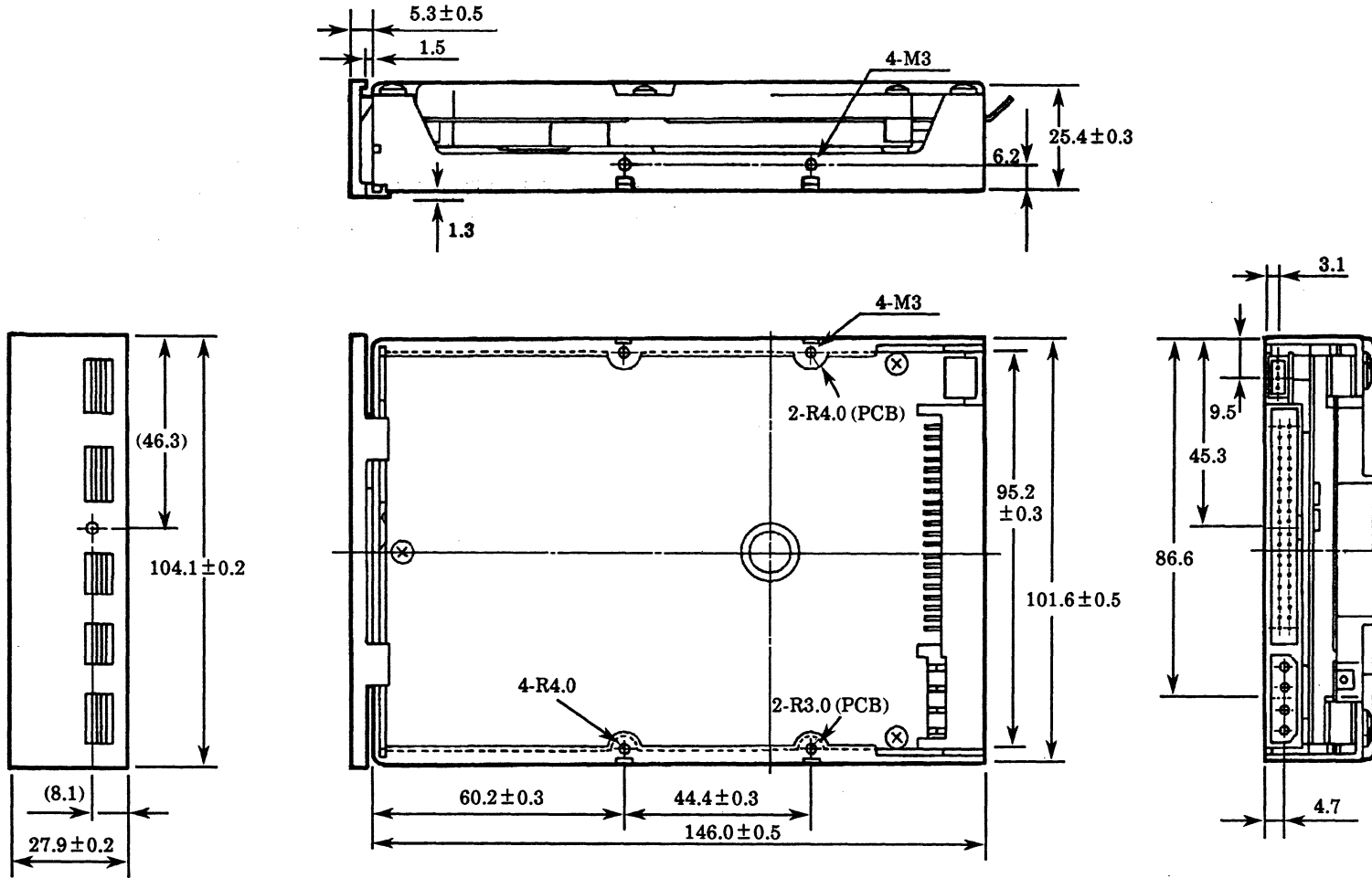
3.1 Outer Dimensions

Figure 3.1 shows the outer dimensions and mounting dimensions. All dimensions are in millimeters.
The front panel is optional.



M2614ET/M2613ET/M2612ET

Figure 3.1 Outer dimensions (1/2)



M2611T

Figure 3.1 Outer dimensions (2/2)

3.2 Notes On Installation

(1) Installation directions

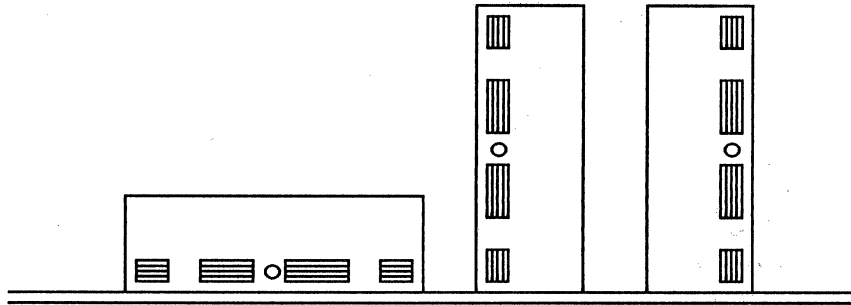


Figure 3.2 Installation directions

If the drive is installed in any of the above three installation directions, the level deviation must not exceed 5°.

(2) Frame structure

The disk enclosure is insulated from the frame by the rubber vibration isolators. The IDD can be installed in a system where the embossed structure is used for the frame.

To install the drive on an embossed frame, put the disk on the bottom.

If the disk is installed on the side, the frame type shown in the detail of B is used.

Note:

Different allowable values apply to the above two installation methods for screw projection distance and total length.

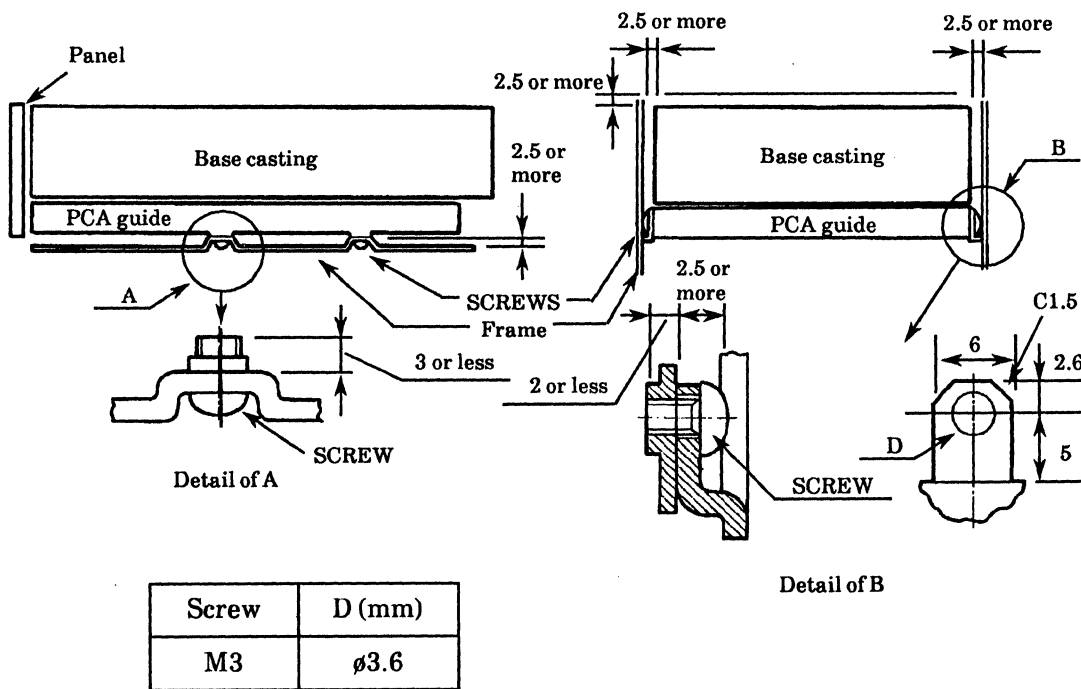


Figure 3.3 Frame structure

(3) Ambient temperature

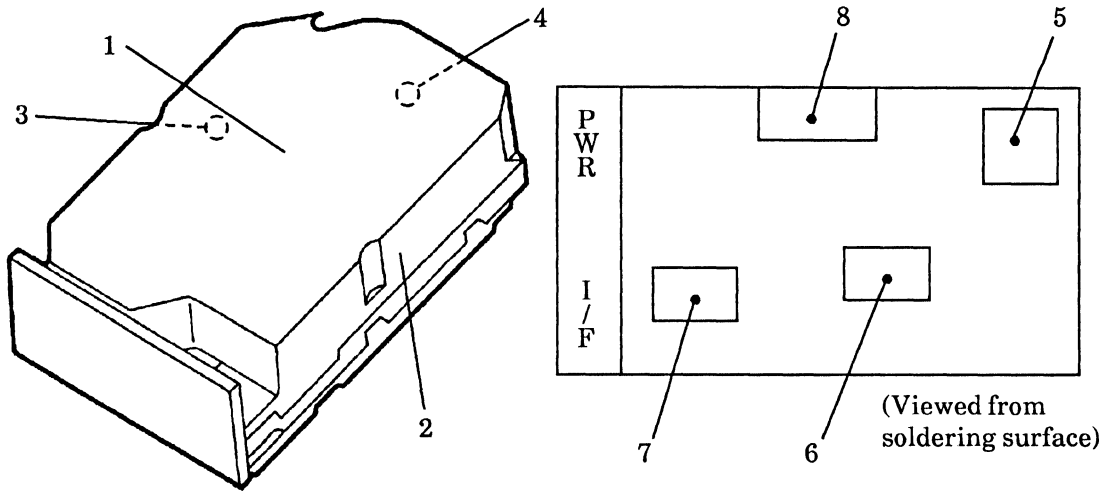
The operating temperature range for the IDD in a cabinet is specified at a distance of 3 cm from the IDD. Design the air flow in the cabinet to keep.

The maximum ambient temperature with in 45°C.

The air circulation in the cabinet must be designed so that the PCA side of the IDD is particularly cooled. The cooling effect should be confirmed in measuring the surface temperature of the specific IC and DE. These surface temperature should be in the specific value shown in the Table 3.1 in spite of any ambient temperature.

Table 3.1 Surface temperature specification

| Number | Specification |
|--------|---------------|
| 1 | 58°C |
| 2 | 58°C |
| 3 | 58°C |
| 4 | 58°C |
| 5 | 80°C |
| 6 | 70°C |
| 7 | 70°C |
| 8 | 80°C |



Notes:

- 1: On the center of the top
- 2: Right side (die-cast)
- 3: Left side (die-cast)
- 4: Back of the IDD (near connector)
- 5: IC CB0125 on the PCA
- 6: IC MB604516 on the PCA
- 7: IC MB84256 on the PCA
- 8: IC HA13441 (mounting side) on the PCA

Figure 3.4 The surface temperature measuring points

(4) Service area

Figure 3.5 shows the service area of the M261XET.

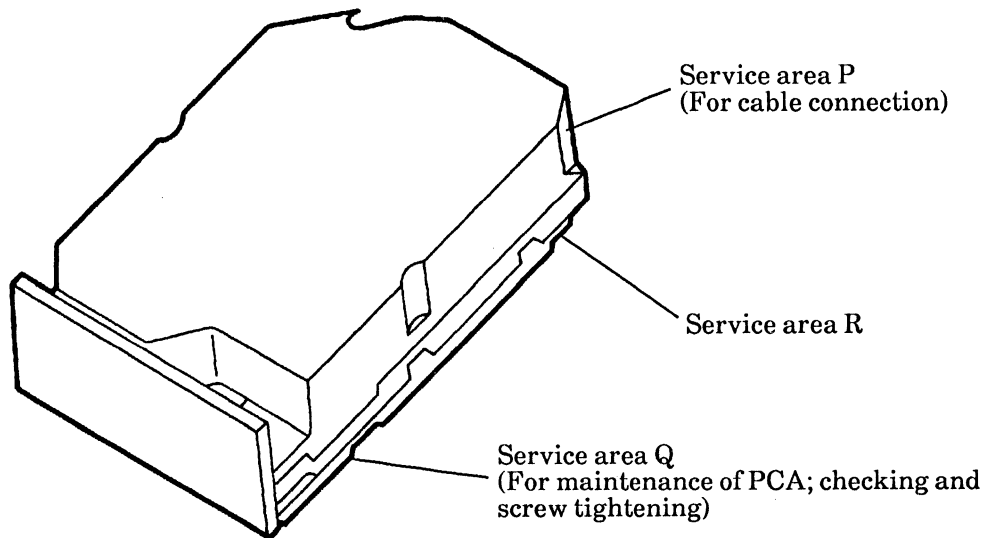


Figure 3.5 Service area

3.3 Cable Connection

3.3.1 Drive connector locations

Power connectors are arranged on the PCA on the lower surface of the drive as shown below:

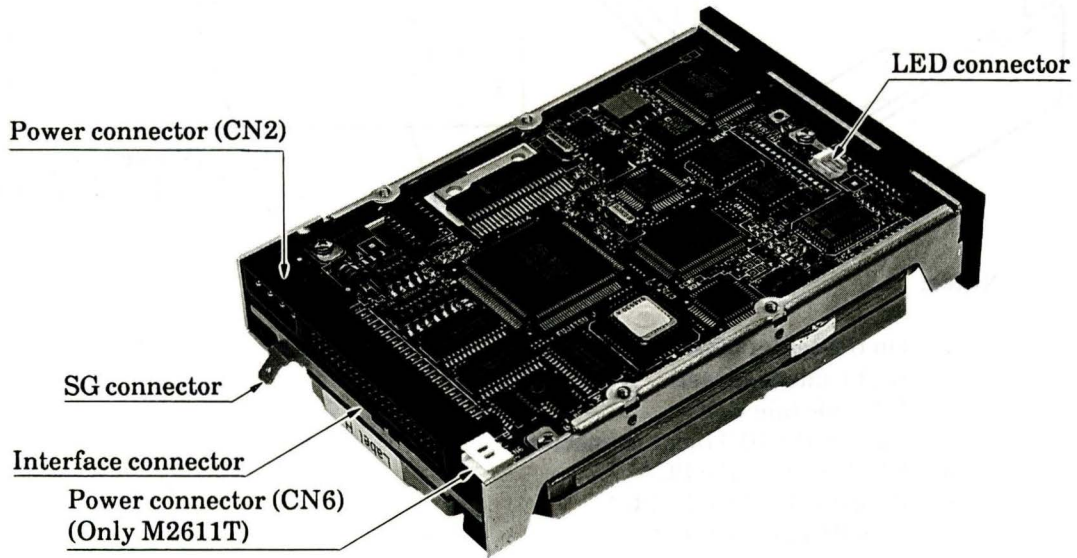


Figure 3.6 Connector locations

3.3.2 Cable and connector specifications

The following table lists recommended cables and connectors.

Table 3.2 Cables and connectors

| | Name | Part number | Manufacturer |
|--------------------------------------|------------------|--|---------------|
| Host Interface (40-Pin) (CNI) | Cable connector | FCN-707B040-AU/B (Closed end) or FCN-707B040-AU/O (Through end) | Fujitsu |
| | Drive connector | 87711-004 | DUPONT |
| | Cable | 445-248-40 | SPECTRA STRIP |
| Drive DC connector (CN1) | Cable connector | 1-480424-0 | AMP |
| | Contact | 170121-4 | AMP |
| | Drive connector | 87711-004 | DUPONT |
| | Cable | AWG 18~24 | |
| *1 Drive DC connector (CN6) | Cable connector | 39-01-0033 | MOLEX |
| | Contact | 39-00-0031 | MOLEX |
| | Drive connector | 39-27-6034 | MOLEX |
| | Cable | AWG 24 | |
| LED connector (CN7) | Cable connector | 608283302815000 | ELCO |
| | Contact | 608283052330808 (cable AWG24~30) 608283252330808 (cable AWG32) | ELCO |
| | Drive connector | 008283021100000 | ELCO |
| | Cable | AWG 24~30, AWG 32 | |
| FS-SG connector | Cable receptacle | 62187-1 | AMP |
| | Drive tab | 61761-2 | AMP |
| | Cable | AWG 20 | |

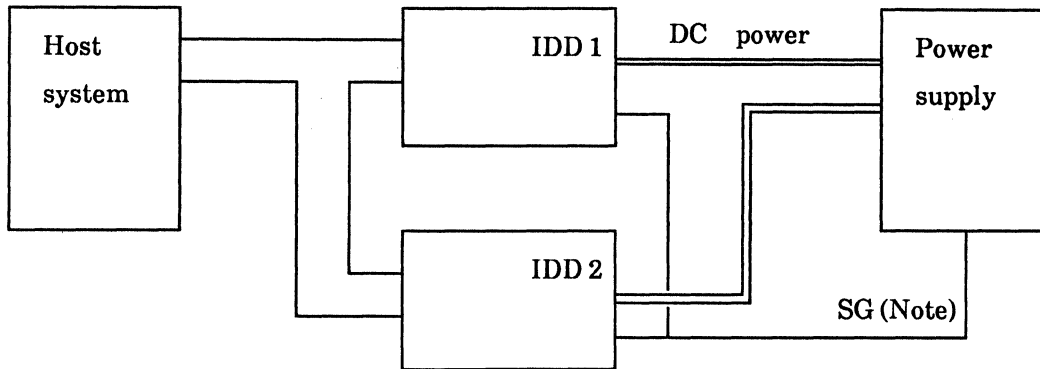
*1 ; Only M2611T provides CN6.

Note :

The cable of twisted pairs and neighboring line separated individually is not allowed to use for the host interface cable. It is because that the location of signal lines in these cables is not fixed, and so the problem on the crosstalk among signal lines may occur.

3.3.3 Connection of components

Figure 3.7 shows the cable connection. Figure 3.8 shows the power connector pin assignment.



Note :

The effect of SG connection varies according to host system. It needs evaluation on user's system.

Figure 3.7 Cable connection

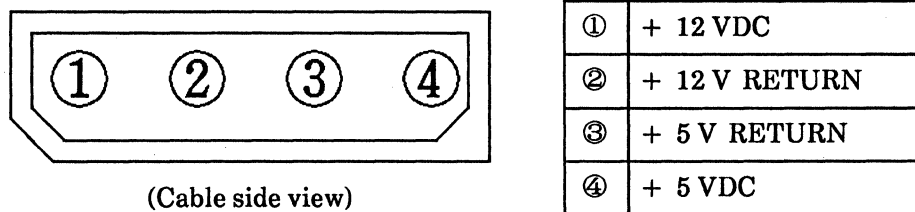


Figure 3.8.a Pin configuration of CN2

CN6 (Only M2611T)

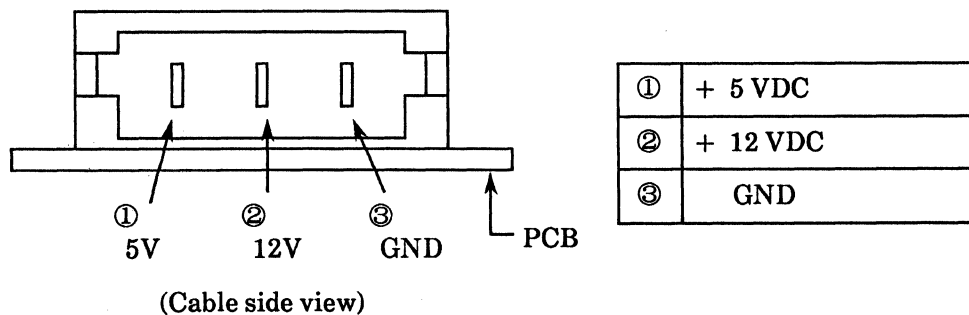


Figure 3.8.b Pin configuration of CN6

3.3.4 Option

The write protect switch is provided as an option.

See Figure 3.9.

3.4 DC Grounding

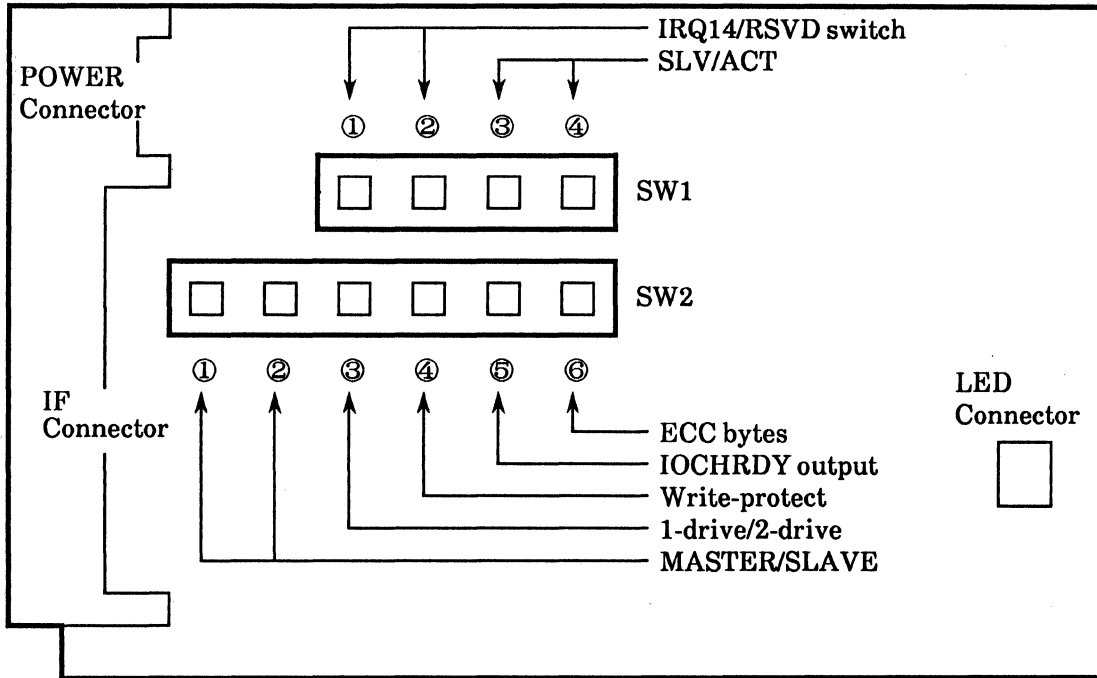
A Faston (quick-connect) terminal is provided as the SG connector for DC grounding.

See Figure 3.6.

3.5 Setting Switches

3.5.1 Switches locations

Figure 3.9 shows the switches locations. Standard setting at factory shipment conforms to this figure.



Note:

The content of this figure is subject to change without prior notice.

Figure 3.9 Switches locations

The standard setting at factory shipment conforms to Figure 3.10. It indicates that SW1 No. 1 is "ON", SW1 No. 2 is "OFF". Others are the same, too.

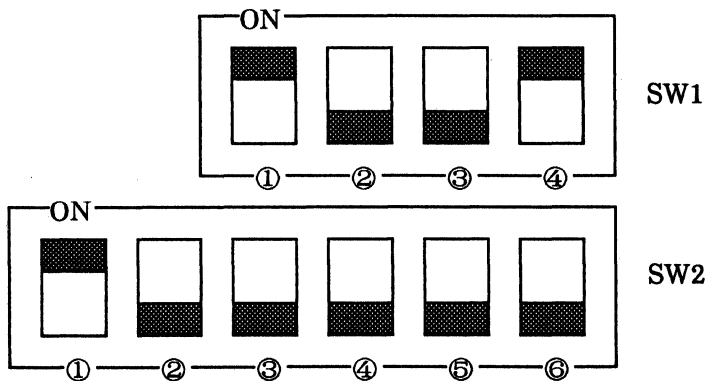


Figure 3.10 Setting switches

3.5.2 Mode settings

The items needed for setting are as follows.

(1) Drive system

① 1-drive/2-drive

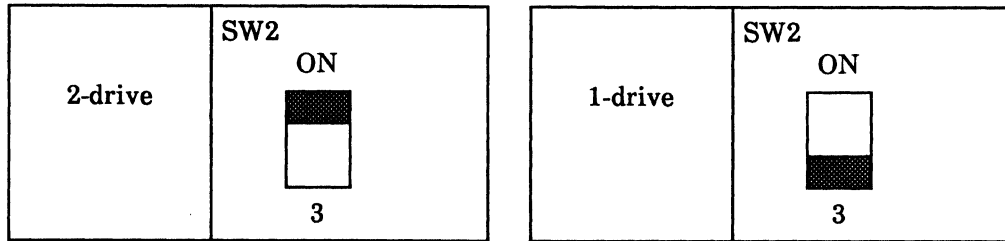


Figure 3.11 Drive system

② MASTER/SLAVE

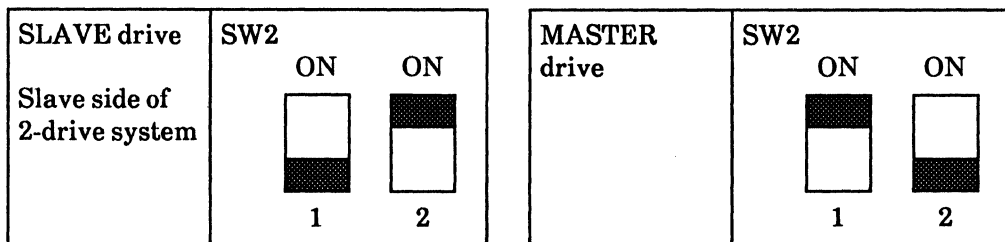


Figure 3.12 MASTER/SLAVE

(2) ECC bytes

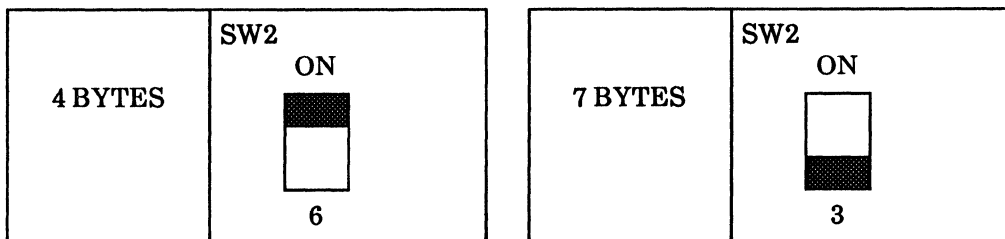


Figure 3.13 Setting of ECC bytes

In 4 BYTES ECC mode, the READ LONG/WRITE LONG command can be executed successfully only under the following conditions.

- READ LONG ⇒ WRITE LONG sequence is only acceptable.
- The Sector Number of READ LONG and WRITE LONG must be the same.
- The number of sector on WRITE LONG must be the same one that host issued to the drive on READ LONG.

(3) Write-protect

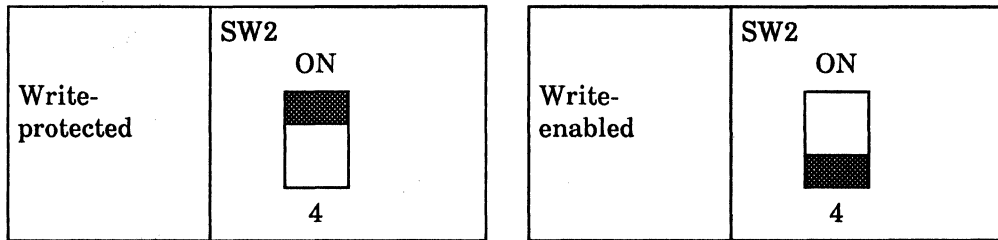


Figure 3.14 Setting of write-protect

(4) I/O channel ready (IOCHRDY) output

When the data transfer rate of the host becomes very high (near 3.7 MW/S or more), the M261xE^T must provide wait state to synchronize data transfer. This setting is used to output IOCHRDY to pin 27 of the host interface.

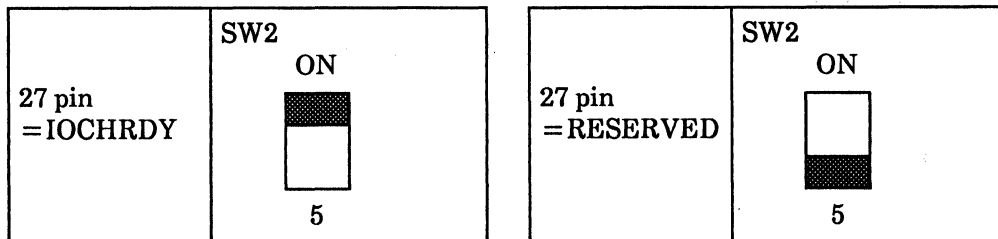


Figure 3.15 Setting of IOCHRDY

(5) IRQ14/RSVD switch

This operation is to exchange settings of pins 29 and 31 to eliminate crosstalk influence in the host interface cable.

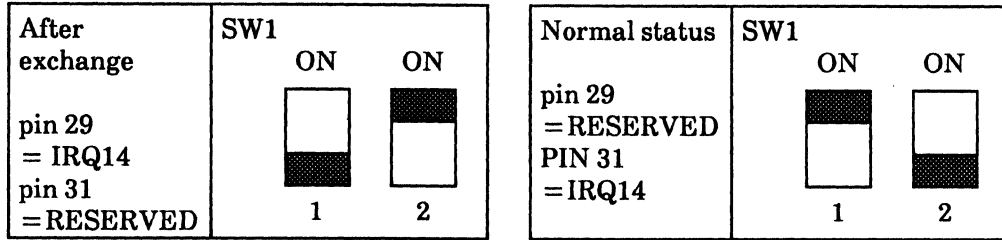


Figure 3.16 Exchange of IRQ14 and RSVD

(6) Slave present mode/Active mode

This operation is to set the slave present or active mode of the M261xET. This setting should be set in active mode on daisy-chained connection of both M261xET.

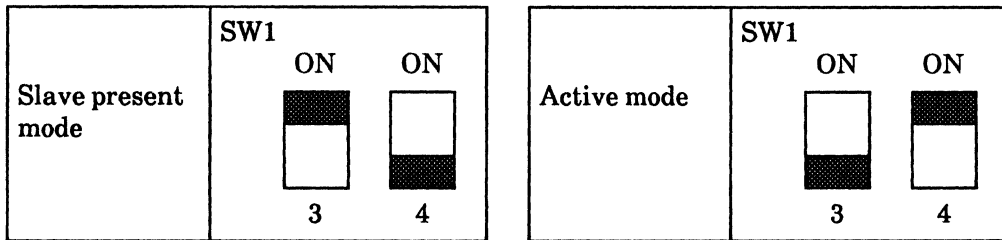


Figure 3.17 SLV/ACT setting

This plug should be set in "Active mode" on daisy - chained connection of both M261xET.

Note:

The logical information of setting plugs is subject to change without prior notice.

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CHAPTER 4 HOST INTERFACE

| | |
|-----|-----------------------|
| 4.1 | Terminology |
| 4.2 | System Configuration |
| 4.3 | Interface Signals |
| 4.4 | Task File Registers |
| 4.5 | Host Interface Timing |

4.1 Terminology

(1) PC-AT interface

This is the extended bus interface of IBM personal computers. The PC-AT interface supports a 16-bit data bus and a 24-bit address bus. However, the IDD uses, as address bits, five bits decoded by the adaptor board.

(2) Power save mode

In power save mode, power is supplied to the disk controller but not supplied to the disk to save power. (In this state, the spindle keeps on revolving.) This is low power consumption mode.

(3) Drive BIOS specification

The PC-AT BIOS specification (parameters such as the number of cylinders, the number of heads, and the numbers of sectors per track) is not always equal to the physical specification of the IDD.

The PC-AT BIOS does not support operation in the full range of the physical specifications of the IDD. To make the IDD work most efficiently according to its physical specification, the logical specifications should be converted in the controller. See Chapter 6 for details.

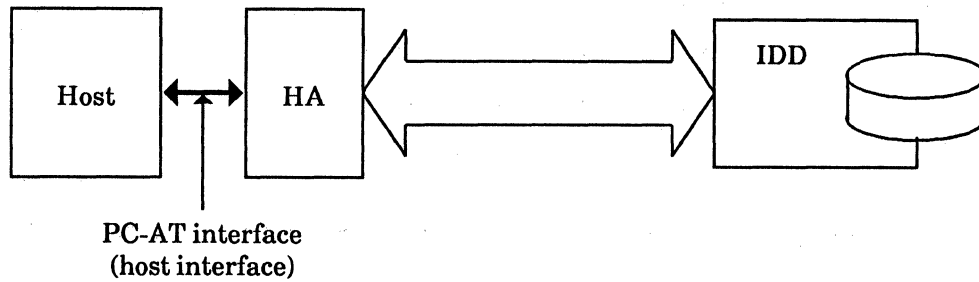
(4) Task file

The host treats the disk controller as a bidirectional I/O unit consisting of eight registers (called task file registers). The host controls these registers to control operation of the IDD.

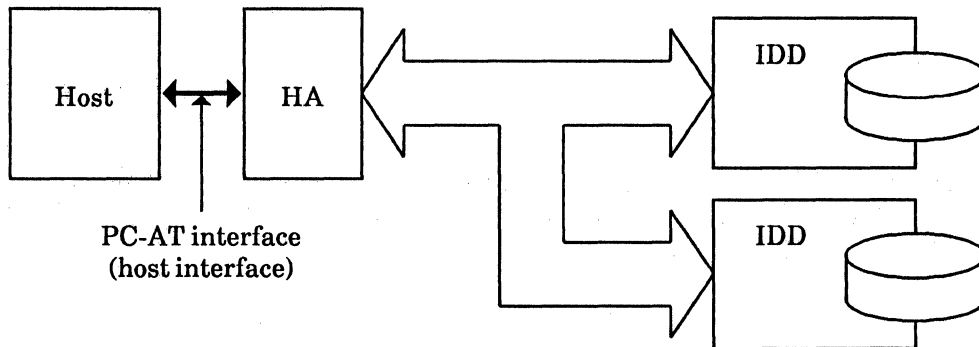
4.2 System Configuration

Figure 4.1 shows a system configuration example.

(1) One-drive connection



(2) Two-drive connection



HA indicates a host adapter, which consists of address decoder and driver/receiver (74LS244/245 or equivalent).

Figure 4.1 System configuration

4.3 Interface Signals

Figure 4.2 shows interface signal lines. Table 4.1 gives the connector pin assignments.

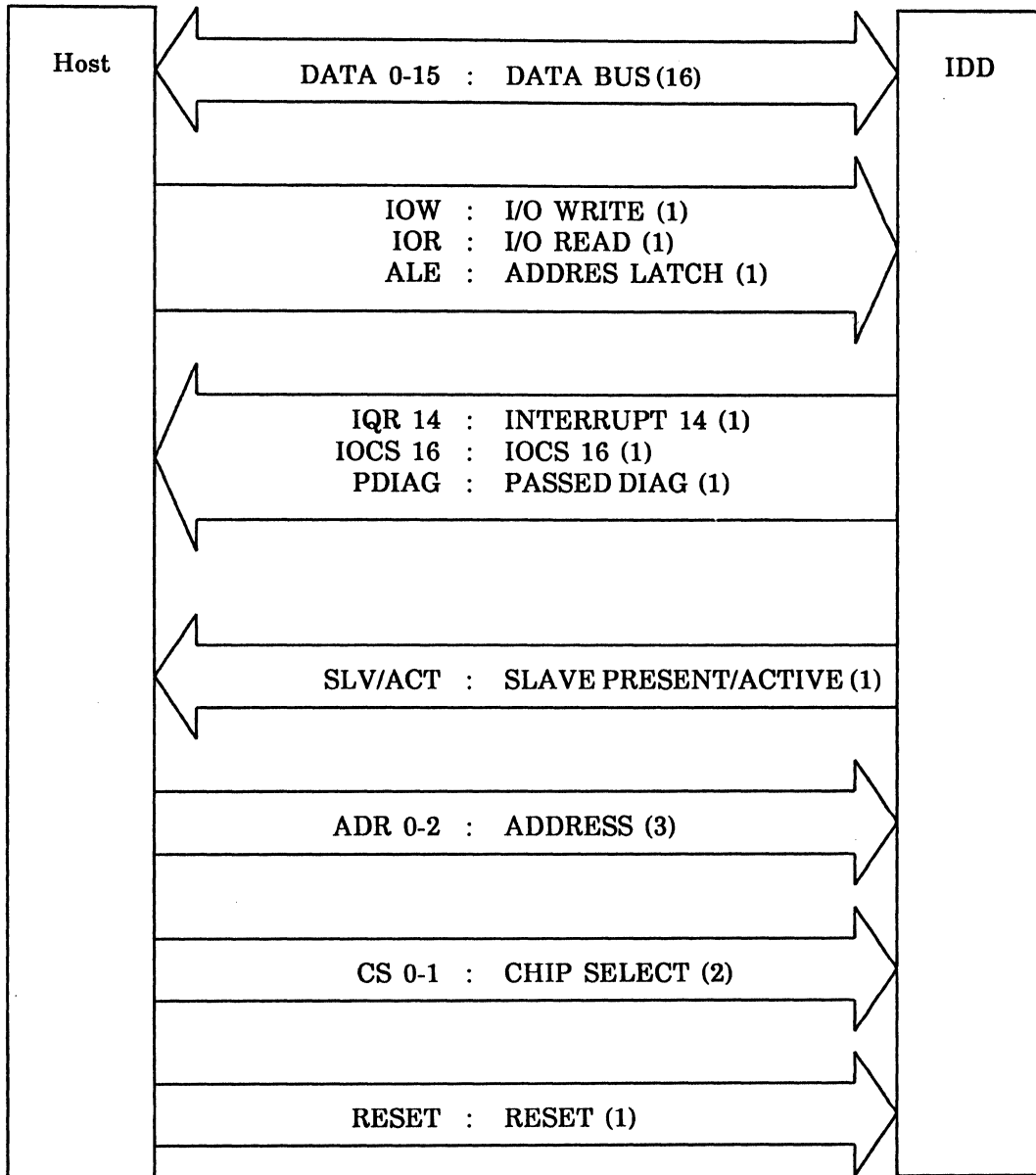


Figure 4.2 Host interface signals

Table 4.1 Connector pin assignments

| | | | |
|----|------------|----|----------|
| 1 | RESET- | 2 | GND |
| 3 | DATA 7 | 4 | DATA 8 |
| 5 | DATA 6 | 6 | DATA 9 |
| 7 | DATA 5 | 8 | DATA 10 |
| 9 | DATA 4 | 10 | DATA 11 |
| 11 | DATA 3 | 12 | DATA 12 |
| 13 | DATA 2 | 14 | DATA 13 |
| 15 | DATA 1 | 16 | DATA 14 |
| 17 | DATA 0 | 18 | DATA 15 |
| 19 | GND | 20 | KEY |
| 21 | RSVD | 22 | GND |
| 23 | IOW- | 24 | GND |
| 25 | IOR- | 26 | GND |
| 27 | RSVD *1 | 28 | ALE |
| 29 | RSVD *2 | 30 | GND |
| 31 | IRQ 14*2 | 32 | IOCS 16- |
| 33 | ADR 1 | 34 | PDIAG |
| 35 | ADR 0 | 36 | ADR 2 |
| 37 | CS 0- | 38 | CSI- |
| 39 | SLV- /ACT- | 40 | GND |

*1 Can be switched to IOCHRDY with jumper.

*2 Can be switched with jumper.

RSVD: Reserved

Explanation of signals

| [Signal Name] | [I/O] | [Explanation] |
|---------------|-------|---|
| RESET- | I | RESET signal from the host system which is active in low state. |
| DATA 0-15 | I/O | 16-bit bi-directional data bus used for data transfer between host and drive. $I_{OL} = 12\text{mA}$ |
| IOW- | I | WRITE strobe signal to set host data bus bits 0 to 15 in the drive register or data register at the rising edge. This signal is active in low state. |
| IOR- | I | READ strobe signal to send data from the drive register to data register A and to data 0 to 15 bus bits, in low state. |
| ALE | I | Address Latch Enable signal to activate the ADR signal in low state. |
| IRQ14 | O | Interrupt signal for the host system which is active in high state and reset when status data is read by the host system or the command is set. This signal is tri-state. $I_{OL} = 12\text{ mA}$ |
| IOCS16- | O | Active in low state to indicate that data is transferred in 16-bit units. This signal is output from the open collector. $I_{OL} = 12\text{ mA}$ |
| CS0- | I | CHIP SELECT signal obtained by decoding the host address bus. When this signal is in low state, the host can access registers X'1F0' to X'1F7'. |
| CS1- | I | CHIP SELECT signal obtained by decoding the host address bus. When this signal is in low state, the host can access registers X'3F6' , X'3F7'. |
| ADR 0-2 | I | Address signal to select the task file register. |
| KEY | - | Key to prevent connectors from being inserted incorrectly |
| PDIAG- | I/O | This signal operates as input in master drive and as output in slave drive. This signal indicates that DIAG in slave drive is passed successfully from the slave drive to the master drive. |
| SLV-/ACT- | O | This signal indicates that a second drive exists when SLAVE PRESENT mode is set by the jumper setting. This signal activates the drive access LED in ACTIVE mode. |
| IOCHRDY | O | This signal can be switched to RSVD assigned 27 pin by the jumper setting. When the data transfer rate becomes very high, near 3.7MW/s or more, this signal changes low state automatically and IDD demands a wait state of the HOST. |

Note:

“I” indicates the direction from host to drive, “O” indicates the direction from drive to host, and “I/O” indicates bidirectional transmission.

4.4 Task File Registers

The host task files can be specified as explained in the following table, according to the CS0-, CS1-, and ADR 0 to 2 signals.

| CS0- | CS1- | ADR 2 | ADR 1 | ADR 0 | TASK FILE REGISTER | | HOST I/O ADDRESS |
|------|------|-------|-------|-------|----------------------|---------------------|------------------|
| | | | | | READ | WRITE | |
| 0 | 1 | 0 | 0 | 0 | Data Register | Data Register | 1F0H |
| 0 | 1 | 0 | 0 | 1 | Error Register | Not Used | 1F1H |
| 0 | 1 | 0 | 1 | 0 | Sector Count | Sector Count | 1F2H |
| 0 | 1 | 0 | 1 | 1 | Sector Number | Sector Number | 1F3H |
| 0 | 1 | 1 | 0 | 0 | Cylinder Low | Cylinder Low | 1F4H |
| 0 | 1 | 1 | 0 | 1 | Cylinder High | Cylinder High | 1F5H |
| 0 | 1 | 1 | 1 | 0 | SDH Register | SDH Register | 1F6H |
| 0 | 1 | 1 | 1 | 1 | Status Register | Command Register | 1F7H |
| 1 | 0 | 1 | 1 | 0 | Alt. Status Register | Fixed Disk Register | 3F6H |
| 1 | 0 | 1 | 1 | 1 | Digi. Input Register | Not Used | 3F7H |
| 1 | 1 | × | × | × | No Operation | No Operation | — |
| 0 | 0 | × | × | × | Invalid address | Invalid address | — |

Notes:

1. The data register can be accessed in units of 16 bits for reading and writing.
2. Registers other than the data register can be accessed in units of 8 bits (data bits 0 to 7) for reading and writing.
3. When the digital input register is read, data bit 7 only enters the high impedance state.

4.4.1 Data register (1F0)

This 16-bit register is for data transfer between host and buffer using the read or write system command in programmed I/O (PIO) mode. However, when the R/W LONG command is executed to transfer the ECC bytes, only the low-order eight bits are used.

4.4.2 Error register (1F1)

This register holds the status of an executed instruction.

If the diagnostic mode is not set, this register is only valid if the error bit is set in the status register. If the diagnostic mode is set, this register is valid regardless of the contents of the status register.

** Diagnostic code **

- 01: The function is normal.
- 02: The controller is abnormal.
- 03: The sector buffer is abnormal.
- 04: The ECC device is abnormal.
- 05: The control CPU is abnormal.

In a 2-drive system, the error register on the master side is valid.

If an error is detected on the slave in this state, "80H" is ORed with the error and sent to the host.

** Status **

- Bit 0: The data address mark is not found (DATA AM NOT FOUND).
- Bit 1: The RESTORE command is executed but cylinder 0 cannot be detected.
- Bit 2: When the disk is not ready, Write Fault signal is detected, or the Seek Complete signal cannot be detected, the IDD aborted.
- Bit 3: Unused
- Bit 4: The target sector is not found (ID NOT FOUND).
- Bit 5: Unused
- Bit 6: An uncorrectable ECC error is detected in the data when the READ SECTOR command is executed (UNCORRECTABLE ECC ERROR).
- Bit 7: A bad block is detected.

4.4.3 Sector count register (1F2)

This register holds the number of sectors to be transferred according to the READ SECTOR or WRITE SECTOR instruction. 0 indicates that 256 is specified.

4.4.4 Sector number register (1F3)

This register holds the address of the starting sector to be processed by the instruction.

X '01' to '21' are valid.

4.4.5 Cylinder number register (1F4, 1F5)

This register holds the address of the starting cylinder to be processed by the instruction.

4.4.6 Drive/head register (1F6)

This register holds the unit address of the disk to be executed by the command and the access start head number in bit correspondence.

| | |
|-------|------------------------------------|
| bit 0 | HEAD 2 ⁰ |
| bit 1 | HEAD 2 ¹ |
| bit 2 | HEAD 2 ² |
| bit 3 | HEAD 2 ³ |
| bit 4 | 0: Disk drive 0 1: Disk drive 1 |
| bit 5 | Always set to 1 |
| bit 6 | Always set to 0 |
| bit 7 | Always set to 1 |

4.4.7 Status register (1F7)

Bit 7 BUSY

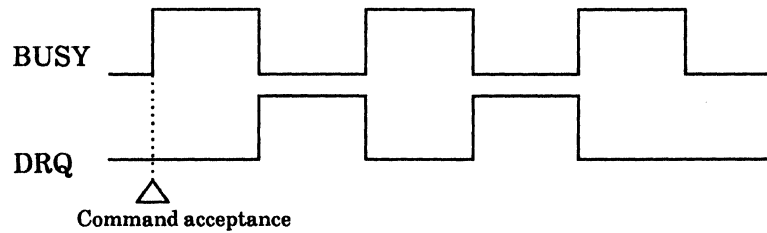
While this bit is set, the host cannot access the task file register.

This bit is set under the following conditions:

- ① The RESET signal becomes active or the SRST bit becomes 1 in the fixed disk register.
- ② The host writes data into the command register.

The relationship with the data request bit (DRQ) is as shown in Figure 4.3 during multi-sector reading or writing.

**** When the write system command is used to transfer two sectors ****



**** When the read system command is used to transfer two sectors ****

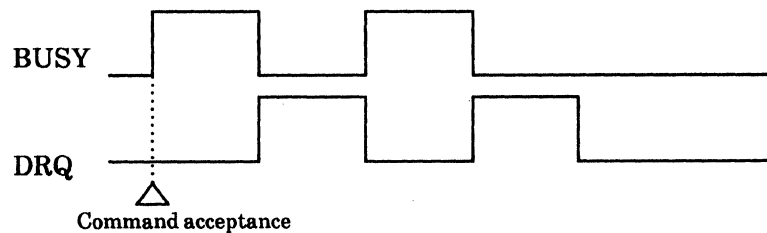


Figure 4.3 Timing of BUSY and DRQ

Bit 6 DRIVE READY

"1" = Indicates that the disk drive is usable.

Bit 5 WRITE FAULT

"1" = Indicates that the Write Fault signal is received from the disk.

Bit 4 COMMAND COMPLETE

"1" = The Command Complete signal from the disk is active.

Bit 3 DATA REQUEST

"1" = Indicates that the controller can transfer data for one sector to the host (DRQ).

Bit 2 CORRECTED DATA

"1" = A correctable ECC error occurs and data correction is done normally.

Bit 1 INDEX

"1" = INDEX pulse signal from the disk is active.

Bit 0 ERROR

"1" = Indicates that an error occurs when an instruction is executed.

4.4.8 Command register (1F7)

This register holds an instruction to be executed by the controller. The controller starts operation when a valid parameter is set and the instruction is specified in this register.

Table 4.2 COMMAND REGISTER

| COMMAND NAME | COMMAND CODE (Bit) | | | | | | | | PARAMETER USED | | | |
|-----------------|--------------------|---|---|---|---|---|---|---|----------------|----|----|-----|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | SC | SN | CY | SDH |
| RESTORE | 0 | 0 | 0 | 1 | × | × | × | × | N | N | N | D |
| SEEK | 0 | 1 | 1 | 1 | × | × | × | × | N | N | Y | Y |
| READ SECTORS | 0 | 0 | 1 | 0 | 0 | 0 | L | R | Y | Y | Y | Y |
| WRITE SECTORS | 0 | 0 | 1 | 1 | 0 | 0 | L | R | Y | Y | Y | Y |
| FORMAT TRACK | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | N | N | Y | Y |
| READ VERIFY | 0 | 1 | 0 | 0 | 0 | 0 | 0 | R | Y | Y | Y | Y |
| DIAGNOSTIC | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | N | N | N | D |
| SET PARAMETERS | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | Y | N | N | Y |
| WRITE STACK | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | N | N | N | D |
| READ STACK | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | N | N | N | D |
| READ PARAMETERS | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | N | N | N | D |
| POWER COMMAND | 1 | 1 | 1 | 0 | P | P | P | P | Y | N | N | D |

Here, symbols are:

L ; 1 = The READ LONG or WRITE LONG command is used, and data (256 words) and ECC (7B or 4B) are transferred with the host.
0 = Data is transferred with the host in units of 256 words.

R ; 1 = Retry is disabled.
0 = Retry is enabled.

SC ; SECTOR COUNT REGISTER (1F2H)
SN ; SECTOR NUMBER REGISTER (1F3H)
CY ; CYLINDER NUMBER REGISTER (1F4H, 1F5H)
SDH ; DRIVE/HEAD REGISTER (1F6H)

Y ; A valid parameter is specified for command execution.
The DRIVE and HEAD parameters must be specified for SDH.

N ; The register value is ignored for command execution.

D ; The DRIVE parameter is valid but the HEAD parameter is ignored.

P ; Indicates valid POWER command bits X 'E0' to 'E3' and 'E5'.

X ; Don't care

Command explanation

(1) RESTORE

This command moves the head to head position 0 on cylinder 0. When this command terminates, IRQ14 becomes active.

(2) SEEK

This command moves the head to the specified cylinder. When this command terminates, IRQ14 becomes active.

(3) READ SECTORS

This command moves the head to the specified cylinder and starts reading with the specified head and sector.

When at least 1 sector of data has been read and stored in the buffer RAM, host read transfer can be started by setting on the DRQ bit in the status register. If a data ECC error occurs during read, the error is automatically corrected and the corrected data is transferred to the host. If an uncorrectable error occurs, data in the sector is transferred to the host. Processing of subsequent sectors is halted, the locations of the cylinder, head, sector where the error occurred are saved in the host task file registers, and the processing terminates.

When the read operation is completed without an error, 0 is set in the sector count register and the termination positions are set in the other task file registers.

(4) WRITE SECTORS

This command moves the head to the specified cylinder and starts the write operation with the specified head and sector.

When this command is accepted, the DRQ bit is immediately set on in the status register and data transferred from the host is stored in the buffer RAM. When data for at least one sector is stored, the data is written to the drive.

When the write operation is completed without an error, 0 is set in the sector count register and the termination positions are set in the other task file registers.

(5) FORMAT TRACK

This command moves the head to the specified cylinder and formats with the specified head for one track. At this time, the host must specify the number of sectors per track in the sector count register. When this command is terminated, 0 is set in this register and IRQ14 becomes active.

The parameter for FORMAT is transferred as data for one sector. 2 bytes of parameter data are set for each sector and 66 bytes of data (33 sectors × 2) is set as the information for one track. Then, X '00' is set in the remaining 446 bytes and the parameter is transferred. The 2-bytes of sector information indicate a normal sector when X '00' is set in the first byte; it indicates a bad sector when X '80' is set. The byte following the X '80' indicates the sector number.

The following format is required for data transferred by this command.

(Example 1) When all sectors in the track are normal.

```
0001 0002 0003 ..... 001F 0020 0021 ← First 66 bytes
0000 0000 0000 ..... 0000 0000 0000 ← Remaining 446 bytes
```

(Example 2) When the second sector is a bad sector.

```
0001 8002 0003 ..... 001F 0020 0021 ← First 66 bytes
0000 0000 0000 ..... 0000 0000 0000 ← Remaining 446 bytes
```

(6) READ VERIFY

This command moves the head to the specified cylinder and starts the read operation with the specified head and sector in the same way as the READ SECTOR command.

This command differs from the READ SECTOR command in that this command does not transfer data to the host and the IRQ14 signal is set on when the command terminates.

If a data ECC error occurs in the read operation, the data is corrected and bit 2 (corrected data) is set on in the status register; if correction fails; bit 6 (uncorrectable ECC Error) is set on in the error register.

(7) DIAGNOSTIC

This command executes the internal self-test. The self-test execution results are set in the error register. In a 2-drive system, the execution results are sent from the master drive to the host together with the slave drive self-test results. When the master drive monitors the -PDIAG signal from the slave drive, if it detects -PDIAG=LOW within five seconds, it posts successful termination of the slave drive self test.

When this command terminates, the IRQ14 signal is set.

(8) SET PARAMETERS

This command is used by the host to define the maximum head number per track and the maximum number of sectors per track. The default values after power-on are 33 sectors per track and 4/8/12/16 heads per drive.

When this command terminates, the IRQ14 signal is set.

(9) WRITE STACK

This command is used by the host to write optional data into the drive buffer RAM. The IRQ14 signal is not set on when this command terminates.

(10) READ STACK

This command is used by the host to read optional data into the drive buffer RAM. The IRQ14 signal is not set on when this command terminates.

(11) READ PARAMETERS

This command is used by the host to obtain the drive parameter. When this command is issued, the drive parameter is prepared in the buffer RAM, the DRQ bit in the status register is set on, and the IRQ14 signal is set on. At this time, the host reads data for one sector from the drive.

Data format in the buffer RAM is shown below:

| | | VALUE (HEX) |
|---------------|--|---------------------|
| WORD 0 | GENERAL CONFIGURATION | 0a5a |
| WORD 1 | NUMBER OF FIXED CYLINDERS | 029b |
| WORD 2 | NUMBER OF REMOVABLE CYLINDERS | 0000 |
| WORD 3 | NUMBER OF HEADS | 0004/0008/000c/0010 |
| WORD 4 | NUMBER OF UNFORMATTED BYTES/PHYSICAL TRACK | 53f0 |
| WORD 5 | NUMBER OF UNFORMATTED BYTES/SECTOR | 0278 |
| WORD 6 | NUMBER OF PHYSICAL SECTORS/TRACK | 0021 |
| WORD 7 | NUMBER OF BYTES OF ISG | 0029 |
| WORD 8 | NUMBER OF BYTES OF PLO | 000c |
| WORD 9 | NUMBER OF WORDS OF VENDOR UNIQUE STATUS | 0000 |
| WORD 10 to 19 | SERIAL NUMBER | 0000 |
| WORD 20 | CONTROLLER TYPE | 0003 |
| | 0003 = DUAL PORTED, MULTI SECTOR BUFFER, CACHE | |
| WORD 21 | CONTROLLER BUFFER SIZE IN 512 BYTE INCREMENTS | 007e |
| WORD 22 | NUMBER OF ECC BYTES TRANSFERRED ON LONG OPERATIONS | 0007 |
| WORD 23 to 26 | CONTROLLER FIRMWARE REVISION (8 ASCII CHAR.) | (*1) |
| WORD 27 to 46 | CONTROLLER MODEL NUMBER (40 ASCII CHAR.) | (*2) |
| WORD 47 | NUMBER OF SECTORS/INTERRUPT | 0001 |
| WORD 48 | DOUBLE WORD TRANSFER FLAG | 0000 |
| | 0 = NOT CAPABLE, 1 = CAPABLE | |
| WORD to 255 | RESERVED | 0000 |

*1: Controller Firmware Rev.: "WS-FT-XX"

*2: Controller model name: PB3-AT-10h + all zeros

or

PB3-AT-0Ch + all zeros

(12) POWER COMMANDS

a. Mode setting

This command enables the user to use the following five power mode commands (see Table 4.3):

Table 4.3 Power-related commands

| Command name | Command register bit | | | | | | | | Hex |
|--------------|----------------------|---|---|---|---|---|---|---|-----|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | E0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | E1 |
| 2 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | E2 |
| 3 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | E3 |
| 4 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | E5 |

Note:

The M261xET supports two power modes and is always in either of the modes. Its status is controlled by command 0 to command 4.

① Idle mode

In this mode, the M261xET is waiting for command input.

② Power save mode

In this mode, power to the drive control circuit is off but the spindle motor keeps rotating. The controller can accept a command in this state but takes 1 second maximum to answer.

b. Explanation of command 0 to command 4

① Command 0 (E0)

The drive is immediately set into Power save mode.

② Command 1 (E1)

The drive is immediately set into Idle mode.
Automatic power saving is reset.

③ Command 2 (E2)

The drive is immediately set into Power save mode.

Automatic power saving is enabled if a value other than 0 is set in the sector count register. If it will take effect when the drive returns to Idle mode.

Automatic power saving is disabled if 0 is set in the sector count register.

④ Command 3 (E3)

The drive is immediately set into Idle mode.

Automatic power saving is enabled if a value other than 0 is set in the sector count register ; if it will take effect when the drive returns to Idle mode.

Automatic power saving is disabled if 0 is set in the sector count register.

⑤ Command 4 (E5)

When this command is accepted in Idle mode, "FF" is set in the sector count register and processing terminates.

When this command is accepted in Power save mode, "00" is set in the sector count register and processing terminates.

Automatic power saving is a function to automatically switch the drive mode from Idle to Power save mode after a specified time elapses.

The specified time is defined as follows :

15 to 1,275 seconds (21.2 minutes), obtained by multiplying the sector count register value (X '01' to X 'FF') by 5. X'01' and X'02' are treated as X'03'.

c. Power command state shift diagram

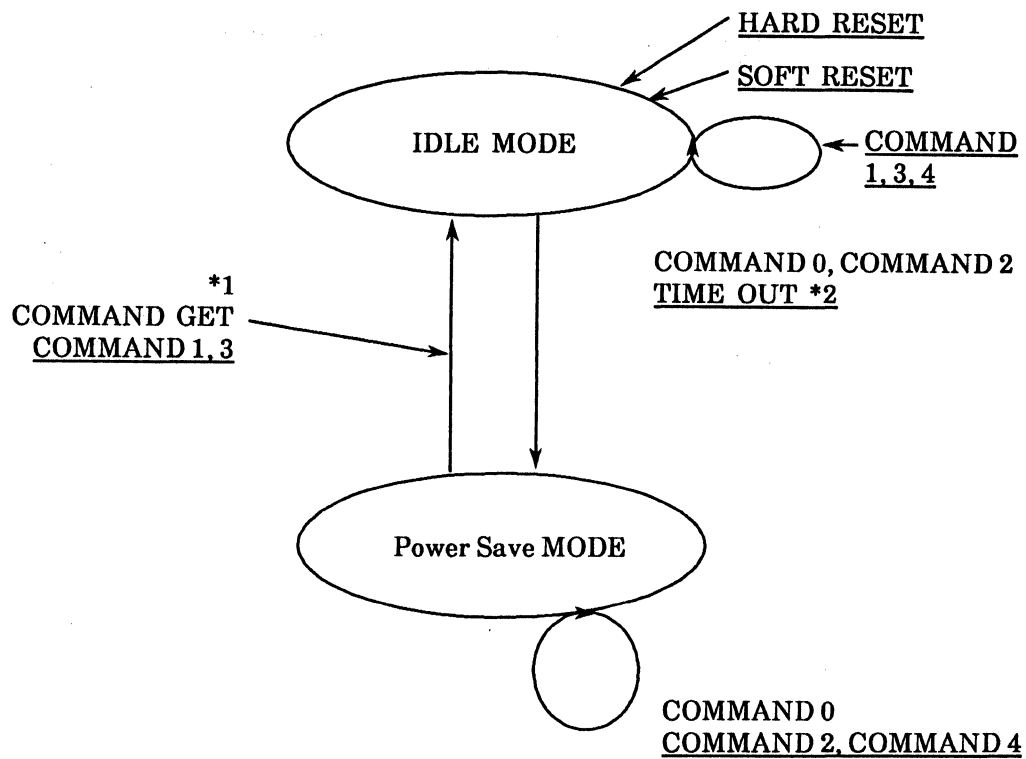


Figure 4.4 POWER COMMANDS

Note: COMMAND X indicates the power command.

*1 Acceptance of commands other than power commands is enabled

*2 Time-out in automatic power saving

4.4.9 Alternate status register

The same value as the content of the status register is stored in this register. This register differs from the status register in that when data is read from this register by the host, the IRQ14 signal is not reset.

4.4.10 Fixed disk register (3F6)

This register is used to set the disk IRQ14 and SOFT reset.

- Bit 7: Unused
- Bit 6: Unused
- Bit 5: Unused
- Bit 4: Unused
- Bit 3: Unused
- Bit 2: SOFT RESET
 - 1: Reset ON (All circuits remain reset while "1" is set here.)
 - 0: Reset OFF
- Bit 1: HARD DISK INTERRUPT DISABLE
 - 1: IRQ14 DISABLE (The IRQ signal is high-impedance.)
 - 0: IRQ14 ENABLE
- Bit 0: Unused

This register is cleared to X '00' when the hardware reset signal RESET becomes active.

4.4.11 Digital input register (3F7)

This register is used to select the head and drive.

- Bit 7: Undefined (high-impedance)
- Bit 6: WRITE GATE-
- Bit 5: HEAD SELECT 2^3 -
- Bit 4: HEAD SELECT 2^2 -
- Bit 3: HEAD SELECT 2^1 -
- Bit 2: HEAD SELECT 2^0 -
- Bit 1: DRIVE SELECT 1-
- Bit 0: DRIVE SELECT 0-

4.5 Host Interface Timing

The driver/receiver in IDD is 74LS244, 74LS245 or equivalent, and signal level is TTL compatible.

| Logic "1" | Logic "0" |
|-------------|---------------|
| 2.0 V (min) | 0.0 V – 0.7 V |

(1) Data writing: Data transfer from the host to the controller

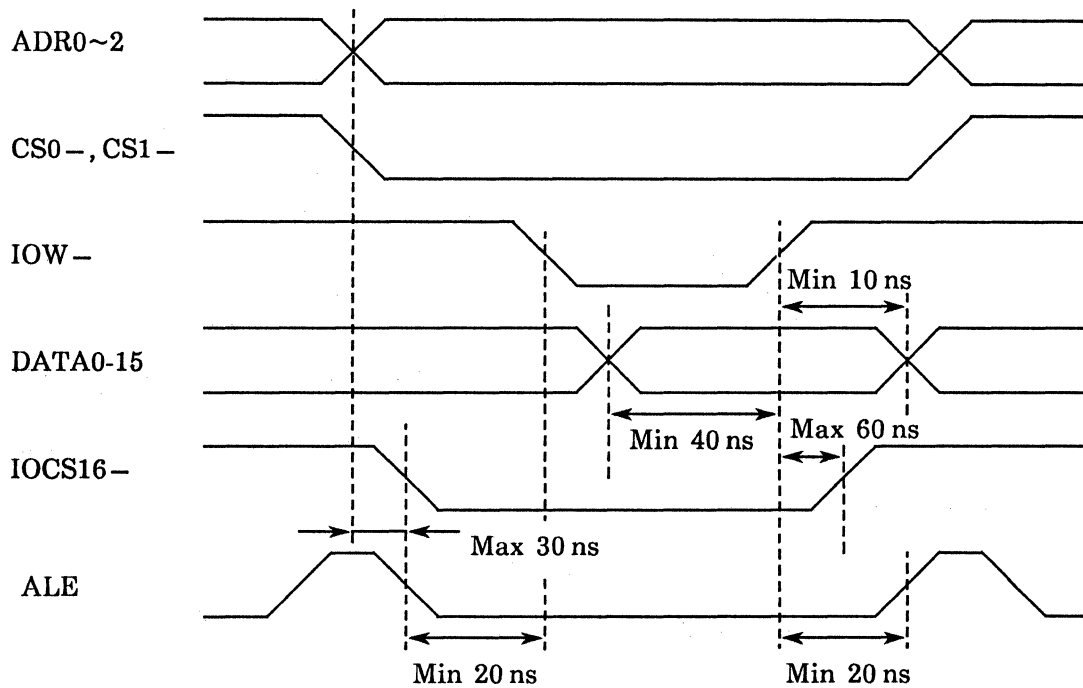


Figure 4.5 a Timing of data writing

Note:

The IOCS16- signal (data writing and data reading) is only generated when the data register is accessed.

(2) Data reading: Data transfer from the controller to the host

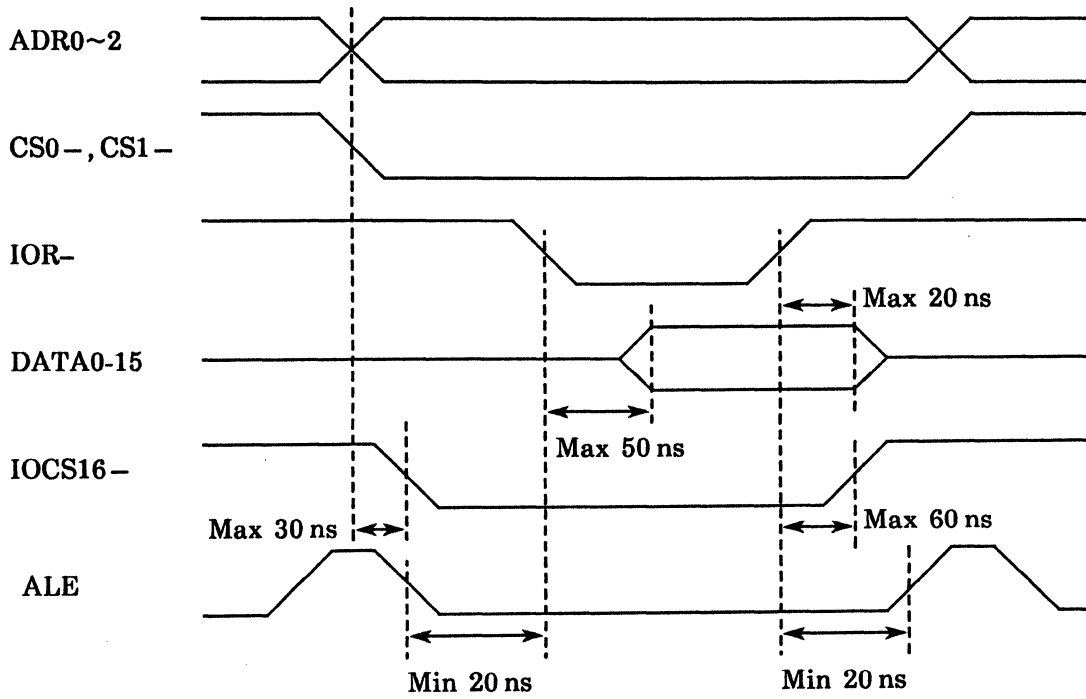
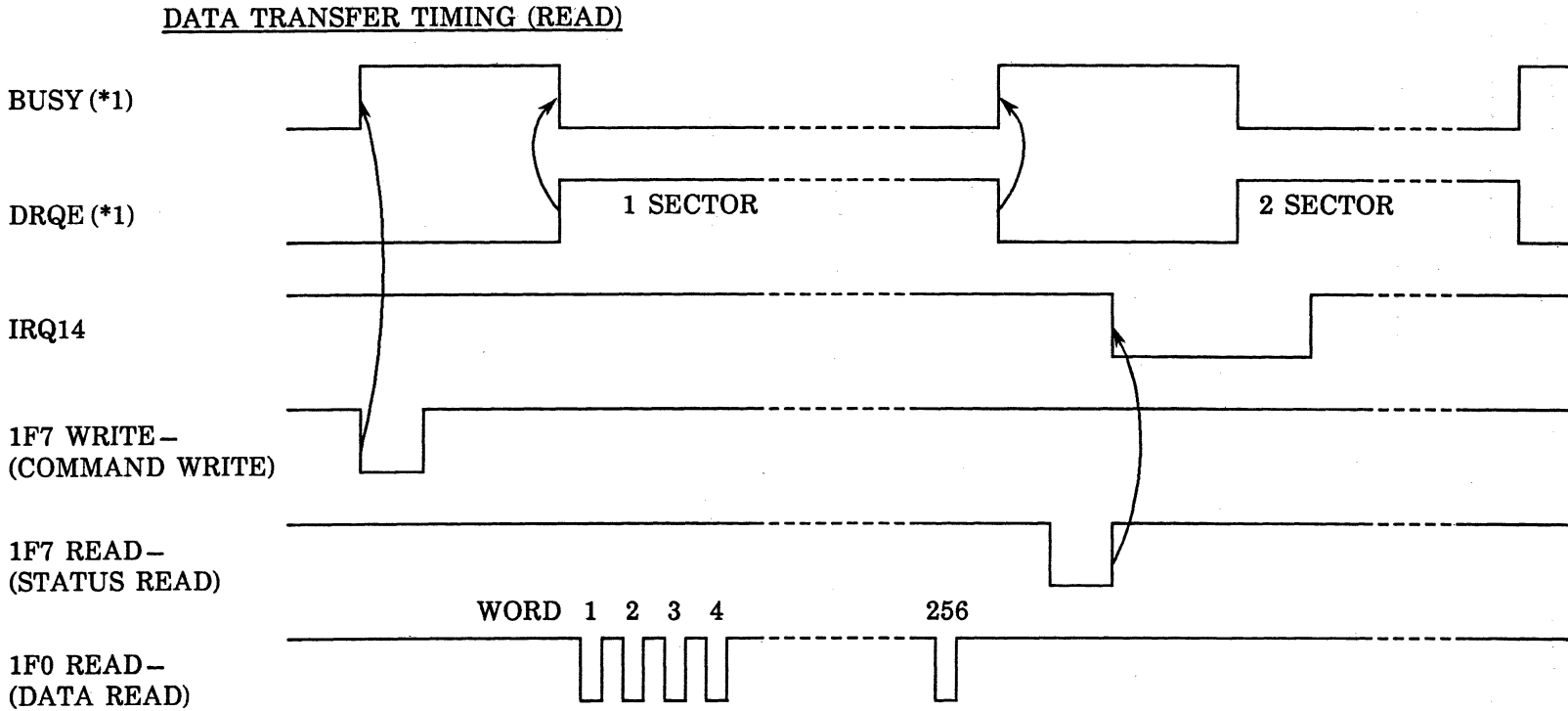


Figure 4.5 b Timing of data reading

Note:

The IOCS16- signal (data writing and data reading) is only generated when the data register is accessed.

For reference, it shows the case of IBM PC-AT BIOS.

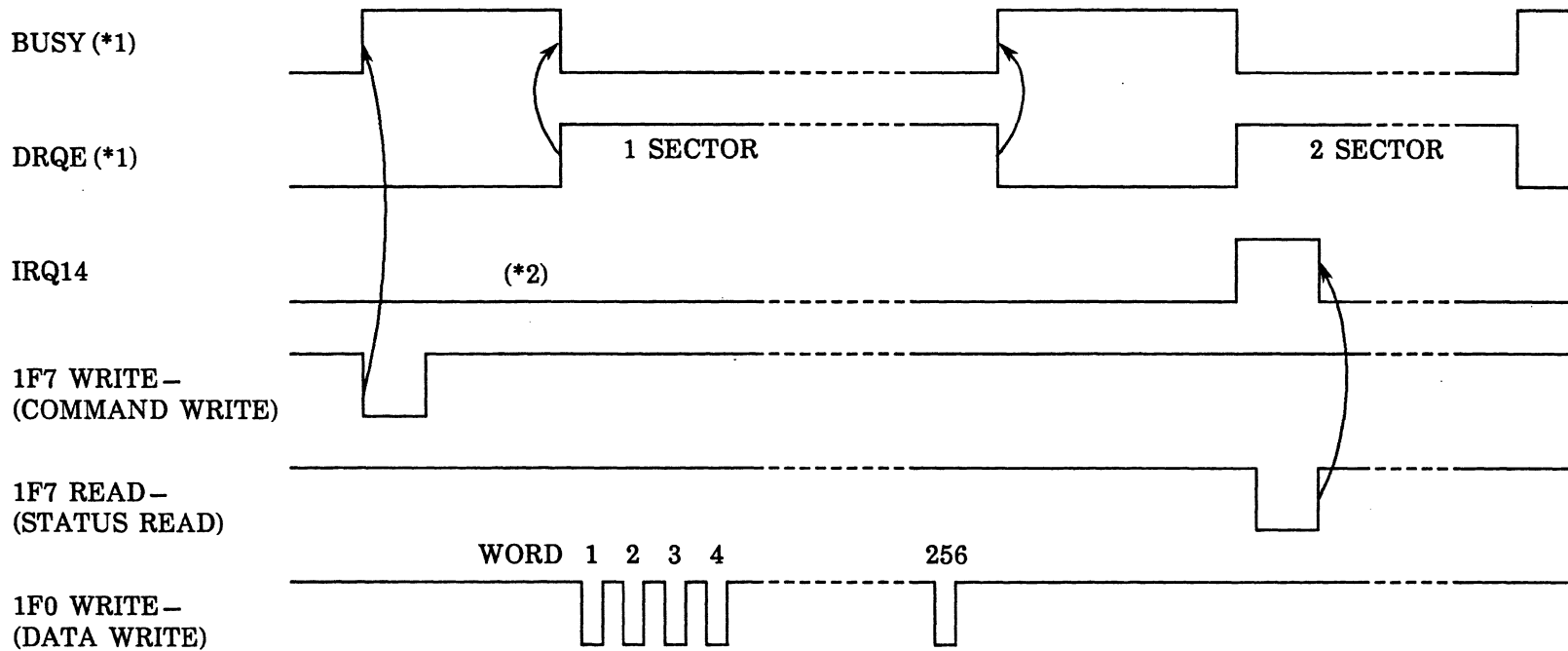


*1 BUSY and DRQ are bits in register X '1F7'.

Figure 4.6 Data transfer (READ)

For reference, it shows the case of IBM PC-AT BIOS.

DATA TRANSFER TIMING (WRITE)



*1 BUSY and DRQ are bits in register X '1F7'.

Figure 4.7 Data transfer (WRITE)

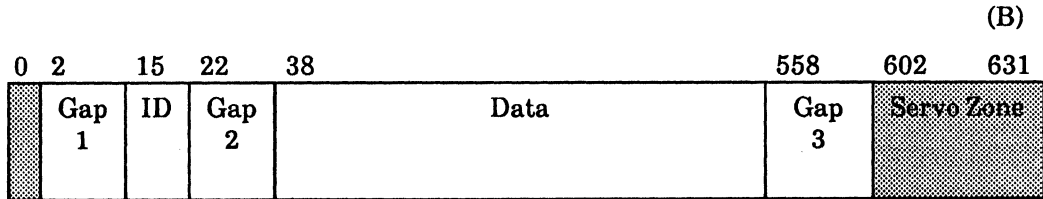
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CHAPTER 5 DATA FORMAT

| | |
|-----|--------------------|
| 5.1 | Sector Format |
| 5.2 | ID Field Structure |
| 5.3 | Cylinder Structure |
| 5.4 | User Area |
| 5.5 | CE cylinder |
| 5.6 | SA cylinder |
| 5.7 | Reformatting |

5.1 Sector Format

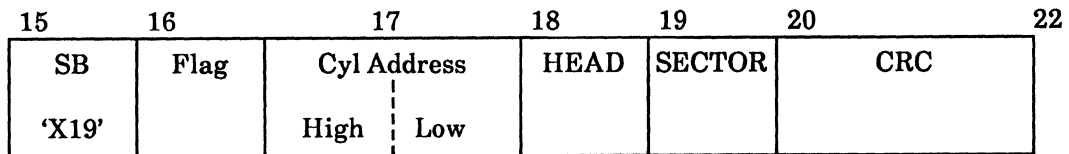
(1) 512 B/sector format



Gap1

Write splice (1B) + Sync (12B) = 13B

ID



Flag — { 0000 : Normal Sector
0001 : Bad Sector

Gap2

Pad (2B) + Write Splice (1B) + Sync (13B) = 16B

Data

| | | | |
|-------|--------|------|-----|
| 38 | 39 | 551 | 558 |
| SB | Data | ECC | |
| 'X19' | (512B) | (7B) | |

Gap3

Pad (2B) + Write Splice (1B) + Isg (41B) = 44B

Servo Zone

2B + 30B (Read/Write Protect)

5.2 ID Field Structure

5.2.1 ID field structure

The ID field is five bytes long. Table 5.1 gives the structure.

Table 5.1 ID field structure

| Byte | Bit | Name | Explanation | |
|------|----------|--------------|---------------|------------------|
| 0 | 7 | 0 | Reserved | |
| | 6 | 0 | | |
| | 5 | 0 | | |
| | 4 | FLAG | | |
| | 1 | 3 | 0 | Cylinder address |
| | | 2 | Cylinder 1024 | |
| | | 1 | Cylinder 512 | |
| | | 0 | Cylinder 256 | |
| 7 | | Cylinder 128 | | |
| 6 | | Cylinder 64 | | |
| 5 | | Cylinder 32 | | |
| 4 | | Cylinder 16 | | |
| 2 | 3 | Cylinder 8 | Head Number | |
| | 2 | Cylinder 4 | | |
| | 1 | Cylinder 2 | | |
| | 0 | Cylinder 1 | | |
| | 7 | 0 | | Reserved |
| | 6 | 0 | | |
| | 5 | 0 | | |
| | 4 | 0 | | |
| 3 | 3 | HEAD 8 | Sector Number | |
| | 2 | HEAD 4 | | |
| | 1 | HEAD 2 | | |
| | 0 | HEAD 1 | | |
| | 7 | 0 | | Sector Number |
| | 6 | 0 | | |
| | 5 | SECTOR 32 | | |
| | 4 | SECTOR 16 | | |
| 3 | SECTOR 8 | | | |
| 2 | SECTOR 4 | | | |
| 1 | SECTOR 2 | | | |
| 0 | SECTOR 1 | | | |

5.2.2 ECC and CRC

(1) CRC

This 2-byte code is to detect an error in the ID field. The generator polynomial and range of detection are shown below:

Polynomial: $P = X^{16} + X^{12} + X^5 + 1$
Initial value: 1 including SB pattern

Detection: 16-bit single burst maximum

(2) ECC

This 7-byte code is to detect and correct an error in the data field. The generator polynomial and range of detection and correction are shown below:

Polynomial: $P = X^{56} + X^{52} + X^{50} + X^{43} + X^{41} + X^{34} + X^{30} + X^{26} + X^{24} + X^8 + 1$
Initial value: 1 including SB pattern

Detection: 22-bit single burst maximum

Correction: 11 bits maximum

5.3 Cylinder Structure

The M261xET uses the device data storage area by dividing it into user area, CE cylinder area, and SA cylinder area as shown in Figure 5.1.

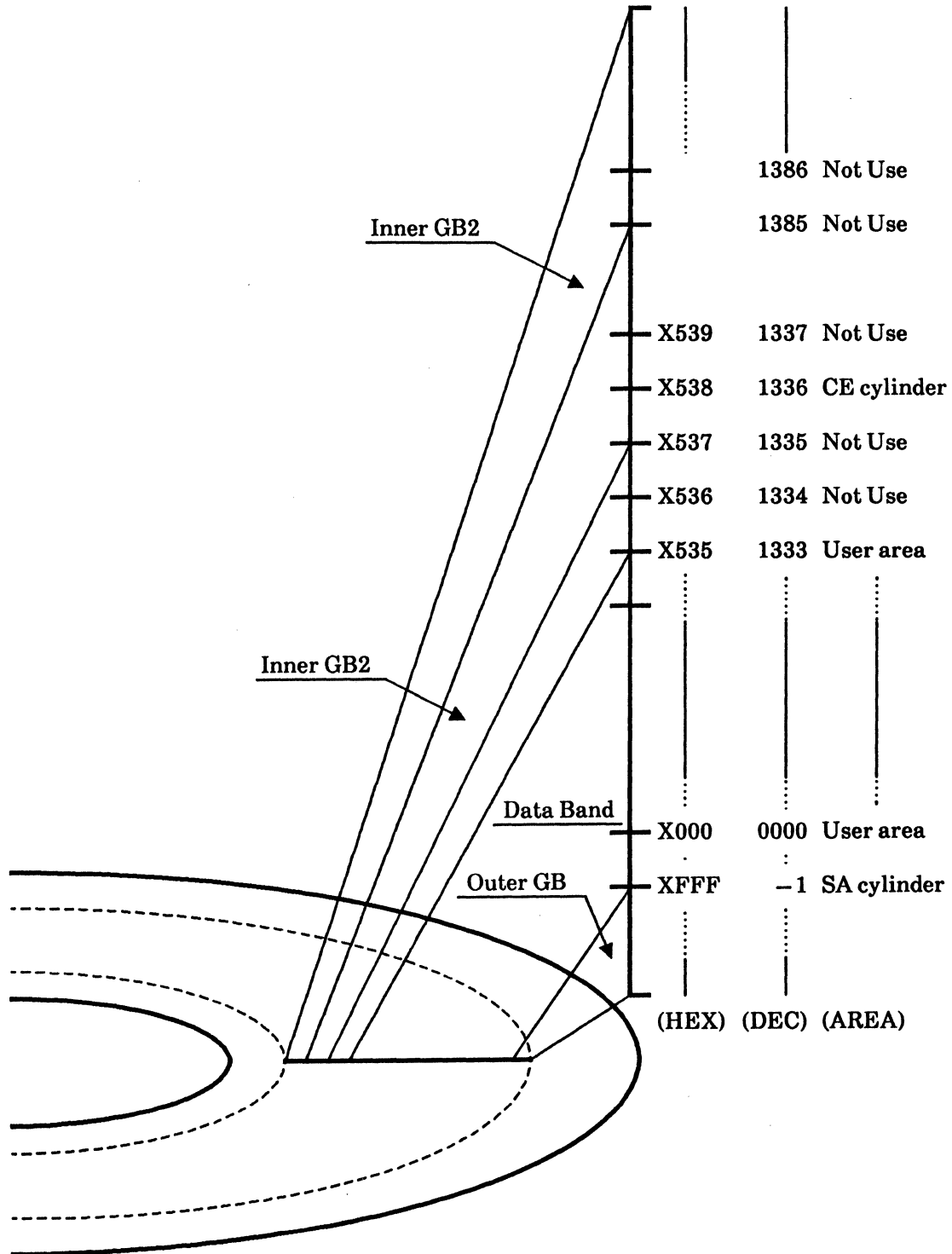


Figure 5.1 Cylinder construction

5.4 User Area

This area holds user data.

5.5 CE Cylinder

This area is used for diagnostics only. The format of this area is the same as that of the user area.

5.6 SA Cylinder

This area (512 bytes) is used mainly by the controller and contains the following information.

- 1) Defect map (primary list) which was factory-set

List of defect positions of the disk in four bytes.

- 2) System information

System information to be used by the controller

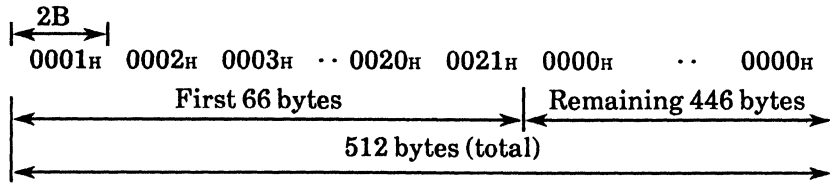
- 3) Factory information

Test and data information which were factory-set

5.7 Reformatting

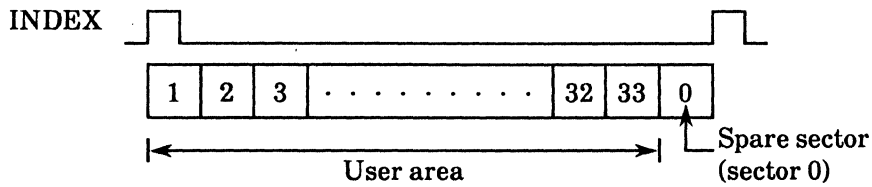
Disks can be reformatted by **FORMAT TRACK** commands. Take the following procedures to reformat :

- 1) Turn on the **POWER** switch (to cause the **AT** controller to read the primary defect list).
- 2) Transfer cylinder/head parameters.
- 3) Enter a **FORMAT TRACK** command.
- 4) Transfer format parameters (as data of one sector). The data is formatted as follows. See item (5) **FORMAT TRACK** in Subsection 4.3.8 for an explanation of the format parameters.



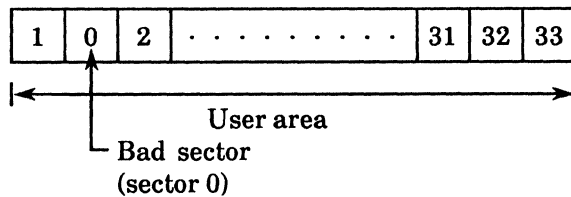
After receiving the above data, the AT controller adds it to the primary defect list which the AT controller read when the system was powered on. Track formatting varies according to the number of bad sectors per track.

a. No bad sector per track



b. 1 bad sector per track

: When the second sector is bad, the sector is skipped and the third sector is treated as sector 2.



c. 2 or more bad sectors per track

Alternate processing is not carried out. All sectors are treated as bad sectors.



Steps ① to ③ above are carried out considering track skew.

The end of the execution of the FORMAT TRACK command is indicated by the BUSY bit of the status register (FALSE).

5) Repeat steps 2) to 4) above on all cylinders and all heads.

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CHAPTER 6 OTHERS

| | |
|------------|---------------------------------------|
| 6.1 | BIOS Specifications of M261XET |
| 6.2 | Low Level Format |

6.1 BIOS Specifications of the M261XET

- (1) As BIOS has a limitation of number of cylinders (~ 1024), a host cannot be operated by physical parameters. Therefore, logical/physical translation (emulation) is needed, a host has to use M261XET by logical parameters. BIOS specifications are defined by "SET PARAMETERS" command which a host issues. A customer who can modify "FIXED DISK PARAMETER TABLE" in the BIOS selects parameter freely and can sets BIOS specification. However, the parameter must be selected within the storage capacity which M261XET has. And it is possible that customer uses M261XET by selecting appropriate DRIVE TYPE in the BIOS. In this case, M261XET works in the storage capacity which customers selected. Logical parameter which can use without loss of physical capacity of M261XET is shown in Table 6.1. Since "LOW LEVEL FORMAT" is performed with these parameters, whole data area of M261XET can be formatted. M261XET is formatted with BIOS specification which shows Table 6.1 at factory shipment.
- (2) When M261XET is operated by TEST PROGRAM (Bench Mark Test etc.) which is for measurement of the performance of HDD, according to BIOS specifications, actual performance may not be measured. For example, in BIOS specification shown in Table 6.1. Track to track seek (sequential seek) becomes 2 position seek. In M2611T or M261XET, example of BIOS specification that actual performance can measure and loss capacity least is shown following. However, the result of Bench Mark Test etc. and the performance of the actual use are not always equal. BIOS specification needs to decide that result of file access depending on systems is evaluated synthetic.

| | M2611T (Example 1) | M2611T (Example 2) | M2612ET |
|--|--------------------|--------------------|-------------------|
| Number of cylinders | 863 | 980 | 863 |
| Number of heads | 6 | 5 | 12 |
| Sector number/Track | 17 | 17 | 17 |
| Total storage capacity (Formatted) (loss sector) | 45.06 MB (18) | 42.64 MB (4744) | 90.13 MB (36) |

- (3) The parameter values (number of cylinders, number of heads, and number of sectors) specified by the host are converted by expressions listed in subsection 6.1.1.

Table 6.1 Logical parameter without loss

| M2611T 45 MB | | |
|---------------------|--------------------|-------------------|
| Type | Physical parameter | Logical parameter |
| Number of cylinders | 1334 | 667 |
| Number of heads | 2 | 4 |
| Sector per track | 33 | 33 |

| M2612ET 90.1 MB | | |
|---------------------|--------------------|-------------------|
| Type | Physical parameter | Logical parameter |
| Number of cylinders | 1334 | 667 |
| Number of heads | 4 | 8 |
| Sector per track | 33 | 33 |

| M2613ET 135.2 MB | | |
|---------------------|--------------------|-------------------|
| Type | Physical parameter | Logical parameter |
| Number of cylinders | 1334 | 667 |
| Number of heads | 6 | 12 |
| Sector per track | 33 | 33 |

| | | |
|---------------------|--------------------|-------------------|
| M2614ET 180.3 MB | | |
| Type | Physical parameter | Logical parameter |
| Number of cylinders | 1334 | 667 |
| Number of heads | 8 | 16 |
| Sector per track | 33 | 33 |

Initially (at power-on), each M261xET uses the values of the logical parameters as BIOS parameter values.

6.1.1 Address conversion

- 1) When the system is powered on, the controller CPU fetches physical specifications of the drive and computes the number of sectors per physical cylinder (①). Parameter symbols are explained below.

- Parameters which the host fetches from the M261xET at power-on
PHD Number of physical read/write heads of the M261xET
- Parameters to be defined by the SET PARAMETERS command
HDS Number of read/write heads + 1
SPT Sectors per track
- Parameters which the host sets in the execution of a command
LC Logical cylinder
LH Logical head
LS Logical sector
- Physical parameters after address conversion
PC Physical cylinder
PH Physical head
PS Physical sector

- 2) The number of sectors per physical cylinder (Y) is

$$Y = 33 \times \text{PHD} = \begin{matrix} 66 & (\text{for PHD}=2) \\ \text{or } 132 & (\text{for PHD}=4) \\ \text{or } 198 & (\text{for PHD}=6) \\ \text{or } 264 & (\text{for PHD}=8) \end{matrix} \dots\dots \textcircled{1}$$

- 3) When a SET PARAMETERS command is entered from the host, the following address conversion is performed :

$$X = \text{LC} \times \text{HDS} \times \text{SPT} + \text{LH} \times \text{SPT} + \text{LS} - 1 \dots\dots \textcircled{2}$$

and

$$\text{PC} = \text{INT} (X/Y) \dots\dots\dots \textcircled{3}$$

$$PH = \text{INT}[(X \bmod Y) / 33] \dots\dots\dots \textcircled{4}$$

$$PS = X \bmod 33 + 1 \dots\dots\dots \textcircled{5}$$

where

$$A \bmod B = A - B \times \text{INT}(A/B)$$

INT(C) Integer less than but closest to C (C if C is an integer)

4) An example of address conversion is shown below.

Assuming HDS=4, SPT=33, and PHD=2

| LC | LH | LS | | PC | PH | PS |
|-----|----|----|---|------|----|----|
| 0 | 0 | 1 | ⇒ | 0 | 0 | 1 |
| | ⋮ | | | | ⋮ | |
| 0 | 0 | 33 | ⇒ | 0 | 0 | 33 |
| 0 | 1 | 1 | ⇒ | 0 | 1 | 1 |
| | ⋮ | | | | ⋮ | |
| 0 | 1 | 33 | ⇒ | 0 | 1 | 33 |
| 0 | 2 | 1 | ⇒ | 1 | 0 | 1 |
| | ⋮ | | | | ⋮ | |
| 0 | 2 | 33 | ⇒ | 1 | 0 | 33 |
| 0 | 3 | 1 | ⇒ | 1 | 1 | 1 |
| | ⋮ | | | | ⋮ | |
| 0 | 3 | 33 | ⇒ | 1 | 1 | 33 |
| | ⋮ | | | | ⋮ | |
| 666 | 0 | 1 | ⇒ | 1332 | 0 | 1 |
| | ⋮ | | | | ⋮ | |
| 666 | 0 | 33 | ⇒ | 1332 | 0 | 33 |
| 666 | 1 | 1 | ⇒ | 1332 | 1 | 1 |
| | ⋮ | | | | ⋮ | |
| 666 | 1 | 33 | ⇒ | 1332 | 1 | 33 |
| 666 | 2 | 1 | ⇒ | 1333 | 0 | 1 |
| | ⋮ | | | | ⋮ | |
| 666 | 2 | 33 | ⇒ | 1333 | 0 | 33 |
| 666 | 3 | 1 | ⇒ | 1333 | 1 | 1 |
| | ⋮ | | | | ⋮ | |
| 666 | 3 | 33 | ⇒ | 1333 | 1 | 33 |

6.2 Low Level Format

Low-level formatting indicates physical disk formatting. Formatting by "FORMAT C: (or D:)/S" by a DOS command is termed high-level formatting.

6.2.1 Notes on execution of low-level formatting

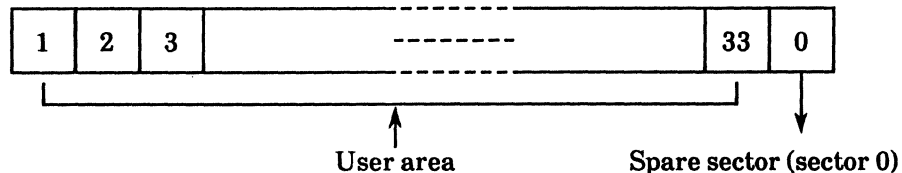
Use a FORMAT TRACK command for low-level formatting. The rules are as follows;

- 1) When a physical track contains only one bad sector, the sector is skipped in formatting. The skipped area is not visible to the host.
- 2) When a physical track contains two or more bad sectors, all sectors in the track are given BAD flags in formatting. The above two formatting operations are performed before the M261xET is shipped as 33 SECTOR/TRACK.
- 3) The track which is judged to be a bad track in the above operation cannot be made good by a FORMAT TRACK command.
- 4) It is possible to make a good track bad by a FORMAT TRACK command. It is also possible to make this bad track good again. Use a FORMAT TRACK command for a track whose sectors are all good or all bad.
- 5) Even when receiving a non-1 : 1 interleaving table from the host, the M261xET internally performs 1 : 1 formatting. This is because;
 - ① interleaving is not required as the look-ahead cache function performs high-speed data transfer at a place where hitting is made.
 - ② interleaving is substantially unnecessary since formatting (e. g. 17 sectors per track) is performed on two consecutive heads or cylinders.

6.2.2 Function of the controller section

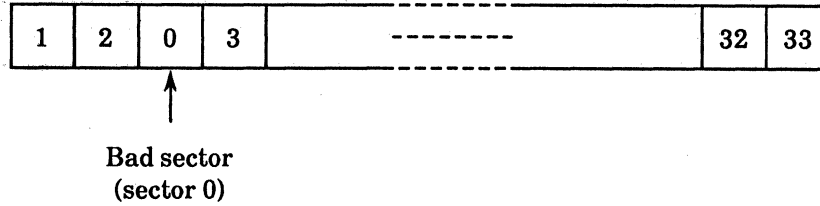
- 1) When the system is powered on, the controller reads the primary defect map from the SA cylinder of the drive and stores it in the work RAM.
- 2) When a FORMAT TRACK command is entered, the controller overlaps the parameter table sent from the host with the defect information of the target track.
- 3) When finding that a track has no bad sectors, the controller performs the following formatting :

1 : 1 interleaving

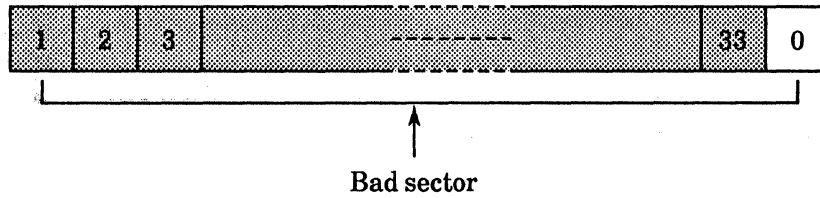


- 4) When finding that the track has one bad sector, the controller performs the following formatting, skipping the bad sector :

Assuming that the third sector is bad



- 5) When finding that the track has two or more bad sectors, the controller performs the following formatting, treating all sectors as bad sectors (without sector alternation) :



- 6) Steps 3) to 5) above are carried out considering track skew. Skew value is 6 ms (8 ms for M2611T) equivalent to 12 sectors (16 sectors for M2611T). No cylinder skew is used.

Comments concerning this manual can be directed to one of the following addresses:

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