HITACHI

ECL LOGIC AND MEMORY DATA BOOK

#LO3

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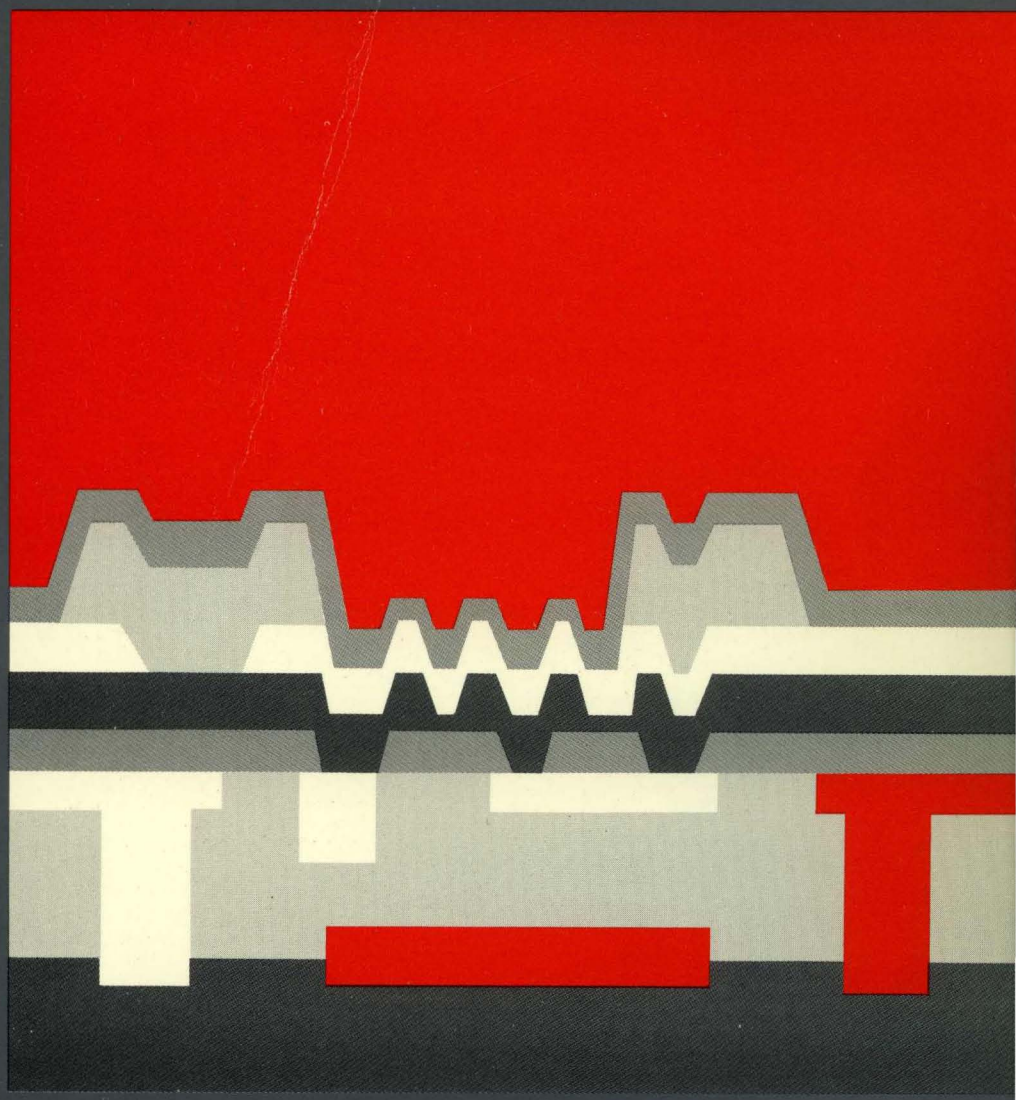

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CONTENTS

GENERAL INFORMATION

Two types of standard high-speed logic IC's typically meet today's computer system technology needs—Schottky TTL's and unsaturated ECL circuits. Schottky TTL logic circuits generally have the same circuit configuration and operating characteristics as standard TTL's. These saturated type circuits accumulate carrier electron charges in the transistor's Base region, due to the forward bias of B-E and B-C junctions during ON time. Discharge through the Collector during OFF time creates a storage time delay problem common to all saturated type logic circuits. TTL logic circuits featuring a Schottky diode clamp between Base and Collector eliminate storage time delay and improve saturation, but increase input capacitance, thus reducing system speed.

Non-saturated ECL circuits do not produce storage time delay, and provide features particularly advantageous in high-speed, low-noise system applications. Hitachi's HD10K series is compatible with Motorola's MECL 10K series, and the HD100K series is compatible with Fairchild's F100K series. In mass production at Hitachi, HD100K has three times the gate speed of HD10K, and is temperature and supply voltage compensated. New technologies have been applied to the HD100K series, such as 3μm lithography process and ion-implantation, which have resulted in high integration and frequency characteristics which greatly improve speed. Fig. 1 and Table 1 show characteristic comparisons among popular Bipolar digital IC families.

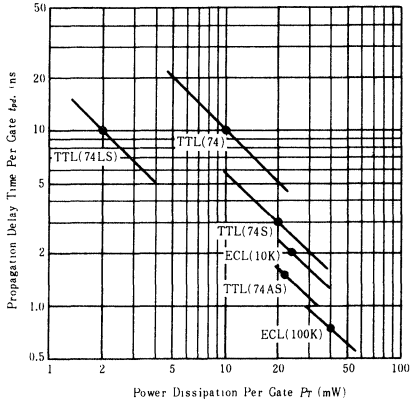


Fig. 1 Propagation Delay Time vs. Power Dissipation

Table 1. Comparisons of High-Speed Products

	HD100K	HD10K	HD74	HD74S	HD74LS
Propagation Delay Time	0.75ns	2ns	10ns	3ns	10ns
Power Dissipation	40mW	25mW	10mW	20mW	2mW
Speed-Power Product	30pJ	50pJ	100pJ	60pJ	20pJ

DEFINITIONS OF LETTER SYMBOLS AND ABBREVIATIONS

Symbol	Abbreviations
I_{EE}	Total power supply current drawn from a ECL test unit by the negative power supply
I_{CC}	Total power supply current drawn from the positive supply by a ECL unit under test
I_F	Forward diode current drawn from an input of a TTL-to-ECL translator when that input is at ground potential
I_{IH}	High level input current, into a node with a specified High level (V_{IH} max) logic voltage applied to that node
I_{IL}	Low level input current, into a node with a specified Low level (V_{IL} min) logic voltage applied to that node
I_{OH}	High level output current: the current flowing into the output, at a specified High level output voltage
I_{OL}	Low level output current: the current flowing into the output, at a specified Low level output voltage
I_{out}	Output current (from a device or circuit, under such conditions mentioned in context)
I_R	Reverse current drawn from a transistor input of a test unit when V_{EE} is applied at that input
I_{SC}	Short-circuit current drawn from a translator saturating output when that output is at ground potential
V_{BB}	Reference bias supply voltage
V_{CC1} (V_{CCA})	Most positive power supply voltage (output devices)
V_{CC2} (V_{CC})	Most positive power supply voltage (current switches and bias driver)
V_{EE}	Most negative power supply voltage for a circuit
V_{TT}	Line load-resistor terminating voltage for outputs from a ECL device
V_{in}	Input voltage (to a circuit or device)
V_{out}	Output voltage
V_{max}	Maximum (most positive) supply voltage, permitted under a specified set of conditions
V_{IH} max	Maximum High level input voltage: The most positive (least negative) value of high-level input voltage, for which operation of the logic element within specification limits is guaranteed
V_{IHA} min (V_{IH} min)	Minimum input logic High level (threshold) voltage for which performance is specified
V_{ILA} max (V_{IL} max)	Maximum input logic Low level (threshold) voltage for which performance is specified
V_{IL} min	Minimum Low level input voltage: The least positive (most negative) value of Low level input voltage for which operation of the logic element within specification limits is guaranteed
V_{OH} max	Maximum output High or high-level voltage for given inputs
V_{OH} min	Minimum output High or high-level voltage for given inputs
V_{OHA} (V_{OHC})	Output logic High threshold voltage level
V_{OLA} (V_{OLC})	Output logic Low threshold voltage level
V_{OL} max	Maximum output Low level voltage for given inputs
V_{OL} min	Minimum output Low level voltage for given inputs
t_{TLH}	Wave form rise time (Low to High)
t_{THL}	Wave form fall time (High to Low)
t_{PLH}, t_{PHL}	Propagation delay time, 50% to 50%
t_{su}	Set-up time of a flip-flop or counter device
t_h	Hold time of a flip-flop or counter device
f_{Tog}	Toggle frequency of a flip-flop or counter device

( ) : apply to the HD100K series only

HD10K GENERAL INFORMATION

■FEATURES

• Complementary outputs cause a function and its complement to appear simultaneously at device outputs, without use of external inverters. This reduces package count by eliminating the need for associated invert functions, and reduces system power requirements and timing differential problems introduced by inverters.

• High Input and Low Output impedances permit large fan-out and versatile drive characteristics.

• Insignificant Power Supply Noise Generation due to differential amplifier design eliminates current spikes even during signal transition period.

• Nearly Constant Power Supply Current Drain simplifies power supply design and reduces costs.

• Low Crosstalk due to low-current switching in signal path and voltage swing (typically 850mV), and to long rise and fall times.

• Transmission Line Drive Capability is afforded by open emitter outputs of ECL devices. No "Line Drivers" are listed in ECL families, as each device is a line driver.

• Wire-Oring reduces the number of logic devices required in system design by producing additional OR gate functions with only an interconnection.

■BASIC HIGH-SPEED LOGIC DESIGN CONSIDERATIONS

Hitachi's 10K ECL logic circuits are designed for complex functions that enhance overall system speed and reduce problems normally associated with high-speed operation. The following factors should be considered in designing high-speed systems:

1. Significant time delays caused by interconnect-wiring:

At logic speeds of 2NS, an equivalent "gate delay" is introduced for every foot of interconnect-wiring. Signals which travel between functions interconnected within a single monolithic chip, as in 10K ECL, avoid such delays.

2. Distorted waveforms due to line reflections:

At high speeds, line lengths can approach the wavelength of the signal. Improperly terminated lines can result in reflections that cause false triggering (see Figure 2). RF technology provides the solution, which is to employ "transmission-line" practices, as well as to terminate each signal line with appropriate impedance. Low-impedance, emitter-follower outputs of ECL circuits facilitate transmission-line practices without upsetting system voltage levels.

3. Crosstalk between adjacent signal leads:

Increased affinity for crosstalk in high-speed circuits is the result of fast rise and fall times. In 10K ECL design, rise and fall times have been deliberately slowed, reducing crosstalk without compromising other important performance parameters.

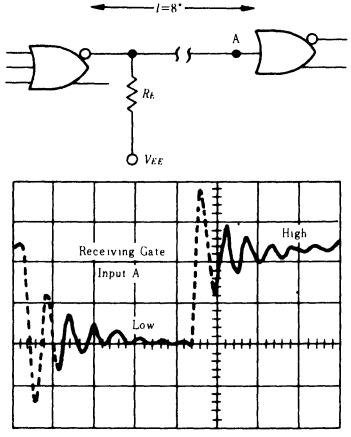


Fig.2a Unterminated Transmission Line (No Ground Plane Used)

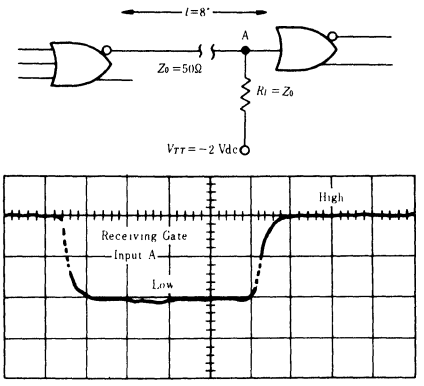


Fig.2b Properly Terminated Transmission Line (Ground Plane Added)

■CIRCUIT DESCRIPTION

A typical ECL circuit, shown in Figure 3, consists of a differential-amplifier input circuit, a temperature and voltage compensated bias network, and emitter-follower outputs to restore dc levels and provide buffering for transmission line driving. High fan-out operation is possible because of the high input impedance of the differential amplifier input and the low output impedance of the emitter follower outputs. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the OR function and its complement, the NOR function.

Power-Supply Connections — Any of the power supply levels V_{TT}, V_{CC}, or V_{EE} may be used as ground. However, the use of the V_{CC} node as ground results in best noise immunity. In such a case; V_{CC}=0, V_{TT} =−2.0V, V_{EE}=−5.2V.

System Logic Specifications — The output logic swing of 0.85V, as shown by the typical transfer characteristics curve, varies from a LOW state of V_{OL}=−1.75V to a HIGH state of V_{OH}=−0.9V with respect to ground.

Positive logic is used when reference is made to logical "0"s or "1"s Then

"0" = −1.75V = LOW
"1" = −0.9V = HIGH typical

Circuit Operation — Beginning with all logic inputs LOW (nominal −1.75V), assume that Q1 through Q4 are cut off because their P-N base-emitter junctions are not conducting, and the forward-biased Q5 is conducting.

Under these conditions, with the base of Q5 held at −1.29V by the V_{BB} network, its emitter will be one diode drop (0.8V) more negative than its base, or −2.09V. (the 0.8V differential is a characteristic of this P-N junction.)

The base-to-emitter differential across Q1 — Q4 is then the difference between the common emitter voltage (−2.09V) and the LOW logic level (−1.75V) or 0.34V.

This is less than the threshold voltage of Q1 through Q4 and these transistors will remain cut off. When any logic input is shifted upward from the −1.75V LOW state to the −0.9V HIGH state, the base voltage of that transistor increases beyond the threshold point and the transistor turns on.

When this happens, the voltage at the common-emitter point rises from −2.09V to −1.75 V (one diode drop below the −0.9V base voltage of the input transistor), and since the base voltage of the fixed-bias transistor (Q5) is held at −1.29V, the base-emitter voltage Q5 cannot sustain conduction, and this transistor is cut off. This action is reversible, and when the input signal(s) return to the LOW state, Q1 — Q4 are again turned off and Q5 again becomes forward biased.

The collector voltages resulting from the switching action of Q1 — Q4 and Q5 are transferred through the output emitter-follower to the output terminal. Note that the differential action of the switching transistors (one section being off when the other is on) furnishes simultaneous complementary signals at the output. This action also maintains constant power supply current drain.

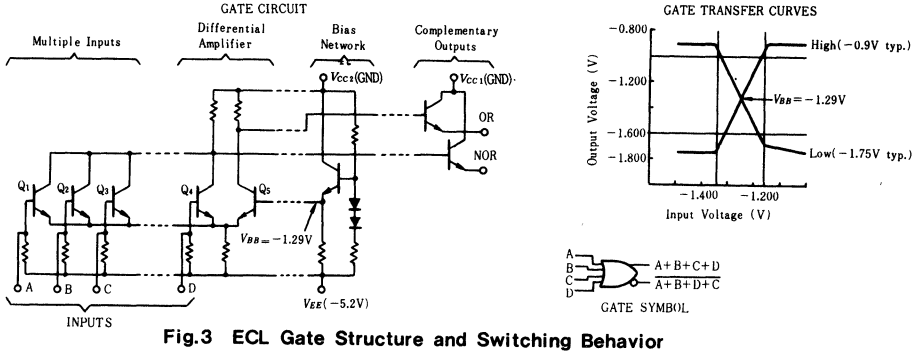


Fig.3 ECL Gate Structure and Switching Behavior

■TECHNICAL DATA

In subsequent sections of this data book, the significant ECL parameters are identified, and complete data provided for each of the functions. Data, characteristics, and application information common to all ECL families are discussed in this section. Common characteristics of major importance are:

- Maximum Ratings, including both AC and DC characteristics and temperature limits.
- Transfer Characteristics, which define logic levels and switching thresholds.
- DC Parameters, such as output levels, threshold levels, and forcing functions.
- AC Parameters, such as propagation delays, rise and fall times, and other time dependent characteristics.

This section also includes general layout and design guides to assist the designer in building and testing systems with ECL circuits.

●Maximum Ratings

Table 1

Item	Symbol	Rating	Unit
Supply Voltage*	V_{EE}	−8~0	V
Input Voltage*	V_{in}	0~V_{EE}	V
Output Current	I_O	50	mA
Surge Output Current	$I_{O(surge)}$	100	mA
Junction Temperature	T_j	125	°C
Storage Temperature	T_{stg}	−55~+125	°C

* Value at V_{CC}=GND

●Recommended Operating Conditions

Table 2

Item	Symbol	Value	Unit
Operating Temperature Range	T_A	−30 to +85	°C
D.C. Fan Out		70	
Supply Voltage Range	V_{EE}	−5.2±10%	V

For ECL logic gates, the complementary outputs are represented by two transfer curves—to describe the OR and NOR switching action, respectively. A typical transfer curve and associated data for all ECL families is shown in Figure 4.

It is not necessary to measure transfer curves at all points of the curves. To guarantee correct operation, measure two sets of min./max. logic level parameters.

The first set is obtained by applying test voltages V_{IL} min. and V_{IH} max. in sequence to the gate inputs, and measuring OR and NOR output levels to make sure they are between V_{OL} max. and V_{OL} min. specifications. The second set of logic level parameters relates to the switching thresholds, and is distinguished by an "A" in symbol subscripts.

A test voltage V_{ILA} max. is applied to the gate, and NOR and OR outputs are measured to be sure they are above the V_{OHA} min. and below the V_{OLA} max. levels, respectively. Similar checks are made using the test input voltage V_{IHA} min. The result of these specifications insures:

a) The switching threshold ($-V_{BB}$) falls within the darkest rectangle; i.e., switching does not begin outside this rectangle.

b) Quiescent logic levels fall in the lightest shaded ranges. Table 3 shows the guaranteed 10K ECL logic levels and switching thresholds.

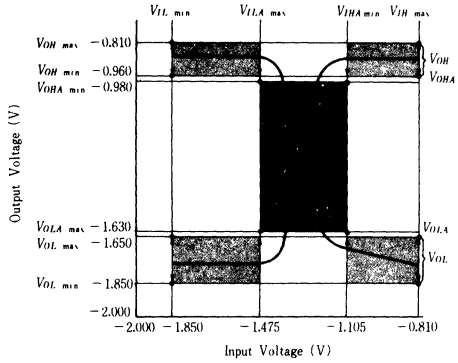


Fig. 4 Transfer Curves (HD10K Example)

Figure 5 shows typical transfer characteristics as a function of temperature.

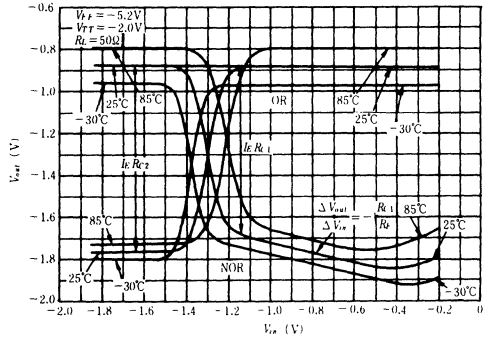


Fig. 5 The Transfer Curves for Temperature Variations.

Table 3 D.C Specification Test Points (HD10K Example)

Input	Output	Value	Unit
V_{IL} min		−1.850	V
V_{IH} max		−0.810	
	V_{OL} min	1.850	
	V_{OL} max	−1.650	
	V_{OH} min	−0.960	
	V_{OH} max	−0.810	
V_{ILA} max		−1.475	
V_{IHA} min		−1.105	
	V_{OLA} max	−1.630	
	V_{OHA} min	−0.980	
With suitable inputs :			
Typical Output HIGH State		−0.900	
Typical Output LOW State		−1.750	
Nominal V_{BB}(Switching Threshold)		−1.290	

Test Conditions;

V_{EE} = -5.2V, V_{CC} = 0V, Ta = 25°C,
after thermal equilibrium has been established on airflow, greater than 500 linear fpm is maintained.
Outputs loaded 50Ω to -2.0Vdc

Table 4 The Temperature Coefficients

		Ta = −30 ~ +25°C	Ta = +25 ~ +85°C
"1" Level	$\Delta V_{IHA}/\Delta T$	1.82mV/°C	1.16mV/°C
	ΔV_{OHA} min/ΔT	1.82mV/°C	1.16mV/°C
	$\Delta V_{NH}/\Delta T$	1.82mV/°C	1.16mV/°C
"0" Level	$\Delta V_{ILA}/\Delta T$	0.46mV/°C	0.58mV/°C
	ΔV_{OLA} max/ΔT	0.46mV/°C	0.58mV/°C
	$\Delta V_{NL}/\Delta T$	0.46mV/°C	0.58mV/°C

Table 4 show the temperature coefficients of ECL 10K DC parameters.

Figure 6 shows transfer characteristic data obtained for a variety of supply voltages.
Table 5 indicates change rates of output voltages as a function of power supply voltages.

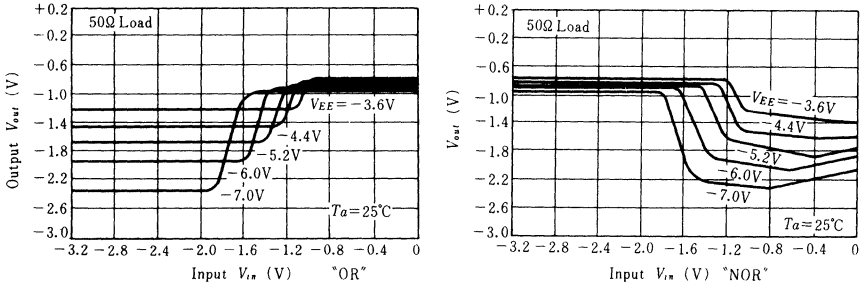


Fig. 6 The Transfer Curves for power supply variations

Table 5 Typical Level Change Rates

$\Delta V_{OH}/\Delta V_{EE}$	0.016
$\Delta V_{OL}/\Delta V_{EE}$	0.250
$\Delta V_{BB}/\Delta V_{EE}$	0.148

■NOISE MARGIN

"Noise Margin" is a measure of a logic circuit's resistance to undesired switching. ECL noise margin is defined in terms of specification points surrounding the switching threshold. The critical parameters of interest are those designated V_{OHA} min., V_{OLA} max., V_{IHA} min., and V_{ILA} max. in the transfer characteristic curves.

Guaranteed noise margin (NM) is defined:

$$NM_{HIGH\ LEVEL} = V_{OHA}\ min. - V_{IHA}\ min.$$
$$NM_{LOW\ LEVEL} = V_{ILA}\ max. - V_{OLA}\ max.$$

To compute noise margin, assume an ECL gate drives a similar ECL gate (Fig. 7). At a gate input (point B) equal to V_{ILA} max., ECL gate #2 can begin to enter the shaded transition region. In this worst-case example, V_{OLA} max. specification point guarantees that no device can enter the transition region before an input equal to V_{ILA} max. is reached. V_{ILA} max. is a critical point for noise margin computation, since it is the edge of the transition region.

To find the other critical voltage, note the output from ECL gate #1 (point A). From Fig. 7, it can be observed that the V_{OLA} max. specification insures that LOW state OR output from gate #1 can be no greater than V_{OLA} max. Note also that V_{OLA} max. is more negative than V_{ILA} max.

With V_{OLA} max. at the input to gate #2, the transition region is not yet reached. (The input voltage to gate #2 is still to the left of V_{ILA} max. on the transfer curve.) To switch gate #2, additional voltage is needed to move the input from V_{OLA} max. to V_{ILA} max., constituting the "safety factor" defined as noise margin, and is calculated as the magnitude of difference between the two specification voltages, or for the 10K ECL levels as follows:

$$NM_{LOW} = V_{ILA}\ max. - V_{OLA}\ max. = 1.475V$$
$$-(-1.630V) = 155mV$$

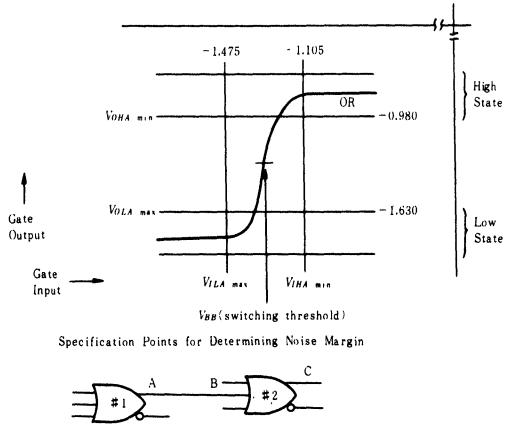
$$NM_{HIGH} = V_{OHA}\ min. - V_{IHA}\ min. = 0.980V$$
$$-(-1.105V) = 125mV$$

Analogous results are obtained for "NOR" transfer data.

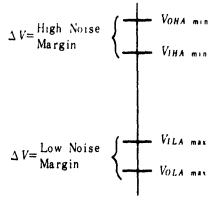
The lesser of the two noise margins is that for the HIGH state, 125mV, or the guaranteed margin against signal undershoot, and power or thermal disturbances. As shown in the table, typical noise margins usually exceed the guaranteed value by about 75mV.

Noise immunity involves line impedances, circuit output impedances, and propagation delay, in addition to noise-margin specifications.

A complete picture of overall system noise immunity involves not only noise-margin specifications, tabulated on ECL data sheets, but other circuit-related factors that determine how difficult it is to apply a noise signal of sufficient magnitude and duration to cause the circuit to propagate a false logic state.



Specification Points for Determining Noise Margin



Noise Margin Computations

Family	Guaranteed Worst-Case dc Noise Margin	Typical dc Noise Margin
ECL 10K	0.125	0.210

Fig.7 ECL Noise Margin Data

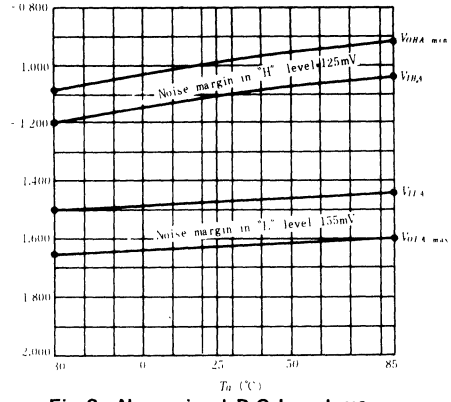


Fig.8 Normarized D.C Level vs. Temperature

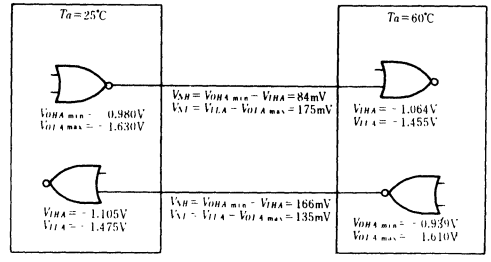


Fig. 9 Noise Margin for Temperature Differences

● AC or Switching Parameters

Time-dependent specifications are defined as circuit effects caused by a specific input signal as it travels through the circuit.

They include the time delay involved in changing the output level from one logic state to another. Memories also include the time required for circuit output to respond to input signal (propagation delay or access time). Because of differing conditions and parameters among logic families, common ECL waveform and propagation delay terminologies are shown in Figure 10.

Specific rise, fall and propagation delay times are given on the data sheet for each specific functional block. Similar to transfer characteristics, however, AC parameters are temperature and voltage dependent. Typical variations for 10K ECL are shown in Figure 11.

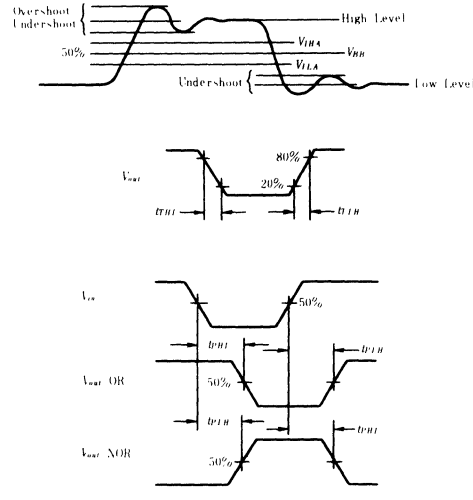


Fig.10 ECL Waveform and Propagation Delay

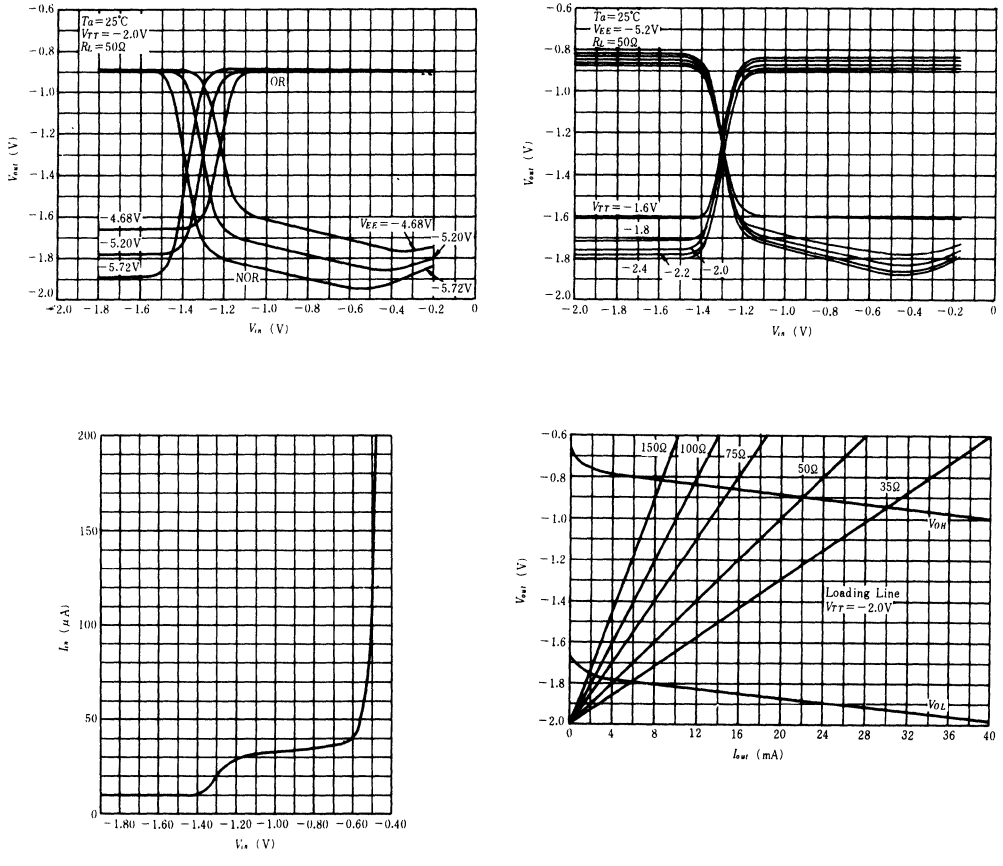


Fig.11 The characteristics of a Standard Gate

● Setup and Hold Times

AC parameters for setup and hold times are defined as follows: In ECL logic devices, t_{su} is the minimum time (50%-50%) before positive transition of clock pulse (C) that information must be present at data input (D) to insure proper operation of the device.

t_h is defined as the minimum time after positive transition of clock pulse (C) that information must remain unchanged at data input (D) to insure proper operation. Setup and hold waveforms are shown in Figure 12.

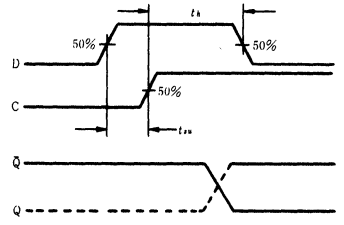
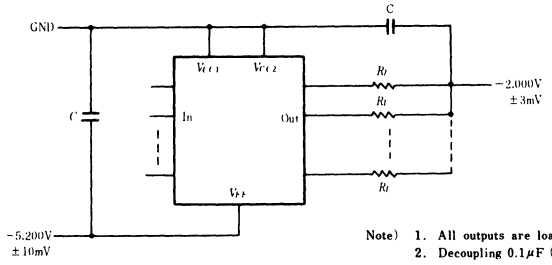


Fig.12 Setup and Hold Waveforms for ECL Logic Devices

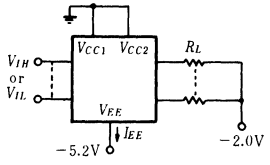
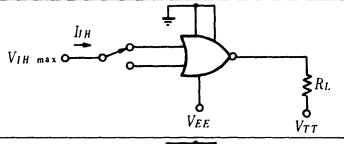
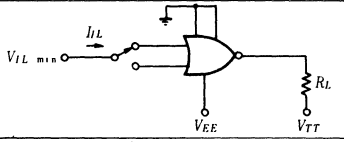
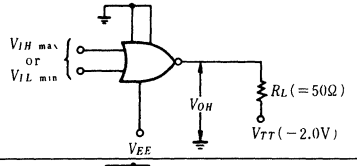
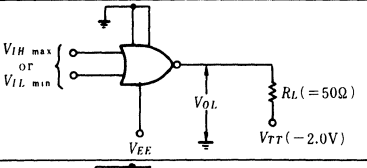
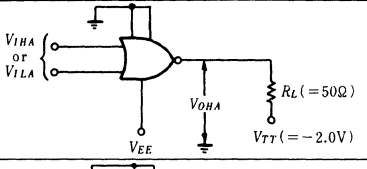
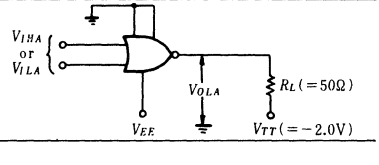
■DEFINITION OF SYMBOLS AND TESTING METHOD

●DC Characteristics

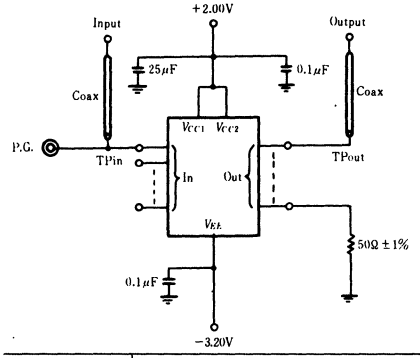


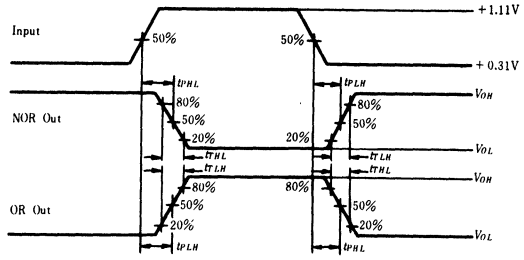
DC Characteristics

Note) 1. All outputs are loaded with 50Ω to GND (50Ω±1%)
2. Decoupling 0.1μF (25V) from GND to V_{CC} and V_{EE}
3. The tolerance of to shall be ±2°C

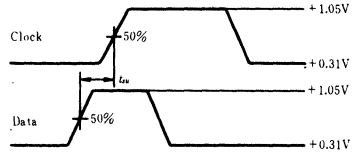
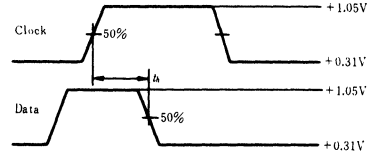
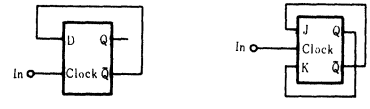
Item	Testing Method and Definitions
I_{EE}	Current required by each device from V_{EE} supply. 
I_{IH}	Current flowing into device lead with specified V_{IH} applied. 
I_{IL}	Current flowing into device lead with specified V_{IL} applied. 
V_{OH}	Voltage level at output terminal with specified output load and conditions applied to establish HIGH output level. All outputs are loaded with 50 to V_{TT} (= −2.0V). 
V_{OL}	Voltage level at output terminal with specified output load and conditions applied to establish LOW output level. All outputs are loaded with 50 to V_{TT} (= −2.0V). 
V_{OHA}	Output HIGH voltage threshold with inputs set at respective threshold levels; V_{IHA} min. or V_{ILA} max. 
V_{OLA}	Output LOW voltage threshold with inputs set at respective threshold levels; V_{ILA} max. or V_{IHA} min. 

●A.C Characteristics



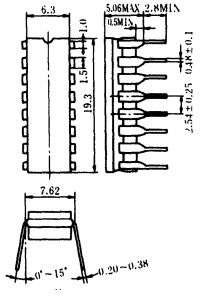


Notes) 1. Input pulse: $t_{TLH} = t_{THL} = 2.0 \pm 0.2$ns (20%−80%)
2. Unused output connected toa 50Ω resistor to GND.
3. All inputs and outputs equal length 50Ω impedance lines R_T equal 50Ω termination of scope.

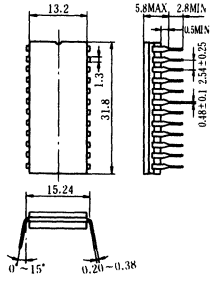
Item	Testing Method and Definitions
t_{TLH}	Time between two specified reference points (20%, 80%) as waveform changes from LOW to HIGH.
t_{THL}	Time between two specified reference points (20%, 80%) as waveform changes from HIGH to LOW.
t_{PLH} t_{PHL}	Time between specified reference points on input and output voltage waveforms with a change in output.
t_{su}	The interval immediately preceding active transition of timing pulse (clock pulse), or preceding transition of the control input to its latching level, during which data must be maintained at input to insure its recognition. 
t_h	The interval immediately following active transition of timing pulse, or following transition of the control input to its latching level, during which data must be maintained at input to insure its continued recognition. 
f_{TOG}	The maximum repetition rate at which clock pulses may be applied to a sequential circuit, above which the device (flip-flop or counter) may cease to function. 

■PACKAGE (Unit : mm)

●16 Pin Ceramic Package



●24 Pin Ceramic Package



OPTIONAL DATA

• Power Supply Considerations

ECL circuits are characterized with the V_{CC} point at ground potential and the V_{EE} point at −5.2V. While this ECL convention is not necessarily mandatory, it does result in maximum noise immunity. This is so because any noise induced on the V_{EE} line is applied to the circuit as a common-mode signal which is rejected by the differential action of the ECL input circuit. Noise induced into the V_{CC} line is not cancelled out in this fashion. Hence, a good system ground at the V_{CC} bus is required for best noise immunity.

Power supply regulation which will achieve 10% regulation or better at the device level is recommended. The −5.2V power supply potential will result in best circuit speed. Other values for V_{EE} may be used. A more negative voltage will increase noise margins at a cost of increased power dissipation. A less negative voltage will have just the opposite effect.

On logic cards, a ground plane or ground bus system should be used. A bus system should be wide enough to prevent significant voltage drops between supply and device and to produce a low source inductance.

Although little power supply noise is generated by ECL logic, power supply bypass capacitors are recommended to handle switching currents caused by stray capacitance and asymmetric circuit loading. A parallel combination of a 1.0μF and a 100pF capacitor at the power entrance to the board, and a 0.01μF low-inductance capacitor between ground and the −5.2V line every four to six packages, are recommended.

Most ECL circuits have two V_{CC} leads. V_{CC1} supplies current to the output transistors and V_{CC2} is connected to the circuit logic transistors. The separate V_{CC} pins reduce cross-coupling between individual circuits within a package when the outputs are driving heavy loads. All V_{CC} pins should be connected to the ground plane or ground bus as close to the package as possible.

• Power Dissipation

The power dissipation of ECL functional blocks is specified on their respective data sheets. This specification does not include power dissipated in the output devices due to output termination. The omission of internal output pull-down resistors permits the use of external terminations designed to yield best system performance. To obtain total operating power dissipation of a particular functional block in a system, the dissipation of the output transistor, under load, must be added to the circuit power dissipation.

The table in Figure 12 lists the power dissipation in the output transistors plus that in the external terminating resistors, for the more commonly used termination values and circuit configurations. To obtain true package power dissipation, one output-transistor power-dissipation value must be added to the specified package power dissipation for each external termination resistor use; in conjunction with that package. To obtain system power dissipation, the stated dissipation in the external terminating resistors must be added as well. Unused outputs draw no power and may be ignored.

Terminating Resistor Value	Output Transistor Power Dissipation (mW)	Terminating Resistor Power Dissipation (mW)
150 ohms to −2.0 Vdc	5.0	4.3
100 ohms to −2.0 Vdc	7.5	6.5
75 ohms to −2.0 Vdc	10	8.7
50 ohms to −2.0 Vdc	15	13
2.0 k ohms to V_{EE}	2.5	7.7
1.0 k ohms to V_{EE}	4.9	15.4
680 ohms to V_{EE}	7.2	22.6
510 ohms to V_{EE}	9.7	30.2
270 ohms to V_{EE}	18.3	57.2
82 ohms to V_{CC} and 130 ohms to V_{EE}	15	140

Fig.12 Average Power Dissipation in Output Circuit with External Terminating Resistors.

The power dissipation of ECL functional blocks varies with both temperature and V_{EE}.

Typical variations are shown in Figure 13. The graph is normalized so that it applies to all ECL lines. The reference temperature is 25°C and the reference power is obtained by multiplying the typical I_E value (total power supply drain current specified on the data sheet) by V_{EE} (5.2V). For those devices where only the maximum value of I_E is specified on the data sheet, typical power dissipation is approximately 80% of that calculated with the I_E (max) specification.

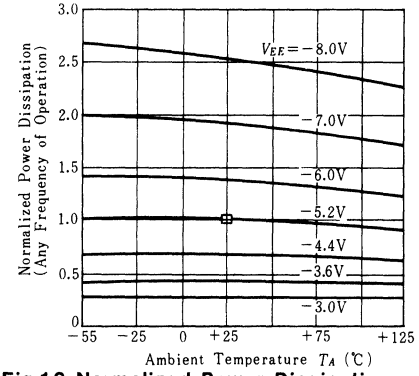


Fig.13 Normalized Power Dissipation vs. Temperature and Supply Voltage

● Loading Characteristics

The differential input to ECL circuits offers several advantages. Its common-mode-rejection feature offers immunity against power-supply noise injection, and its relatively high input impedance makes it possible for any circuit to drive a relatively large number of inputs without deterioration of the guaranteed noise margin. Hence, dc fanout with ECL circuits does not normally present a design problem. Graphs showing typical output voltage levels as a function of load current for ECL 10K are shown in Figure 14. These graphs can be used to determine the actual output voltages for loads exceeding normal operation.

While dc loading increases the capacitances associated with the circuit and, therefore, affects circuit speed, primarily rise and fall times.

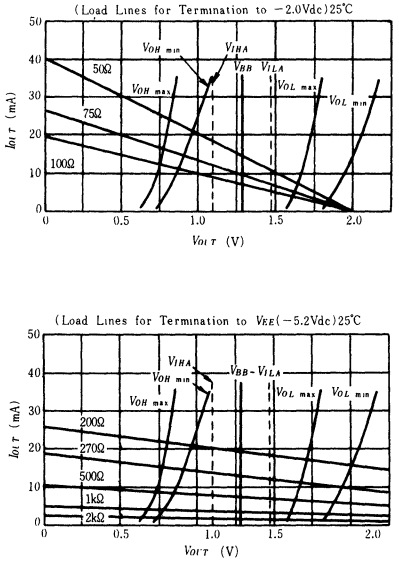


Fig.14 Output Voltage Levels vs. DC Loading

The affections of ac parameter by fanouts are shown in Figure 14-1.

Terminated transmission line signal interconnections are used for best ECL 10K system performance. The propagation delay and rise time of a driving gate are affected very little by capacitance loading along a matched parallel-terminated transmission line. However, the delay and characteristic impedance of the transmission line itself are afected by the distributed capacitance. Signal propagation down the line will be increased by a factor, $\sqrt{1+Cd/Co}$.

Here Co is the normal intrinsic line capacitance, and Cd is the distributed capacitance due to loading and stubs off the line.

Maximum allowable stub lengths for loading off of a ECL 10K transmission line vary with the line impedance. For example, with Zo=50 ohms, maximum stub length would be 4.5 inches. But when Zo=100 ohms, the maximum allowable stub length is decreased to 2.8 inches. The input loading capacitance of a ECL 10K gate is about 2.9pF.

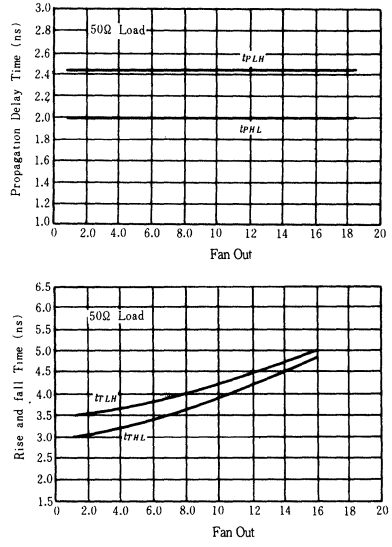


Fig.14-1 AC Parameter vs. Fanout

Therefore in order to keep the system speed, the recommended maximum fanout is defined within 10. (without to use the transmission line.)

● Unused ECL Inputs

All single-ended input ECL logic circuits contain input pulldown resistors between the input transistor bases and V_{EE}. As a result,unused inputs may be left unconnected. Input pulldown resistor values are typically 50 kohms and are not to be used as pulldown resistors for preceding open-emitter outputs.

Several ECL devices do not have input pulldowns. Examples are the differential line receivers. If a single differential receiver within a package is unused, one input of that receiver must be tied to the V_{BB} pin provided, and the other input goes to V_{EE}. (for example; HD10116)

■SYTEM DESIGN CONSIDERATIONS

● Thermal Management

Circuit performance and long-term circuit reliability are affected by die temperature.

Normally, both are improved by keeping the IC junction temperature low.

Electrical power dissipated in any integrated circuit is a source of heat.

This heat source increases the temperature of the die. The basic formula for converting power dissipation to estimated junction temperature is:

$T_j = T_A + P_D\ (\theta_{jc} + \theta_{CA})$

or

$T_j = T_A + P_D\ (\theta_{jA})$

where

T_j = junction temperature

T_A = ambient temperature

P_D = power dissipation

θ_{jc} = average thermal resistance, junction to case

θ_{CA} = average thermal resistance, case to ambient

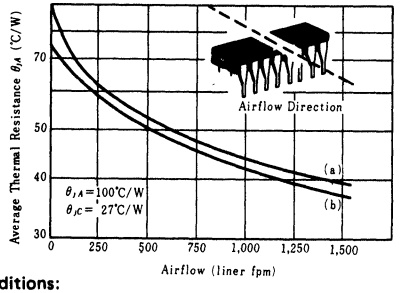
θ_{jA} = average thermal resistance, junction to ambient

Only two terms can be varied by the user-the ambient thermal resistance, θ_{CA}. Both system air flow and the package mounting technique affect the θ_{CA} thermal resistance term.

The maximum and average thermal resistance values for standard ECL IC package are given in Figure 15.

Package Type	θ_{jA}(°C/W)		θ_{jc}(°C/W)
	Maximum	Average	maximum
16 pin Ceramic Package	150	100	50
24 pin Ceramic Package	—	45	10

Fig.15 The Maximum and Average Thermal Resistance Values.



Conditions:
package; 16 pin Ceramic Package power dissipation; 200mW
measurement method; Diode Measurements
(a) Barnes socket
(b) PCB (10.2cm x 15.24cm x 1.6mm Cu)

Fig.16 Airflow vs. Thermal Resistance

The effect of air flow over the packages on θ_{jA} is illustrated in the graphs of Figure 16.

Fig. 17 shows the maximum power dissipation allowable at various ambient temperatures (still air) in a case of 16 pin ceramic dual in line package.

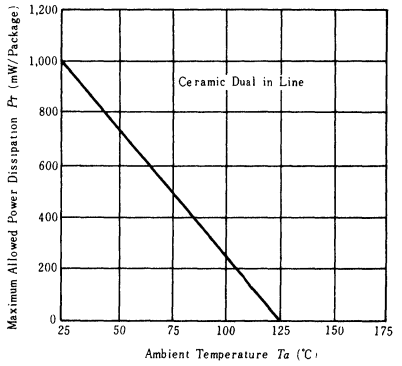


Fig.17 Ambient Temperature Derating Curve

● Interfacing ECL to Slower Logic Types

ECL circuits are interfaceable with MOS other logic forms. For ECL/TTL interfaces, when ECL is operated at the recommended −5.2 volts and TTL at +5V supply, currently available translator circuits, such as the HD10124 and HD10125, may be used.

For systems where a dual supply (−5.2V and +5V) is not practical, a discrete component translator can be designed. ECL also interfaces readily with MOS. With CMOS operating at +5V, any of the ECL to TTL translators works very well.

On the other hand, CMOS will drive ECL directly when using a common −5.2V supply.

● Circuit Interconnections

Though not necessarily essential, the use of multilayer printed circuit boards offers a number of advantages in the development of high-speed logic cards.

Not only do multilayer boards achieve a much higher package density, interconnecting leads are kept shorter, thus minimizing propagation delay between packages.

Moreover, the unbroken ground planes made possible with multilayer boards permit much more precise control of transmission line impedances when these are used for interconnecting purposes. Thus multilayer boards are recommended for ECL at top circuit speed, when high-density packaging is a requirement, or when transmission line interconnects are used. Point-to-point back-lane wiring without matched line terminations may be employed for ECL interconnections if line runs are kept short.

This applies to line runs up to 6 inches. But, because of the open-emitter outputs of ECL circuits, pull-down resistors are always required. Several ways of connecting such pull-down resistors are shown in Figure 18.

Resistor values for the connection in Figure 18a may range from 270 ohms to 2 kohms depending on power and load requirements. Power may be saved by connecting pull-down resistors in the range of 50 ohms to 150 ohms, to −2.0V dc, as shown in Figure 18b. Use of a series damping resistor, Figure 18c, will extend permissible lengths of unmatched-impedance interconnections, with some loss of edge speed.

With proper choice of the series damping resistor, line lengths can be extended to any length, while limiting overshood and undershoot to a predetermined amount.

Damping resistors usually range in value from 10 ohms to 100 ohms, depending on the line length, fanout, and line impedance. The open emitter-follower outputs of ECL give the system designer all possible line driving options.

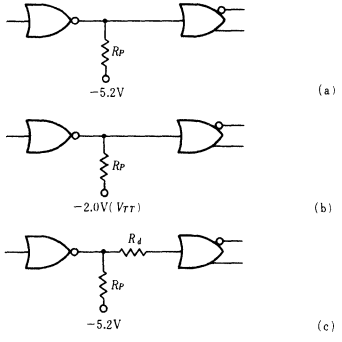


Fig.18 Pull-Down Resistor Techniques

One major advantage of ECL over saturated logic is its capability for driving matched-impedance transmission lines. Use of transmission lines retains signal integrity over long distances. The ECL emitter-follower output transistors will drive a 50-ohm transmission line terminated to −2.0V dc. This is the equivalent current load of 22mA in the HIGH logic state and 6 mA in the LOW state.

Parallel termination of transmission lines can be done in two ways.

One, as shown in Figure 19a, uses a single resistor whose value is equal to the impedance (Zo) of the line. A terminating voltage (V_{TT}) of −2.0Vdc must be supplied to the terminating resistor. Another method of parallel termination uses a pair of resistors, R1 and R2, Figure 19b illustrates this method. The following two equations are used to calculate the values of R1 and R2:

R1 = 1.6Zo

R2 = R1·Z0/(R1-Z0)

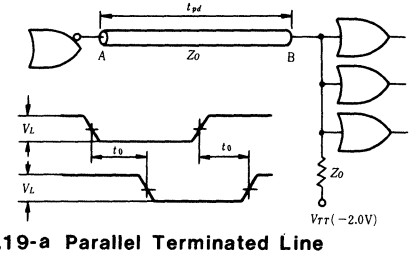


Fig.19-a Parallel Terminated Line

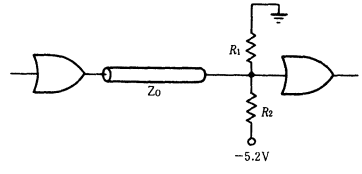


Fig.19-b Parallel Termination Thevenin Equivalent

Another popular approach is the series-terminated transmission line (see Figure 20).

This differs from parallel termination in that only one-half the logic swing is propagated through the lines. The logic swing doubles at the end of the transmission line due to reflection on an open line, again establishing a full logic swing.

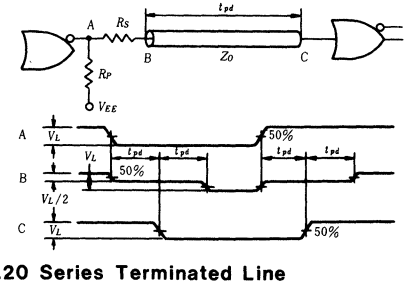


Fig.20 Series Terminated Line

To maintain clean wave fronts, the input impedance of the driven gate must be much greater than the characteristic impedance of the transmission line. This condition is satisfied by ECL circuits which have high impedance inputs. Using the appropriate terminating resistor (Rs) at point A (Figure 20), the reflections in the transmission line will be terminated. The advantages of series termination include ease of driving multiple series-terminated lines, low power consumption, and low cross talk

between adjacent lines. The disadvantage of this system is that loads may not be distributed along the transmission line due to the one-half logic swing present at intermediate points. For board-to-board interconnections, coaxial cable may be used for signal conductors. The termination techniques just discussed also apply when using coax. Coaxial cable has the advantages of good noise immunity and low attenuation at high frequencies. No significant performance degradation occurs for lengths up to 50 feet for ECL.

Twisted pair lines are one of the most popular methods of interconnecting cards or panels. The complementary outputs of any ECL function are connected to one end of the twisted pair line, and any ECL differential line receiver to the other as shown in the example, Figure 21. R_T is used to terminate the twisted pair line.

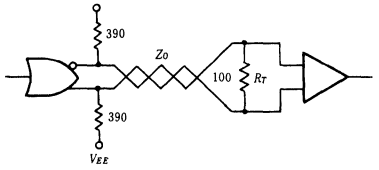


Fig.21 Twisted Pair Line Driver/Receiver

ECL signals may be sent very long distances (>1000 feet) on twisted pair, although line attenuation will limit bandwidth, degrading edge speeds when long line runs are made. If timing is critical, parallel signal paths (shown in Figure 22) should be used when fanout to several cards is required. This will eliminate distortion caused by long stub lengths off a signal path. Wire-wrapped connections can be used with ECL. The mismatch occurs with ECL, but the distance between the wire-wrap connection and the end of the line is generally short enough so the reflections cause no problem.

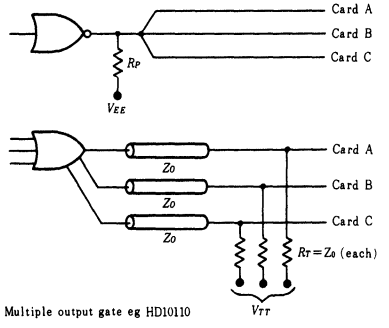


Fig.22 Parallel Fanout Techniques

Series damping resistors may be used with wire-wrapped lines to extend permissible backplane wiring lengths. The recommended wire-wrapped circuit cards have a ground plane on one side.

Microstrip and Stripline

Microstrip and stripline techniques are used with printed circuit boards to form transmission lines. Microstrip consists of a constant-width conductor on one side of a circuit board, with a ground plane on the other side (shown in Figure 23).

The characteristic impedance is determined by the width and thickness of the conductor, the thickness of the circuit board, and the dielectric constant of the circuit board material. Stripline is used with multilayer circuit boards as shown in Figure 23. Stripline consists of a constant-width conductor between two ground planes.

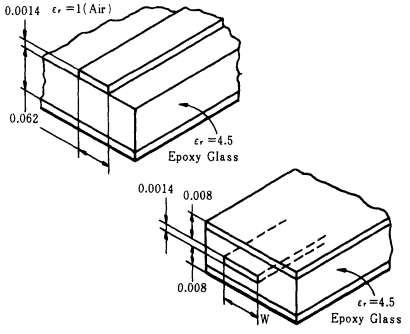


Fig.23 PC Interconnection Lines for use with ECL

● Clock Distribution

Clock distribution can be a system problem.

At ECL speeds, tither coaxial cable or twisted pair line can be used to distribute clock signals throughout a system.

Clock line lengths should be controlled and matched when timing could be critical.

Once the clocking signals arrive on card, a tree distribution should be used for large-fanouts at high frequency. An example of the application of this technique is shown in Figure 24.

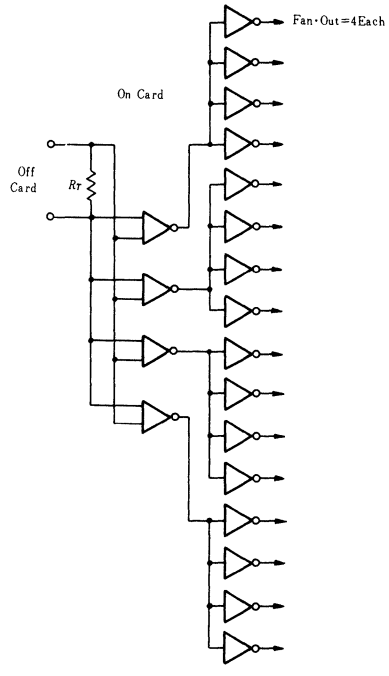


Fig.24 64 Fanout Clock Distribution

● Logic Shortcuts

ECL circuitry offers several logic design conveniences. Among these are:

1. Wire-OR (can be produced by wiring ECL output emitters together outside packages).
2. Complementary Logic Outputs (both OR and NOR are brought out to package pins in most cases).

An example of the use of these two features to reduce gate and package count is shown in Figure 25.

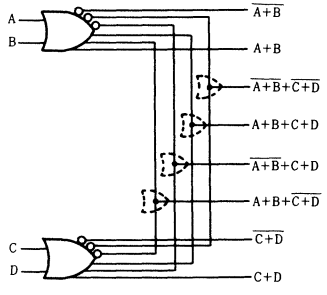


Fig.25 Example (Use of Wire-OR and Complementary Outputs)

The connection shown saves four 2-input gates and two inverter over performing the same functions with saturated type logic.

Propagation delay is increased approximately 50 ps per wire-OR connection.

In general, wire-OR should be limited to 6 ECL outputs to maintain a proper LOW logic level. The use of a single output pulldown resistor is recommended per wire-OR, to economize on power dissipation.

● Testing ECL Series

To obtain results correlating with Hitachi circuit specifications certain test techniques must be used. A schematic of a typical gate test circuit is shown in Figure 26. A solid ground plane is used in the test setup. All power leads and signal leads are kept as short as possible. The sampling scope interface runs directly to the 50-ohm inputs of Channel A and B via 50-ohm coaxial cable.

Equal-length coaxial cables must be used between the test set and the A and B scope inputs. The pulse generator must be capable of 2.0ns rise and fall times for ECL 10K. In addition, the generator voltage must have an offset to give ECL signal swings of ≈±400mV about a threshold of ≈+0.7V when V_{CC}=+2.0V and V_{EE}=−3.2V for ac testing of logic devices. The power supplies are shifted +2.0V, so that the device under test has only one resistor value to load into the precision 50-ohm input impedance of the sampling oscilloscope. Use of this technique yields a close correlation between Hitachi and customer testing. Unused outputs are loaded with a 50-ohm resistor to ground. The positive supply (V_{CC}) should be decoupled from the test board by RF type 25μF capacitors to ground. The V_{CC} pins are bypassed to ground with 0.1μF, as is the V_{EE} pin.

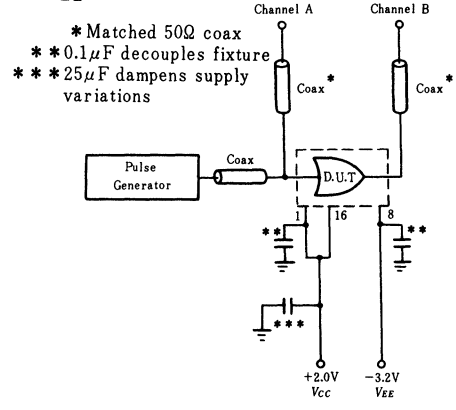


Fig.26 ECL Logic Switching Time Test Setup

HD100K GENERAL INFORMATION

■FEATURES

- On-chip complementary output

Built-in complementary output requires no application of inverters, and avoids problems such as extensive external parts, power dissipation, and propagation delay.

- High input and low output impedances

Due to the high input impedance (compared with TTL devices), greater fan-out is obtained, along with various circuit configuration.

- Stability

Built-in temperature and voltage compensation circuits assure stable output characteristics within all temperature and voltage ranges.

- Compatibility

HD100K is fully compatible with F100K pin configuration, functions and characteristics.

■ELECTRICAL CHARACTERISTICS ($Ta = 0 \sim +85°C$, $V_{EE} = -4.5V$, V_{CC} : GND)

Symbol	Item	min	typ	max	Unit	Conditions
V_{OH}	Output Voltage High	−1025	−955	−880	mV	$V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$ $R_L = 50\Omega$ $V_{TT} = -2V$
V_{OL}	Output Voltage Low	−1810	−1705	−1620	mV	
V_{OHC}	Output Threshold Voltage High	−1035	—	—	mV	$V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$
V_{OLC}	Output Threshold Voltage Low	—	—	−1610	mV	
V_{IH}	Input Voltage High	−1165	—	−880	mV	
V_{IL}	Input Voltage Low	−1810	—	−1475	mV	
I_{IL}	Input Current Low	0.5	—	—	μA	$V_{IN} = V_{IL\ min}$

■MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage*	V_{EE}	−7.0	V
Input Voltage*	V_{in}	$0 \sim V_{EE}$	V
Output Current	I_O	50	mA
Surge Output Current	$I_{O(surge)}$	100	mA
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

* Value at V_{CC} and V_{CCA} = GND

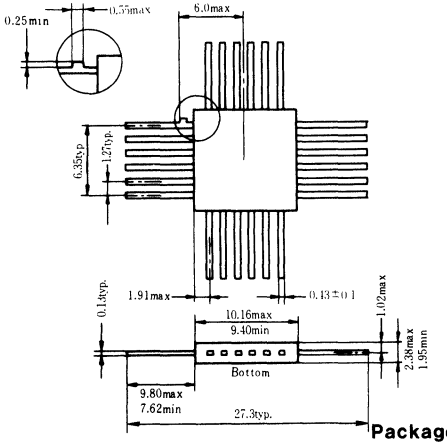
■RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Value	Unit
Operating Temperature Range	T_A	0 ~ 85	°C
Supply Voltage Range	V_{EE}	−4.2 ~ −5.7	V

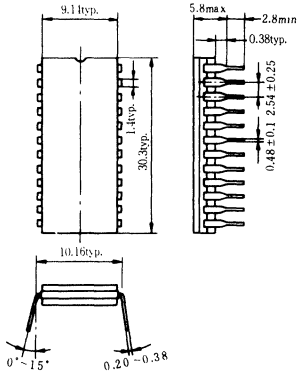
Notes:
1. To guarantee AC and DC specs, refer to each individual specification.
2. When T_j max. exceeds 125° C, heat sink design is required.
3. Relationship between T_j max. and reliability are given in the data sheets that follow.

■PACKAGE

●24 Pin Ceramic Flat Package (HD100KF Series)



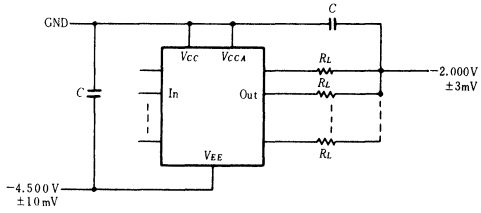
●24 Pin Ceramic Dual-in-line Package (HD100K Series)



Package (Dimensions in mm)

■DEFINITION OF SYMBOLS AND TESTING METHOD

●DC Characteristics

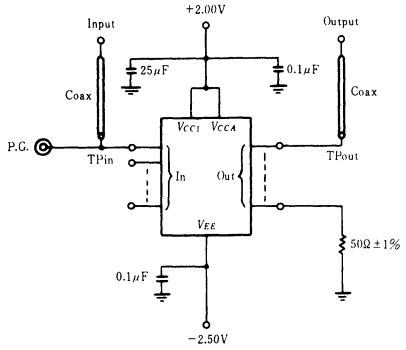


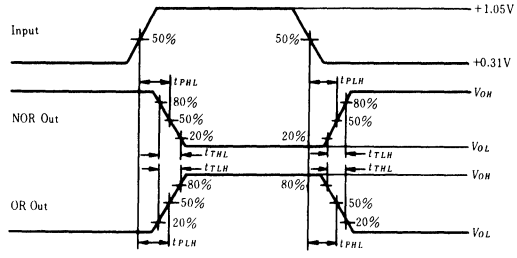
Note) 1. All outputs are loaded with 50Ω to GND (50Ω ± 1%)
2. Decoupling 0.1μF (25V) from GND to V_{CC} and V_{EE}
3. The tolerance of Ta shall be ± 2℃

●DC Characteristic Test Circuit

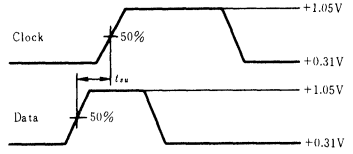
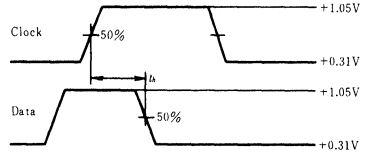
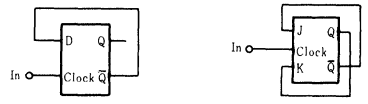
Item	Testing Method and Definitions
I_{EE}	Current required by each device from V_{EE} supply.
I_{IH}	Current flowing into device lead with specified V_{IH} applied.
I_{IL}	Current flowing into device lead with specified V_{IL} applied.
V_{OH}	Voltage level at output terminal with specified output load and conditions applied to establish HIGH output level. All outputs are loaded with 50 to V_{TT} (= −2.0V).
V_{OL}	Voltage level at output terminal with specified output load and conditions applied to establish LOW output level. All outputs are loaded with 50 to V_{TT} (= −2.0V).
V_{OHC}	Output HIGH voltage threshold with inputs set at respective threshold levels; V_{IHA} min. or V_{ILA} max.
V_{OLC}	Output LOW voltage threshold with inputs set at respective threshold levels; V_{ILA} max. or V_{IHA} min.

●AC Characteristics





Note) 1. Input pulse : $t_{TLH} = t_{THL} = 0.7 \pm 0.1$ns (20%~80%)
2. Unused outputs connected to a 50Ω resistor to GND.
3. All inputs and outputs equal length 50Ω impedance lines R_T equal 50Ω termination of scope.
4. C_L = Jig stray capacitance ≦ 3 pF.

Item	Testing Method and Definitions
t_{TLH}	Time between two specified reference points (20%, 80%) as waveform changes from LOW to HIGH.
t_{THL}	Time between two specified reference points (20%, 80%) as waveform changes from HIGH TO LOW.
t_{PLH} t_{PHL}	Time between specified reference points on input and output voltage waveforms with a change in output.
t_{su}	The interval immediately preceding active transition of timing pulse (clock pulse), or preceding transition of the control input to its latching level, during which data must be maintained at the input to insure its recognition. 
t_h	The interval immediately following active transition of timing pulse, or following transition of the control input to its latching level, during which data must be maintained at input to insure its continued recognition. 
f_{Tog}	The maximum repetition rate at which clock pulses may be applied to a sequential circuit, above which the device (flip-flop or counter) may cease to function. 

1. VIEWS ON QUALITY AND RELIABILITY

Basic views on quality at Hitachi are to meet the individual uers' required quality level and maintain a general quality level equal to or above that of the general market. The quality required by the user may be specified by contract, or may be indefinite. In either case, efforts are made to assure reliable performance in actual operating circumstances. Quality control during the manufacturing process, and quality awareness from design through production lead to product quality and customer satisfaction. Our quality assurance technique consists basically of the following steps:

(1) Build in reliability at the design stage of new product development.
(2) Build in quality at all steps in the manufacturing process.
(3) Execute stringent inspection and reliability confirmation of final products.
(4) Enhance quality levels through field data feed back.
(5) Cooperate with research laboratories for higher quality and reliability.

With the views and methods mentioned above, utmost efforts are made to meet users' requirements.

2. RELIABILITY DESIGN OF SEMICONDUCTOR DEVICES

2.1 Reliability Targets

The reliability target is an important factor in sales, manufacturing, performance, and price. It is not adequate to set a reliability target based on a single set of common test conditions. The reliability target is set based on many factors:

(1) End use of semiconductor device.
(2) End use of equipment in which device is used.
(3) Device manufacturing process.
(4) End user manufacturing techniques.
(5) Quality control and screening test methods.
(6) Reliability target of system.

2.2 Reliability Design

The following steps are taken to meet the reliability targets:

(1) Design Standardization
As for design rules, critical items pertaining to quality and reliability are always studied at circuit design, device design, layout design, etc. Therefore, as long as standardized processing and materials are used the reliability risk is extremely small even in the case of new development devices, with the exception of special requirements imposed by functional needs.

(2) Device Design
It is important for the device design to consider total balance of process, structure, circuit, and layout design, especially in the case where new processes and/or new materials are employed. Rigorous technical studies are conducted prior to device development.

(3) Reliability Evaluation by Functional Test
Functional Testing is a useful method for design and process reliability evaluation of IC's and LSI devices which have complicated functions.

The objectives of Functional Test are:

- Determining the fundamental failure mode.
- Analysis of relation between failure mode and manufacturing process.
- Analysis of failure mechanism.
- Establishment of QC points in manufacturing process.

2.3 Design Review

Design Review is an organized method to confirm that a design satisfies the performance required and meets design specifications. In addition, design review helps to insure quality and reliability of the finished products. At Hitachi, design review is performed from the planning stage to production for new products, and also for design changes on existing products. Items discussed and considered at design review are:

(1) Description of the products based on design documents.
(2) From the standpoint of each participant, design documents are studied, and for points needing clarification, further investigation will be carried out.
(3) Specify quality control and test methods based on design documents and drawings.
(4) Check process and ability of manufacturing line to achieve design goal.
(5) Preparation for production.
(6) Planning and execution of sub-programs for design changes proposed by individual specialists,

for test, experiments, and calculations to confirm the design changes.

(7) Analysis of past failures with similar devices, discussion of methods to prevent them, and planning and execution of test programs to confirm success.

3. QUALITY ASSURANCE SYSTEM

3.1 Activity of Quality Assurance

General views of overall quality assurance in Hitachi are as follows:

(1) Problems in each individual process should be solved in the process. Therefore, at the finished product stage the potential failure factors have been removed.

(2) Feedback of information is used to insure a satisfactory level of ability process.

3.2 Quality Approval

To insure quality and reliability, quality approval is carried out at the preproduction stage of device design, as described in section 2. Our views on quality approval are:

(1) A third party executes approval objectively from the standpoint of the customer.

(2) Full consideration is given to past failures and information from the field.

(3) No design change or process change without QA approval.

(4) Parts, materials, and processes are closely monitored.

(5) Control points are established in mass production after studying the process abilities and variables.

3.3 Quality and Reliability Control at Mass Production

Quality control is accomplished through division of functions in manufacturing, quality assurance, and other related departments. The total function flow is shown in Fig. 2. The main points are described below.

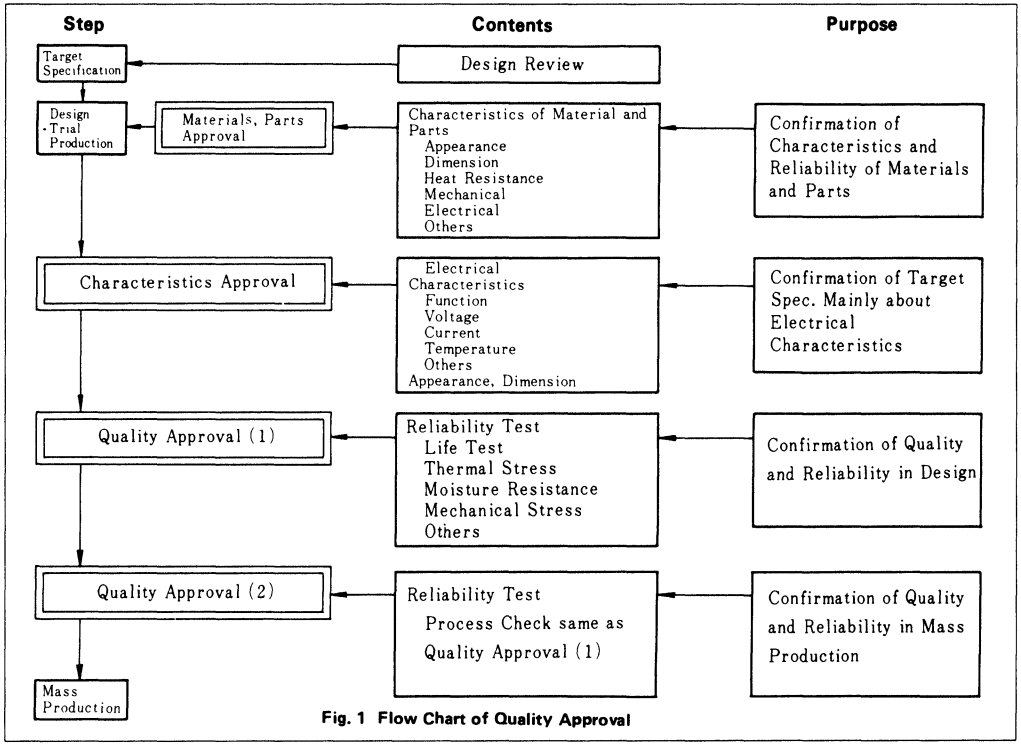


Fig. 1 Flow Chart of Quality Approval

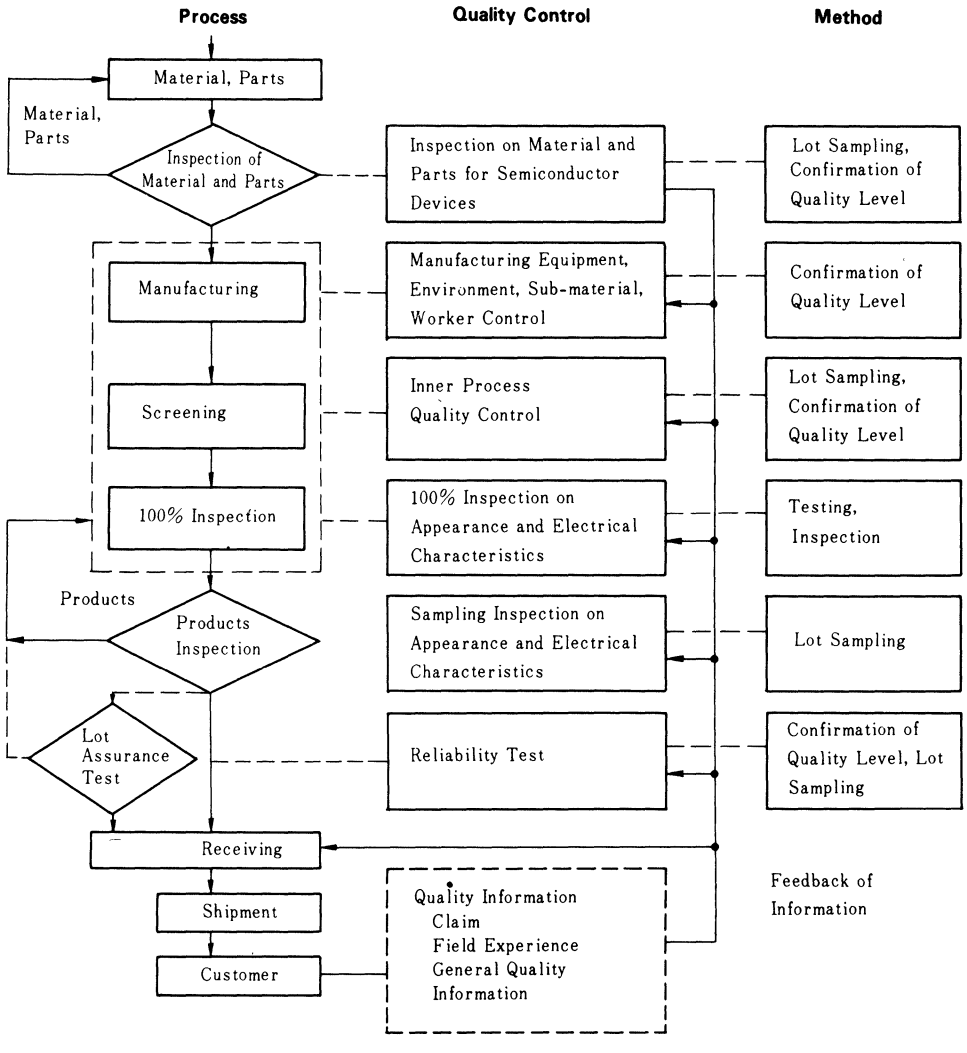


Fig. 2 Flow Chart of Quality Control in Manufacturing Process

3.3.1 Quality Control of Parts and Materials

As semiconductor devices tend towards higher performance and higher reliability, the importance of quality control of parts and materials becomes paramount. Items such as crystals, lead frames, fine wire for wire bonding, packages, and materials needed in manufacturing processes such as masks and chemicals, are all subject to rigorous inspection and control. Incoming inspection is performed based on the purchase specification and drawing. The sampling is executed based mainly on MIL-STD-105D.

The other activities of quality assurance are as follows:

(1) Outside vendor technical information meeting.
(2) Approval and guidance of outside vendors.
(3) Chemical analysis and test.

The typical check points of parts and materials are shown in Table 1.

• Table 1 Quality Control Check Points of Material and Parts (Example)

Material, Parts	Important Control Items	Point for Check
Wafer	Appearance	Damage and Contamination on Surface
	Dimension	Flatness
	Sheet Resistance	Resistance
	Defect Density	Defect Numbers
	Crystal Axis	
Mask	Appearance	Defect Numbers, Scratch
	Dimension	Dimension Level
	Resistoration	
	Gradation	Uniformity of Gradation
Fine Wire for Wire Bonding	Appearance	Contamination, Scratch, Bend, Twist
	Dimension	
	Purity	Purity Level
	Elongation Ratio	Mechanical Strength
Frame	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Processing Accuracy	
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
Ceramic Package	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Leak Resistance	Airtightness
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
	Electrical Characteristics	
	Mechanical Strength	Mechanical Strength
Plastic	Composition	Characteristics of Plastic Material
	Electrical Characteristics	
	Thermal Characteristics	
	Molding Performance	Molding Performance
	Mounting Characteristics	Mounting Characteristics

3.3.2 Inner Process Quality Control

Inner Process Quality Control performs very important functions in quality assurance of semiconductor devices. The manufacturing Inner Process Quality Control is shown in Fig. 3.

(1) Quality Control of Semi-final Products and Final Products

Potential failure factors of semiconductor devices are removed in the manufacturing process. To achieve this, check points are set-up in each process and products which have potential failure factors are not moved to the next process step. Manufacturing lines are rigidly selected and tight inner process quality controls are executed—rigid checks in each process and each lot, 100% inspection to remove failure factors caused by manufacturing variables and high temperature aging and temperature cycling. Elements of inner process quality control are as follows:

- Condition control of equipment and workers environment and random sampling of semi-final products.
- Suggestion system for improvement of work.
- Education of workers.
- Maintenance and improvement of yield.
- Determining quality problems, and implementing countermeasures.
- Transfer of quality information.

(2) Quality Control of Manufacturing Facilities and Measuring Equipment

Manufacturing equipment is improving as higher performance devices are needed. At Hitachi, the automation of manufacturing equipment is encouraged. Maintenance Systems maintain operation of high performance equipment. There are daily inspections which are performed based on related specifications. Inspection points are listed in the specification and are checked one by one to prevent any omission. As for adjustment and maintenance of measuring equipment, specifications are checked one by one to maintain and improve quality.

(3) Quality Control of Manufacturing Circumstances and Sub-Materials

The quality and reliability of semiconductor devices are highly affected by the manufacturing process. Therefore, controls of manufacturing circum-

stances such as temperature, humidity and dust, and the control of submaterials, like gas, and pure water used in a manufacturing process, are intensively executed.

Dust control is essential to realize higher integration and higher reliability of devices. At Hitachi, maintenance and improvement of cleanliness at manufacturing sites is accomplished through attention to buildings, facilities, air conditioning systems, delivered materials, clothes, work environment, and periodic inspection of floating dust concentration.

3.3.3 Final Product Inspection and Reliability Assurance

(1) Final Product Inspection

Lot inspection is done by the quality assurance

Process		Control Point		Purpose of Control
	▽Purchase of Material			
Wafer		Wafer	Characteristics, Appearance	Scratch, Removal of Crystal Defect Wafer
	○Surface Oxidation	Oxidation		Assurance of Resistance
	□Inspection on Surface Oxidation		Appearance, Thickness of Oxide Film	Pinhole, Scratch
	○Photo Resist	Photo Resist		
	□Inspection on Photo Resist		Dimension, Appearance	Dimension Level
	◇PQC Level Check			Check of Photo Resist
	○Diffusion	Diffusion	Diffusion Depth, Sheet Resistance	Diffusion Status
	□Inspection on Diffusion		Gate Width	Control of Basic Parameters (V_{TH}, etc) Cleaness of surface, Prior Check of V_{IH} Breakdown Voltage Check
	◇PQC Level Check		Characteristics of Oxide Film Breakdown Voltage	
	○Evaporation	Evaporation	Thickness of Vapor Film, Scratch, Contamination	Assurance of Standard Thickness
	□Inspection on Evaporation			
	◇PQC Level Check			
	□Wafer Inspection	Wafer	Thickness, V_{TH} Characteristics	Prevention of Crack, Quality Assurance of Scribe
	□Inspection on Chip Electrical Characteristics	Chip	Electrical Characteristics	
	○Chip Scribe		Appearance of Chip	
	□Inspection on Chip Appearance			
	◇PQC Lot Judgement			
Frame				
	○Assembling	Assembling	Appearance after Chip Bonding	Quality Check of Chip Bonding
			Appearance after Wire Bonding	Quality Check of Wire Bonding
	◇PQC Level Check		Pull Strength, Compresion Width, Shear Strength	Prevention of Open and Short
	□Inspection after Assembling		Appearance after Assembling	
	◇PQC Lot Judgement			
Package				
	○Sealing	Sealing	Appearance after Sealing Outline, Dimension	Guarantee of Appearance and Dimension
	◇PQC Level Check	Marking	Marking Strength	
	○Final Electrical Inspection			
	◇Failure Analysis		Analysis of Failures, Failure Mode, Mechanism	Feedback of Analysis Information
	□Appearance Inspection			
	△Sampling Inspection on Products			
	○Receiving			
	↓Shipment			

Fig. 3 Example of Inner Process Quality Control

department for products which were judged good in 100% test . . . the final process in manufacturing. Though 100% yield is expected, sampling inspection is executed to prevent mixture of bad product by mistake. The inspection is executed not only to confirm that the products have met the users' requirements but also to consider potential quality factors. Lot inspection is executed based on MIL-STD-105D.

(2) Reliability Assurance Tests

To assure the reliability of semiconductor devices, reliability tests and tests on individual manufacturing lots that are required by the user, are periodically performed.

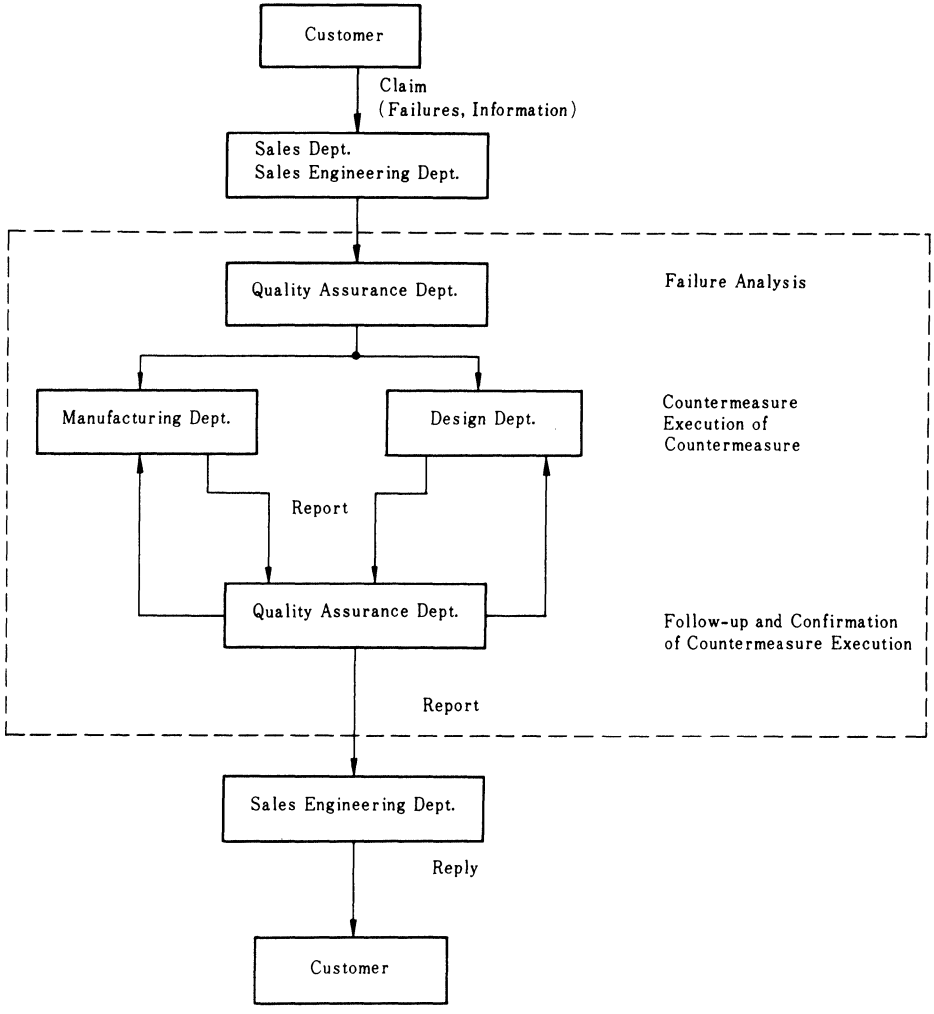


Fig. 4 Process Flow Chart of Field Failure

4. RELIABILITY

4.1 Structure

10K ECL features high integration and speed provided by its vertical structure and collector dot system, multilayer interconnection, and shallow in process diffusion technique. Hitachi's 3μm interconnection and oxidation film separation process assures high reliability due to improved temperature and voltage compensation. Fig. 5 shows a cross-section of 10K and 100K ECL structures.

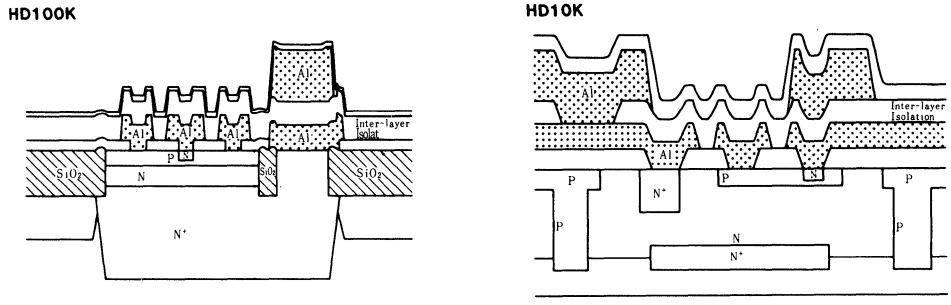


Fig. 5 Cross-section of 10K and 100K ECL structures.

IC chips are produced in Cerdip, Flat, and Ceramic packages. Leadless Chip Carrier (LCC) packaging to increase density is currently under development. These airtight structures are suitable for high reliability system requirements.

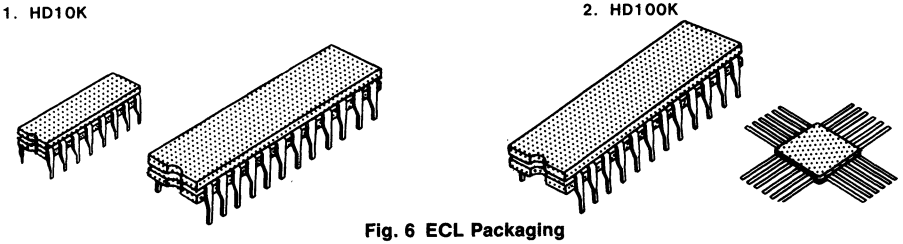


Fig. 6 ECL Packaging

5. RELIABILITY DATA

Examples of reliability test results at Hitachi are shown below.

5.1 Reliability data for 100K ECL

Reliability test data for HD100101, HD100130, and HD100160 are shown in Tables 2 and 3.

Table 2 Reliability Test Results on 100K ECL (1)

Items	HD10010IF					
	Test Condition	Number of Samples	Total Test Period (hours)	Number of Failures	Failure Rate*	
High Temperature Operation	$Ta=125°C$ $V_{EE}=-4.5V$	100pcs	3.7×10^5	0	2.5×10^{-6}	
	$Ta=150°C$ $V_{EE}=-4.5V$	100pcs	2.0×10^5	1 *1	1.0×10^{-5}	*1 Electrostatic destruction
High Temperature Storage	$Ta=150°C$	60pcs	1.2×10^4	0	7.7×10^{-6}	
	$Ta=200°C$	30pcs	6.0×10^4	0	1.5×10^{-5}	
Thermal Fatigue	$Ta=25°C$ $V_{EE}=-5.2V$ ON/OF= 10minutes/10minutes	40pcs	4×10^4 (cycles, pcs)	0	—	

* Reliability level 60%

Table 2 Reliability Test Results of ECL100K (2)

Items	HD100130F				
	Test Condition	Number of Samples	Total Test Period (hours)	Number of Failures	Failure Rate*
High Temperature Operation	$Ta=125°C$ $V_{EE}=-4.5V$	100pcs	1.0×10^5	0	9.2×10^{-6}
	$Ta=150°C$ $V_{EE}=-4.5V$	—	—	—	—
High Temperature Storage	$Ta=150°C$	—	—	—	—
	$Ta=200°C$	30pcs	3.0×10^4	0	3.1×10^{-5}
Thermal Fatigue	$Ta=25°C$ $V_{EE}=-5.2V$ ON/OF= 10minutes/10minutes	—	—	—	—

Table 2 Reliability Test Results of ECL100K (3)

Items	HD100160F				
	Test Condition	Number of Samples	Total Test Period (hours)	Number of Failures	Failure Rate*
High Temperature Operation	$Ta=125°C$ $V_{EE}=-4.5V$	—	—	—	—
	$Ta=150°C$ $V_{EE}=-4.5V$	100pcs	1.0×10^5	0	9.2×10^{-6}
High Temperature Storage	$Ta=150°C$	—	—	—	—
	$Ta=200°C$	30pcs	3.0×10^4	0	3.1×10^{-4}
Thermal Fatigue	$Ta=25°C$ $V_{EE}=-5.2V$ ON/OF= 10minutes/10minutes	50pcs	5×10^5 (cycles·pcs)	0	—

Table 2 Reliability Test Results of ECL100K (4)

Items	HD100101 (Cerdip)				
	Test Condition	Number of Samples	Total Test Period (hours)	Number of Failures	Failure Rate*
High Temperature Operation	$Ta=125°C$ $V_{EE}=-4.5V$	100pcs	2.0×10^5	0	4.6×10^{-6}
	$Ta=150°C$ $V_{EE}=-4.5V$	100pcs	2.0×10^5	0	4.6×10^{-6}
High Temperature Storage	$Ta=150°C$	50pcs	1.0×10^5	0	9.2×10^{-6}
	$Ta=200°C$	30pcs	6.0×10^4	0	1.5×10^{-5}
Thermal Fatigue	$Ta=25°C$ $V_{EE}=-5.2V$ ON/OF= 10minutes/10minutes	30pcs	3×10^4 (cycles·pcs)	0	—

* Reliability level 60%

Table 3 Reliability Test Results of ECL100K (1)

Items	Test Condition	HD100101/HD100130F		HD100101/HD100160 (Cerdip)	
		Number of Samples	Number of Failures	Number of Samples	Number of Failures
Temperature Cycle	−65°C ~ RT ~ +150°C 10cycles	100	0	100	0
Soldering Heat Resistivity	260°C, 10sec	50	0	50	0
Thermal Shock	0°C ~ 100°C 10cycles	50	0	50	0
Drop Shock	1,500G, 0.5ms 3times each on X, Y and Z	30	0	30	0
Variable Frequency Vibration	100 ~ 2,000Hz, 20G 3times each on X, Y and Z	30	0	30	0
Constant Acceleration	20,000G 1minute each on X, Y and Z	30	0	30	0

5.2 Reliability data on 10K ECL

Examples of 10K ECL (HD10101 and HD10136) reliability test data are shown in Tables 4 and 5.

Table 4 Reliability Test Results on 10K ECL (1)

Items	HD10101				
	Test Condition	Number of Sambles	Total Test Period (hours)	Number of Failures	Failure Rate*
High Temperature Operation	$Ta=125°C$ $V_{EE}=-5.2V$	200pcs	4.5×10^5	0	2.3×10^{-6}
	$Ta=150°C$ $V_{EE}=-5.2V$	120pcs	2.4×10^5	0	3.8×10^{-6}
High Temperature Storage	$Ta=150°C$	38pcs	7.6×10^4	0	1.2×10^{-5}
	$Ta=200°C$	22pcs	4.4×10^4	0	2.1×10^{-5}

* Reliability level 60%

Reliability Test Results on 10K ECL (2)

Items	HD10136				
	Test Condition	Number of Samples	Total Test Period (hours)	Number of Failures	Failure Rate*
High Temperature Operation	$Ta=125°C$ $V_{EE}=-5.2V$	100pcs	2.0×10^5	0	4.6×10^{-6}
	$Ta=150°C$ $V_{EE}=-5.2V$	75pcs	1.5×10^5	0	6.1×10^{-6}
High Temperature Storage	$Ta=150°C$	38pcs	7.6×10^4	0	1.2×10^{-5}
	$Ta=200°C$	22pcs	4.4×10^4	0	2.1×10^{-4}

* Reliability level 60%

Table 5 Reliability Test Results on 10K ECL (1)

Items	Test Condition	HD10101		HD10136	
		Number of Samples	Number of Failures	Number of Samples	Number of Failures
Temperature Cycle	−65°C～RT～+150°C 10cycle	150	0	100	0
Soldering Heat Resistivity	260°C, 10sec.	22	0	22	0
Thermal Shock	0°C～100°C 10cycles	45	0	45	0
Drop Shock	1500G, 0.5ms 3 times each on X, Y and Z	38	0	38	0
Variable Frequency Vibration	100～2,000Hz, 20G 3 times each on X, Y and Z	38	0	38	0
Constant Acceleration	20,000G 1 minute each or X, Y and Z	38	0	38	0

5.3 Characteristics Change

Fundamental parameters of change in ECL are h_{FE} and I_{CBO} of transistors, and parasitic leakage paths. In device design, structures are employed and operating conditions are chosen to suppress these degradations, so that they rarely occur under average operating conditions.

AC characteristic changes in HD100101 and HD10101 are shown in Fig. 7 and 8.

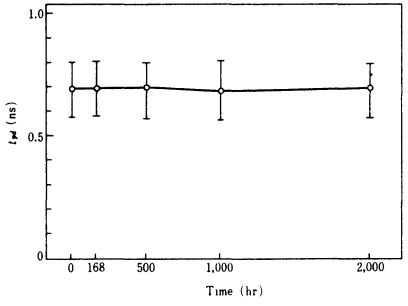


Fig.7 t_{pd} Change of HD100101

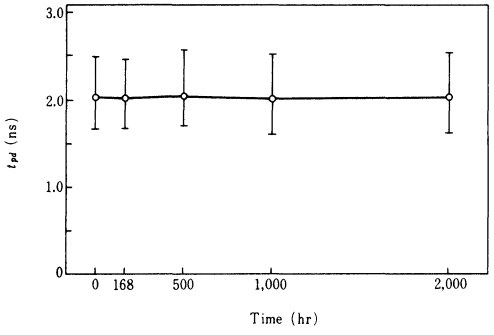


Fig.8 t_{pd} Change of HD10101

5.4 Field Failure Mode

Examples of field failures are shown in Fig. 9 and 10. The fine lithographic techniques employed in manufacturing 10K ECL have resulted in some failures caused by pinholes, photoresist and foreign materials. In 100K ECL, high reliability processing has significantly reduced such failures.

At Hitachi, potential defects are eliminated in the manufacturing process, and 100% screening tests are performed. Analysis of field failure data supplied by users provides effective feedback for the improvement of product design and manufacture.

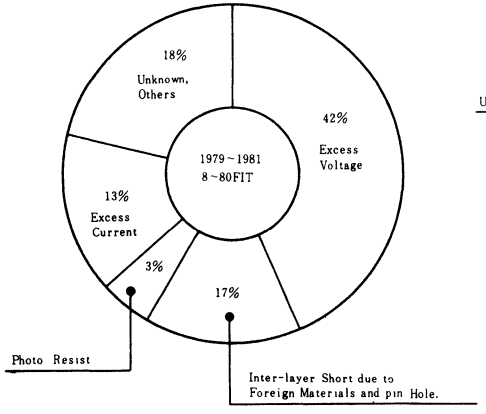


Fig. 9 Field Failure Mode in 10K ECL

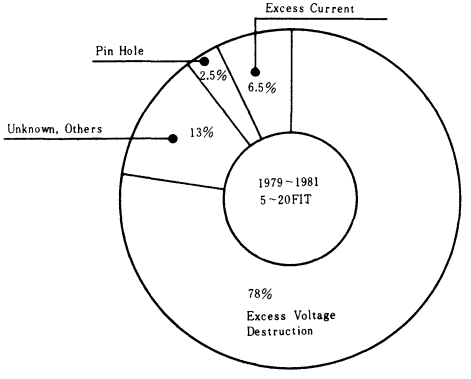


Fig. 10 Field Failure Mode in 100K ECL

HANDLING PRECAUTIONS

Precautions given below for handling ECL IC's will assist the designer in achieving optimum circuit designs, and prevent device malfunction.

1. Precaution Against Electrostatic Charge

The double layer structure and shallow diffusion techniques required for high integration and high speed of ECL products reduce the margin of protection against electrostatic destruction. Greater caution must be provided in handling ECL products, and the following measures are recommended:

(1) Keep all device terminals in a conductive mat to maintain equi-potential during transportation and storage. A conductive mat called "MOSPAK" is commercially available. Unless otherwise specified, all Hitachi ECL's are shipped in plastic magazines. These should not be re-used because re-use greatly diminishes the effectiveness of electrostatic protection.

(2) When handling IC's for inspection or connection, grounding must be provided as shown in Figure 1. The 1M ohm resistor protects the handler from electric shock.

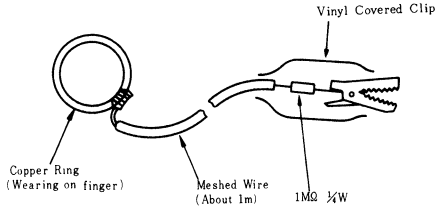


Fig.1 An Example of Grounding to Human Body

(3) Control the ambient relative humidity at about 50 per cent.

(4) Wear cotton clothes instead of synthetic fabrics.

(5) We recommend grounding the tip of solder irons which operate at low voltage (12V or 24V). Grounding of any equipment employed in testing and measurement is also recommended.

(6) Pack IC's mounted on circuit boards in conductive mats.

2. Prevention of Reverse Insertion

Marking of No. 1 pin is clearly stamped on the device package to prevent incorrect insertion of IC's.

3. Mounting and Removal of IC's with Voltage Applied

If IC's are inserted or removed from a board when voltage is applied, the voltage induced at current on/off can destroy the IC's. Mount and remove IC's with power removed. The same precaution is necessary in measurements using a tester.

4. Prevention of Oscillation

ECL Bipolar memory has a high transistor cutoff frequency. Sometimes oscillation is caused by the external circuit, and IC misoperation occurs. In such cases, a high frequency capacitor (0.1μF) is recommended between the IC's ground and voltage supply line.

5. Precaution on Simple "H" Level

If an IC's input is grounded to fix input level at "H," misoperation sometimes occurs due to the internal circuit composition. "H" and "L" input levels are specified V_{IL} (min.) and V_{IH} (max.), respectively. Please refer to these specifications to properly utilize IC's.

6. Cooling

ECL power dissipation is 90mW to 500mW in 10K, and 100mW to 700mW in 100K products. When many ECL's are mounted on a board, forced air cooling may be required. In addition, cooling will improve reliability as shown in Figure 2.

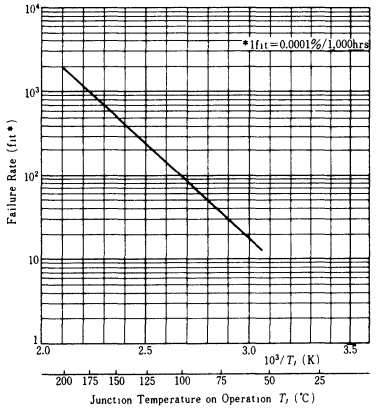


Fig.2 Example of derating of ECL

7. Other Precautions

(1) Deforming of magazine and carrier:
Plastic magazine and carrier material for ECL flat packages is usually thermo-plastic, which deforms at temperatures higher than 40 to 50° C. If burn-in occurs in the field, use an aluminum magazine or other metal type fixture.

(2) Shock in transportation:
Normal handling tests and drop tests (JIS-C7021 A-8) on individual glass-sealed devices indicate no damage. However, strong shock received during transportation or loading of devices packed in magazines may cause damage. Even after devices are board-mounted, IC packages may be damaged if the board strength is insufficient to withstand strong deforming stress. Please contact Hitachi or its representatives regarding handling and transportation of Hitachi devices.

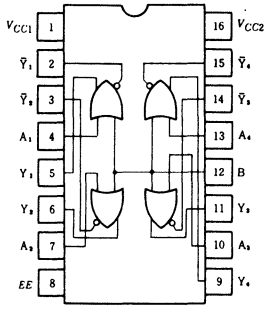
DATA SHEETS

HD10K Series

HD10101

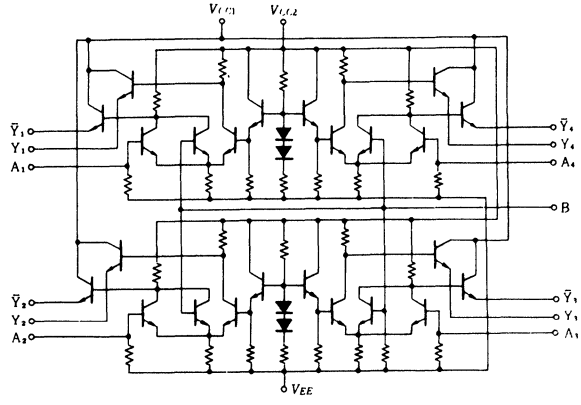
Quardruple OR/NOR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	20	26	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	A input	25°C	—	—	265	μA
			B input		—	—	535	
	I_{IL}	$V_{IL}=-1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$		25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$		25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$		−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$		25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$		−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$		25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$		85°C	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

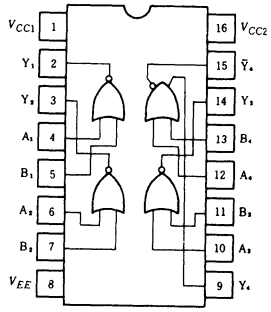
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.0	—	3.3	
	t_{PHL}		−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.0	—	3.3	
Rise/Fall Time	t_{TLH}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	
	t_{THL}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	

Note) Please refer to test circuit and waveform of common item.

HD10102

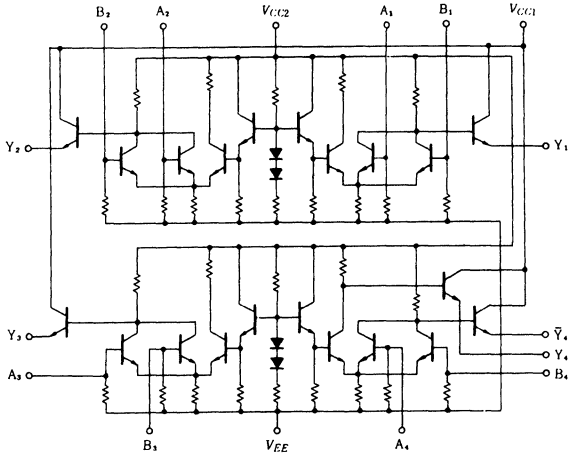
Quadruple 2-input NOR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	20	26	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	25°C	—	—	265	μA
	I_{IL}	$V_{IL}=-1.850V$	25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$	−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$	25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$	85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$	−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$	25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$	−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$	25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$	85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$	−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$	25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$	85°C	—	—	−1.595	

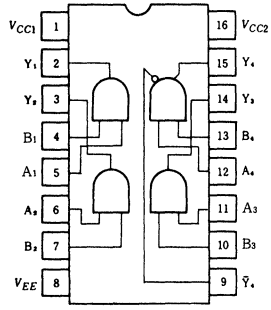
■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.0	—	3.3	
	t_{PHL}		−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.0	—	3.3	
Rise/Fall Time	t_{TLH}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	
	t_{THL}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	

Note) Please refer to test circuit and waveform of common item.

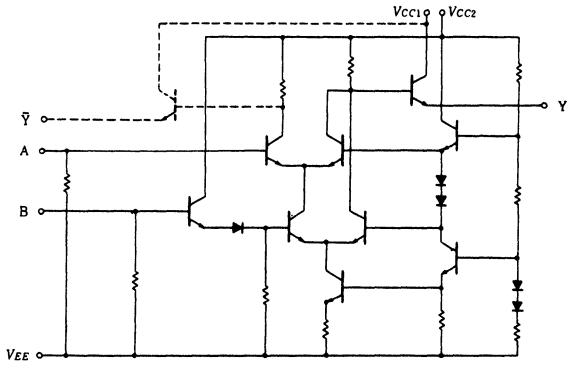
Quadruple 2-input AND Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC (¼)



■DC CHARACTERISTICS ($V_{EE}=-5.2$V, $Ta=-30\sim+85$℃)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25℃	—	28	35	mA
Input Current	I_{IH}	$V_{IH}=-0.810$V, B input $=-0.810$V	A input	25℃	—	—	265	μA
		$V_{IH}=-0.810$V	B input		—	—	220	
	I_{IL}	$V_{IL}=-1.850$V		25℃	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890$V or $V_{IL}=-1.890$V		−30℃	−1.060	—	−0.890	V
		$V_{IH}=-0.810$V or $V_{IL}=-1.850$V		25℃	−0.960	—	−0.810	
		$V_{IH}=-0.700$V or $V_{IL}=-1.825$V		85℃	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890$V or $V_{IH}=-0.890$V		−30℃	−1.890	—	−1.675	V
		$V_{IL}=-1.850$V or $V_{IH}=-0.810$V		25℃	−1.850	—	−1.650	
		$V_{IL}=-1.825$V or $V_{IH}=-0.700$V		85℃	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IH}=-0.890$V, $V_{IHA}=-1.205$V or $V_{ILA}=-1.500$V		−30℃	−1.080	—	—	V
		$V_{IH}=-0.810$V, $V_{IHA}=-1.105$V or $V_{ILA}=-1.475$V		25℃	−0.980	—	—	
		$V_{IH}=-0.700$V, $V_{IHA}=-1.035$V or $V_{ILA}=-1.440$V		85℃	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500$V or $V_{IH}=-0.890$V, $V_{IHA}=-1.205$V		−30℃	—	—	−1.655	V
		$V_{ILA}=-1.475$V or $V_{IH}=-0.810$V, $V_{IHA}=-1.105$V		25℃	—	—	−1.630	
		$V_{ILA}=-1.440$V or $V_{IH}=-0.700$V, $V_{IHA}=-1.105$V		85℃	—	—	−1.595	

■AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30 ~ +85°C)

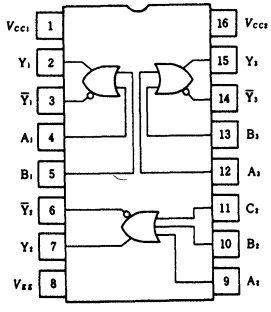
Item	Symbol	Test Condition			min	typ	max	Unit
Propagation Delay Time	t_{PLH}	A input	R_L = 50Ω	−30°C	1.0	—	4.3	ns
				25°C	1.0	2.2	4.0	
				85°C	1.0	—	4.2	
		B input		−30°C	1.0	—	4.3	
				25°C	1.0	2.7	4.0	
				85°C	1.0	—	4.2	
	t_{PHL}	A input		−30°C	1.0	—	4.3	ns
				25°C	1.0	2.2	4.0	
				85°C	1.0	—	4.2	
		B input		−30°C	1.0	—	4.3	
				25°C	1.0	2.7	4.0	
				85°C	1.0	—	4.2	
Rise/Fall Time	t_{TLH}	A, B input		−30°C	1.5	—	3.7	ns
				25°C	1.5	2.0	3.5	
				85°C	1.5	—	3.6	
	t_{THL}			−30°C	1.5	—	3.7	ns
				25°C	1.5	2.0	3.5	
				85°C	1.5	—	3.6	

Note) Please refer to test circuit and waveform of common item.

HD10105

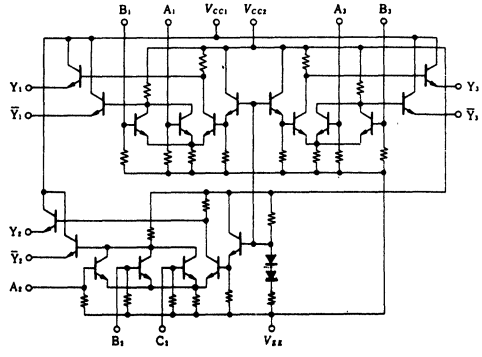
Triple 2-3-2-input OR/NOR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	17	21	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	25°C	—	—	265	μA
	I_{IL}	$V_{IL}=-1.850V$	25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$	−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$	25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$	85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$	−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$	25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$	−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$	25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$	85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$	−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$	25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$	85°C	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

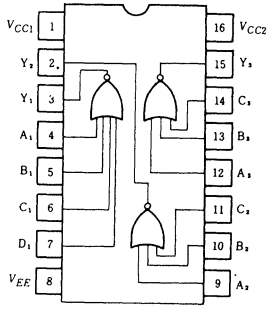
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.0	—	3.3	
	t_{PHL}		−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.0	—	3.3	
Rise/Fall Time	t_{TLH}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	
	t_{THL}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	

Note) Please refer to test circuit and waveform of common item.

HD10106

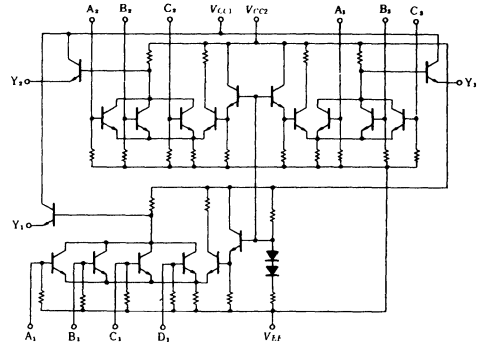
Triple 4-3-3-input NOR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2$V, $Ta=-30\sim+85$°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	17	21	mA
Input Current	I_{IH}	$V_{IH}=-0.810$V	25°C	—	—	265	μA
	I_{IL}	$V_{IL}=-1.850$V	25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IL}=-1.890$V	−30°C	−1.060	—	−0.890	V
		$V_{IL}=-1.850$V	25°C	−0.960	—	−0.810	
		$V_{IL}=-1.825$V	85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IH}=-0.890$V	−30°C	−1.890	—	−1.675	V
		$V_{IH}=-0.810$V	25°C	−1.850	—	−1.650	
		$V_{IH}=-0.700$V	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{ILA}=-1.500$V	−30°C	−1.080	—	—	V
		$V_{ILA}=-1.475$V	25°C	−0.980	—	—	
		$V_{ILA}=-1.440$V	85°C	−0.910	—	—	
	V_{OLA}	$V_{IHA}=-1.205$V	−30°C	—	—	−1.655	V
		$V_{IHA}=-1.105$V	25°C	—	—	−1.630	
		$V_{IHA}=-1.035$V	85°C	—	—	−1.595	

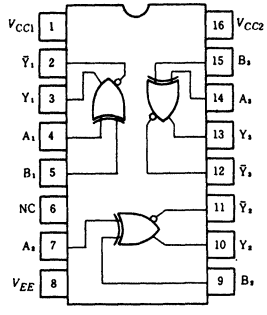
■AC CHARACTERISTICS ($V_{EE}=-3.2$V, $V_{CC}=-2.0$V, $Ta=-30\sim+85$°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.0	—	3.3	
	t_{PHL}		−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.0	—	3.3	
Rise/Fall Time	t_{TLH}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	
	t_{THL}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	

Note) Please refer to test circuit and waveform of common item.

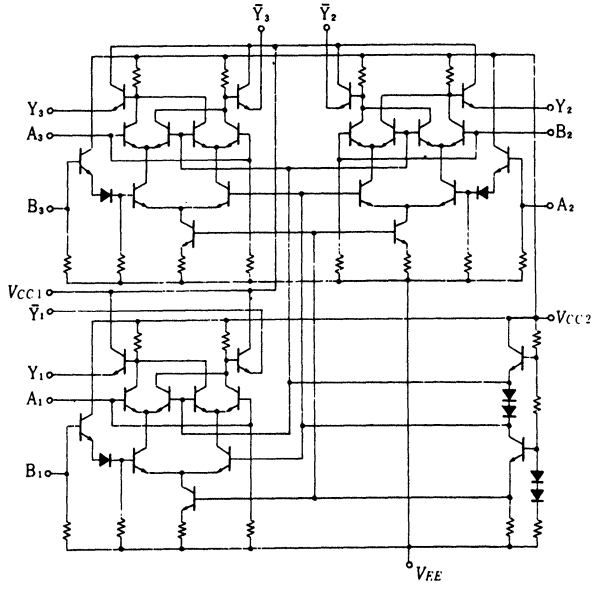
Triple 2-input Exclusive-OR/Exclusive-NOR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All inputs=−0.810V		25°C	—	—	28	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	A input	25°C	—	—	265	μA
			B input		—	—	220	
	I_{IL}	$V_{IL}=-1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$		25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$		25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$		−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$		25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$		−30°C	—	—	−1.655	V
		$V_{ILA}=-1,475V$ or $V_{IHA}=-1.105V$		25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$		85°C	—	—	−1.595	

■AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30 ~ +85°C)

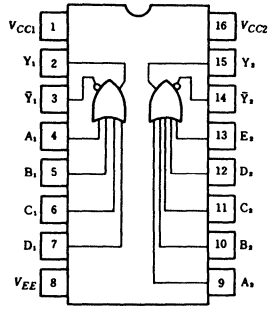
Item	Symbol	Test Condition			min	typ	max	Unit
Propagation Delay Time	t_{PLH}	A input	R_L = 50Ω	−30°C	1.1	—	3.8	ns
				25°C	1.1	2.0	3.7	
				85°C	1.1	—	4.0	
		B input		−30°C	1.1	—	3.8	
				25°C	1.1	2.8	3.7	
				85°C	1.1	—	4.0	
	t_{PHL}	A input		−30°C	1.1	—	3.8	ns
				25°C	1.1	2.0	3.7	
				85°C	1.1	—	4.0	
		B input		−30°C	1.1	—	3.8	
				25°C	1.1	2.8	3.7	
				85°C	1.1	—	4.0	
Rise/Fall Time	t_{TLH}	A, B input		−30°C	1.1	—	3.5	ns
				25°C	1.1	2.5	3.5	
				85°C	1.1	—	3.8	
	t_{THL}			−30°C	1.1	—	3.5	ns
				25°C	1.1	2.5	3.5	
				85°C	1.1	—	3.8	

Note) Please refer to test circuit and waveform of common item.

HD10109

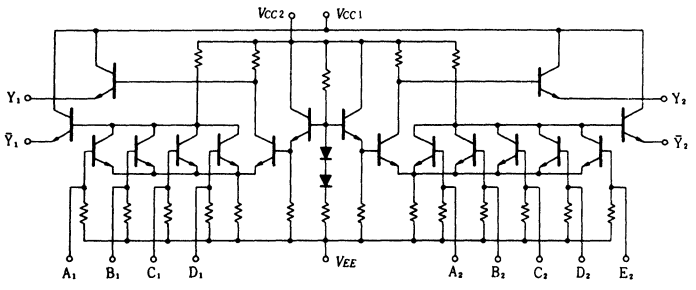
Dual 4-5-input OR/NOR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	11	14	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	25°C	—	—	265	μA
	I_{IL}	$V_{IL}=-1.850V$	25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$	−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$	25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$	85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$	−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$	25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$	−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$	25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$	85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$	−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$	25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$	85°C	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

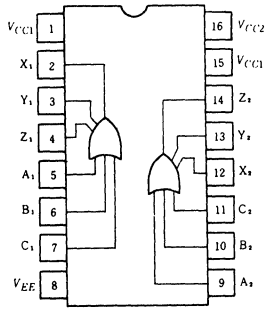
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.0	—	3.3	
	t_{PHL}		−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.0	—	3.3	
Rise/Fall Time	t_{TLH}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	
	t_{THL}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	

Note) Please refer to test circuit and waveform of common item.

HD10110

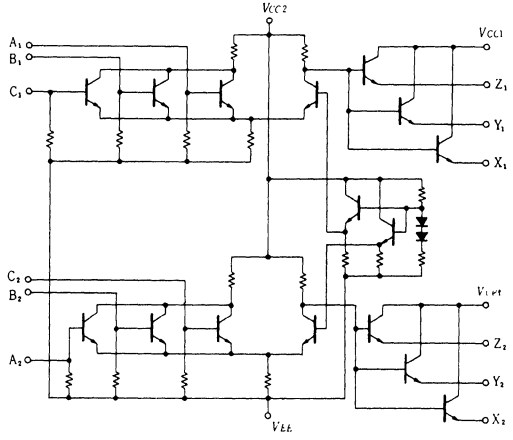
Dual 3-input 3-output OR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	30	38	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	25°C	—	—	425	μA
	I_{IL}	$V_{IL}=-1.850V$	25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$	−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$	25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$	85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$	−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$	25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$	−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$	25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$	85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$	−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$	25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$	85°C	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

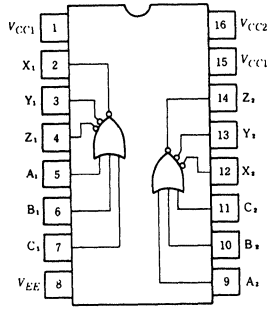
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	−30°C	1.4	—	3.5	ns
			25°C	1.4	2.4	3.5	
			85°C	1.5	—	3.8	
	t_{PHL}		−30°C	1.4	—	3.5	ns
			25°C	1.4	2.4	3.5	
			85°C	1.5	—	3.8	
Rise/Fall Time	t_{TLH}		−30°C	1.0	—	3.5	ns
			25°C	1.1	2.2	3.5	
			85°C	1.2	—	3.8	
	t_{THL}		−30°C	1.0	—	3.5	ns
			25°C	1.1	2.2	3.5	
			85°C	1.2	—	3.8	

Note) Please refer to test circuit and waveform of common item.

HD10111

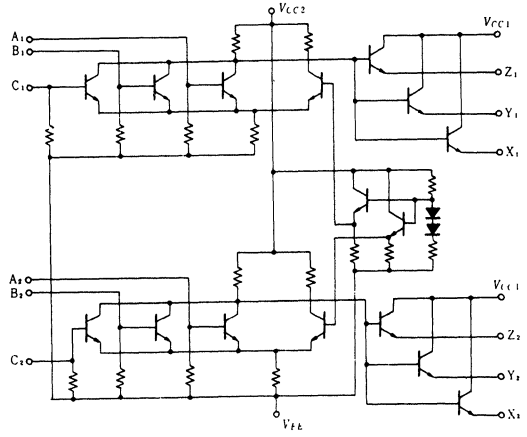
Dual 3-input 3-output NOR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	—	38	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	25°C	—	—	425	μA
	I_{IL}	$V_{IL}=-1.850V$	25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IL}=-1.890V$	−30°C	−1.060	—	−0.890	V
		$V_{IL}=-1.850V$	25°C	−0.960	—	−0.810	
		$V_{IL}=-1.825V$	85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IH}=-0.890V$	−30°C	−1.890	—	−1.675	V
		$V_{IH}=-0.810V$	25°C	−1.850	—	−1.650	
		$V_{IH}=-0.700V$	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{ILA}=-1.500V$	−30°C	−1.080	—	—	V
		$V_{ILA}=-1.475V$	25°C	−0.980	—	—	
		$V_{ILA}=-1.440V$	85°C	−0.910	—	—	
	V_{OLA}	$V_{IHA}=-1.205V$	−30°C	—	—	−1.655	V
		$V_{IHA}=-1.105V$	25°C	—	—	−1.630	
		$V_{IHA}=-1.035V$	85°C	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

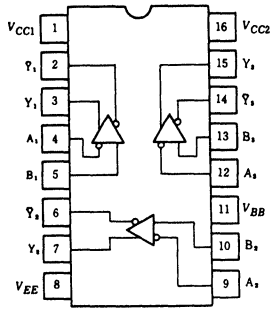
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	−30°C	1.4	—	3.5	ns
			25°C	1.4	2.4	3.5	
			85°C	1.5	—	3.8	
	t_{PHL}		−30°C	1.4	—	3.5	ns
			25°C	1.4	2.4	3.5	
			85°C	1.5	—	3.8	
Rise/Fall Time	t_{TLH}		−30°C	1.0	—	3.5	ns
			25°C	1.1	2.2	3.5	
			85°C	1.2	—	3.8	
	t_{THL}		−30°C	1.0	—	3.5	ns
			25°C	1.1	2.2	3.5	
			85°C	1.2	—	3.8	

Note) Please refer to test circuit and waveform of common item.

Triple Line Receivers

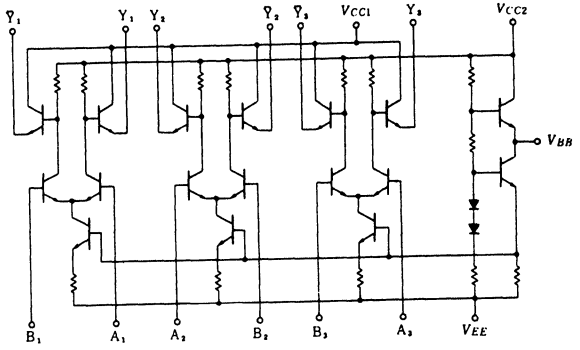
The HD10116 is designed for use in sensing differential signals over long lines. The bias supply (V_{BB}) is made available to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary. Active current source provides these receivers with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} to prevent upsetting the current source bias network.

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}*		25°C	—	17	21	mA
Input Current	I_{IH}**	$V_{IH}=-0.810V$	25°C	—	—	95	μA
	I_{CBO}**	$V_{IN}=-5.2V$	25°C	—	—	1.0	μA
Output Voltage	V_{OH}***	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$	−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$	25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$	85°C	−0.890	—	−0.700	
	V_{OL}***	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$	−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$	25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}***	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$	−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$	25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$	85°C	−0.910	—	—	
	V_{OLA}***	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$	−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$	25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$	85°C	—	—	−1.595	
Reference Voltage	V_{BB}		−30°C	−1.420	—	−1.280	V
			25°C	−1.350	—	−1.230	
			85°C	−1.295	—	−1.150	

* Bn input is connected to V_{BB} and V_{IL} min is supplied to An input.
** Bn input is connected to V_{BB} and V_{IL} min is supplied to A input.
*** Other inputs are connected to V_{BB} and each one input of other receiver is connected to V_{BB}.

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$, Other inputs $=V_{BB}$	−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.1	—	3.3	
	t_{PHL}		−30°C	1.0	—	3.1	ns
			25°C	1.0	2.0	2.9	
			85°C	1.1	—	3.3	
Rise/Fall Time	t_{TLH}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	
	t_{THL}		−30°C	1.1	—	3.6	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.7	

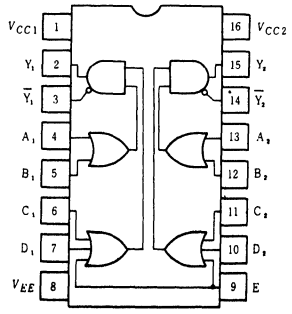
Note) Please refer to test circuit and waveform of common item.

Dual 2-wide 2-3-input OR-AND/OR-AND-INVERT Gates

The HD10117 is designed for use as a data control of digital Multiplexer, data distribution and etc..

The E input (pin 9) is the common input of dual gates.

■PIN ARRANGEMENT



(Top View)

■DC CHARACTERISTICS (V_{EE}=−5.2V, Ta=−30~+85°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	20	26	mA
Input Current	I_{IH}	V_{IH}=−0.810V	E input	25°C	—	—	350	μA
			Other inputs		—	—	265	
	I_{IL}	V_{IL}=−1.850V		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	V_{IH}=−0.890V or V_{IL}=−1.890V		−30°C	−1.060	—	−0.890	V
		V_{IH}=−0.810V or V_{IL}=−1.850V		25°C	−0.960	—	−0.810	
		V_{IH}=−0.700V or V_{IL}=−1.825V		85°C	−0.890	—	−0.700	
	V_{OL}	V_{IL}=−1.890V or V_{IH}=−0.890V		−30°C	−1.890	—	−1.675	V
		V_{IL}=−1.850V or V_{IH}=−0.810V		25°C	−1.850	—	−1.650	
		V_{IL}=−1.825V or V_{IH}=−0.700V		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	V_{IHA}=−1.205V or V_{ILA}=−1.500V		−30°C	−1.080	—	—	V
		V_{IHA}=−1.105V or V_{ILA}=−1.475V		25°C	−0.980	—	—	
		V_{IHA}=−1.035V or V_{ILA}=−1.440V		85°C	−0.910	—	—	
	V_{OLA}	V_{ILA}=−1.500V or V_{IHA}=−1.205V		−30°C	—	—	−1.655	V
		V_{ILA}=−1.475V or V_{IHA}=−1.105V		25°C	—	—	−1.630	
		V_{ILA}=−1.440V or V_{IHA}=−1.035V		85°C	—	—	−1.595	

■AC CHARACTERISTICS (V_{EE}=−3.2V, V_{CC}=+2.0V, Ta=−30~+85°C)

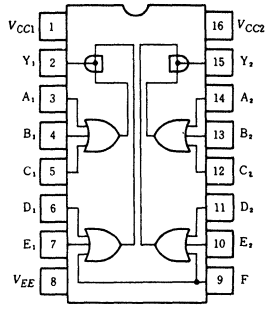
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	R_L=50Ω	−30°C	1.4	—	3.9	ns
			25°C	1.4	2.3	3.4	
			85°C	1.4	—	3.8	
	t_{PHL}		−30°C	1.4	—	3.9	ns
			25°C	1.4	2.3	3.4	
			85°C	1.4	—	3.8	
Rise/Fall Time	t_{TLH}		−30°C	0.9	—	4.1	ns
			25°C	1.1	2.2	4.0	
			85°C	1.1	—	4.6	
	t_{THL}		−30°C	0.9	—	4.1	ns
			25°C	1.1	2.2	4.0	
			85°C	1.1	—	4.6	

Note) Please refer to test circuit and waveform of common item.

HD10118

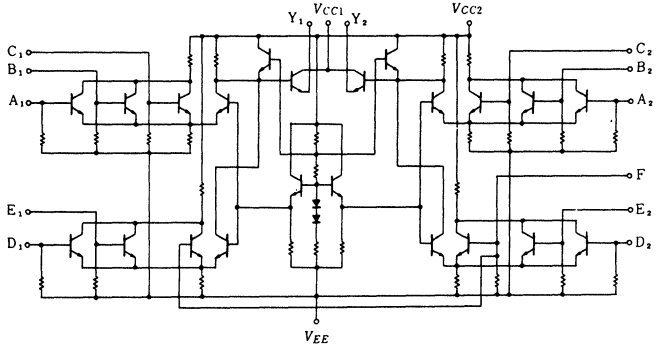
Dual 2-wide 3-input OR-AND Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	20	26	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	F input	25°C	—	—	370	μA
			Other inputs		—	—	265	
	I_{IL}	$V_{IL}=-1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$		25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$		−30°C	−2.000	—	−1.675	V
		$V_{IL}=-1.850V$		25°C	−1.990	—	−1.650	
		$V_{IL}=-1.825V$		85°C	−1.920	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$		−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$		25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$		−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$		25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$		85°C	—	—	−1.595	

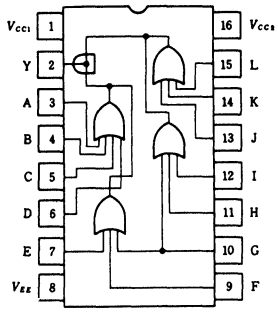
■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	−30°C	1.4	—	3.9	ns
			25°C	1.4	2.3	3.4	
			85°C	1.4	—	3.8	
	t_{PHL}		−30°C	1.4	—	3.9	ns
			25°C	1.4	2.3	3.4	
			85°C	1.4	—	3.8	
Rise/Fall Time	t_{TLH}		−30°C	0.8	—	4.1	ns
			25°C	1.5	2.5	4.0	
			85°C	1.5	—	4.6	
	t_{THL}		−30°C	0.8	—	4.1	ns
			25°C	1.5	2.5	4.0	
			85°C	1.5	—	4.6	

Note) Please refer to test circuit and waveform of common item.

4-wide 4-3-3-3-input OR-AND Gate

■PIN ARRANGEMENT



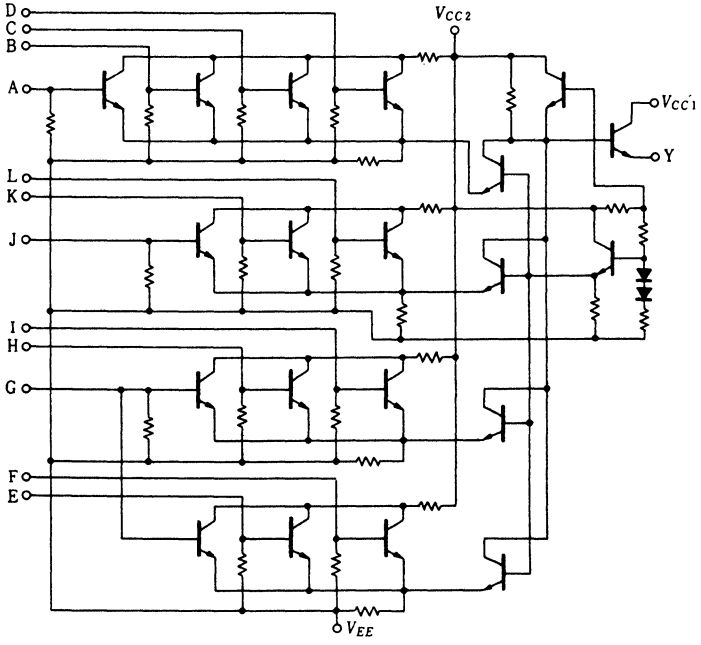
(Top View)

■FUNCTION TABLE

Inputs												Outputs
A	B	C	D	E	F	G	H	I	J	K	L	Y
L	L	L	L	×	×	×	×	×	×	×	×	L
×	×	×	×	L	L	L	×	×	×	×	×	L
×	×	×	×	×	×	L	L	L	×	×	×	L
×	×	×	×	×	×	×	×	×	L	L	L	L
Notes 1												H

Notes) 1. Each input of OR gates are combined to high.
2. X: Don't Care

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	20	26	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	G input	25°C	—	—	370	μA
			Other inputs		—	—	265	
	I_{IL}	$V_{IL}=-1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$		25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$		25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$		−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$		25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$		−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$		25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$		85°C	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

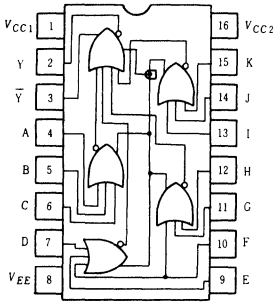
Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	−30°C	1.4	—	3.9	ns
			25°C	1.4	2.3	3.4	
			85°C	1.4	—	3.8	
	t_{PHL}		−30°C	1.4	—	3.9	ns
			25°C	1.4	2.3	3.4	
			85°C	1.4	—	3.8	
Rise/Fall Time	t_{TLH}		−30°C	0.8	—	4.1	ns
			25°C	1.5	2.5	4.0	
			85°C	1.5	—	4.6	
	t_{THL}		−30°C	0.8	—	4.1	ns
			25°C	1.5	2.5	4.0	
			85°C	1.5	—	4.6	

Note) Please refer to test circuit and waveform of common item.

HD10121

4-wide OR-AND/OR-AND-INVERT Gate

■PIN ARRANGEMENT



(Top View)

■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	20	26	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	F input	25°C	—	—	370	μA
			Other inputs		—	—	265	
	I_{IL}	$V_{IL}=-1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$		25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$		25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$		−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$		25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$		−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$		25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$		85°C	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50\Omega$	−30°C	1.4	—	3.9	ns
			25°C	1.4	2.3	3.4	
			85°C	1.4	—	3.8	
	t_{PHL}		−30°C	1.4	—	3.9	ns
			25°C	1.4	2.3	3.4	
			85°C	1.4	—	3.8	
Rise/Fall Time	t_{TLH}		−30°C	0.9	—	4.1	ns
			25°C	1.1	2.5	4.0	
			85°C	1.1	—	4.6	
	t_{THL}		−30°C	0.9	—	4.1	ns
			25°C	1.1	2.5	4.0	
			85°C	1.1	—	4.6	

Note) Please refer to test circuit and waveform of common item.

HD10124

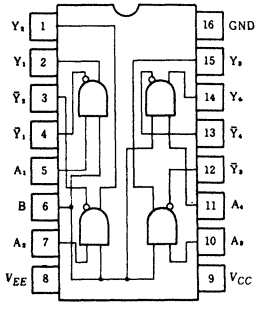
Quadruple TTL to ECL Translators

The HD10124 is a quad translator for interfacing data and control signals between a saturated logic section and the ECL section of digital systems. The device has TTL compatible inputs, and ECL complementary open-emitter outputs that allow use as an inverting/noninverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to a ECL high logic state.

Power supply requirements are ground, +5.0V, and −5.2V. The DC levels are standard or Schottky TTL in, ECL 10K out.

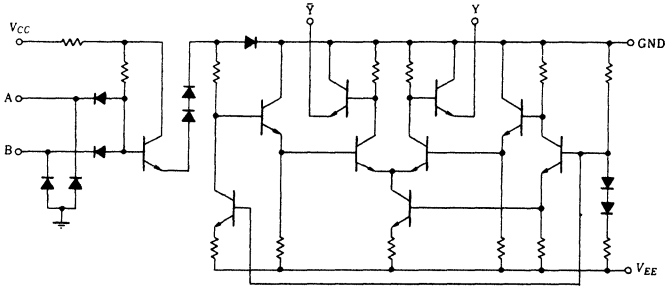
An advantage of this device is that TTL level information can be transmitted differentially, via balanced twisted pair lines, to the ECL equipment, where the signal can be received by any of the ECL receivers or the HD10125 ECL to TTL translator.

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



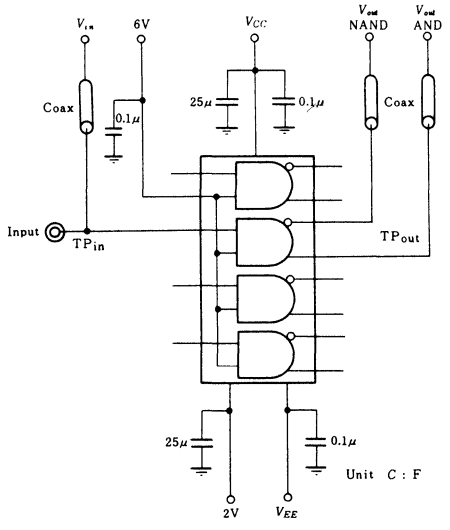
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $V_{CC}=+5.0V$, $Ta=-30\sim+85°C$)

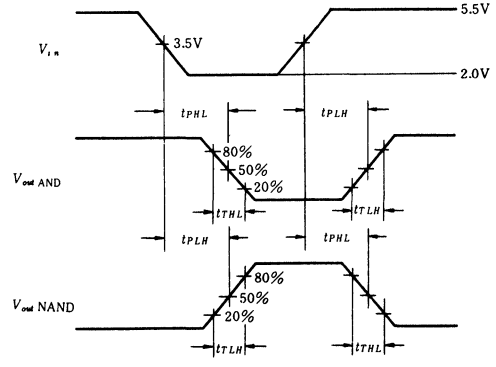
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	—	66	mA
	I_{CCH}	All inputs=4V		25°C	—	—	16	mA
	I_{CCL}	All inputs=0V		25°C	—	—	25	mA
Input Current	I_{IH}	$V_{IN}=2.4V$, Other inputs=0.4V	A input	25°C	—	—	50	μA
			B input		—	—	200	
	I_{IL}	$V_{IN}=0.4V$, Other inputs=4V	A input	25°C	−3.2	—	—	mA
			B input		−12.8	—	—	
	I_I	$V_{IN}=5.5V$, Other inputs=0V		25°C	—	—	1	mA
Input Clamp Voltage	V_{IK}	$I_{IN}=-10mA$, Other inputs open		25°C	−1.5	—	—	V
Output Voltage	V_{OH}	$V_{IH}=4V$ or $V_{IL}=0.4V$		−30°C	−1.060	—	−0.890	V
				25°C	−0.960	—	−0.810	
				85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IH}=4V$ or $V_{IL}=0.4V$		−30°C	−1.890	—	−1.675	V
				25°C	−1.850	—	−1.650	
				85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=2.0V$ or $V_{ILA}=1.10V$		−30°C	−1.080	—	—	V
		$V_{IHA}=1.80V$ or $V_{ILA}=1.10V$		25°C	−0.980	—	—	
		$V_{IHA}=1.80V$ or $V_{ILA}=0.90V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=1.10V$ or $V_{IHA}=2.0V$		−30°C	—	—	−1.655	V
		$V_{ILA}=1.10V$ or $V_{IHA}=1.80V$		25°C	—	—	−1.630	
		$V_{ILA}=0.90V$ or $V_{IHA}=1.80V$		85°C	—	—	−1.595	

■AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +7.0V, GND = +2.0V, Ta = −30 ~ +85°C)

Item		Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	In-phase	t_{PLH}	R_L=50Ω	−30°C	1.0	—	6.8	ns
				25°C	1.5	3.5	6.0	
				85°C	1.0	—	6.8	
		t_{PHL}		−30°C	1.0	—	6.8	ns
				25°C	1.5	3.5	6.0	
				85°C	1.0	—	6.8	
	Out-of-phase	t_{PLH}		−30°C	1.0	—	6.0	ns
				25°C	1.5	3.5	6.0	
				85°C	1.5	—	6.8	
		t_{PHL}		−30°C	1.5	—	6.8	ns
				25°C	1.5	3.5	6.0	
				85°C	1.0	—	6.0	
Rise/Fall Time		t_{TLH}		−30°C	1.0	—	4.2	ns
				25°C	1.1	2.5	3.9	
				85°C	1.1	—	4.3	
		t_{THL}		−30°C	1.0	—	4.2	ns
				25°C	1.1	2.5	3.9	
				85°C	1.1	—	4.3	

■TEST CIRCUIT



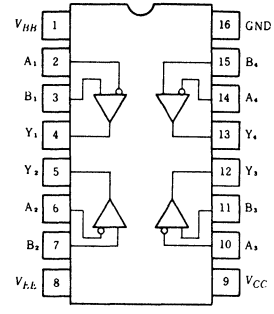


Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Input Pulse; t_{TLH}=t_{THL}=5.5±0.5ns (10 to 90%)
4. Unused outputs connected to a 50Ω resistor to ground.

Quadruple ECL to TTL Translators

The HD10125 is a quad translator for interfacing data and control signals between the ECL section and saturated logic sections of digital systems. The HD10125 incorpolates differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow for use as an inverting/ noninverting translator or as a differential line receiver.
The V_{BB} reference voltage is available on pin 1 for use in single-ended input biasing. The outputs go to a low logic level whenever the inputs are left floating. Power supply requirements are ground, +5V and –5.2V. The HD10125 has a fanout of 10 TTL loads. The DC levels are ECL 10K in and Schottky TTL or standard TTL out. The device has an input common mode noise rejection of ±1.0V.

■PIN ARRANGEMENT



(Top View)

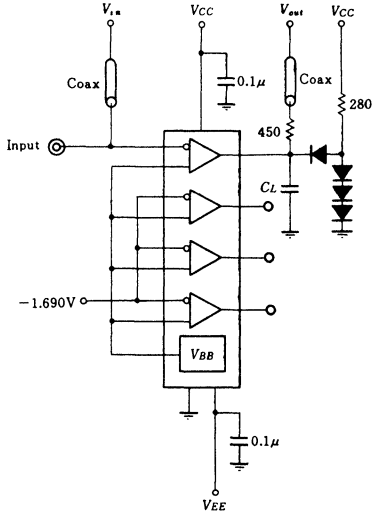
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $V_{CC}=+5.0V$, $Ta=-30\sim+85°C$)

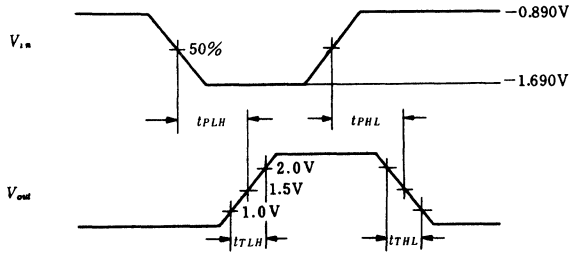
Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	—	40	mA
	I_{CCH}	$V_{IH}=-0.810V$	25°C	—	—	52	mA
	I_{CCL}	$V_{IL}=-1.850V$	25°C	—	—	39	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	25°C	—	—	115	μA
	I_{CBO}	$V_{IN}=-5.2V$	25°C	—	—	1.0	μA
Output Voltage	V_{OH}	$V_{IL}=-1.890V$, $I_{OH}=-2mA$	−30°C	2.5	—	—	V
		$V_{IL}=-1.850V$, $I_{OH}=-2mA$	25°C	2.5	—	—	
		$V_{IL}=-1.825V$, $I_{OH}=-2mA$	85°C	2.5	—	—	
	V_{OL}	$V_{IH}=-0.890V$, $I_{OL}=20mA$	−30°C	—	—	0.5	V
		$V_{IH}=-0.810V$, $I_{OL}=20mA$	25°C	—	—	0.5	
		$V_{IH}=-0.700V$, $I_{OL}=20mA$	85°C	—	—	0.5	
Output Threshold Voltage	V_{OHA}	$V_{ILA}=-1.500V$, $I_{OH}=-2mA$	−30°C	2.5	—	—	V
		$V_{ILA}=-1.475V$, $I_{OH}=-2mA$	25°C	2.5	—	—	
		$V_{ILA}=-1.440V$, $I_{OH}=-2mA$	85°C	2.5	—	—	
	V_{OLA}	$V_{IHA}=-1.205V$, $I_{OL}=20mA$	−30°C	—	—	0.5	V
		$V_{IHA}=-1.105V$, $I_{OL}=20mA$	25°C	—	—	0.5	
		$V_{IHA}=-1.035V$, $I_{OL}=20mA$	85°C	—	—	0.5	
Indeterminate Input Protection Test	V_{OLS1}	$V_{IN}=V_{EE}$, $I_{OL}=20mA$	−30°C	—	—	0.5	V
			25°C	—	—	0.5	
			85°C	—	—	0.5	
	V_{OLS2}	$I_{OL}=20mA$	−30°C	—	—	0.5	V
			25°C	—	—	0.5	
			85°C	—	—	0.5	
Output Short-circuit Current	I_{OS}	A input $=-1.850V$, B input $=V_{BB}$	25°C	40	—	100	mA
Reference Voltage	V_{BB}	A input $=-1.890V$, B input $=V_{BB}$	−30°C	−1.420	—	−1.280	V
		A input $=-1.850V$, B input $=V_{BB}$	25°C	−1.350	—	−1.230	
		A input $=-1.825V$, B input $=V_{BB}$	85°C	−1.295	—	−1.150	
Common Mode Rejection Test	V_{OH}	A input $=-0.890V$ or $-2.890V$, B input $=+0.110V$ or $-1.890V$, $I_{OH}=-2mA$	−30°C	2.5	—	—	V
		A input $=-0.850V$ or $-2.850V$, B input $=+0.190V$ or $-1.810V$, $I_{OH}=-2mA$	25°C	2.5	—	—	
		A input $=-0.825V$ or $-2.825V$, B input $=+0.300V$ or $-1.700V$, $I_{OH}=-2mA$	85°C	2.5	—	—	
	V_{OL}	A input $=+0.110V$ or $-1.890V$, B input $=-0.890V$ or $-2.890V$, $I_{OL}=20mA$	−30°C	—	—	0.5	V
		A input $=+0.190V$ or $-1.810V$, B input $=-0.850V$ or $-2.850V$, $I_{OL}=20mA$	25°C	—	—	0.5	
		A input $=+0.300V$ or $-1.700V$, B input $=-0.825V$ or $-2.825V$, $I_{OL}=20mA$	85°C	—	—	0.5	

■AC CHARACTERISTICS (V_{EE}=−5.2V, V_{CC}=+5.0V, Ta=−30~+85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	R_L=280Ω, C_L=25pF	−30℃	1.0	—	6.0	ns
			25℃	1.0	4.5	6.0	
			85℃	1.0	—	6.0	
	t_{PHL}		−30℃	1.0	—	6.0	ns
			25℃	1.0	4.5	6.0	
			85℃	1.0	—	6.0	
Rise/Fall Time	t_{TLH}		−30℃	—	—	3.3	ns
			25℃	—	—	3.3	
			85℃	—	—	3.3	
	t_{THL}		−30℃	—	—	3.3	ns
			25℃	—	—	3.3	
			85℃	—	—	3.3	

■TEST CIRCUIT



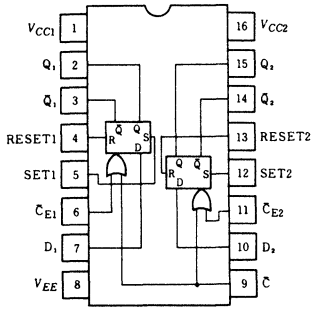


Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be 6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. C_L=25pF, including test fixture.
4. For single-ended input testing, one input from each gate must be tied to V_{BB} (pin 1).

Dual D-type Latches

The HD10130 is a clocked dual D-type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode the enable inputs perform the function of controlling the common clock($\overline{C}$). Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state a change in the information present at the data inputs will not affect the output information. The set and reset inputs do not override the clock and D inputs. They are effective only when either $\overline{C}$ or $\overline{CE}$ or both are high.

■PIN ARRANGEMENT



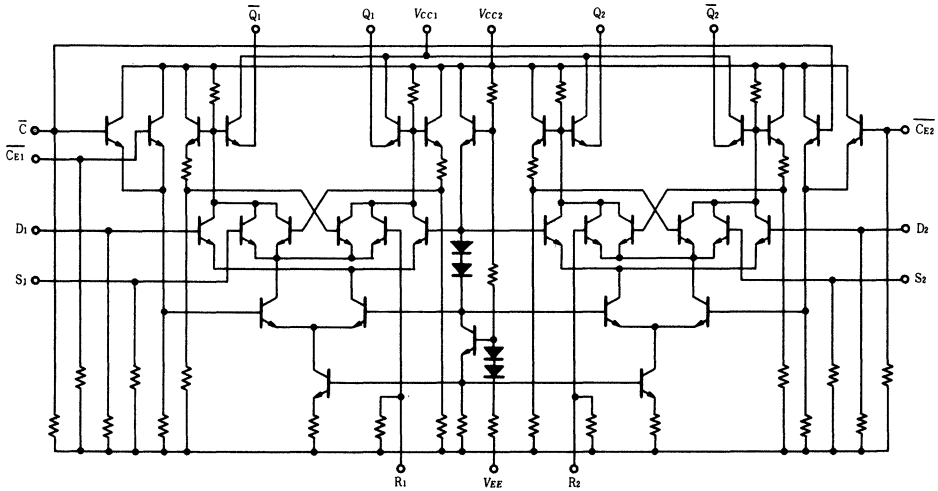
(Top View)

■FUNCTION TABLE

D	$\overline{C}$	$\overline{C}_E$	Q_{n+1}
L	L	L	L
H	L	L	H
×	L	H	Q_n
×	H	L	Q_n
×	H	H	Q_n

× : Don't care.

■CIRCUIT SCHEMATIC



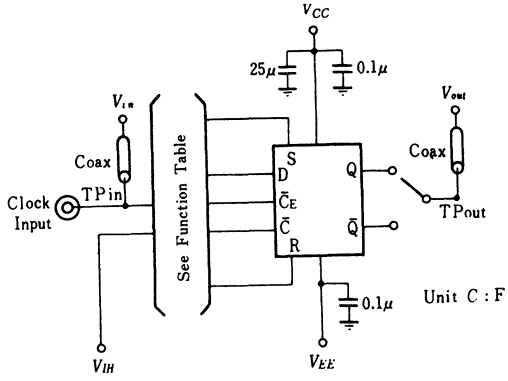
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

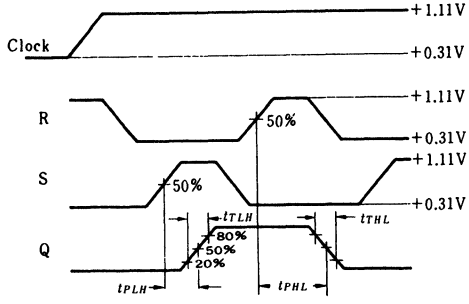
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	30	35	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	$\overline{CE}$	25°C	—	—	220	μA
			$\overline{C}$		—	—	265	
			R, S, $\overline{C}$		—	—	285	
		$V_{IH}=-0.810V$, $\overline{C}=-1.850V$	D, S		—	—	285	
	I_{IL}	$V_{IL}=-1.850V$		25°C	—	—	0.5	μA
Output Voltage	V_{OH}	S=−0.890V		−30°C	−1.060	—	−0.890	V
		S=−0.810V		25°C	−0.960	—	−0.810	
		S=−0.700V		85°C	−0.890	—	−0.700	
	V_{OL}	R=−0.890V		−30°C	−1.890	—	−1.675	V
		R=−0.810V		25°C	−1.850	—	−1.650	
		R=−0.700V		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$\overline{C}=-1.890V$, D=−1.205V		−30°C	−1.080	—	—	V
		$\overline{C}=-1.850V$, D=−1.105V		25°C	−0.980	—	—	
		$\overline{C}=-1.825V$, D=−1.035V		85°C	−0.910	—	—	
	V_{OLA}	$\overline{C}=-1.890V$		−30°C	—	—	−1.655	V
		$\overline{C}=-1.850V$		25°C	—	—	−1.630	
		$\overline{C}=-1.825V$		85°C	—	—	−1.595	

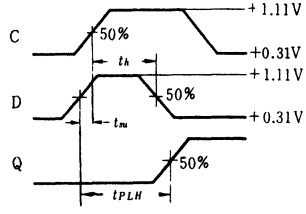
■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

Item	Symbol	Input	Output	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	D	Q, $\overline{Q}$	$R_L=50\Omega$	−30°C	1.0	—	3.6	ns
					25°C	1.0	2.5	3.5	
					85°C	1.0	—	3.8	
	t_{PHL}				−30°C	1.0	—	3.6	ns
					25°C	1.0	2.5	3.5	
					85°C	1.0	—	3.8	
	t_{PLH}	S, R	Q, $\overline{Q}$		−30°C	1.0	—	3.6	ns
					25°C	1.0	2.7	3.5	
					85°C	1.1	—	3.9	
	t_{PHL}				−30°C	1.0	—	3.6	ns
					25°C	1.0	2.7	3.5	
					85°C	1.1	—	3.9	
	t_{PLH}	$\overline{CE}$	Q, $\overline{Q}$		−30°C	1.0	—	4.3	ns
					25°C	1.0	—	4.0	
					85°C	1.0	—	4.1	
	t_{PHL}				−30°C	1.0	—	4.3	ns
					25°C	1.0	—	4.0	
					85°C	1.0	—	4.1	
Rise/Fall Time	t_{TLH}	D	Q, $\overline{Q}$		−30°C	1.0	—	3.6	ns
					25°C	1.1	2.7	3.5	
					85°C	1.1	—	3.8	
	t_{THL}				−30°C	1.0	—	3.6	ns
					25°C	1.1	2.7	3.5	
					85°C	1.1	—	3.8	
Setup Time	t_{su}	$\overline{CE}$, D	Q, $\overline{Q}$		25°C	—	—	2.5	ns
Hold Time	t_h				25°C	—	—	1.5	ns

■TEST CIRCUIT







Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. t_{su} is the minimum time before the positive transition of the clock pulse that information must be present at the data.
4. t_h is the minimum time after the positive transition of the clock pulse that information must remain unchanged at the data.

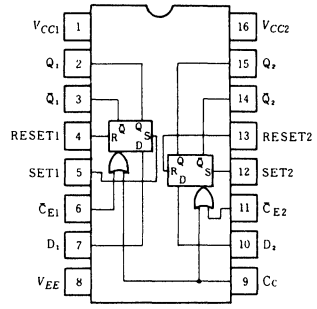
HD10131

Dual D-type Master-Slave Flip Flops

The HD10131 is a dual master-slave type D flip-flop. Asynchronous Set(S) and Reset(R) override Clock(C_C) and Clock Enable($\overline{CE}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data(D) input will not affect the output information at any other time due to master-slave construction.

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

●R-S

R	S	Q_{n+1}	$\overline{Q}_{n+1}$
L	L	Q_n	$\overline{Q}_n$
L	H	H	L
H	L	L	H
H	H	×	×

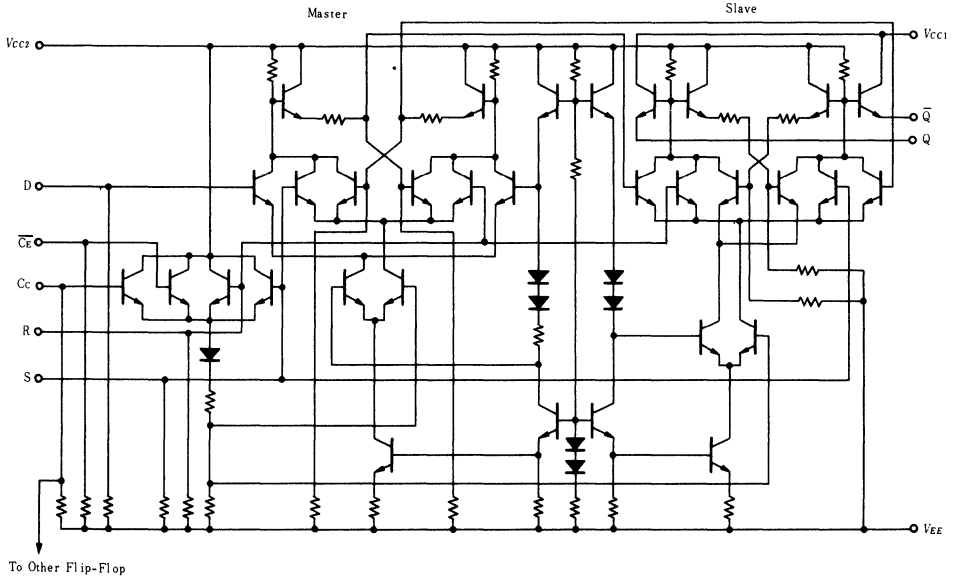
× : Not Defined.

●Clock

C	D	Q_{n+1}
L	×	Q_n
↑	L	L
↑	H	H

Notes) 1. Don't Care
2. $C=\overline{CE}+C_C$
3. A ↑ is a clock transition from a low to a high state.

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS (V_{EE}=−5.2V, Ta=−30~+85°C)

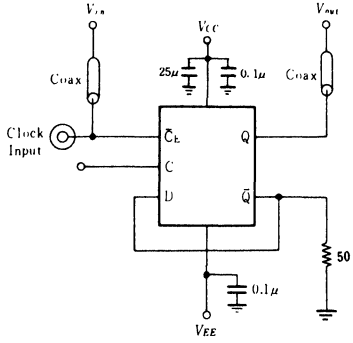
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	45	56	mA
Input Current	I_{IH}	V_{IH}=−0.810V	R, S	25°C	—	—	330	μA
			$\overline{C_E}$		—	—	220	
			D		—	—	245	
			C_C		—	—	265	
	I_{IL}	V_{IL}=−1.850V		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	V_{IH}=−0.890V or V_{IL}=−1.890V		−30°C	−1.060	—	−0.890	V
		V_{IH}=−0.810V or V_{IL}=−1.850V		25°C	−0.960	—	−0.810	
		V_{IH}=−0.700V or V_{IL}=−1.825V		85°C	−0.890	—	−0.700	
	V_{OL}	V_{IL}=−1.890V or V_{IH}=−0.890V		−30°C	−1.890	—	−1.675	V
		V_{IL}=−1.850V or V_{IH}=−0.810V		25°C	−1.850	—	−1.650	
		V_{IL}=−1.825V or V_{IH}=−0.700V		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	V_{IHA}=−1.205V or V_{ILA}=−1.500V		−30°C	−1.080	—	—	V
		V_{IHA}=−1.105V or V_{ILA}=−1.475V		25°C	−0.980	—	—	
		V_{IHA}=−1.035V or V_{ILA}=−1.440V		85°C	−0.910	—	—	
	V_{OLA}	V_{ILA}=−1.500V or V_{IHA}=−1.205V		−30°C	—	—	−1.655	V
		V_{ILA}=−1.475V or V_{IHA}=−1.105V		25°C	—	—	−1.630	
		V_{ILA}=−1.440V or V_{IHA}=−1.035V		85°C	—	—	−1.595	

■AC CHARACTERISTICS (V_{EE}=−3.2V, V_{CC}=+2.0V, Ta=−30~+85°C)

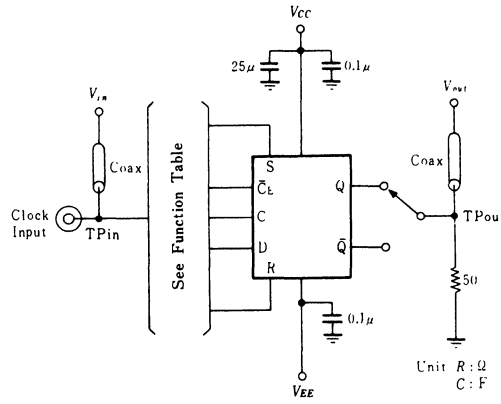
Item	Symbol	Input	Output	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	C_C, $\overline{C_E}$	Q, $\overline{Q}$	R_L=50Ω	−30°C	1.4	—	4.6	ns
					25°C	1.5	3.0	4.5	
					85°C	1.5	—	5.0	
	t_{PHL}				−30°C	1.4	—	4.6	ns
					25°C	1.5	3.0	4.5	
					85°C	1.5	—	5.0	
	t_{PLH}	R, S	Q, $\overline{Q}$		−30°C	1.1	—	4.4	ns
					25°C	1.2	2.8	4.3	
					85°C	1.2	—	4.8	
	t_{PHL}				−30°C	1.1	—	4.4	ns
					25°C	1.2	2.8	4.3	
					85°C	1.2	—	4.8	
Rise/Fall Time	t_{TLH}		Q, $\overline{Q}$		−30°C	1.0	—	4.6	ns
					25°C	1.1	2.5	4.5	
					85°C	1.1	—	4.9	
	t_{THL}				−30°C	1.0	—	4.6	ns
					25°C	1.1	2.5	4.5	
					85°C	1.1	—	4.9	
Setup Time	t_{su}	$\overline{C_E}$, D	Q, $\overline{Q}$		25°C	—	—	2.5	ns
Hold Time	t_h				25°C	—	—	1.5	ns
Max. Toggle Frequency	f_{Tog}	$\overline{C_E}$	Q, $\overline{Q}$		−30°C	125	—	—	MHz
					25°C	125	160	—	
					85°C	125	—	—	

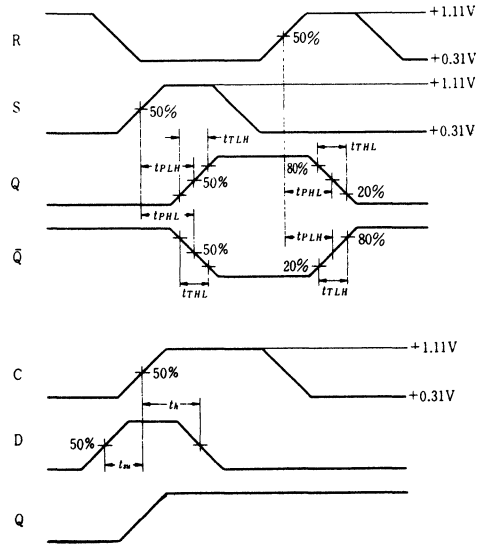
■AC CHARACTERISTIC TEST CIRCUITS

1. Toggle Frequency



2. Switching Time





Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. t_{su} is the minimum time before the positive transition of the clock pulse that information must be present at the data.
4. t_h is the minimum time after the positive transition unchanged at the data.

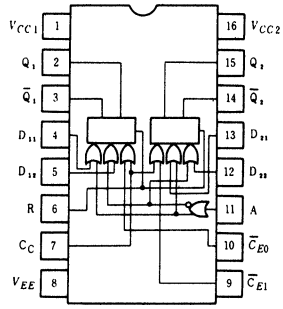
Dual Multiplexers (with Latch and common Reset)

The HD10132 is a dual multiplexer with clocked D type latches. It incorporates common data select and reset inputs. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for a clocking function. If the common clock is to used to clock the latch, the clock enable($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock(C_C). The data select(A) input determines which data input is enabled. A high(H) level enables data inputs D12 and D22 and a low(L) level enables data inputs D11 and D21.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state a change in the information present at the data inputs will not affect the output information.

The reset input is enabled when the clock is in the high state and disabled when the clock is low.

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

R	D	C_C	$\overline{C_E}$	Q_{n+1}
×	L	L	L	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	H	Q_n
×	H	L	L	H
L	H	L	H	Q_n
L	H	H	L	Q_n
L	H	H	H	Q_n
H	×	×	H	L

Notes) 1. Don't care.
2. $D=(\overline{A}\cdot D_{i1})+(A\cdot D_{i2})$

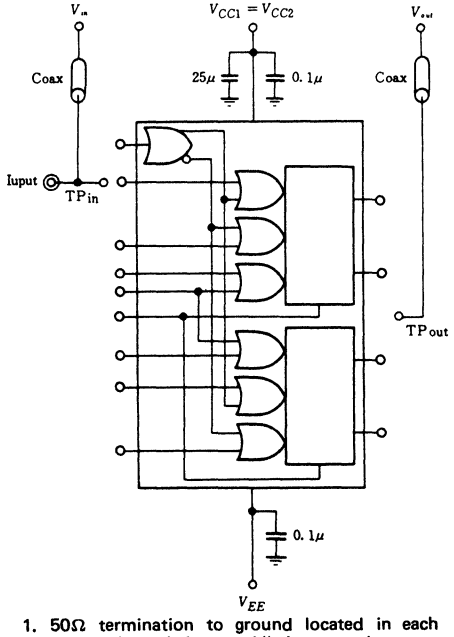
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

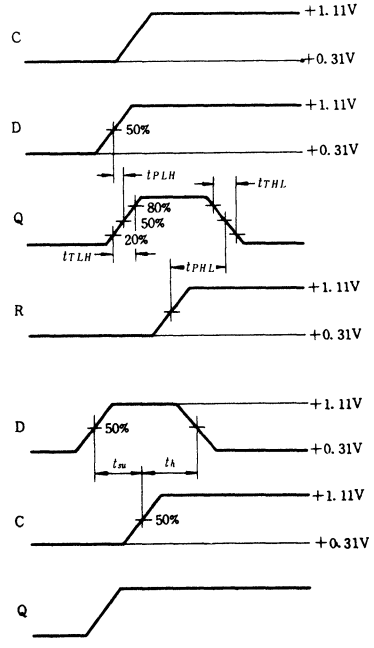
Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	44	55	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	D, C_C	—	—	290	μA
			R	—	—	390	
			$\overline{C_E}$, A	—	—	265	
	I_{IL}	$V_{IL}=-1.850V$	25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$	−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$	25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$	85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$	−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$	25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$	−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$	25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$	85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$	−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$	25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$	85°C	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=25°C$)

Item	Symbol	Input	Output	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	D	Q, $\overline{Q}$	$R_L=50\Omega$	1.0	—	3.3	ns
	t_{PHL}				1.0	—	3.3	ns
	t_{PLH}	R	Q, $\overline{Q}$		1.0	—	3.8	ns
	t_{PHL}				1.0	—	3.8	ns
	t_{PLH}	Cc, $\overline{CE}$	Q, $\overline{Q}$		1.0	—	5.7	ns
	t_{PHL}				1.0	—	5.7	ns
	t_{PLH}	A	Q, $\overline{Q}$		1.0	—	4.6	ns
	t_{PHL}				1.0	—	4.6	ns
Setup Time	t_{su}	D	Q, $\overline{Q}$		—	—	2.5	ns
		A			—	—	3.5	
Hold Time	t_h	D	Q, $\overline{Q}$		—	—	1.5	ns
		A			—	—	1.0	
Rise/Fall Time	t_{TLH}		Q, $\overline{Q}$		1.5	—	3.5	ns
	t_{THL}				1.5	—	3.5	ns

■SWITCHING TIME TEST CIRCUIT



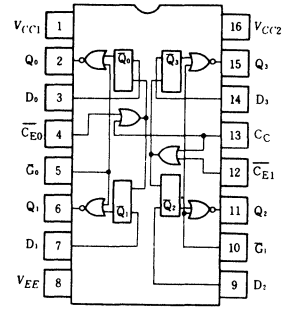


Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.
4. t_{su} is the minimum time before the positive transition of the clock pulse that information must be present at the data.
5. t_h is the minimum time after the positive transition of the clock pulse that information must remain unchanged at the data.

Quadruple Latches

The HD10133 is a high speed, low power quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs, allowing direct wiring to a bus. When the clock is high, outputs will follow D inputs. Information is latched on the negative going transition of the clock. The outputs are gated when the output enable($\overline{G}$) is low. All four latches may be clocked at one time with the common clock(C_C), or each half may be clocked separately with its clock enable ($\overline{CE}$).

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

$\overline{G}$	C	D	Q_{n+1}
H	×	×	L
L	L	×	Q_n
L	H	L	L
L	H	H	H

Notes) × : Don't care.
$C = C_C + \overline{C_E}$

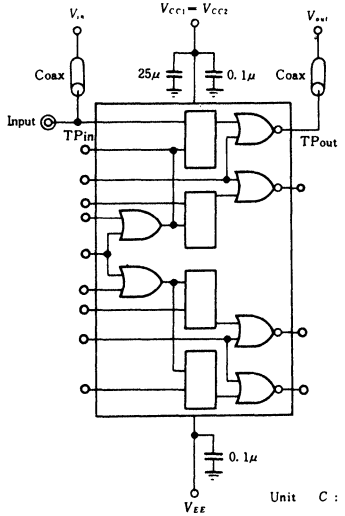
■DC CHARACTERISTICS ($V_{EE} = -5.2V$, $Ta = -30 \sim +85°C$)

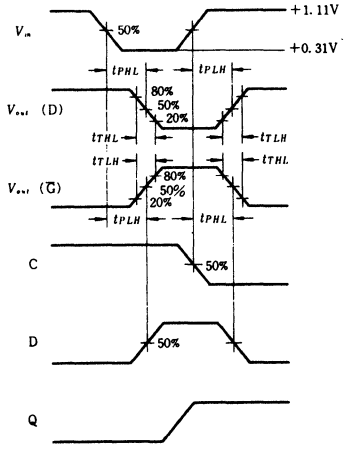
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25℃	—	60	75	mA
Input Current	I_{IH}	$V_{IH} = -0.810V$	D	25℃	—	—	245	μA
			$\overline{C_E}$		—	—	265	
			$\overline{G}$, C_C		—	—	350	
	I_{IL}	$V_{IL} = -1.850V$		25℃	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH} = -0.890V$ or $V_{IL} = -1.890V$		−30℃	−1.060	—	−0.890	V
		$V_{IH} = -0.810V$ or $V_{IL} = -1.850V$		25℃	−0.960	—	−0.810	
		$V_{IH} = -0.700V$ or $V_{IL} = -1.825V$		85℃	−0.890	—	−0.700	
	V_{OL}	$V_{IL} = -1.890V$ or $V_{IH} = -0.890V$		−30℃	−1.890	—	−1.675	V
		$V_{IL} = -1.850V$ or $V_{IH} = -0.810V$		25℃	−1.850	—	−1.650	
		$V_{IL} = -1.825V$ or $V_{IH} = -0.700V$		85℃	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA} = -1.205V$ or $V_{ILA} = -1.500V$		−30℃	−1.080	—	—	V
		$V_{IHA} = -1.105V$ or $V_{ILA} = -1.475V$		25℃	−0.980	—	—	
		$V_{IHA} = -1.035V$ or $V_{ILA} = -1.440V$		85℃	−0.910	—	—	
	V_{OLA}	$V_{ILA} = -1.500V$ or $V_{IHA} = -1.205V$		−30℃	—	—	−1.655	V
		$V_{ILA} = -1.475V$ or $V_{IHA} = -1.105V$		25℃	—	—	−1.630	
		$V_{ILA} = -1.440V$ or $V_{IHA} = -1.035V$		85℃	—	—	−1.595	

■AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30 ~ +85°C)

Item	Symbol	Input	Output	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	D	Q	R_L = 50Ω	−30°C	1.0	—	5.6	ns
					25°C	1.0	—	5.4	
					85°C	1.1	—	5.9	
	t_{PHL}				−30°C	1.0	—	5.6	ns
					25°C	1.0	—	5.4	
					85°C	1.1	—	5.9	
	t_{PLH}	$\overline{C_E}$	Q		−30°C	1.0	—	5.4	ns
					25°C	1.0	—	5.4	
					85°C	1.2	—	6.0	
	t_{PHL}				−30°C	1.0	—	5.4	ns
					25°C	1.0	—	5.4	
					85°C	1.2	—	6.0	
	t_{PLH}	$\overline{G}$	Q		−30°C	1.0	—	3.2	ns
					25°C	1.0	—	3.1	
					85°C	1.0	—	3.4	
	t_{PHL}				−30°C	1.0	—	3.2	ns
					25°C	1.0	—	3.1	
					85°C	1.0	—	3.4	
Rise/Fall Time	t_{TLH}		Q		−30°C	1.0	—	3.6	ns
					25°C	1.1	—	3.5	
					85°C	1.1	—	3.8	
	t_{THL}				−30°C	1.0	—	3.6	ns
					25°C	1.1	—	3.5	
					85°C	1.1	—	3.8	
Setup Time	t_{su}	D	Q		25°C	—	—	2.5	ns
Hold Time	t_h				25°C	—	—	1.5	ns

■SWITCHING TIME TEST CIRCUIT





Notes)

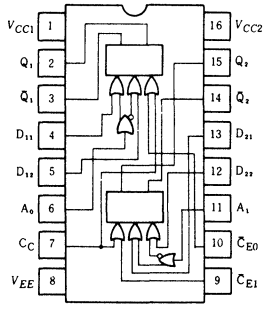
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.
4. t_{su} is the minimum time before the positive transition of the clock pulse that information must be preset at the data.
5. t_h is the minimum time after the positive transition of the clock pulse that information must remain unchanged at the data.

Dual Multiplexers with Latch

The HD10134 is a dual multiplexer with clocked D type latches. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock(C_C).

The data select inputs determine which data input is enabled. A high(H) level on the A0 input enables data input D12 and a low(L) level on the A0 input enables data input D11. A high(H) level on the A1 input enables data input D22 and a low(L) level on the A1 input enables data input D21. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

C	A_0	D_{11}	D_{12}	Q_{n+1}
L	L	L	×	L
L	L	H	×	H
L	H	×	L	L
L	H	×	H	H
H	×	×	×	Q_n

Notes) × : Don't care.
$C=\overline{C}_E+C_C$

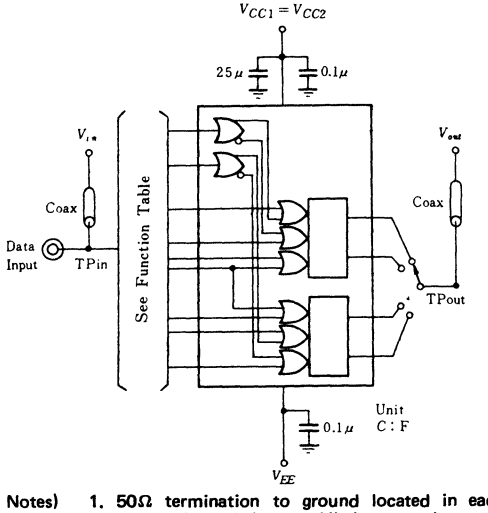
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

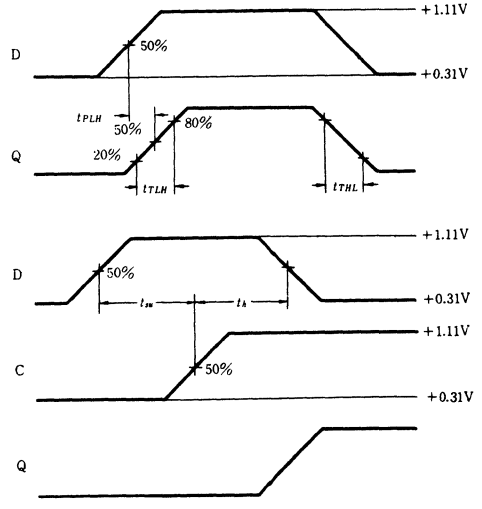
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25℃	—	—	55	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	D, C_C	25℃	—	—	290	μA
			A, $\overline{C_E}$		—	—	265	
	I_{IL}	$V_{IL}=-1.850V$		25℃	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$		−30℃	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$		25℃	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$		85℃	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$		−30℃	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$		25℃	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$		85℃	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$		−30℃	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$		25℃	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$		85℃	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$		−30℃	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$		25℃	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$		85℃	—	—	−1.595	

■AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = 25°C)

Item	Symbol	Input	Output	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	D	Q, $\overline{Q}$	R_L = 50Ω	1.0	—	3.3	ns
	t_{PHL}				1.0	—	3.3	ns
	t_{PLH}	Cc, $\overline{CE}$	Q, $\overline{Q}$		1.0	—	5.7	ns
	t_{PHL}				1.0	—	5.7	ns
	t_{PLH}	A	Q, $\overline{Q}$		1.0	—	4.6	ns
	t_{PHL}				1.0	—	4.6	ns
Setup Time	t_{su}	D	Q, $\overline{Q}$		—	—	2.5	ns
		A	Q, $\overline{Q}$		—	—	3.5	
Hold Time	t_h	D	Q, $\overline{Q}$		—	—	1.5	ns
		A	Q, $\overline{Q}$		—	—	1.0	
Rise/Fall Time	t_{TLH}		Q, $\overline{Q}$		1.5	—	3.5	ns
	t_{THL}				1.5	—	3.5	ns

■SWITCHING TIME TEST CIRCUIT





Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.
4. t_{su} is the minimum time before the positive transition of the clock pulse that information must be present at the data.
5. t_h is the minimum time after the positive transition of the clock pulse that information must remain unchanged at the data.

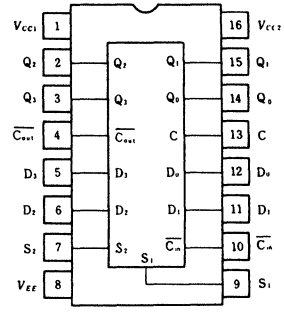
Universal Hexadecimal Counter

The HD10136 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100MHz. The flexibility of this device allows the designer to use one basic counter for most applications, and the synchronous counter feature makes the HD10136 suitable for either computers or instrumentation.

Three control lines (S1, S2, and $\overline{\text{Carry In}}$) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs(D0, D1, D2, and D3) will be entered into the counter. $\overline{\text{Carry Out}}$ goes low on the terminal count, or when the counter is being preset.

This device is not designed for use with gated clocks. Control is via S1 and S2.

■PIN ARRANGEMENT



(Top View)

■FUNCTION SELECT TABLE

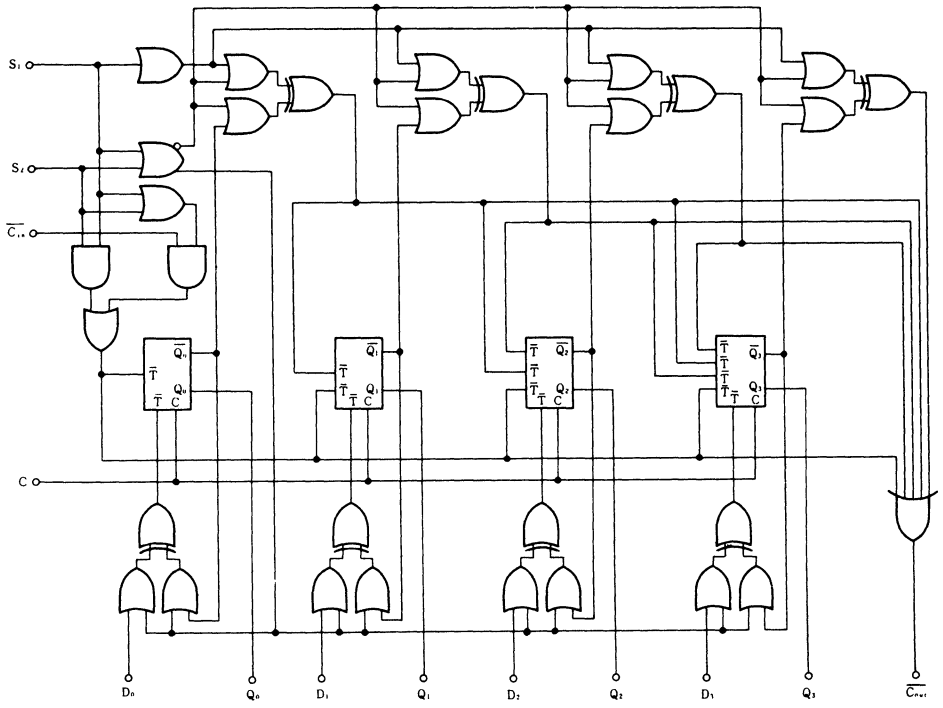
S_1	S_2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

■TRUTH TABLE

Inputs								Outputs				
S_1	S_2	D_0	D_1	D_2	D_3	$\overline{Cin}$	C	Q_0	Q_1	Q_2	Q_3	$\overline{Cout}$
L	L	L	L	H	H	×	↑	L	L	H	H	L
L	H	×	×	×	×	L	↑	H	L	H	H	H
L	H	×	×	×	×	L	↑	L	H	H	H	H
L	H	×	×	×	×	L	↑	H	H	H	H	L
L	H	×	×	×	×	H	L	H	H	H	H	H
L	H	×	×	×	×	H	↑	H	H	H	H	H
H	H	×	×	×	×	×	↑	H	H	H	H	H
L	L	H	H	L	L	×	↑	H	H	L	L	L
H	L	×	×	×	×	L	↑	L	H	L	L	H
H	L	×	×	×	×	L	↑	H	L	L	L	H
H	L	×	×	×	×	L	↑	L	L	L	L	L
H	L	×	×	×	×	L	↑	H	H	H	H	H

Notes) 1. × : Don't care.
2. A ↑ is defined as a clock input transition from a low to a high logic level.

■BLOCK DIAGRAM



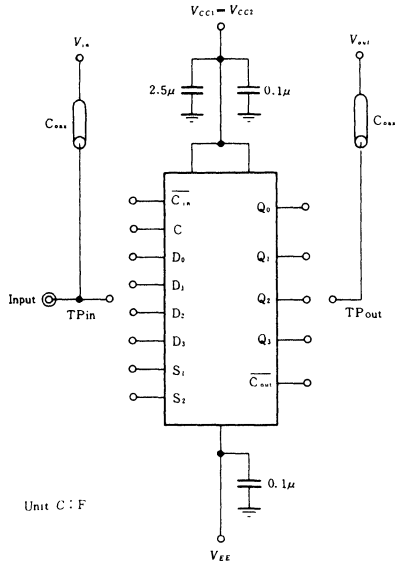
■DC CHARACTERISTICS (V_{EE} = −5.2V, Ta = −30 ~ +85°C)

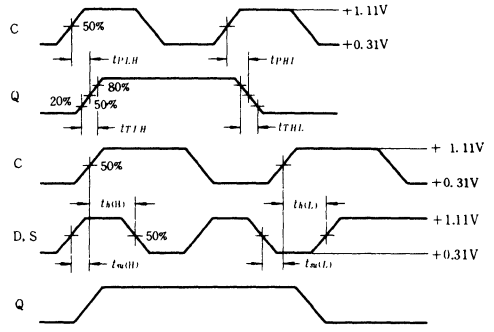
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	120	150	mA
Input Current	I_{IH}	V_{IH} = −0.810V	D	25°C	—	—	220	μA
			S_2		—	—	265	
			S_1, $\overline{Cin}$		—	—	245	
			C		—	—	290	
	I_{IL}	V_{IL} = −1.850V		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	V_{IH} = −0.890V or V_{IL} = −1.890V		−30°C	−1.060	—	−0.890	V
		V_{IH} = −0.810V or V_{IL} = −1.850V		25°C	−0.960	—	−0.810	
		V_{IH} = −0.700V or V_{IL} = −1.825V		85°C	−0.890	—	−0.700	
	V_{OL}	V_{IL} = −1.890V or V_{IH} = −0.890V		−30°C	−1.890	—	−1.675	V
		V_{IL} = −1.850V or V_{IH} = −0.810V		25°C	−1.850	—	−1.650	
		V_{IL} = −1.825V or V_{IH} = −0.700V		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	V_{IHA} = −1.205V or V_{ILA} = −1.500V		−30°C	−1.080	—	—	V
		V_{IHA} = −1.105V or V_{ILA} = −1.475V		25°C	−0.980	—	—	
		V_{IHA} = −1.035V or V_{ILA} = −1.440V		85°C	−0.910	—	—	
	V_{OLA}	V_{ILA} = −1.500V or V_{IHA} = −1.205V		−30°C	—	—	−1.655	V
		V_{ILA} = −1.475V or V_{IHA} = −1.105V		25°C	—	—	−1.630	
		V_{ILA} = −1.440V or V_{IHA} = −1.035V		85°C	—	—	−1.595	

■AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30 ~ +85°C)

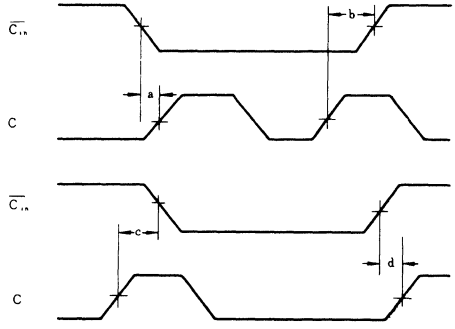
Item		Symbol	Input	Output	Test Condition		min	typ	max	Unit
Propagation Delay Time		t_{PLH}	C	Q	R_L = 50Ω	−30°C	0.8	—	4.8	ns
						25°C	1.0	3.3	4.5	
						85°C	1.4	—	5.0	
		t_{PHL}				−30°C	0.8	—	4.8	ns
						25°C	1.0	3.3	4.5	
						85°C	1.4	—	5.0	
		t_{PLH}	C	$\overline{Cout}$		−30°C	2.0	—	10.9	ns
						25°C	2.5	7.0	10.5	
						85°C	2.4	—	11.5	
		t_{PHL}				−30°C	2.0	—	10.9	ns
						25°C	2.5	7.0	10.5	
						85°C	2.4	—	11.5	
		t_{PLH}	$\overline{Cin}$	$\overline{Cout}$		−30°C	1.6	—	7.4	ns
						25°C	1.6	5.0	6.9	
						85°C	1.9	—	7.5	
		t_{PHL}				−30°C	1.6	—	7.4	ns
						25°C	1.6	5.0	6.9	
						85°C	1.9	—	7.5	
Setup Time		$t_{su(H)}$	D, C	Q	25°C		—	—	3.5	ns
		$t_{su(L)}$					—	—	3.5	ns
		t_{su}	S_1, C	Q			—	—	7.5	ns
			S_2, C	Q			—	—	7.5	
			$\overline{Cin}$, C	Q			—	—	3.7	
			C, $\overline{Cin}$	Q			—	—	−1.0	
Hold Time		$t_{h(H)}$	C, D	Q			—	—	−0.3	ns
		$t_{h(L)}$					—	—	−0.3	ns
		t_h	C, S_1	Q			—	—	−2.5	ns
			C, S_2	Q			—	—	−2.5	
			C, $\overline{Cin}$	Q			—	—	−1.6	
			$\overline{Cin}$, C	Q			—	—	3.1	
Count Frequency	Count Up	f_{count}	C	Q		−30°C	125	—	—	MHz
						25°C	125	150	—	
						85°C	125	—	—	
	Count Down					−30°C	125	—	—	
						25°C	125	150	—	
						85°C	125	—	—	
Rise Time		t_{TLH}	C	$\overline{Cout}$		−30°C	0.9	—	3.3	ns
						25°C	1.1	2.0	3.3	
						85°C	1.1	—	3.5	
			C	Q		−30°C	0.9	—	3.3	
						25°C	1.1	2.0	3.3	
						85°C	1.1	—	3.5	
Fall Time		t_{THL}	C	$\overline{Cout}$		−30°C	0.9	—	3.3	ns
						25°C	1.1	2.0	3.3	
						85°C	1.1	—	3.5	
			C	Q		−30°C	0.9	—	3.3	
						25°C	1.1	2.0	3.3	
						85°C	1.1	—	3.5	

■SWITCHING TIME TEST CIRCUIT





Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.
4. t_{su} is the minimum time before the positive transition of the clock pulse that information must present at the data.
5. t_h is the minimum time after the positive transition of the clock pulse that information must remain unchanged at the data.

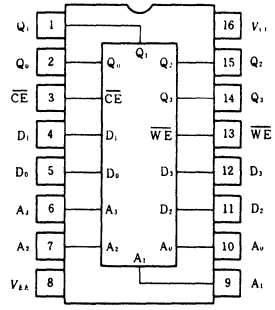


Notes)
1. (a) is the minimum time to wait after the counter has been enabled to clock it.
2. (b) is the minimum time before the counter has been disabled that it may be clocked.
3. (c) is the minimum time before the counter is enabled that a clock pulse may be applied with no effect on the state of the counter.
4. (d) is the minimum time to wait after the counter is disabled that a clock pulse may be applied with no effect in the state of the counter.
5. (b) and (c) may be negative numbers.

64-bit Register File

The HD10145 is a 16 word x 4-bit RAM. Bit selection is achieved by means of a 4-bit address A0 through A3. The active-low chip select allows memory expansion up to 32 words. The fast chip select access time allows memory expansion without affecting system performance. The operating mode of the RAM($\overline{CE}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode- the output is low and the data present at Dn is stored at the selected address.
With $\overline{WE}$ high the chip is in the read mode- The data state at the selected memory location is presented non-inverted at Qn.

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

Mode	Inputs			Output
	$\overline{CE}$	$\overline{WE}$	D	Q
Write "L"	L	L	L	L
Write "H"	L	L	H	L
Read	L	H	×	Q
Disabled	H	×	×	L

Note) × : Don't care.

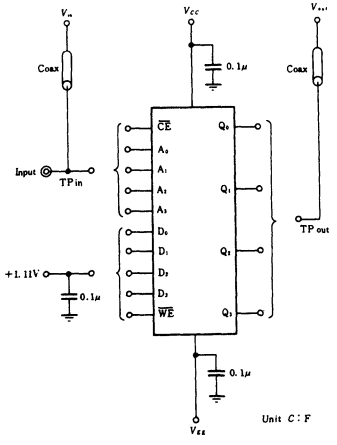
■DC CHARACTERISTICS (V_{EE} = −5.2V, Ta = −30 ~ +85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	120	150	mA
Input Current	I_{IH}	V_{IH} = −0.810V	$\overline{CE}$, A, 25°C	—	—	200	μA
			D, 25°C	—	—	220	
			$\overline{WE}$, 25°C	—	—	470	
	I_{IL}	V_{IL} = −1.850V	25°C	0.5	—	—	μA
Output Voltage	V_{OH}	V_{IH} = −0.890V or V_{IL} = −1.890V	−30°C	−1.060	—	−0.890	V
		V_{IH} = −0.810V or V_{IL} = −1.850V	25°C	−0.960	—	−0.810	
		V_{IH} = −0.700V or V_{IL} = −1.825V	85°C	−0.890	—	−0.700	
	V_{OL}	V_{IL} = −1.890V or V_{IH} = −0.890V	−30°C	−1.890	—	−1.675	V
		V_{IL} = −1.850V or V_{IH} = −0.810V	25°C	−1.850	—	−1.650	
		V_{IL} = −1.825V or V_{IH} = −0.700V	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	V_{IHA} = −1.205V or V_{ILA} = −1.500V	−30°C	−1.080	—	—	V
		V_{IHA} = −1.105V or V_{ILA} = −1.475V	25°C	−0.980	—	—	
		V_{IHA} = −1.035V or V_{ILA} = −1.440V	85°C	−0.910	—	—	
	V_{OLA}	V_{ILA} = −1.500V or V_{IHA} = −1.205V	−30°C	—	—	−1.655	V
		V_{ILA} = −1.475V or V_{IHA} = −1.105V	25°C	—	—	−1.630	
		V_{ILA} = −1.440V or V_{IHA} = −1.035V	85°C	—	—	−1.595	

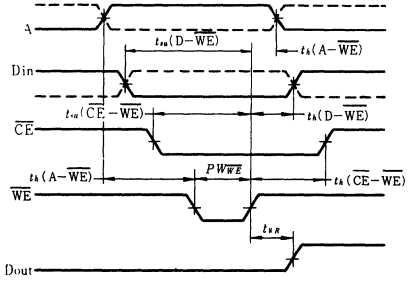
■AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = 25°C)

Item	Symbol	Input	Output	Test Condition	min	typ	max	Unit
Access Time	t_A	$\overline{CE}$	Q		—	7.0	10	ns
		A	Q		—	10	15	
Setup Time	t_{su}	D→$\overline{WE}$	Q		—	7.5	11	ns
		$\overline{CE}$→$\overline{WE}$	Q		—	11	16	
		A→$\overline{WE}$	Q		—	3.5	6	
Hold Time	t_h	D→$\overline{WE}$	Q		—	3.0	5	ns
		$\overline{CE}$→$\overline{WE}$	Q		—	3.0	5	
		A→$\overline{WE}$	Q		—	3.5	5	
Write Recovery Time	t_{WR}	$\overline{WE}$	Q	R_L=50Ω	—	7.5	11	ns
Write Pulse Width	$PW_{\overline{WE}}$	$\overline{WE}$			—	7.5	15	ns
Setup Time	t_{su}	D→$\overline{CE}$	Q		—	7.5	11	ns
		$\overline{WE}$→$\overline{CE}$	Q		—	11	16	
		A→$\overline{CE}$	Q		—	3.0	5	
Hold Time	t_h	D→$\overline{CE}$	Q		—	3.0	5	ns
		$\overline{WE}$→$\overline{CE}$	Q		—	3.0	5	
		A→$\overline{CE}$	Q		—	3.0	5	
Chip Enable Pulse Width	$PW_{\overline{CE}}$	$\overline{CE}$			—	7.5	11	ns
Rise/Fall Time	t_{TLH}		Q		—	3.0	3.3	ns
	t_{THL}				—	3.0	3.3	ns

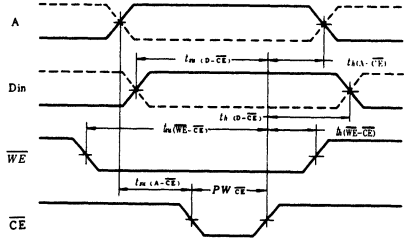
■SWITCHING TIME TEST CIRCUIT



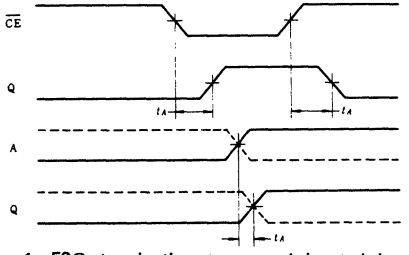
1. Write Timing-Write Strobe Mode



2. Chip Enable Strobe Mode



3. Read Timing

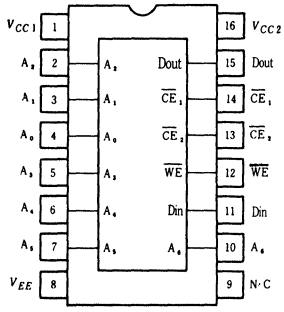


Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

128-word×1-bit Random Access Memory

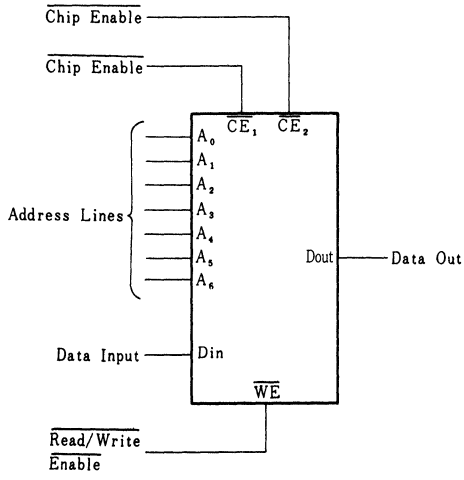
The HD10147 is a fast 128-word x 1-bit RAM. Bit selection is achieved by means of a 7-bit address, A0 through A6. The active-low chip selects and fast chip select access time allow easy memory expansion up to 512 words without affecting system performance. The operating mode ($\overline{CE}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode- the output is low and the data present at Dn is stroed at the selected address. With $\overline{WE}$ high the chip is in the read mode- the data state at the selected memory location is presented non-inverted at Dout.

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■FUNCTION TABLE

Mode	Input				Output
	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	Din	Dout
Write "L"	L	L	L	L	L
Write "H"	L	L	L	H	L
Read	L	L	H	×	Q
Disabled	H	L	×	×	L
	L	H	×	×	L

Note) × : Don't care.

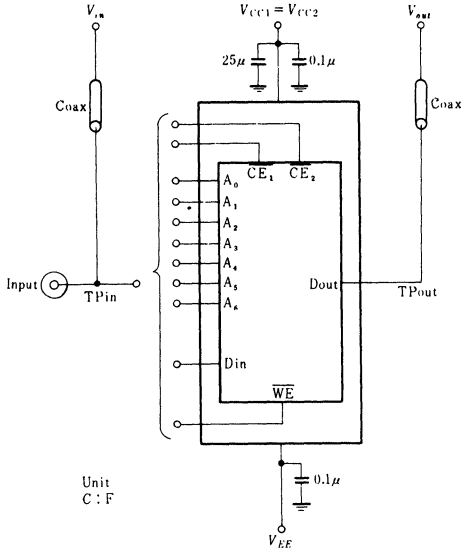
■DC CHARACTERISTICS (V_{EE}=−5.2V, Ta=−30～+85°C)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	80	100	mA
Input Current	I_{IH}	V_{IH}=−0.810V	A, D, $\overline{CE}$	25°C	—	—	35	μA
			$\overline{WE}$		—	—	75	
	I_{IL}	V_{IL}=−1.850V	A, $\overline{WE}$	25°C	−6.0	—	6.0	μA
			D, $\overline{CE}$		—	—	6.0	
Output Voltage	V_{OH}	$\overline{WE}$=−1.205V, $\overline{CE}$=−1.500V		−30°C	−1.060	—	−0.890	V
		$\overline{WE}$=−1.105V, $\overline{CE}$=−1.475V		25°C	−0.960	—	−0.810	
		$\overline{WE}$=−1.035V, $\overline{CE}$=−1.440V		85°C	−0.890	—	−0.700	
	V_{OL}	$\overline{WE}$=−1.205V, $\overline{CE}$=−1.500V		−30°C	−1.890	—	−1.675	V
		$\overline{WE}$=−1.105V, $\overline{CE}$=−1.475V		25°C	−1.850	—	−1.650	
		$\overline{WE}$=−1.035V, $\overline{CE}$=−1.440V		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$\overline{WE}$=−1.205V, $\overline{CE}$=−1.500V		−30°C	−1.080	—	—	V
		$\overline{WE}$=−1.105V, $\overline{CE}$=−1.475V		25°C	−0.980	—	—	
		$\overline{WE}$=−1.035V, $\overline{CE}$=−1.440V		85°C	−0.910	—	—	
	V_{OLA}	$\overline{CE_1}$ or $\overline{CE_2}$=−1.205V		−30°C	—	—	−1.655	V
		$\overline{CE_1}$ or $\overline{CE_2}$=−1.105V		25°C	—	—	−1.630	
		$\overline{CE_1}$ or $\overline{CE_2}$=−1.035V		85°C	—	—	−1.595	

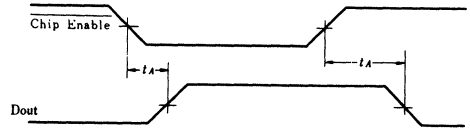
■AC CHARACTERISTICS (V_{EE}=−3.2V, V_{CC}=+2.0V, Ta=25°C)

Item		Symbol	Input	Output	Test Condition	min	typ	max	Unit
Access Time		t_A	$\overline{CE}$	Q	R_L=50Ω	—	—	8.0	ns
			A_5	Q		—	10	12	
			A_0	Q		—	9	10	
Write Strobe Mode	Setup Time	t_{su}	D→$\overline{WE}$	Q		1.0	—	—	ns
			$\overline{CE}$→$\overline{WE}$	Q		1.0	—	—	
			A_2→$\overline{WE}$	Q		3.0	—	—	
			A_5→$\overline{WE}$	Q		4.0	—	—	
	Hold Time	t_h	D→$\overline{WE}$	Q		1.0	—	—	ns
			$\overline{CE}$→$\overline{WE}$	Q		1.0	—	—	
			A→$\overline{WE}$	Q		3.0	—	—	
Write Recovery Time		t_{WR}	$\overline{WE}$	Q		—	—	8.0	ns
Write Pulse Width		$t_{W(\overline{WE})}$	$\overline{WE}$	Q		—	—	8.0	ns
Rise Time		t_{TLH}		Q		—	2.0	—	ns
Fall Time		t_{THL}				—	1.0	—	ns

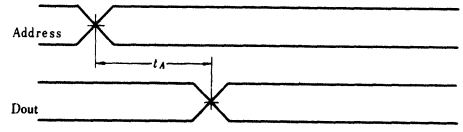
■SWITCHING TIME TEST CIRCUIT



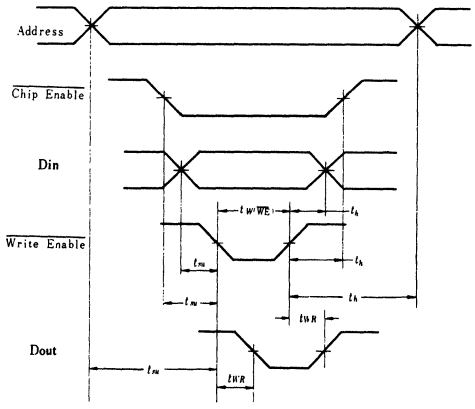
1. Chip Enable Access Time



2. Address Access Time



3. Write Strobe Mode



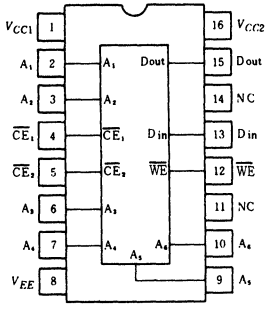
Notes) 1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

HD10148

64-bit Random Access Memory

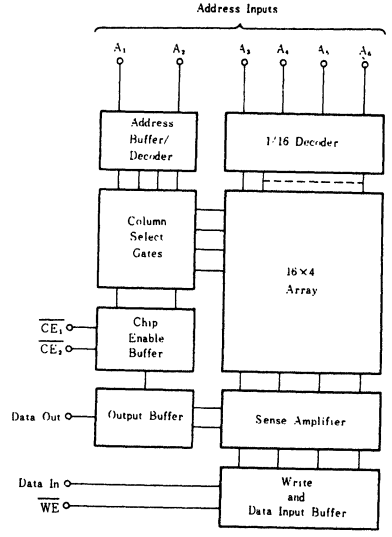
The HD10148 is a fast 64-word x 1-bit RAM. Bit selection is achieved by means of a 6-bit address, A0 through A5. The active low chip selects and fast chip select access time allow easy memory expansion up to 256 words without affecting system performance. The operating mode ($\overline{CE}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode- The output is low and the data present at Din is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode- the data state at the selected memory location is presented non-inverted at Dout.

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■FUNCTION TABLE

Mode	Inputs			Output
	$\overline{CE}$	$\overline{WE}$	Din	Dout
Write "L"	L	L	L	L
Write "H"	L	L	H	L
Read	L	H	×	Q
Disabled	H	×	×	L

× : Don't care.
$\overline{CE} = \overline{CE}_1 + \overline{CE}_2$

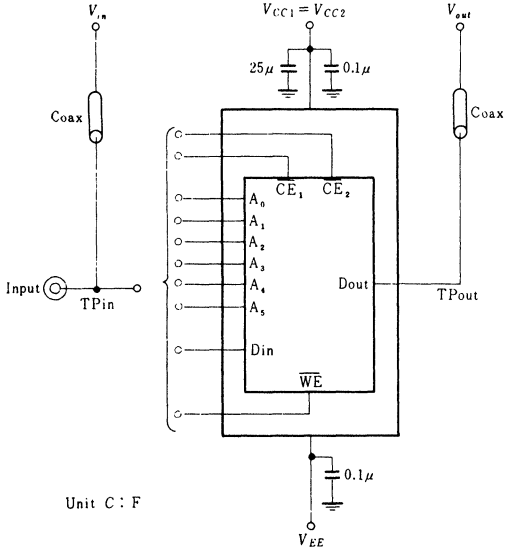
■DC CHARACTERISTICS ($V_{EE} = -5.2V$, $Ta = -30 \sim +85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	80	130	mA
Input Current	I_{IH}	$V_{IH} = -0.810V$	A	25°C	—	—	265	μA
			$\overline{CE}$		—	—	50	
	I_{IL}	$V_{IL} = -1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH} = -0.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH} = -0.810V$		25°C	−0.960	—	−0.810	
		$V_{IH} = -0.700V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IH} = -0.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IH} = -0.810V$		25°C	−1.850	—	−1.650	
		$V_{IH} = -0.700V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA} = -1.205V$		−30°C	−1.080	—	—	V
		$V_{IHA} = -1.105V$		25°C	−0.980	—	—	
		$V_{IHA} = -1.035V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA} = -1.500V$		−30°C	—	—	−1.655	V
		$V_{ILA} = -1.475V$		25°C	—	—	−1.630	
		$V_{ILA} = -1.440V$		85°C	—	—	−1.595	

■ AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = 25°C)

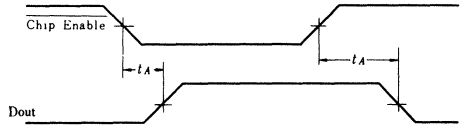
Item		Symbol	Input	Output	Test Condition	min	typ	max	Unit
Access Time		t_A	$\overline{CE}$	Dout	R_L=50Ω	—	—	12	ns
			A	Dout		—	—	15	
Pulse Width		t_w	$\overline{WE}$	Dout		—	—	10	ns
			$\overline{CE}$	Dout		—	—	13	
Write Strobe Mode	Setup Time	t_{su}	Din→$\overline{WE}$	Dout		—	—	0	ns
			$\overline{CE}$→$\overline{WE}$	Dout		—	—	3	
			A→$\overline{WE}$	Dout		—	—	5	
	Hold Time	t_h	$\overline{WE}$→Din	Dout		—	—	3	ns
			$\overline{WE}$→$\overline{CE}$	Dout		—	—	0	
			$\overline{WE}$→A	Dout		—	—	3	

■ SWITCHING TIME TEST CIRCUIT

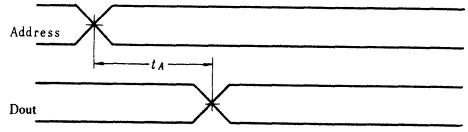


Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

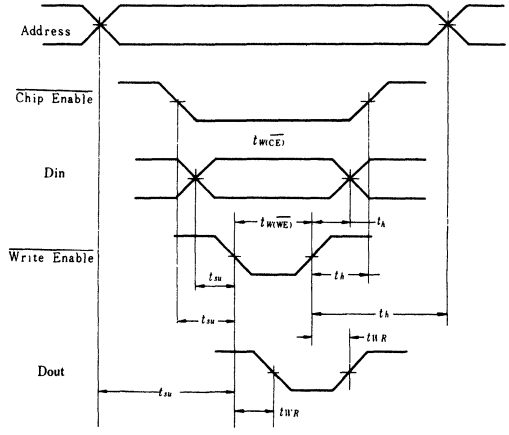
1. Chip Enable Access Time



2. Address Access Time



3. Write Strobe Mode

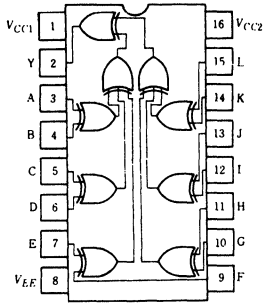


12-bit Parity Generator/Checker

The HD10160 consists of nine Exclusive-OR gates in a single package, internally connected to provide odd parity checking or generation. Output goes high when an odd number of inputs are high.

Unconnected inputs are pulled to low logic levels allowing parity detection and generation for less than 12 bits.

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

Inputs	Output
Sum of High Level Inputs	Y
Even	L
Odd	H

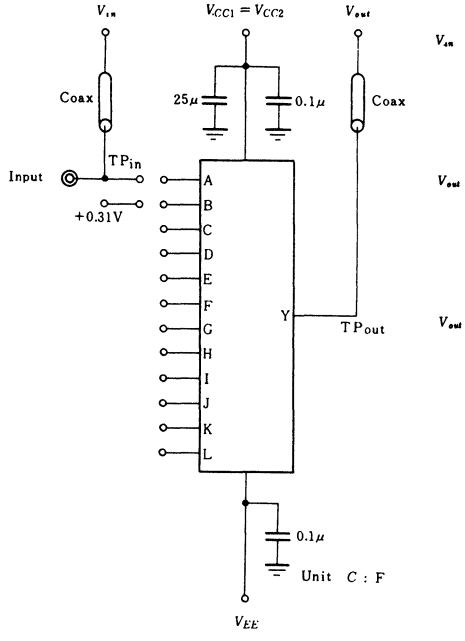
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

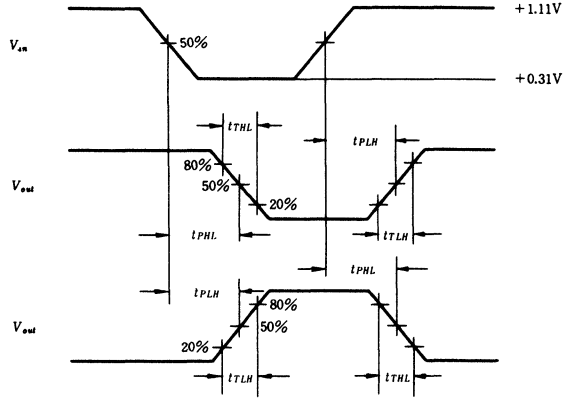
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	B, C, F, G, J, K = −0.810V		25°C	—	62	78	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	A, D, E, H, I, L	25°C	—	—	265	μA
			B, C, F, G, J, K		—	—	220	
	I_{IL}	$V_{IL}=-1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	Each one input = −0.890V, Other inputs = −1.890V		−30°C	−1.060	—	−0.890	V
		Each one input = −0.810V, Other inputs = −1.850V		25°C	−0.960	—	−0.810	
		Each one input = −0.700V, Other inputs = −1.825V		85°C	−0.890	—	−0.700	
	V_{OL}	All inputs = −1.890V		−30°C	−1.890	—	−1.675	V
		All inputs = −1.850V		25°C	−1.850	—	−1.650	
		All inputs = −1.825V		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	Each one input = −1.205V, Other inputs = −1.890V		−30°C	−1.080	—	—	V
		Each one input = −1.105V, Other inputs = −1.850V		25°C	−0.980	—	—	
		Each one input = −1.035V, Other inputs = −1.825V		85°C	−0.910	—	—	
	V_{OLA}	Each one input = −1.500V, Other inputs = −1.890V		−30°C	—	—	−1.655	V
		Each one input = −1.475V, Other inputs = −1.850V		25°C	—	—	−1.630	
		Each one input = −1.440V, Other inputs = −1.825V		85°C	—	—	−1.595	

■ AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30~+85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	R_L=50Ω	−30°C	1.8	—	8.1	ns
			25°C	2.0	5.0	7.5	
			85°C	2.0	—	8.0	
	t_{PHL}		−30°C	1.8	—	8.1	ns
			25°C	2.0	5.0	7.5	
			85°C	2.0	—	8.0	
Rise/Fall Time	t_{TLH}		−30°C	1.1	—	3.5	ns
			25°C	1.1	2.0	3.3	
			85°C	1.0	—	3.5	
	t_{THL}		−30°C	1.1	—	3.5	ns
			25°C	1.1	2.0	3.3	
			85°C	1.0	—	3.5	

■ SWITCHING TIME TEST CIRCUIT



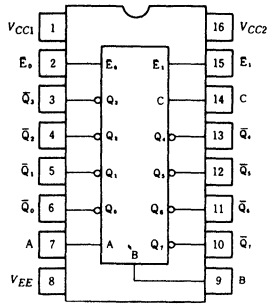


Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

Binary to 1-8 Decoder (low)

The HD10161 is designed to decode a three bit input word to a one of eight line output. The selected output will be low while all other outputs will be high. The enable inputs, when either or both are high, force all outputs high. The HD10161 is a true parallel decoder.
No series gating is used internally, eliminating unequal delay time found in other decoders. This design provides the identical 4ns delay from any address or enable input to any output.

■ PIN ARRANGEMENT



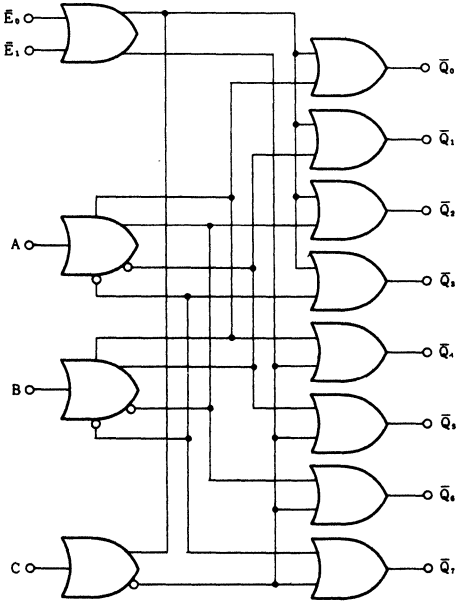
(Top View)

■ FUNCTION TABLE

Enable Inputs		Inputs			Outputs							
$\overline{E}_1$	$\overline{E}_0$	C	B	A	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	×	×	×	×	H	H	H	H	H	H	H	H
×	H	×	×	×	H	H	H	H	H	H	H	H

× : Don't Care

■ BLOCK DIAGRAM



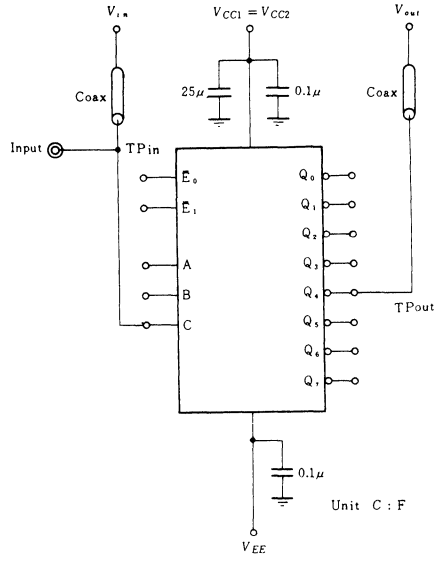
■ DC CHARACTERISTICS (V_{EE} = −5.2V, Ta = −30 ~ +85°C)

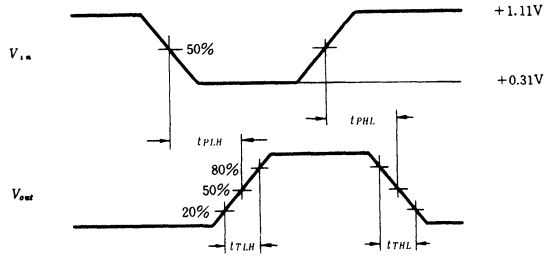
Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All inputs = −0.810V	25°C	—	61	76	mA
Input Current	I_{IH}	V_{IH} = −0.810V	25°C	—	—	220	μA
	I_{IL}	V_{IL} = −1.850V	25°C	0.5	—	—	μA
Output Voltage	V_{OH}	V_{IH} = −0.890V or V_{IL} = −1.890V	−30°C	−1.060	—	−0.890	V
		V_{IH} = −0.810V or V_{IL} = −1.850V	25°C	−0.960	—	−0.810	
		V_{IH} = −0.700V or V_{IL} = −1.825V	85°C	−0.890	—	−0.700	
	V_{OL}	V_{IL} = −1.890V or V_{IH} = −0.890V	−30°C	−1.890	—	−1.675	V
		V_{IL} = −1.850V or V_{IH} = −0.810V	25°C	−1.850	—	−1.650	
		V_{IL} = −1.825V or V_{IH} = −0.700V	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	V_{IHA} = −1.205V or V_{ILA} = −1.500V	−30°C	−1.080	—	—	V
		V_{IHA} = −1.105V or V_{ILA} = −1.475V	25°C	−0.980	—	—	
		V_{IHA} = −1.035V or V_{ILA} = −1.440V	85°C	−0.910	—	—	
	V_{OLA}	V_{ILA} = −1.500V or V_{IHA} = −1.205V	−30°C	—	—	−1.655	V
		V_{ILA} = −1.475V or V_{IHA} = −1.105V	25°C	—	—	−1.630	
		V_{ILA} = −1.440V or V_{IHA} = −1.035V	85°C	—	—	−1.595	

■ AC CHARACTERISTICS (V_{EE} = −3.2V , V_{CC} = +2.0V, Ta = −30 ~ +85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	R_L = 50Ω	−30°C	1.5	—	6.2	ns
			25°C	1.5	4.0	6.0	
			85°C	1.5	—	6.4	
	t_{PHL}		−30°C	1.5	—	6.2	ns
			25°C	1.5	4.0	6.0	
			85°C	1.5	—	6.4	
Rise/Fall Time	t_{TLH}		−30°C	1.0	—	3.3	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.5	
	t_{THL}		−30°C	1.0	—	3.3	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.5	

■ SWITCHING TIME TEST CIRCUIT



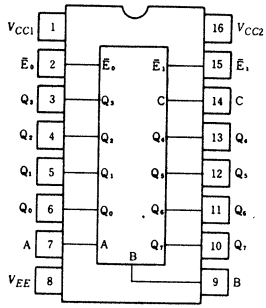


Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

Binary to 1-8 Decoder (high)

The HD10162 is designed to convert three lines of input data to a one-of-eight output. The selected output will be high while all other outputs are low. The enable inputs, when either or both are high, force all outputs low. The HD10162 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders. This device is ideally suited for demultiplexer applications. One of the two enable inputs is used as the data input, while the other is used as a data enable input.

■PIN ARRANGEMENT

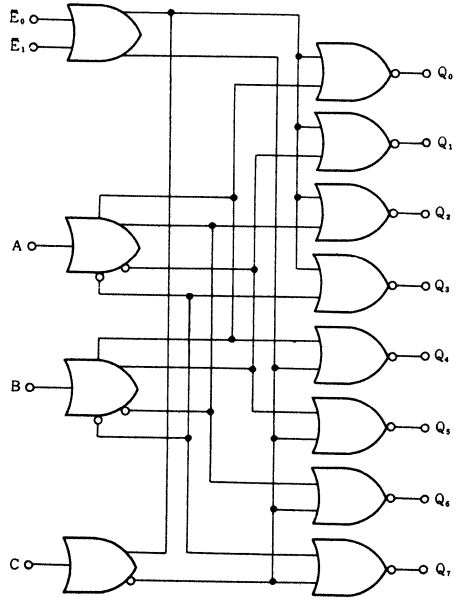


■FUNCTION TABLE

Enable Inputs		Inputs			Outputs							
$\overline{E}_0$	$\overline{E}_1$	C	B	A	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	×	×	×	×	L	L	L	L	L	L	L	L
×	H	×	×	×	L	L	L	L	L	L	L	L

× : Don't Care

■BLOCK DIAGRAM



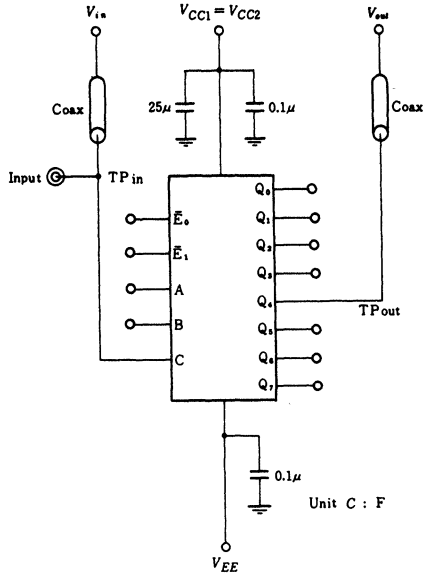
■ DC CHARACTERISTICS (V_{EE} = −5.2V, Ta = −30 ~ +85°C)

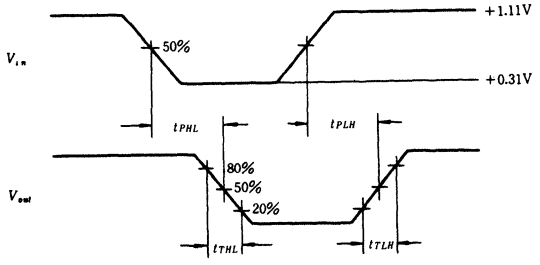
Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	61	76	mA
Input Current	I_{IH}	V_{IH} = −0.810V	25°C	—	—	220	μA
	I_{IL}	V_{IL} = −1.850V	25°C	0.5	—	—	μA
Output Voltage	V_{OH}	V_{IH} = −0.890V or V_{IL} = −1.890V	−30°C	−1.060	—	−0.890	V
		V_{IH} = −0.810V or V_{IL} = −1.850V	25°C	−0.960	—	−0.810	
		V_{IH} = −0.700V or V_{IL} = −1.825V	85°C	−0.890	—	−0.700	
	V_{OL}	V_{IL} = −1.890V or V_{IH} = −0.890V	−30°C	−1.890	—	−1.675	V
		V_{IL} = −1.850V or V_{IH} = −0.810V	25°C	−1.850	—	−1.650	
		V_{IL} = −1.825V or V_{IH} = −0.700V	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	V_{IHA} = −1.205V or V_{ILA} = −1.500V	−30°C	−1.080	—	—	V
		V_{IHA} = −1.105V or V_{ILA} = −1.475V	25°C	−0.980	—	—	
		V_{IHA} = −1.035V or V_{ILA} = −1.440V	85°C	−0.910	—	—	
	V_{OLA}	V_{ILA} = −1.500V or V_{IHA} = −1.205V	−30°C	—	—	−1.655	V
		V_{ILA} = −1.475V or V_{IHA} = −1.105V	25°C	—	—	−1.630	
		V_{ILA} = −1.440V or V_{IHA} = −1.035V	85°C	—	—	−1.595	

■ AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30 ~ +85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	R_L = 50Ω	−30°C	1.5	—	6.2	ns
			25°C	1.5	4.0	6.0	
			85°C	1.5	—	6.4	
	t_{PHL}		−30°C	1.5	—	6.2	ns
			25°C	1.5	4.0	6.0	
			85°C	1.5	—	6.4	
Rise/Fall Time	t_{TLH}		−30°C	1.0	—	3.3	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.5	
	t_{THL}		−30°C	1.0	—	3.3	ns
			25°C	1.1	2.0	3.3	
			85°C	1.1	—	3.5	

■ SWITCHING TIME TEST CIRCUIT



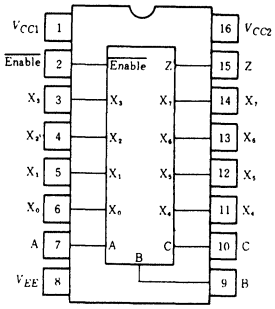


Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

8 Line Multiplexer

The HD10164 can be used whenever data multiplexing or parallel to serial conversion is desirable. Full parallel gating permits equal delays through any data path. The output of the HD10164 incorporates a buffer gate with eight data inputs and an enable. A high level on the enable forces the output low. The HD10164 can be connected directly to a data bus, due to its open emitter output and output enable.

■ PIN ARRANGEMENT



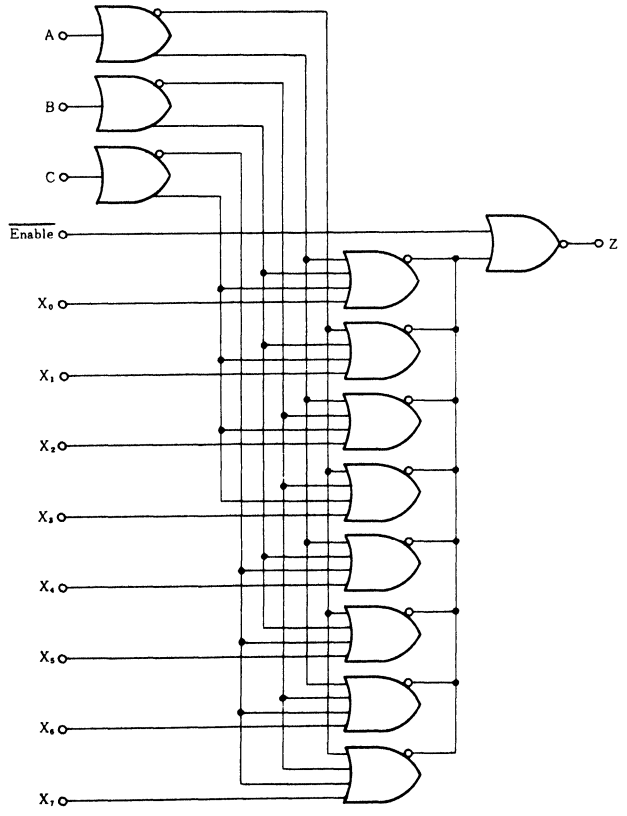
(Top View)

■ FUNCTION TABLE

$\overline{Enable}$	Address Inputs			Z
	C	B	A	
L	L	L	L	X_0
L	L	L	H	X_1
L	L	H	L	X_2
L	L	H	H	X_3
L	H	L	L	X_4
L	H	L	H	X_5
L	H	H	L	X_6
L	H	H	H	X_7
H	×	×	×	L

× : Don't Care

■ BLOCK DIAGRAM



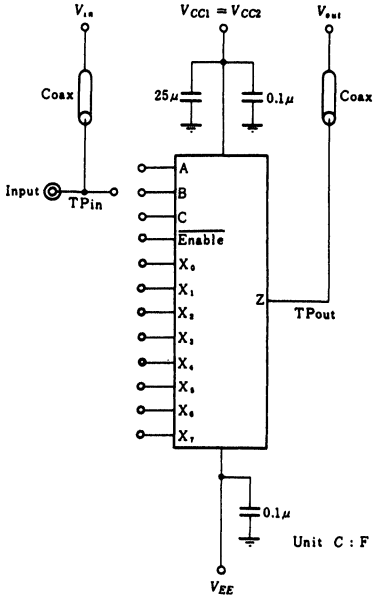
■ DC CHARACTERISTICS (V_{EE} = −5.2V, Ta = −30 ~ +85℃)

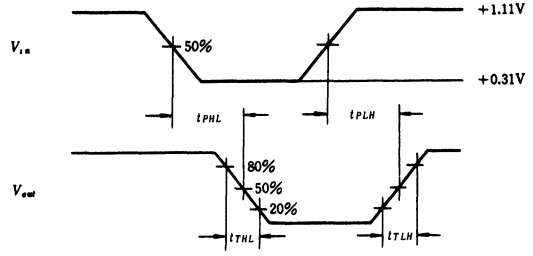
Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25℃	—	60	75	mA
Input Current	I_{IH}	V_{IH} = −0.810V	25℃	—	—	265	μA
	I_{IL}	V_{IL} = −1.850V	25℃	0.5	—	—	μA
Output Voltage	V_{OH}	V_{IH} = −0.890V or V_{IL} = −1.890V	−30℃	−1.060	—	−0.890	V
		V_{IH} = −0.810V or V_{IL} = −1.850V	25℃	−0.960	—	−0.810	
		V_{IH} = −0.700V or V_{IL} = −1.825V	85℃	−0.890	—	−0.700	
	V_{OL}	V_{IL} = −1.890V or V_{IH} = −0.890V	−30℃	−1.890	—	−1.675	V
		V_{IL} = −1.850V or V_{IH} = −0.810V	25℃	−1.850	—	−1.650	
		V_{IL} = −1.825V or V_{IH} = −0.700V	85℃	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	V_{IHA} = −1.205V or V_{ILA} = −1.500V	−30℃	−1.080	—	—	V
		V_{IHA} = −1.105V or V_{ILA} = −1.475V	25℃	−0.980	—	—	
		V_{IHA} = −1.035V or V_{ILA} = −1.440V	85℃	−0.910	—	—	
	V_{OLA}	V_{ILA} = −1.500V or V_{IHA} = −1.205V	−30℃	—	—	−1.655	V
		V_{ILA} = −1.475V or V_{IHA} = −1.105V	25℃	—	—	−1.630	
		V_{ILA} = −1.440V or V_{IHA} = −1.035V	85℃	—	—	−1.595	

■ AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30 ~ +85℃)

Item	Symbol	Input	Output	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	data	Z	R_L = 50Ω	−30℃	1.5	—	4.7	ns
					25℃	1.5	3.0	4.5	
					85℃	1.6	—	4.8	
	t_{PHL}				−30℃	1.5	—	4.7	ns
					25℃	1.5	3.0	4.5	
					85℃	1.6	—	4.8	
	t_{PLH}	address	Z		−30℃	1.9	—	6.3	ns
					25℃	2.0	4.0	6.0	
					85℃	2.2	—	6.5	
	t_{PHL}				−30℃	1.9	—	6.3	ns
					25℃	2.0	4.0	6.0	
					85℃	2.2	—	6.5	
	t_{PLH}	$\overline{\text{Enable}}$	Z		−30℃	0.9	—	3.3	ns
					25℃	1.0	2.0	2.9	
					85℃	1.0	—	3.1	
	t_{PHL}				−30℃	0.9	—	3.3	ns
					25℃	1.0	2.0	2.9	
					85℃	1.0	—	3.1	
Rise/Fall Time	t_{TLH}		Z		−30℃	0.9	—	3.3	ns
					25℃	1.1	2.0	3.3	
					85℃	1.2	—	3.6	
	t_{THL}				−30℃	0.9	—	3.3	ns
					25℃	1.1	2.0	3.3	
					85℃	1.2	—	3.6	

■ SWITCHING TIME TEST CIRCUIT

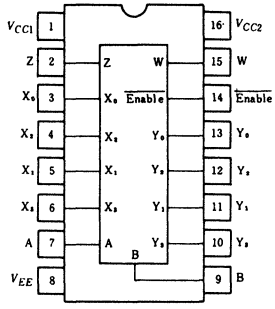




Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected in a 50Ω resistor to ground.

Dual 4 to 1 Multiplexers

■PIN ARRANGEMENT



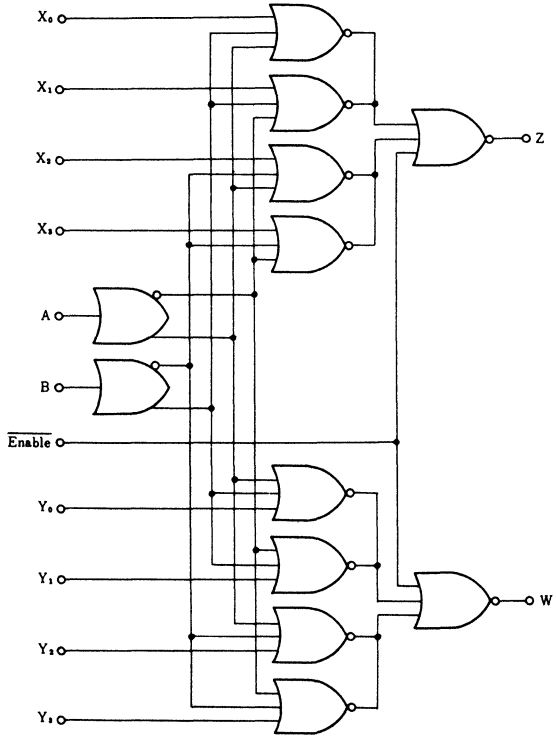
(Top View)

■FUNCTION TABLE

Enable	Address Inputs		Outputs	
$\overline{Enable}$	B	A	Z	W
H	×	×	L	L
L	L	L	X_0	Y_0
L	L	H	X_1	Y_1
L	H	L	X_2	Y_2
L	H	H	X_3	Y_3

× : Don't Care

■BLOCK DIAGRAM



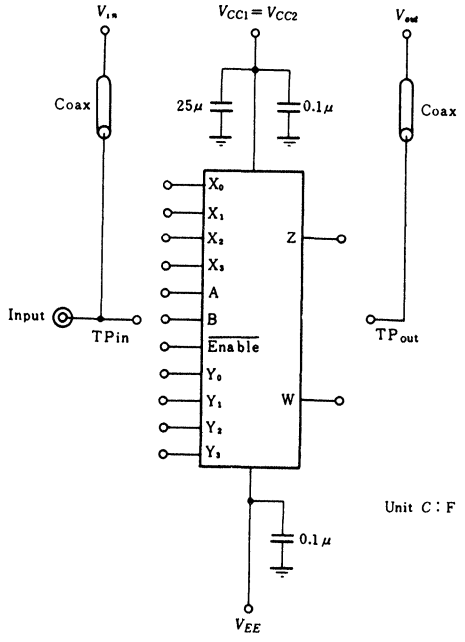
■ DC CHARACTERISTICS (V_{EE} = −5.2V, Ta = −30 ~ +85°C)

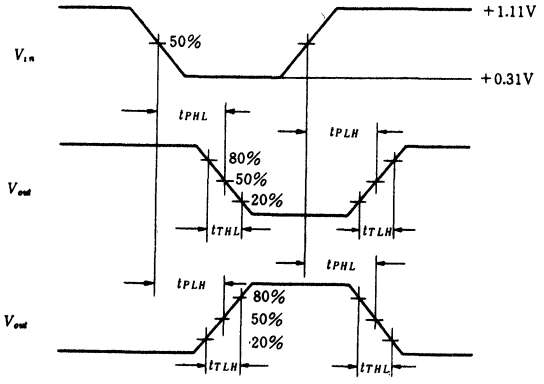
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	58	73	mA
Input Current	I_{IH}	V_{IH} = −0.810V	Data	25°C	—	—	220	μA
			Enable		—	—	330	
	I_{IL}	V_{IL} = −1.850V		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	V_{IH} = −0.890V or V_{IL} = −1.890V		−30°C	−1.060	—	−0.890	V
		V_{IH} = −0.810V or V_{IL} = −1.850V		25°C	−0.960	—	−0.810	
		V_{IH} = −0.700V or V_{IL} = −1.825V		85°C	−0.890	—	−0.700	
	V_{OL}	V_{IL} = −1.890V or V_{IH} = −0.890V		−30°C	−1.890	—	−1.675	V
		V_{IL} = −1.850V or V_{IH} = −0.810V		25°C	−1.850	—	−1.650	
		V_{IL} = −1.825V or V_{IH} = −0.700V		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	V_{IHA} = −1.205V or V_{ILA} = −1.500V		−30°C	−1.080	—	—	V
		V_{IHA} = −1.105V or V_{ILA} = −1.475V		25°C	−0.980	—	—	
		V_{IHA} = −1.035V or V_{ILA} = −1.440V		85°C	−0.910	—	—	
	V_{OLA}	V_{ILA} = −1.500V or V_{IHA} = −1.205V		−30°C	—	—	−1.655	V
		V_{ILA} = −1.475V or V_{IHA} = −1.105V		25°C	—	—	−1.630	
		V_{ILA} = −1.440V or V_{IHA} = −1.035V		85°C	—	—	−1.595	

■ AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30 ~ +85°C.)

Item	Symbol	Input	Output	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	Data	Z, W	R_L = 50Ω	−30°C	1.4	—	4.8	ns
					25°C	1.5	3.5	4.5	
					85°C	1.4	—	4.8	
	t_{PHL}				−30°C	1.4	—	4.8	ns
					25°C	1.5	3.5	4.5	
					85°C	1.4	—	4.8	
	t_{PLH}	Address	Z, W		−30°C	1.9	—	6.4	ns
					25°C	2.0	5.0	6.0	
					85°C	2.1	—	6.4	
	t_{PHL}				−30°C	1.9	—	6.4	ns
					25°C	2.0	5.0	6.0	
					85°C	2.1	—	6.4	
	t_{PLH}	Enable	Z, W		−30°C	1.0	—	3.1	ns
					25°C	1.0	2.0	2.9	
					85°C	0.9	—	3.2	
	t_{PHL}				−30°C	1.0	—	3.1	ns
					25°C	1.0	2.0	2.9	
					85°C	0.9	—	3.2	
Rise Time	t_{TLH}		Z, W		−30°C	1.0	—	3.4	ns
					25°C	1.1	2.0	3.3	
					85°C	1.1	—	3.6	
Fall Time	t_{THL}				−30°C	1.0	—	3.4	ns
					25°C	1.1	2.0	3.3	
					85°C	1.1	—	3.6	

■ SWITCHING TIME TEST CIRCUIT



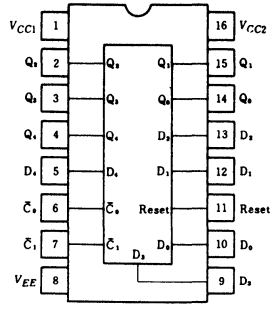


Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

Quintuple Latches

The HD10175 is a high speed, low power quint latch. It features five D type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are "OR"ed together.
Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latches on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled only when the clock is in the high state.

■PIN ARRANGEMENT



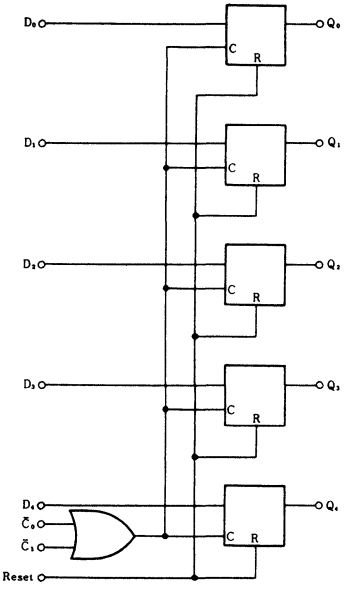
(Top View)

■FUNCTION TABLE

D	$\overline{C_0}$	$\overline{C_1}$	Reset	Q_{n+1}
L	L	L	L	L
H	L	L	L	H
×	H	×	L	Q_n
×	×	H	L	Q_n
×	H	×	H	L
×	×	H	H	L

× : Don't Care

■BLOCK DIAGRAM



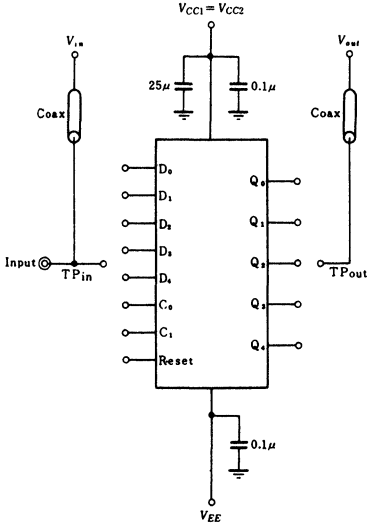
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	78	97	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	Clock, Data	25°C	—	—	290	μA
			Reset		—	—	650	
	I_{IL}	$V_{IL}=-1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$, $V_{IL}=-1.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$, $V_{IL}=-1.850V$		25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$, $V_{IL}=-1.825V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$, $V_{IH}=-0.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$, $V_{IH}=-0.810V$		25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$, $V_{IH}=-0.700V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$		−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$		25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$		−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$		25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$		85°C	—	—	−1.595	

■ AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30 ~ +85°C)

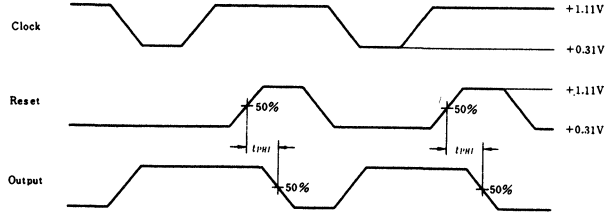
Item	Symbol	Input	Output	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	Data	Q	R_L=50Ω	−30°C	1.0	—	3.6	ns
					25°C	1.0	—	3.5	
					85°C	1.0	—	3.6	
	t_{PHL}				−30°C	1.0	—	3.6	ns
					25°C	1.0	—	3.5	
					85°C	1.0	—	3.6	
	t_{PLH}	Clock	Q		−30°C	1.0	—	4.7	ns
					25°C	1.0	—	4.3	
					85°C	1.0	—	4.4	
	t_{PHL}				−30°C	1.0	—	4.7	ns
					25°C	1.0	—	4.3	
					85°C	1.0	—	4.4	
	t_{PHL}	Reset	Q		−30°C	0.9	—	4.0	ns
					25°C	1.0	—	3.9	
					85°C	1.0	—	4.2	
Setup Time	t_{su}	D → C	Q		25°C	—	—	2.5	ns
Hold Time	t_h				25°C	—	—	1.5	ns
Rise/Fall Time	t_{TLH}		Q		−30°C	1.0	—	3.6	ns
					25°C	1.1	—	3.5	
					85°C	1.1	—	3.7	
	t_{THL}				−30°C	1.0	—	3.6	ns
					25°C	1.1	—	3.5	
					85°C	1.1	—	3.7	

■ SWITCHING TIME TEST CIRCUIT

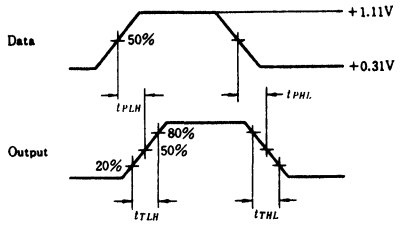


Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

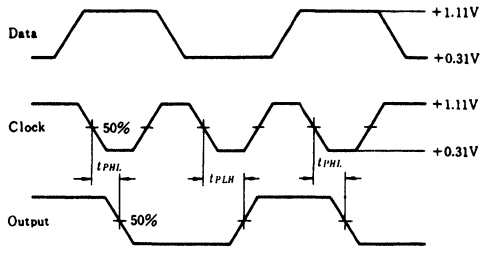
1. Reset



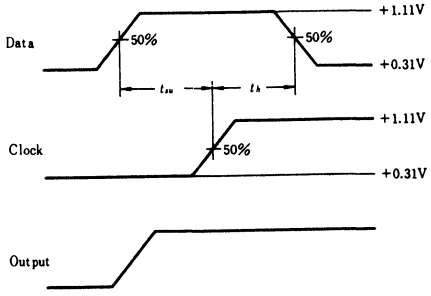
2. Data



3. Clock



4. Setup and Hold



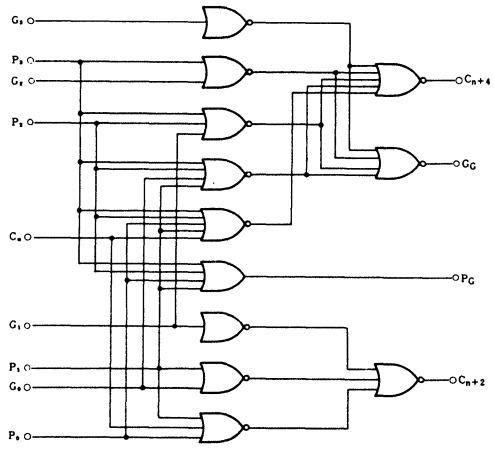
Notes) 1. t_{SU} is minimum time before the positive transition of the clock pulse that information must be present at the data.
2. t_h is the minimum time after the positive transition of the clock pulse that information must remain unchanged at the data.

HD10179

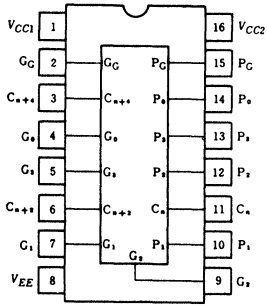
Look-Ahead Carry Block

The HD10179 is a high speed, low power, standard ECL complex function that is designed to perform the look-ahead carry function. This device can be used with the HD10181 4-unit ALU directly, or with the HD10180 dual arithmetic unit in any computer, instrumentation or digital communication application requiring high speed arithmetic operation on long words.

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

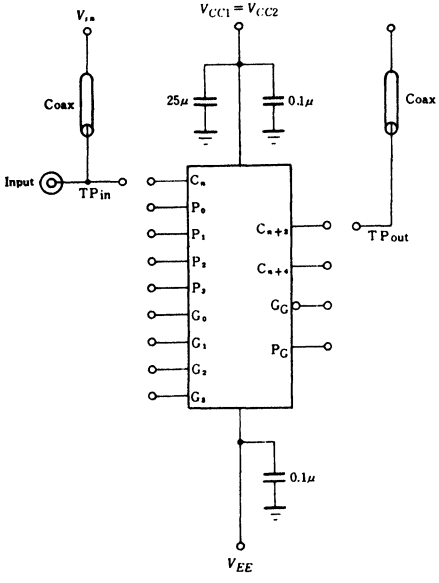
■ DC CHARACTERISTICS ($V_{EE} = -5.2V$, $Ta = -30 \sim +85°C$)

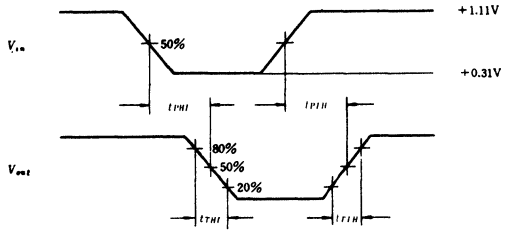
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	58	72	mA
Input Current	I_{IH}	$V_{IH} = -0.810V$	G_0, G_1, Cn	25°C	—	—	270	μA
			G_2, G_3		—	—	225	
			P_1, P_3		—	—	440	
			P_2		—	—	395	
			P_0		—	—	355	
	I_{IL}	$V_{IL} = -1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH} = -0.890V$ or $V_{IL} = -1.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH} = -0.810V$ or $V_{IL} = -1.850V$		25°C	−0.960	—	−0.810	
		$V_{IH} = -0.700V$ or $V_{IL} = -1.825V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL} = -1.890V$ or $V_{IH} = -0.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IL} = -1.850V$ or $V_{IH} = -0.810V$		25°C	−1.850	—	−1.650	
		$V_{IL} = -1.825V$ or $V_{IH} = -0.700V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA} = -1.205V$ or $V_{ILA} = -1.500V$		−30°C	−1.080	—	—	V
		$V_{IHA} = -1.105V$ or $V_{ILA} = -1.475V$		25°C	−0.980	—	—	
		$V_{IHA} = -1.035V$ or $V_{ILA} = -1.440V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA} = -1.500V$ or $V_{IHA} = -1.205V$		−30°C	—	—	−1.655	V
		$V_{ILA} = -1.475V$ or $V_{IHA} = -1.105V$		25°C	—	—	−1.630	
		$V_{ILA} = -1.440V$ or $V_{IHA} = -1.035V$		85°C	—	—	−1.595	

■AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = 25°C)

Item	Symbol	Input	Output	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	G_3	C_{n+4}	R_L = 50Ω	1.0	—	5.5	ns
	t_{PHL}				1.0	—	5.5	
	t_{PLH}	Cn	C_{n+2}		1.0	—	5.5	
	t_{PHL}				1.0	—	5.5	
	t_{PLH}	G_3	G_G		1.0	—	5.5	
	t_{PHL}				1.0	—	5.5	
	t_{PLH}	P_1	C_{n+2}		1.0	—	5.5	
	t_{PHL}				1.0	—	5.5	
	t_{PLH}	P_1	P_G		1.0	—	3.5	
	t_{PHL}				1.0	—	3.5	
Rise Time	t_{TLH}	Cn	C_{n+2}		1.1	—	3.5	ns
Fall Time	t_{THL}				1.1	—	3.5	ns

■SWITCHING TIME TEST CIRCUIT



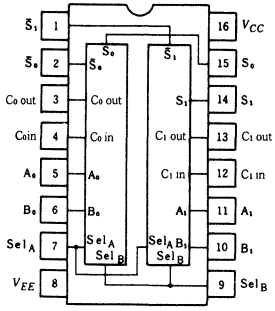


Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

Dual 2-bit Adders/Subtractors

The HD10180 is a high speed, low power, general-purpose adder/subtractor. Inputs for each adder are Carry-in, operand A, and operand B; outputs are Sum, $\overline{\text{Sum}}$, and Carry-out. The common Select inputs serve as a control line to invert A for subtract, and a control line to invert B.

■PIN ARRANGEMENT



(Top View)

■FUNCTION SELECT TABLE

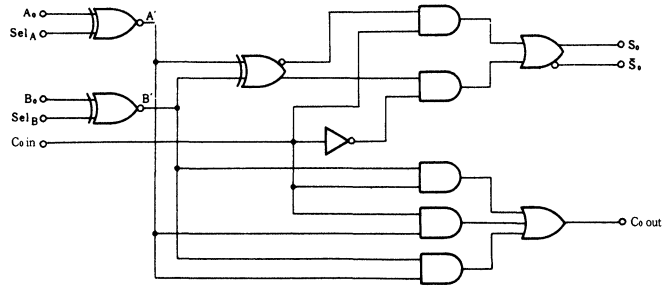
Sel_A	Sel_B	Function
H	H	S = A + B
H	L	S = A − B
L	H	S = B − A
L	L	S = 0 − A − B

■FUNCTION TABLE

Function	Inputs					Outputs		
	Sel_A	Sel_B	A_0	B_0	Cin	S_0	$\overline{S_0}$	Cout
ADD	H	H	L	L	L	L	H	L
	H	H	L	L	H	H	L	L
	H	H	L	H	L	H	L	L
	H	H	L	H	H	L	H	H
	H	H	H	L	L	H	L	L
	H	H	H	L	H	L	H	H
	H	H	H	H	L	L	H	H
	H	H	H	H	H	H	L	H
SUBTRACT	H	L	L	L	L	H	L	L
	H	L	L	L	H	L	H	H
	H	L	L	H	L	L	H	L
	H	L	L	H	H	H	L	L
	H	L	H	L	L	L	H	H
	H	L	H	L	H	H	L	H
	H	L	H	H	L	H	L	L
	H	L	H	H	H	L	H	H

Function	Inputs					Outputs		
	Sel_A	Sel_B	A_0	B_0	Cin	S_0	$\overline{S_0}$	Cout
REVERSE SUBTRACT	L	H	L	L	L	H	L	L
	L	H	L	L	H	L	H	H
	L	H	L	H	L	L	H	H
	L	H	L	H	H	H	L	H
	L	H	H	L	L	L	H	L
	L	H	H	L	H	H	L	L
	L	H	H	H	L	H	L	L
	L	H	H	H	H	L	H	H
	L	L	L	L	L	L	H	H
	L	L	L	L	H	H	L	H
	L	L	L	H	L	H	L	L
	L	L	L	H	H	L	H	H
	L	L	H	L	L	H	L	L
	L	L	H	L	H	L	H	H
	L	L	H	H	L	L	H	L
	L	L	H	H	H	H	L	L

■BLOCK DIAGRAM



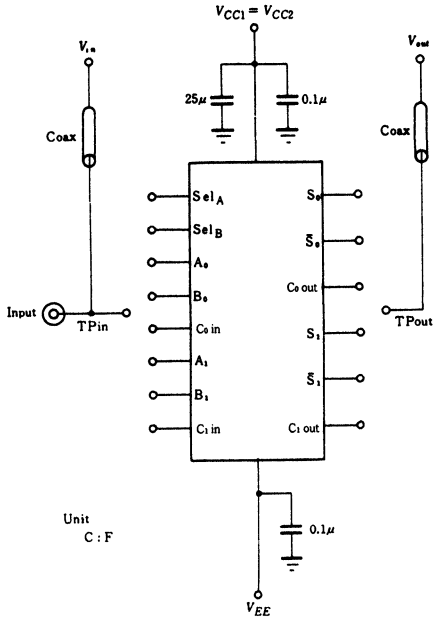
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85℃$)

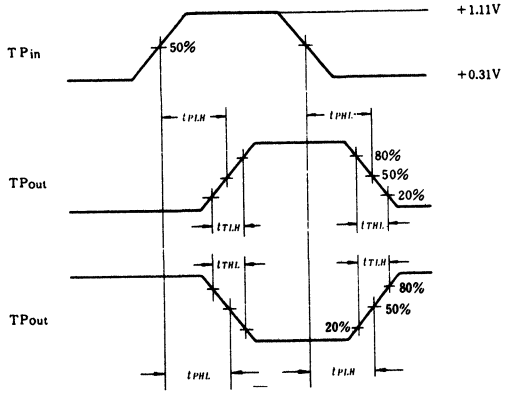
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25℃	—	70	86	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	Cin	25℃	—	—	370	μA
			A, B		—	—	220	
			Sel_A, Sel_B		—	—	290	
	I_{IL}	$V_{IL}=-1.850V$		25℃	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$		−30℃	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$		25℃	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$		85℃	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$		−30℃	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$		25℃	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$		85℃	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$		−30℃	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$		25℃	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$		85℃	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$		−30℃	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$		25℃	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$		85℃	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85℃$)

Item		Symbol	Input	Output	Test Condition		min	typ	max.	Unit
Propagation Delay Time	Operand	t_{PLH} t_{PHL}	A_0	S_0	$R_l=50Ω$	−30℃	1.3	—	5.8	ns
						25℃	1.3	—	5.4	
						85℃	1.1	—	5.8	
			B_0	S_0		−30℃	1.3	—	5.8	
						25℃	1.3	—	5.4	
						85℃	1.1	—	5.8	
	Cin		Cin	S_0		−30℃	1.0	—	3.4	
						25℃	1.0	—	3.3	
						85℃	0.9	—	3.6	
			Cin	Cout		−30℃	1.0	—	3.4	
						25℃	1.0	—	3.3	
						85℃	0.9	—	3.6	
	Select		Sel_A	S_0		−30℃	1.3	—	5.8	
						25℃	1.3	—	5.4	
						85℃	1.1	—	5.8	
			Sel_B	S_0		−30℃	1.3	—	5.8	
						25℃	1.3	—	5.4	
						85℃	1.1	—	5.8	
Rise Time		t_{TLH}	A_0	S_0		−30℃	1.0	—	3.8	ns
						25℃	1.1	—	3.7	
						85℃	1.1	—	3.9	
Fall Time		t_{THL}				−30℃	1.0	—	3.8	ns
						25℃	1.1	—	3.7	
						85℃	1.1	—	3.9	

■SWITCHING TIME TEST CIRCUIT





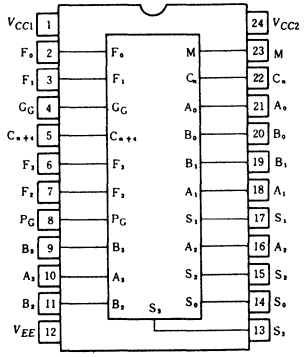
Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

HD10181

4-bit Arithmetic Logic Unit/Function Generator

The HD10181 is a high-speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four-bit words. Full internal carry is incorporated for ripple through operation. Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the table of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast operations on very long words using a second order look-ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

■ PIN ARRANGEMENT



(Top View)

■ FUNCTIONS OF PIN NUMBER

Pin No.	Function
A_3, A_2, A_1, A_0	Word A Inputs
B_3, B_2, B_1, B_0	Word B Inputs
S_3, S_2, S_1, S_0	Function-Select Inputs
C_n	Ripple-Carry Input
M	Mode Control Input
F_3, F_2, F_1, F_0	Function Outputs
P_G	Carry Propagate Output
C_{n+4}	Ripple-Carry Output
G_G	Carry-Generate Output

■ FUNCTION TABLE

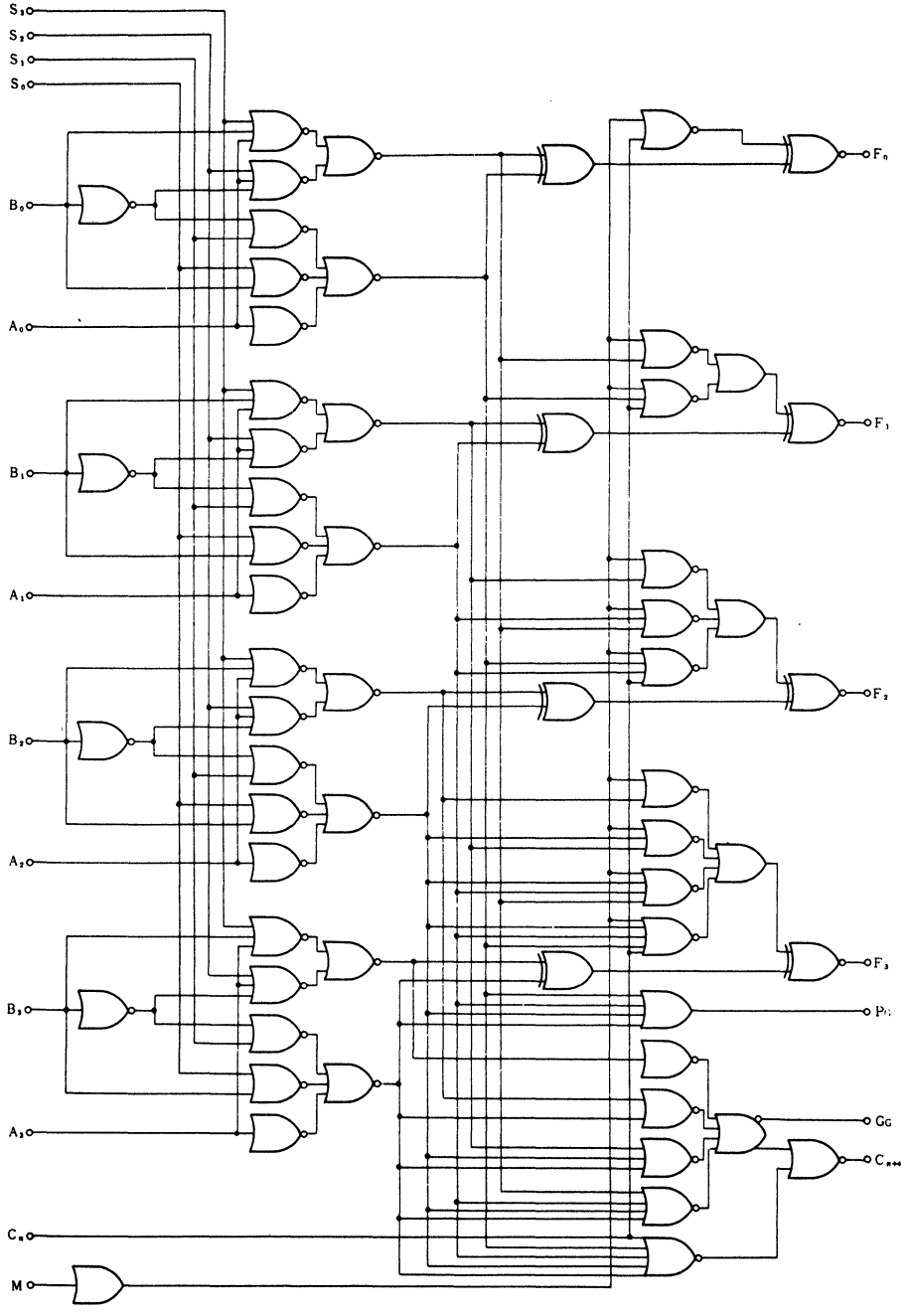
1. Positive Logic

Function Select				Logic Function (M="H")	Arithmetic Operation (M="L", Cn="L")
S_3	S_2	S_1	S_0	F	F
L	L	L	L	$F=\overline{A}$	$F=A+0$
L	L	L	H	$F=\overline{A}+\overline{B}$	$F=A+(A\cdot\overline{B})$
L	L	H	L	$F=\overline{A}+B$	$F=A+(A\cdot B)$
L	L	H	H	F="H"	$F=A\times 2$
L	H	L	L	$F=\overline{A}\cdot\overline{B}$	$F=(A+B)+0$
L	H	L	H	$F=\overline{B}$	$F=(A+B)+(A\cdot\overline{B})$
L	H	H	L	$F=\overline{A\oplus B}$	$F=A+B$
L	H	H	H	$F=A+\overline{B}$	$F=A+(A+B)$
H	L	L	L	$F=\overline{A}\cdot B$	$F=(A+\overline{B})+0$
H	L	L	H	$F=A\oplus B$	$F=A-B-1$
H	L	H	L	$F=B$	$F=(A+\overline{B})+(A\cdot B)$
H	L	H	H	$F=A+B$	$F=(A+\overline{B})+A$
H	H	L	L	F="L"	F=−1 (two's complement)
H	H	L	H	$F=A\cdot\overline{B}$	$F=(A\cdot\overline{B})-1$
H	H	H	L	$F=A\cdot B$	$F=(A\cdot B)-1$
H	H	H	H	$F=A$	$F=A-1$

2. Negative Logic

Function Select				Logic Function (M="H")	Arithmetic Operation (M="L", Cn="H")
S_3	S_2	S_1	S_0	F	F
L	L	L	L	$F=\overline{A}$	$F=A-1$
L	L	L	H	$F=\overline{A+B}$	$F=A+(A+\overline{B})$
L	L	H	L	$F=\overline{A}\cdot B$	$F=A+(A+B)$
L	L	H	H	F="L"	$F=A\times 2$
L	H	L	L	$F=\overline{A\cdot B}$	$F=(A\cdot B)-1$
L	H	L	H	$F=\overline{B}$	$F=(A\cdot B)+(A+\overline{B})$
L	H	H	L	$F=A\oplus B$	$F=A+B$
L	H	H	H	$F=A\cdot\overline{B}$	$F=A+(A\cdot B)$
H	L	L	L	$F=\overline{A}+B$	$F=(A\cdot\overline{B})-0$
H	L	L	H	$F=\overline{A\oplus B}$	$F=A-B-1$
H	L	H	L	$F=B$	$F=(A\cdot\overline{B})+(A+B)$
H	L	H	H	$F=A\cdot B$	$F=(A\cdot\overline{B})+A$
H	H	L	L	F="H"	F=−1 (two's complement)
H	H	L	H	$F=A+\overline{B}$	$F=(A+\overline{B})+0$
H	H	H	L	$F=A+B$	$F=(A+B)+0$
H	H	H	H	$F=A$	$F=A+0$

■ BLOCK DIAGRAM



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85℃$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25℃	—	—	145	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	B_0, B_1, B_2, B_3	25℃	—	—	245	μA
			A_0, A_1, A_2, A_3		—	—	220	
			S_3, M		—	—	200	
			S_0, S_1, S_2		—	—	265	
			C_n		—	—	290	
	I_{IL}	$V_{IL}=-1.850V$		25℃	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$, $V_{IL}=-1.890V$		−30℃	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$, $V_{IL}=-1.850V$		25℃	−0.960	—	−0.810	
		$V_{IH}=-0.700V$, $V_{IL}=-1.825V$		85℃	−0.890	—	−0.700	
	V_{OL}	$V_{IH}=-0.890V$, $V_{IL}=-1.890V$		−30℃	−2.000	—	−1.675	V
		$V_{IH}=-0.810V$, $V_{IL}=-1.850V$		25℃	−1.990	—	−1.650	
		$V_{IH}=-0.700V$, $V_{IL}=-1.825V$		85℃	−1.920	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$, $V_{ILA}=-1.500V$		−30℃	−1.080	—	—	V
		$V_{IHA}=-1.105V$, $V_{ILA}=-1.475V$		25℃	−0.980	—	—	
		$V_{IHA}=-1.035V$, $V_{ILA}=-1.440V$		85℃	−0.910	—	—	
	V_{OLA}	$V_{IHA}=-1.205V$, $V_{ILA}=-1.500V$		−30℃	—	—	−1.655	V
		$V_{IHA}=-1.105V$, $V_{ILA}=-1.475V$		25℃	—	—	−1.630	
		$V_{IHA}=-1.035V$, $V_{ILA}=-1.440V$		85℃	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85℃$, $R_L=50Ω$)

Item	Symbol	Input	Output	High level input*	Ta	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	C_n	C_{n+4}	A_0, A_1, A_2, A_3	−30℃	1.0	—	5.1	ns
					25℃	1.1	3.1	5.0	
					85℃	1.1	—	5.4	
	t_{PHL}				−30℃	1.0	—	5.1	
					25℃	1.1	3.1	5.0	
					85℃	1.1	—	5.4	
Rise Time	t_{TLH}				−30℃	1.0	—	3.2	
					25℃	1.0	2.0	3.0	
					85℃	1.0	—	3.2	
Fall Time	t_{THL}				−30℃	1.0	—	3.2	
					25℃	1.0	2.0	3.0	
					85℃	1.0	—	3.2	
Propagation Delay Time	t_{PLH}	C_n	F_1	A_0	−30℃	1.7	—	7.2	
					25℃	2.0	4.5	7.0	
					85℃	2.0	—	7.5	
	t_{PHL}				−30℃	1.7	—	7.2	
					25℃	2.0	4.5	7.0	
					85℃	2.0	—	7.5	
Rise Time	t_{TLH}				−30℃	1.3	—	5.3	
					25℃	1.5	3.0	5.0	
					85℃	1.5	—	5.3	
Fall Time	t_{THL}				−30℃	1.3	—	5.3	
					25℃	1.5	3.0	5.0	
					85℃	1.5	—	5.3	

(to be continued)

■AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30 ~ +85°C, R_L = 50 Ω)

Item	Symbol	Input	Output	High level input*	Ta	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	A_1	F_1	—	−30°C	2.6	—	10.4	ns
					25°C	3.0	6.5	10.0	
					85°C	3.0	—	10.8	
	t_{PHL}				−30°C	2.6	—	10.4	
					25°C	3.0	6.5	10.0	
					85°C	3.0	—	10.8	
Rise Time	t_{TLH}				−30°C	1.3	—	5.4	
					25°C	1.5	3.0	5.0	
					85°C	1.5	—	5.3	
Fall Time	t_{THL}				−30°C	1.3	—	5.4	
					25°C	1.5	3.0	5.0	
					85°C	1.5	—	5.3	
Propagation Delay Time	t_{PLH}	A_1	P_G	S_0, S_3	−30°C	1.6	—	7.0	
					25°C	2.0	5.0	6.5	
					85°C	2.0	—	7.0	
	t_{PHL}				−30°C	1.6	—	7.0	
					25°C	2.0	5.0	6.5	
					85°C	2.0	—	7.0	
Rise Time	t_{TLH}				−30°C	0.8	—	3.7	
					25°C	1.1	2.0	3.5	
					85°C	1.1	—	3.8	
Fall Time	t_{THL}				−30°C	0.8	—	3.7	
					25°C	1.1	2.0	3.5	
					85°C	1.1	—	3.8	
Propagation Delay Time	t_{PLH}	A_1	G_G	A_0, A_2, A_3, C_n	−30°C	1.1	—	7.4	
					25°C	2.0	4.5	7.0	
					85°C	1.3	—	7.7	
	t_{PHL}				−30°C	1.1	—	7.4	
					25°C	2.0	4.5	7.0	
					85°C	1.3	—	7.7	
Rise Time	t_{TLH}				−30°C	1.2	—	5.1	
					25°C	1.5	4.0	5.0	
					85°C	1.2	—	5.3	
Fall Time	t_{THL}				−30°C	1.2	—	5.1	
					25°C	1.5	4.0	5.0	
					85°C	1.2	—	5.3	
Propagation Delay Time	t_{PLH}	A_1	C_{n+4}	A_0, A_2, A_3, C_n	−30°C	1.7	—	7.3	
					25°C	2.0	5.0	7.0	
					85°C	2.0	—	7.8	
	t_{PHL}				−30°C	1.7	—	7.3	
					25°C	2.0	5.0	7.0	
					85°C	2.0	—	7.8	
Rise Time	t_{TLH}				−30°C	1.0	—	3.1	
					25°C	1.0	2.0	3.0	
					85°C	1.0	—	3.2	
Fall Time	t_{THL}				−30°C	1.0	—	3.1	
					25°C	1.0	2.0	3.0	
					85°C	1.0	—	3.2	

(to be continued)

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85℃$, $R_L=50\,\Omega$)

Item	Symbol	Input	Output	High level input*	Ta	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	B_1	F_1	S_3, C_n	−30℃	2.7	—	11.3	ns
					25℃	3.0	8.0	11.0	
					85℃	3.0	—	11.9	
Rise Time	t_{TLH}				−30℃	1.2	—	5.3	
					25℃	1.5	3.5	5.0	
					85℃	1.5	—	5.3	
Fall Time	t_{THL}				−30℃	1.2	—	5.3	
					25℃	1.5	3.5	5.0	
					85℃	1.5	—	5.3	
Propagation Delay Time	t_{PLH}	B_1	P_G	S_0, S_3	−30℃	1.6	—	7.7	
					25℃	2.0	6.0	7.5	
					85℃	2.0	—	8.0	
	t_{PHL}				−30℃	1.6	—	7.7	
					25℃	2.0	6.0	7.5	
					85℃	2.0	—	8.0	
Rise Time	t_{TLH}				−30℃	1.0	—	3.6	
					25℃	1.1	2.0	3.5	
					85℃	1.1	—	3.9	
Fall Time	t_{THL}				−30℃	1.0	—	3.6	
					25℃	1.1	2.0	3.5	
					85℃	1.1	—	3.9	
Propagation Delay Time	t_{PLH}	B_1	G_G	S_3, C_n	−30℃	1.7	—	8.2	
					25℃	2.0	6.0	8.0	
					85℃	2.0	—	8.6	
	t_{PHL}				−30℃	1.7	—	8.2	
					25℃	2.0	6.0	8.0	
					85℃	2.0	—	8.6	
Rise Time	t_{TLH}				−30℃	1.4	—	5.2	
					25℃	1.5	3.0	5.0	
					85℃	1.2	—	5.4	
Fall Time	t_{THL}				−30℃	1.4	—	5.2	
					25℃	1.5	3.0	5.0	
					85℃	1.2	—	5.4	
Propagation Delay Time	t_{PLH}	B_1	C_{n+4}	S_3, C_n	−30℃	1.8	—	8.2	
					25℃	2.0	6.0	8.0	
					85℃	2.0	—	8.7	
	t_{PHL}				−30℃	1.8	—	8.2	
					25℃	2.0	6.0	8.0	
					85℃	2.0	—	8.7	
Rise Time	t_{TLH}				−30℃	0.9	—	3.1	
					25℃	1.0	2.0	3.0	
					85℃	1.0	—	3.2	
Fall Time	t_{THL}				−30℃	0.9	—	3.1	
					25℃	1.0	2.0	3.0	
					85℃	1.0	—	3.2	

(to be continued)

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85℃$, $R_L=50\Omega$)

Item	Symbol	Input	Output	High level input*	Ta	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	M	F_1	—	−30℃	2.4	—	10.3	ns
					25℃	3.0	6.5	10.0	
					85℃	3.0	—	10.8	
	t_{PHL}				−30℃	2.4	—	10.3	
					25℃	3.0	6.5	10.0	
					85℃	3.0	—	10.8	
Rise Time	t_{TLH}				−30℃	1.1	—	5.1	
					25℃	1.5	4.0	5.0	
					85℃	1.5	—	5.3	
Fall Time	t_{THL}				−30℃	1.1	—	5.1	
					25℃	1.5	4.0	5.0	
					85℃	1.5	—	5.3	
Propagation Delay Time	t_{PLH}	S_1	F_1	A_1, B_1	−30℃	2.5	—	10.7	
					25℃	3.0	6.5	10.0	
					85℃	3.0	—	10.8	
	t_{PHL}				−30℃	2.5	—	10.7	
					25℃	3.0	6.5	10.0	
					85℃	3.0	—	10.8	
Rise Time	t_{TLH}				−30℃	1.0	—	5.4	
					25℃	1.5	3.0	5.0	
					85℃	1.5	—	5.4	
Fall Time	t_{THL}				−30℃	1.0	—	5.4	
					25℃	1.5	3.0	5.0	
					85℃	1.5	—	5.4	
Propagation Delay Time	t_{PLH}	S_1	P_0	A_3, B_3	−30℃	1.7	—	8.3	
					25℃	2.0	6.0	8.0	
					85℃	2.0	—	8.4	
	t_{PHL}				−30℃	1.7	—	8.3	
					25℃	2.0	6.0	8.0	
					85℃	2.0	—	8.4	
Rise Time	t_{TLH}				−30℃	0.8	—	5.1	
					25℃	1.1	3.0	5.0	
					85℃	1.1	—	5.2	
Fall Time	t_{THL}				−30℃	0.8	—	5.1	
					25℃	1.1	3.0	5.0	
					85℃	1.1	—	5.2	
Propagation Delay Time	t_{PLH}	S_1	C_{n+4}	A_3, B_3	−30℃	1.6	—	9.3	
					25℃	2.0	6.0	9.0	
					85℃	2.0	—	9.9	
	t_{PHL}				−30℃	1.6	—	9.3	
					25℃	2.0	6.0	9.0	
					85℃	2.0	—	9.9	
Rise Time	t_{TLH}				−30℃	0.9	—	5.3	
					25℃	1.1	3.0	5.0	
					85℃	1.0	—	5.2	
Fall Time	t_{THL}				−30℃	0.9	—	5.3	
					25℃	1.1	3.0	5.0	
					85℃	1.0	—	5.2	

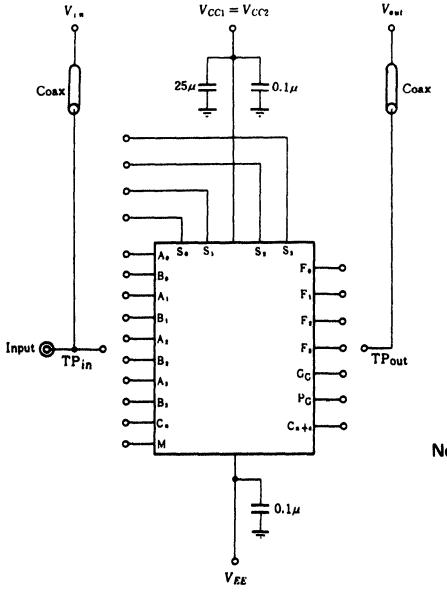
(to be continued)

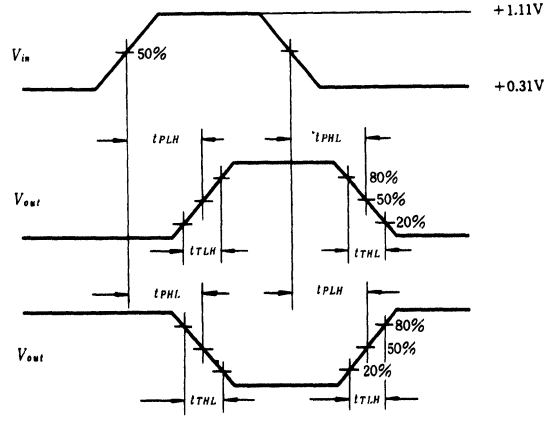
■ AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85℃$, $R_L=50\Omega$)

Item	Symbol	Input	Output	High level input*	Ta	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	S_1	G_G	A_3, B_3	−30℃	1.5	—	9.6	ns
					25℃	2.0	6.0	9.0	
					85℃	1.9	—	9.7	
	t_{PHL}				−30℃	1.5	—	9.6	
					25℃	2.0	6.0	9.0	
					85℃	1.9	—	9.7	
Rise Time	t_{TLH}				−30℃	0.8	—	6.2	
					25℃	0.8	3.0	6.0	
					85℃	0.8	—	6.5	
Fall Time	t_{THL}				−30℃	0.8	—	6.2	
					25℃	0.8	3.0	6.0	
					85℃	0.8	—	6.5	

Note) * : Other inputs are open, or connected to +0.31V.

■ SWITCHING TIME TEST CIRCUIT

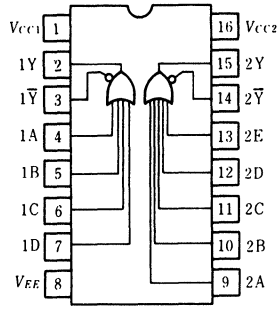




Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

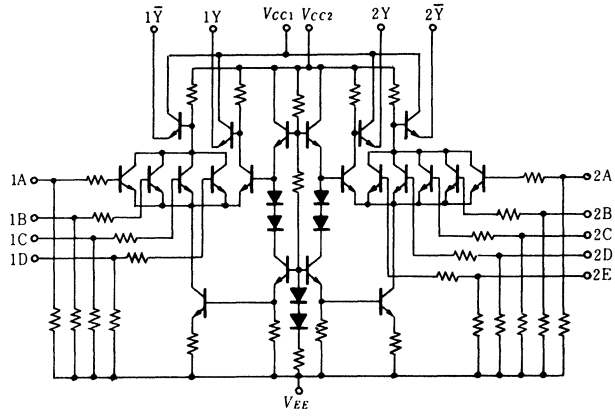
Dual 4-5-input OR/NOR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	11	14	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	25°C	—	—	265	μA
	I_{IL}	$V_{IL}=-1.850V$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$	−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$	25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$	85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$	−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$	25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$	−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$	25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$	85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$	−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$	25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$	85°C	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=25°C$)

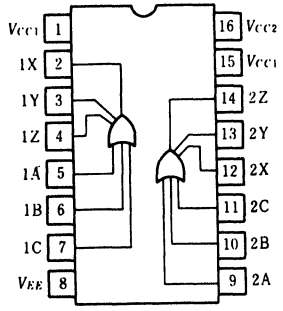
Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50Ω$	0.95	—	1.55	ns
	t_{PHL}		0.95	—	1.55	
Rise/Fall Time	t_{TLH}		0.90	—	2.50	
	t_{THL}		0.90	—	2.50	

Note) Please refer to test circuit and waveform of common item.

HD10210

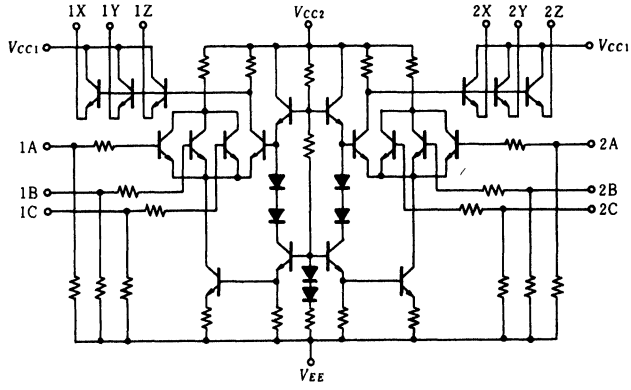
Dual 3-input 3-output OR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



■DC CHARACTERISTICS (V_{EE} = −5.2V, Ta = −30~+85°C)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	30	38	mA
Input Current	I_{IH}	V_{IH} = −0.810V	25°C	—	—	410	μA
	I_{IL}	V_{IL} = −1.850V		0.5	—	—	μA
Output Voltage	V_{OH}	V_{IH} = −0.890V or V_{IL} = −1.890V	−30°C	−1.060	—	−0.890	V
		V_{IH} = −0.810V or V_{IL} = −1.850V	25°C	−0.960	—	−0.810	
		V_{IH} = −0.700V or V_{IL} = −1.825V	85°C	−0.890	—	−0.700	
	V_{OL}	V_{IL} = −1.890V or V_{IH} = −0.890V	−30°C	−1.890	—	−1.675	V
		V_{IL} = −1.850V or V_{IH} = −0.810V	25°C	−1.850	—	−1.650	
		V_{IL} = −1.825V or V_{IH} = −0.700V	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	V_{IHA} = −1.205V or V_{ILA} = −1.500V	−30°C	−1.080	—	—	V
		V_{IHA} = −1.105V or V_{ILA} = −1.475V	25°C	−0.980	—	—	
		V_{IHA} = −1.035V or V_{ILA} = −1.440V	85°C	−0.910	—	—	
	V_{OLA}	V_{ILA} = −1.500V or V_{IHA} = −1.205V	−30°C	—	—	−1.655	V
		V_{ILA} = −1.475V or V_{IHA} = −1.105V	25°C	—	—	−1.630	
		V_{ILA} = −1.440V or V_{IHA} = −1.035V	85°C	—	—	−1.595	

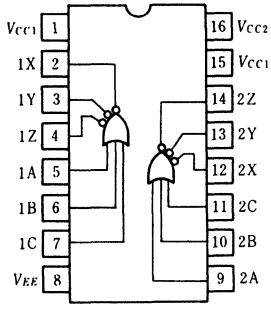
■AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = 25°C)

Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	R_L=50Ω	0.95	1.5	2.5	ns
	t_{PHL}		0.95	1.5	2.5	
Rise/Fall Time	t_{TLH}		0.90	1.5	2.5	
	t_{THL}		0.90	1.5	2.5	

Note) Please refer to test circuit and waveform of common item.

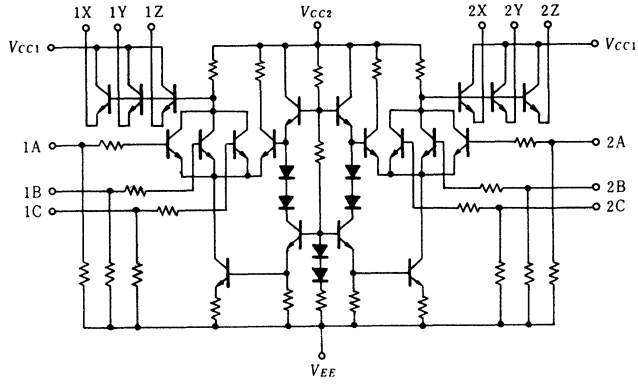
Dual 3-input 3-output NOR Gates

■ PIN ARRANGEMENT



(Top View)

■ CIRCUIT SCHEMATIC



■ DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}		25°C	—	—	38	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	25°C	—	—	410	μA
	I_{IL}	$V_{IL}=-1.850V$		0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$	−30°C	−1.060	—	−0.890	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$	25°C	−0.960	—	−0.810	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$	85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$	−30°C	−1.890	—	−1.675	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$	25°C	−1.850	—	−1.650	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$	85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$	−30°C	−1.080	—	—	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$	25°C	−0.980	—	—	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$	85°C	−0.910	—	—	
	V_{OLA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$	−30°C	—	—	−1.655	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$	25°C	—	—	−1.630	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$	85°C	—	—	−1.595	

■ AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=25°C$)

Item	Symbol	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$R_L=50Ω$	0.95	1.5	2.5	ns
	t_{PHL}		0.95	1.5	2.5	
Rise/Fall Time	t_{TLH}		0.90	1.5	2.5	
	t_{THL}		0.90	1.5	2.5	

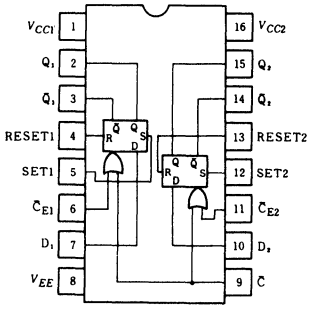
Note) Please refer to test circuit and waveform of common item.

HD10230

High Speed Dual D-type Latches

The HD10230 is a clocked dual D type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock($\overline{C}$). Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data reset inputs do not override the clock and D inputs. They are effective only when either $\overline{C}$ or $\overline{CE}$ or both are high.

■ PIN ARRANGEMENT



(Top View)

■ FUNCTION

D	$\bar{C}$	$\bar{C}_E$	Q_{n+1}
L	L	L	L
H	L	L	H
×	L	H	Q_n
×	H	L	Q_n
×	H	H	Q_n

× : Don't Care

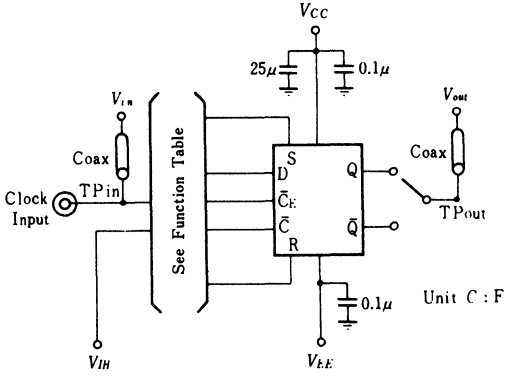
■ DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

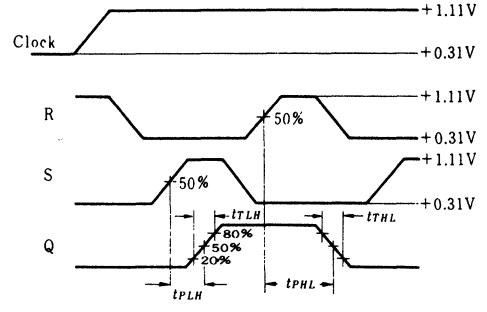
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	—	41	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	$\bar{C}_E$	25°C	—	—	255	μA
			$\bar{C}$		—	—	310	
			Other inputs		—	—	355	
	I_{IL}	$V_{IL}=-1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$ or $V_{IL}=-1.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$ or $V_{IL}=-1.850V$		25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$ or $V_{IL}=-1.825V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$ or $V_{IH}=-0.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$ or $V_{IH}=-0.810V$		25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$ or $V_{IH}=-0.700V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$ or $V_{ILA}=-1.500V$		−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$ or $V_{ILA}=-1.475V$		25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$ or $V_{ILA}=-1.440V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$ or $V_{IHA}=-1.205V$		−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$ or $V_{IHA}=-1.105V$		25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$ or $V_{IHA}=-1.035V$		85°C	—	—	−1.595	

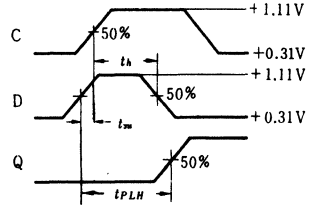
■AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = 25°C)

Item	Symbol	Input	Output	Test Condition	min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$\overline{C}$, $\overline{C}_E$	Q, $\overline{Q}$	R_L=50Ω, C_L=3.5pF	—	1.2	2.0	ns
	t_{PHL}				—	1.2	2.0	
	t_{PLH}	D	Q, $\overline{Q}$		—	1.0	1.8	
	t_{PHL}				—	1.0	1.8	
	t_{PLH}	S, R	Q, $\overline{Q}$		—	1.2	2.0	
	t_{PHL}				—	1.2	2.0	
Rise/Fall Time	t_{TLH}	—	Q, $\overline{Q}$		—	1.5	2.5	ns
	t_{THL}				—	1.5	2.5	
Setup Time	t_{su}	$\overline{C}$→D	Q, $\overline{Q}$		—	—	2.0	ns
Hold Time	t_h				—	—	1.0	ns

■SWITCHING TIME TEST CIRCUIT







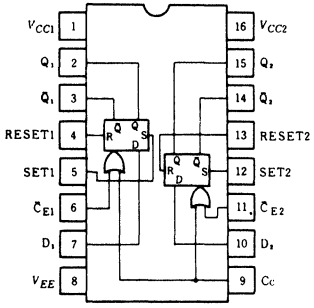
Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope and equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. t_{su} is the minimum time before the positive transition of the clock pulse that information must be present at the data.
4. t_h is the minimum time after the positive transition of the clock pulse that information must remain unchanged at the data.
5. Input Pulse; t_{TLH}=t_{THL}=1.5±0.2ns (20% to 80%).

HD10231

High Speed Dual D-type Master-Slave Flip Flops

The HD10231 is a dual master-slave type D flip-flop. Asynchronous Set(S) and Reset(R) override Clock (C_C) and Clock Enable ($\overline{CE}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.
The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data(D) input will not affect the output information at any other time due to master-slave construction.

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

●R-S

R	S	Q_{n+1}	$\overline{Q}_{n+1}$
L	L	Q_n	$\overline{Q}_n$
L	H	H	L
H	L	L	H
H	H	×	×

× : Don't Care

●CLOCK

C	D	Q_{n+1}
L	×	Q_n
↑	L	L
↑	H	H

1. × : Don't Care
2. $C = \overline{C}_E + C_C$
3. ↑ : transition from low to high

■DC CHARACTERISTICS ($V_{EE} = -5.2V$, $Ta = -30 \sim +85°C$)

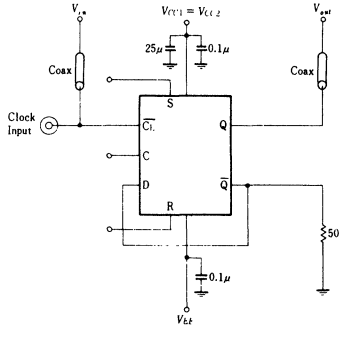
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	52	65	mA
Input Current	I_{IH}	$V_{IH} = -0.810V$	D, $\overline{C_E}$	25°C	—	—	220	μA
			C_C		—	—	290	
			S, R		—	—	410	
	I_{IL}	$V_{IL} = -1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH} = -0.890V$ or $V_{IL} = -1.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH} = -0.810V$ or $V_{IL} = -1.850V$		25°C	−0.960	—	−0.810	
		$V_{IH} = -0.700V$ or $V_{IL} = -1.825V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL} = -1.890V$ or $V_{IH} = -0.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IL} = -1.850V$ or $V_{IH} = -0.810V$		25°C	−1.850	—	−1.650	
		$V_{IL} = -1.825V$ or $V_{IH} = -0.700V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA} = -1.205V$ or $V_{ILA} = -1.500V$		−30°C	−1.080	—	—	V
		$V_{IHA} = -1.105V$ or $V_{ILA} = -1.475V$		25°C	−0.980	—	—	
		$V_{IHA} = -1.035V$ or $V_{ILA} = -1.440V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA} = -1.500V$ or $V_{IHA} = -1.205V$		−30°C	—	—	−1.655	V
		$V_{ILA} = -1.475V$ or $V_{IHA} = -1.105V$		25°C	—	—	−1.630	
		$V_{ILA} = -1.440V$ or $V_{IHA} = -1.035V$		85°C	—	—	−1.595	

■AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30 ~ +85°C)

Item	Symbol	Input	Output	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$\overline{C}$, $\overline{C}_E$	Q, $\overline{Q}$	R_L=50Ω,	−30°C	1.4	—	3.4	ns
					25°C	1.5	—	3.3	
					85°C	1.5	—	3.7	
	t_{PHL}				−30°C	1.4	—	3.4	
					25°C	1.5	—	3.3	
					85°C	1.5	—	3.7	
	t_{PLH}	S	Q, $\overline{Q}$		−30°C	1.0	—	3.4	
					25°C	1.1	—	3.3	
					85°C	1.1	—	3.7	
	t_{PHL}				−30°C	1.0	—	3.4	
					25°C	1.1	—	3.3	
					85°C	1.1	—	3.7	
	t_{PLH}	R	Q, $\overline{Q}$		−30°C	1.0	—	3.4	
					25°C	1.1	—	3.3	
					85°C	1.1	—	3.7	
	t_{PHL}				−30°C	1.0	—	3.4	
					25°C	1.1	—	3.3	
					85°C	1.1	—	3.7	
Rise Time	t_{TLH}		Q, $\overline{Q}$		−30°C	0.9	—	3.3	ns
					25°C	1.0	—	3.1	
					85°C	1.0	—	3.5	
Fall Time	t_{THL}				−30°C	0.9	—	3.3	ns
					25°C	1.0	—	3.1	
					85°C	1.0	—	3.5	
Setup Time	t_{su}	D → $\overline{C}$	Q, $\overline{Q}$		25°C	—	—	1.0	ns
Hold Time	t_h				25°C	—	—	0.75	ns
Max. Toggle Frequency	f_{Tog}	—	—		−30°C	200	—	—	MHz
					25°C	200	250	—	
					85°C	200	—	—	

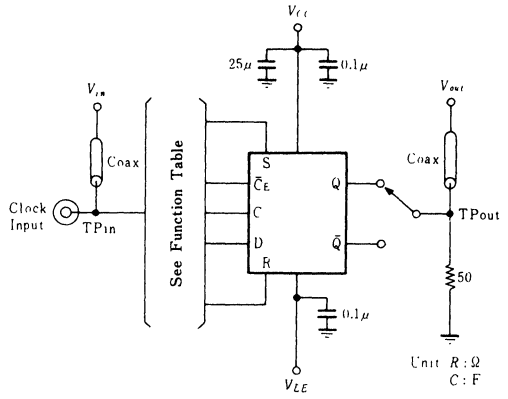
■TEST CIRCUIT OF AC CHARACTERISTICS

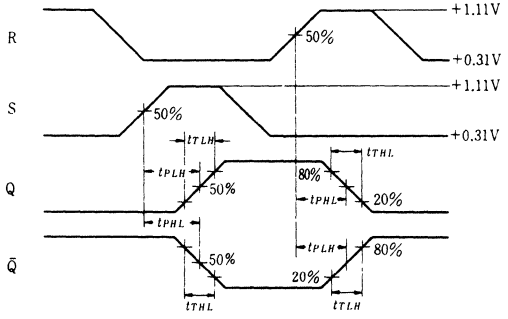
1. Toggle Frequency

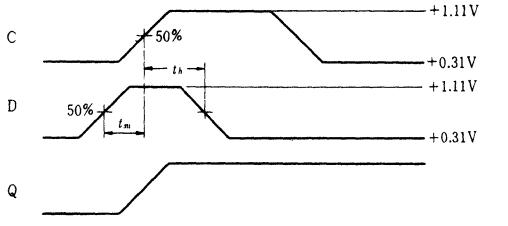


Notes) 1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.

2. Switching Time







Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. t_{su} is the minimum time before the positive transition of the clock pulse that information must be present at the data.
4. t_h is the minimum time after the positive transition of the clock pulse that information must remain unchanged at data.
5. Input Pulse; $t_{TLH}=t_{THL}=1.5\pm0.2$ns (20% to 80%).

HD100K Series

COMMON DC CHARACTERISTICS OF HD100K SERIES

■ $V_{EE}=-4.5V$, $V_{CC}=V_{CCA}=GND$, $Ta=0$ to $+85℃$

Item	Symbol	Test Condition		min	typ	max	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	$R_L=50Ω$	−1025	− 955	− 880	mV
	V_{OL}		$V_{TT}=-2.0V$	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	$R_L=50Ω$	−1035	—	—	mV
	V_{OLC}		$V_{TT}=-2.0V$	—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	− 880	mV
	V_{IL}			−1810	—	−1475	mV
Input Low Current	I_{IL}	$V_{IN}=V_{IL\ min}$		0.50	—	—	μA

■ $V_{EE}=-4.2V$, $V_{CC}=V_{CCA}=GND$, $Ta=0$ to $+85℃$

Item	Symbol	Test Condition		min	typ	max	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	$R_L=50Ω$	−1025	− 955	− 880	mV
	V_{OL}		$V_{TT}=-2.0V$	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	$R_L=50Ω$	−1035	—	—	mV
	V_{OLC}		$V_{TT}=-2.0V$	—	—	−1610	mV
Input Voltage	V_{IH}			−1150	—	− 880	mV
	V_{IL}			−1810	—	−1475	mV
Input Low Current	I_{IL}	$V_{IN}=V_{IL\ min}$		0.50	—	—	μA

■ $V_{EE}=-4.8V$, $V_{CC}=V_{CCA}=GND$, $Ta=0$ to $+85℃$

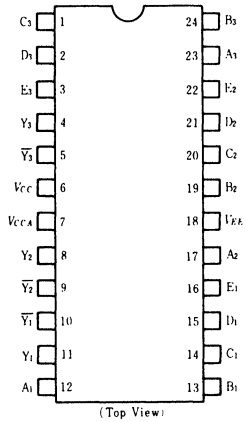
Item	Symbol	Test Condition		min	typ	max	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IH\ max}$ or $V_{IN}=V_{IL\ min}$	$R_L=50Ω$	−1025	− 955	− 880	mV
	V_{OL}		$V_{TT}=-2.0V$	−1810	−1705	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IH\ min}$ or $V_{IN}=V_{IL\ max}$	$R_L=50Ω$	−1035	—	—	mV
	V_{OLC}		$V_{TT}=-2.0V$	—	—	−1610	mV
Input Voltage	V_{IH}			−1165	—	− 880	mV
	V_{IL}			−1810	—	−1490	mV
Input Low Current	I_{IL}	$V_{IN}=V_{IL\ min}$		0.50	—	—	μA

Note) As for other items, refer to the DC characteristics of each device.

Triple 5-input OR/NOR Gates

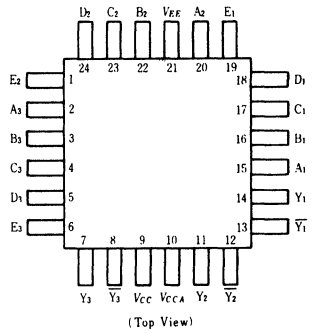
■PIN ARRANGEMENT

● HD100101



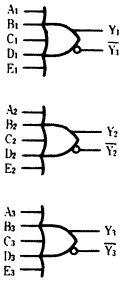
(Top View)

● HD100101F



(Top View)

■LOGIC DIAGRAM



■DC CHARACTERISTICS ($V_{EE}=-4.2$ to -4.8V, $V_{CC}=V_{CCA}$=GND, Ta=0 to +85℃)

Item	Symbol	Test Condition	min	typ	max	Unit
Supply Current	I_{EE}	All input open	18	26	38	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	—	—	350	μA

Note) As for other items, refer to the "Common DC characteristics".

■AC CHARACTERISTICS ($V_{EE}=-2.2$ to -2.8V, $V_{CC}=V_{CCA}$=2.0V)

● HD100101

Item	Symbol	Test Condition	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveforms	0.45	1.15	0.50	0.75	1.15	0.50	1.20	ns
Transition Time	t_{TLH} t_{THL}		0.30	1.10	0.35	0.70	1.10	0.35	1.10	ns

● HD100101F

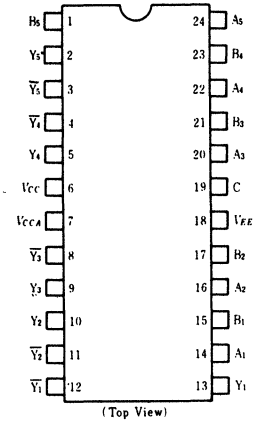
Item	Symbol	Test Condition	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveforms	0.45	0.90	0.45	0.75	0.90	0.45	1.05	ns
Transition Time	t_{TLH} t_{THL}		0.40	1.00	0.45	0.70	1.00	0.45	1.00	ns

Notes) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

Quintuple 2-input OR/NOR Gates

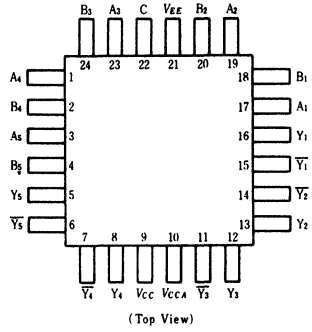
■PIN ARRANGEMENT

● HD100102



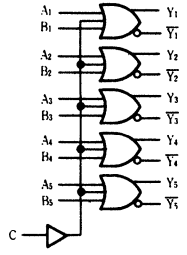
(Top View)

● HD100102F



(Top View)

■LOGIC DIAGRAM



■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		38	55	80	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$	Enable	—	—	300	μA
			All input except Enable	—	—	350	μA

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V,)

● HD100102

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}	See test circuit and waveform	Data→Output	0.50	1.20	0.50	0.75	1.25	0.50	1.30	ns
	t_{PHL}		Enable→Output	0.90	2.00	0.90	1.50	2.00	0.95	2.00	
Transition Time	t_{TLH}			0.40	1.20	0.40	0.70	1.20	0.40	1.10	ns
	t_{THL}										

● HD100102F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}	See test circuit and waveform	Data→Output	0.50	0.95	0.50	0.75	0.95	0.50	1.05	ns
	t_{PHL}		Enable→Output	0.90	1.95	0.90	1.50	1.95	0.90	2.00	
Transition Time	t_{TLH}			0.45	1.10	0.45	0.70	1.10	0.45	1.05	ns
	t_{THL}										

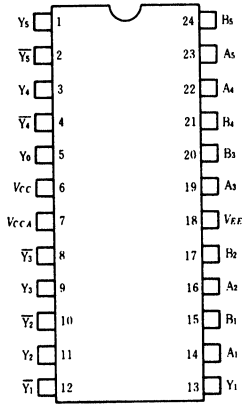
Note) the circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100107/F

Quintuple Exclusive-OR/NOR Gates

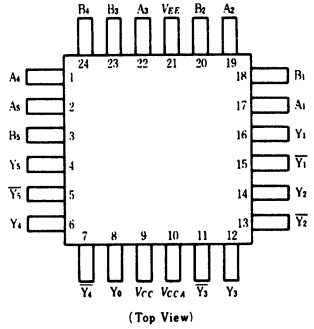
■ PIN ARRANGEMENT

● HD100107



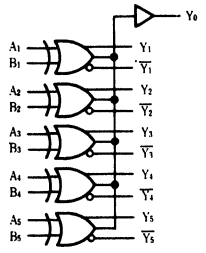
(Top View)

● HD100107F



(Top View)

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		46	66	96	mA
Input Current	I_{IH}	V_{IN} = $V_{IH\ max}$	B_1, B_2, B_3, B_4, B_5	—	—	250	μA
			A_1, A_2, A_3, A_4, A_5	—	—	350	μA

Note) As for other itema, refer to the "Common DC Characteristics".

■ AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100107

Item	Symbol	Test Condition		0℃		25℃			85℃		UnIt
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	A_n input→Y_n, $\overline{Y_n}$	0.55	1.70	0.55	1.10	1.70	0.55	1.70	ns
			B_n input→Y_n, $\overline{Y_n}$	0.55	1.60	0.55	0.90	1.60	0.55	1.60	
			Data→Y_0	1.00	2.65	1.10	1.85	2.65	1.10	2.65	
Transition Time	t_{TLH} t_{THL}			0.40	1.20	0.40	0.70	1.20	0.40	1.20	ns

● HD100107F

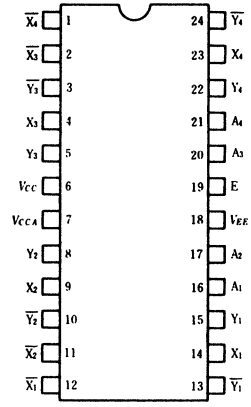
Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	A_n input→Y_n, $\overline{Y_n}$	0.55	1.55	0.55	1.10	1.55	0.55	1.65	ns
			B_n input→Y_n, $\overline{Y_n}$	0.55	1.20	0.55	0.90	1.20	0.55	1.30	
			Data→Y_0	1.05	2.55	1.15	1.85	2.55	1.15	2.55	
Transition Time	t_{TLH} t_{THL}			0.45	1.20	0.45	0.70	1.20	0.45	1.20	ns

Notes) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

Quadruple Drivers

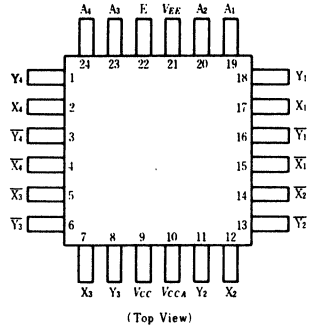
■ PIN ARRANGEMENT

● HD100112



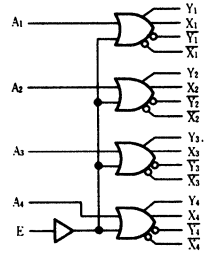
(Top View)

● HD100112F



(Top View)

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		51	73	106	mA
Input Current	I_{IH}	V_{IN} = $V_{IH\ max}$	E	—	—	450	μA
			All input except E	—	—	550	μA

Note) As for other items, refer to the "Common DC Characteristics".

■ AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100112

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}	See test circuit and waveform	E→Xn, Yn, $\overline{X_n}$, $\overline{Y_n}$	0.80	1.85	0.85	1.30	1.85	0.85	1.85	ns
	t_{PHL}		Data→Xn, Yn, $\overline{X_n}$, $\overline{Y_n}$	0.55	1.40	0.55	0.90	1.40	0.55	1.40	
Transition Time	t_{TLH}			0.40	1.40	0.45	0.90	1.40	0.45	1.40	ns
	t_{THL}										

● HD100112F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}	See test circuit and waveform	E→Xn, Yn, $\overline{X_n}$, $\overline{Y_n}$	0.80	1.70	0.85	1.30	1.70	0.85	1.70	ns
	t_{PHL}		Data→Xn, Yn, $\overline{X_n}$, $\overline{Y_n}$	0.55	1.25	0.60	0.90	1.25	0.60	1.25	
Transition Time	t_{TLH}			0.40	1.40	0.45	0.90	1.40	0.45	1.40	ns
	t_{THL}										

Notes) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

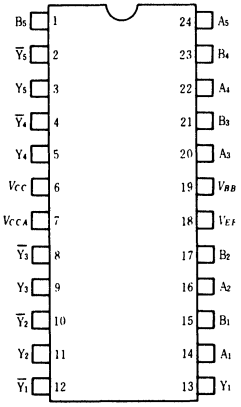
Quint. Differential Line Receivers

The HD100114 is a Quint. Differential Amp. with emitter-follower outputs. An internal reference supply (V_{BB}) is available for single ended reception. Active current sources provide common mode rejection of 1.5V in either the positive or negative direction.

A defined output state exists if both inputs are at the same potential between and including $-V_{EE}$ and V_{CC}. The defined state is logic high on outputs $\overline{Y}n$.

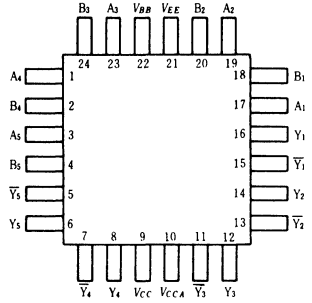
■ PIN ARRANGEMENT

● HD100114



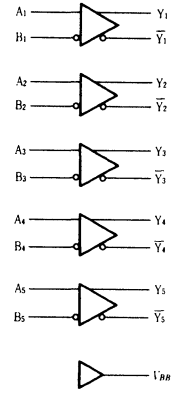
(Top View)

● HD100114F



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE

Input		Output	
A_n	B_n	Y_n	$\overline{Y_n}$
H	V_{BB}	H	L
L	V_{BB}	L	H
V_{BB}	H	L	H
V_{BB}	L	H	L
$A_n - B_n \geqq 0.15$ V		H	L
$A_n - B_n \leqq 0.0$ V		L	H
$0.0 < A_n - B_n < 0.15$ V		*	*
Open	Open	L	H
V_{CC}	V_{CC}	L	H
V_{EE}	V_{EE}	L	H

H = High level
L = Low level
V_{BB} = Base bias voltage
* = Undefined

■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition	min	typ	max	Unit
Supply Current	I_{EE}	A_n = V_{BB}, B_n = $V_{IL\ min}$	51	73	106	mA
Input Current	I_{IH}	V_{IN} = $V_{IH\ max}$, A_n = V_{BB}, B_n = $V_{IL\ min}$	—	20	50	μA
Leakage Current	I_{CBO}	V_{IN} = V_{EE}, A_n = V_{BB}, B_n = $V_{IL\ min}$	—	—	1.0	μA
Common Mode Voltage	V_{CM}	Permissible V_{CM} with respect to V_{CC}	−2.30	—	−0.55	V
Reference Voltage	V_{BB}	Tie A_1, A_2, A_3, A_4, A_5 to V_{BB}	−1380	−1320	−1260	mV
Input Voltage Differential	V_{DIFF}		150	—	—	mV

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100114

Item	Symbol	Test Condition	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	0.65	1.95	0.65	1.20	2.00	0.65	2.00	ns
Transition Time	t_{TLH} t_{THL}		0.35	1.10	0.35	0.70	1.10	0.35	1.05	ns

● HD100114F

Item	Symbol	Test Condition	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	0.65	1.75	0.65	1.20	1.80	0.65	1.80	ns
Transition Time	t_{TLH} t_{THL}		0.45	1.10	0.45	0.90	1.10	0.40	1.05	ns

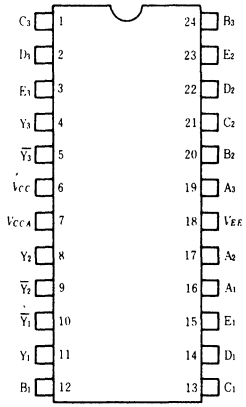
Notes) The circuits in a test soket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100117/F

Triple 2-wide OR-AND/OR-AND-INVERT Gates

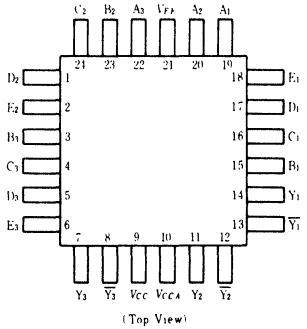
■ PIN ARRANGEMENT

● HD100117



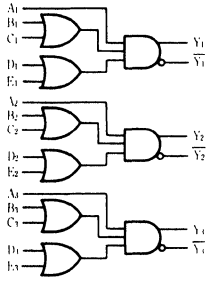
(Top View)

● HD100117F



(Top View)

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		37	54	79	mA
Input Current	I_{IH}	V_{IN} = $V_{IH\ max}$	A_n	—	—	350	μA
			B_n~E_n	—	—	220	μA

Note) As for other items, refer to the "Common DC Characteristics".

■ AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100117

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagotion Delay Time	t_{PLH}	See test circuit and waveform	A_n→Y_n, $\overline{Y_n}$	0.45	1.30	0.45	0.75	1.30	0.45	1.35	ns
	t_{PHL}		B_n~E_n→Y_n, $\overline{Y_n}$	0.90	2.40	0.90	1.70	2.40	0.90	2.40	
Transition Time	t_{TLH}			0.35	1.10	0.35	0.75	1.10	0.35	1.10	ns
	t_{THL}										

● HD100117F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}	See test circuit and waveform	A_n→Y_n, $\overline{Y_n}$	0.45	0.95	0.45	0.75	0.95	0.50	1.05	ns
	t_{PHL}		B_n~E_n→Y_n, $\overline{Y_n}$	0.95	2.10	0.95	1.55	2.10	0.95	2.20	
Transition Time	t_{TLH}			0.40	1.05	0.40	0.75	1.05	0.40	1.05	ns
	t_{THL}										

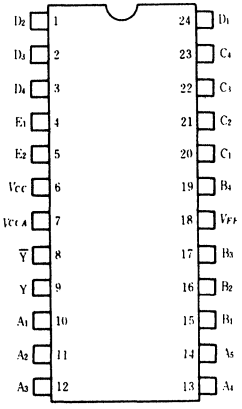
Notes) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100118/F

5-wide OR-AND/OR-AND-INVERT Gate

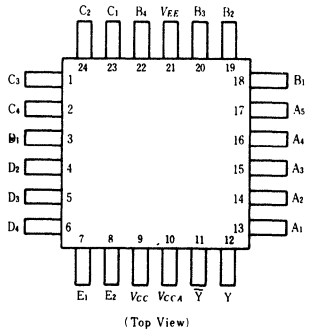
■ PIN ARRANGEMENT

● HD100118



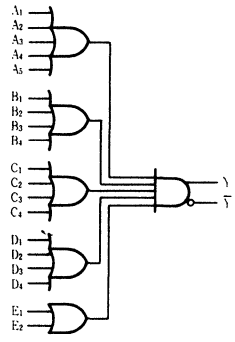
(Top View)

● HD100118F



(Top View)

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		27	39	57	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$	A input	—	—	350	μA
			B~E input	—	—	240	μA

Note) As for other items, refer to the "Common DC Characteristics".

■ AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100118

Item	Symbol	Test Condition	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	0.95	1.90	0.95	1.40	1.90	0.95	1.95	ns
Transition Time	t_{TLH} t_{THL}		0.30	1.35	0.30	0.75	1.35	0.30	1.35	ns

● HD100118F

Item	Symbol	Test Condition	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	0.80	1.90	0.85	1.40	1.90	0.85	1.95	ns
Transition Time	t_{TLH} t_{THL}		0.35	1.20	0.35	0.75	1.20	0.35	1.20	ns

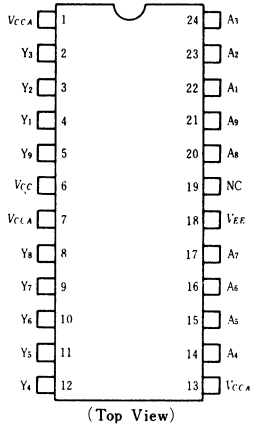
Notes) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

9-bit Buffer

The HD100122 contains nine independent, high speed, buffer gates each with a single input and a single output. The gates are non-inverting. These buffers are useful in bus oriented systems where minimal output loading or bus isolation is desired.

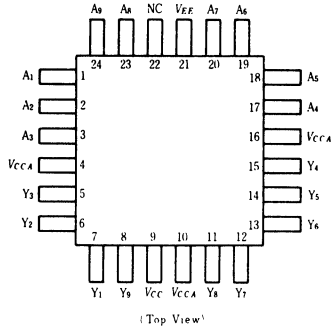
■ PIN ARRANGEMENT

● HD100122



(Top View)

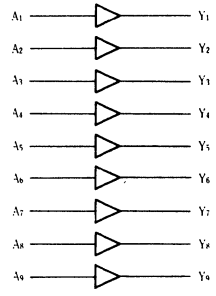
● HD100122F



(Top View)

Note) NC : No connection

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition	min	typ	max	Unit
Supply Current	I_{EE}	All input open	47	70	95.5	mA
Input Current	I_{IH}	V_{IN} = $V_{IH\ max}$	—	—	350	μA

Note) As for other items, refer to the "Common DC Characteristics".

■ AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100122

Item	Symbol	Test Condition	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	0.45	1.40	0.45	0.90	1.45	0.55	1.50	ns
Transition Time	t_{TLH} t_{THL}		0.45	1.40	0.45	0.90	1.40	0.45	1.40	ns

● HD100122F

Item	Symbol	Test Condition	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	0.45	1.05	0.45	0.70	1.05	0.45	1.15	ns
Transition Time	t_{TLH} t_{THL}		0.45	1.10	0.45	0.70	1.10	0.45	1.10	ns

Notes) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100123/F

Hex Bus Drivers

The HD100123 contains six bus drivers capable of driving terminated lines with terminations as low as 25Ω. To reduce crosstalk, each output has its respective ground connection and transition times were designed to be longer than on other HD100K devices.

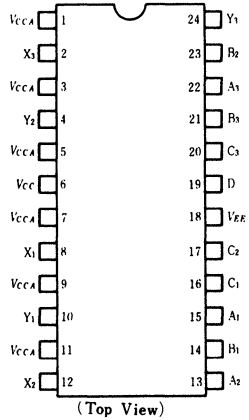
The driver itself performs the positive logic AND of a data input (A, B inputs) and the OR of two select inputs (C, D inputs).

The output voltage low level is designed to be more negative than normal ECL outputs.

This allows an emitter-follower output transistor to turn off when the termination supply is −2.0V ±10%, and thus present a high impedance to the data bus.

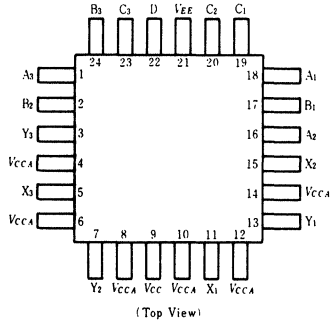
■ PIN ARRANGEMENT

● HD100123



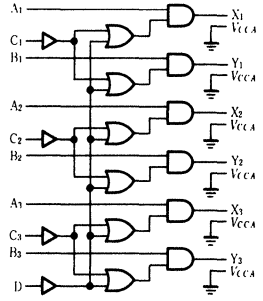
(Top View)

● HD100123F



(Top View)

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}	All input open			113	162	235	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$	A, B, C input		—	—	230	μA
			D input		—	—	330	μA
	I_{IL}	$V_{IN} = V_{IL\ min}$			0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IN} = V_{IH\ max}$ or	R_T = 25Ω	V_{TT} = −2.0 V	−1025	−955	−880	mV
	V_{OL}	$V_{IN} = V_{IL\ min}$		V_{TT} = −2.3 V	—	—	−2200	mV
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IH\ min}$ or	R_T = 25Ω	V_{TT} = −2.0 V	−1035	—	—	mV
	V_{OLC}	$V_{IN} = V_{IL\ max}$		V_{TT} = −2.3 V	—	—	−2200	mV
Input Voltage	V_{IH}				−1165	—	−880	mV
	V_{IL}				−1810	—	−1475	mV

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100123

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}	See test circuit and wavcform	A, B input	1.80	3.90	1.85	3.00	4.00	1.85	4.00	ns
	t_{PHL}			0.95	2.00	1.00	1.30	2.10	1.00	2.10	
	t_{PLH}		C input	2.05	4.40	2.10	3.40	4.50	2.10	4.50	
	t_{PHL}			1.30	2.50	1.40	1.80	2.50	1.40	2.50	
	t_{PLH}		D input	2.10	4.80	2.20	3.50	4.90	2.20	4.90	
	t_{PHL}			1.40	2.45	1.50	1.80	2.55	1.50	2.55	
Transition Time	t_{TLH}			0.70	1.80	0.75	1.30	1.80	0.75	1.80	ns
	t_{THL}			0.40	1.10	0.45	0.80	1.20	0.45	1.20	

● HD100123F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}	See test circuit and waveform	A, B input	1.90	3.90	1.95	2.50	4.00	1.95	4.00	ns
	t_{PHL}			0.95	1.80	1.00	1.30	1.90	1.00	1.90	
	t_{PLH}		C input	2.10	4.20	2.15	2.50	4.30	2.15	4.30	
	t_{PHL}			1.40	2.25	1.40	1.70	2.35	1.40	2.35	
	t_{PLH}		D input	2.30	4.60	2.40	2.70	4.70	2.40	4.70	
	t_{PHL}			1.40	2.25	1.50	1.70	2.35	1.50	2.35	
Transition Time	t_{TLH}			0.75	1.70	0.80	1.00	1.70	0.80	1.70	ns
	t_{THL}			0.45	1.10	0.45	0.65	1.20	0.45	1.20	

Notes) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

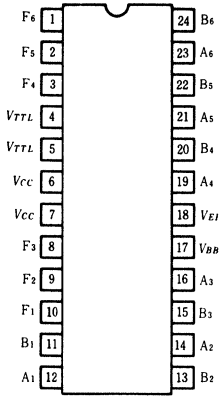
HD100125/F

Hex ECL-to-TTL Translators

The HD100125 is a Hex Translator for converting HD100K logic levels to TTL logic levels. Differential inputs allow each circuits to be used as an inverting, non-inverting or as a differential receiver. An internal reference voltage generator provides V_{BB} on pin 17 for single-ended operation or for use in Schmitt trigger applications. The outputs, which will go low when the inputs are left unconnected, have a fan-out of 10 Schottky TTL loads. When used in the differential mode, the inputs have a common mode rejection of −1V, making this device tolerant of ground offsets and transients between the signal source and the translator.

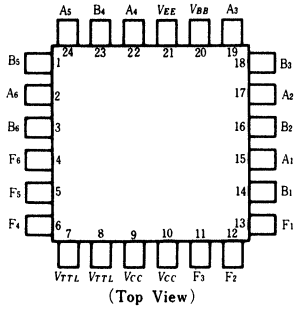
■ PIN ARRANGEMENT

● HD100125



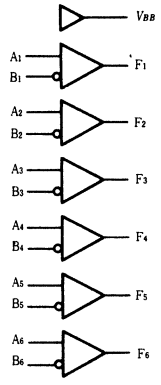
(Top View)

● HD100125F



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE

Inputs		Output
In	$\overline{In}$	On
L	H	L
H	L	H
L	L	*
H	H	*
Open	Open	L
V_{EE}	V_{EE}	L
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	L	H
V_{BB}	H	L

* Undetermind

■ DC CHARACTERISTICS (V_{EE} = −4.2 to +4.8V, V_{CC} = GND = 0V, V_{TTL} = 4.5 to 5.5V, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	$I_{OH}=-2.0$mA	2.5	—	—	V
	V_{OL}		$I_{OL}=20$mA	—	—	0.5	V
	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	$I_{OH}=-2.0$mA	2.5	—	—	V
	V_{OLC}		$I_{OL}=20$mA	—	—	0.5	V
Common Mode Voltage	V_{CM}	V_{CM} ref. to V_{BB} (Notes 1)		—	—	1.0	V
Input Voltage Differential	V_{DIFF}	Required for full output voltage swing		150	—	—	mV
Reference Voltage	V_{BB}	$V_{IN}=V_{ILB}$		−1380	−1320	−1260	mV
Input Current	I_{IL}	$V_{IN}=V_{EE}$ (Notes 2)		5.0	—	—	μA
	I_{IH}	$V_{IN}=V_{IHA}$ (Notes 2)		—	—	350	μA
Short Circuit Current	I_{OS}	V_{IN} = GND (Notes 3)		−100	—	−40	mA
Power Supply Current	I_{EE}	Inputs and Outputs Open		36	65	85	mA
TTL Drive Current	I_{TTL}	$V_{IN}=V_{ILB}$ (Notes 4)		50	88	115	mA

Notes) 1. $V_{CM}=V_{BB}\pm1$V (V_{DIFF} = 150mV)
2. Complementary Input = V_{BB}
3. One Output at a Time
4. True Inputs = V_{BB}, Complementary Inputs = V_{ILB}

■AC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = GND, V_{TTL} = 4.5 to 5.5V)

● HD100125

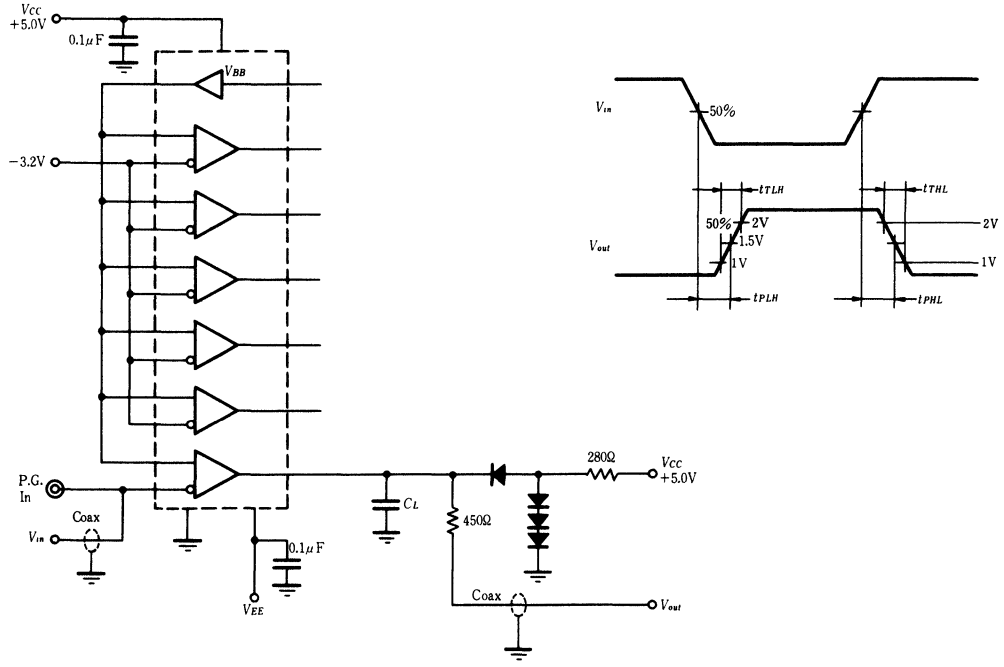
Item	Symbol	Test Condition	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	1.10	3.70	1.10	2.20	3.70	1.10	3.90	ns
Transition Time	t_{TLH} t_{THL}		0.20	1.80	0.20	0.60	1.80	0.20	1.80	ns

● HD100125F

Item	Symbol	Test Condition	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	1.10	3.50	1.10	2.20	3.50	1.10	3.70	ns
Transition Time	t_{TLH} t_{THL}		0.20	1.50	0.20	0.60	1.50	0.20	1.50	ns

Notes) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

■SWITHCING TIME TEST CIRCUIT AND WAVEFORM



Notes)
1. 50Ω termination to ground located in each scope channel input.
2. All input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be <½ inch from TPin to input pin and TPout to output pin.
3. C_L=25pF including.
4. One input from each gate must be tied to V_{BB}.

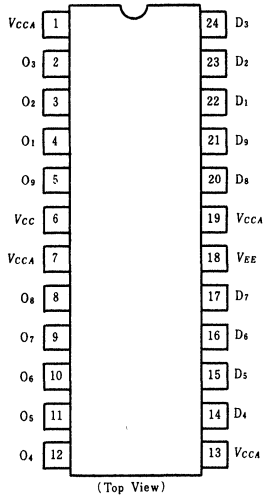
HD100126/F

9-bit Backplane Driver

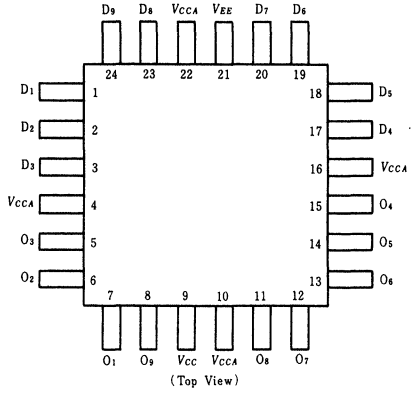
The HD100126 contains nine independent, high speed, buffer gates each with a single input and a single output.
The gates are non-inverting. These buffers are useful in bus-oriented systems where minimal output loading or bus isolation is desired. The output transition times are longer to minimize moise when used as a backplane driver.

■PIN ARRANGEMENT

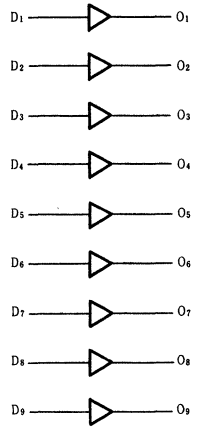
● HD100126



● HD100126F



■LOGIC SYMBOL



■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition	min	typ	max	Unit
Supply Current	I_{EE}	All inputs open	46	70	96	mA
Input Current	I_{IH}	V_{IN} = $V_{IH\ max}$	—	—	350	μA

Note) As for other items, refer to the "Common DC Characteriatics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100126

Item	Symbol	Test Condition	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	1.05	2.75	1.05	1.90	2.75	1.05	2.75	ns
Transition Time	t_{TLH} t_{THL}		1.15	3.40	1.15	2.55	3.40	1.05	3.40	ns

● HD100126F

Item	Symbol	Test Condition	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	1.05	2.55	1.05	1.85	2.55	1.05	2.55	ns
Transition Time	t_{TLH} t_{THL}		1.15	3.30	1.15	2.50	3.30	1.05	3.30	ns

Note) The circuit in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

Triple D-type Latches

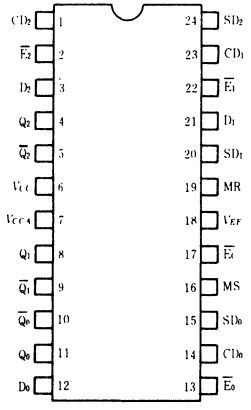
The HD100130 contains three D-type latches with true and complement outputs and with Common Enable ($\overline{Ec}$), Master Set (MS) and Master Reset (MR) inputs. Each latch has its own Enable ($\overline{En}$), Direct Set (SDn) and Direct Clear (CDn) inputs.

The Q output follows its Data (D) input when both $\overline{En}$ and $\overline{Ec}$ are low. When either $\overline{En}$ or $\overline{Ec}$ or both are high, a latch stores the last valid data present on its Dn input before $\overline{En}$ or $\overline{Ec}$ when high. Both Master Reset (MR) and Master Set (MS) inputs override the Enable inputs.

The individual CDn and SDn also override the Enable inputs.

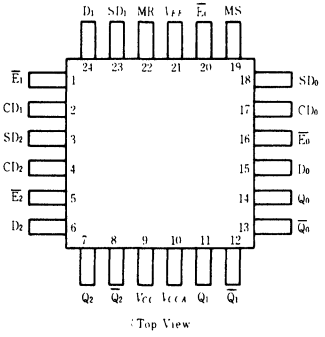
■PIN ARRANGEMENT

●HD100130



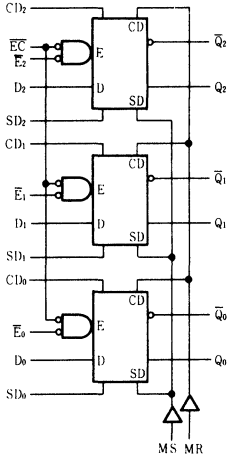
(Top View)

●HD100130F



(Top View)

■LOGIC DIAGRAM



■TRUTH TABLE

D_n	$\overline{E_n}$	$\overline{Ec}$	MS SD_n	MR CD_n	Q_n
L	L	L	L	L	L
H	L	L	L	L	H
×	H	×	L	L	*
×	×	H	L	L	*
×	×	×	H	L	H
×	×	×	L	H	L
×	×	×	H	H	U

H = High level
L = Low level
× = Immaterial
* = Ratains data present before $\overline{E}$ positive transition
U = Undefined

■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		61	88	128	mA
Input Current	I_{IH}	V_{IN} = $V_{IH\ max}$	D_n input	—	—	350	μA
			CD_n, SD_n input	—	—	530	
			$\overline{E_n}$ input	—	—	240	
			$\overline{Ec}$, MR, MS input	—	—	450	

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100130

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	D_n input	0.45	1.20	0.50	0.85	1.20	0.50	1.35	ns
			CD_n, SD_n, E_n input	0.65	1.30	0.65	1.10	1.30	0.65	1.45	
			$\overline{E_C}$ input	0.75	1.15	0.75	1.15	1.45	0.75	1.50	
			MS, MR input	1.05	2.20	1.10	1.40	2.20	1.10	2.20	
Transition Time	t_{TLH}, t_{THL}			0.30	1.50	0.30	0.70	1.50	0.30	1.50	ns
Setup Time	t_{SU}		D_n	0.70	—	0.70	—	—	0.80	—	ns
			CD_n, SD_n (Release Time)	1.10	—	1.10	—	—	1.10	—	
			MR, MS (Release Time)	1.90	—	1.90	—	—	1.90	—	
Hold Time	t_h		D_n	0.00	—	0.00	—	—	0.00	—	ns
Pulse Width	$t_{W(L)}$		$\overline{E_n}$, $\overline{E_C}$	1.20	—	1.20	—	—	1.20	—	ns
	$t_{W(H)}$		CD_n, SD_n, MR, MS	1.35	—	1.35	—	—	1.35	—	

● HD100130F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	D_n input	0.50	1.15	0.50	0.95	1.15	0.50	1.25	ns
			CD_n, SD_n, E_n input	0.65	1.45	0.65	1.10	1.45	0.65	1.55	
			$\overline{E_C}$ input	0.75	1.55	0.75	1.20	1.55	0.75	1.55	
			MS, MR input	1.10	2.20	1.10	1.40	2.20	1.10	2.30	
Transition Time	t_{TLH}, t_{THL}			0.40	1.30	0.40	0.60	1.30	0.40	1.30	ns
Setup Time	t_{SU}		D_n	0.65	—	0.60	—	—	0.60	—	ns
			CD_n, SD_n (Release Time)	1.00	—	1.00	—	—	1.00	—	
			MR, MS (Release Time)	1.80	—	1.80	—	—	1.80	—	
Hold Time	t_h		D_n	0.20	—	0.20	—	—	0.20	—	ns
Pulse Width	$t_{W(L)}$		$\overline{E_n}$, $\overline{E_C}$	1.00	—	1.00	—	—	1.00	—	ns
	$t_{W(H)}$		CD_n, SD_n, MR, MS	1.15	—	1.15	—	—	1.15	—	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

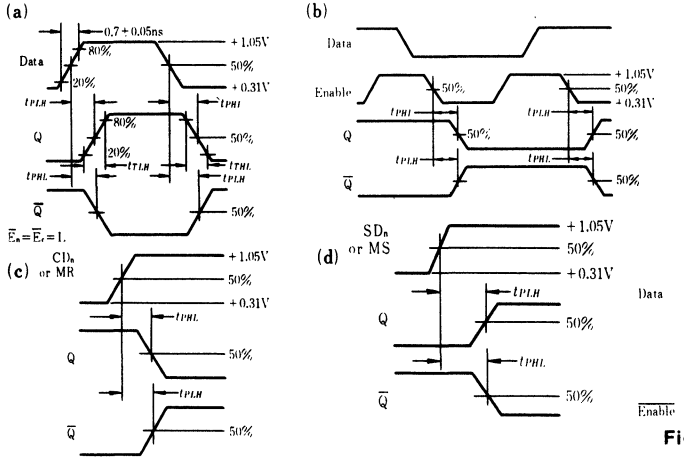


Fig.1 Propagation Delay Time

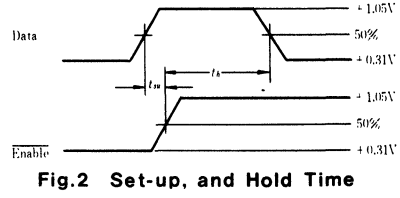


Fig.2 Set-up, and Hold Time

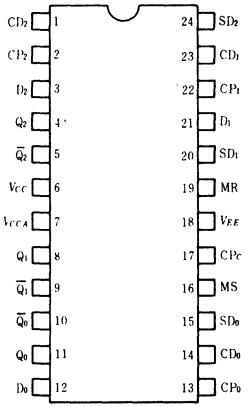
HD100131/F

Triple D-type Flip-Flops

The HD100131 contains three D-type Master Slave Flip Flops with true and complement outputs, a Common Clock (CPc), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual clocks (CPn), Direct Set (SDn) and Direct Clear (CDn) inputs. Data enters a master when both CPn and CPc are low and transfers to a slave when CPn or CPc (or both) go high.
The Master Set, Master Reset and individual CDn and SDn inputs override the Clock inputs.

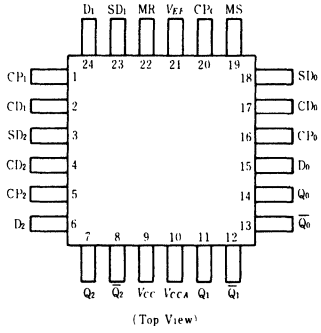
■PIN ARRANGEMENT

● HD100131



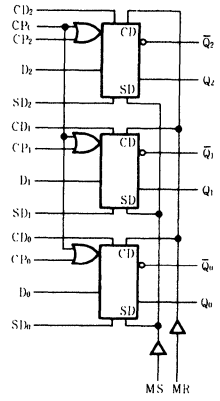
(Top View)

● HD100131F



(Top View)

■LOGIC DIAGRAM



■TRUTH TABLE

D_n	CP_n	CP_C	MS SD_n	MR CD_n	Q_{n+1}
L	↑	L	L	L	L
H	↑	L	L	L	H
L	L	↑	L	L	L
H	L	↑	L	L	H
×	H	×	L	L	Q_n
×	×	H	L	L	Q_n
×	×	×	H	L	H
×	×	×	L	H	L
×	×	×	H	H	U

H = High level
L = Low level
× = Immaterial
U = Undefined
↑ = Clock transition from low level to high level

■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		74	106	149	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$	CP_n, D_n input	—	—	240	μA
			MS, MR, CP_C input	—	—	450	
			CD_n, SD_n input	—	—	530	

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100131

Item	Symbol	Test Condition		0℃ min	0℃ max	25℃ min	25℃ typ	25℃ max	85℃ min	85℃ max	Unit
Toggle Frepuency	f_{Tog}			325	—	325	—	—	325	—	MHz
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	CP_C input	0.70	1.70	0.75	1.00	1.70	0.75	1.70	ns
			CD_n, SD_n input (CP=H)	0.75	1.70	0.80	1.10	1.70	0.80	1.70	
			CD_n, SD_n input (CP=L)	0.65	1.60	0.70	1.10	1.60	0.70	1.70	
			CP_n input	0.65	1.60	0.70	1.10	1.60	0.70	1.60	
			MS, MR input (CP=H)	1.00	2.85	1.05	1.50	2.85	1.05	2.85	
			MS, MR input (CP=L)	1.00	2.55	1.10	1.45	2.55	1.10	2.55	
Transition Time	t_{TLH}, t_{THL}			0.35	1.50	0.35	0.90	1.50	0.35	1.50	ns
Setup Time	t_{SU}		D_n input	0.70	—	0.70	—	—	0.90	—	ns
			CD_n, SD_n input (Release Time)	1.30	—	1.30	—	—	1.40	—	
			MS, MR input (Release Time)	2.20	—	2.20	—	—	2.20	—	
Hold Time	t_h		D_n input	0.20	—	0.20	—	—	0.20	—	ns
Pulse Width	$t_{W(H)}$		CD_n, SD_n, MR, MS	1.35	—	1.35	—	—	1.35	—	ns
	$t_{W(L)}$		CP_n, CP_C	0.95	—	0.95	—	—	0.95	—	

● HD100131F

Item	Symbol	Test Condition		0℃ min	0℃ max	25℃ min	25℃ typ	25℃ max	85℃ min	85℃ max	Unit
Toggle Frequency	f_{Tog}			325	—	325	—	—	325	—	MHz
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	CP_C input	0.70	1.65	0.75	1.05	1.65	0.75	1.65	ns
			CD_n, SD_n input (CP=H)	0.85	1.50	1.00	1.25	1.50	1.00	1.65	
			CD_n, SD_n input (CP=L)	0.50	1.50	0.60	0.90	1.50	0.60	1.50	
			CP_n input	0.70	1.50	0.70	1.00	1.50	0.70	1.50	
			MS, MR input (CP=H)	1.00	2.75	1.05	1.50	2.75	1.00	2.75	
			MS, MR input (CP=L)	1.00	2.40	1.10	1.30	2.40	1.10	2.40	
Transition Time	t_{TLH}, t_{THL}			0.35	1.30	0.35	0.65	1.30	0.35	1.30	ns
Setup Time	t_{SU}		D_n input	0.60	—	0.60	—	—	0.70	—	ns
			CD_n, SD_n input (Release Time)	1.20	—	1.20	—	—	1.25	—	
			MS, MR input (Release Time)	2.00	—	2.00	—	—	2.00	—	
Hold Time	t_h		D_n input	0.05	—	0.00	—	—	0.00	—	ns
Pulse Widtt	$t_{W(H)}$		CD_n, SD_n, MR, MS	1.15	—	1.15	—	—	1.15	—	ns
	$t_{W(L)}$		CP_n, CP_C	0.75	—	0.75	—	—	0.75	—	

Note) The circuits in a test socket or mounted on a printed circuit board and transerse air flow greater than 2.5m/s (500 linear fpm) is maintained.

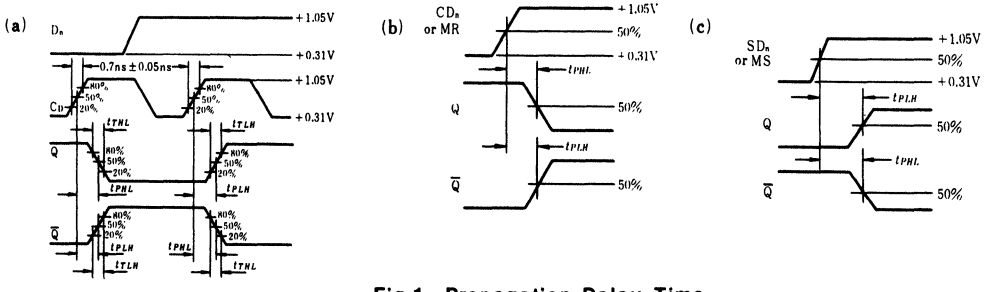


Fig.1 Propagation Delay Time

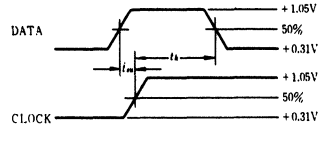


Fig.2 Set-up, and Hold Time

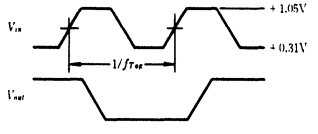


Fig.3 Toggle Frequency

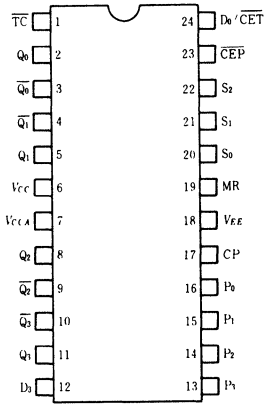
4-stage Counter /Shift Register

The HD100136 operates as either a modulo-16 up/down counter or as a 4-bit bidirectional shift register. Three Select (Sn) inputs determine the mode of operation, as shown in the mode select table. Two Count Enable ($\overline{CEP}$, $\overline{CET}$) inputs are provided for ease of cascading in multi-stage counters. One Count Enable ($\overline{CET}$) input also doubles as a Serial Data (Do) input for shift-up operation.

For shift-down operation D_3 is the Serial Data input. In counting operation the Terminal Count ($\overline{TC}$) output goes low when the counter reaches 15 in the count/up mode or 0 in the count/down mode. In the shift modes, the $\overline{TC}$ output repeats the Q_3 output. The dual nature of this $\overline{TC}/Q_3$ output and the Do/$\overline{CET}$ input means that one interconnection from one stage to the next higher stage serves as the link for multi-stage counting or shift-up operation. The individual Preset (Pn) inputs are used to enter data in parallel or to preset the counter in programmable counter applications. A high signal on the Master Reset (MR) input overrides all other inputs and asynchronously clears the flip-flops. In addition, asynchronous clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops.

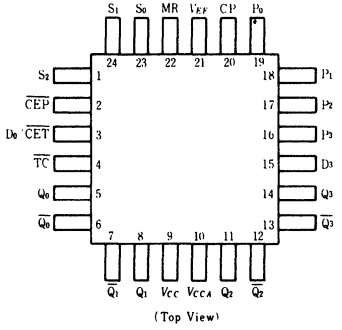
■ PIN ARRANGEMENT

● **HD100136**



(Top View)

● **HD100136F**



(Top View)

■ FUNCTION SELECT TABLE

S_0	S_1	S_2	Function
L	L	L	Load
L	H	L	Shift down
H	H	L	Shift up
L	L	H	Count down
L	H	H	Count up
H	H	H	Hold
H	L	L	Complement
H	L	H	Clear

H = High level
L = Low level

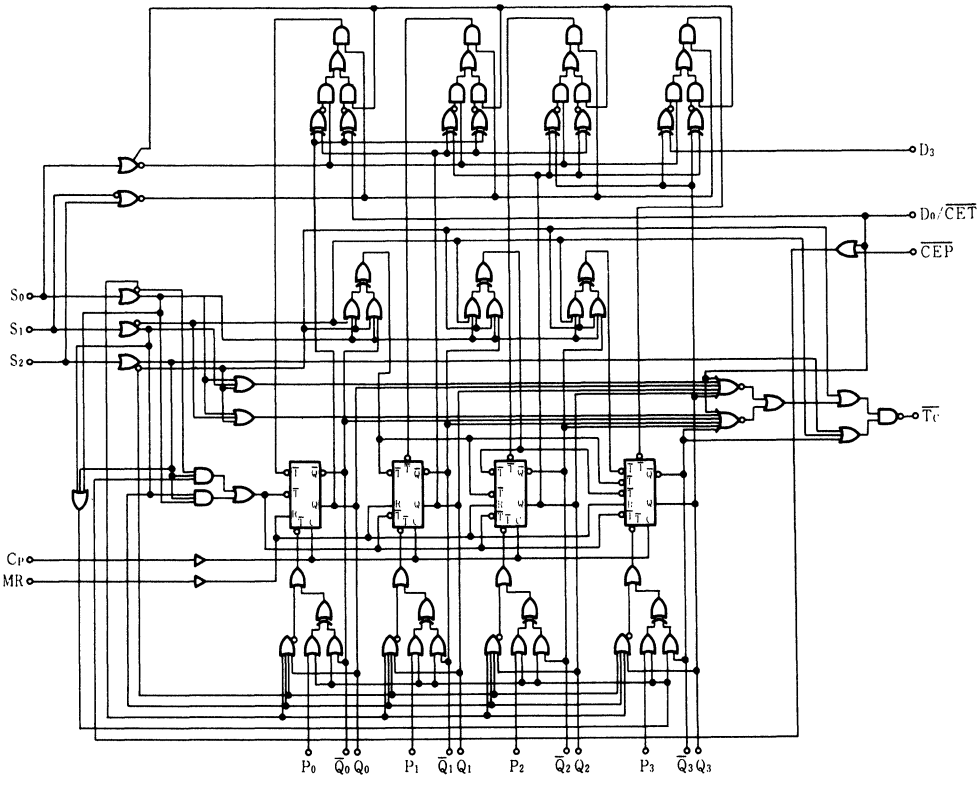
■TRUTH TABLE

Inputs								Outputs					
MR	S_0	S_1	S_2	$\overline{CEP}$	$D_0/\overline{CET}$	D_3	CP	Q_0	Q_1	Q_2	Q_3	$\overline{TC}$	Mode
L	L	L	L	X	X	X	⎍	P_0	P_1	P_2	P_3	L	Preset (Parallel Load)
L	L	L	H	L	L	X	⎍	(Q_{0-3}) minus 1				①	Count Down
L	L	L	H	H	L	X	X	Q_0	Q_1	Q_2	Q_3	①	Count Down with $\overline{CEP}$ not active
L	L	L	H	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Down with $\overline{CET}$ not active
L	L	H	L	X	X	X	⎍	Q_1	Q_2	Q_3	D_3	D_3	Shift Left
L	L	H	H	L	L	X	⎍	(Q_{0-3}) plus 1				②	Count Up
L	L	H	H	H	L	X	X	Q_0	Q_1	Q_2	Q_3	②	Count Up with $\overline{CEP}$ not active
L	L	H	H	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Up with $\overline{CET}$ not active
L	H	L	L	X	X	X	⎍	$\overline{Q_0}$	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	L	Invert
L	H	L	H	X	X	X	⎍	L	L	L	L	H	Clear
L	H	H	L	X	X	X	⎍	D_0	Q_0	Q_1	Q_2	Q_3	Shift Right
L	H	H	H	X	X	X	X	Q_0	Q_1	Q_2	Q_3	H	Hold
H	L	L	L	X	X	X	X	L	L	L	L	L	
H	L	L	H	X	L	X	X	L	L	L	L	L	
H	L	L	H	X	H	X	X	L	L	L	L	H	
H	L	H	L	X	X	X	X	L	L	L	L	L	
H	L	H	H	X	X	X	X	L	L	L	L	H	Asynchronous Master Reset
H	H	L	L	X	X	X	X	L	L	L	L	L	
H	H	L	H	X	X	X	X	L	L	L	L	H	
H	H	H	L	X	X	X	X	L	L	L	L	L	
H	H	H	H	X	X	X	X	L	L	L	L	H	

①=Lif Q_0-Q_3=LLLL Hif Q_0-Q_3≠LLLL ②=Lif Q_0-Q_3=HHHH Hif Q_0-Q_3≠HHHH

H=HIGH Voltage Level L=Low Voltage Level X=Don't Care ⎍=Low-to-HIGH Transition

■LOGIC DIAGRAM



■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		136	195	283	mA
Input Current	I_{IH}	V_{IN} = $V_{IH\ max}$	P_n, S_n input	—	—	180	μA
			$\overline{CEP}$ input	—	—	200	
			MR input	—	—	240	
			D_3 input	—	—	280	
			CP input	—	—	390	
			$D_0/\overline{CEP}$ input	—	—	530	

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100136

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Toggle Frequency	f_{Tog}			300	—	300	—	—	300	—	MHz
Propagation Delay Time	t_{PLH}, t_{PHL}	See tes circuit and waveform	CP→Q	0.80	2.10	0.90	1.25	2.10	0.90	2.10	ns
			CP→$\overline{TC}$	1.60	4.50	1.70	3.10	4.50	1.70	4.50	
			MR→Q	1.30	2.65	1.35	1.85	2.65	1.35	2.65	
			MR→$\overline{TC}$	2.30	4.80	2.40	3.50	4.80	2.40	4.80	
			D_0/CET→$\overline{TC}$	1.40	2.80	1.50	1.90	2.80	1.50	2.80	
			S_n→$\overline{TC}$	1.20	3.30	1.30	2.25	3.30	1.30	3.30	
Transition Time	t_{TLH}, t_{THL}			0.40	1.70	0.40	0.95	1.70	0.40	1.70	ns
Setup Time	t_{SU}		D_n	1.10	—	1.20	—	—	1.20	—	ns
			P_n	1.50	—	1.60	—	—	1.60	—	
			D_0/CET, $\overline{CEP}$	1.35	—	1.45	—	—	1.45	—	
			S_n	3.10	—	3.20	—	—	3.20	—	
			MR (Release Time)	2.50	—	2.60	—	—	2.60	—	
Hold Time	t_h		D_n	−0.10	—	−0.10	—	—	−0.20	—	ns
			P_n	−0.25	—	−0.25	—	—	−0.35	—	
			D_0/CET, $\overline{CEP}$	−0.15	—	−0.15	—	—	−0.25	—	
			S_n	−0.85	—	−0.85	—	—	−0.95	—	
Pulse Width	t_W		CP (H)	2.00	—	2.00	—	—	2.00	—	ns
			MR (H)	2.00	—	2.00	—	—	2.00	—	

● HD100136F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Toggle Frequency	f_{Tog}			300	—	300	—	—	300	—	MHz
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	CP→Q	0.90	1.90	0.95	1.25	1.90	0.95	1.90	ns
			CP→$\overline{TC}$	1.75	4.35	1.75	3.10	4.35	1.75	4.50	
			MR→Q	1.30	2.65	1.40	2.00	2.65	1.40	2.65	
			MR→$\overline{TC}$	2.20	4.60	2.20	3.50	4.60	2.20	5.20	
			D_0/CET→$\overline{TC}$	1.30	3.00	1.40	1.70	3.00	1.40	3.30	
			S_n→$\overline{TC}$	1.20	3.60	1.20	2.25	3.60	1.20	4.10	
Transition Time	t_{TLH}, t_{THL}			0.40	1.70	0.40	0.80	1.70	0.50	1.70	ns
Setup Time	$t_{S\ U}$		D_n	0.90	—	0.90	—	—	1.00	—	ns
			P_n	1.50	—	1.50	—	—	1.60	—	
			D_0/CET, $\overline{CEP}$	1.50	—	1.50	—	—	1.60	—	
			S_n	3.20	—	3.20	—	—	3.50	—	
			MR (Release Time)	2.50	—	2.50	—	—	2.50	—	
Hold Time	t_h		D_n	−0.10	—	−0.20	—	—	−0.20	—	ns
			P_n	−0.40	—	−0.45	—	—	−0.45	—	
			D_0/CET, $\overline{CEP}$	−0.05	—	−0.10	—	—	−0.10	—	
			S_n	−0.85	—	−0.85	—	—	−0.85	—	
Pulse Width	t_W		CP (H)	2.00	—	2.00	—	—	2.00	—	ns
			MR (H)	2.00	—	2.00	—	—	2.00	—	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

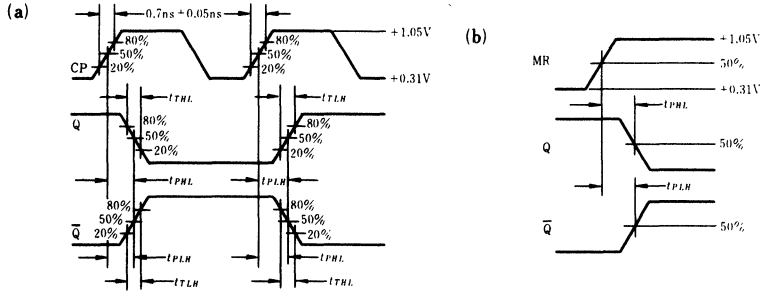


Fig.1 Propagation Delay Time

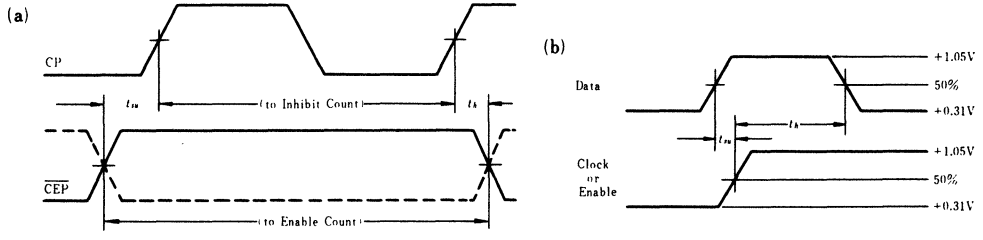


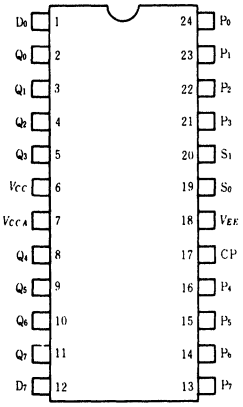
Fig.2 Set-up and Hold Time

8-bit Shift Register

The HD100141 contains eight clocked D-type flip flops with individual inputs (Pn) and outputs (Qn) for parallel operation, and with serial inputs (Dn) and steering logic for bidirectional shifting.
The flip flops accept input data a set-up time before the positive-going transition of the clock pulse and their outputs respond a propagation delay after this rising clock edge.
The circuit operating mode is determined by the Select inputs S_0 and S_1, which are internally decoded to select either "parallel entry", "hold", "shift left" or "shift right" as described in the Function Sheet Table.

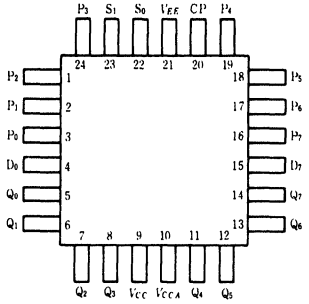
■ PIN ARRANGEMENT

● HD100141



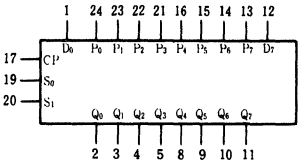
(Top View)

● HD100141F

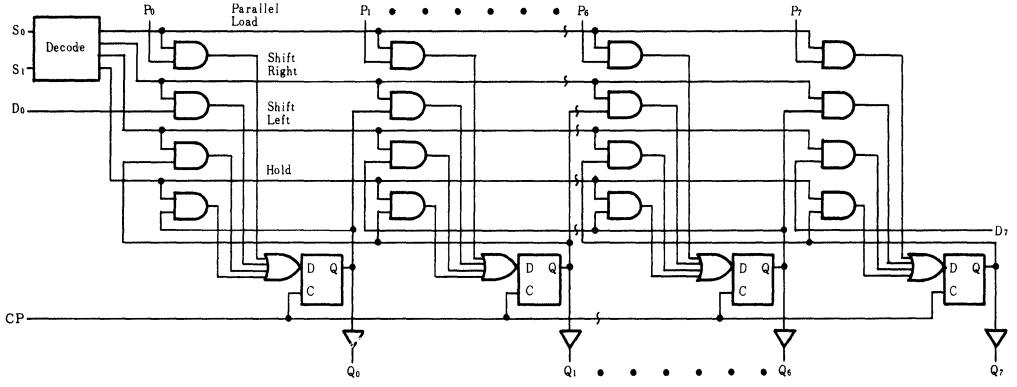


(Top View)

■ LOGIC SYMBOL



■ LOGIC DIAGRAM



■FUNCTION SHEET TABLE

Function	Input					Output							
	D_7	D_0	S_1	S_0	CP	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
Load Register	X	X	L	L	↑	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
Shift Left	X	L	L	H	↑	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	L
Shift Left	X	H	L	H	↑	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	H
Shift Right	L	X	H	L	↑	L	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Shift Right	H	X	H	L	↑	H	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Hold	X	X	H	H	X	← No Change →							
Hold	X	X	X	X	H	← No Change →							
Hold	X	X	X	X	L	← No Change →							

H = High Level
L = Low Level
X = Don't Care
↑ = Low to High transition

■DC CHARACTERISTICS (V_{EE} = −4.2 to +4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		119	170	238	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$	CP input	—	—	640	μA
			Other input	—	—	220	

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

●HD100141

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Shift Frequency	f_{shift}			380	—	380	—	—	380	—	MHz
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform		1.00	2.20	1.10	1.40	2.20	1.10	2.20	ns
Transition Time	t_{TLH}, t_{THL}			0.35	1.30	0.35	0.90	1.30	0.35	1.30	ns
Setup Time	t_{SU}		Serial-in, Parallel-in	0.85	—	0.85	—	—	0.85	—	ns
			Select input	2.00	—	2.00	—	—	2.00	—	
Hold Time	t_h		Serial-in, Parallel-in	0.20	—	0.20	—	—	0.40	—	ns
			Select-input	−0.20	—	−0.20	—	—	−0.20	—	
Pulse Width	t_W		CP (H)	2.00	—	2.00	—	—	2.00	—	ns

● HD100141F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Shift Frequency	f_{shift}			380	—	380	—	—	380	—	MHz
Propagation Delay Time	t_{PLH}, t_{PNL}	See test circuit anb Weveform		1.00	2.10	1.10	1.50	2.10	1.10	2.10	ns
Transition Time	t_{TLH}, t_{THL}			0.40	1.20	0.40	0.70	1.20	0.45	1.20	ns
Setup Time	t_{SU}		Serial-in, Parallel-in	0.75	—	0.75	—	—	0.75	—	ns
			Select input	1.80	—	1.80	—	—	1.80	—	
Hold Time	t_h		Serial-in, Parallel-in	0.20	—	0.20	—	—	0.20	—	ns
			Select input	−0.80	—	−0.80	—	—	−0.80	—	
Pulse Width	t_W		CP (H)	2.00	—	2.00	—	—	2.00	—	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

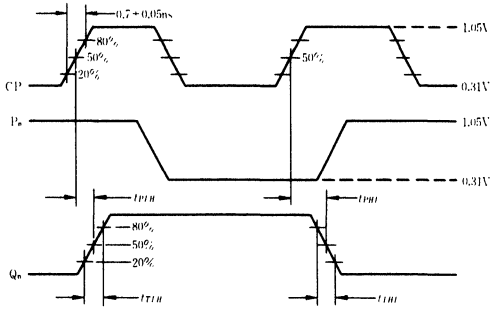


Fig.1 Propagation Delay Time

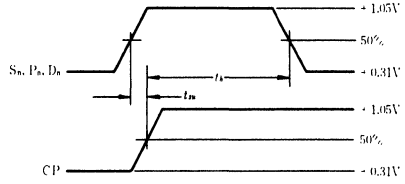


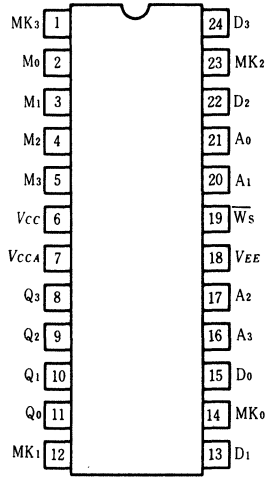
Fig.2 Set-up and Hold Time

4×4 Content Addressable Memory

The HD100142 is a 4 word x 4 bit Content Addressable Memory (CAM). Each word location has its own Address Select line. Reading or Writing is accomplished when the Address Select line is low. In the Read mode, Data from the addressed location appears at the Data (Qi) outputs.
In the Write mode, Data is stored in the addressed location. A low Write Strobe selects the Write mode, a high Write Strobe select the Read mode. Each Data input has its own Mask input that blocks data storage when the Mask is high. The Data input word is simultaneously compared with each of the four memory Words.
If a Search Compare result in a Match, this output will go low. A high Mask input on any bit forces a Match of that bit. Each input has a 50kΩ (typical) pull-down resistor tied to V_{EE}. The outputs require external resistance terminations as they are not terminated internally through resistance to the V_{EE} supply.

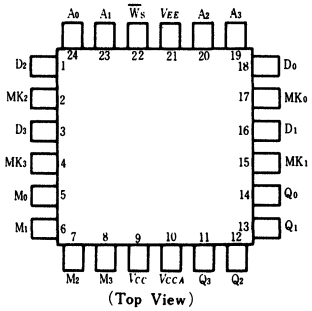
■ PIN ARRANGEMENT

● **HD100142**



(Top View)

● **HD100142F**



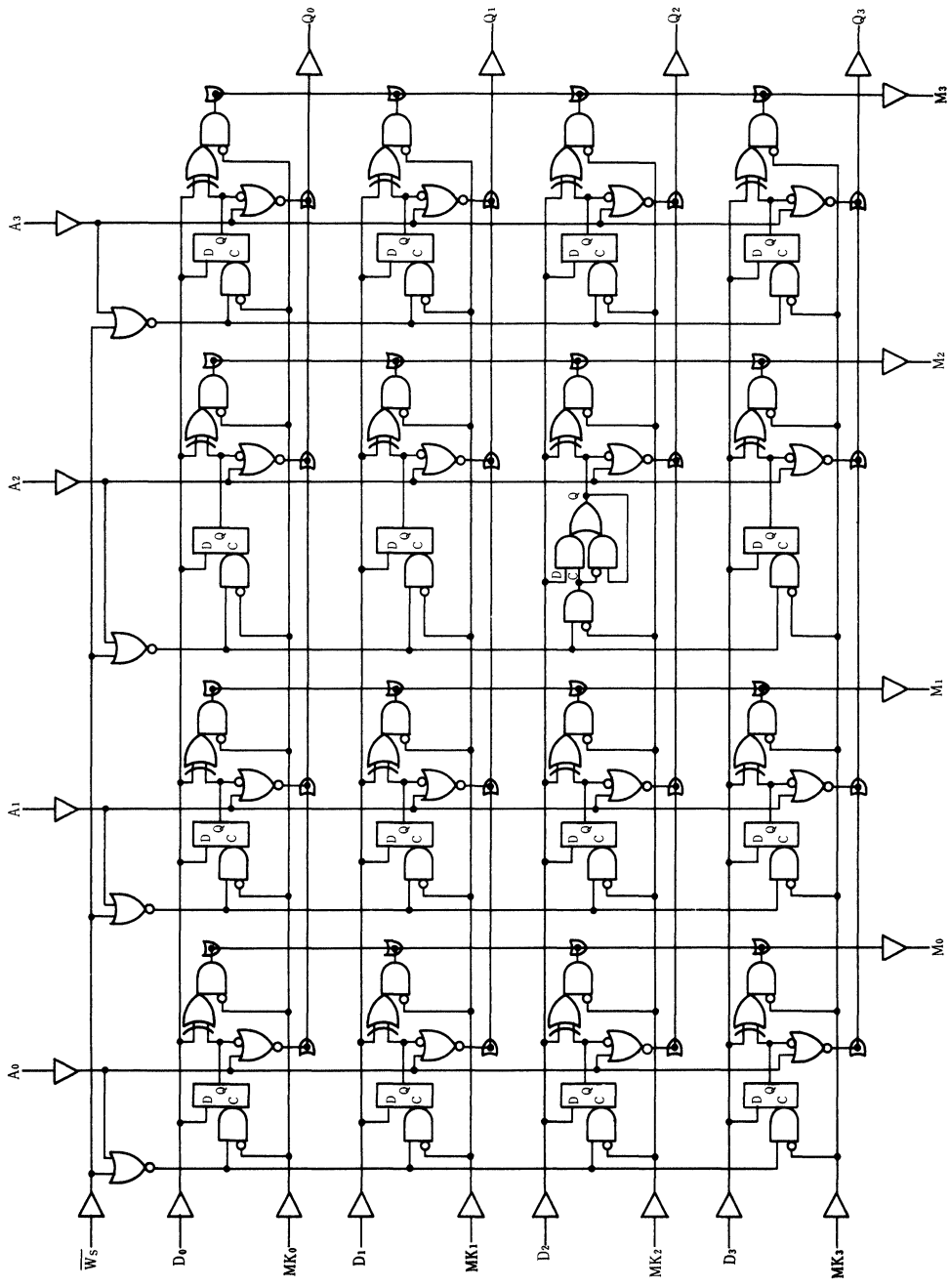
(Top View)

■ TRUTH TABLE

Operation	Inputs				Flip-Flop	Outputs	
	$\overline{WS}$	A_i	D_i	MK_j	Q_{ij}	M_i	Q_j
	$\overline{WS}$	A_0	D_0	MK_0		M_0	Q_0
		A_1	D_1	MK_1		M_1	Q_1
		A_2	D_2	MK_2		M_2	Q_2
		A_3	D_3	MK_3		M_3	Q_3
	×	H	×	×	NC	×	L
Write Disabled	×	L	×	H	NC	L	Q_{ijn-1}
	H	L	×	×	NC	×	Q_{ijn-1}
	L	L	H	L	H	L	H
Write	L	L	L	L	L	L	L
	H	L	×	×	H	×	H
Read	H	L	×	×	L	×	L
Match Masked	H	×	×	H	NC	L	×
	H	L	H	L	L	H	L
Match Not Satisfied	H	H	H	L	L	H	L
	H	H	L	L	H	H	L
	H	L	L	L	H	H	H
	H	L	H	L	H	L	H
Match Satisfied	H	H	H	L	H	L	L
	H	H	L	L	L	L	L
	H	L	L	L	L	L	L

H = High Voltage Level (Most Positive)
L = Low Voltage Level (Most Negative)
× = Don't Care (May be either high or low)
NC = No Change from Previous State
$\overline{WS}$ = Write Strobe
Ai = Address for ith Word
Dj = Data for jth Bit
MKj = Data mask for jth Bit (H = Mask)
Qij = Cell State for ith Word, jth Bit
Mi = Match Output of ith Word (L = True)
Qj = Data Output of jth Bit
Q_{n+1} = Previous Cell State

■ LOGIC DIAGRAM



■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		114	163	288	mA
Input Current	I_{IH}	V_{IN} = $V_{IH\ max}$	$\overline{WS}$, Aj input	—	—	159	μA
			D_n input	—	—	149	
			MK_n input	—	—	164	

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

●HD100142

Item	Symbol	Test Condition	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Address to Data Out	t_{AD}	See test circuit and waveform	1.20	2.90	1.30	1.90	2.90	1.30	3.00	ns
Data In to Match Out Time	t_{DM}		1.45	3.55	1.60	2.45	3.55	1.60	3.55	
Mask In to "Enable Partial" Match Out Time	t_{MM}		1.25	2.85	1.25	1.95	2.85	1.25	3.00	
Data In to New Data Out	t_{DD}		1.90	4.40	1.90	3.00	4.40	1.90	4.50	
Write to New Data Out	t_{WD}		2.40	4.60	2.50	3.00	4.60	2.50	4.60	
Address to Match	t_{AM}		2.50	4.60	2.50	3.30	4.60	2.50	4.60	
Mask to Data	t_{MD}		2.10	4.45	2.20	2.90	4.45	2.20	4.45	
$\overline{WS}$ to Match	t_{WSM}		2.70	4.60	2.80	3.30	4.60	2.80	4.60	
Write Pulse Width	t_W		1.30	—	1.30	—	—	1.30	—	
Address Setup before Write Time	t_{AS}		0.20	—	0.20	—	—	0.20	—	
Address Hold after Write Time	t_{AH}		0.20	—	0.20	—	—	0.20	—	
Data In Setup before Write Time	t_{DS}		−0.60	—	−0.60	—	—	−0.60	—	
Data In Hold after Write Time	t_{DH}		0.70	—	0.70	—	—	0.70	—	
Mask In Hold to inhibit Write Time	t_{MH}		1.30	—	1.30	—	—	1.30	—	
Mask In Setup to inhibit Write Time	t_{MS}		−0.20	—	−0.20	—	—	−0.20	—	
Transition Time	t_{TLH}, t_{THL}		0.40	2.00	0.40	1.30	2.00	0.45	2.00	

●HD100142F

Item	Symbol	Test Condition	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Address to Data Out	t_{AD}	See test circuit and waveform	1.20	2.70	1.20	1.90	2.70	1.30	2.70	ns
Data In to Match Out Time	t_{DM}		1.45	3.35	1.55	2.45	3.35	1.55	3.35	
Mask In to "Enable Partial" Match Out Time	t_{MM}		1.20	2.65	1.25	1.95	2.65	1.25	2.70	
Data In to New Data Out	t_{DD}		1.90	4.20	1.90	3.00	4.20	1.90	4.20	
Write to New Data Out	t_{WD}		2.40	4.40	2.50	3.00	4.40	2.50	4.40	
Address to Match	t_{AM}		2.50	4.40	2.50	3.10	4.40	2.50	4.40	
Mask to Data	t_{MD}		2.10	4.15	2.20	2.90	4.25	2.20	4.25	
$\overline{WS}$ to Match	t_{WSM}		2.70	4.30	2.80	3.30	4.40	2.80	4.40	
Write Pulse Width	t_W		1.20	—	1.20	—	—	1.20	—	
Address Setup before Write Time	t_{AS}		0.00	—	0.00	—	—	0.00	—	
Address Hold after Write Time	t_{AH}		0.00	—	0.00	—	—	0.00	—	
Data In Setup before Write Time	t_{DS}		−0.60	—	−0.60	—	—	−0.60	—	
Data In Hold after Write Time	t_{DH}		0.50	—	0.50	—	—	0.50	—	
Mask In Hold to inhibit Write Time	t_{MH}		1.00	—	1.10	—	—	1.10	—	
Mask In Setup to inhibit Write Time	t_{MS}		−0.30	—	−0.30	—	—	−0.30	—	
Transition Time	t_{TLH}, t_{THL}		0.40	2.00	0.40	1.10	2.00	0.40	2.00	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

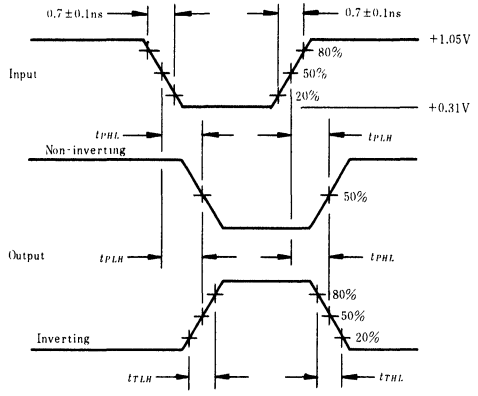


Fig. 1 Output Rise and Fall Times and Waveforms

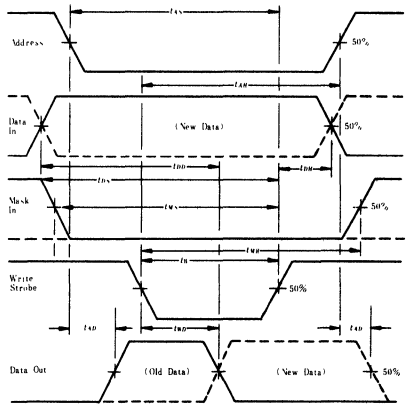


Fig. 2 Write Mode and Read/Write Mode Waveforms

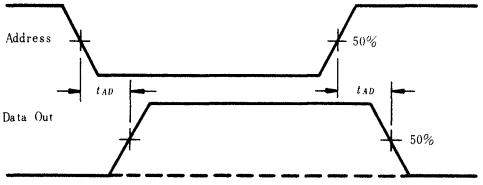


Fig. 3 Read Mode Waveforms

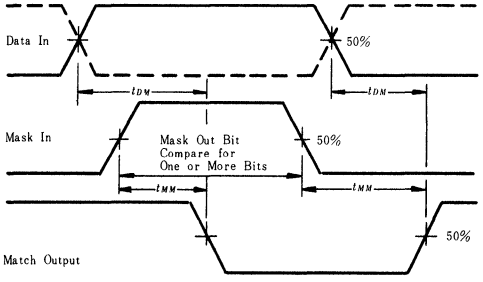


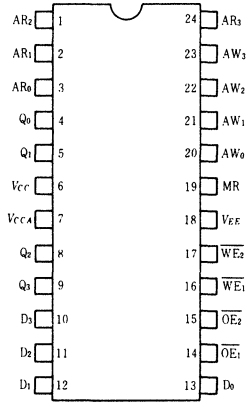
Fig. 4 Search Mode Waveforms

16×4 Read/Write Register File

The HD100145 is a 64-bit Register File organized as 16 words of four bits each. Separate address inputs for Read (AR_n) and Write (AW_n) operations reduce overall cycle time by allowing one address to be setting-up while the other is being executed. Operating speed is also enhanced by four output latches which store data from the previous read operation while writing is in progress. When both Write Enable ($\overline{WE}$) inputs are LOW, the circuit is in the WRITE mode and the latches are in a HOLD mode. When either $\overline{WE}$ input is HIGH, the circuit is in the READ mode, but the outputs can be forced LOW by a HIGH signal on either of the Output Enable ($\overline{OE}$) inputs. This makes it possible to tie one $\overline{WE}$ input and one $\overline{OE}$ input together to serve as an active LOW Chip Select ($\overline{CS}$) input. When this wired $\overline{CS}$ input is HIGH, reading will still take place internally and the resulting data will enter the latches and become available as soon as the $\overline{CS}$ signal goes LOW, provided that the other $\overline{OE}$ input is LOW. A HIGH signal on the Master Reset (MR) input overrides all other inputs, clears all cells in the memory, resets the output latches and forces the outputs LOW.

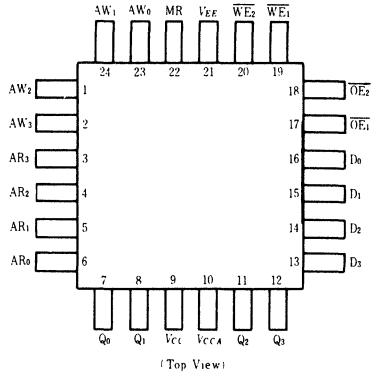
■ PIN ARRANGEMENT

●HD100145



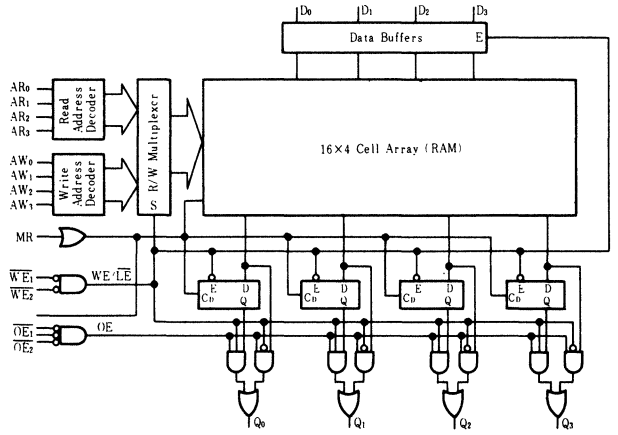
(Top View)

●HD100145F



(Top View)

■ LOGIC DIAGRAM



■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		119	170	247	mA
Input Current	I_{IH}	V_{IN} = $V_{IH\ max}$	WE/$\overline{\text{LE}}$ input	—	—	270	μA
			All input except WE/$\overline{\text{LE}}$	—	—	220	μA

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100145

Item		Symbol	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Access/Recovery Timing	Address Access	t_{AA}	2.00	7.40	2.00	5.50	7.40	2.00	7.40	ns
	Output Recovery	t_{OR}	0.80	3.10	0.80	2.20	3.10	0.80	3.30	
	Output Disable	t_{OD}	0.80	3.10	0.80	2.20	3.10	0.80	3.30	
Read Timing	Address Setup	t_{RSA1}	3.20	—	3.20	2.00	—	3.20	—	
	Output Delay	t_{WEQ}	2.00	6.10	2.00	4.50	6.10	2.00	6.60	
Outpul Latch Timing	Address Setup	t_{RSA2}	8.50	—	8.50	5.50	—	8.50	—	
	Address Hold	t_{RHA}	0.20	—	0.20	−2.00	—	0.20	—	
Write Timing	Address Setup	t_{WSA}	3.20	—	3.20	2.00	—	3.20	—	
	Address Hold	t_{WHA}	0.20	—	0.20	−1.30	—	0.20	—	
	Data Setup	t_{WSD}	9.20	—	9.20	6.00	—	9.20	—	
	Data Hold	t_{WHD}	0.20	—	0.20	−1.20	—	0.20	—	
	Min. Write Pulse Width	t_W	6.20	—	6.20	4.00	—	6.20	—	
	$\overline{\text{WE}}$ to $\overline{\text{WE}}$ Setup	t_{SW}	0.70	—	0.70	—	—	0.70	—	
	$\overline{\text{WE}}$ to $\overline{\text{WE}}$ Hold	t_{HW}	0.20	—	0.20	—	—	0.20	—	
Master Reset Timing	Min. Reset Pulse Width	t_M	4.50	—	4.50	—	—	4.50	—	
	$\overline{\text{WE}}$ Hold to Write	t_{MHW}	9.20	—	9.20	—	—	10.60	—	
	Output Disable	t_{MQ}	3.70	—	3.70	2.70	—	3.70	—	

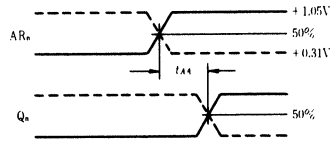
● HD100145F

Item		Symbol	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Access/Recovery Timing	Address Access	t_{AA}	2.00	7.20	2.00	5.50	7.20	2.00	7.20	ns
	Output Recovery	t_{OR}	1.00	2.90	1.00	2.20	2.90	1.00	3.20	
	Output Disable	t_{OD}	1.00	2.90	1.00	2.20	2.90	1.00	3.20	
Read Timing	Address Setup	t_{RSA1}	3.00	—	3.00	2.00	—	3.00	—	
	Output Delay	t_{WEQ}	2.00	5.90	2.00	4.50	5.90	2.00	6.40	
Output Latch Timing	Address Setup	t_{RSA2}	8.30	—	8.30	5.50	—	8.30	—	
	Address Hold	t_{RHA}	0.00	—	0.00	−2.00	—	0.00	—	
Write Timing	Address Setup	t_{WSA}	3.00	—	3.00	2.00	—	3.00	—	
	Address Hold	t_{WHA}	0.00	—	0.00	−1.30	—	0.00	—	
	Data Setup	t_{WSD}	9.00	—	9.00	6.00	—	9.00	—	
	Data Hold	t_{WHD}	0.00	—	0.00	−1.20	—	0.00	—	
	Min. Write Pulse Width	t_W	6.00	—	6.00	4.00	—	6.50	—	
	$\overline{\text{WE}}$ to $\overline{\text{WE}}$ Setup	t_{SW}	0.50	—	0.50	—	—	0.50	—	
	$\overline{\text{WE}}$ to $\overline{\text{WE}}$ Hold	t_{HW}	0.00	—	0.00	—	—	0.00	—	
Master Reset Timing	Min. Reset Pulse Width	t_M	4.30	—	4.30	—	—	4.30	—	
	$\overline{\text{WE}}$ Hold to Write	t_{MHW}	9.00	—	9.00	—	—	10.40	—	
	Output Disable	t_{MQ}	3.50	—	3.50	—	—	3.50	—	

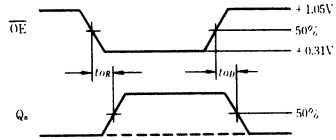
Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

■ TIMING RELATIONSHIPS

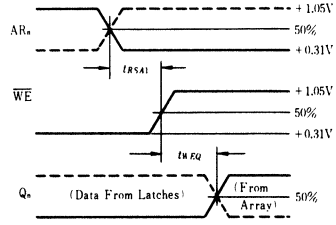
(a) Address Access Time
($\overline{WE}_1$, or $\overline{WE}_2$ = High : $\overline{OE}_1 = \overline{OE}_2$ = Low)



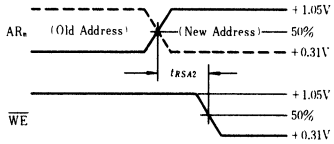
(b) Output Recovery/Disable Time
(unpulsed $\overline{OE}$ = Low)



(c) Read Timing, Address Set-up Time
(unpulsed $\overline{WE}$, $\overline{OE}_1$, $\overline{OE}_2$ = Low)



(d) Output Latch Timing, Address Set-up Time
(unpulsed $\overline{WE}$ = Low)



(e) Output Latch Timing, Address Hold Time
(unpulsed $\overline{WE}$ = Low)

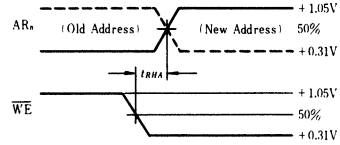
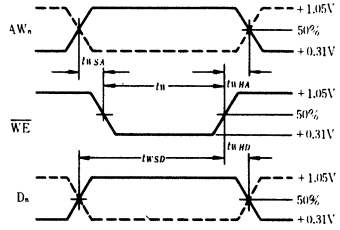


Fig.1 Read Timing

(a) Address and Data Set-up Time and Hold Time, Write Pulse Width (unpulsed $\overline{WE}$ = Low)



(b) $\overline{WE}$ Set-up and hold times, write with other $\overline{WE}$

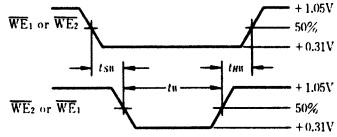
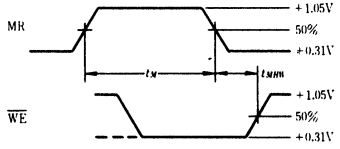


Fig.2 Write Timing

(a) Reset pulse width, $\overline{WE}$ hold time for subsequent writing (address already set-up, unpulsed $\overline{WE}$ = Low)



(b) Output reset delay, MR to Q_n

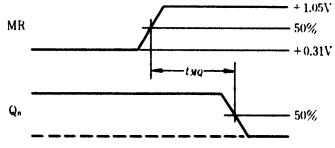


Fig.3 Master Reset Timing

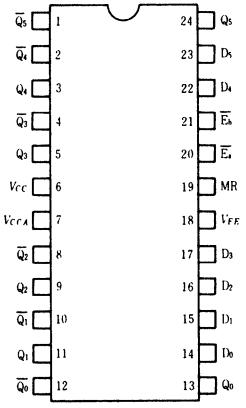
HD100150/F

Hex D-type Latches

The HD100150 contains six D type latches with the True and Complement Outputs, a pair of Common Enables ($\overline{Ea}$ and $\overline{Eb}$), and a common Master Reset(MR). A Q output follows its D input when both $\overline{Ea}$ and $\overline{Eb}$ are low. When either $\overline{Ea}$ or $\overline{Eb}$ (or both) are high, a latch stores the last valid data present on its D input before $\overline{Ea}$ or $\overline{Eb}$ went high. The MR input overrides all other inputs and makes the Q outputs low.

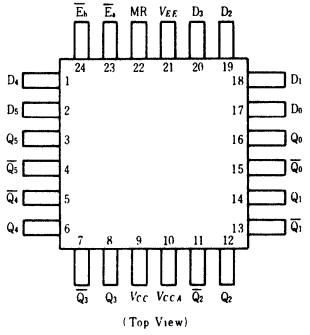
■ PIN ARRANGEMENT

● HD100150



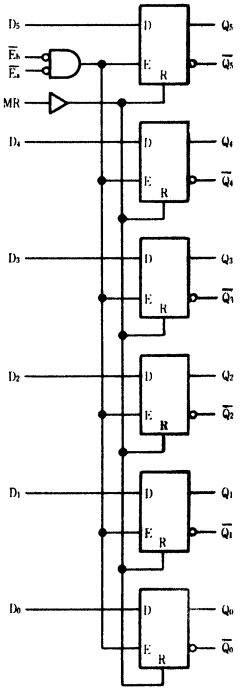
(Top View)

● HD100150F



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE (each latch)

Dn	$\overline{Ea}$	$\overline{Eb}$	MR	Q_n
L	L	L	L	L
H	L	L	L	H
×	H	×	L	*
×	×	H	L	*
×	×	×	H	L

H = High Level
L = Low Level
× = Immaterial
* = Retains data present before $\overline{E}$ positive transition

■ DC CHARACTERISTICS ($V_{EE}=-4.5V$, $V_{CC}=GND$, $Ta=0$ to $+85℃$)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		79	113	159	mA
Input Current	I_{IH}	$V_{IN}=V_{IL\ max}$	MR input	—	—	450	μA
			Data input	—	—	340	μA
			Enable input	—	—	520	μA

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100150

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	$\overline{E_a}$, $\overline{E_b}$ input	0.75	1.50	0.75	1.15	1.50	0.85	1.60	ns
			MR input	1.00	2.25	1.10	1.55	2.35	1.10	2.35	
			D_n input	0.50	1.35	0.55	0.60	1.40	0.55	1.40	
Transition Time	t_{TLH}, t_{THL}			0.35	1.50	0.35	0.70	1.50	0.35	1.50	ns
Setup Time	t_{SU}		D_n input	0.60	—	0.60	—	—	0.60	—	ns
			MR input (Release Time)	1.90	—	2.10	—	—	2.10	—	
Hold Time	t_h		D_n input	0.50	—	0.50	—	—	0.40	—	ns
Pulse Width	t_W		$\overline{E_a}$, $\overline{E_b}$ (L)	0.95	—	0.95	—	—	0.95	—	ns
			MR (H)	1.50	—	1.50	—	—	1.50	—	

● HD100150F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	$\overline{E_a}$, $\overline{E_b}$ input	0.70	1.45	0.75	1.05	1.50	0.75	1.50	ns
			MR input	1.10	2.10	1.15	1.50	2.20	1.15	2.20	
			D_n input	0.50	1.10	0.55	0.85	1.15	0.55	1.15	
Transition Time	t_{TLH}, t_{THL}			0.45	1.50	0.45	0.70	1.50	0.45	1.50	ns
Setup Time	t_{SU}		D_n input	0.60	—	0.60	—	—	0.60	—	ns
			MR input (Release Time)	1.80	—	2.00	—	—	2.00	—	
Hold Time	t_h		D_n input	0.30	—	0.30	—	—	0.20	—	ns
Pulse Width	t_W		$\overline{E_a}$, $\overline{E_b}$ (L)	0.75	—	0.75	—	—	0.75	—	ns
			MR (H)	1.30	—	1.30	—	—	1.30	—	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

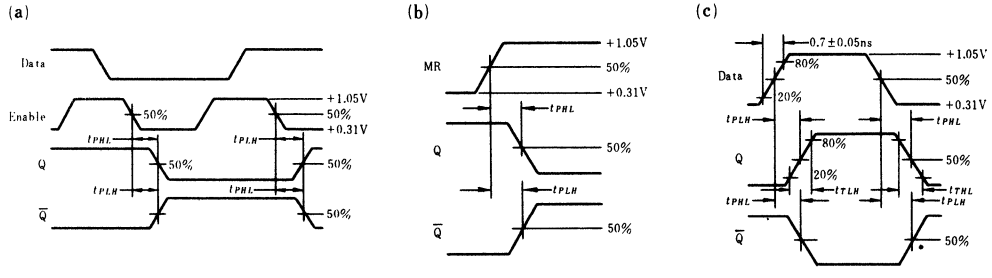


Fig.1 Propagation Delay Time

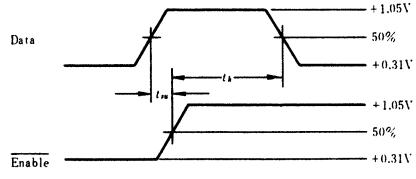


Fig.2 Set-up and Hold Time

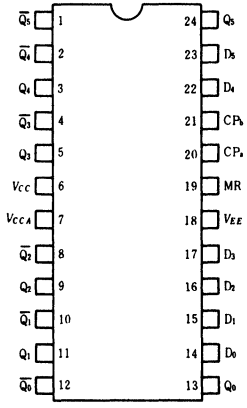
HD100151/F

Hex D-type Flip-Flops

HD100151 contains six master/slave fli-flops with True and Complement outputs. A pair of Common Clock inputs (CPa and CPb) and common Master Reset (MR) input. Data enters a master when both CPa and CPb are low and transfers to the slave when CPa or CPb (or both) go high. The MR inputs overrides all other inputs and makes the Q outputs low.

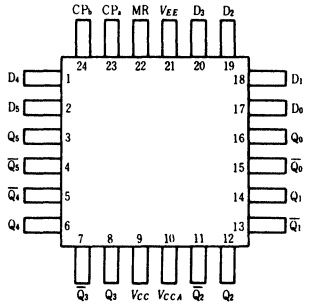
■ PIN ARRANGEMENT

● HD100151



(Top View)

● HD100151F



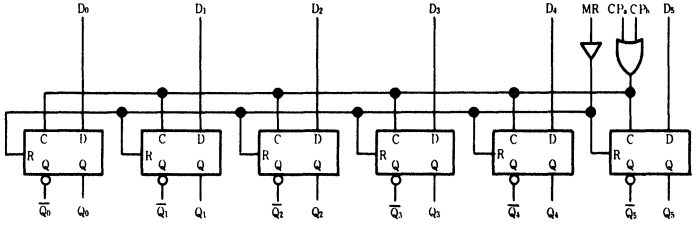
(Top View)

■ TRUTH TABLE (Each Flip Flop)

D_n	CP_a	CP_b	MR	$Q_{n(t+1)}$
L	⎍	L	L	L
H	⎍	L	L	H
L	L	⎍	L	L
H	L	⎍	L	H
×	H	⎍	L	$Q_{n(t)}$
×	⎍	H	L	$Q_{n(t)}$
×	×	×	H	L

×: Immaterial
t, t+1 : Time before and after CP positive transition

■ LOGIC DIAGAM



■ DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		98	141	198	mA
Input Current	I_{IH}	V_{IN} = $V_{IN\ max}$	MR input	—	—	450	μA
			D_0~D_5 input	—	—	225	μA
			CP_a, CP_b input	—	—	520	μA

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100151

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}		CP_a, CP_b input	0.70	1.70	0.80	1.30	1.80	0.90	1.90	ns
			MR input	1.30	2.50	1.30	1.65	2.60	1.30	2.60	
Transition Time	t_{TLH}, t_{THL}	See test circuit and waveform		0.35	1.20	0.35	0.65	1.20	0.35	1.20	
Toggle Frequency	f_{tog}			400	—	400	—	—	400	—	MHz
Setup Time	t_{SU}		D_n input	0.60	—	0.60	—	—	0.60	—	ns
			MR input (Release Time)	2.20	—	2.20	—	—	2.20	—	
Hold Time	t_h		D_n input	0.50	—	0.50	—	—	0.50	—	ns
Pulse Width	t_W		$\overline{E_a}$, $\overline{E_b}$ (L)	1.30	—	1.30	—	—	1.30	—	ns
			MR (H)	1.50	—	1.50	—	—	1.50	—	

● HD100151F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}		CP_a, CP_b input	0.80	1.70	0.90	1.20	1.80	0.90	1.80	ns
			MR input	1.35	2.50	1.35	1.60	2.50	1.35	2.60	
Transition Time	t_{TLH}, t_{THL}	See test circuit and waveform		0.35	1.20	0.35	0.60	1.20	0.35	1.20	
Toggle Frequency	f_{tog}			400	—	400	—	—	400	—	MHz
Setup Time	t_{SU}		D_n input	0.60	—	0.60	—	—	0.60	—	ns
			MR input (Release Time)	1.40	—	1.50	—	—	1.50	—	
Hold Time	t_h		D_n input	0.30	—	0.30	—	—	0.30	—	ns
Pulse Width	t_W		$\overline{E_a}$, $\overline{E_b}$ (L)	1.10	—	1.10	—	—	1.10	—	ns
			MR (H)	1.30	—	1.30	—	—	1.30	—	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

Quad. Multiplexers/Latches

The HD100155 contains four transparent latches, each of which can accept and store data from two sources. When both Enable ($\overline{En}$) inputs are low, the data that appears at an outputs is controlled by the Select (Sn) inputs, as shown in the operating mode table. In addition to routing data from either D_0 or D_1, the Select inputs can force the outputs low for the case where the latch is transparent (both Enables are low) and can steer a high signal from either D_0 or D_1 to an output. The Select inputs can be tied together for applications requiring only that data be steered from either D_0 or D_1.

A positive-going signal on either Enable input latches the outputs. A high signal on the Master Reset (MS) input overrides all the other inputs and forces the Q outputs low.

■ OPERATING MODE TABLE

CONTROLS				OUTPUT
$\overline{E_1}$	$\overline{E_2}$	$\overline{S_0}$	S_1	Q_n
H	×	×	×	latched*
×	H	×	×	latched*
L	L	L	L	D_{0n}
L	L	L	H	$D_{0n}+D_{1n}$
L	L	H	L	L
L	L	H	H	D_{1n}

H = High Level
L = Low Level
× = Immaterial
* = Stores data present before En went high.

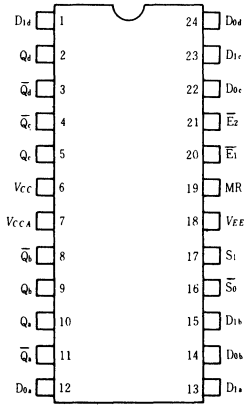
■ TRUTH TABLE

Input							Output	
MR	$\overline{E_1}$	$\overline{E_2}$	S_1	$\overline{S_0}$	D_{1a} D_{1b} D_{1c} D_{1d}	D_{0a} D_{0b} D_{0c} D_{0d}	$\overline{Q_a}$ $\overline{Q_b}$ $\overline{Q_c}$ $\overline{Q_d}$	Q_a Q_b Q_c Q_d
H	×	×	×	×	×	×	H	L
L	L	L	H	H	H	×	L	H
L	L	L	H	H	L	×	H	L
L	L	L	L	L	×	H	L	H
L	L	L	L	L	×	L	H	L
L	L	L	L	H	×	×	H	L
L	L	L	H	L	H	×	L	H
L	L	L	H	L	×	H	L	H
L	L	L	H	L	L	L	H	L
L	H	×	×	×	×	×	No Change	
L	×	H	×	×	×	×	No Change	

H = High Level
L = Low Level
× = Immaterial

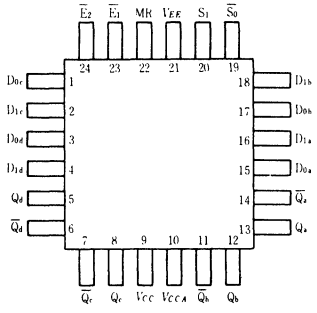
■ PIN ARRANGEMENT

● HD100155



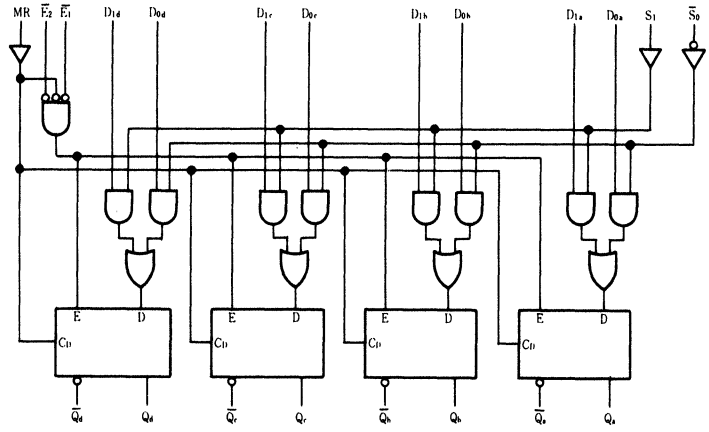
(Top View)

● HD100155F



(Top View)

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		60	95	133	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$	S_n input	—	—	220	μA
			$\overline{E_n}$ input	—	—	350	
			Data input	—	—	340	
			MR input	—	—	430	

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100155

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	Date input	0.55	1.50	0.60	1.00	1.55	0.60	1.55	ns
			S input	1.40	3.00	1.50	1.80	3.10	1.50	3.10	
			$\overline{E}$ input	0.90	1.90	1.00	1.40	2.00	1.00	2.00	
			MR input	0.95	1.65	1.00	1.70	2.50	1.00	2.50	
Transition Time	t_{TLH}, t_{THL}			0.55	1.75	0.50	1.10	1.65	0.50	1.65	ns
Setup Time	t_{SU}		Data input	0.60	—	0.60	—	—	0.60	—	ns
			S input	2.30	—	2.30	—	—	2.30	—	
			MR input (Release Time)	1.30	—	1.50	—	—	1.50	—	
Hold Time	t_h		Data input	0.50	—	0.40	—	—	0.40	—	ns
			S input	−0.45	—	−0.50	—	—	−0.50	—	
Pulse Width	t_W		$\overline{E_1}$, $\overline{E_2}$ (L)	2.00	—	2.00	—	—	2.00	—	ns
			MR (H)	2.00	—	2.00	—	—	2.00	—	

● HD100155F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	Data input	0.60	1.45	0.70	0.95	1.55	0.70	1.55	ns
			S input	1.50	3.00	1.50	1.80	3.20	1.50	3.20	
			$\overline{E}$ input	0.90	2.10	1.00	1.50	2.20	1.00	2.20	
			MR input	1.00	2.50	1.00	1.60	2.70	1.00	2.70	
Transition Time	t_{TLH}, t_{THL}			0.50	1.65	0.50	1.00	1.65	0.50	1.65	ns
Setup Time	t_{SU}		Data input	0.50	—	0.60	—	—	0.60	—	ns
			S input	2.10	—	2.30	—	—	2.30	—	
			MR input (Release Time)	1.20	—	1.40	—	—	1.40	—	
Hold Time	t_h		Data imput	0.30	—	0.30	—	—	0.30	—	ns
			S input	−0.70	—	−0.70	—	—	−0.80	—	
Pulse Width	t_W		$\overline{E_1}$, $\overline{E_2}$ (L)	2.00	—	2.00	—	—	2.00	—	ns
			MR (H)	2.00	—	2.00	—	—	2.00	—	

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

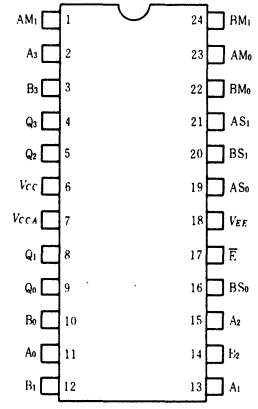
Mask-merge

The HD100156 merges two 4-bit words to form a 4-bit output word. The AMj enable allows the merge of An into Bn by one, two, or three places (per the ASj value) from the left. The BMj enable similarly allows the merge of Bn into An from the left (per the BSj value). The Bn merge overrides the An merge when both are enabled. This means An first merges into Bn and Bn then merges into the An merge. A Bn address (BSj) greater than or equal to the An address (ASj) thus forces the outputs to all Bn. The merge outputs feed 4 latches, which have a common enable ($\overline{E}$) input. All inputs have a 50kΩ (typ.) pull-down resistor tied to V_{EE}.

All four outputs do not have pull-down resistors, so they have wired-OR capability and will require external resistors.

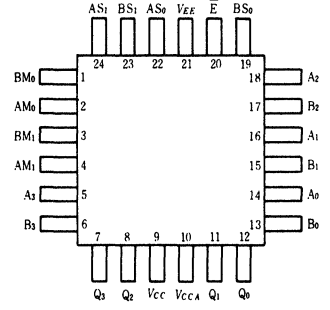
■ PIN ARRANGEMENT

● **HD100156**



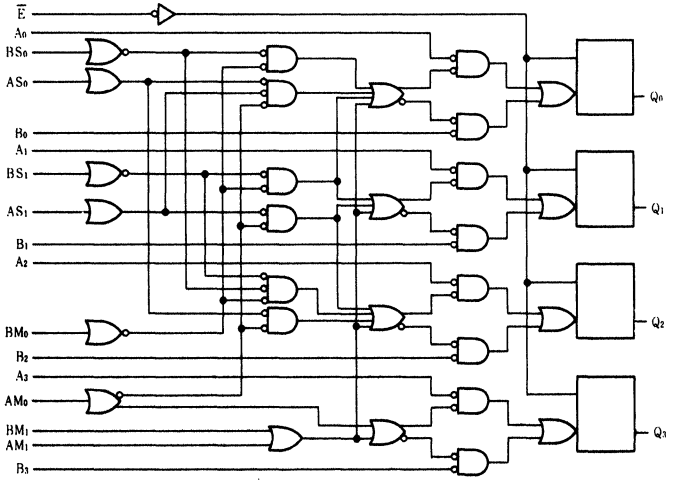
(Top View)

● **HD100156F**



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE

Input									Output				
BM_1	BM_0	AM_1	AM_0	BS_1	BS_0	AS_1	AS_0	$\overline{E}$	Q_0	Q_1	Q_2	Q_3	
×	×	H	×	×	×	×	×	L	B_0	B_1	B_2	B_3	
H	×	×	×	×	×	×	×	L	B_0	B_1	B_2	B_3	
L	L	L	L	×	×	×	×	L	A_0	A_1	A_2	A_3	
L	L	L	H	×	×	L	L	L	B_0	B_1	B_2	B_3	
L	L	L	H	×	×	L	H	L	A_0	B_1	B_2	B_3	
L	L	L	H	×	×	H	L	L	A_0	A_1	B_2	B_3	
L	L	L	H	×	×	H	H	L	A_0	A_1	A_2	B_3	
L	H	L	L	L	L	×	×	L	A_0	A_1	A_2	A_3	
L	H	L	L	L	H	×	×	L	B_0	A_1	A_2	A_3	
L	H	L	L	H	L	×	×	L	B_0	B_1	A_2	A_3	
L	H	L	L	H	H	×	×	L	B_0	B_1	B_2	A_3	
L	H	L	H	L	L	L	H	L	A_0	B_1	B_2	B_3	
L	H	L	H	L	L	H	L	L	A_0	A_1	B_2	B_3	
L	H	L	H	L	L	H	H	L	A_0	A_1	A_2	B_3	
L	H	L	H	L	H	H	L	L	B_0	A_1	B_2	B_3	
L	H	L	H	L	H	H	H	L	B_0	A_1	A_2	B_3	
L	H	L	H	H	L	H	H	L	B_0	B_1	A_2	B_3	
L	H	L	H	H	H	H	H	L	B_0	B_1	B_2	B_3	ADDRESS (BS) > ADDRESS (AS)
L	H	L	H	H	H	H	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	H	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	H	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	H	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	H	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	H	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	L	L	L	L	B_0	B_1	B_2	B_3	
×	×	×	×	×	×	×	×	H	Q_0	Q_1	Q_2	Q_3	

H = High Level
L = Low Level
× = Don't Care

■ DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, $V_{CC} = V_{CCA}$ = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		89	135	196	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$	BS_1, AS_1, $\overline{E}$, BM_1, AM_1	—	—	265	μA
			A_n, B_n	—	—	340	

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

●HD100156

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	A_n, B_n to Output	0.60	1.70	0.70	1.10	1.80	0.70	1.80	ns
			$\overline{E}$ to Ootput	1.20	2.30	1.30	1.50	2.40	1.30	2.40	
			AS_n, BS_n to Output	1.50	3.60	1.60	2.00	3.70	1.60	3.70	
			AM_n, BM_n to Output	1.50	3.60	1.60	2.30	3.70	1.60	3.70	
Transition Time	t_{TLH}, t_{THL}			0.50	1.80	0.50	0.90	1.80	0.50	1.80	ns
Setup Time	t_{SU}		A_n, B_n	0.20	—	0.20	—	—	0.20	—	ns
			AM_n, BM_n, AS_n, BS_n	2.00	—	2.00	—	—	2.00	—	
Hold Time	t_h		A_n, B_n	1.70	—	1.70	—	—	1.70	—	ns
			AM_n, BM_n, AS_n, BS_n	−0.30	—	−0.30	—	—	−0.30	—	
Pulse Width	$t_{W(L)}$		$\overline{E}$	2.00	—	2.00	—	—	2.00	—	ns

●HD100156F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	A_n, B_n to Output	0.60	1.50	0.70	1.00	1.60	0.70	1.60	ns
			$\overline{E}$ to Output	1.30	2.20	1.40	1.70	2.20	1.40	2.35	
			AS_n,BS_n to Output	1.60	3.40	1.60	2.20	3.50	1.60	3.50	
			AM_n, BM_n to Output	1.60	3.40	1.60	2.20	3.50	1.60	3.50	
Transition Time	t_{TLH}, t_{THL}			0.45	1.70	0.45	0.70	1.70	0.45	1.70	ns
Setup Time	t_{SU}		A_n, B_n	0.00	—	0.00	—	—	0.00	—	ns
			AM_n, BM_n, AS_n, BS_n	1.80	—	1.80	—	—	1.90	—	
Hold Time	t_h		A_n, B_n	1.50	—	1.50	—	—	1.50	—	ns
			AM_n, BM_n, AS_n, BS_n	−0.30	—	−0.30	—	—	−0.30	—	
Pulse Width	$t_{W(L)}$		$\overline{E}$	2.00	—	2.00	—	—	2.00	—	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow grater than 2.5m/s (500 linear fpm) is maintained.

8-bit Shift Matrix

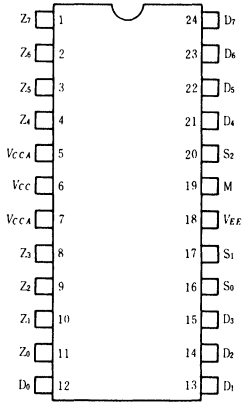
The HD100158 contains a combinatorial network which performs the function of an 8-bit shift matrix. Three control lines (Sn) are internally decoded and define the number of places which an 8-bit word present at the inputs (Dn) is shifted to the left and presented at the outputs (Zn). A Mode Control input (M) is provided which if low, forces low all outputs to the right of the one that contain D_7. This operation is sometimes referred to as "low backfill".

If M is high, an end-round shift is performed such that D_0 appears at the output to the right of the one that contains D_7.

This operation is commonly referred to as "barrel shifting".

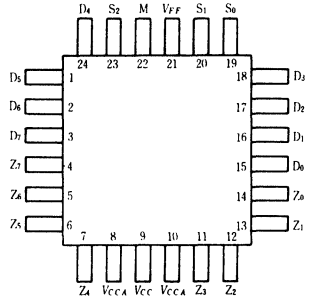
■ PIN ARRANGEMENT

● HD100158



(Top View)

● HD100158F



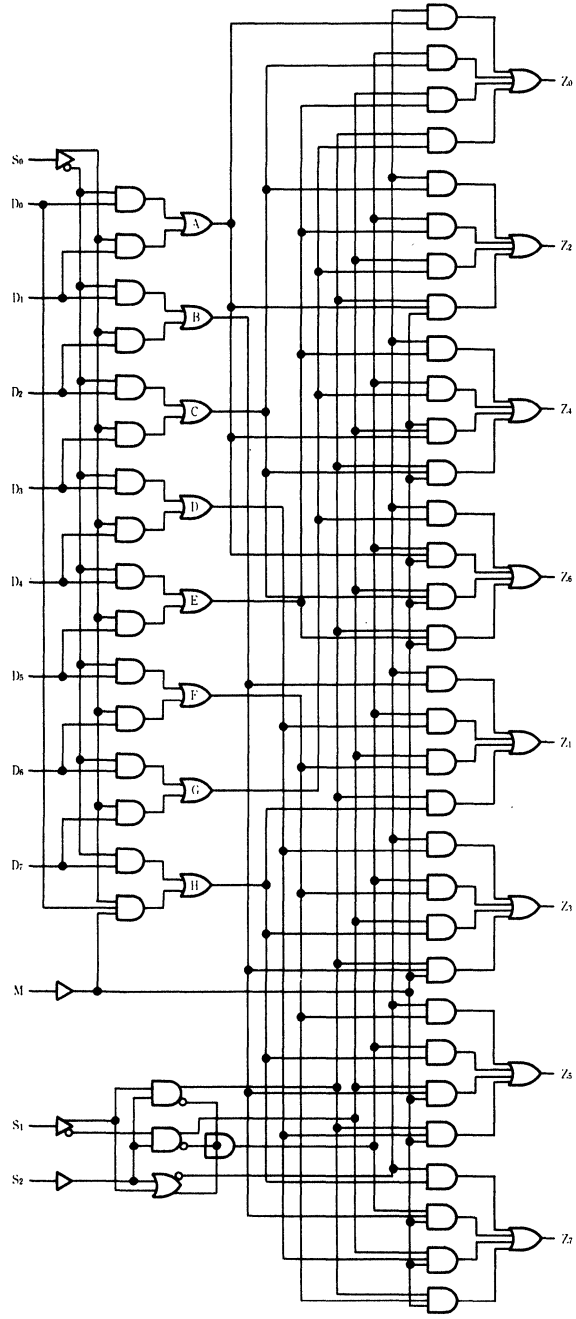
(Top View)

■ TRUTH TABLE

INPUT				OUTPUT							
M	S_0	S_1	S_2	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
×	L	L	L	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
L	H	L	L	D_1	D_2	D_3	D_4	D_5	D_6	D_7	L
L	L	H	L	D_2	D_3	D_4	D_5	D_6	D_7	L	L
L	H	H	L	D_3	D_4	D_5	D_6	D_7	L	L	L
L	L	L	H	D_4	D_5	D_6	D_7	L	L	L	L
L	H	L	H	D_5	D_6	D_7	L	L	L	L	L
L	L	H	H	D_6	D_7	L	L	L	L	L	L
L	H	H	H	D_7	L	L	L	L	L	L	L
H	H	L	L	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0
H	L	H	L	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_1
H	H	H	L	D_3	D_4	D_5	D_6	D_7	D_0	D_1	D_2
H	L	L	H	D_4	D_5	D_6	D_7	D_0	D_1	D_2	D_3
H	H	L	H	D_5	D_6	D_7	D_0	D_1	D_2	D_3	D_4
H	L	H	H	D_6	D_7	D_0	D_1	D_2	D_3	D_4	D_5
H	H	H	H	D_7	D_0	D_1	D_2	D_3	D_4	D_5	D_6

H = High level
L = Low level
× = Immaterial

■ LOGIC DIAGRAM



■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition	min	typ	max	Unit
Supply Current	I_{EE}	All input open	84	120	168	mA
Input Current	I_{IH}	V_{IN} = $V_{IH\ max}$	—	—	220	μA

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100158

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	D_n input to Output	1.10	2.25	1.10	1.70	2.25	1.20	2.35	ns
			M input to Output	1.25	3.50	1.25	2.30	3.70	1.25	3.70	
			S_n input to Output	1.70	3.70	1.70	2.80	3.70	1.70	3.70	
Transition Time	t_{TLH}, t_{THL}			0.50	2.20	0.50	1.30	2.20	0.50	2.20	ns

● HD100158F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test ciscuit and waveform	D_n input to Output	1.10	2.40	1.10	1.60	2.40	1.10	2.50	ns
			M input to Output	1.25	3.70	1.25	2.30	3.80	1.25	3.80	
			S_n input to Output	1.70	3.70	1.70	2.40	3.70	1.70	3.70	
Transition Time	t_{TLH}, t_{THL}			0.50	2.20	0.50	1.00	2.20	0.50	2.20	ns

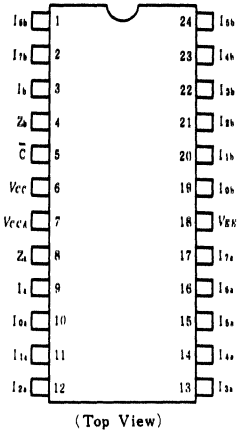
Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

Dual Parity Generators/Checker

The HD100160 is a Dual Parity Checker/Generator. Each half has nine inputs, with the output being high when an even number of inputs are high. One of the nine inputs(Ia or Ib) has the shorter through-put delay and is therefore preferred as the expansion input for generating parity for 16 or more bits. The HD100160 also has a Compare ($\overline{C}$) output which allows the circuit to compare two 8-bit words.
The $\overline{C}$ output is low when the two words match, bit for bit.

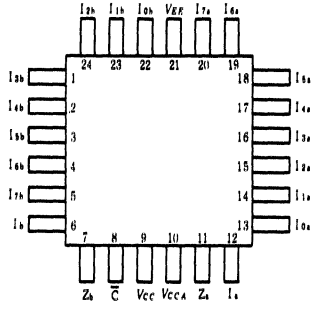
■ PIN ARRANGEMENT

● HD100160



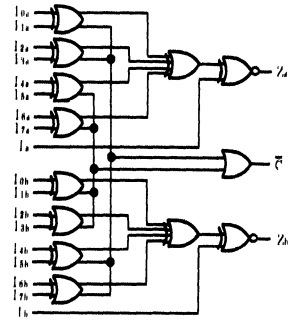
(Top View)

● HD100160F



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE (each half)

Sum of High Input	Output Z
EVEN	H
ODD	L

$\overline{C} = (I_{0a} \oplus I_{1a}) + (I_{2a} \oplus I_{3a}) + (I_{4a} \oplus I_{5a}) + (I_{6a} \oplus I_{7a}) + (I_{0b} \oplus I_{1b}) + (I_{2b} \oplus I_{3b}) + (I_{4b} \oplus I_{5b}) + (I_{6b} \oplus I_{7b})$

■ DC CHARACTERISTICS ($V_{EE} = -4.2$ to -4.8V, $V_{CC} = V_{CCA} = $GND, $Ta = 0$ to $+85$℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		57	82	115	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$	I_b, I_a	—	—	340	μA
			All input except I_b and I_a	—	—	220	μA

Note) As for other items,trefer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100160

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	I_{na}, I_{nb} to Z_a, Z_b	1.20	3.50	1.30	2.50	3.60	1.30	3.60	ns
			I_{na}, I_{nb} to $\overline{C}$	1.10	2.65	1.20	2.00	2.75	1.20	2.75	
			I_a, I_b to Z_a, Z_b	0.50	1.20	0.60	0.90	1.30	0.60	1.30	
Transition Time	t_{TLH}, t_{THL}			0.40	1.40	0.40	0.90	1.40	0.40	1.40	ns

● HD100160F

Item	Symbol	Test Condition		0℃		25℃			85℃ ℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	I_{na}, I_{nb} to Z_a, Z_b	1.20	3.60	1.30	2.30	3.75	1.30	3.75	ns
			I_{na}, I_{nb} to $\overline{C}$	1.10	2.80	1.20	1.90	2.90	1.20	2.90	
			I_d, I_b to Z_a, Z_b	0.50	1.20	0.60	0.80	1.30	0.60	1.30	
Transition Time	t_{TLH}, t_{THL}			0.35	1.30	0.35	0.75	1.30	0.35	1.30	ns

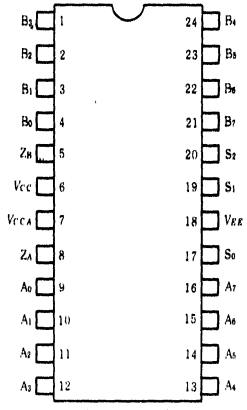
Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

Dual 8-input Multiplexers

The HD100163 is a dual 8-input Multiplexer. The Data Select(Sn) inputs determine which bit (An and Bn) will be presented at the Outputs (Z_A and Z_B respectively). The same bit (0–7) will be selected for both the Z_A and Z_B output.

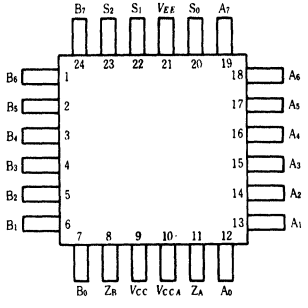
■ PIN ARRANGEMENT

● HD100163



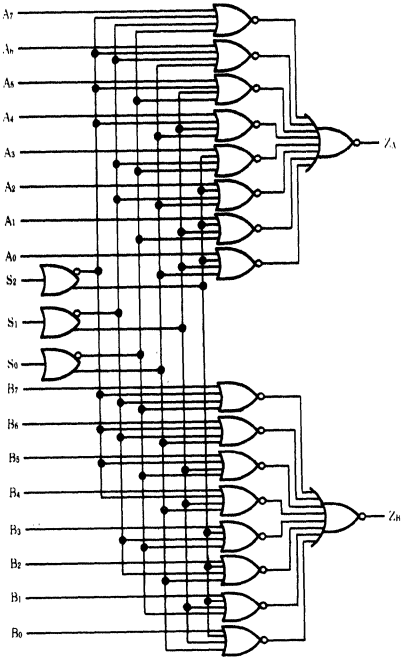
(Top View)

● HD100163F



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE

Input											Output
Address			Data								
S_2	S_1	S_0	A_7 B_7	A_6 B_6	A_5 B_5	A_4 B_4	A_3 B_3	A_2 B_2	A_1 B_1	A_0 B_0	
L	L	L	×	×	×	×	×	×	×	L	L
L	L	L	×	×	×	×	×	×	×	H	H
L	L	H	×	×	×	×	×	×	L	×	L
L	L	H	×	×	×	×	×	×	H	×	H
L	H	L	×	×	×	×	×	L	×	×	L
L	H	L	×	×	×	×	×	H	×	×	H
L	H	H	×	×	×	×	L	×	×	×	L
L	H	H	×	×	×	×	H	×	×	×	H
H	L	L	×	×	×	L	×	×	×	×	L
H	L	L	×	×	×	H	×	×	×	×	H
H	L	H	×	×	L	×	×	×	×	×	L
H	L	H	×	×	H	×	×	×	×	×	H
H	H	L	×	L	×	×	×	×	×	×	L
H	H	L	×	H	×	×	×	×	×	×	H
H	H	H	L	×	×	×	×	×	×	×	L
H	H	H	H	×	×	×	×	×	×	×	H

■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		76	109	153	mA
Input Current	I_{IH}	V_{IN} = $V_{IH\ max}$	S_n input	—	—	265	μA
			A_n, B_n input	—	—	340	μA

Note) As for other item, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100163

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	A_n, B_n input to output	0.60	1.30	0.60	0.95	1.40	0.60	1.40	ns
			S_n input to output	1.25	2.45	1.30	1.75	2.50	1.30	2.50	
Transition Time	t_{TLH}, t_{THL}			0.55	1.70	0.55	1.20	1.70	0.55	1.70	ns

● HD100163F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	A_n, B_n input to output	0.70	1.40	0.80	0.95	1.50	0.80	1.50	ns
			S_n input to output	1.30	2.40	1.40	1.75	2.50	1.40	2.50	
Transition Time	t_{TLH}, t_{THL}			0.55	1.60	0.55	1.10	1.60	0.55	1.60	ns

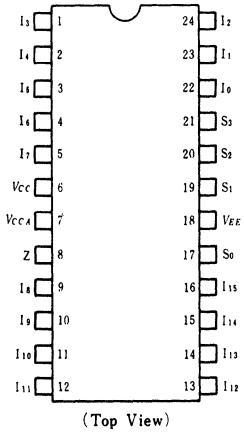
Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

16-input Multiplexer

The HD100164 is a 16-input Multiplexer. Data paths are controlled by four select line (S_0-S_3). Their decoding is shown in the truth table. Output data polarity is the same as the selected input data.

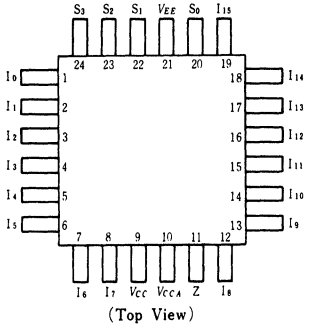
■ PIN ARRANGEMENT

● HD100164



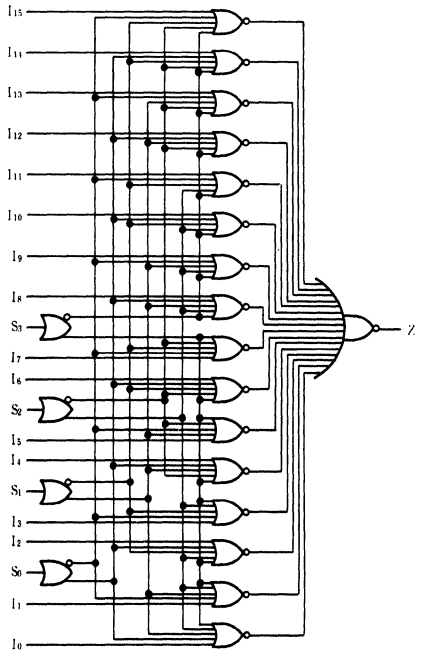
(Top View)

● HD100164F



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE

S_0	S_1	S_2	S_3	Z
L	L	L	L	I_0
H	L	L	L	I_1
L	H	L	L	I_2
H	H	L	L	I_3
L	L	H	L	I_4
H	L	H	L	I_5
L	H	H	L	I_6
H	H	H	L	I_7
L	L	L	H	I_8
H	L	L	H	I_9
L	H	L	H	I_{10}
H	H	L	H	I_{11}
L	L	H	H	I_{12}
H	L	H	H	I_{13}
L	H	H	H	I_{14}
H	H	H	H	I_{15}

■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		43	70	98	mA
Input Current	I_{IH}	V_{IN} = $V_{IH\ max}$	I_n input	—	—	280	μA
			S_0, S_1 input	—	—	240	μA
			S_2, S_3 input	—	—	200	μA

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100164

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	In input to output	0.90	2.20	0.95	1.35	2.35	0.95	2.35	ns
			S_0, S_1 input to output	1.45	3.10	1.45	1.90	3.20	1.45	3.20	
			S_2, S_3 input to output	1.05	2.40	1.10	1.50	2.50	1.10	2.50	
Transition Time	t_{TLH}, t_{THL}			0.55	1.60	0.55	0.90	1.60	0.55	1.60	ns

● HD100164F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	In input to output	0.90	2.00	1.00	1.35	2.15	1.00	2.15	ns
			S_0, S_1 input to output	1.35	2.90	1.45	2.00	3.00	1.45	3.00	
			S_2, S_3 input to output	1.00	2.20	1.10	1.50	2.30	1.10	2.30	
Transition Time	t_{TLH}, t_{THL}			0.50	1.50	0.50	0.90	1.50	0.50	1.50	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

Universal Priority Encoders

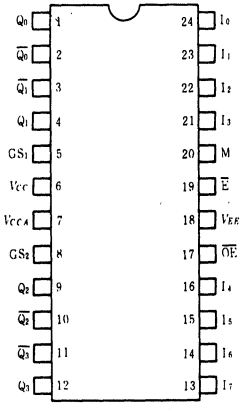
The HD100165 contains eight input latches with a Common Enable ($\overline{E}$) followed by encoding logic which generates the binary address of the highest priority input having a high signal. The circuit operates as a dual 4-input encoder when the Mode Control input (M) is low, and as a single 8-input encoder when M is high.

In the 8-input mode, Q_0, Q_1 and Q_2 are the relevant outputs, I_0 is the highest priority input and GS_1 is the relevant Group Signal output. In the dual mode, Q_0, Q_1 and GS_1 operate with I_0-I_3. Q_2, Q_3 and GS_2 operate with I_4-I_7.

A GS output goes low when its pertinent inputs are all low. Inputs are latched when $\overline{E}$ goes high. A high signal on the Output Enable ($\overline{OE}$) input forces all Q outputs low and GS outputs high. Expansion to accommodate more inputs can be done by connecting the GS output of a higher priority group to the $\overline{OE}$ input of the next lower priority group.

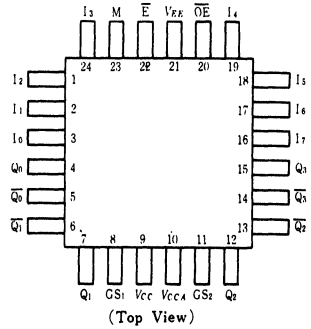
■ PIN ARRANGEMENT

● HD100165



(Top View)

● HD100165F



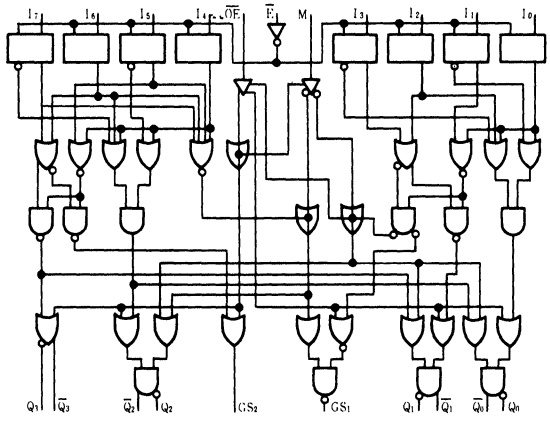
(Top View)

■ TRUTH TABLE

$\overline{E}$	$\overline{OE}$	M	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Q_0	Q_1	Q_2	Q_3	GS_1	GS_2
L	L	L	H	×	×	×					L	L			H	
L	L	L	L	H	×	×					H	L			H	
L	L	L	L	L	H	×					L	H			H	
L	L	L	L	L	L	H					H	H			H	
L	L	L	L	L	L	L					L	L			L	
L	L	L					H	×	×	×			L	L		H
L	L	L					L	H	×	×			H	L		H
L	L	L					L	L	H	×			L	H		H
L	L	L					L	L	L	H			H	H		H
L	L	L					L	L	L	L			L	L		L
L	L	H	H	×	×	×	×	×	×	×	L	L	L	L	H	H
L	L	H	L	H	×	×	×	×	×	×	H	L	L	L	H	H
L	L	H	L	L	H	×	×	×	×	×	L	H	L	L	H	H
L	L	H	L	L	L	H	×	×	×	×	H	H	L	L	H	H
L	L	H	L	L	L	L	H	×	×	×	L	L	H	L	H	H
L	L	H	L	L	L	L	L	H	×	×	H	L	H	L	H	H
L	L	H	L	L	L	L	L	L	H	×	L	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	H	H	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H
×	H	×	×	×	×	×	×	×	×	×	L	L	L	L	H	H
H	L	L	×	×	×	×	×	×	×	×	*	*	*	*	*	*
H	L	H	×	×	×	×	×	×	×	×	*	*	*	*	*	*

H = High Level
L = Low Level
* = Stores data present before $\overline{E}$ went high.

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS (V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition	min	typ	max	Unit
Supply Current	I_{EE}	All input open	77	110	154	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$	—	—	230	μA

Note) As for other items, refer to the "Common DC Characteristics".

■ AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100165

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	In input to Q_n, $\overline{Q_n}$	1.00	3.35	1.10	2.15	3.40	1.20	3.60	ns
			In input to GS_1, GS_2	1.20	3.35	1.30	2.00	3.40	1.40	3.60	
			$\overline{E}$ input to Q_n, $\overline{Q_n}$, GS_1, GS_2	1.50	3.70	1.50	3.00	3.80	1.60	3.90	
			$\overline{OE}$ input to Q_n, $\overline{Q_n}$	0.90	2.45	1.00	1.75	2.60	1.10	2.80	
			$\overline{OE}$ input to GS_1, GS_2	1.00	2.50	1.10	1.70	2.60	1.20	2.60	
			M input to Q_n, $\overline{Q_n}$, GS_1, GS_2	0.90	3.05	1.00	2.00	3.10	1.10	3.30	
Transition Time	t_{TLH}, t_{THL}			0.35	1.30	0.35	0.75	1.30	0.35	1.30	ns
Setup Time	t_{SU}			0.70	—	0.80	—	—	0.80	—	ns
Hold Time	t_h			0.60	—	0.60	—	—	0.70	—	ns

● HD100165F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	In input to Q_n, $\overline{Q_n}$	1.00	3.40	1.10	2.15	3.45	1.10	3.55	ns
			In input to GS_1, GS_2	1.20	3.40	1.30	2.00	3.45	1.30	3.55	
			$\overline{E}$ input to Q_n, $\overline{Q_n}$, GS_1, GS_2	1.50	3.70	1.60	3.00	3.80	1.70	3.90	
			$\overline{OE}$ input to Q_n, $\overline{Q_n}$	0.90	2.40	1.00	1.75	2.50	1.00	2.50	
			$\overline{OE}$ input to GS_1, GS_2	1.00	2.30	1.10	1.70	2.40	1.10	2.40	
			M input to Q_n, $\overline{Q_n}$, GS_1, GS_2	1.00	3.00	1.00	2.00	3.00	1.00	3.00	
Transition Time	t_{TLH}, t_{THL}			0.40	1.30	0.40	0.80	1.30	0.40	1.30	ns
Setup Time	t_{SU}			0.60	—	0.60	—	—	0.60	—	ns
Nold Time	t_h			0.40	—	0.40	—	—	0.40	—	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

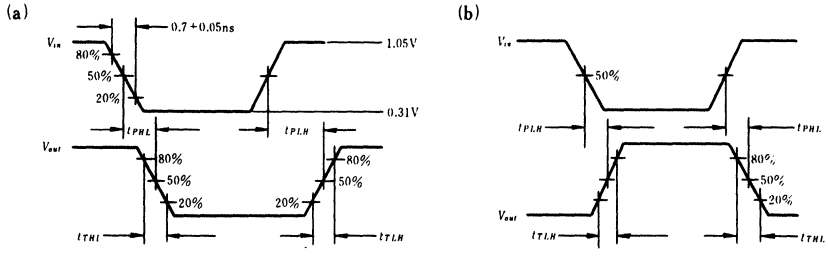


Fig.1 Propagation Delay Time

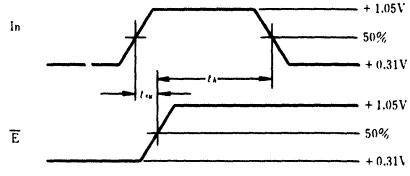


Fig.2 Set-up and Hold Time

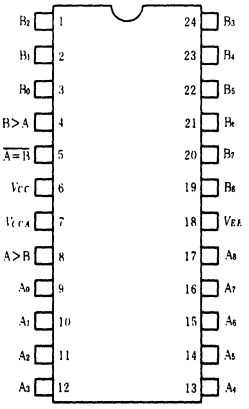
9-bit Comparator

The HD100166 is a 9-bit Magnitude Comparator which compares the arithmetic value of two 9-bit words and indicates whether one word is greater than, or equal to the other.

The outputs do not have pull down resistors, which provides the wire OR functions by trying several outputs together.

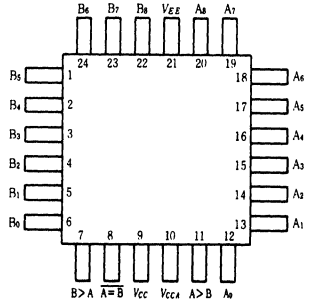
■ PIN ARRANGEMENT

● HD100166



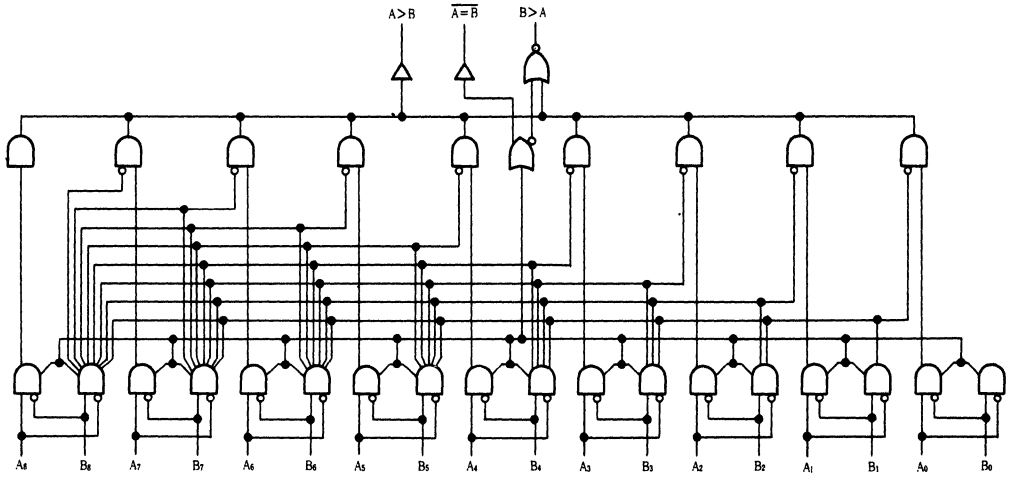
(Top View)

● HD100166F



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE

Input										Output		
A_8 B_8	A_7 B_7	A_6 B_6	A_5 B_5	A_4 B_4	A_3 B_3	A_2 B_2	A_1 B_1	A_0 B_0		A>B	B>A	$\overline{A=B}$
H L										H	L	H
L H										L	H	H
$A_8=B_8$	H L									H	L	H
$A_8=B_8$	L H									L	H	H
$A_8=B_8$	$A_7=B_7$	H L								H	L	H
$A_8=B_8$	$A_7=B_7$	L H								L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	H L							H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	L H							L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	H L						H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	L H						L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	H L					H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	L H					L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	H L				H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	L H				L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	H L			H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	L H			L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	H L		H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	L H		L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$		L	L	L

H = High Level
L = Low Level
Blank = Don't care

■ DC CHARACTERISTICS ($V_{EE}=-4.2$ to -4.8V, $V_{CC}=V_{CCA}=$GND, $Ta=0$ to $+85$℃)

Item	Symbol	Test Condition	min	typ	max	Unit
Supply Current	I_{EE}	All input open	119	170	238	mA
Input Current	I_{IH}	$V_{IH}=V_{IH\ max}$	—	—	250	μA

Note) As for other items, refer to the "Common DC Characteristics".

■ AC CHARACTERISTICS ($V_{EE}=-2.2$ to -2.8V, $V_{CC}=V_{CCA}=2.0$V)

● HD100166

Item	Symbol	Test Condition	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	1.30	2.90	1.40	2.10	3.00	1.40	3.00	ns
Transition Time	t_{TLH} t_{THL}		0.45	1.55	0.45	0.90	1.45	0.45	1.45	ns

● HD100166F

Item	Symbol	Test Condition	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	1.40	3.10	1.40	2.10	3.00	1.40	3.10	ns
Transition Time	t_{THL} t_{THL}		0.45	1.30	0.45	0.90	1.30	0.45	1.30	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100170/F

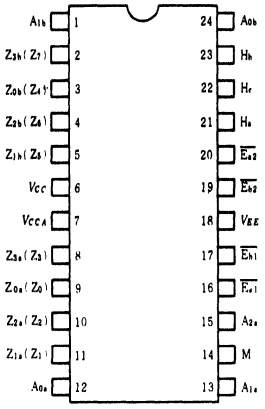
Universal Demultiplexer/Decoder

The HD100170 Universal Demultiplexer/Decoder functions as either a dual Mode Control input(M). In the dual mode, each half has a pair of active low Enable($\overline{E}$) inputs. Pin assignments for the $\overline{E}$ inputs are such that in the 1-of-8 mode they can easily be tied together in pairs to provide two active low enables (pin 16 to 17 and pin 19 to 20).

Signals applied to auxiliary inputs Ha, Hb and Hc determine whether the outputs are active high or active low. In the dual 1-of-4 mode the address inputs are A0a, A1a and A0b, A1b with A2a unused (i.e., left open, tied to V_{BB} or with low signal applied). In the 1-of-8 mode, the address inputs are A0a, A1a, A2a with A0b and A1b low or open.

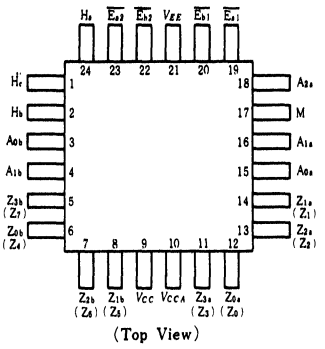
■ PIN ARRANGEMENT

● HD100170



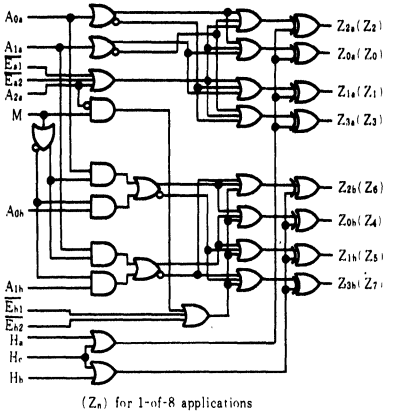
(Top View)

● HD100170F



(Top View)

■ LOGIC DIAGRAM



(Z_n) for 1-of-8 applications

■ TRUTH TABLE

● Dual 1-of-4 Mode ($M = A_{2a} = Hc = L$)

Input				Active High Output ($H_a, H_b = H$)				Active Low Output ($H_a, H_b = L$)			
$\overline{E_{a1}}$	$\overline{E_{a2}}$	A_{1a}	A_{0a}	Z_{0a}	Z_{1a}	Z_{2a}	Z_{3a}	Z_{0a}	Z_{1a}	Z_{2a}	Z_{3a}
$\overline{E_{b1}}$	$\overline{E_{b2}}$	A_{1b}	A_{0b}	Z_{0b}	Z_{1b}	Z_{2b}	Z_{3b}	Z_{0b}	Z_{1b}	Z_{2b}	Z_{3b}
H	×	×	×	L	L	L	L	H	H	H	H
×	H	×	×	L	L	L	L	H	H	H	H
L	L	L	L	H	L	L	L	L	H	H	H
L	L	L	H	L	H	L	L	H	L	H	H
L	L	H	L	L	L	H	L	H	H	L	H
L	L	H	H	L	L	L	H	H	H	H	L

● Single 1-of-8 Mode ($M=H: A_{0b}=A_{1b}=H_a=H_b=L$)

Input					Active High Output ($H_C=H$)*							
$\overline{E_1}$	$\overline{E_2}$	A_{2a}	A_{1a}	A_{0a}	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
H	×	×	×	×	L	L	L	L	L	L	L	L
×	H	×	×	×	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

* For H_C = Low, output states are complemented.
$E_1 = E_{a1} \cdot E_{b1}$, $E_{a2} \cdot E_{b2}$

■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, $V_{CC}=V_{CCA}$=GND, Ta=0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		76	109	153	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	H_0, A_0, A_{1a}, A_{2a} input	—	—	310	μA
			All other input	—	—	250	μA

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, $V_{CC}=V_{CCA}$=2.0V)

● HD100170

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	$\overline{E_{an}}$, $\overline{E_{bn}}$, input to output	0.80	1.65	0.90	1.35	1.75	0.90	1.75	ns
			A_{na}, A_{nb} input to output	0.75	2.10	0.90	1.40	2.20	0.90	2.20	
			H input to output	0.90	2.50	1.00	1.75	2.60	1.00	2.60	
			M input to output	1.40	3.30	1.55	2.10	3.50	1.55	3.55	
Transition Time	t_{TLH}, t_{THL}			0.35	2.20	0.35	1.00	2.20	0.35	2.20	ns

● HD100170F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	$\overline{E_{an}}$, $\overline{E_{bn}}$ input to output	0.80	1.70	0.90	1.30	1.80	0.90	1.80	ns
			A_{nd}, A_{nb} inqut to output	0.80	2.20	0.90	1.60	2.30	0.90	2.30	
			H input to output	0.90	2.40	1.00	1.75	2.50	1.00	2.50	
			M input to Output	1.50	3.40	1.60	2.10	3.60	1.60	3.60	
Transition Time	t_{TLH}, t_{THL}			0.45	1.60	0.45	1.00	1.60	0.45	1.60	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

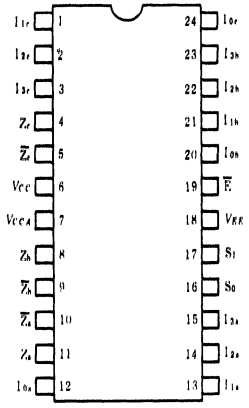
HD100171/F

Triple 4-input Multiplexers with Enable

The HD100171 contains Triple 4-input multiplexers which share a common decoder (inputs S0 and S1). Output buffer gates provide true and complement outputs. A high on the Enable input ($\overline{E}$) forces all true outputs low (see truth table).

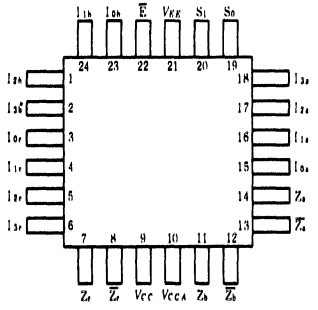
■ PIN ARRANGEMENT

● HD100171

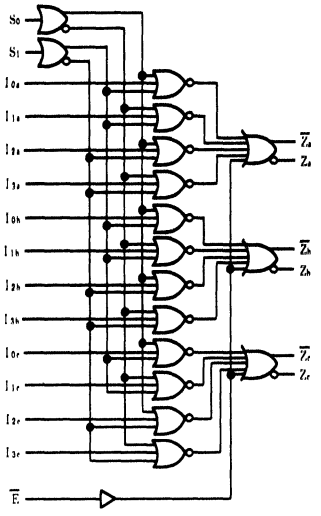


(Top View)

● HD100171F



■ LOGIC DIAGRAM



■ TRUTH TABLE

$\overline{E}$	S_0	S_1	Z_n
L	L	L	I_{0n}
L	H	L	I_{1n}
L	L	H	I_{2n}
L	H	H	I_{3n}
H	×	×	L

■ DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, $V_{CC} = V_{CCA}$ = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		56	81	114	mA
Inqut Current	I_{IH}	$V_{IN} = V_{IH\ max}$	S_0, S_1, $\overline{E}$ input	—	—	300	μA
			Data input	—	—	340	μA

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100171

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	I_{0x}~I_{3x} input to output	0.45	1.30	0.55	0.95	1.40	0.60	1.45	ns
			S_0/S_1 input to output	0.90	2.10	1.00	1.30	2.20	1.00	2.20	
			$\overline{E}$ input to output	0.80	1.95	0.90	1.50	2.05	0.90	2.05	
Transition Time	t_{TLH}, t_{THL}			0.40	1.40	0.40	0.80	1.40	0.40	1.40	ns

● HD100171F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	I_{0x}~I_{3x} input to output	0.45	1.25	0.55	0.90	1.30	0.55	1.40	ns
			S_0/S_1 input to output	1.00	2.20	1.10	1.40	2.30	1.10	2.30	
			$\overline{E}$ input to output	0.90	2.00	1.00	1.50	2.10	1.00	2.10	
Transition Time	t_{TLH}, t_{THL}			0.50	1.35	0.50	0.90	1.35	0.50	1.35	ns

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

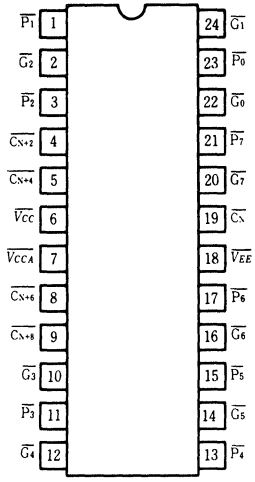
HD100179/F

Carry Look-ahead

The HD100179 is a high speed carry look-ahead generator intended for use with the HD100180 6-bit fast Adder and the HD100181 4-bit ALU.

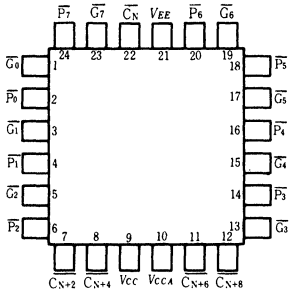
■ PIN ARRANGEMENT

● HD100179



(Top View)

● HD100179F



(Top View)

■ TRUTH TABLE

● $\overline{C_{N+2}}$ Output

$\overline{C_N}$	$\overline{G_0}$	$\overline{P_0}$	$\overline{G_1}$	$\overline{P_1}$	$\overline{C_{N+2}}$
×	×	×	L	×	L
×	L	×	×	L	L
L	×	L	×	L	L
All other combinations					H

$\overline{C_{N+2}} = \overline{G_1} \cdot (\overline{P_1} + \overline{G_0}) \cdot (\overline{P_1} + \overline{P_0} + \overline{C_N})$

× = Don't care

● $\overline{C_{N+4}}$ Output

$\overline{C_N}$	$\overline{G_0}$	$\overline{P_0}$	$\overline{G_1}$	$\overline{P_1}$	$\overline{G_2}$	$\overline{P_2}$	$\overline{G_3}$	$\overline{P_3}$	$\overline{C_{N+4}}$
×	×	×	×	×	×	×	L	×	L
×	×	×	×	×	L	×	×	L	L
×	×	×	L	×	×	L	×	L	L
×	L	×	×	L	×	L	×	L	L
L	×	L	×	L	×	L	×	L	L
All other combinations									H

$\overline{C_{N+4}} = \overline{G_3} \cdot (\overline{P_3} + \overline{G_2}) \cdot (\overline{P_3} + \overline{P_2} + \overline{G_1}) \cdot (\overline{P_3} + \overline{P_2} + \overline{P_1} + \overline{G_0}) \cdot (\overline{P_3} + \overline{P_2} + \overline{P_1} + \overline{P_0} + \overline{C_N})$

● $\overline{C_{N+6}}$ Output

$\overline{C_N}$	$\overline{G_0}$	$\overline{P_0}$	$\overline{G_1}$	$\overline{P_1}$	$\overline{G_2}$	$\overline{P_2}$	$\overline{G_3}$	$\overline{P_3}$	$\overline{G_4}$	$\overline{P_4}$	$\overline{G_5}$	$\overline{P_5}$	$\overline{C_{N+6}}$
×	×	×	×	×	×	×	×	×	×	×	L	×	L
×	×	×	×	×	×	×	×	×	L	×	×	L	L
×	×	×	×	×	×	×	L	×	×	L	×	L	L
×	×	×	×	×	L	×	×	L	×	L	×	L	L
×	×	×	L	×	×	L	×	L	×	L	×	L	L
×	L	×	×	L	×	L	×	L	×	L	×	L	L
L	×	L	×	L	×	L	×	L	×	L	×	L	L
All other combinations													H

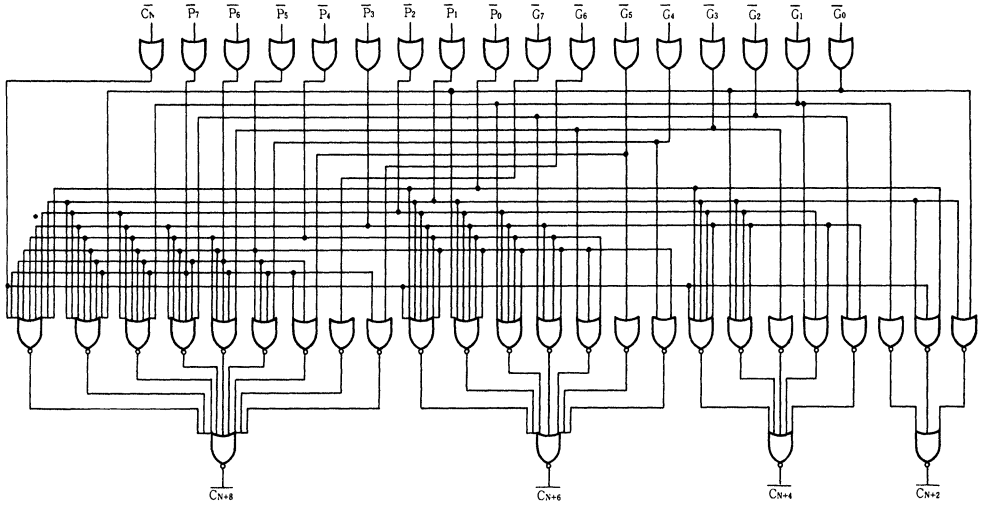
$\overline{C_{N+6}} = \overline{G_5} \cdot (\overline{P_5} + \overline{G_4}) \cdot (\overline{P_5} + \overline{P_4} + \overline{G_3}) \cdot (\overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{G_2}) \cdot (\overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{P_2} + \overline{G_1}) \cdot (\overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{P_2} + \overline{P_1} + \overline{G_0}) \cdot (\overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{P_2} + \overline{P_1} + \overline{P_6} + \overline{C_N})$

● $\overline{C_{N+8}}$ Output

$\overline{C_N}$	$\overline{G_0}$	$\overline{P_0}$	$\overline{G_1}$	$\overline{P_1}$	$\overline{G_2}$	$\overline{P_2}$	$\overline{G_3}$	$\overline{P_3}$	$\overline{G_4}$	$\overline{P_4}$	$\overline{G_5}$	$\overline{P_5}$	$\overline{G_6}$	$\overline{P_6}$	$\overline{G_7}$	$\overline{P_7}$	$\overline{C_{N+8}}$
×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	L	×	L
×	×	×	×	×	×	×	×	×	×	×	×	×	L	×	×	L	L
×	×	×	×	×	×	×	×	×	×	×	L	×	×	L	×	L	L
×	×	×	×	×	×	×	×	×	L	×	×	L	×	L	×	L	L
×	×	×	×	×	×	×	L	×	×	L	×	L	×	L	×	L	L
×	×	×	×	×	L	×	×	L	×	L	×	L	×	L	×	L	L
×	×	×	L	×	×	L	×	L	×	L	×	L	×	L	×	L	L
×	L	×	×	L	×	L	×	L	×	L	×	L	×	L	×	L	L
L	×	L	×	L	×	L	×	L	×	L	×	L	×	L	×	L	L
All other combinations																	H

$\overline{C_{N+8}} = \overline{G_7} \cdot (\overline{P_7} + \overline{G_6}) \cdot (\overline{P_7} + \overline{P_6} + \overline{G_5}) \cdot (\overline{P_7} + \overline{P_6} + \overline{P_5} + \overline{G_4}) \cdot (\overline{P_7} + \overline{P_6} + \overline{P_5} + \overline{P_4} + \overline{G_3}) \cdot (\overline{P_7} + \overline{P_6} + \overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{G_2}) \cdot (\overline{P_7} + \overline{P_6} + \overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{P_2} + \overline{G_1}) \cdot (\overline{P_7} + \overline{P_6} + \overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{P_2} + \overline{P_1} + \overline{G_0}) \cdot (\overline{P_7} + \overline{P_6} + \overline{P_5} + \overline{P_4} + \overline{P_3} + \overline{P_2} + \overline{P_1} + \overline{P_0} + \overline{C_N})$

■LOGIC DIAGRAM



■DC CHARACTERISTICS ($V_{EE}=-4.2$ to -4.8V, $V_{CC}=V_{CCA}$=GND, $Ta=0$ to $+85$℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		115	165	231	mA
Input Current	I_{IH}	$V_{IN}=V_{IH\ max}$	$\overline{C_n}$, $\overline{G_n}$ input	—	—	250	μA
			$\overline{P_n}$ input	—	—	340	

Note) As for other items, refer the "Common DC Characteristics".

■AC CHARACTERISTICS ($V_{EE}=-2.2$ to -2.8V, $V_{CC}=V_{CCA}=2.0$V)

● HD100170

Item	Symbol	Test Condition	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	1.10	2.30	1.10	1.70	2.40	1.20	2.40	ns
Transition Time	t_{TLH} t_{THL}		0.40	1.60	0.40	0.80	1.60	0.40	1.60	ns

● HD100179F

Item	Symbol	Test Condition	0℃		25℃			85℃		Unit
			min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	1.00	2.45	1.10	1.50	2.45	1.10	2.55	ns
Transition Time	t_{TLH} t_{THL}		0.45	1.50	0.45	0.65	1.50	0.45	1.50	ns

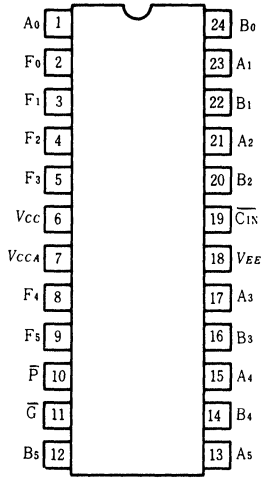
Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

Fast 6-bit Adder

The HD100180 is a High Speed 6-bit Adder capables of performing as full 6-bit addition of 2 operands in 2ns.
Inputs for the adder are active low Carry-In, Operand A, and Operand B; outputs are Function, active low Carry Generate, and active low Carry Propagate. When used with the HD100179, Full Carry Lookahead, as a second order Lookahead Block. HD100180 provides high speed addition of very long words.

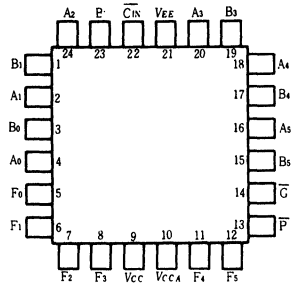
■PIN ARRANGEMENT

● **HD100180**



(Top View)

● **HD100180F**



(Top View)

■LOGIC FUNCTION

$F_0 = P_0 \oplus C_{IN}$

$F_1 = P_1 \oplus (G_0 + P_0 C_{IN})$

$F_2 = P_2 \oplus (G_1 + P_1 G_0 + P_1 P_0 C_{IN})$

$F_3 = P_3 \oplus (G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_{IN})$

$F_4 = P_4 \oplus (G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 G_0 C_{IN})$

$F_5 = P_5 \oplus (G_4 + P_4 G_3 + P_4 P_3 G_2 + P_4 P_3 P_2 G_1 + P_4 P_3 P_2 P_1 G_0 + P_4 P_3 P_2 P_1 P_0 C_{IN})$

$\bar{P} = \overline{P_0 P_1 P_2 P_3 P_4 P_5}$

$\bar{G} = \overline{G_5 + P_5 G_4 + P_5 P_4 G_3 + P_5 P_4 P_3 G_2 + P_5 P_4 P_3 P_2 G_1 + P_5 P_4 P_3 P_2 P_1 G_0}$

$P_0 = A_0 \oplus B_0 \quad G_0 = A_0 \cdot B_0$

$P_1 = A_1 \oplus B_1 \quad G_1 = A_1 \cdot B_1$

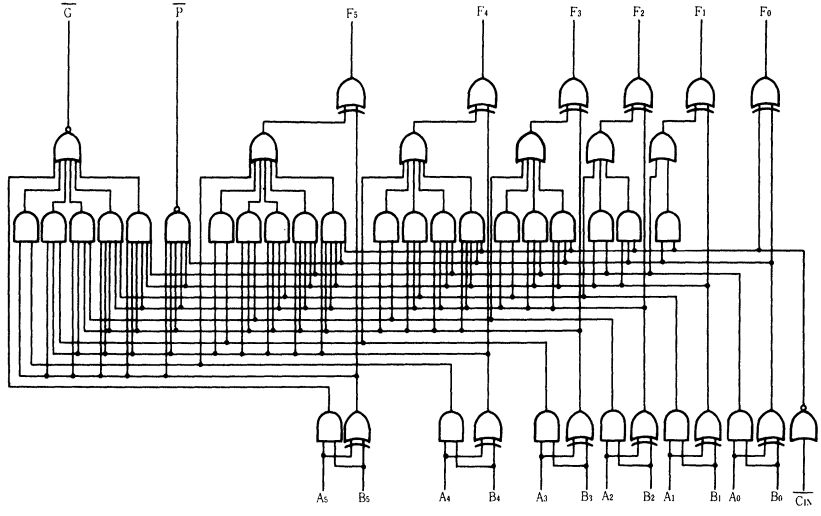
$P_2 = A_2 \oplus B_2 \quad G_2 = A_2 \cdot B_2$

$P_3 = A_3 \oplus B_3 \quad G_3 = A_3 \cdot B_3$

$P_4 = A_4 \oplus B_4 \quad G_4 = A_4 \cdot B_4$

$P_5 = A_5 \oplus B_5 \quad G_5 = A_5 \cdot B_5$

■LOGIC DIAGRAM



■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition	min	typ	max	Unit
Supply Current	I_{EE}	All input open	137	195	255	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$	—	—	220	μA

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100180

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	A_n, B_n input to F_n	1.10	3.40	1.20	2.25	3.55	1.20	3.75	ns
			A_n, B_n input to $\overline{P}$	0.85	2.60	1.00	1.70	2.75	1.00	2.85	
			A_n, B_n input to $\overline{G}$	1.40	3.00	1.40	2.30	3.20	1.60	3.55	
			$\overline{C_{IN}}$ input to F_n	0.90	3.10	1.00	2.10	3.25	1.00	3.40	
Transition Time	t_{TLH}, t_{THL}			0.45	2.30	0.45	1.30	2.30	0.45	2.40	ns

● HD100180F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	A_n, B_n input to F_n	1.20	3.40	1.20	2.25	3.55	1.40	3.85	ns
			A_n, B_n input to $\overline{P}$	0.85	2.60	0.90	1.70	2.70	1.00	2.80	
			A_n, B_n input to $\overline{G}$	1.40	3.10	1.40	2.10	3.20	1.60	3.55	
			$\overline{C_{IN}}$ input to F_n	0.90	3.25	1.00	2.10	3.25	1.00	3.60	
Transition Time	t_{TLH}, t_{THL}			0.45	2.20	0.45	1.30	2.20	0.45	2.20	ns

Note) The circuit in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

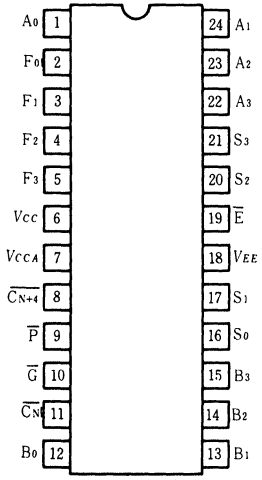
4-bit Binary/BCD ALU

The HD100181 performs eight logic operations and eight arithmetic operations on a pair of 4-bit words. The operating mode is determined by signals applied to the Select (Sn) inputs, as shown in the Function Select table. In addition to performing binary arithmetic, the circuit contains the necessary correction logic to perform BCD addition and subtraction. Output latches are provided to reduce overall package count and increase system operating speed. When the latches are not required, leaving the Enable ($\overline{E}$) input open makes the latches transparent.

The circuit uses internal lookahead carry to minimize delay to the F outputs and to the ripple Carry Output, $\overline{Cn+4}$. Group carry lookahead Propagate ($\overline{P}$) and Generate ($\overline{G}$) outputs are also provided, which are independent of the carry In $\overline{Co}$. The $\overline{P}$ output goes low when a plus operation produces fifteen (nine for BCD) or when a minus operation produces zero. Similarly, $\overline{G}$ goes low when the sum of A and B is greater than fifteen (nine for BCD) in plus mode, or when their difference is greater than zero in a minus mode.

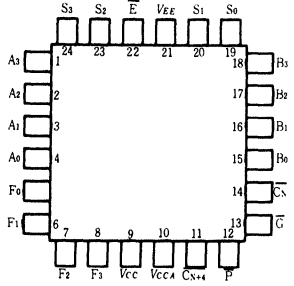
■PIN ARRANGEMENT

● HD100181



(Top View)

● HD100181F

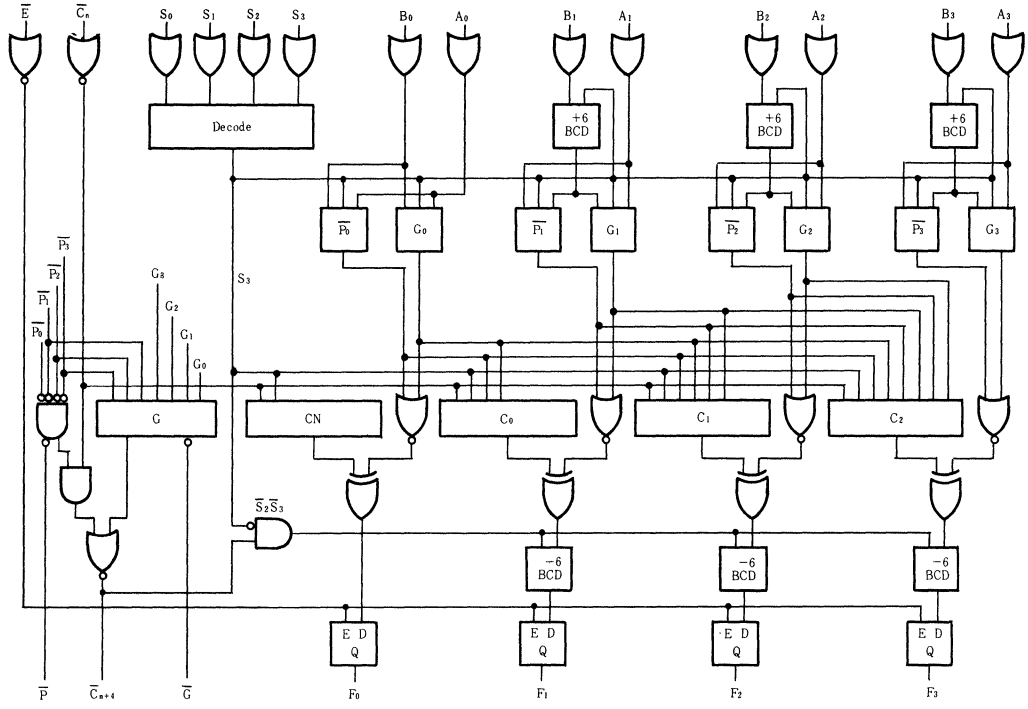


(Top View)

■FUNCTION SELECT TABLE

S_3	S_2	S_1	S_0	Function
L	L	L	L	A plus B BCD
L	L	L	H	A minus B BCD
L	L	H	L	B minus A BCD
L	L	H	H	0 minus B BCD
L	H	L	L	A plus B Binary
L	H	L	H	A minus B Binary
L	H	H	L	B minus A Binary
L	H	H	H	0 minus B Binary
H	L	L	L	$Fn=AnBn+\overline{An}\overline{Bn}$
H	L	L	H	$Fn=An\overline{Bn}+\overline{An}Bn$
H	L	H	L	$Fn=An+Bn$
H	L	H	H	$Fn=An$
H	H	L	L	$Fn=\overline{Bn}$
H	H	L	H	$Fn=Bn$
H	H	H	L	$Fn=AnBn$
H	H	H	H	Fn=Low

■LOGIC DIAGRAM



■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		135	195	270	mA
Input Current	I_{IH}	V_{IN} = $V_{IH\ max}$	S_n, $\overline{E}$ input	—	—	350	μA
			Other inputs	—	—	250	μA

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100181

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	$\overline{C_n}\rightarrow F_n$	1.50	5.00	1.60	3.00	5.20	1.60	5.40	ns
			$\overline{C_n}\rightarrow\overline{C_{n+4}}$	1.10	2.80	1.30	1.80	3.00	1.30	3.00	
			$A_n, B_n\rightarrow\overline{P}, \overline{G}$	1.30	3.80	1.40	2.50	3.90	1.40	3.90	
			$S_n\rightarrow\overline{P}, \overline{G}$	1.80	4.90	2.00	3.50	5.10	2.00	5.40	
			$A_n, B_n\rightarrow\overline{C_{n+4}}$	2.00	5.00	2.00	3.50	5.10	2.10	5.30	
			$S_n\rightarrow\overline{C_{n+4}}$	2.70	6.50	2.80	4.00	6.75	2.80	6.90	
			$A_n, B_n\rightarrow F_n$	2.10	6.20	2.10	4.00	6.20	2.20	6.40	
			$S_n\rightarrow F_n$	1.30	6.20	1.50	4.00	6.50	1.50	6.90	
			$\overline{E}\rightarrow F_n$	0.90	2.50	1.00	1.50	2.50	1.00	2.50	
Transition Time	t_{THL}, t_{TLH}			0.45	3.60	0.45	1.00	3.50	0.45	3.60	ns
Setup Time	t_{SU}	$A_n, B_n\rightarrow\overline{E}$		5.20	—	5.50	—	—	6.00	—	ns
		$S_n\rightarrow\overline{E}$		6.00	—	6.00	—	—	6.50	—	
		$\overline{C_n}\rightarrow\overline{E}$		4.30	—	4.50	—	—	4.80	—	
Hold Time	t_h	$A_n, B_n\rightarrow\overline{E}$		0.10	—	0.10	—	—	0.10	—	ns
		$S_n\rightarrow\overline{E}$		0.60	—	0.60	—	—	0.60	—	
		$\overline{C_n}\rightarrow\overline{E}$		0.60	—	0.60	—	—	0.60	—	
Pulse Width	$t_{W(L)}$	$\overline{E}$		2.00	—	2.00	—	—	2.00	—	ns

● HD100181F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	$\overline{C_n}\rightarrow F_n$	1.50	4.80	1.60	3.00	5.00	1.80	5.50	ns
			$\overline{C_n}\rightarrow\overline{C_{n+4}}$	1.25	2.50	1.35	1.80	2.80	1.35	2.90	
			$A_n, B_n\rightarrow\overline{P}, \overline{G}$	1.30	3.40	1.40	2.20	3.70	1.60	3.90	
			$S_n\rightarrow\overline{P}, \overline{G}$	1.90	4.80	2.00	2.80	5.00	2.20	5.80	
			$A_n, B_n\rightarrow\overline{C_{n+4}}$	2.00	5.20	2.00	3.60	5.70	2.40	6.00	
			$S_n\rightarrow\overline{C_{n+4}}$	2.70	6.40	2.80	4.50	6.75	3.00	7.40	
			$A_n, B_n\rightarrow F_n$	2.00	6.00	2.10	4.50	6.30	2.30	6.80	
			$S_n\rightarrow F_n$	1.30	7.00	1.50	5.00	7.20	1.70	7.80	
			$\overline{E}\rightarrow F_n$	0.85	2.50	0.90	1.50	2.80	0.90	2.80	
Transition Time	t_{THL}, t_{TLH}			0.45	3.50	0.45	1.50	3.50	0.45	3.50	ns
Setup Time	t_{SU}	$A_n, B_n\rightarrow\overline{E}$		7.00	—	7.40	—	—	8.20	—	ns
		$S_n\rightarrow\overline{E}$		8.00	—	8.00	—	—	8.30	—	
		$\overline{C_n}\rightarrow\overline{E}$		5.00	—	5.20	—	—	6.20	—	
Hold Time	t_h	$A_n, B_n\rightarrow\overline{E}$		0.00	—	0.00	—	—	0.00	—	ns
		$S_n\rightarrow\overline{E}$		0.50	—	0.50	—	—	0.30	—	
		$\overline{C_n}\rightarrow\overline{E}$		0.50	—	0.50	—	—	0.20	—	
Pulse Width	$t_{W(L)}$	$\overline{E}$		2.00	—	2.00	—	—	2.00	—	ns

Note) The circuit in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

9-bit Wallace Tree Adder

The HD100182 is a 9-bit Wallace tree adder. It is designed to assist in performing high-speed hardware multiplication.

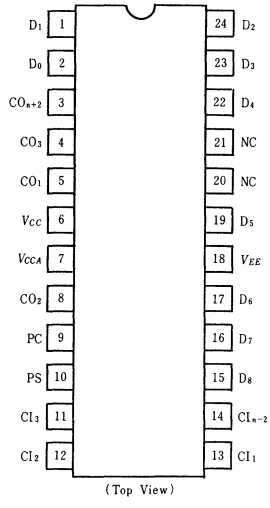
The device is designed to add 9-bits of data 1-bit-slice wide and handle the carry-ins from the previous slices.

The HD100182 is easily expanded and still maintains four levels of delay regardless of input string length.

In conjunction with the HD100183 Recode Multiplier, the HD100179 Carry Lookahead, and the HD100180 High-speed Adder, the HD100182 assists in performing parallel multiplication of two signed numbers to produce a signed two's complement product.

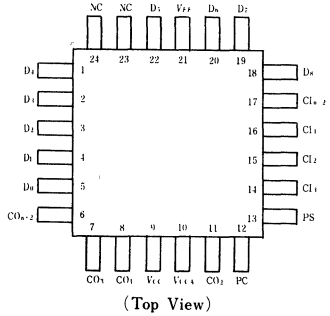
■PIN ARRANGEMENT

● HD100182



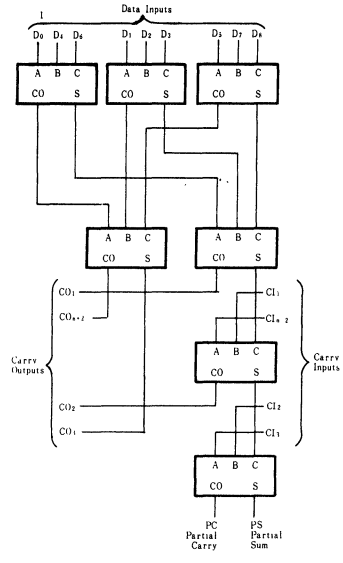
(Top View)

● HD100182F

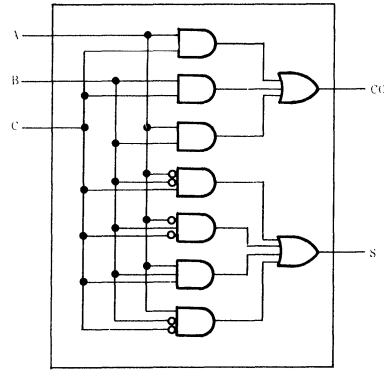


(Top View)

■LOGIC DIAGRAM



● Adder Logic Diagram



● Adder Truth Table

Inputs			Outputs	
A	B	C	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		125	180	260	mA
Input Current	I_{IH}	V_{IN} = $V_{IH\ max}$	CI_1~CI_3, CI_{n-2}, D_1, D_3~D_6, D_8	—	—	300	μA
			D_0, D_2, D_7	—	—	250	μA

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100182

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	D_n→CO_{n+2}	1.20	4.30	1.40	2.15	4.50	1.50	4.50	ns
			D_n→CO_1	1.20	4.50	1.30	2.20	4.70	1.40	4.70	
			D_n→CO_2	2.00	5.80	2.20	3.00	6.10	2.30	6.10	
			D_n→CO_3	1.30	4.50	1.40	2.10	4.70	1.50	4.70	
			D_n→PC, PS	2.30	7.00	2.50	3.80	7.20	2.60	7.20	
			CI_{n-2}, CI_1→CO_2	0.90	3.20	1.00	1.50	3.40	1.10	3.40	
			CI_{n-2}, CI_1→PC, PS	1.40	4.20	1.50	2.15	4.45	1.60	4.45	
			CI_2, CI_3→PC, PS	0.80	3.00	0.80	1.45	3.20	0.90	3.20	
Transition Time	t_{TLH} t_{THL}			0.45	1.60	0.45	0.75	1.60	0.45	1.60	ns

● HD100182F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	D_n→CO_{n+2}	1.20	4.10	1.40	2.10	4.30	1.50	4.30	ns
			D_n→CO_1	1.20	4.20	1.30	2.10	4.50	1.40	4.50	
			D_n→CO_2	2.10	5.60	2.20	2.90	5.90	2.30	5.90	
			D_n→CO_3	1.30	4.30	1.40	2.00	4.50	1.50	4.50	
			D_n→PC, PS	2.40	6.80	2.50	3.70	7.00	2.60	7.00	
			CI_{n-2}, CI_1→CO_2	0.90	3.00	1.00	1.40	3.20	1.10	3.20	
			CI_{n-2}, CI_1→PC, PS	1.40	4.00	1.50	2.05	4.25	1.60	4.25	
			CI_2, CI_3→PC, PS	0.70	2.80	0.80	1.35	3.00	0.90	3.00	
Transition Time	t_{TLH} t_{THL}			0.45	1.50	0.45	0.70	1.50	0.45	1.50	ns

Note) The circuit in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

HD100183/F

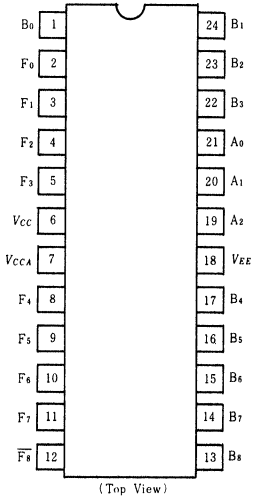
2 × 8-bit Recode Multiplier

The HD100183 is a 2 x 8-bit recode multiplier designed to perform high-speed hardware multiplication.

In conjuction with the HD100182 Wallace Tree Adder, the HD100179 Carry Lookahead, and the HD100180 High-speed Adder, the HD100183 performs parallel multiplication of two signed numbers in two's complement form to produce a signed two's complement product.

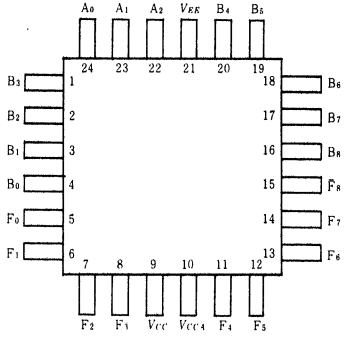
■PIN ARRANGEMENT

● HD100183



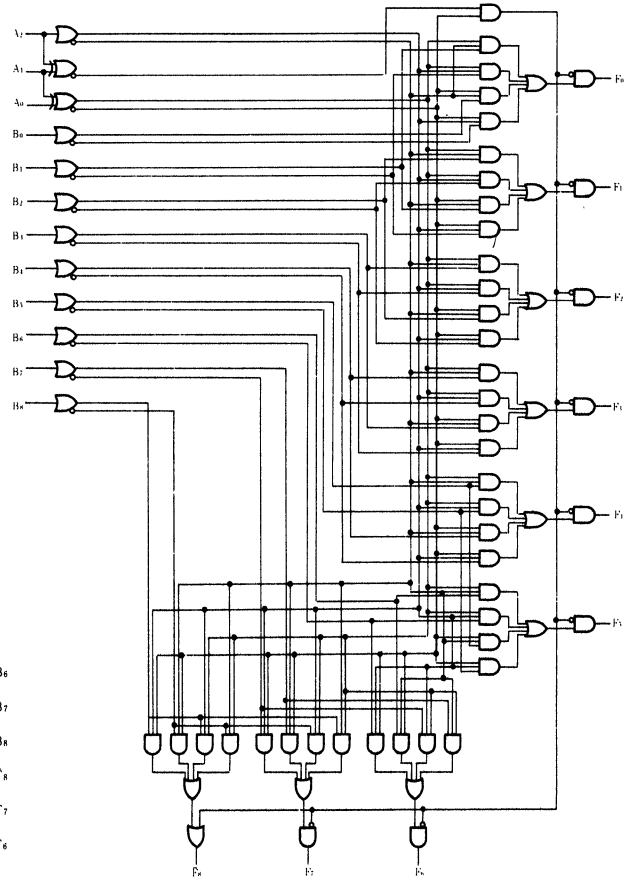
(Top View)

● HD100183F



(Top View)

■LOGIC DIAGRAM



■TRUTH TABLE

Inputs			Recode Mode	Outputs								
A_0	A_1	A_2		F_0	F_1	F_2	F_3	F_4	F_5	F_6	F_7	$\overline{F_8}$
L	L	L	0	L	L	L	L	L	L	L	L	H
H	L	L	+1	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	$\overline{B_8}$
L	H	L	+1	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	$\overline{B_8}$
H	H	L	+2	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	$\overline{B_8}$
L	L	H	−2	$\overline{B_0}$	$\overline{B_1}$	$\overline{B_2}$	$\overline{B_3}$	$\overline{B_4}$	$\overline{B_5}$	$\overline{B_6}$	$\overline{B_7}$	B_8
H	L	H	−1	$\overline{B_1}$	$\overline{B_2}$	$\overline{B_3}$	$\overline{B_4}$	$\overline{B_5}$	$\overline{B_6}$	$\overline{B_7}$	$\overline{B_8}$	B_8
L	H	H	−1	$\overline{B_1}$	$\overline{B_2}$	$\overline{B_3}$	$\overline{B_4}$	$\overline{B_5}$	$\overline{B_6}$	$\overline{B_7}$	$\overline{B_8}$	B_8
H	H	H	0	L	L	L	L	L	L	L	L	H

■DC CHARACTERISTICS (V_{EE} = −4.2 to −4.8V, V_{CC} = V_{CCA} = GND, Ta = 0 to +85℃)

Item	Symbol	Test Conditions		min	typ	max	Unit
Supply Current	I_{EE}	All inputs open		115	170	250	mA
Input Current	I_{IH}	$V_{IN} = V_{IH\ max}$	B_0 ~ B_8	—	—	215	μA
			A_0	—	—	215	
			A_1	—	—	285	
			A_2	—		310	

Notes) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS (V_{EE} = −2.2 to −2.8V, V_{CC} = V_{CCA} = 2.0V)

● HD100183

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	A_0 ~ A_2 → F_0 ~ F_7	1.10	3.90	1.10	2.20	3.80	1.10	4.20	ns
			A_0 ~ A_2 → $\overline{F_8}$	0.90	3.20	1.00	1.60	3.10	1.00	3.60	
			B_0 ~ B_8 → F_0 ~ F_7	0.80	2.20	0.90	1.40	2.15	0.90	2.50	
			B_8 → $\overline{F_8}$	0.80	2.00	0.90	1.30	2.00	0.90	2.50	
Transition Time	t_{TLH} t_{THL}			0.35	2.50	0.35	0.75	2.40	0.35	2.60	ns

● HD100183F

Item	Symbol	Test Condition		0℃		25℃			85℃		Unit
				min	max	min	typ	max	min	max	
Propagation Delay Time	t_{PLH} t_{PHL}	See test circuit and waveform	A_0 ~ A_2 → F_0 ~ F_7	1.10	3.70	1.10	2.20	3.60	1.10	4.00	ns
			A_0 ~ A_2 → $\overline{F_8}$	0.90	3.00	1.00	1.60	2.90	1.00	3.40	
			B_0 ~ B_8 → F_0 ~ F_7	0.80	2.00	0.90	1.40	1.95	0.90	2.30	
			B_8 → $\overline{F_8}$	0.80	1.80	0.90	1.30	1.80	0.90	2.30	
Transition Time	t_{TLH} t_{THL}			0.35	2.40	0.35	0.75	2.30	0.35	2.50	ns

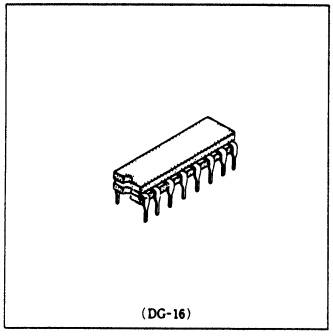
Note) The circuit in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

ECL Memories

256-word × 1-bit Fully Decoded Random Access Memory

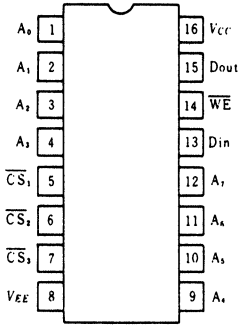
The HM10414 is ECL 10K compatible, 256-word x 1-bit, read write, random access memory developed for high speed systems such as scratch pad and control/buffer storages.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10414 is encapsulated in cerdip-16pin package, compatible with Fairchild's F10414.

- Fully compatible with 10K ECL level
- Address access time: HM10414: 10ns (max.)
  HM10414-1: 8ns (max.)
- Write pulse width: 6ns (min.)
- Three chip select pins
- Output obtainable by wired-OR (open emitter)



(DG-16)

■ PIN ARRANGEMENT



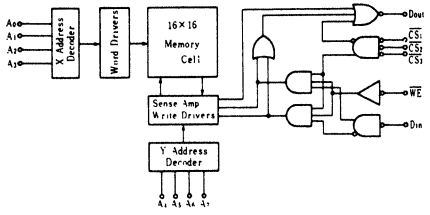
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
any one H	×	×	L	Not Selected
all L	L	L	L	Write "0"
all L	L	H	L	Write "1"
all L	H	×	Dout *	Read

× : Don't care
* : Read out non-inverted

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE}=-5.2V$, $R_L=50\Omega$ to $-2.0V$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	−	−840	mV
			+25°C	−960	−	−810	
			+75°C	−900	−	−720	
	V_{OL}		0°C	−1870	−	−1665	
			+25°C	−1850	−	−1650	
			+75°C	−1830	−	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	−	−	mV
			+25°C	−980	−	−	
			+75°C	−920	−	−	
	V_{OLC}		0°C	−	−	−1645	
			+25°C	−	−	−1630	
			+75°C	−	−	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	−	−840	mV
			+25°C	−1105	−	−810	
			+75°C	−1045	−	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	−	−1490	
			+25°C	−1850	−	−1475	
			+75°C	−1830	−	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$	0 to +75°C	−	−	220	μA
	I_{IL}	$\overline{CS}$ / $V_{IN}=V_{ILB}$	0 to +75°C	0.5	−	170	
		Other		−50	−	−	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 8	+75°C	−	−130	−	mA
			0°C	−180	−140	−	

● AC CHARACTERISTICS

($V_{EE}=-5.2V\pm5\%$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM10414			HM10414-1			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACR}		−	3	6	−	3	6	ns
Chip Select Recovery Time	t_{RCS}		−	3	6	−	3	6	ns
Address Access Time	t_{AA}		−	7	10	−	6	8	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	$t_{WSA}=2ns$	6	4	−	ns
Data Setup Time	t_{WSD}		1	0	−	ns
Data Hold Time	t_{WHD}		1	0	−	ns
Address Setup Time	t_{WSA}	$t_W=6ns$	2	0	−	ns
Address Hold Time	t_{WHA}		2	0	−	ns
Chip Select Setup Time	t_{WSCS}		1	0	−	ns
Chip Select Hold Time	t_{WHCS}		1	0	−	ns
Write Disable Time	t_{WS}		−	−	5	ns
Write Recovery Time	t_{WR}		−	−	5	ns

3. RISE/FALL TIME

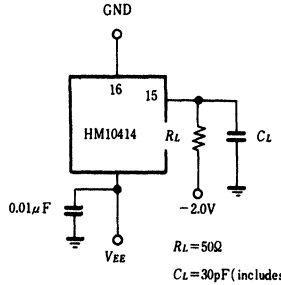
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		−	1.5	2.5	ns
Output Fall Time	t_f		−	1.5	2.5	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		−	3	5	pF
Output Capacitance	C_{out}		−	5	8	pF

■ TEST CIRCUIT AND WAVEFORMS

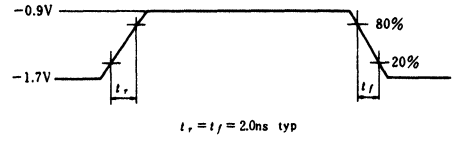
1. LOADING CONDITIONS



R_L=50Ω

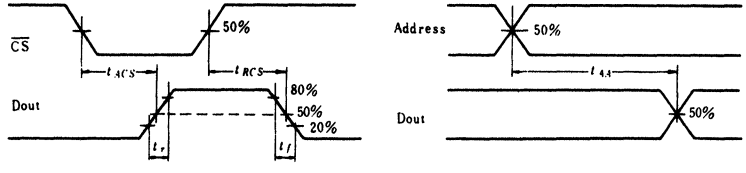
C_L=30pF(includes jig and stray capacitance)

2. INPUT PULSE

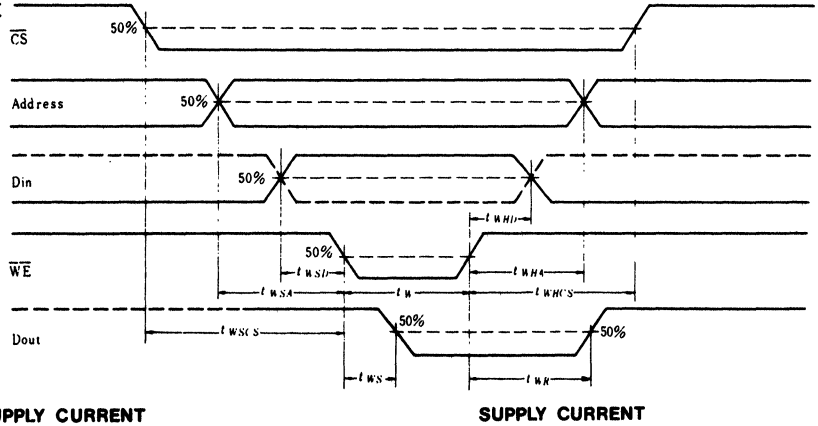


$t_r = t_f$ = 2.0ns typ

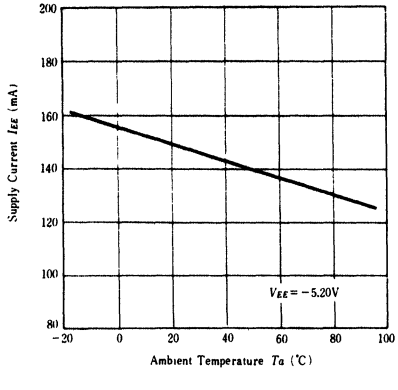
3. READ MODE



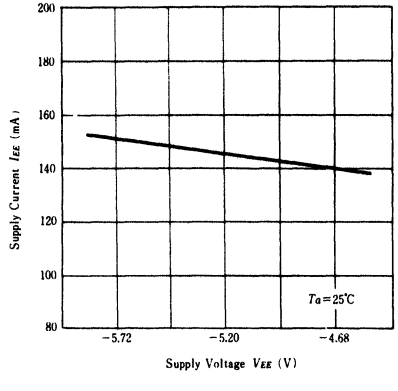
4. WRITE MODE



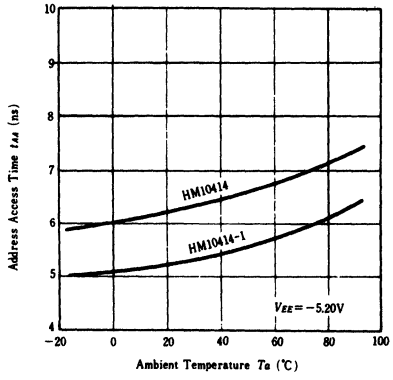
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



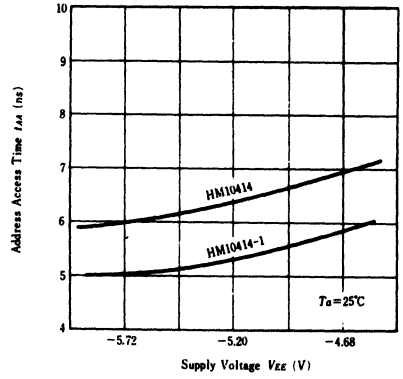
SUPPLY CURRENT vs. SUPPLY VOLTAGE



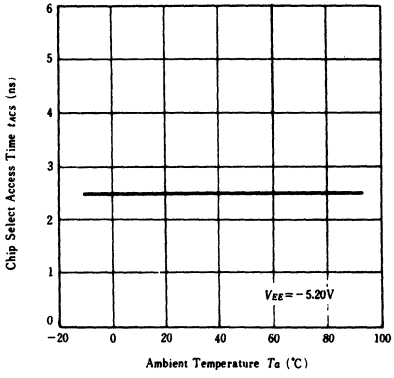
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



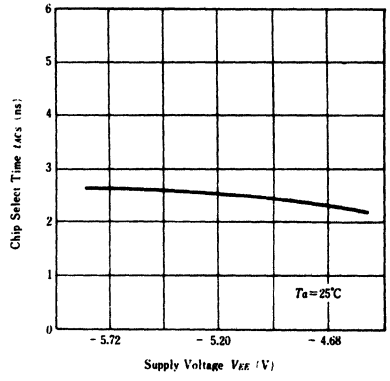
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



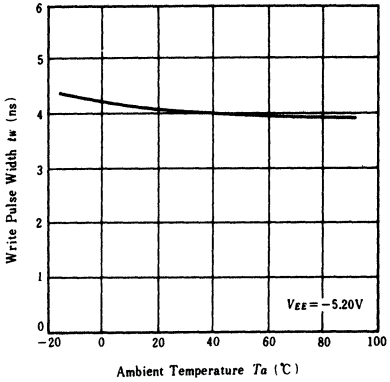
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



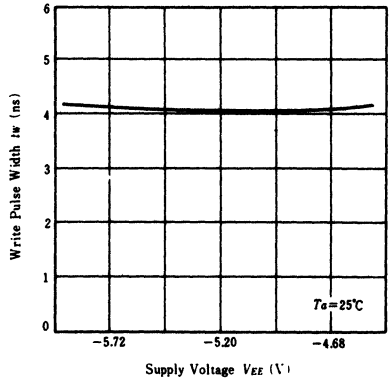
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE

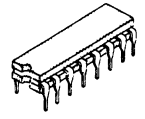


HM2110, HM2110-1

1024-word × 1-bit Fully Decoded Random Access Memory

The HM2110 Series item is an ECL compatible, 1024-word x 1-bit, read/write, random access memory developed for application to scratch pads, control and buffer memories, etc. which require high speeds.

- It is compatible with 10K ECL logic.
- Chip select access time .....10ns (max.)
- Address access time ..... HM2110: 35ns (max.)
  HM2110-1: 25ns (max.)
- Power consumption .....0.5mW/bit (typ)
- Output obtainable by Wired-OR (open emitter).



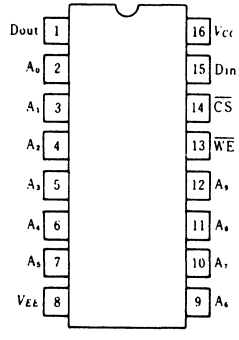
DG - 16A

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

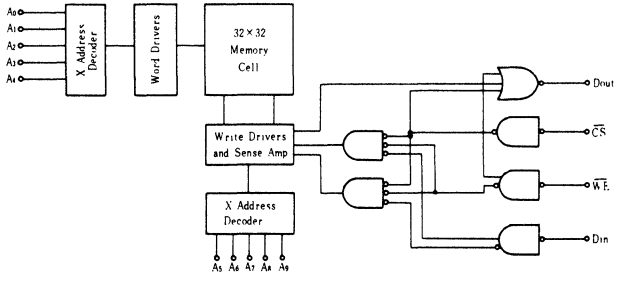
× : irrelevant
* : Read out noninverted

■ PIN ARRANGEMENT



Top View

■ BLOCK DIAGRAM



■ ABSOLUTE MAXMUM RATINGS

Item	Symbol	HM2110 Series	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

HITACHI

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS ($V_{EE}=-5.2V$, $R_L=50\Omega$ to $-2.0V$, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / $V_{IN}=V_{ILB}$	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 8	$0\leqq Ta<25°C$	−150	−100	—	mA
			$Ta\geqq 25°C$	−125	−90	—	

●AC CHARACTERISTICS

($V_{EE}=-5.2V$ ±5%, $Ta=0$ to $+75°C$, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM2110			HM2110-1			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	7	10	—	7	10	ns
Chip Select Recovery Time	t_{RCS}		—	7	10	—	7	10	ns
Address Access Time	t_{AA}		—	20	35	—	15	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM2110			HM2110-1			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	$t_{WSA}=8ns$	25	—	—	25	—	—	ns
Data Setup Time	t_{WSD}		5	—	—	5	—	—	ns
Data Hold Time	t_{WHD}		5	—	—	5	—	—	ns
Address Setup Time	t_{WSA}	$t_W=25ns$	8	—	—	8	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		5	—	—	5	—	—	ns
Chip Select Hold Time	t_{WHCS}		5	—	—	5	—	—	ns
Write Disable Time	t_{WS}		—	—	10	—	—	10	ns
Write Recovery Time	t_{WR}		—	—	10	—	—	10	ns

3. RISE/FALL TIME

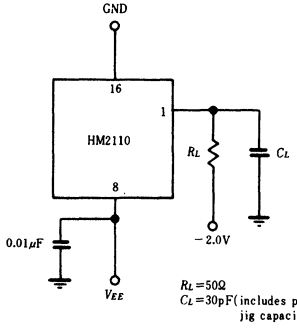
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	5	—	ns
Output Fall Time	t_f		—	5	—	ns

4. CAPACITANCE

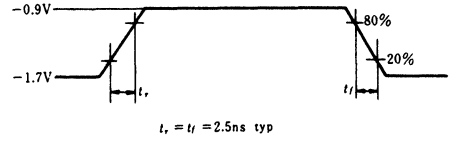
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	5	pF
Output Capacitance	C_{out}		—	7	8	pF

■ TEST CIRCUIT AND WAVEFORMS

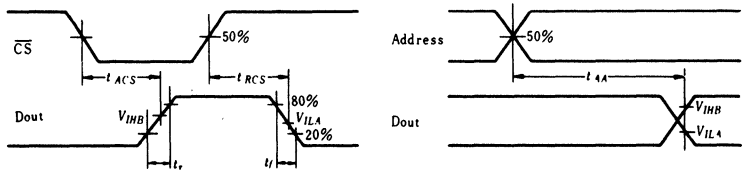
1. LOADING CONDITION



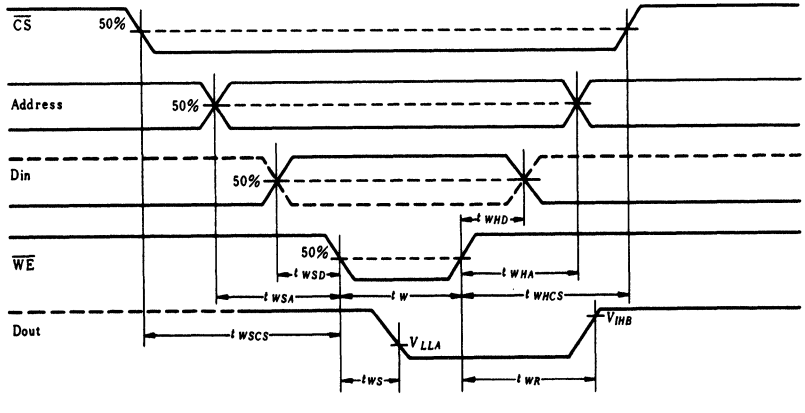
2. INPUT PULSE



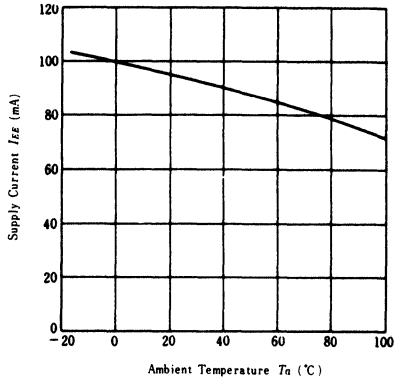
3. READ MODE



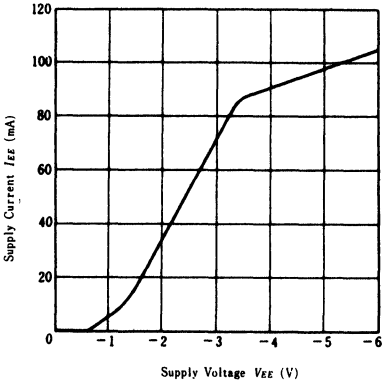
4. WRITE MODE



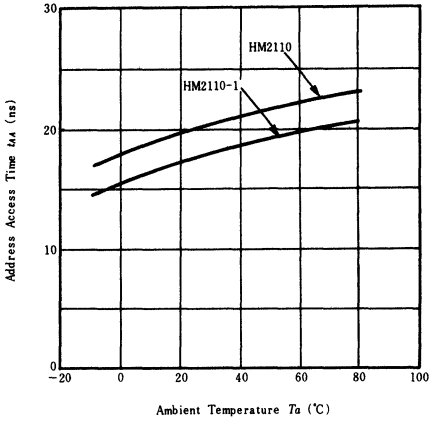
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



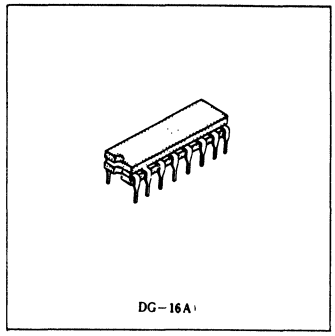
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



HM2112, HM2112-1

1024-word×1-bit Fully Decoded Random Access Memory

The HM2112 is an ECL compatible, 1024-word x 1-bit, read/write, random access memory developed for application to scratch pads, control and buffer memories, etc. which require high speeds.



■FEATURES

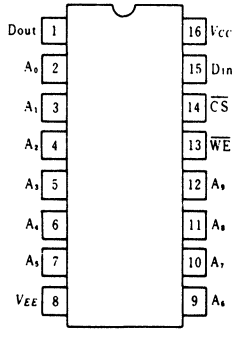
- Level ..... 10k ECL Compatible
- Construction ..... 1024-word by 1-bit
- Address Access Time ..... HM2112 10ns (max.)
  HM2112-1 8ns (max.)
- Chip Select Access Time ..... 5ns (max.)
- Power Consumption ..... 0.8mW/bit (typ)
- Output Obtainable by Wired-OR (open emitter)
- Fully Pin Compatible with F10415

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

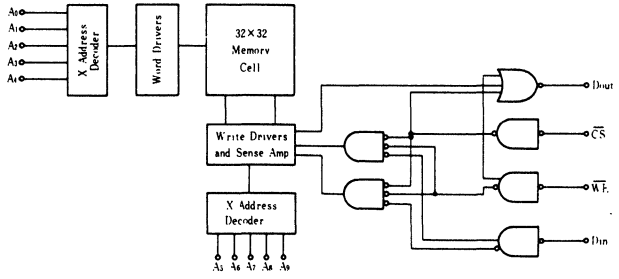
× : Irrelevant
* : Read out noniverted

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM2112	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

(V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

●DC CHARACTERISTICS

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IL}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / $V_{IN}=V_{ILB}$	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 8	Ta=0°C	−200	—	—	mA
			Ta=75°C	−170	—	—	

●AC CHARACTERISTICS

(V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM2112-1			HM2112			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		1	3	5	1	3	5	ns
Chip Select Recovery Time	t_{RCS}		1	3	5	1	3	5	ns
Address Access Time	t_{AA}		3	6.5	8	3	7.5	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM2112-1			HM2112			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA}=3ns	6	2	—	6	2	—	ns
Data Setup Time	t_{WSD}		1	0	—	1	0	—	ns
Data Hold Time	t_{WHD}		1	0	—	1	0	—	ns
Address Setup Time	t_{WSA}	t_W=6ns	3	0	—	3	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	2	0	—	ns
Chip Select Setup Time	t_{WSCS}		1	0	—	1	0	—	ns
Chip Select Hold Time	t_{WHCS}		1	0	—	1	0	—	ns
Write Disable Time	t_{WS}		1	3	5	1	3	5	ns
Write Recovery Time	t_{WR}		1	3	5	1	3	5	ns

3. RISE/FALL TIME

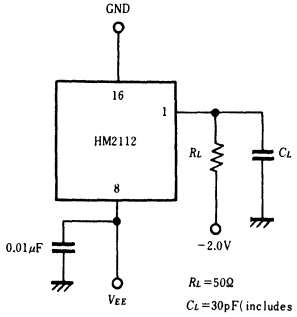
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		0.8	1.5	2.5	ns
Output Fall Time	t_f		0.8	1.5	2.5	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		1	3	5	pF
Output Capacitance	C_{out}		3	5	8	pF

■TEST CIRCUIT AND WAVEFORMS

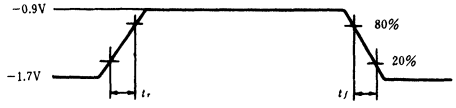
1. LOADING CONDITION



R_L=50Ω

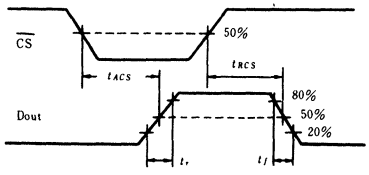
C_L=30pF(includes probe and jig capacitance)

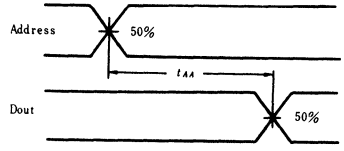
2. INPUT PULSE



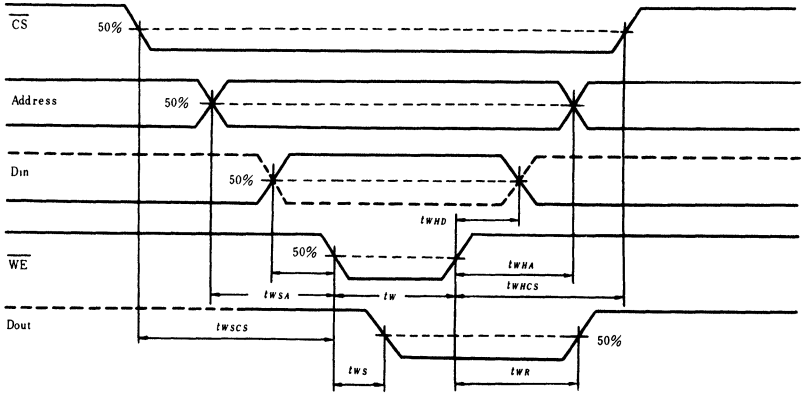
$t_r = t_f$=2.0ns typ

3. READ MODE

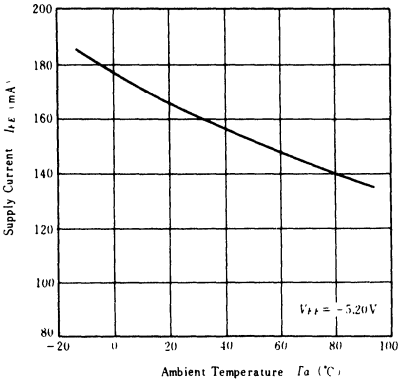




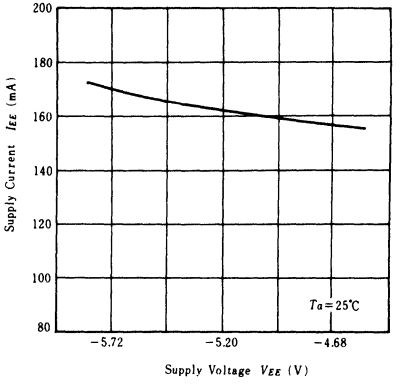
4. WRITE MODE



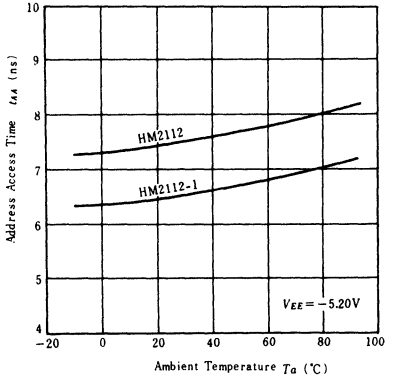
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



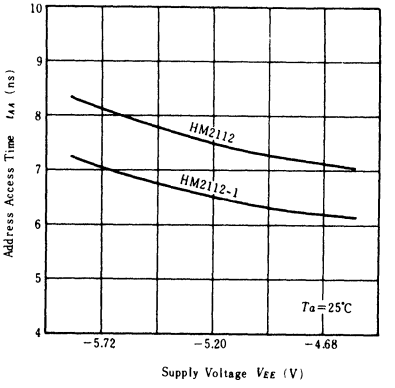
SUPPLY CURRENT vs. SUPPLY VOLTAGE



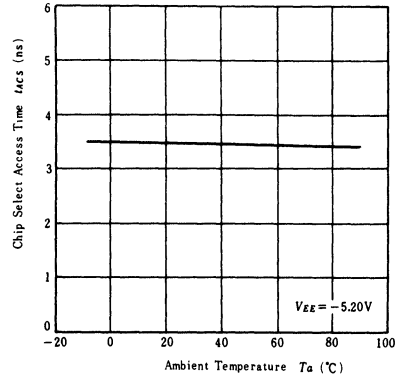
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



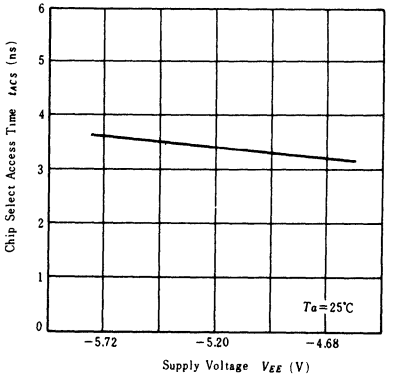
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



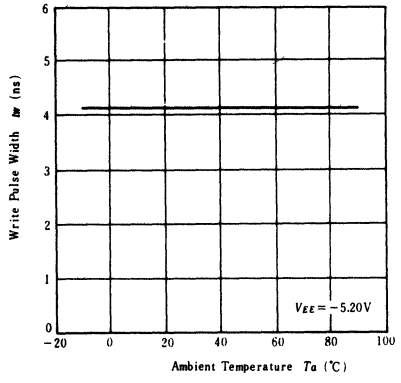
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



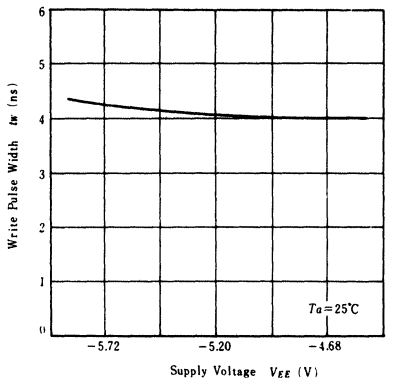
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



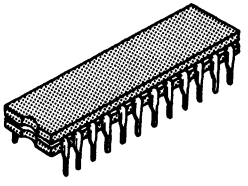
WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



HM10422

256-word×4-bit Fully Decoded Random Access Memory

The HM10422 is ECL 10K compatible, 256-word x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control buffer storages.
Four active Low Block Select lines are provided to select each block independently.
The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10422 is encapsulated in cerdip-24 pin package, compatible with Fairchild's F10422.



(DG-24A)

■ FEATURES

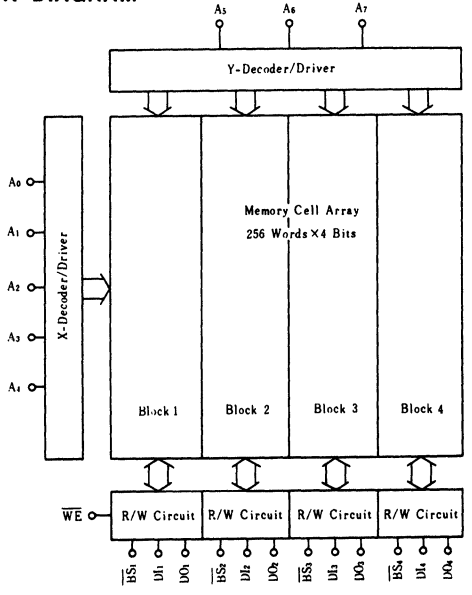
- 256-word x 4 bit organization.
- Fully compatible with 10K ECL level
- Address access time: 10ns (max)
- Write pulse width: 6ns (min)
- Power dissipation: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

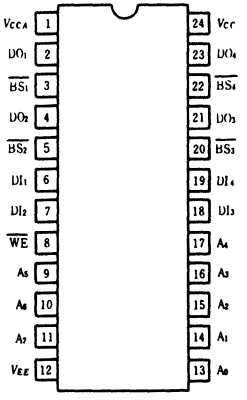
Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read out noninvert

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

(V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

● DC CHARACTERISTICS

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{BS}$	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	Ta=0°C	−200	−160	—	mA
			Ta=75°C	—	−145	—	

● AC CHARACTERISTICS

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	t_{ABS}		—	—	5	ns
Block Select Recovery Time	t_{RBS}		—	—	5	ns
Address Access Time	t_{AA}		—	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA}=2ns	6	4.5	—	ns
Data Setup Time	t_{WSD}		2	0	—	ns
Data Hold Time	t_{WHD}		2	0	—	ns
Address Setup Time	t_{WSA}	t_W=6ns	2	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Block Select Setup Time	t_{WSBS}		2	0	—	ns
Block Select Hold Time	t_{WHBS}		2	0	—	ns
Write Disable Time	t_{WS}		—	4	5	ns
Write Recovery Time	t_{WR}		—	4.5	9	ns

3. RISE/FALL TIME

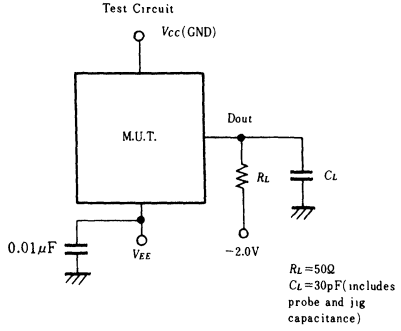
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

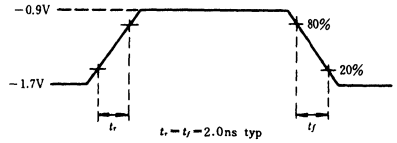
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

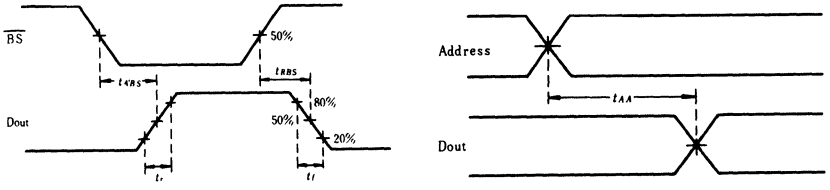
1. LOADING CONDITION



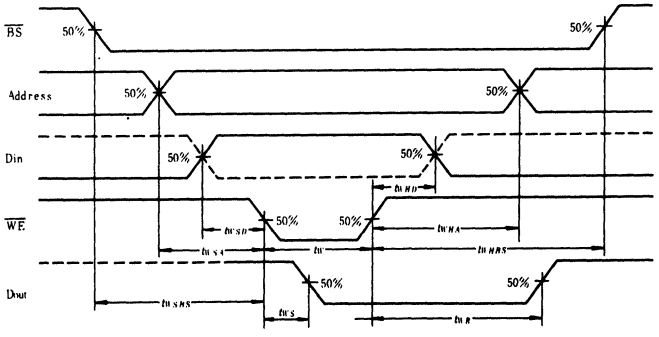
2. INPUT PULSE



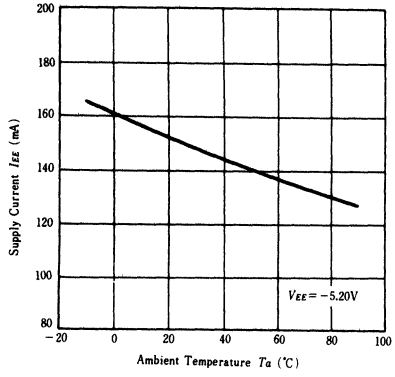
3. READ MODE



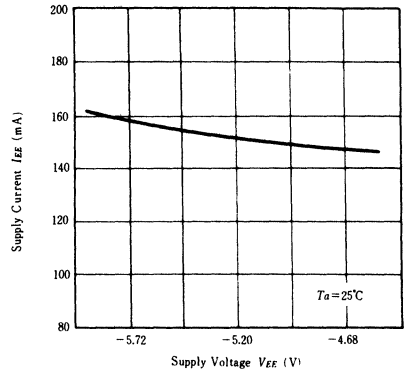
4. WRITE MODE



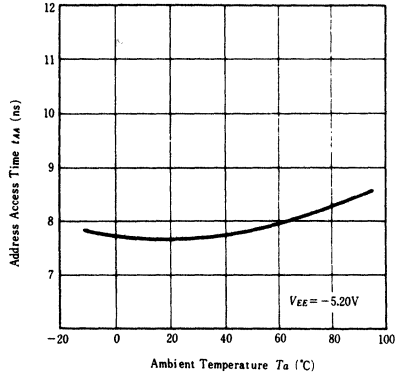
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



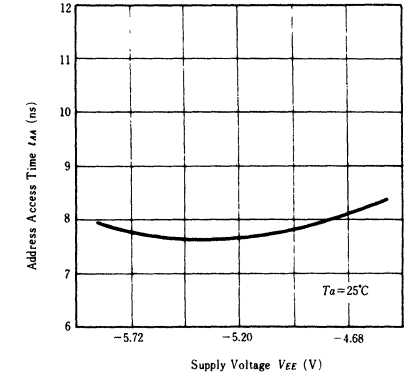
SUPPLY CURRENT vs. SUPPLY VOLTAGE



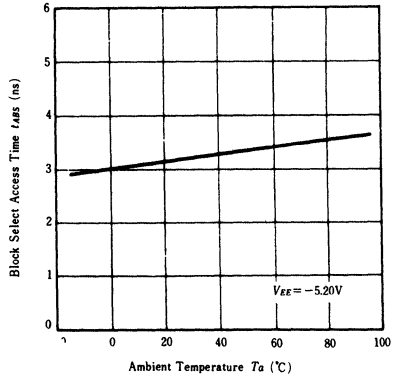
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



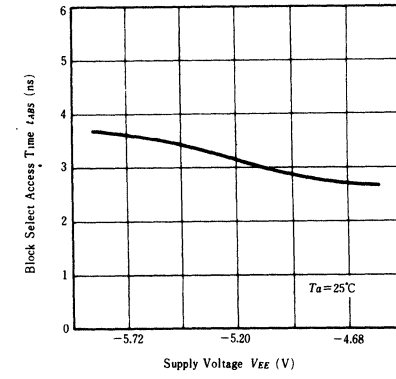
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



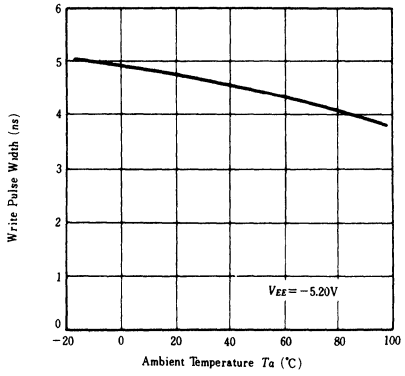
BLOCK SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



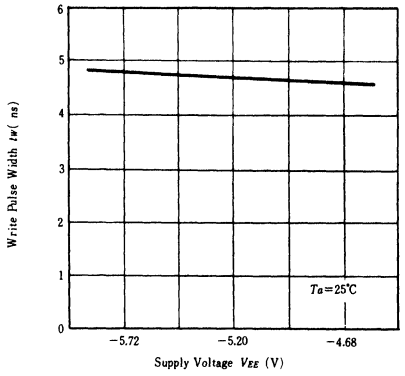
BLOCK SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



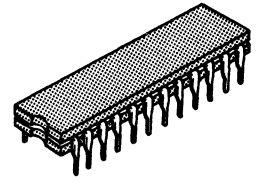
WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



HM10422-7

256-word × 4-bit Fully Decoded Random Access Memory

The HM10422 is ECL 10K compatible, 256-word x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control buffer storages.
Four active Low Block Select lines are provided to select each block independently.
The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10422 is encapsulated in cerdip-24 pin package, compatible with Fairchild's F10422.

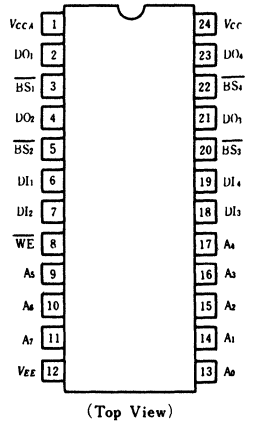


(DG-24A)

■ FEATURES

- 256-word x 4 bit organization
- Fully compatible with 10K ECL level
- Address access time: 7ns (max)
- Write pulse width: 4ns (min)
- Power dissipation: 1.0 mW/bit
- Output obtainable by wired-OR (open emitter)

■ PIN ARRANGEMENT



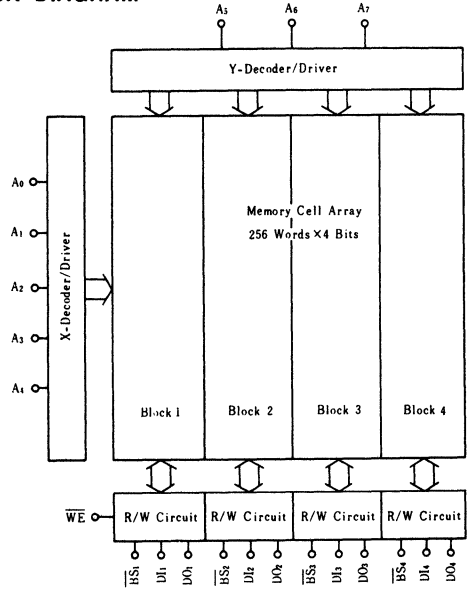
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read out noninvert

■ BLOCK DIAGRAM



HITACHI

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

(V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

●DC CHARACTERISTICS

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{BS}$	0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	Ta = 0°C	−240	−200	—	mA
			Ta = 75°C	—	−180	—	

●AC CHARACTERISTICS

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	t_{ABS}		—	—	5	ns
Block Select Recovery Time	t_{RBS}		—	—	5	ns
Address Access Time	t_{AA}		—	4	7	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 2ns	4	3	—	ns
Data Setup Time	t_{WSD}		1		—	ns
Data Hold Time	t_{WHD}		1		—	ns
Address Setup Time	t_{WSA}	t_W = 4ns	2		—	ns
Address Hold Time	t_{WHA}		1		—	ns
Block Select Setup Time	t_{WSBS}		1		—	ns
Block Select Hold Time	t_{WHBS}		1		—	ns
Write Disable Time	t_{WS}		—	3	5	ns
Write Recovery Time	t_{WR}		—	3	5	ns

3. RISE/FALL TIME

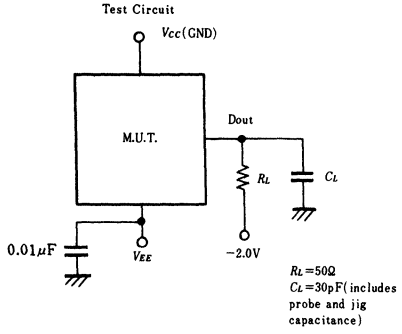
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

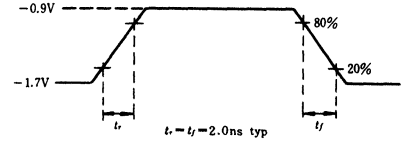
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■TEST CIRCUIT AND WAVEFORMS

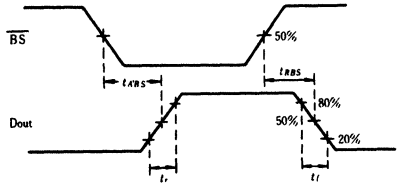
1. LOADING CONDITION

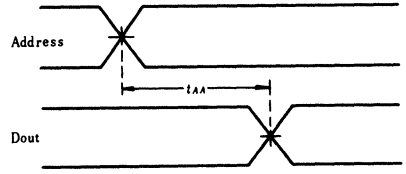


2. INPUT PULSE

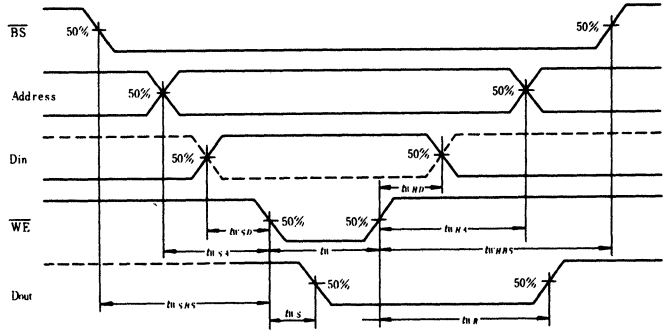


3. READ MODE





4. WRITE MODE

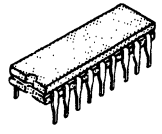


HM10470, HM10470-1

4096-word x 1-bit Fully Decoded Random Access Memory

The HM10470 is ECL 10K compatible, 4096-words x 1-bit, read write random access memory developed for high speed systems such as scratch pads and control/buffer storages.
The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10470 is encapsulated in cerdip-18 pin compatible with Fairchild's F10470.

HM10470, HM10470-1



(DG-18)

■ FEATURES

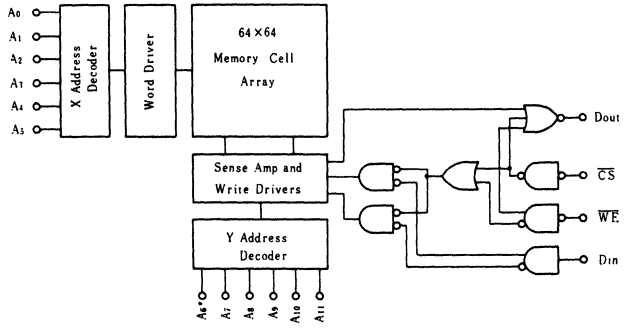
- 4096-word x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: HM10740 25ns (max)
  HM10470-1 15ns (max)
- Write pulse width: HM10470 25ns (min)
  HM10470-1 15ns (min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

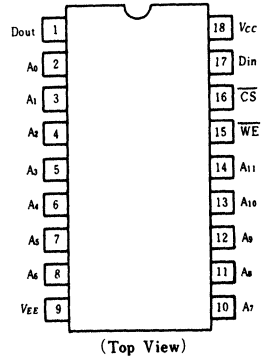
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Noninvert

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ TEST CIRCUIT AND WAVEFORMS

● DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{IN}=V_{IHA}$ or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{IHB}$ or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	$V_{IN}=V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / $V_{IN}=V_{ILB}$	0 to +75°C	0.5	—	170	
		Other / $V_{IN}=V_{ILB}$	0 to +75°C	−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 9	Ta=0°C	−200*	−160*	—	mA
				−280**	−200**	—	
			Ta=75°C	—	−145	—	

* HM10470/F
** HM10470-1

● AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition	HM10470			HM10470-1			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	—	10	—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	—	—	8	ns
Address Access Time	t_{AA}		—	15	25	—	12	15	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM10470			HM10470-1			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA}=3ns	25	—	—	15	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	$t_W=t_{W\,min}$	3	—	—	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	10	—	—	8	ns
Write Recovery Time	t_{WR}		—	—	10	—	—	8	ns

3. RISE/FALL TIME

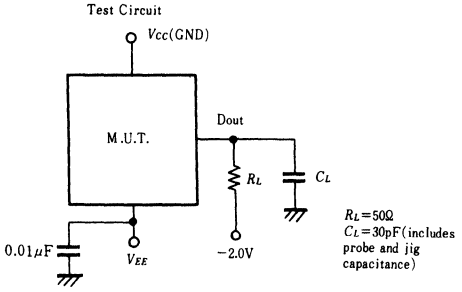
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

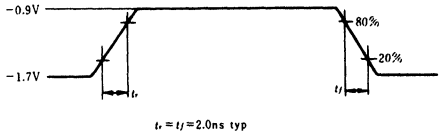
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

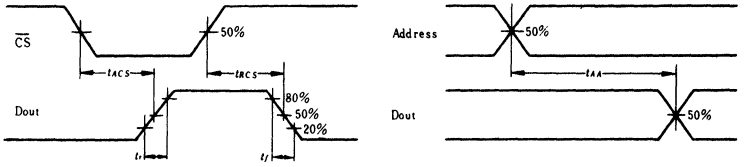
1. LOADING CONDITION



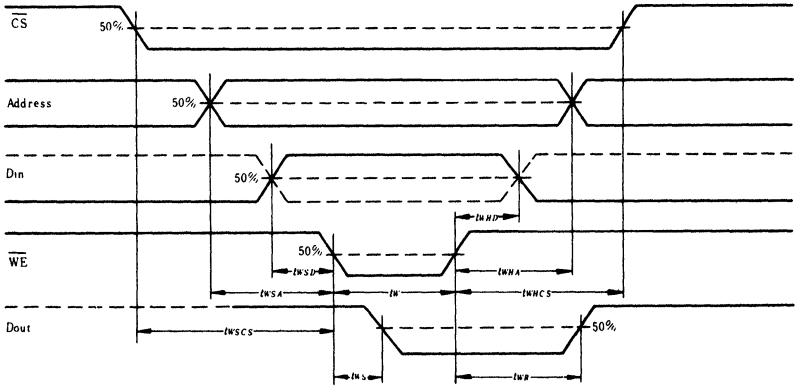
2. INPUT PULSE



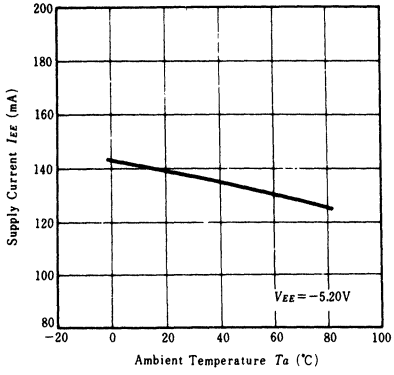
3. READ MODE



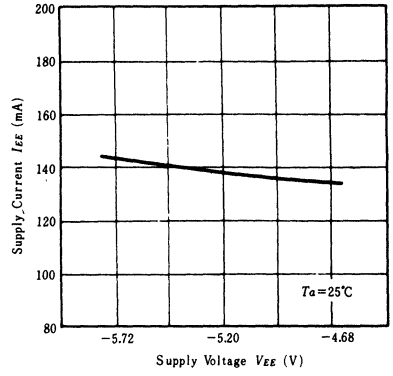
4. WRITE MODE



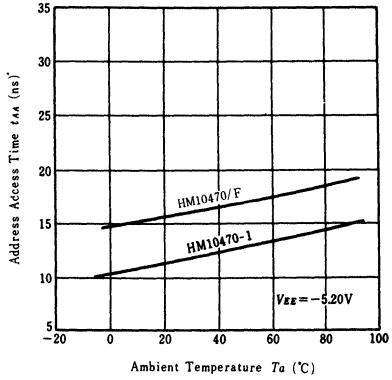
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



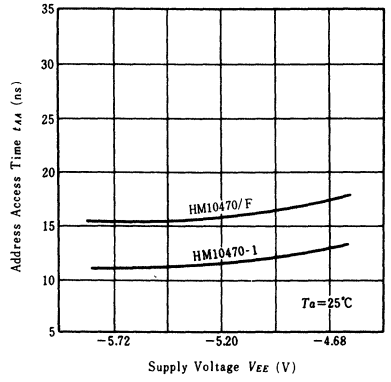
SUPPLY CURRENT vs. SUPPLY VOLTAGE



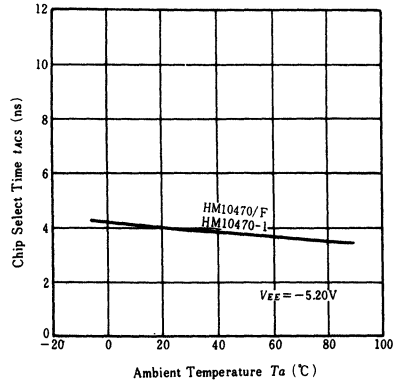
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



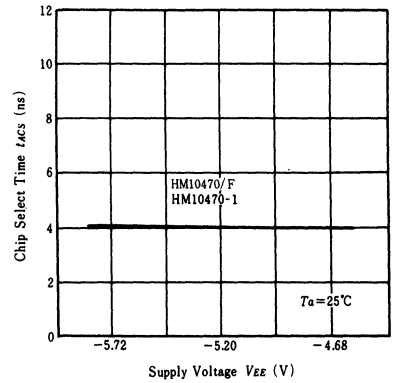
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



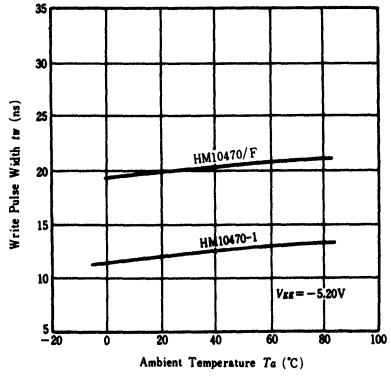
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



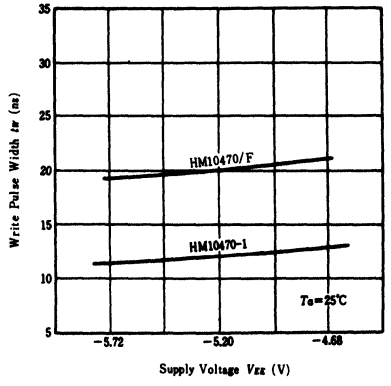
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



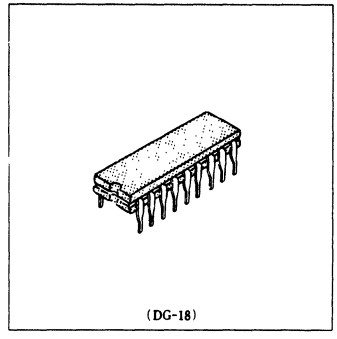
WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



HM10470-15

4096-word × 1-bit Fully Decoded Random Access Memory

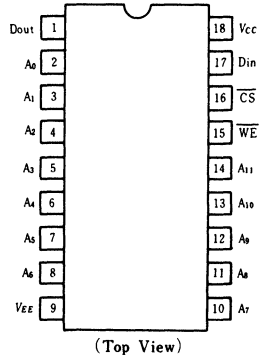
The HM10470 is ECL 10K compatible, 4096-words x 1-bit, read/write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10470 is encapsulated in cerdip-18 pin package, compatible with Fairchild's F10470.



■ FEATURES

- 4096-word x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: 15ns (max)
- Write pulse width: 15ns (min)
- Low power dissipation: 0.2 mW/bit
- Output obtainable by wired-OR (open emitter)

■ PIN ARRANGEMENT



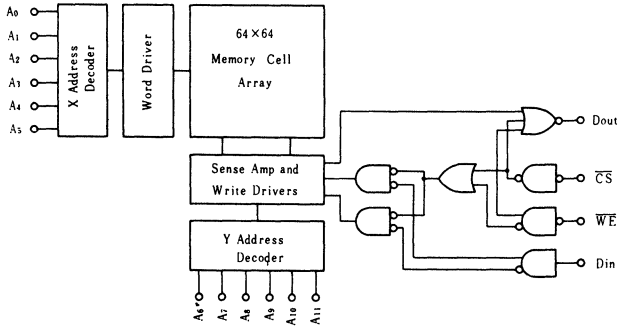
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout *	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	℃
Storage Temperature	T_{stg} (Bias)*	−55 to +125	℃

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$	V_{IN} = V_{ILB} 0 to +75°C	0.5	—	170	
		Other		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	Ta = 0°C	−200	−160	—	mA
			Ta = 75°C	—	−145	—	

●AC CHARACTERISTICS (V_{EE} = −5.2V±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	8	ns
Address Access Time	t_{AA}		—	—	15	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 3ns	15	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	ns
Address Setup Time	t_{WSA}	t_W = 15ns	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	ns
Write Disable Time	t_{WS}		—	—	8	ns
Write Recovery Time	t_{WR}		—	—	8	ns

3. RISE/FALL TIME

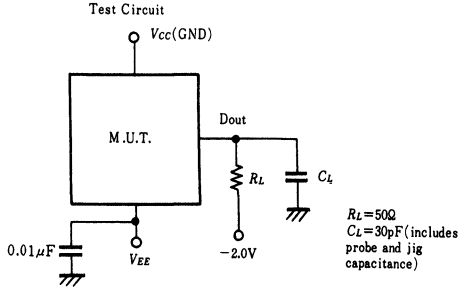
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

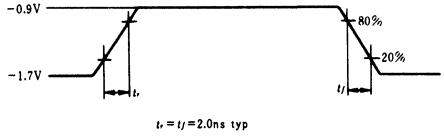
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

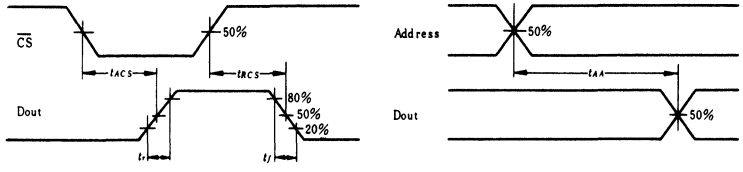
1. LOADING CONDITION



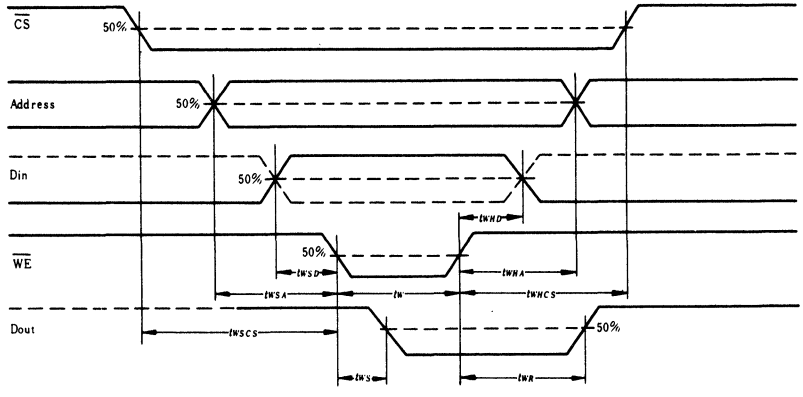
2. INPUT PULSE



3. READ MODE



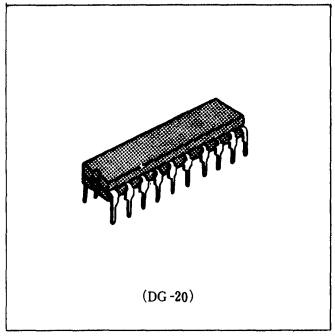
4. WRITE MODE



HM2142

4096-words × 1-bit Very High Speed Random Access Memory

The HM2142 is 4096-words x 1-bit very high speed read/write, random access memory developed for high speed systems such as pads and control/buffer storages.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM2142 is encapsulated in cerdip-20 pin package.



■ FEATURES

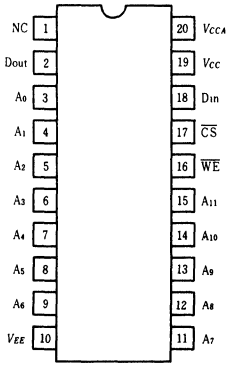
- 4096-words x 1 bit organization
- Very high speed address access time: 10ns (max)
- Write pulse width: 10ns (min)
- Power dissipation: 0.3 mW/bit
- Output obtainable by wired-OR

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout *	Read

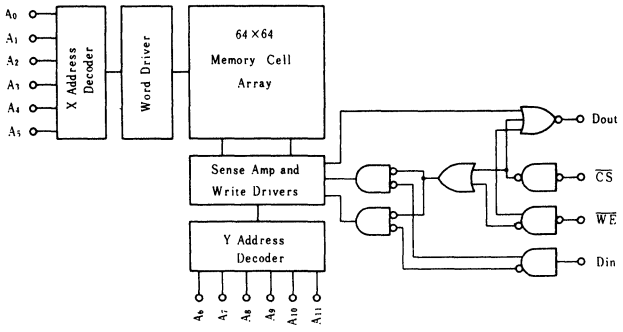
Notes) × : Irrelevant
* : Read Out Nonivert

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg} (Bias)*	−55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{EE}=−5.2V, R_L=50Ω to −2.0V, Ta=0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{IH}=V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−980	—	−810	
			+75°C	−950	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IH}=V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1165	—	−880	mV
			+25°C	−1165	—	−880	
			+75°C	−1165	—	−880	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1810	—	−1560	
			+25°C	−1810	—	−1560	
			+75°C	−1810	—	−1560	
Input Current	I_{IH}	V_{IN}=V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / V_{IN}=V_{ILB}	0 to +75°C	0.5	—	170	
		Others / V_{IN}=V_{ILB}	0 to +75°C	−50	—	—	
Supply Current	I_{EE}	All Input and Output Open.	Ta=0°C	−270	−240	—	mA
			Ta=75°C	—	−220	—	

● AC CHARACTERISTICS (V_{EE}=−5.2V±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	—	6	ns
Chip Select Recovery Time	t_{RCS}		—	—	6	ns
Address Access Time	t_{AA}		—	—	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA}=3ns	10	—	—	ns
Data Setup Time	t_{WSD}		1	—	—	ns
Data Hold Time	t_{WHD}		1	—	—	ns
Address Setup Time	t_{WSA}	t_W=10ns	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		1	—	—	ns
Chip Select Hold Time	t_{WHCS}		1	—	—	ns
Write Disable Time	t_{WS}		—	—	6	ns
Write Recovery Time	t_{WN}		—	—	6	ns

3. RISE/FALL TIME

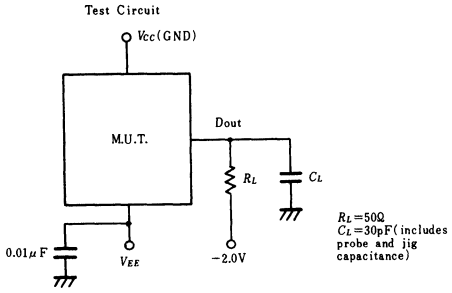
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

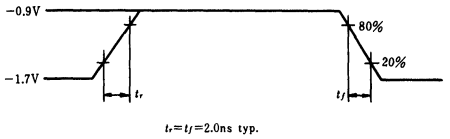
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

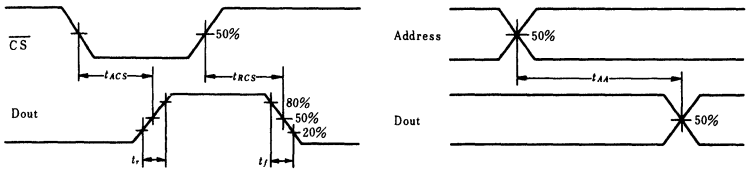
1. LOADING CONDITION



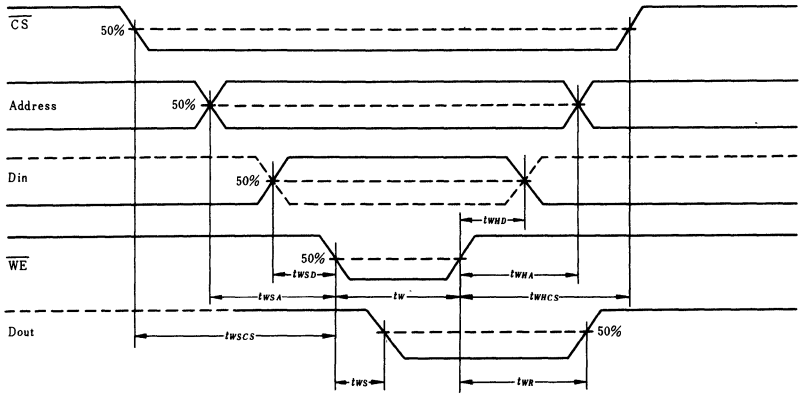
2. INPUT PULSE



3. READ MODE



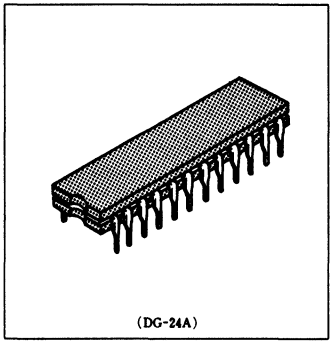
4. WRITE MODE



HM10474, HM10474-15

1024-word×4-bit Fully Decoded Random Access Memory

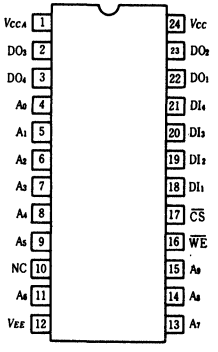
The HM10474 is ECL 10k compatible, 1024-words x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.
The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10474 is encapsulated in cerdip-24pin package, compatible with Fairchild's F10474.


(DG-24A)

■ FEATURES

- 1024-word x 4-bit organization
- Fully compatible with 10K ECL level
- Address access time: HM10474 25ns (max)
  HM10474-15 15ns (max)
- Write pulse width: HM10474 25ns(min)
  HM10474-15 15ns (min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)

■ PIN ARRANGEMENT



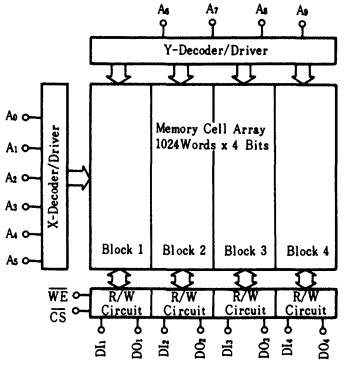
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

HITACHI

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$	0 to +75°C	0.5	—	170	
		Others		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	Ta = 0°C	−200	−160	—	mA
			Ta = 75°C	—	−145	—	

●AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM10474			HM10474-15			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	—	10	—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	—	—	8	ns
Address Access Time	t_{AA}		—	15	25	—	—	15	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM10474			HM10474-15			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA} = 3ns	25	15	—	15	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	t_W = $t_{W\,min}$	3	—	—	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	10	—	—	8	ns
Write Recovery Time	t_{WR}		—	—	10	—	—	8	ns

3. RISE/FALL TIME

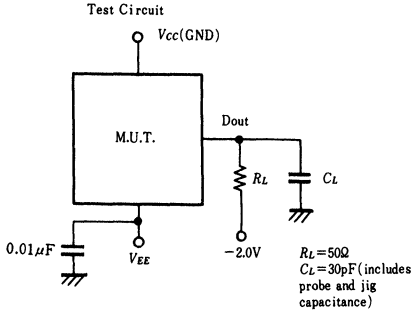
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

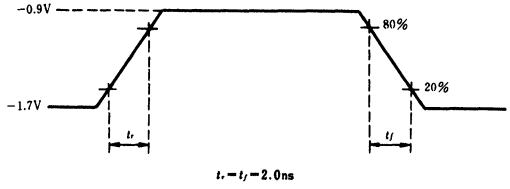
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

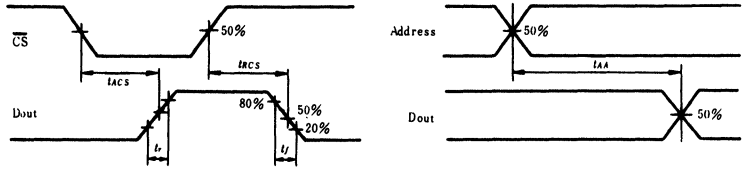
1. LOADING CONDITION



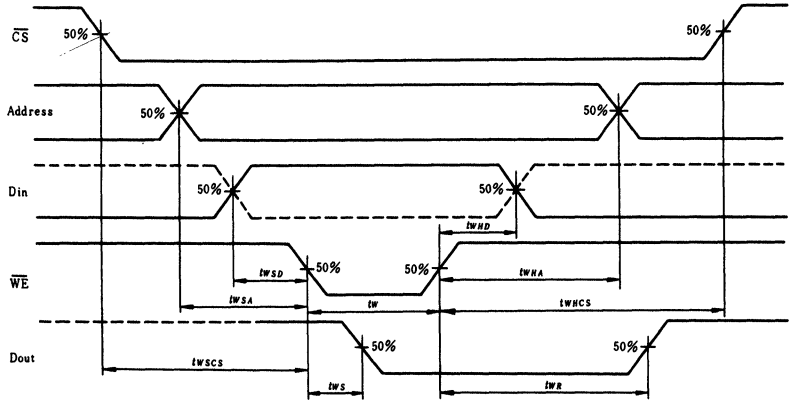
2. INPUT PULSE



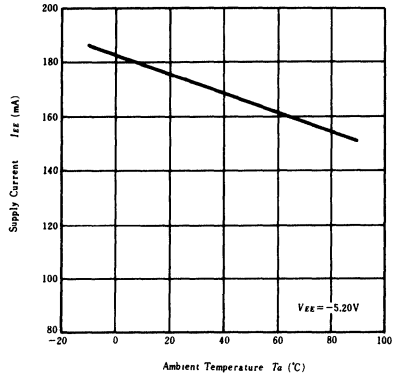
3. READ MODE



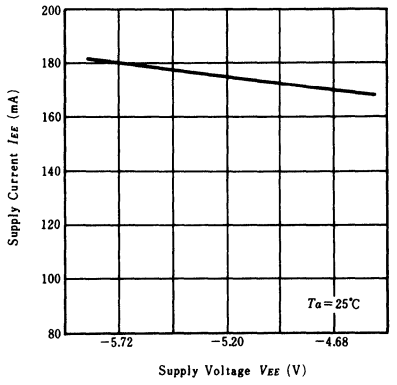
4. WRITE MODE



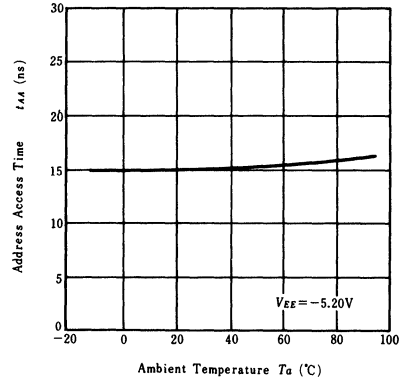
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



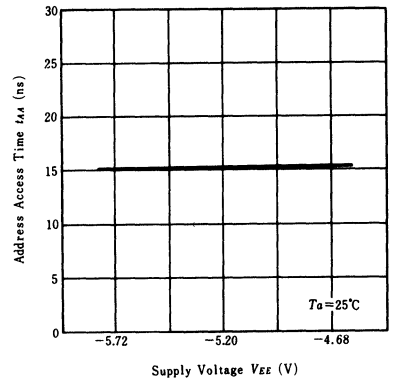
SUPPLY CURRENT vs. SUPPLY VOLTAGE



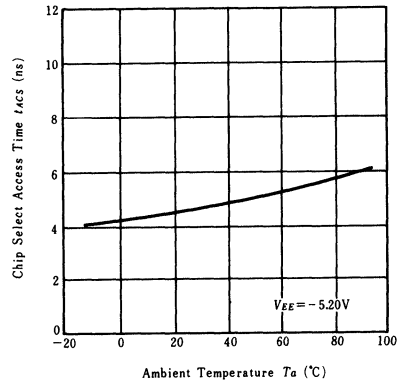
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



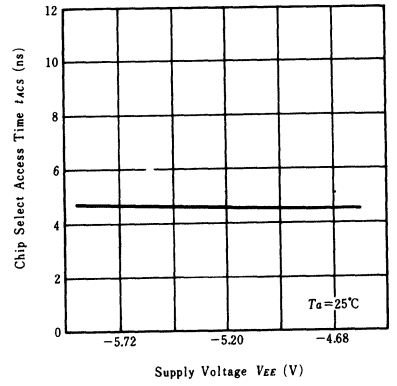
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



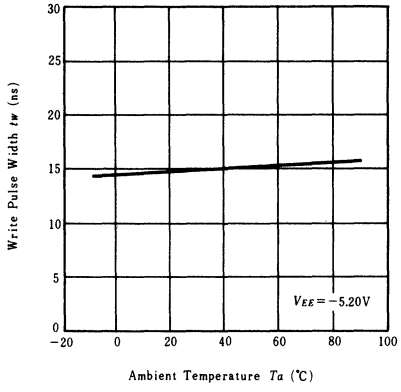
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



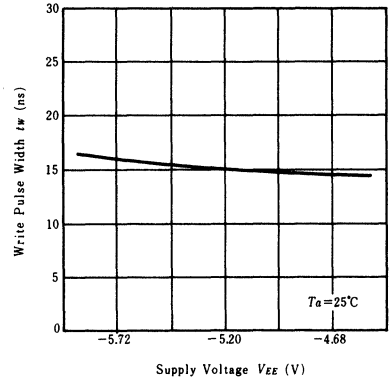
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE

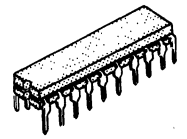


HM10480, HM10480F

16,384-words × 1-bit Fully Decoded Random Access Memory

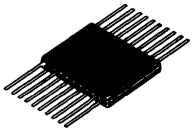
The HM10480 is ECL 10K compatible, 16,384-words x 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storages.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM10480 is encapsulated in cerdip-20 pin and flat 20-pin package, compatible with Fairchild's F10480.

HM10480



(DG-20)

HM10480F



(FG-20)

■FEATURES

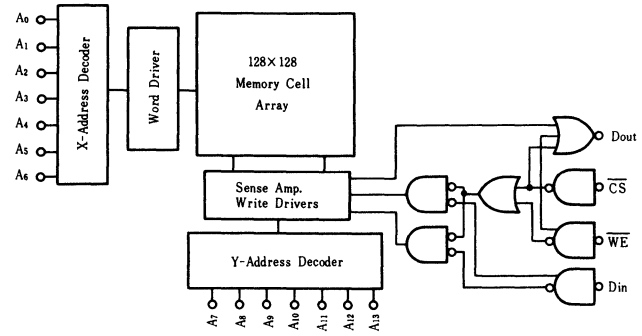
- 16,384-words x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: 25ns (max)
- Write pulse width: 25ns(min)
- Low power dissipation: 0.05mW/bit
- Output obtainable by wired-OR (open emitter)

■TRUTH TABLE

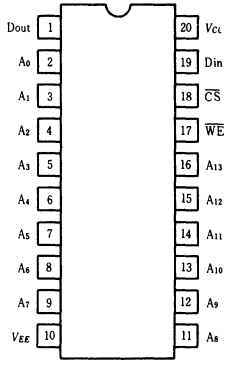
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Noninvert

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −5.2V, R_L = 50Ω to −2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit
Output Voltage	V_{OH}	V_{IN} = V_{IHA} or V_{ILB}	0°C	−1000	—	−840	mV
			+25°C	−960	—	−810	
			+75°C	−900	—	−720	
	V_{OL}		0°C	−1870	—	−1665	
			+25°C	−1850	—	−1650	
			+75°C	−1830	—	−1625	
Output Threshold Voltage	V_{OHC}	V_{IN} = V_{IHB} or V_{ILA}	0°C	−1020	—	—	mV
			+25°C	−980	—	—	
			+75°C	−920	—	—	
	V_{OLC}		0°C	—	—	−1645	
			+25°C	—	—	−1630	
			+75°C	—	—	−1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	−1145	—	−840	mV
			+25°C	−1105	—	−810	
			+75°C	−1045	—	−720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	—	−1490	
			+25°C	−1850	—	−1475	
			+75°C	−1830	—	−1450	
Input Current	I_{IH}	V_{IN} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{CS}$ / V_{IN} = V_{ILB}	0 to +75°C	0.5	—	170	
		Others		−50	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 10	Ta = 0°C	−170	−140	—	mA
			Ta = 75°C	—	−130	—	

●AC CHARACTERISTICS (V_{EE} = −5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		2	—	10	ns
Chip Select Recovery Time	t_{RCS}		2	—	10	ns
Address Access Time	t_{AA}		3	15	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 5ns	25	—	—	ns
Data Setup Time	t_{WSD}		5	—	—	ns
Data Hold Time	t_{WHD}		5	—	—	ns
Address Setup Time	t_{WSA}	t_W = 25ns	5	—	—	ns
Address Hold Time	t_{WHA}		5	—	—	ns
Chip Select Setup Time	t_{WSCS}		5	—	—	ns
Chip Select Hold Time	t_{WHCS}		5	—	5	ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	10	ns

3. RISE/FALL TIME

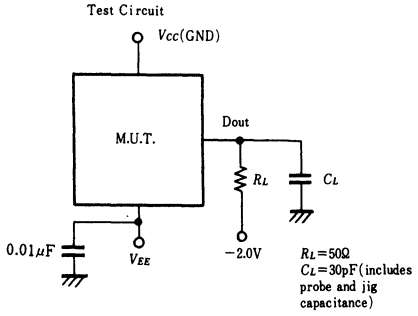
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

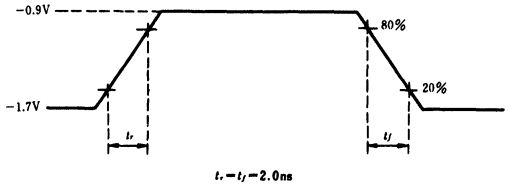
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

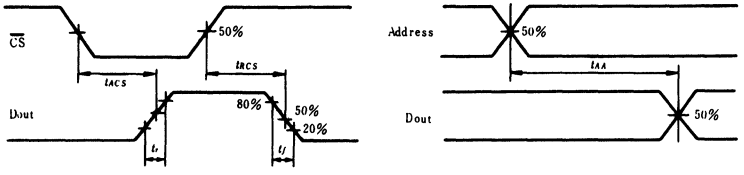
1. LOADING CONDITION



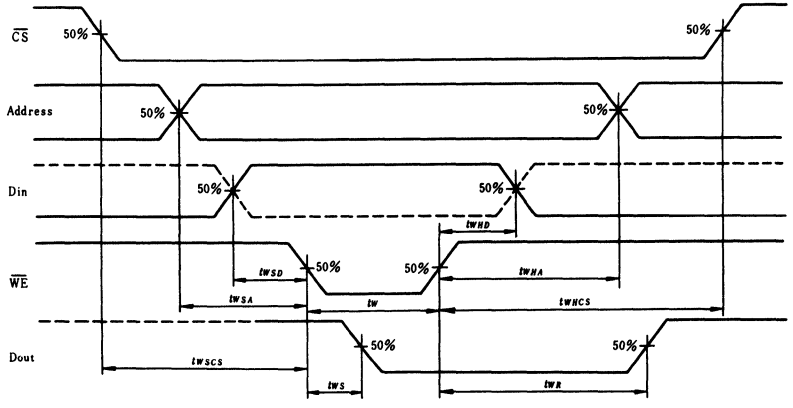
2. INPUT PULSE



3. READ MODE



4. WRITE MODE

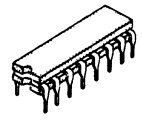


HM100415,HM100415CC

1024-word×1-bit Fully Decoded Random Access Memory

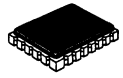
The HM100415 is a 1024-word x 1-bit, read/write random access memory developed for application to scratch pads, control and buffer storages which require very high speeds.
The HM100415 is compatible with the HD100K families and includes on-chip voltage and temperature compensation for improved noise margin. This memory is encapsulated in cerdip-16pin package.

HM100415



(DG-16A)

HM100415CC



(CC-24)

■FEATURES

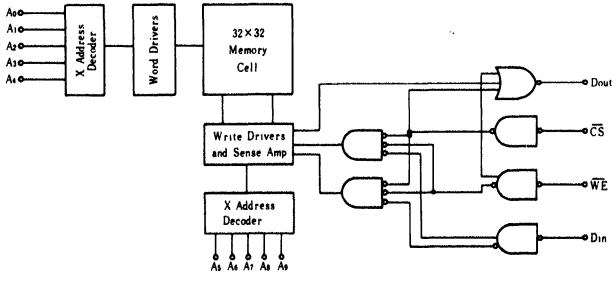
- Level ..... 100K ECL Compatible
- Organization ..... 1024-word by 1-bit
- Address Access Time ..... 10ns (max)
- Chip Select Access Time ..... 5ns (max.)
- Power Consumption ..... 0.6mW/bit (typ)
- Output Obtainable by Wired-OR (open emitter)
- Compatible with Fairchild F100415.

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

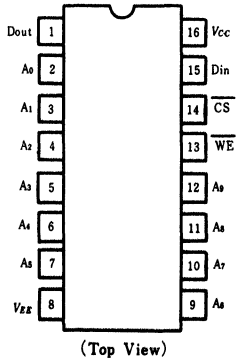
Notes) × : Irrelevant
* : Read Out Noninvert

■BLOCK DIAGRAM



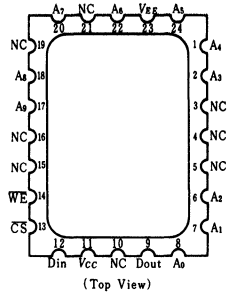
■PIN ARRANGEMENT

●HM100415



(Top View)

●HM100415CC



(Top View)

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

HITACHI

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −4.5V, R_L = 50Ω to −2.0V, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage		−1165	—	−880	mV
	V_{IL}	High/Low for All Inputs		−1810	—	−1475	mV
Input Current	I_{IH}	V_{in} = V_{IHA}		—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−150	—	mA

●AC CHARACTERISTICS (V_{EE} = −4.5V ±5%, Ta = 0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	3	5	ns
Chip Select Recovery Time	t_{RCS}		—	3	5	ns
Address Access Time	t_{AA}		—	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA} = 2ns	6	4	—	ns
Data Setup Time	t_{WSD}		2	0	—	ns
Data Hold Time	t_{WHD}		2	0	—	ns
Address Setup Time	t_{WSA}	t_W = 6ns	2	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Chip Select Setup Time	t_{WSCS}		2	0	—	ns
Chip Select Hold Time	t_{WHCS}		2	0	—	ns
Write Disable Time	t_{WS}		—	3	5	ns
Write Recovery Time	t_{WR}		—	3	5	ns

3. RISE/FALL TIME

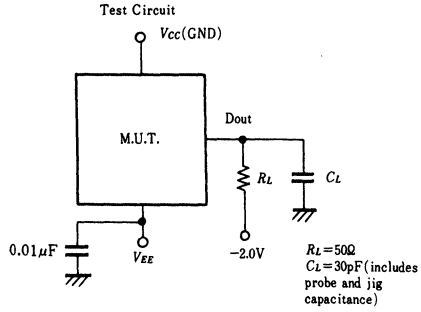
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

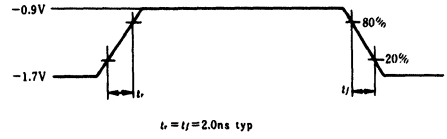
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

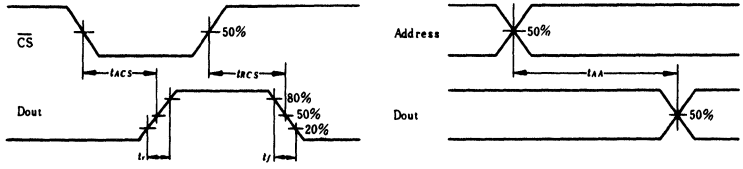
1. LOADING CONDITION



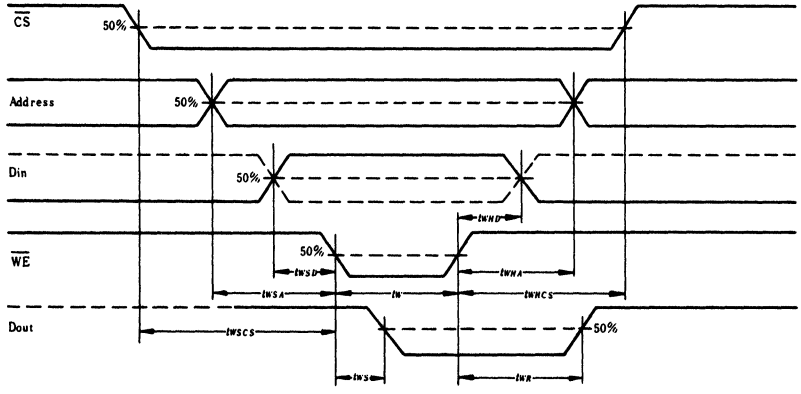
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



HM100422,HM100422F
HM100422CC

256-word×4-bit Fully Decoded Random Access Memory

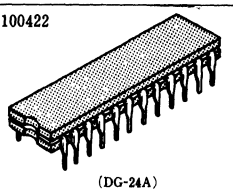
The HM100422 is ECL 100K compatible, 256-word x 4-bit, read write, random access memory developed for high speed system such as scratch pads and control/buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

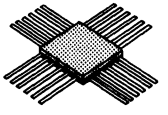
The HM100422 is encapsulated in cerdip-24pin package, or 24pin flat package compatible with Fairchild's F100422.

HM100422



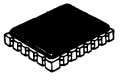
(DG-24A)

HM100422F



(FG-24)

HM100422CC



(CC-24)

■FEATURES

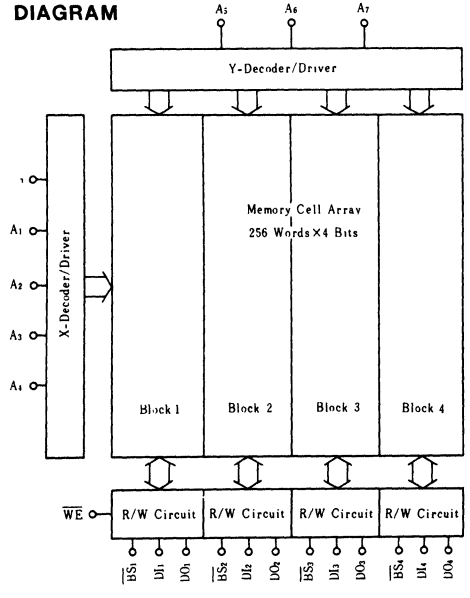
- 256-word x 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: 10ns (max.)
- Minimum write pulse width: 6ns (min.)
- Low power dissipation: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

■TRUTH TABLE

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

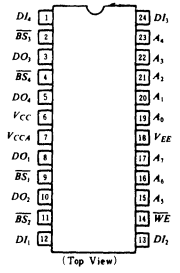
Notes) × : Irrelevant
* : Read Out Noninvert

■BLOCK DIAGRAM



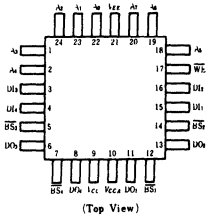
■PIN ARRANGEMENT

●HM100422



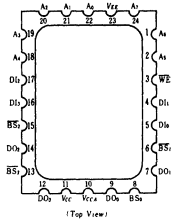
(Top View)

●HM100422F



(Top View)

●HM100422CC



(Top View)

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE}=−4.5V, R_L=50Ω to −2.0V, Ta=0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{in}=V_{IHA}$ or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{in}=V_{IHB}$ or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage		−1165	—	−880	mV
	V_{IL}	High/Low for All Inputs		−1810	—	−1475	mV
Input Current	I_{IH}	$V_{in}=V_{IHA}$		—	—	220	μA
	I_{IL}	$V_{in}=V_{ILB}$	$\overline{BS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	—	mA

●AC CHARACTERISTICS (V_{EE}=−4.5V ±5%, Ta=0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	t_{ABS}		—	—	5	ns
Block Select Recovery Time	t_{RBS}		—	—	5	ns
Address Access Time	t_{AA}		—	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA}=2ns	6	4.5	—	ns
Data Setup Time	t_{WSD}		2	0	—	ns
Data Hold Time	t_{WHD}		2	0	—	ns
Address Setup Time	t_{WSA}	t_W=6ns	2	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Block Select Setup Time	t_{WSBS}		2	0	—	ns
Block Select Hold Time	t_{WHBS}		2	0	—	ns
Write Disable Time	t_{WS}		—	4	5	ns
Write Recovery Time	t_{WR}		—	4.5	9	ns

3. RISE/FALL TIME

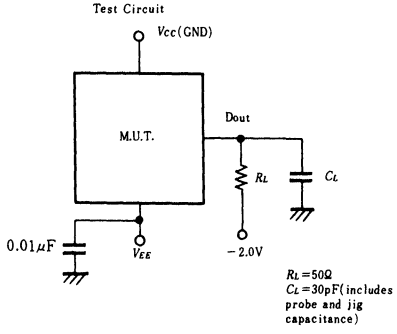
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

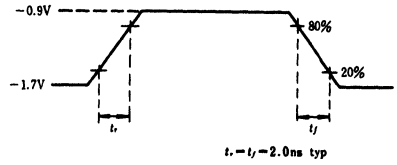
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

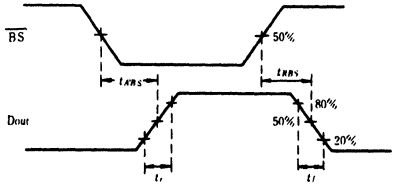
1. LOADING CONDITION

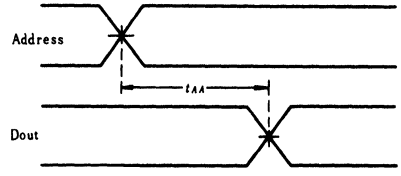


2. INPUT PULSE

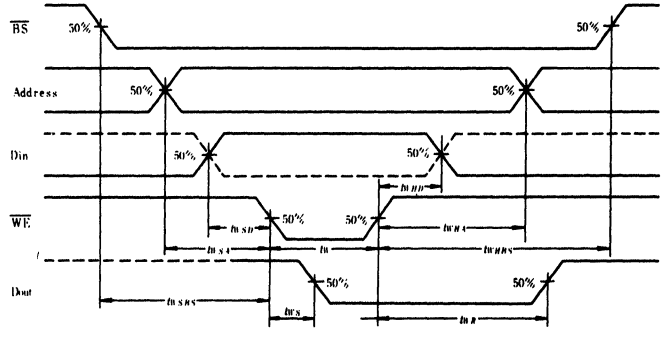


3. READ MODE





4. WRITE MODE



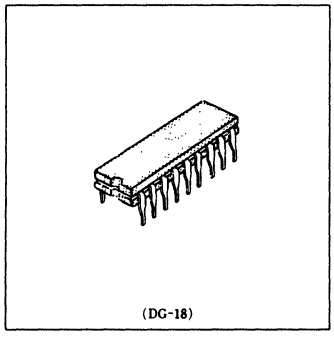
HM100470,HM100470-15

4096-word×1-bit Fully Decoded Random Access Memory

The HM100470 is a 4096-words x 1-bit, read/write, random access memory developed for high speed systems such as scratch pads and control buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM100470 is compatible with the HD100K ECL families and includes on-chip voltage and temperature compensation for improved noise margin. This device is encapsulated in cerdip-18pin package, compatible with Fairchild's F100470.

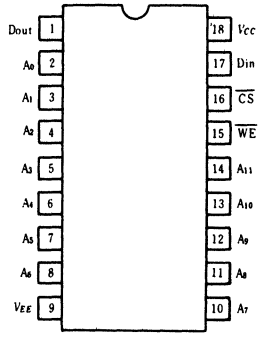


(DG-18)

■FEATURES

- 4096-word x 1-bit organization
- Full compatible with 100K ECL level
- Address access time: HM100470 25ns(max)
- HM100470-15 15ns(max)
- Write pulse width: HM100470 25ns (min)
- HM100470-15 15ns (min)
- Output obtainable by wired-OR (open emitter)

■PIN ARRANGEMENT



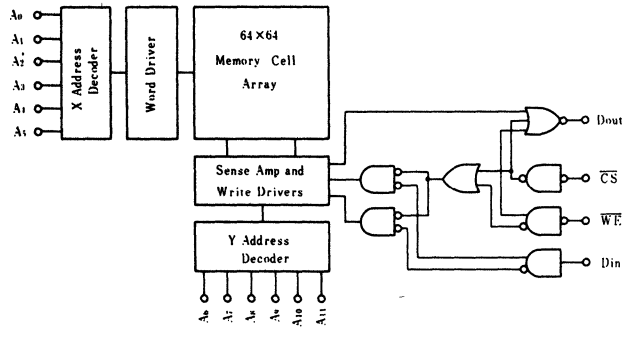
(Top View)

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

HITACHI

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −4.5V, R_L=50Ω to −2.0V, Ta=0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{in}=V_{IHA}$ or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{in}=V_{IHB}$ or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage		−1165	—	−880	mV
	V_{IL}	High/Low for All Inputs		−1810	—	−1475	mV
Input Current	I_{IH}	$V_{in}=V_{IHA}$		—	—	220	μA
	I_{IL}	$V_{in}=V_{ILB}$	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	—	mA

●AC CHARACTERISTICS (V_{EE} = −4.5V ±5%, Ta=0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM100470-15			HM100470			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	—	8	—	—	10	ns
Chip Select Recovery Time	t_{RCS}		—	—	8	—	—	10	ns
Address Access Time	t_{AA}		—	—	15	—	—	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM100470-15			HM100470			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA}=3ns	15	—	—	25	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	t_W=twmin	3	—	—	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	8	—	—	10	ns
Write Recovery Time	t_{WR}		—	—	8	—	—	10	ns

3. RISE/FALL TIME

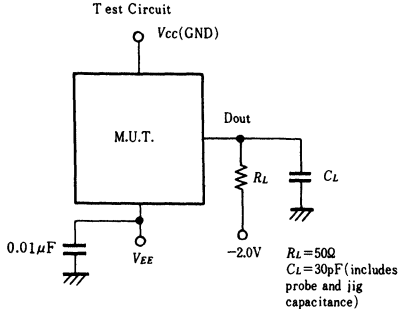
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

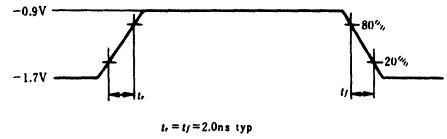
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

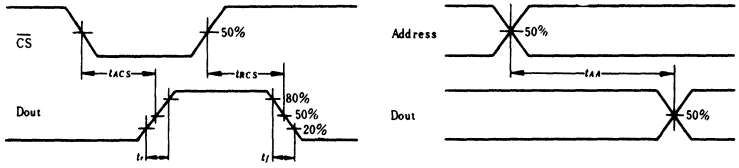
1. LOADING CONDITION



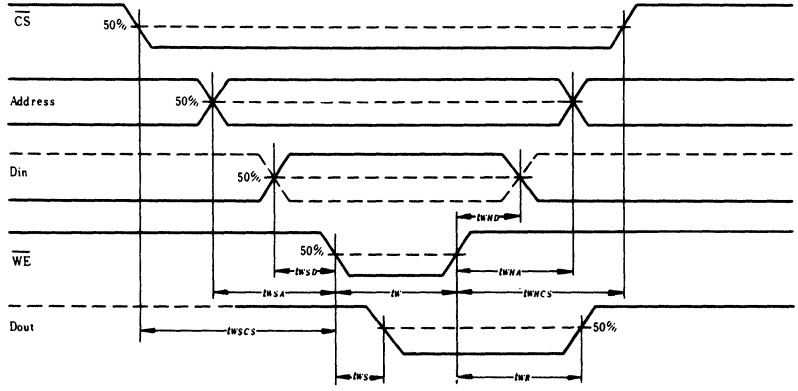
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



HM100474,HM100474-15
HM100474F,HM100474F-15

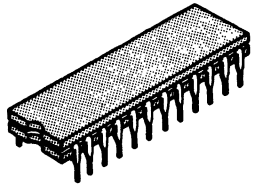
1024-word×4-bit Fully Decoded Random Access Memory

The HM100474 is a 1024-words x 4-bit, read/write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

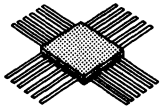
The HM100474 is compatible with the HD100K ECL families and includes on-chip voltage and temperature compensation for improved noise margin. This device is encapsulated in cerdip-24-pin and flat 24pin package, compatible with Fairchild's F100474.

HM100474, HM100474-15



(DG-24A)

HM100474F, HM100474F-15



(FG-24)

■FEATURES

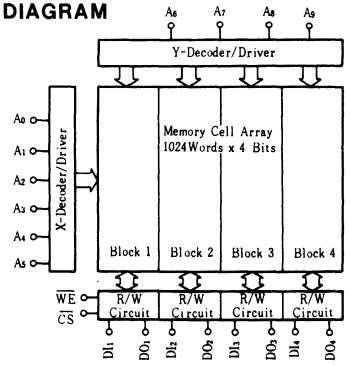
- 1024-word x 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: HM100474/F 25ns(max)
  HM100474/F-15 15ns(max)
- Write pulse width: HM100474/F 25ns(min)
  HM100474/F-15 15ns(min)
- Output obtainble by wired-OR (open emitter)

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Nonivert

■BLOCK DIAGRAM



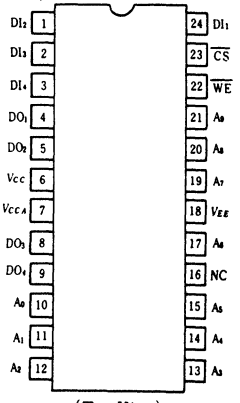
■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

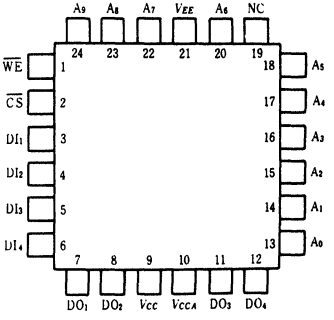
■PIN ARRANGEMENT

●HM100474,HM100474-15



(Top View)

●HM100474F, HM100474F-15



(Top View)

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS (V_{EE} = −4.5V, R_L = 50Ω to −2.0V, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{in} = V_{IHA}$ or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	$V_{in} = V_{IHB}$ or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		−1165	—	−880	mV
	V_{IL}			−1810	—	−1475	mV
Input Current	I_{IH}	$V_{in} = V_{IHA}$		—	—	220	μA
	I_{IL}	$V_{in} = V_{ILB}$	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	—	mA

●AC CHARACTERISTICS (V_{EE} = −4.5V ±5%, Ta = 0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM100474/F-15			HM100474/F			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	—	8	—	—	10	ns
Chip Select Recovery Time	t_{RCS}		—	—	8	—	—	10	ns
Address Access Time	t_{AA}		—	—	15	—	15	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM100474/F-15			HM100474/F			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	t_{WSA} = 3ns	15	—	—	25	15	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	t_W = twmin	3	—	—	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	8	—	—	10	ns
Write Recovery Time	t_{WR}		—	—	8	—	—	10	ns

3. RISE/FALL TIME

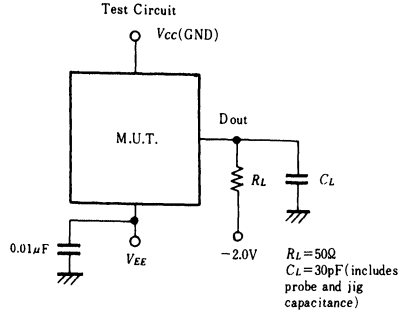
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

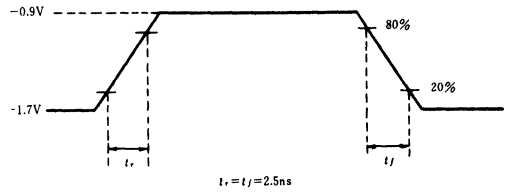
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

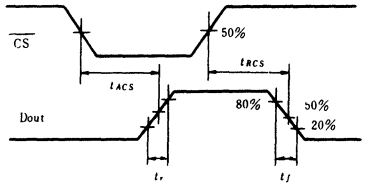
1. LOADING CONDITION

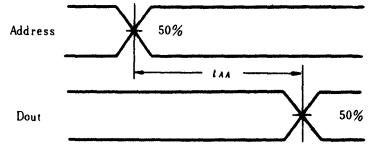


2. INPUT PULSE

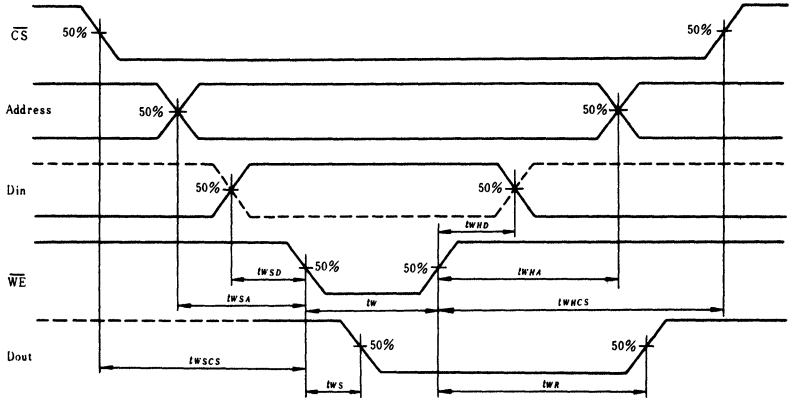


READ MODE

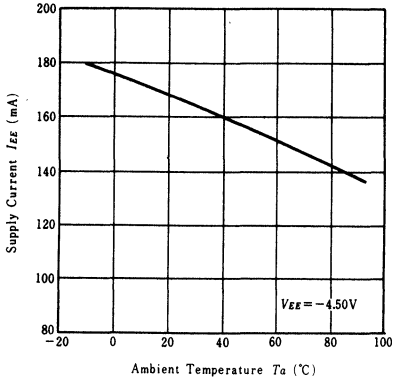




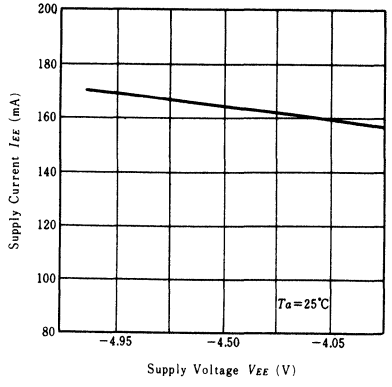
4. WRITE MODE



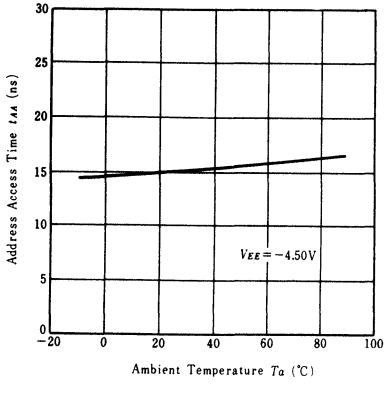
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



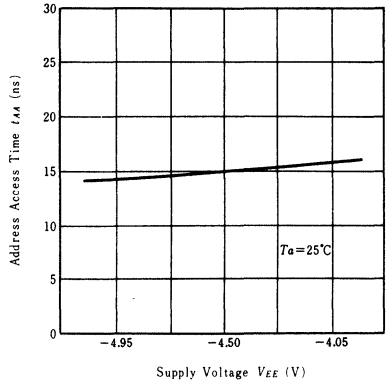
SUPPLY CURRENT vs. SUPPLY VOLTAGE



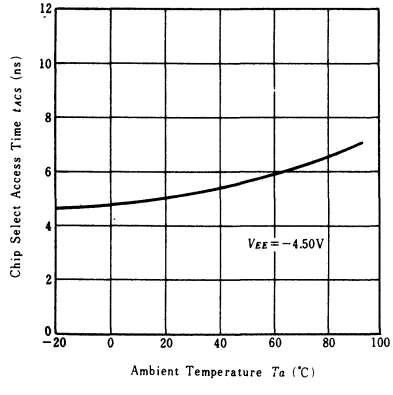
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



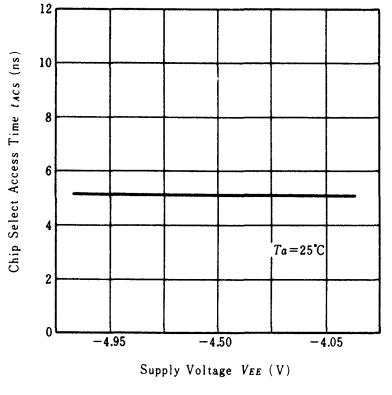
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



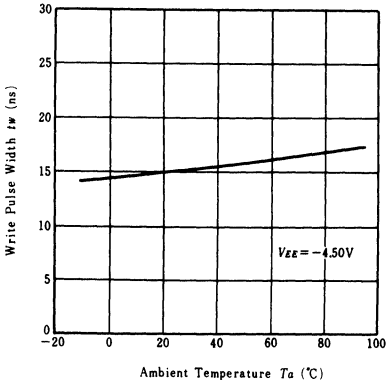
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



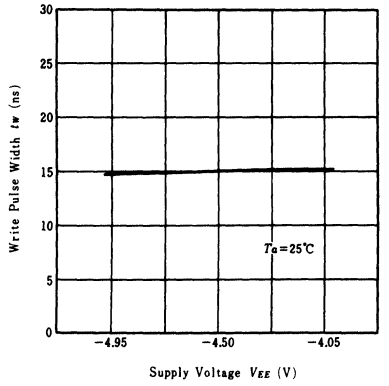
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE

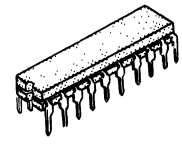


HM100480, HM100480F

16,384-words×1-bit Fully Decoded Random Access Memory

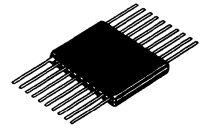
The HM100480 is ECL 100K compatible, 16,384-words x 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storages.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM100480 is encapsulated in cerdip-20 pin and flat-20 pin package, compatible with Fairchild's 100480.

HM100480



(DG-20)

HM100480F



(FG-20)

■FEATURES

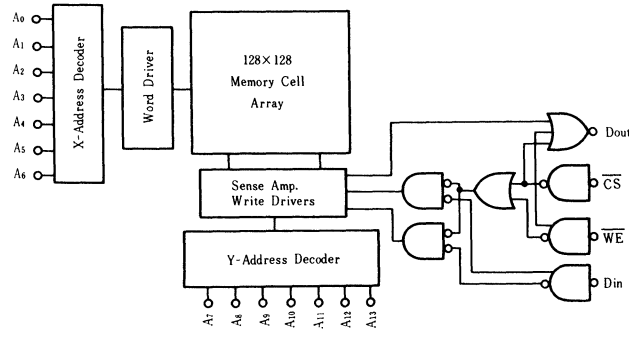
- 16,384-words x 1-bit organization
- Fully compatible with 100K ECL level
- Address access time: 25ns (max)
- Write pulse width: 25ns (min)
- Low power dissipation: 0.05mW/bit
- Output obtainable by wired-OR (open emitter)

■TRUTH TABLE

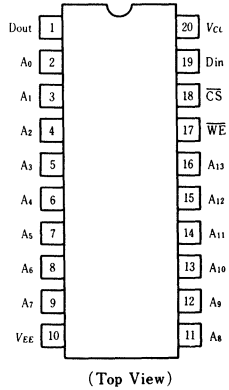
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Noninvert

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

HITACHI

■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

■ELECTRICAL CHARACTERISTICS

●DC CHARACTERISTICS(V_{EE}=−4.5V, R_L=50Ω to −2.0V, Ta=0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	V_{in}=V_{IHA} or V_{ILB}		−1025	−955	−880	mV
	V_{OL}			−1810	−1715	−1620	mV
Output Threshold Voltage	V_{OHC}	V_{in}=V_{IHB} or V_{ILA}		−1035	—	—	mV
	V_{OLC}			—	—	−1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage		−1165	—	−880	mV
	V_{IL}	High/Low for All Input		−1810	—	−1475	mV
Input Current	I_{IH}	V_{in}=V_{IHA}		—	—	220	μA
	I_{IL}	V_{in}=V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	−50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		−200	−165	—	mA

●AC CHARACTERISTICS (V_{EE}=−4.5V±5%, Ta=0 to +85°C, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		2	—	10	ns
Chip Select Recovery Time	t_{RCS}		2	—	10	ns
Address Access Time	t_{AA}		3	—	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	t_{WSA}=5ns	25	—	—	ns
Data Setup Time	t_{WSD}		5	—	—	ns
Data Hold Time	t_{WHD}		5	—	—	ns
Address Setup Time	t_{WSA}	t_W=t_W min	5	—	—	ns
Address Hold Time	t_{WHA}		5	—	—	ns
Chip Select Setup Time	t_{WSCS}		5	—	—	ns
Chip Select Hold Time	t_{WHCS}		—	—	5	ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	10	ns

3. RISE/FALL TIME

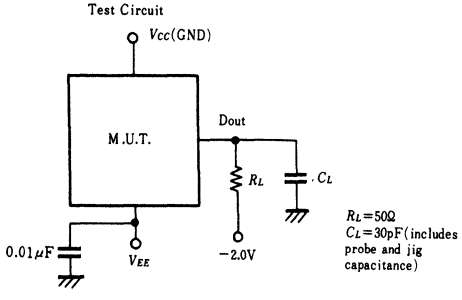
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

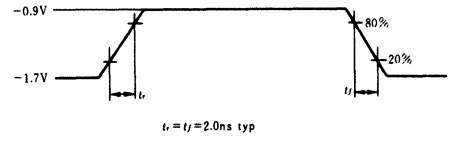
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

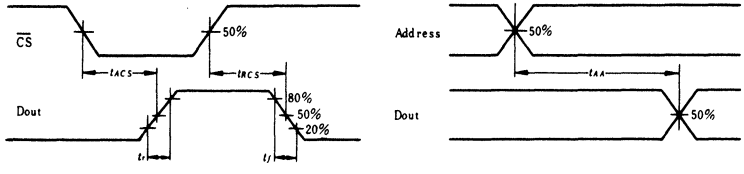
1. LOADING CONDITION



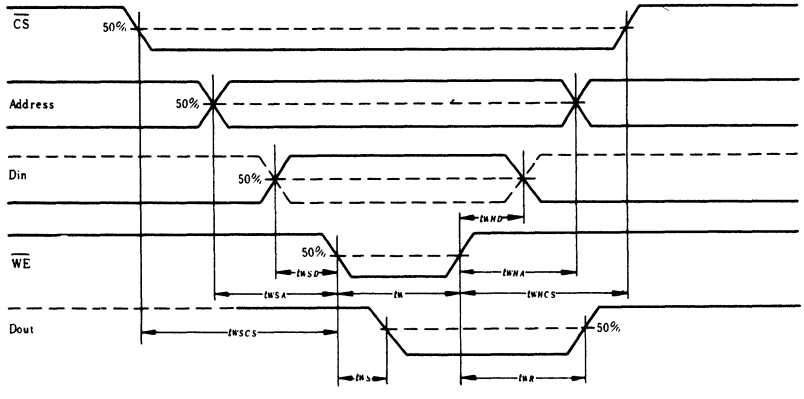
2. INPUT PULSE



3. READ MODE

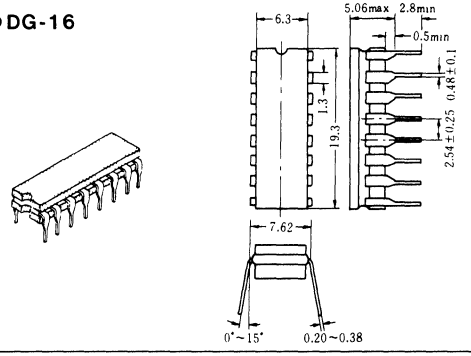


4. WRITE MODE

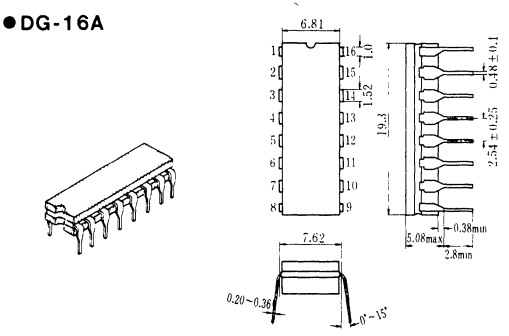


● CERDIP

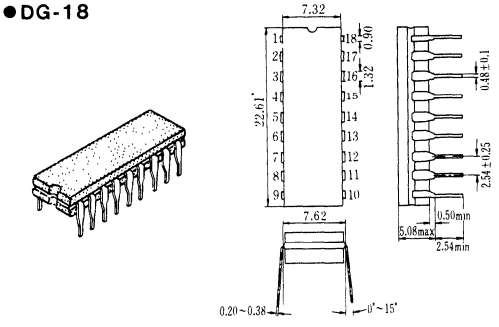
● DG-16



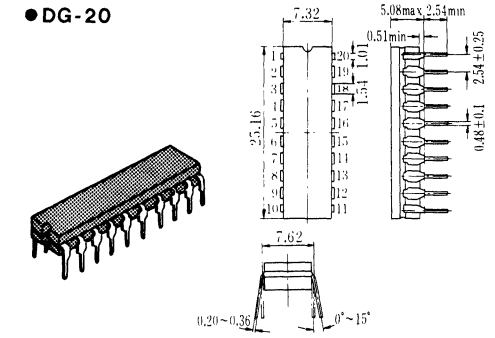
● DG-16A



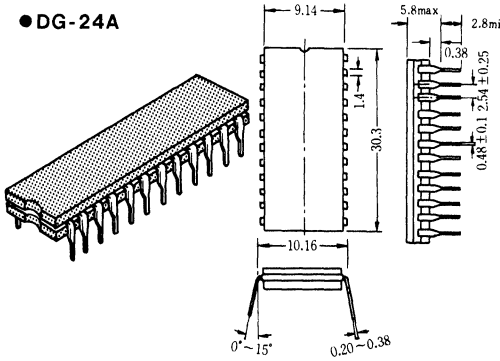
● DG-18



● DG-20

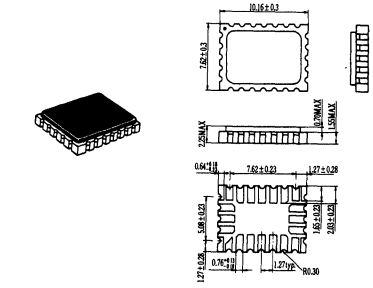


● DG-24A



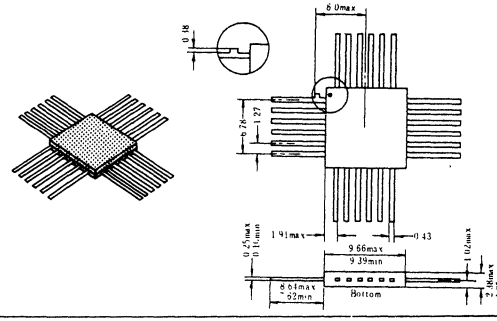
● Leadless Chip Carrier

● CC-24

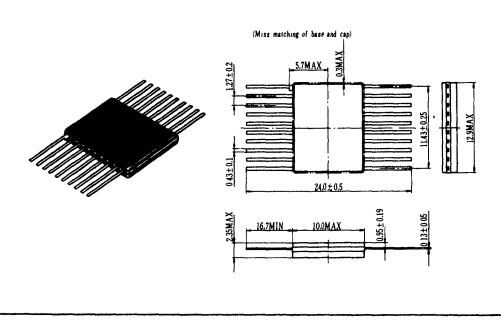


● Flat Package

● FG-24



● FG-20



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