HITACHI®

DRAM DATA BOOK

DRAM
DATA BOOK

#M11T011

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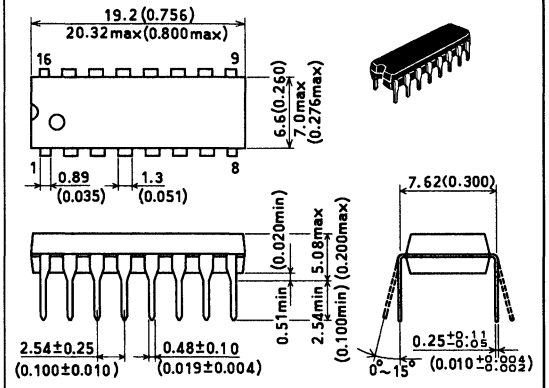
■ PACKAGE INFORMATION

• **Dual-in-line Plastic**

Unit: mm (inch) Scale 3/2

• **DP-16B**



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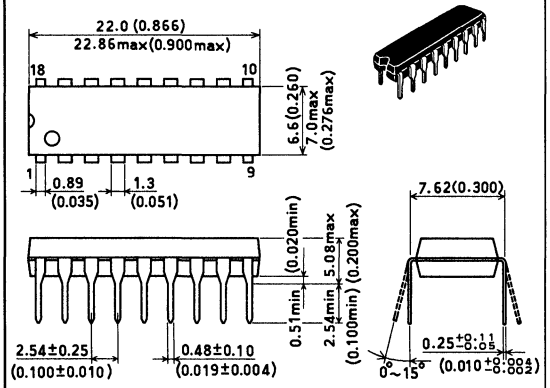

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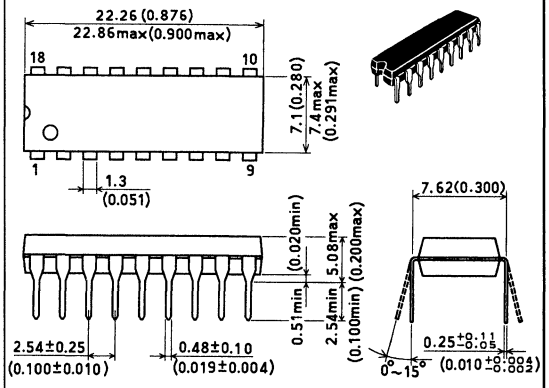

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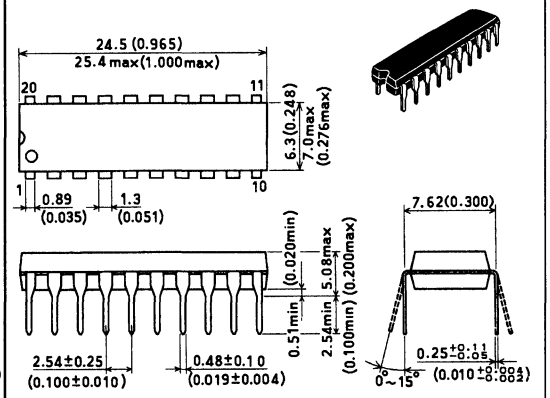

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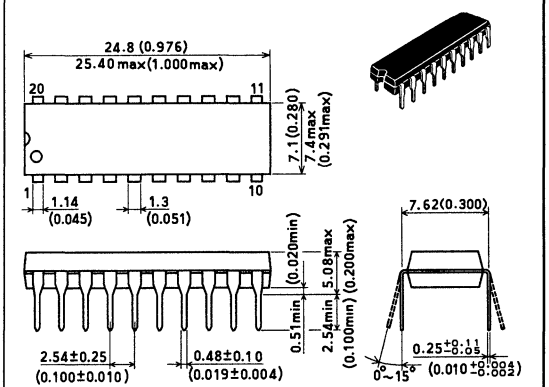

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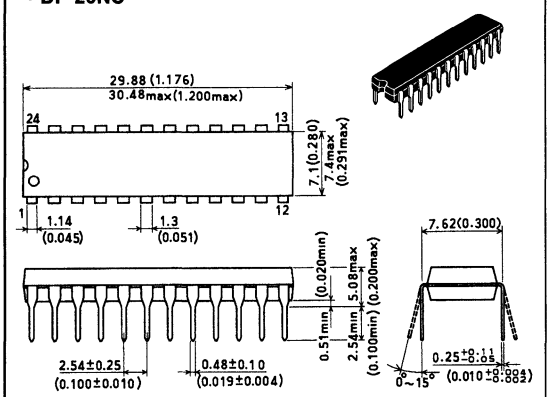

PACKAGE INFORMATION

• Dual-in-line Plastic

Unit: mm (inch) Scale 3/2

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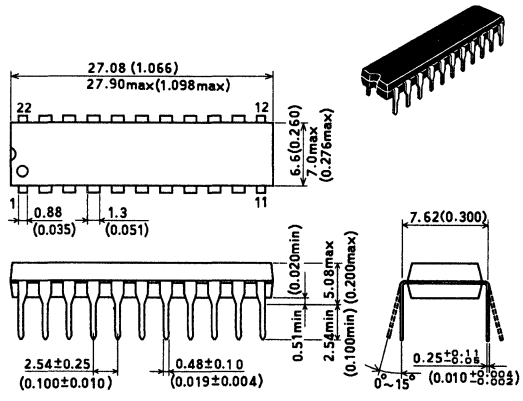

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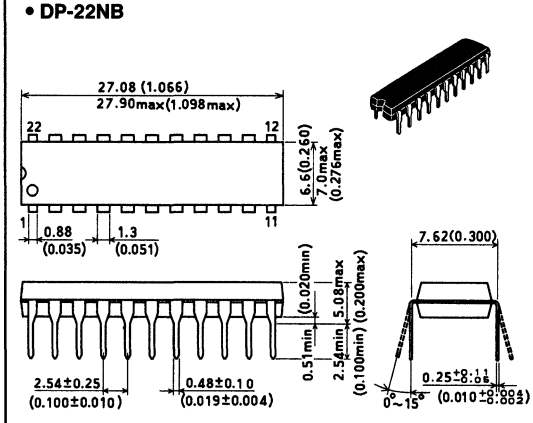

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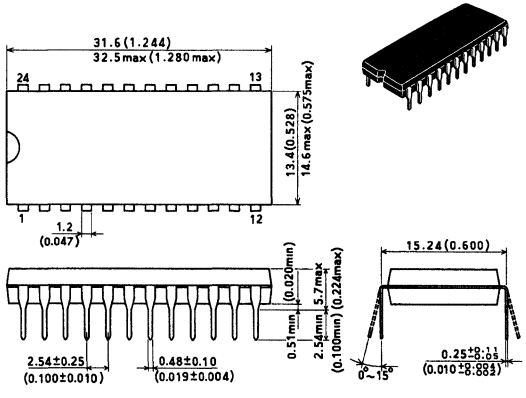

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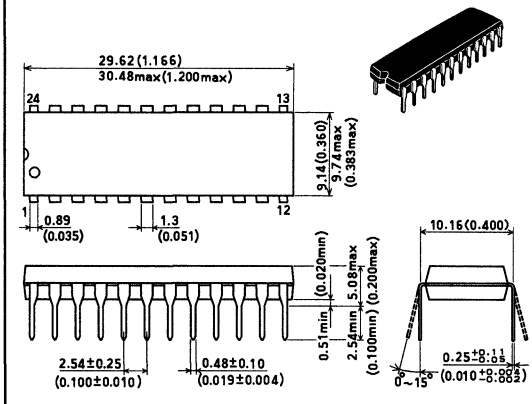

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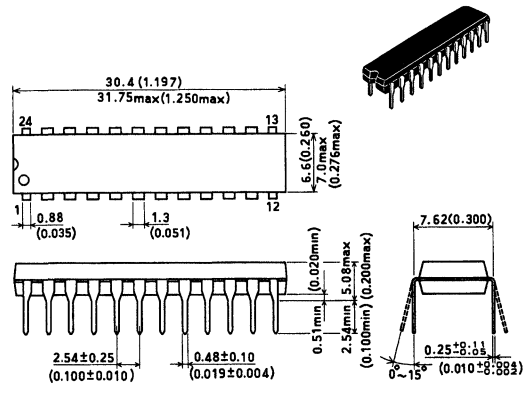

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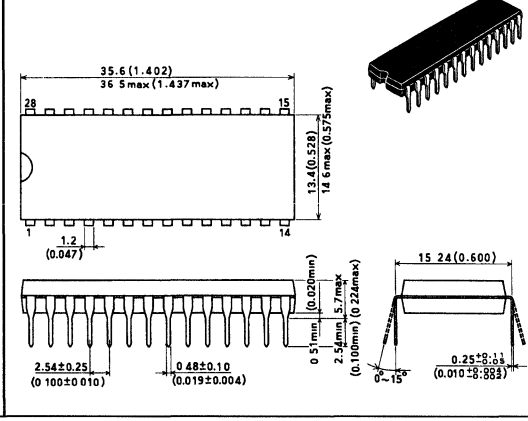
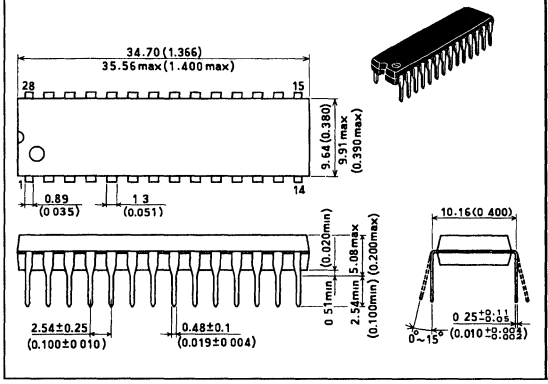


• Dual-in-line Plastic

Unit: mm (inch) Scale 3/2

• DP-28C



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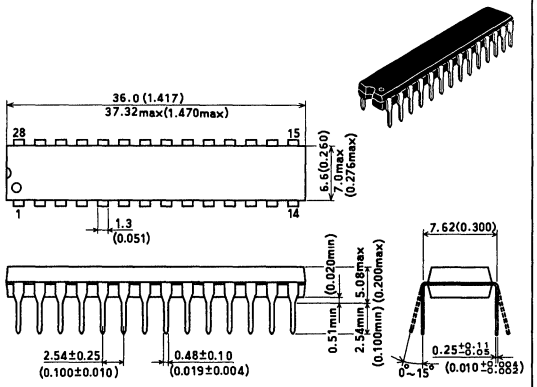
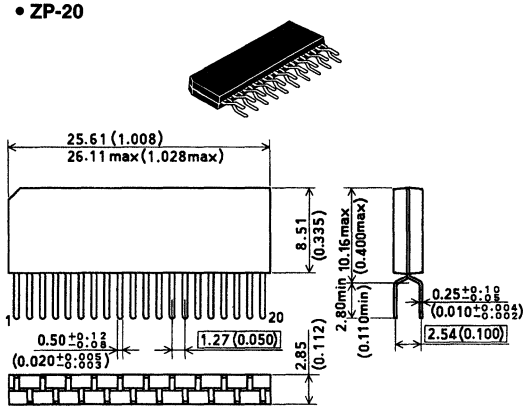


PACKAGE INFORMATION

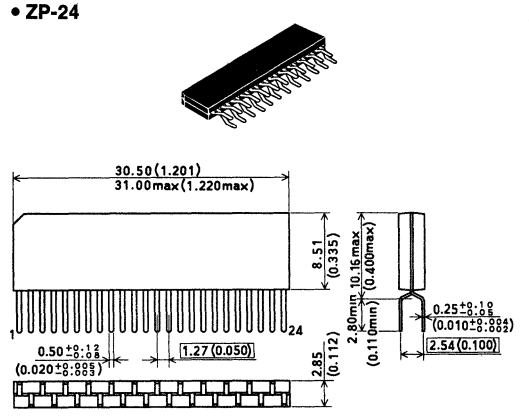
• Zigzag-in-line Plastic

Unit: mm (inch) Scale 3/2

• ZP-20



• ZP-24



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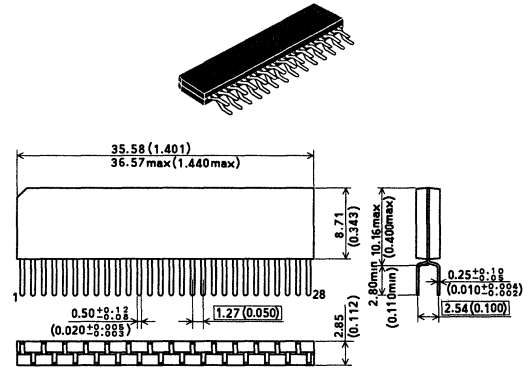
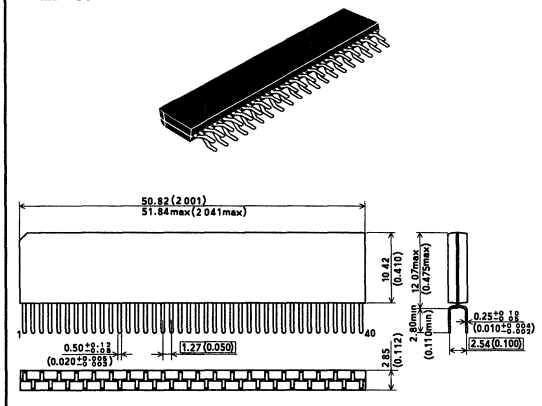


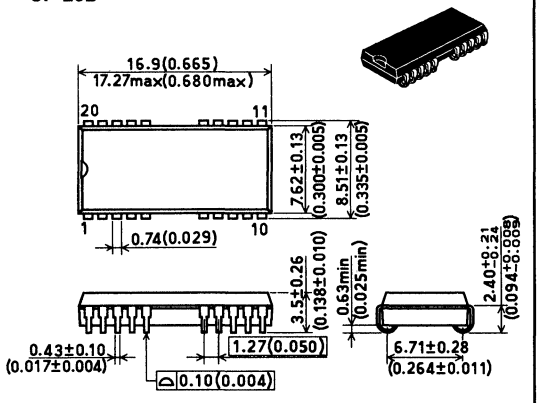
• ZP-40



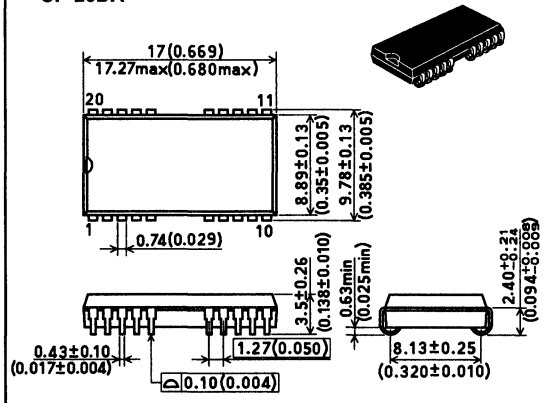
• Flat Package (J-bend Leads)

Unit: mm (inch) Scale 3/2

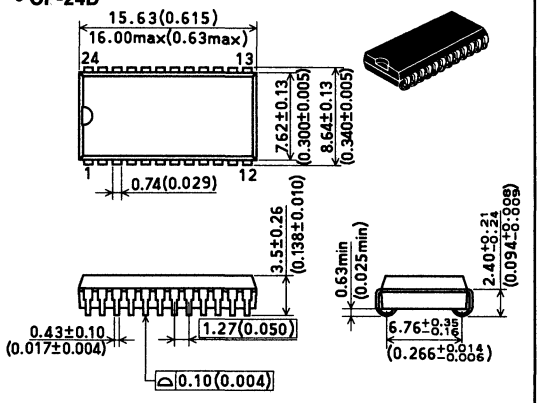
• CP-20D



• CP-20DA



• CP-24D



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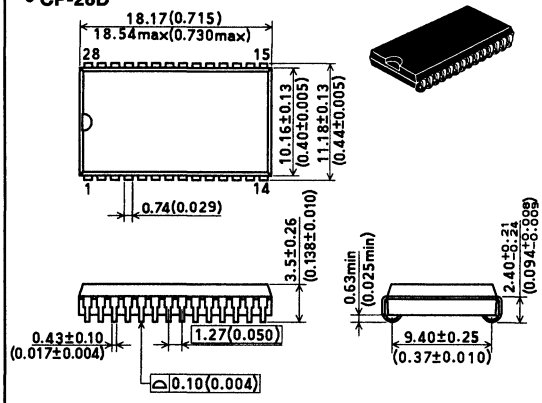

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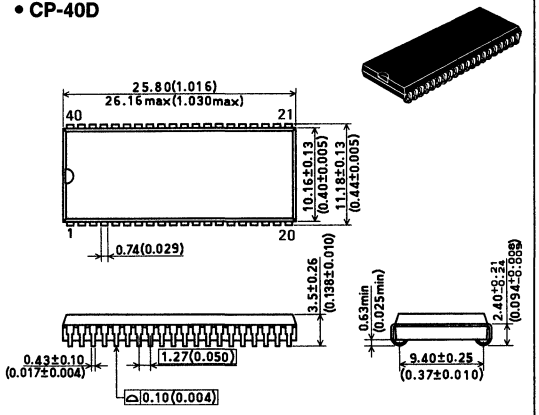
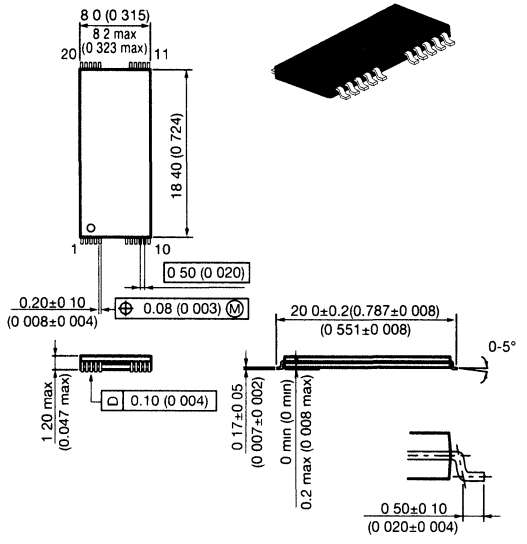


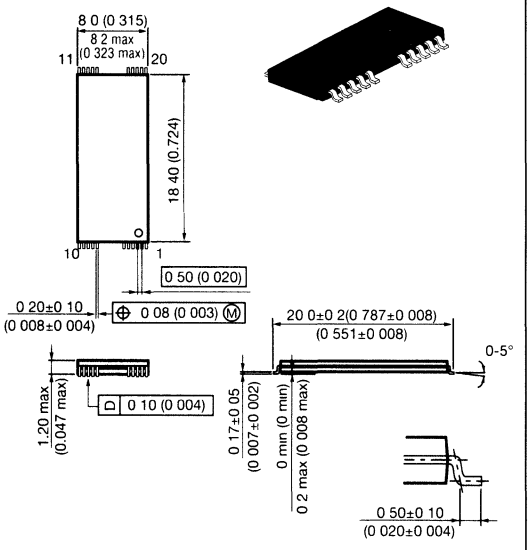
• TSOP (Thin Small Outline Package)

Unit: mm (inch) Scale 3/2

• TFP-20DA



• TFP-20DAR



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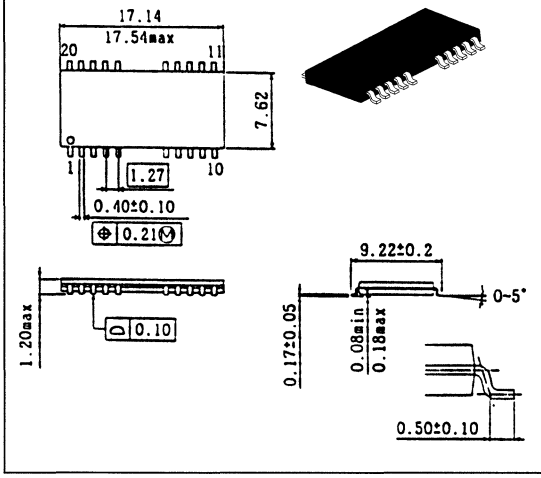

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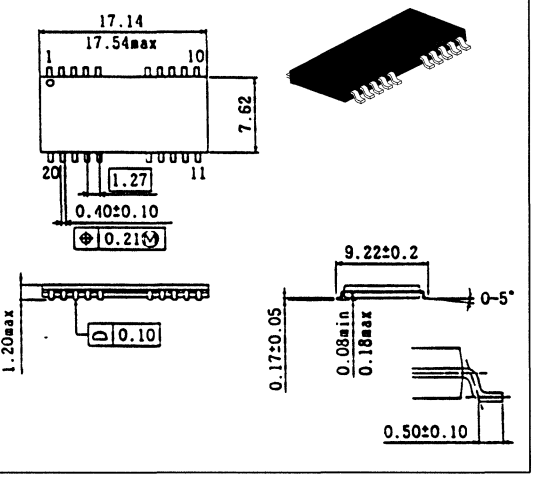


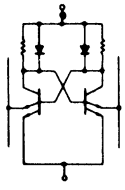
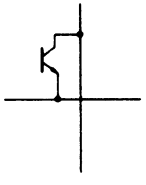
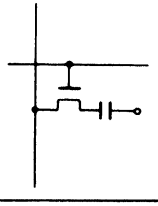
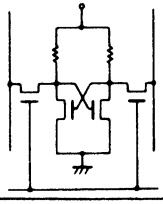
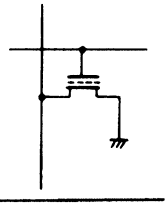
■ RELIABILITY OF HITACHI IC MEMORIES

1. STRUCTURE

IC memories are basically classified into bipolar type and MOS type and utilized effectively by their characteristics. The characteristic of bipolar memories is high speed but small capacity, instead, MOS memories have large capacity. There are also differences in circuit design, layout pattern, degree of integration, and manufacturing process. These memories have been produced with the standardized concept of design and inspection all through the processes of designing, manufacturing and inspection.

IC memories are constituted by the unit patterns called cells, which are integrated in high density. The knowhows based on our experience have been applied in every production stage. In addition, reliability has been ensured using TEG (Test Element Group) evaluation. Examples of cell circuits of bipolar and MOS memories are shown in Table 1.

• Table 1. Basic Cell Circuit of IC Memories

Classification	Bipolar memory (RAM)	Bipolar memory (PROM)	NMOS memory (Dynamic RAM)	NMOS, CMOS memories (Static RAM)	NMOS memory (PROM)
Application	Buffer memory, control memory of high-speed computer	Microcomputer control use	Main memory of computer, microcomputer memory		For microcomputer control
Example of basic cell circuit					

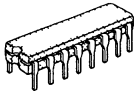
0137-16

Dies of IC memories are produced in various packages. In this process of packaging, Hitachi has also innovated new techniques and ensured to high level. As packages for IC memories, cerdip (glass-sealed) packages and plastic packages are currently used. Also such packages as LCC (Leadless Chip Carrier) or SOP (Small Outline Package) have been developed for high density packaging. Cerdip packages sealed hermetically are suitable equipment requiring high reliability. Plastic packages are widely applied to many kinds of equipment. Hitachi plastic packages have improved the reliability level as highly as that of the hermetically sealed packages. Table 2 shows the outlines of the Hitachi packages.

• Table 2. IC Memory Package Outline

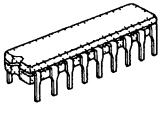
■ **Cerdip**

• 16-Pin



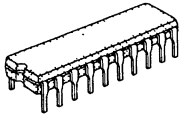
3DDG16

• 18-Pin



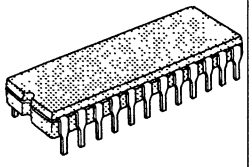
3DDG18

• 20-Pin



3DDG20N

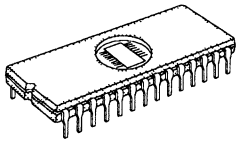
• 24-Pin



3DDG24N

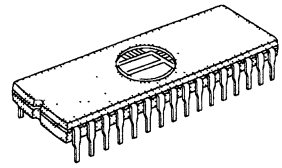
■ **Cerdip** (continued)

•28-Pin with Lid



3DDG28

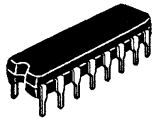
•32-Pin with Lid



3DDG32

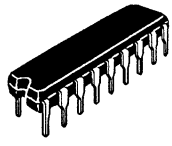
■ **Plastic DIP**

•16-Pin



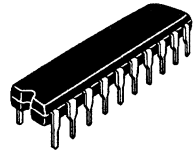
3DDP16B

•18-Pin



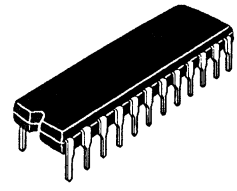
3DDP18B

•20-Pin



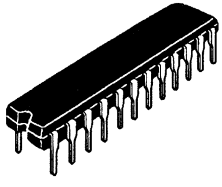
3DDP20N

•24-Pin



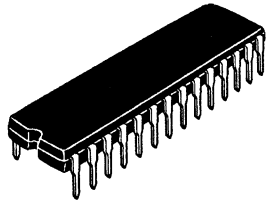
3DDP24A

• 24-Pin



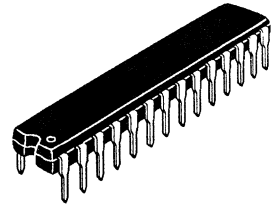
3DDP24N

• 28-Pin



3DDP28

• 28-Pin



3DDP28N

■ **Leadless Chip Carrier**

• 20-Pin

3DCG20

• 22-Pin

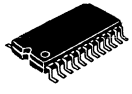
3DCG22A

• 24-Pin

3DCG24

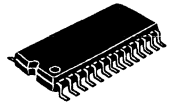
■ **SOP**

• 24-Pin



3DFP24D

• 28/32-Pin



3DFP28D

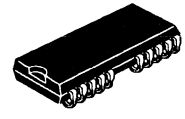
■ **PLCC**

• 18-Pin

3DCP18

■ **SOJ**

• 20/26/28/32-Pin



3DCP20D

2. RELIABILITY

Results of reliability tests are listed below

2.1 Reliability Test Data on Bipolar Memories

The reliability test data on the bipolar memories are shown in Table 3 and 4. Since they are manufactured under the standardized design rules and quality control, there is no difference in reliability among the various types. And the larger the capacity is, the higher the reliability per bit becomes.

• Table 3. Results on Bipolar Memory Reliability Test (1)

Test Item	HM10480-15					HM2144CG				
	Test Conditions	Samples	Total Component Hours	Failures	Failure Rate* (1/Hr)	Test Conditions	Samples	Total Component Hours	Failures	Failure Rate* (1/Hr)
High-Temperature (Operating)	T_A = 125°C V_{EE} = −5.2V	340	C.H. 3.4×10^5	0	1/H 2.7×10^{-6}	T_A = 125°C V_{EE} = −5.2V	120	C.H. 1.2×10^5	0	1/H 7.7×10^{-6}
High-Temp Storage	T_A = 200°C	351	3.51×10^5	0	2.6×10^{-5}	T_A = 200°C	120	1.2×10^5	0	7.7×10^{-6}

* Confidence level 60%

• Table 4. Results on Bipolar Memory Reliability Test (2)

Test Item	Test Conditions	HM10480-15		HM2144CG	
		Samples	Failure	Samples	Failures
Temperature Cycling	−55°C to +150°C, 10 Cycle	160	0	180	0
Soldering Heat	260°C, 10 Seconds	35	0	22	0
Thermal Shock	0°C to +100°C, 10 Cycles	50	0	50	0
Mechanical Shock	1500G, 0.5 ms, Three Times Each for X, Y and Z	30	0	22	0
Variable Frequency	100 to 200 Hz, 20G, Three Times Each for X, Y and Z	40	0	22	0
Constant-Acceleration	20000G, 1 Minute, Each for X, Y and Z	40	0	22	0

2.2 Reliability Test Data on Hi-BiCMOS Memory

Hi-BiCMOS memory is newly designed based on the latest fine machining technologies (2m ~ 1m), which features low electric consumption/high integrity by CMOS and high speed/high drivability by bipolar. This device also attains high speed close to ECL and low electric consumption as CMOS. Input and output level supports both ECL and TTL. Reliability test data of HM100490-15 (64k-words x 1-bit) and HM6788P-25 (16k-words x 4-bits) are listed in Table 5 and Table 6.

The above shows the sufficient reliability of high speed Hi-BiCMOS in the normal use with some limitations considered from its own circuit composition. For further information, see each data sheet. Besides the caution points with CMOS and bipolar device, avoid abnormal use as in deformed or slow wave form which causes malfunction and latch up.

• Table 5. Results on Hi-BiCMOS Memory Reliability Test (1)

Test Item	HM100490-15 (Cerdip)					Test Item	HM6788P-25 (Plastic)					Remarks
	Test Conditions	Samples	Total Test Time	Failures	Failure Rate		Test Conditions	Samples	Total Test Time	Failures	Failure Rate	
High-Temperature Pulse Operation	T_A = 125°C V_{EE} = −4.5V	380	C.H. 3.8×10^5	0	1/H 2.4×10^{-6}	High-Temperature Pulse Operation	T_A = 125°C V_{CC} = 5.0V	420	C.H. 4.2×10^5	1*1	1/H 4.8×10^{-6}	*1 Foreign Matter
						Moisture Endurance	85°C 85% RH 5V	210	2.1×10^5	0	4.8×10^{-6}	
High-Temp. Storage	T_A = 200°C	330	3.3×10^5	0	3.0×10^{-6}	Pressure Cooker	121°C 100% RH	80	0.16×10^5	0	6.3×10^{-5}	

• Table 6. Results on Hi-BiCMOS Memory Reliability Test (2)

Test Item	Test Conditions	HM100490-15 (Cerdip)		HM6788P-25 (Plastic)	
		Samples	Failure	Samples	Failure
Temperature Cycling	− 55°C ~ − 150°C 100 Cycles	180	0	180	0
Soldering Heat	250°C 10 Seconds	22	0	22	0
Thermal Shock	0°C ~ 100°C 10 Cycles	50	0	50	0
Mechanical Shock	1500G, 0.5 ms Three Times Each for X, Y and Z	22	0	—	—
Variable Frequency	100 ~ 200 Hz, 20G Three Times Each for X, Y and Z	22	0	—	—
Constant Acceleration	20000G, 1 Minute Each for X, Y and Z	22	0	—	—

2.3 Reliability Test Data on MOS Memories

2.3.1 Reliability Test Data on MOS DRAM and SRAM

Table 7 and Table 8 shows the reliability test data on the representative types of 1M DRAM (HM511000/HM514256), 256k SRAM (HM62256) 1M SRAM (HM628128FP).

The life test is performed at high temperature and high voltage to evaluate the reliability of products using fewer samples. All failures are caused in manufacturing process, so we feedback the data into manufacturing process to improve the quality and reliability.

• Table 7. Reliability Data on 1M DRAM

Test Item	Test Conditions	HM511000P/HM514256P Series (DIP)				HM511000JP/HM514256JP Series (SOP)				Remarks
		Samples	Total Test Time	Failures	Failure Rate* (1/Hr)	Samples	Total Test Time	Failures	Failure Rate* (1/Hr)	
High-Temperature Pulse Operations	125°C/5.5V	300	6.00×10^5	0	1.53×10^{-6}	200	4.00×10^5	0	2.30×10^{-6}	
	125°C/7V	1252	4.50×10^5	1*	4.48×10^{-6}	3186	9.34×10^5	0	9.85×10^{-7}	
	150°C/7V	200	4.00×10^5	0	2.30×10^{-6}	200	4.00×10^5	0	2.30×10^{-6}	*1 Oxide Film Failure x1
Moisture Endurance	85°C 85% RH 5.5V	420	8.40×10^5	0	1.10×10^{-6}	682	1.36×10^6	0	6.74×10^{-7}	
Pressure Cooker	121°C/100% RH	150	4.50×10^4	0	2.04×10^{-5}	200	6.00×10^4	0	1.53×10^{-5}	

*Confidence level 60%

• Table 8. Reliability Data on 256k and 1M SRAM

Test Item	Test Conditions	HM62256FP (SOP)				HM628128FP (SOP)				Remarks
		Samples	Total Test Time	Failures	Failure Rate* (1/Hr)	Samples	Total Test Time	Failures	Failure Rate* (1/Hr)	
High-Temperature Pulse Operation	125°C/5.5V	3088	3.11×10^6	0	8.88×10^{-7}	1038	1.04×10^6	0	8.86×10^{-7}	
	125°C/7V	455	4.55×10^5	0	2.02×10^{-6}	951	5.33×10^5	1*1	3.79×10^{-6}	*1 Foreign x 2
	150°C/7V	103	1.00×10^5	1*1	2.02×10^{-5}	80	1.60×10^5	0	5.75×10^{-6}	
Moisture Endurance	85°C/85% RH 7V	680	6.80×10^5	0	1.35×10^{-6}	127	2.54×10^5	0	3.62×10^{-6}	*2 Leak x 1
Pressure Cooker	121°C/100% RH	320	6.40×10^4	1*2	3.16×10^{-5}	90	2.70×10^4	0	3.41×10^{-5}	

*Confidence level 60%

2.3.2 Reliablity Test Data on EPROM

EPROM has two types; conventional EPROM with transparent window and one time programmable ROM (OTPROM) packaged in plastic package. Table 9 shows reliability test data on the representative EPROM types 512k EPROM (HN27512, HN27512P), 1M EPROM (HN27C101, HN27C301).

• Table 9. Reliability Data on 512k and 1M EPROM

Test Item	Test Conditions	HN27512 (Cerdip/Plastic)				HN27C101/HN27C301				Remarks
		Samples	Total Test Time	Failures	Failure Rate* (1/Hr)	Samples	Total Test Time	Failures	Failure Rate* (1/Hr)	
High-Temperature Operation	125°C/5.5V	200	3.72×10^5	0	2.47×10^{-6}	180	3.24×10^5	0	2.84×10^{-6}	*1 Data Dissipation x 49
	125°C/7V	530	7.95×10^5	0	1.16×10^{-6}	327	6.54×10^5	0	1.41×10^{-6}	
High-Temperature Bake	175°C	260	4.91×10^5	0	1.87×10^{-6}	150	7.5×10^5	0	1.23×10^{-6}	
	200°C	240	3.72×10^5	1*1	5.43×10^{-6}	130	6.49×10^5	1*1	3.11×10^{-6}	
	250°C	180	1.89×10^5	7*1	4.44×10^{-5}	110	3.07×10^5	40*1	1.30×40^{-4}	
Moisture Endurance	85°C/85% RH 5.5V	290	5.22×10^5	0	1.76×10^{-6}	—	—	—	—	Data of 512k OTPROM
Pressure Cooker	121°C/100% RH	50	0.10×10^5	0	9.20×10^{-5}	—	—	—	—	

*Confidence level 60%

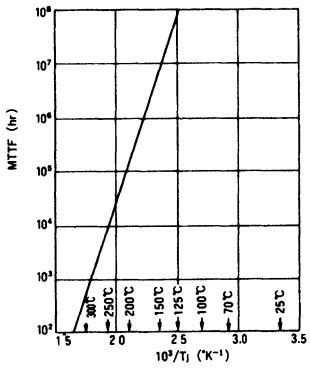
The failure shown in Table 9 is due to the data dissipation in memory cells. Getting thermal energy, electrons in memory cells are activated and go through the floating gate. In actual usage, however, it has no problem because this phenomenon depends on temperature (about 1.0 eV of activated energy) greatly. The moisture resistance of OTPROM is also satisfactory.

Table 10 shows the example of PROM derating. When derating, the parameter is generally only the temperature because other operating conditions are specified. Especially to lower the junction temperature during mounting is important for stabilizing the operation relative to access time, refresh time and other characteristics.

• Table 10. Example of HN27C101/HN27C301 Derating

Factor	Temperature
Failure Criteria	Electrical Characteristics, Function Test
Failure Mechanism	Increase of Leak Current and Others

Results:
The result from high temperature baking of PROM is shown in the right figure.



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Note: Decreasing junction temperature shown in the figure will promise the higher reliability. The junction temperature can be calculated by a formula: $T_J = T_A + \theta_{JA} \bullet P_J$ θ_{JA} in about 100°C/W with no air flow and about 60 to 70°C/W with 2.5 m/s air flow.

2.3.3 Reliability Data on MASK ROM

Table 9 shows the reliability test data on 2M and 4M bit MASK ROM. MASK ROM is patterned according to ROM information in manufacturing process, so data dissipation isn't occurred in high temperature like EPROM and EEPROM.

• Table 11. Reliability Data on 2M and 4M MASK ROM

Test Item	Test Conditions	HN62412P (Plastic)				HN62404P (Plastic)				Remarks
		Samples	Total Test Time	Failures	Failure Rate* (1/Hr)	Samples	Total Test Time	Failures	Failure Rate* (1/Hr)	
High-Temp. Pulse Operation	125°C/5.5V	—	—	—	—	200	4.0×10^5	0	2.3×10^{-6}	
	125°C/7V	120	1.2×10^5	0	7.67×10^{-6}	300	3.0×10^5	0	3.0×10^{-6}	
Moisture Endurance	85°C/85% RH 5.5V	120	1.2×10^5	0	7.67×10^{-6}	120	1.20×10^5	0	7.67×10^{-6}	
Pressure Cooker	121°C/ 100% RH	45	2.3×10^4	0	4.1×10^{-5}	45	2.3×10^4	0	4.1×10^{-5}	

*Confidence level 60%

2.3.4 Reliability Data on MOS Memory (The result of environment test)

Table 12 shows examples of each environment test data. They show good results without any failure even in severe environment.

V_{TH} of MOS transistor is one of the basic process parameters in MOS memory, which has almost no change using surface stabilization technology and clean process. Figure 4 shows the examples of time changes for 1M DRAM; V_{DD} min. (V_{min}) and access time (t_{RAC}) in high temperature pulse test.

• Table 12. Reliability Data on MOS Memories

Test Item	Test Conditions	HM511000P (DIP)		HM511000JP (SOJ)		HM62256FP (SOP)		HM62128FP (SOP)		EPROM (Cerdip)		Remarks
		Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	
Temperature Cycling	− 55°C to 150°C 10 Cycle	3755	0	2786	0	3328	0	710	0	2790	0	
Temperature Cycling	− 55°C to 150°C 500 Cycle	150	0	200	0	482	0	105	0	450	0	
Thermal Shock	− 65°C to 150°C 15 Cycle	77	0	100	0	76	0	77	0	80	0	
Soldering Heat	260°C, 10 Seconds	22	0	22	0	22	0	22	0	22	0	
Mechanical Shock	1,500G, 0.5 ms									38	0	
Variable Frequency	100 to 2,000 Hz 20G									38	0	
Constant-Acceleration	6000G									38	0	*6,000G

2.4 Change of Electrical Characteristics on IC Memory

The degradation of I_{CBO} and h_{FE} are the main factors of degradation in inner cell transistor of bipolar memory. In actual element designing, however, it is designed to operate in the range at which no degradation happen. Therefore no change of characteristics including access time are observed. Time dependence in access time for HM10470 are shown in Figure 1.

Example	
Device Name	HM10480-15
Test Conditions	T_A = 125°C, V_{EE} = −5.2V
Failure Criteria	t_{AA} = 15 ns
Failure Mechanism	Surface Degradation
Results: Access time is stabilized.	

Example of Time Change in Access Time for Bipolar Memory

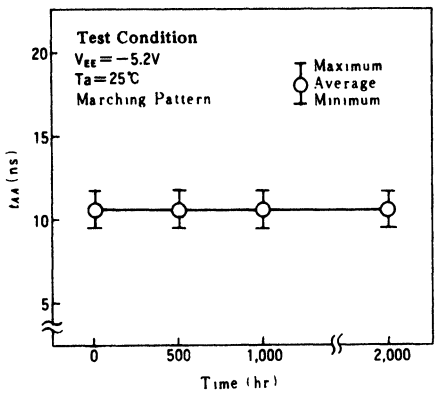

Figure 1. Time Change in Access Time for Bipolar Memory

Example	
Device Name	HM100490
Test Conditions	T_A = 125°C, V_{EE} = −4.5V All Bit Scanning
Failure Criteria	t_{AA} = 15 ns
Failure Mechanism	Surface Degradation
Results: Access time is stabilized.	

Example of Time Change in Access Time for Hi-BiCMOS Memory

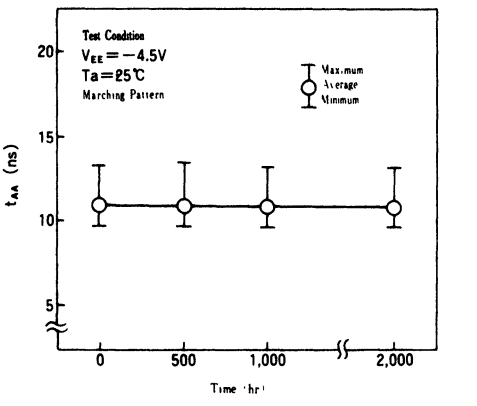

Figure 2. Time Change in Access Time for Hi-BiCMOS Memory

Example	
Device Name	HM6788P-25
Test Conditions	T_A = 125°C, V_{EE} = 5.0V All Bit Scanning
Failure Criteria	V_{CC} = 4.5V, t_{AA} = 25 ns
Failure Mechanism	Surface Degradation
Results: Both of V_{CC} (min) and t_{AA} are stabilized.	

Examples of Time Change in V_{CC} Min and t_{AA} for Hi-BiCMOS Memory

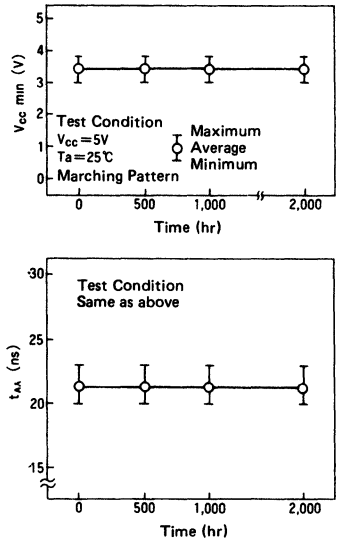

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Figure 3. Time Change in V_{CC} Min and t_{AA} for Hi-BiCMOS Memory

Example	
Device Name	HM511000P
Test Conditions	T_A = 125°C, V_{CC} = 7V All Bit Scanning
Failure Criteria	V_{DD} = 4.5V, ΔV_{DD} = 1.0V
Failure Mechanism	Surface Degradation
Results: Access time (t_{AA}) is stabilized and is within the failure criteria.	
Note: Test Accuracy is 0.2V, 2 ns.	

Example of Time Change in V_{DD} Min and t_{RAC} for MOS Memory

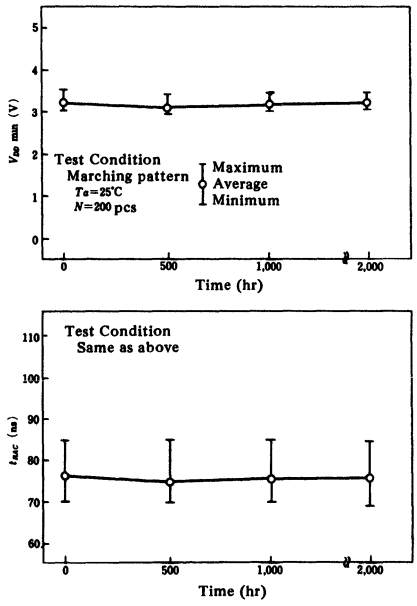

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Figure 4. Time Change in V_{DD} Min and t_{RAC} for MOS Memory

2.5 Failure Mode Rate

Figures 5 and 6 show examples of failure more happened in users' application. Since IC memories require the finest pattern process technology, the percentage of failures, such as pinholes, defects on photoresist and foreign materials, tends to increase. To eliminate the defects in the manufacturing process, Hitachi has improved the process and performed 100% burn-in screening under high temperature. Hitachi has been collecting and checking customers' process-data and marketing data for higher reliability of our products. To analyze them is very helpful for the improvement of designing and manufacturing.

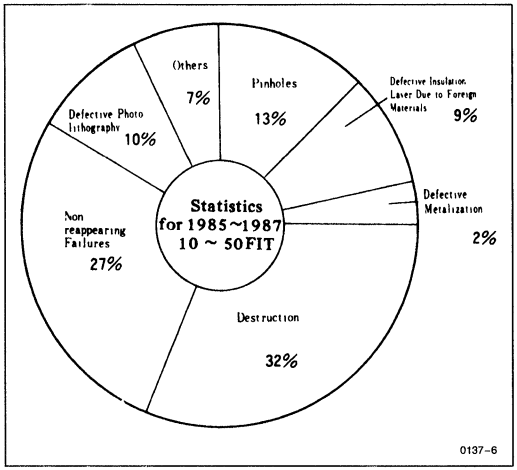

Figure 5. Failure Mode Rate of Bipolar Memory

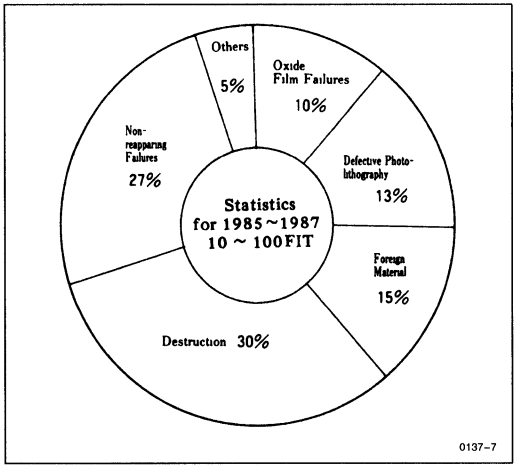

Figure 6. Failure Mode Rate of MOS Memory

3. RELIABILITY OF SEMICONDUCTOR DEVICES

3.1 Reliability Characteristics for Semiconductor Devices

Hitachi semiconductor devices are designed, manufactured and inspected so as to achieve a high level of reliability. Accordingly, system reliability can be improved by combining highly reliable components along proper environmental conditions. This section describes reliability characteristics, failure types and their mechanisms in terms of devices. First, semiconductor device characteristics are examined in light of their reliability.

(1) Semiconductor devices are essentially structure sensitive as seen in surface phenomenon. Fabricating the device requires precise control of a large number of process steps.

(2) Device reliability is partly governed by electrode materials and package materials, as well as by the coordination of these materials with the device materials.

(3) Devices employ thin-film and fine-processing techniques for metallization and bonding. Fine materials and thin film surfaces sometimes exhibit physically different characteristics from the bulks.

(4) Semiconductor device technology advances drastically: Many new devices have been developed using new processes over a short period of time. Thus, conventional device reliability data cannot be used in some cases.

(5) Semiconductor devices are characterized by volume production. Therefore, variations should be an important consideration.

(6) Initial and accidental failures are only considered to be semiconductor device failures based on the fact that semiconductor devices are essentially operable semipermanently. However, wear failures caused by worn materials and migration should also be reviewed when electrode and package materials are not suited for particular environmental conditions.

(7) Component reliability may depend on device mounting, conditions for use, and environment. Device reliability is affected by such factors as voltage, electric field strength, current density, temperature, humidity, gas, dust, mechanical stress, vibration, mechanical shock, and radiation magnetic field strength.

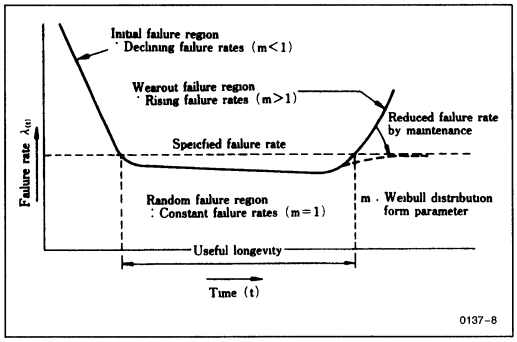

Figure 7. Typical Failure Rate Curve

Device reliability is generally represented by the failure rate. "Failure" means that a device loses its function, including intermittent degradation as well as complete destruction.

Generally, the failure rate of electric components and equipment is represented by the bathtub curve shown in Figure 7. For semiconductor devices, the configuration parameter of the Weibull distribution is smaller than 1, which means an initial failure type. Such devices ensure a long lifetime unless extreme environmental stress is applied. Therefore, initial and accidental failures can become a problem for semiconductor devices. Semiconductor device reliability can be physically represented as well as statistically. Both aspects of failures have been thoroughly analyzed to establish a high level of reliability.

3.2 Failure Types and Their Mechanisms

3.2.1 Failure Physics

Failure physics is, in a broad sense, a basic technology of "physics + engineering". It is used to examine the physical mechanism of failures in terms of atoms and molecules to improve device reliability. This physical approach was introduced to the reliability field with the demand for minimized development cost and period, as technology rapidly developed and system performance increased, requiring more complex and higher levels of reliability. These conditions derived from the development of solid state physics (semiconductor physics) after World War II and associated device development. Failure physics have been employed to:

1) Detect failed devices as soon as possible

2) Establish models and equation used for failure prediction

3) Evaluate reliability in short periods by accelerated life test

The purpose of the failure physics approach is to contribute to reliability related fields such as product design, prediction, test, storage and usage by adding physics as a basic technology to conventional experimental and statistical approaches.

3.2.2 Failure Types and Their Mechanism

Device failures are physically discussed in this section. Semiconductor device failures are basically categorized as disconnection, short-circuit, deterioration and miscellaneous failures. These failures and their causes are summarized in Table 11. Typical failure mechanisms are reviewed next.

(1) Surface Deterioration

The pn junction has a charge density of $10^{14} - 10^{20}/cm^3$. If charges exceeding the above density are accumulated on the pn junction surface, particularly adjacent to a depletion layer, electric characteristics of the junction tend to be easily varied. Although the surface of such devices as planar transistors is generally covered with a SiO_2 film and is in an inactive state, the possibility of deterioration caused by surface channels still exists. Surface deterioration depends heavily on applied temperature and voltage and is often handled by the reaction model.

One example of recent failures is surface deterioration caused by hot carriers. Hot carriers are generated when such devices as MOS dynamic RAMs are operated at a voltage near the minimum breakdown voltage BV_{DS} by raising internal voltage and when a strong electric field is established near the MOS device's drain resulting from reduced device geometry from 2 μm to 0.8 μm. Generated hot carriers may affect surface boundary characteristics on a part of the gate oxide film, resulting in degradation of threshold voltage (V_{TH}) and counter conductance (gm). Hitachi devices have employed improved design and process techniques to prevent these problems. However, as process becomes finer, surface deterioration may possibly become a serious problem.

(2) Electrode-Related Failures

Electrode-related failures have become increasingly important as multi-layer wiring has become more complicated. Noticeable failures include electro-migration and Al wiring corrosion in plastic sealed packages.

① Electromigration

This is a phenomenon in which metal atoms are moved by a large current of about 10^6 A/cm^2 supplied to the metal. When ionized atoms collide with current of about scattering electrons, an "electron wind" is produced. This wind moves the metal atoms in the opposite direction from the current flow, which generates voids at a negative electrode, and hillock and whiskers at an opposite one. The generated voids increase wiring resistance and cause excessive currents to flow in some areas, leading to disconnection. The generated whiskers may cause shortcircuits in multi-metal line.

② Multi-Metal Line Related Failures

Major failures associated with multi-metal line include increased leak currents, shortcircuits caused by a failed dielectric interlayer, and increased contact metal resistance and disconnection between metal wirings.

③ Al Line Corrosion and Disconnection

When Plastic encapsulated devices are subjected to high-temperatures, high-humidity or a bias-applied condition, Al electrodes in devices can cause corrosion or disconnection (Figure 8). Under high-temperature and high-humidity, corro-

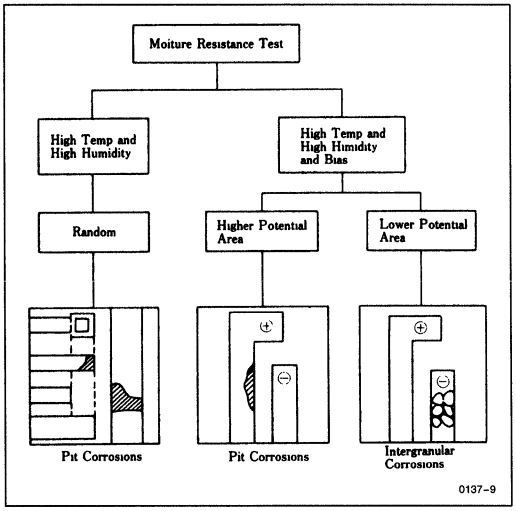

Figure 8. Categorized Al Corrosion Mode

sions are randomly generated over the element surface. However, after an extended period of time, the corrosions have not significantly increased. Accordingly, this failure is possibly due to an initial failure associated with manufacturing. It is also verified that this type of failure can be generated when the adhesion surface between an element and resin is separated or when foreign materials are attached to the element with human saliva. Under a bias-applied, high-temperature, high-humidity condition, on the other hand, corrosions are generated in higher potential areas while in lower potential areas, grain corrosion occurs. Once this failure occurs in part of a device, the device can become worn out in a relatively short time. This failure proves to depend on the hydroscopic volume resistivity of sealed resin. The Al line corrosion mechanism described above is summarized in Figure 9.

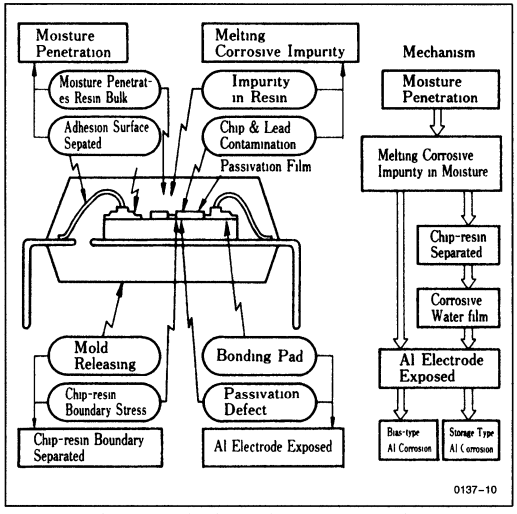

Figure 9. Plastic Package Cross Section and Al Corrosion Mechanism

(3) Bonding Related Failures

① Degradation Caused by Intermetallic Formation

Bonding strength degradation and contact resistance increase are caused by compounds formed in connections between Au wire and Al film or between Au film and Al Wire. These are the most serious problems in terms of reliability. The compounds are formed rapidly during bonding and are increased through thermal treatment. Consequently, Hitachi products are subjected to a lower-temperature, shorter-period bonding whenever possible.

② Wire Creep

Wire creep is wire neck destruction in an Au ball along an integranular system occurring when a plastic sealed device is subjected to a long-term thermal cycling test. This failure results from increased crystal grains due to heat application when forming a ball at the top of an Au wire, or from an impurity introducing to the intergranular system. Bonding under usual conditions with no loop configuration failures does not cause this failure unless a severe long-term thermal cycling test is applied. Accordingly, wire creep is not a problem in actual usage.

③ Chip Crack

With the increase in chip size associated with the increased number of incorporated functions, more problems have been occurring during assembly, such as chip cracks during bonding. Bonding methods include Au-silicon eutectic, soldering and Ag-paste. Soldering and Ag-paste exhibit few chip crack problems. For Au-silicon eutectic, in contrast, large stress is applied to a pellet due to its strength and high temperature resistance for attachment, which may result in critical chip defects. Today, the chip destruction limit can be determined by finite-element analysis and by distortion measurement using a fine accuracy gauge. Ideally, Au-silicon eutectic should be evenly applied over the entire surface. However, this is difficult due to the existence of a silicon oxide film on the silicon back surface. Therefore, specifications for Au-silicon eutectic have been established based on stress analysis and thermal cycling test results.

④ Reduced Maximum Power Dissipations

For power devices, heat fatigue due to thermal expansion coefficient mismatch among different materials deteriorates thermal resistance. This results in decreased maximum power dissipations.

(4) Sealing Related Failures

Hermetic sealing packages, including metal, glass, ceramic, and all other types, have the possibility of the following failures.

1. Al line corrosion on the chip surface due to slight moisture and reaction between the different ionized materials.
2. Intermittent moving foreign metals short
3. Al line corrosion due to extraneous H_2O caused by hermetic failure

Moving foreign matter, even if it is a non-active solid, can be charged up within a cavity during movement, thereby inducing parasitic effects and metal shorts. The foreign matter detection method is specified by MIL-STD-883C, PIND (Particle Impact Noise Detection) Test. The PIND test consists of filtering a particle impact waveform (ultrasonic waveform), detecting it with a microphone, and then amplifying.

(5) Disturbance

① Electrostatic Discharge Destruction

Destruction caused by electrostatic discharge is a problem common to semiconductor devices. A recent report introduced three modes of this failure; the human body model, charged device model and field induced model.

The human body is easily charged. A person just walking across a carpet can be charged up to 15000V. This voltage is high enough to destroy a device. An equivalent circuit of the human body model is shown in Figure 10. The human body's capacitance Cb and resistance Rb are 100 to 200 pF and 1000 to 2000Ω, respectively. Assuming a body is charged with 2000V, the dissipated energy is obtained as follows: With a time constant of 10^{-7} sec, the dissipated energy is 2 KW, which is enough to destroy a small area of a chip.

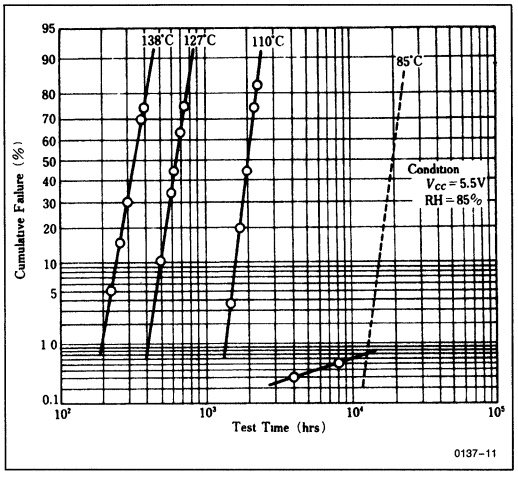

Figure 10. An Example of Moisture Resistance by High Temp. and High Humidity and Bias

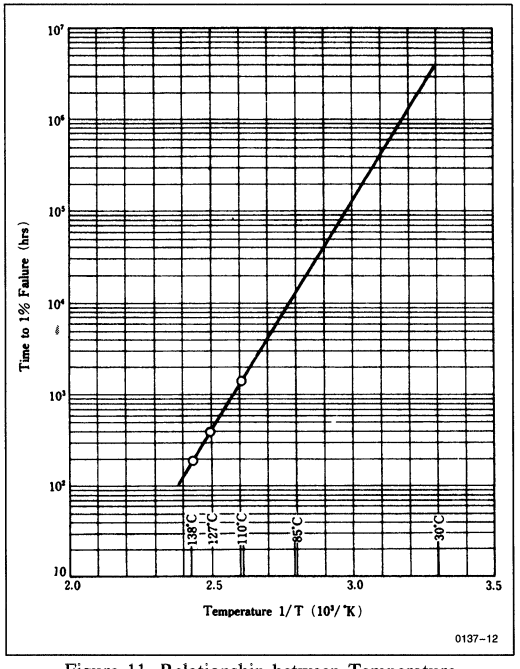

Figure 11. Relationship between Temperature and Time to 1% Failure (RH = 85%)

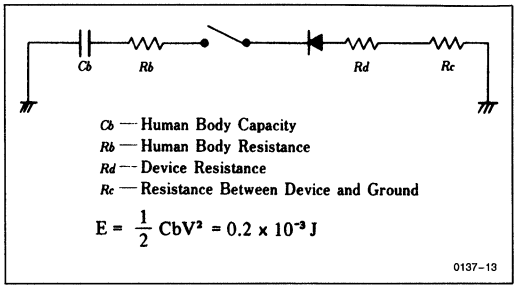

Figure 12. Equivalent Circuit of Human Body Model

In the charged device model, charges are accumulated in a device, not a human body, and discharged through contact resistance during a short time. The equivalent circuit of this model is shown in Figure 13. Device size and device position relative to GND are important parameters in this model since the model depends on device capacity.

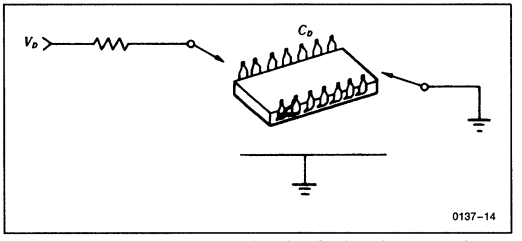

Figure 13. Equivalent Circuit of Charging Model

In the field induced model a device is left under a strong electric field or is affected by neighboring high voltage material. Since the capacitor of device or lead of device acts like an antenna, the following cases will possibly cause destruction. 1) a device is incorporated into a high electric field such as a CRT, 2) a device is left under a high frequency electric field and 3) a device is moved with a container charged at high voltage, such as a tube.

② Latch Up

Latch up is a problem unique to CMOS devices. This problem is a thyristor phenomenon caused by a parasitic PNP or NPN transistor formed in the CMOS configuration. Latch up occurs when an accidental surge voltage exceeding a maximum rating, a power supply ripple, an unregulated power supply and noise is applied, or when a device is operated from two sources having different set-up voltages. These cases can cause input or output current to flow in the opposite direction from usual flow, which triggers parasitic thyristors. This results in excessive current flowing between a power supply and ground. This phenomenon continues until the power is off or the flowing current is forced to be reduced to a certain level. Once latch up occurs in an operating device, the device will be destroyed.

Much effort should be made in designing circuits to prevent latch up. Latch up triggering input or output currents start to flow under the following conditions.

$V_{in} < V_{CC}$ or $V_{in} <$ GND for input level

$V_{out} > V_{CC}$ or $V_{out} <$ GND for input level

Therefore, circuits should be designed so that no forward current flows through the input protection diodes or output parasitic diodes.

③ Soft Errors

When α particles are generated from uranium or thorium in a package the silicon surface of an LSI chip, electron-hole pairs are formed which act as noise to data lines and other floating nodes, causing temporary soft errors. This phenomenon is shown in Figure 14. Only electrons from among the electron-hole pairs are only collected to a memory cell. As a result, the cell changes from a state of 1 to 0, which is a soft error.

Hitachi devices have been subjected to simulation and irradiation tests to prevent soft errors. In some cases, organic material, PIQ, is applied to the surface of the device.

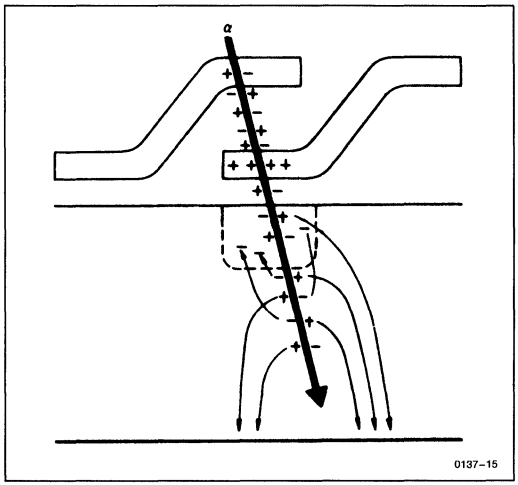

Figure 14. Soft Error Caused by α Particles in Dynamic Memory

• Table 13. Failure Causes and Mechanism

Failure Related Causes		Failure Mechanisms	Failure Modes
Passivation	Surface Oxide Film, Insulating Film between Wires	Pin Hole, Crack, Uneven Thickness, Contamination, Surface Inversion, Hot Carrier Injected	Withstanding Voltage Reduced, Short, Leak Current Increased, h_{FE} Degraded, Threshold Voltage Variation, Noise
Metallization	Interconnection, Contact, Through Hole	Flaw, Void, Mechanical Damage, Break Due to Uneven Surface, Non-ohmic Contact, Insufficient Adhesion Strength, Improper Thickness, Electromigration, Corrosion	Open, Short, Resistance Increased
Connection	Wire Bonding, Ball Bonding	Bonding Runout, Compounds between Metals, Bonding Position Mismatch, Bonding Damaged	Open, Short Resistance Increased
Wire Lead	Internal Connection	Disconnection, Sagging, Short	Open, Short
Diffusion, Junction	Junction Diffusion, Isolation	Crystal Defect, Crystallized Impurity, Photo Resist Mismatching	Withstanding Voltage Reduced, Short
Die Bonding	Connection between Die and Package	Peeling Chip, Crack	Open, Short, Unstable Operation, Thermal Resistance Increased
Package Sealing	Packaging, Hermetic Seal, Lead Plating, Hermetic Package and Plastic Package, Filler Gas	Integrity, Moisture Ingress, Impurity Gas, High Temperature, Surface Contamination, Lead Rust, Lead Bend, Break	Short, Leak Current Increased, Open, Corrosion Disconnection, Soldering Failure
Foreign Matter	Foreign Matter in Package	Dirt, Conducting Foreign Matter, Organic Carbide	Short, Leak Current Increased
Input/Output Pin	Electrostatistics, Excessive Voltage, Surge	Electron Destroyed	Short, Open, Fusing
Disturbance	α Particle	Electron Hole Generated	Soft Error
	High Electric Field	Surface Inversion	Leak Current Increased

(6) Fine Geometry Related Problems

In response to higher integration requirements for memories and microcomputers, LSI geometry has been reduced in the way of 3 μm $\rightarrow$ 2 μm $\rightarrow$ 1.3 μm $\rightarrow$ 0.8 μm. However power supply has not been scaled down used for 5V, only line dimensions have been fined increasingly. Problems associated with finer geometry are shown in Table 14.

• Table 14. Finer Geometry Related Problems

Item	Problems	Countermeasure
5V Single Supply Voltage	• Breakdown Voltage of Gate Oxide Films • SiO_2 Defects	Oxide Film Formation Process Improved • Cleaning • Gettering • Screening
Horizontal Dimension Reduction	• Soft Errors by α Particles • Al Reliability Reduced • CMOS Latch Up • Mask Alignment Margin Reduced • Hot Carriers	Surface Passivation Film Improved • Metallization Improved • Design/Layout Improved • Process Improved
Vertical and Horizontal Dimension Reduction	• Higher Breakdown Voltage Not Permitted • Electrostatic Discharge Resistance Reduced	Use of Low Voltage Examined • Configuration Improved • Protection Circuits Enhanced

■ QUALITY ASSURANCE OF IC MEMORY

1. VIEWS ON QUALITY AND RELIABILITY

Hitachi basic views on quality are to meet individual users' purpose and their required quality level and also to maintain the satisfied level for general application. Hitachi has made efforts to assure the standardized reliability of our IC memories in actual usage. To meet users' requests and to cover expanding application, Hitachi performs the following:

(1) Establish the reliability in design at the stage of new product development.

(2) Establish the quality at all steps in manufacturing process.

(3) Intensify the inspection and the assurance of reliability of products.

(4) Improve the product quality based on marketing data.

Furthermore, to get higher quality and reliability, we cooperate with our research laboratories.

With the views and methods mentioned above, Hitachi makes the best efforts to meet the users' requirements.

2. RELIABILITY DESIGN OF SEMICONDUCTOR DEVICES

2.1 Reliability Target

Establishment of reliability target is important in manufacturing and marketing as well as function and price. It is not practical to determine the reliability target based on the failure rate under single common test condition. So, the reliability target is determined based on many factors such as each characteristics of equipment, reliability target of system, derating applied in design, operating condition and maintenance.

2.2 Reliability Design

Timely study and execution are essential to achieve the reliability based on reliability targets. The main items are the design standardization, device design including process and structural design, design review and reliability test.

(1) Design Standardization

Design standardization needs establishing design rules and standardizing parts, material, and process. When design rules are established on circuit, cell, and layout design, critical items about quality and reliability should be examined. Therefore, in using standardized process or material, even newly developed products would have high reliability, with the exception of special requirement on function.

(2) Device Design

It is important for device design to consider total balance of process design, structure design, circuit and layout design. Especially in case of applying new process or new material, we study the technology prior to development of the device in detail.

(3) Reliability Test by Test Site

Test site is sometimes called Test Pattern. It is useful method for evaluating reliability of designing and processing ICs with complicated functions.

1. Purposes of Test Site are as follows:
   - Making clear about fundamental failure mode.
   - Analysis of relation between failure mode and manufacturing process condition.
   - Analysis of failure mechanism.
   - Establishment of QC point in manufacturing.
2. Effects of evaluation by Test Site are as follows:
   - Common fundamental failure mode and failure mechanism in devices can be evaluated.
   - Factors dominating failure mode can be picked up, and compared with the process having been experienced in field.
   - Able to analyze relation between failure causes and manufacturing factors.
   - Easy to run tests.

2.3 Design Review

Design review is a method to confirm systematically whether or not design satisfies the performance required including by users, follows the specified ways, and whether or not the technical items accumulated in test data and application data are effectively applied.

In addition, from the standpoint of competition with other products, the major purpose of design review is to insure quality and reliability of the product. In Hitachi, design review is performed in designing new products and also in changing products.

The followings are the itmes to consider at design review.

(1) Describe the products based on specified design documents.

(2) Considering the documents from the standpoint of each participant, plan and execute the sub-program such as calculation, experiments and investigation if unclear matter is found.

(3) Determine the contents and methods of reliability test based on design document and drawing.

(4) Check process ability of manufacturing line to achieve design goal.

(5) Arrange the preparation for production.

(6) Plan and execute the sub-programs of design changes proposed by individual specialists, for tests, experiments and calculation to confirm the design change.

(7) Refer to the past failure experiences with similar devices, confirm the prevention against them, and plan and execute the test program for confirmation of them.

In Hitachi, these study and decision at design review are made using the individual check lists according to its objects.

3. QUALITY ASSURANCE SYSTEM OF SEMICONDUCTOR DEVICES

3.1 Activity of Quality Assurance

The following items are the general views of overall quality assurance in Hitachi;

(1) Problems are solved in each process so that even the potential failure factors will be removed at final stage of production.

(2) Feedback of information is made to insure satisfied level of process ability.

As the result, we assure the reliability.

3.2 Qualification

To assure the quality and reliability, the qualification tests are done at each stage of trial production and mass production based on the reliability design described in Section 2.

The following are the views on qualification in Hitachi:

(1) From the standpoint of customers, qualify the products objectively by a third party.

(2) Consider the failure experiences and data from customers.

(3) Qualify every change in design and work.

(4) Qualify intensively on parts and materials and process.

(5) Considering the process ability and factor of manufacturing fluctuation, establish the control points in mass production.

Considering the views mentioned above, qualification shown in Figure 1 is done.

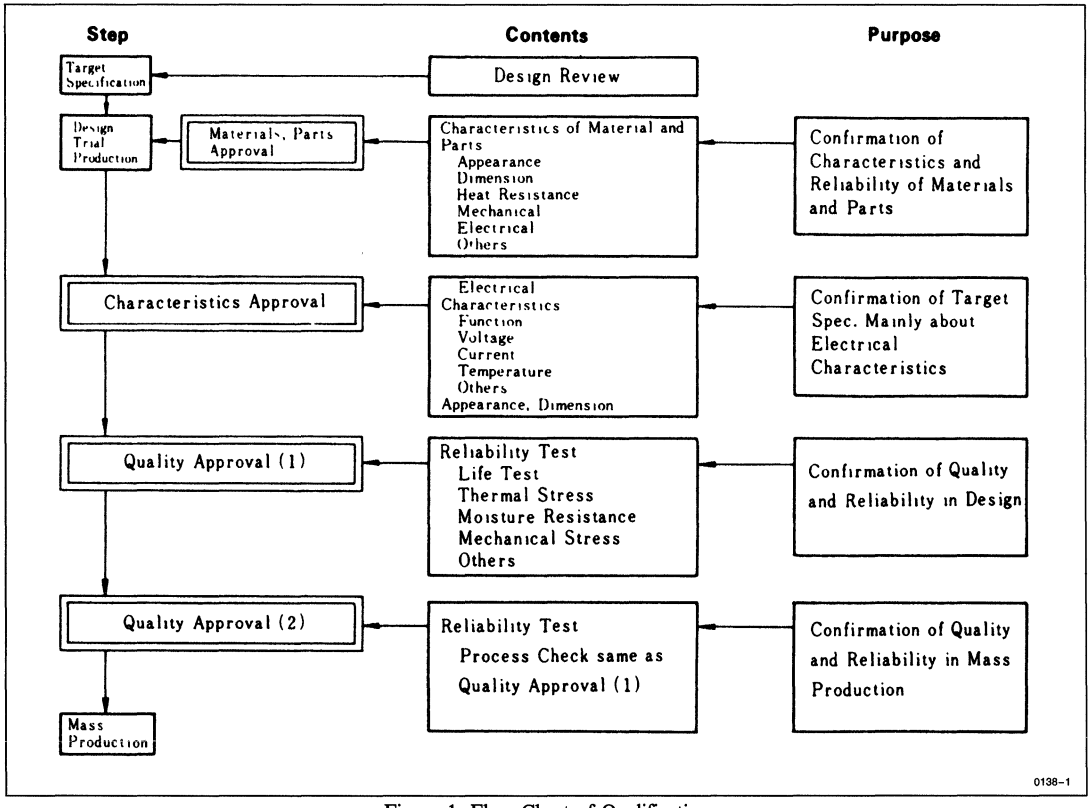

Figure 1. Flow Chart of Qualification

3.3 Quality and Reliability Control in Mass Production

To assure quality in mass production, quality is controlled functionally by each department, mainly by manufacturing department and quality assurance department. The total function flow is shown in Figure 2.

3.3.1 Quality Control on Parts and Materials

With the tendency toward higher performance and higher reliability of devices, quality control of parts and materials becomes more important. The terms such as crystal, lead frame, fine wire for wire bonding, package and materials required in manufacturing process like mask pattern and chemicals, are all subject to inspection and control.

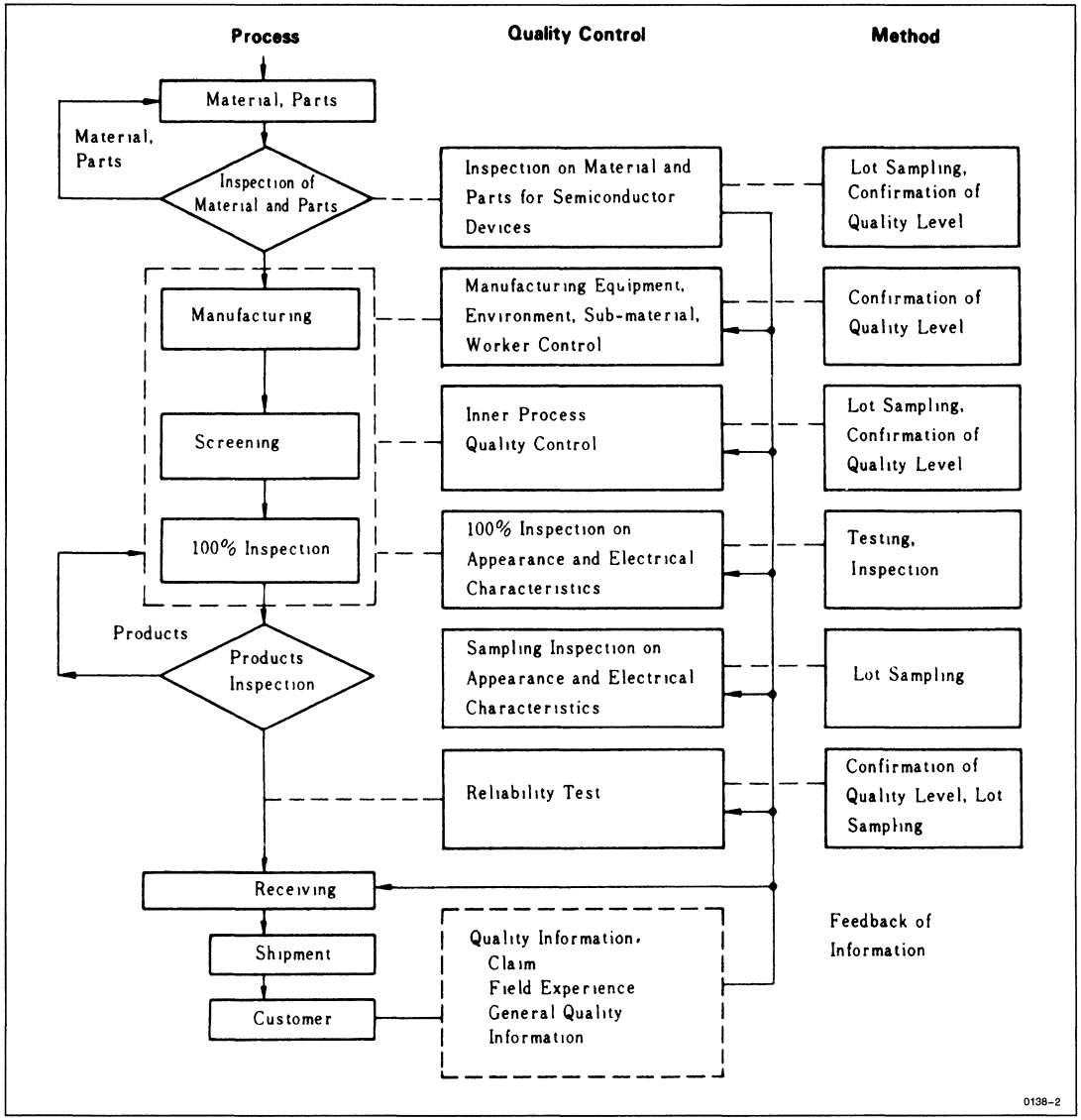

Figure 2. Flow Chart of Quality Control in Manufacturing Process

Besides qualification of parts and materials stated in 3.2, quality control of parts and materials is defined in incoming inspection. Incoming inspection is performed based on its purchase specification, drawing and mainly sampling test based on MIL-STD-105D.

The other activities for quality assurance are as follows:

(1) Technology Meeting with Vendors

(2) Approval and Guidance of Vendors

(3) Analysis and tests of physical chemistry

The typical check points of parts and materials are shown in Table 1.

• Table 1. Quality Control Check Points of Parts and Material (example)

Material Parts	Important Control Items	Point for Check
Wafer	Appearance	Damage and Contamination on Surface
	Dimension	Flatness
	Sheet Resistance	Resistance
	Defect Density	Defect Numbers
	Crystal Axis	
Mask	Appearance	Defect Numbers, Scratch
	Dimension	Dimension Level
	Resistoration	
	Gradation	Uniformity of Gradation
Fine Wire for Wire Bonding	Appearance	Contamination, Scratch, Bend, Twist
	Dimension	
	Purity	Purity Level
	Elongation Ratio	Mechanical Strength
Frame	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Processing Accuracy	
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
Ceramic Package	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Leak Resistance	Airtightness
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
	Electrical Characteristics	
	Mechanical Strength	Mechanical Strength
Plastic	Composition	Characteristics of Plastic Material
	Electrical Characteristics	
	Thermal Characteristics	
	Molding Performance	Molding Performance
	Mounting Characteristics	Mounting Characteristics

3.3.2 Inner Process Quality Control

To control inner process quality is very significant for quality assurance of devices. The quality control of products in every stage of production is explained below. Figure 3 shows inner process quality control.

(1) Quality Control of Products in Every Stage of Production

Potential failure factors of devices should be removed in manufacturing process. Therefore, check points are set up in each process so as not to move the products with failure factors to the next process. Especially, for high reliability devices, manufacturing lines are rigidly selected in order to control the quality in process. Additionally we perform rigid check per process or per lot, 100% inspection in proper processes so as to remove failure factors caused by manufacturing fluctuation, and screenings depending on high temperature aging or temperature cycling. Contents of controlling quality under processing are as follows:

- Control of conditions of equipment and workers and sampling test of uncompleted products.
- Proposal and execution of working improvement.
- Education of workers
- Maintenance and improvement of yield
- Picking up of quality problems and execution of countermeasures toward them.
- Communication of quality information.

(2) Quality Control of Manufacturing Facilities and Measuring Equipment

Manufacturing facilities have been developed with the need of higher devices in performance and the automated production. It is also important to determine quality and reliability.

In Hitachi, automated manufacturing is promoted to avoid manufacturing fluctuation, and the operation of high performance equipment is controlled to function properly.

As for maintenance inspection for quality control, daily and periodically inspections are performed based on specification on every check point.

As for adjustment and maintenance of measuring equipment, the past data and specifications are clearly checked to keep and improve quality.

(3) Quality Control of Manufacturing Circumstances and Submaterial.

Quality and reliability of devices are affected especially by manufacturing process. Therefore, we thoroughly control the manufacturing circumstances such as temperature, humidity, dust, and the sub-materials like gas or pure water used in manufacturing process.

Dust control is essential to realize higher integration and higher reliability of devices. To maintain and improve the clearness of manufacturing site, we take care of buildings, facilities, air-conditioning system, materials, clothes and works. Moreover, we periodically check on floating dust in the air, fallen dust or dirtiness on floor.

Process	Control Point		Purpose of Control
▽ Purchase of Material			
Wafer	Wafer	Characteristics, Appearance	Scratch, Removal of Crystal Defect Wafer
○ Surface Oxidation	Oxidation		Assurance of Resistance
□ Inspection on Surface Oxidation		Appearance, Thickness of Oxide Film	Pinhole, Scratch
○ Photo Resist	Photo Resist		
□ Inspection on Photo Resist		Dimension, Appearance	Dimension Level
◇ PQC Level Check			Check of Photo Resist
○ Diffusion	Diffusion	Diffusion Depth, Sheet Resistance	Diffusion Status
□ Inspection on Diffusion		Gate Width	Control of Basic Parameters (V_{TH}, etc) Cleaness of surface, Prior Check of V_{TH} Breakdown Voltage Check
◇ PQC Level Check		Characteristics of Oxide Film Breakdown Voltage	
○ Evaporation	Evaporation	Thickness of Vapor Film, Scratch, Contamination	Assurance of Standard Thickness
□ Inspection on Evaporation			
◇ PQC Level Check			
□ Wafer Inspection	Wafer	Thickness, V_{TH} Characteristics	Prevention of Crack, Quality Assurance of Scribe
□ Inspection on Chip Electrical Characteristics	Chip	Electrical Characteristics	
○ Chip Scribe		Appearance of Chip	
□ Inspection on Chip Appearance			
◇ PQC Lot Judgement			
Frame			
○ Assembling	Assembling	Appearance after Chip Bonding	Quality Check of Chip Bonding
		Appearance after Wire Bonding	Quality Check of Wire Bonding
◇ PQC Level Check		Pull Strength, Compresion Width, Shear Strength	Prevention of Open and Short
□ Inspection after Assembling		Appearance after Assembling	
◇ PQC Lot Judgement			
Package			
○ Sealing	Sealing	Appearance after Sealing Outline, Dimension	Guarantee of Appearance and Dimension
◇ PQC Level Check	Marking	Marking Strength	
○ Final Electrical Inspection			
◇ Failure Analysis		Analysis of Failures, Failure Mode, Mechanism	Feedback of Analysis Information
□ Appearance Inspection			
△ Sampling Inspection on Products			
○ Receiving			
Shipment			

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Figure 3. Example of Inner Process Quality Control

3.3.3 Final Tests and Reliability Assurance

(1) Final Tests

Lot inspection is done by quality assurance department for the product passed in 100% test in final manufacturing process. Though 100% of passed products is expected, sampling inspection is subjected to prevent mixture of failed products by mistake.

The inspection is executed not only to confirm that the products meet users' requirement, but to consider potential factors. Our lot inspection is based on MIL-STD-105D.

(2) Reliability Assurance Tests

To assure reliability, the reliability tests are performed periodically, and performed on each manufacturing lot if user requires.

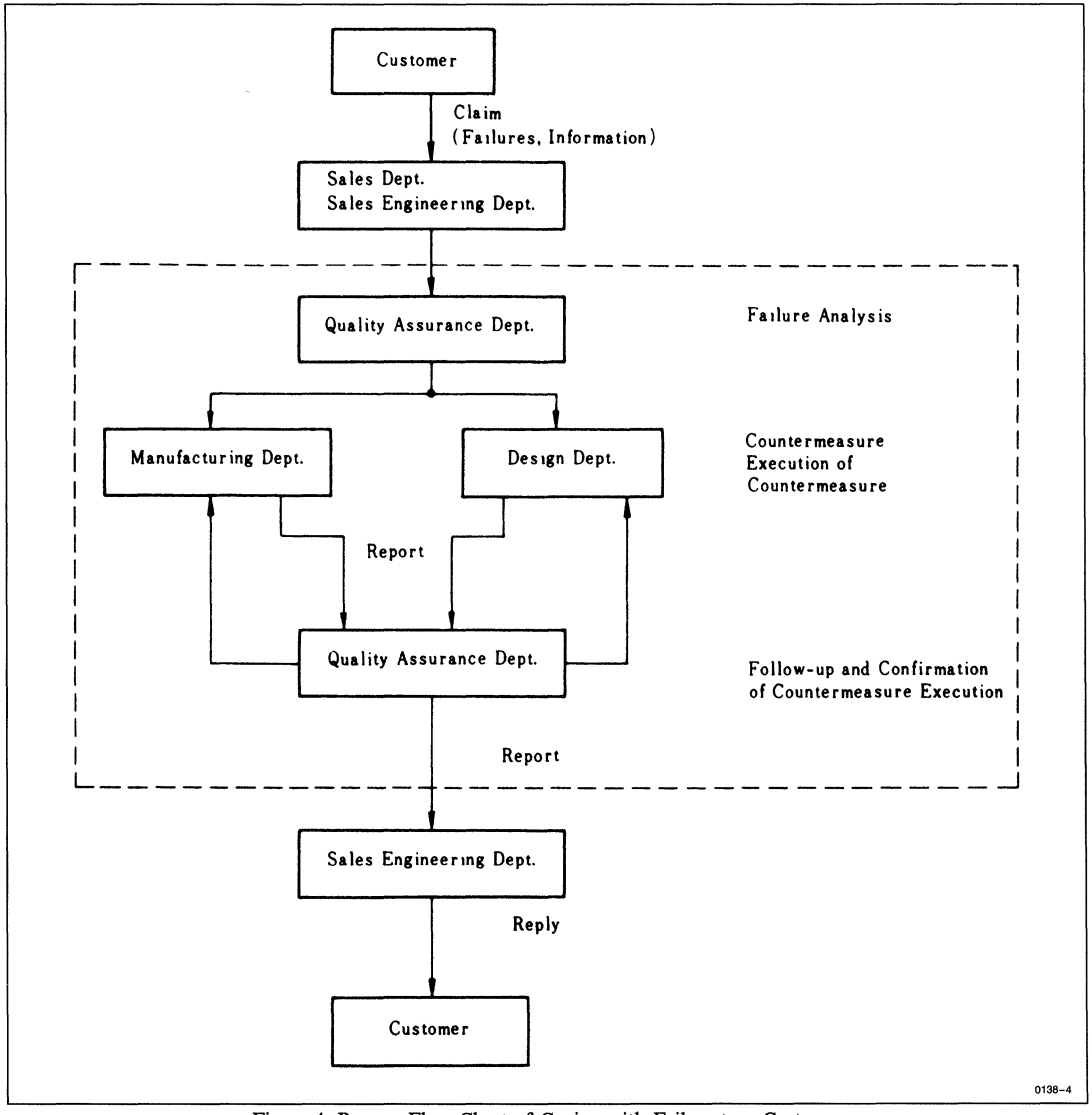

Figure 4. Process Flow Chart of Coping with Failure to a Customer

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■ OUTLINE OF TESTING METHOD

1. INSPECTION METHOD

Compared to conventional core memories, IC memories contain all peripheral circuits, such as the decoder circuit, write circuit and read circuit. As a result, assembly and electrical inspection of ICs are all performed by IC manufacturers. Consequently, as the electrical inspection of IC memories are becoming more systematic, conventional IC inspection facilities are becoming useless. This has led to the development and introduction of a memory tester with pattern generator to generate the inspection pattern of the memory IC at high speed. A function test for such as TTL gates can be performed even by a simple DC parameter facility. However, when the address input becomes multiplexed as in 16k, 64k and 256k memory, even the generation of the function test pattern becomes a serious problem.

In the memory IC inspection, its quality cannot be judged by DC test on external pins only, because the number of the element such as transistor which can be judged in the DC test is only 1/1000 of all elements. The following are the address patterns proposed to inspect whether the internal circuits are functioning correctly.

(1) All "Low", All "High"
(2) Checker Flag
(3) Stripe Pattern
(4) Marching Pattern
(5) Galloping
(6) Waling
(7) Ping-Pong

Those are not all, but only representative ones. There are the pattern to check the mutual interference of bits and the pattern for the maximum power dissipation. Among the above mentioned patterns, those of (1) to (4) are called N pattern, which can check one sequence of N bit IC memory with the several times of N patterns at most. Those of (5) to (7) are called N^2 pattern, which need several times of N^2 patterns to check one sequence of N bit IC memory. Serious problem arises in using N^2 pattern in a large-capacity memory. For example, inspection of 16k memory with galloping pattern takes a lot of time = about 30 minutes. (1), (2) and (3) are rather simple and good methods, however, they are not perfect to find any failure in decoder circuits. Marching is the most simple and necessary pattern to check the function of IC memories.

2. MARCHING PATTERN

The marching pattern, as its name indicates, is a pattern in which "1"s march into all bits of "0"s. For example, a simple addressing of 16-bit memory is described below.

(1) Clear all bits .....See Fig. 1 (a)
(2) Read "0" from 0th address and check that the read data is "0". Hereafter, "Read" means "checking and judging data"
(3) Write "1" on 0th address .....See Fig. 1 (b)
(4) Read "0" from 1st address.
(5) Write "1" on 1st address.
(6) Read "0" from nth address.
(7) Write "1" on nth address .....See Fig. 1 (c)
(8) Repeat (6) to (7) to the last address. Finally, all data will be "1".
(9) After all data become "1", repeat from (2) to (8) replacing "0" and "1".

In this method, 5N address patterns are necessary for the N-bit memory.

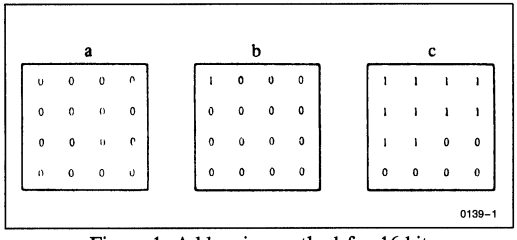


Figure 1. Addressing method for 16-bit memory in the Marching pattern

■ APPLICATION

1. VIDEO RAM

1.1 Multiport Video RAM

Figure 1-1 shows general idea of video RAM. Multiport video RAM provides an internal data register (SAM) with the memory (RAM). Both of them can be accessed asynchronously.

Effective graphic display memory is realized by using the random port of the RAM part for graphic processor drawing and the serial port of the SAM part for CRT display.

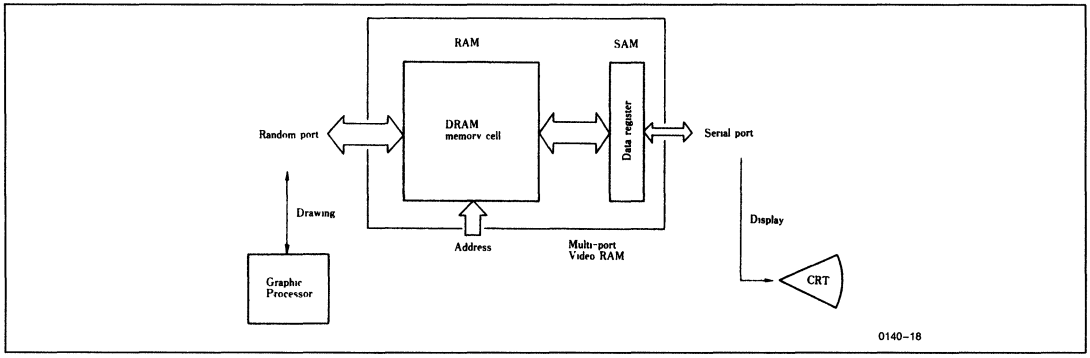


Figure 1-1. General Idea of Multi-Port Video RAM

Figure 1-2 shows the block diagram of the 256-kbit multiport video RAM HM53461, and Table 1-1 shows the operation modes of the HM53461.

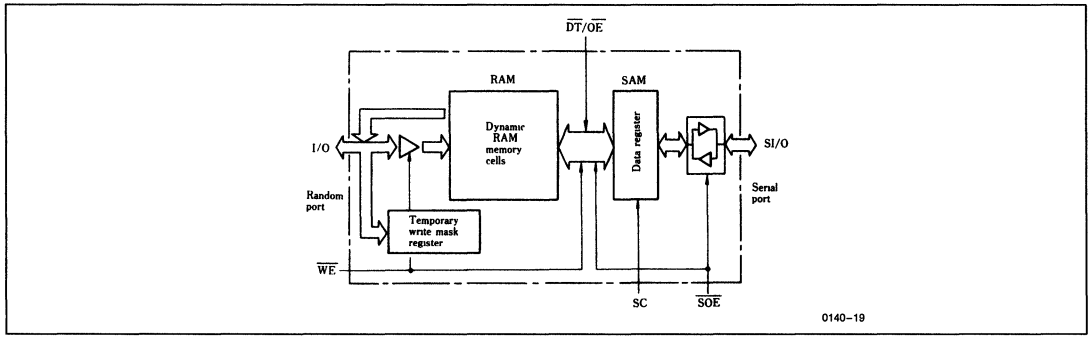


Figure 1-2. Block Diagram of HM53461

The operation modes shown in Table 1-1 are described as follows.

• Table 1-1. Operation Modes of HM53461

At the Falling Edge of $\overline{RAS}$				RAM Modes	SAM Modes	
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WE}$	$\overline{SOE}$		SI/O Direction	Notes
H	H	H	X	Read/Write	S_{in}/S_{out}	1, 2, 3
H	H	L	X	Temporary Write Mask Data Program	S_{in}/S_{out}	1, 2, 3
H	L	H	X	Read Transfer	S_{out}	2
H	L	L	L	Write Transfer	S_{in}	
H	L	L	H	Pseudo Transfer	S_{in}	
L	X	X	X	CBR Refresh	S_{in}/S_{out}	1, 2

H: High L: Low X: Don't Care

Notes: 1. Transfer cycle executed previously defines SI/O direction.
2. SI/O is in high impedance state with $\overline{SOE}$ high, even if the direction is S_{out}.
3. The HM53461 starts write operation if WE is low at the falling edge of $\overline{CAS}$ or become low between the falling edge of $\overline{CAS}$ and the rising edge of $\overline{RAS}$.

Read/Write Operation: Read/write is performed on the random port in the same sequence as for a dynamic RAM (Figure 1-3). The HM53461 starts the read operation with $\overline{WE}$ high and the write operation at the falling edge of $\overline{WE}$.

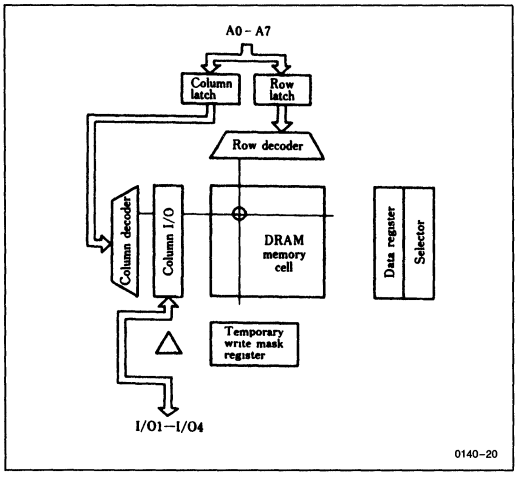


Figure 1-3. Read/Write Operation

Temporary Write Mask Set and Temporary Masked Write Operation: The HM53461 provides temporary masked write operation which inhibits to write data bit-by-bit (write mask) during one $\overline{RAS}$ cycle. Temporary write mask set function defines the bits to be inhibited (Figure 1-4). This operation puts the data on $I/O_1-I/O_4$ into the internal temporary write mask register. When 0 is programmed to the register, writing to the corresponding bit is inhibited.

The temporary write mask register is reset at the rising edge of $\overline{RAS}$.

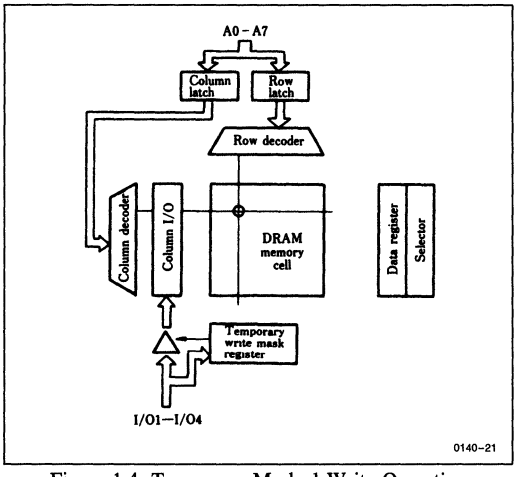


Figure 1-4. Temporary Masked Write Operation

Read Transfer Operation: In this cycle, the HM53461 transfers the data of one row in RAM (1024 bits), which address is specified at the falling edge of $\overline{RAS}$, to SAM (Figure 1-5). The start address in SAM can be programmed at the falling edge of $\overline{CAS}$ in this cycle. After data transfer, the serial port turns to serial read mode at the rising edge of $\overline{DT}/\overline{OE}$.

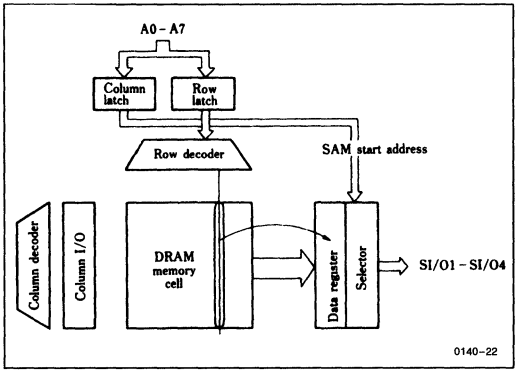


Figure 1-5. Read Transfer Operation

Write Transfer Operation: In this cycle, the HM53461 transfers the data in the SAM data register (1024-bits) to one row in RAM, which address is specified at the falling edge of $\overline{RAS}$ (Figure 1-6). The start address in SAM can be programmed in this cycle. After data transfer, serial port turns to serial write mode.

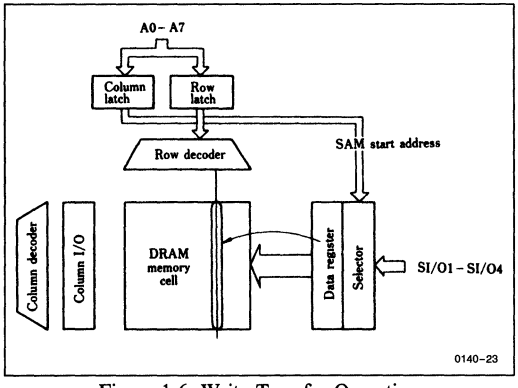


Figure 1-6. Write Transfer Operation

Pseudo Transfer Operation: This operation switches the serial port to serial write mode (Figure 1-7). It does not perform data transfer between RAM and SAM. Sam start address can be programmed in this cycle.

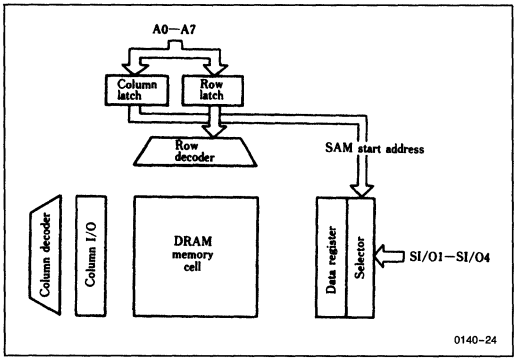


Figure 1-7. Pseudo Transfer Operation

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Operation: The HM53461 performs refresh by using the internal address counter in this operation (Figure 1-8).

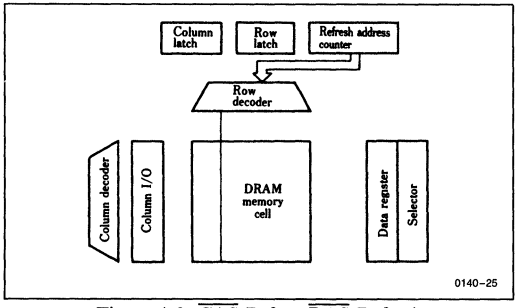


Figure 1-8. $\overline{CAS}$ Before $\overline{RAS}$ Refresh

Serial Read/Write Operation: The HM53461 reads/writes the contents of the SAM data register in serial at the rising edge of SC (serial clock input) (Figure 1-9). The address for serial access is generated by the internal address pointer, independently of random port operation. It should be considered that serial access is restricted in transfer cycles. The SAM, employing static-type data registers, requires no refresh.

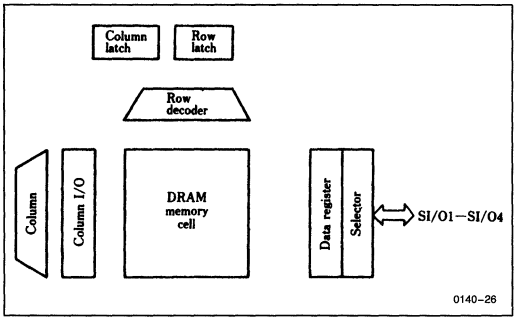


Figure 1-9. Serial Read/Write Operation

The HM53462 is a multiport video RAM, adding logic operation capability to the advantages of HM53461.

Figure 1-10 shows the block diagram. Table 1-2 describes the operation modes.

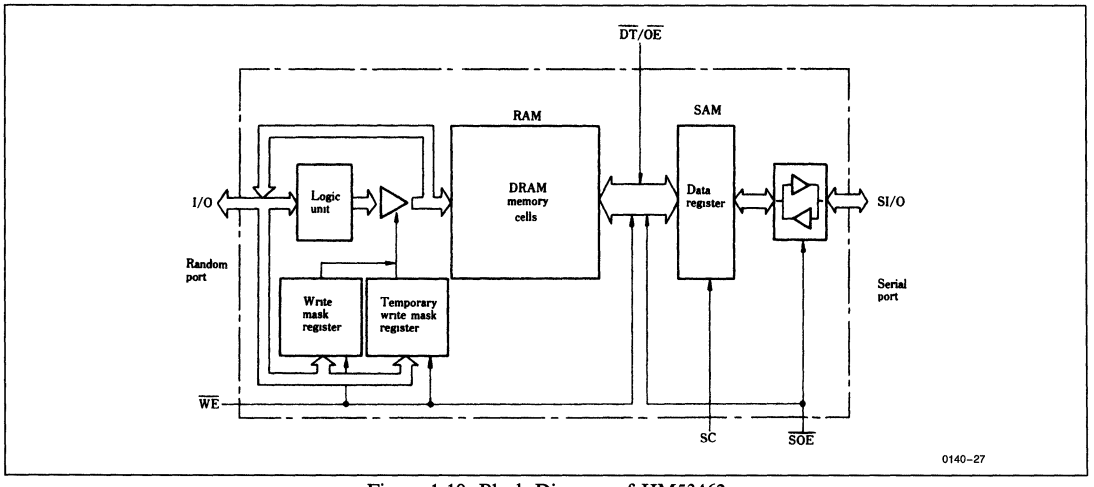


Figure 1-10. Block Diagram of HM53462

• Table 1-2. Operation Modes of HM53462

At the Falling Edge of $\overline{RAS}$				RAM Modes	SAM Modes	
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SOE}$		SI/O Direction	Notes
H	H	H	X	Read/Write	S_{in}/S_{out}	1, 2, 3
H	H	L	X	Temporary Masked Write	S_{in}/S_{out}	1, 2, 3
H	L	H	X	Read Transfer	S_{out}	2
H	L	L	L	Write Transfer	S_{in}	
H	L	L	H	Pseudo Transfer	S_{in}	
L	X	X	X	$\overline{CAS}$ Before $\overline{RAS}$ Refresh	S_{in}/S_{out}	1, 2
L	X	L	X	Logic Operation Program (CBR Refresh)	S_{in}/S_{out}	1, 2

H: High L: Low X: Don't Care

Notes: 1. Transfer cycle previously executed defines SI/O direction.
2. SI/O is in high impedance with $\overline{SOE}$ high, even if SI/O direction is S_{out}.
3. HM53462 writes if $\overline{WE}$ is low at the falling edge of $\overline{CAS}$ or becomes low between the falling edge of $\overline{CAS}$ and the rising edge of RAS.

Logic Operation Programming: This function programs a logic operation (Figure 1-11). The logic operation is available uintil re-programmed or reset. In logic operation mode, HM53462 performs read-modify-write internally when data is written into random port. The result of the logic operation between memory data and written data is put into the address from which the memory data is transferred.

In the logic operation programming cycle, the mask register, which differs from the temporary mask register, is also programmed. It is available until reprogrammed.

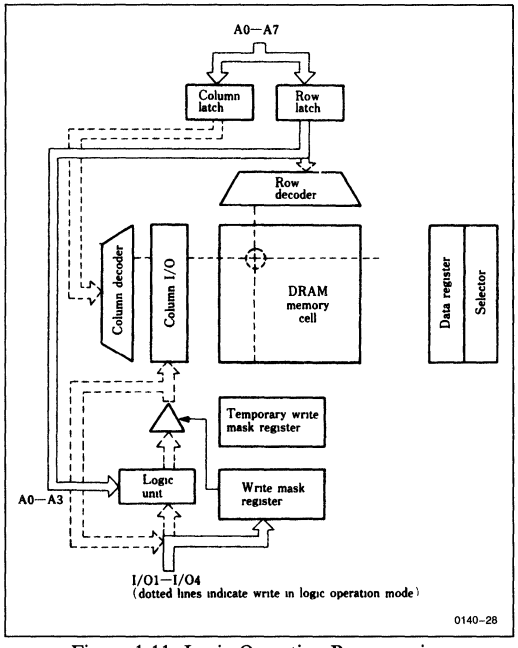


Figure 1-11. Logic Operation Programming

Notes: Notes on using HM53461/HM53462 are as follows:

- Dummy $\overline{RAS}$ Cycle. Devices should be initialized by 8 dummy $\overline{RAS}$ cycles (minimum) before access to random port. Refresh cycle can be inserted for initialization. It is recommended that the system be initialized by dummy $\overline{RAS}$ cycle in the automatic reset time of the processor.
- Bypass Capacitor. One bypass capacitor should be inserted between V_{CC} and V_{SS} to each device. The V_{CC} pin should be connected to the capacitor by the shortest path. A capacitor of several μF is suitable.
- Negative Voltage Input. Negative polarity input level to input pin or I/O pin should be under -1V. In this range, it has no effect on device characteristics or RAM/SAM data retention.
- Initialization of logic operation mode (HM53462). The logic operation programming cycle should be executed before access to the random port to initialize logic operation mode after power on. At this point, the operation codes (0101) and all 1 write mask data are recommended.

1.2 Line Memory

Hitachi has produced a line memory for line buffers with simple circuits, providing specific functions as described below.

The line buffer can improve picture quality by storing 1 horizontal line data. It has following features.

- Capacity to store 1 horizontal line data
- High-speed operation matching the sampling speed of PAL TV signal (4 fsc/8 fsc) or NTSC TV signal (4 fsc/8 fsc).
- Separate data inputs/outputs and capability of serial data inputs and outputs.

The conventional line buffer composed of high speed static RAMs requires separate input/output for double buffer organization. It also requires interleaving for high speed operation, matching 4 fsc/8 fsc, where fsc is the subcarrier frequency. In addition, external circuits are needed for serial address scan.

The line memory provides all of these functions. Figure 1-12 shows the standard ogranization of a conventional memory buffer and Figure 1-13 shows the block diagram of line memory.

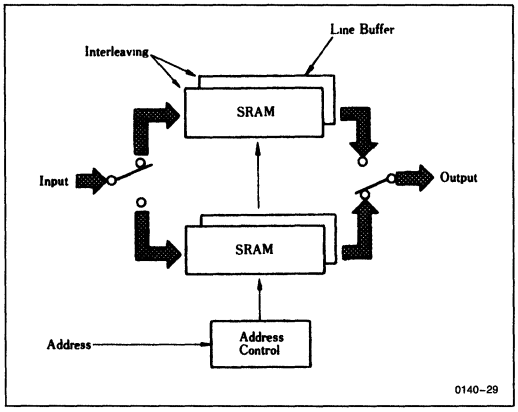
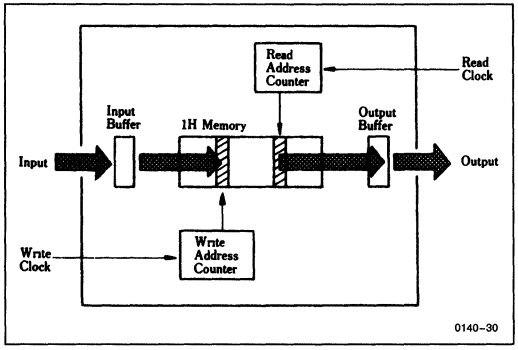


Figure 1-12. Standard Organization of Conventional Line Buffer



Figurer 1-13. Block Diagram of Line Memory

The Hitachi HM63021 is a 2048-word x 8-bit line memory storing 2 horizontal lines of data.

It has five different modes for various video graphic system applications. It realizes high speed operations for PAL and NTSC TV signals, and dissipates little power employing 1.3 μm CMOS technology and static-type memory cells.

The features of the HM63021 are described as follows:

- Five modes for various video graphic system applications
  - —Delay line mode
  - —Alternate 1H/2H delay mode
  - —TBC (Time-Base Corrector) mode
  - —Double speed conversion mode
  - —Time-base compression/expansion mode
- High speed cycle time
  - —HM63021-34: 34 ns min (corresponds to 8 fsc of NTSC TV signal)
  - —HM63021-28: 28 ns min (corresponds to 8 fsc of PAL TV signal).

Line memory in the system using digital signal processing technologies offers following applications:

1. comb filter
2. double-speed conversion (non-interface)
3. compression/expansion of graphics (picture-in-picture)
4. dropout canceller
5. time-base corrector
6. noise reducer

2. DYNAMIC RAM

2.1 Dynamic RAM Memory Call

The dynamic RAM memory cell consists of 1 MOS transistor and 1 capacitor, as shown in Figure 2-1. It detects the data in the cell (1 or 0) by the charge stored in capacitor. Dynamic RAM offers higher density than that of static RAM because of fewer components per chip.

However, Dynamic RAM must rewrite data, called refresh, in a defined cycle because the charge stored in the capacitor leaks.

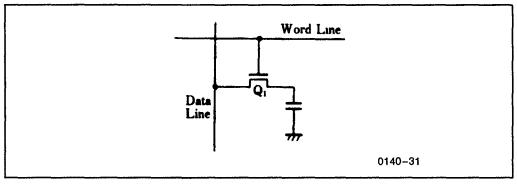


Figure 2-1. Memory Cell of Dynamic RAM

2.2 Power On Procedure

After turning on power, to set the internal memory circuitry, hold for more than 100 μs, then apply eight or more dummy cycles before operation. The dummy cycle may be either a normal read/write cycle or a refresh cycle. When using an internal refresh counter, eight or more $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required as dummy cycles.

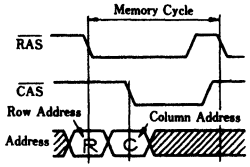
2.3 Address Multiplexing

Dynamic RAMs are used to increase capacity because of their smaller cell area. In using dynamic RAMs in systems, however, it is desirable to increase the memory density by using smaller packages. To reduce the number of pins and the package size, address multiplexing is used.

Using a 1-Mbit dynamic RAM, 20-address signals are necessary to select one of 1,048,576 memory cells. Address multiplexing allows address signals to be applied to each address pin. Thus only 10-address input pins are required to select one of 1,048,576 addresses. Multiplexed address inputs are latched as follows: $\overline{RAS}$ (Row Address Strobe) selects one of word lines according to the row address signal, and one of column decoders is selected by $\overline{CAS}$ (column address strobe) following column address signal. Although two extra signals, $\overline{RAS}$ and $\overline{CAS}$, are required, the number of address pins is reduced to half. Figure 2-2 shows the pin arrangement, address latch waveform, and the block diagram of address-multiplexed 1-Mbit dynamic RAM. Systems need an address multiplexer in order to latch the multiplexed address signals into the device.

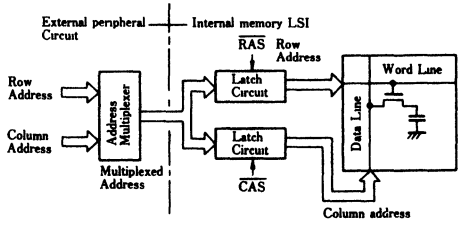
A_0–A_9	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{in}	Data In
D_{out}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+ 5V)
V_{SS}	Ground
A_0–A_8	Refresh Address Inputs

(a) Pin Arrangement



(b) Address Latch

0140-32

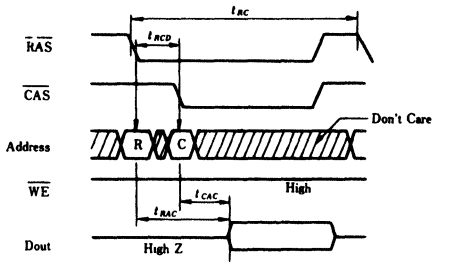


(c) Block diagram of Address Multiplexing

0140-33

Figure 2-2. Address Multiplexing of Dynamic RAMs

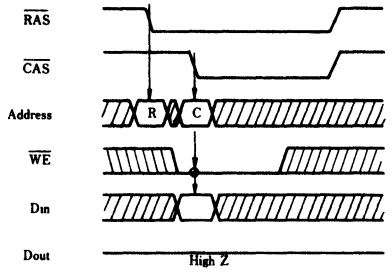
2.4 Dynamic RAM Function



(a) Read Cycle

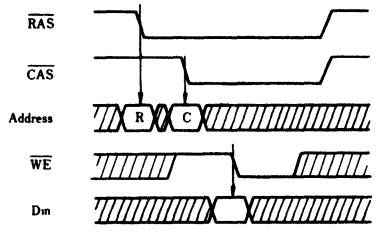
0140-34

t_{RC}: Random Read or Write Cycle Time
t_{RCD}: RAS to CAS Delay Time
t_{RAC}: Access Time from RAS
t_{CAC}: Access Time from CAS
R: Row Address
C: Column Address



(Early Write)

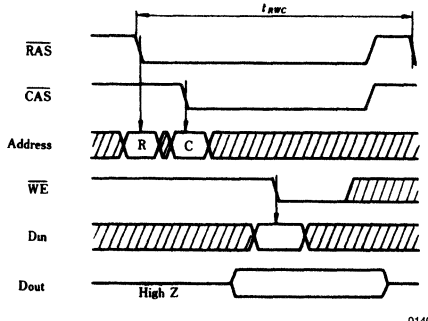
0140-35



(Delayed Write)

0140-37

(b) Write Cycle



(c) Read-Modify-Write Cycle

0140-36

t_{RWC}: Read-Write Cycle Time

Figure 2-3. Normal Function of Dynamic RAM

Read Cycle: In the read cycle, a row address is latched at the falling edge of $\overline{RAS}$, and a column address is latched at the falling edge of $\overline{CAS}$ after the $\overline{RAS}$ falling edge. If $\overline{WE}$ is high, the data is read out from D_{out} with the access time of t_{CAC} (Access time from $\overline{CAS}$) or t_{RAC} (Access time from $\overline{RAS}$).

The t_{RCD} maximum ($\overline{RAS}$ to $\overline{CAS}$ delay time) is specified only to guarantee the specified minimum values of other timings such as the cycle time, $\overline{RAS}/\overline{CAS}$ pulse width. Therefore, when using these timings with more than the specified minimum value, there is no need to limit the t_{RCD} to the specified maximum value.

Write Cycle: Dynamic RAM provides two write cycle modes: early write cycle and delayed write cycle. In the early write cycle, when $\overline{WE}$ is low, data is written into D_{in} at the falling edge of $\overline{CAS}$. In delayed write cycle, when $\overline{WE}$ is high, data is written into D_{in} at the falling edge of $\overline{WE}$ after $\overline{CAS}$ falling.

Read-Modify-Write Cycle: The read-modify-write cycle is initiated by taking $\overline{WE}$ high. Data is read out from D_{out} at the falling edge of $\overline{CAS}$ with $\overline{WE}$ high. Then, when $\overline{WE}$ goes low, data is written into the same address from D_{in} in the same cycle.

The cycle time in the read-modify-write mode (t_{RWC}) is longer than the cycle time in read/write mode (t_{RC}).

2.5 High Speed Access Mode

Dynamic RAM access time is typically longer than that of static RAMs. To realize higher speed operation, they have high speed access modes.

The read operation in dynamic RAM is performed as follows:

When a word line is selected by row address, all data in the memory cells connected to the selected word line is transferred to sense amplifiers. One of these sense amplifiers is selected by the column address, and its contents are output.

The output of data from other sense amplifiers is controlled only by the column address.

Access controlled only by column address with the row address fixed is called high speed access mode. Table 2-1 compares each mode.

Page Mode: This is the most typical access mode in dynamic RAM. The column address is switched synchronized with $\overline{CAS}$ falling.

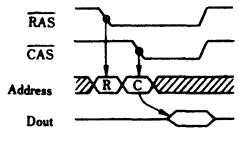
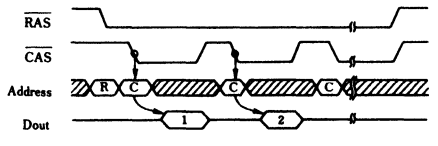
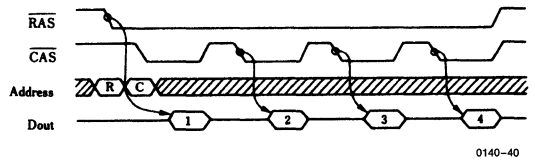
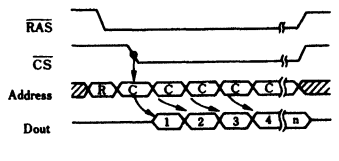
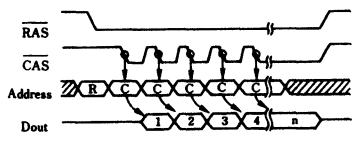
Nibble Mode: In a nibble mode dynamic RAM, data from 4 sequential addresses is stored in the 4-bit output latch circuits. Output is provided by the $\overline{CAS}$ signal, which controls the latch circuits.

When 4 addresses are accessed sequentially, the row addresses on and after second bit need not be selected. Therefore, it facilitates the timing design. In nibble mode, the operation is limited to 4 addresses, however, it enables faster access (t_{NAC}) than that in page mode.

Static Column Mode: In static column mode, the column address is switched without the synchronized signal by high-speed static RAM technology in the peripheral circuits.

High Speed Page Mode: This mode is the advanced mode of static column mode, with $\overline{CAS}$ providing the address latch function.

• Table 2-1. Comparison of Dynamic RAM High Speed Access Modes

Normal Mode	 R: Row Address C: Column Address
Page Mode	
Nibble Mode	
Static Column Mode	
High-Speed Page Mode	

2.6 Refresh

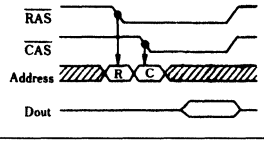
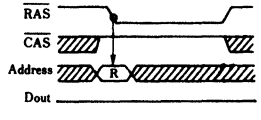
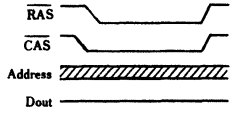
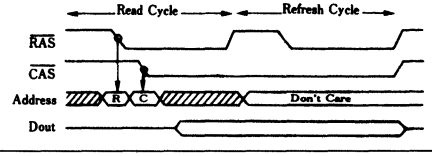
Refresh operation is performed by accessing every word line within the specified time (refresh cycle). Table 2-2 compares the following refresh modes in dynamic RAM.

$\overline{\text{RAS}}$ Only Refresh: In $\overline{\text{RAS}}$ only refresh mode, refresh can be completed by selecting only row addresses synchronized with $\overline{\text{RAS}}$.

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh: This mode refreshes by the $\overline{\text{CAS}}$ falling edge before $\overline{\text{RAS}}$ in the period defined by the internal refresh address generator. This mode simplifies the external address multiplexer.

Hidden Refresh: In hidden refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is performed while output data is valid.

• Table 2-2. Comparison of Dynamic RAM Refresh Modes

Read	 0140-43
$\overline{\text{RAS}}$ Only Refresh	 0140-44
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh	 0140-45
Hidden Refresh	 0140-46

 : Don't care
0140-47

3. INSTRUCTIONS FOR USING MEMORY DEVICES

3.1 Prevention of Electrostatic Discharge

As semiconductor memory designs are based on a very fine pattern, they can be subject to malfunction or defects caused by static electricity. Though the built-in protection circuits assure unaffected reliability in normal use, devices should be handled according to the following instructions.

1. In transporting and storing memory devices, put them in conductive magazine or put all pins of each device into a conductive mat so that they are kept at the same potential. Manufacturers should give enough consideration to packing when shipping their products.
2. When devices touch a human body in mounting or inspection, the handler must be grounded. Do not forget to insert a resistor (1 MΩ approx. is desirable) in series to protect the handles from electrical shock.
3. Keep the relative ambient humidity at about 50% in process.
4. For working clothes, cotton is preferrable to synthetic fabrics.
5. Use a soldering iron operating at low voltage (12V or 24V, if possible) with its tip grounded.
6. In transporting the board with memory devices mounted on it, cover it with conductive sheets.
7. Use conductive sheets of high resistance to protect devices from electrostatic discharge. For, if dropped onto conductive materials like a metal sheet, devices may deteriorate or even breakdown owing to sudden discharge of the charge stored on the surface.
8. Never set the system to which memory devices are applied near anything that generates high voltage (e.g., CRT Anode electrode, etc.).

3.2 Using CMOS Memories

As shown in Figure 3-1, the input of a CMOS memory is connected to the gate of an inverter consisting of PMOS and NMOS transistors. Figure 3-2 shows the relationship between the input voltage and current in this inverter. The top and bottom transistors turn ON and make current flown when the input voltage becomes intermediate level. Therefore, it is necessary to keep the input voltage below 0.2V or above V_{CC} − 0.2V in order to minimize power consumption. The data sheet specifies the stand-by current for both the cases of input level with minimum V_{IH} and maximum V_{IL}, and that with 0.2V or V_{CC} − 0.2V, and the difference in value is remarkably great. Some memory devices are designed to cut off such current flow in standby mode by the control of input signals, but it depends on device type. This should be confirmed in data sheets for each device type.

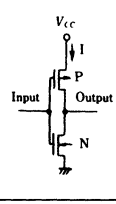


Figure 3-1. CMOS Inverter

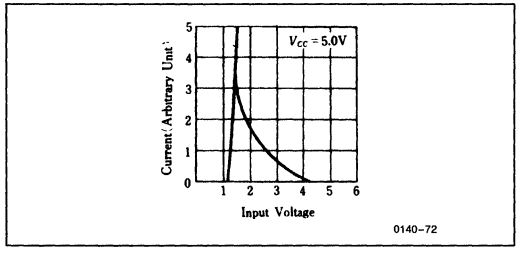


Figure 3-2. Relationship between Input Voltage and Current in CMOS Inverter

Another problem particular to CMOS devices is latch-up. Figure 3-3 shows the cross section of a CMOS inverter and the structure of a parasitic bipolar transistor. The equivalent circuit of the parasitic thyristor is shown in Figure 3-4. When positive DC current or pulse noise is applied (Figure 3-4 (a)), TR3 is turned on owing to the bias voltage generated between base and emitter. And trigger current flows into GND through R_P, the base resistance of TR2. As a result, TR2 becomes conductive and current flows from power supply (V_{CC}) through the base resistance of TR1 (R_N), which puts TR1 into conduction, too. Then, as the base of TR2 is rebiased by collector current from TR1, the closed loop consisting of TR1 and TR2 reacts. Thus current flows constantly between power supply (V_{CC}) and GND even without trigger current caused by outside noise.

Latch-up can be caused by a negative pulse, too (Figure 3-4 (bb)). Most of semiconductor memory manufacturers are trying to improve latch-up immunity of their products. Hitachi provides enough guard band by applying diffusion layer around inputs and outputs, taking care not to connect input to p^+ diffusion layer. Input voltage for 64K-bit static RAM HM6264A, for example, is specified as follows:

V_{IH} max 6.0V (not depending on V_{CC})
V_{IL} min 3.0V (pulse width = 50 ns)
−0.3V (DC level)

Thus almost no consideration for latch-up is required in system design.

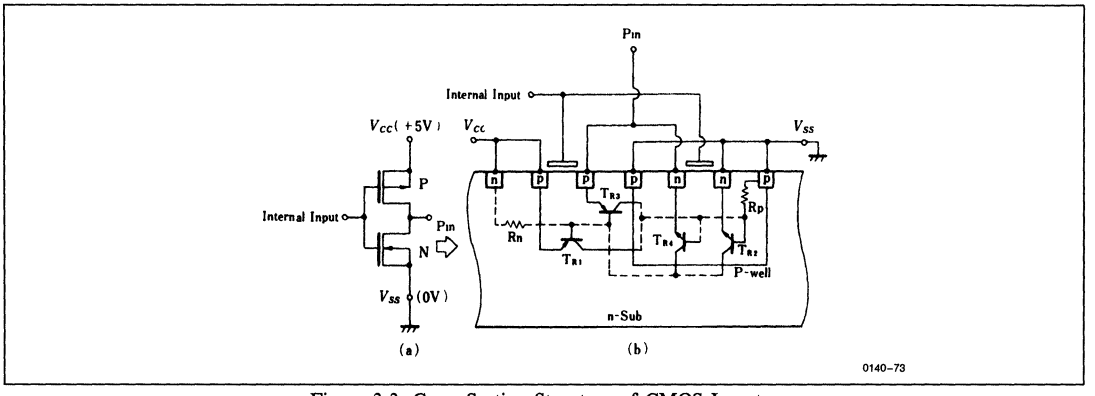


Figure 3-3. Cross Section Structure of CMOS Inverter

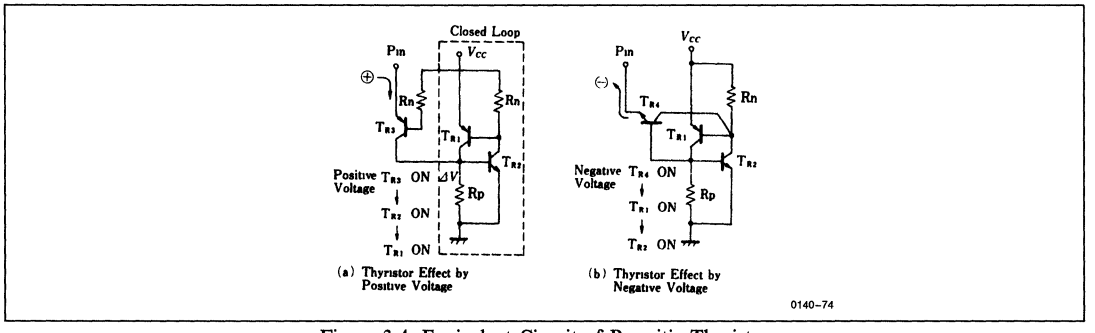


Figure 3-4. Equivalent Circuit of Parasitic Thyristor

3.3 Noise Prevention

Noise in semiconductor memories is roughly classified into input signal noise and power supply noise.

3.3.1 Input Signal Noise

Input signal noise is caused by overshoot and undershoot. If either of them is out of recommended DC operating conditions, normal operation is hindered, and voltage over absolute maximum rating will break the device. In operating high speed systems, special care is required to prevent input signal noise.

The noise can be prevented by inserting a serial resistance of less than 50Ω into each input or a terminating resistance into the input line. Actually, however, input signal noise can be simply reduced by a stable power supply line, because it is often caused by unstable reference voltage (GND level).

3.3.2 Power Supply Noise

The power source noise can be classed as low-frequency noise and high-frequency noise as shown in Figure 3-5. To assure stable memory operation, the peak-to-peak power supply voltage in the presence of low-or high-frequency noise should be held below 10 percent of its standard level.

Devices like dynamic RAMs, which operate from clock signals, or high speed CMOS static RAMs, through which current flows during transition of signals, consume high peak

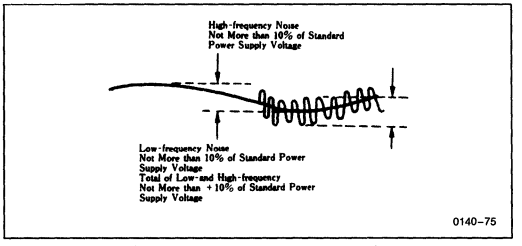


Figure 3-5. Power Source Noise

current. When a power supply does not have enough capacity for the peak current, voltage drops. And if the recovery rate of the power supply synchronizes with its time constant, it may start oscillating. To reduce the influence of the peak current, a bypass capacitor of 0.1 – 0.01 μF should be inserted near the device. The following points must be considered in designing pattern of the board:

- For bypass capacitors, use titanium, ceramic, or tantalum capacitors which have better high-frequency characteristics.
- Bypass capacitors must be applied as near to the power supply pin of memory devices as possible, and inductance in the path from V_{CC} pin to V_{SS} pin through the bypass capacitor must be as little as possible.

- The line connected to the power supply on the board should be as wide as possible.
- It is preferable for the power supply line to be at right angles to devices selected at the same time, lest too much peak current should flow through one power supply line at a time.

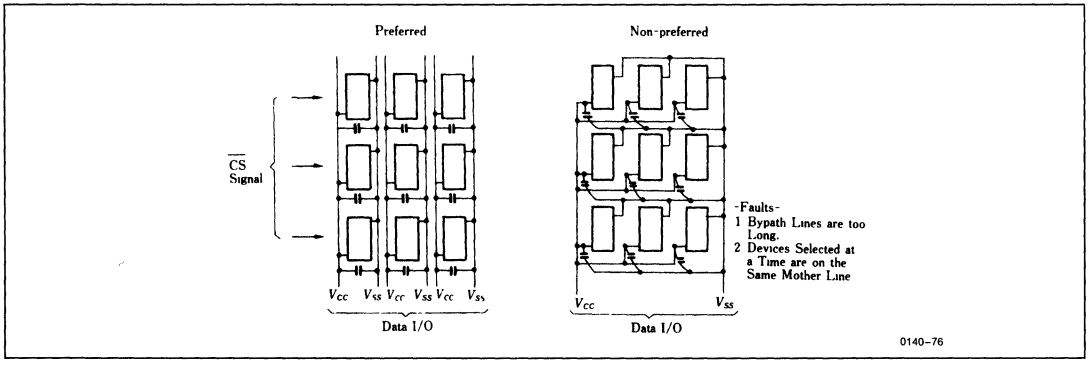


Figure 3-6. Examples of Power Supply Board Pattern

3.4 Address Input Waveform of Hi-BiCMOS Memory

Data stored in memory might be destructed in case that Address Input of the HM6716, HM6719, HM6787, HM6788 and HM6789 series becomes floating and sticks at and around threshold voltage. (e.g., CPU does Address Bus to off state in Figure 1.) Consequently, the following three methods are recommended so as to preserve malfunction of memory device.

A: Insert latch as shown in Figure 3-7 lest Address Input should become floating.

B: Put $\overline{CS}$ into High while Address Input becomes floating. (Dotted line in Figure 3-8)

C: Insert Pull-up Resistor (R) to hold time constant of Rising Edge waveform of Address Input pin (t_r = R x C) below 150 ns.

Stable operation can be assured if you have already adopted the above three methods (A, B, C), while if you have any problem, please contact our sales offices.

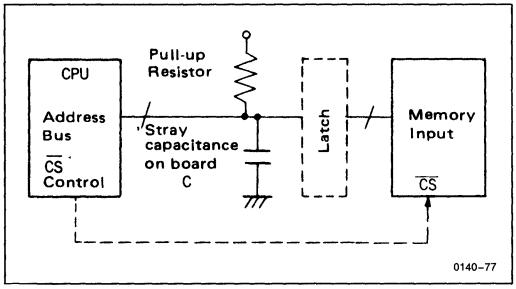


Figure 3-7

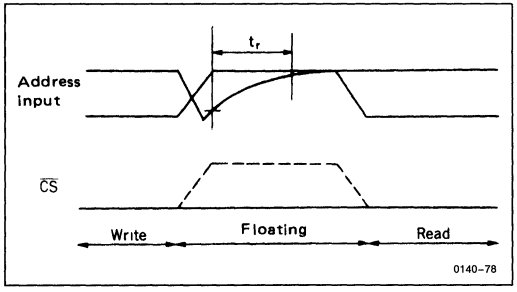


Figure 3-8

2

Section 2
MOS Dynamic RAM

HITACHI®

HM514256A/AL Series

262,144-Word x 4-Bit CMOS Dynamic RAM

■ DESCRIPTION

The Hitachi HM514256A/AL is a CMOS dynamic RAM organized 262,144-word x 4-bit. HM514256A/AL has realized higher density, higher performance and various functions by employing 1.3 μm CMOS technology and some new CMOS circuit design technologies. The HM514256A/AL offers Fast Page Mode as a high speed access mode.

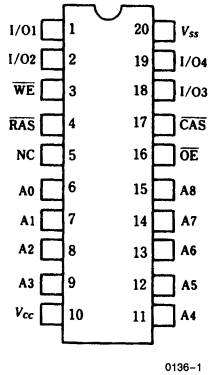
Multiplexed address input permits the HM514256A/AL to be packaged in standard 20-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low Power
  - Standby .....11 mW (max), 1.7 mW (max) (L Version)
  - Active.....495 mW/440 mW/363 mW/302.5 mW/258.5 mW (max)
- Fast Page Mode Capability
- 512 Refresh Cycles .....(8 ms), (64 ms) (L Version)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh

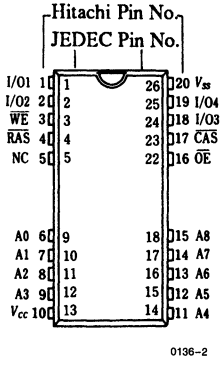
■ PIN OUT

HM514256A/ALP Series



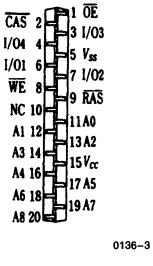
(Top View)

HM514256A/ALJP Series



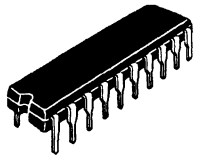
(Top View)

HM514256A/ALZP Series



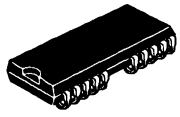
(Top View)

HM514256A/ALP Series



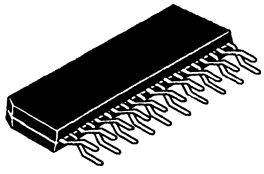
(DP-20NA)

HM514256A/ALJP Series



(CP-20D)

HM514256A/ALZP Series



(ZP-20)

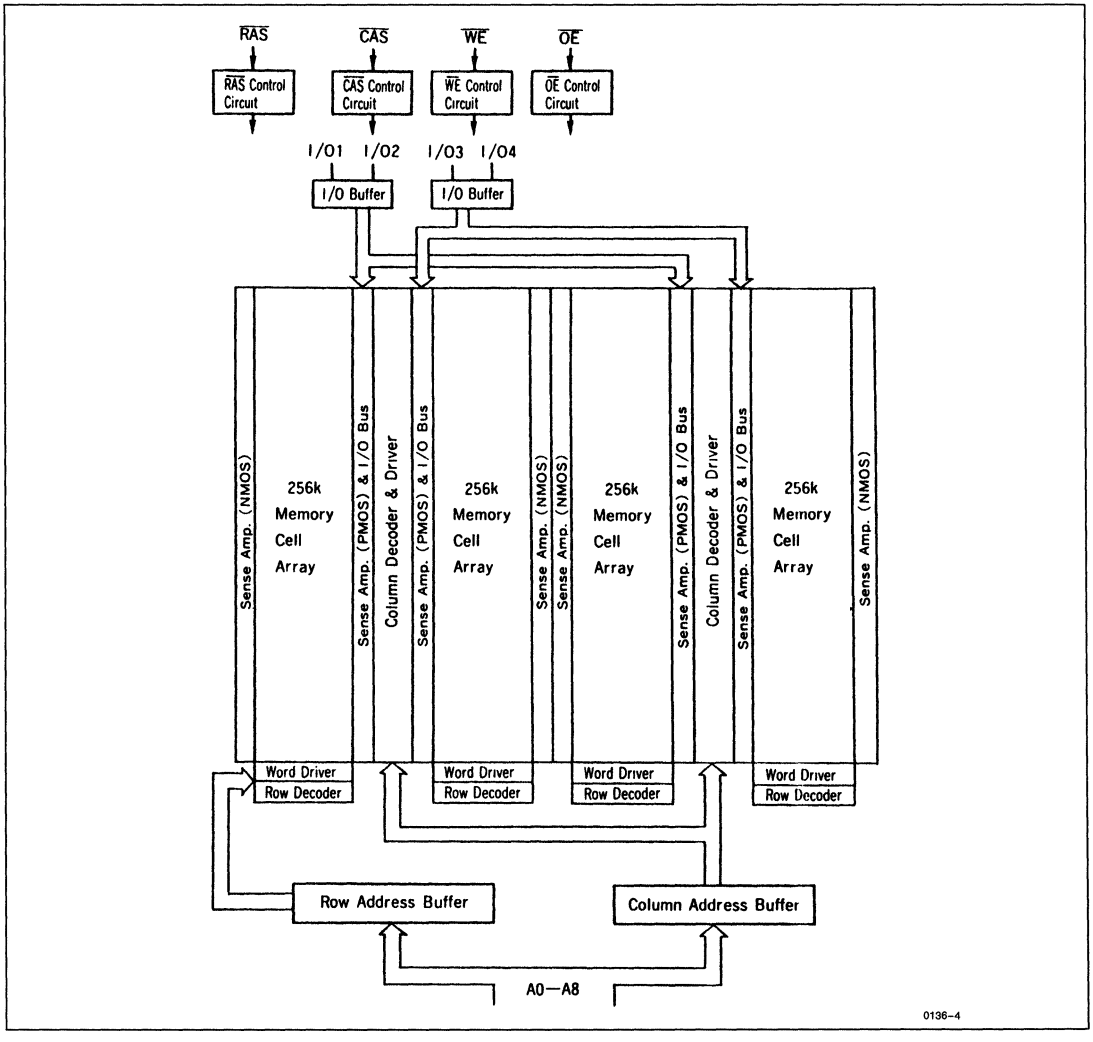
■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Input
A_0–A_8	Refresh Address Input
I/O_1–I/O_4	Data Input/Data Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground

■ ORDERING INFORMATION

Part No.	Access Time	Package	Part No.	Access Time	Package
HM514256AP-6	60 ns		HM514256ALP-6	60 ns	
HM514256AP-7	70 ns	300-mil 20-pin	HM514256ALP-7	70 ns	300-mil 20-pin
HM514256AP-8	80 ns	Plastic DIP	HM514256ALP-8	80 ns	Plastic DIP
HM514256AP-10	100 ns	(DP-20NA)	HM514256ALP-10	100 ns	(DP-20NA)
HM514256AP-12	120 ns		HM514256ALP-12	120 ns	
HM514256AJP-6	60 ns		HM514256ALJP-6	60 ns	
HM514256AJP-7	70 ns	300-mil 20-pin	HM514256ALJP-7	70 ns	300-mil 20-pin
HM514256AJP-8	80 ns	Plastic SOJ	HM514256ALJP-8	80 ns	Plastic SOJ
HM514256AJP-10	100 ns	(CP-20D)	HM514256ALJP-10	100 ns	(CP-20D)
HM514256AJP-12	120 ns		HM514256ALJP-12	120 ns	
HM514256AZP-6	60 ns		HM514256ALZP-6	60 ns	
HM514256AZP-7	70 ns	400-mil 20-pin	HM514256ALZP-7	70 ns	400-mil 20-pin
HM514256AZP-8	80 ns	Plastic ZIP	HM514256ALZP-8	80 ns	Plastic ZIP
HM514256AZP-10	100 ns	(ZP-20)	HM514256ALZP-10	100 ns	(ZP-20)
HM514256AZP-12	120 ns		HM514256ALZP-12	120 ns	

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temerature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55° to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Item		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	I/O Pin	V_{IL}	− 1.0	—	0.8	V	1
	Others	V_{IL}	− 2.0	—	0.8	V	1

Note: 1. All voltage reference to V_{SS}.

• DC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Item	Symbol	HM514256 A/AL-6 Min	A/AL-6 Max	A/AL-7 Min	A/AL-7 Max	A/AL-8 Min	A/AL-8 Max	A/AL-10 Min	A/AL-10 Max	A/AL-12 Min	A/AL-12 Max	Unit	Test Conditions	Note
Operating Current	I_{CC1}	—	90	—	80	—	66	—	55	—	47	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	—	2	—	2	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z TTL Interface	
		—	1	—	1	—	1	—	1	—	1		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V CMOS Interface	
		—	300	—	300	—	300	—	300	—	300	μA	D_{out} = High-Z CMOS Interface L-Version	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	90	—	80	—	66	—	55	—	47	mA	t_{RC} = Min	2
Battery Backup Current (Only for L-Version)	I_{CC4}	—	300	—	300	—	300	—	300	—	300	μA	t_{RC} = 125 μs $\overline{CAS}$ Before $\overline{RAS}$ Cycling	4
Standby Current	I_{CC5}	—	5	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	80	—	70	—	66	—	55	—	47	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	80	—	70	—	55	—	55	—	47	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	

• **DC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V) (continued)

Item	Symbol	HM514256										Unit	Test Conditions	Note
		A/AL-6		A/AL-7		A/AL-8		A/AL-10		A/AL-12				
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. t_{RAS} = t_{RAS} (min) to 1 μs.
Input Voltage: I/O Pins: $V_{IH} \geq V_{CC} - 0.2V$, $V_{IL} \leq 0.2V$ or High-Z
The Other Pins: $V_{IH} \geq V_{CC} - 0.2V$, or $V_{IL} \leq 0.2V$

• **Capacitance** (T_A = 25°C, V_{CC} ±10%)

Item		Symbol	Typ	Max	Unit	Note
Input Capacitance	Address	C_{I1}	—	5	pF	1
	Clock	C_{I2}	—	7	pF	1
Input/Output Capacitance	Data Input/Data Output	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[14]

Test Conditions

Input Rise and Fall Times	5 ns
Input Timing Reference Levels	0.8V, 2.4V
Output Load	2 TTL Gate + C_L (100 pF) (Including Scope and Jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Item	Symbol	HM514256										Unit	Note
		A/AL-6		A/AL-7		A/AL-8		A/AL-10		A/AL-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	120	—	130	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	50	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Delay Time	t_{RAD}	15	30	15	35	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	ns	

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters) (continued)

Item	Symbol	HM514256										Unit	Note
		A/AL-6		A/AL-7		A/AL-8		A/AL-10		A/AL-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	20	—	20	—	20	—	25	—	30	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	0	—	0	—	ns	
$\overline{CAS}$ Delay Time from D_{in}	t_{DZC}	0	—	0	—	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	1, 7
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ms	
Refresh Period (Only for L-Version)	t_{REF}	—	64	—	64	—	64	—	64	—	64	ms	

Read Cycle

Item	Symbol	HM514256										Unit	Note
		A/AL-6		A/AL-7		A/AL-8		A/AL-10		A/AL-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	55	ns	3, 5
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	—	25	—	30	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	—	20	—	20	—	20	—	25	—	30	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	—	20	—	20	—	20	—	25	—	30	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	20	—	20	—	20	—	25	—	30	—	ns	

Write Cycle

Item	Symbol	HM514256										Unit	Note
		A/AL-6		A/AL-7		A/AL-8		A/AL-10		A/AL-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	25	—	30	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in Hold time	t_{DH}	15	—	15	—	15	—	20	—	25	—	ns	11

Read-Modify-Write Cycle

Item	Symbol	HM514256										Unit	Note
		A/AL-6		A/AL-7		A/AL-8		A/AL-10		A/AL-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read-Write Cycle Time	t_{RWC}	170	—	180	—	220	—	255	—	295	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	85	—	95	—	110	—	135	—	160	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	45	—	45	—	55	—	60	—	70	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	55	—	60	—	70	—	80	—	95	—	ns	10
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	20	—	20	—	25	—	25	—	30	—	ns	

Refresh Cycle

Item	Symbol	HM514256										Unit	Note
		A/AL-6		A/AL-7		A/AL-8		A/AL-10		A/AL-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

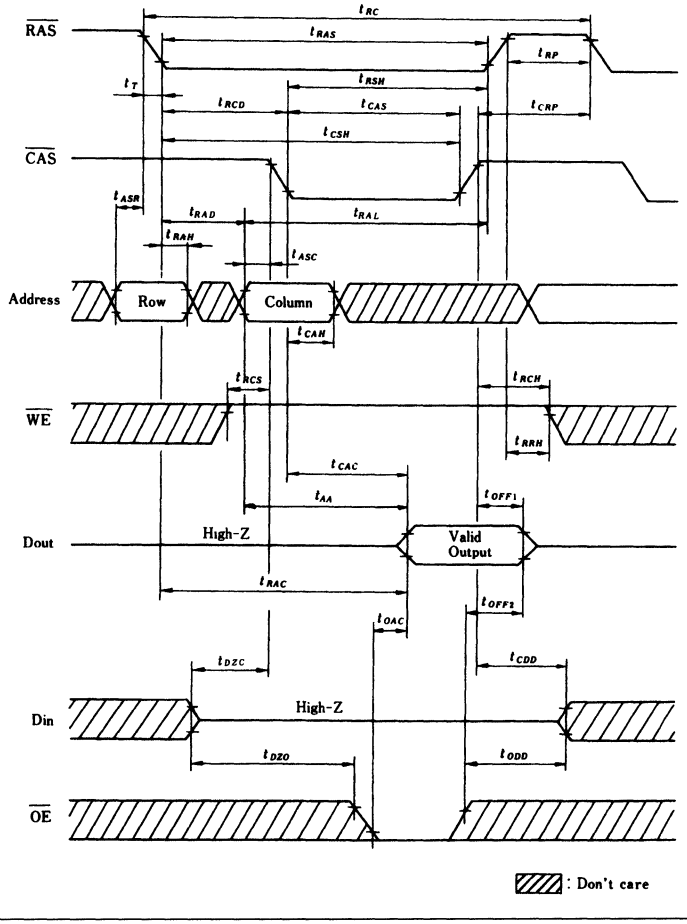
Item	Symbol	HM514256										Unit	Note
		A/AL-6		A/AL-7		A/AL-8		A/AL-10		A/AL-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	1000000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	—	50	—	60	ns	13
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	50	—	60	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{PCM}	95	—	100	—	110	—	115	—	135	—	ns	

Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

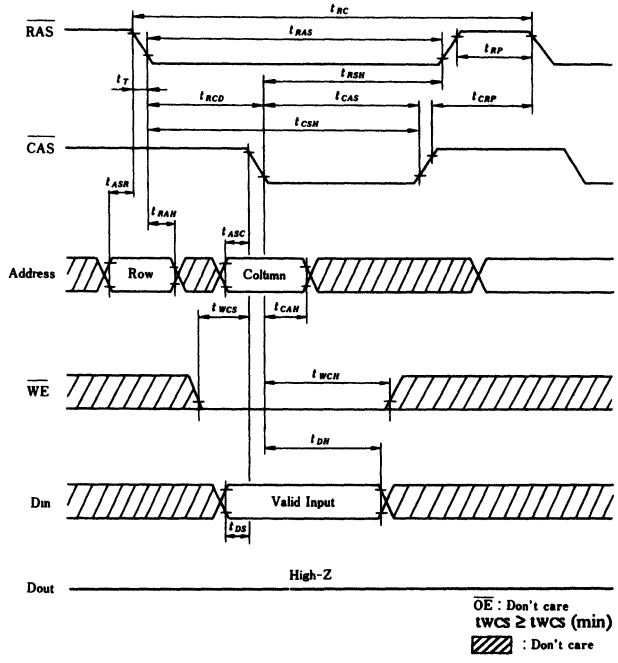
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power-up followed by eight or more initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If the internal refresh counter is used, eight or more $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.

■ TIMING WAVEFORMS

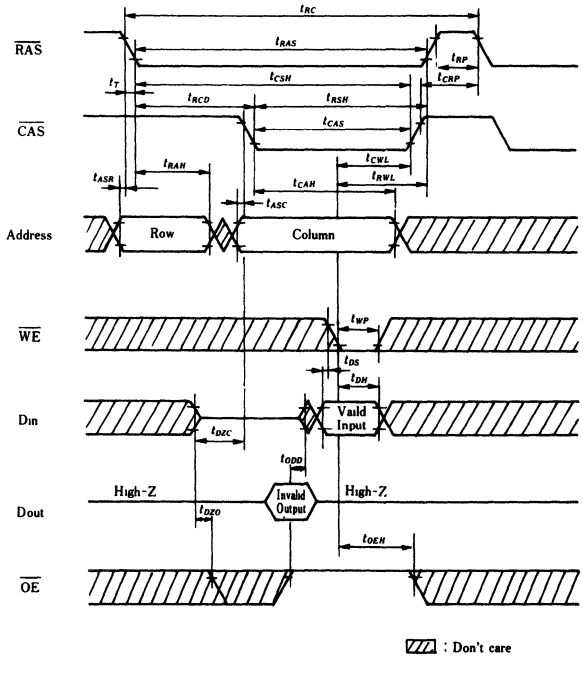
• Read Cycle



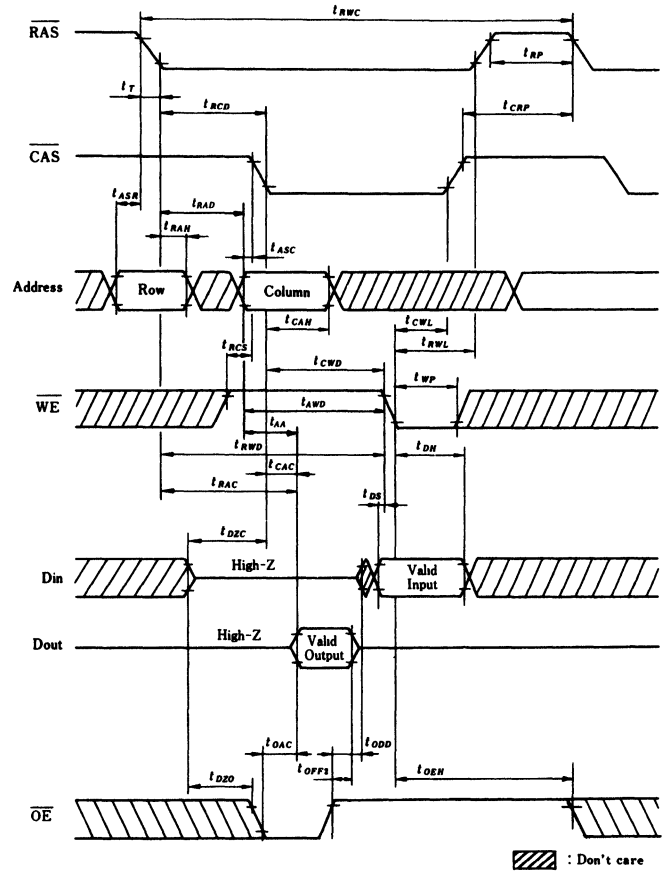
• Early Write Cycle



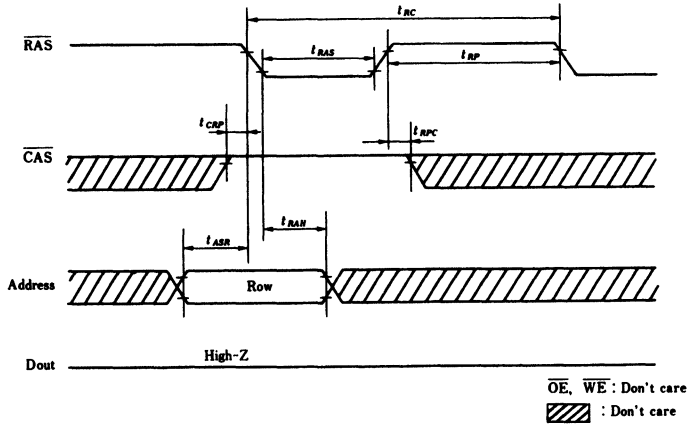
• Delayed Write Cycle



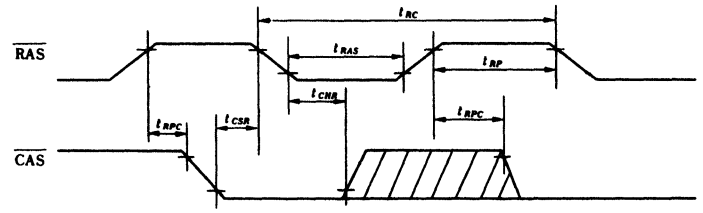
• **Read-Modify-Write Cycle**



• **$\overline{RAS}$ Only Refresh Cycle**



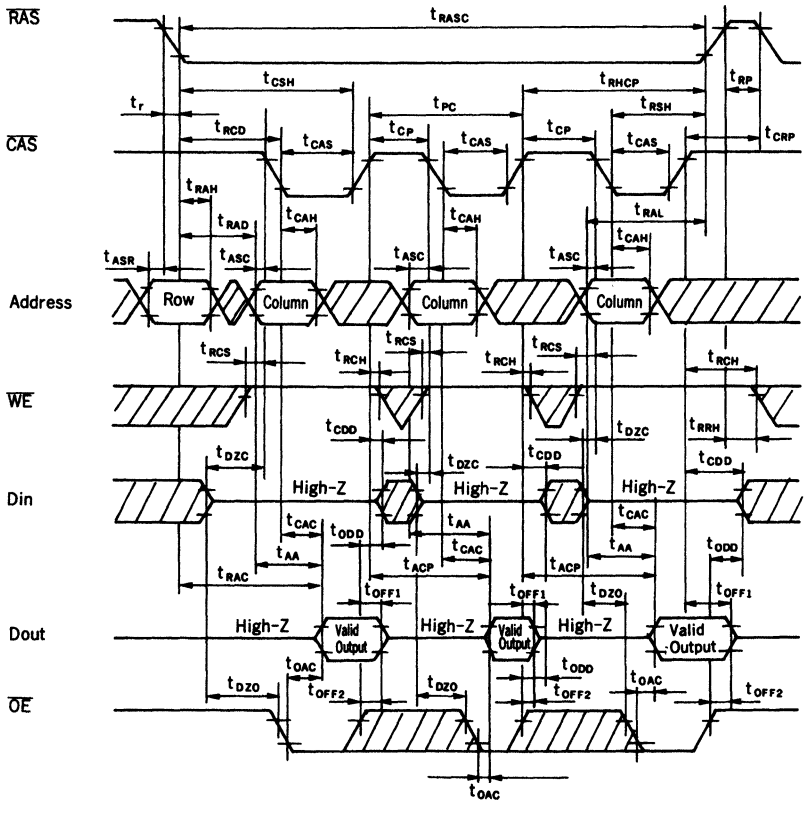
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Address, Din, $\overline{WE}$: Don't care
Dout : High-Z
▨ : Don't care

0136-10

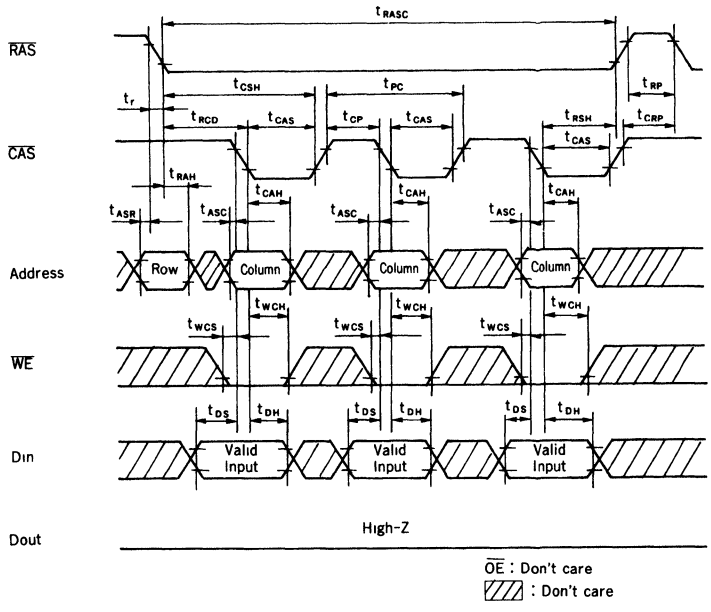
• Fast Page Mode Read Cycle



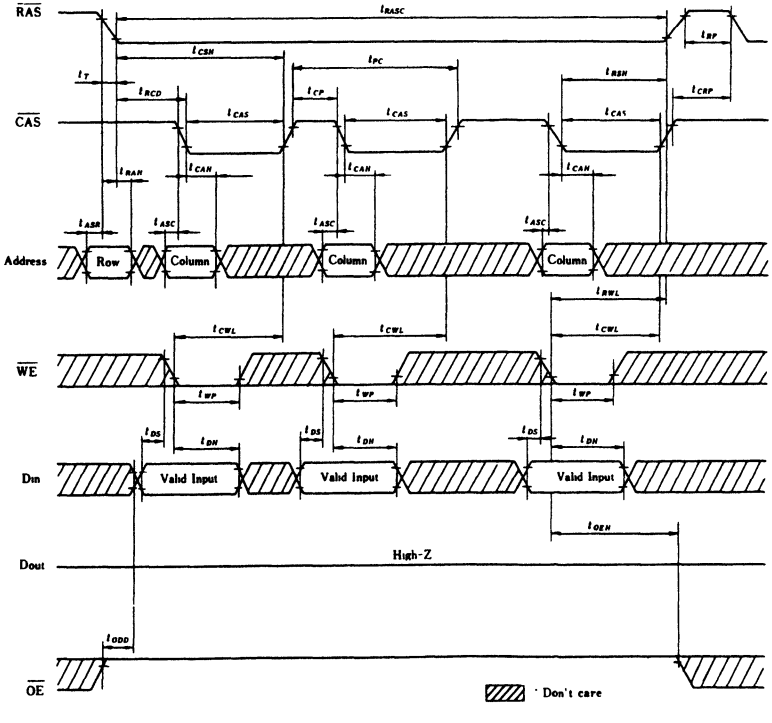
▨ : Don't care

0136-11

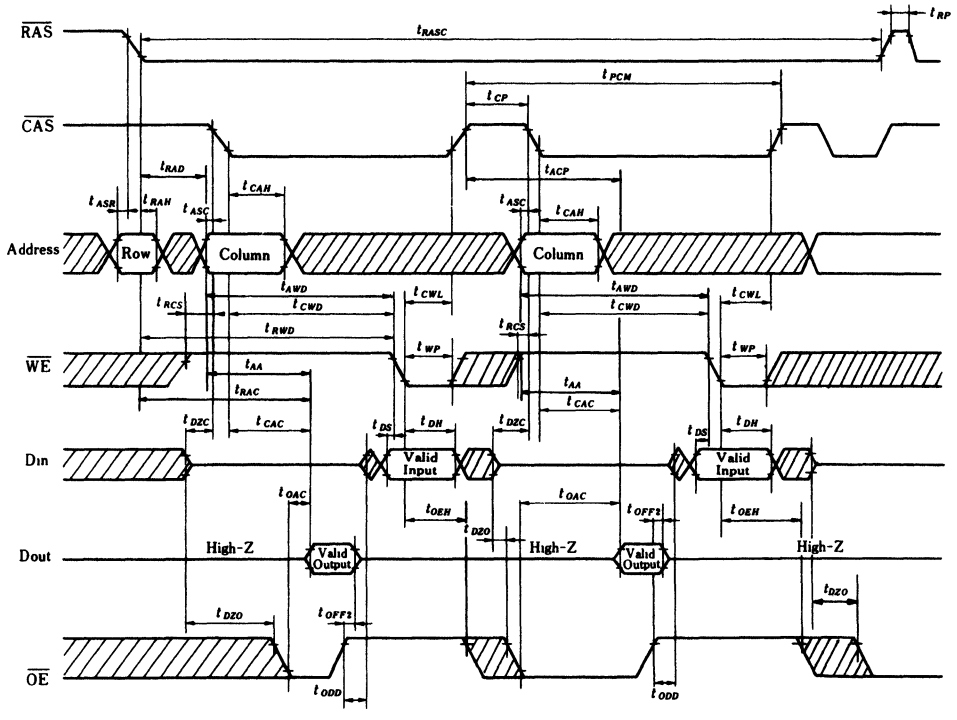
• Fast Page Mode Early Write Cycle



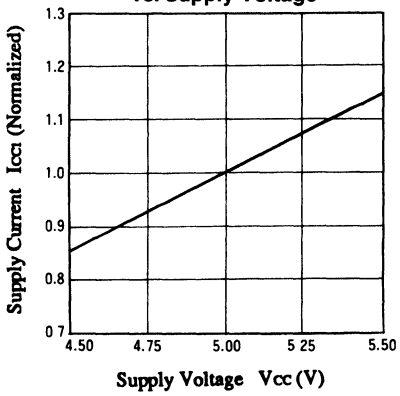
• Fast Page Delayed Write Cycle



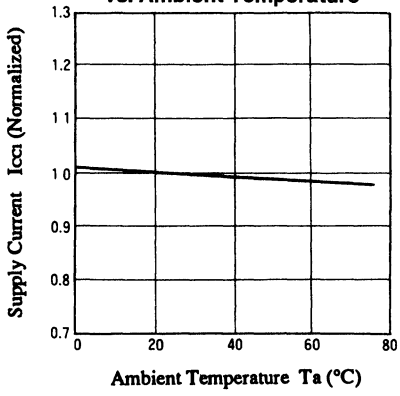
• Fast Page Mode Read-Modify-Write Cycle



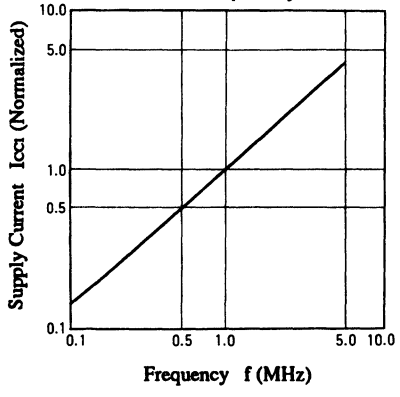
Supply Current (Active) vs. Supply Voltage



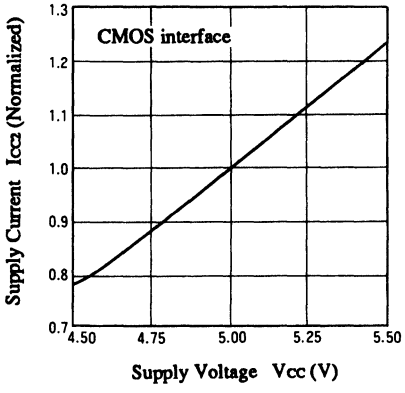
Supply Current (Active) vs. Ambient Temperature



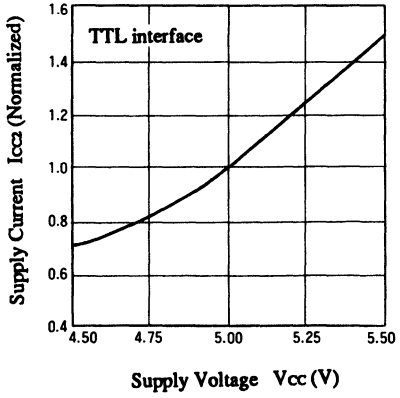
Supply Current (Active) vs. Frequency



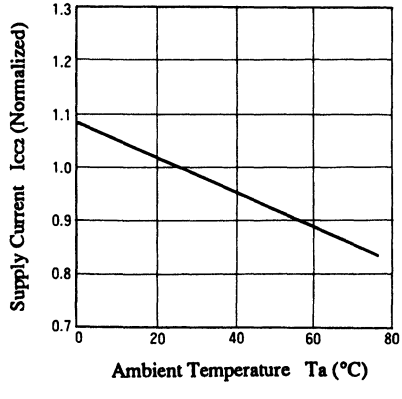
Supply Current (Standby) vs. Supply Voltage



Supply Current (Standby) vs. Supply Voltage

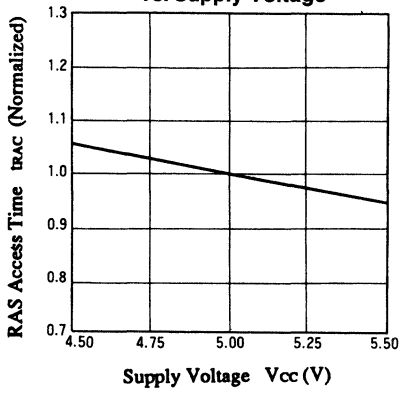


Supply Current (Standby) vs. Ambient Temperature

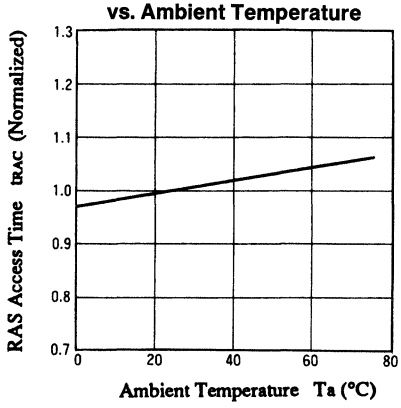


0136-15

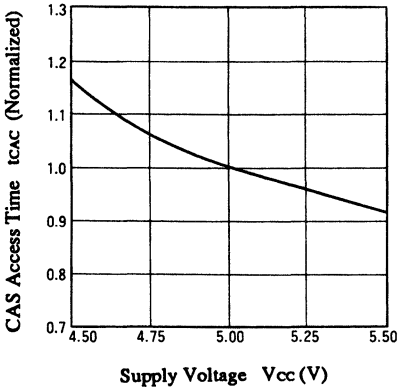
$\overline{RAS}$ Access Time vs. Supply Voltage



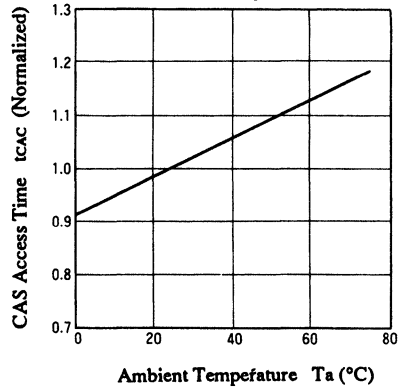
$\overline{RAS}$ Access Time vs. Ambient Temperature



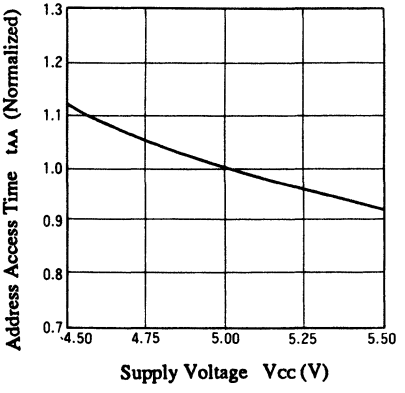
$\overline{CAS}$ Access Time vs. Supply Voltage



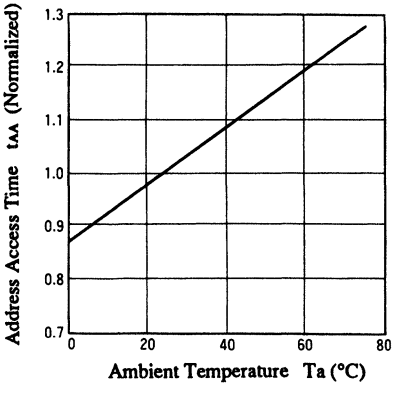
$\overline{CAS}$ Access Time vs. Ambient Temperature



Address Access Time vs. Supply Voltage



Address Access Time vs. Ambient Temperature



0136-16

HM514258A Series

262,144-Word X 4-Bit CMOS Dynamic RAM

■ DESCRIPTION

The Hitachi HM514258A is a CMOS dynamic RAM organized 262144-word x 4-bit. HM514258A has realized higher density, higher performance and various functions by employing 1.3 μm CMOS technology and some new CMOS circuit design technologies. The HM514258A offers Static Column Mode as a high speed access mode.

Multiplexed address input permits the HM514258A to be packaged in standard 20-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

■ FEATURES

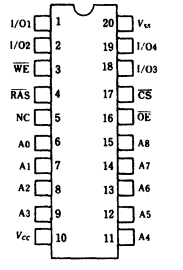
- Single 5V (±10%)
- High Speed
  - Access Time .....60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low Power
  - Standby .....11 mW (max)
  - Active .....495 mW/440 mW/413 mW/358 mW/303 mW (max)
- Static Column Mode Capability
- 512 Refresh Cycles .....(8 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CS}$ Before $\overline{RAS}$ Refresh

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM514258AP-6	60 ns	300 mil 20-pin Plastic DIP (DP-20NA)
HM514258AP-7	70 ns	
HM514258AP-8	80 ns	
HM514258AP-10	100 ns	
HM514258AP-12	120 ns	
HM514258AJP-6	60 ns	300 mil 20-pin Plastic SOJ (CP-20D)
HM514258AJP-7	70 ns	
HM514258AJP-8	80 ns	
HM514258AJP-10	100 ns	
HM514258AJP-12	120 ns	
HM514258AZP-6	60 ns	400 mil 20-pin Plastic ZIP (ZP-20)
HM514258AZP-7	70 ns	
HM514258AZP-8	80 ns	
HM514258AZP-10	100 ns	
HM514258AZP-12	120 ns	

■ PIN OUT

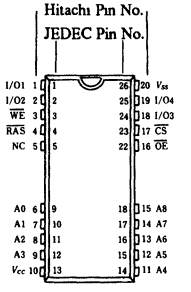
HM514258AP Series



0114-1

(Top View)

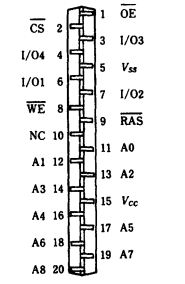
HM514258AJP Series



0114-2

(Top View)

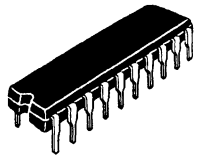
HM514258AZP Series



0114-3

(Bottom View)

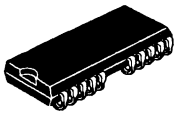
HM514258AP Series



3DDP20NA

(DP-20NA)

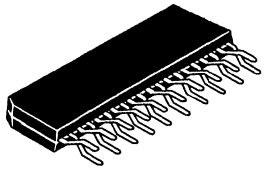
HM514258AJP Series



3DCP20D

(CP-20D)

HM514258AZP Series



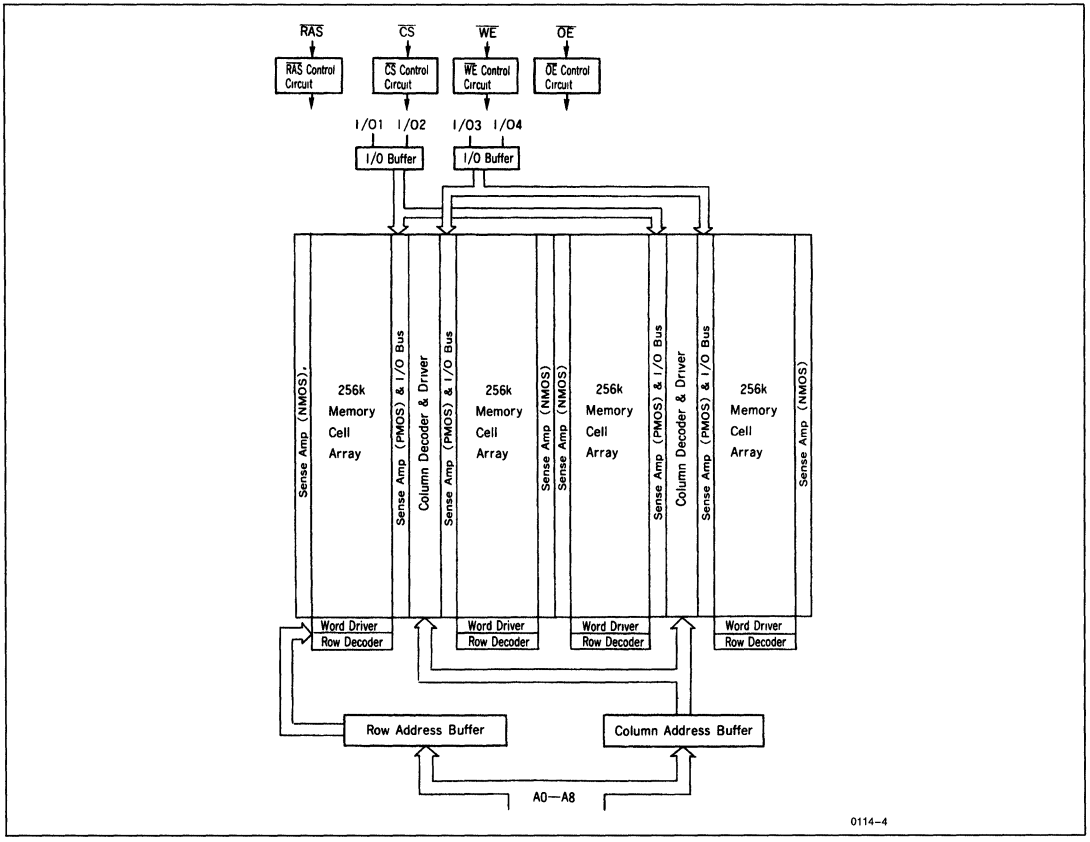
3DZP20

(ZP-20)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Input
A_0–A_8	Refresh Address Input
I/O_0–I/O_4	Data Input/Data Output
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	I/O Pin	V_{IL}	−1.0	—	0.8	V	1
	Others	V_{IL}	−2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	75	—	65	—	55	mA	$\overline{RAS}$, $\overline{CS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CS}$ = V_{IH}, D_{out} = High-Z	
		—	1	—	1	—	1	—	1	—	1	mA	CMOS Interface, $\overline{RAS}$, $\overline{CS} \geq V_{CC} - 0.2V$, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	90	—	80	—	75	—	65	—	55	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	80	—	70	—	65	—	55	—	45	mA	t_{RC} = Min	
Static Column Mode Current	I_{CC9}	—	80	—	70	—	65	—	55	—	45	mA	t_{SC} = Min	1, 3
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	$0V \leq V_{in} \leq 7V$	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	$0V \leq V_{out} \leq 7V$, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Input/Output Capacitance (Data Input, Data Output)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[17, 18]

Test Conditions

Input Rise and Fall Times:	5 ns
Input timing reference levels:	0.8V, 2.4V
Output load:	2 TTL Gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	120	—	130	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	50	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CS}$ Pulse Width	t_{SP}	20	10000	20	10000	25	10000	30	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASW}	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{AHW}	15	—	15	—	20	—	25	—	25	—	ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	70	25	90	ns	8
$\overline{RAS}$ Hold Time	t_{RSL}	20	—	20	—	25	—	30	—	30	—	ns	
$\overline{CS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CS}$ to $\overline{RAS}$ Precharge Time	t_{SRS}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	20	—	20	—	20	—	25	—	30	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	0	—	0	—	ns	
$\overline{CS}$ Delay Time from D_{in}	t_{DZC}	0	—	0	—	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	1, 7
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ms	

Read Cycle

Parameter	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access Time from $\overline{CS}$	t_{ACS}	—	20	—	20	—	25	—	30	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	50	—	55	ns	3, 5, 14
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	—	25	—	30	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	

Read Cycle (continued)

Parameter	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to Column Address Hold Time	t_{AHR}	15	—	15	—	15	—	15	—	15	—	ns	16
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	50	20	65	ns	9
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	50	—	55	—	ns	
Column Address Hold Time from $\overline{RAS}$	t_{AR}	60	—	70	—	80	—	100	—	120	—	ns	
Output Buffer Turn-off Time	t_{OFF}	—	20	—	20	—	20	—	25	—	30	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	—	20	—	20	—	20	—	25	—	30	ns	6
Output Hold Time from Address	t_{AOH}	5	—	5	—	5	—	5	—	5	—	ns	
$\overline{CS}$ to D_{in} Delay Time	t_{CDD}	20	—	20	—	20	—	25	—	30	—	ns	
$\overline{CS}$ Hold Time from $\overline{OE}$	t_{OCH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{OE}$ Hold Time from $\overline{RAS}$	t_{ROH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{OE}$ Hold Time from $\overline{CS}$	t_{COH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{OE}$ Pulse Width	t_{OEP}	20	—	20	—	25	—	25	—	30	—	ns	

Write Cycle

Parameter	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	25	—	25	—	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	55	—	65	—	75	—	95	—	115	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	25	—	30	—	ns	
Write Command to $\overline{CS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	25	—	30	—	ns	
D_{in} Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	11
D_{in} Hold Time	t_{DH}	15	—	15	—	20	—	25	—	25	—	ns	11
D_{in} Hold Time to $\overline{RAS}$	t_{DHR}	55	—	65	—	75	—	95	—	115	—	ns	
Column Address Hold Time from $\overline{RAS}$	t_{AWR}	55	—	65	—	75	—	95	—	115	—	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	170	—	180	—	220	—	255	—	295	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	85	—	93	—	110	—	135	—	160	—	ns	10
$\overline{CS}$ to $\overline{WE}$ Delay Time	t_{CWD}	45	—	45	—	55	—	65	—	70	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	55	—	60	—	70	—	85	—	95	—	ns	10

Refresh Cycle

Parameter	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CS}$ Setup Time ($\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CS}$ Hold Time ($\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CS}$ Hold Time	t_{ZRH}	10	—	10	—	10	—	10	—	10	—	ns	

Static Column Mode Cycle

Parameter	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Static Column Mode Cycle Time	t_{SC}	35	—	40	—	45	—	55	—	60	—	ns	
Static Column Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	ns	
$\overline{RAS}$ to Second $\overline{WE}$ Delay Time	t_{RSWD}	70	—	80	—	90	—	110	—	135	—	ns	
Static Column Mode $\overline{CS}$ Precharge Time	t_{SI}	10	—	10	—	10	—	10	—	15	—	ns	
Static Column Mode $\overline{WE}$ Precharge Time	t_{WI}	10	—	10	—	10	—	10	—	15	—	ns	

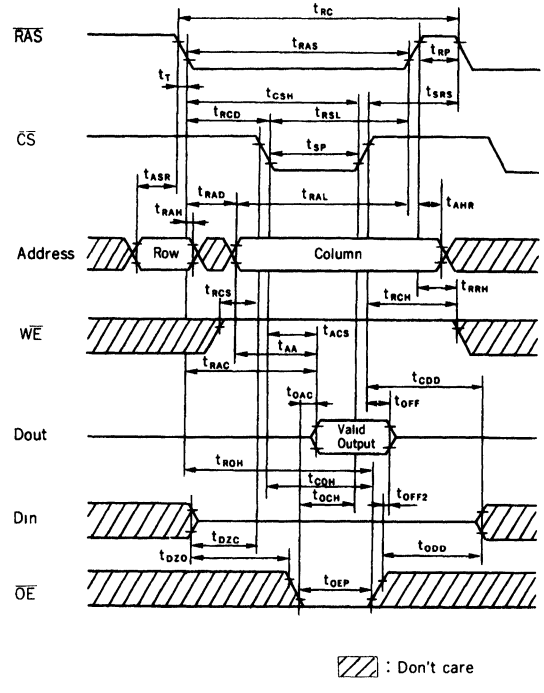
Static Column Mode Read-Modify-Write Cycle and Mixed Cycle

Parameter	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Static Column Mode Cycle Time on Read-Modify-Write	t_{SRW}	90	—	100	—	120	—	140	—	160	—	ns	12
Access Time from First $\overline{WE}$	t_{ALW}	—	65	—	75	—	85	—	100	—	115	ns	3, 13
Last $\overline{WE}$ to Column Address Delay Time	t_{LWAD}	20	35	20	40	25	45	25	50	30	60	ns	15
Last $\overline{WE}$ to Column Address Hold Time	t_{AHLW}	65	—	75	—	85	—	100	—	115	—	ns	

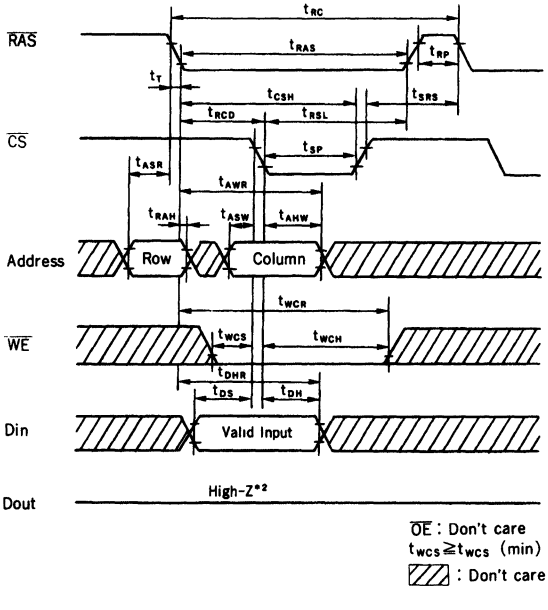
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL load and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{ACS}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min) the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. t_{SRW} (min) = t_{AWD} (min) + t_{LWAD} (max) + t_T
13. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} exceeds the value shown.
14. Assumes that $t_{LWAD} \geq t_{LWAD}$ (max).
15. Operation with the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met, t_{LWAD} (max) is specified as a reference point only, if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AHR} is defined as the time at which the column address hold is set.
17. An initial pause of 100 μs is required after power-up followed by eight or more initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If internal refresh counter is used, eight or more $\overline{CS}$ before $\overline{RAS}$ refresh cycles are required.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffers prior to applying data to the device.

■ TIMING WAVEFORMS

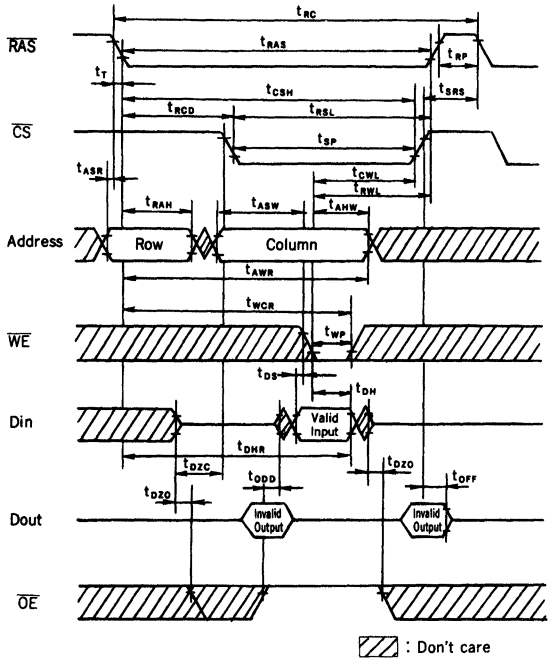
• Read Cycle



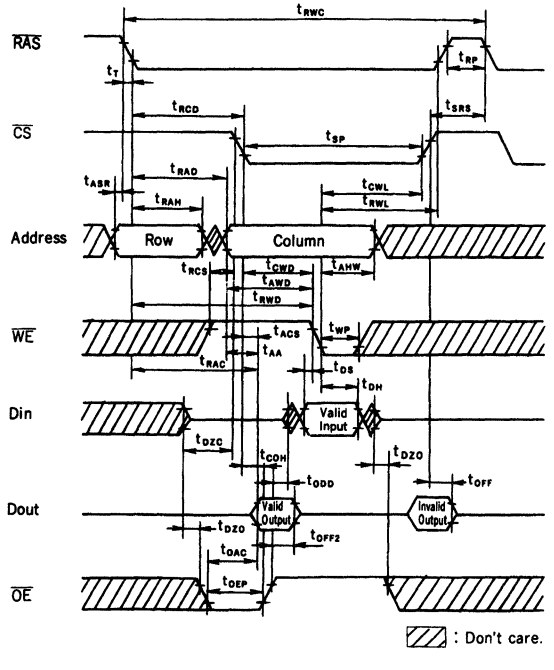
• Early Write Cycle



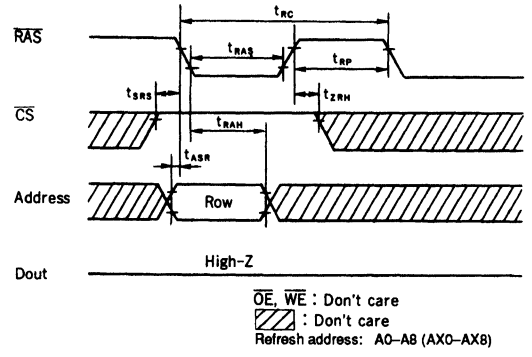
• **Delayed Write Cycle**



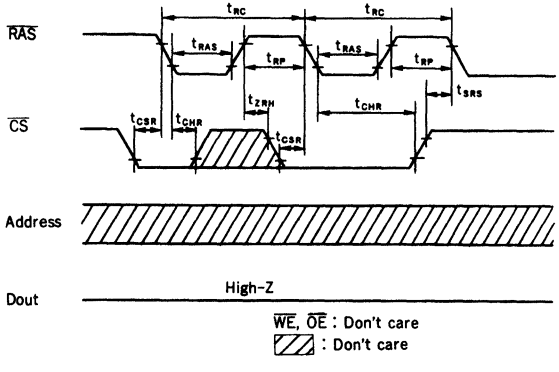
• **Read-Modify-Write Cycle**



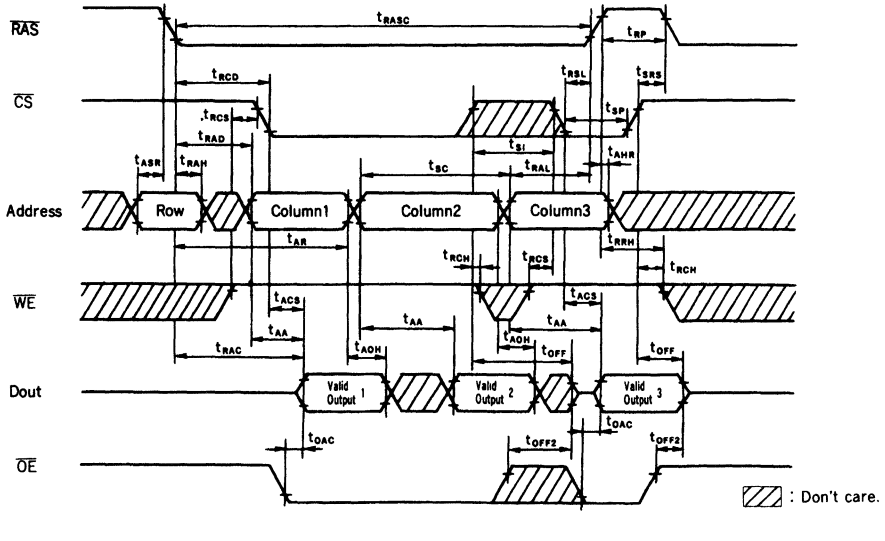
• $\overline{RAS}$ Only Refresh Cycle



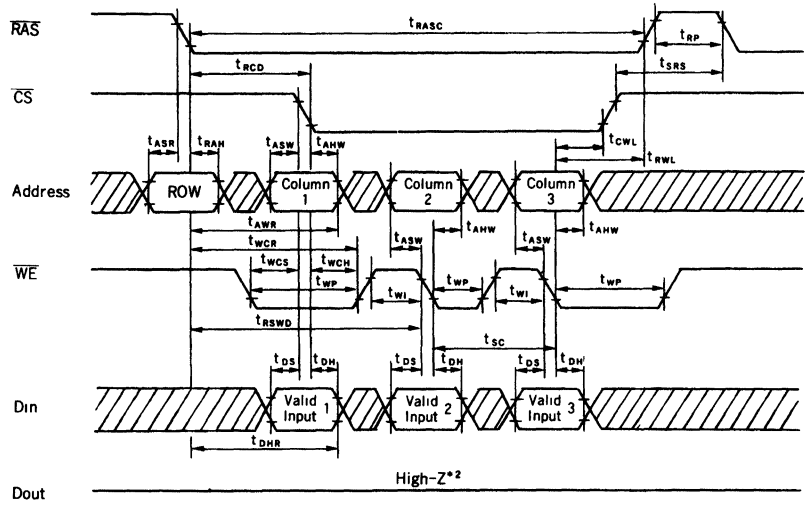
• $\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle



• Static Column Mode Read Cycle



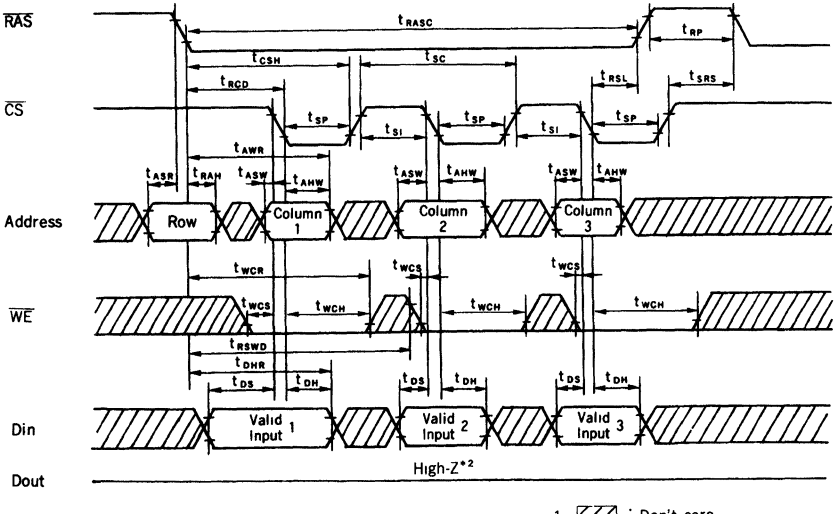
• Static Column Mode Write Cycle (1)



1. ▨ : Don't care
2. $t_{WCS} \geqq t_{WCS}(min)$
3. $\overline{OE}$: Don't care

0114-12

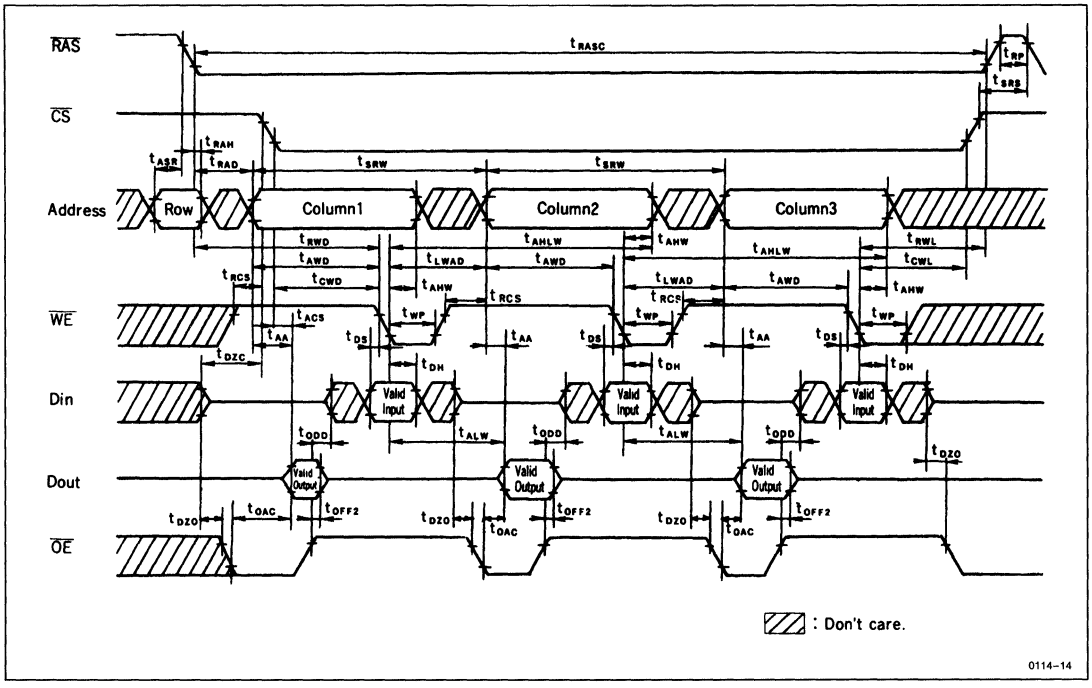
• Static Column Mode Write Cycle (2)



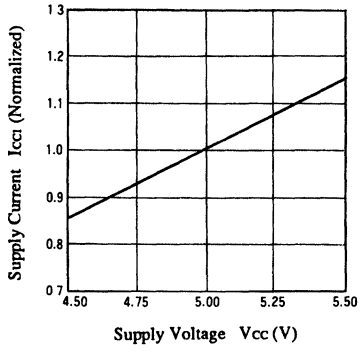
1. ▨ : Don't care.
2. $t_{WCS} \geqq t_{WCS}(min)$
3. $\overline{OE}$: Don't care.

0114-13

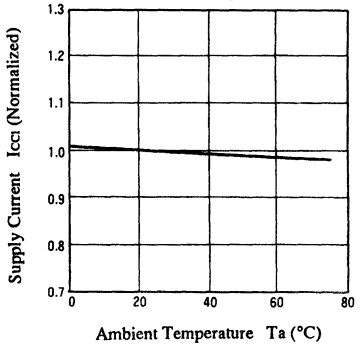
• **Static Column Mode Read-Modify-Write Cycle**



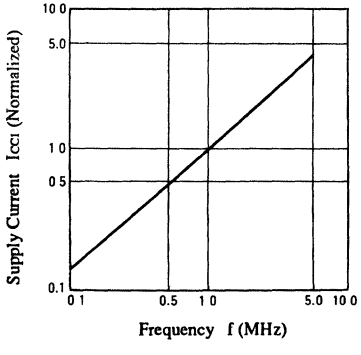
Supply Current (Active) vs Supply Voltage



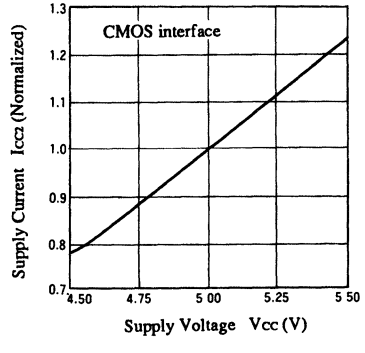
Supply Current (Active) vs Ambient Temperature



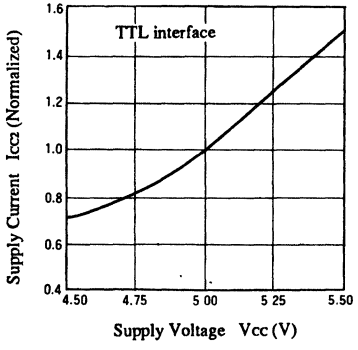
Supply Current (Active) vs Frequency



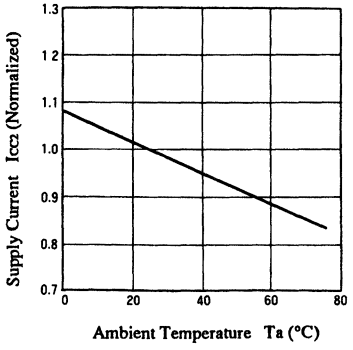
Supply Current (Standby) vs Supply Voltage



Supply Current (Standby) vs Supply Voltage

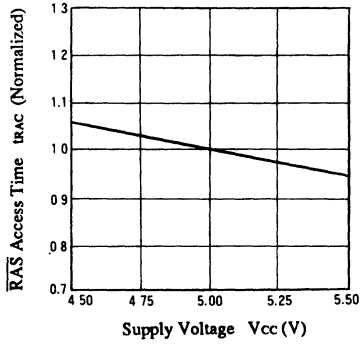


Supply Current (Standby) vs Ambient Temperature

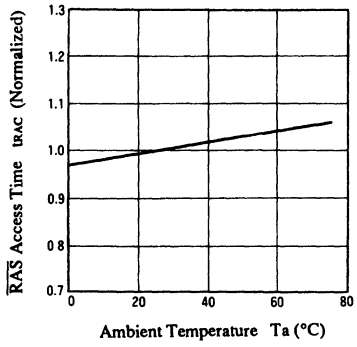


0114-15

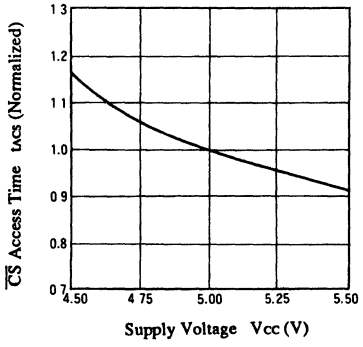
$\overline{RAS}$ Access Time vs Supply Voltage



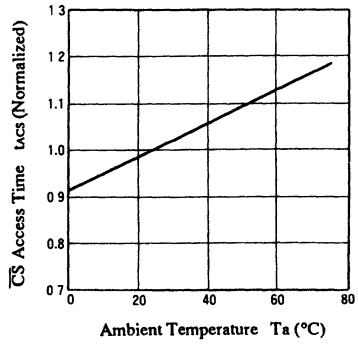
$\overline{RAS}$ Access Time vs Ambient Temperature



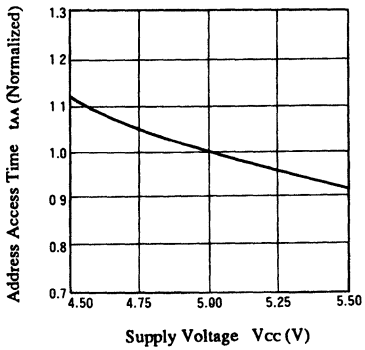
$\overline{CS}$ Access Time vs Supply Voltage



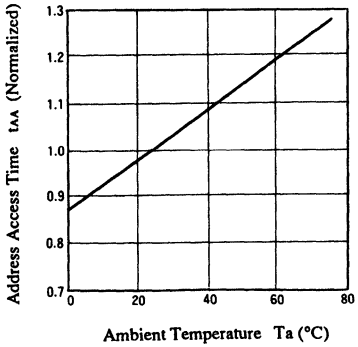
$\overline{CS}$ Access Time vs Ambient Temperature



Address Access Time vs Supply Voltage



Address Access Time vs Ambient Temperature



0114-16

HM514266 Series

262,144-Word x 4-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514266A is a CMOS dynamic RAM organized 262,144-word x 4-bit. HM514266A has realized higher density, higher performance and various functions by employing 1.3 μm CMOS process technology and some new CMOS circuit design technologies. The HM514266A offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514266A to be packaged in standard 20-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

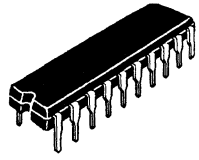
■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode .....495 mW/440 mW/363 mW/303 mW/259 mW (max)
  - Standby Mode.....11 mW (max)
- Fast Page Mode Capability
- 512 Refresh Cycles .....(8 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Write per Bit Capability

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM514266AP-6	60 ns	300 mil 20-pin Plastic DIP (DP-20NA)
HM514266AP-7	70 ns	
HM514266AP-8	80 ns	
HM514266AP-10	100 ns	
HM514266AP-12	120 ns	
HM514266AJP-6	60 ns	300 mil 20-pin Plastic SOJ (CP-20D)
HM514266AJP-7	70 ns	
HM514266AJP-8	80 ns	
HM514266AJP-10	100 ns	
HM514266AJP-12	120 ns	
HM514266AZP-6	60 ns	400 mil 20-pin Plastic ZIP (ZP-20)
HM514266AZP-7	70 ns	
HM514266AZP-8	80 ns	
HM514266AZP-10	100 ns	
HM514266AZP-12	120 ns	

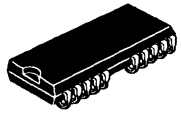
HM514266AP Series



3DDP20NA

(DP-20NA)

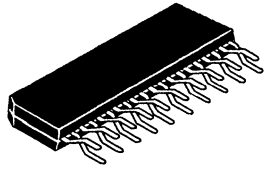
HM514266AJP Series



3DCP20D

(CP-20D)

HM514266AZP Series



3DZP20

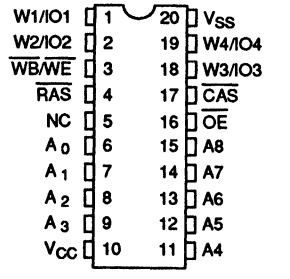
(ZP-20)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Input
A_0–A_8	Refresh Address Input
W_1/IO_1–W_1/IO_4	Write Select/ Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB}/\overline{WE}$	Write Per Bit/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply (+5.0V)
V_{SS}	Ground

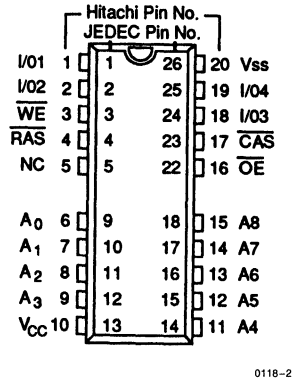
■ PIN OUT

HM514266AP Series



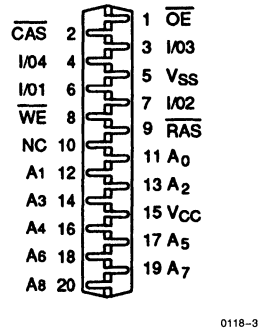
(Top View)

HM514266AJP Series



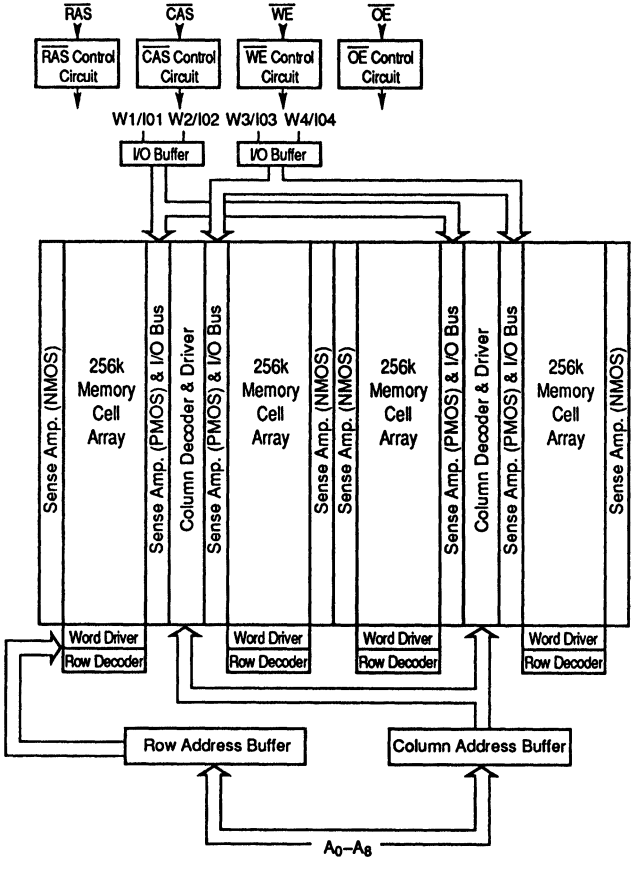
(Top View)

HM514266AZP Series



(Bottom View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	− 1.0	—	0.8	V	1
	(Others)	V_{IL}	− 2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	514266A-6		514266A-7		514266A-8		514266A-10		514266A-12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	66	—	55	—	47	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	1	—	1	—	1	—	1	—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	90	—	80	—	66	—	55	—	47	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	80	—	70	—	66	—	55	—	47	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	80	—	70	—	55	—	55	—	47	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 14]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	514266A-6		514266A-7		514266A-8		514266A-10		514266A-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	120	—	130	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	50	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	20	—	20	—	20	—	25	—	30	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	0	—	0	—	ns	
$\overline{CAS}$ Delay Time from D_{in}	t_{DZC}	0	—	0	—	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ms	

Read Cycle

Parameter	Symbol	514266A-6		514266A-7		514266A-8		514266A-10		514266A-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	55	ns	3, 5
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	—	25	—	30	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	20	—	35	—	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	—	20	—	20	—	20	—	25	—	30	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	—	20	—	20	—	20	—	25	—	30	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	20	—	20	—	20	—	25	—	30	—	ns	

Write Cycle

Parameter	Symbol	514266A-6		514266A-7		514266A-8		514266A-10		514266A-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	25	—	30	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	20	—	25	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	514266A-6		514266A-7		514266A-8		514266A-10		514266A-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read-Write Cycle Time	t_{RWC}	170	—	180	—	220	—	255	—	295	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	85	—	95	—	110	—	135	—	160	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	45	—	45	—	55	—	60	—	70	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	55	—	60	—	70	—	80	—	95	—	ns	10
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	20	—	20	—	25	—	25	—	30	—	ns	

Refresh Cycle

Parameter	Symbol	514266A-6		514266A-7		514266A-8		514266A-10		514266A-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	514266A-6		514266A-7		514266A-8		514266A-10		514266A-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	—	50	—	60	ns	13
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	50	—	60	—	ns	
Fast Page Mode Read-Write Cycle Time	t_{PCM}	95	—	100	—	110	—	115	—	135	—	ns	

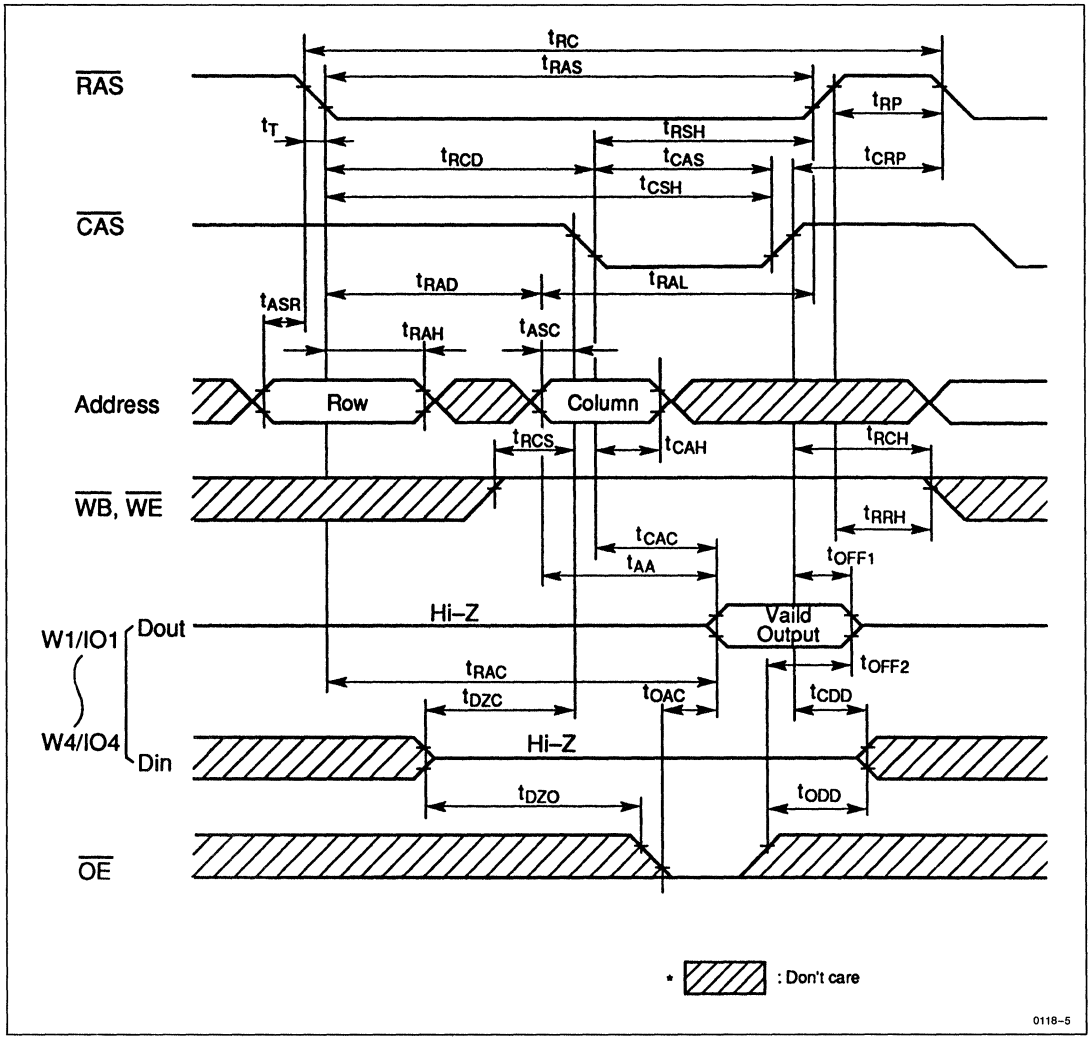
Write Per Bit[15, 16]

Parameter	Symbol	514266A-6		514266A-7		514266A-8		514266A-10		514266A-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write per Bit Setup Time	t_{WBS}	0	—	0	—	0	—	0	—	0	—	ns	
Write per Bit Hold Time	t_{WBH}	10	—	10	—	12	—	15	—	15	—	ns	
Write per Bit Selection Setup time	t_{WDS}	0	—	0	—	0	—	0	—	0	—	ns	
Write per Bit Selection Hold Time	t_{WDH}	10	—	10	—	12	—	15	—	15	—	ns	

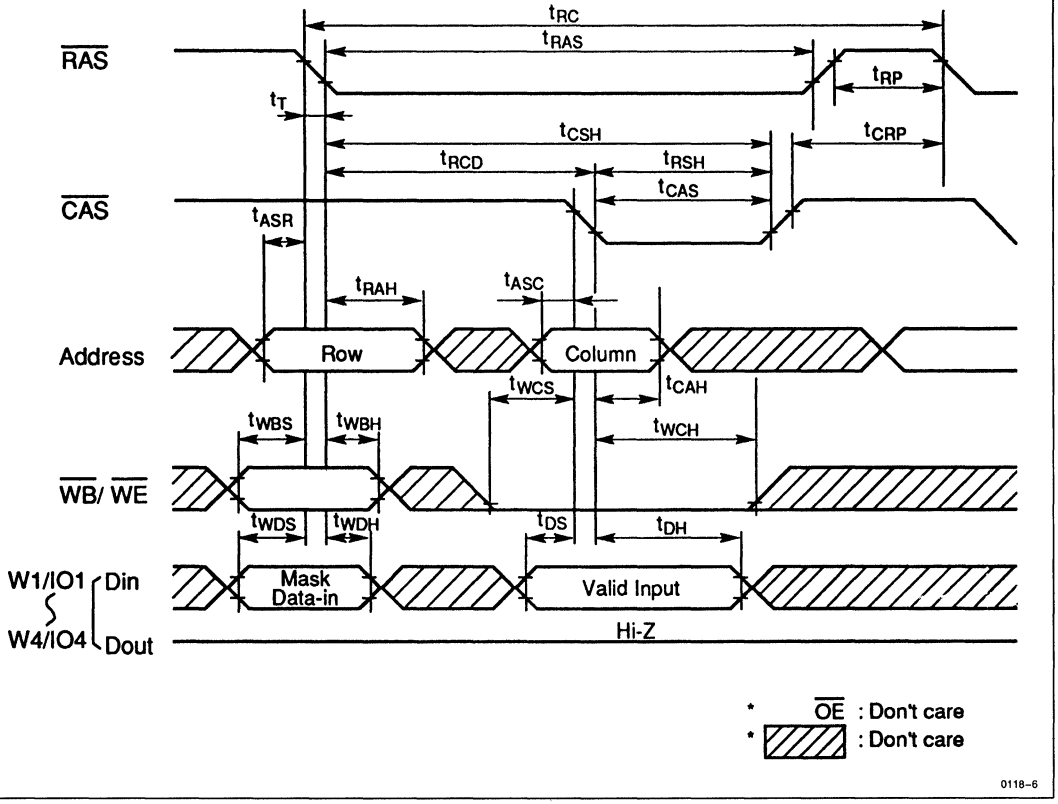
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WB}/\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
15. When using the write-per-bit capability, $\overline{WB}/\overline{WE}$ must be low as $\overline{RAS}$ falls.
16. The data bits to which the write operation is applied can be specified by keeping Wi/IOi high with setup and hold time referenced to the $\overline{RAS}$ negative transition.

■ TIMING WAVEFORMS

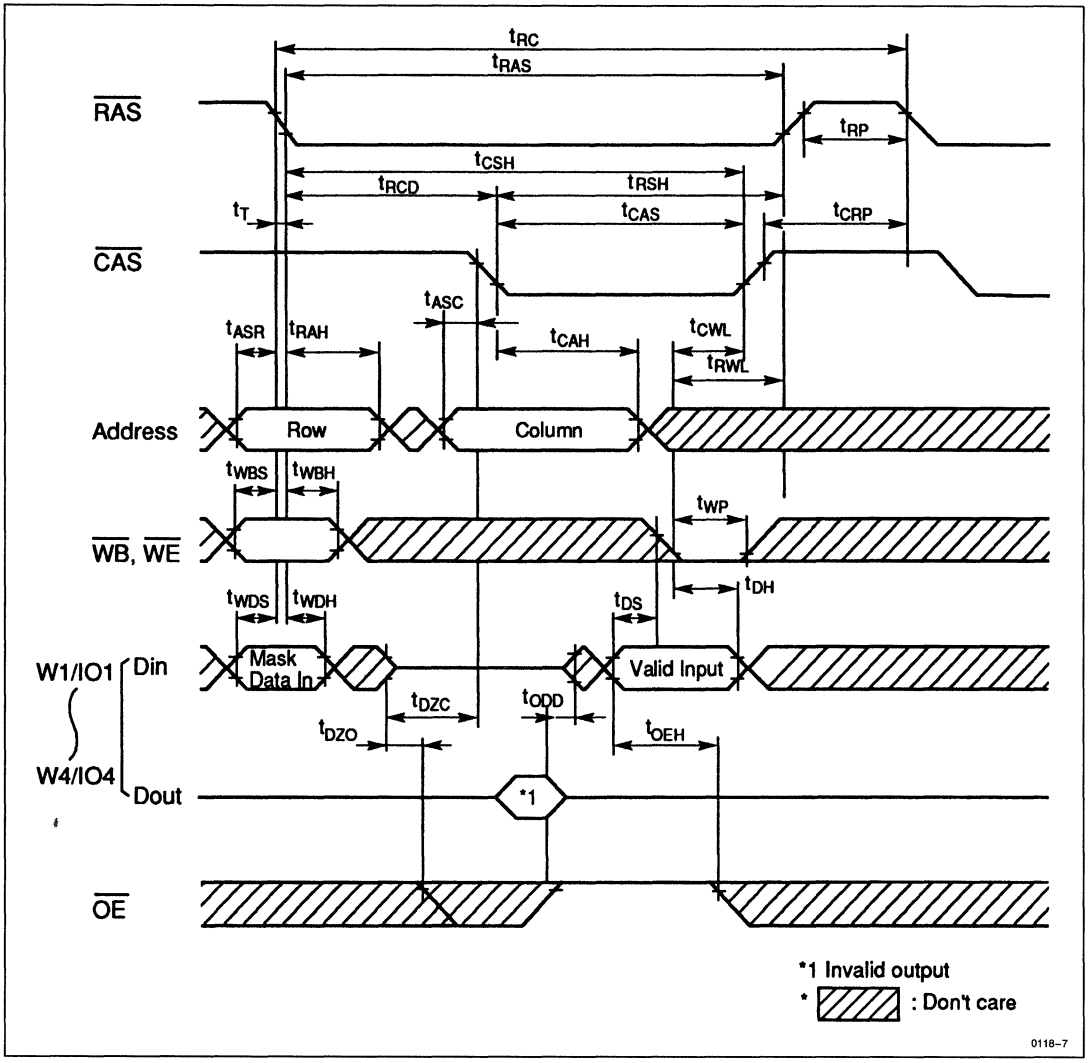
• Read Cycle



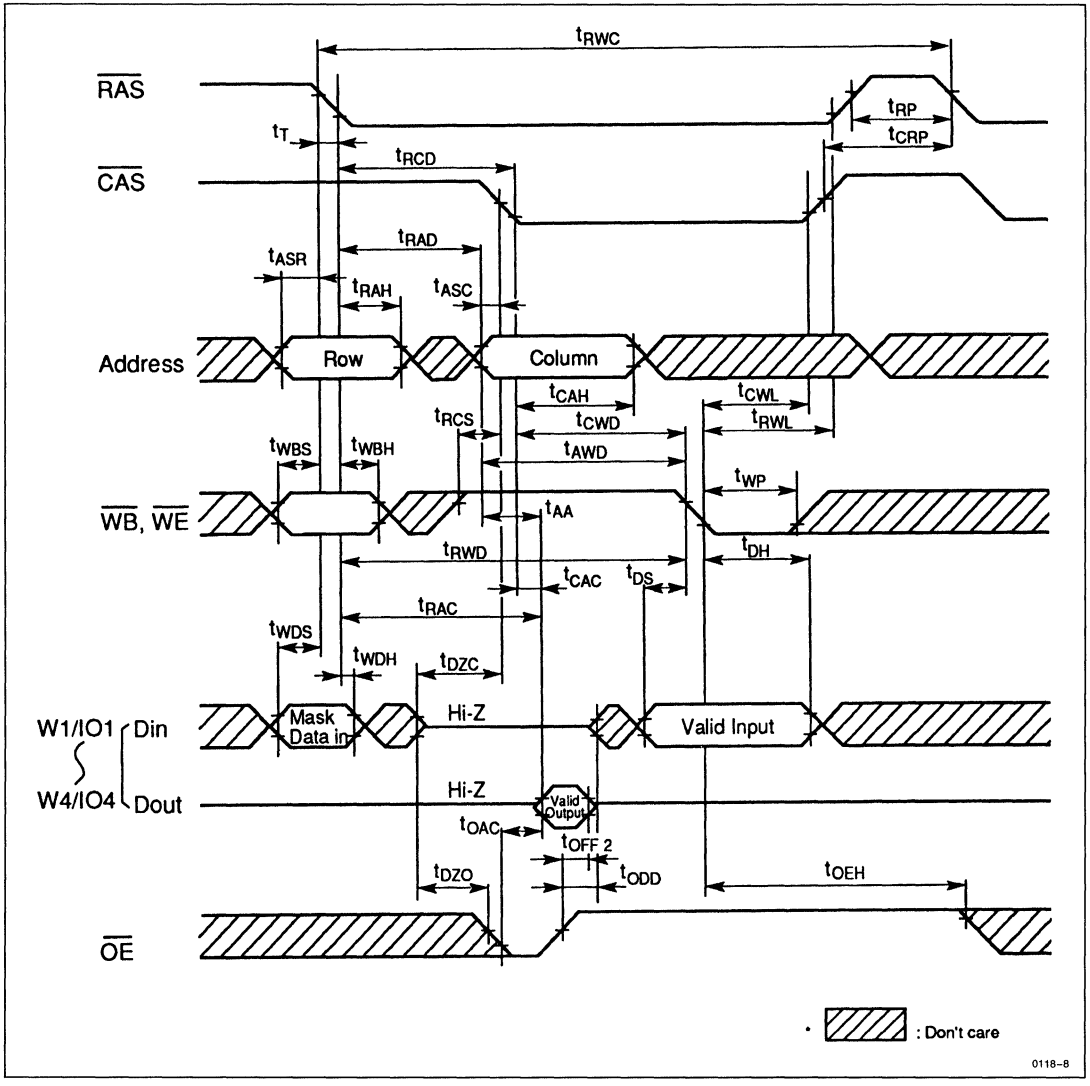
• **Early Write Cycle**



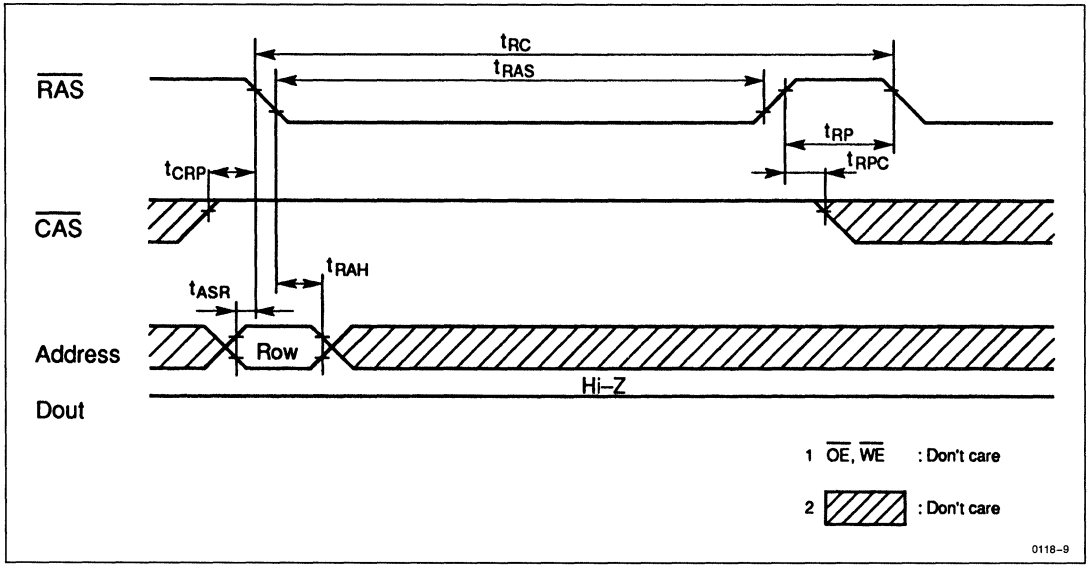
• **Delayed Write Cycle**



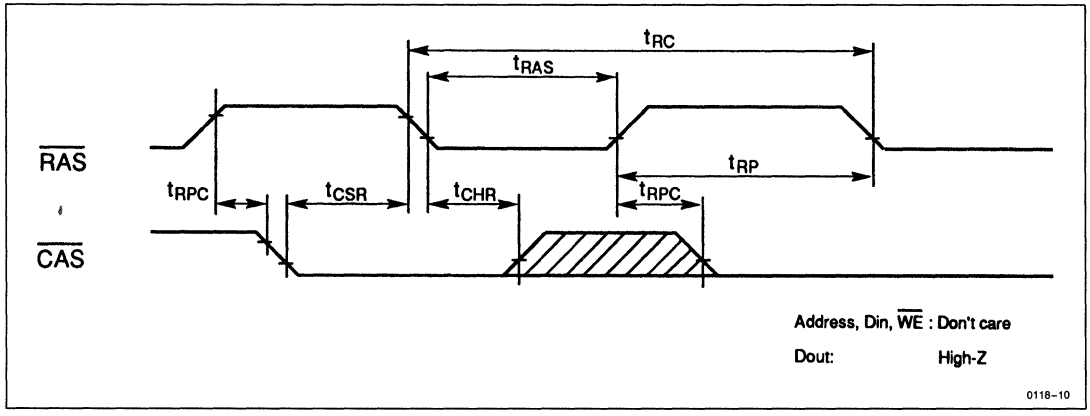
• **Read-Modify-Write Cycle**



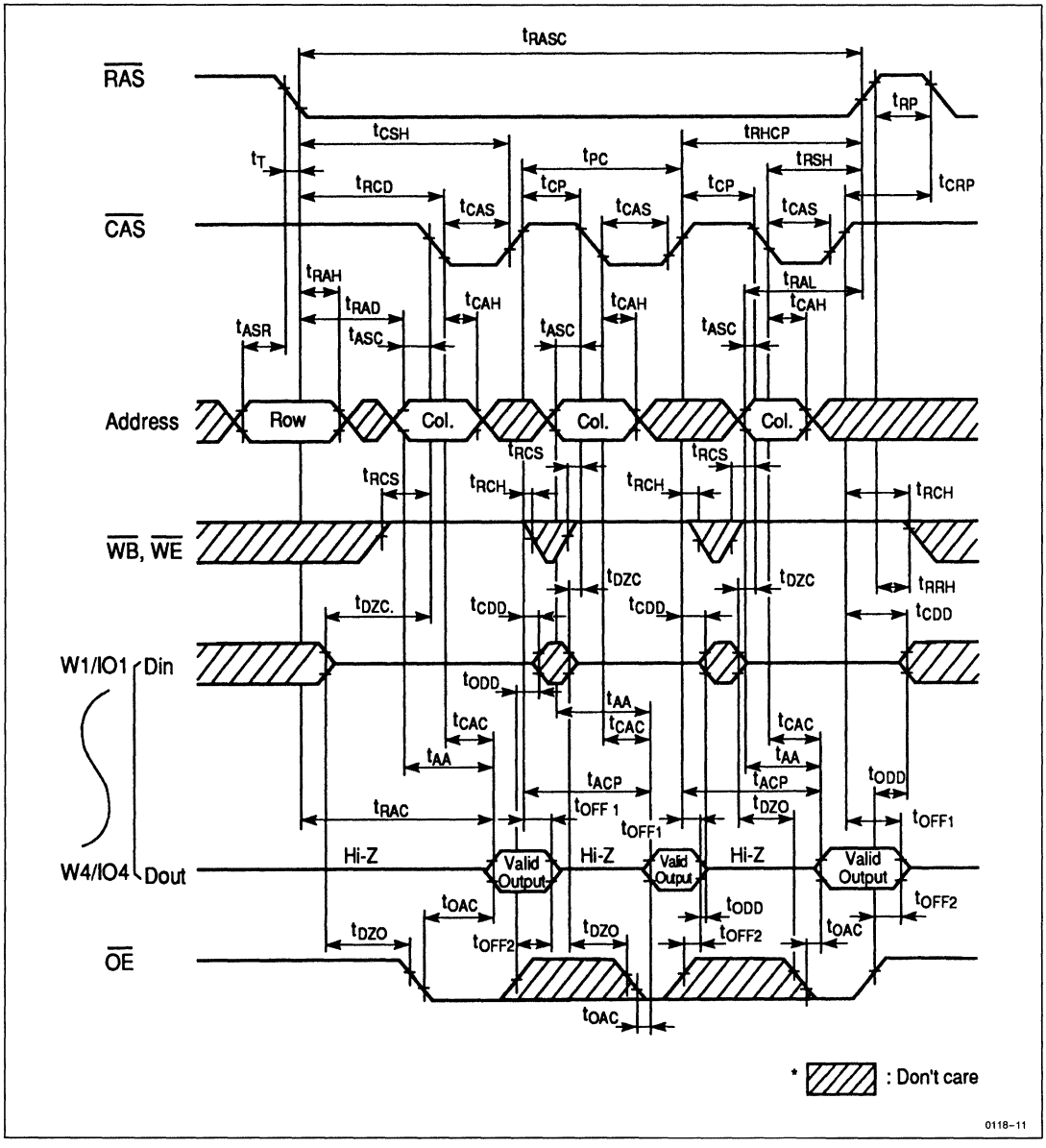
• $\overline{RAS}$ Only Refresh Cycle



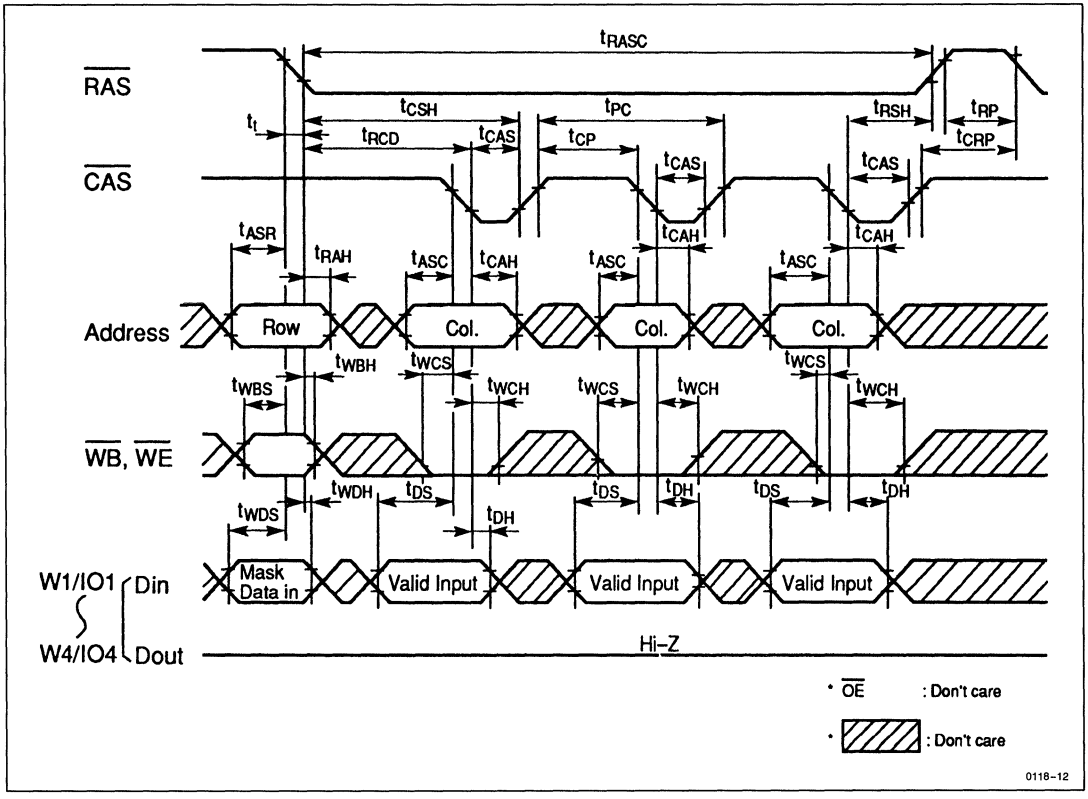
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



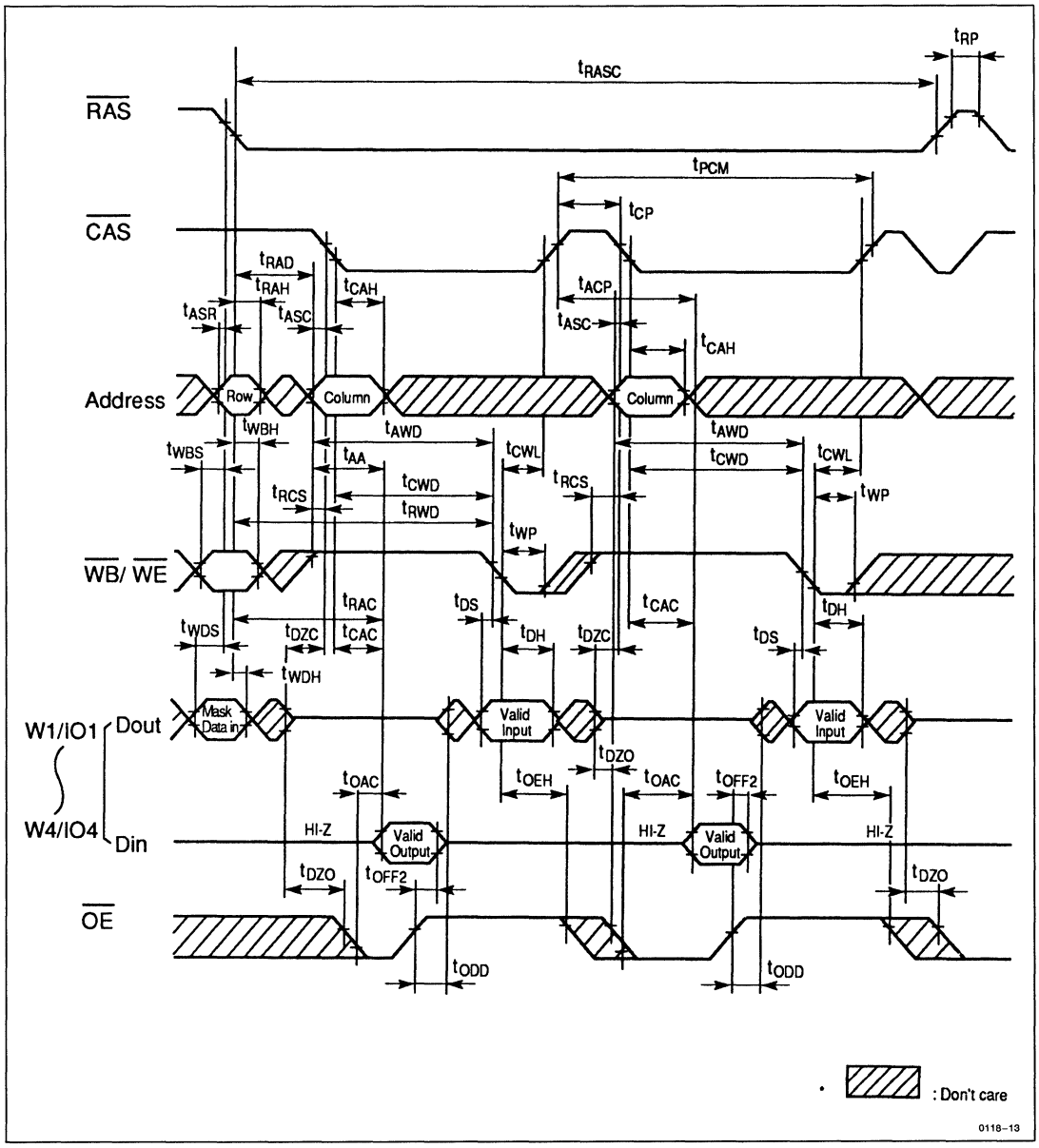
• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



• **Fast Page Mode Read-Modify-Write Cycle**



HM511000A Series
HM511000AL Series

1048576-Word x 1-Bit CMOS Dynamic RAM

■ DESCRIPTION

The Hitachi HM511000A/AL series is a CMOS dynamic RAM organized 1048576-word x 1-bit. HM511000A/AL has realized higher density, higher performance and various functions by employing 1.3 μm CMOS process technology and some new CMOS circuit design technologies.

The HM511000A/AL offers Fast Page Mode as a high speed access mode.

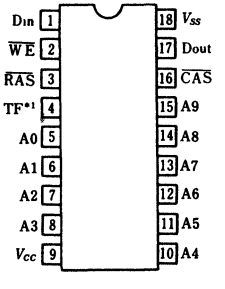
Multiplexed address input permits the HM511000A/AL to be packaged in standard 18-pin plastic DIP, 20-pin plastic ZIP and 20-pin plastic SOJ.

■ FEATURES

- High Speed
  - Access Time .....60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode .....495 mW/440 mW/385 mW/330 mW/275 mW (max)
  - Standby Mode.....11 mW (max)
- Single 5V Supply (±10%)
- Fast Page Mode Capability
- 512 Refresh Cycles .....(8 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh

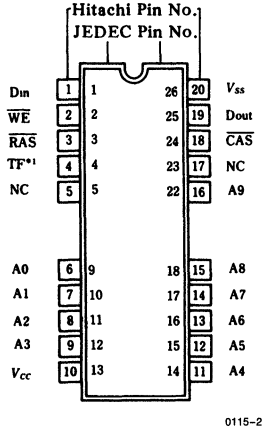
■ PIN OUT

HM511000A/ALP Series



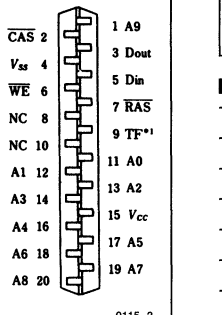
(Top View)

HM511000A/ALJP Series



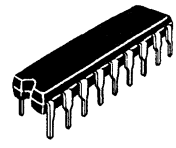
(Top View)

HM511000A/ALZP Series



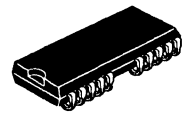
(Bottom View)

HM511000A/ALP Series



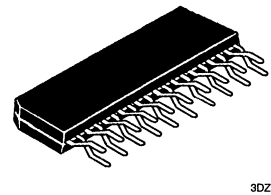
(DP-18C)

HM511000A/ALJP Series



(CP-20D)

HM511000A/ALZP Series



(ZP-20)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_8	Refresh Address Input
D_{in}	Data-in
D_{out}	Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
TF[1]	Test Function
V_{CC}	Power (+ 5V)
V_{SS}	Ground

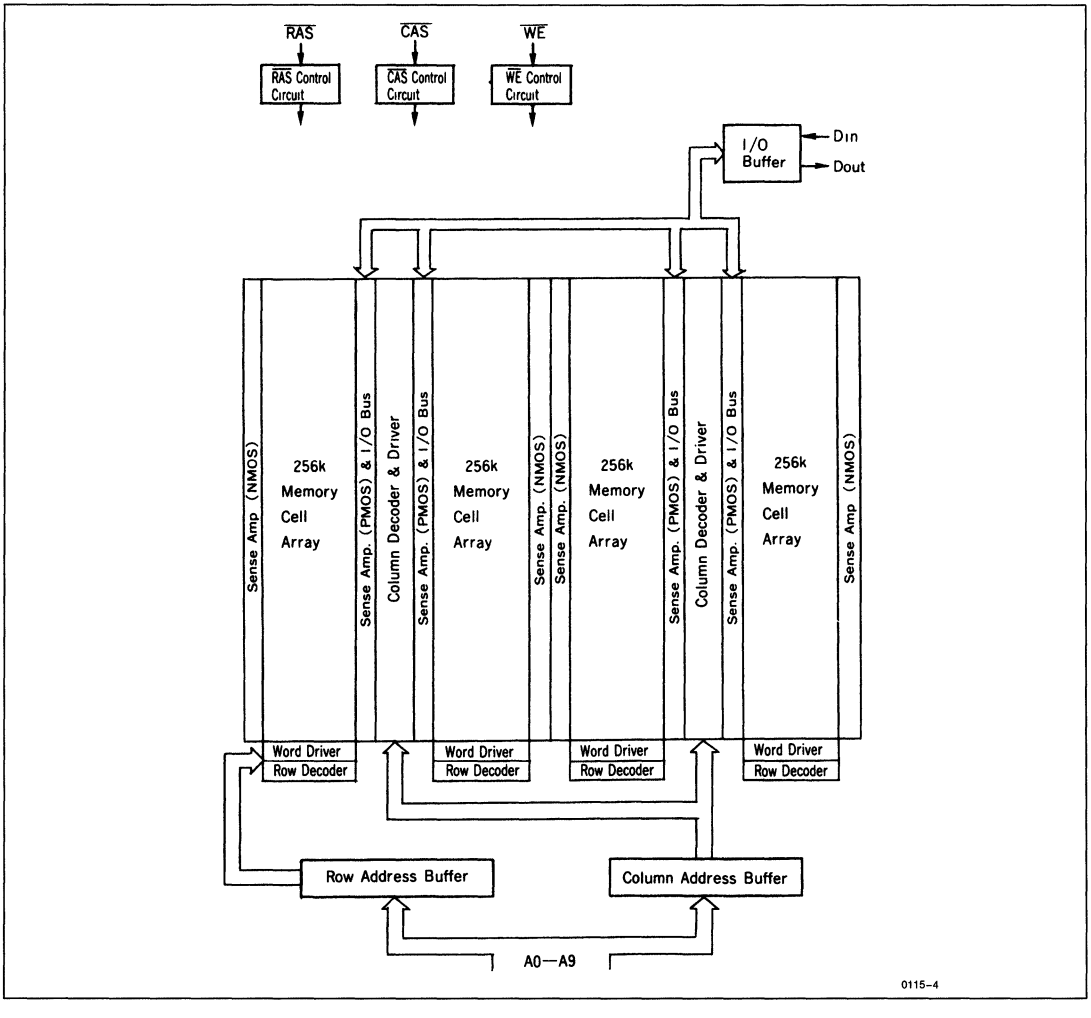
Note: 1. TF pin can be connected with any line or unconnected provided the voltage level of TF pin must be kept lower than V_{CC} + 0.5V.

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM511000AP-6	60 ns	300 mil 18-pin Plastic DIP (DP-18C)
HM511000AP-7	70 ns	
HM511000AP-8	80 ns	
HM511000AP-10	100 ns	
HM511000AP-12	120 ns	
HM511000AJP-6	60 ns	300 mil 20-pin Plastic SOJ (CP-20D)
HM511000AJP-7	70 ns	
HM511000AJP-8	80 ns	
HM511000AJP-10	100 ns	
HM511000AJP-12	120 ns	
HM511000AZP-6	60 ns	400 mil 20-pin Plastic ZIP (ZP-20)
HM511000AZP-7	70 ns	
HM511000AZP-8	80 ns	
HM511000AZP-10	100 ns	
HM511000AZP-12	120 ns	

Part No.	Access Time	Package
HM511000ALP-6	60 ns	300 mil 18-pin Plastic DIP (DP-18C)
HM511000ALP-7	70 ns	
HM511000ALP-8	80 ns	
HM511000ALP-10	100 ns	
HM511000ALP-12	120 ns	
HM511000ALJP-6	60 ns	300 mil 20-pin Plastic SOJ (CP-20D)
HM511000ALJP-7	70 ns	
HM511000ALJP-8	80 ns	
HM511000ALJP-10	100 ns	
HM511000ALJP-12	120 ns	
HM511000ALZP-6	60 ns	400 mil 20-pin Plastic ZIP (ZP-20)
HM511000ALZP-7	70 ns	
HM511000ALZP-8	80 ns	
HM511000ALZP-10	100 ns	
HM511000ALZP-12	120 ns	

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	−2.0	—	0.8	V

Note: All voltages referenced to V_{SS}.

• DC Electrical Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = 0 to +70°C)

Parameter	Symbol	HM511000A /AL-6		HM511000A /AL-7		HM511000 /A-8		HM511000 /A-10		HM511000 /A-12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	70	—	60	—	50	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	1	—	1	—	1	—	1	—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
		—	300	—	300	—	300	—	300	—	300	μA	CMOS Interface L-Version	
Refresh Current	I_{CC3}	—	90	—	80	—	60	—	50	—	45	mA	$\overline{RAS}$ Only Refresh, t_{RC} = Min	2
Battery Back Up Current (Only for L-Version)	I_{CC4}	—	300	—	300	—	300	—	300	—	300	μA	t_{RC} = 125 μs, $\overline{CAS}$ Before $\overline{RAS}$ Cycling	4
Standby Current	I_{CC5}	—	5	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
Refresh Current	I_{CC6}	—	80	—	70	—	60	—	50	—	40	mA	$\overline{CAS}$ Before $\overline{RAS}$ Refresh t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	80	—	70	—	50	—	50	—	40	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, t_{PC} = Min	1, 3

• **DC Electrical Characteristics** (V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = 0 to +70°C) (continued)

Parameter	Symbol	HM511000A /AL-6		HM511000A /AL-7		HM511000 /A-8		HM511000 /A-10		HM511000 /A-12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Input Leakage	I_{LI}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	V_{in} = 0 to +7V	
Output Leakage	I_{LO}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	V_{out} = 0 to +7V, D_{out} = Disable	
Output Levels	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = −5 mA	
	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once while $\overline{CAS}$ = V_{IH}.
4. t_{RAS} = t_{RAS} (min) to 1 μs
Input voltage: All pins: $V_{IH} \geq V_{CC} - 0.2V$ or $V_{IL} \leq 0.2V$.

• **Capacitance** (V_{CC} = 5V ±10%, T_A = 25°C)

Parameter		Symbol	Typ	Max	Unit	Note
Input Capacitance	Address, Data Input	C_{I1}	—	5	pF	1
	Clocks	C_{I2}	—	7	pF	1
Output Capacitance	Data Output	C_O	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{SS} = 0V, V_{CC} = 5V ±10%)

Test Conditions

Input rise and fall times: 5 ns
Input timing reference levels: 0.8V, 2.4V (Including scope and jig)
Output load: 2 TTL Gate + C_L (100 pF)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM511000A /AL-6		HM511000A /AL-7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	120	—	130	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	50	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ms	
Refresh Period (Only for L-Version)	t_{REF}	—	64	—	64	—	64	—	64	—	64	ms	

Read Cycle

Parameter	Symbol	HM511000A /AL-6		HM511000A /AL-7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	55	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	10
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	—	20	—	20	—	20	—	25	—	30	ns	6

Write Cycle

Parameter	Symbol	HM511000A /AL-6		HM511000A /AL-7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	25	—	30	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	20	—	25	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM511000A /AL-6		HM511000A /AL-7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read-Write Cycle Time	t_{RWC}	145	—	155	—	190	—	220	—	255	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	60	—	70	—	80	—	100	—	120	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	20	—	20	—	25	—	25	—	30	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	30	—	35	—	40	—	45	—	55	—	ns	10

Refresh Cycle

Parameter	Symbol	HM511000A /AL-6		HM511000A /AL-7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	0	—	0	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM511000A /AL-6		HM511000A /AL-7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	55	—	65	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	—	50	—	60	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	50	—	60	—	ns	

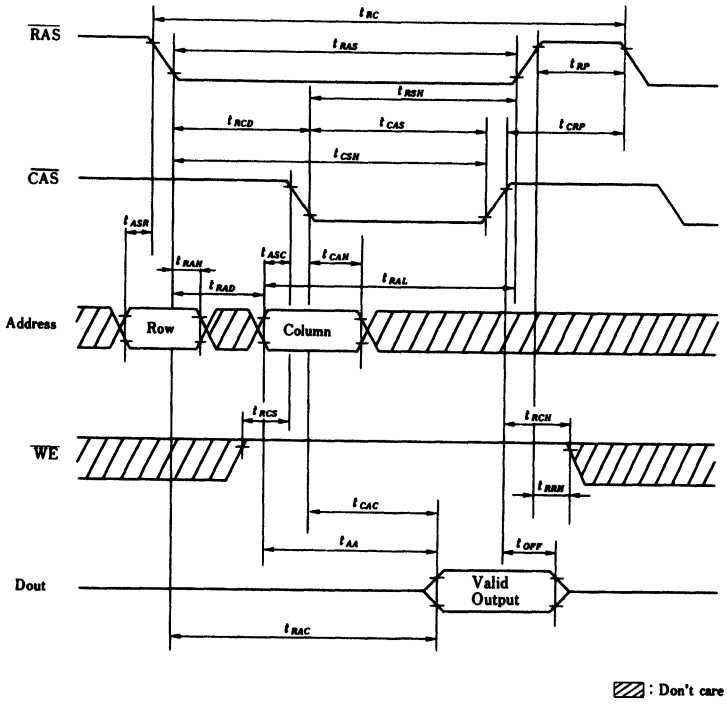
Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM511000A /AL-6		HM511000A /AL-7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	70	—	75	—	85	—	85	—	100	—	ns	

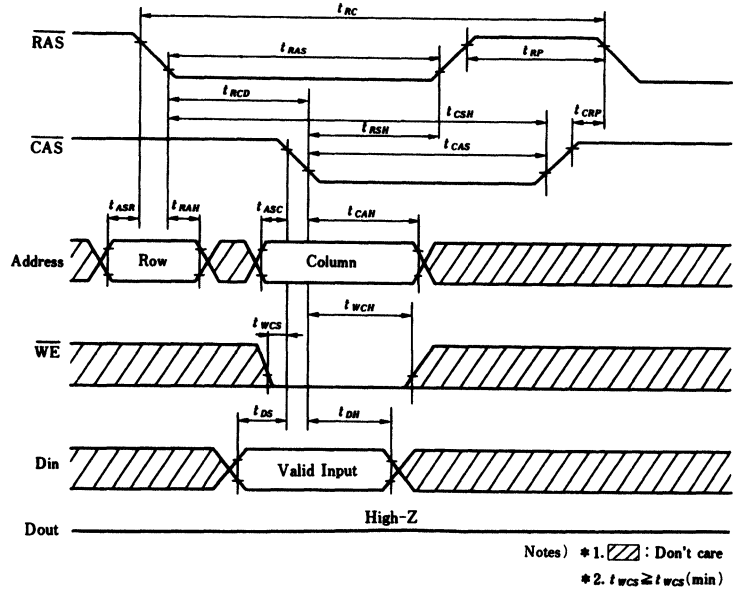
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. An initial pause of 100 μs is required after power-up followed by eight or more initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If internal refresh counter is used, eight or more $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycle.
14. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{ACP}.

■ TIMING WAVEFORMS

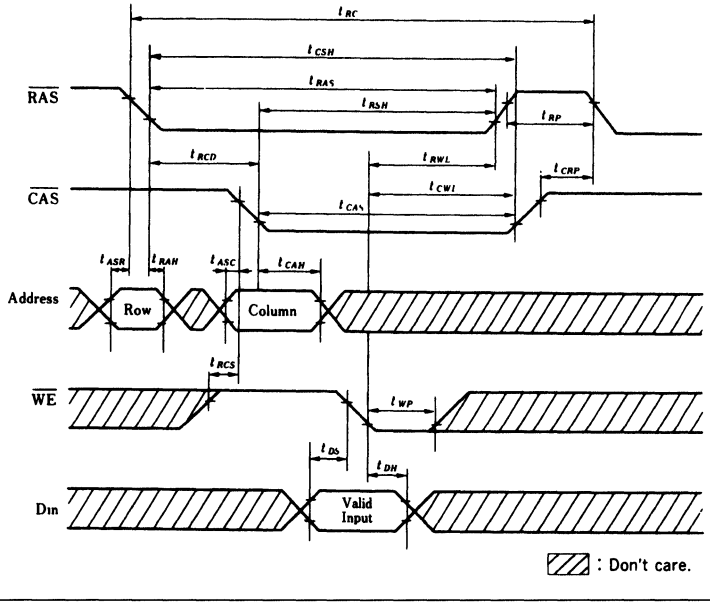
• Read Cycle



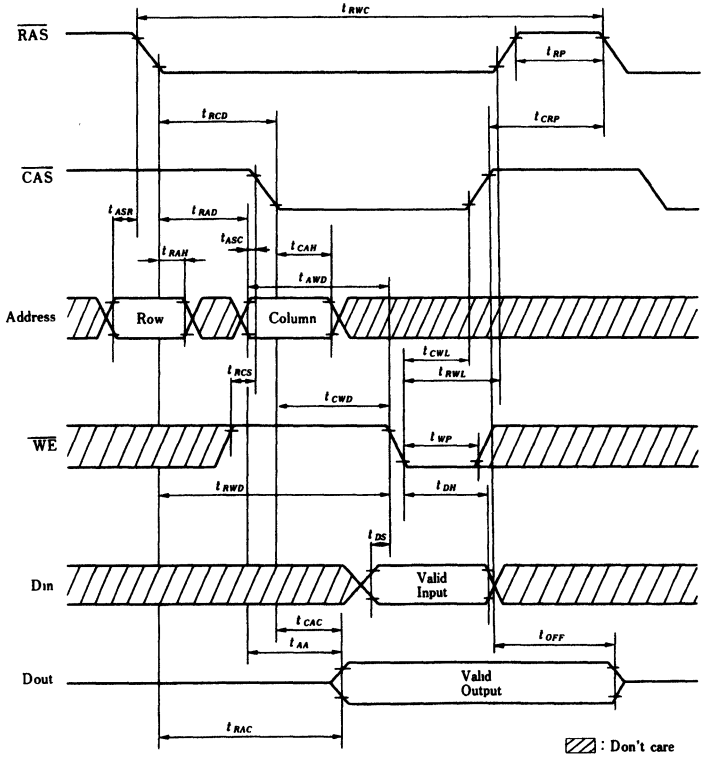
• Early Write Cycle



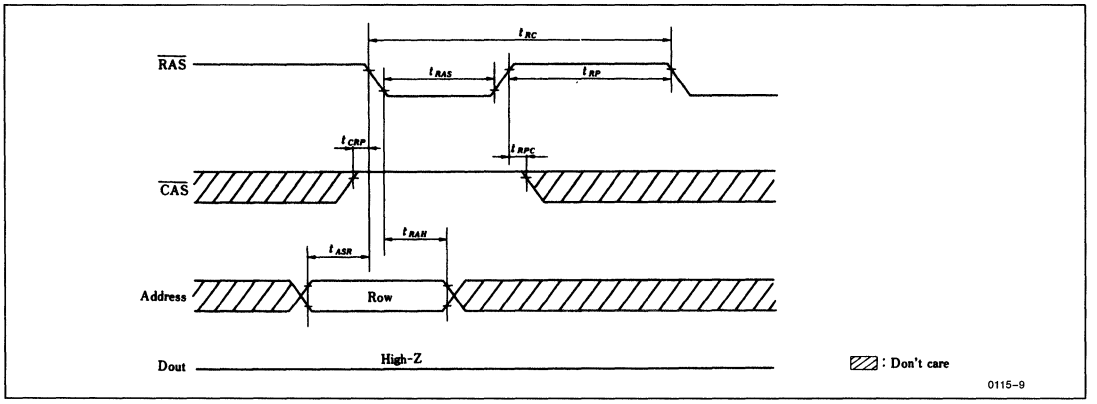
• **Delayed Write Cycle**



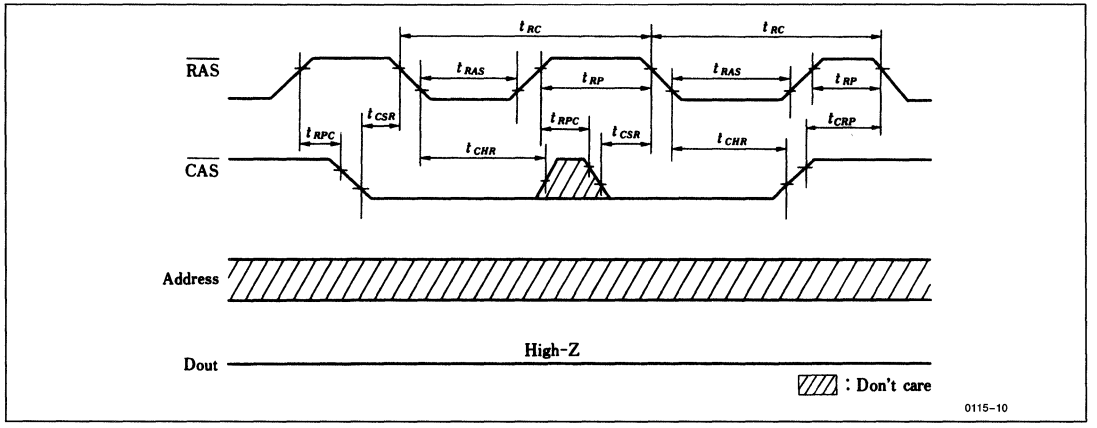
• **Read-Modify-Write Cycle**



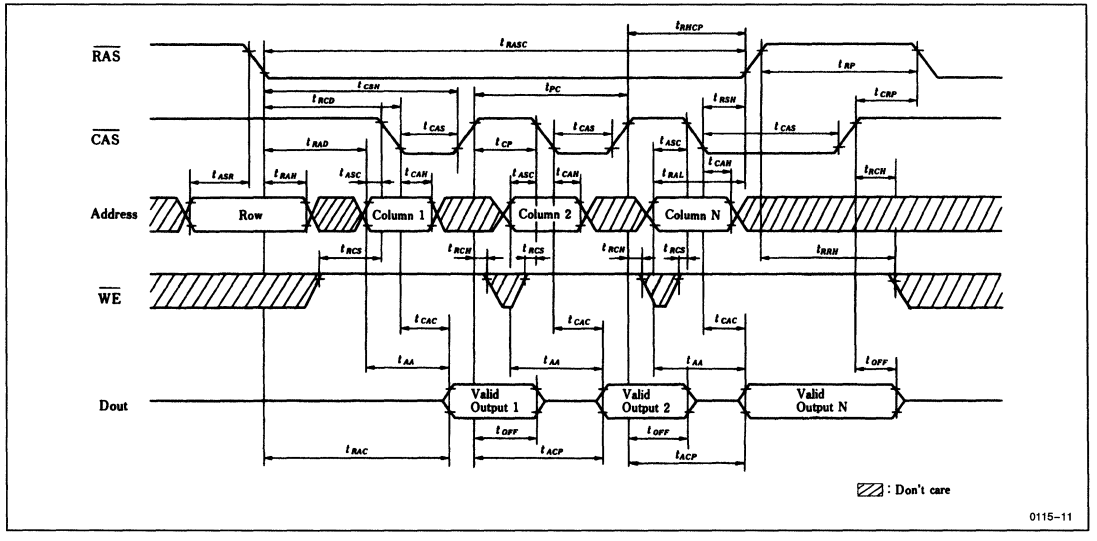
• $\overline{RAS}$ Only Refresh Cycle



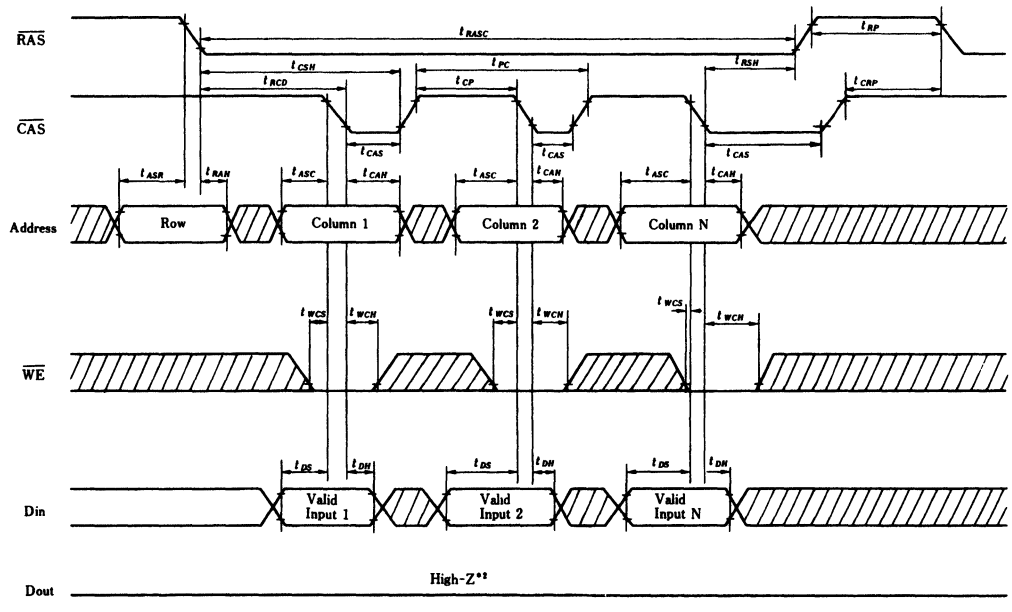
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



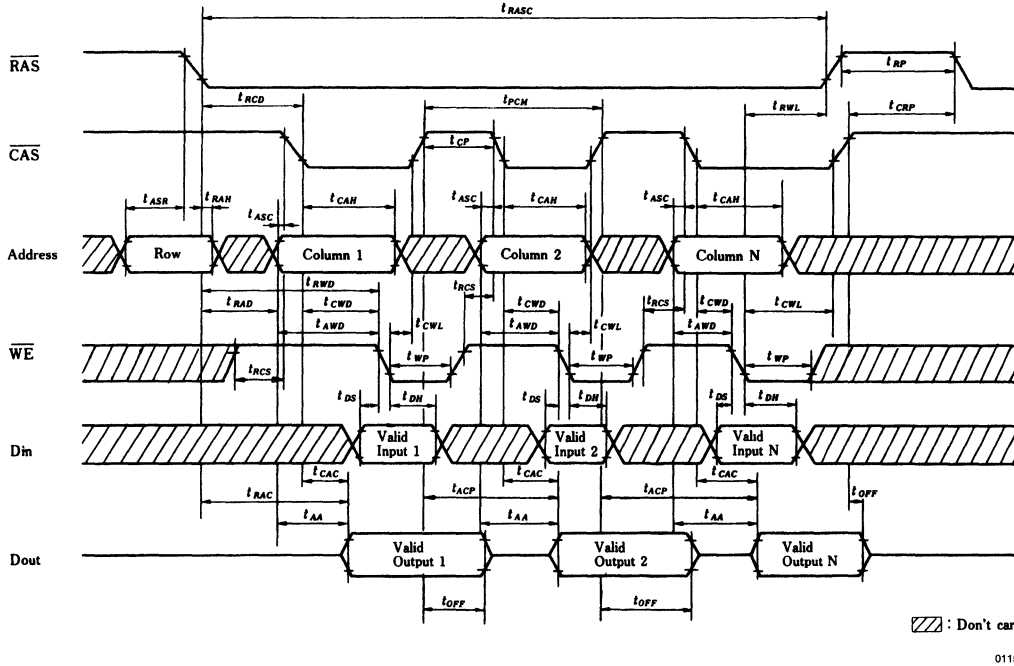
• Fast Page Mode Read Cycle



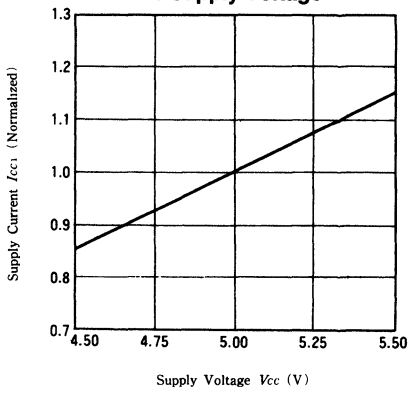
• Fast Page Mode Write Cycle



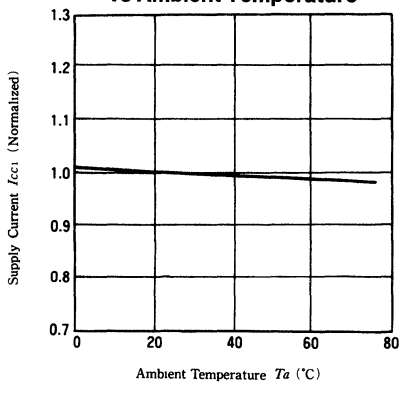
• Fast Page Mode Read Modify Write Cycle



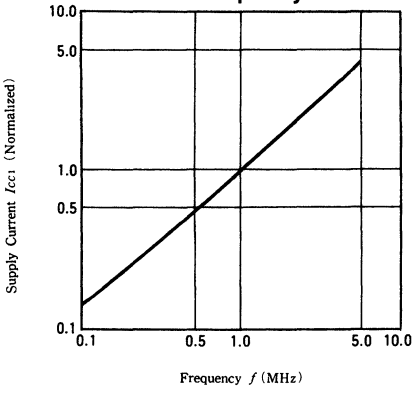
Supply Current (Active) vs Supply Voltage



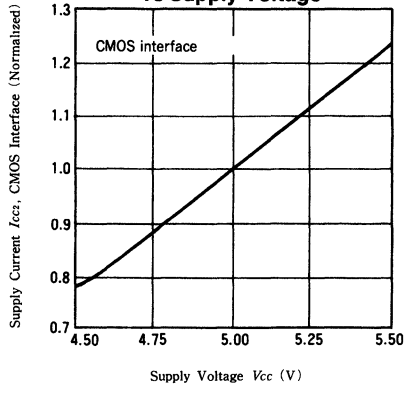
Supply Current (Active) vs Ambient Temperature



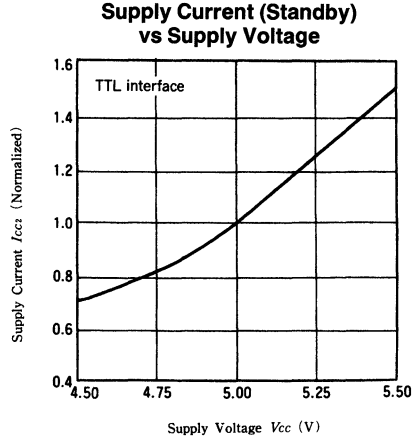
Supply Current (Active) vs Frequency



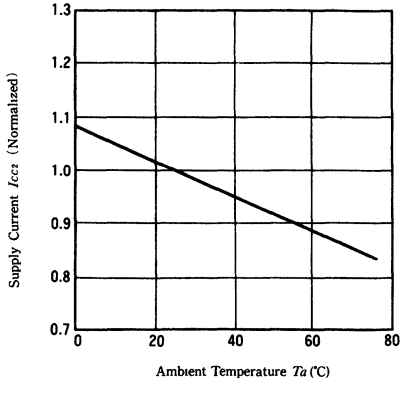
Supply Current (Standby) vs Supply Voltage



Supply Current (Standby) vs Supply Voltage

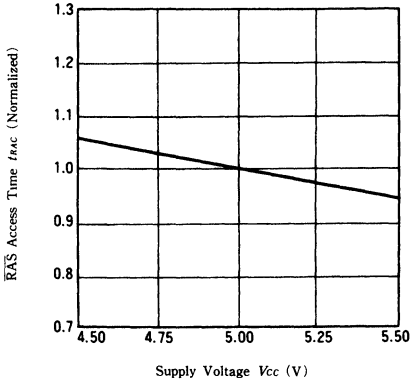


Supply Current (Standby) vs Ambient Temperature

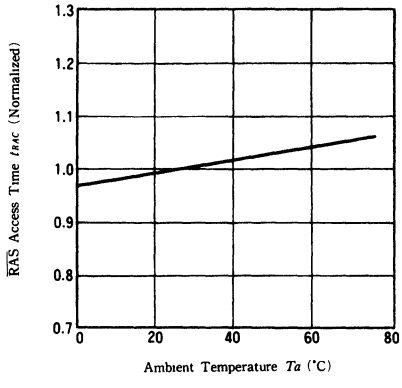


0115-14

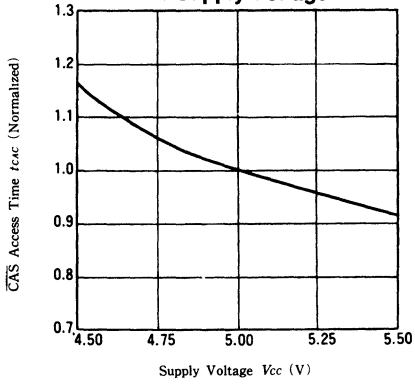
$\overline{RAS}$ Access Time vs Supply Voltage



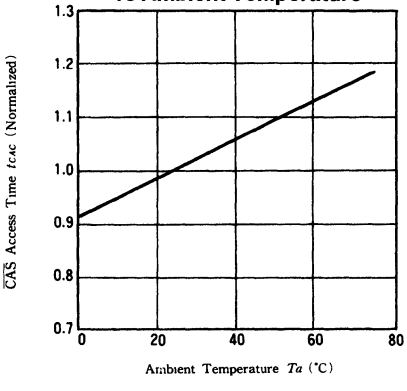
$\overline{RAS}$ Access Time vs Ambient Temperature



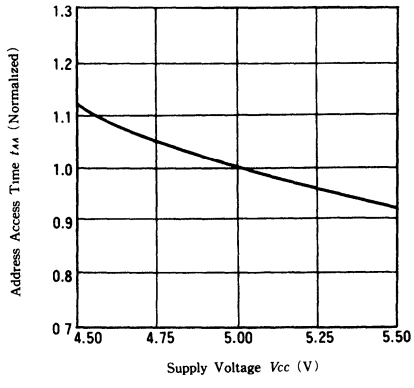
$\overline{CAS}$ Access Time vs Supply Voltage



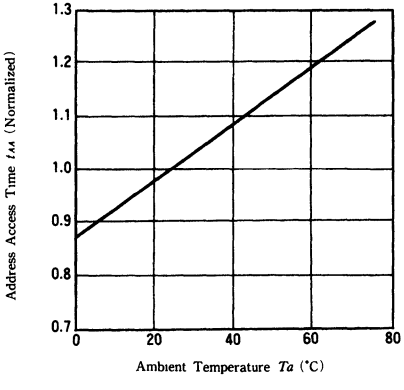
$\overline{CS}$ Access Time vs Ambient Temperature



Address Access Time vs Supply Voltage



Address Access Time vs Ambient Temperature



0115-15

HM511001A Series

1,048,576-Word x 1-Bit CMOS Dynamic RAM

■ DESCRIPTION

The Hitachi HM511001A series is a CMOS dynamic RAM organized 1,048,576-word x 1-bit. HM511001A has realized higher density, higher performance and various functions by employing 1.3 μm CMOS process technology and some new CMOS circuit design technologies.

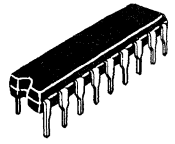
The HM511001A offers Nibble Mode as a high speed access mode.

Multiplexed address input permits the HM511001A to be packaged in standard, 18-pin plastic DIP, 20-pin plastic ZIP and 20-pin plastic SOJ.

■ FEATURES

- High Speed
  - Access Time .....60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low Power
  - Active.....495 mW/440 mW/385 mW/330 mW/275 mW
  - Standby .....11 mW
- Single 5V Supply (±10%)
- Nibble Mode Capability
- 512 Refresh Cycles .....(8 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh

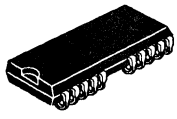
HM511001AP Series



3DDP18C

(DP-18C)

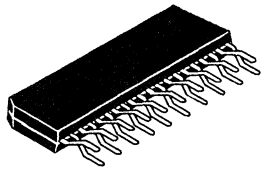
HM511001AJP Series



3DCP20D

(CP-20D)

HM511001AZP Series

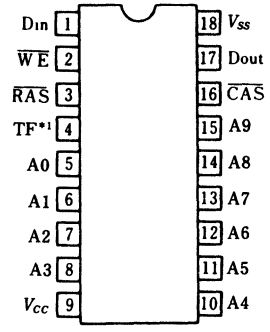


3DZP20

(ZP-20)

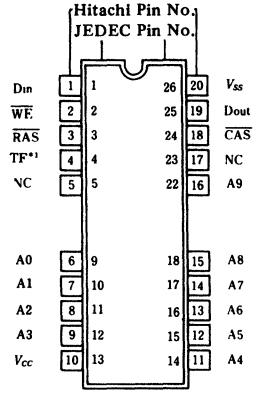
■ PIN OUT

HM511001AP Series



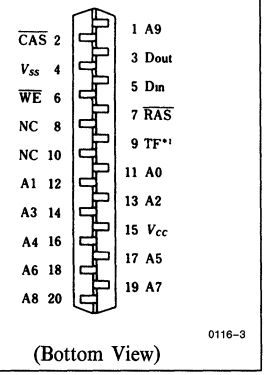
(Top View)

HM511001AJP Series



(Top View)

HM511001AZP Series



(Bottom View)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_8	Refresh Address Input
A_9	Nibble Address Input
D_{in}	Data Input
D_{out}	Data Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Row Address Input
$\overline{WE}$	Read/Write Input
TF*1	Test Function
V_{CC}	Power (+5V)
V_{SS}	Ground

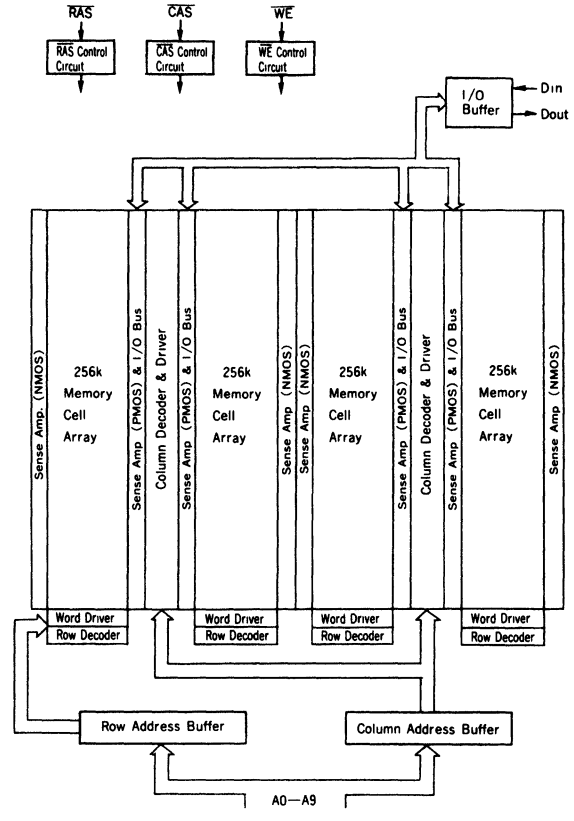
Note: *1. TF pin can be connected with any line or unconnected provided the voltage level of TF pin must be kept lower than V_{CC} + 0.5V.

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM511001AP-6	60 ns	300 mil 18-pin Plastic DIP (DP-18C)
HM511001AP-7	70 ns	
HM511001AP-8	80 ns	
HM511001AP-10	100 ns	
HM511001AP-12	120 ns	
HM511001AJP-6	60 ns	300 mil 20-pin Plastic SOJ (CP-20D)
HM511001AJP-7	70 ns	
HM511001AJP-8	80 ns	
HM511001AJP-10	100 ns	
HM511001AJP-12	120 ns	

Part No.	Access Time	Package
HM511001AZP-6	60 ns	400 mil 20-pin Plastic DIP (ZP-20)
HM511001AZP-7	70 ns	
HM511001AZP-8	80 ns	
HM511001AZP-10	100 ns	
HM511001AZP-12	120 ns	

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	−2.0	—	0.8	V

Note: 1. All voltages referenced to V_{SS}.

• DC Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = 0 to +70°C)

Parameter	Symbol	HM511001A										Unit	Test Condition	Note
		-6		-7		-8		-10		-12				
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	70	—	60	—	50	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	—	2	—	2	mA	$\overline{RAS}$ $\overline{CAS}$ = V_{IH} TTL Interface, D_{out} = High-Z	
		—	1	—	1	—	1	—	1	—	1		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V CMOS Interface, D_{out} = High-Z	
Refresh Current	I_{CC3}	—	90	—	80	—	70	—	60	—	50	mA	$\overline{RAS}$ Only Refresh, t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
Refresh Current	I_{CC6}	—	80	—	70	—	60	—	50	—	40	mA	$\overline{CAS}$ Before RAS Refresh, t_{RC} = Min	
Nibble Mode Current	I_{CC8}	—	70	—	70	—	50	—	50	—	40	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, t_{NC} = Min	1, 3
Input Leakage	I_{LI}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	V_{IN} = 0 to +7V	
Output Leakage	I_{LO}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	V_{in} = 0 to +7V, D_{out} = Disabled	
Output Levels	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = −5 mA	
	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• Capacitance (V_{CC} = 5V ±10%, T_A = 25°C)

Parameter		Symbol	Typ	Max	Unit	Note
Input Capacitance	Address, Data Input	C_{I1}	—	5	pF	1
	Clocks	C_{I2}	—	7	pF	1
Output Capacitance	Data Output	C_O	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 10]

Test Conditions

Input Rise and Fall Times .....5 ns
Input Timing Reference Levels 0.8V, 2.4V
Output Load .....2 TTL Gate + C_L (100 pF) (Including Scope and Jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM511001A										Unit	Note
		-6		-7		-8		-10		-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	120	—	130	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	50	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	75	25	90	ns	7
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	55	20	65	ns	11
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	6
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ms	

Read Cycle

Parameter	Symbol	HM511001A										Unit	Note
		-6		-7		-8		-10		-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	55	ns	3, 4
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	55	—	ns	
Output Buffer Turn-off Delay	t_{OFF}	—	20	—	20	—	20	—	25	—	30	ns	5

Write Cycle

Parameter	Symbol	HM511001A										Unit	Note
		-6		-7		-8		-10		-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	25	—	30	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	20	—	25	—	ns	9

Read-Modify-Write Cycle

Parameter	Symbol	HM511001A										Unit	Note
		-6		-7		-8		-10		-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read-Write Cycle Time	t_{RWC}	145	—	155	—	190	—	210	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	60	—	70	—	80	—	90	—	110	—	ns	8
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	20	—	20	—	25	—	25	—	30	—	ns	8
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	30	—	35	—	40	—	45	—	55	—	ns	8

Refresh Cycle

Parameter	Symbol	HM511001A										Unit	Note
		-6		-7		-8		-10		-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	ns	

Nibble Mode Cycle

Parameter	Symbol	HM511001A										Unit	Note
		-6		-7		-8		-10		-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Nibble Mode Access Time	t_{NAC}	—	20	—	20	—	25	—	25	—	30	ns	
Nibble Mode Cycle Time	t_{NC}	40	—	40	—	45	—	45	—	50	—	ns	
Nibble Mode $\overline{CAS}$ Precharge Time	t_{NCP}	10	—	10	—	10	—	10	—	10	—	ns	
Nibble Mode $\overline{CAS}$ Pulse Width	t_{NCA}	20	—	20	—	25	—	25	—	30	—	ns	
Nibble Mode $\overline{RAS}$ Hold Time	t_{NRSH}	20	—	20	—	25	—	25	—	30	—	ns	

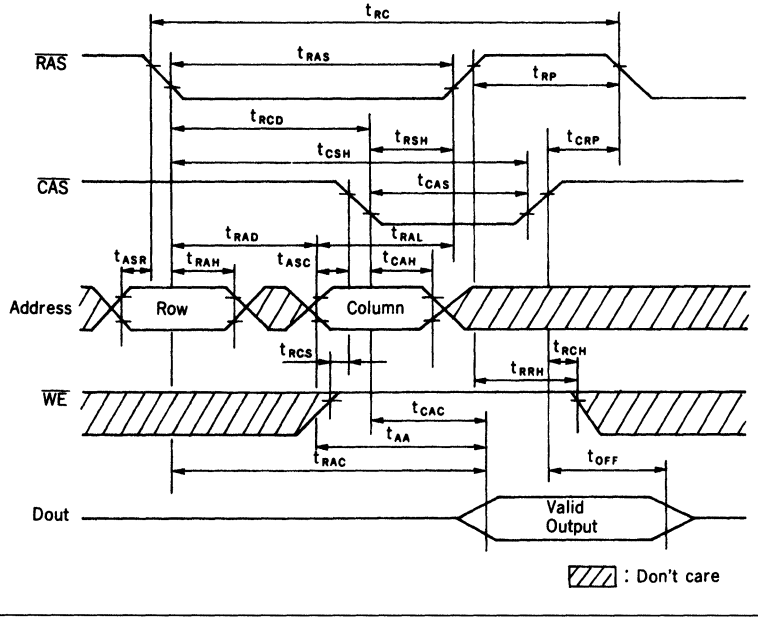
Nibble Mode Read-Modify-Write Cycle

Parameter	Symbol	HM511001A										Unit	Note
		-6		-7		-8		-10		-12			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Nibble Mode Read-Modify-Write Cycle Time	t_{NRWC}	65	—	65	—	65	—	65	—	75	—	ns	
Nibble Mode Write Command $\overline{CAS}$ Lead Time	t_{NCWL}	20	—	20	—	20	—	20	—	25	—	ns	
Nibble Mode $\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{NCWD}	20	—	20	—	20	—	20	—	25	—	ns	

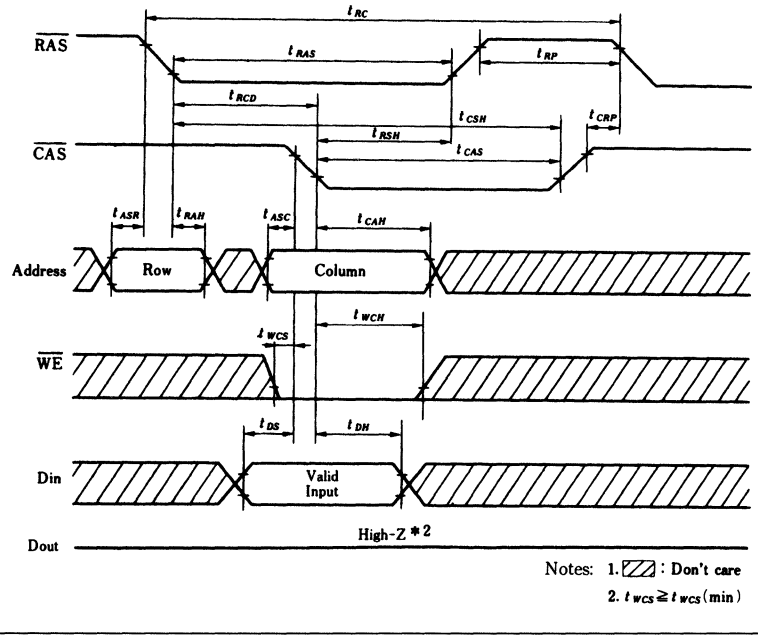
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100 μs is required after power-up followed by eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If internal refresh counter is used, eight or more $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
11. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

■ TIMING WAVEFORMS

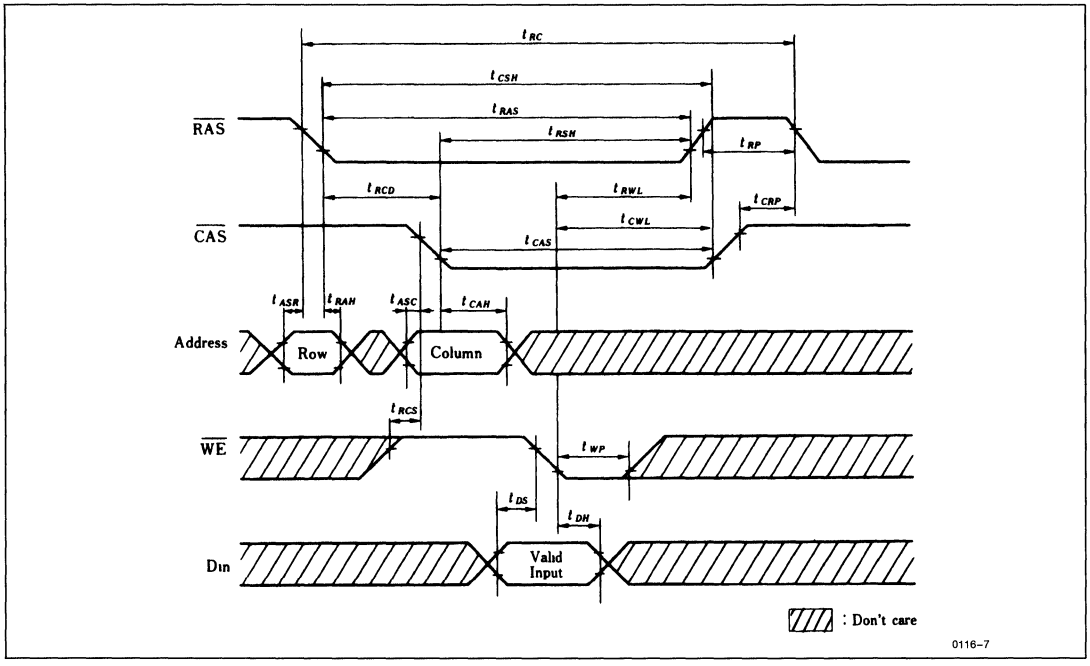
• Read Cycle



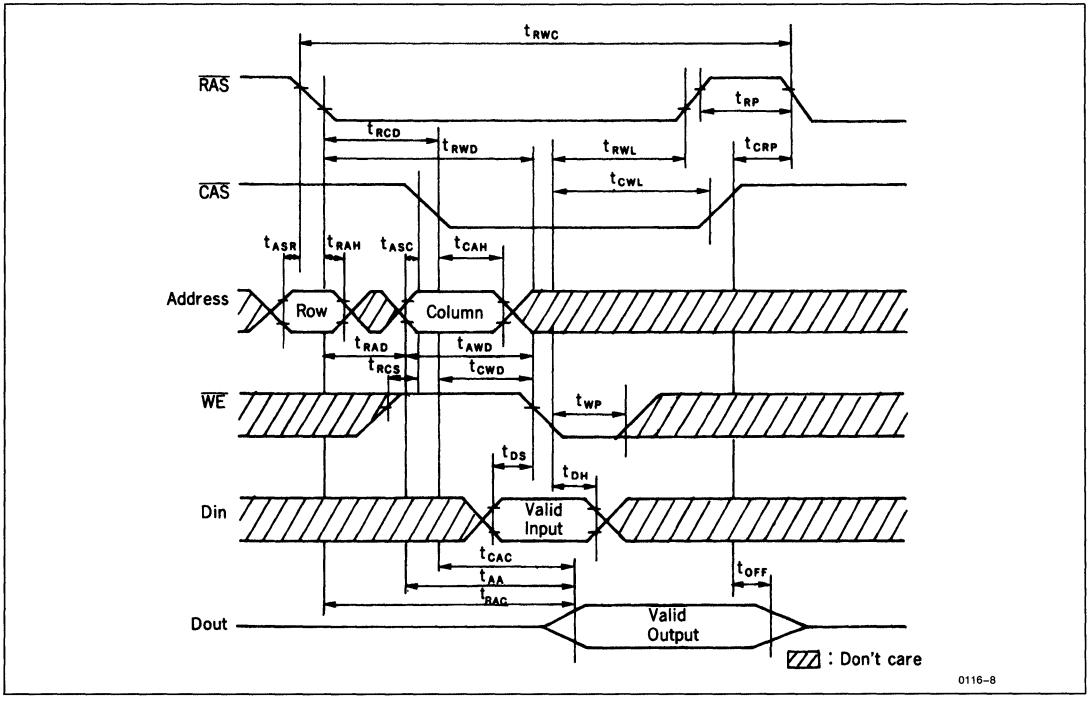
• Early Write Cycle



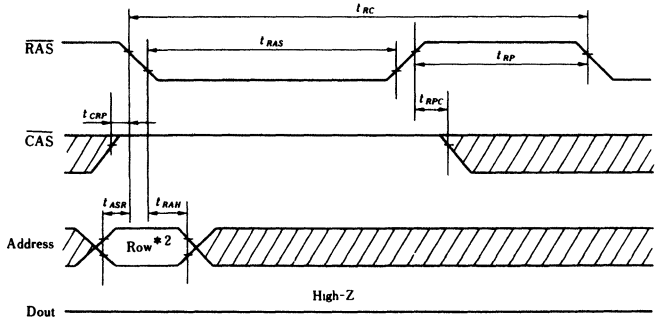
• **Delayed Write Cycle**



• **Read-Modify-Write Cycle**



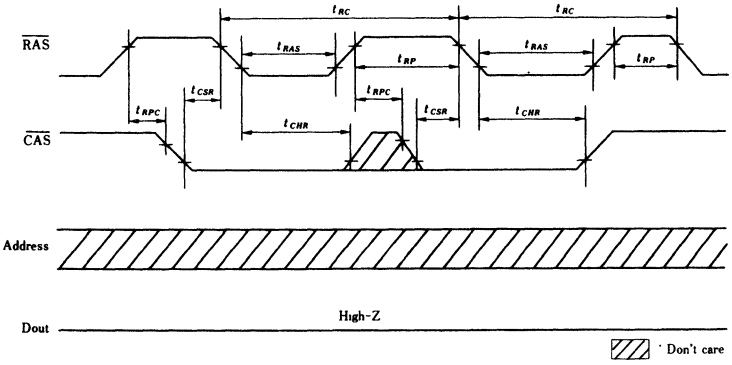
• $\overline{RAS}$ Only Refresh Cycle



Notes 1. ▨: Don't care
2. Refresh address A0-A8(AX0-AX8)

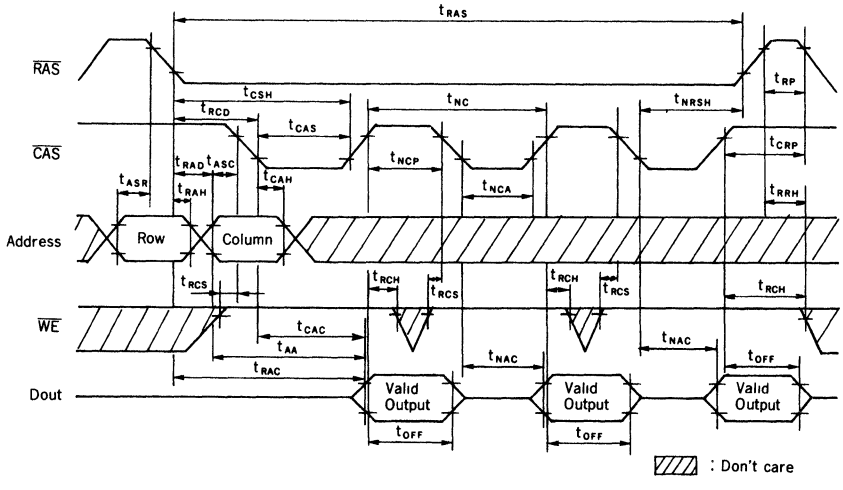
0116-9

• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



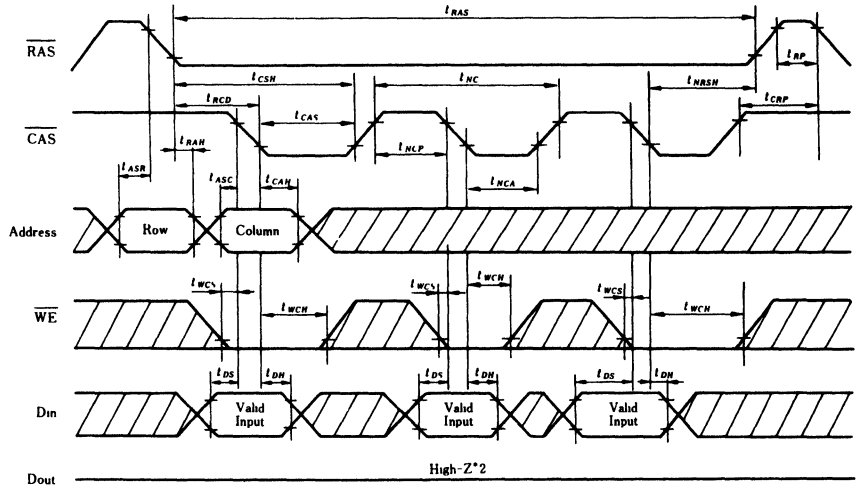
0116-10

• Nibble Mode Read Cycle

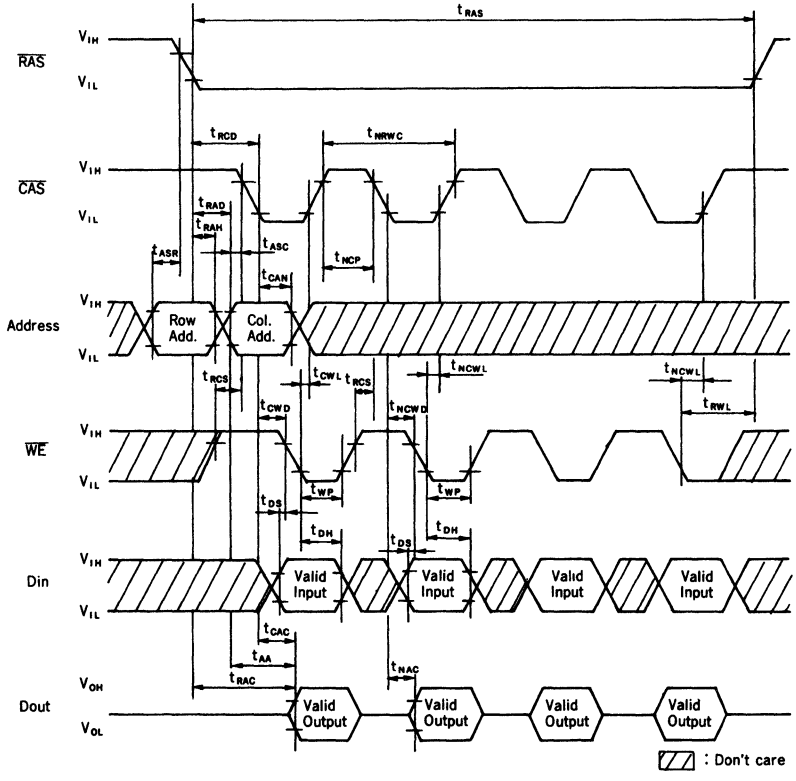


0116-11

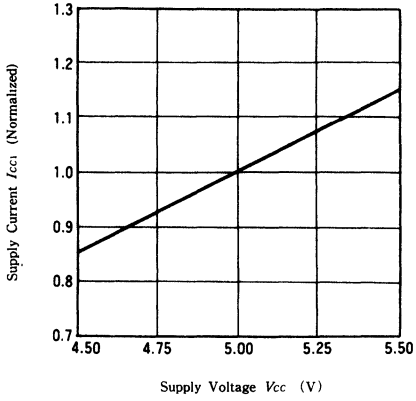
• Nibble Mode Write Cycle



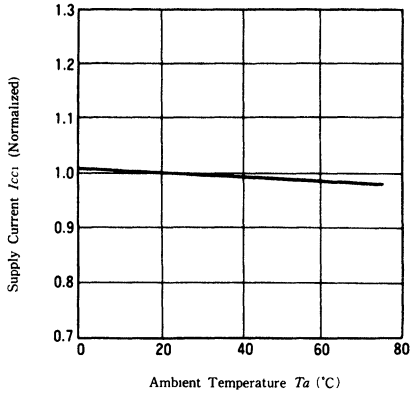
• Nibble Mode Read-Modify-Write Cycle



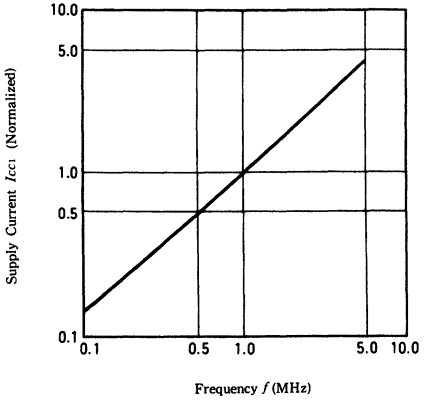
Supply Current (Active) vs. Supply Voltage



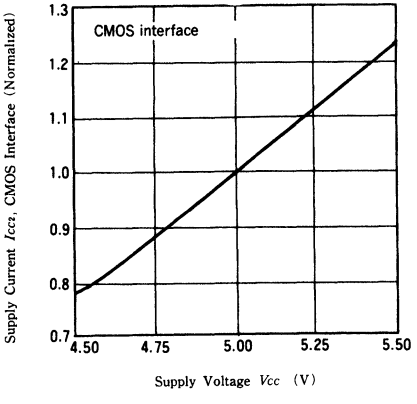
Supply Current (Active) vs. Ambient Temperature



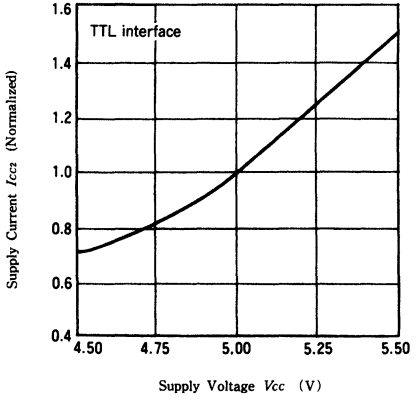
Supply Current (Active) vs. Frequency



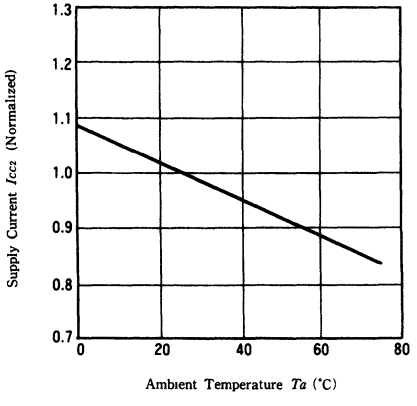
Supply Current (Standby) vs. Supply Voltage



Supply Current (Standby) vs. Supply Voltage

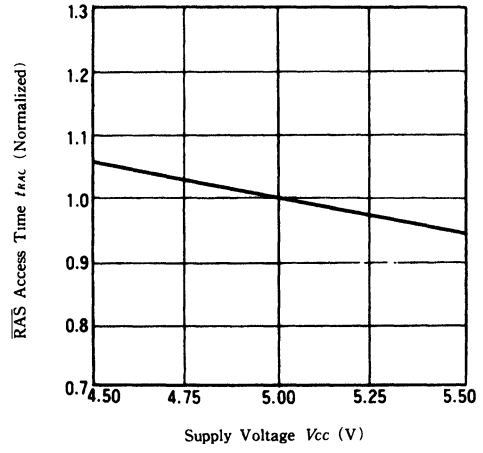


Supply Current (Standby) vs. Ambient Temperature

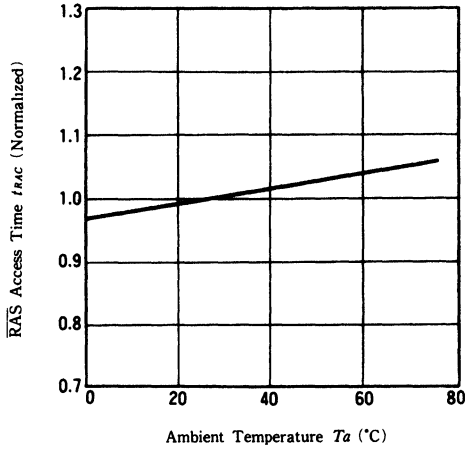


0116-14

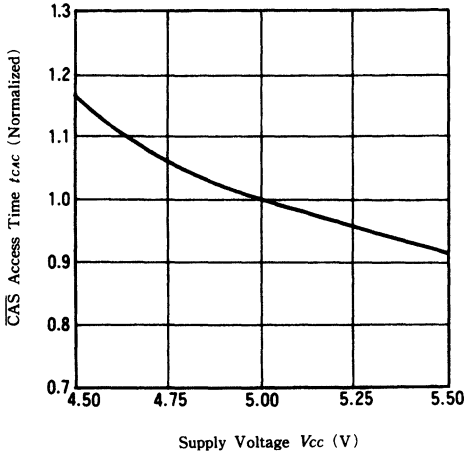
$\overline{RAS}$ Access Time vs. Supply Voltage



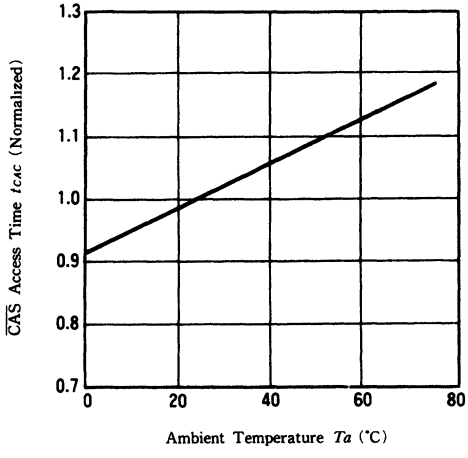
$\overline{RAS}$ Access Time vs. Ambient Temperature



$\overline{CAS}$ Access Time vs. Supply Voltage



$\overline{CAS}$ Access Time vs. Ambient Temperature



0116-15

HM511002A Series

1,048,576-word x 1-bit CMOS Dynamic RAM

■ DESCRIPTION

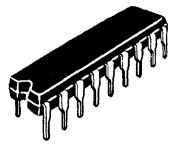
The Hitachi HM511002A Series is a CMOS dynamic RAM organized 1,048,576-word x 1-bit. HM511002A has realized higher density, higher performance and various functions by employing 1.3 μm CMOS process technology and some new CMOS circuit design technologies. The HM511002A offers Static Column Mode as a high speed access mode.

Multiplexed address input permits the HM511002A to be packaged in standard 18-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

■ FEATURES

- High Speed
  - Access Time .....60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low Power
  - Standby .....11 mW
  - Active.....495 mW/440 mW/385 mW/330 mW/275 mW
- Single 5V Supply (±10%)
- Static Column Mode Capability
- 512 Refresh Cycles .....(8 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh

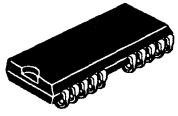
HM511002AP Series



3DDP18C

(DP-18C)

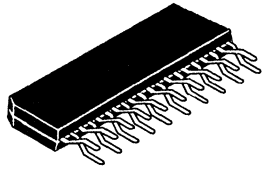
HM511002AJP Series



3DCP20D

(CP-20D)

HM511002AZP Series

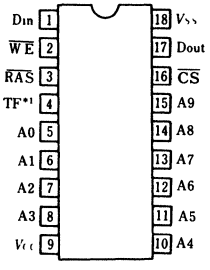


3DZP20

(ZP-20)

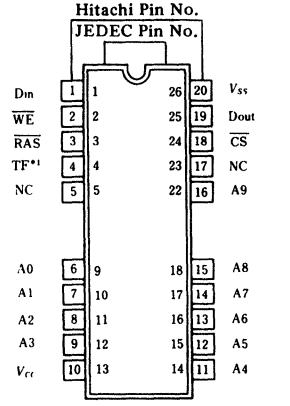
■ PIN OUT

HM511002AP Series



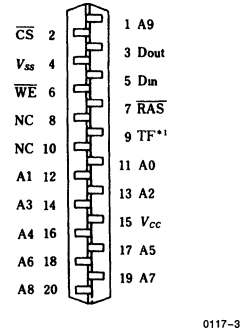
(Top View)

HM511002AJP Sereis



(Top View)

HM511002AZP Series



(Bottom View)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_8	Refresh Address Input
D_{in}	Data Input
D_{out}	Data Output
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
TF*1	Test Function

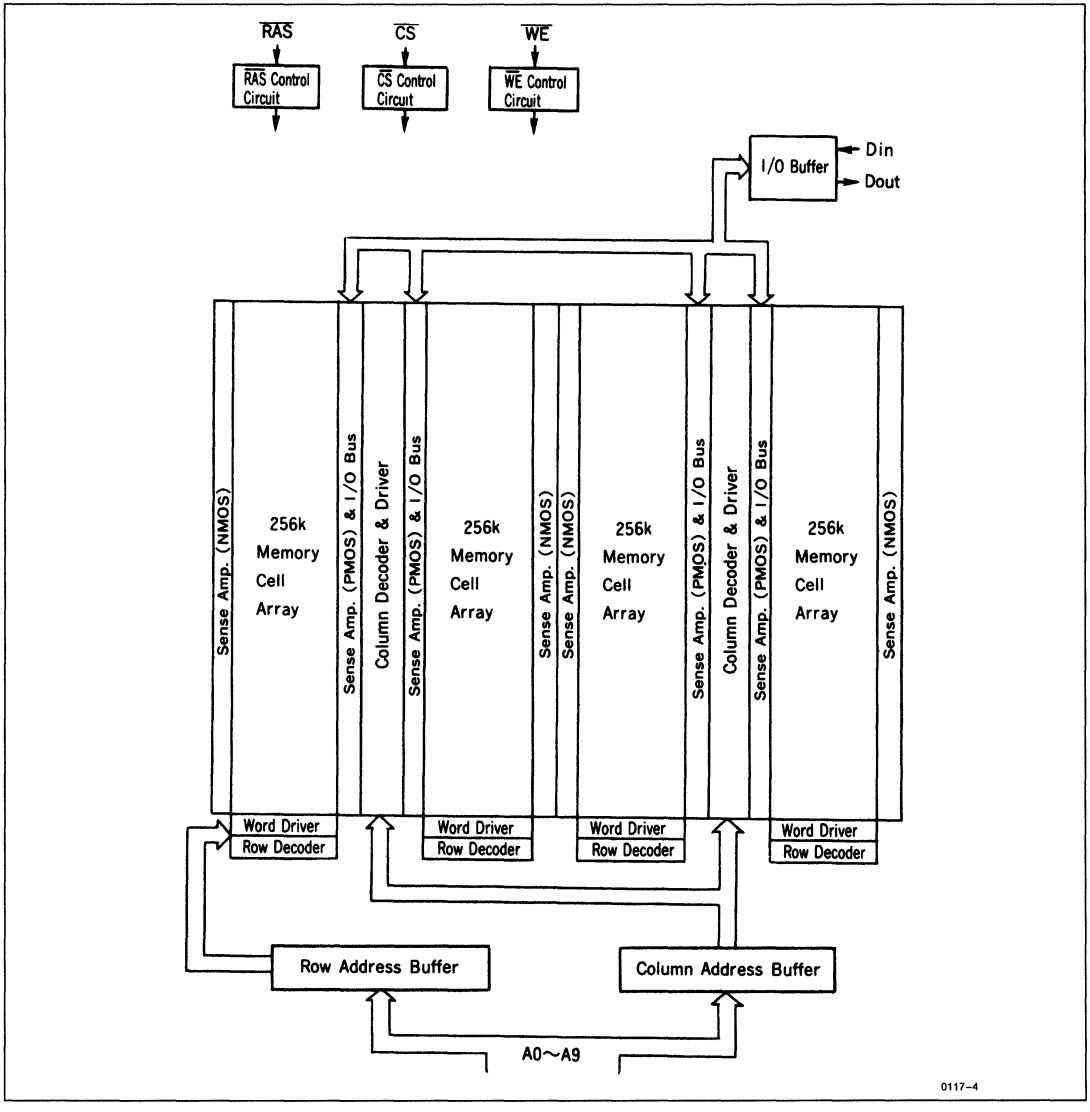
Note: *1. TF pin can be connected with any line or unconnected provided the voltage level of TF pin must be kept lower than V_{CC} + 0.5V.

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM511002AP-6	60 ns	300 mil 18-pin Plastic DIP (DP-18C)
HM511002AP-7	70 ns	
HM511002AP-8	80 ns	
HM511002AP-10	100 ns	
HM511002AP-12	120 ns	
HM511002AJP-6	60 ns	300 mil 20-pin Plastic SOJ (CP-20D)
HM511002AJP-7	70 ns	
HM511002AJP-8	80 ns	
HM511002AJP-10	100 ns	
HM511002AJP-12	120 ns	

Part No.	Access Time	Package
HM511002AZP-6	60 ns	400 mil 20-pin Plastic ZIP (ZP-20)
HM511002AZP-7	70 ns	
HM511002AZP-8	80 ns	
HM511002AZP-10	100 ns	
HM511002AZP-12	120 ns	

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.4	—	6.5	V	
Input Low Voltage	V_{IL}	−2.0	—	0.8	V	

Note: 1. All voltages referenced to V_{SS}.

• DC Electrical Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = 0 to +70°C)

Parameter	Symbol	HM511002A -6		HM511002A -7		HM511002A -8		HM511002A -10		HM511002A -12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	70	—	60	—	50	mA	$\overline{RAS}$, $\overline{CS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CS}$ = V_{IH} D_{out} = High-Z	
		—	1	—	1	—	1	—	1	—	1		CMOS Interface $\overline{RAS}$, $\overline{CS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
Refresh Current	I_{CC3}	—	90	—	80	—	60	—	50	—	45	mA	$\overline{RAS}$ Only Refresh t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IL}, D_{out} = Enable	1
Refresh Current	I_{CC6}	—	80	—	70	—	60	—	50	—	40	mA	$\overline{CS}$ Before $\overline{RAS}$ Refresh, t_{RC} = Min	
Static Column Mode Current	I_{CC9}	—	80	—	70	—	60	—	50	—	40	mA	t_{SC} = Min	3
Input Leakage	I_{LI}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	V_{IN} = 0 to +7V	
Output Leakage	I_{LO}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	V_{out} = 0 to +7V, D_{out} = Disable	
Output Levels	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = −5 mA	
	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CS}$ = V_{IH}.

• Capacitance (V_{CC} = 5V ±10% T_A = 25°C)

Parameter		Symbol	Typ	Max	Unit	Note
Input Capacitance	Address, Data Input	C_{I1}	—	5	pF	1
	Clocks	C_{I2}	—	7	pF	1
Output Capacitance	Data Output	C_O	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CS}$ = V_{IH} to disable D_{out}.

• AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 17]

Test Conditions

Input Rise and Fall Times	5 ns
Input Timing Reference Levels	0.8V, 2.4V
Output Load	2 TTL Gates + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HM511002A-6		HM511002A-7		HM511002A-8		HM511002A-10		HM511002A-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	120	—	130	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	50	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CS}$ Pulse Width	t_{SP}	20	10000	20	10000	25	10000	30	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASW}	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{AHW}	15	—	15	—	20	—	25	—	25	—	ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	70	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	50	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSL}	20	—	20	—	25	—	30	—	30	—	ns	
$\overline{CS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CS}$ to $\overline{RAS}$ Pre-charge Time	t_{SRS}	10	—	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise to Fall)	t_r	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ms	

Read Cycle

Parameter	Symbol	HM511002A-6		HM511002A-7		HM511002A-8		HM511002A-10		HM511002A-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access Time from $\overline{CS}$	t_{ACS}	—	20	—	20	—	25	—	30	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	50	—	55	ns	3, 5, 14
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	50	—	55	—	ns	

Read Cycle (continued)

Parameter	Symbol	HM511002A-6		HM511002A-7		HM511002A-8		HM511002A-10		HM511002A-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to Column Address Hold Time	t_{AHR}	15	—	15	—	15	—	15	—	15	—	ns	16
Output Hold Time from Address	t_{AOH}	5	—	5	—	5	—	5	—	5	—	ns	
Output Buffer Turn-off Time	t_{OFF}	—	20	—	20	—	20	—	25	—	30	ns	6
Column Address Hold Time to $\overline{RAS}$ on Read	t_{AR}	60	—	70	—	80	—	100	—	120	—	ns	

Write Cycle

Parameter	Symbol	HM511002A-6		HM511002A-7		HM511002A-8		HM511002A-10		HM511002A-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	25	—	25	—	ns	
Write Command Hold Time to $\overline{RS}$	t_{WCR}	55	—	65	—	75	—	95	—	115	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	25	—	30	—	ns	
Write Command to $\overline{CS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	25	—	30	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	25	—	25	—	ns	11
Data-in Hold Time to $\overline{RAS}$	t_{DHR}	55	—	65	—	75	—	95	—	115	—	ns	
Column Address Hold Time to $\overline{RAS}$ or Write	t_{AWR}	55	—	65	—	75	—	95	—	115	—	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM511002A-6		HM511002A-7		HM511002A-8		HM511002A-10		HM511002A-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read-Write Cycle Time	t_{RWC}	145	—	155	—	190	—	220	—	255	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	60	—	70	—	80	—	100	—	120	—	ns	10
$\overline{CS}$ to $\overline{WE}$ Delay Time	t_{CWD}	20	—	20	—	25	—	30	—	30	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	30	—	35	—	40	—	50	—	55	—	ns	10
Output Hold Time from $\overline{WE}$	t_{WOH}	0	—	0	—	0	—	0	—	0	—	ns	

Refresh Cycle

Parameter	Symbol	HM511002A-6		HM511002A-7		HM511002A-8		HM511002A-10		HM511002A-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CS}$ Setup Time ($\overline{CS}$ Before $\overline{RAS}$ Refresh)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CS}$ Hold Time ($\overline{CS}$ Before $\overline{RAS}$ Refresh)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CS}$ Hold Time	t_{ZRH}	10	—	10	—	10	—	10	—	10	—	ns	

SC Mode Cycle

Parameter	Symbol	HM511002A-6		HM511002A-7		HM511002A-8		HM511002A-10		HM511002A-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{SC}$ Mode Cycle Time	t_{SC}	35	—	40	—	45	—	55	—	60	—	ns	
$\overline{SC}$ Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	ns	
$\overline{RAS}$ to Second $\overline{WE}$ Delay Time	t_{RSWD}	70	—	80	—	90	—	110	—	135	—	ns	
$\overline{SC}$ Mode $\overline{CS}$ Precharge Time	t_{SI}	10	—	10	—	10	—	10	—	15	—	ns	
Write Invalid Time	t_{WI}	10	—	10	—	10	—	10	—	15	—	ns	

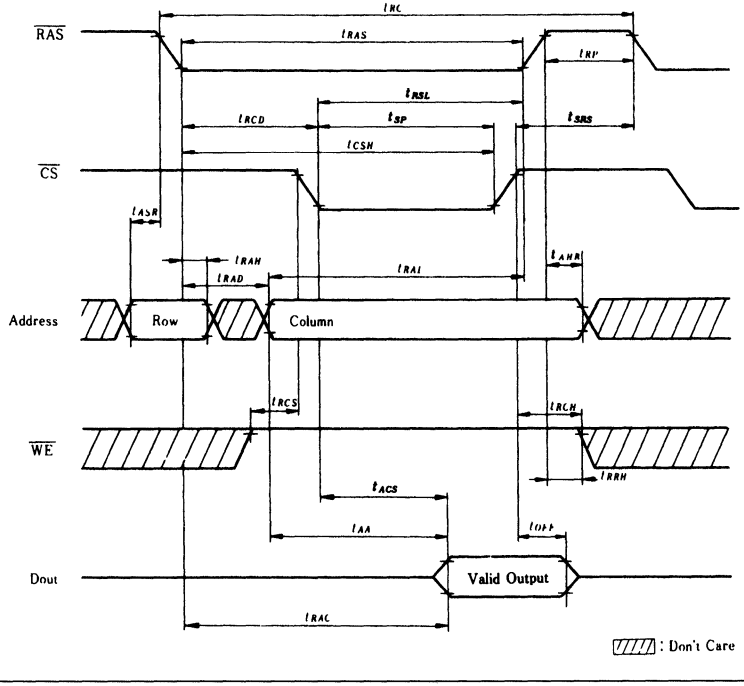
SC Mode Read-Modify-Write and Mixed Cycle

Parameter	Symbol	HM511002A-6		HM511002A-7		HM511002A-8		HM511002A-10		HM511002A-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{SC}$ Mode Cycle Time on Read-Write	t_{SRW}	70	—	80	—	90	—	105	—	120	—	ns	12
Access Time from Previous $\overline{WE}$	t_{ALW}	—	65	—	75	—	85	—	100	—	115	ns	3, 13
Previous $\overline{WE}$ to Column Address Delay Time	t_{LWAD}	20	35	20	40	25	45	25	50	30	60	ns	15
Column Address Hold Time to Previous $\overline{WE}$	t_{AHLW}	65	—	75	—	85	—	100	—	115	—	ns	
Output Enable Time from $\overline{WE}$	t_{OW}	—	25	—	25	—	30	—	30	—	35	ns	

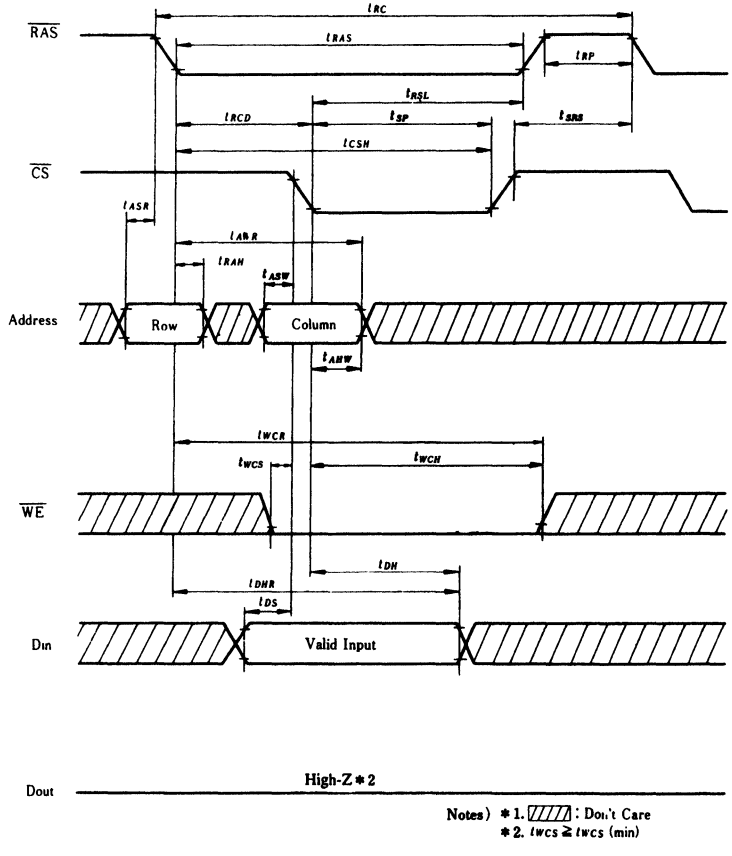
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{ACS}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. t_{SRW} (min) = t_{AWD} (min) + t_{LWAD} (max) + t_T.
13. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} exceeds the value shown.
14. Assumes that $t_{LWAD} \geq t_{LWAD}$ (max).
15. Operation with the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met, t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AHR} is defined as the time at which the column address hold.
17. An initial pause of 100 μs is required after power-up followed by eight or more initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If internal refresh counter is used, eight or more $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.

■ TIMING WAVEFORMS

• Read Cycle



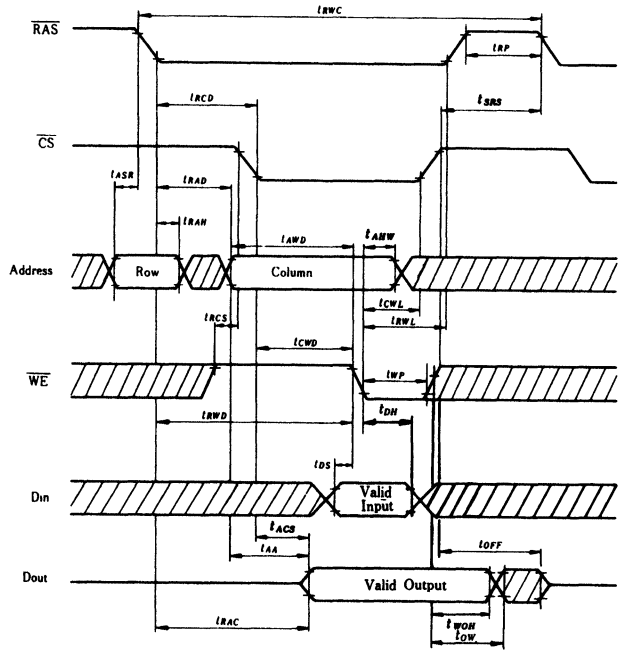
• **Early Write Cycle**



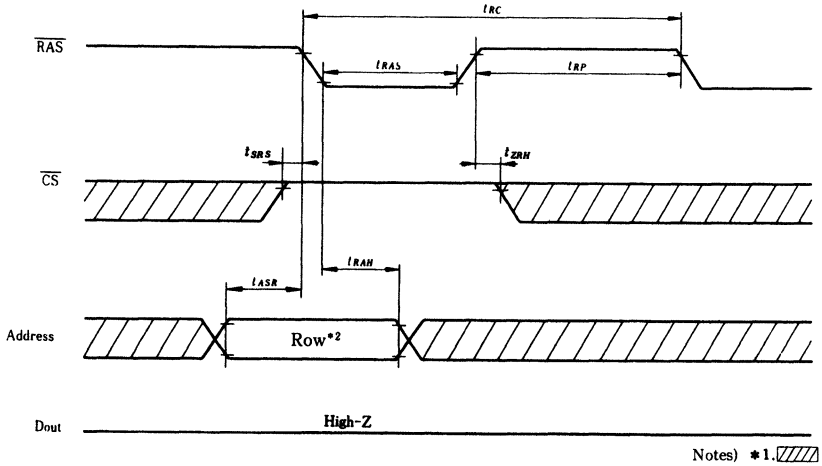
Notes) *1. ▨: Don't Care
*2. $t_{WCS} \geq t_{WCS}$ (min)

0117-6

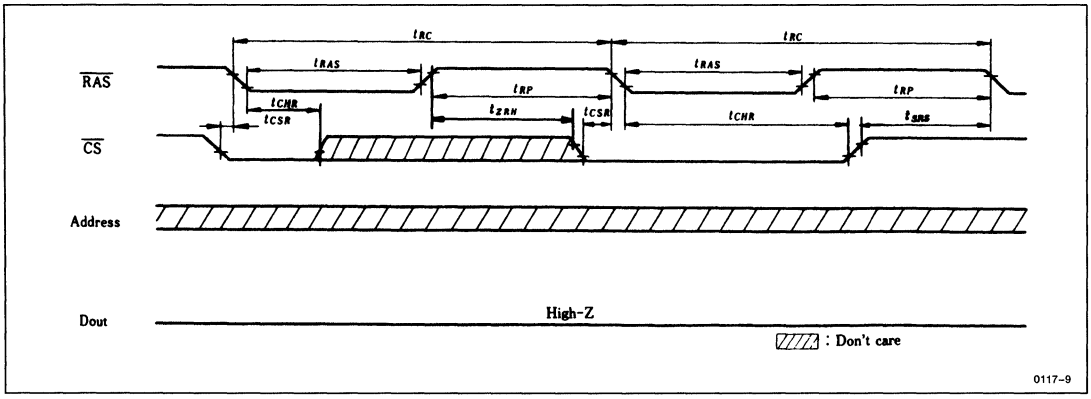
• Read-Modify-Write Cycle



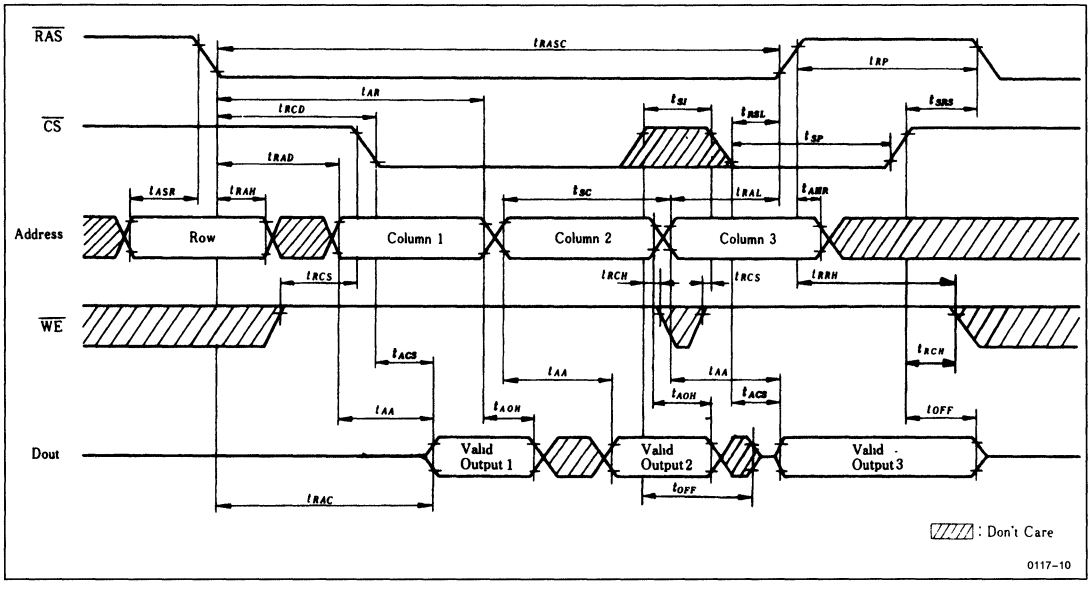
• $\overline{RAS}$ Only Refresh Cycle



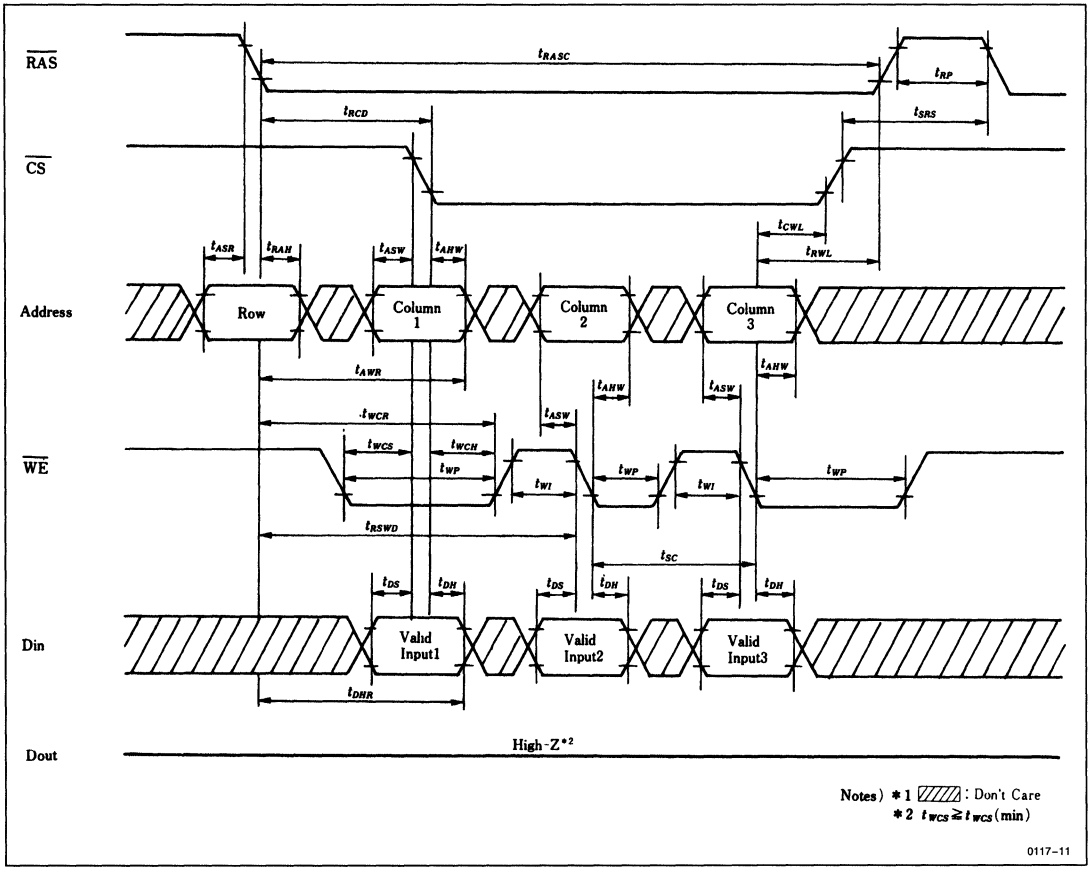
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



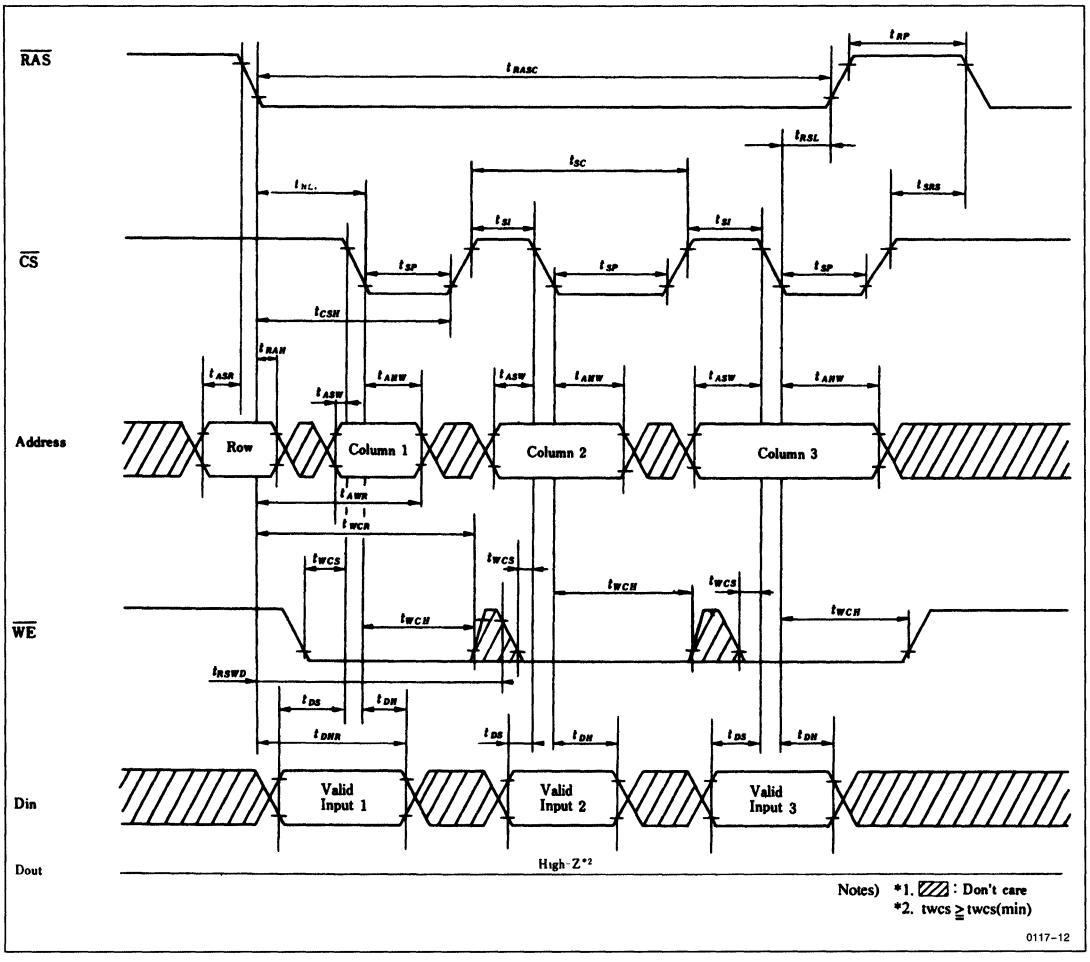
• Static Column Mode Read Cycle



• Static Column Mode Write Cycle (1)



• **Static Column Mode Write Cycle (2)**



Notes) *1. ▨ : Don't care
*2. twcs ≧ twcs(min)

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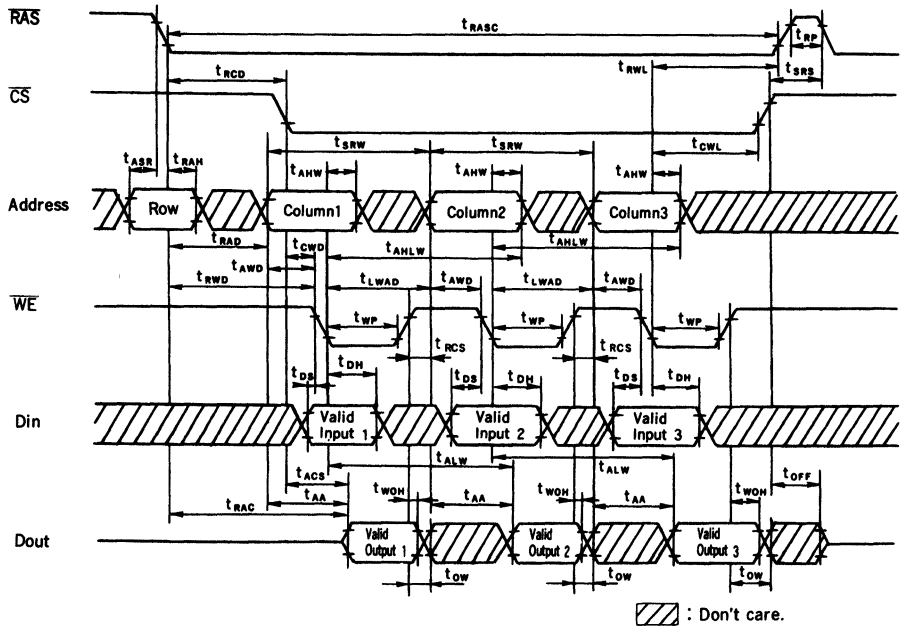
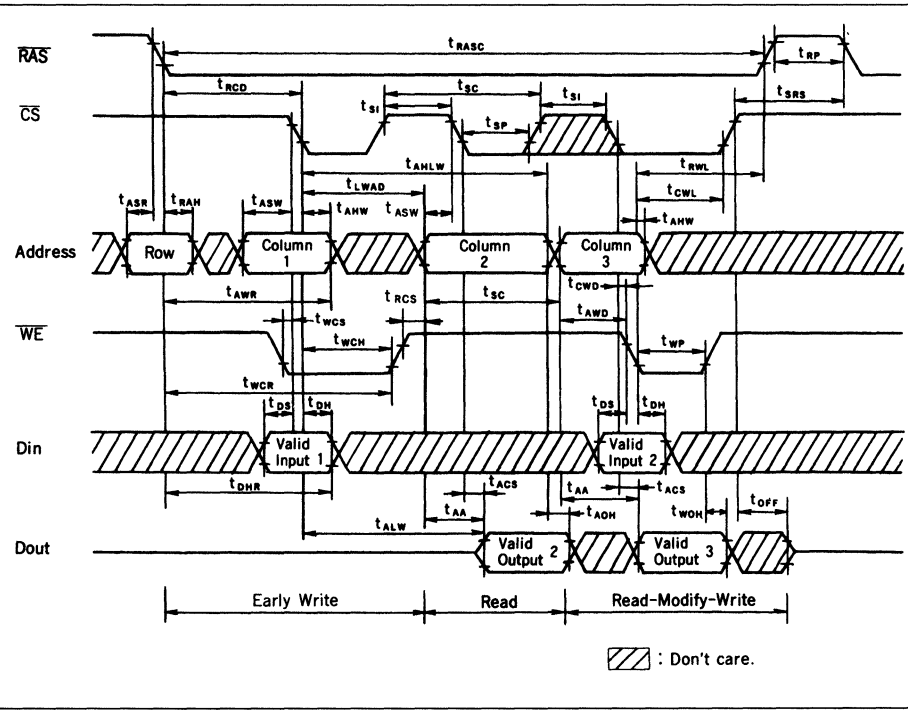
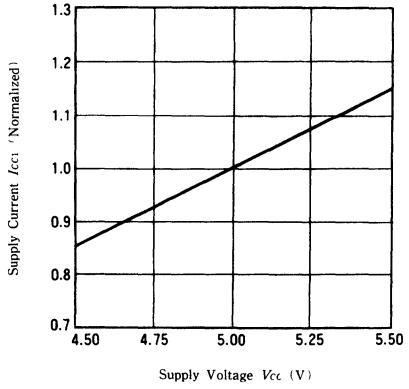
• **Static Column Mode Read-Modify-Write Cycle**



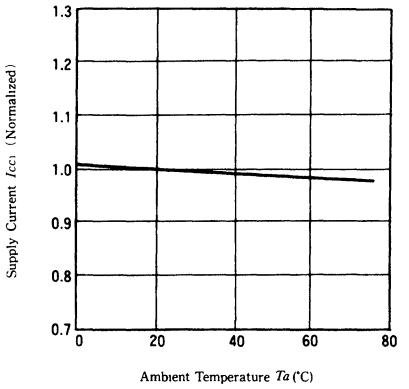
• **Static Column Mode Mixed Cycle**



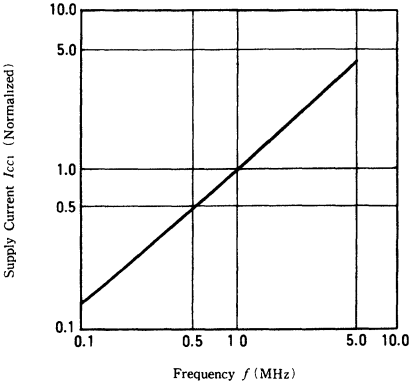
SUPPLY CURRENT (ACTIVE) vs. SUPPLY VOLTAGE



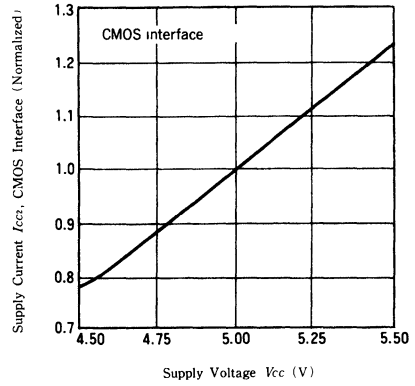
SUPPLY CURRENT (ACTIVE) vs. AMBIENT TEMPERATURE



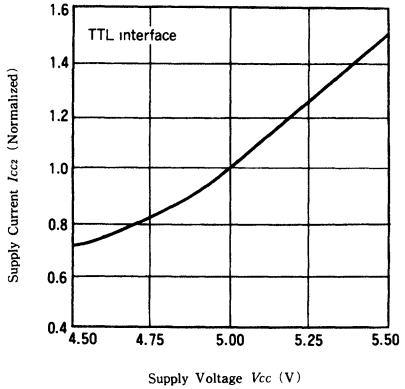
SUPPLY CURRENT (ACTIVE) vs. FREQUENCY



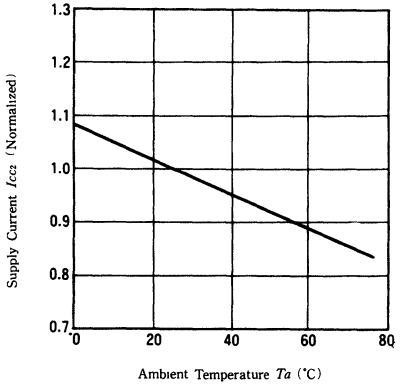
SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE



SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE

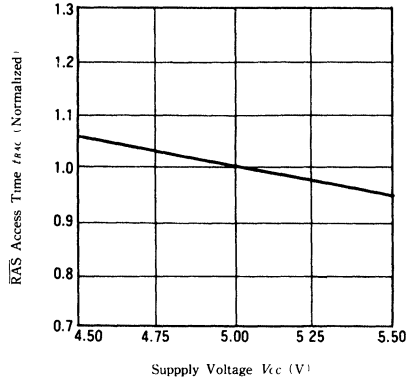


SUPPLY CURRENT (STANDBY) vs. AMBIENT TEMPERATURE

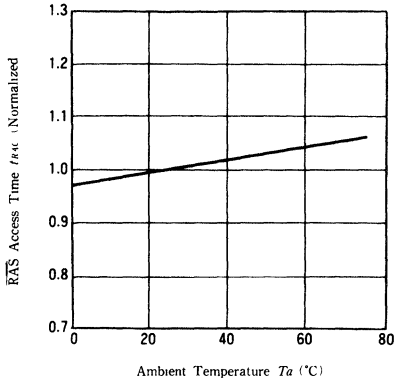


0117-15

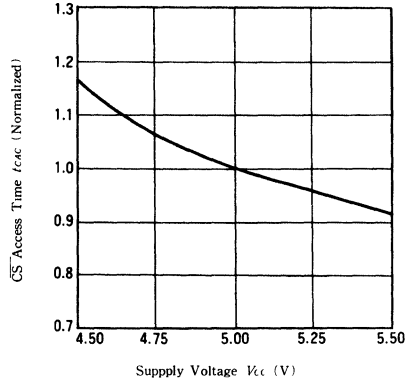
$\overline{RAS}$ ACCESS TIME vs. SUPPLY VOLTAGE



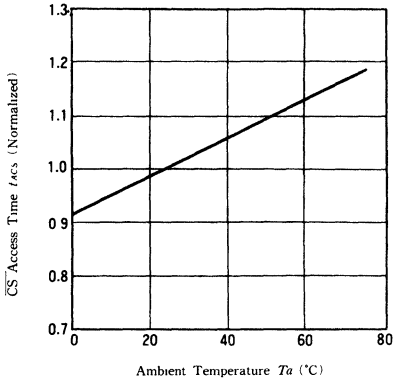
$\overline{RAS}$ ACCESS TIME vs. AMBIENT TEMPERATURE



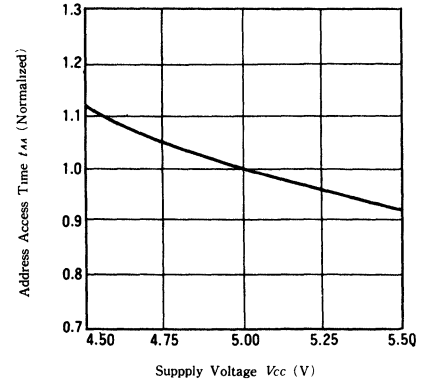
$\overline{CS}$ ACCESS TIME vs. SUPPLY VOLTAGE



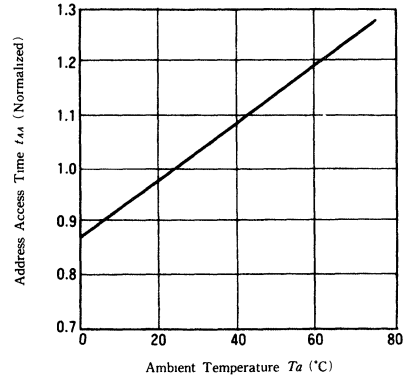
$\overline{CS}$ ACCESS TIME vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



0117-16

HM511664 Series — Preliminary

65,536-Word x 16-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM511664 are CMOS dynamic RAM organized as 65,536-word x 16-bit. HM511664 have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM511664 offer Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM511664 to be packaged in standard 400 mil 40-pin plastic SOJ, standard 475 mil 40-pin plastic ZIP.

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode .....TBD
  - Standby Mode.....11 mW (max)
- Fast Page Mode Capability
- Byte Write Capability
- 256 Refresh Cycles .....(4 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh

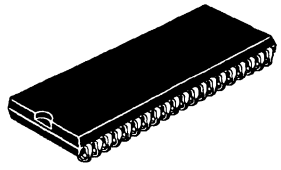
■ ORDERING INFORMATION

Part No.	Access Time	Package
HM511664JP-8 HM511664JP-10	80 ns 100 ns	400 mil 40-pin Plastic SOJ (CP-40D)
HM511664ZP-8 HM511664ZP-10	80 ns 100 ns	475 mil 40-pin Plastic ZIP (ZP-40)

■ PIN DESCRIPTION

Pin Name	Function
A_0-A_7	Address Input Refresh Address Input
I/O_1-I/O_{16}	Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{UW}$	Read/Upper Byte Write Enable
$\overline{LW}$	Read/Lower Byte Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

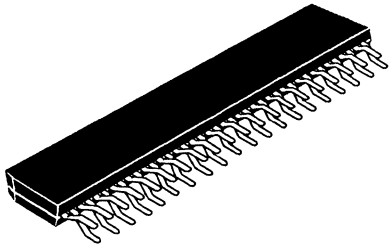
HM511664JP Series



3DCP40D

(CP-40D)

HM511664ZP Series

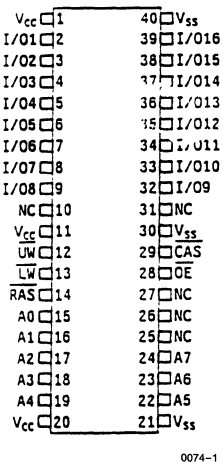


3DZP40

(ZP-40)

■ PIN OUT

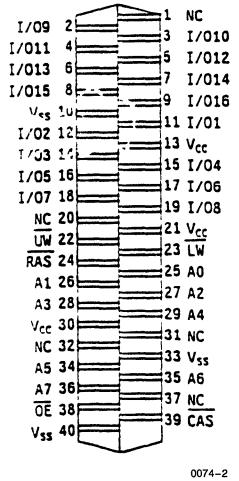
HM511664JP Series



0074-1

(Top View)

HM511664ZP Series



0074-2

(Bottom View)

■ TRUTH TABLE

Inputs					I/O		Operation
$\overline{RAS}$	$\overline{CAS}$	$\overline{LW}$	$\overline{UW}$	$\overline{OE}$	I/O_1–I/O_8	I/O_9–I/O_{16}	
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	D_{out}	D_{out}	Read
L	L	L	H	H	D_{in}	Don't Care	Lower Byte Write
L	L	H	L	H	Don't Care	D_{in}	Upper Byte Write
L	L	L	L	H	D_{in}	D_{in}	Word Write
L	L	L	L	H	High-Z	High-Z	

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	0.8	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/Oi Pin)	V_{IL}	−0.5	—	0.8	V	1, 2
	(Others)	V_{IL}	−1.0	—	0.8	V	1, 2

Notes: 1. All voltage referenced to V_{SS}.
2. The device will withstand undershoots to the −2V level with a maximum pulse width of 20 ns at the −1.5V level. (See figure 1.)

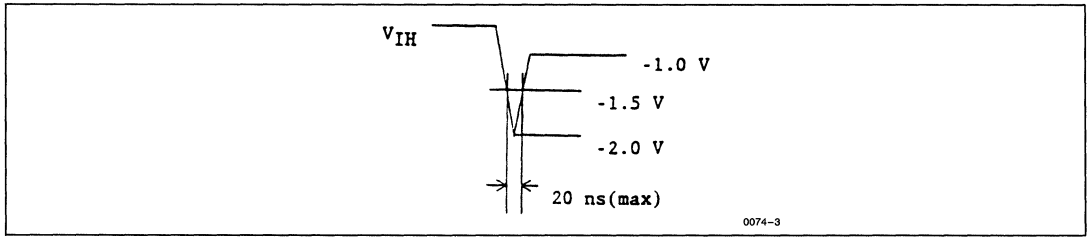


Figure 1. Undershoot of input voltage

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM511664-8		HM511664-10		Unit	Test Conditions	Note
		Min	Max	Min	Max			
Operating Current	I_{CC1}	TBD				mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	2				mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		1				mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	TBD				mA	t_{RC} = Min	2
Standby Current	I_{CC5}	TBD				mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	TBD				mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	TBD				mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	µA	0V ≤ V_{in} ≤ 6.5V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	µA	0V ≤ V_{out} ≤ 5.5V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 2.5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	V	Low I_{out} = 2.1 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• Capacitance (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 14, 15, 16]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM511664-8		HM511664-10		Unit	Note
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	135	—	170	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	45	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	30	10000	40	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	20	60	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	15	45	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	30	—	40	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	15	—	15	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	ns	
$\overline{CAS}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	4	—	4	ms	

Read Cycle

Parameter	Symbol	HM511664-8		HM511664-10		Unit	Note
		Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	—	40	ns	3, 4, 13
Access Time from Address	t_{AA}	—	45	—	55	ns	3, 5, 13
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	40	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	20	0	20	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	15	0	15	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	20	—	20	—	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	t_{ROH}	10	—	10	—	ns	

Write Cycle

Parameter	Symbol	HM511664-8		HM511664-10		Unit	Note
		Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM511664-8		HM511664-10		Unit	Note
		Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	185	—	220	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	105	—	125	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	55	—	65	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	70	—	80	—	ns	10, 13
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	15	—	15	—	ns	

Refresh Cycle

Parameter	Symbol	HM511664-8		HM511664-10		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time in Normal Mode	t_{CPN}	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM511664-8		HM511664-10		Unit	Note
		Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	80	100000	100	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	45	—	55	ns	3, 13
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	45	—	55	—	ns	
Fast Page Mode Read-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPW}	70	—	80	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	100	—	110	—	ns	

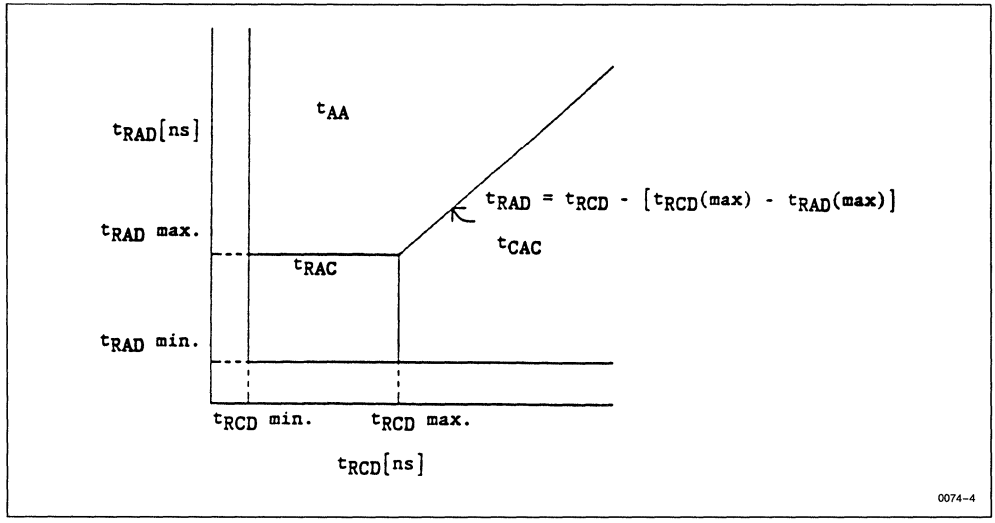
Counter Test Cycle

Parameter	Symbol	HM511664-8		HM511664-10		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	40	—	ns	

Byte Write Mode

Parameter	Symbol	HM511664-8		HM511664-10		Unit	Note
		Min	Max	Min	Max		
Masked Write Setup Time	t_{MCS}	0	—	0	—	ns	
Masked Write Hold Time Referenced to $\overline{RAS}$	t_{MRH}	0	—	0	—	ns	
Masked Write Hold Time Referenced to $\overline{CAS}$	t_{MCH}	0	—	0	—	ns	

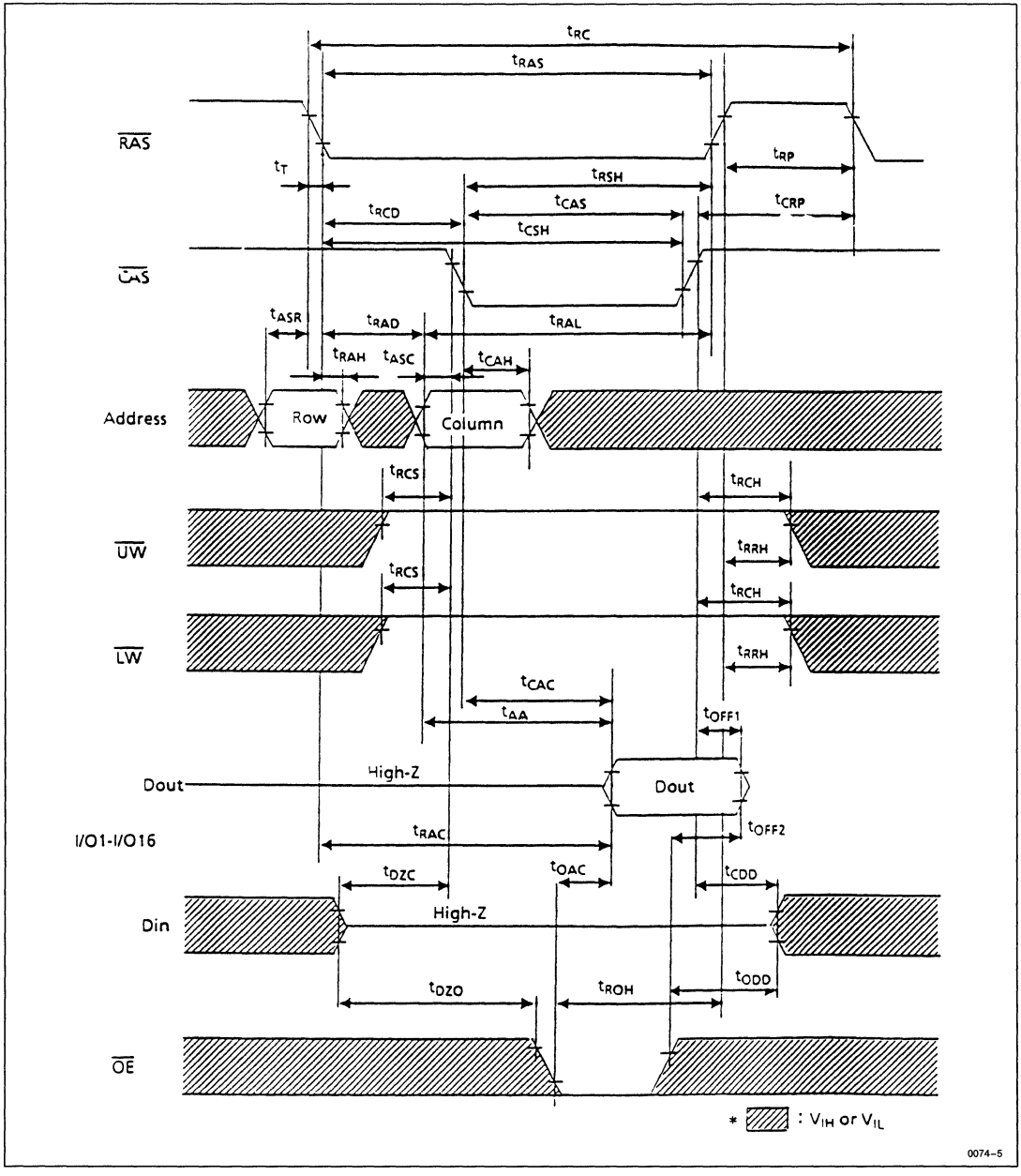
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 1 TTL load and 50 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $(t_{RCD} - t_{RAD}) \geq [t_{RCD}$ (max) $- t_{RAD}$ (max)].
5. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $(t_{RCD} - t_{RAD}) \leq [t_{RCD}$ (max) $- t_{RAD}$ (max)]. t_{RAC}, t_{CAC}, and t_{AA} are determined as follows.



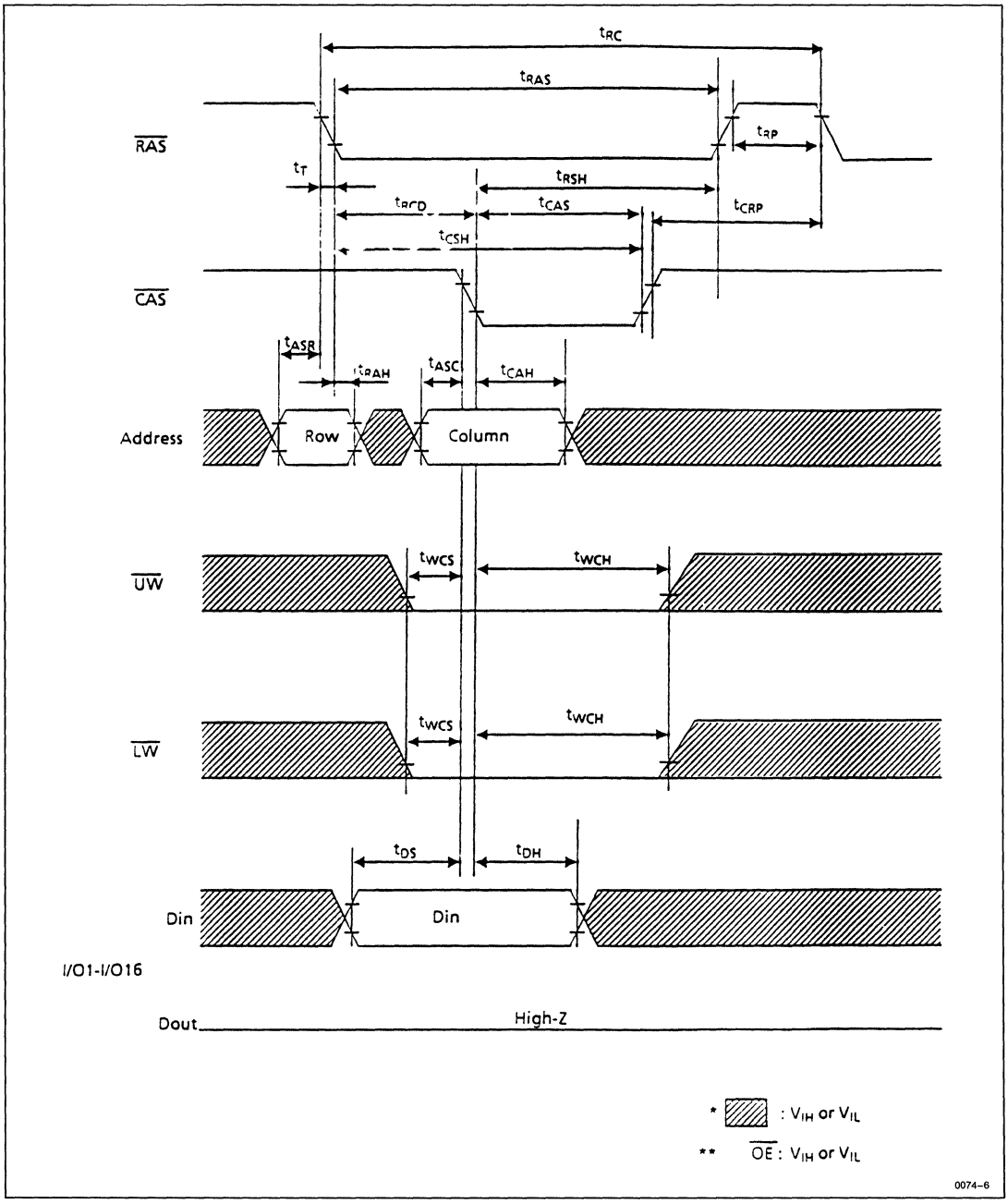
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, OE must disable output buffer prior to applying data to the device.
16. When both $\overline{LW}$ and $\overline{UW}$ go low at the same time, all 16-bits data are written into the device. $\overline{LW}$ and $\overline{UW}$ cannot be staggered within the same write cycle.

■ TIMING WAVEFORMS

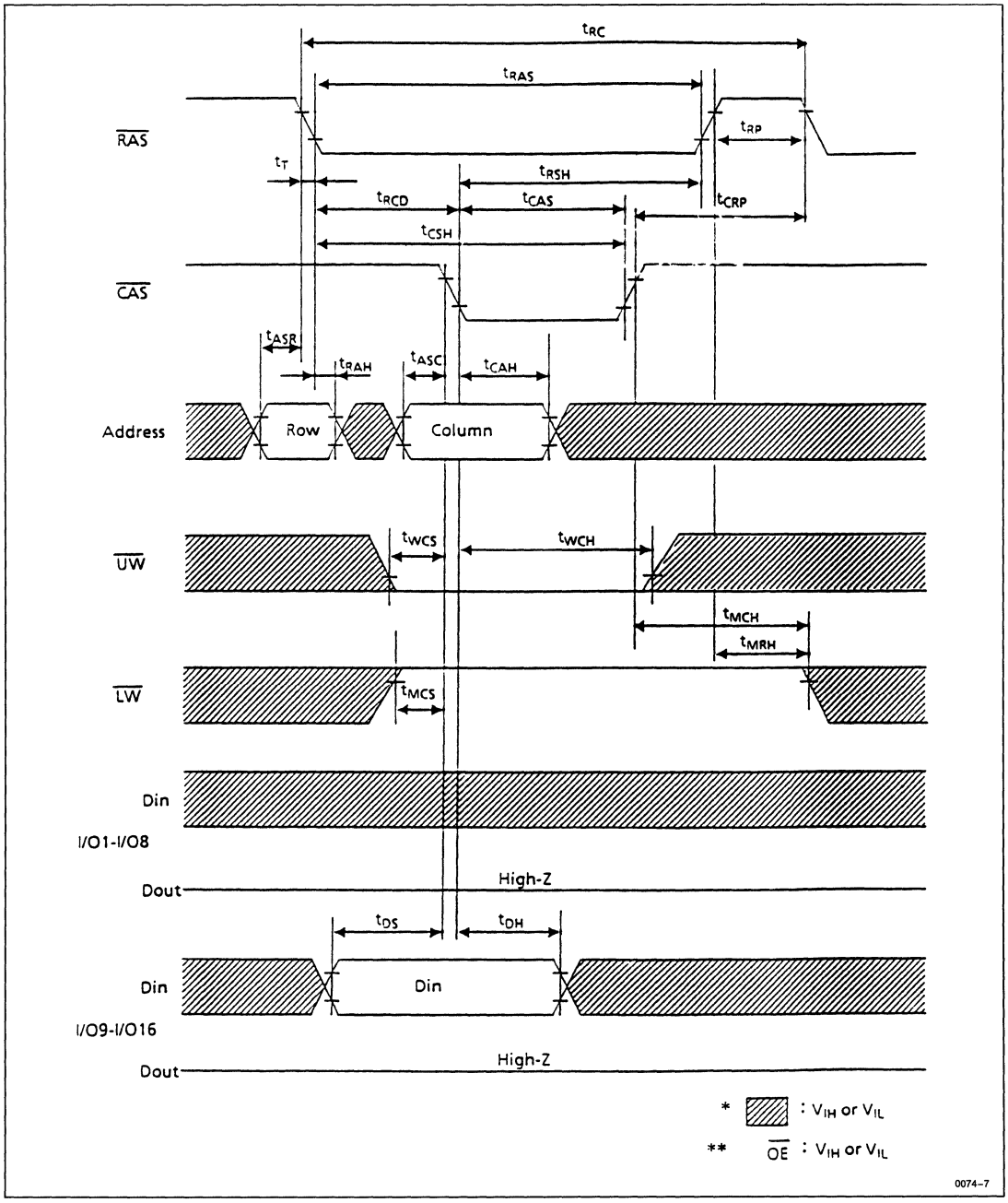
• Read Cycle



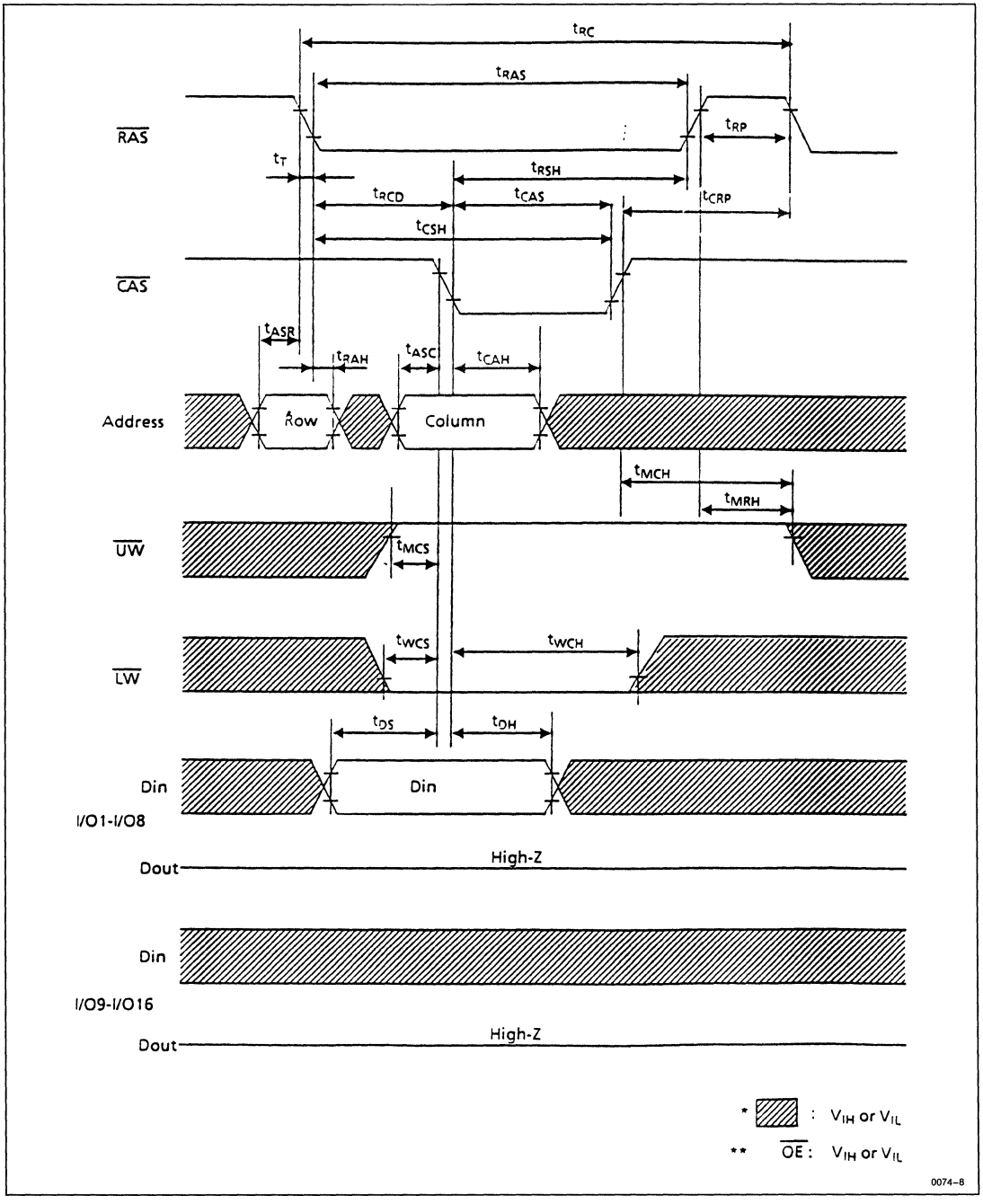
• **Early Write Cycle**



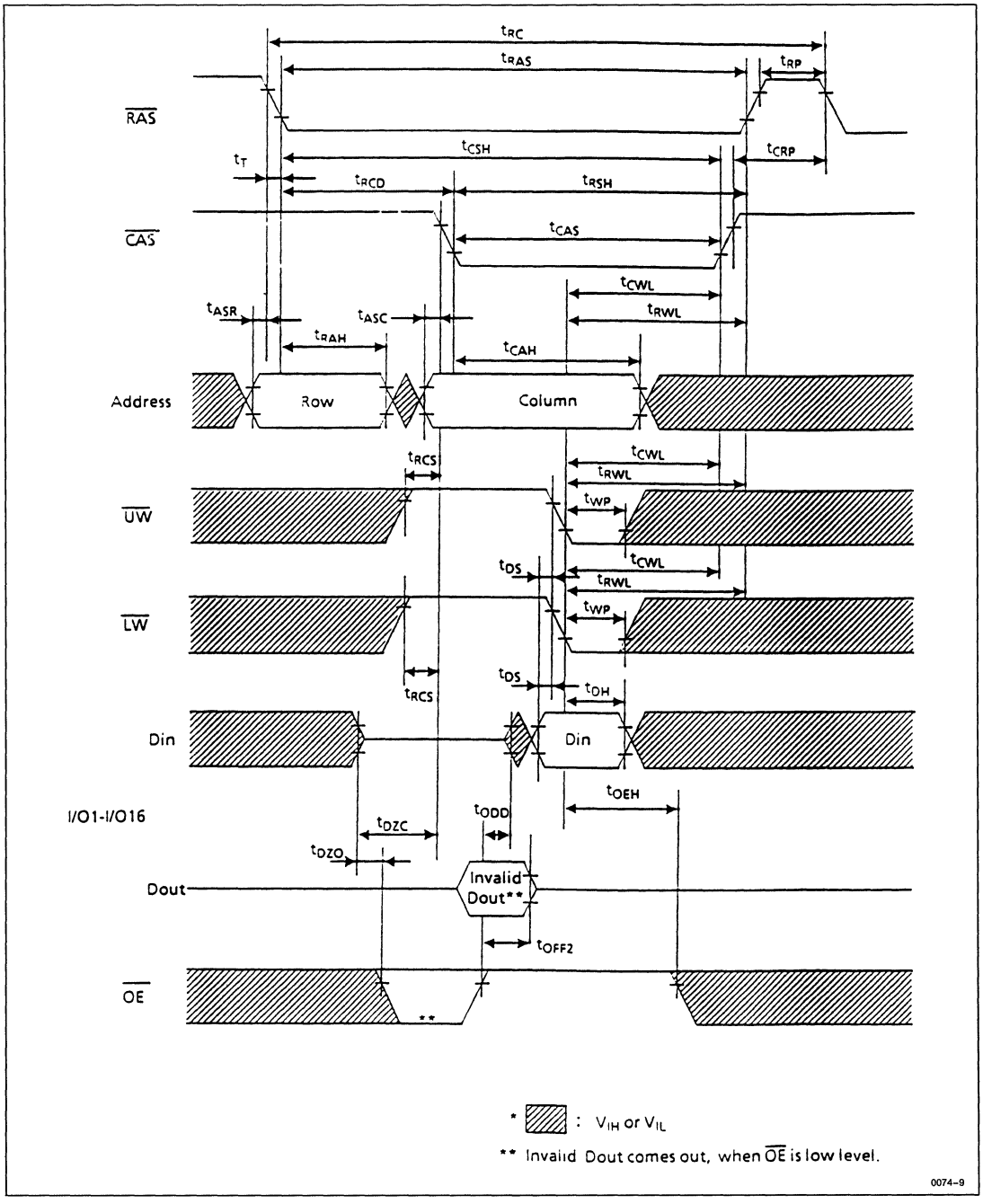
• **Upper Byte Early Write Cycle**



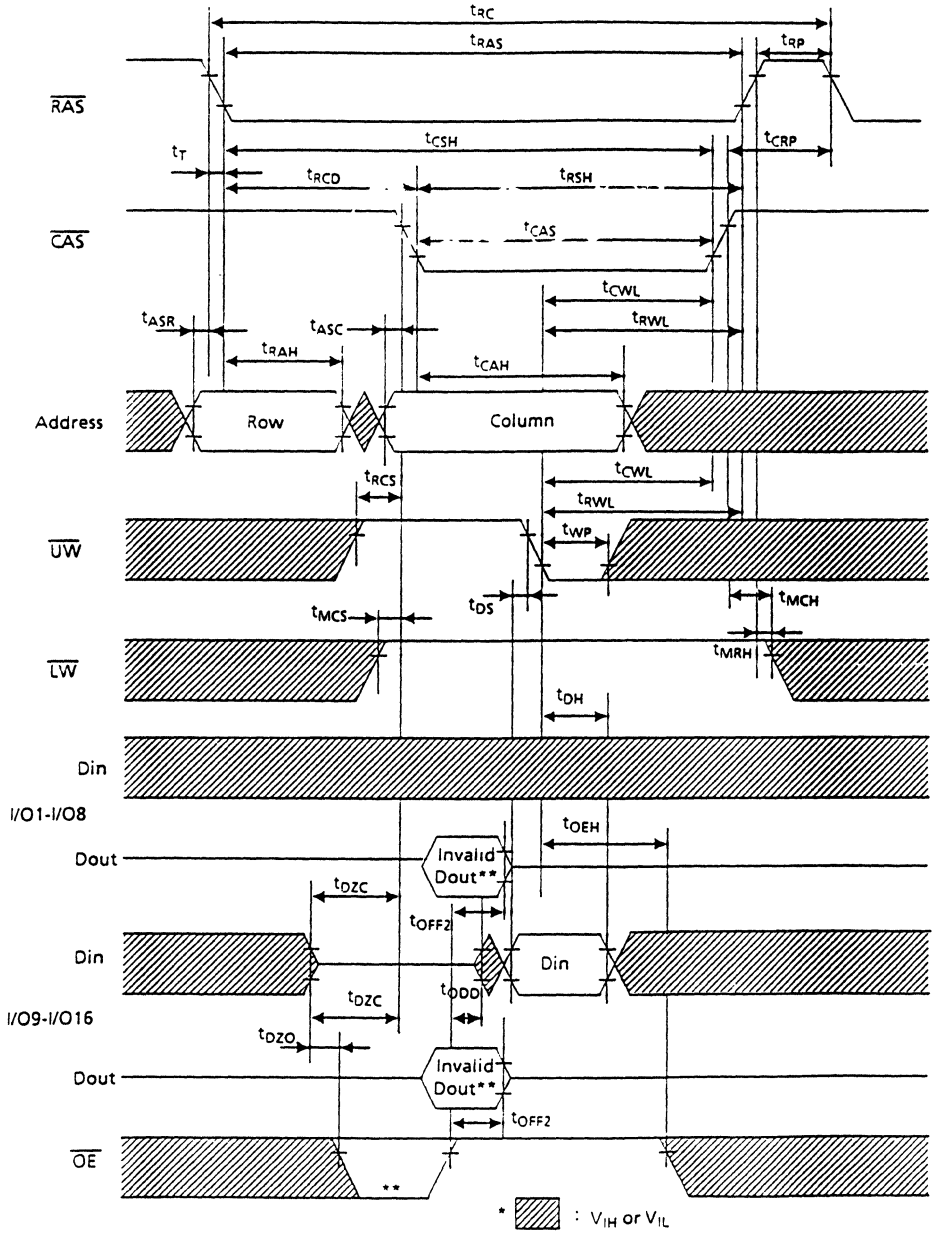
• **Lower Byte Early Write Cycle**



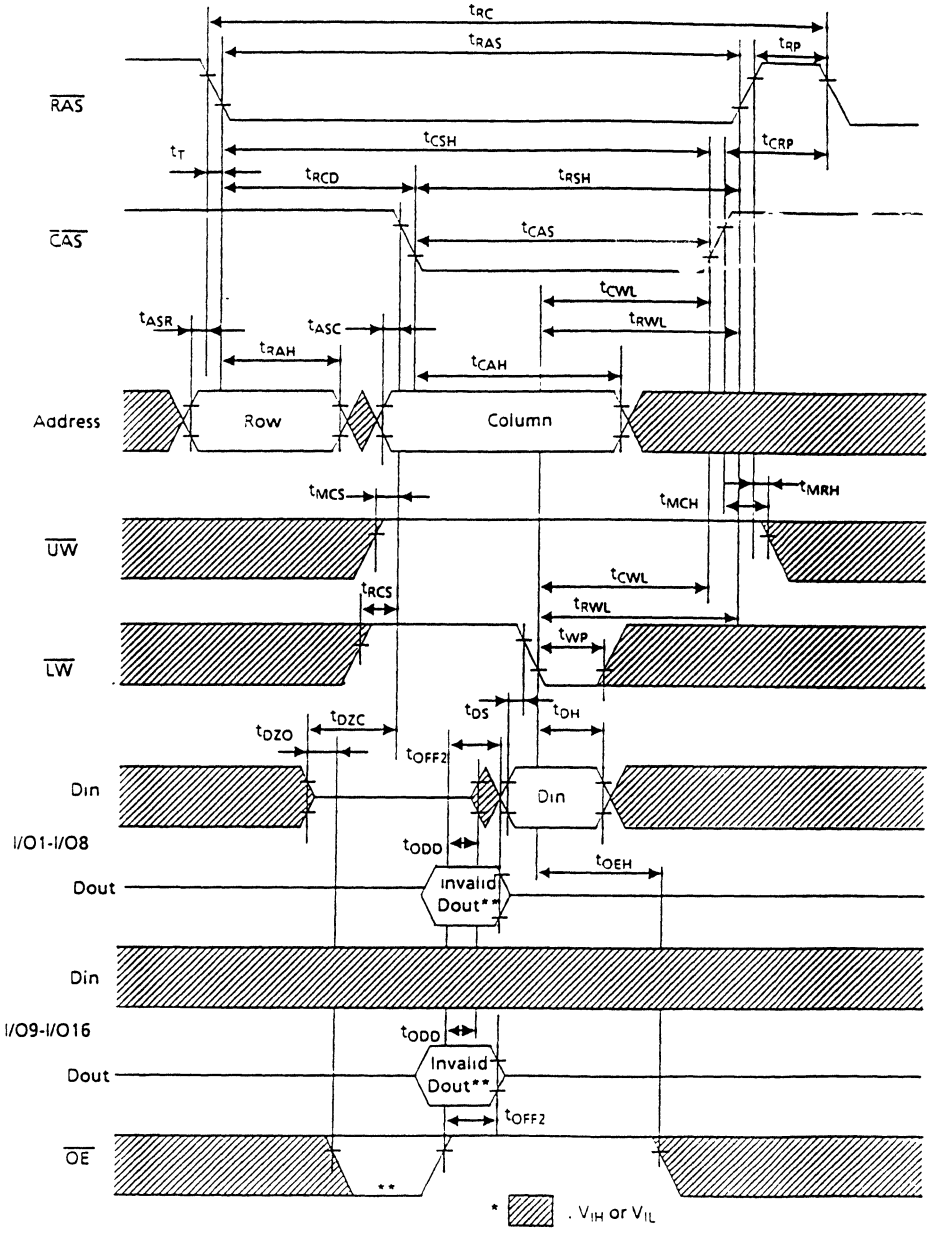
• **Delayed Write Cycle**



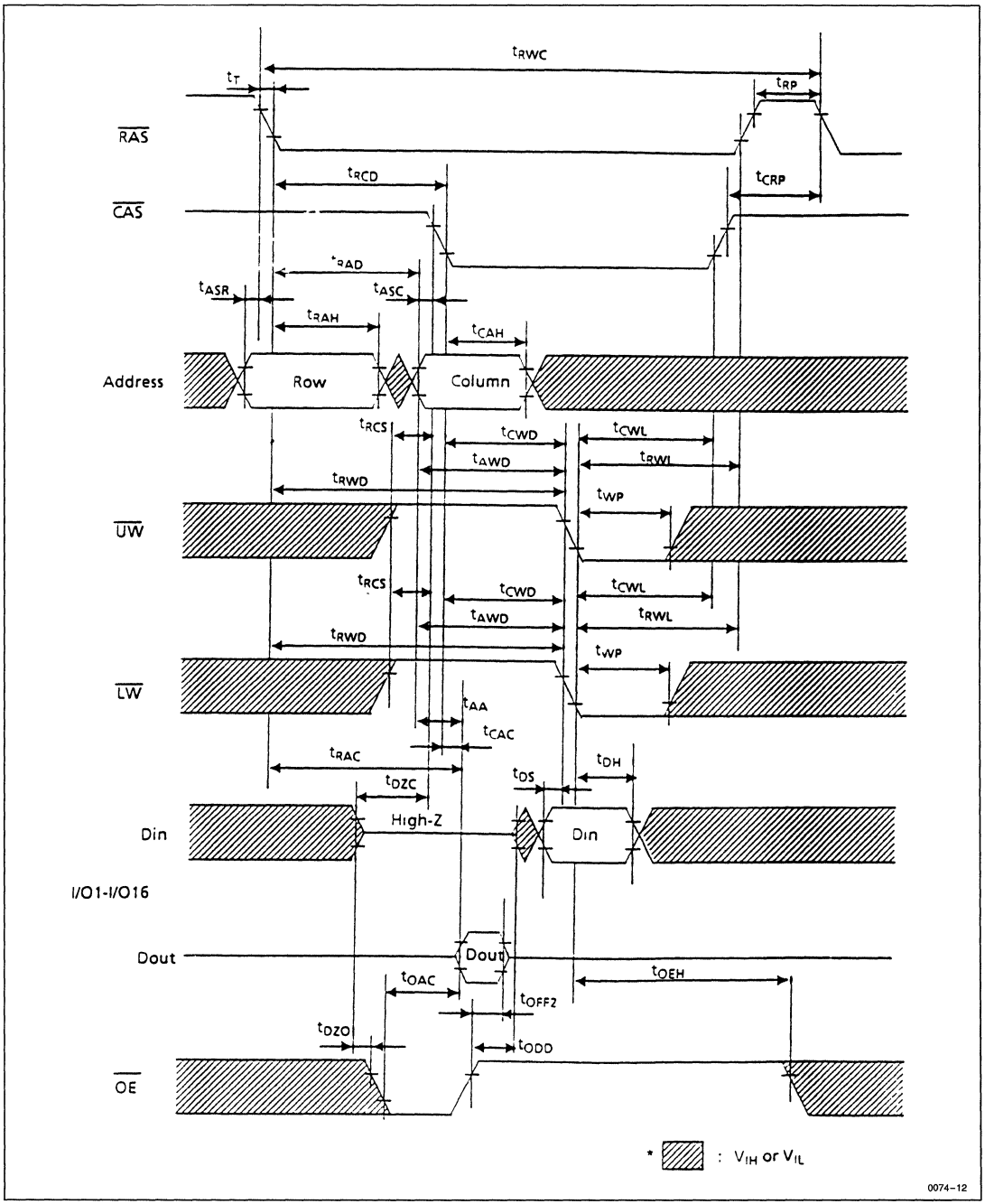
• **Upper Byte Delayed Write Cycle**



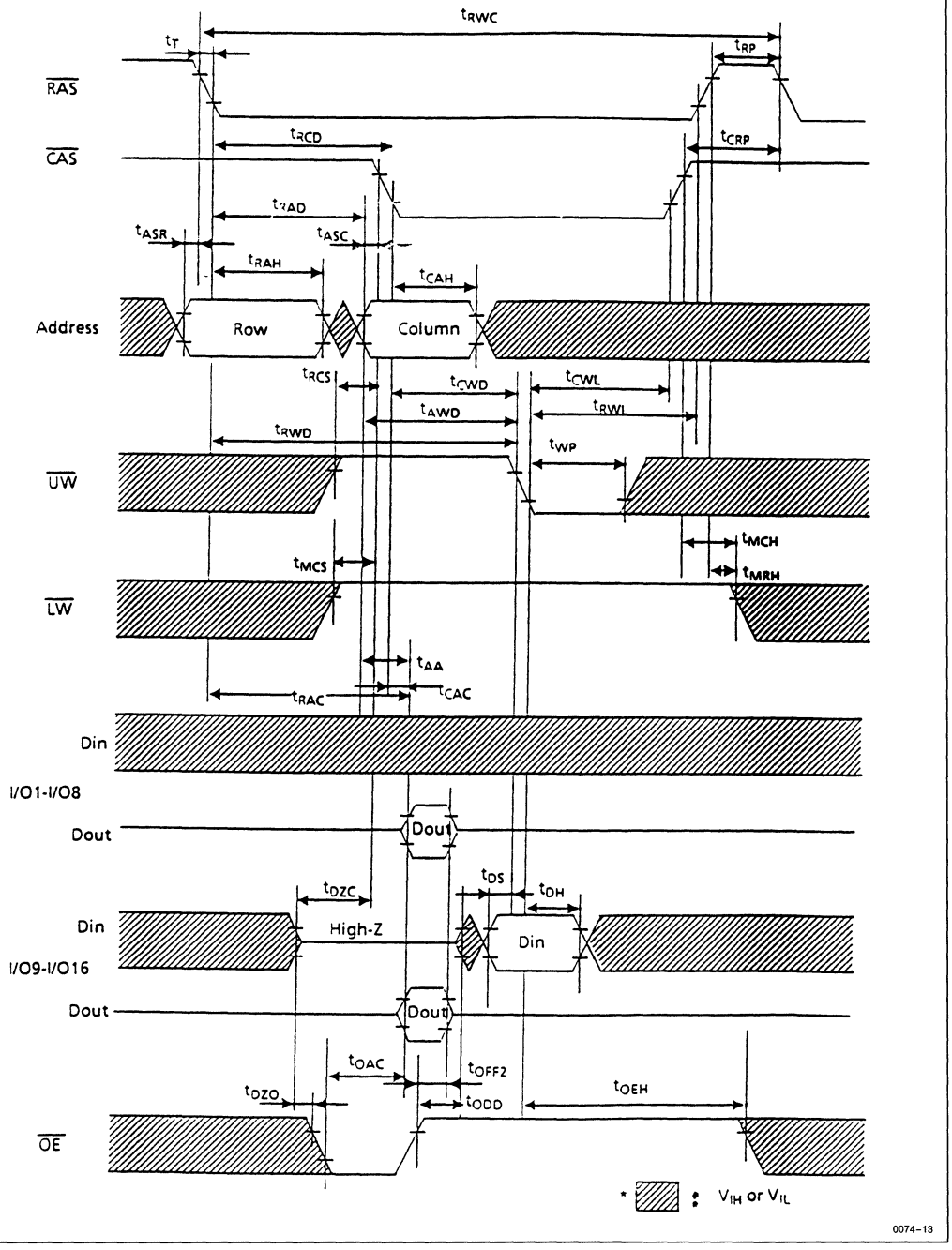
• **Lower Byte Delayed Write Cycle**



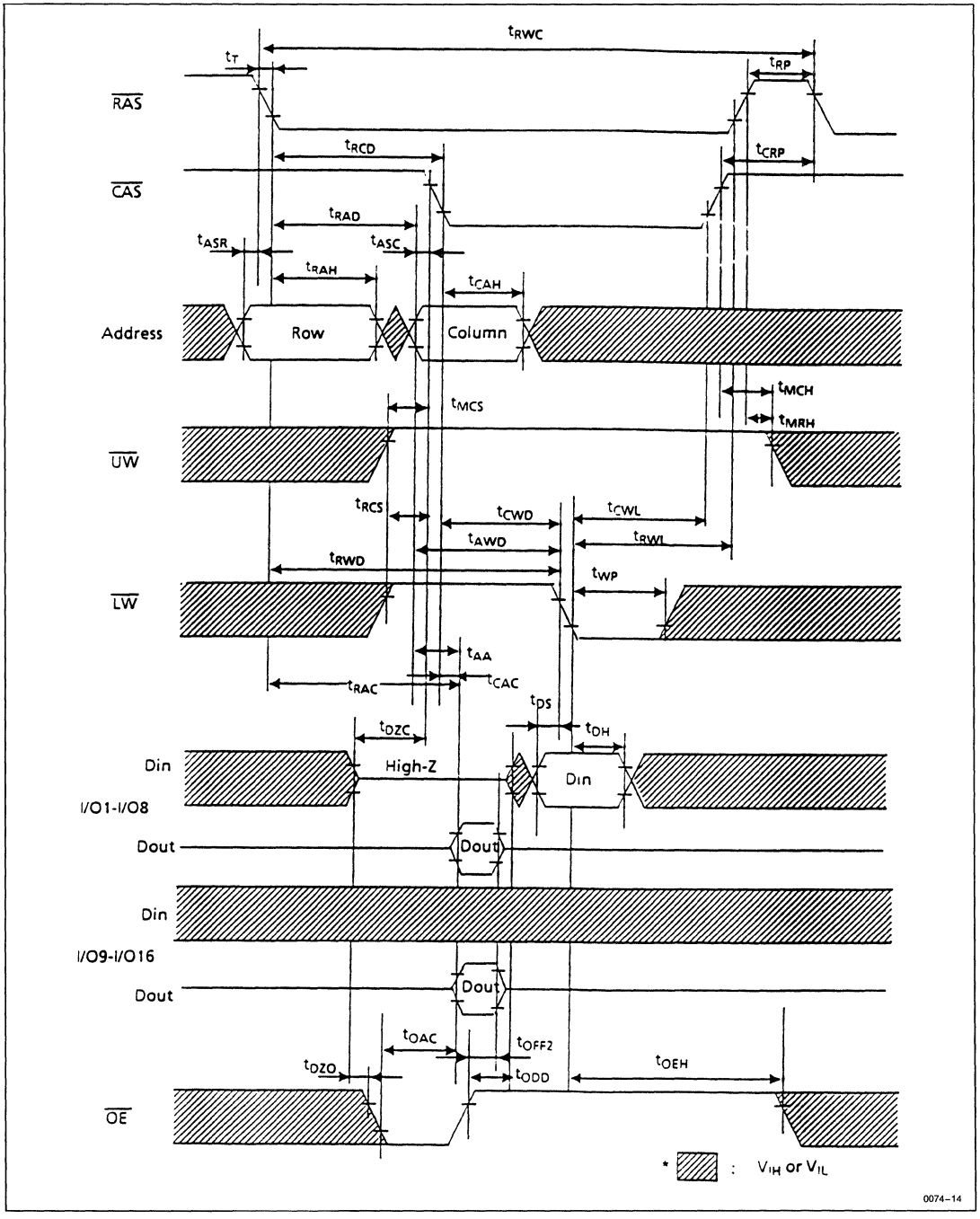
• **Read-Modify-Write Cycle**



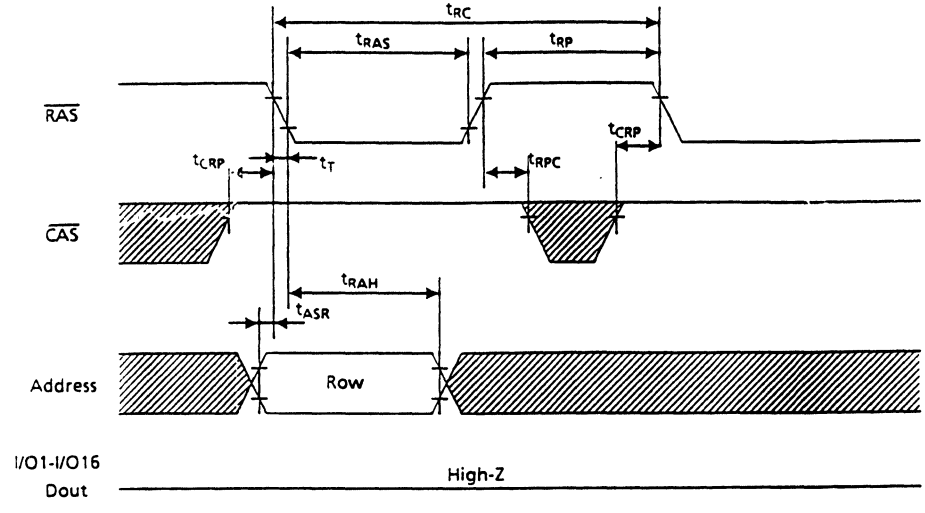
• **Read Modify Upper Byte Write Cycle**



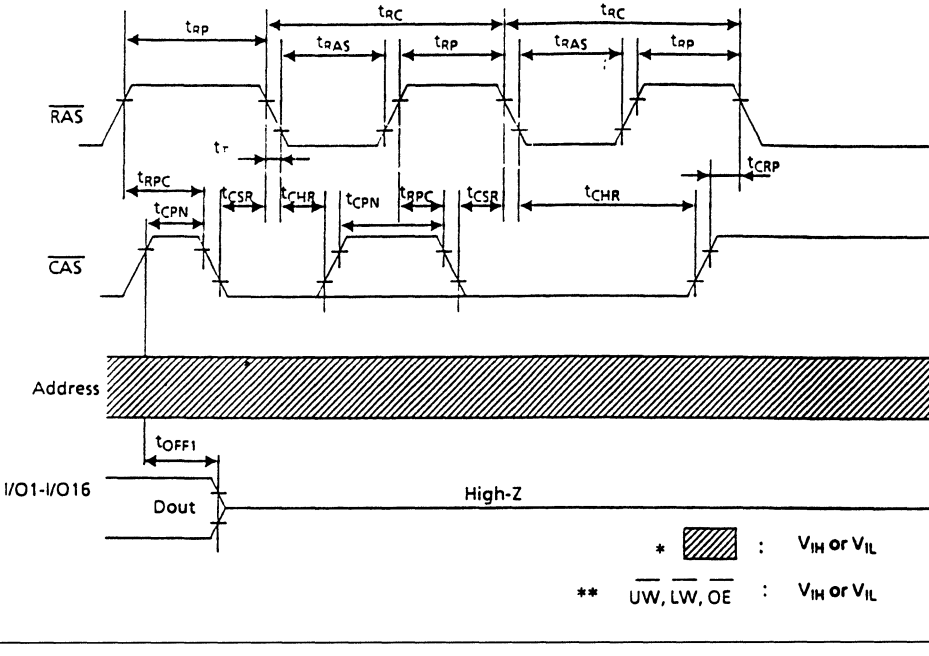
• **Read Modify Lower Byte Write Cycle**



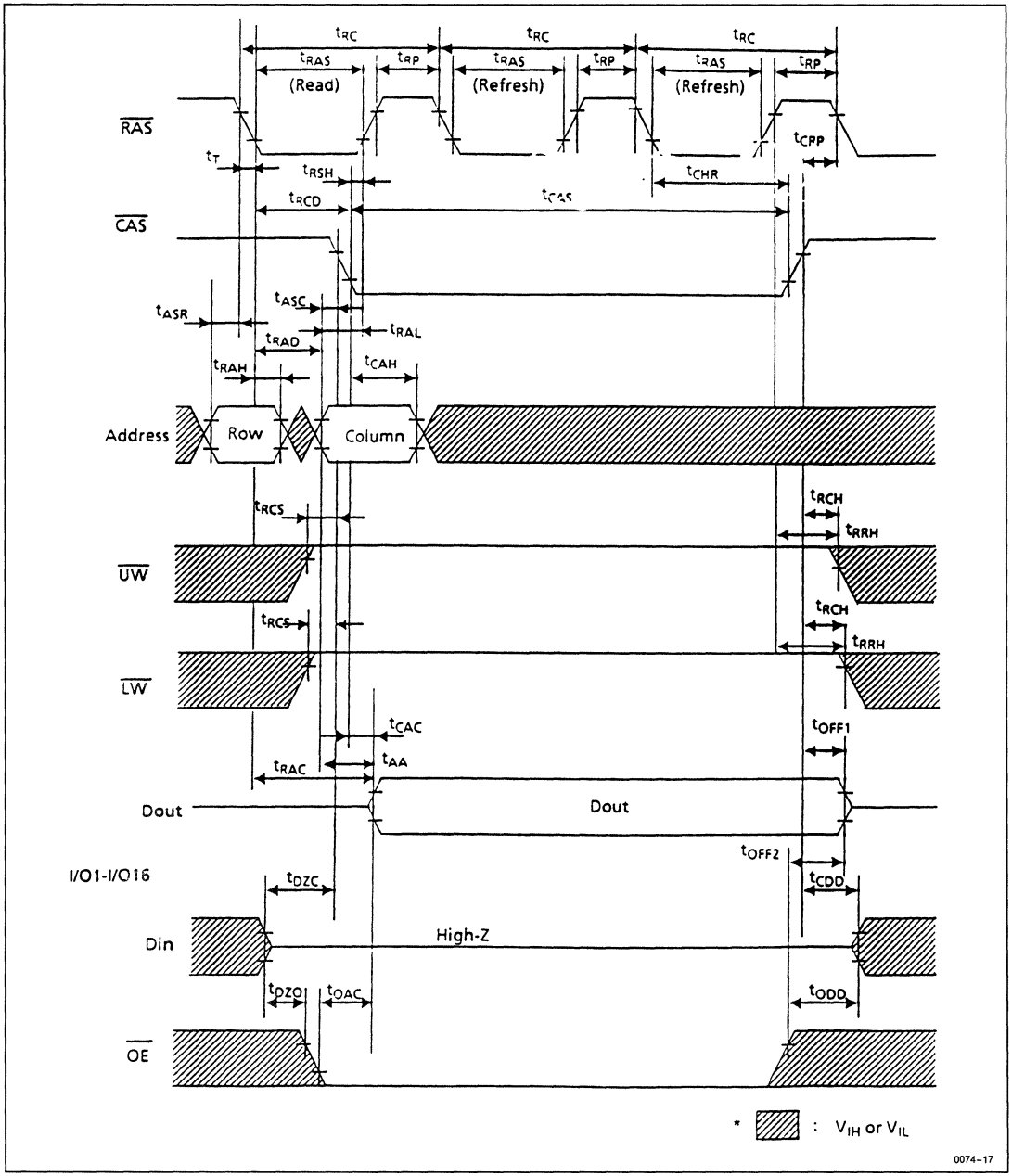
• $\overline{RAS}$ Only Refresh Cycle



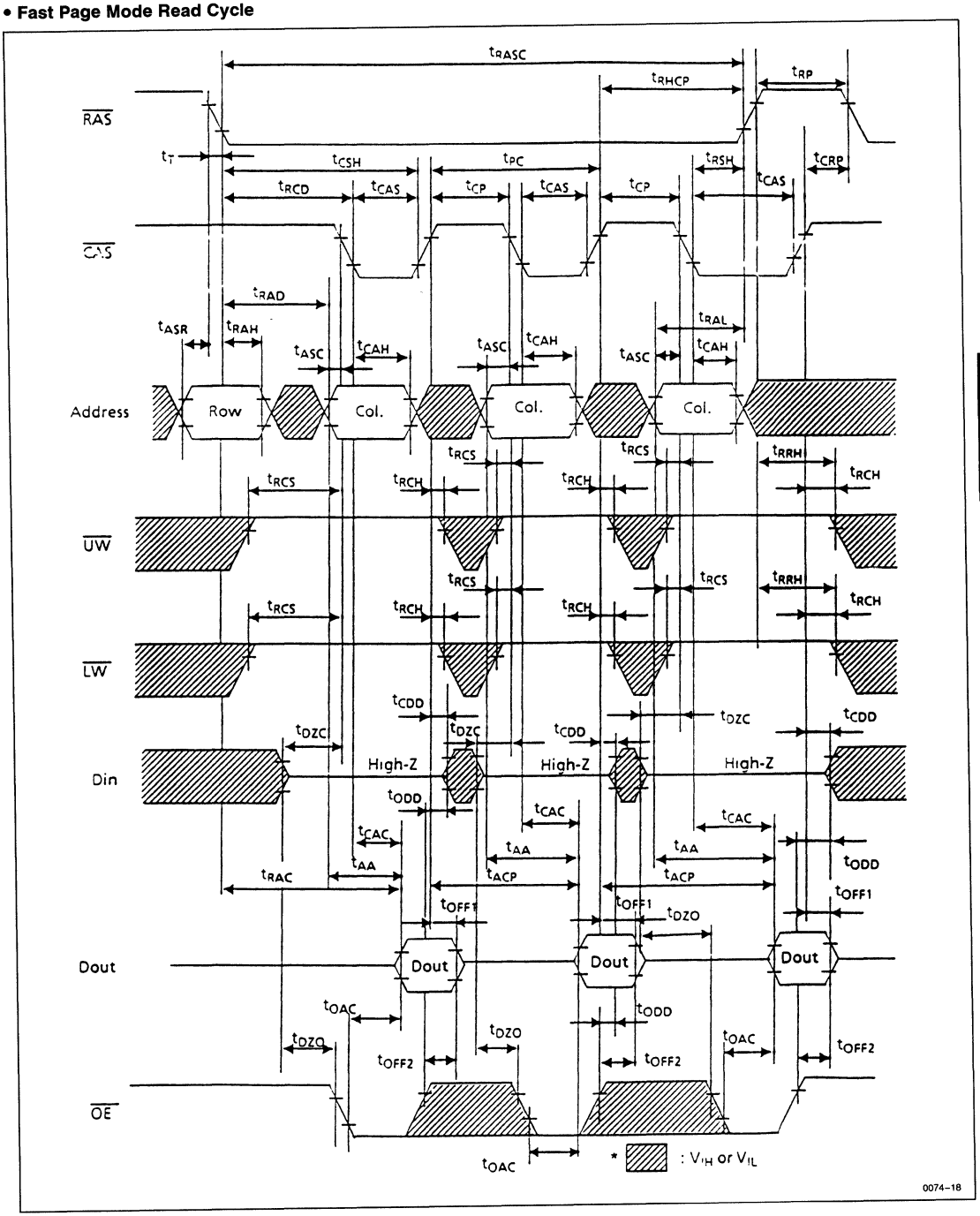
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



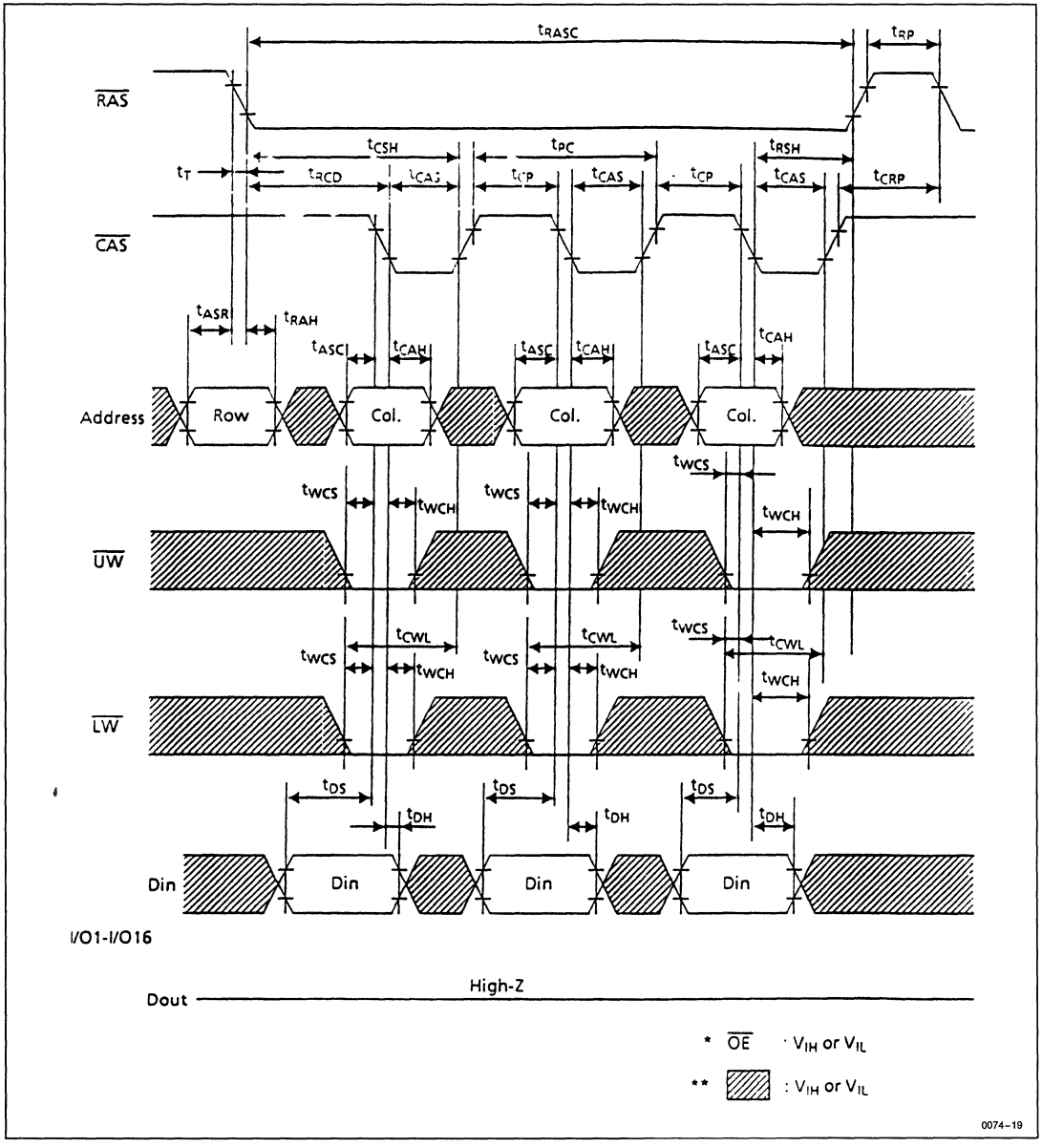
• Hidden Refresh Cycle



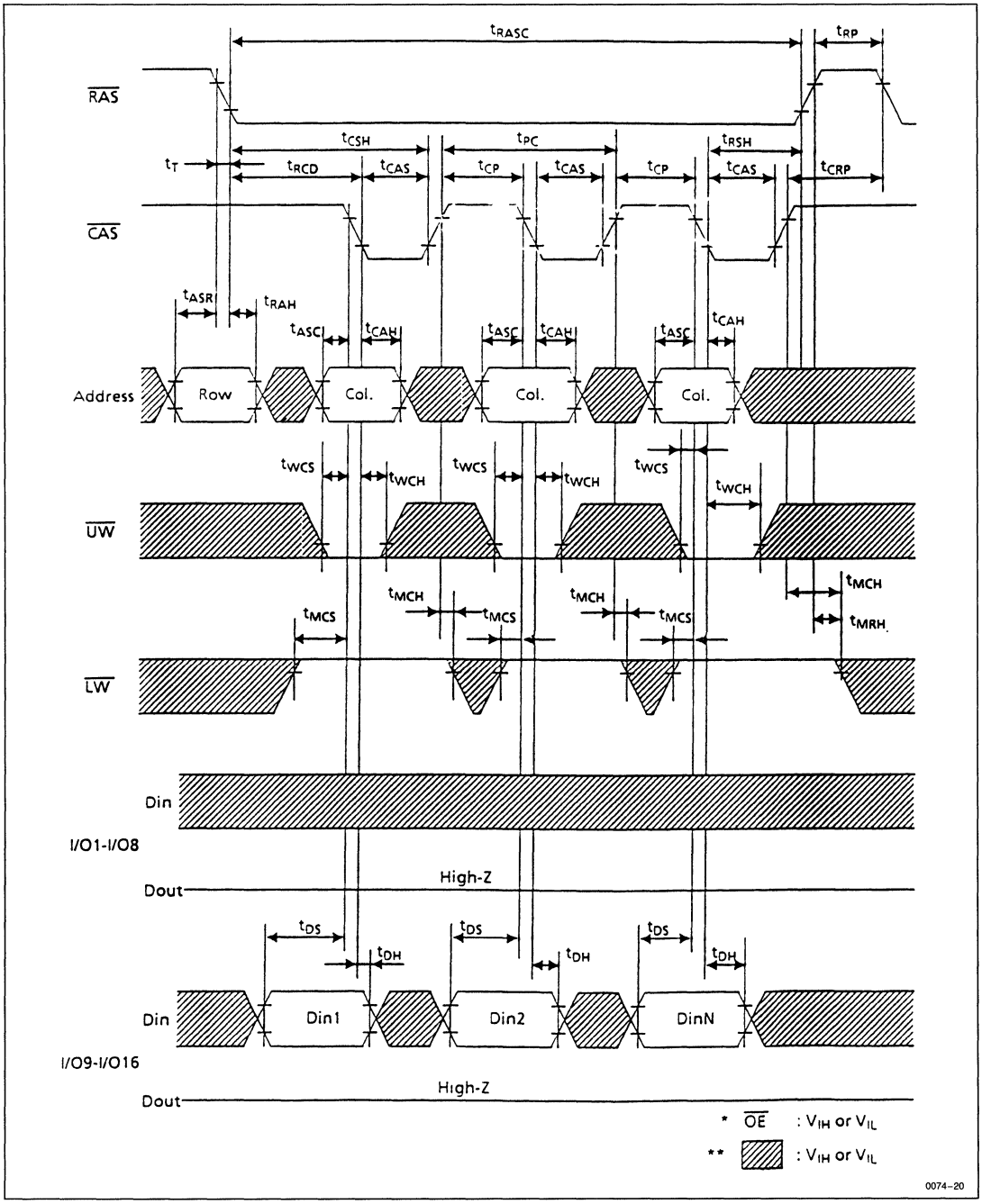
• **Fast Page Mode Read Cycle**



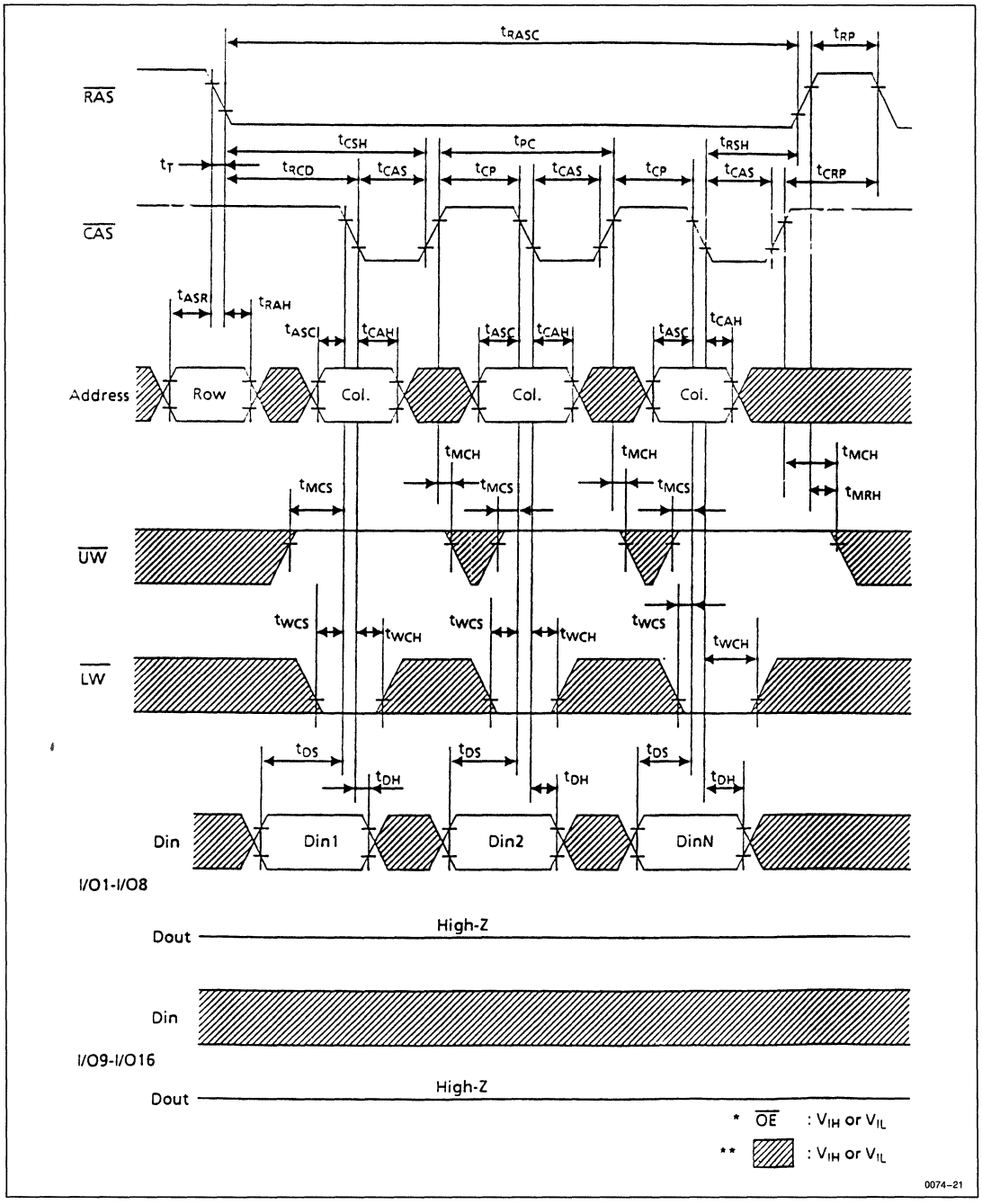
• **Fast Page Mode Early Write Cycle**



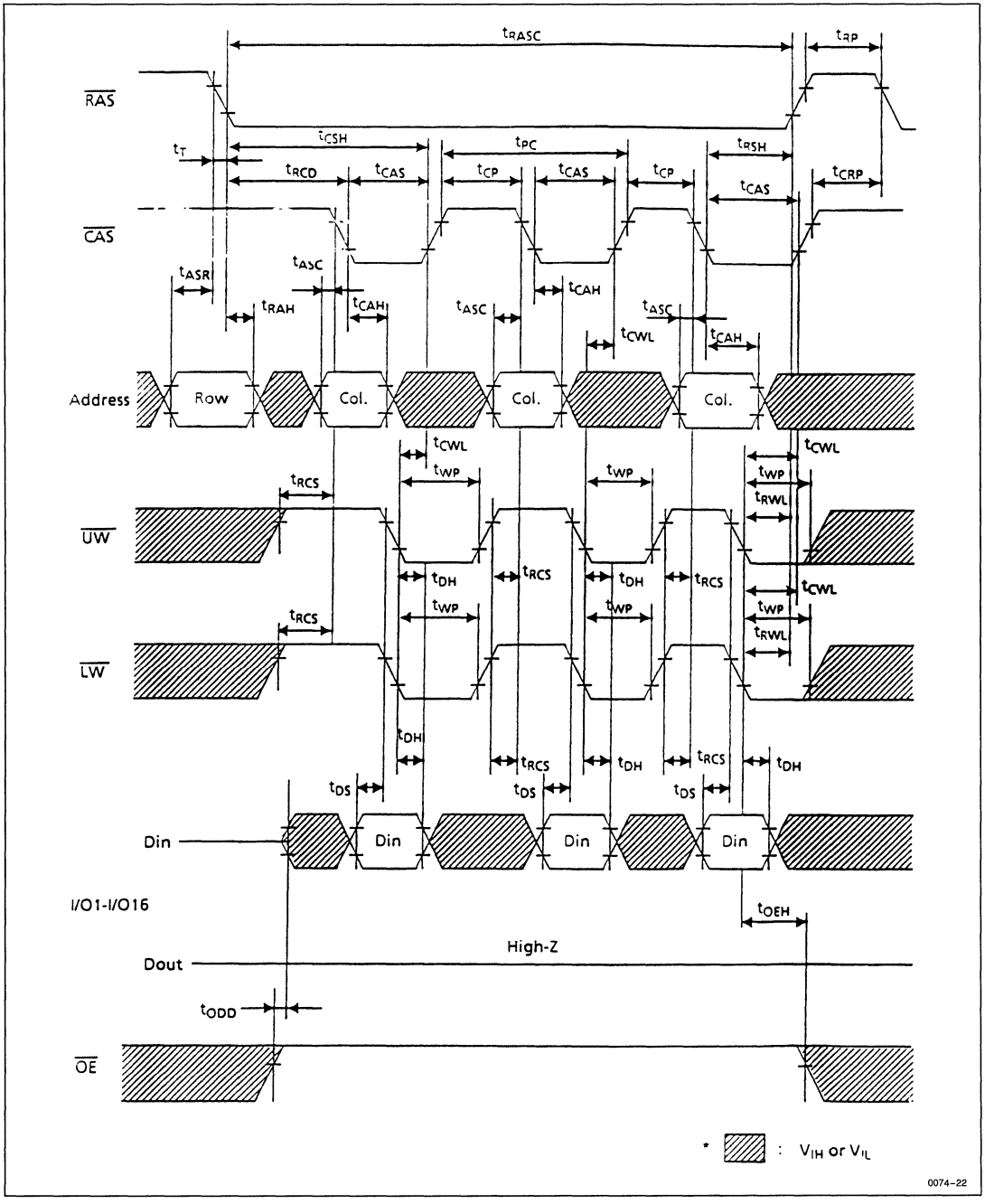
• **Fast Page Mode Upper Byte Early Write Cycle**



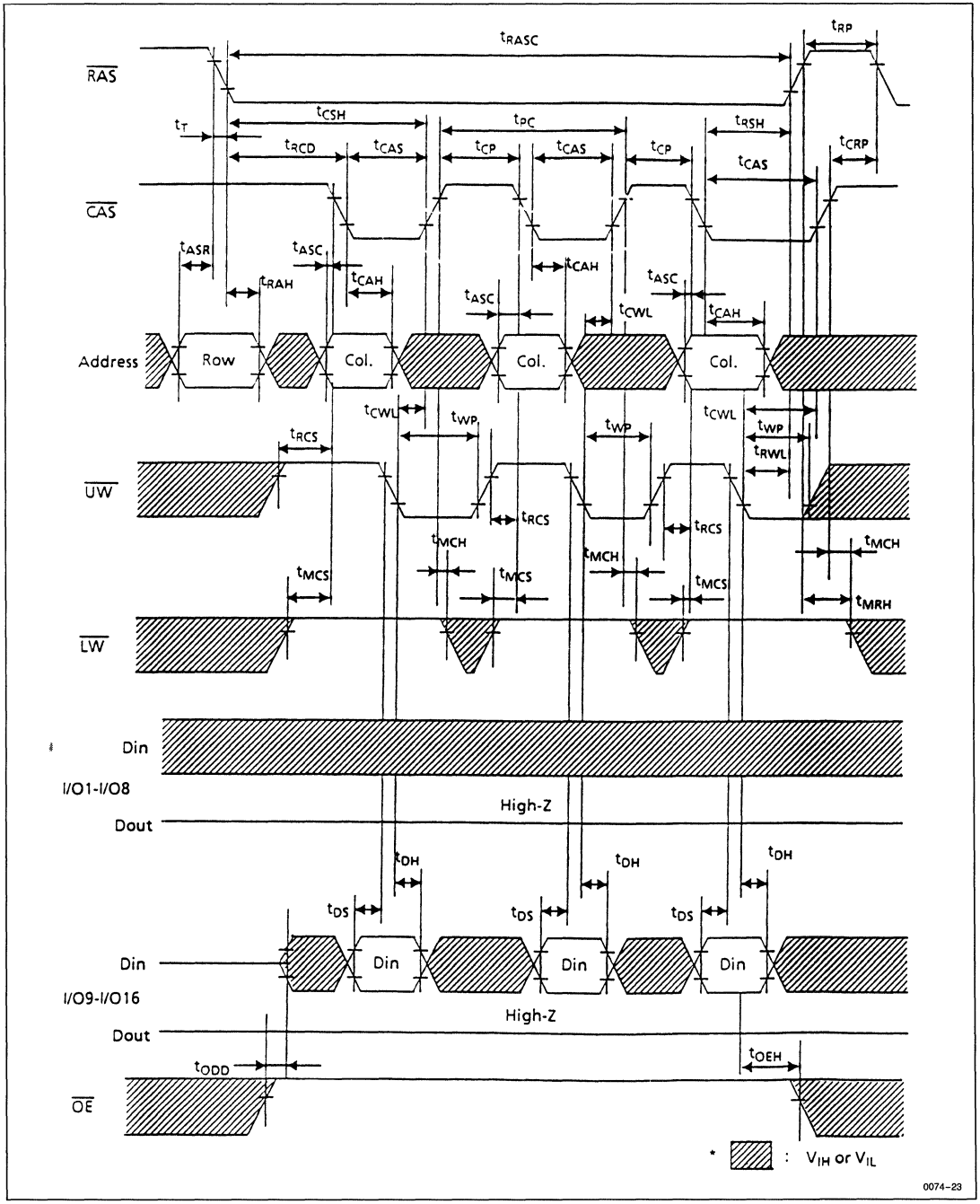
• Fast Page Mode Lower Byte Early Write Cycle



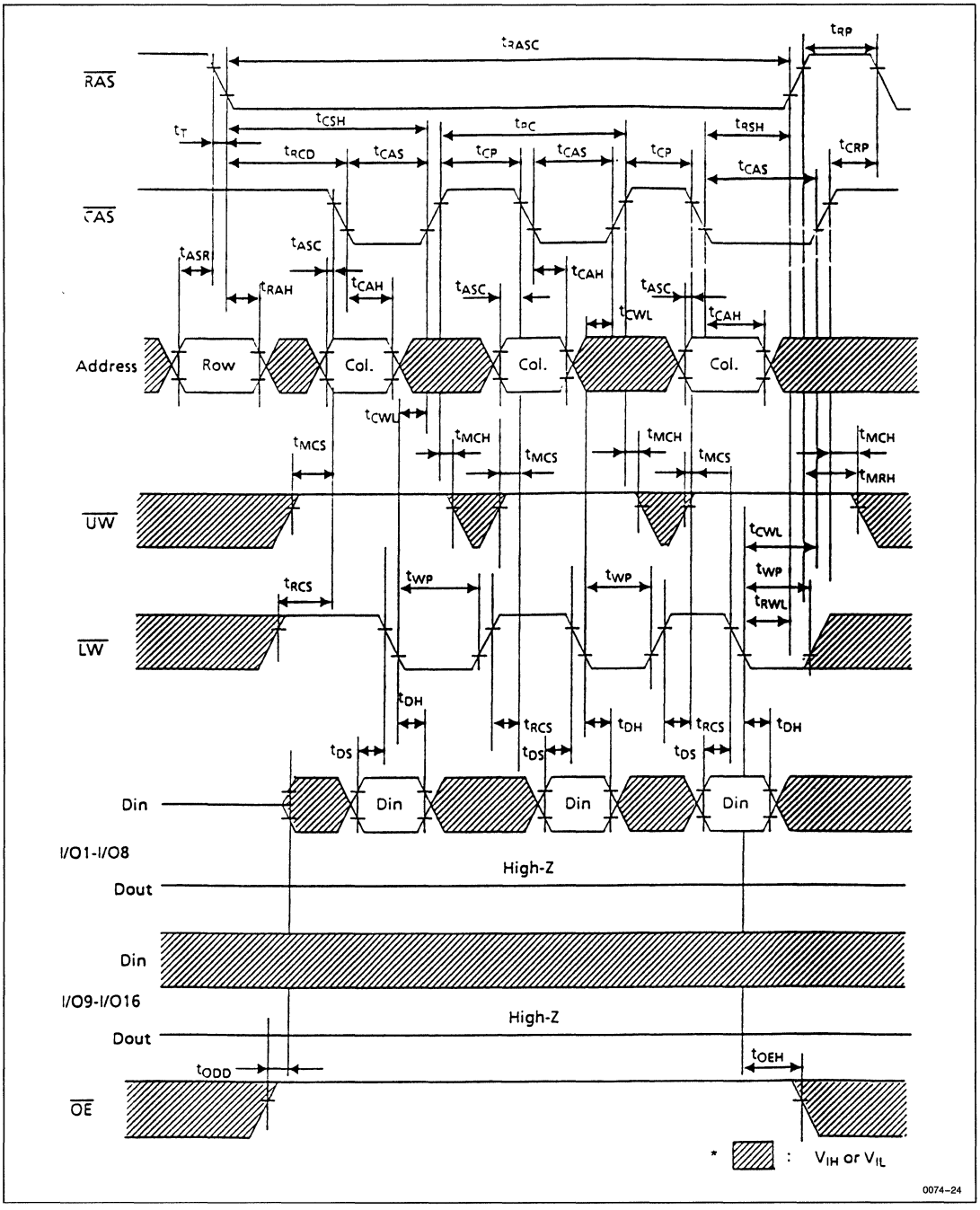
• **Fast Page Mode Delayed Write Cycle**



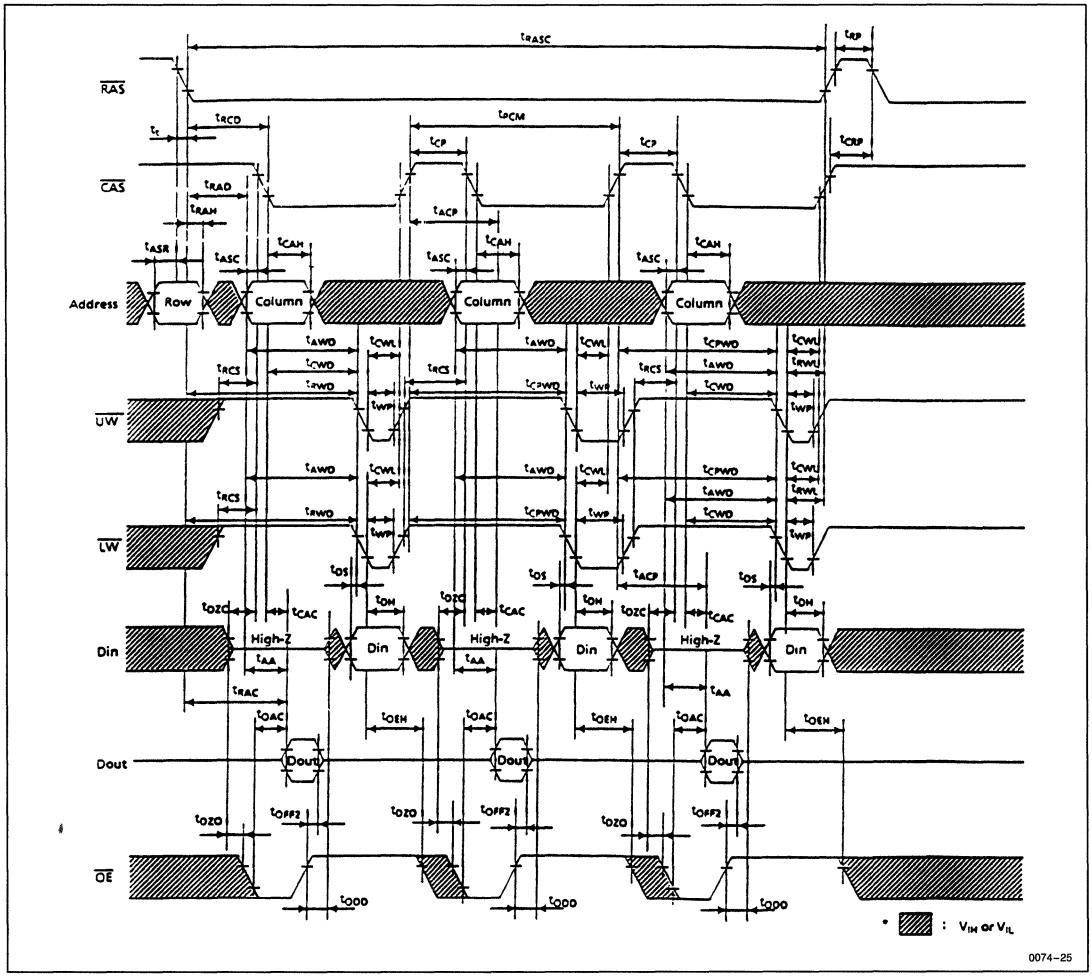
• Fast Page Mode Upper Byte Delayed Write Cycle



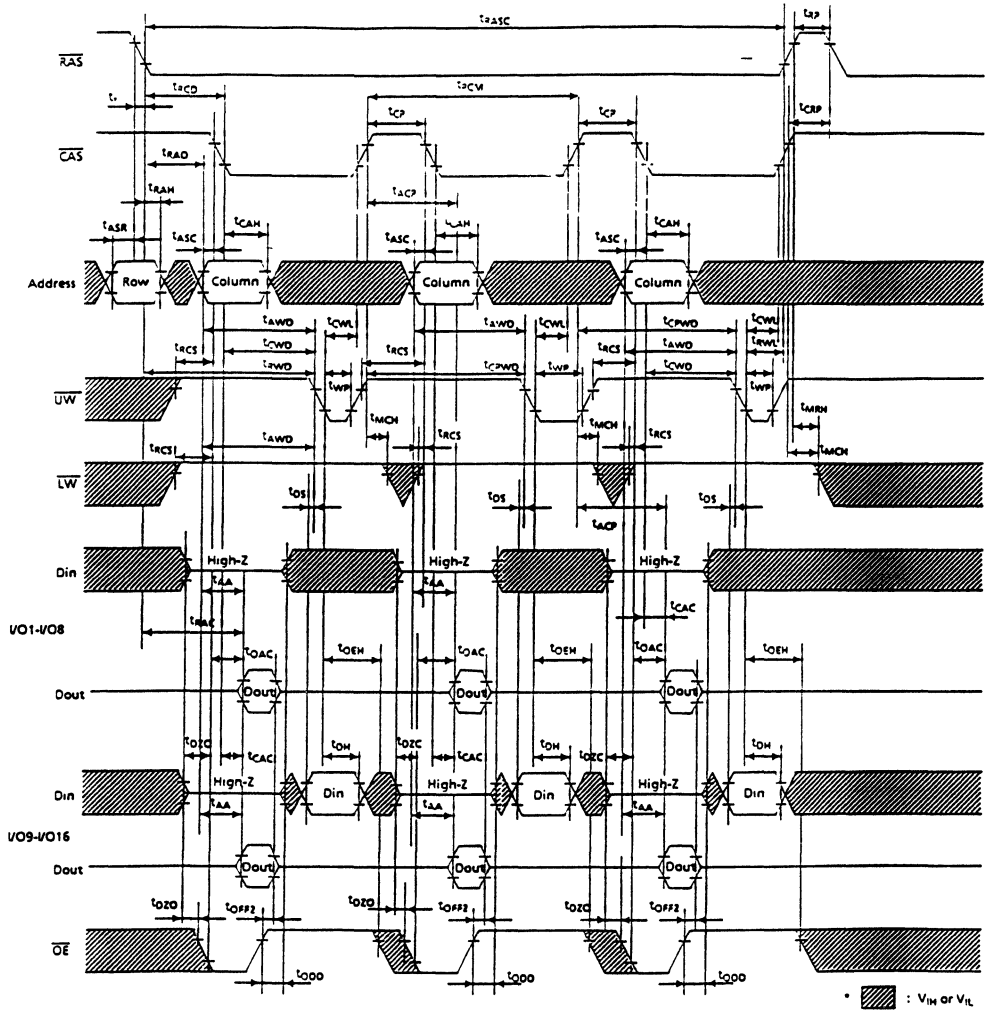
• **Fast Page Mode Lower Byte Delayed Write Cycle**



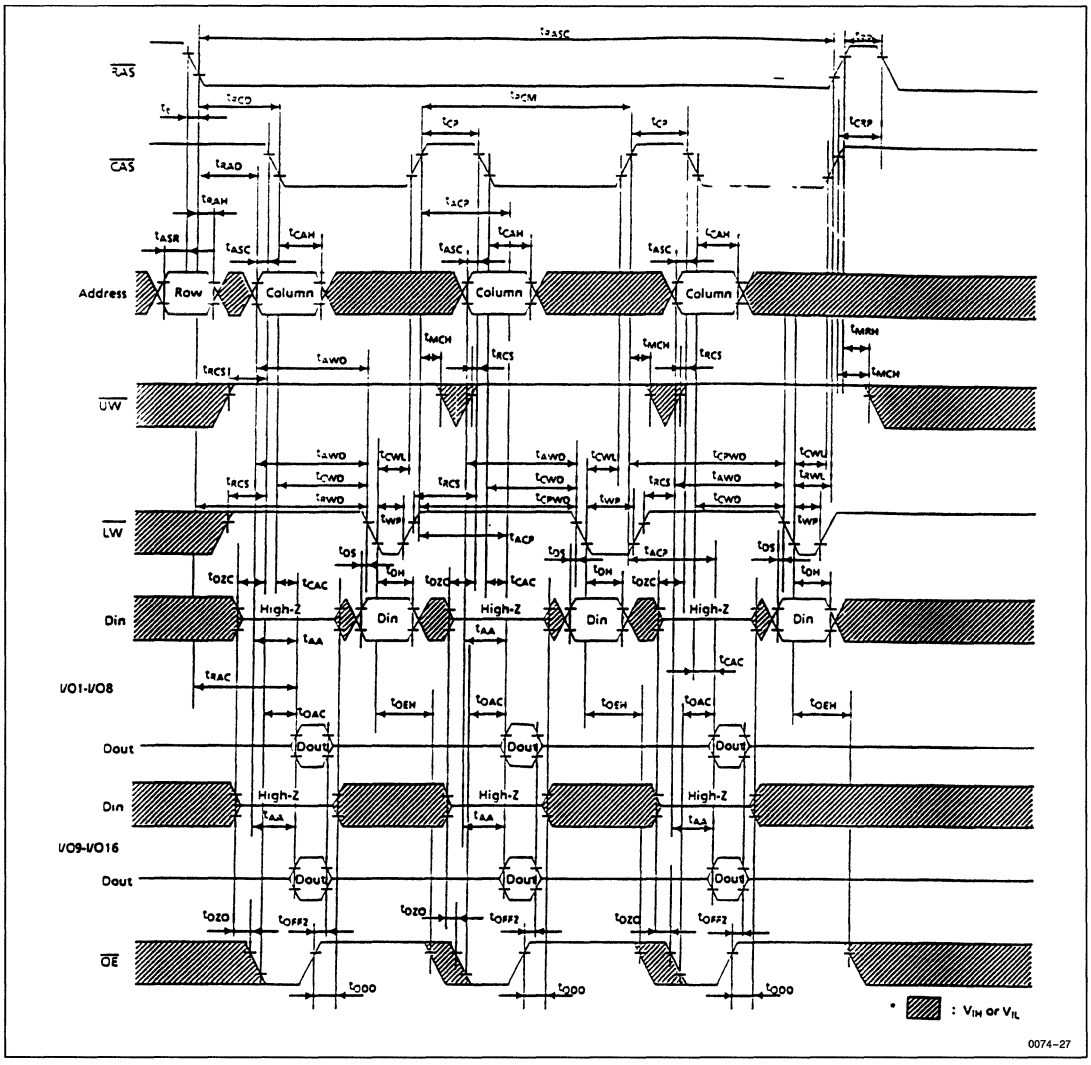
• Fast Page Mode Read-Modify-Write Cycle



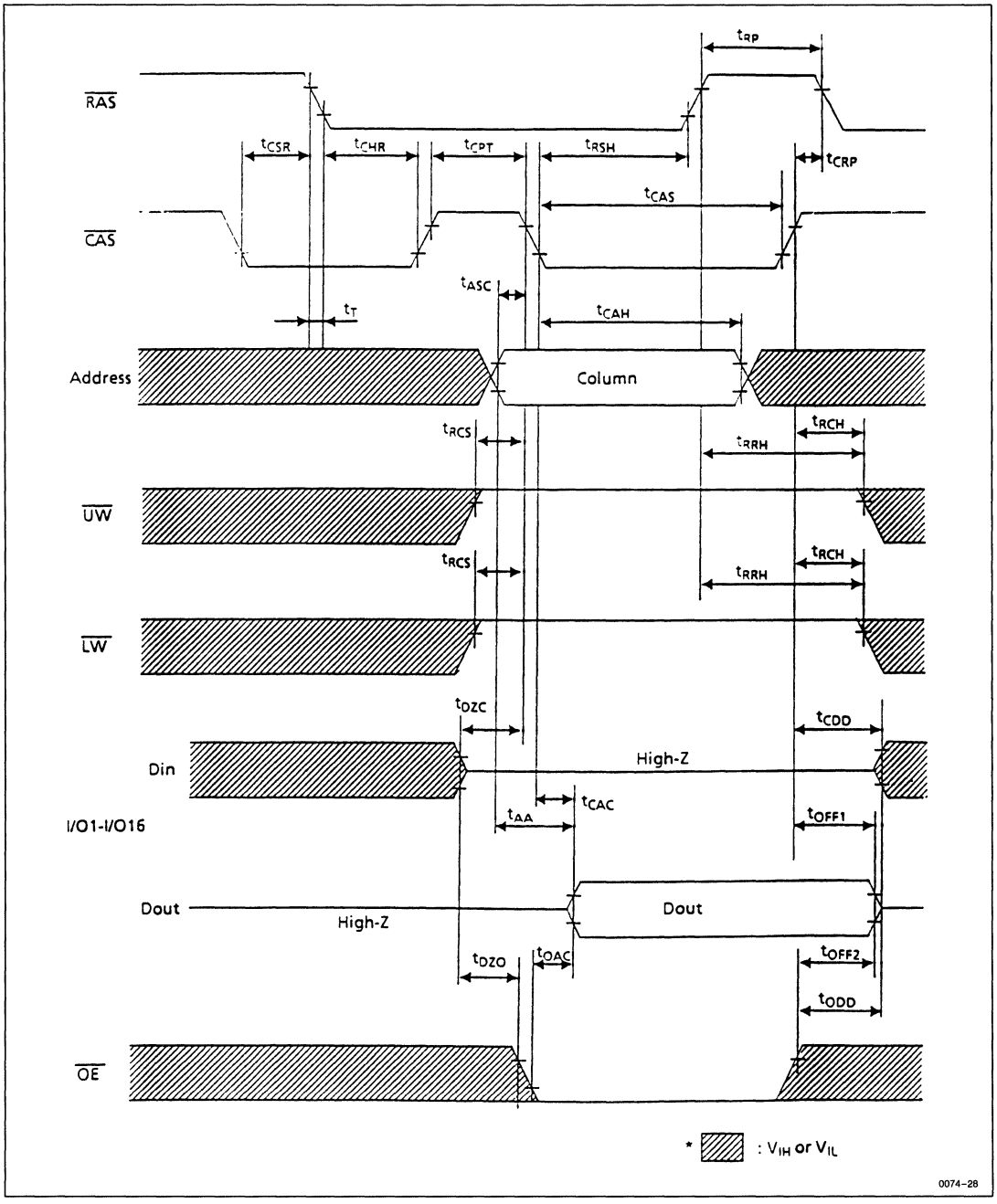
• **Fast Page Mode Read-Modify-Upper-Byte-Write Cycle**



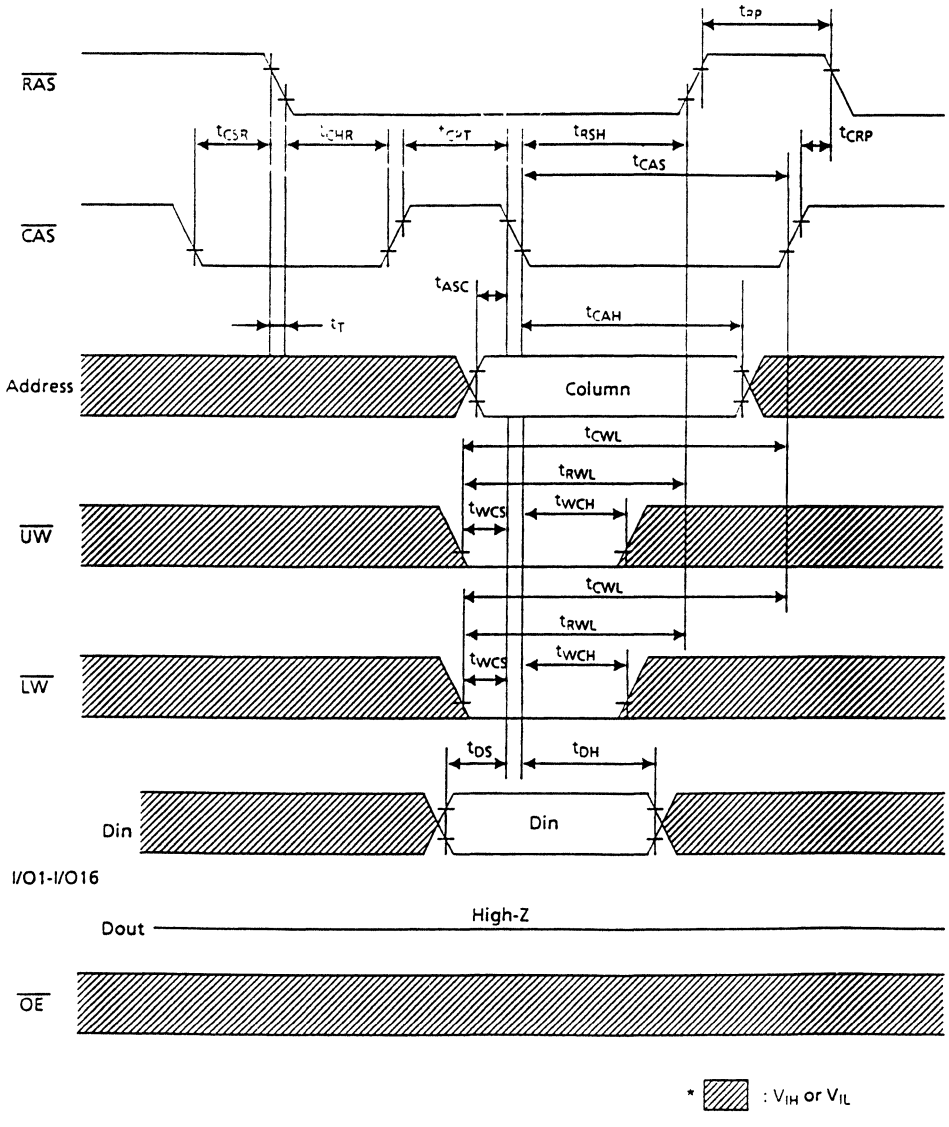
• Fast Page Mode Read-Modify-Lower-Byte-Write Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM511664/L Series — Preliminary

65,536-Word x 16-Bit Dynamic RAM

■ DESCRIPTION

The Hitachi HM511664/HM511664L are CMOS dynamic RAM organized as 65,536-word x 16-bit. HM511664/HM511664L have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM511664/HM511664L offer Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM511664/HM511664L to be packaged in standard 400 mil 40-pin plastic SOJ, standard 475 mil 40-pin plastic ZIP.

■ FEATURES

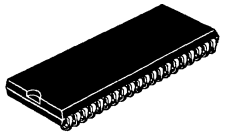
- Single 5V (±10%)
- High Speed
  - Access Time .....80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode.....633 mW/495 mW (max)
  - Standby Mode (TTL) .....11 mW (max)
  - Standby Mode (CMOS) .....5.5 mW (max)
  - ....1.1 mW (max) (L-Version)
- Fast Page Mode Capability
- Byte Write Capability
- 256 Refresh Cycles .....(4 ms)
  .....(32 ms) (L-Version)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Battery Back-up Operation
  - HM511664L Series (L-Version)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_7	Address Input Refresh Address Input
I/O_1–I/O_{16}	Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{UW}$	Read/Upper Byte Write Enable
$\overline{LW}$	Read/Lower Byte Write Enable
$\overline{OE}$	Output Enable
V_{CC}[1]	Power (+5V)
V_{SS}[2]	Ground
NC	No Connection

Notes: 1. This device has 3 V_{CC} pins (SOJ: 1, 11, 20 pin/ZIP: 13, 21, 30 pin). All V_{CC} pins must be connected with the same power-supply wiring on the memory board.
2. This device has 3 V_{SS} pins (SOJ: 21, 30, 40 pin/ZIP: 10, 33, 40 pin). All V_{SS} pins must be connected with the same ground wiring on the memory board.

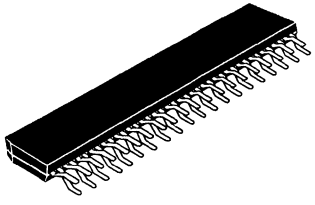
HM511664JP Series



3DCP40D

(CP-40D)

HM511664ZP Series

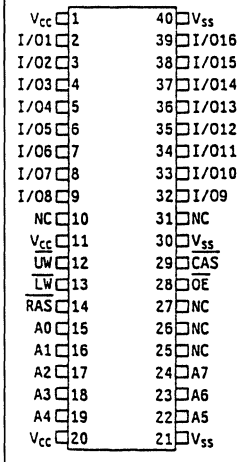


3DZP40

(ZP-40)

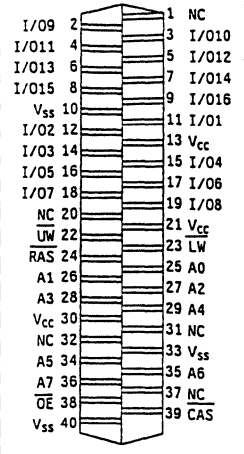
■ PIN OUT

HM511664JP Series



(Top View)

HM511664ZP Series

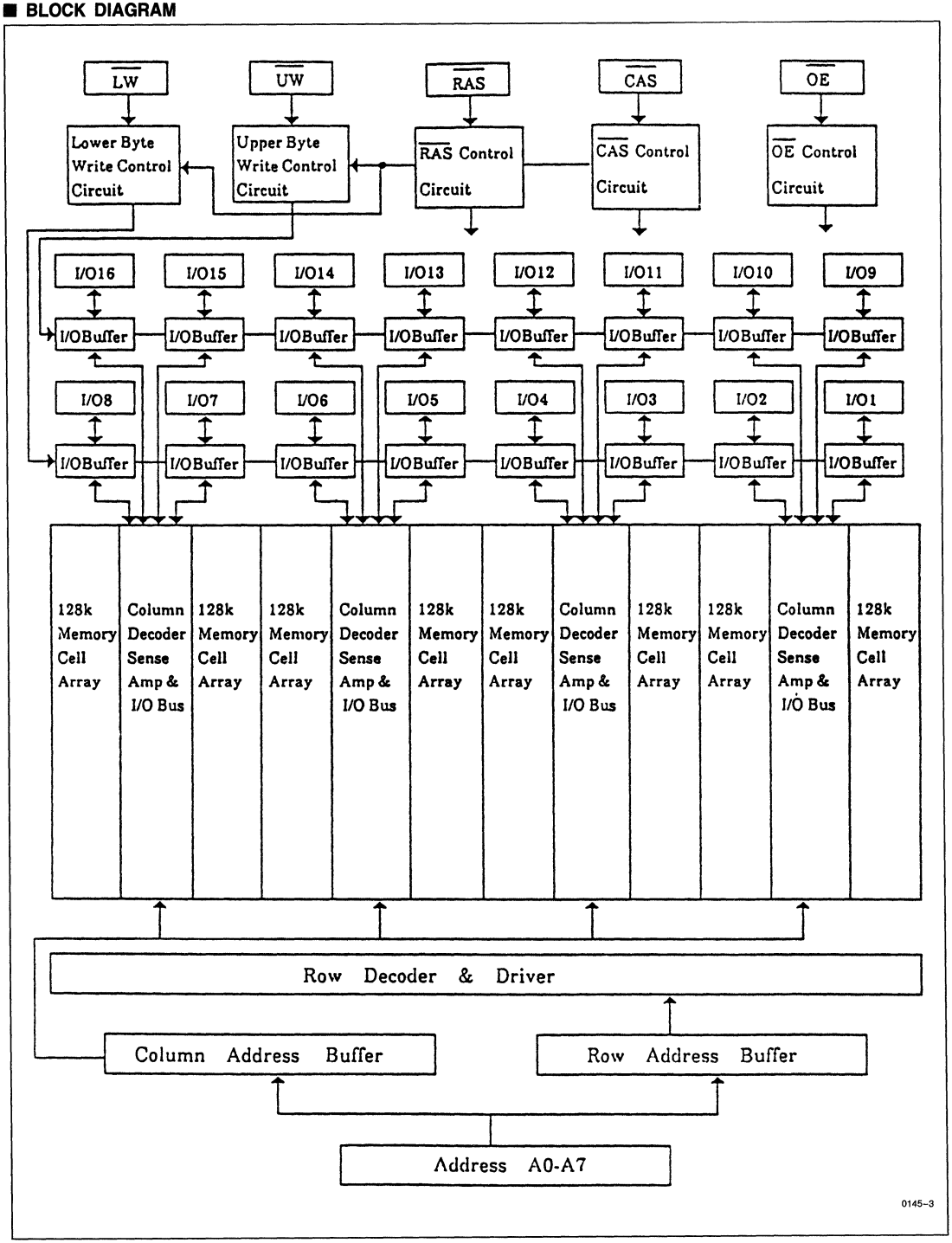


(Bottom View)

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM511664JP-8 HM511664JP-10	80 ns 100 ns	400 mil 40-pin Plastic SOJ (CP-40D)
HM511664LJ-8 HM511664LJ-10	80 ns 100 ns	
HM511664ZP-8 HM511664ZP-10	80 ns 100 ns	475 mil 40-pin Plastic ZIP (ZP-40)
HM511664LZ-8 HM511664LZ-10	80 ns 100 ns	

■ BLOCK DIAGRAM



■ TRUTH TABLE

Inputs					I/O		Operation
$\overline{RAS}$	$\overline{CAS}$	$\overline{LW}$	$\overline{UW}$	$\overline{OE}$	I/O_1–I/O_8	I/O_9–I/O_{16}	
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	D_{out}	D_{out}	Read
L	L	L	H	H	D_{in}	Don't Care	Lower Byte Write
L	L	H	L	H	Don't Care	D_{in}	Upper Byte Write
L	L	L	L	H	D_{in}	D_{in}	Word Write
L	L	L	L	H	High-Z	High-Z	

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	0.8	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/Oi Pin)	V_{IL}	−0.5	—	0.8	V	1, 2
	(Others)	V_{IL}	−1.0	—	0.8	V	1, 2

Notes: 1. All voltage referenced to V_{SS}.
2. The device will withstand undershoots to the −2V level with a maximum pulse width of 20 ns at the −1.5V level. (See figure 1.)

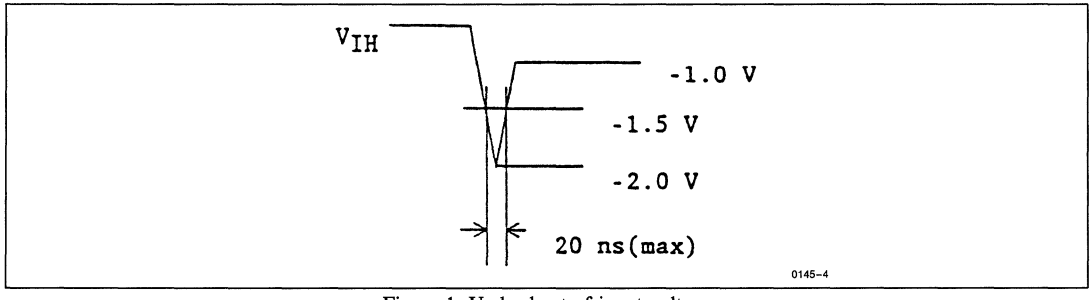


Figure 1. Undershoot of input voltage

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM511664-8 HM511664L-8		HM511664-10 HM511664L-10		Unit	Test Conditions	Note
		Min	Max	Min	Max			
Operating Current	I_{CC1}	—	115	—	90	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	2				mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	4
		1				mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	4
(L-Version) Standby Current	I_{CC2}	—	200	—	200	μA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, $\overline{WE}$, $\overline{OE}$, Address and D_{in} = V_{IH} or V_{IL} D_{out} = High-Z	5
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	115	—	90	mA	t_{RC} = Min	2
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	115	—	90	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	100	—	85	mA	t_{PC} = Min	1, 3
(L-Version) Battery Back-up Operating Current (Standby with CBR Refresh)	I_{CC10}	—	300	—	300	μA	t_{RC} = 125 μs $t_{\overline{RAS}}$ ≤ 1 μs $\overline{WE}$ = V_{IH}, $\overline{CAS}$ = V_{IL} $\overline{OE}$, Address and D_{in} = V_{IH} or V_{IL} D_{out} = High-Z	5
Input Leakage Current	I_{LI}	−10	10	−10	10	μA	0V ≤ V_{in} ≤ 6.5V	
Output Leakage Current	I_{LO}	−10	10	−10	10	μA	0V ≤ V_{out} ≤ 5.5V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −2.5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	V	Low I_{out} = 2.1 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. Clock voltages ($\overline{RAS}$ and $\overline{CAS}$) must be applied simultaneously with or prior to applying supply voltage.
5. V_{CC} − 0.2V ≤ V_{IH} ≤ 6.5V and 0V ≤ V_{IL} ≤ 0.2V.

• Capacitance (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 14, 15, 16]

Test Conditions

Input Rise and Fall Times:	5 ns
Input Timing Reference Levels:	0.8V, 2.4V
Output Load:	1 TTL Gate + C_L (50 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM511664-8 HM511664L-8		HM511664-10 HM511664L-10		Unit	Note
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	135	—	170	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	45	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	30	10000	40	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	20	60	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	15	45	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	30	—	40	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	15	—	15	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	ns	
$\overline{CAS}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	4	—	4	ms	
		—	32	—	32	ms	L-Version

Read Cycle

Parameter	Symbol	HM511664-8 HM511664L-8		HM511664-10 HM511664L-10		Unit	Note
		Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	—	40	ns	3, 4, 13
Access Time from Address	t_{AA}	—	45	—	55	ns	3, 5, 13
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	40	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	20	0	20	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	15	0	15	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	20	—	20	—	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	t_{ROH}	10	—	10	—	ns	

Write Cycle

Parameter	Symbol	HM511664-8 HM511664L-8		HM511664-10 HM511664L-10		Unit	Note
		Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM511664-8 HM511664L-8		HM511664-10 HM511664L-10		Unit	Note
		Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	185	—	220	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	105	—	125	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	55	—	65	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	70	—	80	—	ns	10, 13
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	15	—	15	—	ns	

Refresh Cycle

Parameter	Symbol	HM511664-8 HM511664L-8		HM511664-10 HM511664L-10		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time in Normal Mode	t_{CPN}	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM511664-8 HM511664L-8		HM511664-10 HM511664L-10		Unit	Note
		Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	80	100000	100	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	60	ns	3, 13
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	45	—	55	—	ns	
Fast Page Mode Read-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPW}	70	—	80	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	100	—	110	—	ns	

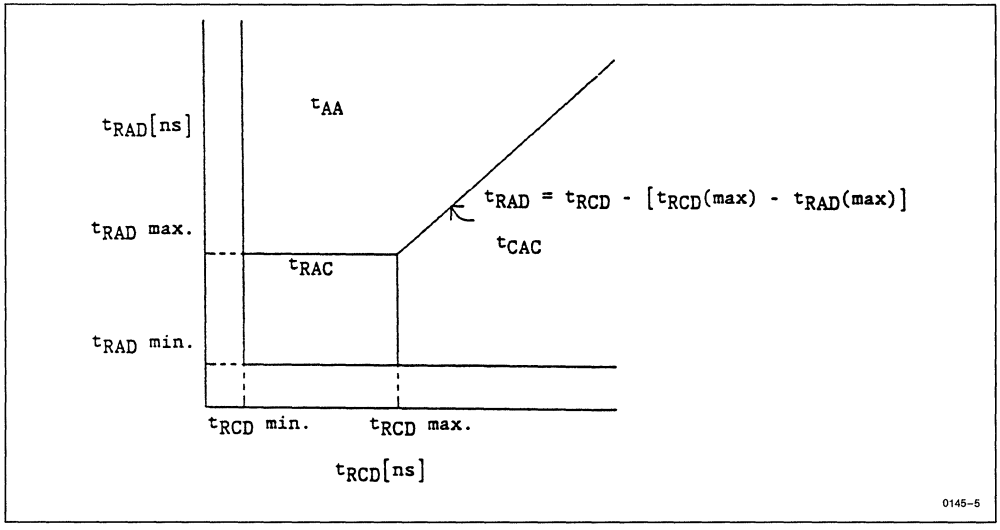
Counter Test Cycle

Parameter	Symbol	HM511664-8 HM511664L-8		HM511664-10 HM511664L-10		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	40	—	ns	

Byte Write Mode

Parameter	Symbol	HM511664-8 HM511664L-8		HM511664-10 HM511664L-10		Unit	Note
		Min	Max	Min	Max		
Masked Write Setup Time	t_{MCS}	0	—	0	—	ns	
Masked Write Hold Time Referenced to $\overline{RAS}$	t_{MRH}	0	—	0	—	ns	
Masked Write Hold Time Referenced to $\overline{CAS}$	t_{MCH}	0	—	0	—	ns	

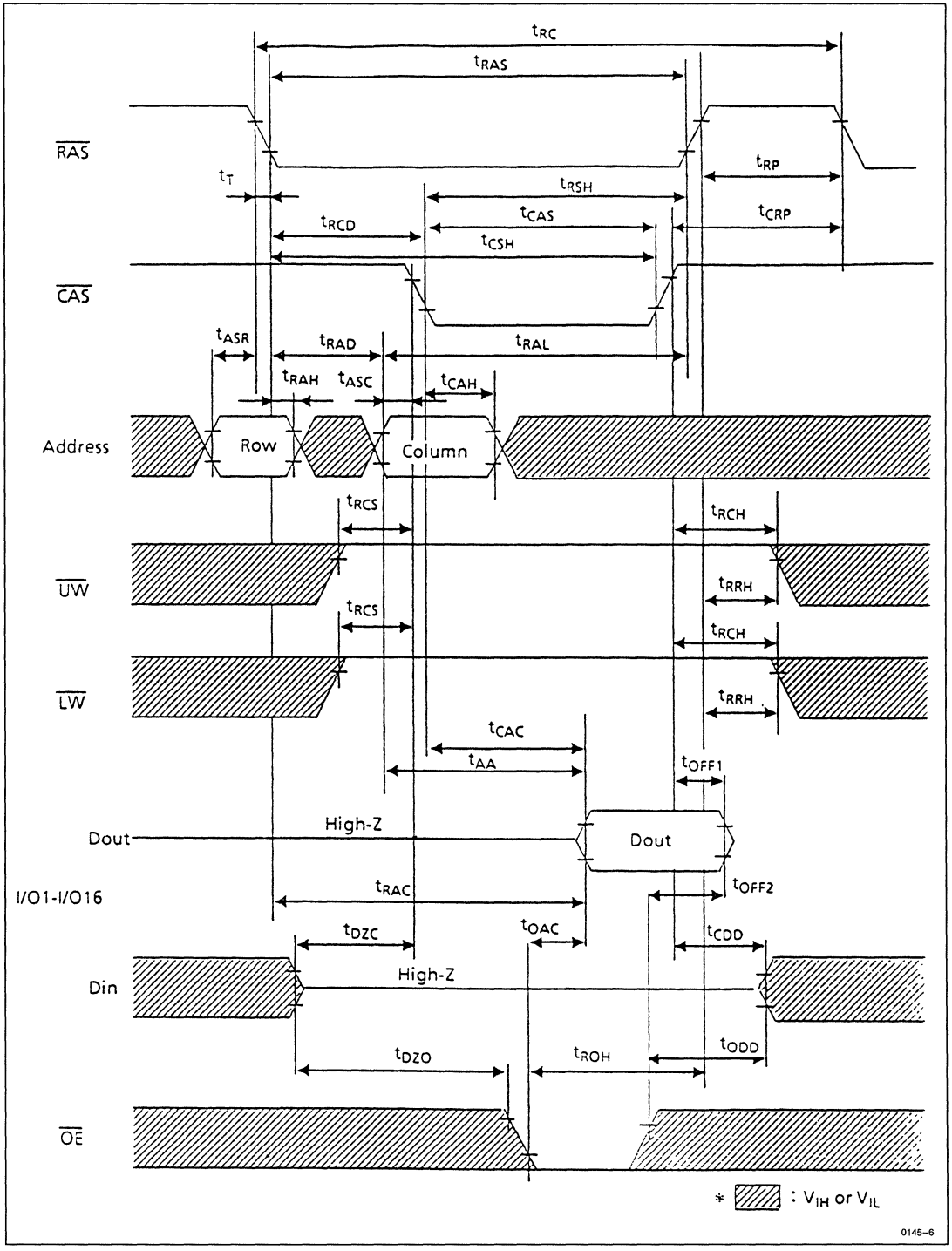
Notes: 1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 1 TTL load and 50 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $(t_{RCD} - t_{RAD}) \geq [t_{RCD}$ (max) $- t_{RAD}$ (max)].
5. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $(t_{RCD} - t_{RAD}) \leq [t_{RCD}$ (max) $- t_{RAD}$ (max)]. t_{RAC}, t_{CAC}, and t_{AA} are determined as follows.



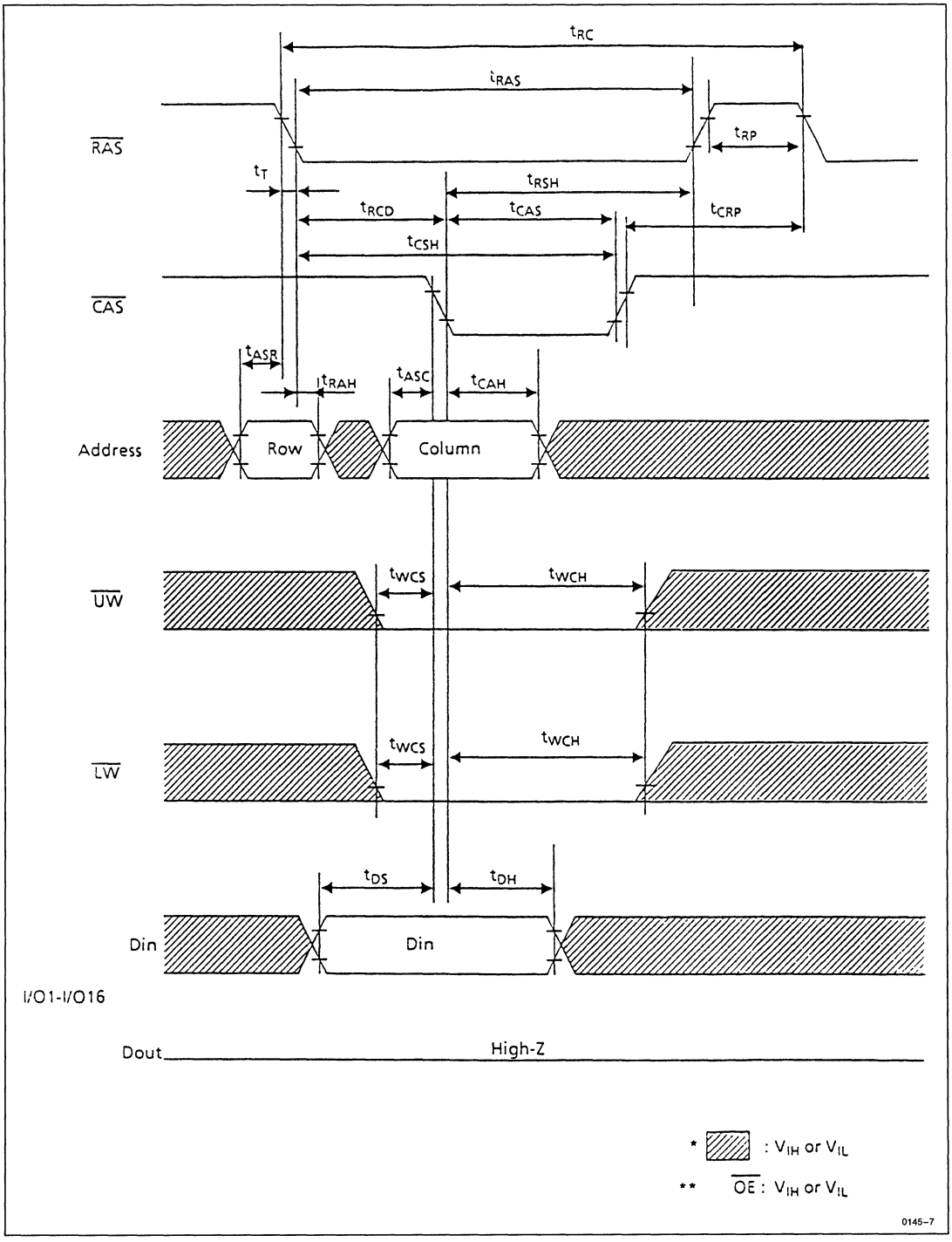
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. When both $\overline{LW}$ and $\overline{UW}$ go low at the same time, all 16-bits data are written into the device. $\overline{LW}$ and $\overline{UW}$ cannot be staggered within the same write cycle.

■ TIMING WAVEFORMS

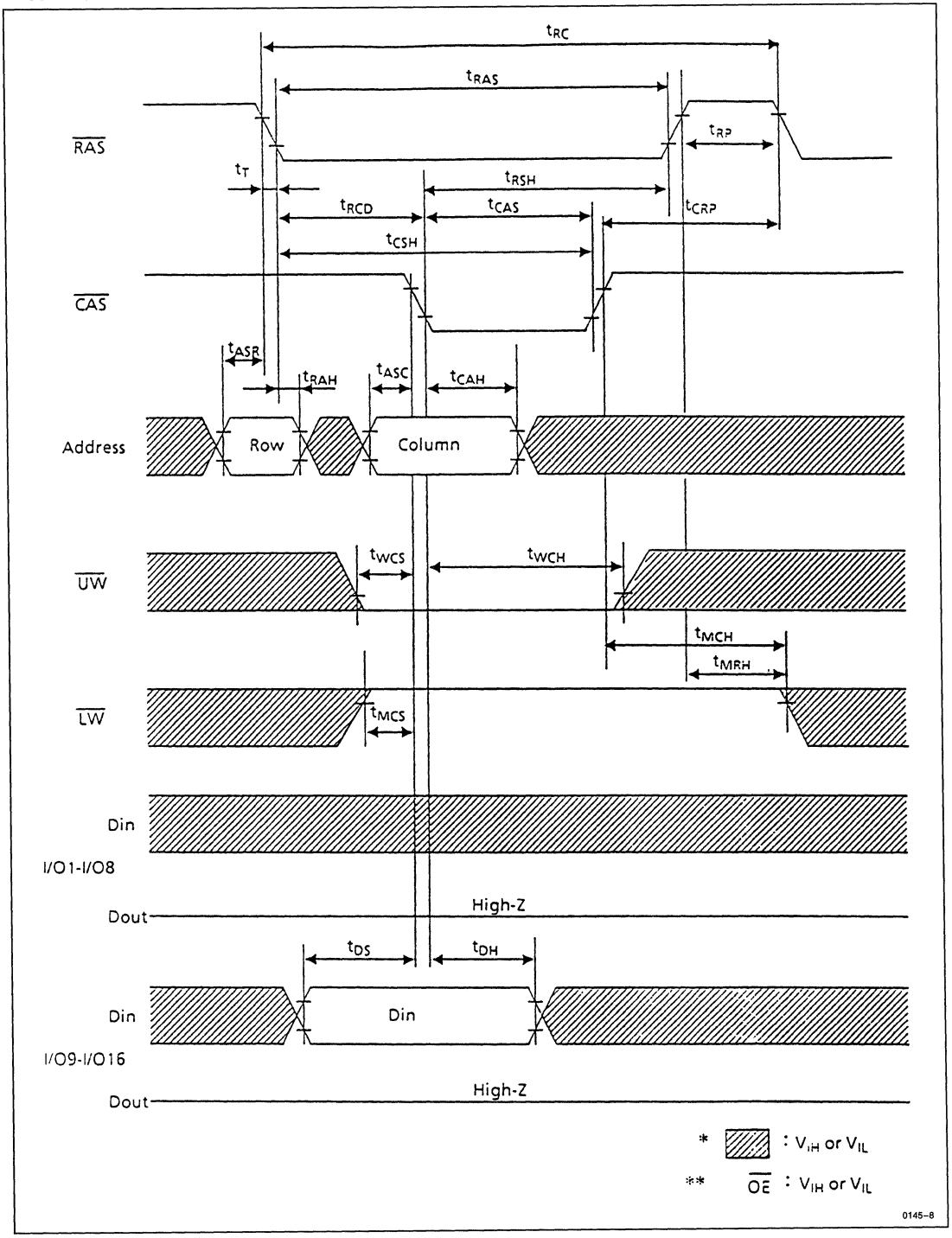
• Read Cycle



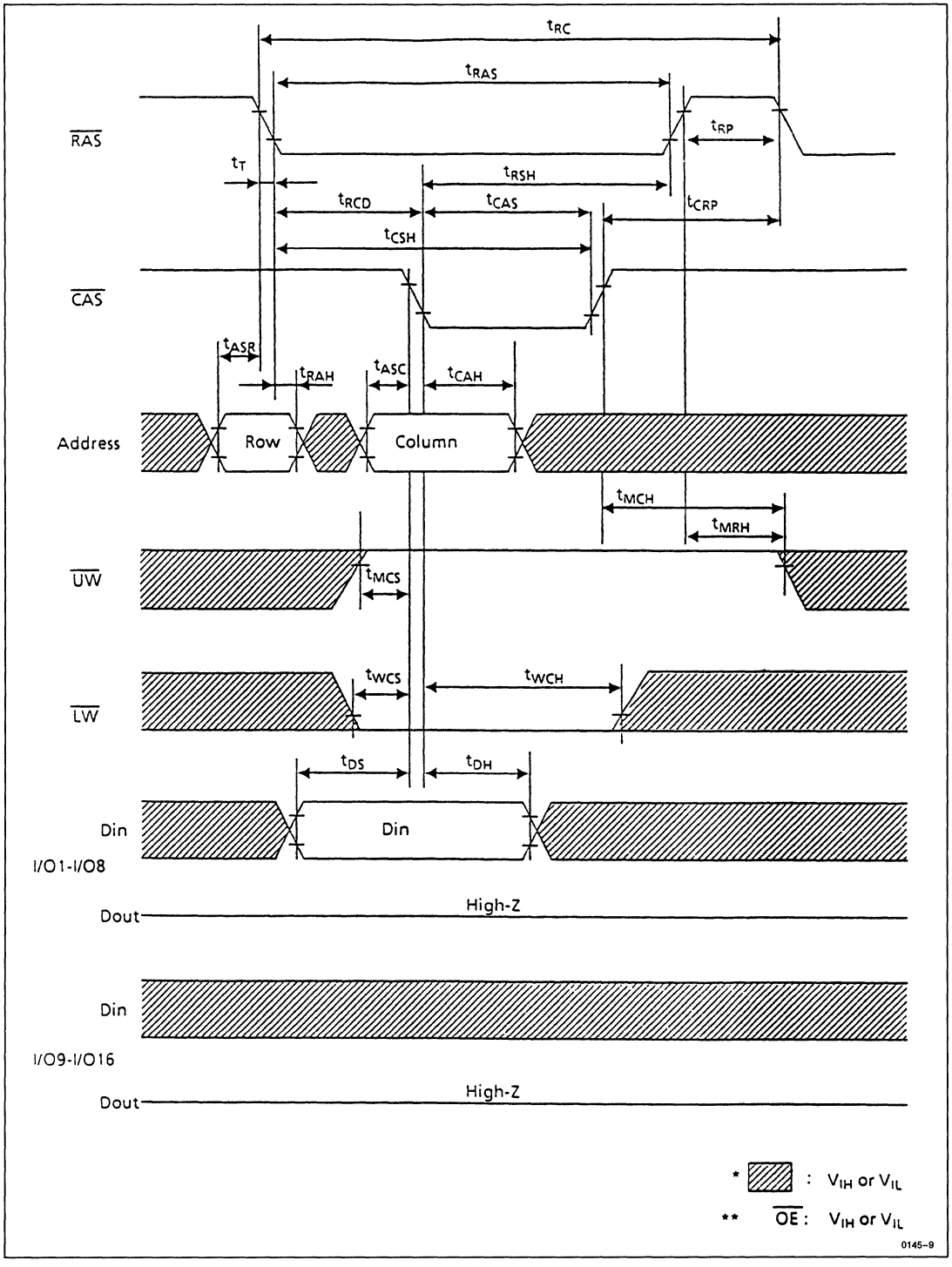
• **Early Write Cycle**



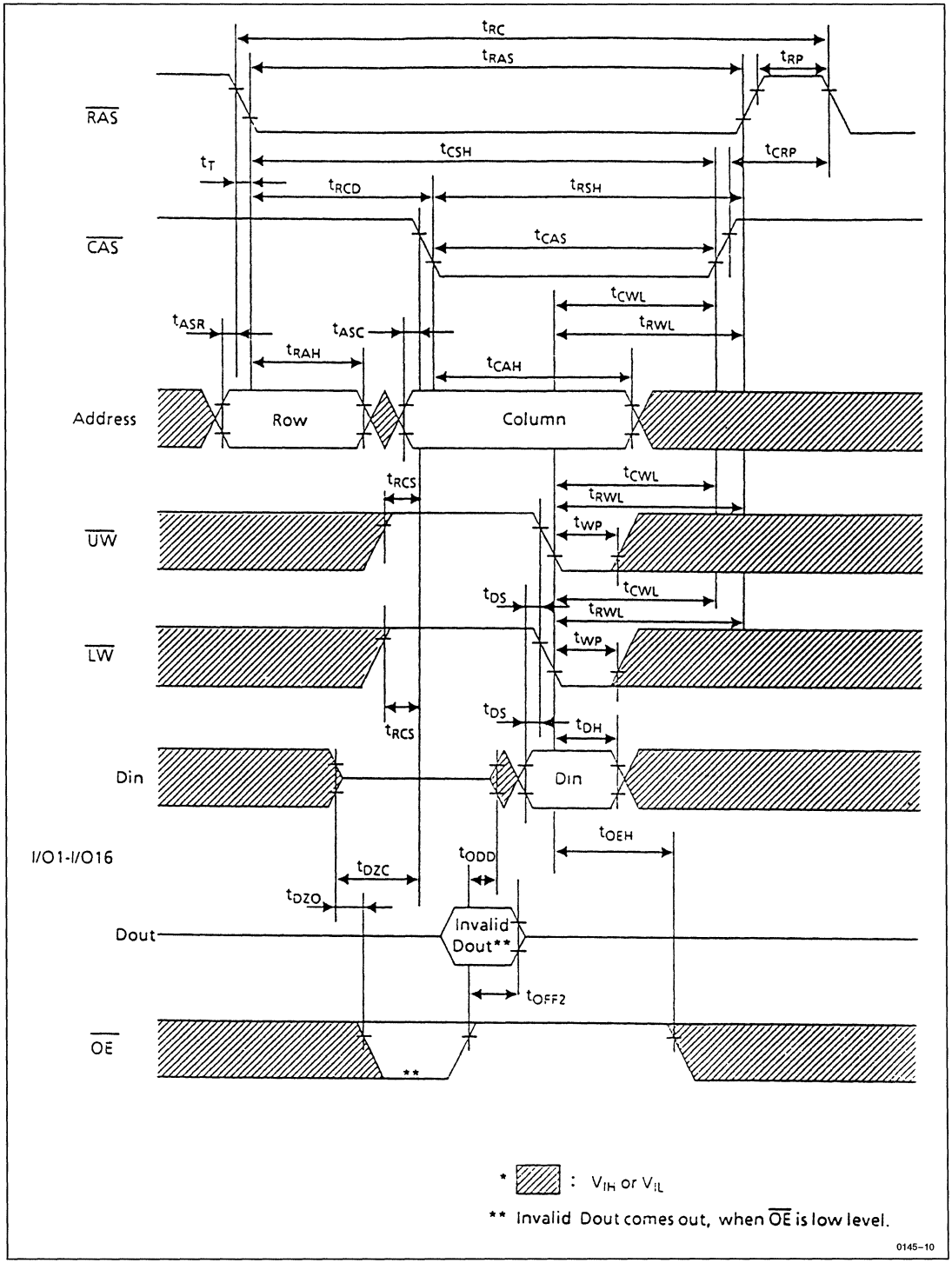
• **Upper Byte Early Write Cycle**



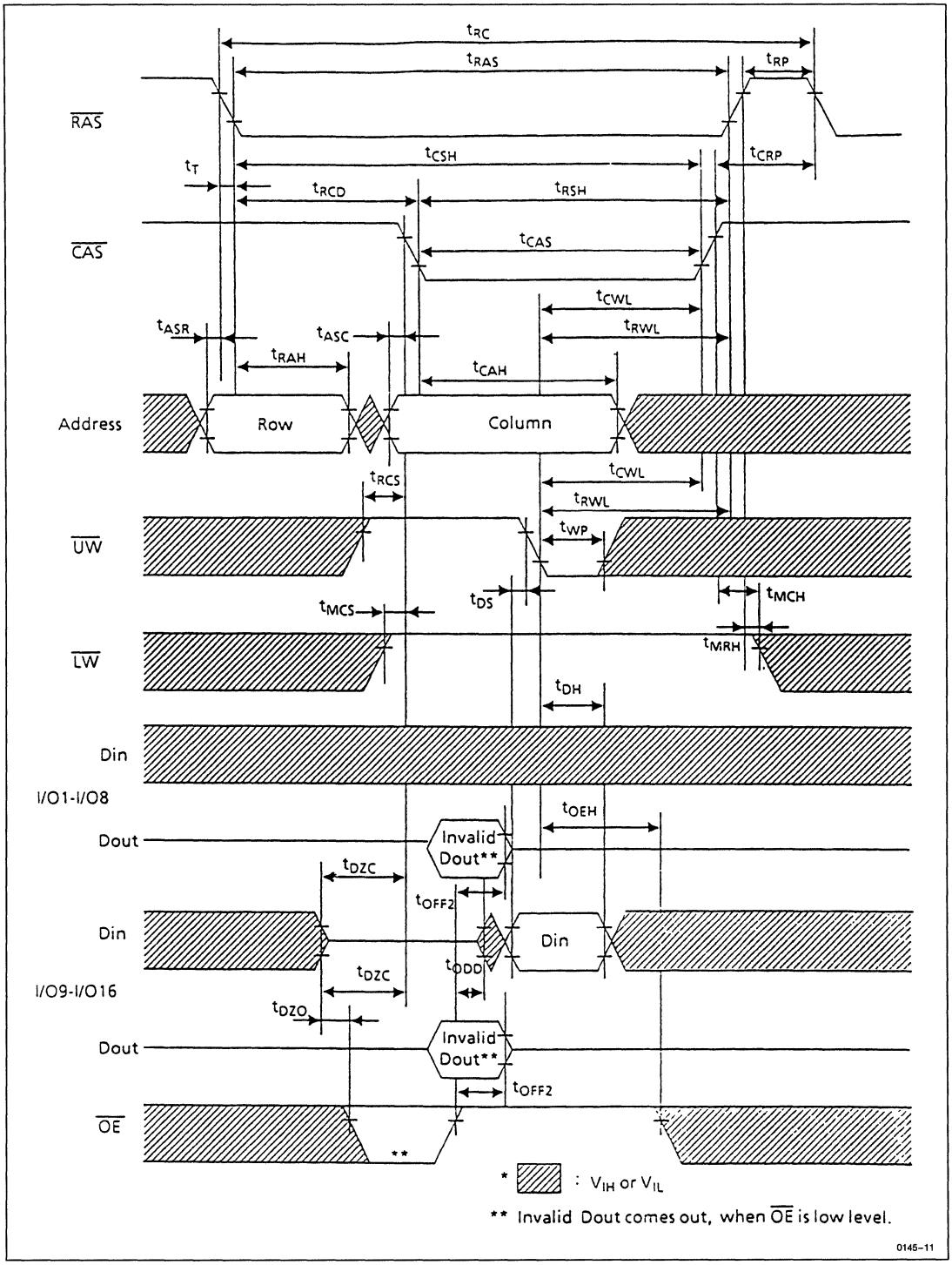
• **Lower Byte Early Write Cycle**



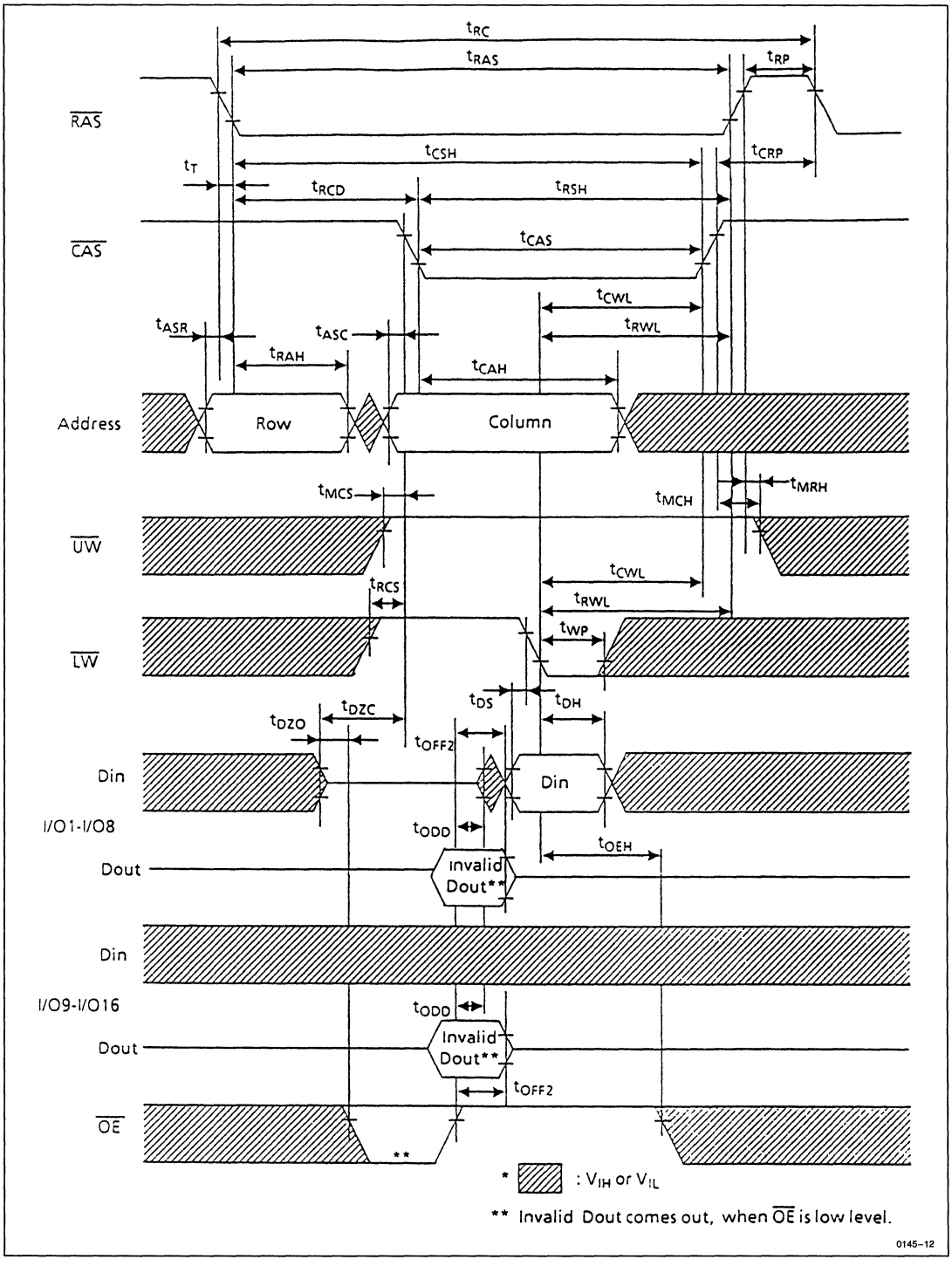
• **Delayed Write Cycle**



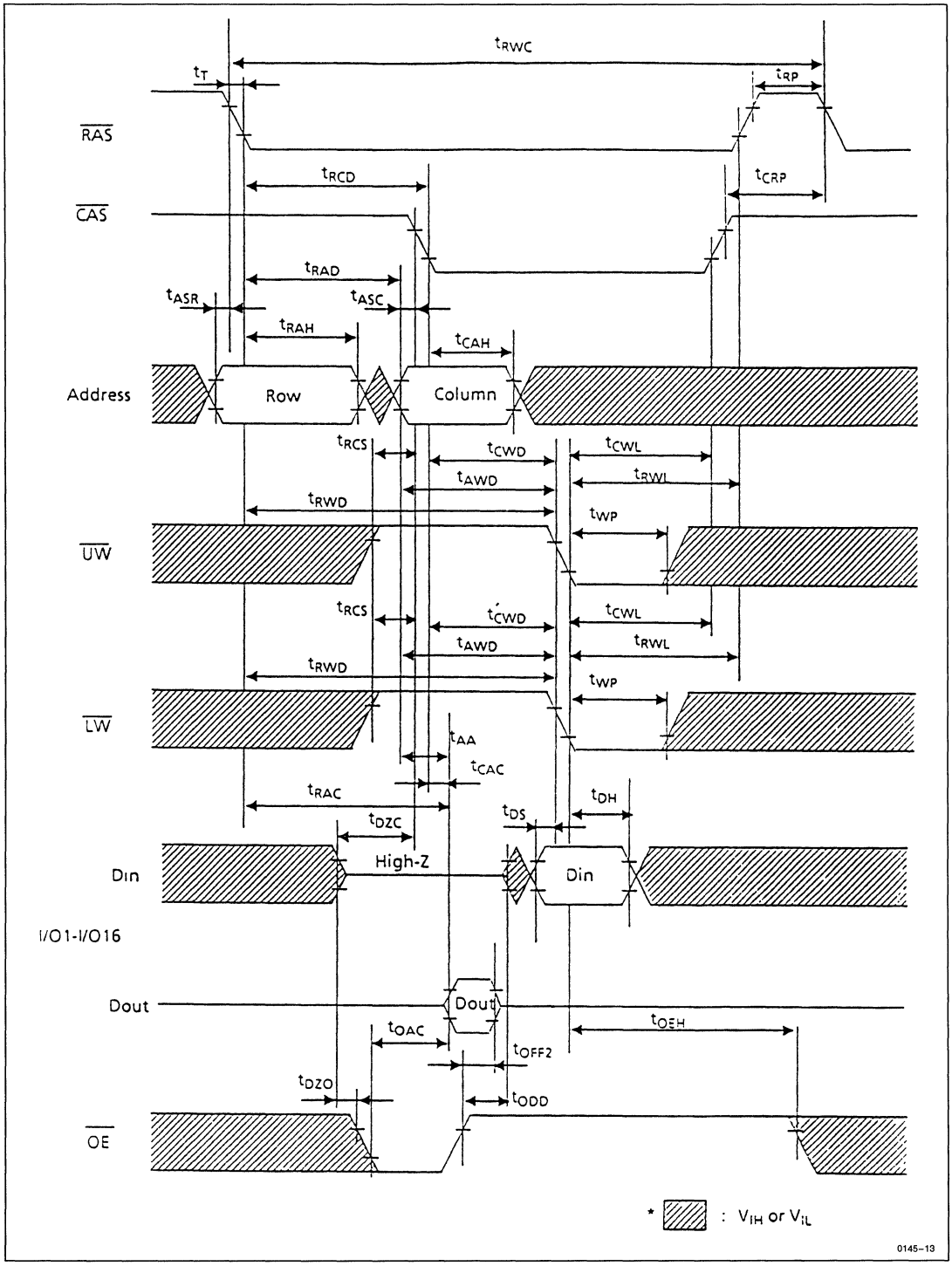
• **Upper Byte Delayed Write Cycle**



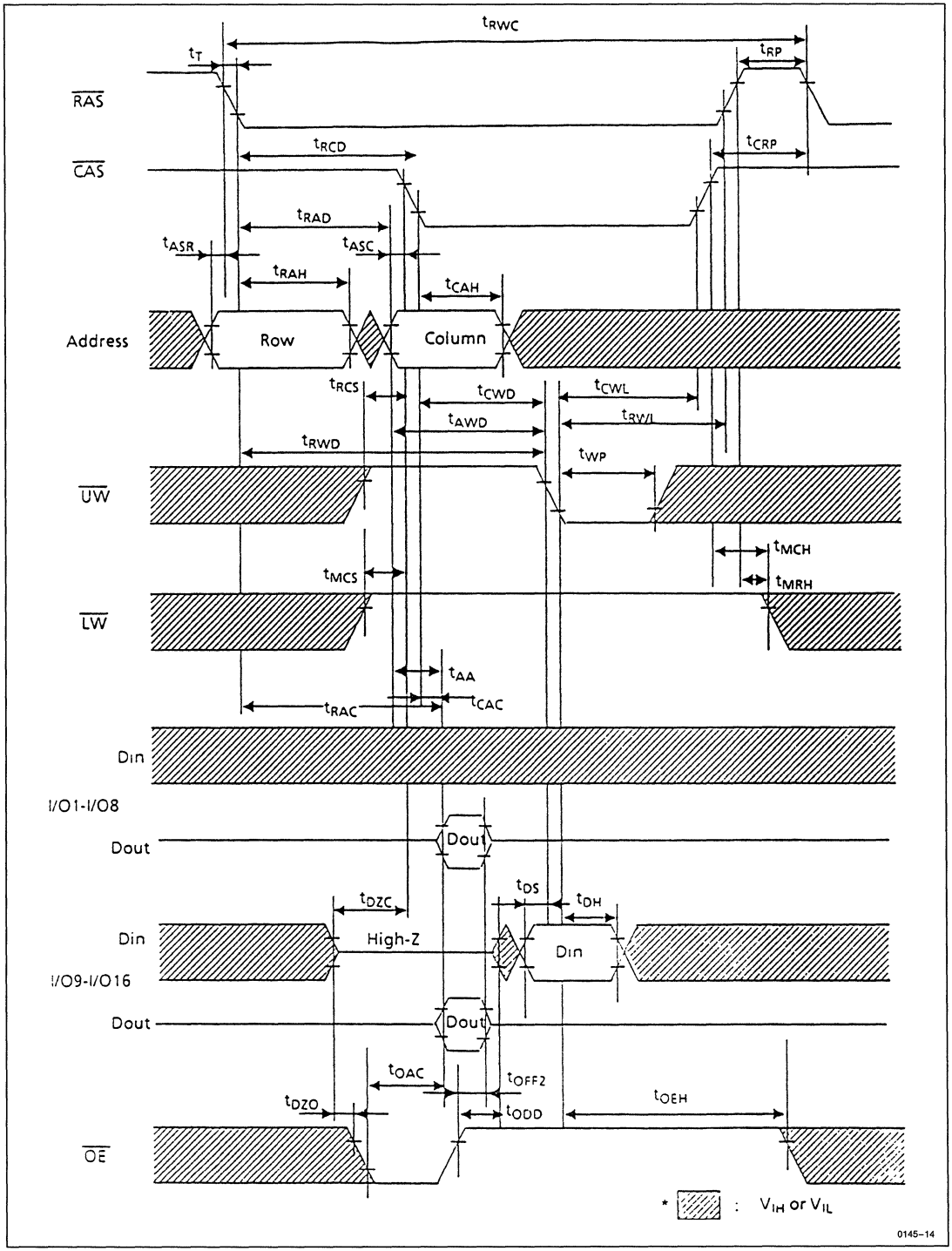
• **Lower Byte Delayed Write Cycle**



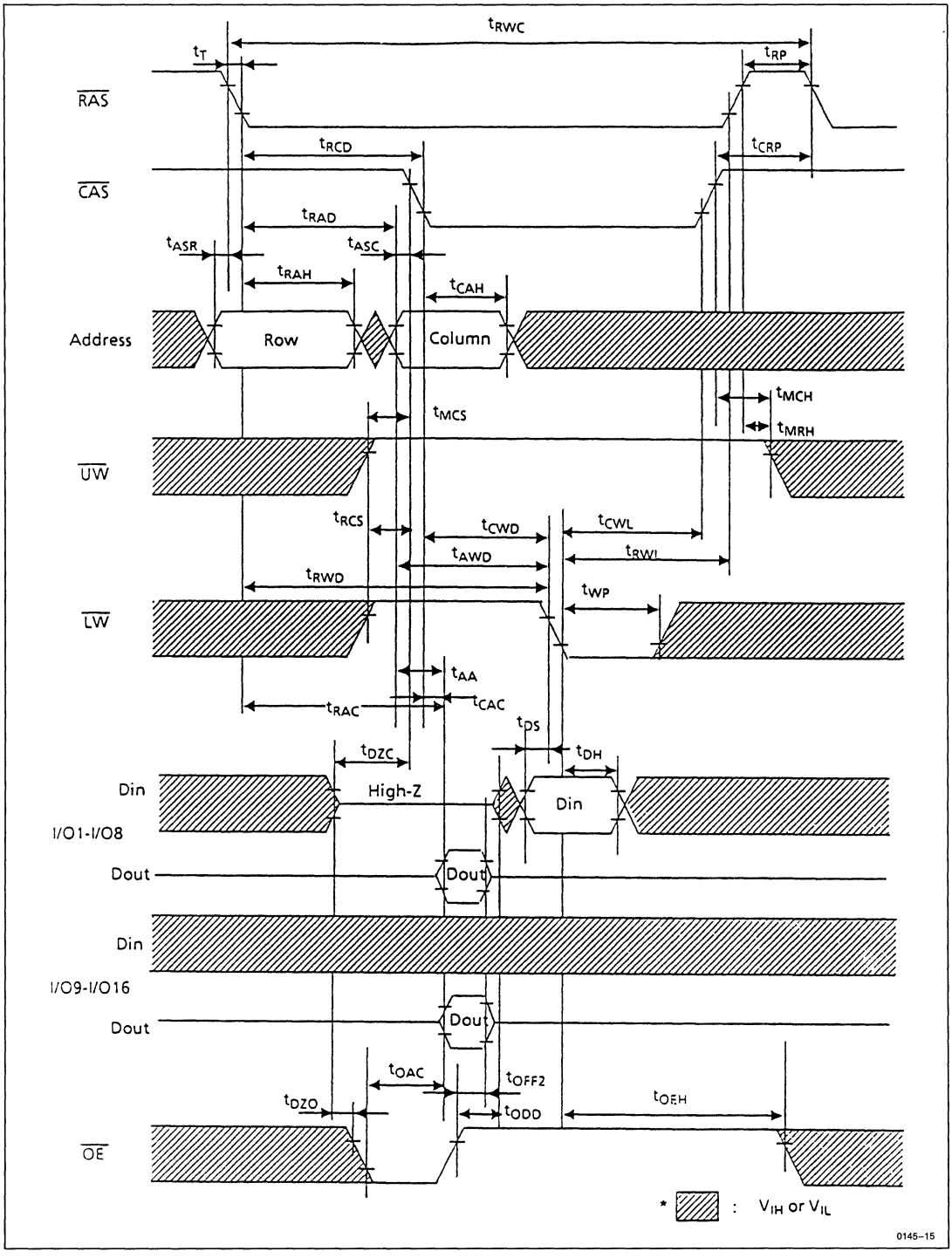
• **Read-Modify-Write Cycle**



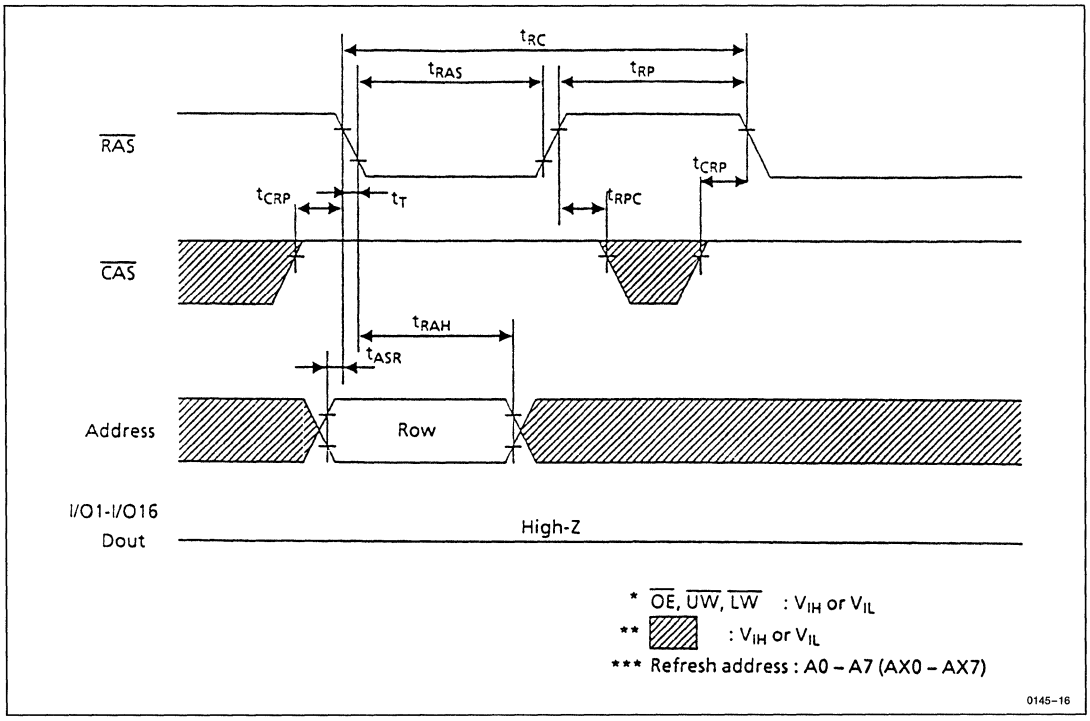
• **Read Modify Upper Byte Write Cycle**



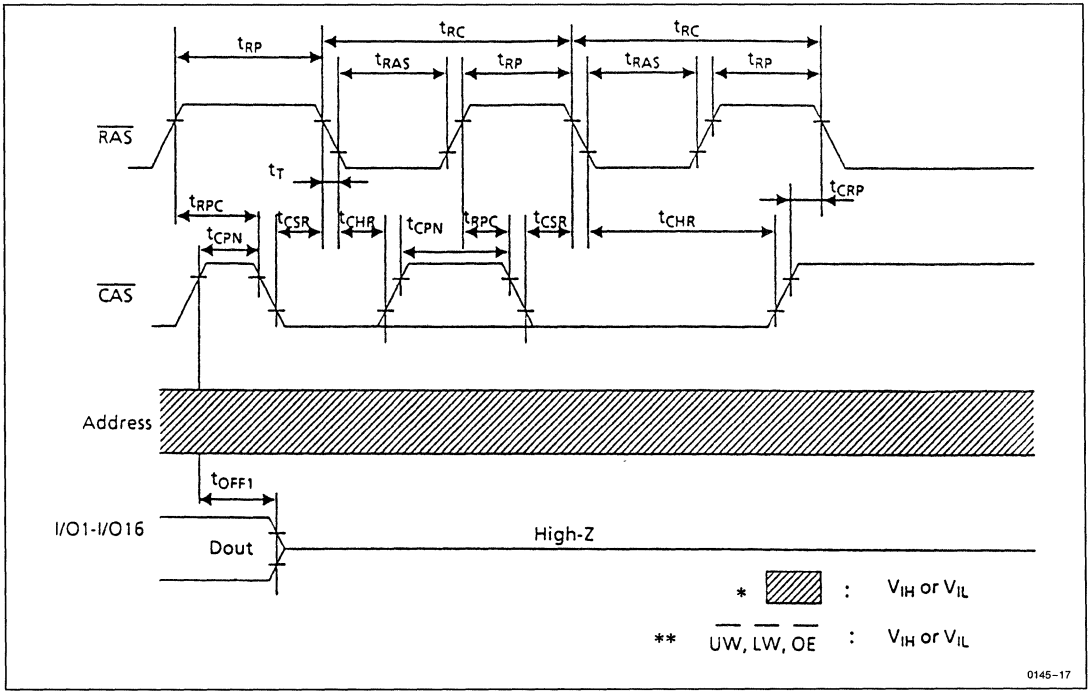
• **Read Modify Lower Byte Write Cycle**



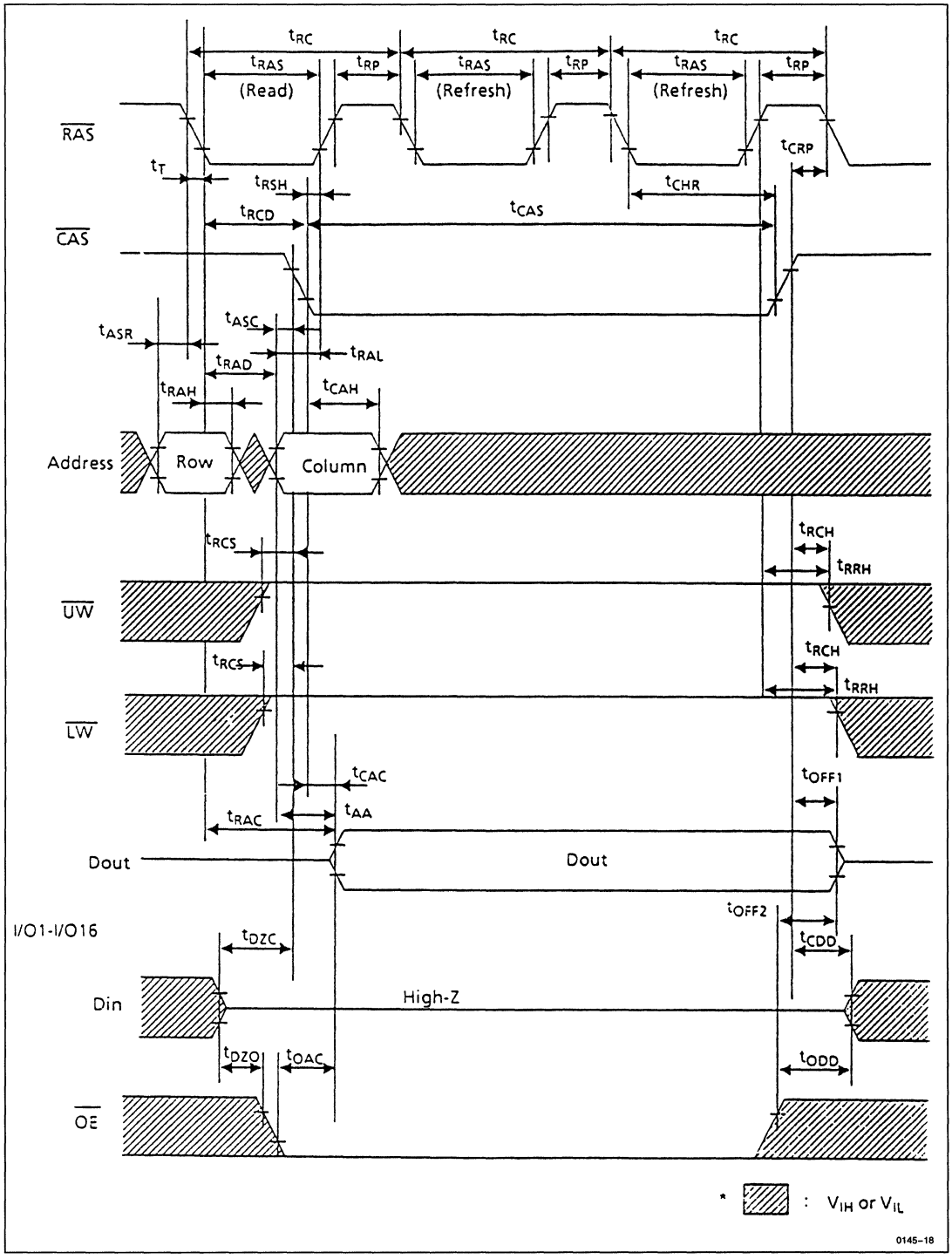
• $\overline{RAS}$ Only Refresh Cycle



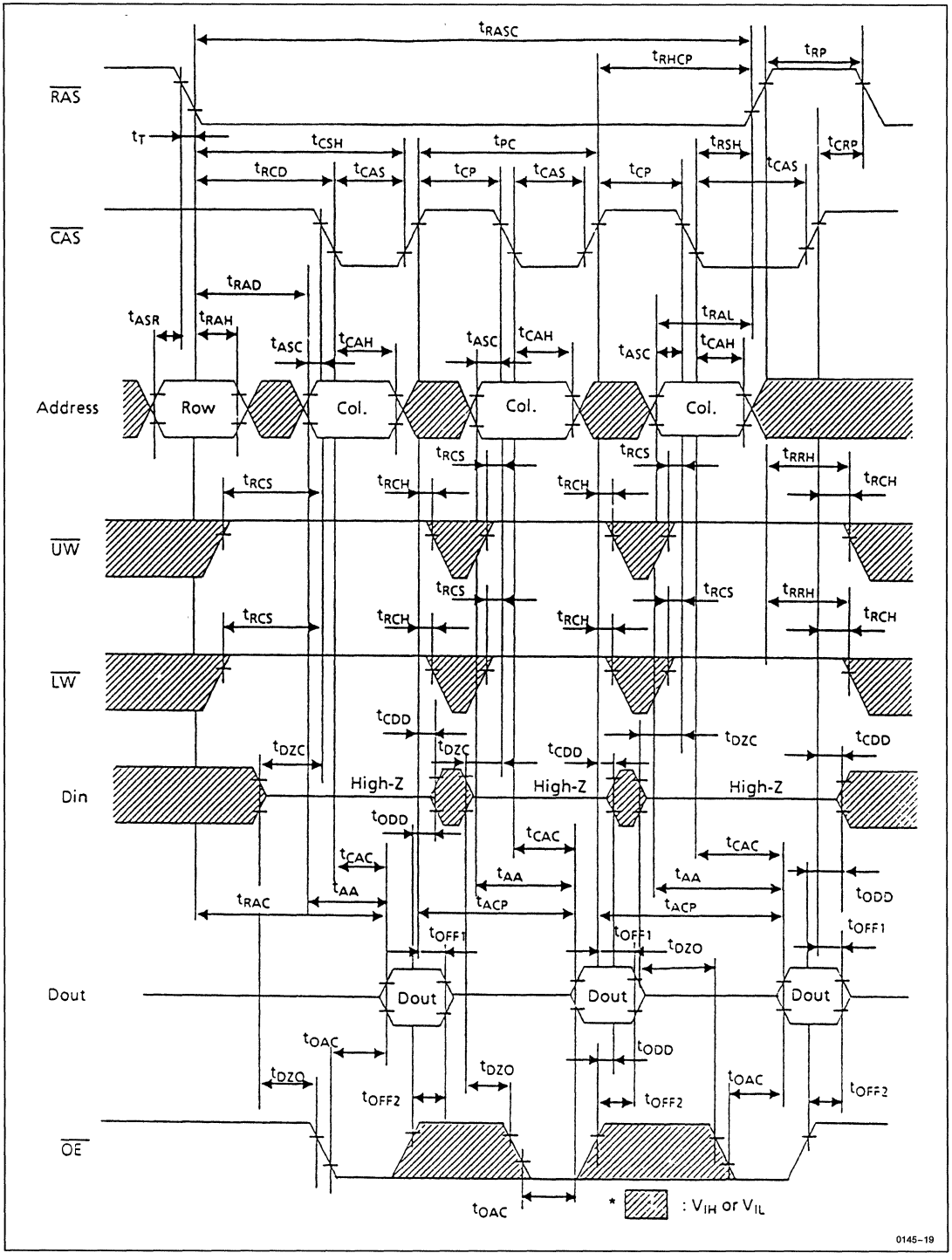
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



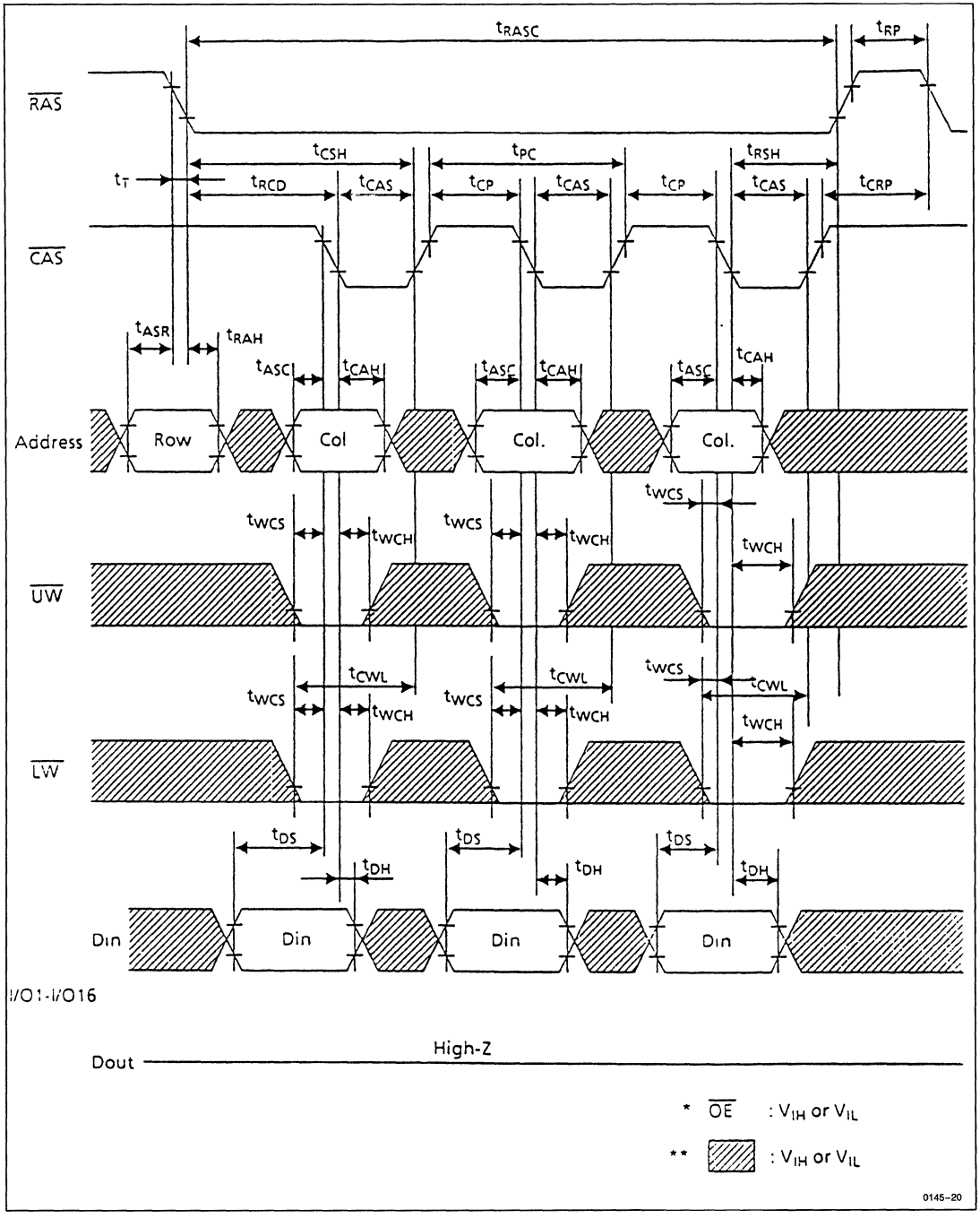
• **Hidden Refresh Cycle**



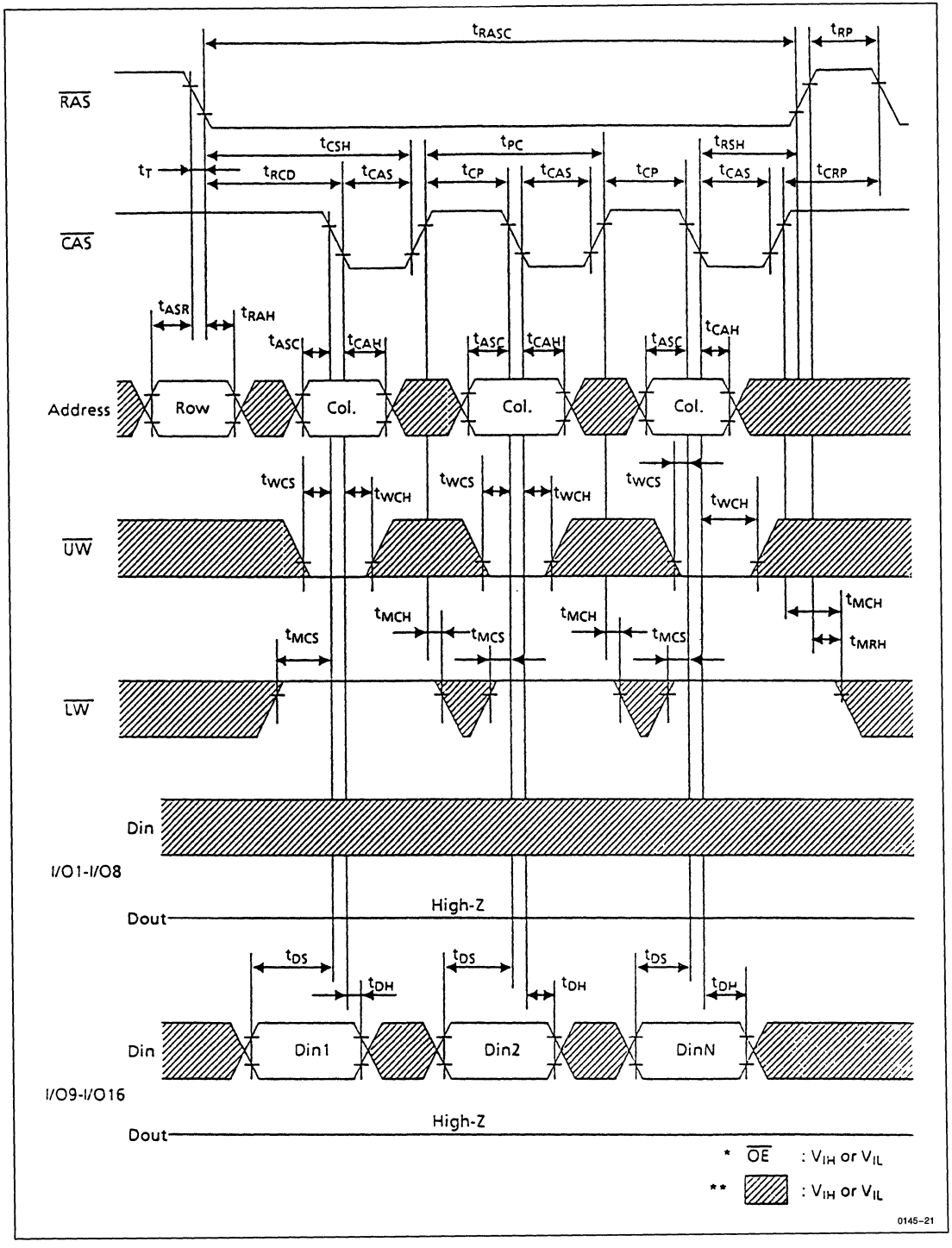
• Fast Page Mode Read Cycle



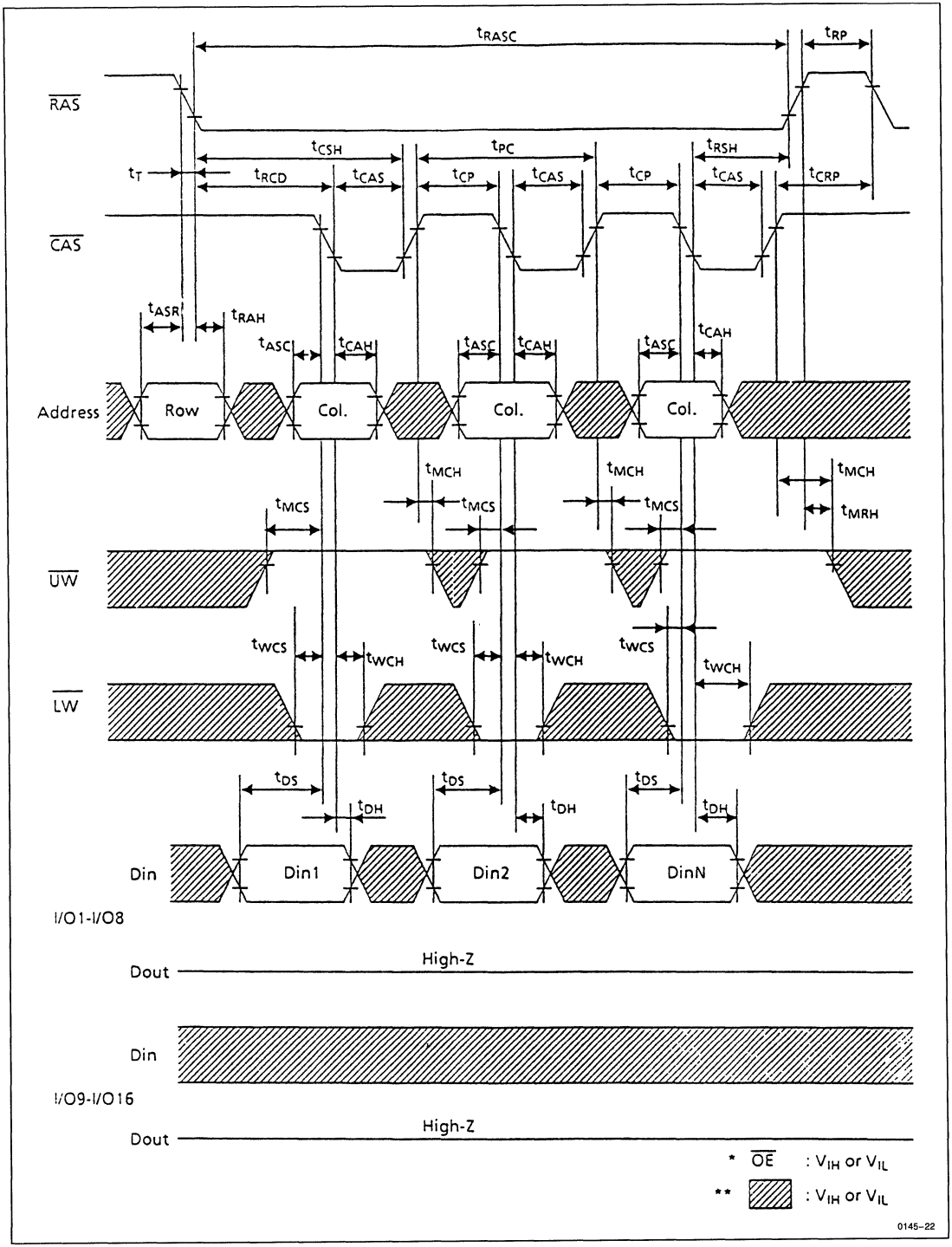
• **Fast Page Mode Early Write Cycle**



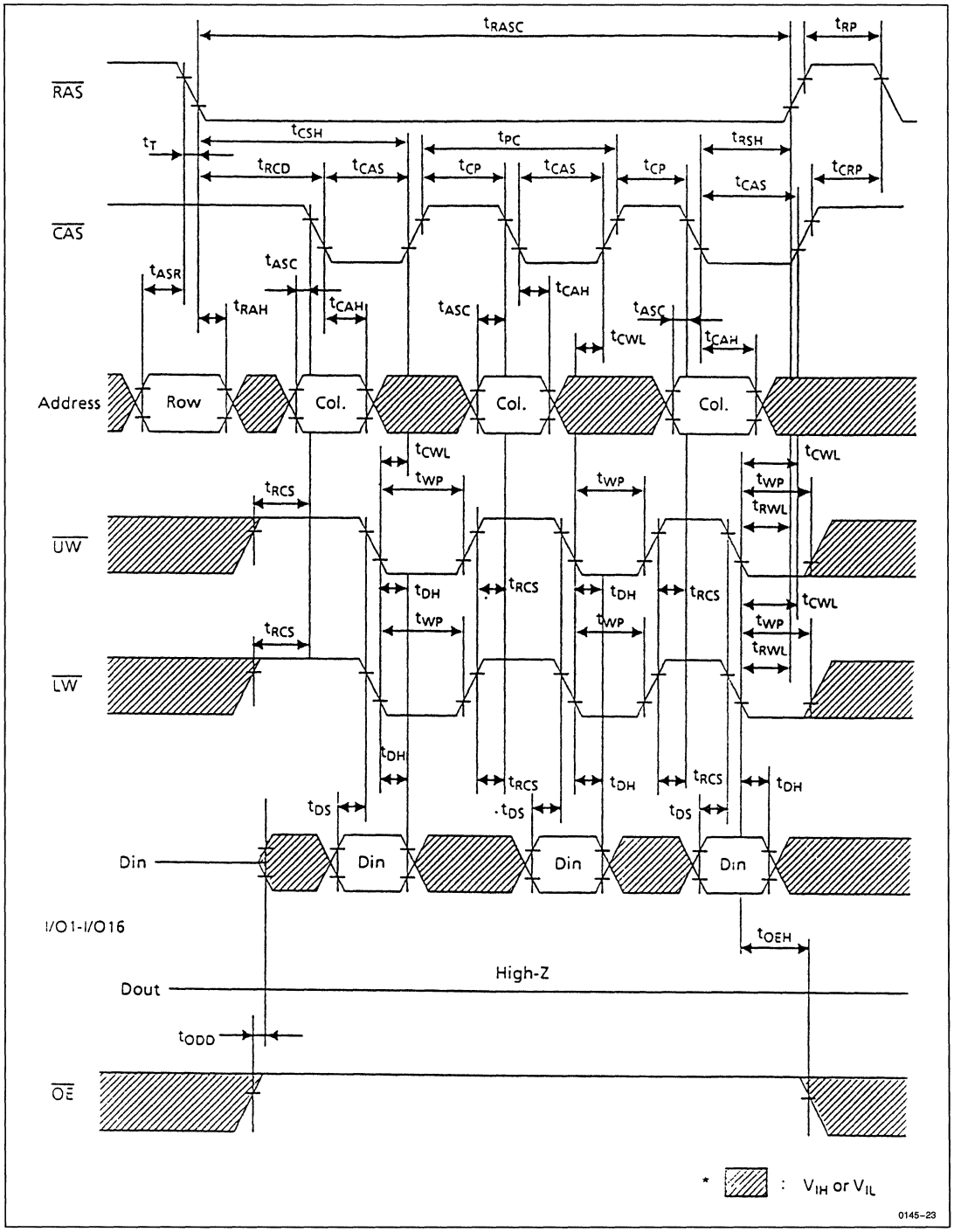
• **Fast Page Mode Upper Byte Early Write Cycle**



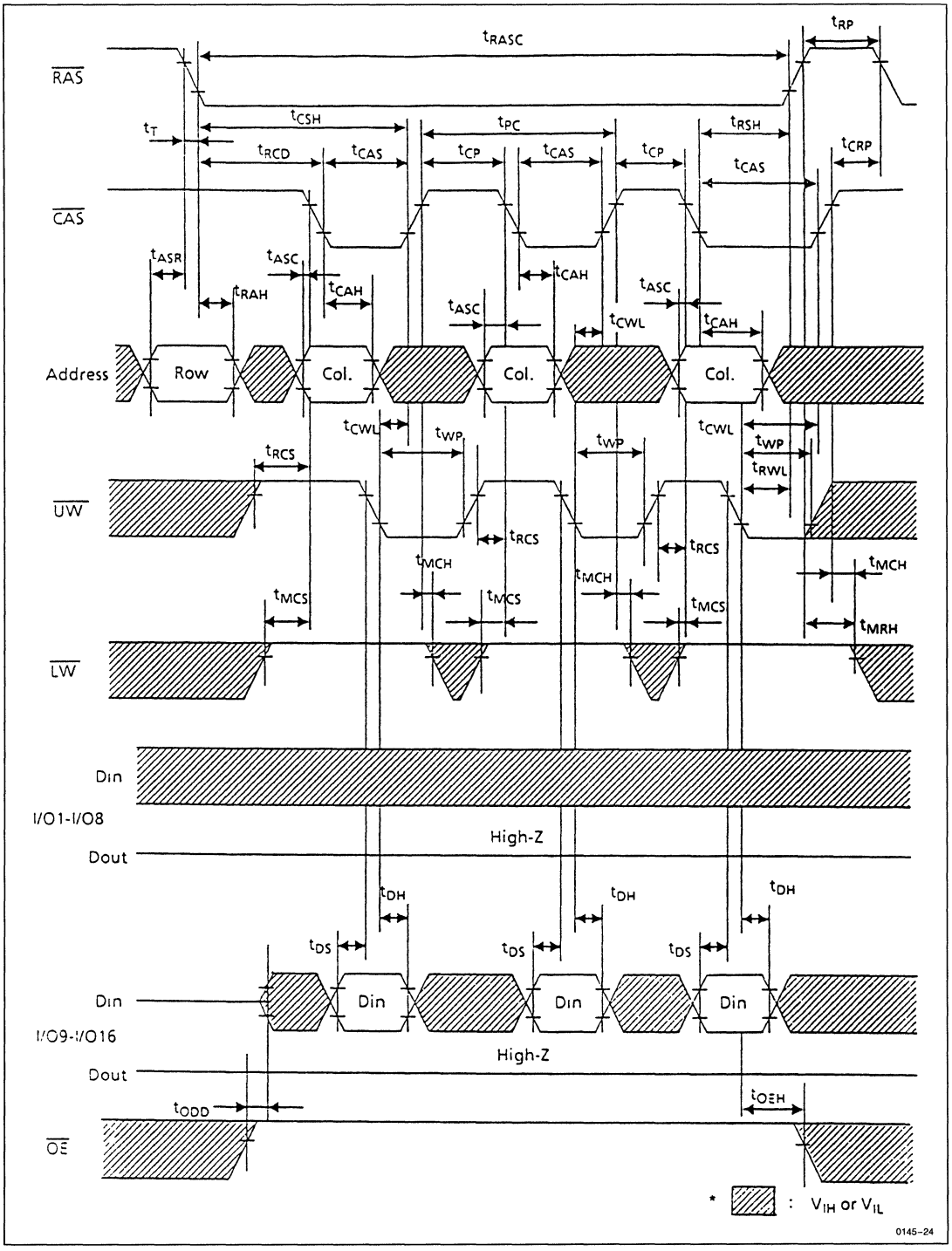
• **Fast Page Mode Lower Byte Early Write Cycle**



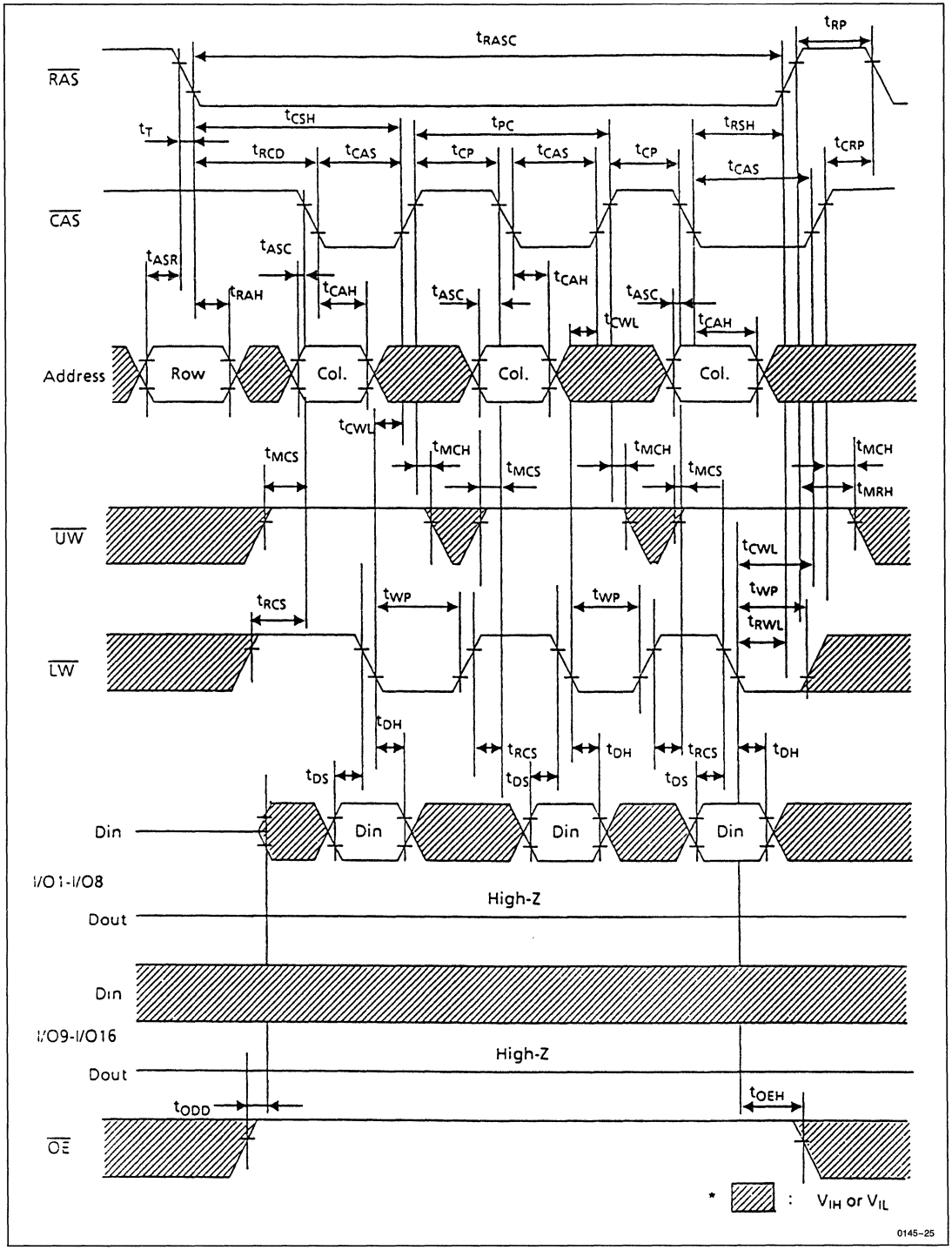
• **Fast Page Mode Delayed Write Cycle**



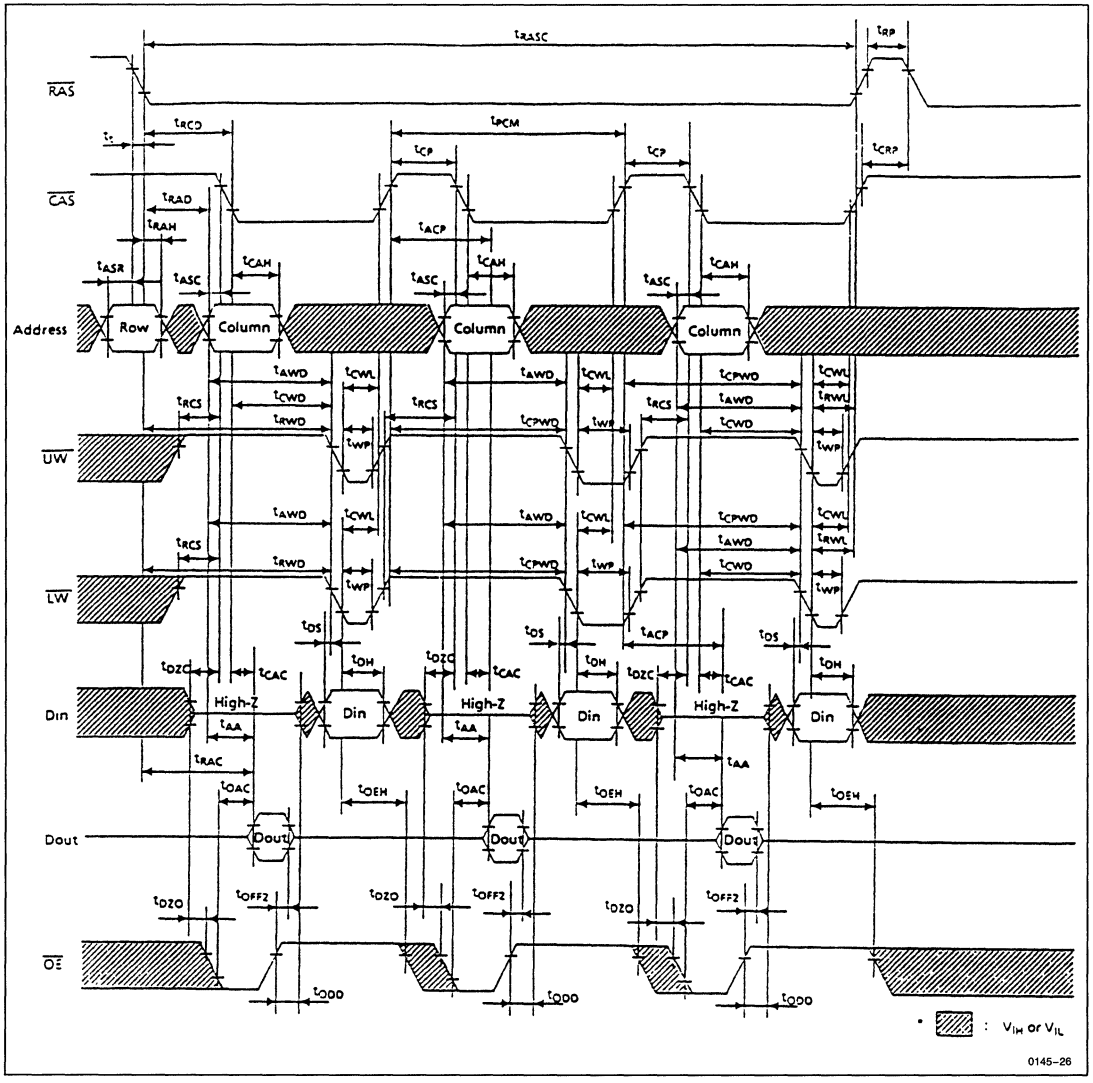
• **Fast Page Mode Upper Byte Delayed Write Cycle**



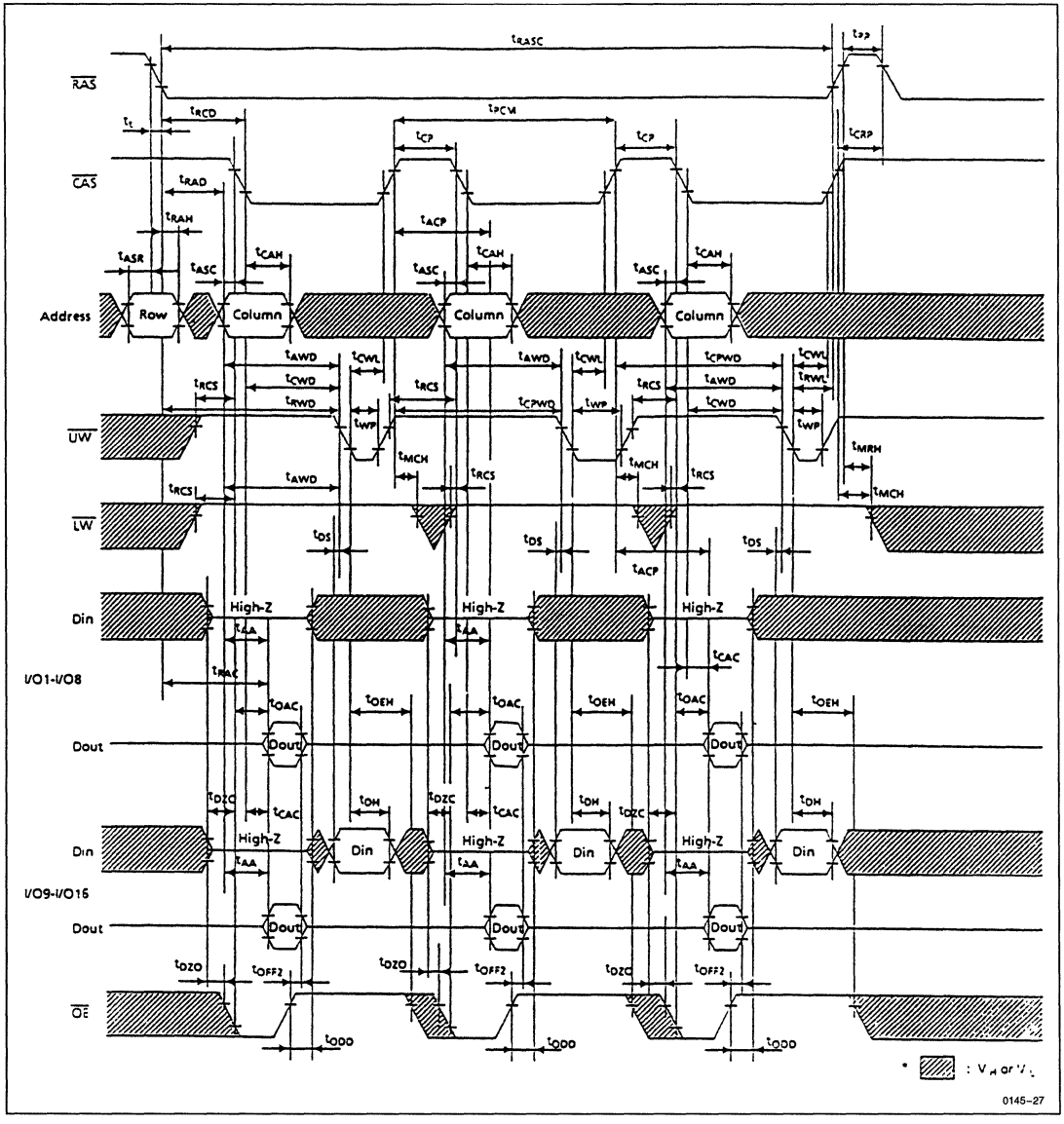
• **Fast Page Mode Lower Byte Delayed Write Cycle**



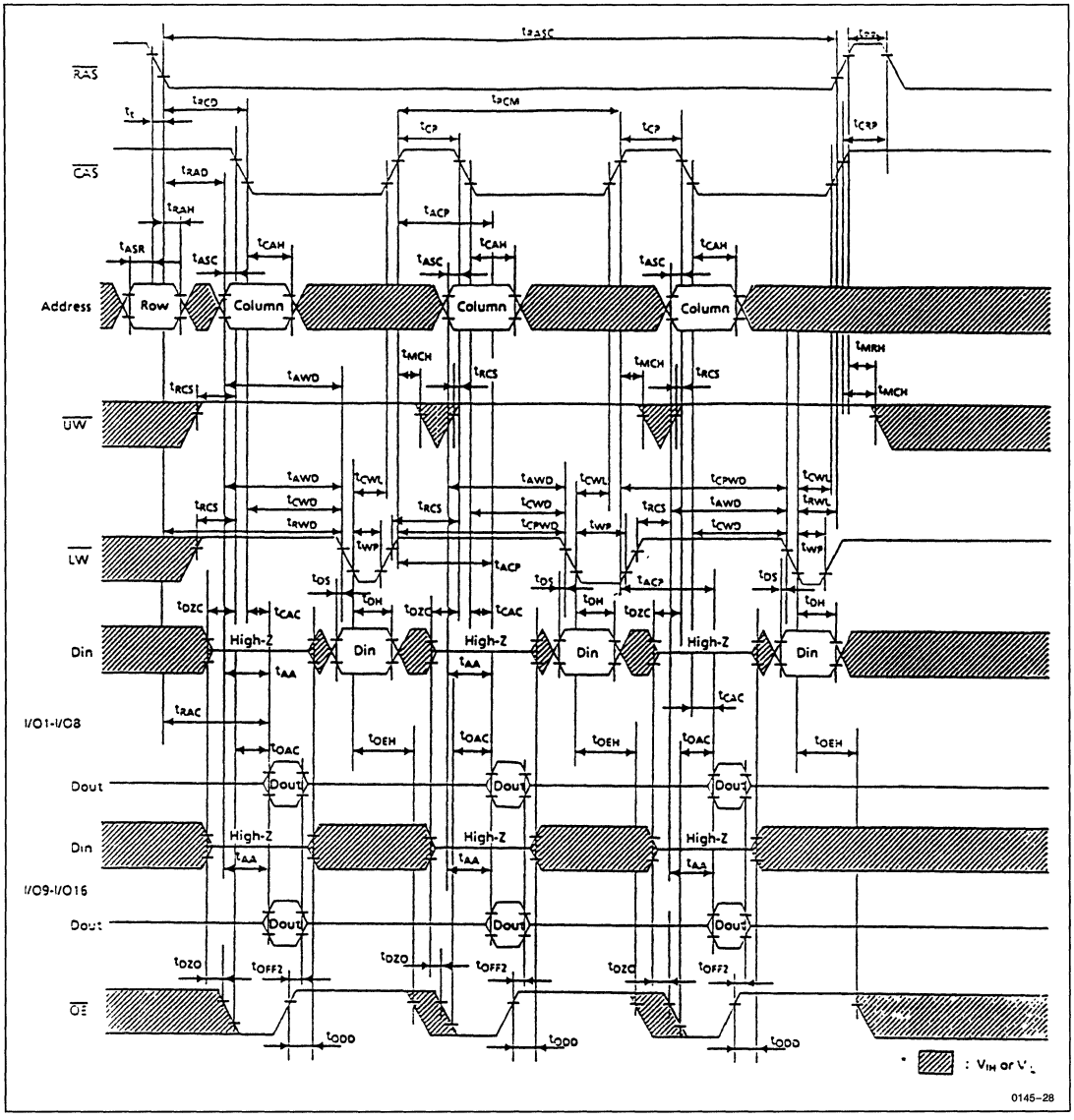
• **Fast Page Mode Read-Modify-Write Cycle**



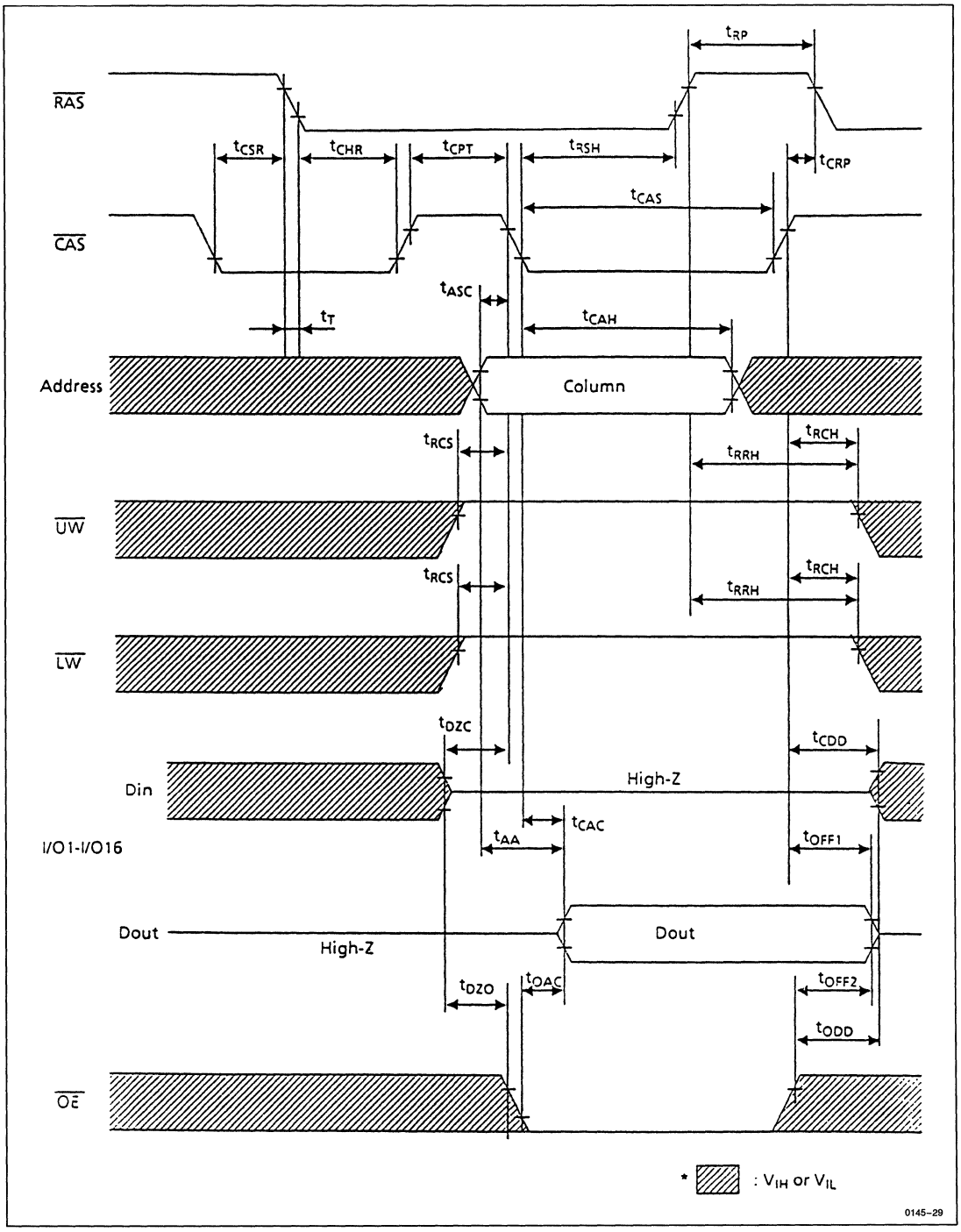
• Fast Page Mode Read-Modify-Upper-Byte-Write Cycle



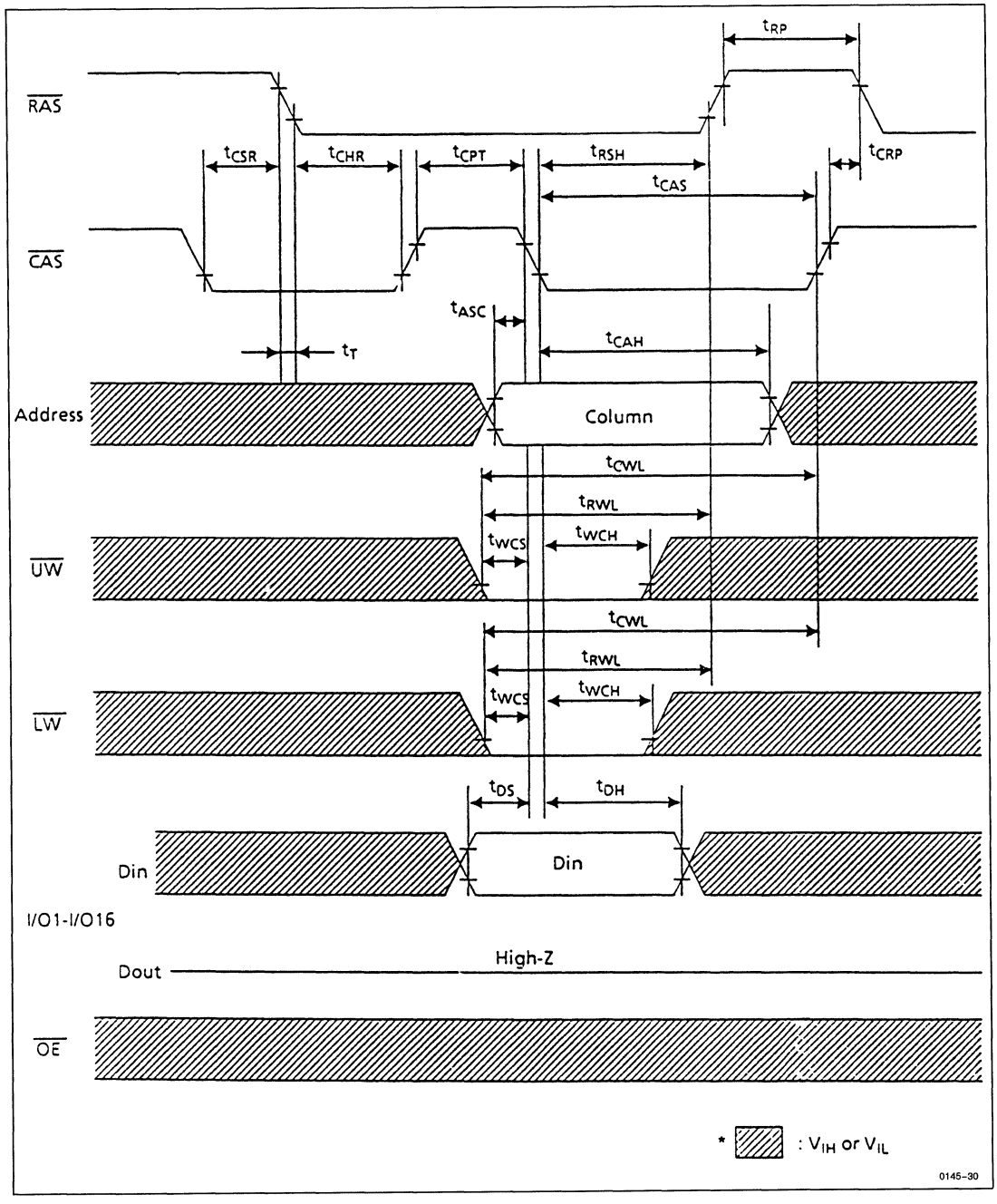
• **Fast Page Mode Read-Modify-Lower-Byte-Write Cycle**



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM511665 Series — Preliminary

65,536-Word x 16-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM511665 are CMOS dynamic RAM organized as 65,536-word x 16-bit. HM511665 have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM511665 offer Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM511665 to be packaged in standard 400 mil 40-pin plastic SOJ, standard 475 mil 40-pin plastic ZIP.

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode .....TBD
  - Standby Mode.....11 mW (max)
- Fast Page Mode Capability
- Write per Bit Capability
- 256 Refresh Cycles .....(4 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh

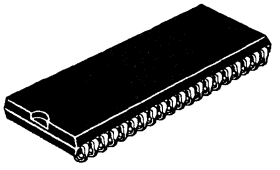
■ ORDERING INFORMATION

Part No.	Access Time	Package
HM511665JP-8 HM511665JP-10	80 ns 100 ns	400 mil 40-pin Plastic SOJ (CP-40D)
HM511665ZP-8 HM511665ZP-10	80 ns 100 ns	475 mil 40-pin Plastic ZIP (ZP-40)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_7	Address Input Refresh Address Input
$W1/I/O_1$–$W16/I/O_{16}$	Write Select/Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB}/\overline{WE}$	Write per Bit/Read/Write Enable
$\overline{WB}/\overline{WE}$	Write per Bit/Read/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

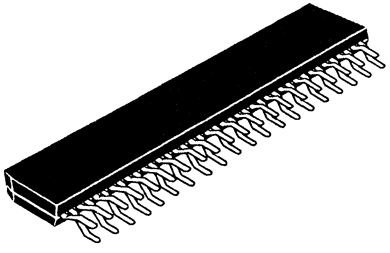
HM511665JP Series



3DCP40D

(CP-40D)

HM511665ZP Series

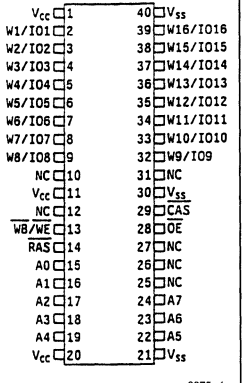


3DZP40

(ZP-40)

■ PIN OUT

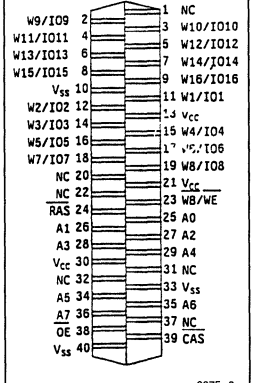
HM511665JP Series



0075-1

(Top View)

HM511665ZP Series



0075-2

(Bottom View)

■ TRUTH TABLE

Inputs				I/O	Operation
$\overline{RAS}$	$\overline{CAS}$	$\overline{WB}/\overline{WE}$	$\overline{OE}$	$W1/I/O_1$–$W16/I/O_{16}$	
H	H	H	H	High-Z	Standby
L	H	H	H	High-Z	Refresh
L	L	H	L	D_{out}	Read
L	L	L	H	D_{in}	Write
L	L	H	H	High-Z	

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	0.8	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(Wi/I/Oi Pin)	V_{IL}	−0.5	—	0.8	V	1, 2
	(Others)	V_{IL}	−1.0	—	0.8	V	1, 2

Notes: 1. All voltage referenced to V_{SS}.
2. The device will withstand undershoots to the −2V level with a maximum pulse width of 20 ns at the −1.5V level. (See figure 1.)

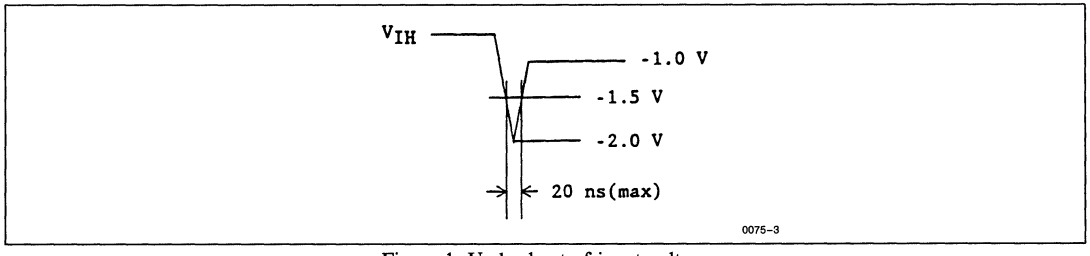


Figure 1. Undershoot of input voltage

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM511665-8		HM511665-10		Unit	Test Conditions	Note
		Min	Max	Min	Max			
Operating Current	I_{CC1}	TBD				mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	2				mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		1				mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	TBD				mA	t_{RC} = Min	2
Standby Current	I_{CC5}	TBD				mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	TBD				mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	TBD				mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	µA	0V ≤ V_{in} ≤ 6.5V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	µA	0V ≤ V_{out} ≤ 5.5V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 2.5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	V	Low I_{out} = 2.1 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• Capacitance (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 14, 15]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM511665-8		HM511665-10		Unit	Note
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	135	—	170	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	45	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	30	10000	40	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	20	60	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	15	45	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	30	—	40	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	15	—	15	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	ns	
$\overline{CAS}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	4	—	4	ms	

Read Cycle

Parameter	Symbol	HM511665-8		HM511665-10		Unit	Note
		Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	—	40	ns	3, 4, 13
Access Time from Address	t_{AA}	—	45	—	55	ns	3, 5, 13
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	40	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	20	0	20	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	15	0	15	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	20	—	20	—	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	t_{ROH}	10	—	10	—	ns	

Write Cycle

Parameter	Symbol	HM511665-8		HM511665-10		Unit	Note
		Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM511665-8		HM511665-10		Unit	Note
		Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	185	—	220	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	105	—	125	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	55	—	65	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	70	—	80	—	ns	10, 13
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	15	—	15	—	ns	

Refresh Cycle

Parameter	Symbol	HM511665-8		HM511665-10		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time in Normal Mode	t_{CPN}	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM511665-8		HM511665-10		Unit	Note
		Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	80	100000	100	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	45	—	55	ns	3, 13
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	45	—	55	—	ns	
Fast Page Mode Read-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPW}	70	—	80	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	100	—	110	—	ns	

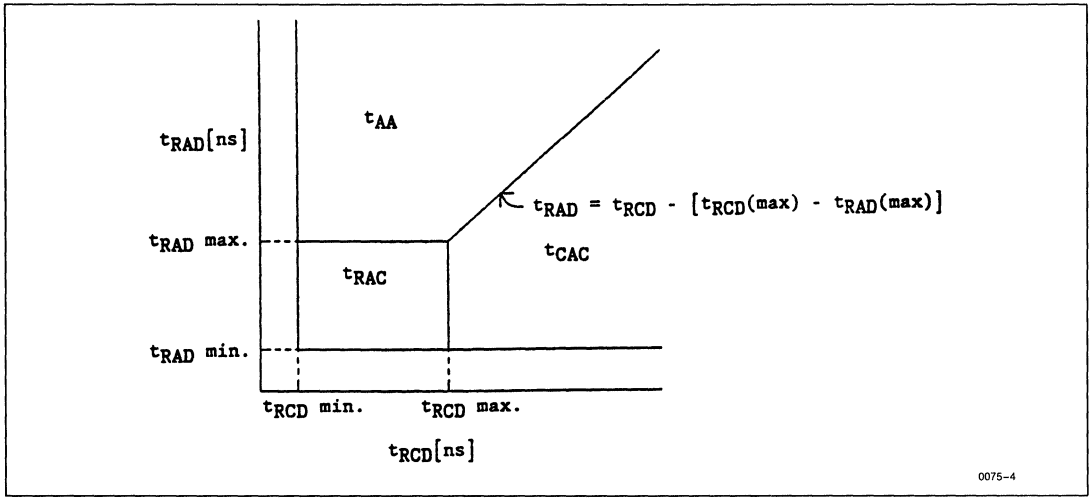
Counter Test Cycle

Parameter	Symbol	HM511665-8		HM511665-10		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	40	—	ns	

Write per Bit Cycle[16, 17]

Parameter	Symbol	HM511665-8		HM511665-10		Unit	Note
		Min	Max	Min	Max		
Write per Bit Setup Time	t_{WBS}	0	—	0	—	ns	
Write per Bit Hold Time	t_{WBH}	10	—	10	—	ns	
Write per Bit Selection Setup Time	t_{WDS}	0	—	0	—	ns	
Write per Bit Selection Hold Time	t_{WDH}	10	—	10	—	ns	

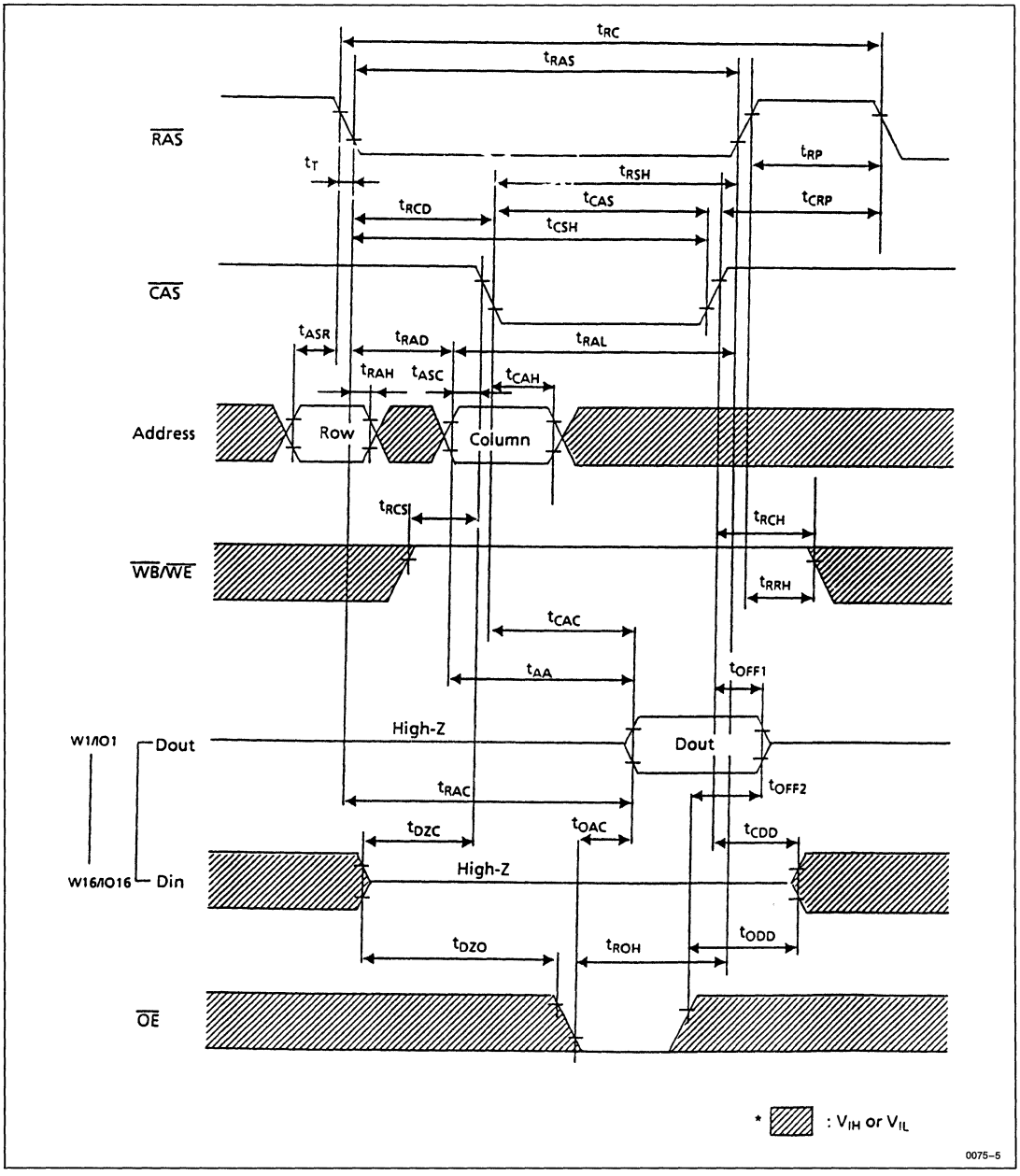
Notes: 1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 1 TTL load and 50 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $(t_{RCD} - t_{RAD}) \geq [t_{RCD}$ (max) $- t_{RAD}$ (max)].
5. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $(t_{RCD} - t_{RAD}) \leq [t_{RCD}$ (max) $- t_{RAD}$ (max)]. t_{RAC}, t_{CAC}, and t_{AA} are determined as follows.



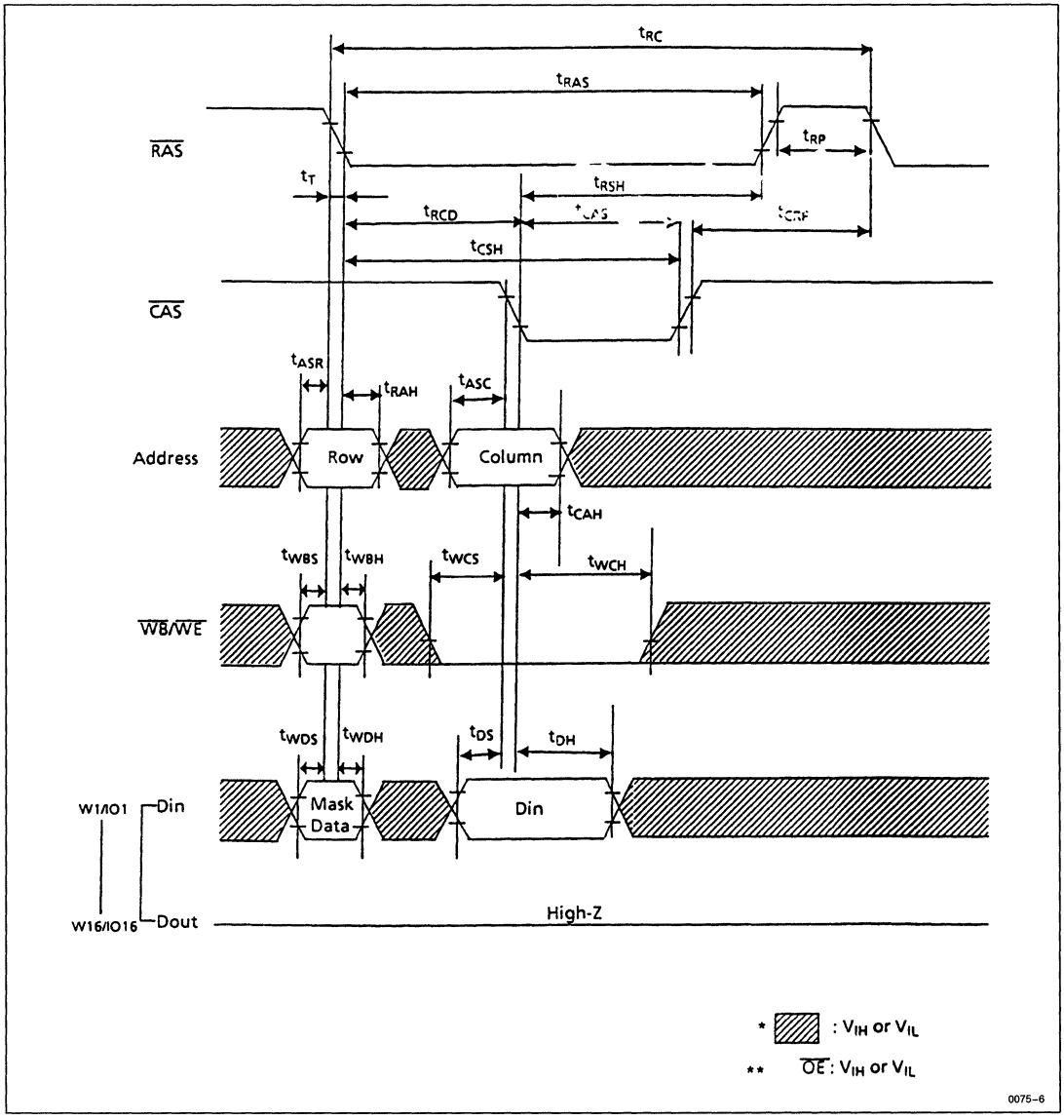
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to CAS leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. When using the write-per-bit capability, $\overline{WB/WE}$ must be low as $\overline{RAS}$ falls.
17. The data bits to which the write operation is applied can be specified by keeping Wi/I/Oi high with setup and hold time referenced to the $\overline{RAS}$ negative transition.

■ TIMING WAVEFORMS

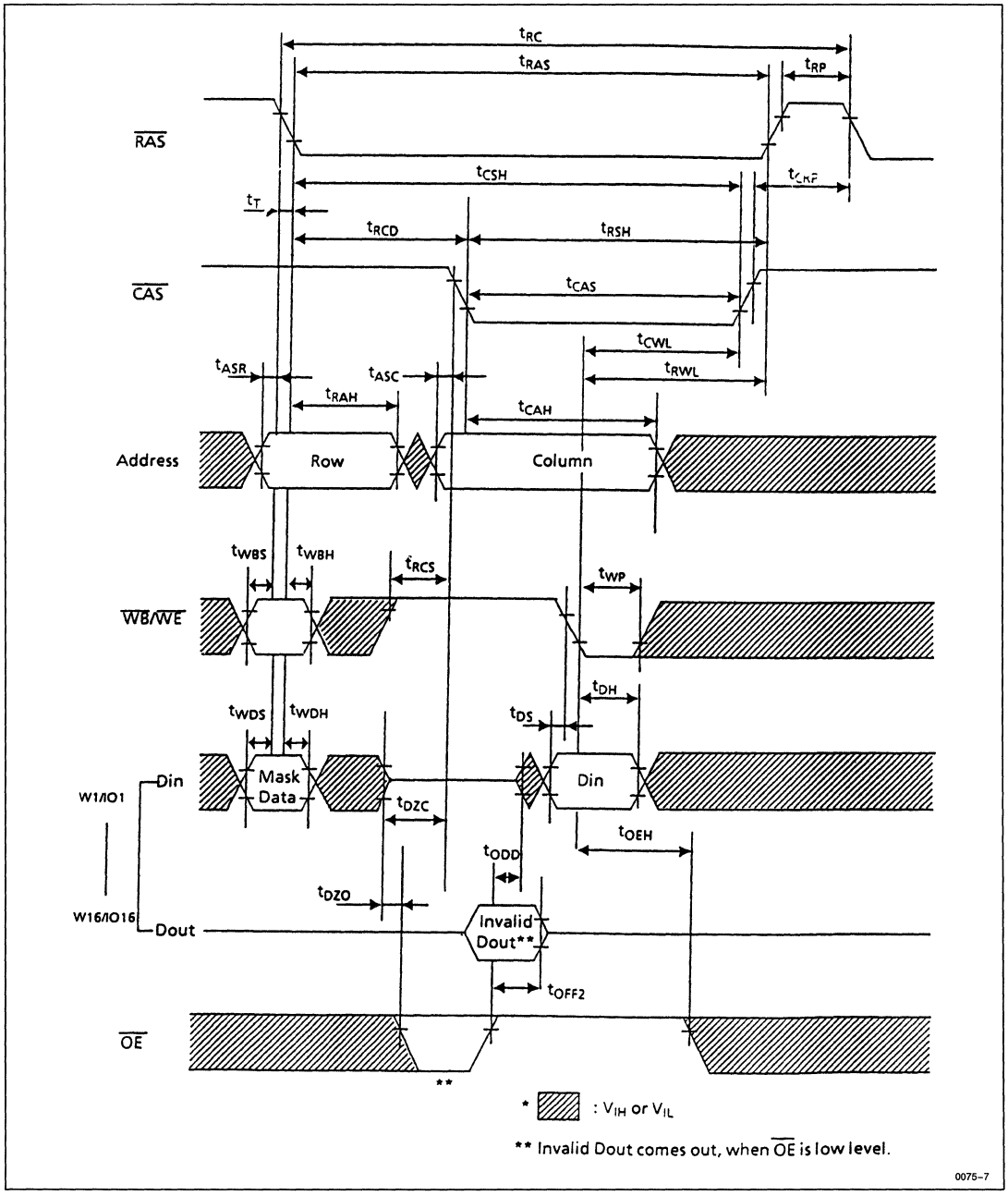
• Read Cycle



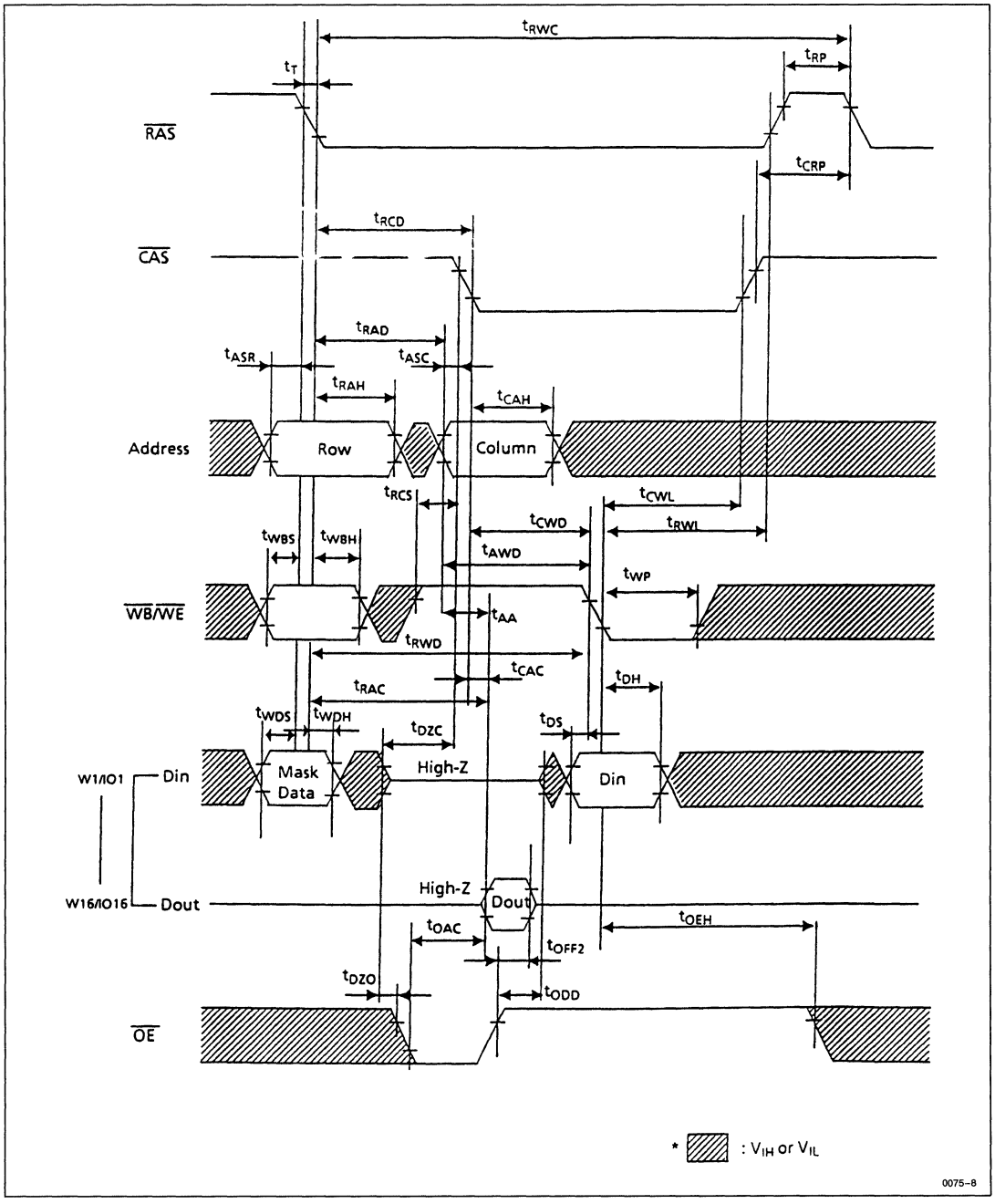
• **Early Write Cycle**



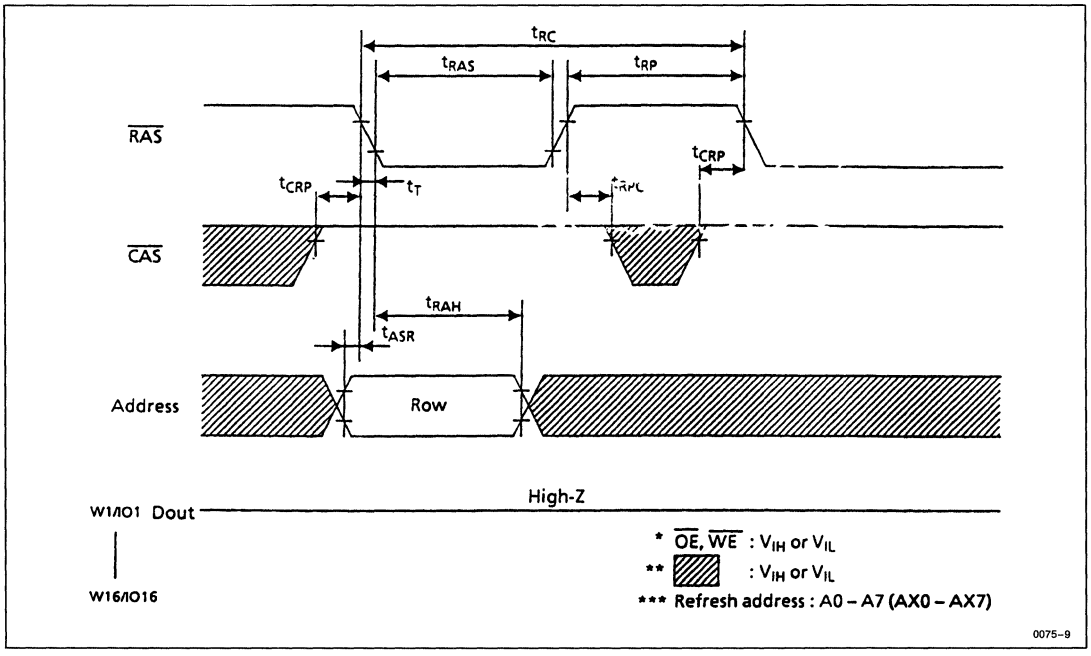
• **Delayed Write Cycle**



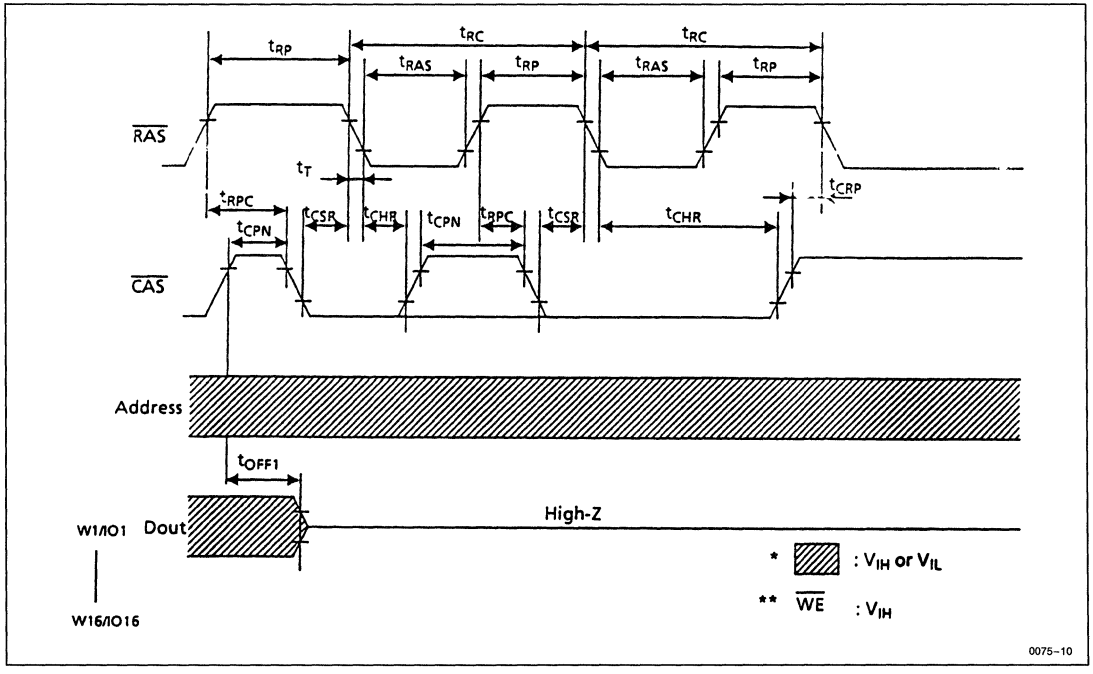
• **Read-Modify-Write Cycle**



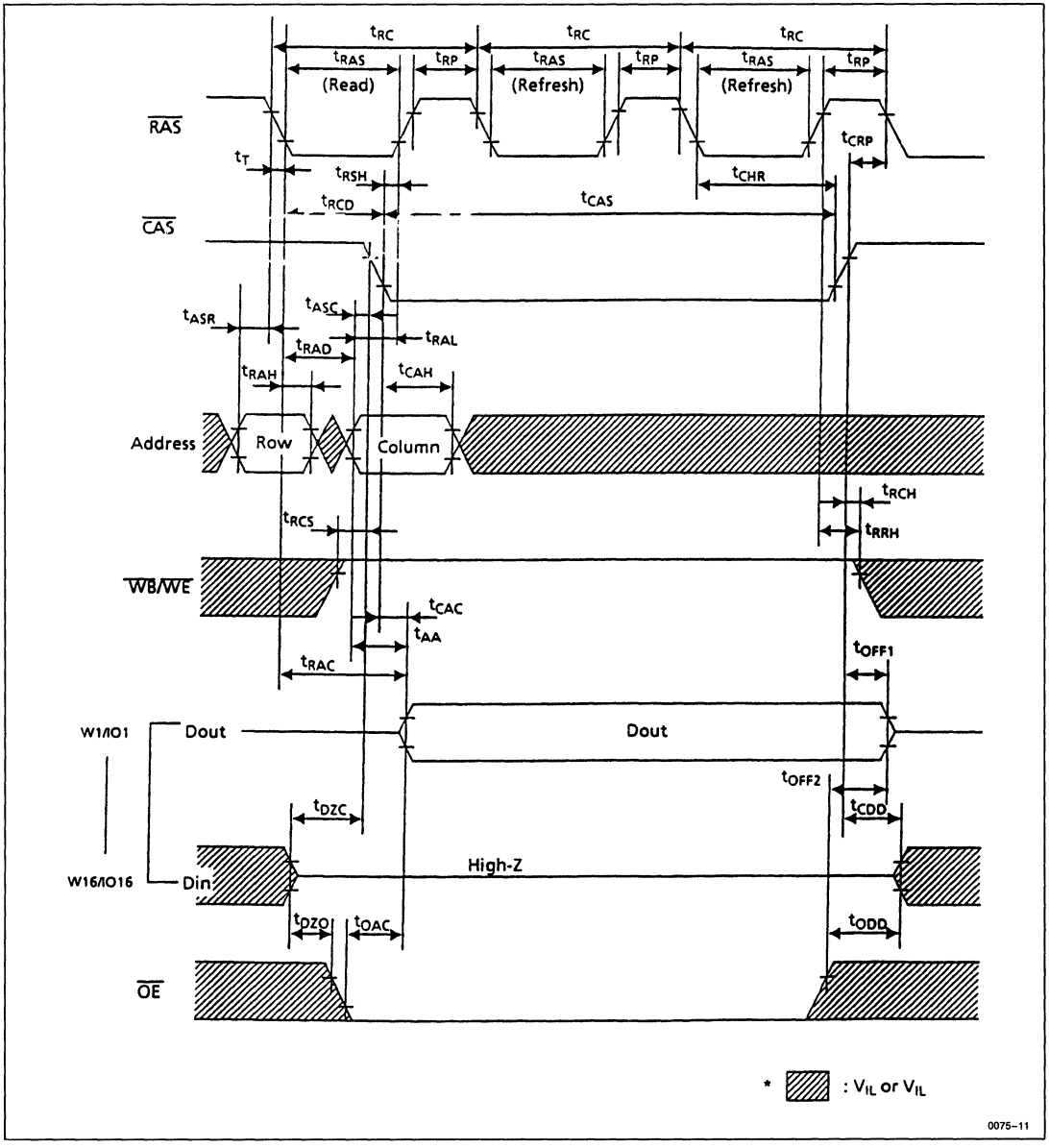
• $\overline{RAS}$ Only Refresh Cycle



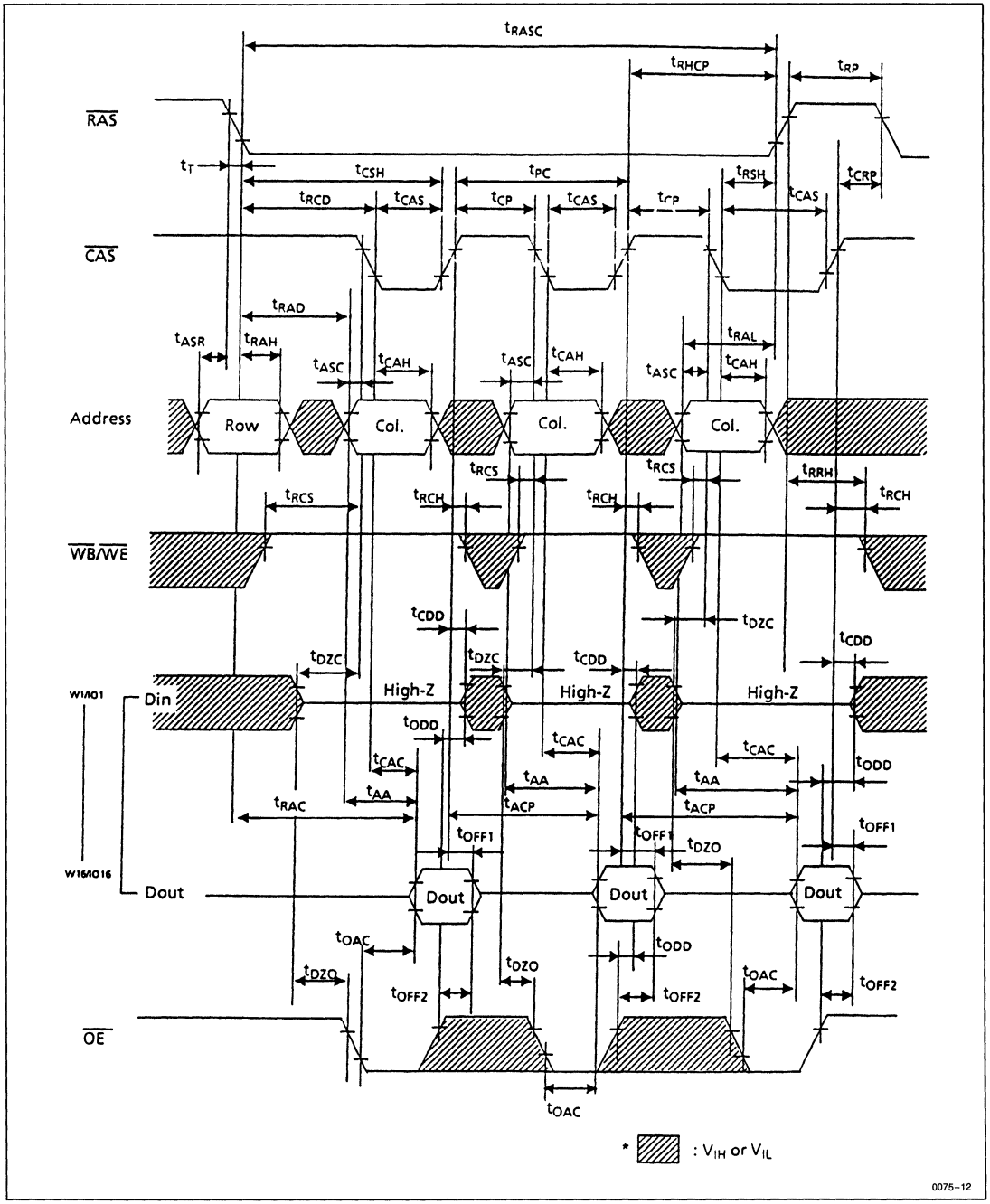
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



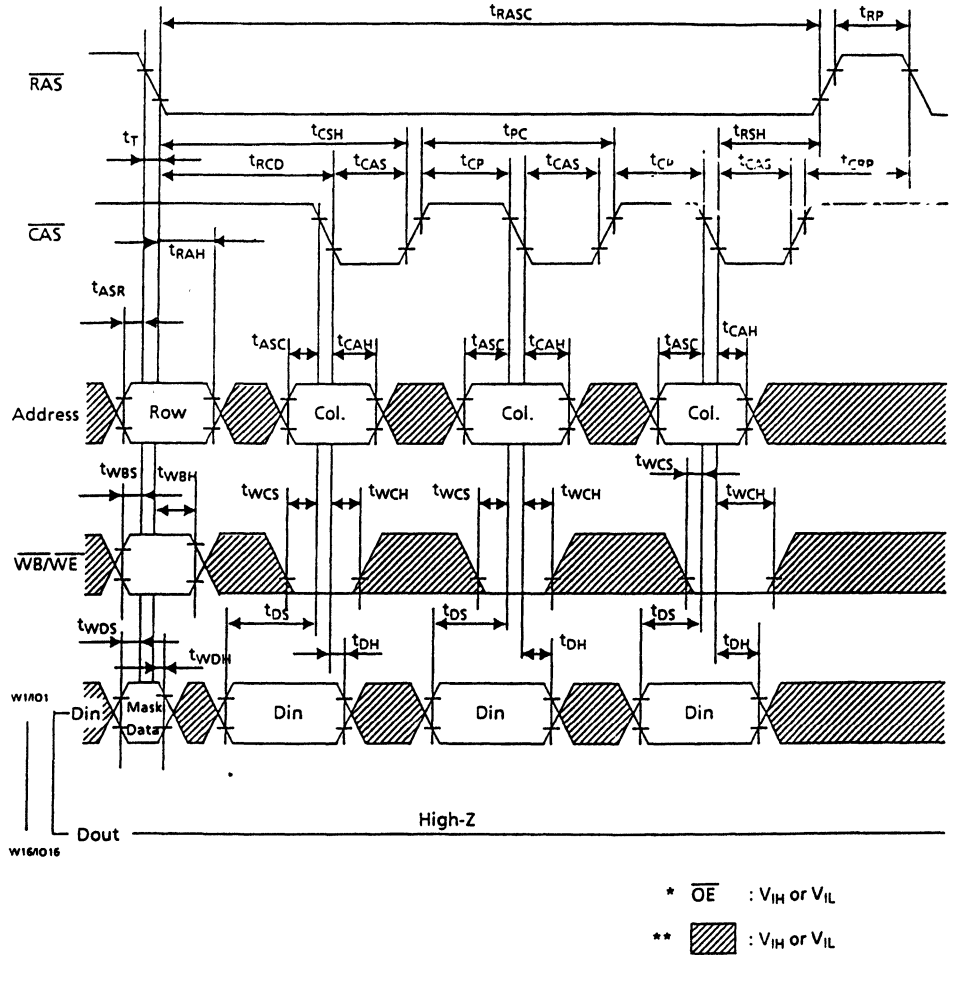
• **Hidden Refresh Cycle**



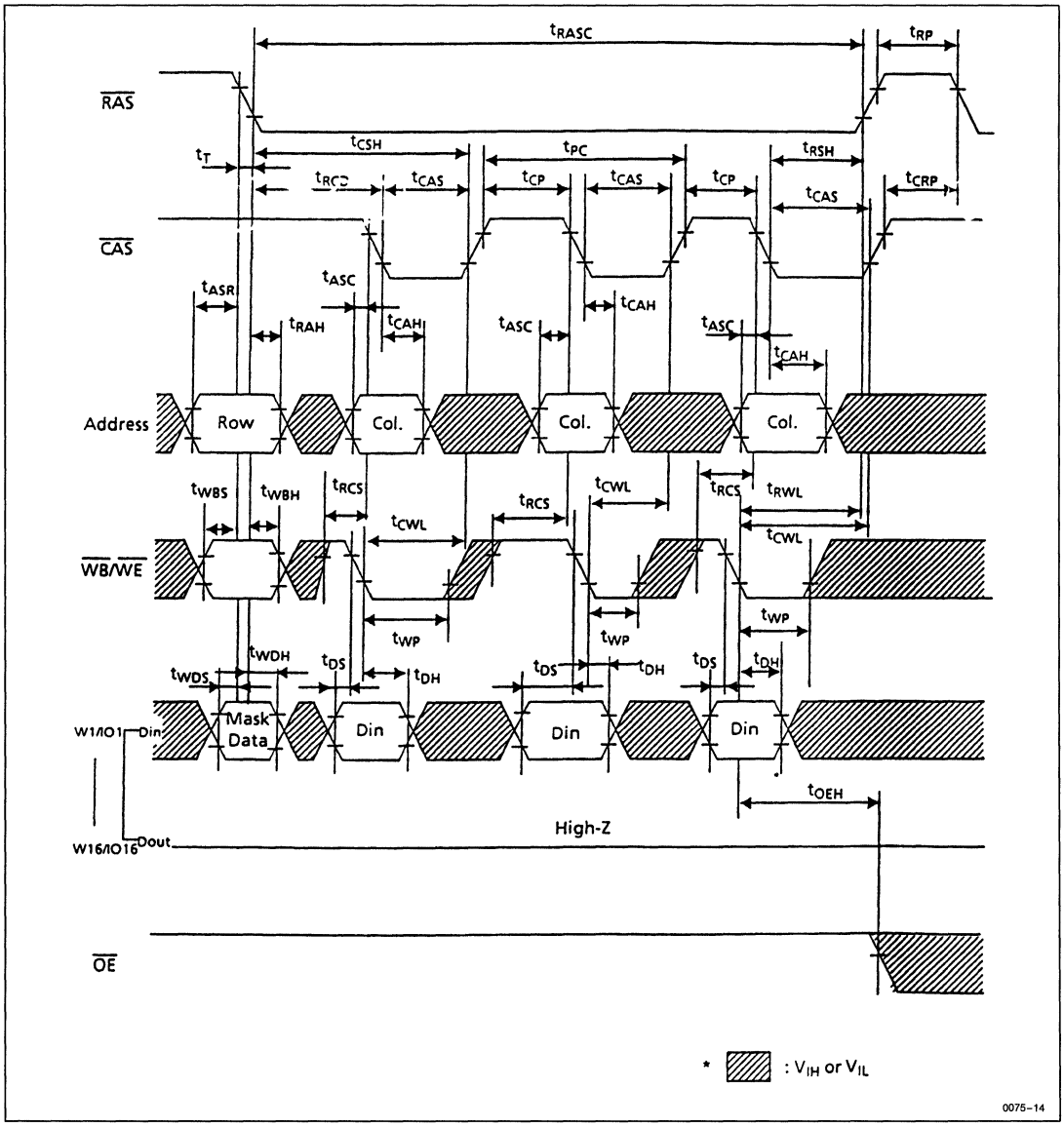
• **Fast Page Mode Read Cycle**



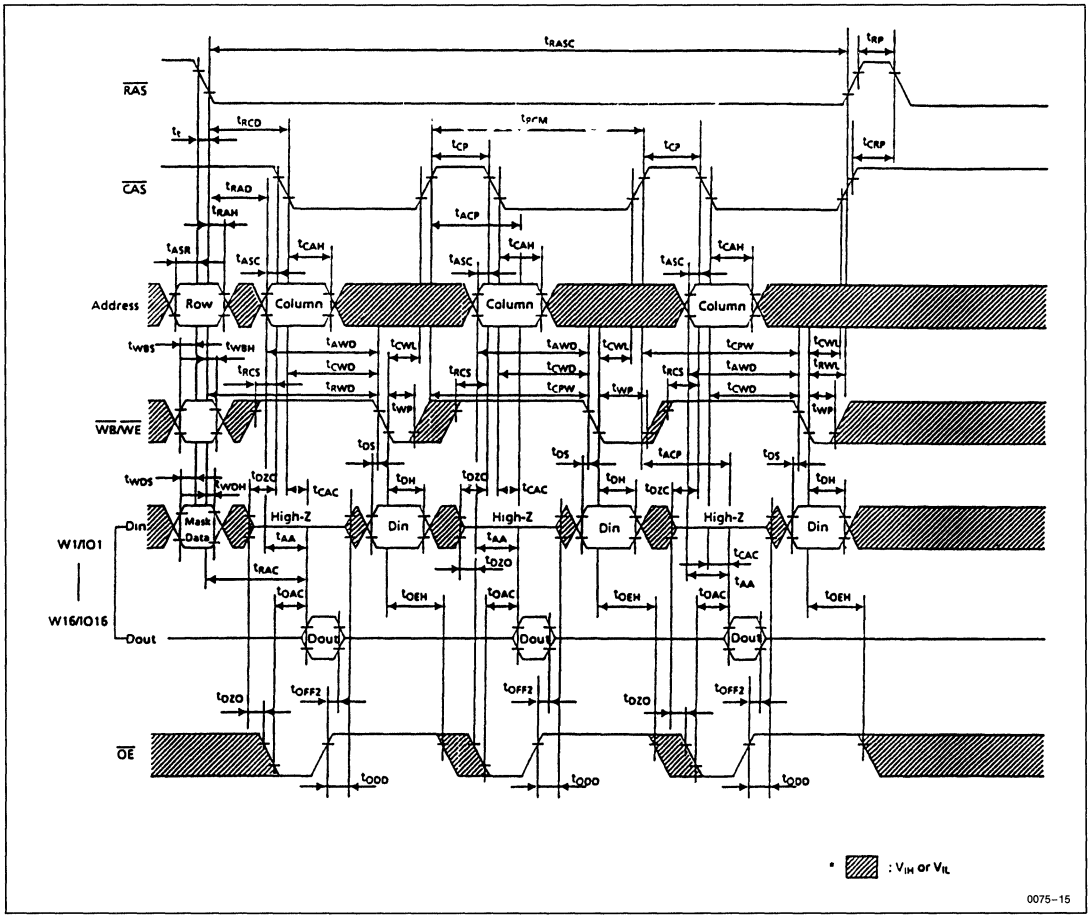
• **Fast Page Mode Early Write Cycle**



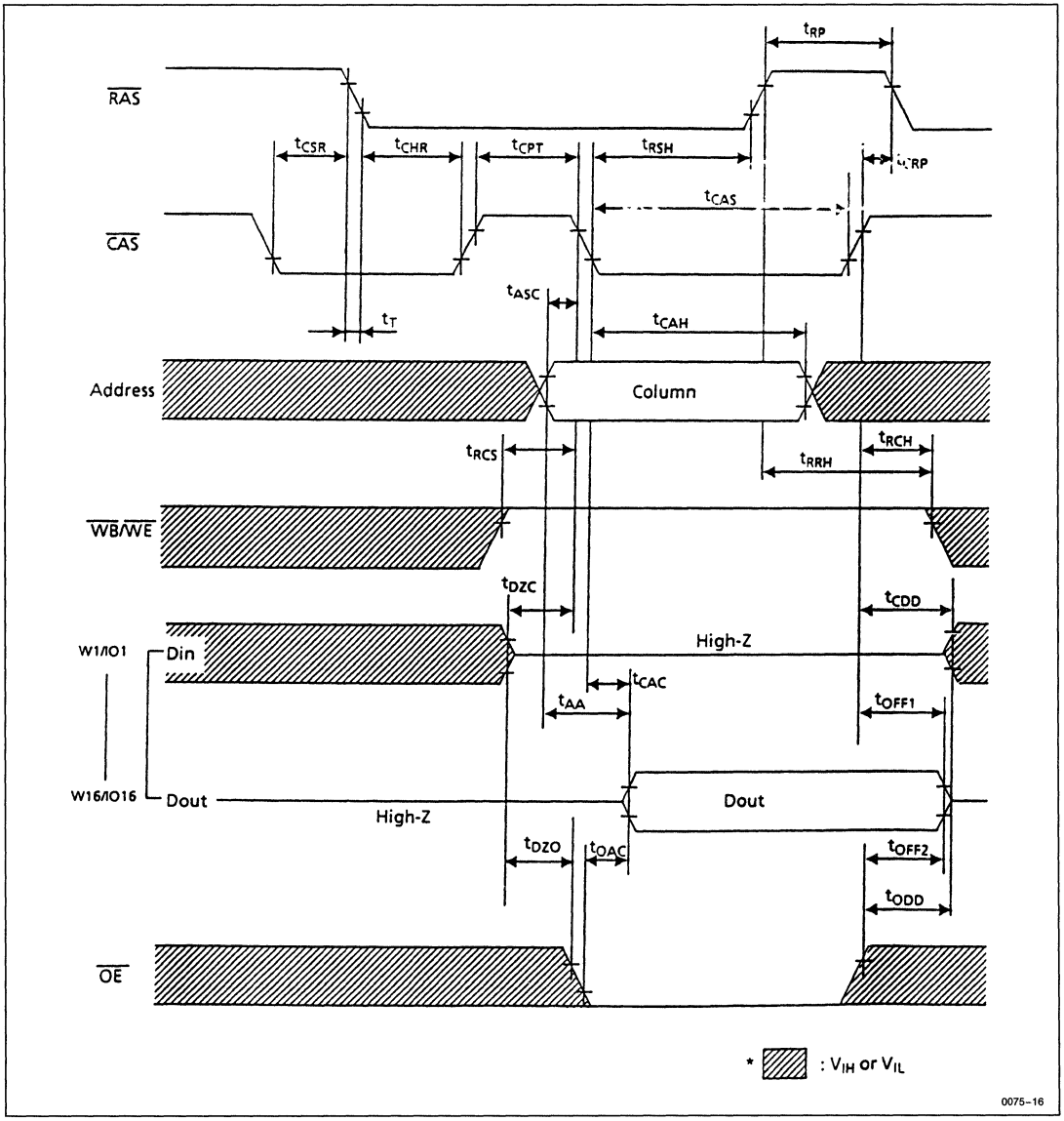
• **Fast Page Mode Delayed Write Cycle**



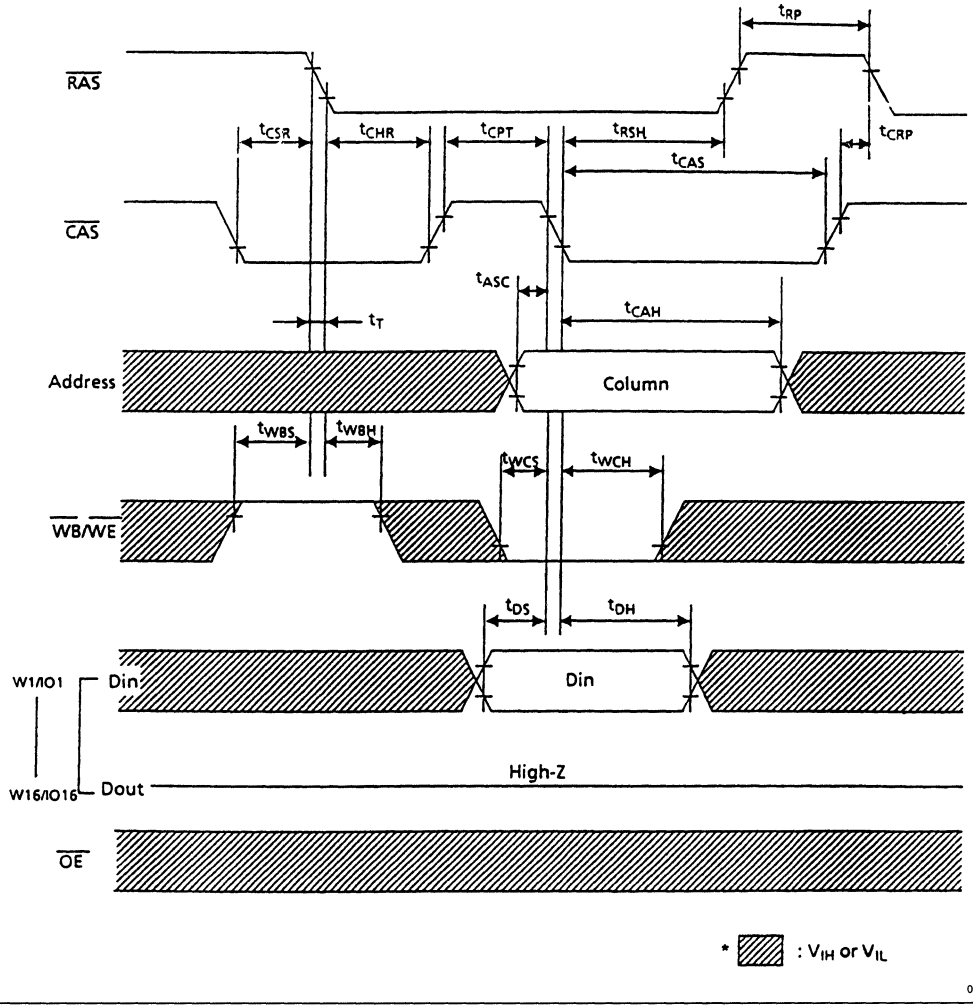
• **Fast Page Mode Read-Modify-Write Cycle**



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Check Cycle (Write)



HM511665/L Series

65,536-Word x 16-Bit Dynamic RAM

■ DESCRIPTION

The Hitachi HM511665/HM511665L are CMOS dynamic RAM organized as 65,536-word x 16-bit. HM511665/11665L have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM511665/HM511665L offer Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM511665/HM511665L to be packaged in standard 400 mil 40-pin plastic SOJ, standard 475 mil 40-pin plastic ZIP.

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode.....633 mW/495 mW (max)
  - Standby Mode (TTL) .....11 mW (max)
  - Standby Mode (CMOS) .....5.5 mW (max)
  - .....1.1 mW (max) (L-Version)
- Fast Page Mode Capability
- Write per Bit Capability
- 256 Refresh Cycles .....(4 ms)
  - .....(32 ms) (L-Version)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Battery Back-up Operation
  - HM511665L Series (L-Version)

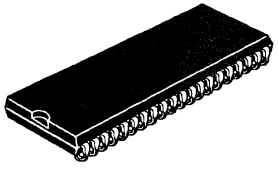
■ PIN DESCRIPTION

Pin Name	Function
A_0–A_7	Address Input Refresh Address Input
$W1/I/O_1$–$W16/I/O_{16}$	Write Select/Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB}/\overline{WE}$	Write per Bit/Read/Write Enable
$\overline{OE}$	Output Enable
V_{CC}[1]	Power (+ 5V)
V_{SS}[2]	Ground
NC	No Connection

Notes: 1. This device has 3 V_{CC} pins (SOJ: 1, 11, 20 pin/ZIP: 13, 21, 30 pin). All V_{CC} pins must be connected with the same power-supply wiring on the memory board.

2. This device has 3 V_{SS} pins (SOJ: 21, 30, 40 pin/ZIP: 10, 33, 40 pin). All V_{SS} pins must be connected with the same ground wiring on the memory board.

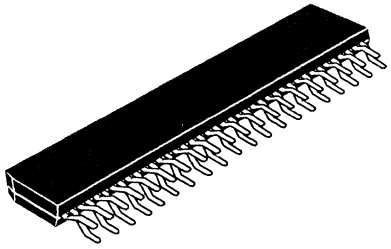
HM511665JP Series



3DCP40D

(CP-40D)

HM511665ZP Series

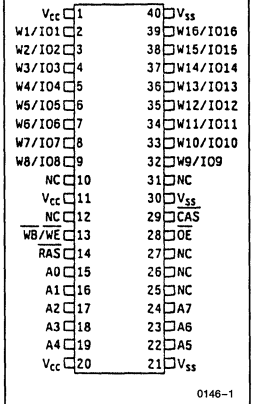


3DZP40

(ZP-40)

■ PIN OUT

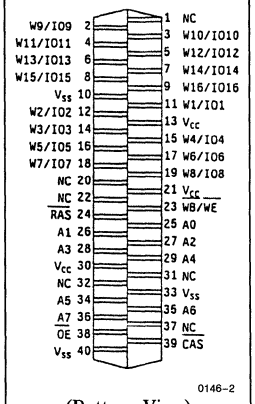
HM511665JP Series



0146-1

(Top View)

HM511665ZP Series



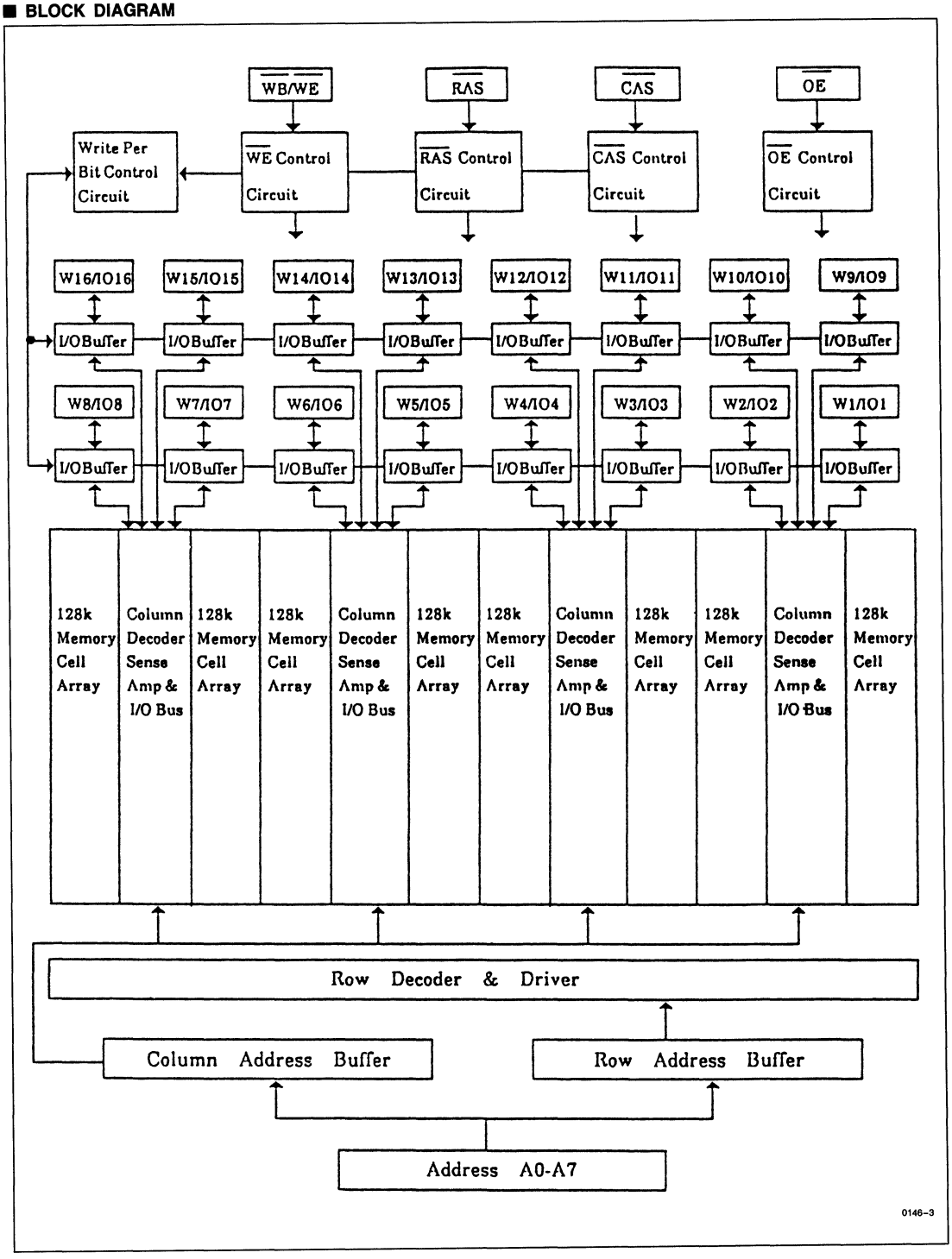
0146-2

(Bottom View)

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM511665JP-8 HM511665JP-10	80 ns 100 ns	400 mil 40-pin Plastic SOJ (CP-40D)
HM511665LJ-8 HM511665LJ-10	80 ns 100 ns	
HM511665ZP-8 HM511665ZP-10	80 ns 100 ns	475 mil 40-pin Plastic ZIP (ZP-40)
HM511665LZ-8 HM511665LZ-10	80 ns 100 ns	

■ BLOCK DIAGRAM



■ TRUTH TABLE

Inputs				I/O	Operation
$\overline{RAS}$	$\overline{CAS}$	$\overline{WB}/\overline{WE}$	$\overline{OE}$	W1/I/O$_1$–W16/I/O$_{16}$	
H	H	H	H	High-Z	Standby
L	H	H	H	High-Z	Refresh
L	L	H	L	D_{out}	Read
L	L	L	H	D_{in}	Write
L	L	H	H	High-Z	

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	0.8	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(Wi/I/Oi Pin)	V_{IL}	−0.5	—	0.8	V	1, 2
	(Others)	V_{IL}	−1.0	—	0.8	V	1, 2

Notes: 1. All voltage referenced to V_{SS}.
2. The device will withstand undershoots to the −2V level with a maximum pulse width of 20 ns at the −1.5V level. (See figure 1.)

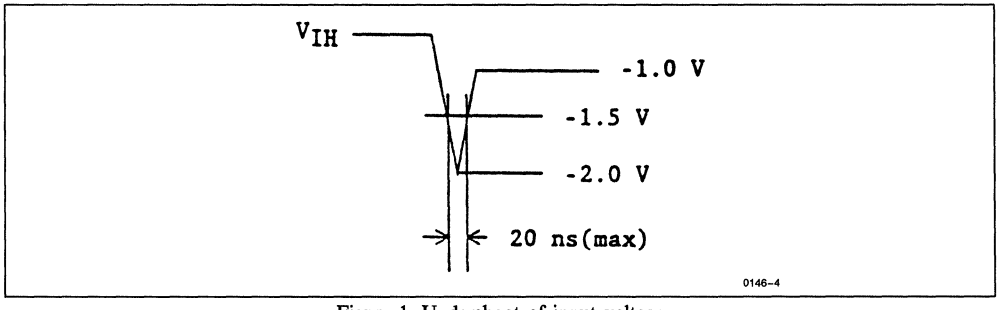


Figure 1. Undershoot of input voltage

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM511665-8 HM511665L-8		HM511665-10 HM511665L-10		Unit	Test Conditions	Note
		Min	Max	Min	Max			
Operating Current	I_{CC1}	—	115	—	90	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	2				mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	4
		1				mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	4
(L-Version) Standby Current	I_{CC2}	—	200	—	200	µA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} $\overline{WE}$, $\overline{OE}$, Address and D_{in} = V_{IH} or V_{IL} D_{out} = High-Z	5
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	115	—	90	mA	t_{RC} = Min	2
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	115	—	90	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	100	—	85	mA	t_{PC} = Min	1, 3
(L-Version) Battery Back-up Operating Current (Standby with CBR Refresh)	I_{CC10}	—	300	—	300	µA	t_{RC} = 125 µs t_{RAS} ≤ 1 µs $\overline{WE}$ = V_{IH}, $\overline{CAS}$ = V_{IL} $\overline{OE}$, Address and D_{in} = V_{IH} or V_{IL} D_{out} = High-Z	5
Input Leakage Current	I_{LI}	−10	10	−10	10	µA	0V ≤ V_{in} ≤ 6.5V	
Output Leakage Current	I_{LO}	−10	10	−10	10	µA	0V ≤ V_{out} ≤ 5.5V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −2.5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	V	Low I_{out} = 2.1 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. Clock voltages ($\overline{RAS}$ and $\overline{CAS}$) must be applied simultaneously with or prior to applying supply voltage.
5. V_{CC} − 0.2V ≤ V_{IH} ≤ 6.5V and 0V ≤ V_{IL} ≤ 0.2V.

• Capacitance (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 14, 15]

Test Conditions

Input Rise and Fall Times: 5 ns
Input Timing Reference Levels: 0.8V, 2.4V
Output Load: 1 TTL Gate + C_L (50 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM511665-8 HM511665L-8		HM511665-10 HM511665L-10		Unit	Note
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	135	—	170	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	45	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	30	10000	40	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	20	60	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	15	45	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	30	—	40	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	15	—	15	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	ns	
$\overline{CAS}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	4	—	4	ms	
		—	32	—	32	ms	L-Version

Read Cycle

Parameter	Symbol	HM511665-8 HM511665L-8		HM511665-10 HM511665L-10		Unit	Note
		Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	—	40	ns	3, 4, 13
Access Time from Address	t_{AA}	—	45	—	55	ns	3, 5, 13
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	40	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	20	0	20	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	15	0	15	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	20	—	20	—	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	t_{ROH}	10	—	10	—	ns	

Write Cycle

Parameter	Symbol	HM511665-8 HM511665L-8		HM511665-10 HM511665L-10		Unit	Note
		Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM511665-8 HM511665L-8		HM511665-10 HM511665L-10		Unit	Note
		Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	185	—	220	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	105	—	125	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	55	—	65	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	70	—	80	—	ns	10, 13
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	15	—	15	—	ns	

Refresh Cycle

Parameter	Symbol	HM511665-8 HM511665L-8		HM511665-10 HM511665L-10		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time in Normal Mode	t_{CPN}	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM511665-8 HM511665L-8		HM511665-10 HM511665L-10		Unit	Note
		Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	80	100000	100	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	60	ns	3, 13
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	45	—	55	—	ns	
Fast Page Mode Read-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPW}	70	—	80	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	100	—	110	—	ns	

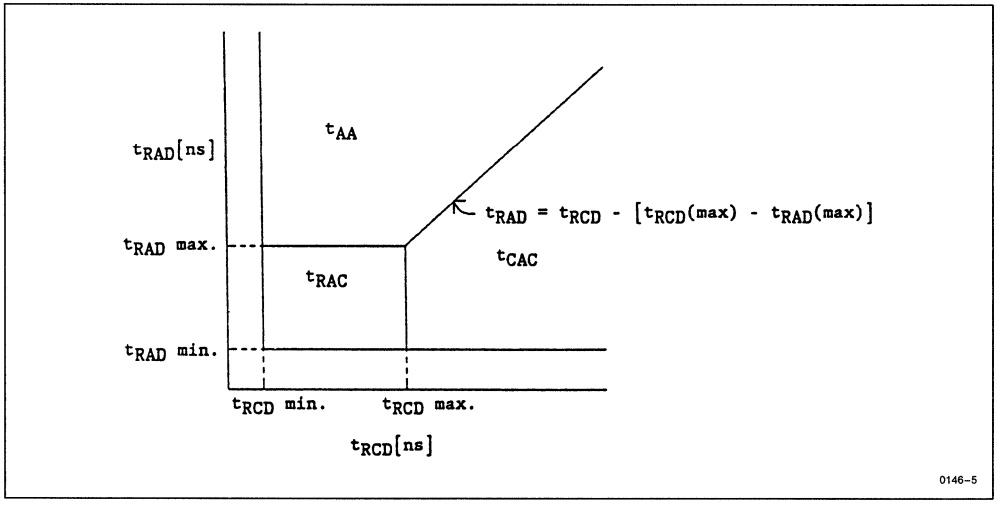
Counter Test Cycle

Parameter	Symbol	HM511665-8 HM511665L-8		HM511665-10 HM511665L-10		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	40	—	ns	

Write Per Bit Cycle[16, 17]

Parameter	Symbol	HM511665-8 HM511665L-8		HM511665-10 HM511665L-10		Unit	Note
		Min	Max	Min	Max		
Write per Bit Setup Time	t_{WBS}	0	—	0	—	ns	
Write per Bit Hold Time	t_{WBH}	10	—	10	—	ns	
Write per Bit Selection Setup Time	t_{WDS}	0	—	0	—	ns	
Write per Bit Selection Hold Time	t_{WDH}	10	—	10	—	ns	

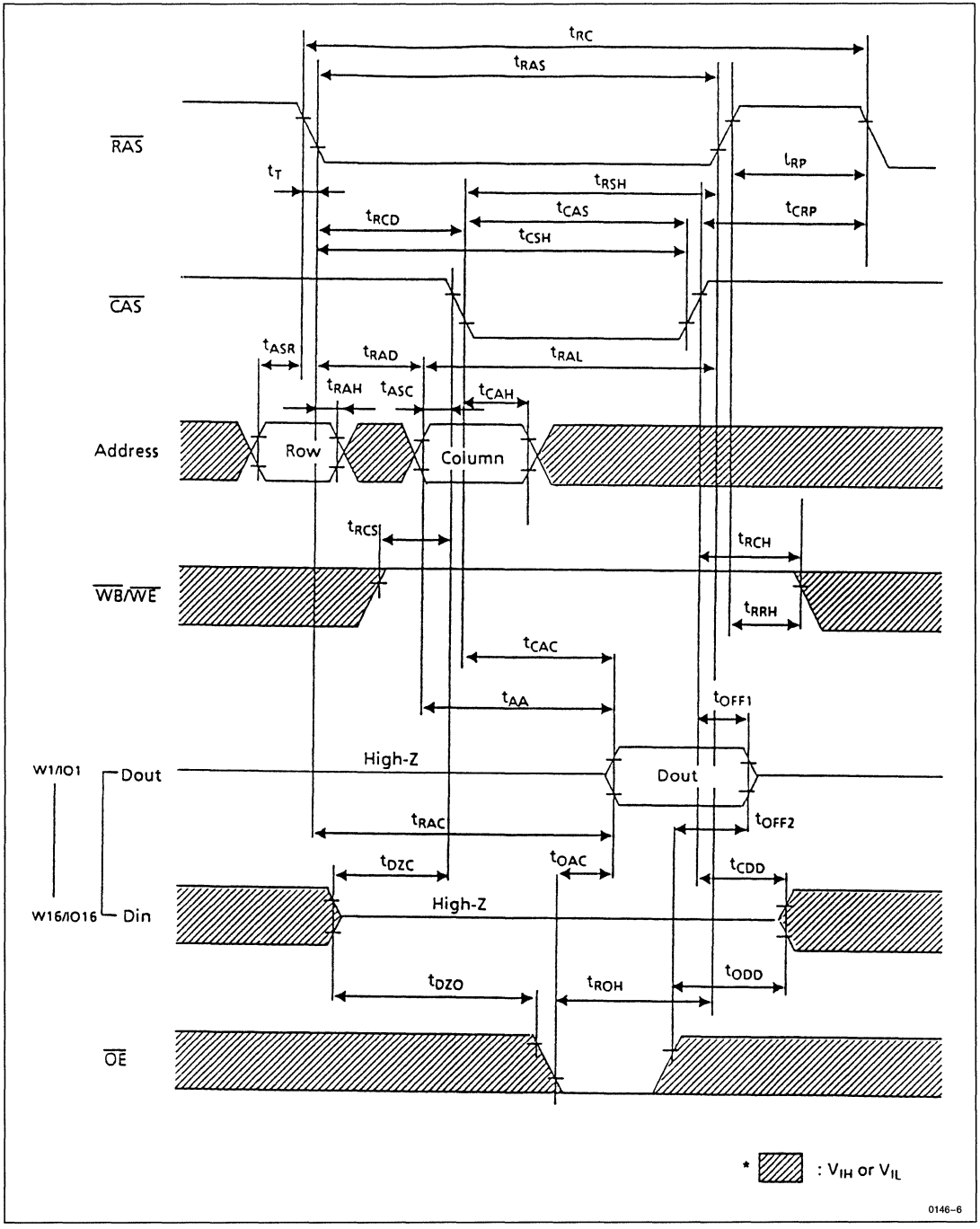
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 1 TTL load and 50 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $(t_{RCD} - t_{RAD}) \geq [t_{RCD}$ (max) $- t_{RAD}$ (max)].
5. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $(t_{RCD} - t_{RAD}) \leq [t_{RCD}$ (max) $- t_{RAD}$ (max)]. t_{RAC}, t_{CAC}, and t_{AA} are determined as follows:



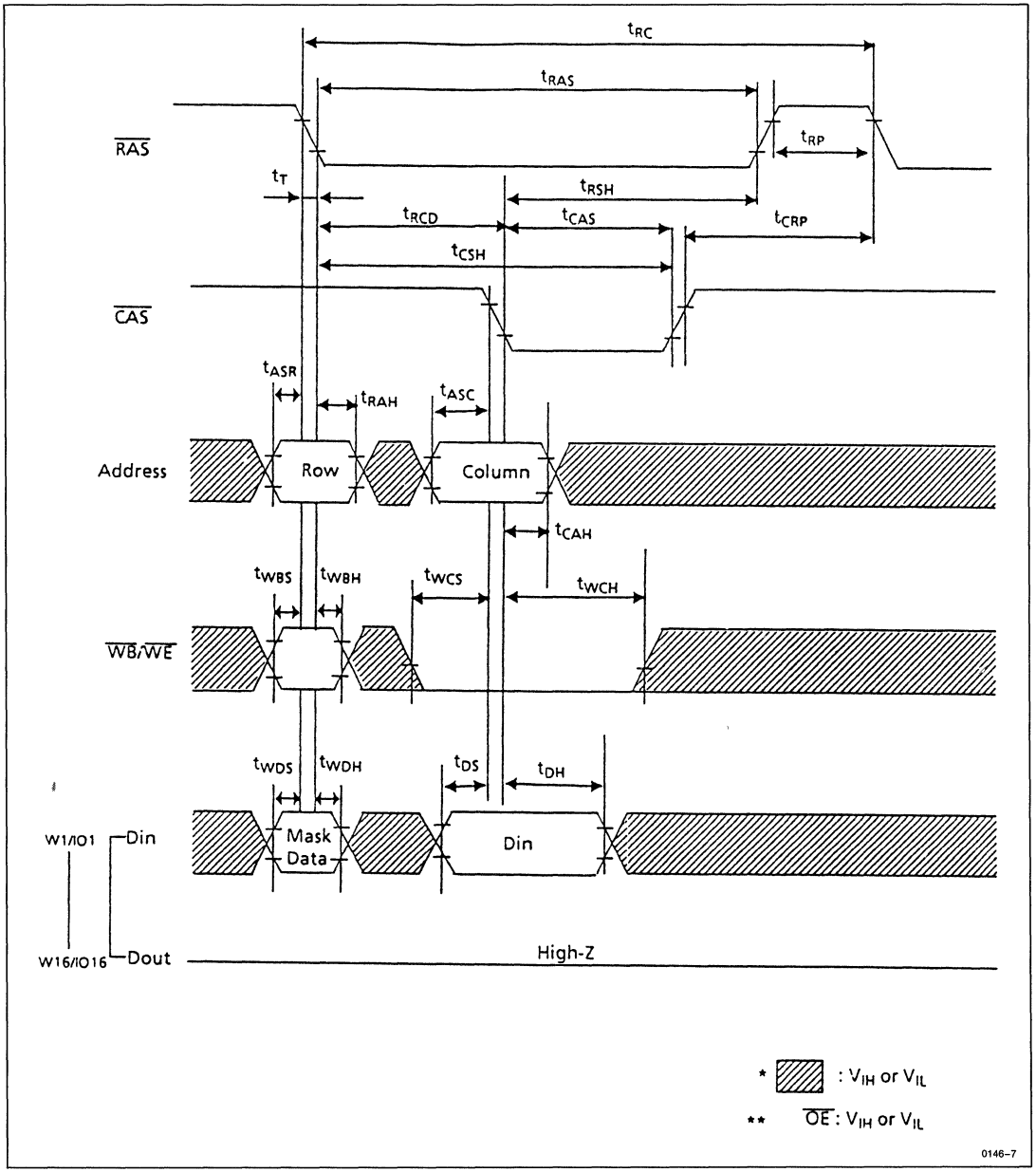
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. When using the write-per-bit capability, $\overline{WB}/\overline{WE}$ must be low as $\overline{RAS}$ falls.
17. The data bits to which the write operation is applied can be specified by keeping Wi/IOi high with setup and hold time referenced to the $\overline{RAS}$ negative transition.

■ TIMING WAVEFORMS

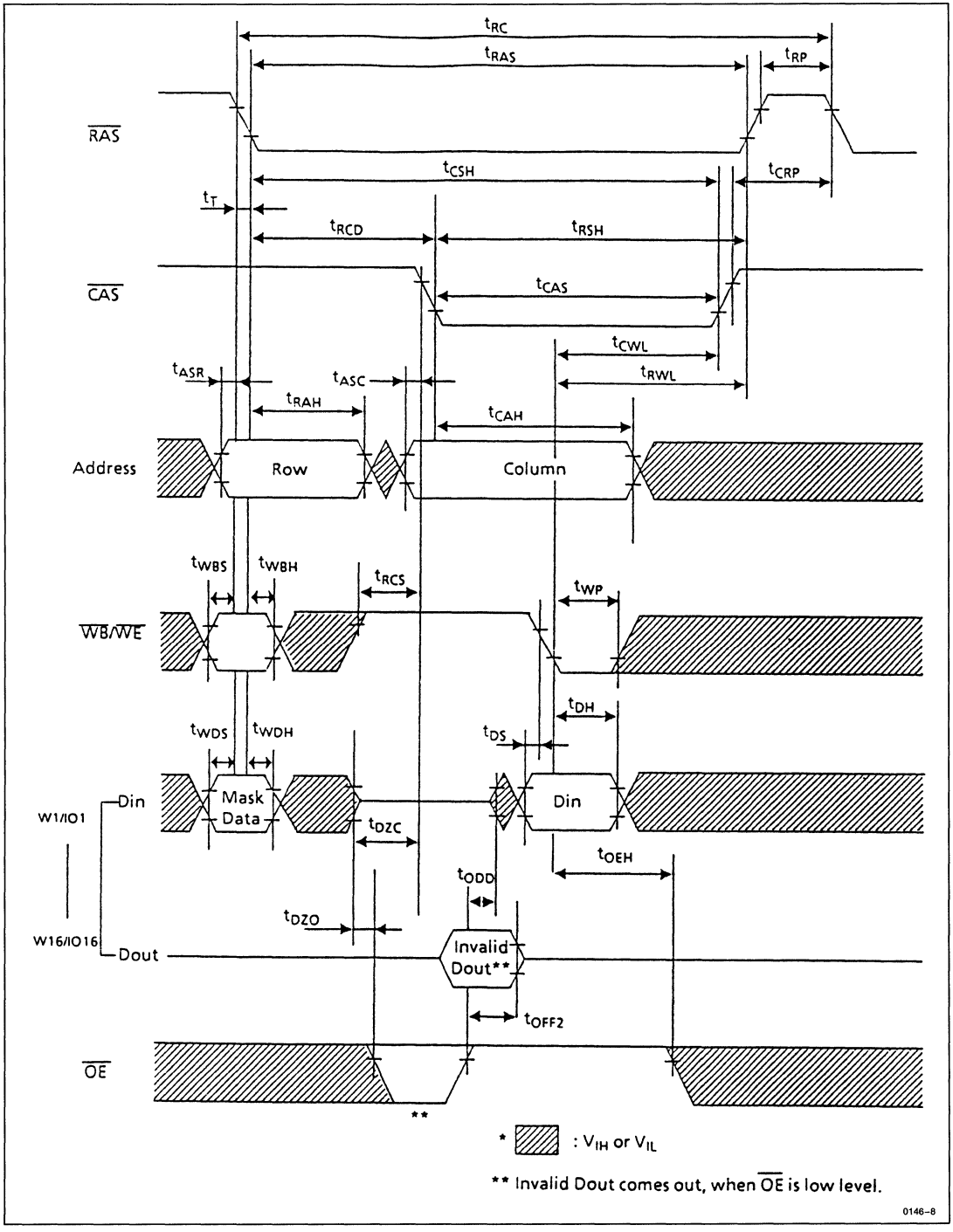
• Read Cycle



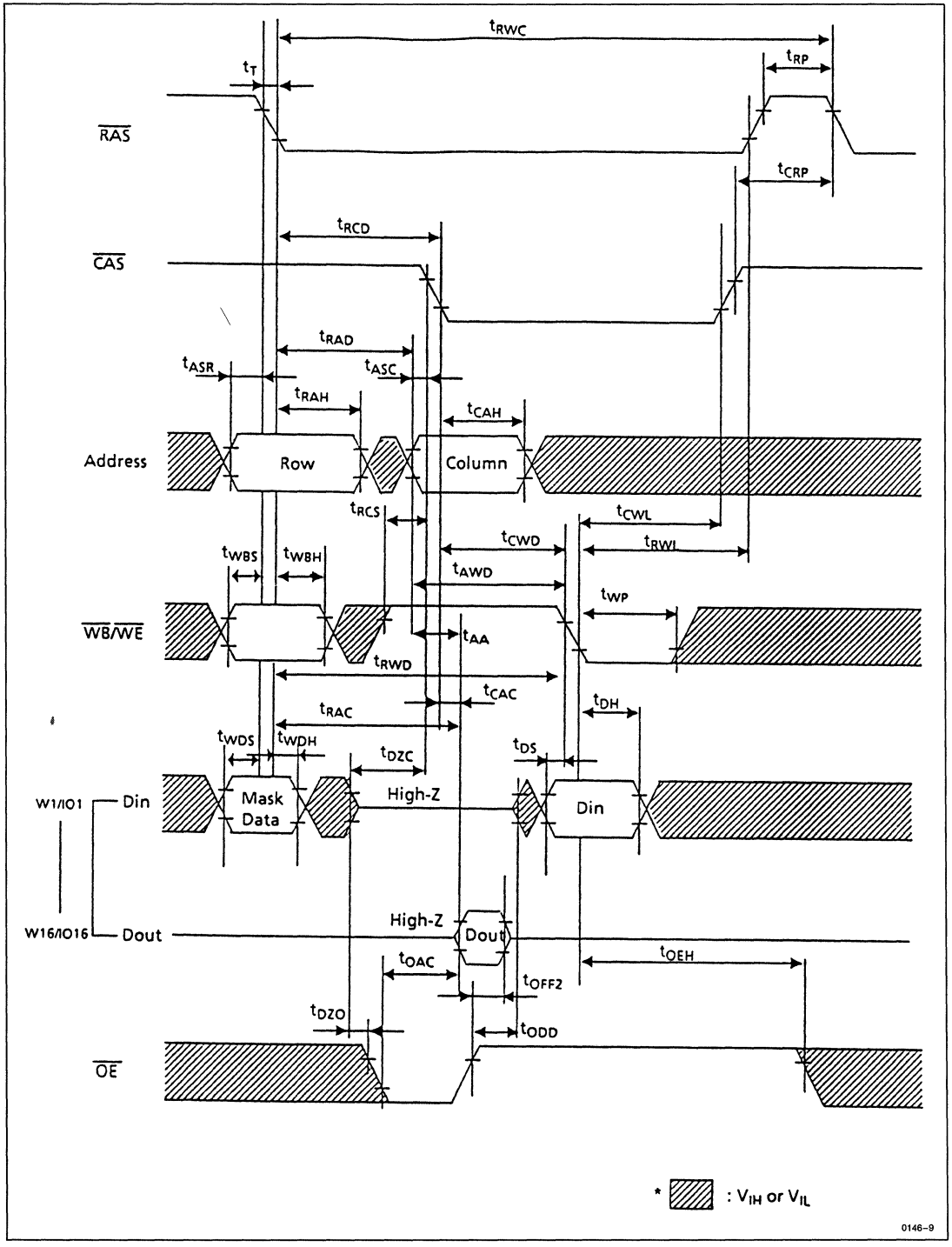
• **Early Write Cycle**



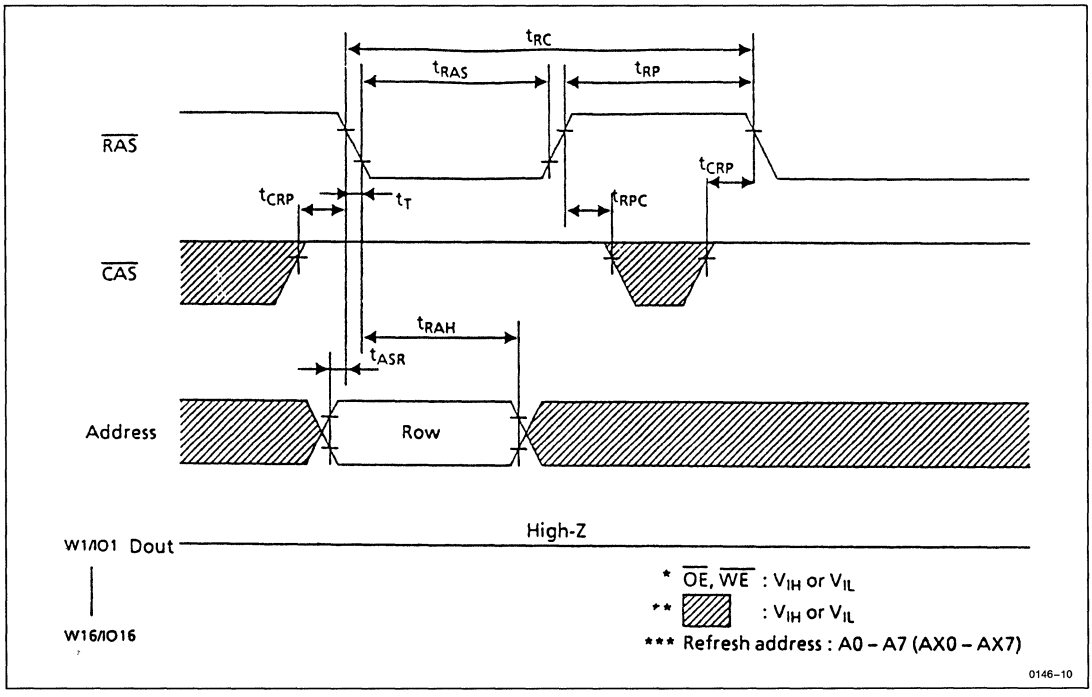
• **Delayed Write Cycle**



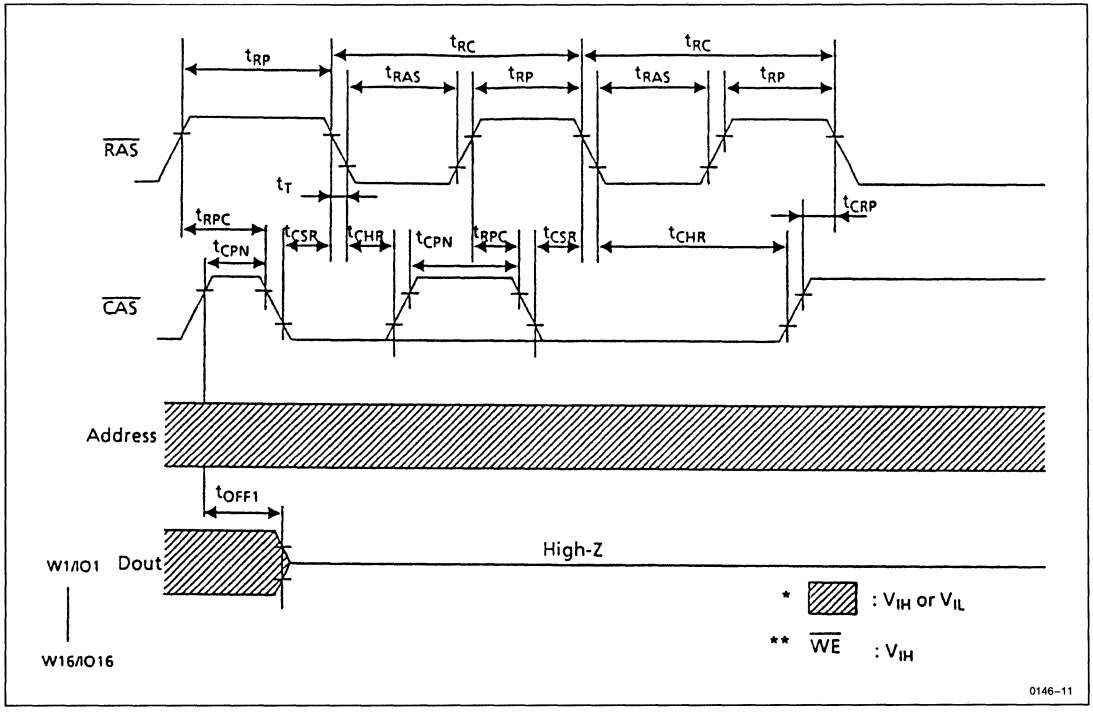
• **Read-Modify-Write Cycle**



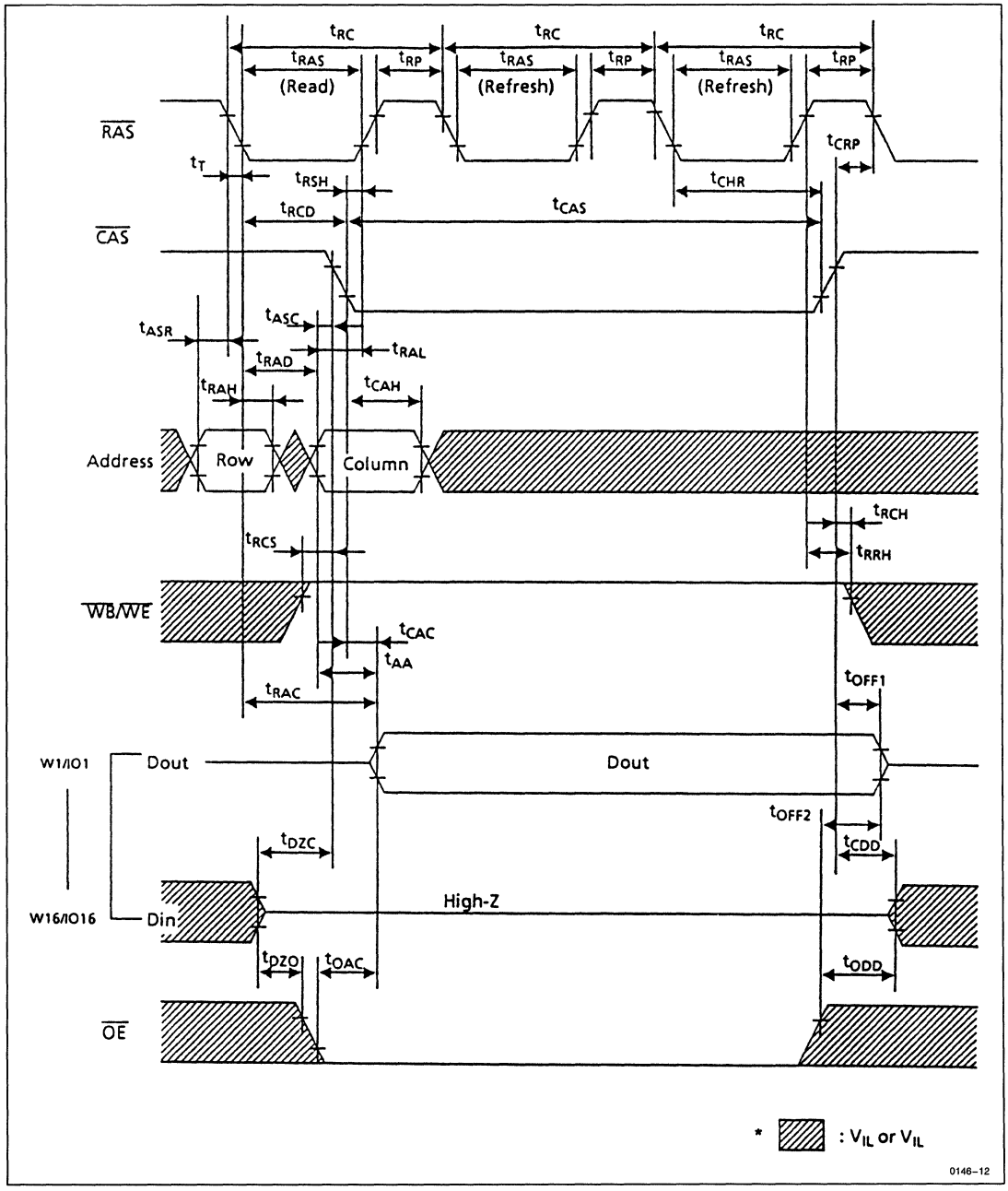
• $\overline{RAS}$ Only Refresh Cycle



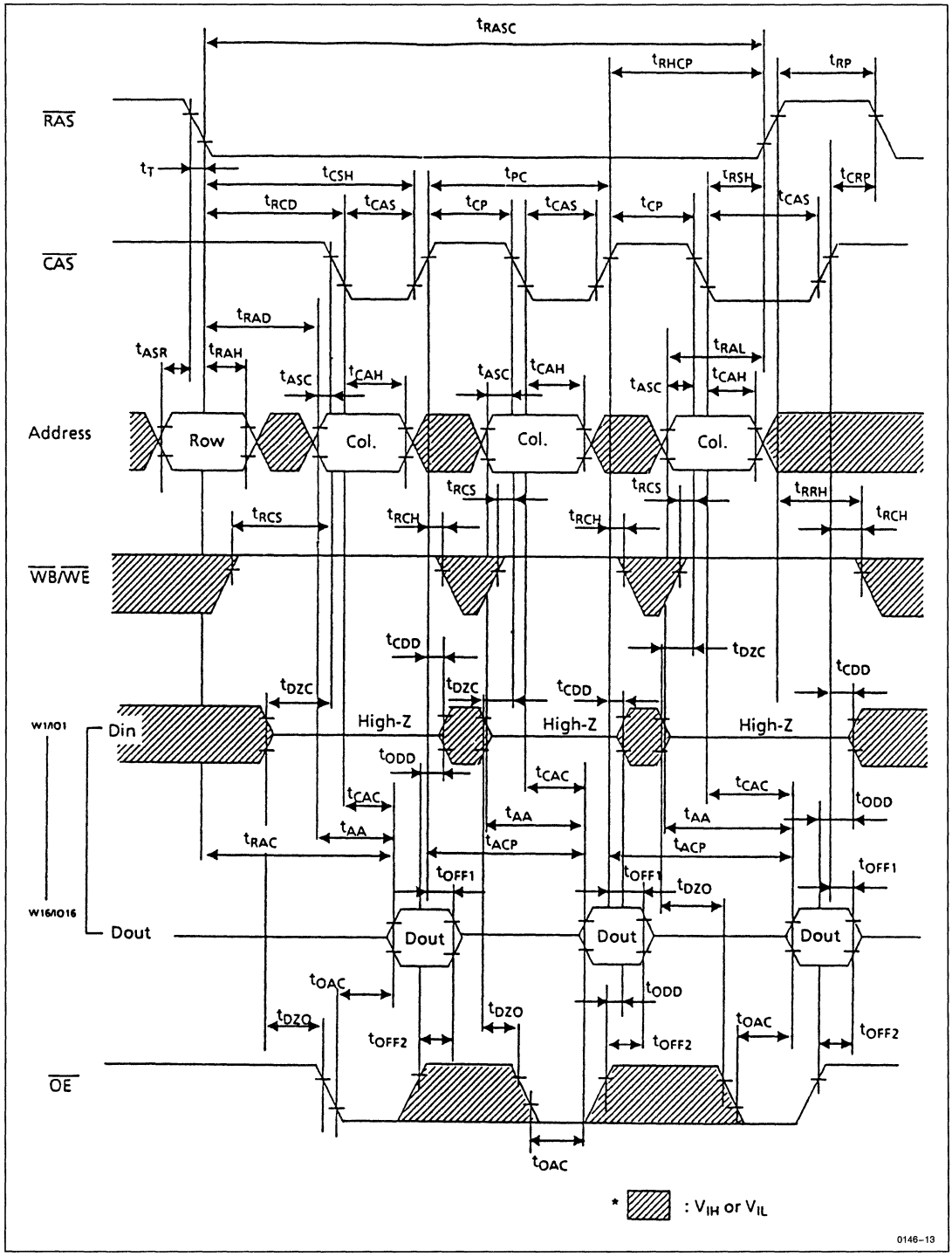
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



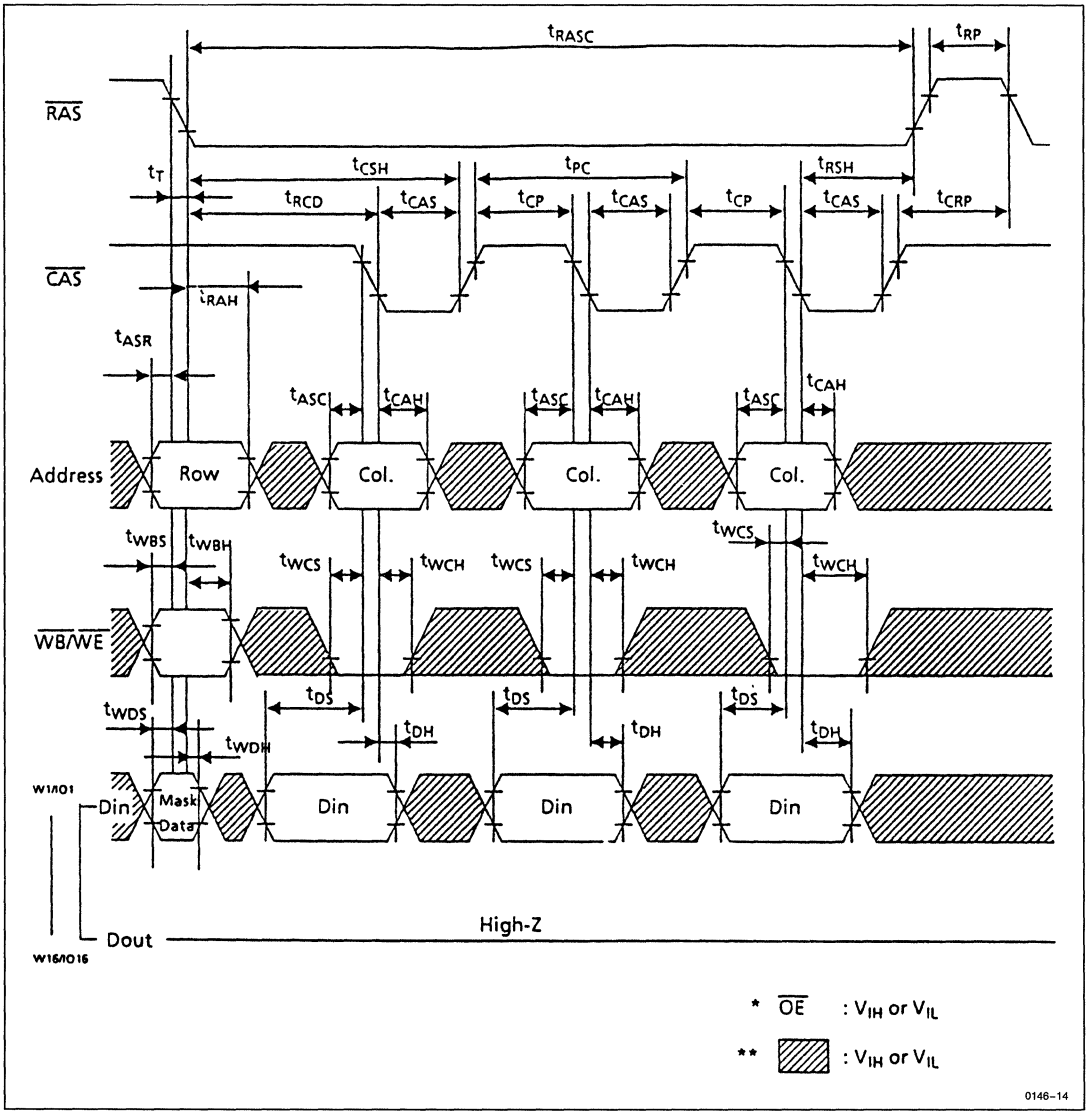
• **Hidden Refresh Cycle**



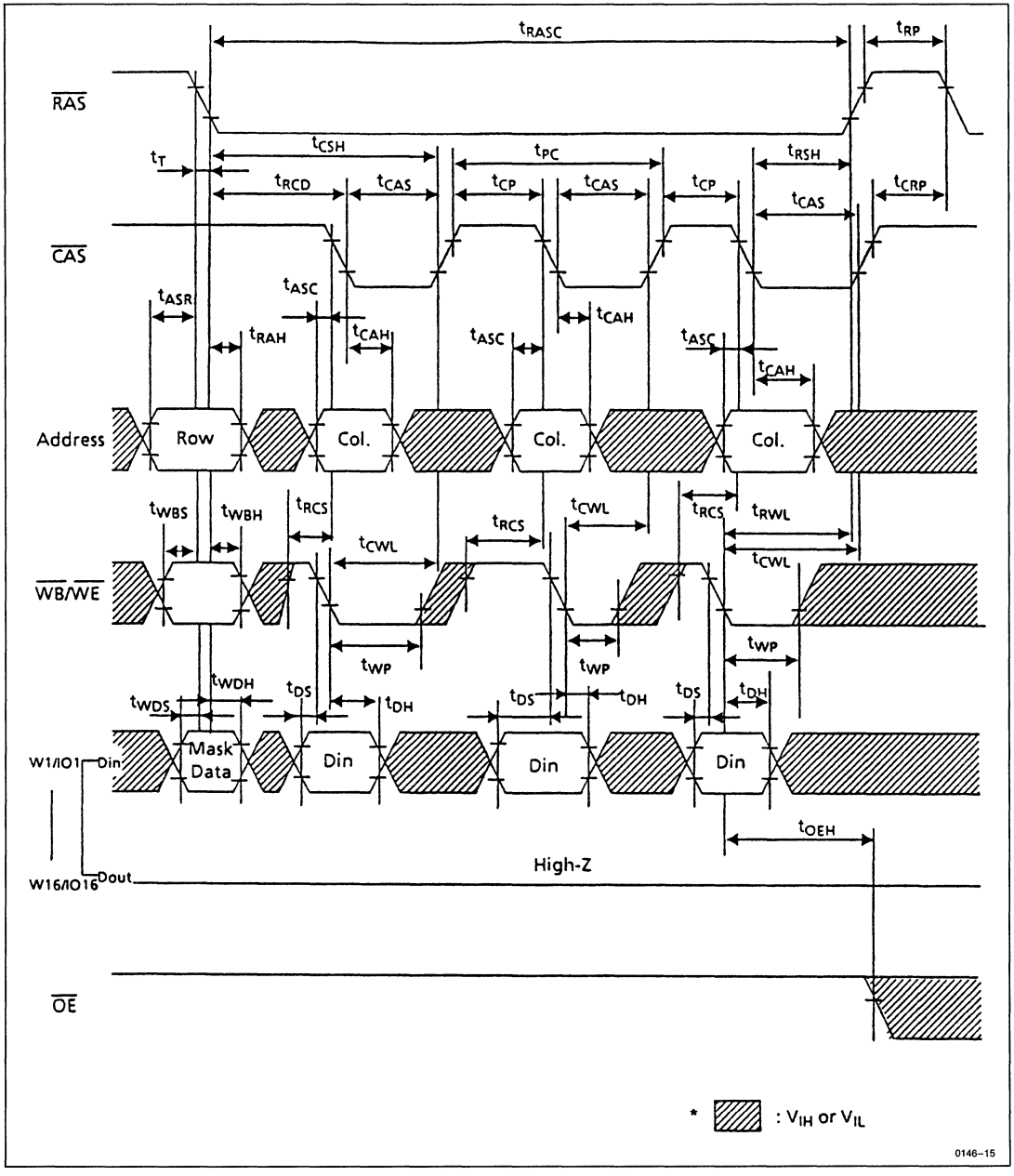
• **Fast Page Mode Read Cycle**



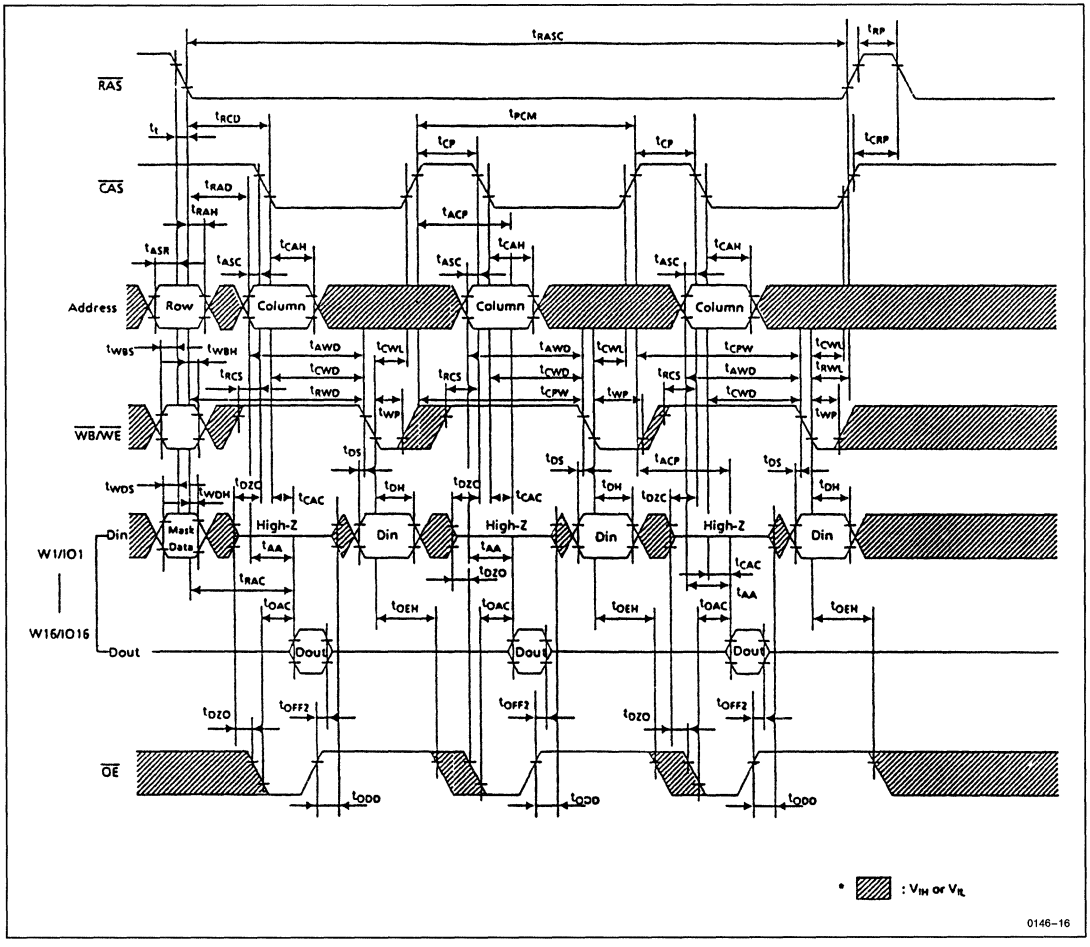
• **Fast Page Mode Early Write Cycle**



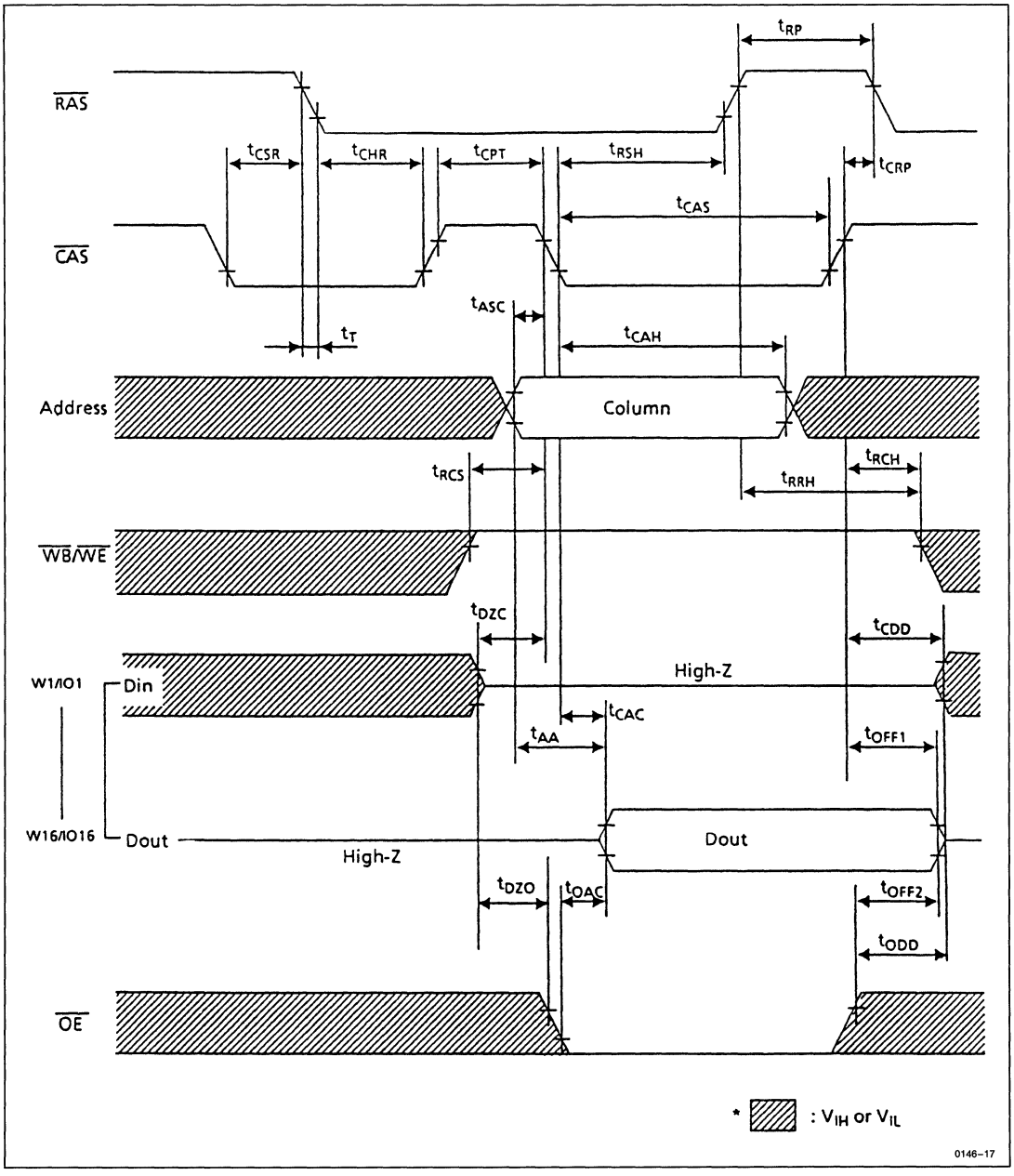
• **Fast Page Mode Delayed Write Cycle**



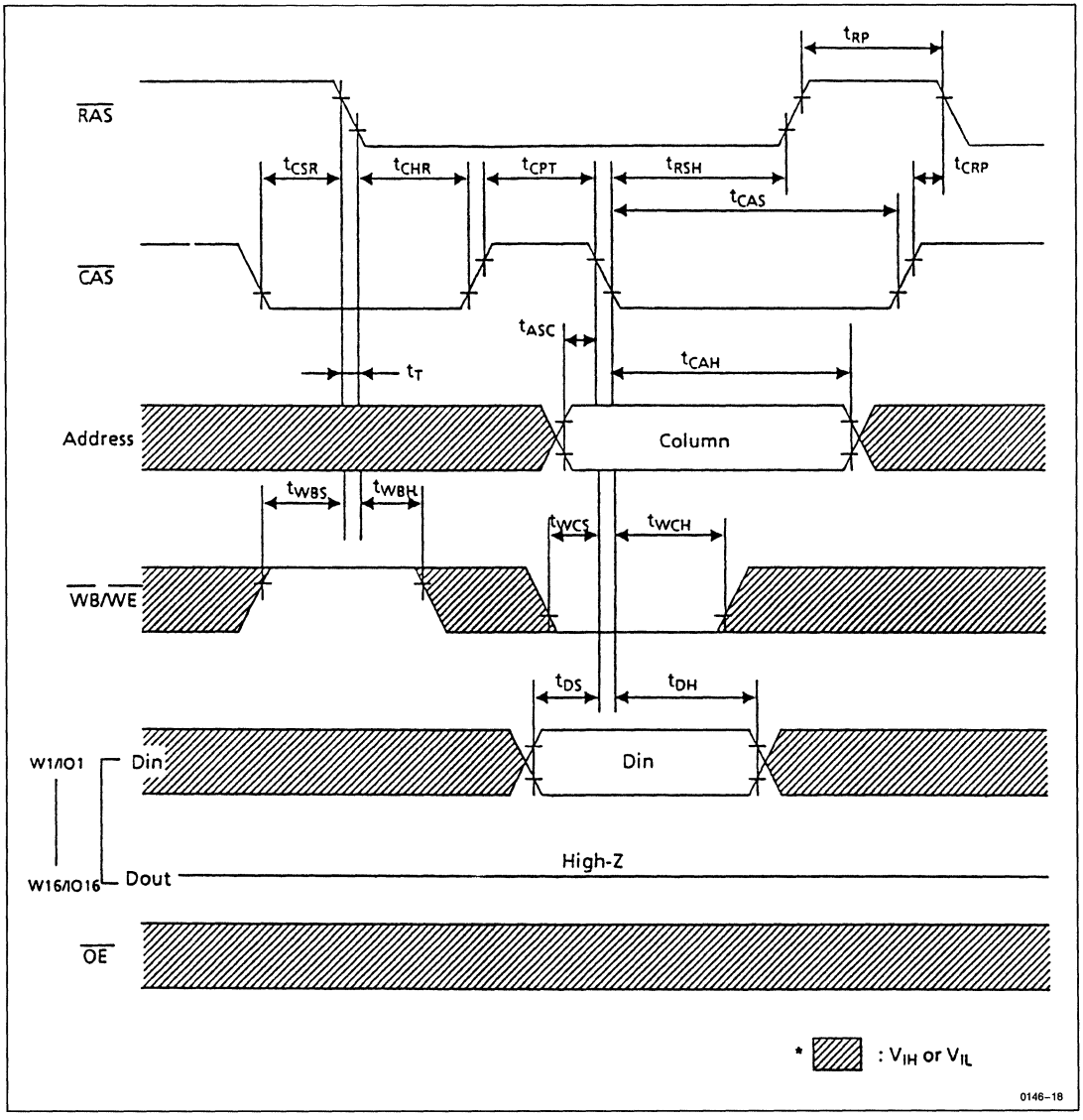
• Fast Page Mode Read-Modify-Write Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM511666 Series

Preliminary

65,536-Word x 16-Bit Dynamic RAM

■ DESCRIPTION

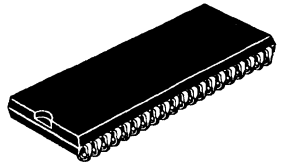
The Hitachi HM511666 are CMOS dynamic RAM organized as 65,536-word x 16-bit. HM511666 have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM511666 offers Static Column Mode as a high speed access mode.

Multiplexed address input permits the HM511666 to be packaged in standard 400 mil 40-pin plastic SOJ, standard 475 mil 40-pin plastic ZIP.

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode.....633 mW/495 mW (max)
  - Standby Mode.....11 mW (max)
- Static Column Mode Capability
- Byte Write Capability
- 256 Refresh Cycles .....(4 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CS}$ Before $\overline{RAS}$ Refresh

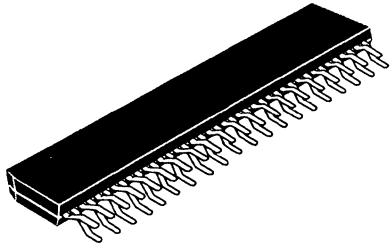
HM511666JP Series



3DCP40D

(CP-40D)

HM511666ZP Series



3DZP40

(ZP-40)

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM511666JP-8 HM511666JP-10	80 ns 100 ns	400 mil 40-pin Plastic SOJ (CP-40D)
HM511666ZP-8 HM511666ZP-10	80 ns 100 ns	475 mil 40-pin Plastic ZIP (ZP-40)

■ PIN DESCRIPTION

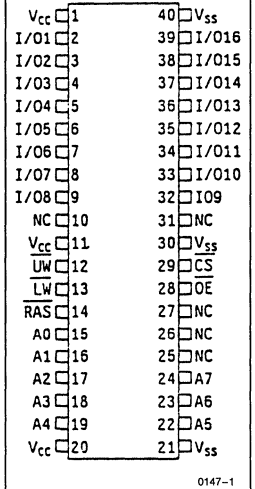
Pin Name	Function
A_0–A_7	Address Input Refresh Address Input
I/O_1–I/O_{16}	Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
$\overline{UW}$	Read/Upper Byte Write Enable
$\overline{LW}$	Read/Lower Byte Write Enable
$\overline{OE}$	Output Enable
V_{CC}*1	Power (+5V)
V_{SS}*2	Ground
NC	No Connection

Notes: 1. This device has 3 V_{CC} pins (SOJ: 1, 11, 20 pin/ZIP: 13, 21, 30 pin). All V_{CC} pins must be connected with the same power-supply wiring on the memory board.

2. This device has 3 V_{SS} pins (SOJ: 21, 30, 40 pin/ ZIP: 10, 33, 40 pin). All V_{SS} pins must be connected with the same ground wiring on the memory board.

■ PIN OUT

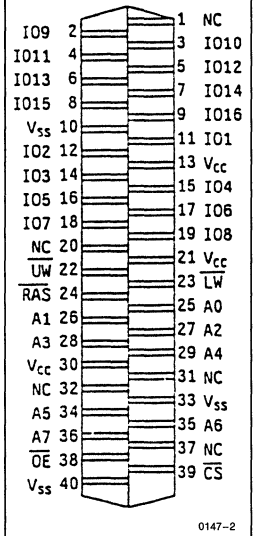
HM511666JP Series



0147-1

(Top View)

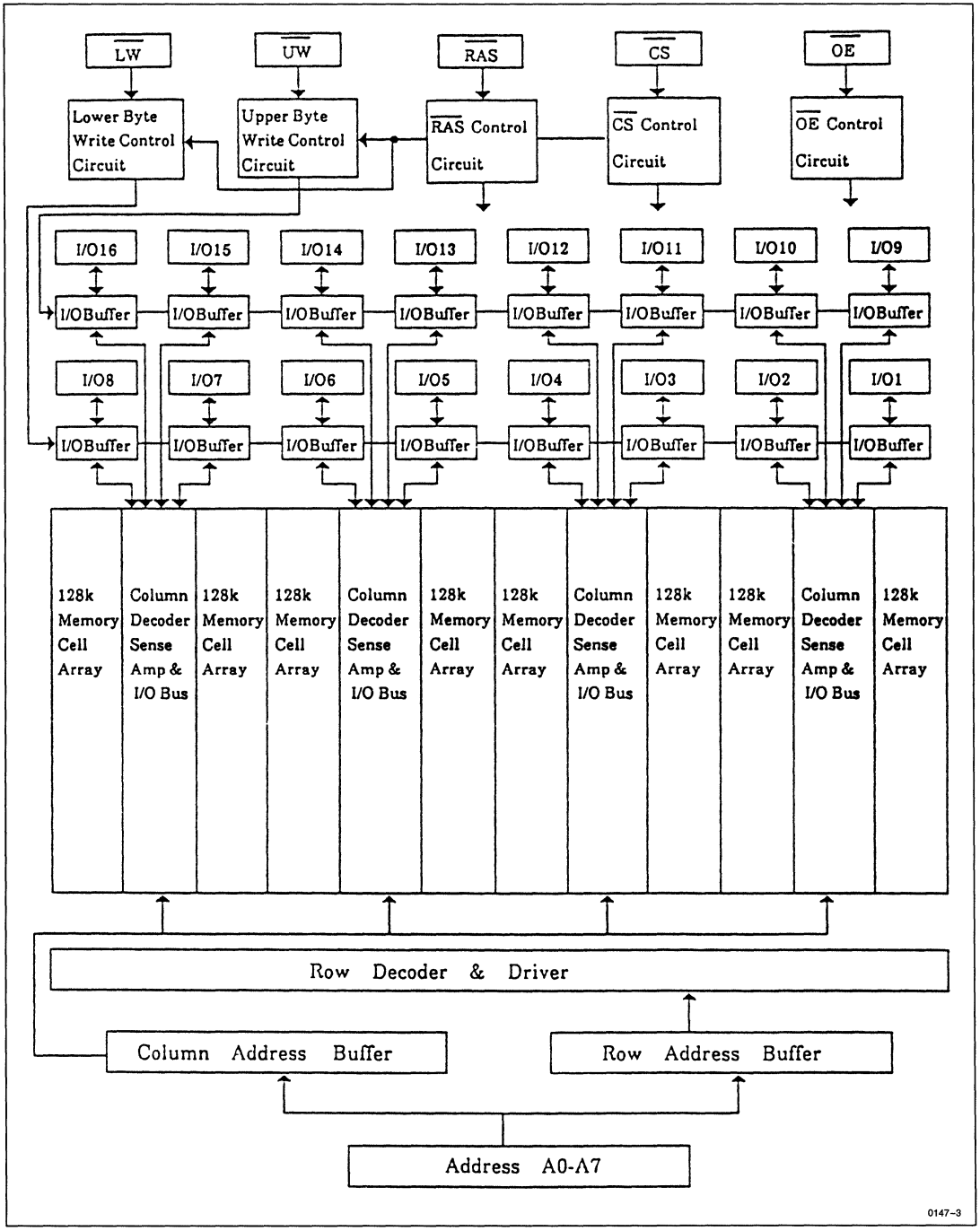
HM511666ZP Series



0147-2

(Bottom View)

■ BLOCK DIAGRAM



■ TRUTH TABLE

Inputs					I/O		Operation
$\overline{RAS}$	$\overline{CS}$	$\overline{LW}$	$\overline{UW}$	$\overline{OE}$	I/O_1–I/O_8	I/O_9–I/O_{16}	
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	D_{out}	D_{out}	Read
L	L	L	H	H	D_{in}	Don't Care	Lower Byte Write
L	L	H	L	H	Don't Care	D_{in}	Upper Byte Write
L	L	L	L	H	D_{in}	D_{in}	Word Write
L	L	L	L	H	High-Z	High-Z	

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	0.8	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/Oi Pin)	V_{IL}	−0.5	—	0.8	V	1, 2
	(Others)	V_{IL}	−1.0	—	0.8	V	1, 2

Notes: 1. All voltage referenced to V_{SS}.
2. The device will withstand undershoots to the −2V level with a maximum pulse width of 20 ns at the −1.5V level. (See figure 1.)

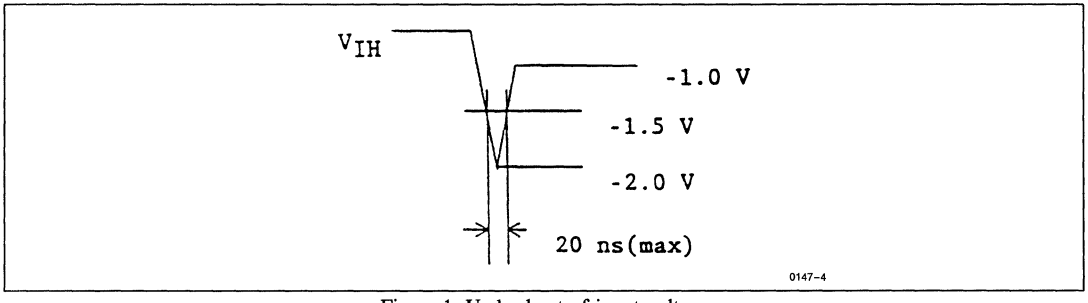


Figure 1. Undershoot of input voltage

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM511666-8		HM511666-10		Unit	Test Conditions	Note
		Min	Max	Min	Max			
Operating Current	I_{CC1}	—	115	—	90	mA	$\overline{RAS}$, $\overline{CS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	2				mA	TTL Interface $\overline{RAS}$, $\overline{CS}$ = V_{IH}, D_{out} = High-Z	4
		1				mA	CMOS Interface $\overline{RAS}$, $\overline{CS} \geq V_{CC} - 0.2V$, D_{out} = High-Z	4
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	115	—	90	mA	t_{RC} = Min	2
$\overline{CS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	115	—	90	mA	t_{RC} = Min	
Static Column Current	I_{CC9}	—	110	—	100	mA	t_{SC} = Min	1, 3
Input Leakage Current	I_{LI}	−10	10	−10	10	μA	$0V \leq V_{in} \leq 6.5V$	
Output Leakage Current	I_{LO}	−10	10	−10	10	μA	$0V \leq V_{out} \leq 5.5V$, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −2.5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	V	Low I_{out} = 2.1 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CS}$ = V_{IH}.
4. Clock voltages ($\overline{RAS}$ and $\overline{CS}$) must be applied simultaneously with or prior to applying supply voltage.

• Capacitance (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CS}$ = V_{IH} to disable D_{out}.

• AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 14, 15, 16]

Test Conditions

Input Rise and Fall Times	5 ns
Input Timing Reference Levels	0.8V, 2.4V
Output Load	1 TTL Gate + C_L (50 pF) (Including scope and jig)

Read, Write, and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM511666-8		HM511666-10		Unit	Note
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	135	—	170	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	45	—	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	ns	
$\overline{CS}$ Pulse Width	t_{SP}	30	10000	40	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{ASW}	0	—	0	—	ns	
Column Address Hold Time	t_{AHW}	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RCD}	20	50	20	60	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	15	45	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	30	—	40	—	ns	
$\overline{CS}$ Hold Time	t_{CSH}	80	—	100	—	ns	
$\overline{CS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	15	—	15	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	ns	
$\overline{CS}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	4	—	4	ms	

Read Cycle

Parameter	Symbol	HM511666-8		HM511666-10		Unit	Note
		Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	ns	2, 3
Access Time from $\overline{CS}$	t_{ACS}	—	30	—	40	ns	3, 4, 13
Access Time from Address	t_{AA}	—	45	—	55	ns	3, 5, 13
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	40	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time to $\overline{CS}$	t_{RCH}	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	20	0	20	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	15	0	15	ns	6
$\overline{CS}$ to D_{in} Delay Time	t_{CDD}	20	—	20	—	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	t_{ROH}	10	—	10	—	ns	
$\overline{RAS}$ to Column Address Hold Time	t_{AHR}	15	—	15	—	ns	17
Output Hold Time from Address	t_{AOH}	5	—	5	—	ns	
Column Address Hold Time to $\overline{RAS}$ on Read	t_{AR}	80	—	100	—	ns	

Write Cycle

Parameter	Symbol	HM511666-8		HM511666-10		Unit	Note
		Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	ns	
Write Command to $\overline{CS}$ Lead Time	t_{CWL}	20	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	ns	11
Data-in Hold time to $\overline{RAS}$	t_{DHR}	65	—	75	—	ns	
Column Address Hold Time to $\overline{RAS}$ on Write	t_{AWR}	65	—	75	—	ns	
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	15	—	15	—	ns	

Refresh Cycle

Parameter	Symbol	HM511666-8		HM511666-10		Unit	Note
		Min	Max	Min	Max		
$\overline{CS}$ Setup Time ($\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CS}$ Hold Time ($\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CS}$ Hold Time	t_{ZRH}	10	—	10	—	ns	
$\overline{CS}$ Precharge Time in Normal Mode	t_{SIN}	10	—	10	—	ns	

Static Column Mode Cycle

Parameter	Symbol	HM511666-8		HM511666-10		Unit	Note
		Min	Max	Min	Max		
Static Column Mode Cycle Time	t_{SC}	50	—	60	—	ns	
Static Column Mode $\overline{CS}$ Precharge Time	t_{SI}	10	—	10	—	ns	
Static Column Mode $\overline{RAS}$ Pulse Width	t_{RASC}	80	100000	100	100000	ns	12
$\overline{RAS}$ to Second $\overline{WE}$ Delay Time	t_{RSWD}	80	—	100	—	ns	
Write Invalid Time	t_{WI}	10	—	10	—	ns	

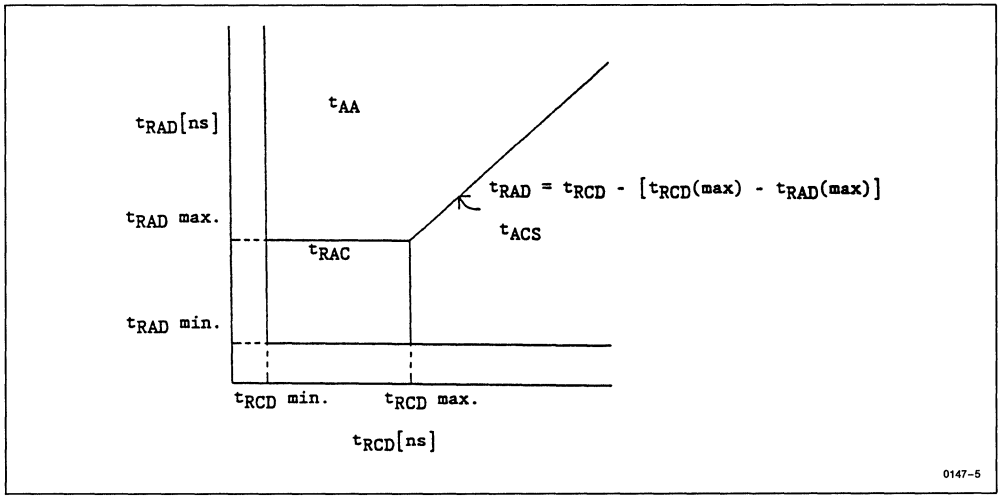
Counter Test Cycle

Parameter	Symbol	HM511666-8		HM511666-10		Unit	Note
		Min	Max	Min	Max		
$\overline{CS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	40	—	ns	

Byte Write Mode

Parameter	Symbol	HM511666-8		HM511666-10		Unit	Note
		Min	Max	Min	Max		
Masked Write Setup Time	t_{MCS}	0	—	0	—	ns	
Masked Write Hold Time Referenced to $\overline{RAS}$	t_{MRH}	0	—	0	—	ns	
Masked Write Hold Time Referenced to $\overline{CS}$	t_{MCH}	0	—	0	—	ns	

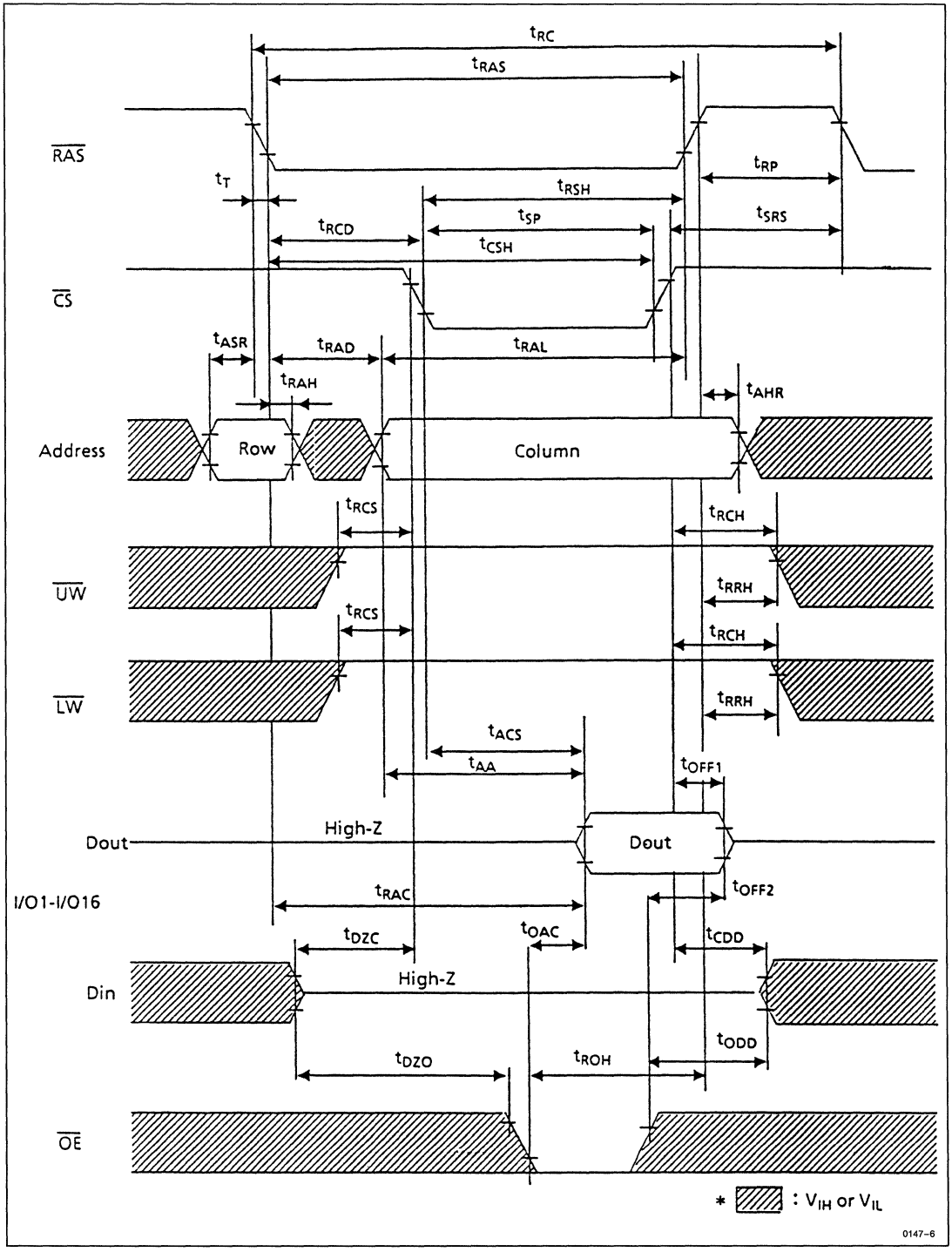
Notes: 1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 1TTL load and 50 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $(t_{RCD} - t_{RAD}) \geq [t_{RCD}$ (max) $- t_{RAD}$ (max)].
5. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $(t_{RCD} - t_{RAD}) \leq [t_{RCD}$ (max) $- t_{RAD}$ (max)]. t_{RAC}, t_{ACS}, and t_{AA} are determined as follows.



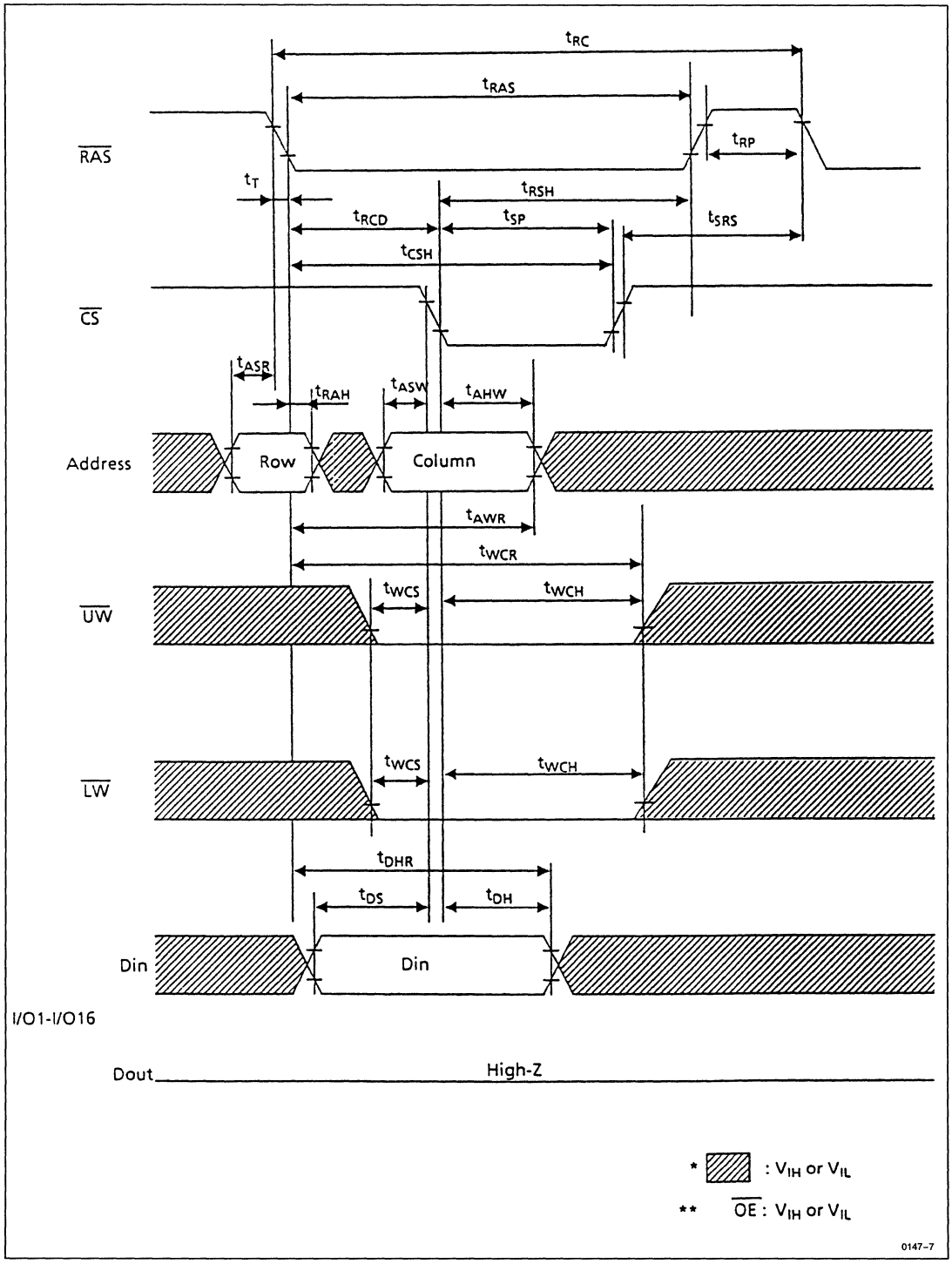
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{ACS}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS} is not restrictive operating parameter. It is included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
11. These parameters are referenced to $\overline{CS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in static column mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC}.
14. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. When both $\overline{LW}$ and $\overline{UW}$ go low at the same time, all 16 bits data are written into the device. $\overline{LW}$ and $\overline{UW}$ cannot be staggered within the same write cycle.
17. t_{AHR} defines the time at which the column addresses hold.

■ TIMING WAVEFORMS

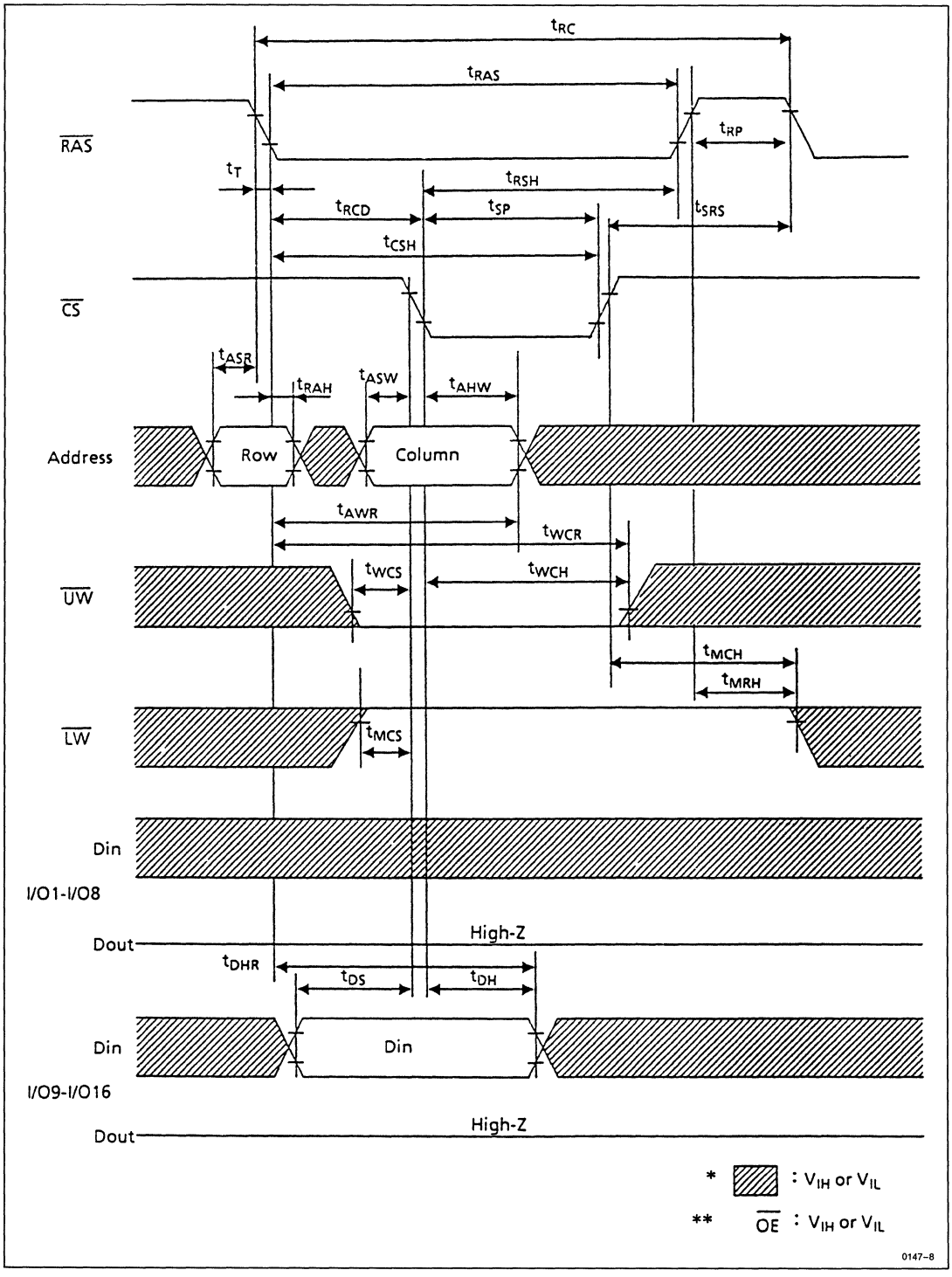
• Read Cycle



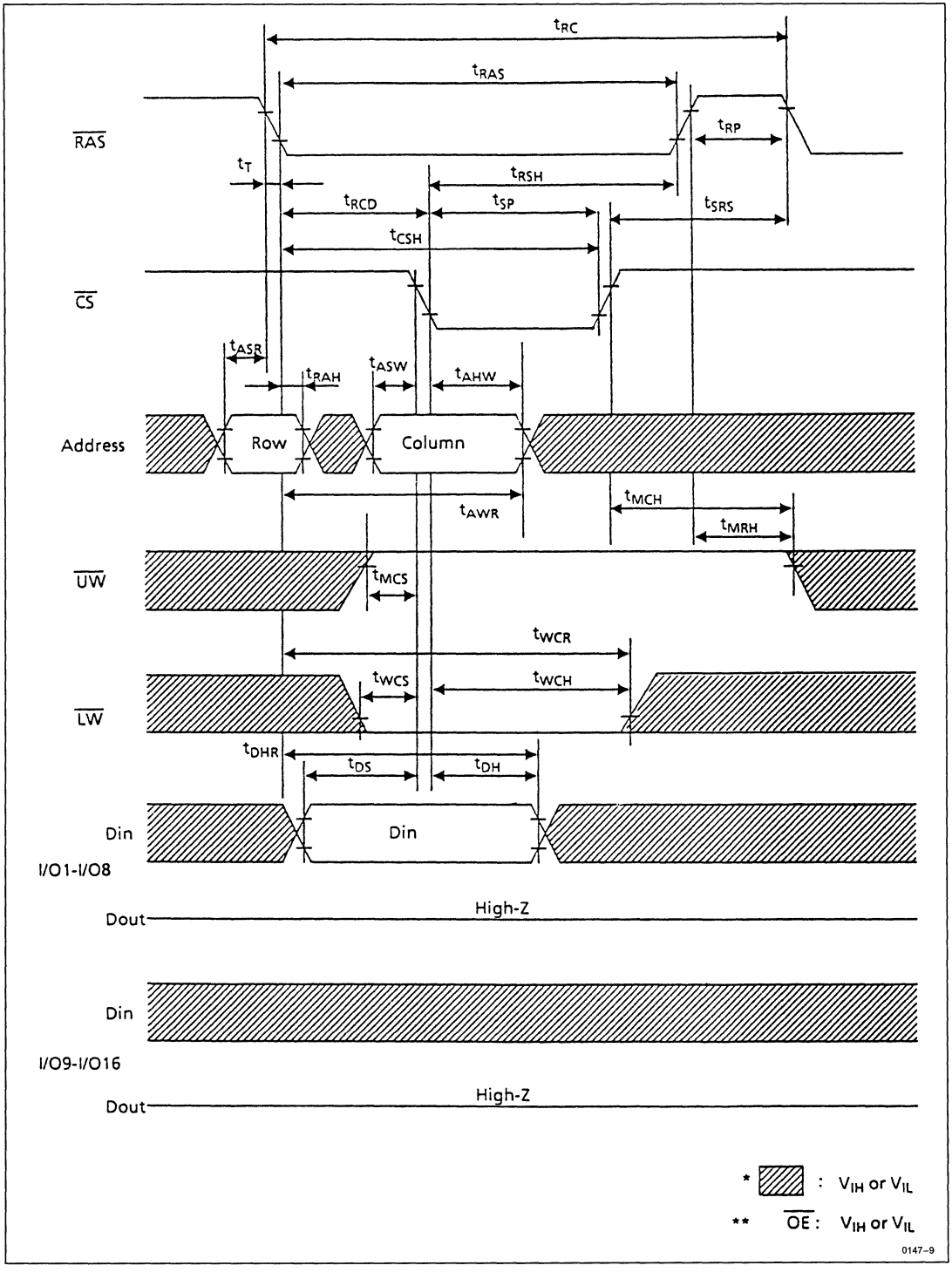
• **Early Write Cycle**



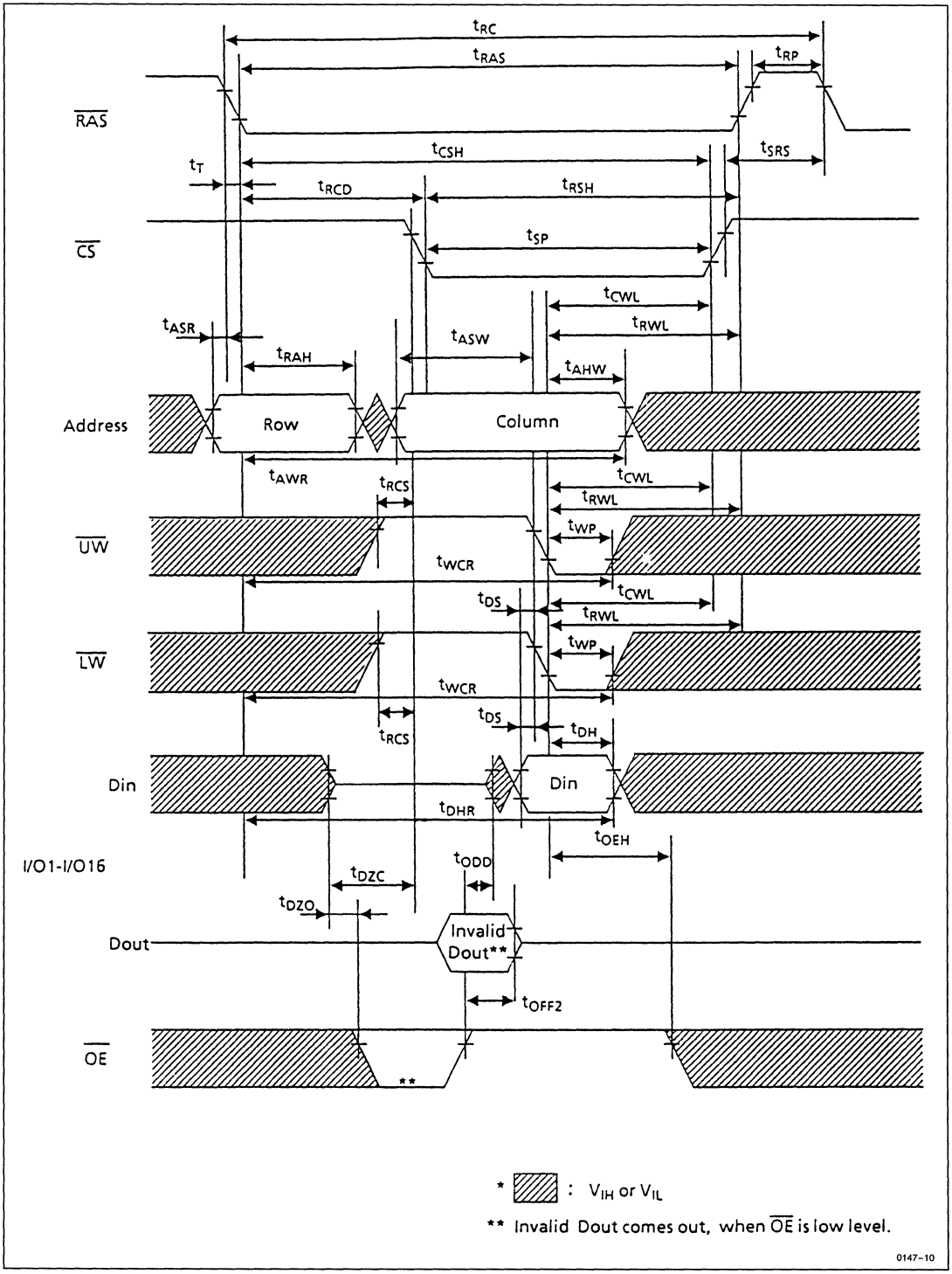
• **Upper Byte Early Write Cycle**



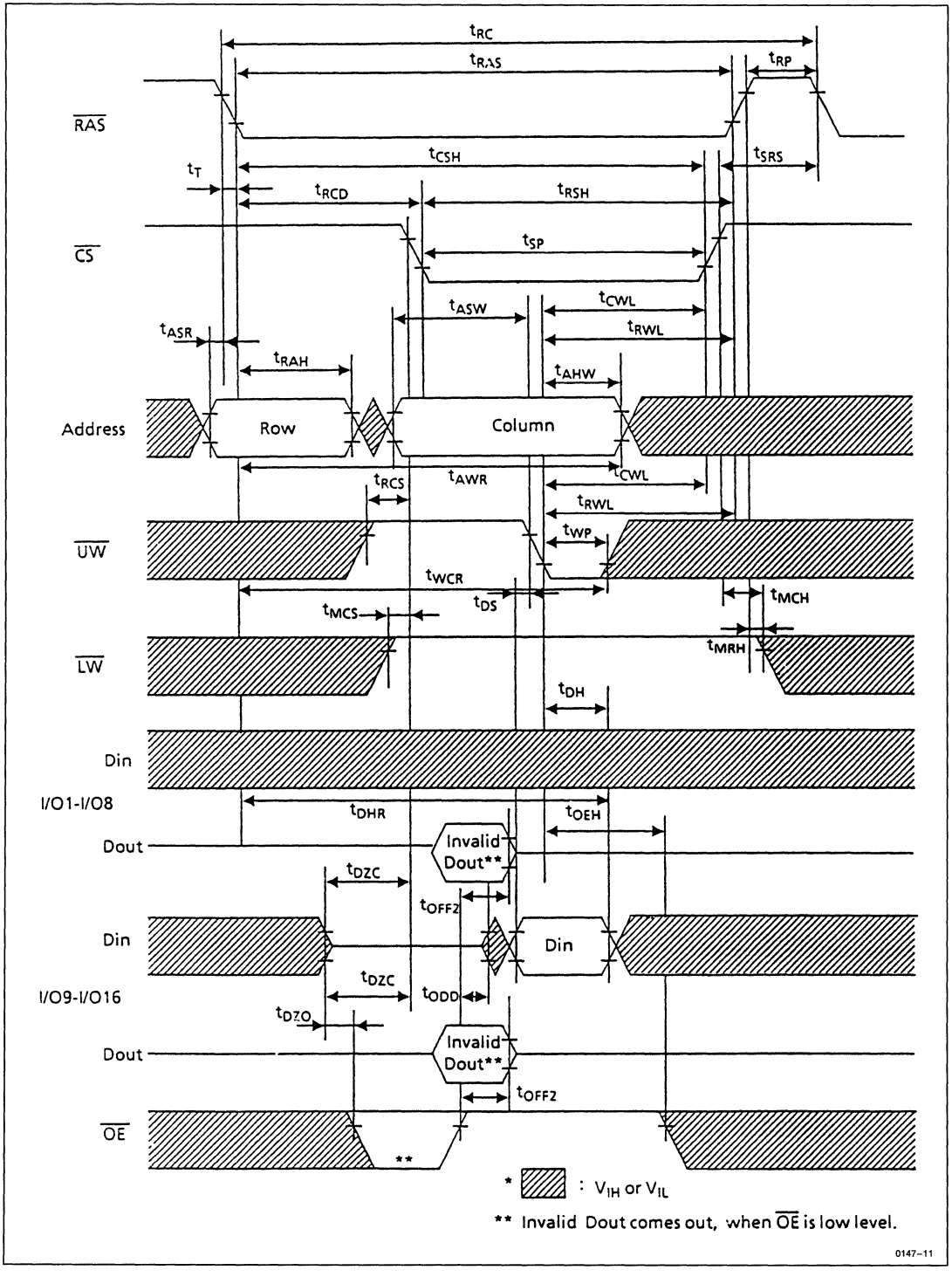
• **Lower Byte Early Write Cycle**



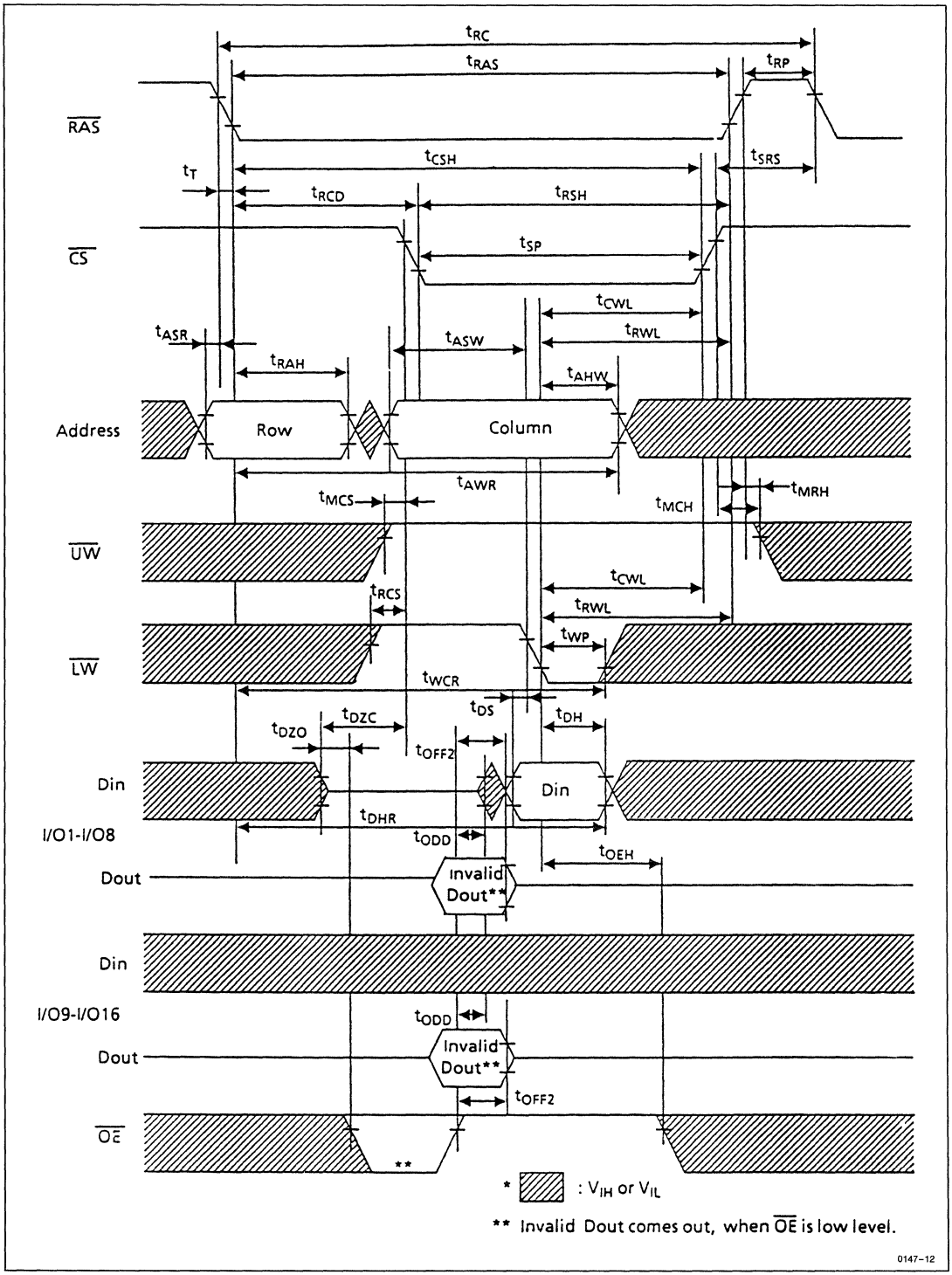
• **Delayed Write Cycle**



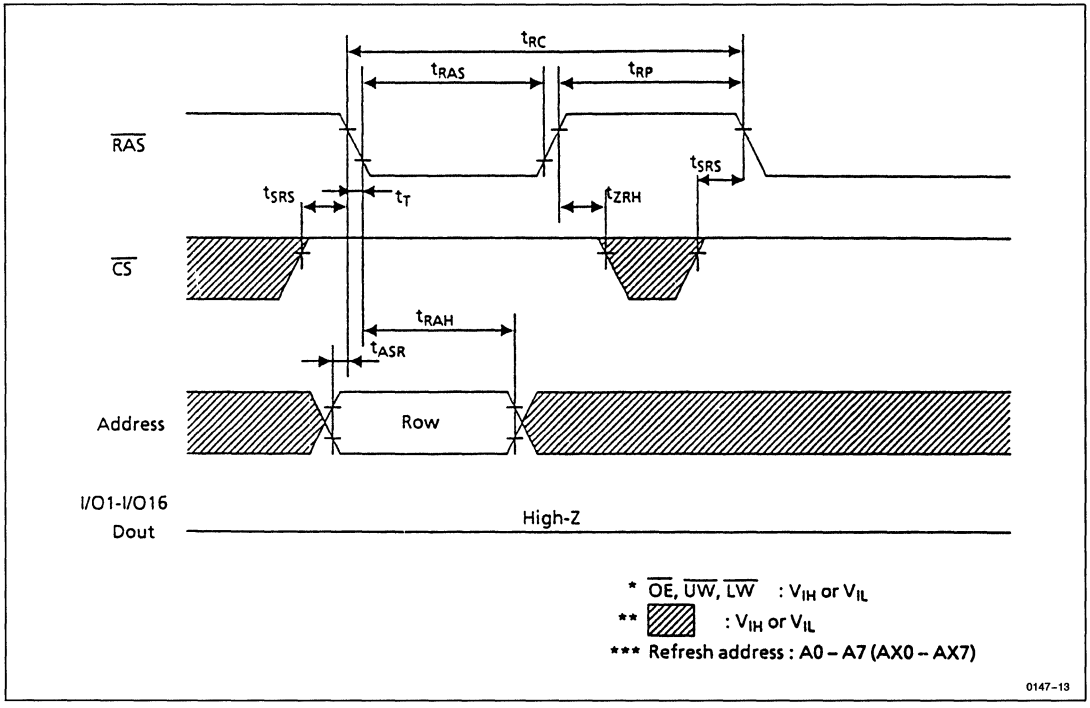
• **Upper Byte Delayed Write Cycle**



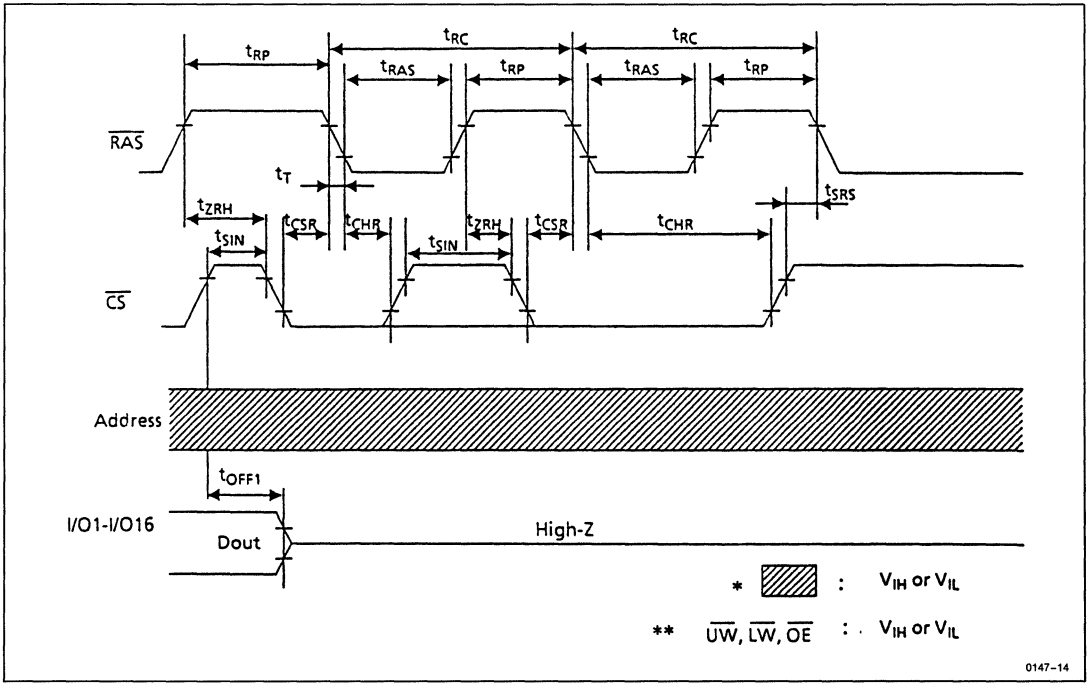
• **Lower Byte Delayed Write Cycle**



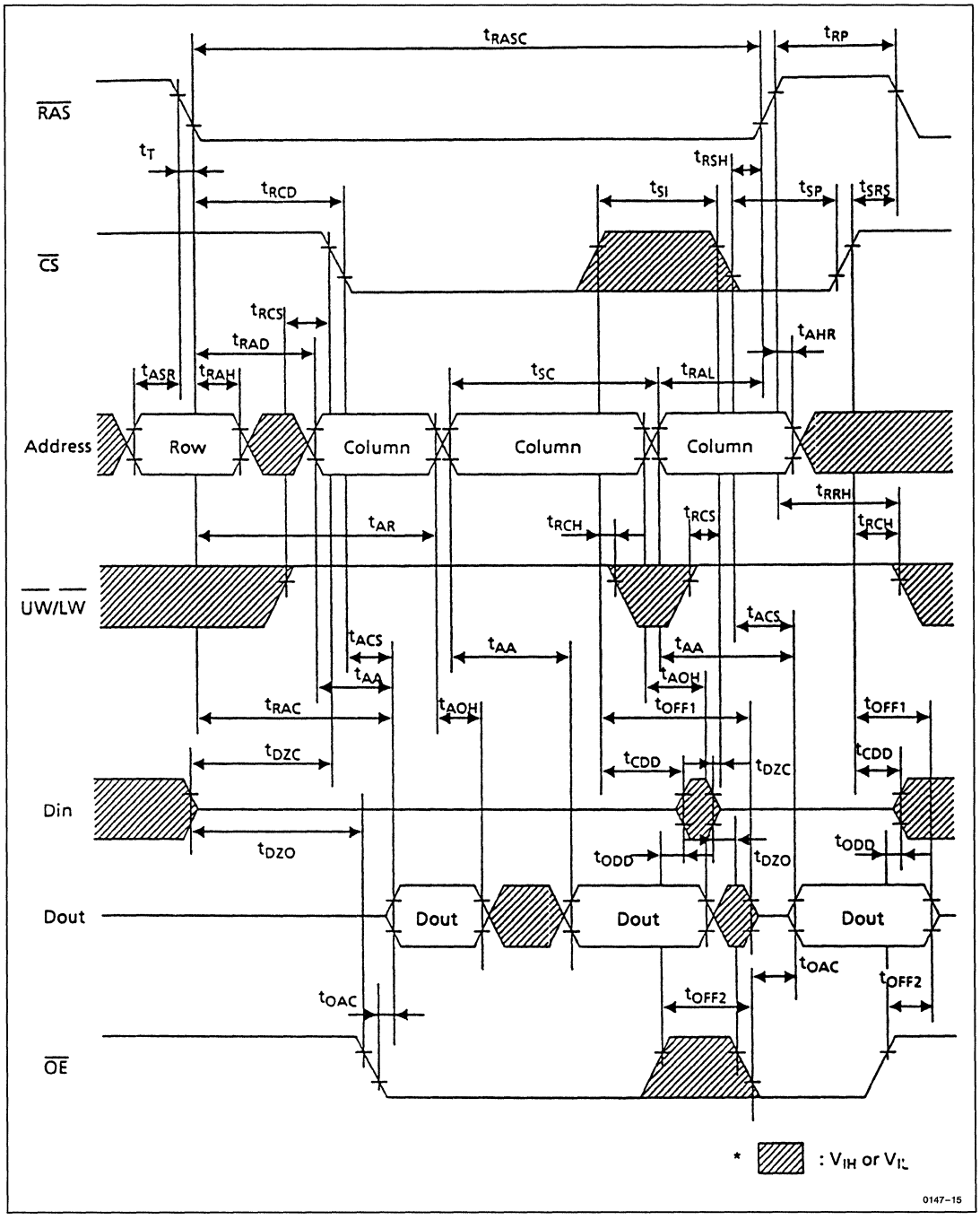
• **$\overline{RAS}$ Only Refresh Cycle**



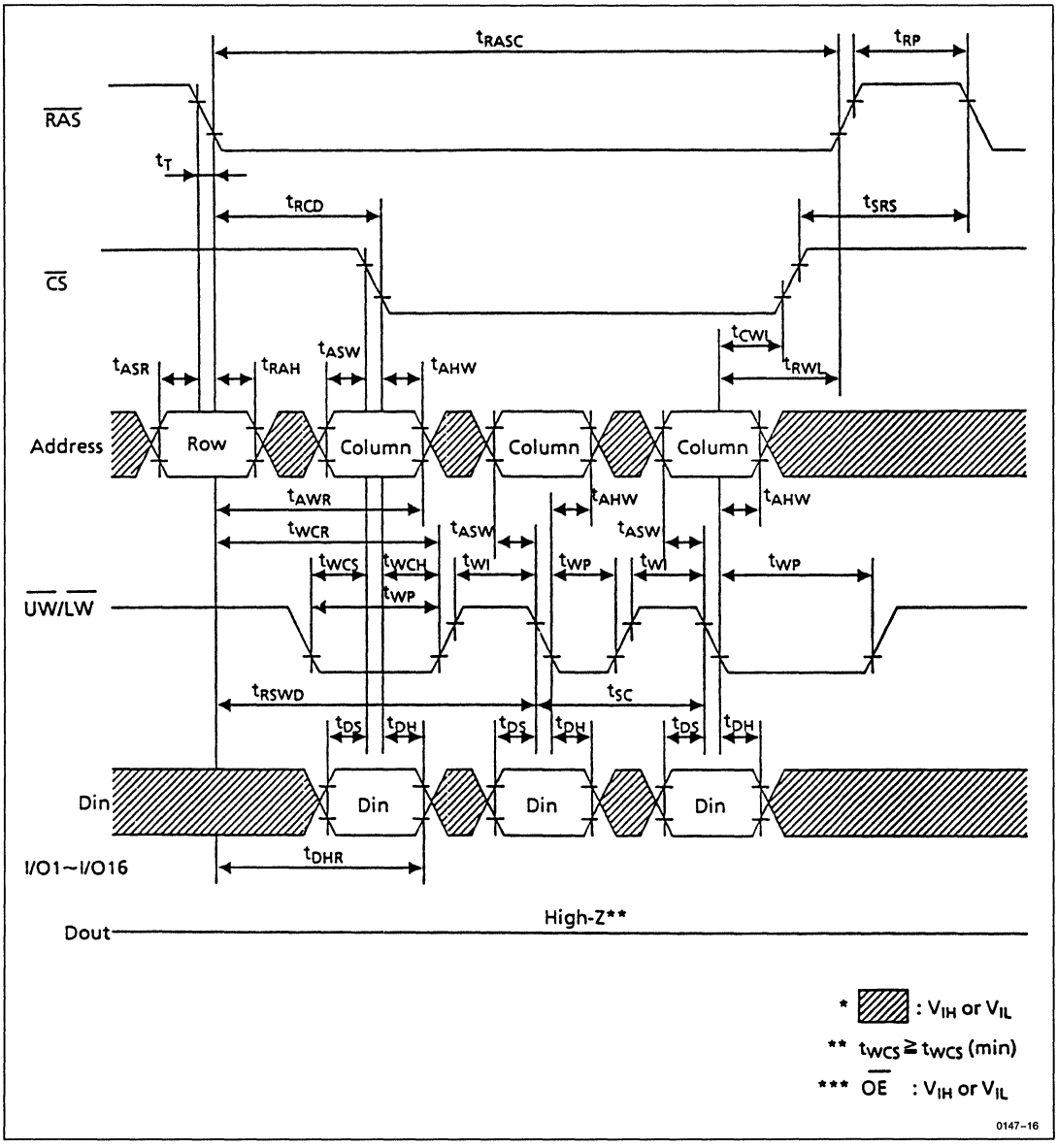
• **$\overline{CS}$ Before $\overline{RAS}$ Cycle**



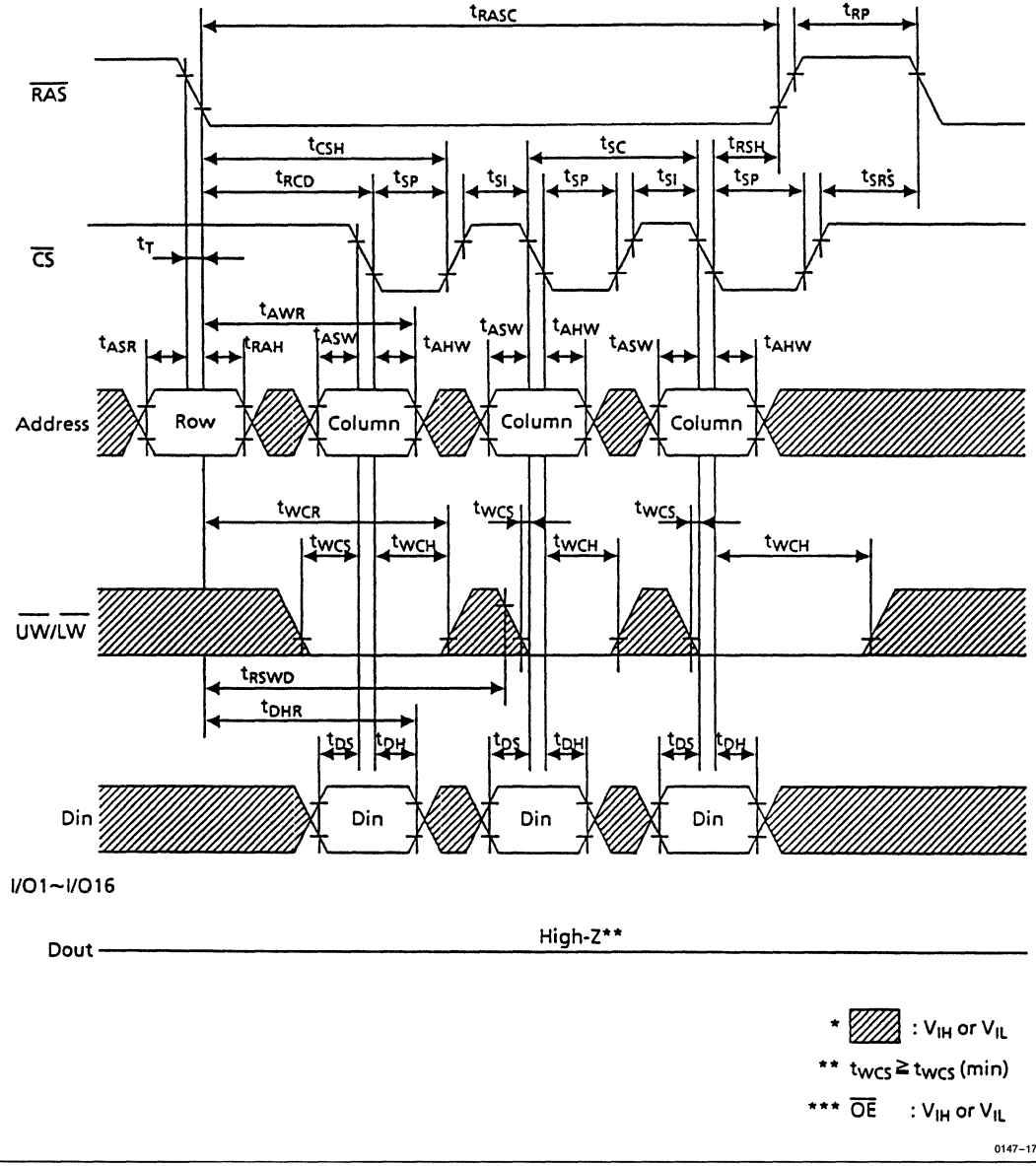
• **Static Column Mode Read Cycle**



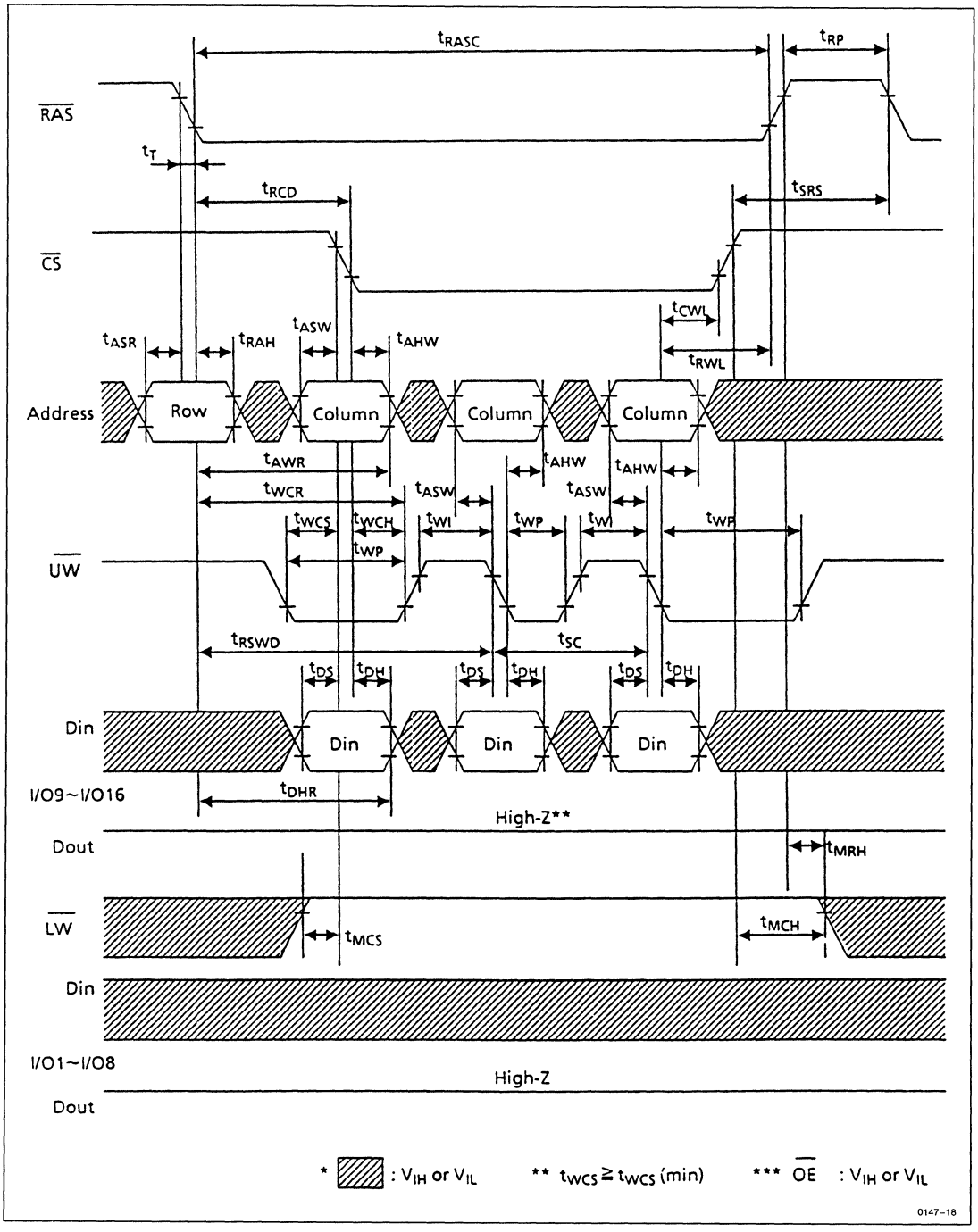
• **Static Column Mode Early Write Cycle (1)**



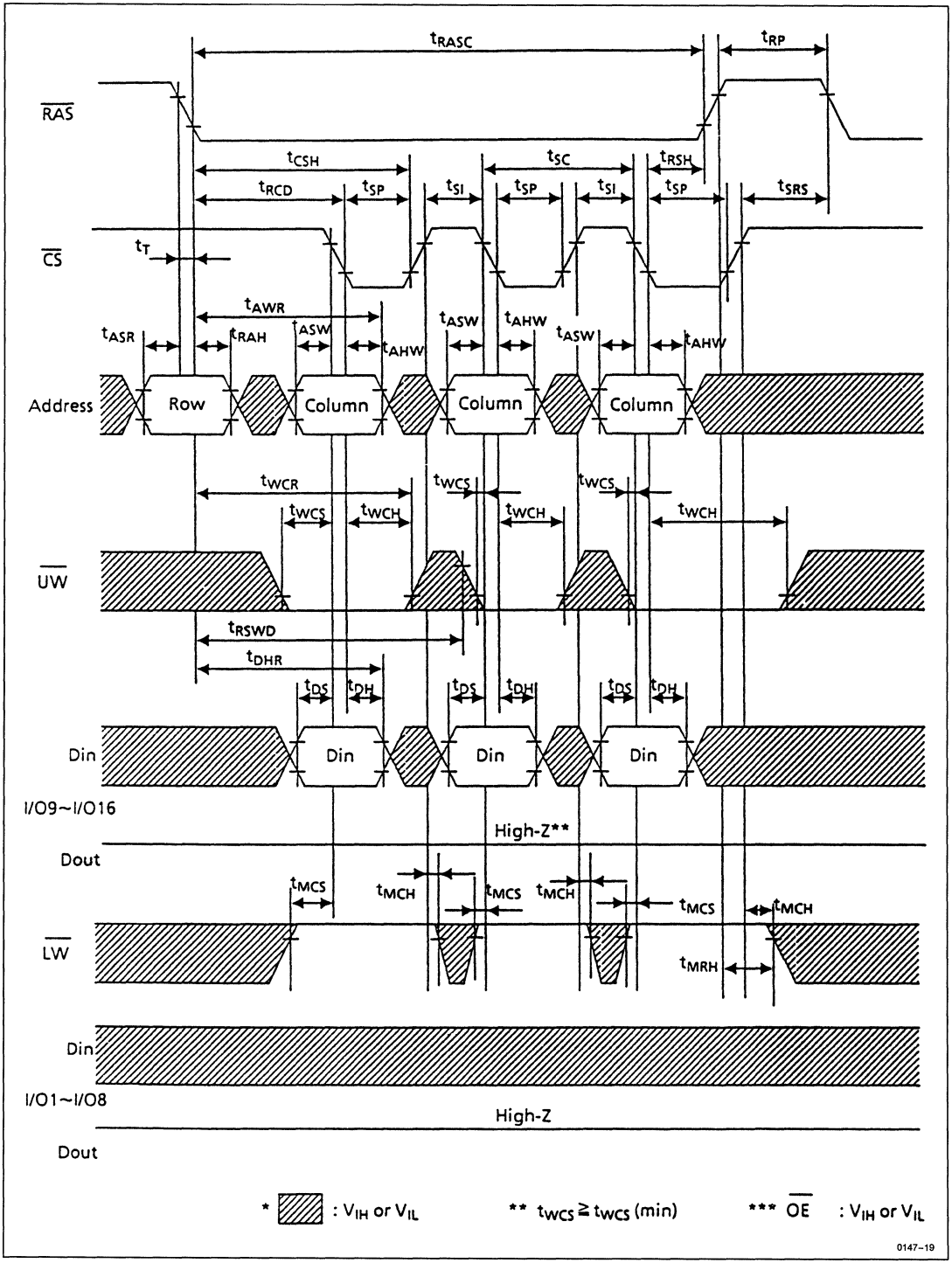
• **Static Column Mode Write Cycle (2)**



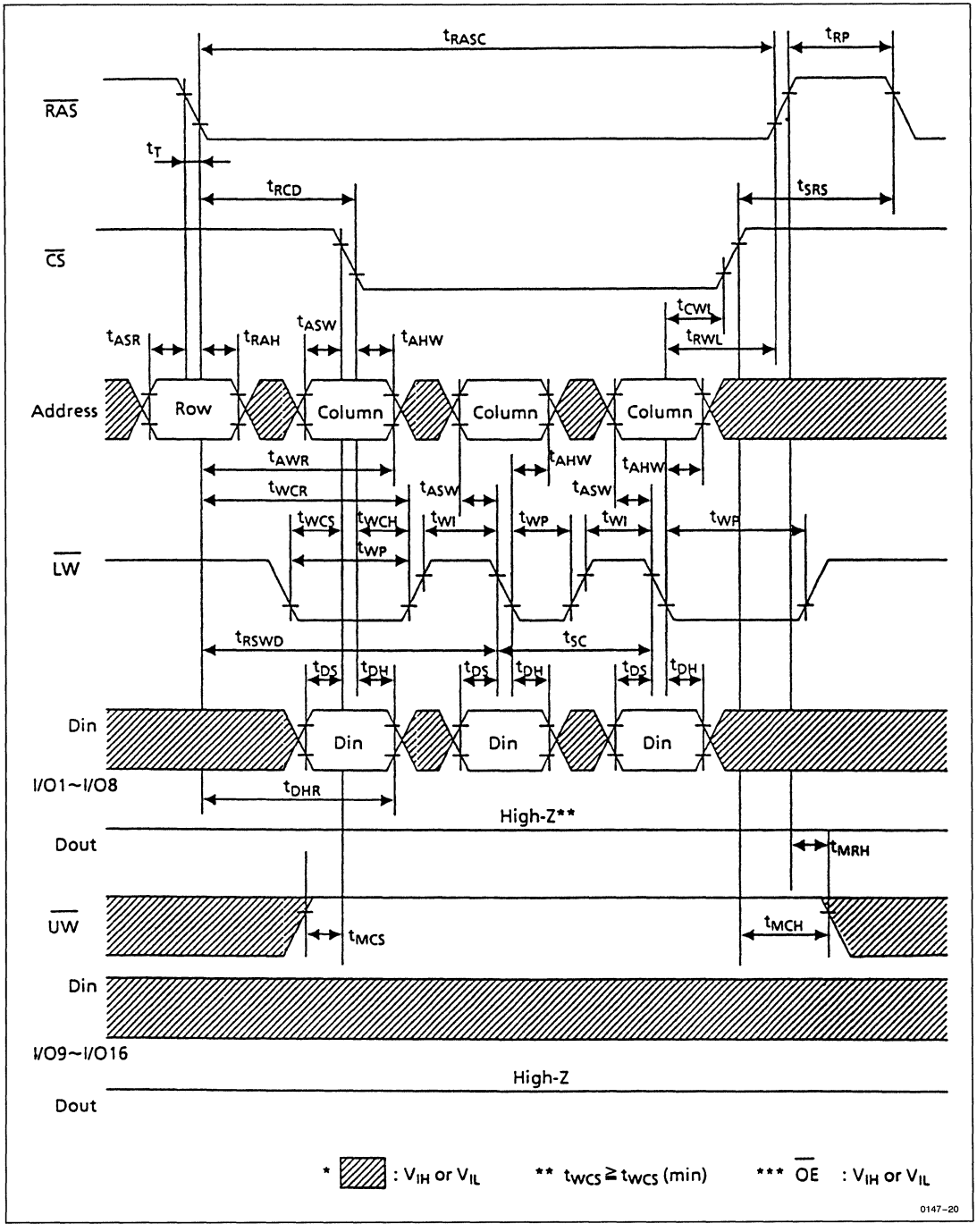
• **Static Column Mode Upper Byte Early Write Cycle (1)**



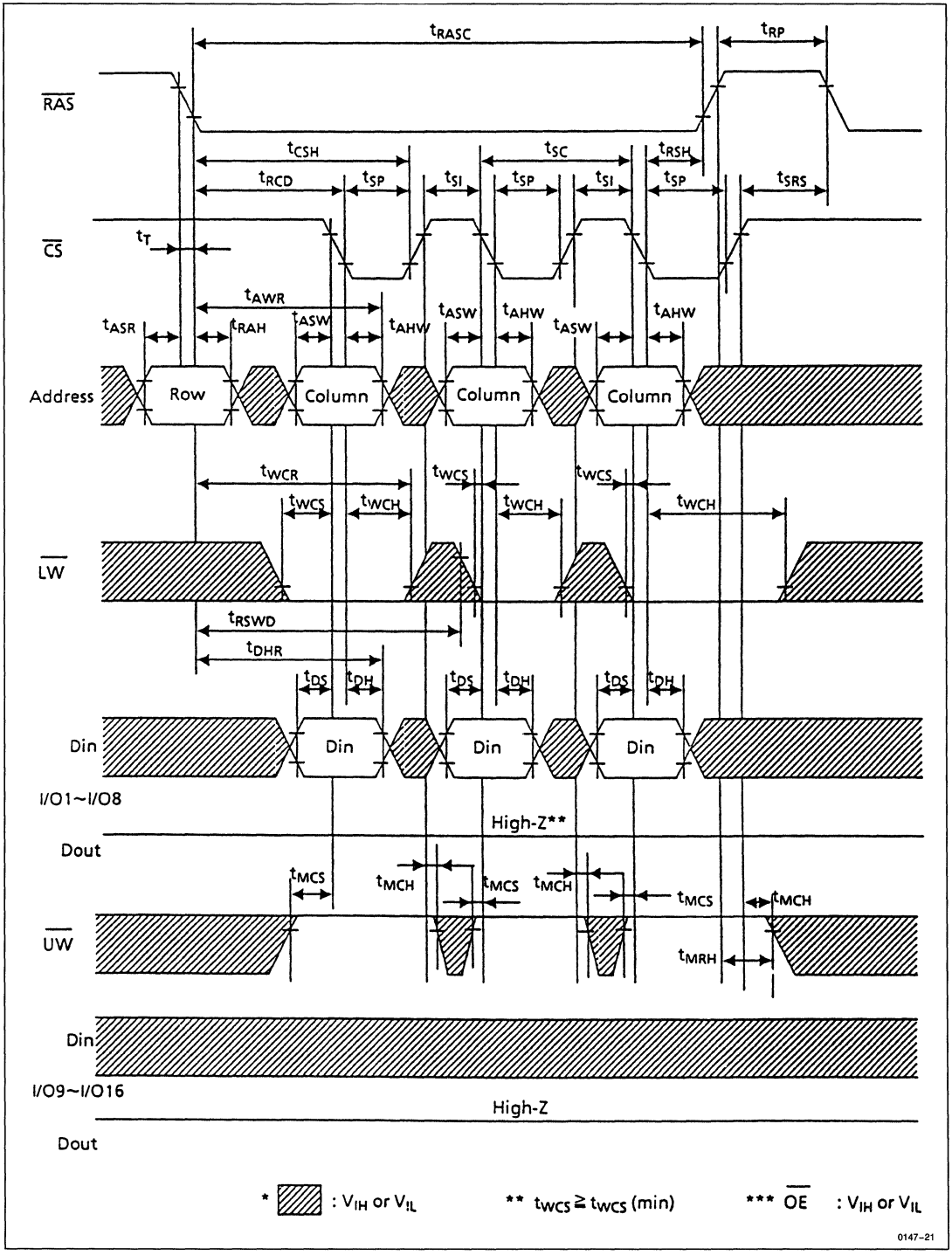
• **Static Column Mode Upper Byte Write Cycle (2)**



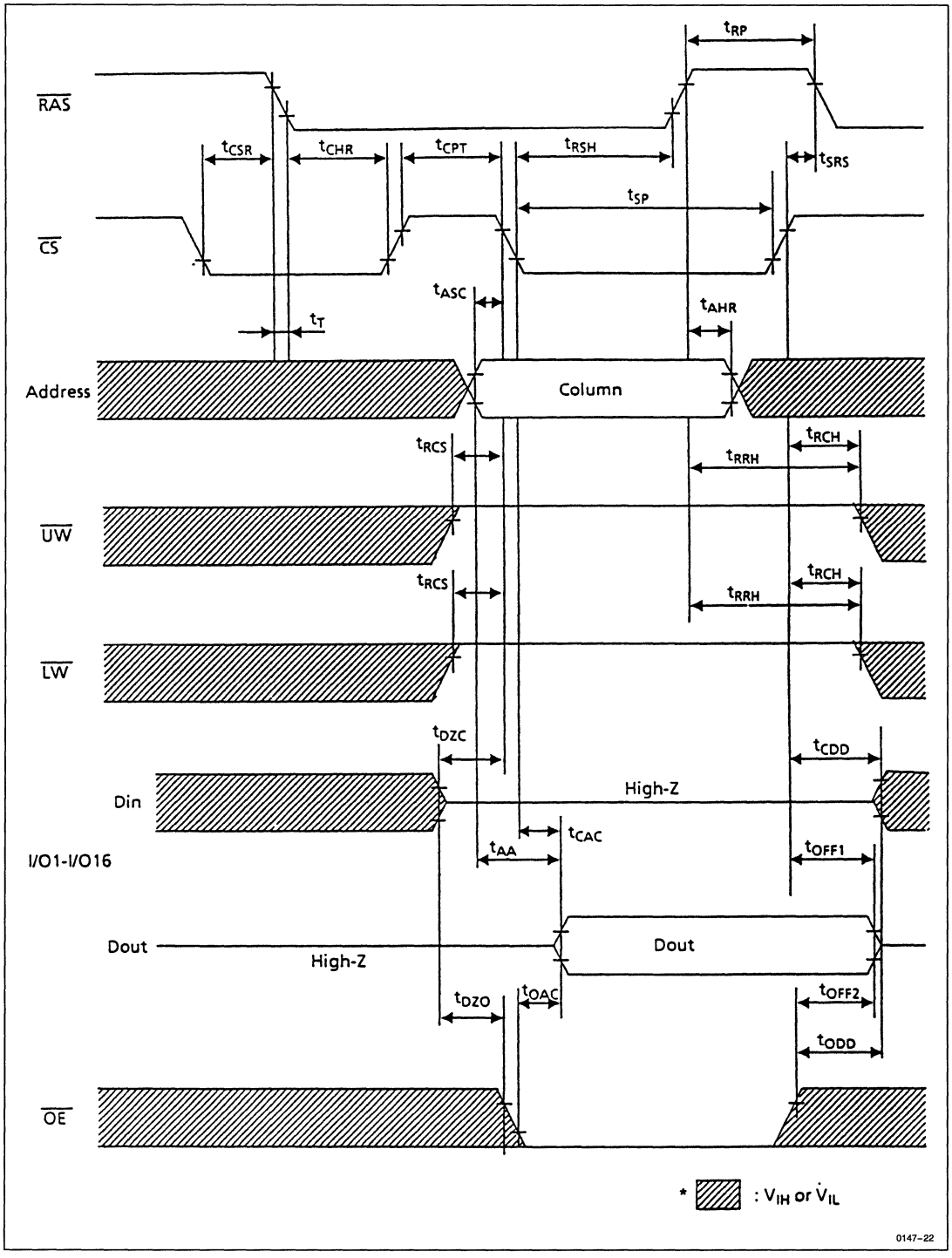
• **Static Column Mode Lower Byte Early Write Cycle (1)**



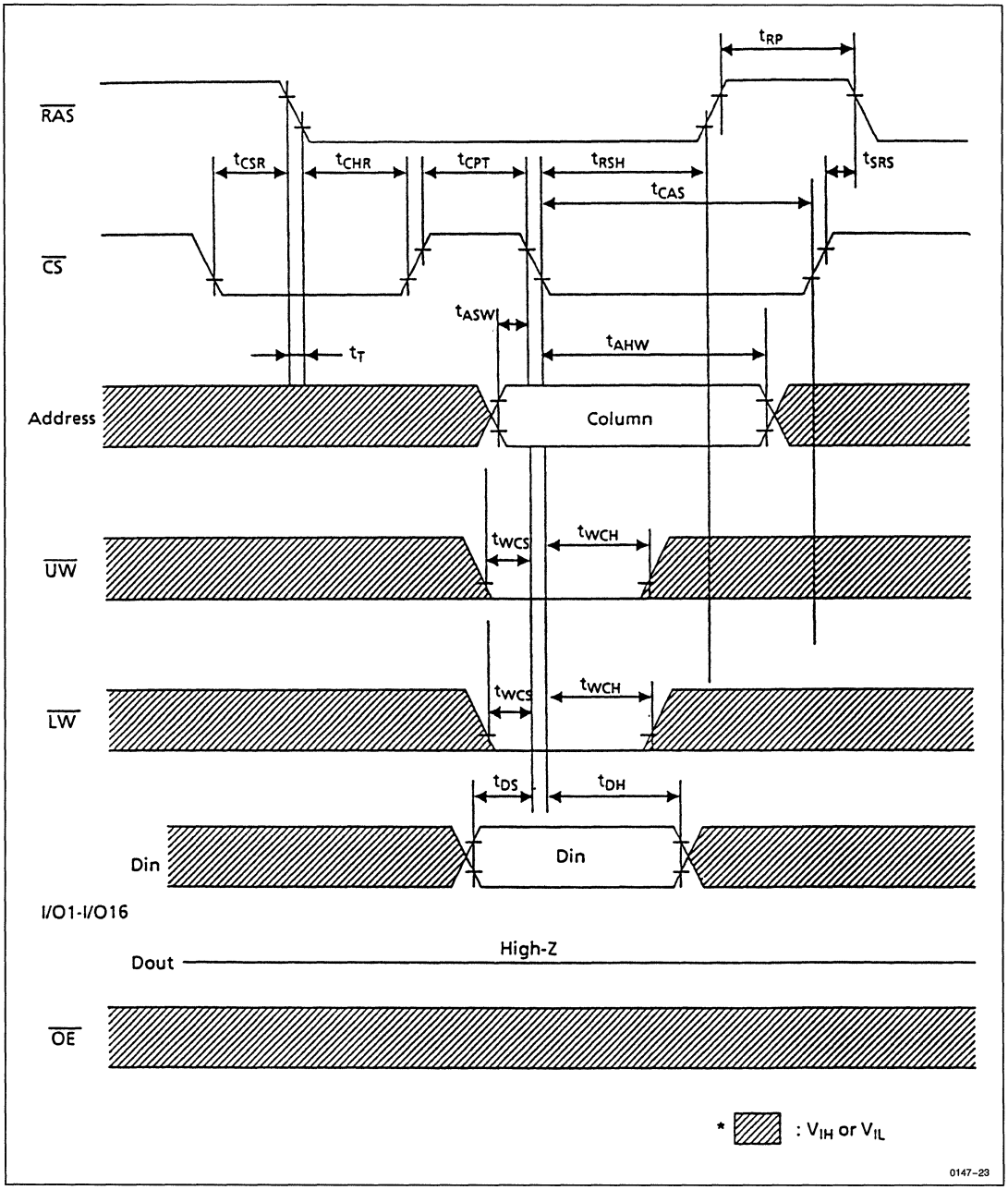
• **Static Column Mode Lower Byte Write Cycle (2)**



• $\overline{CS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



• $\overline{CS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM514100A Series — Preliminary
HM514100AL Series Low Power Version
HM514100ASL Series Super Low Power Version

4,194,304-Word x 1-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514100A is a CMOS dynamic RAM organized 4,194,304 word x 1-bit HM514100A has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514100A offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514100A to be packaged in standard 350 mil 20-pin plastic SOJ, standard 300 mil 20-pin plastic SOJ, standard 400 mil 20-pin plastic ZIP, 20-pin plastic TSOP I, 20-pin plastic TSOP I reverse type, 20-pin plastic TSOP II, and 20-pin plastic TSOP II reverse type.

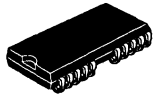
■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode .....605 mW/550 mW/495 mW/440 mW (max)
  - Standby Mode .....11 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles .....(16 ms, 128 ms, 256 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Test Function
- Battery Back Up Operation
  - HM514100AL Series (L-Version)
- Data Retention Operation
  - HM514100ASL Series (SL-Version)

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM514100AJ/ALJ/ASLJ-6	60 ns	350 mil 20-pin
HM514100AJ/ALJ/ASLJ-7	70 ns	Plastic SOJ
HM514100AJ/ALJ/ASLJ-8	80 ns	(CP-20DA)
HM514100AJ/ALJ/ASLJ-10	100 ns	
HM514100AS/ALS/ASLS-6	60 ns	300 mil 20-pin
HM514100AS/ALS/ASLS-7	70 ns	Plastic SOJ
HM514100AS/ALS/ASLS-8	80 ns	(CP-20D)
HM514100AS/ALS/ASLS-10	100 ns	
HM514100AZ/ALZ/ASLZ-6	60 ns	400 mil 20-pin
HM514100AZ/ALZ/ASLZ-7	70 ns	Plastic ZIP
HM514100AZ/ALZ/ASLZ-8	80 ns	(ZP-20)
HM514100AZ/ALZ/ASLZ-10	100 ns	
HM514100AT/ALT/ASLT-6	60 ns	20-pin
HM514100AT/ALT/ASLT-7	70 ns	Plastic TSOP I
HM514100AT/ALT/ASLT-8	80 ns	(TFP-20DA)
HM514100AT/ALT/ASLT-10	100 ns	
HM514100AR/ALR/ASLR-6	60 ns	20-pin
HM514100AR/ALR/ASLR-7	70 ns	Plastic TSOP I
HM514100AR/ALR/ASLR-8	80 ns	Reverse Type
HM514100AR/ALR/ASLR-10	100 ns	(TFP-20DAR)
HM514100ATT/ALTT/ASLTT-6	60 ns	20-pin
HM514100ATT/ALTT/ASLTT-7	70 ns	Plastic TSOP II
HM514100ATT/ALTT/ASLTT-8	80 ns	(TTP-20D)
HM514100ATT/ALTT/ASLTT-10	100 ns	
HM514100ARR/ALRR/ASLRR-6	60 ns	20-pin
HM514100ARR/ALRR/ASLRR-7	70 ns	Plastic TSOP II
HM514100ARR/ALRR/ASLRR-8	80 ns	Reverse Type
HM514100ARR/ALRR/ASLRR-10	100 ns	(TTP-20DR)

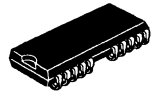
HM514100AJ Series



3DCP20DA

(CP-20DA)

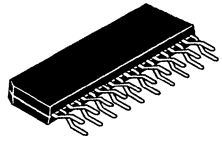
HM514100AS Series



3DCP20D

(CP-20D)

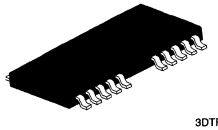
HM514100AZ Series



3DZP20

(ZP-20)

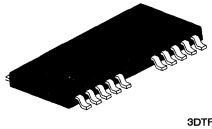
HM514100AT Series



3DTFP20DA

(TFP-20DA)

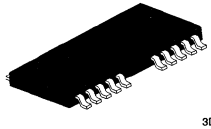
HM514100AR Series



3DTFP20DAR

(TFP-20DAR)

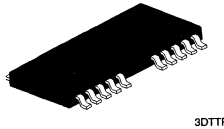
HM514100ATT Series



3DTTP20D

(TTP-20D)

HM514100ARR Series

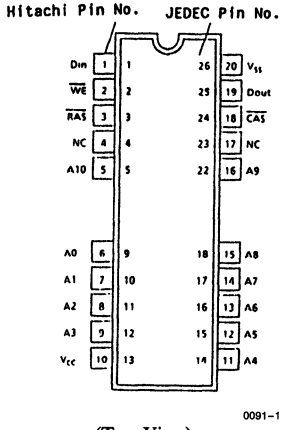


3DTTP20DR

(TTP-20DR)

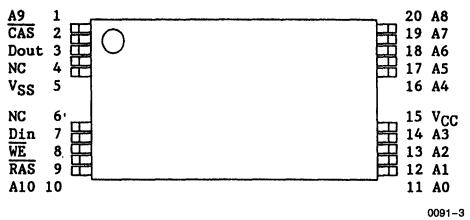
■ PIN OUT

HM514100AJ/ALJ/ASLJ Series
HM514100AS/ALS/ASLS Series



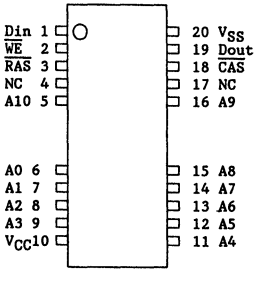
(Top View)

HM514100AT/ALZ/ASLT Series



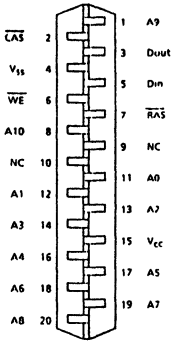
(Top View)

HM514100ATT/ALTT /ASLTT Series



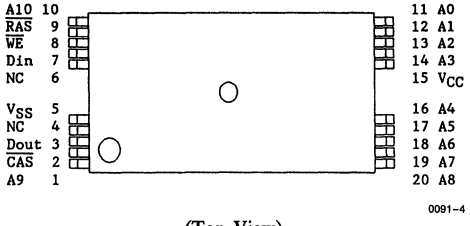
(Top View)

HM514100AZ/ALZ/ASLZ Series



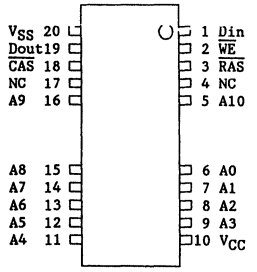
(Bottom View)

HM514100AR/ALR/ASLR Series



(Top View)

HM514100ARR/ALRR /ASLRR Series



(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{10}	Address Input
A_0–A_9	Refresh Address Input
D_{in}	Data-in
D_{out}	Data-out
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Read/Write Enable
V_{CC}	Power (+ 5V)
V_{SS}	Ground
NC	No Connection

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)
(T_A = 0 to +60°C (SL-Version))

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
		4.0	—	5.5	V	1, 2 (SL-Version)
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−2.0	—	0.8	V	1

Notes: 1. All voltage referenced to V_{SS}.
2. Data retention operation only.

• DC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)
(T_A = 0 to +60°C, V_{CC} = 5V ±10%, V_{SS} = 0V (SL-Version))

Parameter	Symbol	HM514100A-6		HM514100A-7		HM514100A-8		HM514100A-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	110	—	100	—	90	—	80	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	—	2	mA	TTL Interface RAS, CAS = V_{IH} D_{out} = High-Z	
		—	1	—	1	—	1	—	1	mA	CMOS Interface RAS, CAS > V_{CC} − 0.2V D_{out} = High-Z	
[L-Version] Standby Current		—	200	—	200	—	200	—	200	μA	CMOS Interface RAS, CAS = V_{IH} WE, Address and D_{in} = V_{IH} or V_{IL} D_{out} = High-Z	4
[SL-Version] Standby Current		—	100	—	100	—	100	—	100	μA	CMOS Interface RAS, CAS = V_{IH} WE, Address and D_{in} = V_{IH} or V_{IL} D_{out} = High-Z	4
RAS Only Refresh Current	I_{CC3}	—	110	—	100	—	90	—	80	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	—	5	mA	RAS = V_{IH} CAS = V_{IL} D_{out} = Enable	1
CAS Before RAS Refresh Current	I_{CC6}	—	110	—	100	—	90	—	80	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	110	—	100	—	90	—	80	mA	t_{PC} = Min	1, 3

• **DC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)
(T_A = 0 to +60°C, V_{CC} = 5V ±10%, V_{SS} = 0V (SL-Version)) (continued)

Parameter	Symbol	HM514100A-6		HM514100A-7		HM514100A-8		HM514100A-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max			
[L-Version] Battery Back Up Operating Current (Standby with CBR Refresh)	I_{CC10}	—	300	—	300	—	300	—	300	µA	t_{RC} = 125 µs t_{RAS} ≤ 1 µs WE = V_{IH}, CAS = V_{IL} Address, D_{in} = V_{IH} or V_{IL} D_{out} = High-Z	4
[SL-Version] Data Retention Current (Equivalent Refresh Time is 256 ms)		—	150	—	150	—	150	—	150	µA	t_{RC} = 250 µs t_{RAS} ≤ 200 ns WE = V_{IH}, CAS = V_{IL} Address, D_{in} = V_{IH} or V_{IL} D_{out} = High-Z 4.0V ≤ V_{CC} ≤ 5.5V	4
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	−10	10	µA	0V ≤ V_{IN} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	−10	10	µA	0V ≤ V_{IN} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. V_{CC} − 0.2V ≤ V_{IH} ≤ 6.5V and 0V ≤ V_{IL} ≤ 0.2V.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address, Data-in)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-out)	C_O	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 12, 15]
(T_A = 0 to +60°C, V_{CC} = 5V ±10%, V_{SS} = 0V (SL-Version))

Test Conditions: Input rise and fall times: 5 ns
Input timing reference levels: 0.8V, 2.4V
Output load: 2 TTL Gate + CL (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514100A-6		HM514100A-7		HM514100A-8		HM514100A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10000	20	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	15	—	ns	

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters) (continued)

Parameter	Symbol	HM514100A-6		HM514100A-7		HM514100A-8		HM514100A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	20	60	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	—	16	ms	
Refresh Period (L-Version)	t_{REF}	—	128	—	128	—	128	—	128	ms	
Refresh Period (SL-Version)	t_{REF}	—	16	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514100A-6		HM514100A-7		HM514100A-8		HM514100A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	2, 3, 16
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	—	25	ns	3, 4, 14, 16
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	ns	3, 5, 14, 16
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	15	0	20	0	20	0	25	ns	6

Write Cycle

Parameter	Symbol	HM514100A-6		HM514100A-7		HM514100A-8		HM514100A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	10	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	20	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	20	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514100A-6		HM514100A-7		HM514100A-8		HM514100A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	130	—	155	—	175	—	210	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	60	—	70	—	80	—	100	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	15	—	20	—	20	—	25	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	30	—	35	—	40	—	45	—	ns	10

Refresh Cycle

Parameter	Symbol	HM514100A-6		HM514100A-7		HM514100A-8		HM514100A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time in Normal Mode	t_{CPN}	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514100A-6		HM514100A-7		HM514100A-8		HM514100A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	40		45	—	50	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	35	—	40	—	45	—	50	ns	3, 14, 16
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	45	—	50	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM514100A-6		HM514100A-7		HM514100A-8		HM514100A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	60	—	70	—	75	—	85	—	ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPW}	35	—	40	—	45	—	50	—	ns	10

Test Mode Cycle

Parameter	Symbol	HM514100A-6		HM514100A-7		HM514100A-8		HM514100A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	10	—	10	—	10	—	10	—	ns	

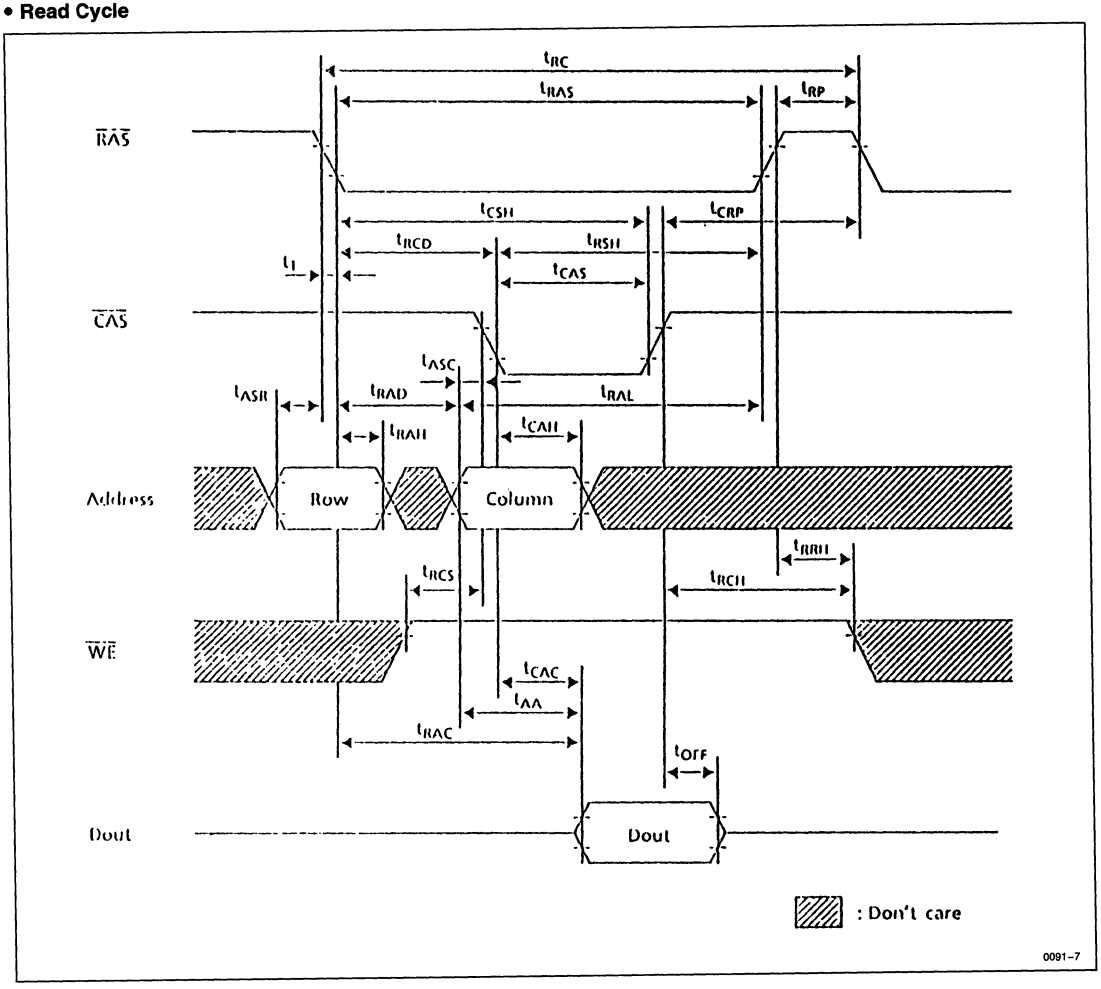
Counter Test Cycle

Parameter	Symbol	HM514100A-6		HM514100A-7		HM514100A-8		HM514100A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	40	—	40	—	40	—	ns	

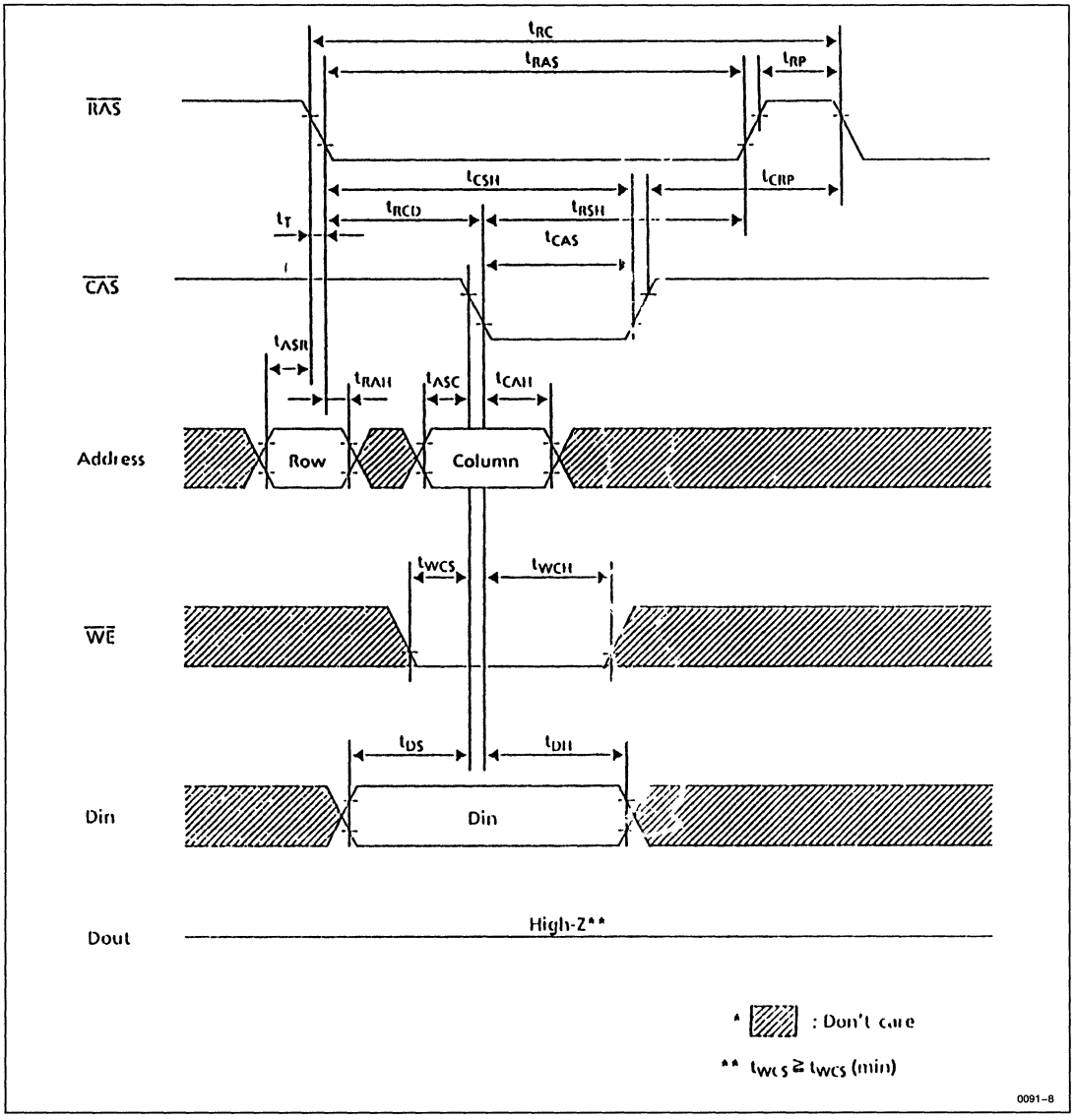
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits—RA10, CA10 and CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is D_{out} and data input pin is D_{in}. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
16. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORMS

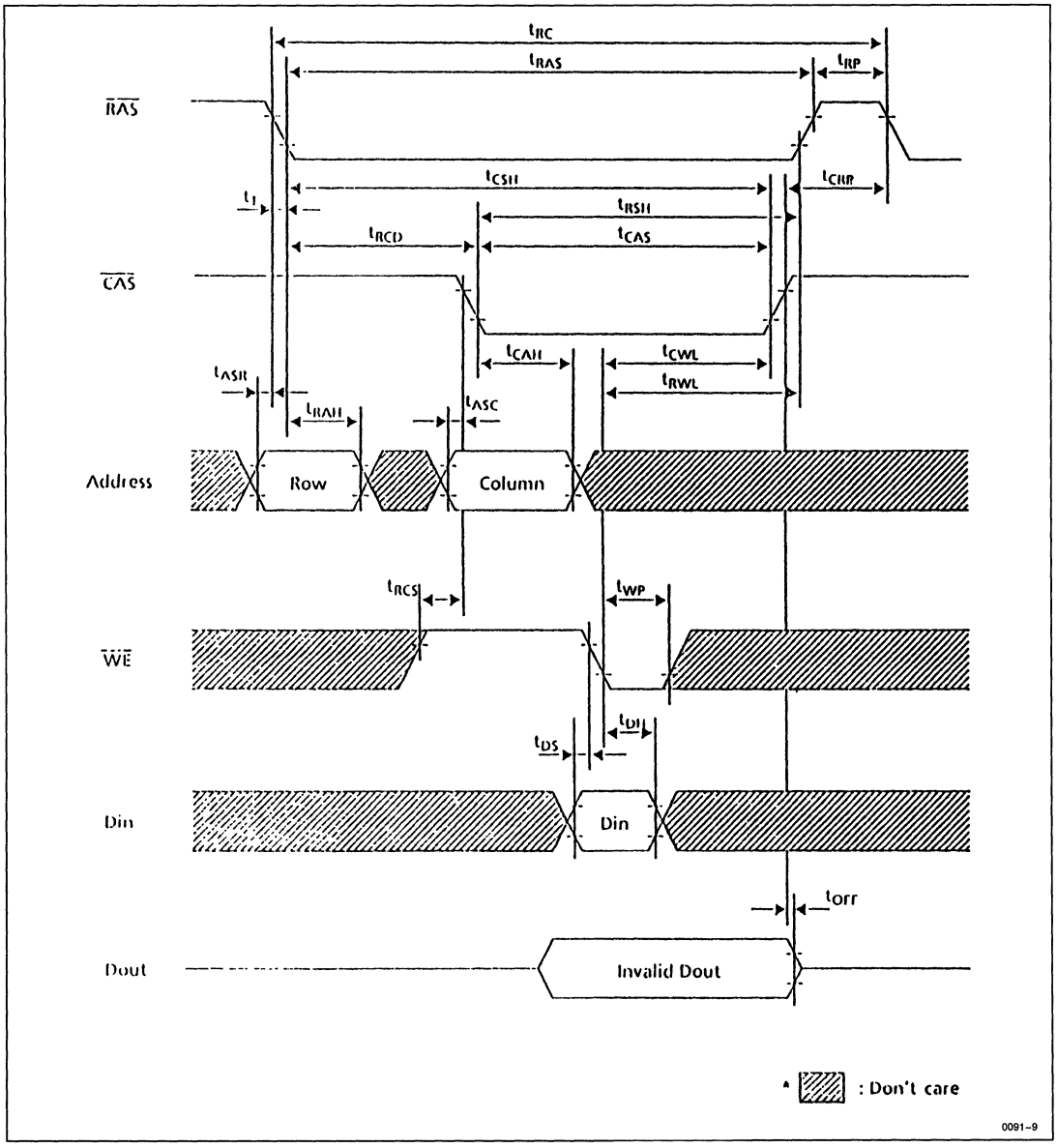
• Read Cycle



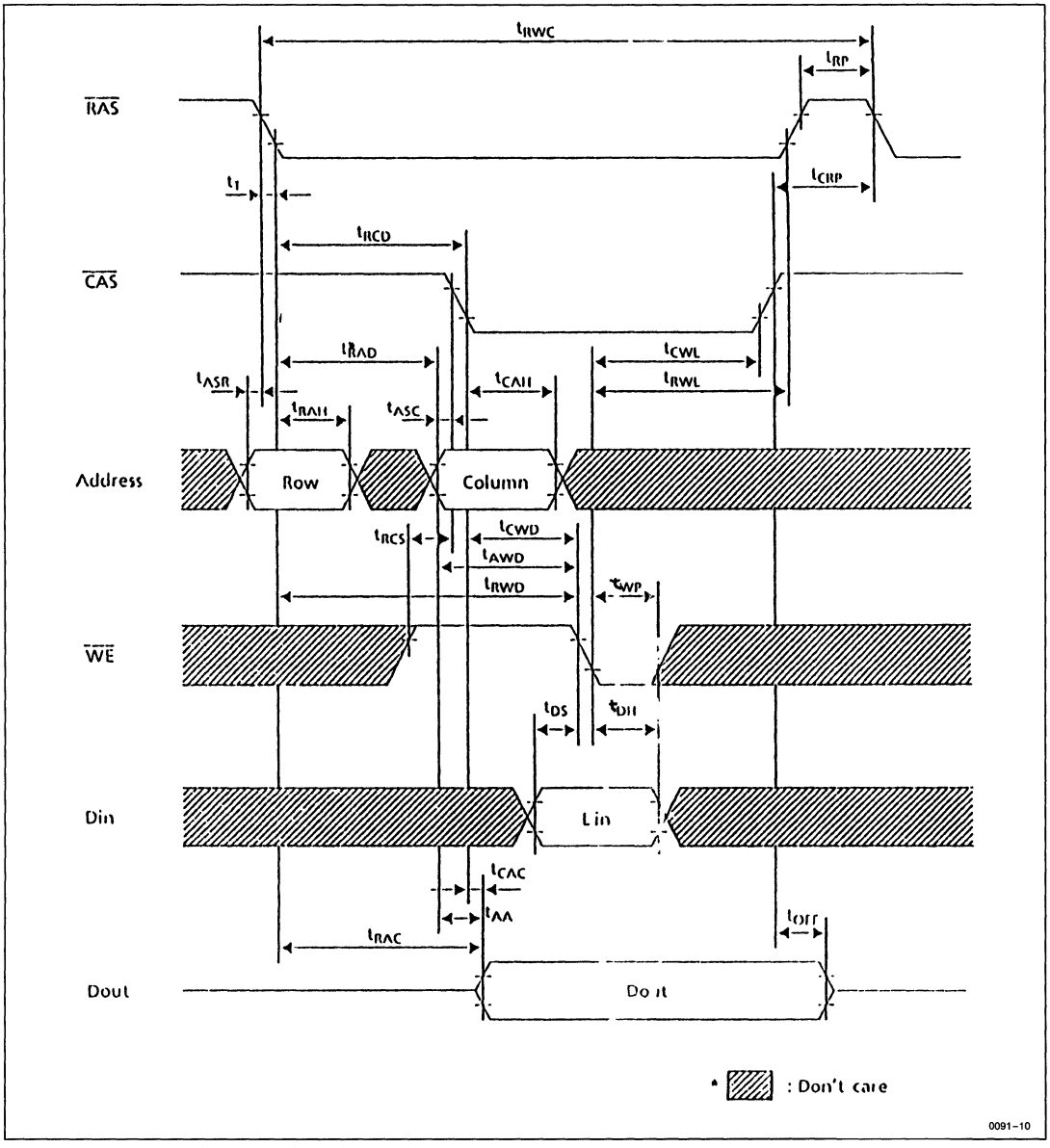
• **Early Write Cycle**



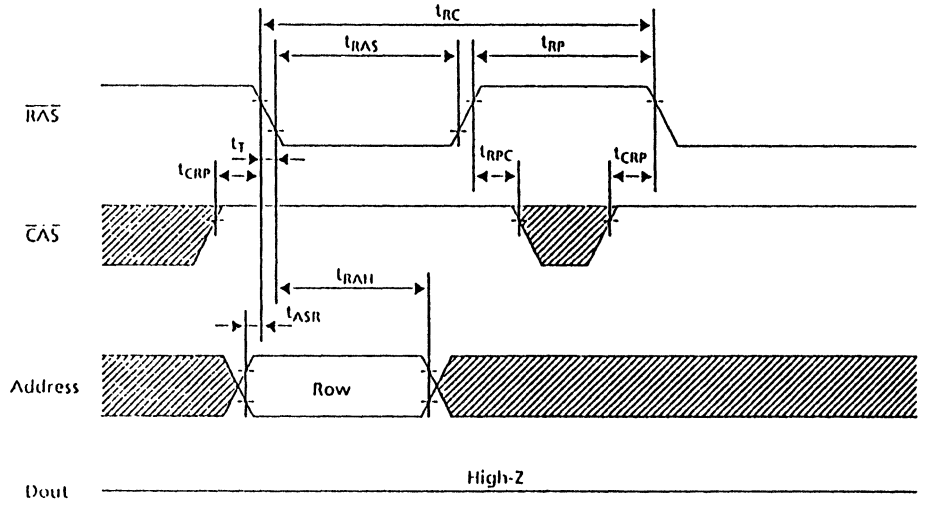
• **Delayed Write Cycle**



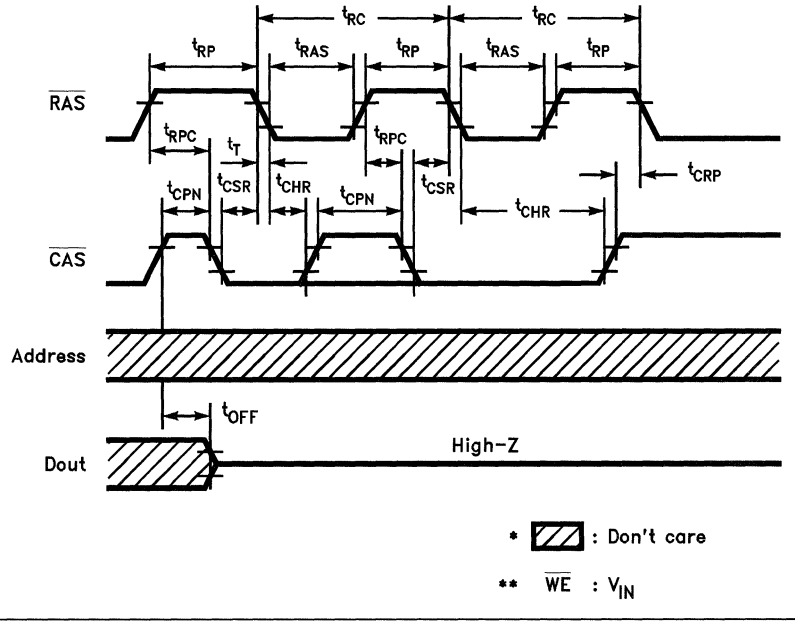
• **Read-Modify-Write Cycle**



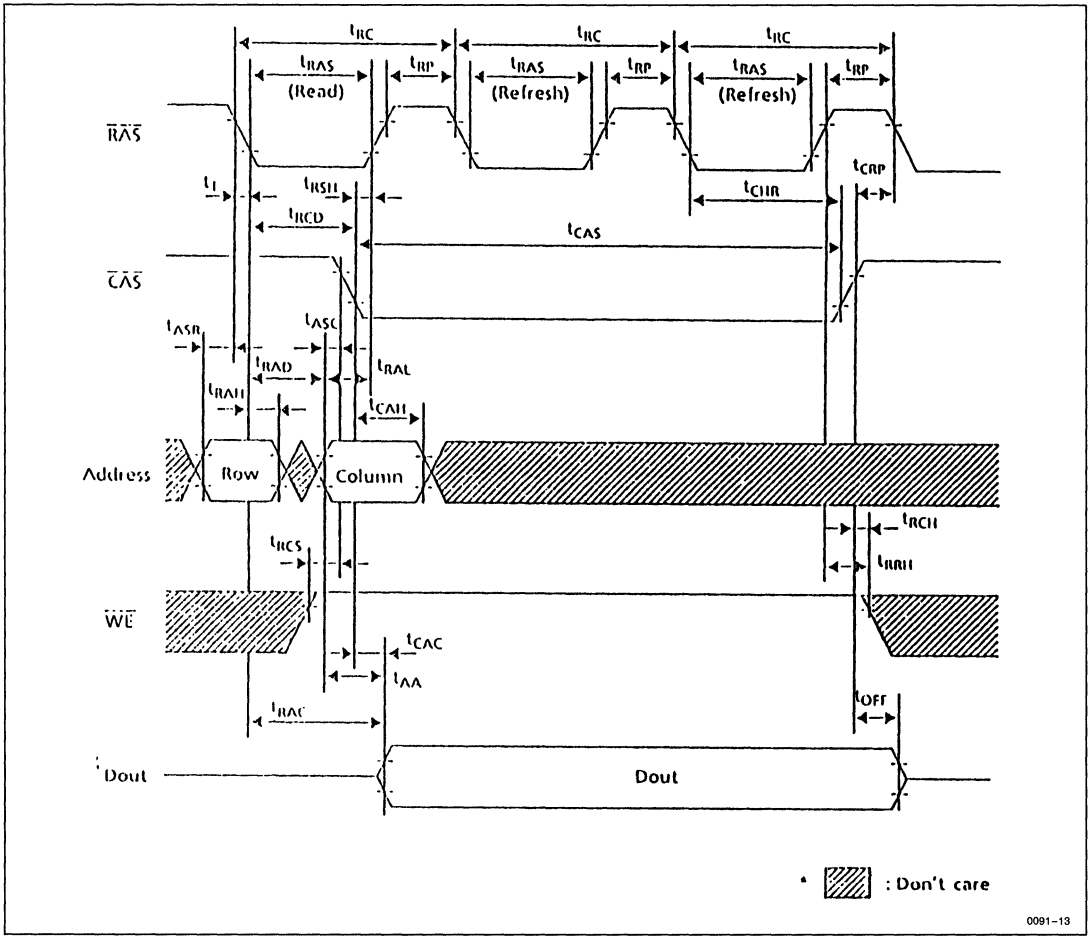
• $\overline{RAS}$ Only Refresh Cycle



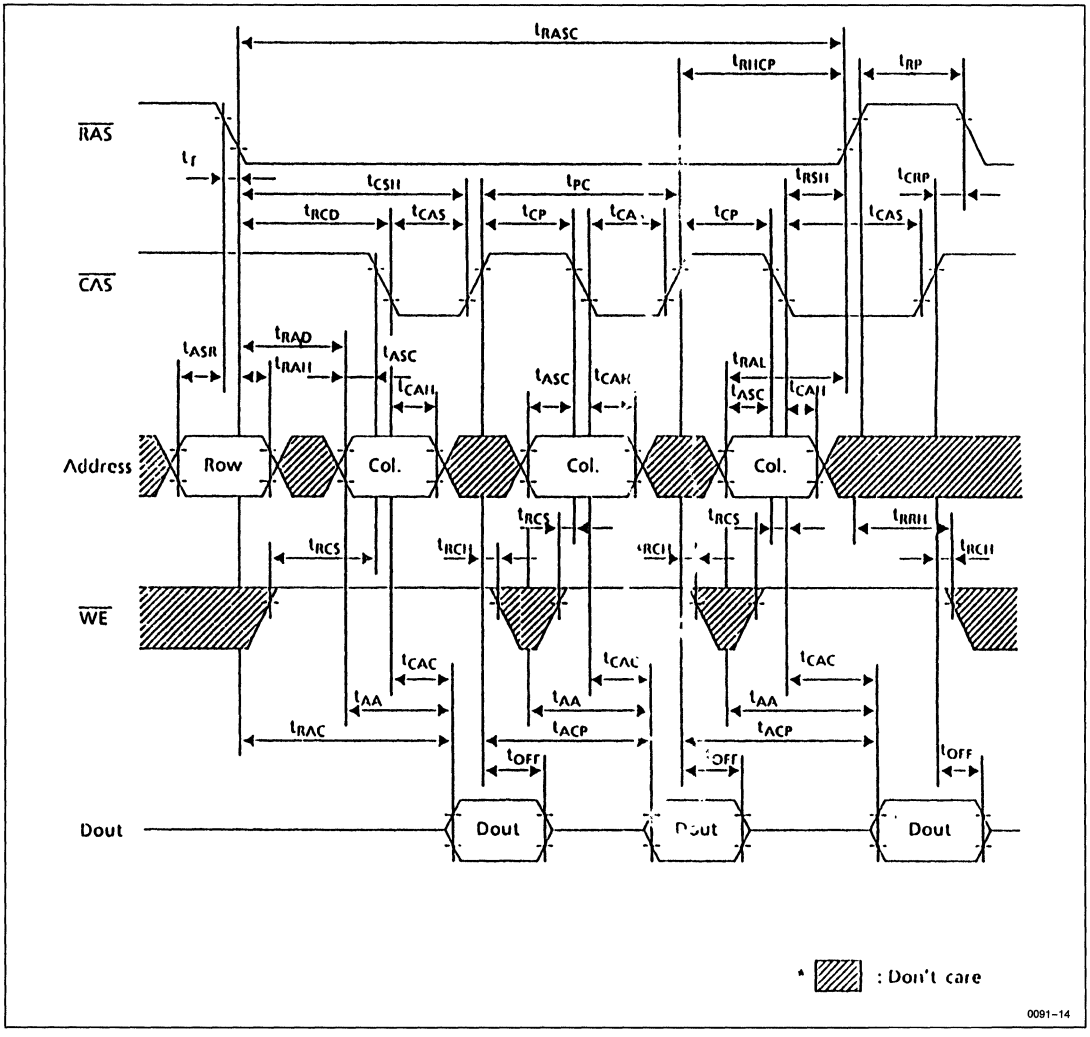
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



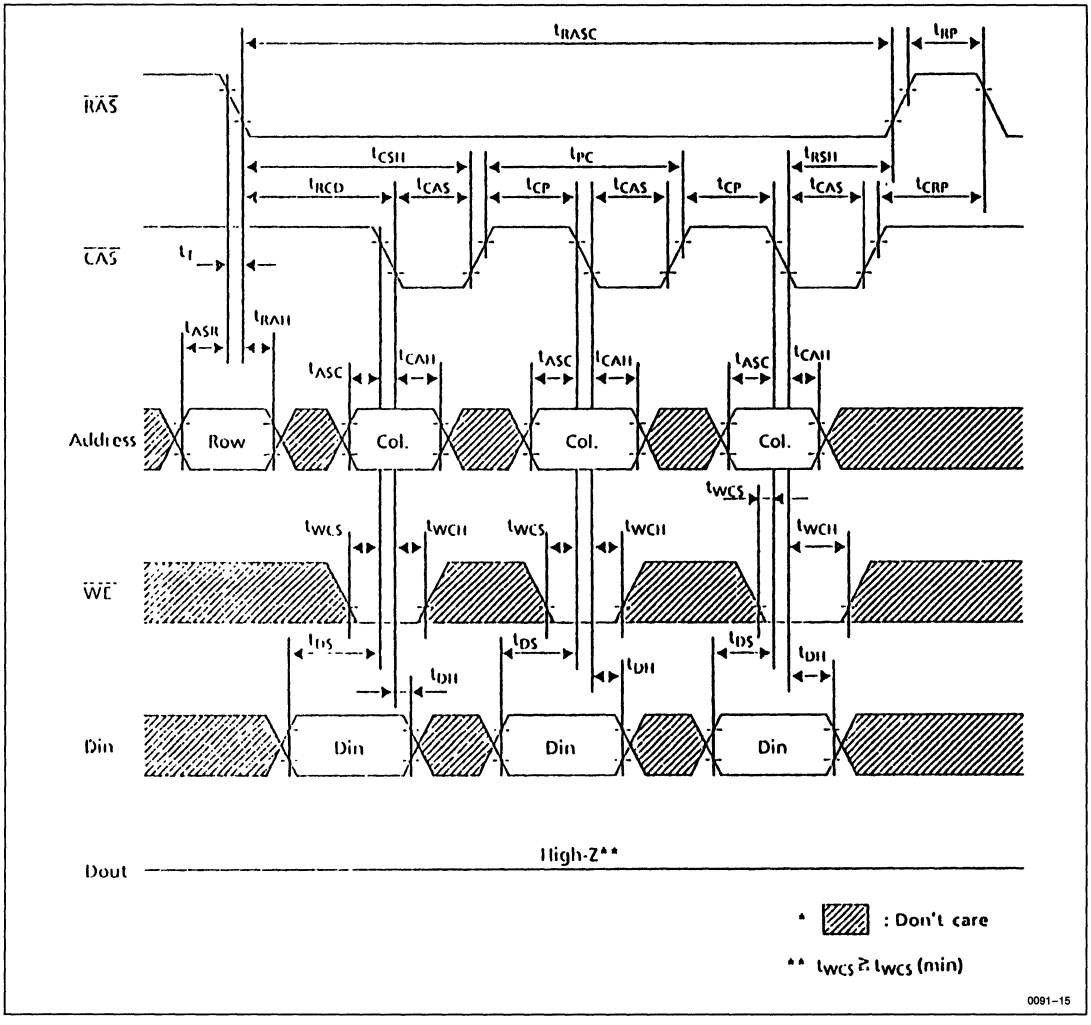
• **Hidden Refresh Cycle**



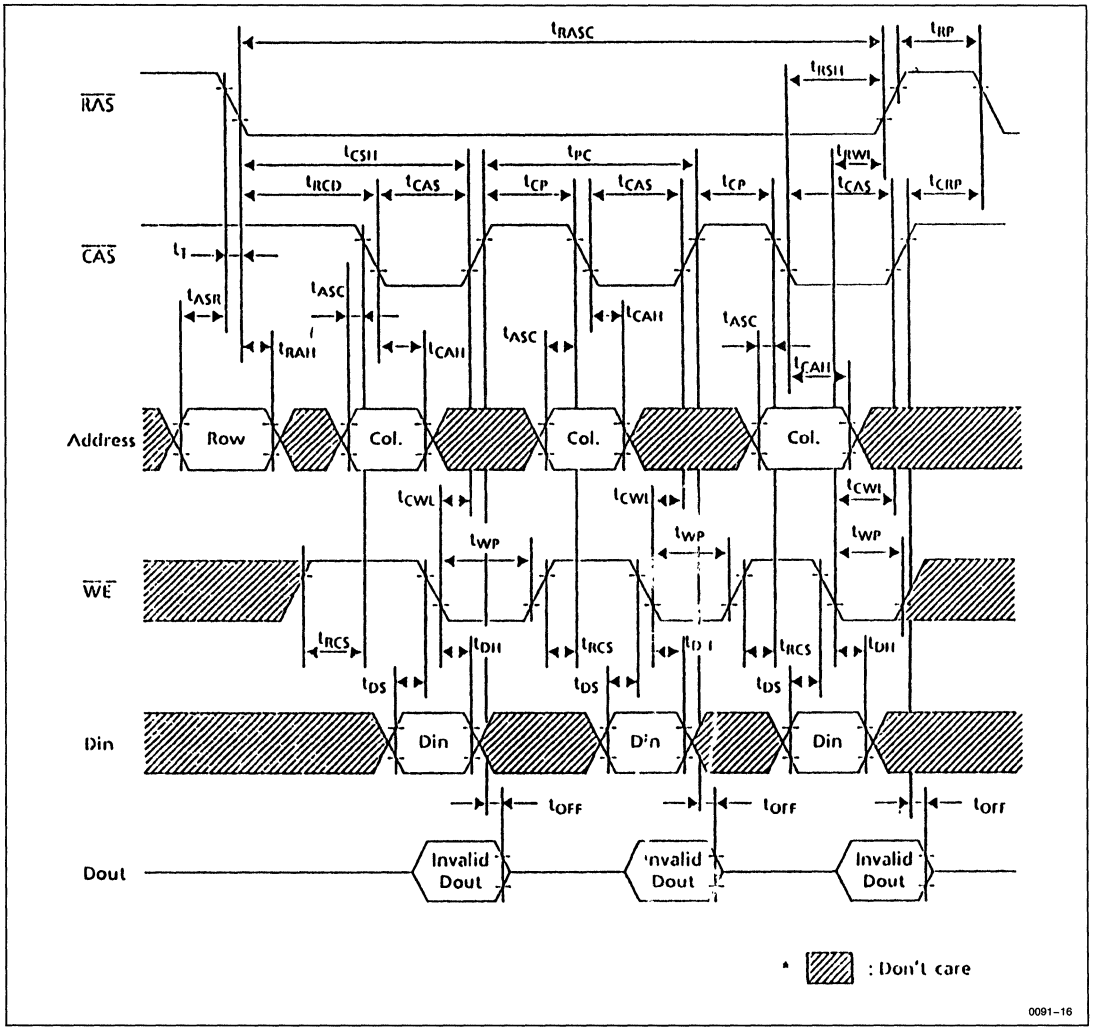
• **Fast Page Mode Read Cycle**



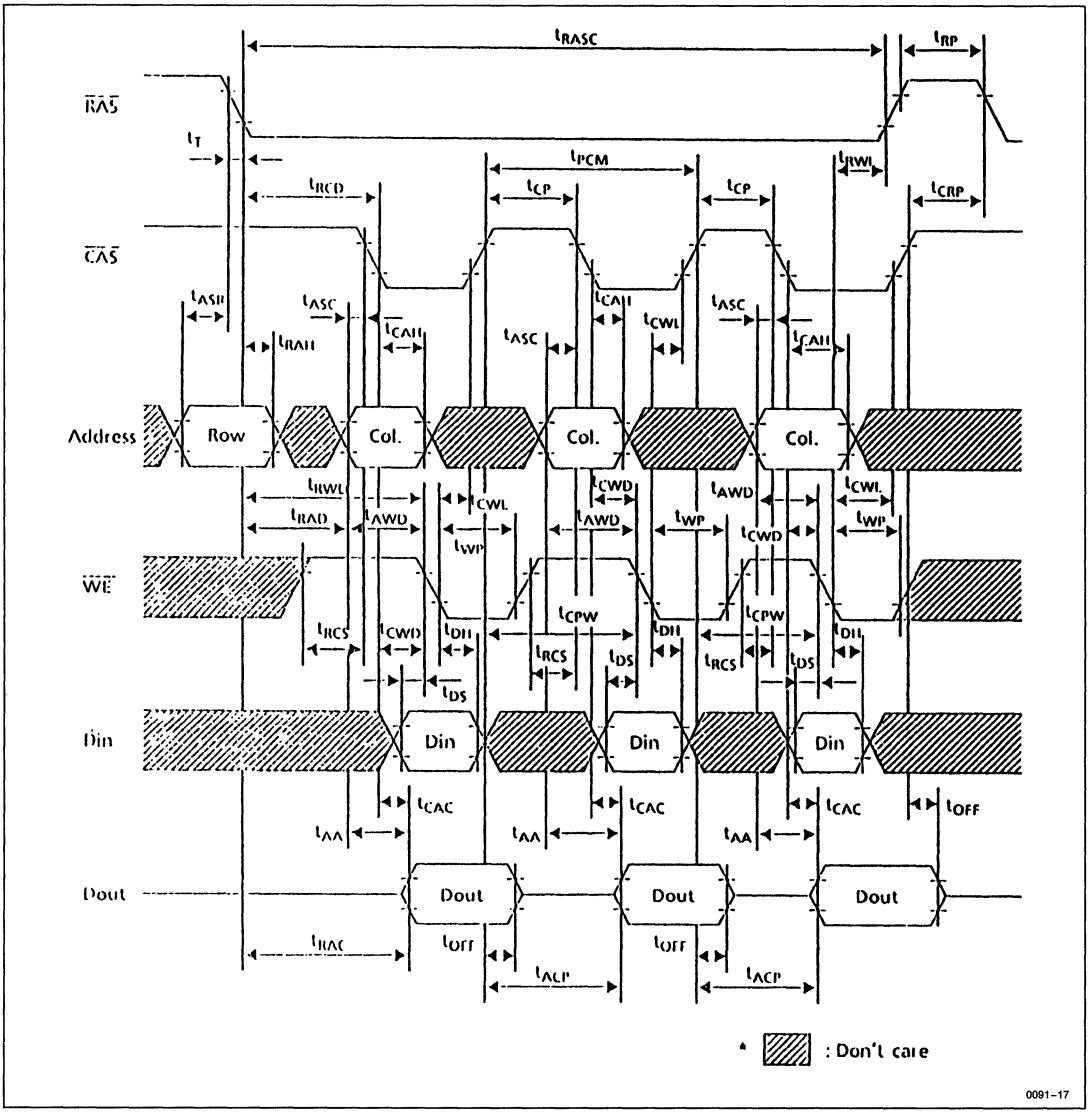
• **Fast Page Mode Early Write Cycle**



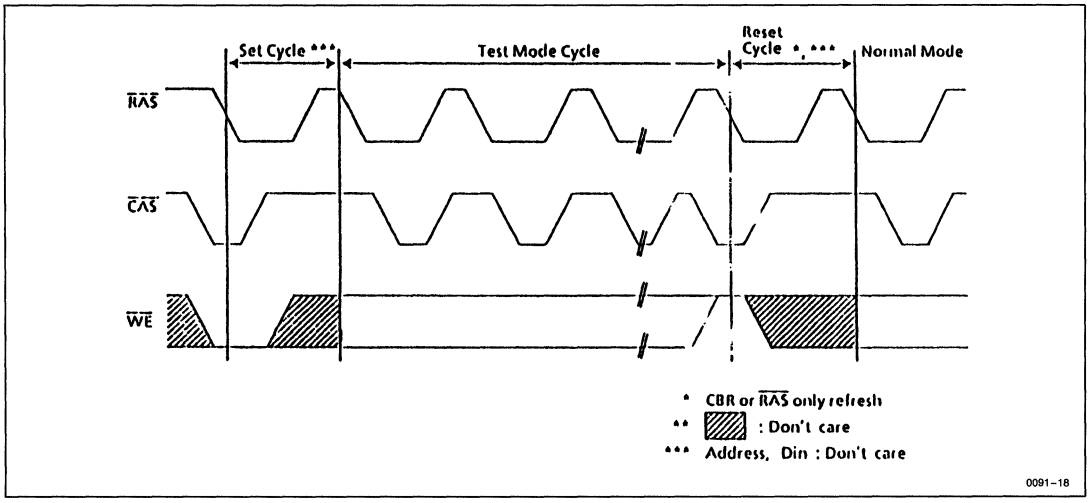
• **Fast Page Mode Delayed Write Cycle**



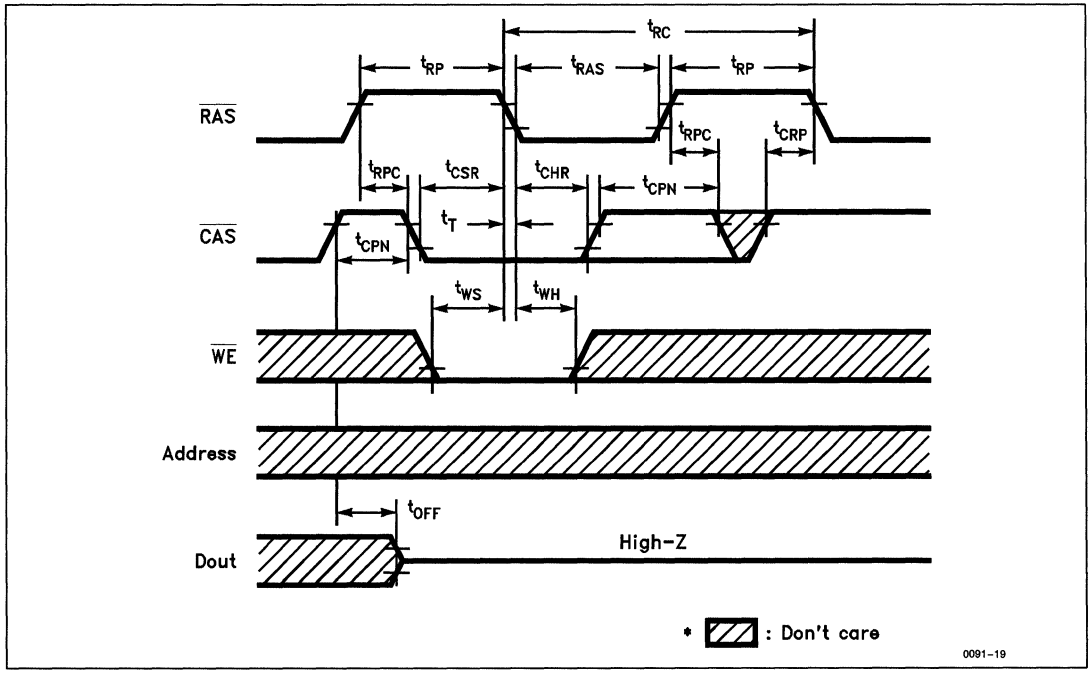
• **Fast Page Mode Read-Modify-Write Cycle**



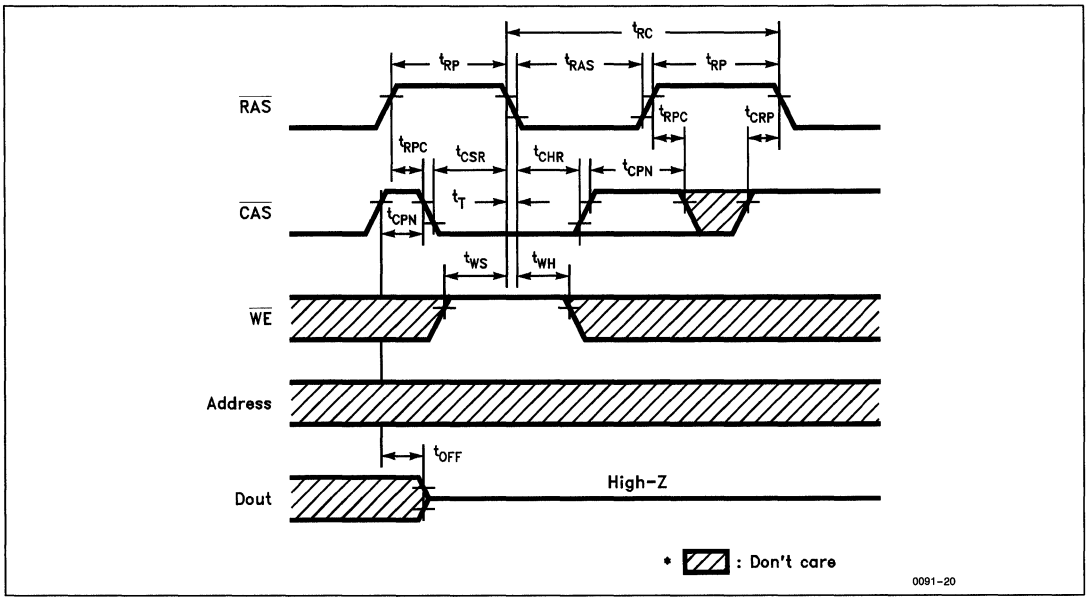
• **Test Mode Cycle**



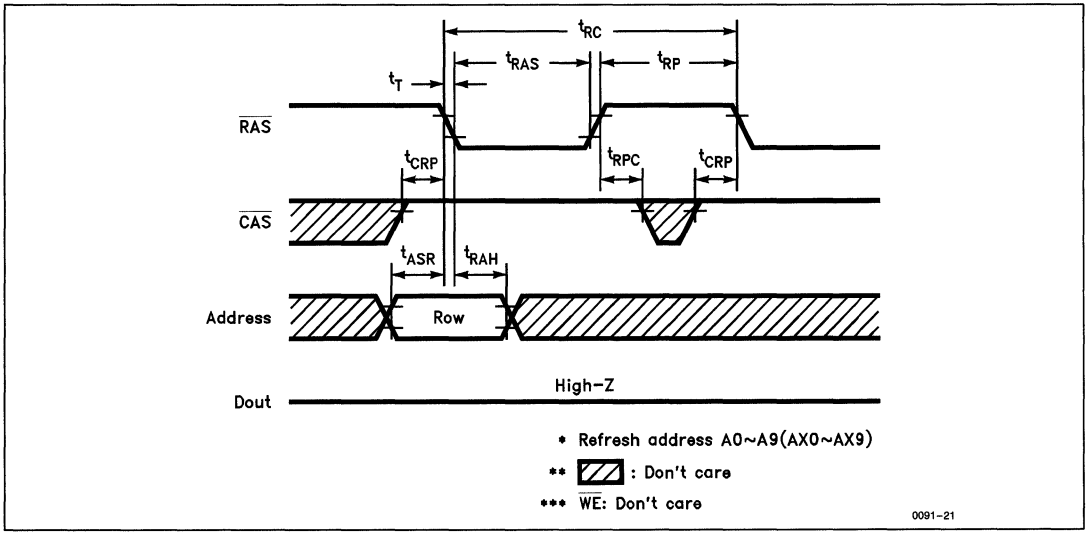
• **Test Mode Set Cycle**
WE And CAS Before RAS Refresh



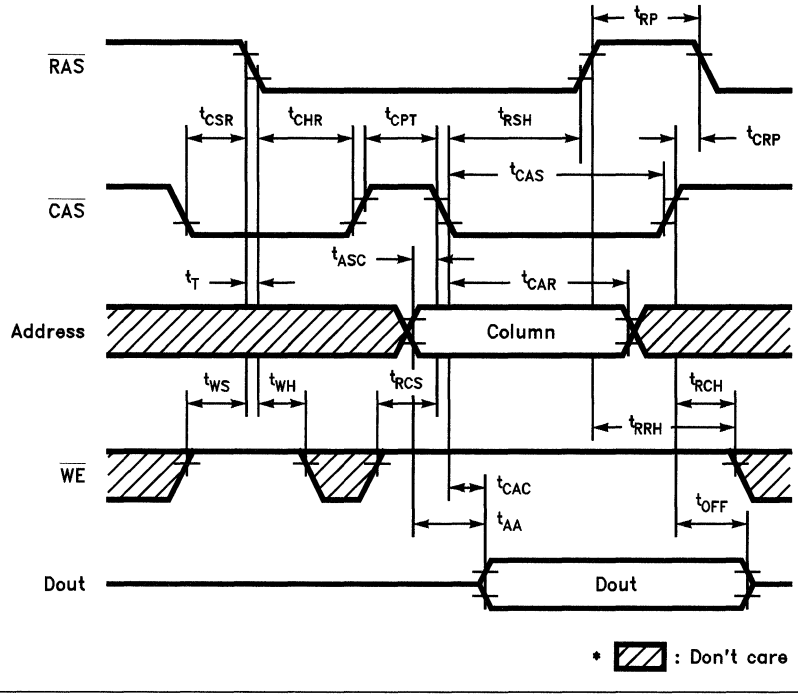
• **Test Mode Reset Cycle**
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



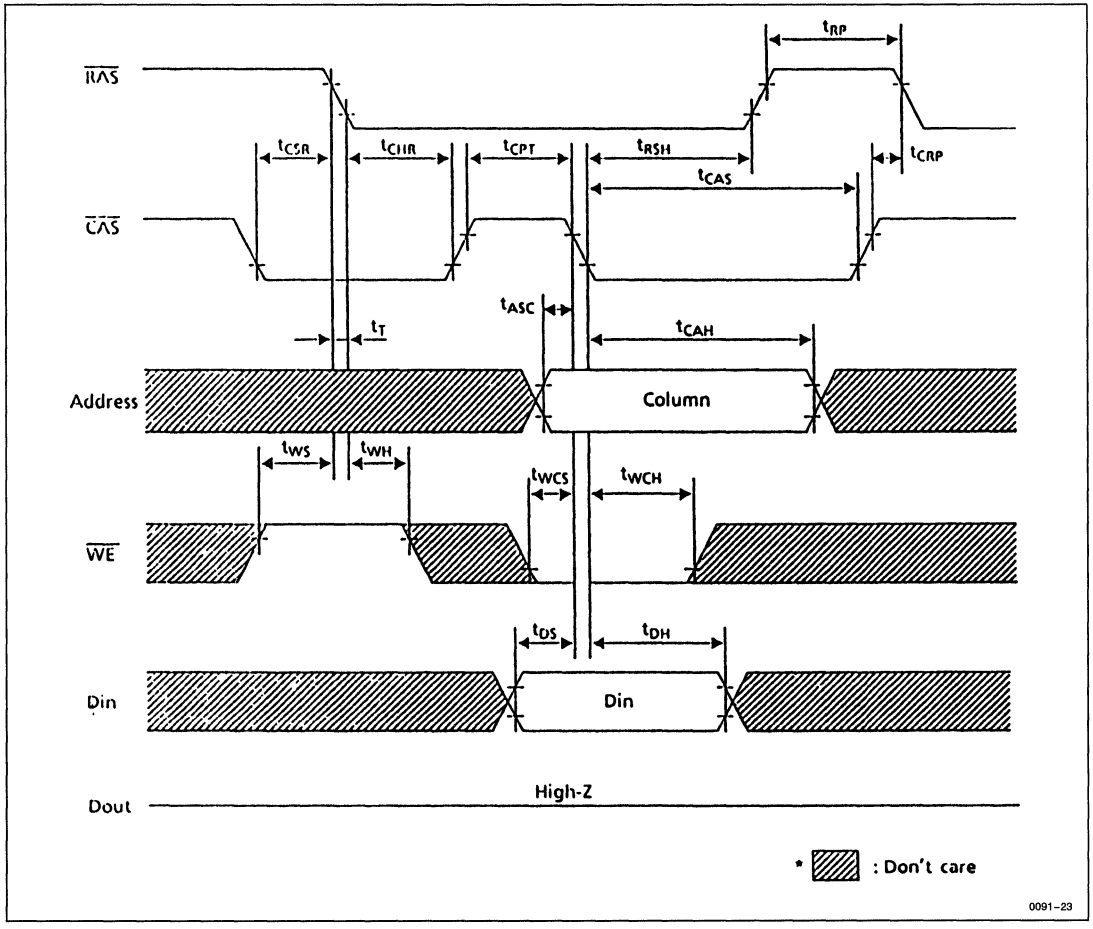
$\overline{RAS}$ Only Refresh Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM514400A Series — Preliminary

HM514400AL Series Low Power Version

HM514400ASL Series Super Low Power Version

1,048,576-Word x 4-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514400A is a CMOS dynamic RAM organized 1,048,576 word x 4-bit. HM514400A has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514400A offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514400A to be packaged in standard 350 mil 20-pin plastic SOJ, standard 300 mil 20-pin plastic SOJ, standard 400 mil 20-pin plastic ZIP, 20-pin plastic TSOP I, 20-pin plastic TSOP I reverse type, 20-pin plastic TSOP II, and 20-pin plastic TSOP II reverse type.

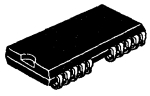
■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode .....605 mW/550 mW/495 mW/440 mW (max)
  - Standby Mode .....11 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles .....(16 ms, 128 ms, 256 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Test Function
- Battery Backup Operation
  - HM514400AL Series (L-Version)
- Data Retention Operation
  - HM514400ASL Series (SL-Version)

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM514400AJ/ALJ/ASLJ-6 HM514400AJ/ALJ/ASLJ-7 HM514400AJ/ALJ/ASLJ-8 HM514400AJ/ALJ/ASLJ-10	60 ns 70 ns 80 ns 100 ns	350 mil 20-pin Plastic SOJ (CP-20DA)
HM514400AS/ALS/ASLS-6 HM514400AS/ALS/ASLS-7 HM514400AS/ALS/ASLS-8 HM514400AS/ALS/ASLS-10	60 ns 70 ns 80 ns 100 ns	300 mil 20-pin Plastic SOJ (CP-20D)
HM514400AZ/ALZ/ASLZ-6 HM514400AZ/ALZ/ASLZ-7 HM514400AZ/ALZ/ASLZ-8 HM514400AZ/ALZ/ASLZ-10	60 ns 70 ns 80 ns 100 ns	400 mil 20-pin Plastic ZIP (ZP-20)
HM514400AT/ALT/ASLT-6 HM514400AT/ALT/ASLT-7 HM514400AT/ALT/ASLT-8 HM514400AT/ALT/ASLT-10	60 ns 70 ns 80 ns 100 ns	20-pin Plastic TSOP I (TFP-20DA)
HM514400AR/ALR/ASLR-6 HM514400AR/ALR/ASLR-7 HM514400AR/ALR/ASLR-8 HM514400AR/ALR/ASLR-10	60 ns 70 ns 80 ns 100 ns	20-pin Plastic TSOP I Reverse Type (TFP-20DAR)
HM514400ATT/ALTT/ASLTT-6 HM514400ATT/ALTT/ASLTT-7 HM514400ATT/ALTT/ASLTT-8 HM514400ATT/ALTT/ASLTT-10	60 ns 70 ns 80 ns 100 ns	20-pin Plastic TSOP II (TTP-20D)
HM514400ARR/ALRR/ASLRR-6 HM514400ARR/ALRR/ASLRR-7 HM514400ARR/ALRR/ASLRR-8 HM514400ARR/ALRR/ASLRR-10	60 ns 70 ns 80 ns 100 ns	20-pin Plastic TSOP II Reverse Type (TTP-20DR)

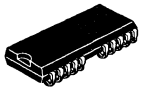
HM514400AJ/ALJ/ALSJ Series



3DCP20DA

(CP-20DA)

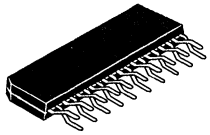
HM514400AS/ALS/ASLS Series



3DCP20D

(CP-20D)

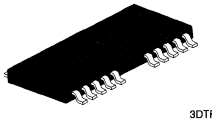
HM514400AZ/ALZ/ASLZ Series



3DZP20

(ZP-20)

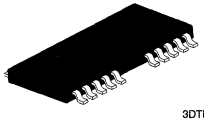
HM514400AT/ALT/ASLT Series



3DTFP20DA

(TFP-20DA)

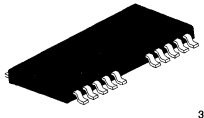
HM514400AR/ALR/ASLR Series



3DTFP20DAR

(TFP-20DAR)

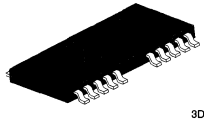
HM514400ATT/ALTT/ASLTT Series



3DTTP20D

(TTP-20D)

HM514400ARR/ALRR/ASLRR Series

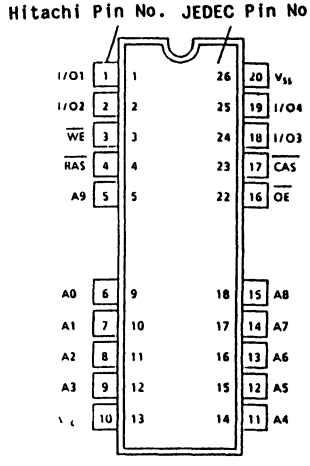


3DTTP20DR

(TTP-20DR)

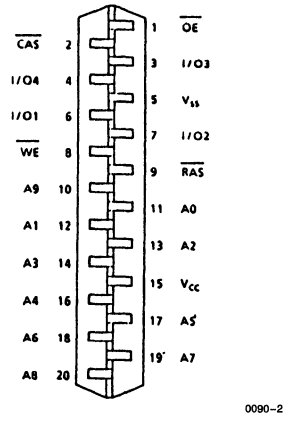
■ PIN OUT

HM514400AJ/ALJ/ASLJ Series
HM514400CAS/ALS/ASLS Series



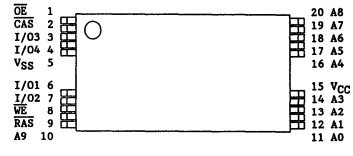
(Top View)

HM514400AZ/ALZ/ASLZ Series



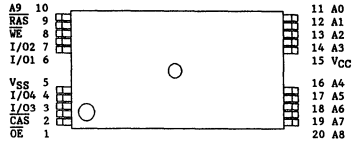
(Bottom View)

HM514400AT/ALT/ASLT Series



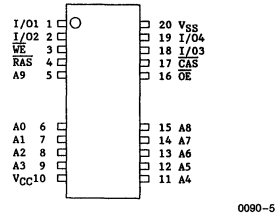
(Top View)

HM514400AR/ALR/ASLR Series



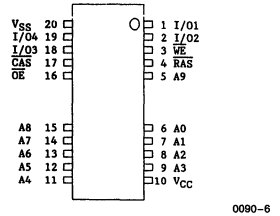
(Top View)

HM514400ATT/ALTT/ASLTT Series



(Top View)

HM514400ARR/ALRR/ASLRR Series



(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_9	Refresh Address Input
I/O_1–I/O_4	Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+ 5V)
V_{SS}	Ground

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)
(T_A = 0 to +60°C (SL-Version)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
			4.0	—	5.5	V	1, 2 (SL-Version)
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	− 1.0	—	0.8	V	1
	(Others)	V_{IL}	− 2.0	—	0.8	V	1

Notes: 1. All voltage referenced to V_{SS}.
2. Data retention operation only.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)
(T_A = 0 to +60°C, V_{CC} = 5V ±10%, V_{SS} = 0V (SL-Version)

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	110	—	100	—	90	—	80	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	1	—	1	—	1	—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
[L-Version] Standby Current		—	200	—	200	—	200	—	200	μA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, $\overline{WE}$, $\overline{OE}$, Address and D_{in} = V_{IH} or V_{IL}, D_{out} = High-Z	4
[SL-Version] Standby Current		—	100	—	100	—	100	—	100	μA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, $\overline{WE}$, $\overline{OE}$, Address and D_{in} = V_{IH} or V_{IL}, D_{out} = High-Z	4
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	110	—	100	—	90	—	80	mA	t_{RC} = Min	2

• **DC Electrical Characteristics** (continued) (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)
(T_A = 0 to +60°C, V_{CC} = 5V ±10%, V_{SS} = 0V (SL-Version)

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max			
Standby Current	I_{CC5}	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	110	—	100	—	90	—	80	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	110	—	100	—	90	—	80	mA	t_{PC} = Min	1, 3
[L-Version] Battery Backup Operating Current (Standby with CBR Refresh)	I_{CC10}	—	300	—	300	—	300	—	300	µA	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, $\overline{WE}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, $\overline{OE}$, Address and D_{in} = V_{IH} or V_{IL}, D_{out} = High-Z	4
[SL-Version] Data Retention Current (Equivalent Refresh Time is 256 ms)	I_{CC10}	—	150	—	150	—	150	—	150	µA	t_{RC} = 250 µs, t_{RAS} ≤ 200 ns, $\overline{WE}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, $\overline{OE}$, Address and D_{in} = V_{IH} or V_{IL}, D_{out} = High-Z, 4.0V ≤ V_{CC} ≤ 5.5V	4
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	−10	10	µA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	−10	10	µA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. V_{CC} − 0.2V ≤ V_{IH} ≤ 6.5V and 0V ≤ V_{IL} ≤ 0.2V.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 14, 15, 16]
(T_A = 0 to 60°C, V_{CC} = 5V ±10%, V_{SS} = 0V (SL-Version))

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10000	20	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	20	60	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	15	—	20	—	20	—	25	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	0	—	ns	
$\overline{CAS}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	—	16	ms	
Refresh Period (L-Version)	t_{REF}	—	128	—	128	—	128	—	128	ms	
Refresh Period (SL-Version)	t_{REF}	—	16	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	2, 3, 17
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	—	25	ns	3, 4, 13, 17
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	ns	3, 5, 13, 17
Access Time from $\overline{OE}$	t_{OAC}	—	15	—	20	—	20	—	25	ns	3, 17
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	ns	18
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	0	—	ns	18
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	15	0	20	0	20	0	25	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	15	0	20	0	20	0	25	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	15	—	20	—	20	—	25	—	ns	

Write Cycle

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	10	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	20	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	20	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	150	—	180	—	200	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	95	—	105	—	135	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	35	—	45	—	45	—	60	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	50	—	60	—	65	—	80	—	ns	10
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	15	—	20	—	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time in Normal Mode	t_{CPN}	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	35	—	40	—	45	—	50	ns	3, 13, 17
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	45	—	50	—	ns	
Fast Page Mode Read-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPW}	55	—	65	—	70	—	85	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	80	—	95	—	100	—	110	—	ns	

Test Mode Cycle

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	10	—	10	—	10	—	10	—	ns	

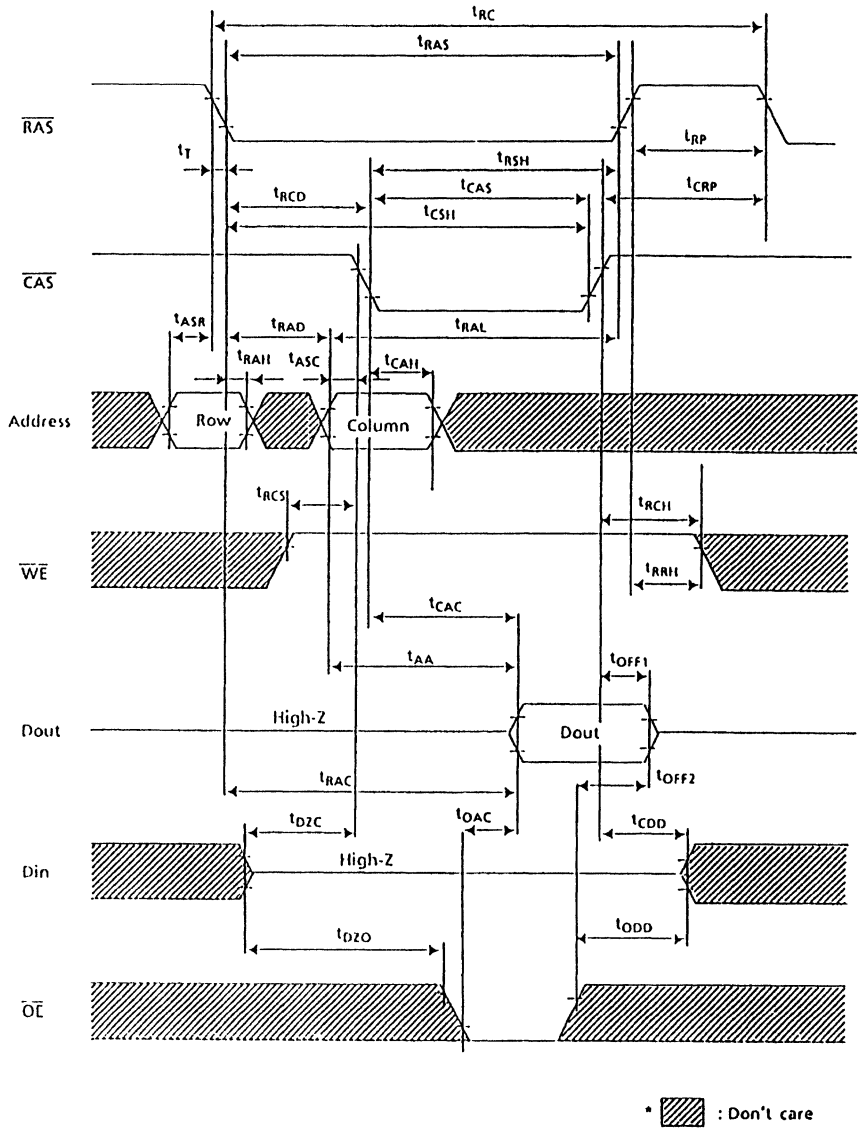
Counter Test Cycle

Parameter	Symbol	HM514400A-6		HM514400A-7		HM514400A-8		HM514400A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	40	—	40	—	50	—	ns	

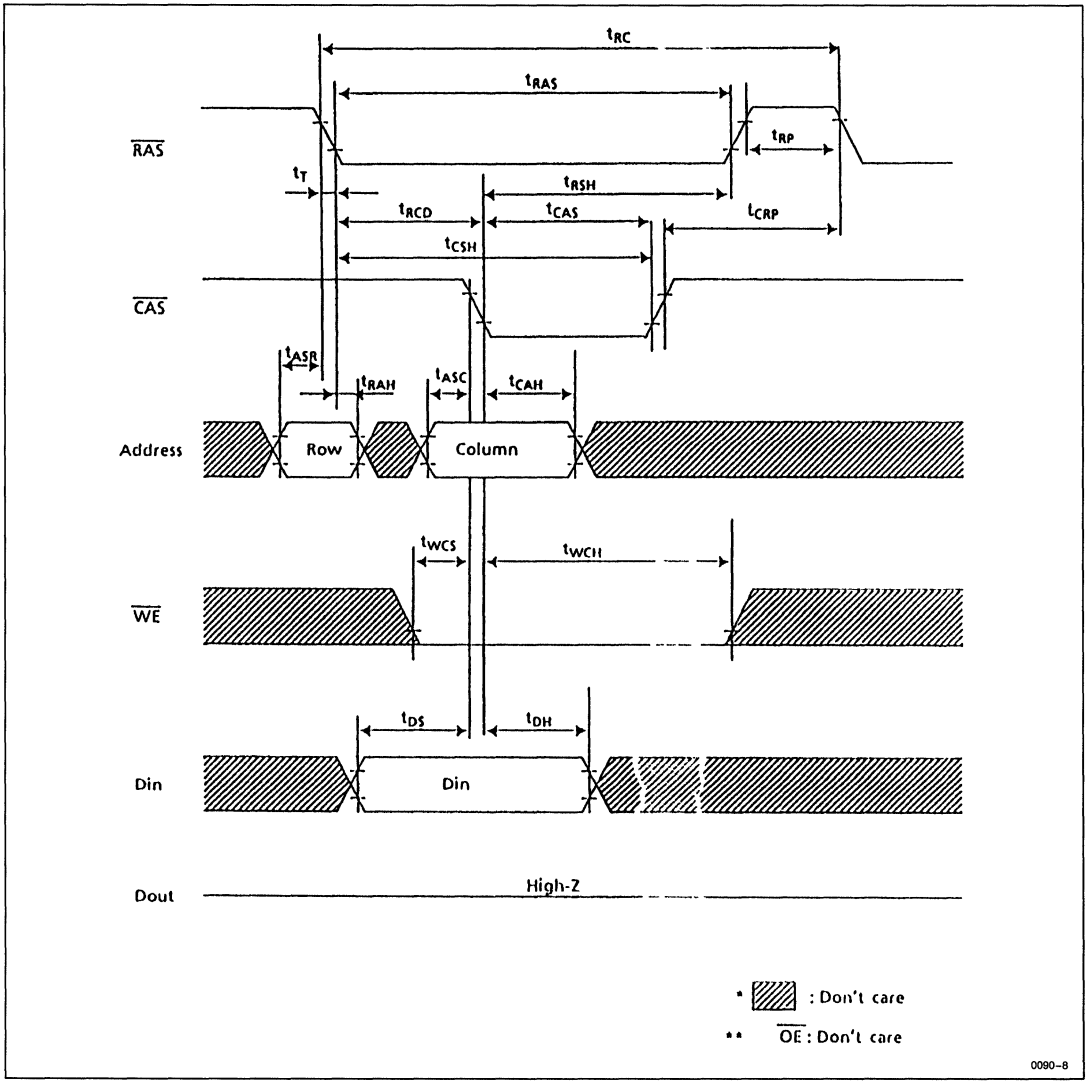
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and t_{RAD} (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, OE must disable output buffer prior to applying data to the device.
16. Test mode operation specified in this data sheet is 2-bit test function controlled by control address bits ... CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of two test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC}, t_{OAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORMS

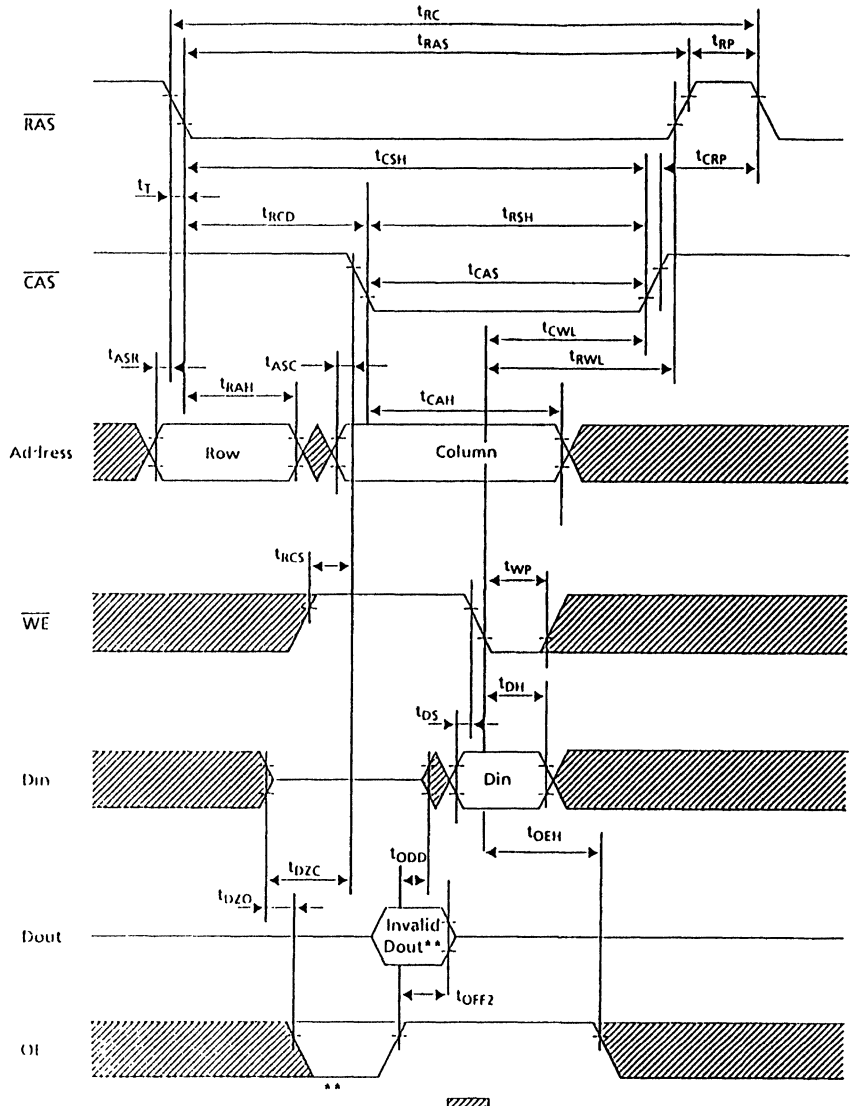
• Read Cycle



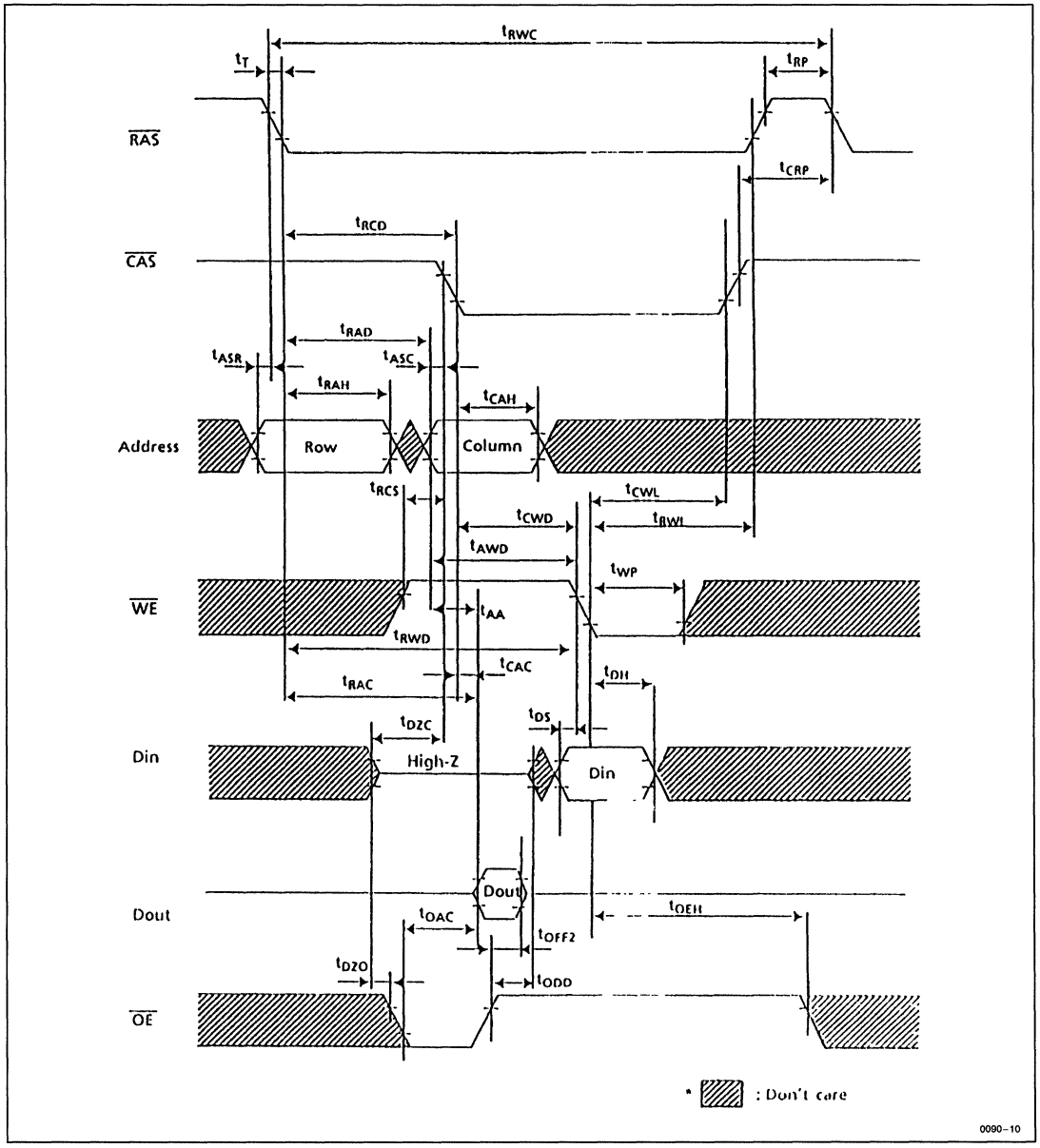
• **Early Write Cycle**



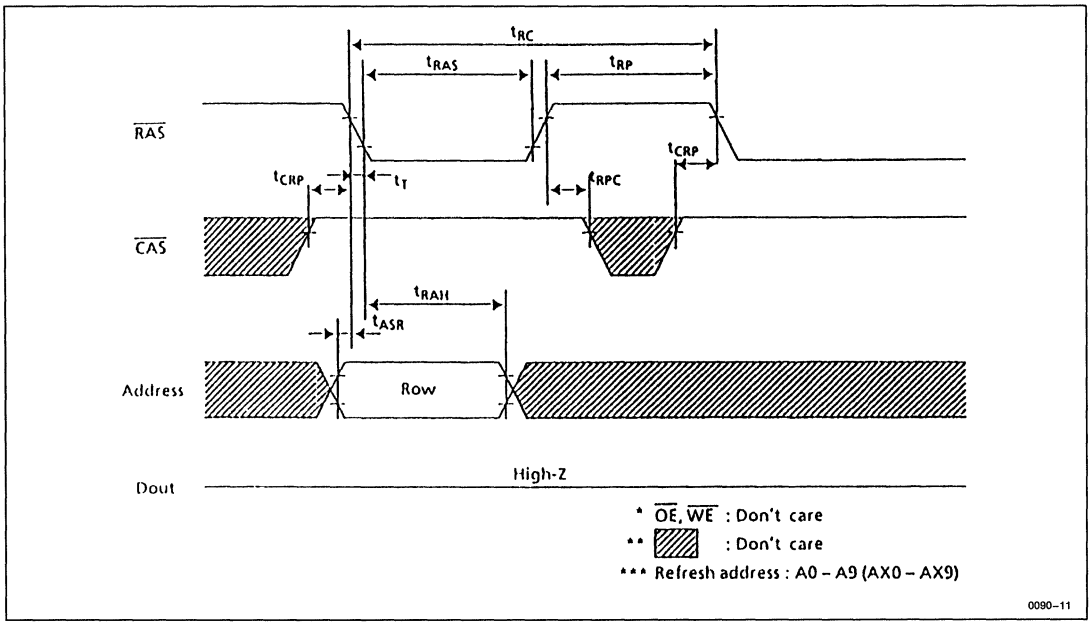
• **Delayed Write Cycle**



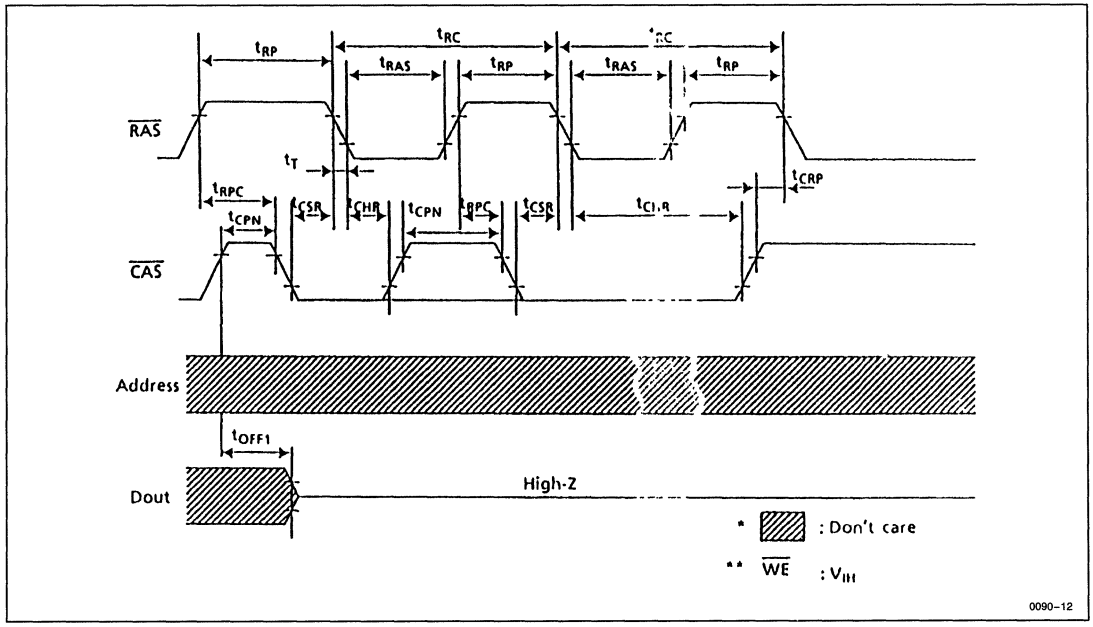
• Read-Modify-Write Cycle



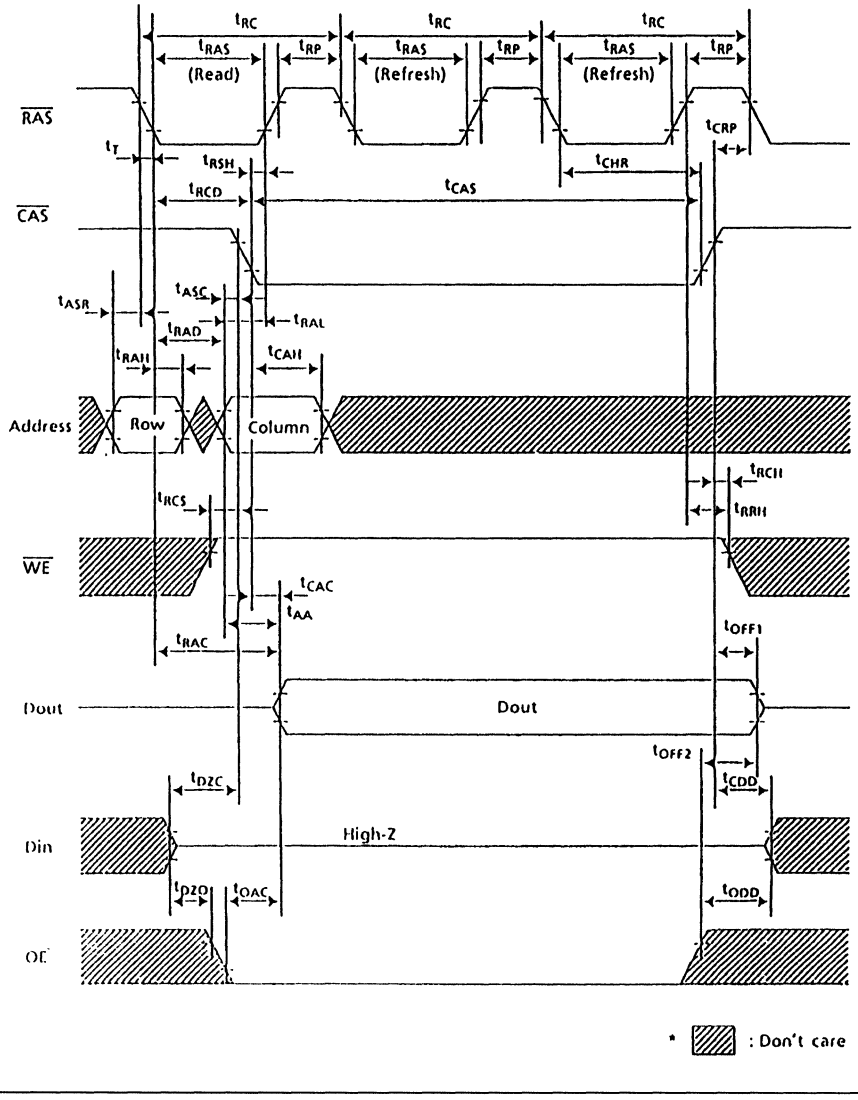
• $\overline{RAS}$ Only Refresh Cycle



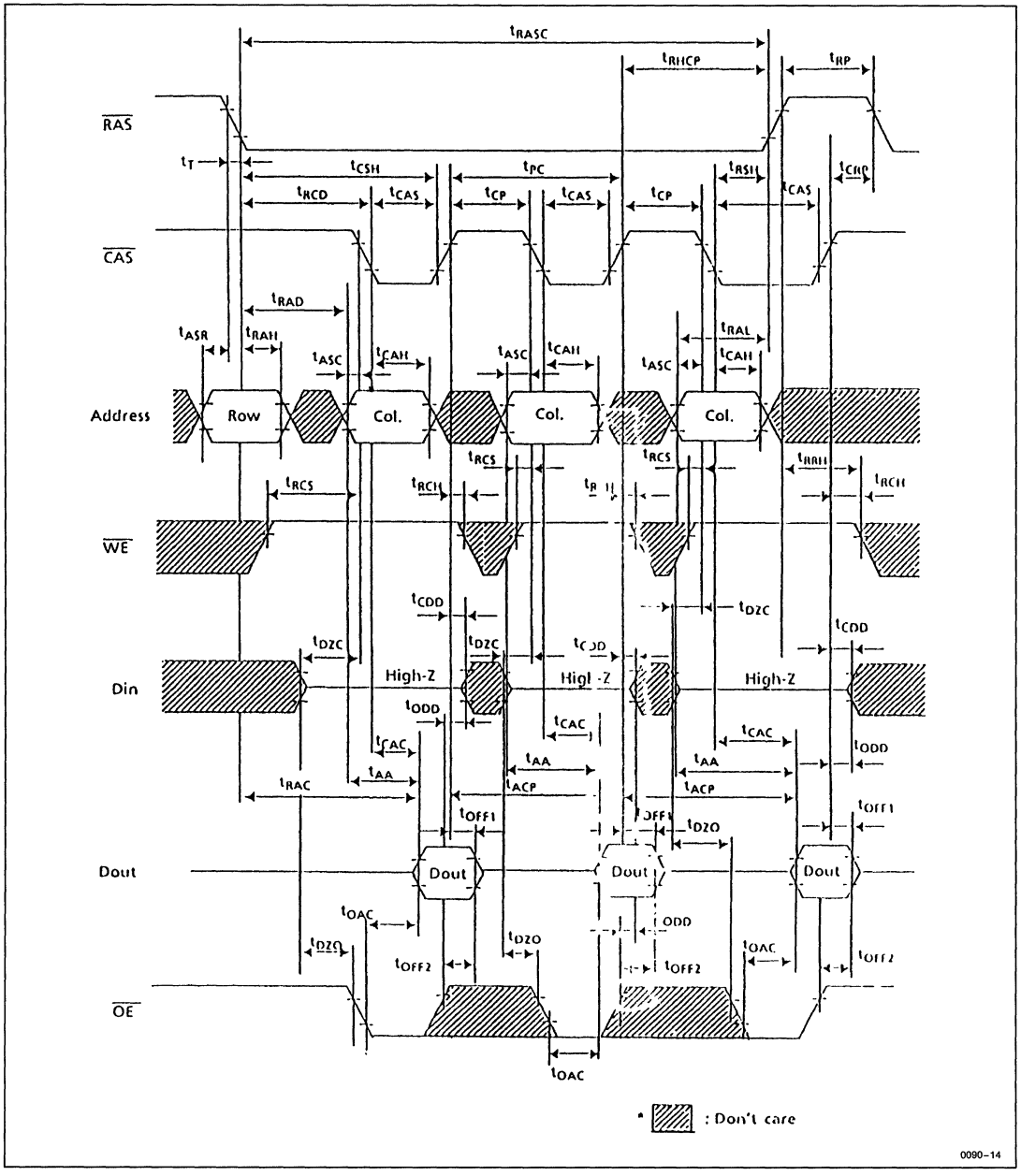
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



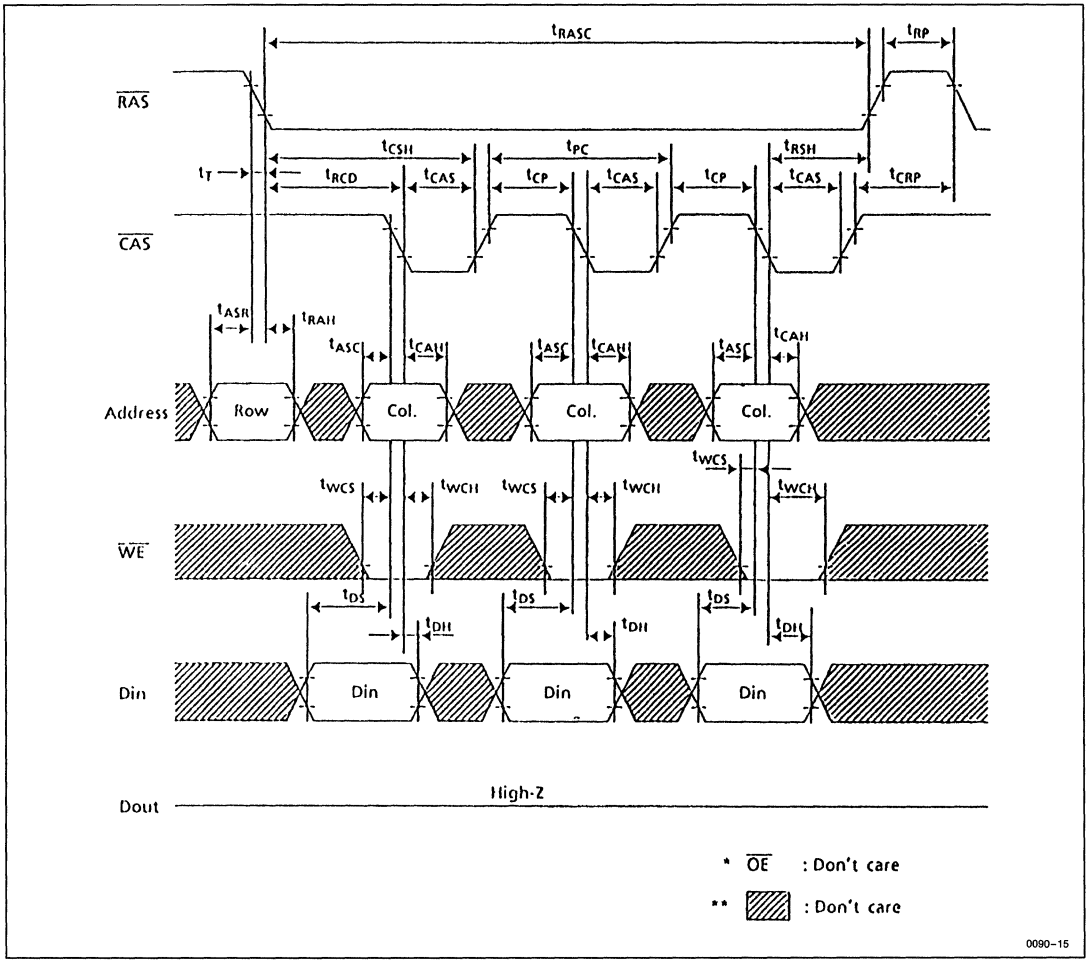
• Hidden Refresh Cycle



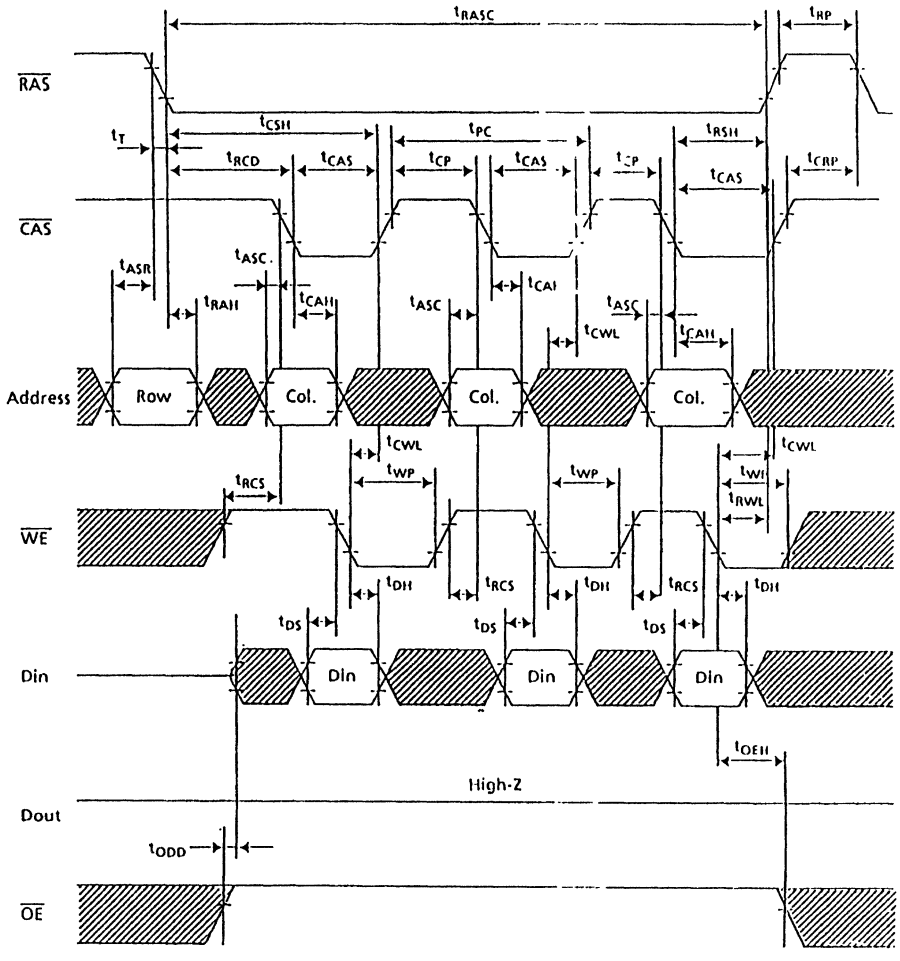
• **Fast Page Mode Read Cycle**



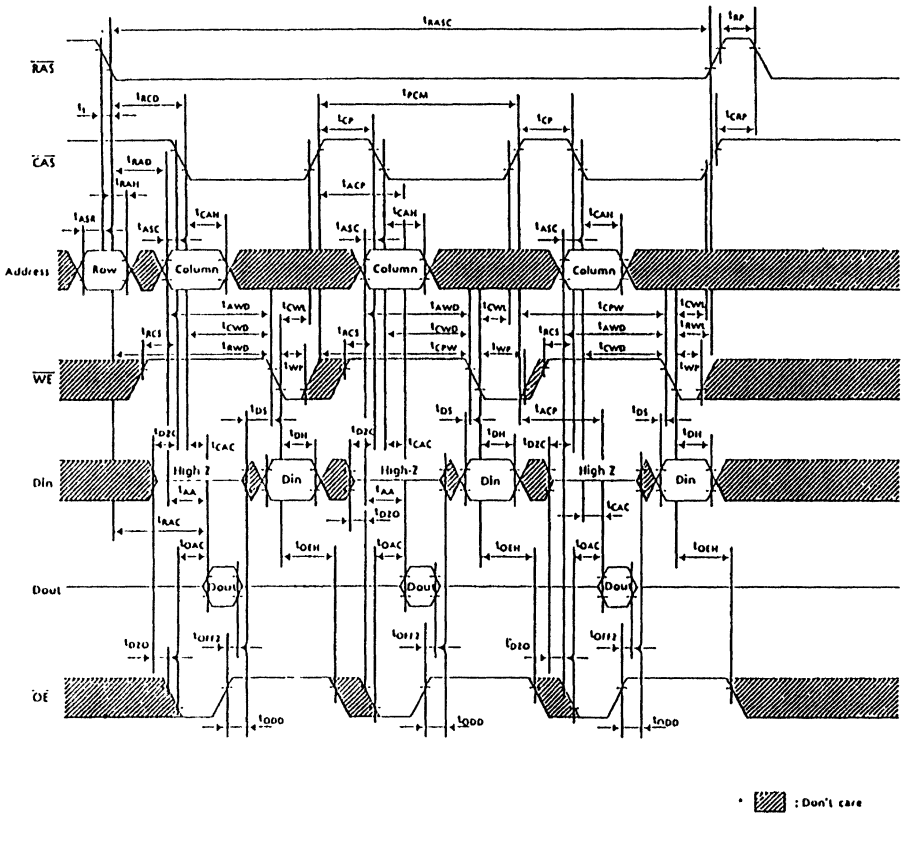
• Fast Page Mode Early Write Cycle



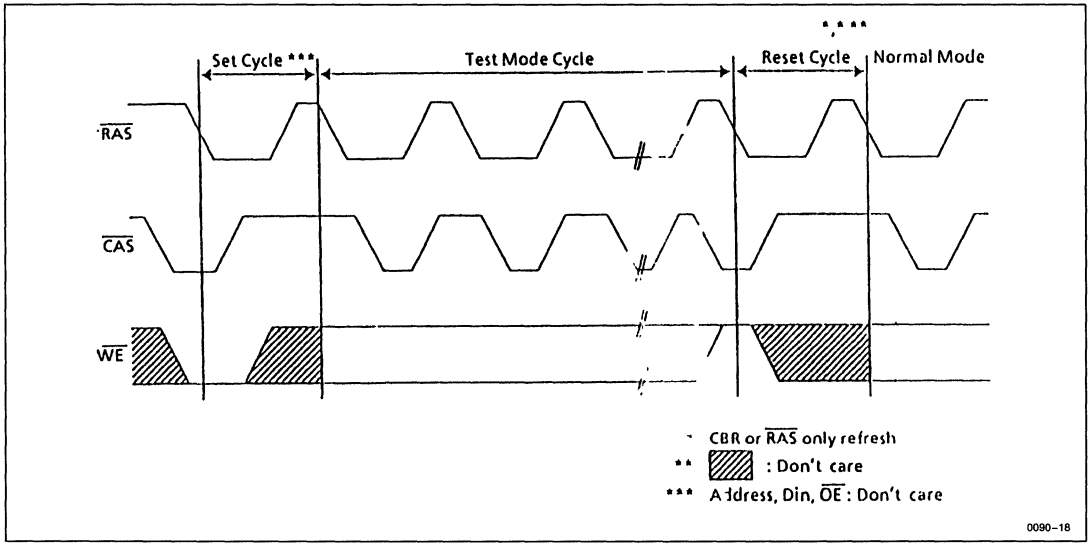
• **Fast Page Mode Delayed Write Cycle**



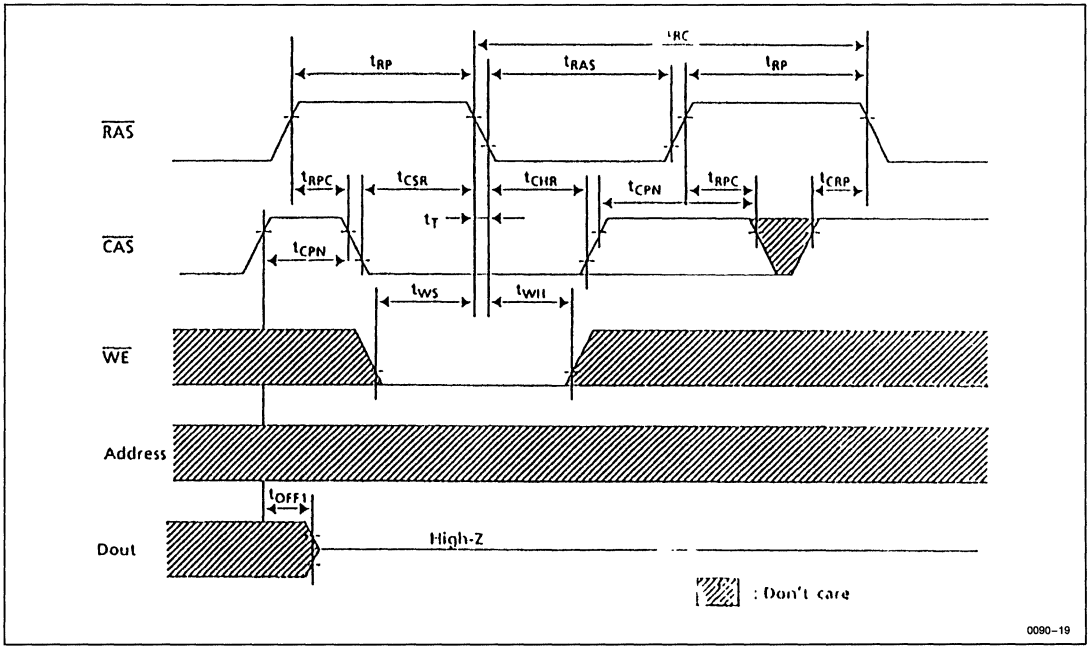
• Fast Page Mode Read-Modify-Write Cycle



• **TEST MODE CYCLE**

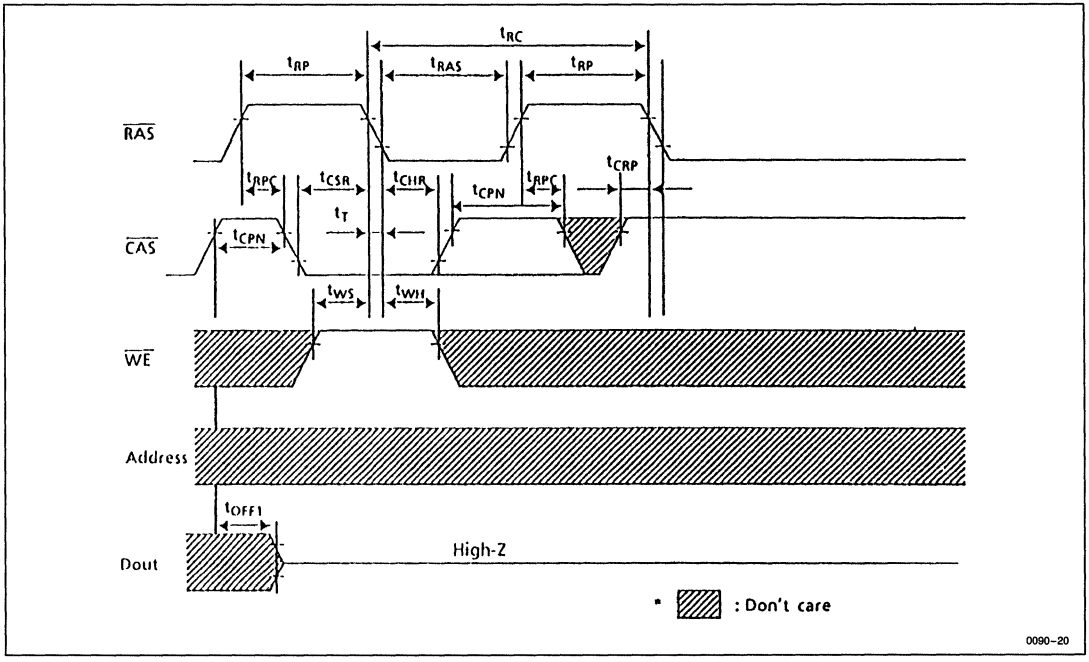


• **Test Mode Set Cycle**
WE And CAS Before RAS Refresh

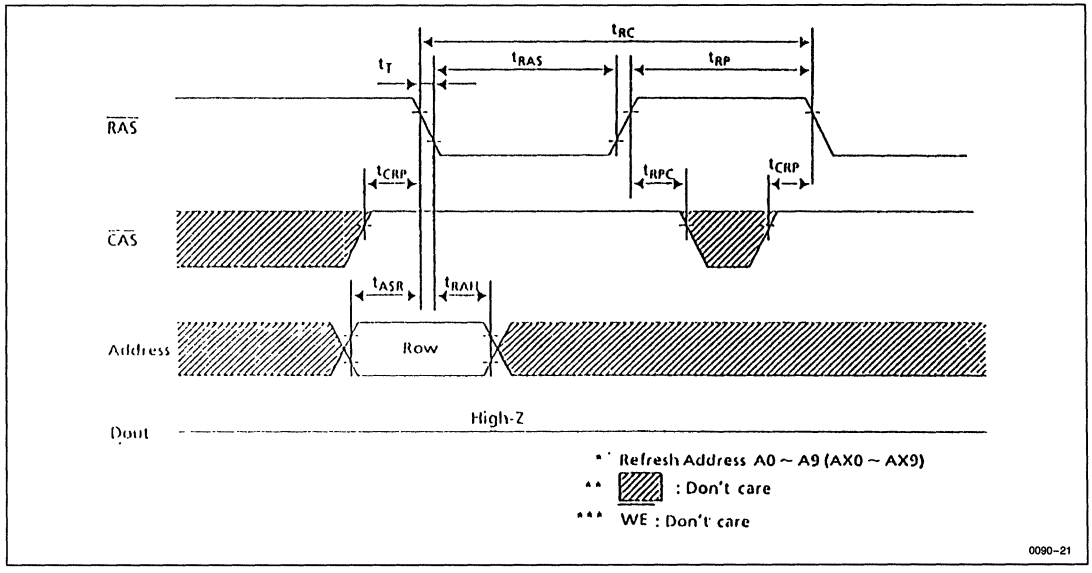


- **Test Mode Reset Cycle**

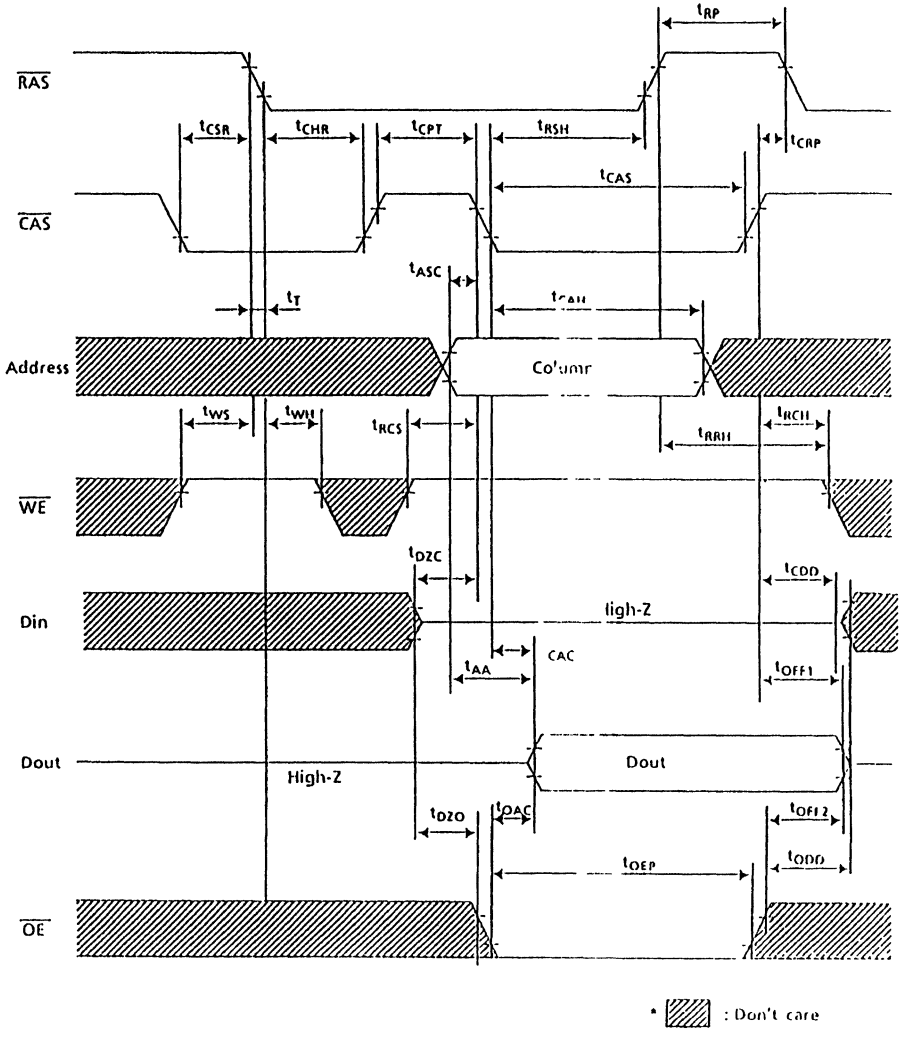
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



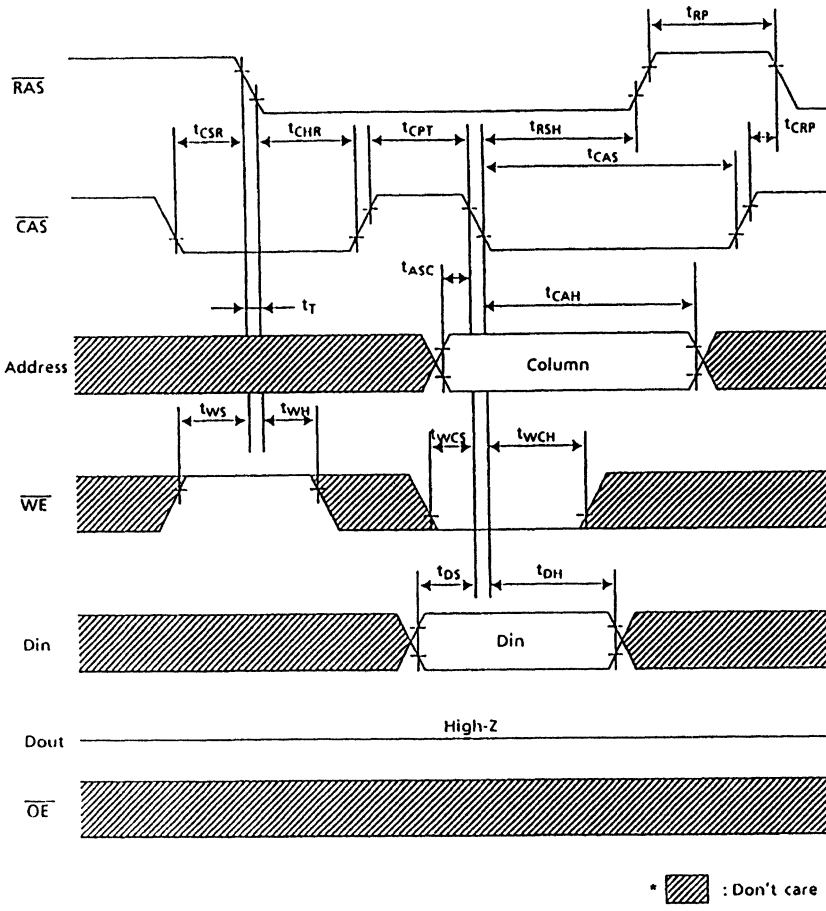
$\overline{RAS}$ Only Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM514100 Series

4,194,304-Word x 1-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514100 is a CMOS dynamic RAM organized 4,194,304 word x 1-bit. HM514100 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514100 offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514100 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time ..... 80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode ..... 495 mW/440 mW/385 mW (max)
  - Standby Mode ..... 11 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles ..... (16 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Test Function

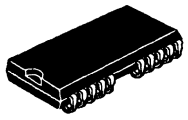
■ ORDERING INFORMATION

Part No.	Access	Package
HM514100JP-8	80 ns	350 mil 20-pin
HM514100JP-10	100 ns	Plastic SOJ
HM514100JP-12	120 ns	(CP-20DA)
HM514100ZP-8	80 ns	400 mil 20-pin
HM514100ZP-10	100 ns	Plastic ZIP
HM514100ZP-12	120 ns	(ZP-20)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{10}	Address Input
A_0–A_9	Refresh Address Input
D_{in}	Data-in
D_{out}	Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

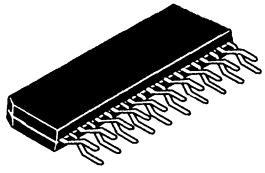
HM514400JP Series



3DCP20DA

(CP-20DA)

HM514400ZP Series

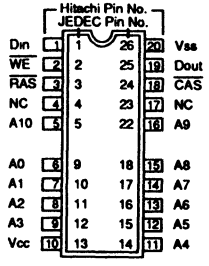


3DZP20

(ZP-20)

■ PIN OUT

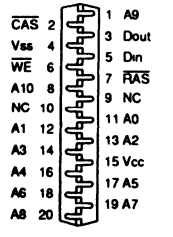
HM514100JP Series



0061-1

(Top View)

HM514100ZP Series



0061-2

(Bottom View)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Disspation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	− 2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Test Condition	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	70	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	1	—	1	—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	90	—	80	—	70	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	90	—	80	—	70	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	90	—	80	—	70	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less $\overline{CAS}$ = V_{IH}.

• Capacitance (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address, Data-in)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-out)	C_O	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 12, 15]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	150	—	180	—	210	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3, 16
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4, 14
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5, 14, 16
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	ns	6

Write Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	20	—	25	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	180	—	210	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	100	—	120	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	25	—	25	—	30	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40	—	45	—	55	—	ns	10

Refresh Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	14, 16
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	85	—	85	—	100	—	ns	

Test Mode Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	20	—	20	—	20	—	ns	

Counter Test Cycle

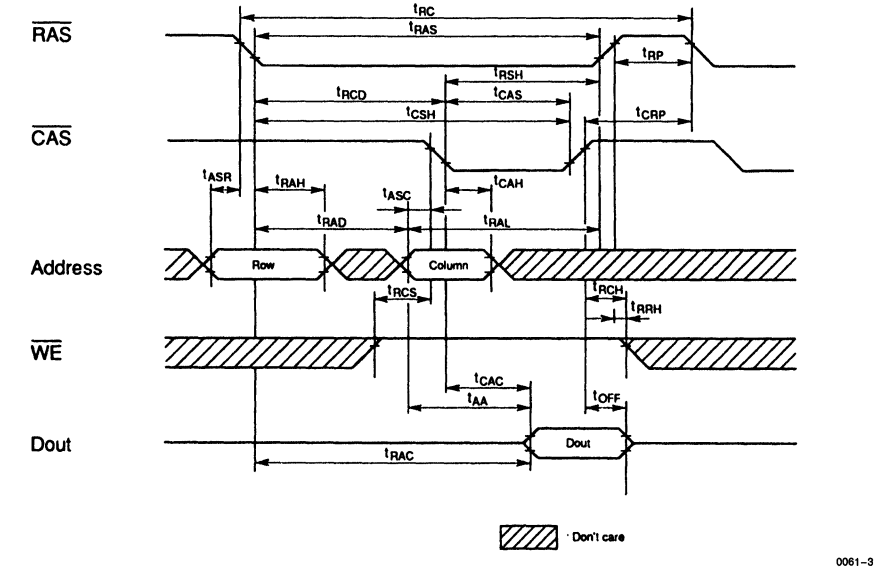
Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	50	—	60	—	ns	

Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq T_{RCD}$ (max) and t_{RAD} (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.

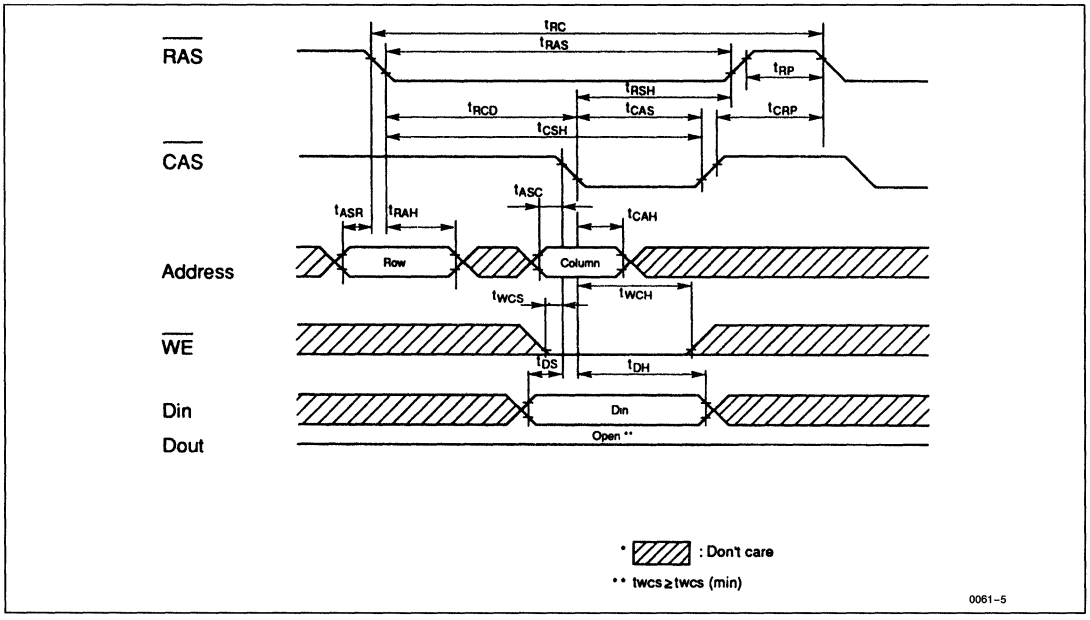
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits—RA10, CA10 and CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is D_{out} and data input pin is D_{in}. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
16. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORMS

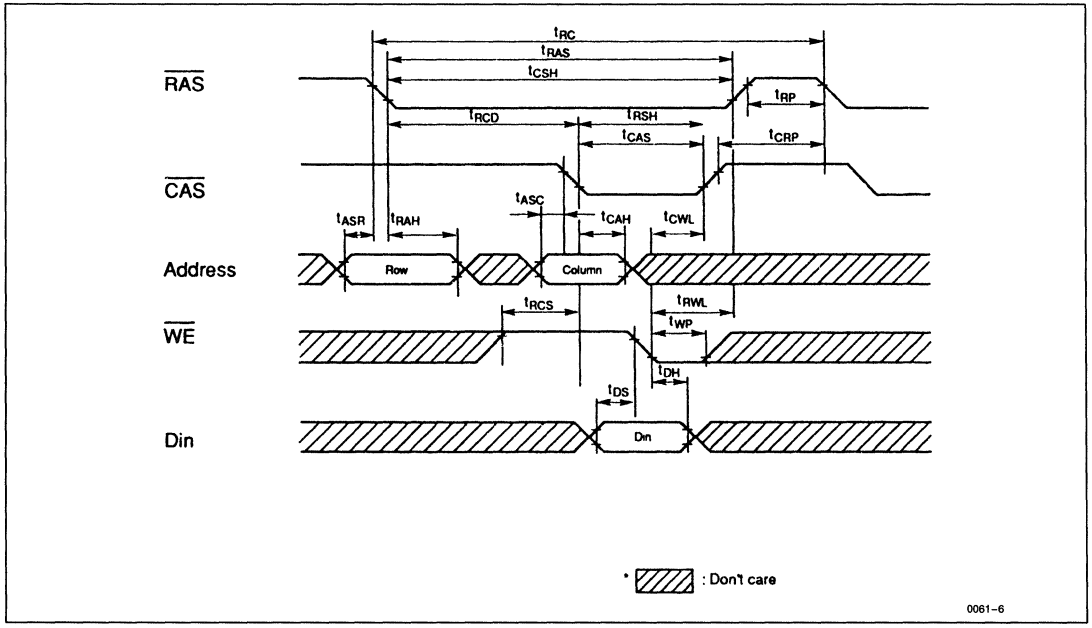
• Read Cycle



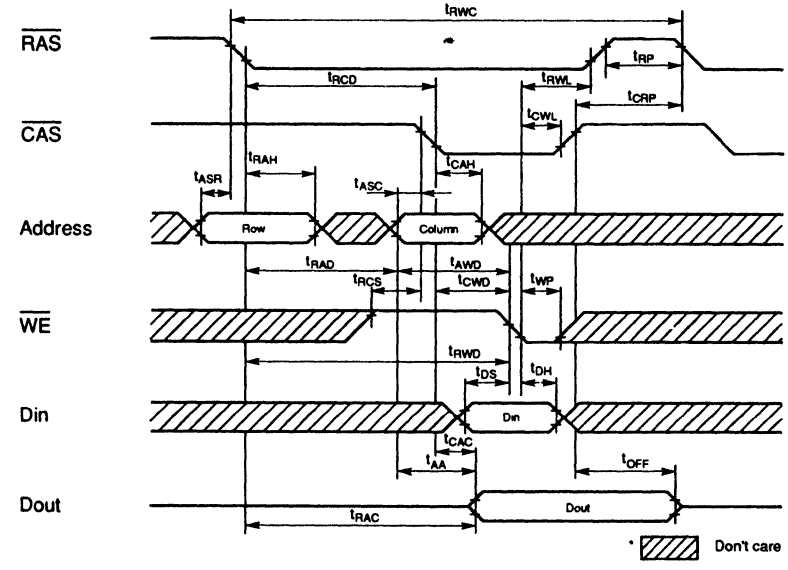
• Early Write Cycle



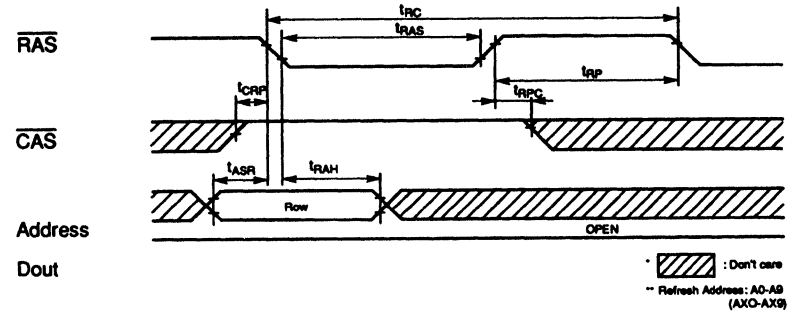
• Delayed Write Cycle



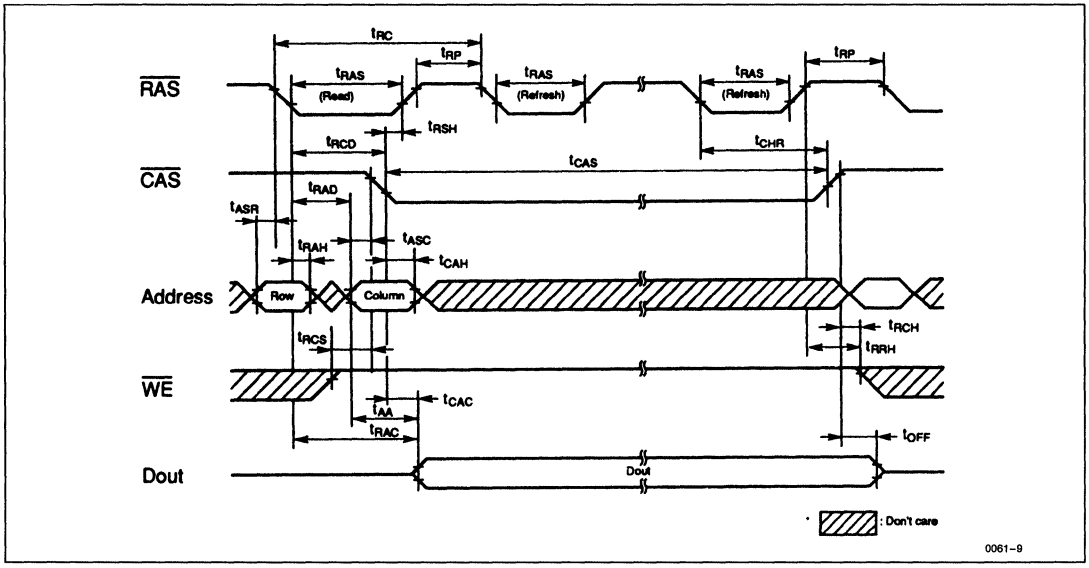
• **Read-Modify-Write Cycle**



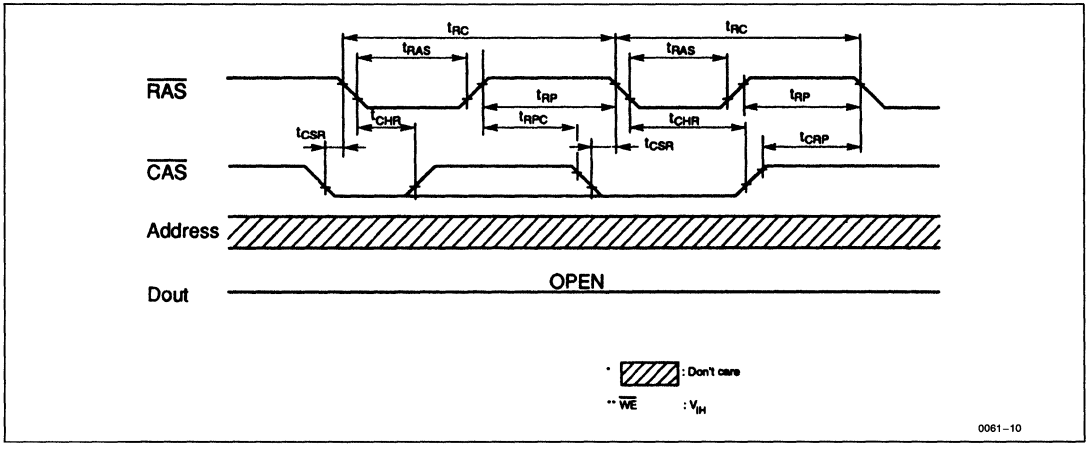
• **$\overline{RAS}$ Only Refresh Cycle**



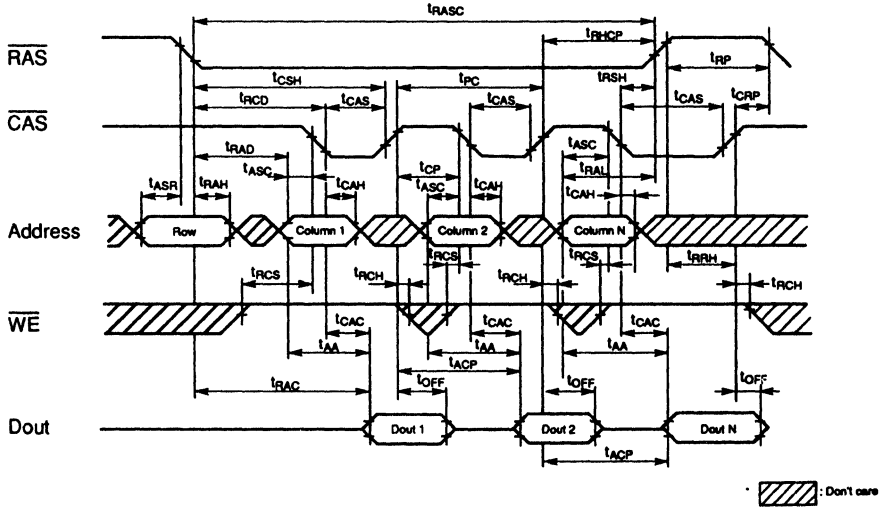
• Hidden Refresh Cycle



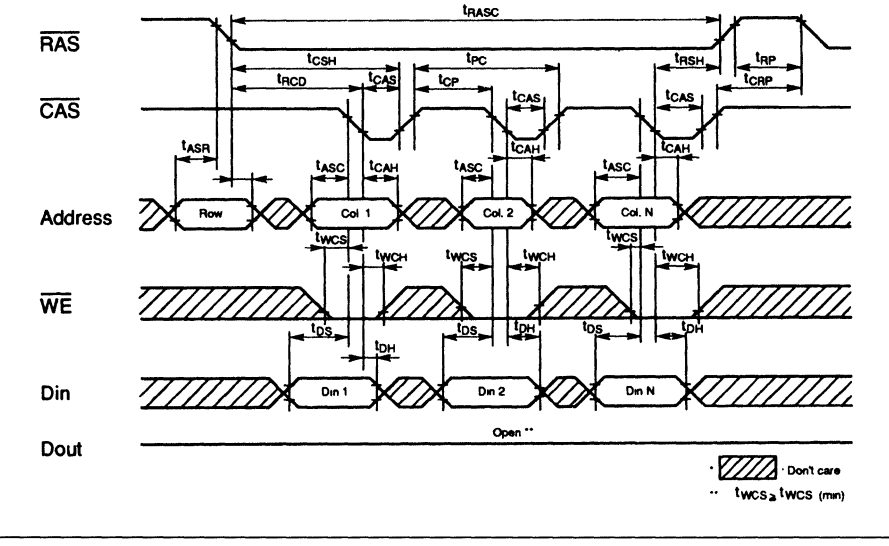
CAS Before RAS Refresh Cycle



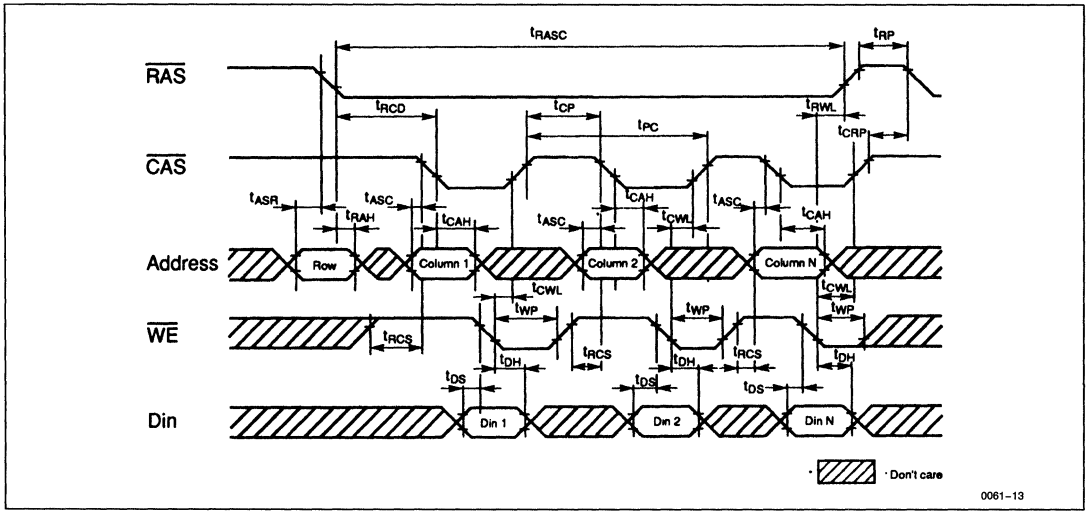
• **Fast Page Mode Read Cycle**



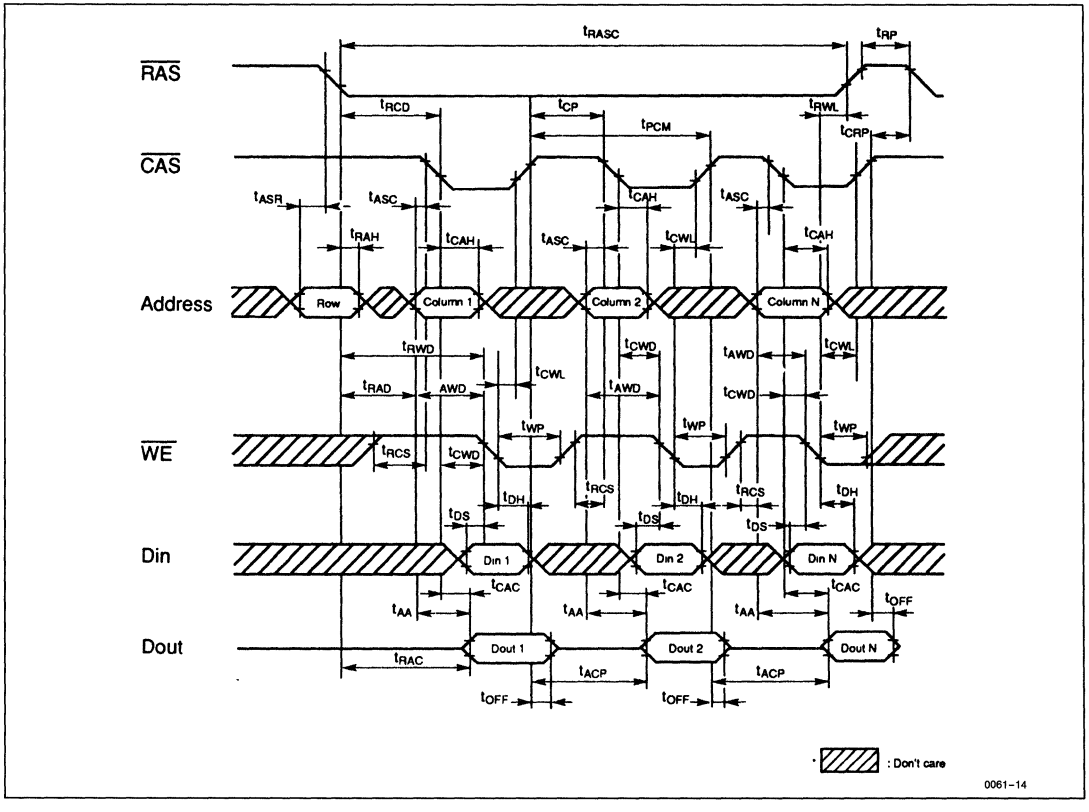
• **Fast Page Mode Early Write Cycle**



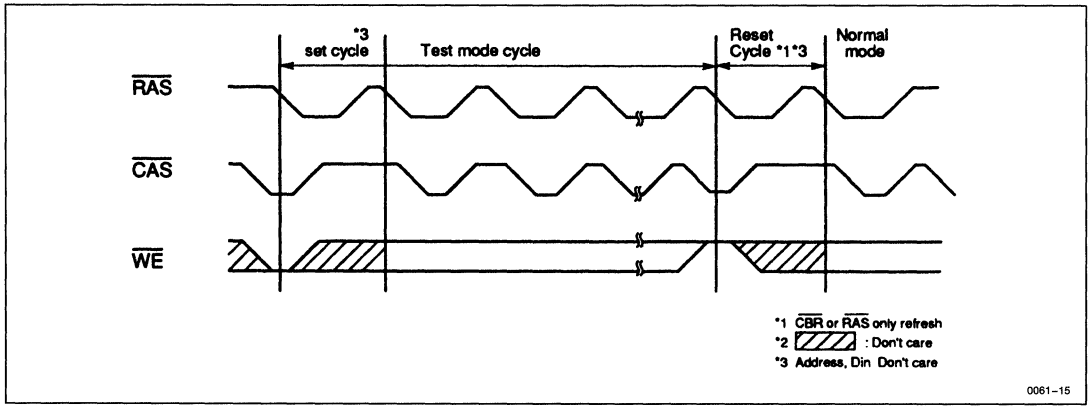
• **Fast Page Delayed Write Cycle**



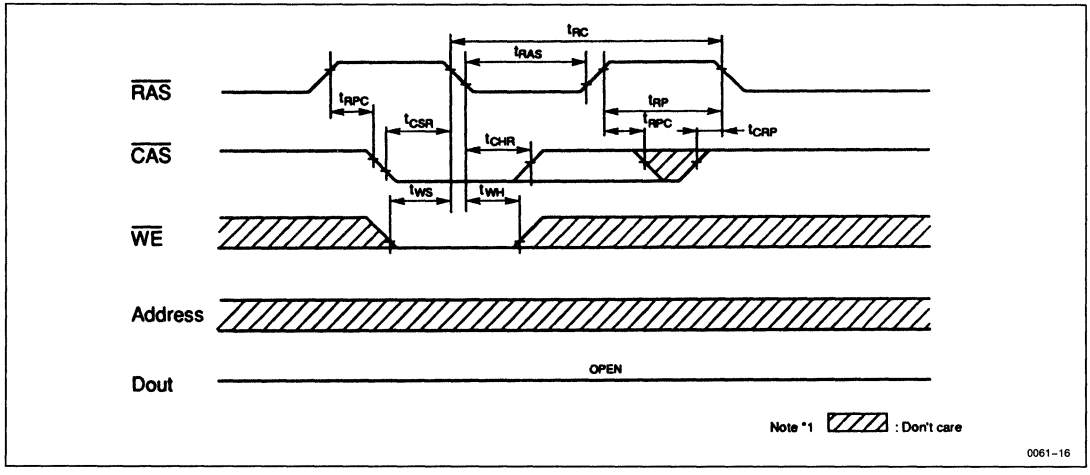
• **Fast Page Mode Read-Modify-Write Cycle**



• **Test Mode Cycle**

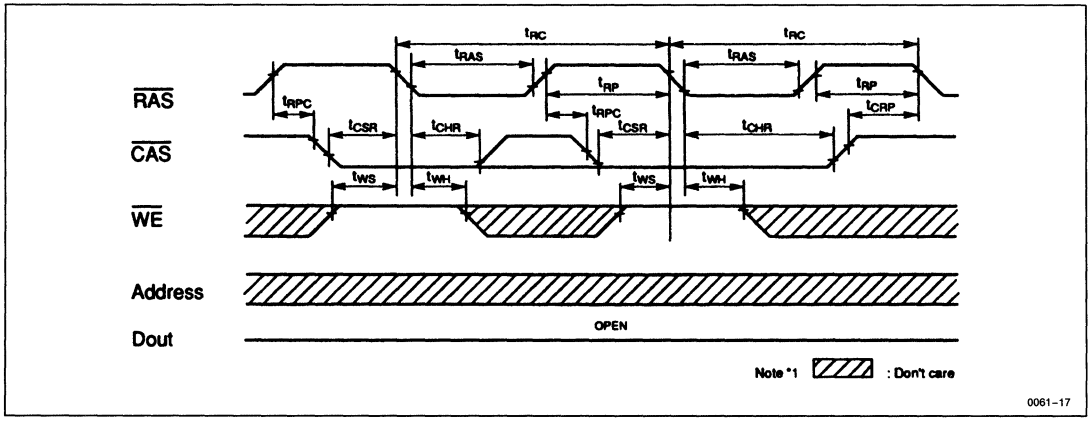


• **Test Mode Set Cycle**

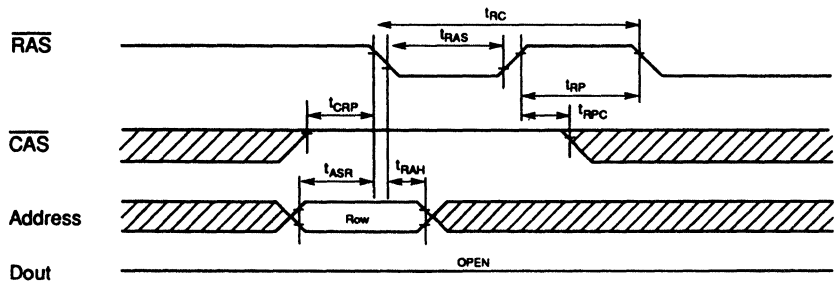


■ TEST MODE RESET CYCLE

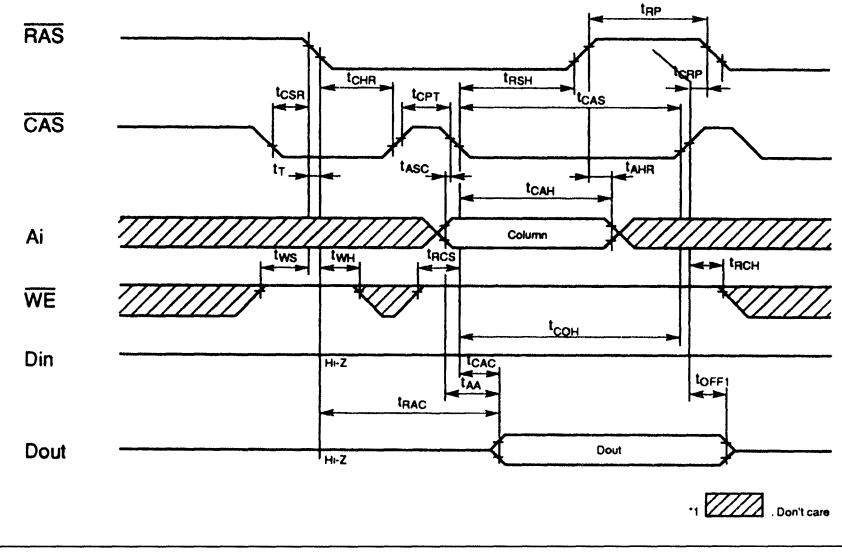
• **CAS Before RAS Refresh Cycle**



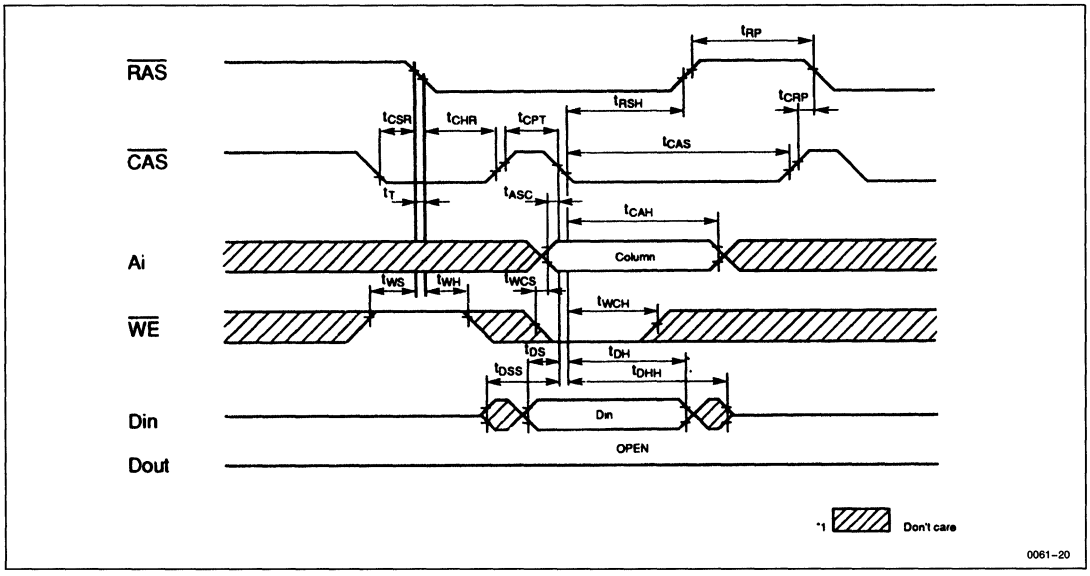
• $\overline{RAS}$ Only Refresh Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (READ)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (WRITE)



■ 4M DRAM LOW POWER VERSION

The specification on the low power version is the same as the standard 4 Megabit DRAM with the exception of the following parameters.

Item	Conditions	Spec.
Type No.	4M x 1	HM514100LJP/LZP
	1M x 4	
Temperature	—	0–55°C
I_{CC2} (Standby CMOS Interface)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ ≥ V_{CC} − 0.2V Other Pin ≥ V_{CC} − 0.2V or ≤ 0.2V (Address and D_{in} is Stable) D_{out}: High-Z	200 µA Max
I_{CC10} (Standby with CBR Refresh)	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs $\overline{V_{IL}}1$ ≥ V_{CC} − 0.2V, V_{IL} ≤ 0.2V $\overline{WE}$ and $\overline{OE}$ = V_{IH}, Address and D_{in} is Stable D_{out}: High-Z	300 µA Max
Refresh t_{REF}		128 ms

*only for 1M x 4.

HM514100JP/ZP-7

4,194,304-Word x 1-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514100 is a CMOS dynamic RAM organized 4,194,304 word x 1-bit. HM514100 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514100 offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514100 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

■ FEATURES

- Single 5V (±10%, −5%)
- High Speed
  - Access Time ..... 70 ns (max)
- Low Power Dissipation
  - Active Mode ..... 550 mW (max)
  - Standby Mode ..... 11 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles ..... (16 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Test Function

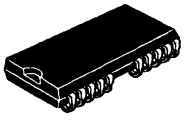
■ ORDERING INFORMATION

Part No.	Access	Package
HM514100JP-7	70 ns	350 mil 20-pin Plastic SOJ (CP-20DA)
HM514100ZP-7	70 ns	400 mil 20-pin Plastic ZIP (ZP-20)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{10}	Address Input
A_0–A_9	Refresh Address Input
D_{in}	Data-in
D_{out}	Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power (+ 5V)
V_{SS}	Ground

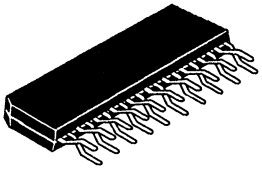
HM514400JP Series



3DCP20DA

(CP-20DA)

HM514400ZP Series

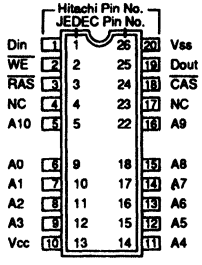


3DZP20

(ZP-20)

■ PIN OUT

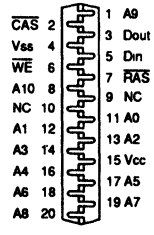
HM514100JP Series



0062-1

(Top View)

HM514100ZP Series



0062-2

(Bottom View)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Disspation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.75	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, −5%, V_{SS} = 0V)

Parameter	Symbol	HM514100-7		Unit	Test Condition	Note
		Min	Max			
Operating Current	I_{CC1}	—	100	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	100	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	100	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	100	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	−10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	V	High I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less $\overline{CAS}$ = V_{IH}.

• Capacitance (T_A = 25°C, V_{CC} = 5V ±10%, −5%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address, Data-in)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-out)	C_O	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, −5%, V_{SS} = 0V)[1, 12, 15]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514100-7		Unit	Note
		Min	Max		
Random Read or Write Cycle Time	t_{RC}	140	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	70	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	ns	
Column Address Setup Time	t_{ASC}	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	70	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	ns	7
Refresh Period	t_{REF}	—	16	ms	

Read Cycle

Parameter	Symbol	HM514100-7		Unit	Note
		Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	70	ns	2, 3, 16
Access Time from $\overline{CAS}$	t_{CAC}	—	25	ns	3, 4, 14
Access Time from Address	t_{AA}	—	40	ns	3, 5, 14, 16
Read Command Setup Time	t_{RCS}	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	ns	6

Write Cycle

Parameter	Symbol	HM514100-7		Unit	Note
		Min	Max		
Write Command Setup Time	t_{WCS}	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	ns	
Write Command Pulse Width	t_{WP}	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514100-7		Unit	Note
		Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	170	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	70	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	25	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40	—	ns	10

Refresh Cycle

Parameter	Symbol	HM514100-7		Unit	Note
		Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514100-7		Unit	Note
		Min	Max		
Fast Page Mode Cycle Time	t_{PC}	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	ns	14, 16
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	50	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM514100-7		Unit	Note
		Min	Max		
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	85	—	ns	

Test Mode Cycle

Parameter	Symbol	HM514100-7		Unit	Note
		Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	20	—	ns	

Counter Test Cycle

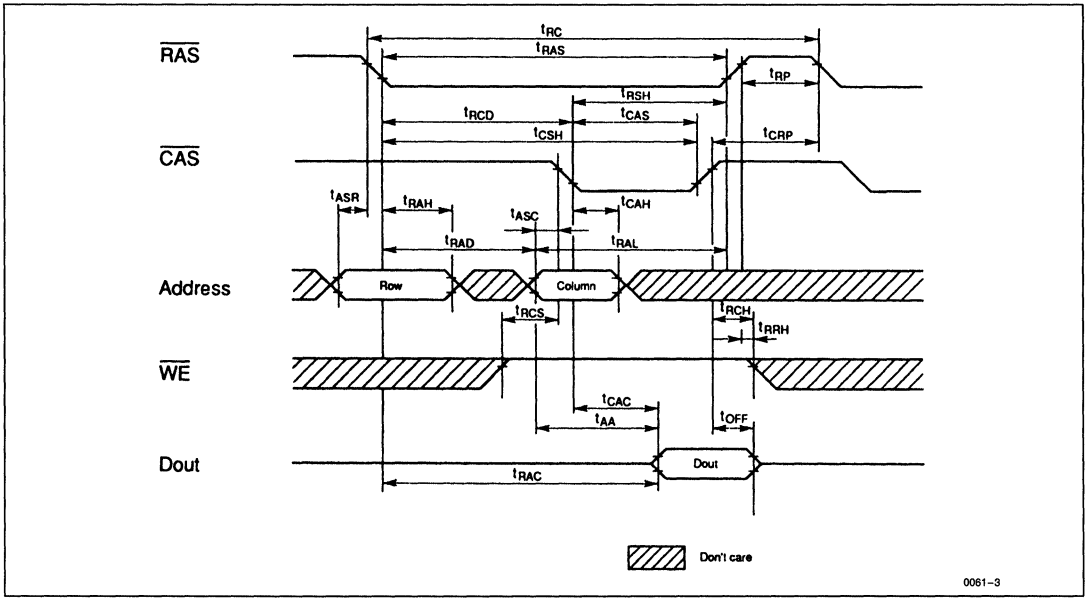
Parameter	Symbol	HM514100-7		Unit	Note
		Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	ns	

Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and t_{RAD} (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.

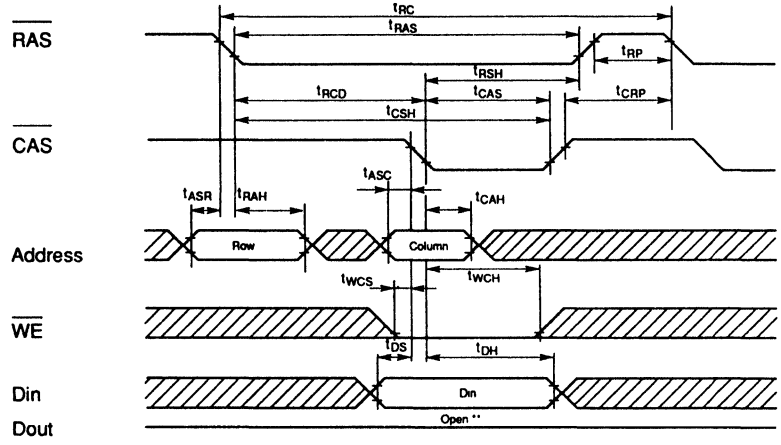
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits—RA10, CA10 and CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is D_{out} and data input pin is D_{in}. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
16. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORMS

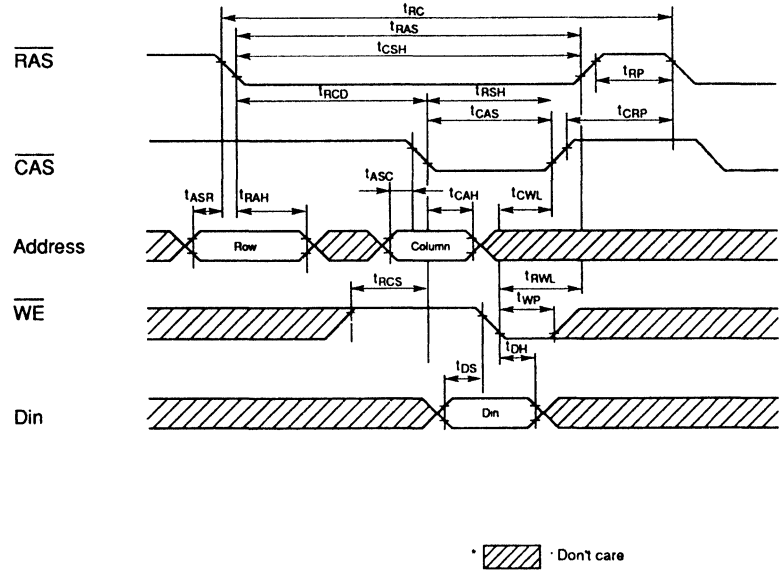
• Read Cycle



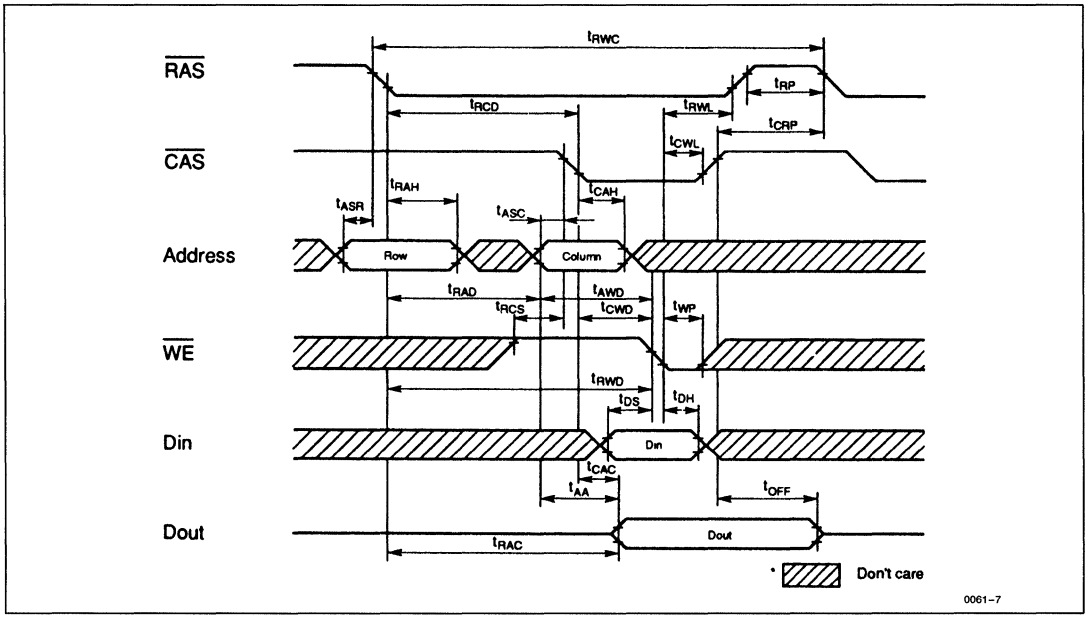
• **Early Write Cycle**



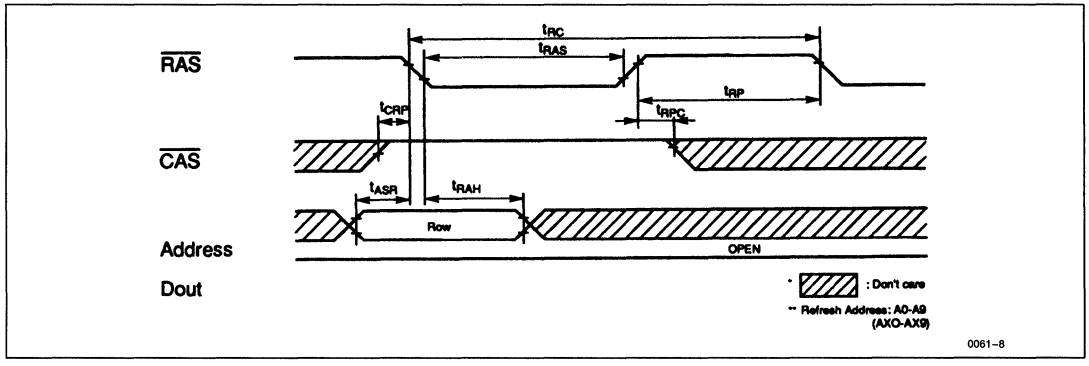
• **Delayed Write Cycle**



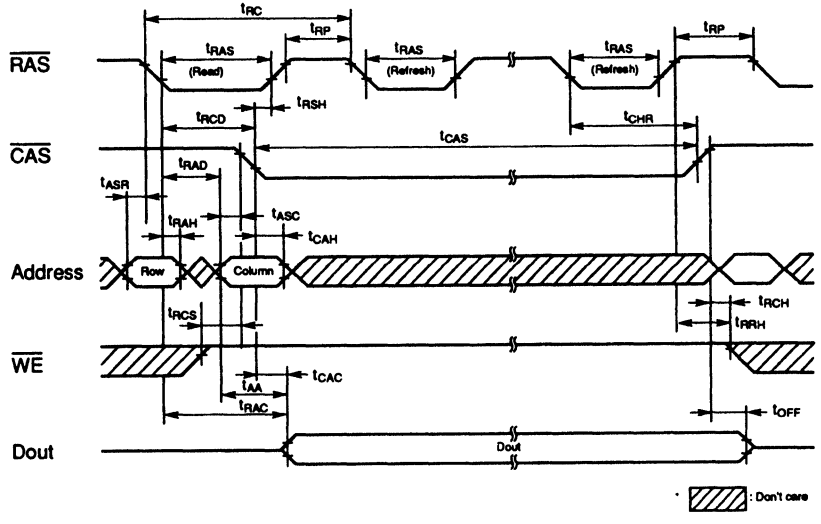
- **Read-Modify-Write Cycle**



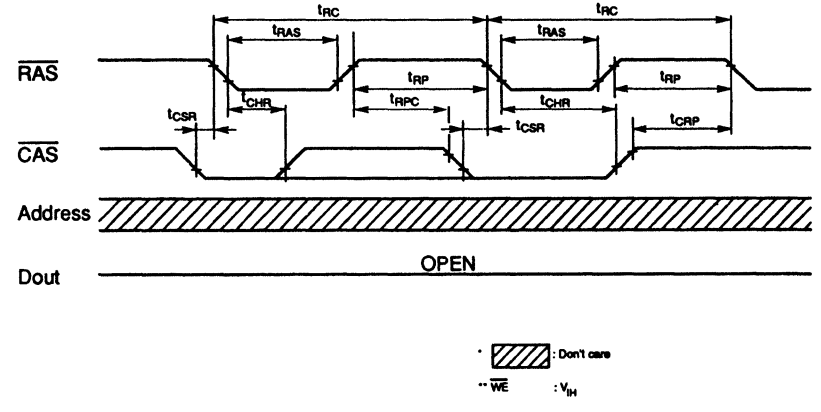
- **$\overline{\text{RAS}}$ Only Refresh Cycle**



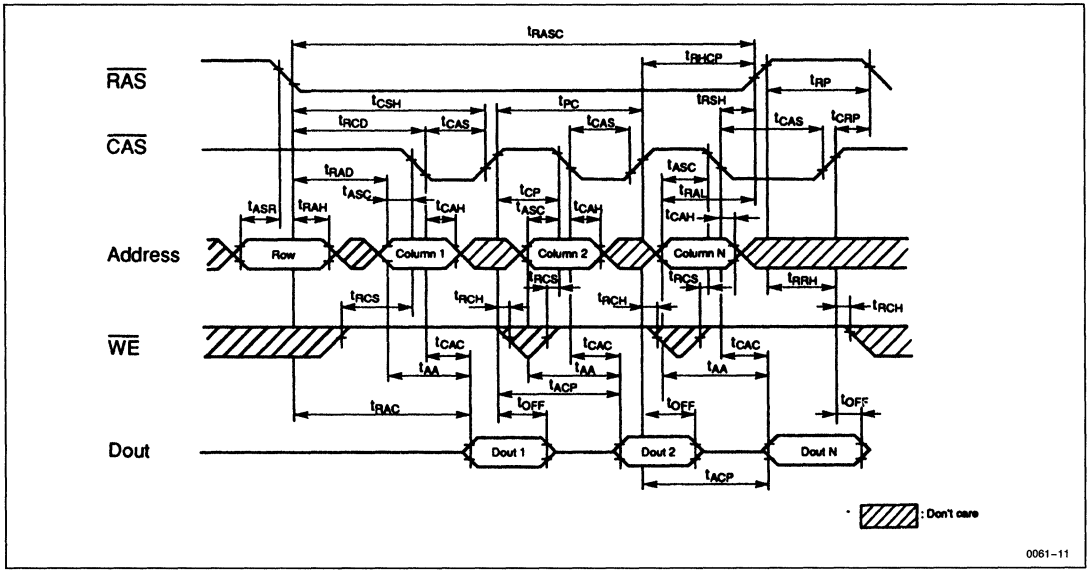
• **Hidden Refresh Cycle**



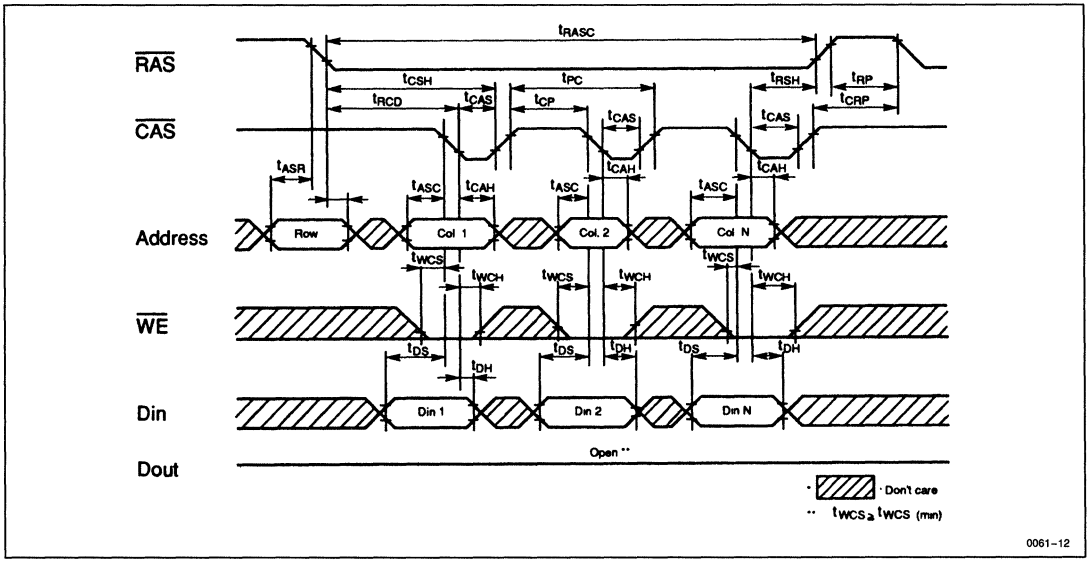
• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**



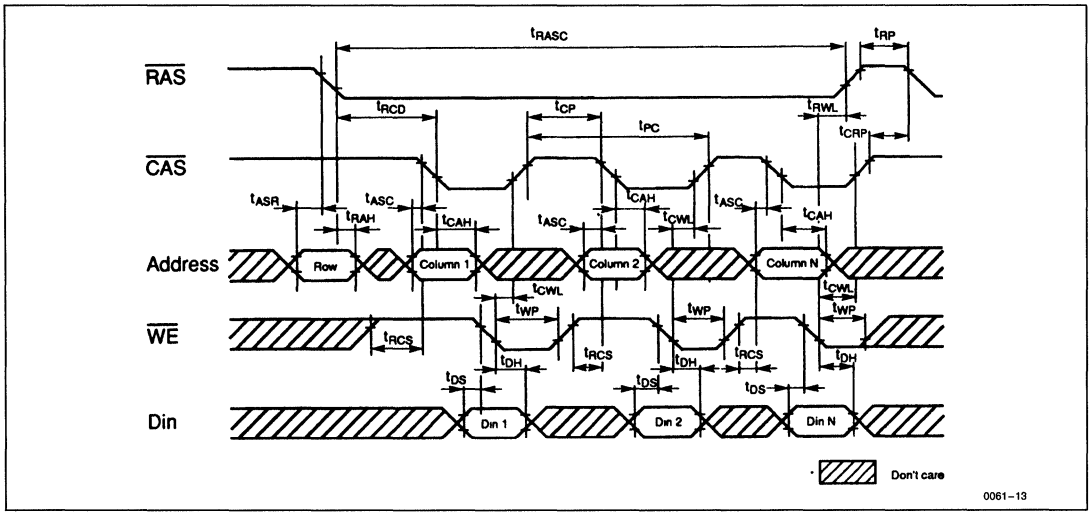
• Fast Page Mode Read Cycle



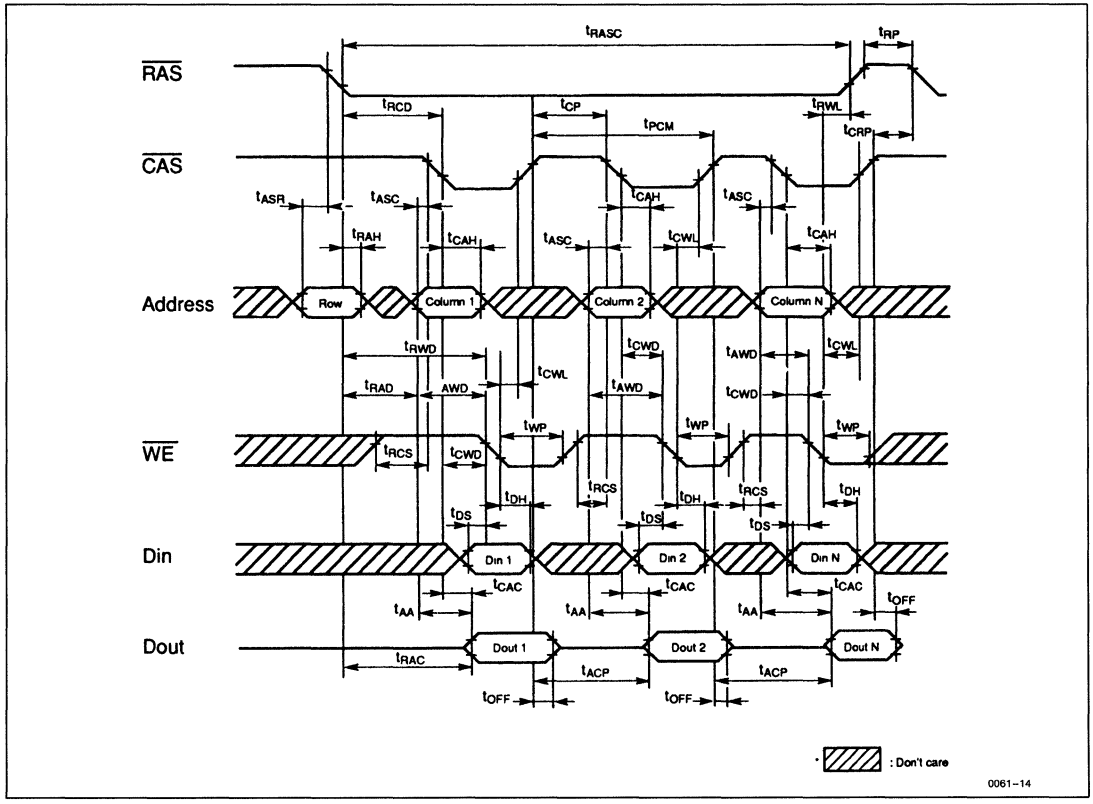
• Fast Page Mode Early Write Cycle



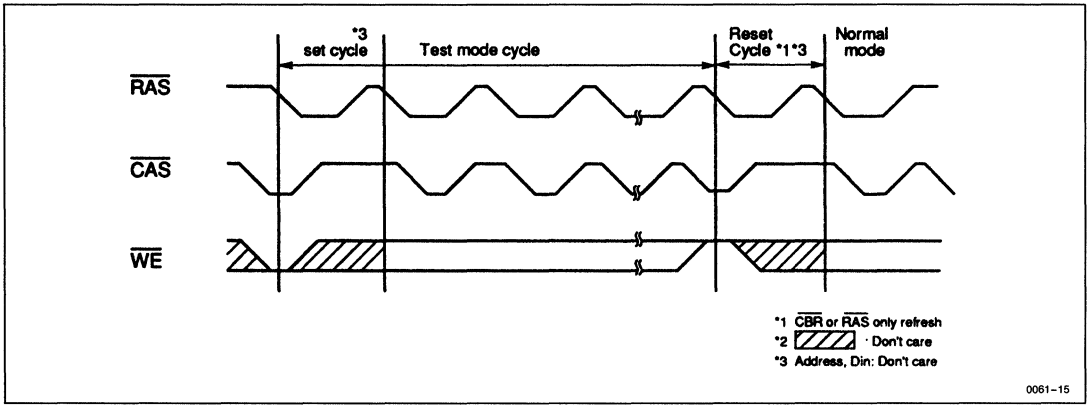
• **Fast Page Mode Delayed Write Cycle**



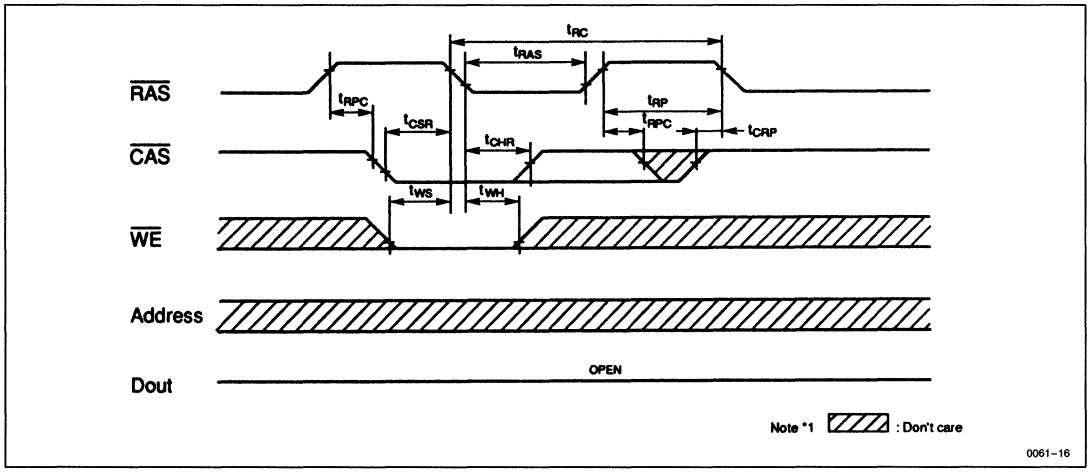
• **Fast Page Mode Read-Modify-Write Cycle**



■ TEST MODE CYCLE

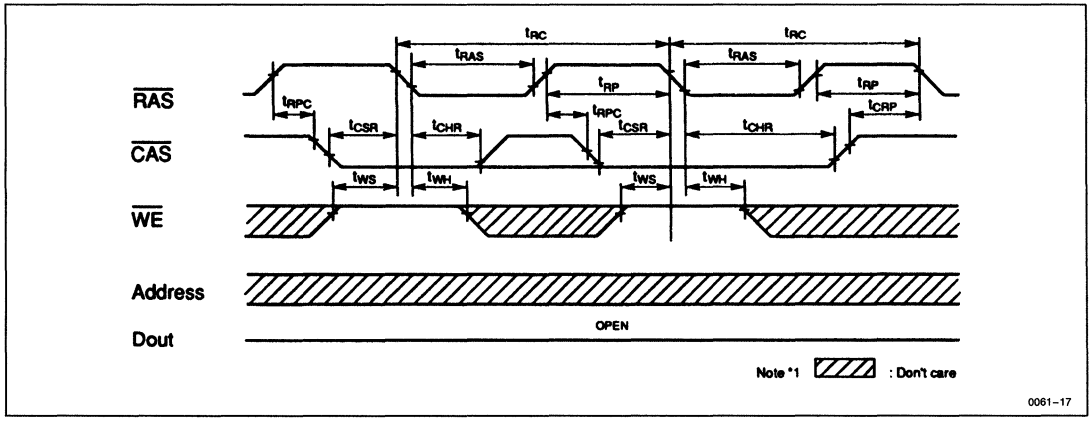


• Test Mode Set Cycle

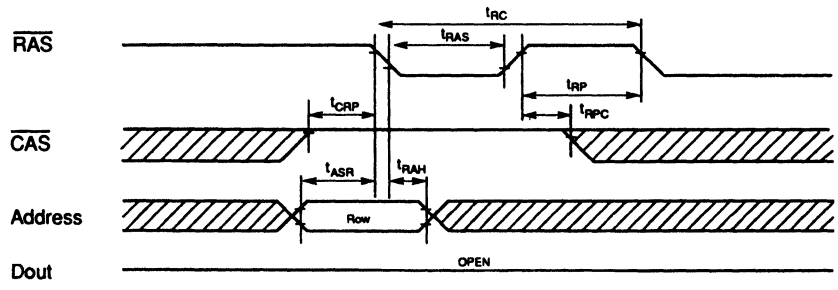


■ TEST MODE RESET CYCLE

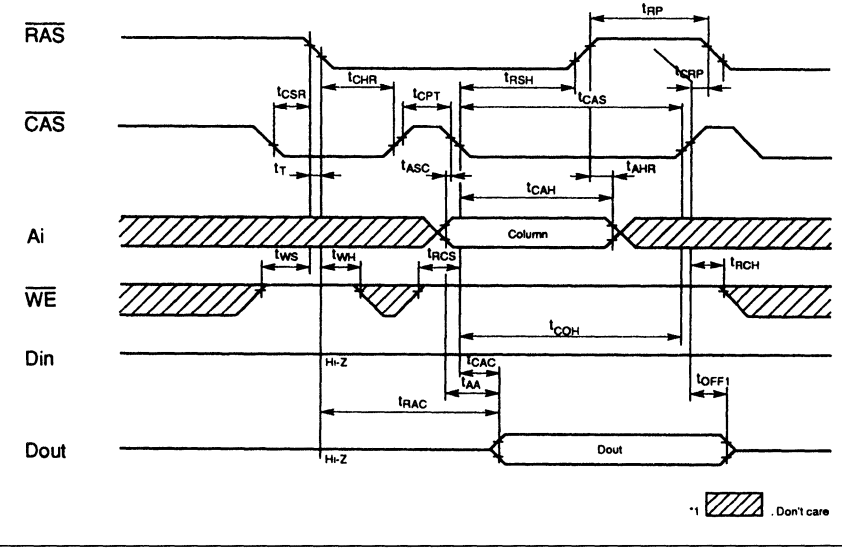
• CAS Before RAS Refresh Cycle



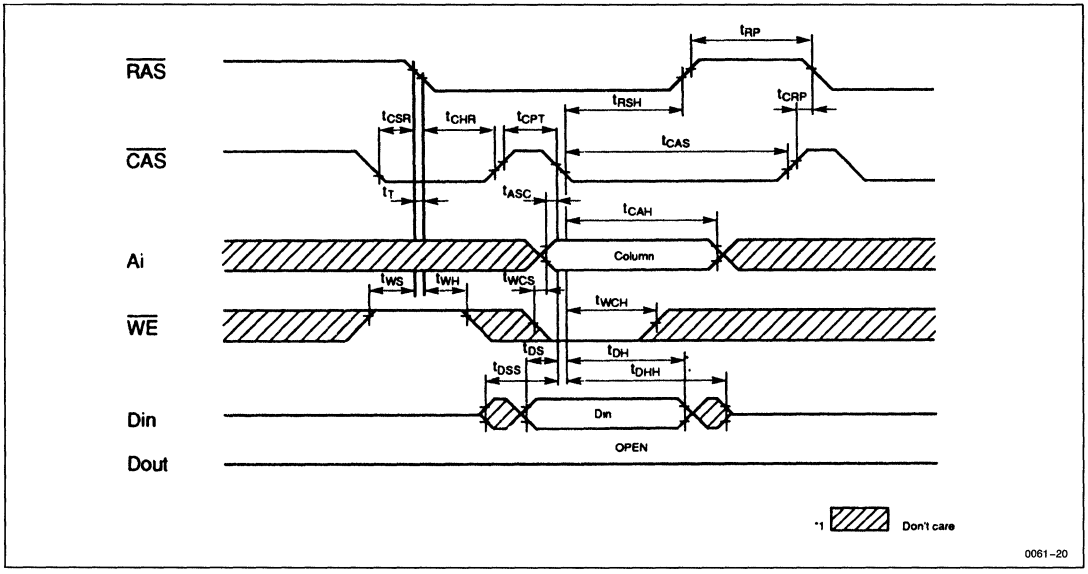
• $\overline{RAS}$ Only Refresh Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (READ)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (WRITE)



■ 4M DRAM LOW POWER VERSION

The specification on the low power version is the same as the standard 4 megabit DRAM with the exception of the following parameters.

Item	Conditions	Spec.
Type No.	4M x 1	HM514100LJP/LZP
	1M x 4	
Temperature	—	0–55°C
I_{CC2} (Standby CMOS Interface)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ ≥ V_{CC} − 0.2V Other Pin ≥ V_{CC} − 0.2V or ≤ 0.2V (Address and D_{in} is Stable) D_{out}: High-Z	200 μA Max
I_{CC10} (Standby with CBR Refresh)	t_{RC} = 125 μs, t_{RAS} ≤ 1 μs V_{IL1} ≥ V_{CC} − 0.2V, V_{IL} ≤ 0.2V $\overline{WE}$ and $\overline{OE}$ = V_{IH}, Address and D_{in} is Stable D_{out}: High-Z	300 μA Max
Refresh t_{REF}		128 ms

*only for 1M x 4.

HM514100L Series Low Power Version

4,194,304-Word x 1-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514100 is a CMOS dynamic RAM organized 4,194,304 word x 1-bit. HM514100 has realized high density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514100 offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514100 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time ..... 80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode ..... 495 mW/440 mW/385 mW (max)
  - Standby Mode ..... 11 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles ..... (128 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Test Function
- Battery Back Up Operation

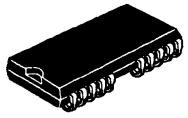
■ ORDERING INFORMATION

Part No.	Access Time	Package
HM514100LJP-8	80 ns	350 mil 20-pin
HM514100LJP-10	100 ns	Plastic SOJ
HM514100LJP-12	120 ns	(CP-20DA)
HM514100LZP-8	80 ns	400 mil 20-pin
HM514100LZP-10	100 ns	Plastic ZIP
HM514100LZP-12	120 ns	(ZP-20)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{10}	Address Input
A_0–A_9	Refresh Address Input
D_{in}	Data-in
D_{out}	Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

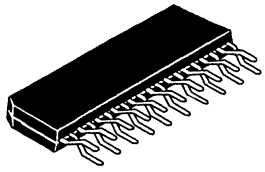
HM514100LJP Series



3DCP20DA

(CP-20DA)

HM514100LZP Series

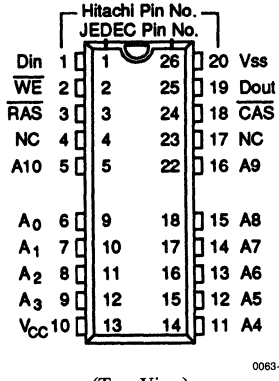


3DZP20

(ZP-20)

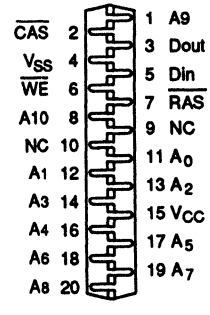
■ PIN OUT

HM514100LJP Series



(Top View)

HM514100LZP Series



(Bottom View)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	− 2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	70	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	200	—	200	—	200	μA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ ≥ V_{CC} − 0.2V or ≤ 0.2V, Address and D_{in}: Stable, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	90	—	80	—	70	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	90	—	80	—	70	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	90	—	80	—	70	mA	t_{PC} = Min	1, 3
Battery Back Up Operating Current (Standby with CBR Refresh)	I_{CC10}	—	300	—	300	—	300	μA	t_{RC} = 125 μs, t_{RAS} ≤ 1 μs V_{CC} − 0.2V ≤ V_{IH} ≤ 6.5V, 0V ≤ V_{IL} ≤ 0.2V $\overline{WE}$ = V_{IH}, Address and D_{in}: Stable, D_{out} = High-Z	
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{CAS}$ = V_{IL}.
3. Address can be changed once or less $\overline{CAS}$ = V_{IH}.

• Capacitance (T_A = 25°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address, Data-in)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-out)	C_O	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)[1, 12, 15]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	150	—	180	—	210	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	128	—	128	—	128	ns	

Read Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3, 16
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4, 14
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5, 14, 16
Read Command to Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	ns	6

Write Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	20	—	25	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	180	—	210	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	100	—	120	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	25	—	25	—	30	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40	—	45	—	55	—	ns	10

Refresh Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	14, 16
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	85	—	85	—	100	—	ns	

Test Mode Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	20	—	20	—	20	—	ns	

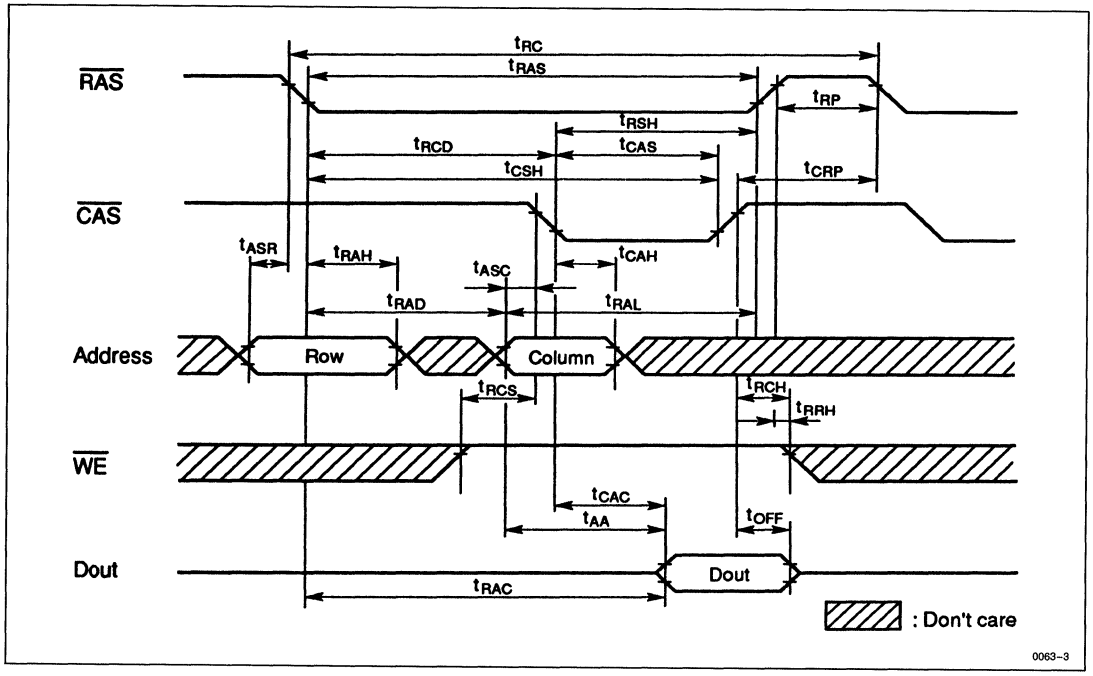
Counter Test Cycle

Parameter	Symbol	HM514100-8		HM514100-10		HM514100-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	50	—	60	—	ns	

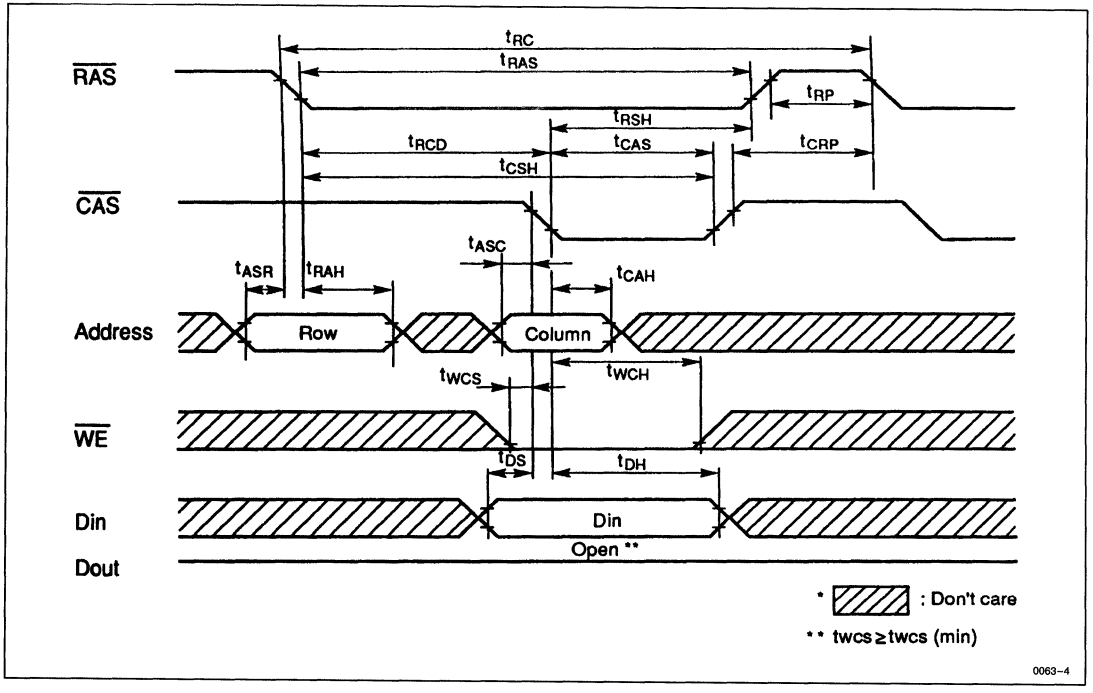
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits—RA_{10}, CA_{10} and CA_0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is D_{out} and data input pin is D_{in}. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
16. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORMS

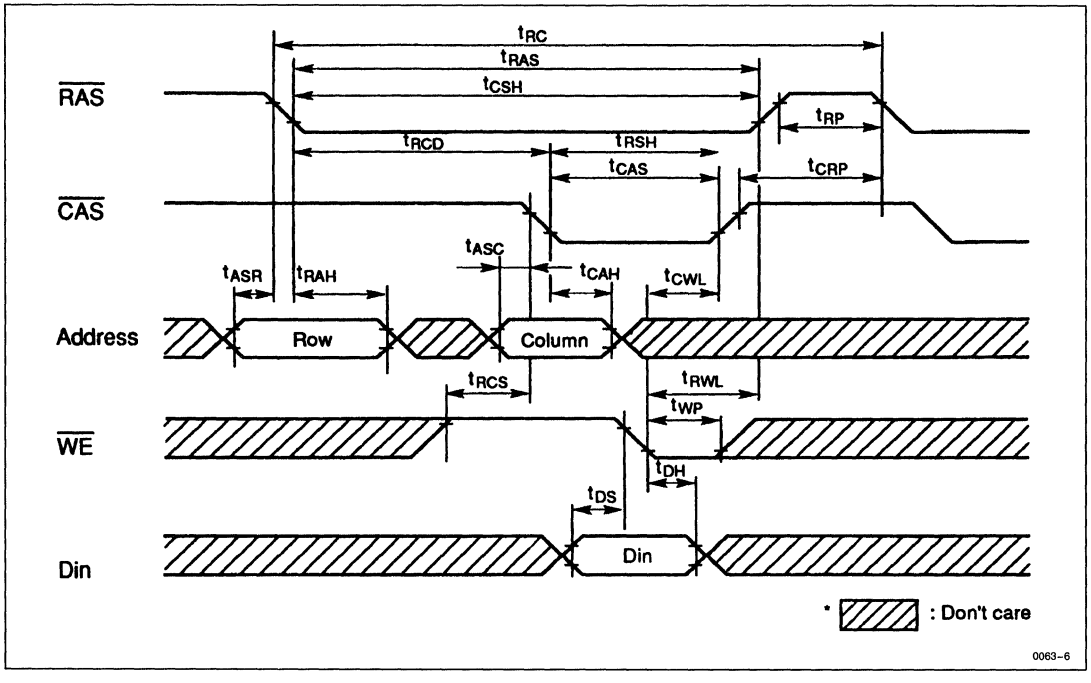
• Read Cycle (1)



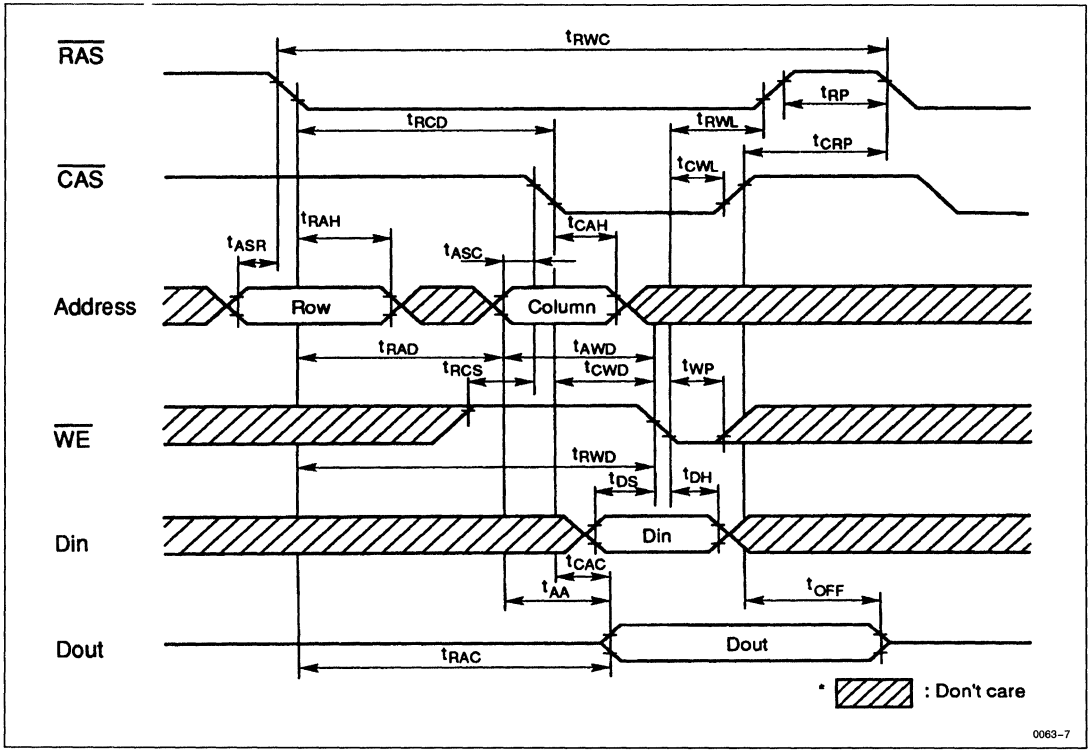
• Early Write Cycle (2)



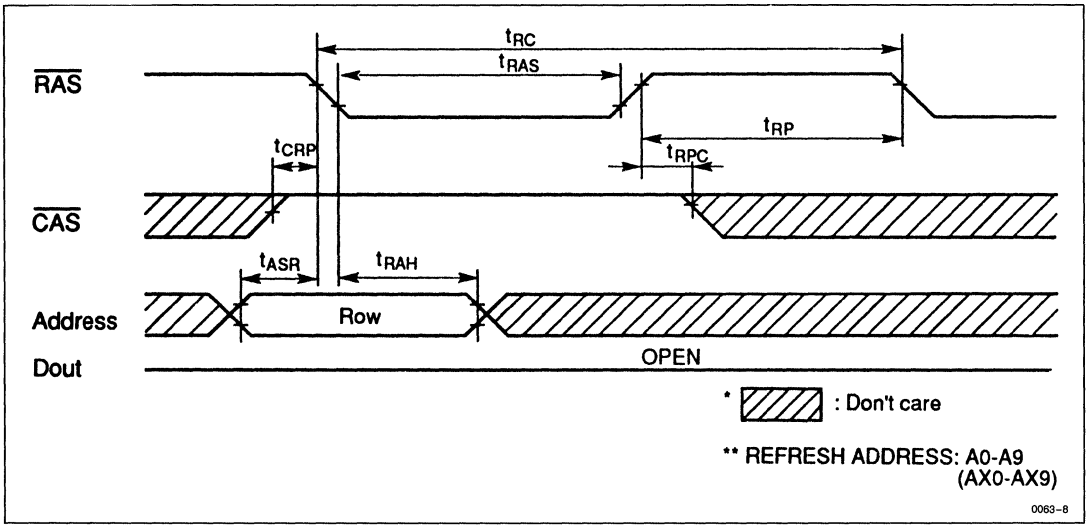
• **Delayed Write Cycle (3)**



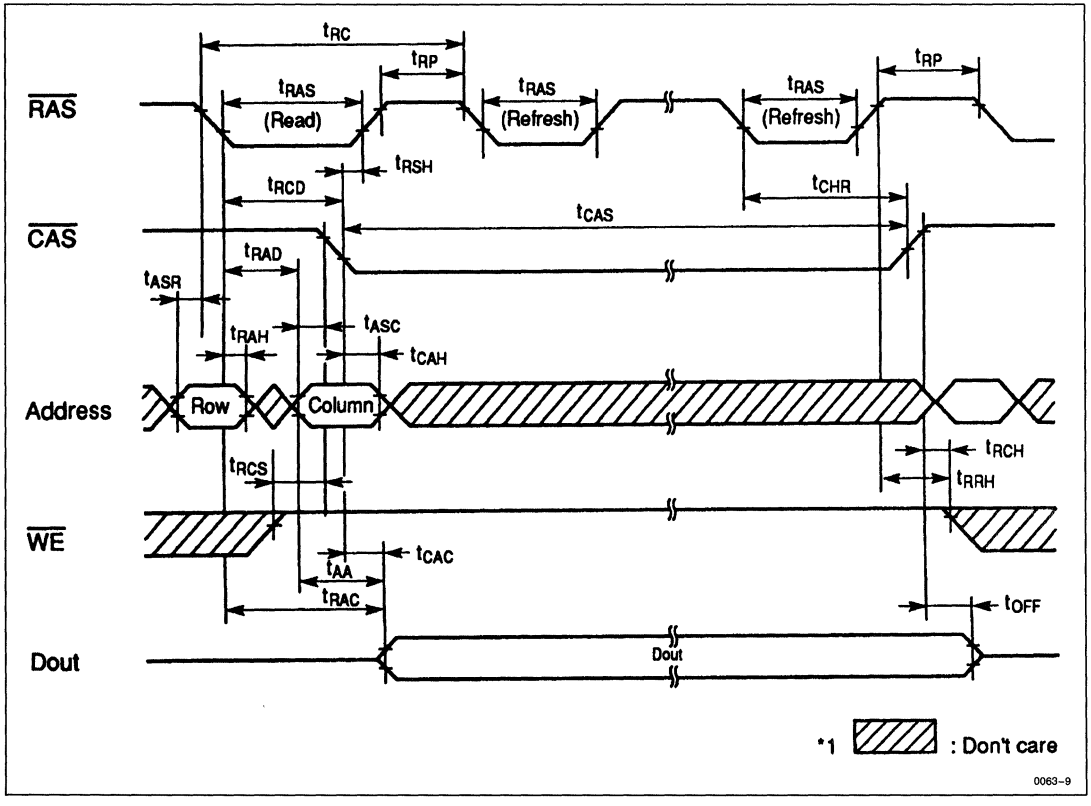
• **Read-Modify-Write Cycle (4)**



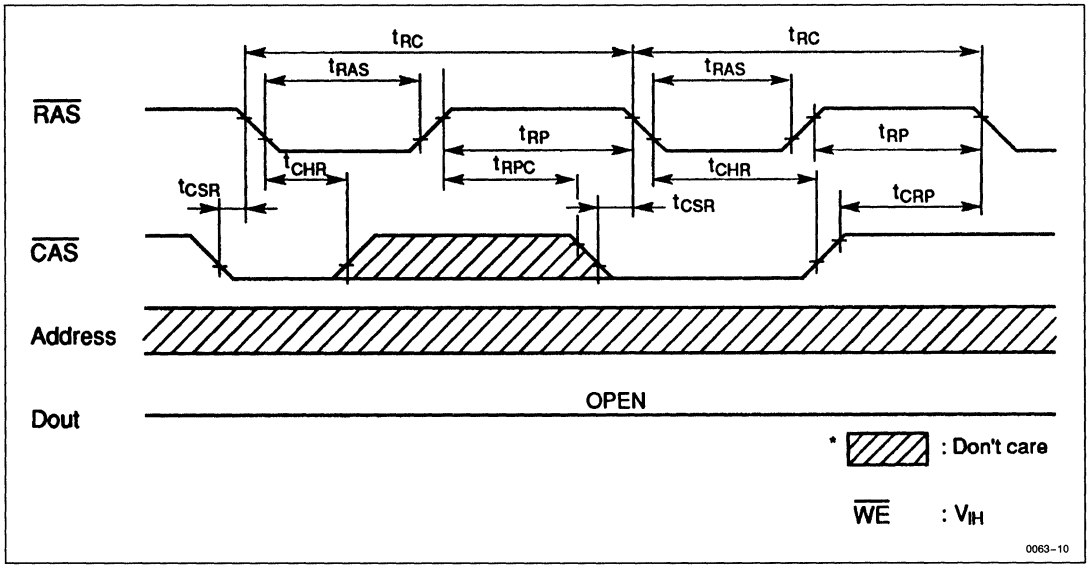
• $\overline{RAS}$ Only Refresh Cycle (5)



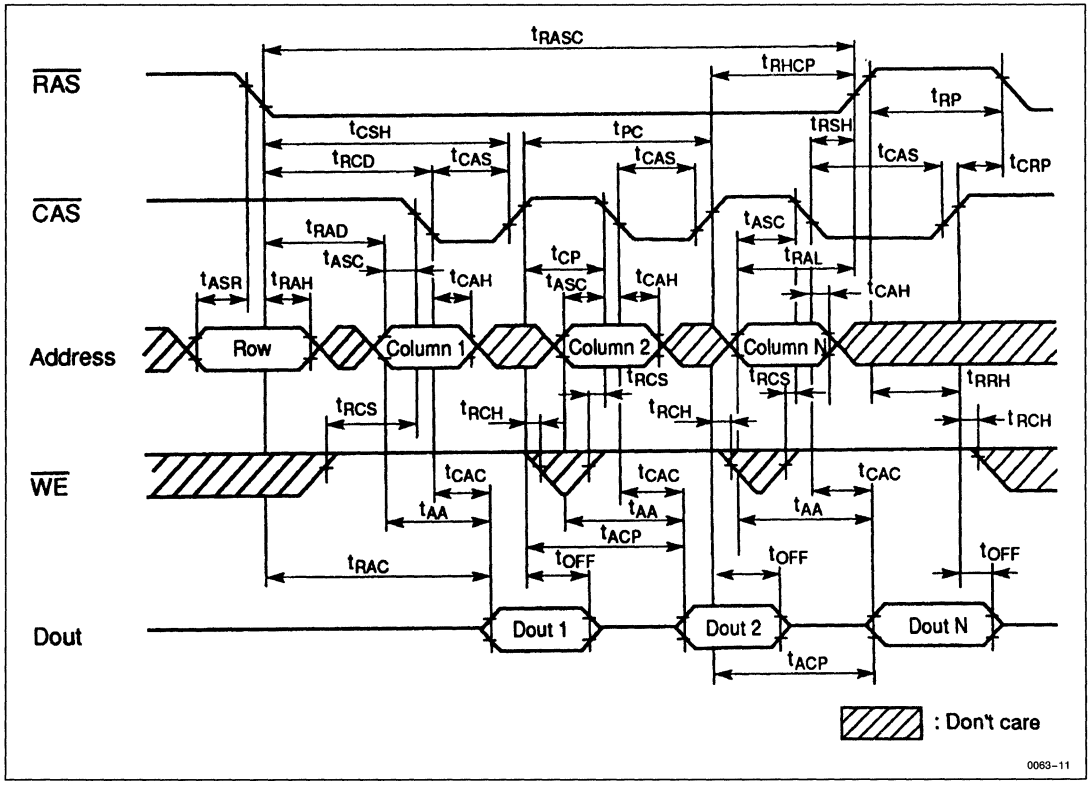
• Hidden Refresh Cycle (6)



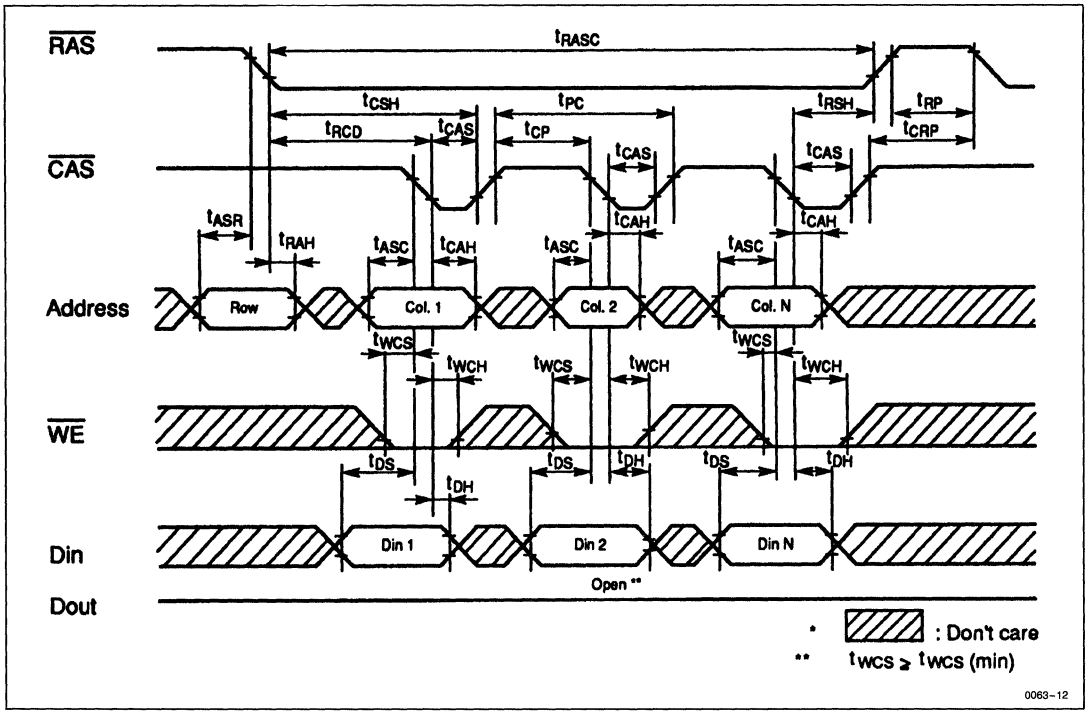
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle (7)



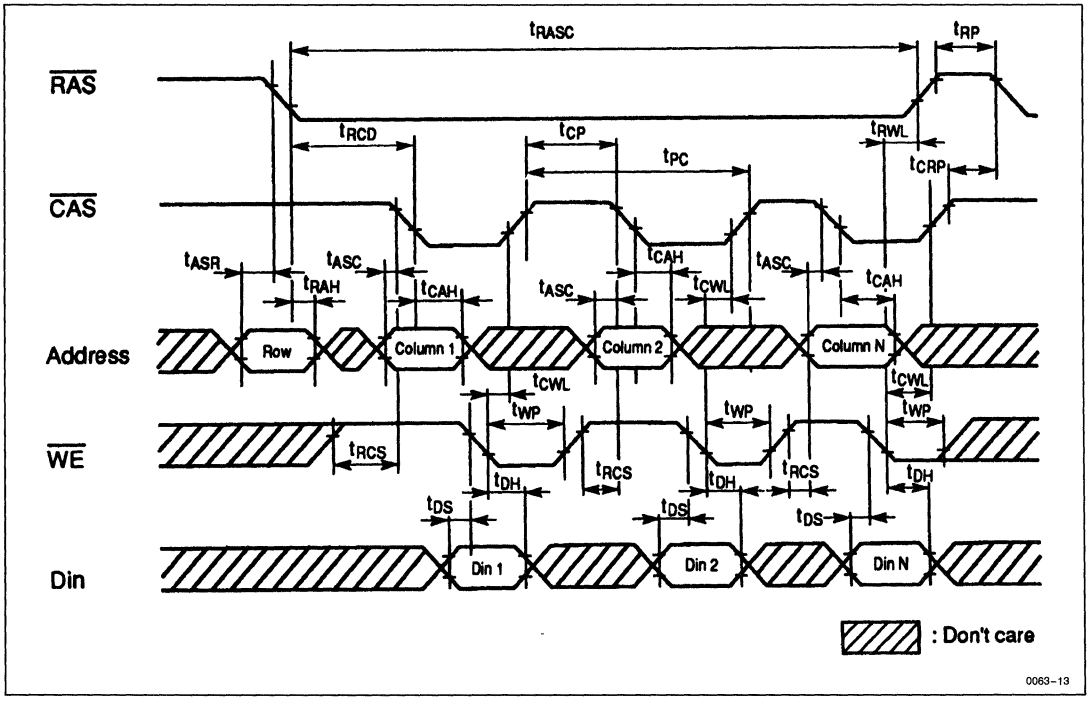
• Fast Page Mode Read Cycle (8)



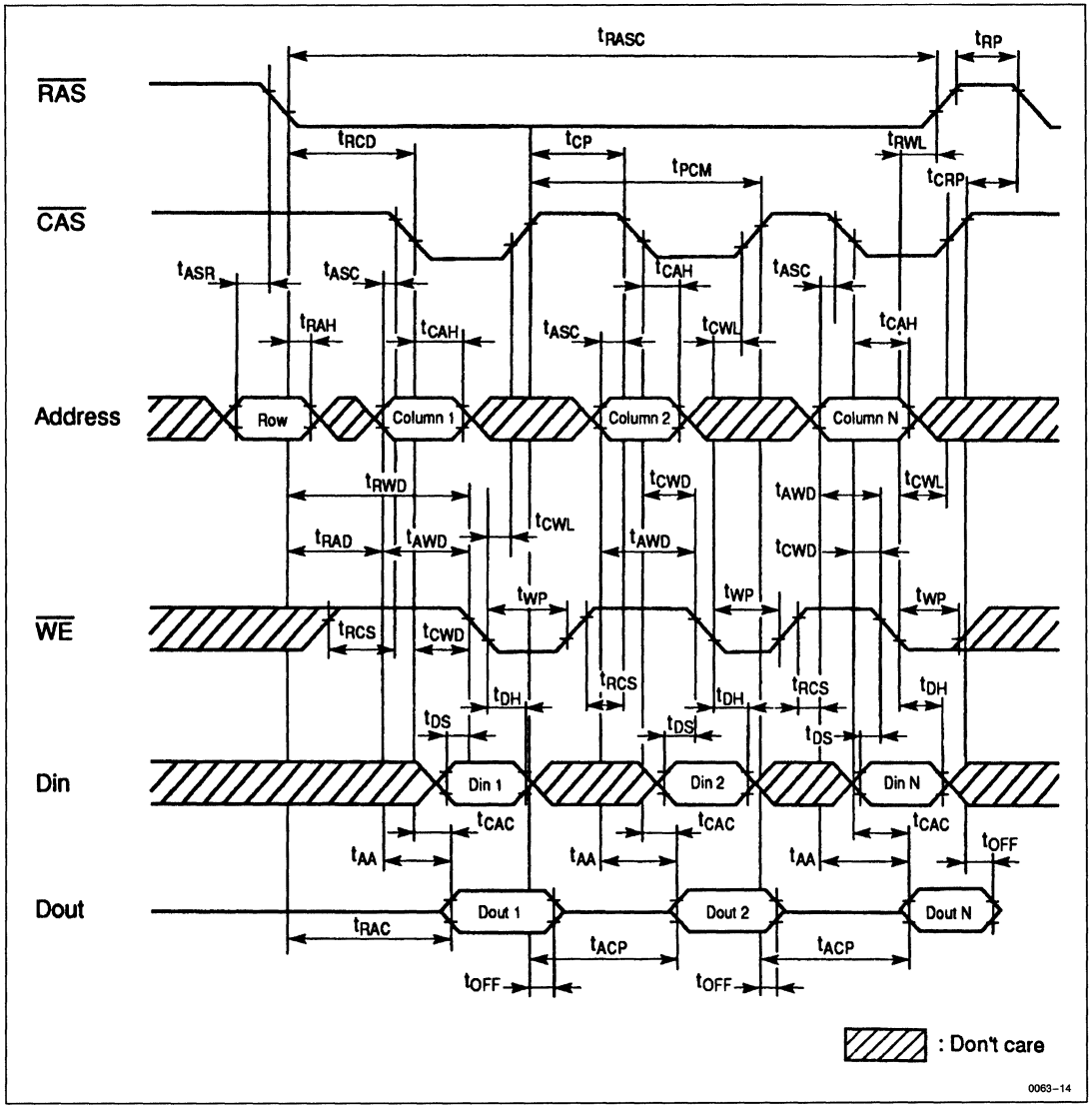
• **Fast Page Mode Early Write Cycle (9)**



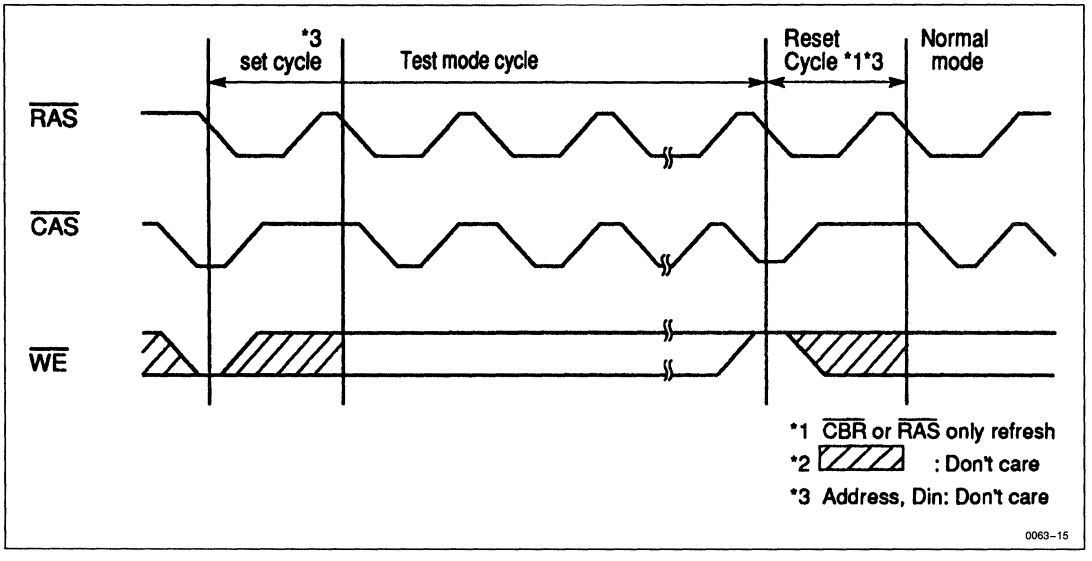
• **Fast Page Delayed Write Cycle (10)**



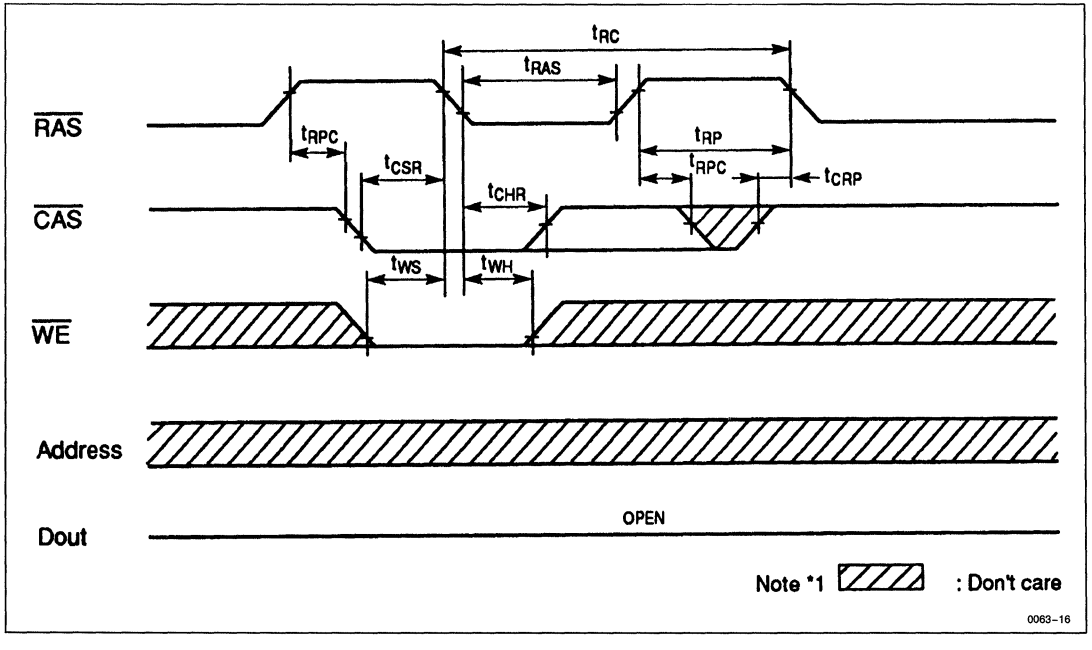
• **Fast Page Mode Read-Modify-Write Cycle (11)**



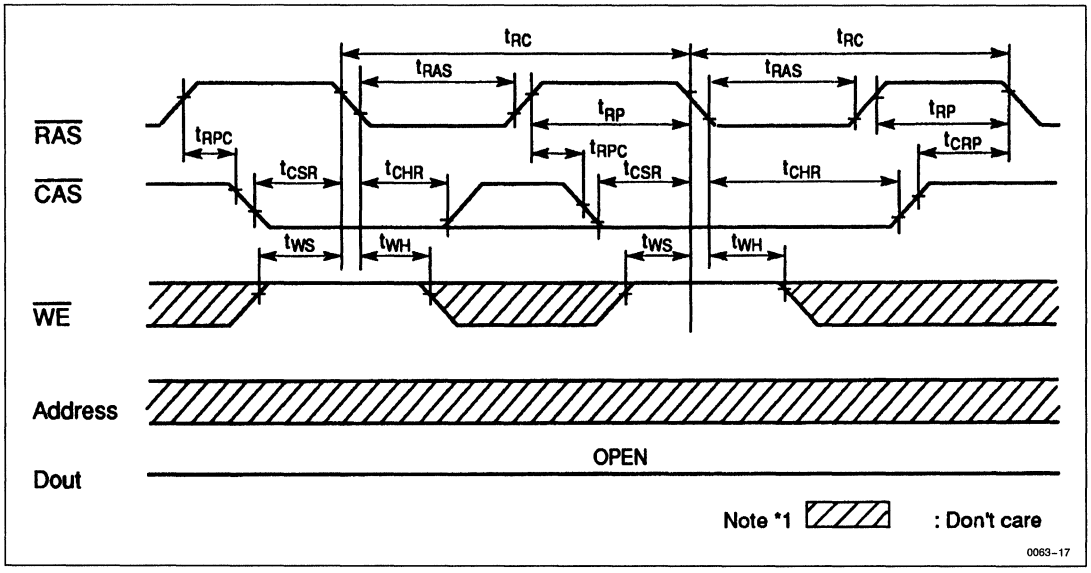
• Test Mode Cycle



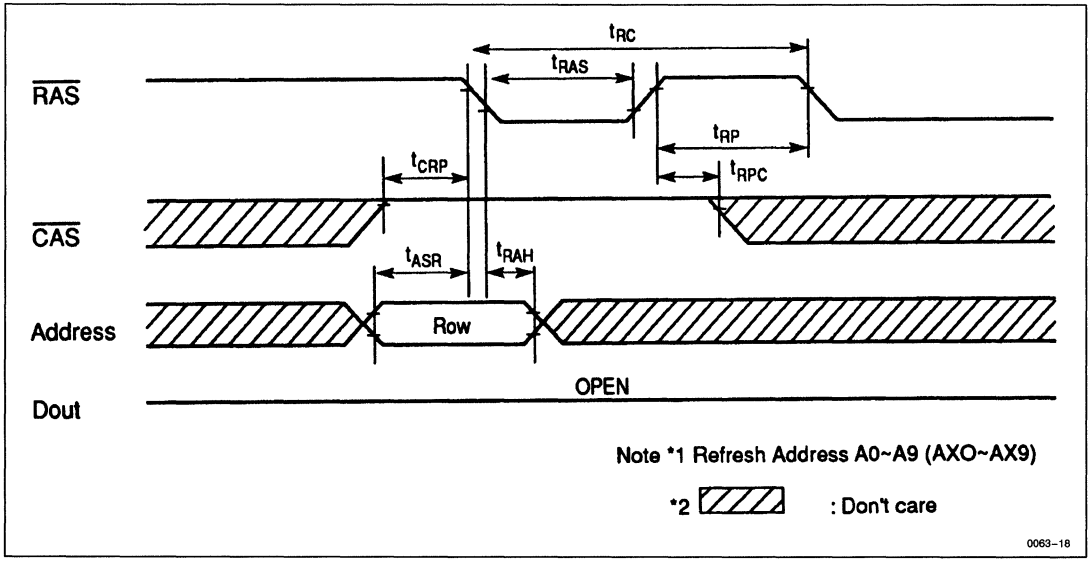
• Test Mode Set Cycle (1)



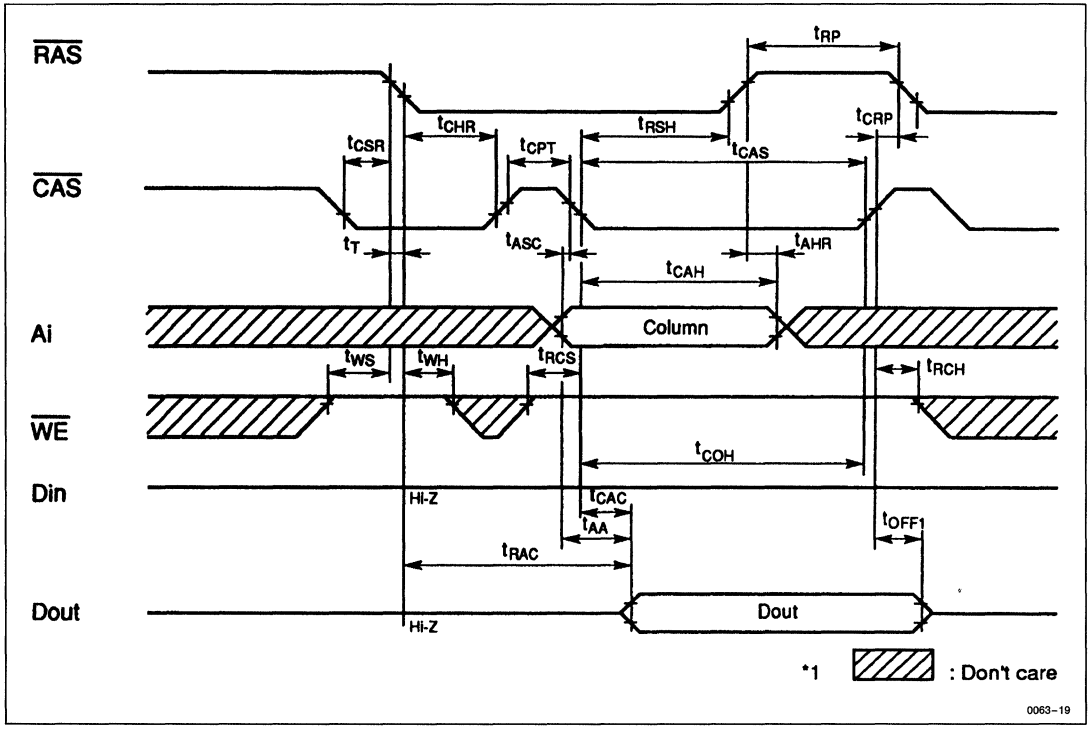
• **Test Mode Reset Cycle (2)**



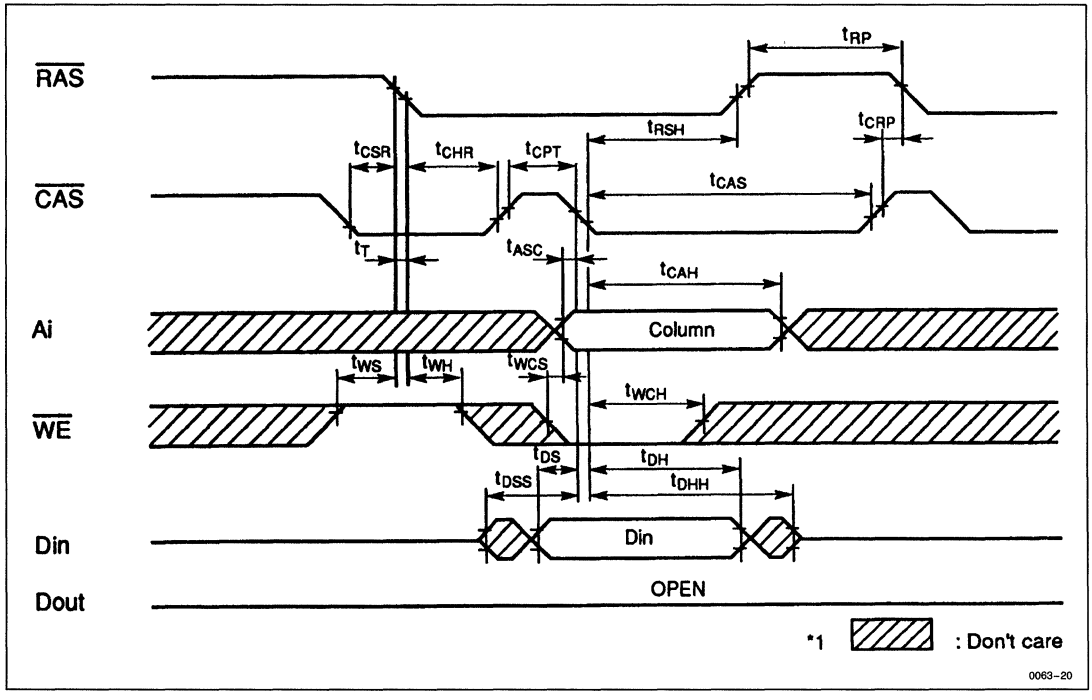
• **$\overline{RAS}$ Only Refresh Cycle**



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (READ)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (WRITE)



HM514101 Series

4,194,304-Word x 1-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514101 is a CMOS dynamic RAM organized 4,194,304 word x 1-bit. HM514101 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514101 offers Nibble Mode as a high speed access mode.

Multiplexed address input permits the HM514101 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time ..... 80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode ..... 495 mW/440 mW/385 mW (max)
  - Standby Mode ..... 11 mW (max)
- Nibble Mode Capability
- 1,024 Refresh Cycles ..... (16 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Test Function

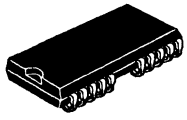
■ ORDERING INFORMATION

Part No.	Access Time	Package
HM514101JP-8	80 ns	350 mil 20-pin
HM514101JP-10	100 ns	Plastic SOJ
HM514101JP-12	120 ns	(CP-20DA)
HM514101ZP-8	80 ns	400 mil 20-pin
HM514101ZP-10	100 ns	Plastic ZIP
HM514101ZP-12	120 ns	(ZP-20)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{10}	Address Input
A_0–A_9	Refresh Address Input
D_{in}	Data-in
D_{out}	Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

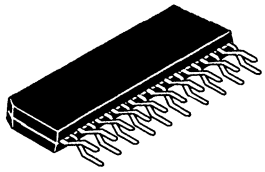
HM514101JP Series



3DCP20DA

(CP-20DA)

HM514101ZP Series

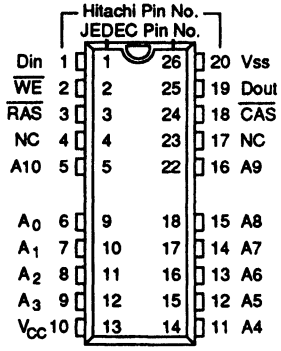


3DZP20

(ZP-20)

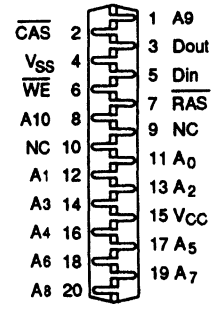
■ PIN OUT

HM514101JP Series



(Top View)

HM514101ZP Series



(Bottom View)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	− 2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM514101-8		HM514101-10		HM514101-12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	70	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	1	—	1	—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	90	—	80	—	70	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	90	—	80	—	70	mA	t_{RC} = Min	
Nibble Mode Current	I_{CC8}	—	90	—	80	—	70	mA	t_{NC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• Capacitance (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address, Data-in)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-out)	C_O	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 12, 13]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514101-8		HM514101-10		HM514101-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	150	—	180	—	210	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514101-8		HM514101-10		HM514101-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3, 14
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5, 14
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	ns	6

Write Cycle

Parameter	Symbol	HM514101-8		HM514101-10		HM514101-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	20	—	25	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514101-8		HM514101-10		HM514101-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	180	—	210	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	100	—	120	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	25	—	25	—	30	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40	—	45	—	55	—	ns	10

Refresh Cycle

Parameter	Symbol	HM514101-8		HM514101-10		HM514101-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

Nibble Mode Cycle

Parameter	Symbol	HM514101-8		HM514101-10		HM514101-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Nibble Mode Access Time	t_{NAC}	—	25	—	25	—	30	ns	
Nibble Mode Cycle Time	t_{NC}	45	—	45	—	55	—	ns	
Nibble Mode $\overline{CAS}$ Precharge Time	t_{NCP}	10	—	10	—	15	—	ns	
Nibble Mode $\overline{CAS}$ Pulse Width	t_{NCA}	25	—	25	—	30	—	ns	
Nibble Mode $\overline{RAS}$ Hold Time	t_{NRSH}	25	—	25	—	30	—	ns	

Nibble Mode Read-Modify-Write Cycle

Parameter	Symbol	HM514101-8		HM514101-10		HM514101-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Nibble Mode Read-Modify-Write Cycle Time	t_{NRWC}	75	—	75	—	90	—	ns	
Nibble Mode Write Command to $\overline{CAS}$ Lead Time	t_{NCWL}	25	—	25	—	30	—	ns	
Nibble Mode $\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{NCWD}	25	—	25	—	30	—	ns	

Test Mode Cycle

Parameter	Symbol	HM514101-8		HM514101-10		HM514101-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	20	—	20	—	20	—	ns	

Counter Test Cycle

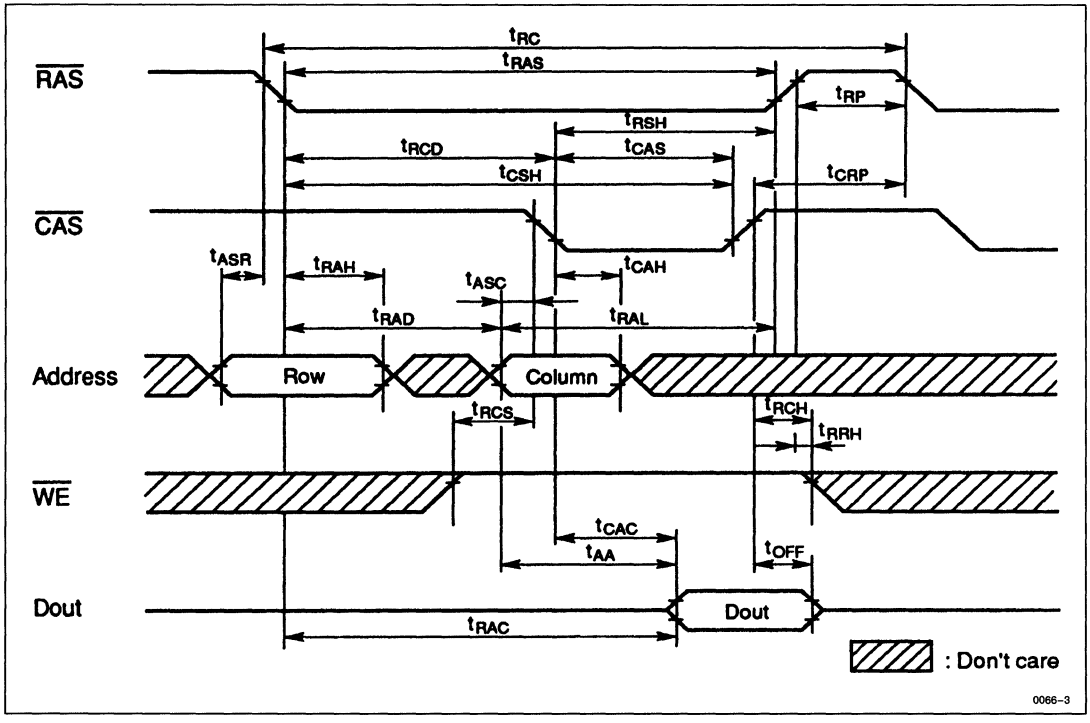
Parameter	Symbol	HM514101-8		HM514101-10		HM514101-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	50	—	60	—	ns	

Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RCD} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

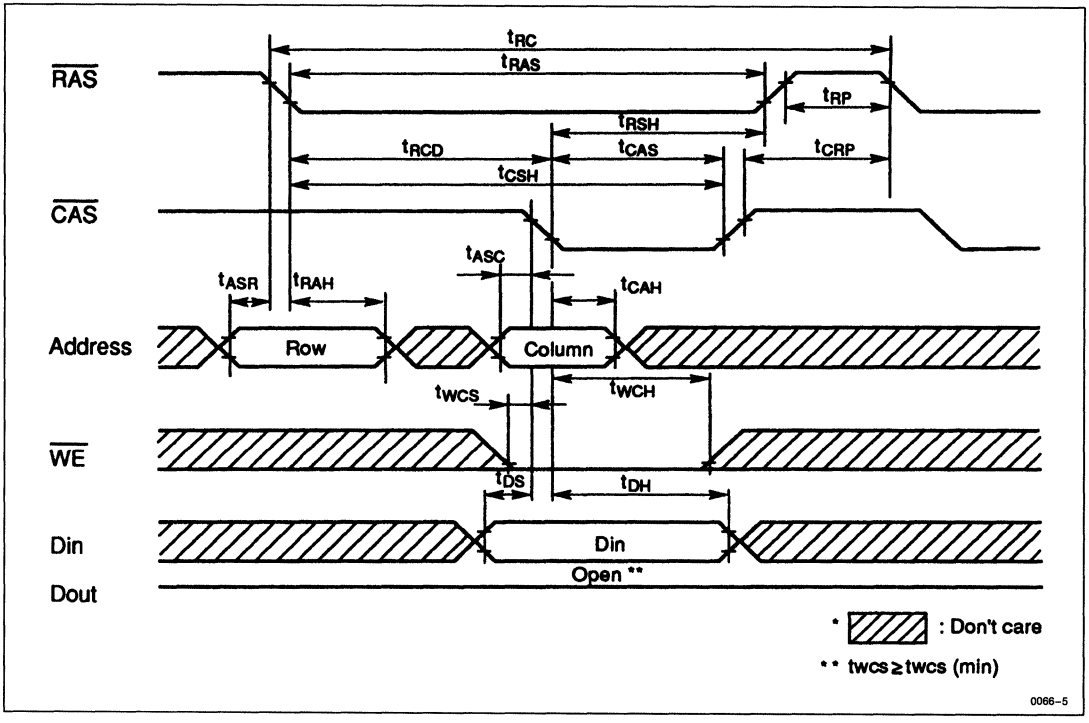
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
13. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits—RA10, CA10 and CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is D_{out} and data input pin is D_{in}. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
14. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{NAC} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORMS

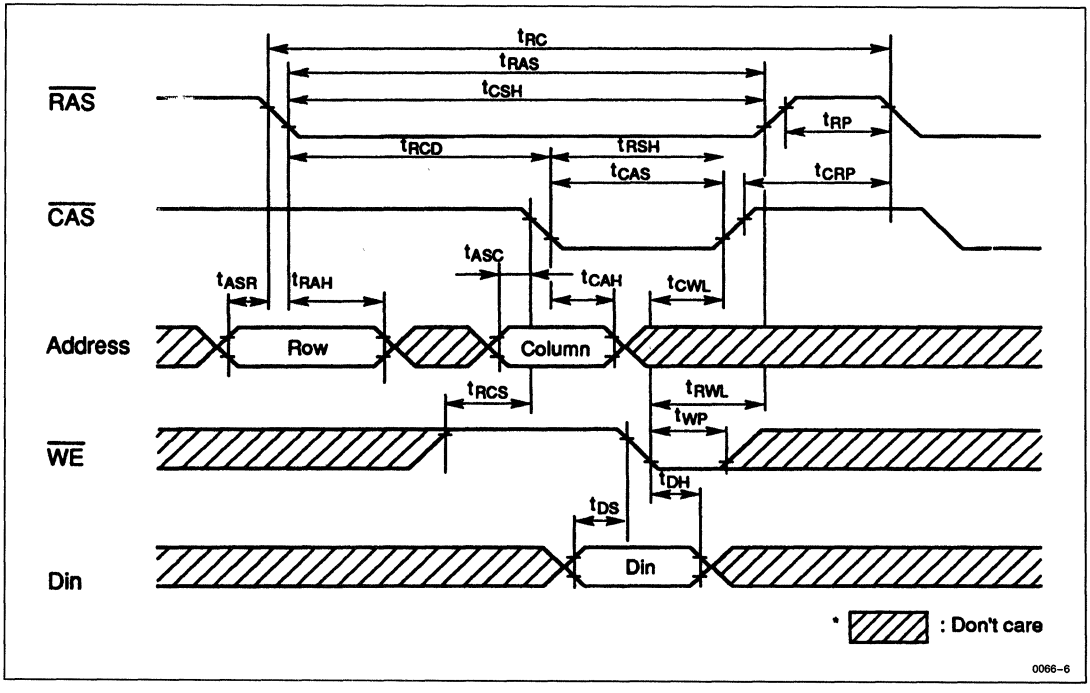
• Read Cycle (1)



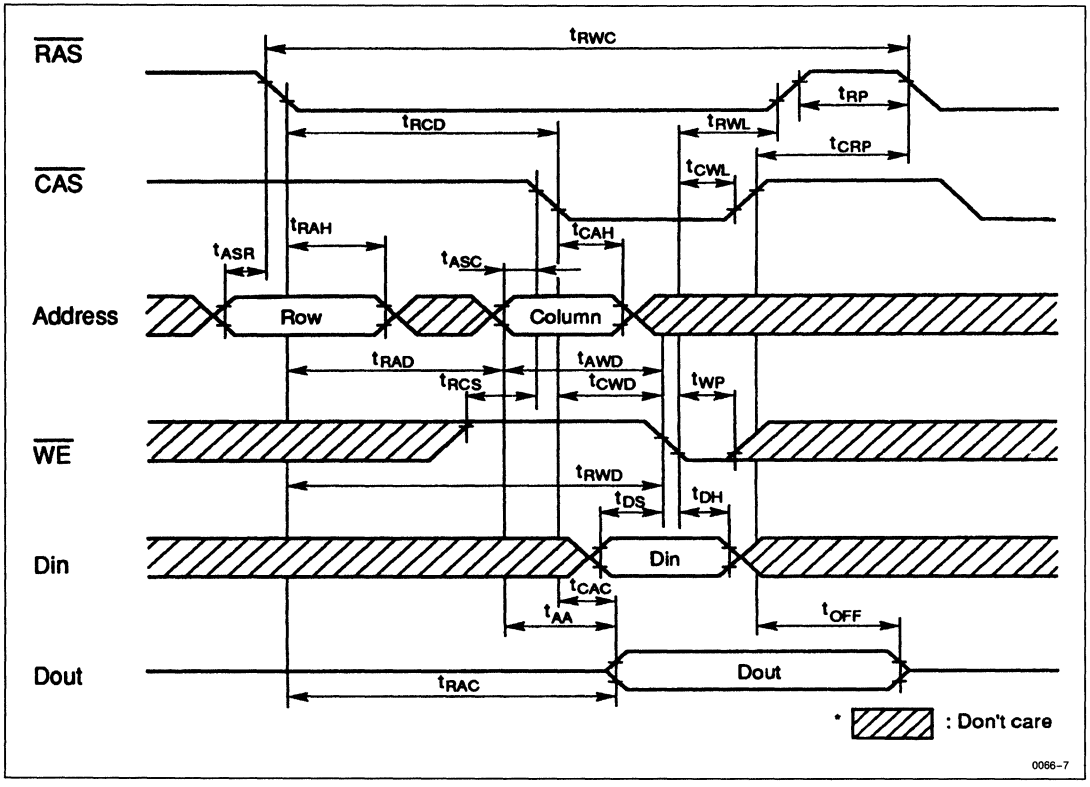
• Early Write Cycle (2)



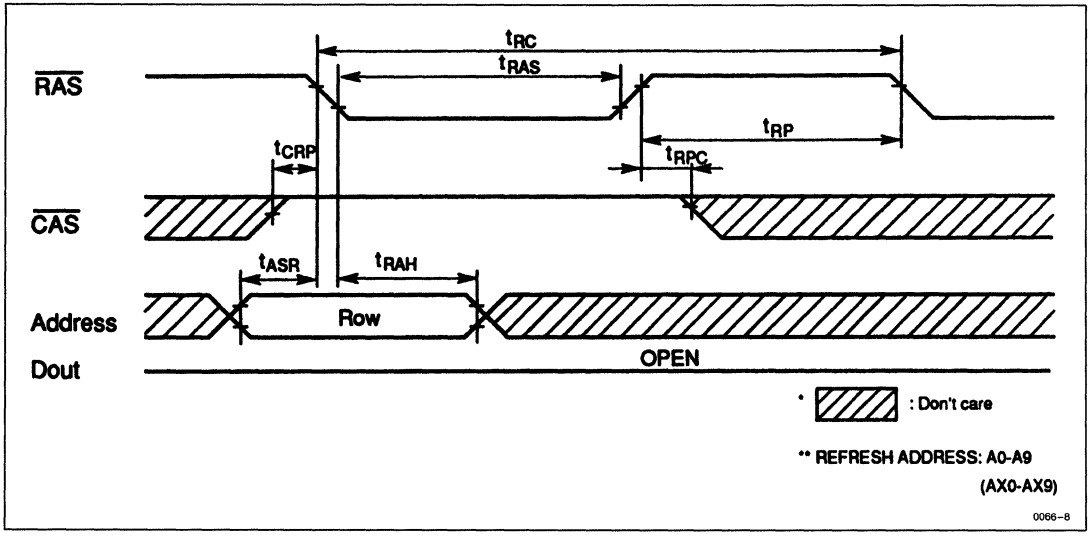
• Delayed Write Cycle (3)



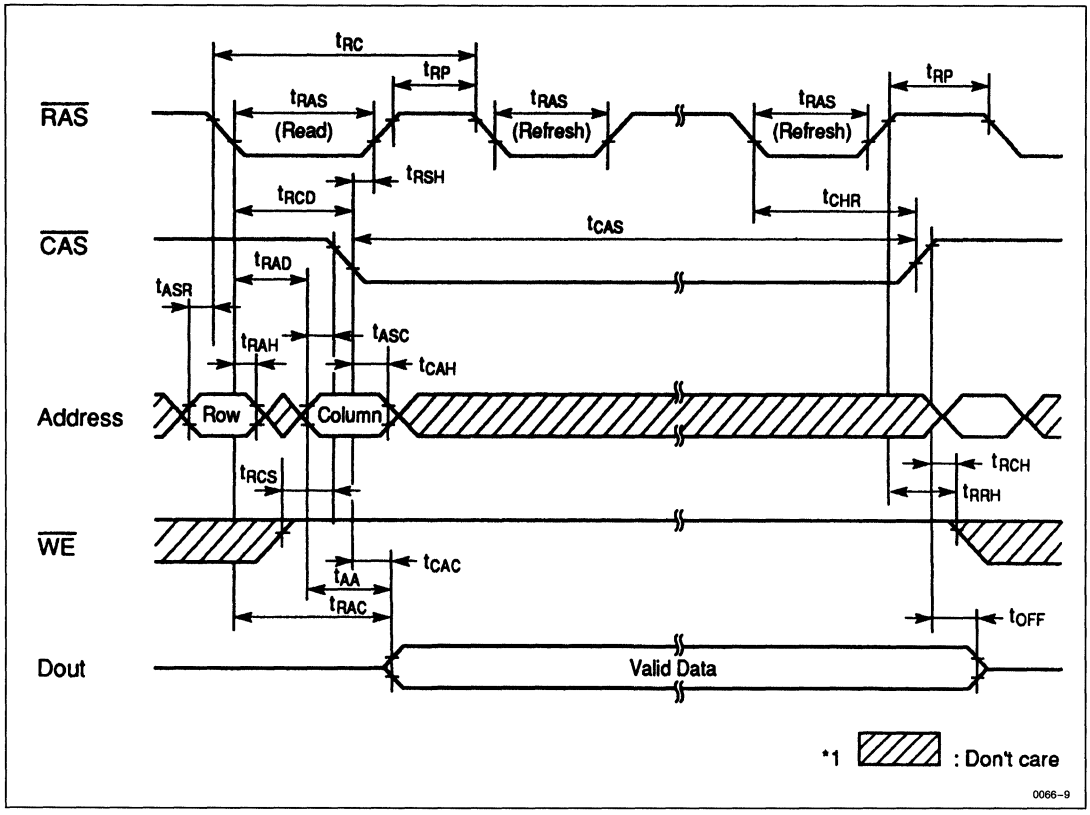
• **Read-Modify-Write Cycle (4)**



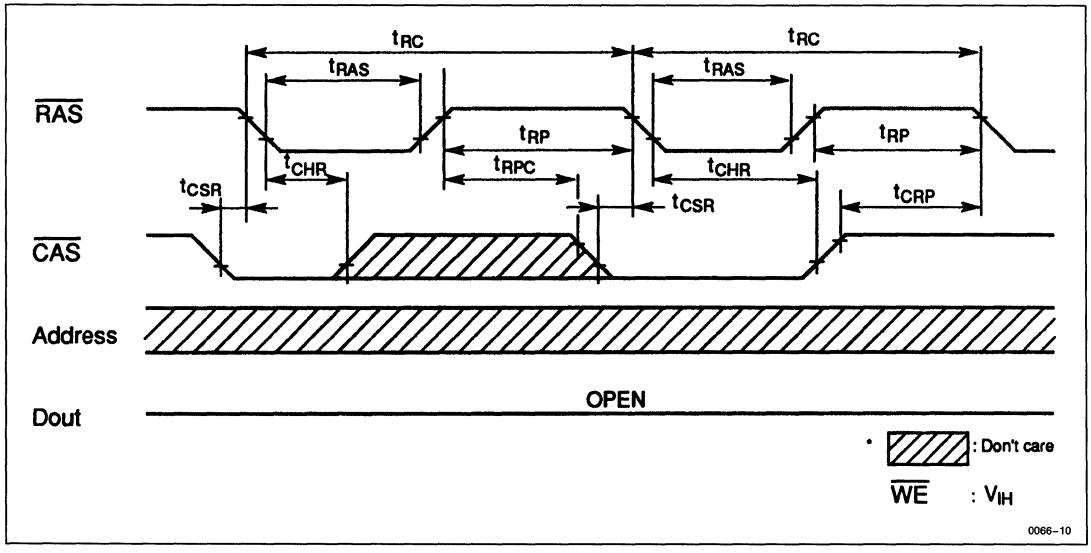
• **$\overline{RAS}$ Only Refresh Cycle (5)**



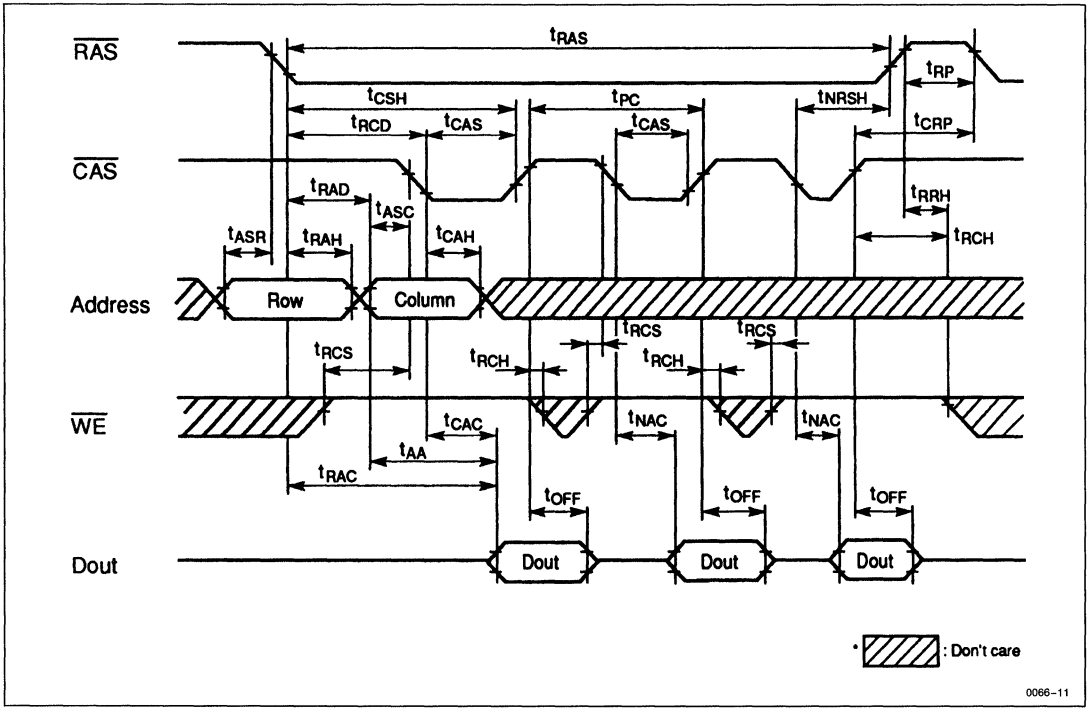
• **Hidden Refresh Cycle (6)**



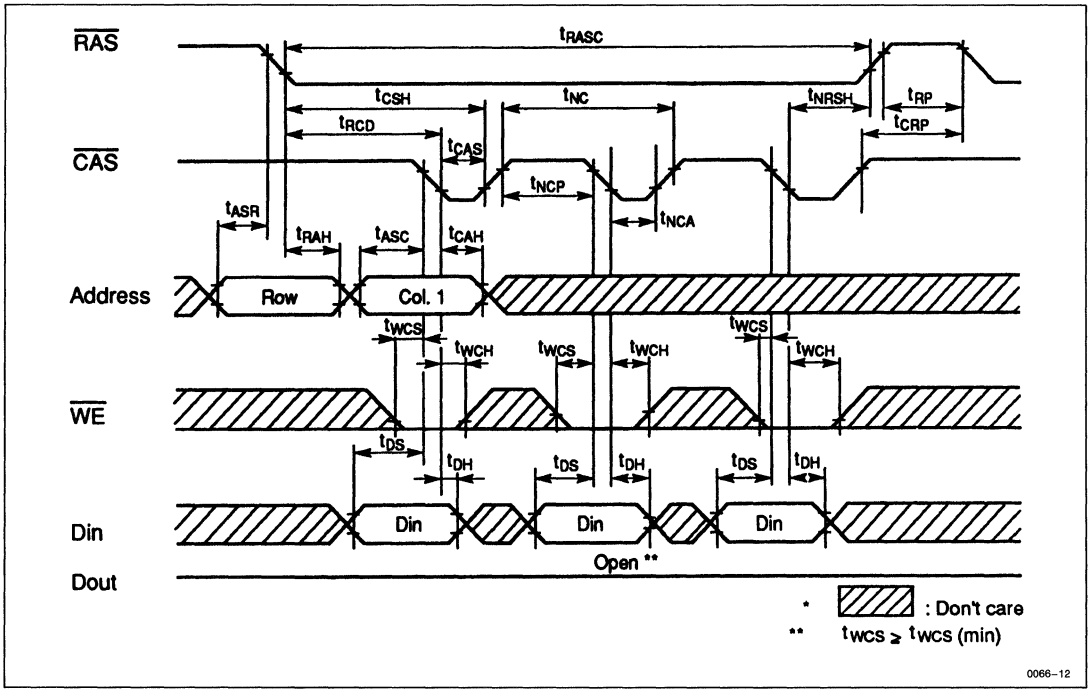
• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle (7)**



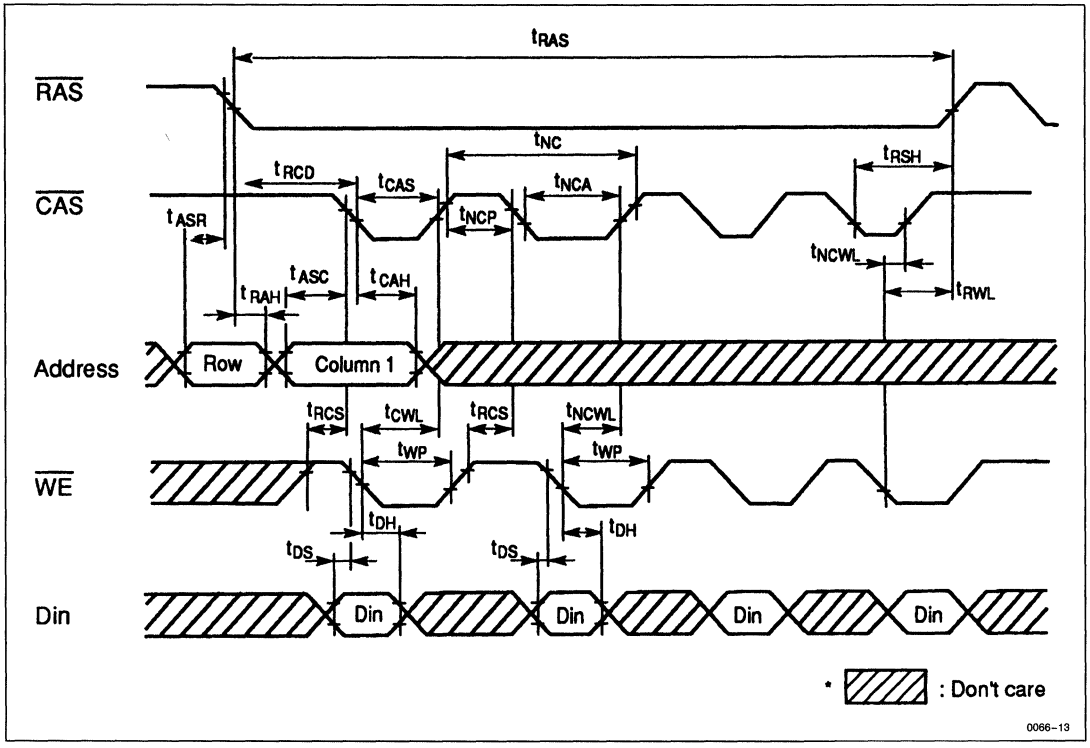
• **Nibble Mode Read Cycle (8)**



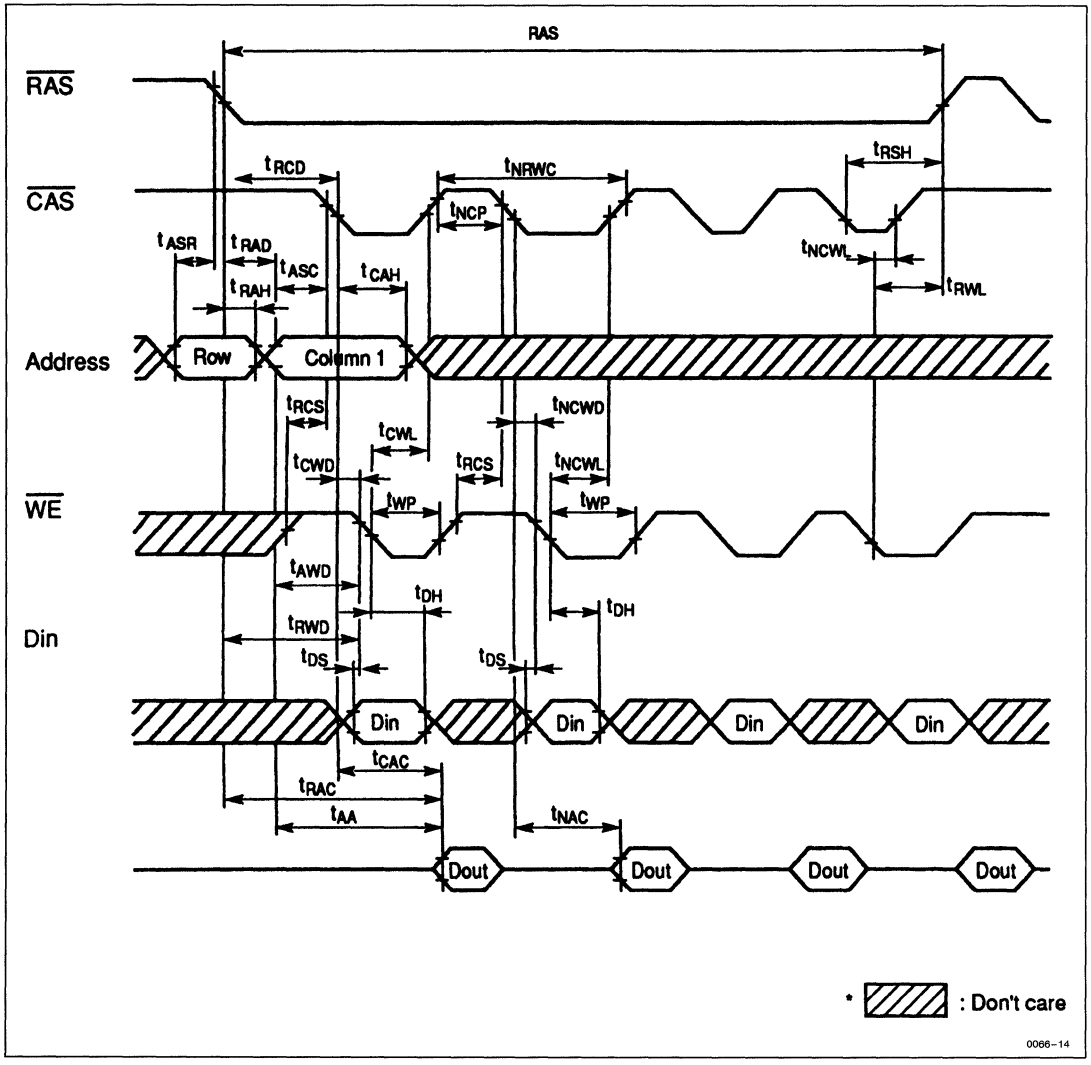
• **Nibble Mode Early Write Cycle (9)**



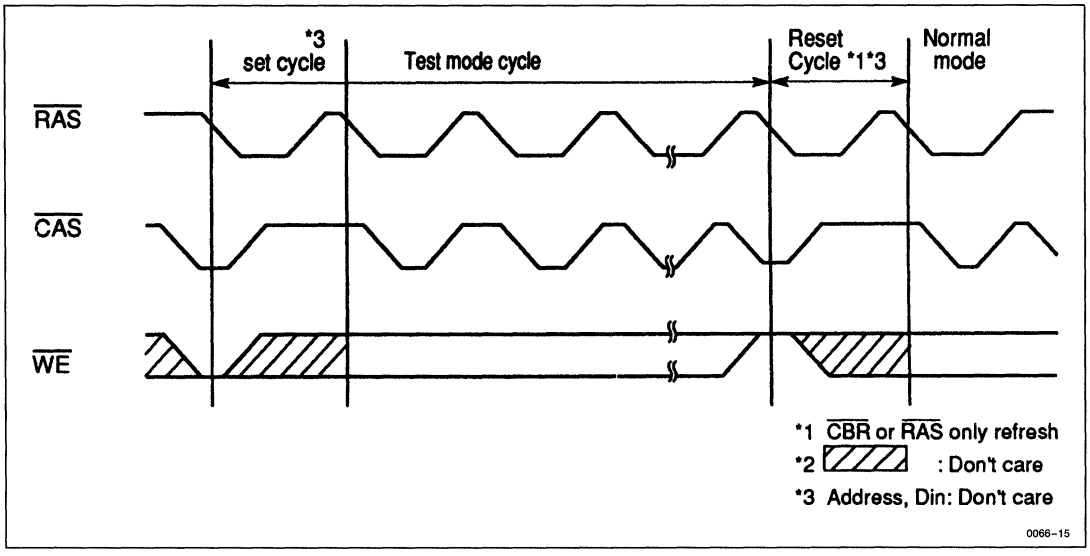
• **Nibble Mode Delayed Write Cycle (10)**



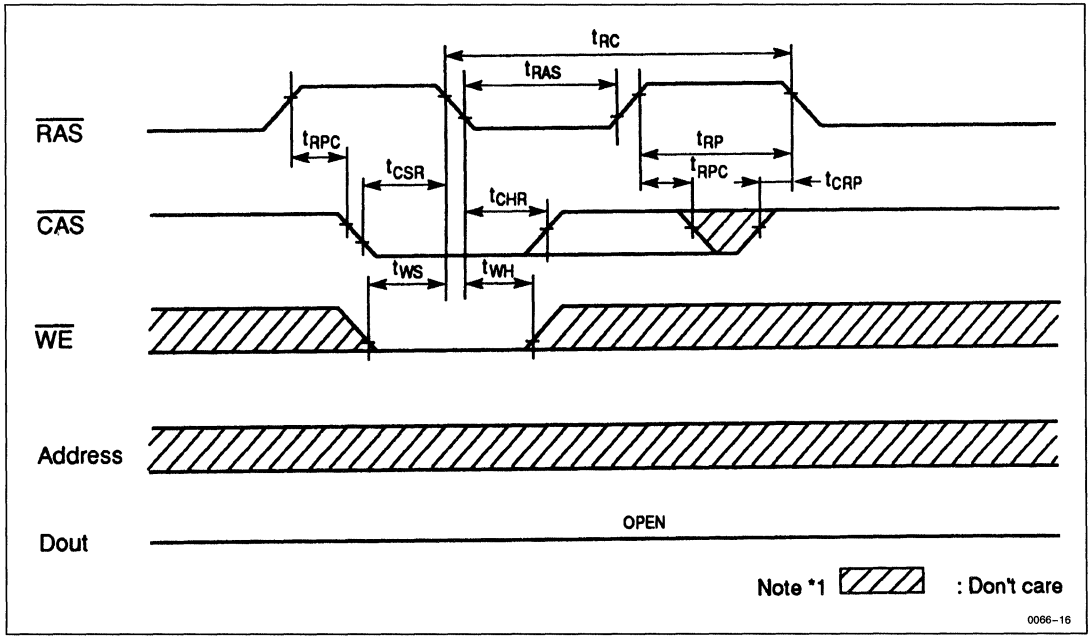
• **Nibble Mode Read-Modify-Write Cycle (11)**



• Test Mode Cycle

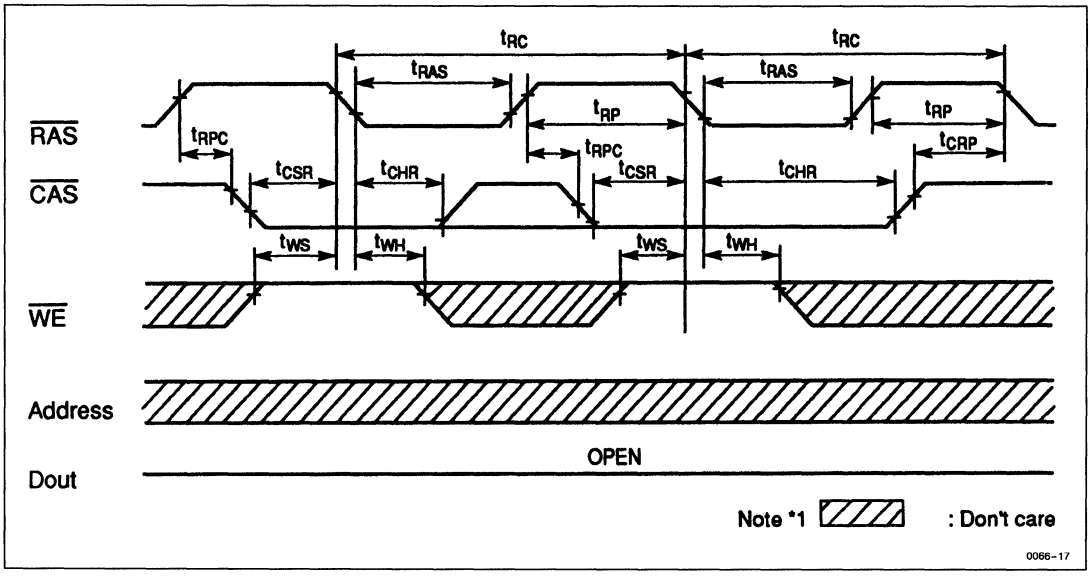


Test Mode Set Cycle (1)

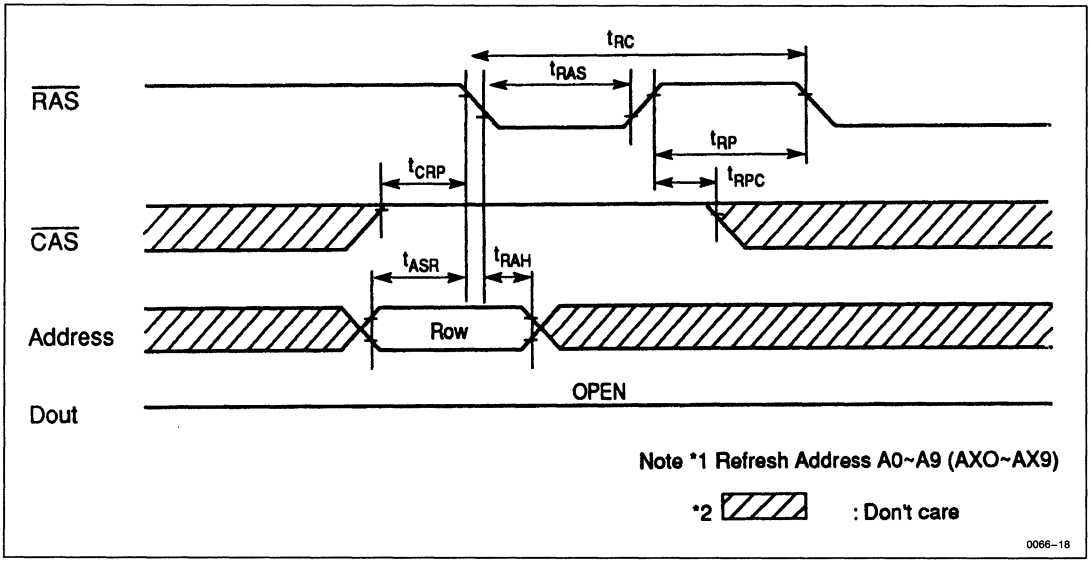


• **Test Mode Reset Cycle (2)**

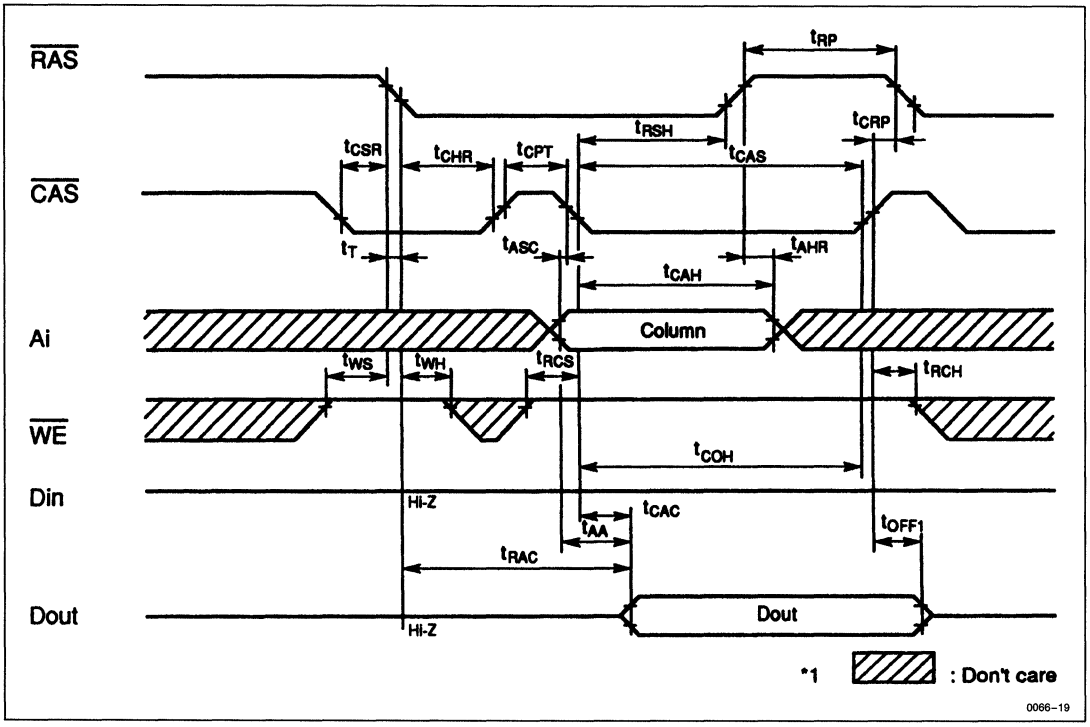
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



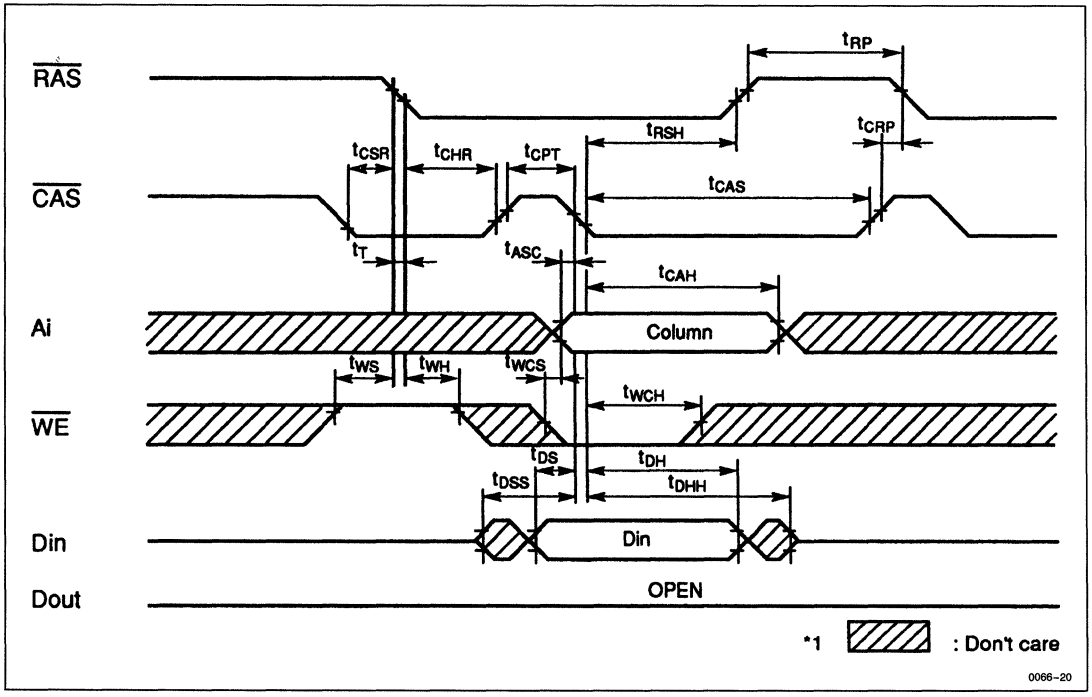
$\overline{RAS}$ Only Refresh Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (READ)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (WRITE)



HM514101A Series — Preliminary

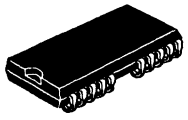
4,194,304-Word x 1-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514101A is a CMOS dynamic RAM organized as 4,194,304-word x 1-bit. HM514101A has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514101A offers Nibble Mode as a high speed access mode.

Multiplexed address input permits the HM514101A to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

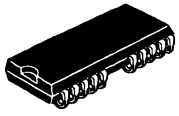
HM514101AJ Series



3DCP20DA

(CP-20DA)

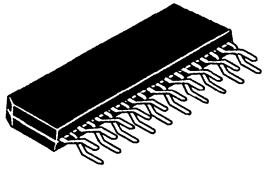
HM514101AS Series



3DCP20D

(CP-20D)

HM514101AZ Series



3DZP20

(ZP-20)

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode .....550 mW/495 mW/440 mW (max)
  - Standby Mode.....11 mW (max)
- Nibble Mode Capability
- 1,024 Refresh Cycles.....(16 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Test Function

■ ORDERING INFORMATION

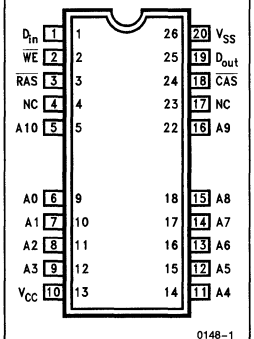
Part No.	Access Time	Package
HM514101AJ-7	70 ns	350 mil 20-pin
HM514101AJ-8	80 ns	Plastic SOJ
HM514101AJ-10	100 ns	(CP-20DA)
HM514101AS-7	70 ns	300 mil 20-pin
HM514101AS-8	80 ns	Plastic SPJ
HM514101AS-10	100 ns	(CP-20D)
HM514101AZ-7	70 ns	400 mil 20-pin
HM514101AZ-8	80 ns	Plastic ZIP
HM514101AZ-10	100 ns	(ZP-20)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{10}	Address Input
A_0–A_9	Refresh Address Input
D_{in}	Data-in
D_{out}	Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power (+ 5V)
V_{SS}	Ground

■ PIN OUT

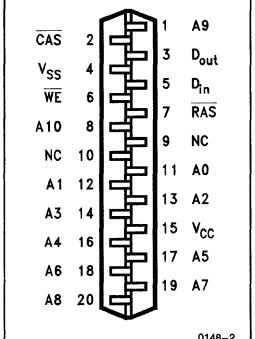
HM514101AJ/AS Series



0148-1

(Top View)

HM514101AZ Series



0148-2

(Bottom View)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	− 2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HM514101A-7		HM514101A-8		HM514101A-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	100	—	90	—	80	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	1	—	1	—	1	mA	CMOS Interface, $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	100	—	90	—	80	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	100	—	90	—	80	mA	t_{RC} = Min	
Nibble Mode Current	I_{CC8}	—	100	—	90	—	80	mA	t_{NC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed ≤ 1 time while $\overline{RAS}$ = V_{IL}.
3. Address can be changed ≤ 1 time while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address, Data-in)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-out)	C_O	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 12, 13]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514101A-7		HM514101A-8		HM514101A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	20	60	25	75	ns	8
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	15	40	20	55	ns	9
$\overline{CAS}$ Hold Time	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514101A-7		HM514101A-8		HM514101A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	2, 3, 14
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	3, 4
Access Time from Address	t_{AA}	—	35	—	40	—	45	ns	3, 5, 14
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	35	—	40	—	45	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	20	0	25	ns	6

Write Cycle

Parameter	Symbol	HM514101A-7		HM514101A-8		HM514101A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514101A-7		HM514101A-8		HM514101A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	155	—	175	—	210	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	70	—	80	—	100	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	20	—	20	—	25	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	35	—	40	—	45	—	ns	10

Refresh Cycle

Parameter	Symbol	HM514101A-7		HM514101A-8		HM514101A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time in Normal Mode	t_{CPN}	10	—	10	—	10	—	ns	

Nibble Mode Cycle

Parameter	Symbol	HM514101A-7		HM514101A-8		HM514101A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Nibble Mode Access Time	t_{NAC}	—	20	—	25	—	25	ns	
Nibble Mode Cycle Time	t_{NC}	40	—	45	—	45	—	ns	
Nibble Mode $\overline{CAS}$ Precharge Time	t_{NCP}	10	—	10	—	10	—	ns	
Nibble Mode $\overline{CAS}$ Pulse Width	t_{NCA}	20	—	25	—	25	—	ns	
Nibble Mode $\overline{RAS}$ Hold Time	t_{NRSH}	20	—	25	—	25	—	ns	

Nibble Mode Read-Modify-Write Cycle

Parameter	Symbol	HM514101A-7		HM514101A-8		HM514101A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Nibble Mode Read-Modify-Write Cycle Time	t_{NRWC}	55	—	75	—	75	—	ns	
Nibble Mode Write Command to $\overline{CAS}$ Lead Time	t_{NCWL}	20	—	25	—	25	—	ns	
Nibble Mode $\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{NCWD}	20	—	25	—	25	—	ns	

Test Mode Cycle

Parameter	Symbol	HM514101A-7		HM514101A-8		HM514101A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WS}	10	—	10	—	10	—	ns	

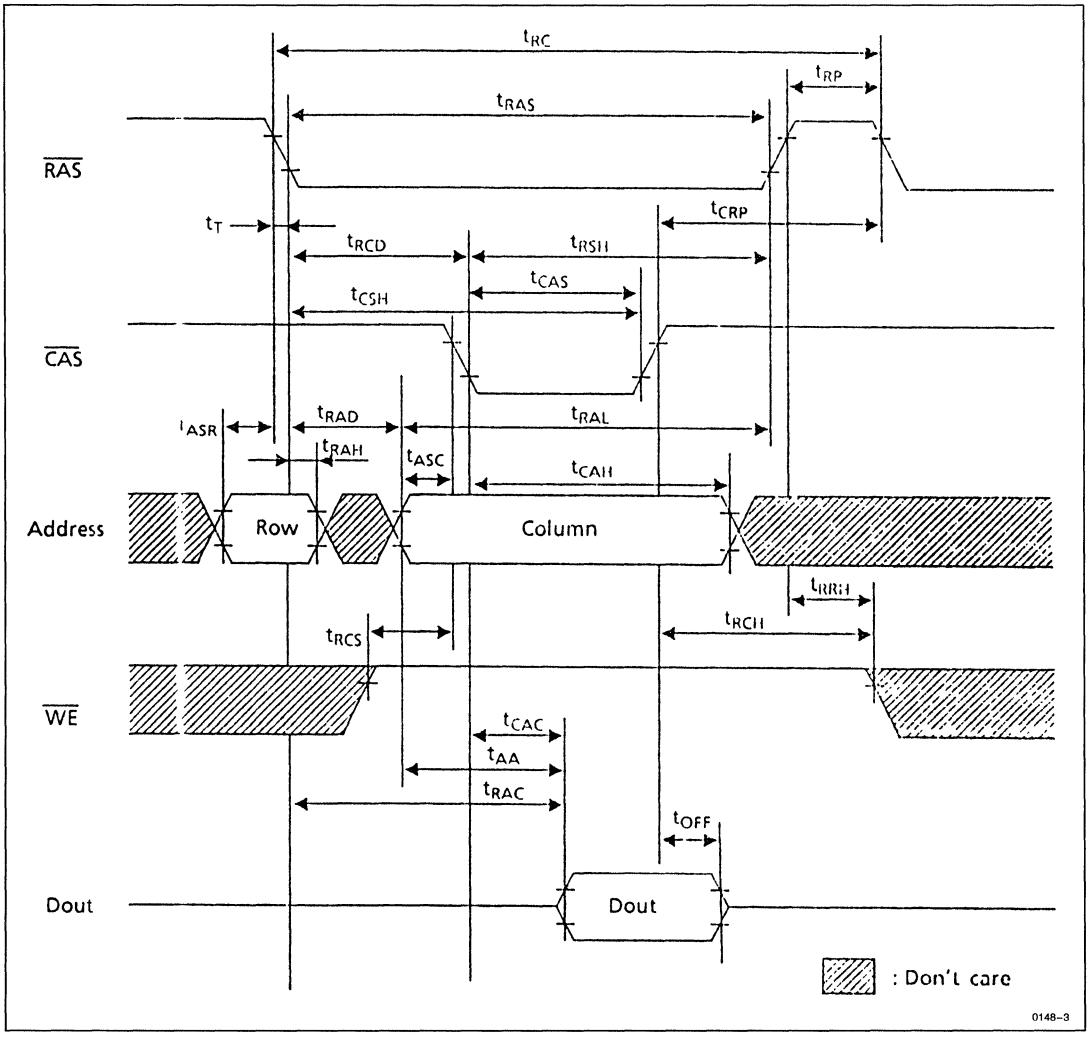
Counter Test Cycle

Parameter	Symbol	HM514101A-7		HM514101A-8		HM514101A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	40	—	50	—	ns	

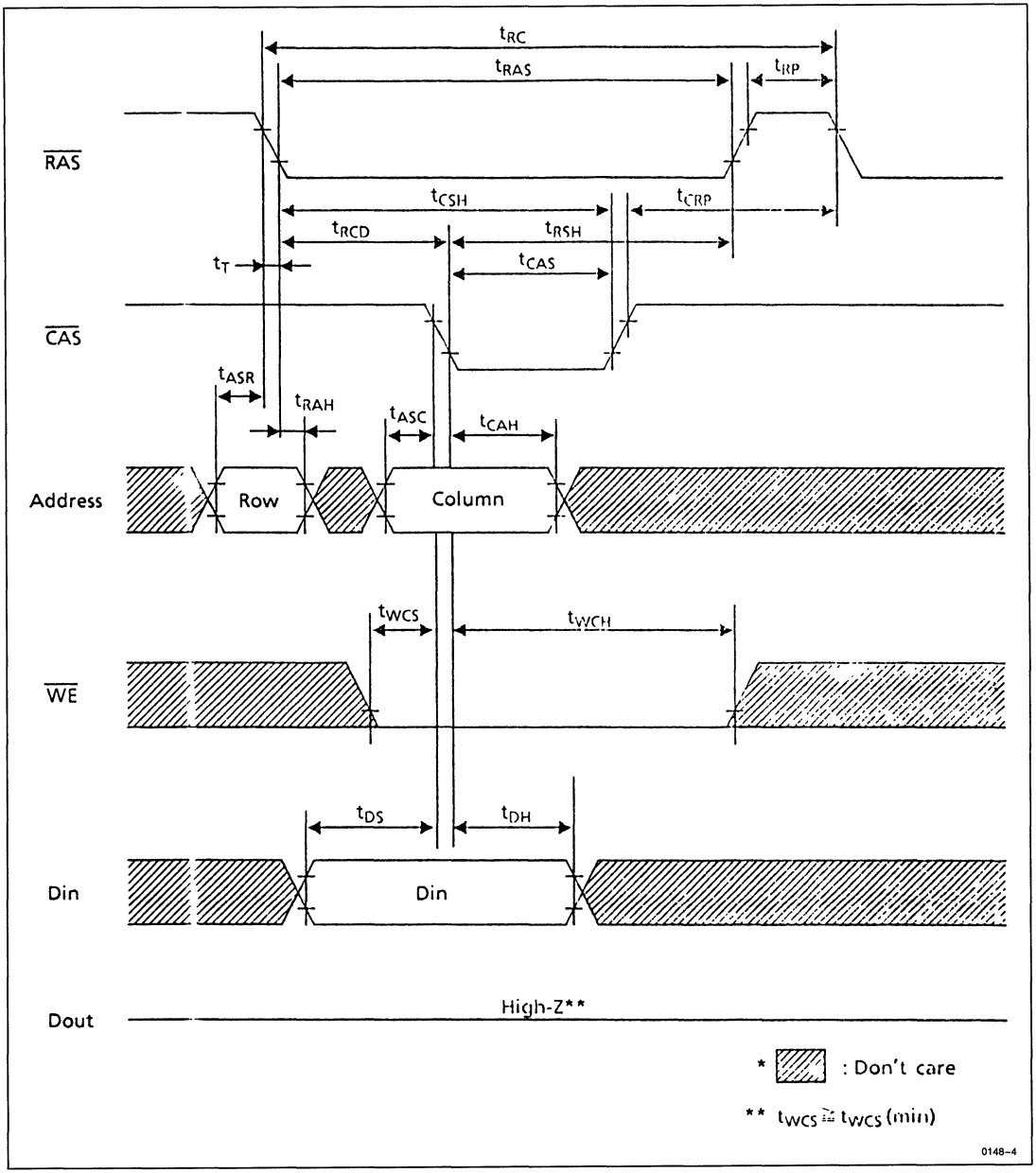
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. An initial pause of 100 μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
13. Test mode operation specified in this data sheet is 8-bit test function with control address bits—RA10, CA10 and CA0 being don't care. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits match each other, the condition of the output data is high level. When the state of test bits do not match, the condition of the output data is low level. Data output pin is D_{out} and data input pin is D_{in}. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
14. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{NAC} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORMS

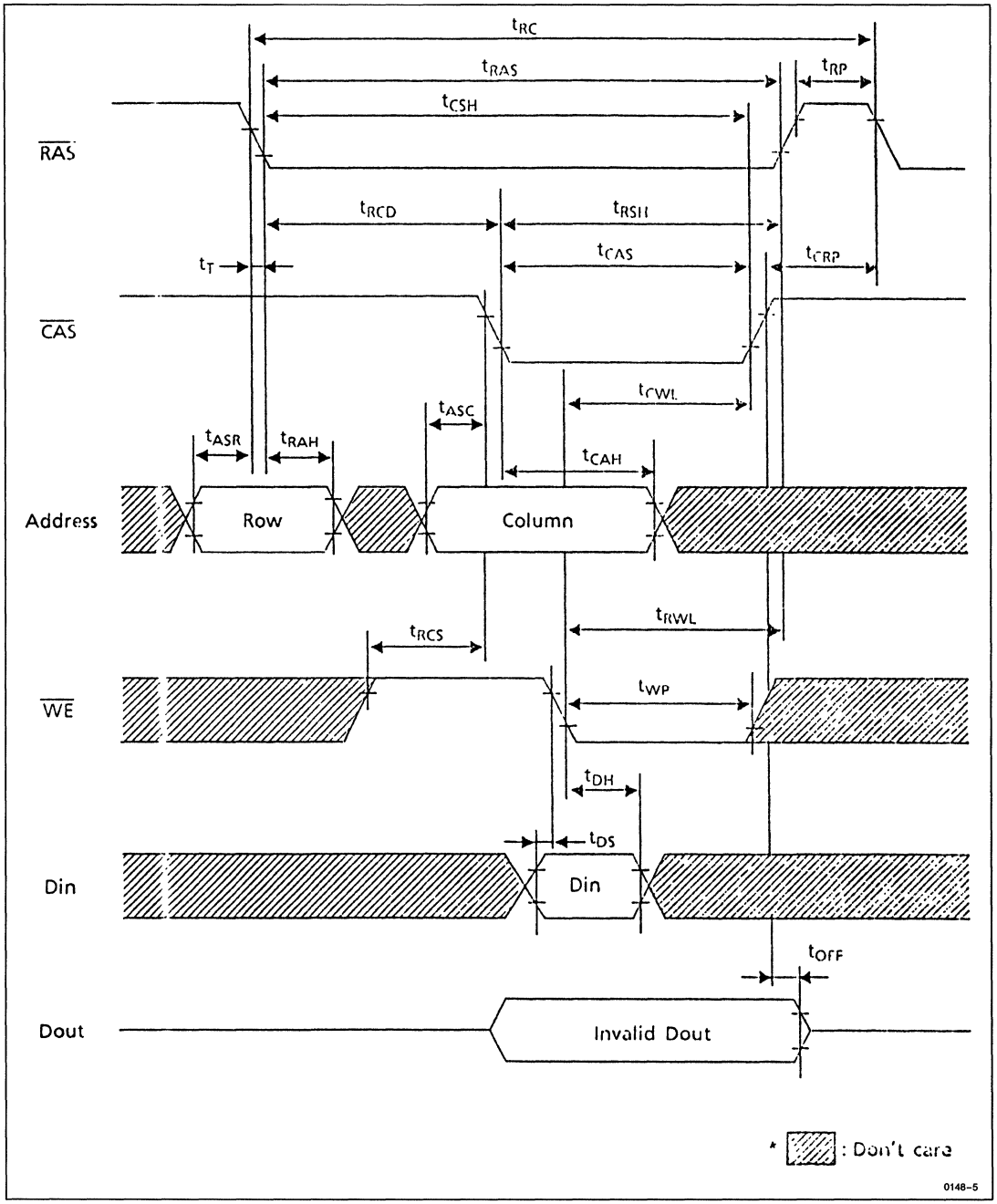
• Read Cycle



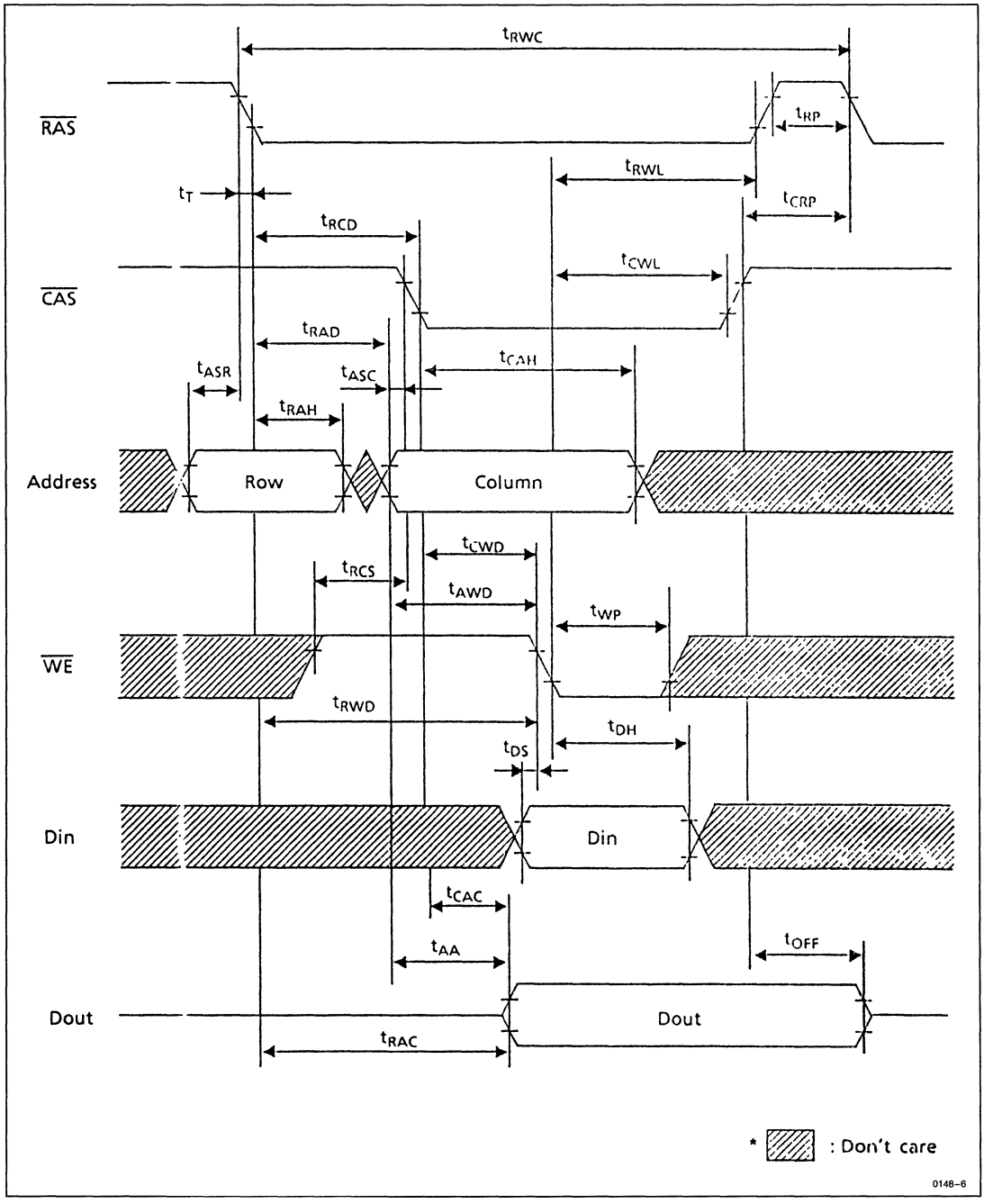
• **Early Write Cycle**



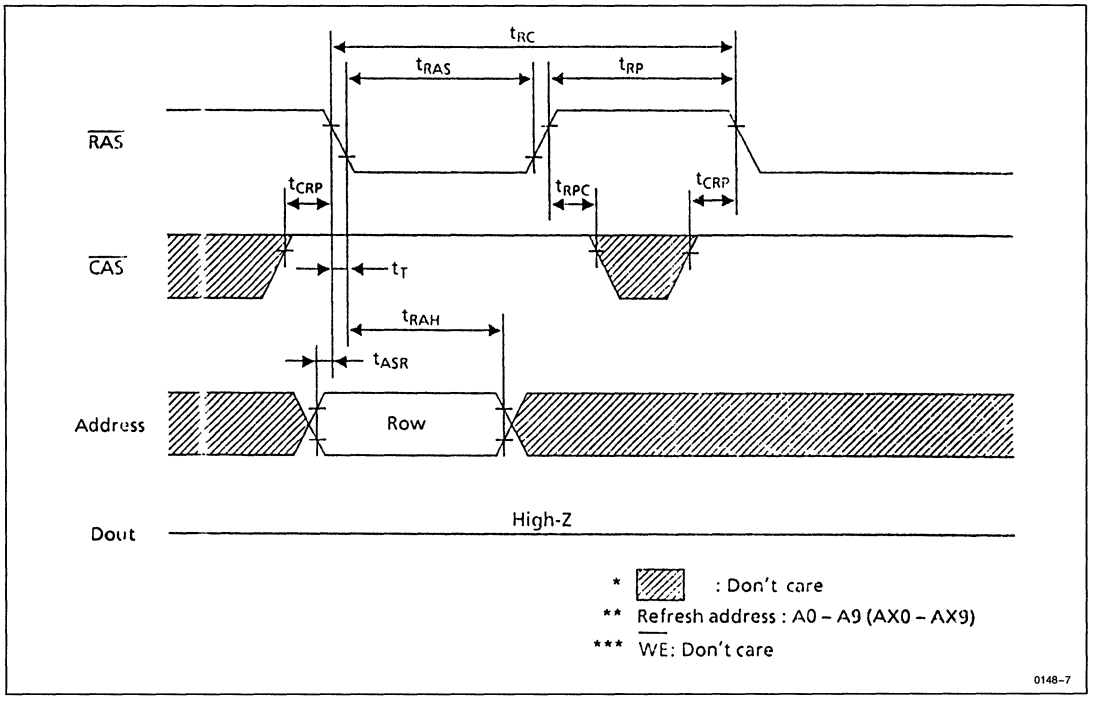
• **Delayed Write Cycle**



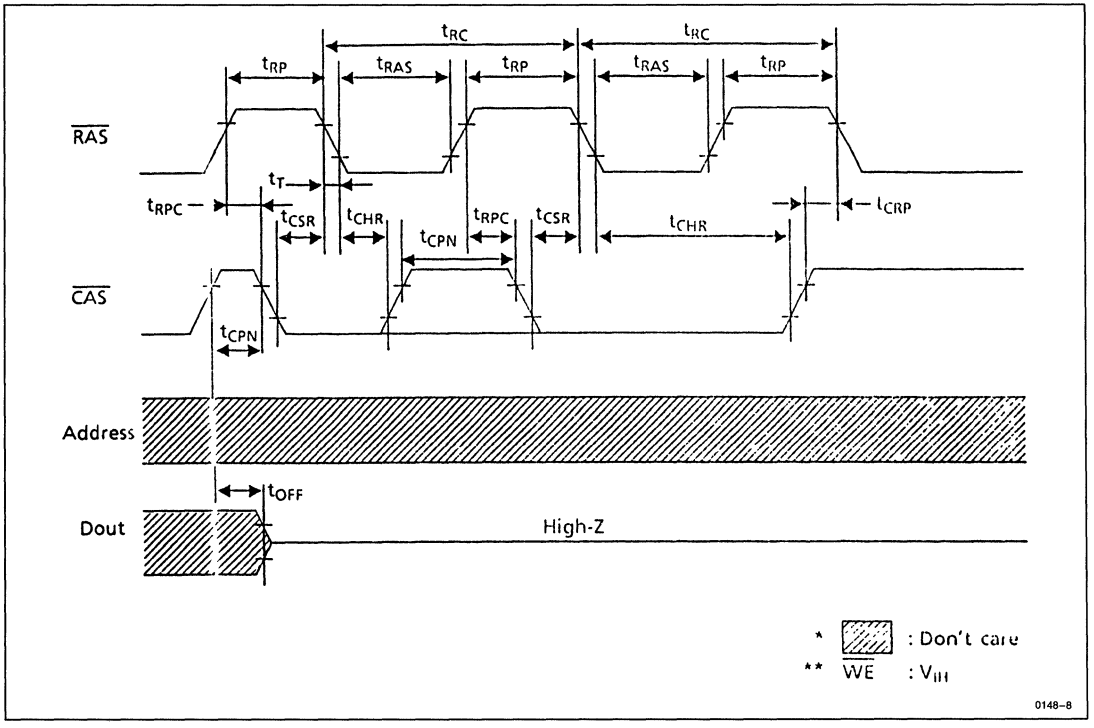
• **Read-Modify-Write Cycle**



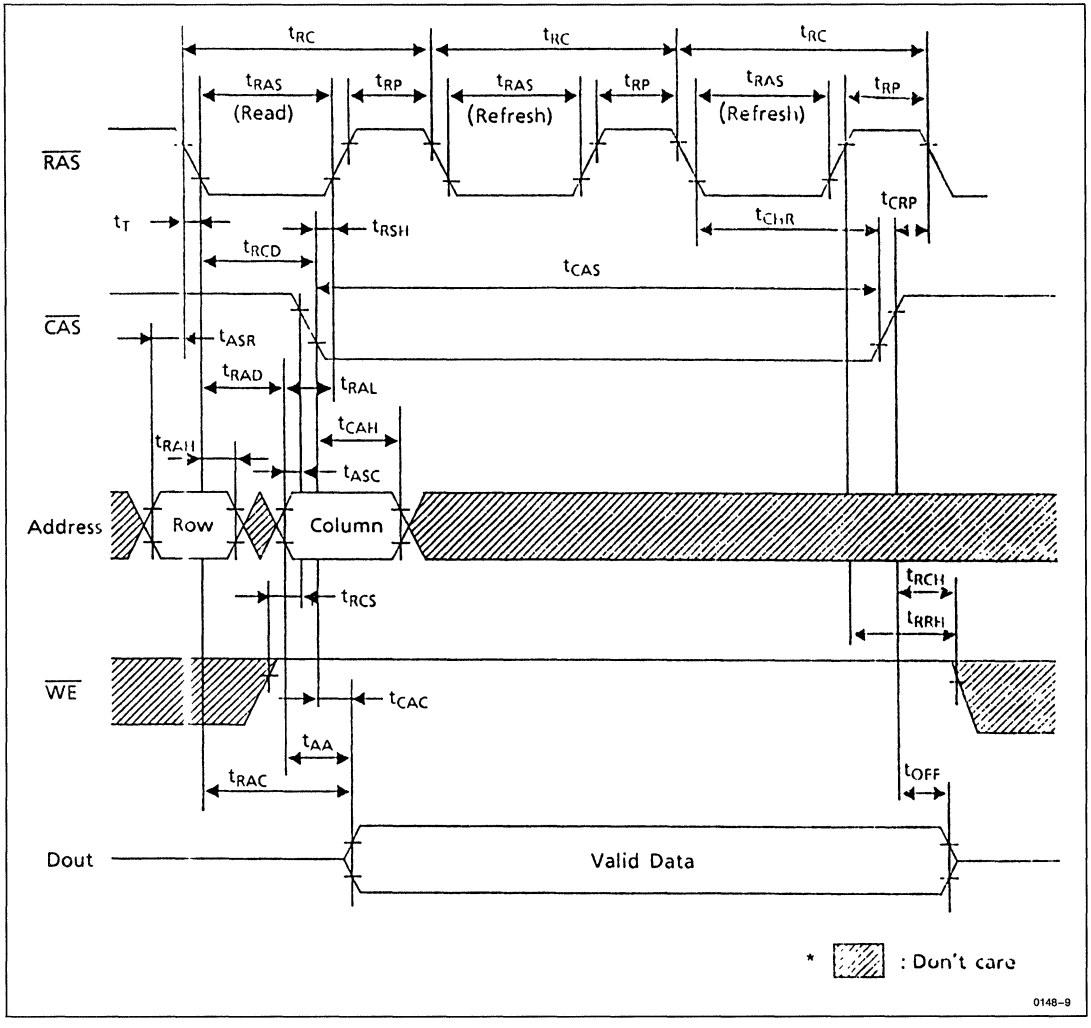
• $\overline{RAS}$ Only Refresh Cycle



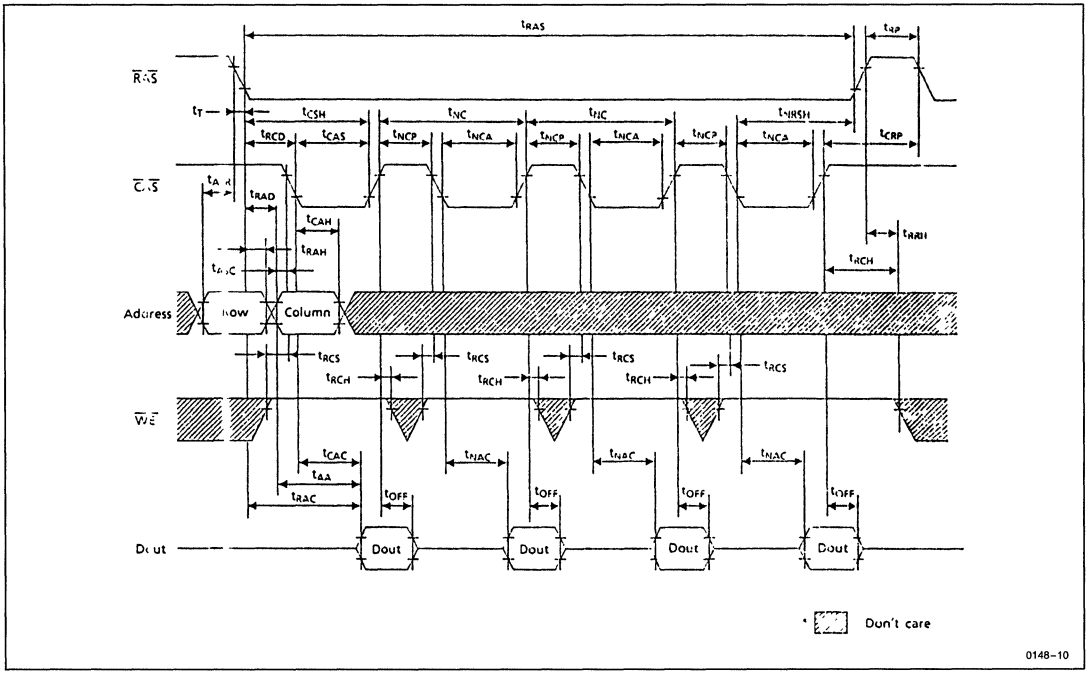
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



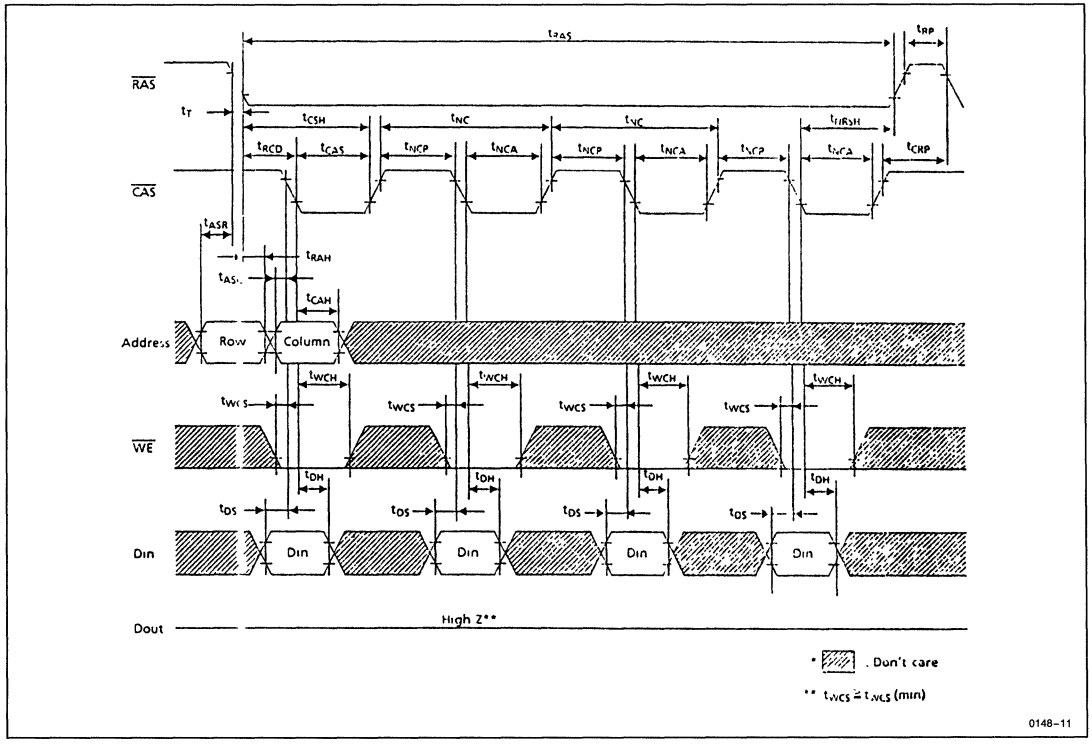
• **Hidden Refresh Cycle**



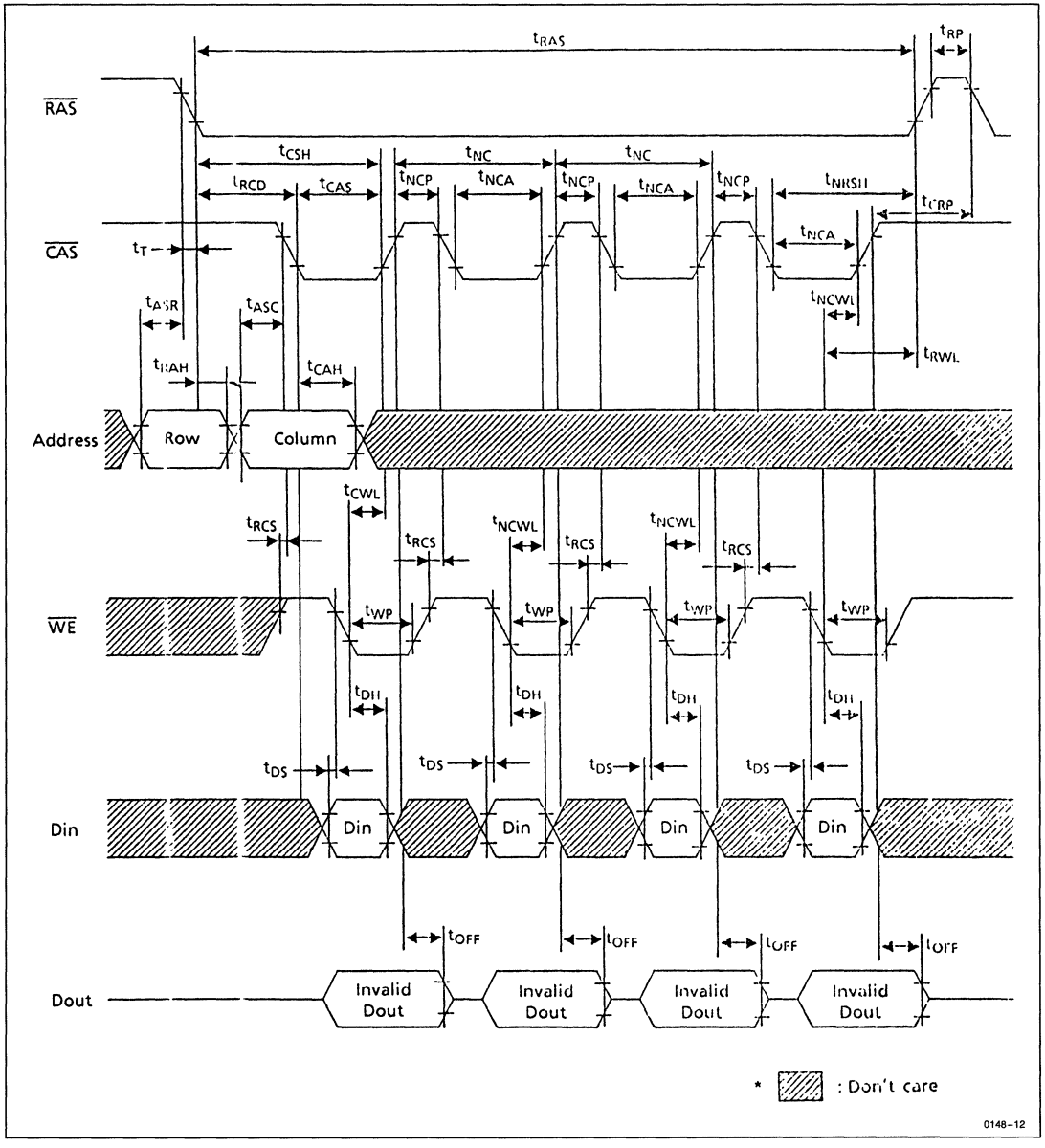
• Nibble Mode Read Cycle



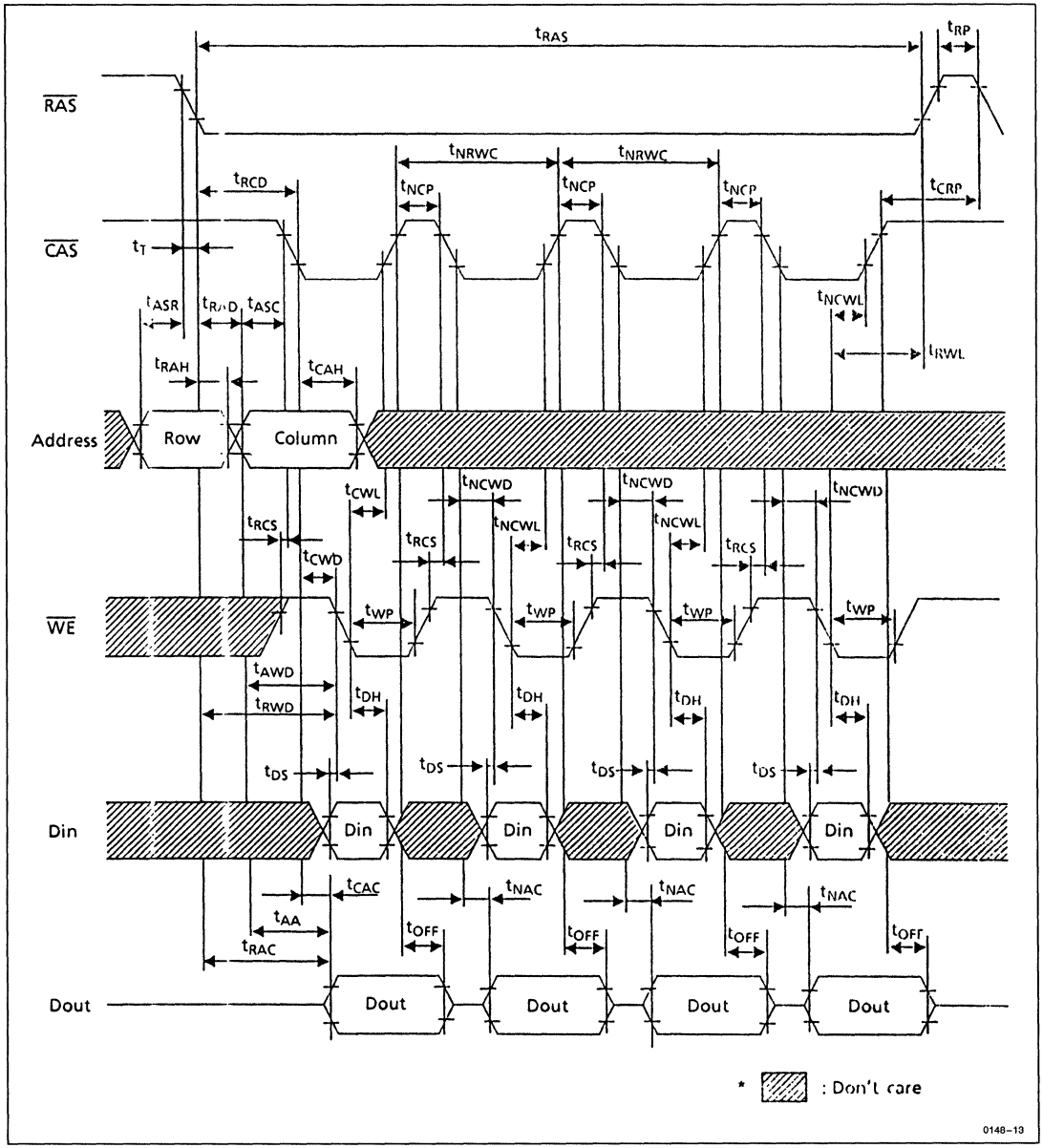
• Nibble Mode Early Write Cycle



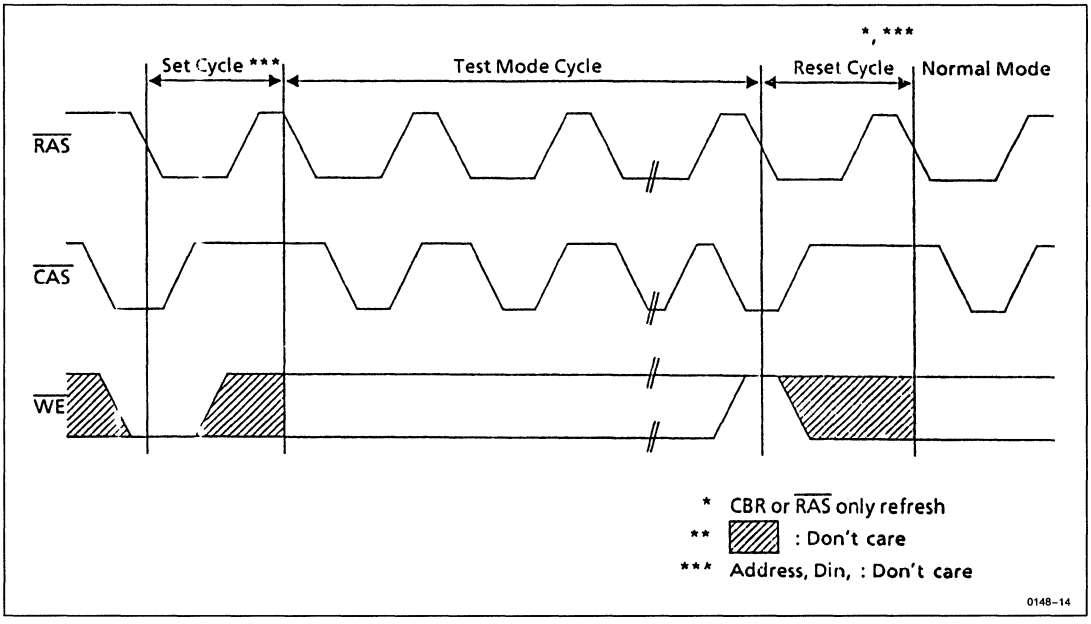
• **Nibble Mode Delayed Write Cycle**



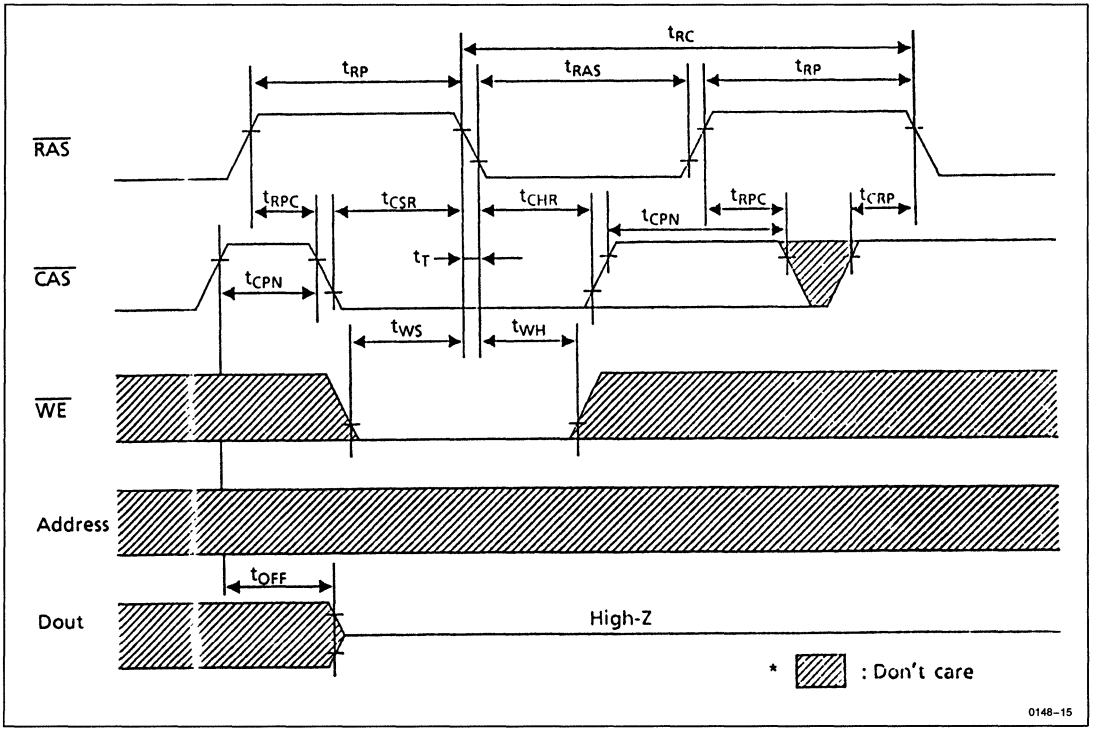
• **Nibble Mode Read-Modify-Write Cycle**



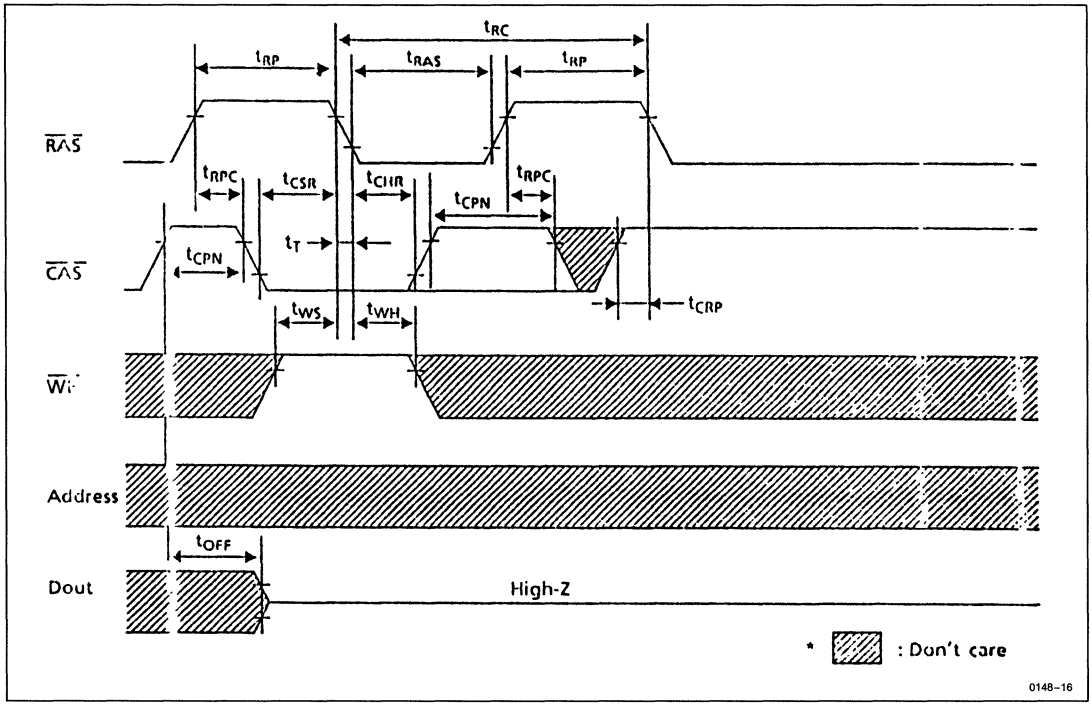
• **Test Mode Cycle**



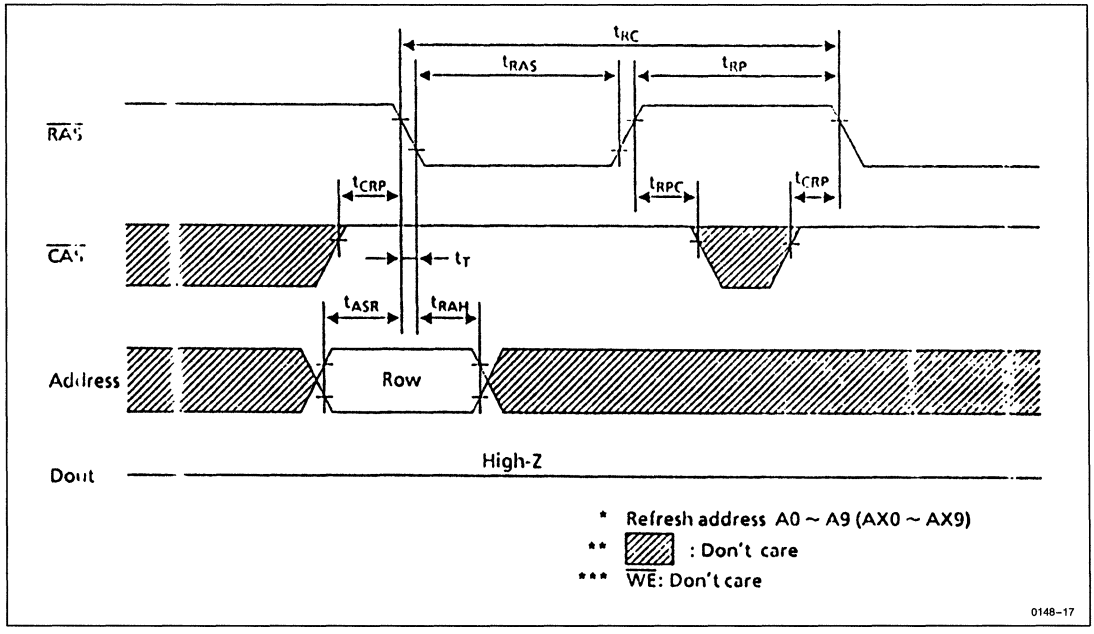
• **Test Mode Set Cycle**
WE and CAS Before RAS Refresh Cycle



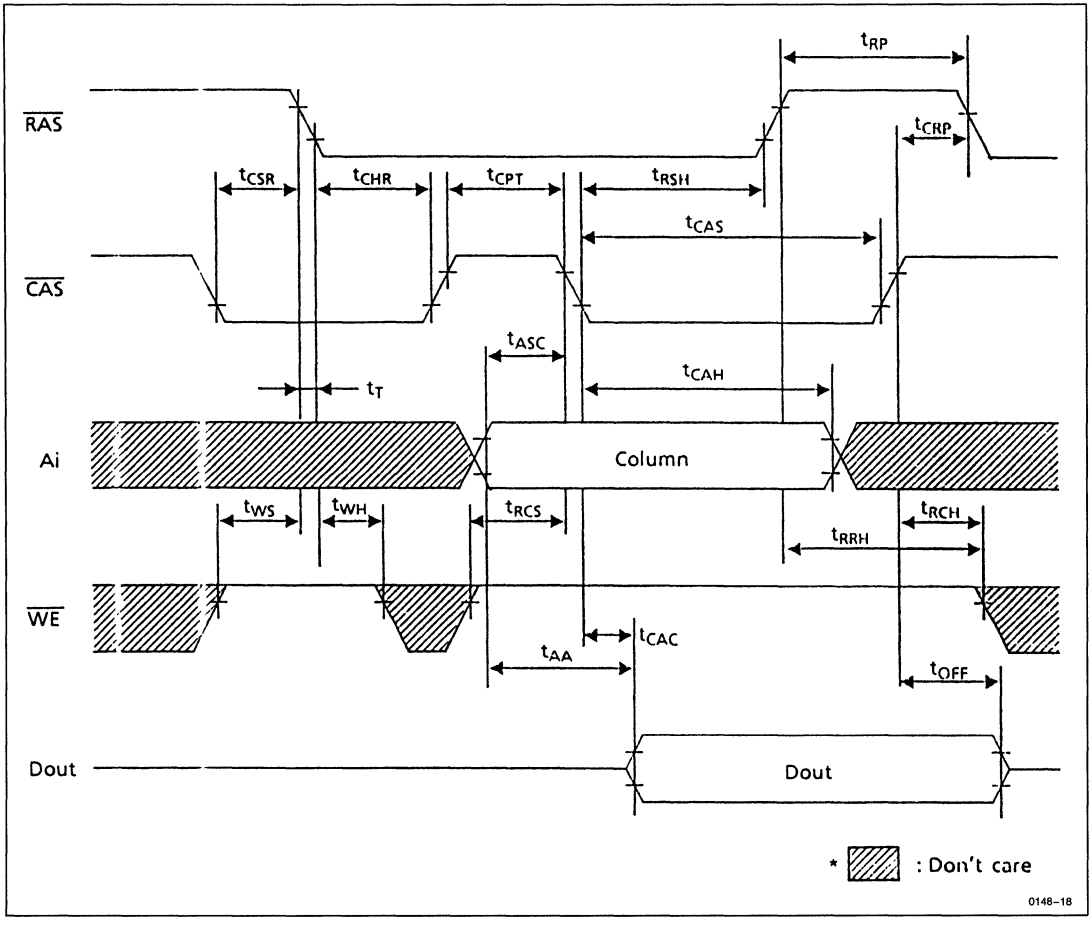
• **Test Mode Reset Cycle**
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



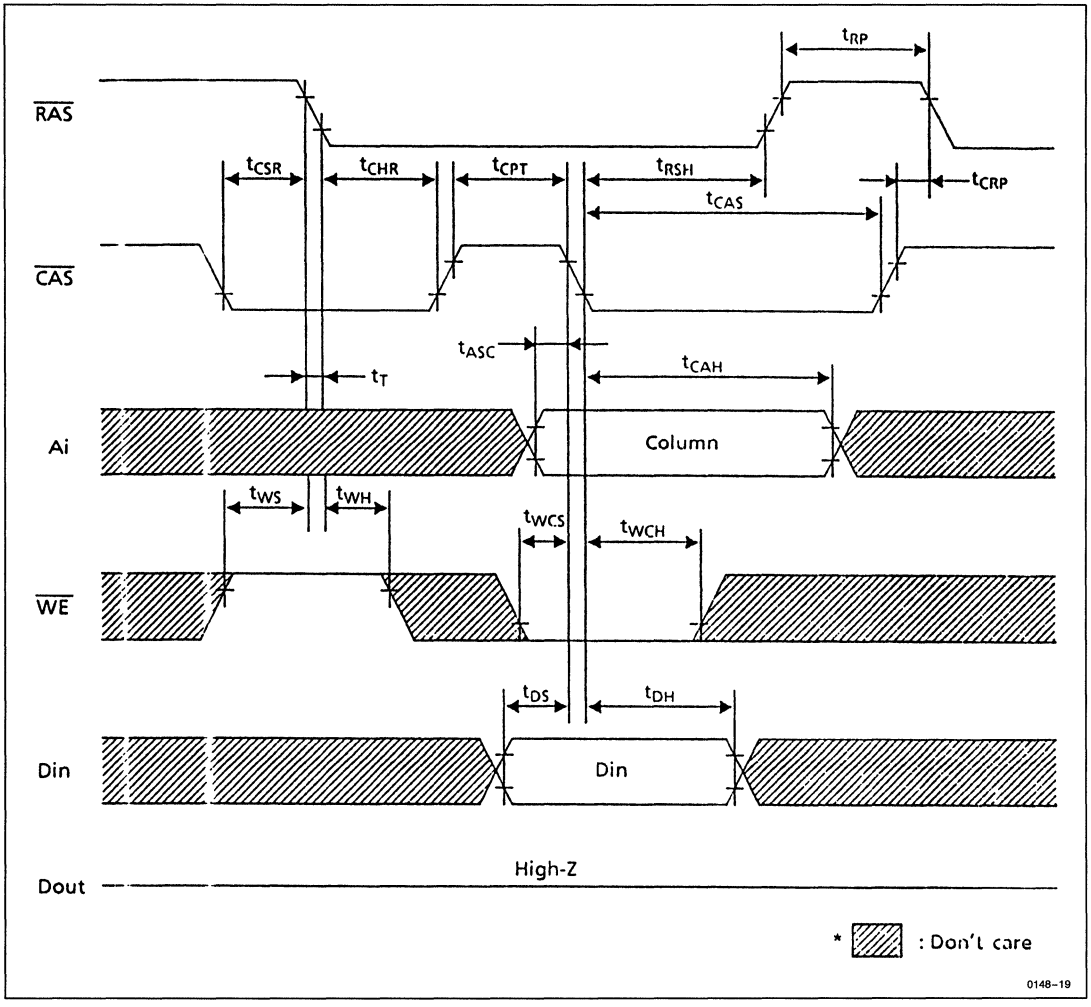
$\overline{RAS}$ Only Refresh Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM514400 Series

1,048,576-Word x 4-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514400 is a CMOS dynamic RAM organized 1,048,576 word x 4-bit. HM514400 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514400 offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514400 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time ..... 80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode ..... 495 mW/440 mW/385 mW (max)
  - Standby Mode ..... 11 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles ..... (16 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Test Function

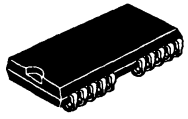
■ ORDERING INFORMATION

Part No.	Access	Package
HM514400JP-8	80 ns	350 mil 20-pin
HM514400JP-10	100 ns	Plastic SOJ
HM514400JP-12	120 ns	(CP-20DA)
HM514400ZP-8	80 ns	400 mil 20-pin
HM514400ZP-10	100 ns	Plastic ZIP
HM514400ZP-12	120 ns	(ZP-20)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_9	Refresh Address Input
I/O_1–I/O_4	Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

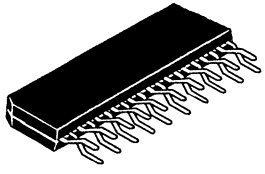
HM514400JP Series



3DCP20DA

(CP-20DA)

HM514400ZP Series

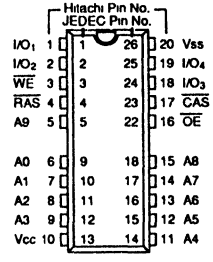


3DZP20

(ZP-20)

■ PIN OUT

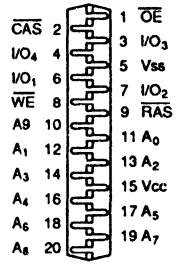
HM514400JP Series



0064-1

(Top View)

HM514100ZP Series



0064-2

(Bottom View)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	− 1.0	—	0.8	V	1
	(Others)	V_{IL}	− 2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	70	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	1	—	1	—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	90	—	80	—	70	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	90	—	80	—	70	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	90	—	80	—	70	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• Capacitance (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 14, 15, 16]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	150	—	180	—	210	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	20	—	25	—	30	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3, 17
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4, 13
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5, 13, 16
Access Time from $\overline{OE}$	t_{OAC}	—	25	—	25	—	30	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	20	0	25	0	30	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	20	0	25	0	30	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	20	—	25	—	30	—	ns	

Write Cycle

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	20	—	25	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	210	—	245	—	285	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	110	—	135	—	160	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	55	—	60	—	70	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	70	—	80	—	95	—	ns	10
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	25	—	25	—	30	—	ns	

Refresh Cycle

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	13, 17
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	105	—	110	—	130	—	ns	

Test Mode Cycle

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	20	—	20	—	20	—	ns	

Counter Test Cycle

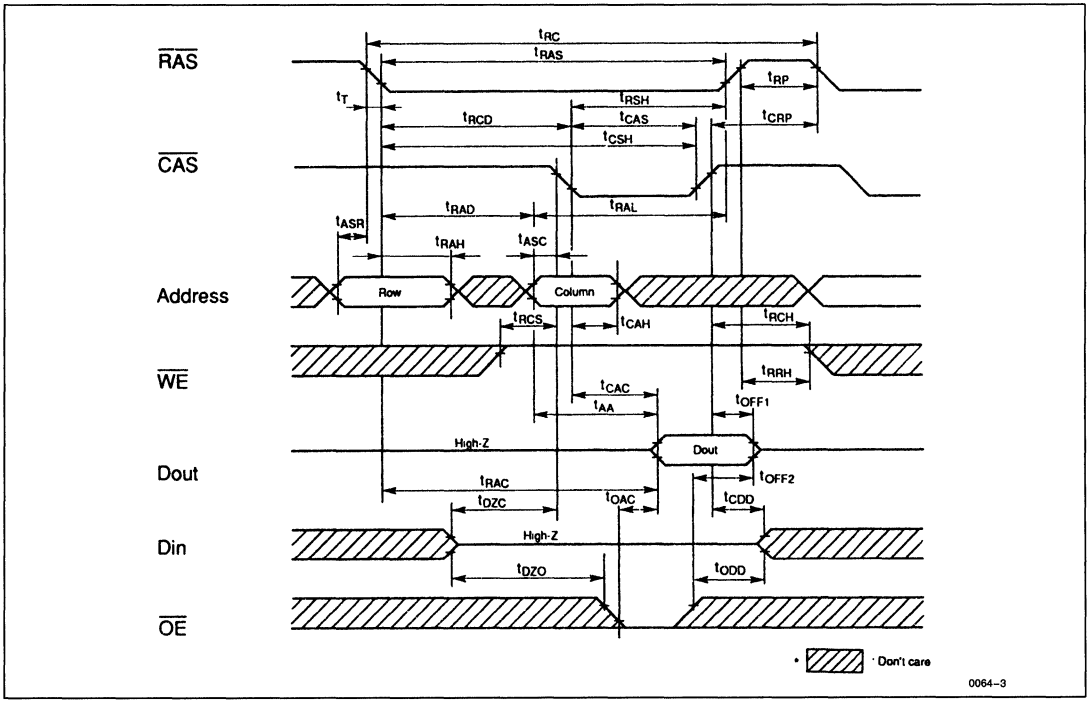
Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	50	—	60	—	ns	

Notes: 1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

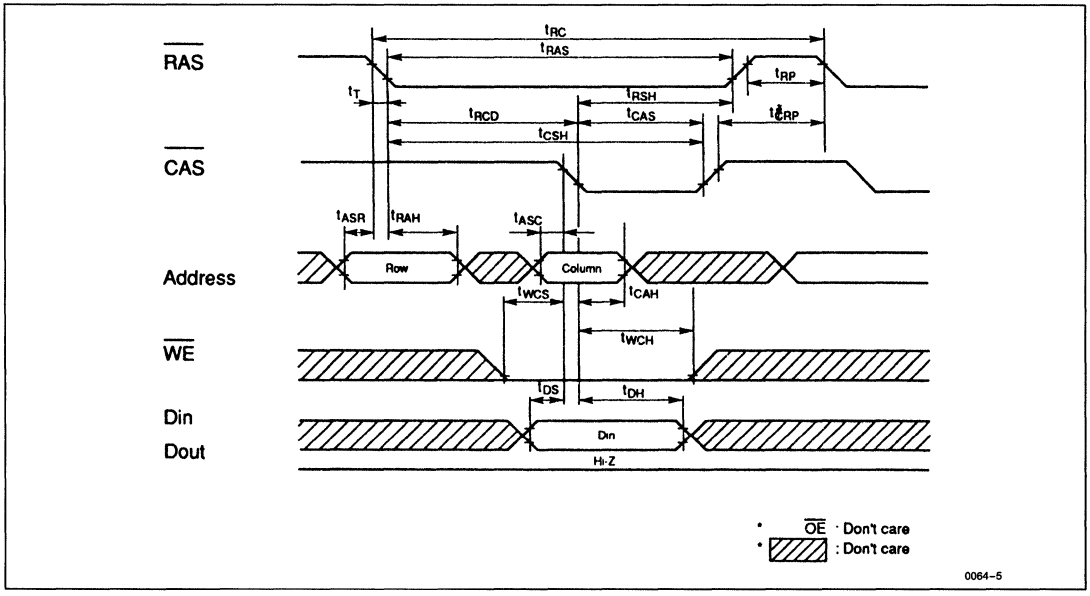
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits—CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is I/O3 and data input pin is I/O2. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{OAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORMS

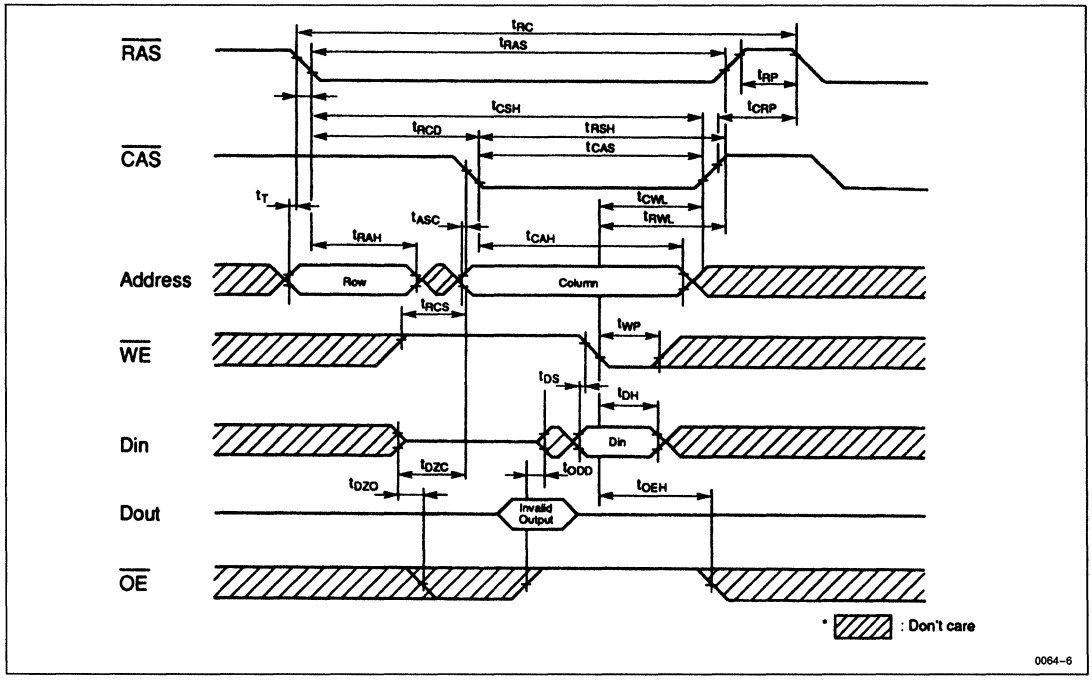
• Read Cycle



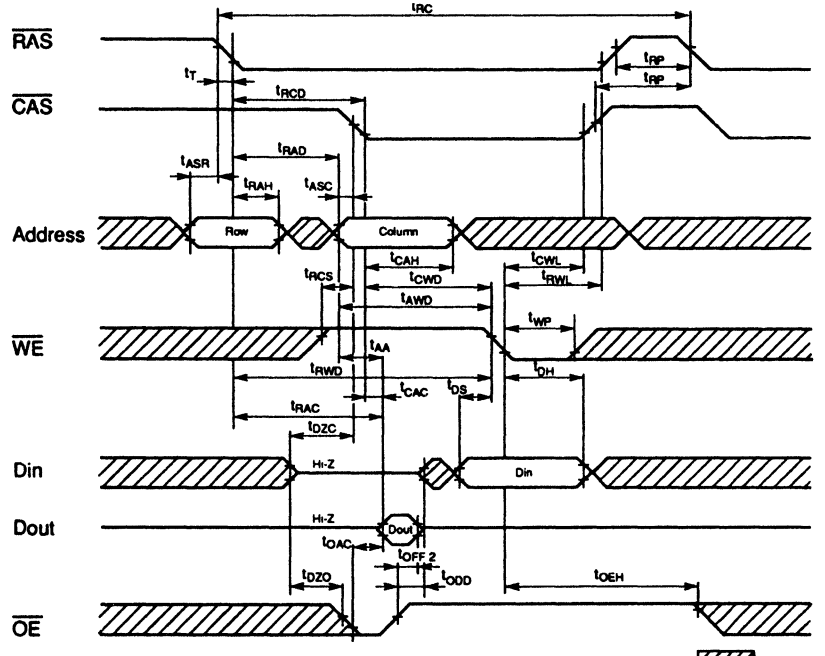
• Early Write Cycle



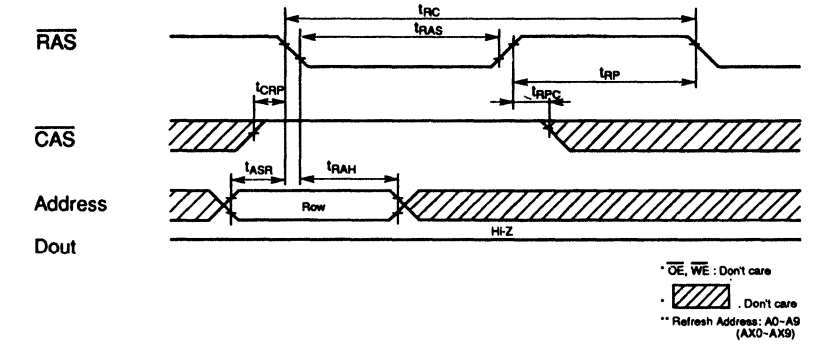
• Delayed Write Cycle



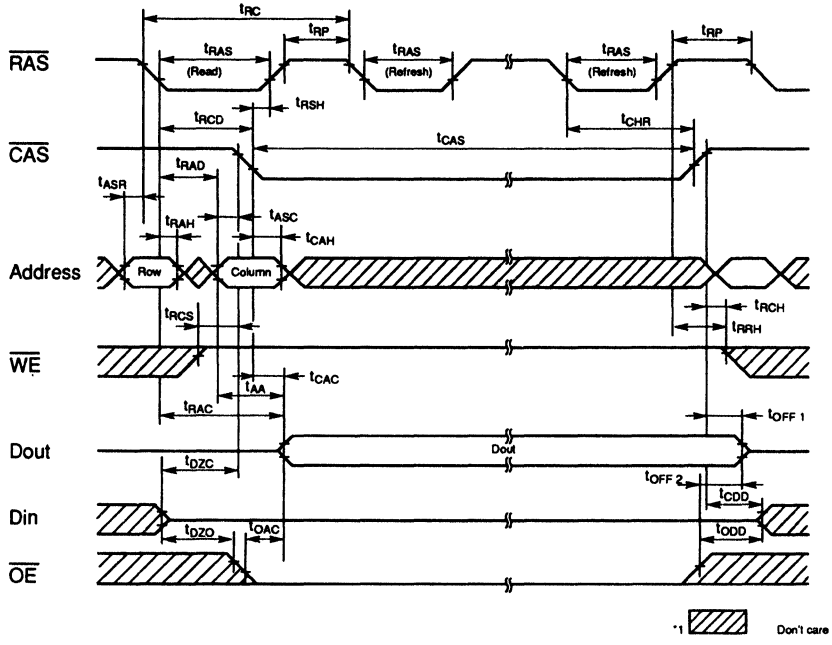
• **Read-Modify-Write Cycle**



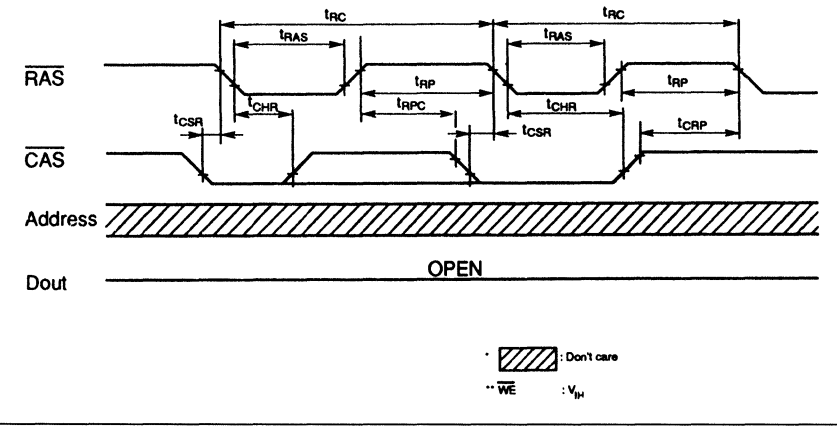
• **$\overline{RAS}$ Only Refresh Cycle**



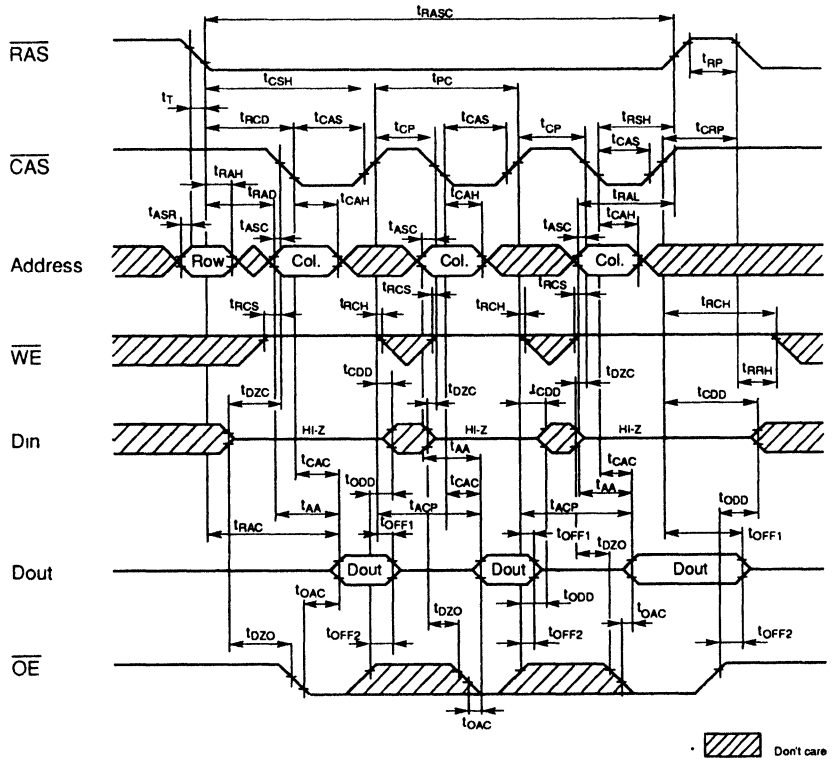
• Hidden Refresh Cycle



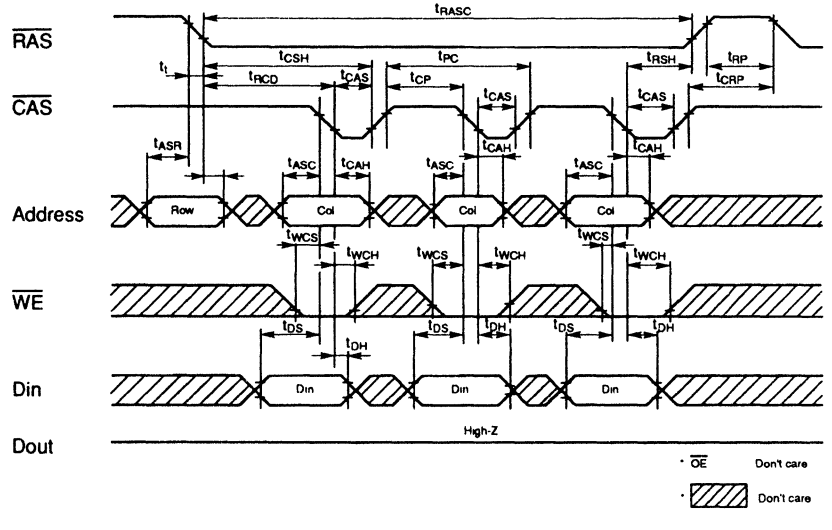
• CAS Before RAS Refresh Cycle



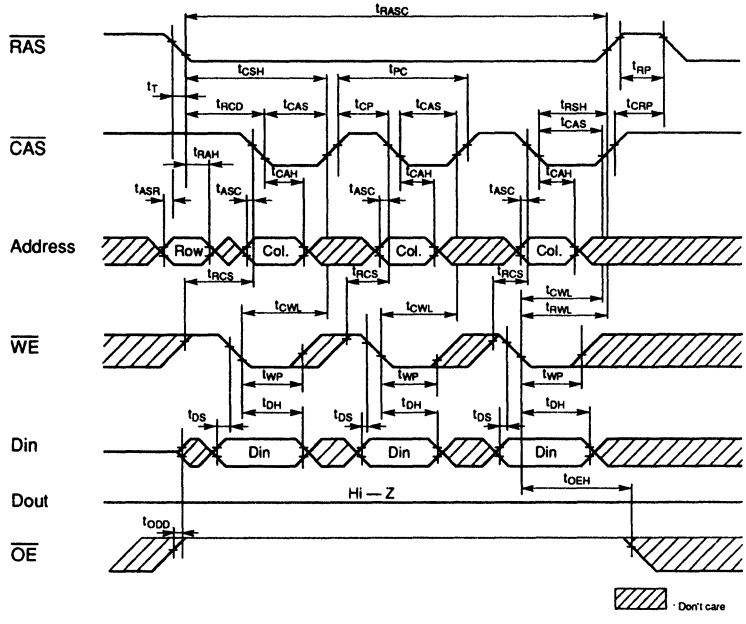
• Fast Page Mode Read Cycle



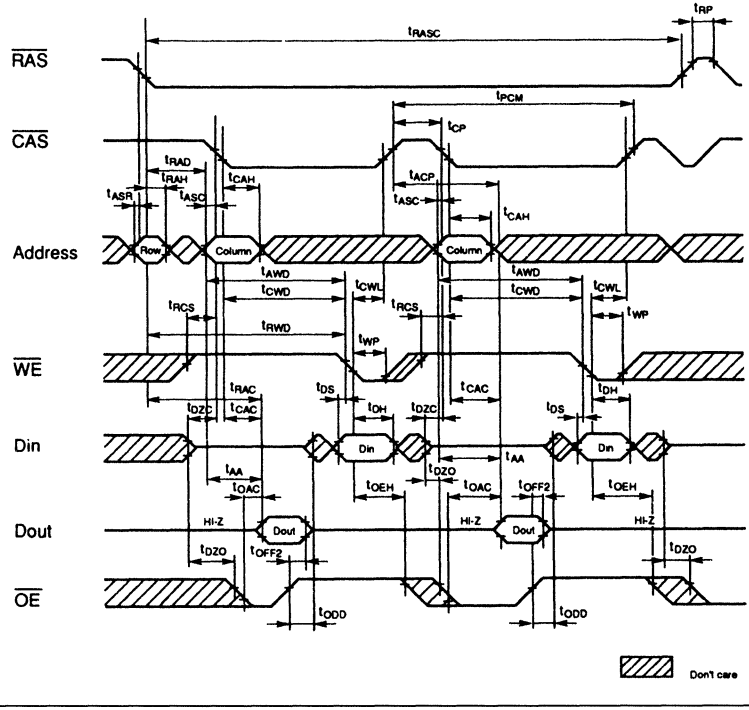
• Fast Page Mode Early Write Cycle



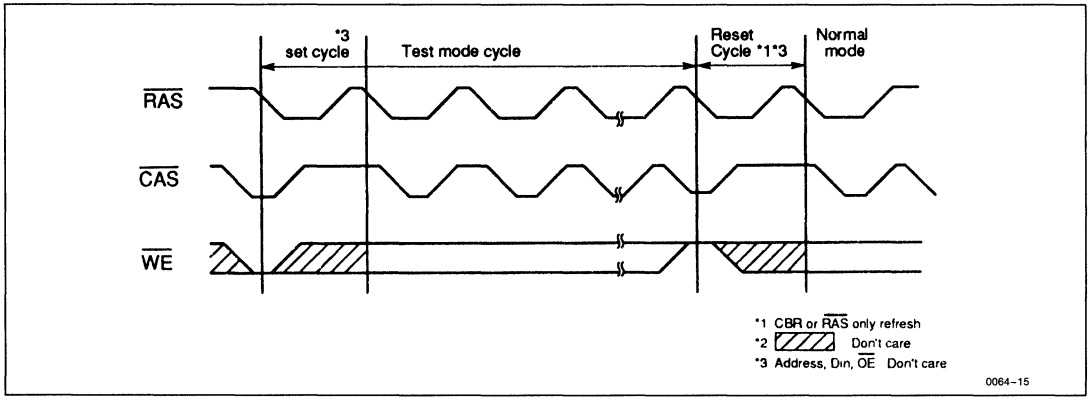
• Fast Page Delayed Cycle



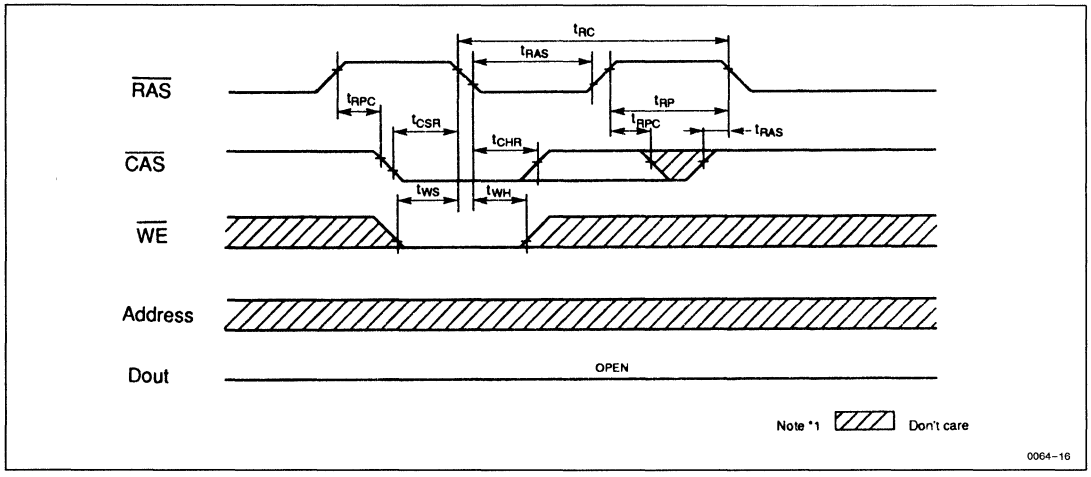
• Fast Page Mode Read-Modify-Write Cycle



• Test Mode Cycle

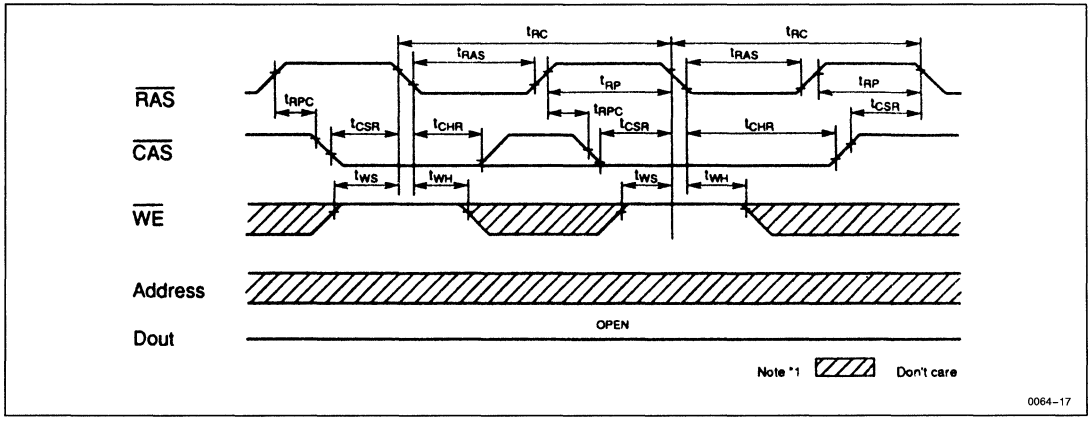


• Test Mode Set Cycle

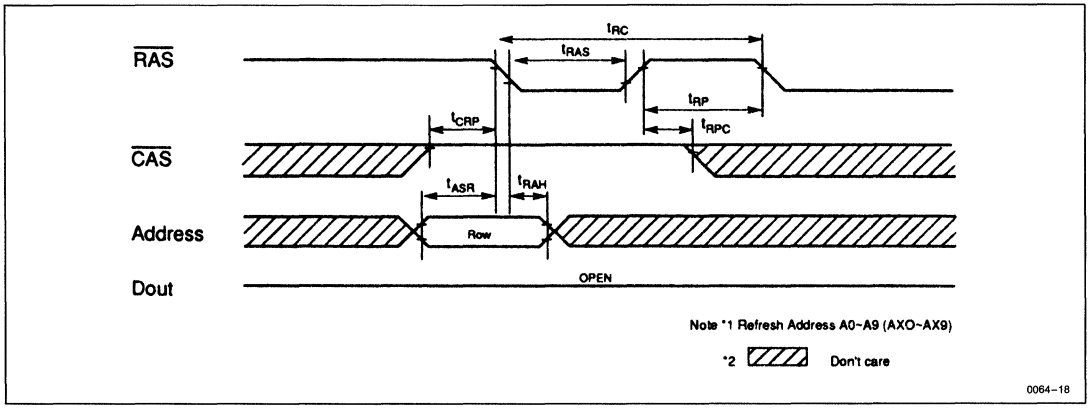


• Test Mode Reset Cycle

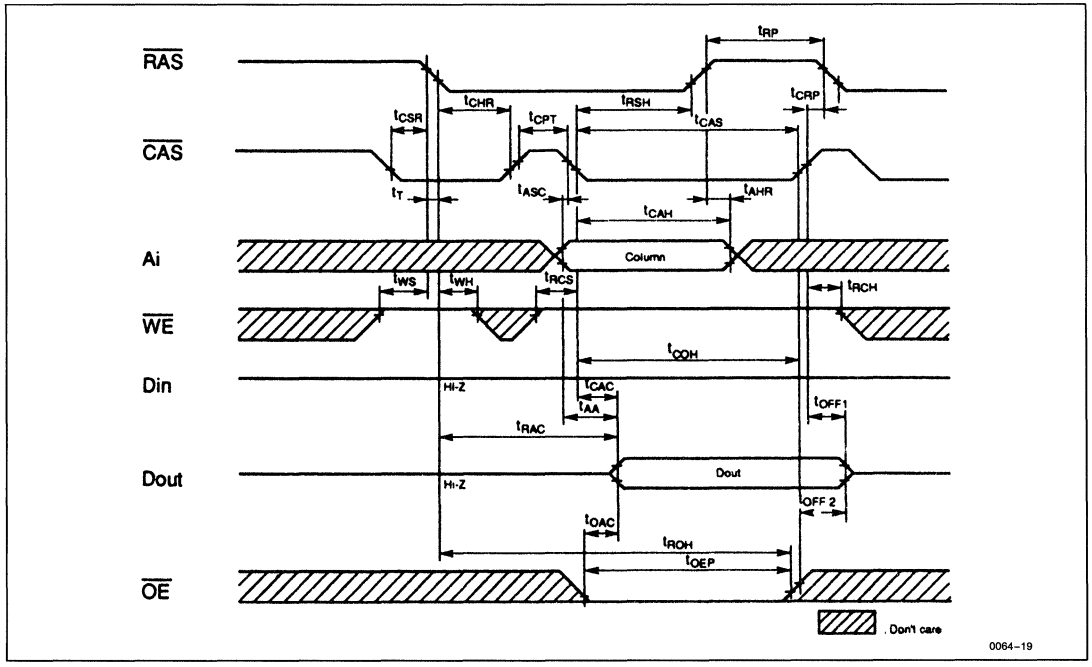
CAS Before RAS Refresh Cycle



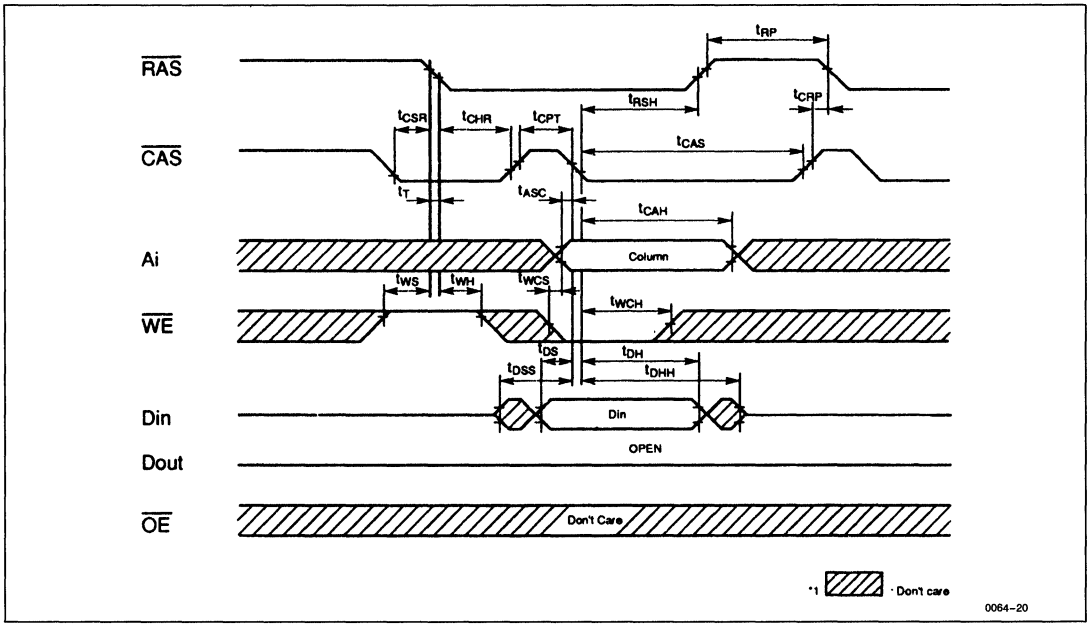
• $\overline{RAS}$ Only Refresh Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (READ)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (WRITE)



■ 4M DRAM LOW POWER VERSION

The specification on the low power version is the same as the standard 4 megabit DRAM with the exception of the following parameters.

Item	Conditions	Specifications
Type No.	4M x 1	HM514100LJP/LZP
	1M x 4	
Temperature	—	0–55°C
I_{CC2} (Standby CMOS Interface)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ ≥ V_{CC} − 0.2V Other Pin ≥ V_{CC} − 0.2V or ≤ 0.2V (Address and D_{in} is Stable) D_{out}: High-Z	200 μA max
I_{CC10} (Standby with CBR Refresh)	t_{RC} = 125 μs, t_{RAS} ≤ 1 μs V_{IL1} ≥ V_{CC} − 0.2V, V_{IL} ≤ 0.2V $\overline{WE}$ and $\overline{OE}$ = V_{IH}, Address and D_{in} is Stable D_{out}: High-Z	300 μA max
Refresh t_{REF}	—	128 ms

HM514400L Series Low Power Version

1,048,576-Word x 4-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514400 is a CMOS dynamic RAM organized 1,048,576 word x 4-bit. HM514400 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514400 offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514400 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time ..... 80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode ..... 495 mW/440 mW/385 mW (max)
  - Standby Mode ..... 11 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles ..... (128 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Test Function
- Battery Back Up Operation

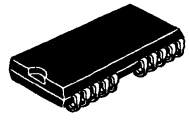
■ ORDERING INFORMATION

Part No.	Access	Package
HM514400LJP-8	80 ns	350 mil 20-pin
HM514400LJP-10	100 ns	Plastic SOJ
HM514400LJP-12	120 ns	(CP-20DA)
HM514400LZP-8	80 ns	400 mil 20-pin
HM514400LZP-10	100 ns	Plastic ZIP
HM514400LZP-12	120 ns	(ZP-20)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_9	Refresh Address Input
I/O_1–I/O_4	Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

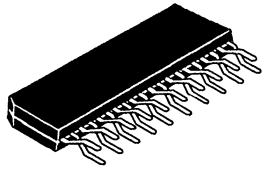
HM514400LJP Series



3DCP20DA

(CP-20DA)

HM514400LZP Series

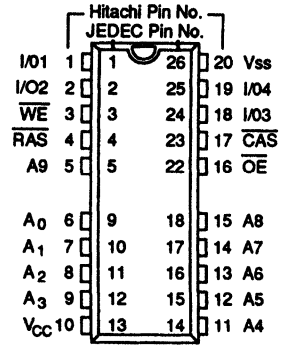


3DZP20

(ZP-20)

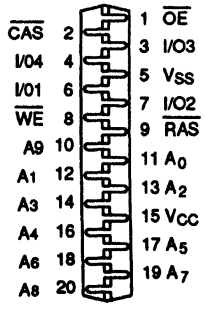
■ PIN OUT

HM514400LJP Series



(Top View)

HM514400LZP Series



(Bottom View)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	− 1.0	—	0.8	V	1
	(Others)	V_{IL}	− 2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	70	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	200	—	200	—	200	μA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ ≥ V_{CC} − 0.2V or ≤ 0.2V, Address and D_{in}: Stable, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	90	—	80	—	70	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	90	—	80	—	70	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	90	—	80	—	70	mA	t_{PC} = Min	1, 3
Battery Back Up Operating Current (Standby with CBR Refresh)	I_{CC10}	—	300	—	300	—	300	μA	t_{RC} = 125 μs, t_{RAS} ≤ 1 μs V_{CC} − 0.2V ≤ V_{IH} ≤ 6.5V, 0V ≤ V_{IL} ≤ 0.2V, $\overline{WE}$ and $\overline{OE}$ = V_{IH}, Address and D_{in}: Stable, D_{out} = High-Z	
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 14, 15, 16]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	150	—	180	—	210	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	20	—	25	—	30	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	ns	
CAS Setup Time from D_{in}	t_{DZC}	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	128	—	128	—	128	ms	

Read Cycle

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3, 17
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4, 13, 17
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5, 13, 16, 17
Access Time from $\overline{OE}$	t_{OAC}	—	25	—	25	—	30	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	18
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	18
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	20	0	25	0	30	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	20	0	25	0	30	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	20	—	25	—	30	—	ns	

Write Cycle

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	20	—	25	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	210	—	245	—	285	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	110	—	135	—	160	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	55	—	60	—	70	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	70	—	80	—	95	—	ns	10
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	25	—	25	—	30	—	ns	

Refresh Cycle

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	13, 17
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	105	—	110	—	130	—	ns	

Test Mode Cycle

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	20	—	20	—	20	—	ns	

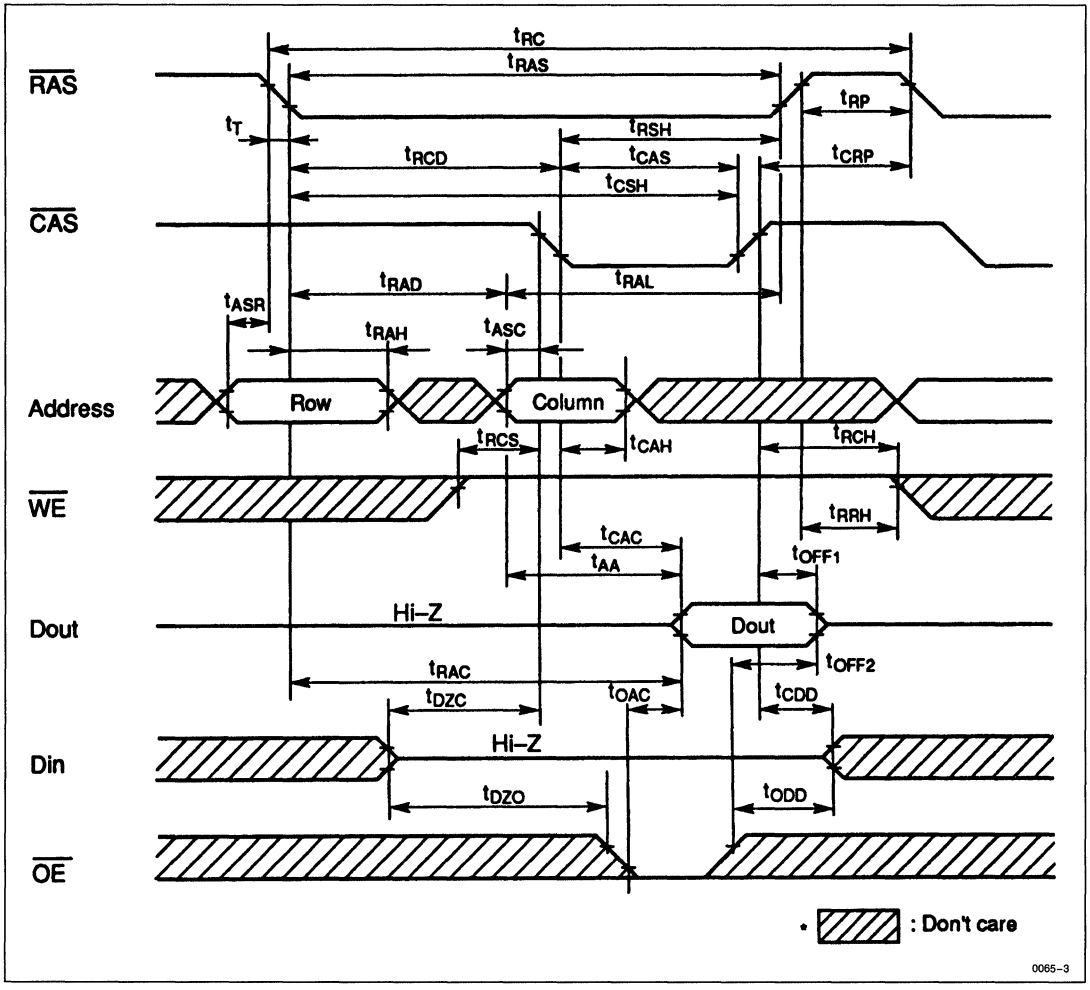
Counter Test Cycle

Parameter	Symbol	HM514400-8		HM514400-10		HM514400-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	50	—	60	—	ns	

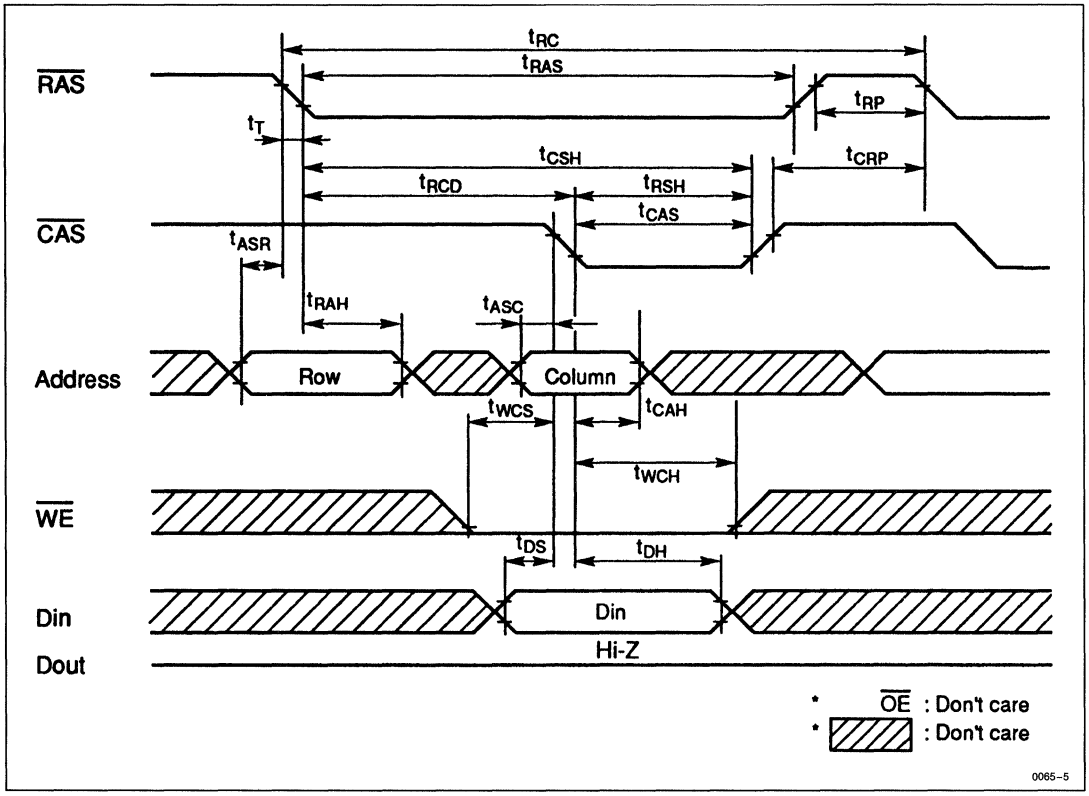
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits—CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is I/O_3 and data input pin is I/O_2. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{OAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORMS

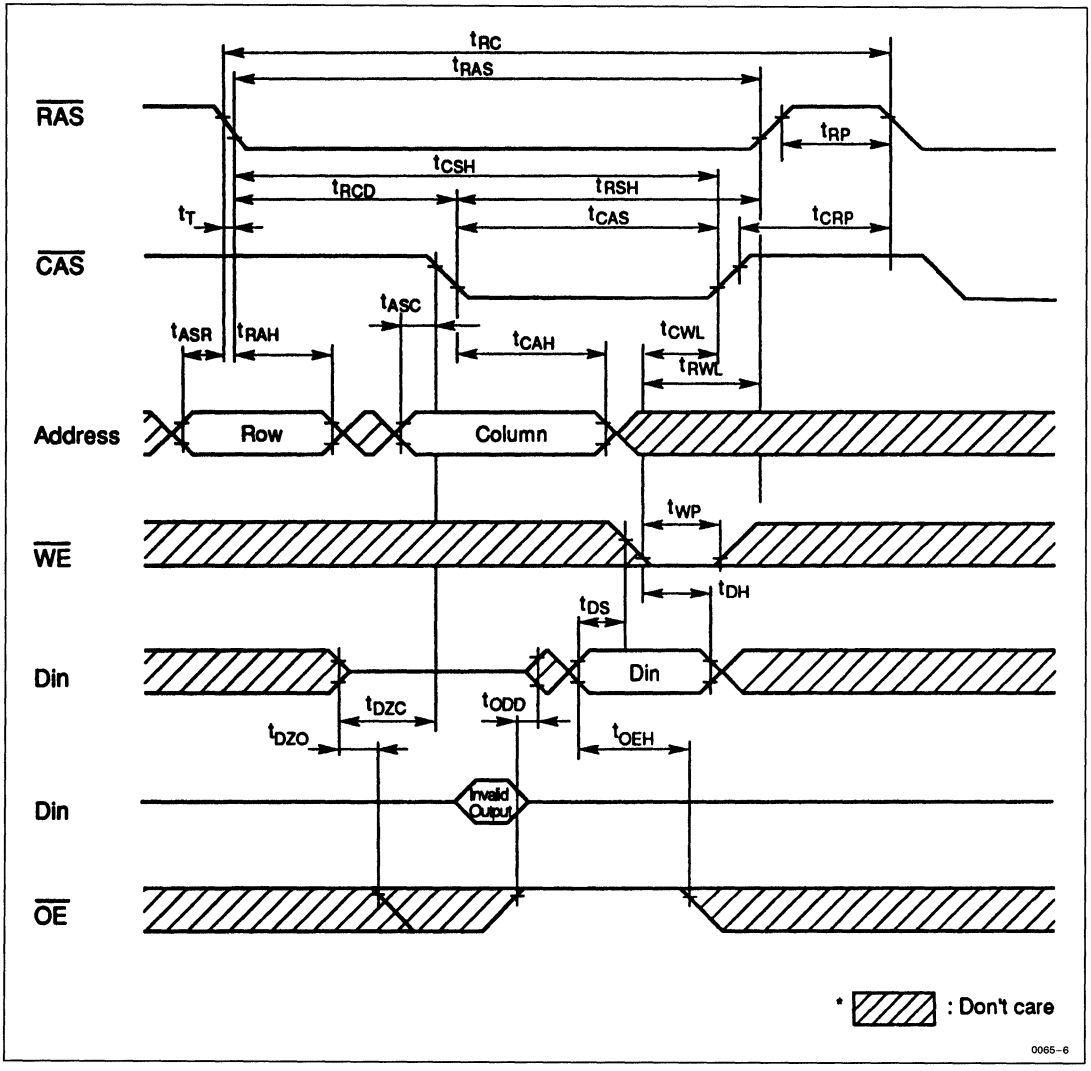
• Read Cycle (1)



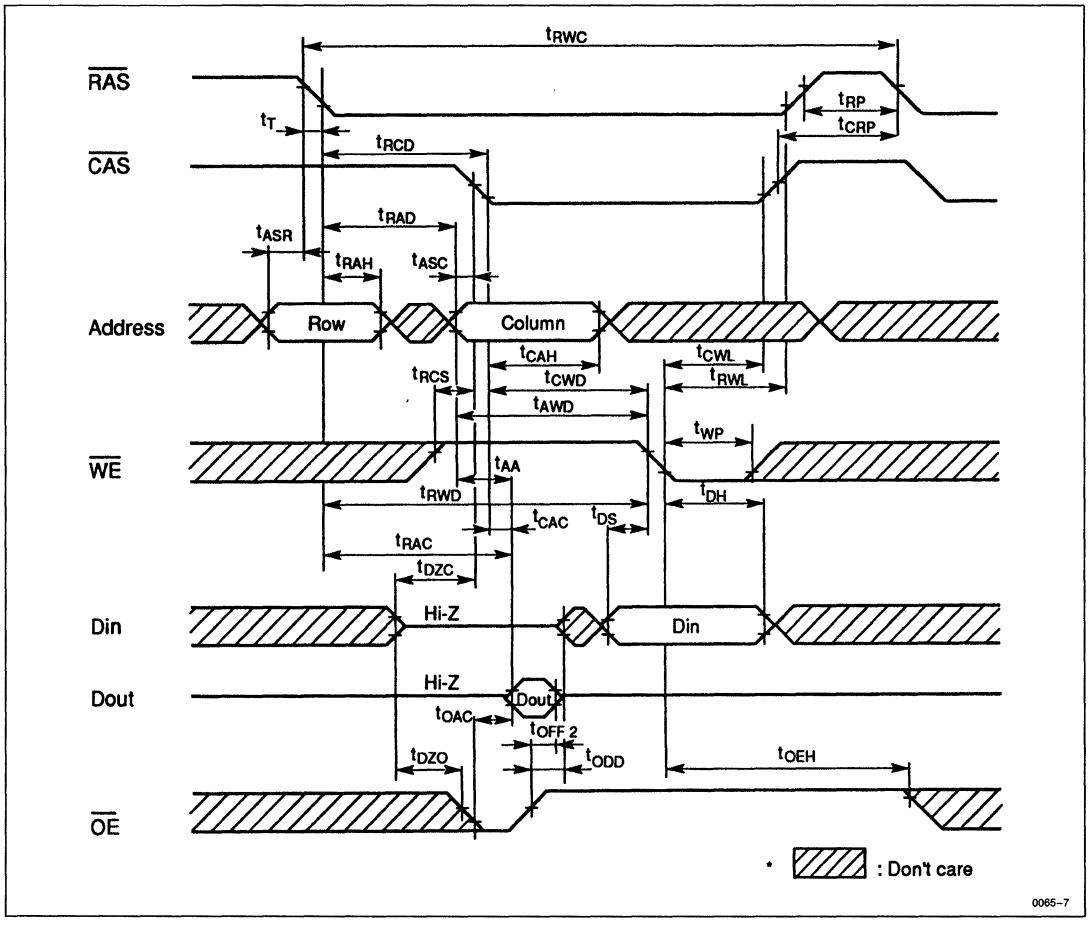
• **Early Write Cycle (2)**



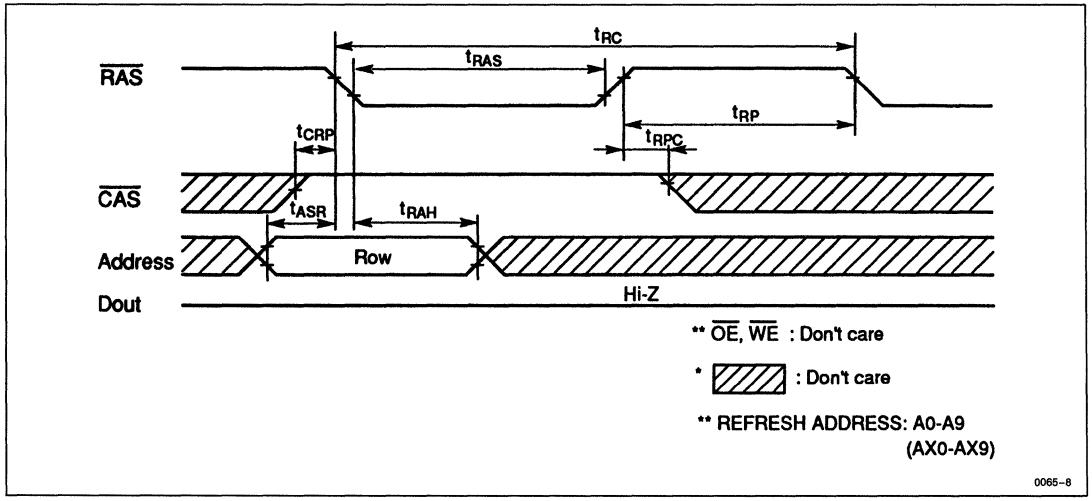
• **Delayed Write Cycle (3)**



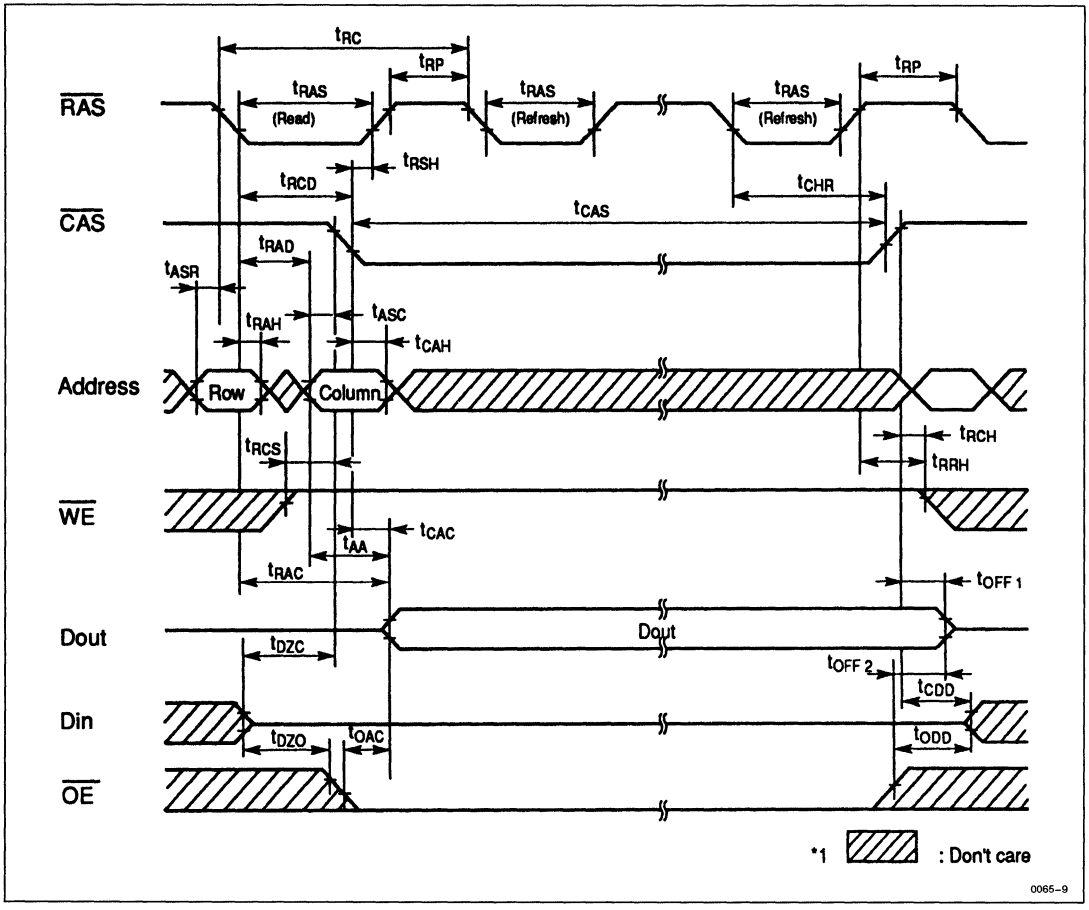
• **Read-Modify-Write Cycle (4)**



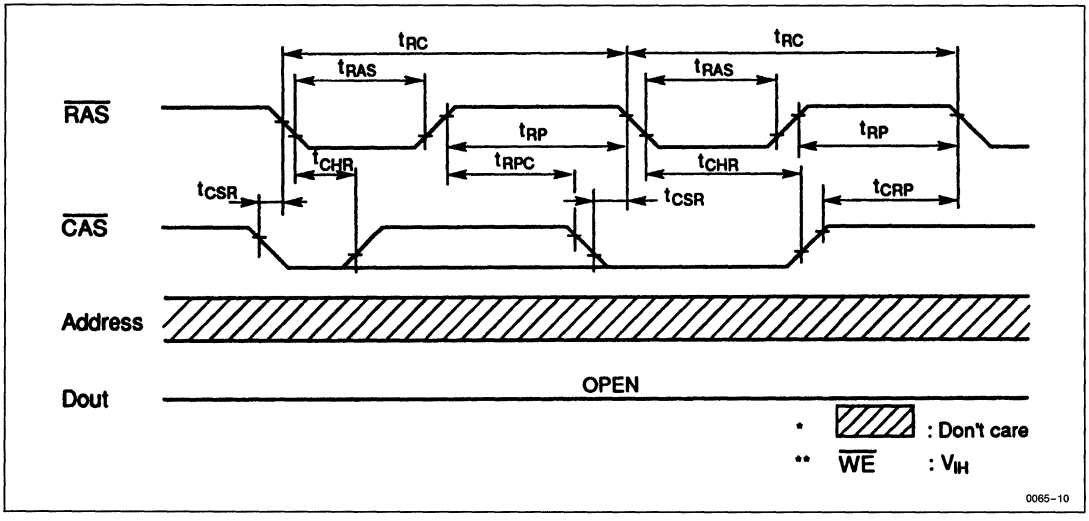
• **$\overline{RAS}$ Only Refresh Cycle (5)**



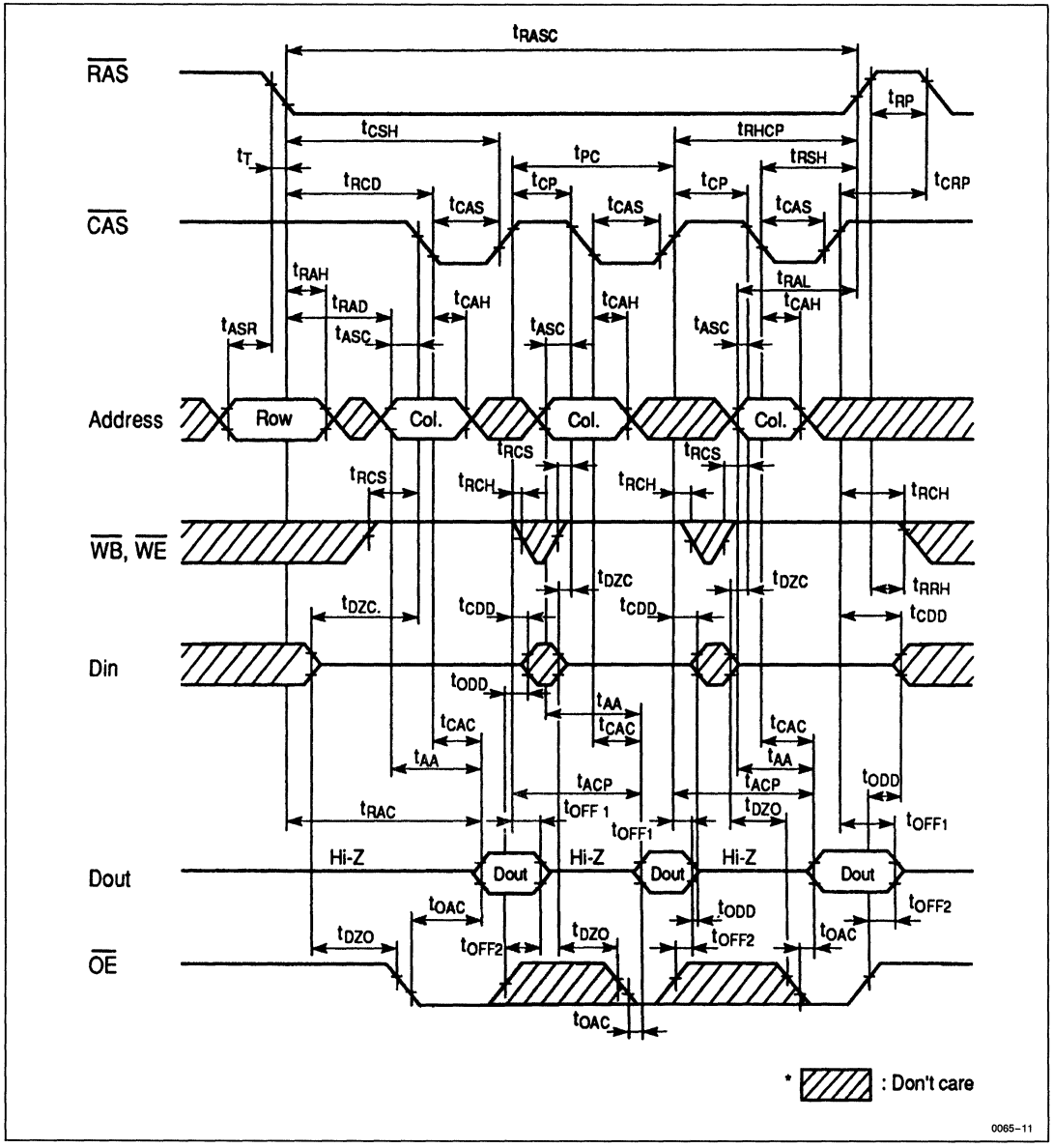
• **Hidden Refresh Cycle (6)**



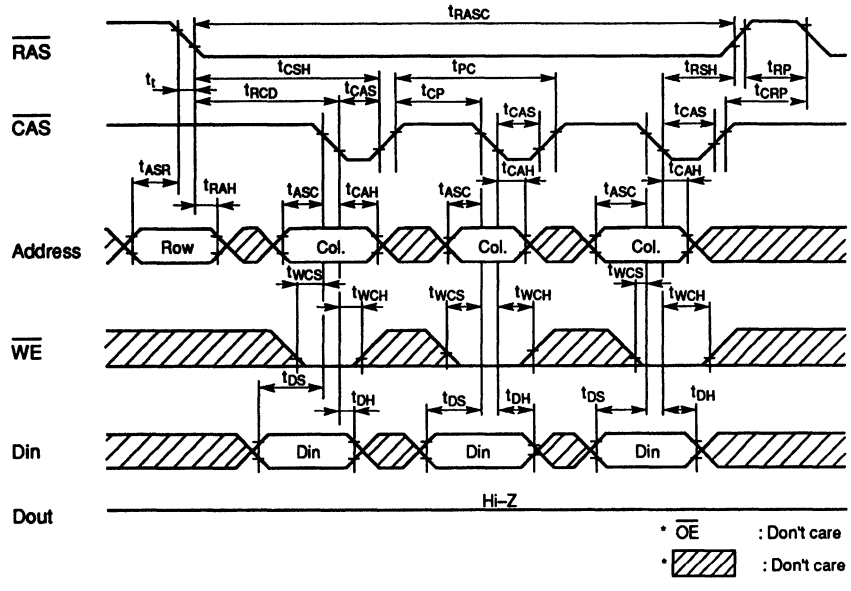
• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle (7)**



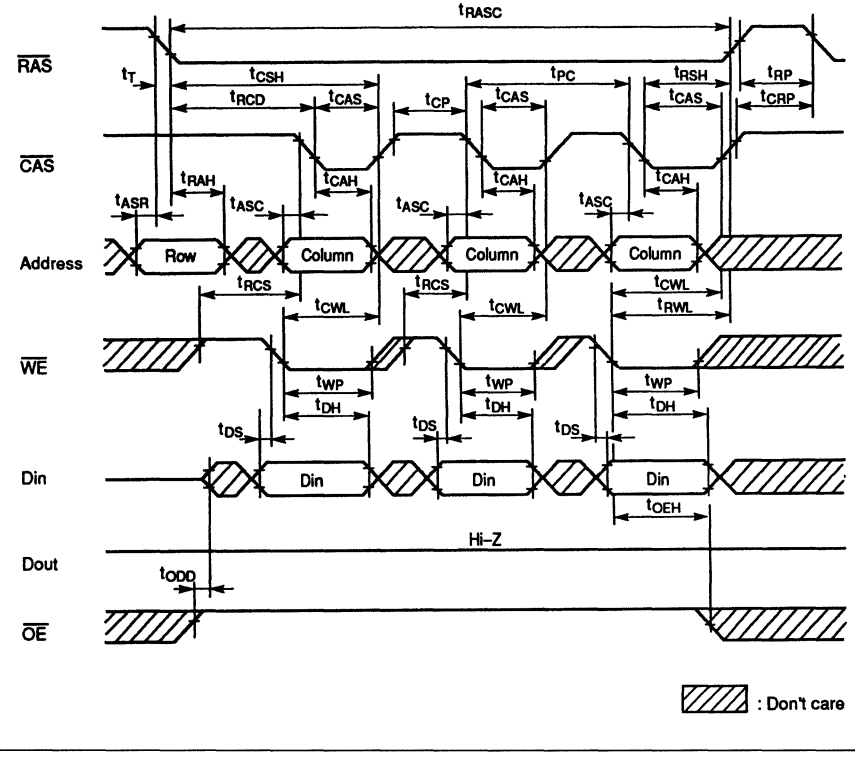
• **Fast Page Mode Read Cycle (8)**



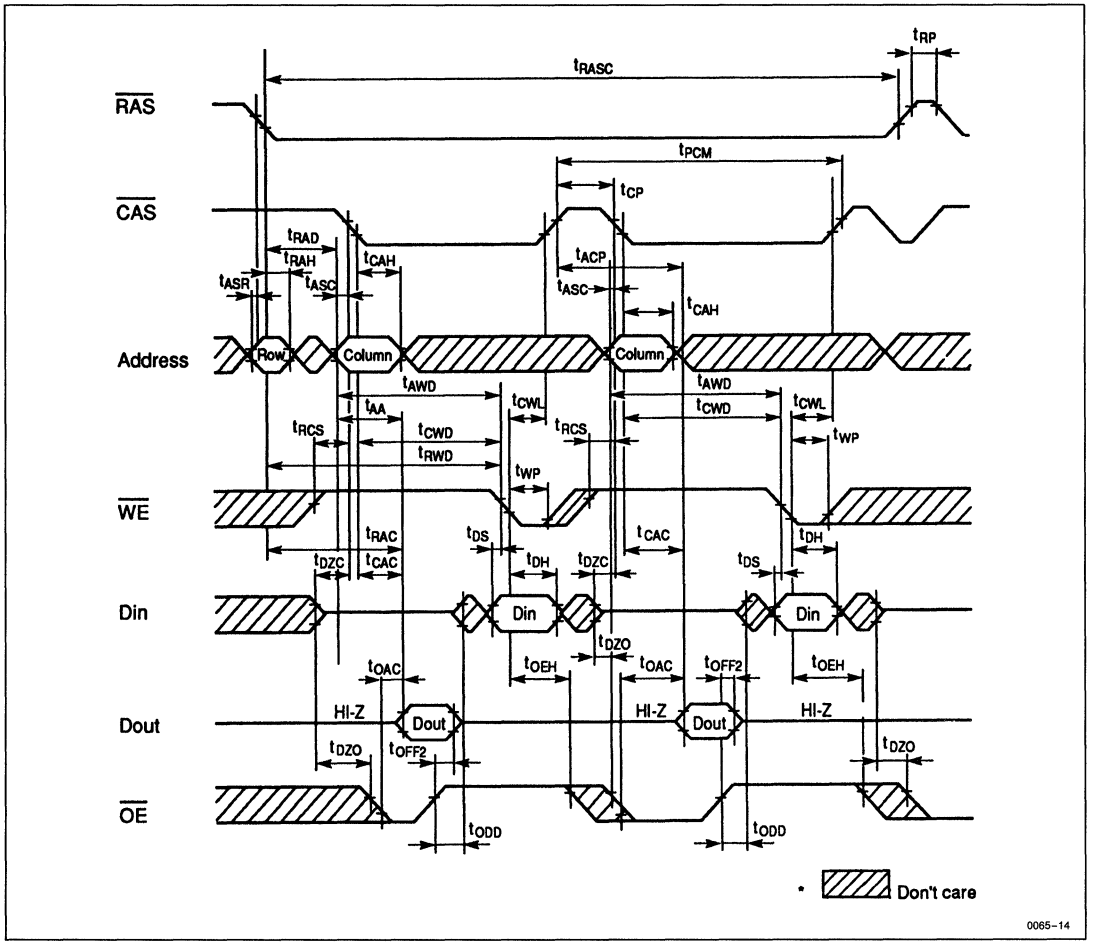
• **Fast Page Mode Early Write Cycle (9)**



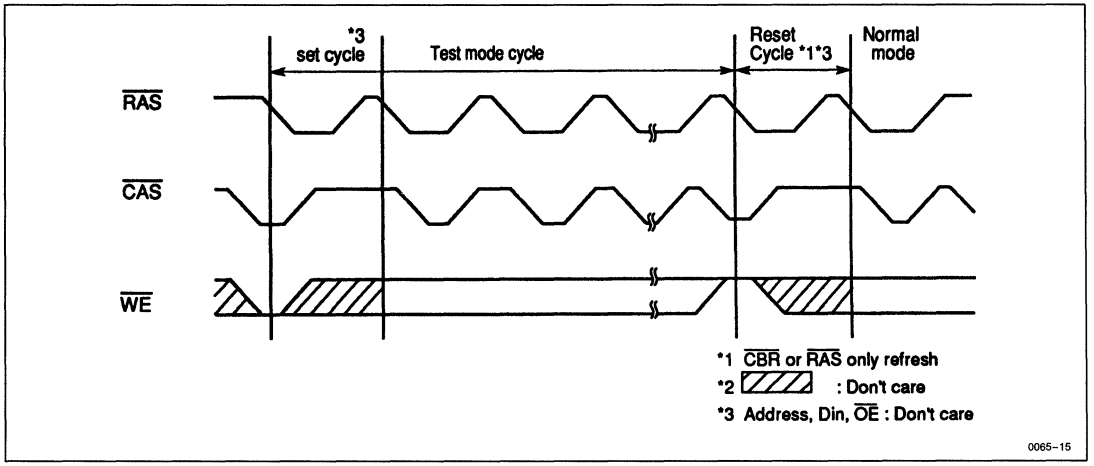
• **Fast Page Delayed Write Cycle (10)**



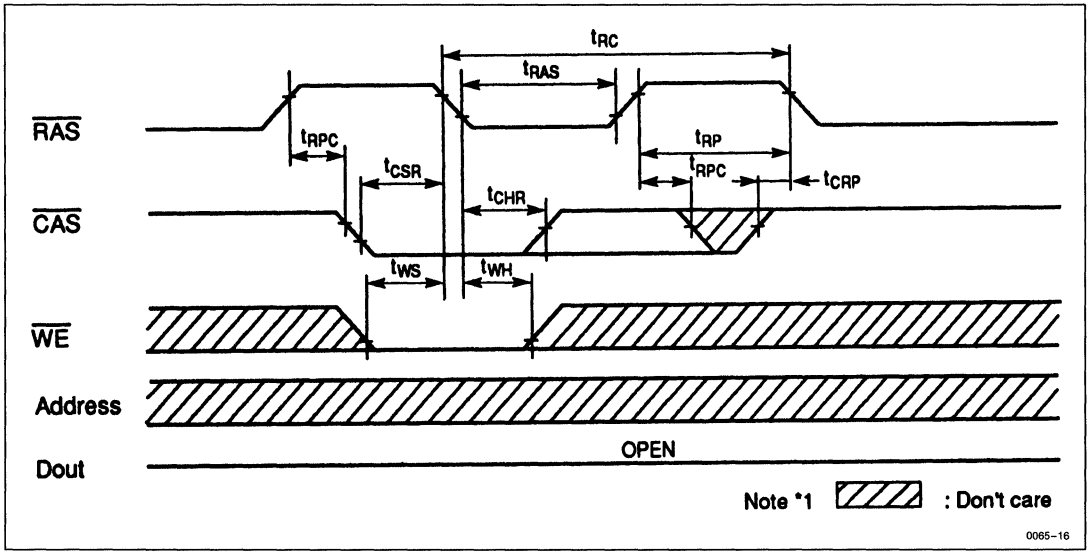
• Fast Page Mode Read-Modify-Write Cycle (11)



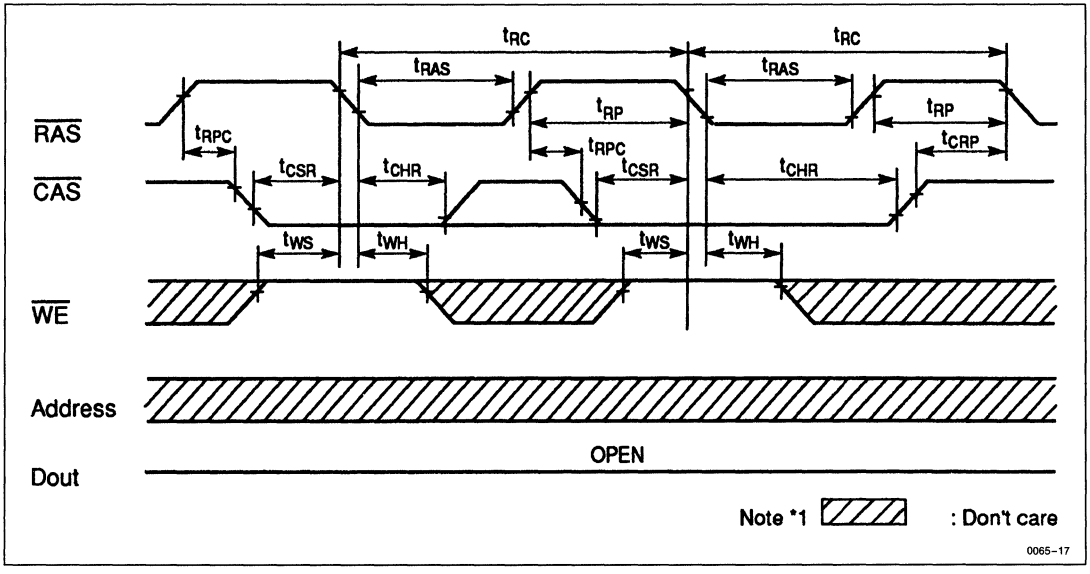
• Test Mode Cycle



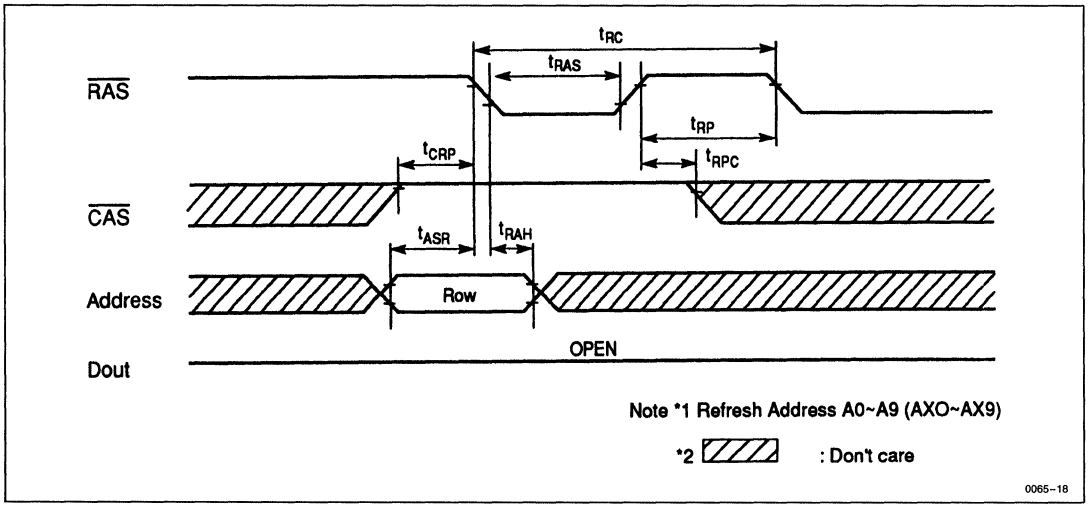
• **Test Mode Set Cycle (1)**



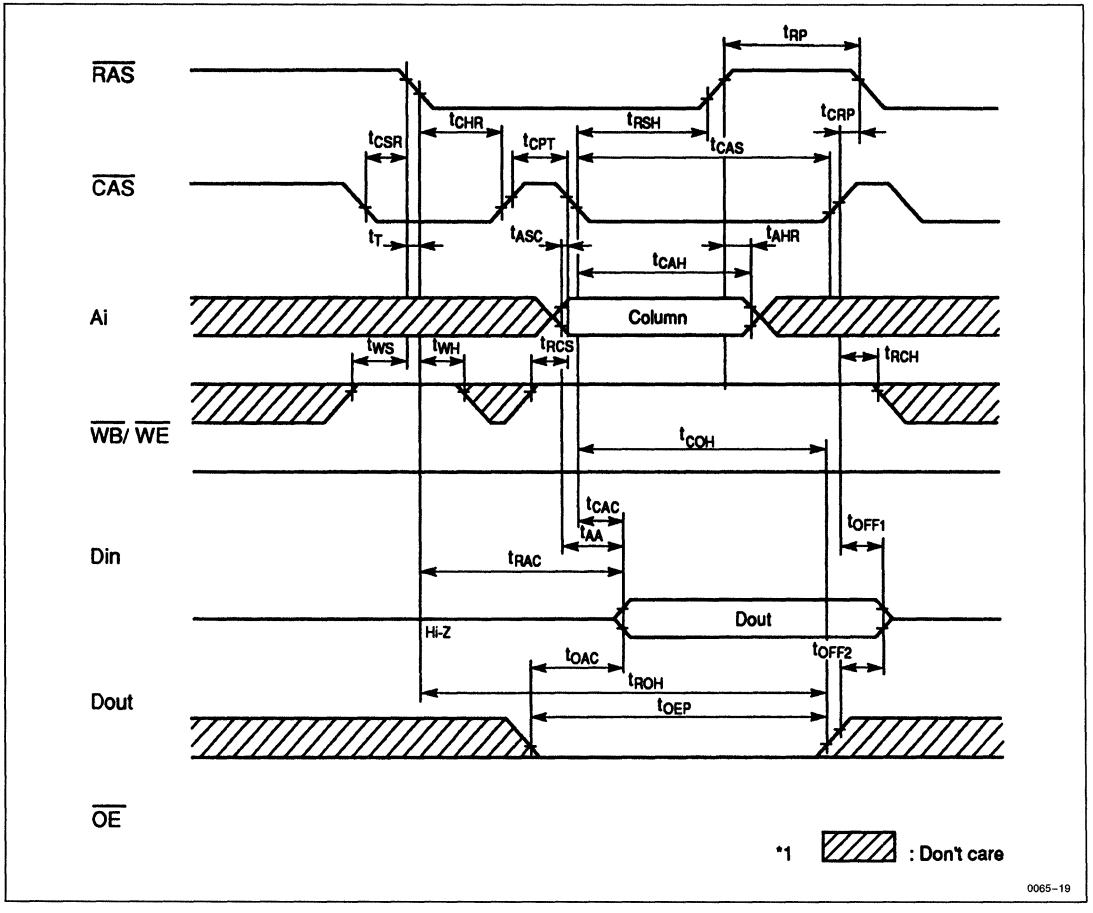
• **Test Mode Reset Cycle (2)**



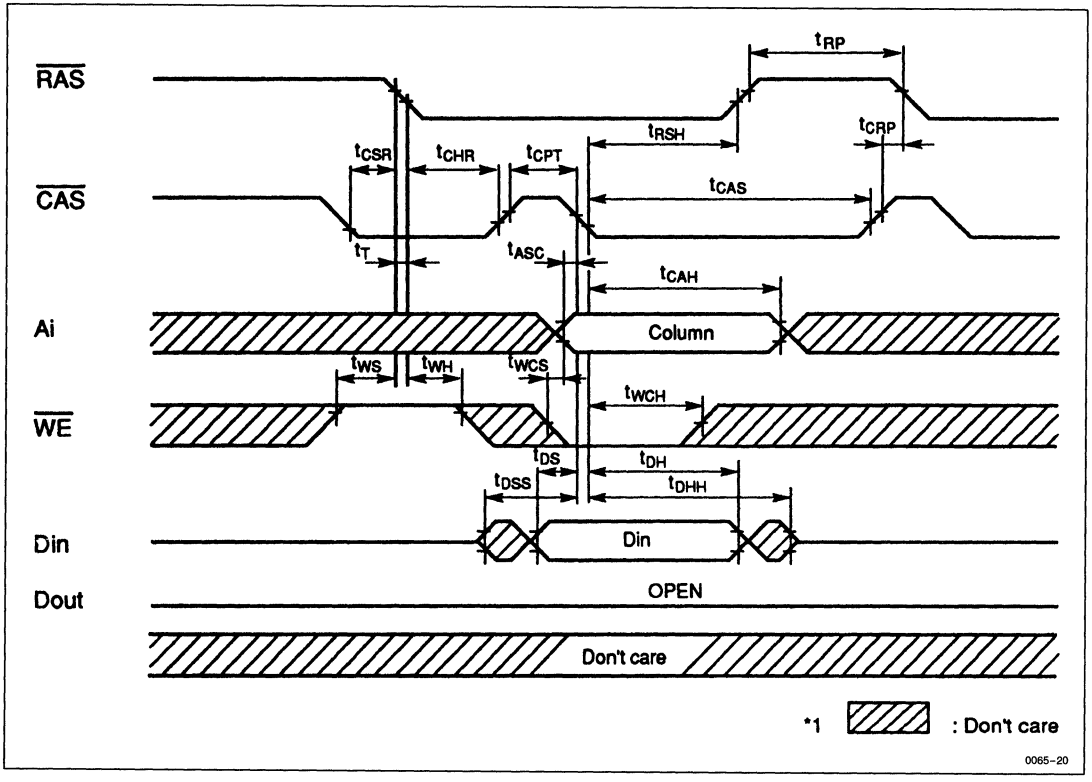
• $\overline{RAS}$ Only Refresh Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle, (READ)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle, (WRITE)



HM514410 Series — Preliminary

1,048,576-Word x 4-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514410 is a CMOS dynamic RAM organized 1,048,576 word x 4-bit. HM514410 has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514410 offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514410 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time ..... 80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode ..... 495 mW/440 mW/385 mW (max)
  - Standby Mode ..... 11 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles ..... (16 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Test Function
- Write per Bit Capability

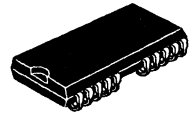
■ ORDERING INFORMATION

Part No.	Access Time	Package
HM514410JP-8	80 ns	350 mil 20-pin
HM514410JP-10	100 ns	Plastic SOJ
HM514410JP-12	120 ns	(CP-20DA)
HM514410ZP-8	80 ns	400 mil 20-pin
HM514410ZP-10	100 ns	Plastic ZIP
HM514410ZP-12	120 ns	(ZP-20)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_9	Refresh Address Input
W_1/IO_1–W_4/IO_4	Write Select/Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB}/\overline{WE}$	Write per Bit/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

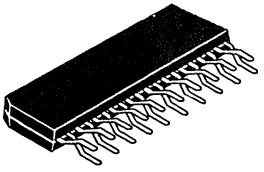
HM514410JP Series



3DCP20DA

(CP-20DA)

HM514410ZP Series

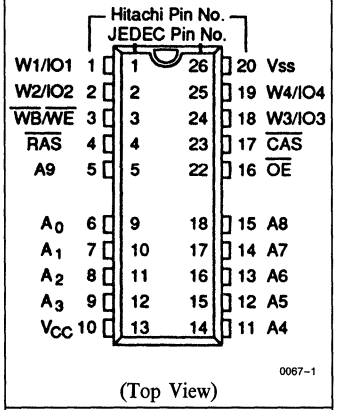


3DZP20

(ZP-20)

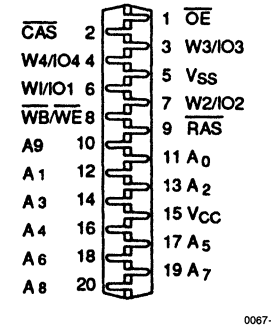
■ PIN OUT

HM514410JP Series



(Top View)

HM514410ZP Series



(Bottom View)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	− 1.0	—	0.8	V	1
	(Others)	V_{IL}	− 2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM514410-8		HM514410-10		HM514410-12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	70	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	1	—	1	—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	90	—	80	—	70	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	90	—	80	—	70	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	90	—	80	—	70	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• Capacitance (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• AC Characteristics (T_A = 0 to 70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 14, 15, 16]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514410-8		HM514410-10		HM514410-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	150	—	180	—	210	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	20	—	25	—	30	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514410-8		HM514410-10		HM514410-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3, 17
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4, 13, 17
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5, 13, 16, 17
Access Time from $\overline{OE}$	t_{OAC}	—	25	—	25	—	30	ns	17
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	20	0	25	0	30	ns	6
Output Buffer Turn-off Time to $\overline{OE}$	t_{OFF2}	0	20	0	25	0	30	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	20	—	25	—	30	—	ns	

Write Cycle

Parameter	Symbol	HM514410-8		HM514410-10		HM514410-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	20	—	25	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514410-8		HM514410-10		HM514410-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	210	—	245	—	285	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	110	—	135	—	160	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	55	—	60	—	70	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	70	—	80	—	95	—	ns	10
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	25	—	25	—	30	—	ns	

Refresh Cycle

Parameter	Symbol	HM514410-8		HM514410-10		HM514410-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Normal Mode)	t_{CPN}	10	—	10	—	15	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514410-8		HM514410-10		HM514410-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	13, 17
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	105	—	110	—	130	—	ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPW}	80	—	85	—	100	—	ns	

Test Mode Cycle

Parameter	Symbol	HM514410-8		HM514410-10		HM514410-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	20	—	20	—	20	—	ns	

Counter Test Cycle

Parameter	Symbol	HM514410-8		HM514410-10		HM514410-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	50	—	60	—	ns	

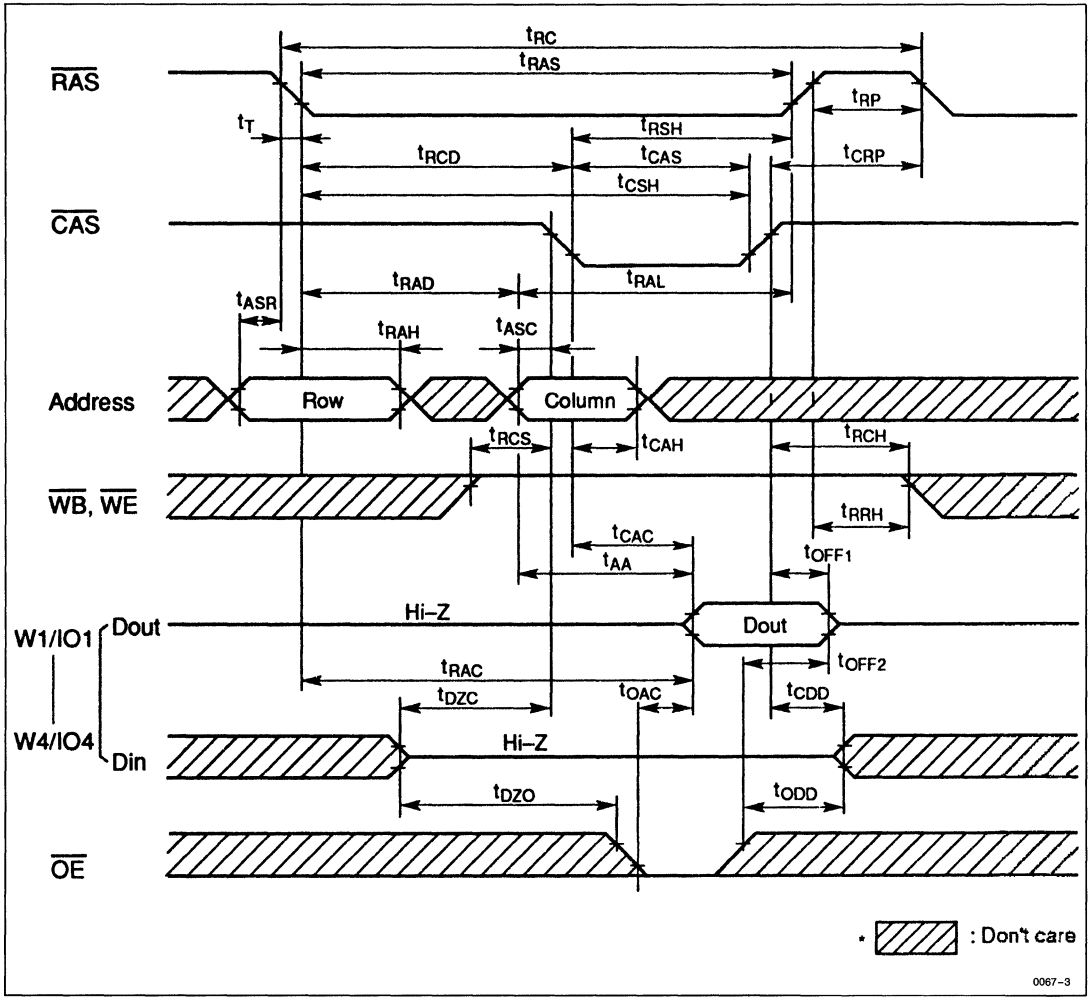
Write per Bit[18, 19]

Parameter	Symbol	HM514410-8		HM514410-10		HM514410-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write per Bit Setup Time	t_{WBS}	0	—	0	—	0	—	ns	
Write per Bit Hold Time	t_{WBH}	12	—	15	—	15	—	ns	
Write per Bit Selection Setup Time	t_{WDS}	0	—	0	—	0	—	ns	
Write per Bit Selection Hold Time	t_{WDH}	12	—	15	—	15	—	ns	

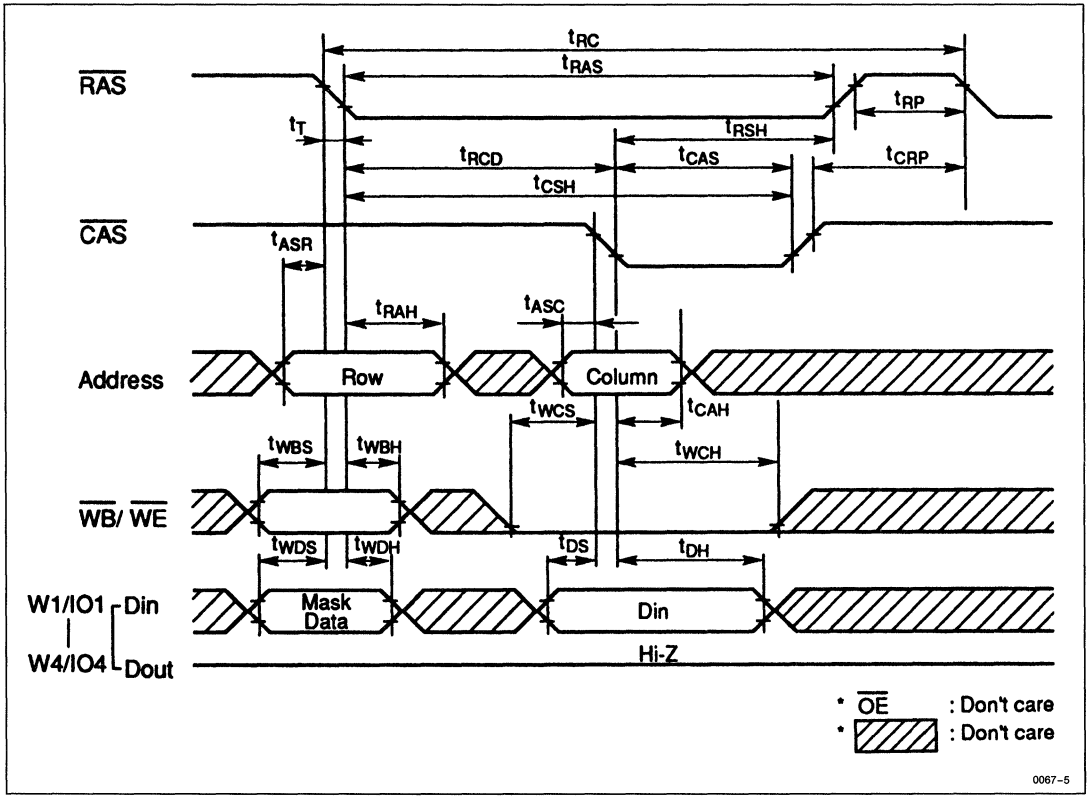
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle of $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits—CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is I/O_3 and data input pin is I/O_2. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of t_{RAC}, t_{CAC}, t_{AA}, t_{OAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
18. When using the write-per-bit capability, $\overline{WB}/\overline{WE}$ must be low as $\overline{RAS}$ falls.
19. The data bits to which the write operation is applied can be specified by keeping $W1/IO_1$, $W2/IO_2$, $W3/IO_3$ and $W4/IO_4$ high with setup and hold time referenced to the $\overline{RAS}$ negative transition.

■ TIMING WAVEFORMS

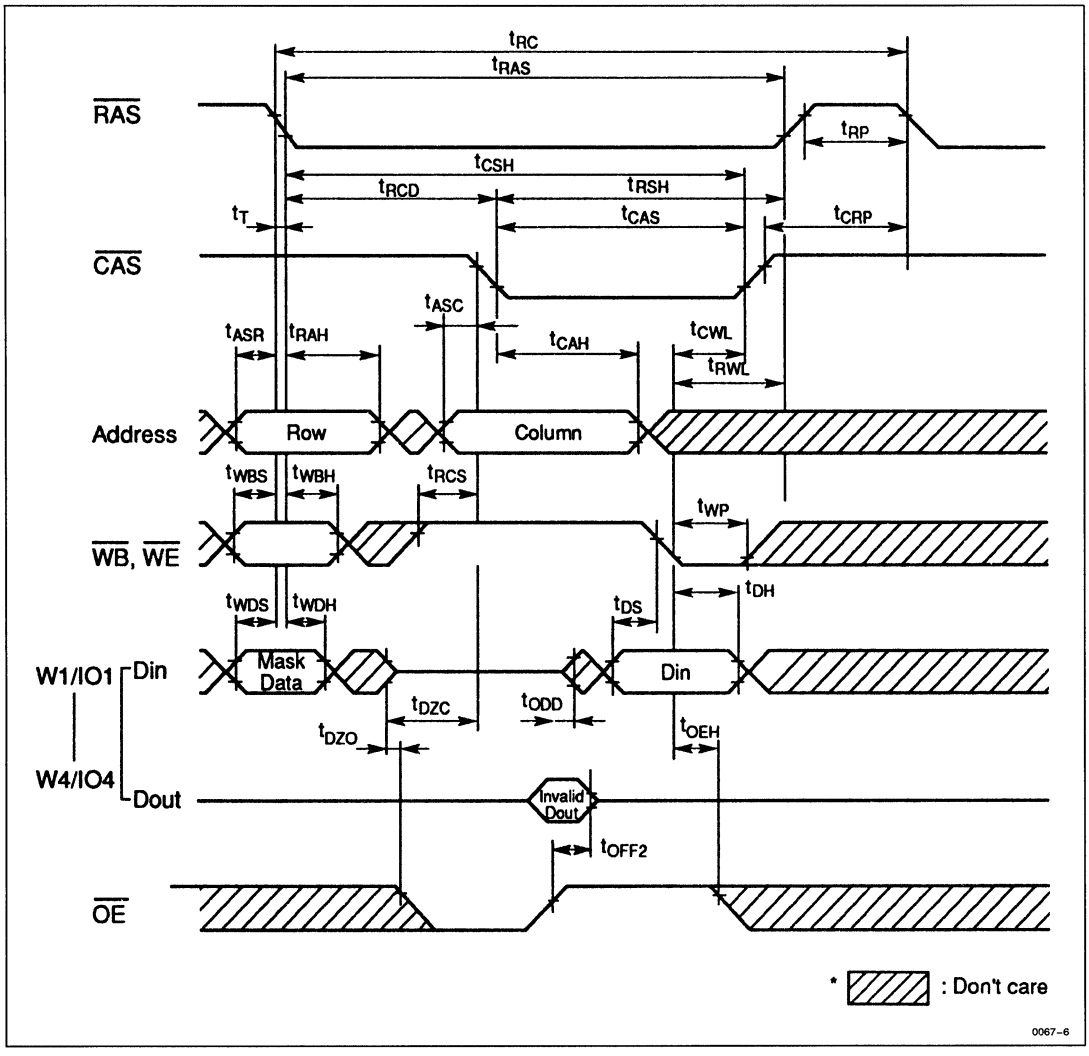
• Read Cycle (1)



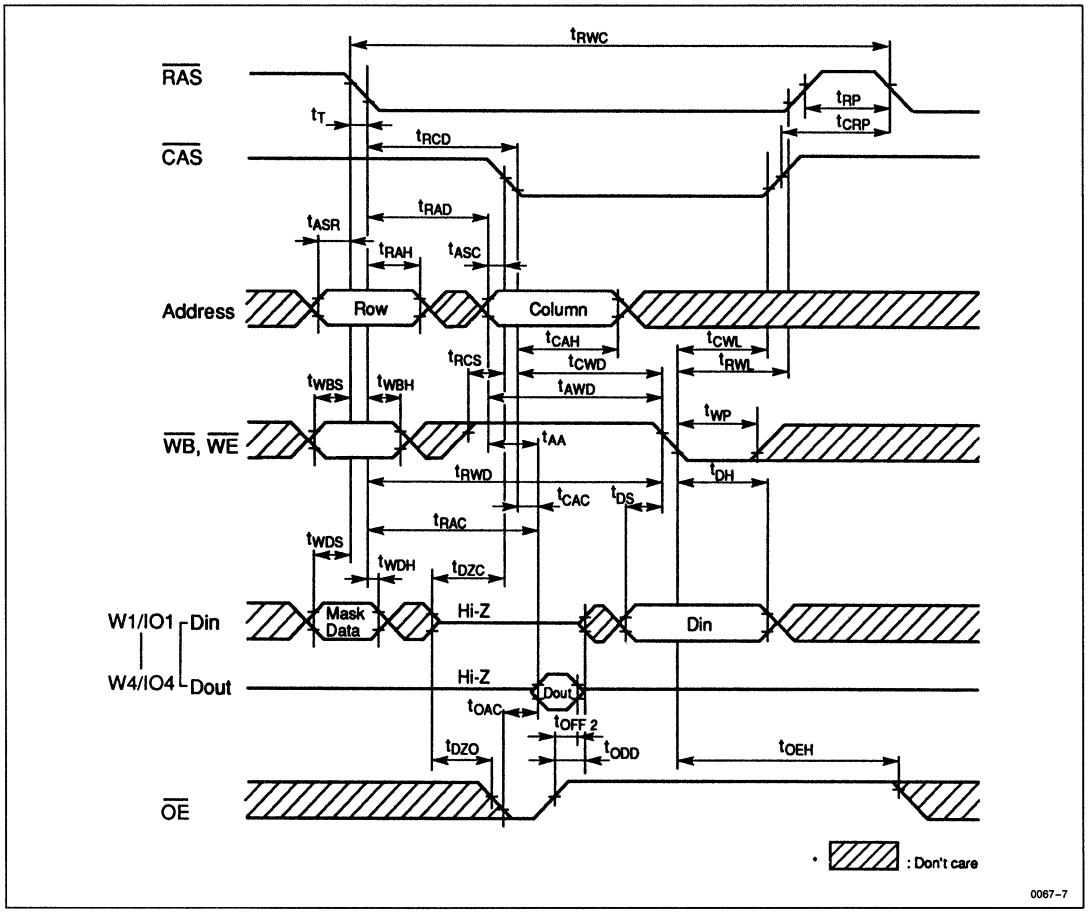
• Early Write Cycle (2)



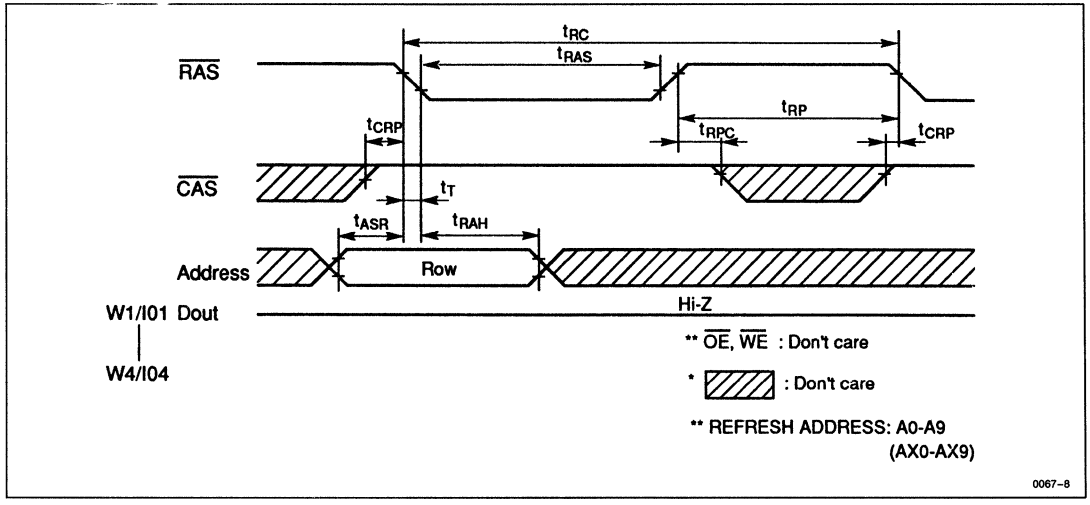
• **Delayed Write Cycle (3)**



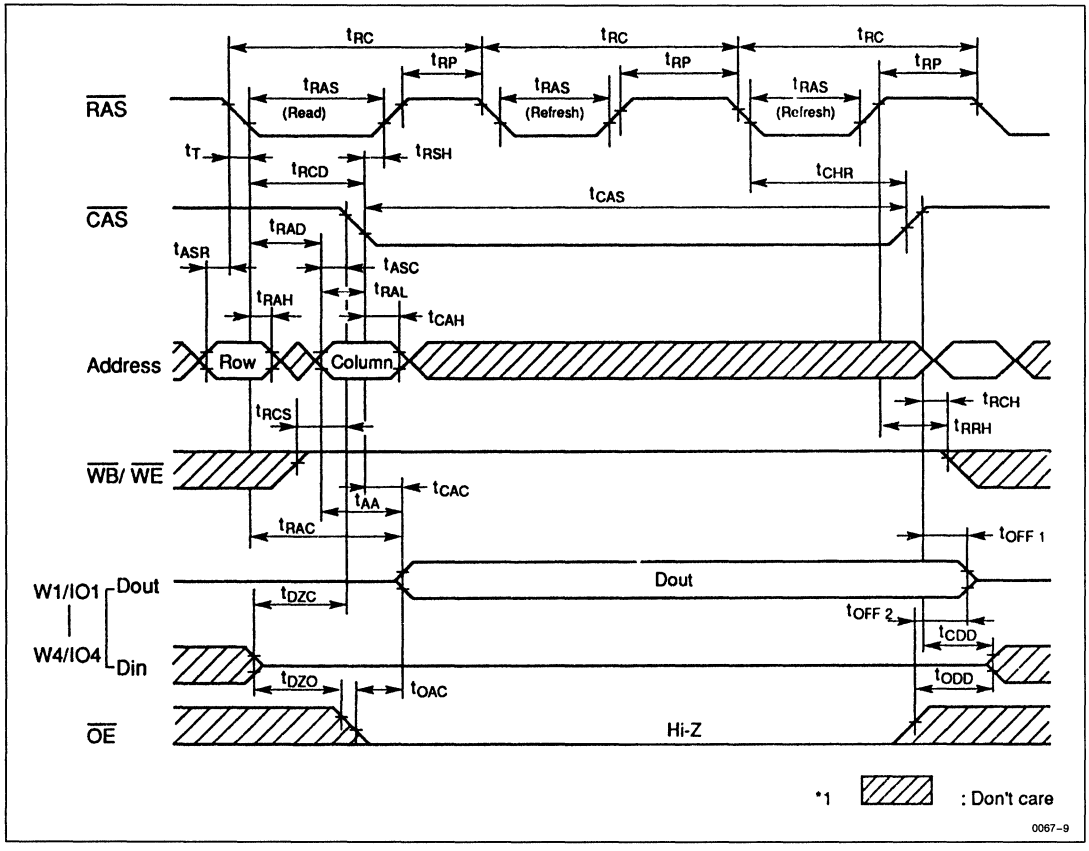
• **Read-Modify-Write Cycle (4)**



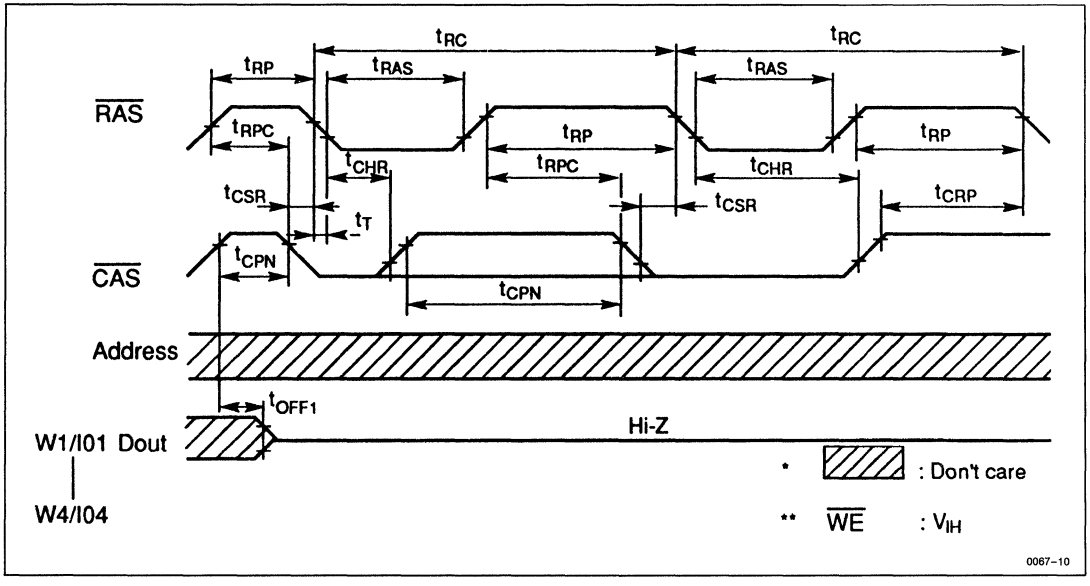
• **$\overline{RAS}$ Only Refresh Cycle (5)**



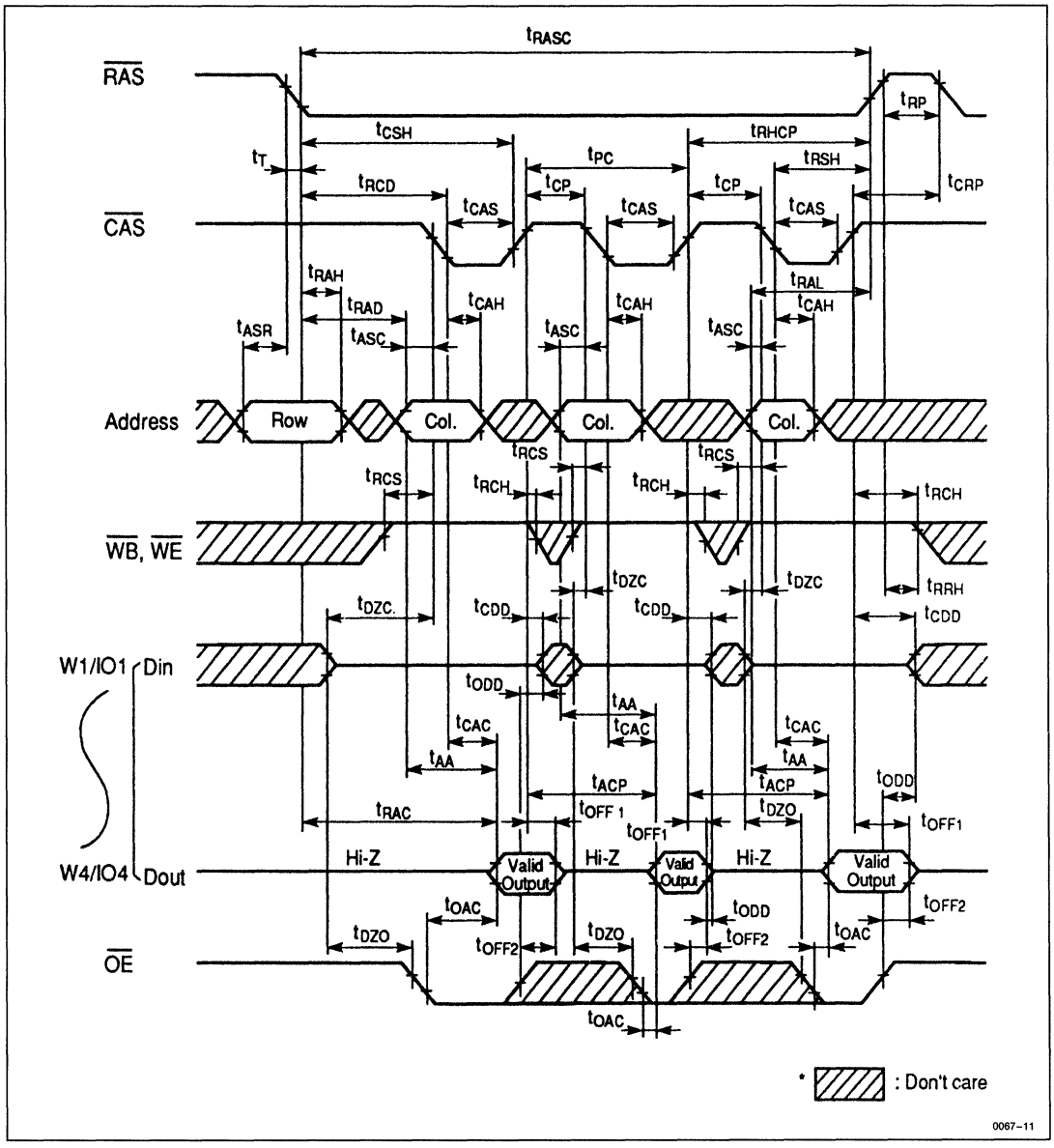
• **Hidden Refresh Cycle (6)**



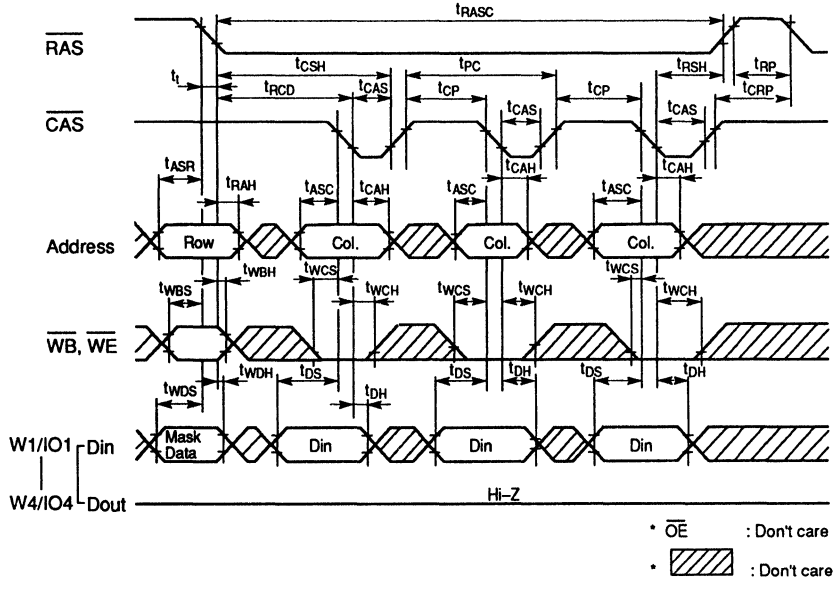
• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle (7)**



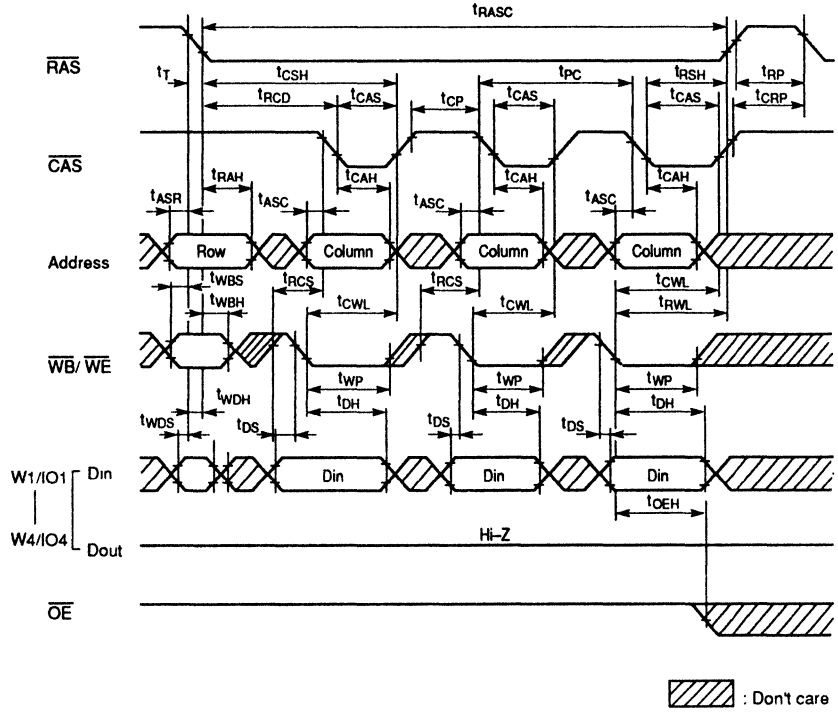
• Fast Page Mode Read Cycle (8)



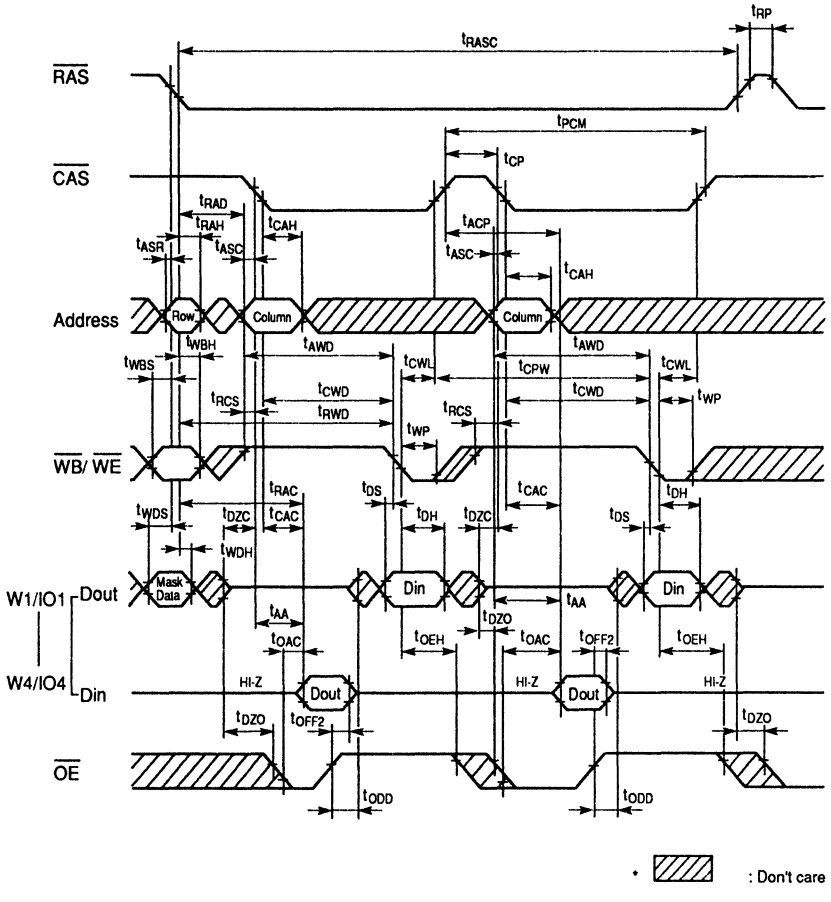
• **Fast Page Mode Early Write Cycle (9)**



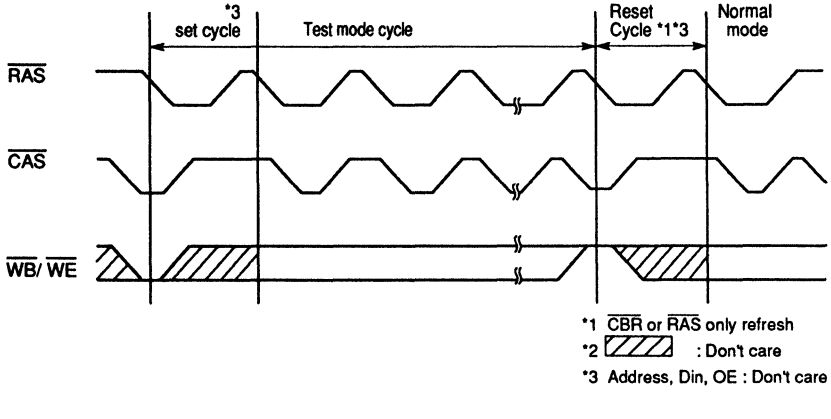
• **Fast Page Delayed Write Cycle (10)**



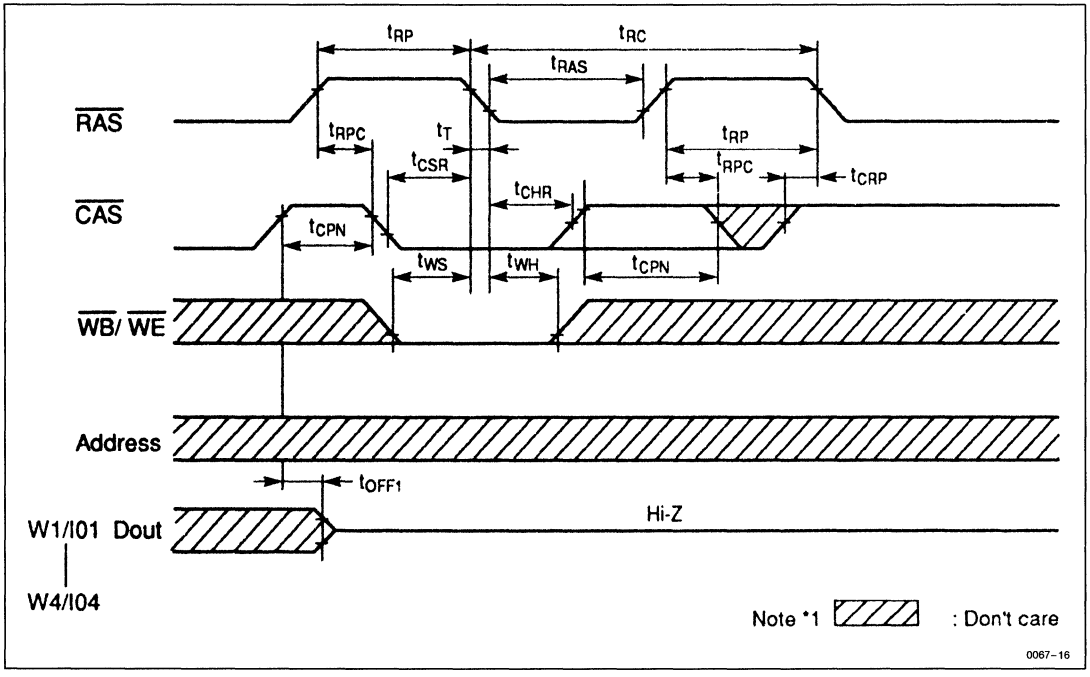
• Fast Page Mode Read-Modify-Write Cycle (11)



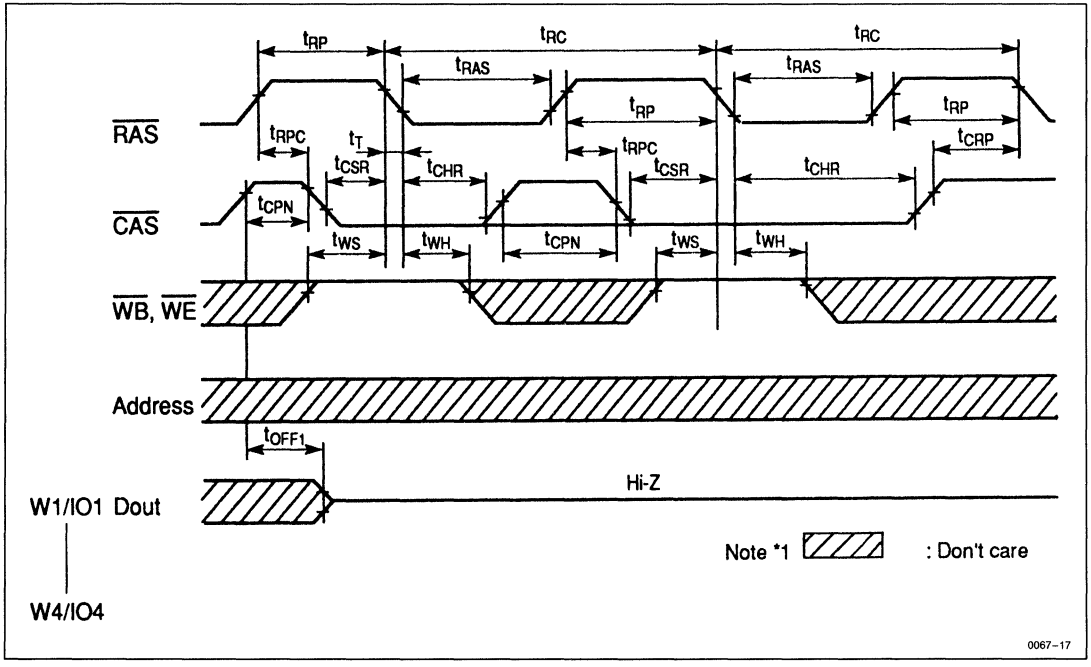
• Test Mode Cycle



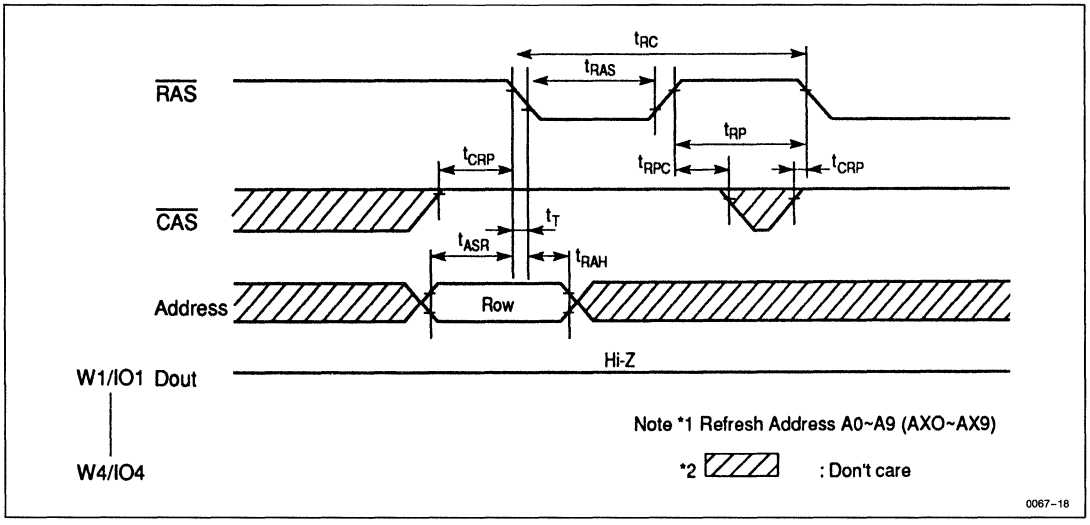
• **Test Mode Set Cycle (1)**



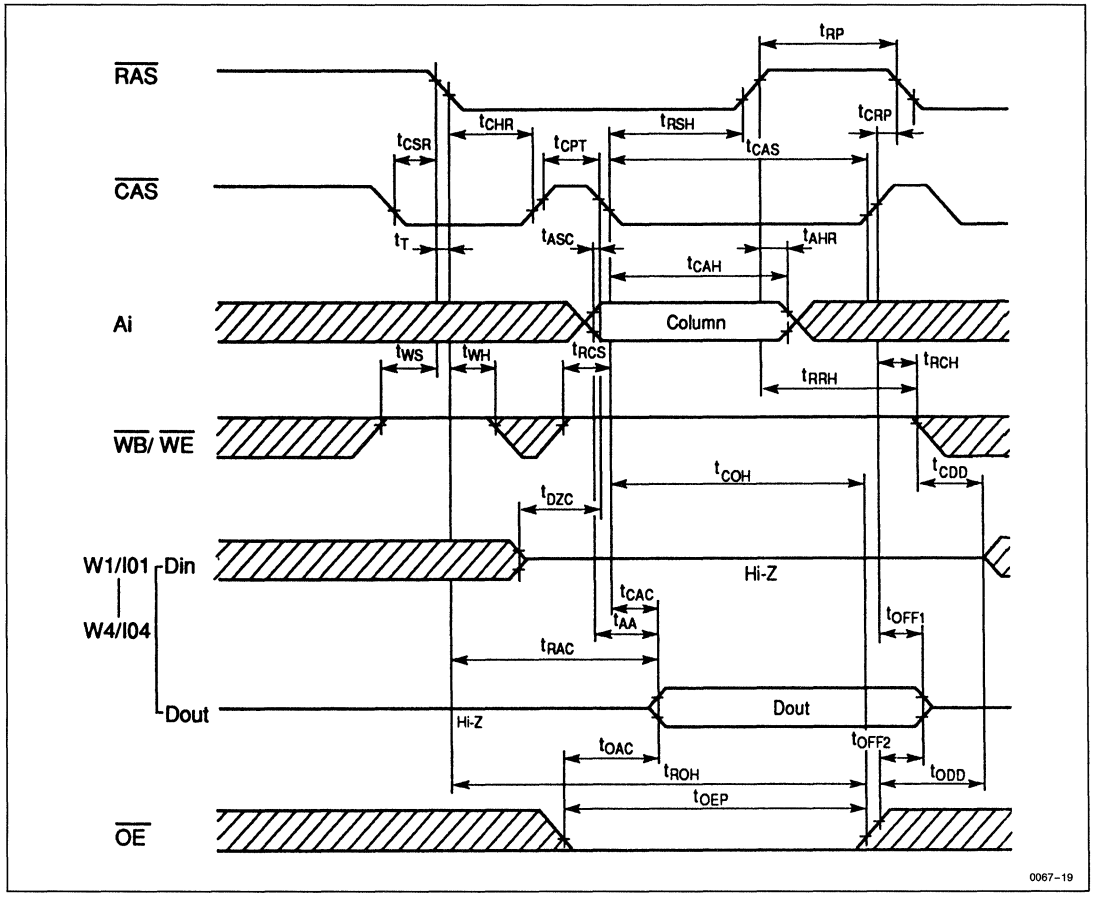
• **Test Mode Reset Cycle (2)**



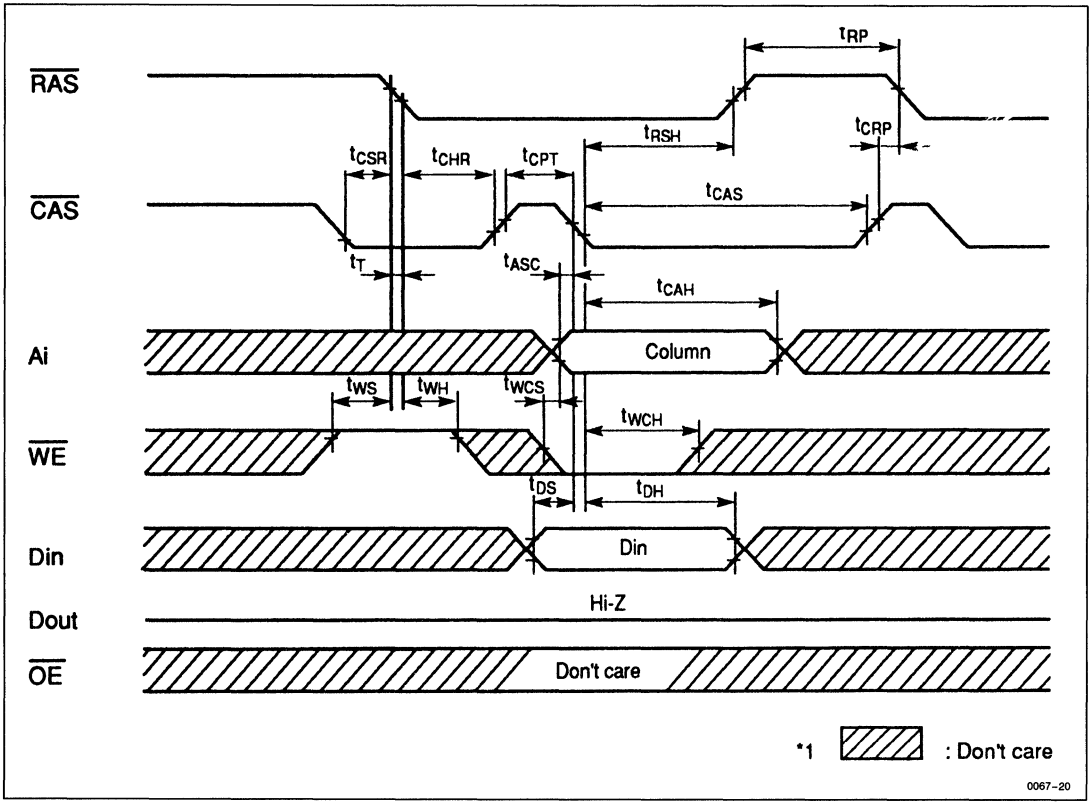
• $\overline{RAS}$ Only Refresh Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle, (READ)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle, (WRITE)



HM514410A Series — Preliminary

1,048,576-Word x 4-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514410A is a CMOS dynamic RAM organized 1,048,576-word x 4-bit. HM514400A has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514410A offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514410A to be packaged in standard 350 mil 20-pin plastic SOJ, standard 300 mil 20-pin plastic SOJ, standard 400 mil 20-pin plastic ZIP, 20-pin plastic TSOP I, 20-pin plastic TSOP I reverse type, 20-pin plastic TSOP II, and 20-pin plastic TSOP II reverse type.

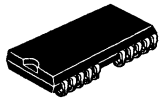
■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time ..... 60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode ..... 577.5 mW/550 mW/495 mW/440 mW (max)
  - Standby Mode ..... 11 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles ..... (16 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Test Function
- Write per Bit Capability

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM514410AJ-6	60 ns	350 mil 20-pin
HM514410AJ-7	70 ns	Plastic SOJ
HM514410AJ-8	80 ns	(CP-20DA)
HM514410AJ-10	100 ns	
HM514410AS-6	60 ns	300 mil 20-pin
HM514410AS-7	70 ns	Plastic SOJ
HM514410AS-8	80 ns	(CP-20D)
HM514410AS-10	100 ns	
HM514410AZ-6	60 ns	400 mil 20-pin
HM514410AZ-7	70 ns	Plastic ZIP
HM514410AZ-8	80 ns	(ZP-20)
HM514410AZ-10	100 ns	
HM514410AT-6	60 ns	20-pin
HM514410AT-7	70 ns	Plastic TSOP I
HM514410AT-8	80 ns	(TFP-20DA)
HM514410AT-10	100 ns	
HM514410AR-6	60 ns	20-pin
HM514410AR-7	70 ns	Plastic TSOP I
HM514410AR-8	80 ns	Reverse Type
HM514410AR-10	100 ns	(TFP-20DAR)
HM514410ATT-6	60 ns	20-pin
HM514410ATT-7	70 ns	Plastic TSOP II
HM514410ATT-8	80 ns	(TTP-20D)
HM514410ATT-10	100 ns	
HM514410ARR-6	60 ns	20-pin
HM514410ARR-7	70 ns	Plastic TSOP II
HM514410ARR-8	80 ns	Reverse Type
HM514410ARR-10	100 ns	(TTP-20DR)

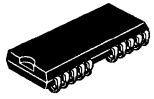
HM514410AJ Series



3DCP20DA

(CP-20DA)

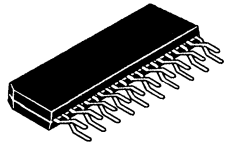
HM514410AS Series



3DCP20D

(CP-20D)

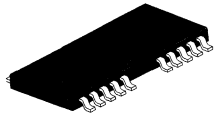
HM514410AZ Series



3DZP20

(ZP-20)

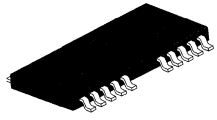
HM514410AT Series



3DTFP20DA

(TFP-20DA)

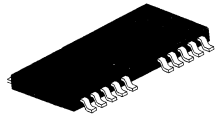
HM514410AR Series



3DTFP20DAR

(TFP-20DAR)

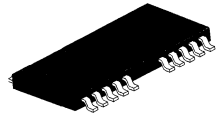
HM514410ATT Series



3DTTP20D

(TTP-20D)

HM514410ARR Series

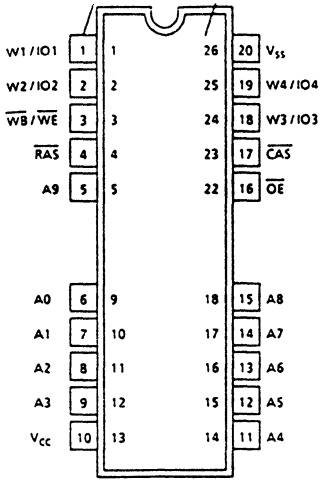


3DTTP20DR

(TTP-20DR)

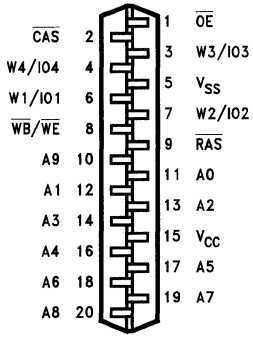
■ PIN OUT

HM514410AJ Series
HM514410AS Series



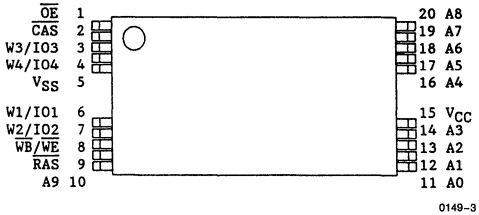
(Top View)

HM514410AZ Series



(Bottom View)

HM514410AT Series



(Top View)

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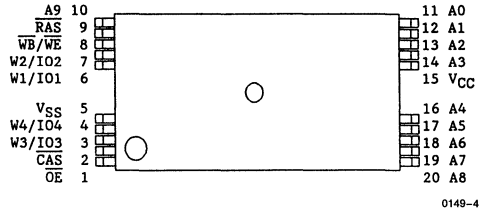

(Top View)

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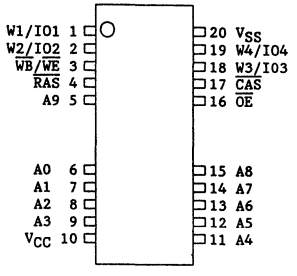
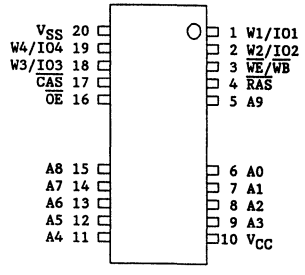


(Top View)

HM514410ARR Series



(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{10}	Address Input
A_0–A_9	Refresh Address Input
$W1/IO_1$–$W4/IO_4$	Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB}/\overline{WE}$	Read/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+ 5V)
V_{SS}	Ground

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	− 1.0	—	0.8	V	1
	(Others)	V_{IL}	− 2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HM514410A-6		HM514410A-7		HM514410A-8		HM514410A-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	110	—	100	—	90	—	80	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	1	—	1	—	1	—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	110	—	100	—	90	—	80	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	110	—	100	—	90	—	80	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	110	—	100	—	90	—	80	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed ≤ 1 time while $\overline{RAS}$ = V_{IL}.
3. Address can be changed ≤ 1 time while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 14, 15, 16]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514410A-6		HM514410A-7		HM514410A-8		HM514410A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10000	20	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	20	60	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	15	—	20	—	20	—	25	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	0	—	ns	
$\overline{CAS}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	0	—	0	—	ns	
Transition Time (Rise to Fall)	t_T	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514410A-6		HM514410A-7		HM514410A-8		HM514410A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	2, 3, 17
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	—	25	ns	3, 4, 13, 17
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	ns	3, 5, 13, 17
Access Time from $\overline{OE}$	t_{OAC}	—	15	—	20	—	20	—	25	ns	3, 17
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	ns	20
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	0	—	ns	20
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	15	0	20	0	20	0	25	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	15	0	20	0	20	0	25	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	15	—	20	—	20	—	25	—	ns	

Write Cycle

Parameter	Symbol	HM514410A-6		HM514410A-7		HM514410A-8		HM514410A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	10	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	20	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	20	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514410A-6		HM514410A-7		HM514410A-8		HM514410A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	150	—	180	—	200	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	95	—	105	—	135	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	35	—	45	—	45	—	60	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	50	—	60	—	65	—	80	—	ns	10
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	15	—	20	—	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM514410A-6		HM514410A-7		HM514410A-8		HM514410A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh) Cycle	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh) Cycle	t_{CHR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge to Time in Normal Mode	t_{CPN}	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514410A-6		HM514410A-7		HM514410A-8		HM514410A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	35	—	40	—	45	—	50	ns	3, 13, 17
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	45	—	50	—	ns	
Fast Page Mode Read-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPW}	55	—	65	—	70	—	85	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	80	—	95	—	100	—	110	—	ns	

Test Mode Cycle

Parameter	Symbol	HM514410A-6		HM514410A-7		HM514410A-8		HM514410A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	10	—	10	—	10	—	10	—	ns	

Counter Test Cycle

Parameter	Symbol	HM514410A-6		HM514410A-7		HM514410A-8		HM514410A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	40	—	40	—	40	—	50	—	ns	

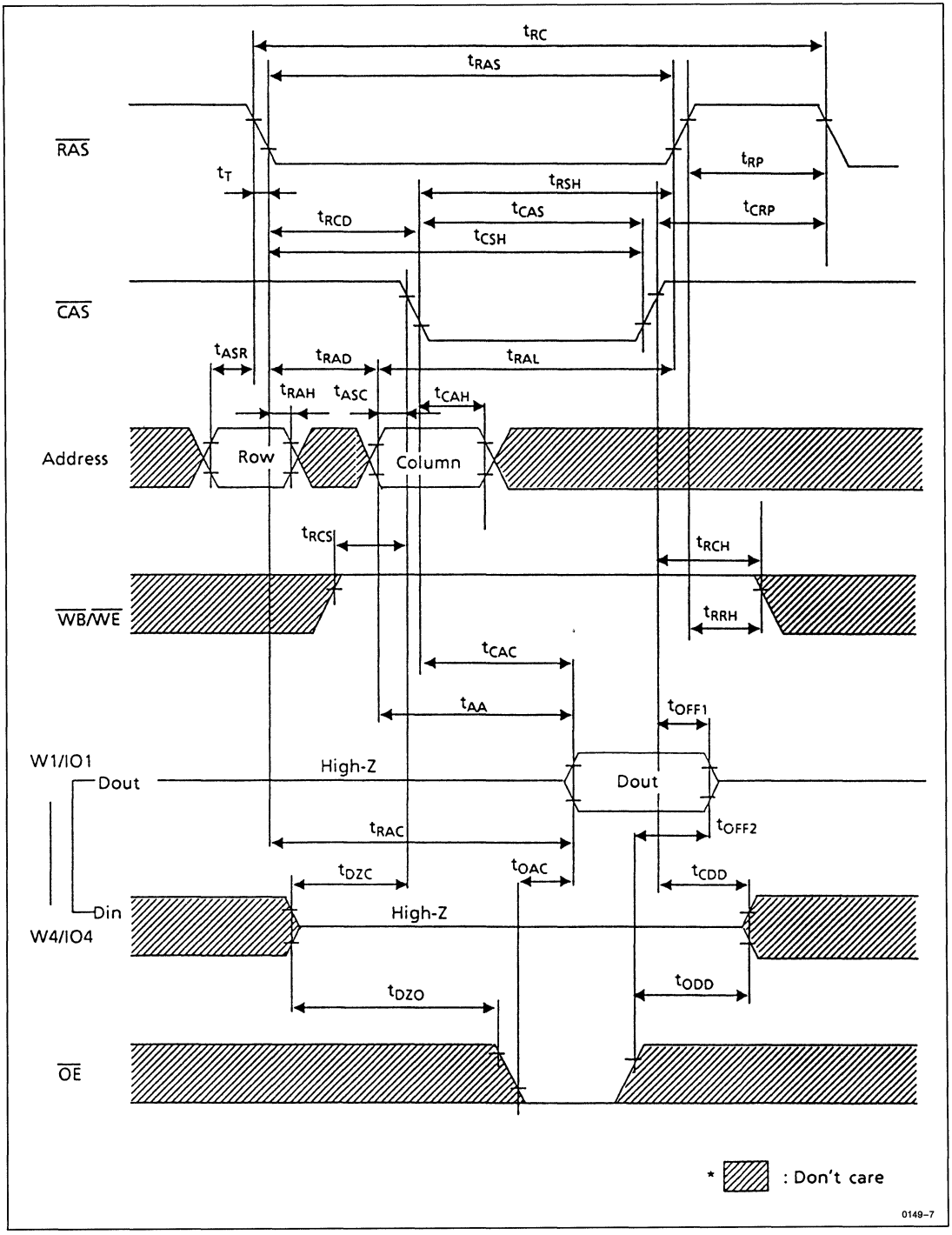
Write Per Bit[18, 19]

Parameter	Symbol	HM514410A-6		HM514410A-7		HM514410A-8		HM514410A-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write per Bit Setup Time	t_{WBS}	0	—	0	—	0	—	0	—	ns	
Write per Bit Hold Time	t_{WBH}	10	—	10	—	10	—	15	—	ns	
Write per Bit Selection Setup Time	t_{WDS}	0	—	0	—	0	—	0	—	ns	
Write per Bit Selection Hold Time	t_{WDS}	10	—	10	—	10	—	15	—	ns	

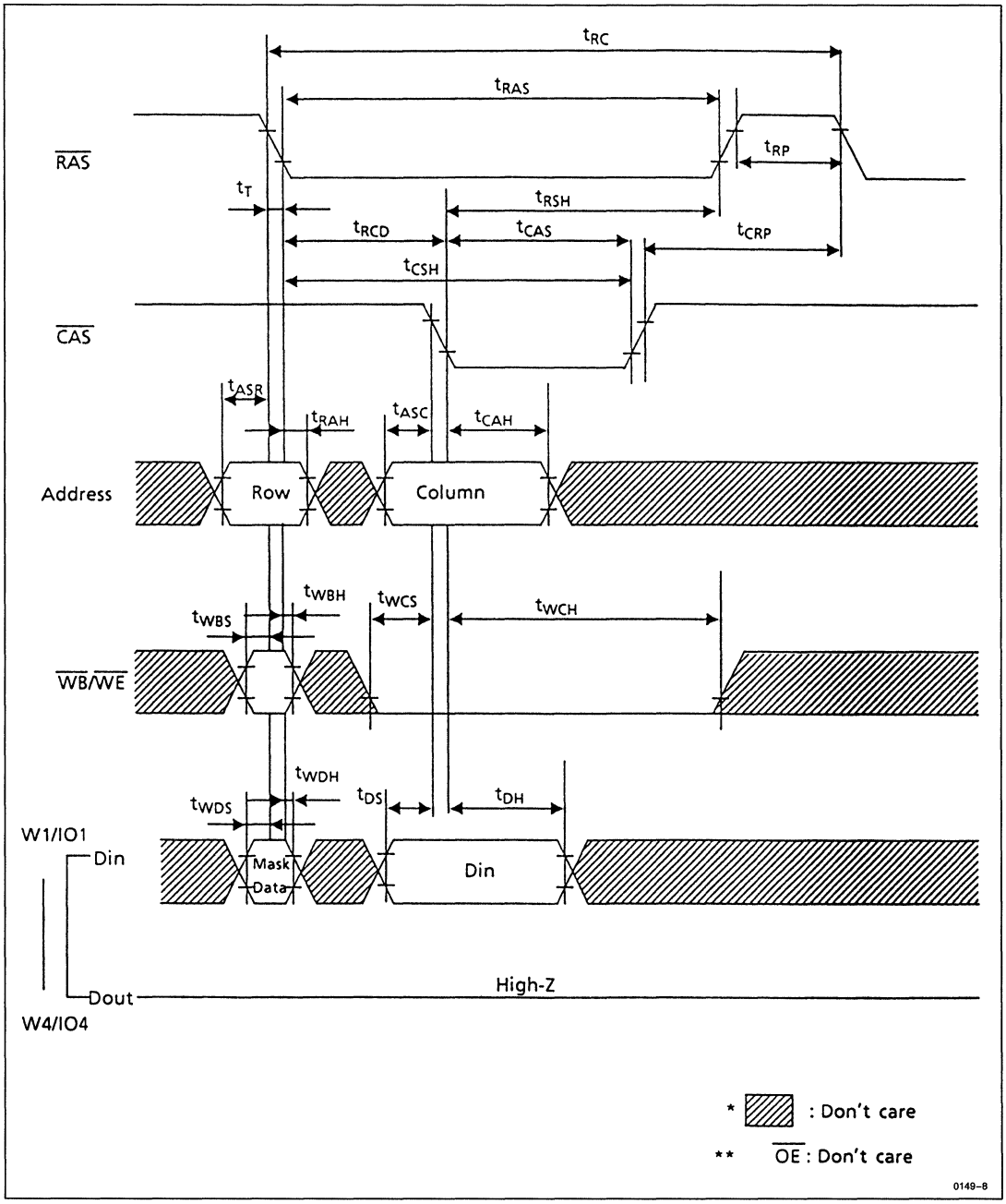
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, OE must disable output buffer prior to applying data to the device.
16. Test mode operation specified in this data sheet is 2-bit test function controlled by control address bits—CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of two test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC}, t_{OAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
18. When using the write per bit capability, $\overline{WB}/\overline{WE}$ must be low as $\overline{RAS}$ falls.
19. The data bits to which the write operation is applied can be specified by keeping $W1/IO_1$, $W2/IO_2$, $W3/IO_3$, and $W4/IO_4$ high with setup and hold time referenced to the $\overline{RAS}$ negative transition.
20. Either t_{RCH} or t_{RRH} shall be satisfied.

■ TIMING WAVEFORMS

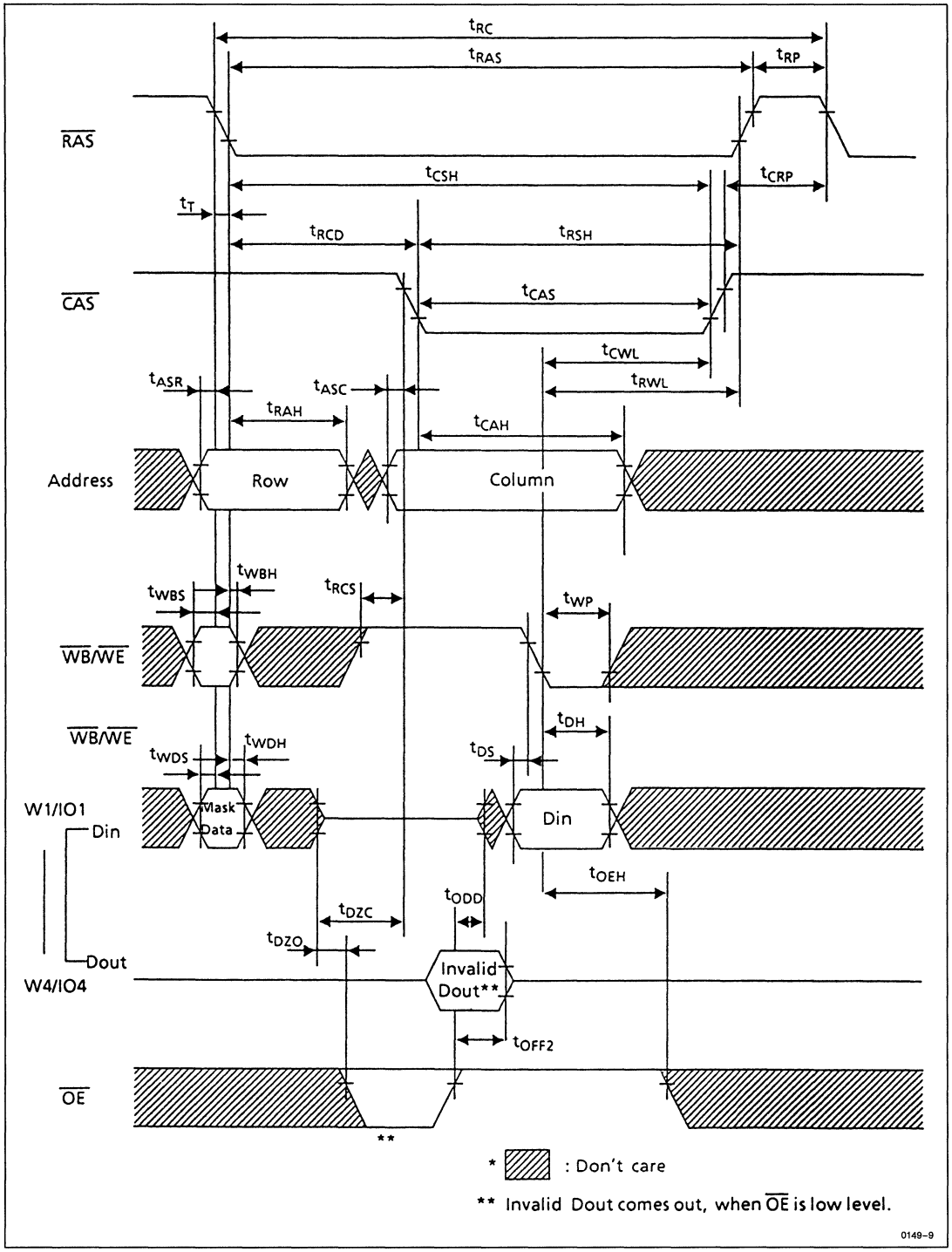
• Read Cycle



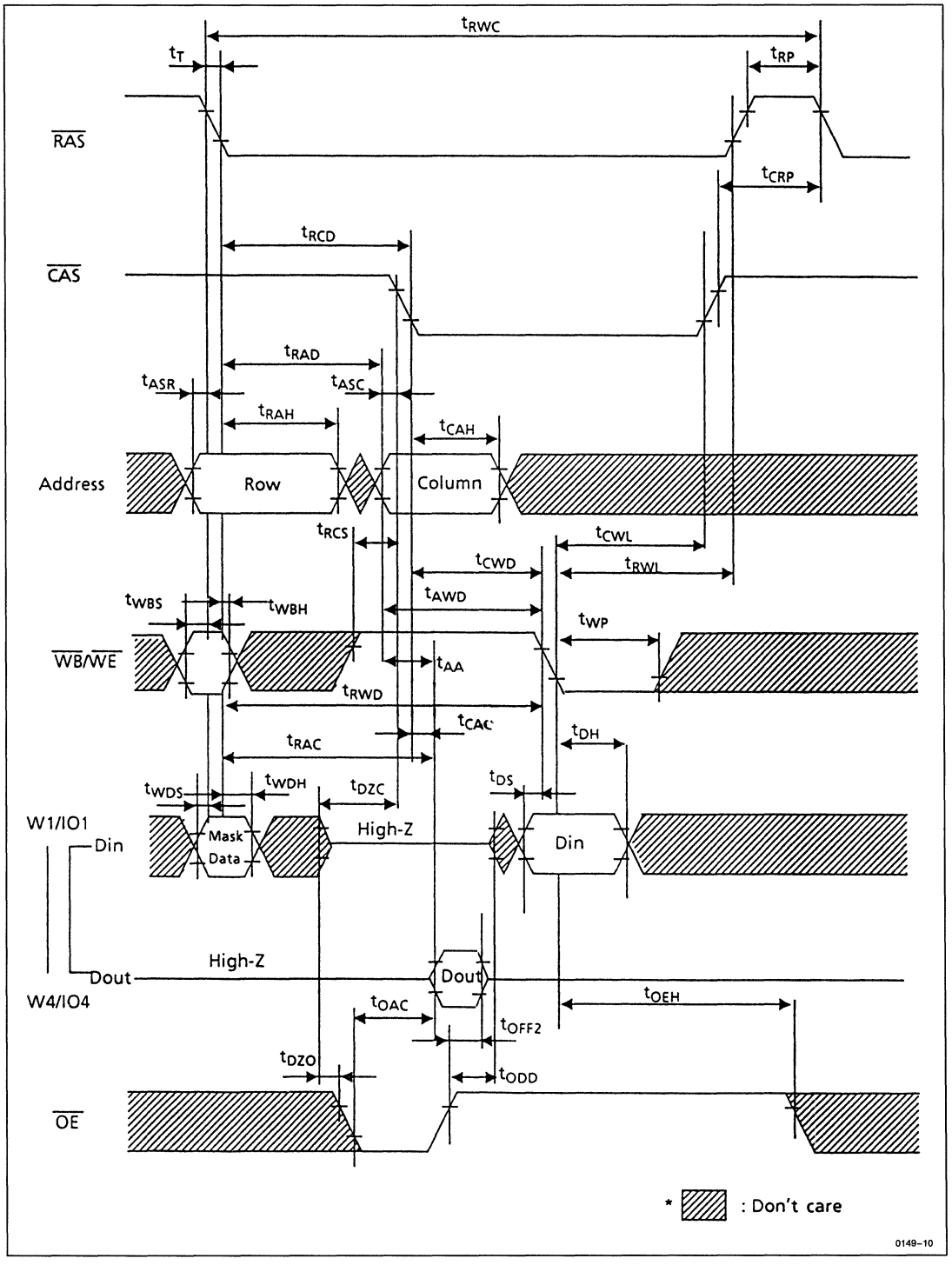
• **Early Write Cycle**



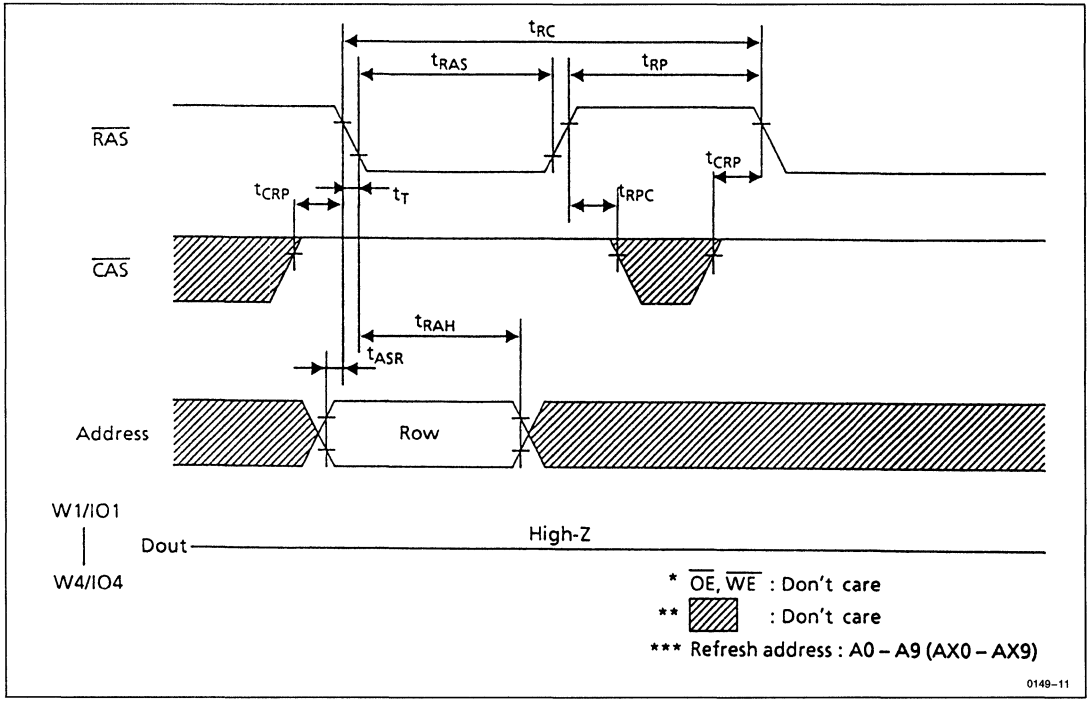
• **Delayed Write Cycle**



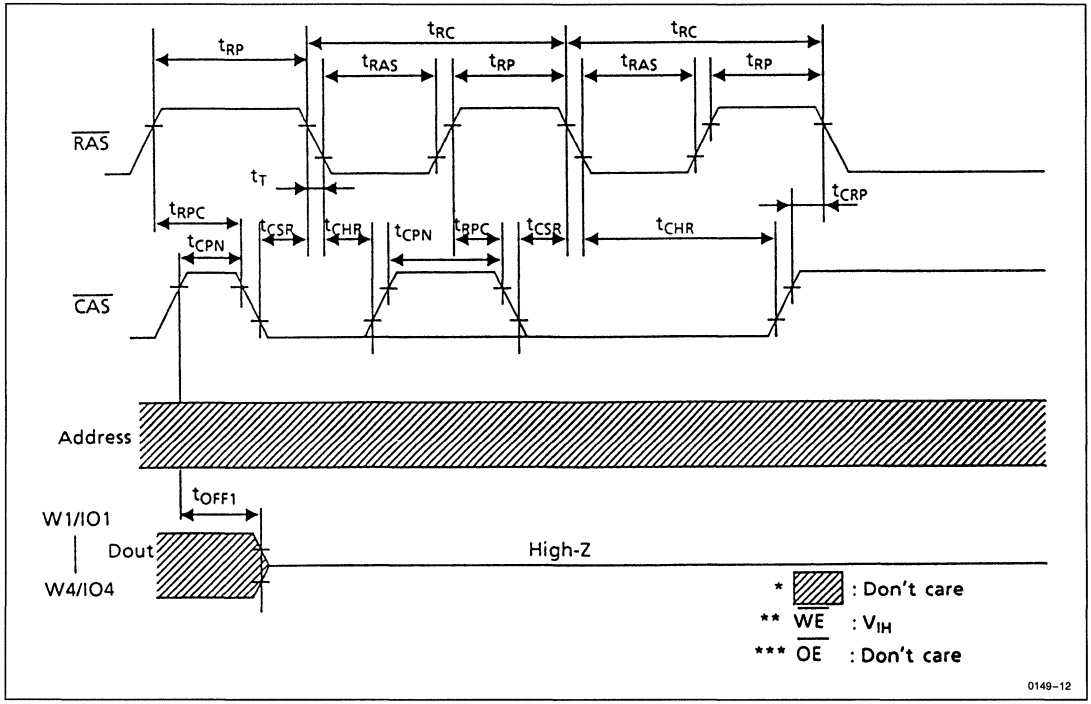
• **Read-Modify-Write Cycle**



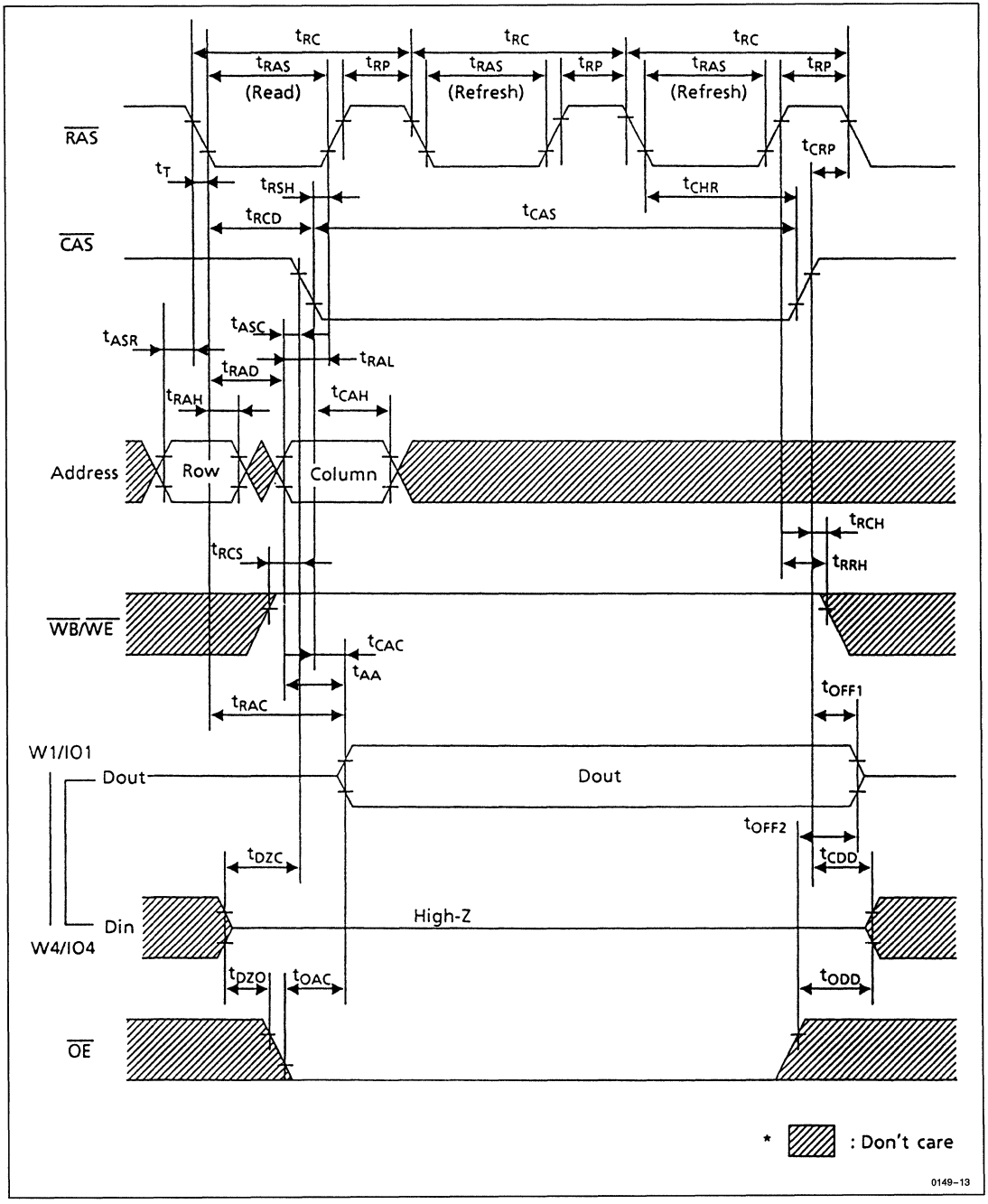
• $\overline{RAS}$ Only Refresh Cycle



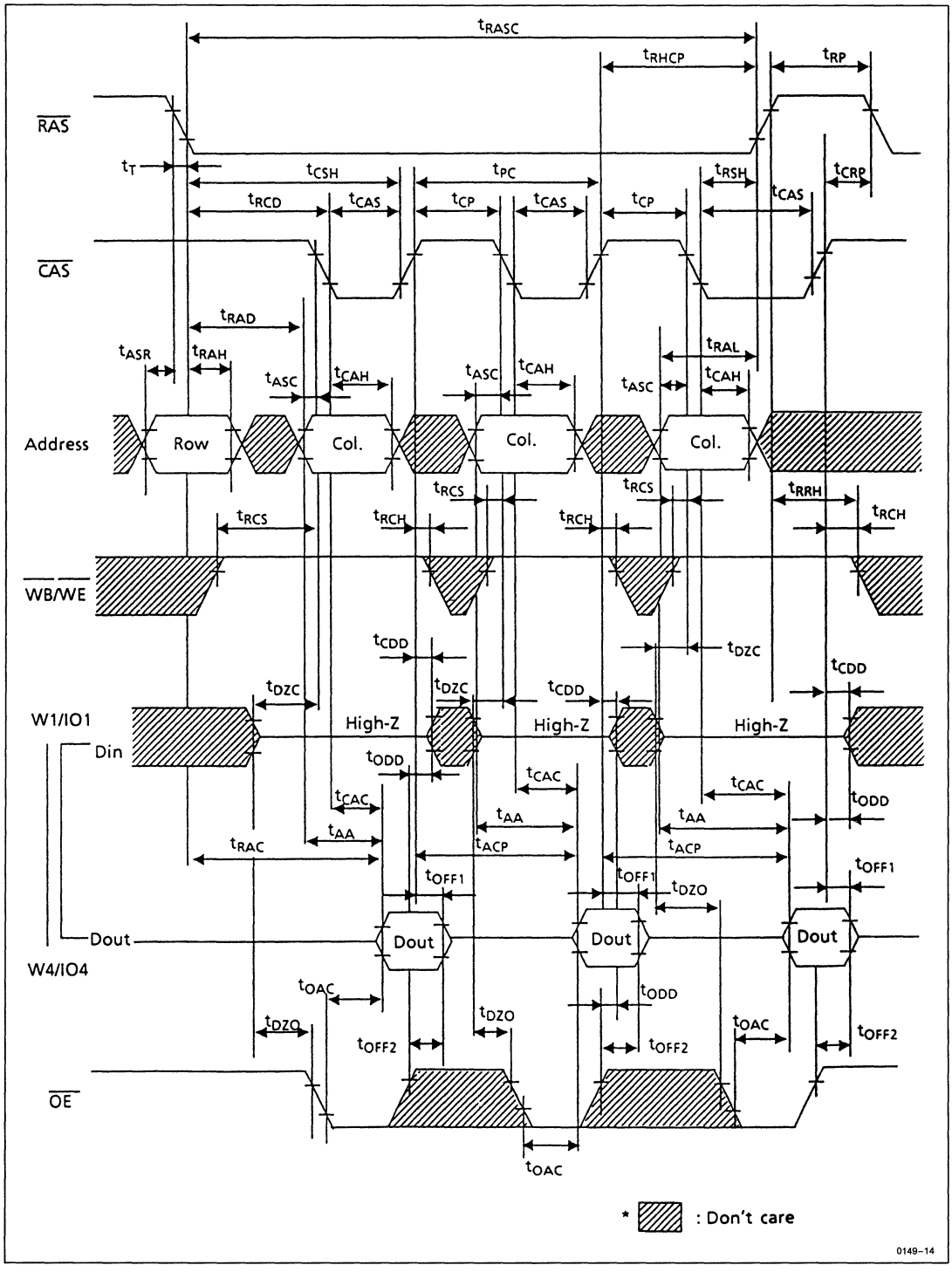
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



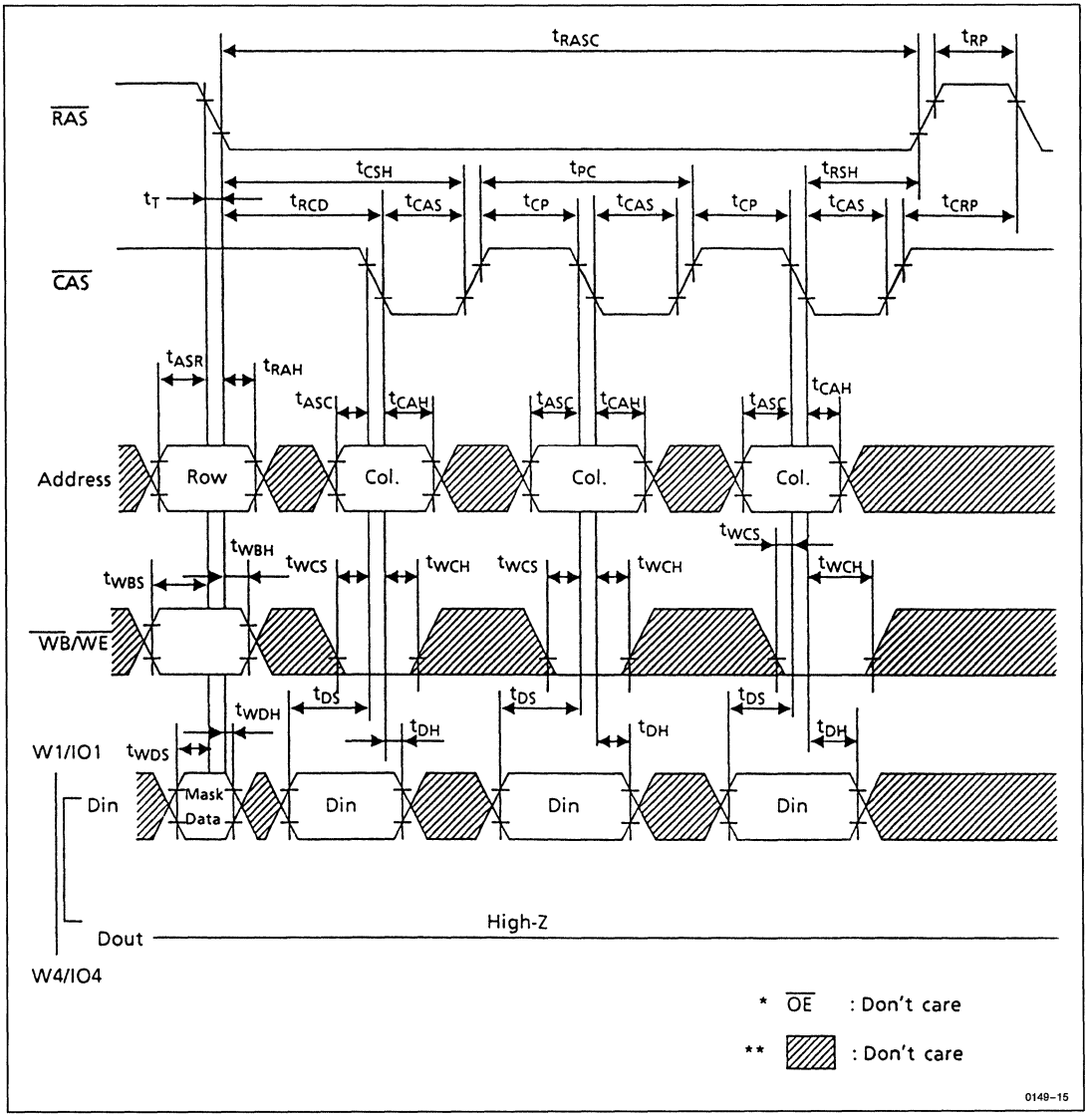
• Hidden Refresh Cycle



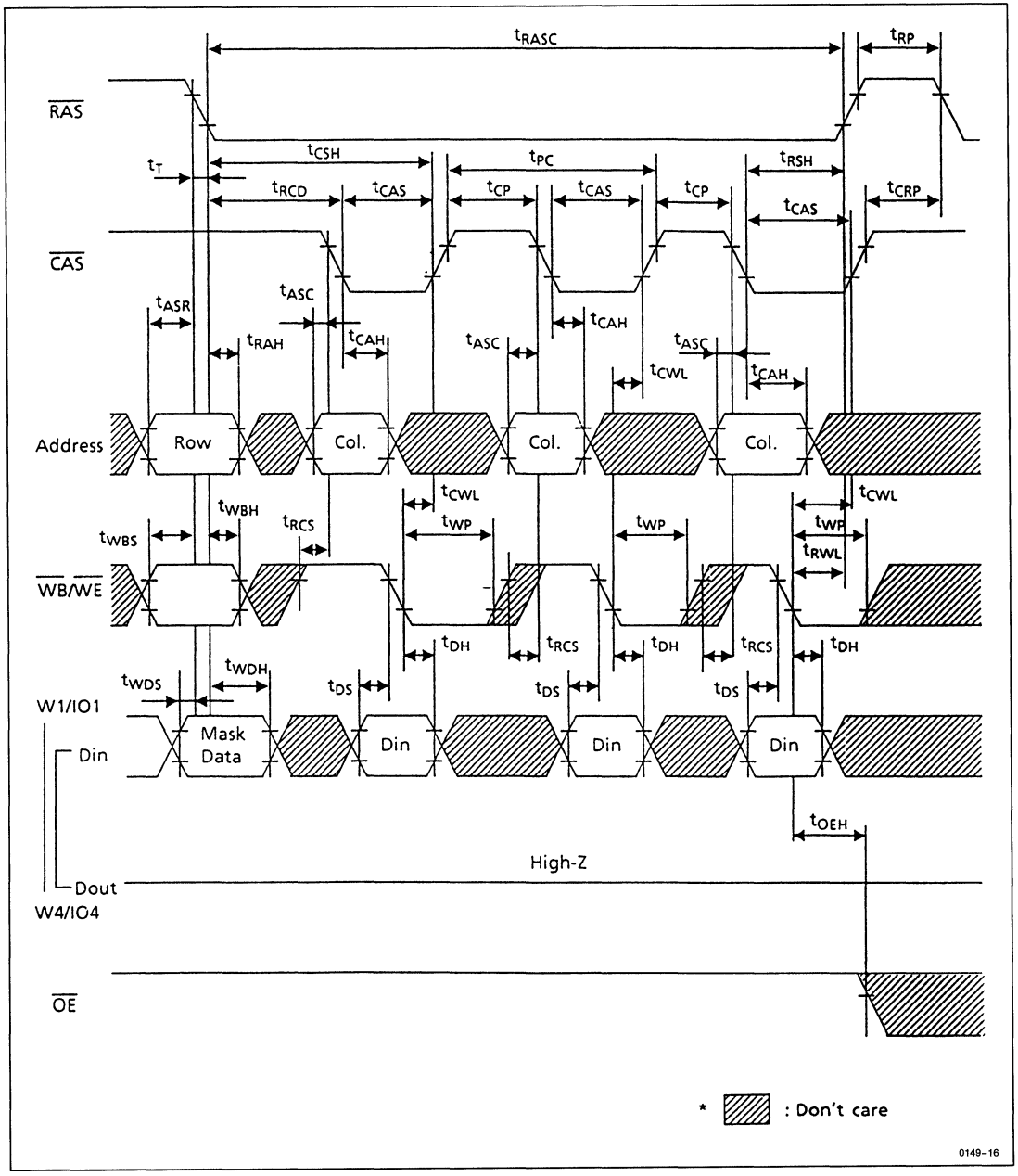
• **Fast Page Mode Read Cycle**



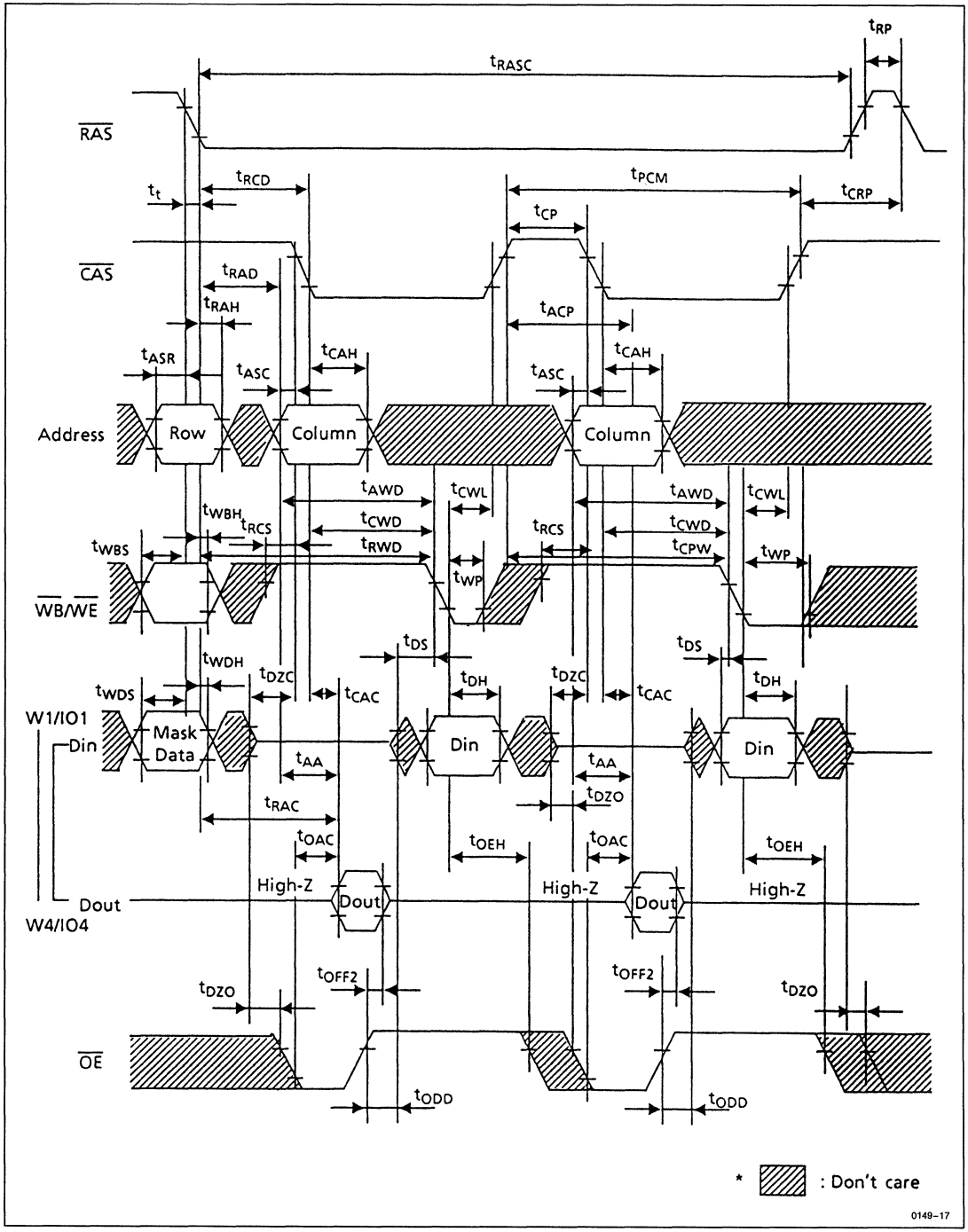
• **Fast Page Mode Early Write Cycle**



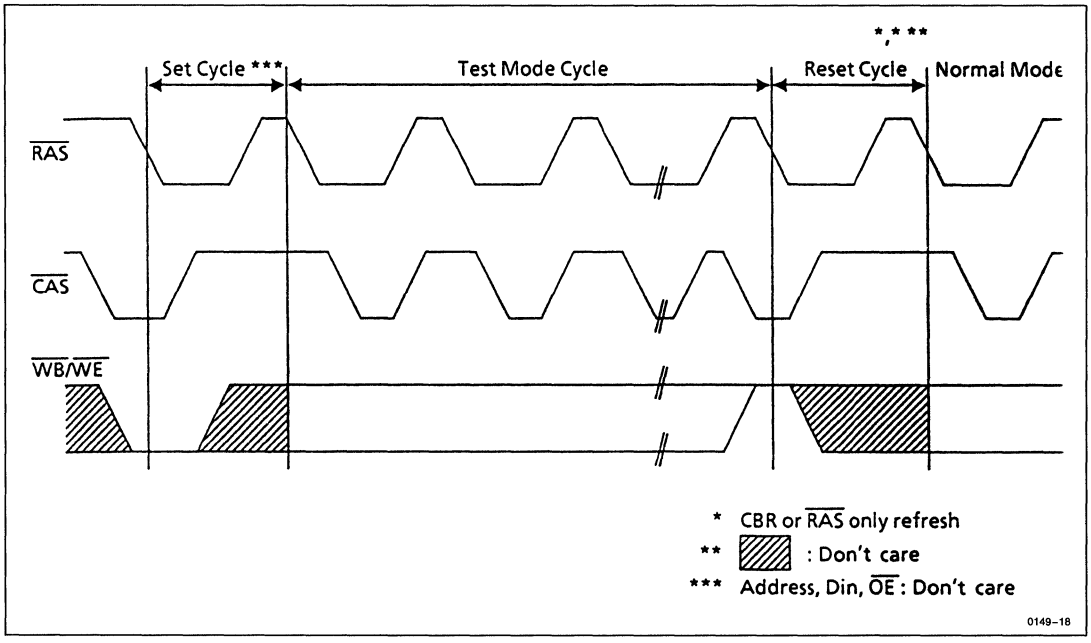
• **Fast Page Delayed Cycle**



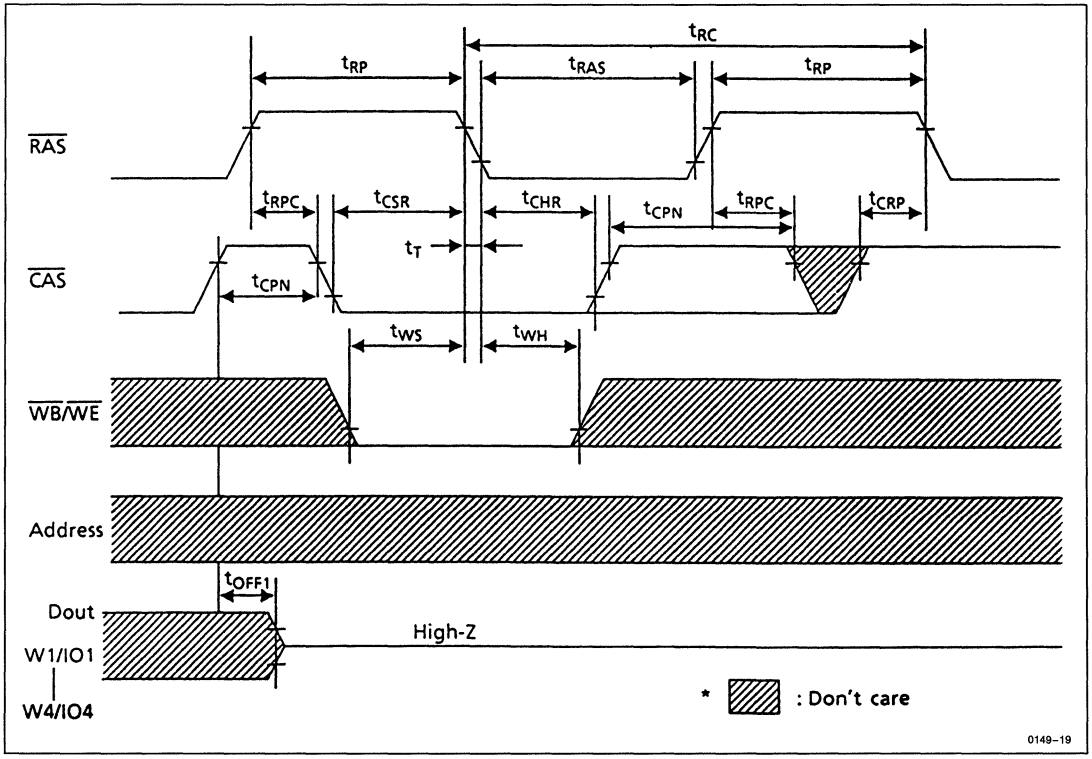
• **Fast Page Mode Read-Modify Write Cycle**



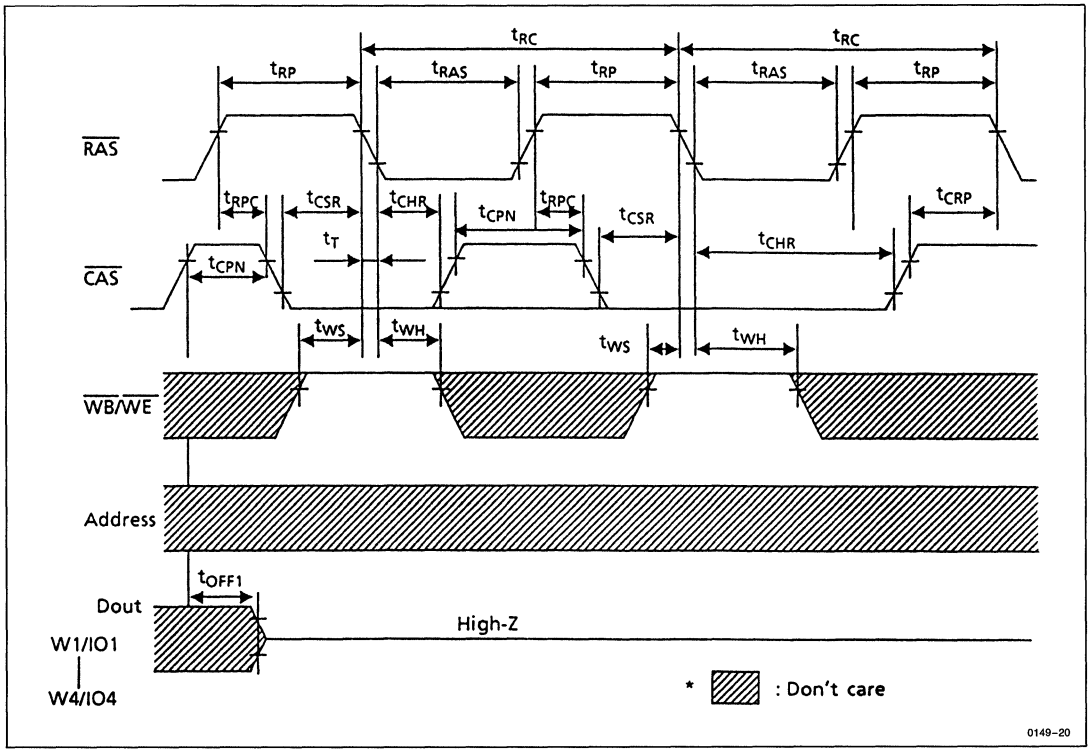
• **Test Mode Cycle**



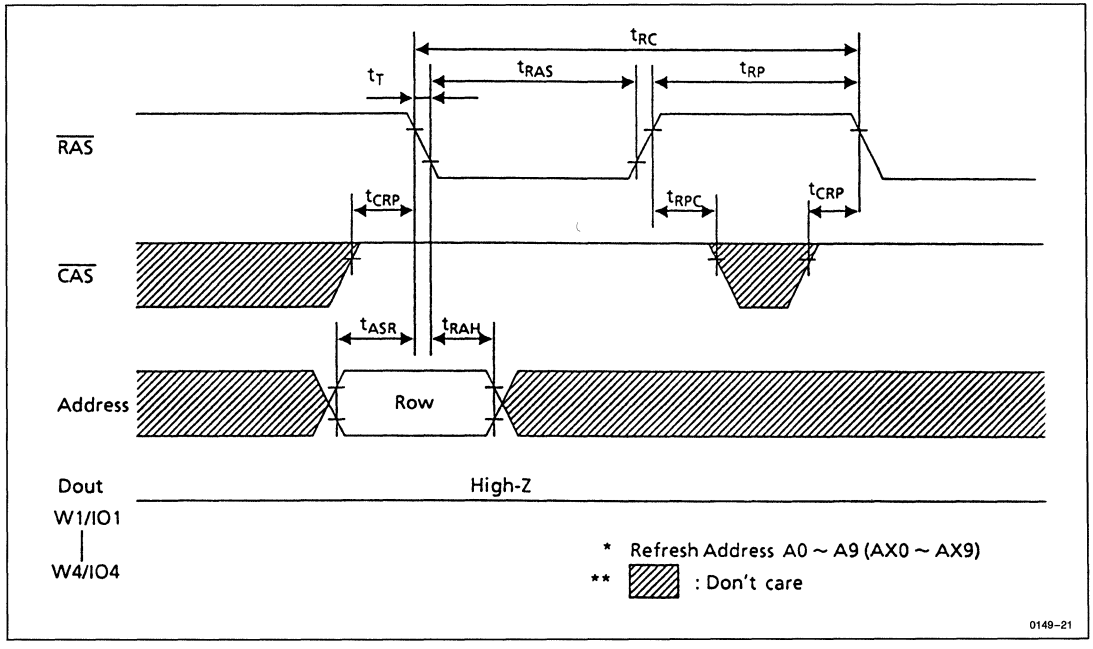
• **Test Mode Set Cycle**



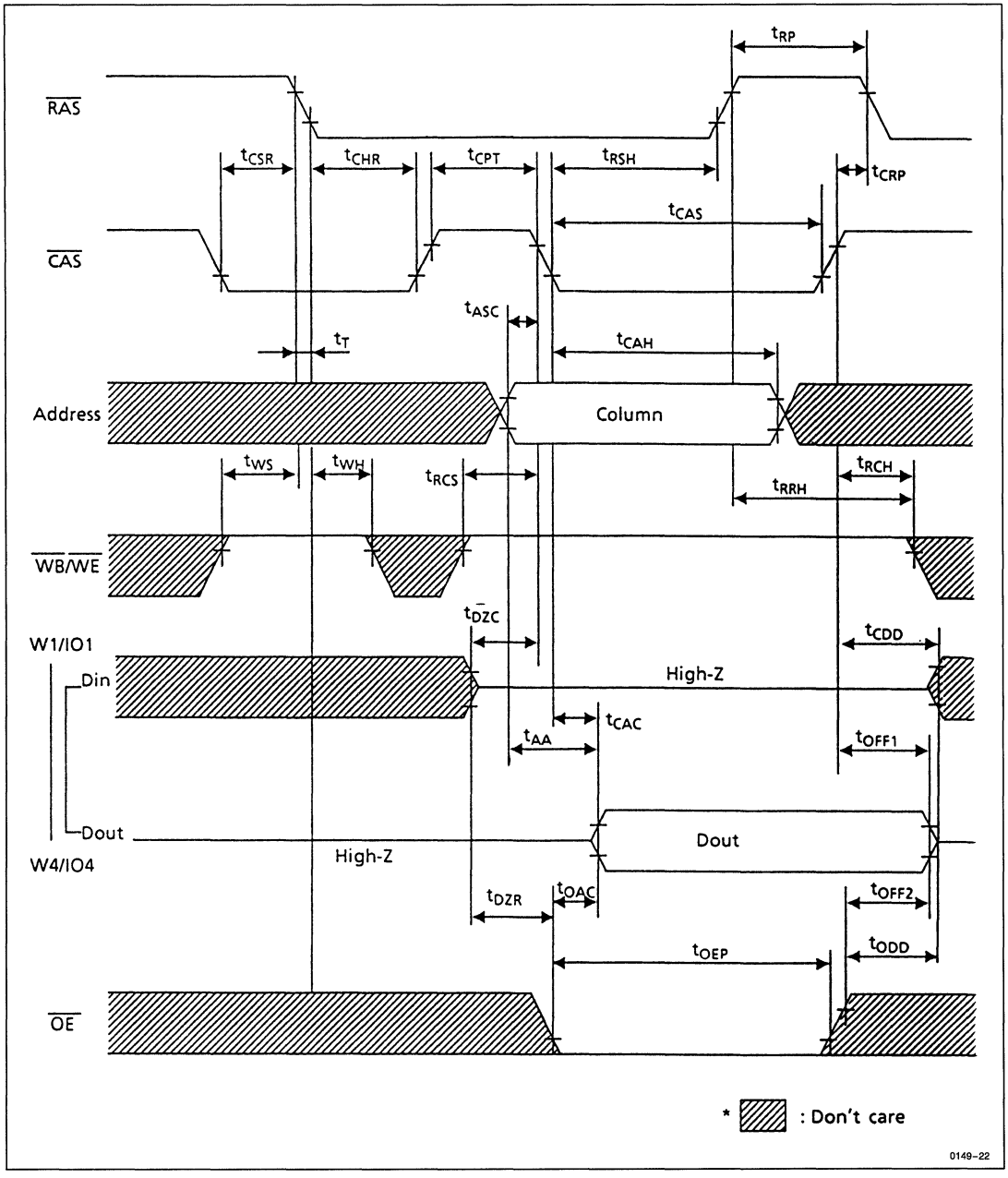
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



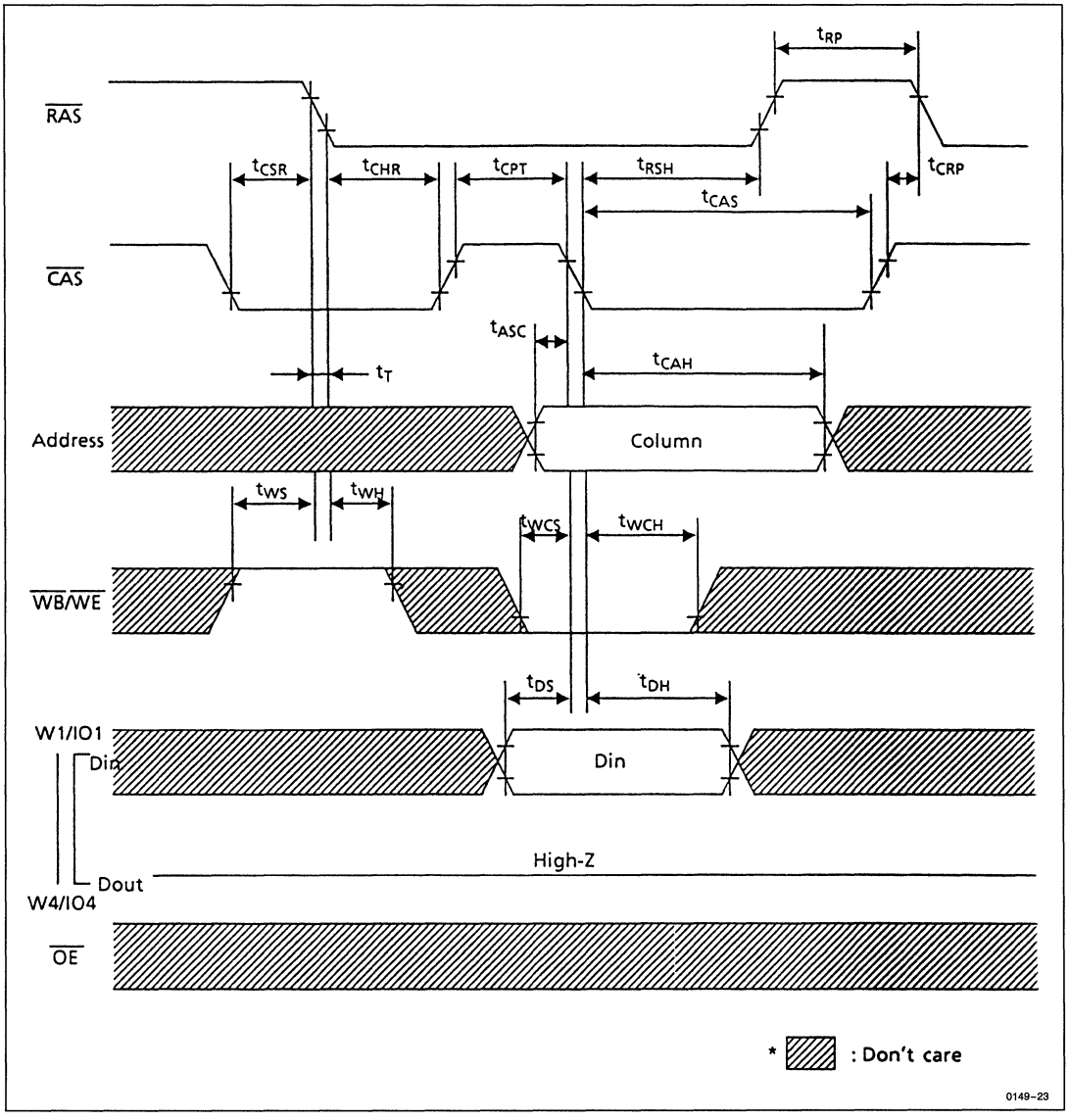
• $\overline{RAS}$ Only Refresh Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM514800 Series — Preliminary

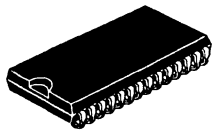
524,288-Word x 8-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514800 are CMOS dynamic RAM organized as 524,288-word x 8-bit. HM514800 have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514800 offer Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514800 to be packaged in standard 400 mil 28-pin plastic SOJ, standard 400 mil 28-pin plastic ZIP.

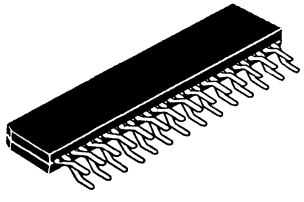
HM514800JP Series



3DCP28D

(CP-28D)

HM514800ZP Series



3DZP28

(ZP-28)

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time ..... 70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode ..... 605 mW/550 mW/495 mW (max)
  - Standby Mode ..... 11 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles ..... (16 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh

■ ORDERING INFORMATION

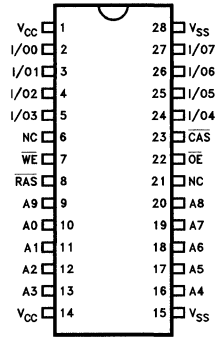
Part No.	Access Time	Package
HM514800JP-7	70 ns	400 mil 28-pin
HM514800JP-8	80 ns	Plastic SOJ
HM514800JP-10	100 ns	(CP-28D)
HM514800ZP-7	70 ns	400 mil 28-pin
HM514800ZP-8	80 ns	Plastic ZIP
HM514800ZP-10	100 ns	(ZP-28)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input —Row Address A_0–A_9 —Column Address A_0–A_8 —Refresh Address A_0–A_9
I/O_0–I/O_7	Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

■ PIN OUT

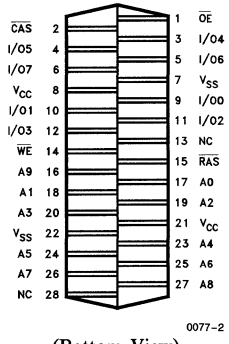
HM514800JP Series



0077-1

(Top View)

HM514800ZP Series



0077-2

(Bottom View)

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	− 1.0	—	0.8	V	1
	(Others)	V_{IL}	− 2.0	—	0.8	V	1

Notes: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM514800-7		HM514800-8		HM514800-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	110	—	100	—	90	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	1	—	1	—	1	mA	CMOS Interface, $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	110	—	100	—	90	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	110	—	100	—	90	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	110	—	100	—	90	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 14, 15]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514800-7		HM514800-8		HM514800-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	20	60	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	15	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	20	—	20	—	25	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514800-7		HM514800-8		HM514800-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	3, 4, 13
Access Time from Address	t_{AA}	—	35	—	40	—	45	ns	3, 5, 13
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	35	—	40	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	15	0	15	0	20	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	15	0	15	0	20	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	15	—	15	—	20	—	ns	

Write Cycle

Parameter	Symbol	HM514800-7		HM514800-8		HM514800-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514800-7		HM514800-8		HM514800-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	180	—	200	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	95	—	105	—	135	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	45	—	45	—	60	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	60	—	65	—	80	—	ns	10, 13
$\overline{OE}$ to Hold Time from $\overline{WE}$	t_{OEH}	20	—	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM514800-7		HM514800-8		HM514800-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time in Normal Mode	t_{CPN}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514800-7		HM514800-8		HM514800-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	ns	3, 13
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	ns	
Fast Page Mode Read-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPW}	65	—	70	—	85	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	95	—	100	—	110	—	ns	

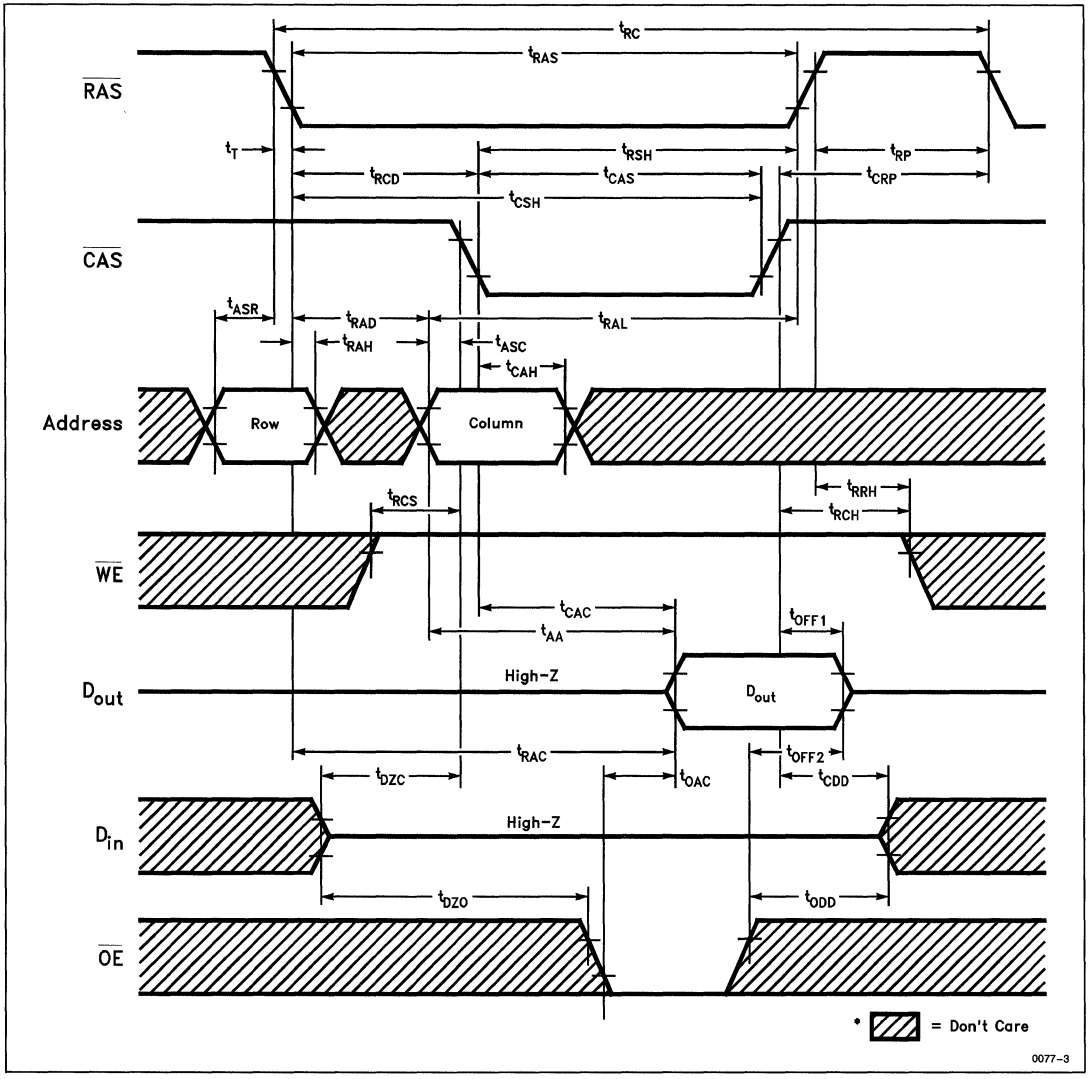
Counter Test Cycle

Parameter	Symbol	HM514800-7		HM514800-8		HM514800-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	50	—	50	—	50	—	ns	

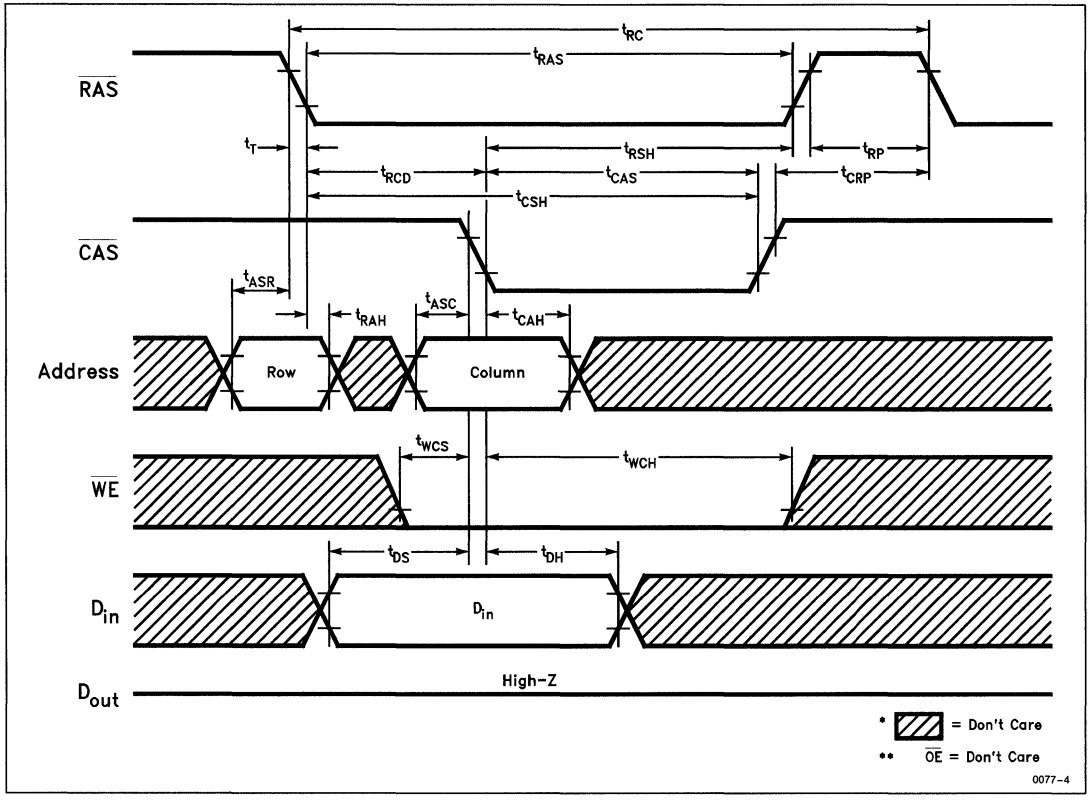
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL load and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Either t_{RCH} or T_{RRH} must be satisfied for a read cycle.

■ TIMING WAVEFORMS

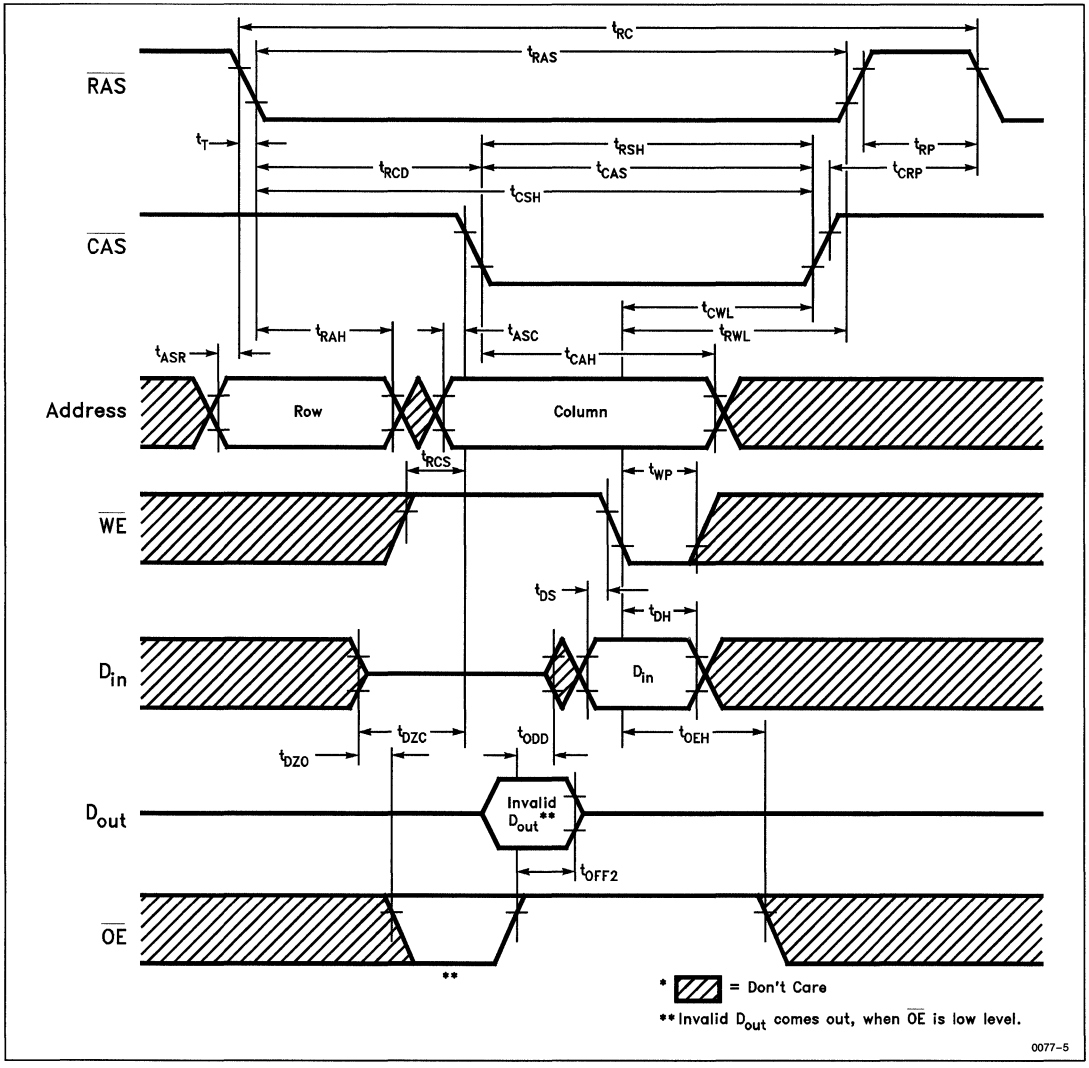
• Read Cycle



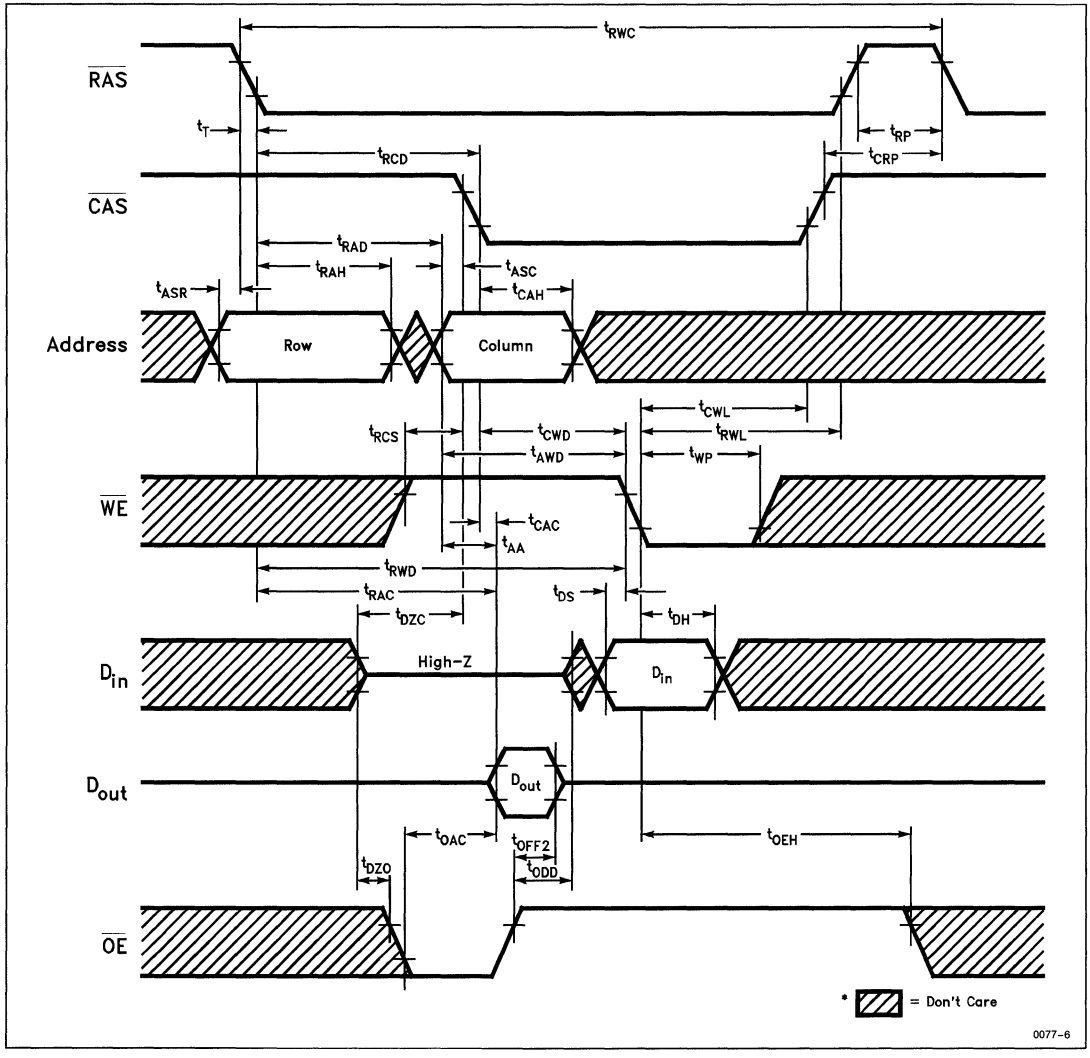
• **Early Write Cycle**



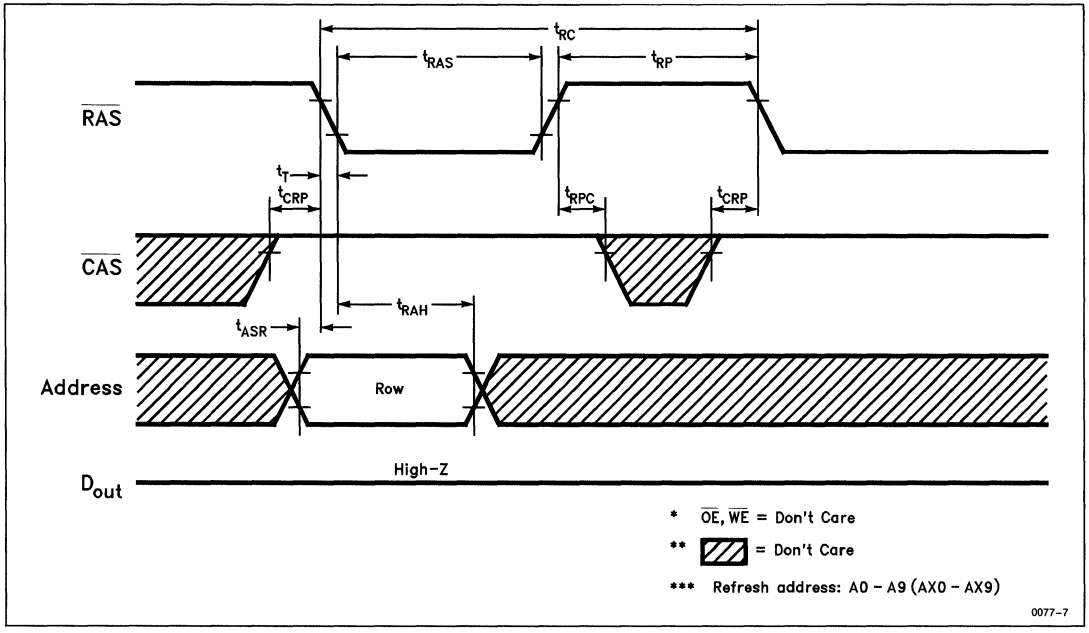
• **Delayed Write Cycle**



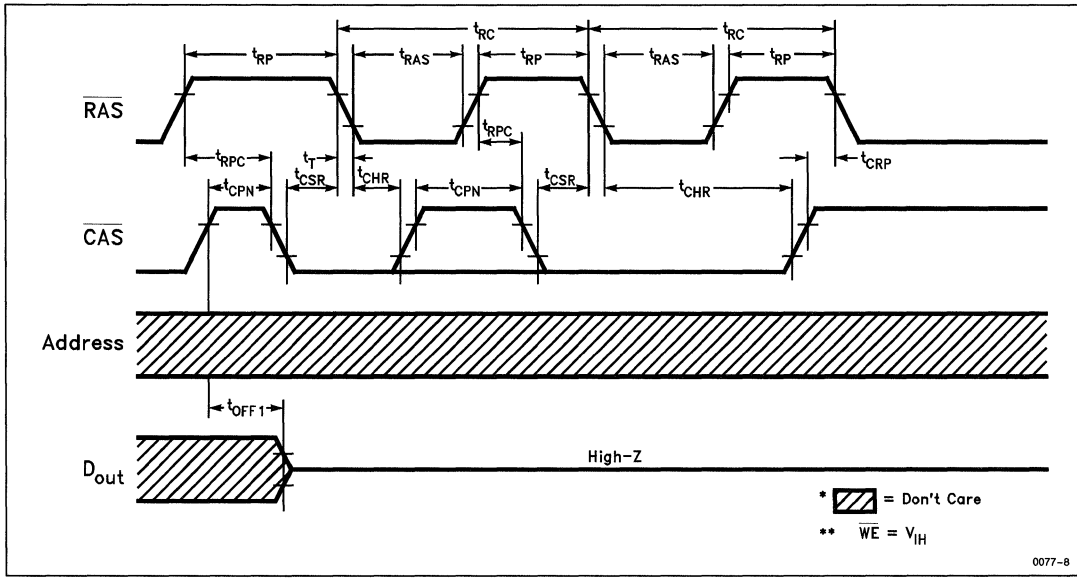
• **Read-Modify-Write Cycle**



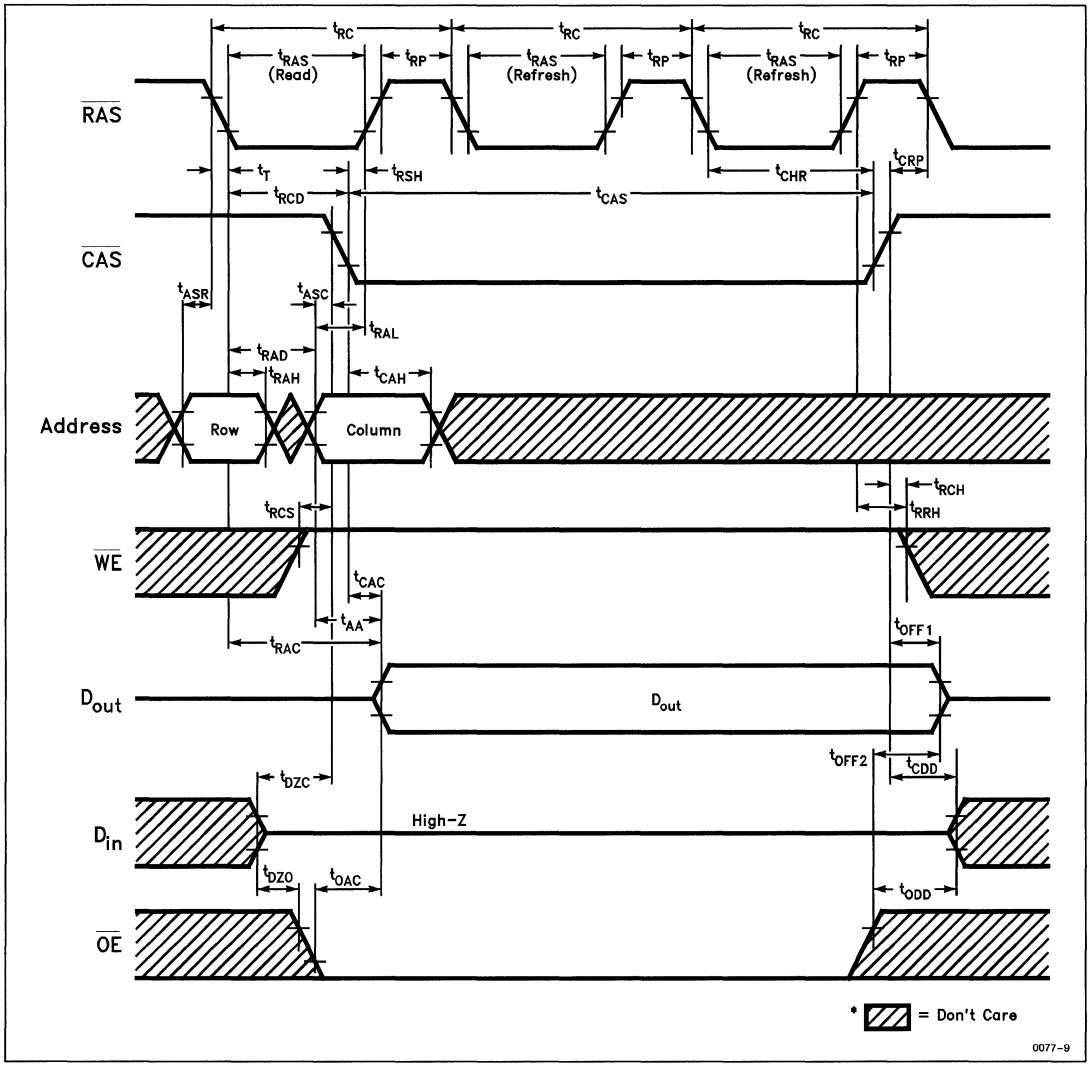
• $\overline{RAS}$ Only Refresh Cycle



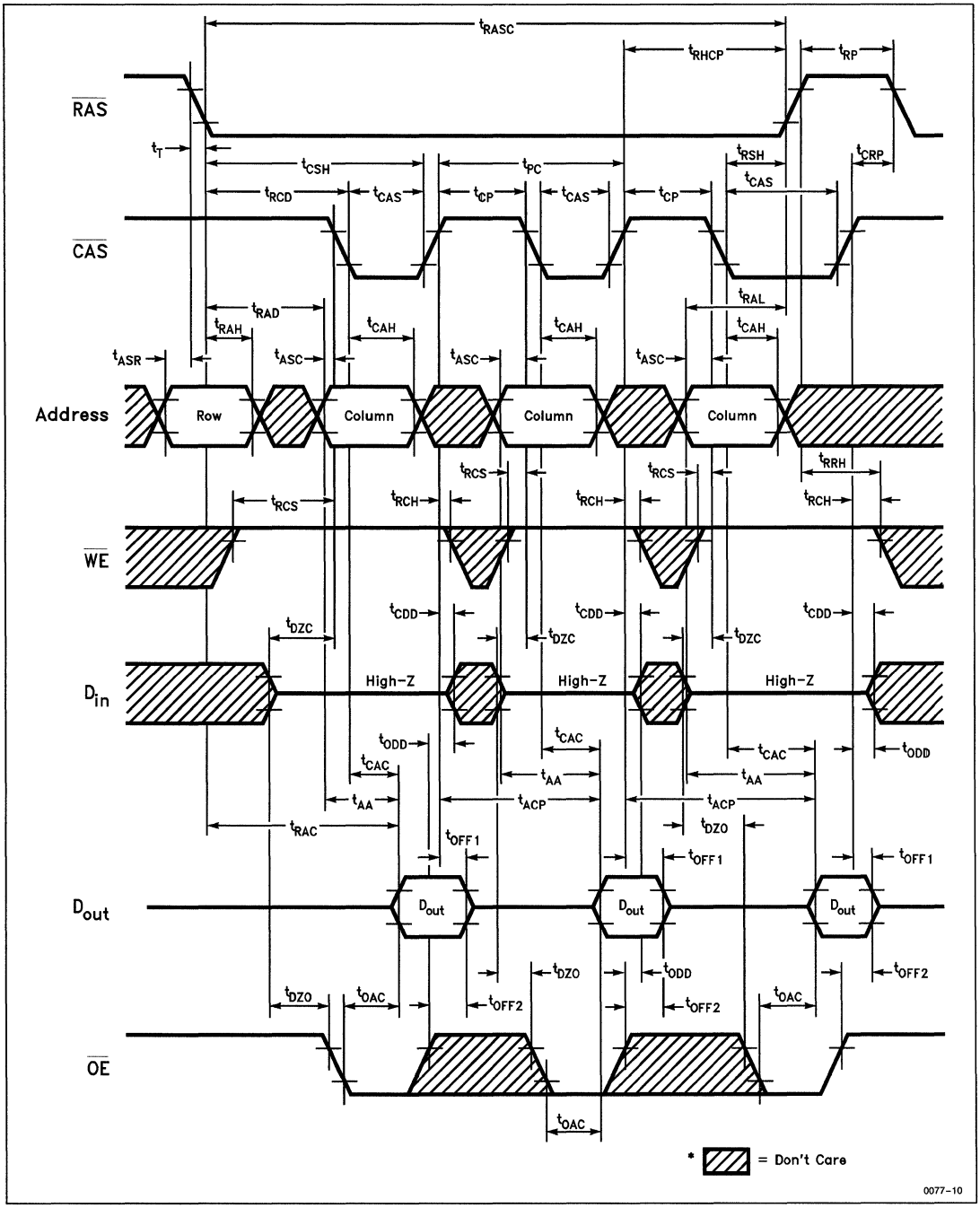
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



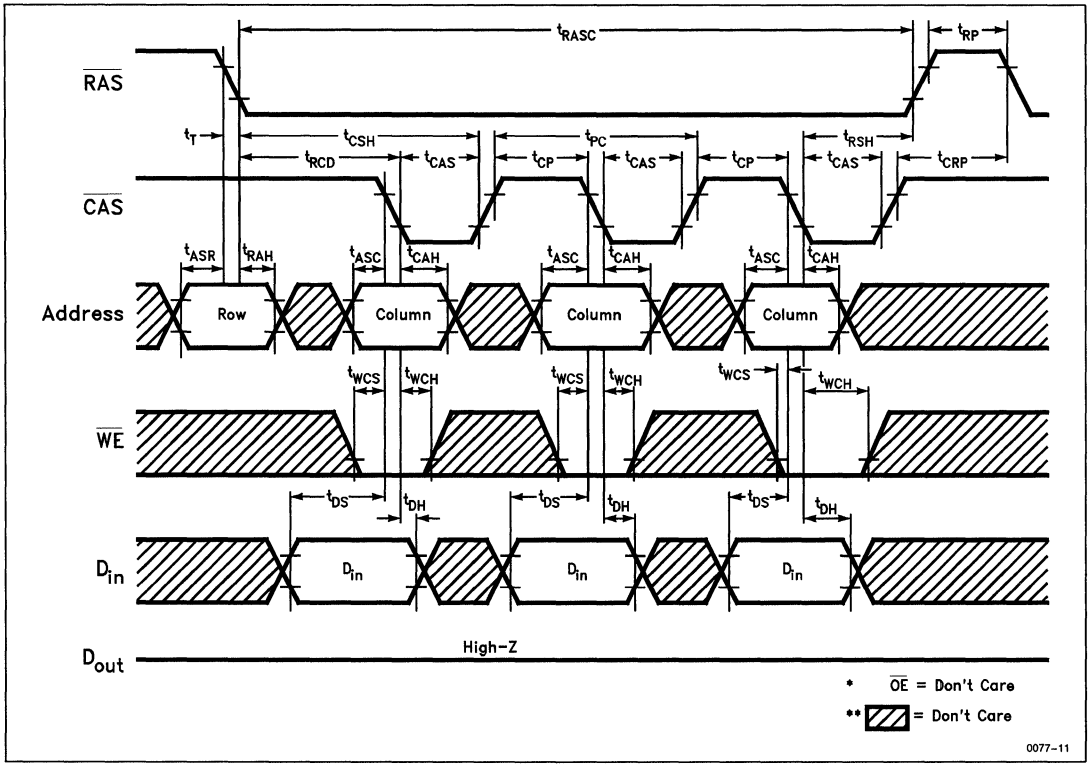
• **Hidden Refresh Cycle**



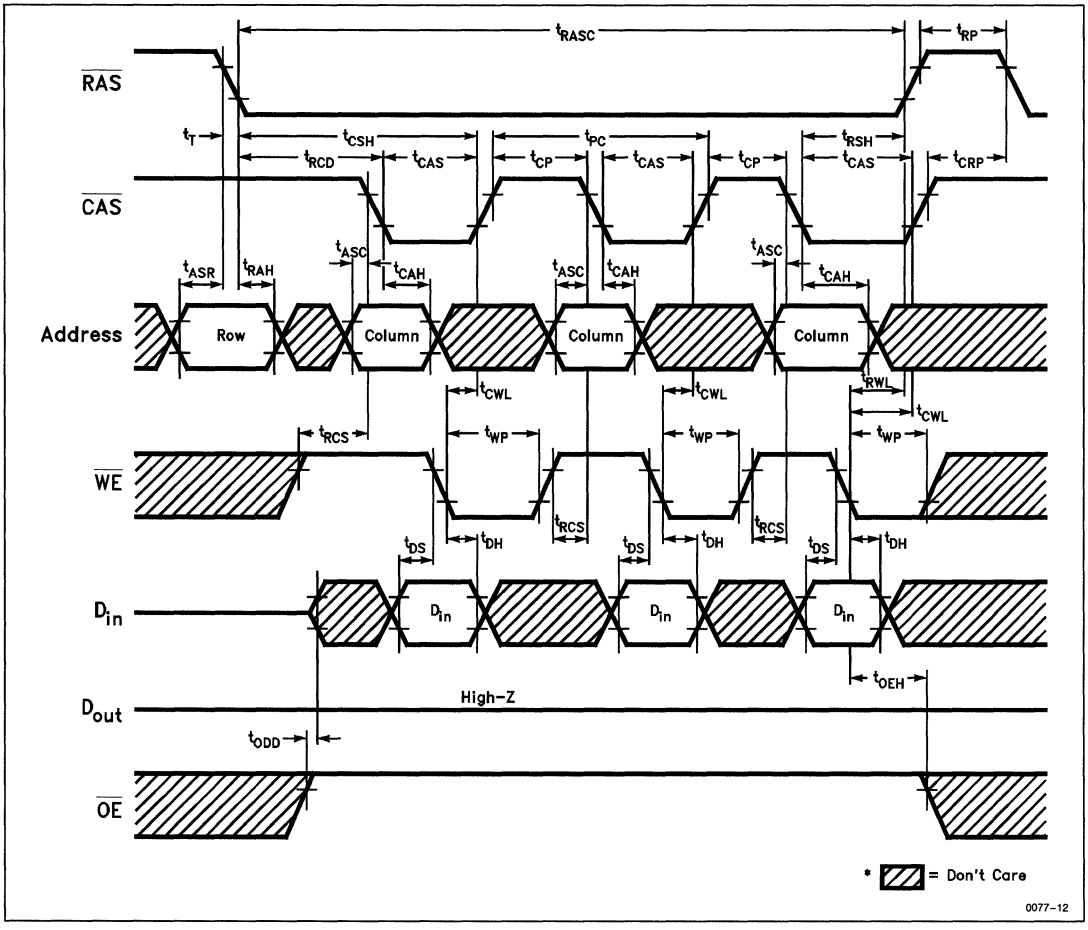
• **Fast Page Mode Read Cycle**



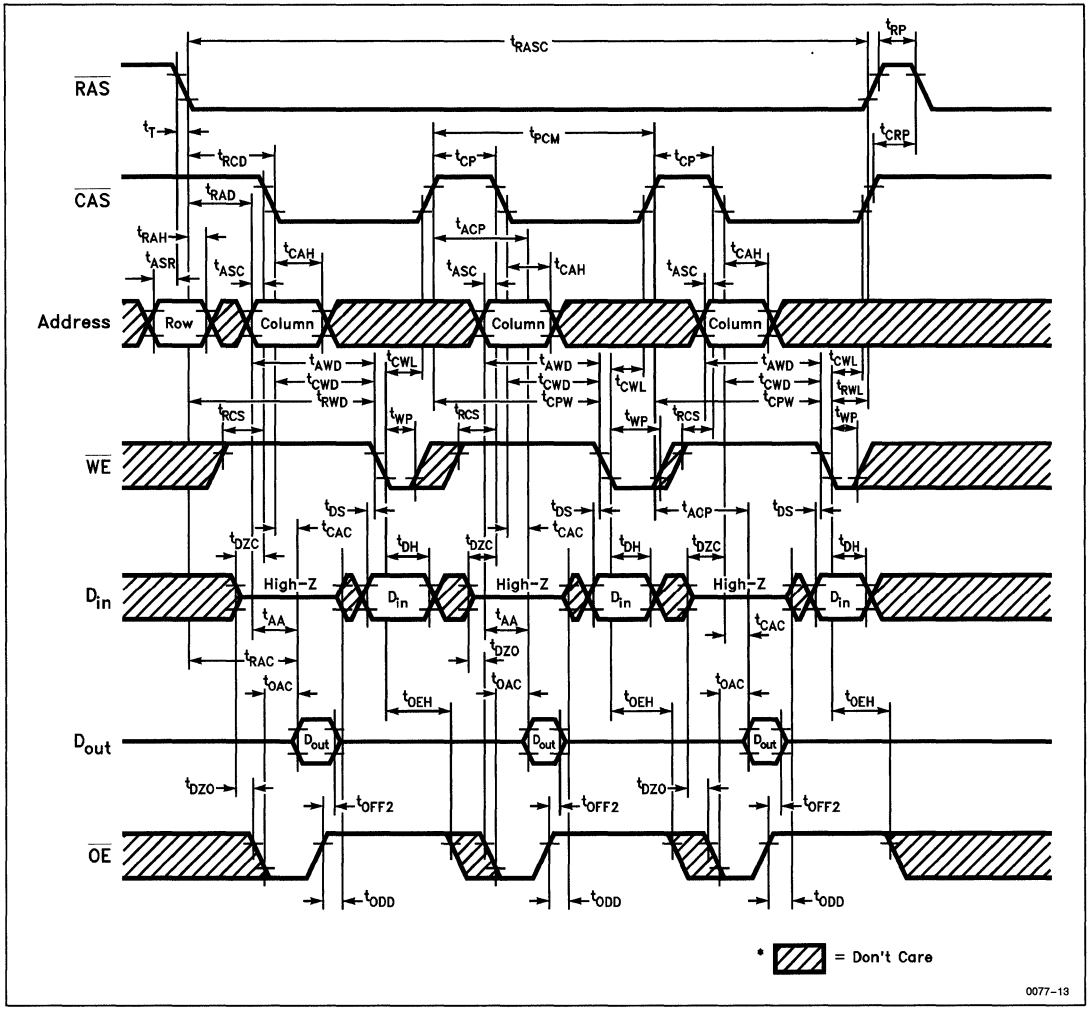
• **Fast Page Mode Early Write Cycle**



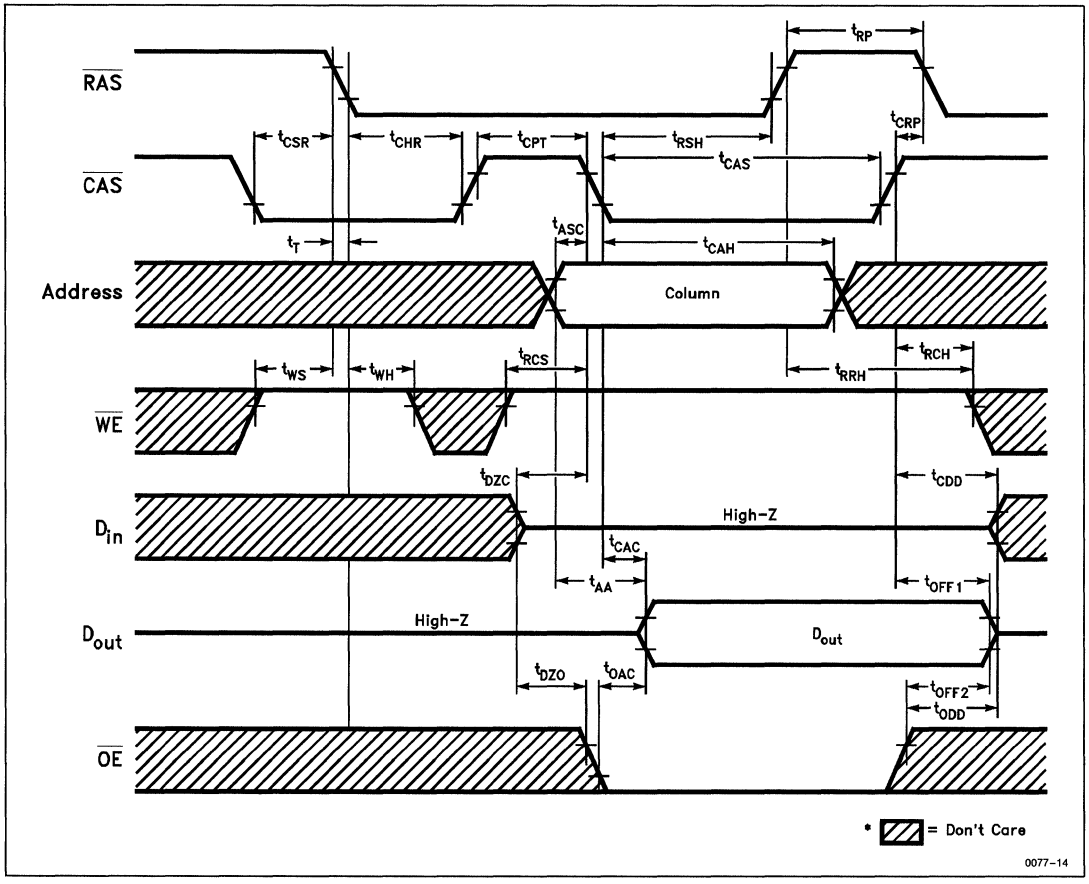
• **Fast Page Mode Delayed Write Cycle**



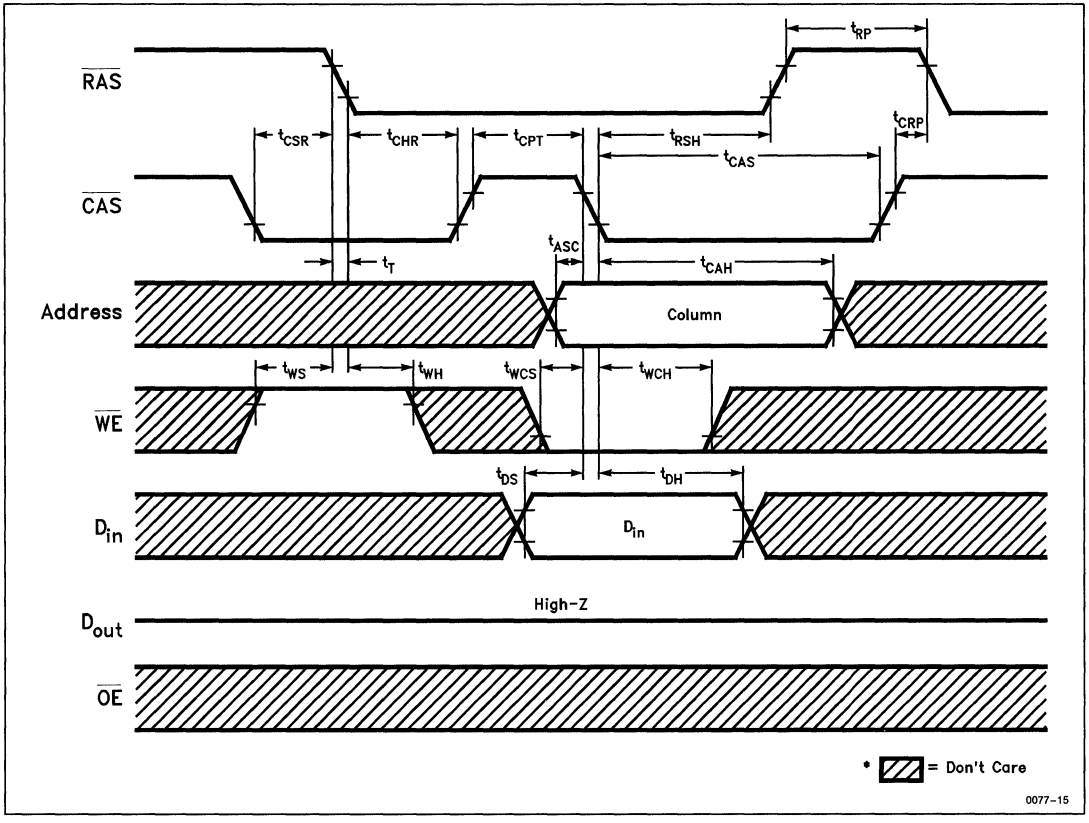
• **Fast Page Mode Read-Modify-Write Cycle**



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM514800L Series Low Power Version — Preliminary

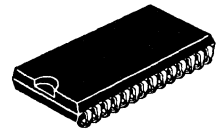
524,288-Word x 8-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514800 are CMOS dynamic RAM organized as 524,288-word x 8-bit. HM514800 have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514800 offer Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514800 to be packaged in standard 400 mil 28-pin plastic SOJ, standard 400 mil 28-pin plastic ZIP.

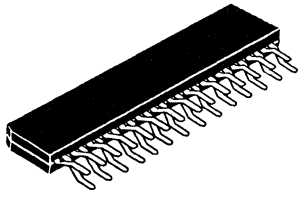
HM514800LJP Series



3DCP28D

(CP-28D)

HM514800LZP Series



3DZP28

(ZP-28)

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time ..... 70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode ..... 605 mW/550 mW/495 mW (max)
  - Standby Mode ..... 11 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles ..... (128 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Battery Back-up Operation

■ ORDERING INFORMATION

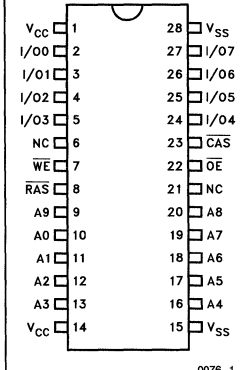
Part No.	Access Time	Package
HM514800LJP-7	70 ns	400 mil 28-pin
HM514800LJP-8	80 ns	Plastic SOJ
HM514800LJP-10	100 ns	(CP-28D)
HM514800LZP-7	70 ns	400 mil 28-pin
HM514800LZP-8	80 ns	Plastic ZIP
HM514800LZP-10	100 ns	(ZP-28)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input —Row Address A_0–A_9 —Column Address A_0–A_8 —Refresh Address A_0–A_9
I/O_0–I/O_7	Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

■ PIN OUT

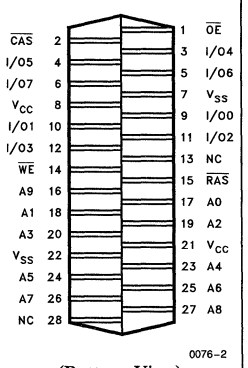
HM514800LJP Series



0076-1

(Top View)

HM514800LZP Series



0076-2

(Bottom View)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	− 1.0	—	0.8	V	1
	(Others)	V_{IL}	− 2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM514800-7		HM514800-8		HM514800-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	110	—	100	—	90	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	200	—	200	—	200	μA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	110	—	100	—	90	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	110	—	100	—	90	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	110	—	100	—	90	mA	t_{PC} = Min	1, 3
Battery Back-up Current (Standby with CBR Refresh)	I_{CC10}	—	300	—	300	—	300	μA	Standby: CMOS Interface D_{out} = High-Z CBR Refresh: t_{RC} = 125 μs t_{RAS} ≤ 1 μs, $\overline{CAS}$ = V_{IL} $\overline{WE}$ = V_{IH}	4
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. V_{IH} ≥ V_{CC} − 0.2V, V_{IL} ≤ 0.2V.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 14, 15]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514800-7		HM514800-8		HM514800-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	20	60	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	15	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	20	—	20	—	25	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	128	—	128	—	125	ms	

Read Cycle

Parameter	Symbol	HM514800-7		HM514800-8		HM514800-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	3, 4, 13
Access Time from Address	t_{AA}	—	35	—	40	—	45	ns	3, 5, 13
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	35	—	40	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	15	0	15	0	20	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	15	0	15	0	20	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	15	—	15	—	20	—	ns	

Write Cycle

Parameter	Symbol	HM514800-7		HM514800-8		HM514800-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514800-7		HM514800-8		HM514800-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	180	—	200	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	95	—	105	—	135	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	45	—	45	—	60	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	60	—	65	—	80	—	ns	10, 13
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	20	—	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM514800-7		HM514800-8		HM514800-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time in Normal Mode	t_{CPN}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514800-7		HM514800-8		HM514800-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	ns	3, 13
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	ns	
Fast Page Mode Read-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPW}	65	—	70	—	85	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	95	—	100	—	110	—	ns	

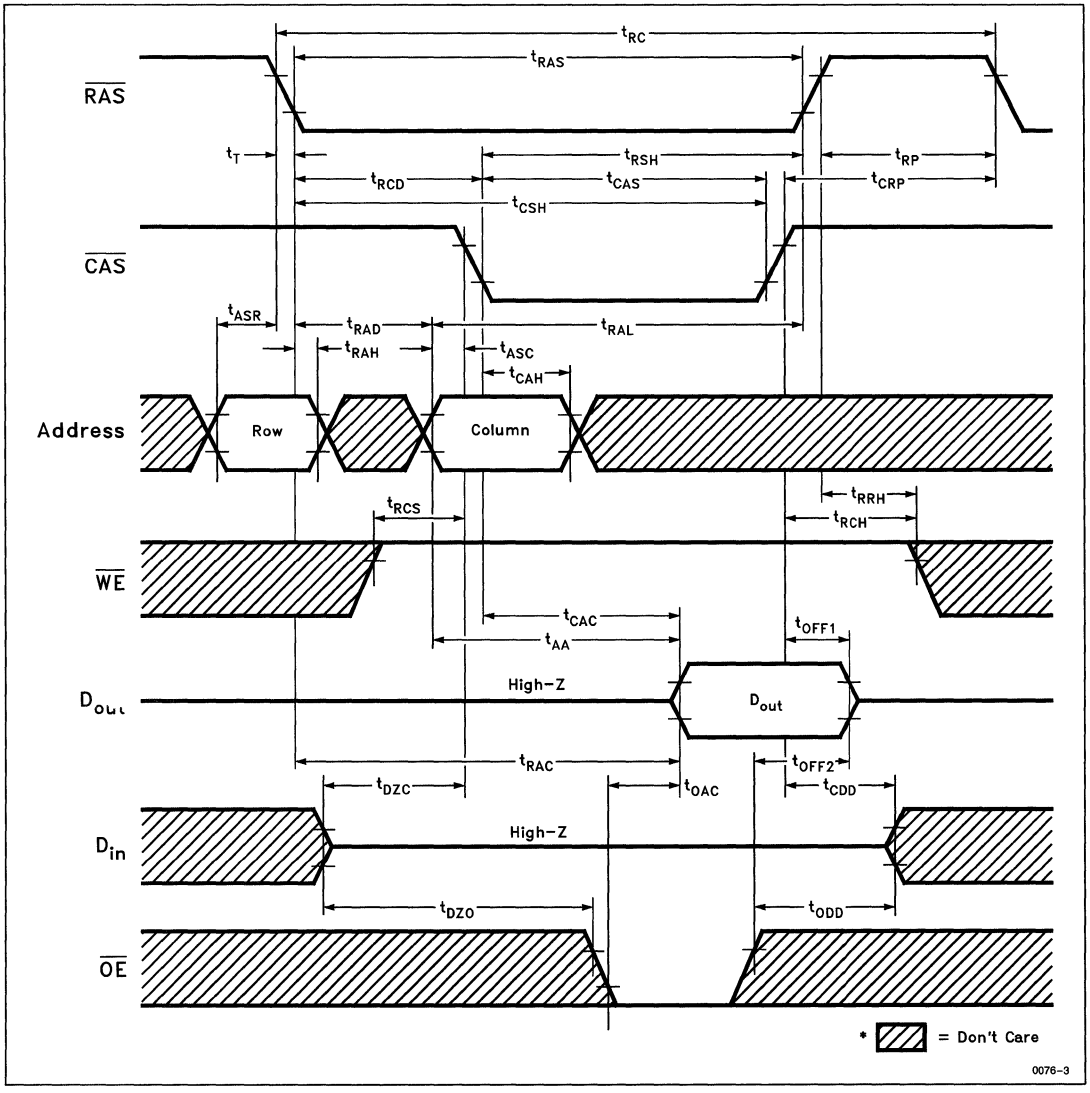
Counter Test Cycle

Parameter	Symbol	HM514800-7		HM514800-8		HM514800-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	50	—	50	—	50	—	ns	

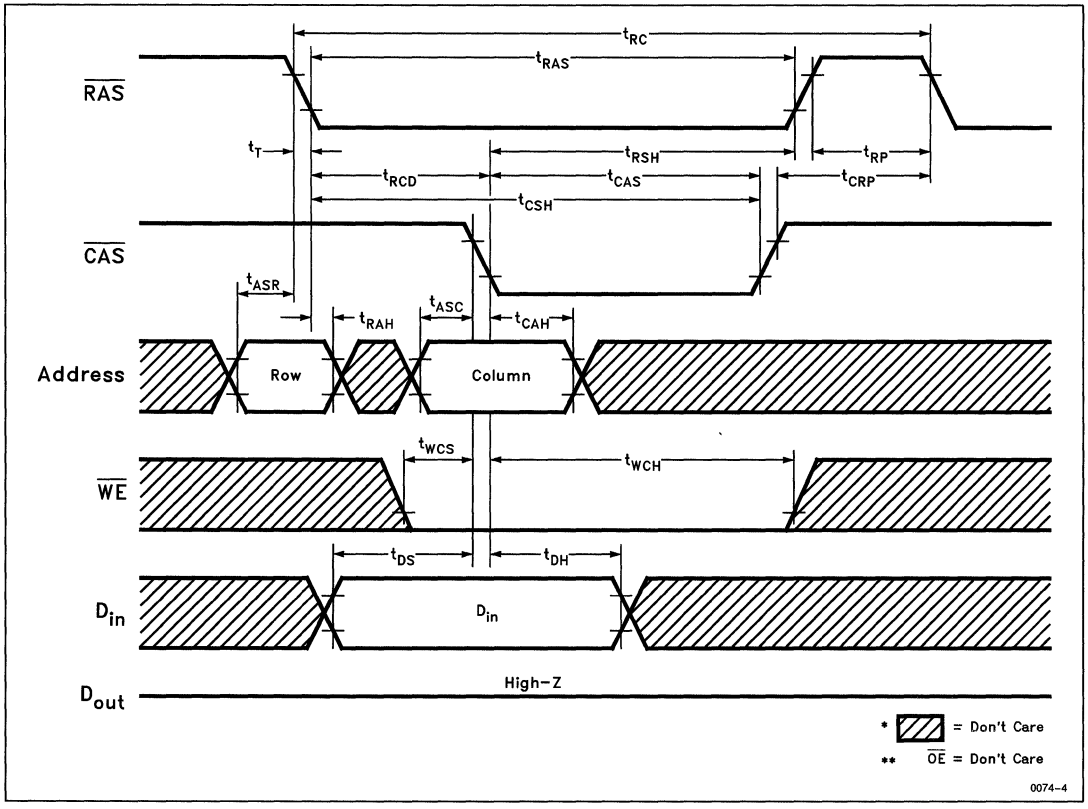
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL load and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Either t_{RCH} or T_{RRH} must be satisfied for a read cycle.

■ TIMING WAVEFORMS

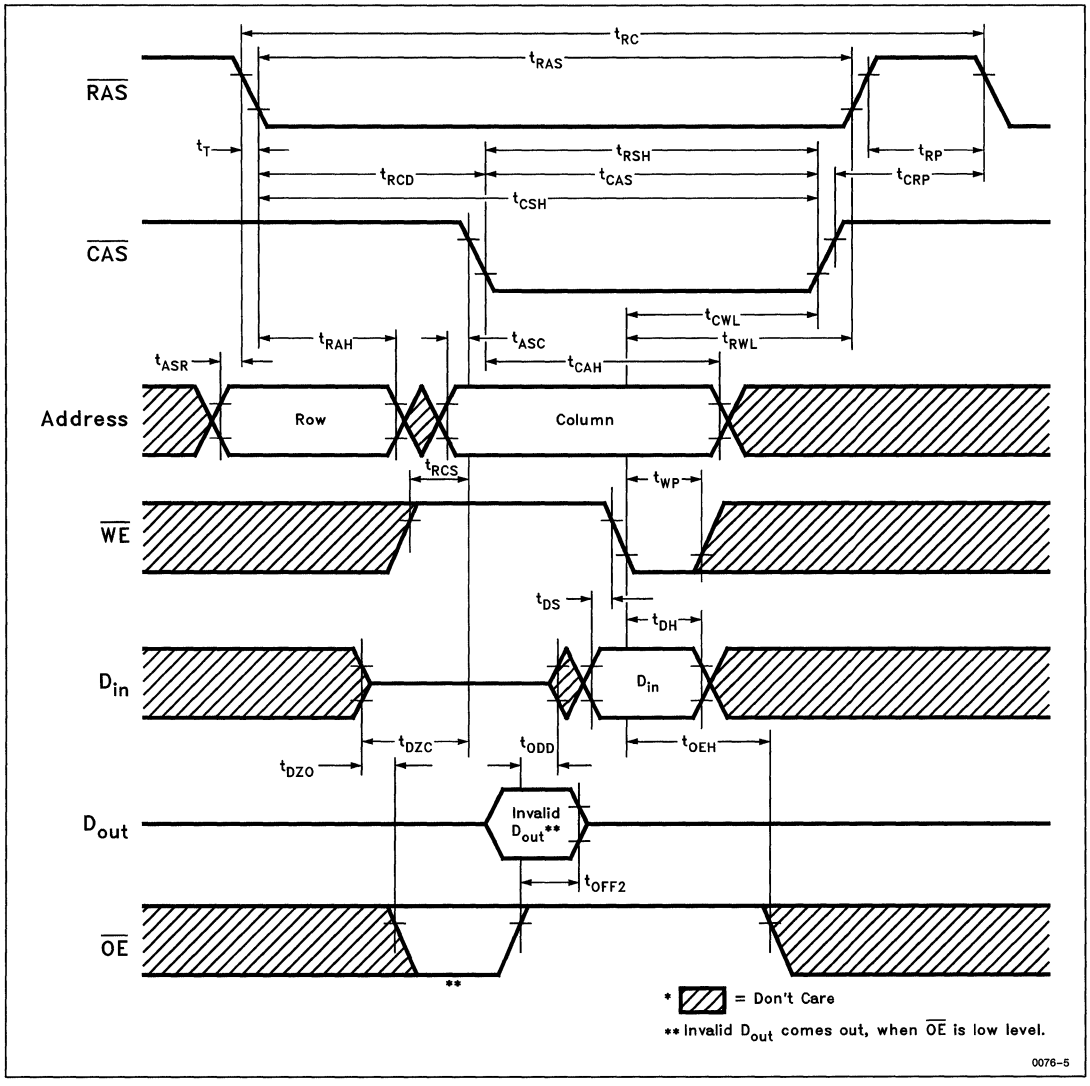
• Read Cycle



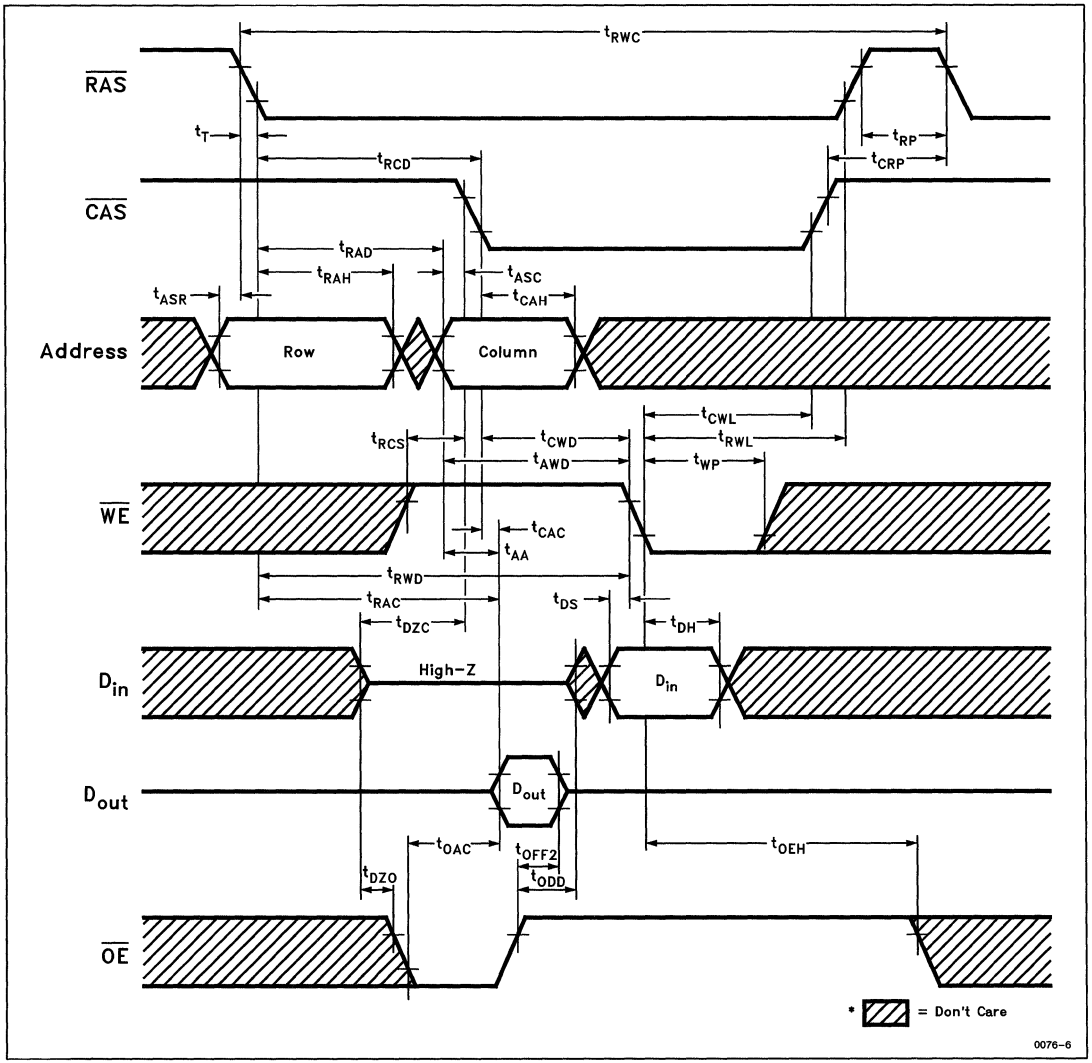
• **Early Write Cycle**



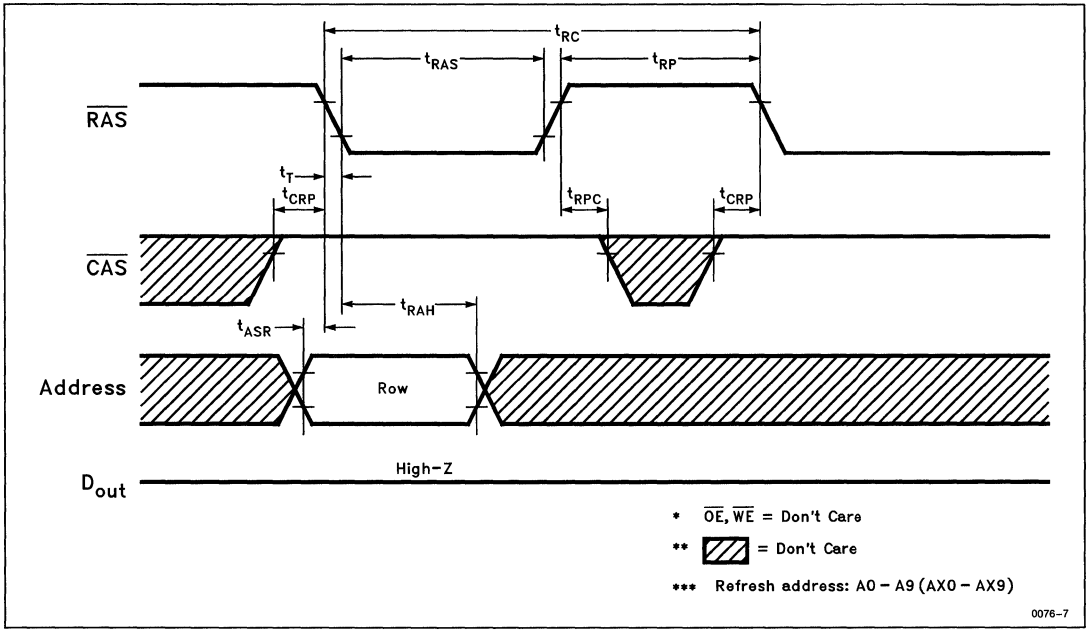
• **Delayed Write Cycle**



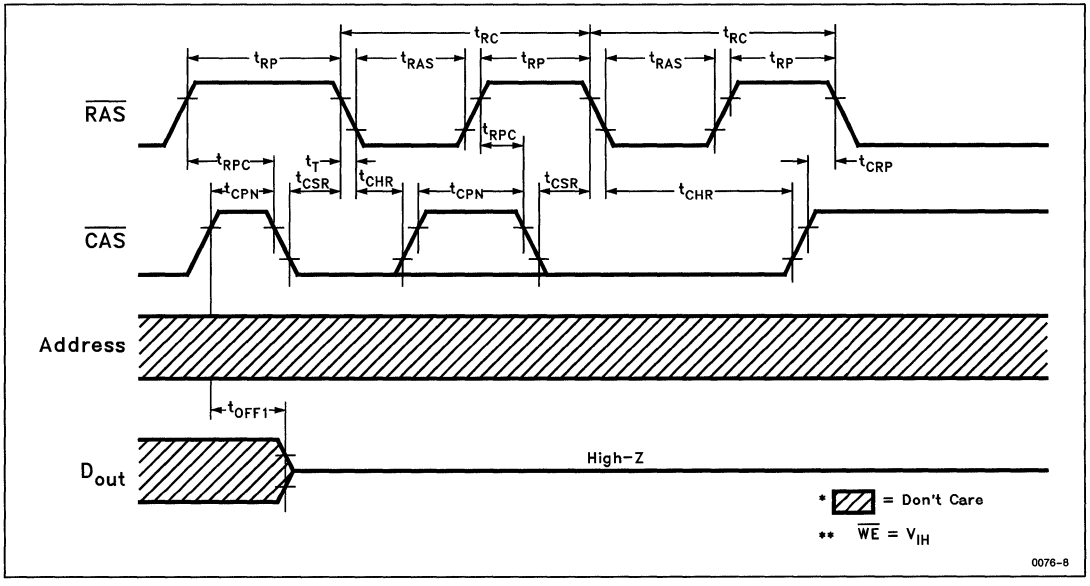
• **Read-Modify-Write Cycle**



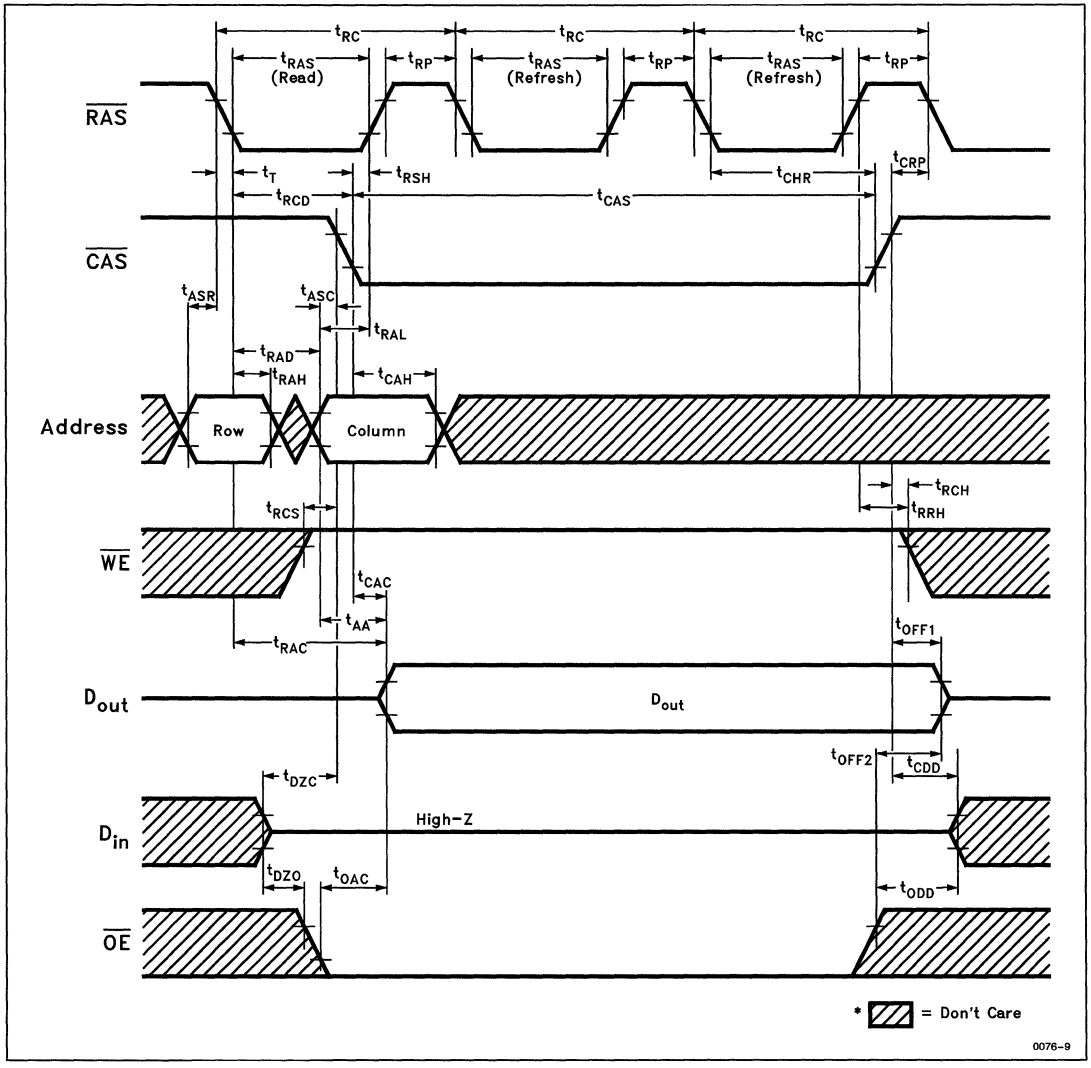
• $\overline{RAS}$ Only Refresh Cycle



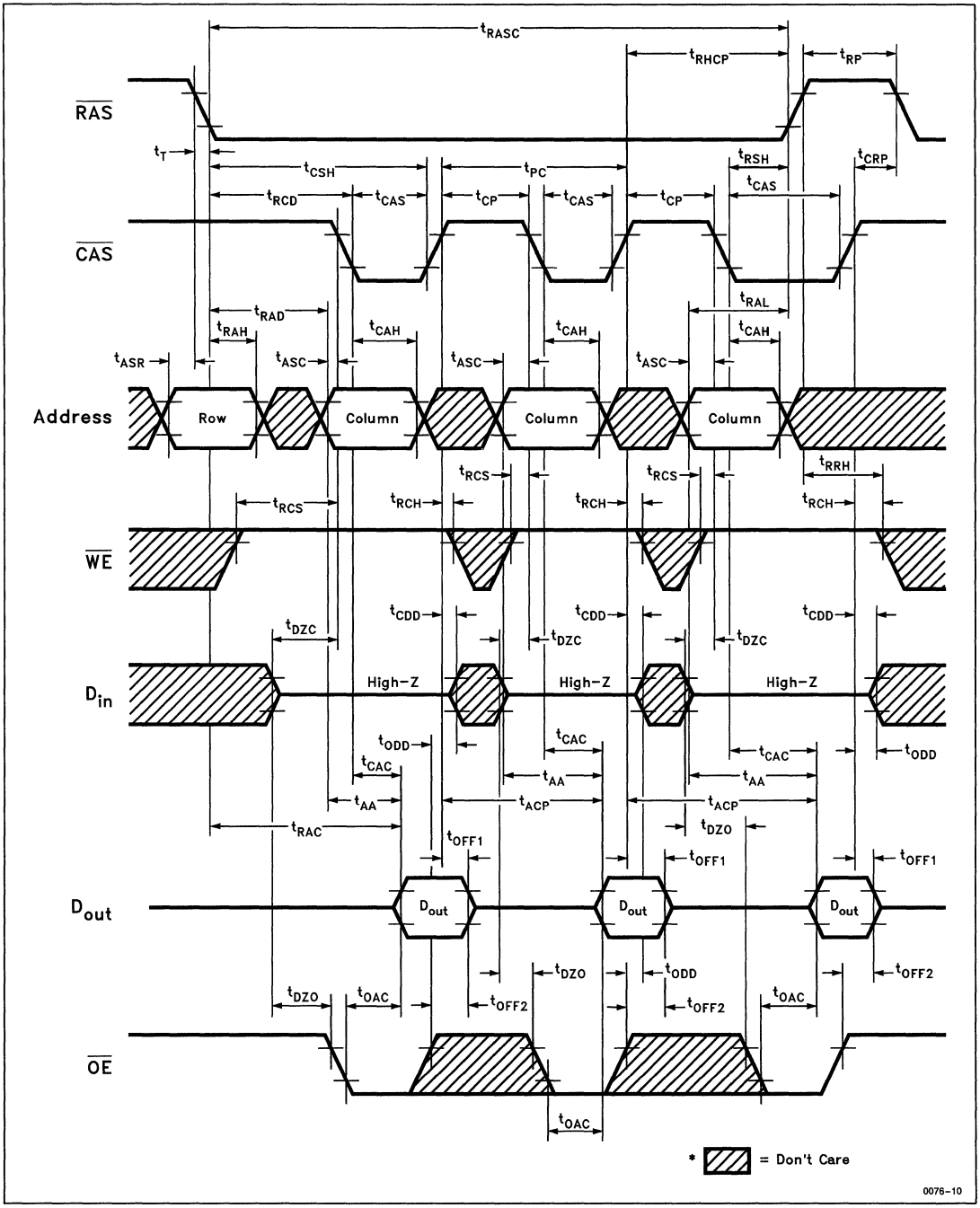
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



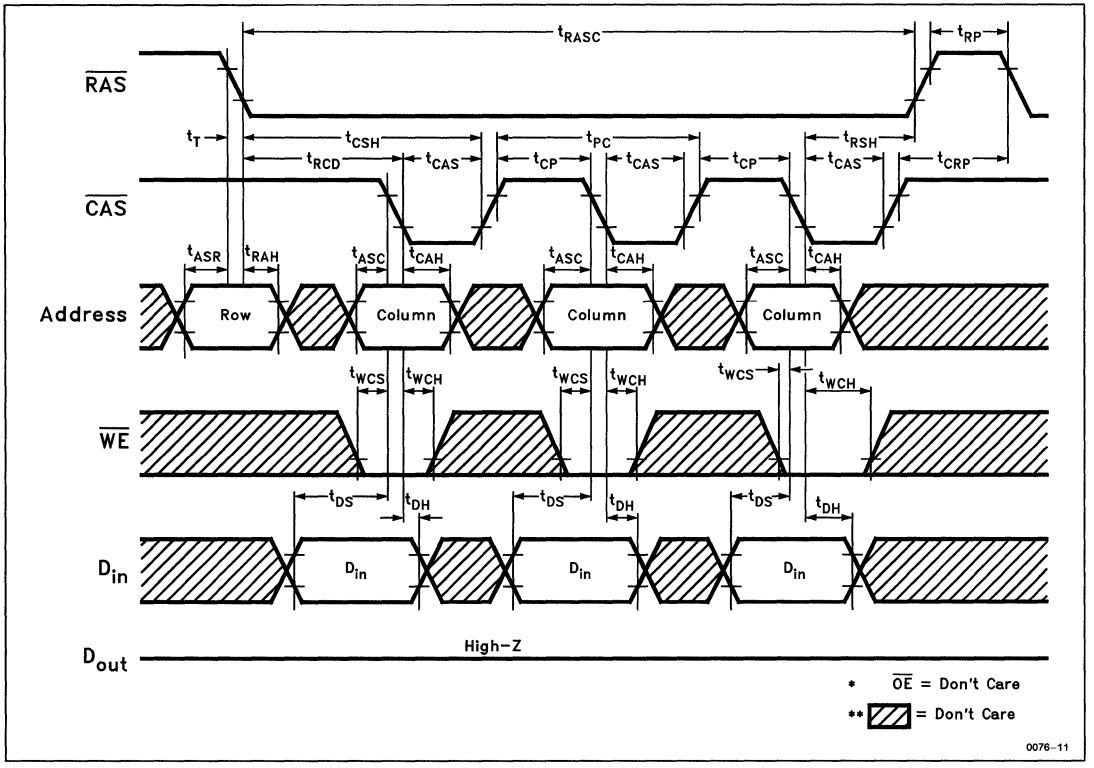
• **Hidden Refresh Cycle**



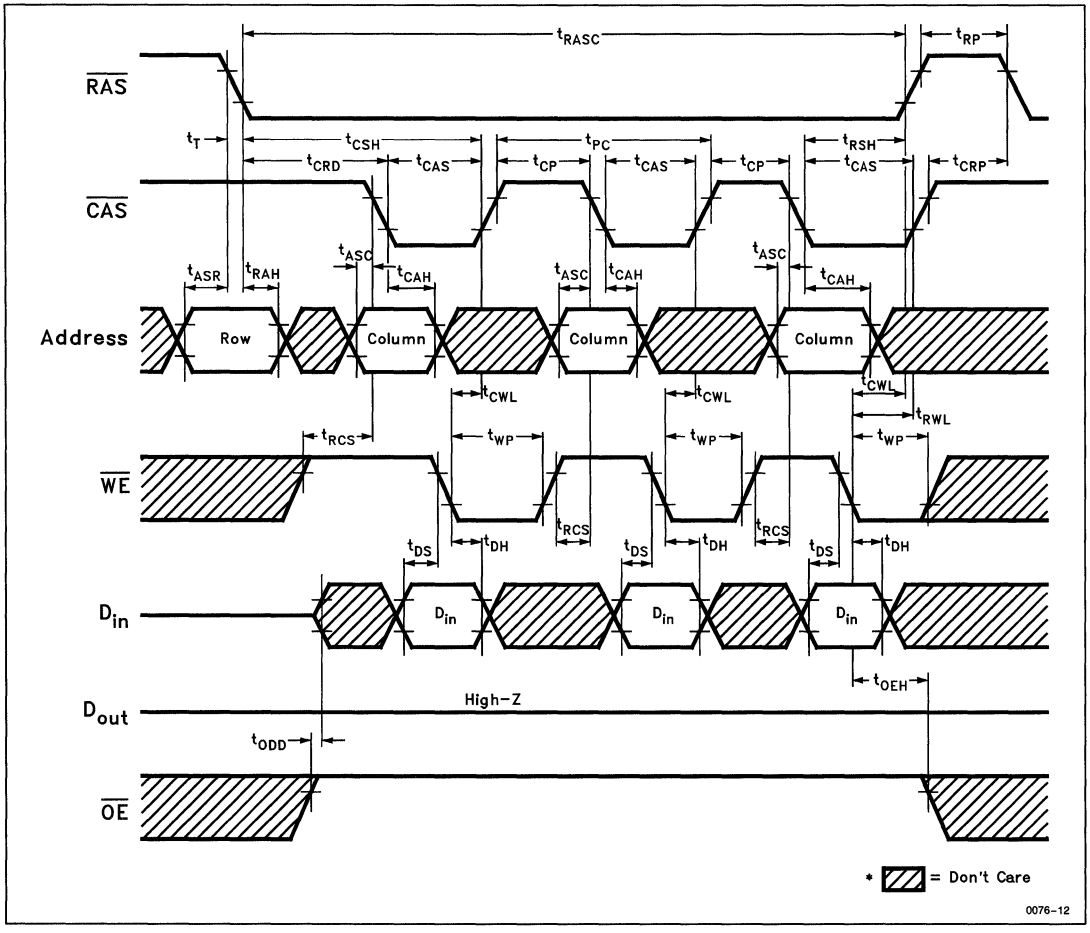
• **Fast Page Mode Read Cycle**



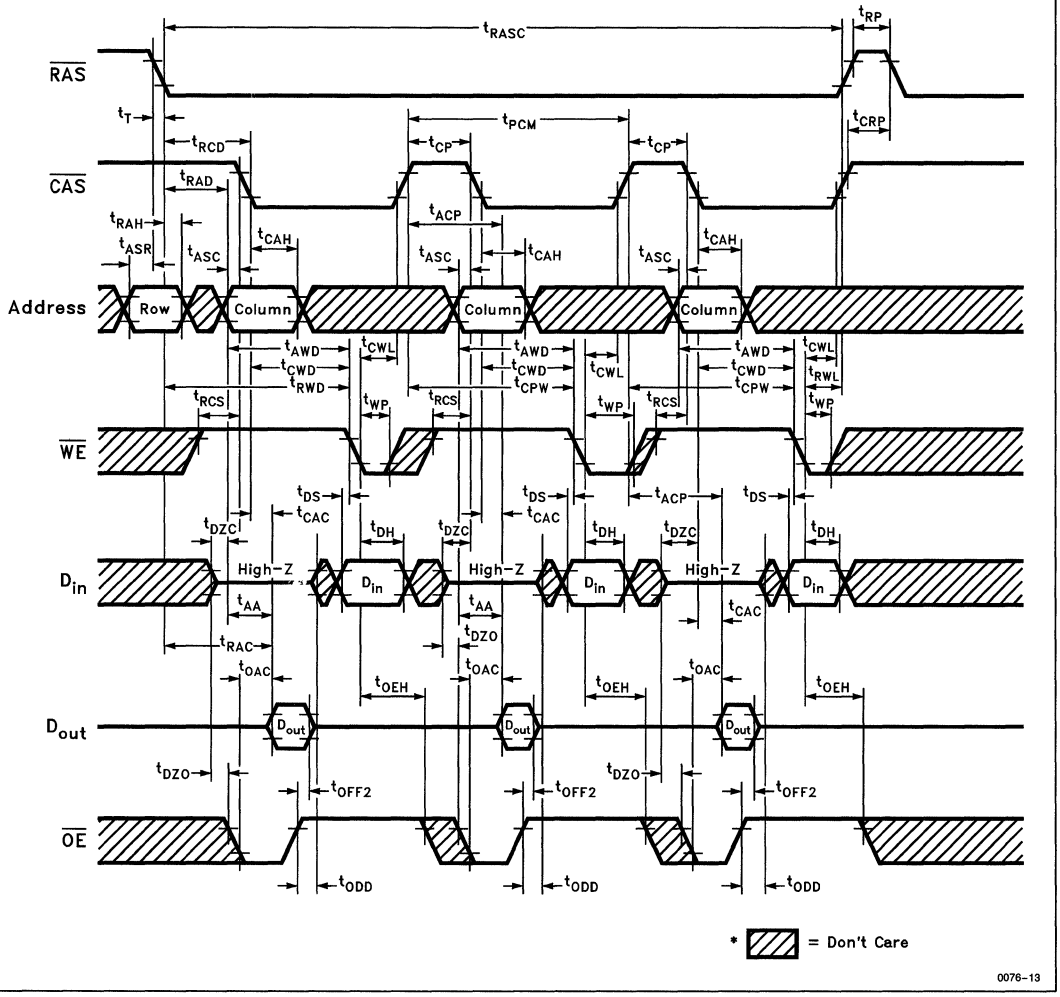
• Fast Page Mode Early Write Cycle



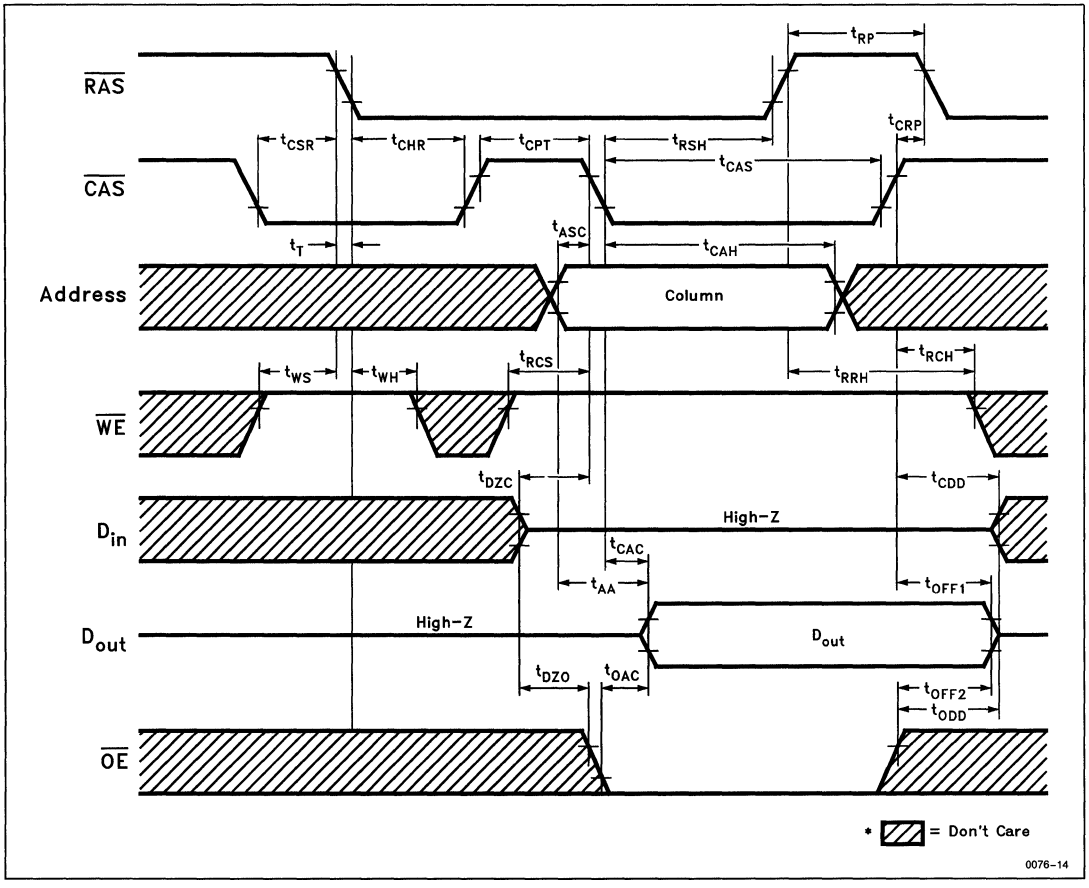
• **Fast Page Mode Delayed Write Cycle**



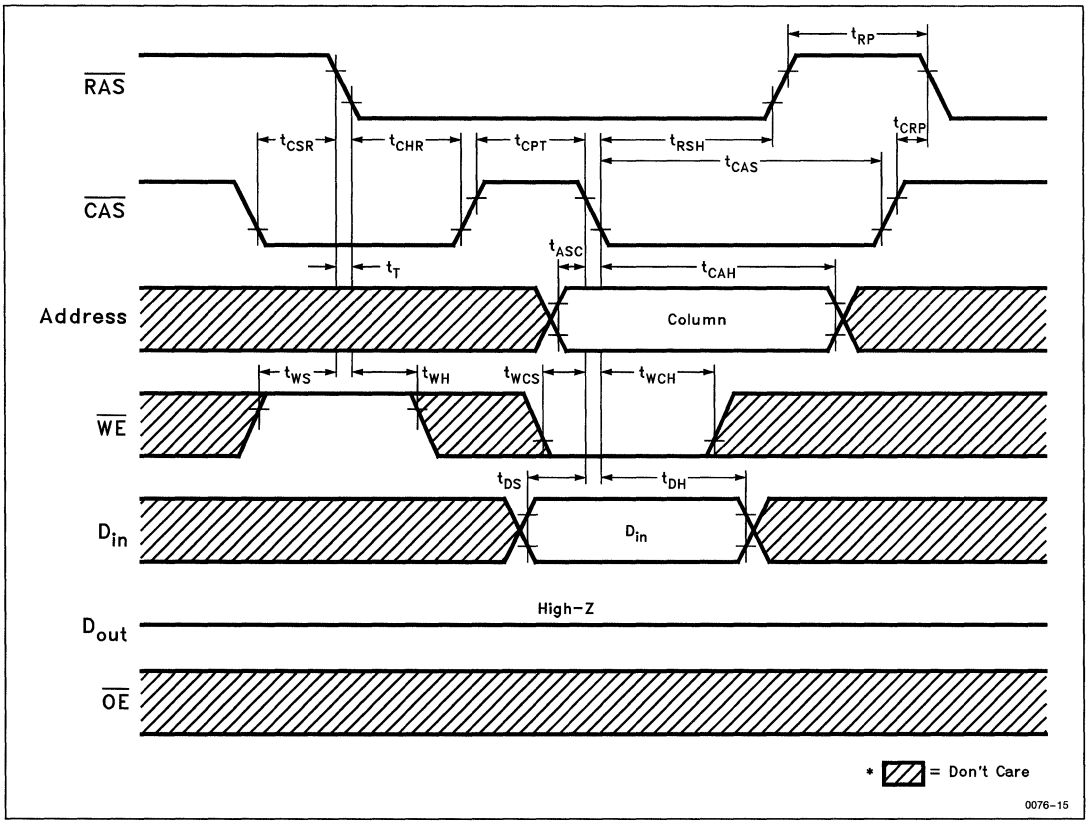
• **Fast Page Mode Read-Modify-Write Cycle**



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM514900 Series — Preliminary

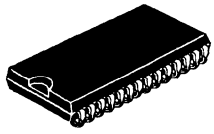
524,288-Word x 9-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514900 are CMOS dynamic RAM organized as 524,288-word x 9-bit. HM514900 have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514900 offer Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514900 to be packaged in standard 400 mil 28-pin plastic SOJ, standard 400 mil 28-pin plastic ZIP.

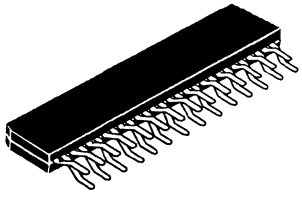
HM514900JP Series



3DCP28D

(CP-28D)

HM514900ZP Series



3DZP28

(ZP-28)

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode .....605 mW/550 mW/495 mW (max)
  - Standby Mode .....11 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles .....(16 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh

■ ORDERING INFORMATION

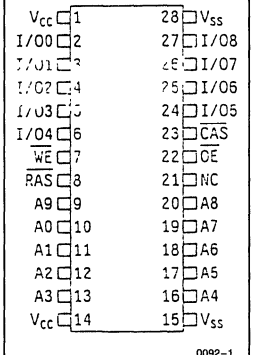
Part No.	Access Time	Package
HM514900JP-7	70 ns	400 mil 28-pin
HM514900JP-8	80 ns	Plastic SOJ
HM514900JP-10	100 ns	(CP-28D)
HM514900ZP-7	70 ns	400 mil 28-pin
HM514900ZP-8	80 ns	Plastic ZIP
HM514900ZP-10	100 ns	(ZP-28)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input —Row Address A_0–A_9 —Column Address A_0–A_8 —Refresh Address A_0–A_9
I/O_0–I/O_8	Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

■ PIN OUT

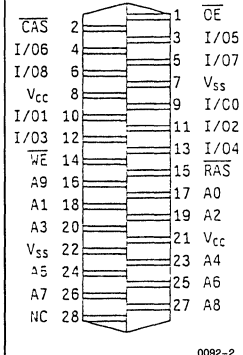
HM514900JP Series



0092-1

(Top View)

HM514900ZP Series



0092-2

(Bottom View)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	− 1.0	—	0.8	V	1
	(Others)	V_{IL}	− 2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM514900-7		HM514900-8		HM514900-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	110	—	100	—	90	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	1	—	1	—	1	mA	CMOS Interface, $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	110	—	100	—	90	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	110	—	100	—	90	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	110	—	100	—	90	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 14, 15]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514900-7		HM514900-8		HM514900-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	20	60	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	15	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	20	—	20	—	25	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514900-7		HM514900-8		HM514900-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	3, 4, 13
Access Time from Address	t_{AA}	—	35	—	40	—	45	ns	3, 5, 13
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	35	—	40	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	15	0	15	0	20	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	15	0	15	0	20	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	15	—	15	—	20	—	ns	

Write Cycle

Parameter	Symbol	HM514900-7		HM514900-8		HM514900-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514900-7		HM514900-8		HM514900-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	180	—	200	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	95	—	105	—	135	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	45	—	45	—	60	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	60	—	65	—	80	—	ns	10, 13
$\overline{OE}$ to Hold Time from $\overline{WE}$	t_{OEH}	20	—	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM514900-7		HM514900-8		HM514900-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time in Normal Mode	t_{CPN}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514900-7		HM514900-8		HM514900-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	ns	3, 13
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	ns	
Fast Page Mode Read-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPW}	65	—	70	—	85	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	95	—	100	—	110	—	ns	

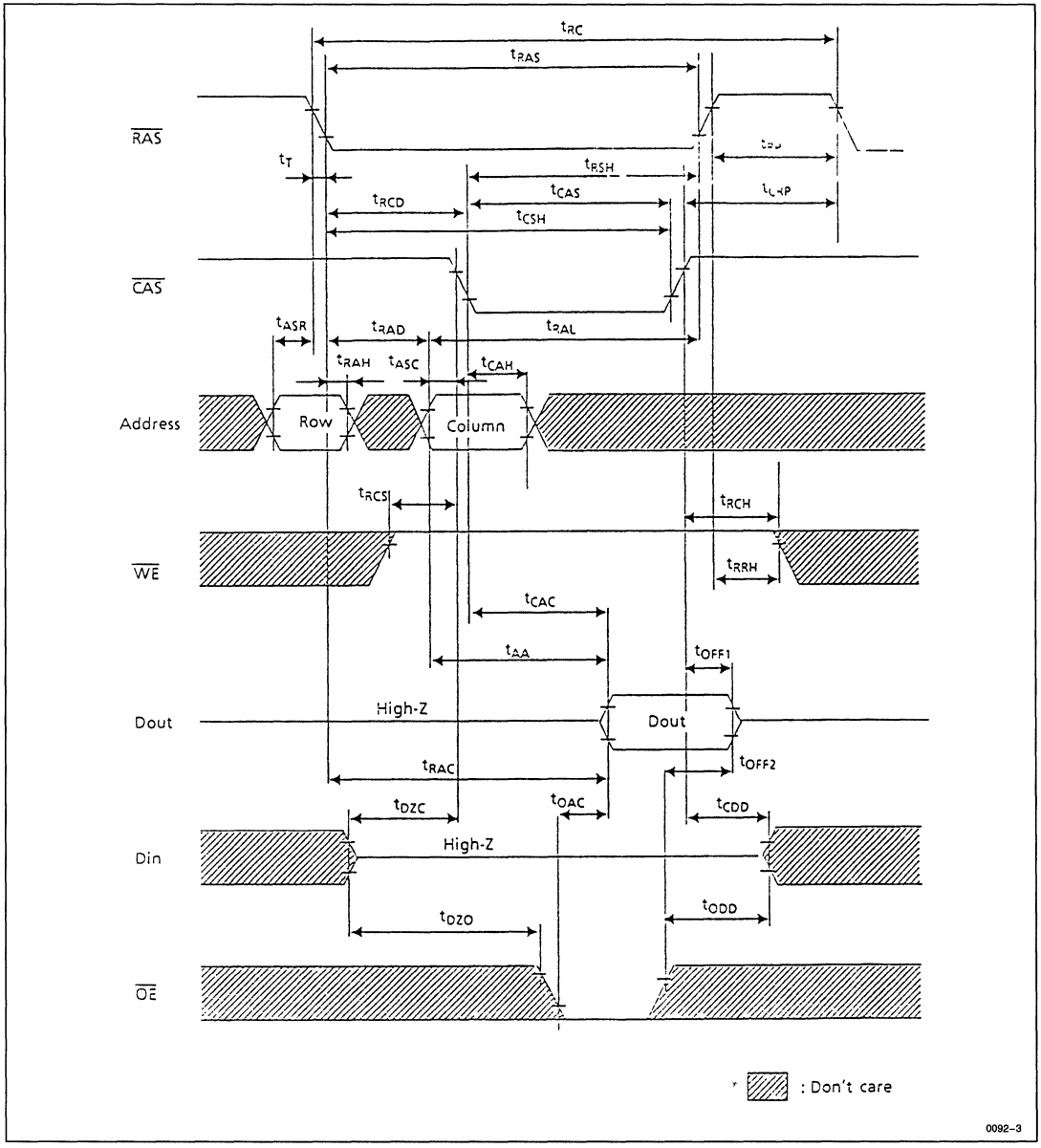
Counter Test Cycle

Parameter	Symbol	HM514900-7		HM514900-8		HM514900-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	50	—	50	—	50	—	ns	

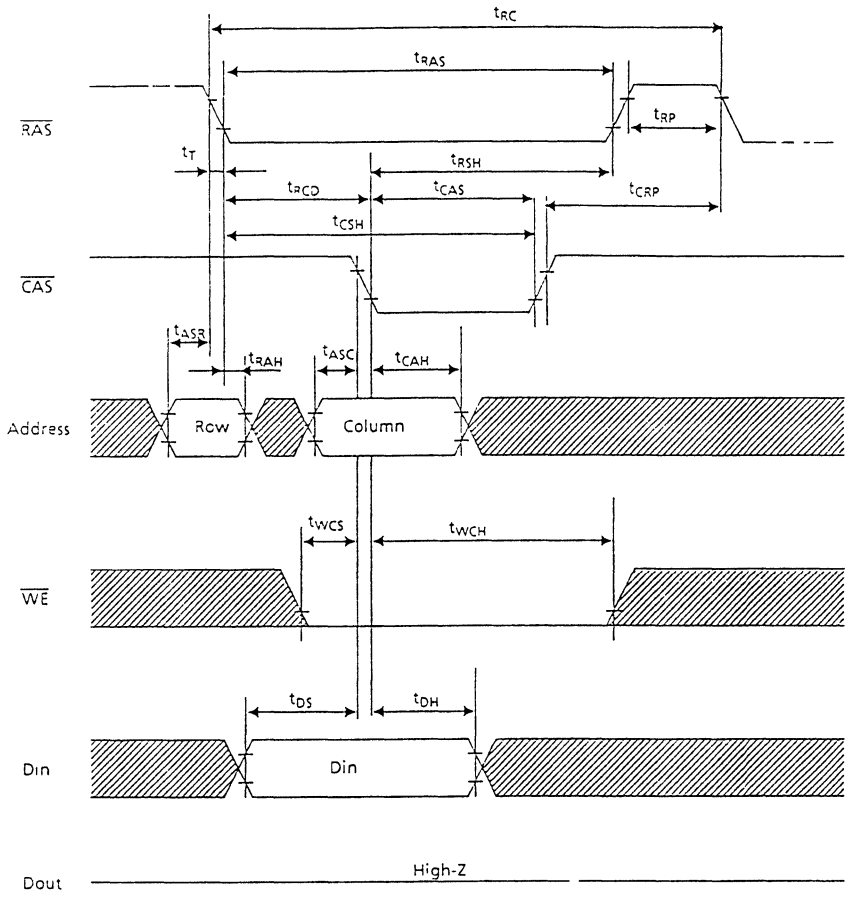
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL load and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Either t_{RCH} or T_{RRH} must be satisfied for a read cycle.

■ TIMING WAVEFORMS

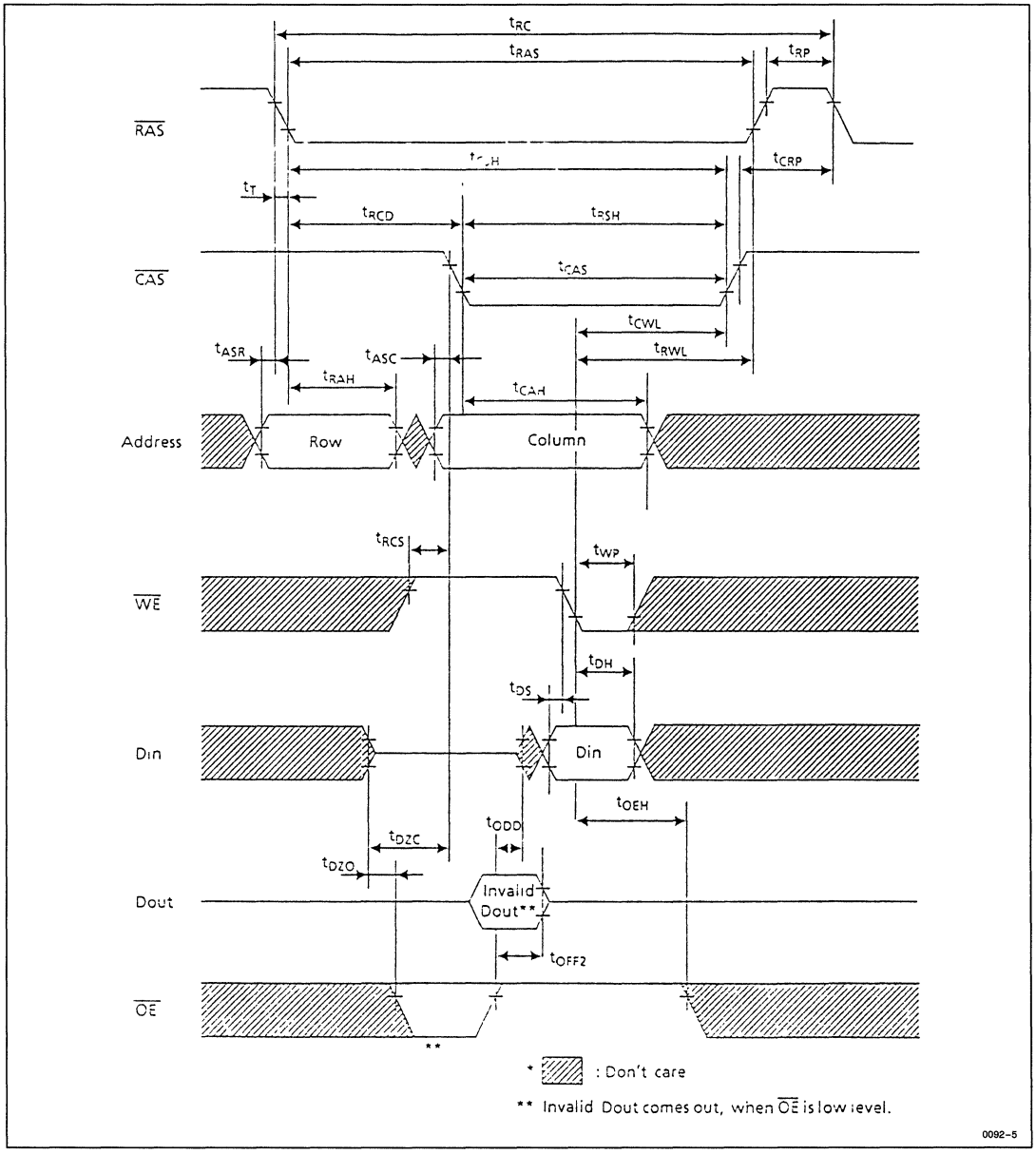
• Read Cycle



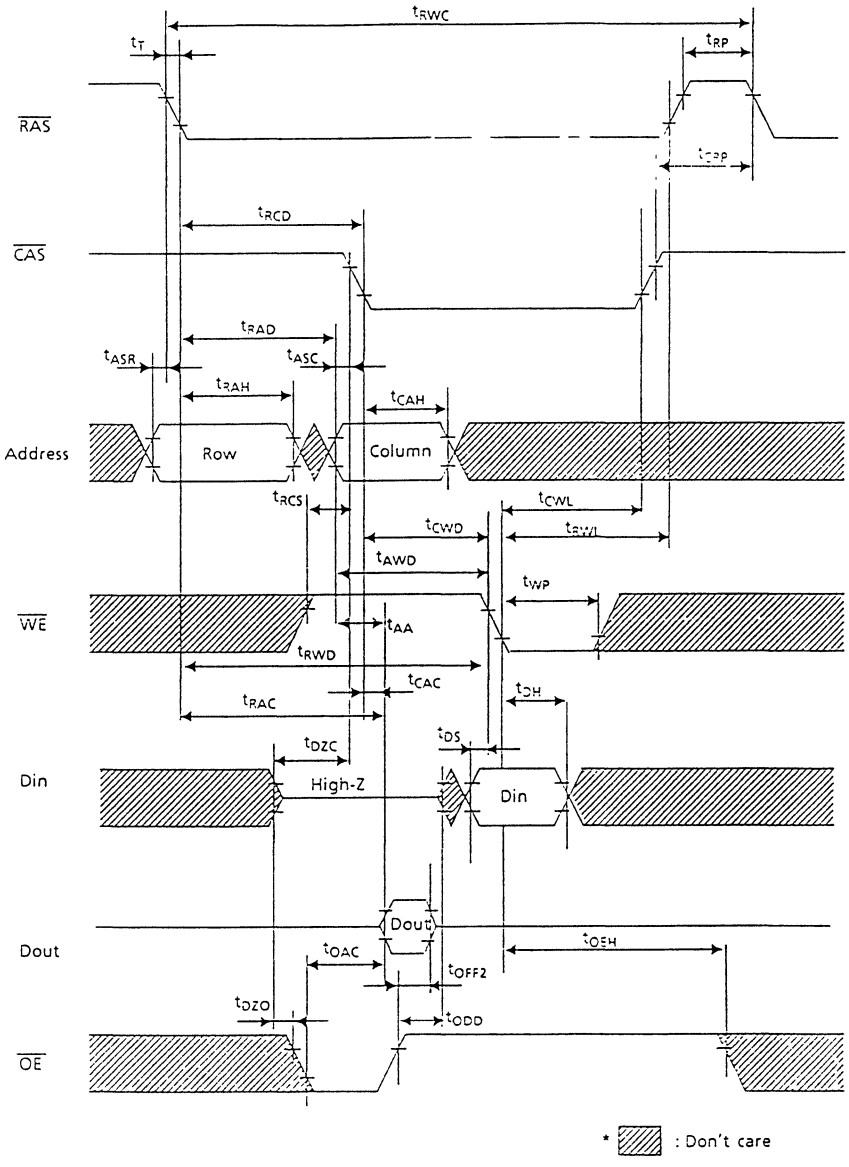
• **Early Write Cycle**



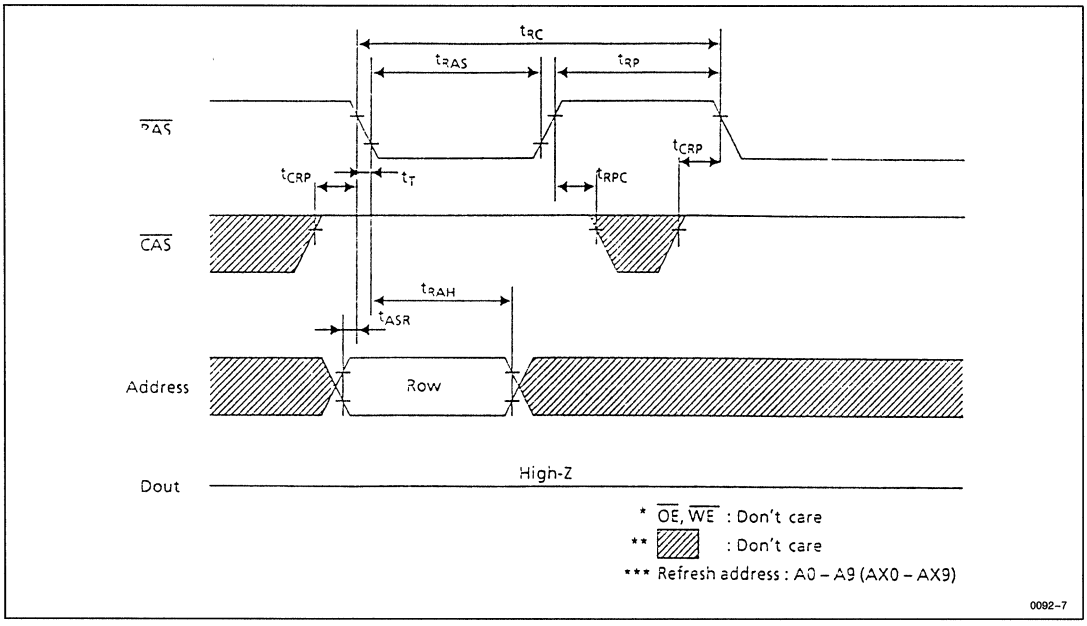
• **Delayed Write Cycle**



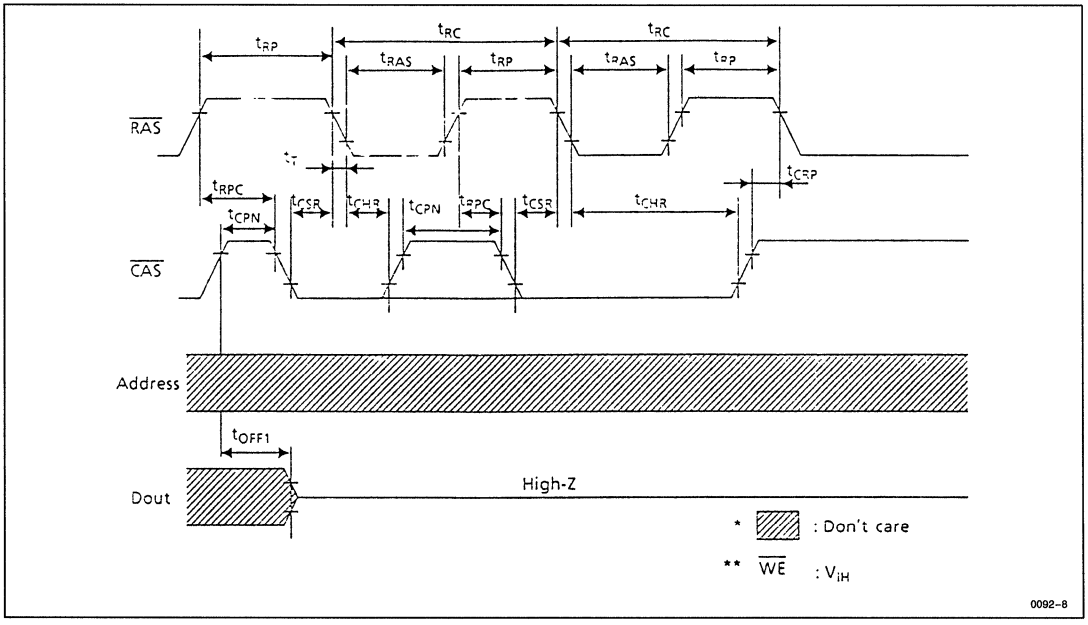
• **Read-Modify-Write Cycle**



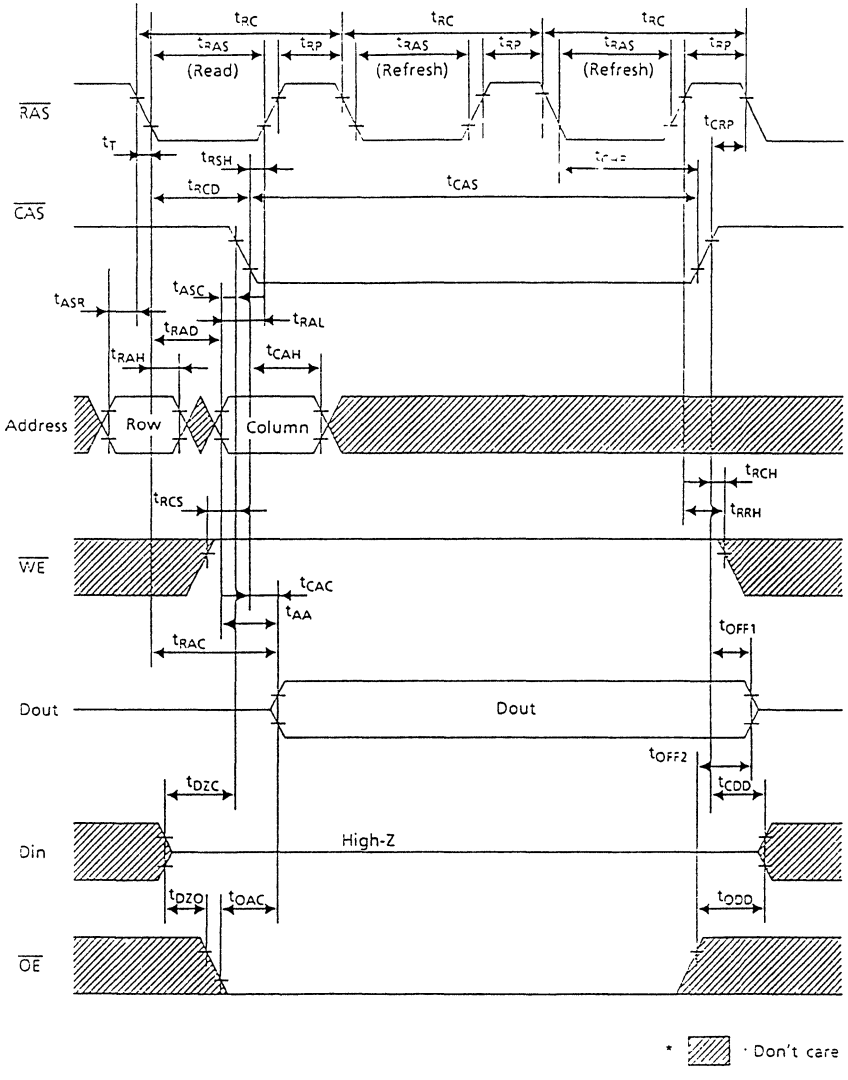
• $\overline{RAS}$ Only Refresh Cycle



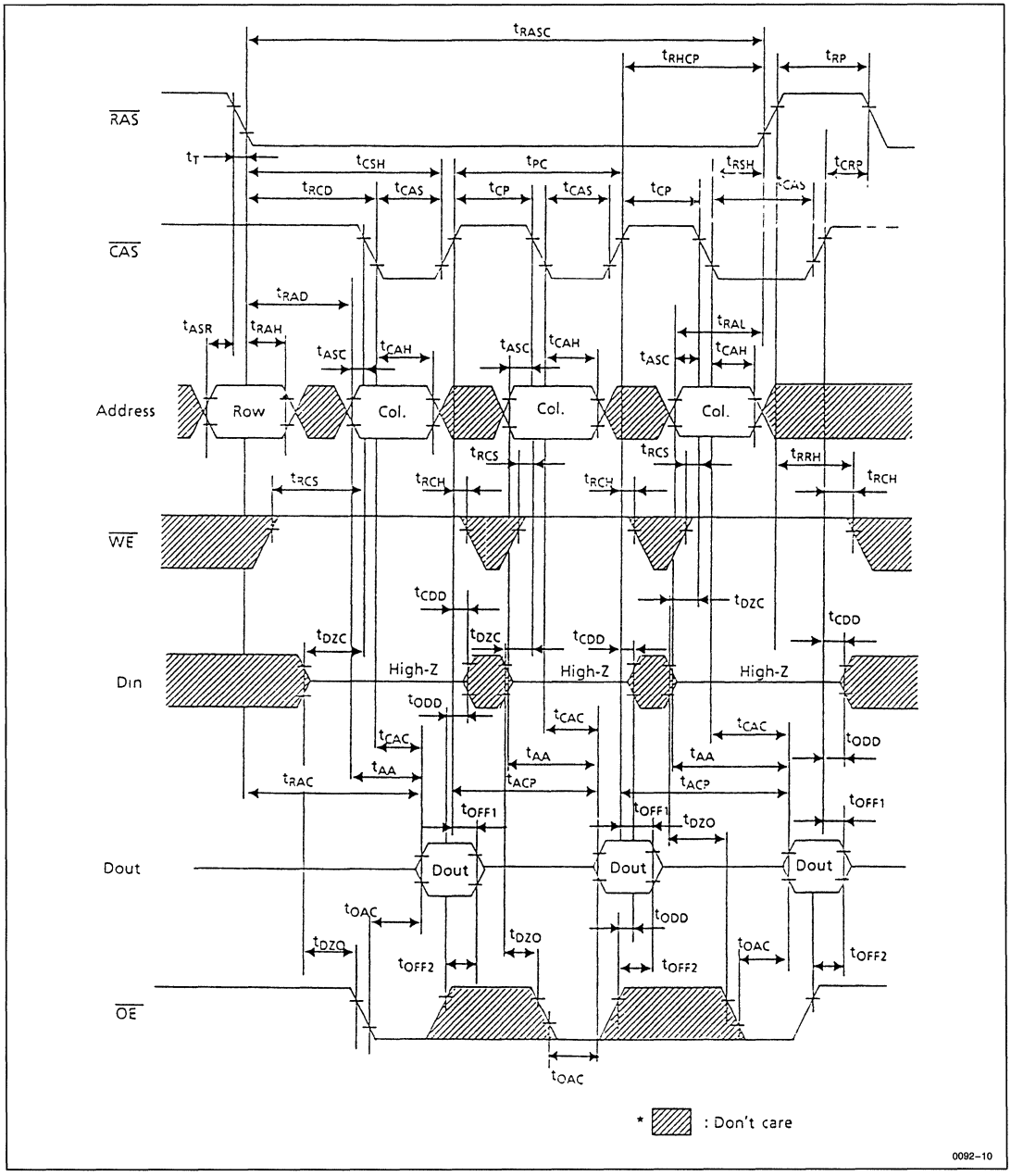
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



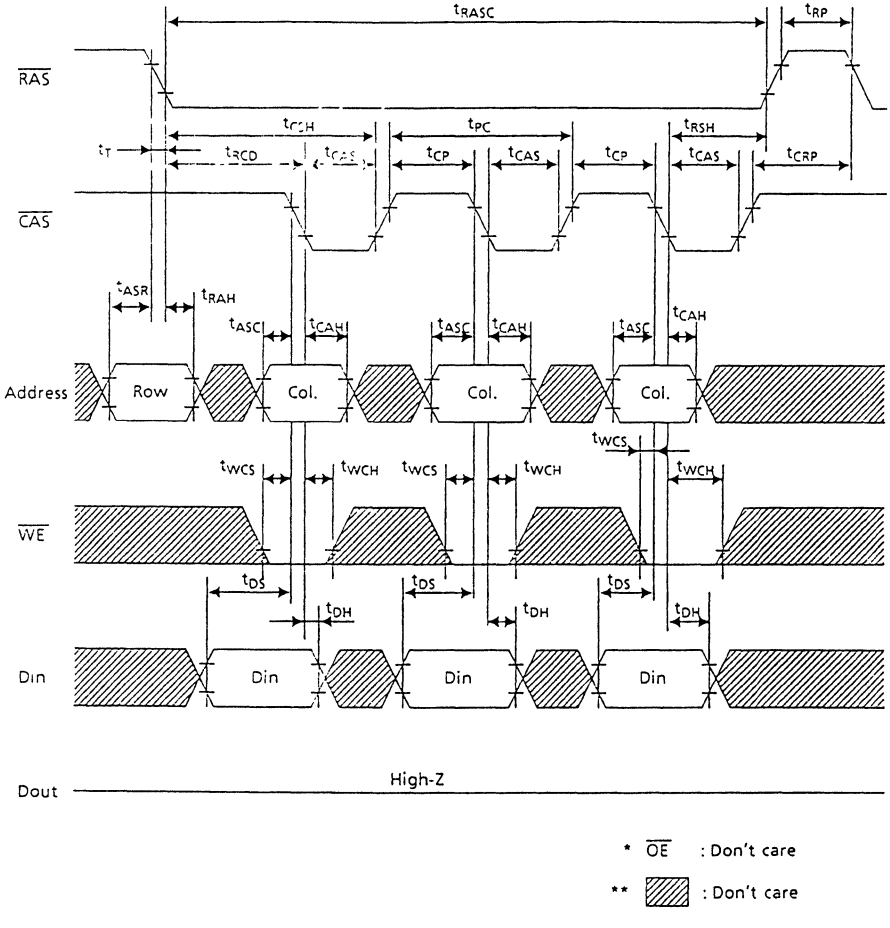
• Hidden Refresh Cycle



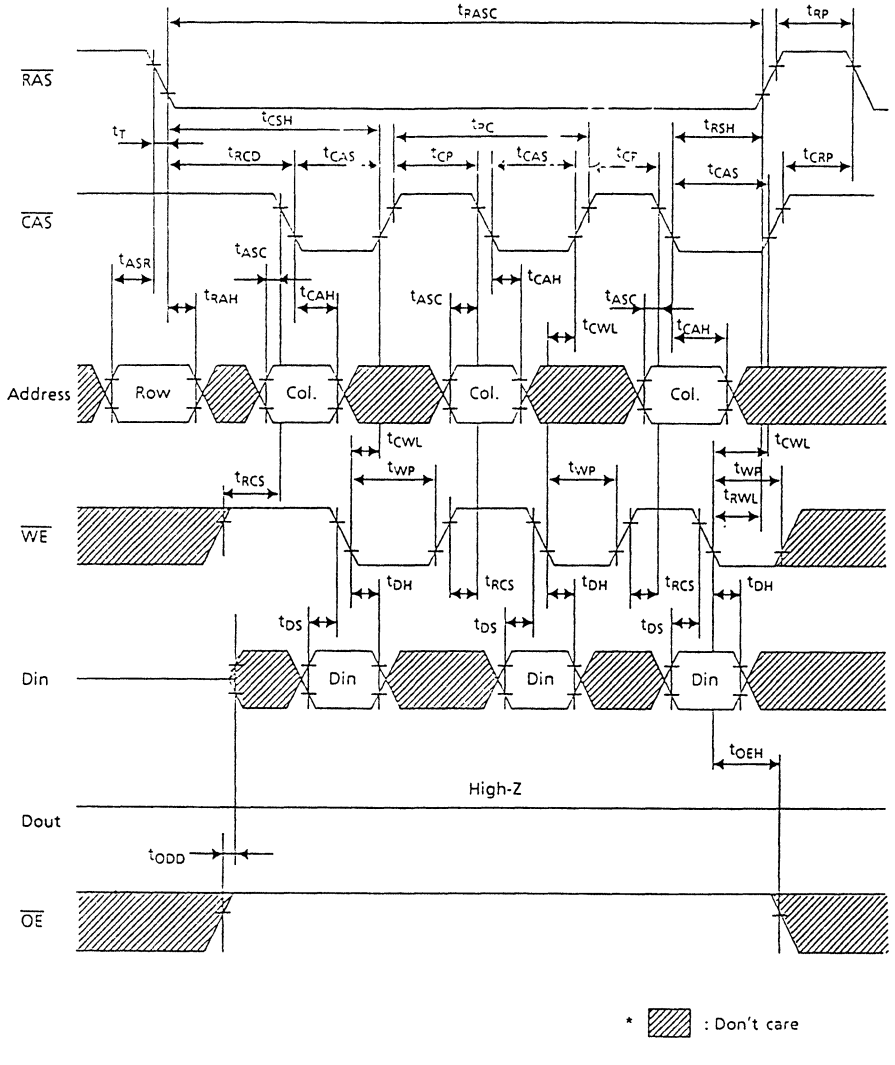
• Fast Page Mode Read Cycle



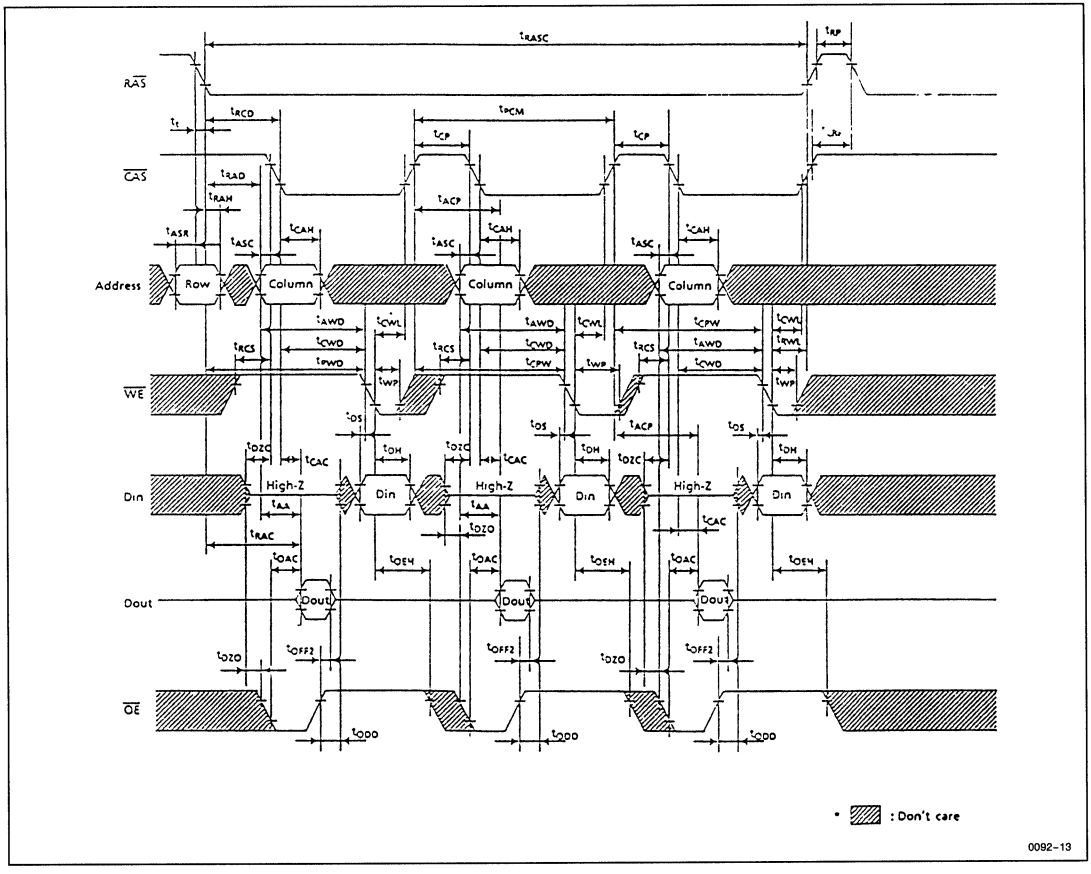
• **Fast Page Mode Early Write Cycle**



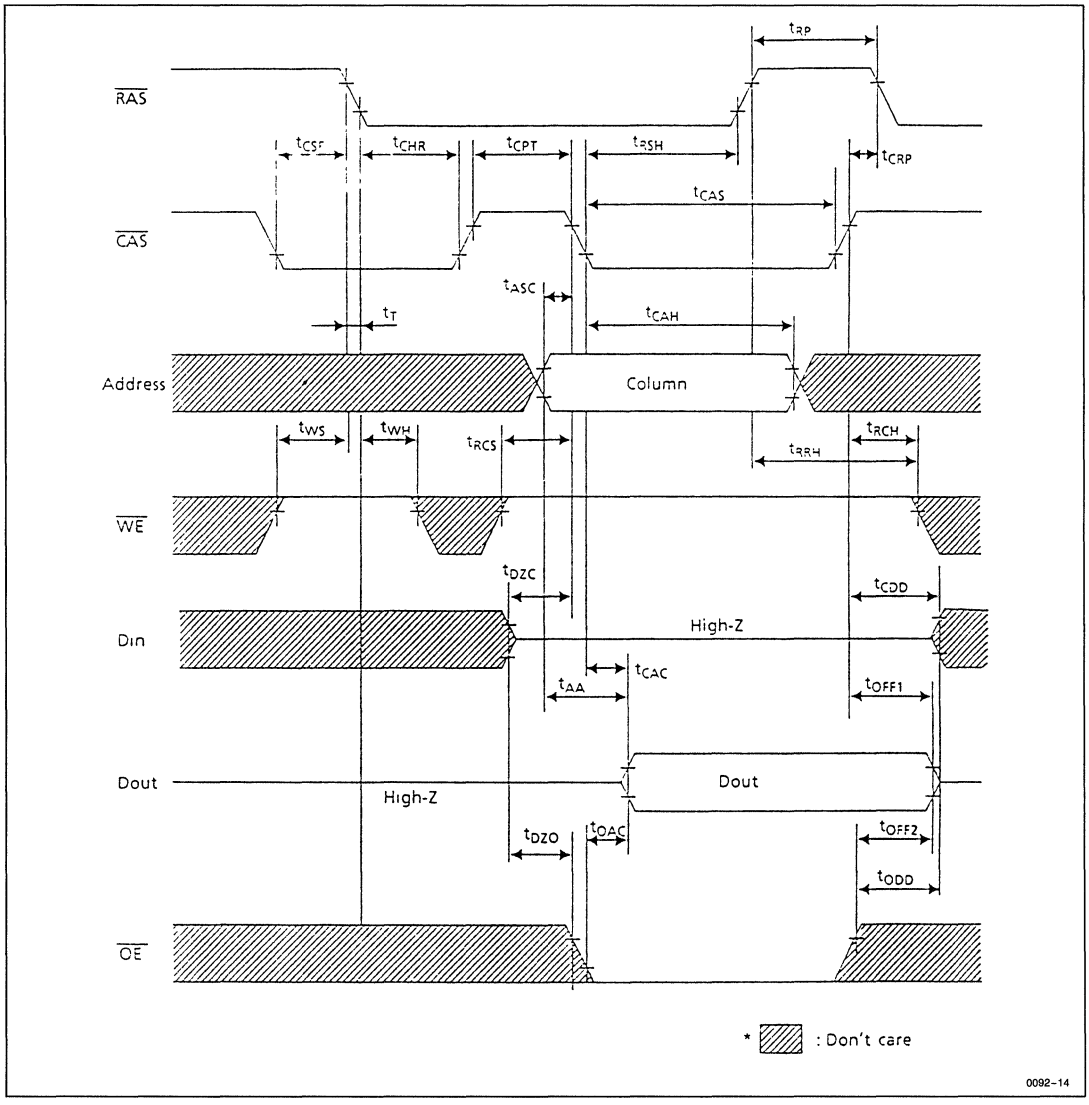
• Fast Page Mode Delayed Write Cycle



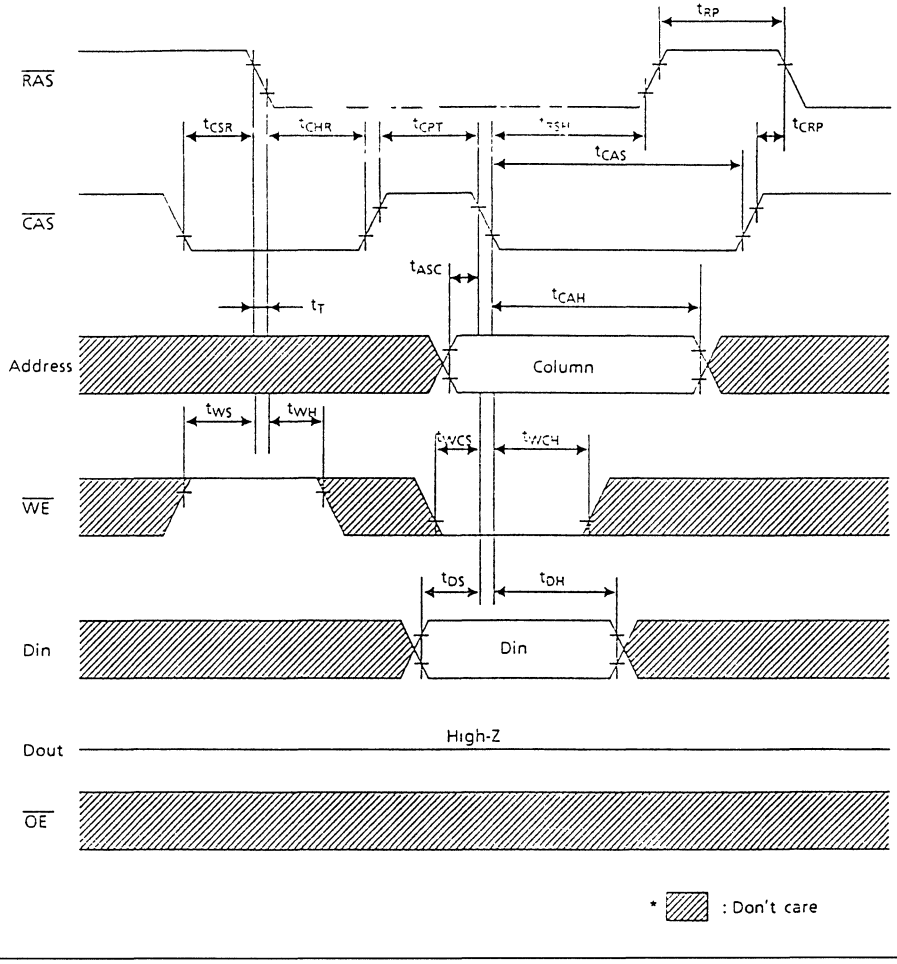
• Fast Page Mode Read-Modify-Write Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)**



HM514260 Series — Preliminary

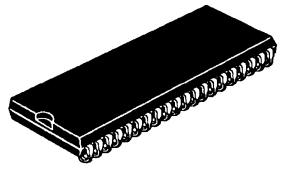
262,144-Word x 16-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514260 are CMOS dynamic RAM organized as 262,144-word x 16-bit. HM514260 have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514260 offer Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514260 to be packaged in standard 400 mil 40-pin plastic SOJ, standard 475 mil 40-pin plastic ZIP.

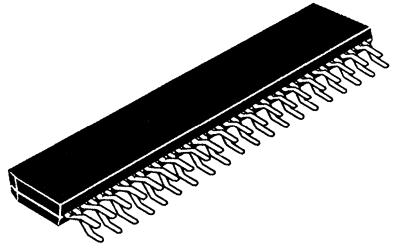
HM514260JP Series



3DCP40D

(CP-40D)

HM514260ZP Series



3DZP40

(ZP-40)

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode .....935 mW/825 mW/715 mW (max)
  - Standby Mode.....11 mW (max)
- Fast Page Mode Capability
- 512 Refresh Cycles .....(8 ms)
- 2$\overline{CAS}$ Byte Control
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh

■ ORDERING INFORMATION

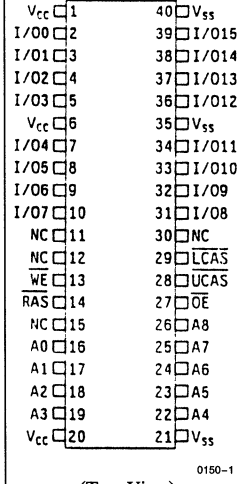
Part No.	Access Time	Package
HM514260JP-7	70 ns	400 mil 40-pin
HM514260JP-8	80 ns	Plastic SOJ
HM514260JP-10	100 ns	(CP-40D)
HM514260ZP-7	70 ns	475 mil 40-pin
HM514260ZP-8	80 ns	Plastic ZIP
HM514260ZP-10	100 ns	(ZP-40)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Input —Row Address A_0–A_8 —Column Address A_0–A_8 —Refresh Address A_0–A_8
I/O_0–I/O_{15}	Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$, $\overline{LCAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

■ PIN OUT

HM514260JP Series



(Top View)

HM514260ZP Series

I/O_9	2		1	I/O_8
I/O_{11}	4		3	I/O_{10}
I/O_{12}	6		5	V_{SS}
I/O_{14}	8		7	I/O_{13}
V_{SS}	10		9	I/O_{15}
I/O_0	12		11	V_{CC}
I/O_2	14		13	I/O_1
V_{CC}	16		15	I/O_3
I/O_5	18		17	I/O_4
I/O_7	20		19	I/O_6
NC	22		21	NC
$\overline{RAS}$	24		23	$\overline{WE}$
A_0	26		25	NC
A_2	28		27	A_1
V_{CC}	30		29	A_3
A_4	32		31	V_{SS}
A_6	34		33	A_5
A_8	36		35	A_7
$\overline{UCAS}$	38		37	$\overline{OE}$
NC	40		39	$\overline{LCAS}$

(Bottom View)

■ TRUTH TABLE

Inputs					I/O		Operation
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	I/O_0–I/O_7	I/O_8–I/O_{15}	
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	D_{out}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D_{out}	Upper Byte Read
L	L	L	H	L	D_{out}	D_{out}	Word Read
L	L	H	L	H	D_{in}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D_{in}	Upper Byte Write
L	L	L	L	H	D_{in}	D_{in}	Word Write
L	L	L	H	H	High-Z	High-Z	

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	− 1.0	—	0.8	V	1
	(Others)	V_{IL}	− 2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HM514260-7		HM514260-8		HM514260-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	170	—	150	—	130	mA	$\overline{RAS}$ Cycling $\overline{LCAS}$ or $\overline{UCAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ = V_{IH} D_{out} = High-Z	
		—	1	—	1	—	1	mA	CMOS Interface, $\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	150	—	130	—	110	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{LCAS}$ or $\overline{UCAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	150	—	130	—	110	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	130	—	120	—	110	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	

• **DC Electrical Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V) (continued)

Parameter	Symbol	HM514260-7		HM514260-8		HM514260-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{LCAS}$ and $\overline{UCAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{LCAS}$ and $\overline{UCAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 14, 15]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514260-7		HM514260-8		HM514260-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	20	60	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	15	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	20	—	20	—	25	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	ms	

Read Cycle

Parameter	Symbol	HM514260-7		HM514260-8		HM514260-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	3, 4, 13
Access Time from Address	t_{AA}	—	35	—	40	—	45	ns	3, 5, 13
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	35	—	40	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	15	0	15	0	20	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	15	0	15	0	20	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	15	—	15	—	20	—	ns	

Write Cycle

Parameter	Symbol	HM514260-7		HM514260-8		HM514260-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514260-7		HM514260-8		HM514260-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	180	—	200	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	95	—	105	—	135	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	45	—	45	—	60	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	60	—	65	—	80	—	ns	10, 13
$\overline{OE}$ to Hold Time from $\overline{WE}$	t_{OEH}	20	—	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM514260-7		HM514260-8		HM514260-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time in Normal Mode	t_{CPN}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514260-7		HM514260-8		HM514260-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	ns	3, 13
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	ns	
Fast Page Mode Read-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPW}	65	—	70	—	85	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	95	—	100	—	110	—	ns	

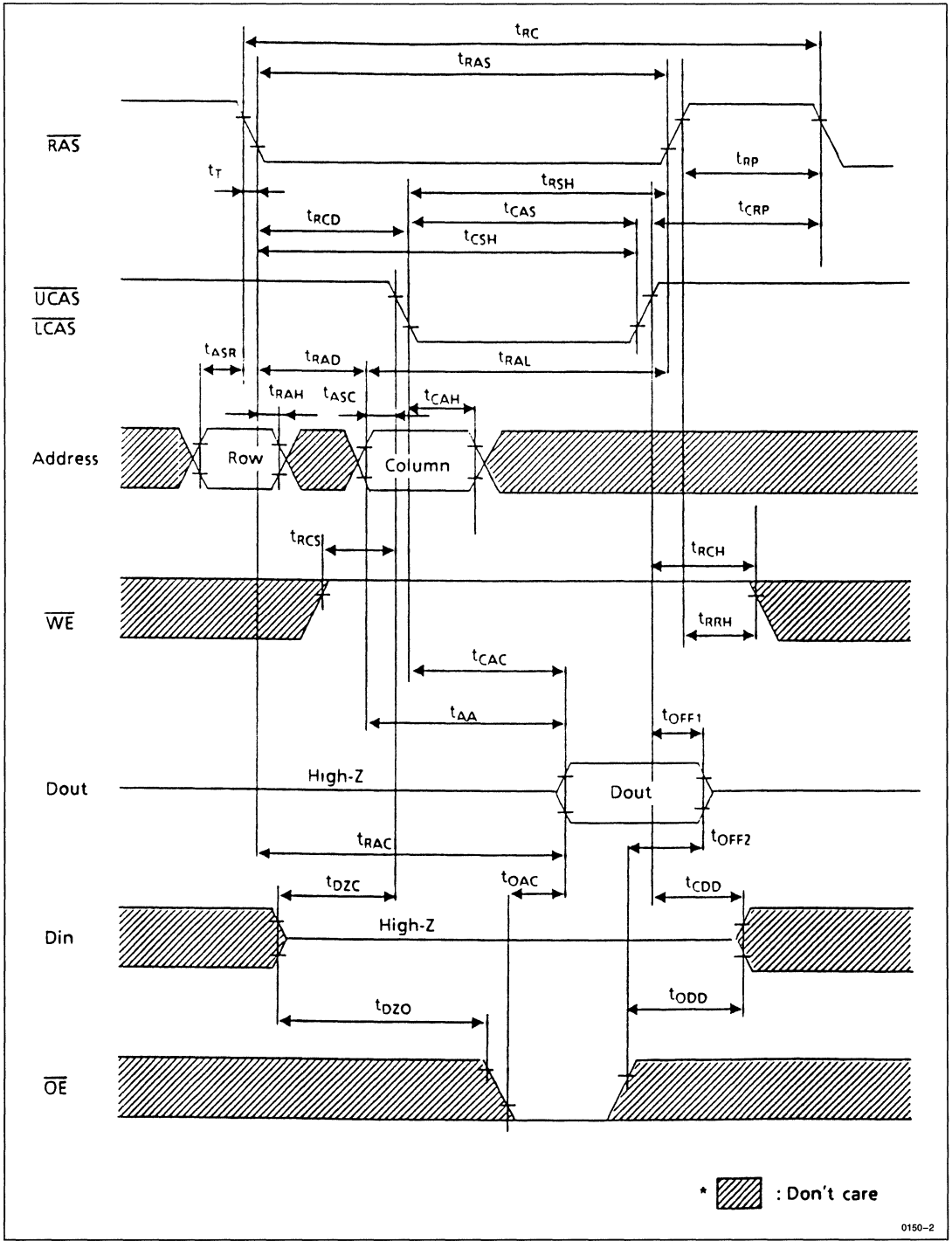
Counter Test Cycle

Parameter	Symbol	HM514260-7		HM514260-8		HM514260-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	50	—	50	—	50	—	ns	

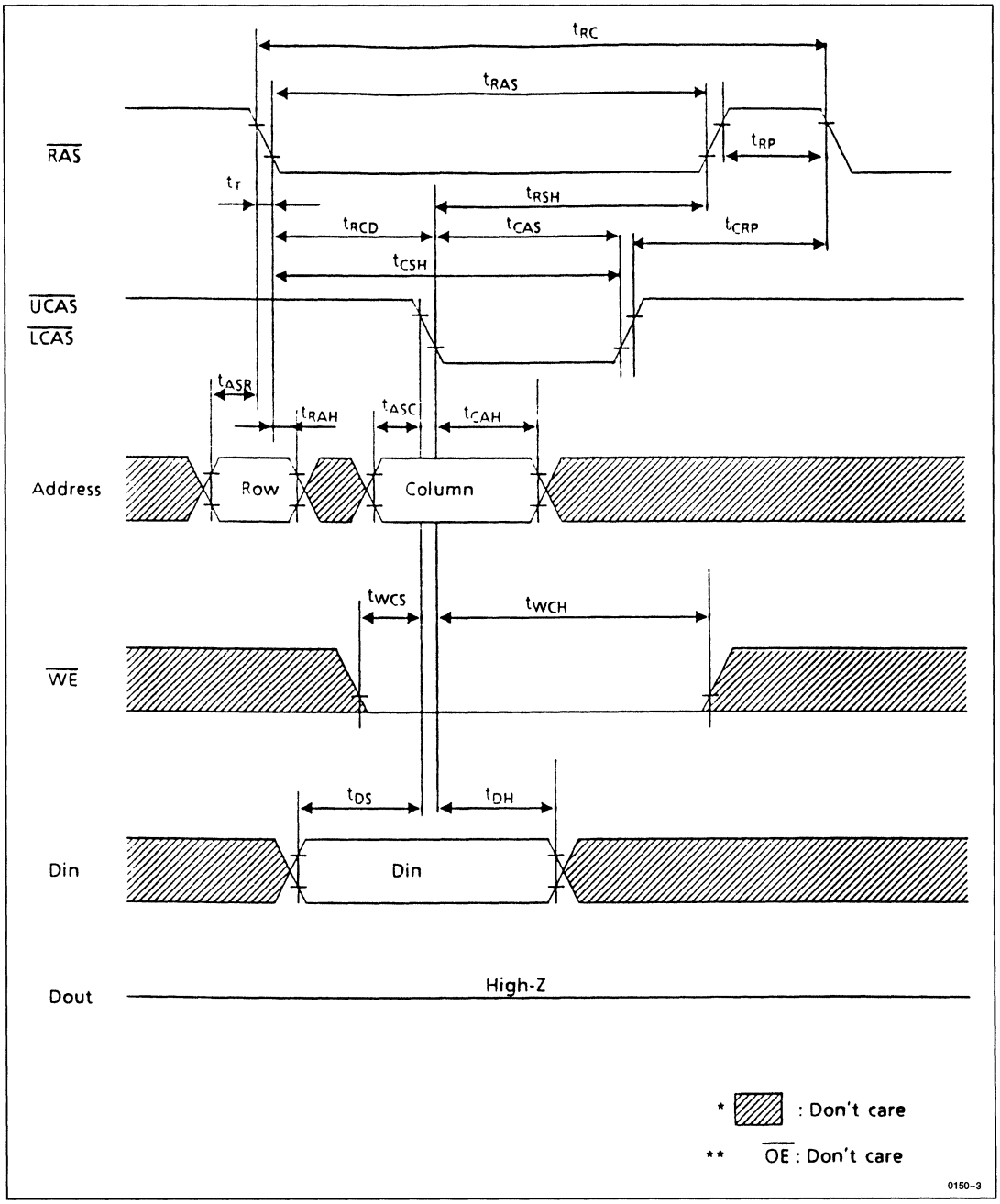
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Either t_{RCH} or T_{RRH} must be satisfied for a read cycle.
17. When both $\overline{LCAS}$ and $\overline{UCAS}$ go low at the same time, all 16 bits data are written into the device. $\overline{LCAS}$ or $\overline{UCAS}$ cannot be staggered within the same write/read cycles.

■ TIMING WAVEFORMS

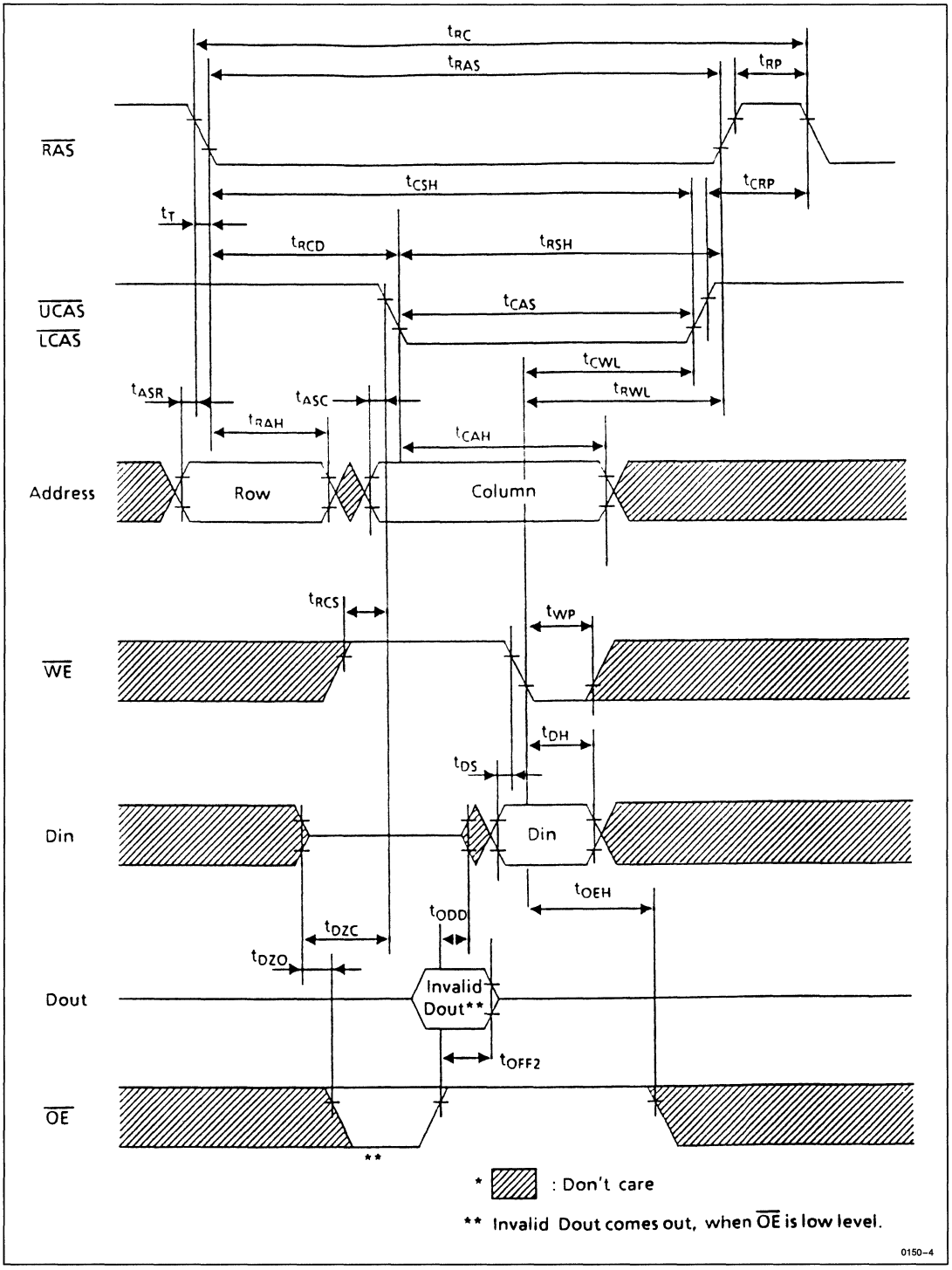
• Read Cycle



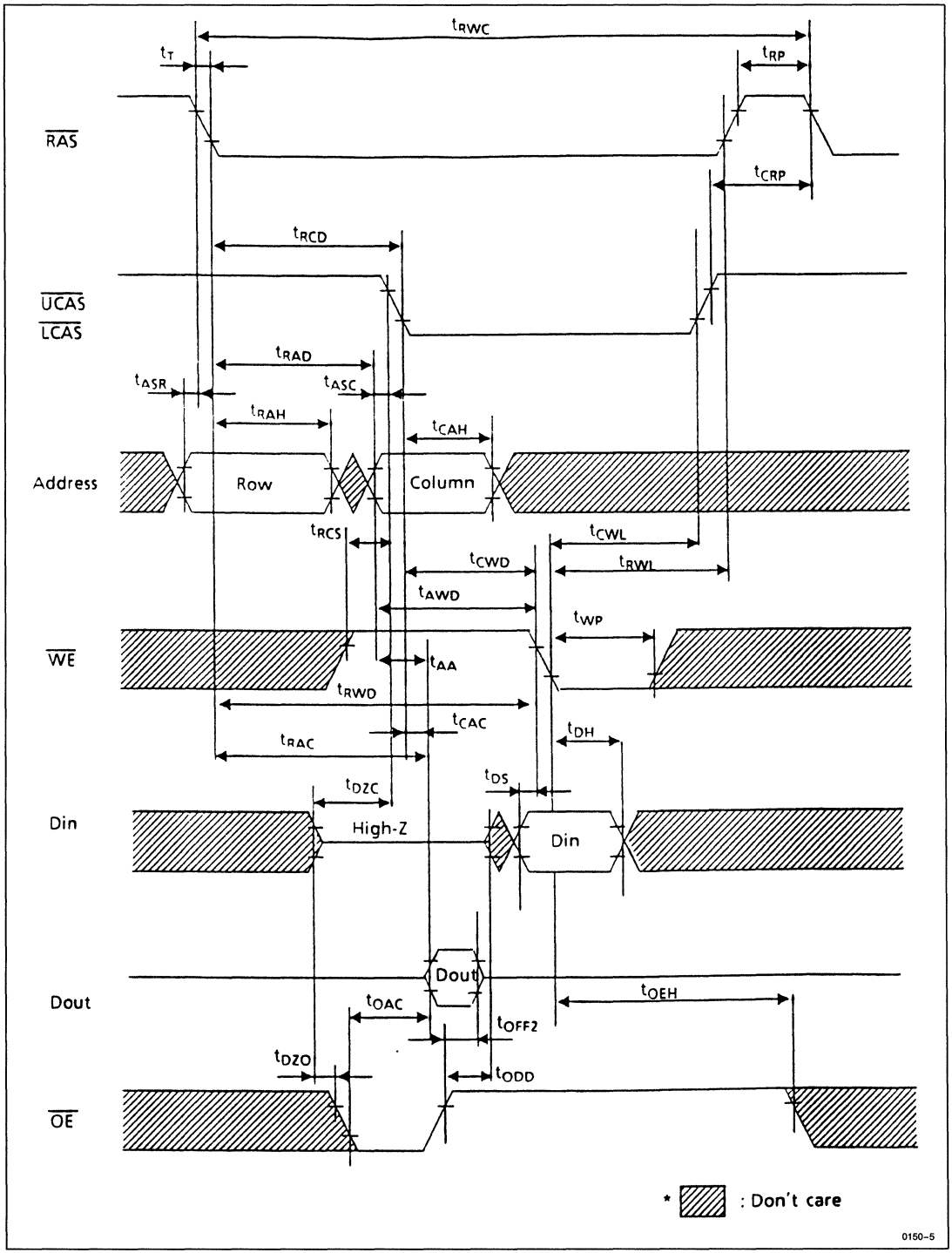
• **Early Write Cycle**



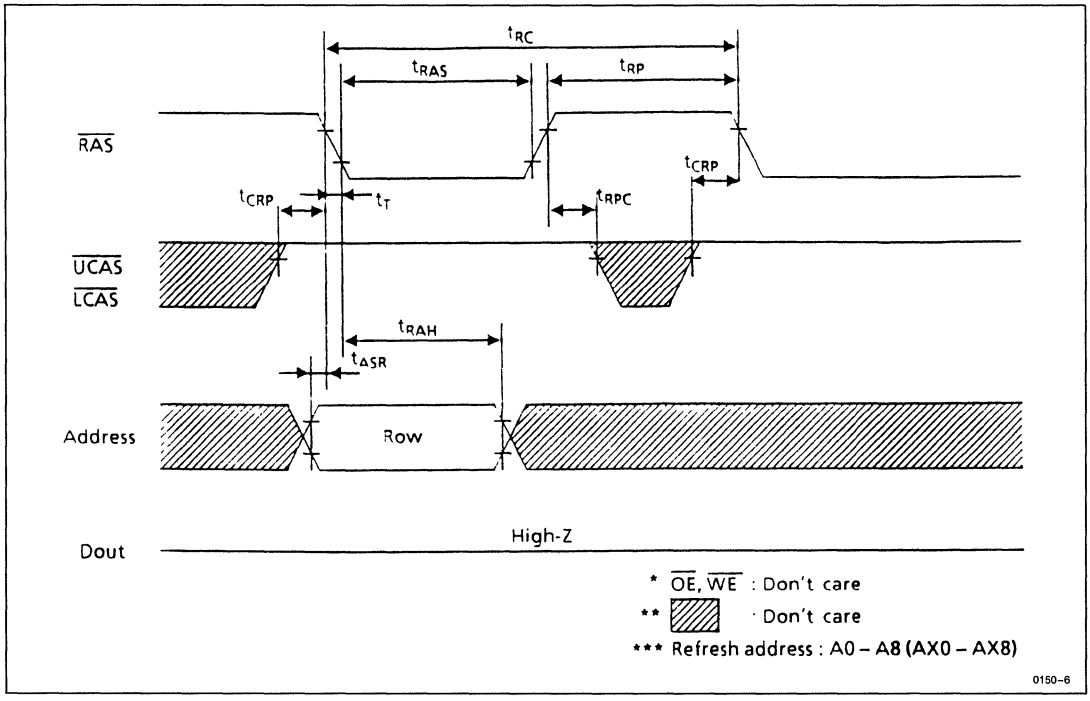
• **Delayed Write Cycle**



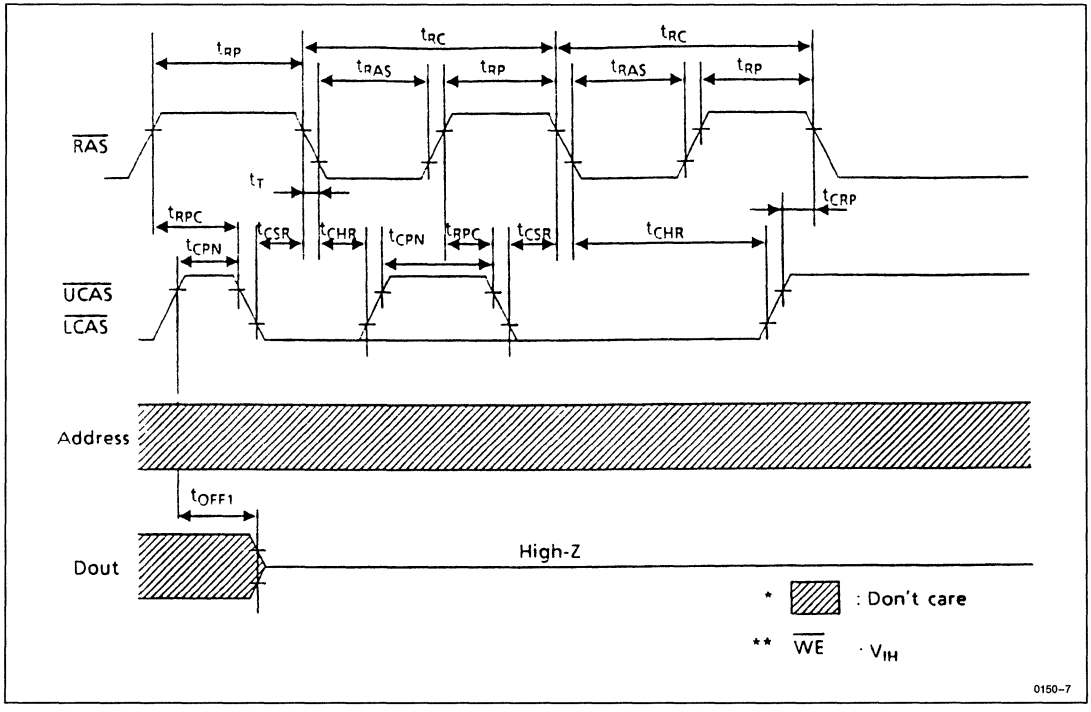
• **Read-Modify-Write Cycle**



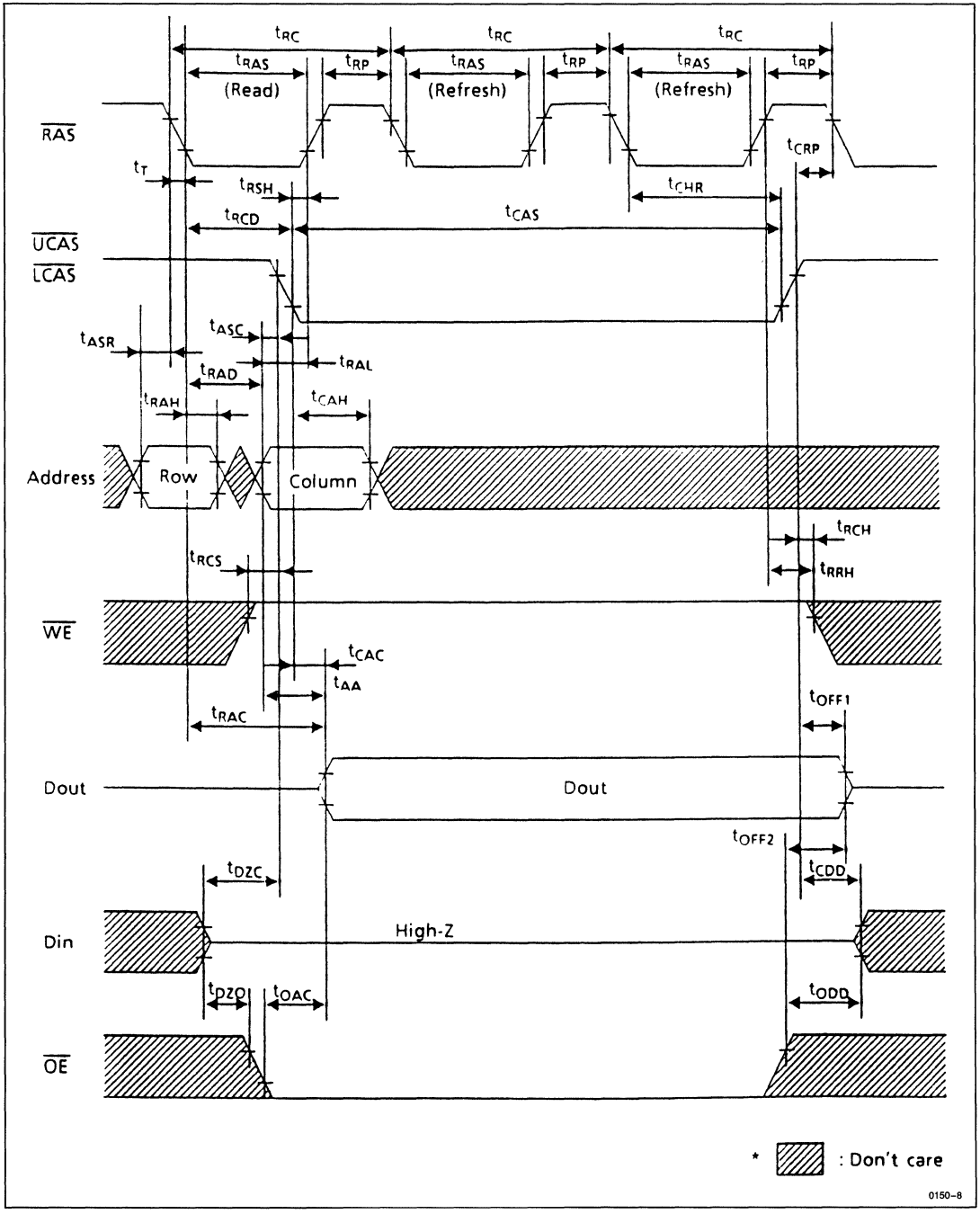
• **$\overline{RAS}$ Only Refresh Cycle**



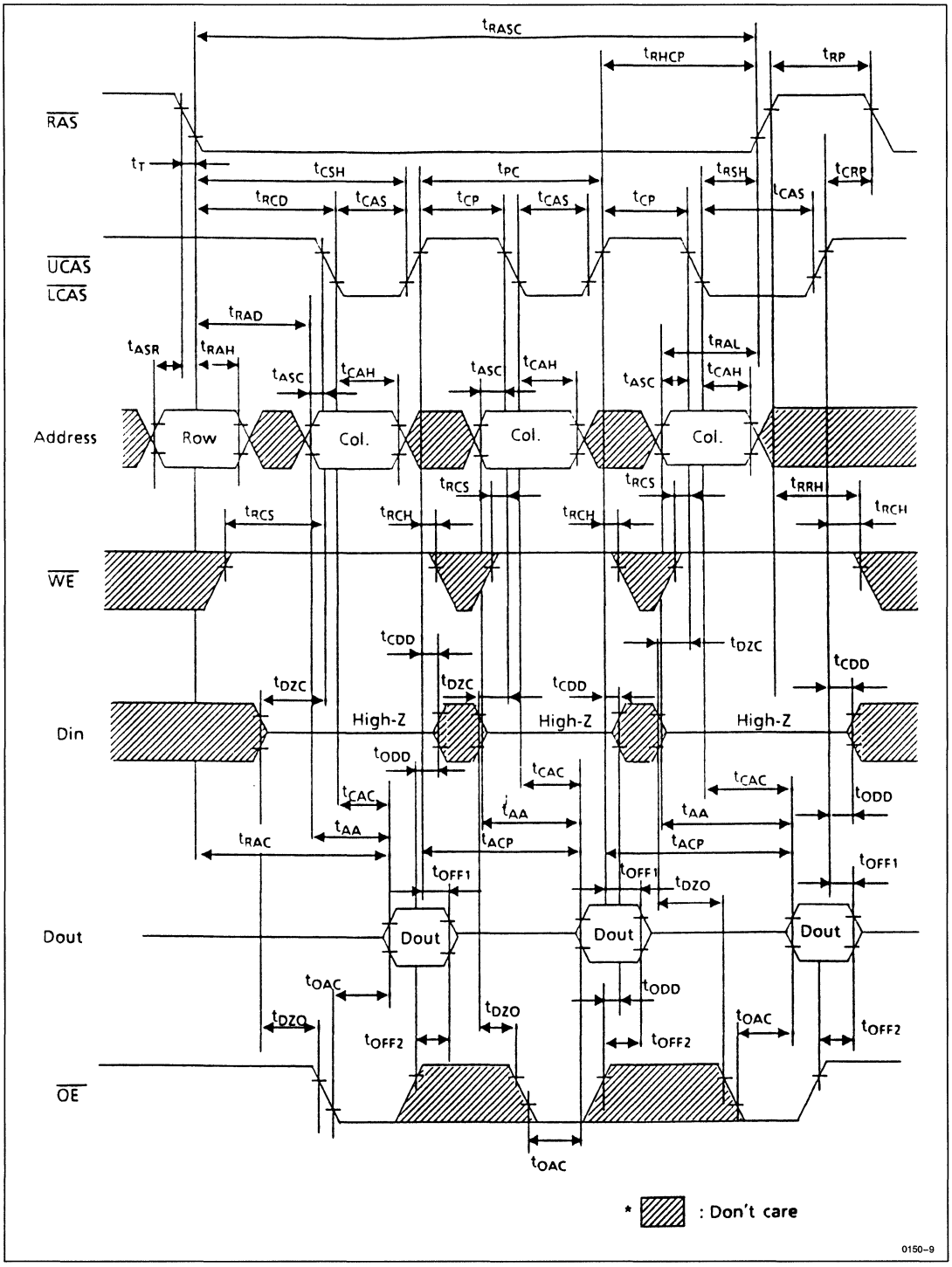
• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**



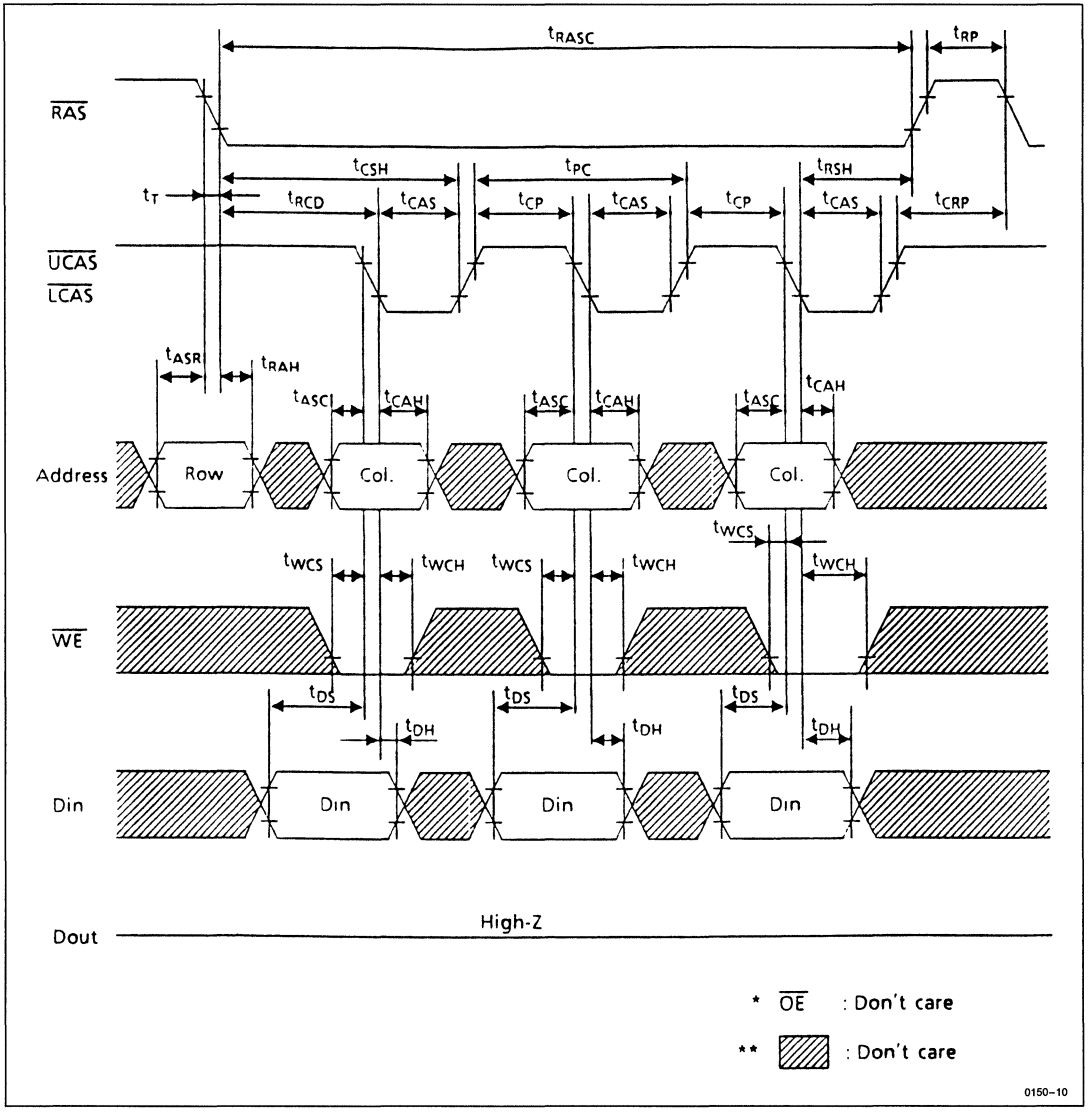
• **Hidden Refresh Cycle**



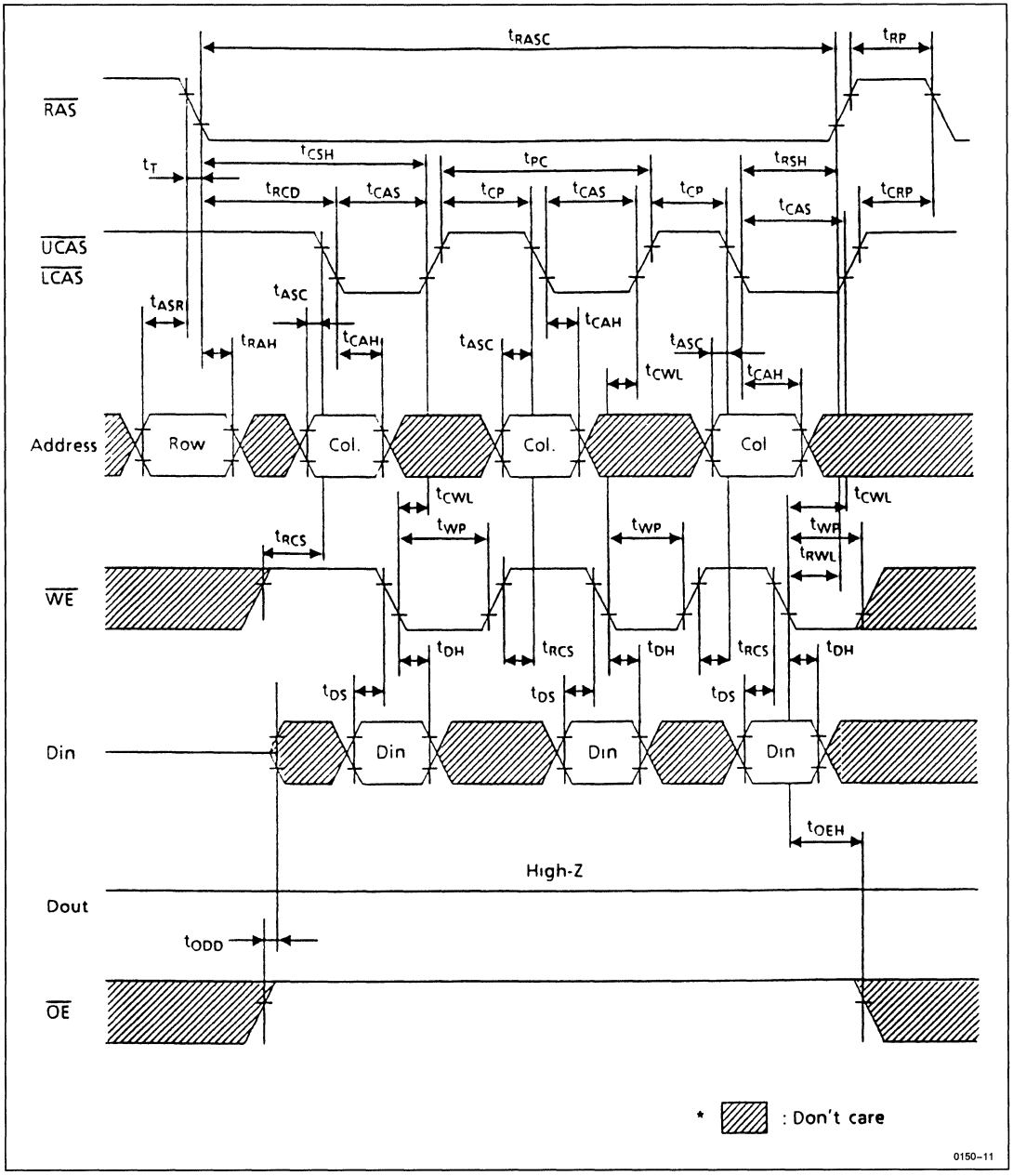
• **Fast Page Mode Read Cycle**



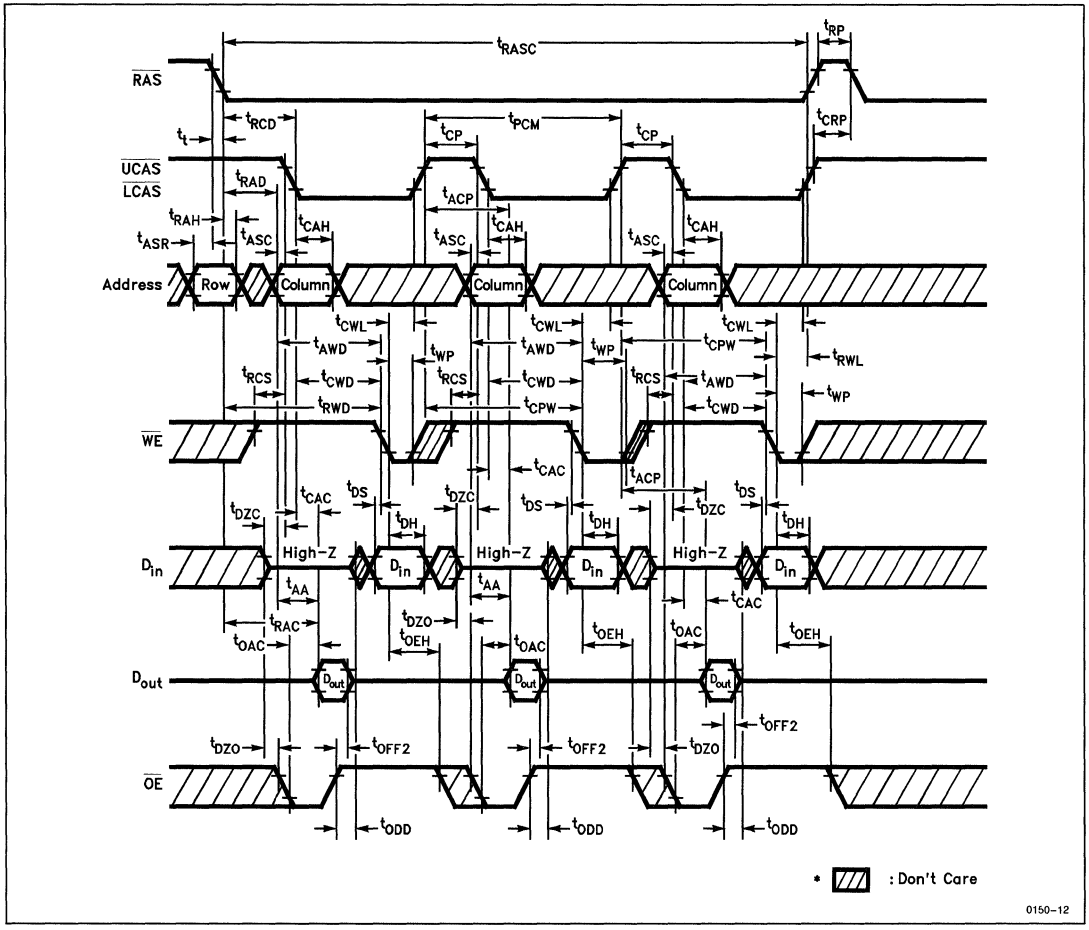
• **Fast Page Mode Early Write Cycle**



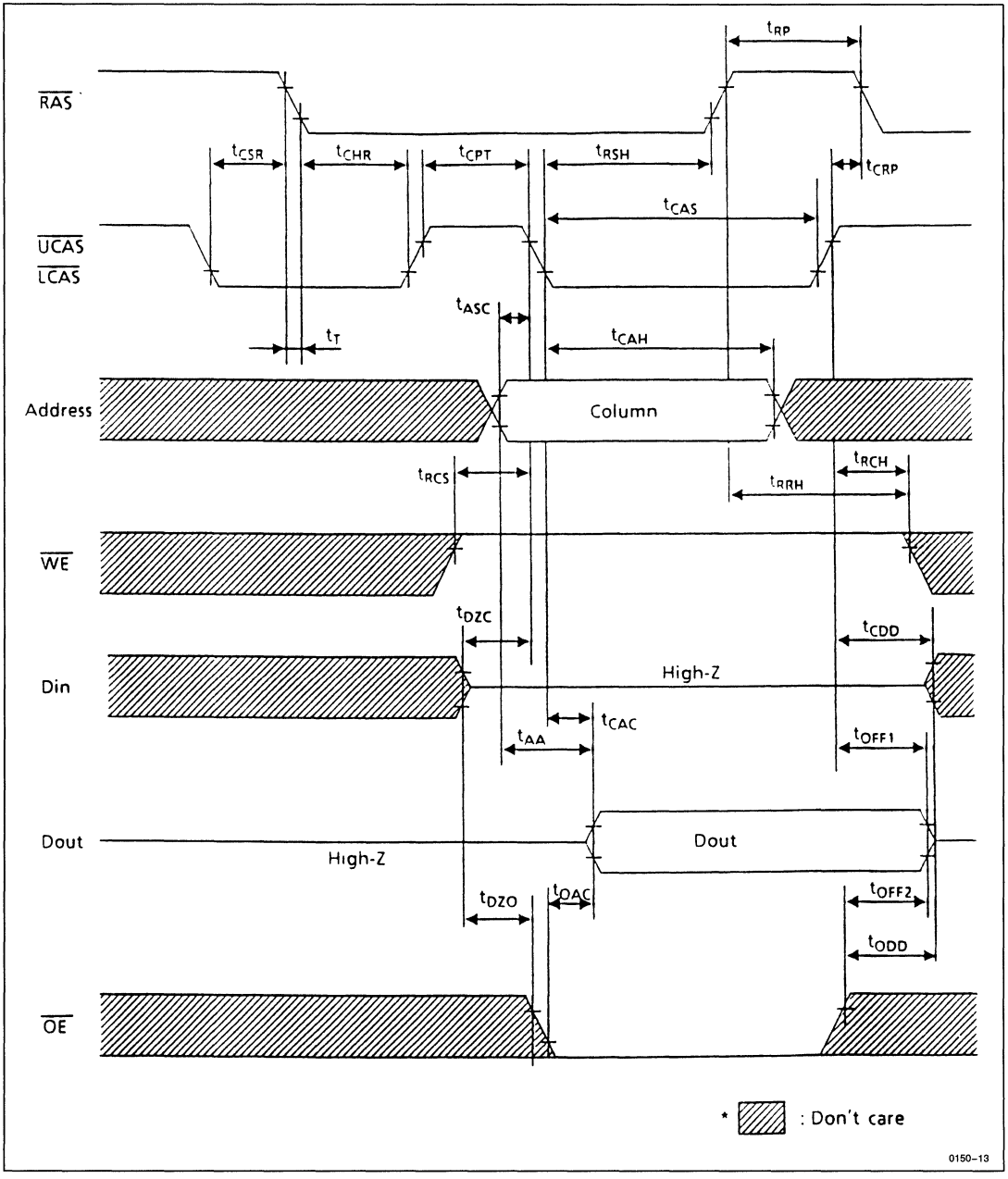
• **Fast Page Mode Delayed Write Cycle**



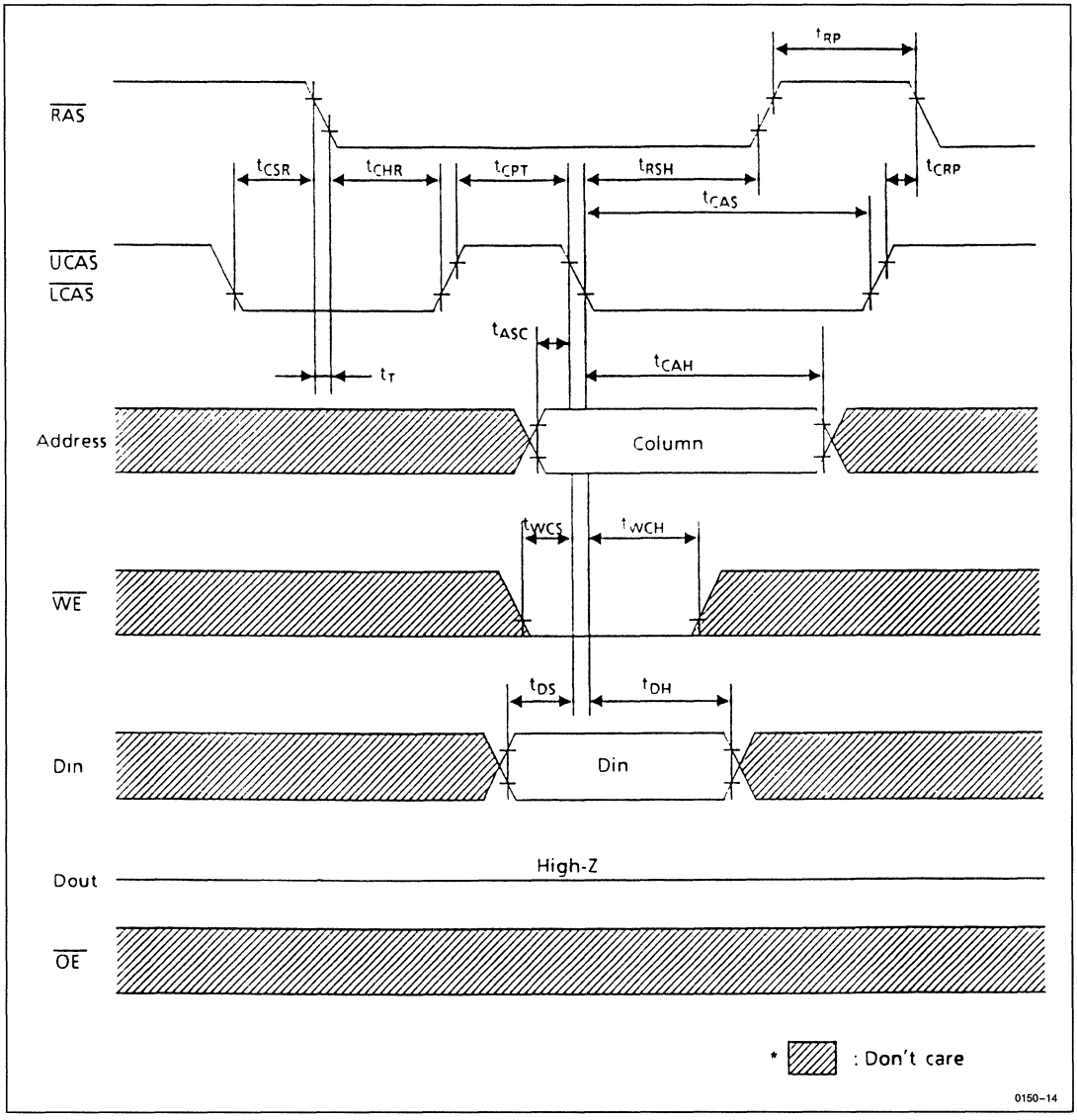
• Fast Page Mode Read-Modify-Write Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM514170 Series

Preliminary

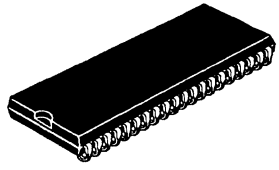
262,144-Word x 16-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514170 are CMOS dynamic RAM organized as 262,144-word x 16-bit. HM514170 have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514170 offer Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514170 to be packaged in standard 400 mil 40-pin plastic SOJ, standard 475 mil 40-pin plastic ZIP.

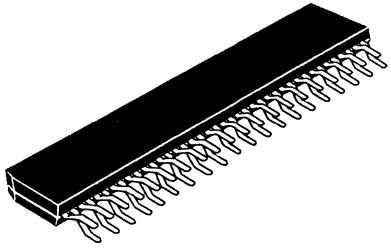
HM514170JP Series



3DCP40D

(CP-40D)

HM514170ZP Series



3DZP40

(ZP-40)

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode .....770 mW/660 mW/550 mW (max)
  - Standby Mode.....11 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles .....(16 ms)
- 2$\overline{WE}$ Byte Control
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh

■ ORDERING INFORMATION

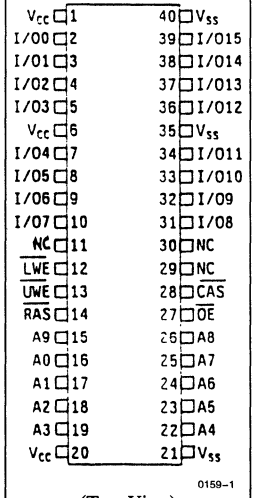
Part No.	Access Time	Package
HM514170JP-7	70 ns	400 mil 40-pin
HM514170JP-8	80 ns	Plastic SOJ
HM514170JP-10	100 ns	(CP-40D)
HM514170ZP-7	70 ns	475 mil 40-pin
HM514170ZP-8	80 ns	Plastic ZIP
HM514170ZP-10	100 ns	(ZP-40)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input —Row Address A_0–A_9 —Column Address A_0–A_7 —Refresh Address A_0–A_9
I/O_0–I/O_{15}	Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{UWE}$, $\overline{LWE}$	Read/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

■ PIN OUT

HM514170JP Series



0159-1

(Top View)

HM514170ZP Series

I/O_9	2		1	I/O_8
I/O_{11}	4		3	I/O_{10}
I/O_{12}	6		5	V_{SS}
I/O_{14}	8		7	I/O_{13}
V_{SS}	10		9	I/O_{15}
I/O_0	12		11	V_{CC}
I/O_2	14		13	I/O_1
V_{CC}	16		15	I/O_3
I/O_5	18		17	I/O_4
I/O_7	20		19	I/O_5
$\overline{LWE}$	22		21	NC
$\overline{RAS}$	24		23	$\overline{UWE}$
NC	26		25	NC
A_0	28		27	A_1
A_2	30		29	A_3
V_{CC}	32		31	V_{SS}
A_4	34		33	A_5
A_6	36		35	A_7
A_8	38		37	$\overline{OE}$
$\overline{CAS}$	40		39	NC

(Bottom View)

■ TRUTH TABLE

Inputs					I/O		Operation
$\overline{RAS}$	$\overline{LWE}$	$\overline{UWE}$	$\overline{CAS}$	$\overline{OE}$	I/O_0–I/O_7	I/O_8–I/O_{15}	
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	H	H	L	L	D_{out}	D_{out}	Word Read
L	L	H	L	H	D_{in}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D_{in}	Upper Byte Write
L	L	L	L	H	D_{in}	D_{in}	Word Write
L	H	H	L	H	High-Z	High-Z	

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	−1.0	—	0.8	V	1
	(Others)	V_{IL}	−2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM514170-7		HM514170-8		HM514170-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	140	—	120	—	100	mA	$\overline{RAS}$ Cycling $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	1	—	1	—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	150	—	130	—	110	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	150	—	130	—	110	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	130	—	120	—	110	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	µA	0V ≤ V_{in} ≤ 7V	

• **DC Electrical Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V) (continued)

Parameter	Symbol	HM514170-7		HM514170-8		HM514170-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed ≤1 time while $\overline{RAS}$ = V_{IL}.
3. Address can be changed ≤1 time while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Electrical Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 14, 15]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514170-7		HM514170-8		HM514170-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	20	60	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	15	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	20	—	20	—	25	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514170-7		HM514170-8		HM514170-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	3, 4, 13
Access Time from Address	t_{AA}	—	35	—	40	—	45	ns	3, 5, 13
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	35	—	40	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	15	0	15	0	20	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	15	0	15	0	20	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	15	—	15	—	20	—	ns	

Write Cycle

Parameter	Symbol	HM514170-7		HM514170-8		HM514170-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514170-7		HM514170-8		HM514170-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	180	—	200	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	95	—	105	—	135	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	45	—	45	—	60	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	60	—	65	—	80	—	ns	10, 13
$\overline{OE}$ to Hold Time from $\overline{WE}$	t_{OEH}	20	—	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM514170-7		HM514170-8		HM514170-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time in Normal Mode	t_{CPN}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514170-7		HM514170-8		HM514170-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	ns	3, 13
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	ns	
Fast Page Mode Read-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPW}	65	—	70	—	85	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	95	—	100	—	110	—	ns	

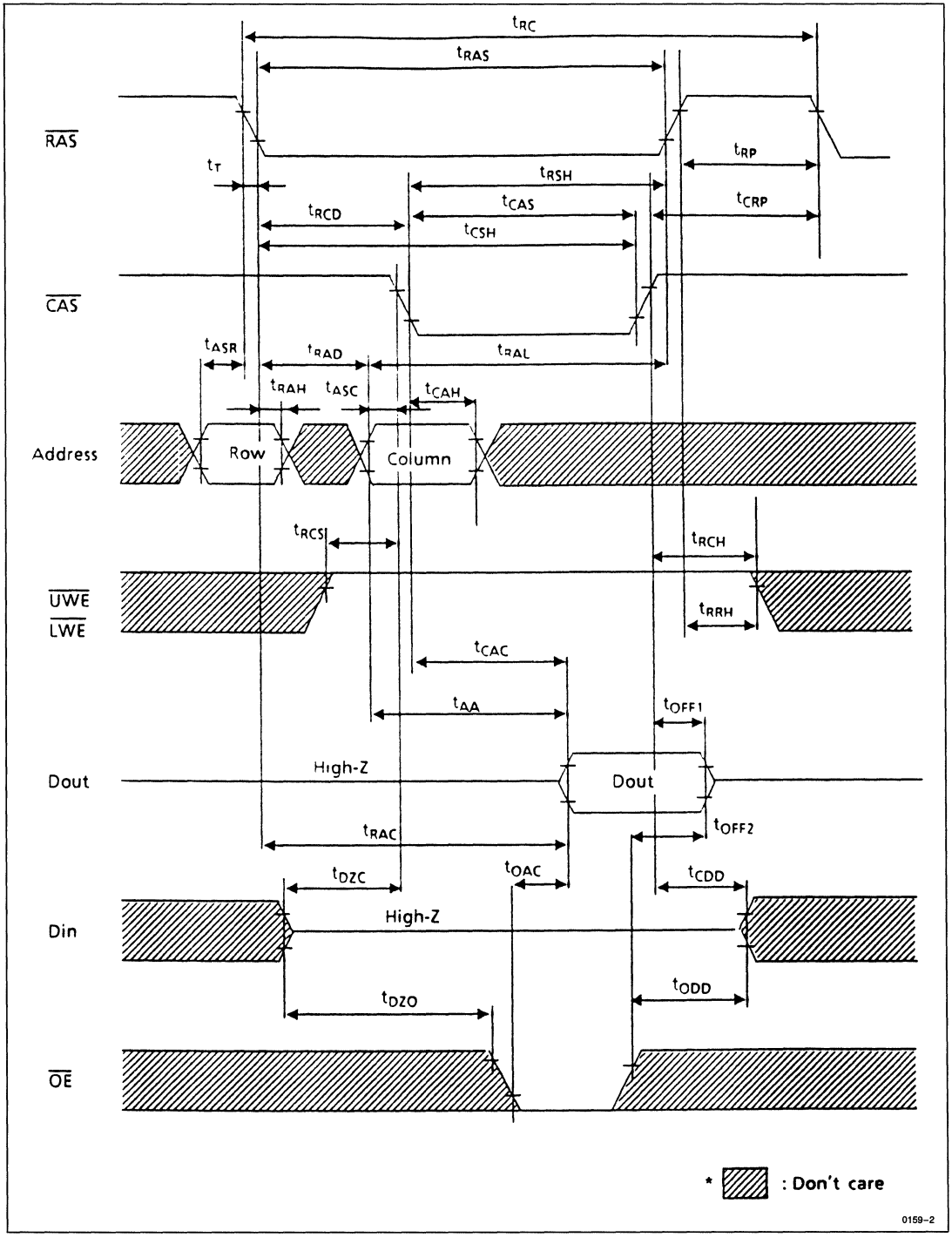
Counter Test Cycle

Parameter	Symbol	HM514170-7		HM514170-8		HM514170-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	50	—	50	—	50	—	ns	

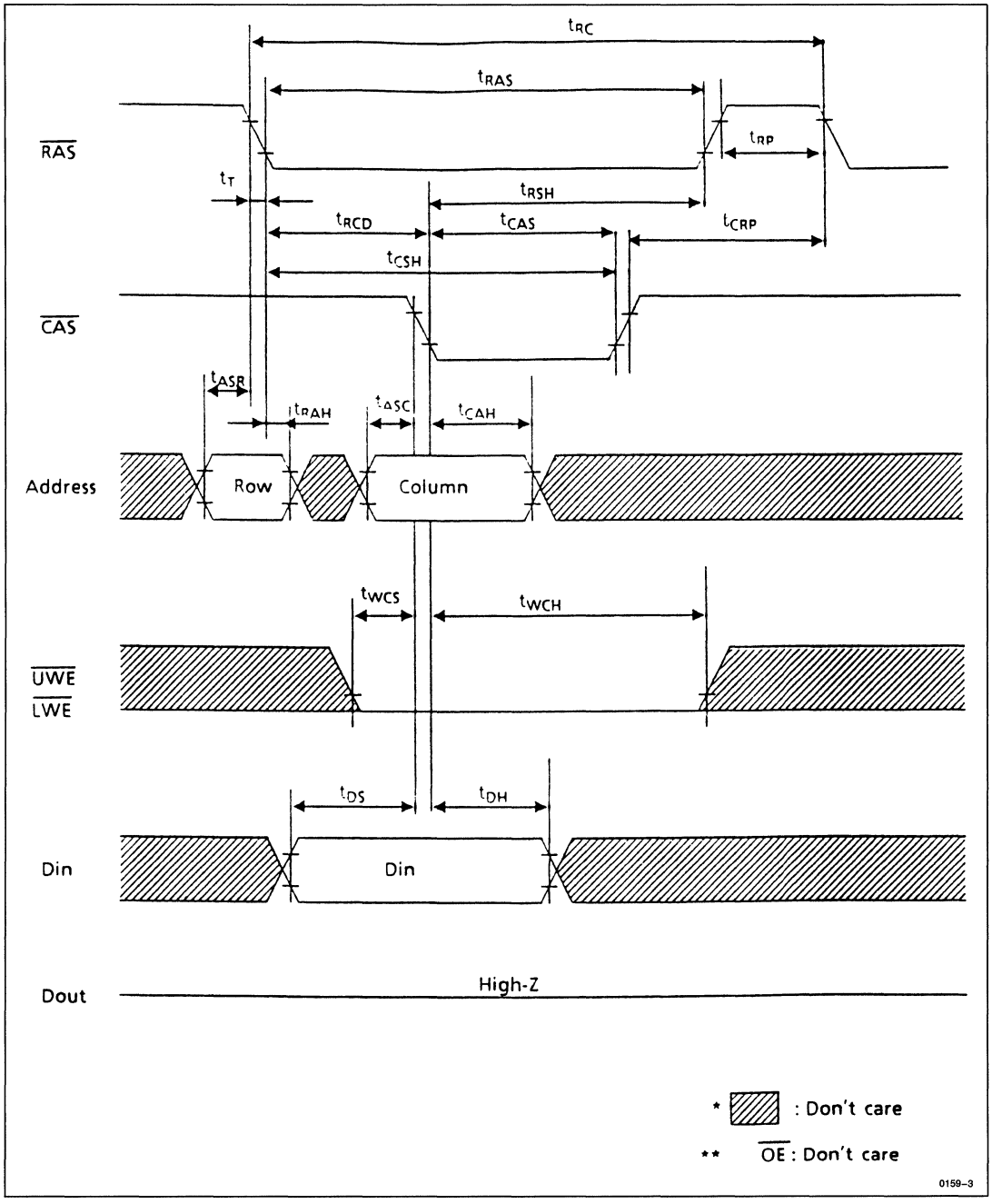
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Either t_{RCH} or T_{RRH} must be satisfied for a read cycle.
17. When both $\overline{LWE}$ and $\overline{UWE}$ go low at the same time, all 16-bits data are written into the device. $\overline{LWE}$ and $\overline{UWE}$ cannot be staggered within the same write cycles.

■ TIMING WAVEFORMS

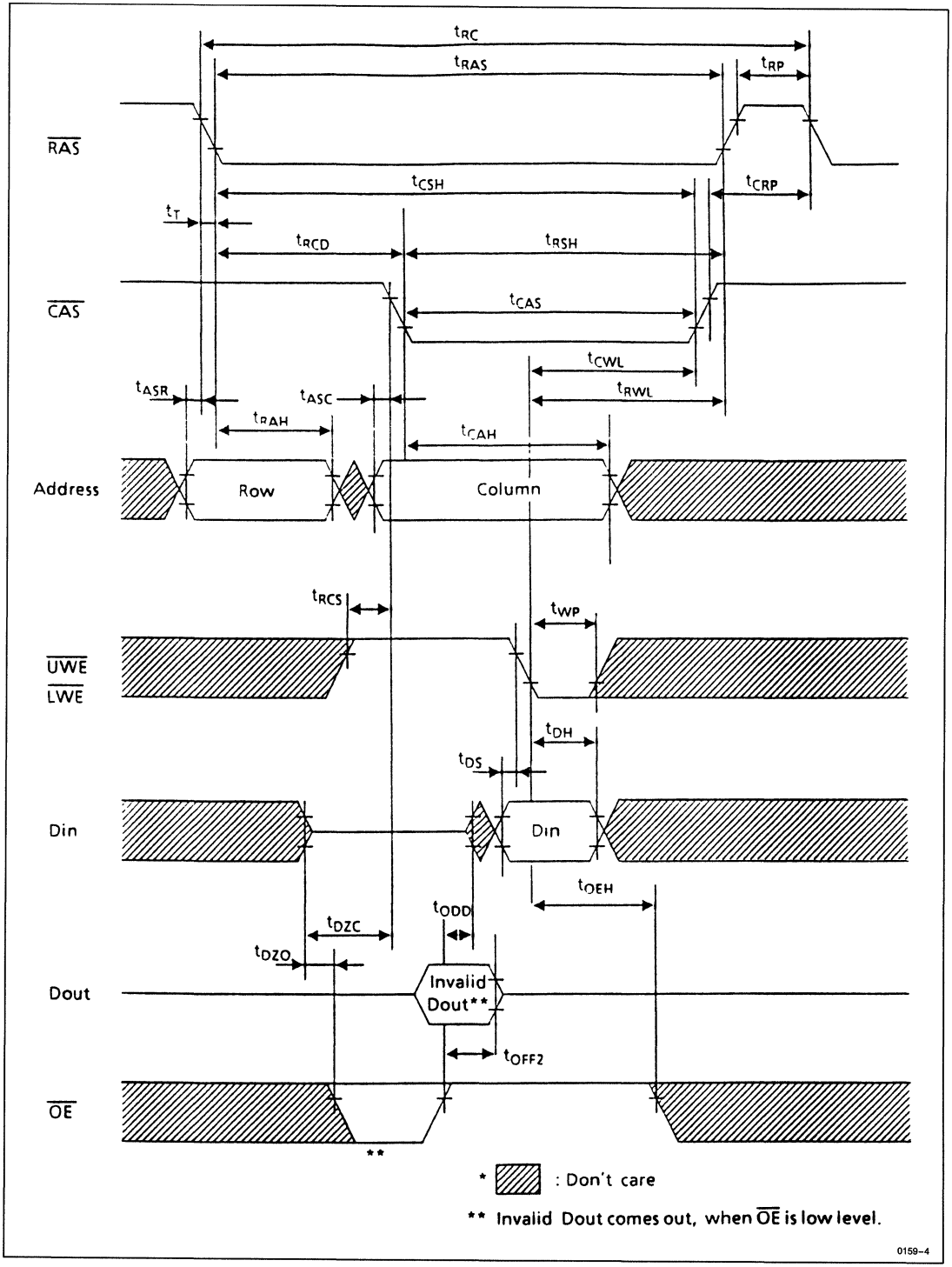
• Read Cycle



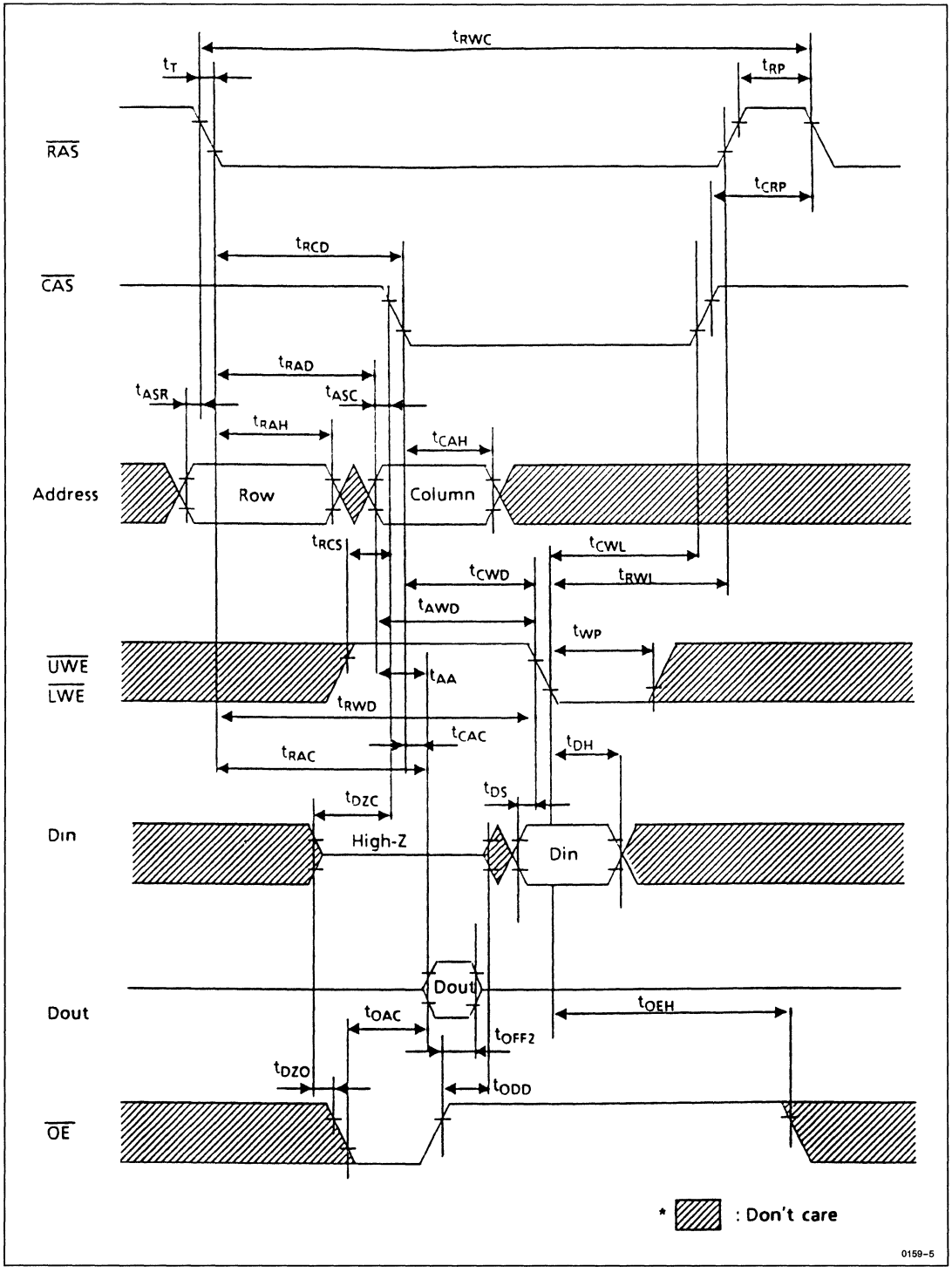
• **Early Write Cycle**



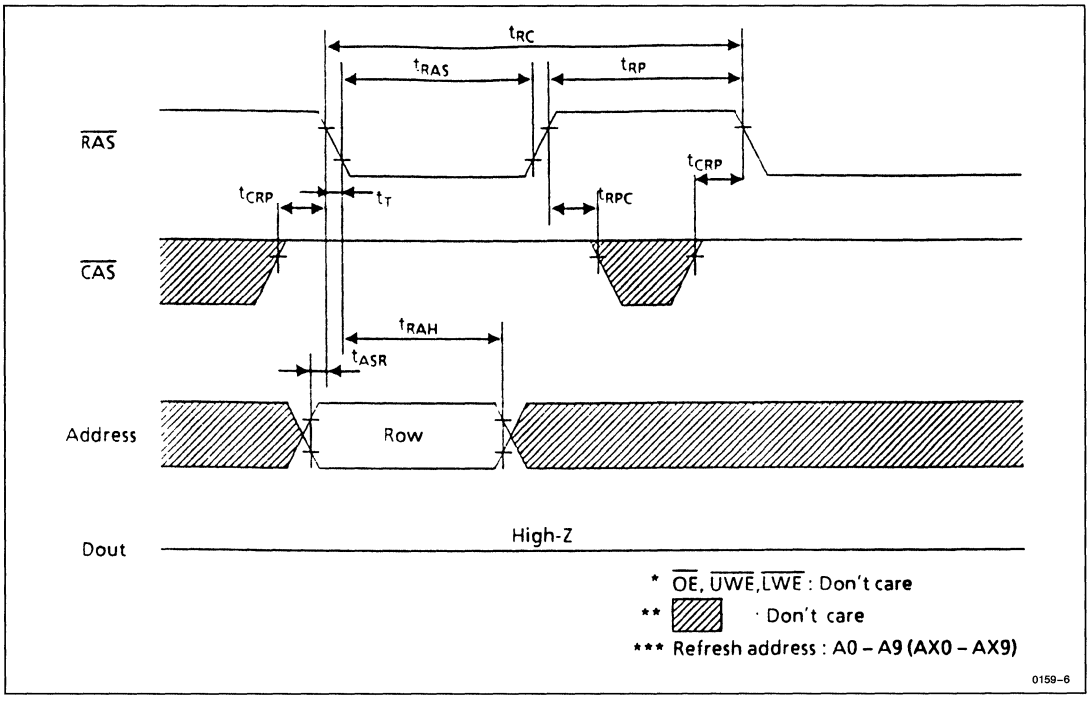
• **Delayed Write Cycle**



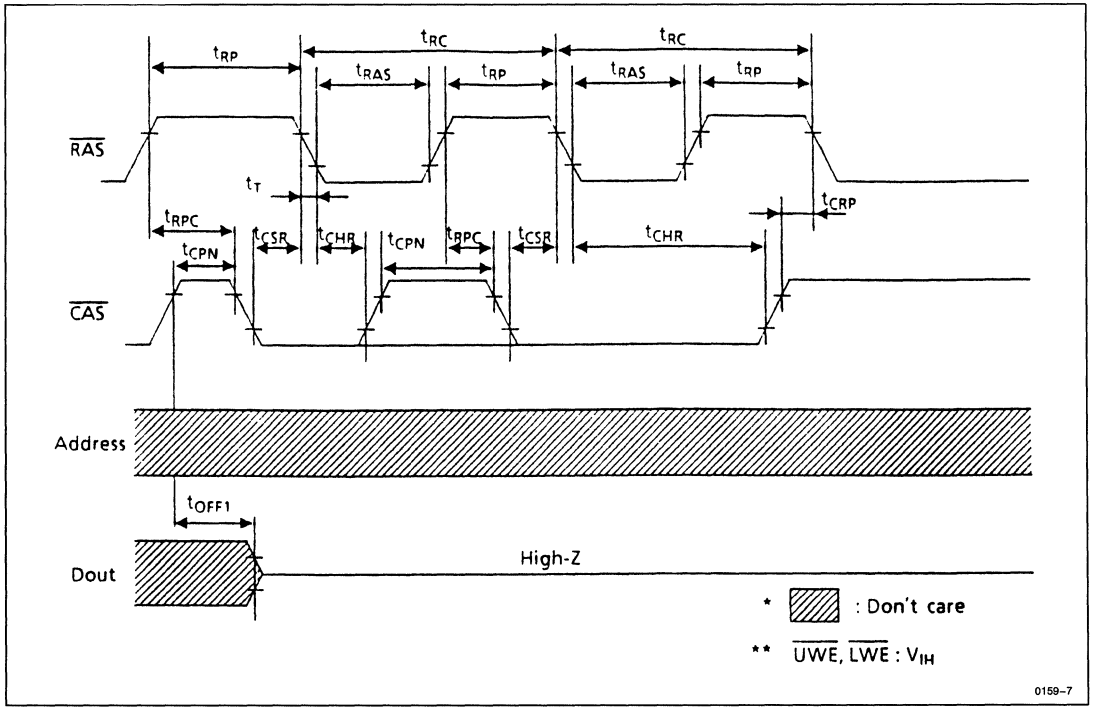
• **Read-Modify-Write Cycle**



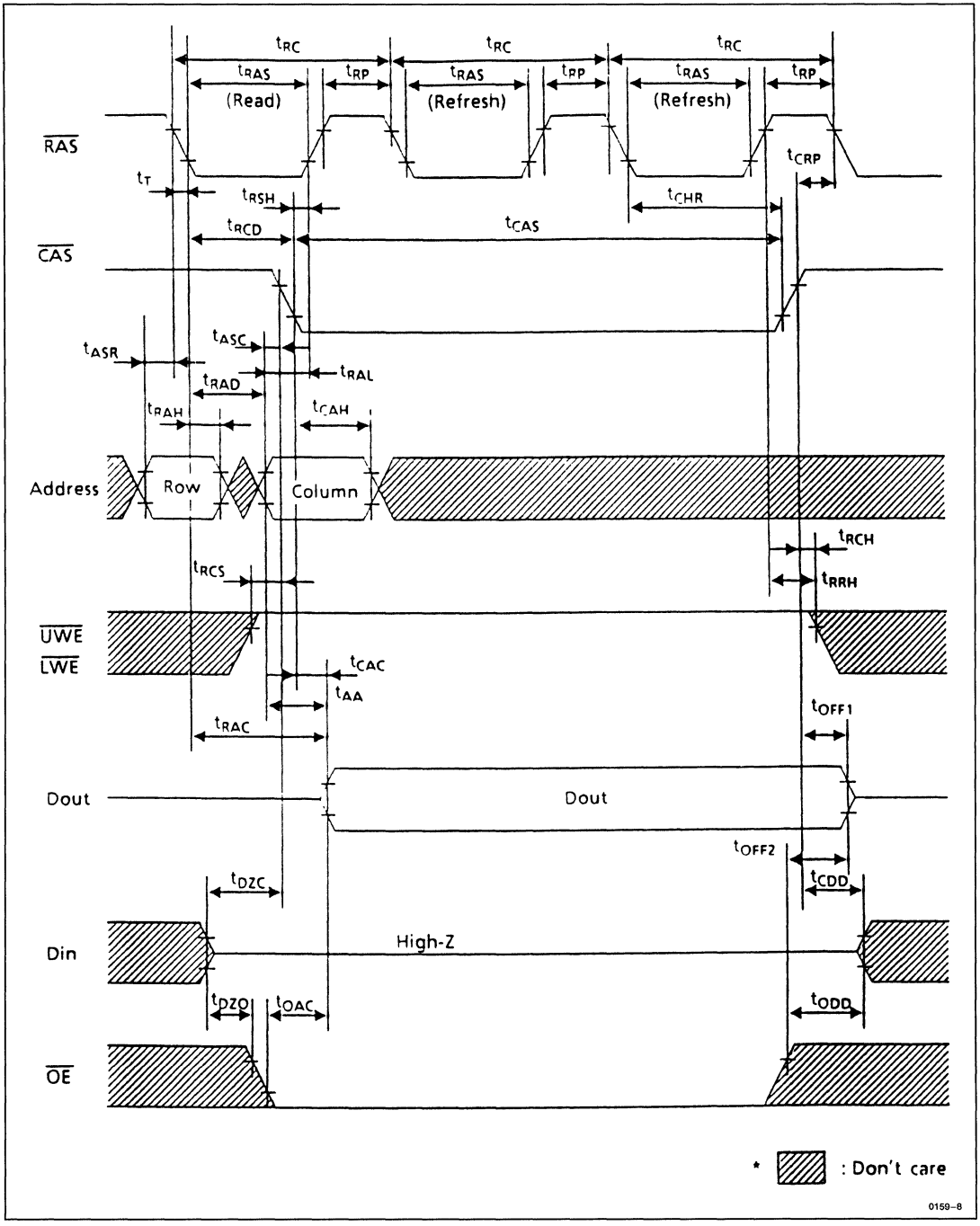
• $\overline{RAS}$ Only Refresh Cycle



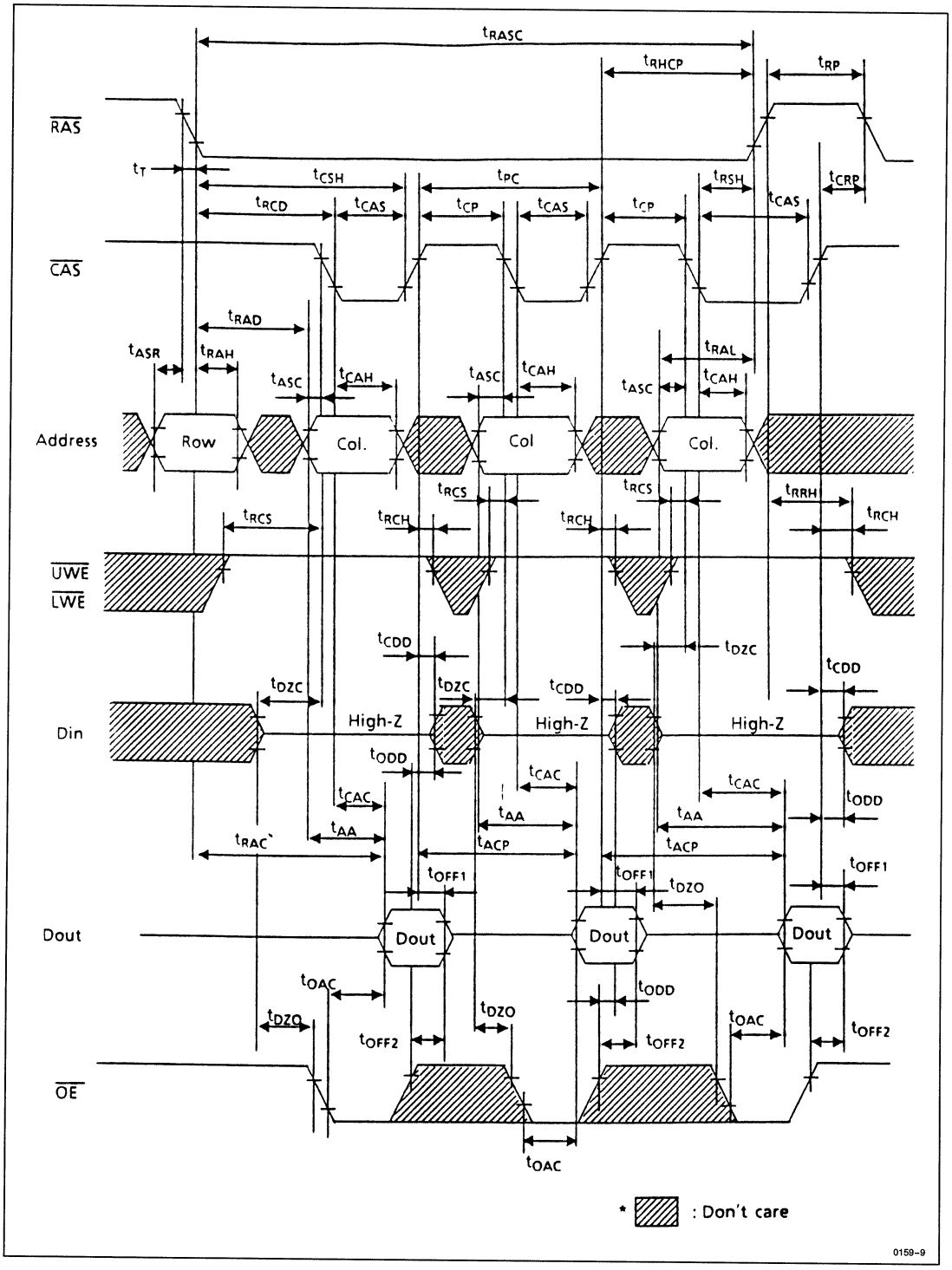
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



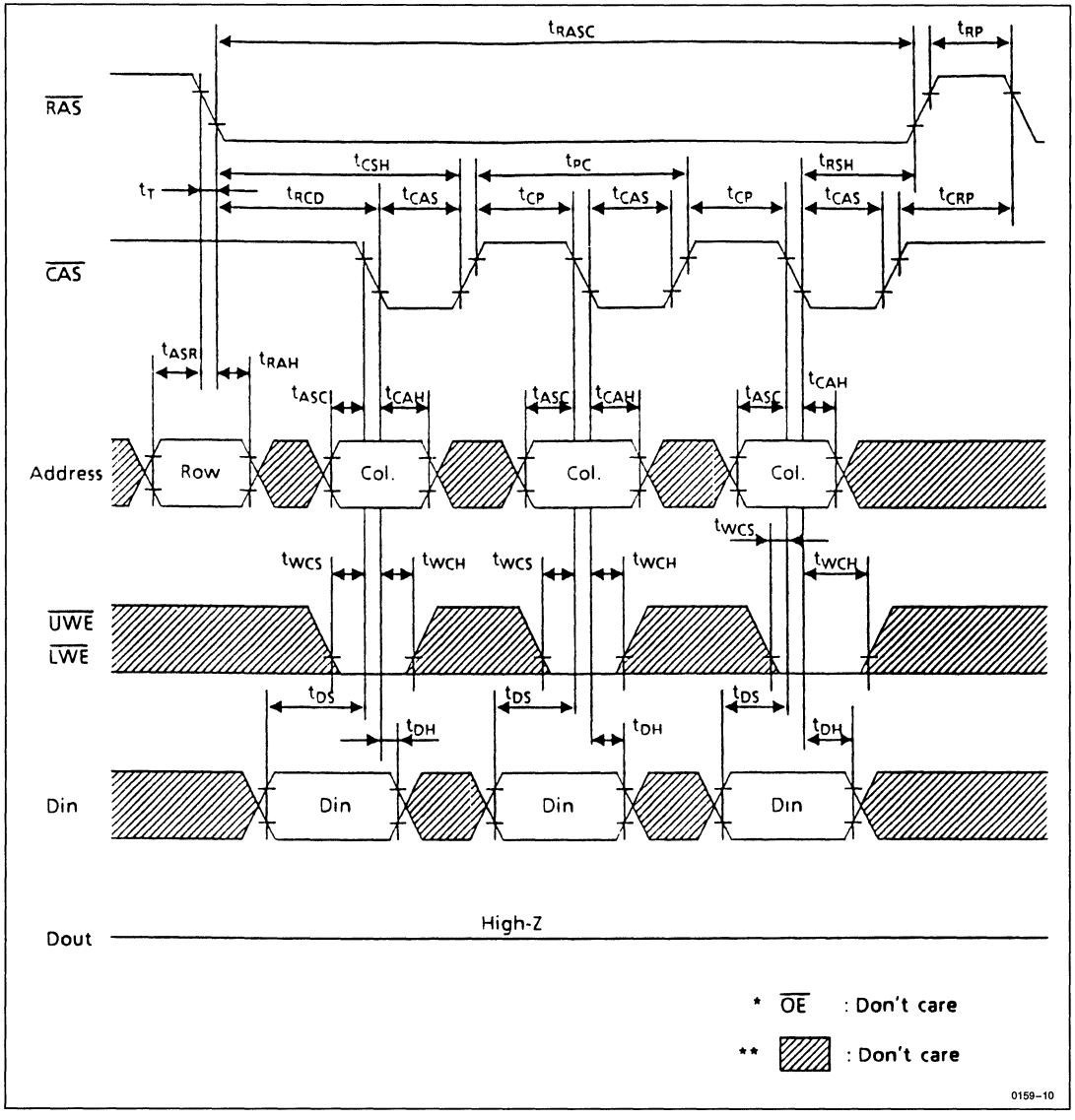
• **Hidden Refresh Cycle**



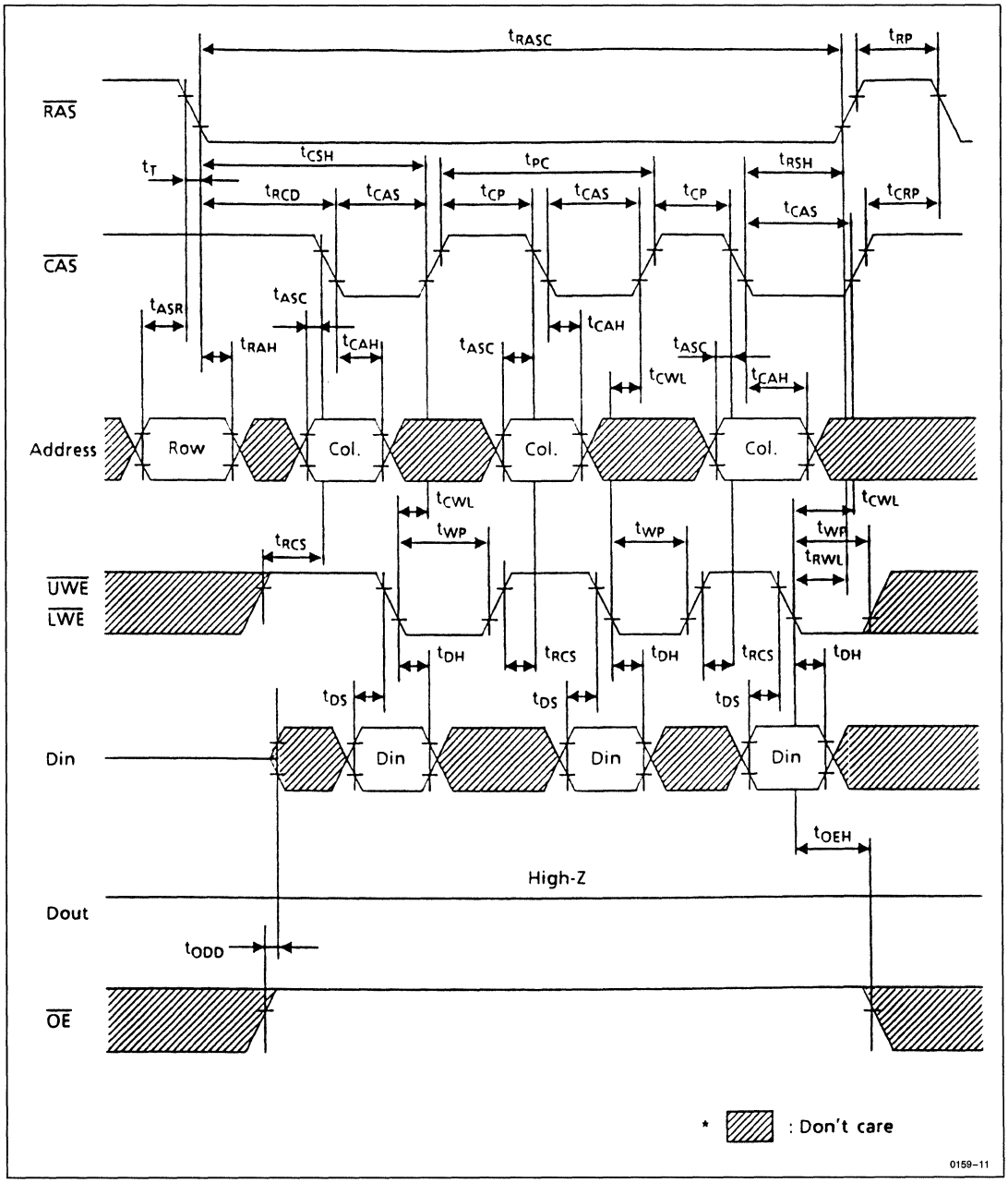
• **Fast Page Mode Read Cycle**



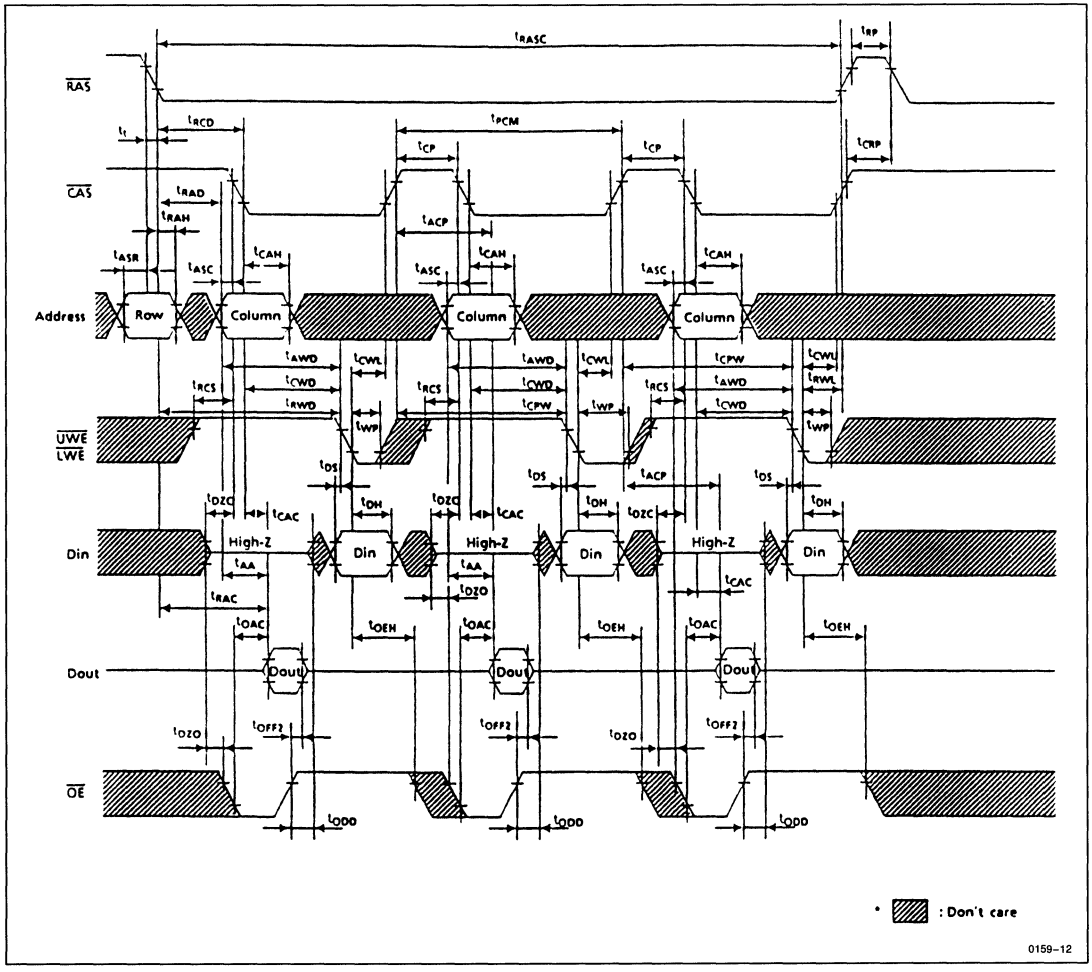
• **Fast Page Mode Early Write Cycle**



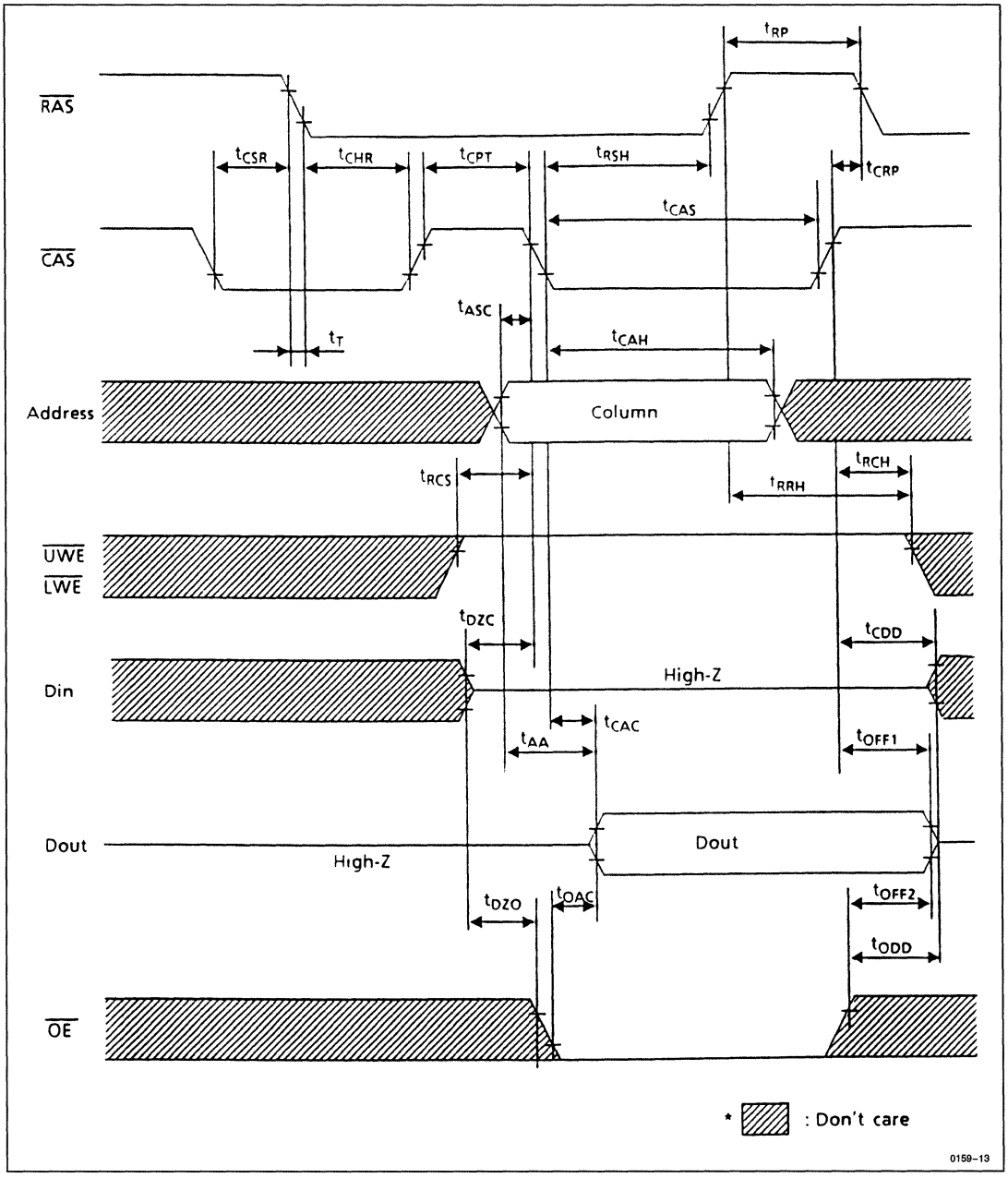
• **Fast Page Mode Delayed Write Cycle**



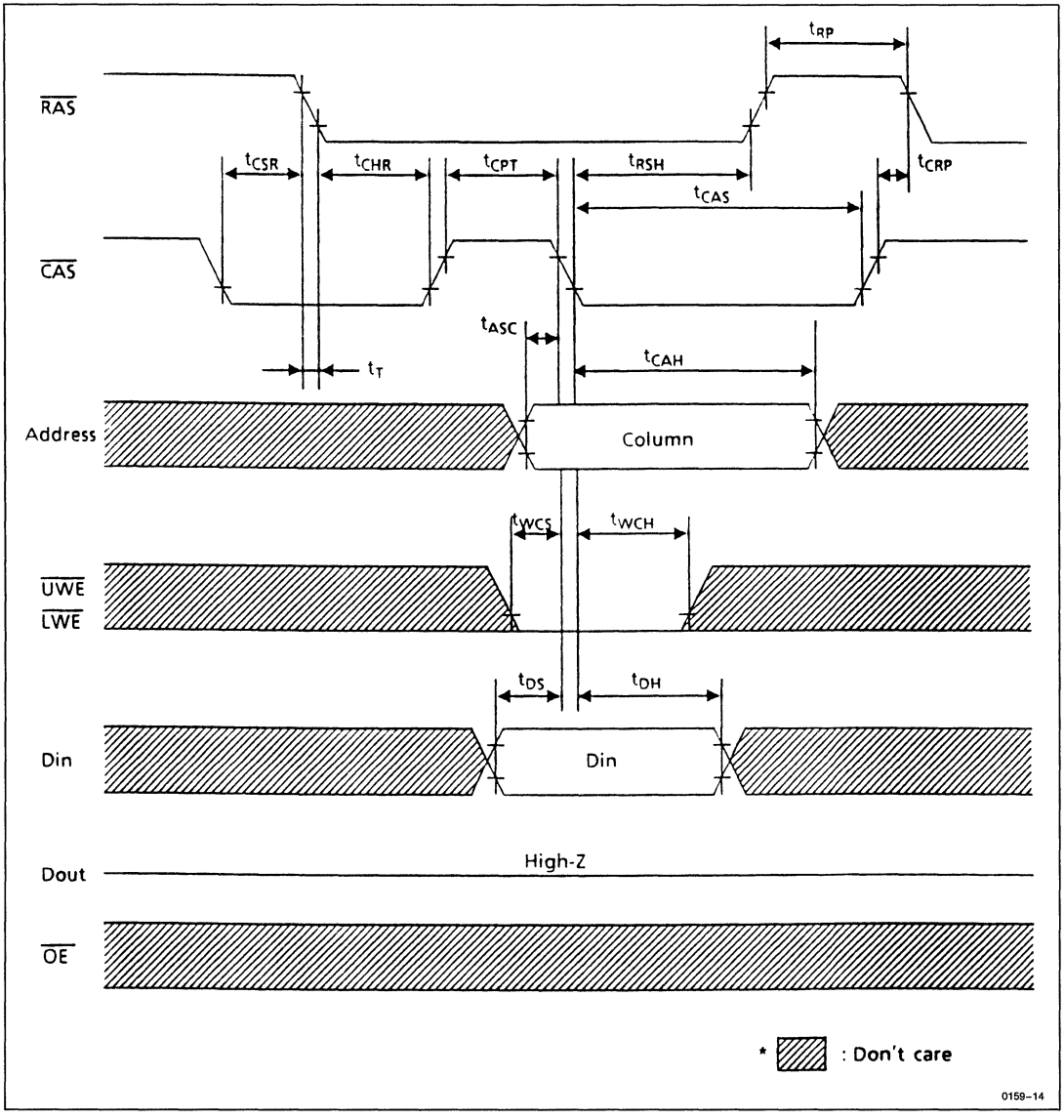
• **Fast Page Mode Read-Modify-Write Cycle**



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM514280 Series — Preliminary

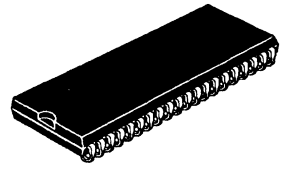
262,144-Word x 18-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514280 are CMOS dynamic RAM organized as 262,144-word x 18-bit. HM514280 have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514280 offer Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514280 to be packaged in standard 400 mil 40-pin plastic SOJ, standard 475 mil 40-pin plastic ZIP.

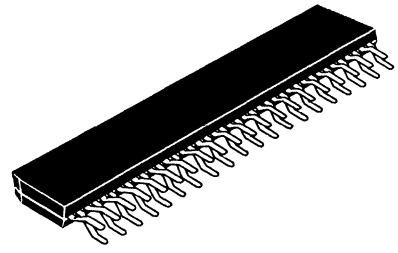
HM514280JP Series



3DCP40D

(CP-40D)

HM514280ZP Series



3DZP40

(ZP-40)

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode .....935 mW/825 mW/715 mW (max)
  - Standby Mode.....11 mW (max)
- Fast Page Mode Capability
- 512 Refresh Cycles .....(8 ms)
- 2$\overline{CAS}$ Byte Control
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh

■ ORDERING INFORMATION

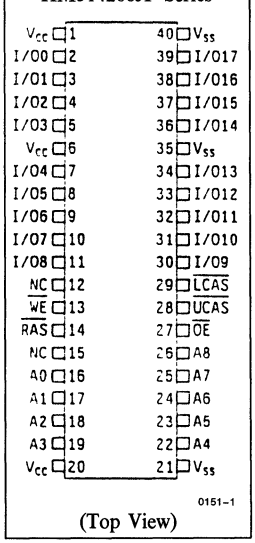
Part No.	Access Time	Package
HM514280JP-7	70 ns	400 mil 40-pin
HM514280JP-8	80 ns	Plastic SOJ
HM514280JP-10	100 ns	(CP-40D)
HM514280ZP-7	70 ns	475 mil 40-pin
HM514280ZP-8	80 ns	Plastic ZIP
HM514280ZP-10	100 ns	(ZP-40)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Input
—Row Address	A_0–A_8
—Column Address	A_0–A_8
—Refresh Address	A_0–A_8
I/O_0–I/O_{17}	Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$, $\overline{LCAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

■ PIN OUT

HM514280JP Series



0151-1

(Top View)

HM514280ZP Series

I/O_{11}	2	1	I/O_{10}
I/O_{13}	4	3	I/O_{12}
I/O_{14}	6	5	V_{SS}
I/O_{16}	8	7	I/O_{15}
V_{SS}	10	9	I/O_{17}
I/O_0	12	11	V_{CC}
I/O_2	14	13	I/O_1
V_{CC}	16	15	I/O_3
I/O_5	18	17	I/O_4
I/O_7	20	19	I/O_6
NC	22	21	I/O_8
$\overline{RAS}$	24	23	$\overline{WE}$
A_0	26	25	NC
A_2	28	27	A_1
V_{CC}	30	29	A_3
A_4	32	31	V_{SS}
A_6	34	33	A_5
A_8	36	35	A_7
$\overline{UCAS}$	38	37	$\overline{OE}$
I/O_9	40	39	$\overline{LCAS}$

(Bottom View)

■ TRUTH TABLE

Inputs					I/O		Operation
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	I/O_0–I/O_8	I/O_9–I/O_{17}	
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	D_{out}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D_{out}	Upper Byte Read
L	L	L	H	L	D_{out}	D_{out}	Word Read
L	L	H	L	H	D_{in}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D_{in}	Upper Byte Write
L	L	L	L	H	D_{in}	D_{in}	Word Write
L	L	L	H	H	High-Z	High-Z	

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	−1.0	—	0.8	V	1
	(Others)	V_{IL}	−2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM514280-7		HM514280-8		HM514280-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	170	—	150	—	130	mA	$\overline{RAS}$ Cycling $\overline{LCAS}$ or $\overline{UCAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ = V_{IH}, D_{out} = High-Z	
		—	1	—	1	—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	150	—	130	—	110	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{LCAS}$ or $\overline{UCAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	150	—	130	—	110	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	130	—	120	—	110	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	μA	0V ≤ V_{in} ≤ 7V	

• **DC Electrical Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V) (continued)

Parameter	Symbol	HM514280-7		HM514280-8		HM514280-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed ≤1 time while $\overline{RAS}$ = V_{IL}.
3. Address can be changed ≤1 time while $\overline{LCAS}$ and $\overline{UCAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{LCAS}$ and $\overline{UCAS}$ = V_{IH} to disable D_{out}.

• **AC Electrical Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 14, 15]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514280-7		HM514280-8		HM514280-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	20	60	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	15	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	20	—	20	—	25	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514280-7		HM514280-8		HM514280-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	3, 4, 13
Access Time from Address	t_{AA}	—	35	—	40	—	45	ns	3, 5, 13
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	35	—	40	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	15	0	15	0	20	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	15	0	15	0	20	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	15	—	15	—	20	—	ns	

Write Cycle

Parameter	Symbol	HM514280-7		HM514280-8		HM514280-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514280-7		HM514280-8		HM514280-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	180	—	200	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	95	—	105	—	135	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	45	—	45	—	60	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	60	—	65	—	80	—	ns	10, 13
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	20	—	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM514280-7		HM514280-8		HM514280-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time in Normal Mode	t_{CPN}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514280-7		HM514280-8		HM514280-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	ns	3, 13
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	ns	
Fast Page Mode Read-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPW}	65	—	70	—	85	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	95	—	100	—	110	—	ns	

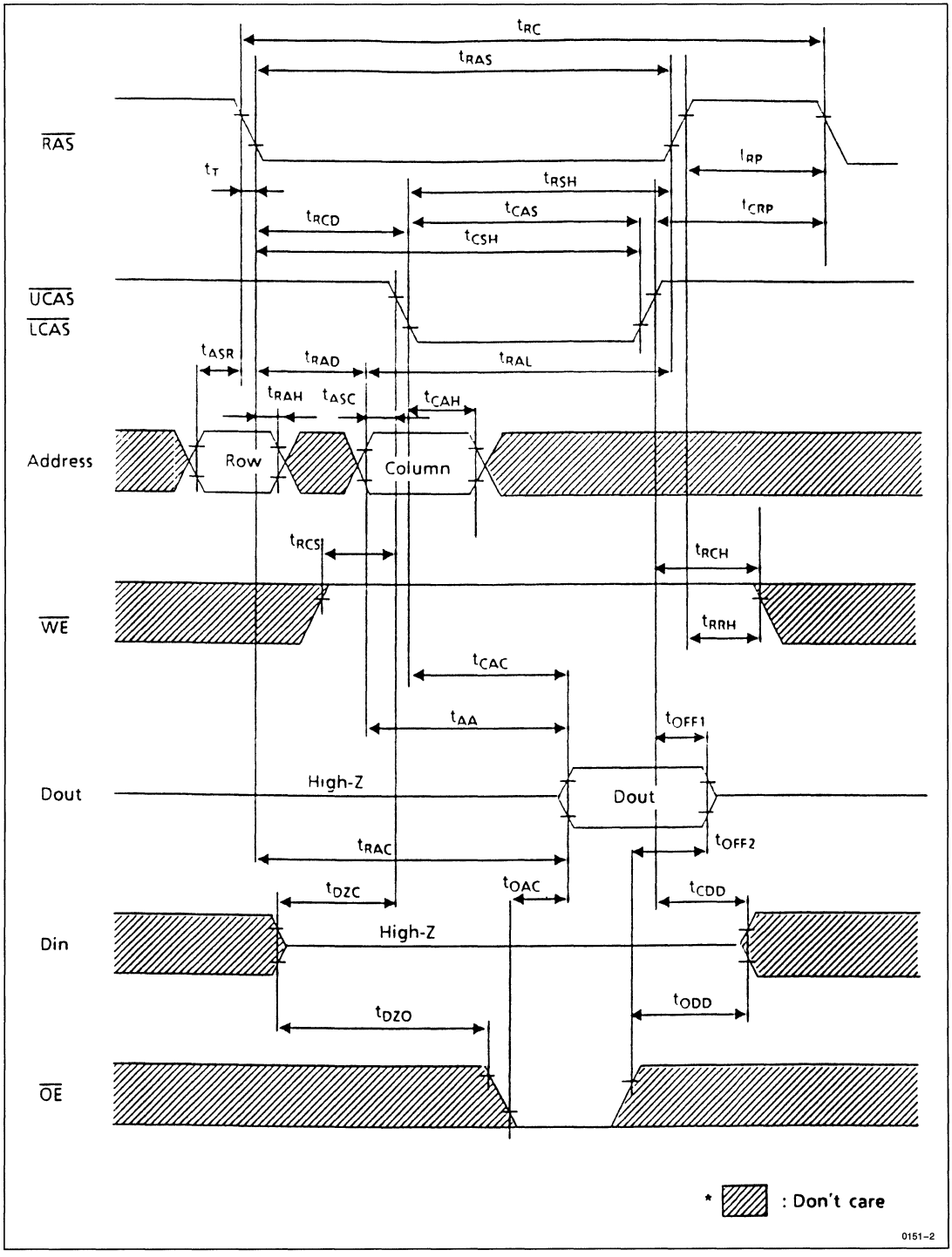
Counter Test Cycle

Parameter	Symbol	HM514280-7		HM514280-8		HM514280-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	50	—	50	—	50	—	ns	

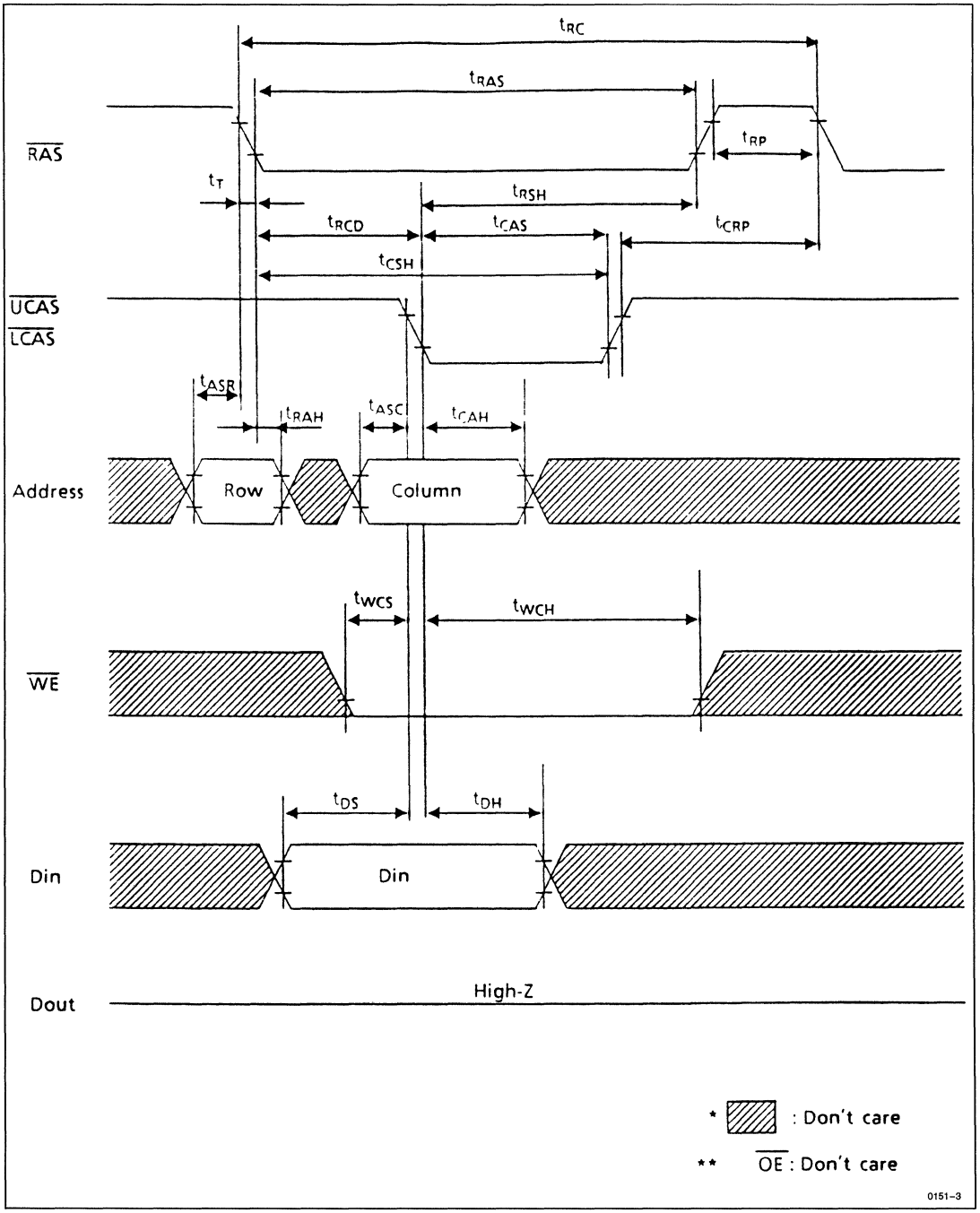
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Either t_{RCH} or T_{RRH} must be satisfied for a read cycle.
17. When both $\overline{LCAS}$ and $\overline{UCAS}$ go low at the same time, all 18-bits data are written into the device. $\overline{LCAS}$ and $\overline{UCAS}$ cannot be staggered within the same write/read cycles.

■ TIMING WAVEFORMS

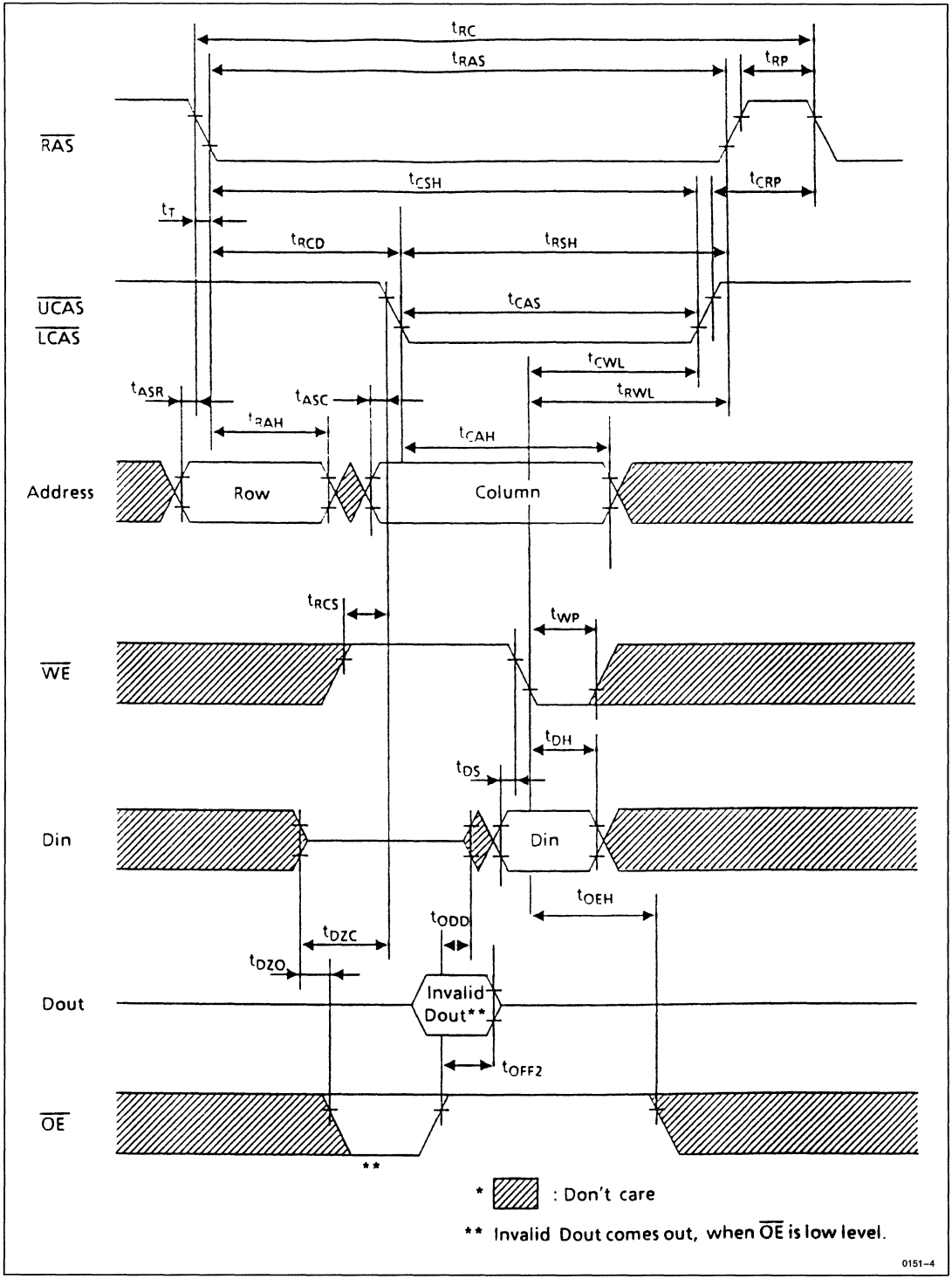
• Read Cycle



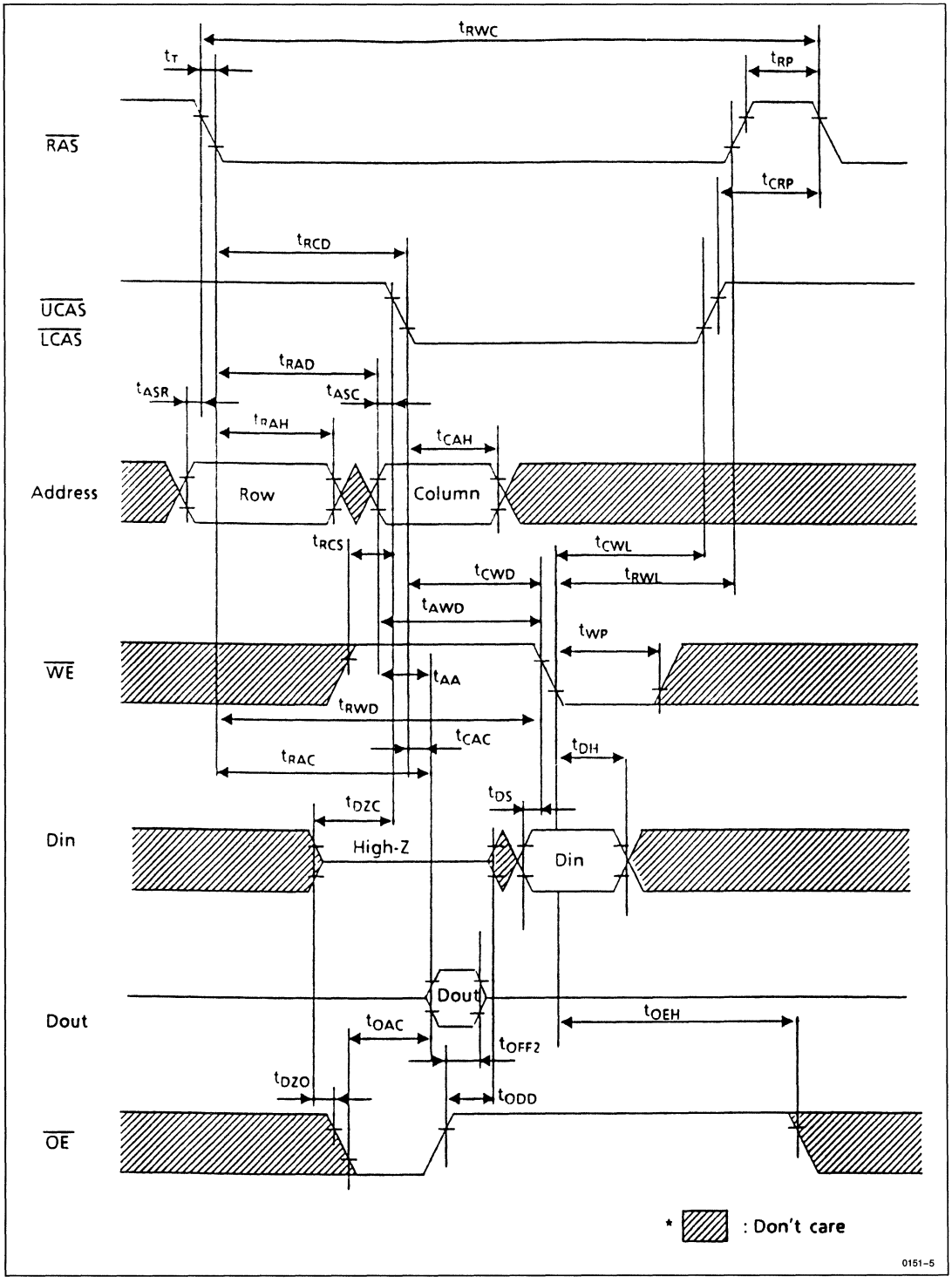
• **Early Write Cycle**



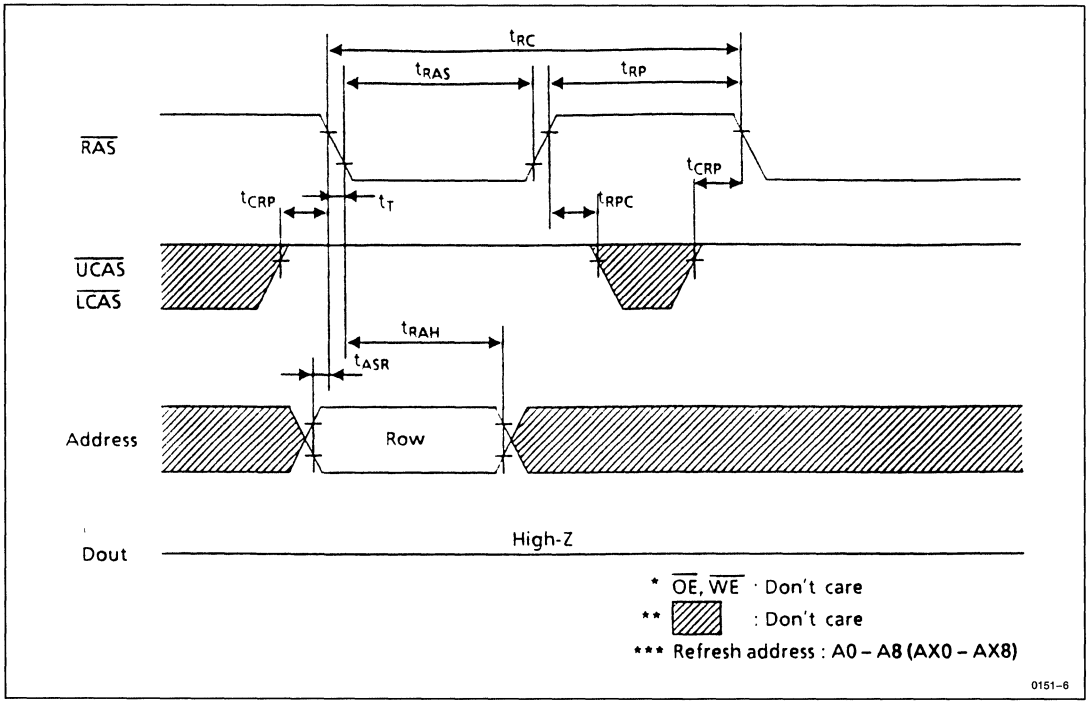
• **Delayed Write Cycle**



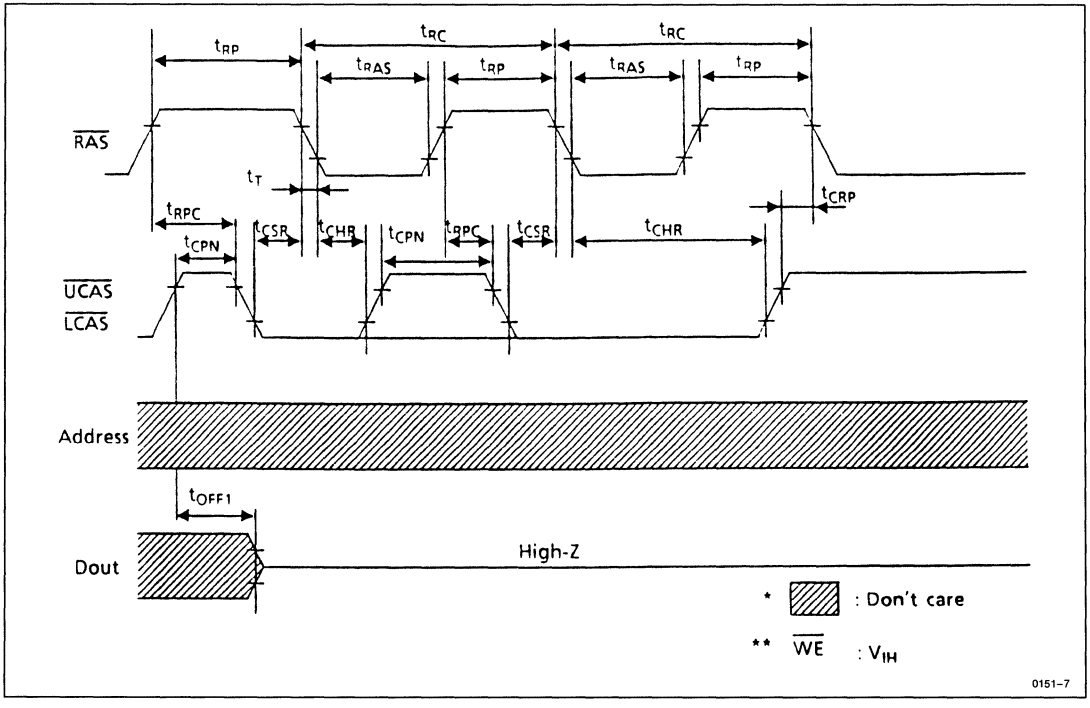
• **Read-Modify-Write Cycle**



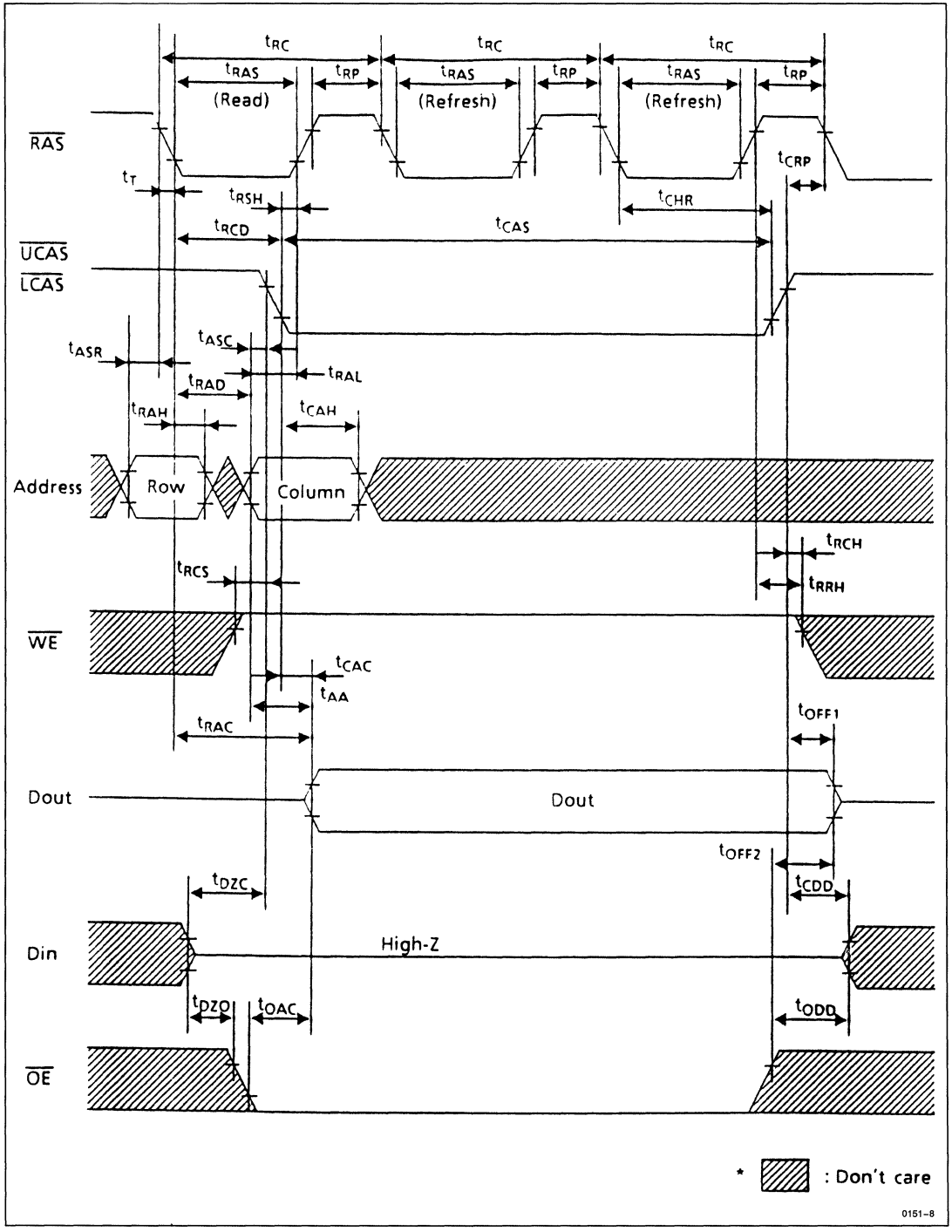
• $\overline{RAS}$ Only Refresh Cycle



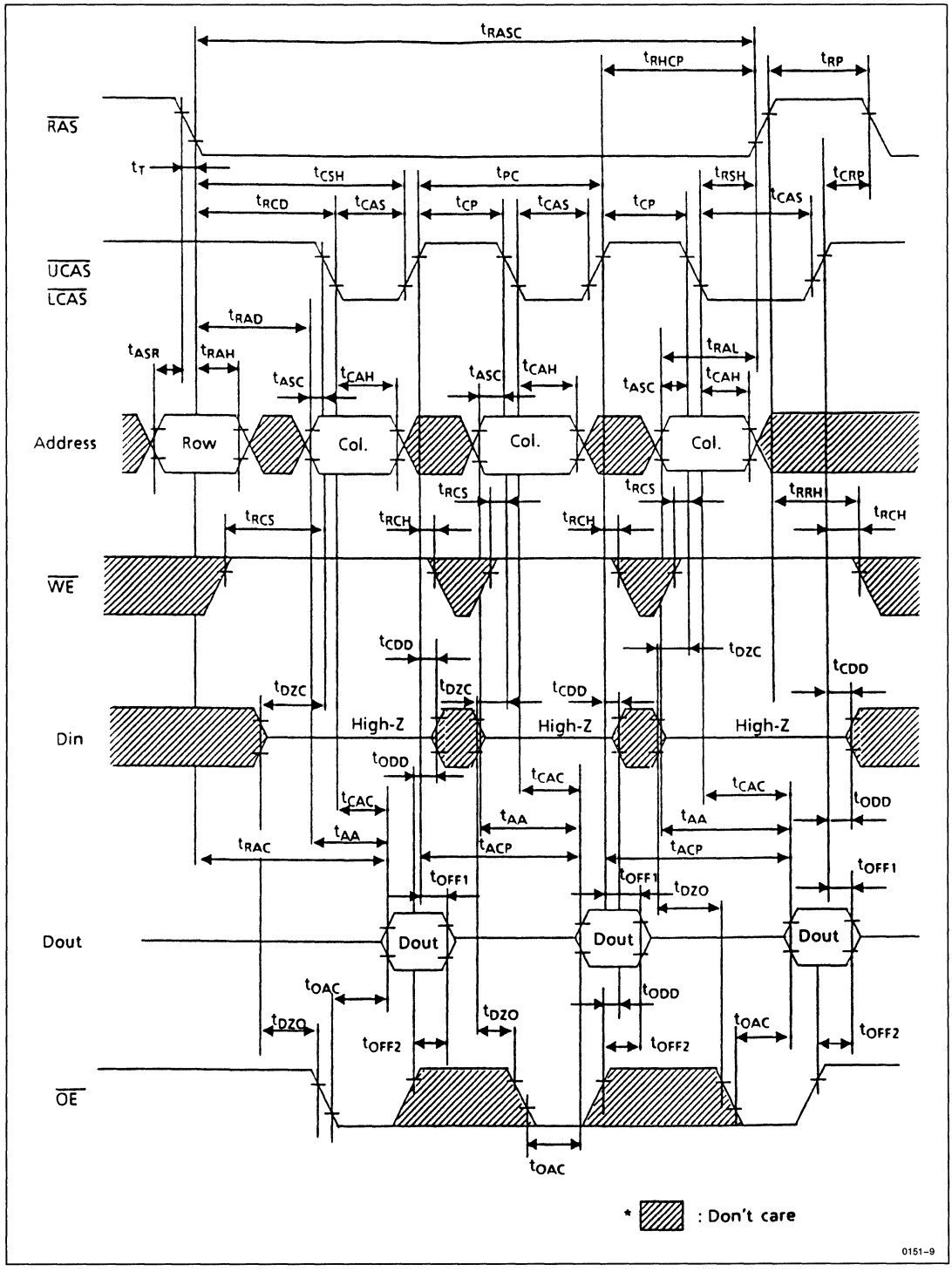
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



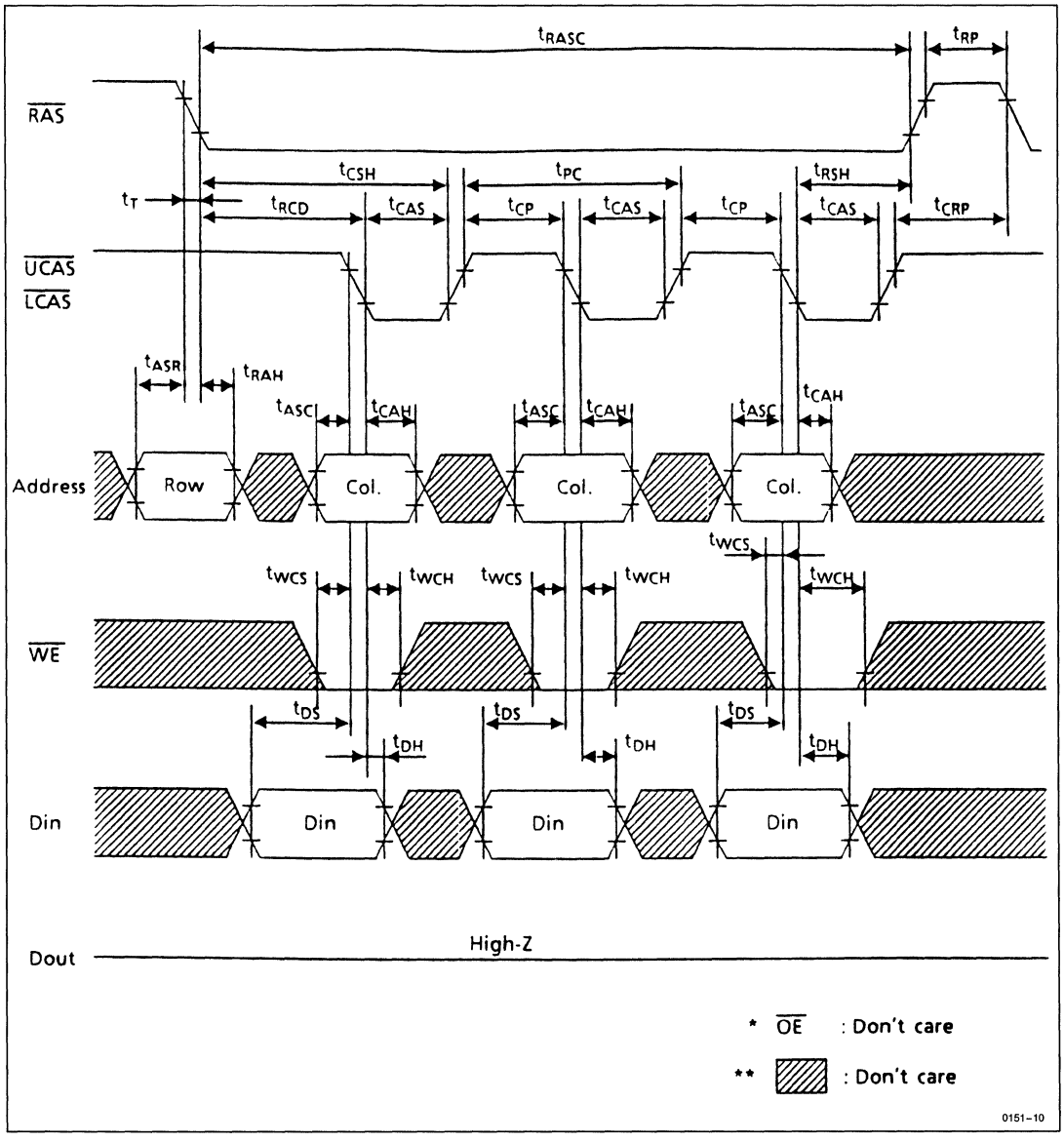
• Hidden Refresh Cycle



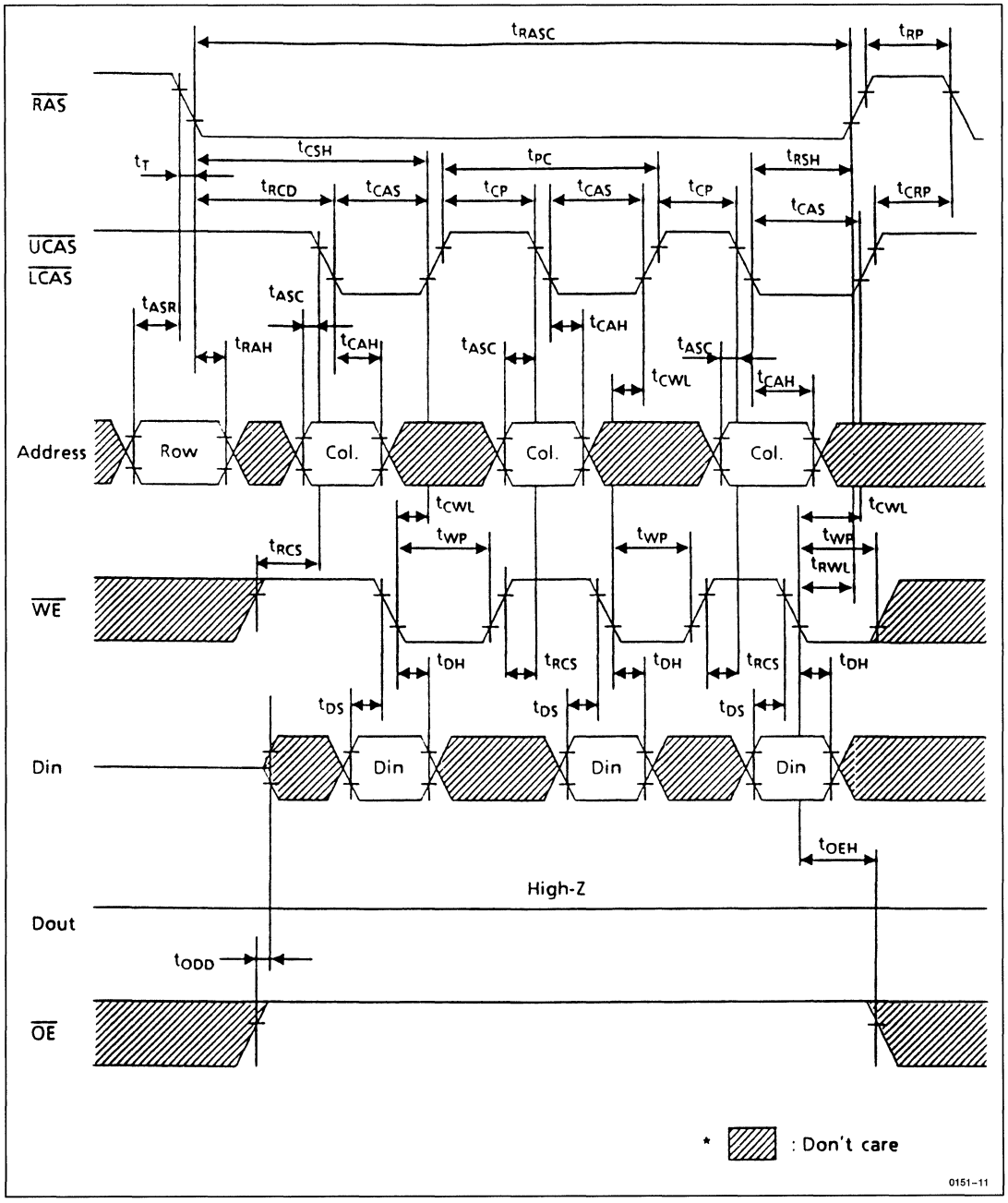
• **Fast Page Mode Read Cycle**



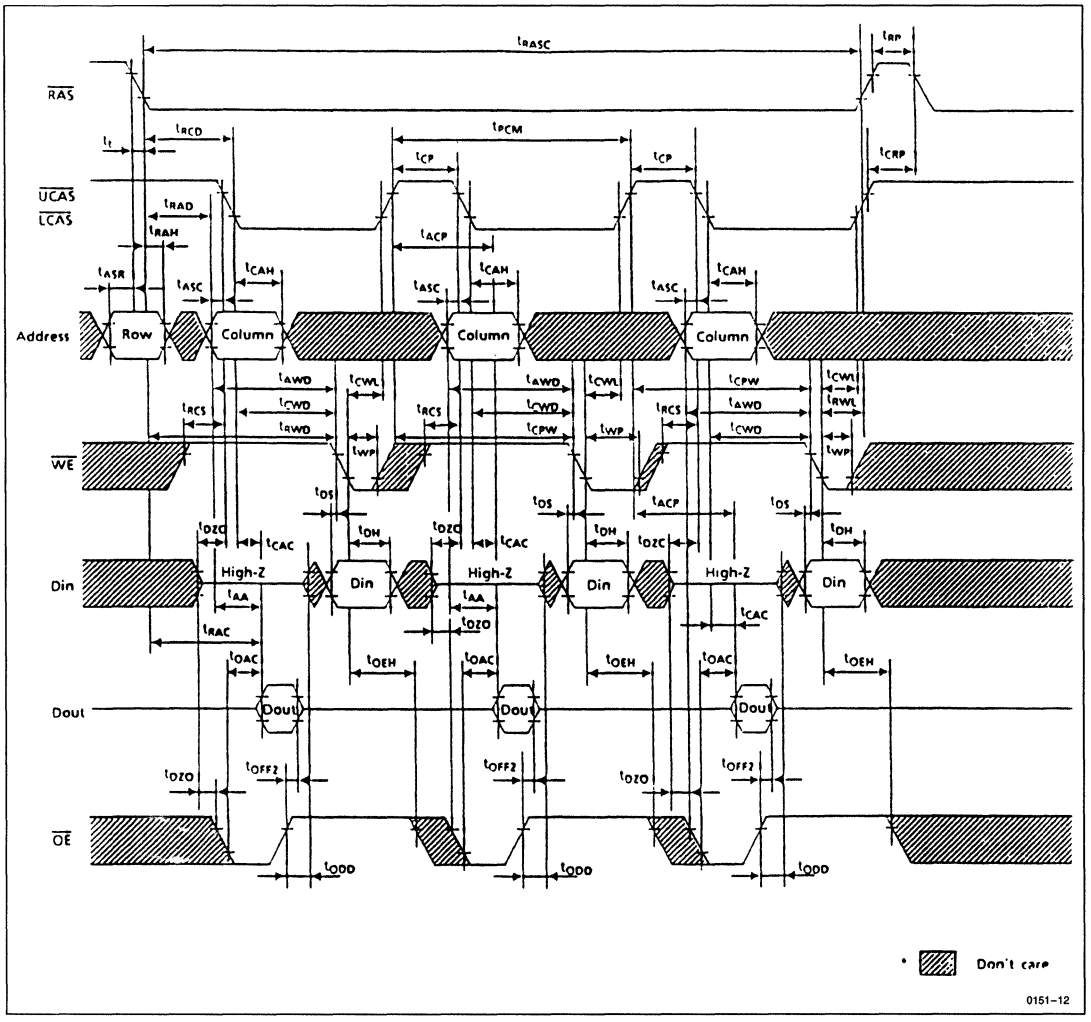
• **Fast Page Mode Early Write Cycle**



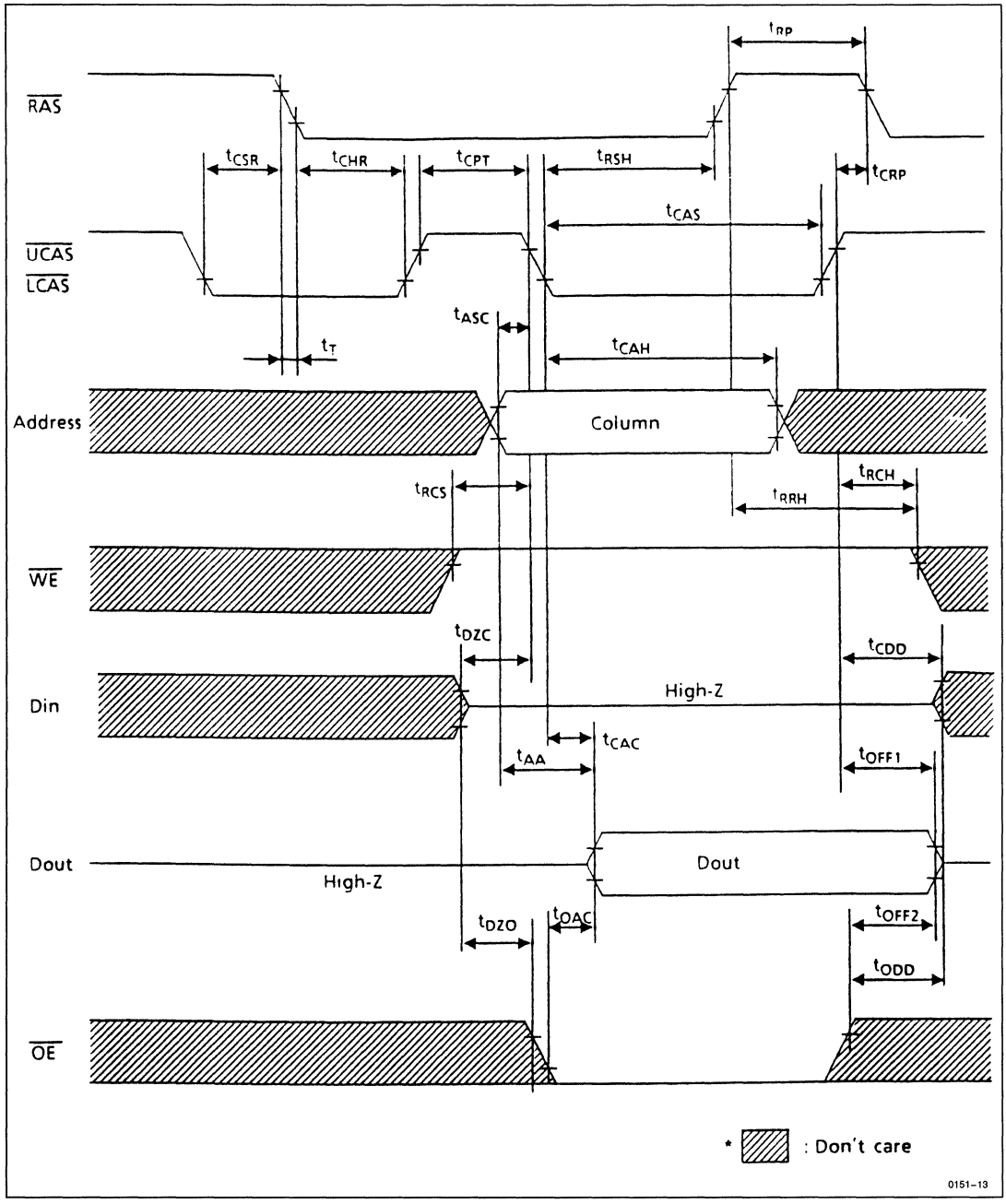
• **Fast Page Mode Delayed Write Cycle**



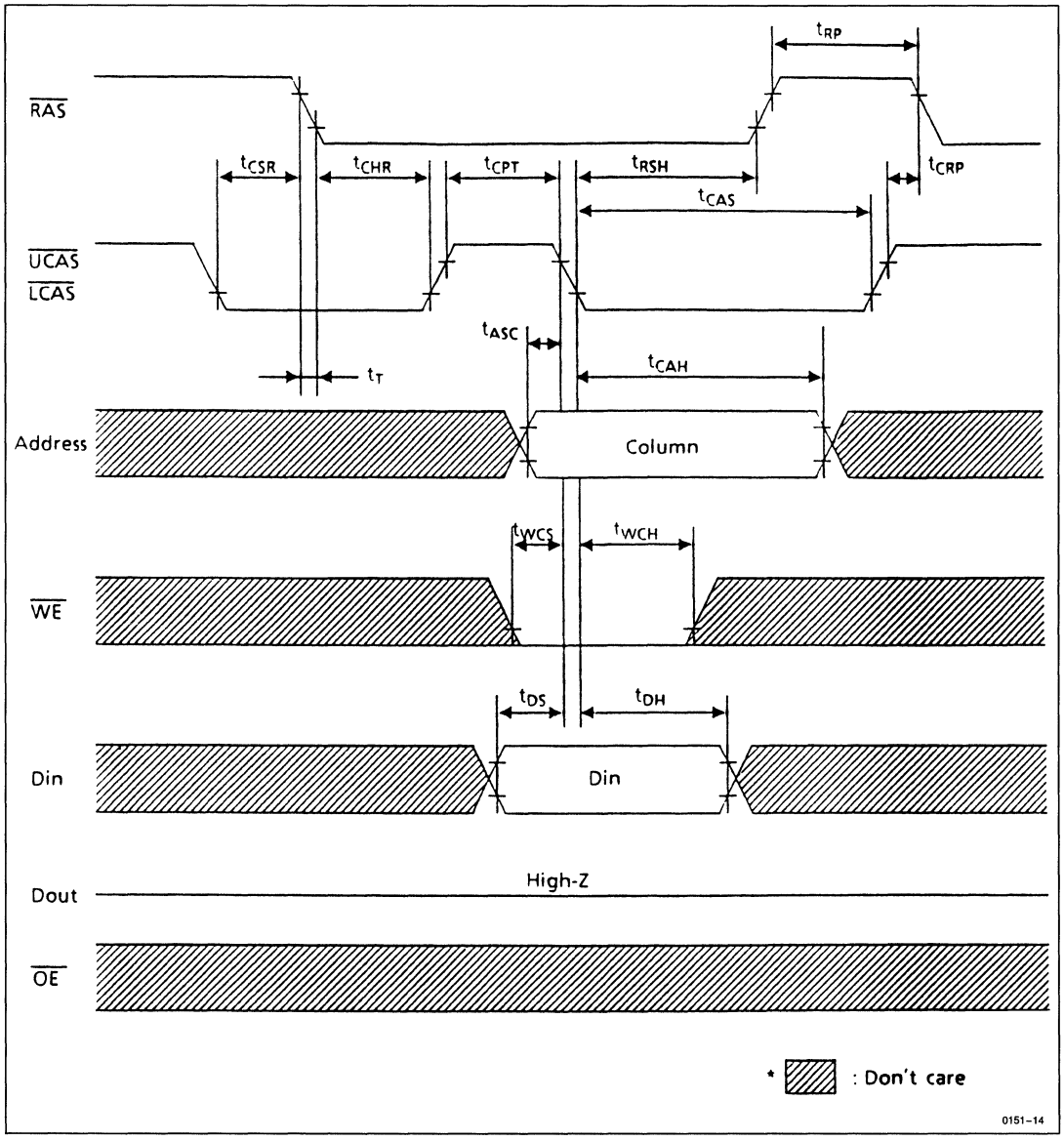
• Fast Page Mode Read-Modify-Write Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM514190 Series — Preliminary

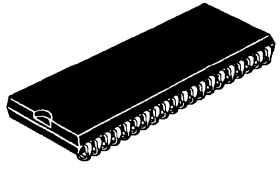
262,144-Word x 18-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM514190 are CMOS dynamic RAM organized as 262,144-word x 18-bit. HM514190 have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514190 offer Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514190 to be packaged in standard 400 mil 40-pin plastic SOJ, standard 475 mil 40-pin plastic ZIP.

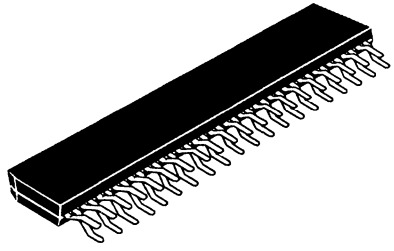
HM514190JP Series



3DCP40D

(CP-40D)

HM514190ZP Series



3DZP40

(ZP-40)

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode .....770 mW/660 mW/550 mW (max)
  - Standby Mode.....11 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles .....(16 ms)
- 2 $\overline{WE}$ Byte Control
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh

■ ORDERING INFORMATION

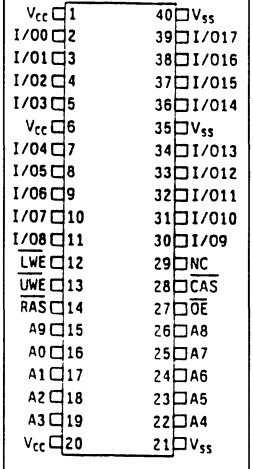
Part No.	Access Time	Package
HM514190JP-7	70 ns	400 mil 40-pin
HM514190JP-8	80 ns	Plastic SOJ
HM514190JP-10	100 ns	(CP-40D)
HM514190ZP-7	70 ns	475 mil 40-pin
HM514190ZP-8	80 ns	Plastic ZIP
HM514190ZP-10	100 ns	(ZP-40)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
—Row Address	A_0–A_9
—Column Address	A_0–A_7
—Refresh Address	A_0–A_9
I/O_0–I/O_{17}	Data-in/Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{UWE}$, $\overline{LWE}$	Read/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

■ PIN OUT

HM514190JP Series



0152-1

(Top View)

HM514190ZP Series

I/O_{11}	2		1	I/O_{10}
I/O_{13}	4		3	I/O_{12}
I/O_{14}	6		5	V_{SS}
I/O_{16}	8		7	I/O_{15}
V_{SS}	10		9	I/O_{17}
I/O_0	12		11	V_{CC}
I/O_2	14		13	I/O_1
V_{CC}	16		15	I/O_3
I/O_5	18		17	I/O_4
I/O_7	20		19	I/O_6
$\overline{LWE}$	22		21	I/O_8
$\overline{RAS}$	24		23	$\overline{UWE}$
A_0	26		25	A_9
A_2	28		27	A_1
V_{CC}	30		29	A_3
A_4	32		31	V_{SS}
A_6	34		33	A_5
A_8	36		35	A_7
$\overline{CAS}$	38		37	$\overline{OE}$
I/O_9	40		39	NC

(Bottom View)

■ TRUTH TABLE

Inputs					I/O		Operation
$\overline{RAS}$	$\overline{LWE}$	$\overline{UWE}$	$\overline{CAS}$	$\overline{OE}$	I/O_0–I/O_8	I/O_9–I/O_{17}	
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	H	H	L	L	D_{out}	D_{out}	Word Read
L	L	H	L	H	D_{in}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D_{in}	Upper Byte Write
L	L	L	L	H	D_{in}	D_{in}	Word Write
L	H	H	L	H	High-Z	High-Z	

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage		V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	(I/O Pin)	V_{IL}	− 1.0	—	0.8	V	1
	(Others)	V_{IL}	− 2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HM514190-7		HM514190-8		HM514190-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	140	—	120	—	100	mA	$\overline{RAS}$ Cycling $\overline{CAS}$ Cycling t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	1	—	1	—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	150	—	130	—	110	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	150	—	130	—	110	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	130	—	120	—	110	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	

• **DC Electrical Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V) (continued)

Parameter	Symbol	HM514190-7		HM514190-8		HM514190-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 14, 15]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514190-7		HM514190-8		HM514190-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	20	60	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	15	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	20	—	20	—	25	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514190-7		HM514190-8		HM514190-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	3, 4, 13
Access Time from Address	t_{AA}	—	35	—	40	—	45	ns	3, 5, 13
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	35	—	40	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	15	0	15	0	20	ns	6
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}	0	15	0	15	0	20	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	15	—	15	—	20	—	ns	

Write Cycle

Parameter	Symbol	HM514190-7		HM514190-8		HM514190-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514190-7		HM514190-8		HM514190-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	180	—	200	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	95	—	105	—	135	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	45	—	45	—	60	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	60	—	65	—	80	—	ns	10, 13
$\overline{OE}$ to Hold Time from $\overline{WE}$	t_{OEH}	20	—	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM514190-7		HM514190-8		HM514190-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time in Normal Mode	t_{CPN}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514190-7		HM514190-8		HM514190-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	ns	3, 13
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	ns	
Fast Page Mode Read-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPW}	65	—	70	—	85	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	95	—	100	—	110	—	ns	

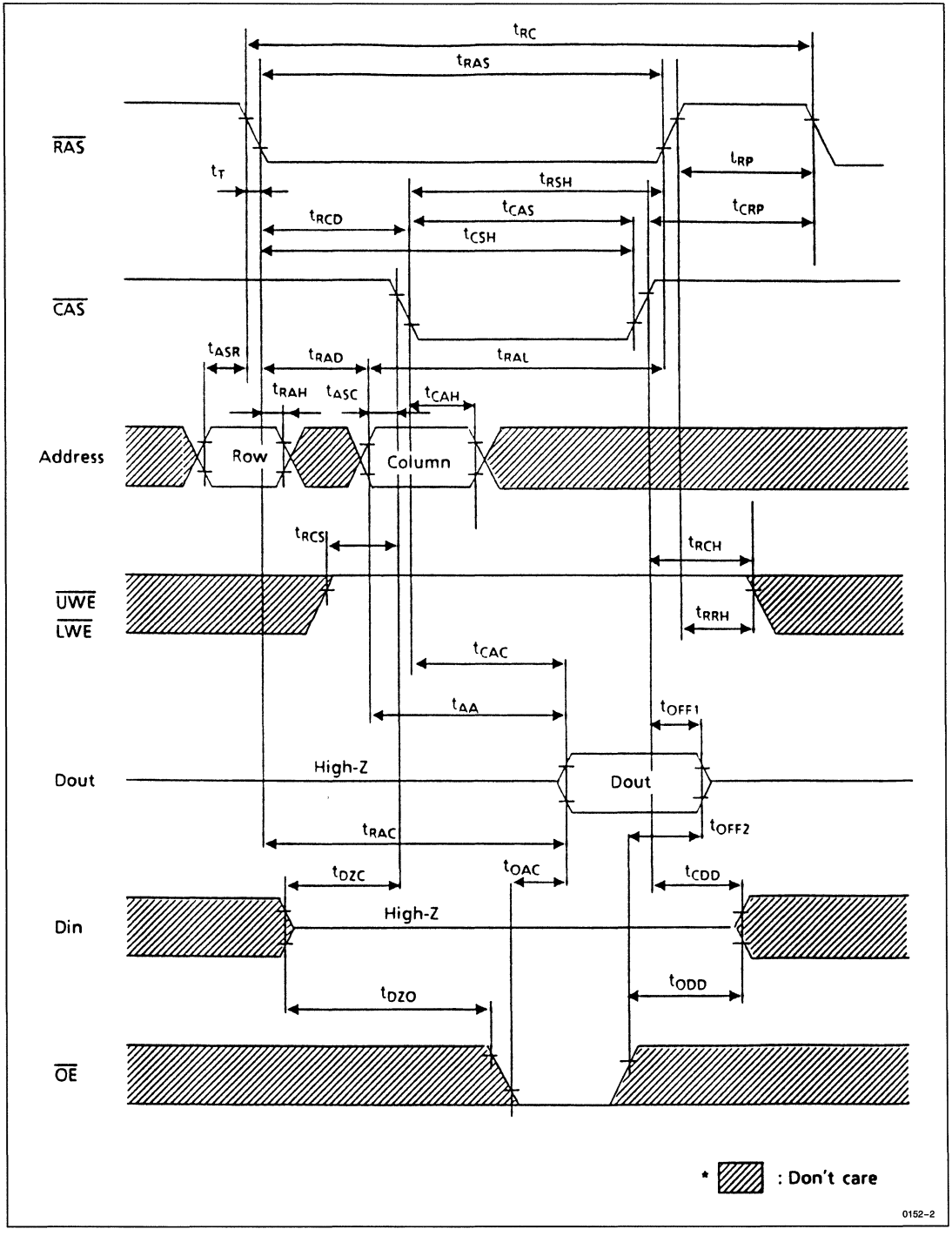
Counter Test Cycle

Parameter	Symbol	HM514190-7		HM514190-8		HM514190-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	50	—	50	—	50	—	ns	

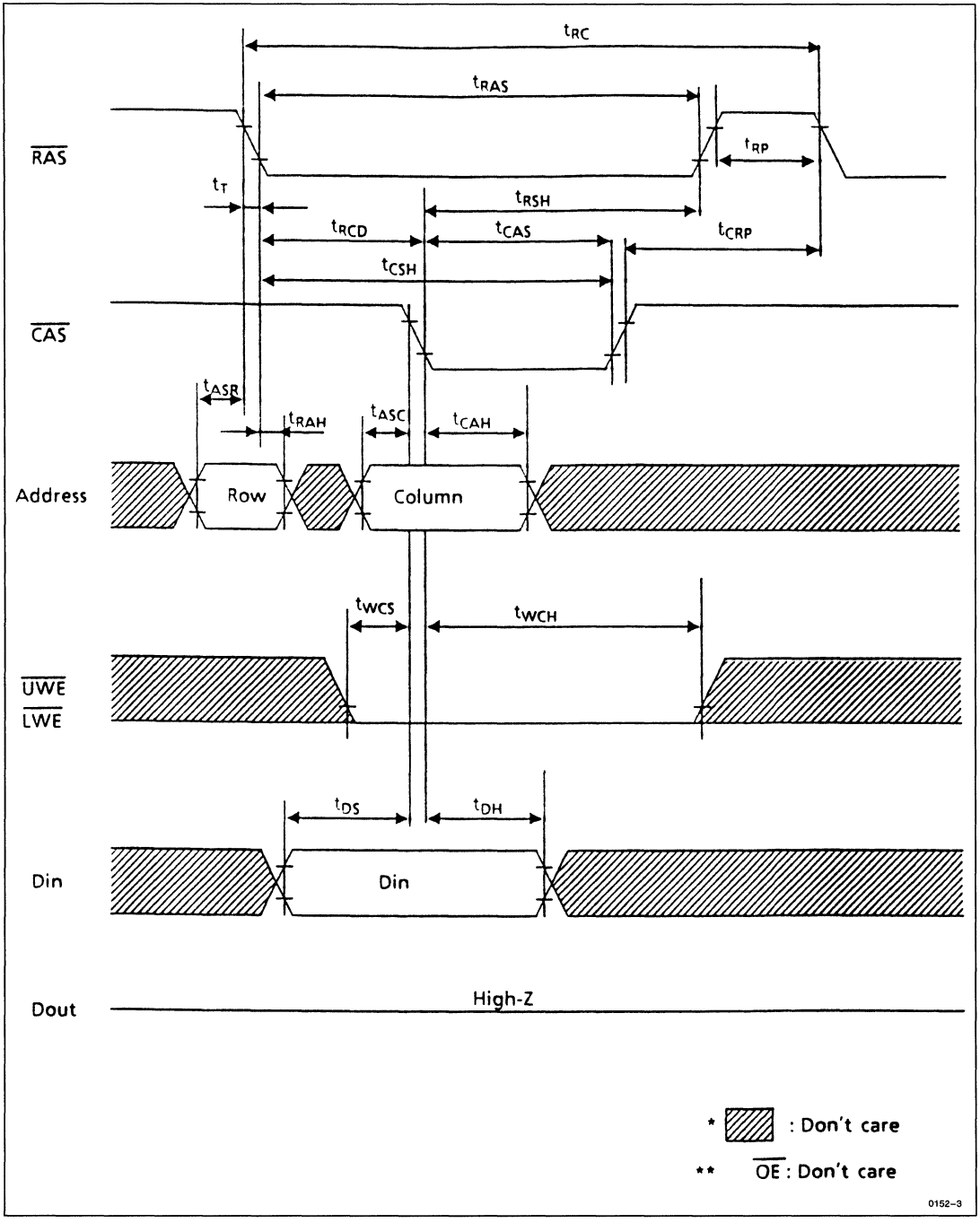
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Either t_{RCH} or T_{RRH} must be satisfied for a read cycle.
17. When both $\overline{LWE}$ and $\overline{UWE}$ go low at the same time, all 16-bits data are written into the device. $\overline{LWE}$ and $\overline{UWE}$ cannot be staggered within the same write cycles.

■ TIMING WAVEFORMS

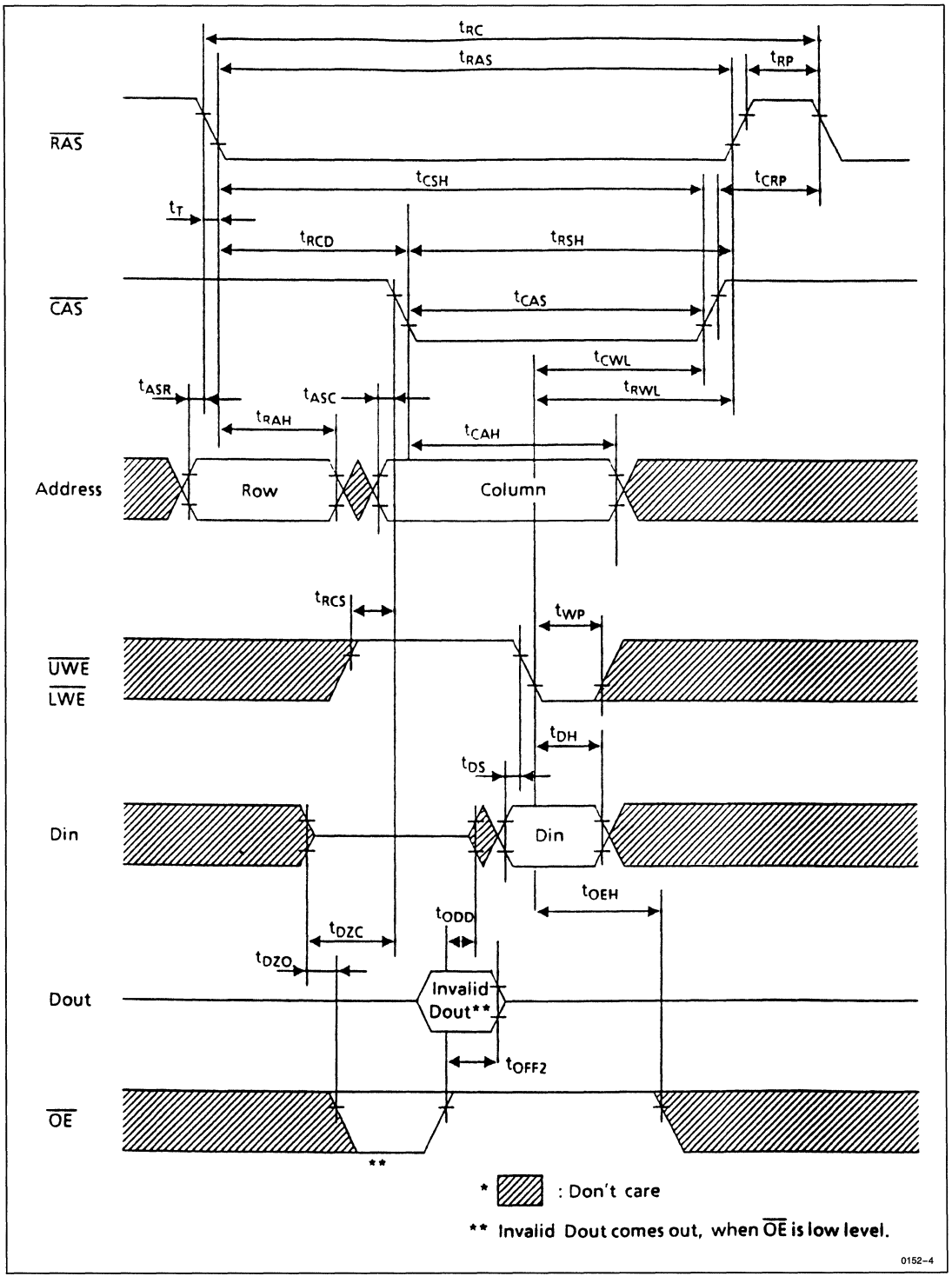
• Read Cycle



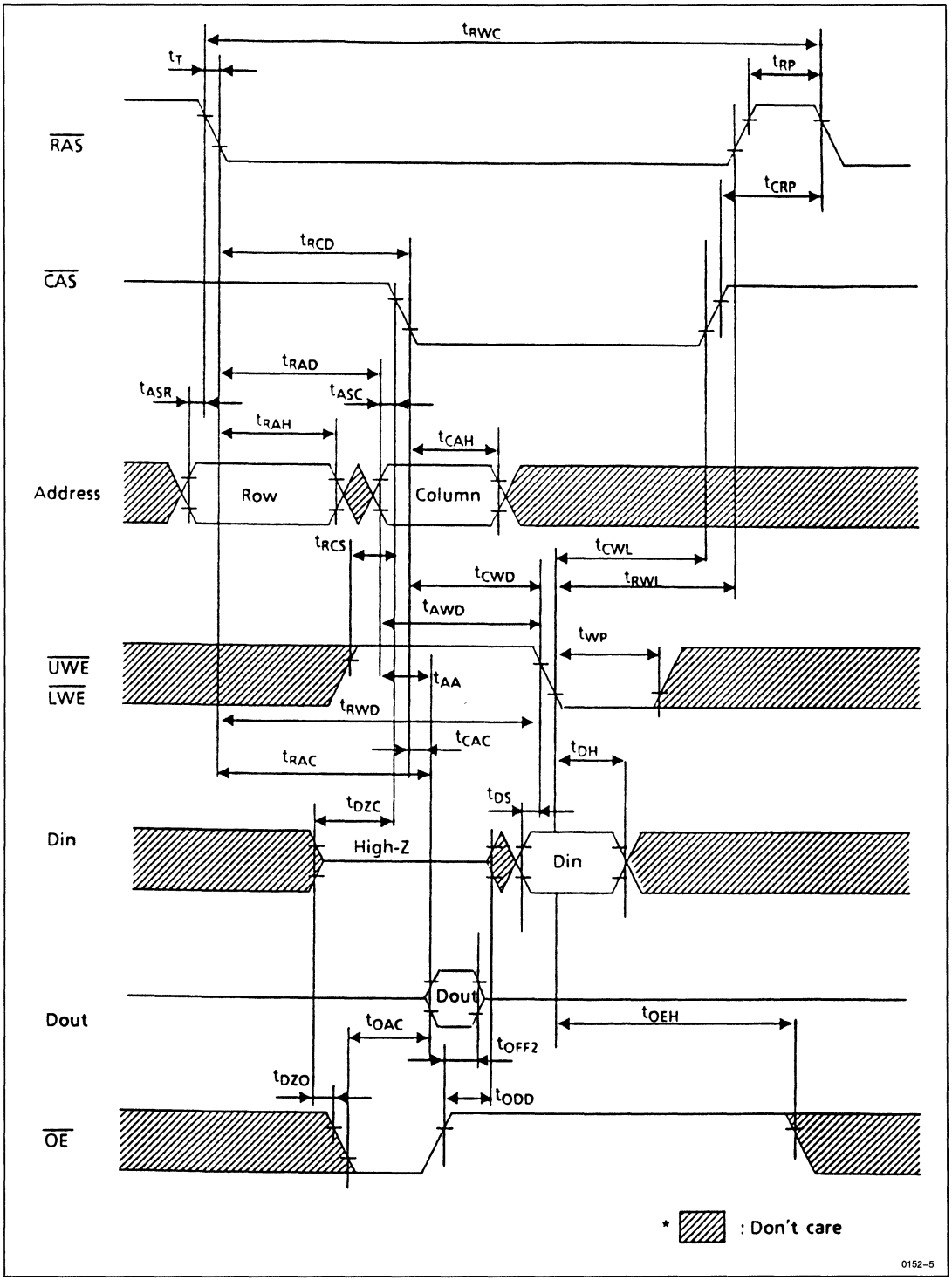
• **Early Write Cycle**



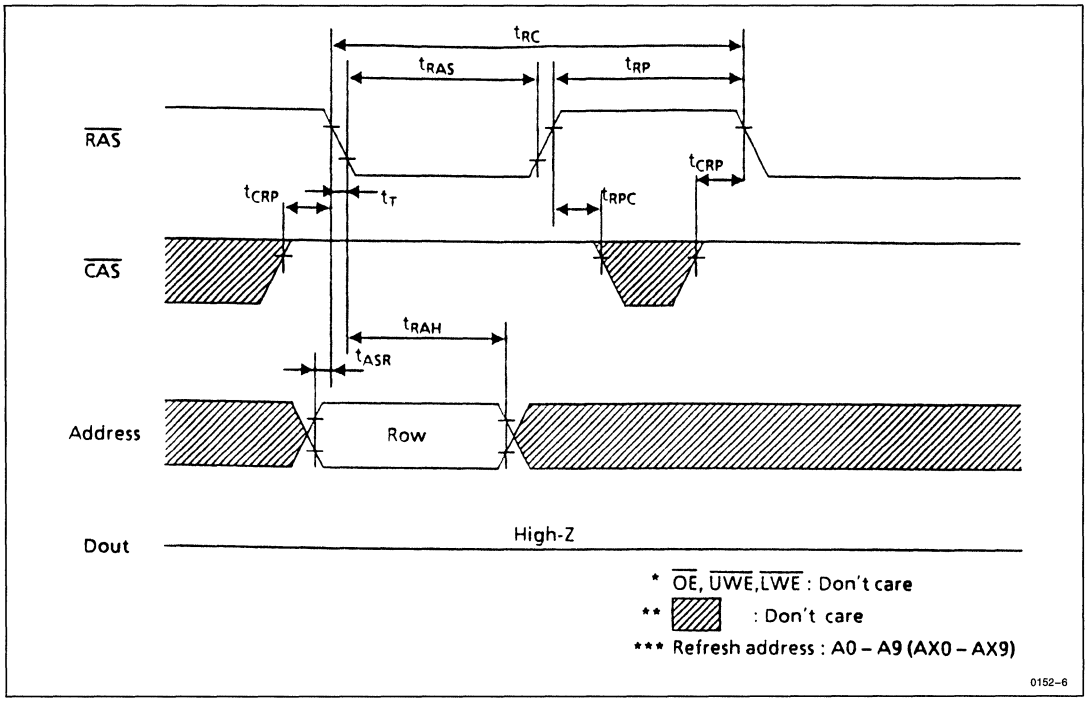
• **Delayed Write Cycle**



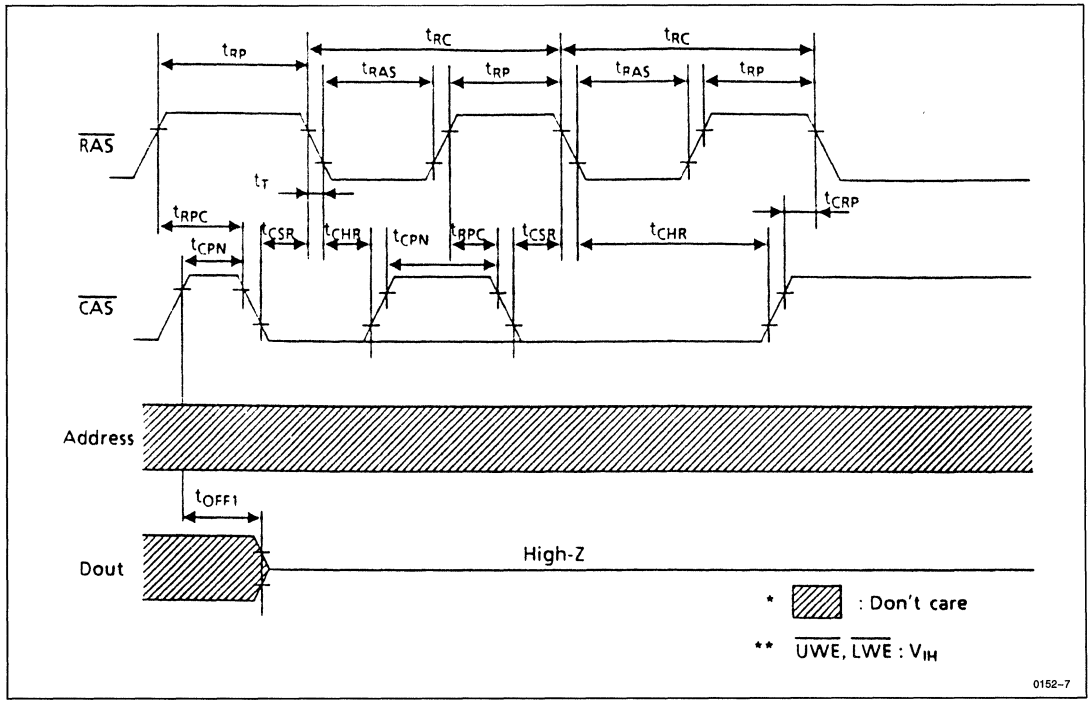
• **Read-Modify-Write Cycle**



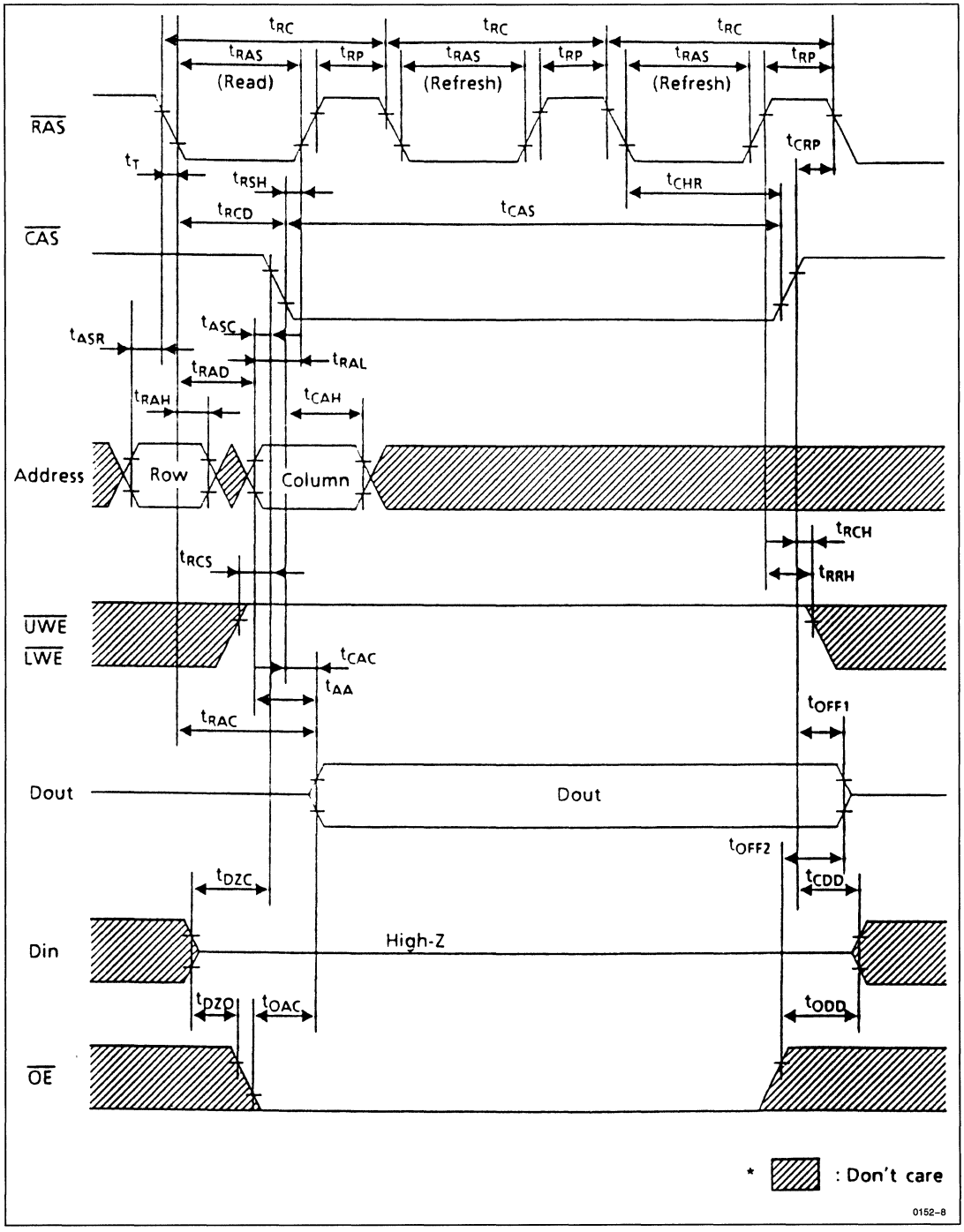
• $\overline{RAS}$ Only Refresh Cycle



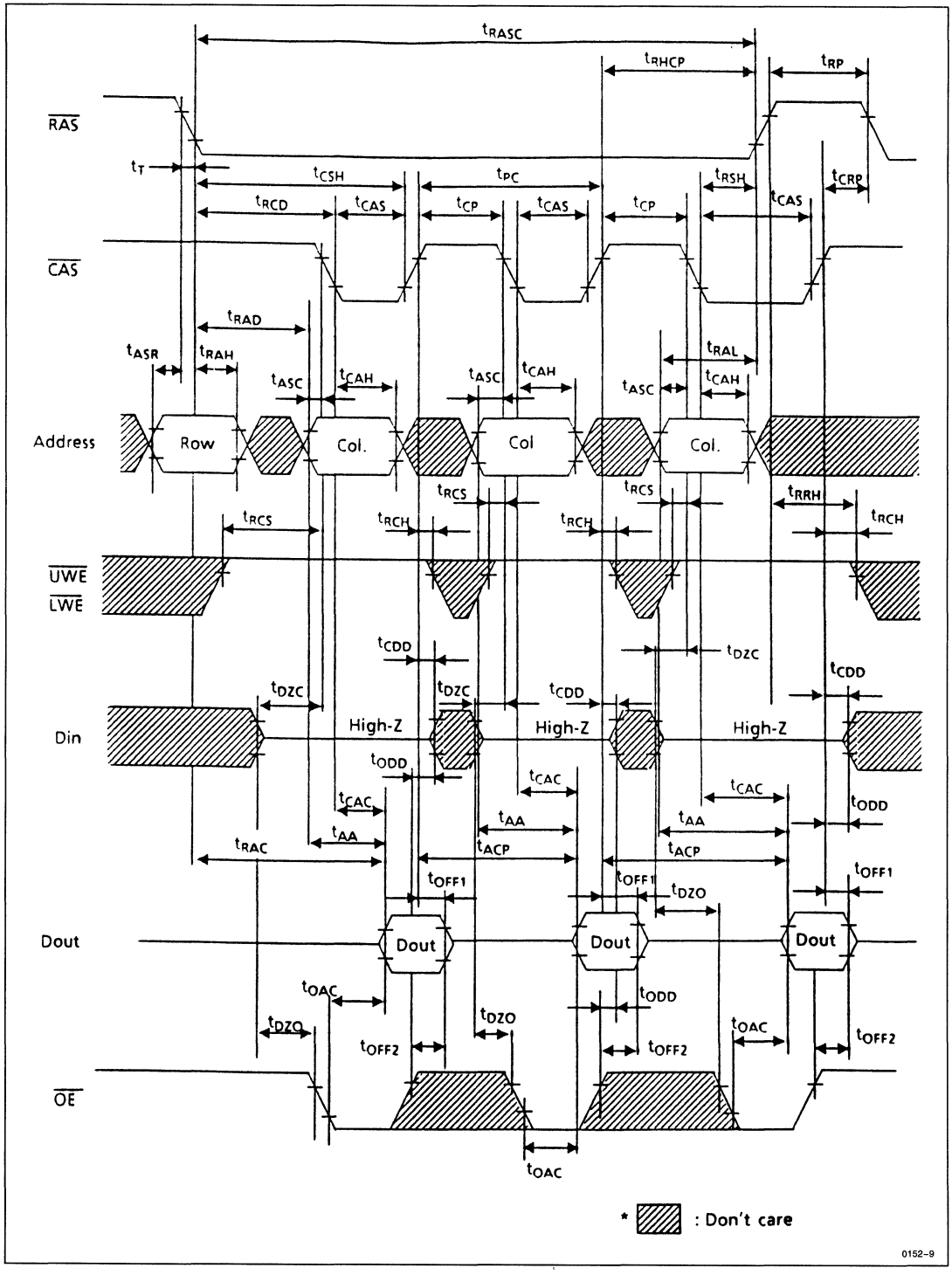
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



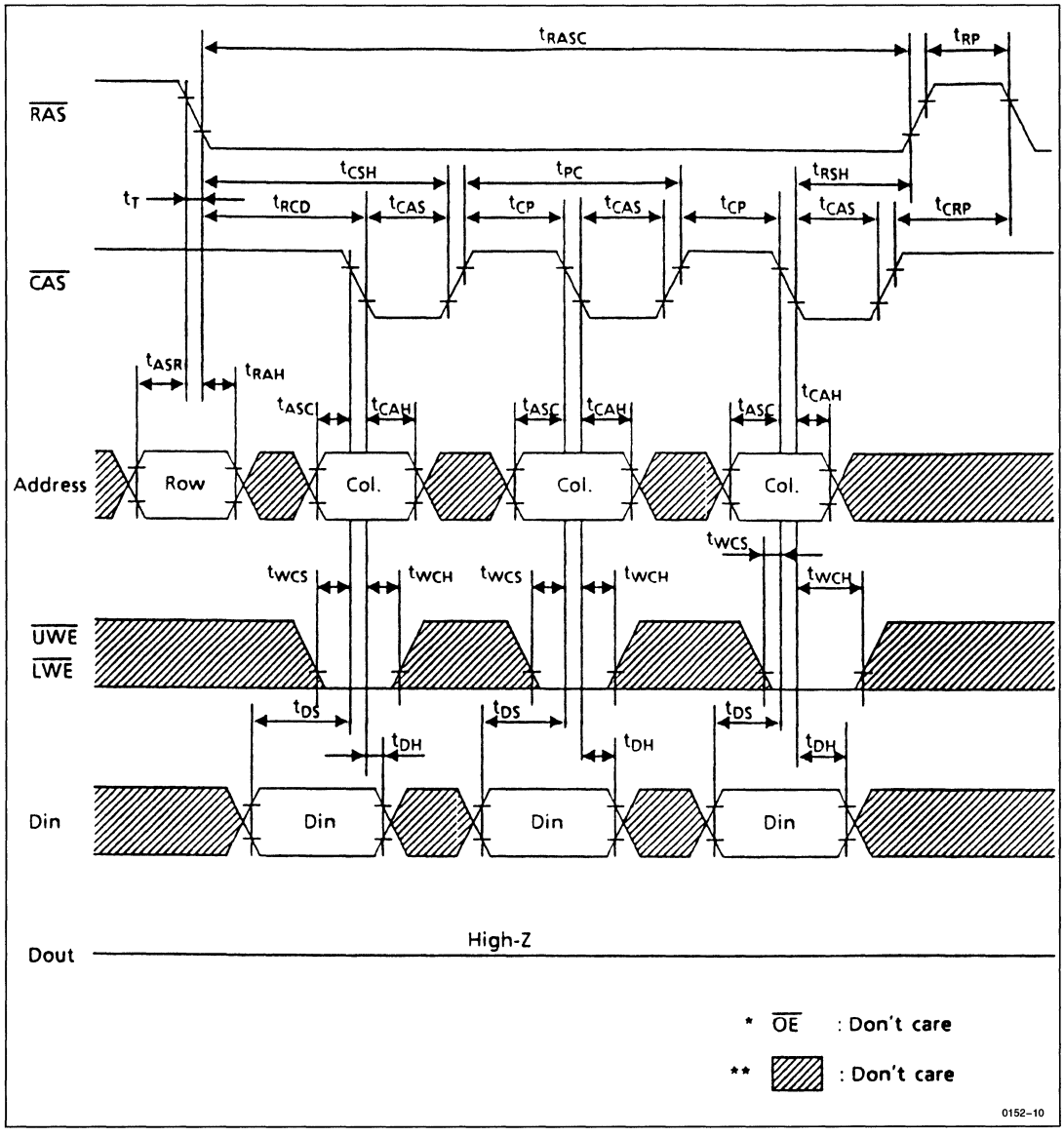
• **Hidden Refresh Cycle**



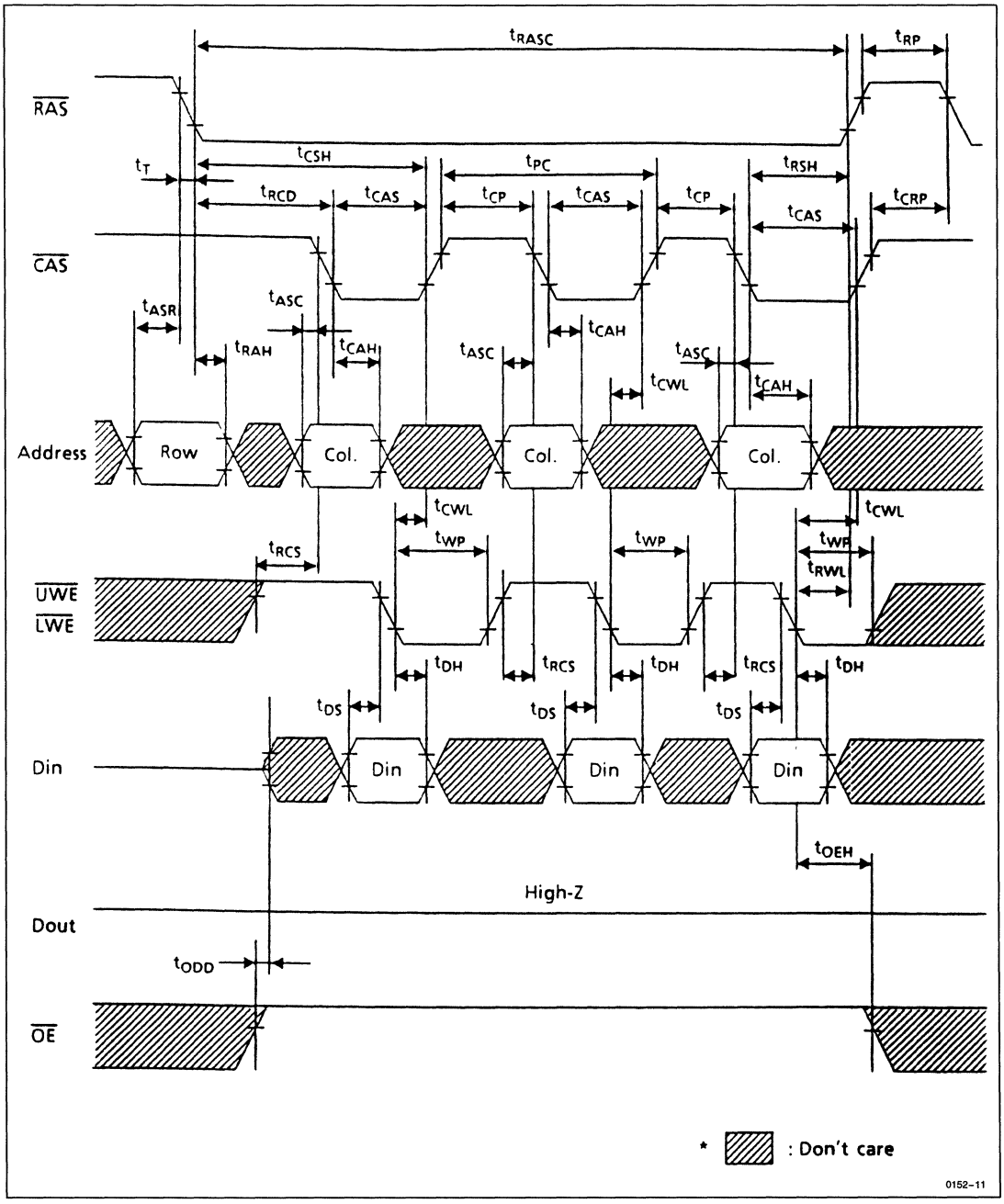
• **Fast Page Mode Read Cycle**



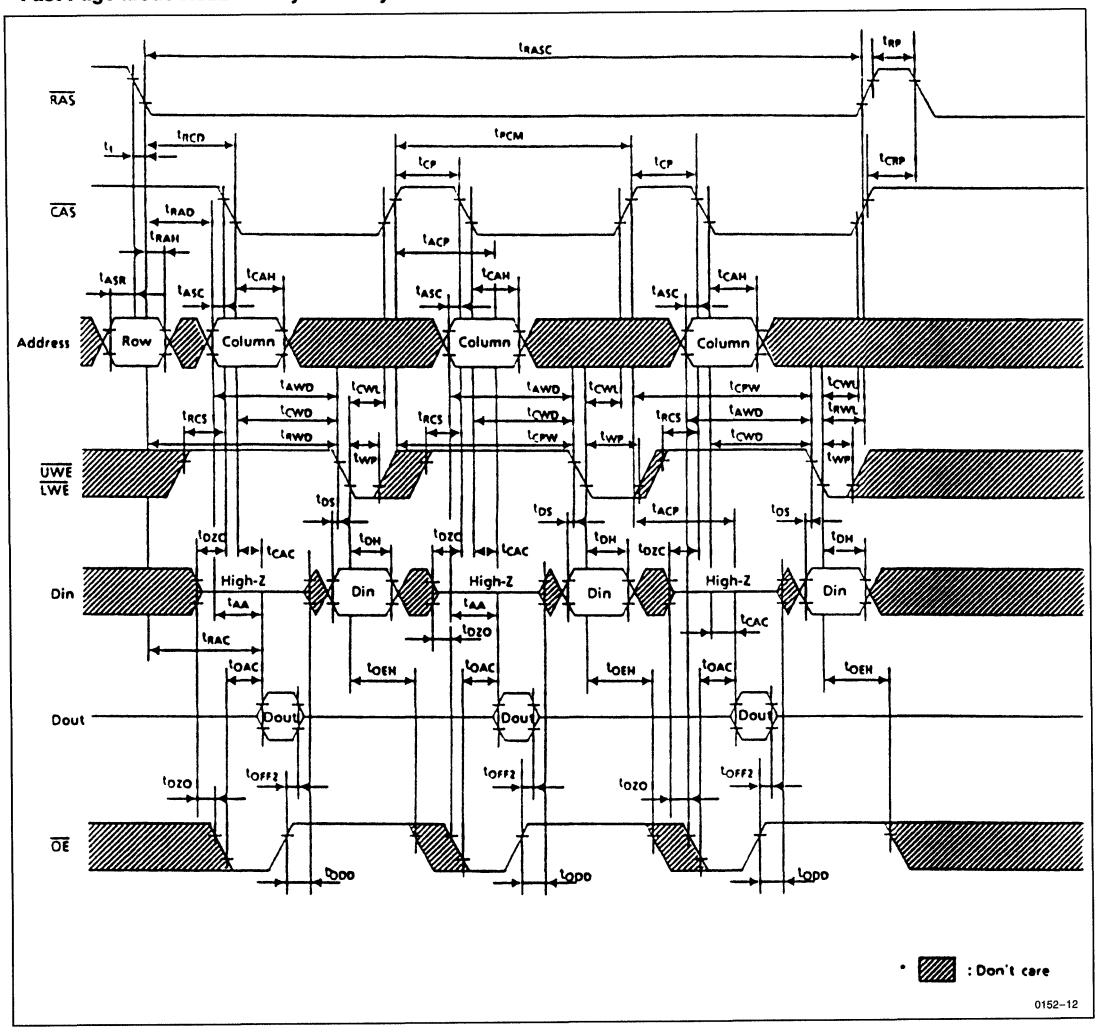
• **Fast Page Mode Early Write Cycle**



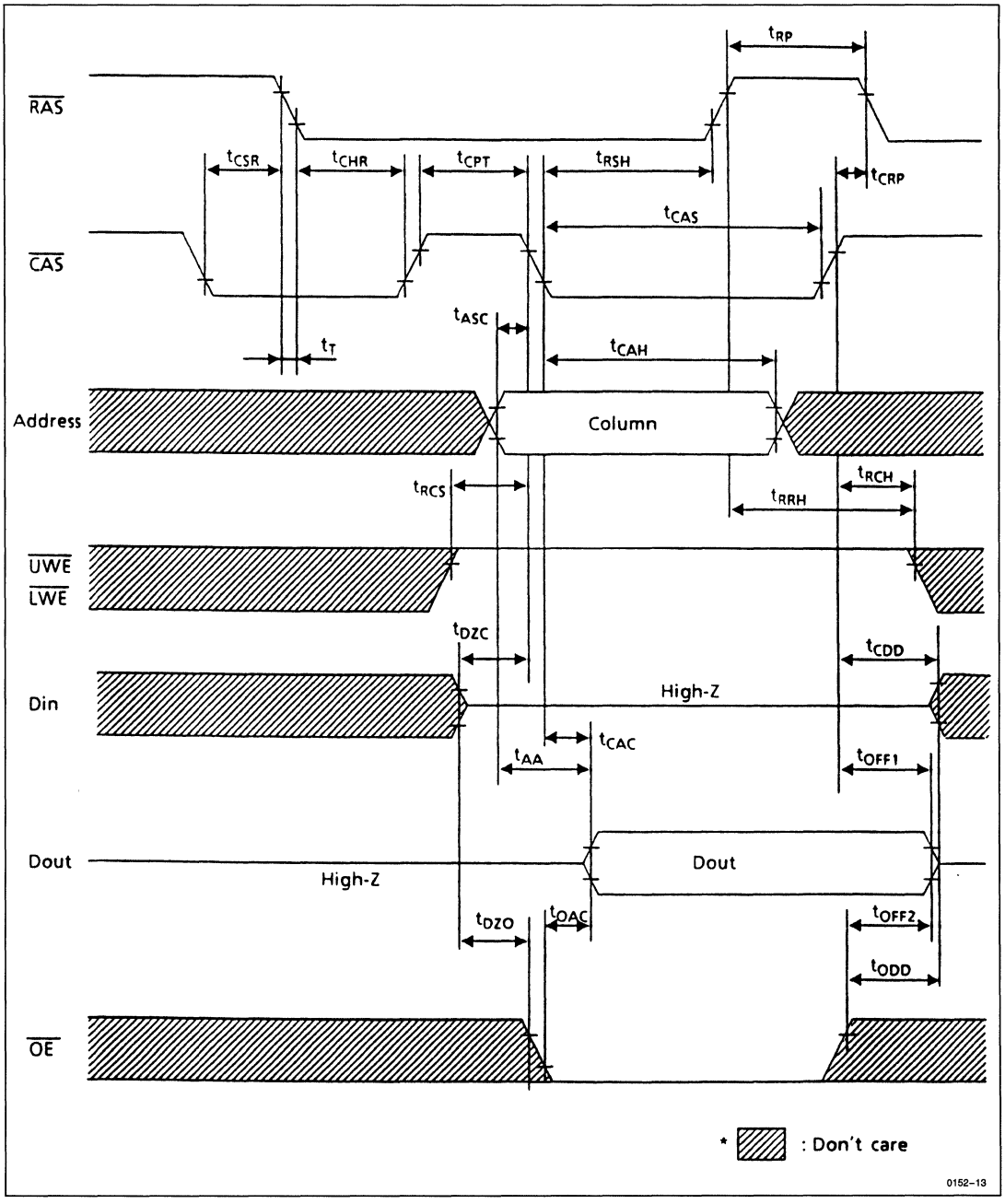
• **Fast Page Mode Delayed Write Cycle**



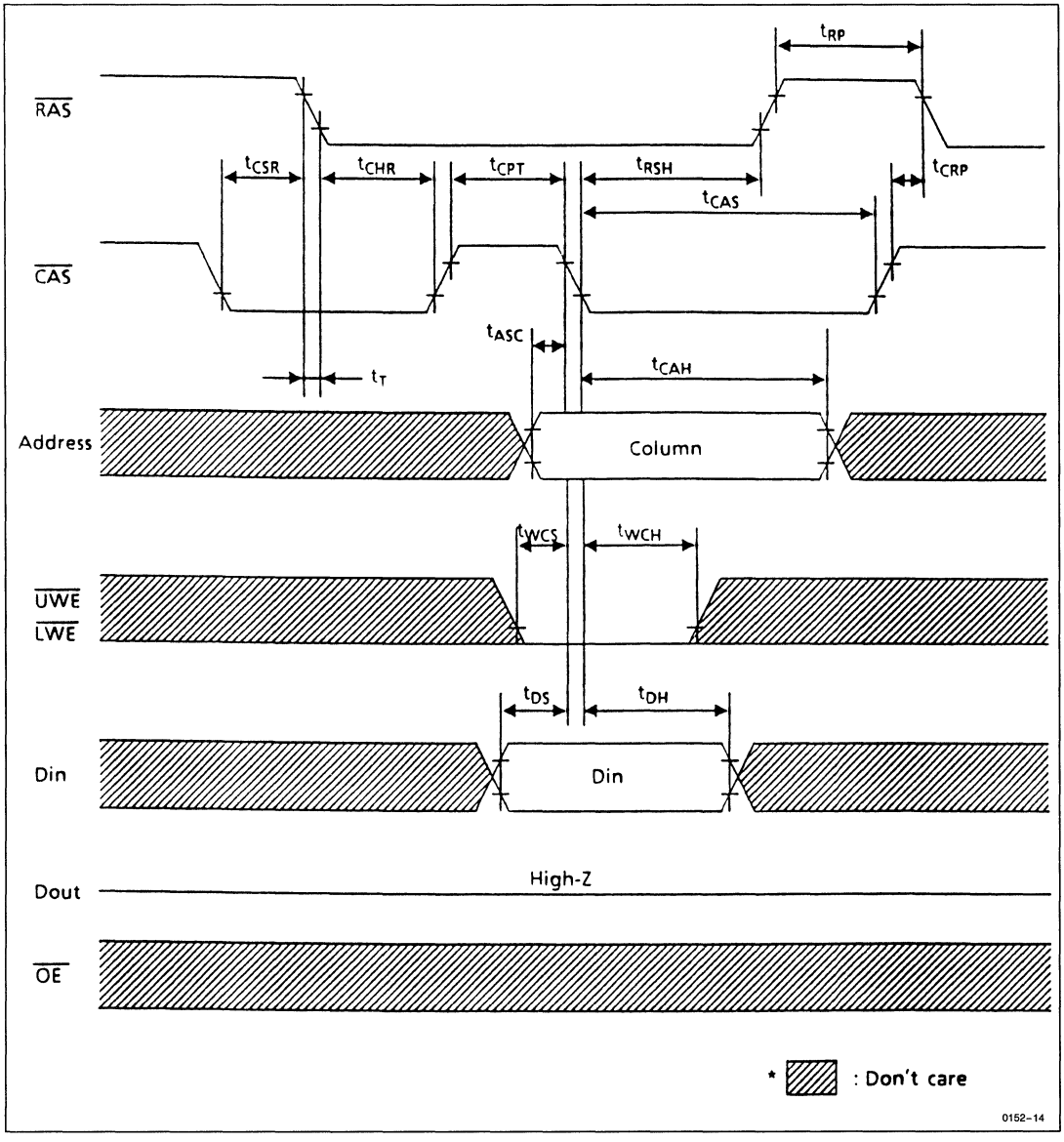
• **Fast Page Mode Read-Modify-Write Cycle**



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)



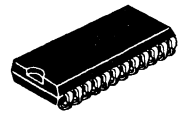
HM5116100 Series — Preliminary

16,777,216-Word x 1-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM5116100 is a CMOS dynamic RAM organized 16,777,216-word x 1-bit. It employs the most advanced CMOS technology for high performance and low power. The HM5116100 offers Fast Page Mode as a high speed access mode.

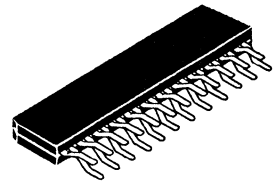
HM5116100J Series



3DCP24D

(CP-24D)

HM5116100Z Series



3DZP24

(ZP-24)

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time ..... 60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode ..... 495 mW/440 mW/385 mW/330 mW (max)
  - Standby Mode ..... 11 mW (max)
- Fast Page Mode Capability
- Long Refresh Period
- 4096 Refresh Cycles ..... (64 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh

■ ORDERING INFORMATION

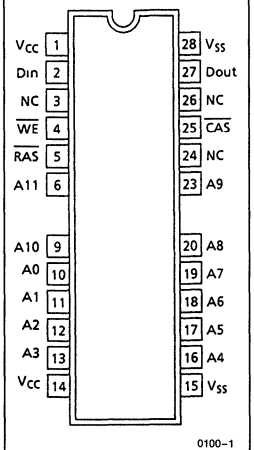
Part No.	Access Time	Package
HM5116100J-6	60 ns	400 mil 24-pin Plastic SOJ (CP-24D)
HM5116100J-7	70 ns	
HM5116100J-8	80 ns	
HM5116100J-10	100 ns	
HM5116100Z-6	60 ns	475 mil 24-pin Plastic ZIP (ZP-24)
HM5116100Z-7	70 ns	
HM5116100Z-8	80 ns	
HM5116100Z-10	100 ns	

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{11}	Address Input
A_0–A_{11}	Refresh Address Input
D_{in}	Data Input
D_{out}	Data Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	No Connection

■ PIN OUT

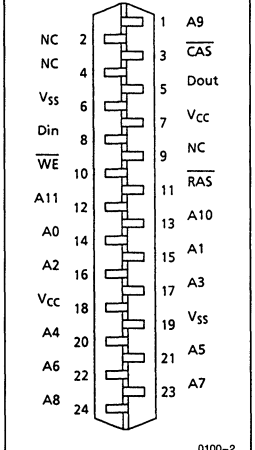
HM5116100J Series



0100-1

(Top View)

HM5116100Z Series

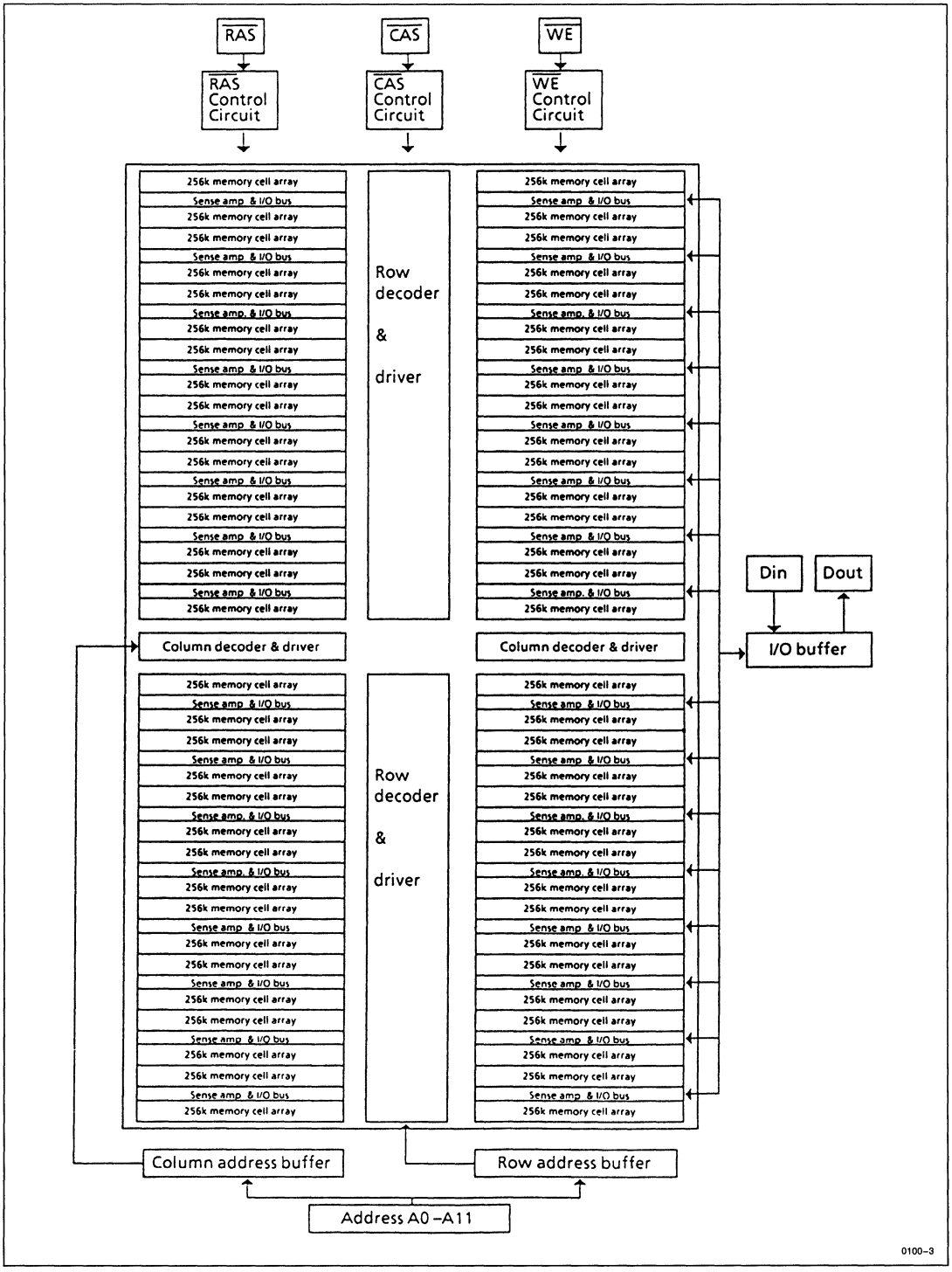


0100-2

(Bottom View)

This specification is fully compatible with the preliminary 16MB DRAM specifications from TEXAS INSTRUMENTS.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM5116100J/Z								Unit	Test Conditions	Note
		-6		-7		-8		-10				
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	70	—	60	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High Z	
		—	1	—	1	—	1	—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	90	—	80	—	70	—	60	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1, 4
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	90	—	80	—	70	—	60	mA	t_{RC} = Min	4
Fast Page Mode Current	I_{CC7}	—	70	—	60	—	50	—	45	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. Clock voltages ($\overline{RAS}$ and $\overline{CAS}$) must be applied simultaneously with or prior to applying supply voltage.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address, Data-in)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-out)	C_O	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 2, 16]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM5116100J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	70	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10000	18	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	10	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	52	20	60	20	75	ns	3
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	20	55	ns	4
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	18	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	5	—	5	—	ns	
Transition Time (Rise and Fall)	t_T	3	30	3	30	3	30	3	30	ns	5

Read Cycle

Parameter	Symbol	HM5116100J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	6, 7, 17
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	18	—	20	—	25	ns	7, 8, 17
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	ns	7, 9, 17
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	ns	10
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	5	—	5	—	5	—	5	—	ns	10
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	ns	
Column Address to $\overline{CAS}$ Lead Time	t_{CAL}	30	—	35	—	40	—	45	—	ns	
$\overline{CAS}$ to Output in Low-Z	t_{CLZ}	0	—	0	—	0	—	0	—	ns	
Output Data Hold Time	t_{OH}	3	—	3	—	3	—	3	—	ns	
Output Buffer Turn-off Time	t_{OFF}	—	15	—	18	—	20	—	25	ns	11

Write Cycle

Parameter	Symbol	HM5116100J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	12
Write Command Hold Time	t_{WCH}	15	—	15	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	18	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	18	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	13
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	15	—	ns	13

Read-Modify-Write Cycle

Parameter	Symbol	HM5116100J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	130	—	153	—	175	—	210	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	60	—	70	—	80	—	100	—	ns	12
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	15	—	18	—	20	—	25	—	ns	12
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	30	—	35	—	40	—	45	—	ns	12

Refresh Cycle

Parameter	Symbol	HM5116100J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time (CBR Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time (CBR Refresh Cycle)	t_{CHR}	20	—	20	—	20	—	20	—	ns	
$\overline{WE}$ Setup Time (CBR Refresh Cycle)	t_{WRP}	10	—	10	—	10	—	10	—	ns	
$\overline{WE}$ Hold Time (CBR Refresh Cycle)	t_{WRH}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	0	—	0	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM5116100J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASP}	—	100000	—	100000	—	100000	—	100000	ns	14
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	35	—	40	—	45	—	50	ns	15, 17
$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	t_{CPW}	35	—	40	—	45	—	50	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{CPRH}	35	—	40	—	45	—	50	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM5116100J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	60	—	68	—	75	—	85	—	ns	

Test Mode Cycle

Parameter	Symbol	HM5116100J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WTS}	10	—	10	—	10	—	10	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WTH}	10	—	10	—	10	—	10	—	ns	

Counter Test Cycle

Parameter	Symbol	HM5116100J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	TBD	—	TBD	—	TBD	—	TBD	ns		

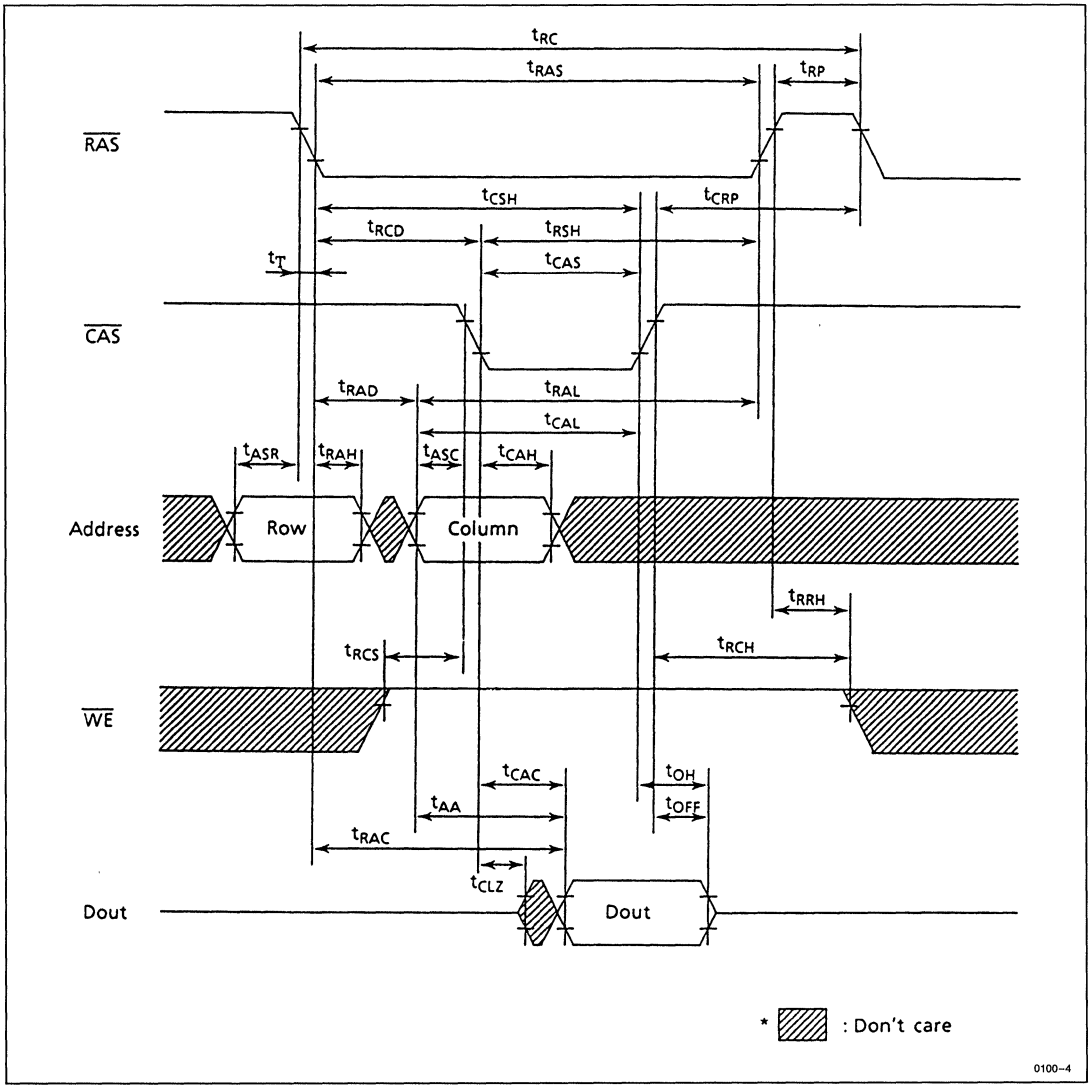
Refresh (T_J = 85°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Max	Unit	Note
Refresh Period	t_{REF}	64	ms	4096 Cycles

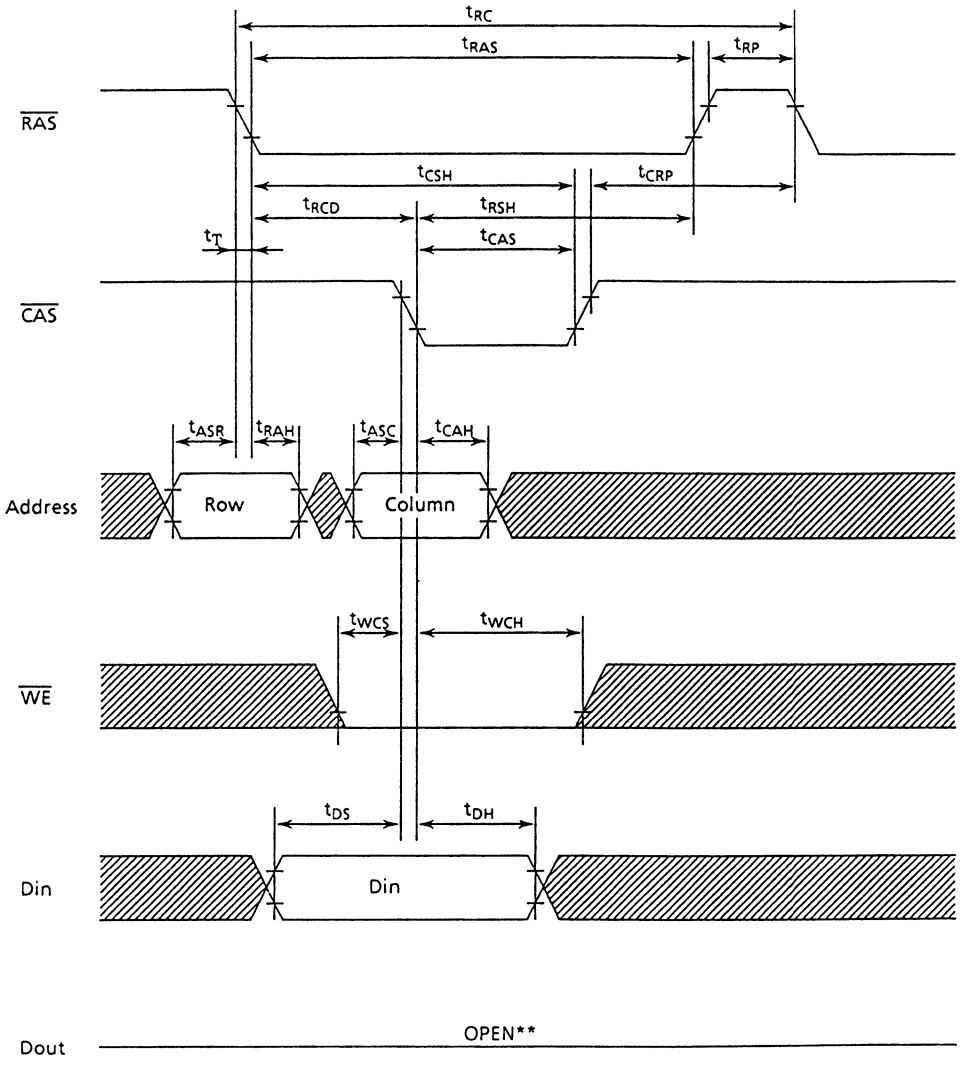
Notes:
1. AC measurements assume t_T = 5 ns.
2. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ only Refresh or $\overline{CAS}$ before $\overline{RAS}$ Refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} < t_{RCD}$ (max) and $t_{RAD} < t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to WE leading edge in delayed write or read-modify-write cycles.
14. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
15. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
16. Test mode operation specified in this data sheet is 16-bits test function controlled by compression addresses ... CA0, CA1, CA10 and CA11. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of sixteen test bits accord with each other, the state of the output data is high level. When the state of test bits do not accord with each other, the state of the output data is low level. Data output pin is D_{out} and data input in is D_{in}. If any refresh cycle has occurred, the test mode is reset.
17. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{CPA} is delayed by 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORMS

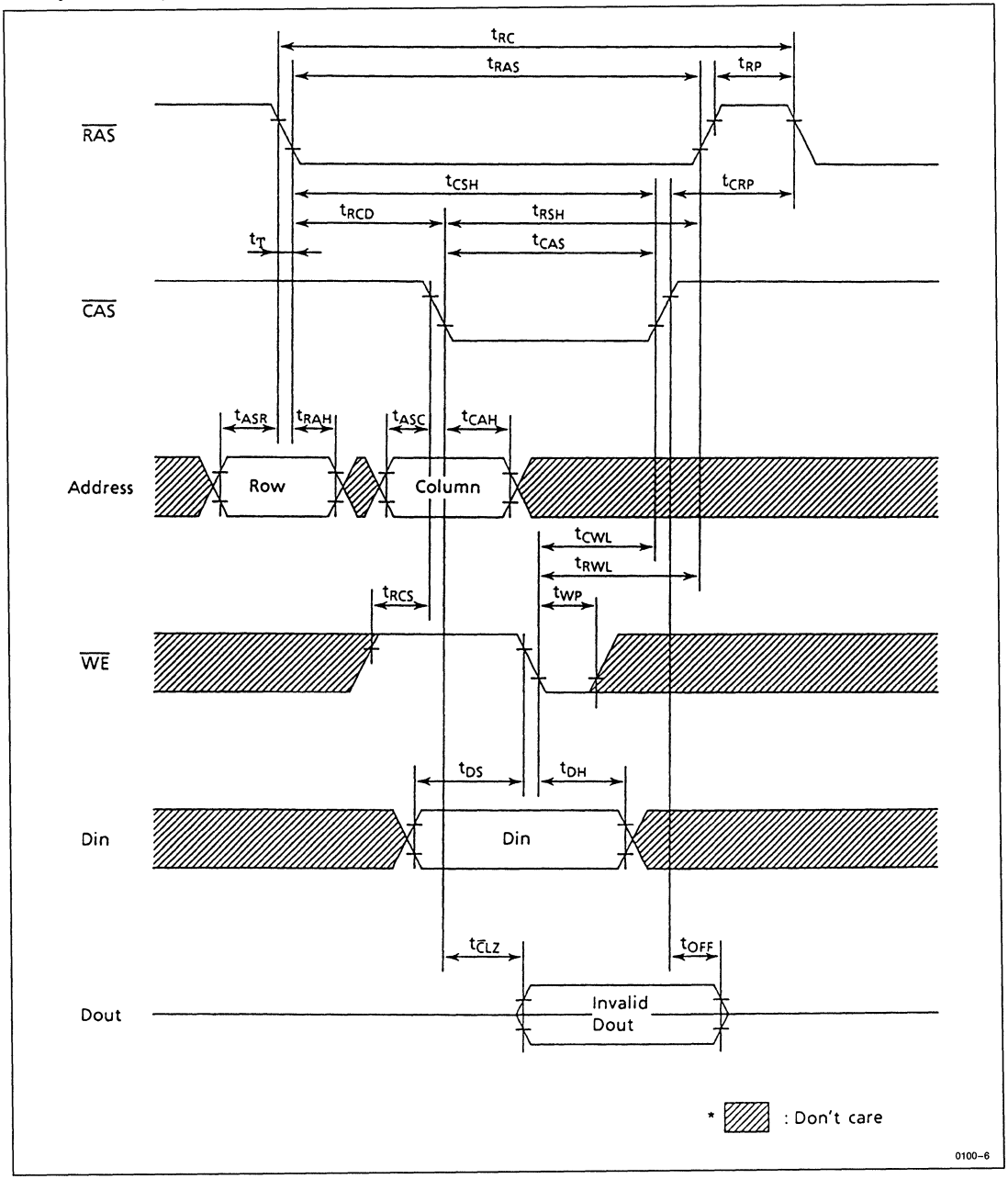
• Read Cycle



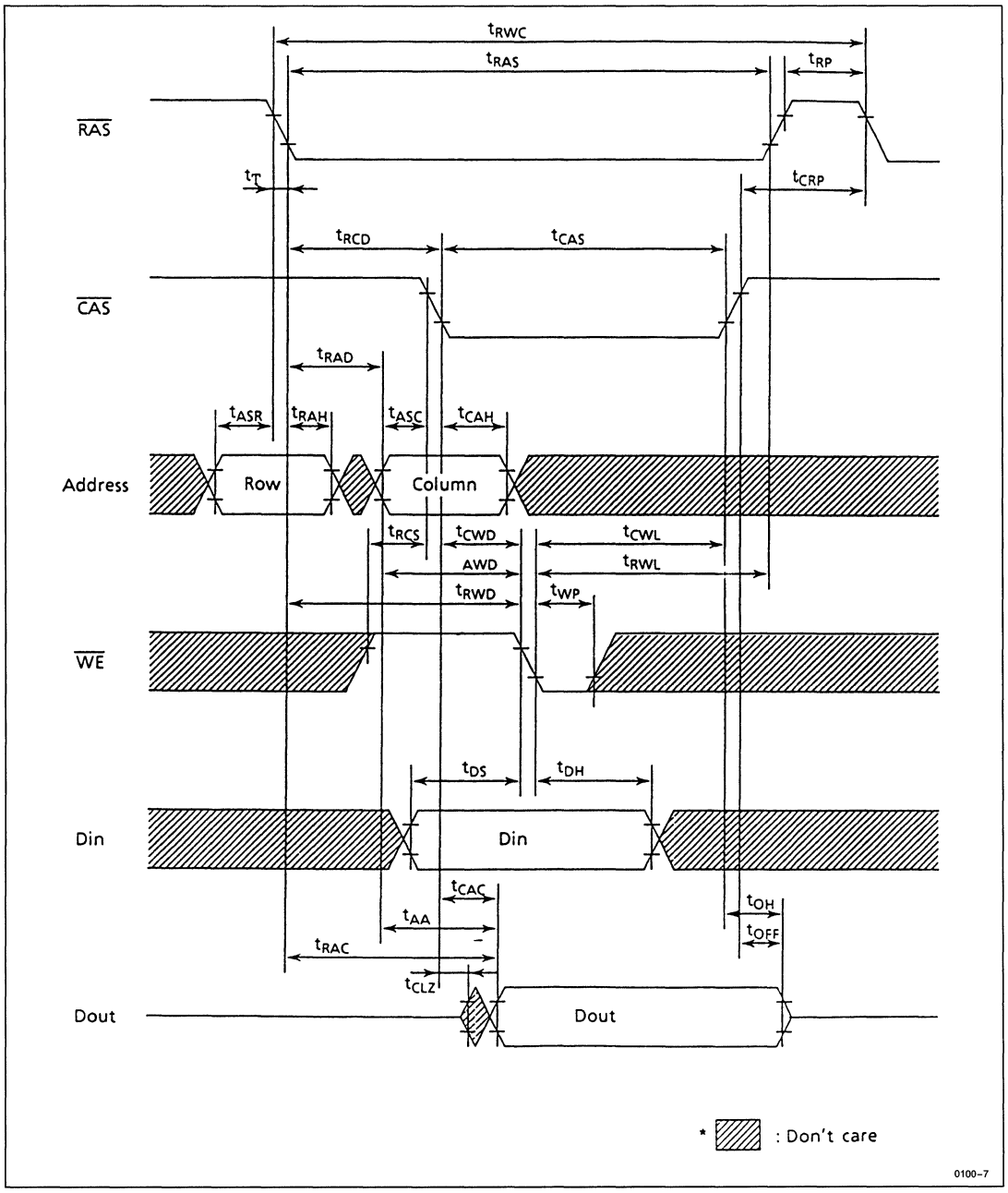
• **Early Write Cycle**



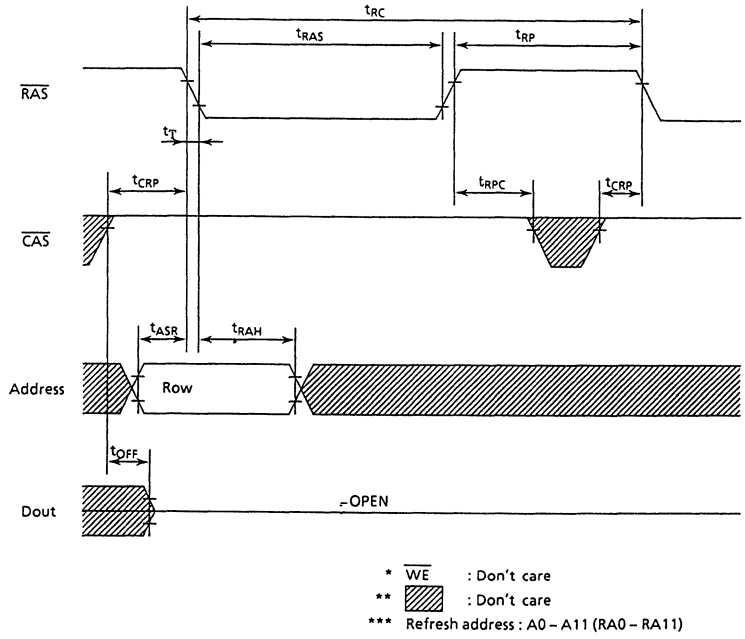
• **Delayed Write Cycle**



• **Read-Modify-Write Cycle**

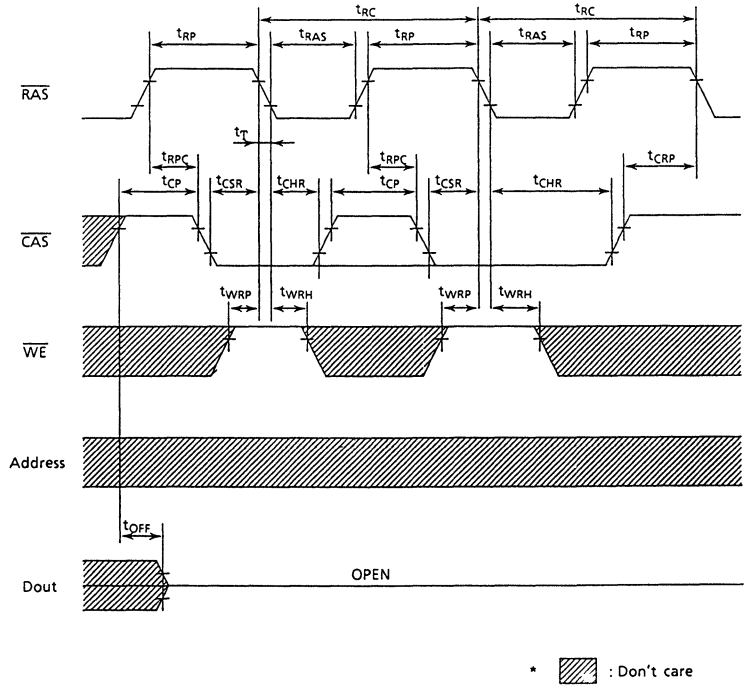


• $\overline{RAS}$ Only Refresh Cycle



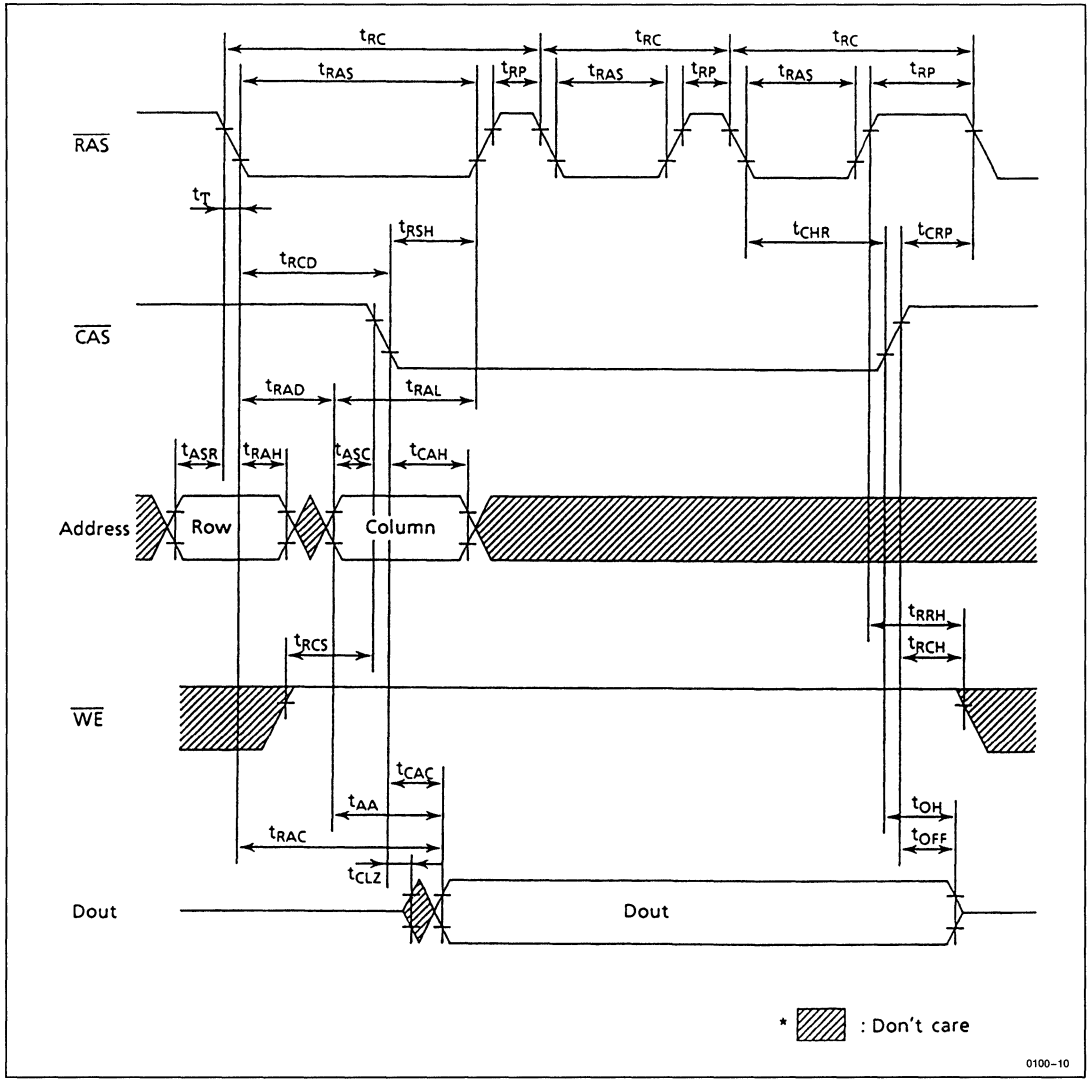
0100–8

• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

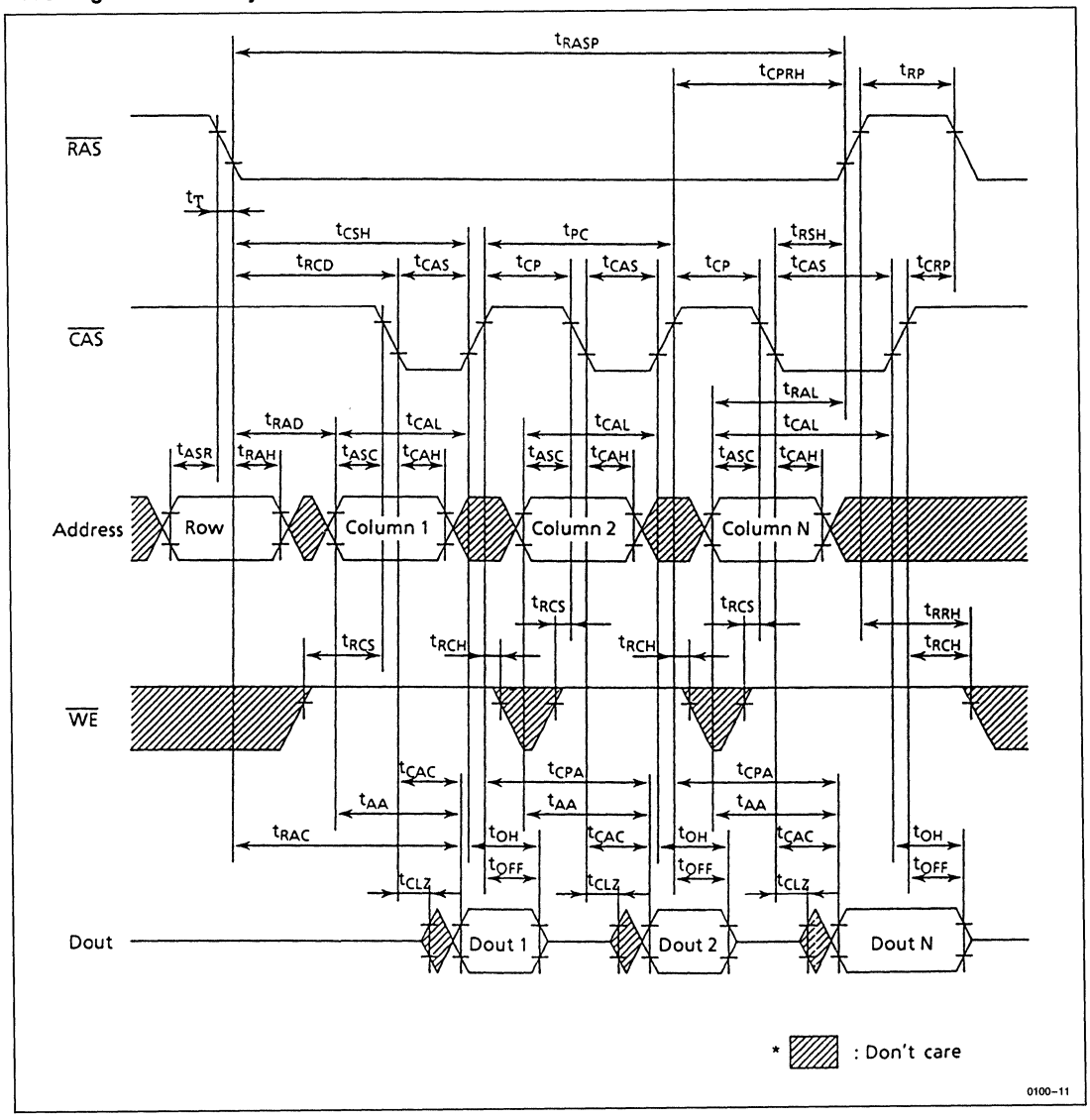


0100–9

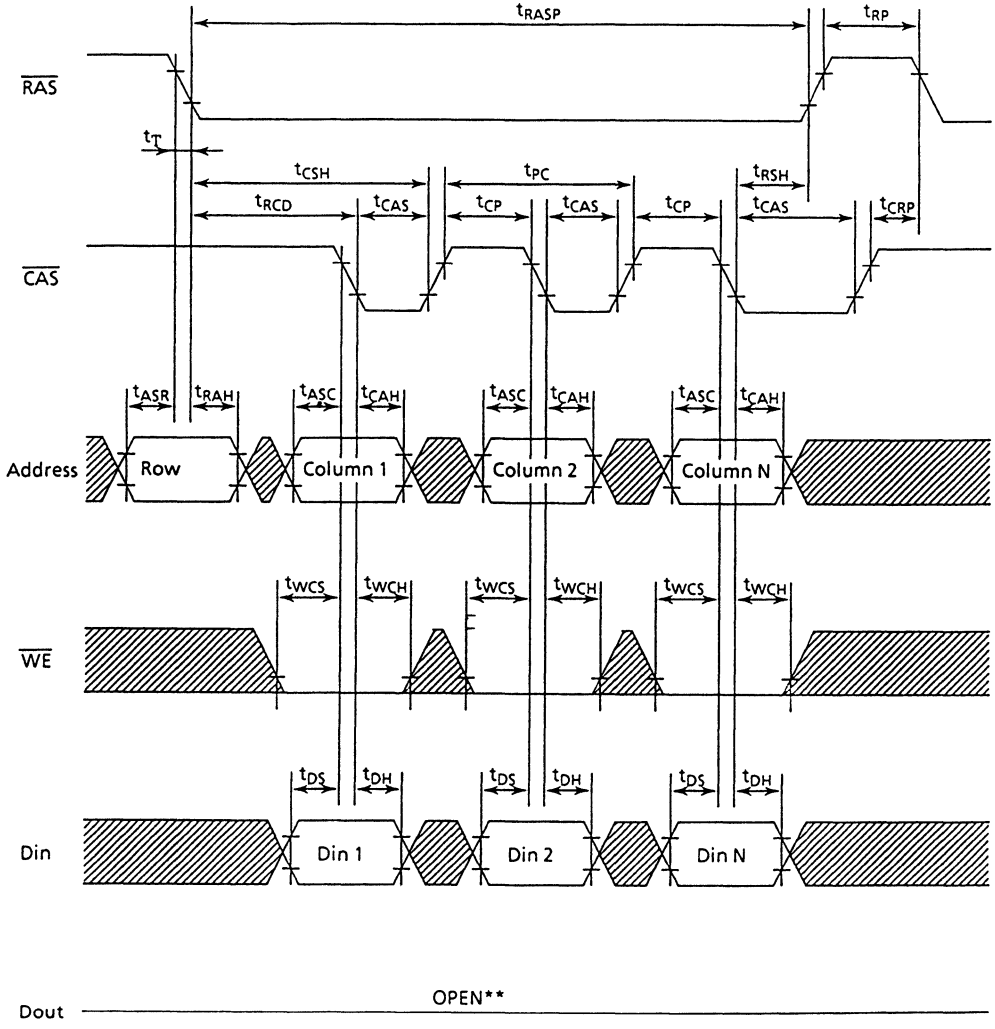
• **Hidden Refresh Cycle**



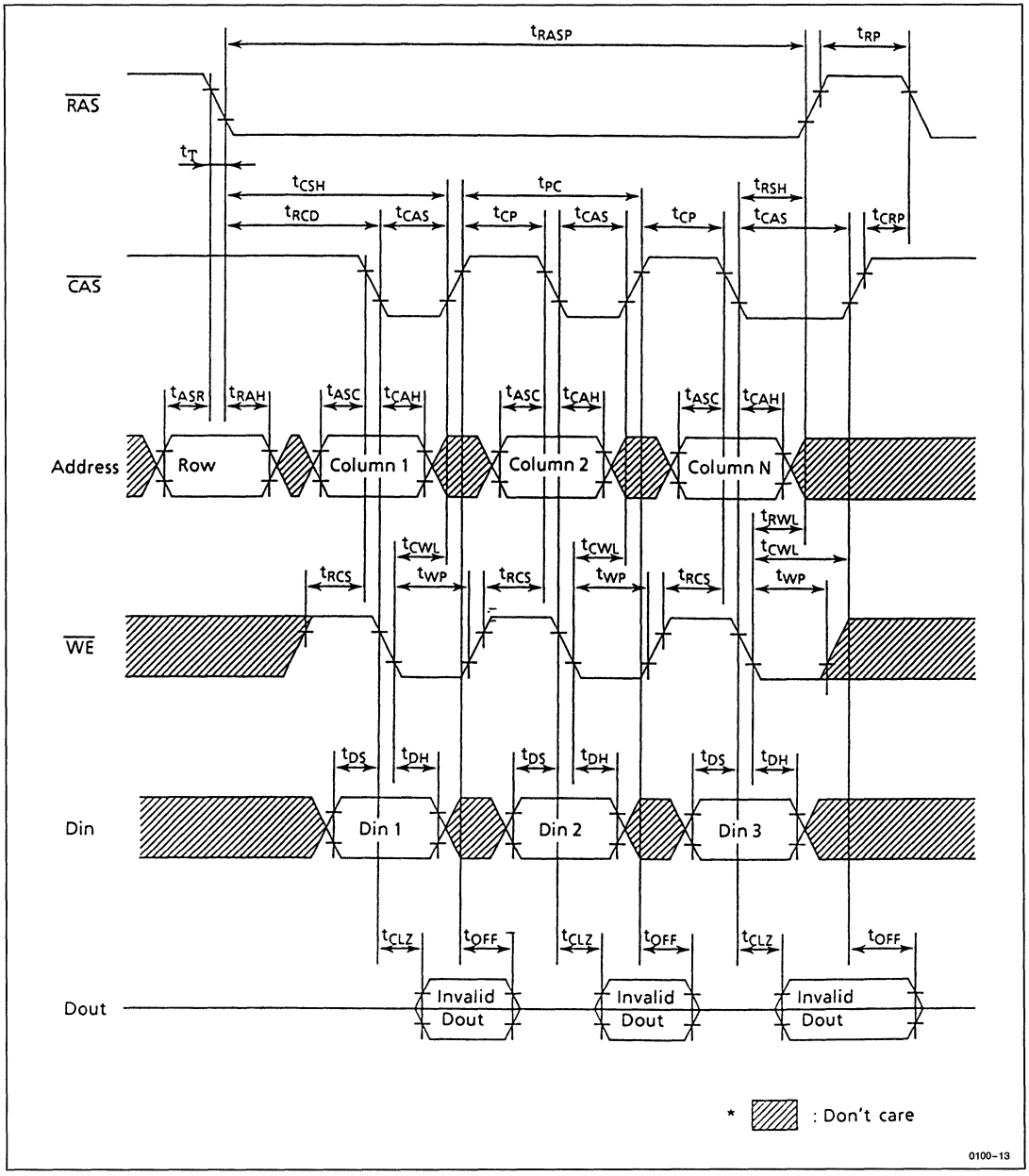
• **Fast Page Mode Read Cycle**



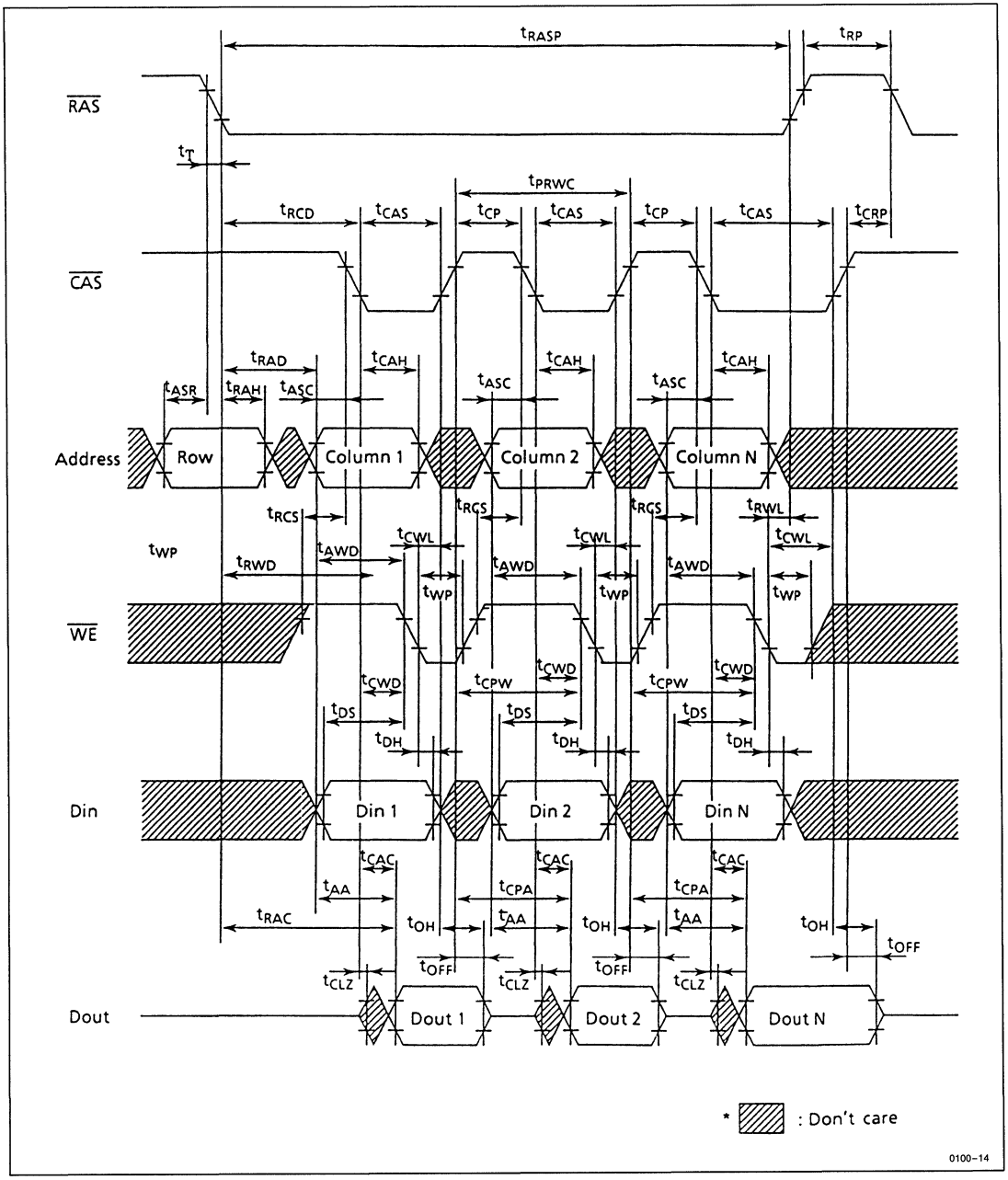
• **Fast Page Mode Early Write Cycle**



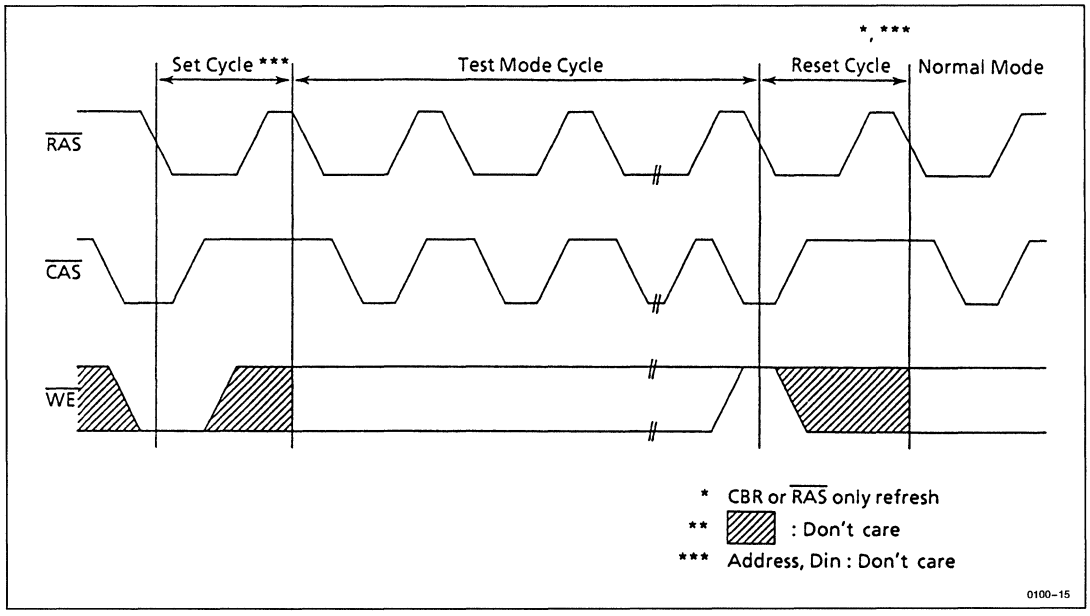
• **Fast Page Mode Delayed Write Cycle**



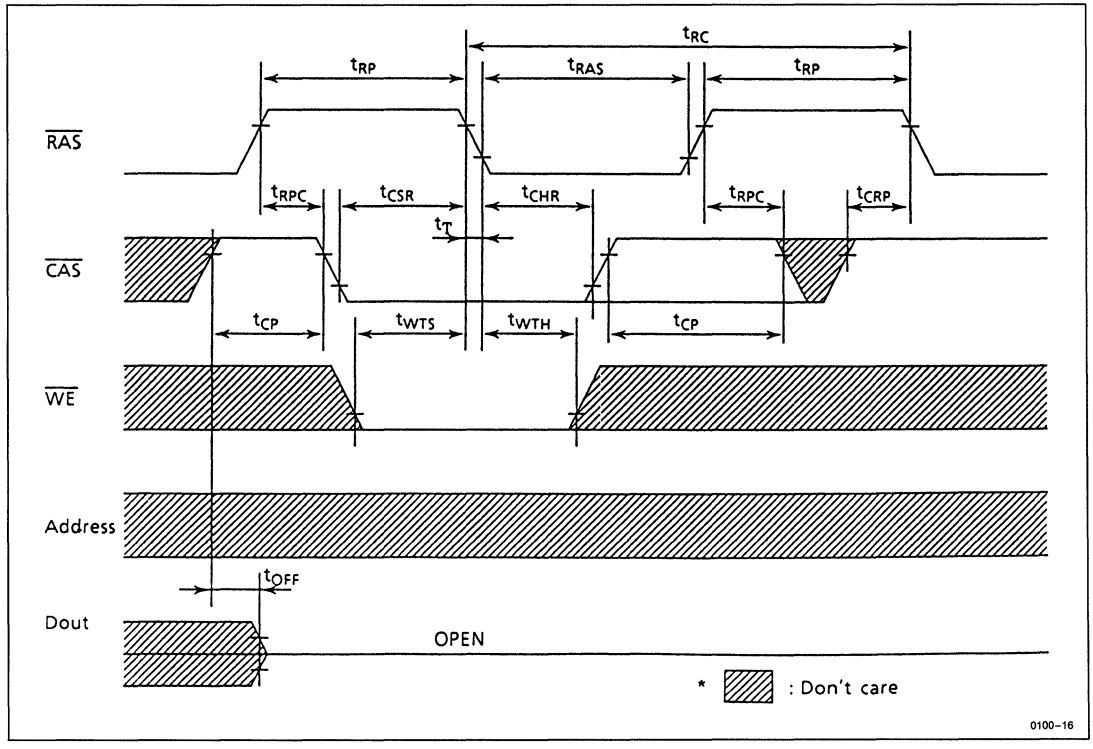
• **Fast Page Mode Read-Modify-Write Cycle**



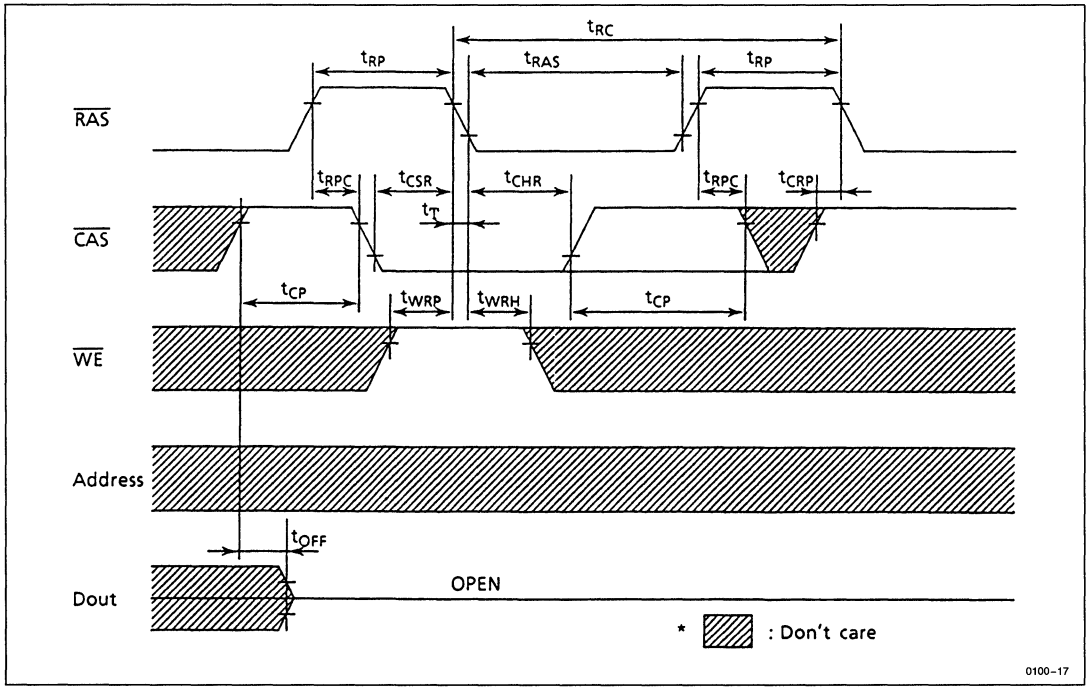
• **Test Mode Cycle**



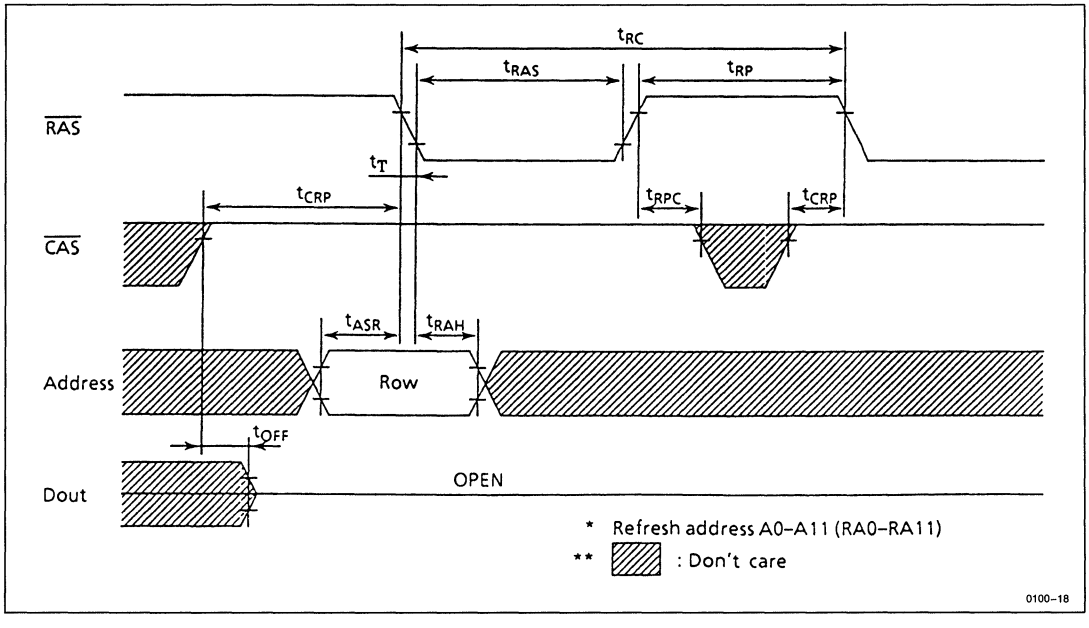
• **Test Mode Set Cycle**



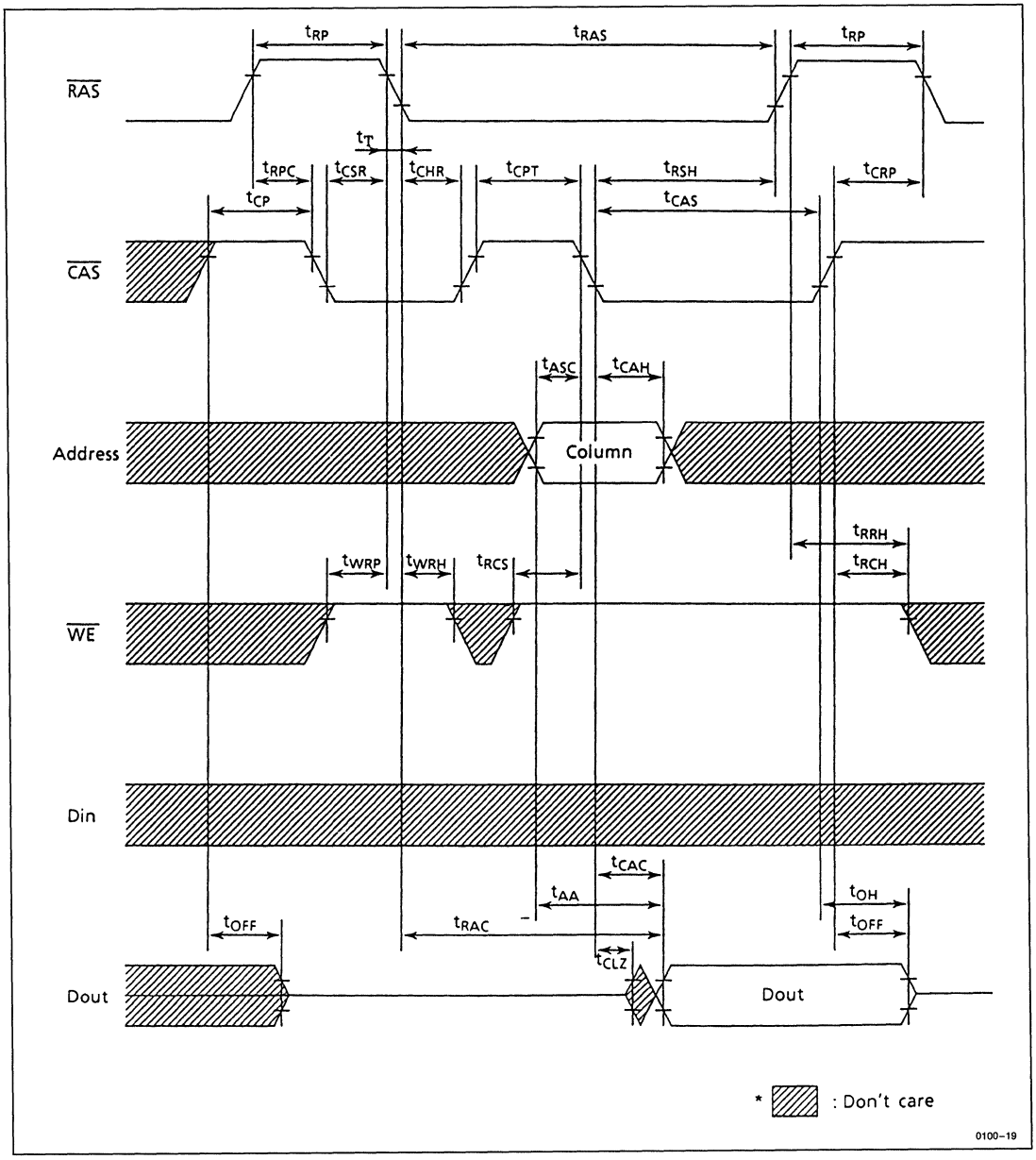
• **Test Mode Reset Cycle**
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



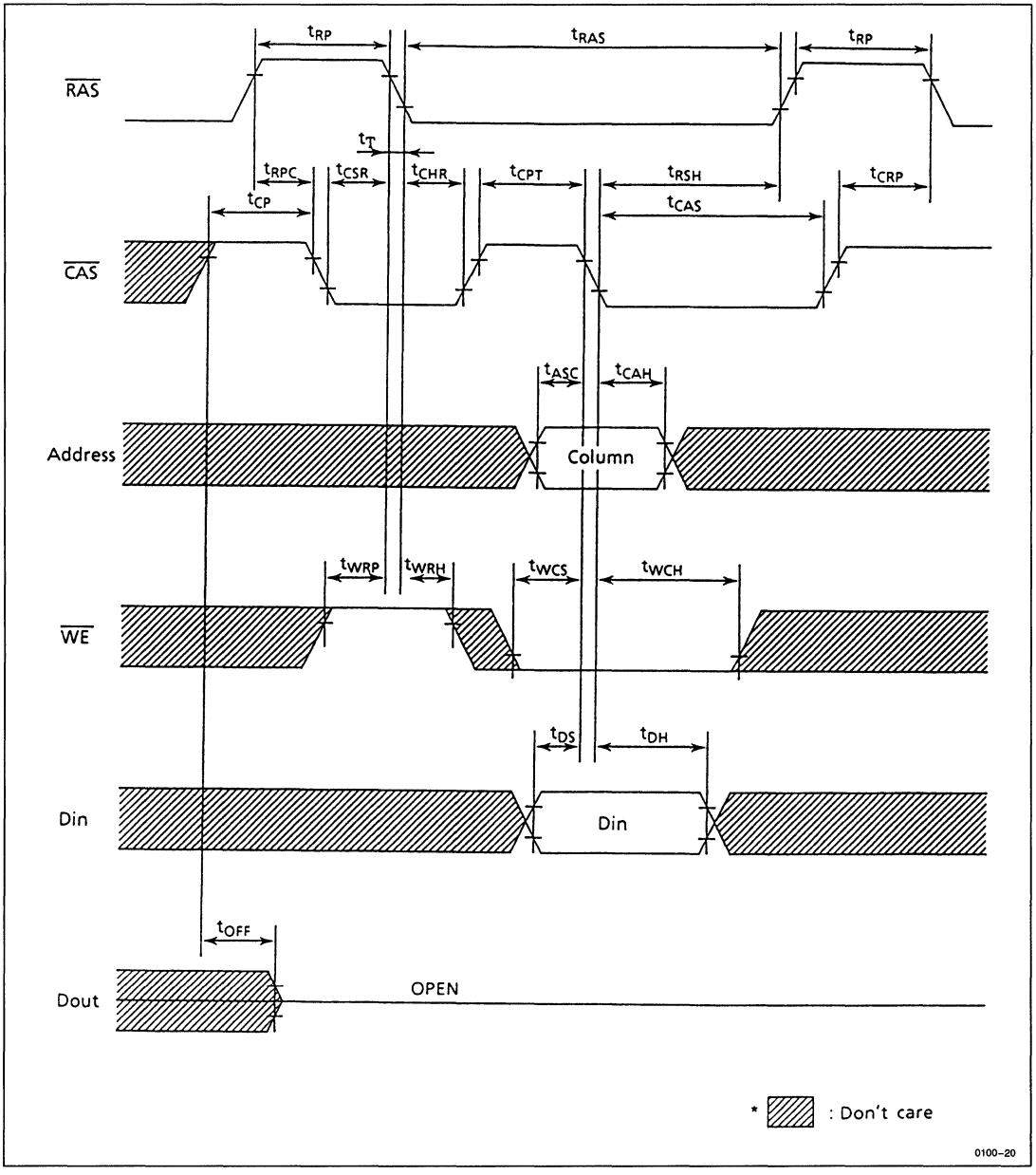
$\overline{RAS}$ Only Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)



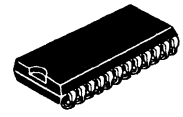
HM5116100L Series Low Power Version — Product Preview

16,777,216-Word x 1-Bit Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM5116100 is a CMOS dynamic RAM organized 16,777,216 words x 1-bit. It employs the most advanced CMOS technology for high performance and low power. The HM5116100 offers Fast Page Mode as a high speed access mode.

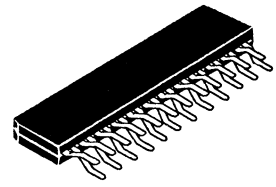
HM5116100LJ Series



3DCP24D

(CP-24D)

HM5116100LZ Series



3DZP24

(ZP-24)

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time ..... 60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode ..... 495 mW/440 mW/385 mW/330 mW (max)
  - Standby Mode ..... 11 mW (max)
- Fast Page Mode Capability
- Long Refresh Period
  - 4096 Refresh Cycles ..... (256 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Battery Back Up Operation

■ ORDERING INFORMATION

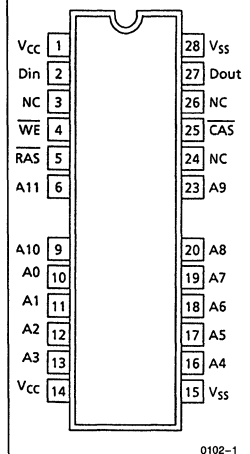
Part No.	Access Time	Package
HM5116100LJ-6	60 ns	400 mil 24-pin Plastic SOJ (CP-24D)
HM5116100LJ-7	70 ns	
HM5116100LJ-8	80 ns	
HM5116100LJ-10	100 ns	
HM5116100LZ-6	60 ns	475 mil 24-pin Plastic ZIP (ZP-24)
HM5116100LZ-7	70 ns	
HM5116100LZ-8	80 ns	
HM5116100LZ-10	100 ns	

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{11}	Address Input
A_0–A_{11}	Refresh Address Input
D_{in}	Data Input
D_{out}	Data Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power Supply (+ 5V)
V_{SS}	Ground
NC	No Connection

■ PIN OUT

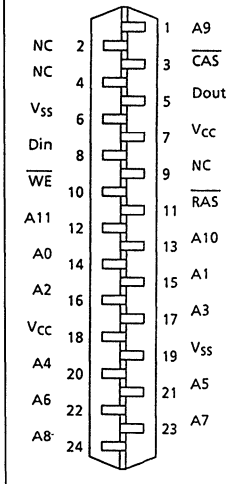
HM5116100LJ Series



0102-1

(Top View)

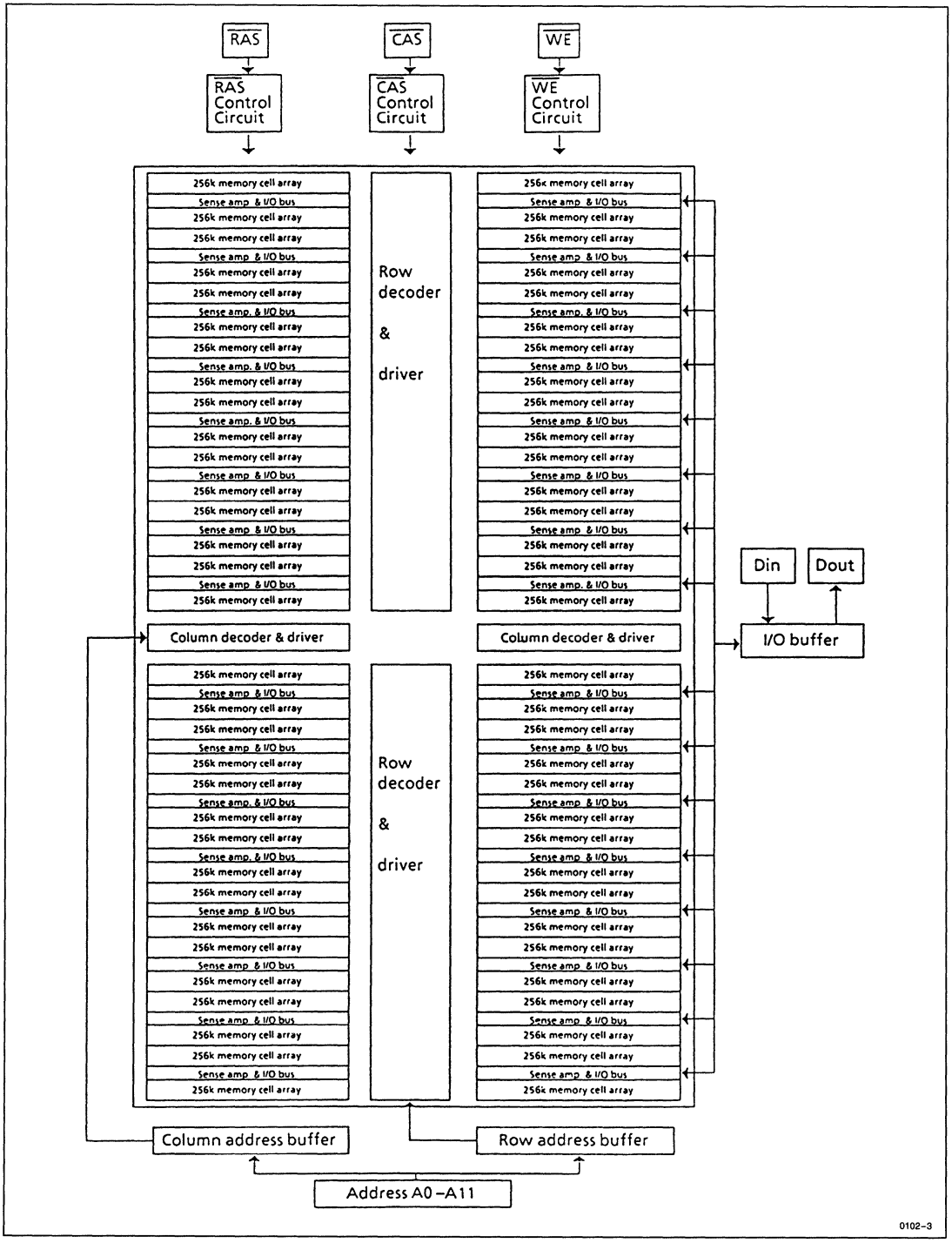
HM5116100LZ Series



0102-2

(Bottom View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Disspation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HM5116100-6		HM5116100-7		HM5116100-8		HM5116100-10		Unit	Test Condition	Note
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	70	—	60	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	300	—	300	—	300	—	300	μA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ > V_{CC} − 0.2V, or ≤ 6.5V Address and D_{in} = Stable D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	90	—	80	—	70	—	60	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1, 4
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	90	—	80	—	70	—	60	mA	t_{RC} = Min	4
Fast Page Mode Current	I_{CC7}	—	70	—	60	—	50	—	45	mA	t_{PC} = Min	1, 3
Battery Back-up Operating Current (Standby with CBR Refresh)	I_{CC10}	—	500	—	500	—	500	—	500	μA	Standby: CMOS Interface CBR Refresh: t_{RC} = 62.5 μs t_{RAS} ≤ 1 μs Address and D_{in} = Stable D_{out} = High-Z	5
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	

• **DC Electrical Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V) (continued)

Parameter	Symbol	HM5116100-6		HM5116100-7		HM5116100-8		HM5116100-10		Unit	Test Condition	Note
		Min	Max	Min	Max	Min	Max	Min	Max			
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. Clock voltages ($\overline{RAS}$ and $\overline{CAS}$) must be applied simultaneously with or prior to applying supply voltage.
5. V_{CC} − 0.2V ≤ V_{IH} ≤ 6.5V, 0V ≤ V_{IL} ≤ 0.2V.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address, Data-in)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-out)	C_O	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to 70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 2, 16]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM5116100-6		HM5116100-7		HM5116100-8		HM5116100-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Max	Max		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	70	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10000	18	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	10	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	52	20	60	20	75	ns	3
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	15	55	ns	4
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	18	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	5	—	5	—	ns	
Transition Time (Rise and Fall)	t_T	3	30	3	30	3	30	3	30	ns	5

Read Cycle

Parameter	Symbol	HM5116100-6		HM5116100-7		HM5116100-8		HM5116100-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	6, 7, 17
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	18	—	20	—	25	ns	7, 8, 17
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	ns	7, 9, 17
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	ns	10
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	5	—	5	—	5	—	5	—	ns	10

Read Cycle (continued)

Parameter	Symbol	HM5116100-6		HM5116100-7		HM5116100-8		HM5116100-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	ns	
Column Address to $\overline{CAS}$ Lead Time	t_{CAL}	30	—	35	—	40	—	45	—	ns	
$\overline{CAS}$ to Output in Low-Z	t_{CLZ}	0	—	0	—	0	—	0	—	ns	
Output Data Hold Time	t_{OH}	3	—	3	—	3	—	3	—	ns	
Output Buffer Turn-off Time	t_{OFF}	—	15	—	18	—	20	—	25	ns	11

Write Cycle

Parameter	Symbol	HM5116100-6		HM5116100-7		HM5116100-8		HM5116100-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	12
Write Command Hold Time	t_{WCH}	15	—	15	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	18	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	18	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	13
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	15	—	ns	13

Read-Modify-Write Cycle

Parameter	Symbol	HM5116100-6		HM5116100-7		HM5116100-8		HM5116100-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	130	—	153	—	175	—	210	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	60	—	70	—	80	—	100	—	ns	12
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	15	—	18	—	20	—	25	—	ns	12
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	30	—	35	—	40	—	45	—	ns	12

Refresh Cycle

Parameter	Symbol	HM5116100-6		HM5116100-7		HM5116100-8		HM5116100-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time (CBR Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time (CBR Refresh Cycle)	t_{CHR}	20	—	20	—	20	—	20	—	ns	
$\overline{WE}$ Setup Time (CBR Refresh Cycle)	t_{WRP}	10	—	10	—	10	—	10	—	ns	
$\overline{WE}$ Hold Time (CBR Refresh Cycle)	t_{WRH}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	0	—	0	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM5116100-6		HM5116100-7		HM5116100-8		HM5116100-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASP}	—	100000	—	100000	—	100000	—	100000	ns	14
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	35	—	40	—	45	—	50	ns	15, 17
$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	t_{CPW}	35	—	40	—	45	—	50	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{CPRH}	35	—	40	—	45	—	50	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM5116100-6		HM5116100-7		HM5116100-8		HM5116100-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	60	—	68	—	75	—	85	—	ns	

Test Mode Cycle

Parameter	Symbol	HM5116100-6		HM5116100-7		HM5116100-8		HM5116100-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WTS}	10	—	10	—	10	—	10	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WTH}	10	—	10	—	10	—	10	—	ns	

Counter Test Cycle

Parameter	Symbol	HM5116100-6		HM5116100-7		HM5116100-8		HM5116100-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	TBD	—	TBD	—	TBD	—	TBD	—	ns	

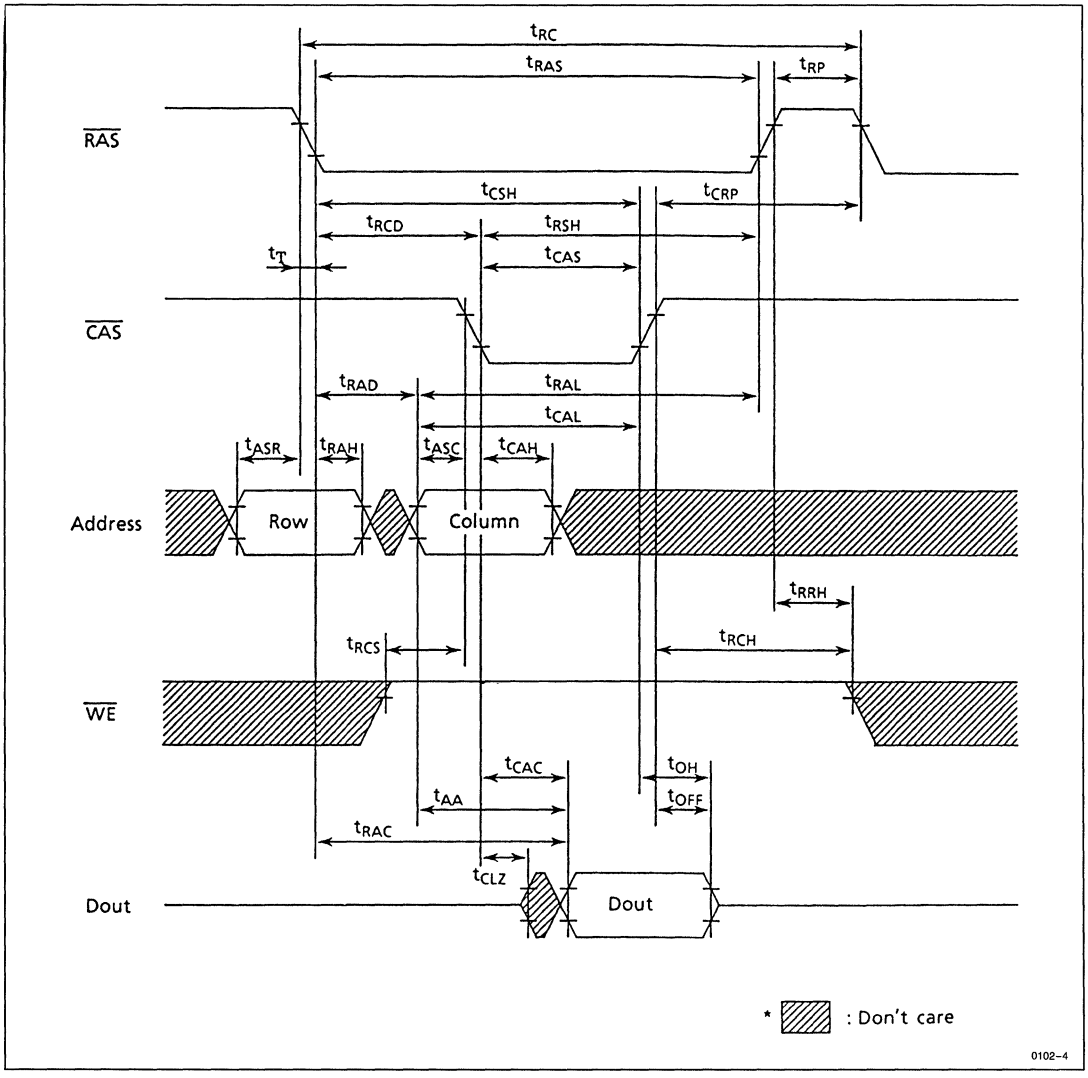
Refresh (T_J = 85°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Max	Unit	Note
Refresh Period	t_{REF}	256	ms	4096 Cycles

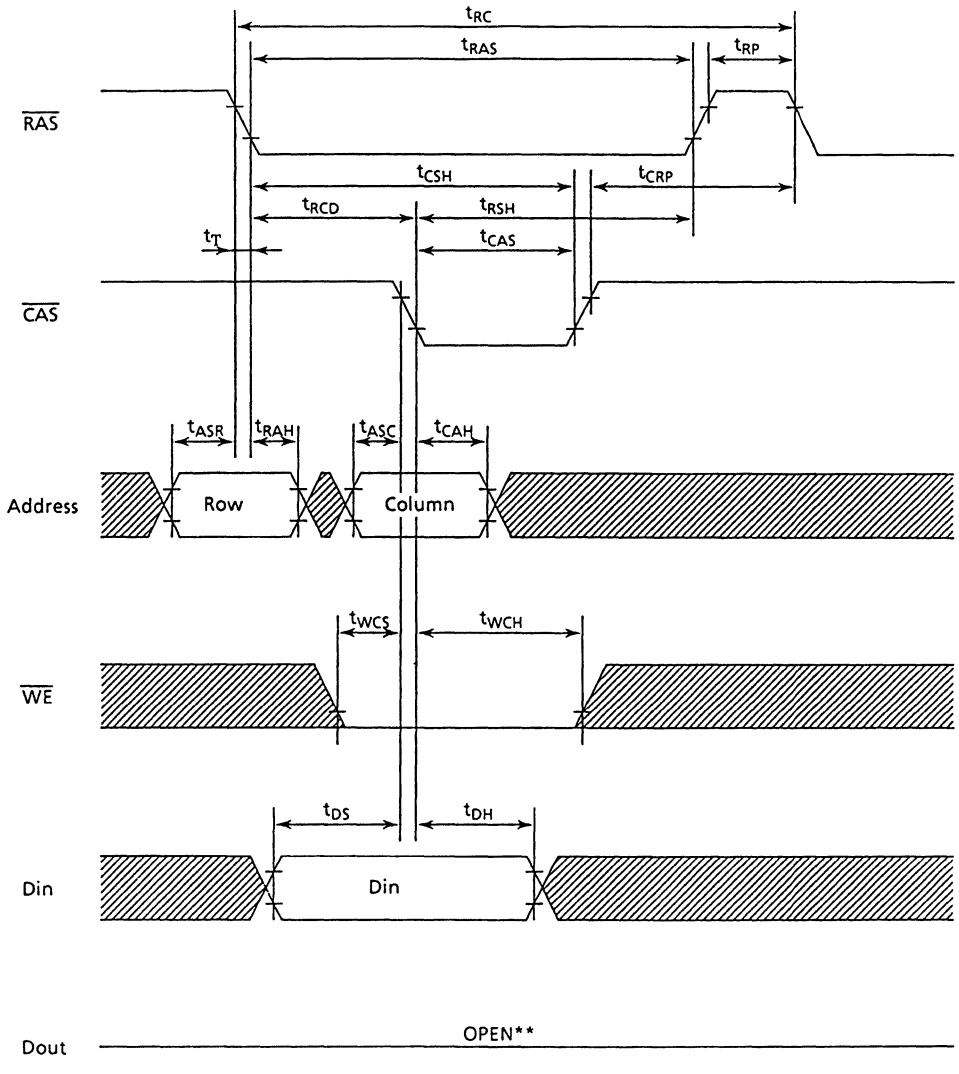
Notes:
1. AC measurements assume t_T = 5 ns.
2. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} < t_{RCD}$ (max) and $t_{RAD} < t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
14. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
15. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
16. Test mode operation specified in this data sheet is 16 bits test function controlled by compression addresses — CA0, CA1, CA10 and CA11. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of sixteen test bits accord with each other, the state of the output data is high level. When the state of test bits do not accord with each other, the state of the output data is low level. Data output pin is D_{out} and data input pin is D_{in}. If any refresh cycle is occurred, the test mode is reset.
17. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{CPA} is delayed by 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORMS

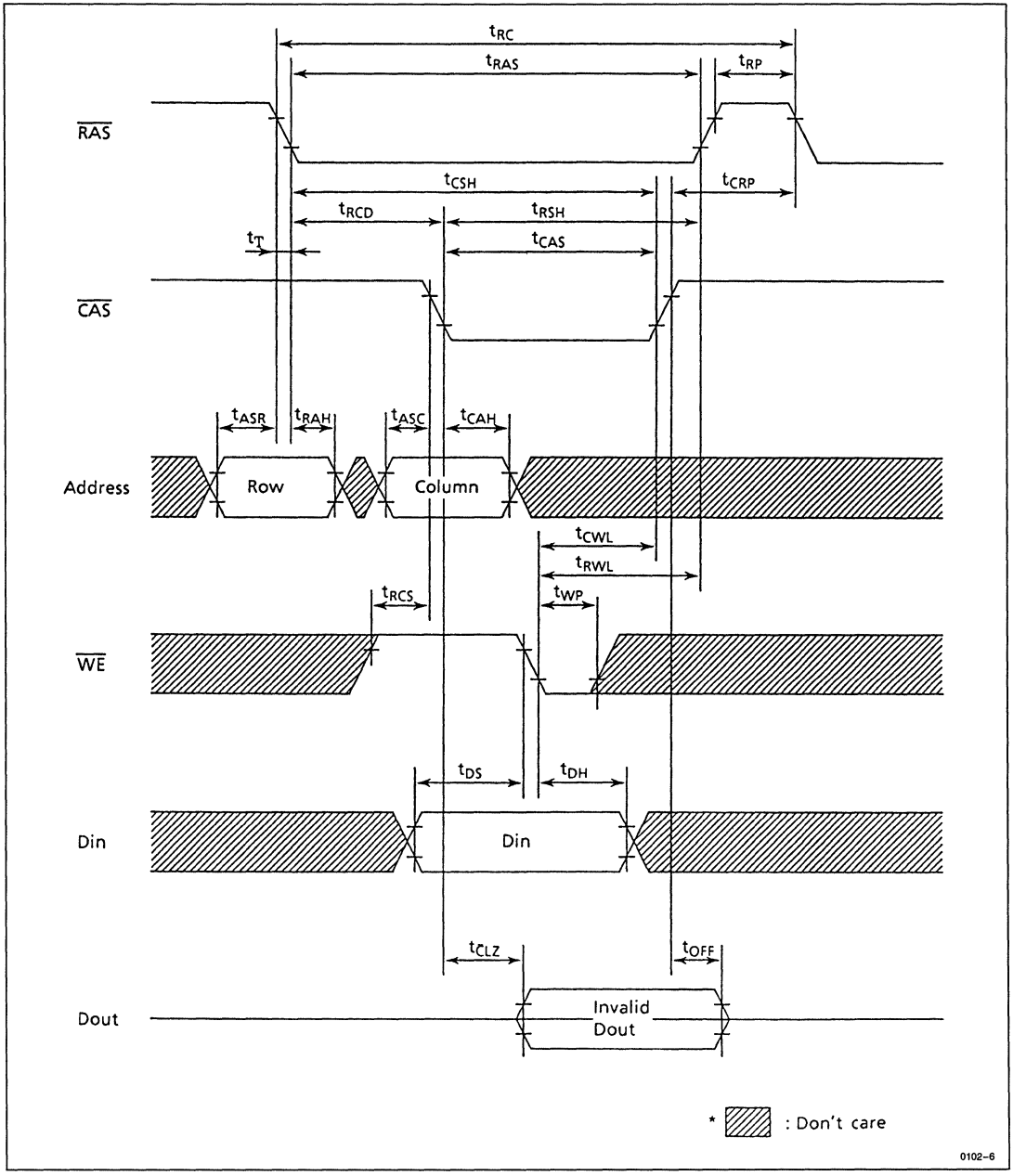
• Read Cycle



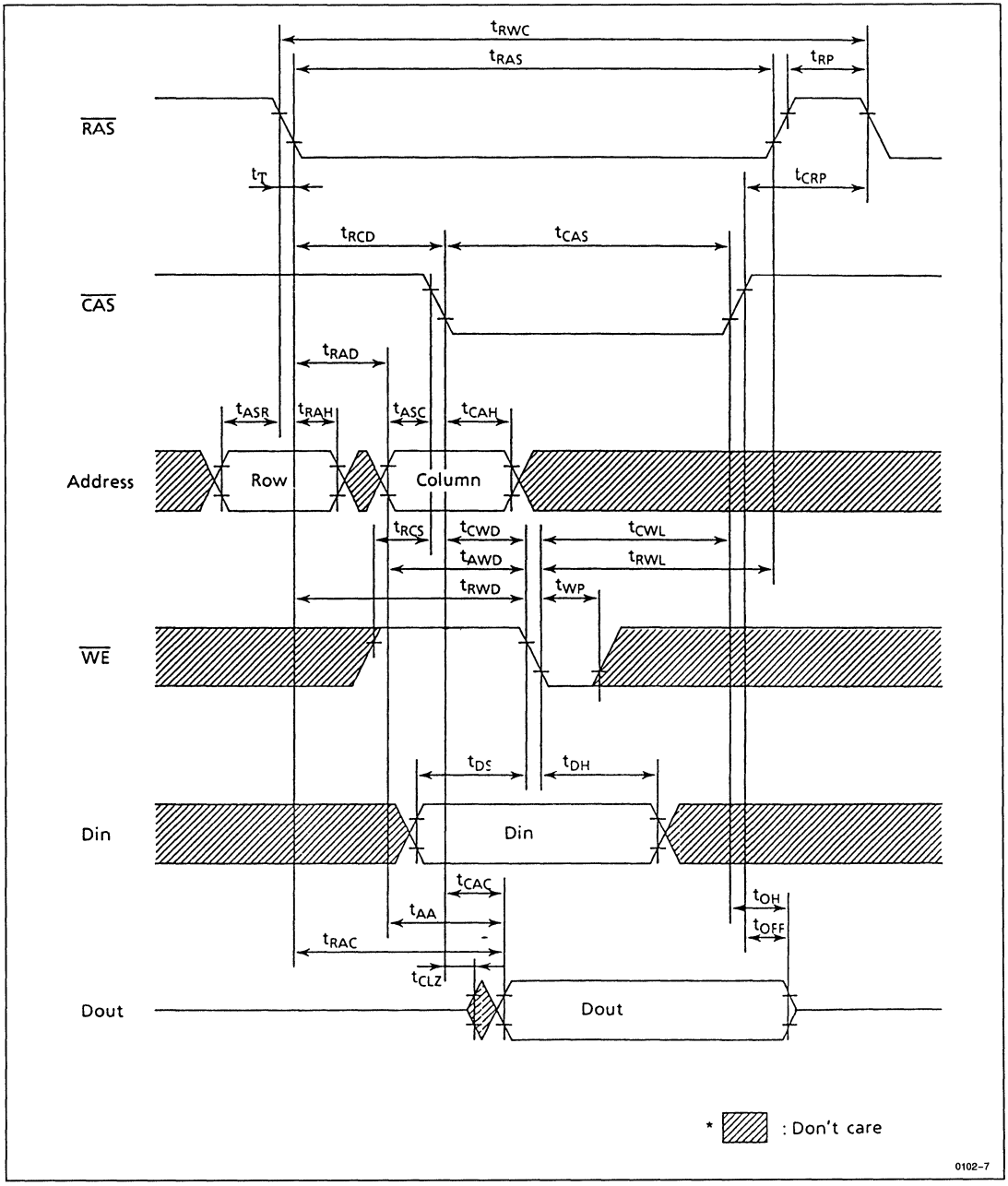
• **Early Write Cycle**



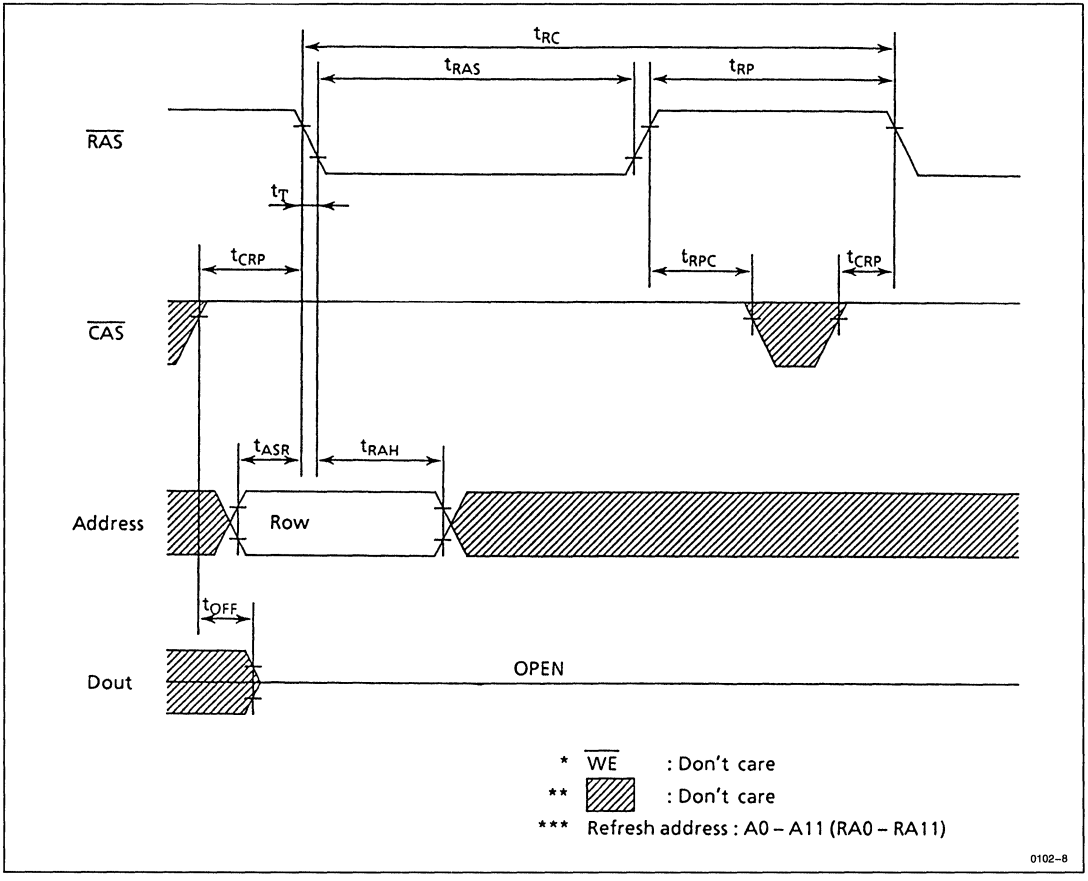
• **Delayed Write Cycle**



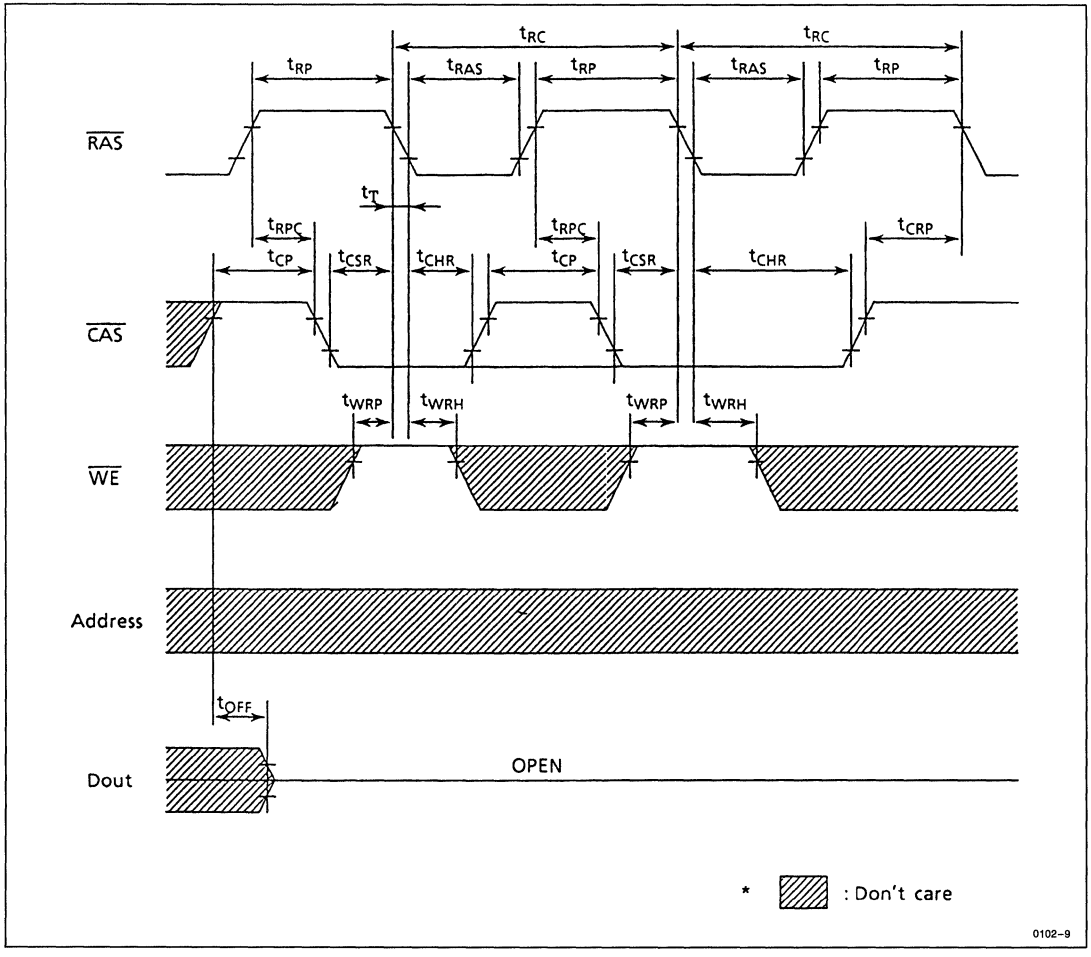
• **Read-Modify-Write Cycle**



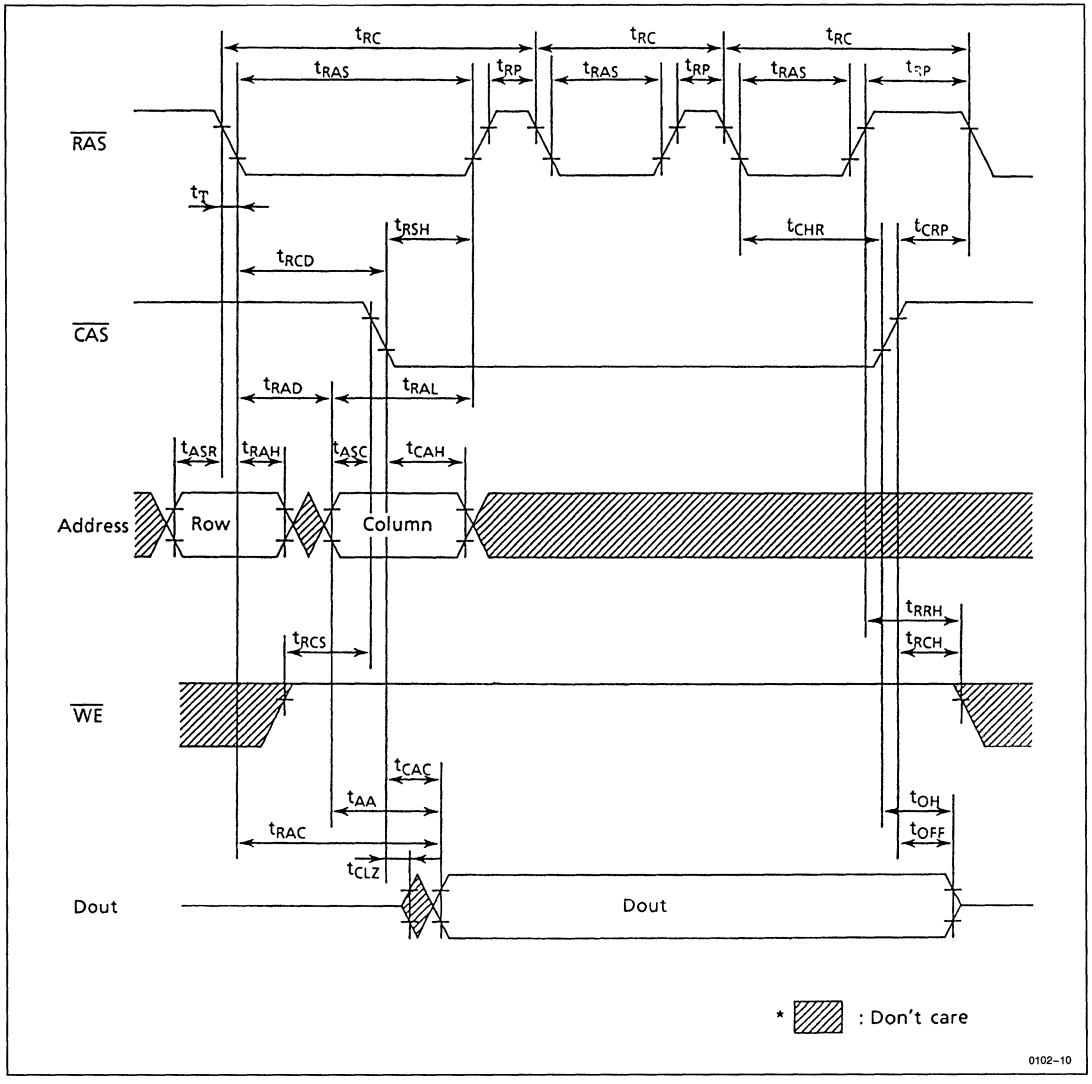
• $\overline{RAS}$ Only Refresh Cycle



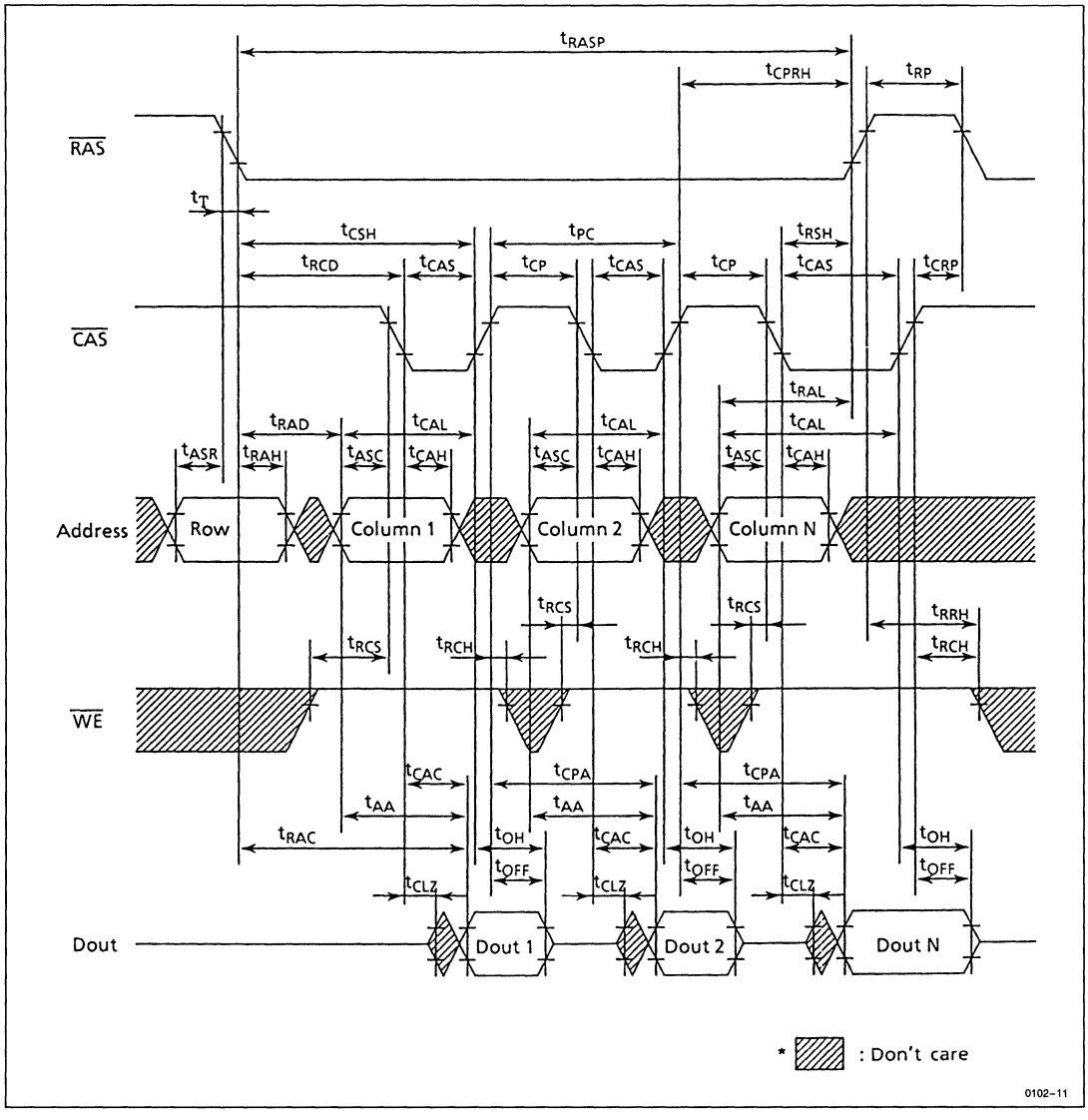
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



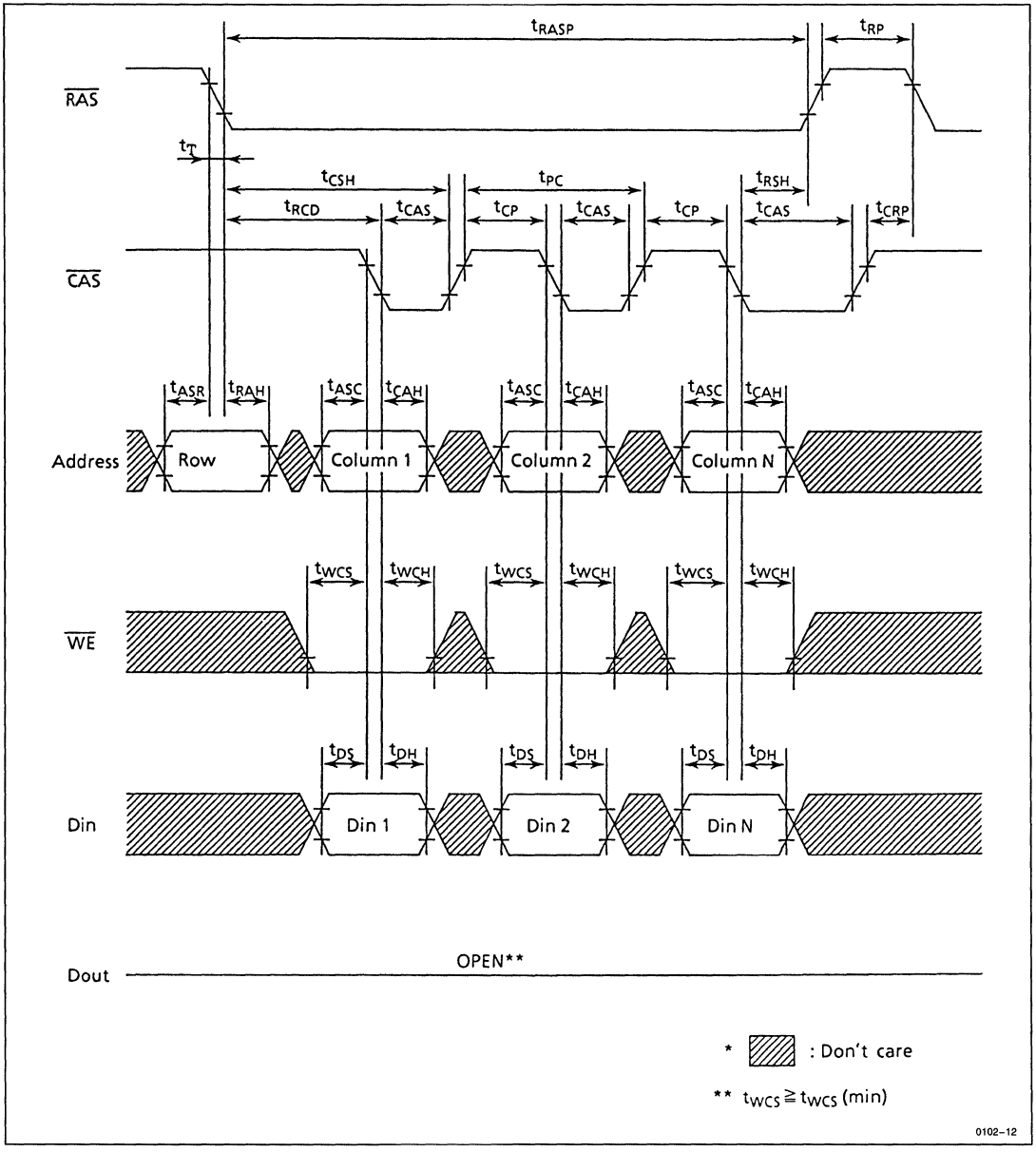
• **Hidden Refresh Cycle**



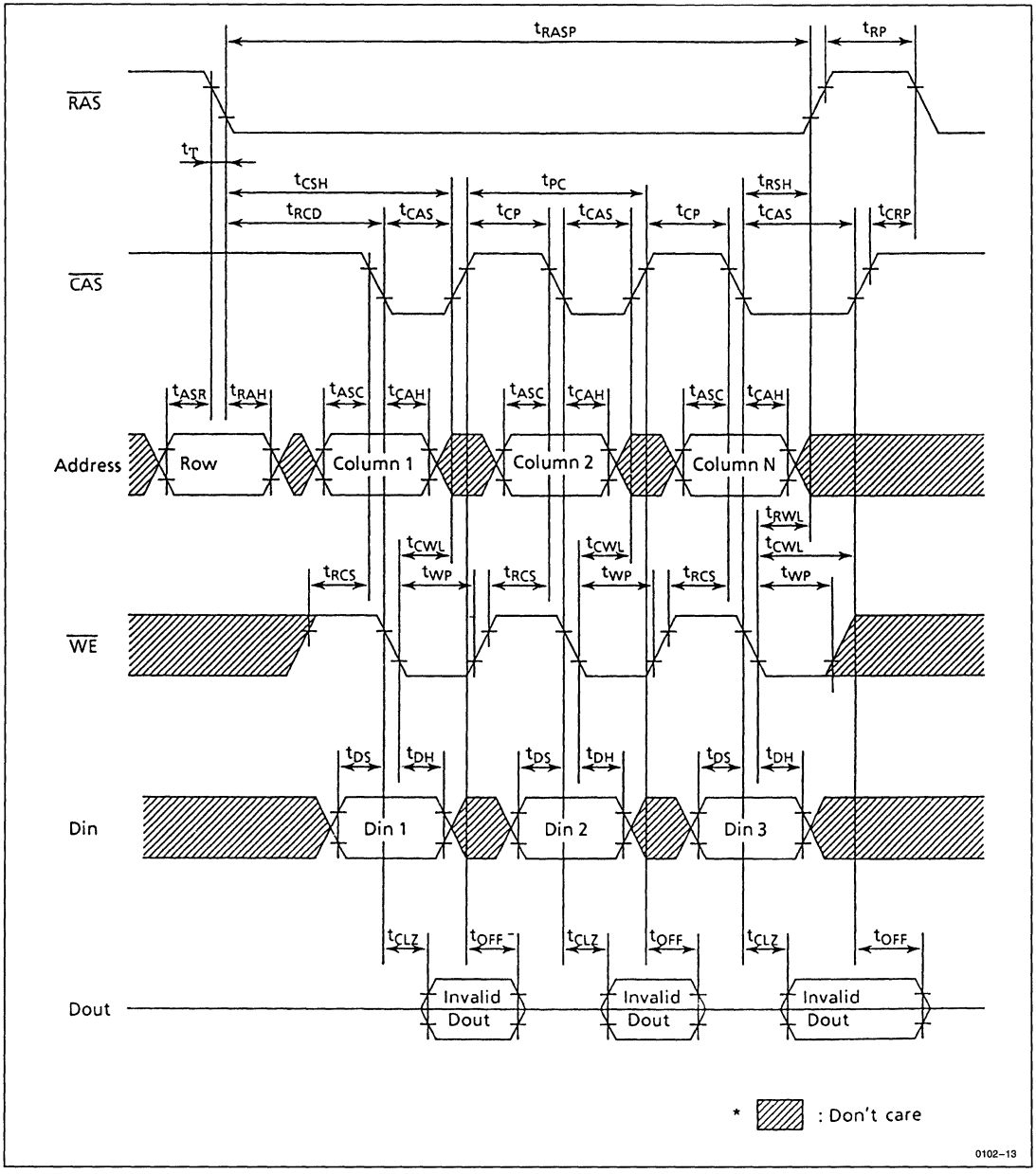
• **Fast Page Mode Read Cycle**



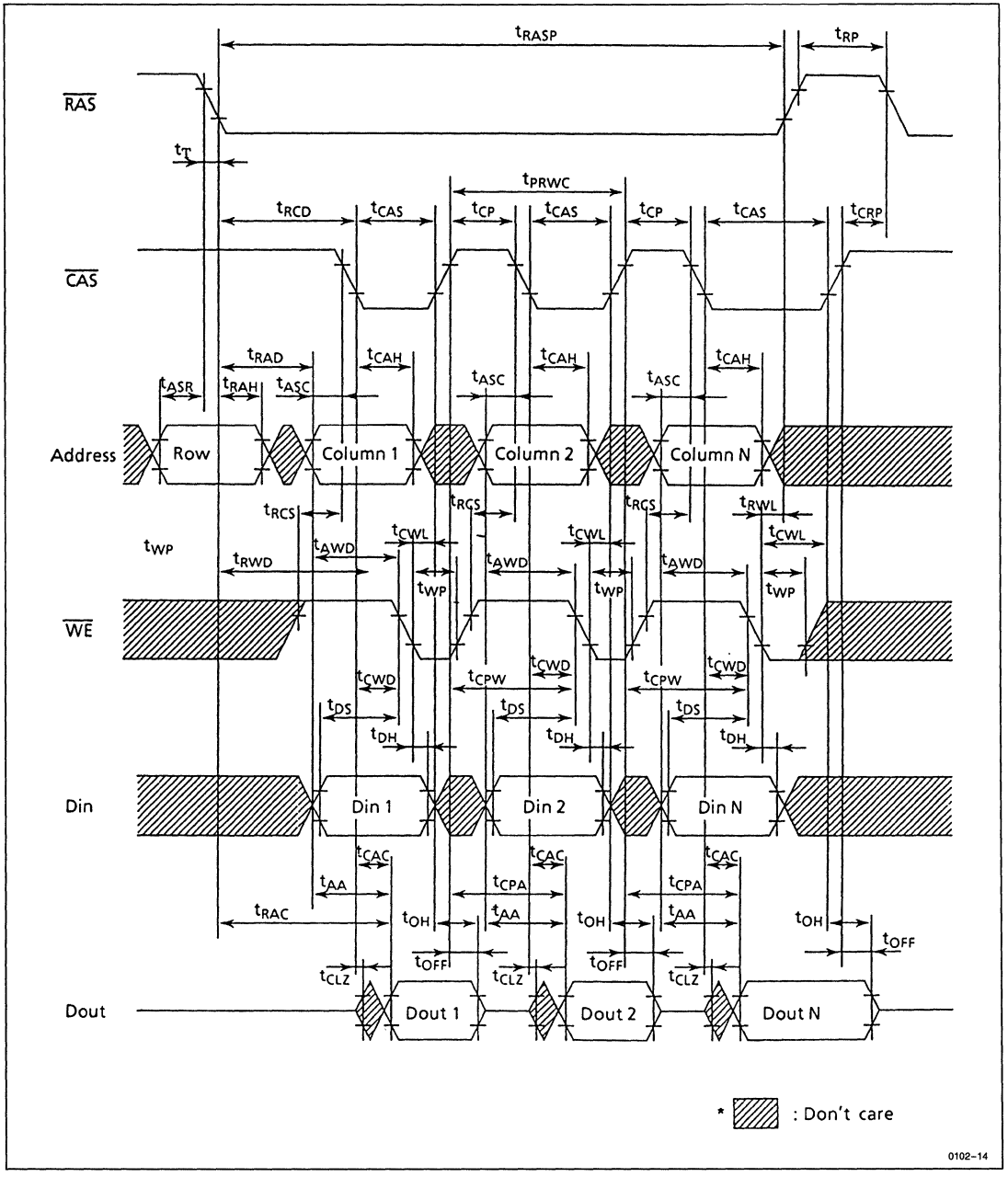
• **Fast Page Mode Early Write Cycle**



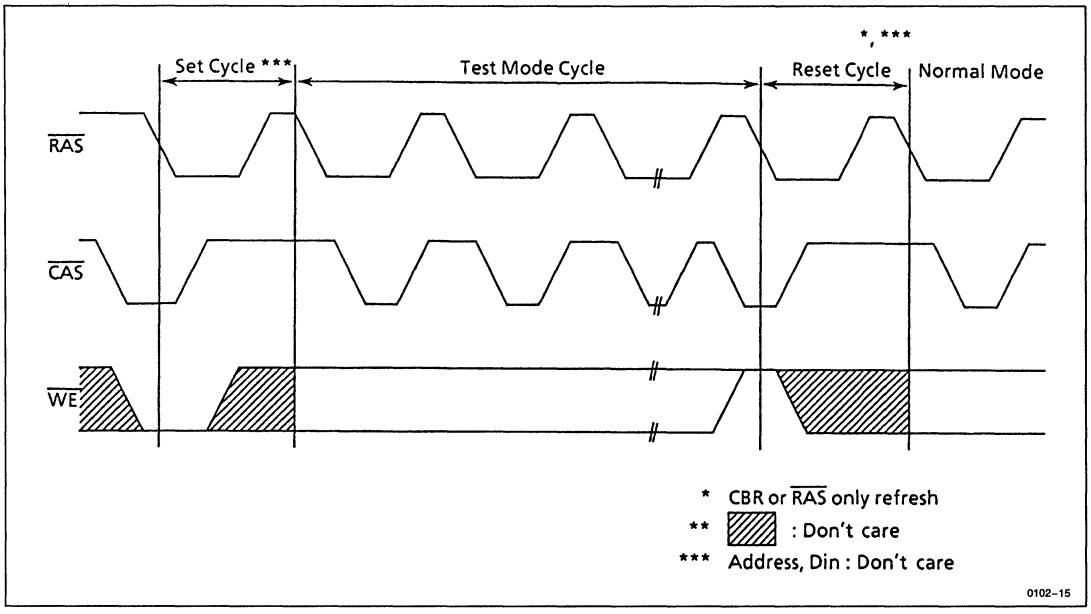
• **Fast Page Mode Delayed Write Cycle**



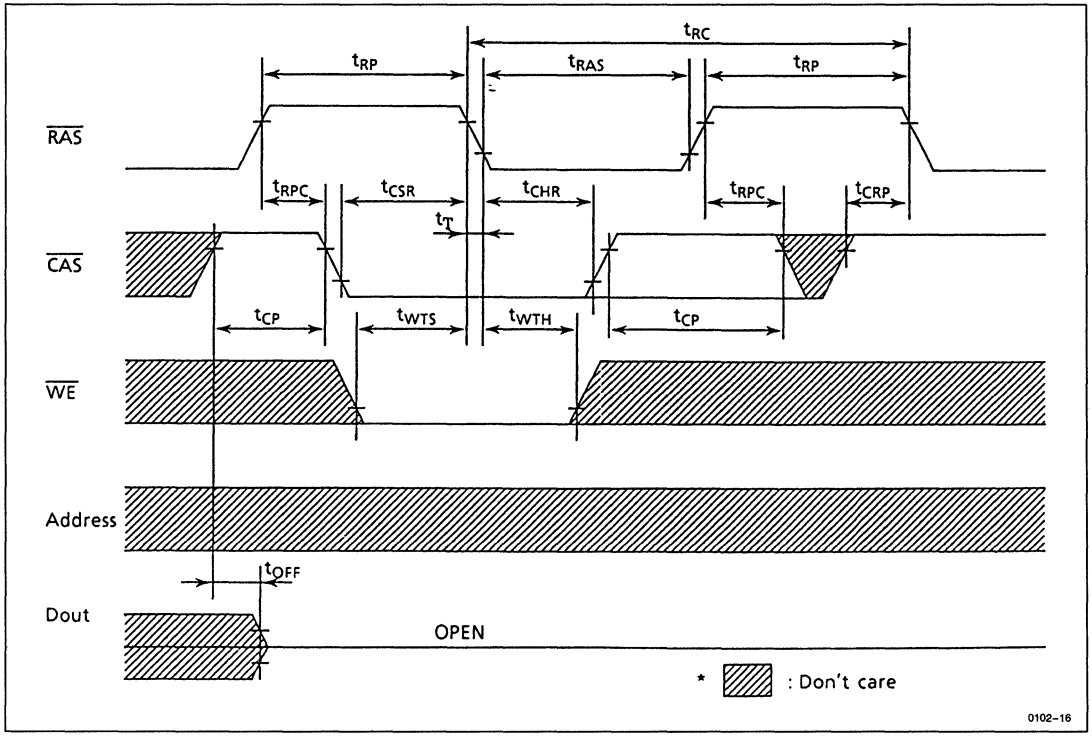
• **Fast Page Mode Read-Modify-Write Cycle**



• **Test Mode Cycle**

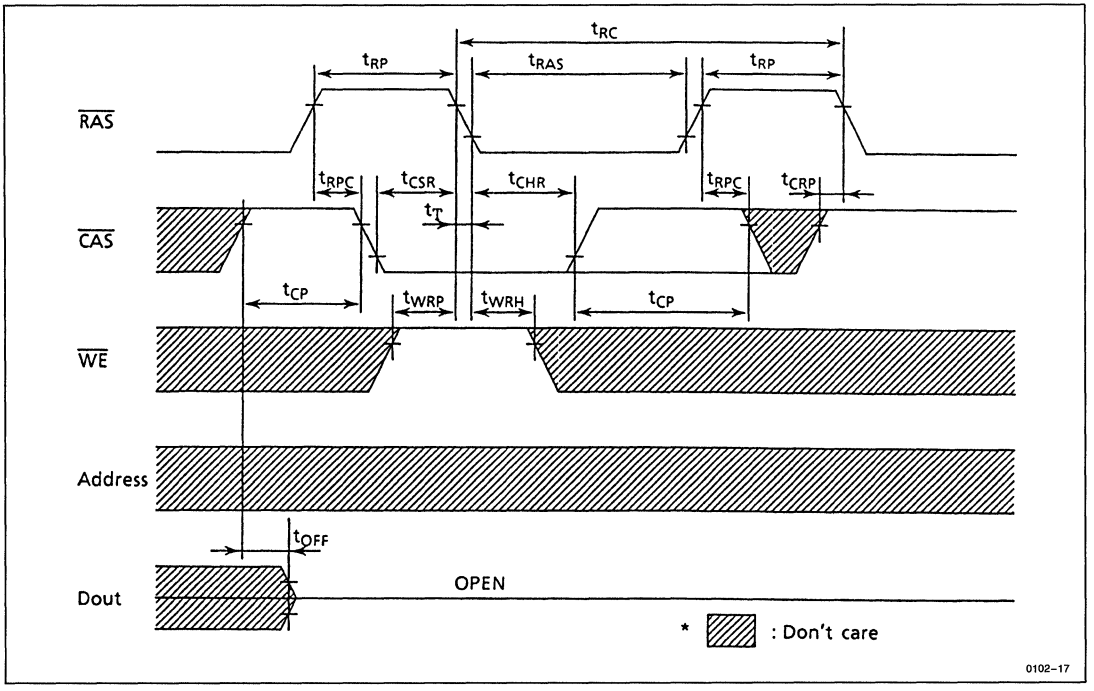


• **Test Mode Set Cycle**

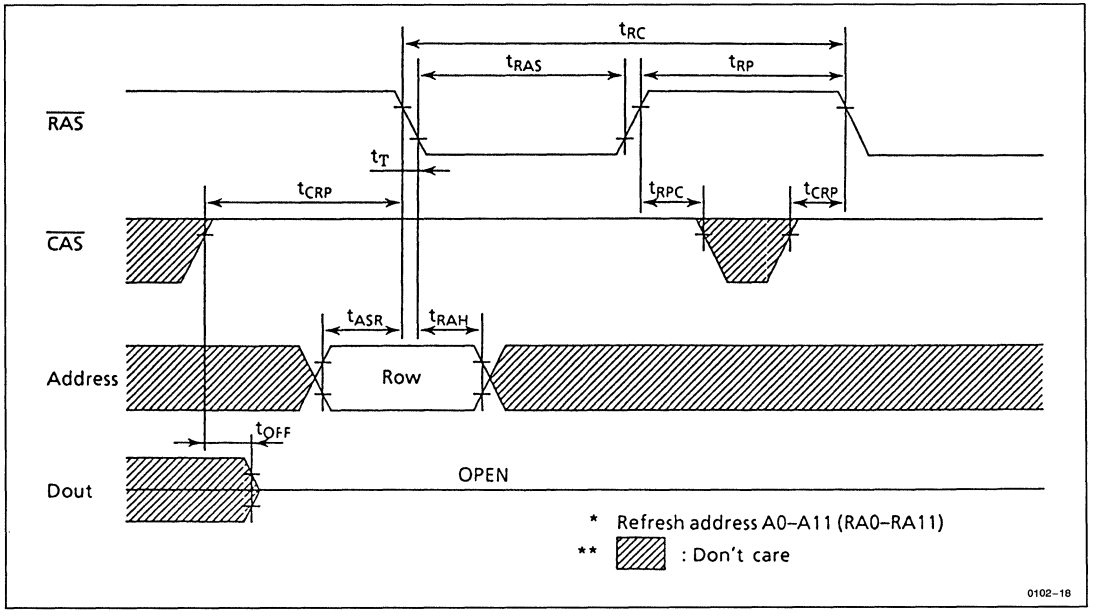


• **Test Mode Reset Cycle**

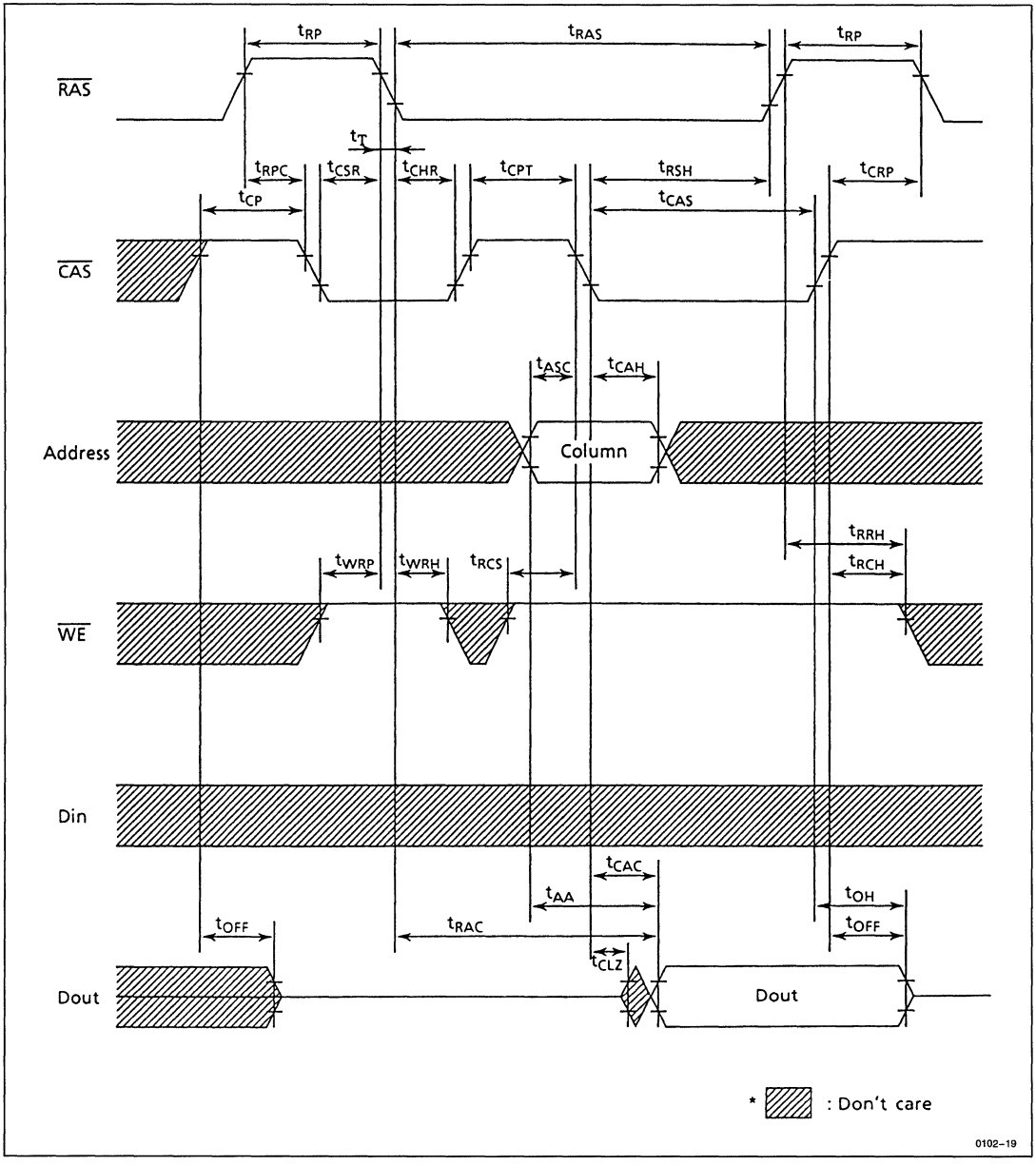
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



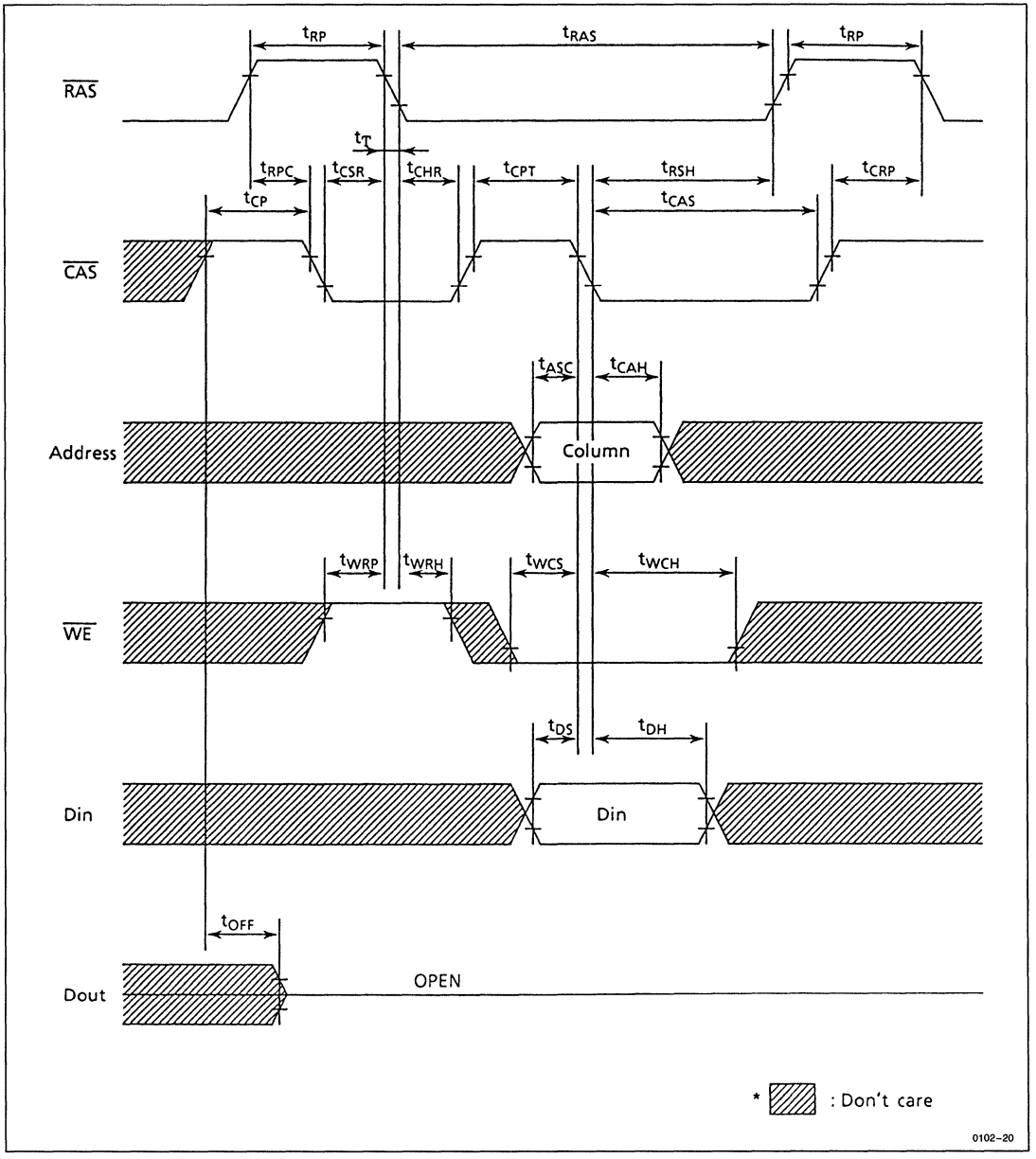
$\overline{RAS}$ Only Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM5116400 Series

Product Preview

4,194,304-Word x 4-Bit Dynamic Random Access Memory

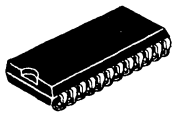
■ DESCRIPTION

The Hitachi HM5116400 is a CMOS dynamic RAM organized 4,194,304 words x 4 bits. It employs the most advanced CMOS technology for high performance and low power. The HM5116400 offers Fast Page Mode as a high speed access mode.

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode.....495 mW/440 mW/385 mW/330 mW (max)
  - Standby Mode.....11 mW (max)
- Fast Page Mode Capability
- Long Refresh Period
  - 4096 Refresh Cycles .....(64 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh

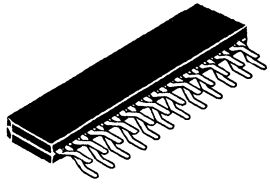
HM5116400J Series



3DCP24D

(CP-24D)

HM5116400Z Series



3DZP24

(ZP-24)

■ ORDERING INFORMATION

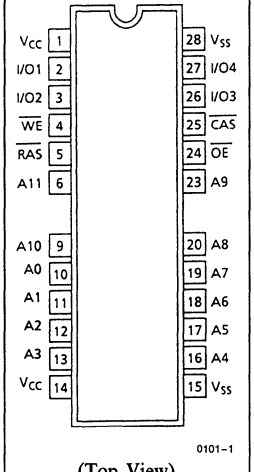
Part No.	Access Time	Package
HM5116400J-6	60 ns	400 mil 24-pin Plastic SOJ (CP-24D)
HM5116400J-7	70 ns	
HM5116400J-8	80 ns	
HM5116400J-10	100 ns	
HM5116400Z-6	60 ns	475 mil 24-pin Plastic ZIP (ZP-24)
HM5116400Z-7	70 ns	
HM5116400Z-8	80 ns	
HM5116400Z-10	100 ns	

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{11}	Address Input
A_0–A_{11}	Refresh Address Input
I/O_0–I/O_4	Data Input/Data Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

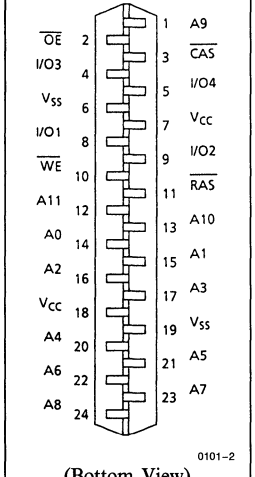
■ PIN OUT

HM5116400J Series



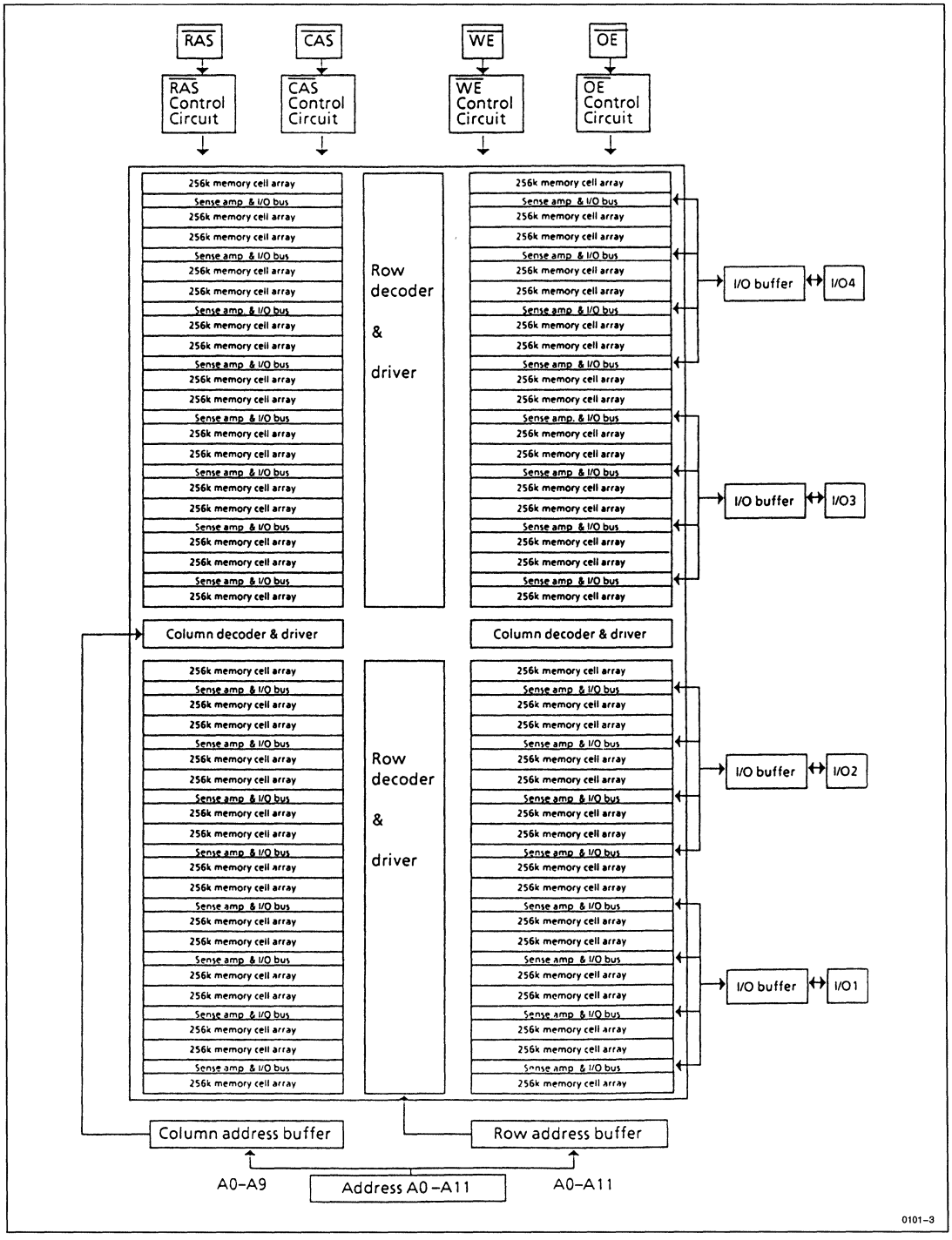
(Top View)

HM5116400Z Series



(Bottom View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HM5116400J/Z								Unit	Test Conditions	Note
		-6		-7		-8		-10				
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	70	—	60	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	1	—	1	—	1	—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	90	—	80	—	70	—	60	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1, 4
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	90	—	80	—	70	—	60	mA	t_{RC} = Min	4
Fast Page Mode Current	I_{CC7}	—	70	—	60	—	50	—	45	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{IN} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. Clock voltages ($\overline{RAS}$ and $\overline{CAS}$) must be applied simultaneously with or prior to applying supply voltage.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	C_O	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 2, 3, 19, 20]

Read, Write Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM5116400J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	70	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10000	18	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	10	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	52	20	60	20	75	ns	4
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	15	55	ns	5
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	18	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	5	—	5	—	ns	
$\overline{OE}$ to Din Delay Time	t_{OED}	15	—	18	—	20	—	25	—	ns	6
$\overline{OE}$ Delay Time from Din	t_{DZO}	0	—	0	—	0	—	0	—	ns	7
$\overline{CAS}$ Delay Time from Din	t_{DZC}	0	—	0	—	0	—	0	—	ns	7
Transition Time (Rise and Fall)	t_T	3	30	3	30	3	30	3	30	ns	8

Read Cycle

Parameter	Symbol	HM5116400J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	9, 10, 21
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	18	—	20	—	25	ns	10, 11, 21
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	ns	10, 12, 21
Access Time from $\overline{OE}$	t_{OEA}	—	15	—	18	—	20	—	25	ns	10, 21
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	ns	13
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	5	—	5	—	5	—	5	—	ns	13
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	ns	
Column Address to $\overline{CAS}$ Lead Time	t_{CAL}	30	—	35	—	40	—	45	—	ns	
$\overline{CAS}$ to Output in Low-Z	t_{CLZ}	0	—	0	—	0	—	0	—	ns	

Read Cycle (continued)

Parameter	Symbol	HM5116400J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Output Data Hold Time	t_{OH}	3	—	3	—	3	—	3	—	ns	
Output Data Hold Time from $\overline{OE}$	t_{OHO}	3	—	3	—	3	—	3	—	ns	
Output Buffer Turn-off Time	t_{OFF}	—	15	—	18	—	20	—	25	ns	14
Output Buffer Turn-off Time to $\overline{OE}$	t_{OEZ}	—	15	—	18	—	20	—	25	ns	14
$\overline{CAS}$ to Din Delay Time	t_{CDD}	15	—	18	—	20	—	25	—	ns	6

Write Cycle

Parameter	Symbol	HM5116400J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	15
Write Command Hold Time	t_{WCH}	15	—	15	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	18	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	18	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	16
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	20	—	ns	16

Read-Modify-Write Cycle

Parameter	Symbol	HM5116400J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	150	—	176	—	200	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	93	—	105	—	135	—	ns	15
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	35	—	41	—	45	—	60	—	ns	15
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	50	—	58	—	65	—	80	—	ns	15
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	15	—	18	—	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM5116400J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time (CBR Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time (CBR Refresh Cycle)	t_{CHR}	20	—	20	—	20	—	20	—	ns	
$\overline{WE}$ Setup Time (CBR Refresh Cycle)	t_{WRP}	10	—	10	—	10	—	10	—	ns	
$\overline{WE}$ Hold Time (CBR Refresh Cycle)	t_{WRH}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	0	—	0	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM5116400J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASP}	—	100000	—	100000	—	100000	—	100000	ns	17
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	35	—	40	—	45	—	50	ns	18, 21
$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	t_{CPW}	55	—	63	—	70	—	85	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{CPRH}	35	—	40	—	45	—	50	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM5116400J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	80	—	91	—	100	—	110	—	ns	

Test Mode Cycle

Parameter	Symbol	HM5116400J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WTS}	10	—	10	—	10	—	10	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WTH}	10	—	10	—	10	—	10	—	ns	

Counter Test Cycle

Parameter	Symbol	HM5116400J/Z								Unit	Note
		-6		-7		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	TBD	—	TBD	—	TBD	—	TBD	ns		

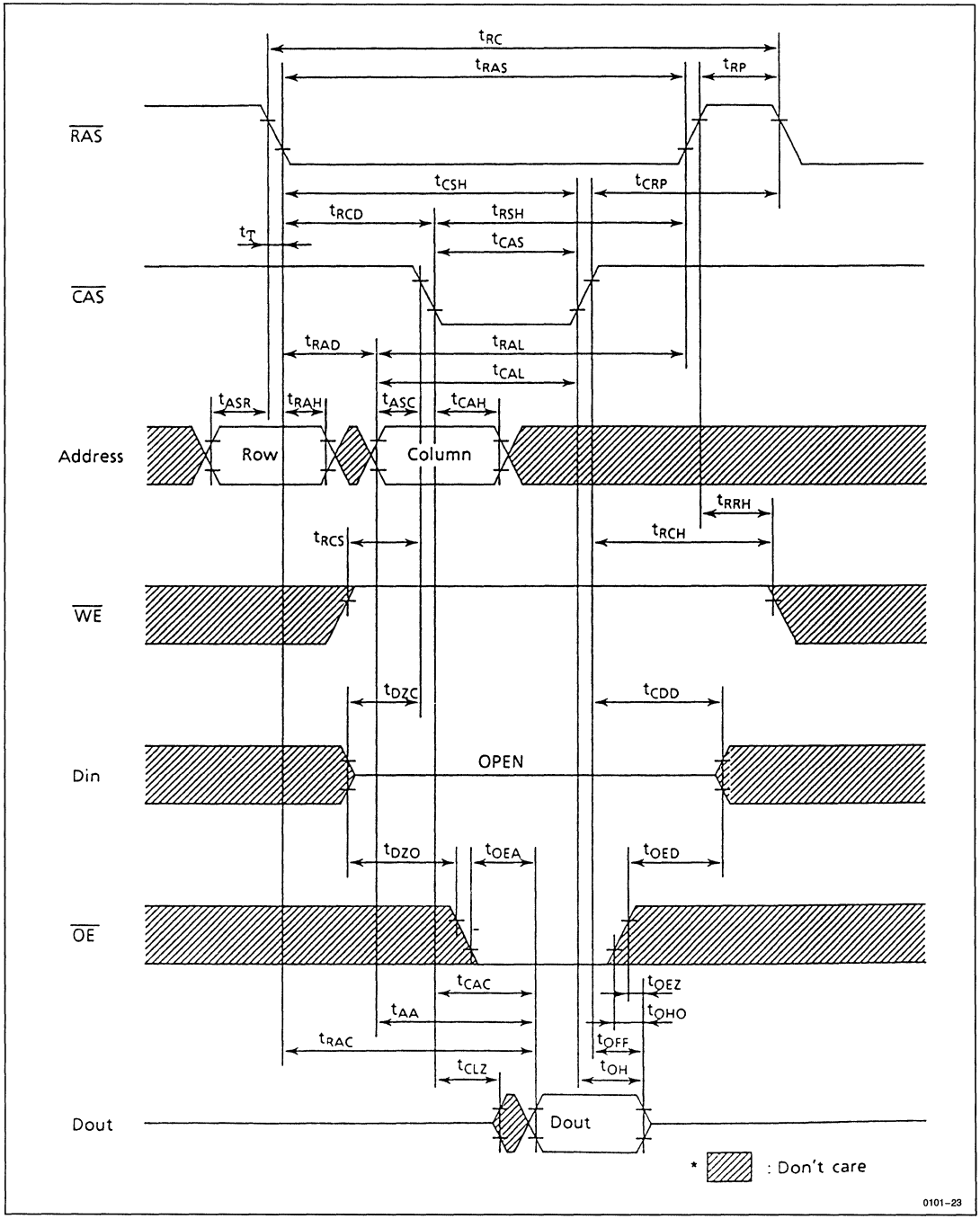
Refresh (T_J = 85°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Max	Unit	Note
Refresh Period	t_{REF}	64	ms	4096 Cycles

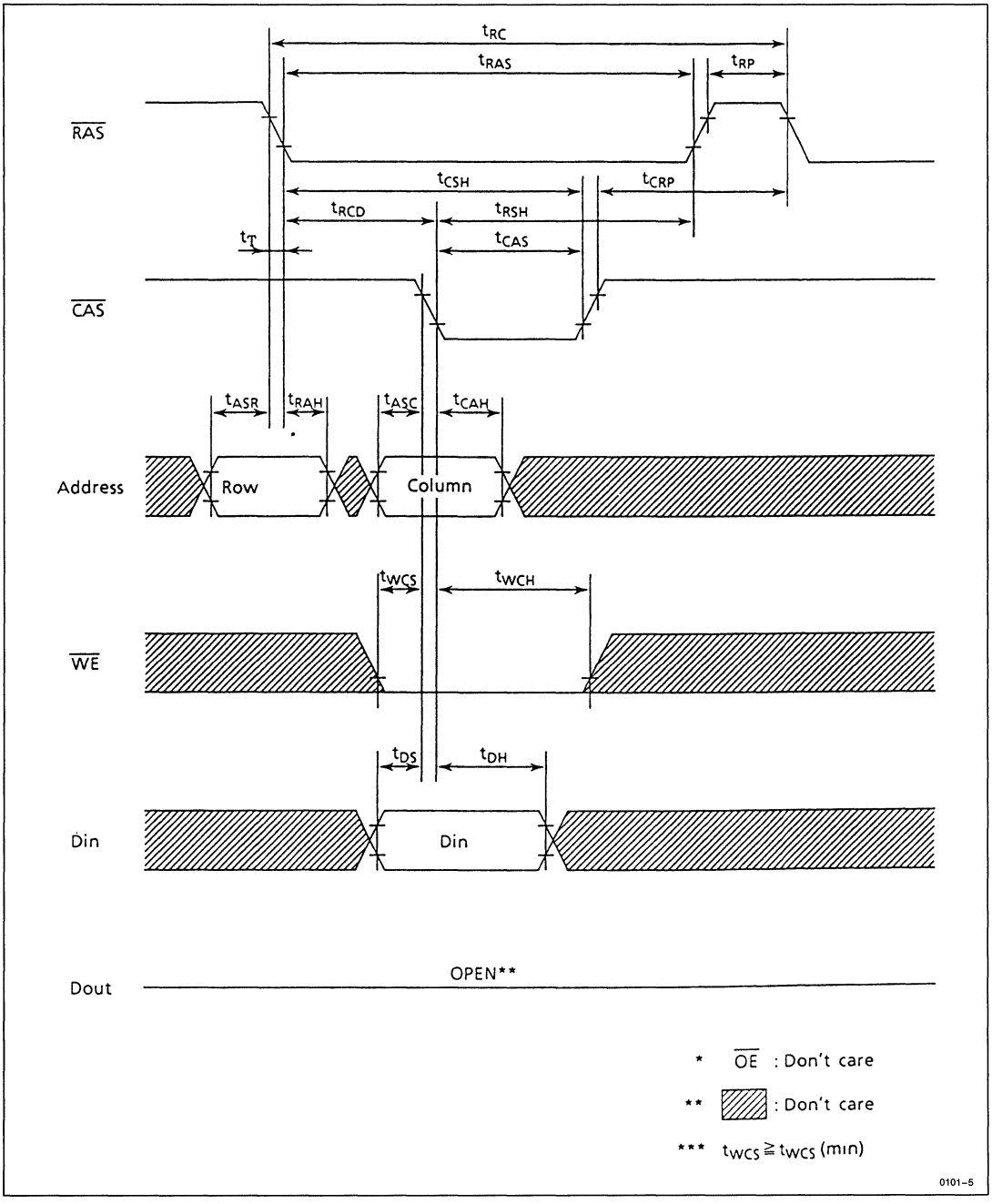
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ only Refresh or $\overline{CAS}$ before $\overline{RAS}$ Refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
3. Only row address is indispensable on address A10 and A11.
4. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
5. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
6. Either t_{ODD} or t_{CDD} must be satisfied.
7. Either t_{DZO} or t_{DZC} must be satisfied.
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
9. Assumes that $t_{RCD} < t_{RCD}$ (max) and $t_{RAD} < t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
10. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
12. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
13. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
14. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min) the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
16. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
17. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
18. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
19. In delay write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
20. Test mode operation specified in this data sheet is 16 bits test function controlled by compression addresses ... CA0 and CA1. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of four test bits on each I/O accord with each other, the state of the output data on the I/O is high level. When the state of four test bits on the I/O do not accord with each other, the state of the output data on the I/O is low level. Data input and output pins are I/O_1–I/O_4. If any refresh cycle is occurred, the test mode is reset.
21. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{CPA} is delayed by 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORMS

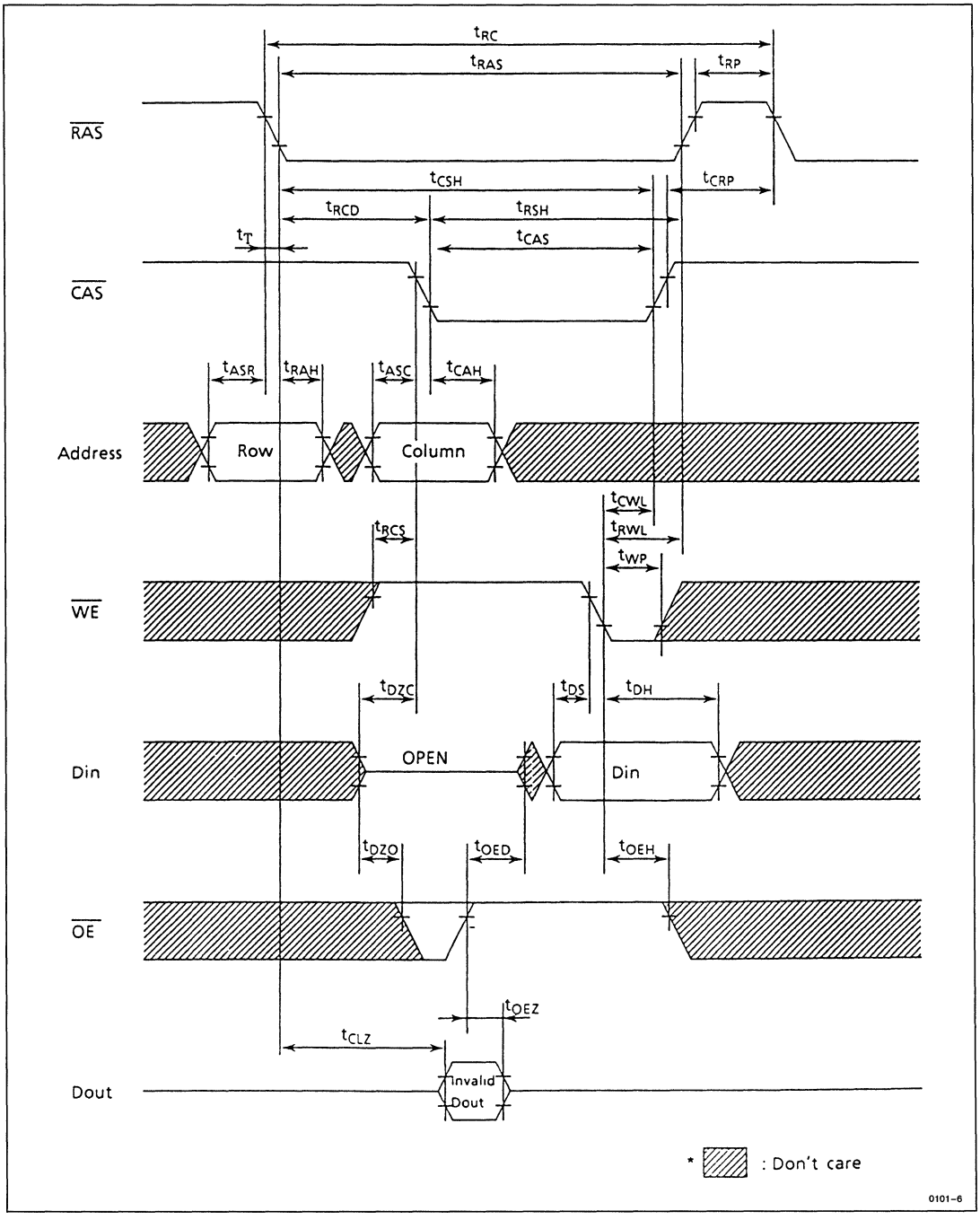
• Read Cycle



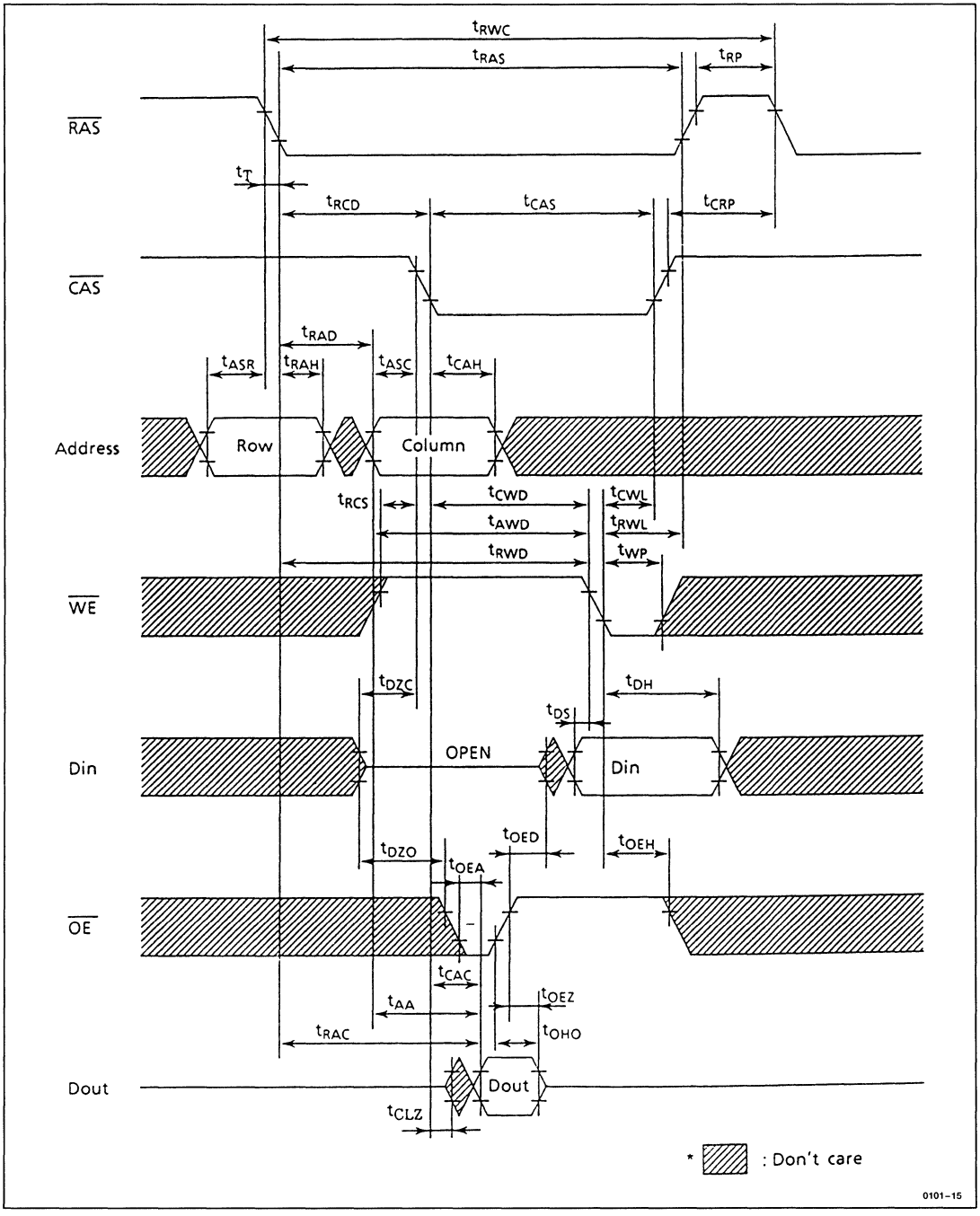
• **Early Write Cycle**



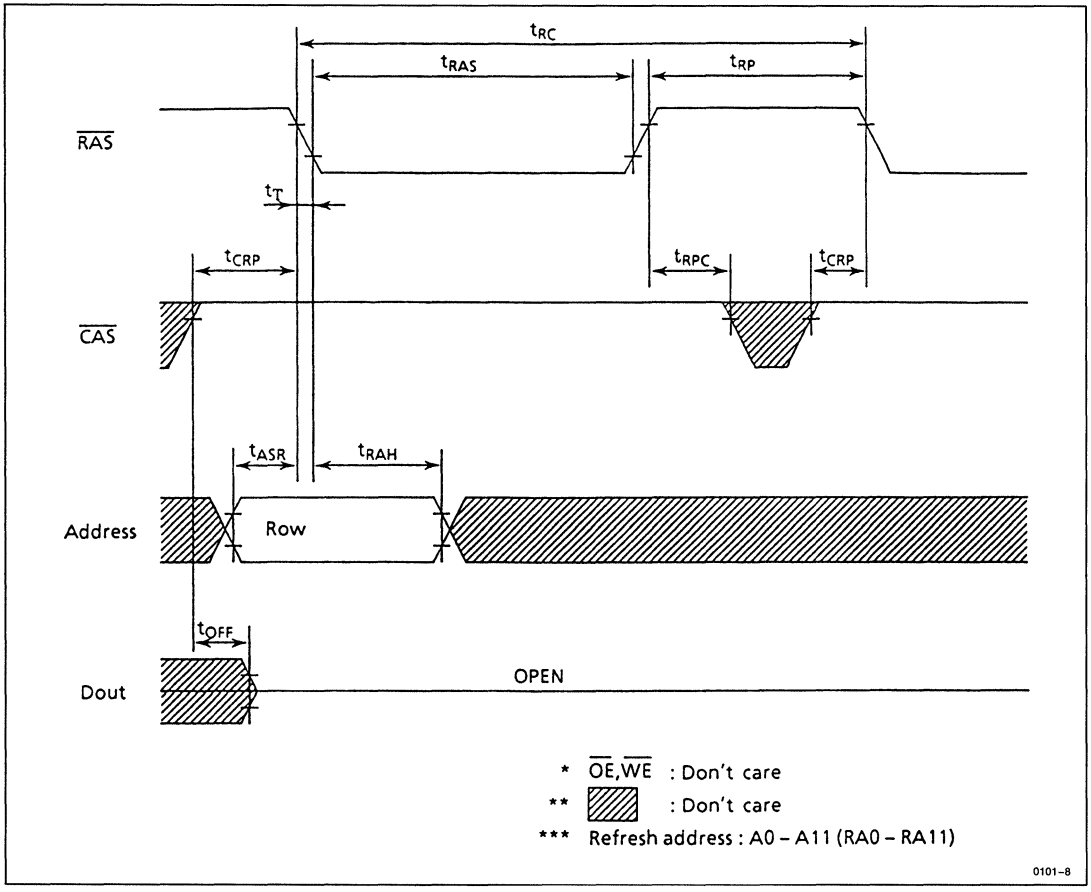
• **Delayed Write Cycle**



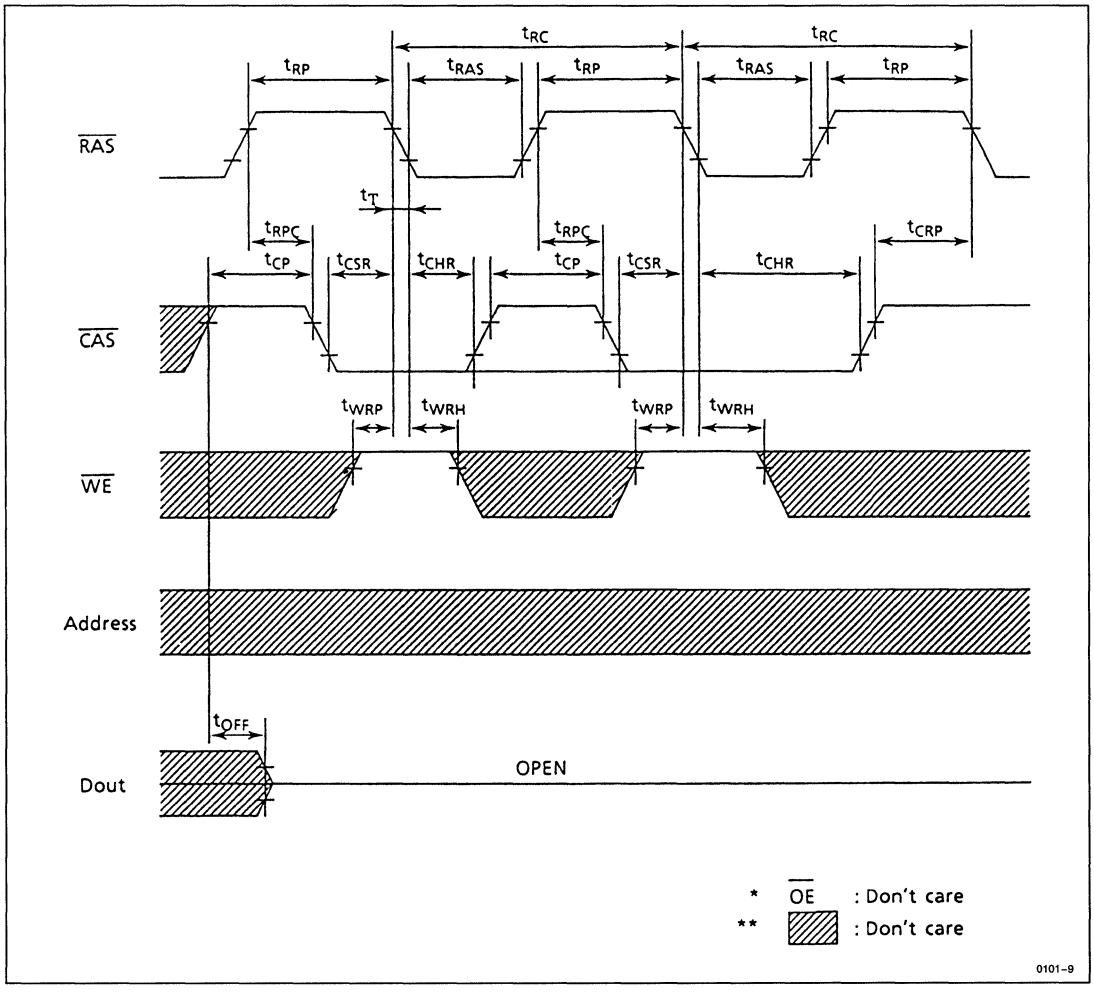
• **Read-Modify-Write Cycle**



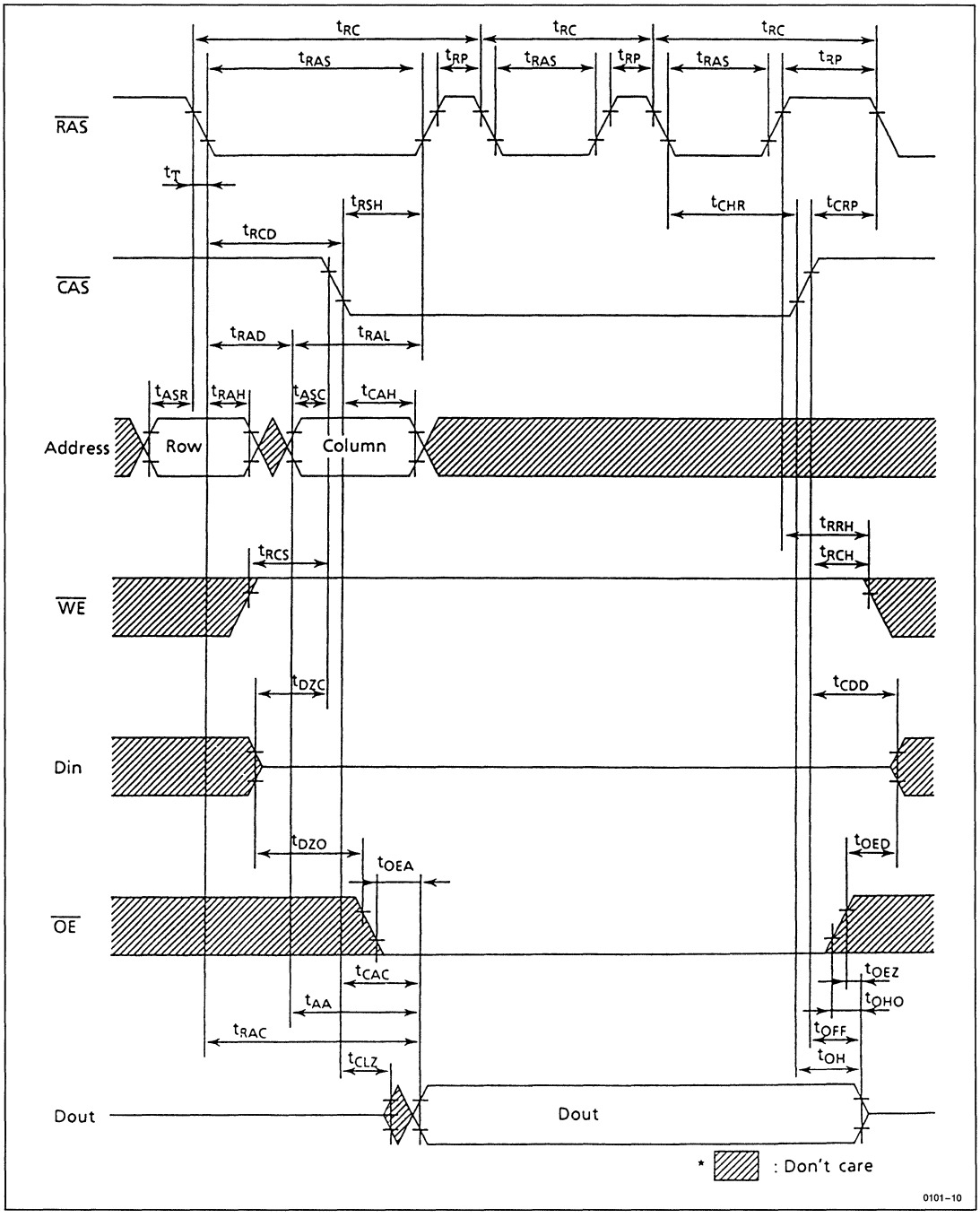
• $\overline{RAS}$ Only Refresh Cycle



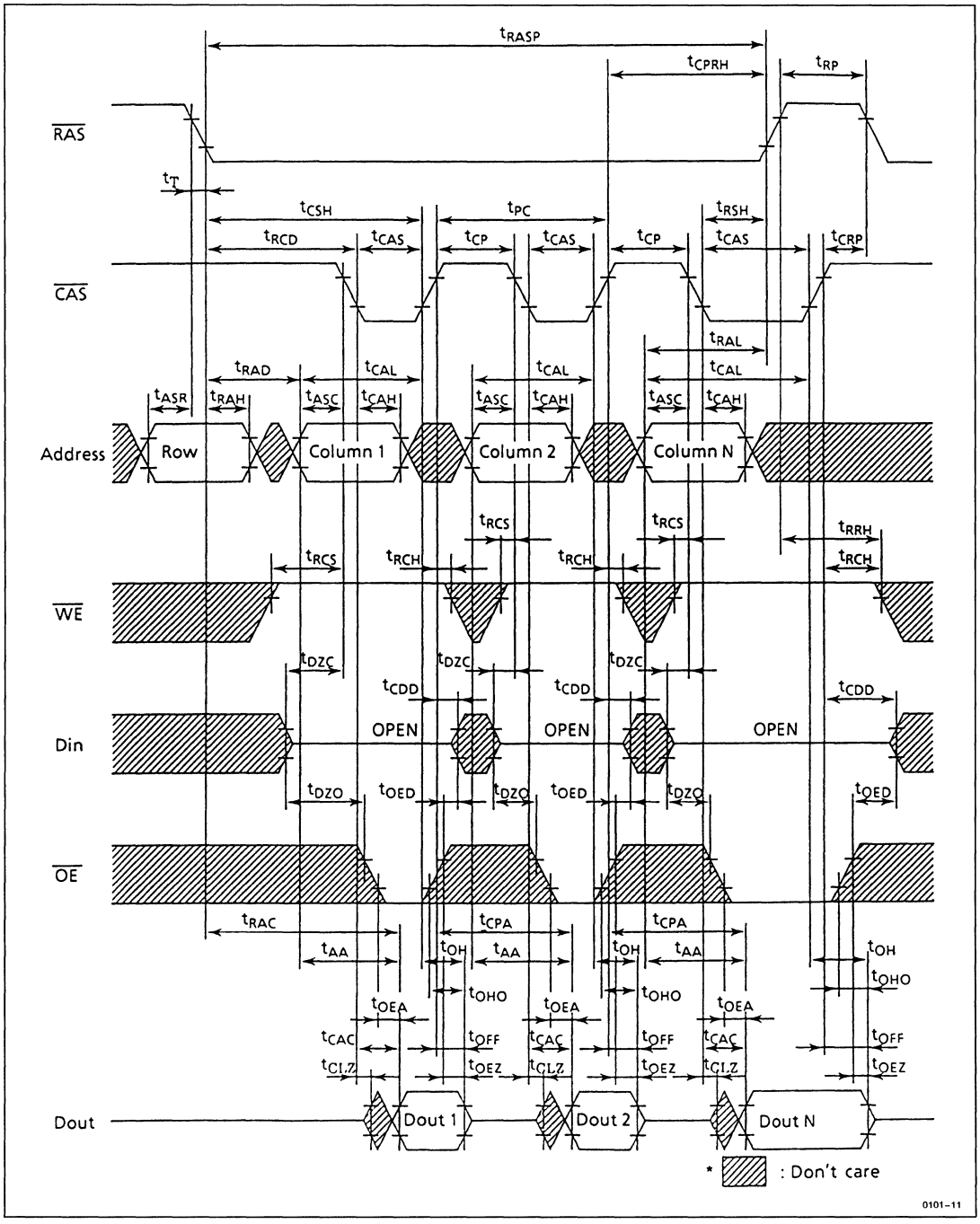
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



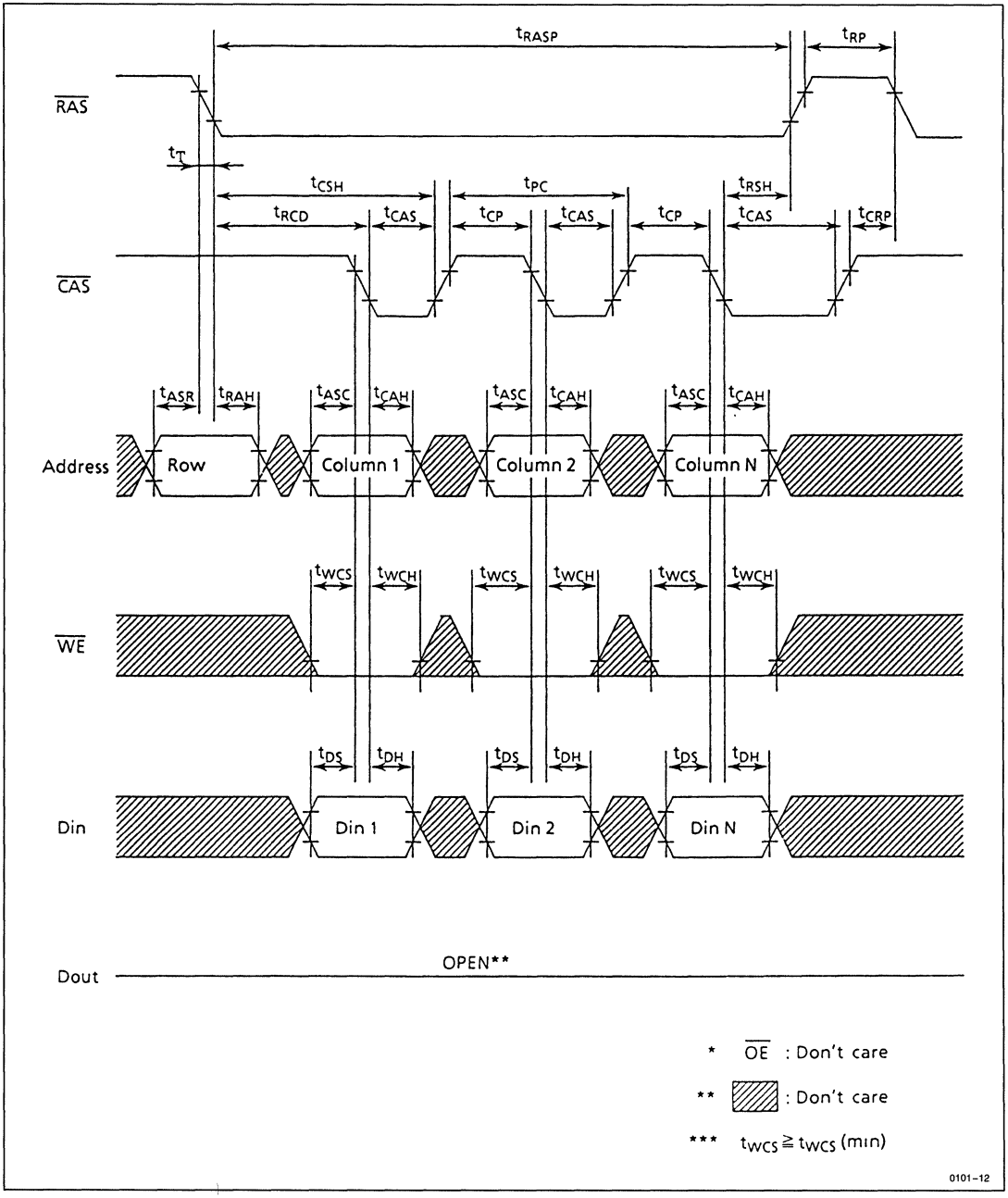
• **Hidden Refresh Cycle**



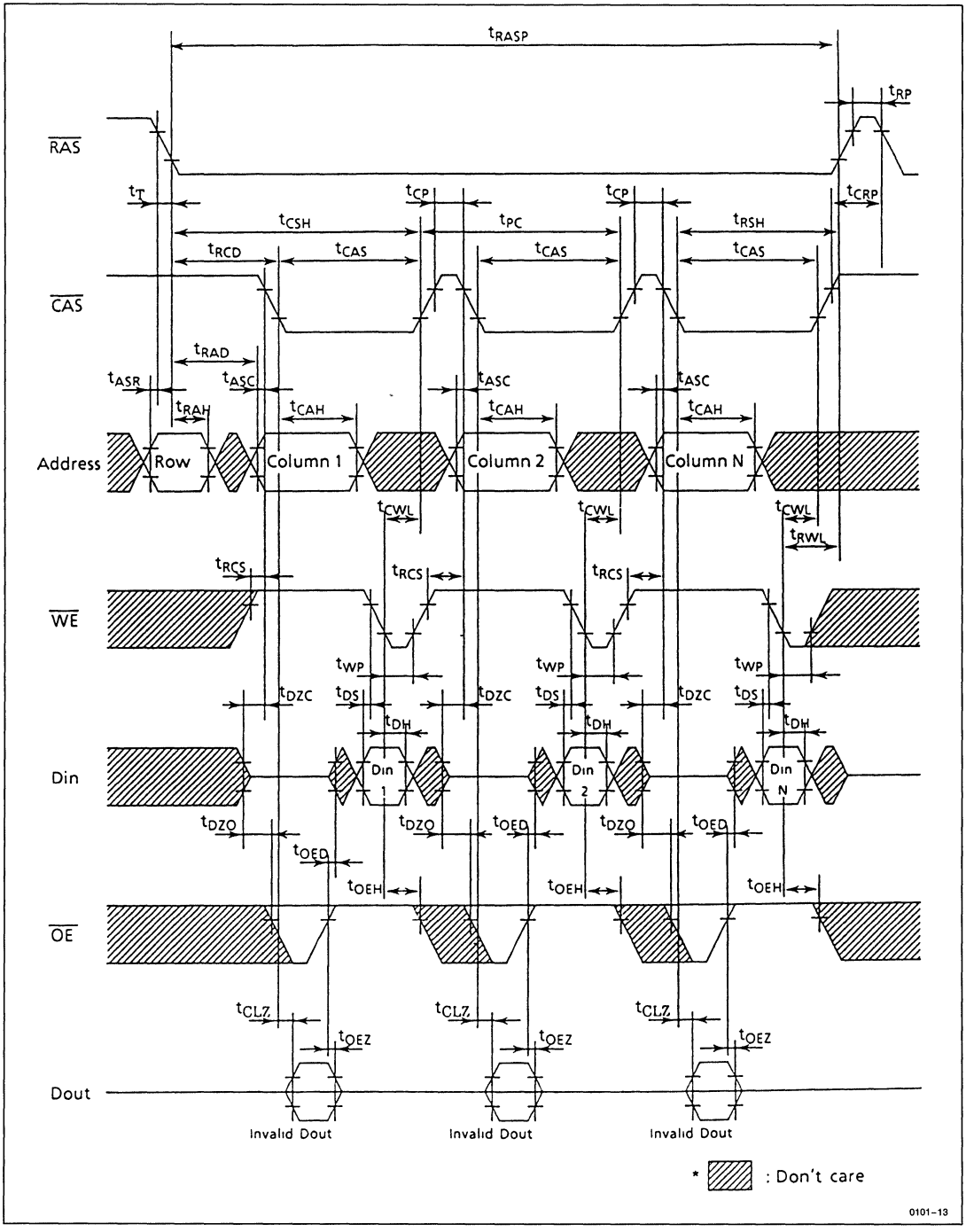
• **Fast Page Mode Read Cycle**



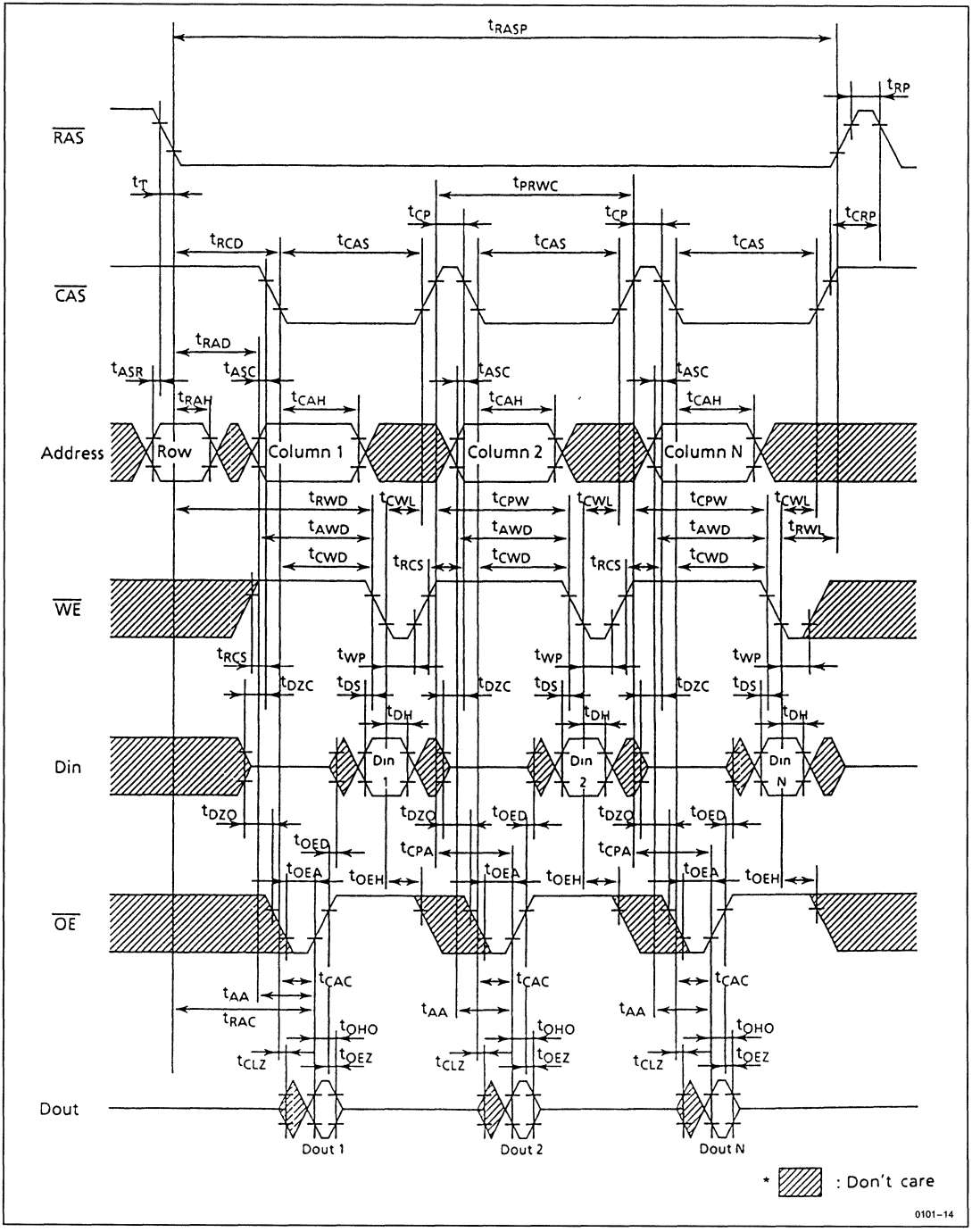
• **Fast Page Mode Early Write Cycle**



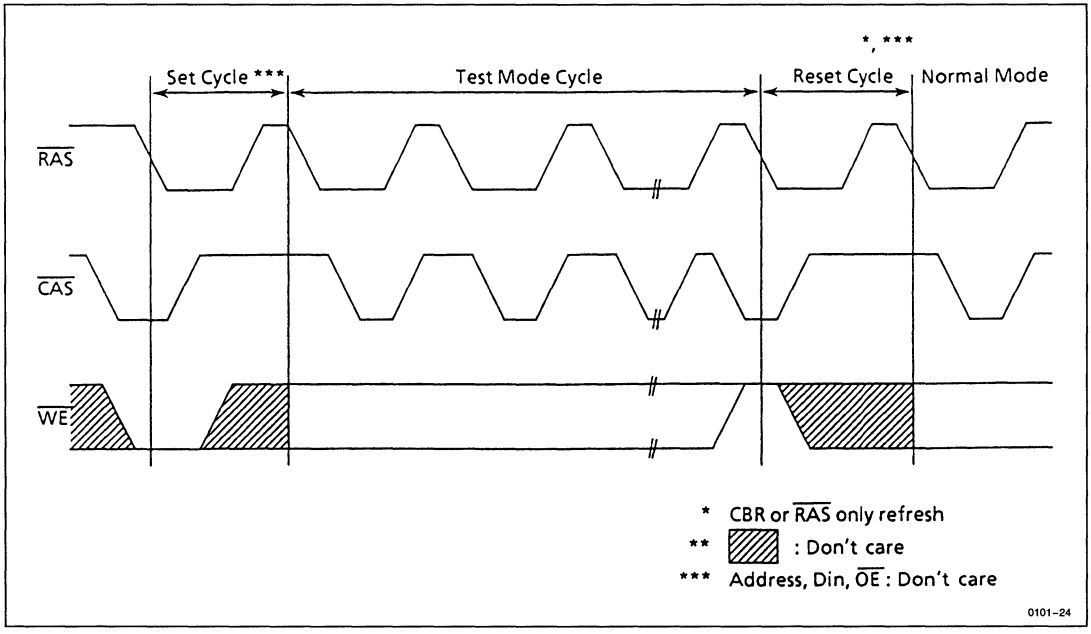
• **Fast Page Mode Delayed Write Cycle**



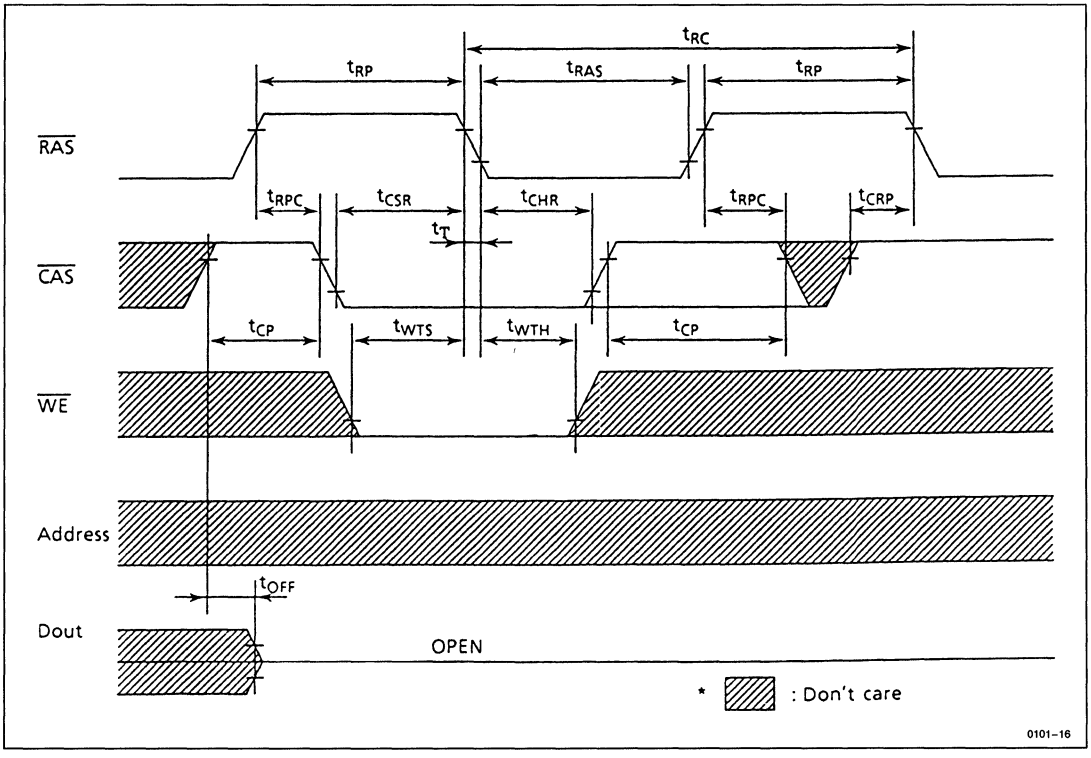
• **Fast Page Mode Read-Modify-Write Cycle**



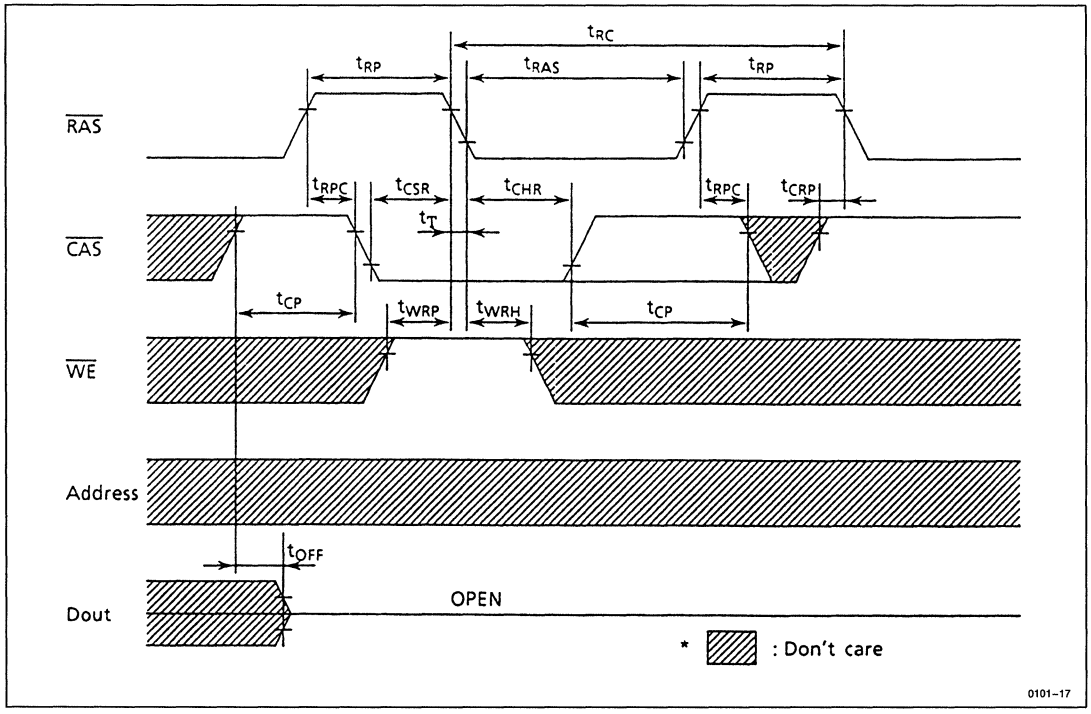
• **Test Mode Cycle**



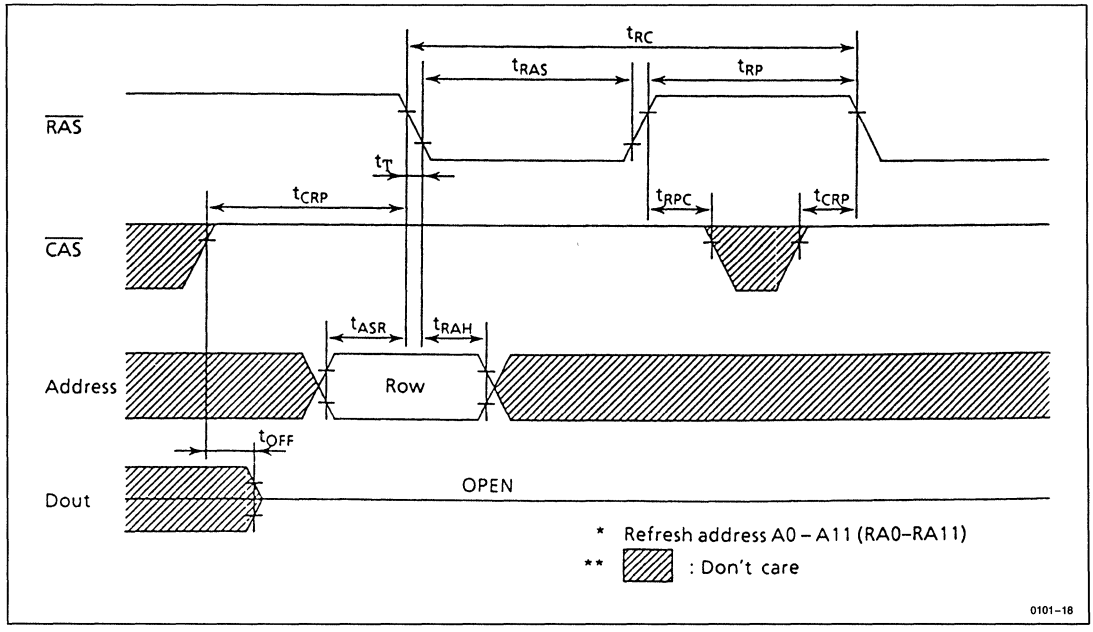
•**Test Mode Set Cycle**



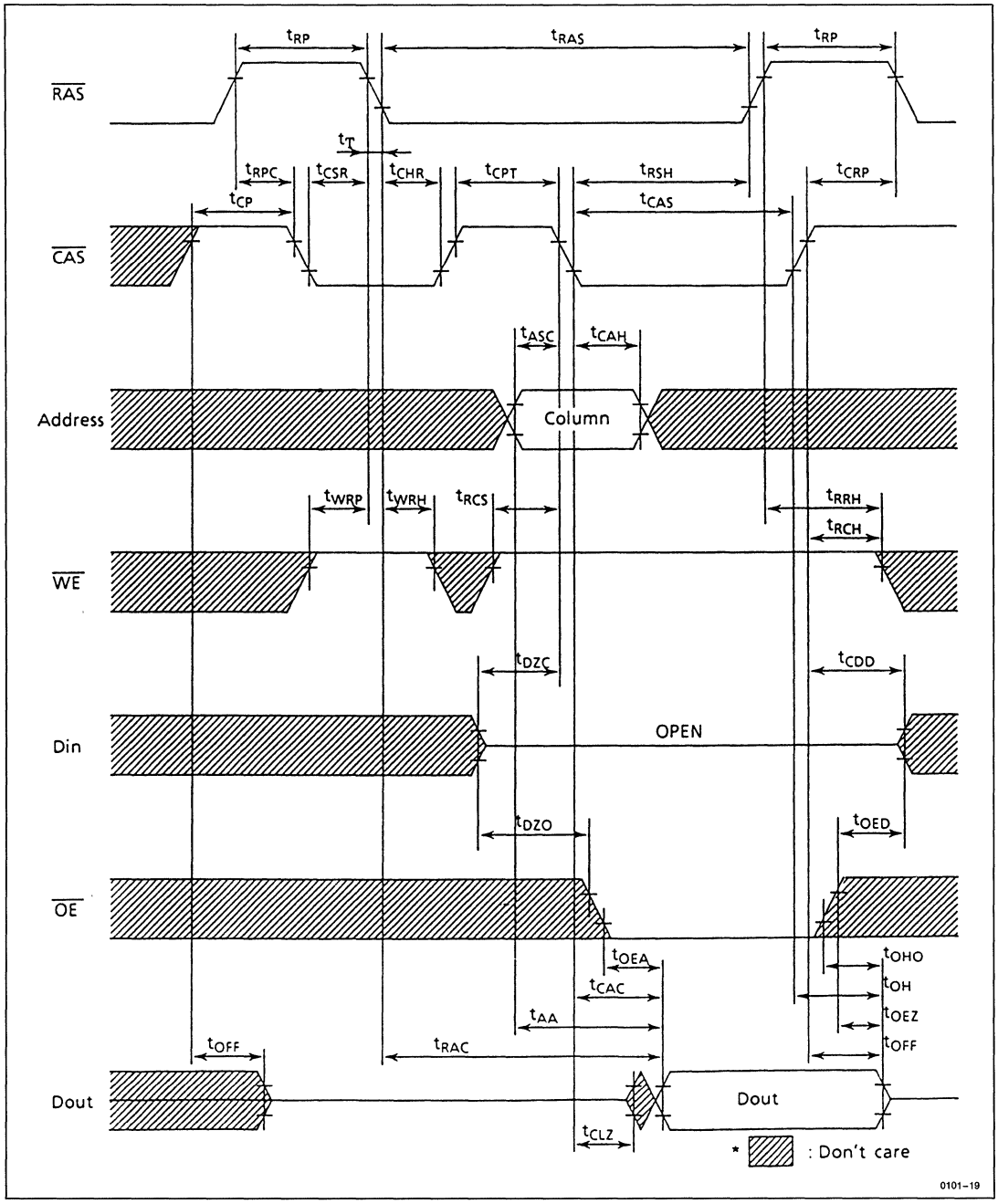
•Test Mode Reset Cycle
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



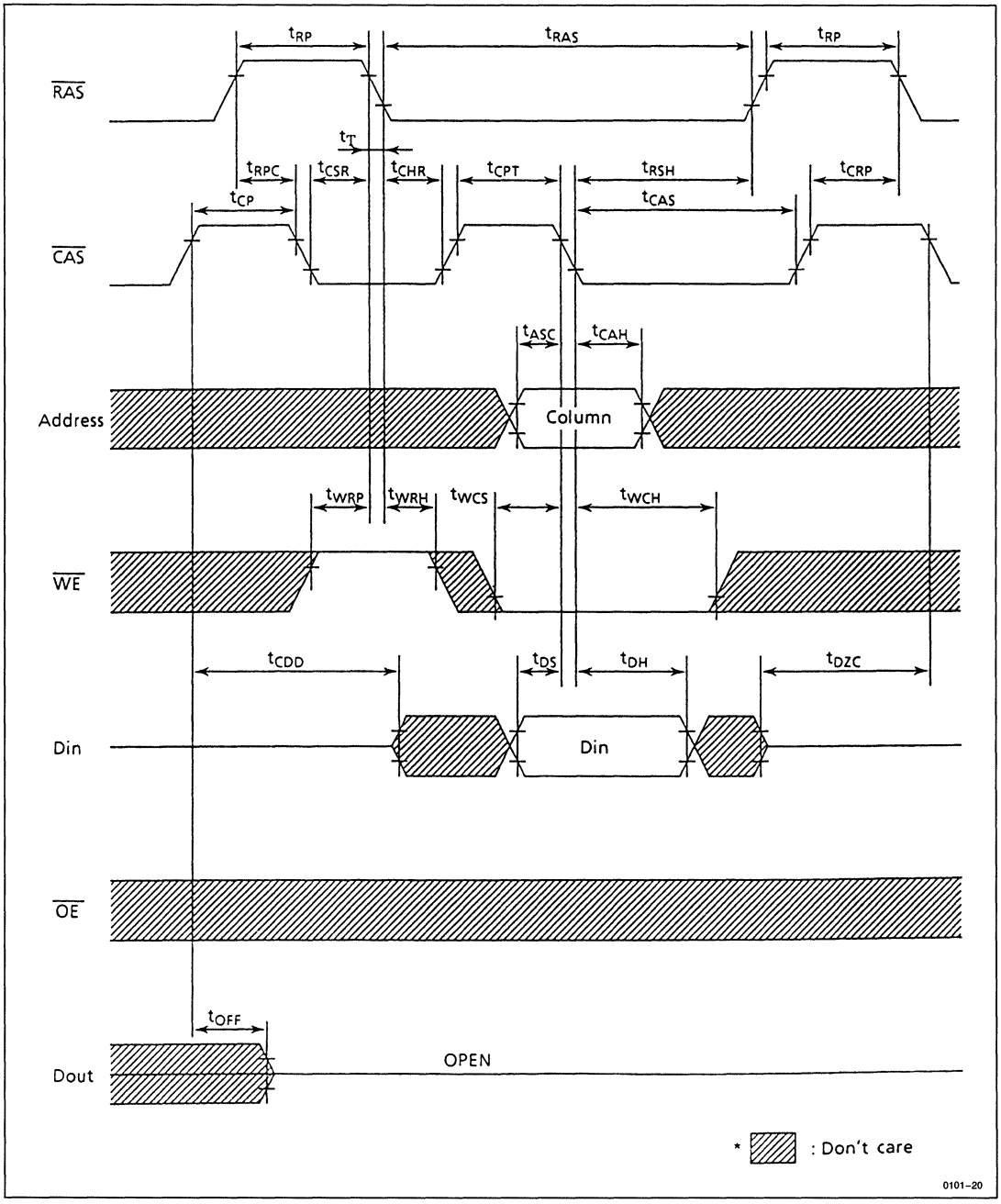
$\overline{RAS}$ Only Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM5116400L Series Low Power Version — Product Preview

4,194,304-Word x 4-Bit Dynamic Random Access Memory

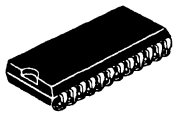
■ DESCRIPTION

The Hitachi HM5116400 is a CMOS dynamic RAM organized 4,194,304 words x 4 bits. It employs the most advanced CMOS technology for high performance and low power. The HM5116400 offers Fast Page Mode as a high speed access mode.

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode .....495 mW/440 mW/385 mW/330 mW (max)
  - Standby Mode .....11 mW (max)
- Fast Page Mode Capability
- Long Refresh Period
  - 4,096 Refresh Cycles .....(256 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Battery Back Up Operation

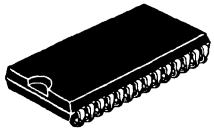
HM5116400LJ Series



3DCP24D

(CP-24D)

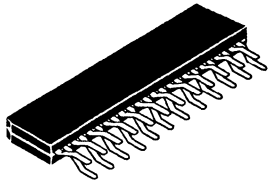
HM5116400LJ Series



3DCP28D

(CP-28D)

HM5116400LZ Series



3DZP24

(ZP-24)

■ ORDERING INFORMATION

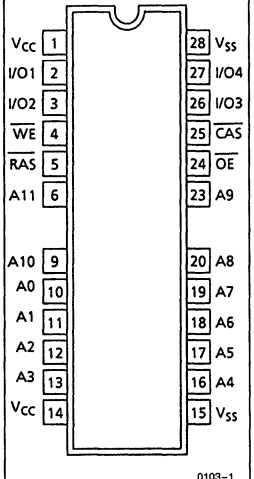
Part No.	Access Time	Package
HM5116400LJ-6 HM5116400LJ-7 HM5116400LJ-8 HM5116400LJ-10	60 ns 70 ns 80 ns 100 ns	400 mil 24-pin Plastic SOJ (CP-24D)
HM5116400LZ-6 HM5116400LZ-7 HM5116400LZ-8 HM5116400LZ-10	60 ns 70 ns 80 ns 100 ns	475 mil 24-pin Plastic ZIP (ZP-24)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{11}	Address Input
A_0–A_{11}	Refresh Address Input
I/O_0–I/O_4	Data-input/Data-output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	No Connection

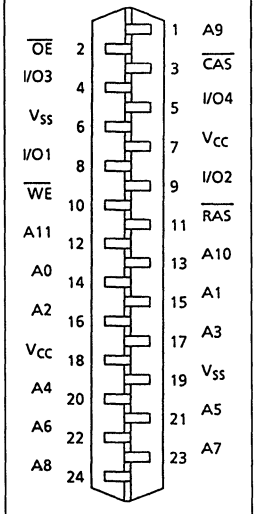
■ PIN OUT

HM5116400LJ Series



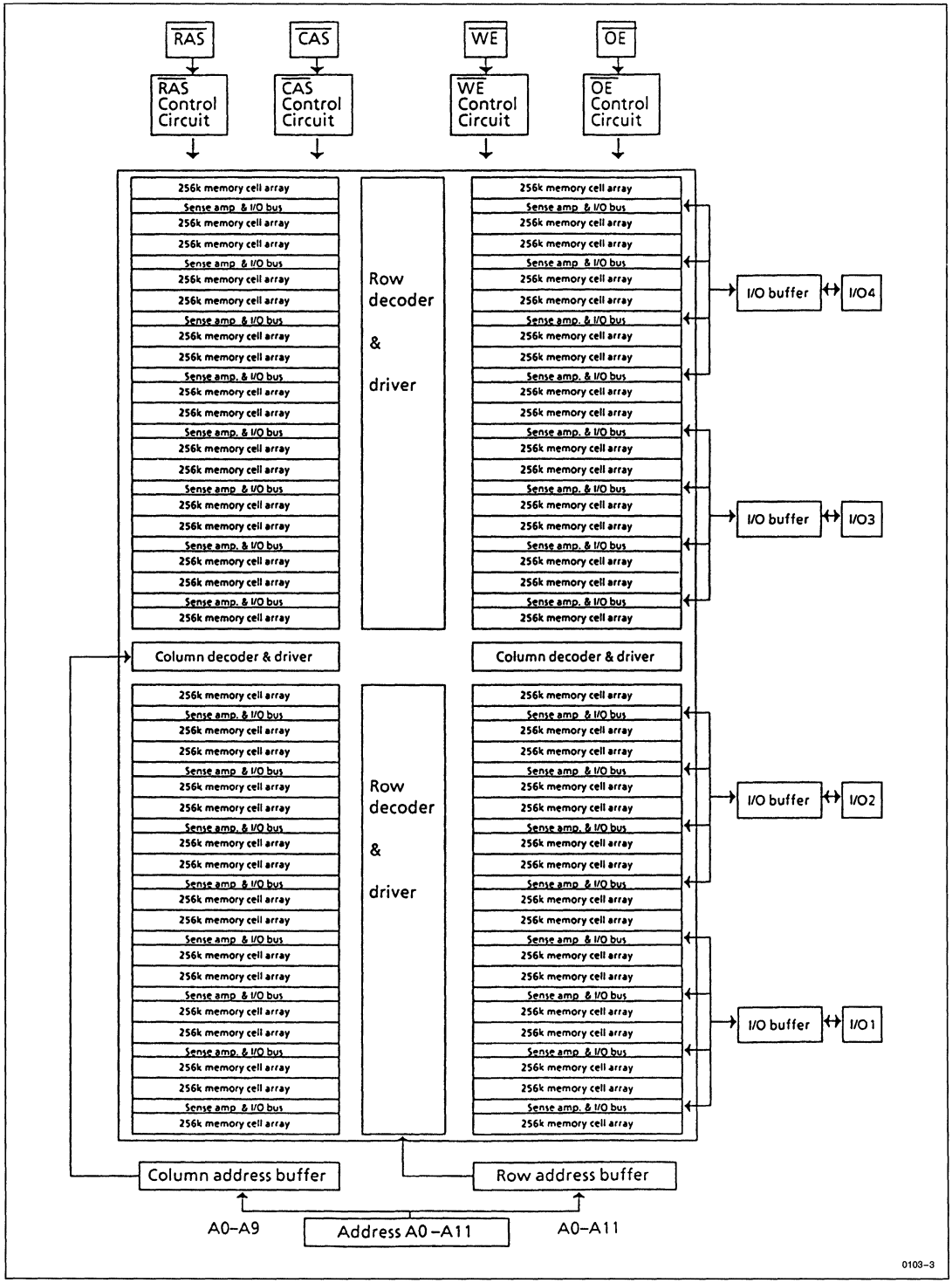
(Top View)

HM5116400LZ Series



(Bottom View)

■ BLOCK DIAGRAM



HITACHI
Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM5116400-6		HM5116400-7		HM5116400-8		HM5116400-10		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	70	—	60	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	300	—	300	—	300	—	300	μA	CMOS Interface, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ > V_{CC} − 0.2V or ≤ 6.5V Address and D_{in} = stable D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	90	—	80	—	70	—	60	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1, 4
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	90	—	80	—	70	—	60	mA	t_{RC} = Min	4
Fast Page Mode Current	I_{CC7}	—	70	—	60	—	50	—	45	mA	t_{PC} = Min	1, 3
Battery Back Up Operating Current (Standby with CBR Refresh)	I_{CC10}	—	500	—	500	—	500	—	500	μA	Standby: CMOS Interface CBR Refresh: t_{RC} = 62.5 μs t_{RAS} ≤ 1 μs Address and D_{in} = Stable D_{out} = High-Z	5
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. Clock voltages ($\overline{RAS}$ and $\overline{CAS}$) must be applied simultaneously with or prior to applying supply voltage.
5. V_{CC} − 0.2V ≤ V_{IH} ≤ 6.5V, 0V ≤ V_{IL} ≤ 0.2V.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	5	pF	1
Input Capacitance (Clocks)	C_{I2}	—	7	pF	1
Output Capacitance (Data-in, Data-out)	C_O	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 2, 3, 19, 20]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM5116400-6		HM5116400-7		HM5116400-8		HM5116400-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	70	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10000	18	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	10	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	52	20	60	20	75	ns	4
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	15	55	ns	5
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	18	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	5	—	5	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{OED}	15	—	18	—	20	—	25	—	ns	6
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	0	—	ns	7
$\overline{CAS}$ Delay Time from D_{in}	t_{DZC}	0	—	0	—	0	—	0	—	ns	7
Transition Time (Rise and Fall)	t_T	3	30	3	30	3	30	3	30	ns	8

Read Cycle

Parameter	Symbol	HM5116400-6		HM5116400-7		HM5116400-8		HM5116400-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	9, 10, 21
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	18	—	20	—	25	ns	10, 11, 21
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	ns	10, 12, 21
Access Time from $\overline{OE}$	t_{OEA}	—	15	—	18	—	20	—	25	ns	10, 21
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	ns	13
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	5	—	5	—	5	—	5	—	ns	13
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	ns	
Column Address to $\overline{CAS}$ Lead Time	t_{CAL}	30	—	35	—	40	—	45	—	ns	
$\overline{CAS}$ to Output in Low-Z	t_{CLZ}	0	—	0	—	0	—	0	—	ns	
Output Data Hold Time	t_{OH}	3	—	3	—	3	—	3	—	ns	
Output Data Hold Time from $\overline{OE}$	t_{OH0}	3	—	3	—	3	—	3	—	ns	
Output Buffer Turn-off Time	t_{OFF}	—	15	0	18	—	20	—	25	ns	14
Output Buffer Turn-off to $\overline{OE}$	t_{OEZ}	—	15	—	18	—	20	—	25	ns	14
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	15	—	18	—	20	—	25	—	ns	6

Write Cycle

Parameter	Symbol	HM5116400-6		HM5116400-7		HM5116400-8		HM5116400-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	15
Write Command Hold Time	t_{WCH}	15	—	15	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	15	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	18	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	18	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	16
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	15	—	ns	16

Read-Modify-Write Cycle

Parameter	Symbol	HM5116400-6		HM5116400-7		HM5116400-8		HM5116400-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	150	—	176	—	200	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	93	—	105	—	135	—	ns	15
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	35	—	41	—	45	—	60	—	ns	15
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	50	—	58	—	65	—	80	—	ns	15
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	15	—	18	—	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM5116400-6		HM5116400-7		HM5116400-8		HM5116400-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time (CBR Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time (CBR Refresh Cycle)	t_{CHR}	20	—	20	—	20	—	20	—	ns	
$\overline{WE}$ Setup Time (CBR Refresh Cycle)	t_{WRP}	10	—	10	—	10	—	10	—	ns	
$\overline{WE}$ Hold Time (CBR Refresh Cycle)	t_{WRH}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	—	0	—	0	—	0	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM5116400-6		HM5116400-7		HM5116400-8		HM5116400-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASP}	—	100000	—	100000	—	100000	—	100000	ns	17
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	35	—	40	—	45	—	50	ns	18, 21
$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	t_{CPW}	55	—	63	—	70	—	85	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{CPRH}	35	—	40	—	45	—	50	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM5116400-6		HM5116400-7		HM5116400-8		HM5116400-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	80	—	91	—	100	—	110	—	ns	

Test Mode Cycle

Parameter	Symbol	HM5116400-6		HM5116400-7		HM5116400-8		HM5116400-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WTS}	10	—	10	—	10	—	10	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WTH}	10	—	10	—	10	—	10	—	ns	

Counter Test Cycle

Parameter	Symbol	HM5116400-6		HM5116400-7		HM5116400-8		HM5116400-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Precharge Time in Counter Test Cycle	t_{CPT}	TBD	—	TBD	—	TBD	—	TBD	—	ns	

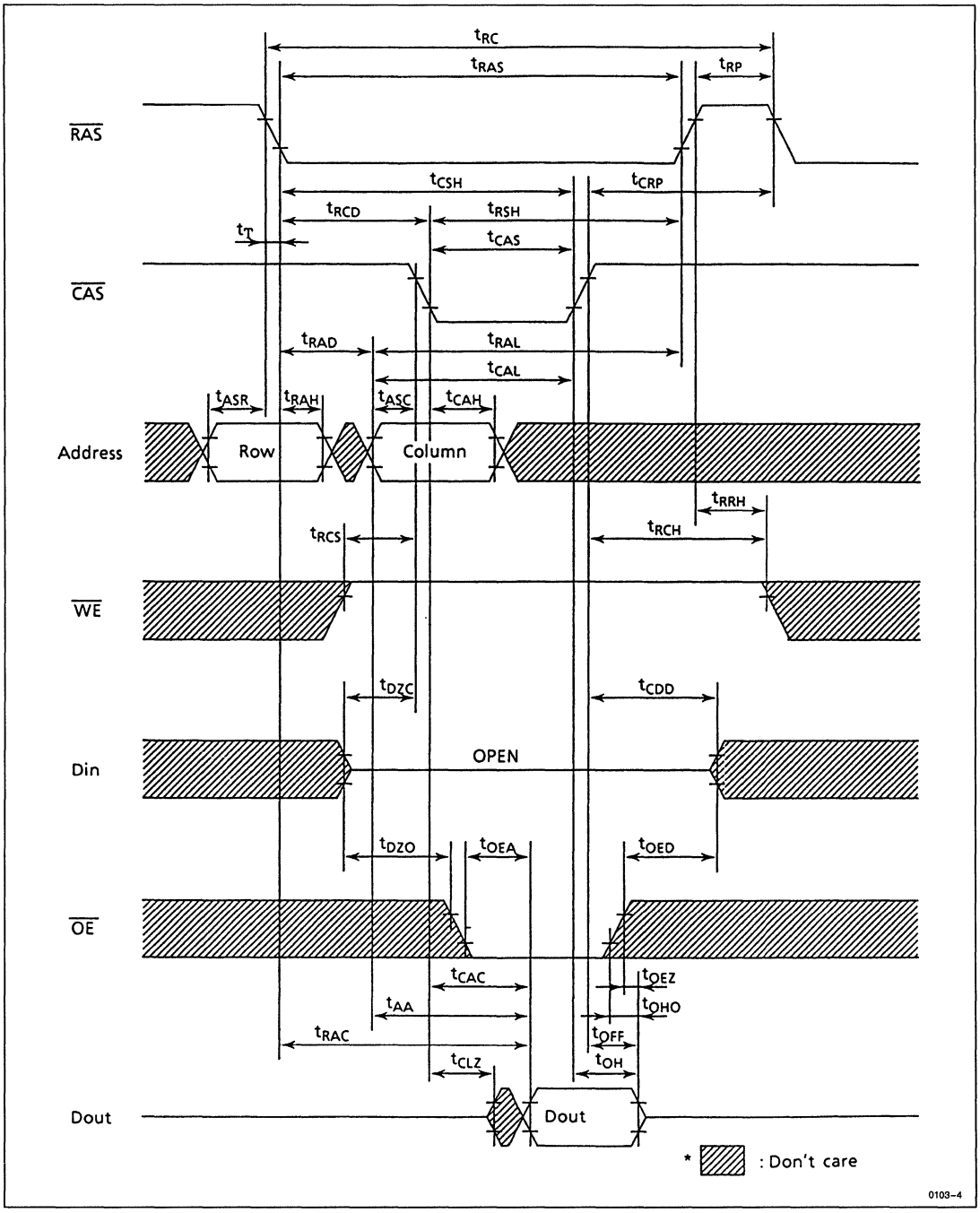
Refresh (T_J = 85°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Max	Unit	Note
Refresh Period	t_{REF}	256	ms	4096 Cycles

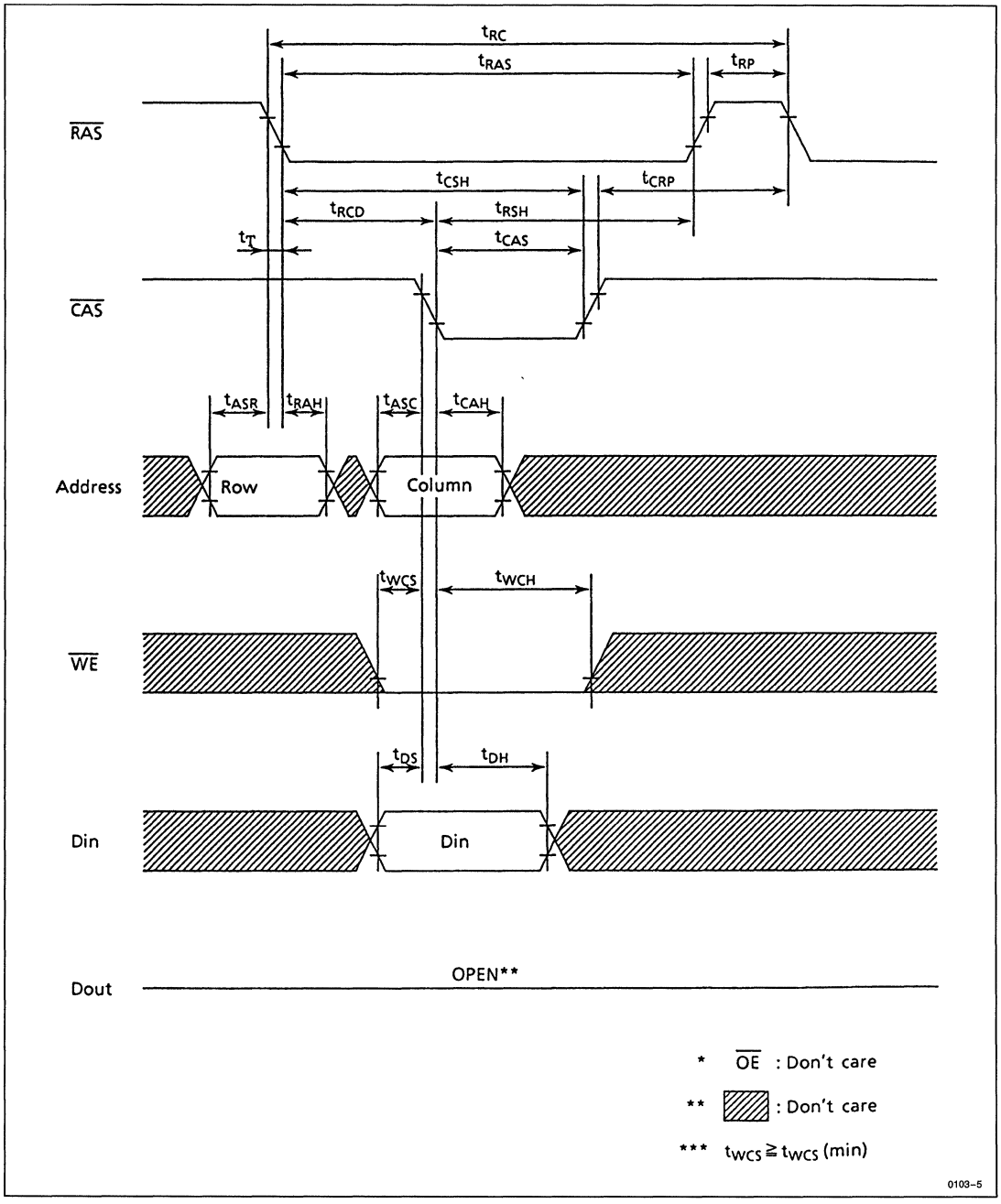
Notes:
1. AC measurements assume t_T = 5 ns.
2. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
3. Only row address is indispensable on address A10 and A11.
4. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
5. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
6. Either t_{ODD} or T_{CDD} must be satisfied.
7. Either t_{DZO} or T_{DZC} must be satisfied.
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
9. Assumes that $t_{RCD} < t_{RCD}$ (max) and $t_{RAD} < t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
10. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
12. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
13. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
14. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min) the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
16. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
17. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
18. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
19. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
20. Test mode operation specified in this data sheet is 16 bits test function controlled by compression addresses — CA0 and CA1. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of four test bits on each I/O accord with each other, the state of the output data on the I/O is high level. When the state of four test bits on the I/O do not accord with each other, the state of the output data on the I/O is low level. Data input and output pins are I/O-1 to I/O-4. If any refresh cycle is occurred, the test mode is reset.
21. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{CPA} is delayed by 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORMS

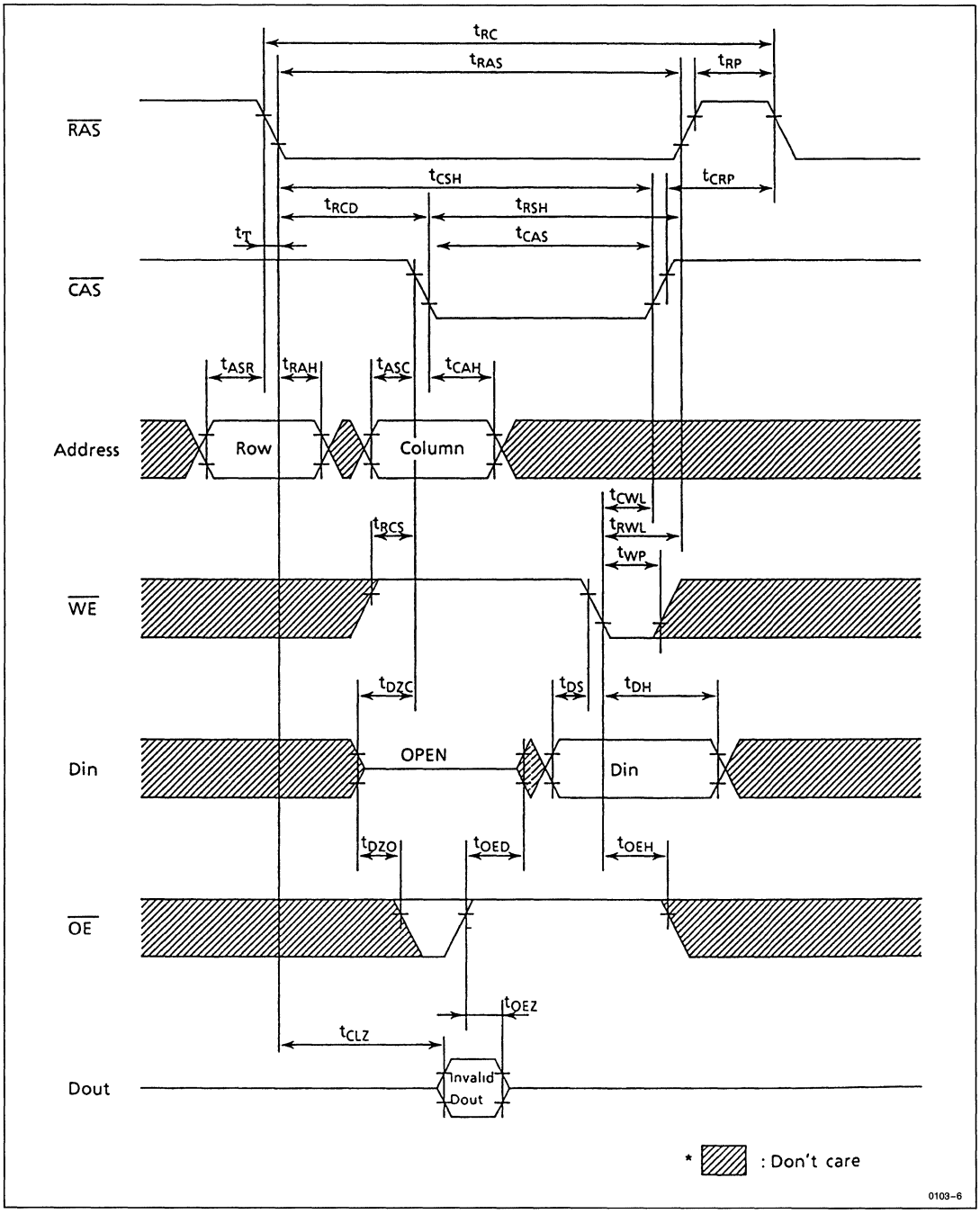
• Read Cycle



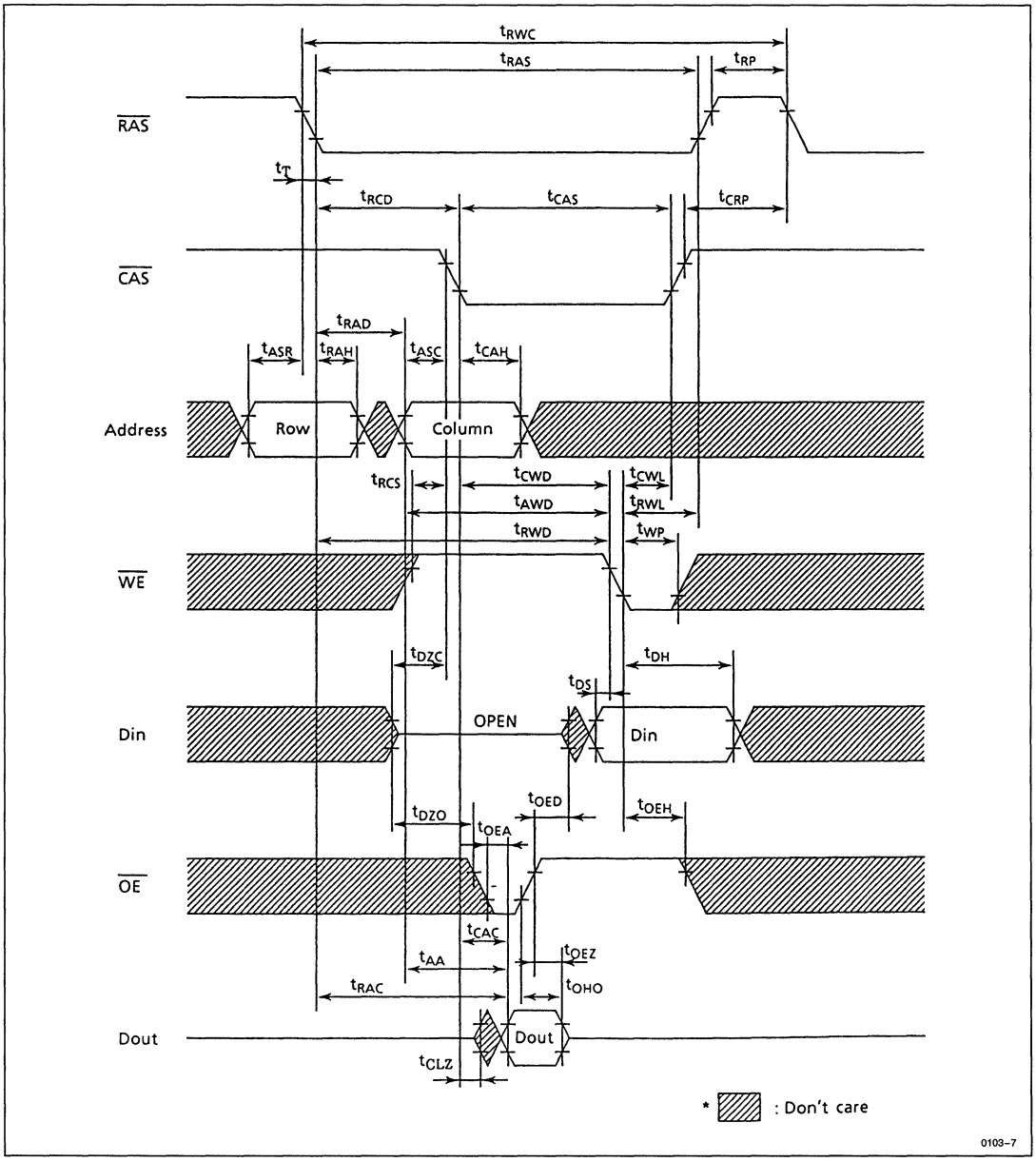
• **Early Write Cycle**



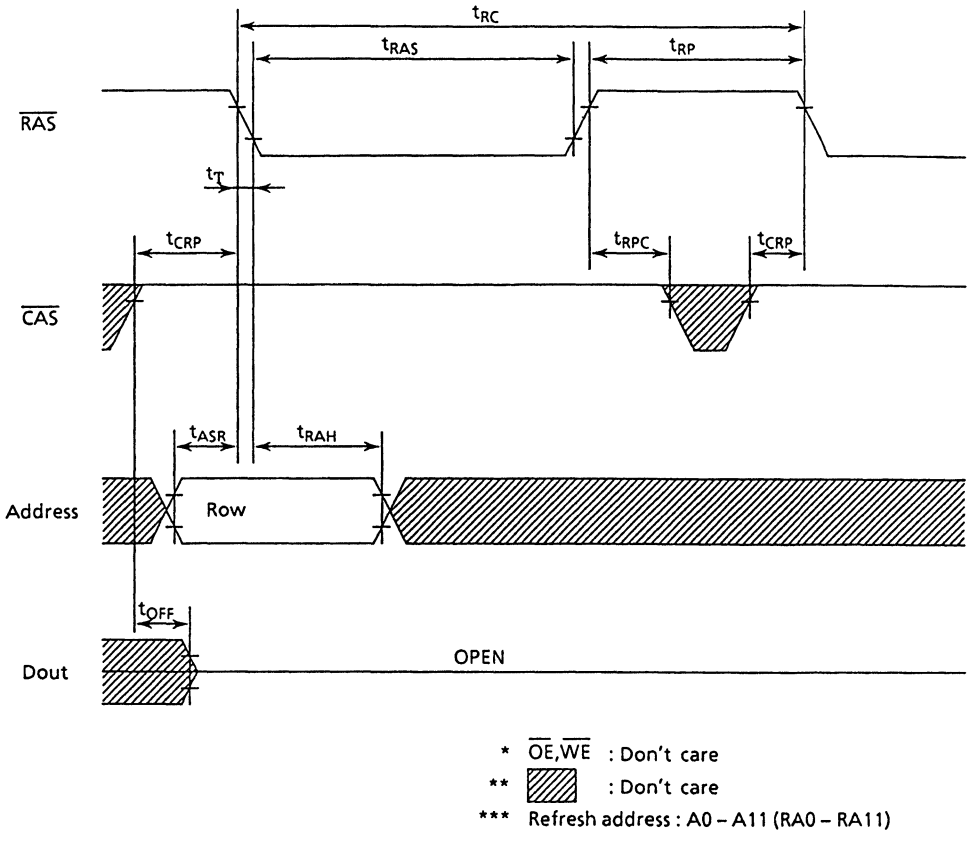
• **Delayed Write Cycle**



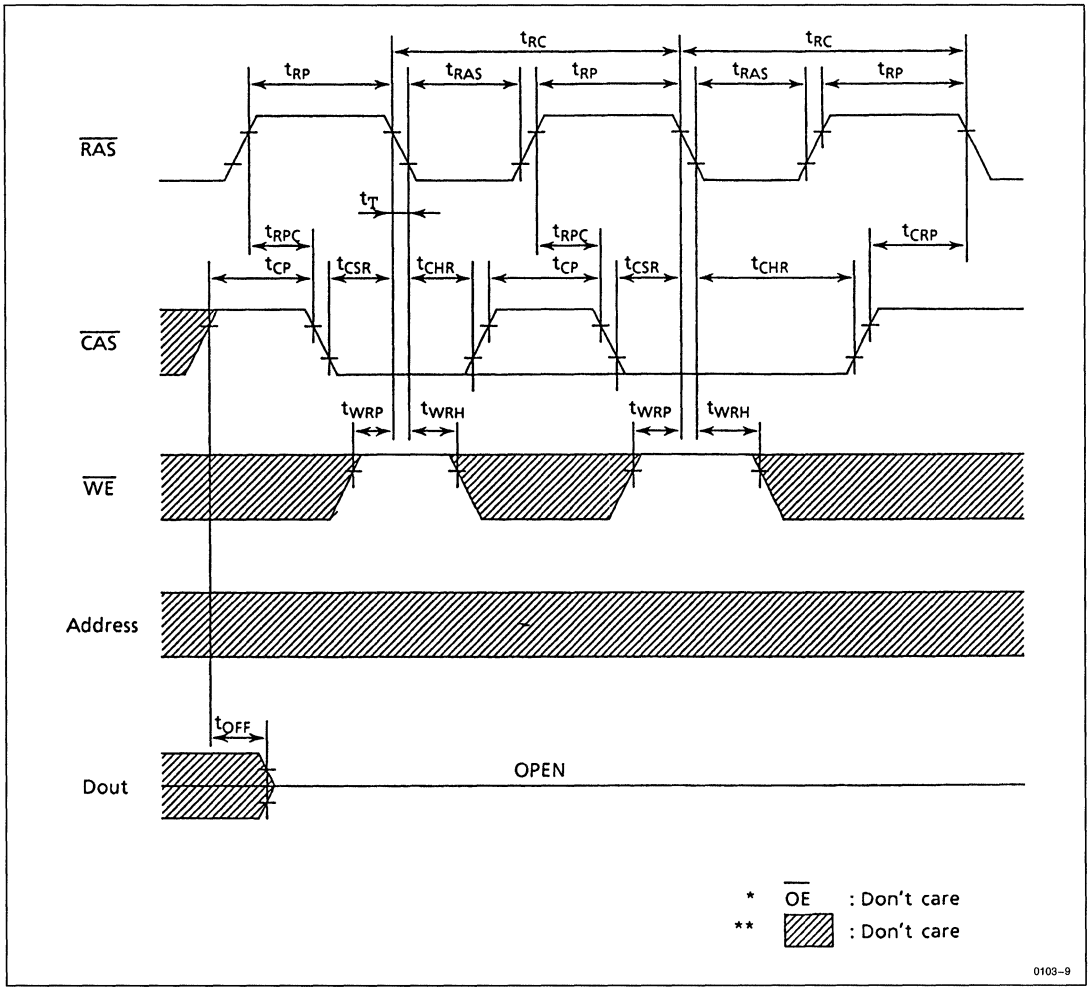
• **Read-Modify-Write Cycle**



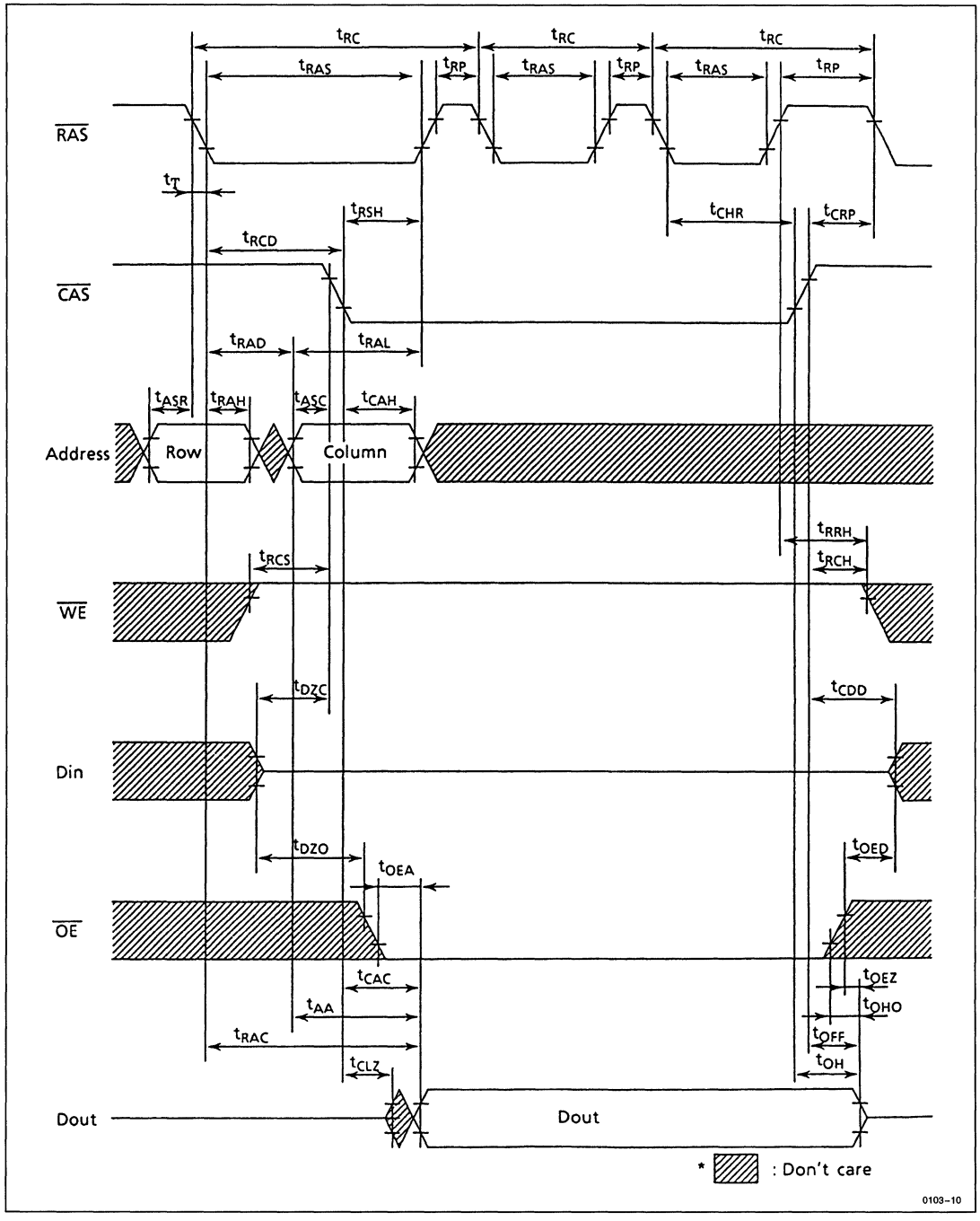
• $\overline{RAS}$ Only Refresh Cycle



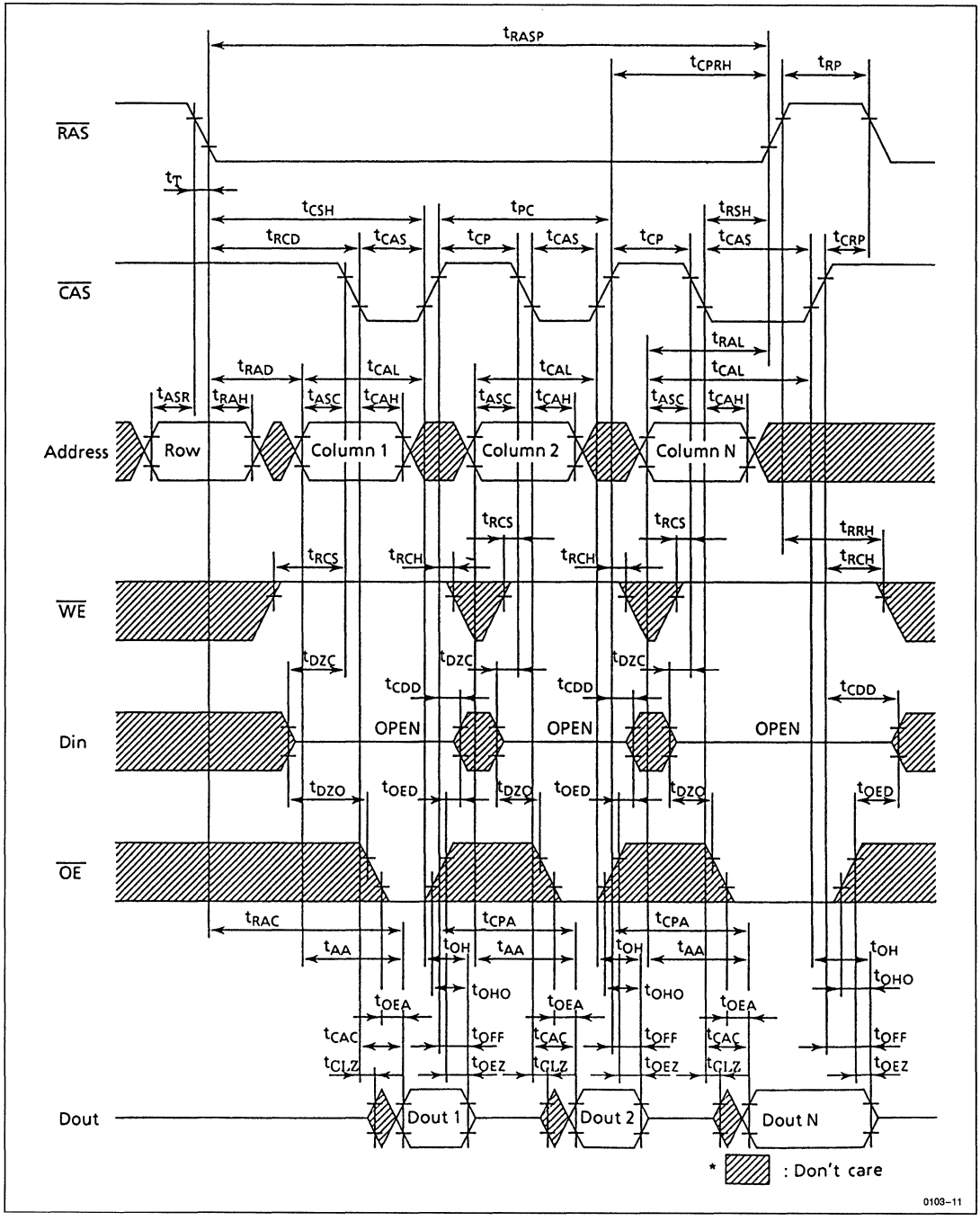
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



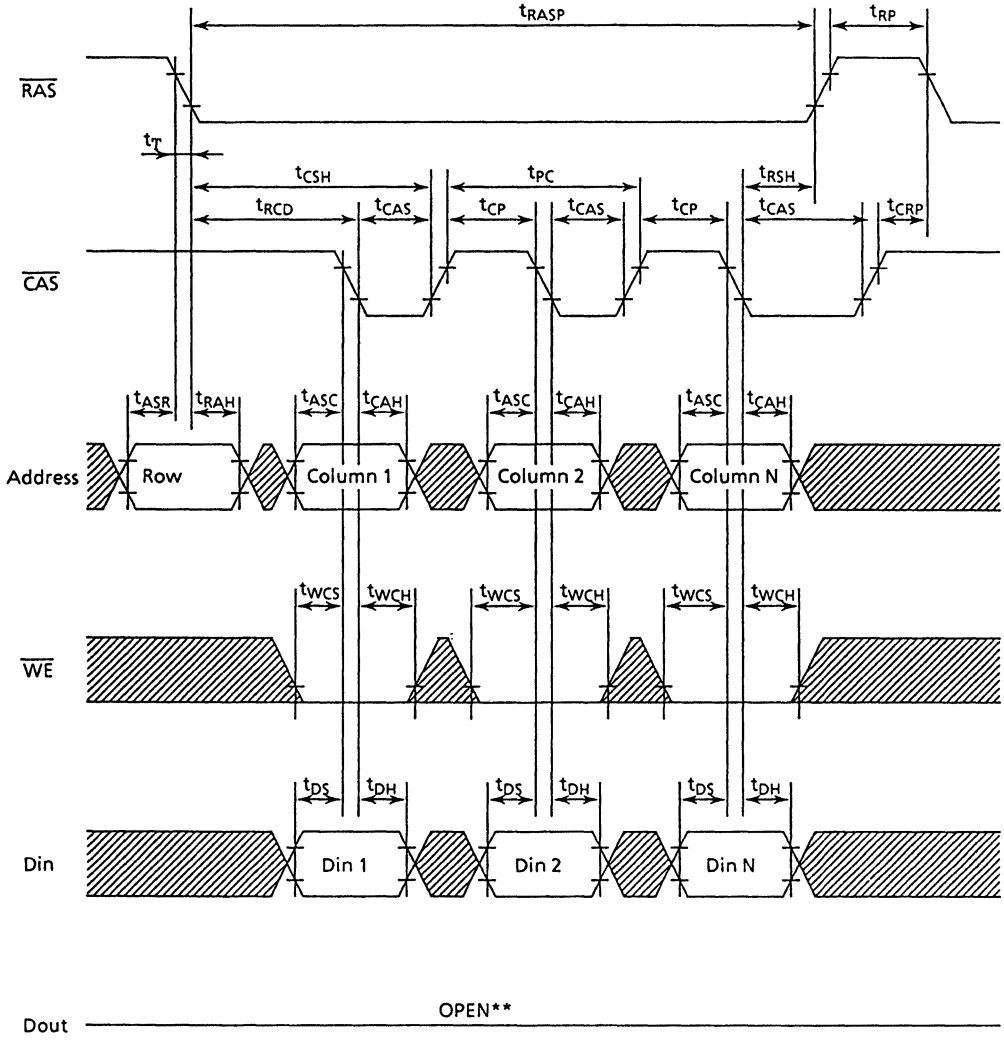
• **Hidden Refresh Cycle**



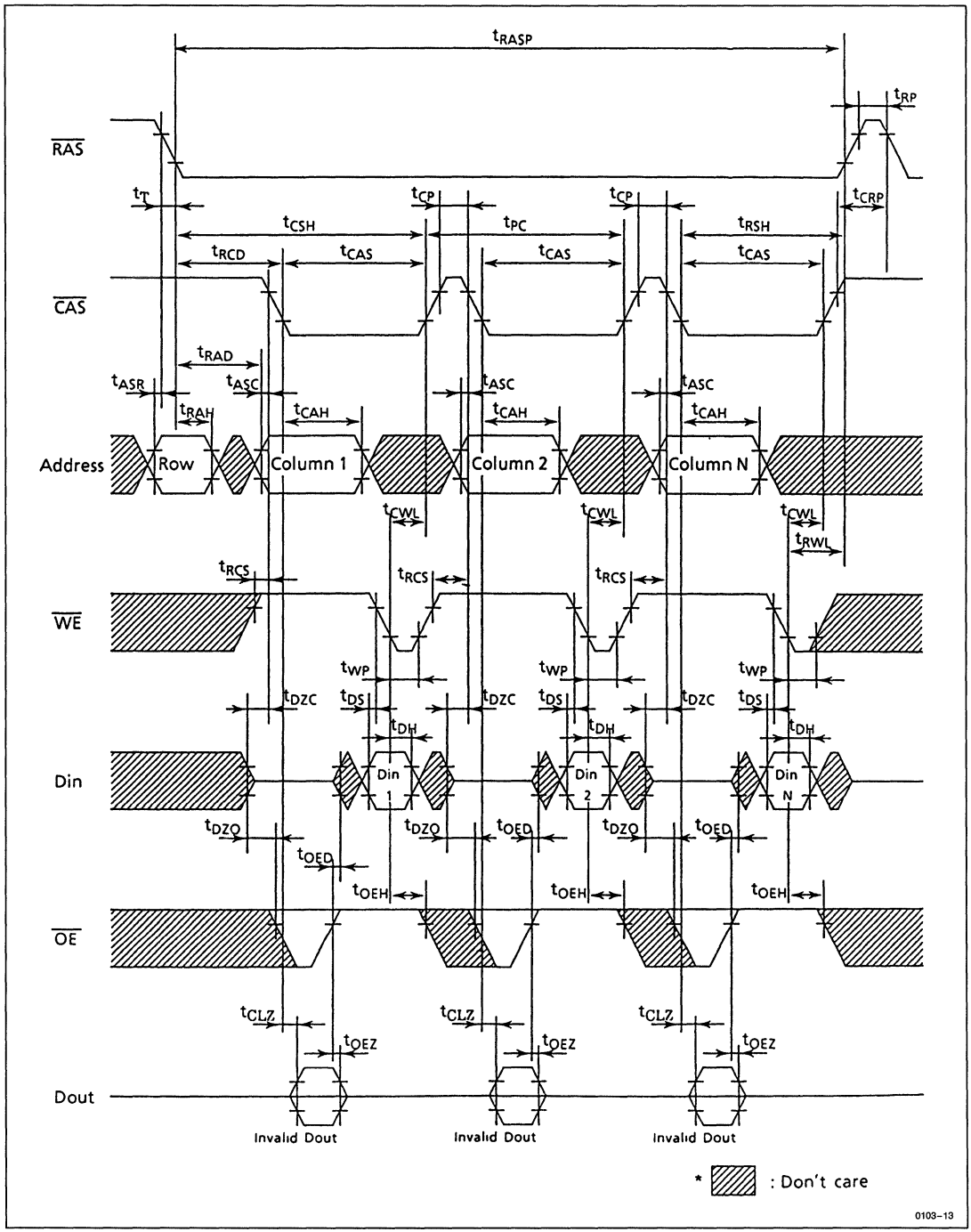
• **Fast Page Mode Read Cycle**



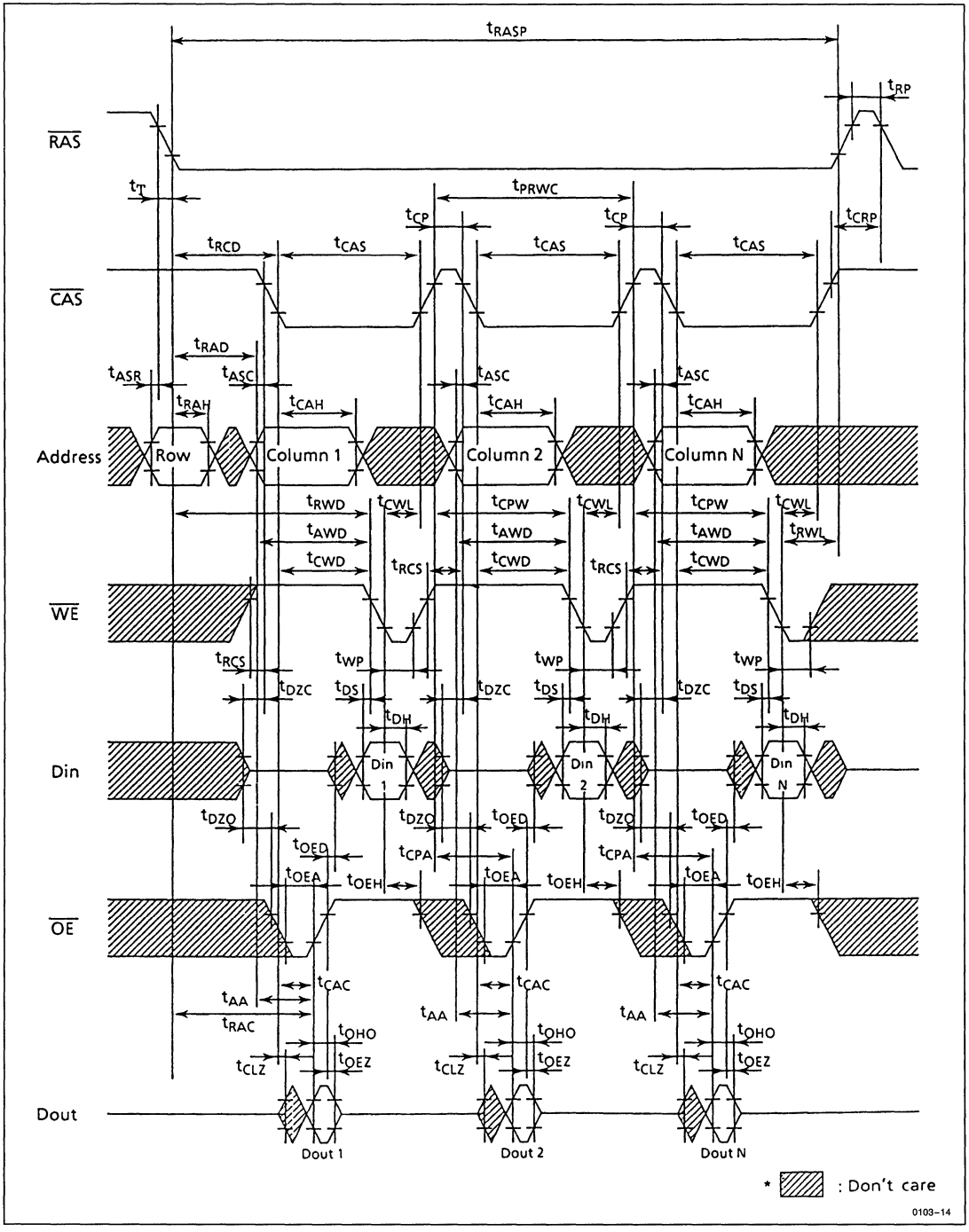
• **Fast Page Mode Early Write Cycle**



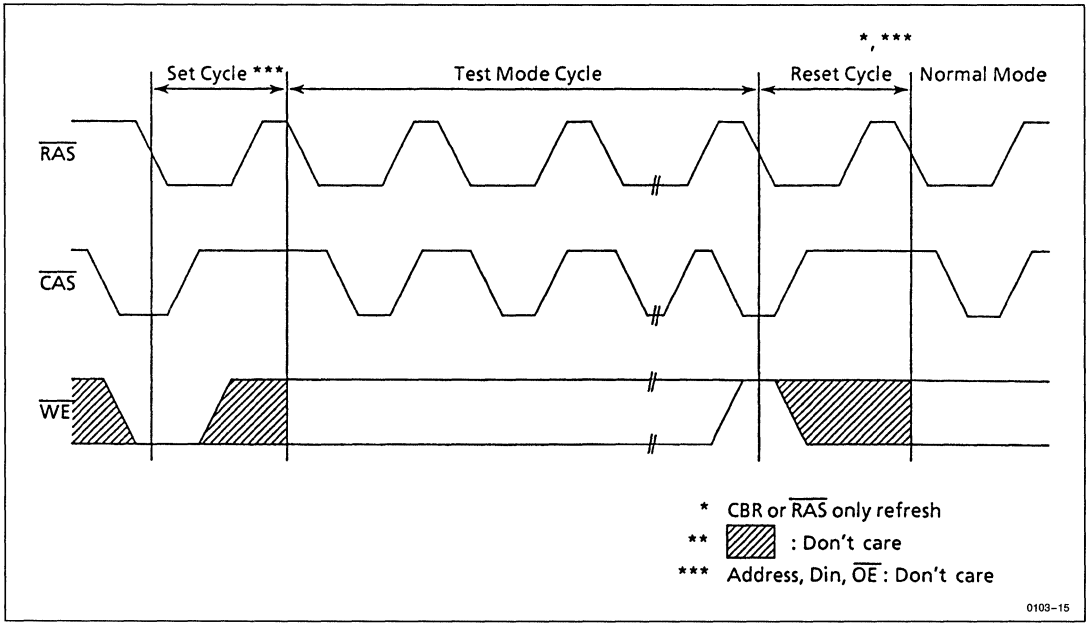
• **Fast Page Mode Delayed Write Cycle**



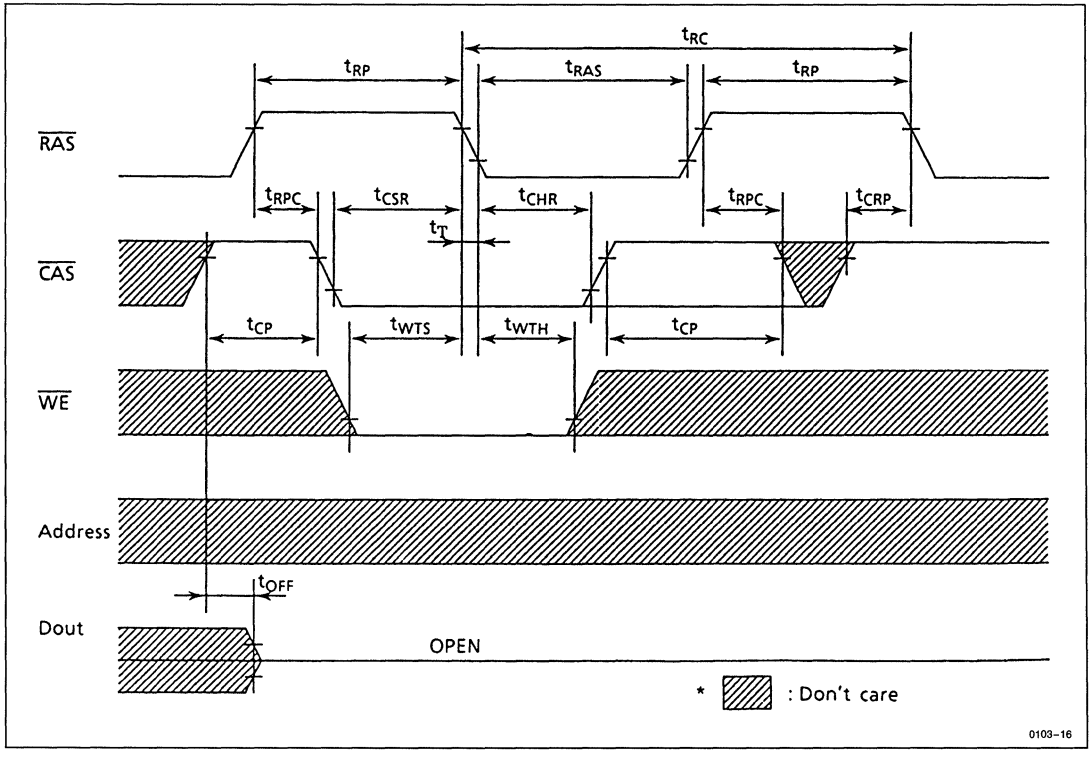
• **Fast Page Mode Read-Modify-Write Cycle**



• **Test Mode Cycle**

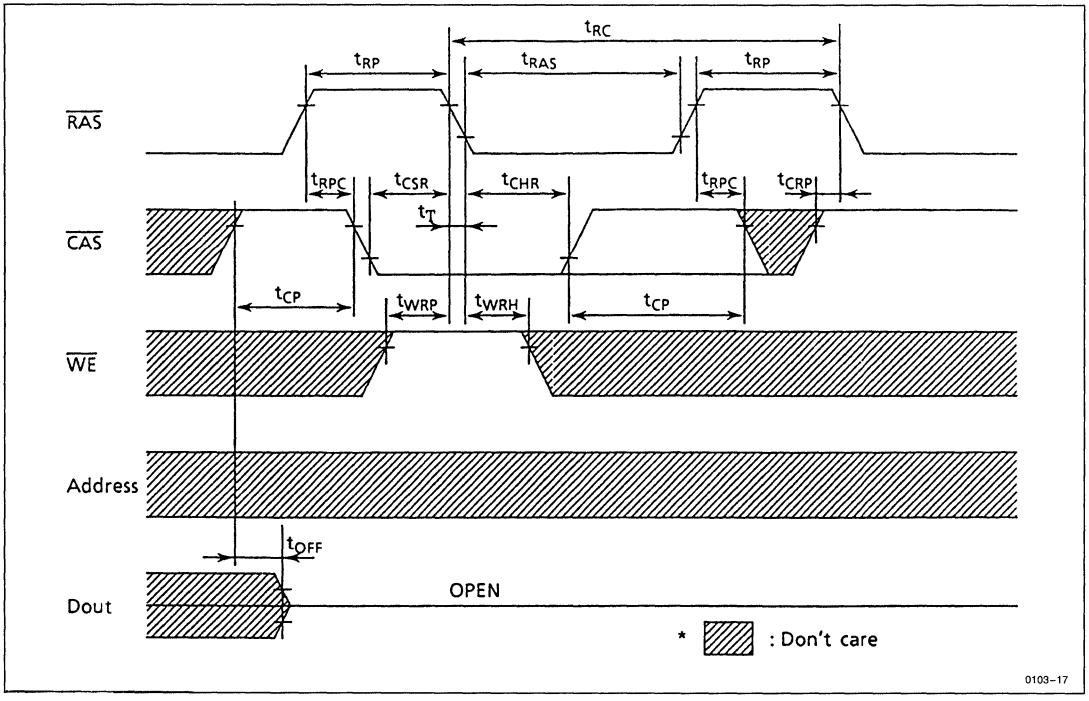


• **Test Mode Set Cycle**

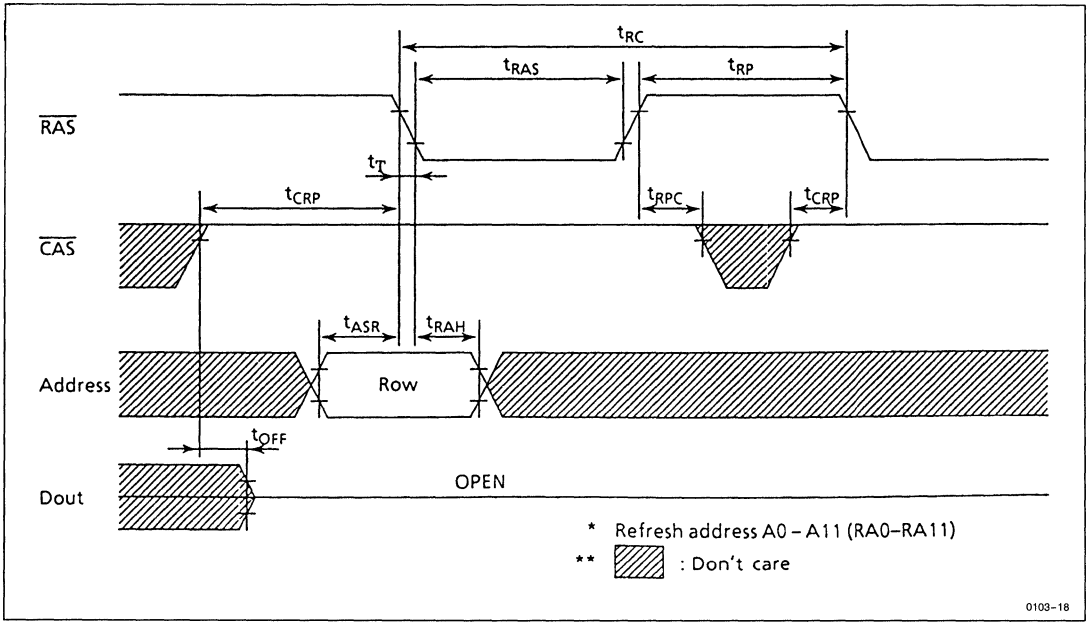


• **Test Mode Reset Cycle**

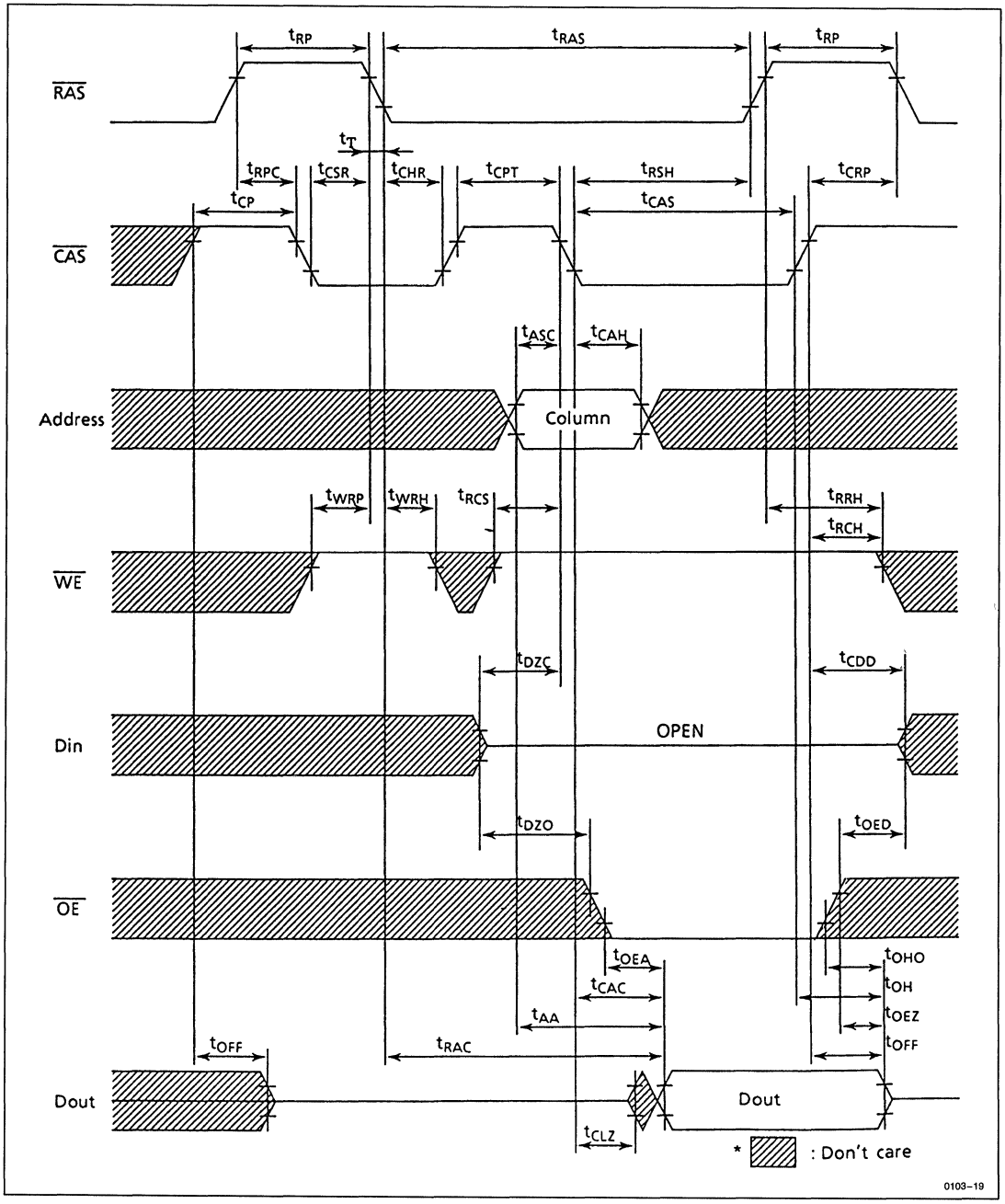
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Cycle



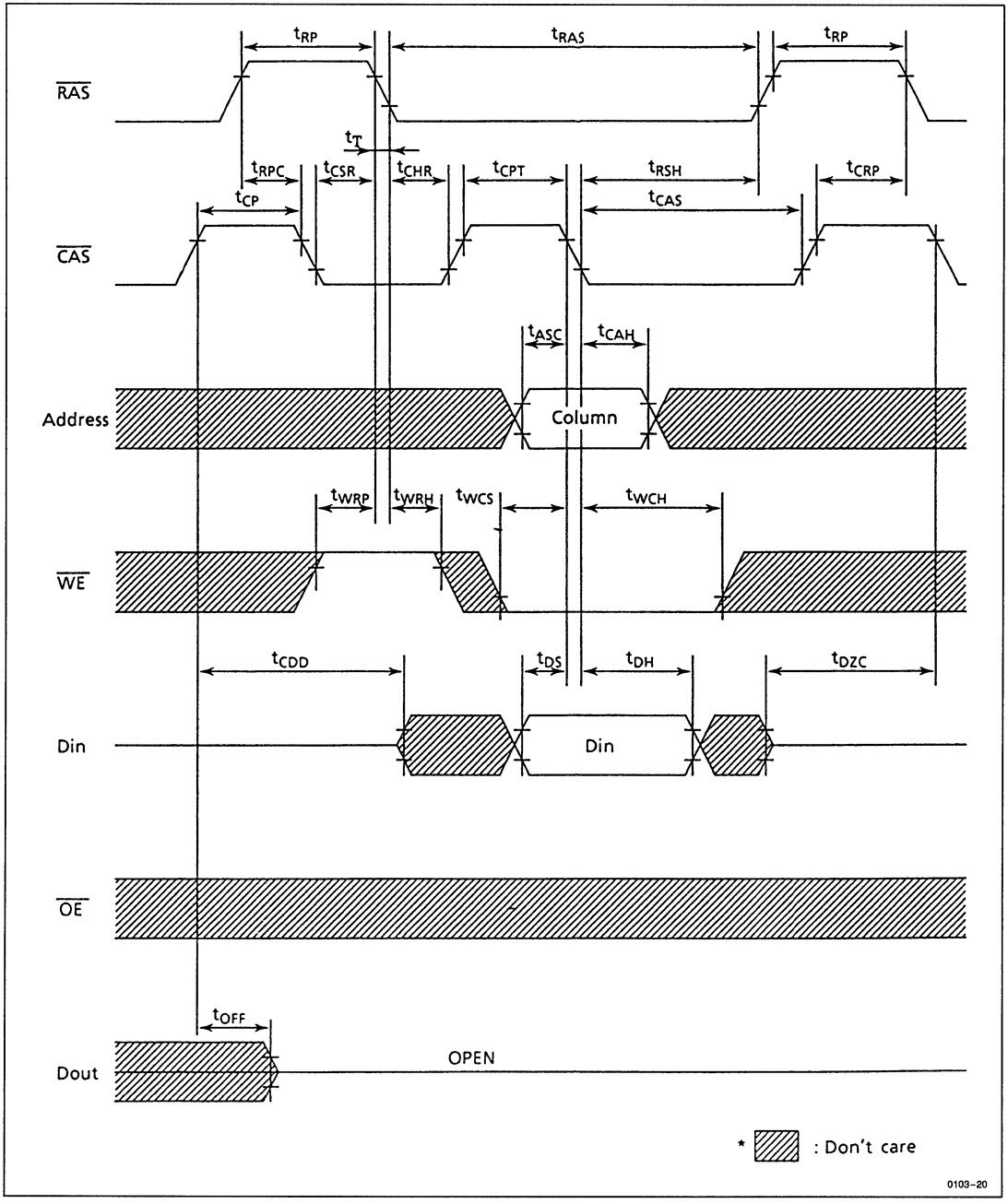
• **$\overline{RAS}$ Only Refresh Cycle**



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Read)



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Check Cycle (Write)



Section 3
High Speed BiCMOS Dynamic RAM

3

HITACHI®

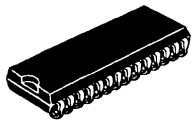
HM571000 Series

1,048,576-Word x 1-Bit High Speed Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM571000 is a super high speed dynamic RAM organized 1,048,576-word x 1-bit. HM571000 have realized higher density, higher performance and various functions by employing 1.3 μm Bi-CMOS technology and some new Bi-CMOS circuit design technologies. The HM571000 offers 8 bits static column mode as a high speed access mode.

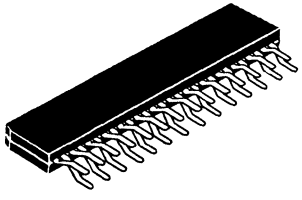
HM571000JP Series



3DCP28DN

(CP-28DN)

HM571000ZP Series



3DZP28

(ZP-28)

■ FEATURES

- Single
  - 5V (±10%) for HM571000JP/ZP-40/45
  - 5V (±5%) for HM571000JP/ZP-35R
- High Speed
  - Access Time .....35 ns/40 ns/45 ns (max)
- 512 Refresh Cycles .....(4 ms)
- 2 Variations of Refresh
  - $\overline{CE}$ Refresh
  - Automatic Refresh
- 8 Bits Static Column Mode

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM571000JP-35R HM571000JP-40 HM571000JP-45	35 ns 40 ns 45 ns	300 mil 28-pin Plastic SOJ (CP-28DN)
HM571000ZP-35*1 HM571000ZP-40*1 HM571000ZP-45*1	35 ns 40 ns 45 ns	400 mil 28-pin Plastic ZIP (ZP-28)

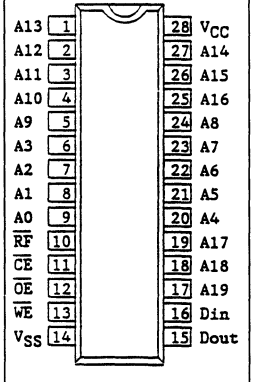
Note: *1. ZIP type products are preliminary.

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input for $\overline{CE}$ Refresh
A_9–A_{16}	Address Input
A_{17}–A_{19}	Address Input for Static Column Mode
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Read/Write Enable
D_{in}	Data-in
D_{out}	Data-out
$\overline{RF}$	Refresh Control
V_{CC}	Power (+5V)
V_{SS}	Ground

■ PIN OUT

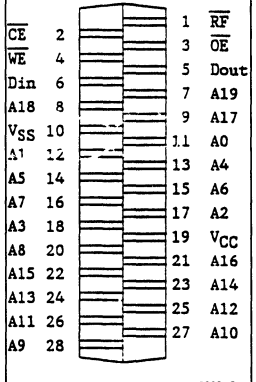
HM571000JP Series



0080-1

(Top View)

HM571000ZP Series



0080-2

(Bottom View)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_T	0.8	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	-35R	V_{CC}	4.75	5.0	5.25	V	1
	-40/-45		4.50		5.50		
Input High Voltage		V_{IH}	2.4	—	6.5	V	1, 3
Input Low Voltage		V_{IL}	− 1.0	—	0.8	V	1, 2

Notes: 1. All voltage referenced to V_{SS}.
2. The device will withstand undershoots to the − 2V level with a maximum pulse width of 20 ns at the − 1.5V level. (See Figure 1.)

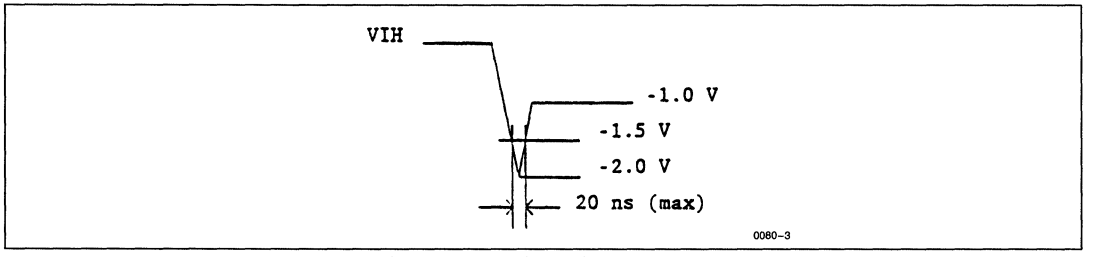


Figure 1. Undershoot of Input Voltage

3. The V_{IH} level of $\overline{OE}$ shall be lower than V_{CC} + 0.5V.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{SS} = 0V)
(V_{CC} = 5V ± 10% for HM571000JP-40/45)
(V_{CC} = 5V ± 5% for HM571000JP-35R)

Parameter	Symbol	HM571000-35R		HM571000-40		HM571000-45		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Normal Operating Current	I_{CCA}	See Figure 2						mA		1
Refresh Current	I_{CCR}	See Figure 2						mA		1
Standby Current	I_{CCS}	—	5	—	5	—	5	mA		
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	µA	$0V < V_{in} < 7V$	2
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	µA	$0V < V_{out} < 7V$, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 4 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 8 mA	

Notes: 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.
2. The V_{IN} level of $\overline{OE}$ that is I_{LI} test condition of $\overline{OE}$ must be lower than V_{CC} + 0.5V.

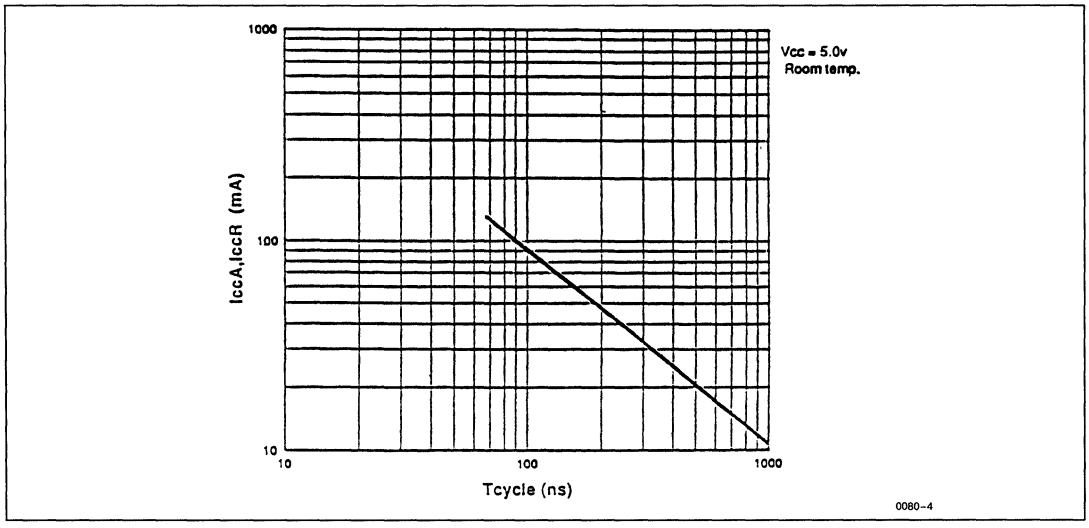


Figure 2. I_{CCA}, I_{CCR} vs T_{cycle}

• **Capacitance** (T_A = 25°C)
(V_{CC} = 5V ±10% for HM571000JP-40/45)
(V_{CC} = 5V ± 5% for HM571000JP-35R)

Parameter		Symbol	Typ	Max	Unit	Note
Input Capacitance	Address, Data-in	C_{in1}	—	5	pF	1
	Clocks ($\overline{CE}$, $\overline{OE}$)	C_{in2}	—	5	pF	1
	Clock ($\overline{WE}$, $\overline{RF}$)	C_{in3}	—	7	pF	1
Output Capacitance	(Data-out)	C_O	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{OE}$, $\overline{CE}$ = V_{IH} to disable D_{out}.

• **AC CHARACTERISTICS** [1] (T_A = 0 to +70°C, V_{SS} = 0V)
(V_{CC} = 5V ±10% for HM571000JP/40/45)
(V_{CC} = 5V ±5% for HM571000JP/35R)

Test Conditions
Input Pulse Levels: V_{IH} = 3.0V, V_{IL} = 0V
Transition Time: t_T = 3 ns
Input Timing Reference Levels: High = 2.4V, Low = 0.8V (See Figure 3.)
Output Timing Reference Levels: High = 2.4V, Low = 0.4V
Output Load: See Figure 4.

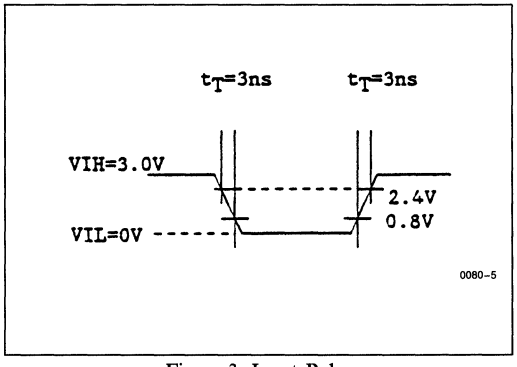


Figure 3. Input Pulse

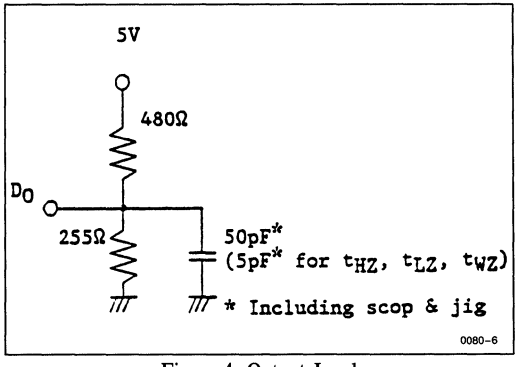


Figure 4. Output Load

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM571000-35R		HM571000-40		HM571000-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read/Write Cycle Time	t_{CC}	75	—	85	—	90	—	ns	
$\overline{CE}$ Pulse Width	t_{CE}	35	5000	40	5000	45	5000	ns	
$\overline{CE}$ Precharge Time	t_{CP}	34	—	39	—	39	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Address Hold Time	t_{AH}	5	—	5	—	5	—	ns	
Transition Time (Rise and Fall)	t_T	1	10	1	10	1	10	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	

Read Cycle

Parameter	Symbol	HM571000-35R		HM571000-40		HM571000-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{CE}$	t_{ACS}	—	35	—	40	—	45	ns	
Address Access Time	t_{AA}	—	25	—	30	—	30	ns	
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	25	—	25	ns	
Setup Time on Read	t_{RS}	0	—	0	—	0	—	ns	
Hold Time on Read	t_{RH}	5	—	5	—	5	—	ns	
$\overline{OE}$ Setup Time	t_{OES}	5	—	5	—	5	—	ns	
$\overline{OE}$ Enable to Output in Low-Z	t_{LZ}	0	—	0	—	0	—	ns	
$\overline{OE}$ Disable to Output in High-Z	t_{HZ}	—	15	—	20	—	20	ns	
Output Hold Time from Address	t_{AOH}	3	—	3	—	3	—	ns	
Output Hold Time from $\overline{CE}$	t_{COH}	0	—	0	—	0	—	ns	
$\overline{CE}$ to $\overline{OE}$ Precharge Time	t_{COP}	10	—	10	—	10	—	ns	

Write Cycle

Parameter	Symbol	HM571000-35R		HM571000-40		HM571000-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Data Setup Time	t_{DW}	20	—	25	—	30	—	ns	
Data Hold Time	t_{DH}	5	—	5	—	5	—	ns	
Setup Time on Early Write	t_{ES}	5	—	5	—	5	—	ns	
$\overline{WE}$ Pulse Width	t_{WP}	25	—	30	—	35	—	ns	
Write Hold Time from $\overline{CE}$	t_{WH}	35	—	40	—	45	—	ns	
$\overline{WE}$ Enable to Output in High-Z	t_{WZ}	—	15	—	20	—	20	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM571000-35R		HM571000-40		HM571000-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{WE}$ Delay Time from $\overline{CE}$	t_{CWD}	35	—	40	—	45	—	ns	

Refresh Cycle

Parameter	Symbol	HM571000-35R		HM571000-40		HM571000-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{RF}$ Setup Time	t_{FS}	5	—	5	—	5	—	ns	
$\overline{RF}$ Hold Time	t_{FH}	15	—	15	—	15	—	ns	
Mode Selection Setup Time	t_{MS}	0	—	0	—	0	—	ns	
Mode Selection Hold Time	t_{MH}	15	—	20	—	20	—	ns	
Setup Time on $\overline{CE}$ Refresh	t_{CRS}	15	—	20	—	20	—	ns	

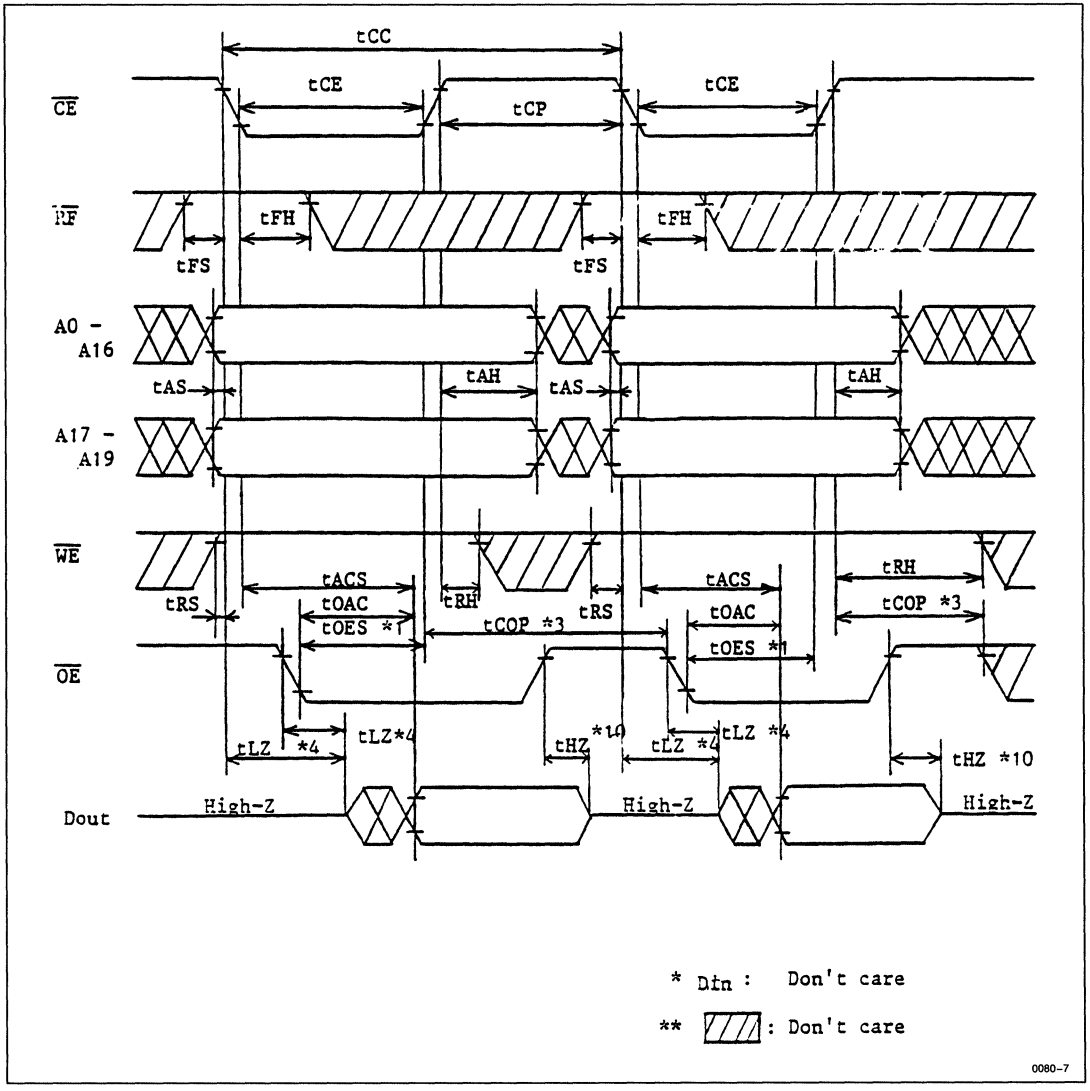
Static Column Mode Cycle

Parameter	Symbol	HM571000-35R		HM571000-40		HM571000-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Static Column Address Setup Time	t_{ASZ}	20	—	25	—	25	—	ns	
Address Setup Time to $\overline{WE}$	t_{WS}	0	—	0	—	0	—	ns	
Address Hold Time from $\overline{WE}$	t_{WR}	0	—	0	—	0	—	ns	

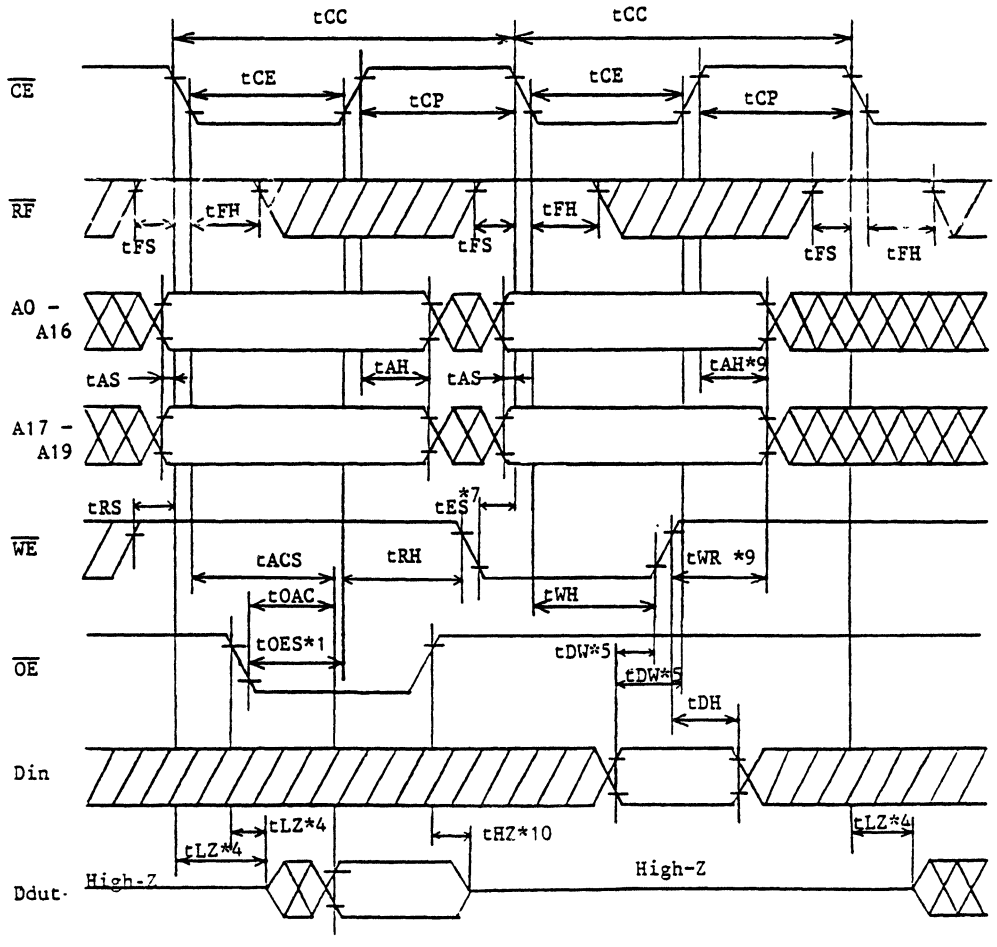
Notes:
1. If $t_{OES} > t_{OES}$ (min) and $\overline{OE}$ is held at low level, D_{out} will be valid until the next negative transition of $\overline{CE}$.
2. Both t_{WH} and t_{WP} must be satisified for a delayed write cycle.
3. If $t_{COP} < t_{COP}$ (min), D_{out} cannot be guaranteed to be in high impedance.
4. If the negative transition of $\overline{OE}$ occurs before that of $\overline{CE}$, t_{LZ} is controlled by $\overline{CE}$.
5. t_{WP} and t_{DW} are specified by the positive transition of $\overline{CE}$ or $\overline{WE}$ whichever occurs earlier.
6. When $\overline{WE}$ goes low, D_{out} becomes high impedance and is held in this condition to the next cycle. If the negative transition of $\overline{WE}$ occurs before that of $\overline{CE}$, D_{out} is controlled by $\overline{CE}$. t_{WZ} defines the time at which the output achieves the open circuit condition.
7. If $t_{ES} > t_{ES}$ (min), the cycle is early write and D_{out} is in high impedance.
8. In static column mode cycles, read operation cannot be performed after write operation.
9. Both t_{AH} and t_{WR} must be satisified for a write cycle.
10. t_{HZ} defines the time at which the output achieves the open circuit condition.
11. An initial pause of 100 μS is required after power-up, then execute at least eight $\overline{CE}$ refresh cycles.
12. In static column mode cycle, there must not be any invalid address inputs for static column mode (A_{17}–A_{19}) which are less than t_{AA}.

■ TIMING WAVEFORMS

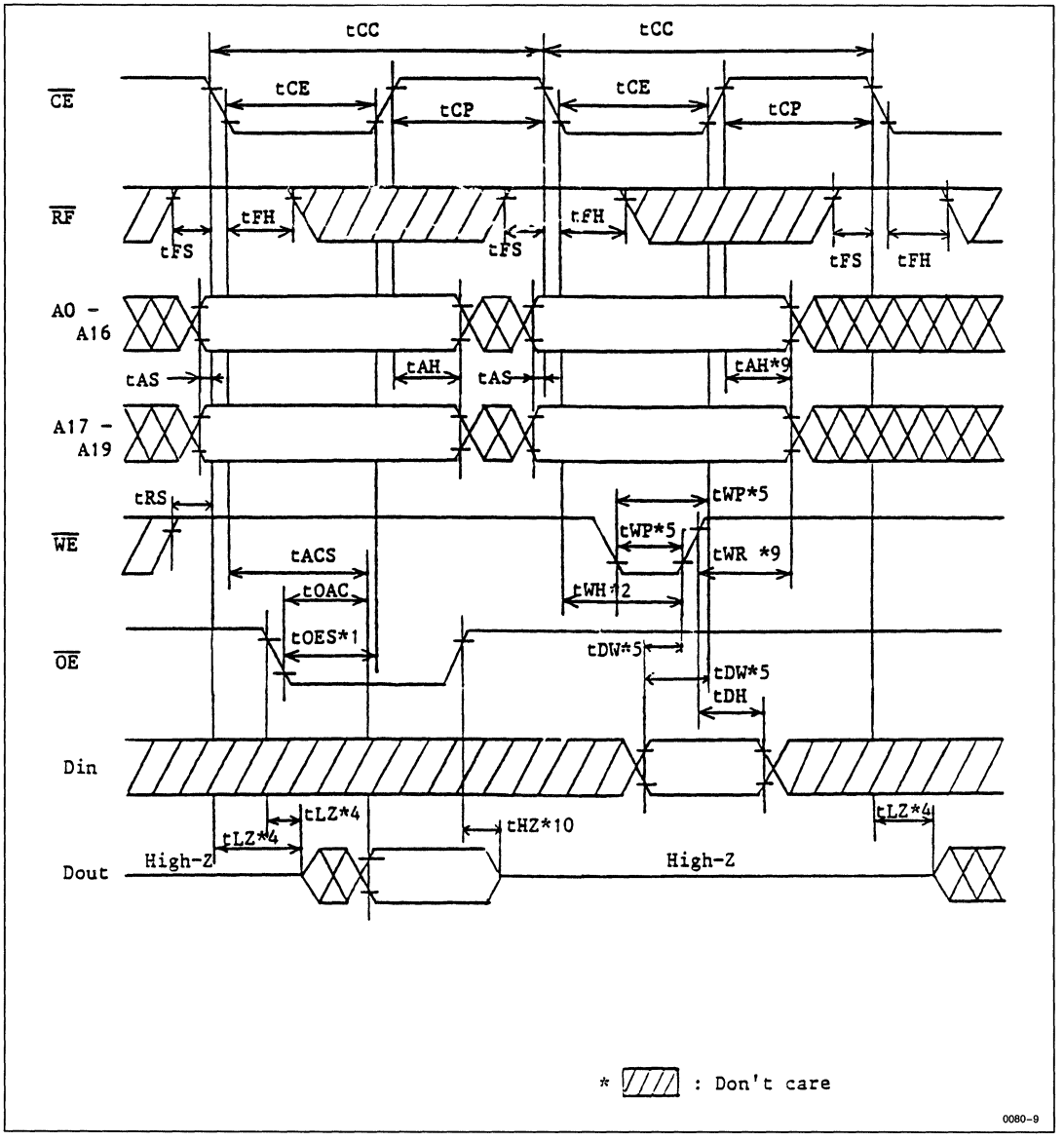
• Read/Read Cycle



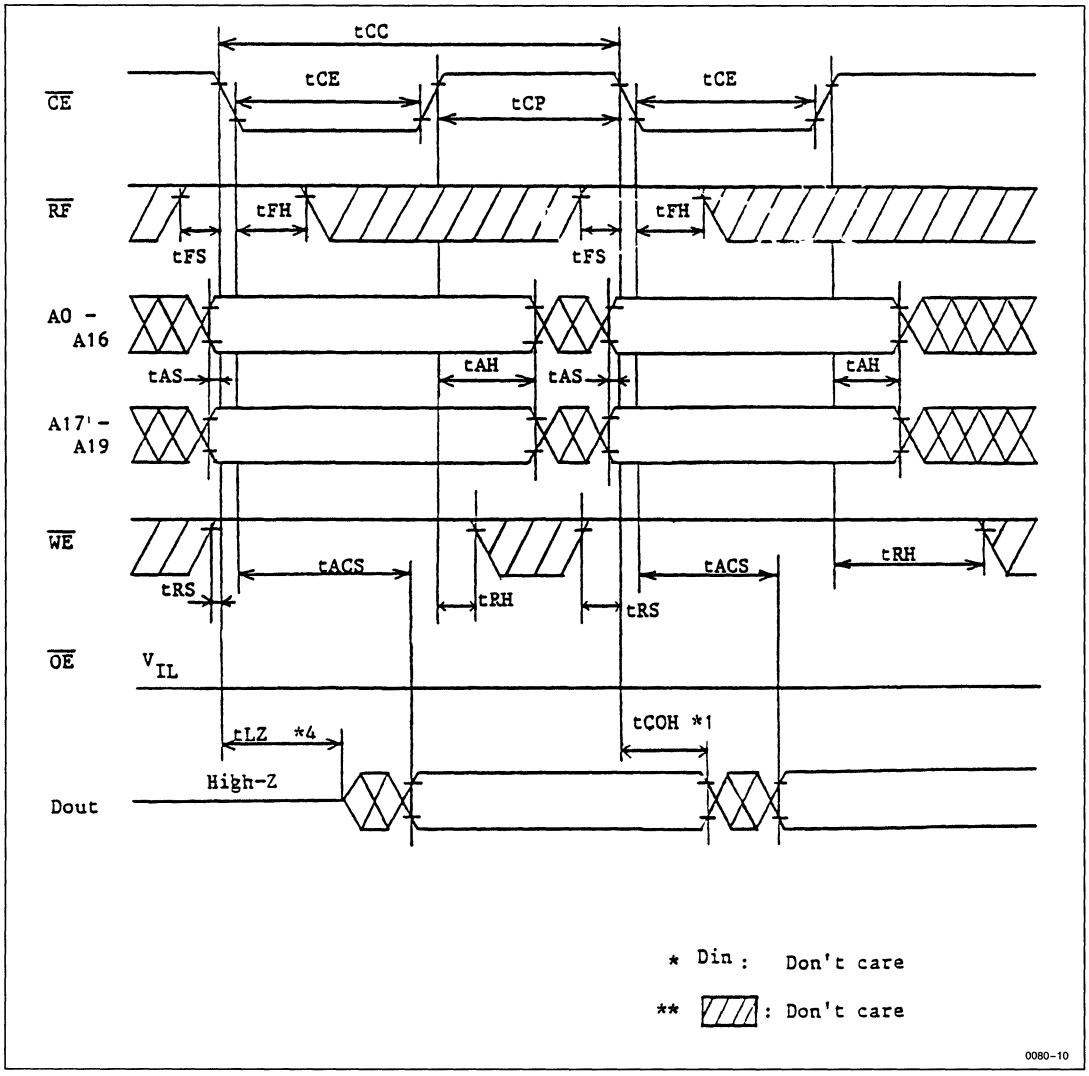
• **Read/Early Write Cycle**



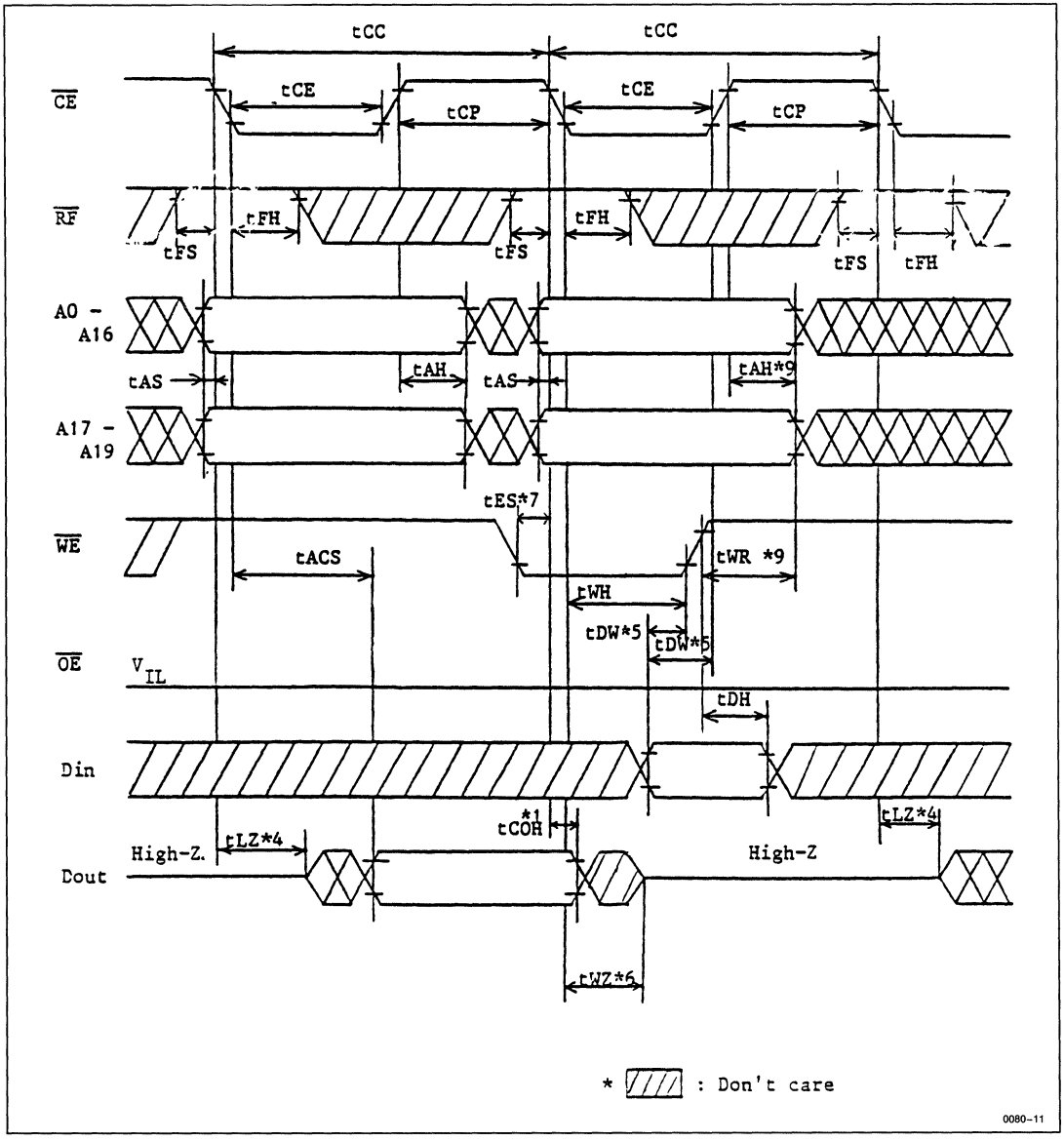
• **Read/Delayed Write Cycle**



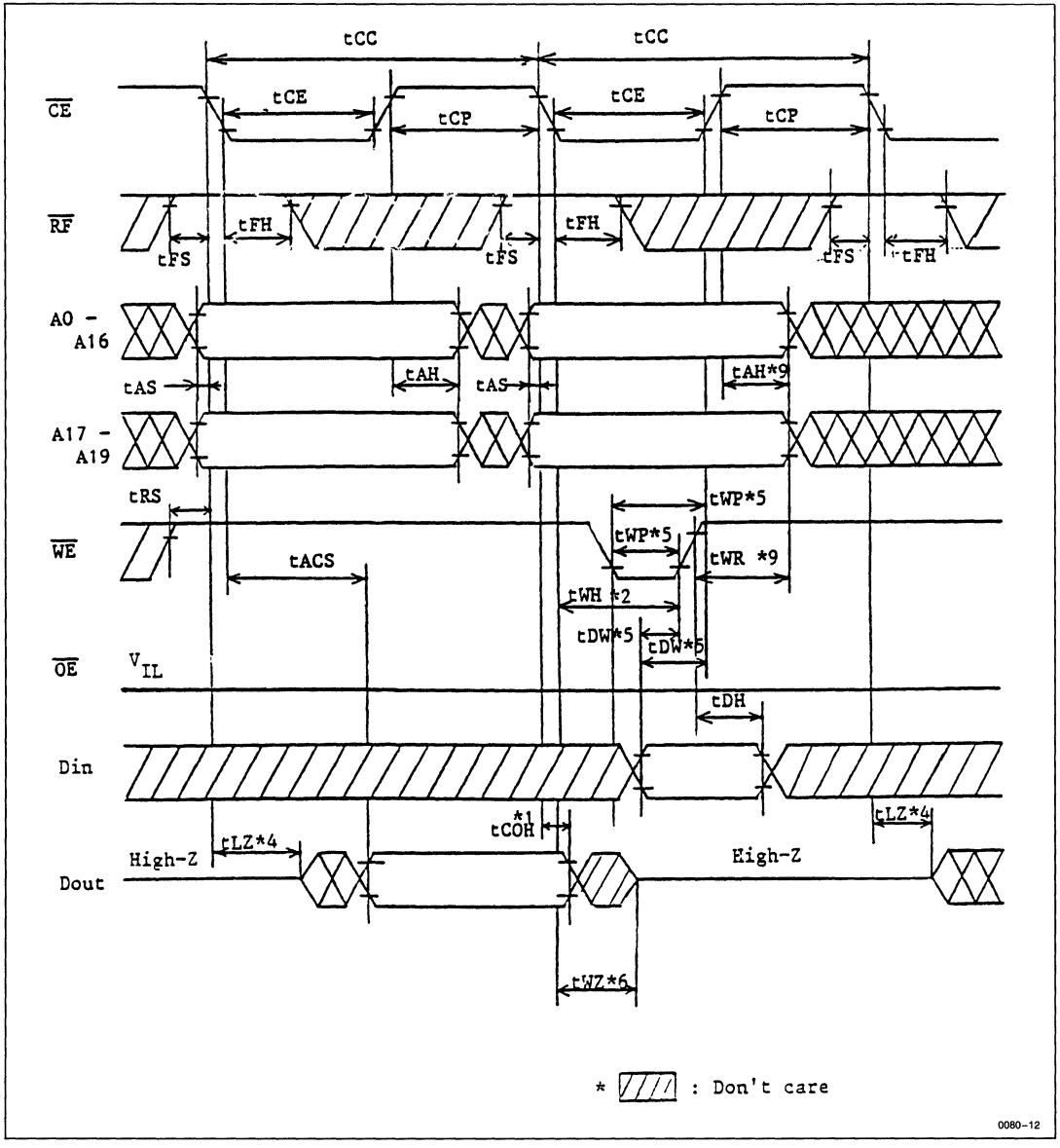
• **Read/Read Cycle ($\overline{OE}$ = V_{IL})**



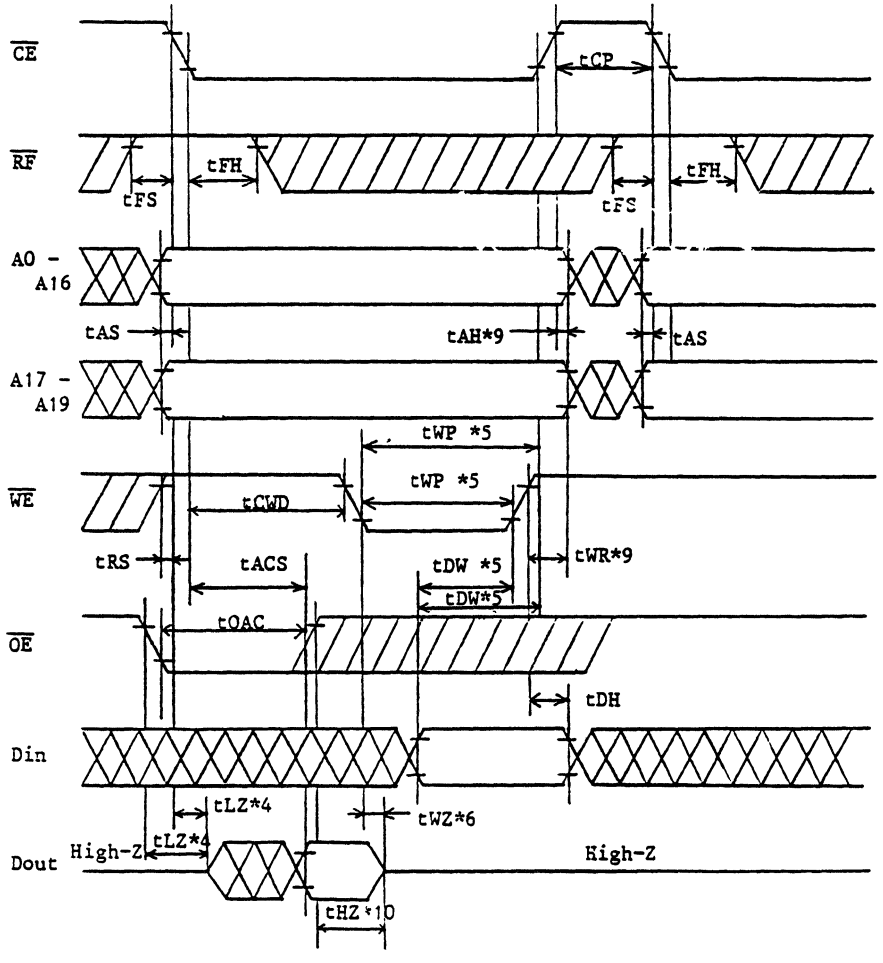
• **Read/Early Write Cycle ($\overline{OE}$ = V_{IL})**



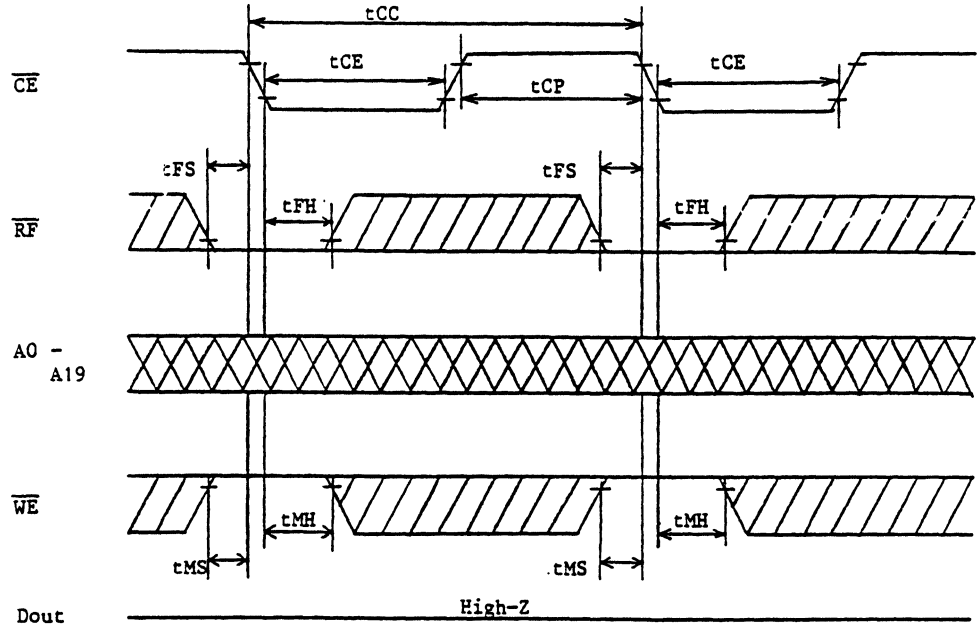
• **Read/Delayed Write Cycle ($\overline{OE}$ = V_{IL})**



• **Read-Modify-Write Cycle**



• **Automatic Refresh Cycle**



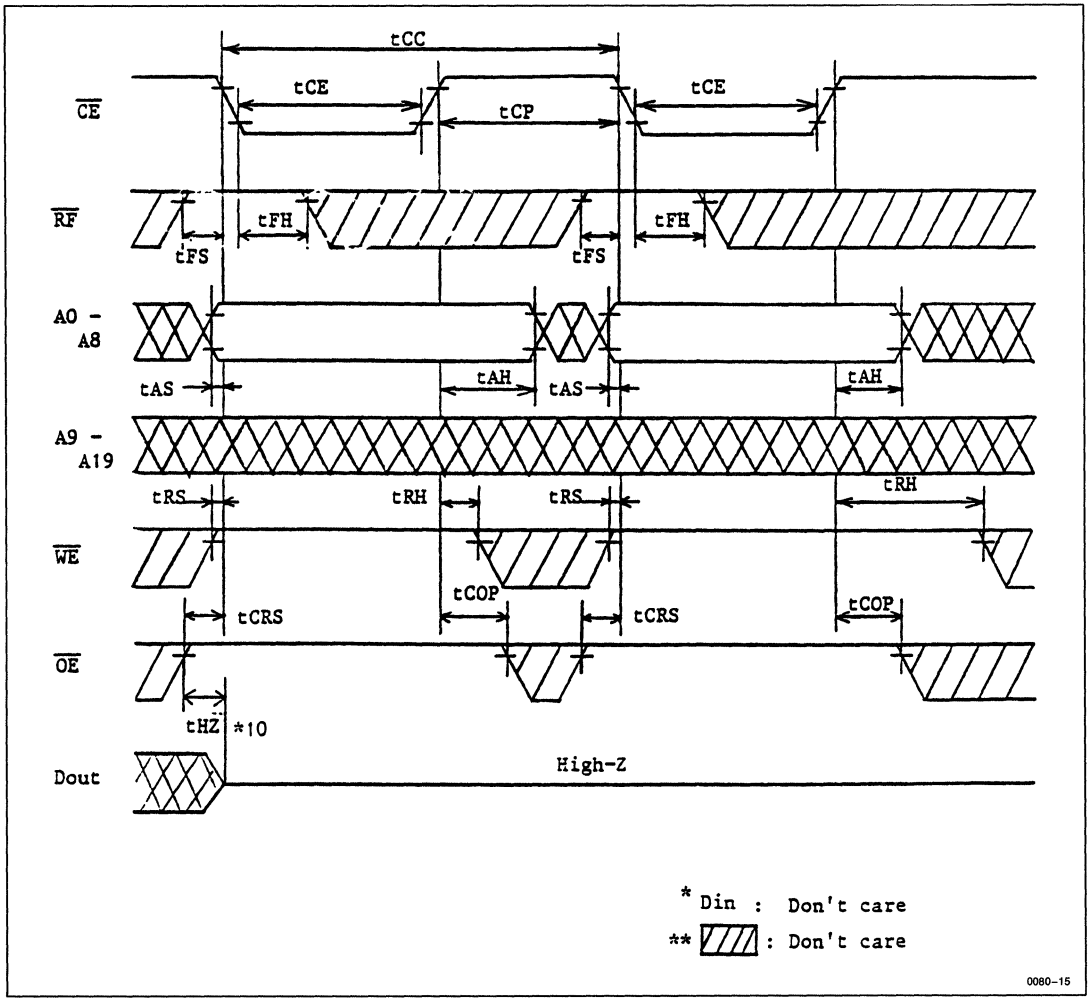
* A0 - A19: Don't care

** $\overline{OE}$, Din : Don't care

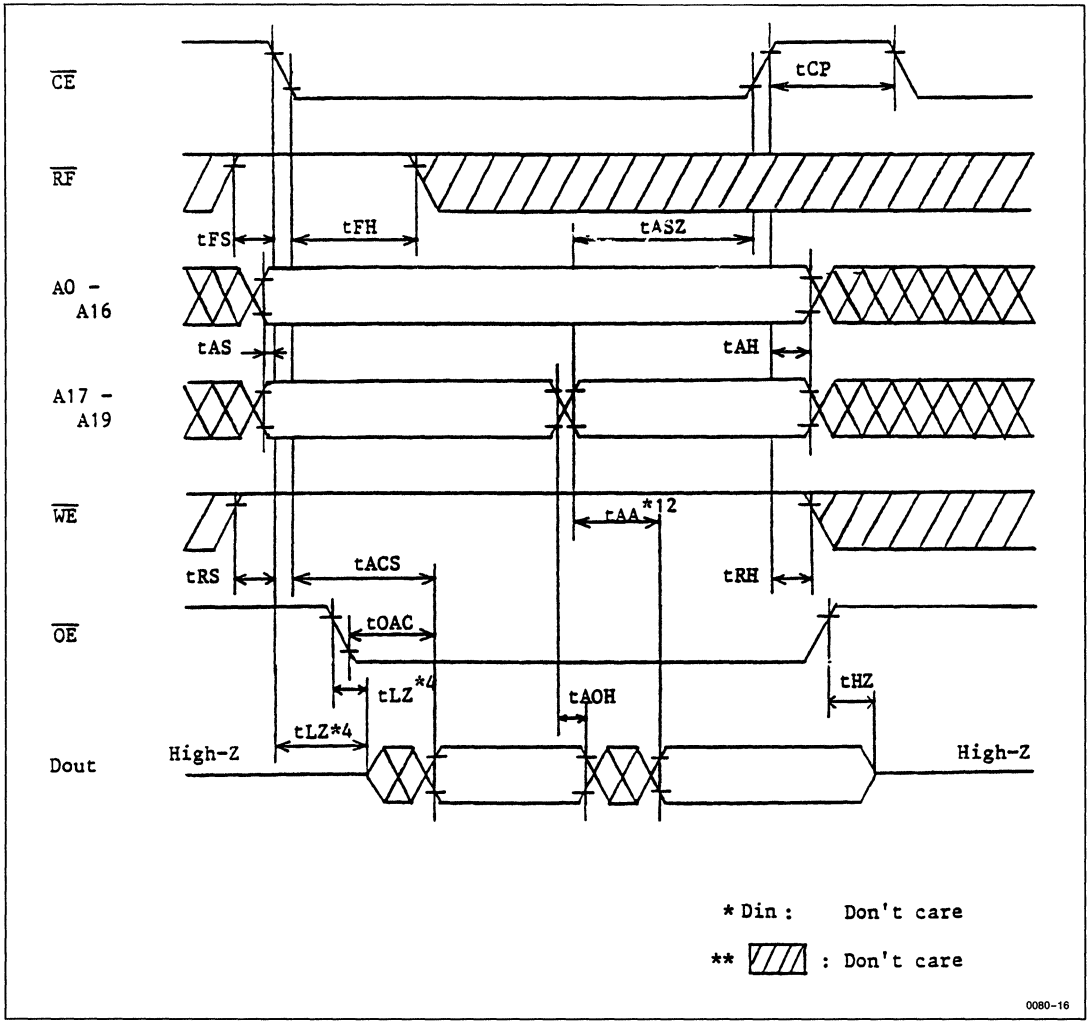
*** ▨ : Don't care

0080-14

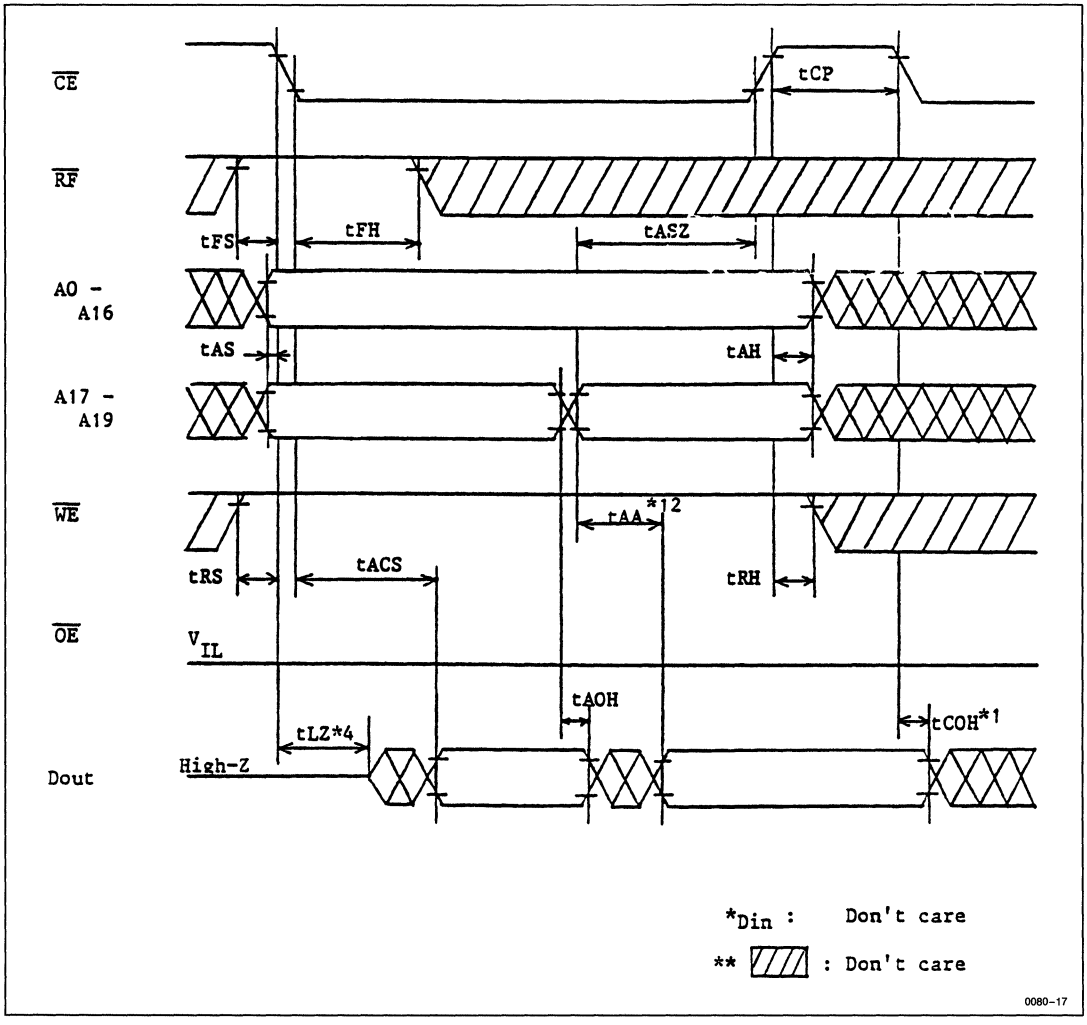
• $\overline{CE}$ Refresh



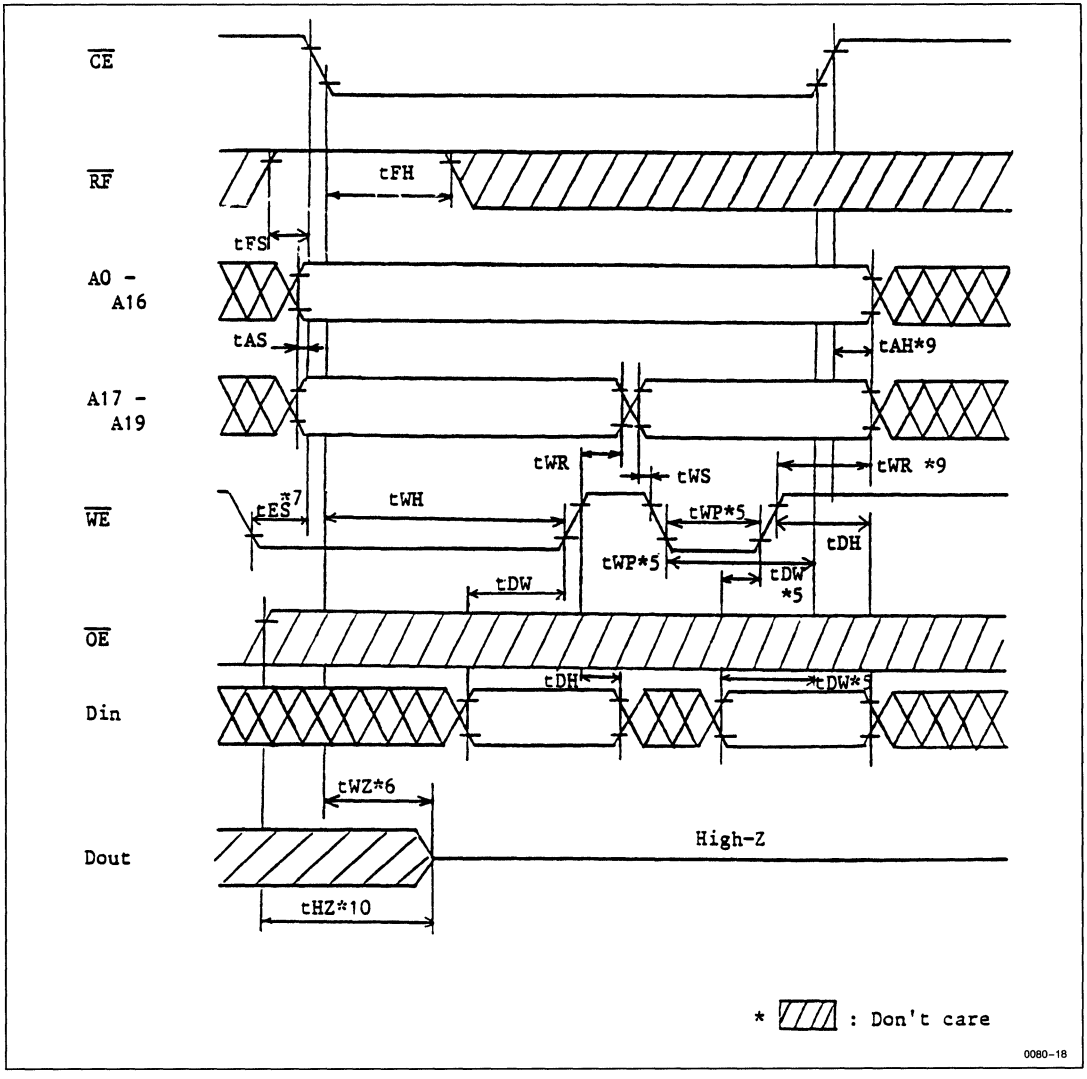
• **Static Column Mode Read Cycle**



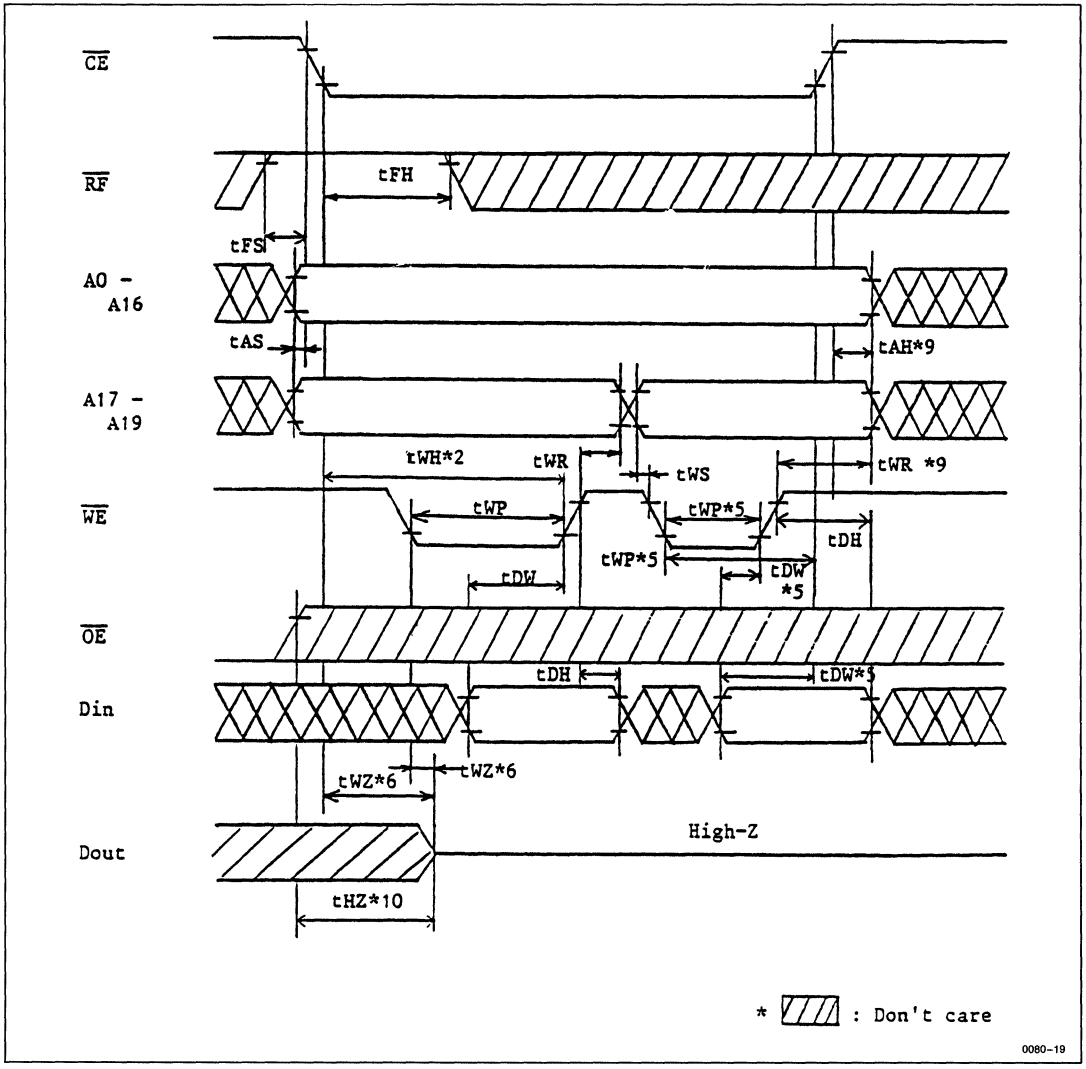
• **Static Column Mode Read Cycle ($\overline{OE}$ = V_{IL})**



• **Static Column Mode Write Cycle *8 (1st Cycle = Early Write Cycle)**



• Static Column Mode Write Cycle *8 (1st Cycle = Delayed Write Cycle)



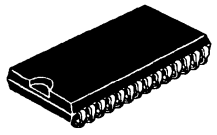
HM574256 Series

262,144-Word x 4-Bit High Speed Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM574256 is a super high speed dynamic RAM organized 262,144-word x 4-bit. HM574256 has realized higher density, higher performance and various functions by employing 1.3 μm Bi-CMOS technology and some new Bi-CMOS circuit design technologies. The HM574256 offers 2-bit static column mode as a high speed access mode.

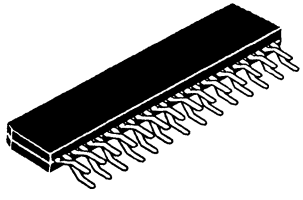
HM574256JP Series



3DCP28DN

(CP-28DN)

HM574256ZP Series



3DZP28

(ZP-28)

■ FEATURES

- Single
  - 5V (±10%) for HM574256JP/ZP-40/45
  - 5V (±5%) for HM574256JP/ZP-35R
- High Speed
  - Access Time .....35 ns/40 ns/45 ns (max)
- 512 Refresh Cycles .....(4 ms)
- 2 Variations of Refresh
  - $\overline{CE}$ Refresh
  - Automatic Refresh
- 2 Bits Static Column Mode

■ ORDERING INFORMATION

Part No.	Access Time	Package	Note
HM574256JP-35R HM574256JP-40 HM574256JP-45	35 ns 40 ns 45 ns	300 mil 28-pin Plastic SOJ (CP-28DN)	
HM574256ZP-35R HM574256ZP-40 HM574256ZP-45	35 ns 40 ns 45 ns	400 mil 28-pin Plastic ZIP (ZP-28)	1 1 1

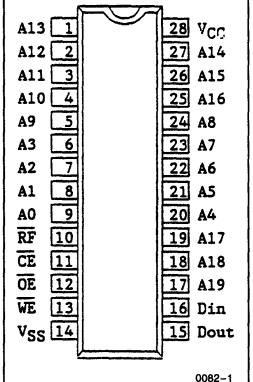
Note: 1. ZIP type products are preliminary.

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Input for $\overline{CE}$ Refresh
A_9–A_{16}	Address Input
A_{17}	Address Input for Static Column Mode
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Read/Write Enable
I/O_0–I/O_4	Data-in/Data-out
$\overline{RF}$	Refresh Control
V_{CC}	Power (+5V)
V_{SS}	Ground

■ PIN OUT

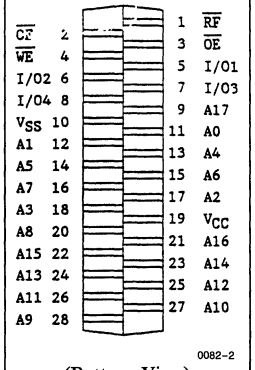
HM574256JP Series



0082-1

(Top View)

HM574256ZP Series



0082-2

(Bottom View)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_T	0.8	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	-35R	V_{CC}	4.75	5.0	5.25	V	1
	-40/-45		4.50		5.50		
Input High Voltage		V_{IH}	2.4	—	6.5	V	1, 3
Input Low Voltage		V_{IL}	− 1.0	—	0.8	V	1, 2

Notes: 1. All voltage referenced to V_{SS}.

2. The device will withstand undershoots to the − 2V level with a maximum pulse width of 20 ns at the − 1.5V level. (See Figure 1.)

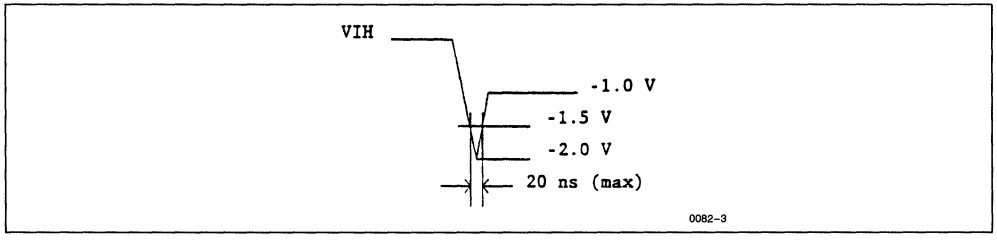


Figure 1. Undershoot of Input Voltage

3. The V_{IH} level of $\overline{OE}$ shall be lower than V_{CC} + 0.5V.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{SS} = 0V)

(V_{CC} = 5V ± 10% for HM5474256JP-40/45)

(V_{CC} = 5V ± 10% for HM5474256JP-35R)

Parameter	Symbol	HM574256-35R		HM574256-40		HM574256-45		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Normal Operating Current	I_{CCA}	See Figure 2						mA		1
Refresh Current	I_{CCR}	See Figure 2						mA		1
Standby Current	I_{CCS}	—	5	—	5	—	5	mA		
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	$0V < V_{in} < 7V$	2
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	μA	$0V \leq V_{out} \leq 7V$, D_{out} = Disable	

• **DC Electrical Characteristics** (T_A = 0 to +70°C, V_{SS} = 0V)
(V_{CC} = 5V ±10% for HM5474256JP-40/45)
(V_{CC} = 5V ±10% for HM5474256JP-35R) (continued)

Parameter	Symbol	HM574256-35R		HM574256-40		HM574256-45		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −4 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 8 mA	

Notes: 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.
2. The V_{in} level of $\overline{OE}$ that is I_{LI} test condition of $\overline{OE}$ must be lower than V_{CC} + 0.5V.

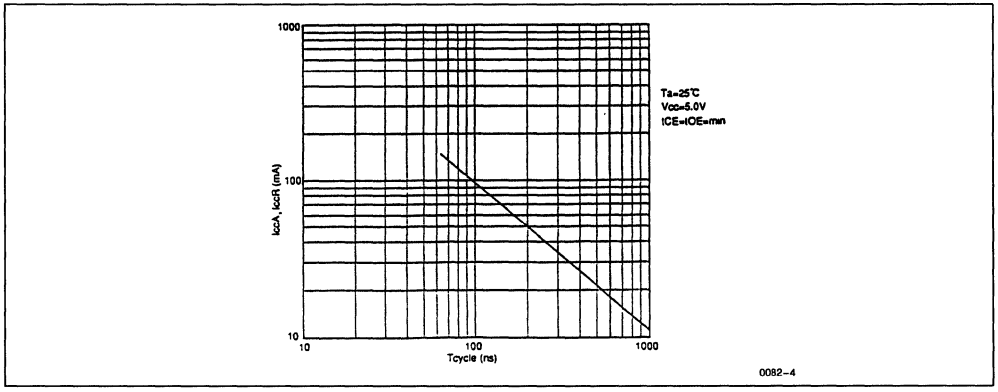


Figure 2. I_{CCA}, I_{CCR} vs T_{cycle}

• **Capacitance** (T_A = 25°C)
(V_{CC} = 5V ±5% for HM5474256JP-40/45)
(V_{CC} = 5V ±5% for HM5474256JP-35R)

Parameter		Symbol	Typ	Max	Unit	Note
Input Capacitance	Address, Data-in	C_{in1}	—	5	pF	1
	Clock ($\overline{CE}$, $\overline{OE}$)	C_{in2}	—	5	pF	1
	Clock ($\overline{WE}$, $\overline{RF}$)	C_{in3}	—	7	pF	1
Output Capacitance (Data-in, Data-out)		$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{OE}$, $\overline{CE}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{SS} = 0V)[1]
(V_{CC} = 5V ±10% for HM5474256JP-40/45)
(V_{CC} = 5V ±10% for HM5474256JP-35R)

Test Conditions

Input pulse levels: V_{IH} = 3.0V, V_{IL} = 0V
Transition time: t_T = 3 ns
Input timing reference levels: High = 2.4V, Low = 0.8V (See Figure 3.)
Output timing reference levels: High = 2.4V, Low = 0.4V
Output load: See Figure 4.

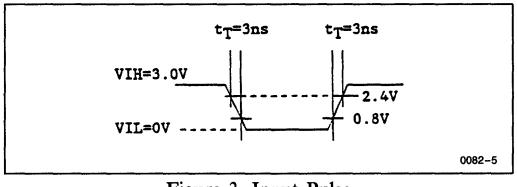


Figure 3. Input Pulse

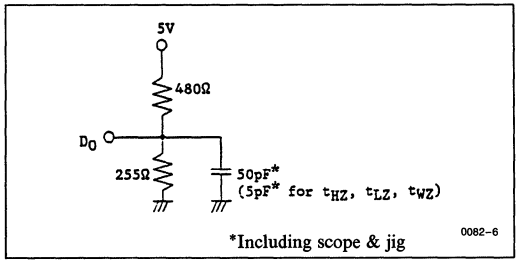


Figure 4. Output Load

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM574256-35R		HM574256-40		HM574256-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read/Write Cycle Time	t_{CC}	75	—	85	—	90	—	ns	
CE Pulse Width	t_{CE}	35	5000	40	5000	45	5000	ns	
CE Precharge Time	t_{CP}	34	—	39	—	39	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Address Hold Time	t_{AH}	5	—	5	—	5	—	ns	
Transition Time (Rise and Fall)	t_T	1	10	1	10	1	10	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	

Read Cycle

Parameter	Symbol	HM574256-35R		HM574256-40		HM574256-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{CE}$	t_{ACS}	—	35	—	40	—	45	ns	
Address Access Time	t_{AA}	—	25	—	30	—	30	ns	
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	25	—	25	ns	
Setup Time On Read	t_{RS}	0	—	0	—	0	—	ns	
Hold Time on Read	t_{RH}	5	—	5	—	5	—	ns	
$\overline{OE}$ Setup Time	t_{OES}	5	—	5	—	5	—	ns	
$\overline{OE}$ Enable to Output in Low-Z	t_{LZ}	0	—	0	—	0	—	ns	
$\overline{OE}$ Disable to Output in High-Z	t_{HZ}	—	15	—	20	—	20	ns	
Output Hold Time from Address	t_{AOH}	3	—	3	—	3	—	ns	
Output Hold Time from $\overline{CE}$	t_{COH}	0	—	0	—	0	—	ns	
$\overline{CE}$ to $\overline{OE}$ Precharge Time	t_{COP}	10	—	10	—	10	—	ns	

Write Cycle

Parameter	Symbol	HM574256-35R		HM574256-40		HM574256-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Data Setup Time	t_{DW}	20	—	25	—	30	—	ns	
Data Hold Time	t_{DH}	5	—	5	—	5	—	ns	
Setup Time on Early Write	t_{ES}	5	—	5	—	5	—	ns	
$\overline{WE}$ Pulse Width	t_{WP}	25	—	30	—	35	—	ns	
Write Hold Time from $\overline{CE}$	t_{WH}	35	—	40	—	45	—	ns	
$\overline{WE}$ Enable to Output in High-Z	t_{WZ}	—	15	—	20	—	20	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	15	—	20	—	20	—	ns	
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	15	—	20	—	20	—	ns	
$\overline{CE}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	0	—	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM574256-35R		HM574256-40		HM574256-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{WE}$ Delay Time from $\overline{CE}$	t_{CWD}	35	—	40	—	45	—	ns	

Refresh Cycle

Parameter	Symbol	HM574256-35R		HM574256-40		HM574256-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{RF}$ Setup Time	t_{FS}	5	—	5	—	5	—	ns	
$\overline{RF}$ Hold Time	t_{FH}	15	—	15	—	15	—	ns	
Mode Selection Setup Time	t_{MS}	0	—	0	—	0	—	ns	
Mode Selection Hold Time	t_{MH}	15	—	20	—	20	—	ns	
Setup Time on $\overline{CE}$ Refresh	t_{CRS}	15	—	20	—	20	—	ns	

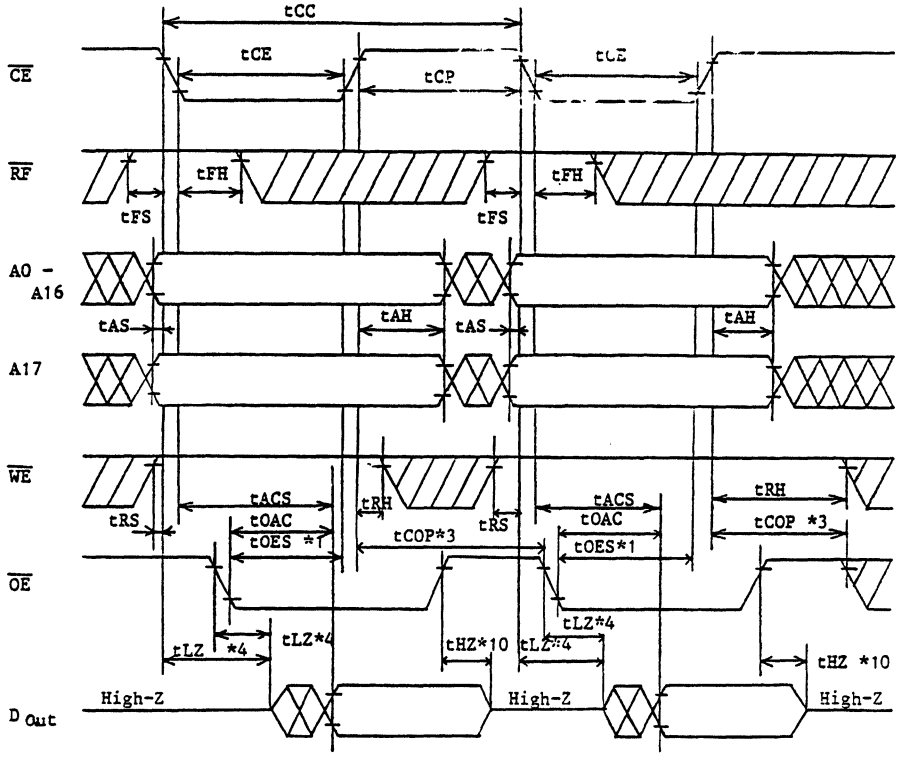
Static Column Mode Cycle

Parameter	Symbol	HM574256-35R		HM574256-40		HM574256-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Static Column Address Setup Time	t_{ASZ}	20	—	25	—	25	—	ns	
Address Setup Time to $\overline{WE}$	t_{WS}	0	—	0	—	0	—	ns	
Address Hold Time from $\overline{WE}$	t_{WR}	0	—	0	—	0	—	ns	

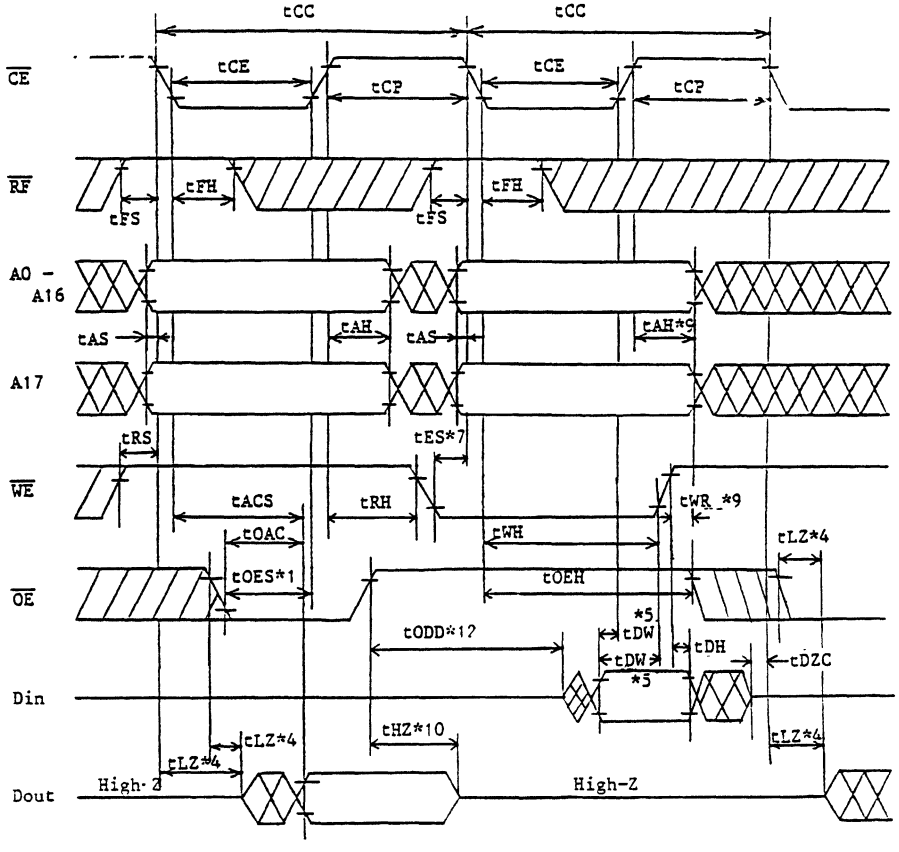
Notes:
1. If $t_{OES} > t_{OES}$ (min) and $\overline{OE}$ is held at low level, D_{out} will be valid until the next negative transition of $\overline{CE}$.
2. Both t_{WH} and t_{WP} must be satisfied for a delayed write cycle.
3. If $t_{COP} < t_{COP}$ (min), D_{out} cannot be guaranteed to be in high impedance.
4. If the negative transition of $\overline{OE}$ occurs before that of $\overline{CE}$, t_{LZ} is controlled by $\overline{CE}$.
5. t_{WP} and t_{DW} are specified by the positive transition of $\overline{CE}$ or $\overline{WE}$ whichever occurs earlier.
6. When $\overline{WE}$ goes low, D_{out} becomes high impedance and is held in this condition to the next cycle. If the negative transition of $\overline{WE}$ occurs before that of $\overline{CE}$, D_{out} is controlled by $\overline{CE}$. t_{WZ} defines the time at which the output achieves the open circuit condition.
7. If $t_{ES} > t_{ES}$ (min), the cycle is early write and D_{out} is in high impedance.
8. In static column mode cycles, read operation cannot be performed after write operation.
9. Both t_{AH} and t_{WR} must be satisfied for a write cycle.
10. t_{HZ} defines the time at which the output achieves the open circuit condition.
11. An initial pause of 100 μs is required after power-up, then execute at least eight $\overline{CE}$ refresh cycles.
12. During I/O pins are in the output state, Data-in shall not be applied to I/O pins. So, in all write cycles (early write, delayed write and read-modify-write), $\overline{OE}$ must go to high level to disable the output buffer prior to applying data to the device.
13. In static column mode cycle, there must not be any invalid address inputs for static column mode (A17) which are less than t_{AA}.

■ TIMING WAVEFORMS

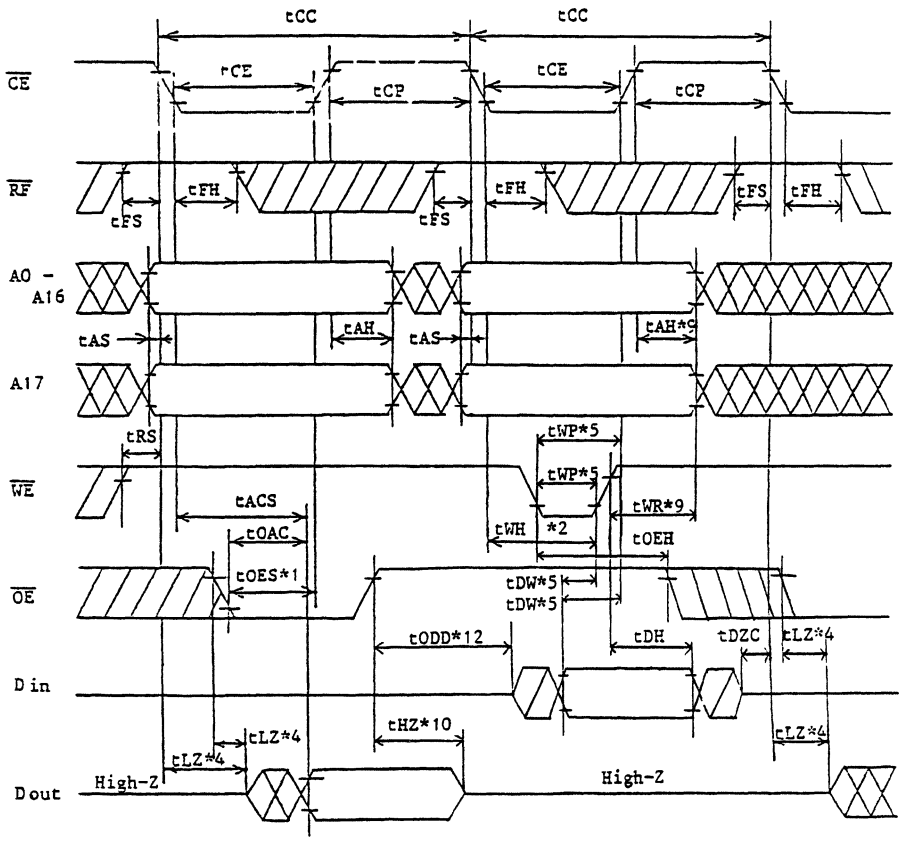
• Read/Read Cycle



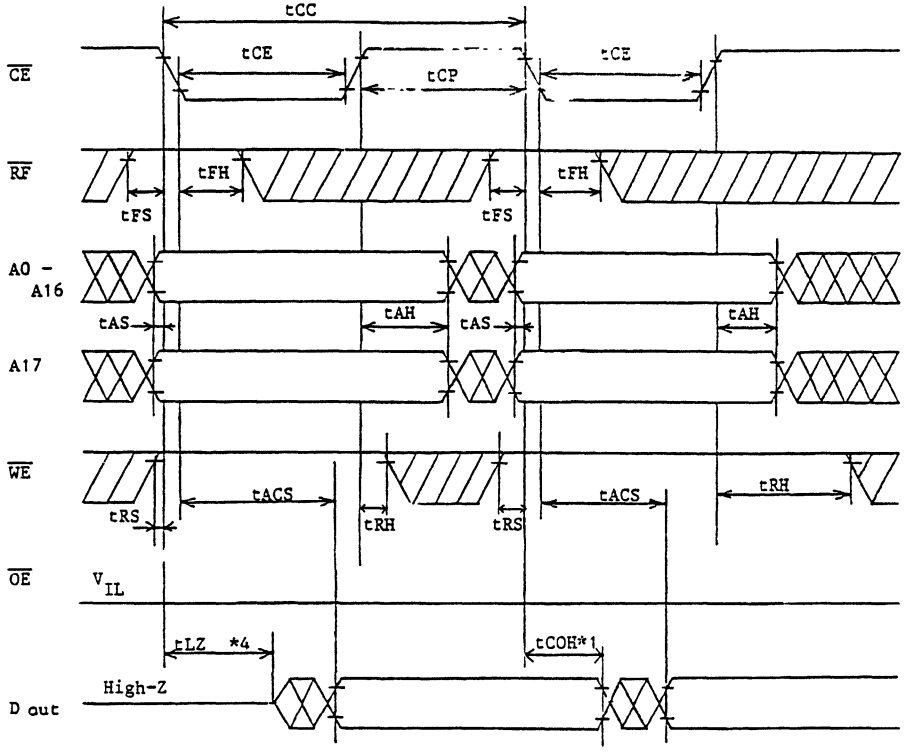
• **Read/Early Write Cycle**



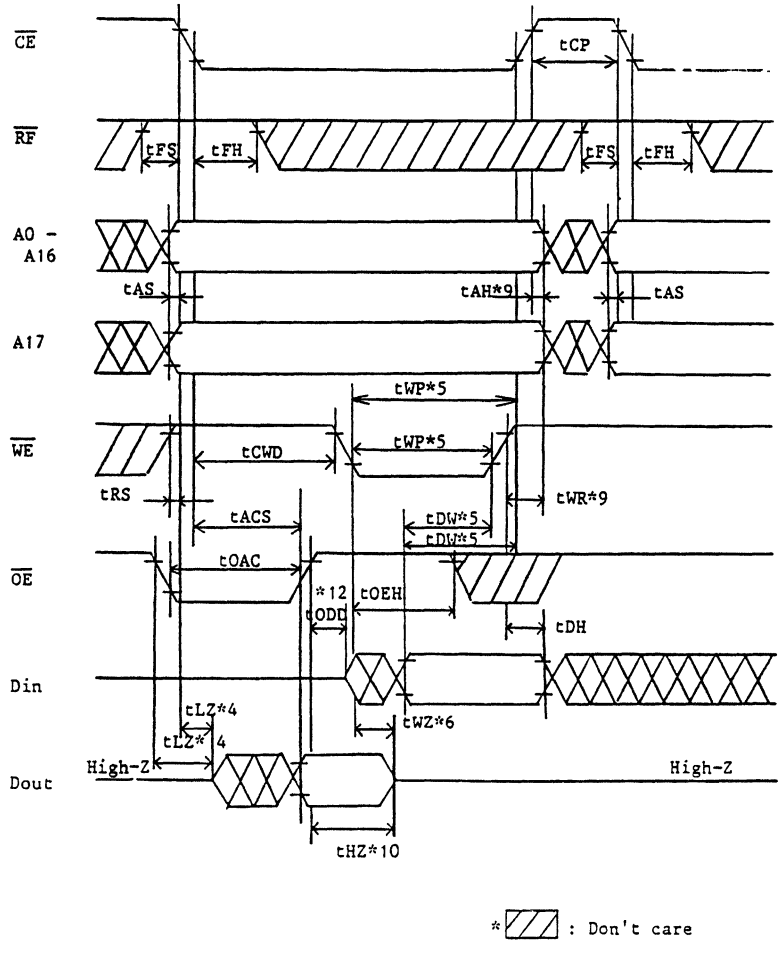
• **Read/Delayed Write Cycle**



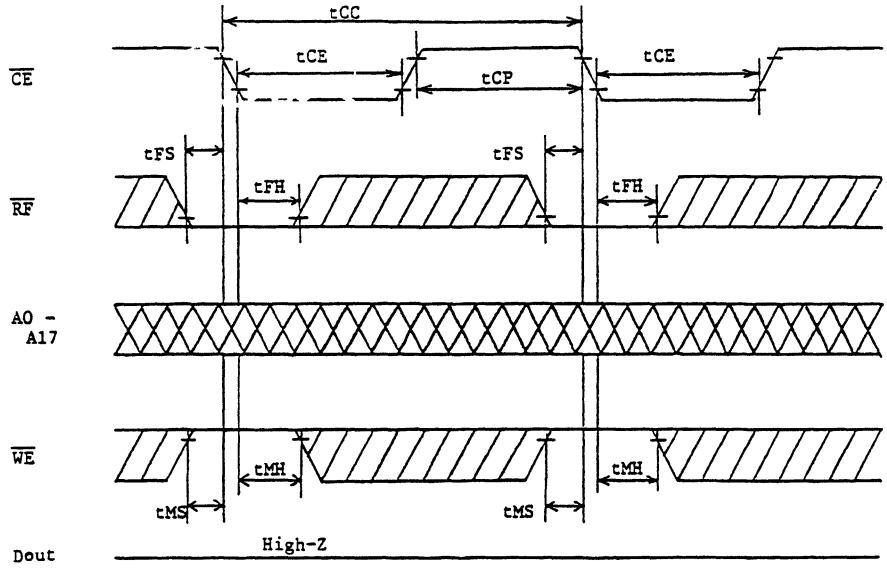
• **Read/Read Cycle ($\overline{OE}$ = V_{IL})**



• **Read-Modify-Write Cycle**



• **Automatic Refresh Cycle**



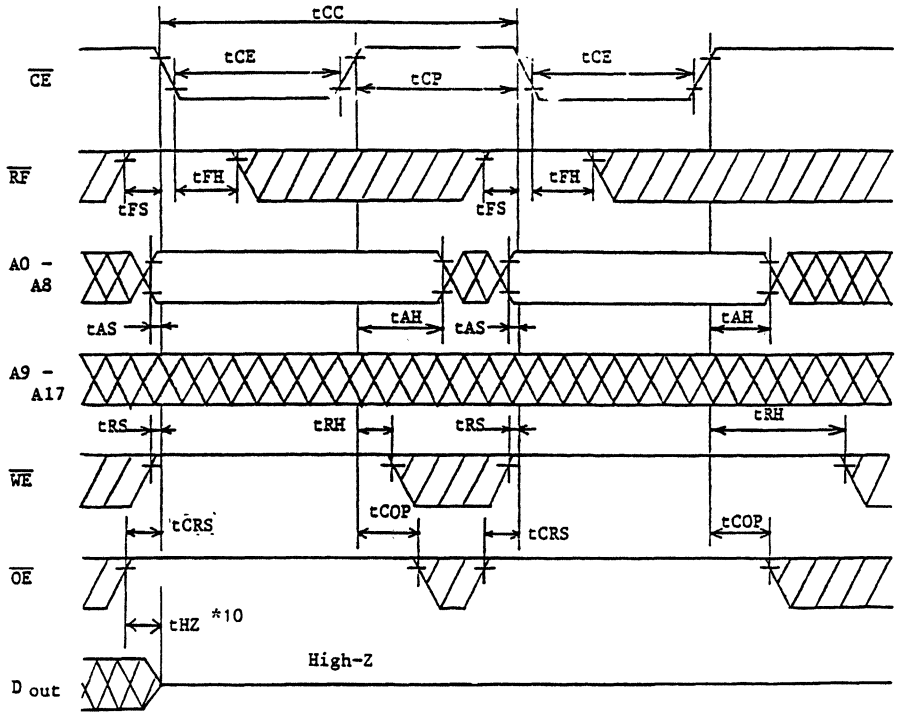
* A0 - A17 : Don't care

** $\overline{OE}$, Din : Don't care

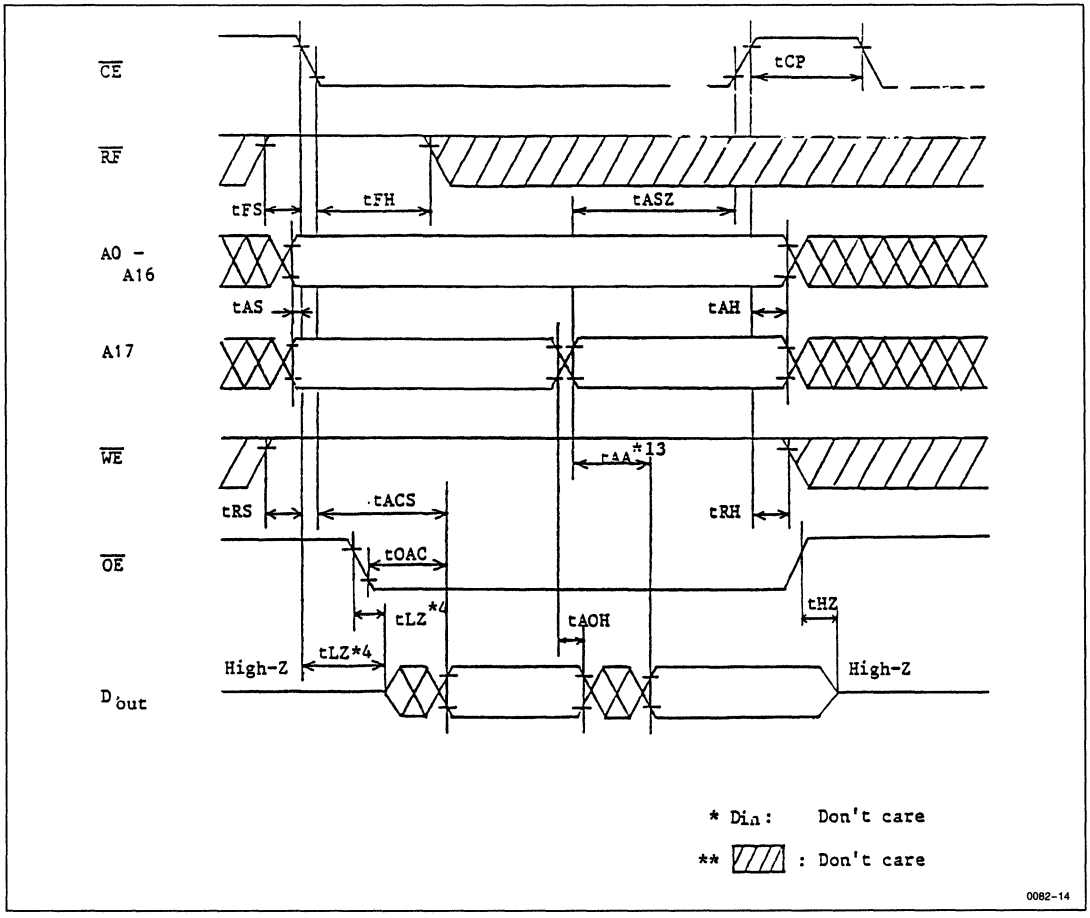
*** ▨ : Don't care

0082-12

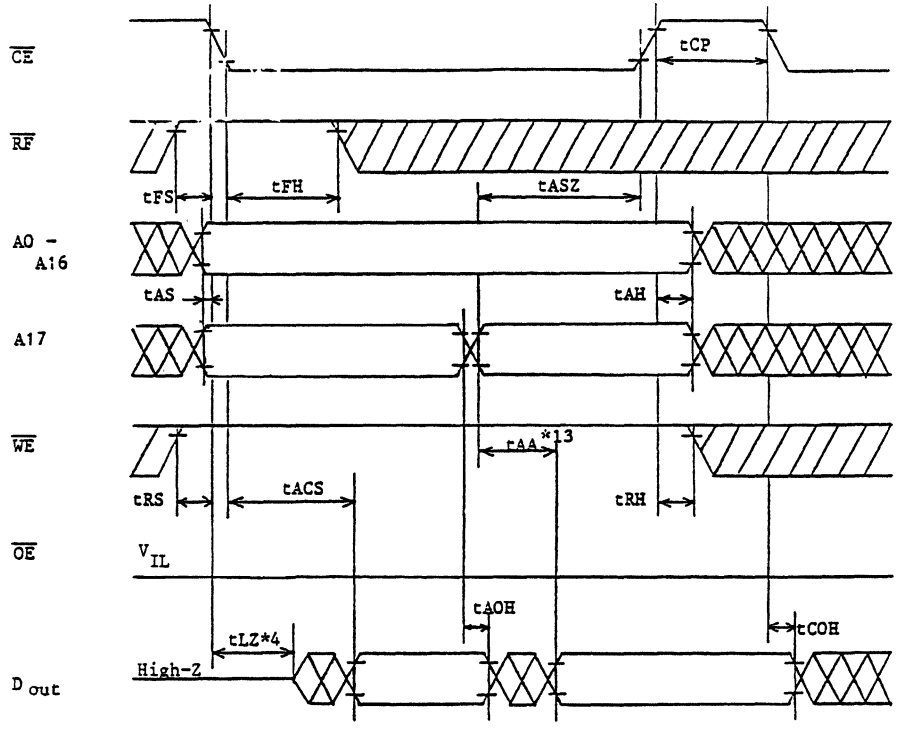
• $\overline{CE}$ Refresh



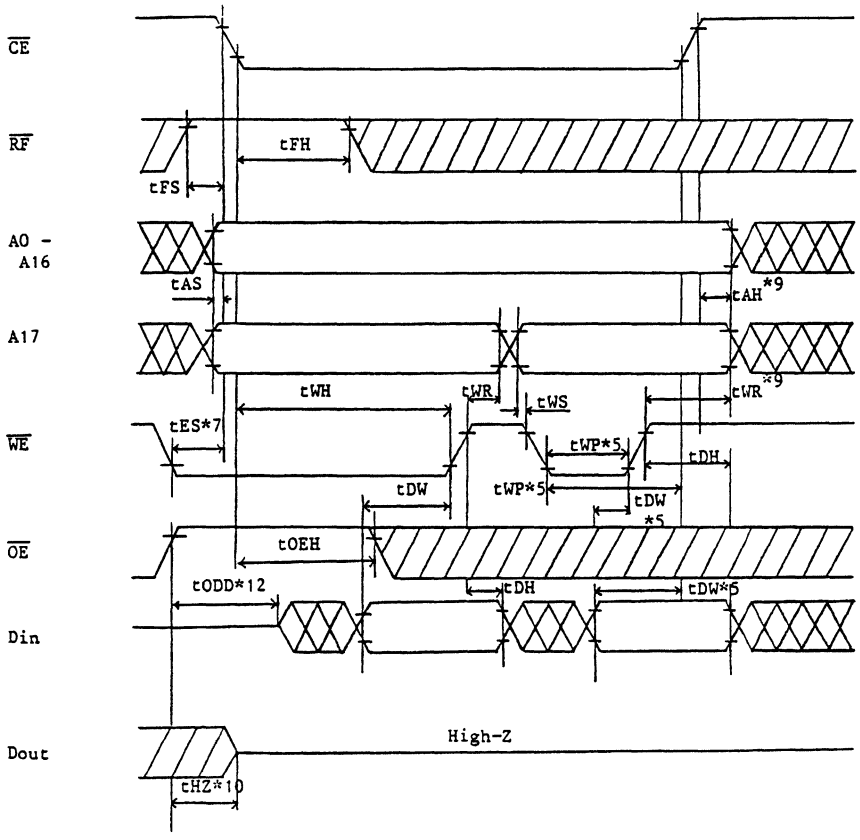
• **Static Column Mode Read Cycle**



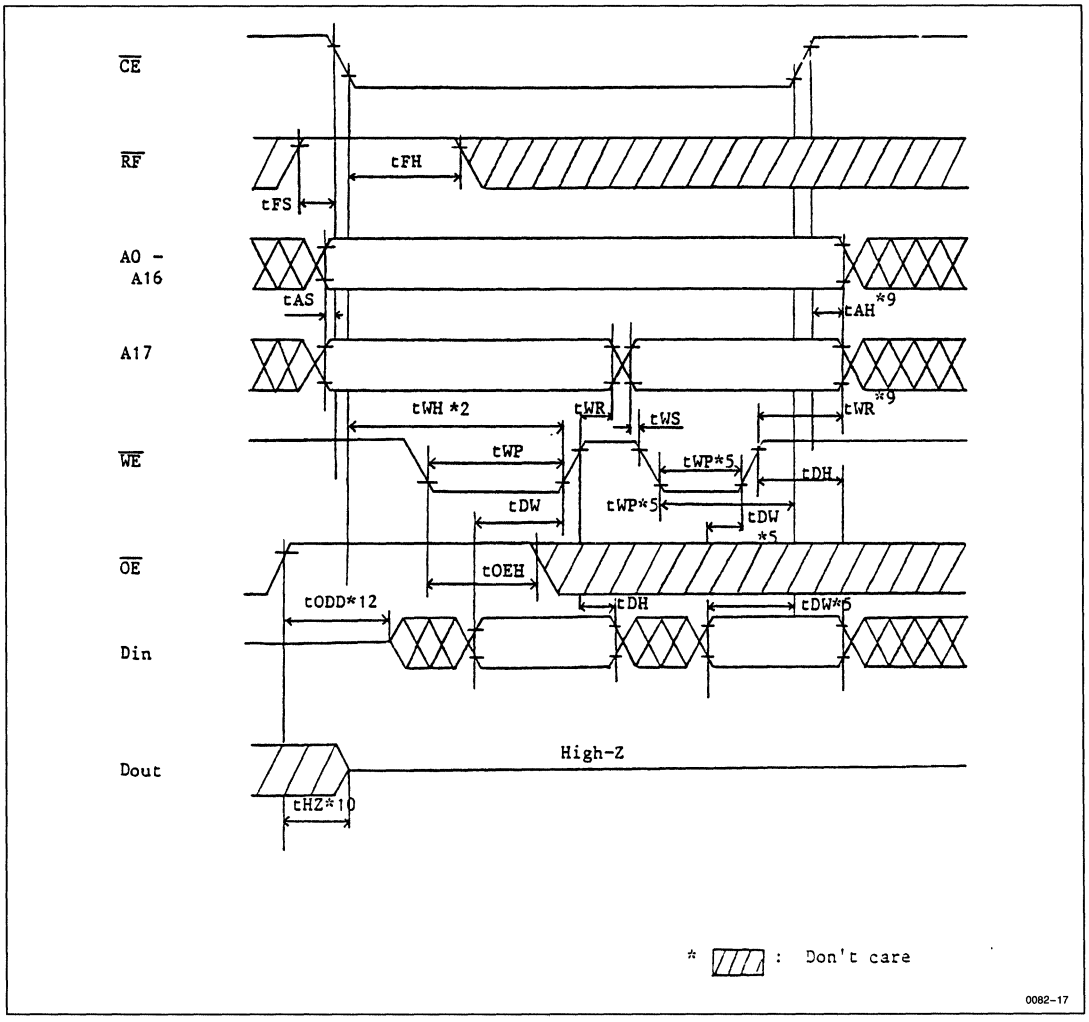
• **Static Column Mode Read Cycle ($\overline{OE}$ = V_{IL})**



• **Static Column Mode Write Cycle[8]** (1st Cycle = Early Write Cycle)



• **Static Column Mode Write Cycle[8]** (1st Cycle = Delayed Write Cycle)



HM574100 Series — Preliminary

4,194,304-Word x 1-Bit High Speed Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM574100 is a super high speed dynamic RAM organized 4,194,304-word x 1-bit. HM574100 has realized higher density, higher performance and various functions by employing 0.8 μm Bi-CMOS technology and some new Bi-CMOS circuit design technologies. The HM574100 offers 8 bit static column mode as a high speed access mode.

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....35 ns/40 ns/45 ns (max)
- 2,048 Refresh Cycles.....(16 ms)
- 2 Variations of Refresh
  - $\overline{CE}$ Refresh
  - Automatic Refresh
- 8 Bits Static Column Mode

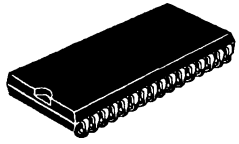
■ ORDERING INFORMATION

Part No.	Access Time	Package
HM574100JP-35	35 ns	300 mil 32-pin
HM574100JP-40	40 ns	Plastic SOJ
HM574100JP-45	45 ns	(CP-32D)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{10}	Address Input for $\overline{CE}$ Refresh
A_{11}–A_{18}	Address Input
A_{19}–A_{21}	Address Input for Static Column Mode
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Read/Write Enable
D_{in}	Data-in
D_{out}	Data-out
$\overline{RF}$	Refresh Control
V_{CC}	Power (+ 5V)
V_{SS}	Ground

HM574100JP Series

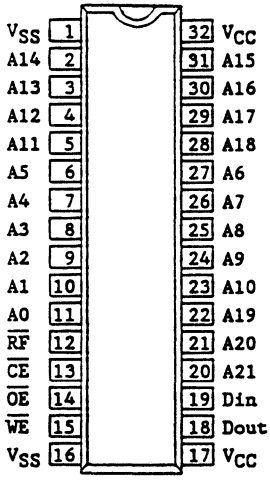


3DCP32D

(CP-32D)

■ PIN OUT

HM574100JP Series



0079-1

(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_T	0.8	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1, 2

Notes: 1. All voltage referenced to V_{SS}.
2. The device will withstand undershoots to the −2.0V level with a maximum pulse width of 20 ns at the −1.5V level. (See Figure 1.)

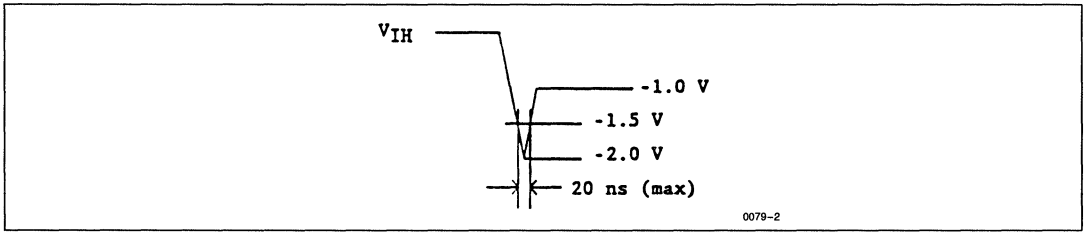


Figure 1. Undershoot of Input Voltage

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM574100-35		HM574100-40		HM574100-45		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Normal Operating Current	I_{CCA}	TBD	TBD	TBD	TBD	TBD	TBD	mA		1
Refresh Current	I_{CCR}	TBD	TBD	TBD	TBD	TBD	TBD	mA		1
Standby Current	I_{CCS}	—	5	—	5	—	5	mA		
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	μA	$0V < V_{in} < 7V$	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	μA	$0V < V_{out} < 7V$ D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −4 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 8 mA	

Note: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.

• Capacitance (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter		Symbol	Typ	Max	Unit	Note
Input Capacitance	Address, Data-in	C_{in1}	—	5	pF	1
	Clock	C_{in2}	—	5	pF	1
Output Capacitance	(Data-out)	C_O	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{OE}$, $\overline{CE}$ = V_{IH} to disable D_{out}.

• AC CHARACTERISTICS[1] (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

• Test Conditions

Input Pulse Levels: V_{IH} = 3.0V, V_{IL} = 0V
Transition Time: t_T = 3 ns
Input Timing Reference Levels: High = 2.4V, Low = 0.8V (See Figure 2.)
Output Timing Reference Levels: High = 2.4V, Low = 0.4V
Output Load: See Figure 3.

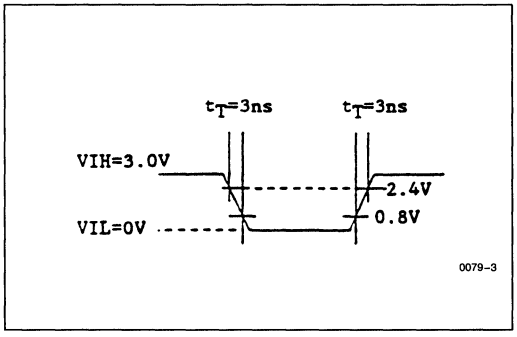


Figure 2. Input Pulse

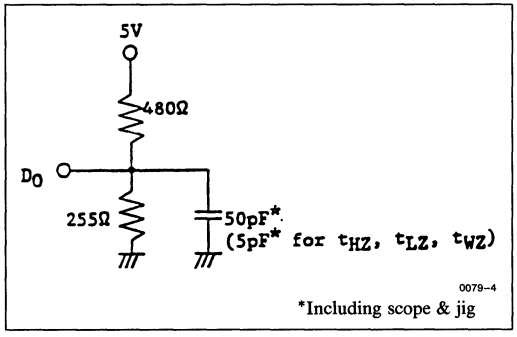


Figure 3. Output Load

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM574100-35		HM574100-40		HM574100-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read/Write Cycle Time	t_{CC}	70	—	80	—	90	—	ns	
$\overline{CE}$ Pulse Width	t_{CE}	35	5000	40	5000	45	5000	ns	
$\overline{CE}$ Precharge Time	t_{CP}	29	—	34	—	39	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Address Hold Time	t_{AH}	5	—	5	—	5	—	ns	
Transition Time (Rise and Fall)	t_T	1	10	1	10	1	10	ns	
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM574100-35		HM574100-40		HM574100-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{CE}$	t_{ACS}	—	35	—	40	—	45	ns	
Address Access Time	t_{AA}	—	25	—	30	—	30	ns	
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	25	—	25	ns	
Setup Time on Read	t_{RS}	0	—	0	—	0	—	ns	
Hold Time on Read	t_{RH}	5	—	5	—	5	—	ns	
$\overline{OE}$ Setup Time	t_{OES}	5	—	5	—	5	—	ns	
$\overline{OE}$ Enable to Output in Low-Z	t_{LZ}	0	—	0	—	0	—	ns	
$\overline{OE}$ Disable to Output in High-Z	t_{HZ}	—	15	—	20	—	20	ns	
Output Hold Time from Address	t_{AOH}	3	—	3	—	3	—	ns	
Output Hold Time from $\overline{CE}$	t_{COH}	0	—	0	—	0	—	ns	
$\overline{CE}$ to $\overline{OE}$ Precharge Time	t_{COP}	10	—	10	—	10	—	ns	

Write Cycle

Parameter	Symbol	HM574100-35		HM574100-40		HM574100-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Data Setup Time	t_{DW}	20	—	25	—	30	—	ns	
Data Hold Time	t_{DH}	5	—	5	—	5	—	ns	
Setup Time on Early Write	t_{ES}	5	—	5	—	5	—	ns	
$\overline{WE}$ Pulse Width	t_{WP}	25	—	30	—	35	—	ns	
Write Hold Time from $\overline{CE}$	t_{WH}	35	—	40	—	45	—	ns	
$\overline{WE}$ Enable to Outupt in High-Z	t_{WZ}	—	15	—	20	—	20	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM574100-35		HM574100-40		HM574100-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{WE}$ Delay Time from $\overline{CE}$	t_{CWD}	35	—	40	—	45	—	ns	

Refresh Cycle

Parameter	Symbol	HM574100-35		HM574100-40		HM574100-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{RF}$ Setup Time	t_{FS}	5	—	5	—	5	—	ns	
$\overline{RF}$ Hold Time	t_{FH}	15	—	15	—	15	—	ns	
Mode Selection Setup Time	t_{MS}	0	—	0	—	0	—	ns	
Mode Selection Hold Time	t_{MH}	15	—	20	—	20	—	ns	
Setup Time on $\overline{CE}$ Refresh	t_{CRS}	15	—	20	—	20	—	ns	

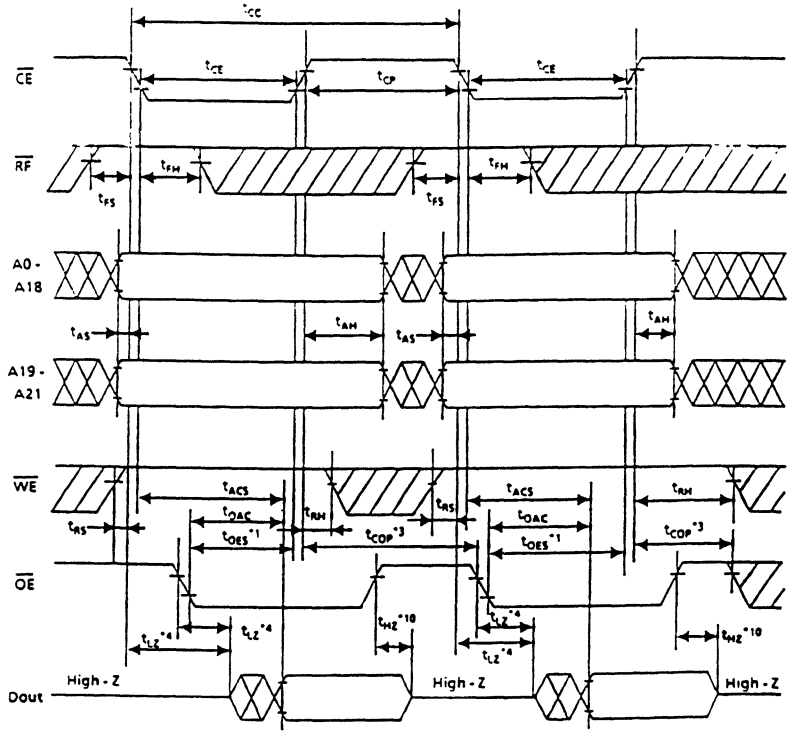
Static Column Mode Cycle

Parameter	Symbol	HM574100-35		HM574100-40		HM574100-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Static Column Address Setup Time	t_{ASZ}	20	—	25	—	25	—	ns	
Address Setup Time to $\overline{WE}$	t_{WS}	0	—	0	—	0	—	ns	
Address Hold Time from $\overline{WE}$	t_{WR}	0	—	0	—	0	—	ns	

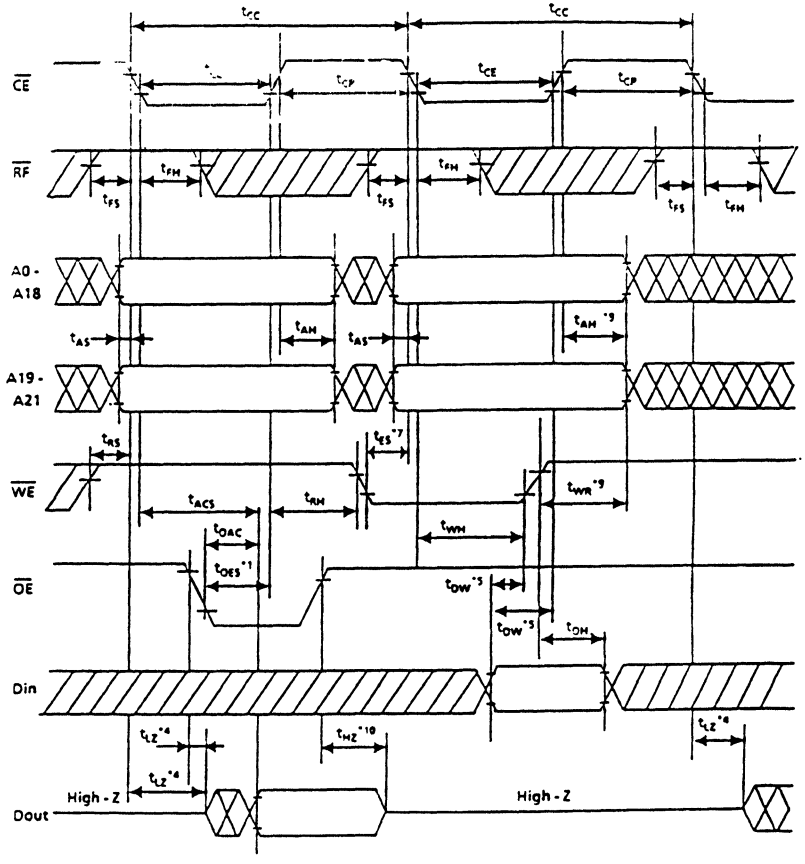
Notes:
1. If $t_{OES} > t_{OES}$ (min) and $\overline{OE}$ is held at low level, D_{out} will be valid until the next negative transition of $\overline{CE}$.
2. Both t_{WH} and t_{WP} must be satisified for a delayed write cycle.
3. If $t_{COP} < t_{COP}$ (min), D_{out} cannot be guaranteed to be in high impedance.
4. If the negative transition of $\overline{OE}$ occurs before that of $\overline{CE}$, t_{LZ} is controlled by $\overline{CE}$.
5. t_{WP} and t_{DW} are specified by the positive transition of $\overline{CE}$ or $\overline{WE}$ whichever occurs earlier.
6. When $\overline{WE}$ goes low, D_{out} becomes high impedance and is held in this condition to the next cycle. If the negative transition of $\overline{WE}$ occurs before that of $\overline{CE}$, D_{out} is controlled by $\overline{CE}$. t_{WZ} defines the time at which the output achieves the open circuit condition.
7. If $t_{ES} > t_{ES}$ (min), the cycle is early write and D_{out} is in high impedance.
8. In static column mode cycles, read operation cannot be performed after write operation.
9. Both t_{AH} and t_{WR} must be satisified for a write cycle.
10. t_{HZ} defines the time at which the output achieves the open circuit condition.
11. An initial pause of 100 μs is required after power-up, then execute at least eight $\overline{CE}$ refresh cycles.
12. In static column mode cycle, there must not be any invalid address inputs for static column mode (A_{19}–A_{21}) are less than t_{AA}.

■ TIMING WAVEFORMS

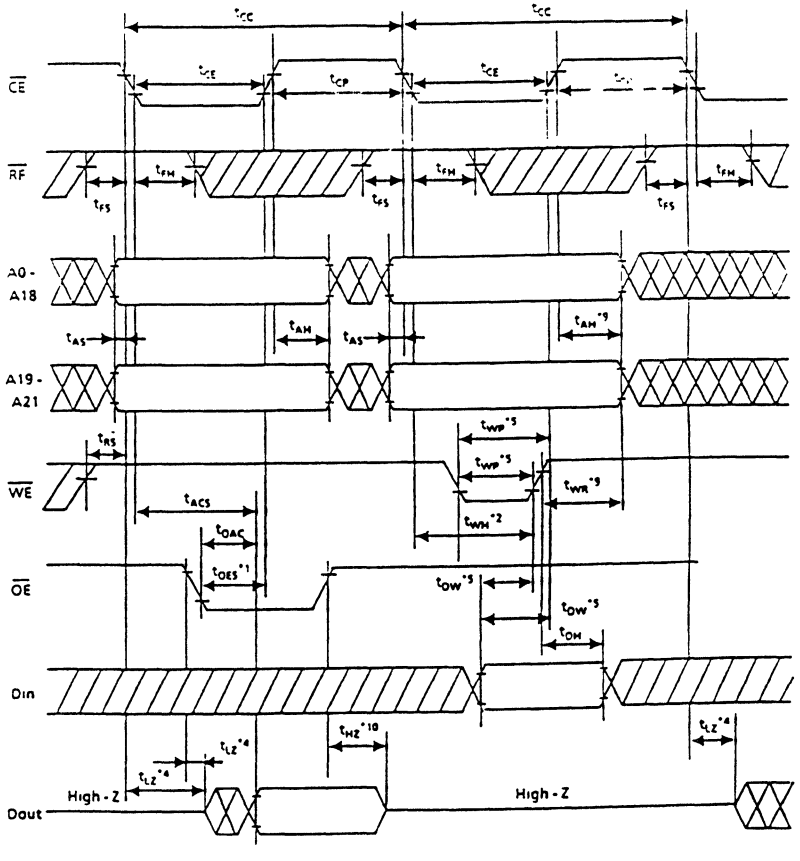
• Read/Read Cycle



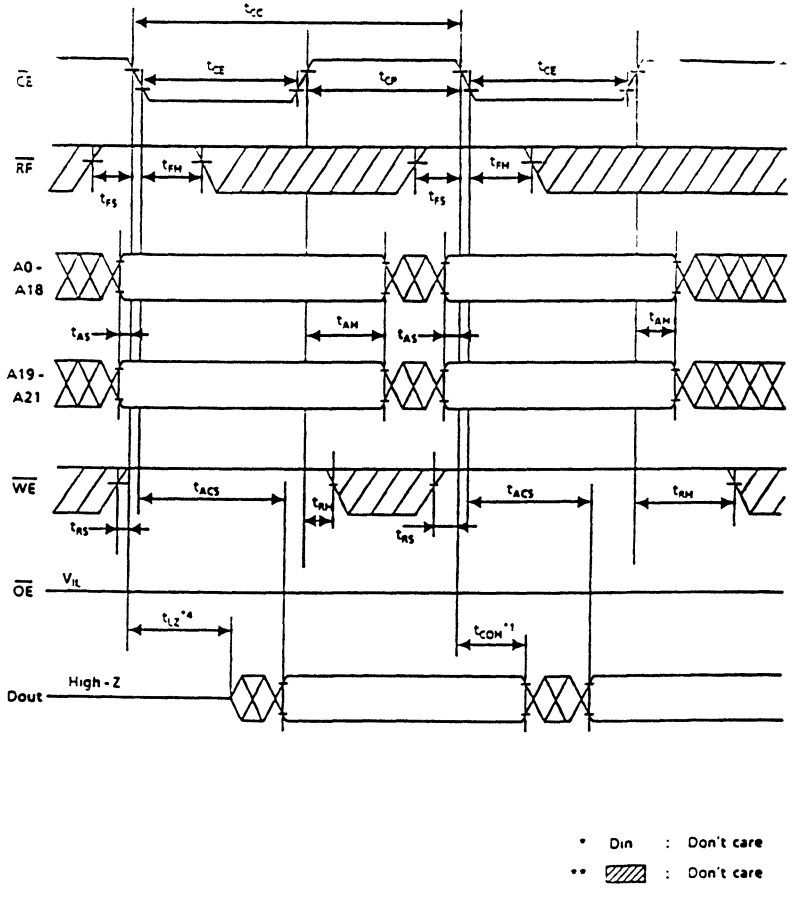
• **Read/Early Write Cycle**



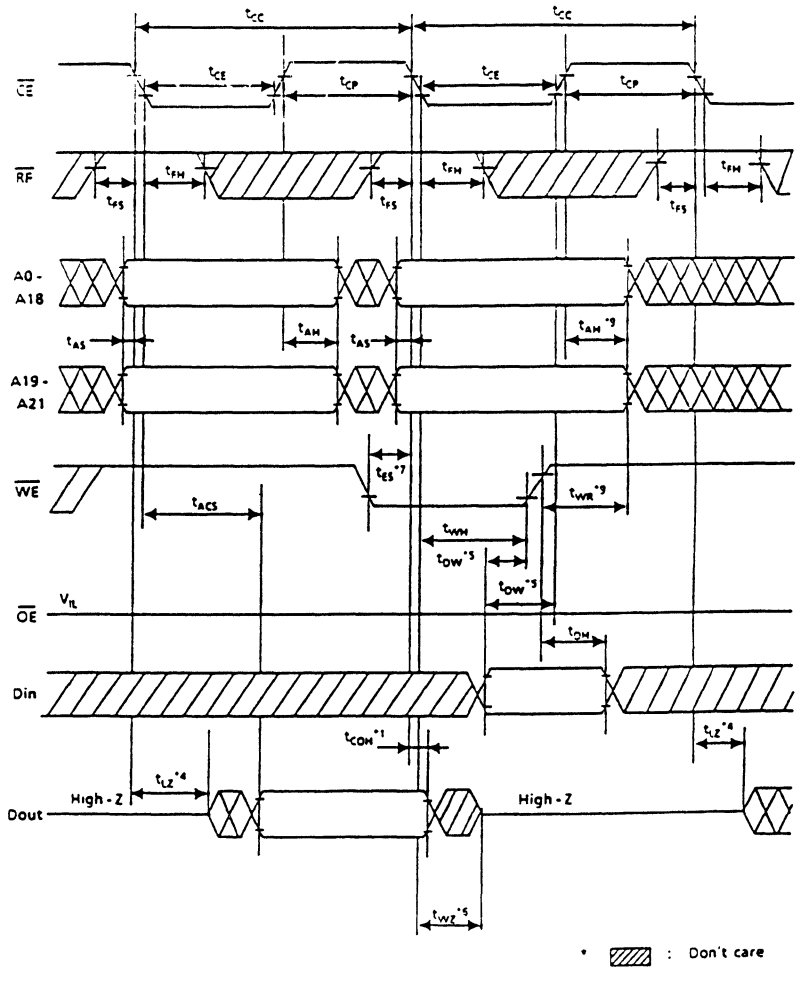
• **Read/Delayed Write Cycle**



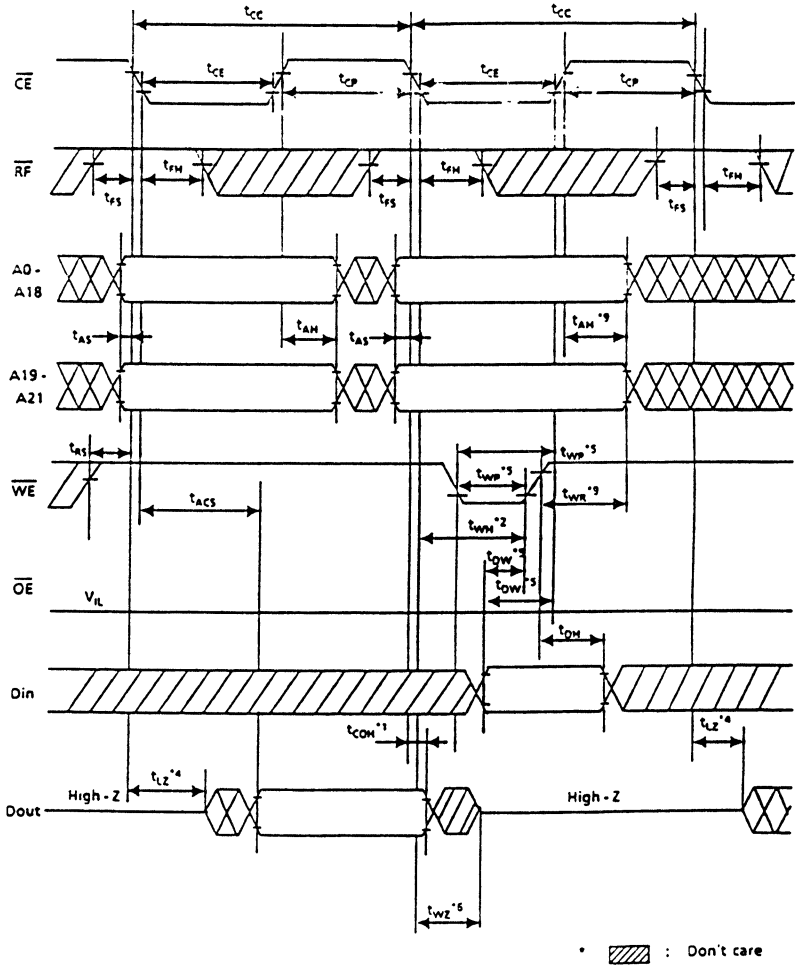
• **Read/Read Cycle ($\overline{OE}$ = V_{IL})**



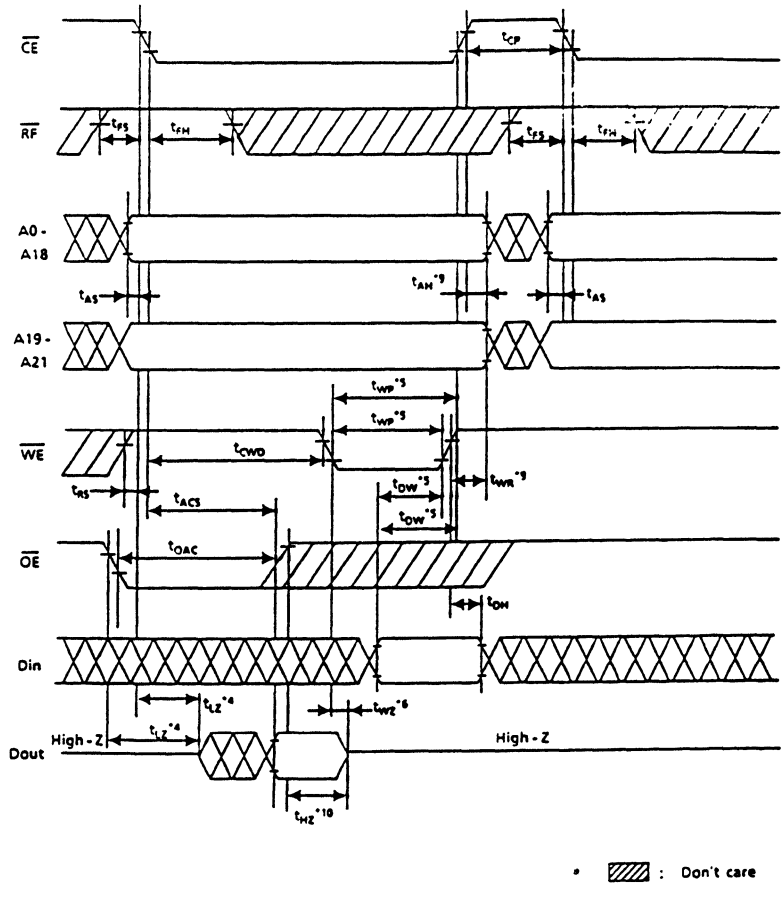
• **Read/Early Write Cycle ($\overline{OE}$ = V_{IL})**



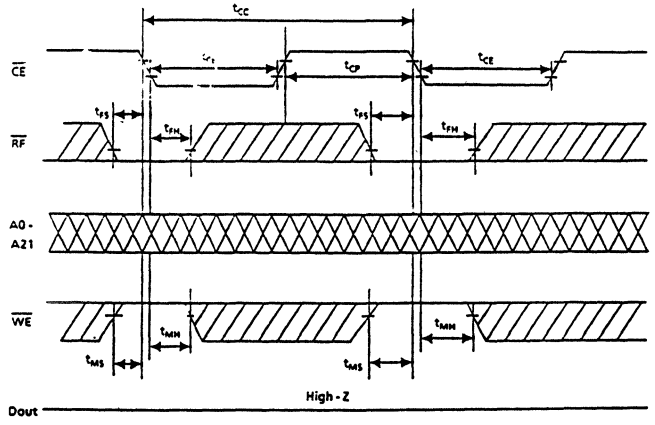
• **Read/Delayed Write Cycle ($\overline{OE}$ = V_{IL})**



• **Read-Modify-Write Cycle**



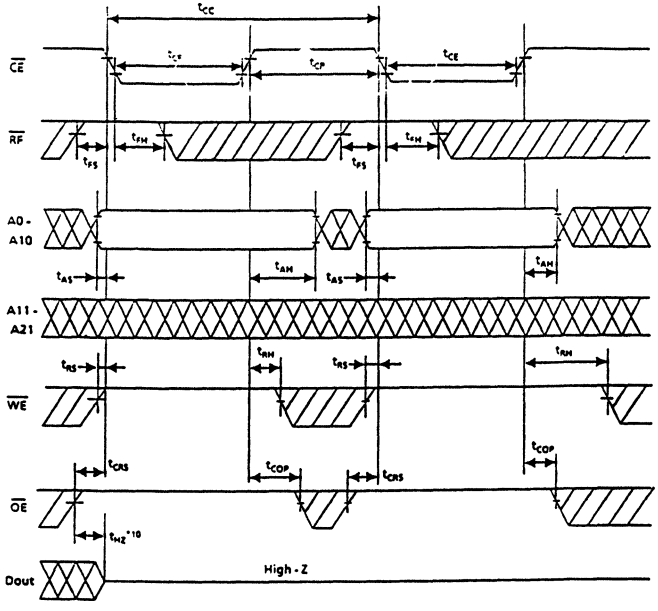
• Automatic Refresh Cycle



* A0 - A19 : Don't care
** $\overline{OE}$, Din : Don't care
*** ▨ : Don't care

0079-12

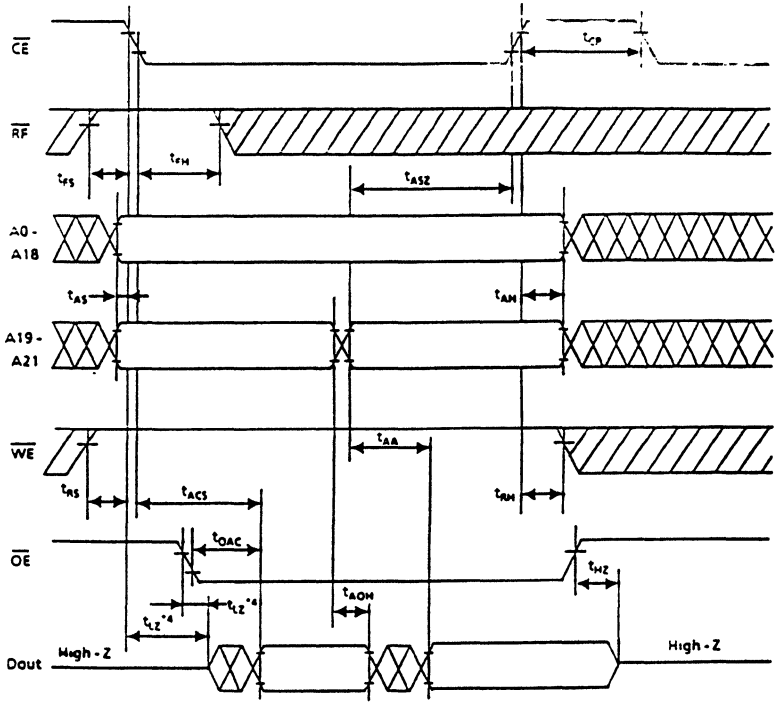
• $\overline{CE}$ Refresh Cycle



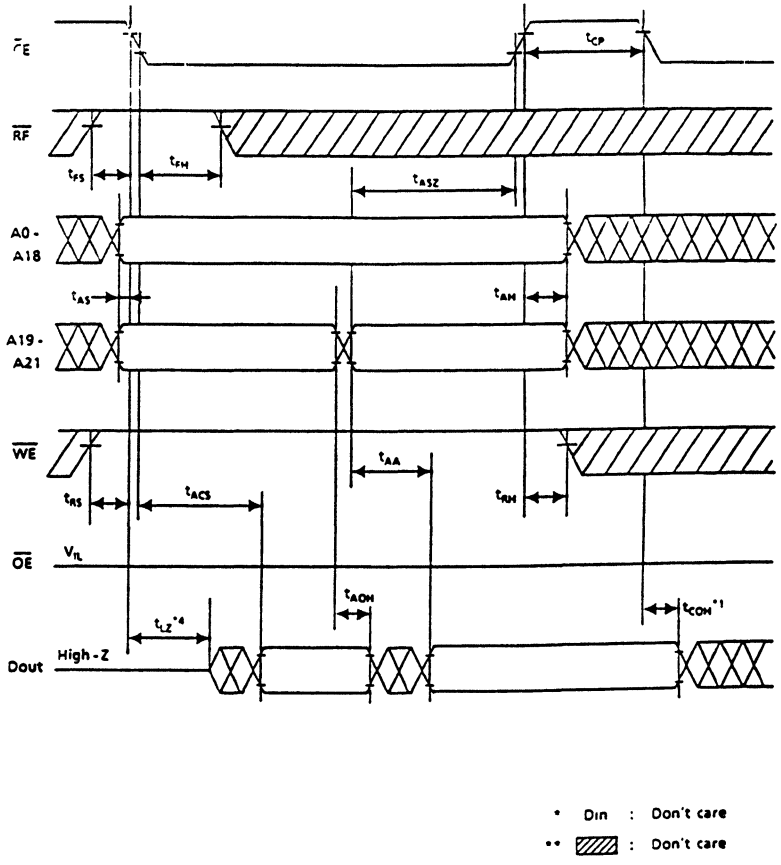
* Din : Don't care
** ▨ : Don't care

0079-13

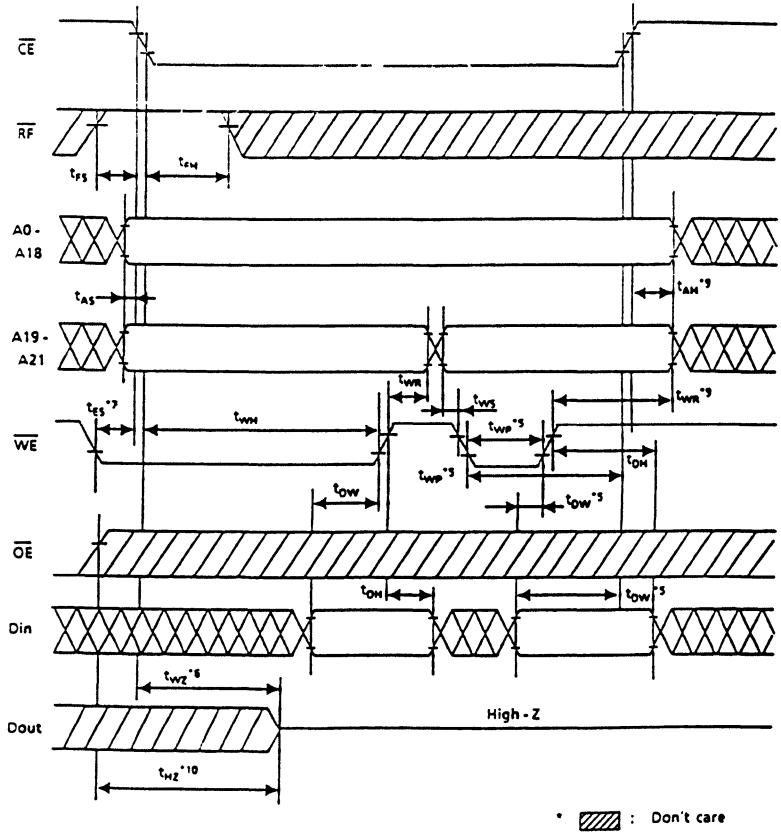
• **Static Column Mode Read Cycle**



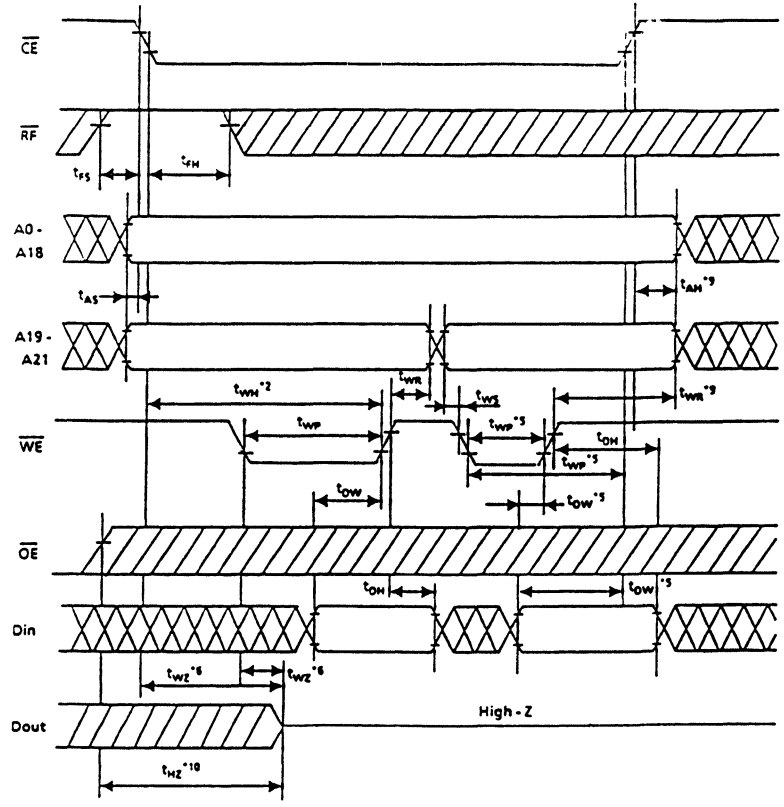
• Static Column Mode Read Cycle ($\overline{OE}$ = V_{IL})



• **Static Column Mode Write Cycle*8 (1st Cycle = Early Write Cycle)**



• **Static Column Mode Write Cycle*8 (1st Cycle = Delayed Write Cycle)**



HM574400 Series — Preliminary

1,048,576-Word x 4-Bit High Speed Dynamic Random Access Memory

■ DESCRIPTION

The Hitachi HM574400 is a super high speed dynamic RAM organized 1,048,576-word x 4-bit. HM574400 has realized higher density, higher performance and various functions by employing 0.89 μm Bi-CMOS technology and some new Bi-CMOS circuit design technologies. The HM574400 offers 2-bit static column mode as a high speed access mode.

■ FEATURES

- Single 5V (±10%)
- High Speed
  - Access Time .....35 ns/40 ns/45 ns (max)
- 2048 Refresh Cycles .....(16 ms)
- 2 Variations of Refresh
  - $\overline{CE}$ Refresh
  - Automatic Refresh
- 2 Bits Static Column Mode

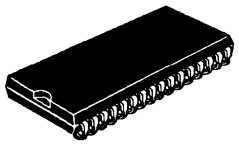
■ ORDERING INFORMATION

Part No.	Access Time	Package
HM574400JP-35	35 ns	300 mil 32-pin
HM574400JP-40	40 ns	Plastic SOJ
HM574400JP-45	45 ns	(CP-32D)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{10}	Address Input for $\overline{CE}$ Refresh
A_{11}–A_{18}	Address Input
A_{19}	Address Input for Static Column Mode
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Read/Write Enable
I/O_1–I/O_4	Data-in/Data-out
RF	Refresh Control
V_{CC}	Power (+5V)
V_{SS}	Ground

HM574400JP Series

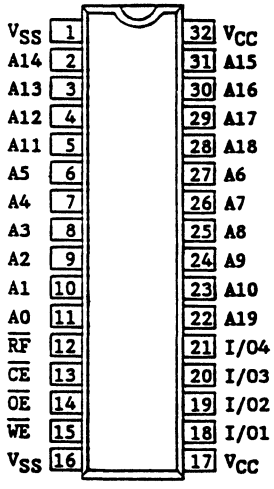


3DCP32D

(CP-32D)

■ PIN OUT

HM574400JP Series



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_T	0.8	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1, 2

Notes: 1. All voltage referenced to V_{SS}.
2. The device will withstand undershoots to the − 2.0V level with a maximum pulse width of 20 ns at the − 1.5V level. (See Figure 1.)

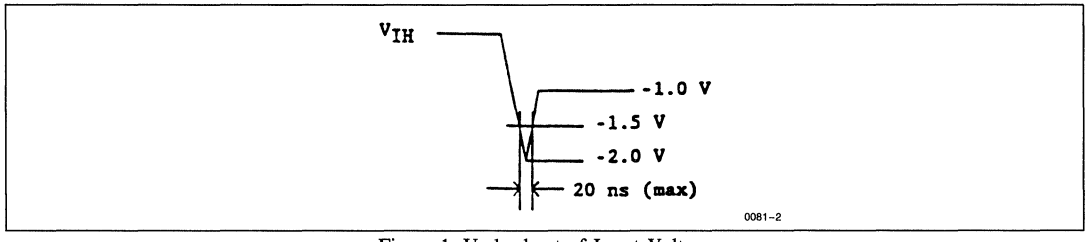


Figure 1. Undershoot of Input Voltage

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM574400-35		HM574400-40		HM574400-45		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Normal Operating Current	I_{CCA}	TBD	TBD	TBD	TBD	TBD	TBD	mA		1
Refresh Current	I_{CCR}	TBD	TBD	TBD	TBD	TBD	TBD	mA		1
Standby Current	I_{CCS}	—	5	—	5	—	5	mA		
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	$0V < V_{in} < 7V$	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	μA	$0V < V_{out} < 7V$, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 4 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 8 mA	

Note: 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter		Symbol	Typ	Max	Unit	Note
Input Capacitance	Address, Data-in	C_{in1}	—	5	pF	1
	Clock	C_{in2}	—	5	pF	1
Output Capacitance (Data-in, Data-out)		$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{OE}$, $\overline{CE}$ = V_{IH} to disable D_{out}.

• **AC Characteristics**[1] (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Test Conditions

Input Pulse Levels: V_{IH} = 3.0V, V_{IL} = 0V
Transition Time: t_T = 3 ns
Input Timing Reference Levels: High = 2.4V, Low = 0.8V (See Figure 2.)
Output Timing Reference Levels: High = 2.4V, Low = 0.4V
Output Load: See Figure 3.

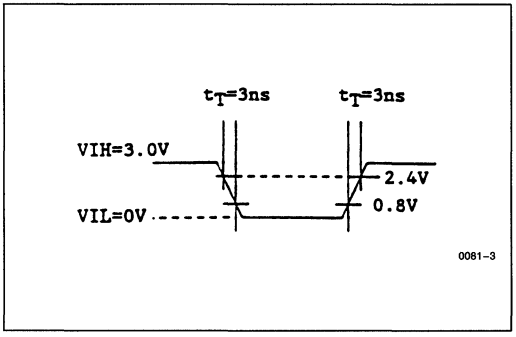


Figure 2. Input Pulse

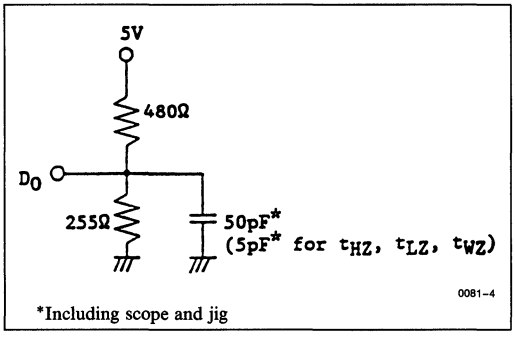


Figure 3. Output Load

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM574400-35		HM574400-40		HM574000-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read/Write Cycle Time	t_{CC}	70	—	80	—	90	—	ns	
$\overline{CE}$ Pulse Width	t_{CE}	35	5000	40	5000	45	5000	ns	
$\overline{CE}$ Precharge Time	t_{CP}	29	—	34	—	39	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Address Hold Time	t_{AH}	5	—	5	—	5	—	ns	
Transition Time (Rise and Fall)	t_T	1	10	1	10	1	10	ns	
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM574400-35		HM574400-40		HM574400-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{CE}$	t_{ACS}	—	35	—	40	—	45	ns	
Address Access Time	t_{AA}	—	25	—	30	—	30	ns	
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	25	—	25	ns	
Setup Time on Read	t_{RS}	0	—	0	—	0	—	ns	
Hold Time on Read	t_{RH}	5	—	5	—	5	—	ns	
$\overline{OE}$ Setup Time	t_{OES}	5	—	5	—	5	—	ns	
$\overline{OE}$ Enable to Output in Low-Z	t_{LZ}	0	—	0	—	0	—	ns	
$\overline{OE}$ Disable to Output in High-Z	t_{HZ}	—	15	—	20	—	20	ns	
Output Hold Time from Address	t_{AOH}	3	—	3	—	3	—	ns	
Output Hold Time from $\overline{CE}$	t_{COH}	0	—	0	—	0	—	ns	
$\overline{CE}$ to $\overline{OE}$ Precharge Time	t_{COP}	10	—	10	—	10	—	ns	

Write Cycle

Parameter	Symbol	HM574400-35		HM574400-40		HM574400-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Data Setup Time	t_{DW}	20	—	25	—	30	—	ns	
Data Hold Time	t_{DH}	5	—	5	—	5	—	ns	
Setup Time on Early Write	t_{ES}	5	—	5	—	5	—	ns	
$\overline{WE}$ Pulse Width	t_{WP}	25	—	30	—	35	—	ns	
Write Hold Time from $\overline{CE}$	t_{WH}	35	—	40	—	45	—	ns	
$\overline{WE}$ Enable to Output in High-Z	t_{WZ}	—	15	—	20	—	20	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	15	—	20	—	20	—	ns	
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	15	—	20	—	20	—	ns	
$\overline{CE}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	0	—	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM574400-35		HM574400-40		HM574400-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{WE}$ Delay Time from $\overline{CE}$	t_{CWD}	35	—	40	—	45	—	ns	

Refresh Cycle

Parameter	Symbol	HM574400-35		HM574400-40		HM574400-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{RF}$ Setup Time	t_{FS}	5	—	5	—	5	—	ns	
$\overline{RF}$ Hold Time	t_{FH}	15	—	15	—	15	—	ns	
Mode Selection Setup Time	t_{MS}	0	—	0	—	0	—	ns	
Mode Selection Hold Time	t_{MH}	15	—	20	—	20	—	ns	
Setup Time on $\overline{CE}$ Refresh	t_{CRS}	15	—	20	—	20	—	ns	

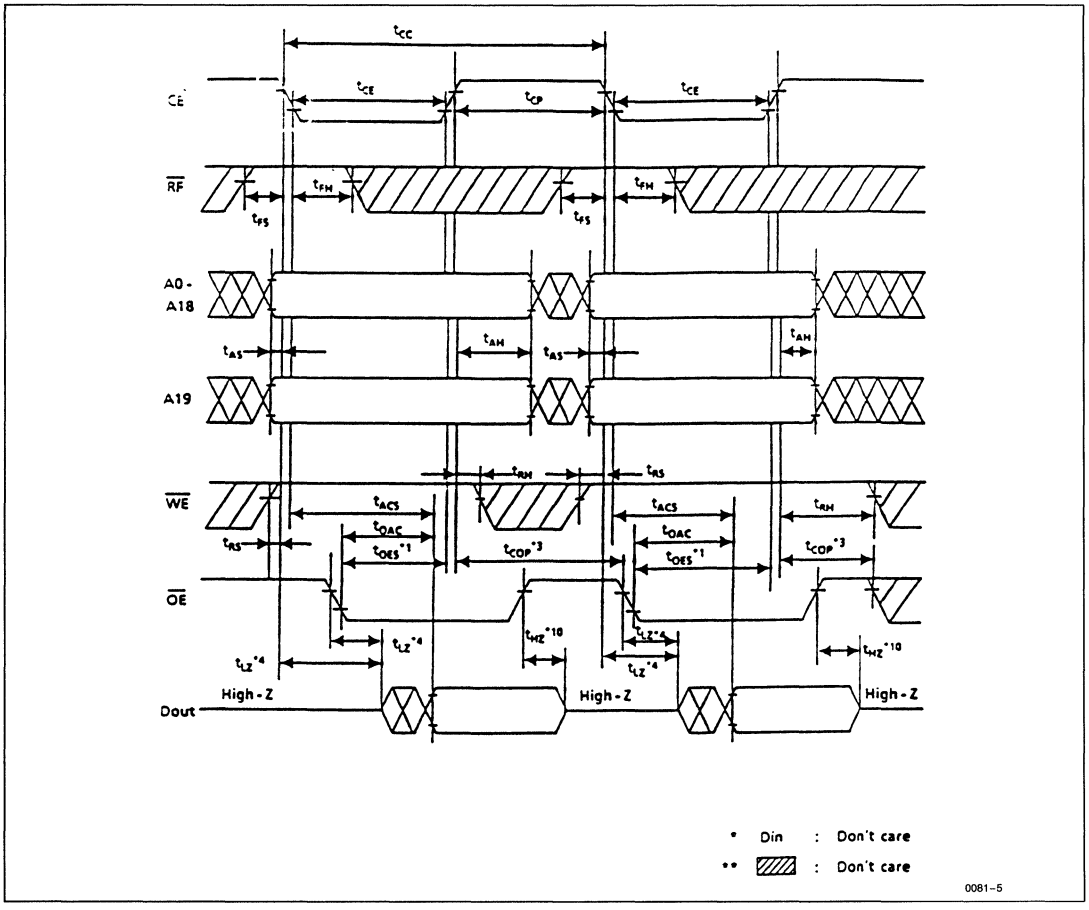
Static Column Mode

Parameter	Symbol	HM574400-35		HM574400-40		HM574400-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Static Column Address Setup Time	t_{ASZ}	20	—	25	—	25	—	ns	
Address Setup Time to $\overline{WE}$	t_{WS}	0	—	0	—	0	—	ns	
Address Hold Time from $\overline{WE}$	t_{WR}	0	—	0	—	0	—	ns	

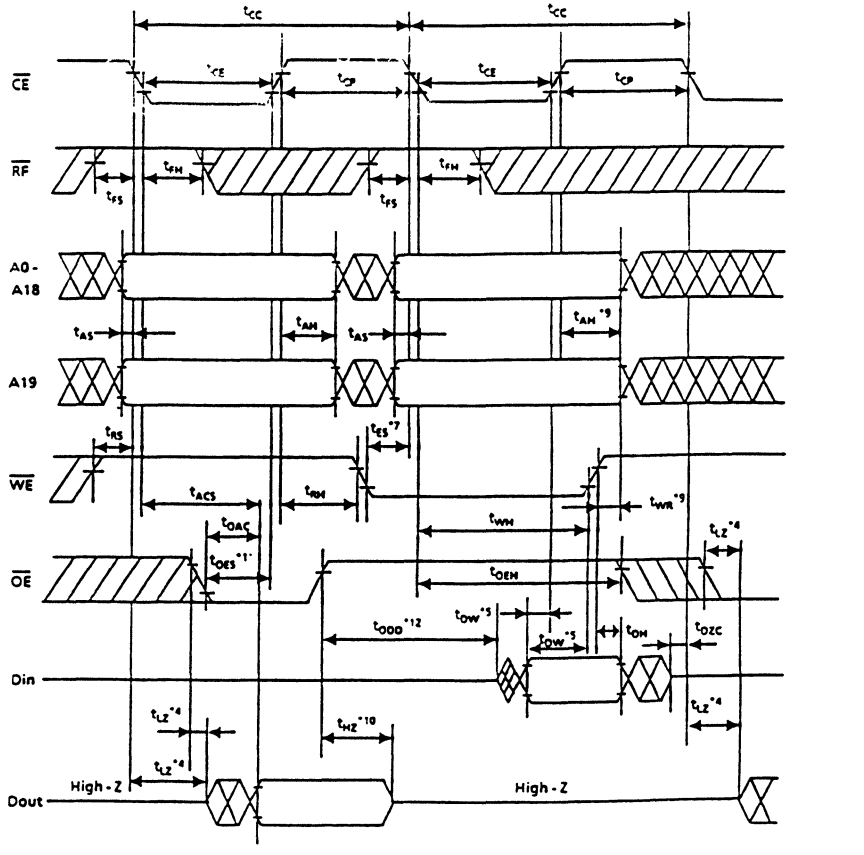
Notes:
1. If $t_{OES} > t_{OES}$ (min) and $\overline{OE}$ is held at low level, D_{out} will be valid until the next negative transition of $\overline{CE}$.
2. Both t_{WH} and t_{WP} must be satisfied for a delayed write cycle.
3. If $t_{COP} < t_{COP}$ (min), D_{out} cannot be guaranteed to be in high impedance.
4. If the negative transition of $\overline{OE}$ occurs before that of $\overline{CE}$, t_{LZ} is controlled by $\overline{CE}$.
5. t_{WP} and t_{DW} are specified by the positive transition of $\overline{CE}$ or $\overline{WE}$ whichever occurs earlier.
6. When $\overline{WE}$ goes low, D_{out} becomes high impedance and is held in this condition to the next cycle. If the negative transition of $\overline{WE}$ occurs before that of $\overline{CE}$, D_{out} is controlled by $\overline{CE}$. t_{WZ} defines the time at which the output achieves the open circuit condition.
7. If $t_{ES} > t_{ES}$(min), the cycle is early write and D_{out} is in high impedance.
8. In static column mode cycles, read operation cannot be performed after write operation.
9. Both t_{AH} and t_{WR} must be satisfied for a write cycle.
10. t_{HZ} defines the time at which the output achieves the open circuit condition.
11. An initial pause of 100 μs is required after power-up, then execute at least eight $\overline{CE}$ refresh cycles.
12. During I/O pins are in the output state, Data-in shall not be applied to I/O pins. So, in all write cycles (early write, delayed write and read-modify-write), $\overline{OE}$ must go to high level to disable the output buffer prior to applying data to the device.
13. In static column mode cycle, there must not be any invalid address inputs for static column mode (A19) which are less than t_{AA}.

■ TIMING WAVEFORMS

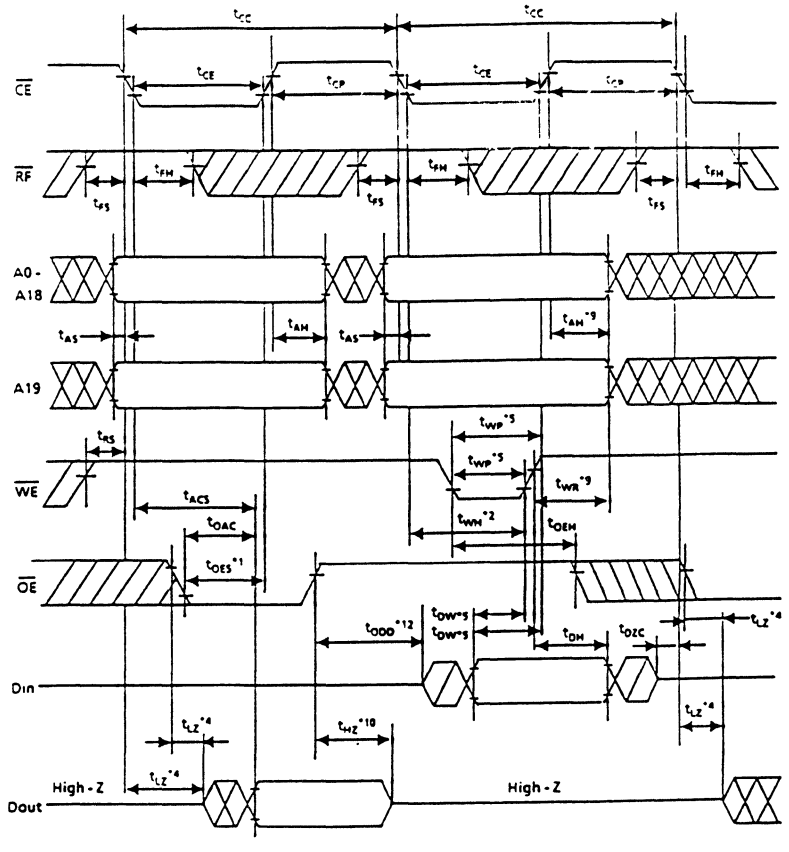
• Read/Read Cycle



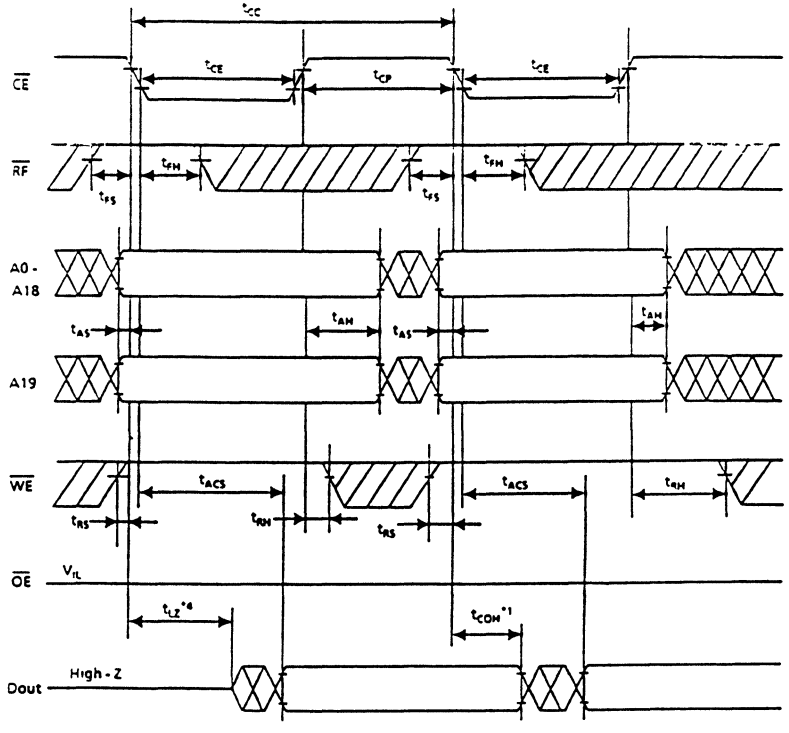
• **Read/Early Write Cycle**



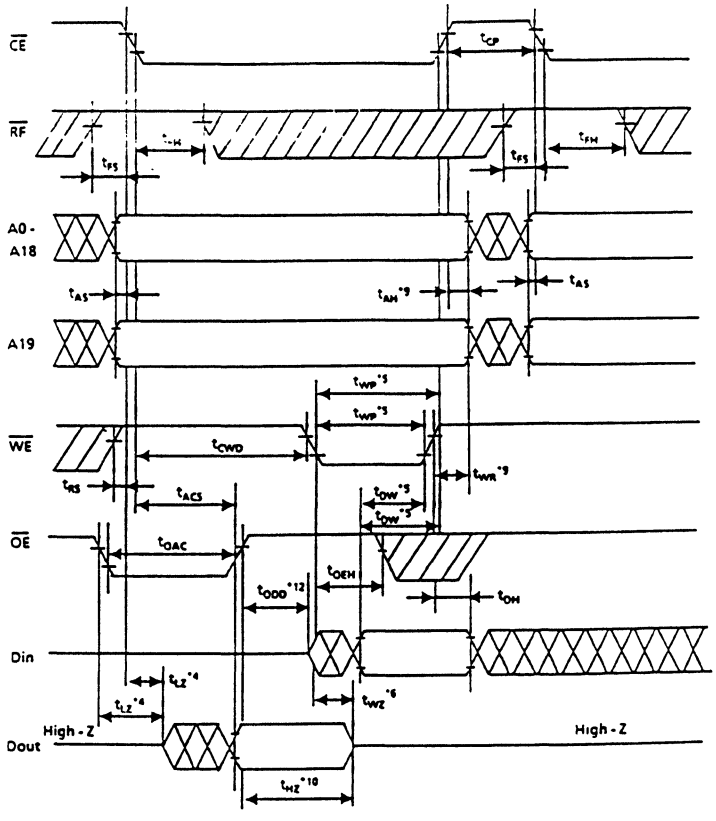
• **Read/Delayed Write Cycle**



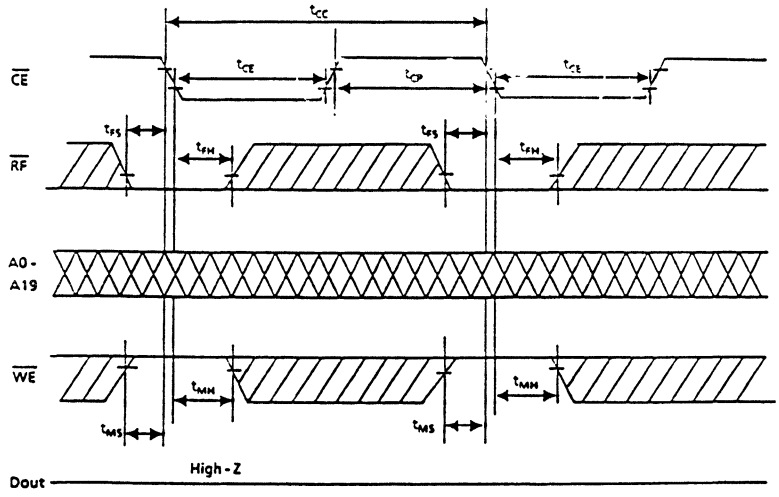
• **Read/Read Cycle ($\overline{OE}$ = V_{IL})**



• **Read-Modify-Write Cycle**



• **Automatic Refresh Cycle**



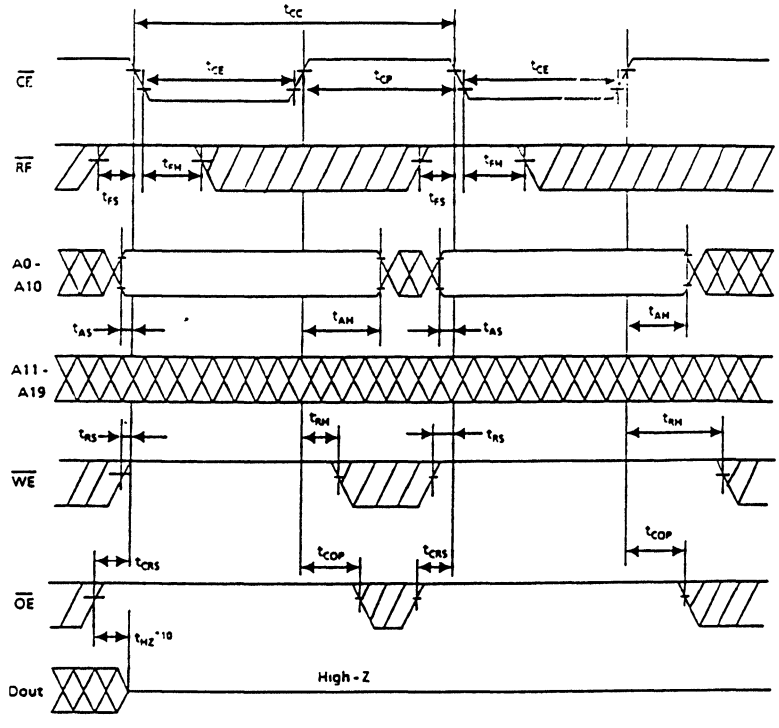
* A0 - A19 : Don't care

** $\overline{OE}$, Din : Don't care

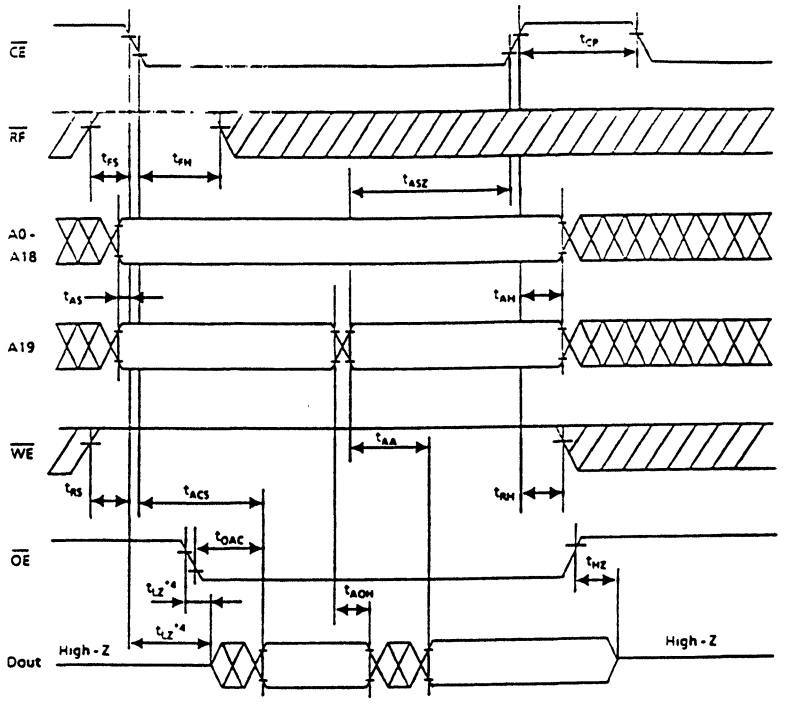
*** ▨ : Don't care

0081-10

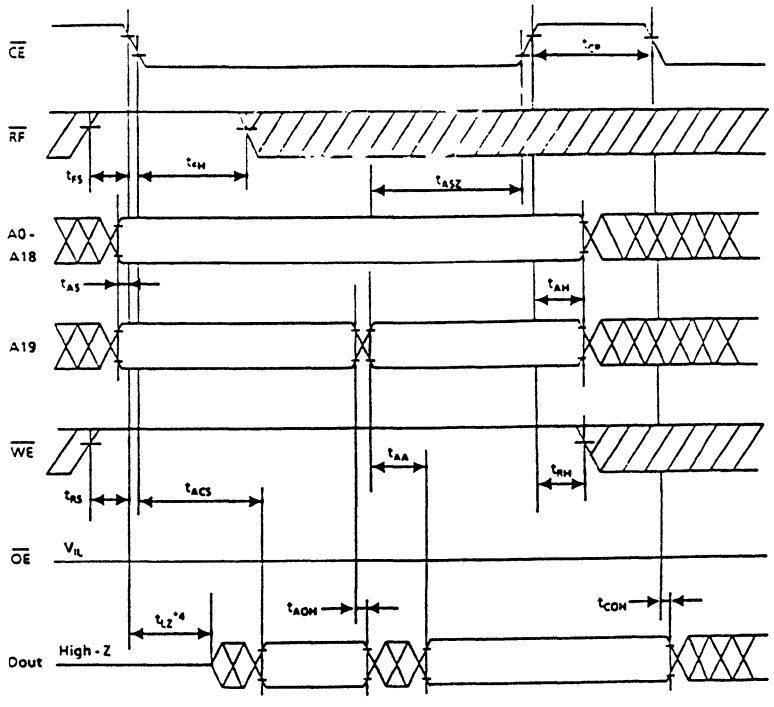
• $\overline{CE}$ Refresh Cycle



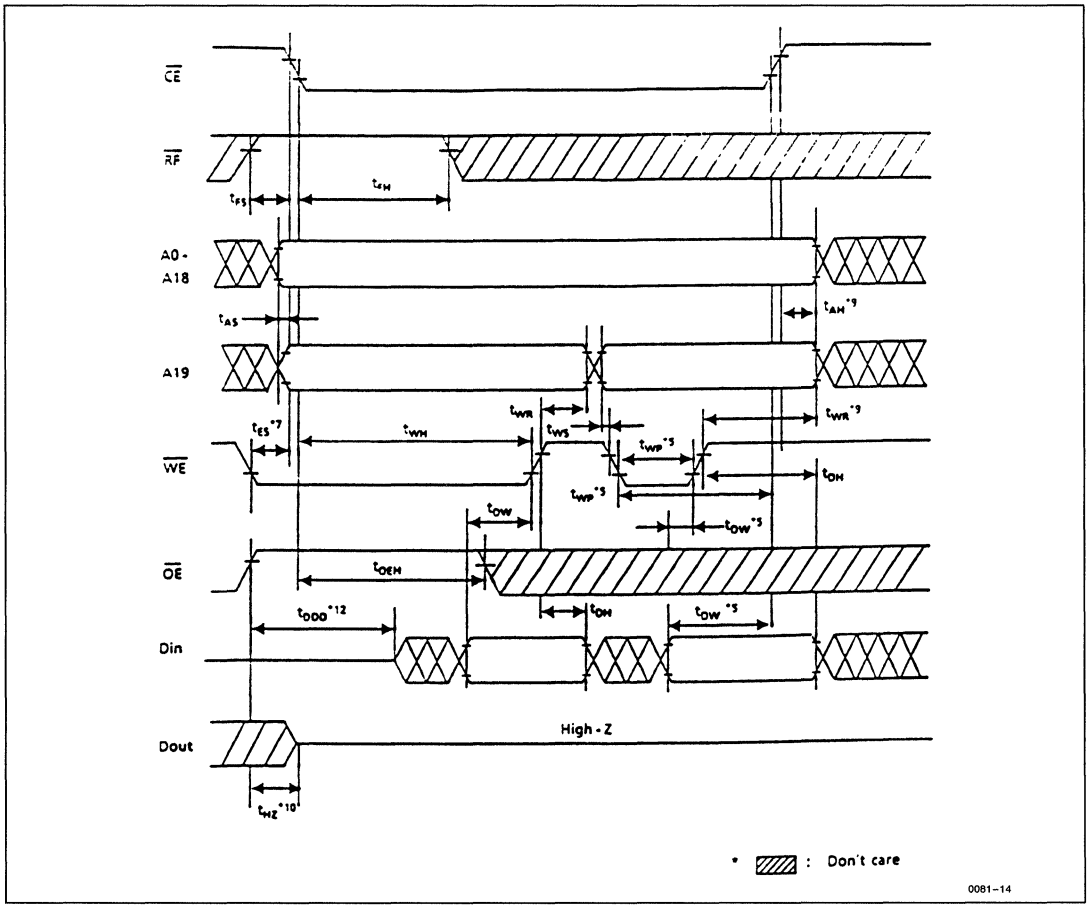
• **Static Column Mode Read Cycle**



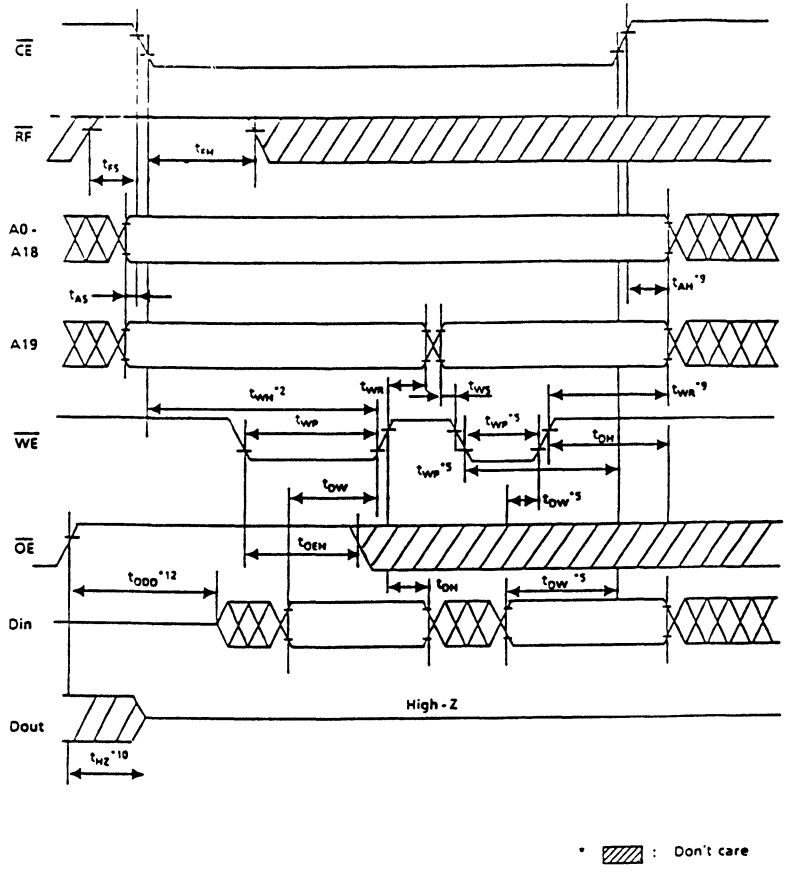
• **Static Column Mode Read Cycle ($\overline{OE}$ = V_{IL})**



• Static Column Mode Write Cycle*8 (1st Cycle = Early Write Cycle)



• **Static Column Mode Write Cycle*8 (1st Cycle = Delayed Write Cycle)**



Section 4
MOS Dynamic RAM Modules

4

HITACHI®

HB56A18 Series

1,048,576-Word x 8-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56A18 is a 1M x 8 dynamic RAM module, mounted eight 1-Mbit DRAM (HM511000JP) sealed in SOJ package. An outline of the HB56A18 is 30-pin single in-line package having Lead types (HB56A18A, HB56A18AT), socket type (HB56A18B). Therefore, the HB56A18 makes high density mounting possible without surface mount technology. The HB56A18 provides common data inputs and outputs. Its module board has decoupling capacitors beneath each SOJ.

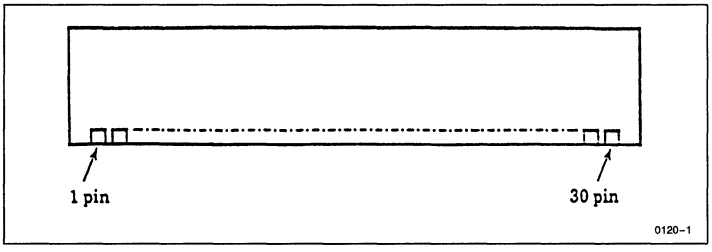
■ FEATURES

- 30-pin Single In-line Package
  - Lead Pitch 2.54mm
- Single 5V (±10%) Supply
- High Speed
  - Access Time ..... 60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode..... 3.96 mW/3.52 mW/3.08 mW/2.64 mW/2.20 mW (max)
  - Standby Mode..... 88 mW (max)
- Fast Page Mode Capability
- 512 Refresh Cycle ..... (8 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

Access Time	Package		
	30-pin SIP Lead Type	30-pin SIP Low Profile Lead Type	30-pin SIMM Socket Type
60 ns	HB56A18A-6H	HB56A18AT-6H	HB56A18B-6H
70 ns	HB56A18A-7H	HB56A18AT-7H	HB56A18B-7H
80 ns	HB56A18A-8A	HB56A18AT-8A	HB56A18B-8A
100 ns	HB56A18A-10A	HB56A18AT-10A	HB56A18B-10A
120 ns	HB56A18A-12A	HB56A18AT-12A	HB56A18B-12A

■ PIN OUT



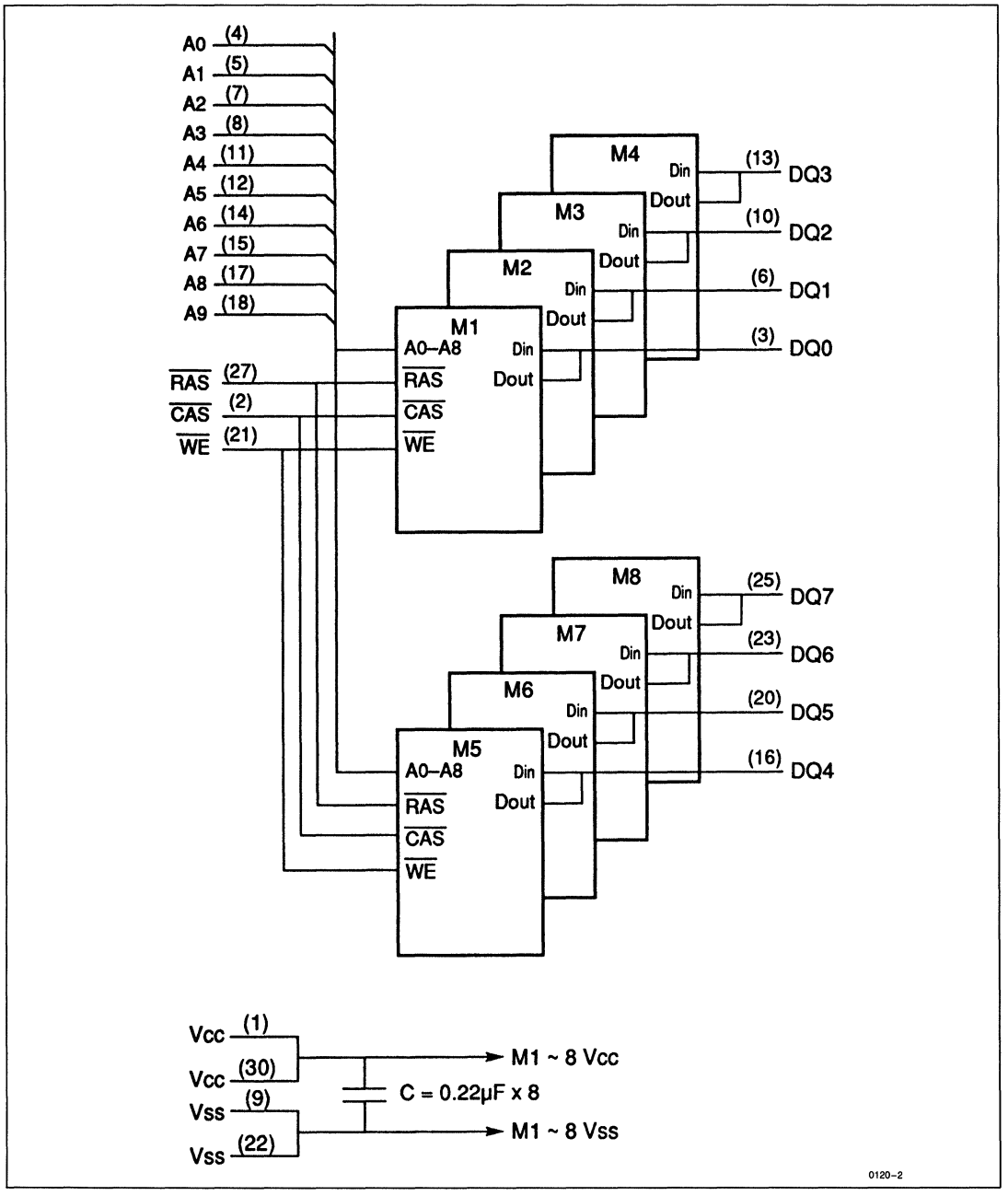
■ PIN DESCRIPTION

Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CAS}$	17	A_8
3	DQ_0	18	A_9
4	A_0	19	NC
5	A_1	20	DQ_5
6	DQ_1	21	$\overline{WE}$
7	A_2	22	V_{SS}
8	A_3	23	DQ_6
9	V_{SS}	24	NC
10	DQ_2	25	DQ_7
11	A_4	26	NC
12	A_5	27	$\overline{RAS}$
13	DQ_3	28	NC
14	A_6	29	NC
15	A_7	30	V_{CC}

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_8	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
DQ_0–DQ_7	Data-in/Data-out
V_{CC}	Power Supply (+ 5V)
V_{SS}	Ground
NC	Non-Connection

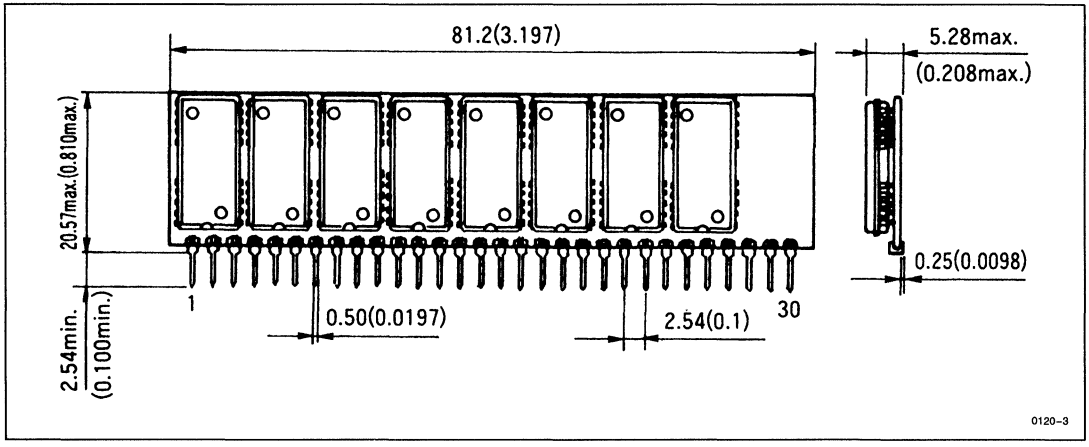
■ BLOCK DIAGRAM



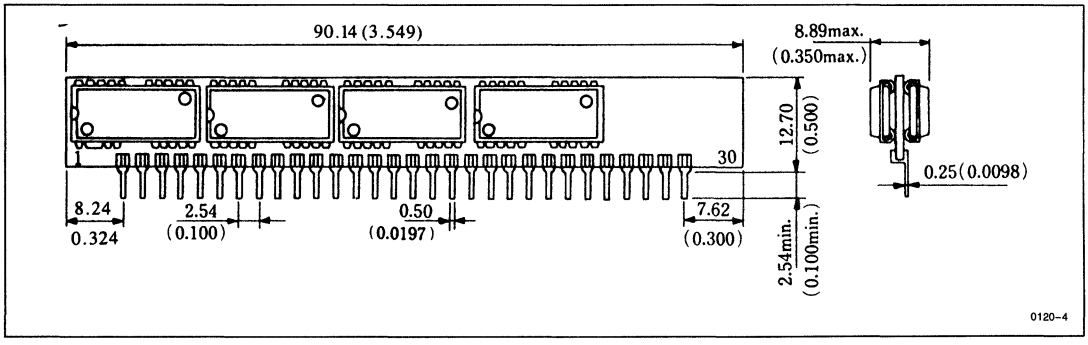
■ PHYSICAL OUTLINE

Unit: mm / inch

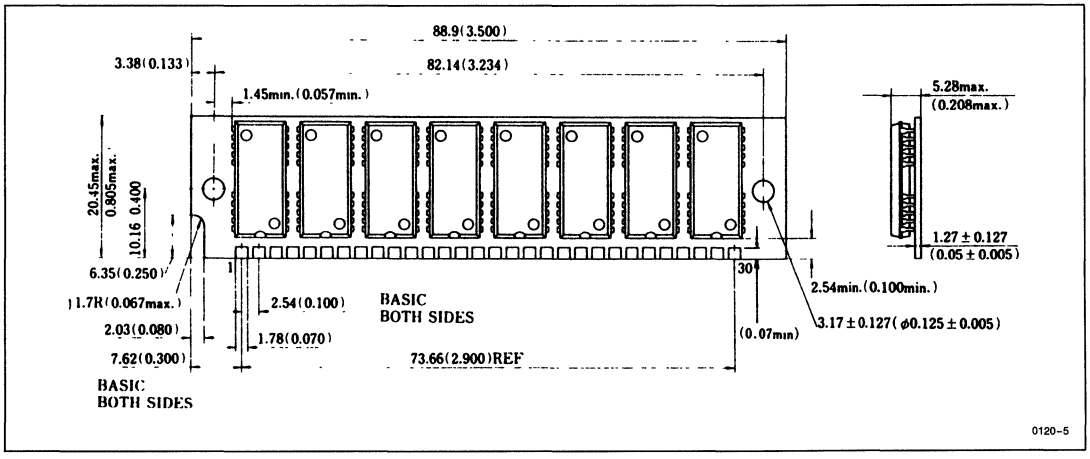
• HB56A18A Series



• HB56A18AT Series



• HB56A18B Series



Note: 1. The plating of the contact finger is solder coat.

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	Input	V_{in}	−1.0 to +7.0	V
	Output	V_{out}	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	8	W
Operating Temperature		T_{opr}	0 to +70	°C
Storage Temperature		T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HB56A18A/AT/B										Unit	Test Conditions	Note
		-6H		-7H		-8A		-10A		-12A				
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	720	—	640	—	560	—	480	—	400	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	16	—	16	—	16	—	16	—	16	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	8	—	8	—	8	—	8	—	8	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	720	—	640	—	480	—	400	—	360	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	40	—	40	—	40	—	40	—	40	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	720	—	640	—	480	—	400	—	320	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	720	—	640	—	400	—	400	—	320	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	55	pF	1
Input Capacitance (Clock)	C_{I2}	—	70	pF	1
Input/Output Capacitance (DQ_0–DQ_7)	$C_{I/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics**

Please show at HM511000H series or HM511000A series about AC Characteristics. But don't use by Delayed Write Cycle, because the HB56A18 provides common data inputs and outputs. Please use by Early Write Cycle. ($t_{WCS} \geq t_{WCS}$ (min)).

HB56C18 Series

1,048,576-Word x 8-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56C18 is a 1M x 8 static column mode dynamic RAM module, mounted eight 1-Mbit DRAM (HM511002JP) sealed in SOJ package. An outline of the HB56C18 is 30-pin single in-line package having Lead types (HB56C18A, HB56C18AT), socket type (HB56C18B). Therefore, the HB56C18 makes high density mounting possible without surface mount technology. The HB56C18 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath each SOJ.

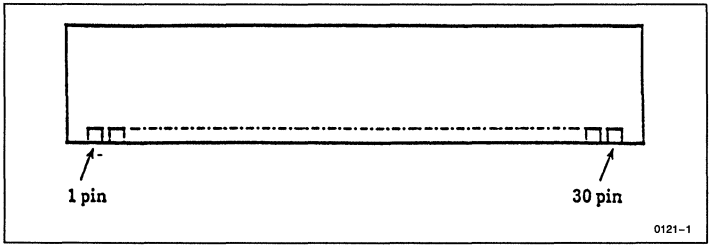
■ FEATURES

- 30-pin Single In-line Package
  - Lead Pitch 2.54mm
- Single 5V (±10%) Supply
- High Speed
  - Access Time ..... 80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode ..... 3080 mW/2640 mW/2200 mW (max)
  - Standby Mode ..... 88 mW (max)
- Static Column Mode Capability
- 512 Refresh Cycle ..... (8 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

Access Time	Package		
	30-pin SIP Lead Type	30-pin SIP Low Profile Lead Type	30-pin SIP Socket Type
80 ns	HB56C18A-8A	HB56C18AT-8A	HB56C18B-8A
100 ns	HB56C18A-10A	HB56C18AT-10A	HB56C18B-10A
120 ns	HB56C18A-12A	HB56C18AT-12A	HB56C18B-12A

■ PIN OUT



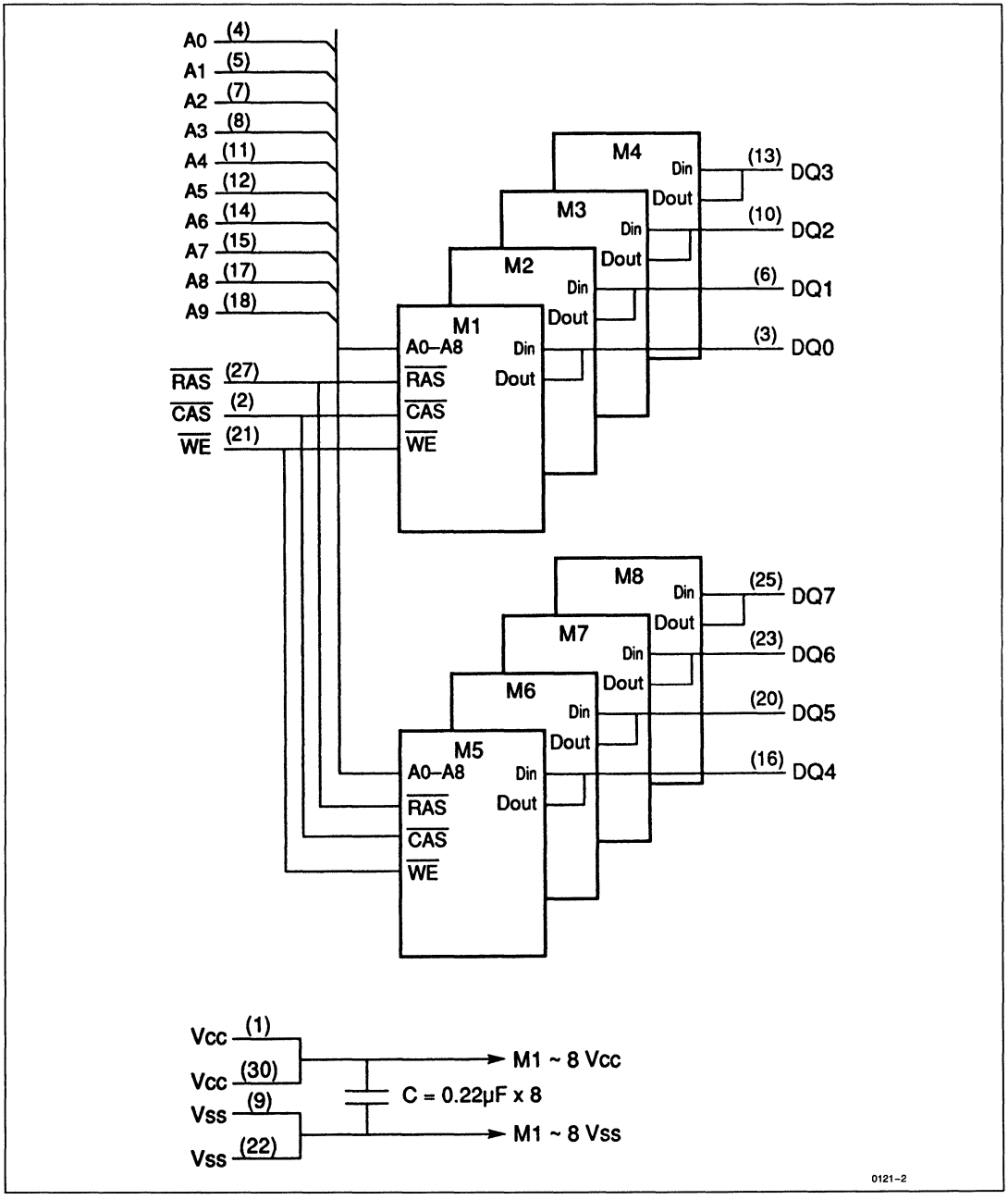
■ PIN DESCRIPTION

Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CAS}$	17	A_8
3	DQ_0	18	A_9
4	A_0	19	NC
5	A_1	20	DQ_5
6	DQ_1	21	$\overline{WE}$
7	A_2	22	V_{SS}
8	A_3	23	DQ_6
9	V_{SS}	24	NC
10	DQ_2	25	DQ_7
11	A_4	26	NC
12	A_5	27	$\overline{RAS}$
13	DQ_3	28	NC
14	A_6	29	NC
15	A_7	30	V_{CC}

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_8	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
$\overline{WE}$	Read/Write Enable
DQ_0–DQ_7	Data-in/Data-out
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	Non-Connection

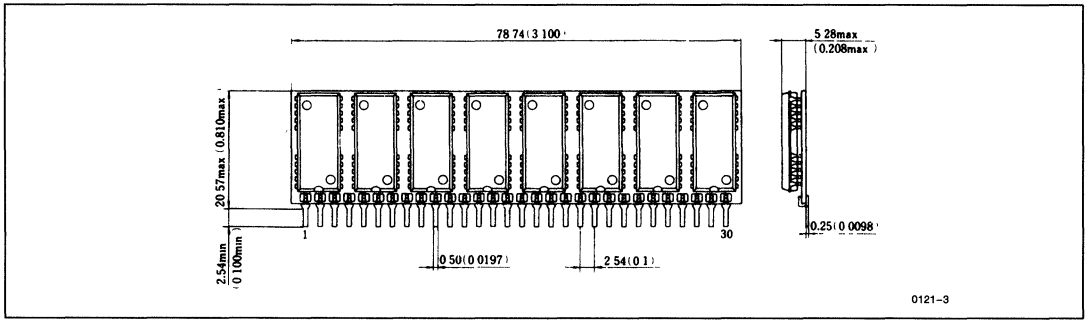
■ BLOCK DIAGRAM



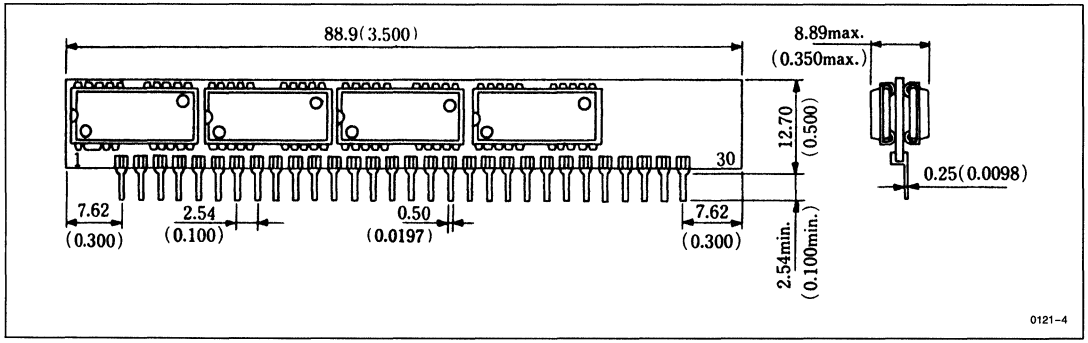
■ PHYSICAL OUTLINE

Unit: mm (inch)

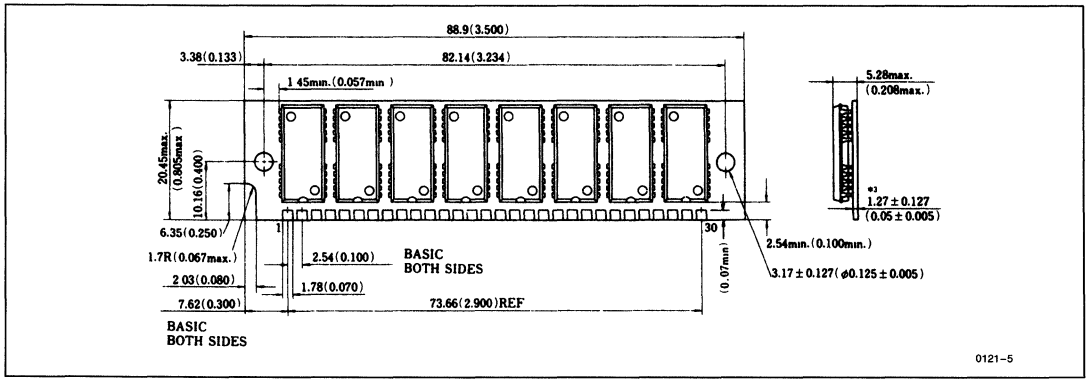
• HB56C18A Series



• HB56C18AT Series



• HB56C18B Series



Note: 1. The plating of the contact finger is solder coat.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	8.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HB56C18A/AT/B						Unit	Test Conditions	Note
		-8A		-10A		-12A				
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	560	—	480	—	400	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	16	—	16	—	16	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	8	—	8	—	8	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	480	—	400	—	360	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	40	—	40	—	40	mA	$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	480	—	400	—	320	mA	t_{RC} = Min	
Static Column Mode Current	I_{CC9}	—	480	—	400	—	320	mA	Static Column Mode t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	55	pF	1
Input Capacitance (Clock)	C_{I2}	—	70	pF	1, 2
Input/Output Capacitance (DQ_0–DQ_7)	$C_{I/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics**

Please show at HM511002H series about AC Characteristics. But don't use by Delayed Write Cycle, because the HB56C18 provides common data inputs and outputs. Please use by Early Write Cycle. ($t_{WCS} \geq t_{WCS}$ (min)).

HB56G18 Series

1,048,576-Word x 8-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56G18 is a 1M x 8 dynamic RAM module, mounted two 4 Mbit DRAM (HM514400AS) sealed in SOJ package. An outline of the HB56G18 is 30-pin single in-line package (socket type).

Therefore, the HB56G18 makes high density mounting possible without surface mount technology. The HB56G18 provides common data inputs and outputs. Its module board has decoupling capacitors beside each SOJ.

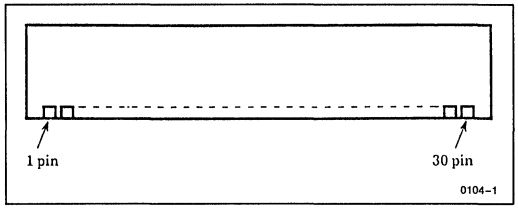
■ FEATURES

- 30-pin Single In-line Package
  - Lead Pitch 2.54mm
- Single 5V (±10%) Supply
- High Speed
  - Access Time ..... 70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode ..... 1100 mW/990 mW/880 mW (max)
  - Standby Mode ..... 22 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles ..... (16 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

Part No.	Access Time	Package	Contact Pad
HB56G18B-7A HB56G18B-8A HB56G18B-10A	70 ns 80 ns 100 ns	30-pin SIP Socket Type	Solder
HB56G18GB-7A HB56G18GB-8A HB56G18GB-10A	70 ns 80 ns 100 ns	30-pin SIP Socket Type	Gold

■ PIN OUT

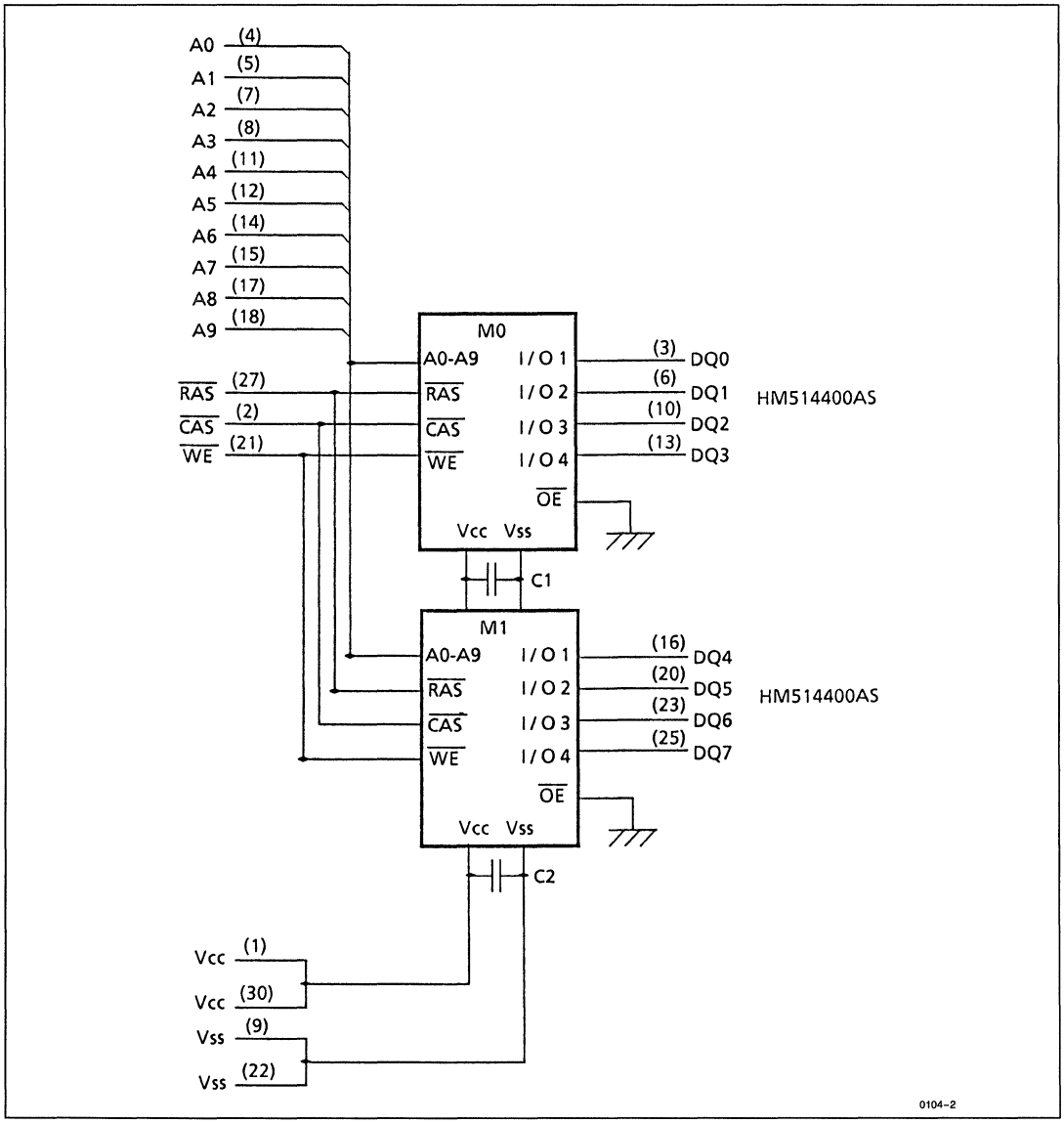


Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CAS}$	17	A_8
3	DQ0	18	A_9
4	A0	19	NC
5	A1	20	DQ_5
6	DQ1	21	$\overline{WE}$
7	A2	22	V_{SS}
8	A3	23	DQ_6
9	V_{SS}	24	NC
10	DQ2	25	DQ_7
11	A4	26	NC
12	A5	27	$\overline{RAS}$
13	DQ3	28	NC
14	A6	29	NC
15	A7	30	

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_9	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
DQ_0–DQ_7	Data-in/Data-out
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	No Connection

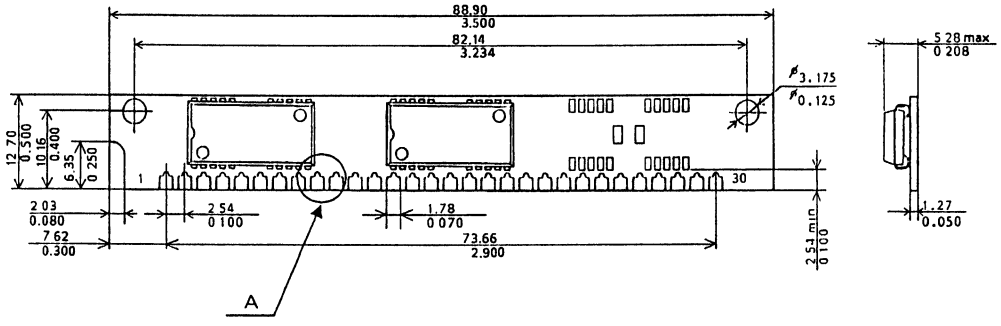
■ Block Diagram



■ PHYSICAL OUTLINE

Unit: mm / inch

• HB56G188/GB Series



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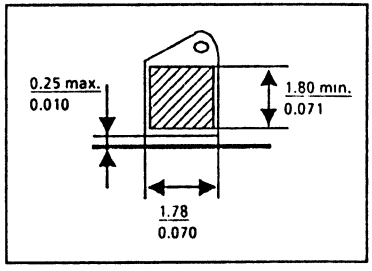
Note: Following the specification of the contact pad.

Part No.	Contact Pad
HB56G18B-XX	Solder
HB56G18GB-XX	Gold

Detail A



0104-4

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input)	V_{in}	− 1.0 to + 7.0	V
	(Output)	V_{out}	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	2.0	W
Operating Temperature		T_{opr}	0 to + 70	°C
Storage Temperature		T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HB56G18B/GB-7A		HB56G18B/GB-8A		HB56G18B/GB-10A		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	200	—	180	—	160	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	4	—	4	—	4	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	2	—	2	—	2	mA	CMOS Interface, $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	200	—	180	—	160	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	10	—	10	—	10	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	200	—	180	—	160	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	200	—	180	—	160	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	30	pF	1
Input Capacitance (Clock)	C_{I2}	—	34	pF	1
Input/Output Capacitance (DQ_{0-7})	$C_{I/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 12]

Read, Write, and Refresh Cycles (Common Parameters)

Parameter	Symbol	HB56G18B/GB-7A		HB56G18B/GB-8A		HB56G18B/GB-10A		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	130	—	150	—	190	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	20	60	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	15	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	15

Read Cycle

Parameter	Symbol	HB56G18B/GB-7A		HB56G18B/GB-8A		HB56G18B/GB-10A		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	3, 4
Access Time from Address	t_{AA}	—	35	—	40	—	45	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	35	—	40	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	20	0	20	0	25	ns	6

Write Cycle

Parameter	Symbol	HB56G18B/GB-7A		HB56G18B/GB-8A		HB56G18B/GB-10A		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	ns	11

Refresh Cycle

Parameter	Symbol	HB56G18B/GB-7A		HB56G18B/GB-8A		HB56G18B/GB-10A		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

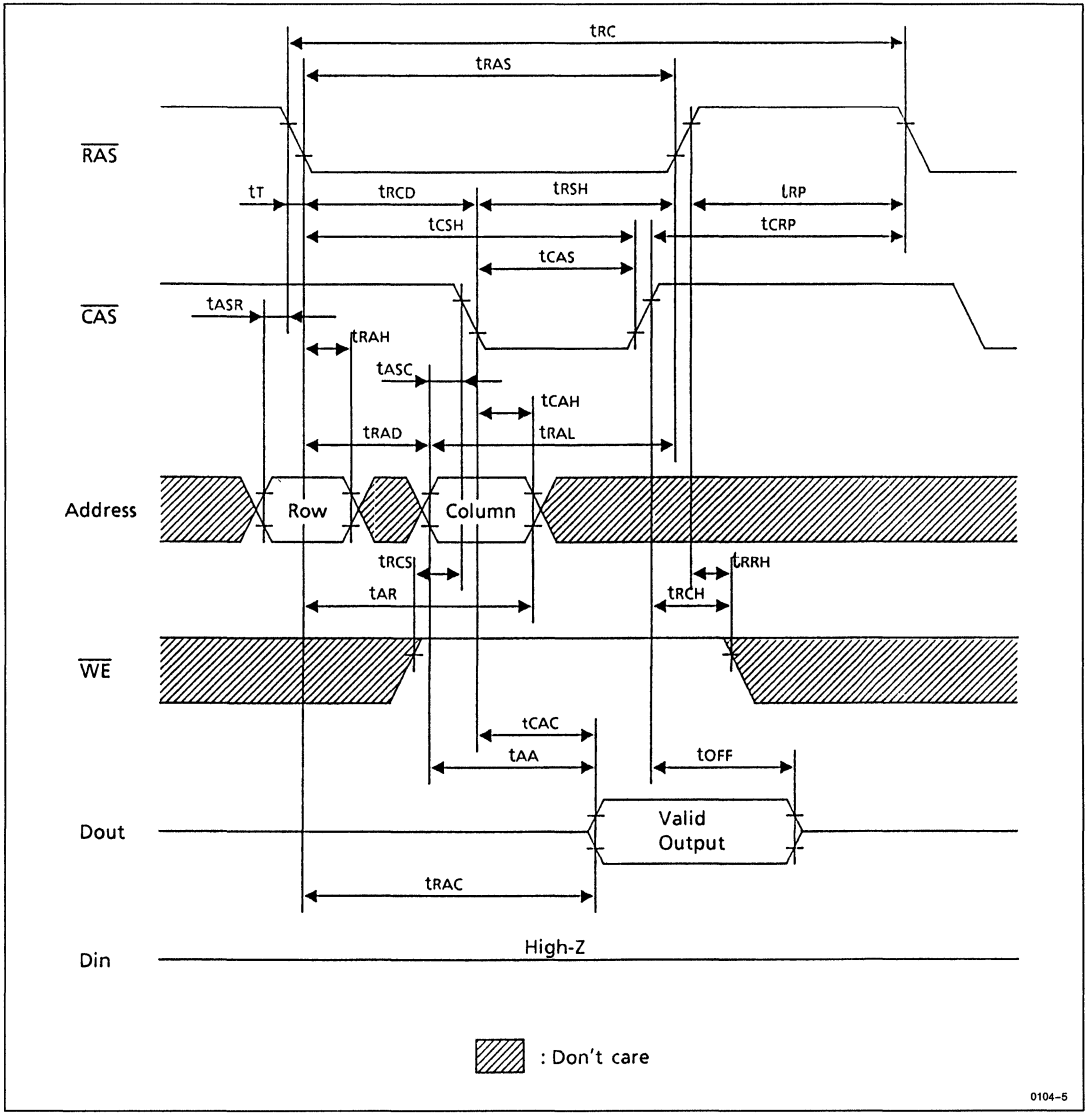
Fast Page Mode Cycle

Parameter	Symbol	HB56G18B/GB-7A		HB56G18B/GB-8A		HB56G18B/GB-10A		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	ns	

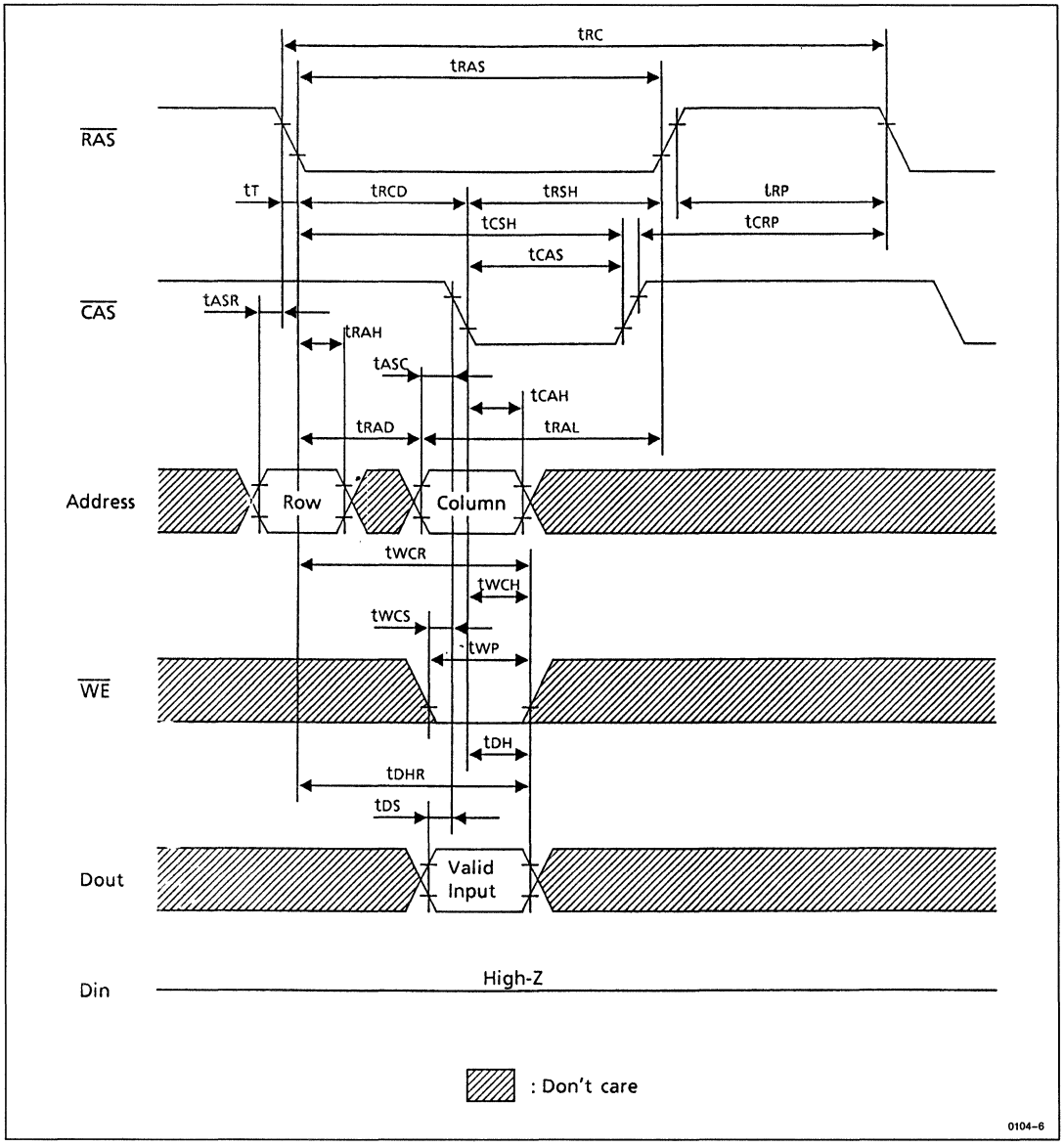
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL load and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min))
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is determined by 1,024 refresh cycles.

■ TIMING WAVEFORMS

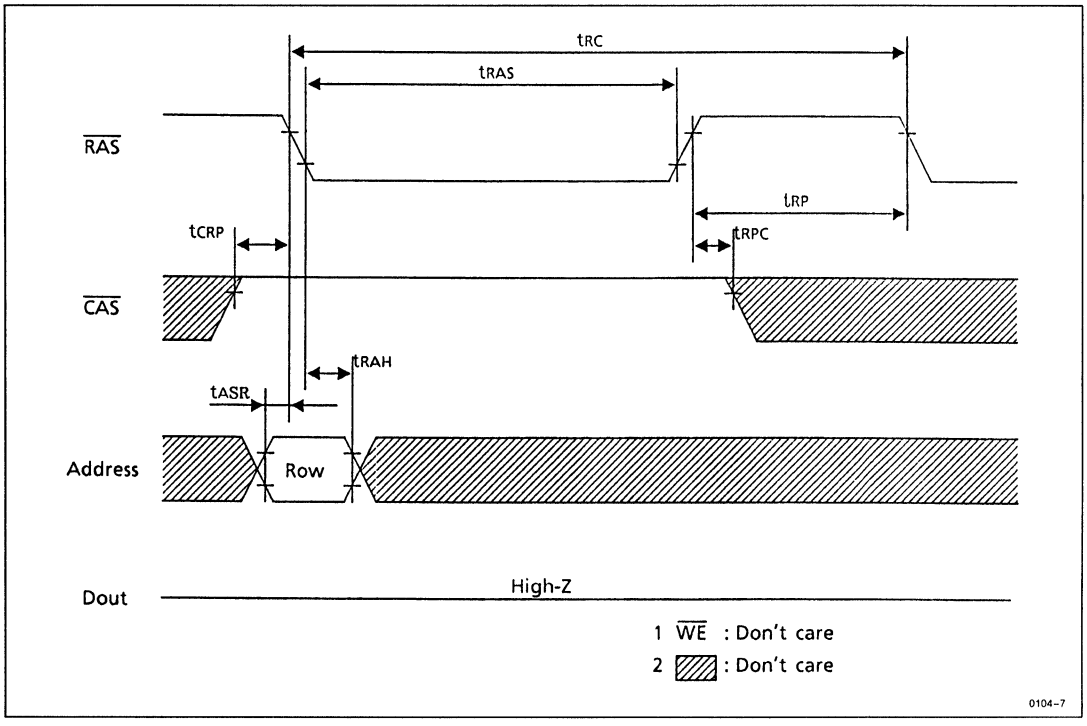
• Read Cycle



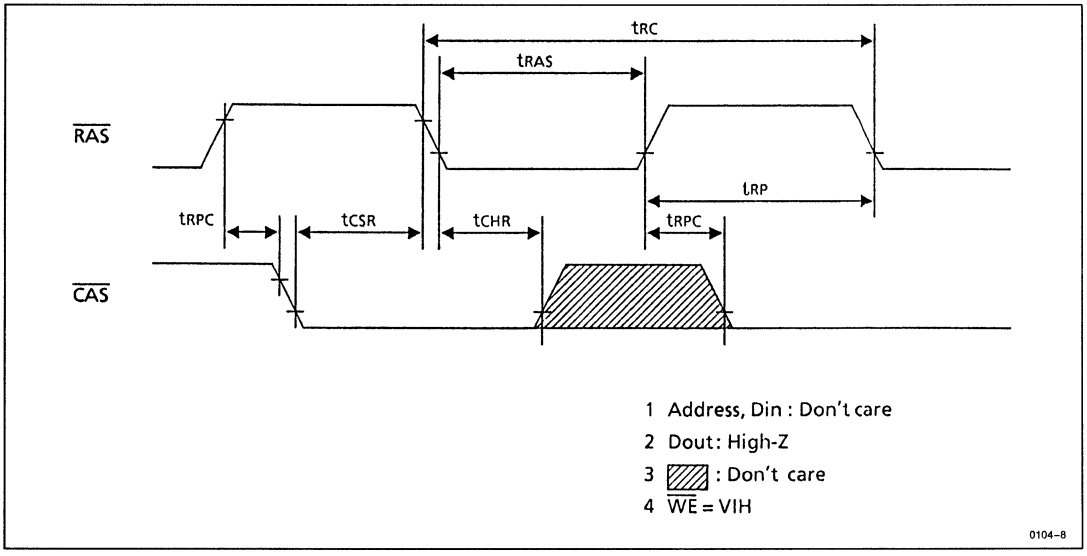
• **Early Write Cycle**



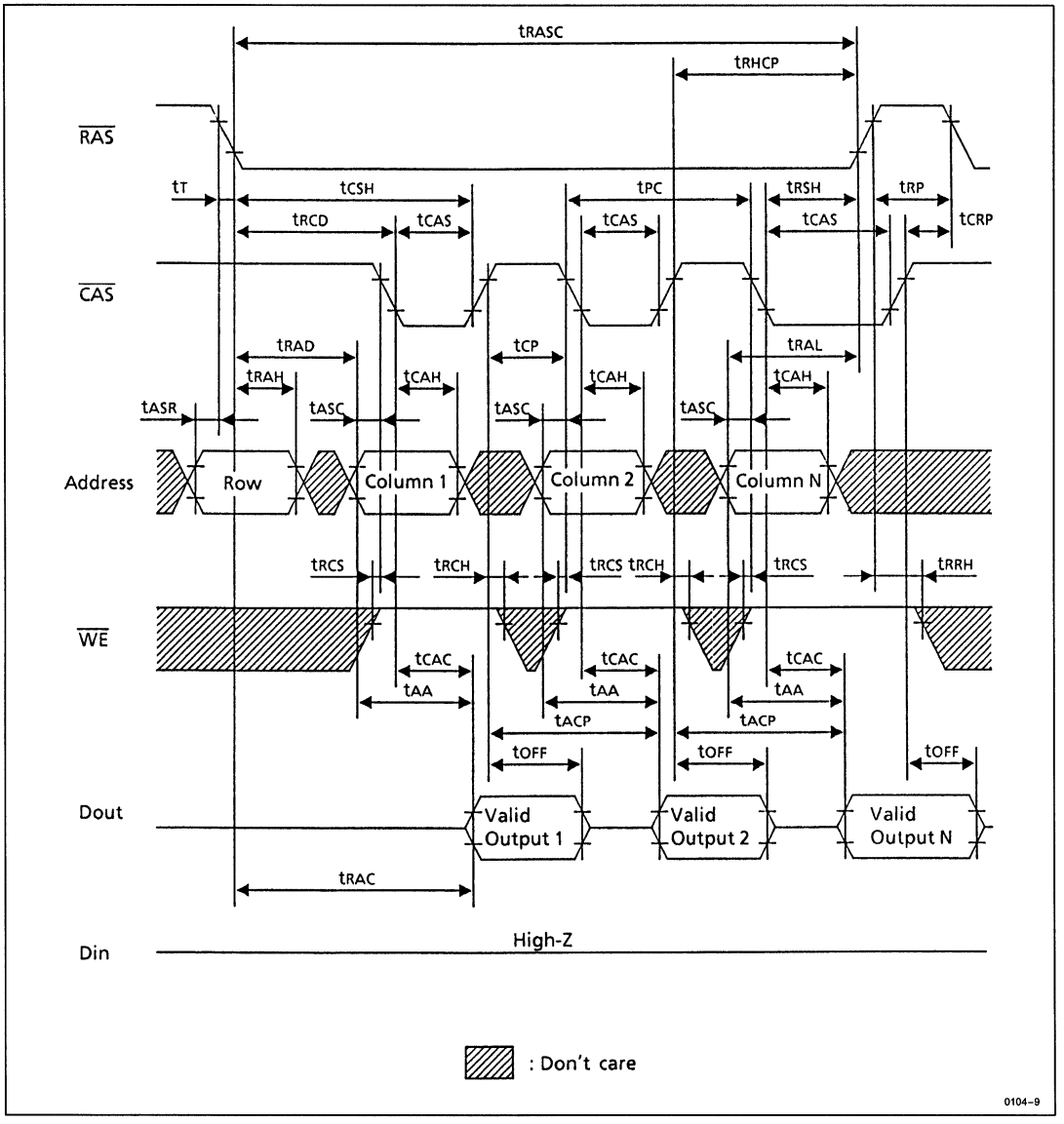
• **$\overline{RAS}$ Only Refresh Cycle**



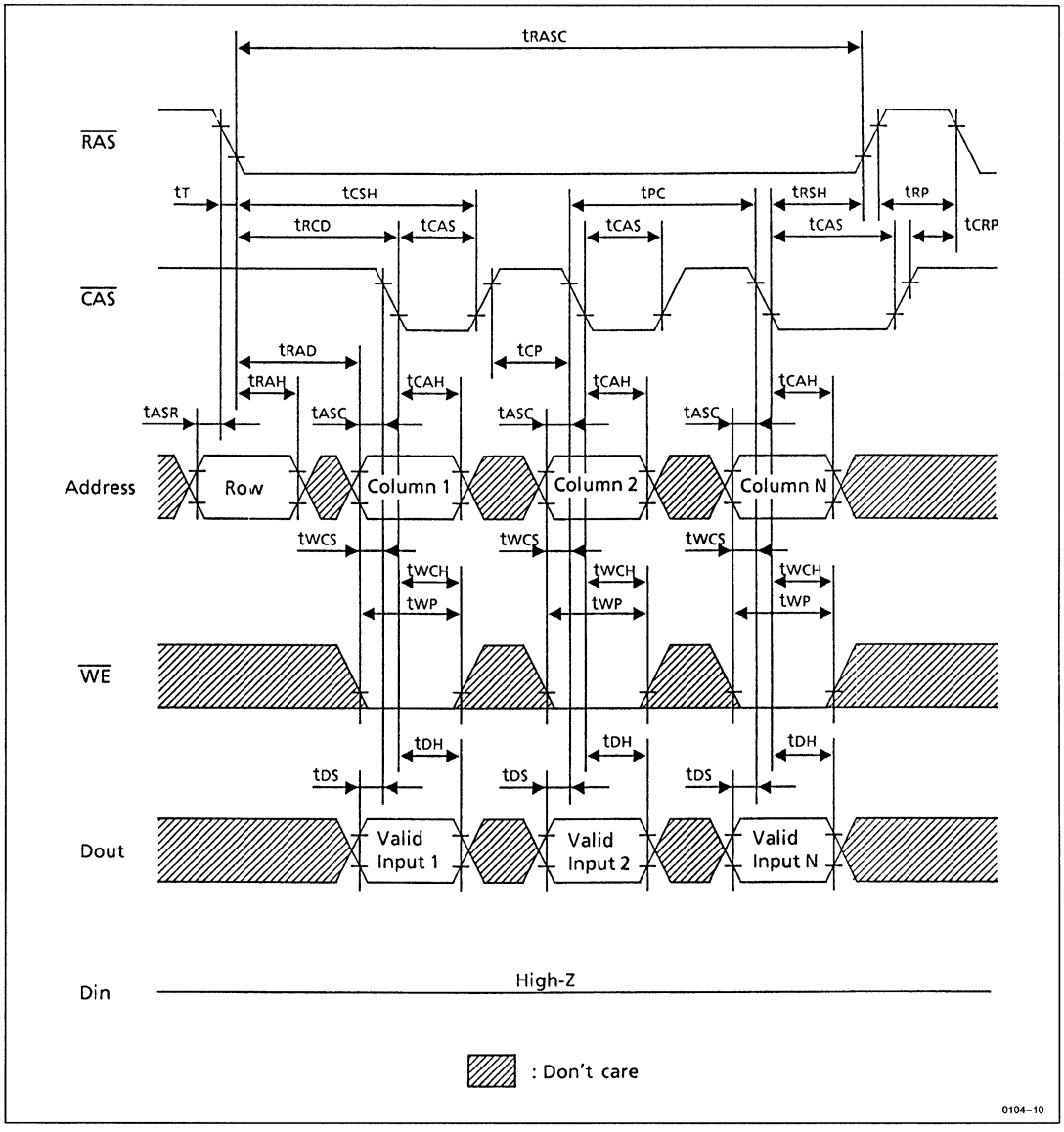
• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**



• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



HB56A48 Series

4,194,304-Word x 8-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56A48 is a 4M x 8 dynamic RAM module, mounted 8 pieces of 4 Mbit DRAM (HM514100AS, HM514100JP) sealed in SOJ package. An outline of the HB56A48 is 30-pin single in-line package. Therefore, the HB56A48 makes high density mounting possible without surface mount technology. The HB56A48 provides common data inputs and outputs.

Decoupling capacitors are mounted beneath each SOJ.

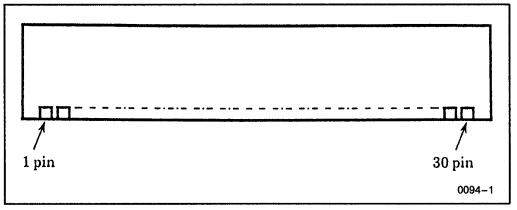
■ FEATURES

- 30-pin Single In-line Package
  - Lead Pitch 2.54mm
- Single 5V (±10%) Supply
- High Speed
  - Access Time .....60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode .....4840 mW/4400 mW/ 3960 mW/3520 mW (max)
  - Standby Mode.....88 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycle .....(16 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- TTL Compatible

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{10}	Address Input
A_0–A_9	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
DQ_0–DQ_7	Data-in/Data-out
V_{CC}	Power Supply (+ 5V)
V_{SS}	Ground
NC	No Connection

■ PIN OUT



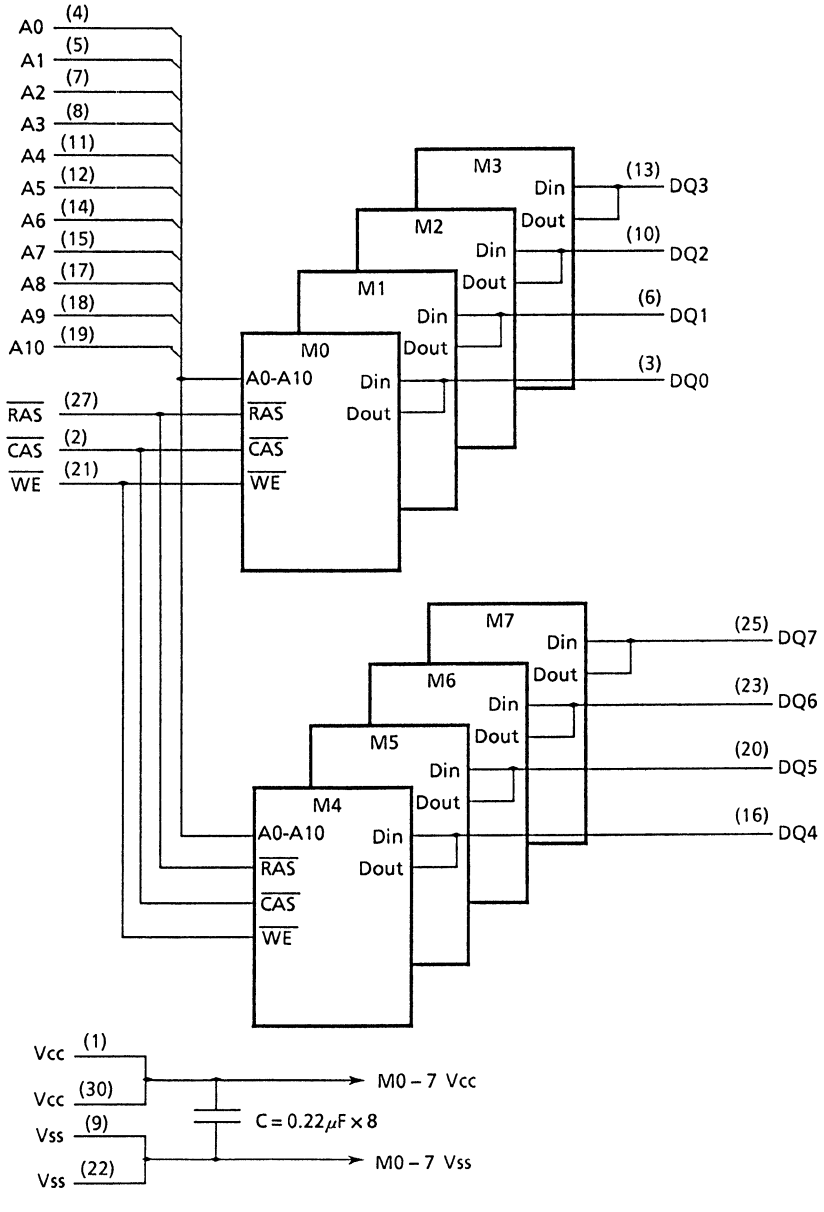
Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CAS}$	17	A_8
3	DQ_0	18	A_9
4	A_0	19	A_{10}
5	A_1	20	DQ_5
6	DQ_1	21	$\overline{WE}$
7	A_2	22	V_{SS}
8	A_3	23	DQ_6
9	V_{SS}	24	NC
10	DQ_2	25	DQ_7
11	A_4	26	NC
12	A_5	27	$\overline{RAS}$
13	DQ_3	28	NC
14	A_6	29	NC
15	A_7	30	V_{CC}

■ ORDERING INFORMATION

Access Time	Package					
	30-pin [1] SIP Socket Type	30-pin [1] SIP Socket Type	30-pin SIP Lead Type	30-pin SIP Lead Type	30-pin SIP Low Profile Lead Type	30-pin SIP Low Profile Lead Type
	0.945 Inch Height	0.805 Inch Height	0.989 Inch Height	0.810 Inch Height	0.591 Inch Height	0.500 Inch Height
60 ns	—	HB56A48BR/GBR-6A	—	HB56A48AR-6A	—	HB56A48ATR-6A
70 ns	—	HB56A48BR/GBR-7A	—	HB56A48AR-7A	—	HB56A48ATR-7A
80 ns	HB56A48B/GB-8	HB56A48BR/GBR-8A	HB56A48A-8	HB56A48AR-8A	HB56A48AT-8	HB56A48ATR-8A
100 ns	HB56A48B/GB-10	HB56A48BR/GBR-10A	HB56A48A-10	HB56A48AR-10A	HB56A48AT-10	HB56A48ATR-10A

Note: 1. Following the specification of the contact pad.
HB56A48B-XX, HB56A48BR-XX: solder
HB56A48GB-XX, HB56A48GBR-XX: gold

■ BLOCK DIAGRAM

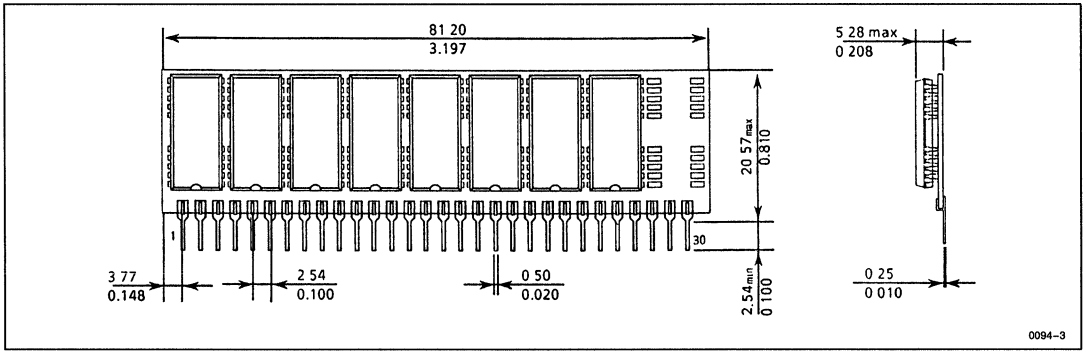


Note: M0–M7[HB56A48XX-XXA]: HM514100AS
M0–M7[HB56A48XX-8/10: HM514100JP

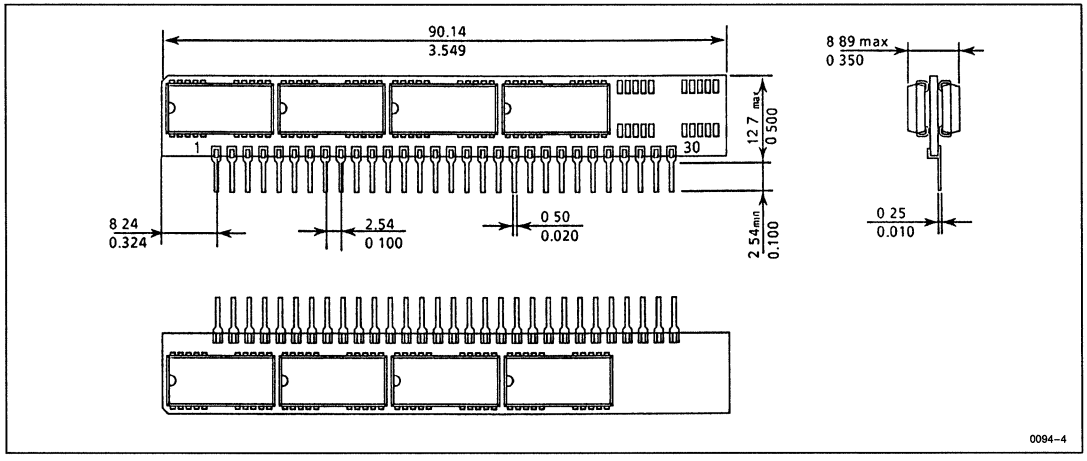
■ PHYSICAL OUTLINE

Unit: mm (inch)

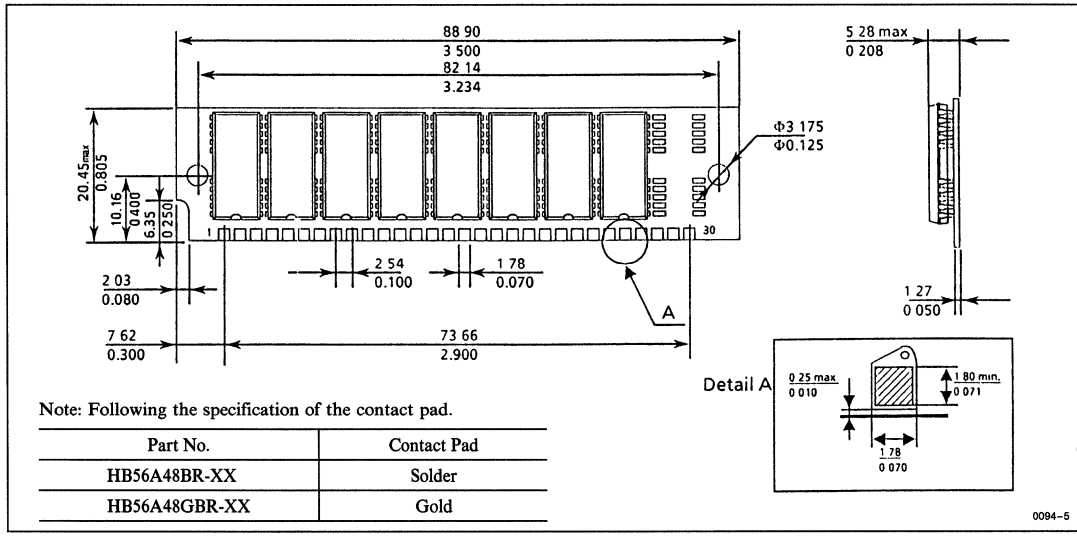
• HB56A48AR Series



• HB56A48ATR Series



• HB56A48BR/GBR Series



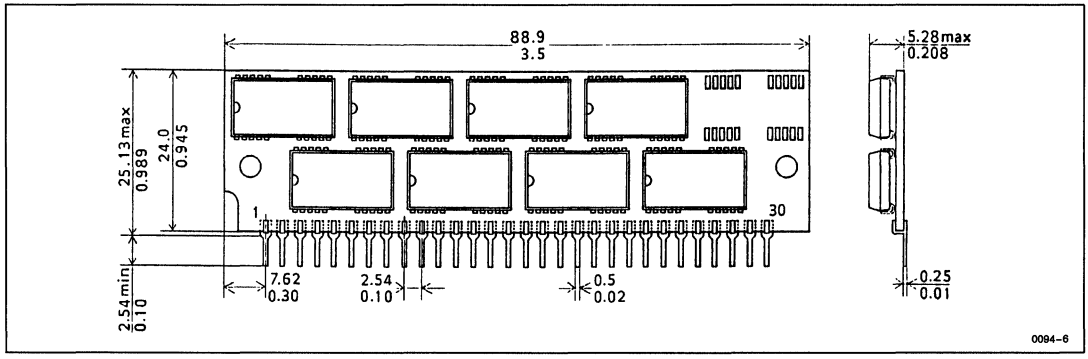
Note: Following the specification of the contact pad.

Part No.	Contact Pad
HB56A48BR-XX	Solder
HB56A48GBR-XX	Gold

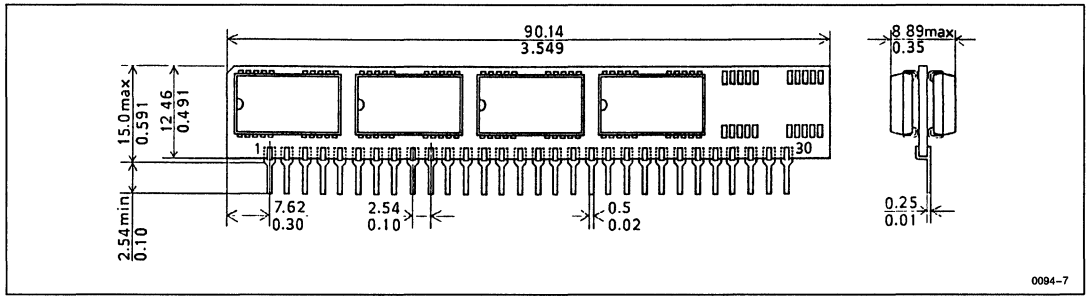
■ PHYSICAL OUTLINE (continued)

Unit: mm (inch)

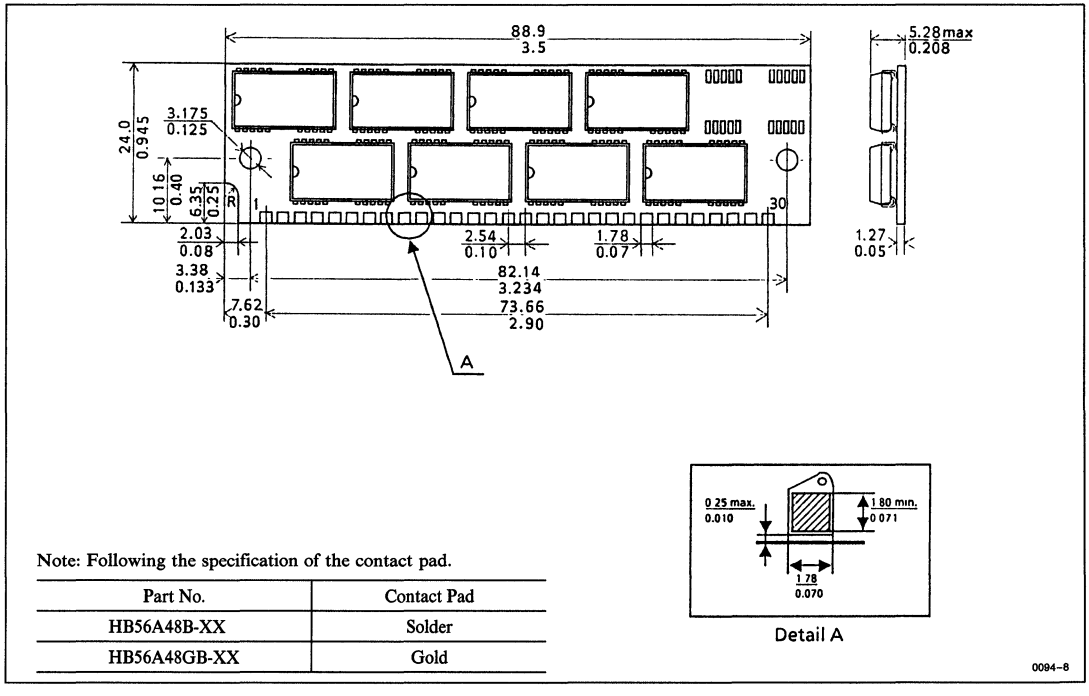
• HB56A48A Series



• HB56A48AT Series



• HB56A48B/GB Series



Note: Following the specification of the contact pad.

Part No.	Contact Pad
HB56A48B-XX	Solder
HB56A48GB-XX	Gold

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	8	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HB56A48B/GB/BR/GBR/A/AR/AT/ATR								Unit	Test Condition	Note
		-6A		-7A		-8/-8A		-10/-10A				
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	880	—	800	—	720	—	640	mA	t_{RC} = min	1, 2
Standby Current	I_{CC2}	—	16	—	16	—	16	—	16	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	8	—	8	—	8	—	8	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	880	—	800	—	720	—	640	mA	t_{RC} = min	2
Standby Current	I_{CC5}	—	40	—	40	—	40	—	40	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	880	—	800	—	720	—	640	mA	t_{RC} = min	
Page Mode Current	I_{CC7}	—	880	—	800	—	720	—	640	mA	t_{PC} = min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{IN} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	HB56A48				Unit	Note
		BR/GBR/AR/ATR		A/AT/B/GB			
		Typ	Max	Typ	Max		
Input Capacitance (Address)	C_{I1}	—	55	—	65	pF	1
Input Capacitance (Clock)	C_{I2}	—	68	—	81	pF	1
Input/Output Capacitance (DQ_{0-7})	$C_{I/O}$	—	17	—	30	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 12, 15]

Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56A48B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	180	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	70	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10000	20	10000	20	10000	25	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	15	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	20	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	20	50	20	60	25	75	20	60	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	15	35	15	40	20	55	15	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	20	—	25	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	—	16	—	16	—	16	ms	17

Read Cycle

Parameter	Symbol	HB56A48B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	80	—	100	ns	2, 3, 16
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	—	25	—	25	—	25	ns	3, 4, 14
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	40	—	45	ns	3, 5, 14, 16
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	0	—	10	—	10	—	ns	

Read Cycle (continued)

Parameter	Symbol	HB56A48B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	40	—	45	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	15	0	20	0	20	0	25	0	20	0	25	ns	6

Write Cycle

Parameter	Symbol	HB56A48B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	15	—	20	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	10	—	20	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	20	—	25	—	25	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	20	—	20	—	25	—	25	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	20	—	15	—	20	—	ns	11

Refresh Cycle

Parameter	Symbol	HB56A48B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	10	—	20	—	20	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HB56A48B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	55	—	55	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	—	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	35	—	40	—	45	—	50	—	50	—	50	ns	14, 16
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	45	—	50	—	50	—	50	—	ns	

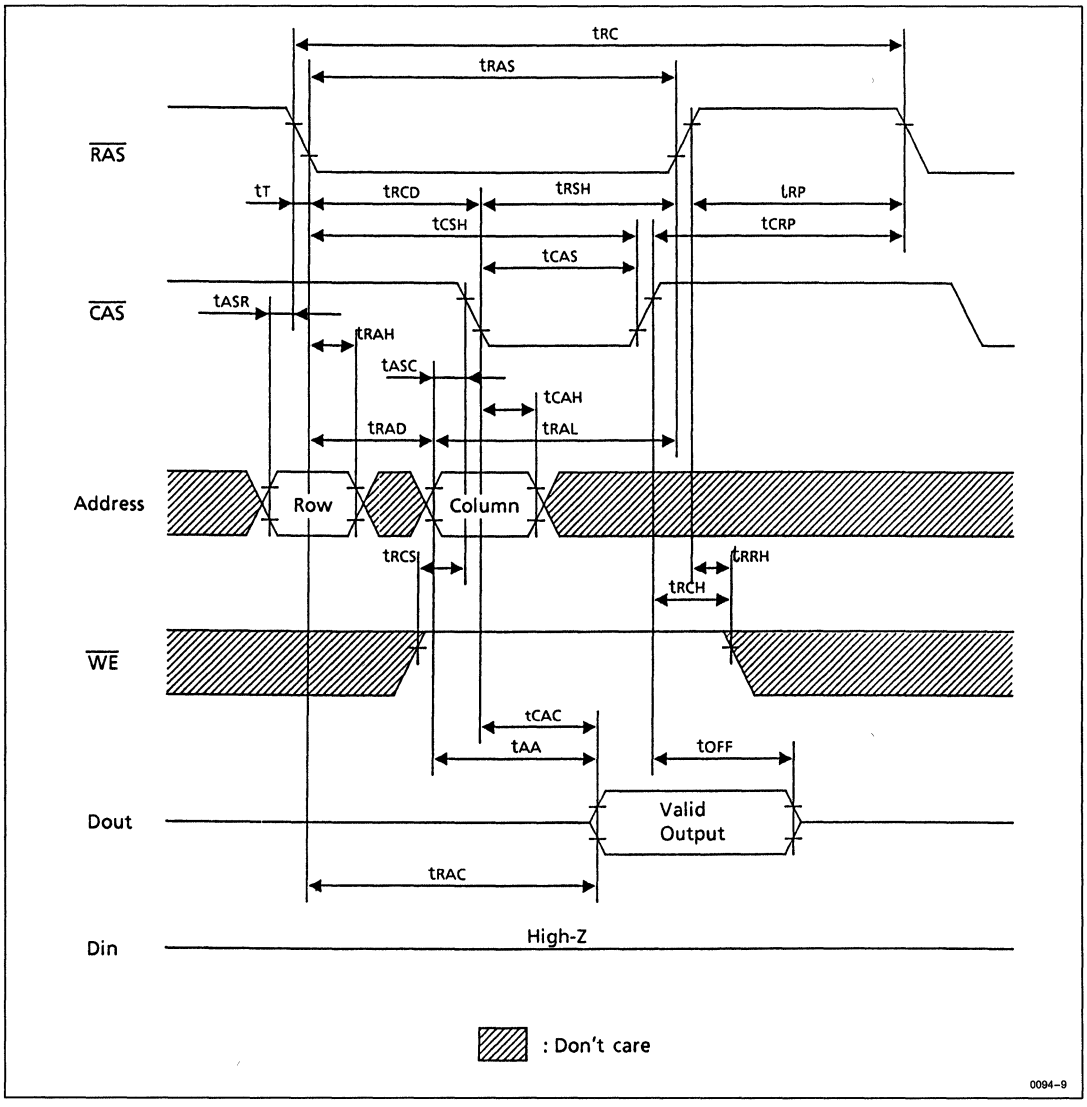
Test Mode Cycle

Parameter	Symbol	HB56A48B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	10	—	10	—	10	—	10	—	20	—	20	—	ns	

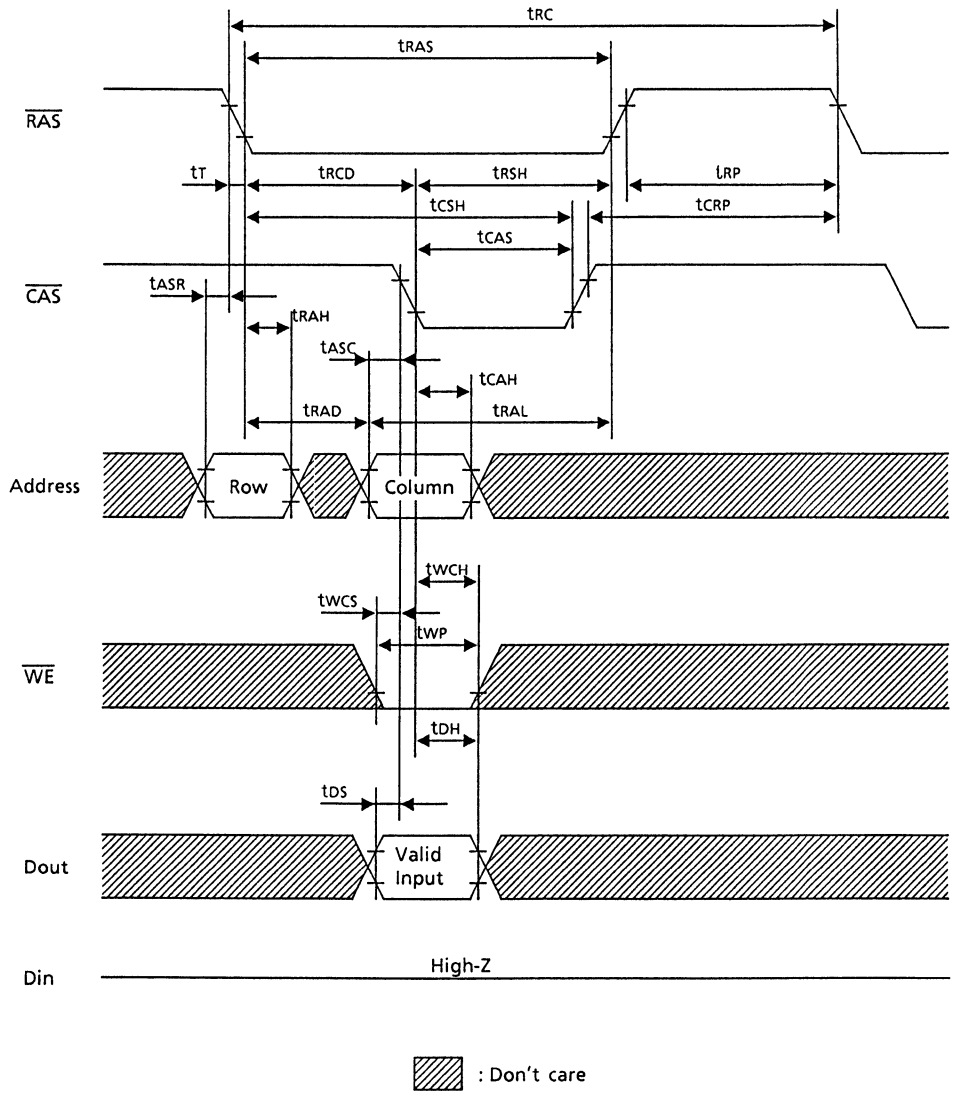
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as RAS-only refresh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits . . . RA10, CA10 and CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is D_{out} and data input pin is D_{in}. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
16. In a test mode read cycle, the value of t_{RAC}, t_{AA} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
17. t_{REF} is determined by 1,024 refresh cycles.

■ TIMING WAVEFORM

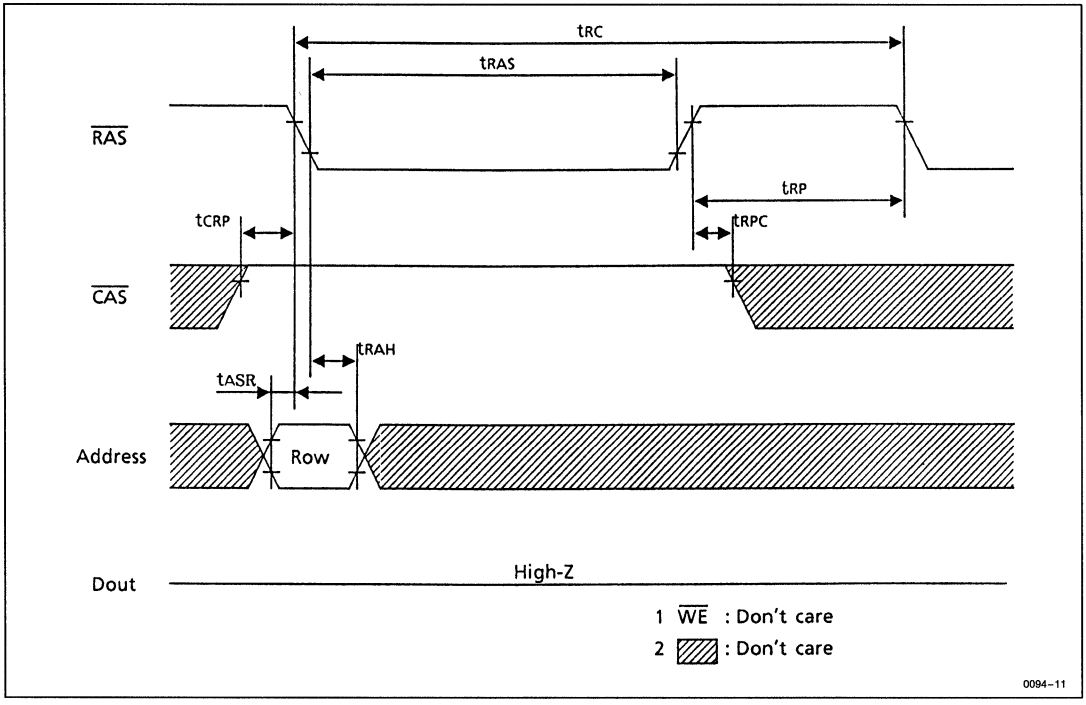
• Read Cycle



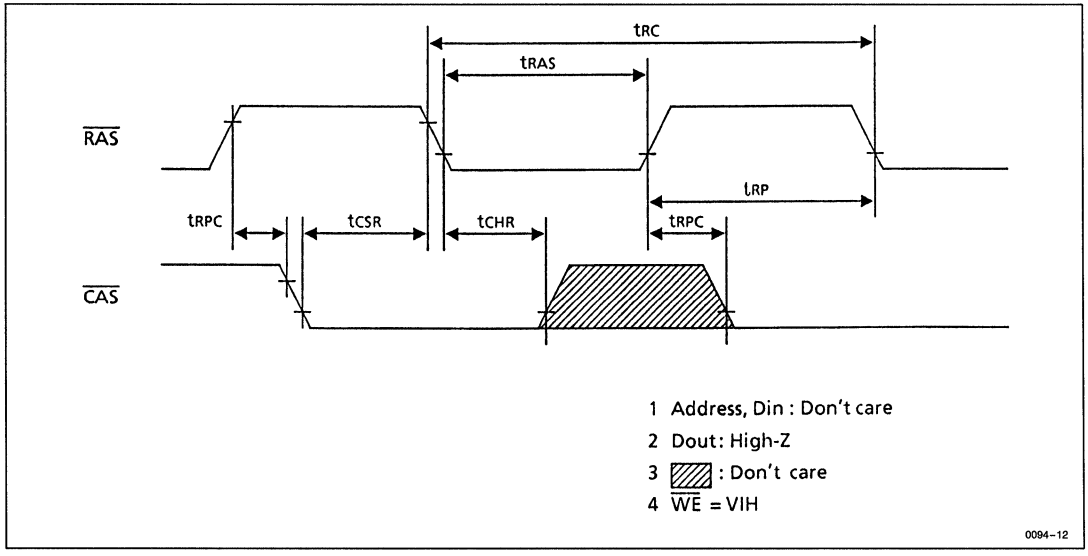
• **Early Write Cycle**



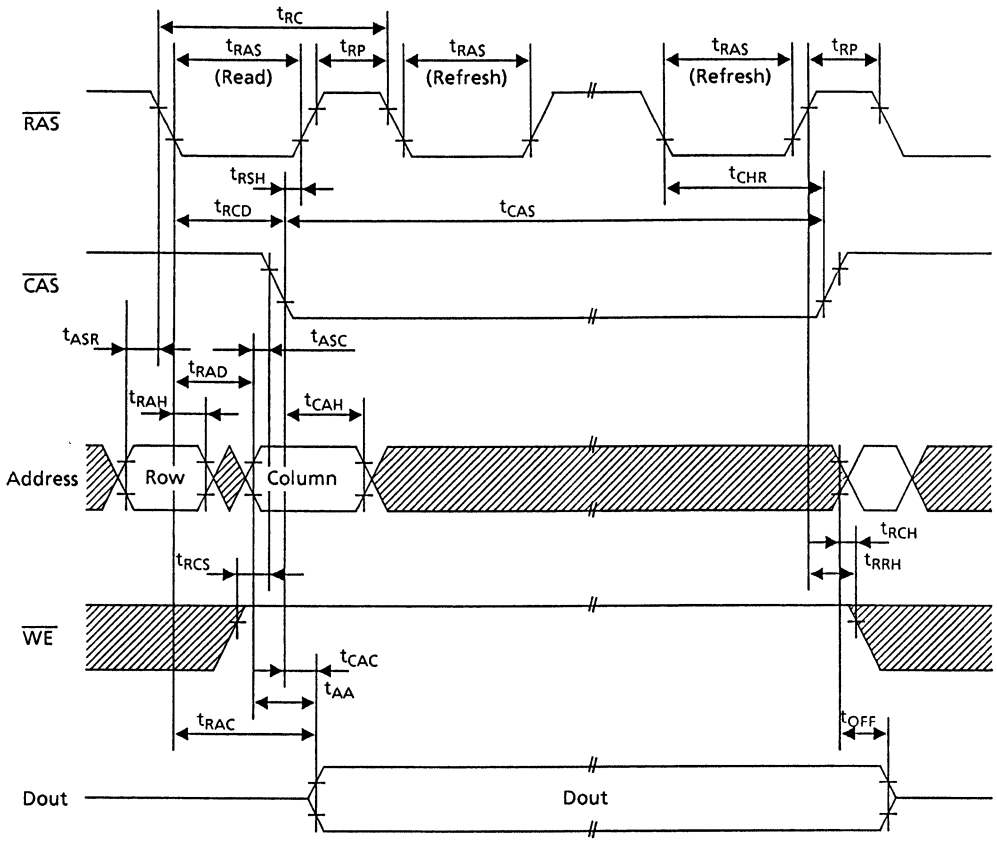
• $\overline{RAS}$ Only Refresh Cycle



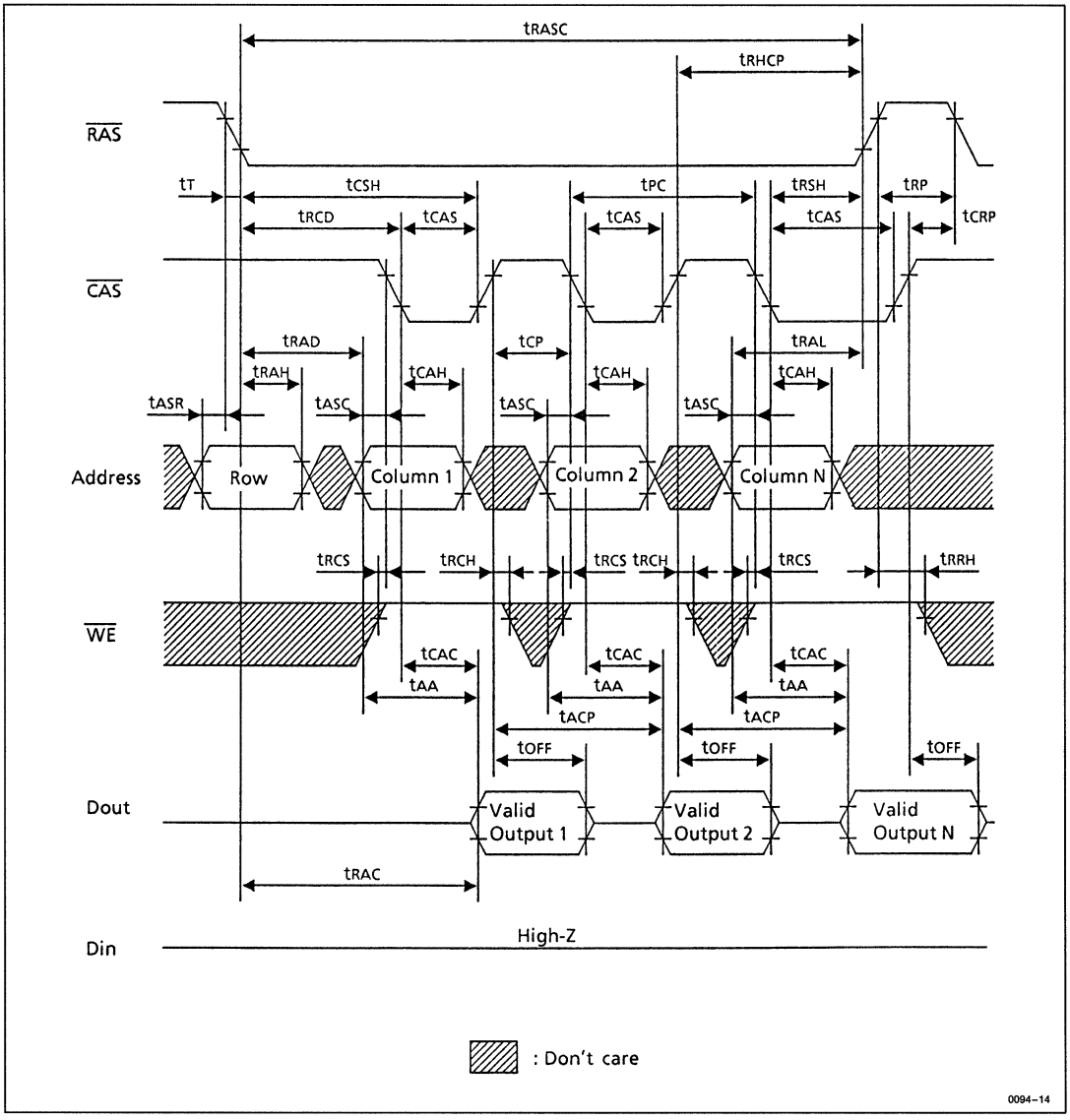
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



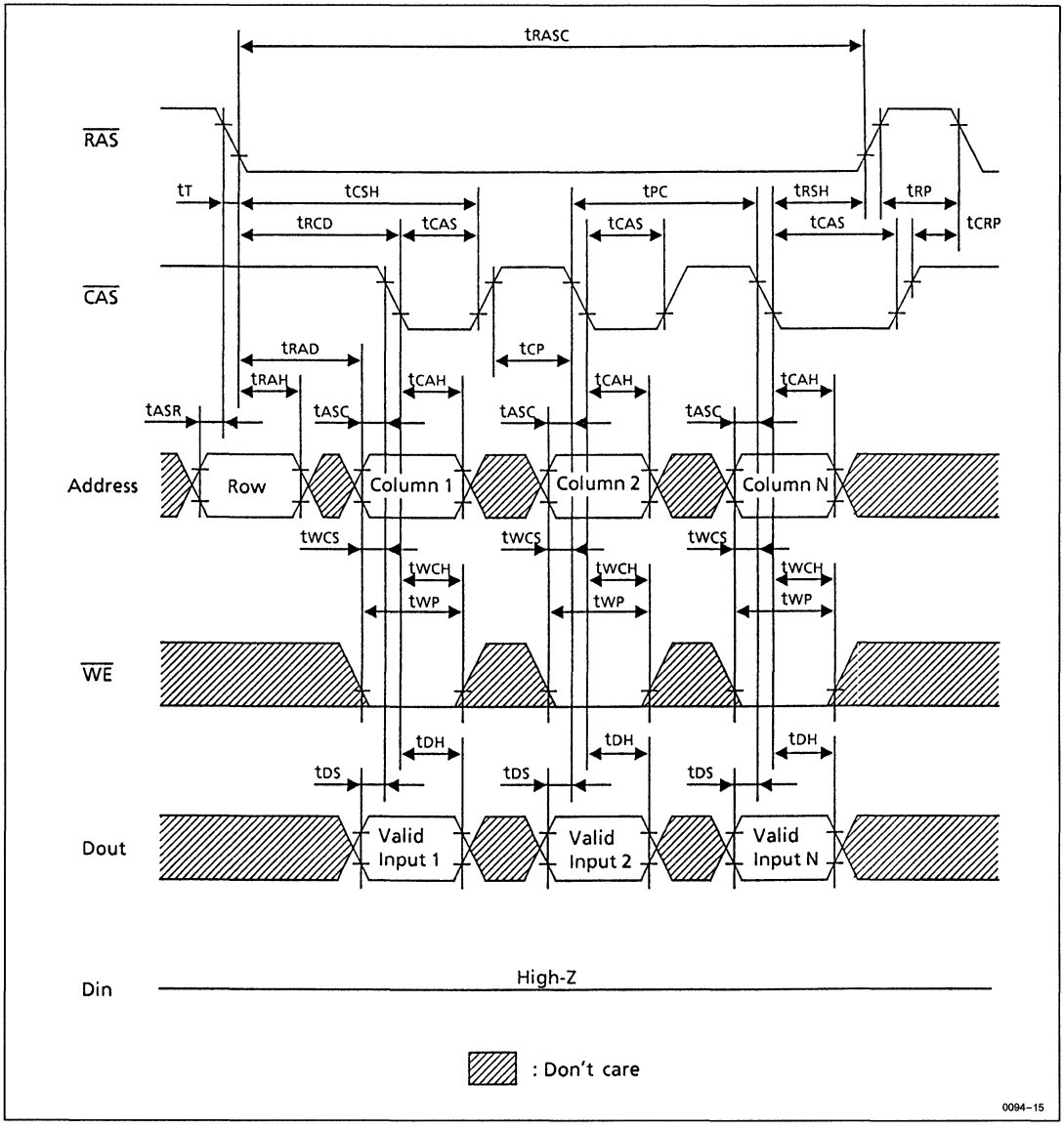
• **Hidden Refresh Cycle**



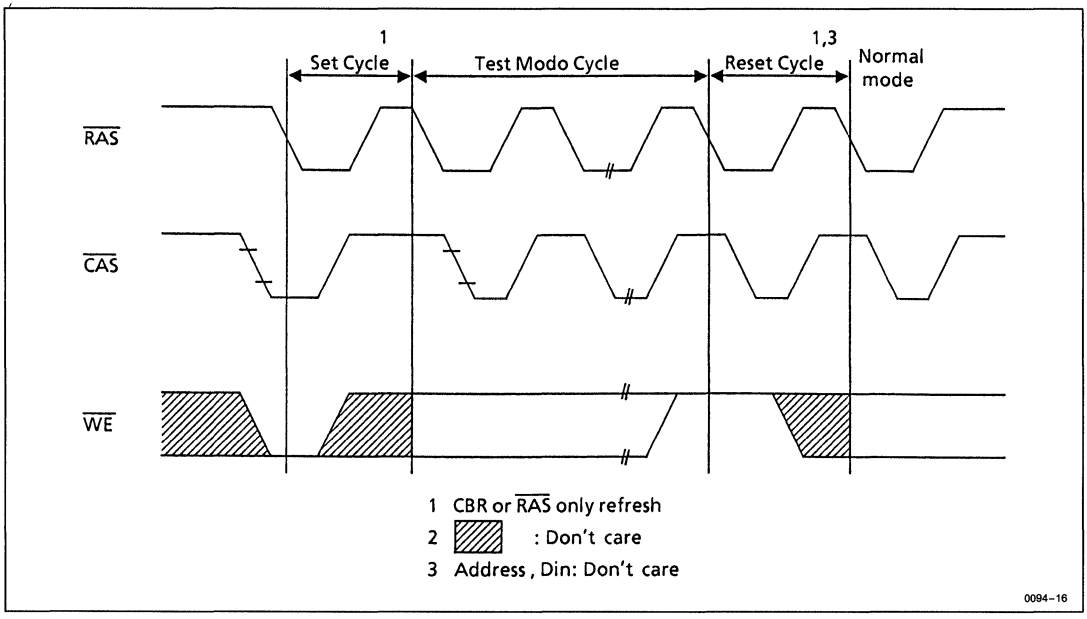
• **Fast Page Mode Read Cycle**



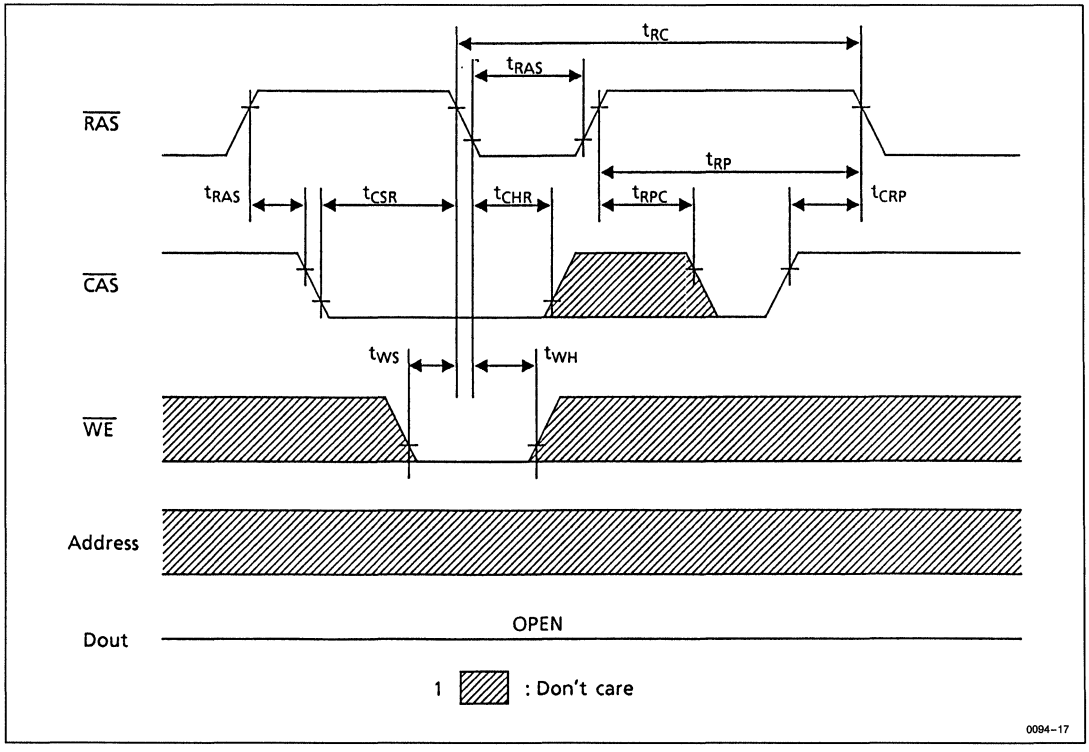
• **Fast Page Mode Early Write Cycle**



• **TEST MODE CYCLE**

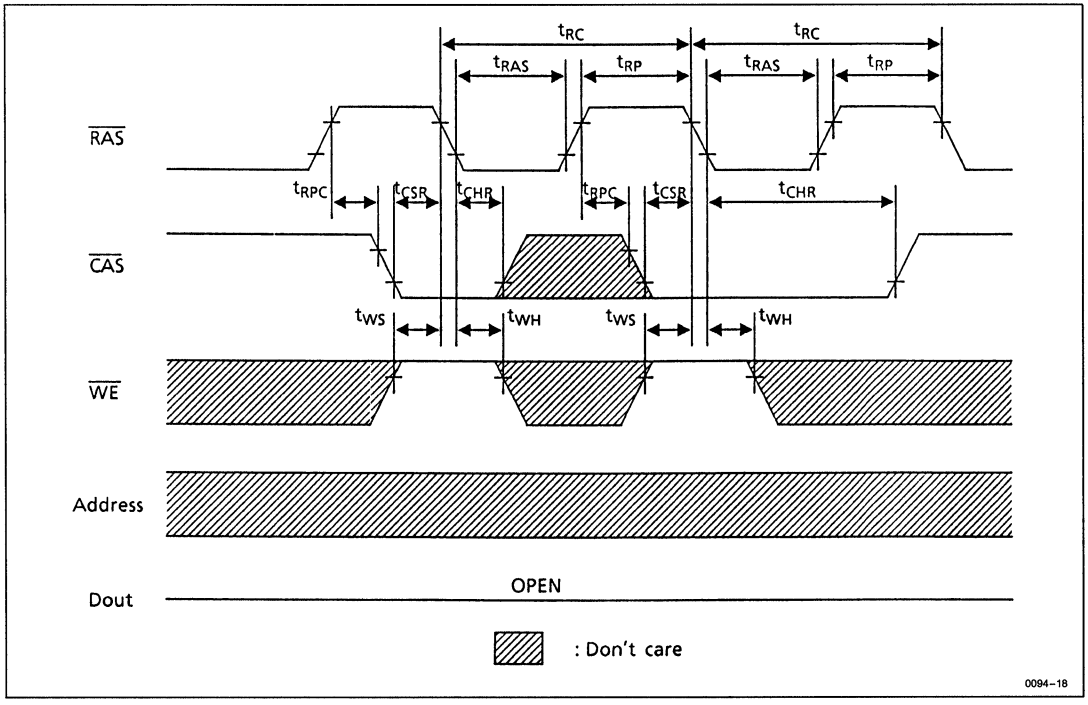


• **Test Mode Set Cycle**

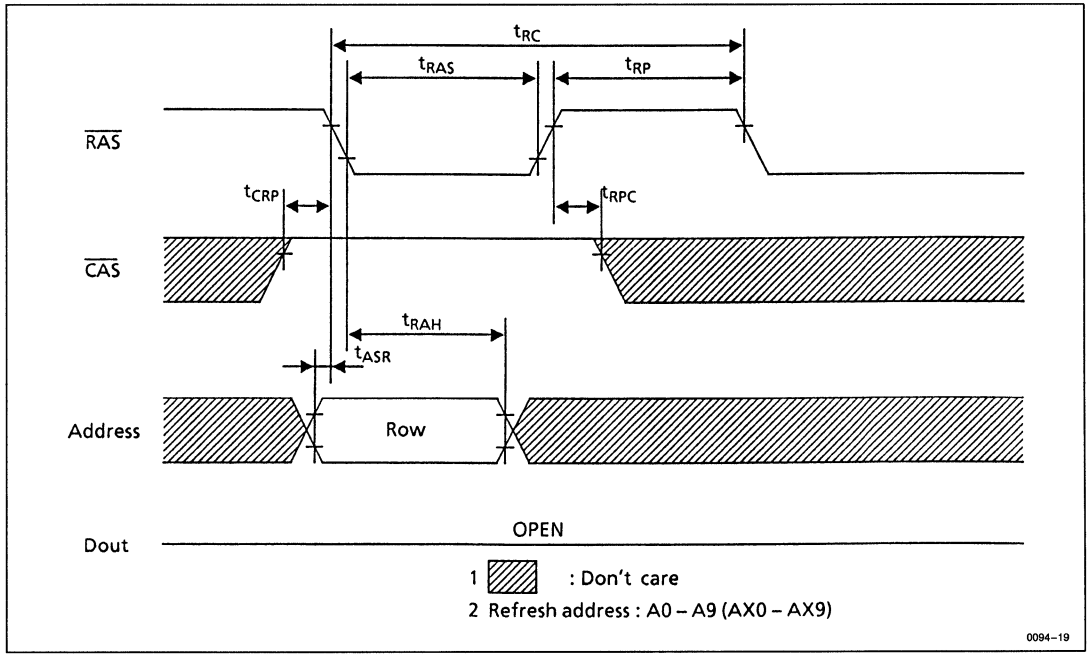


• **Test Mode Reset Cycle**

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



$\overline{RAS}$ Only Refresh Cycle



HB56A19 Series

1,048,576-Word x 9-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56A19 is a 1M x 9 dynamic RAM module, mounted nine 1-Mbit DRAM (HM511000JP) sealed in SOJ package. An outline of the HB56A19 is 30-pin single in-line package having Lead types (HB56A19A, HB56A19AT), Socket type (HB56A19B). Therefore, the HB56A19 makes high density mounting possible without surface mount technology. The HB56A19 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath each SOJ.

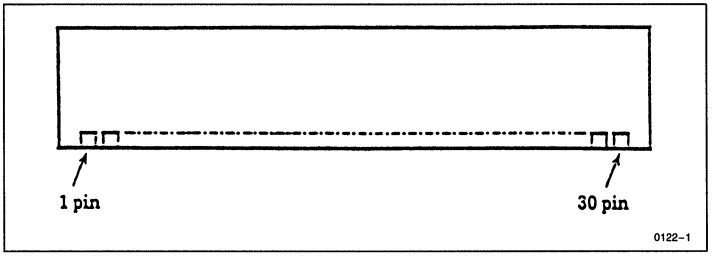
■ FEATURES

- 30-pin Single In-line Package
  - Lead Pitch 2.54mm
- Single 5V (±10%) Supply
- High Speed
  - Access Time ..... 60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode ..... 4455 mW/3960 mW/3465 mW/2970 mW/2475 mW (max)
  - Standby Mode ..... 99 mW (max)
- Fast Page Mode Capability
- 512 Refresh Cycle ..... (8 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

Access Time	Package		
	30-pin SIP Lead Type	30-pin SIP Low Profile Lead Type	30-pin SIMM Socket Type
60 ns	HB56A19A-6H	HB56A19AT-6H	HB56A19B-6H
70 ns	HB56A19A-7H	HB56A19AT-7H	HB56A19B-7H
80 ns	HB56A19A-8A	HB56A19AT-8A	HB56A19B-8A
100 ns	HB56A19A-10A	HB56A19AT-10A	HB56A19B-10A
120 ns	HB56A19A-12A	HB56A19AT-12A	HB56A19B-12A

■ PIN OUT

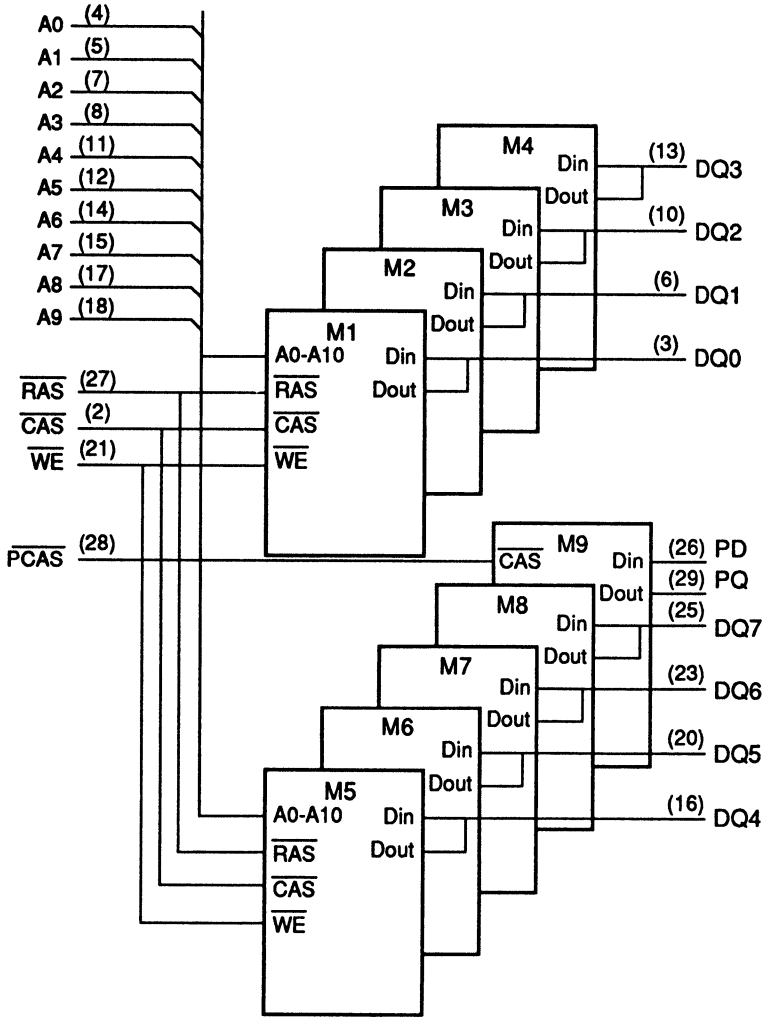


Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CAS}$	17	A_8
3	DQ_0	18	A_9
4	A_0	19	NC
5	A_1	20	DQ_5
6	DQ_1	21	$\overline{WE}$
7	A_2	22	V_{SS}
8	A_3	23	DQ_6
9	V_{SS}	24	NC
10	DQ_2	25	DQ_7
11	A_4	26	PQ
12	A_5	27	$\overline{RAS}$
13	DQ_3	28	$\overline{PCAS}$
14	A_6	29	PD
15	A_7	30	V_{CC}

■ PIN DESCRIPTION

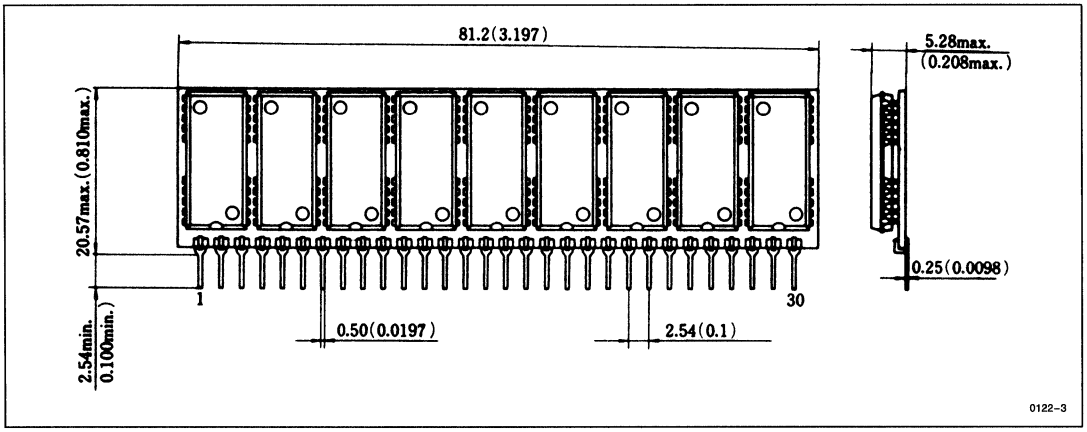
Pin Name	Function
A_0–A_9	Address Input
A_0–A_8	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$, $\overline{PCAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
DQ_0–DQ_7	Data-in/Data-out
PD	Parity Data-in
PQ	Parity Data-out
V_{CC}	Power Supply (+ 5V)
V_{SS}	Ground
NC	Non-Connection

■ BLOCK DIAGRAM

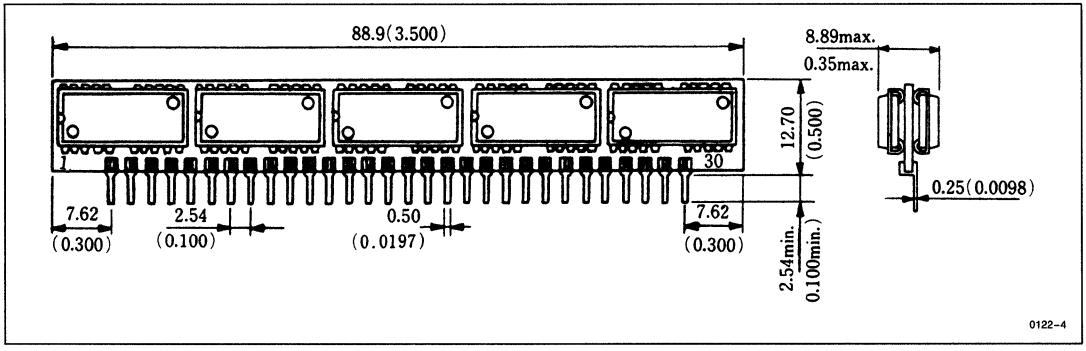


■ PHYSICAL OUTLINE

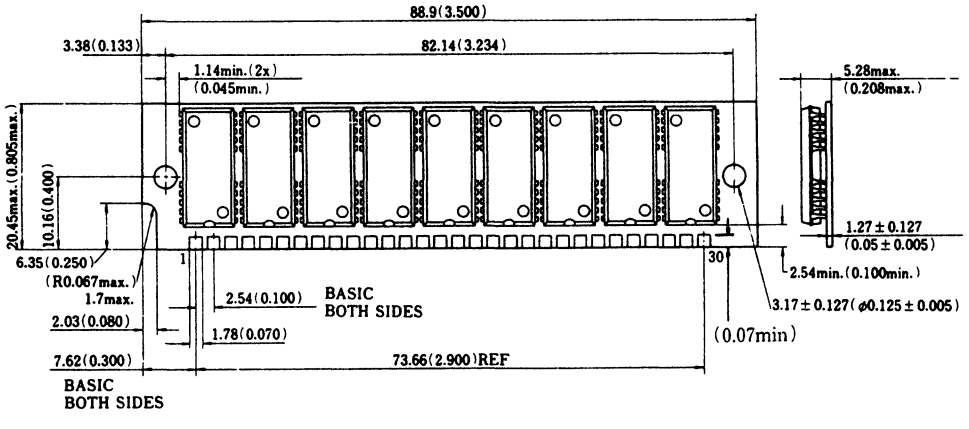
• HB56A19A Series



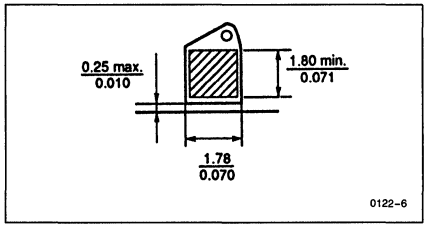
• HB56A19AT Series



• **HB56A19B Series**



Detail A



Note: The plating of the contact finger is solder coat.

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	Input	V_{in}	−1.0 to +7.0	V
	Output	V_{out}	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	9	W
Operating Temperature		T_{opr}	0 to +70	°C
Storage Temperature		T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HB56A19A/AT/B										Unit	Test Conditions	Note
		-6H		-7H		-8A		-10A		-12A				
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	810	—	720	—	630	—	540	—	450	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	18	—	18	—	18	—	18	—	18	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	9	—	9	—	9	—	9	—	9	mA	CMOS Interface, $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	810	—	720	—	540	—	450	—	405	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	45	—	45	—	45	—	45	—	45	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	810	—	720	—	540	—	360	—	320	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	810	—	720	—	450	—	450	—	360	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	−10	10	−	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	60	pF	1
Input Capacitance (Clock)	C_{I2}	—	75	pF	1
Input/Output Capacitance (DQ_0–DQ_7)	$C_{I/O}$	—	17	pF	1, 2
Input Capacitance (PD)	C_{I3}	—	10	pF	1, 2
Output Capacitance (PQ)	C_O	—	12	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics**

Please show at HM511000H series or HM511000A series about AC Characteristics. But don't use by Delayed Write Cycle, because the HB56A19 provides common data inputs and outputs. Please use by Early Write Cycle. ($t_{WCS} \geq t_{WCS}$ (min)).

HB56A19L Series

1,048,576-Word x 9-Bit High Density Dynamic RAM Module

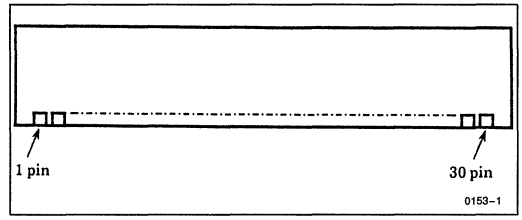
■ DESCRIPTION

The HB56A19 is a 1M x 9 dynamic RAM module, mounted nine 1 Mbit DRAM (HM511000ALJP) sealed in SOJ package. An outline of the HB56A19 is 30-pin single in-line package having lead types (HB56A19A, HB56A19AT), socket type (HB56A19B, HB56A19GB). Therefore, the HB56A19 makes high density mounting possible without surface mount technology. The HB56A19 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath each SOJ.

■ FEATURES

- 30-pin Single In-line Package
  Lead Pitch .....2.54 mm
- Single 5V (±10%) Supply
- High Speed
  Access Time .....60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  Active Mode .....4455 mW/3960 mW/3465 mW/2970 mW/2475 mW (max)
  Standby Mode .....15.3 mW (max)
- Fast Page Mode Capability
- 512 Refresh Cycle/64 ms (Distribution Refresh)
- 2 Variations of Refresh
  $\overline{RAS}$ Only Refresh
  $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ PIN OUT



Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CAS}$	17	A_8
3	DQ_0	18	A_9
4	A_0	19	NC
5	A_1	20	DQ_5
6	DQ_1	21	$\overline{WE}$
7	A_2	22	V_{SS}
8	A_3	23	DQ_6
9	V_{SS}	24	NC
10	DQ_2	25	DQ_7
11	A_4	26	PQ
12	A_5	27	$\overline{RAS}$
13	DQ_3	28	$P\overline{CAS}$
14	A_6	29	PD
15	A_7	30	V_{CC}

■ ORDERING INFORMATION

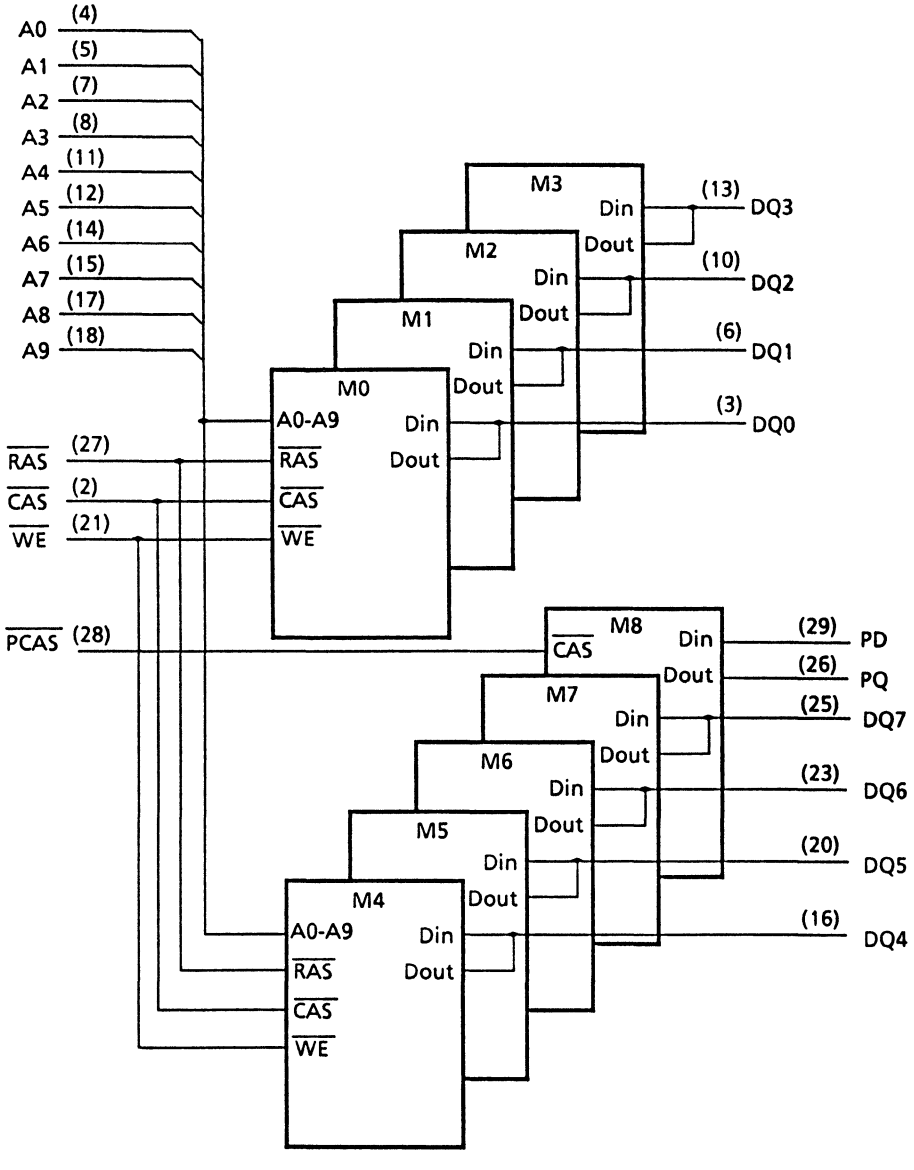
Access Time	Package			
	30-pin SIP Lead Type	30-pin SIP Low Profile Lead Type	30-pin SIP[1] Socket Type	30-pin SIP[1] Socket Type
60 ns	HB56A19A-6L	HB56A19AT-6L	HB56A19B-6L	HB56A19GB-6L
70 ns	HB56A19A-7L	HB56A19AT-7L	HB56A19B-7L	HB56A19GB-7L
80 ns	HB56A19A-8L	HB56A19AT-8L	HB56A19B-8L	HB56A19GB-8L
100 ns	HB56A19A-10L	HB56A19AT-10L	HB56A19B-10L	HB56A19GB-10L
120 ns	HB56A19A-12L	HB56A19AT-12L	HB56A19B-12L	HB56A19GB-12L

Note: 1. Following the specification of the contact pad.
HB56A19B-XXL : solder
HB56A19GB-XXL : gold

■ PIN DESCRIPTION

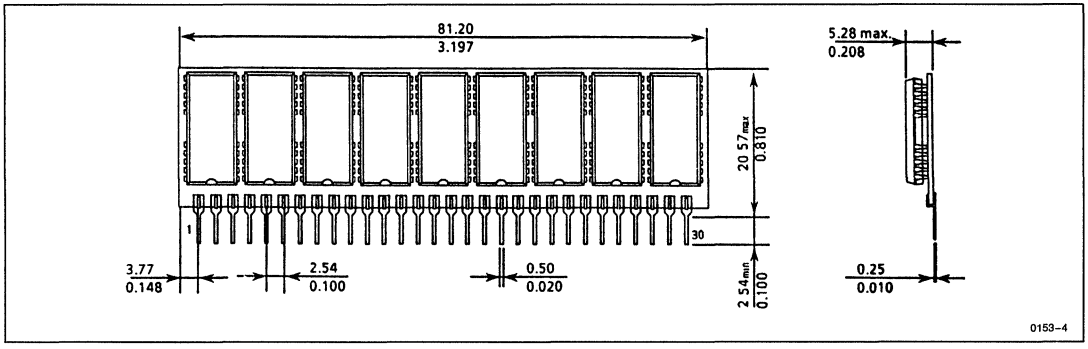
Pin Name	Function
A_0–A_9	Address Input
A_0–A_8	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$, $P\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
DQ_0–DQ_{17}	Data-in/Data-out
PD	Parity Data-in
PQ	Parity Data-out
V_{CC}	Power Supply (+ 5V)
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM

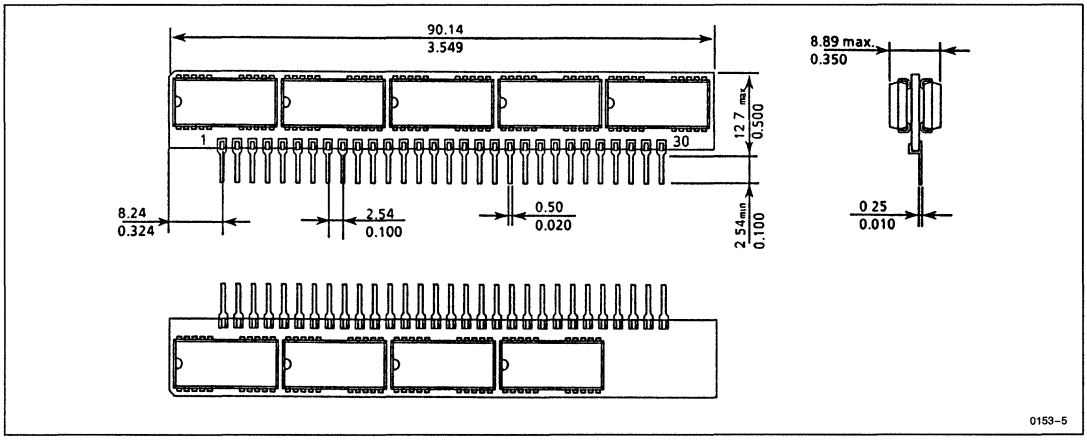


■ PHYSICAL OUTLINE

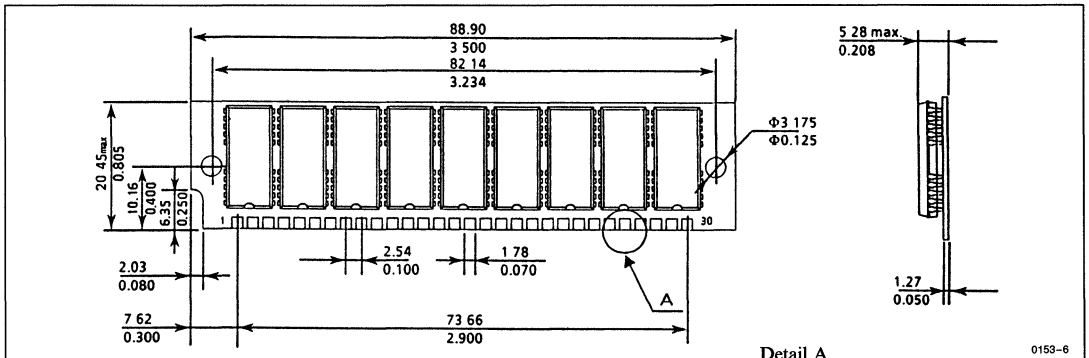
• HB56A19A Series



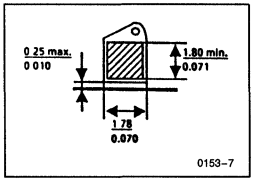
• HB56A19AT Series



• HB56A19B/GB Series



Detail A



Note: Following the specification of the contact pad

Part No.	Contact Pad
HB56A19B-6L/7L/8L/10L/12L	Solder
HB56A19GB-6L/7L/8L/10L/12L	Gold

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input)	V_{in}	− 1.0 to + 7.0	V
	(Output)	V_{out}	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	9	W
Operating Temperature		T_{opr}	0 to + 70	°C
Storage Temperature		T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HB56A19/AT/B/GB										Unit	Test Conditions	Note
		-6L		-7L		-8L		-10L		-12L				
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	810	—	720	—	630	—	540	—	450	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	18	—	18	—	18	—	18	—	18	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	2.7	—	2.7	—	2.7	—	2.7	—	2.7	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	810	—	720	—	540	—	450	—	405	mA	t_{RC} = Min	2
Battery Back Up Current	I_{CC4}	—	2.7	—	2.7	—	2.7	—	2.7	—	2.7	mA	t_{RC} = 125 μs $\overline{CAS}$ Before $\overline{RAS}$ Refresh	4
Standby Current	I_{CC5}	—	45	—	45	—	45	—	45	—	45	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	720	—	630	—	540	—	450	—	360	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	720	—	630	—	450	—	450	—	360	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed ≤ 1 time while $\overline{CAS}$ = V_{IH}.
4. t_{RAS} = t_{RAS} (min) to 1 μs.
Input voltage: All pins: V_{IH} ≥ V_{CC} − 0.2V or V_{IL} ≤ 0.2V.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	60	pF	1
Input Capacitance (Clock)	C_{I2}	—	75	pF	1
Input/Output Capacitance (DQ_{0-7})	$C_{I/O}$	—	17	pF	1, 2
Input Capacitance (PD)	C_{I3}	—	10	pF	1
Output Capacitance (PQ)	C_O	—	12	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 12]

Read, Write, and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56A19/AT/B/GB										Unit	Note
		-6L		-7L		-8L		-10L		-12L			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	120	—	130	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	50	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	70	10000	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	64	—	64	—	64	—	64	—	64	ms	15

Read Cycle

Parameter	Symbol	HB56A19A/AT/B/GB										Unit	Note
		-6L		-7L		-8L		-10L		-12L			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	55	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	—	20	—	20	—	20	—	25	—	30	ns	6

Write Cycle

Parameter	Symbol	HB56A19A/AT/B/GB										Unit	Note
		-6L		-7L		-8L		-10L		-12L			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	20	—	25	—	ns	11

Refresh Cycle

Parameter	Symbol	HB56A19A/AT/B/GB										Unit	Note
		-6L		-7L		-8L		-10L		-12L			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	ns	

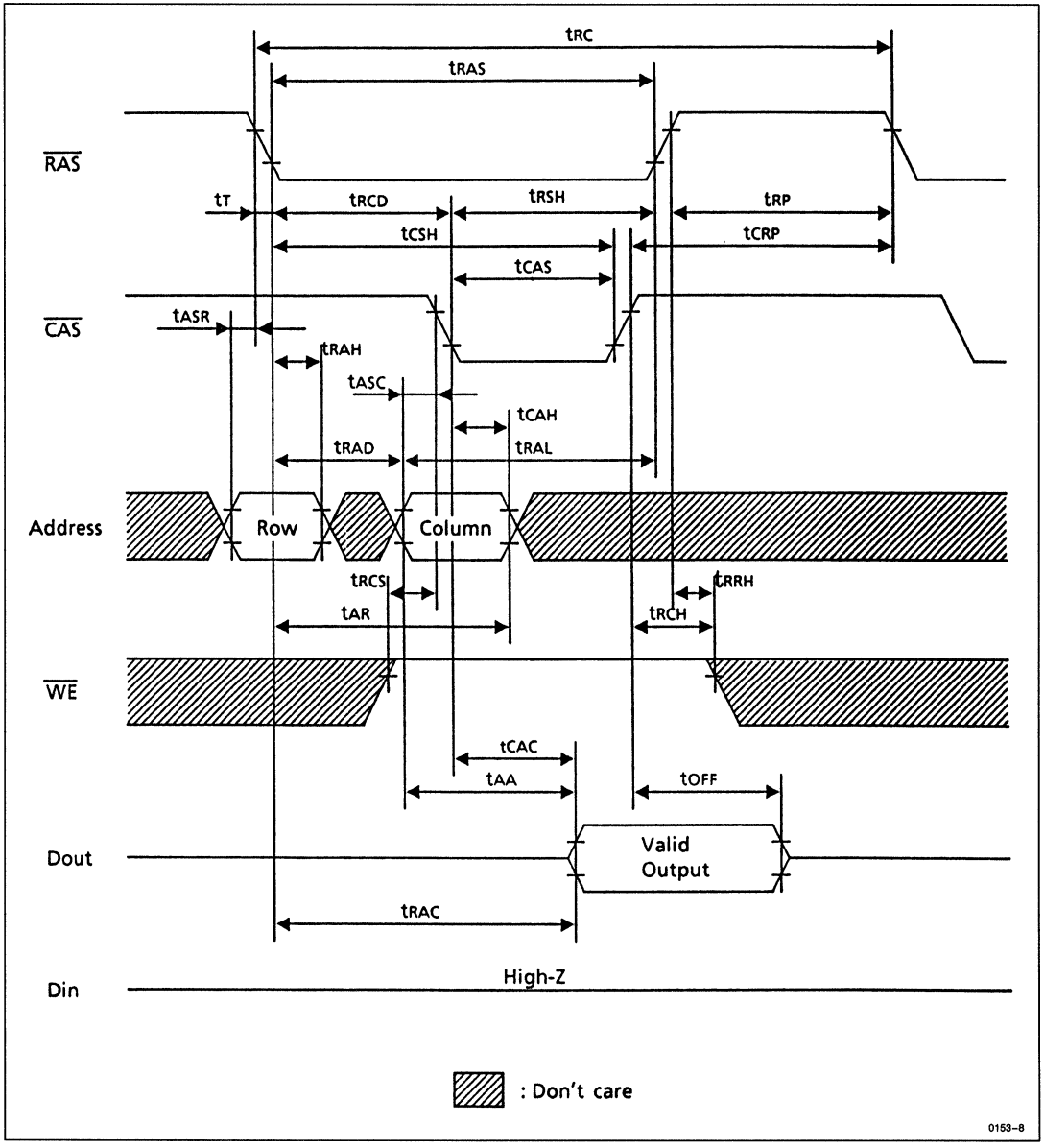
Fast Page Mode Cycle

Parameter	Symbol	HB56A19A/AT/B/GB										Unit	Note
		-6L		-7L		-8L		-10L		-12L			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	—	50	—	60	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	50	—	60	—	ns	

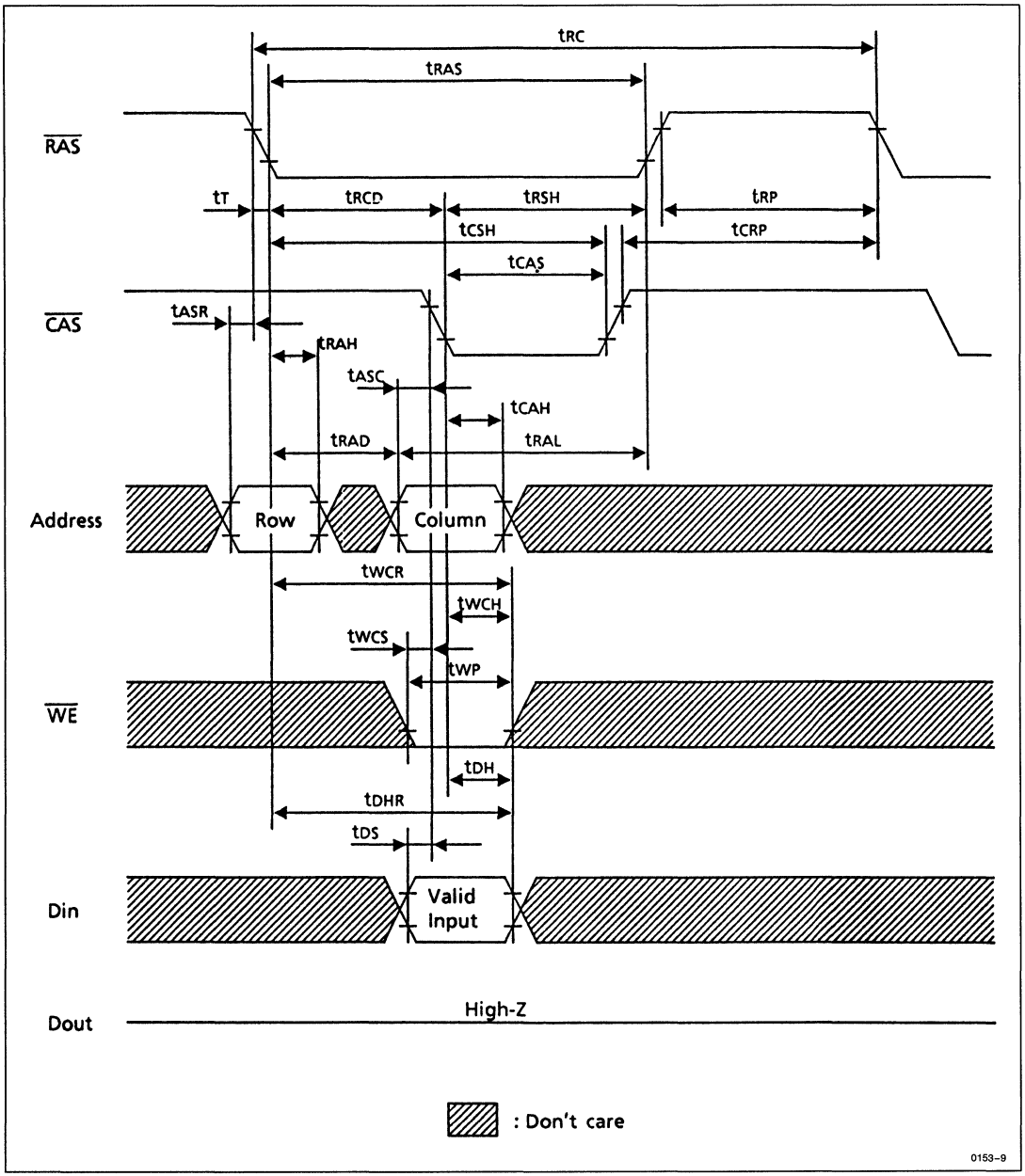
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $\geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is determined by 512 refresh cycles.

■ TIMING WAVEFORMS

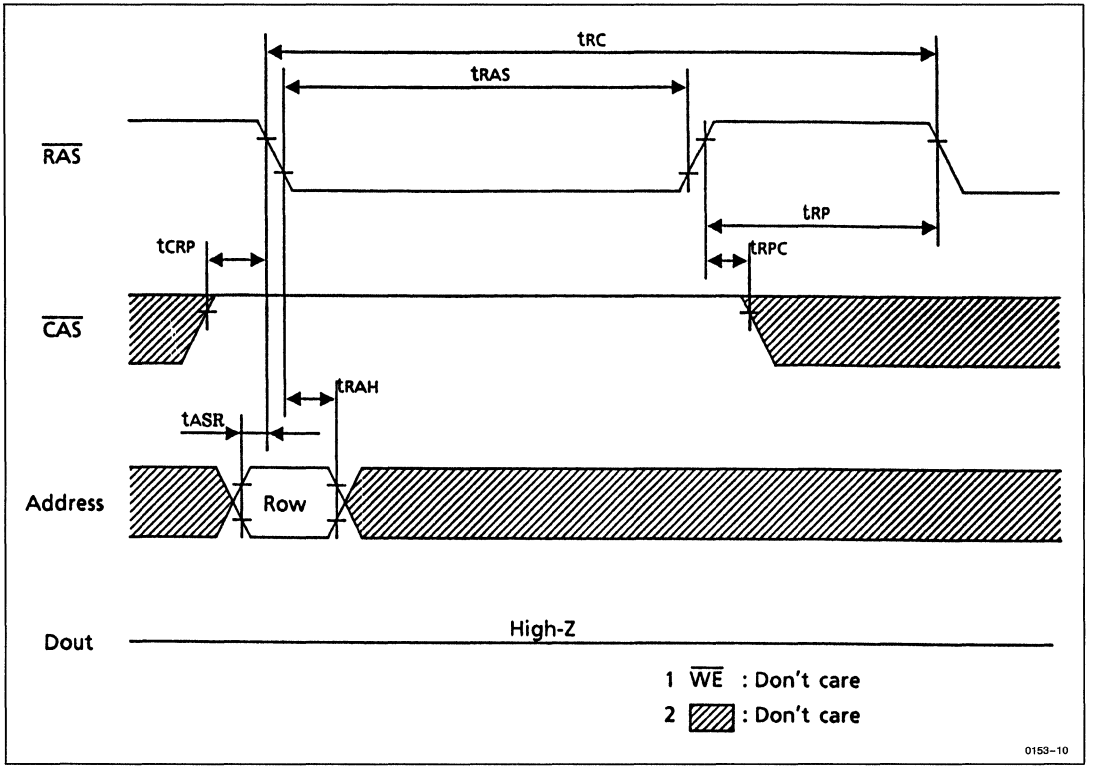
• Read Cycle



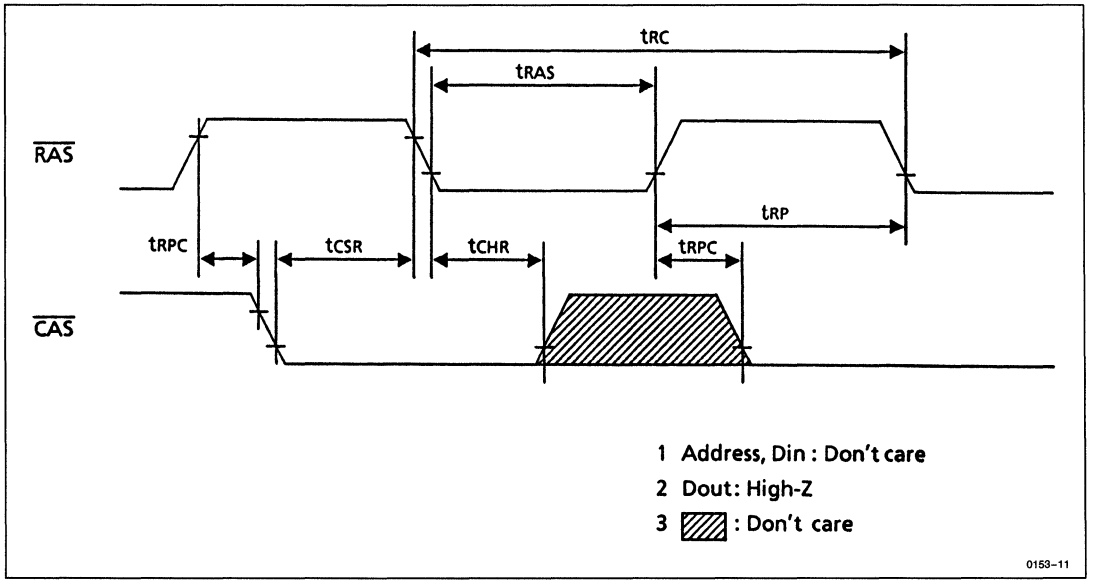
• **Early Write Cycle**



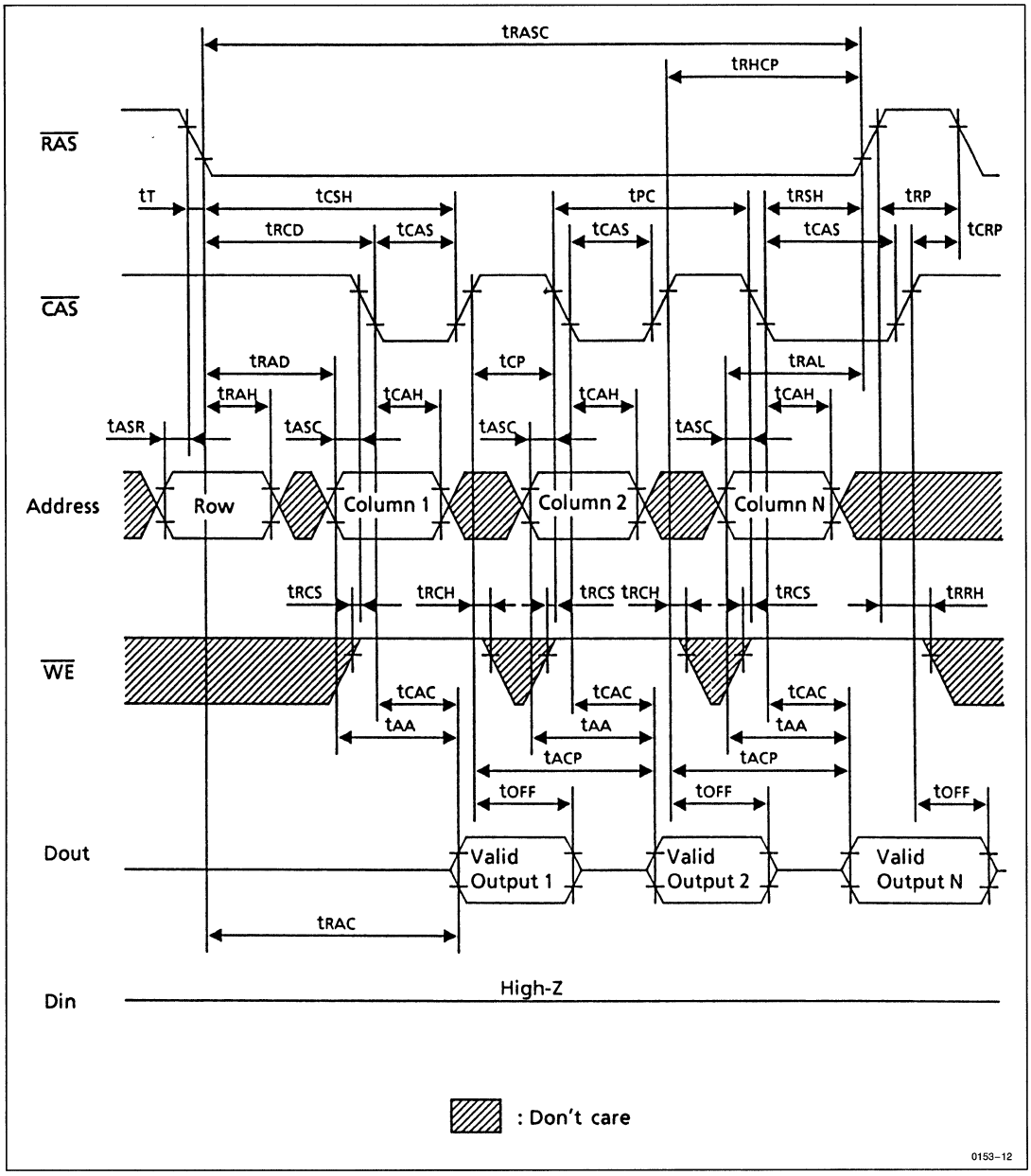
• $\overline{RAS}$ Only Refresh Cycle



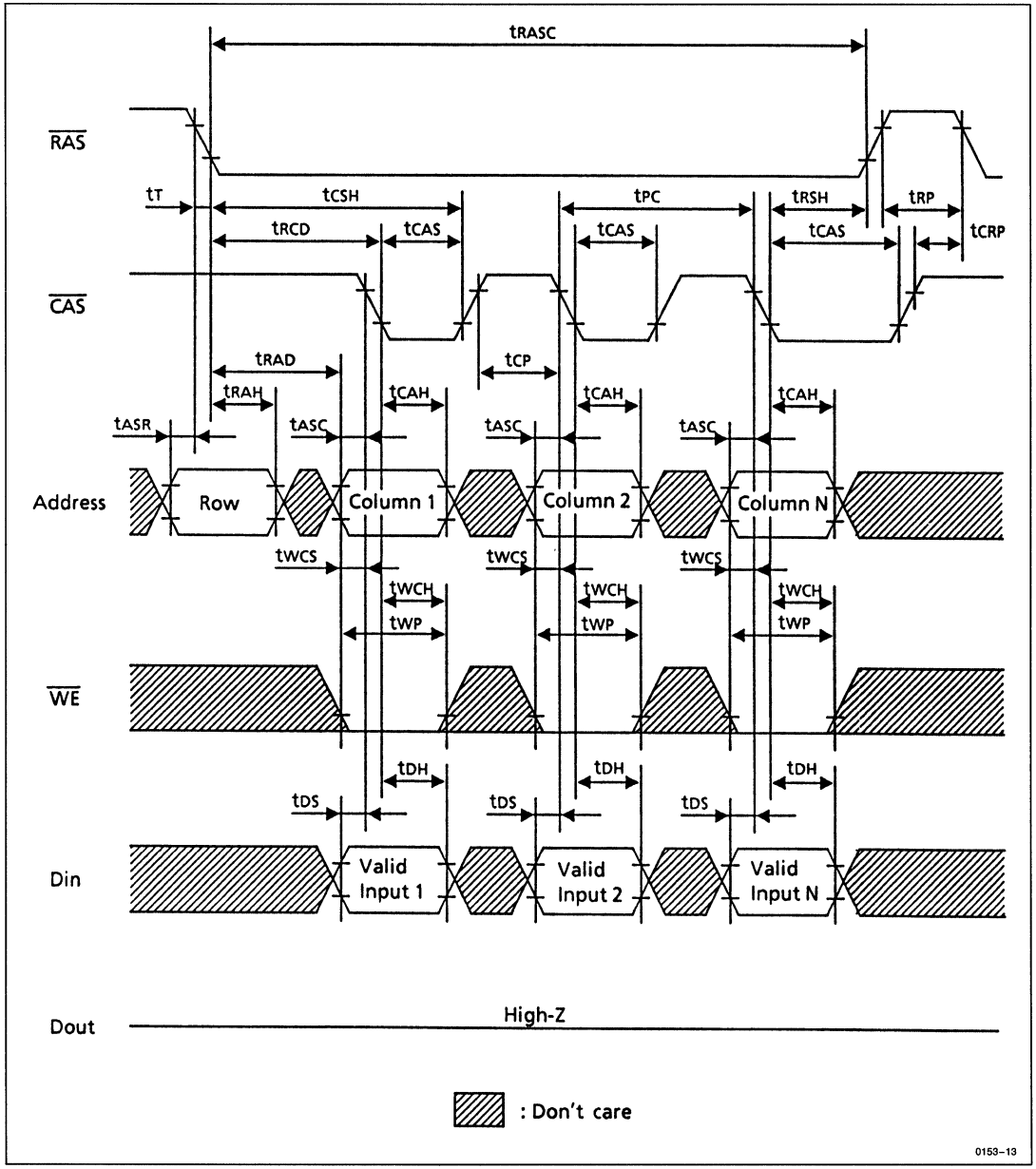
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



HB56C19 Series

1,048,576-Word x 9-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56C19 is a 1M x 9 static column mode dynamic RAM module, mounted nine 1-Mbit DRAM (HM511002JP) sealed in SOJ package. An outline of the HB56C19 is 30-pin single in-line package having Lead types (HB56C19A, HB56C19AT), socket type (HB56C19B). Therefore, the HB56C19 makes high density mounting possible without surface mount technology. The HB56C19 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath each SOJ.

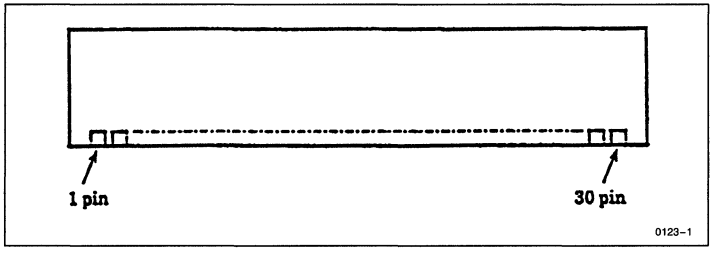
■ FEATURES

- 30-pin Single In-line Package
  - Lead Pitch 2.54mm
- Single 5V (± 10%) Supply
- High Speed
  - Access Time ..... 80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode ..... 3465 mW/2970 mW/2475 mW (max)
  - Standby Mode ..... 99 mW (max)
- Static Column Mode Capability
- 512 Refresh Cycle ..... (8 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

Access Time	Package		
	30-pin SIP Lead Type	30-pin SIP Low Profile Lead Type	30-pin SIMM Socket Type
80 ns	HB56C19A-8A	HB56C19AT-8A	HB56C19B-8A
100 ns	HB56C19A-10A	HB56C19AT-10A	HB56C19B-10A
120 ns	HB56C19A-12A	HB56C19AT-12A	HB56C19B-12A

■ PIN OUT



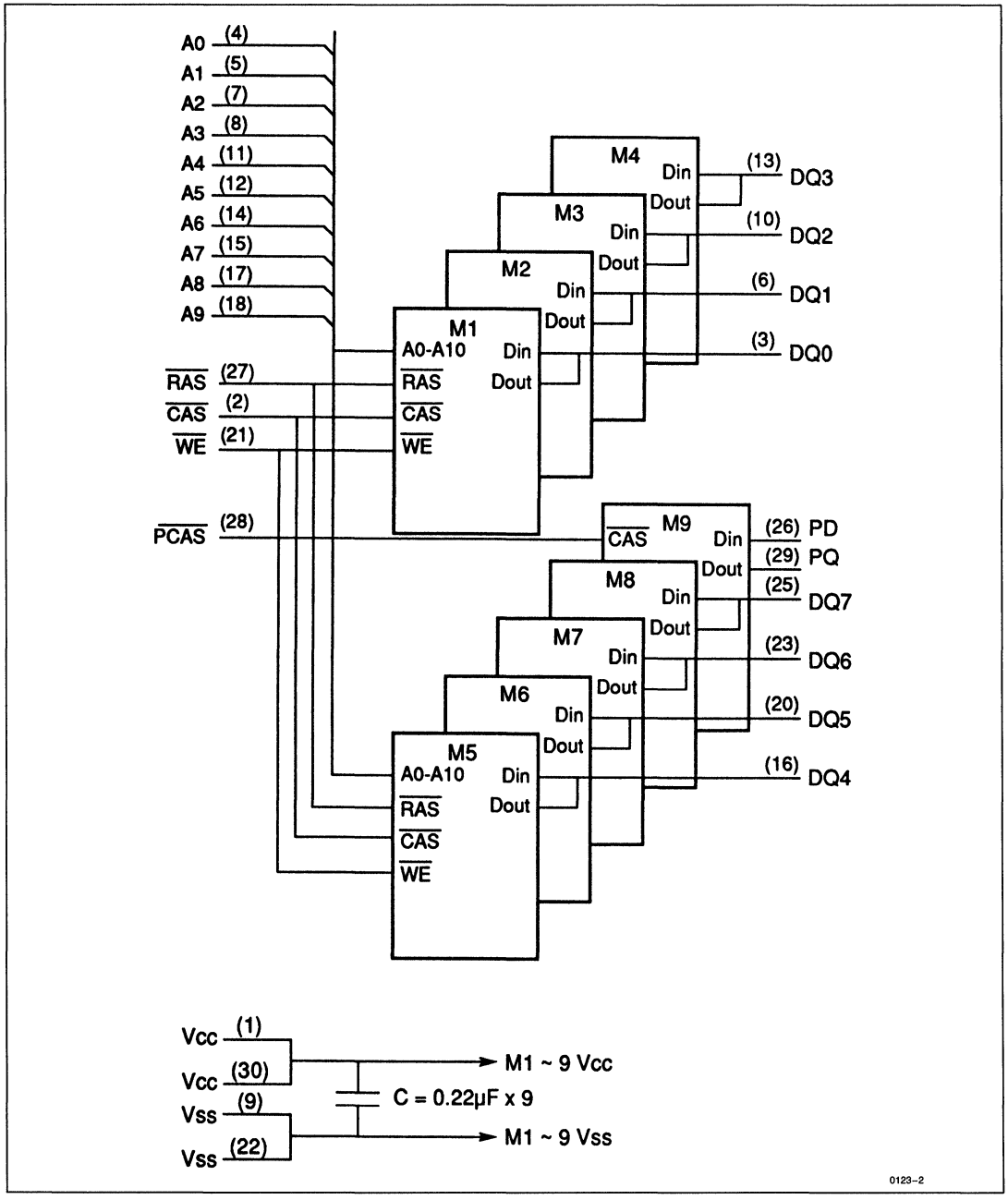
■ PIN DESCRIPTION

Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CS}$	17	A_8
3	DQ_0	18	A_9
4	A_0	19	NC
5	A_1	20	DQ_5
6	DQ_1	21	$\overline{WE}$
7	A_2	22	V_{SS}
8	A_3	23	DQ_6
9	V_{SS}	24	NC
10	DQ_2	25	DQ_7
11	A_4	26	PQ
12	A_5	27	$\overline{RAS}$
13	DQ_3	28	$\overline{PCS}$
14	A_6	29	PD
15	A_7	30	V_{CC}

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_8	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
$\overline{PCS}$	Parity Chip Select
$\overline{WE}$	Read/Write Enable
DQ_0–DQ_7	Data-in/Data-out
PD	Parity Data-in
PQ	Parity Data-out
V_{CC}	Power Supply (+ 5V)
V_{SS}	Ground
NC	Non-Connection

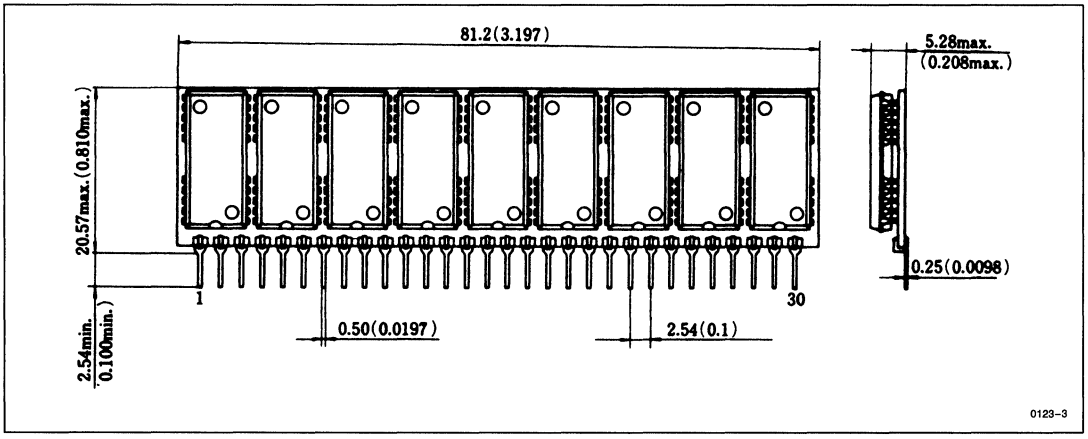
■ BLOCK DIAGRAM



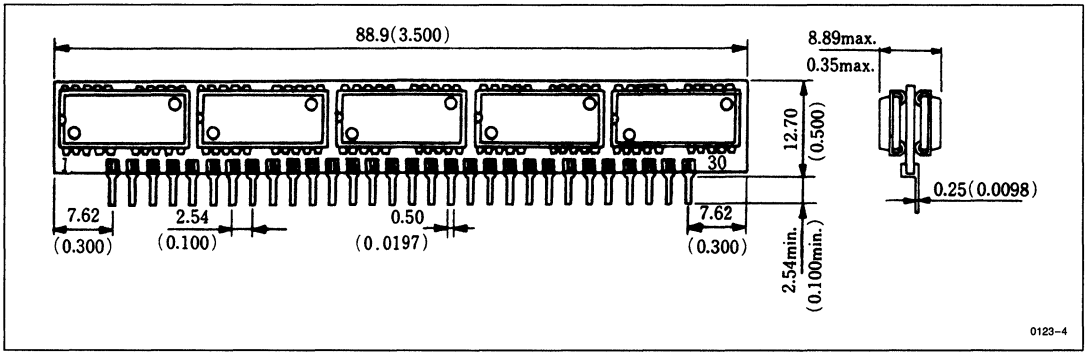
■ PHYSICAL OUTLINE

Unit: mm (inch)

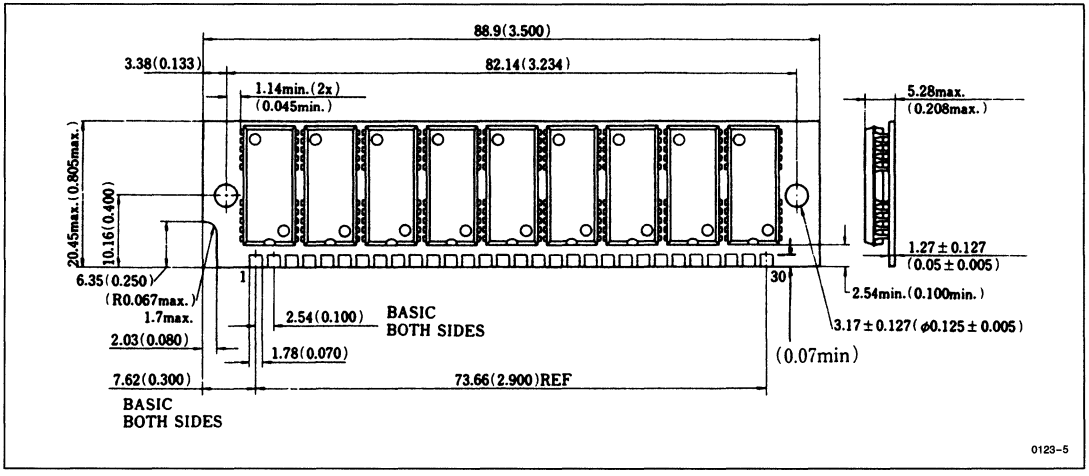
• HB56C19A Series



• HB56C19AT Series



• HB56C19B Series



Note: 1. The plating of the contact finger is solder coat.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	9.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HB56C19A/AT/B						Unit	Test Conditions	Note
		-8A		-10A		-12A				
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	630	—	540	—	450	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	18	—	18	—	18	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	9	—	9	—	9	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	540	—	450	—	405	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	45	—	45	—	45	mA	$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	540	—	450	—	360	mA	t_{RC} = Min	
Static Column Mode Current	I_{CC9}	—	540	—	450	—	360	mA	Static Column Mode t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Currernt	I_{LO}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	60	pF	1
Input Capacitance (Clock)	C_{I2}	—	75	pF	1, 2
Input/Output Capacitance (DQ_0–DQ_7)	$C_{I/O}$	—	17	pF	1, 2
Input Capacitance (PD)	C_{I3}	—	10	pF	1
Output Capacitance (PQ)	C_O	—	12	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics**

Please show at HM511002A series about AC Characteristics. But don't use by Delayed Write Cycle, because the HB56C19 provides common data inputs and outputs. Please use by Early Write Cycle. ($t_{WCS} \geq t_{WCS}$ (min)).

HB56G19 Series

1,048,576-Word x 9-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56G19 is a 1M x 9 dynamic RAM module, mounted two 4 Mbit DRAM (HM514400AS) sealed in SOJ package and 1 Mbit DRAM (HM511000AJP) sealed in SOJ package. An outline of the HB56G19 is 30-pin single in-line package having lead types (HB56G19A), socket type (HB56G19B/GB). Therefore, the HB56G19 makes high density mounting possible without surface mount technology. The HB56G19 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath each SOJ.

■ FEATURES

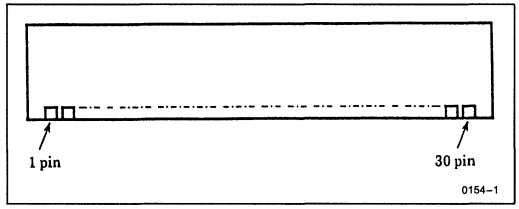
- 30-pin Single In-line Package
  - Lead Pitch 2.54mm
- Single 5V (±10%) Supply
- High Speed
  - Access Time ..... 60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode ..... 1705 mW/1540 mW/1375 mW/1210 mW (max)
  - Standby Mode ..... 33 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycle ..... (16 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

Part No.	Access Time	Package
HB56G19A-6A	60 ns	30-pin SIP Low Profile Lead Type
HB56G19A-7A	70 ns	
HB56G19A-8A	80 ns	
HB56G19A-10A	100 ns	
HB56G19B/GB-6A	60 ns	30-pin SIP Socket Type
HB56G19B/GB-7A	70 ns	
HB56G19B/GB-8A	80 ns	
HB56G19B/GB-10A	100 ns	

Note: Following the specification of the contact pads.
HB56G19B-XX :solder
HB56G19GB-XX :gold

■ PIN OUT

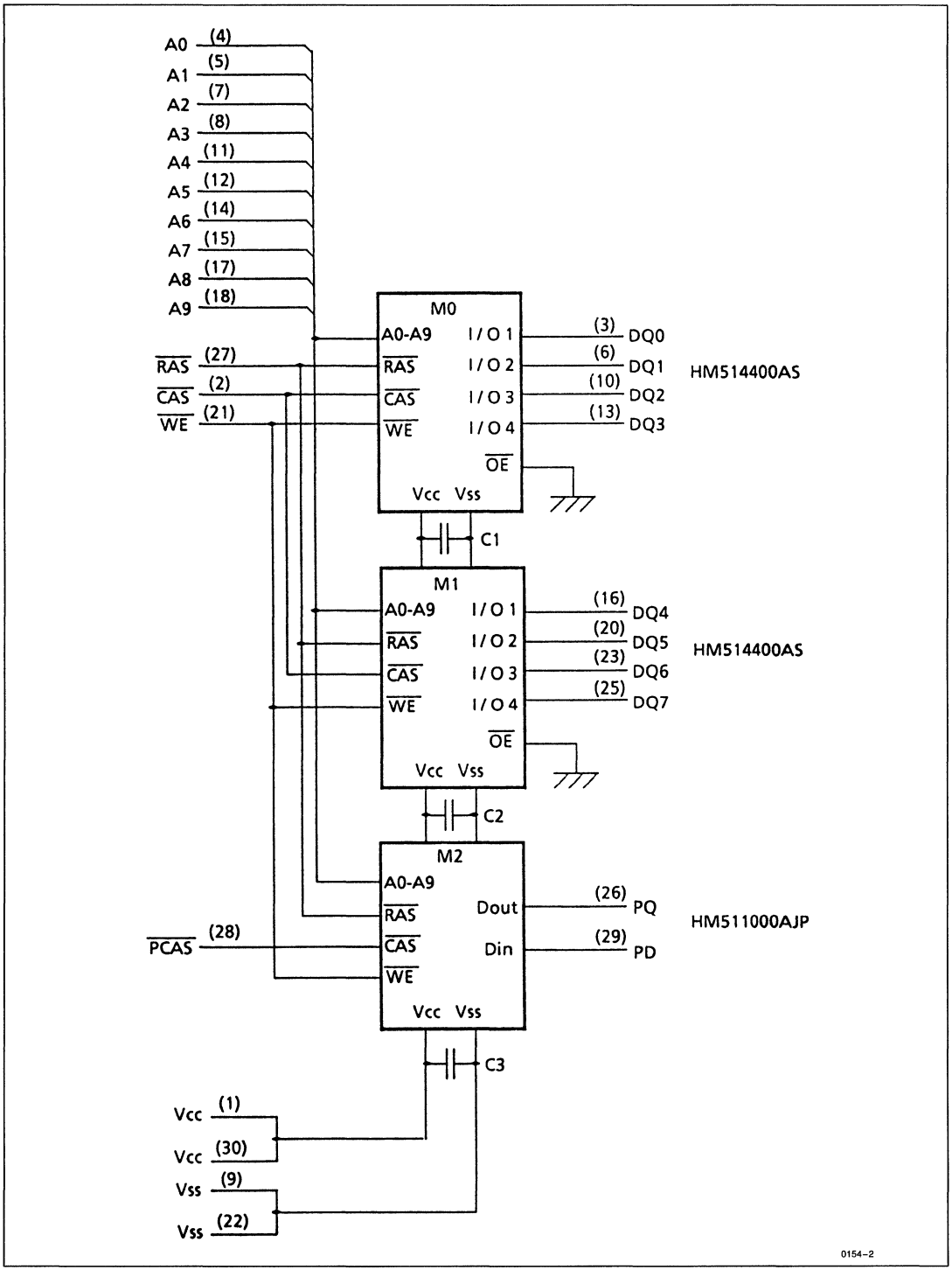


Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CAS}$	17	A_8
3	DQ_0	18	A_9
4	A_0	19	NC
5	A_1	20	DQ_5
6	DQ_1	21	$\overline{WE}$
7	A_2	22	V_{SS}
8	A_3	23	DQ_6
9	V_{SS}	24	NC
10	DQ_2	25	DQ_7
11	A_4	26	PQ
12	A_5	27	$\overline{RAS}$
13	DQ_3	28	$\overline{PCAS}$
14	A_6	29	PD
15	A_7	30	V_{CC}

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_9	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$, $\overline{PCAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
DQ_0–DQ_7	Data-in/Data-out
PD	Parity Data-in
PQ	Parity Data-out
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	No Connection

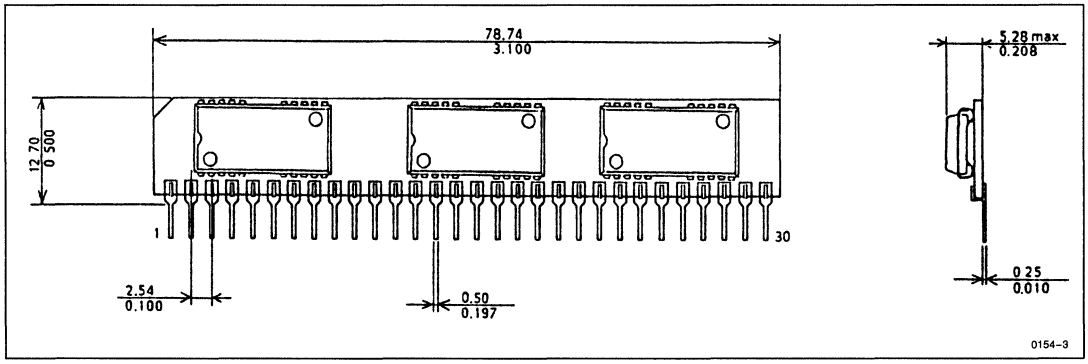
■ BLOCK DIAGRAM



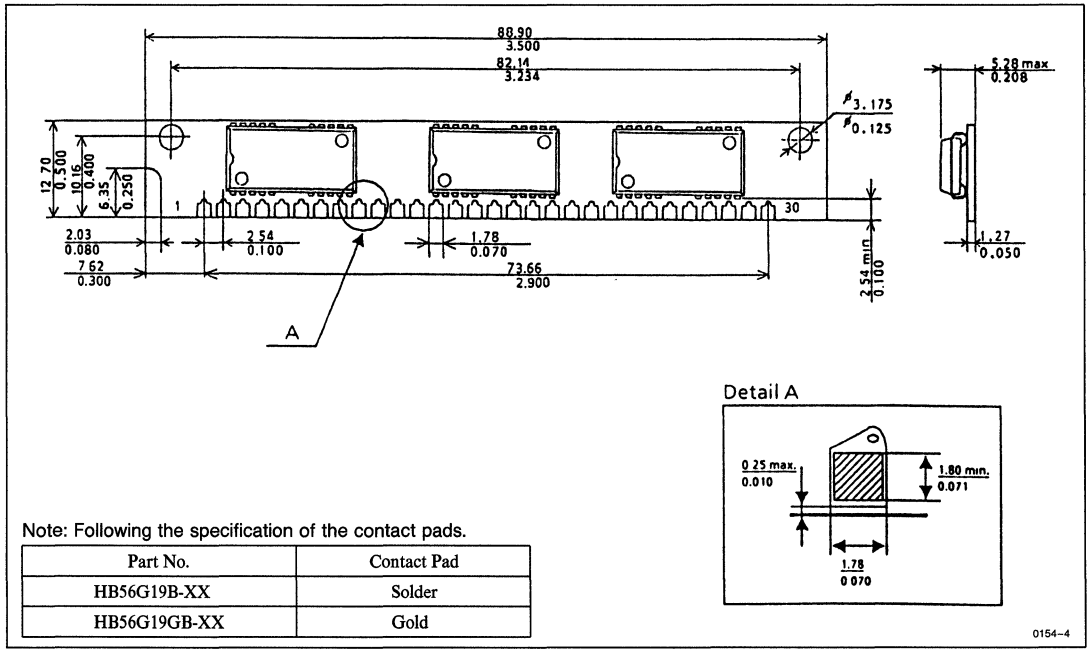
■ PHYSICAL OUTLINE

Unit: mm / inch

• HB56G19A Series



• HB56G19B/GB Series



Note: Following the specification of the contact pads.

Part No.	Contact Pad
HB56G19B-XX	Solder
HB56G19GB-XX	Gold

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input)	V_{in}	−1.0 to +7.0	V
	(Output)	V_{out}	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	8	W
Operating Temperature		T_{opr}	0 to +70	°C
Storage Temperature		T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HB56G19A/B/GB								Unit	Test Conditions	Note
		-6A		-7A		-8A		-10A				
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	310	—	280	—	250	—	220	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	6	—	6	—	6	—	6	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	3	—	3	—	3	—	3	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	310	—	280	—	240	—	210	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	15	—	15	—	15	—	15	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	300	—	270	—	240	—	210	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	300	—	270	—	230	—	210	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed ≤1 time while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	30	pF	1
Input Capacitance (Clock)	C_{I2}	—	36	pF	1
Input/Output Capacitance (DQ_{0-7})	$C_{I/O}$	—	17	pF	1, 2
Input Capacitance (PD)	C_{I3}	—	10	pF	1
Output Capacitance (PQ)	C_O	—	12	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Electrical Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 12]

Read, Write, and Refresh Cycles (Common Parameters)

Parameter	Symbol	HB56G19A/B/GB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	120	—	130	—	160	—	190	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	50	—	70	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	—	16	ms	15

Read Cycle

Parameter	Symbol	HB56G19A/B/GB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	20	0	20	0	25	ns	6

Write Cycle

Parameter	Symbol	HB56G19A/B/GB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	20	—	ns	11

Refresh Cycle

Parameter	Symbol	HB56G19A/B/GB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	15	—	20	—	20	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

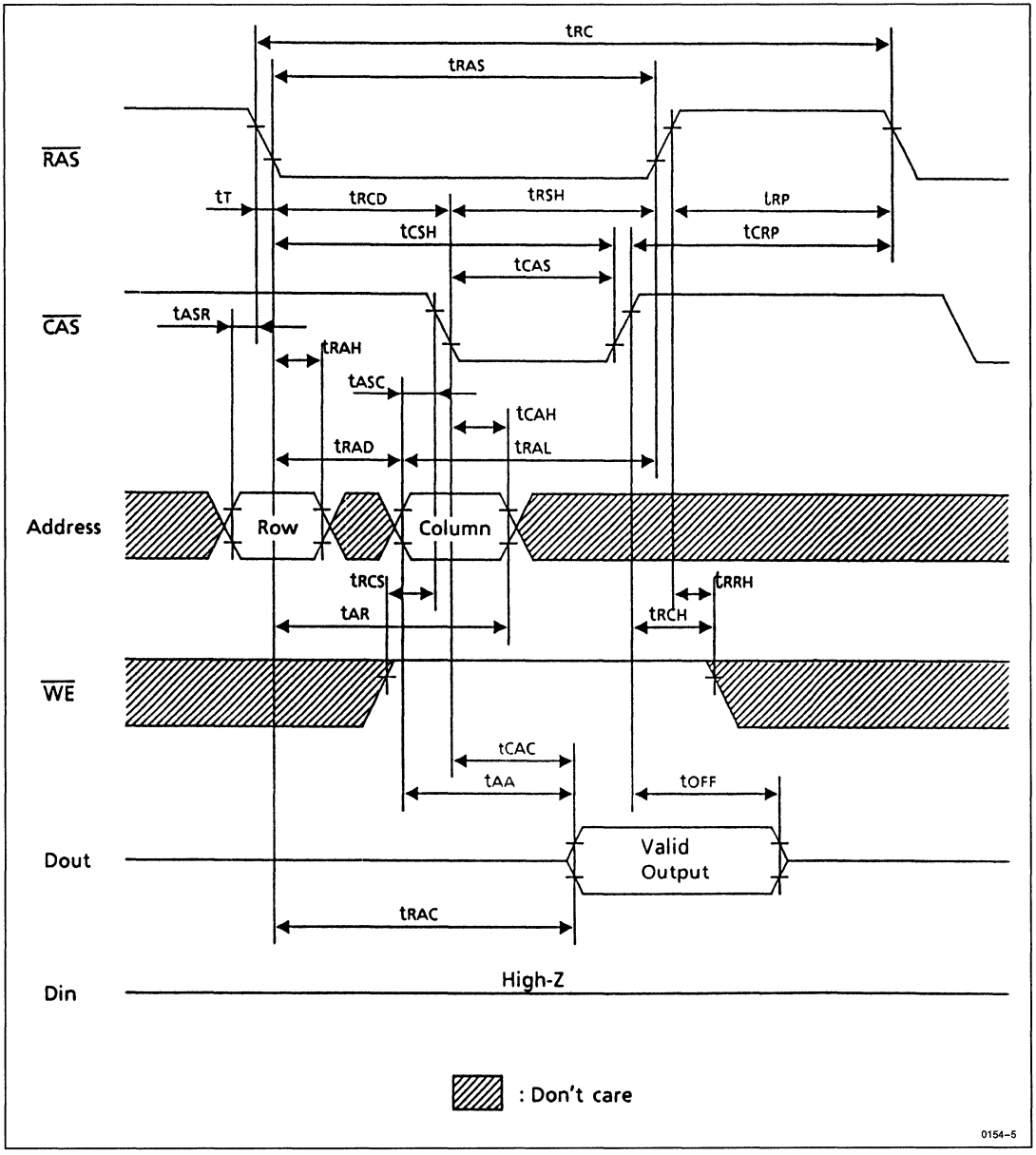
Fast Page Mode Cycle

Parameter	Symbol	HB56G19A/B/GB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	60	100000	70	100000	80	100000	100	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	—	50	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	50	—	ns	

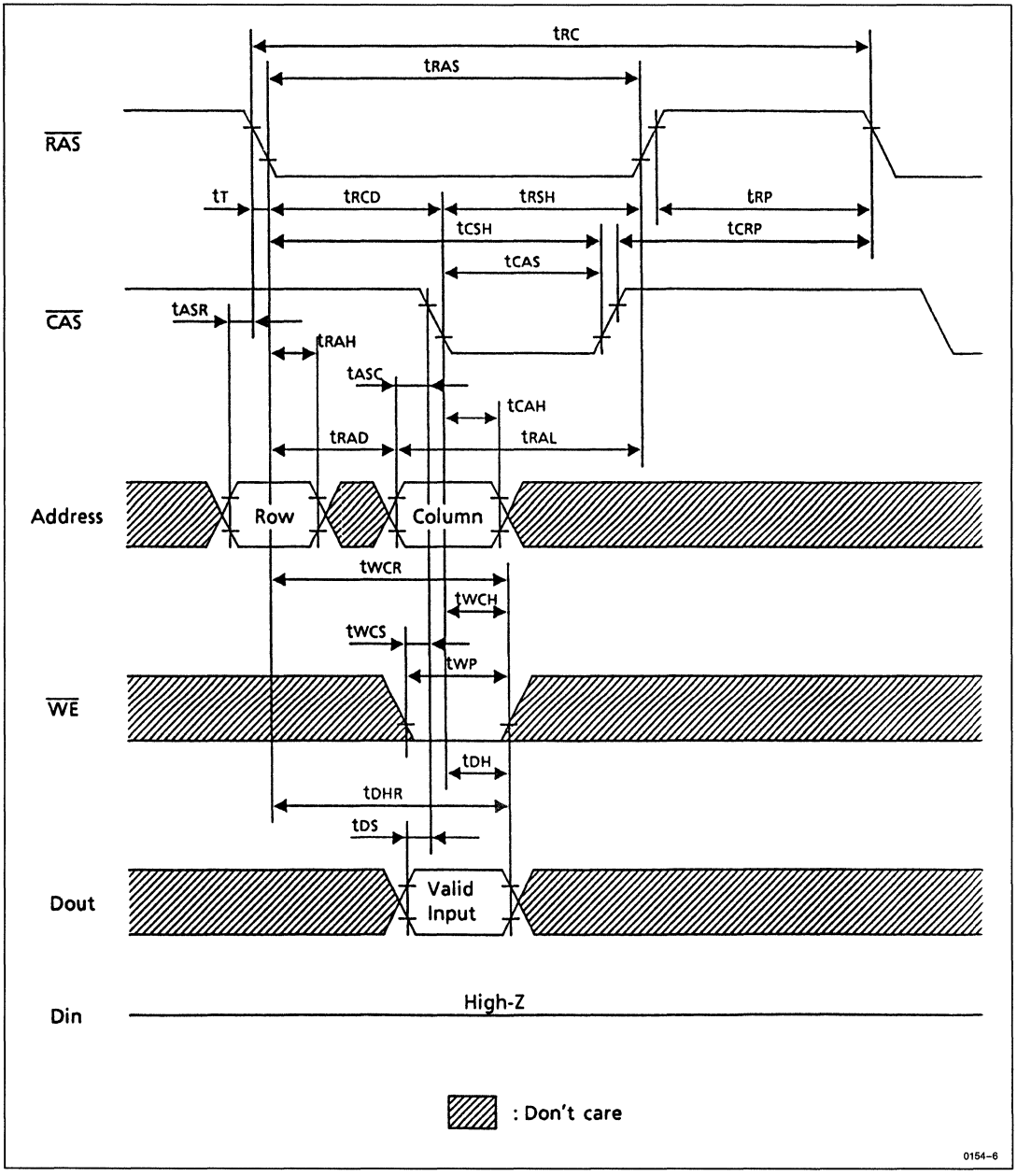
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is determined by 1,024 refresh cycles.

■ TIMING WAVEFORMS

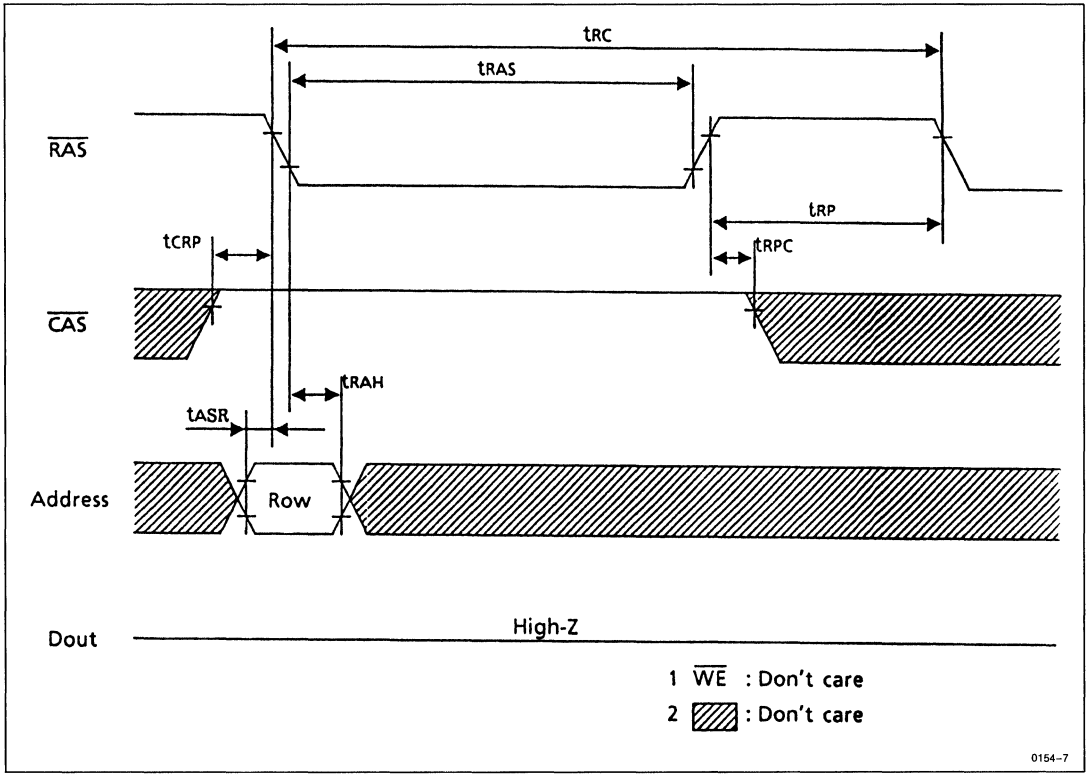
• Read Cycle



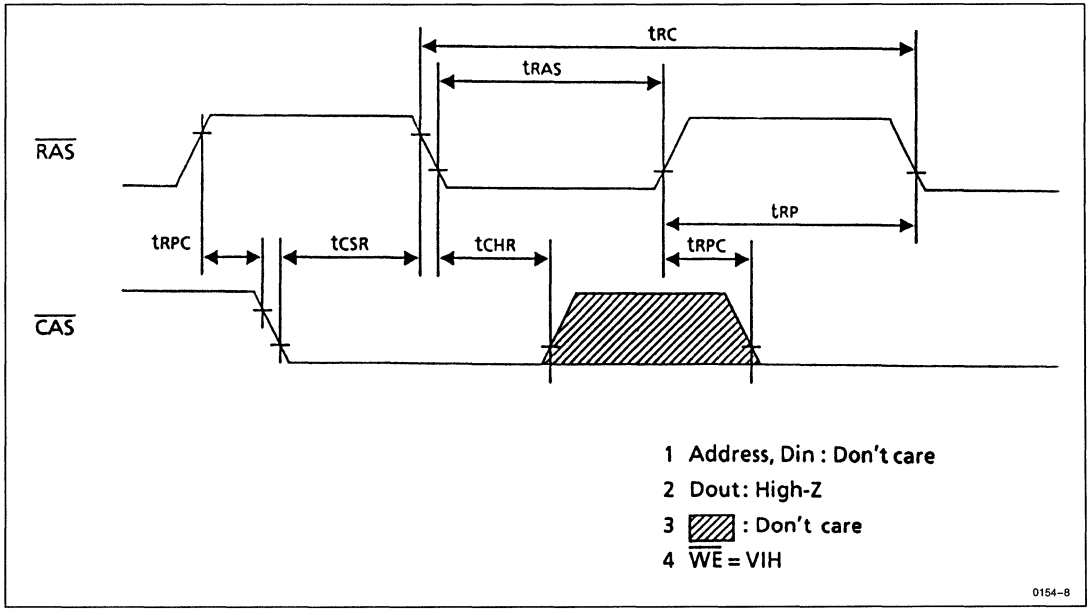
• **Early Write Cycle**



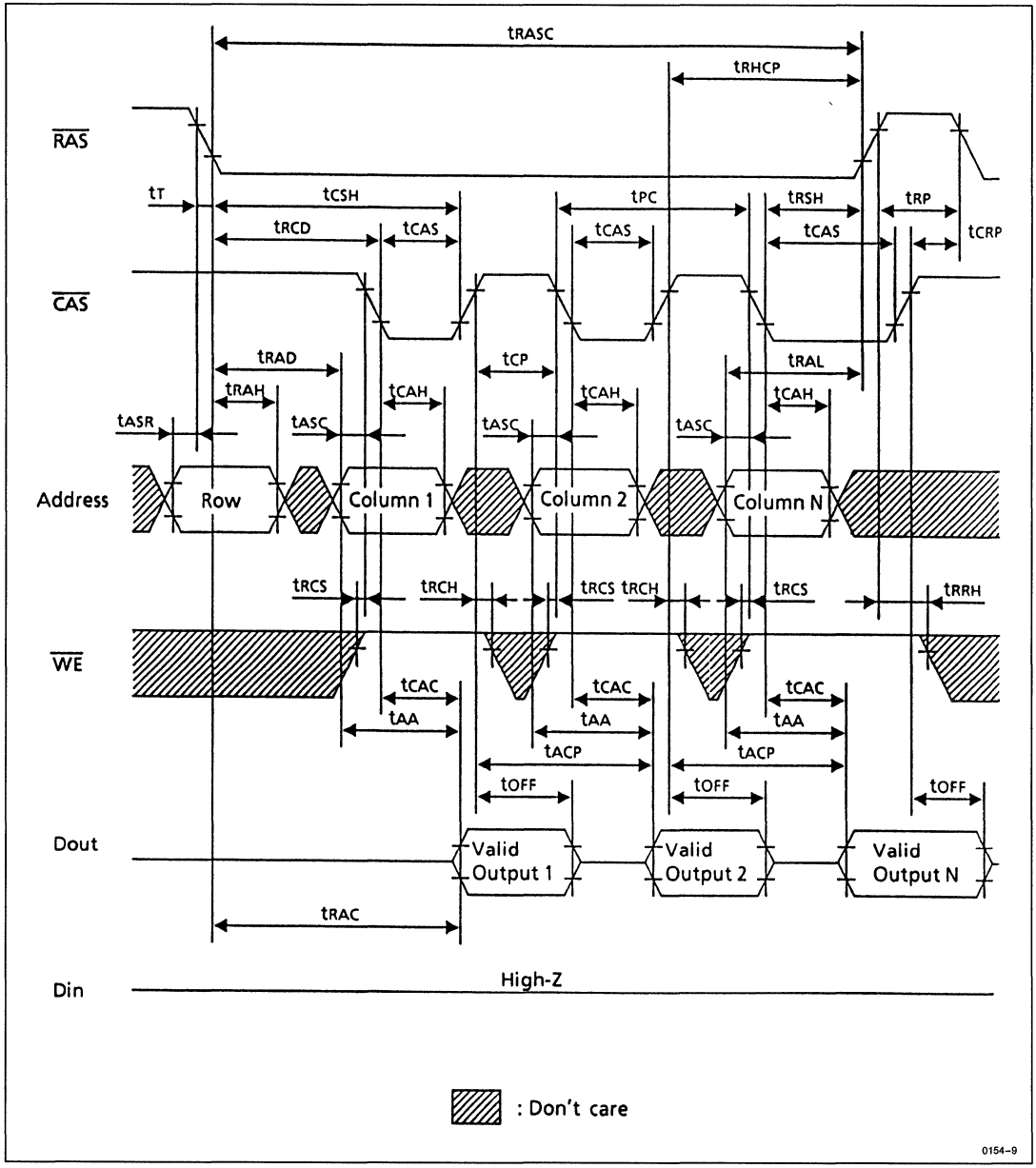
• $\overline{RAS}$ Only Refresh Cycle



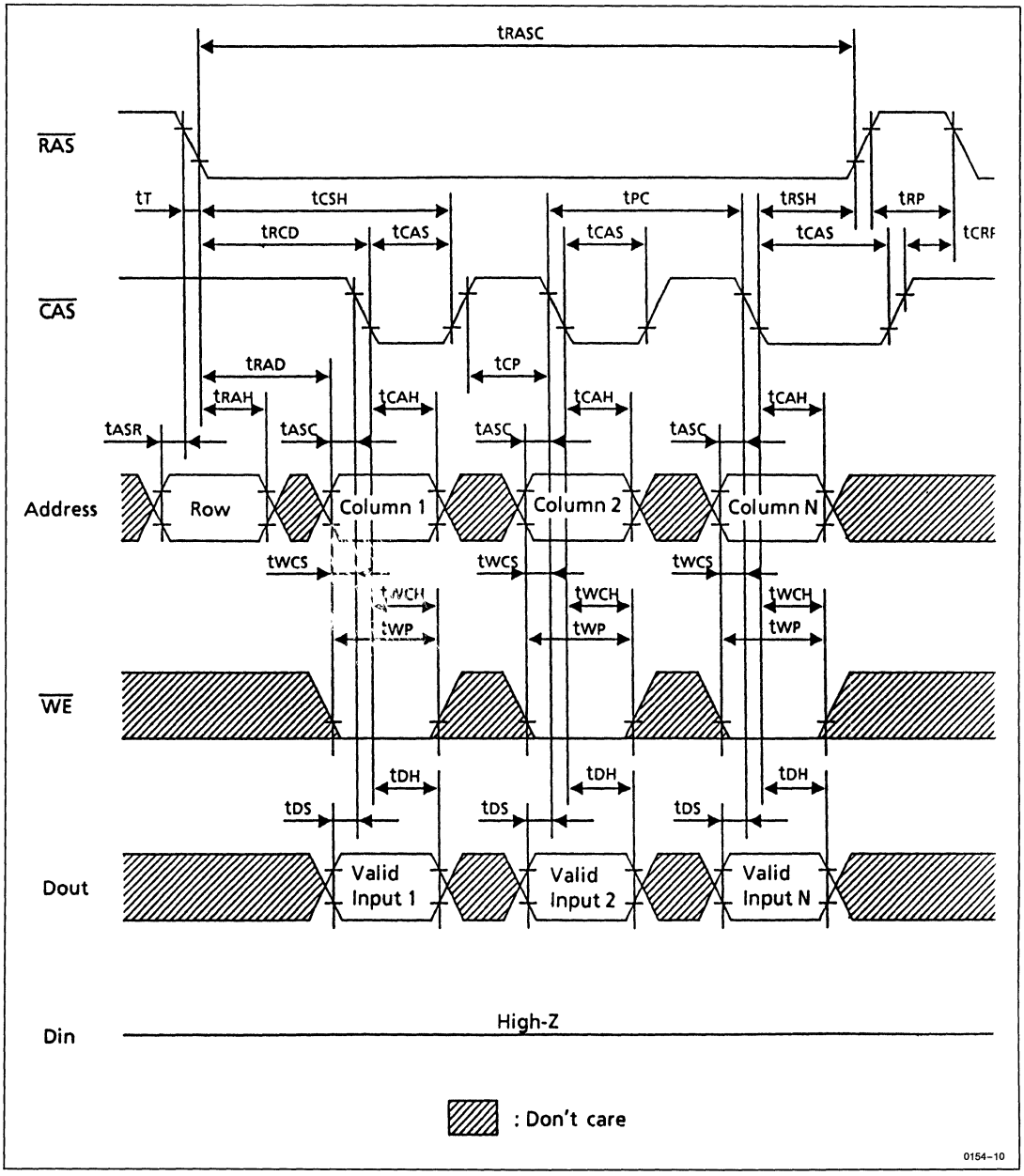
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



HB56A49 Series

4,194,304-Word x 9-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56A49 is a 4M x 9 dynamic RAM module, mounted 9 pieces of 4 Mbit DRAM (HM514100AS, HM514100JP) sealed in an SOJ package. An outline of the HB56A49 is the 30-pin single in-line package. Therefore, the HB56A49 makes high density mounting possible without surface mount technology. The HB56A49 provides common data inputs and outputs, and also provides separate I/O parity bit for parity check. Decoupling capacitors are mounted beneath each SOJ.

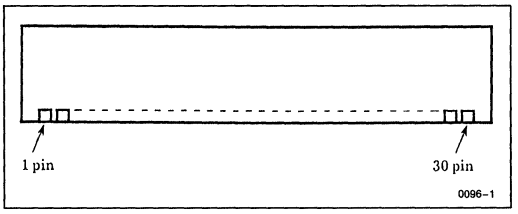
■ FEATURES

- 30-pin Single In-line Package
  - Lead Pitch 2.54mm
- Single 5V (±10%) Supply
- High Speed
  - Access Time .....60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode .....5445 mW/4059 mW/4455 mW/3960 mW (max)
  - Standby Mode.....99 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycle .....(16 ms)
- 3 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_{10}	Address Input
A_0–A_9	Refresh Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$, $P\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
DQ_0–DQ_7	Data-in/Data-out
PD	Parity Data-in
PQ	Parity Data-out
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	No Connection

■ PIN OUT



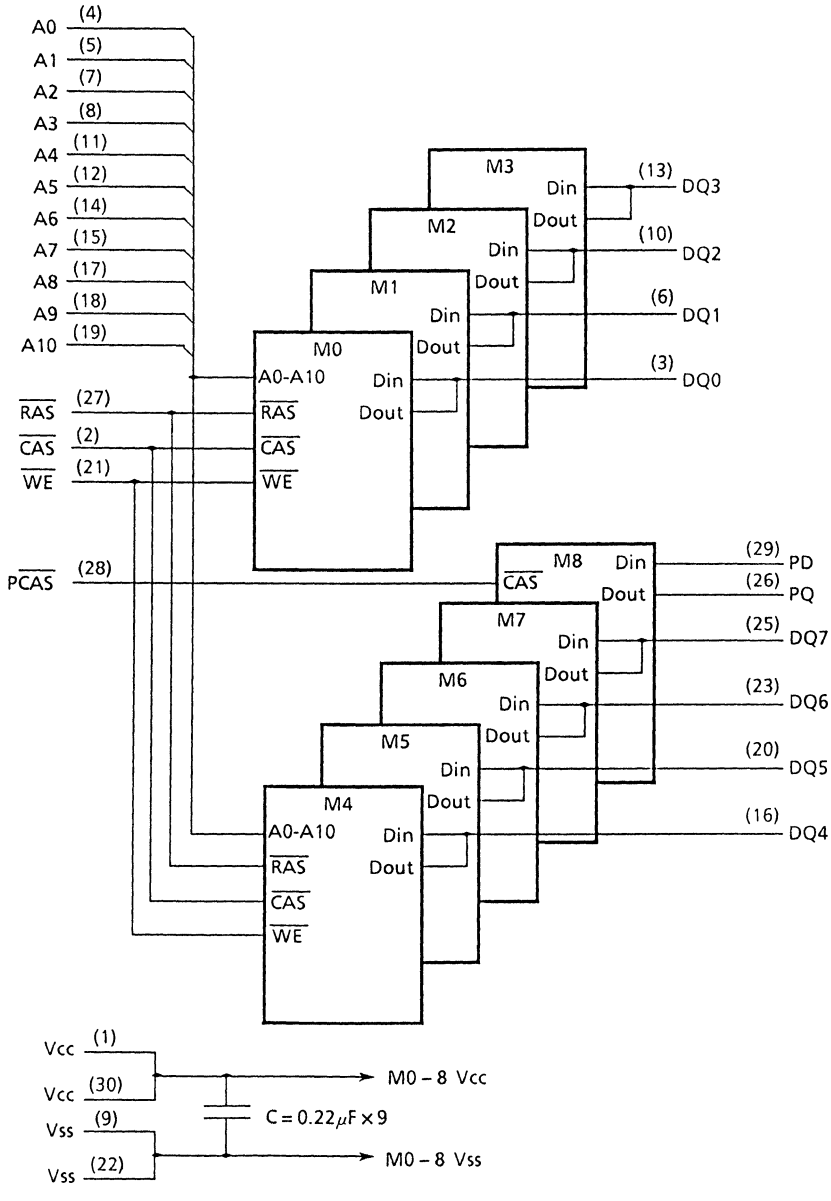
Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC}	16	DQ_4
2	$\overline{CAS}$	17	A_8
3	DQ_0	18	A_9
4	A_0	19	A_{10}
5	A_1	20	DQ_5
6	DQ_1	21	$\overline{WE}$
7	A_2	22	V_{SS}
8	A_3	23	DQ_6
9	V_{SS}	24	NC
10	DQ_2	25	DQ_7
11	A_4	26	PQ
12	A_5	27	$\overline{RAS}$
13	DQ_3	28	$P\overline{CAS}$
14	A_6	29	PD
15	A_7	30	V_{CC}

■ ORDERING INFORMATION

Access Time	Package					
	30-pin [1] SIP Socket Type	30-pin [1] SIP Socket Type	30-pin SIP Lead Type	30-pin SIP Lead Type	30-pin SIP Low Profile Lead Type	30-pin SIP Low Profile Lead Type
	0.945 Inch Height	0.805 Inch Height	0.989 Inch Height	0.810 Inch Height	0.591 Inch Height	0.500 Inch Height
60 ns	—	HB56A49BR/GBR-6A	—	HB56A49AR-6A	—	HB56A49ATR-6A
70 ns	—	HB56A49BR/GBR-7A	—	HB56A49AR-7A	—	HB56A49ATR-7A
80 ns	HB56A49B/GB-8	HB56A49BR/GBR-8A	HB56A49A-8	HB56A49AR-8A	HB56A49AT-8	HB56A49ATR-8A
100 ns	HB56A49B/GB-10	HB56A49BR/GBR-10A	HB56A49A-10	HB56A49AR-10A	HB56A49AT-10	HB56A49ATR-10A

Note: 1. Following the specification of the contact pad.
HB56A49B-XX, HB56A49BR-XX: solder
HB56A49GB-XX, HB56A49GBR-XX: gold

■ BLOCK DIAGRAM

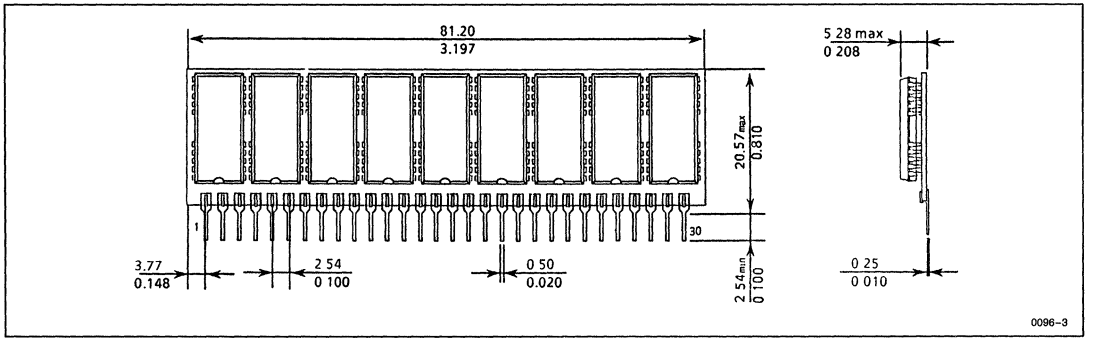


Note: M0–M8[HB56A49XX-XXA]: HM514100AS
M0–M8[HB56A49XX-8/10]: HM514100JP

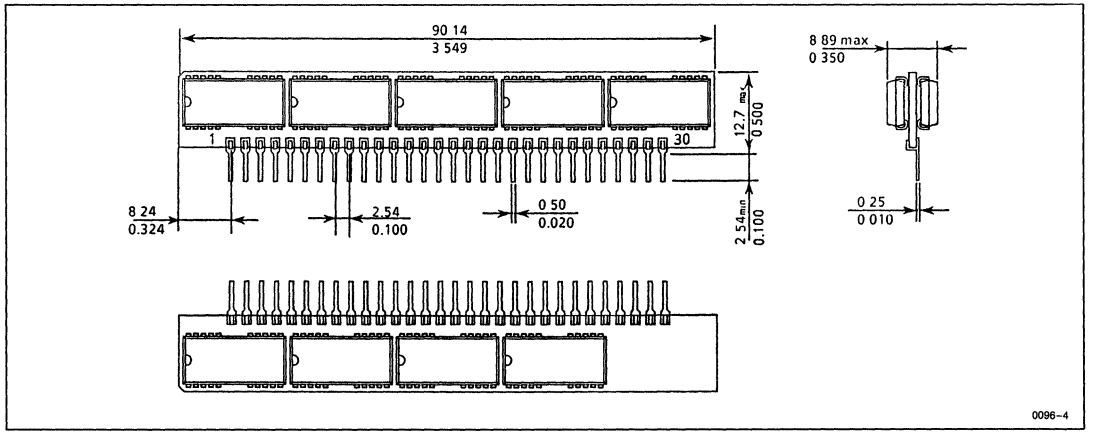
■ PHYSICAL OUTLINE

Unit: mm / inch

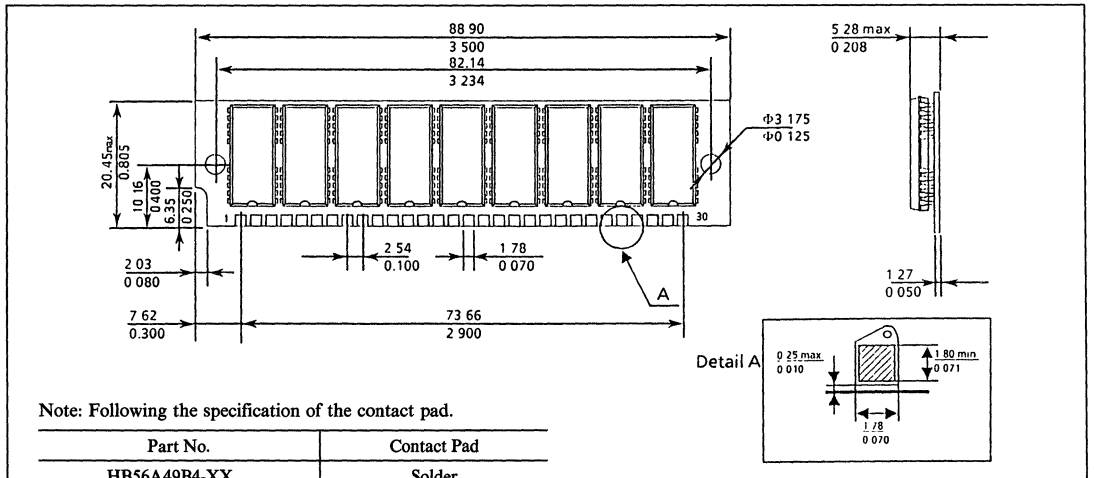
• HB56A49AR Series



• HB56A49ATR Series



• HB56A49BR/GBR Series

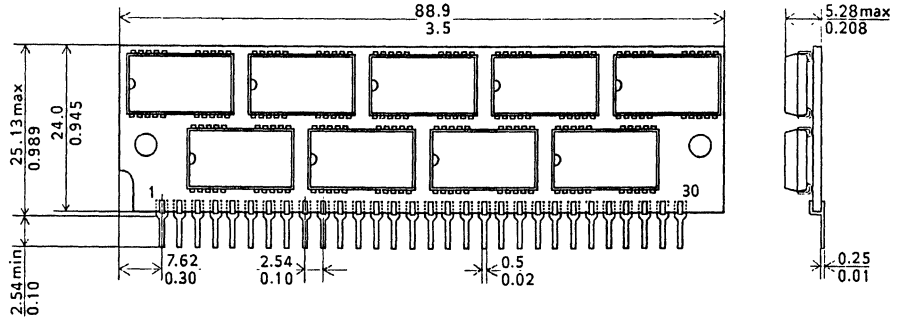


Note: Following the specification of the contact pad.

Part No.	Contact Pad
HB56A49B4-XX	Solder
HB56A49GBR-XX	Gold

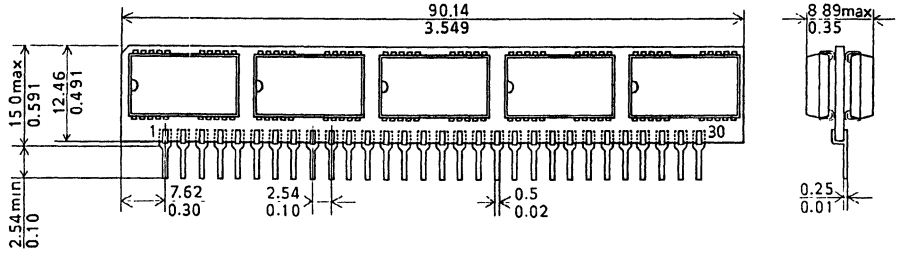
• **HB56A49A Series**

Unit: mm / inch



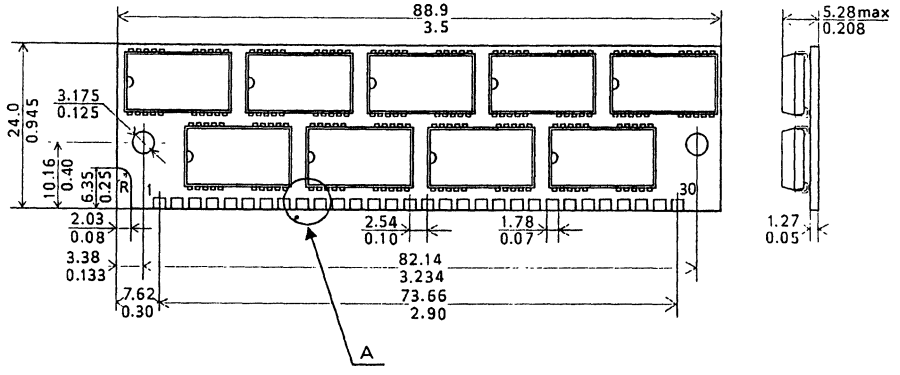
0096-6

• **HB56A49AT Series**



0096-7

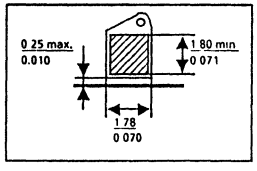
• **HB56A49B/GB Series**



0096-8

Note: Following the specification of the contact pad.

Part No.	Contact Pad
HB56A49B-XX	Solder
HB56A49GB-XX	Gold



Detail A

0096-9

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	9	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	− 0.5	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR								Unit	Test Condition	Note
		-6A		-7A		-8/-8A		-10/-10A				
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	990	—	900	—	810	—	720	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	18	—	18	—	18	—	18	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	9	—	9	—	9	—	9	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	990	—	900	—	810	—	720	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	45	—	45	—	45	—	45	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	990	—	900	—	810	—	720	mA	t_{RC} = Min	
Page Mode Current	I_{CC7}	—	990	—	900	—	810	—	720	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{IN} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±10%)

Parameter	Symbol	HB56A49				Unit	Note
		BR/GBR/AR/ATR		A/AT/B/GB			
		Typ	Max	Typ	Max		
Input Capacitance (Address)	C_{I1}	—	60	—	70	pF	1
Input Capacitance (Clock)	C_{I2}	—	75	—	88	pF	1
Input Capacitance ($\overline{PCAS}$)	C_{I3}	—	12	—	20	pF	1
Input/Output Capacitance (DQ_{0-7})	$C_{I/O}$	—	17	-	30	pF	1, 2
Input Capacitance (PD)	C_{I4}	—	10	—	20	pF	1
Output Capacitance (PQ)	C_O	—	12	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 12, 15]

Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Ramdon Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	180	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	70	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10000	20	10000	20	10000	25	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	15	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	20	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	50	20	50	20	60	25	75	20	60	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	35	15	35	15	40	20	55	15	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	20	—	25	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	—	16	—	16	—	16	ms	17

Read Cycle

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	80	—	100	ns	2, 3, 16
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	—	25	—	25	—	25	ns	3, 4, 14
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	40	—	45	ns	3, 5, 14, 16
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	

Read Cycle (continued)

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	0	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	40	—	45	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	15	0	20	0	20	0	25	0	20	0	25	ns	6

Write Cycle

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	15	—	20	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	10	—	20	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	20	—	25	—	25	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	20	—	20	—	25	—	25	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	20	—	15	—	20	—	ns	11

Refresh Cycle

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	10	—	20	—	20	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	55	—	55	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	—	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	35	—	40	—	45	—	50	—	50	—	50	ns	14, 16
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	45	—	50	—	50	—	50	—	ns	

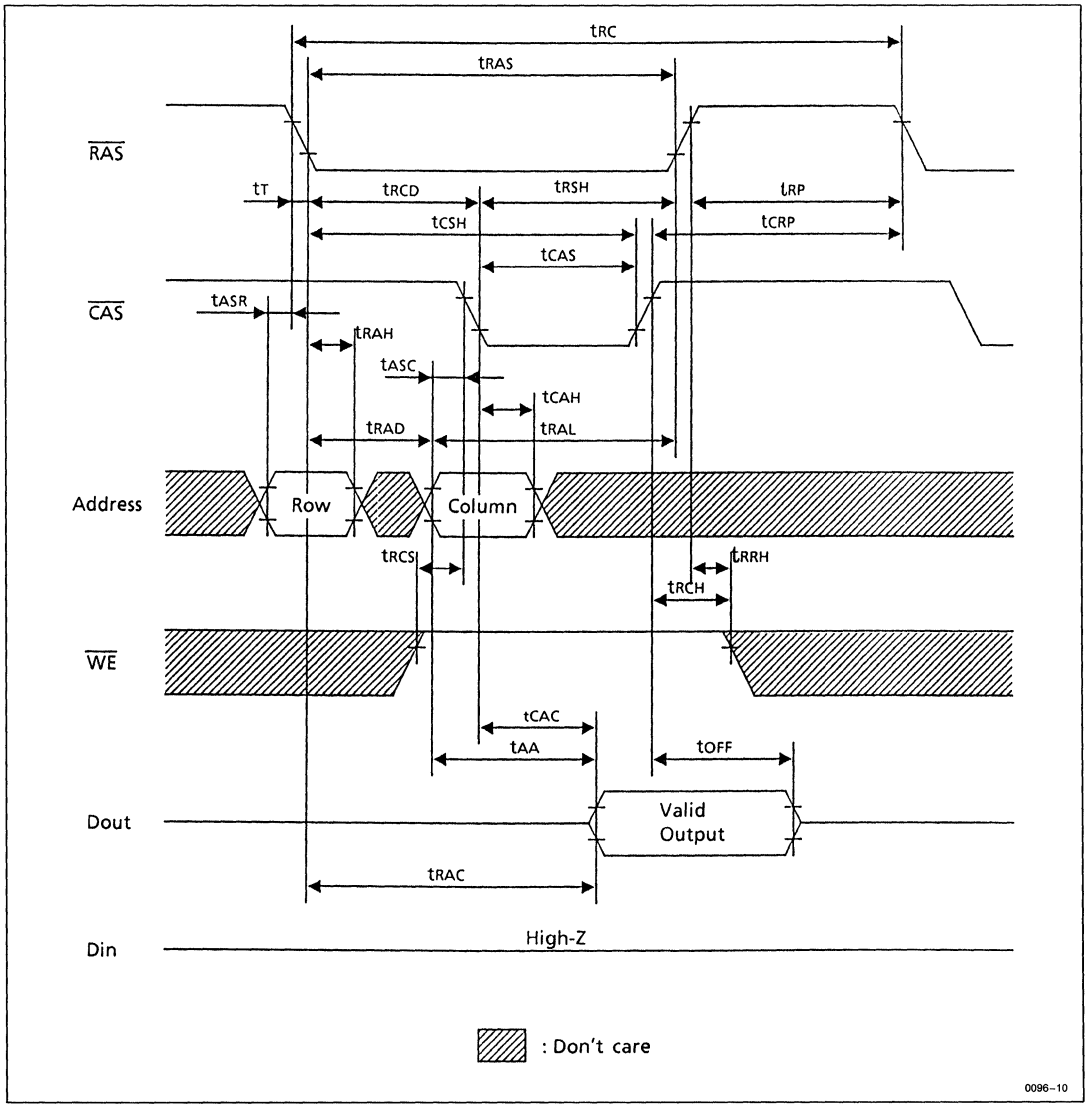
Test Mode Cycle

Parameter	Symbol	HB56A49B/GB/BR/GBR/A/AR/AT/ATR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	10	—	10	—	10	—	10	—	20	—	20	—	ns	

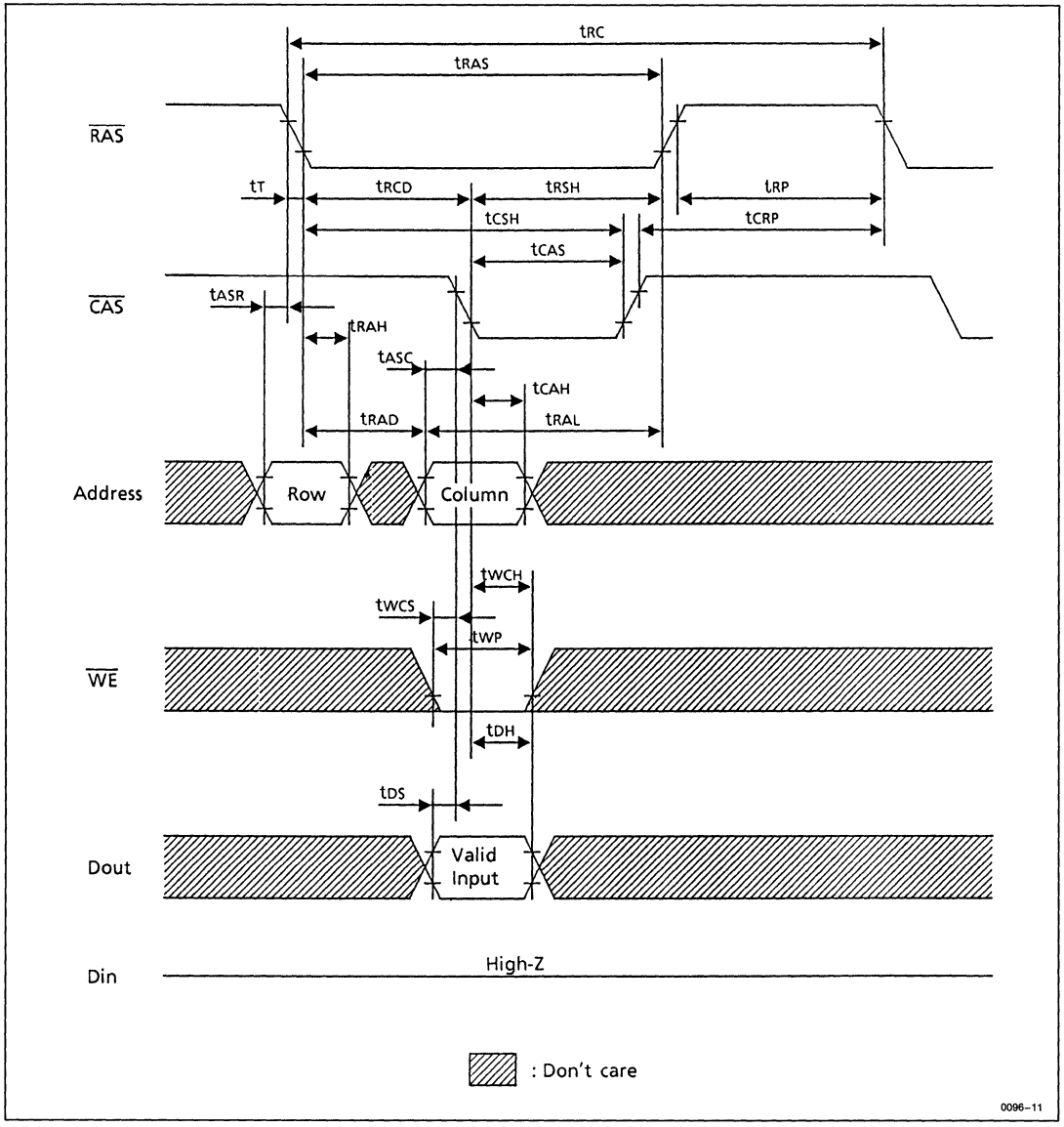
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as RAS only refresh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CAP}.
15. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits . . . RA10, CA10 and CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is D_{out} and data input pin is D_{in}. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
16. In a test mode read cycle, the value of t_{RAC}, t_{AA} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
17. t_{REF} is determined by 1,024 refresh cycles.

■ TIMING WAVEFORM

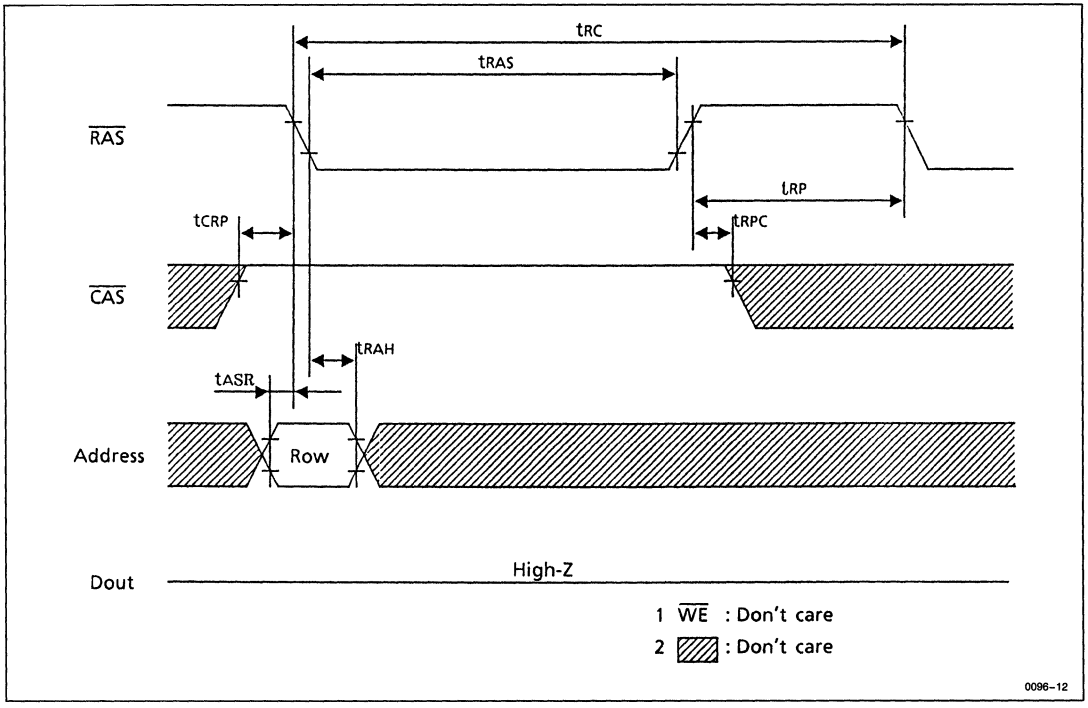
• Read Cycle



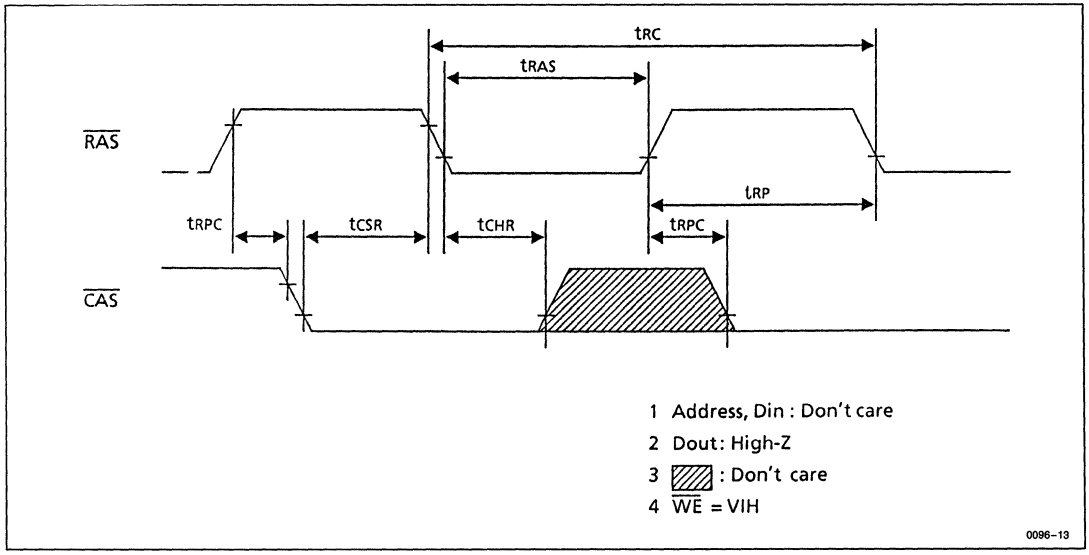
• **Early Write Cycle**



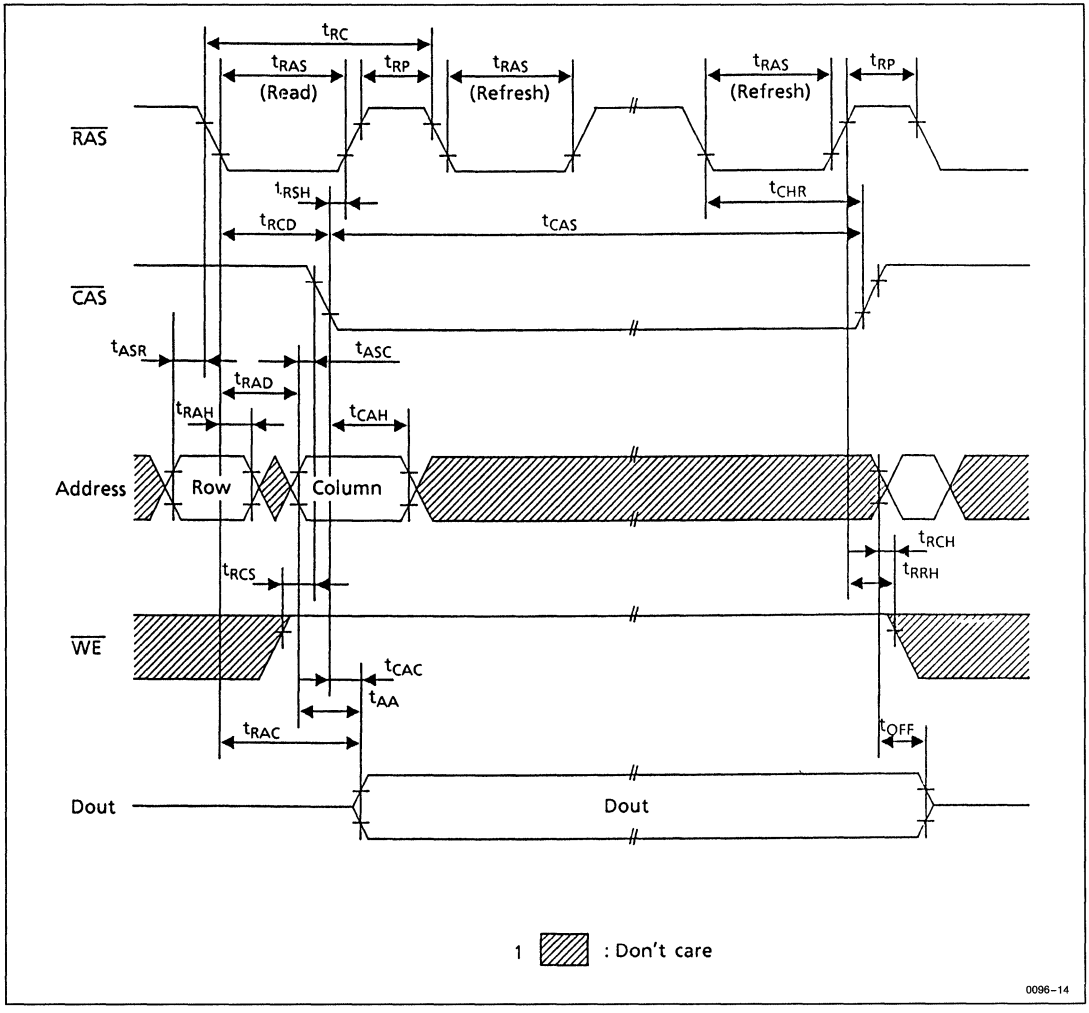
• $\overline{RAS}$ Only Refresh Cycle



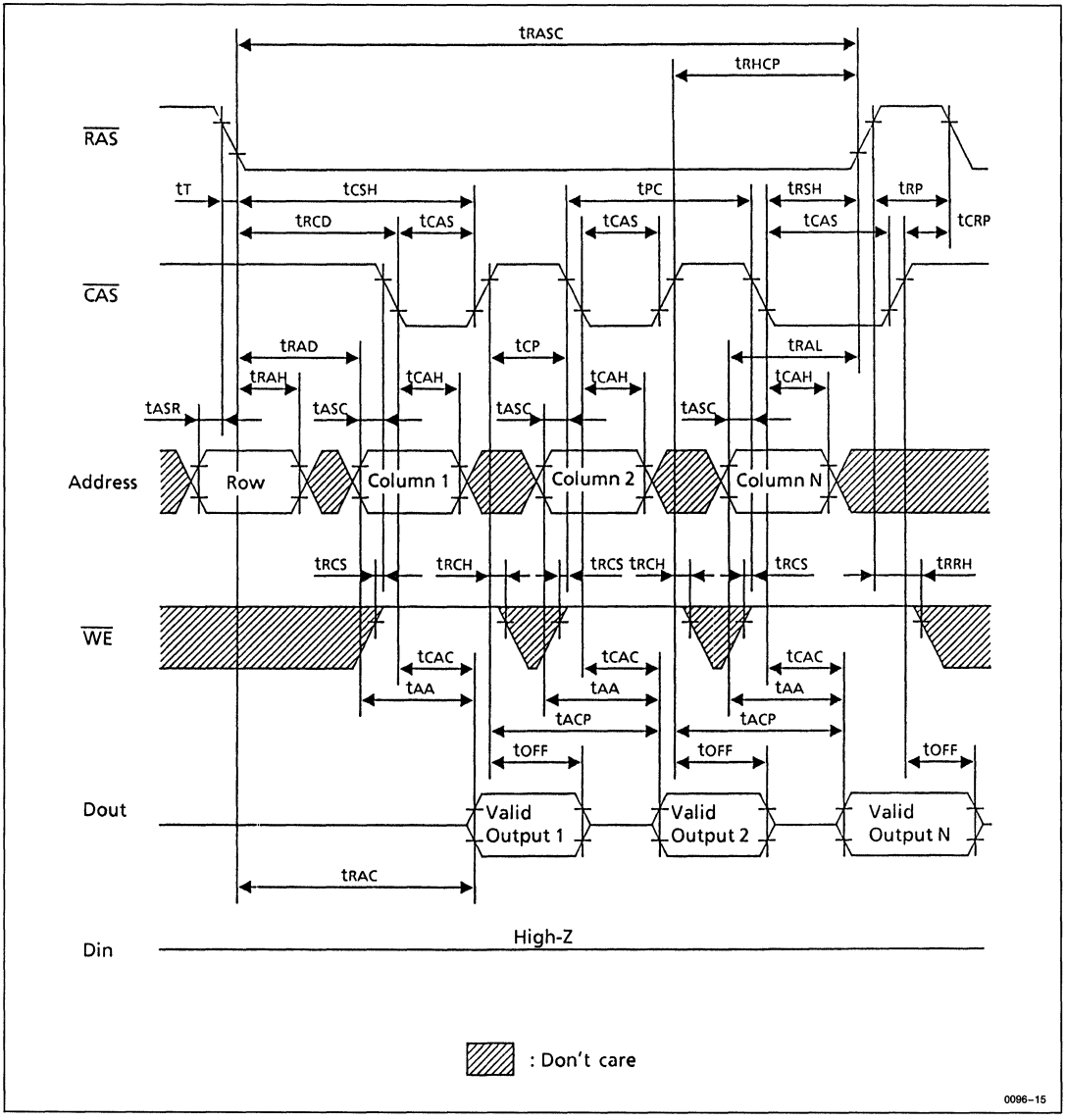
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



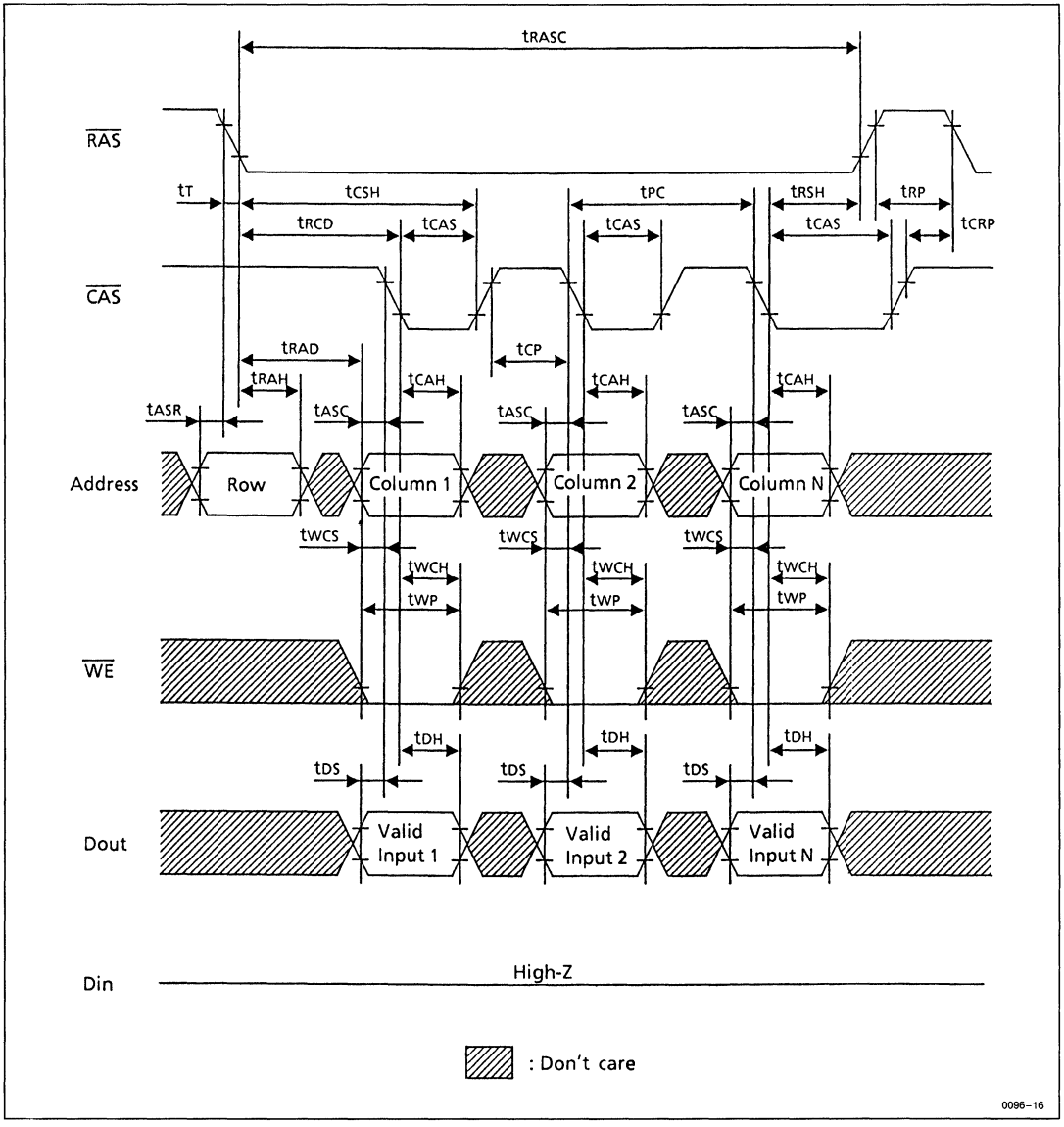
• **Hidden Refresh Cycle**



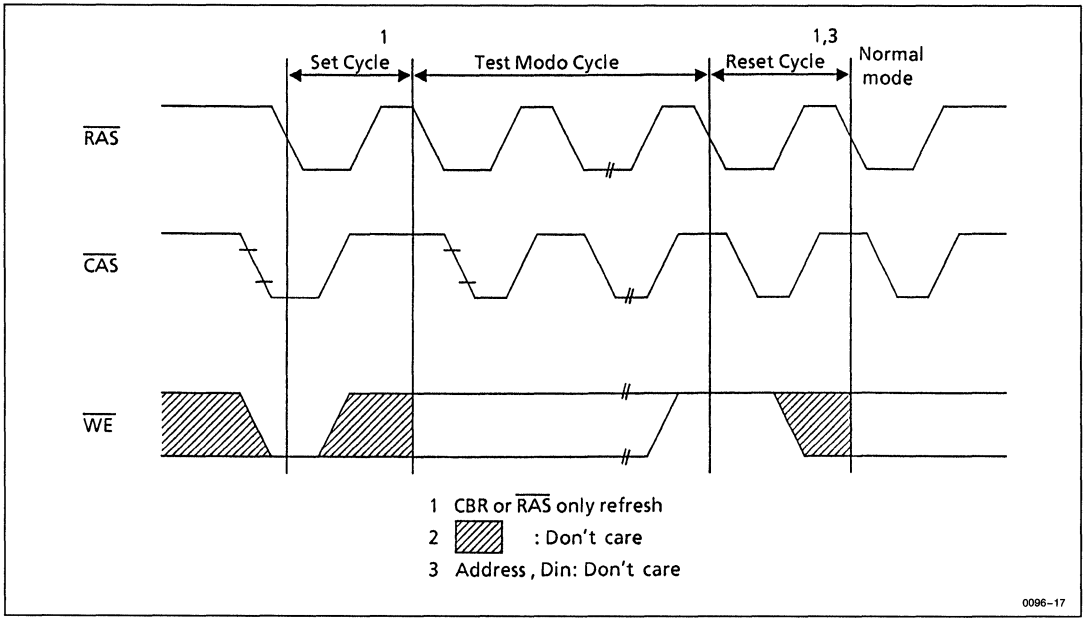
• **Fast Page Mode Read Cycle**



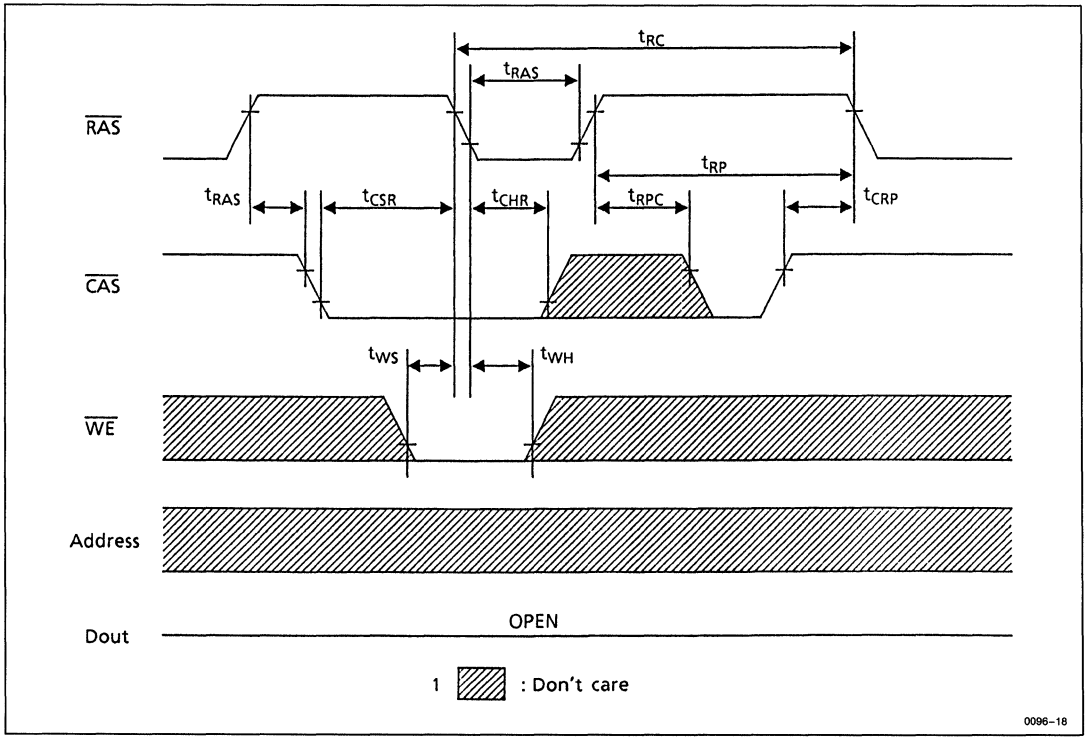
• **Fast Page Mode Early Write Cycle**



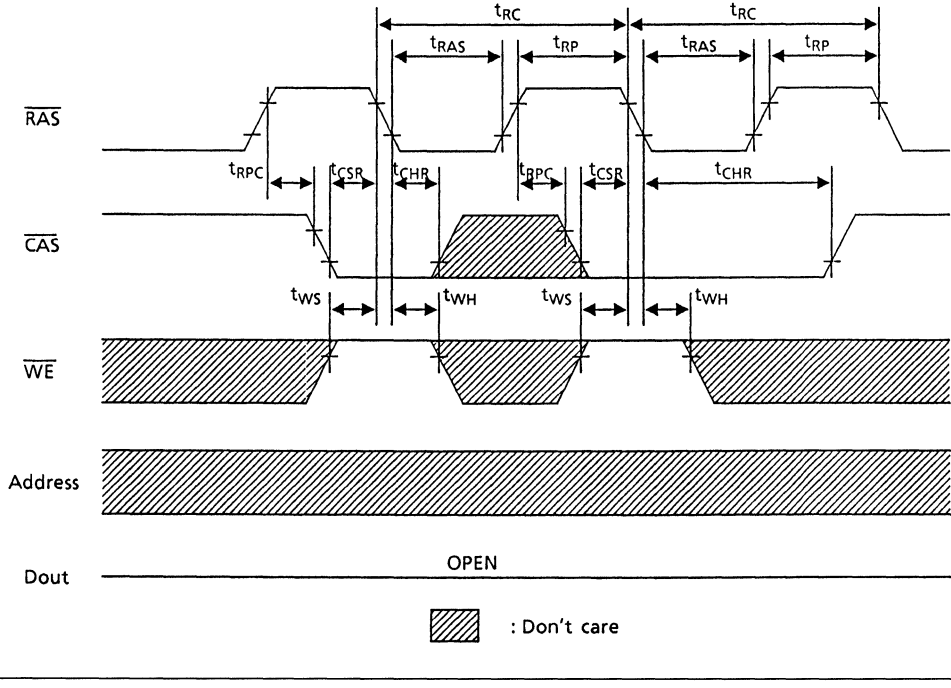
• **TEST MODE CYCLE**



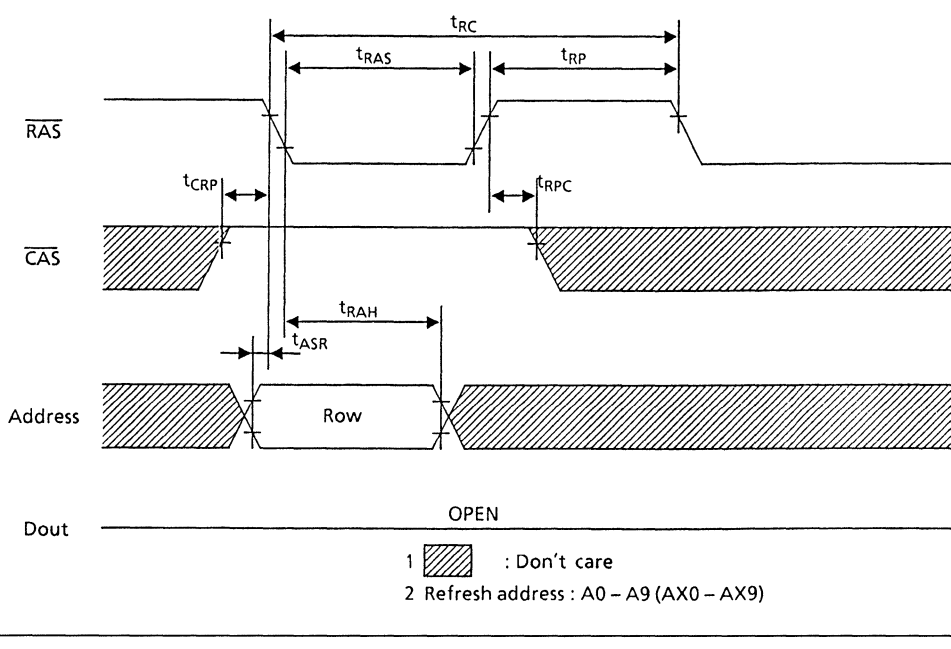
• **Test Mode Set Cycle**



• **Test Mode Reset Cycle**
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



$\overline{RAS}$ Only Refresh Cycle



HB56D25632 Series

262,144-Word x 32-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56D25632B is a 256k x 32 dynamic RAM module, mounted 8 pieces of 1 Mbit DRAM (HM514256JP) sealed in SOJ package. An outline of the HB56D25632B is 72-pin single in-line package. Therefore, the HB56D25632B makes high density mounting possible without surface mount technology. The HB56D25632B provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ.

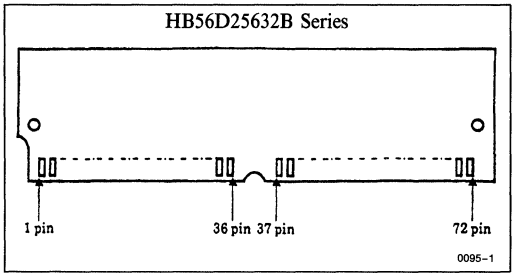
■ FEATURES

- 72-pin Single In-line Package
  - Lead Pitch 1.27mm
- Single 5V (±5%) Supply
- High Speed
  - Access Time ..... 60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode ..... 3.78W/3.36W/2.772W/2.31W/1.974W (max)
  - Standby Mode ..... 84 mW (max)
- Fast Page Mode Capability
- 512 Refresh Cycle/8 ms
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

Part No.	Access Time	Package
HB56D25632B-6A	60 ns	72-pin SIP Socket Type
HB56D25632B-7A	70 ns	
HB56D25632B-8A	80 ns	
HB56D25632B-10A	100 ns	
HB56D25632B-12A	120 ns	

■ PIN OUT

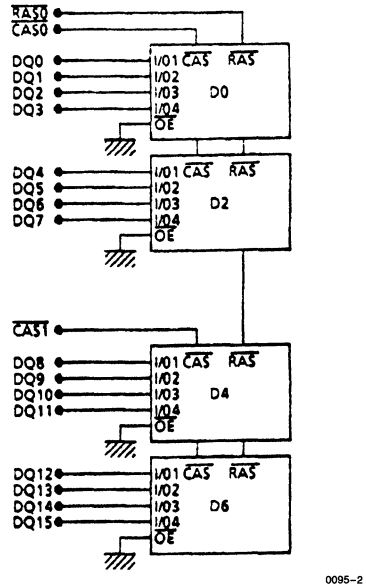


Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	NC	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	V_{SS}	57	DQ12
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ28
5	DQ17	23	DQ21	41	$\overline{CAS2}$	59	V_{CC}
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ29
7	DQ18	25	DQ22	43	$\overline{CAS1}$	61	DQ13
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ30
9	DQ19	27	DQ23	45	NC	63	DQ14
10	V_{CC}	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	$\overline{WE}$	65	DQ15
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	V_{SS}
14	A2	32	NC	50	DQ24	68	NC
15	A3	33	NC	51	DQ9	69	T.B.D.
16	A4	34	$\overline{RAS2}$	52	DQ25	70	T.B.D.
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	V_{SS}

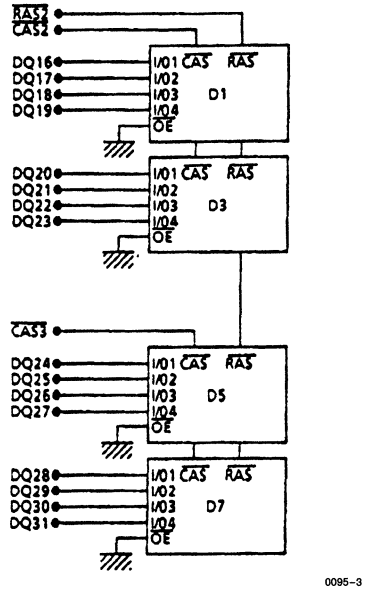
■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Input
A_0–A_8	Refresh Address Input
DQ_0–DQ_{31}	Data-in/Data-out
$\overline{CAS0}$– $\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$– $\overline{RAS2}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

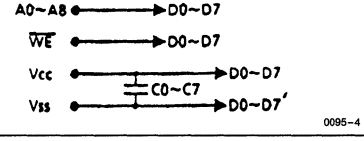
■ BLOCK DIAGRAM



0095-2



0095-3

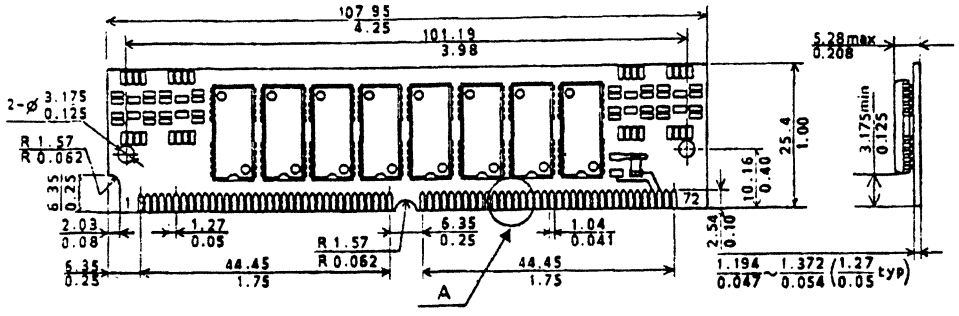


0095-4

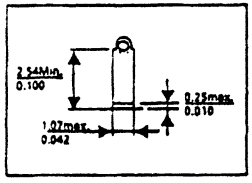
* D0~D7 : HM514256

■ PHYSICAL OUTLINE

Unit: mm / inch



Detail A



Note: The plating of the contact finger is gold.

0095-5

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input)	V_{in}	− 1.0 to + 7.0	V
	(Output)	V_{out}	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	8	W
Operating Temperature		T_{opr}	0 to + 70	°C
Storage Temperature		T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note 1. All voltage referenced to V_{SS}.

• **DC Electrical Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Test Condition	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	720	—	640	—	528	—	440	—	376	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	16	—	16	—	16	—	16	—	16	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	8	—	8	—	8	—	8	—	8	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	720	—	640	—	528	—	440	—	376	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	40	—	40	—	40	—	40	—	40	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	720	—	640	—	528	—	440	—	376	mA	t_{RC} = Min	
Page Mode Current	I_{CC7}	—	720	—	640	—	440	—	440	—	376	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	68	pF	1
Input Capacitance ($\overline{WE}$)	C_{I2}	—	76	pF	1
Input Capacitance ($\overline{RAS}$)	C_{I3}	—	43	pF	1
Input Capacitance ($\overline{CAS}$)	C_{I4}	—	29	pF	1
Output Capacitance (DQ0–DQ31)	$C_{I/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)[1, 12]

Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	125	—	140	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	55	—	60	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	

Read, Write and Refresh Cycle (Common Parameters) (continued)

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ns	15

Read Cycle

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	55	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	—	20	—	20	—	20	—	25	—	30	ns	6

Write Cycle

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	20	—	25	—	ns	11

Refresh Cycle

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	ns	

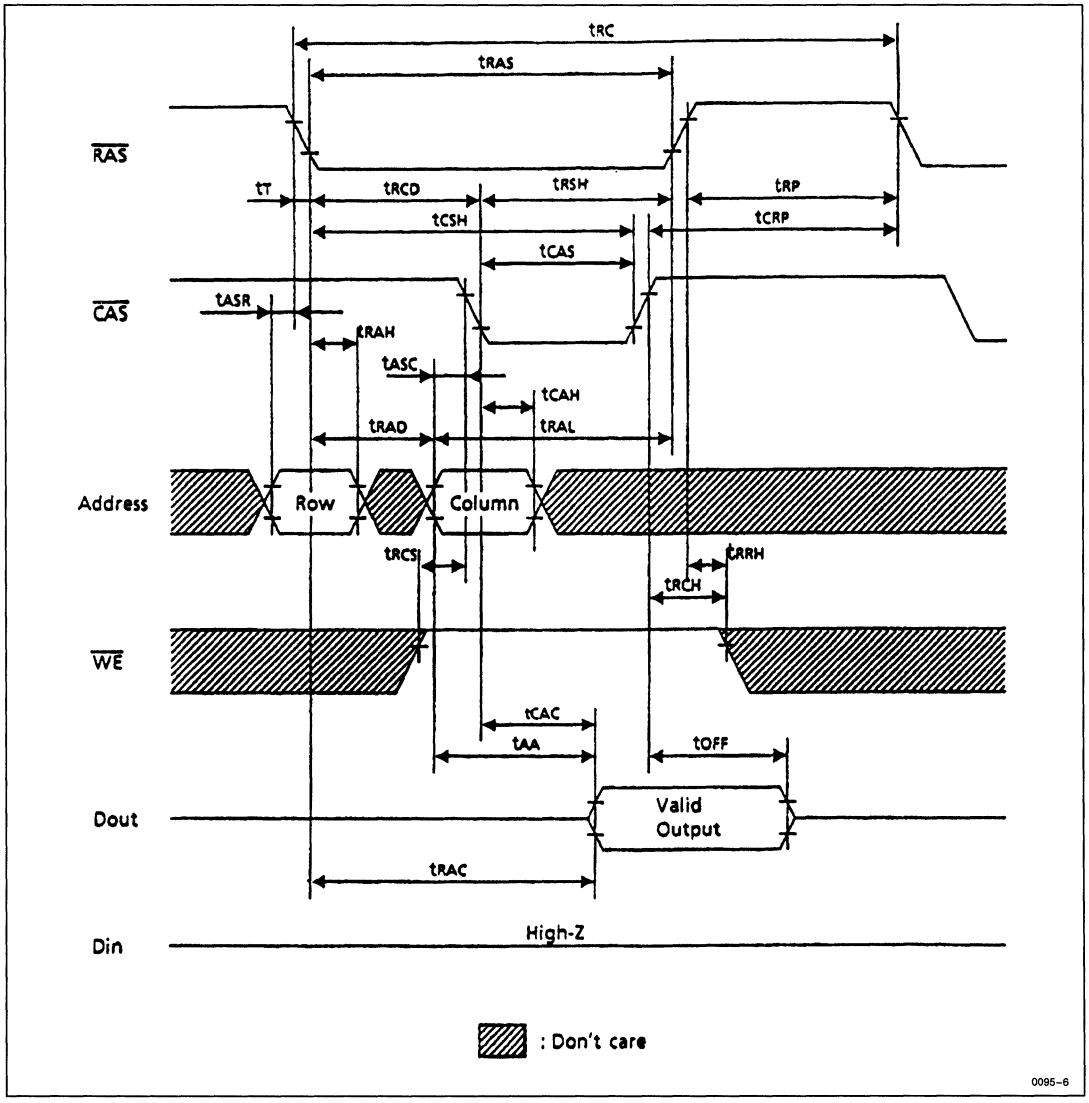
Fast Page Mode Cycle

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	15	—	20	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	—	50	—	60	ns	13
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	50	—	60	—	ns	

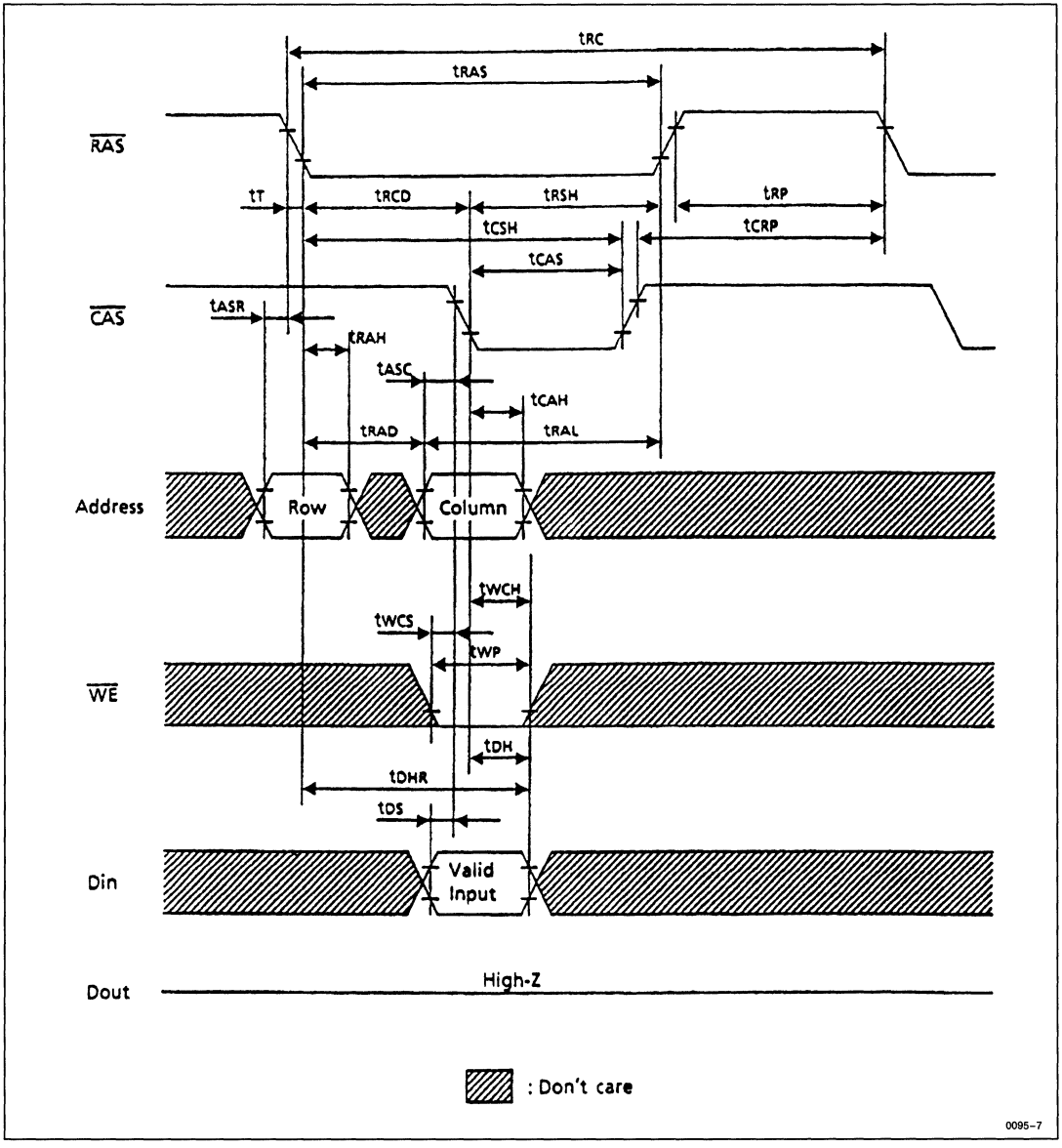
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is determined by 512 refresh cycles.

■ TIMING WAVEFORM

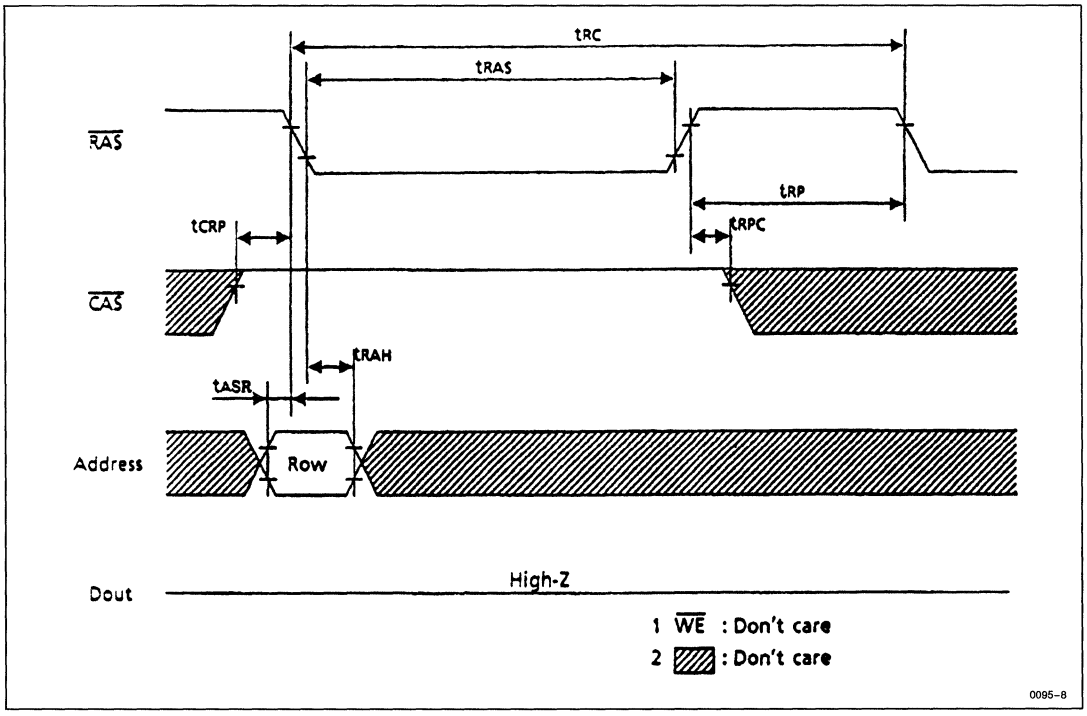
• Read Cycle



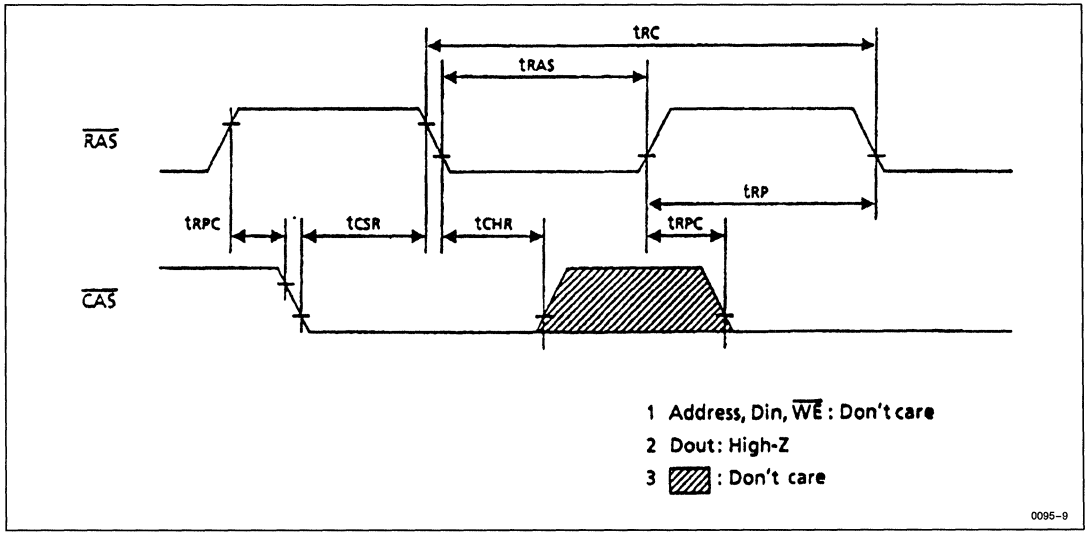
■ **Early Write Cycle**



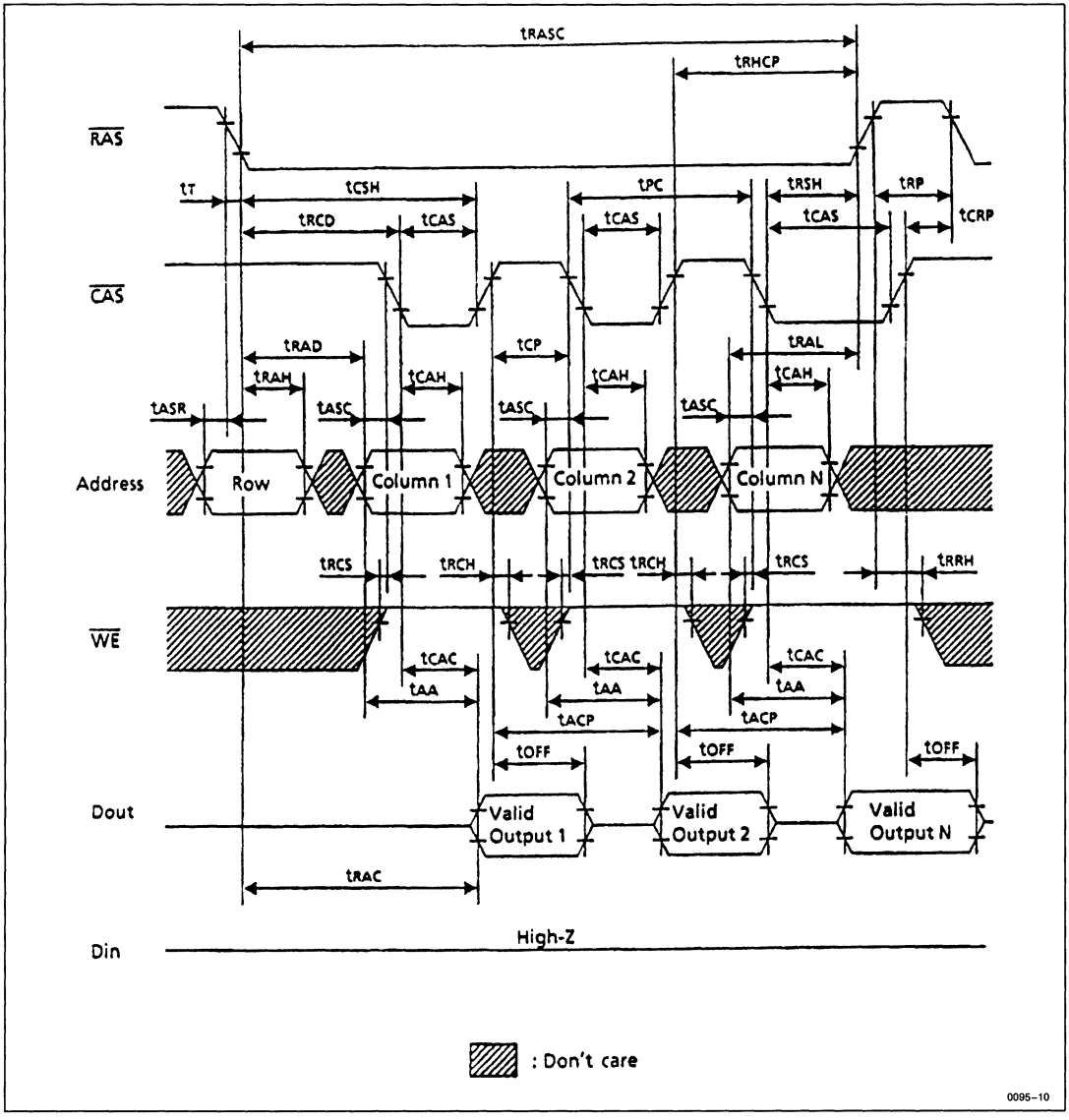
• $\overline{RAS}$ Only Refresh Cycle



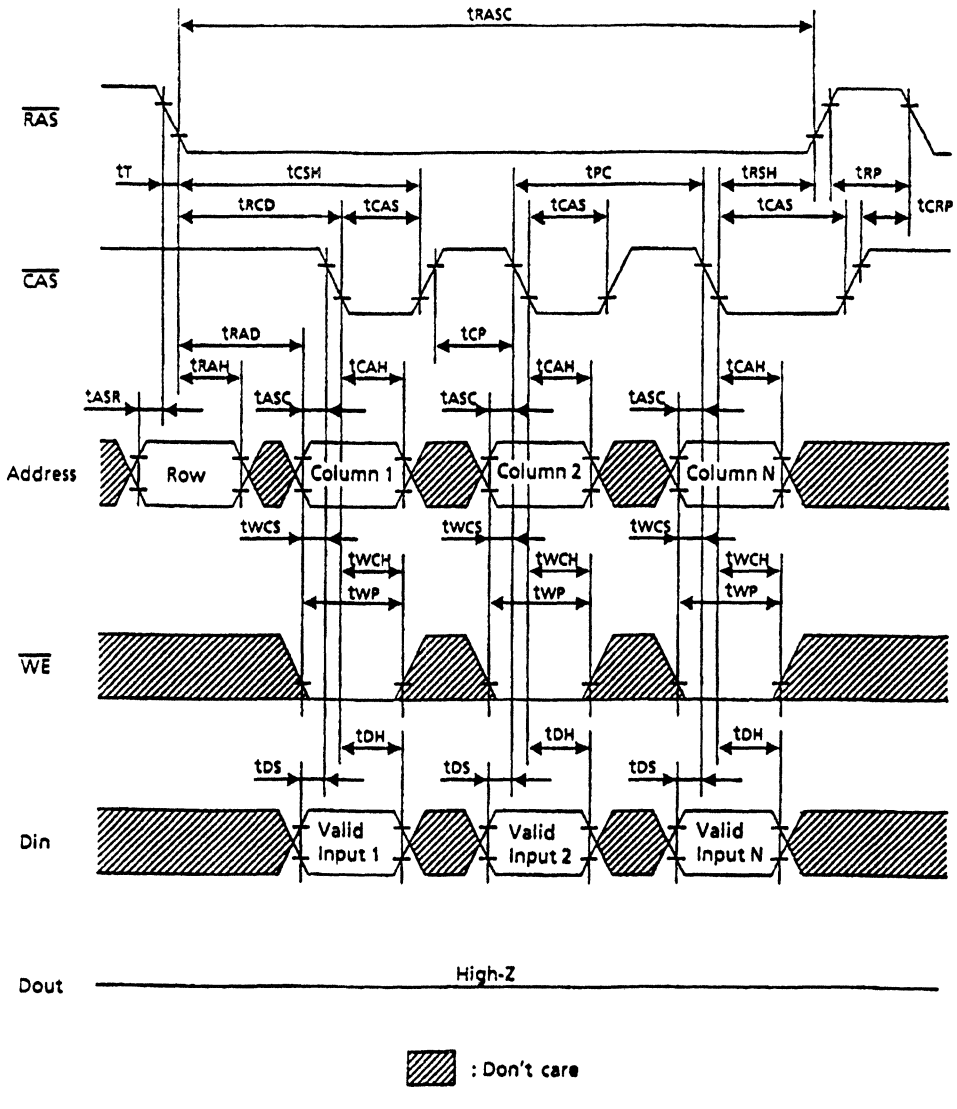
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



HB56D51232 Series

524,288-Word x 32-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56D51232SB is a 512k x 32 dynamic RAM module, mounted 16 pieces of 1 Mbit DRAM (HM514256JP) sealed in SOJ package. An outline of the HB56D51232SB is 72-pin single in-line package. Therefore, the HB56D51232SB makes high density mounting possible without surface mount technology. The HB56D51232SB provides common data inputs and outputs.

Decoupling capacitors are mounted beneath each SOJ but only on the one side of its module board.

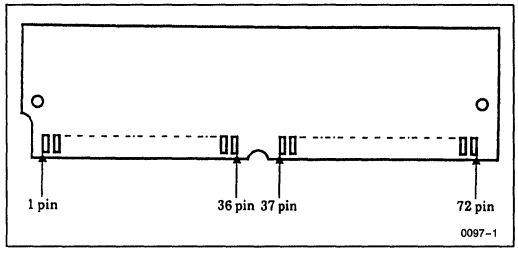
■ FEATURES

- 72-pin Single In-line Package
  - Lead Pitch 1.27mm
- Single 5V (±5%) Supply
- High Speed
  - Access Time ..... 60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode ..... 3.95W/3.57W/2.982W/2.52W/2.184W (max)
  - Standby Mode ..... 168 mW (max)
- Fast Page Capability
- 512 Refresh Cycles/8 ms
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

Part No.	Access Time	Package
HB56D51232SB-6A	60 ns	72-pin SIP Socket Type
HB56D51232SB-7A	70 ns	
HB56D51232SB-8A	80 ns	
HB56D51232SB-10A	100 ns	
HB56D51232SB-12A	120 ns	

■ PIN OUT



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	NC	37	NC	55	DQ_{11}
2	DQ_0	20	DQ_4	38	NC	56	DQ_{27}
3	DQ_{16}	21	DQ_{20}	39	V_{SS}	57	DQ_{12}
4	DQ_1	22	DQ_5	40	$\overline{CAS0}$	58	DQ_{28}
5	DQ_{17}	23	DQ_{21}	41	$\overline{CAS2}$	59	V_{CC}
6	DQ_2	24	DQ_6	42	$\overline{CAS3}$	60	DQ_{29}
7	DQ_{18}	25	DQ_{22}	43	$\overline{CAS1}$	61	DQ_{13}
8	DQ_3	26	DQ_7	44	$\overline{RAS0}$	62	DQ_{30}
9	DQ_{19}	27	DQ_{23}	45	$\overline{RAS1}$	63	DQ_{14}
10	V_{CC}	28	A_7	46	NC	64	DQ_{31}
11	NC	29	NC	47	$\overline{WE}$	65	DQ_{15}
12	A_0	30	V_{CC}	48	NC	66	NC
13	A_1	31	A_8	49	DQ_8	67	NC
14	A_2	32	NC	50	DQ_{24}	68	V_{SS}
15	A_3	33	$\overline{RAS3}$	51	DQ_9	69	PD1
16	A_4	34	$\overline{RAS2}$	52	DQ_{25}	70	PD2
17	A_5	35	NC	53	DQ_{10}	71	NC
18	A_6	36	NC	54	DQ_{26}	72	V_{SS}

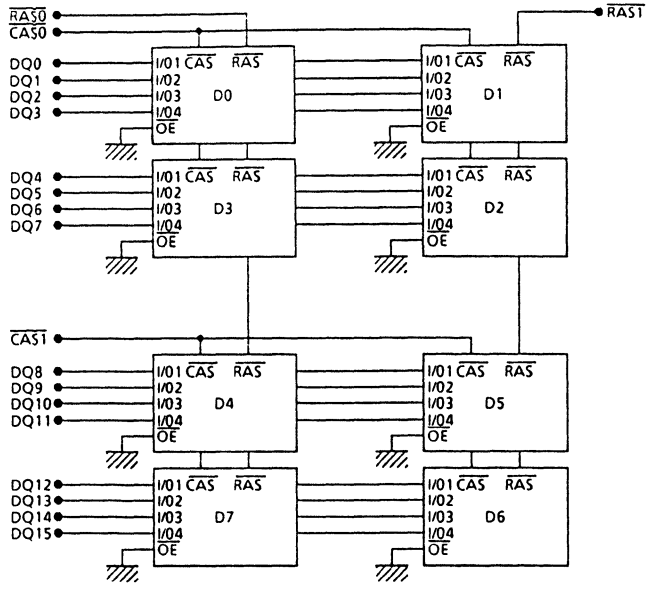
■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Input
A_0–A_8	Refresh Address Input
DQ_0–DQ_{31}	Data-in/Data-out
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$–$\overline{RAS3}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power Supply (+ 5V)
V_{SS}	Ground
NC	No Connection

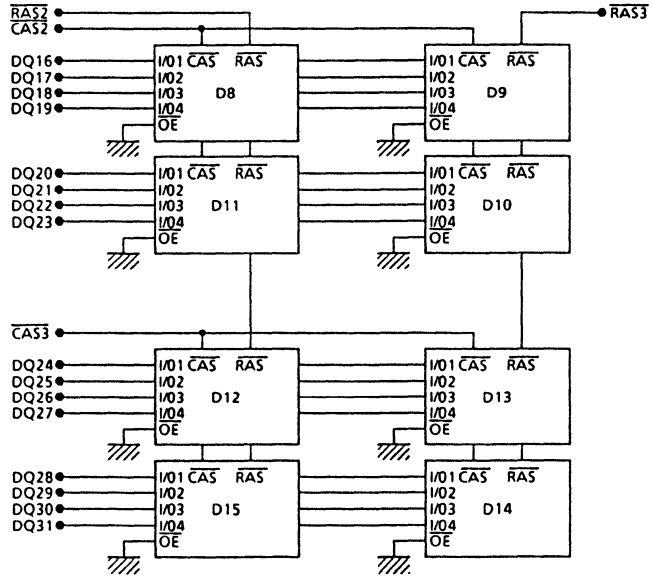
■ PRESENCE DETECT PINOUT

Pin No.	Pin Name	HB56D51232SB				
		60 ns	70 ns	80 ns	100 ns	120 ns
69	PD1	NC	V_{SS}	NC	V_{SS}	NC
70	PD2	NC	NC	V_{SS}	V_{SS}	NC

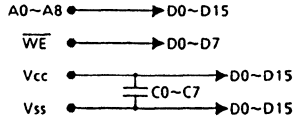
■ BLOCK DIAGRAM



0097-2



0097-3

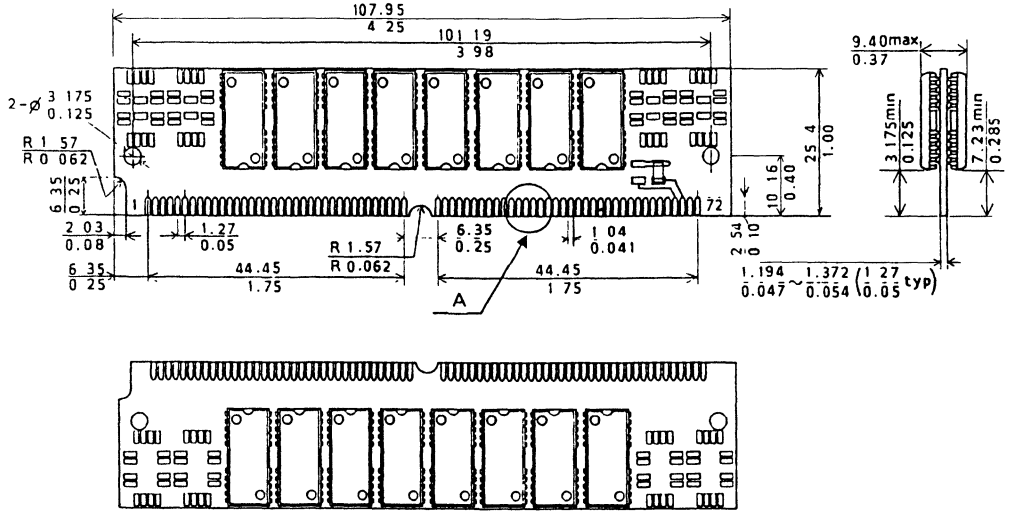


* D0~D15 : HM514256

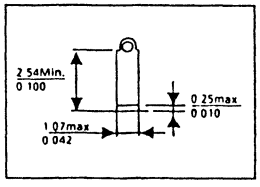
0097-4

■ PACKAGE OUTLINE

Unit: mm/inch



Detail A



0097-5

Note: Contact finish 2.2 μm (86.6 μinch) Solder over 2.0 μm (78.7 μinch) Ni.

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input)	V_{in}	−1.0 to +7.0	V
	(Output)	V_{out}	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	16	W
Operating Temperature		T_{opr}	0 to +70	°C
Storage Temperature		T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Test Condition	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	760	—	680	—	568	—	480	—	416	mA	t_{RC} = min	1, 2
Standby Current	I_{CC2}	—	32	—	32	—	32	—	32	—	32	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	16	—	16	—	16	—	16	—	16	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	760	—	680	—	568	—	480	—	416	mA	t_{RC} = min	2
Standby Current	I_{CC5}	—	80	—	80	—	80	—	80	—	80	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	760	—	680	—	568	—	480	—	416	mA	t_{RC} = min	
Page Mode Current	I_{CC7}	—	760	—	680	—	480	—	480	—	416	mA	t_{PC} = min	1, 3
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V_{IN} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V_{OUT} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• Capacitance (T_A = 25°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Typ	Max	Unit	Unit
Input Capacitance (Address)	C_{I1}	—	121	pF	1
Input Capacitance ($\overline{WE}$)	C_{I2}	—	137	pF	1
Input Capacitance ($\overline{RAS}$)	C_{I3}	—	48	pF	1
Input Capacitance ($\overline{CAS}$)	C_{I4}	—	48	pF	1
Output Capacitance (DQ_0–DQ_{31})	$C_{I/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)[1, 12]

Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	125	—	140	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	55	—	60	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	20	—	25	—	ns	

Read, Write and Refresh Cycle (Common Parameters) (continued)

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ns	15

• Read Cycle

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	55	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	55	—	ns	
Output Buffer Turn-Off Time	t_{OFF}	—	20	—	20	—	20	—	25	—	30	ns	6

• Write Cycle

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	20	—	25	—	ns	11

• Refresh Cycle

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	ns	

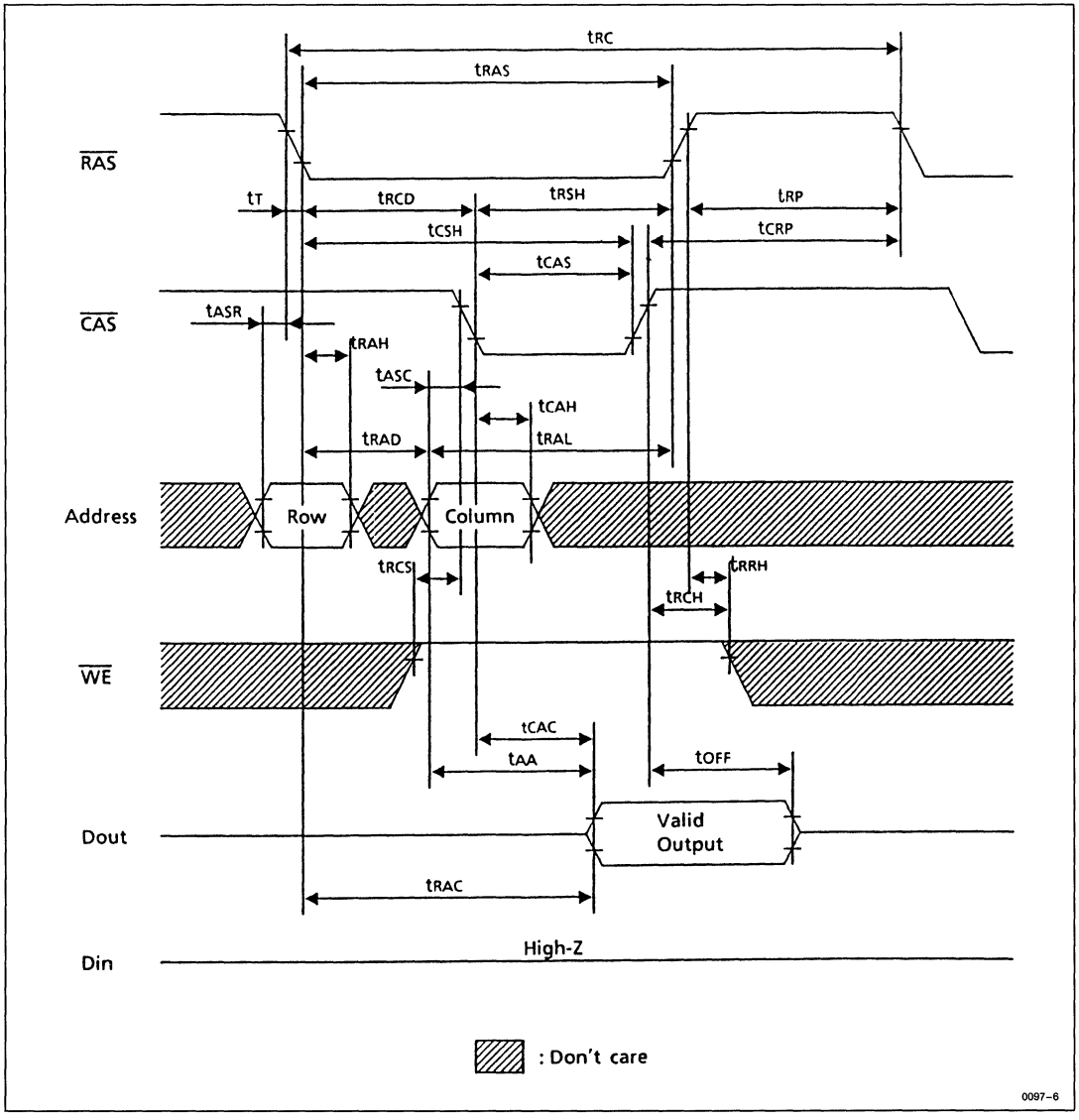
• Fast Page Mode Cycle

Parameter	Symbol	-6A		-7A		-8A		-10A		-12A		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	15	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	—	50	—	60	ns	13
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	50	—	60	—	ns	

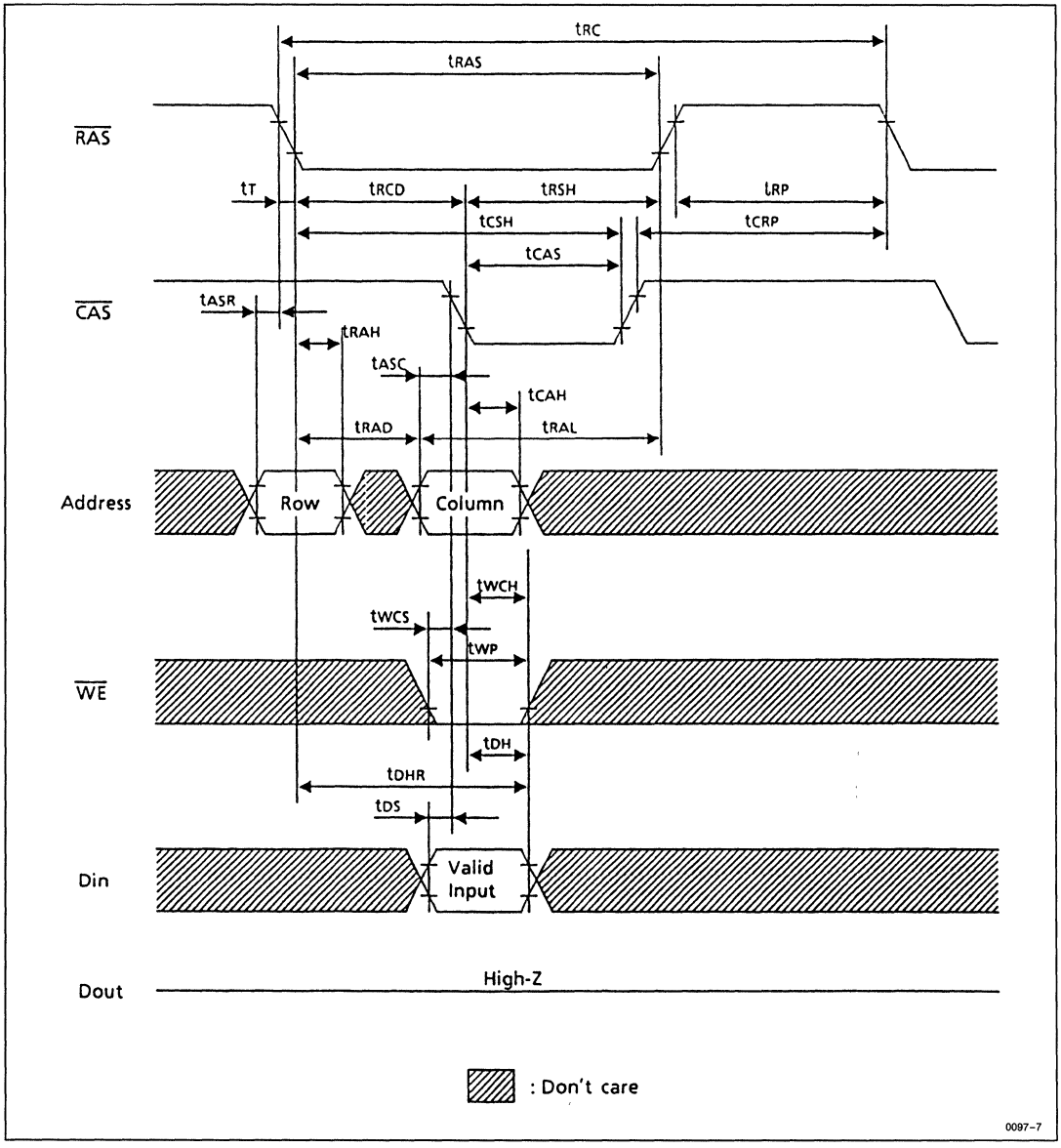
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is determined by 512 refresh cycles.

■ TIMING WAVEFORMS

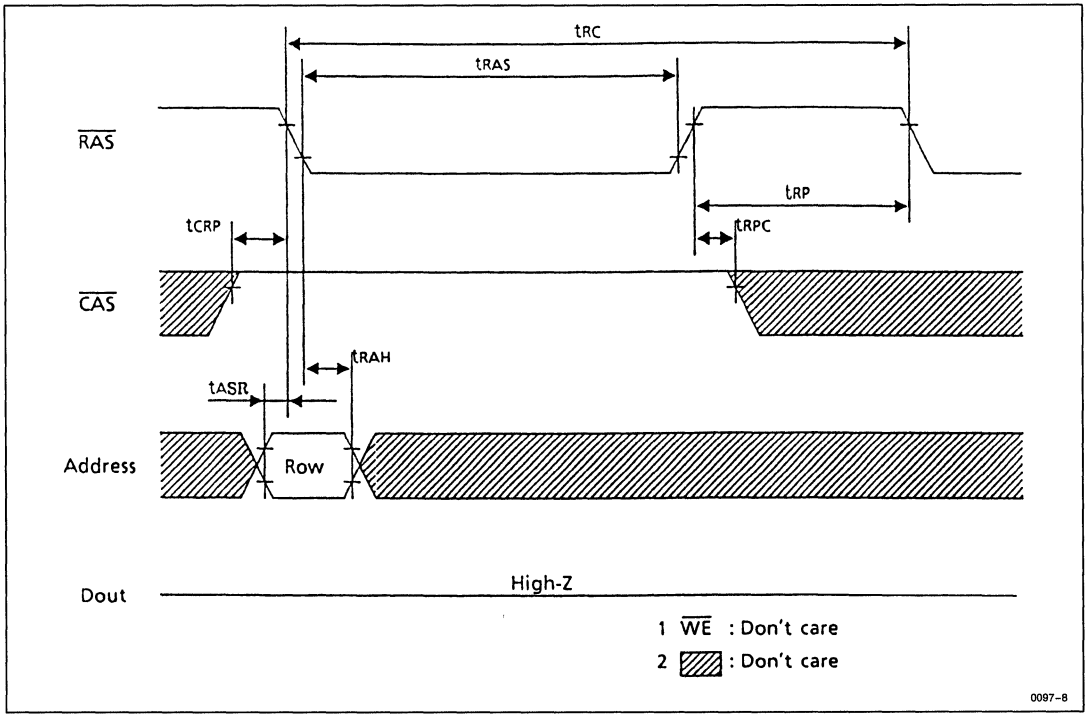
• Read Cycle



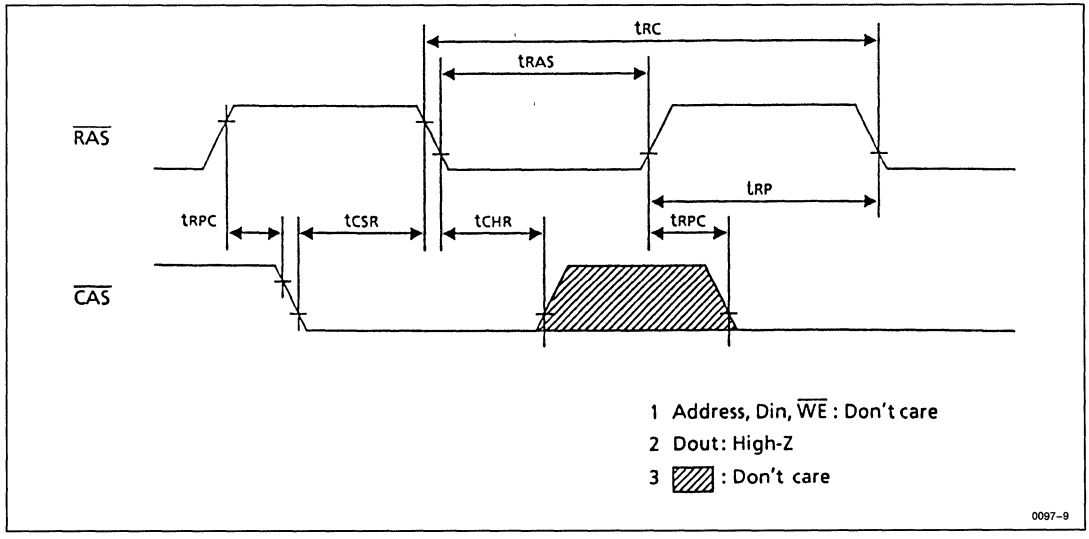
• **Early Write Cycle**



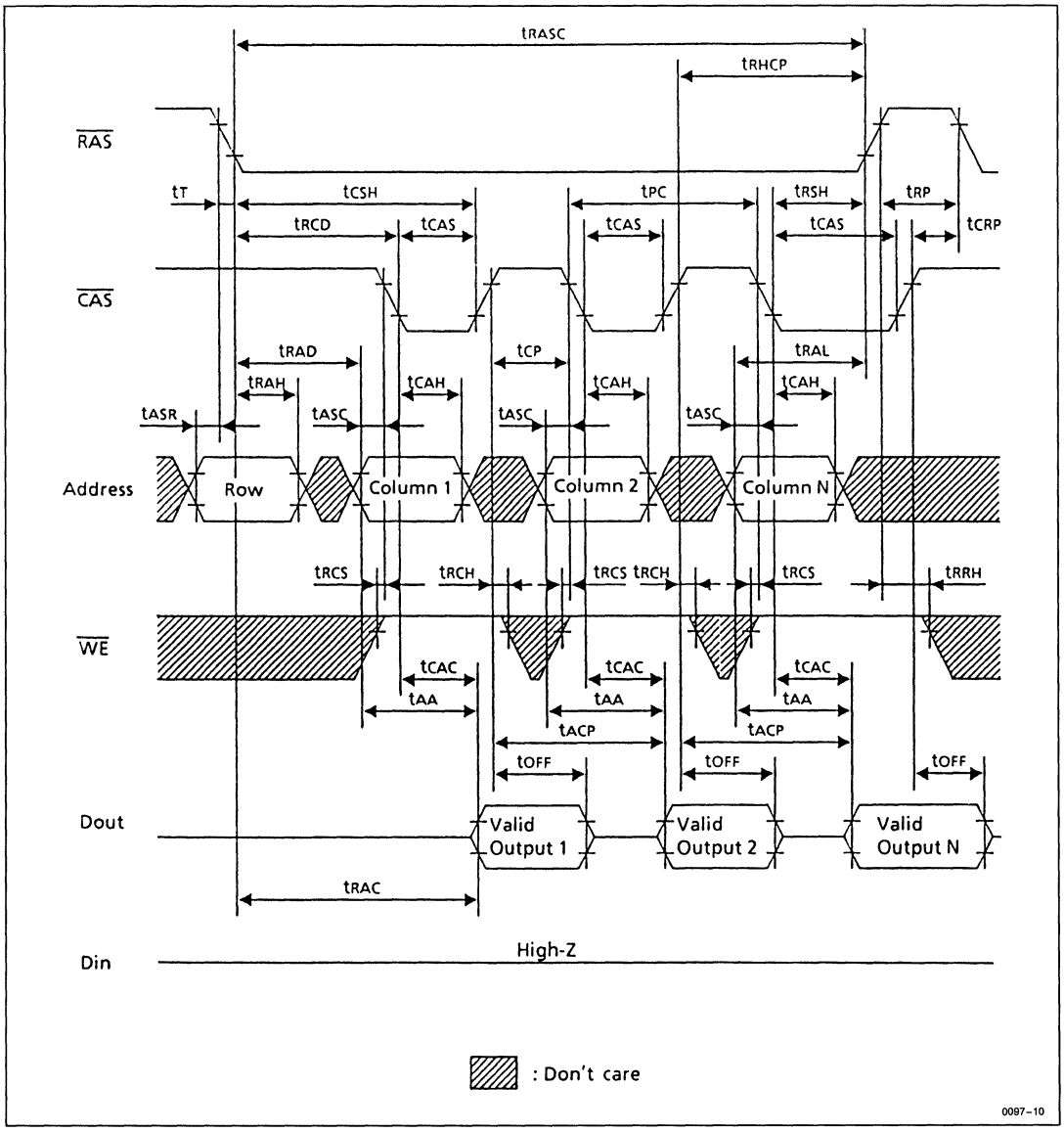
• $\overline{RAS}$ Only Refresh Cycle



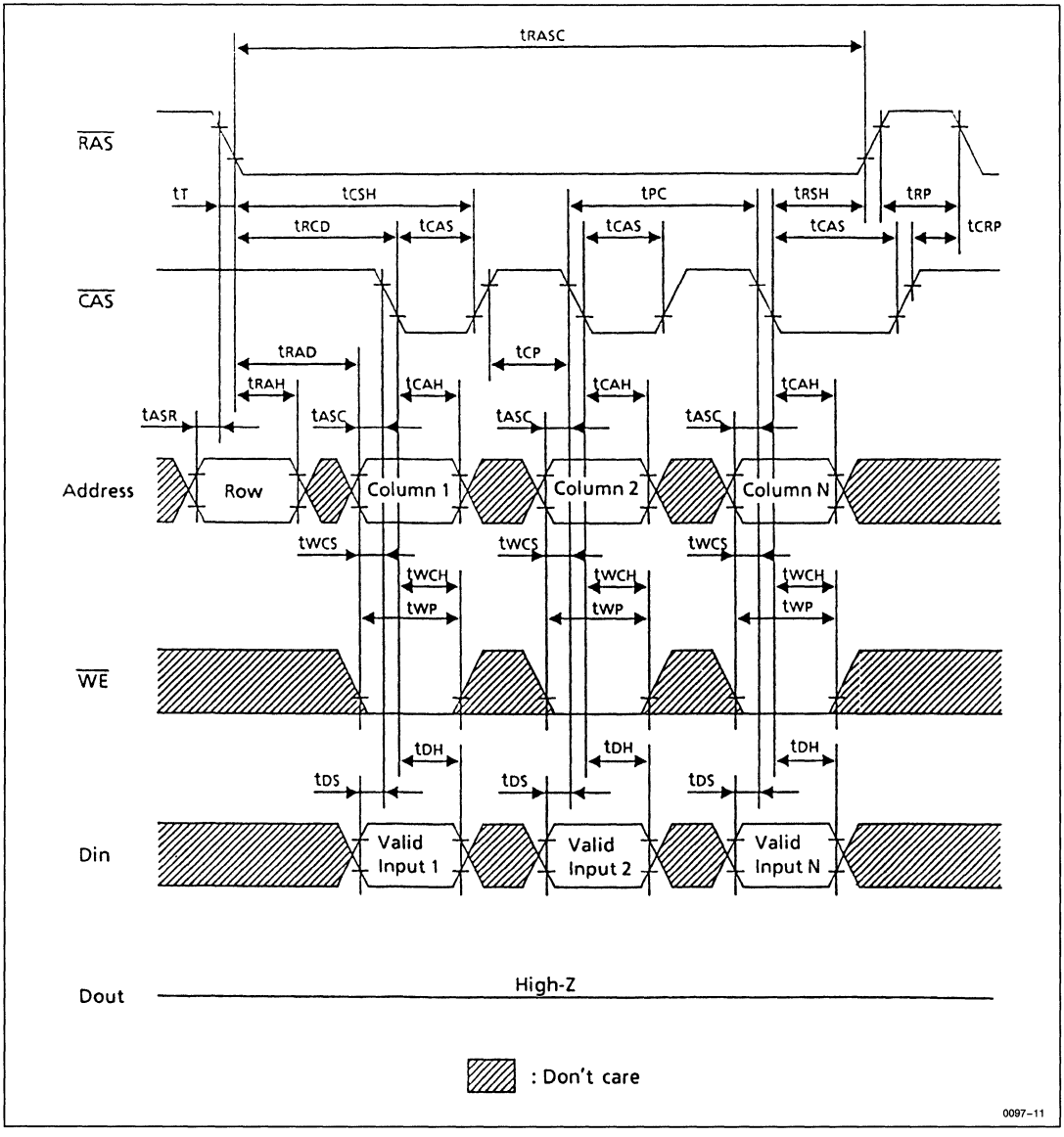
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



HB56D132 Series

1,048,576-Word x 32-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56D132BR/SBR is a 1M x 32 dynamic RAM module, mounted 8 pieces of 4 Mbit DRAM (HM514400JP/AJ) sealed in SOJ package. An outline of the HB56D132BR/SBR is 72-pin single in-line package. Therefore, the HB56D132BR/SBR makes high density mounting possible without surface mount technology. The HB56D132BR/SBR provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ.

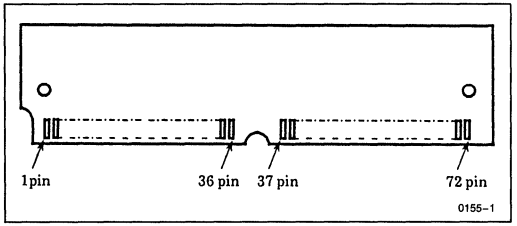
■ FEATURES

- 72-pin Single In-line Package
  Lead Pitch 1.27mm
- Single 5V (±5%) Supply
- High Speed
  Access Time ..... 60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  Active Mode ..... 4.62W/4.40W/3.96W/3.52W (max)
  Standby Mode ..... 88 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycle ..... (16 ms)
- 2 Variations of Refresh
  $\overline{RAS}$ Only Refresh
  $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

Part No.	Access Time	Package	Contact Pad
HB56D132BR-6A	60 ns	72-pin SIP Socket Type	Gold
HB56D132BR-7A	70 ns		
HB56D132BR-8A	80 ns		
HB56D132BR-10A	100 ns		
HB56D132BR-8	80 ns		
HB56D132BR-10	100 ns		
HB56D132SBR-6A	60 ns	72-pin SIP Socket Type	Solder
HB56D132SBR-7A	70 ns		
HB56D132SBR-8A	80 ns		
HB56D132SBR-10A	100 ns		
HB56D132SBR-8	80 ns		
HB56D132SBR-10	100 ns		

■ PIN OUT

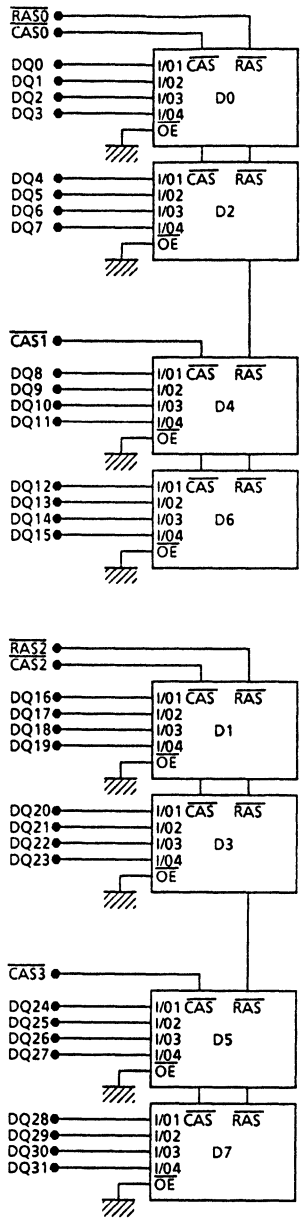


Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	NC	37	NC	55	DQ_{11}
2	DQ_0	20	DQ_4	38	NC	56	DQ_{27}
3	DQ_{16}	21	DQ_{20}	39	V_{SS}	57	DQ_{12}
4	DQ_1	22	DQ_5	40	$\overline{CAS0}$	58	DQ_{28}
5	DQ_{17}	23	DQ_{21}	41	$\overline{CAS2}$	59	V_{CC}
6	DQ_2	24	DQ_6	42	$\overline{CAS3}$	60	DQ_{29}
7	DQ_{18}	25	DQ_{22}	43	$\overline{CAS1}$	61	DQ_{13}
8	DQ_3	26	DQ_7	44	$\overline{RAS0}$	62	DQ_{30}
9	DQ_{19}	27	DQ_{23}	45	NC	63	DQ_{14}
10	V_{CC}	28	A_7	46	NC	64	DQ_{31}
11	NC	29	NC	47	$\overline{WE}$	65	DQ_{15}
12	A_0	30	V_{CC}	48	NC	66	NC
13	A_1	31	A_8	49	DQ_8	67	V_{SS}
14	A_2	32	A_9	50	DQ_{24}	68	V_{SS}
15	A_3	33	NC	51	DQ_9	69	NC
16	A_4	34	$\overline{RAS2}$	52	DQ_{25}	70	NC
17	A_5	35	NC	53	DQ_{10}	71	NC
18	A_6	36	NC	54	DQ_{26}	72	V_{SS}

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_9	Refresh Address Input
DQ_0–DQ_{31}	Data-in/Data-out
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$–$\overline{RAS2}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power Supply (+ 5V)
V_{SS}	Ground
PD1–PD4	Presence Detect Pin
NC	No Connection

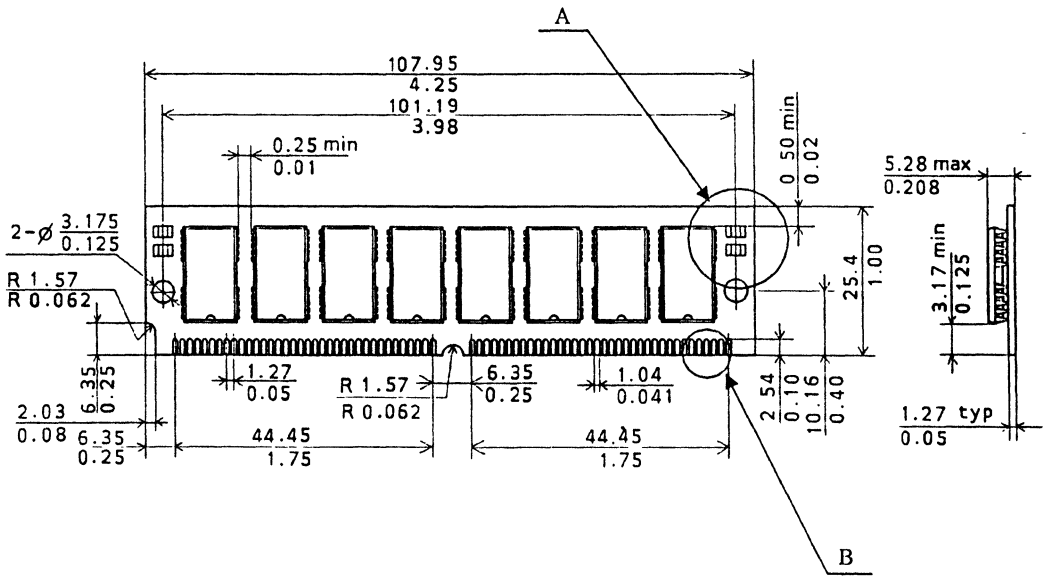
■ BLOCK DIAGRAM



* D0 – D7 : HM514400JP/AJ

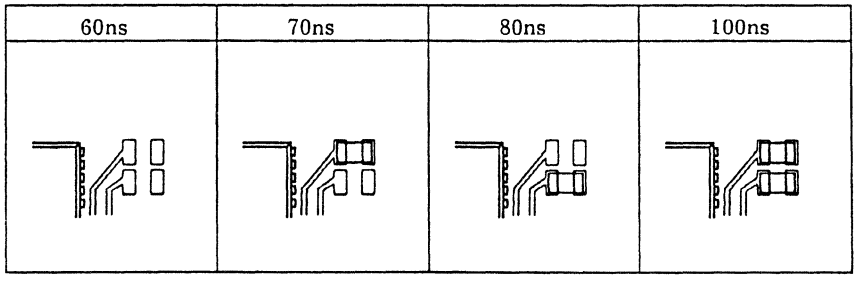
■ PHYSICAL OUTLINE

Unit: mm / inch

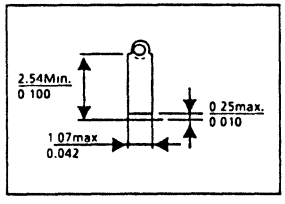


0155-3

Detail A



Detail B



Note: Following the specification of the contact pads.

Part No.	Contact Pad
HB56D132BR-XX	Gold
HB56D132SBR-XX	Solder

0155-4

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input)	V_{in}	−1.0 to +7.0	V
	(Output)	V_{out}	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	8	W
Operating Temperature		T_{opr}	0 to +70	°C
Storage Temperature		T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)

Parameter	Symbol	HB56D132BR/SBR												Unit	Test Conditions	Note
		-6A		-7A		-8A		-10A		-8		-10				
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	880	—	800	—	720	—	640	—	720	—	640	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	16	—	16	—	16	—	16	—	16	—	16	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	8	—	8	—	8	—	8	—	8	—	8	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2V$ D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	880	—	800	—	720	—	640	—	720	—	640	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	40	—	40	—	40	—	40	—	40	—	40	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	880	—	800	—	720	—	640	—	720	—	640	mA	t_{RC} = Min	
Page Mode Current	I_{CC7}	—	880	—	800	—	720	—	640	—	720	—	640	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	68	pF	1
Input Capacitance ($\overline{WE}$)	C_{I2}	—	76	pF	1
Input Capacitance ($\overline{RAS}$)	C_{I3}	—	43	pF	1
Input Capacitance ($\overline{CAS}$)	C_{I4}	—	29	pF	1
Output Capacitance (DQ_0–DQ_{31})	$C_{I/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)[1, 12]

Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56D132BR/SBR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	180	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	70	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10000	20	10000	20	10000	25	10000	25	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	15	—	12	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	20	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	20	60	25	75	22	55	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	20	55	17	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	20	—	25	—	25	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	5	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	—	16	—	16	—	16	ms	15

Read Cycle

Parameter	Symbol	HB56D132BR/SBR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	—	25	—	25	—	25	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	40	—	45	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	0	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	55	—	40	—	45	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	15	0	20	0	20	0	25	0	20	0	25	ns	6

Write Cycle

Parameter	Symbol	HB56D132BR/SBR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	15	—	20	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	10	—	20	—	15	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DD}	15	—	15	—	15	—	20	—	15	—	20	—	ns	11

Refresh Cycle

Parameter	Symbol	HB56D132BR/SBR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	10	—	20	—	20	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	10	—	ns	

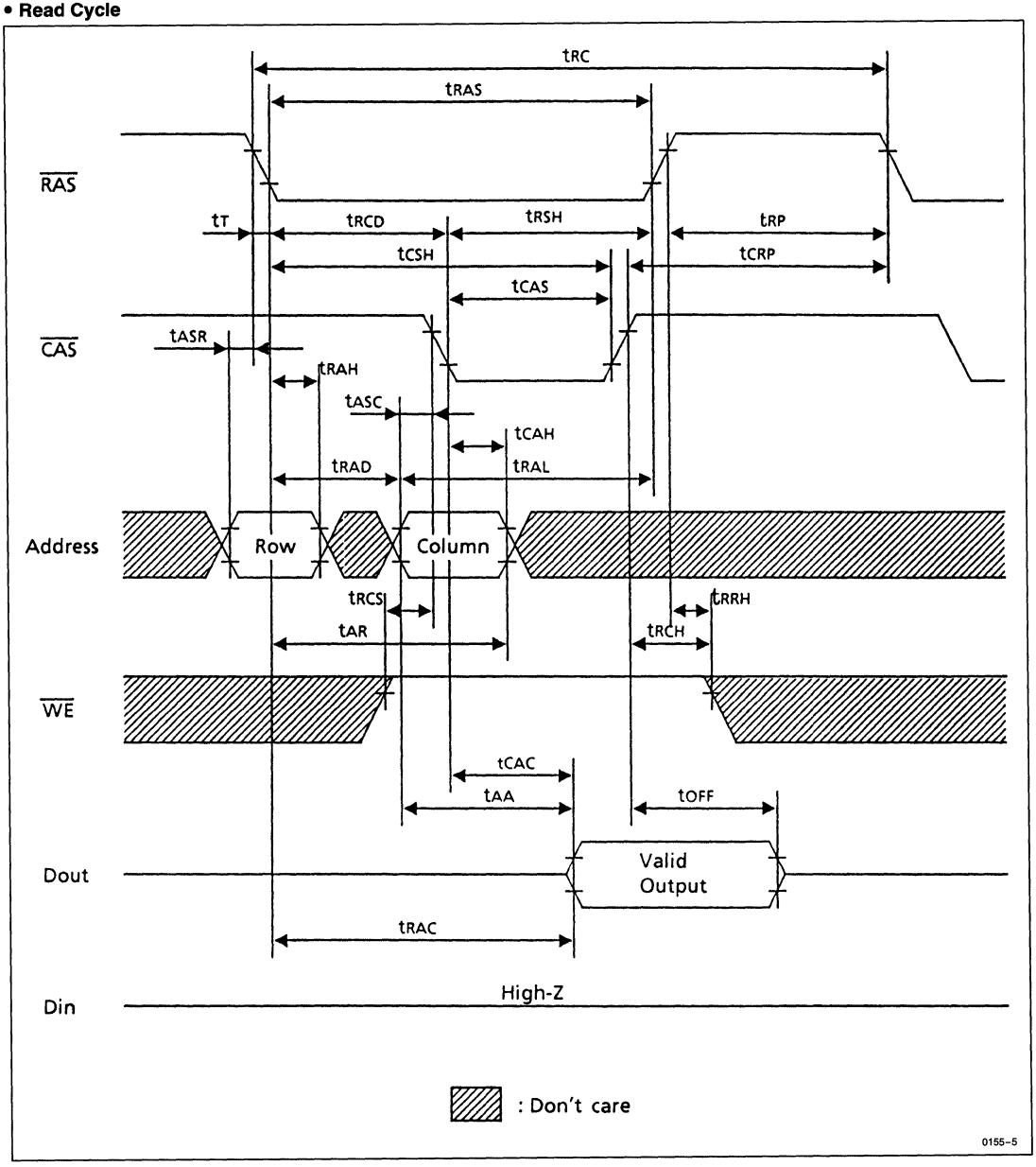
Fast Page Mode Cycle

Parameter	Symbol	HB56D132BR/SBR												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	55	—	55	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	—	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	35	—	40	—	45	—	50	—	50	—	50	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	45	—	50	—	50	—	50	—	ns	

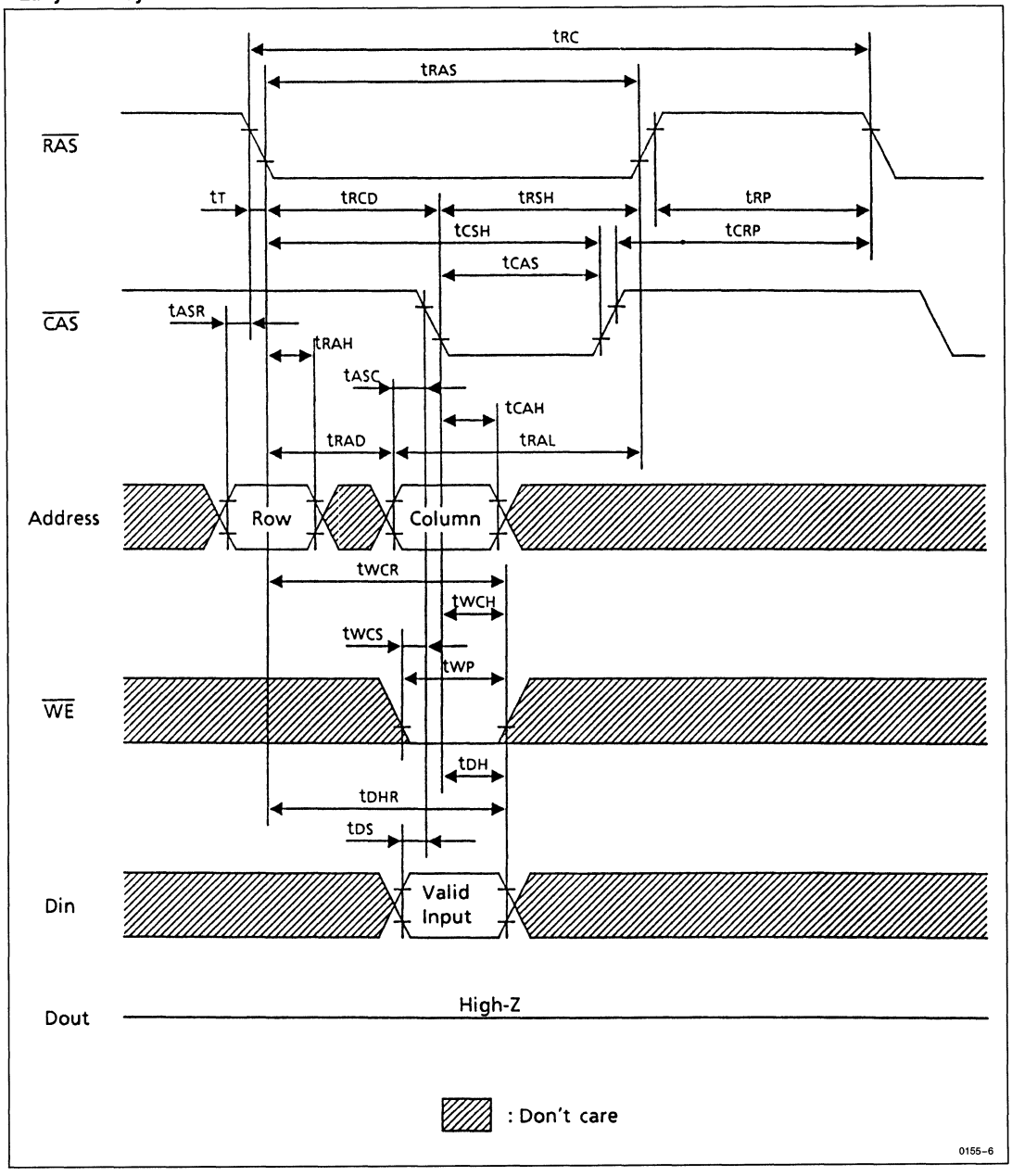
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is determined by 1,024 refresh cycles.

■ TIMING WAVEFORMS

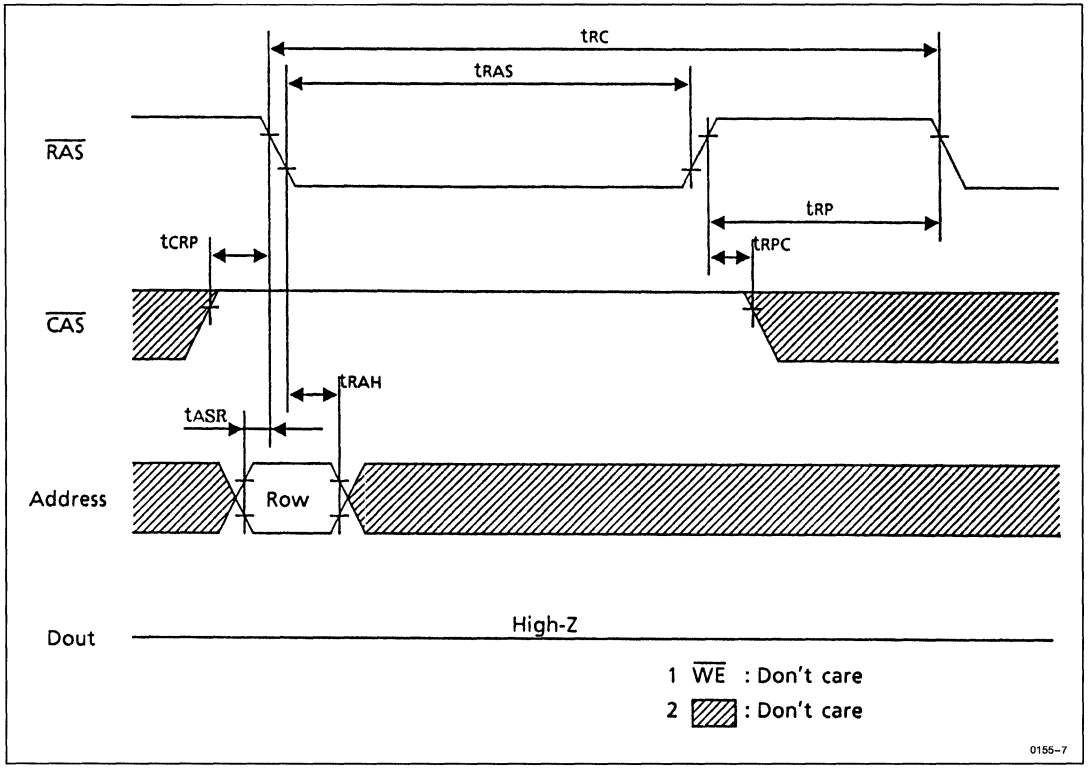
• Read Cycle



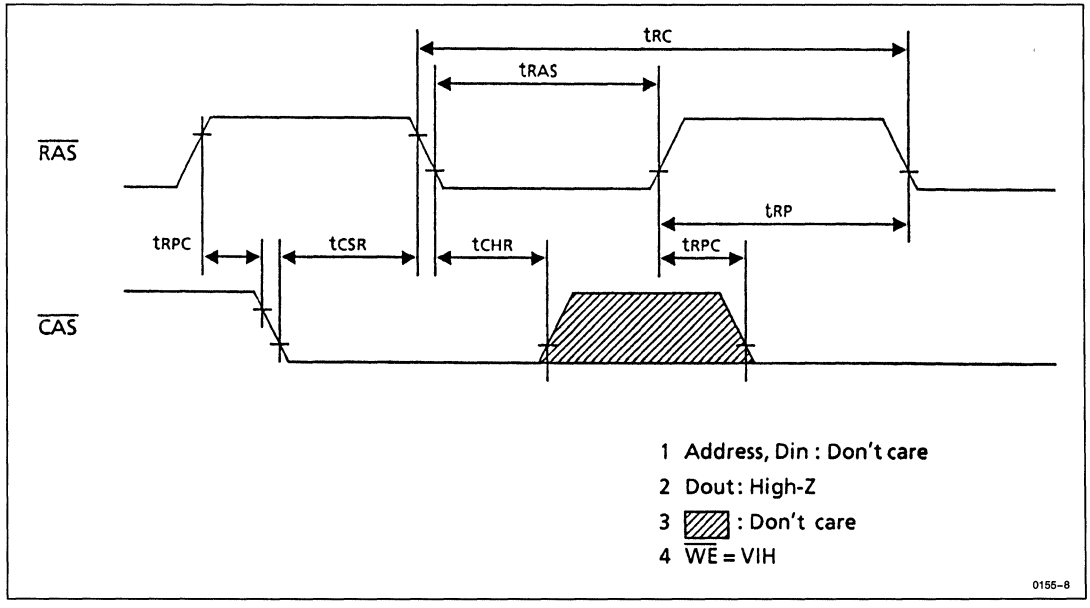
• **Early Write Cycle**



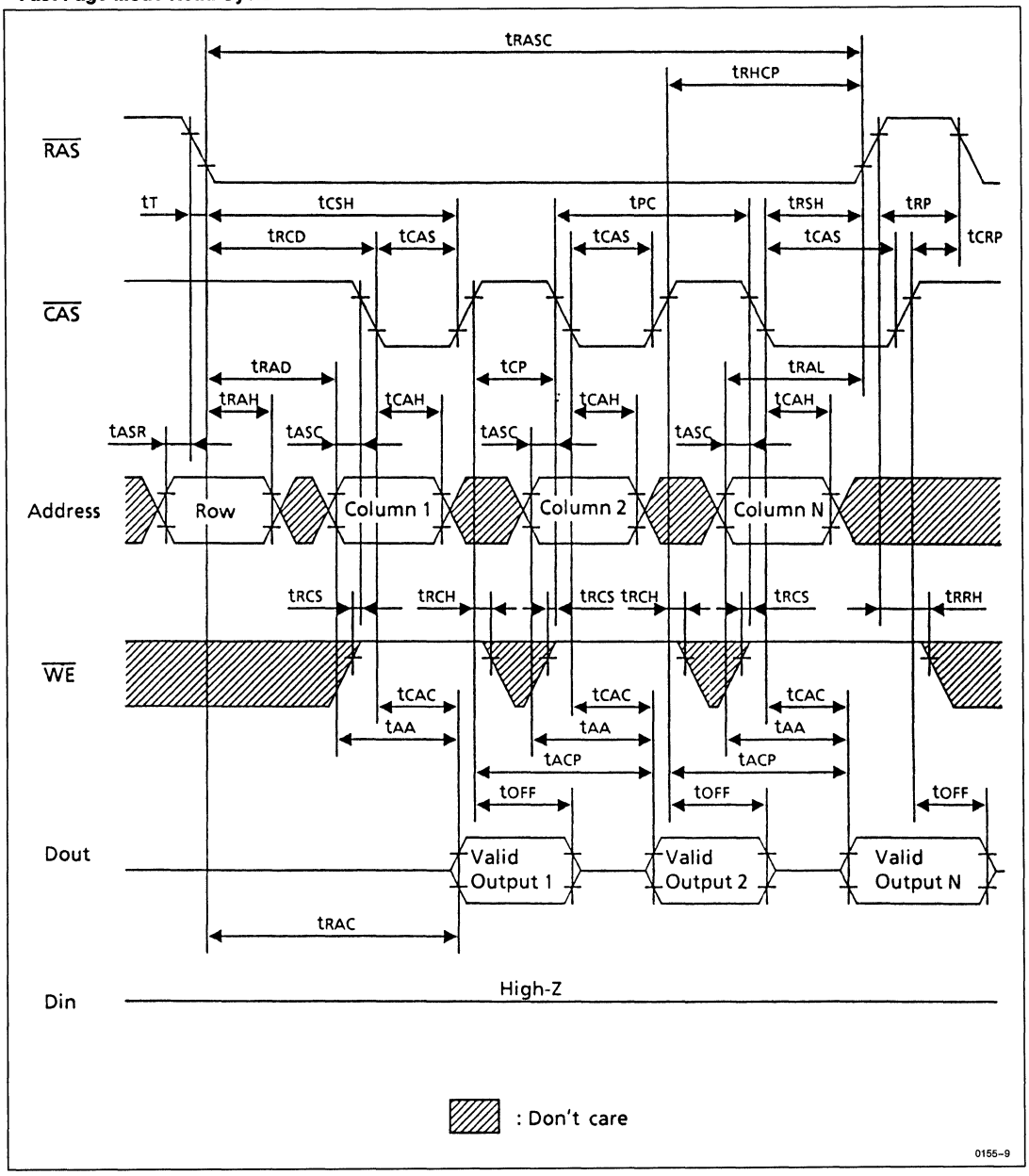
• $\overline{RAS}$ Only Refresh Cycle



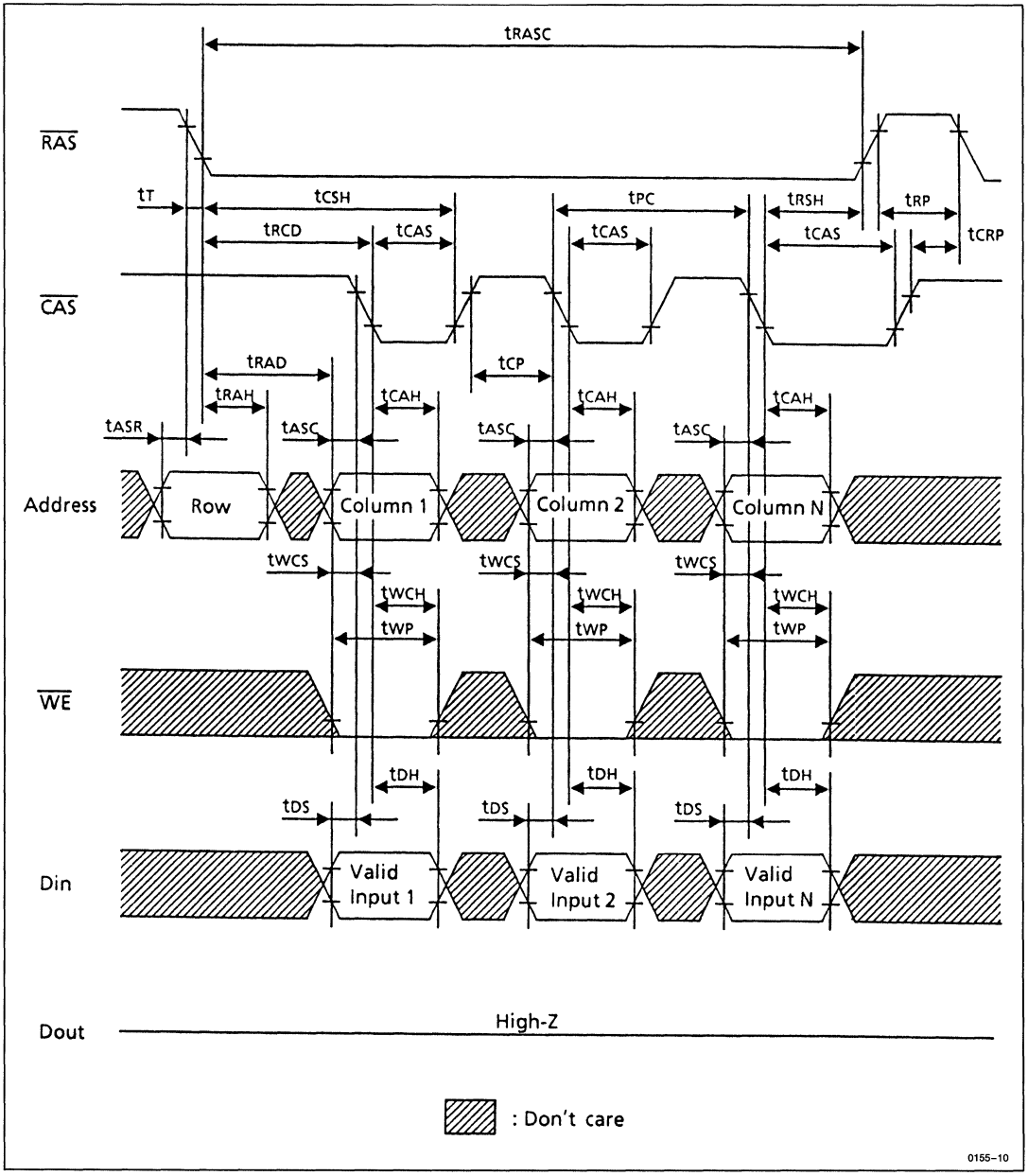
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



HB56D232B Series

2,097,152-Word x 32-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56D232B is a 2M x 32 dynamic RAM module, mounted 16 pieces of 4Mbit DRAM (HM514400JP) sealed in SOJ package. An outline of the HB56D232B is 72-pin single in-line package. Therefore, the HB56D232B makes high density mounting possible without surface mount technology. The HB56D232B provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ but only on the one side of its module board.

■ FEATURES

- 72-pin Single In-line Package
  - Lead Pitch 1.27mm
- Single 5V (±5%) Supply
- High Speed
  - Access Time ..... 80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode..... 3.99W/3.57W/3.15W (max)
  - Standby Mode ..... 168 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles ..... (16 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

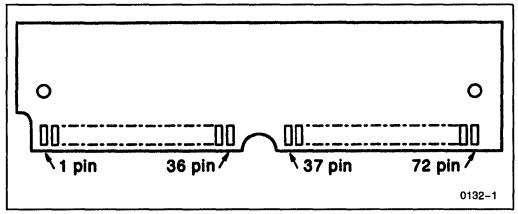
■ ORDERING INFORMATION

Part No.	Access Time	Package
HB56D232B-8	80 ns	72-pin SIP Socket Type
HB56D232B-10	100 ns	
HB56D232B-12	120 ns	

■ PRESENCE DETECT PINOUT

Pin No.	Pin Name	HB56D132BR		
		80 ns	100 ns	120 ns
67	PD_1	V_{SS}	V_{SS}	V_{SS}
68	PD_2	V_{SS}	V_{SS}	V_{SS}
69	PD_3	NC	V_{SS}	NC
70	PD_4	V_{SS}	V_{SS}	NC

■ PIN OUT

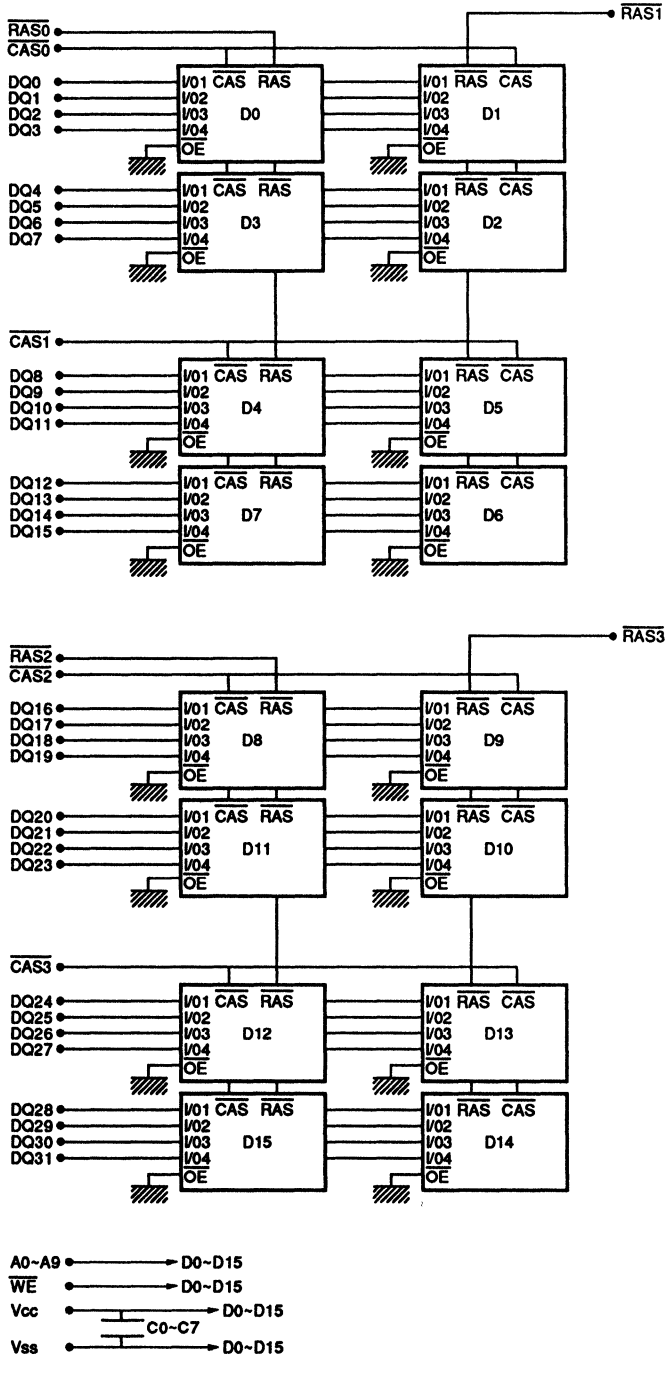


Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	NC	37	NC	55	DQ_{11}
2	DQ_0	20	DQ_4	38	NC	56	DQ_{27}
3	DQ_{16}	21	DQ_{20}	39	V_{SS}	57	DQ_{12}
4	DQ_1	22	DQ_5	40	$\overline{CAS0}$	58	DQ_{28}
5	DQ_{17}	23	DQ_{21}	41	$\overline{CAS2}$	59	V_{CC}
6	DQ_2	24	DQ_6	42	$\overline{CAS3}$	60	DQ_{29}
7	DQ_{18}	25	DQ_{22}	43	$\overline{CAS1}$	61	DQ_{13}
8	DQ_3	26	DQ_7	44	$\overline{RAS0}$	62	DQ_{30}
9	DQ_{19}	27	DQ_{23}	45	$\overline{RAS1}$	63	DQ_{14}
10	V_{CC}	28	A_7	46	NC	64	DQ_{31}
11	NC	29	NC	47	$\overline{WE}$	65	DQ_{15}
12	A_0	30	V_{CC}	48	NC	66	NC
13	A_1	31	A_8	49	DQ_8	67	PD_1
14	A_2	32	A_9	50	DQ_{24}	68	PD_2
15	A_3	33	$\overline{RAS3}$	51	DQ_9	69	PD_3
16	A_4	34	$\overline{RAS2}$	52	DQ_{25}	70	PD_4
17	A_5	35	NC	53	DQ_{10}	71	NC
18	A_6	36	NC	54	DQ_{26}	72	V_{SS}

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_9	Refresh Address Input
DQ_0–DQ_{31}	Data-in/Data-out
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$–$\overline{RAS3}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power Supply (+ 5V)
V_{SS}	Ground
PD_1–PD_4	Presence Detect Pin
NC	Non-Connection

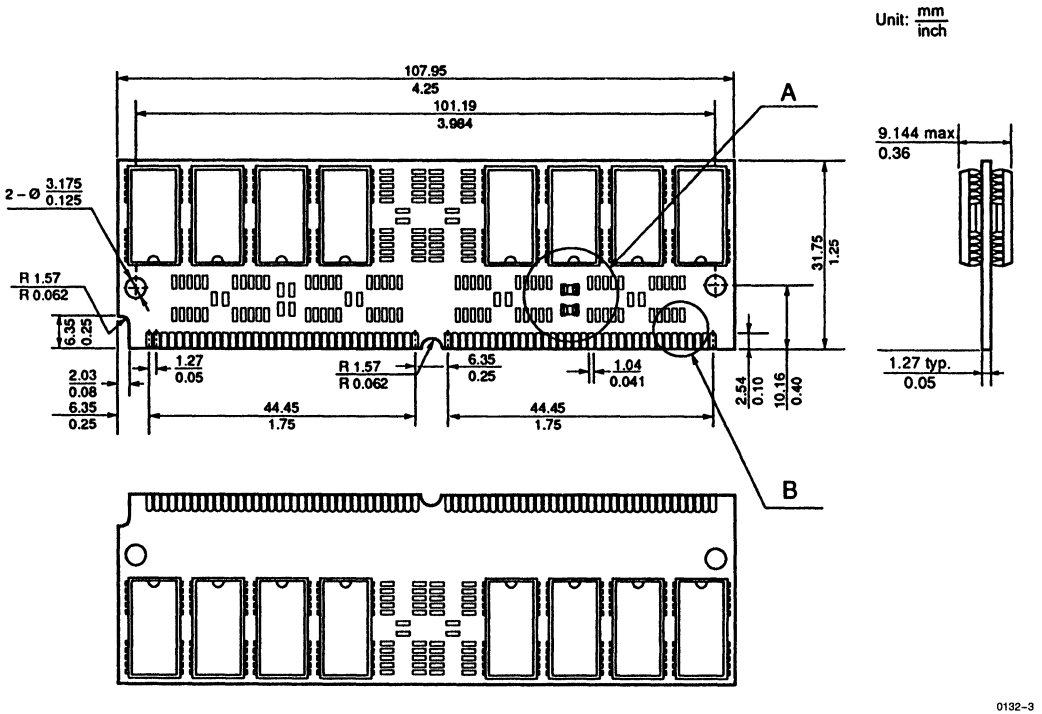
■ BLOCK DIAGRAM

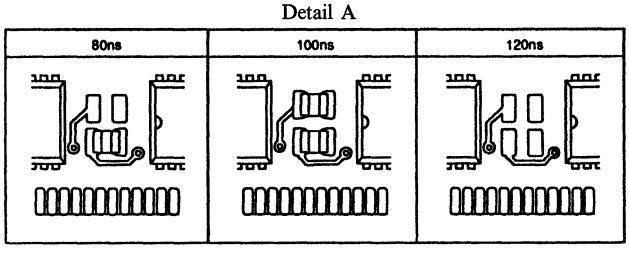


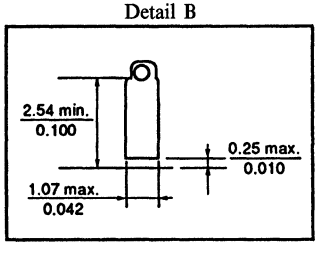
* D0~D15 : HM514400JP

0132-2

■ PHYSICAL OUTLINE







Note: The plating of the contact finger is gold.

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input)	V_{in}	− 1.0 to + 7.0	V
	(Output)	V_{out}	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	8	W
Operating Temperature		T_{opr}	0 to + 70	°C
Storage Temperature		T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)

Parameter	Symbol	HB56D232B-8		HB56D232B-10		HB56D232B-12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	760	—	680	—	600	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	32	—	32	—	32	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	16	—	16	—	16	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	760	—	680	—	600	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	80	—	80	—	80	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	760	—	680	—	600	mA	t_{RC} = Min	
Page Mode Current	I_{CC7}	—	760	—	680	—	600	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	121	pF	1
Input Capacitance ($\overline{WE}$)	C_{I2}	—	137	pF	1
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I3}	—	48	pF	1
Output Capacitance (DQ_0–DQ_{31})	$C_{I/O}$	—	29	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0°C to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)[1, 12]

Read, Write, and Refresh Cycles (Common Parameters)

Parameter	Symbol	HB56D232B-8		HB56D232B-10		HB56D232B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	150	—	180	—	210	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	15

Read Cycle

Parameter	Symbol	HB56D232B-8		HB56D232B-10		HB56D232B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	ns	6

Write Cycle

Parameter	Symbol	HB56D232B-8		HB56D232B-10		HB56D232B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	20	—	25	—	ns	11

Refresh Cycle

Parameter	Symbol	HB56D232B-8		HB56D232B-10		HB56D232B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

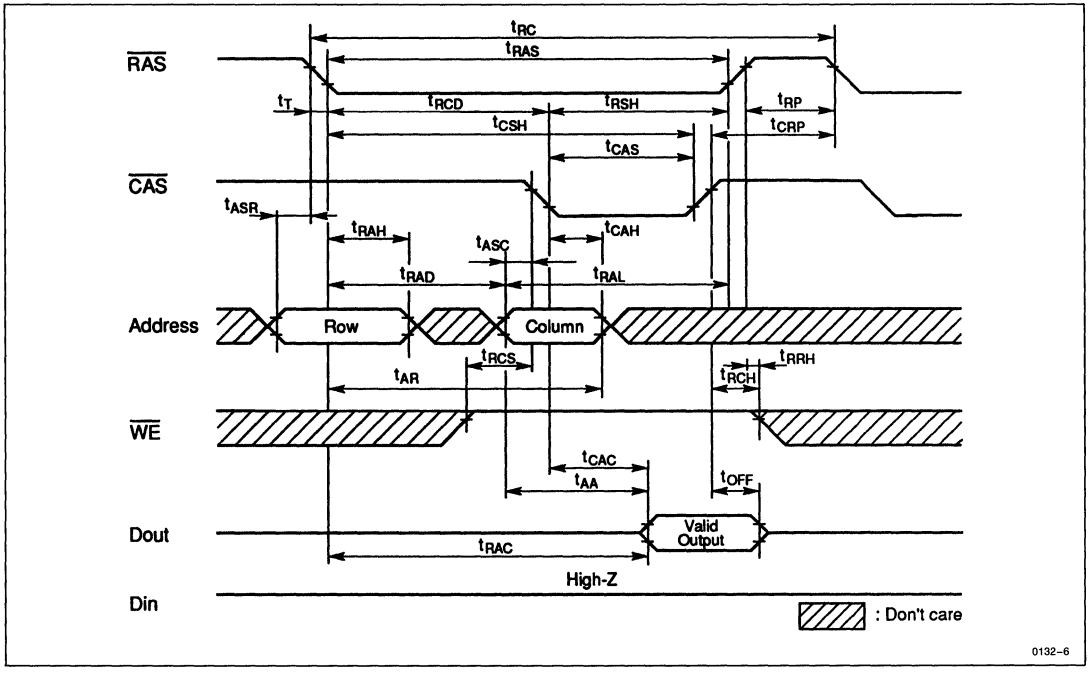
Fast Page Mode Cycle

Parameter	Symbol	HB56D232B-8		HB56D232B-10		HB56D232B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	80	100000	100	100000	120	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	50	—	ns	

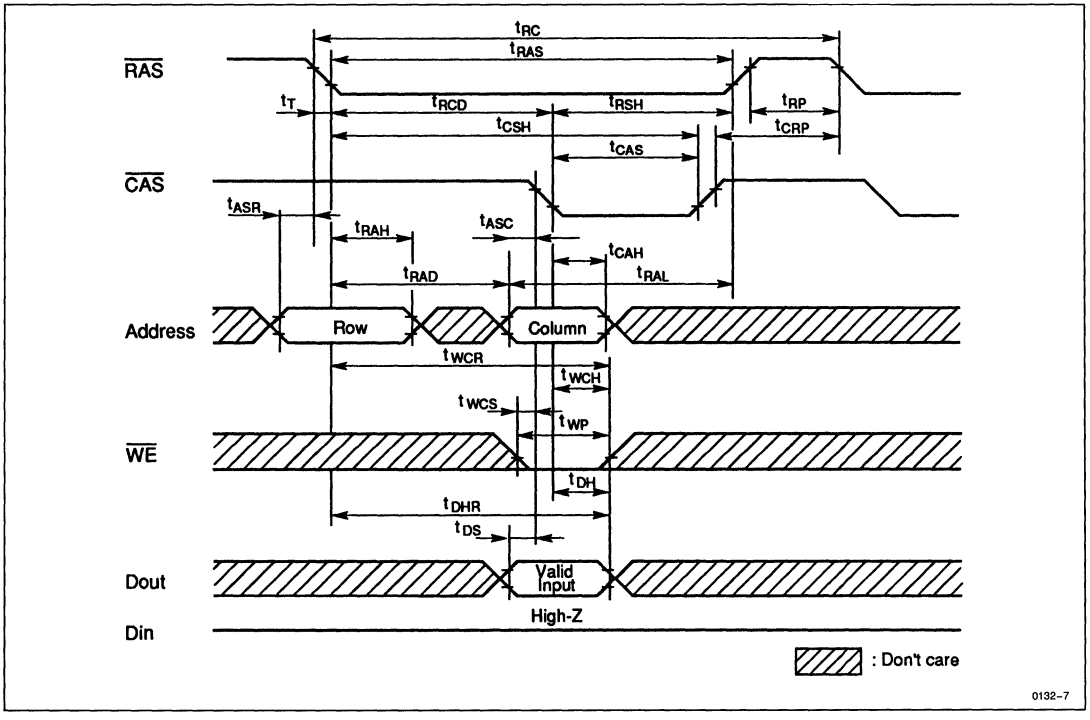
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is determined by 1,024 refresh cycles.

■ TIMING WAVEFORMS

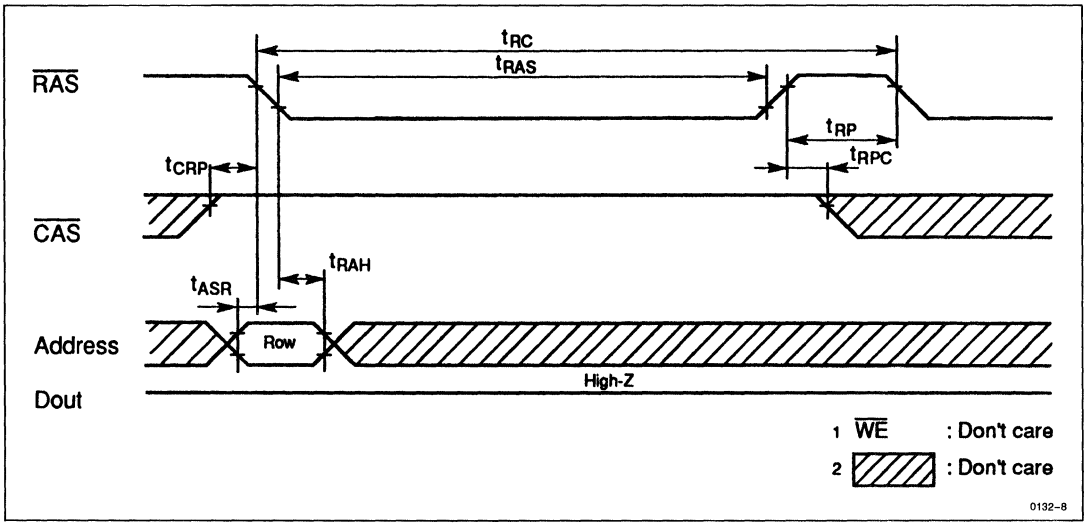
• Read Cycle



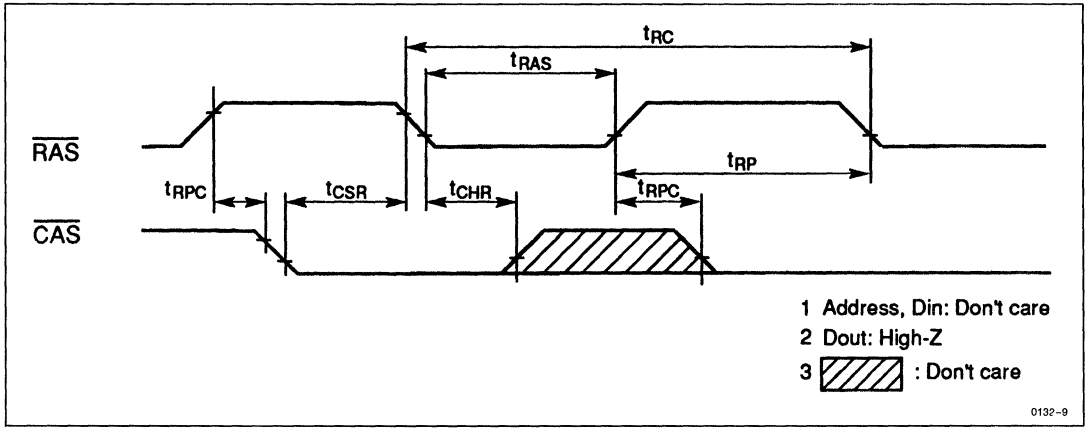
• Early Write Cycle



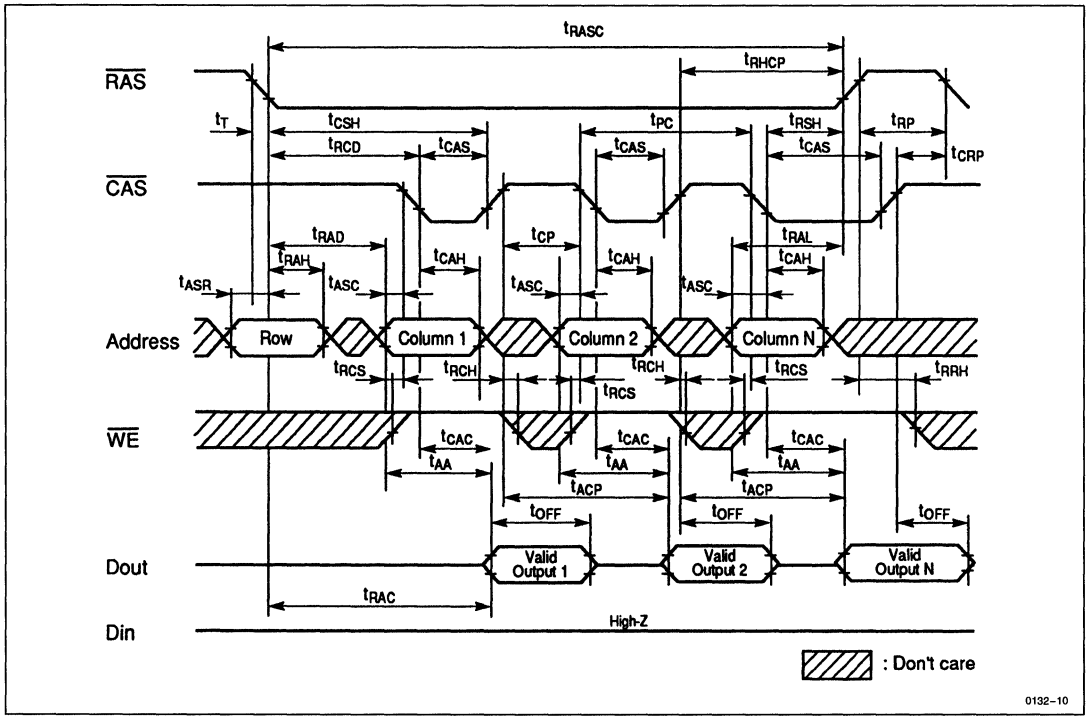
• $\overline{RAS}$ Only Refresh Cycle



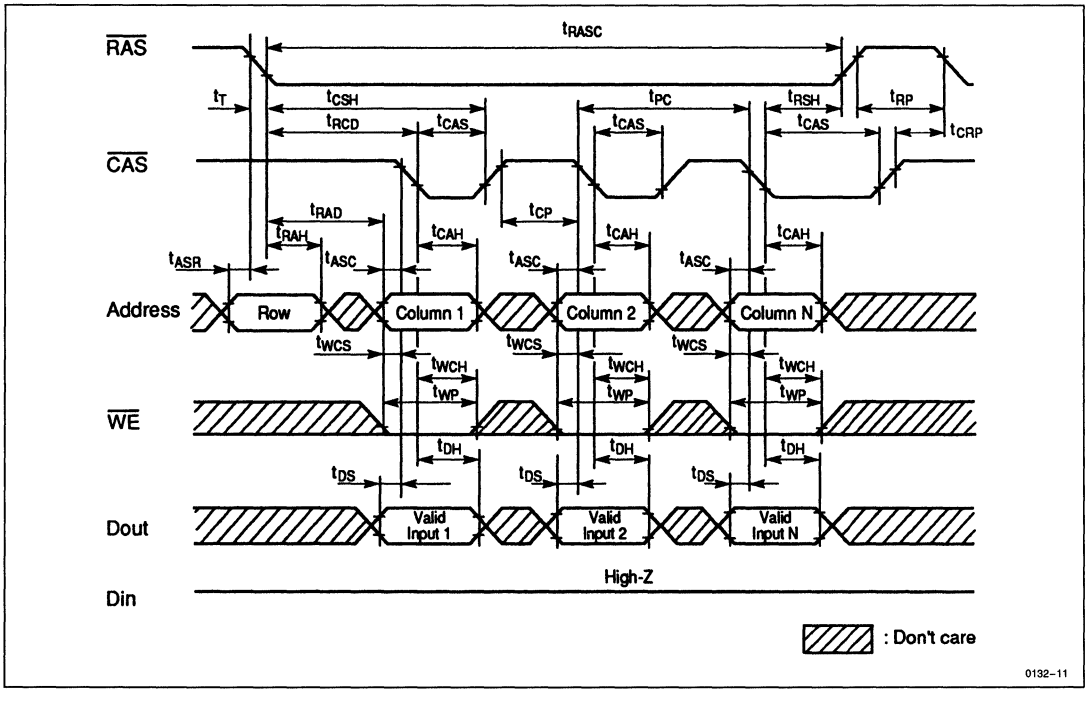
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



HB56D232BS/SBS Series

2,097,152-Word x 32-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56D232BS/SBS is a 2M x 32 dynamic RAM module, mounted 16 pieces of 4 Mbit DRAM (HM514400AJ) sealed in SOJ package. An outline of the HB56D232BS/SBS is the 72-pin single in-line package. Therefore, the HB56D232BS/SBS makes high density mounting possible without surface mount technology. The HB56D232BS/SBS provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ.

■ FEATURES

- 72-pin Single In-line Package
  - Lead Pitch 1.27mm
- Single 5V (±5%) Supply
- High Speed
  - Access Time ..... 60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode ..... 4.83W/4.41/3.99W/3.57W (max)
  - Standby Mode ..... 168 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycle ..... (16 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

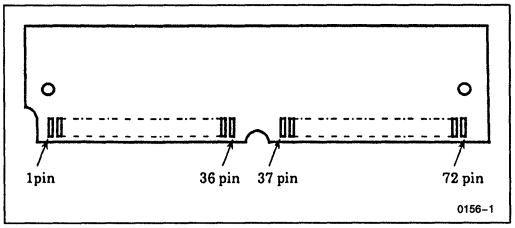
■ ORDERING INFORMATION

Part No.	Access Time	Package	Contact Pad
HB56D232BS-6A	60 ns	72-pin SIP Socket Type	Gold
HB56D232BS-7A	70 ns		
HB56D232BS-8A	80 ns		
HB56D232BS-10A	100 ns		
HB56D232SBS-6A	60 ns	72-pin SIP Socket Type	Solder
HB56D232SBS-7A	70 ns		
HB56D232SBS-8A	80 ns		
HB56D232SBS-10A	100 ns		

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_9	Refresh Address Input
DQ_0–DQ_{31}	Data-in/Data-out
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$–$\overline{RAS2}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power Supply (+ 5V)
V_{SS}	Ground
PD1–PD4	Presence Detect Pin
NC	No Connection

■ PIN OUT

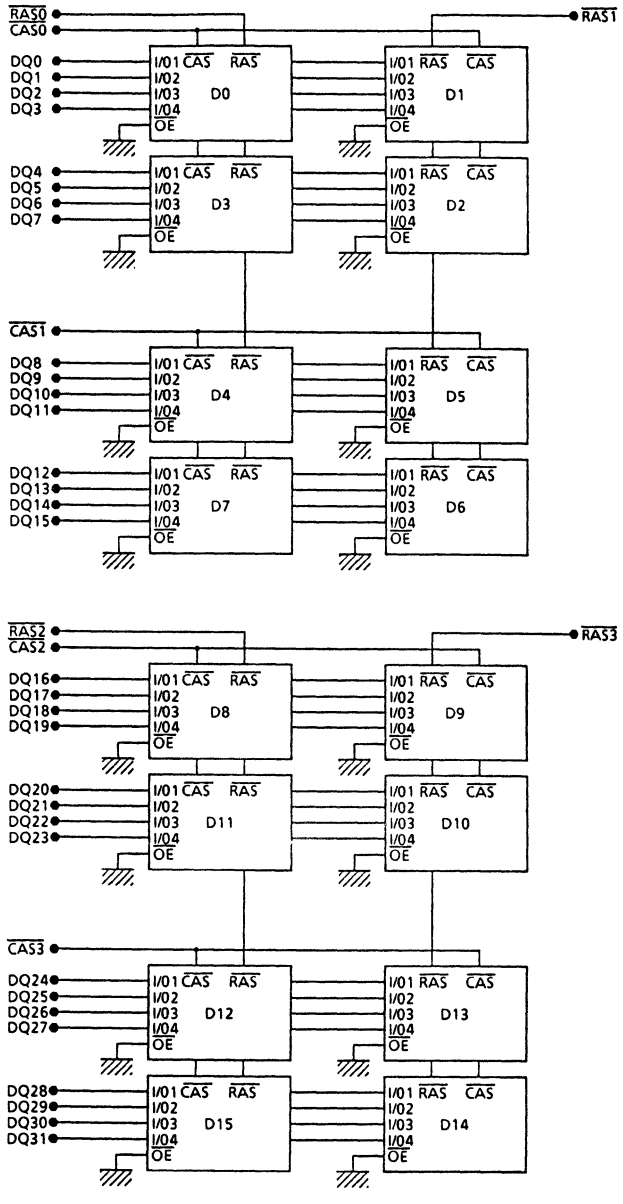


Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	NC	37	NC	55	DQ_{11}
2	DQ_0	20	DQ_4	38	NC	56	DQ_{27}
3	DQ_{16}	21	DQ_{20}	39	V_{SS}	57	DQ_{12}
4	DQ_1	22	DQ_5	40	$\overline{CAS0}$	58	DQ_{28}
5	DQ_{17}	23	DQ_{21}	41	$\overline{CAS2}$	59	V_{CC}
6	DQ_2	24	DQ_6	42	$\overline{CAS3}$	60	DQ_{29}
7	DQ_{18}	25	DQ_{22}	43	$\overline{CAS1}$	61	DQ_{13}
8	DQ_3	26	DQ_7	44	$\overline{RAS0}$	62	DQ_{30}
9	DQ_{19}	27	DQ_{23}	45	$\overline{RAS1}$	63	DQ_{14}
10	V_{CC}	28	A_7	46	NC	64	DQ_{31}
11	NC	29	NC	47	$\overline{WE}$	65	DQ_{15}
12	A_0	30	V_{CC}	48	NC	66	NC
13	A_1	31	A_8	49	DQ_8	67	PD1
14	A_2	32	A_9	50	DQ_{24}	68	PD2
15	A_3	33	NC	51	DQ_9	69	PD3
16	A_4	34	$\overline{RAS2}$	52	DQ_{25}	70	PD4
17	A_5	35	NC	53	DQ_{10}	71	NC
18	A_6	36	NC	54	DQ_{26}	72	V_{SS}

■ PRESENCE DETECT PINOUT

Pin No.	Pin Name	HB56D232BS/SBS			
		-6A	-7A	-8A	-10A
67	PD1	NC	NC	NC	NC
68	PD2	NC	NC	NC	NC
69	PD3	NC	V_{SS}	NC	V_{SS}
70	PD4	NC	NC	V_{SS}	V_{SS}

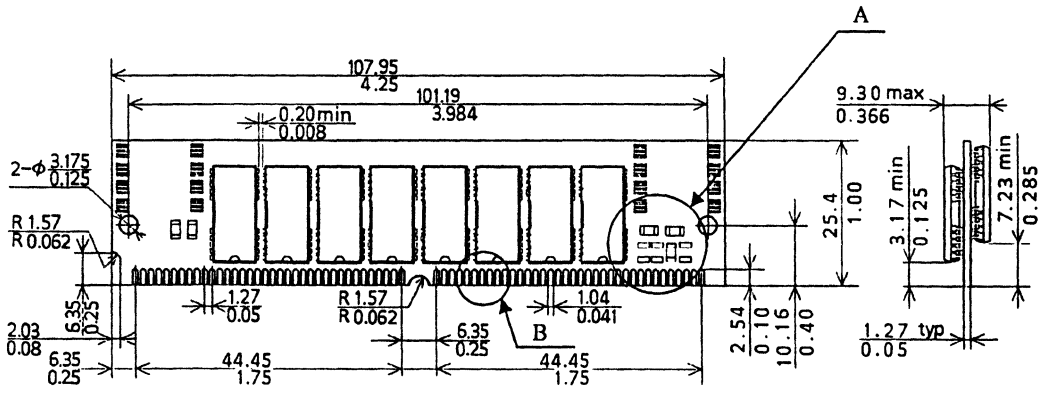
■ BLOCK DIAGRAM

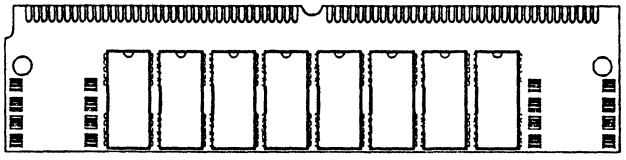


*D0–D15: HM514400AJ

■ PHYSICAL OUTLINE

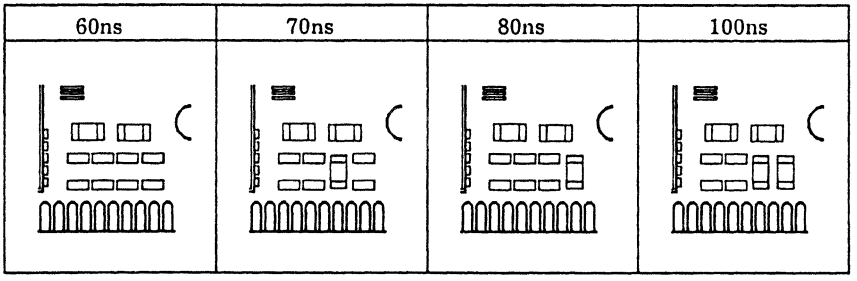
Unit: mm / inch



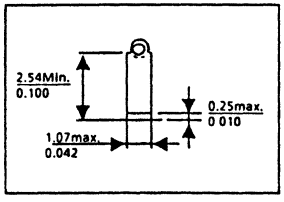


0156-3

Detail A



Detail B



Note: Following the specification of the contact pads.

Part No.	Contact Pad
HB56D232BS-XX	Gold
HB56D232SBS-XX	Solder

0156-4

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input)	V_{in}	− 1.0 to + 7.0	V
	(Output)	V_{out}	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	8	W
Operating Temperature		T_{opr}	0 to + 70	°C
Storage Temperature		T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)

Parameter	Symbol	HB56D232BS/SBS								Unit	Test Condition	Note
		-6A		-7A		-8A		-10A				
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	920	—	840	—	760	—	680	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	32	—	32	—	32	—	32	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	16	—	16	—	16	—	16	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	920	—	840	—	760	—	680	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	80	—	80	—	80	—	80	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	920	—	840	—	760	—	680	mA	t_{RC} = Min	
Page Mode Current	I_{CC7}	—	920	—	840	—	760	—	680	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed ≤ 1 time while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	121	pF	1
Input Capacitance ($\overline{WE}$)	C_{I2}	—	137	pF	1
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I3}	—	48	pF	1
Output Capacitance (DQ_0–DQ_{31})	$C_{I/O}$	—	29	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)[1, 12]

Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56D232BS/SBS								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10000	20	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	20	60	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	—	16	ms	15

Read Cycle

Parameter	Symbol	HB56D232BS/SBS								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	—	25	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RCH}	0	—	0	—	0	—	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	15	0	20	0	20	0	25	ns	6

Write Cycle

Parameter	Symbol	HB56D232BS/SBS								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	10	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	20	—	ns	11

Refresh Cycle

Parameter	Symbol	HB56D232BS/SBS								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

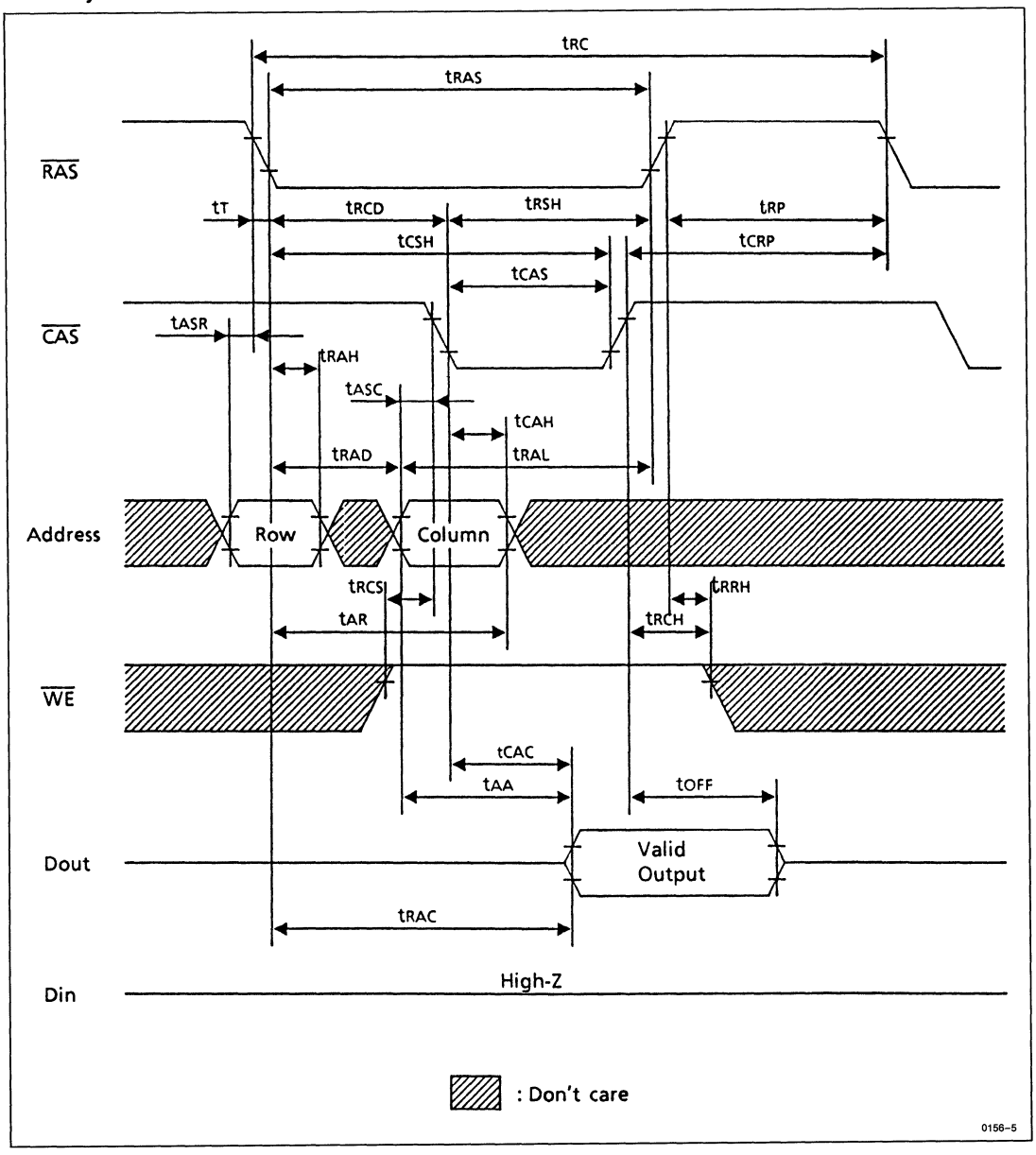
Fast Page Mode Cycle

Parameter	Symbol	HB56D232BS/SBS								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35	—	40	—	45	—	50	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	45	—	50	—	ns	

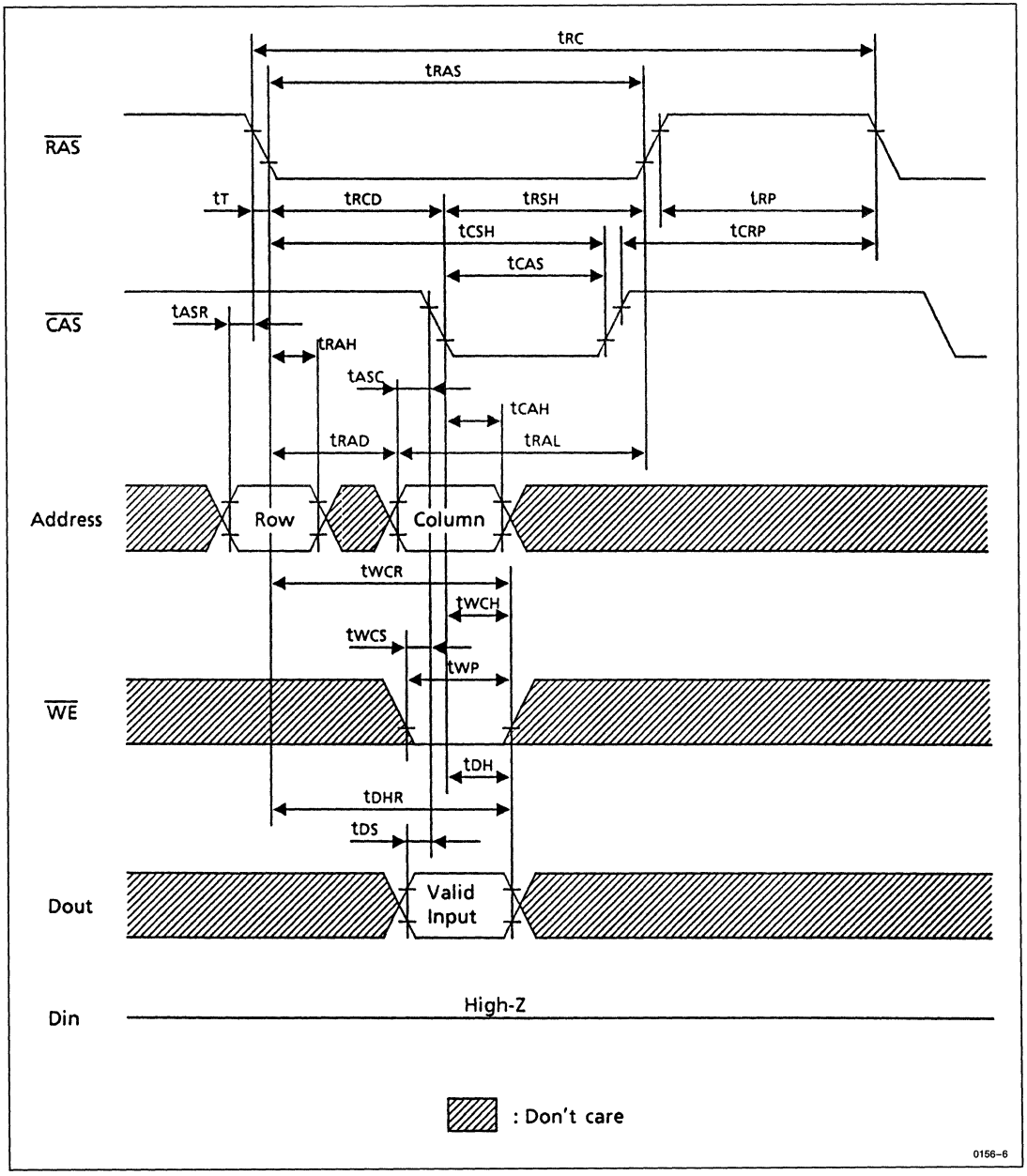
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is determined by 1,024 refresh cycles.

■ TIMING WAVEFORMS

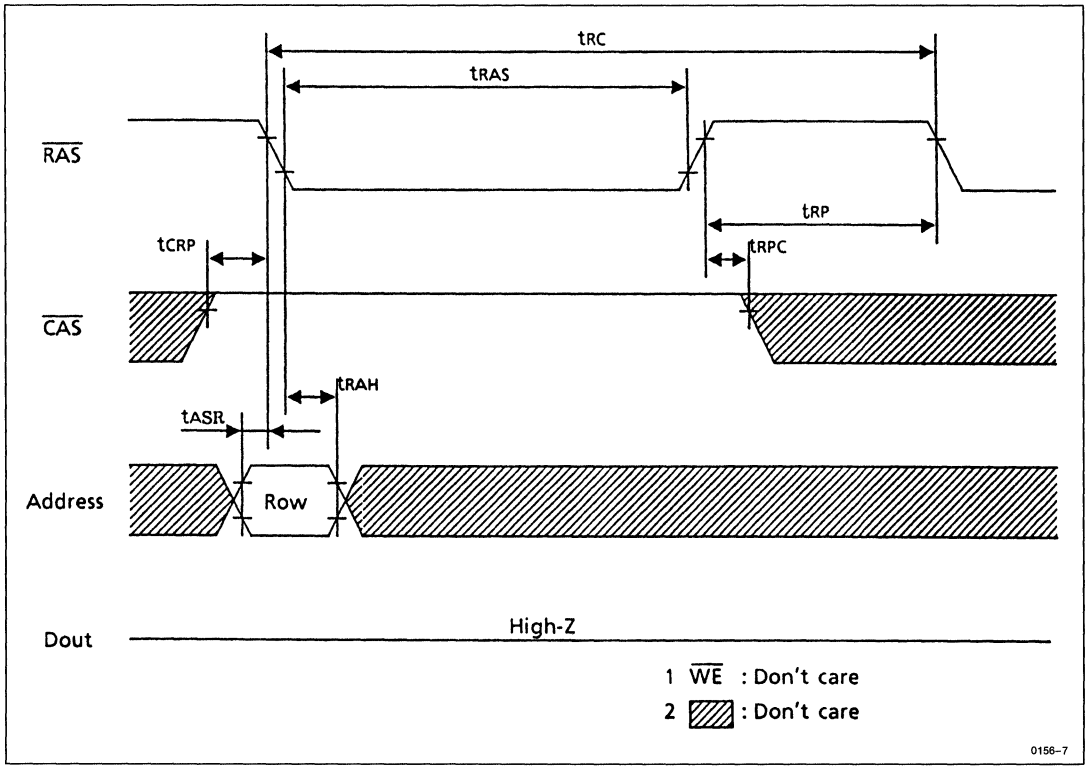
• **Read Cycle**



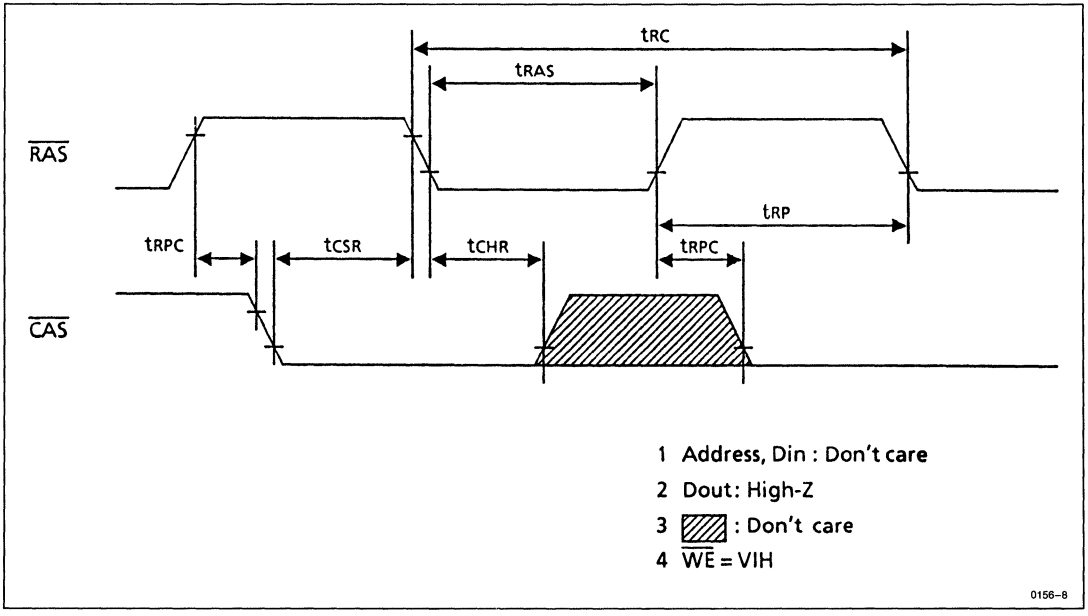
• **Early Write Cycle**



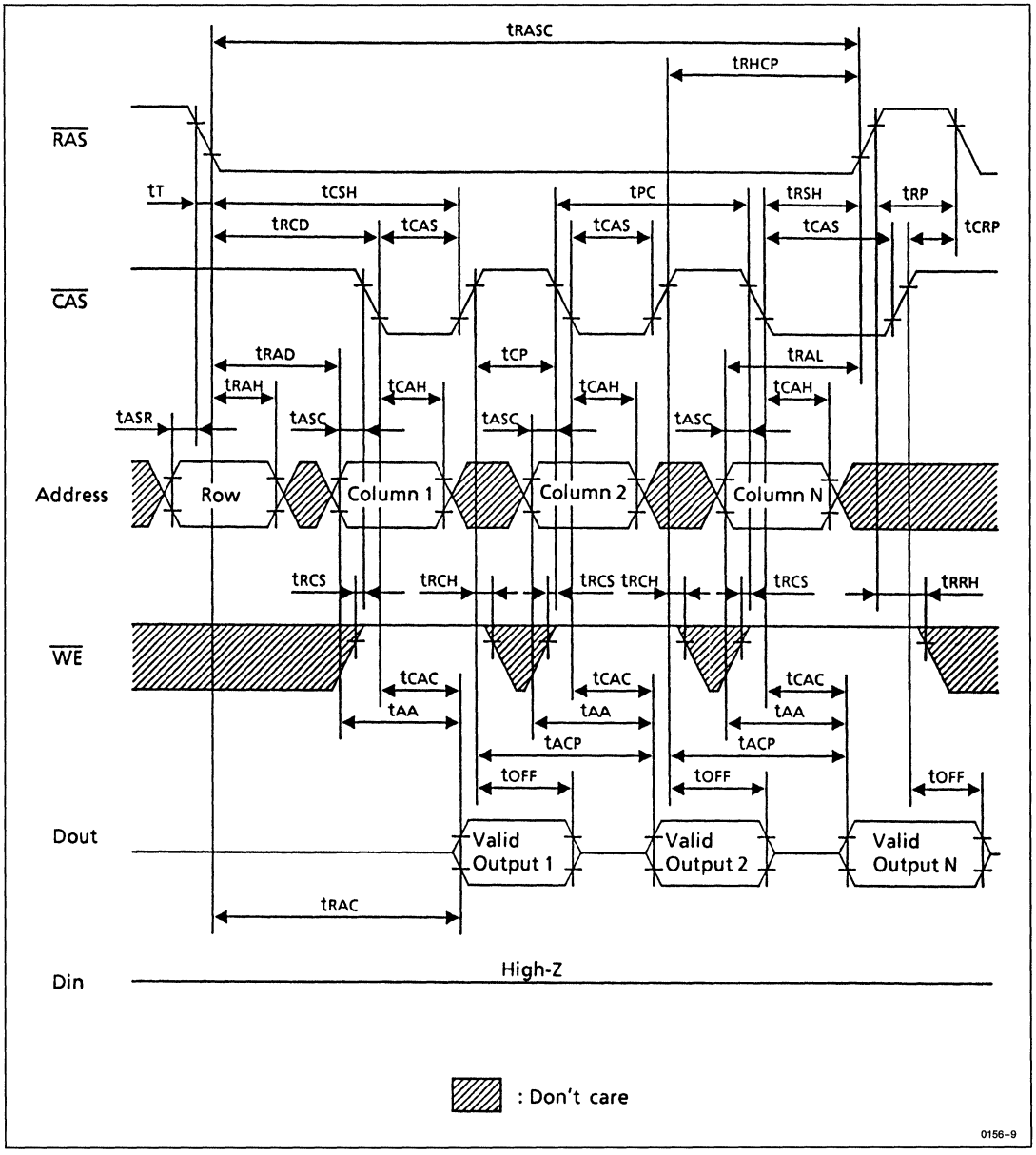
• $\overline{RAS}$ Only Refresh Cycle



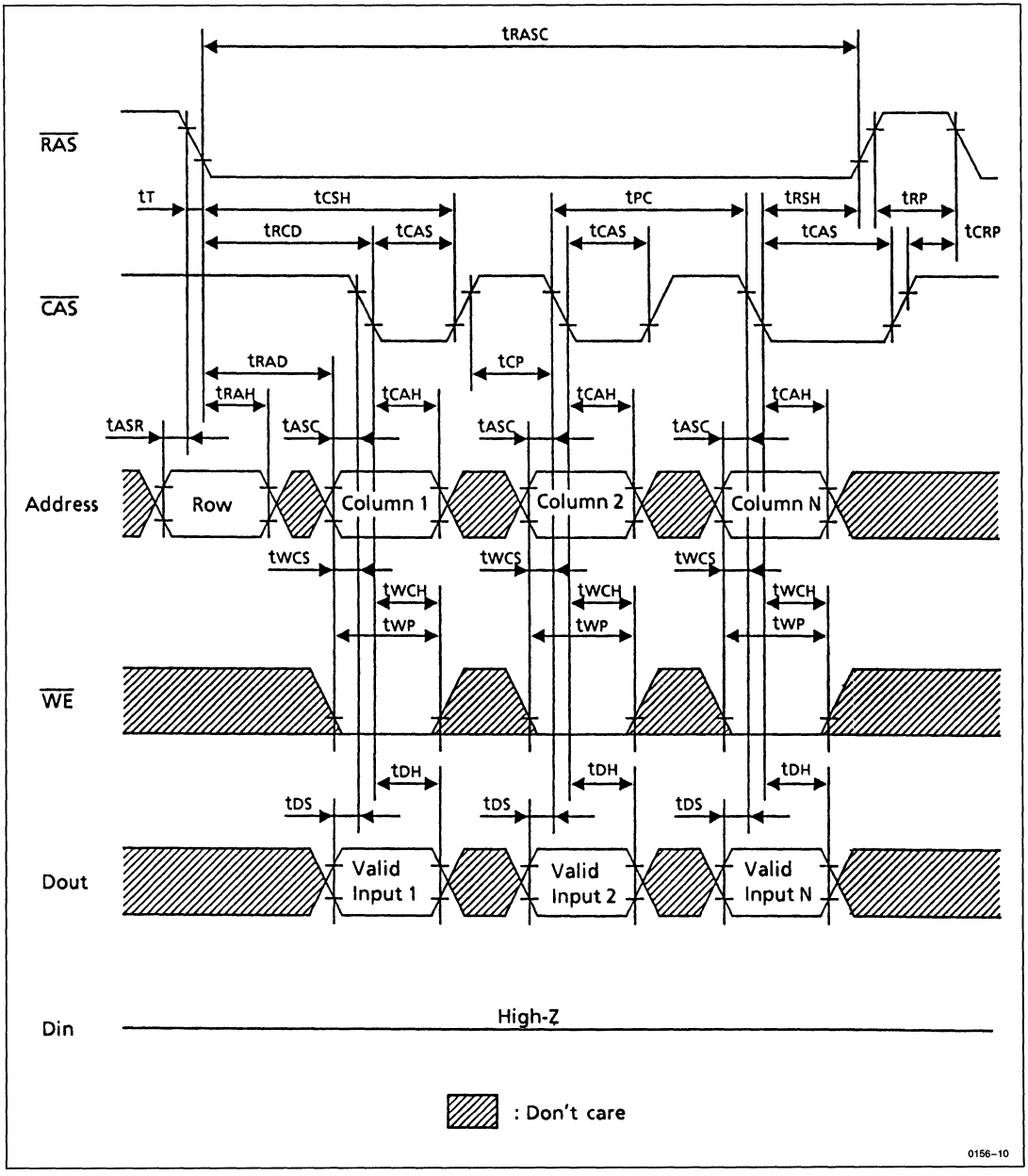
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



HB56D25636 Series

262,144-Word x 36-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56D25636B is a 256k x 36 dynamic RAM module, mounted 8 pieces of 1 Mbit DRAM (HM514256JP) sealed in SOJ package and 4 pieces of 256k-bit DRAM (HM51256CP) sealed in PLCC package. An outline of the HB56D25636B is 72-pin single in-line package. Therefore, the HB56D25636B makes high density mounting possible without surface mount technology. The HB56D25636B provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ and PLCC.

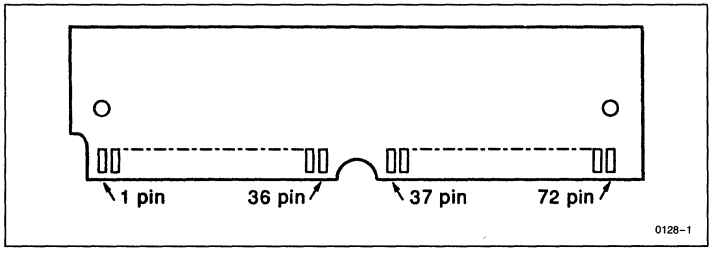
■ FEATURES

- 72-pin Single In-line Package
  - Lead Pitch 1.27mm
- Single 5V (±5%) Supply
- High Speed
  - Access Time ..... 85 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode ..... 4.24 mW/3.57 mW/3.02 mW (max)
  - Standby Mode ..... 126 mW (max)
- Fast Page Mode Capability
- 512 Refresh Cycle ..... (8 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

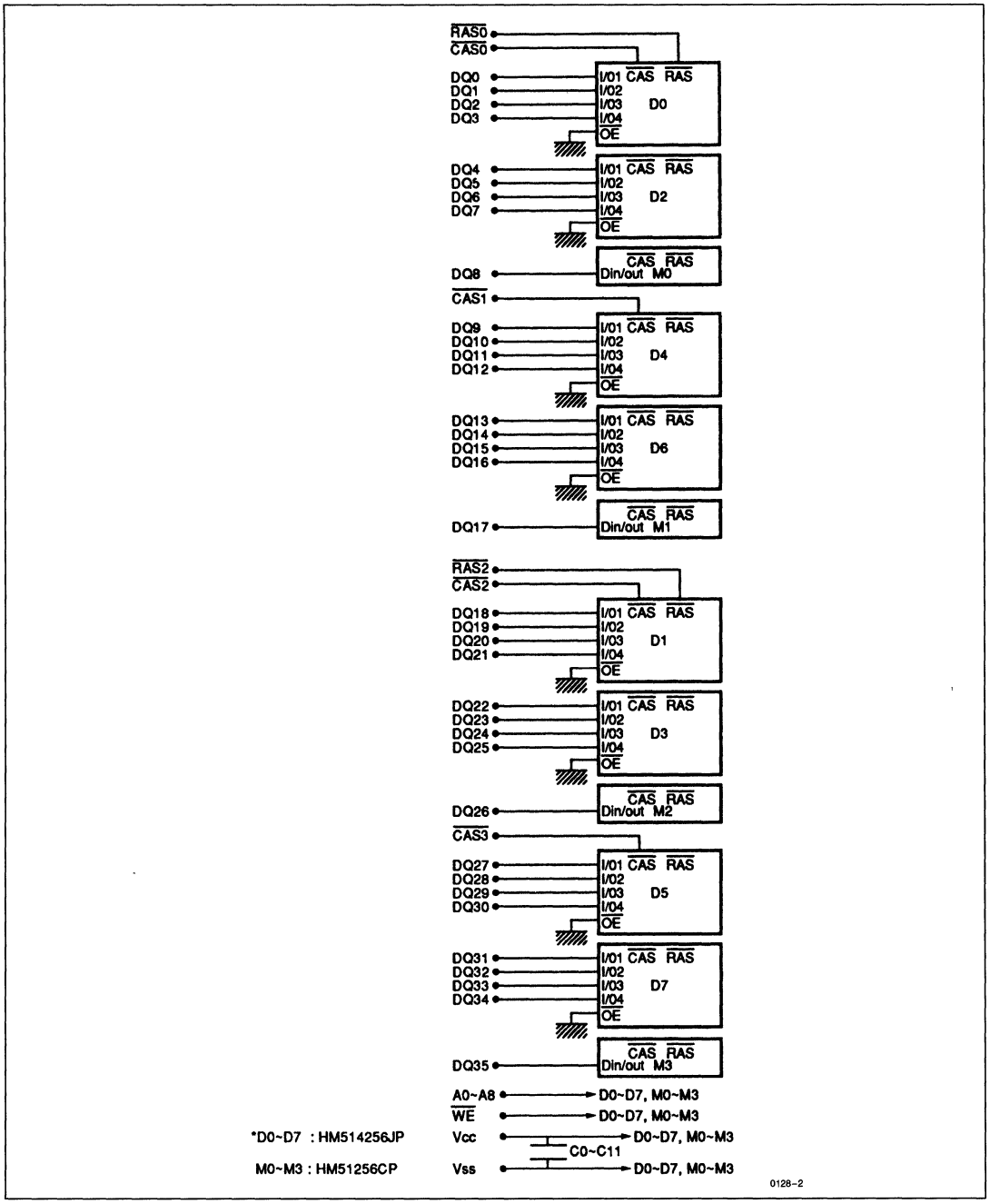
Part No.	Access Time	Package
HB56D25636B-85	85 ns	72-pin SIP Socket Type
HB56D25636B-10	100 ns	
HB56D25636B-12	120 ns	

■ PIN OUT

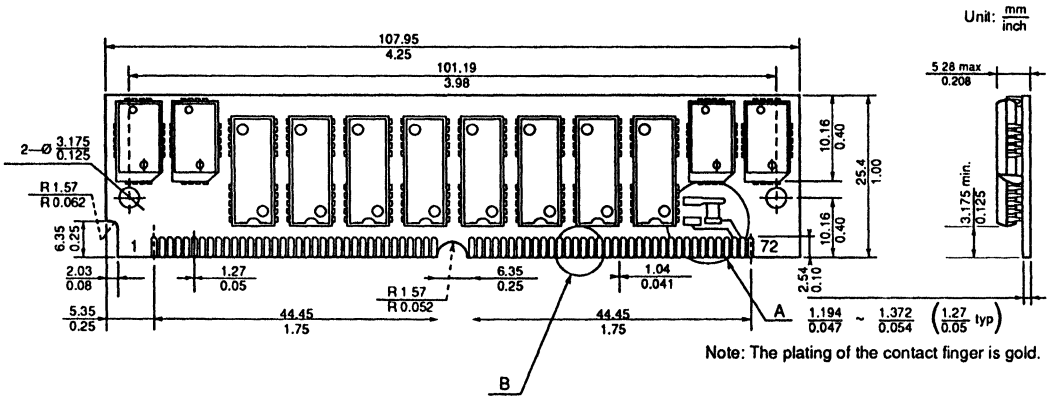


Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	37	DQ_{17}
2	DQ_0	38	DQ_{35}
3	DQ_{18}	39	V_{SS}
4	DQ_1	40	$\overline{CAS0}$
5	DQ_{19}	41	$\overline{CAS2}$
6	DQ_2	42	$\overline{CAS3}$
7	DQ_{20}	43	$\overline{CAS1}$
8	DQ_3	44	$\overline{RAS0}$
9	DQ_{21}	45	NC
10	V_{CC}	46	NC
11	NC	47	$\overline{WE}$
12	A_0	48	NC
13	A_1	49	DQ_9
14	A_2	50	DQ_{27}
15	A_3	51	DQ_{10}
16	A_4	52	DQ_{28}
17	A_5	53	DQ_{11}
18	A_6	54	DQ_{29}
19	NC	55	DQ_{12}
20	DQ_4	56	DQ_{30}
21	DQ_{22}	57	DQ_{13}
22	DQ_5	58	DQ_{31}
23	DQ_{23}	59	V_{CC}
24	DQ_6	60	DQ_{32}
25	DQ_{24}	61	DQ_{14}
26	DQ_7	62	DQ_{33}
27	DQ_{25}	63	DQ_{15}
28	A_7	64	DQ_{34}
29	NC	65	DQ_{16}
30	V_{CC}	66	NC
31	A_8	67	PD_1
32	NC	68	PD_2
33	NC	69	PD_3
34	$\overline{RAS2}$	70	PD_4
35	DQ_{26}	71	NC
36	DQ_8	72	V_{SS}

■ BLOCK DIAGRAM

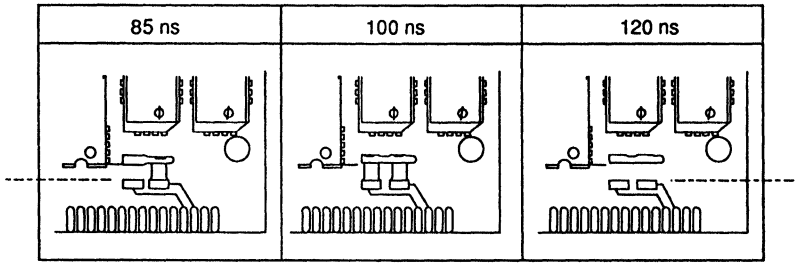


■ PHYSICAL OUTLINE

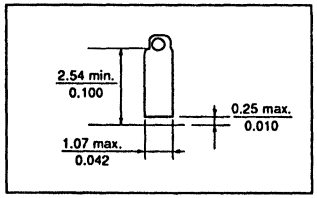


Note: The plating of the contact finger is gold.

Detail A



Detail B



0128-3

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Input
A_0–A_8	Refresh Address Input
DQ_0–DQ_{35}	Data-in/Data-out
$\overline{CAS0}$, $\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power Supply (+ 5V)
V_{SS}	Ground
PD_1–PD_4	Presence Detect Pin
NC	Non-Connection

■ PRESENCE DETECT PIN ARRANGEMENT

Pin No.	Pin Name	HB56D25636B		
		85 ns	100 ns	120 ns
67	PD_1	V_{SS}	V_{SS}	V_{SS}
68	PD_2	NC	NC	NC
69	PD_3	NC	V_{SS}	NC
70	PD_4	V_{SS}	V_{SS}	NC

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input)	V_{IN}	− 1.0 to + 7.0	V
	(Output)	V_{OUT}	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	12	W
Operating Temperature		T_{opr}	0 to + 70	°C
Storge Temperature		T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)

Parameter	Symbol	HB56D25636B						Unit	Test Conditions	Note
		-85		-10		-12				
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	808	—	680	—	576	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	24	—	24	—	24	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	12	—	12	—	12	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	808	—	680	—	576	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	64	—	64	—	64	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	768	—	660	—	556	mA	t_{RC} = Min	
Page Mode Current	I_{CC7}	—	764	—	680	—	576	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• Capacitance (T_A = 25°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	88	pF	1
Input Capacitance ($\overline{WE}$)	C_{I2}	—	104	pF	1
Input Capacitance ($\overline{RAS}$)	C_{I3}	—	57	pF	1
Input Capacitance ($\overline{CAS}$)	C_{I4}	—	36	pF	1
Output Capacitance (DQ_0–DQ_7, DQ_9–DQ_{16}, DQ_{18}–DQ_{25}, DQ_{27}–DQ_{34})	$C_{I/O1}$	—	17	pF	1, 2
Output Capacitance (DQ_8, DQ_{17}, DQ_{26}, DQ_{35})	$C_{I/O2}$	—	22	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)[1, 12]

Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56D25636B-85		HB56D25636B-10		HB56D25636B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
Column Address Hold Time to $\overline{RAS}$	t_{AR}	60	—	75	—	90	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	45	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	85	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	ns	15

Read Cycle

Parameter	Symbol	HB56D25636B-85		HB56D25636B-10		HB56D25636B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	85	—	100	—	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	ns	6

Refresh Cycle

Parameter	Symbol	HB56D25636B-85		HB56D25636B-10		HB56D25636B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	15	—	15	—	15	—	ns	

Write Cycle

Parameter	Symbol	HB56D25636B-85		HB56D25636B-10		HB56D25636B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	20	—	25	—	30	—	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	65	—	80	—	95	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	20	—	20	—	25	—	ns	11
Data-in Hold Time to $\overline{RAS}$	t_{DHR}	60	—	75	—	90	—	ns	

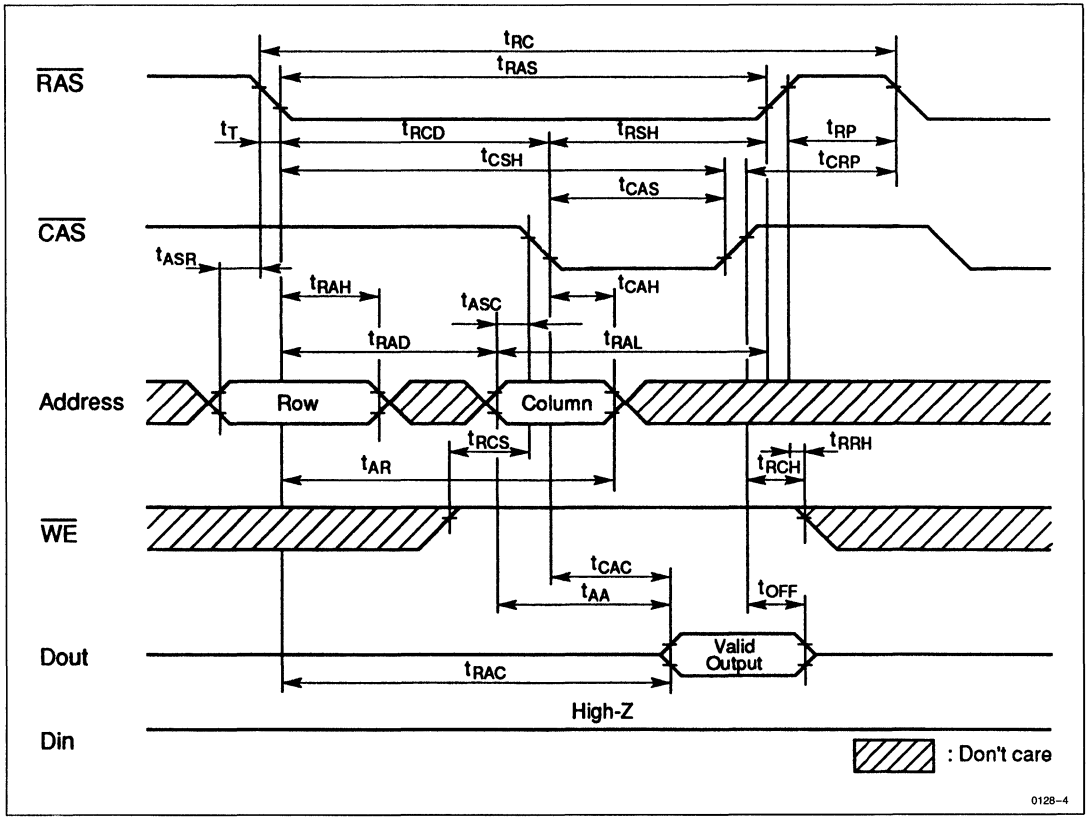
Fast Page Mode Cycle

Parameter	Symbol	HB56D25636B-85		HB56D25636B-10		HB56D25636B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	15	—	20	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	80	100000	100	100000	120	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	

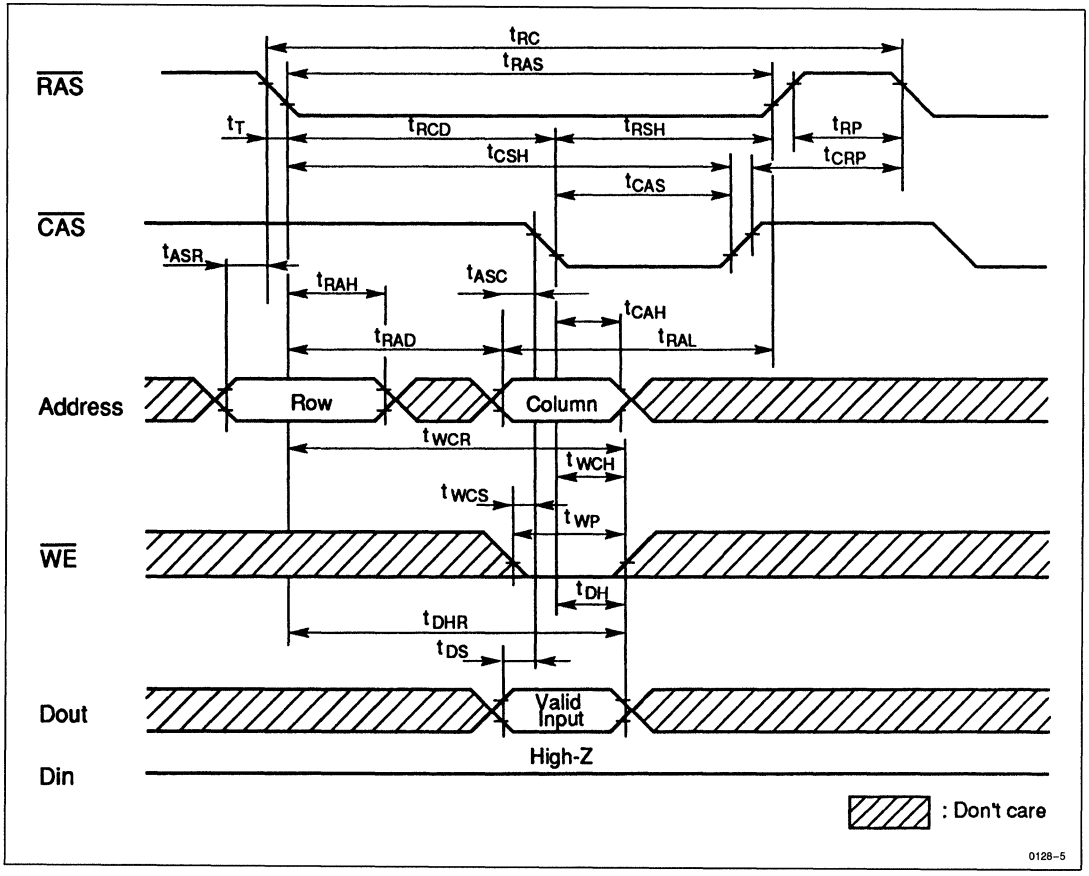
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL load and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh).
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} defines is 512 refresh cycles.

■ TIMING WAVEFORMS

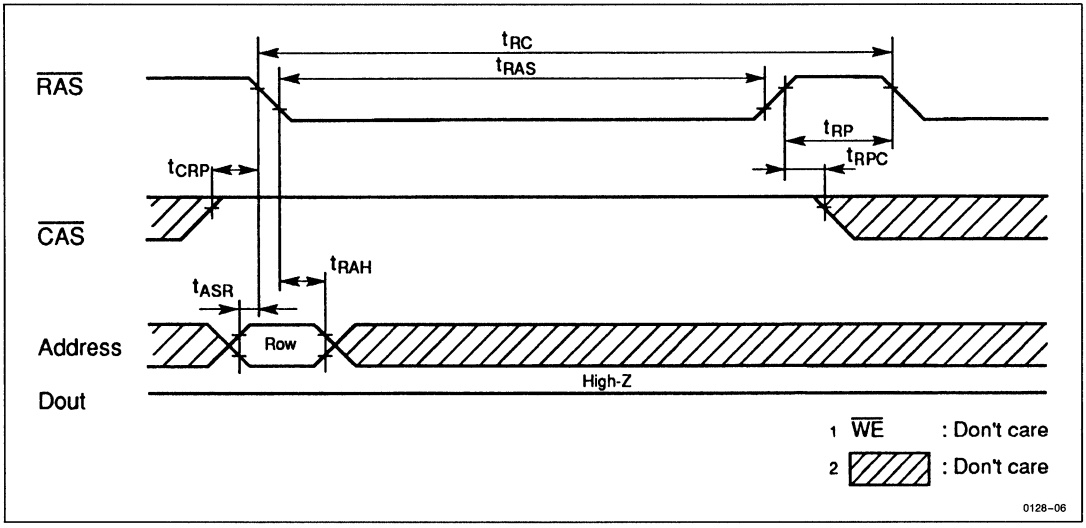
• Read Cycle



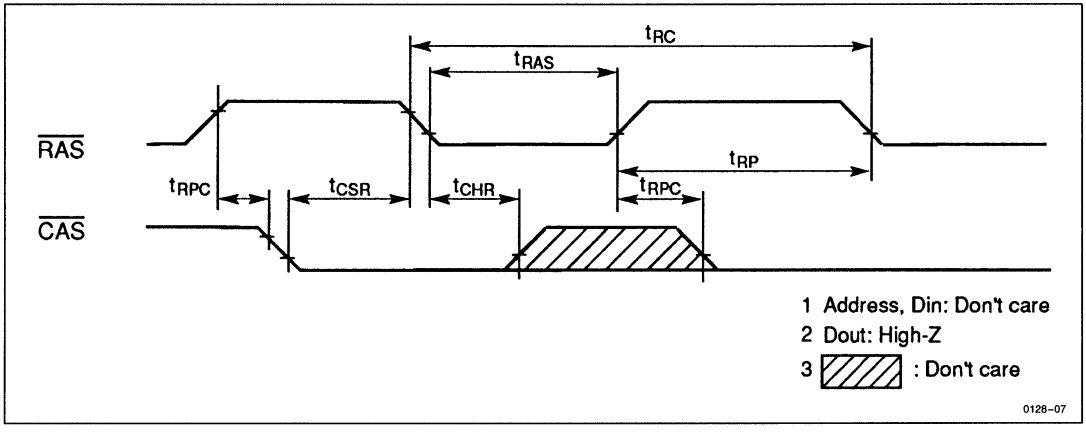
• Early Write Cycle



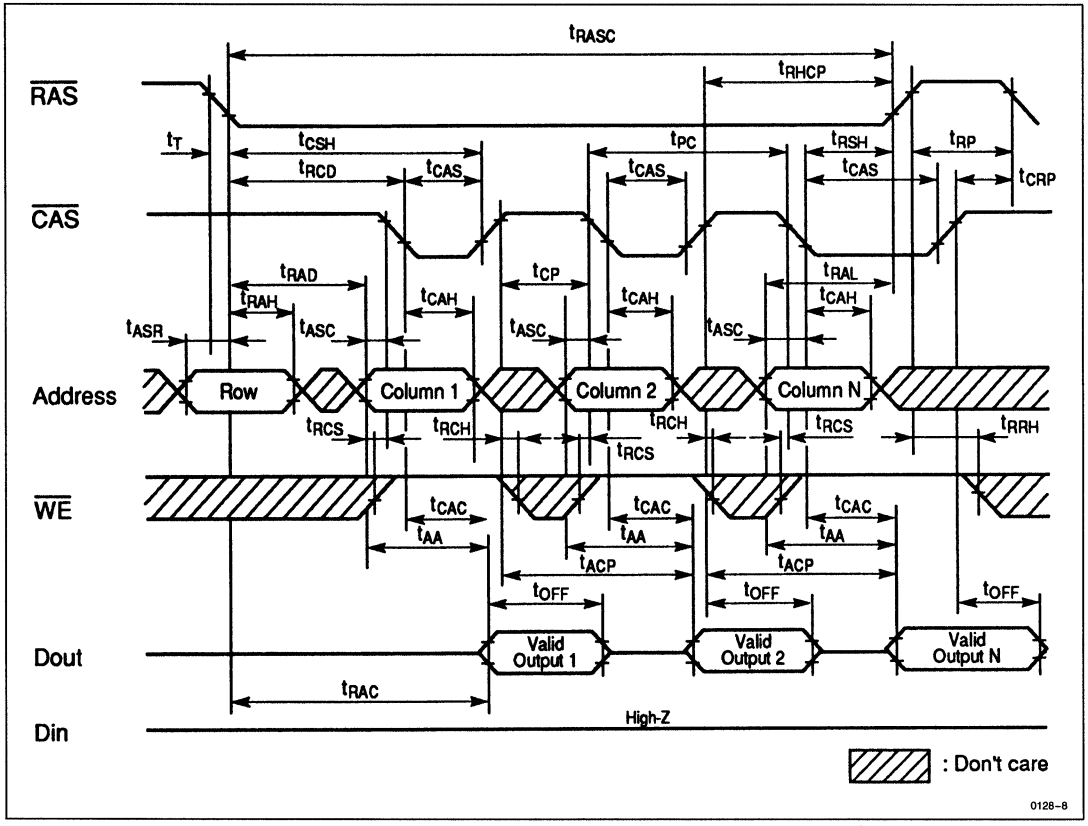
• $\overline{RAS}$ Only Refresh Cycle



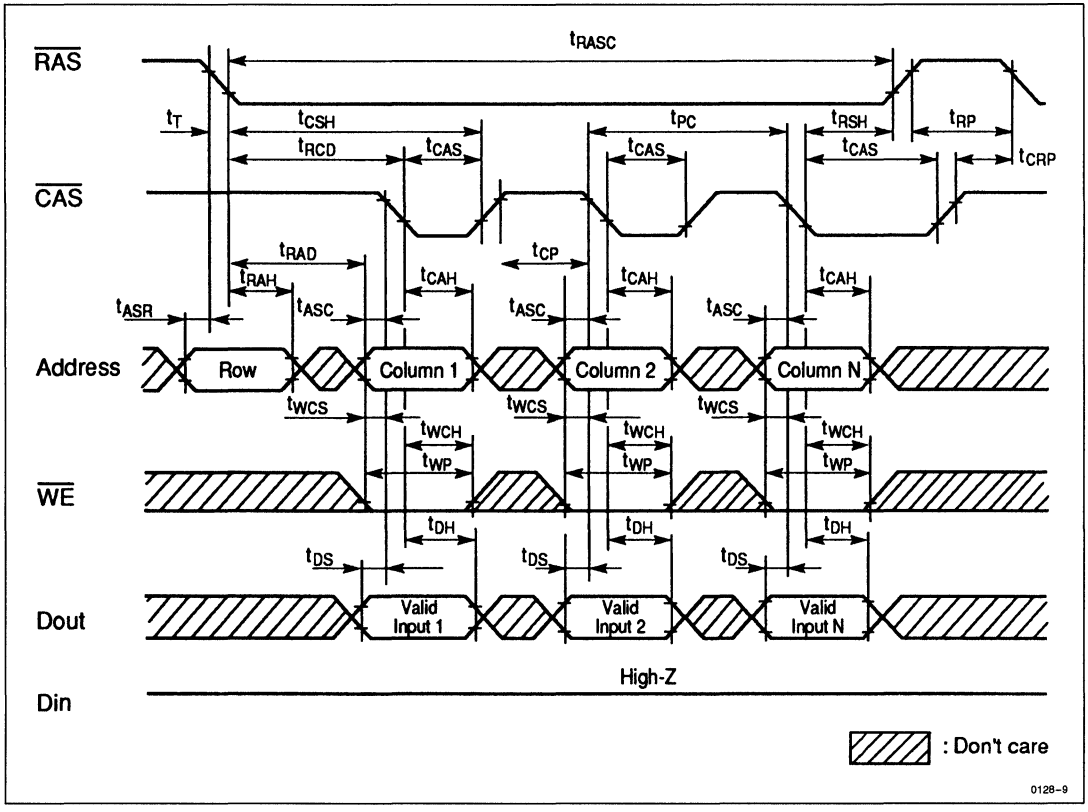
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



HB56D51236 Series

524,288-Word x 36-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56D51236B is a 512k x 36 dynamic RAM module, mounted 16 pieces of 1 Mbit DRAM (HM514256JP) sealed in SOJ package and 8 pieces of 256k-bit DRAM (HM51256CP) sealed in PLCC package. An outline of the HB56D51236B is 72-pin single in-line package. Therefore, the HB56D51236B makes high density mounting possible without surface mount technology. The HB56D51236B provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ and PLCC but only on the one side of its module board.

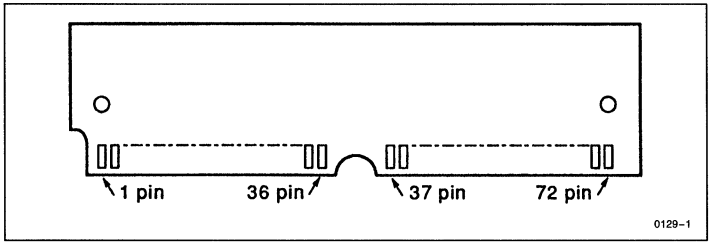
■ FEATURES

- 72-pin Single In-line Package
  - Lead Pitch 1.27mm
- Single 5V (±5%) Supply
- High Speed
  - Access Time ..... 85 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode ..... 4.58W/3.91W/3.36W (max)
  - Standby Mode ..... 252 mW (max)
- Fast Page Mode Capability
- 512 Refresh Cycle ..... (8 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

■ ORDERING INFORMATION

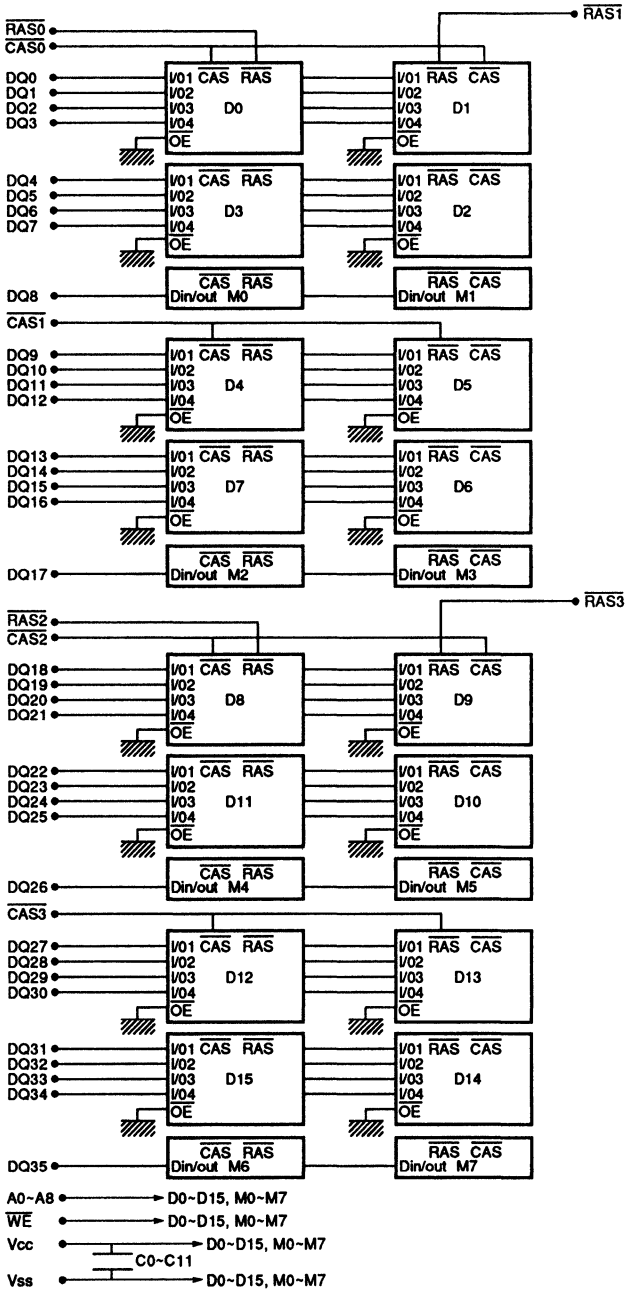
Part No.	Access Time	Package
HB56D51236B-85	85 ns	72-pin SIP Socket Type
HB56D51236B-10	100 ns	
HB56D51236B-12	120 ns	

■ PIN OUT



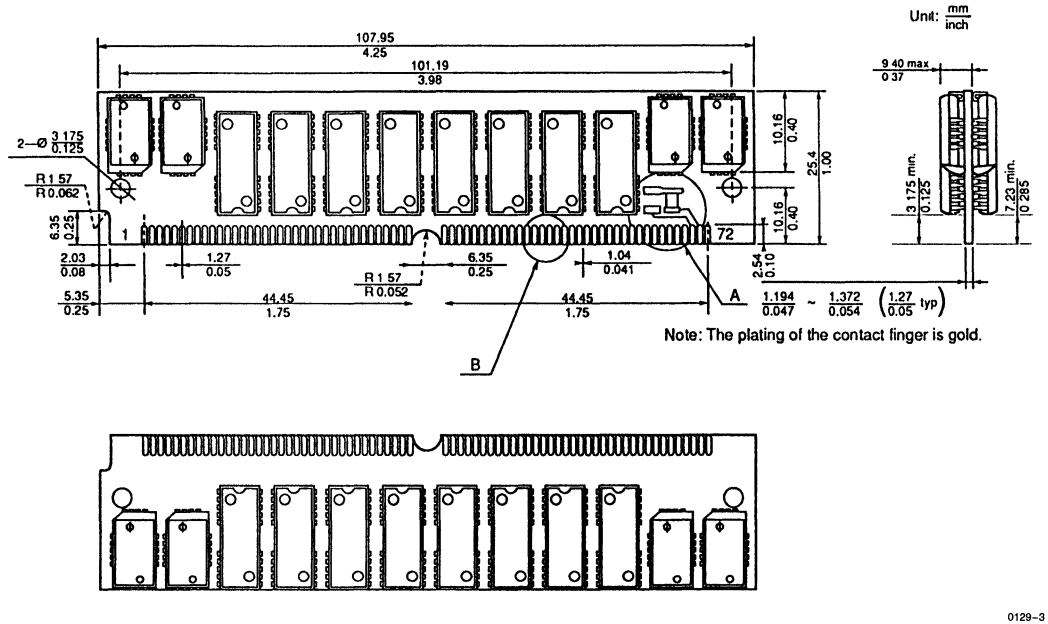
Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	37	DQ_{17}
2	DQ_0	38	DQ_{35}
3	DQ_{18}	39	V_{SS}
4	DQ_1	40	$\overline{CAS0}$
5	DQ_{19}	41	$\overline{CAS2}$
6	DQ_2	42	$\overline{CAS3}$
7	DQ_{20}	43	$\overline{CAS1}$
8	DQ_3	44	$\overline{RAS0}$
9	DQ_{21}	45	$\overline{RAS1}$
10	V_{CC}	46	NC
11	NC	47	$\overline{WE}$
12	A_0	48	NC
13	A_1	49	DQ_9
14	A_2	50	DQ_{27}
15	A_3	51	DQ_{10}
16	A_4	52	DQ_{28}
17	A_5	53	DQ_{11}
18	A_6	54	DQ_{29}
19	NC	55	DQ_{12}
20	DQ_4	56	DQ_{30}
21	DQ_{22}	57	DQ_{13}
22	DQ_5	58	DQ_{31}
23	DQ_{23}	59	V_{CC}
24	DQ_6	60	DQ_{32}
25	DQ_{24}	61	DQ_{14}
26	DQ_7	62	DQ_{33}
27	DQ_{25}	63	DQ_{15}
28	A_7	64	DQ_{34}
29	NC	65	DQ_{16}
30	V_{CC}	66	NC
31	A_8	67	PD_1
32	NC	68	PD_2
33	$\overline{RAS3}$	69	PD_3
34	$\overline{RAS2}$	70	PD_4
35	DQ_{26}	71	NC
36	DQ_8	72	V_{SS}

■ BLOCK DIAGRAM



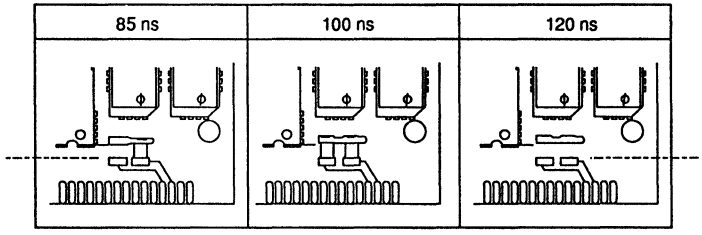
*D0～D15: HM514256JP
M0～M7: HM51256CP

■ PHYSICAL OUTLINE



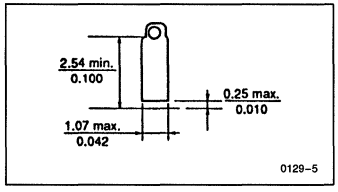
0129-3

Detail A



0129-4

Detail B



■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Input
A_0–A_8	Refresh Address Input
DQ_0–DQ_{35}	Data-in/Data-out
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$–$\overline{RAS3}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
PD_1–PD_4	Presence Detect Pin
NC	Non-Connection

■ PRESENCE DETECT PIN OUT

Pin No.	Pin Name	HB56D51236B		
		85 ns	100 ns	120 ns
67	PD_1	NC	NC	NC
68	PD_2	V_{SS}	V_{SS}	V_{SS}
69	PD_3	NC	V_{SS}	NC
70	PD_4	V_{SS}	V_{SS}	NC

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input)	V_{in}	−1.0 to +7.0	V
	(Output)	V_{out}	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	12	W
Operating Temperature		T_{opr}	0 to +70	°C
Storage Temperature		T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)

Parameter	Symbol	HB56D51236B-85		HB56D51236B-10		HB56D51236B-12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	872	—	744	—	640	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	48	—	48	—	48	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	24	—	24	—	24	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	872	—	744	—	640	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	128	—	128	—	128	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	832	—	724	—	620	mA	t_{RC} = Min	
Page Mode Current	I_{CC7}	—	828	—	744	—	640	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	µA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	µA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• Capacitance (T_A = 25°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	161	pF	1
Input Capacitance ($\overline{WE}$)	C_{I2}	—	193	pF	1
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I3}	—	62	pF	1
Output Capacitance (DQ_{0-7}, DQ_{9-16}, DQ_{18-25}, DQ_{27-34})	$C_{I/O1}$	—	29	pF	1, 2
Output Capacitance ($DQ_{8, 17, 26, 35}$)	$C_{I/O2}$	—	39	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)[1, 12]

Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56D51236B-85		HB56D51236B-10		HB56D51236B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
Column Address Hold Time to $\overline{RAS}$	t_{AR}	60	—	75	—	90	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	45	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	85	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	ns	15

Read Cycle

Parameter	Symbol	HB56D51236B-85		HB56D51236B-10		HB56D51236B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	85	—	100	—	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	ns	6

Write Cycle

Parameter	Symbol	HB56D51236B-85		HB56D51236B-10		HB56D51236B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	20	—	25	—	30	—	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	65	—	80	—	95	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	20	—	20	—	25	—	ns	11
Data-in Hold Time to $\overline{RAS}$	t_{DHR}	60	—	75	—	90	—	ns	

Refresh Cycle

Parameter	Symbol	HB56D51236B-85		HB56D51236B-10		HB56D51236B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	15	—	15	—	15	—	ns	

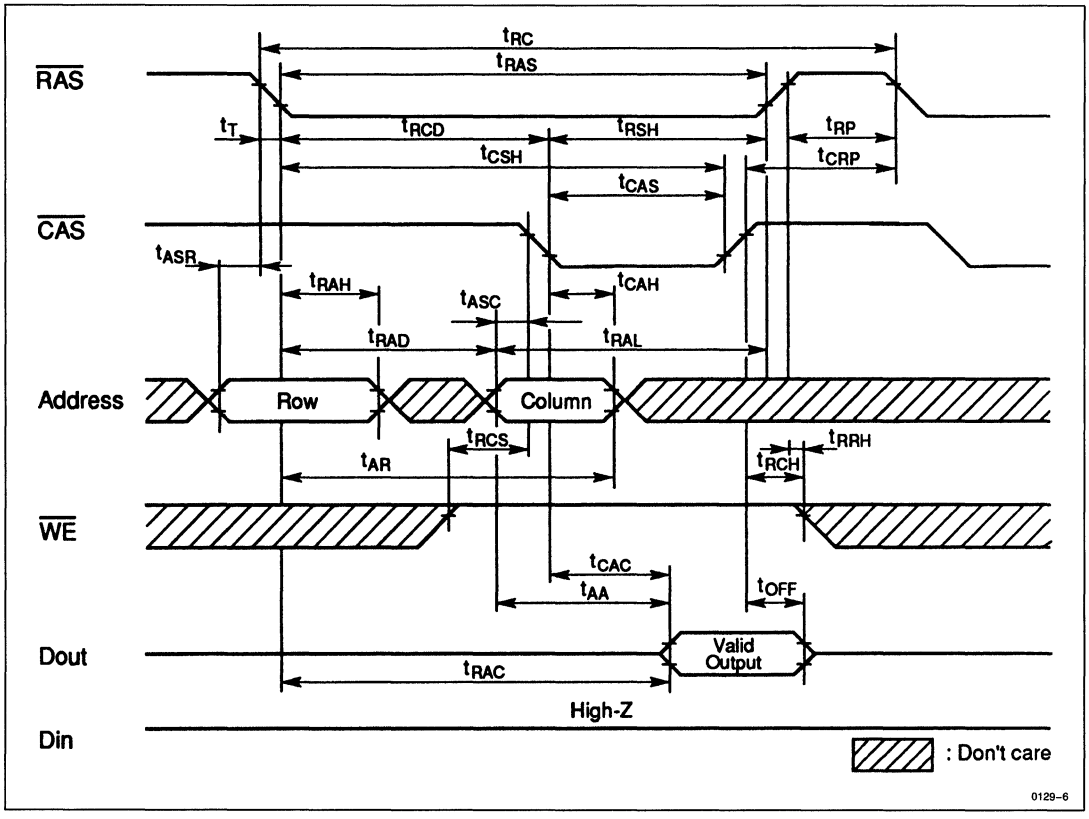
Fast Page Mode Cycle

Parameter	Symbol	HB56D51236B-85		HB56D51236B-10		HB56D51236B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	15	—	20	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	80	100000	100	100000	120	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	

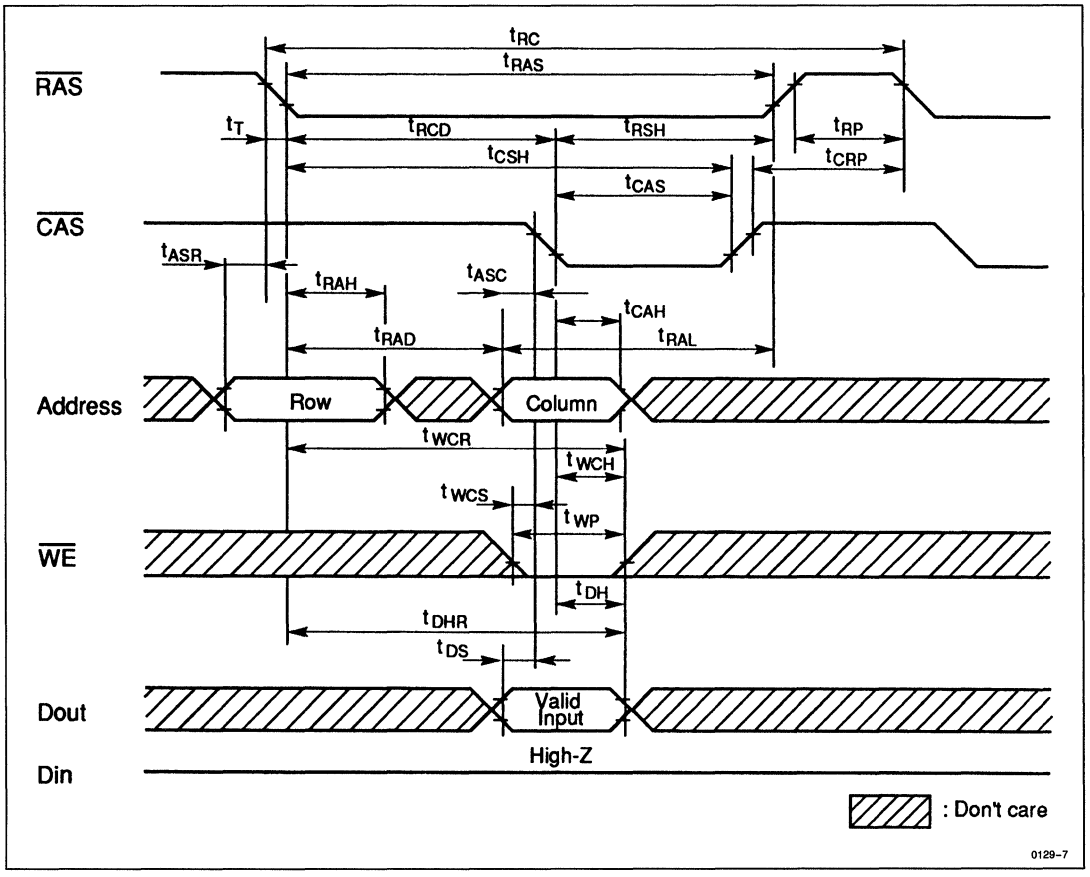
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh).
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is defined as 512 refresh cycles.

■ TIMING WAVEFORMS

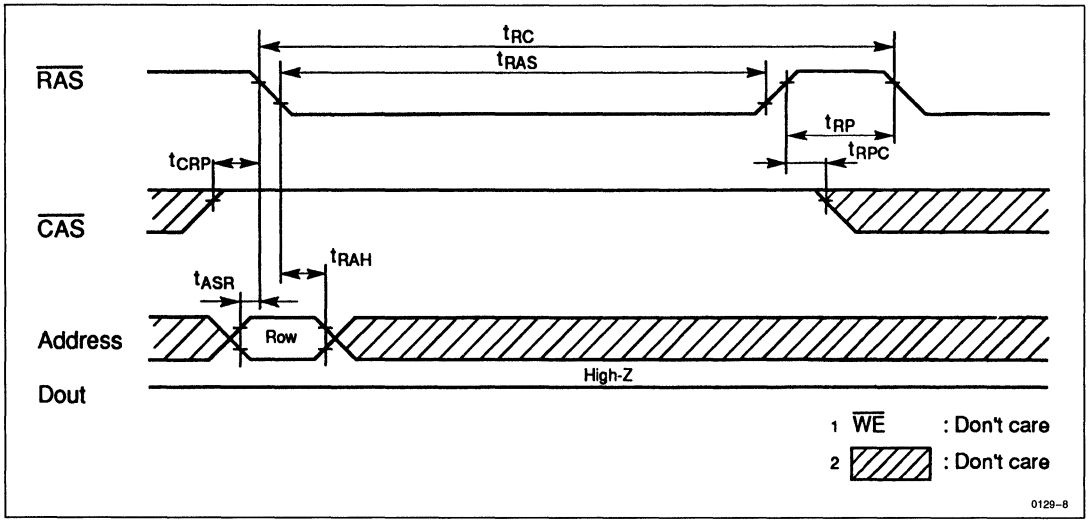
• Read Cycle



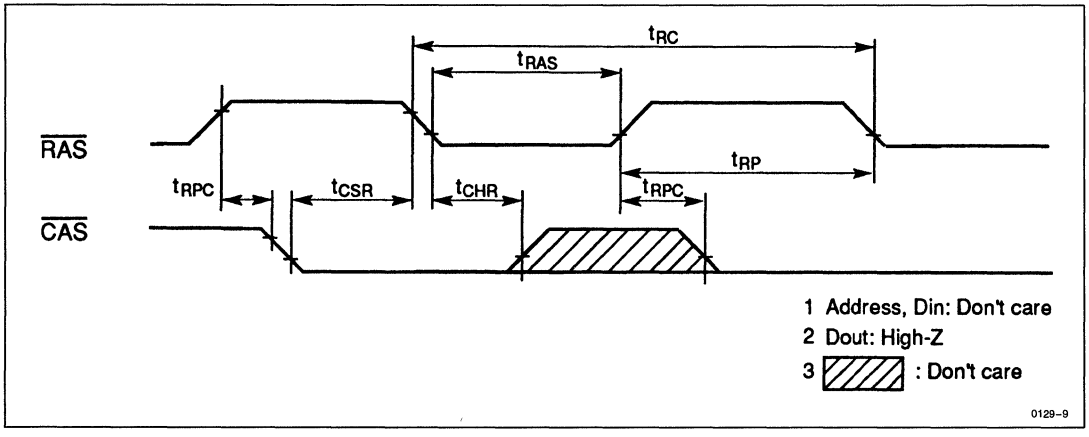
• **Early Write Cycle**



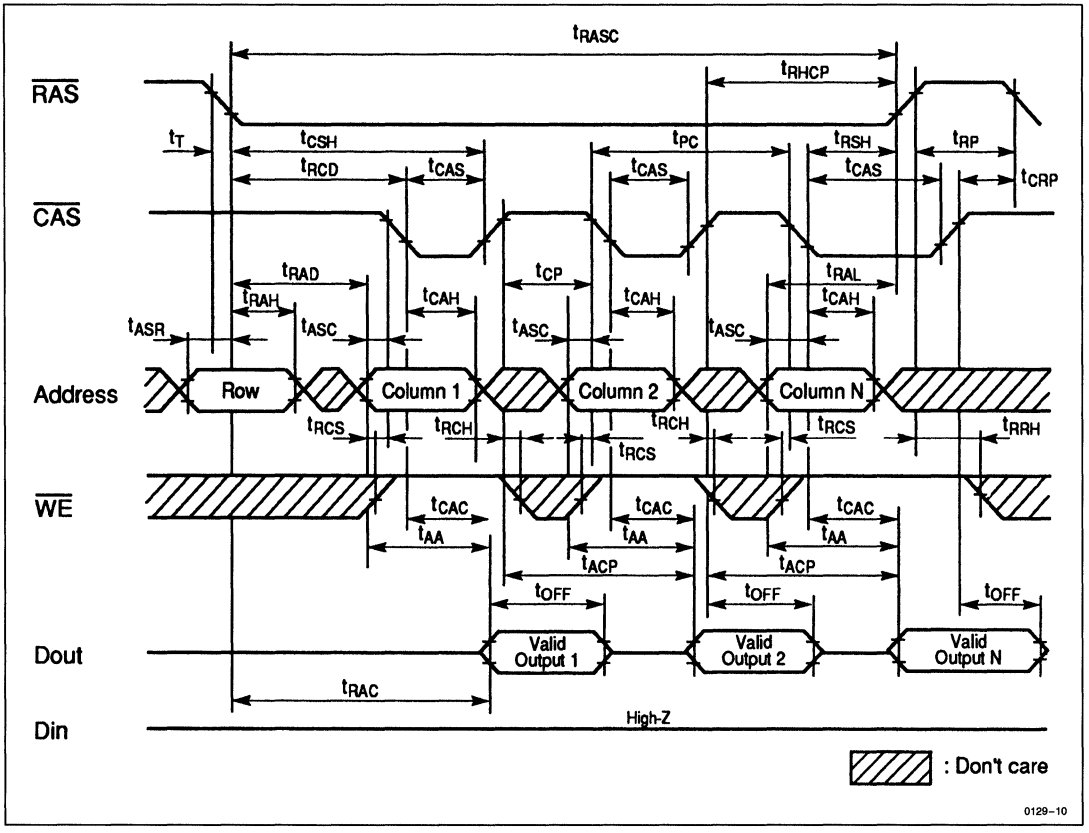
• $\overline{RAS}$ Only Refresh Cycle



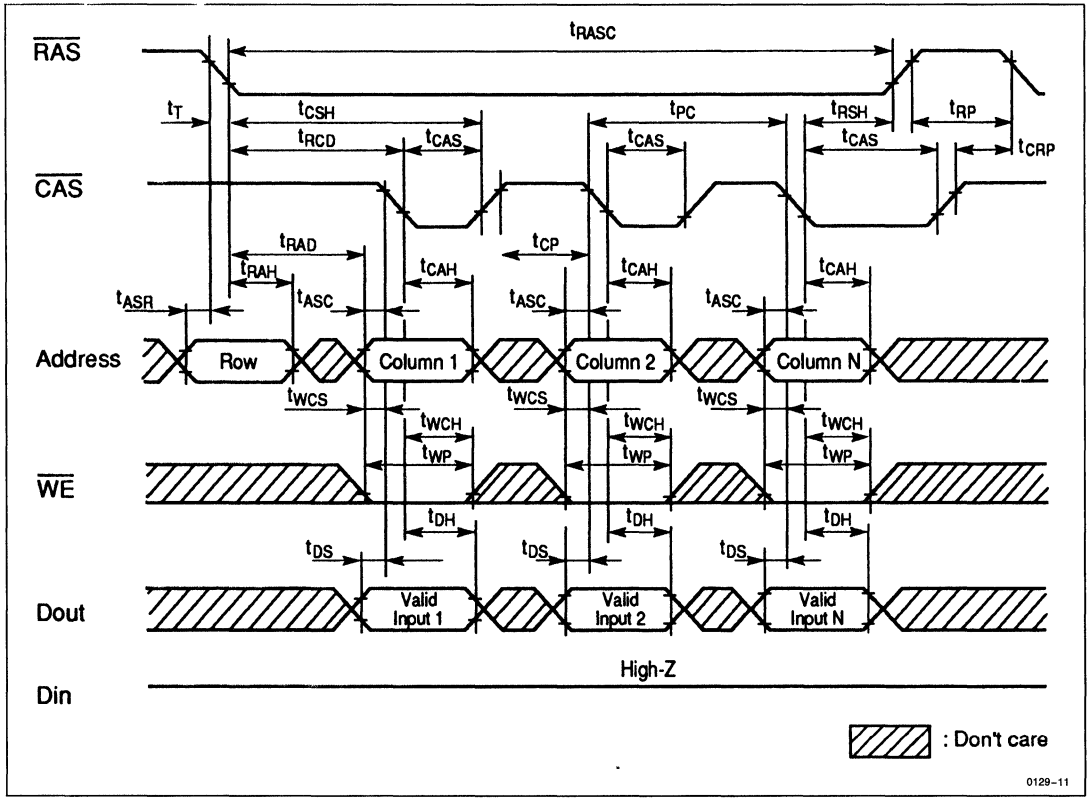
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



HB56D136B Series

1,048,576-Word x 36-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56D136B is a 1M x 36 dynamic RAM module, mounted 8 pieces of 4 Mbit DRAM (HM514400JP) sealed in SOJ package and 4 pieces of 1 Mbit DRAM (HM511000AJP) sealed in SOJ package. An outline of the HB56D136B is 72-pin single in-line package. Therefore, the HB56D136B makes high density mounting possible without surface mount technology. The HB56D136B provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ.

■ FEATURES

- 72-pin Single In-line Package
  - Lead Pitch 1.27mm
- Single 5V (±5%) Supply
- High Speed
  - Access Time ..... 80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode ..... 5.25W/4.62W/3.99W (max)
  - Standby Mode ..... 126 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycle ..... (16 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

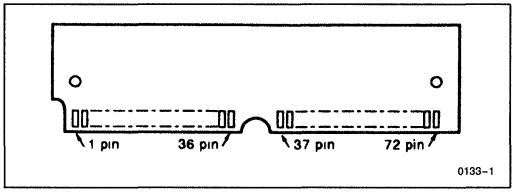
■ ORDERING INFORMATION

Part No.	Access Time	Package
HB56D136B-8	80 ns	72-pin SIP Socket Type
HB56D136B-10	100 ns	
HB56D136B-12	120 ns	

■ PRESENCE DETECT PIN OUT

Pin No.	Pin Name	HB56D136B		
		80 ns	100 ns	120 ns
67	PD_1	V_{SS}	V_{SS}	V_{SS}
68	PD_2	V_{SS}	V_{SS}	V_{SS}
69	PD_3	NC	V_{SS}	NC
70	PD_4	V_{SS}	V_{SS}	NC

■ PIN OUT

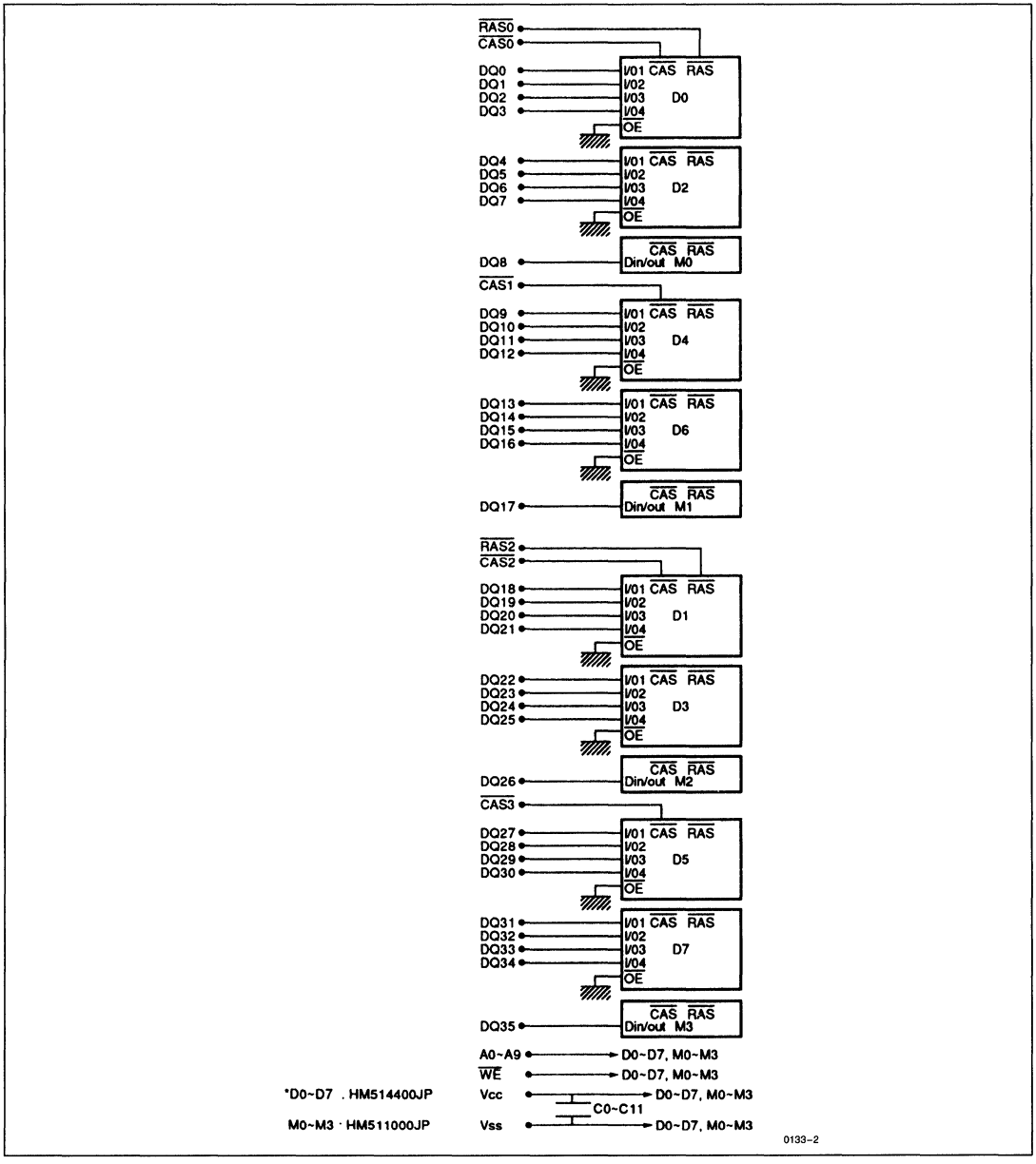


Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	NC	37	DQ_{17}	55	DQ_{12}
2	DQ_0	20	DQ_4	38	DQ_{35}	56	DQ_{30}
3	DQ_{18}	21	DQ_{22}	39	V_{SS}	57	DQ_{13}
4	DQ_1	22	DQ_5	40	$\overline{CAS}_0$	58	DQ_{31}
5	DQ_{19}	23	DQ_{23}	41	$\overline{CAS}_2$	59	V_{CC}
6	DQ_2	24	DQ_6	42	$\overline{CAS}_3$	60	DQ_{32}
7	DQ_{20}	25	DQ_{24}	43	$\overline{CAS}_1$	61	DQ_{14}
8	DQ_3	26	DQ_7	44	$\overline{RAS}_0$	62	DQ_{33}
9	DQ_{21}	27	DQ_{25}	45	NC	63	DQ_{15}
10	V_{CC}	28	A_7	46	NC	64	DQ_{34}
11	NC	29	NC	47	$\overline{WE}$	65	DQ_{16}
12	A_0	30	V_{CC}	48	NC	66	NC
13	A_1	31	A_8	49	DQ_9	67	PD_1
14	A_2	32	A_9	50	DQ_{27}	68	PD_2
15	A_3	33	NC	51	DQ_{10}	69	PD_3
16	A_4	34	$\overline{RAS}_2$	52	DQ_{28}	70	PD_4
17	A_5	35	DQ_{26}	53	DQ_{11}	71	NC
18	A_6	36	DQ_8	54	DQ_{29}	72	V_{SS}

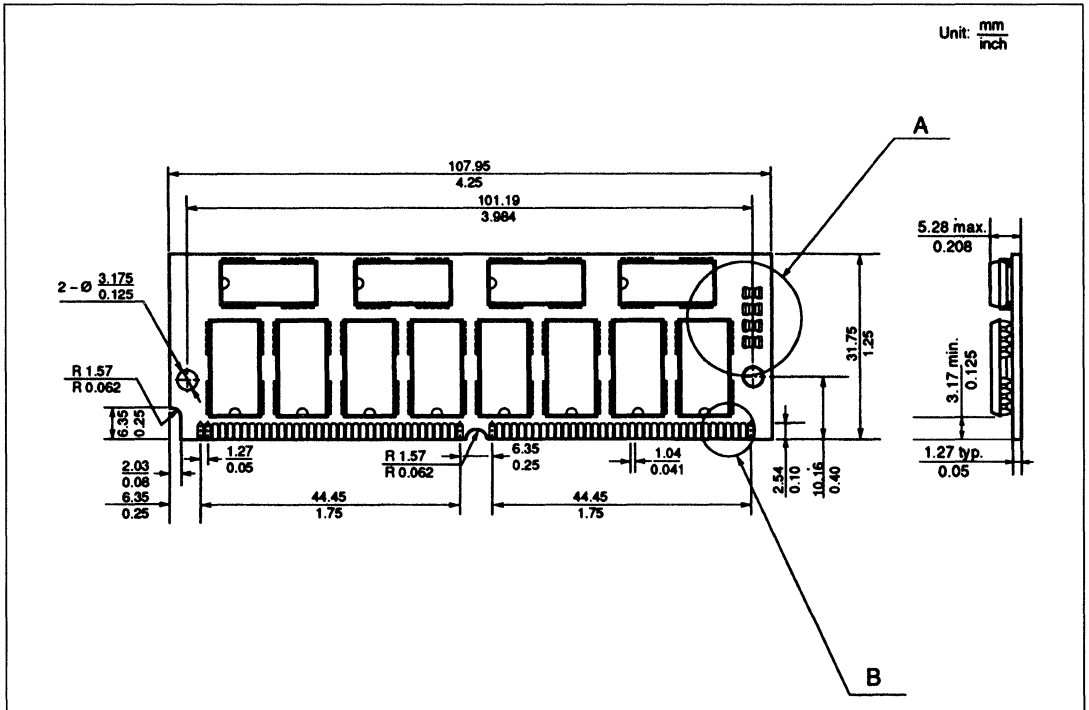
■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_9	Refresh Address Input
DQ_0–DQ_{35}	Data-in/Data-out
$\overline{CAS}_0$–$\overline{CAS}_3$	Column Address Strobe
$\overline{RAS}_0$, $\overline{RAS}_2$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
PD_1–PD_4	Presence Detect Pin
NC	Non-Connection

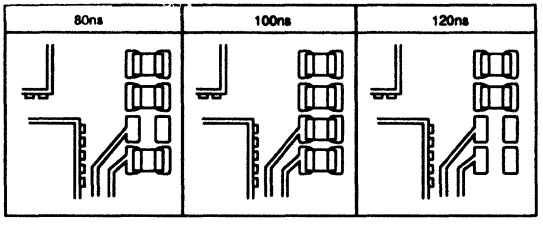
■ BLOCK DIAGRAM



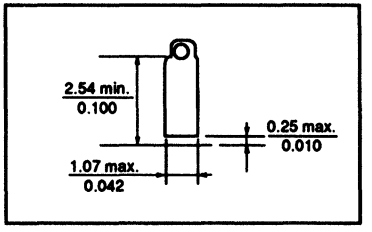
■ PHYSICAL OUTLINE



Detail A



Detail B



Note: The plating of the contact finger is gold.

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input)	V_{in}	− 1.0 to + 7.0	V
	(Output)	V_{out}	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	12	W
Operating Temperature		T_{opr}	0 to + 70	°C
Storage Temperature		T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)

Parameter	Symbol	HB56D136B-8		HB56D136B-10		HB56D136B-12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	1000	—	880	—	760	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	24	—	24	—	24	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	12	—	12	—	12	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	960	—	840	—	740	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	60	—	60	—	60	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	960	—	840	—	720	mA	t_{RC} = Min	
Page Mode Current	I_{CC7}	—	920	—	840	—	720	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	88	pF	1
Input Capacitance ($\overline{WE}$)	C_{I2}	—	104	pF	1
Input Capacitance ($\overline{RAS}$)	C_{I3}	—	57	pF	1
Input Capacitance ($\overline{CAS}$)	C_{I4}	—	36	pF	1
Output Capacitance (DQ_{0-7}, DQ_{9-16}, DQ_{18-25}, DQ_{27-34})	$C_{I/O1}$	—	17	pF	1, 2
Output Capacitance ($DQ_{8, 17, 26, 35}$)	$C_{I/O2}$	—	22	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)[1, 12]

Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56D136B-8		HB56D136B-10		HB56D136B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	45	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	15

Read Cycle

Parameter	Symbol	HB56D136B-8		HB56D136B-10		HB56D136B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	ns	6

Write Cycle

Parameter	Symbol	HB56D136B-8		HB56D136B-10		HB56D136B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	20	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	20	—	20	—	25	—	ns	11

Refresh Cycle

Parameter	Symbol	HB56D136B-8		HB56D136B-10		HB56D136B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	15	—	15	—	15	—	ns	

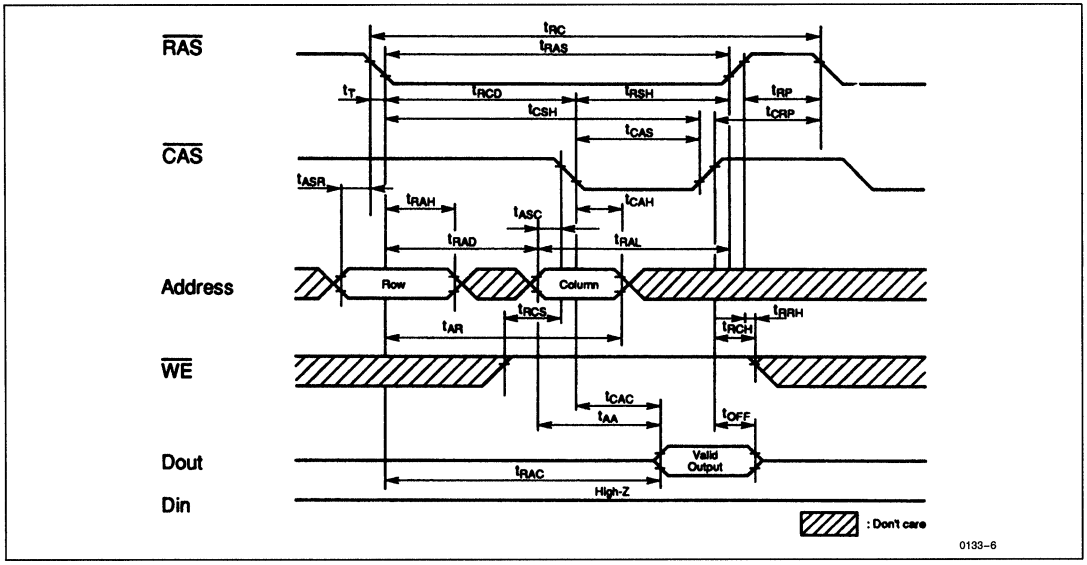
Fast Page Mode Cycle

Parameter	Symbol	HB56D136B-8		HB56D136B-10		HB56D136B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	20	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	80	100000	100	100000	120	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	

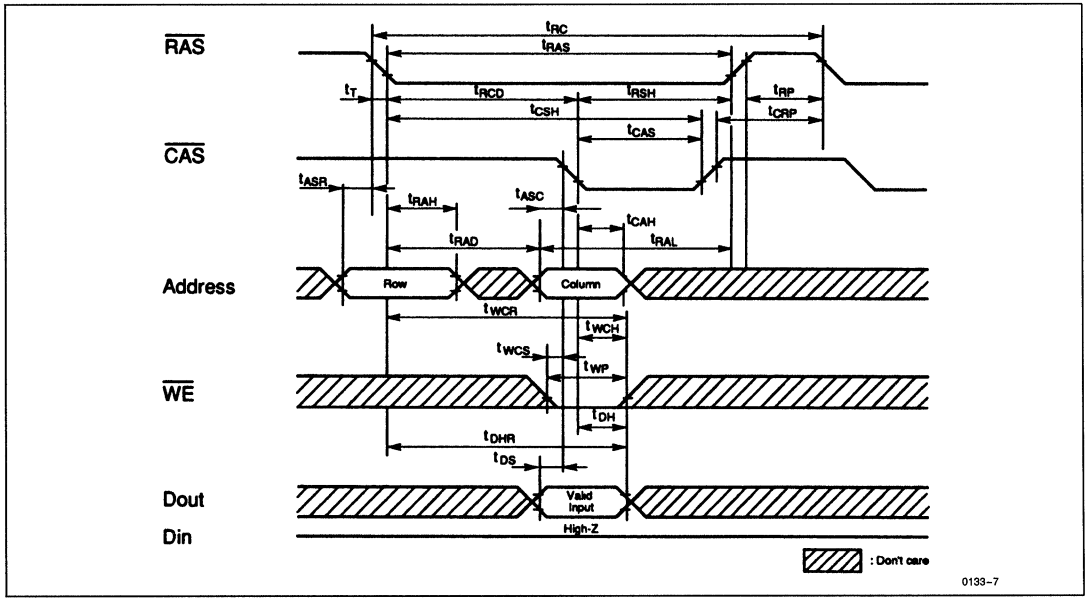
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh).
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is 1,024 refresh cycles.

■ TIMING WAVEFORMS

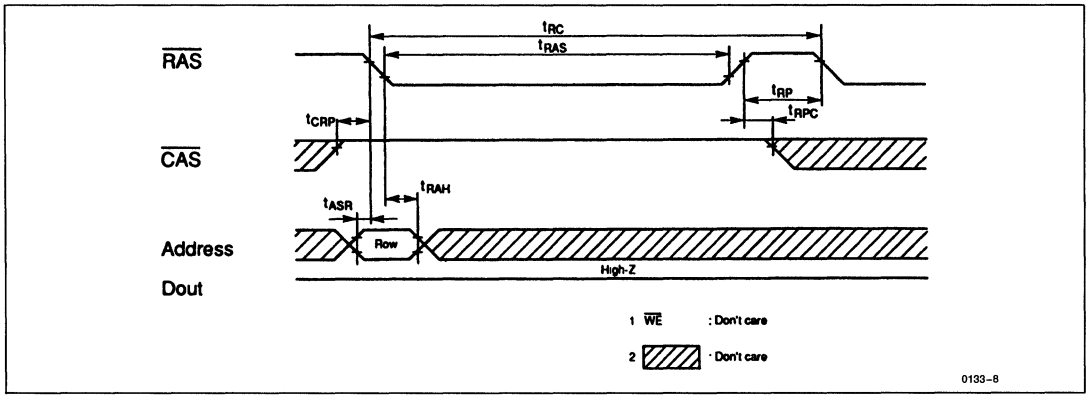
• Read Cycle



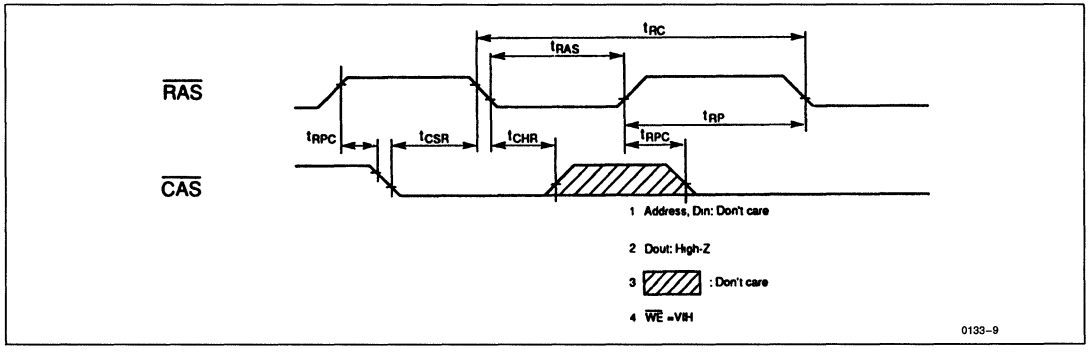
• Early Write Cycle



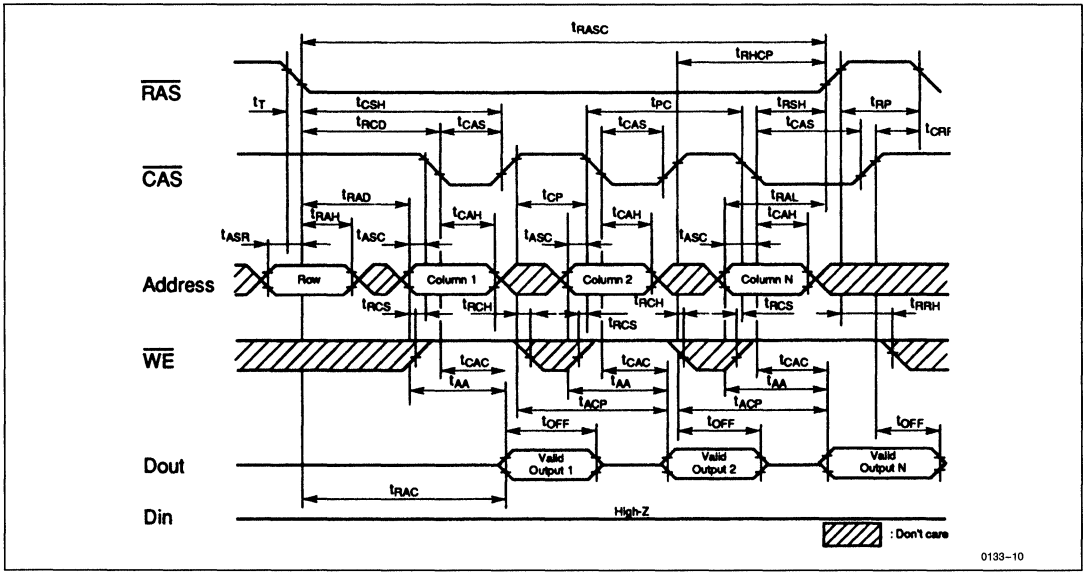
• $\overline{RAS}$ Only Refresh Cycle



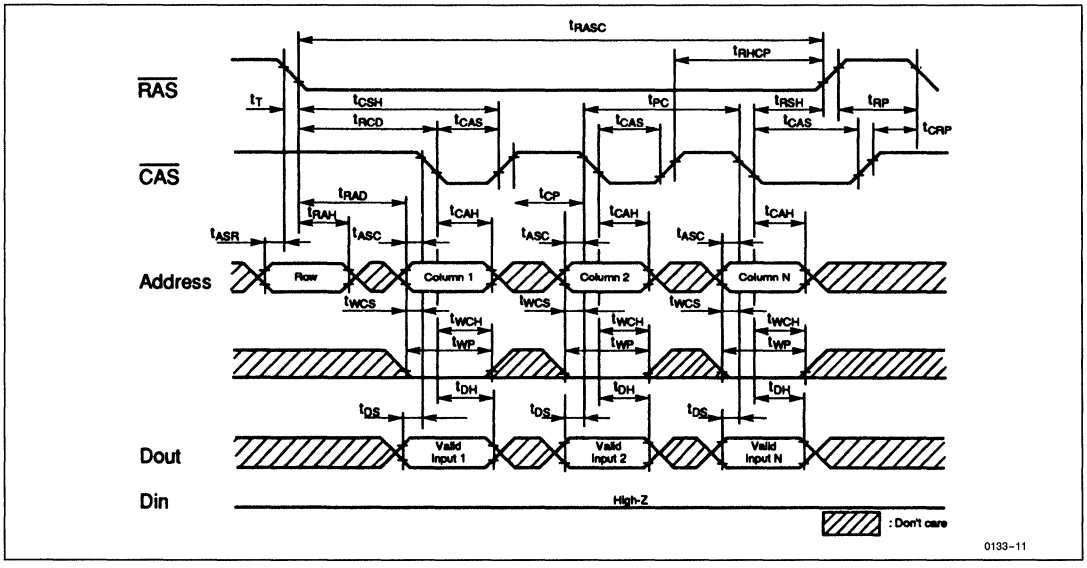
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



HB56D136B/S Series

1,048,576-Word x 36-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56D136B/SB/BR/SBR/BS/SBS is a 1M x 36 dynamic RAM module, mounted 8 pieces of 4 Mbit DRAM (HM514400JP/AJ) sealed in SOJ package and 4 pieces of 1 Mbit DRAM (HM511000JP) sealed in SOJ package (HB56D136B/SB/BR/SBR) or 4 pieces of 1 Mbit DRAM (HM511000ATS) sealed in TSOP package (HB56D136SB/SBS). An outline of the HB56D136B/SB/BR/SBR/BS/SBS is 72-pin single in-line package. Therefore, the HB56D136B/SB/BR/SBR/BS/SBS makes high density mounting possible without surface mount technology. The HB56D136B/SB/BR/SBR/BS/SBS provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ or beside each TSOP but only on the one side of its module board.

■ FEATURES

- 72-pin Single In-line Package
  - Lead Pitch .....1.27 mm
- Single 5V (±5%) Supply
- High Speed
  - Access Time .....60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode .....6.51W/5.88W/5.25W/4.62W (max)
  - Standby Mode .....126 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycle .....(16 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

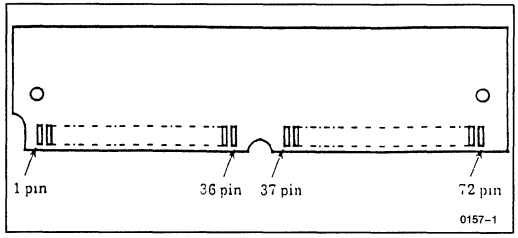
■ ORDERING INFORMATION

Part No.	Access Time	Package	Contact Pad
HB56D136B/BR/BS-6A	60 ns	72-pin SIP Socket Type	Gold
HB56D136B/BR/BS-7A	70 ns		
HB56D136B/BR/BS-8A	80 ns		
HB56D136B/BR/BS-10A	100 ns		
HB56D136B/BR-8	80 ns		
HB56D136B/BR-10	100 ns		
HB56D136SB/SBR/SBS-6A	60 ns	72-pin SIP Socket Type	Solder
HB56D136SB/SBR/SBS-7A	70 ns		
HB56D136SB/SBR/SBS-8A	80 ns		
HB56D136SB/SBR/SBS-10A	100 ns		
HB56D136SB/SBR-8	80 ns		
HB56D136SB/SBR-10	100 ns		

■ PRESENCE DETECT PINOUT

Pin No.	Pin Name	HB56D136B/SB/BR/SBR/BS/SBS					
		-6A	-7A	-8A	-10A	-8	-10
67	PD_1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
68	PD_2	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
69	PD_3	NC	V_{SS}	NC	V_{SS}	NC	V_{SS}
70	PD_4	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}

■ PIN OUT

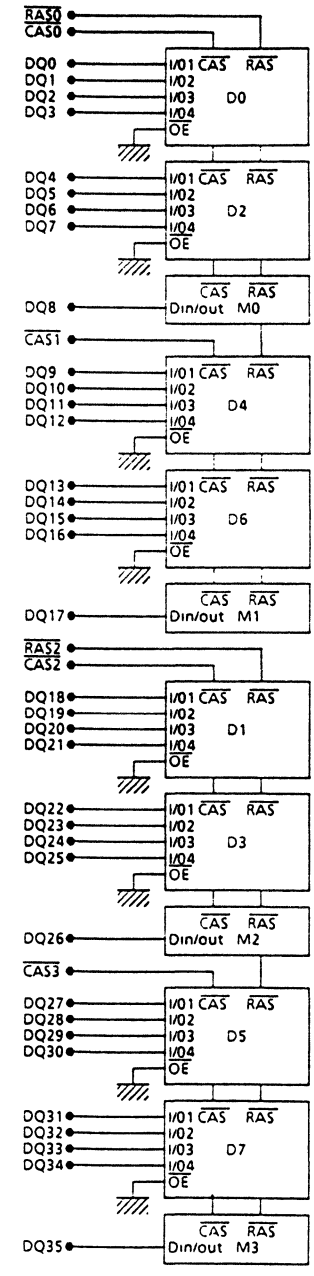


Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	NC	37	DQ_{17}	55	DQ_{12}
2	DQ_0	20	DQ_4	38	DQ_{35}	56	DQ_{30}
3	DQ_{18}	21	DQ_{22}	39	V_{SS}	57	DQ_{13}
4	DQ_1	22	DQ_5	40	$\overline{CAS0}$	58	DQ_{31}
5	DQ_{19}	23	DQ_{23}	41	$\overline{CAS2}$	59	V_{CC}
6	DQ_2	24	DQ_6	42	$\overline{CAS3}$	60	DQ_{32}
7	DQ_{20}	25	DQ_{24}	43	$\overline{CAS1}$	61	DQ_{14}
8	DQ_3	26	DQ_7	44	$\overline{RAS0}$	62	DQ_{33}
9	DQ_{19}	27	DQ_{25}	45	NC	63	DQ_{15}
10	V_{CC}	28	A_7	46	NC	64	DQ_{34}
11	NC	29	NC	47	$\overline{WE}$	65	DQ_{16}
12	A_0	30	V_{CC}	48	NC	66	NC
13	A_1	31	A_8	49	DQ_9	67	PD_1
14	A_2	32	A_9	50	DQ_{27}	68	PD_2
15	A_3	33	NC	51	DQ_{10}	69	PD_3
16	A_4	34	$\overline{RAS2}$	52	DQ_{28}	70	PD_4
17	A_5	35	DQ_{26}	53	DQ_{11}	71	NC
18	A_6	36	DQ_8	54	DQ_{29}	72	V_{SS}

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_9	Refresh Address Input
DQ_0–DQ_{35}	Data-in/Data-out
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$–$\overline{RAS3}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power Supply (+ 5V)
V_{SS}	Ground
PD_1–PD_4	Presence Detect Pin
NC	No Connection

■ BLOCK DIAGRAM

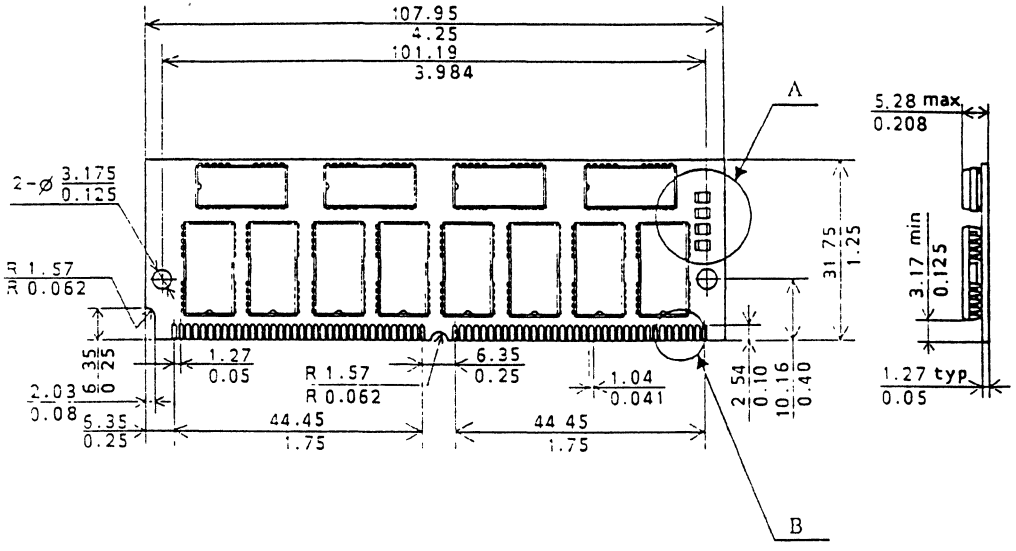


*D0–D7: HM51400JP/AJ
M0–M3: HM511000JP/ATS

■ PHYSICAL OUTLINE

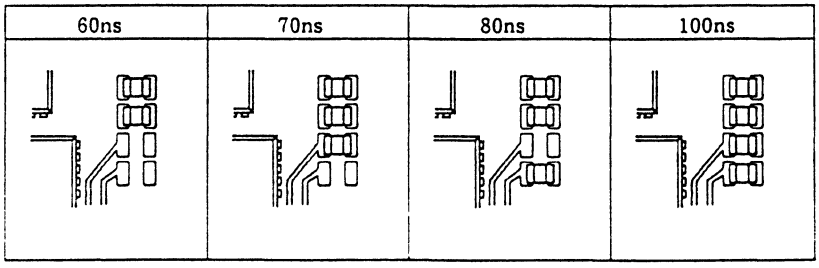
Unit: mm / inch

• HB56D136B/SB

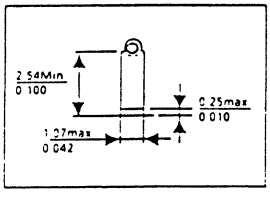


0157-3

Detail A



Detail B



Note: Following the specification of the contact pads.

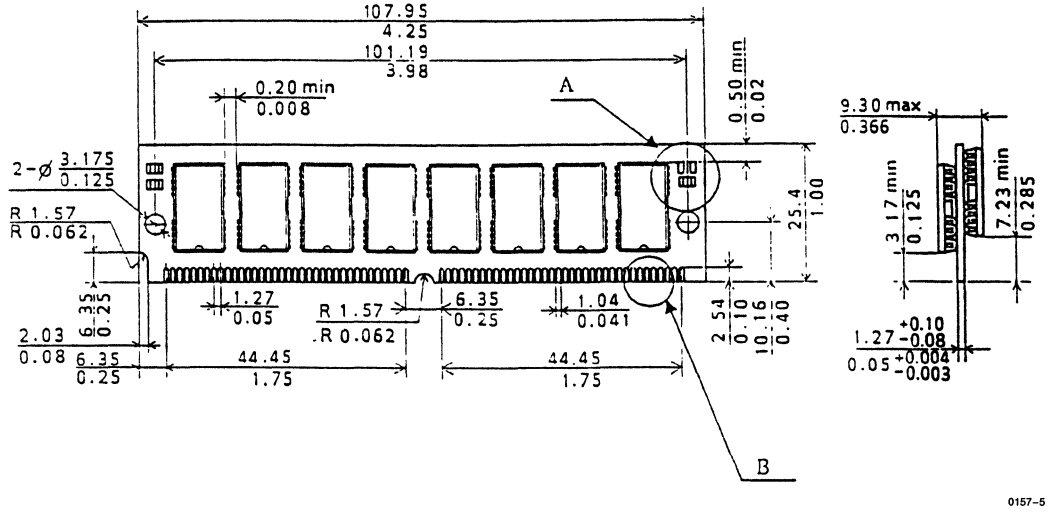
Part No.	Contact Pad
HB56D136B-XX	Gold
HB56D136SB-XX	Solder

0157-4

■ PHYSICAL OUTLINE

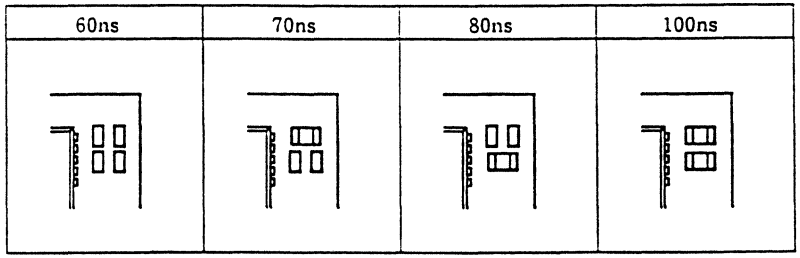
Unit: mm / inch

• HB56D136BR/SBR

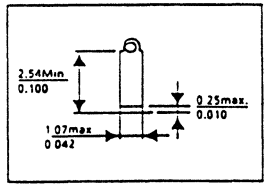


0157-5

Detail A



Detail B



Note: Following the specification of the contact pads.

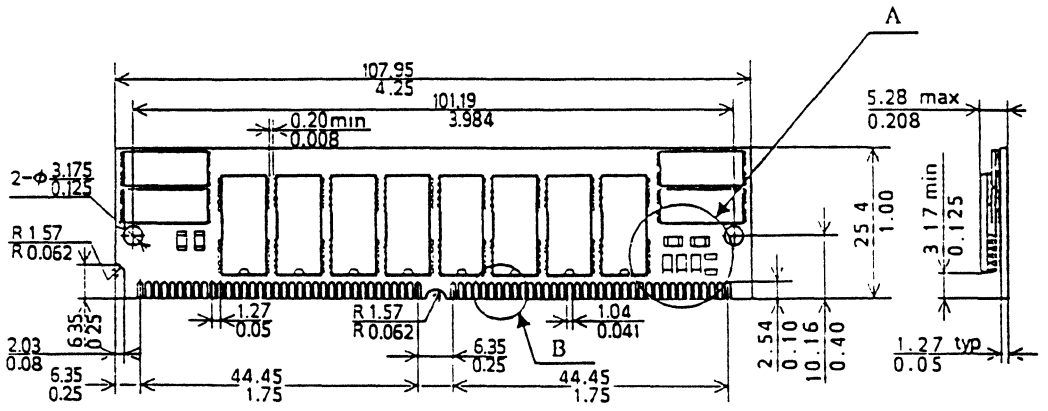
Part No.	Contact Pad
HB56D136BR-XX	Gold
HB56D136SBR-XX	Solder

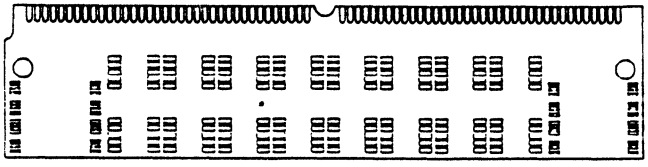
0157-6

■ PHYSICAL OUTLINE

Unit: mm / inch

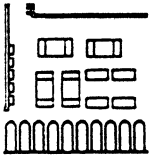
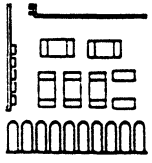
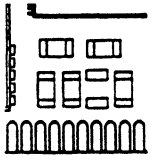
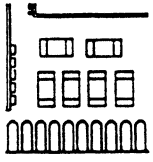
• HB56D136BS/SBS



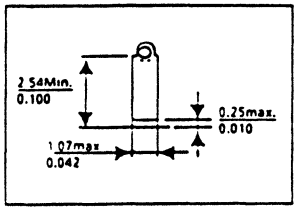


0157-7

Detail A

60ns	70ns	80ns	100ns
			

Detail B



Note: Following the specification of the contact pads.

Part No.	Contact Pad
HB56D136BS-XX	Gold
HB56D136SBS-XX	Solder

0157-8

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input)	V_{in}	−1.0 to +7.0	V
	(Output)	V_{out}	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	8	W
Operating Temperature		T_{opr}	0 to +70	°C
Storage Temperature		T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)

Parameter	Symbol	HB56D136B/SB/BR/SBR/BS/SBS												Unit	Test Conditions	Note
		-6A		-7A		-8A		-10A		-8		-10				
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	1240	—	1120	—	1000	—	880	—	1000	—	880	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	24	—	24	—	24	—	24	—	24	—	24	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	12	—	12	—	12	—	12	—	12	—	12	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	1240	—	1120	—	960	—	840	—	960	—	840	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	60	—	60	—	60	—	60	—	60	—	60	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	1200	—	1080	—	960	—	840	—	960	—	840	mA	t_{RC} = Min	
Page Mode Current	I_{CC7}	—	1200	—	1080	—	920	—	840	—	920	—	840	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	−10	10	−10	10	−10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed ≤ 1 time while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	88	pF	1
Input Capacitance ($\overline{WE}$)	C_{I2}	—	104	pF	1
Input Capacitance ($\overline{RAS}$)	C_{I3}	—	57	pF	1
Input Capacitance ($\overline{CAS}$)	C_{I4}	—	36	pF	1
Output Capacitance (DQ_0–$DQ_{7, 9-16, 18-25, 27-34}$)	$C_{I/O1}$	—	17	pF	1, 2
Output Capacitance ($DQ_{8, 17, 26, 35}$)	$C_{I/O2}$	—	22	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Electrical Characteristics** (T_A = 0 to 70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)[1, 12]

Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56D136B/SB/BR/SBR/BS/SBS												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	120	—	130	—	160	—	190	—	160	—	190	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	50	—	70	—	80	—	70	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	25	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	12	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	20	—	20	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	75	22	55	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	55	17	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	25	—	25	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	—	16	—	16	—	16	ms	15

Read Cycle

Parameter	Symbol	HB56D136B/SB/BR/SBR/BS/SBS												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	25	—	25	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	40	—	45	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	55	—	40	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	—	20	—	20	—	20	—	25	—	20	—	25	ns	6

Write Cycle

Parameter	Symbol	HB56D136B/SB/BR/SBR/BS/SBS												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	20	—	20	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	20	—	15	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	20	—	20	—	20	—	ns	11

Refresh Cycle

Parameter	Symbol	HB56D136B/SB/BR/SBR/BS/SBS												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	15	—	20	—	20	—	20	—	20	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	10	—	ns	

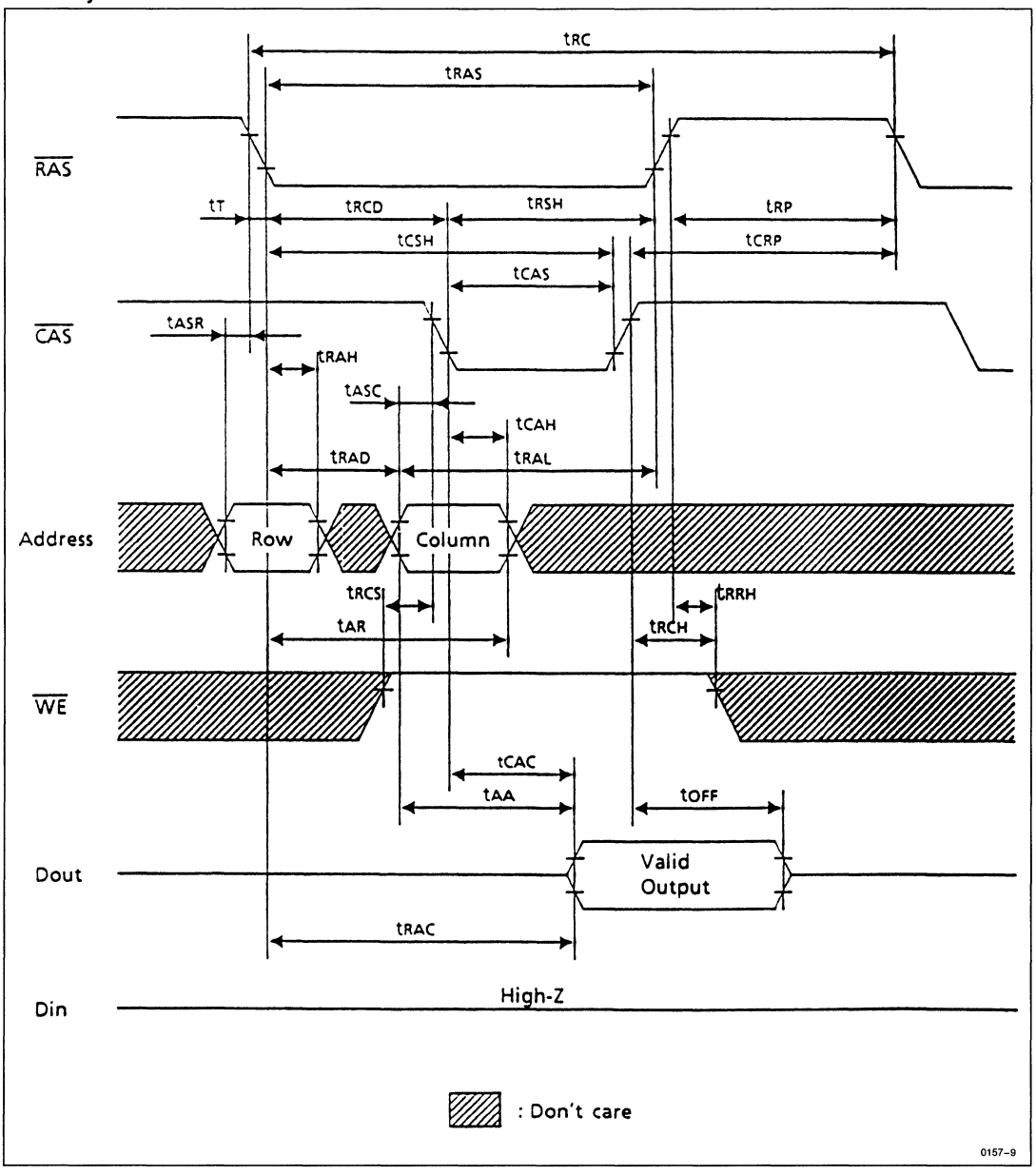
Fast Page Mode Cycle

Parameter	Symbol	HB56D136B/SB/BR/SBR/BS/SBS												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	55	—	55	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	—	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	—	50	—	50	—	50	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	50	—	50	—	50	—	ns	

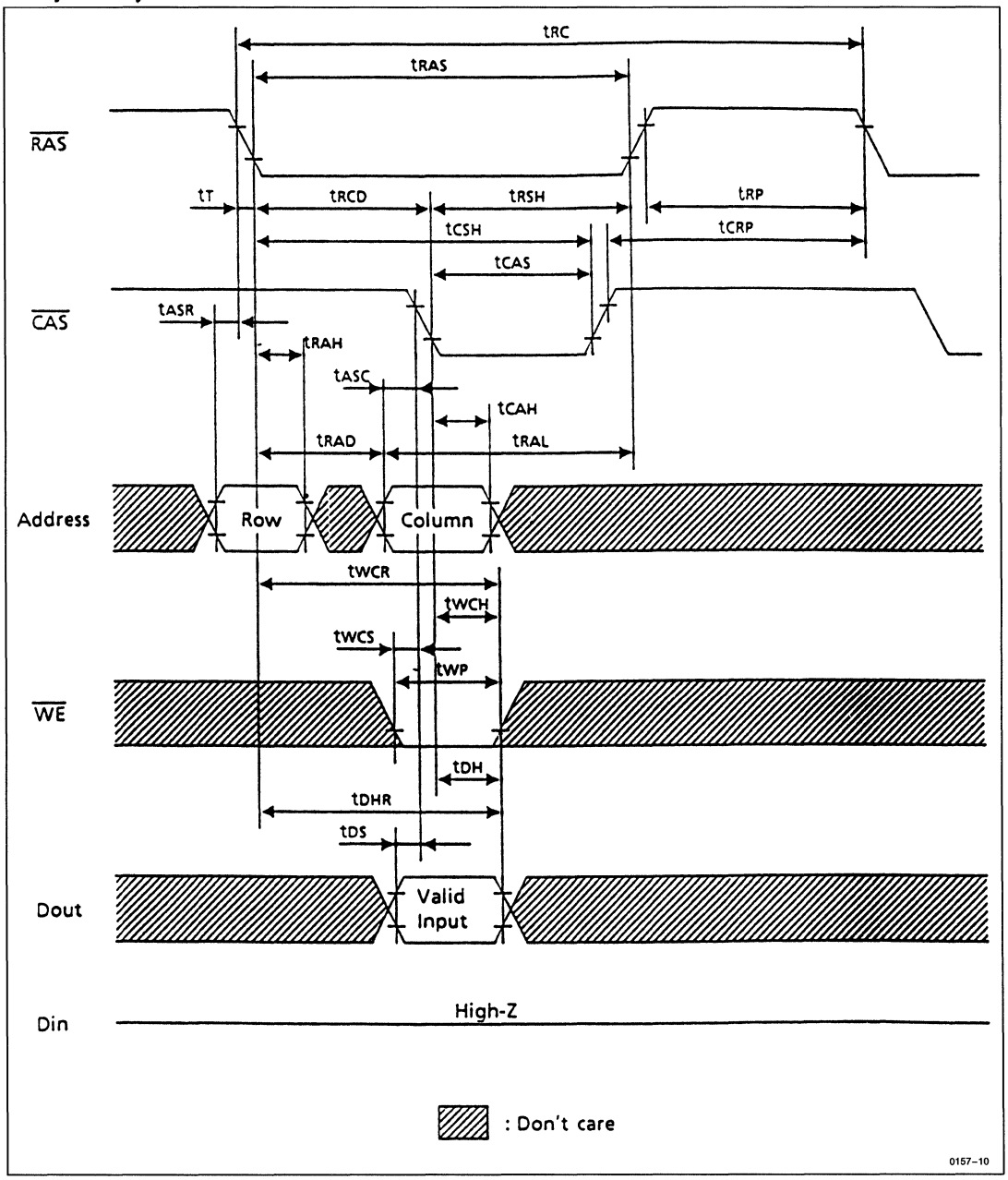
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is determined by 1,024 refresh cycles.

■ TIMING WAVEFORMS

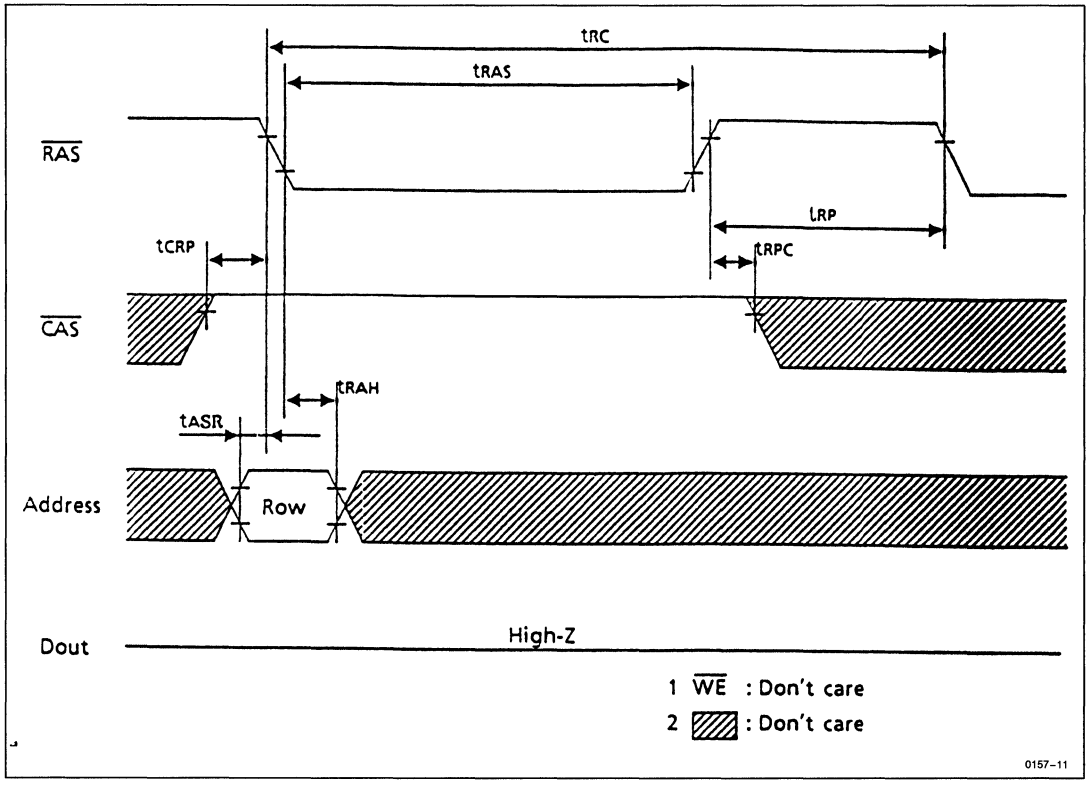
• Read Cycle



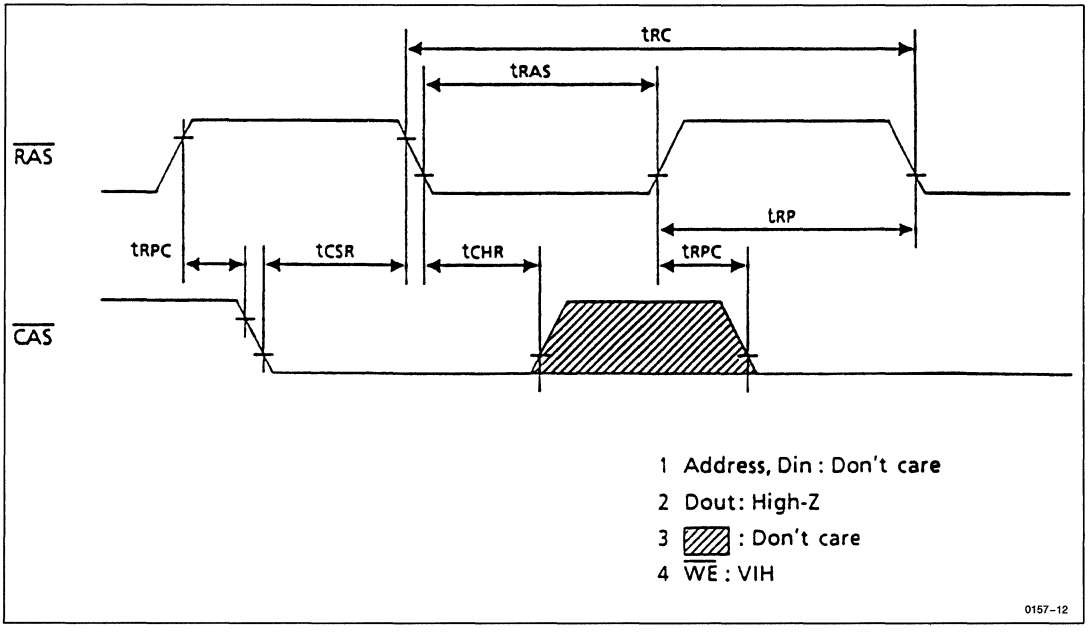
• **Early Write Cycle**



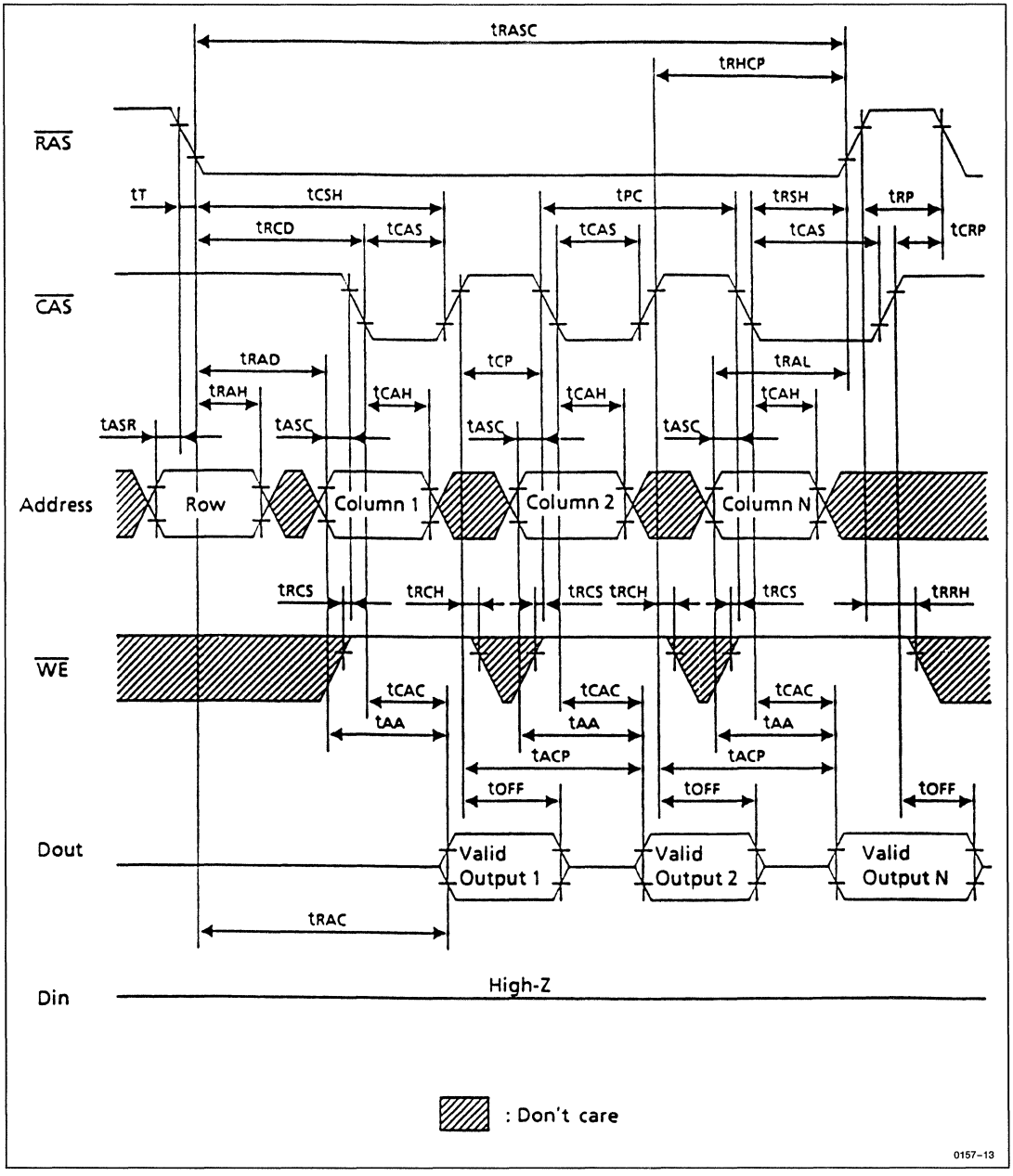
• $\overline{RAS}$ Only Refresh Cycle



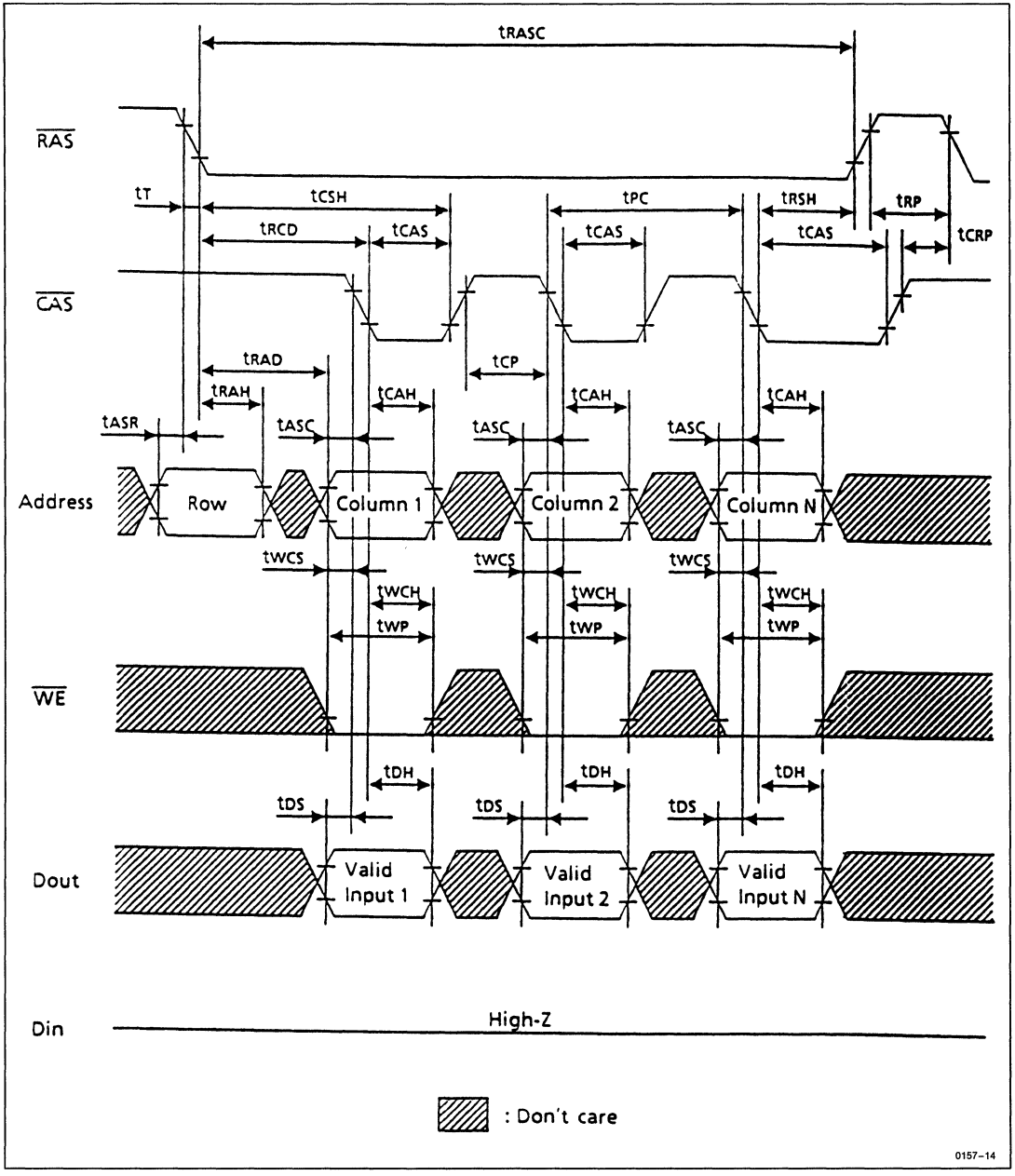
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



HB56D236B Series

2,097,152-Word x 36-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56D236B is a 2M x 36 dynamic RAM module, mounted 16 pieces of 4 Mbit DRAM (HM514400JP) sealed in SOJ package and 8 pieces of 1 Mbit DRAM (HM511000AJP) sealed in SOJ package. An outline of the HB56D236B is 72-pin single in-line package. Therefore, the HB56D236B makes high density mounting possible without surface mount technology. The HB56D236B provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ but only on the side of its module board.

■ FEATURES

- 72-pin Single In-line Package
  - Lead Pitch 1.27mm
- Single 5V (±5%) Supply
- High Speed
  - Access Time .....80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode.....5.57 mW/4.94 mW/4.31 mW (max)
  - Standby Mode .....252 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycle .....(16 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

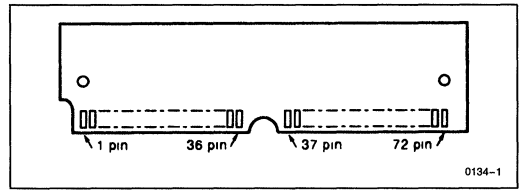
■ ORDERING INFORMATION

Part No.	Access Time	Package
HB56D236B-8	80 ns	72-pin SIP Socket Type
HB56D236B-10	100 ns	
HB56D236B-12	120 ns	

■ PRESENCE DETECT PIN OUT

Pin No.	Pin Name	HB56D236B		
		80 ns	100 ns	120 ns
67	PD_1	NC	NC	NC
68	PD_2	NC	NC	NC
69	PD_3	NC	V_{SS}	NC
70	PD_4	V_{SS}	V_{SS}	NC

■ PIN OUT

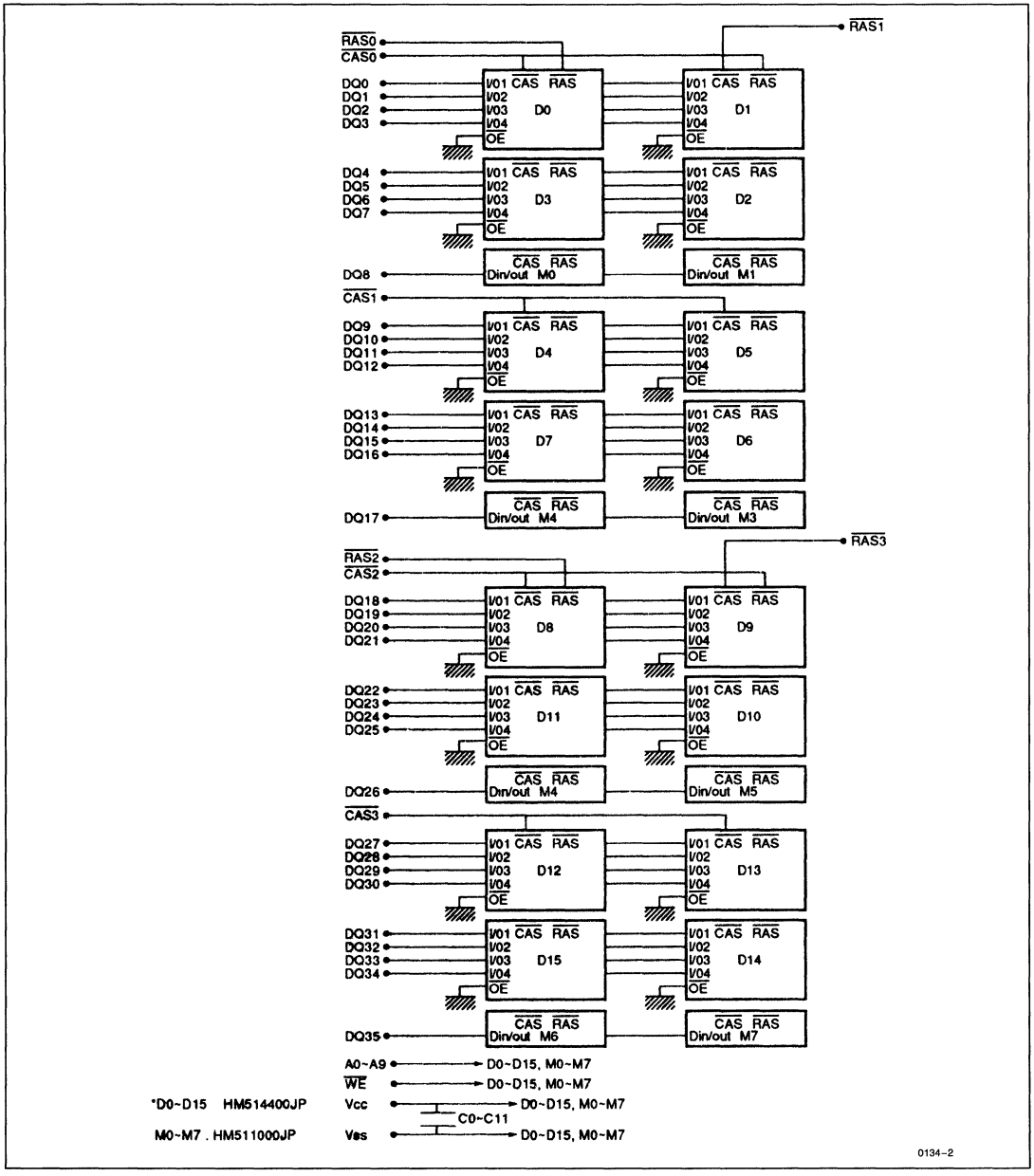


Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	NC	37	DQ_{17}	55	DQ_{12}
2	DQ_0	20	DQ_4	38	DQ_{35}	56	DQ_{30}
3	DQ_{18}	21	DQ_{22}	39	V_{SS}	57	DQ_{13}
4	DQ_1	22	DQ_5	40	$\overline{CAS_0}$	58	DQ_{31}
5	DQ_{19}	23	DQ_{23}	41	$\overline{CAS_2}$	59	V_{CC}
6	DQ_2	24	DQ_6	42	$\overline{CAS_3}$	60	DQ_{32}
7	DQ_{20}	25	DQ_{24}	43	$\overline{CAS_1}$	61	DQ_{14}
8	DQ_3	26	DQ_7	44	$\overline{RAS_0}$	62	DQ_{33}
9	DQ_{21}	27	DQ_{25}	45	$\overline{RAS_1}$	63	DQ_{15}
10	V_{CC}	28	A_7	46	NC	64	DQ_{34}
11	NC	29	NC	47	$\overline{WE}$	65	DQ_{16}
12	A_0	30	V_{CC}	48	NC	66	NC
13	A_1	31	A_8	49	DQ_9	67	PD_1
14	A_2	32	A_9	50	DQ_{27}	68	PD_2
15	A_3	33	$\overline{RAS_3}$	51	DQ_{10}	69	PD_3
16	A_4	34	$\overline{RAS_2}$	52	DQ_{28}	70	PD_4
17	A_5	35	DQ_{26}	53	DQ_{11}	71	NC
18	A_6	36	DQ_8	54	DQ_{29}	72	V_{SS}

■ PIN DESCRIPTION

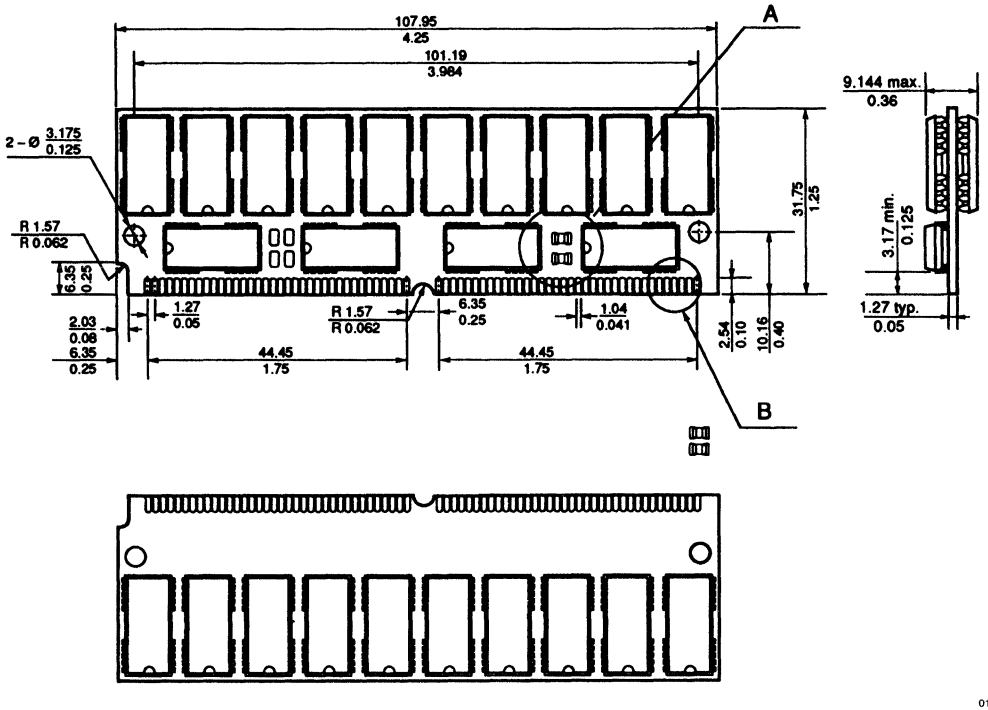
Pin Name	Function
A_0–A_9	Address Input
A_0–A_9	Refresh Address Input
DQ_0–DQ_{35}	Data-in/Data-out
$\overline{CAS_0}$–$\overline{CAS_3}$	Column Address Strobe
$\overline{RAS_0}$–$\overline{RAS_3}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power (+ 5V)
V_{SS}	Ground
PD_1–PD_4	Presence Detect Pin
NC	Non-Connection

■ BLOCK DIAGRAM

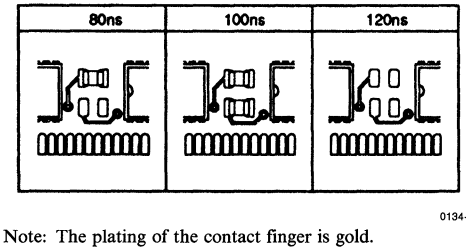


■ PHYSICAL OUTLINES

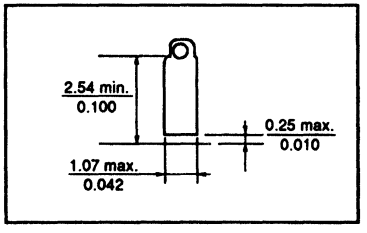
Unit: mm / inch



Detail A



Detail B



Note: The plating of the contact finger is gold.

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input)	V_{in}	−1.0 to +7.0	V
	(Output)	V_{out}	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	12	W
Operating Temperature		T_{opr}	0 to +70	°C
Storage Temperature		T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltages referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)

Parameter	Symbol	HB56D236B-8		HB56D236B-10		HB56D236B-12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	1060	—	940	—	820	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	48	—	48	—	48	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	24	—	24	—	24	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	1020	—	900	—	800	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	120	—	120	—	120	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	1020	—	900	—	780	mA	t_{RC} = Min	
Page Mode Current	I_{CC7}	—	980	—	900	—	780	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	μA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	161	pF	1
Input Capacitance ($\overline{WE}$)	C_{I2}	—	193	pF	1
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I3}	—	62	pF	1
Output Capacitance (DQ_{0-7}, DQ_{9-16}, DQ_{18-25}, DQ_{27-34})	$C_{I/O1}$	—	29	pF	1, 2
Output ($DQ_{8, 17, 26, 35}$)	$C_{I/O2}$	—	39	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)[1, 12]

Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56D236B-8		HB56D236B-10		HB56D236B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	45	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	15

Read Cycle

Parameter	Symbol	HB56D236B-8		HB56D236B-10		HB56D236B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	ns	6

Write Cycle

Parameter	Symbol	HB56D236B-8		HB56D236B-10		HB56D236B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	20	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	20	—	20	—	25	—	ns	11

Refresh Cycle

Parameter	Symbol	HB56D236B-8		HB56D236B-10		HB56D236B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	15	—	15	—	15	—	ns	

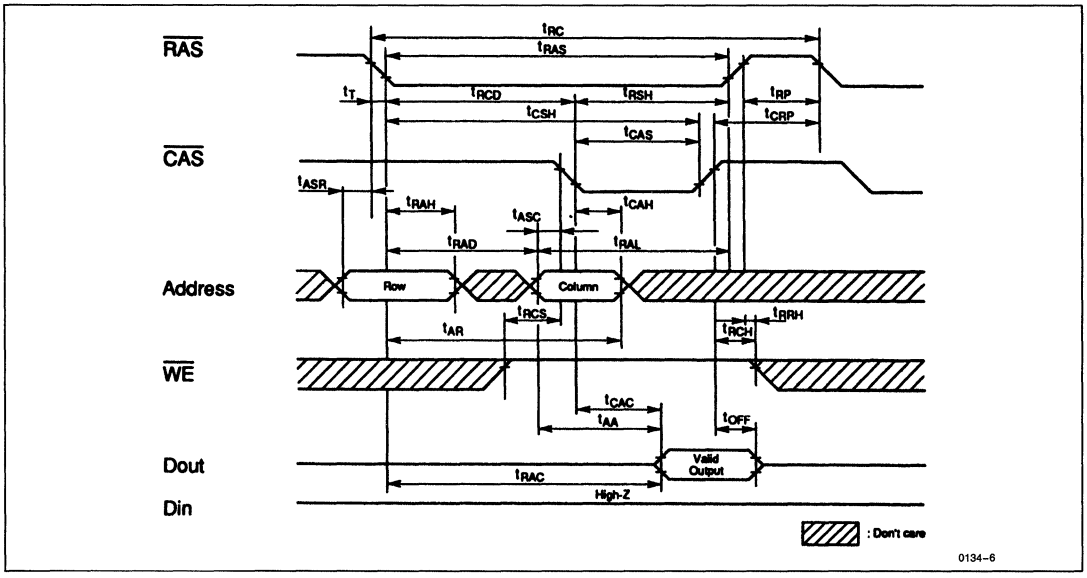
Fast Page Mode Cycle

Parameter	Symbol	HB56D236B-8		HB56D236B-10		HB56D236B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	20	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	80	100000	100	100000	120	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	60	—	ns	

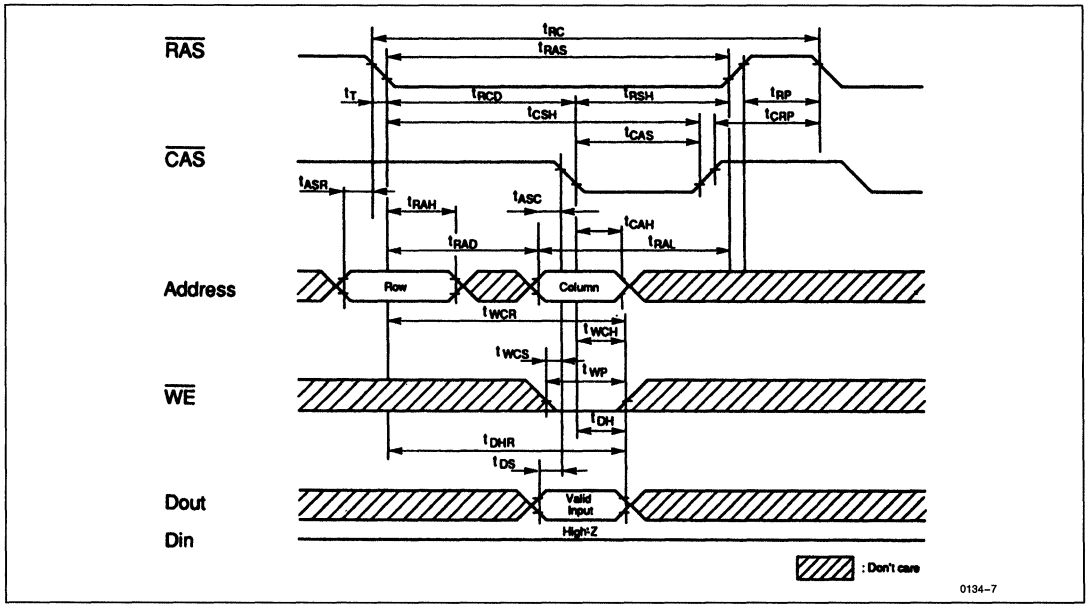
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh).
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} defines is 1,024 refresh cycles.

■ TIMING WAVEFORMS

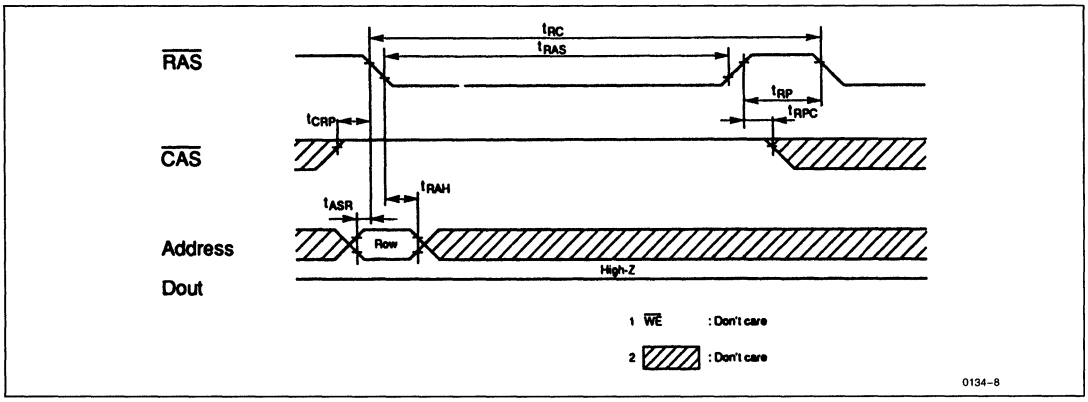
• Read Cycle



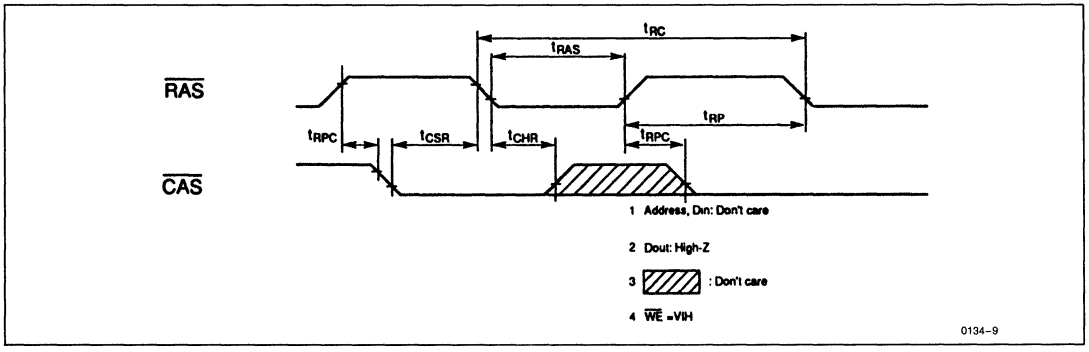
• Early Write Cycle



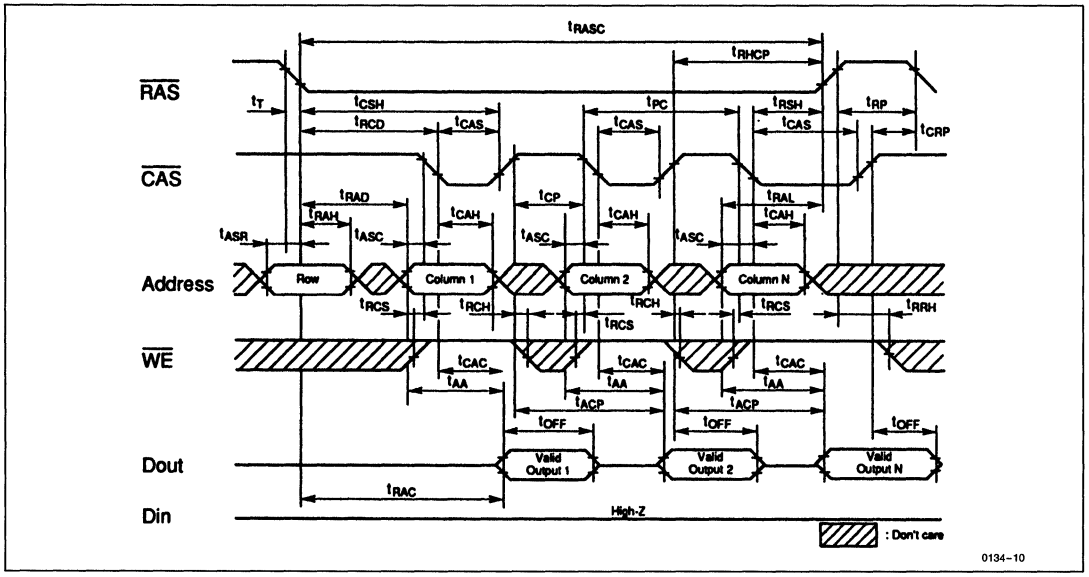
• $\overline{RAS}$ Only Refresh Cycle



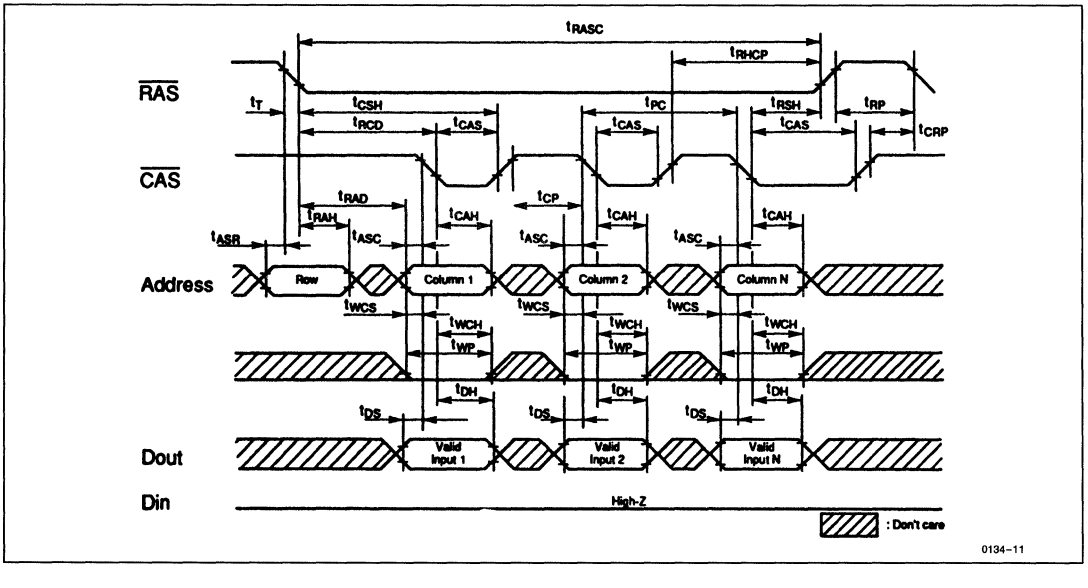
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



HB56D236B/SB Series

2,097,152-Word x 36-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56D236B/SB/BS/SBS is a 2M x 36 dynamic RAM module, mounted 16 pieces of 4 Mbit DRAM (HM514400JP/AJ) sealed in SOJ package and 8 pieces of 1 Mbit DRAM (HM511000JP) sealed in SOJ package (HB56D236B/SB or 8 pieces of 1 Mbit DRAM (HM511000ATS) sealed in TSOP package (HB56D236SB/SBS). An outline of the HB56D236B/SB/BS/SBS is 72-pin single in-line package. Therefore, the HB56D236B/SB/BS/SBS makes high density mounting possible without surface mount technology. The HB56D236B/SB/BS/SBS provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ or beside each TSOP but only on the one side of its module board.

■ FEATURES

- 72-pin Single In-line Package
  - Lead Pitch ..... 1.27 mm
- Single 5V (±5%) Supply
- High Speed
  - Access Time ..... 60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Active Mode . 6.825W/6.195W/5.565W/4.935W (max)
  - Standby Mode ..... 252 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycle ..... (16 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

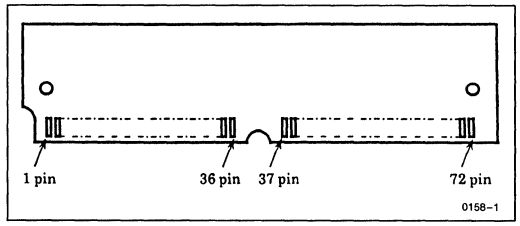
■ ORDERING INFORMATION

Part No.	Access Time	Package	Contact Pad
HB56D236B/BS-6A	60 ns	72-pin SIP Socket Type	Gold
HB56D236B/BS-7A	70 ns		
HB56D236B/BS-8A	80 ns		
HB56D236B/BS-10A	100 ns		
HB56D236B-8	80 ns		
HB56D236B-10	100 ns		
HB56D236SB/SBS-6A	60 ns	72-pin SIP Socket Type	Solder
HB56D236SB/SBS-7A	70 ns		
HB56D236SB/SBS-8A	80 ns		
HB56D236SB/SBS-10A	100 ns		
HB56D236SB-8	80 ns		
HB56D236SB-10	100 ns		

■ PRESENCE DETECT PINOUT

Pin No.	Pin Name	HB56D236B/SB/BS/SBS					
		-6A	-7A	-8A	-10A	-8	-10
67	PD1	NC	NC	NC	NC	NC	NC
68	PD2	NC	NC	NC	NC	NC	NC
69	PD3	NC	V_{SS}	NC	V_{SS}	NC	V_{SS}
70	PD4	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}

■ PIN OUT

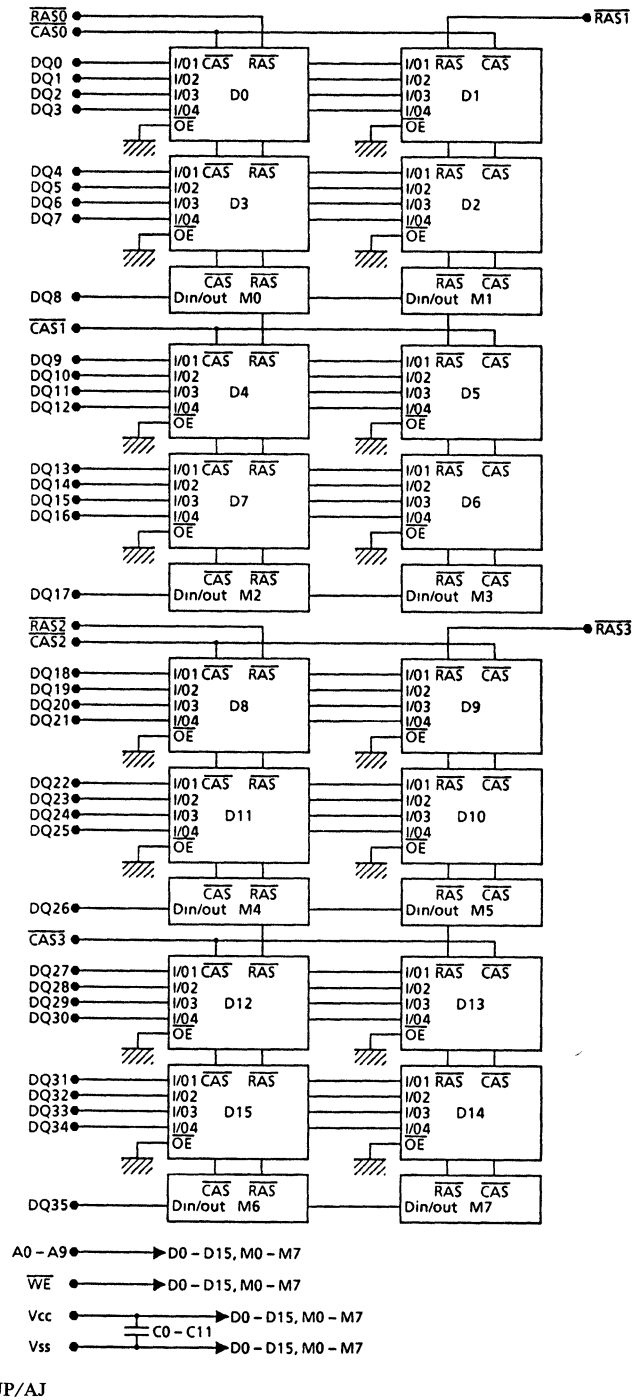


Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	NC	37	DQ_{17}	55	DQ_{12}
2	DQ_0	20	DQ_4	38	DQ_{35}	56	DQ_{30}
3	DQ_{18}	21	DQ_{22}	39	V_{SS}	57	DQ_{13}
4	DQ_1	22	DQ_5	40	$\overline{CAS0}$	58	DQ_{31}
5	DQ_{19}	23	DQ_{23}	41	$\overline{CAS2}$	59	V_{CC}
6	DQ_2	24	DQ_6	42	$\overline{CAS3}$	60	DQ_{32}
7	DQ_{20}	25	DQ_{24}	43	$\overline{CAS1}$	61	DQ_{14}
8	DQ_3	26	DQ_7	44	$\overline{RAS0}$	62	DQ_{33}
9	DQ_{21}	27	DQ_{25}	45	$\overline{RAS1}$	63	DQ_{15}
10	V_{CC}	28	A_7	46	NC	64	DQ_{34}
11	NC	29	NC	47	$\overline{WE}$	65	DQ_{16}
12	A_0	30	V_{CC}	48	NC	66	NC
13	A_1	31	A_8	49	DQ_9	67	PD1
14	A_2	32	A_9	50	DQ_{27}	68	PD2
15	A_3	33	$\overline{RAS3}$	51	DQ_{10}	69	PD3
16	A_4	34	$\overline{RAS2}$	52	DQ_{28}	70	PD4
17	A_5	35	DQ_{26}	53	DQ_{11}	71	NC
18	A_6	36	DQ_8	54	DQ_{29}	72	V_{SS}

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_9	Refresh Address Input
DQ_0–DQ_{35}	Data-in/Data-out
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$–$\overline{RAS3}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power Supply (+ 5V)
V_{SS}	Ground
PD_1–PD_4	Presence Detect Pin
NC	No Connection

■ BLOCK DIAGRAM

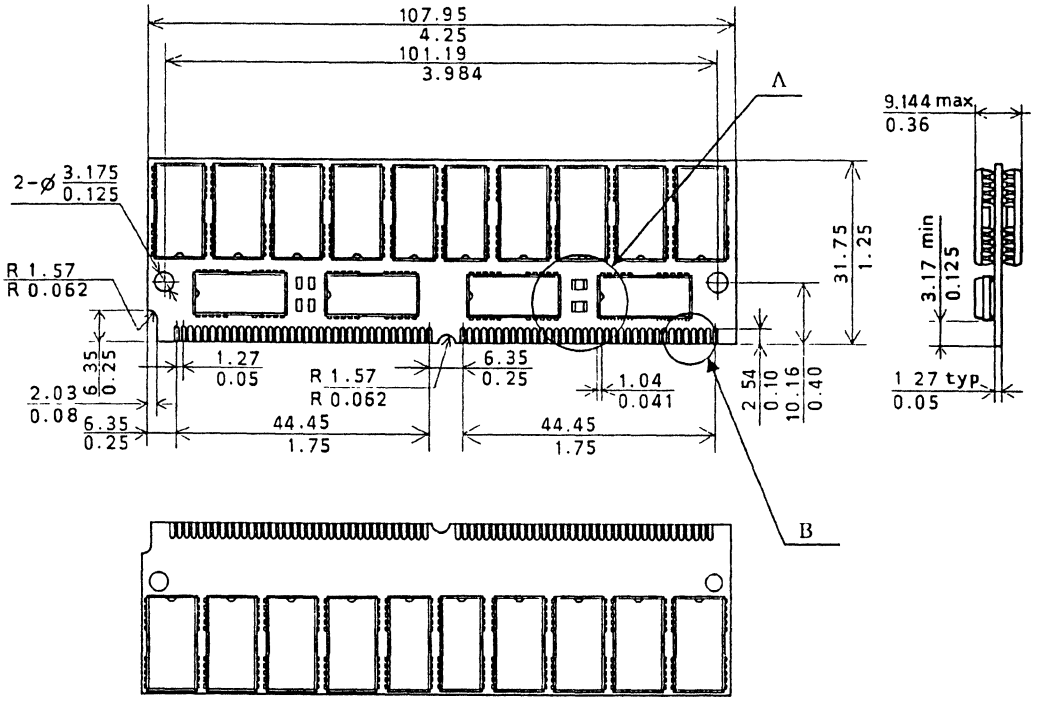


*D0–D15: HM514400JP/AJ
M0–M7: HM511000JP/ATS

■ PHYSICAL OUTLINE

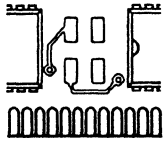
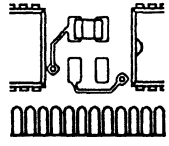
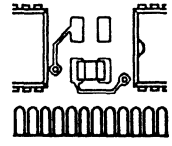
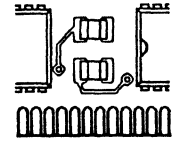
Unit: mm / inch

• **HB56D236B/SB**

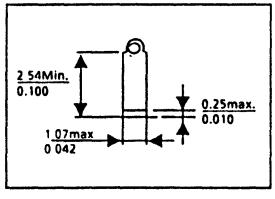


0158-3

Detail A

60ns	70ns	80ns	100ns
			

Detail B



Note: Following the specification of the contact pads.

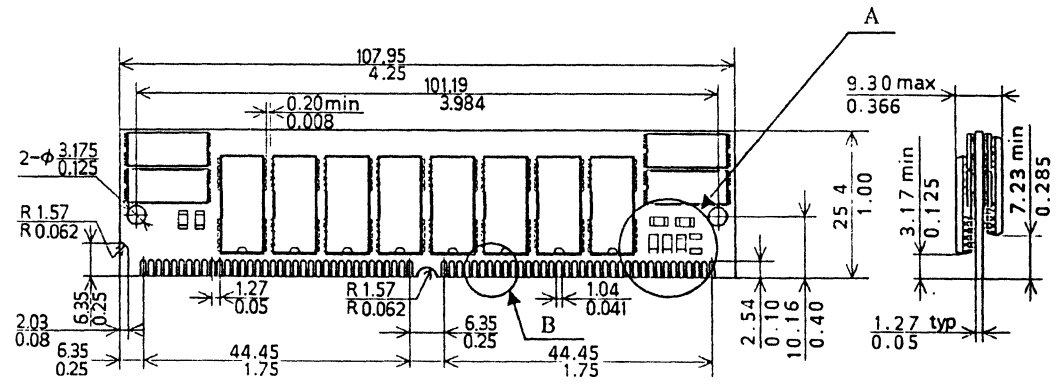
Part No.	Contact Pad
HB56D236B-XX	Gold
HB56D236SB-XX	Solder

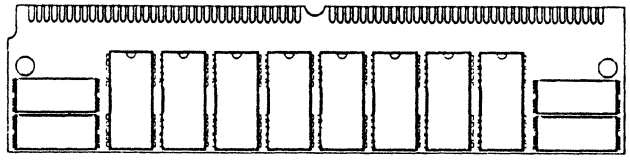
0158-4

■ PHYSICAL OUTLINE (continued)

Unit: mm / inch

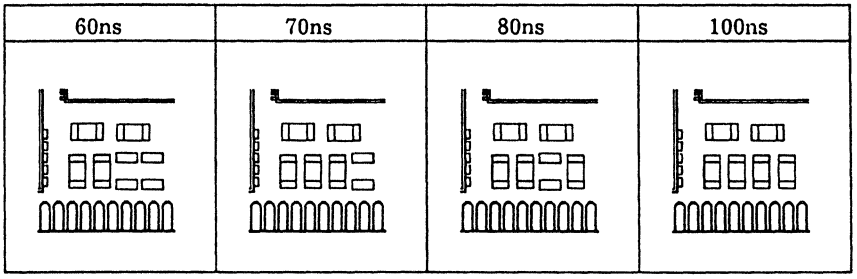
• HB56D236BS/SBS



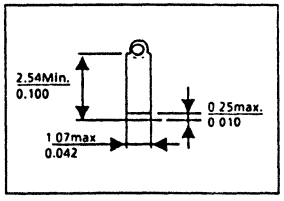


0158-5

Detail A



Detail B



Note: Following the specification of the contact pads.

Part No.	Contact Pad
HB56D236BS-XX	Gold
HB56D236SBS-XX	Solder

0158-6

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input)	V_{in}	− 1.0 to + 7.0	V
	(Output)	V_{out}	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	8	W
Operating Temperature		T_{opr}	0 to + 70	°C
Storage Temperature		T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V)

Parameter	Symbol	HB56D236B/SB/BS/SBS												Unit	Test Conditions	Note
		-6A		-7A		-8A		-10A		-8		-10				
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	1300	—	1180	—	1060	—	940	—	1060	—	940	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	48	—	48	—	48	—	48	—	48	—	48	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	24	—	24	—	24	—	24	—	24	—	24	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	1300	—	1180	—	1020	—	900	—	1020	—	900	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	120	—	120	—	120	—	120	—	120	—	120	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	1260	—	1140	—	1020	—	900	—	1020	—	900	mA	t_{RC} = Min	
Page Mode Current	I_{CC7}	—	1260	—	1140	—	980	—	900	—	980	—	900	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed ≤ 1 time while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	161	pF	1
Input Capacitance ($\overline{WE}$)	C_{I2}	—	193	pF	1
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I3}	—	62	pF	1
Output Capacitance ($DQ_{0-7, 9-16, 18-25, 27-34}$)	$C_{I/O1}$	—	29	pF	1, 2
Output Capacitance ($DQ_{8, 17, 26, 35}$)	$C_{I/O2}$	—	39	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)[1, 12]

Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56D236B/SB/BS/SBS												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	120	—	130	—	160	—	190	—	160	—	190	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	50	—	70	—	80	—	70	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	25	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	12	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	20	—	20	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	75	22	55	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	55	17	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	25	—	25	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	—	16	—	16	—	16	ms	15

Read Cycle

Parameter	Symbol	HB56D236B/SB/BS/SBS												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	80	—	100	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	25	—	25	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	40	—	45	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	55	—	40	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	—	20	—	20	—	20	—	25	—	20	—	25	ns	6

Write Cycle

Parameter	Symbol	HB56D236B/SB/BS/SBS												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	20	—	20	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	20	—	15	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DD}	15	—	15	—	20	—	20	—	20	—	20	—	ns	11

Refresh Cycle

Parameter	Symbol	HB56D236B/SB/BS/SBS												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	15	—	20	—	20	—	20	—	20	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	10	—	ns	

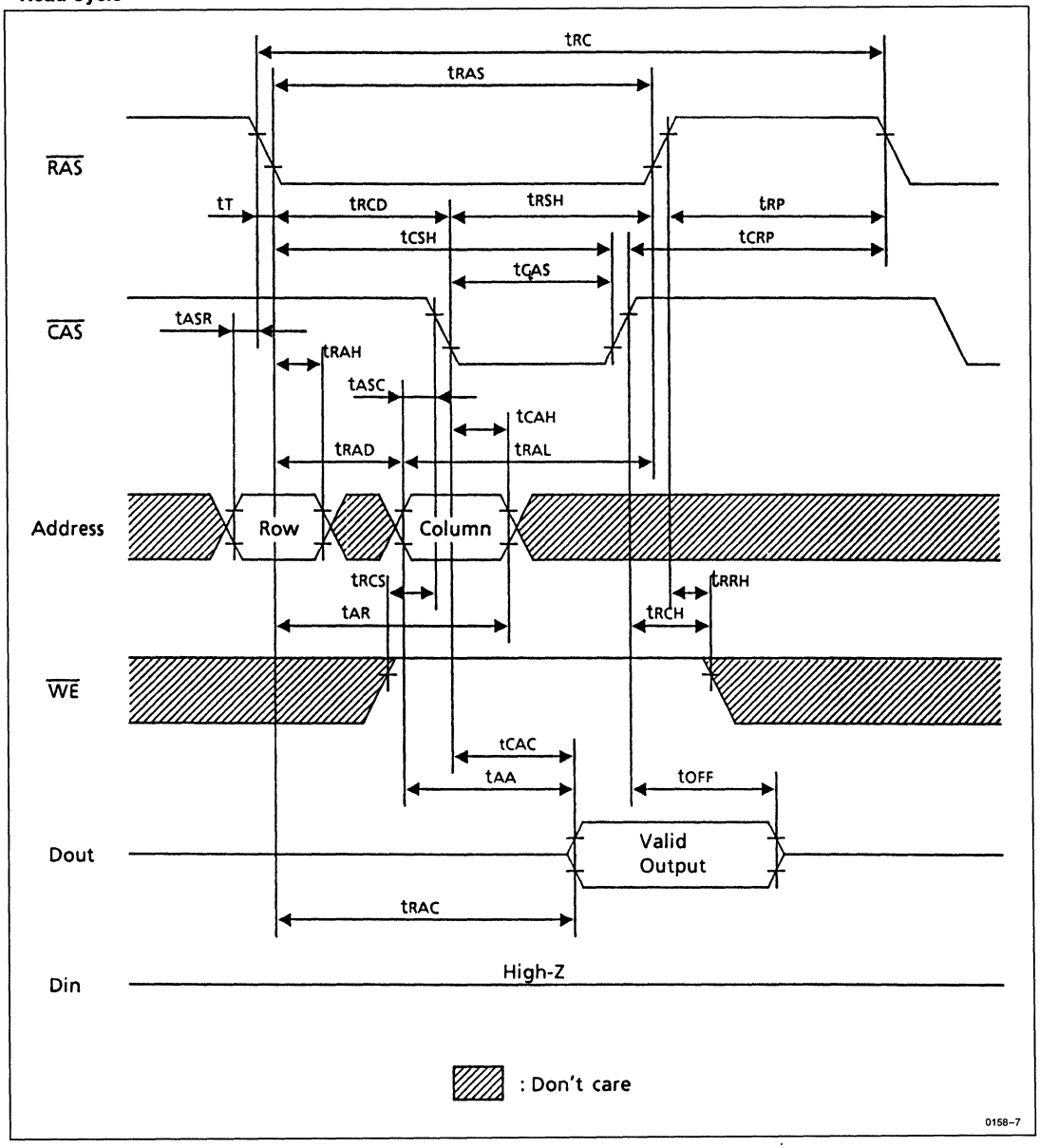
Fast Page Mode Cycle

Parameter	Symbol	HB56D236B/SB/BS/SBS												Unit	Note
		-6A		-7A		-8A		-10A		-8		-10			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	55	—	55	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	—	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	—	50	—	50	—	50	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	50	—	50	—	50	—	ns	

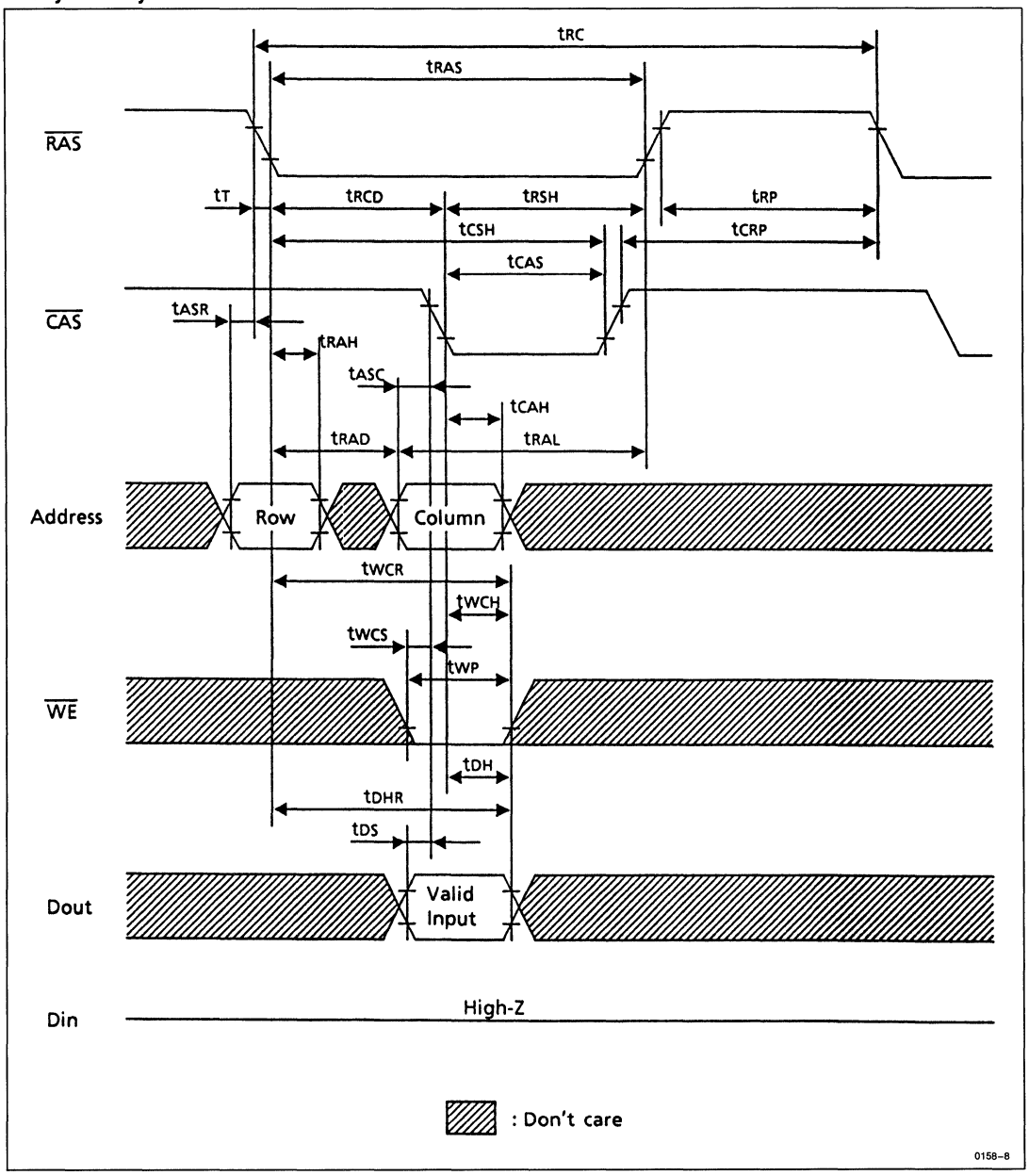
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refrersh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is determined by 1,024 refresh cycles.

■ TIMING WAVEFORMS

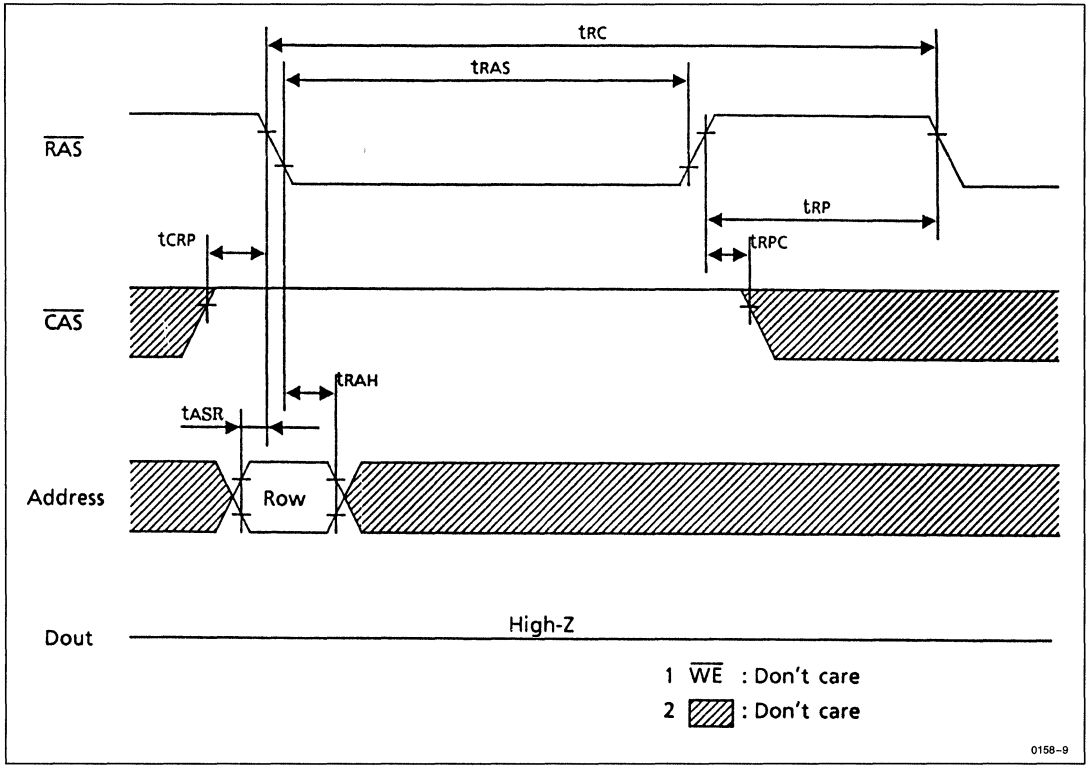
• Read Cycle



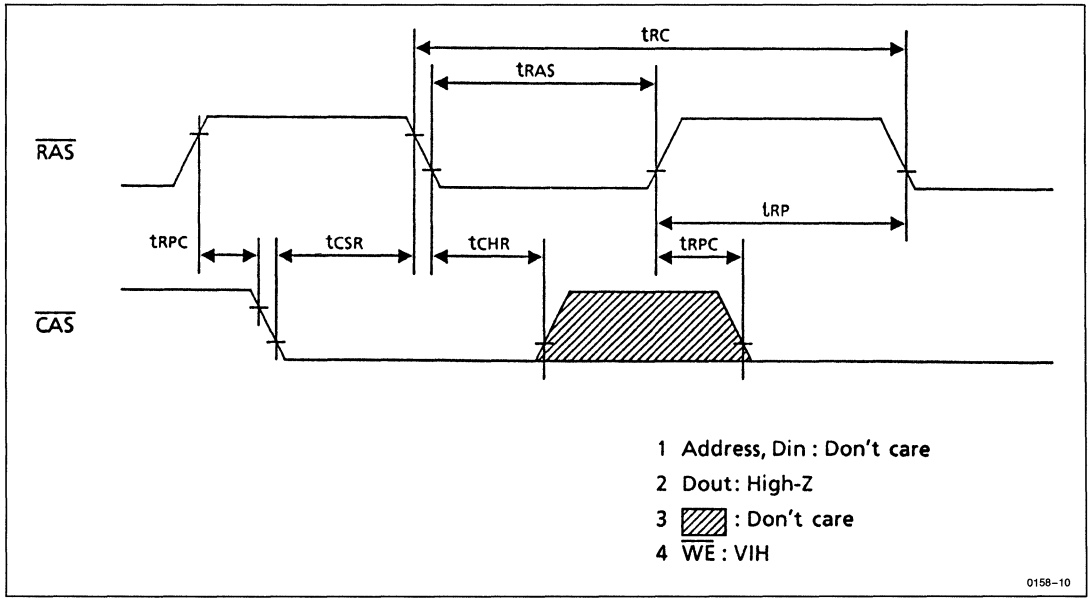
• **Early Write Cycle**



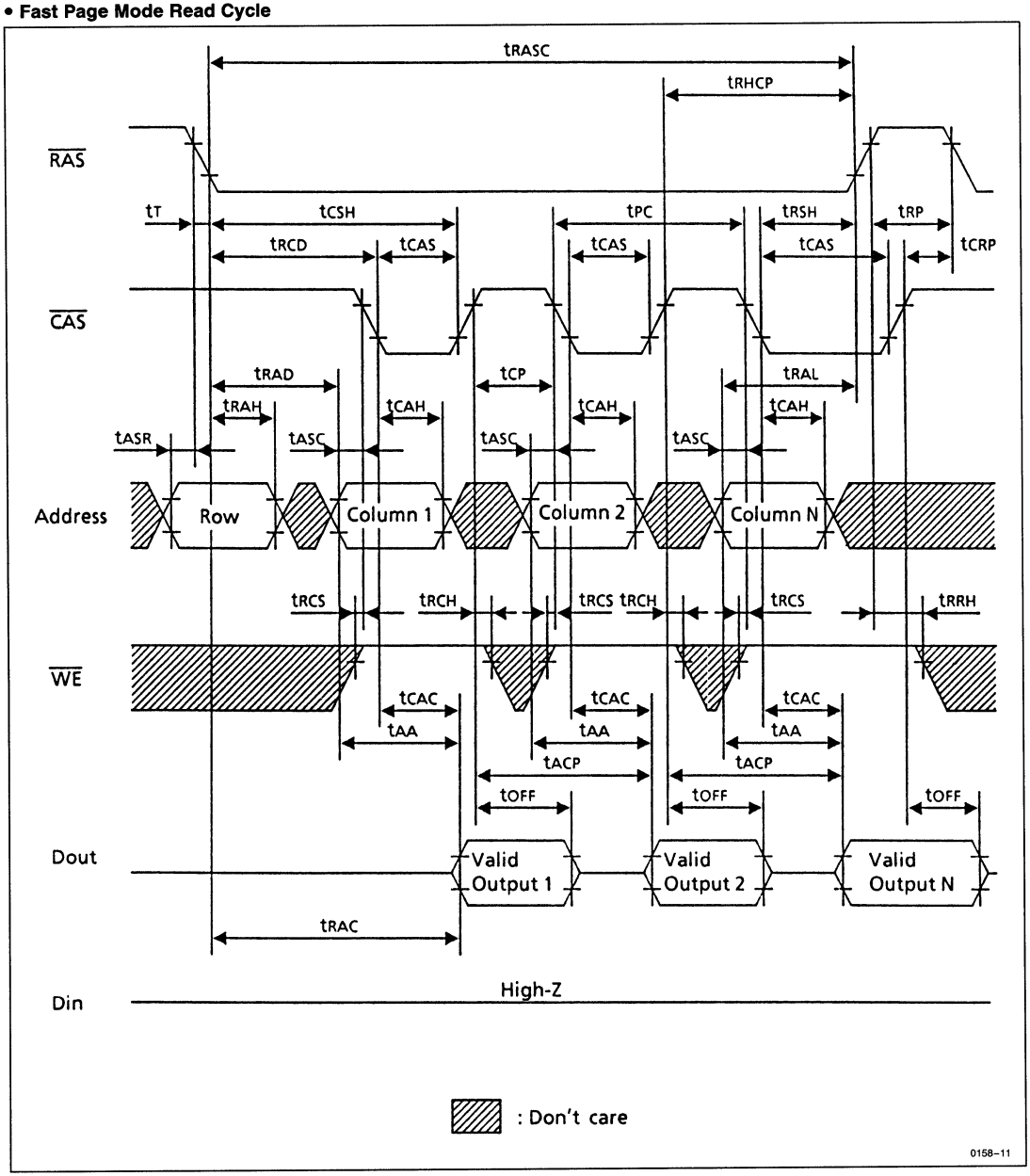
• $\overline{RAS}$ Only Refresh Cycle



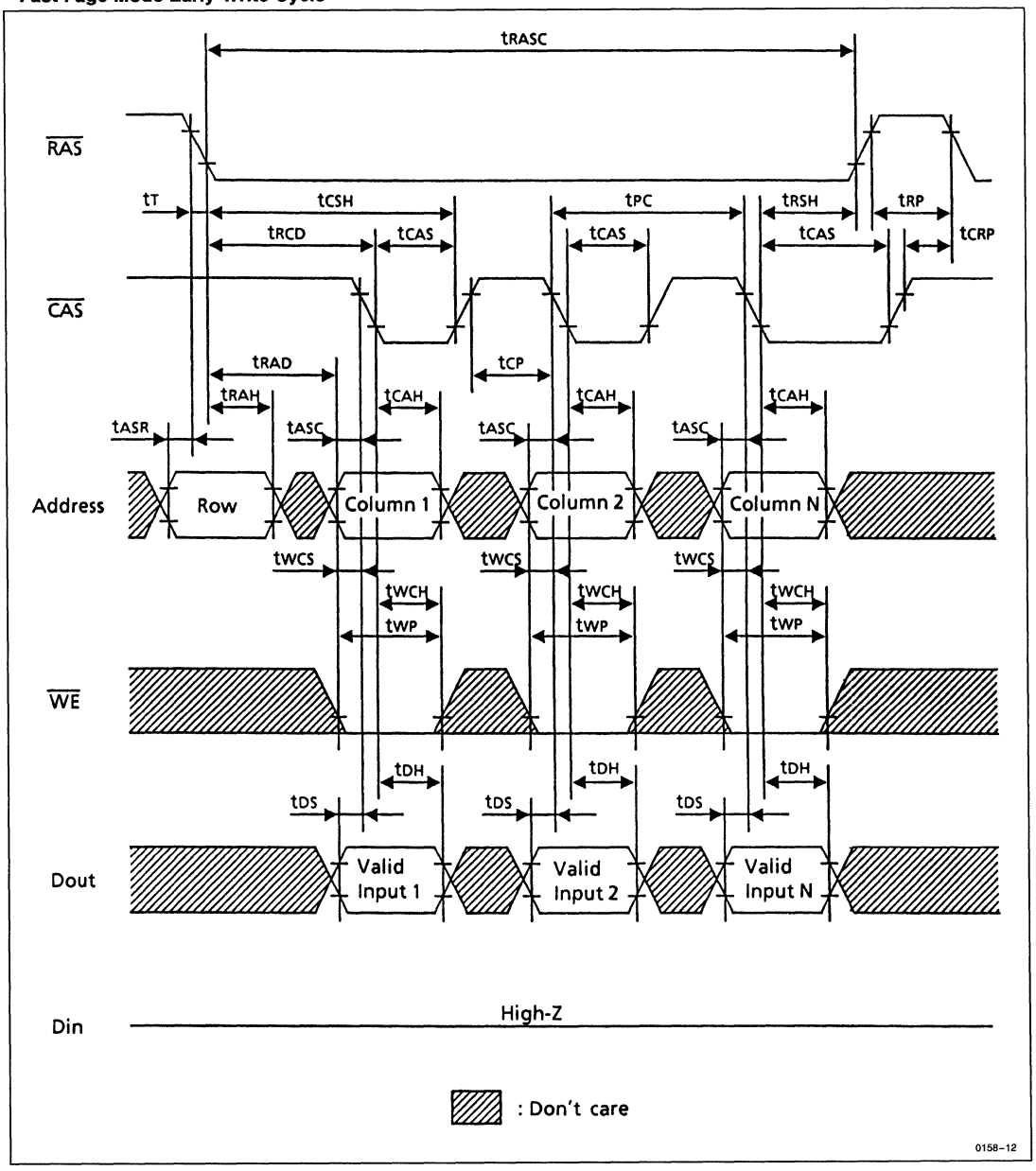
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



HB56A140 Series

1,048,576-Word x 40-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56A140B/SB is a 1M x 40 dynamic RAM module, mounted 10 pieces of 4 Mbit DRAM (HM514400AS) sealed in SOJ package. An outline of the HB56A140B/SB is a 72-pin single in-line package. Therefore, the HB56A140B/SB makes high density mounting possible without surface mount technology. The HB56A140B/SB provides common data inputs and outputs. Its module board has decoupling capacitors beneath the each SOJ.

■ FEATURES

- 72-pin Single In-line Package
  - Lead Pitch 1.27mm
- Single 5V (±5%) Supply
- High Speed
  - Access Time ..... 60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Operation ..... 5775 mW/5250 mW/4725 mW/4200 mW (max)
  - Standby ..... 105 mW
- Fast Page Mode Capability
- 1,024 Refresh Cycles ..... (16 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

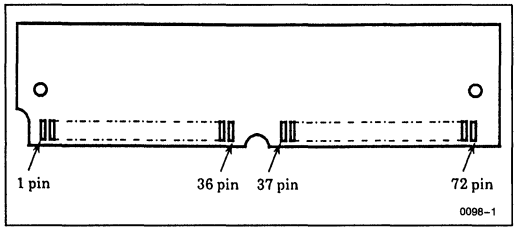
■ ORDERING INFORMATION

Part No.	Access Time	Package	Contact Pad
HB56A140B-6A	60 ns	72-pin SIP Socket Type	Gold
HB56A140B-7A	70 ns		
HB56A140B-8A	80 ns		
HB56A140B-10A	100 ns		
HB56A140SB-6A	60 ns	72-pin SIP Socket Type	Solder
HB56A140SB-7A	70 ns		
HB56A140SB-8A	80 ns		
HB56A140SB-10A	100 ns		

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_8	Refresh Address Input
DQ_0–DQ_{39}	Data-in/Data-out
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power Supply (+ 5V)
V_{SS}	Ground
PD1–PD4	Presence Detect Pin
NC	No Connection

■ PIN OUT

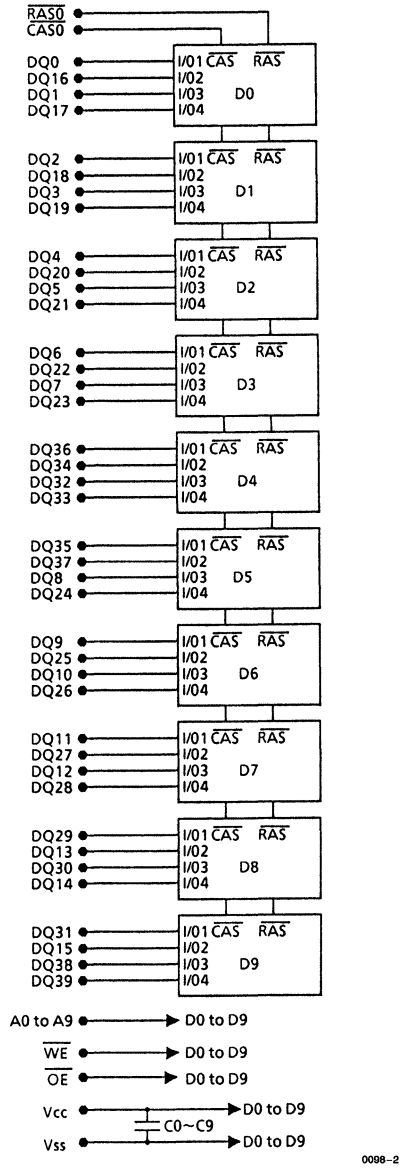


Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	$\overline{OE}$	37	DQ_{33}	55	DQ_{11}
2	DQ_0	20	DQ_4	38	DQ_{35}	56	DQ_{27}
3	DQ_{16}	21	DQ_{20}	39	V_{SS}	57	DQ_{12}
4	DQ_1	22	DQ_5	40	NC	58	DQ_{28}
5	DQ_{17}	23	DQ_{21}	41	$\overline{CAS}$	59	V_{DD}
6	DQ_2	24	DQ_6	42	NC	60	DQ_{29}
7	DQ_{18}	25	DQ_{22}	43	NC	61	DQ_{13}
8	DQ_3	26	DQ_7	44	$\overline{RAS}$	62	DQ_{30}
9	DQ_{19}	27	DQ_{23}	45	NC	63	DQ_{14}
10	V_{DD}	28	A_7	46	DQ_{37}	64	DQ_{31}
11	NC	29	DQ_{36}	47	$\overline{WE}$	65	DQ_{15}
12	A_0	30	V_{DD}	48	GND	66	DQ_{38}
13	A_1	31	A_8	49	DQ_8	67	PD1
14	A_2	32	A_9	50	DQ_{24}	68	PD2
15	A_3	33	NC	51	DQ_9	69	PD3
16	A_4	34	NC	52	DQ_{25}	70	PD4
17	A_5	35	DQ_{34}	53	DQ_{10}	71	DQ_{39}
18	A_6	36	DS_{36}	54	DQ_{26}	72	V_{SS}

■ PRESENCE DETECT PINOUT

Pin No.	Pin Name	HB56A140B/SB			
		-6A	-7A	-8A	-10A
67	PD1	V_{SS}	V_{SS}	V_{SS}	V_{SS}
68	PD2	V_{SS}	V_{SS}	V_{SS}	V_{SS}
69	PD3	NC	V_{SS}	NC	V_{SS}
70	PD4	NC	NC	V_{SS}	V_{SS}

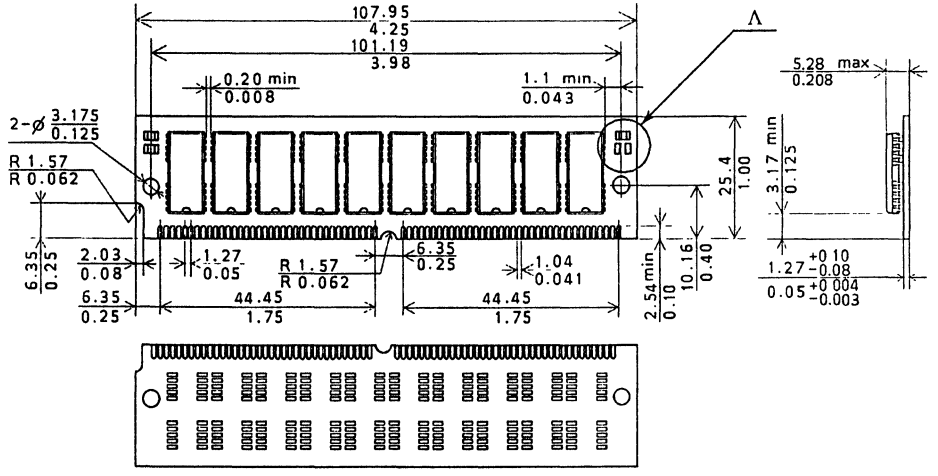
■ BLOCK DIAGRAM



* D0 to D9: HM514400AS

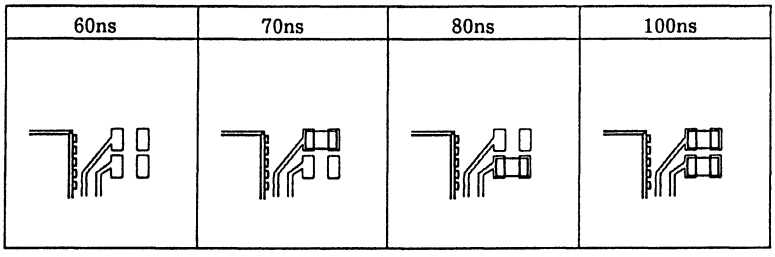
■ PACKAGE OUTLINE

Unit: mm / inch



0098-3

Detail A



0098-4

Note: Following the specification of the contact pad.

Part No.	Contact Pad
HB56A140B-XXA	Gold
HB56A140SB-XXA	Solder

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	10	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)

Parameter	Symbol	HB56A140B/SB								Unit	Test Conditions	Note
		-6A		-7A		-8A		-10A				
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	1100	—	1000	—	900	—	800	mA	t_{RC} = min	1, 2
Standby Current	I_{CC2}	—	20	—	20	—	20	—	20	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High Z	
		—	10	—	10	—	10	—	10	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	1100	—	1000	—	900	—	800	mA	t_{RC} = min	2
Standby Current	I_{CC5}	—	50	—	50	—	50	—	50	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	1100	—	1000	—	900	—	800	mA	t_{RC} = min	
Fast Page Mode Current	I_{CC7}	—	1100	—	1000	—	900	—	800	mA	t_{PC} = min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{IN} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{OUT} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed ≤ 1 time while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address A_0–A_9)	C_{I1}	—	90	pF	1
Input Capacitance ($\overline{WE}$, $\overline{OE}$)	C_{I2}	—	90	pF	1
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I3}	—	90	pF	1
Input/Output Capacitance (DQ_0 to DQ_{39})	$C_{I/O1}$	—	20	pF	1

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)[1, 14, 15, 16]

Read, Write and Refresh Cycle (Common Parameters)

Parameter	Symbol	HB56A140B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10000	20	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	20	60	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	15	—	20	—	20	—	25	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	0	—	ns	
$\overline{CAS}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	
Refresh Period	t_{REF}	—	16	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HB56A140B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	2, 3, 17
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	—	25	ns	3, 4, 13
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	ns	3, 4, 13, 16
Access Time from $\overline{OE}$	t_{OAC}	—	15	—	20	—	20	—	25	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	15	0	20	0	20	0	20	ns	6
Output Buffer Turn-off Time to $\overline{OE}$	t_{OFF2}	0	15	0	20	0	20	0	20	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	15	—	20	—	20	—	25	—	ns	

Write Cycle

Parameter	Symbol	HB56A140B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	10	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	20	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	20	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HB56A140B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-Write Cycle Time	t_{RWC}	150	—	180	—	200	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	95	—	105	—	135	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	35	—	45	—	45	—	60	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	50	—	60	—	65	—	80	—	ns	10
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	15	—	20	—	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HB56A140B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HB56A140B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	35	—	40	—	45	—	50	ns	13, 17
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	45	—	50	—	ns	
Fast Page mode Read-Modify-Write Cycle Time	t_{PCM}	80	—	95	—	100	—	110	—	ns	

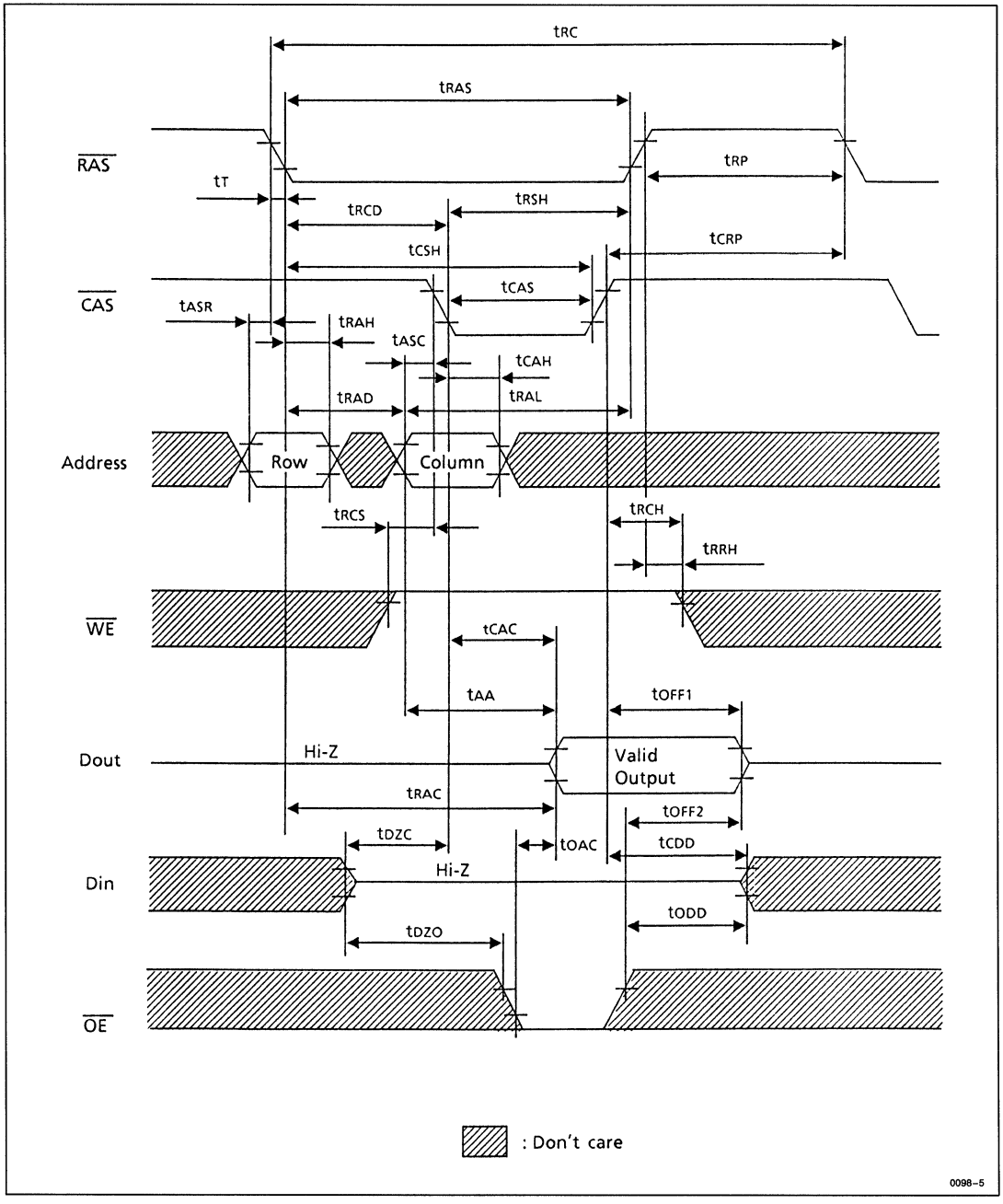
Test Mode Cycle

Parameter	Symbol	HB56A140B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	10	—	10	—	10	—	10	—	ns	

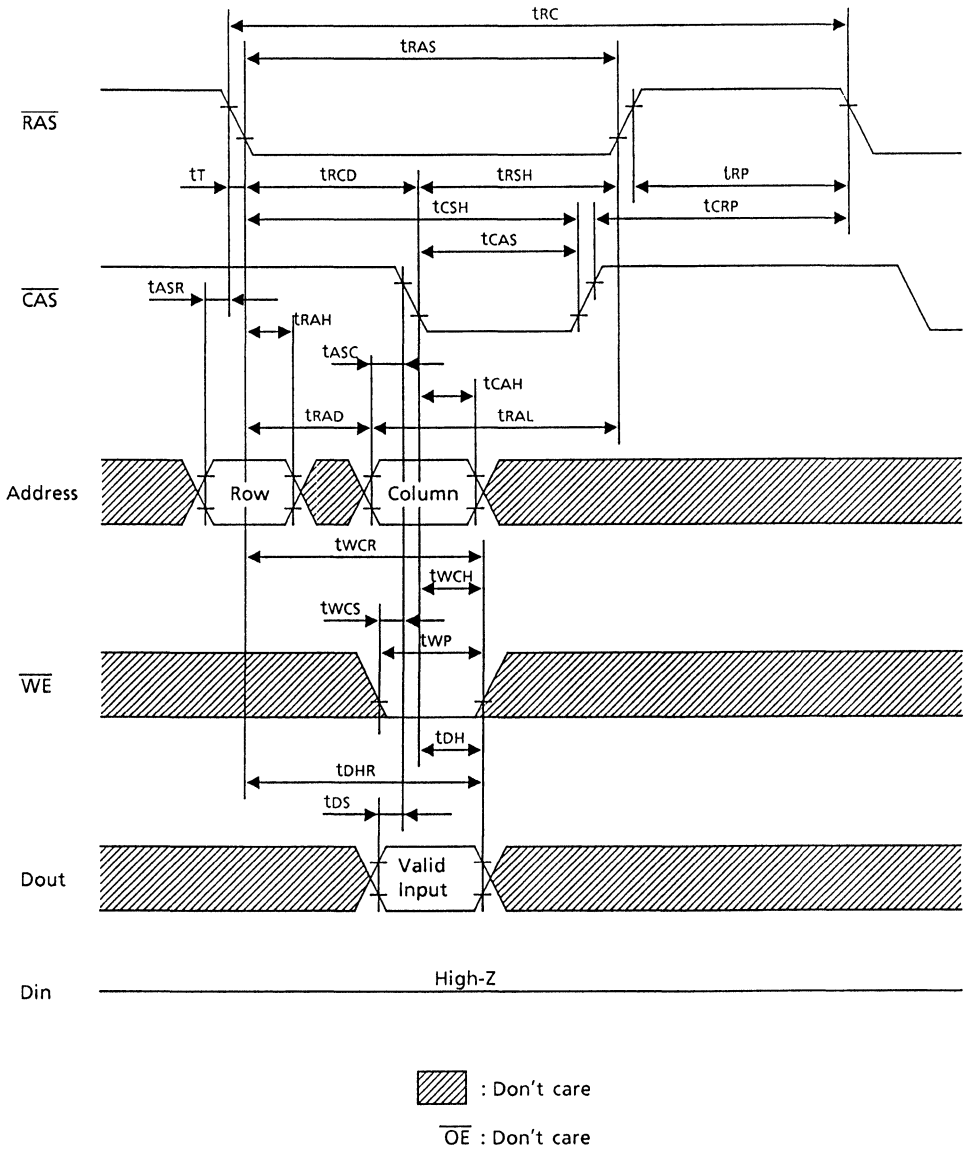
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL load and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading in an early write cycle and to WE leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycle.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits ... CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is low level. Data output pin is I/O_3 and data input pin is I/O_2. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{OAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORMS

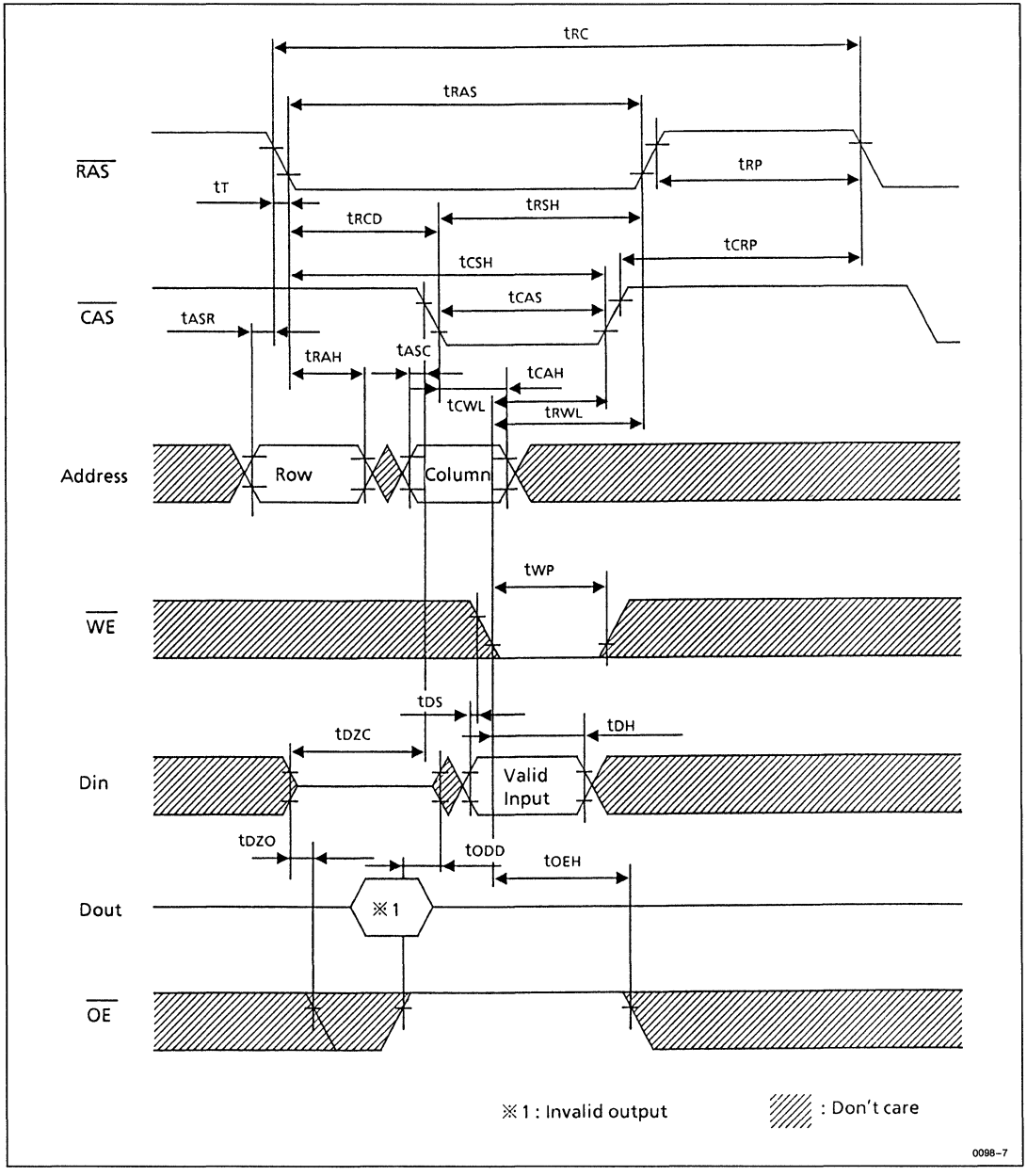
• Read Cycle



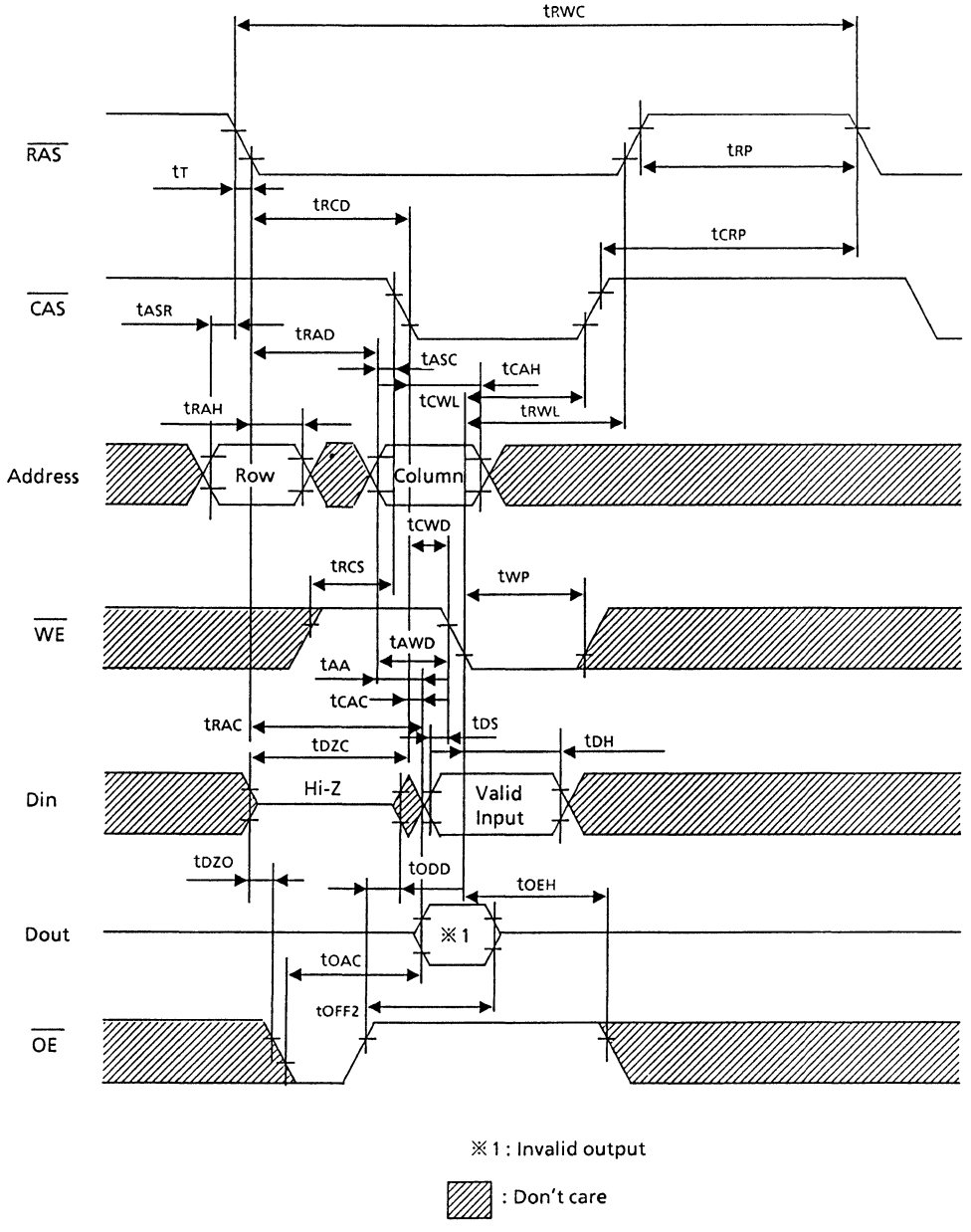
• **Early Write Cycle**



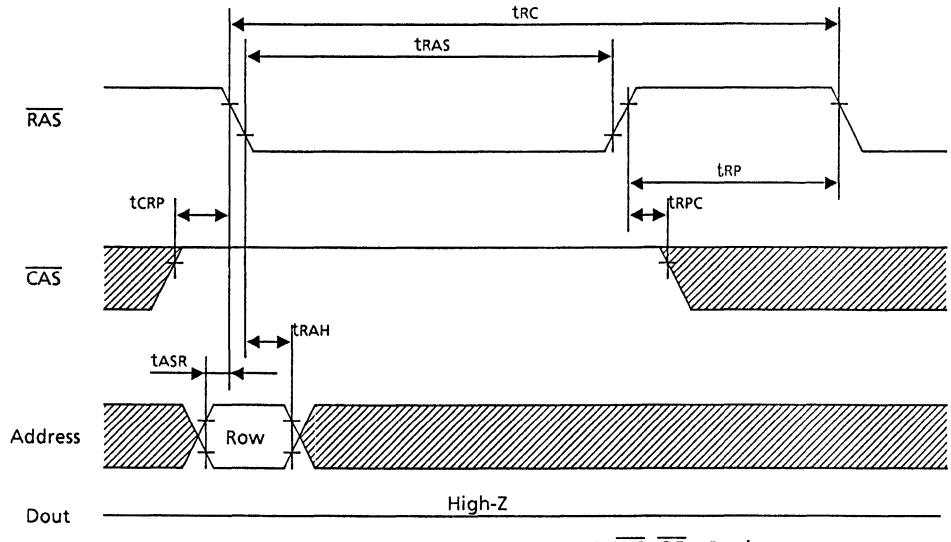
• **Delayed Write Cycles**



• **Read-Modify-Write Cycle**



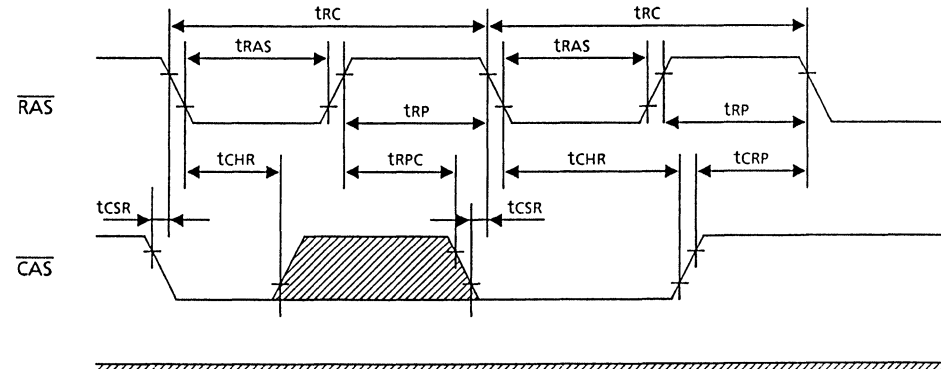
• $\overline{RAS}$ Only Refresh Cycle



1 $\overline{WE}$, $\overline{OE}$: Don't care
2 ▨ : Don't care
3 REFRESH ADDRESS : A0 - A9
(AX0 - AX9)

0098-9

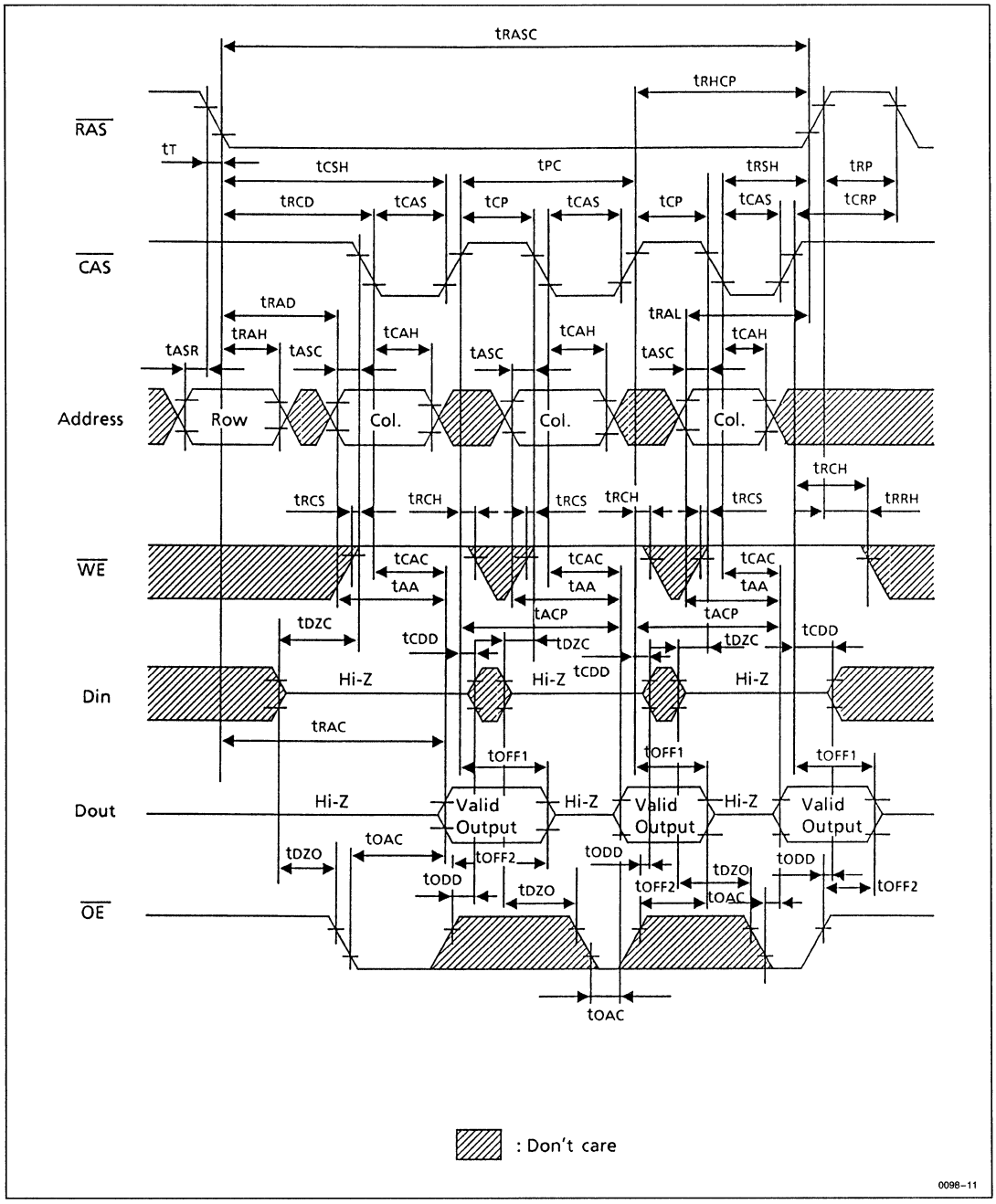
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



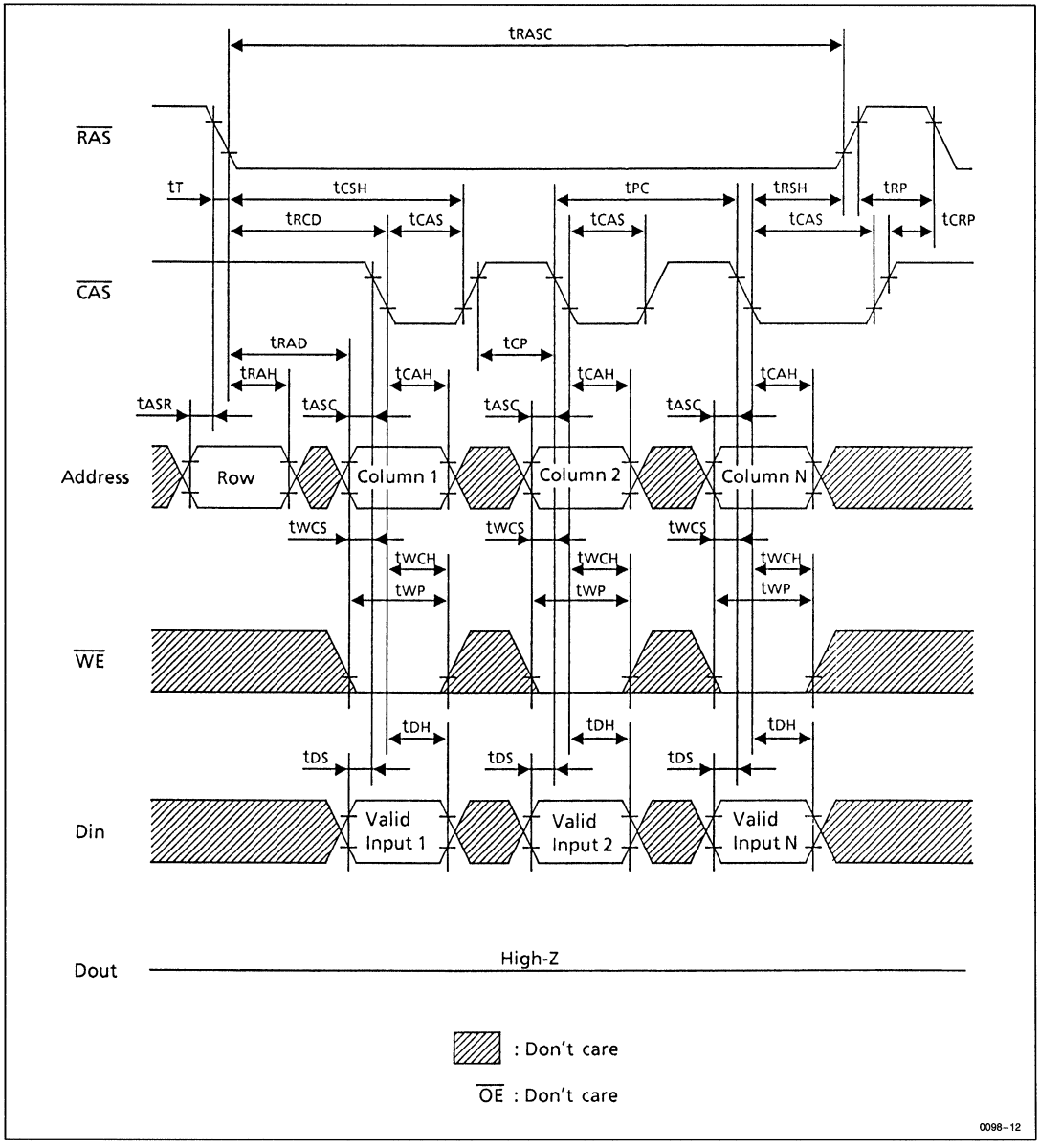
1 $\overline{WE}$: V_{IH}
2 ▨ : Don't care

0098-10

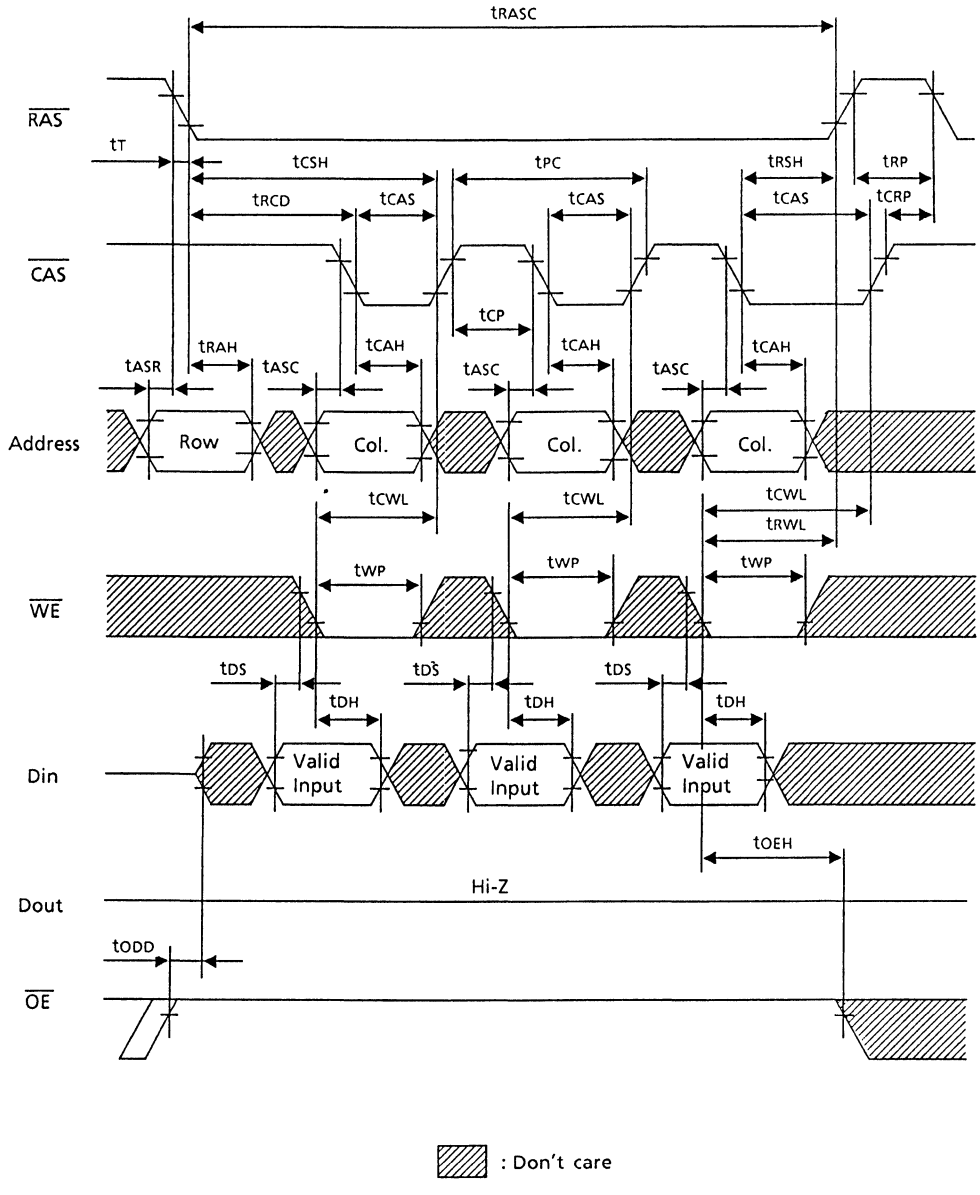
• **Fast Page Mode Read Cycle**



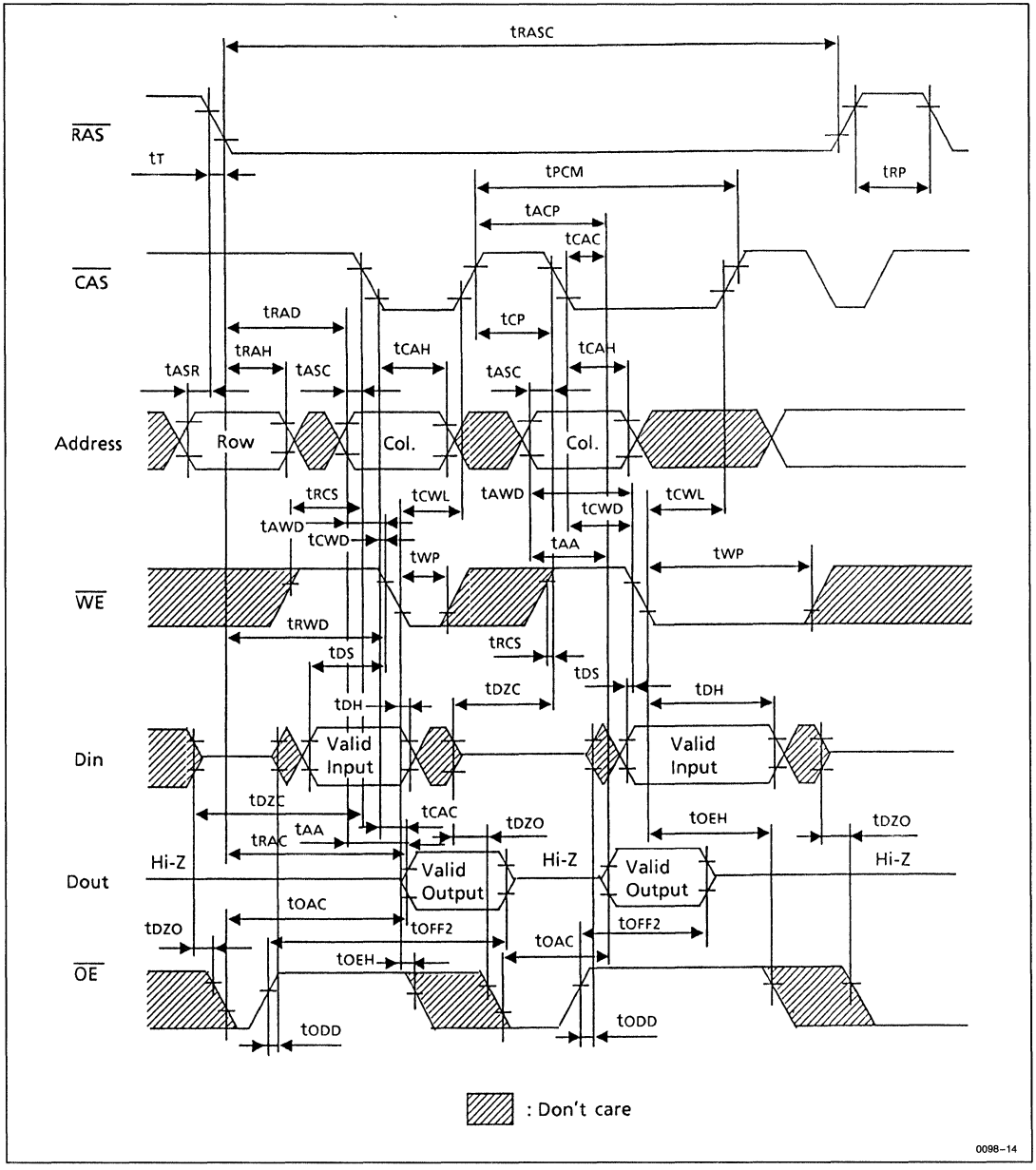
• **Fast Page Mode Early Write Cycle**



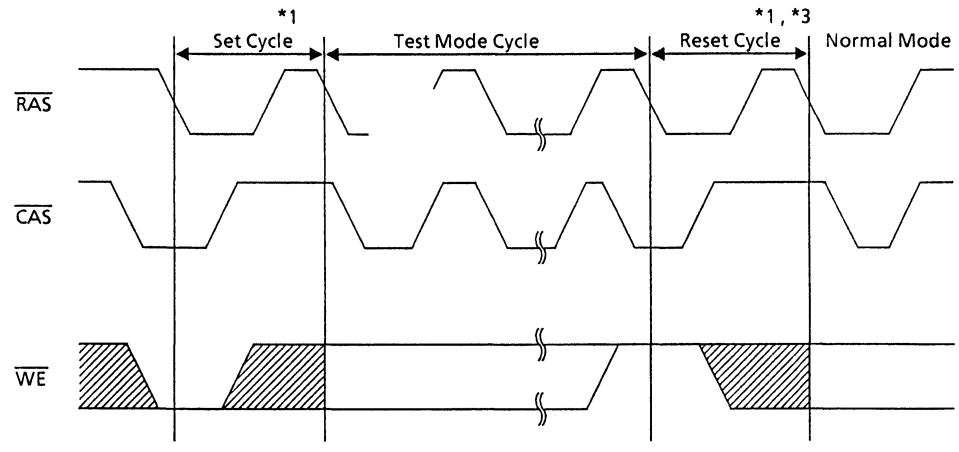
• **Fast Page Mode Delayed Write Cycle**



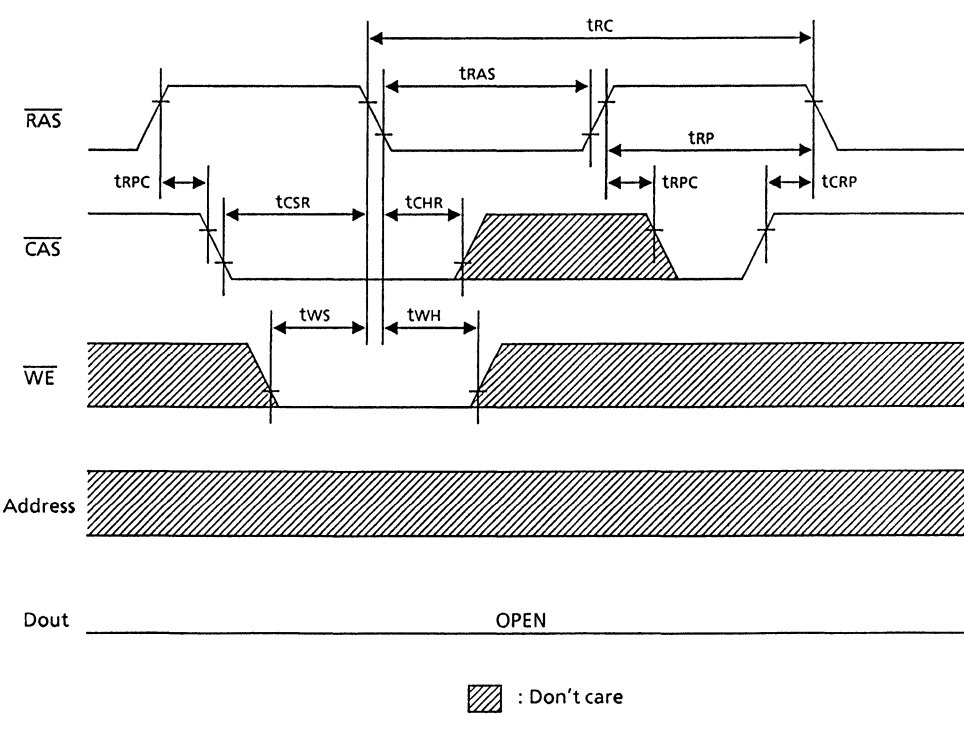
• **Fast Page Mode Read-Modify-Write Cycle**



• **TEST MODE CYCLE**

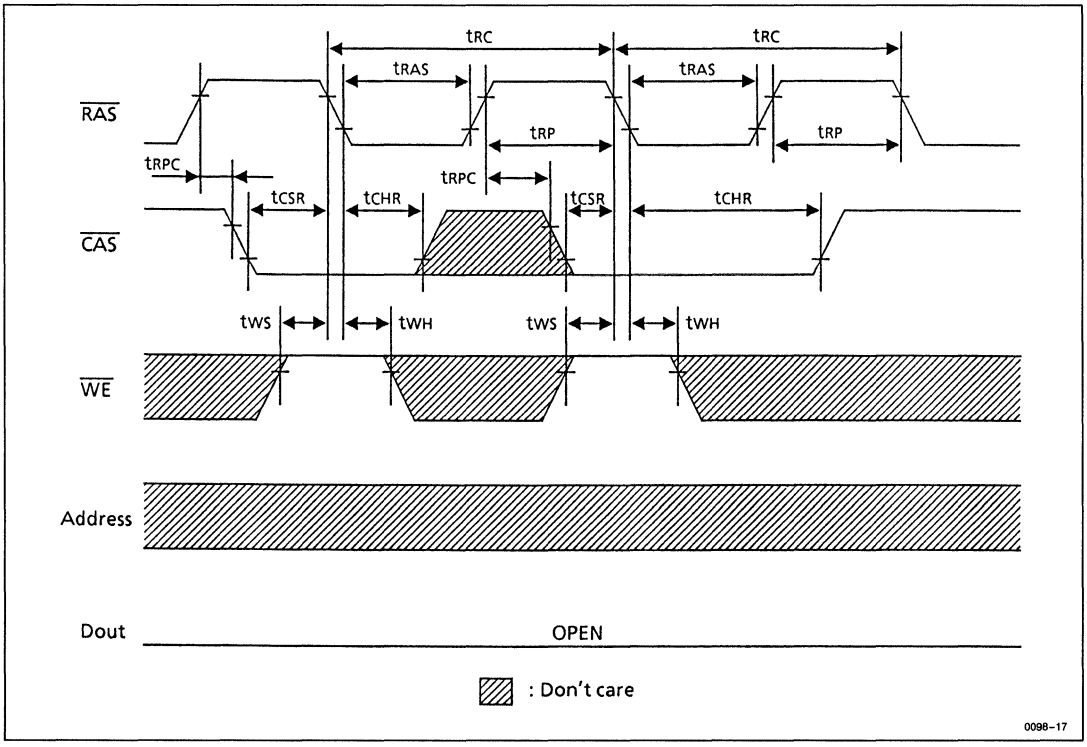


• **(1) Test Mode Set Cycle**

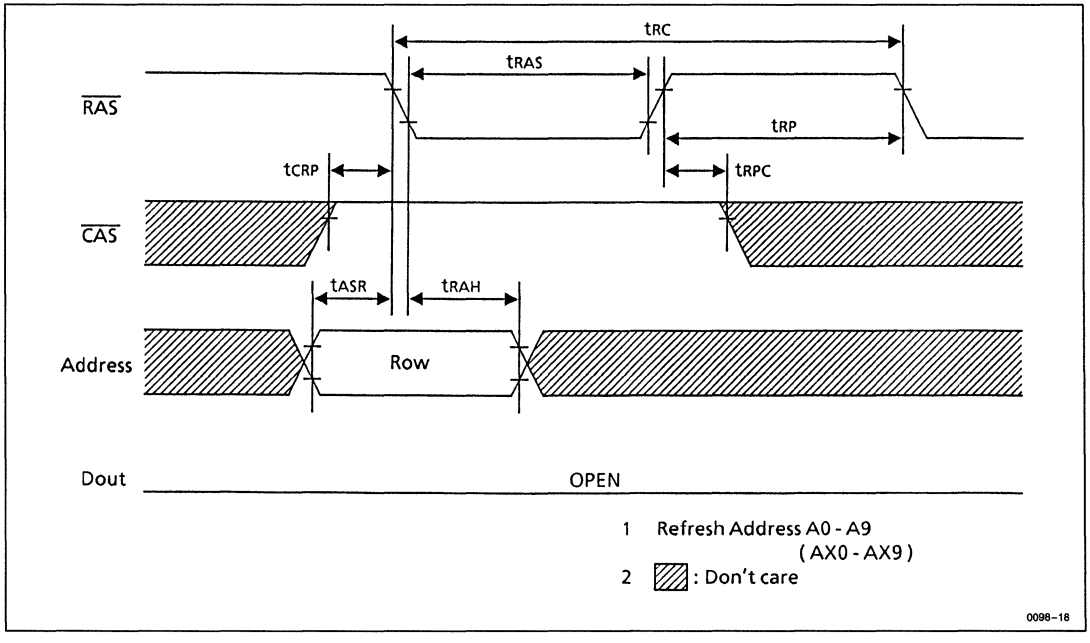


• (2) Test Mode Reset Cycle

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



$\overline{RAS}$ Only Refresh Cycle



HB56A240 Series

2,097,152-Word x 40-Bit High Density Dynamic RAM Module

■ DESCRIPTION

The HB56A240B/SB is a 2M x 40 dynamic RAM module, mounted 20 pieces of 4 Mbit DRAM (HM514400AS) sealed in SOJ package. An outline of the HB56A240B/SB is a 72-pin single in-line package. Therefore, the HB56A240B/SB makes high density mounting possible without surface mount technology. The HB56A240B/SB provides common data inputs and outputs. Its module board has decoupling capacitors beneath the each SOJ but only on the one side of its module board.

■ FEATURES

- 72-pin Single In-line Package
  - Lead Pitch 1.27mm
- Single 5V (±5%) Supply
- High Speed
  - Access Time .....60 ns/70 ns/80 ns/100 ns (max)
- Low Power Dissipation
  - Operation .....6038 mW/5513 mW/4988 mW/4463 mW (max)
  - Standby .....210 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles .....(16 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

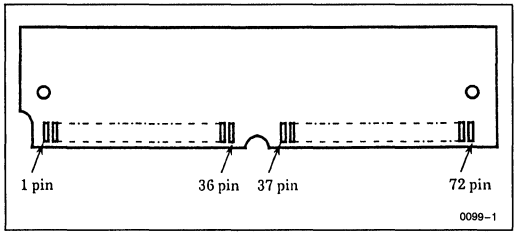
■ ORDERING INFORMATION

Part No.	Access Time	Package	Contact Pad
HB56A240B-6A	60 ns	72-pin SIP Socket Type	Gold
HB56A240B-7A	70 ns		
HB56A240B-8A	80 ns		
HB56A240B-10A	100 ns		
HB56A240SB-6A	60 ns	72-pin SIP Socket Type	Solder
HB56A240SB-7A	70 ns		
HB56A240SB-8A	80 ns		
HB56A240SB-10A	100 ns		

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_8	Refresh Address Input
DQ_0–DQ_{39}	Data-in/Data-out
$\overline{CAS0}$, $\overline{CAS1}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS0}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power Supply (+5V)
V_{SS}	Ground
PD1–PD4	Presence Detect Pin
NC	No Connection

■ PINOUT

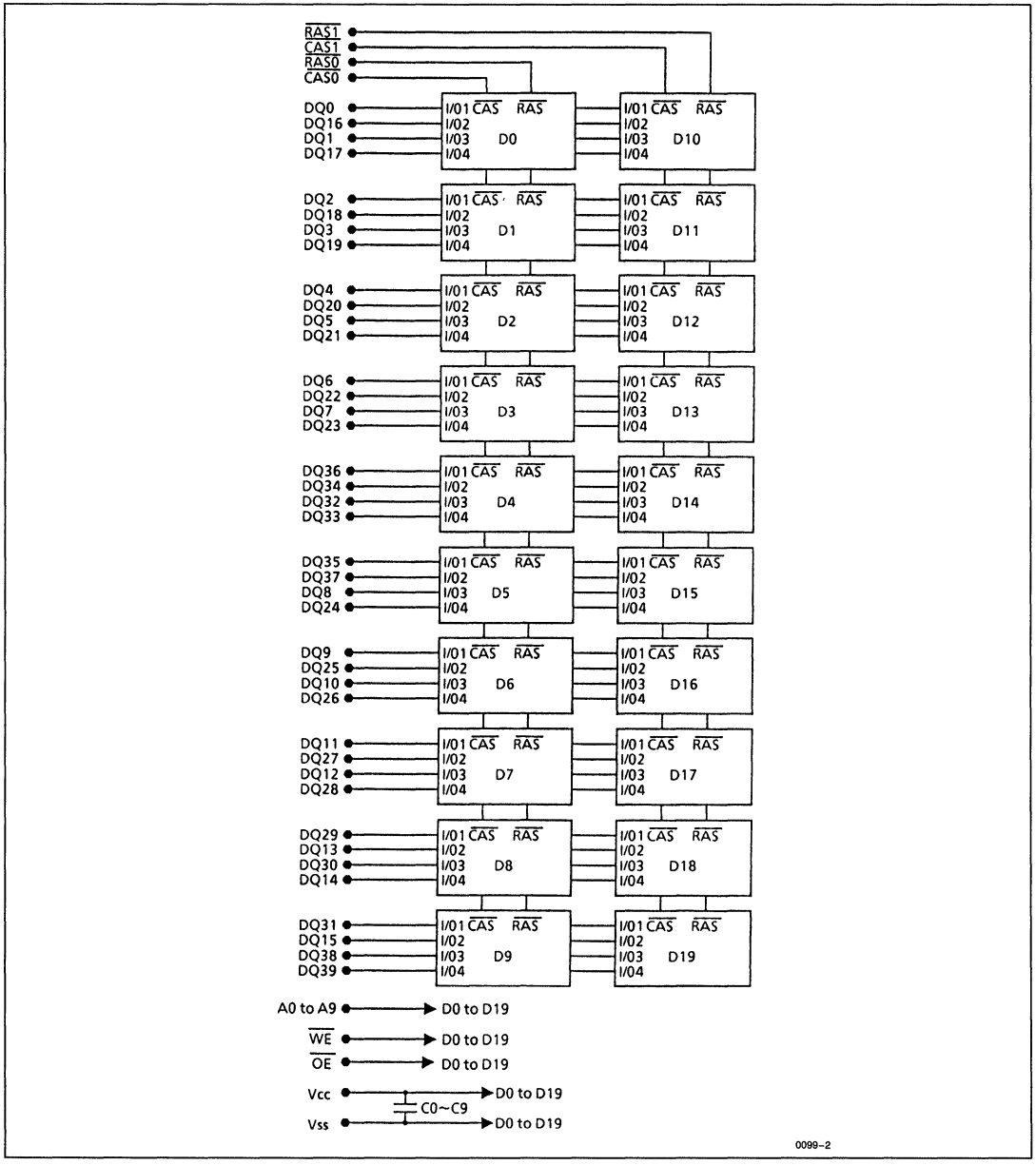


Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	$\overline{OE}$	37	DQ_{33}	55	DQ_{11}
2	DQ_0	20	DQ_4	38	DQ_{35}	56	DQ_{27}
3	DQ_{16}	21	DQ_{20}	39	V_{SS}	57	DQ_{12}
4	DQ_1	22	DQ_5	40	NC	58	DQ_{28}
5	DQ_{17}	23	DQ_{21}	41	$\overline{CAS0}$	59	V_{DD}
6	DQ_2	24	DQ_6	42	$\overline{CAS1}$	60	DQ_{29}
7	DQ_{18}	25	DQ_{22}	43	NC	61	DQ_{13}
8	DQ_3	26	DQ_7	44	$\overline{RAS0}$	62	DQ_{30}
9	DQ_{19}	27	DQ_{23}	45	$\overline{RAS1}$	63	DQ_{14}
10	V_{DD}	28	A_7	46	DQ_{37}	64	DQ_{31}
11	NC	29	DQ_{36}	47	$\overline{WE}$	65	DQ_{15}
12	A_0	30	V_{DD}	48	GND	66	DQ_{38}
13	A_1	31	A_8	49	DQ_8	67	PD1
14	A_2	32	A_9	50	DQ_{24}	68	PD2
15	A_3	33	NC	51	DQ_9	69	PD3
16	A_4	34	NC	52	DQ_{25}	70	PD4
17	A_5	35	DQ_{34}	53	DQ_{10}	71	DQ_{39}
18	A_6	36	DS_{36}	54	DQ_{26}	72	V_{SS}

■ PRESENCE DETECT PINOUT

Pin No.	Pin Name	HB56A240B/SB			
		-6A	-7A	-8A	-10A
67	PD1	NC	NC	NC	NC
68	PD2	NC	NC	NC	NC
69	PD3	NC	V_{SS}	NC	V_{SS}
70	PD4	NC	NC	V_{SS}	V_{SS}

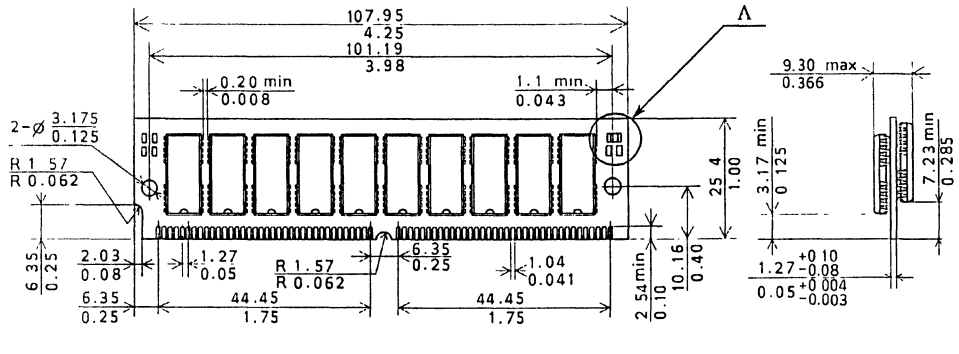
■ BLOCK DIAGRAM



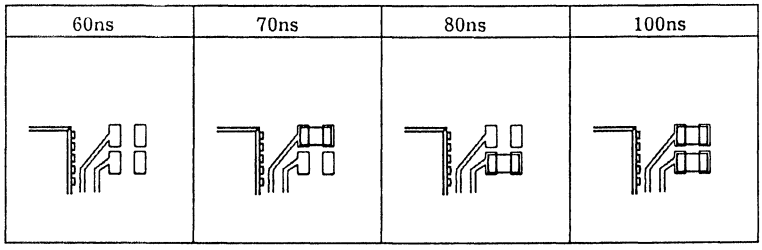
* D0 to D9: HM514400AS

■ PHYSICAL OUTLINE

Unit: mm / inch



Detail A



Note: Following the specification of the contact pad.

Part No.	Contact Pad
HB56A240B-XXA	Gold
HB56A240SB-XXA	Solder

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	− 1.0 to + 7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	10	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	− 1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V)

Parameter	Symbol	HB56A240B/SB								Unit	Test Conditions	Note
		-6A		-7A		-8A		-10A				
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	1150	—	1050	—	950	—	850	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	40	—	40	—	40	—	40	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} D_{out} = High-Z	
		—	20	—	20	—	20	—	20	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	1150	—	1050	—	950	—	850	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	100	—	100	—	100	—	100	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	1150	—	1050	—	950	—	850	mA	t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	1150	—	1050	—	950	—	850	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	− 10	10	− 10	10	− 10	10	− 10	10	μA	0V ≤ V_{out} ≤ 7V D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = − 5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address A_0–A_9)	C_{I1}	—	140	pF	1
Input Capacitance ($\overline{WE}$, $\overline{OE}$)	C_{I2}	—	160	pF	1
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I4}	—	90	pF	1
Input/Output Capacitance (DQ_0 to DQ_{39})	$C_{I/O1}$	—	25	pF	1

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)[1, 14, 15, 16]

Read, Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	150	—	180	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	60	—	70	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	100000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10000	20	10000	20	10000	25	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	20	60	25	75	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	20	55	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
$\overline{OE}$ to D_{in} Delay Time	t_{ODD}	15	—	20	—	20	—	25	—	ns	
$\overline{OE}$ Delay Time from D_{in}	t_{DZO}	0	—	0	—	0	—	0	—	ns	
$\overline{CAS}$ Setup Time from D_{in}	t_{DZC}	0	—	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	
Refresh Period	t_{REF}	—	16	—	16	—	16	—	16	ms	

• **Read Cycle**

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	ns	2, 3, 17
Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	—	25	ns	3, 4, 13
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	ns	3, 4, 13, 16
Access Time from $\overline{OE}$	t_{OAC}	—	15	—	20	—	20	—	25	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	0	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	ns	
Output Buffer Turn-off Time	t_{OFF1}	0	15	0	20	0	20	0	20	ns	6
Output Buffer Turn-off Time to $\overline{OE}$	t_{OFF2}	0	15	0	20	0	20	0	20	ns	6
$\overline{CAS}$ to D_{in} Delay Time	t_{CDD}	15	—	20	—	20	—	25	—	ns	

• Write Cycle

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	10	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	20	—	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	20	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	15	—	20	—	ns	11

• Read-Modify-Write Cycle

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-Write Cycle Time	t_{RWC}	150	—	180	—	200	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	80	—	95	—	105	—	135	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	35	—	45	—	45	—	60	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	50	—	60	—	65	—	80	—	ns	10
$\overline{OE}$ Hold Time from $\overline{WE}$	t_{OEH}	15	—	20	—	20	—	25	—	ns	

• Refresh Cycle

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

• Fast Page Mode Cycle

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	50	—	55	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	ns	12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	35	—	40	—	45	—	50	ns	13, 17
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	45	—	50	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	80	—	95	—	100	—	110	—	ns	

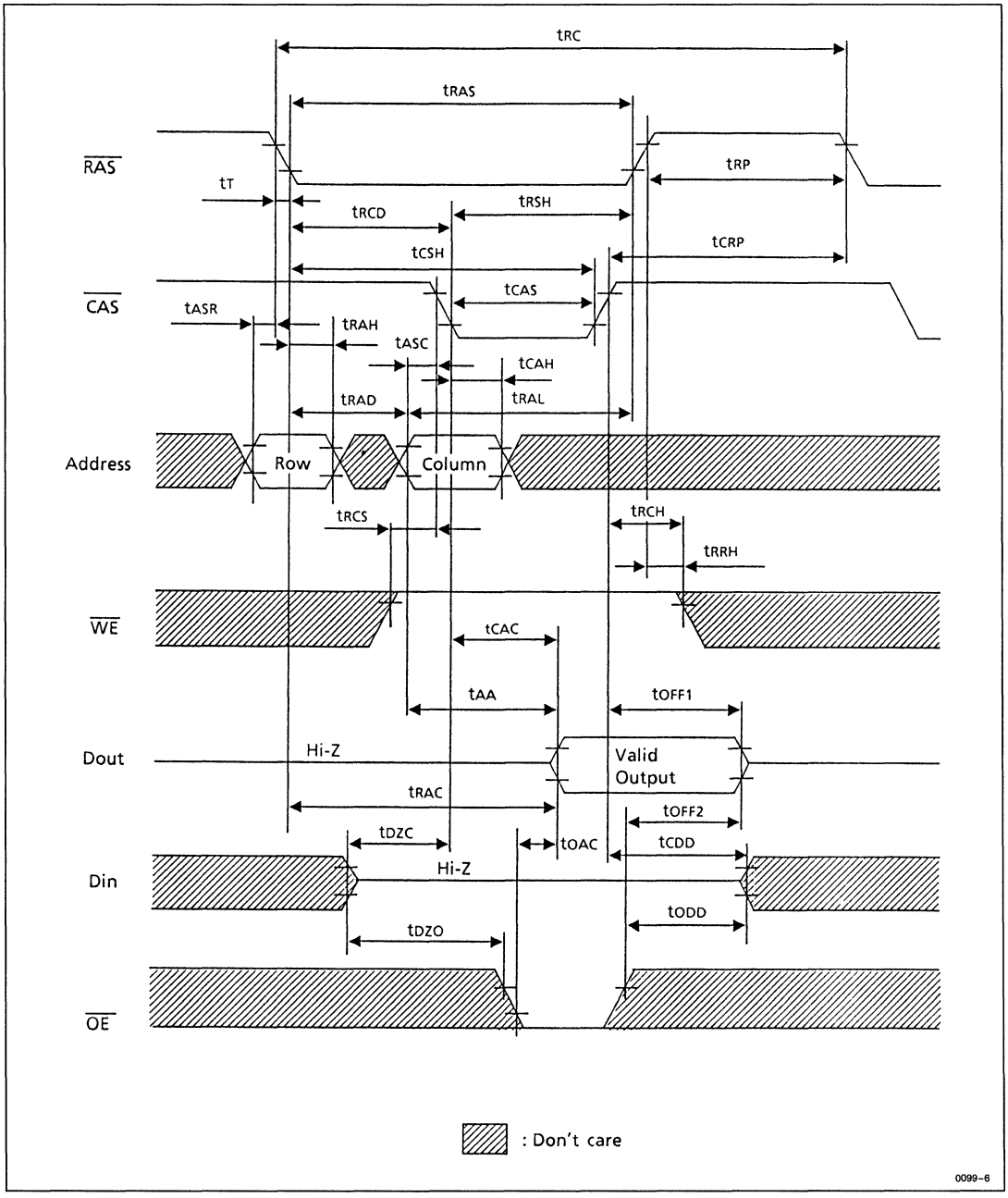
• Test Mode Cycle

Parameter	Symbol	HB56A240B/SB								Unit	Note
		-6A		-7A		-8A		-10A			
		Min	Max	Min	Max	Min	Max	Min	Max		
Test Mode $\overline{WE}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
Test Mode $\overline{WE}$ Hold Time	t_{WH}	10	—	10	—	10	—	10	—	ns	

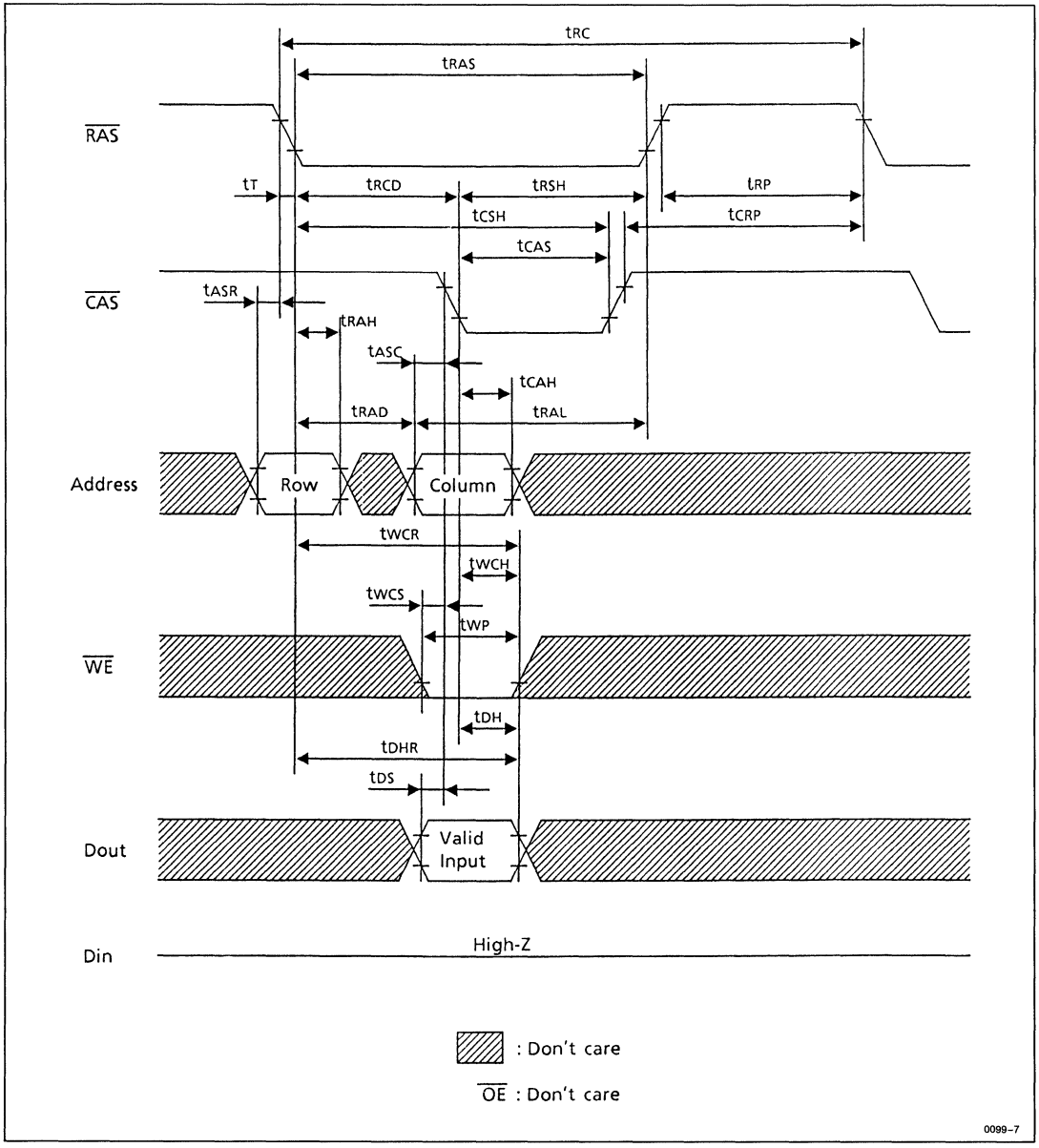
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL load and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of condition is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading in an early write cycle and to WE leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycle.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pulse of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycle is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits . . . CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is low level. Data output pin is I/O_3 and data input pin is I/O_2. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{OAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

■ TIMING WAVEFORMS

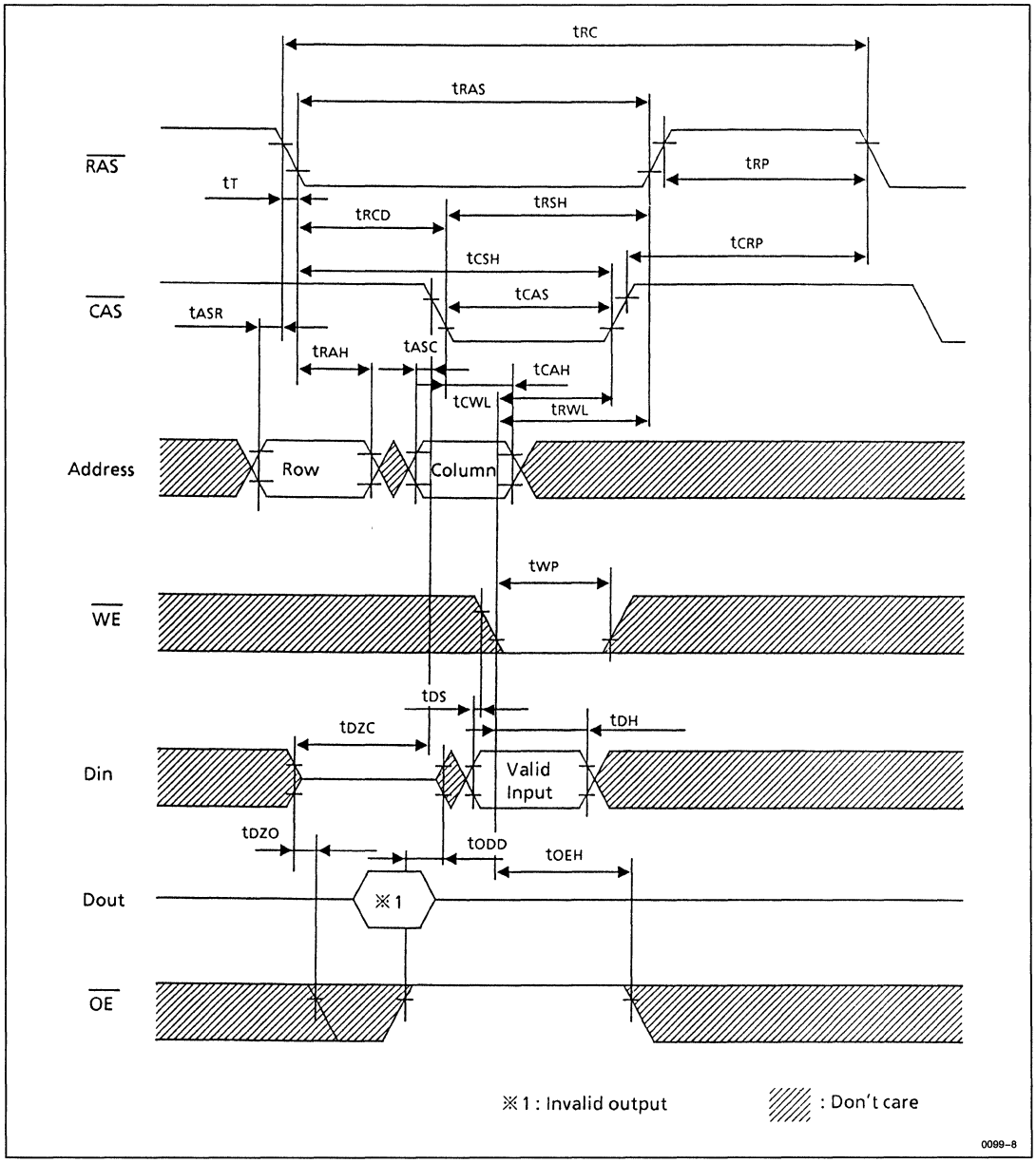
• Read Cycle



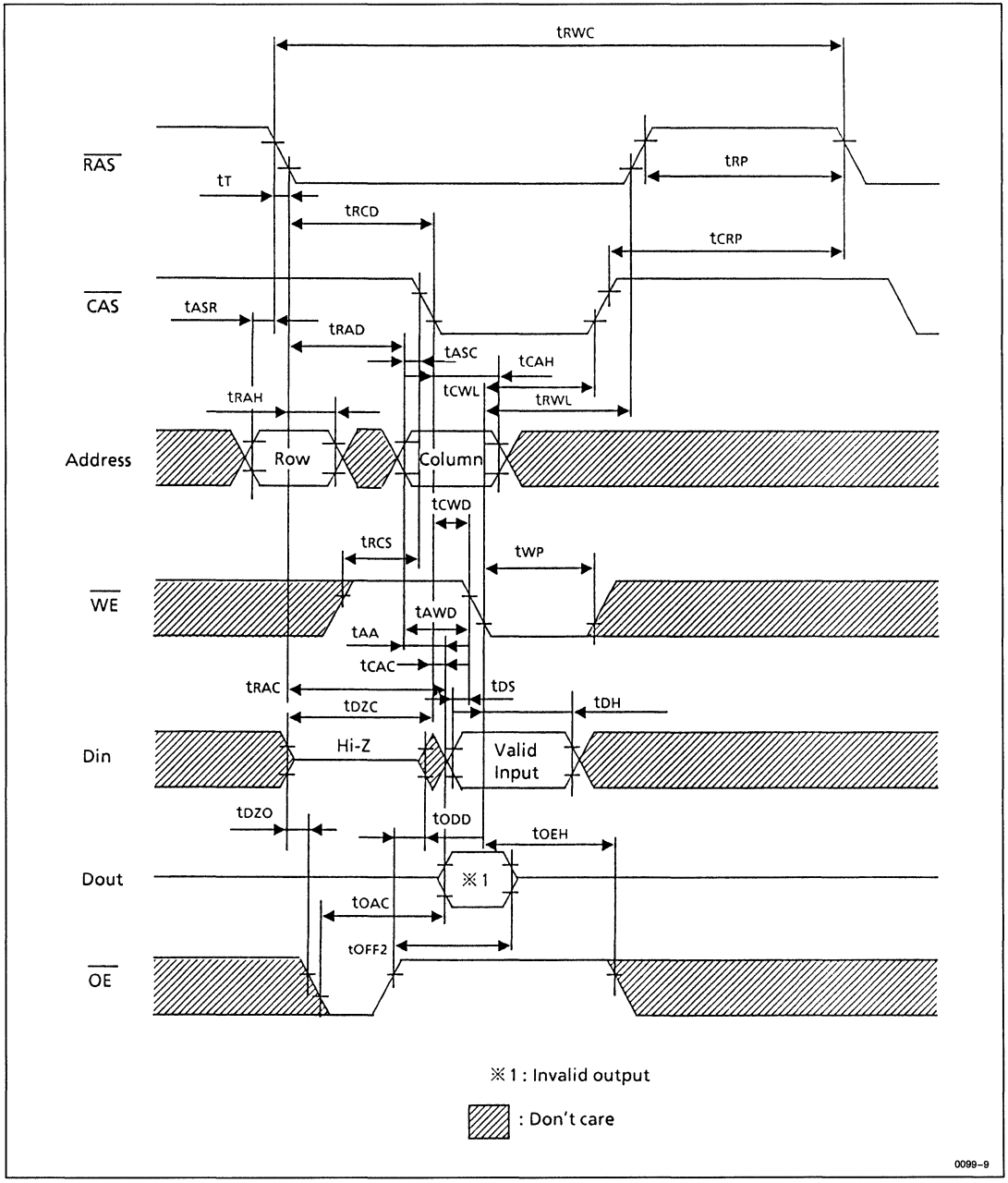
• **Early Write Cycle**



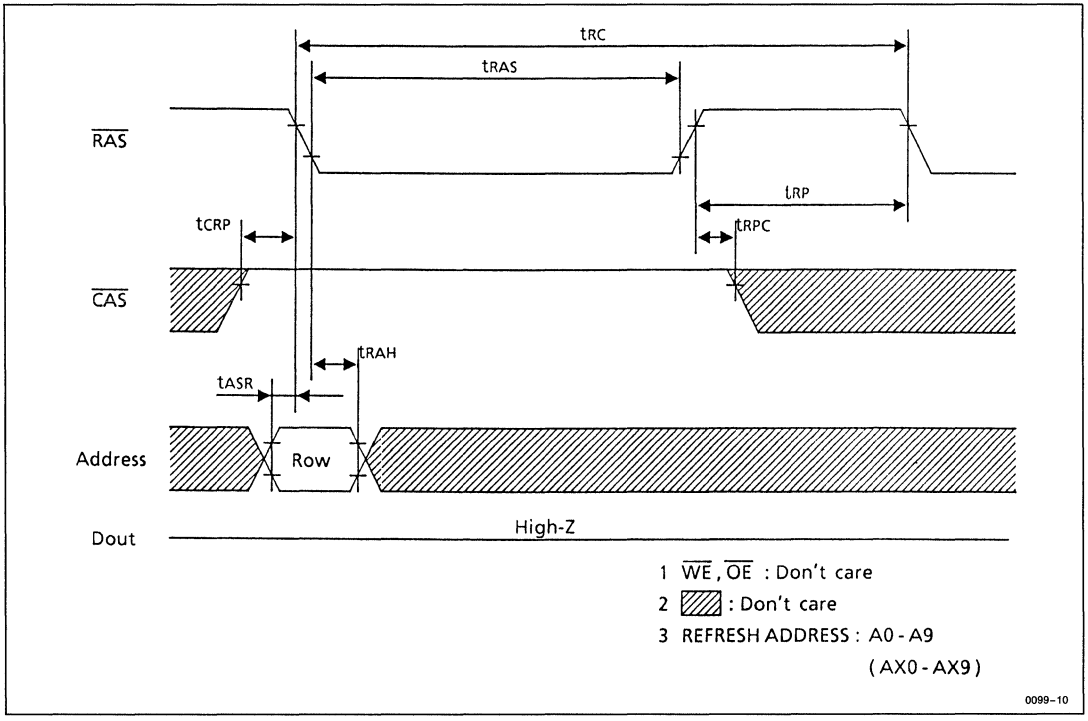
• **Delayed Write Cycles**



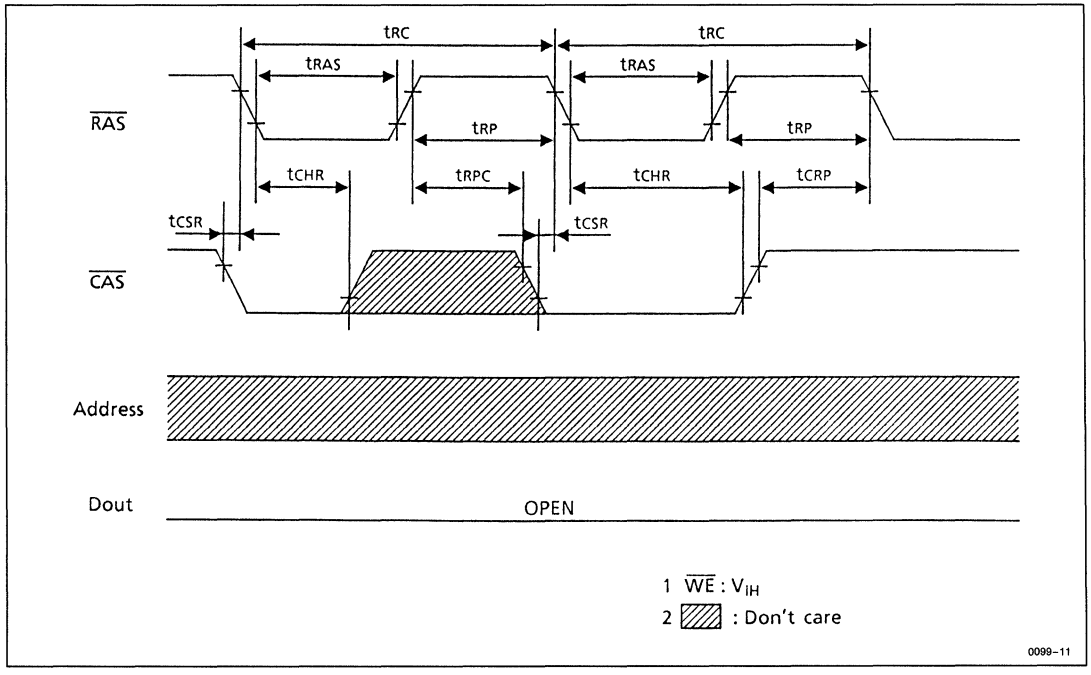
• **Read-Modify-Write Cycle**



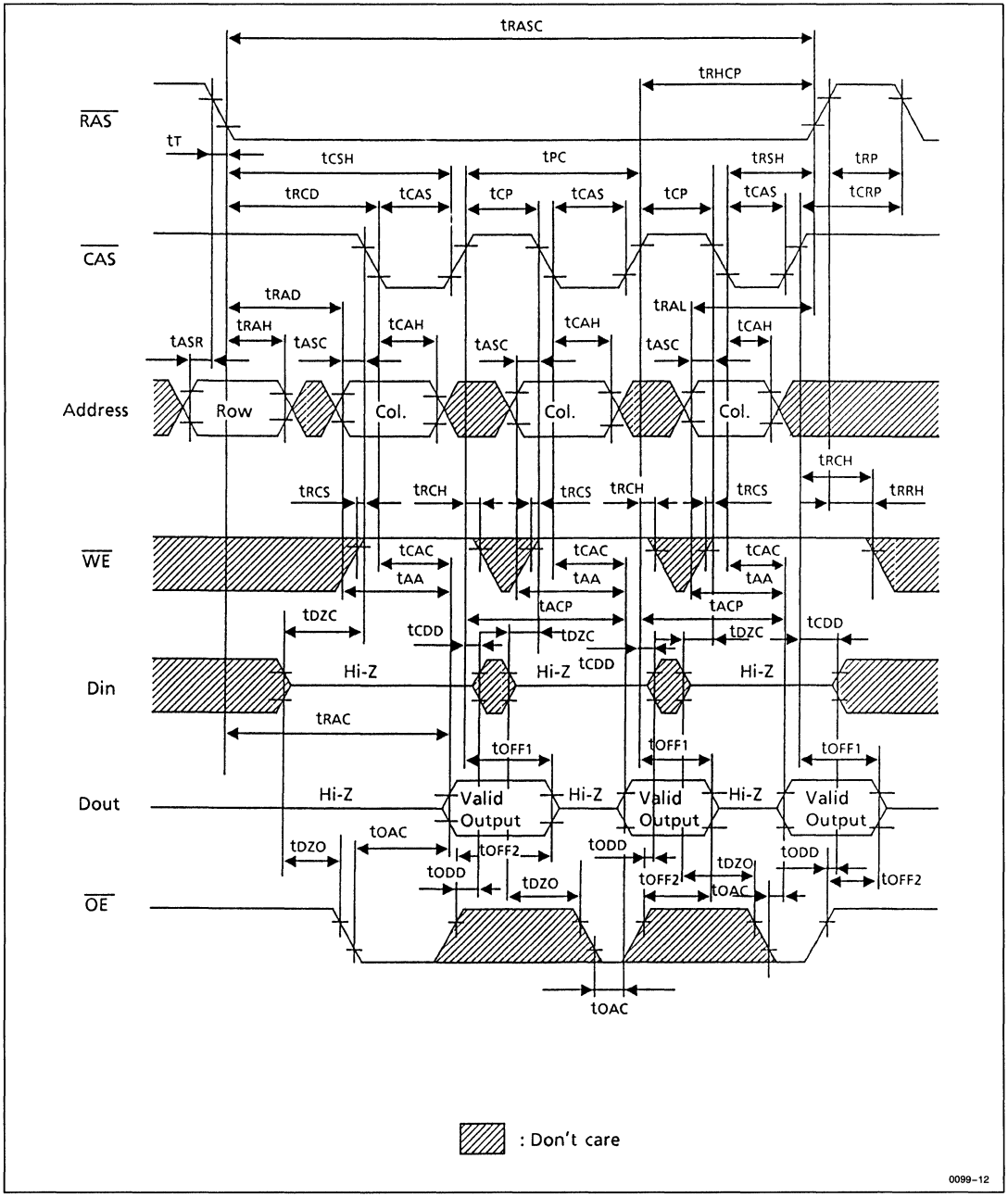
• **$\overline{RAS}$ Only Refresh Cycle**



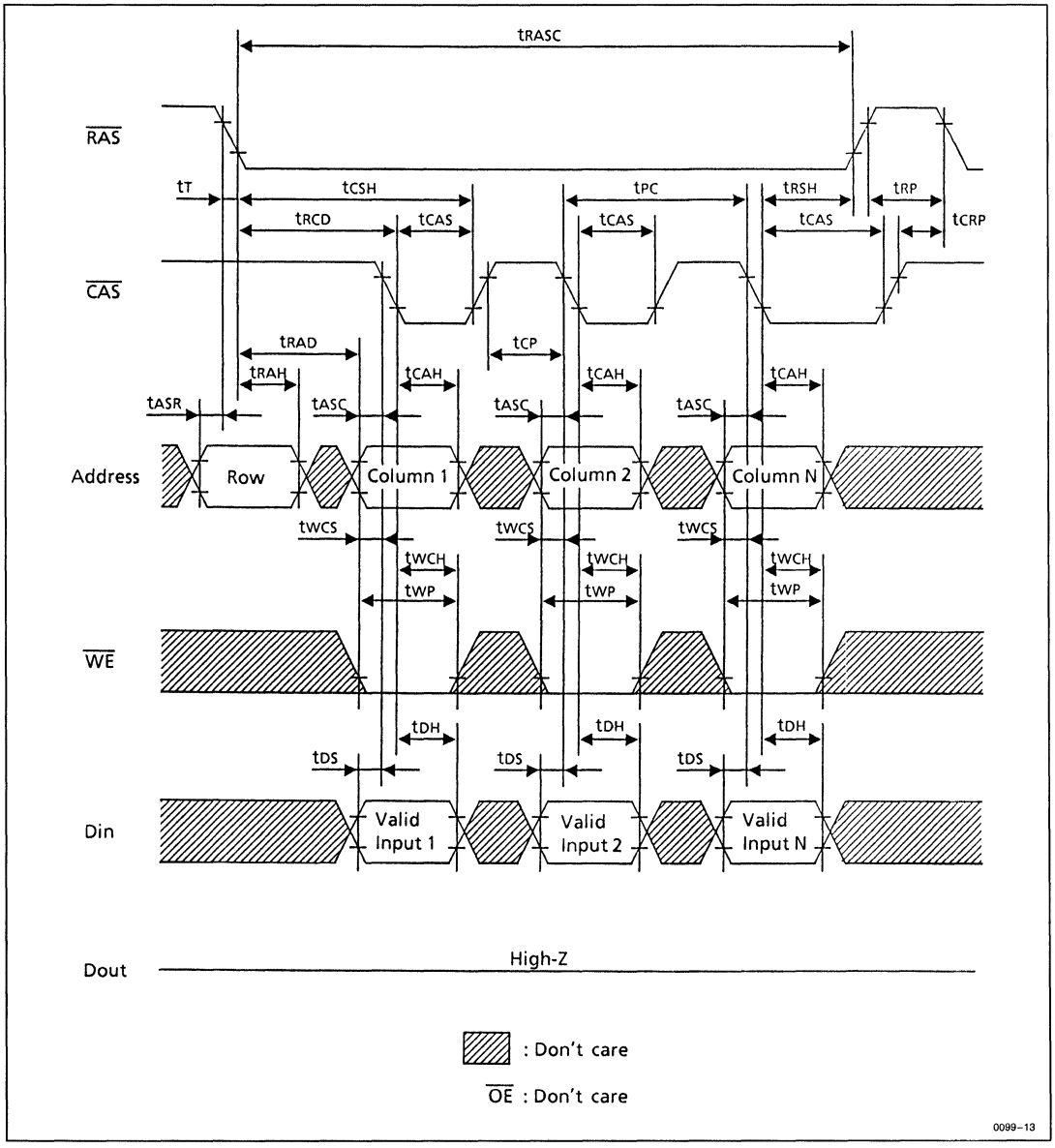
• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**



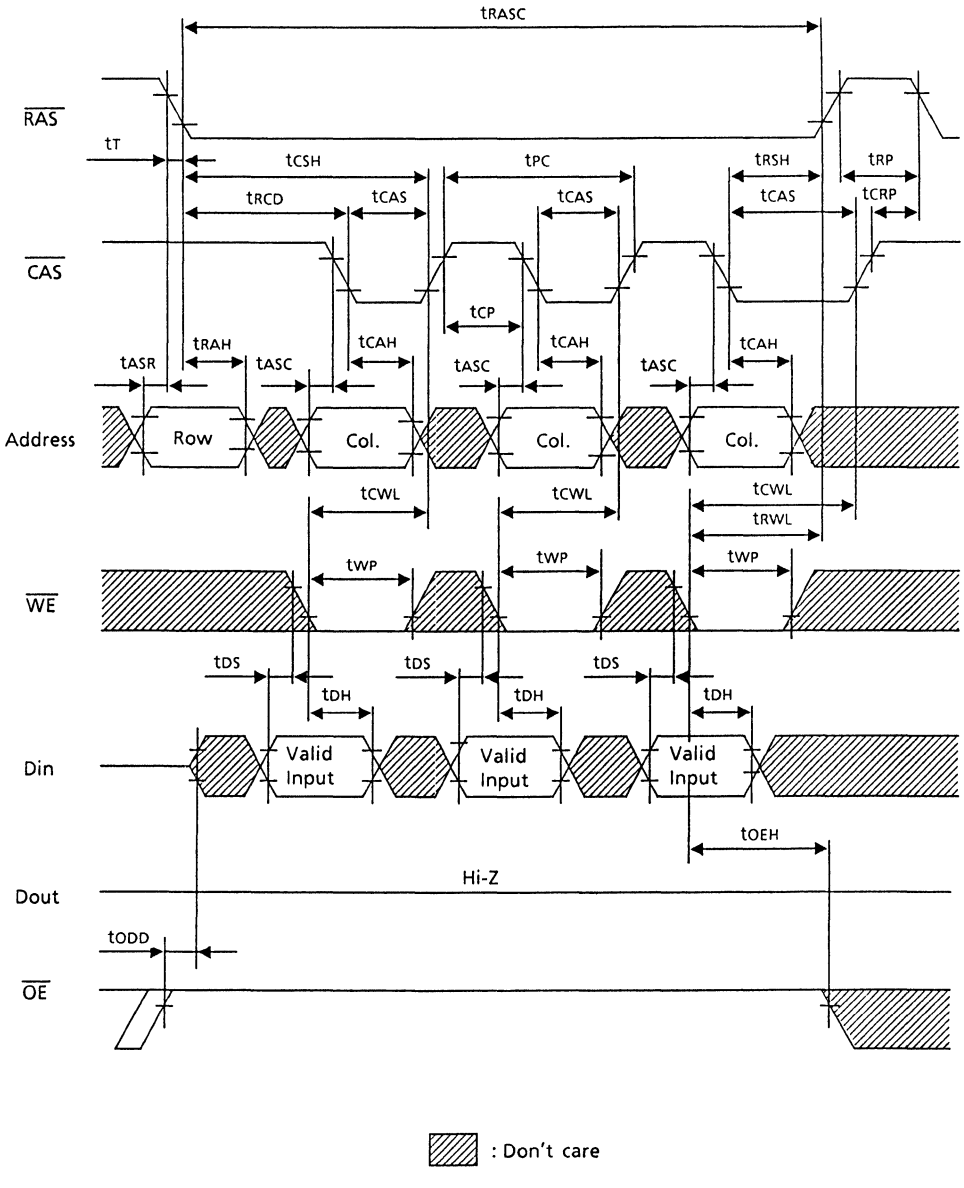
• Fast Page Mode Read Cycle



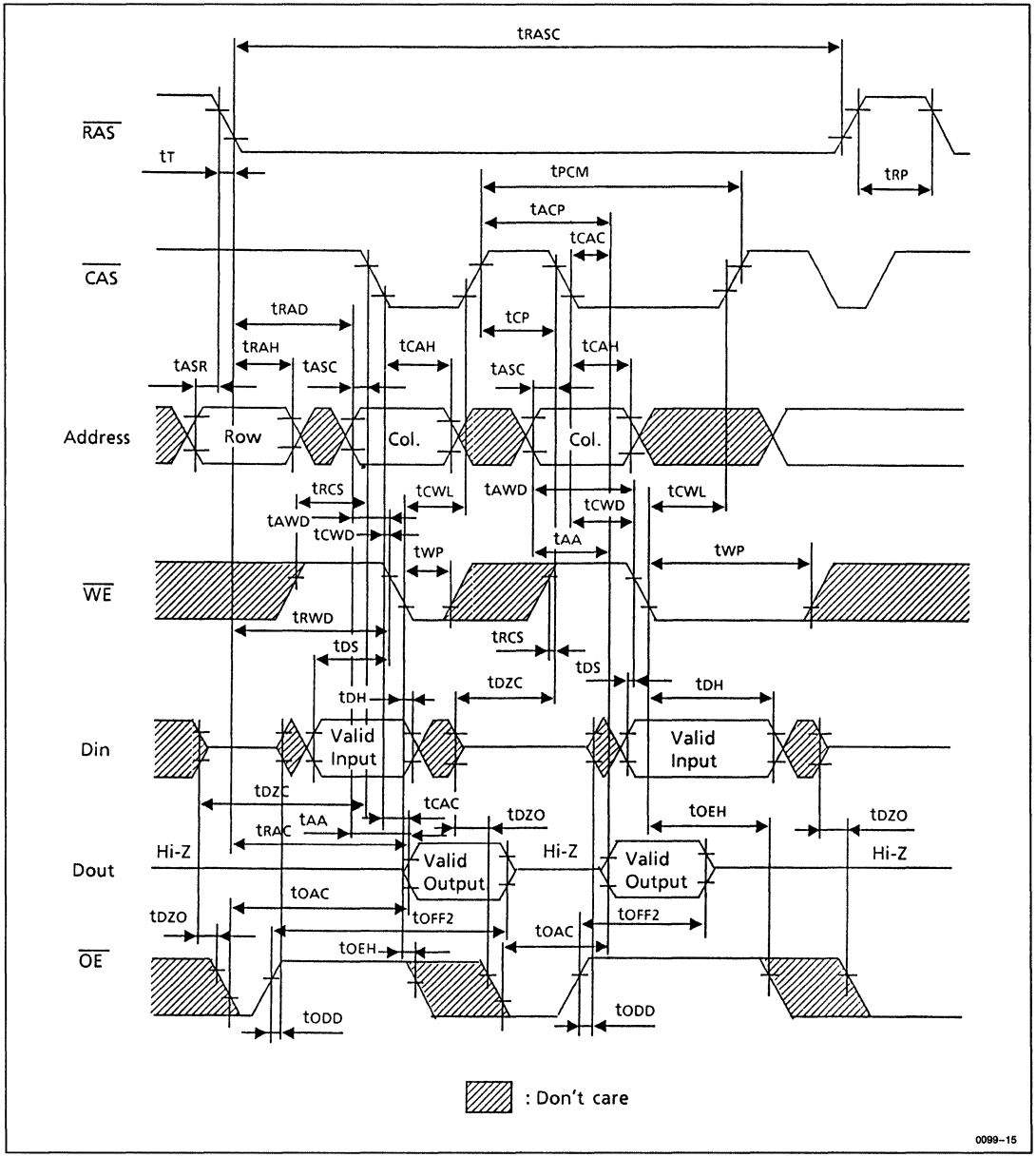
• **Fast Page Mode Early Write Cycle**



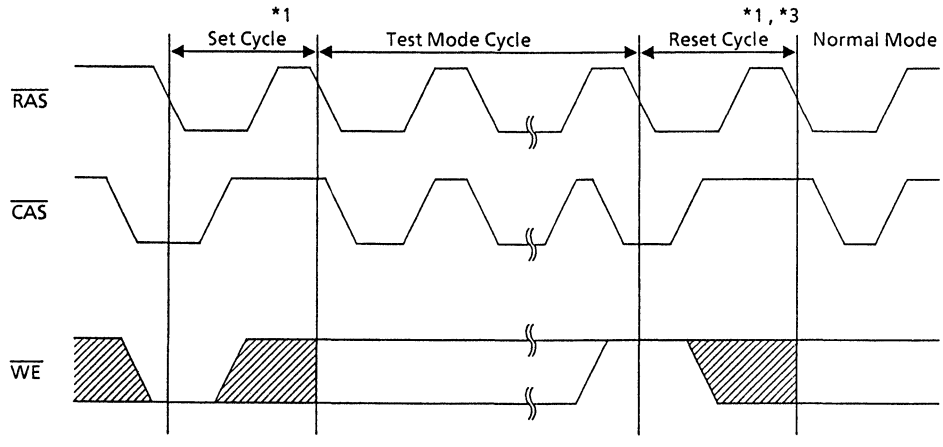
• **Fast Page Mode Delayed Write Cycle**



• **Fast Page Mode Read-Modify-Write Cycle**



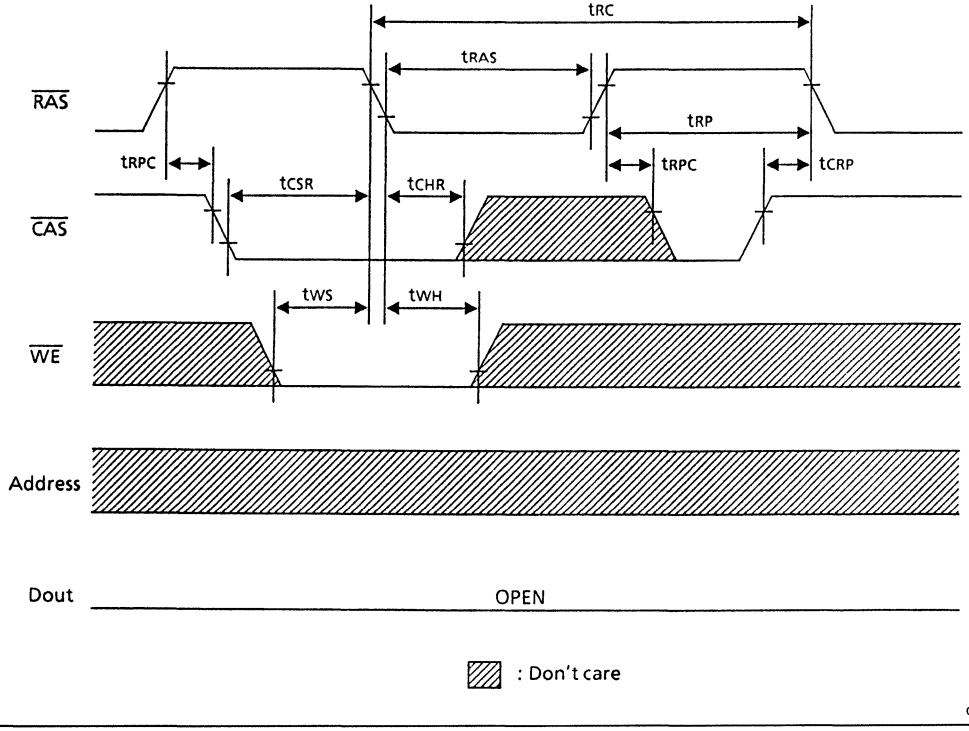
• **TEST MODE CYCLE**



Note *1 CBR or RAS-only refresh
*2 ▨: Don't care
*3 Address, Din, OE : Don't care

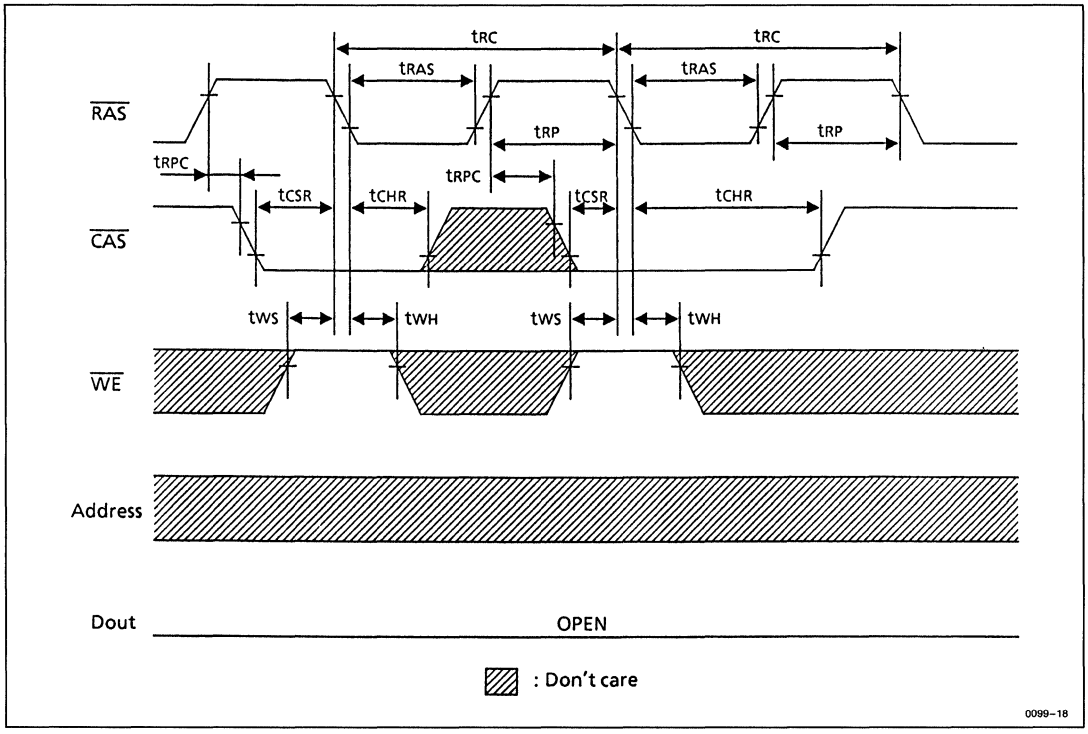
0099-16

• **(1) Test Mode Set Cycle**

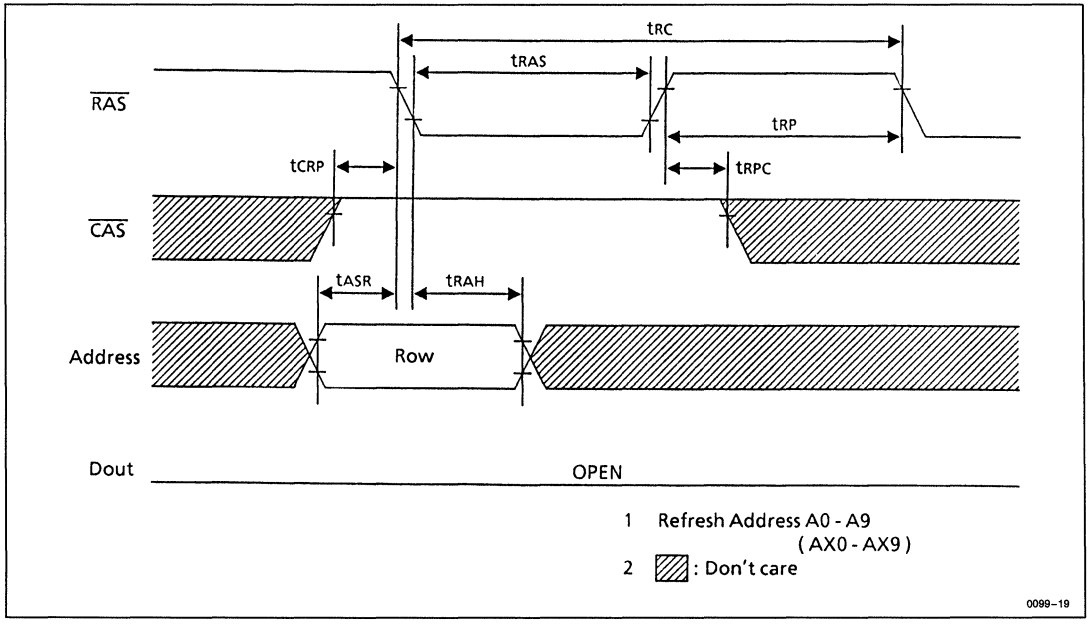


0099-17

• (2) Test Mode Reset Cycle
CAS Before RAS Refresh Cycle



RAS Only Refresh Cycle



Section 5
Video RAM

5

HITACHI®

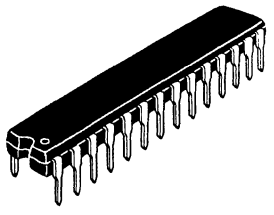
HM63021 Series

2048-Word x 8-Bit Line Memory

■ DESCRIPTION

HM63021 is a 2048-word x 8-bit static Serial Access Memory (SAM) with separate data inputs and outputs. Since it has an internal address counter, no external address signal is required and internal addresses are scanned serially. Using five different address scan modes, it is applicable to FIFO memories, double-speed conversions, 1H delay lines and 1H/2H delay lines for digital TV signals. Its minimum cycle times are 28 ns and 34 ns each corresponding to 8 fsc of PAL TV signals and NTSC TV signals. All intputs and outputs are TTL-compatible. This device is packaged in a 300 mil dual-in-line plastic package.

HM63021 Series



3DDP28N

(DP-28N)

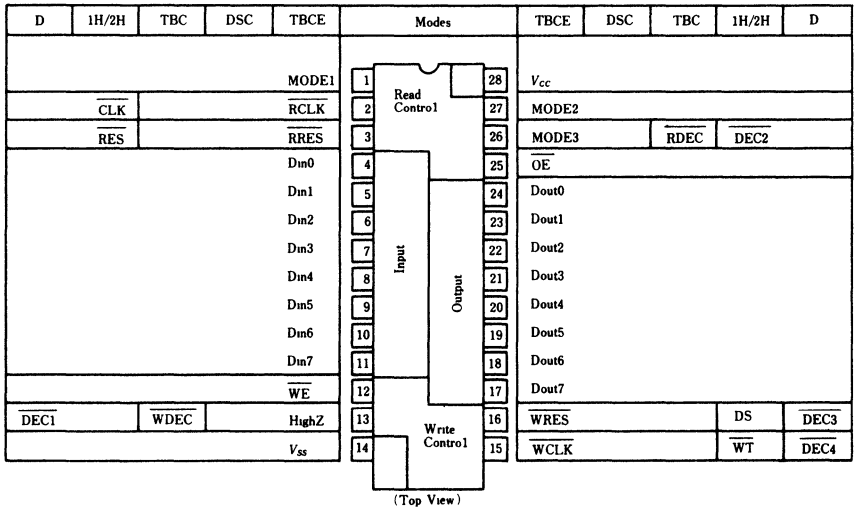
■ FEATURES

- Five Modes for Various Applications
- Corresponds to Digital TV System with 4 fsc Sampling (PAL, NTSC)
- Decoder Signal Output Pin; Fewer External Circuits
- Asynchronous Read/Write Operation;
  - Separate Address Counter for Read/Write
  - No Address Input Required
- High Speed; Cycle Time .....28 ns/34 ns/45 ns (min)
- Completely Static Memory; No Refresh Required
- 8-bit SAM with Separate I/O
- Low Power .....250 mW typ. Active
- Single 5V Supply
- TTL Compatible

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM63021P-28	28 ns	300 mil 28-pin
HM63021P-34	34 ns	Plastic DIP
HM63021P-45	45 ns	(DP-28N)

■ PIN OUT



0106-1

■ PIN DESCRIPTION

Pin No.	Pin Name	Function
1	MODE1	Mode Input 1 (All Modes)
1	$\overline{RCLK}/\overline{CLK}$	Read Clock Input (TBCE, DSC, TBC) Clock Input (1H/2H, D)
3	$\overline{RRES}/\overline{RES}$	Read Reset Input (TBCE, DSC, TBC) Reset Input (1H/2H, D)
4–11	D_{in0}–D_{in7}	Data Input (All Modes)
12	$\overline{WE}$	Write Enable Input (All Modes)
13	High Z/$\overline{WDEC}/\overline{DEC1}$	High Impedance (TBCE, DSC) Write Decode Pulse Output (TBC) Decode Pulse Output 1 (1H/2H, D)
14	V_{SS}	Ground (All Modes)
15	$\overline{WCLK}/\overline{WT}/\overline{DEC4}$	Write Clock Input (TBCE, DSC, TBC) Write Timing Input (1H/2H) Decode Pulse Output 4 (D)
16	$\overline{WRES}$/DS/$\overline{DEC3}$	Write Reset Input (TBCE, DSC, TBC) Delay Select Input (1H/2H) Decode Pulse Output 3 (D)
17–24	D_{out0}–D_{out7}	Data Outputs (All Modes)
25	$\overline{OE}$	Output Enable Input (All Modes)
26	MODE3/$\overline{RDEC}/\overline{DEC2}$	Mode Input 3 (TBCE) Read Decode Pulse Output (TBC) Decode Pulse Output 2 (1H/2H, D)
27	MODE2	Mode Input 2 (All Modes)
28	V_{CC}	Power Supply (+ 5V) (All Modes)

■ MODE TABLE

Mode Signals			Mode	Application Example	Note
MODE1	MODE2	MODE3			
H	H	H	Time Base Compression/Expansion (TBCE)	Picture in Picture	
H	H	L	Double Speed Conversion (DSC)	Non Interface	
H	L	—	Time Base Correction (TBC)	Time Base Corrector	1
L	H	—	1H/2H Delay (1H/2H)	Vertical Filter	1
L	L	—	Delay Line (D)	Delay Line	1

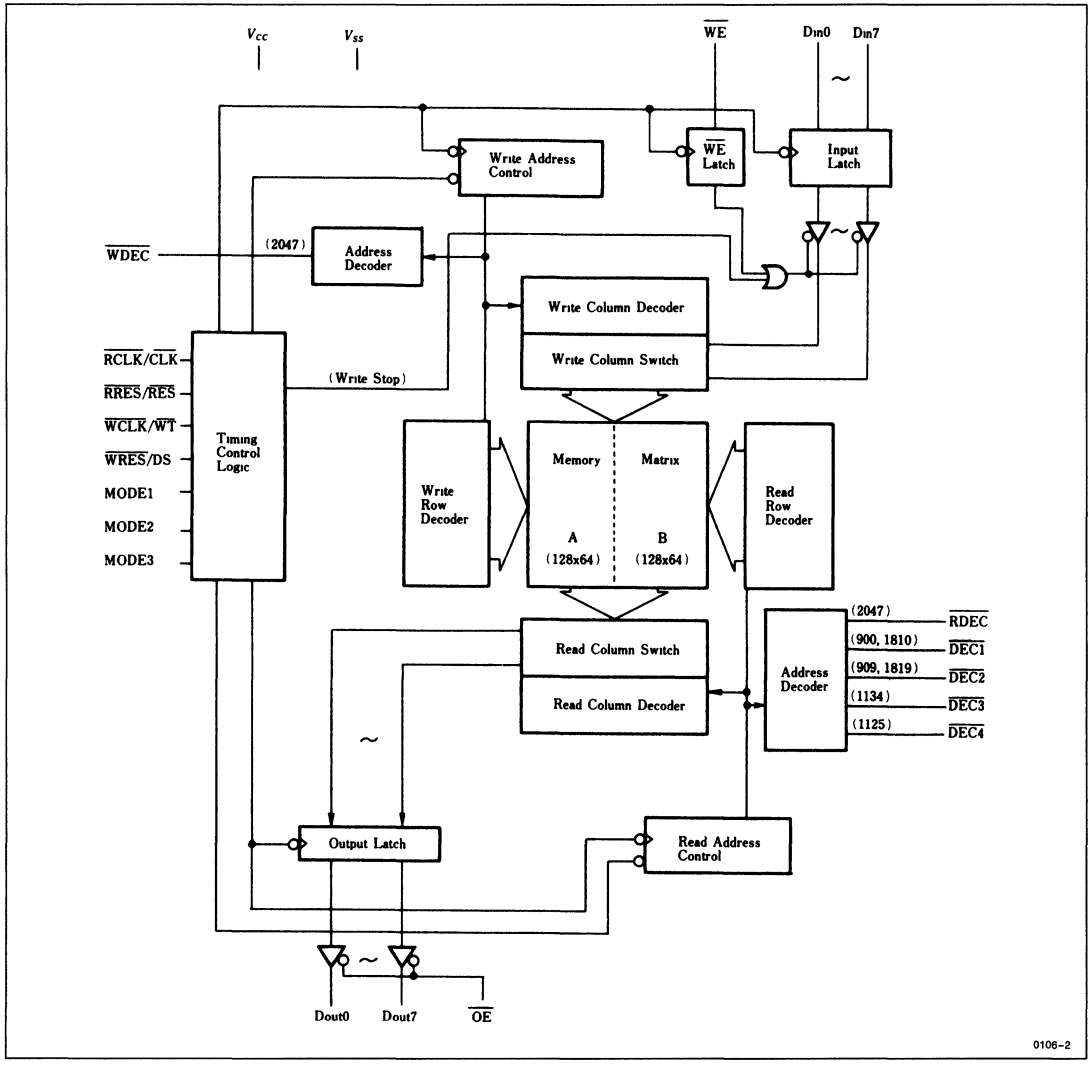
Note: 1. Decoder Output Signal ($\overline{RDEC}$, $\overline{DEC2}$).

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Notes
Voltage on Any Pin Relative to V_{SS}	V_T	− 0.5 to + 7.0	V	1
Power Dissipation	P_T	1.0	W	
Operating Temperature	T_{opr}	0 to + 70	°C	
Storage Temperature	T_{stg}	− 55 to + 125	°C	
Storage Temperature Under Bias	T_{bias}	− 10 to + 85	°C	

Note: 1. − 3.5V for pulse width ≤ 10 ns.

■ BLOCK DIAGRAM



■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input Voltage	V_{IH}	2.4	—	6.0	V	
	V_{IL}	−0.5	—	0.8	V	1

Note: 1. −3.0V for pulse width ≤ 10 ns.

• DC and Operating Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input Leakage Current	$\|I_{LI}\|$	—	—	10	µA	V_{CC} = 5.5V V_{in} = V_{SS} to V_{CC}	
Output Leakage Current	$\|I_{LO}\|$	—	—	10	µA	$\overline{OE}$ = V_{IH} V_{out} = V_{SS} to V_{CC}	
Operating Power Supply Current	I_{CC}	—	50	90	mA	Min. Cycle, I_{out} = 0 mA	1
Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA, D_{out0} to D_{out7} $\overline{DEC}$ Output Pin	2
	V_{OH}	2.4	—	—	V	I_{OH} = −4 mA, D_{out0} to D_{out7} Pin	
		2.4	—	—	V	I_{OH} = −1 mA, $\overline{DEC}$ Output Pin	

Notes: 1. Typical values are at V_{CC} = 5V, T_A = 25°C and for reference only.
2. I_{OL} = 6 mA for 45 ns version.

• Capacitance (T_A = 25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions	Note
Input Capacitance	C_{in}	—	—	6	pF	V_{in} = 0V	
Output Capacitance	C_{out}	—	—	9	pF	V_{out} = 0V	2

Notes: 1. This parameter is sampled and not 100% tested.
2. 13, 15–24, 26 pin.

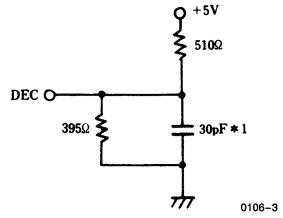
• AC Characteristics (V_{CC} = 5V ±10%, T_A = 0 to +70°C, unless otherwise noted.)

AC Test Conditions

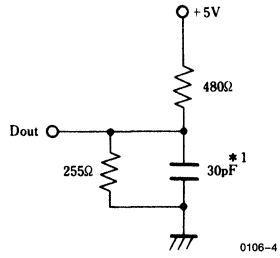
Input and Output Timing Reference Levels: 1.5V
Input Pulse Levels: V_{SS} to 3V
Input Rise and Fall Times: 5 ns

HM63021-28/34

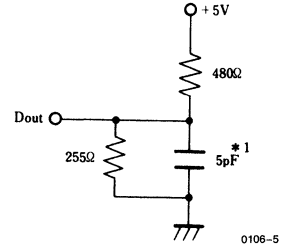
DEC Output Load



D_{out} Output Load (A)



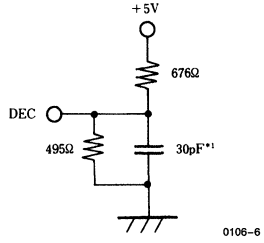
D_{out} Output Load (B) (t_{OLZ}, t_{OHZ})



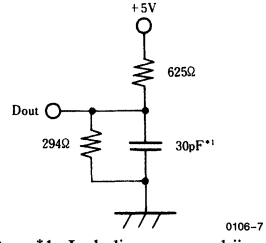
Note: *1. Including scope and jig.

HM63021-45

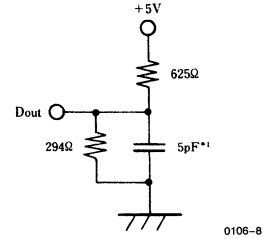
DEC Output Load



D_{out} Output Load (A)



D_{out} Output Load (B) (t_{OLZ}, t_{OHZ})



Note: *1. Including scope and jig.

Read Cycle

Parameter		Symbol	HM63021-28		HM63021-34		HM63021-45		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time		t_{RC}	28	—	34	—	45	—	ns
Read Clock Width		t_{RWL}	10	—	10	—	15	—	ns
		t_{RWH}	10	—	10	—	15	—	ns
Access Time		t_{AC}	—	20	—	25	—	30	ns
Decode Output Access Time	(Fall)	t_{DA1}	—	20	—	25	—	30	ns
	(Rise)	t_{DA2}	—	40	—	50	—	60	ns
Output Hold Time		t_{OH}	5	—	5	—	5	—	ns
Decode Output Hold Time	(Fall)	t_{DOH1}	5	—	5	—	5	—	ns
	(Rise)	t_{D0H2}	5	—	5	—	5	—	ns
Output Enable Access Time		t_{OE}	—	20	—	25	—	30	ns
Output Disable to Output in High Z		t_{OHZ}	0	15	0	20	0	25	ns
Output Enable to Output in Low Z		t_{OLZ}	5	—	5	—	5	—	ns

Write Cycle

Parameter	Symbol	HM63021-28		HM63021-34		HM63021-45		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	28	—	34	—	45	—	ns
	t_{WC} (1H/2H Mode)	56	—	68	—	90	—	ns
Write Clock Width	t_{WWL}	10	—	10	—	15	—	ns
	t_{WWH}	10	—	10	—	15	—	ns
Input Data Setup Time	t_{DS}	5	—	5	—	7	—	ns
Input Data Hold Time	t_{DH}	5	—	5	—	7	—	ns
$\overline{WE}$ Setup Time	t_{WESL}	5	—	5	—	7	—	ns
	t_{WESH}	5	—	5	—	7	—	ns
$\overline{WE}$ Hold Time	t_{WEHL}	5	—	5	—	7	—	ns
	t_{WEHH}	5	—	5	—	7	—	ns
$\overline{WT}$ Setup Time	t_{WTSL}	5	—	5	—	7	—	ns
	t_{WTSH}	5	—	5	—	7	—	ns
$\overline{WT}$ Hold Time	t_{WTHL}	5	—	5	—	7	—	ns
	t_{WTHH}	5	—	5	—	7	—	ns

Reset Cycle

Parameter	Symbol	HM63021-28		HM63021-34		HM63021-45		Unit
		Min	Max	Min	Max	Min	Max	
Reset Setup Time	t_{RES}	8	—	9	—	10	—	ns
Reset Hold Time	t_{REH}	5	—	5	—	7	—	ns
Clock Setup Time Before Reset	t_{REPS}	8	—	9	—	10	—	ns
Clock Hold Time Before Reset	t_{REPH}	5	—	5	—	7	—	ns

Mode Description

- Time Base Compression/Expansion Mode

  This mode turns HM63021 into a 2048-word x 8-bit FIFO memory with asynchronous input/output. The HM63021 provides 2 clocks ($\overline{RCLK}$, $\overline{WCLK}$) and 2 resets ($\overline{RRES}$, $\overline{WRES}$), one each for read and write. The internal address counters increment by 1 address clock and are reset to address 0. A write-inhibit function of HM63021 stops writing automatically after the data has been written into all addresses 0 to 2047. The write-inhibit function is released by reset using $\overline{WRES}$, and the HM63021 restarts writing into address 0.

- Double-Speed Conversion Mode

  This mode turns HM63021 into a 1024-word x 8-bit x 2 memory with asynchronous input/output. It is used for generating non-interlaced TV signals. When the original signal and the interpolated signal (1 field delay) of interlaced signls are input to the HM63021, multiplexed per dot, it outputs non-interlaced signals for each line. 8 fsc should be input to $\overline{RCLK}$ and $\overline{WCLK}$. A standard H synchronizing signal and a non-interlace H synchronizing signal are input to $\overline{WRES}$ and $\overline{RRES}$ respectively. A write-inhibit function is provided in this mode, making it applicable to PAL TV, where extra data (1135−1024 = 111 bits) is ignored.

- TBC Mode

  This mode turns HM63021 into 2048-word x 8-bit FIFO memory with asynchronous input/output. The HM63021 provides 2 clocks ($\overline{RCLK}$, $\overline{WCLK}$) and 2 resets ($\overline{RRES}$, $\overline{WRES}$), one each for read and write. The internal address counters increment by 1 address at each clock and are reset to address 0. The internal address counters return to address 0 after they reach address 2047. The HM63021 outputs a write decode pulse from $\overline{WDEC}$, synchronizing it with address 2047 in the write address counter, and read a decode pulse from $\overline{RDEC}$, synchronizing with address 2047 in the read address counter. Using these pulses, the memory area can be extended easily (multiple-HM63021s can be used with ease).

- 1H/2H Delay Mode

  This mode turns HM63021 into a 1024-word x 8-bit x 2 delay line with synchronous input/output. Delay time is defined by the reset period of $\overline{RES}$. Since the HM63021 outputs a 901 decode pulse ($\overline{DEC1}$) and a 910 decode pulse ($\overline{DEC2}$), connecting $\overline{DEC2}$ to $\overline{RES}$, for example, outputs 1H- and 2H- delayed signals alternately at a 8- fsc cycle when the original signal is input at a 4- fsc cycle. A write-inhibit function is provided in this mode, making it applicable to PAL TV, where extra data (1135−1024 = 111 bits) is ignored.

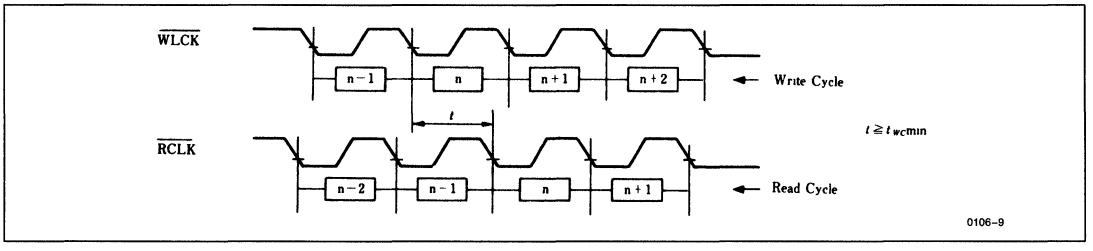
- Delay Line Mode

  This mode turns HM63021 into a 2048-word x 8-bit delay line with synchronous input/output. Delay time (3 to 2048 bits) is defined by the reset period of $\overline{RES}$. The delay is 2048 bits when $\overline{RES}$ is fixed High. Signals delayed by 910 bits to 1135 bits for example, can be easily obtained without external circuits by just connecting selected decoded pulses on $\overline{DEC1}$–$\overline{DEC4}$ to $\overline{RES}$.

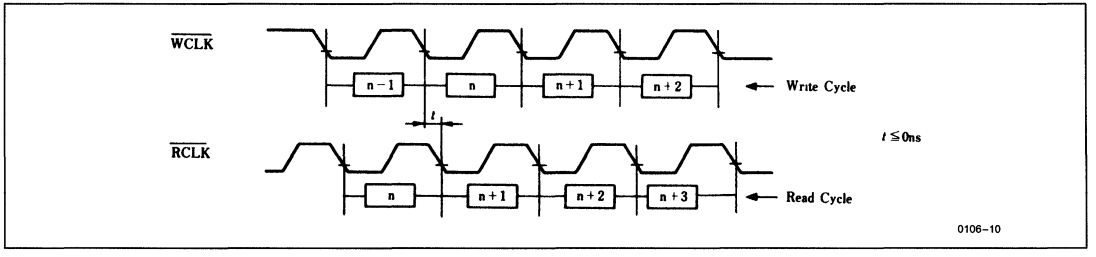
Notes on Using HM63021

- Hitachi recommends that pin 13 (high impedance) should be fixed by pulling up or down with a resistor (of several kΩ) in TBC or DSC mode.
- Hitachi recommends that the mode signal input pins and DS pin should be fixed by pulling them up or down with a resistor (of several kΩ).
- Data integrity cannot be guaranteed when mode is changed during operation.
- When a read address coincides with a write address in TBCE, TBC or DSC mode, the data is written correctly but it is not always read correctly.

(1) Read after Write (3 bits delay)



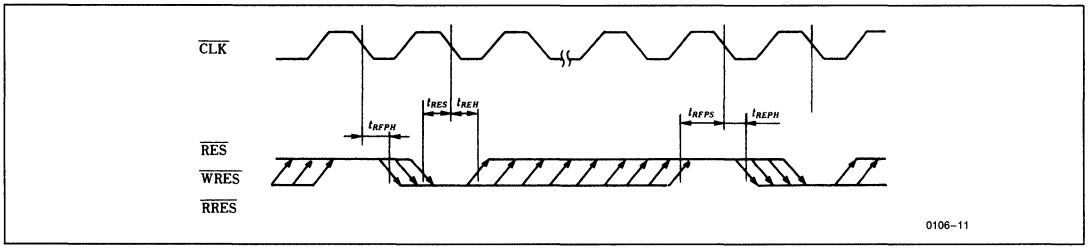
(2) Write after Read (2048 bits delay)



- At power on, the output of the address counter is not defined. Therefore, operations before the system is reset cannot be guaranteed, and decode signal output is not defined until after the first reset cycle.
- The decode signal is latched by a decode output latch circuit at the previous address of the internal counter address and is output synchronized with the next address. For example, $\overline{WDEC}$ in TBC mode is latched at write address 2046 and is output at write address 2047. If a write reset is performed on address 2047 at this time, the write address becomes 0 and $\overline{WDEC}$ is output.

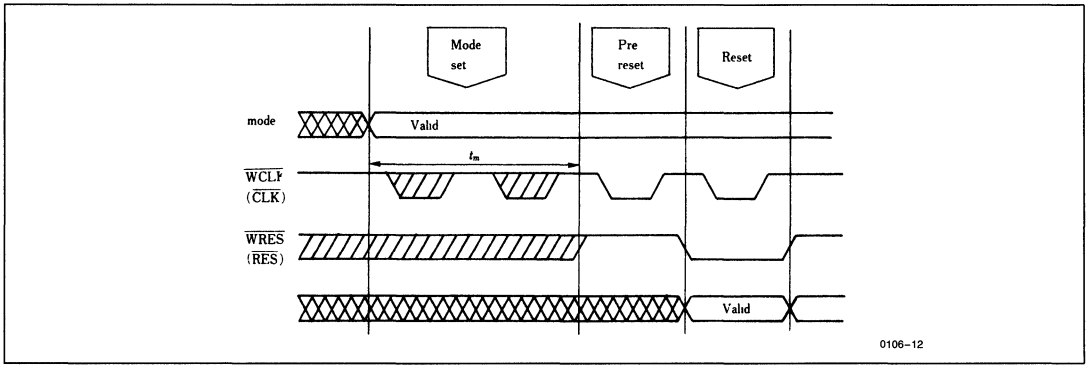
  The same operation is performed in other modes.

- In the reset cycle, the input levels of $\overline{WRES}$, $\overline{RRES}$, $\overline{RES}$ are raised to satisfy t_{REH}, and are fixed high until t_{REPH} in the next pre-reset cycle is satisfied. The rise timings of the reset signals ($\overline{RES}$, $\overline{WRES}$, $\overline{RRES}$) are optionals provided that the t_{REPS} specification is satisfied. The timings at which $\overline{RES}$, $\overline{WRES}$, and $\overline{RRES}$ fall after preset are also optional, provided that the t_{REPH} and t_{RES} specifications are satisfied.

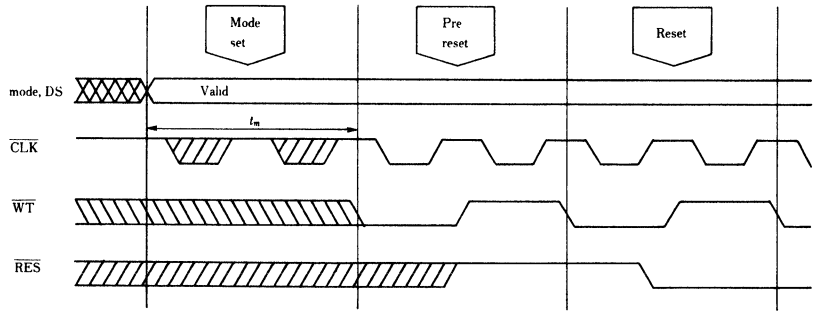


- Hitachi recommends that t_m (time between mode set and the first cycle (Pre-reset)) should be kept for 2 cycle time (56 ns/68 ns/90 ns) or more while the power supply is on.

(1) TBCE, TBC, DSC and Delay Line Mode



(2) 1H/2H Delay Mode



Note: When mode pins are fixed with V_{CC}, GND in mode set while the power supply in on, t_m spec is not needed.

Decode Signal

When internal address counter reaches the specified address as shown below, decode outputs become low.

Mode	Pin No.	Pin Name	Internal Address Counter	Timing of the Output Signal	Operation
TBC	13	$\overline{\text{WDEC}}$	Write 2047	After Write 2047	Completion of Writing on all bits is detected.
	26	$\overline{\text{RDEC}}$	Read 2047	Output of 2046	Completion of Reading from all bits is detected.
1H/2H	13	$\overline{\text{DEC1}}$	Read 900 (2H)	Output of 900 (1H)	By inputting this signal to pin #3, 901/1802-bit delay output is obtained.
	26	$\overline{\text{DEC2}}$	Read 909 (2H)	Output of 909 (1H)	By inputting this signal to pin #3, 910/1820-bit delay output is obtained.
Delay Line	13	$\overline{\text{DEC1}}$	Read 900	Output of 899	By inputting this signal to pin #3, 901-bit delay output is obtained.
			Read 1810	Output of 1809	By inputting this signal to pin #3 after the frequency of $\overline{\text{DEC1}}$ is divided into two, 1811-bit delay output is obtained.
	26	$\overline{\text{DEC2}}$	Read 909	Output of 908	By inputting this signal to pin #3, 910-bit delay output is obtained.
			Read 1819	Output 1818	By inputting this signal to pin #3 after the frequency of $\overline{\text{DEC2}}$ is divided into two, 1820-bit delay output is obtained.
	16	$\overline{\text{DEC3}}$	Read 1134	Output 1133	By inputting this signal to pin #3, 1135-bit delay output is obtained.
	15	$\overline{\text{DEC4}}$	Read 1125	Output 1124	By inputting this signal to pin #3, 1126-bit delay output is obtained.

Note: 1. When counter is reset by Reset Signal ($\overline{\text{RRES}}$, $\overline{\text{RES}}$, $\overline{\text{WRES}}$), address becomes 0.

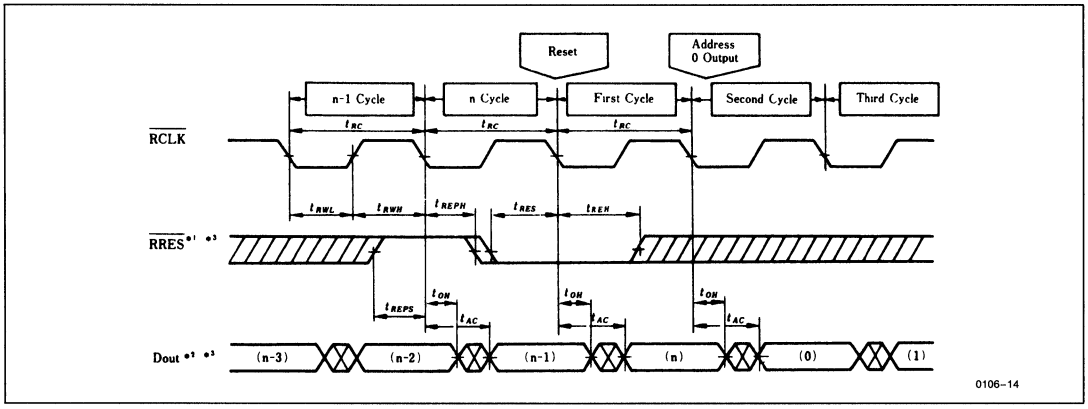
Write-Inhibit Function

When internal address counter is as follows, writing is inhibited automatically for the next cycle. the write-inhibit function is cancelled by reset through $\overline{\text{WRES}}$ or $\overline{\text{RES}}$.

Mode	Write-Inhibit Function (Internal Counter Address)
TBCE	Write-inhibit after address 2047
DSC	Write-inhibit after address 1023 x 2
TBC	No function
1H/2H	Write-inhibit after address 1023
D	No function

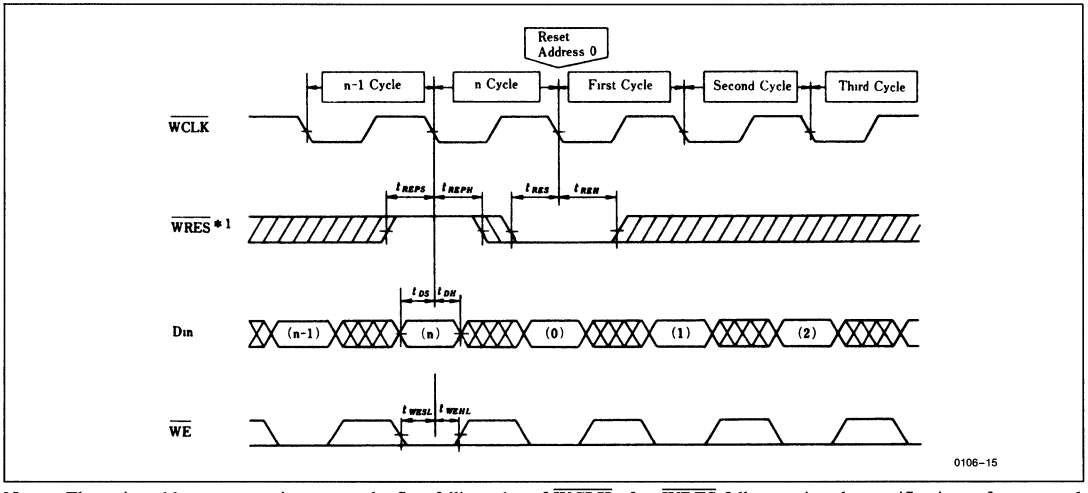
Note: When address counter is reset by $\overline{\text{WRES}}$ or $\overline{\text{RES}}$, address becomes 0.

Read Reset Cycle (TBCE, TBC Modes)



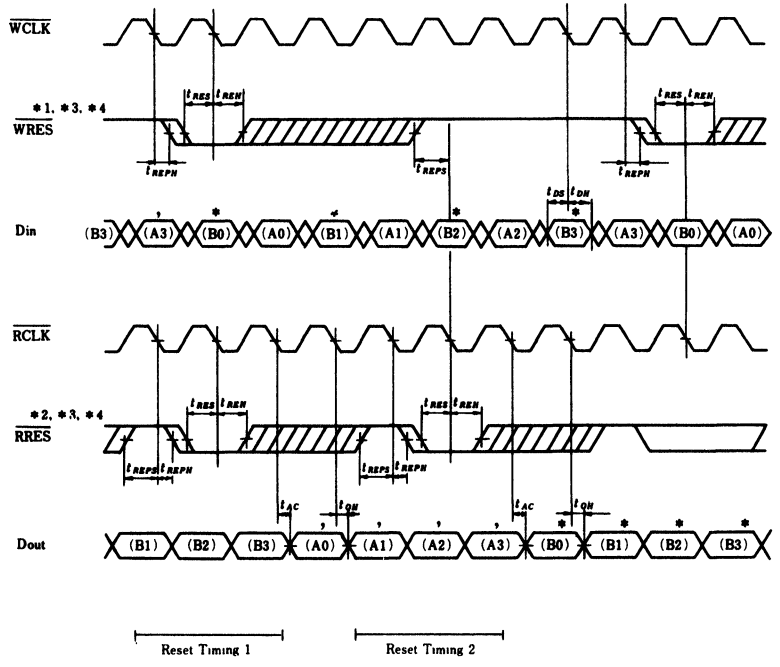
Notes: *1. The read address counter is reset at the first falling edge of $\overline{RCLK}$ after $\overline{RRES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{RCLK}$ even if $\overline{RRES}$ is kept low.
When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed.
*2. Output is from the read address of the previous cycle.
*3. When $\overline{RRES}$ is fixed high, the data at the read address counter is reset after the data of address 2047 is output, and the same operation restarts.

Write Reset Cycle (TBCE, TBC Modes)



Note: The write address counter is reset at the first falling edge of $\overline{WCLK}$ after $\overline{WRES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{WCLK}$ even if $\overline{WRES}$ is kept low.
When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed.

Reset Cycle (DSC Modes)



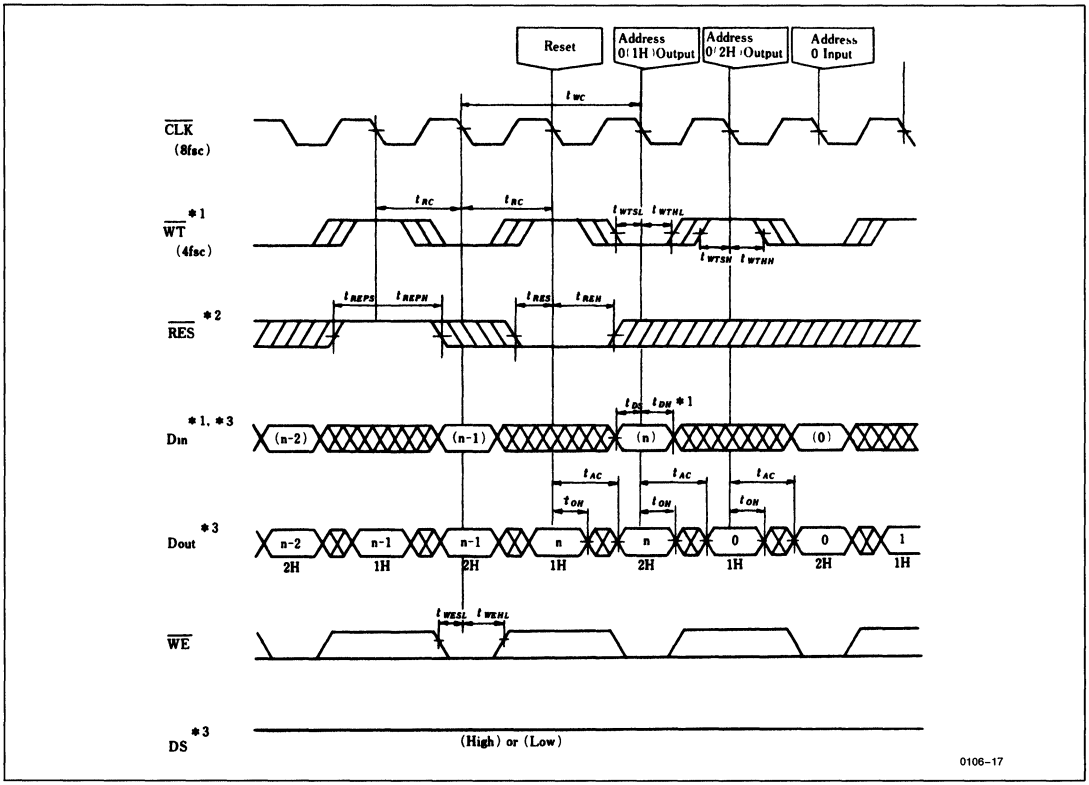
Notes: *1. The write address counter is reset at the first falling edge of $\overline{WCLK}$ after $\overline{WRES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{WCLK}$ even if $\overline{WRES}$ is kept low.
When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed.

*2. The read address counter is reset at the first falling edge of $\overline{RCLK}$ after $\overline{RRES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{RCLK}$ even if $\overline{RRES}$ is kept low.
When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed.

*3. When t_{REPH}, t_{RES}, t_{REH} ($\overline{WRES}$ to $\overline{WCLK}$), or t_{REPS}, t_{REPH}, t_{RES}, t_{REH} ($\overline{PRES}$ to $\overline{RCLK}$) cannot meet the specifications, the output of video signal A is not guaranteed. (Reset Timing I).

*4. When t_{REPS} (WRES to $\overline{RCLK}$), or t_{RES}, t_{REH}, t_{REPS}, t_{REPH} ($\overline{PRES}$ to $\overline{RCLK}$) cannot meet the specifications, the interpolation signal B is not guaranteed. (Reset Timing II).

Reset Cycle (1H/2H Mode)

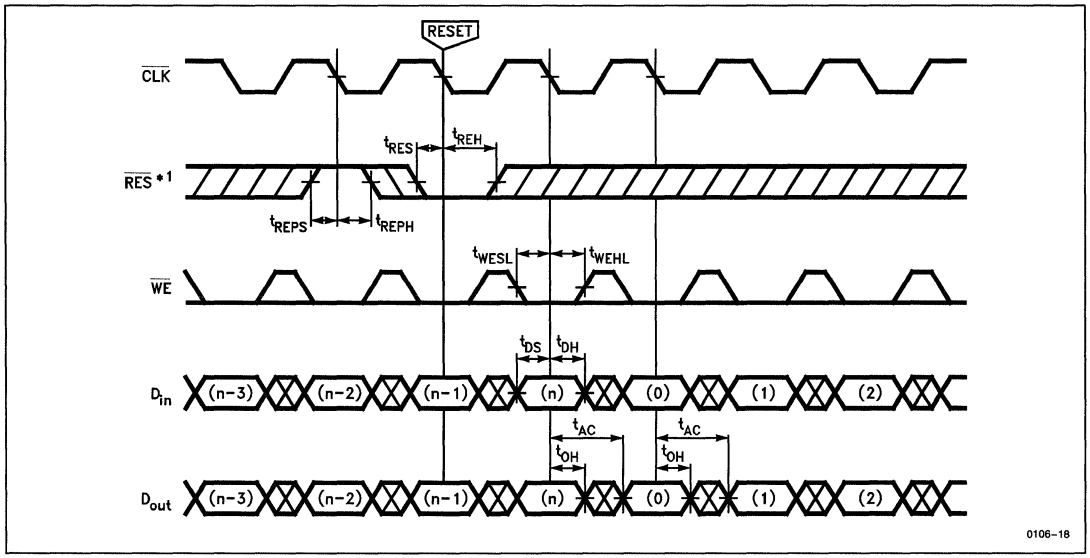


Notes: *1. $\overline{WT}$ is the input during half cycle of $\overline{CLK}$, meeting the specifications of t_{WTSL}, t_{WTHL}, t_{WTSH}, and t_{WTHH}. Data is written when $\overline{WT}$ is low. Reset is possible when $\overline{WT}$ is high.

*2. Read address counter is reset at the first falling edge of $\overline{CLK}$ after $\overline{RES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{CLK}$ even if $\overline{RES}$ is kept low.
When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed.

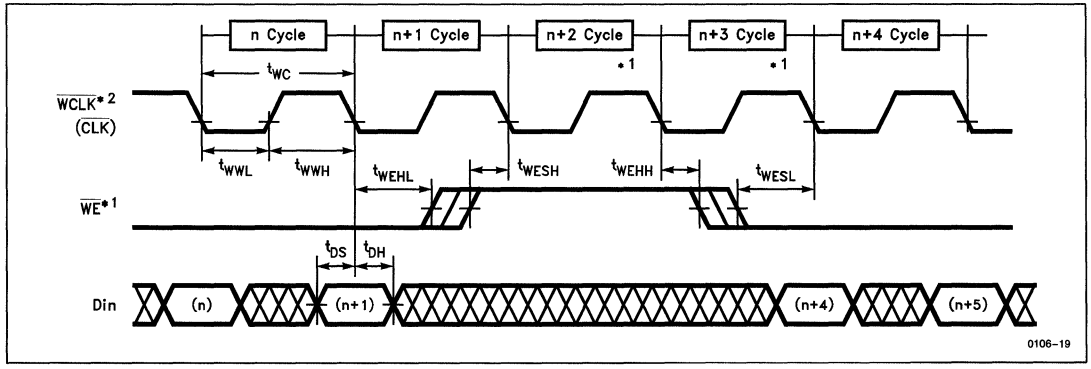
*3. When DS is fixed high, 1H output data is delayed by n bits and 2H output data is delayed by 2n bits where 2n is the reset cycle of $\overline{RES}$.
When DS is fixed low, 1H output data is delayed by n − 5 bits and 2H output data is delayed by 2n − 5 bits.

Reset Cycle (D Mode)



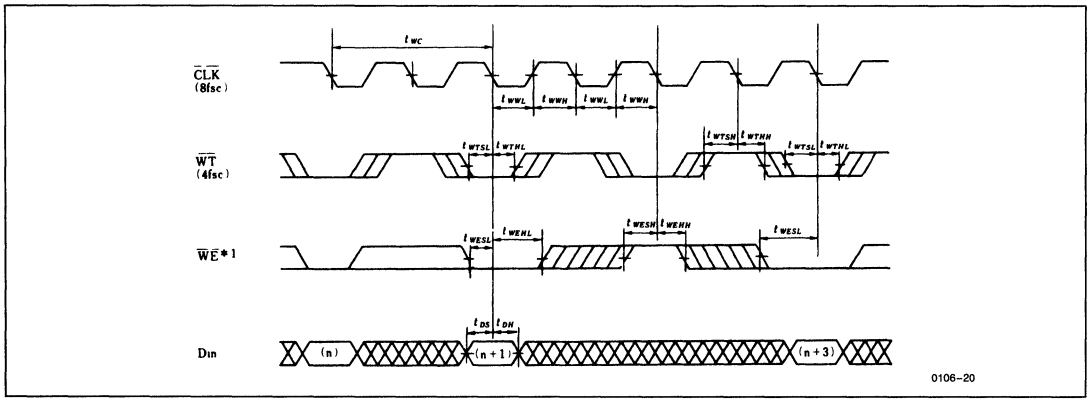
Note: *1. The read address counter is reset at the first falling edge of $\overline{CLK}$ after $\overline{RES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{CLK}$ even if $\overline{RES}$ is kept low.
When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed.

Write Enable (TBCE, DSC, TBC, D Modes)



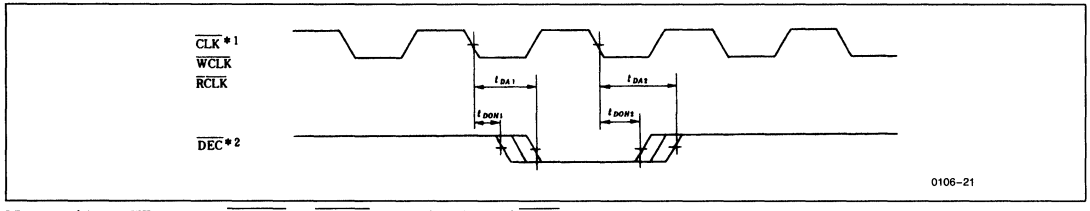
Notes: *1. When t_{WEHL}, t_{WESH}, t_{WEHH}, and t_{WESL} cannot meet the specifications, the write enable operation is not guaranteed.
*2. In the delay line mode, $\overline{CLK}$ takes the place of $\overline{WCLK}$.

Write Enable (1H/2H Mode)



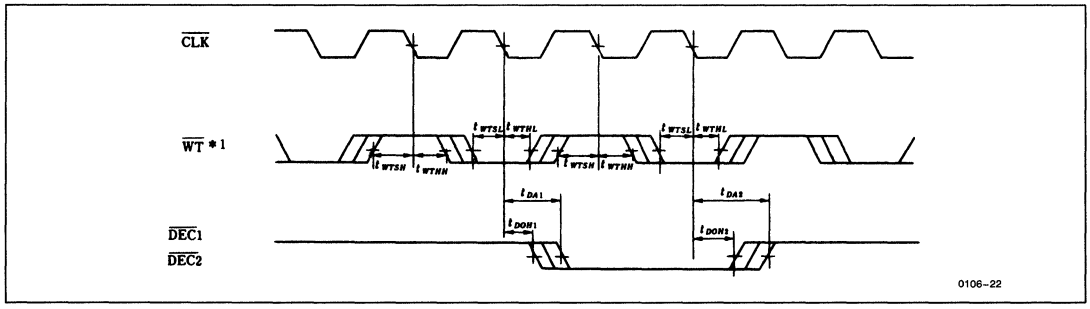
Note: *1. When t_{WTSL}, t_{WTHL}, t_{WEHL}, and t_{WEHH} cannot meet the specifications, the write enbable operation is not guaranteed.

Decode Output (TBC, D Modes)



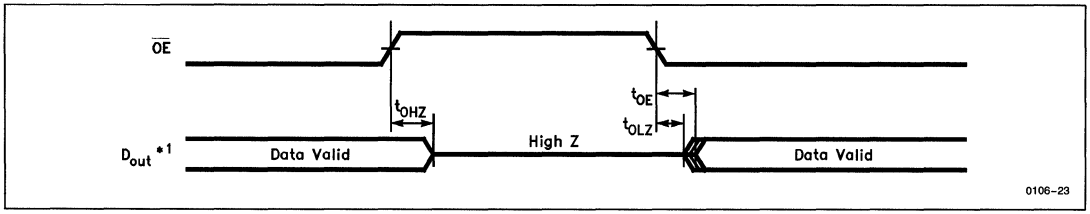
Notes: *1. In TBC mode, $\overline{WCLK}$ or $\overline{RCLK}$ takes the place of $\overline{CLK}$.
*2. $\overline{DEC}$ is $\overline{WDEC}$ or $\overline{RDEC}$ in $\overline{TBC}$, $\overline{DEC1}$, $\overline{DEC2}$, $\overline{DEC3}$ or $\overline{DEC4}$ in D mode.

Decode Output (1H/2H Mode)



Note: *1. When t_{WTSL}, t_{WTHL}, t_{WTSH}, and t_{WTHH} cannot meet the specifications, the decde output operation is not guaranteed.

Output Enable (All Modes)



Note: *1. Transition of t_{OHZ} and t_{WLZ} is measured ±200 mV from steady state voltage with Output Load B. This parameter is sampled and not 100% tested.

HM53051 Series

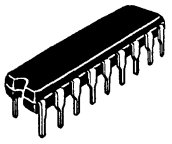
262,144-Word x 4-Bit Frame Memory

■ DESCRIPTION

HM53051P is a 262,144-word x 4-bit frame memory, using the most advanced 1.3 μm CMOS processes. It performs serial access by an internal address generator.

It offers a high-speed cycle time of 45 ns or 60 ns (min). As input data and output data can be written or read in any cycle, synchronized with a system clock, and the delay between data read/write operations is freely settable. Y/C separation and frozen pictures can be realized easily in 4 fsc NTSC digital TV or VCR systems. Also, it enables random access in 32-word x 4-bit data block. With this function, picture in picture or a multiplexed picture can be displayed with ease.

HM53051P Series



3DDP18B

(DP-18B)

■ FEATURES

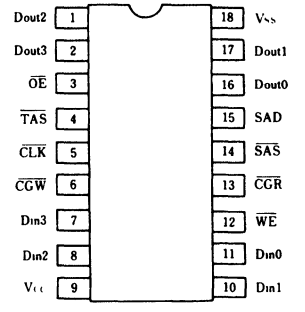
- 262,144-Word x 4-Bit Serial Access Memory
- Organized with Dual Ports
  - Serial Input ..... x 4-Bit
  - Serial Output ..... x 4-Bit
- High Speed
  - Read/Write Cycle Time ..... 45 ns/60 ns (min)
  - Access Time ..... 35 ns/40 ns (max)
- Semi-Synchronous Read/Write Cycle
- Low Power
  - Active: 200 mW (typ)
- Random Access in 32-Word x 4-Bit Blocks
- External Refresh Control is Unnecessary

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM53051P-45 HM53051P-60	45 ns 60 ns	300 mil 18-pin Plastic DIP (DP-18B)

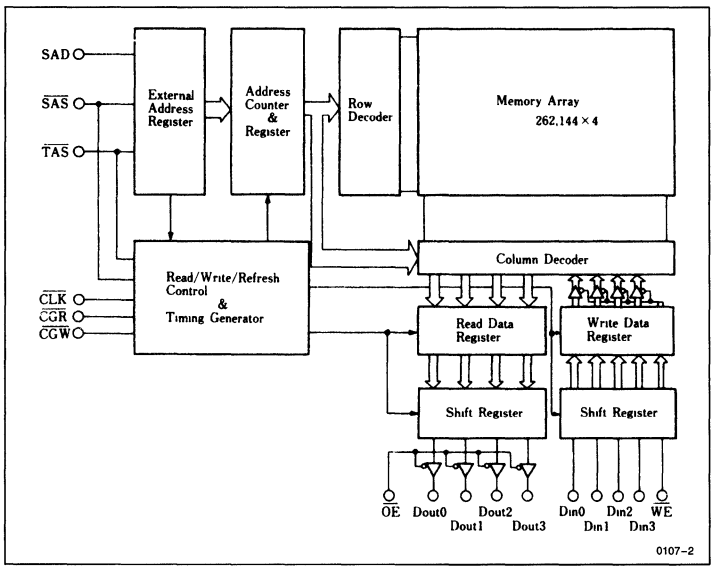
■ PIN OUT

HM53051P Series



(Top View)

■ BLOCK DIAGRAM



■ PIN DESCRIPTION

Pin Name	Function
D_{in}	Data Input
D_{out}	Data Output
$\overline{OE}$	Output Enable
$\overline{TAS}$	Transfer Address Strobe
$\overline{CLK}$	System Clock
$\overline{CGW}$	Clock Gate (Write)
$\overline{CGR}$	Clock Gate (Read)
SAD	Serial Address
$\overline{SAS}$	Serial Address Strobe
$\overline{WE}$	Read/Write Enable

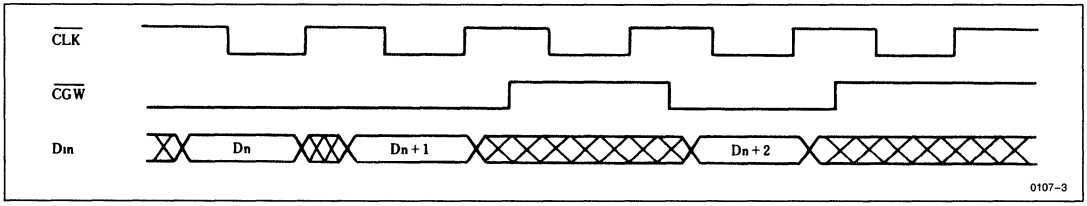
■ FUNCTIONAL DESCRIPTION

• Serial Access Memory with I/O Separated

Read cycle and write cycle of HM53051 can be operated independently synchronized with a system clock. It realizes time compression or expansion for picture in picture in digital TV, for example.

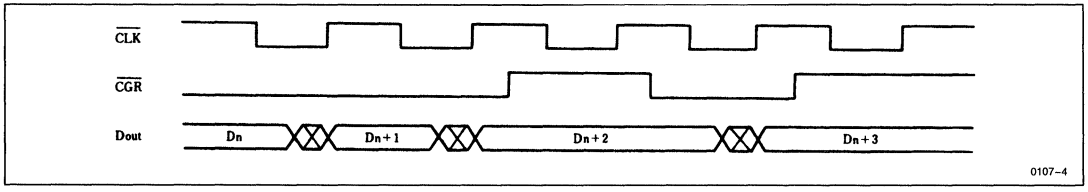
• Write Cycle by $\overline{CGW}$

Write data are taken in at the falling edge of the system clock $\overline{CLK}$ when $\overline{CGW}$ is low. If $\overline{CGW}$ is high, HM53051 does not enter write cycle (cycle time is defined by system clock cycle time). Time is compressed easily with $\overline{CGW}$.



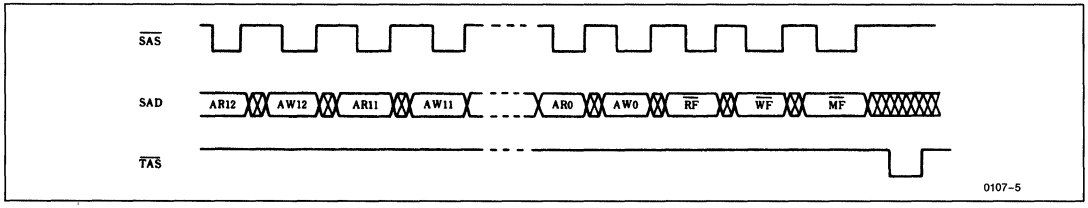
• Read Cycle by $\overline{CGR}$

Read data is output at the falling edge of the system clock $\overline{CLK}$ when $\overline{CGR}$ is low. If $\overline{CGR}$ is high, HM53051 does not enter read cycle (cycle time is defined by system clock time). Time is expanded is realized easily with $\overline{CGR}$.



■ RANDOM ACCESS

The HM53051 is also capable of random access by serial address input, SAD. Random access by the unit of 32-word x 4-bit is performed, when $\overline{TAS}$ is low after read address (AR0–AR12), write address (AW0–AW12) and mode setting flags, $\overline{RF}$ (Read Flag), $\overline{WF}$ (Write Flag) and $\overline{MF}$ (Mode Flag) are read into by $\overline{SAD}$ with synchronous $\overline{SAS}$. In order to output data continuously, the address specified by $\overline{SAD}$ increments automatically.



■ MODE PROGRAMMING

Operation mode in HM53051 is programmed by the combination of SAD 5-bit.

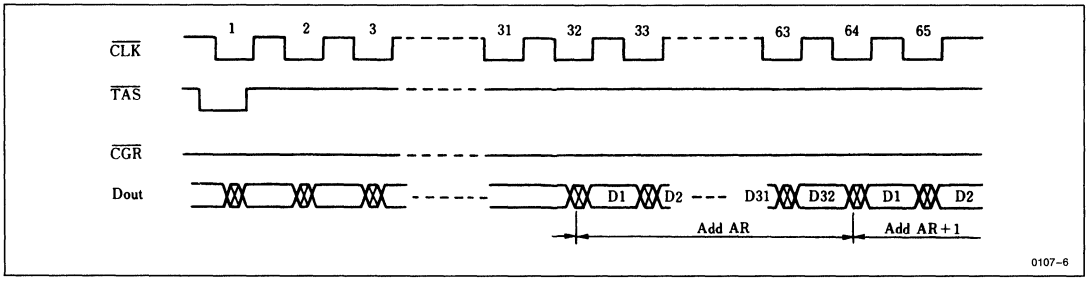
$\overline{MF}$	$\overline{WF}$	$\overline{RF}$	AW0	AR0	Mode
0	0	0	x	x	Write/Read Address Asynchronous Transfer
0	0	1	x	x	Write Address Asynchronous Transfer
0	1	0	x	x	Read Address Asynchronous Transfer
0	1	1	x	x	
1	0	0	x	x	Write/Read Address Synchronous Transfer
1	0	1	x	x	Write Address Synchronous Transfer
1	1	0	x	x	Read Address Synchronous Transfer
1	1	1	1	1	System Reset
1	1	1	0	0	Inhibit
1	1	1	0	1	
1	1	1	1	0	

Note: x means Don't Care.

■ READ/WRITE ADDRESS ASYNCHRONOUS TRANSFER MODE

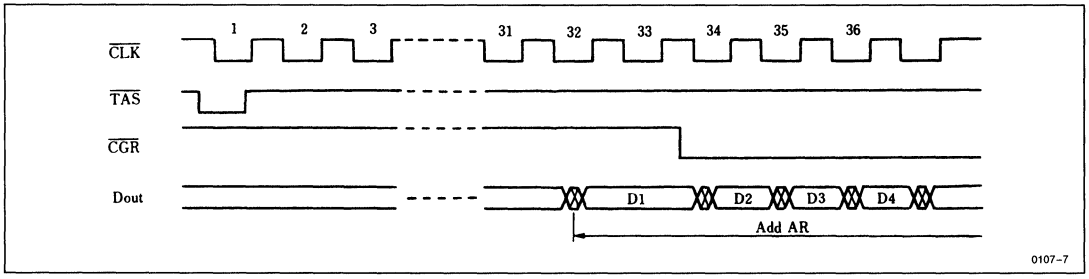
• Read Address Asynchronous Transfer Mode

(1) Read address asynchronous transfer mode (1) ($\overline{CGR}$: Low)



Note: The data block at read address AR, specified by SAD, is output starting from the 32nd system clock after the falling of $\overline{TAS}$.

(2) Read address asynchronous transfer mode (2) ($\overline{CGR}$: High)

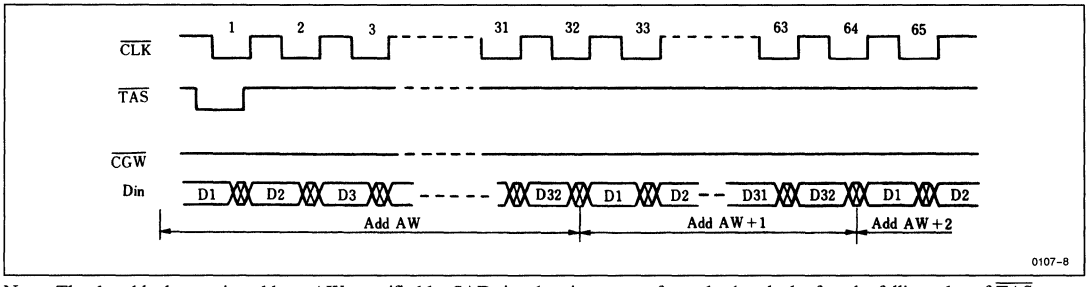


Notes: 1. The data block at read address AR, specified by SAD, is output starting from the 32nd system clock after the falling of $\overline{TAS}$.

2. If $\overline{CGR}$ is turned to low after 33rd clock from falling edge of $\overline{TAS}$, the data at read address AR(D2, D3, D4 . . .) is output with synchronous $\overline{CLK}$ while $\overline{CGR}$ is low.

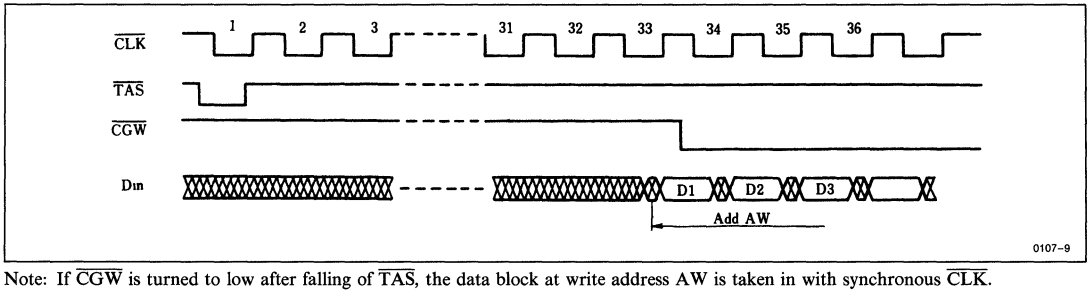
• Write Address Asynchronous Transfer Mode

(1) Write address asynchronous transfer mode (1) ($\overline{GRW}$: Low)



Note: The data block at write address AW, specified by SAD, is taken in starting from the 1st clock after the falling edge of $\overline{TAS}$.

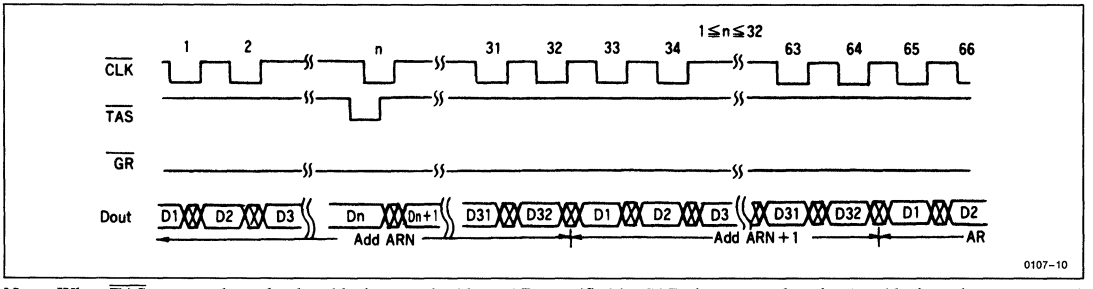
(2) Write address asynchronous transfer mode (2) ($\overline{CGW}$: High)



Note: If $\overline{CGW}$ is turned to low after falling of $\overline{TAS}$, the data block at write address AW is taken in with synchronous $\overline{CLK}$.

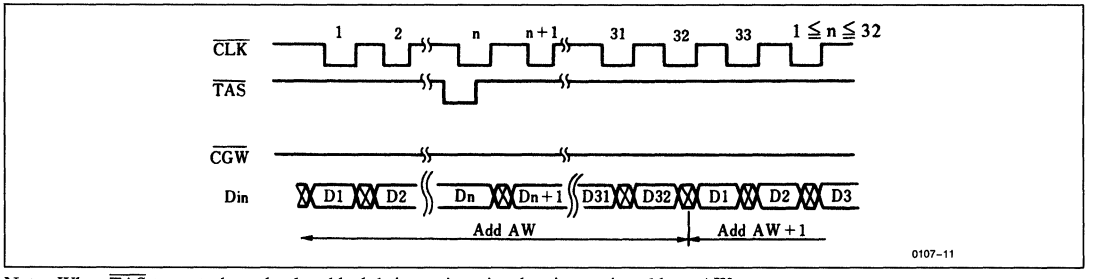
■ READ/WRITE ADDRESS SYNCHRONOUS TRANSFER MODE

• Read Address Synchronous Transfer Mode



Note: When $\overline{TAS}$ turns to low, the data block at read address AR, specified by SAD, is output after the data block at the present read address ARN, and the next address ARN + 1 is put out.

• Write Address Synchronous Transfer Mode



Note: When $\overline{TAS}$ turns to low, the data block being written is taken into write address AW.

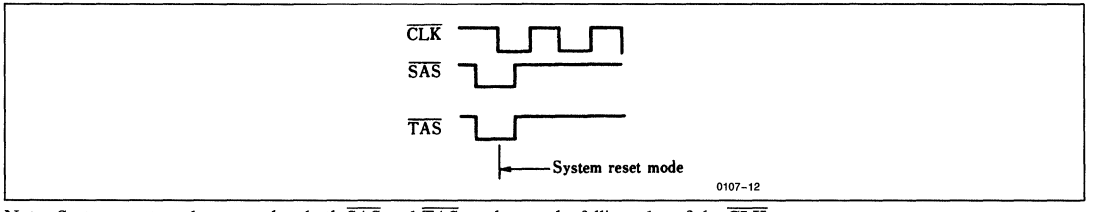
■ SYSTEM RESET MODE

System reset mode is the same as read/write address asynchronous transfer mode except that read/write address are reset to 0.

- System Reset by SAD

Note: System reset mode starts when $\overline{MF}$, $\overline{WF}$, $\overline{RF}$, AW0, and AR0 are all high.

- System Reset by $\overline{SAS}$ and $\overline{TAS}$



Note: System reset mode starts when both $\overline{SAS}$ and $\overline{TAS}$ are low at the falling edge of the $\overline{CLK}$.

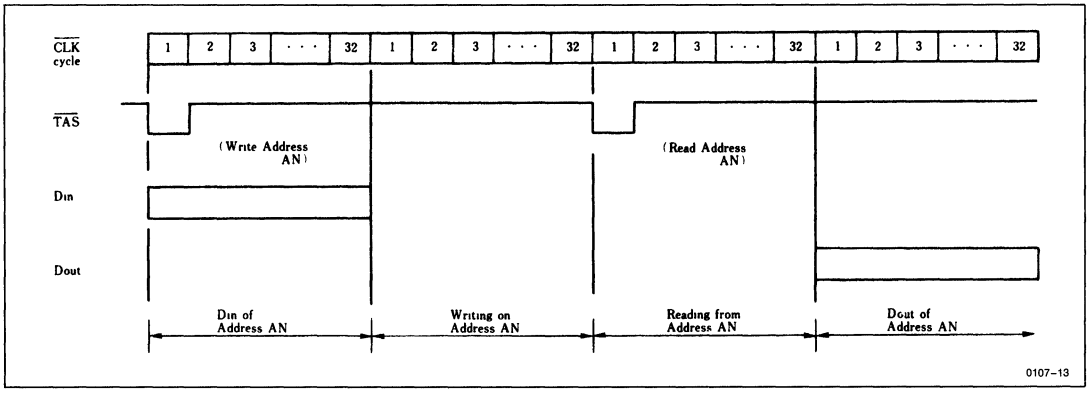
- 1 Field Delay

Note: Field-delayed data is output, when $\overline{CGR}$ and $\overline{CGW}$ turn to high before the system reset at the beginning of every field, and turn to low simultaneously after the 33rd clock from the system reset.

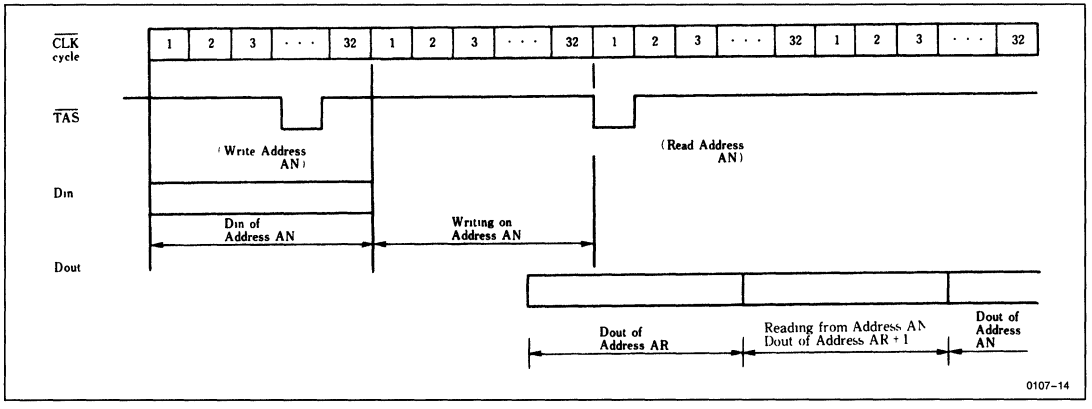
■ NOTES ON USING HM53051

- Input/Output data of 32 words is not written or read in read/write address asynchronous transfer mode or during system reset. The data is written or read out in blocks of 32-word x 4-bit. Input data of less than 32 words is not written in write address asynchronous transfer mode or during system reset. When asynchronous read address transfer mode or system reset mode is activated, output from the current data block will continue. When output data from the current data block is finished, the next data block is not read out if it has less than 32 words.
- Input data is not read out immediately. The data (32 word x 4-bit) is written into the memory array in the next 32 cycles after it is taken in.
  The data can be read out only after writing to the memory array is completed. If read address transfer mode is programmed after the 33 word clock from on input data block, new data can be read out. If this mode is programmed before the 33 word clock, new data or old data is output.

(1) Read/write address asynchronous transfer mode



(2) Read/write address synchronous transfer mode

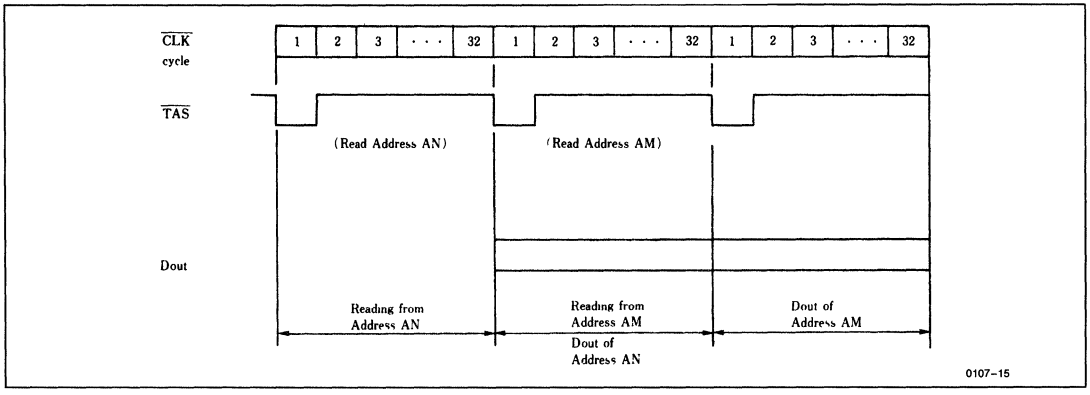


• Mode Programming

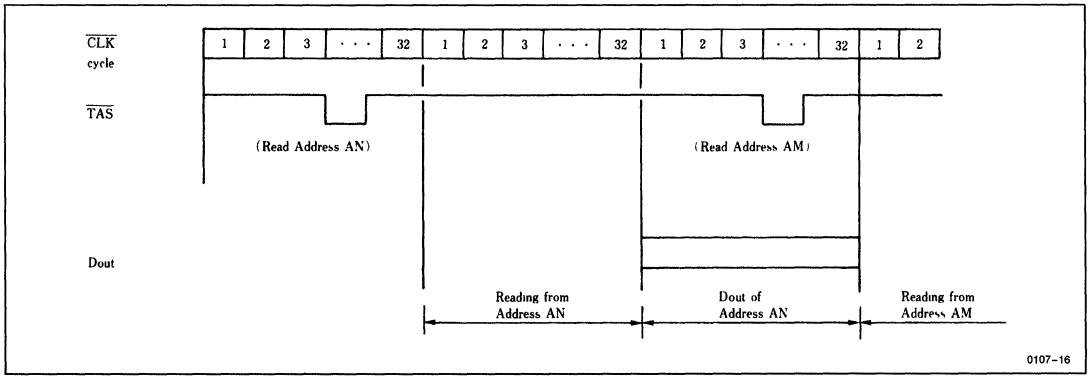
Do not reprogram read address transfer mode before a read operation of the previous read address transfer mode or system reset mode is completed. If it is reprogrammed during a read operation, address becomes invalid, and the device may malfunction.

Do not reprogram write address transfer mode or system reset mode before a write operation of the previous write address transfer mode or system reset mode is completed. If it is reprogrammed during a write operation, address becomes invalid, and the device may malfunction.

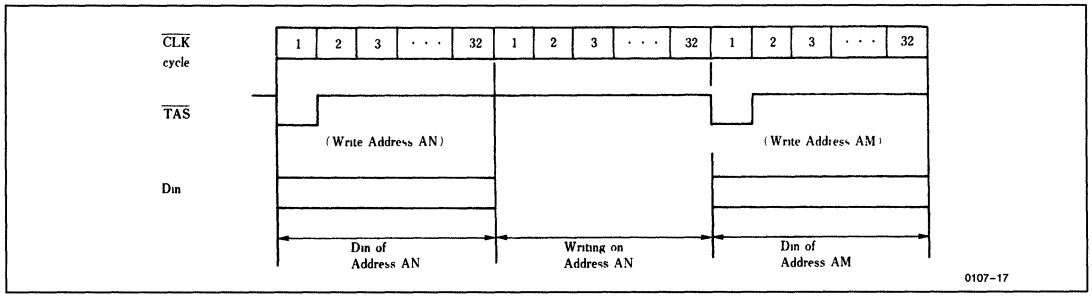
(1) Read address asynchronous transfer mode



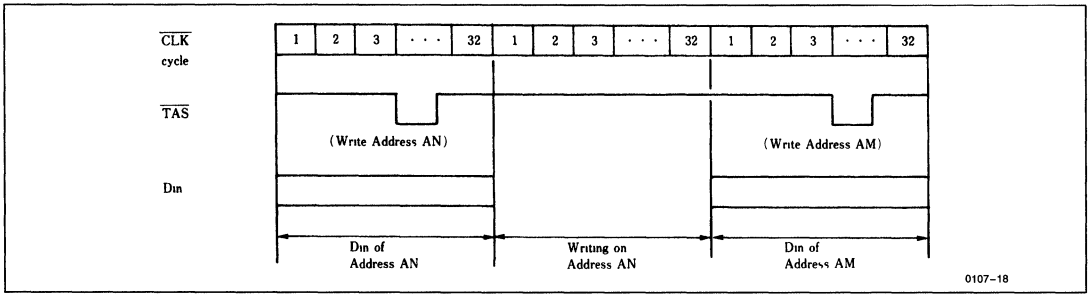
(2) Read address synchronous transfer mode



(3) Write address asynchronous transfer mode



(4) Write address synchronous transfer mode



- Addresses must be set by read and write address asynchronous transfer or system reset 100 μs after power on. Before an address can be set, 32 $\overline{CLK}$ initialization cycles or more are required.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 35 to + 125	°C
Storage Temperature (under Bias)	T_{bias}	− 10 to + 85	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input Voltage	V_{IH}	2.7	—	6.5	V	
	V_{IL}	− 0.5	—	0.8	V	1

Note: 1. − 3.0V for pulse width ≤ 10 ns.

• DC and Operating Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
Operating Power Supply Current	I_{CC}	—	40	60	mA	Min. Cycle, I_{out} = 0 mA	
Input Leakage Current	I_{LI}	− 10	—	10	μA	V_{CC} = 5.5V, V_{in} = V_{SS} to V_{CC}	
Output Leakage Current	I_{LO}	− 10	—	10	μA	$\overline{OE}$ = V_{IH}, V_{out} = V_{SS} to V_{CC}	
Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 4.2 mA	
	V_{OH}	2.4	—	—	V	I_{OH} = − 2 mA	

• Capacitance (T_A = 25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions	Note
Input Capacitance	C_{in}	—	—	5	pF	V_{in} = 0V	
Output Capacitance	C_{out}	—	—	7	pF	V_{out} = 0V	

Note: This parameter is sampled and not 100% tested.

• AC Characteristics (V_{CC} = 5V ±10%, T_A = 0 to +70°C)

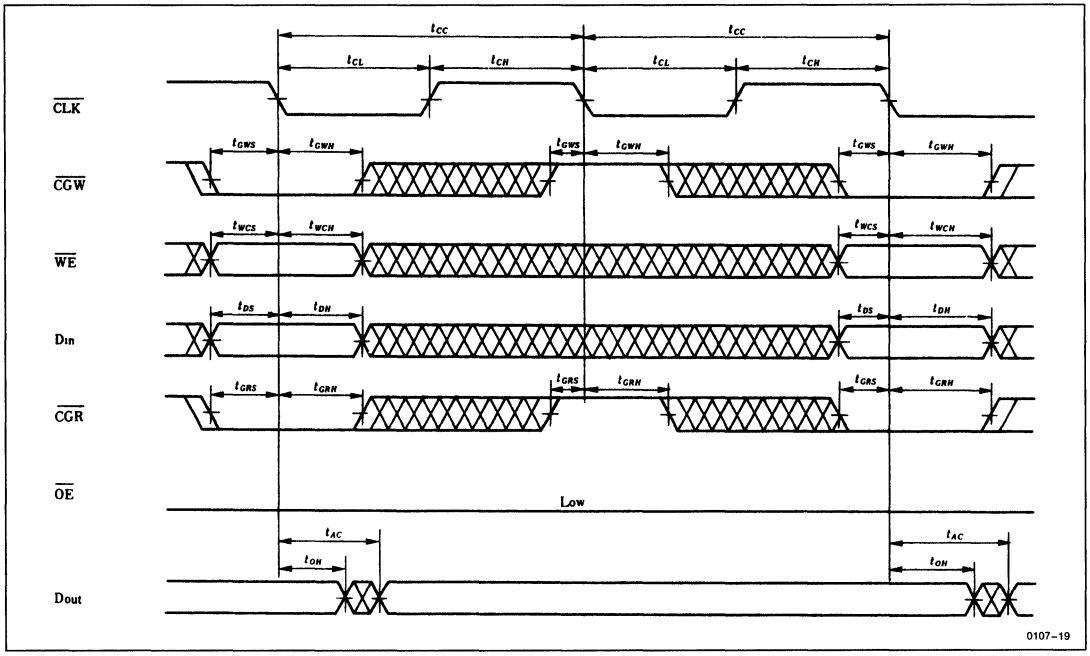
AC Test Conditions

Input and Output Timing Reference Levels: 1.5V
Input Pulse Levels: V_{SS} to 3V
Input Rise and Fall Times: 5 ns
Output Load: 2 TTL + 50 pF
(Including scope and jig)

Parameter	Symbol	HM53051-45		HM53051-60		Unit
		Min	Max	Min	Max	
System Clock Cycle Time	t_{CC}	45	300	60	300	ns
$\overline{CLK}$ Pulse Width	t_{CL}	15	—	15	—	ns
	t_{CH}	15	—	15	—	ns
Access Time from $\overline{CLK}$	t_{AC}	—	35	—	40	ns
Output Hold Time	t_{OH}	5	—	8	—	ns
Output Enable Access Time	t_{OEA}	—	25	—	30	ns
Output Enable to Output in Low Z	t_{OLZ}	5	—	5	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	20	0	20	ns
$\overline{CGR}$ Setup Time	t_{GRS}	15	—	15	—	ns
$\overline{CGR}$ Hold Time	t_{GRH}	5	—	5	—	ns
$\overline{CGW}$ Setup Time	t_{GWS}	15	—	15	—	ns
$\overline{CGW}$ Hold Time	t_{GWH}	5	—	5	—	ns
Write Command Setup Time	t_{WCS}	15	—	15	—	ns
Write Command Hold Time	t_{WCH}	5	—	5	—	ns
Data Input Setup Time	t_{DS}	15	—	15	—	ns
Data Input Hold Time	t_{DH}	5	—	5	—	ns
$\overline{SAS}$ Cycle Time	t_{SC}	45	—	60	—	ns
$\overline{SAS}$ Pulse Width	t_{SL}	15	—	15	—	ns
	t_{SH}	15	—	15	—	ns
Serial Address Setup Time	t_{SAS}	15	—	15	—	ns
Serial Address Hold Time	t_{SAH}	5	—	5	—	ns
$\overline{SAS}$ Setup Time during Mode Programming	t_{SSH}	15	—	15	—	ns
$\overline{SAS}$ Hold Time during Mode Programming	t_{SHH}	5	—	5	—	ns
$\overline{TAS}$ Setup Time	t_{TS}	15	—	15	—	ns
$\overline{TAS}$ Hold Time	t_{TH}	5	—	5	—	ns
$\overline{SAS}$ Setup Time during System Reset by $\overline{SAS}/\overline{TAS}$	t_{SSL}	15	—	15	—	ns
$\overline{SAS}$ Hold Time during System Reset by $\overline{SAS}/\overline{TAS}$	t_{SHL}	5	—	5	—	ns

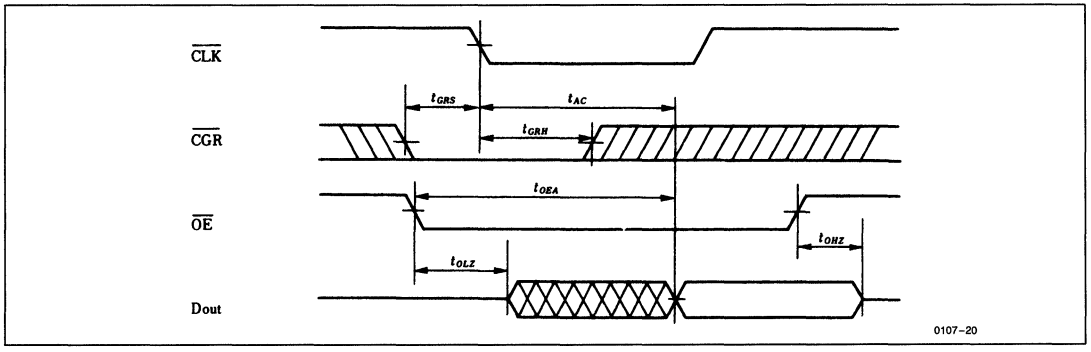
■ TIMING WAVEFORMS

• Read/Write Cycle



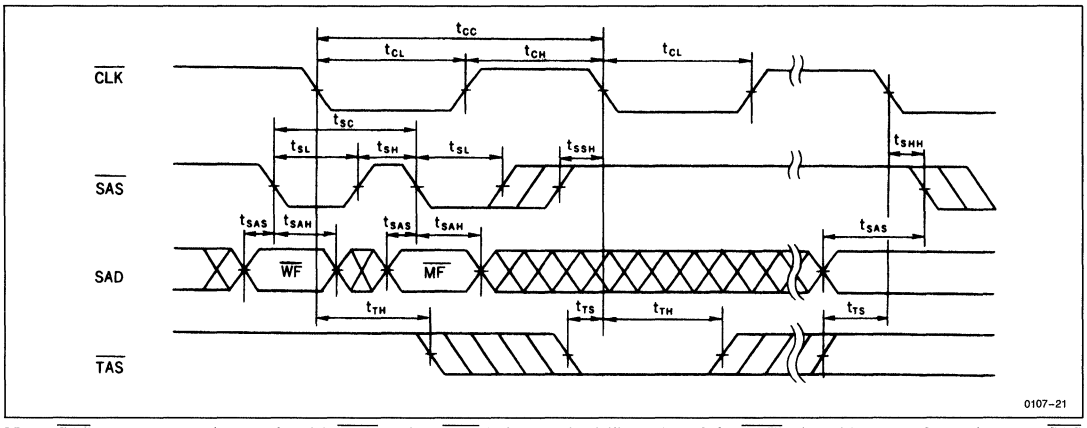
Notes: 1. Write cycle starts when $\overline{CGW}$ is low and $\overline{WE}$ is low. Data are not written when $\overline{WE}$ is high. Time-compression mode is realized by controlling $\overline{CGW}$.
2. Read cycle starts when $\overline{CGR}$ is low. Time-expansion mode is realized by controlling $\overline{CGR}$.

• Read Cycle ($\overline{OE}$ Control)



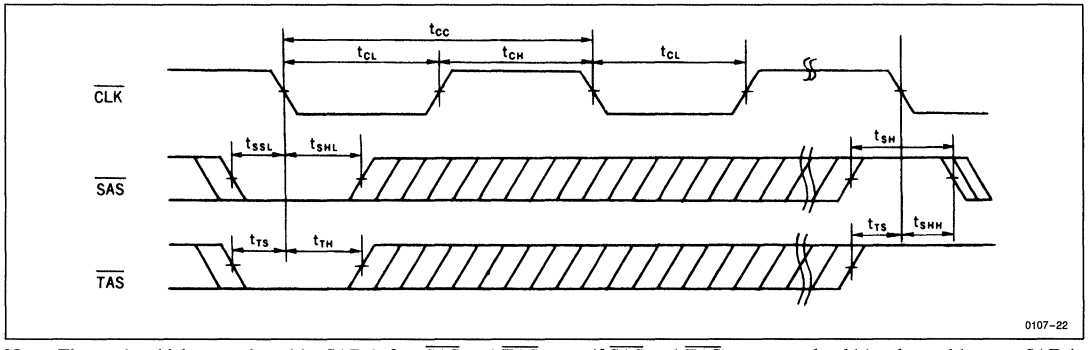
Notes: 1. t_{OHZ} is defined by the time at which the output achieves the open circuit condition.
2. t_{OLZ} and t_{OHZ} are sampled and not 100% tested.

• Mode Selection



Note: $\overline{SAS}$ operates asynchronously with $\overline{CLK}$. When $\overline{TAS}$ is low at the falling edge of the $\overline{CLK}$, the addres transfer cycle starts. $\overline{SAS}$ should be high during the address transfer cycle.

• $\overline{SAS}$, $\overline{TAS}$ Reset Mode



Note: The mode which was selected by SAD before $\overline{SAS}$ and $\overline{TAS}$ reset, if $\overline{SAS}$ and $\overline{TAS}$ are reset, should be changed because SAD is newly taken into by SAS. The mode should be reselected by SAD after $\overline{SAS}$ and $\overline{TAS}$ reset.

HM53461 Series

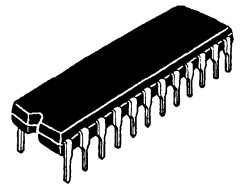
65,536-word x 4-bit Multiport CMOS Video RAM

■ DESCRIPTION

The HM53461 is a 262,144-bit multiport memory equipped with a 64k-word x 4-bit Dynamic RAM port and a 256-word x 4-bit Serial Access Memory (SAM) port. The SAM port is connected to an internal 1,024-bit data register through a 256-word x 4-bit serial read or write access control. In the read transfer cycle, the memory cell data is transferred from a selected word line of the RAM port to the data register. The RAM port has a write mask capability in addition to the conventional operation mode. Write bit selection out of 4 data bit can be achieved.

Utilizing the Hitachi 2 μm CMOS process, fast serial access operation and low power dissipation are realized. All inputs and outputs, including clocks, are TTL compatible.

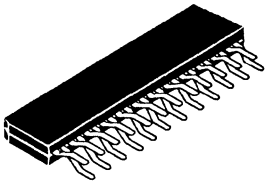
HM53461P Series



3DDP24A

(DP-24A)

HM53461ZP Series



3DZP24

(ZP-24)

■ FEATURES

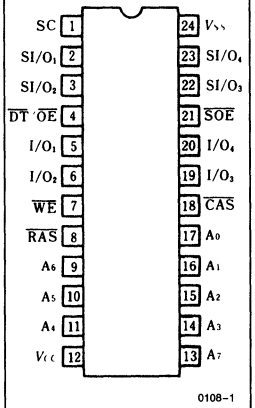
- Multiport Organization
  (RAM; 64k-word x 4-bit and SAM; 256 word x 4-bit)
- Double Layer Polysilicon/Polyicide n-Well CMOS Process
- Single 5V (±10%)
- Low Power
  - Active
    - RAM ..... 380 mW (max)
    - SAM ..... 220 mW (max)
  - Standby ..... 40 mW (max)
- Access Time
  - RAM ..... 100 ns/120 ns/150 ns
  - SAM ..... 40 ns/40 ns/60 ns
- Cycle Time Random Read or Write Cycle Time (RAM) ..... 190 ns/220 ns/260 ns
  Serial Read or Write Cycle Time (SAM) ..... 40 ns/40 ns/60 ns
- TTL Compatible
- 256 Refresh Cycles ..... 4 ms
- Refresh Function
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Data Transfer Operation (RAM ⟷ SAM)
- Fast Serial Access Operation Asynchronized with RAM Port Except Data Transfer Cycle
- Real Time Read Transfer Capability
- Write Mask Mode Capability

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM53461P-10	100 ns	400 mil 24-pin
HM53461P-12	120 ns	Plastic DIP
HM53461P-15	150 ns	(DP-24A)
HM53461ZP-10	100 ns	24-pin
HM53461ZP-12	120 ns	Plastic ZIP
HM53461ZP-15	150 ns	(ZP-24)

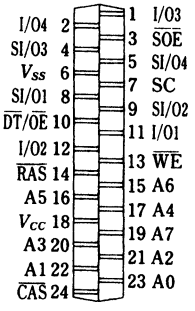
■ PIN OUT

HM53461P Series



(Top View)

HM53461ZP Series

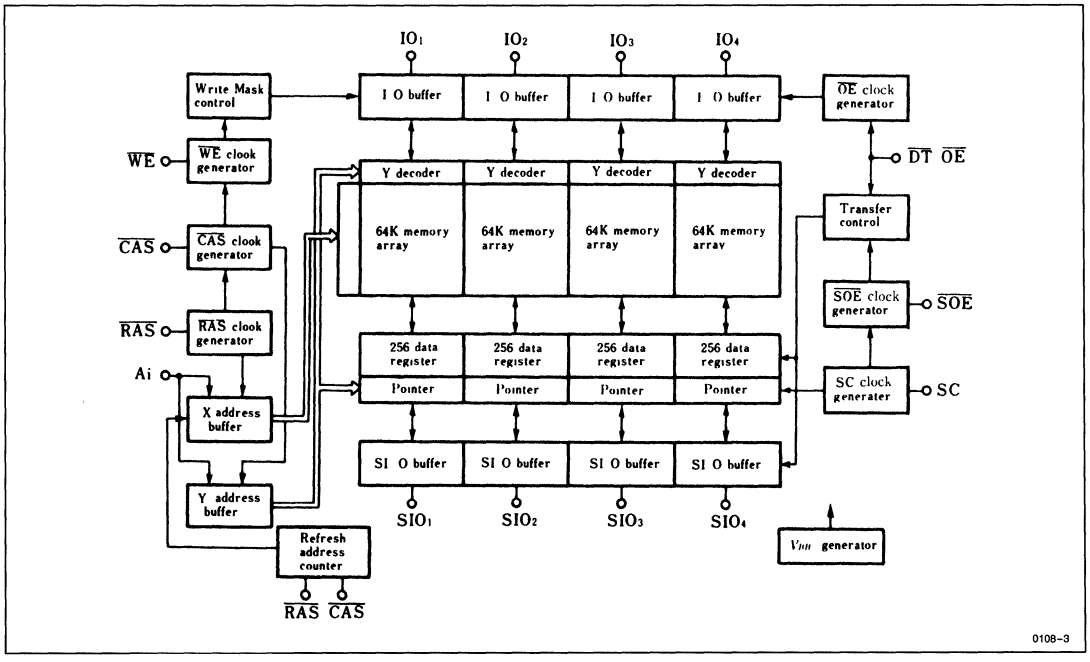


(Bottom View)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_7	Address Inputs
I/O_1–I/O_4	RAM Port Data Input/Output
SI/O_1–SI/O_4	SAM Port Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
SC	Serial Clock
$\overline{WE}$	Write Enable
$\overline{DT/OE}$	Data Transfer/Output Enable
$\overline{SOE}$	SAM Port Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Power Supply Voltage Relative to V_{SS}	V_{CC}	−0.5 to +7.0	V
Operating Temperature, T_A (Ambient)	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.4	—	6.5	V	
Input Low Voltage	V_{IL}	−0.5	—	0.8	V	2

Notes: 1. All voltages referenced to V_{SS}.
2. −3.0V for pulse width ≤ 10 ns.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	SAM PORT		HM53461-10	HM53461-12	HM53461-15	Unit	RAM PORT	Note
		Standby	Active					Test Conditions	
Operating Current	I_{CC1}	—	×	70	60	50	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	
	I_{CC7}	×	—	110	100	80	mA		
Standby Current	I_{CC2}	—	×	7	7	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	
	I_{CC8}	×	—	40	40	30	mA		
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	×	60	50	40	mA	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling t_{RC} = Min	
	I_{CC9}	×	—	100	90	70	mA		
Page Mode Current	I_{CC4}	—	×	50	40	35	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling t_{PC} = Min	
	I_{CC10}	×	—	90	80	65	mA		
CBR Refresh Current	I_{CC5}	—	×	60	50	40	mA	$\overline{RAS}$ Cycling t_{RC} = Min	
	I_{CC11}	×	—	100	90	70	mA		
Data Transfer Current	I_{CC6}	—	×	75	65	55	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	
	I_{CC12}	×	—	115	105	85	mA		

Parameter	Symbol	Min	Max	Unit	Test Conditions	Note
Input Leakage	I_{LI}	−10	10	μA		
Output Leakage	I_{LO}	−10	10	μA		
Output High Voltage	V_{OH}	2.4	—	V	I_{OH} = −2 mA	
Output Low Voltage	V_{OL}	—	0.4	V	I_{OL} = 4.2 mA	

■ INPUT/OUTPUT CAPACITANCE

Parameter	Symbol	Typ	Max	Unit	Note
Address	C_{I1}	—	5	pF	
Clocks	C_{I2}	—	5	pF	
I/O, SI/O	$C_{I/O}$	—	7	pF	

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 10, 11]

Parameter	Symbol	HM53461-10		HM53461-12		HM53461-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	190	—	220	—	260	—	ns	
Read-Modify-Write Cycle Time	t_{RWC}	260	—	300	—	355	—	ns	
Page Mode Cycle Time	t_{PC}	70	—	85	—	105	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	50	—	60	—	75	ns	3, 4
Output Buffer Turn-off Delay Referenced to $\overline{CAS}$	t_{OFF1}	0	25	0	30	0	40	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
$\overline{RAS}$ Precharge Time	t_{RP}	80	—	90	—	100	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	50	25	60	30	75	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	50	—	60	—	75	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	25	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	35	—	40	—	45	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	35	—	40	—	45	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	25	—	25	—	30	—	ns	8, 9
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	
$\overline{RAS}$ Pulse Width (Read-Modify-Write Cycle)	t_{RWS}	170	10000	200	10000	245	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	85	—	100	—	125	—	ns	8
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CHR}	20	—	25	—	30	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	15	—	20	—	ns	
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	35	—	40	ns	
Output Buffer Turn-off Delay referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	25	—	30	—	40	—	ns	
$\overline{OE}$ Hold Time referenced to $\overline{WE}$	t_{OEH}	10	—	15	—	20	—	ns	
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	0	—	ns	
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{OE}$ to $\overline{RAS}$ Delay Time	t_{ORD}	35	—	40	—	45	—	ns	
Serial Clock Cycle Time	t_{SCC}	40	—	40	—	60	—	ns	
Access Time from SC	t_{SCA}	—	40	—	40	—	60	ns	10
Access Time from $\overline{SOE}$	t_{SEA}	—	25	—	30	—	40	ns	10

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

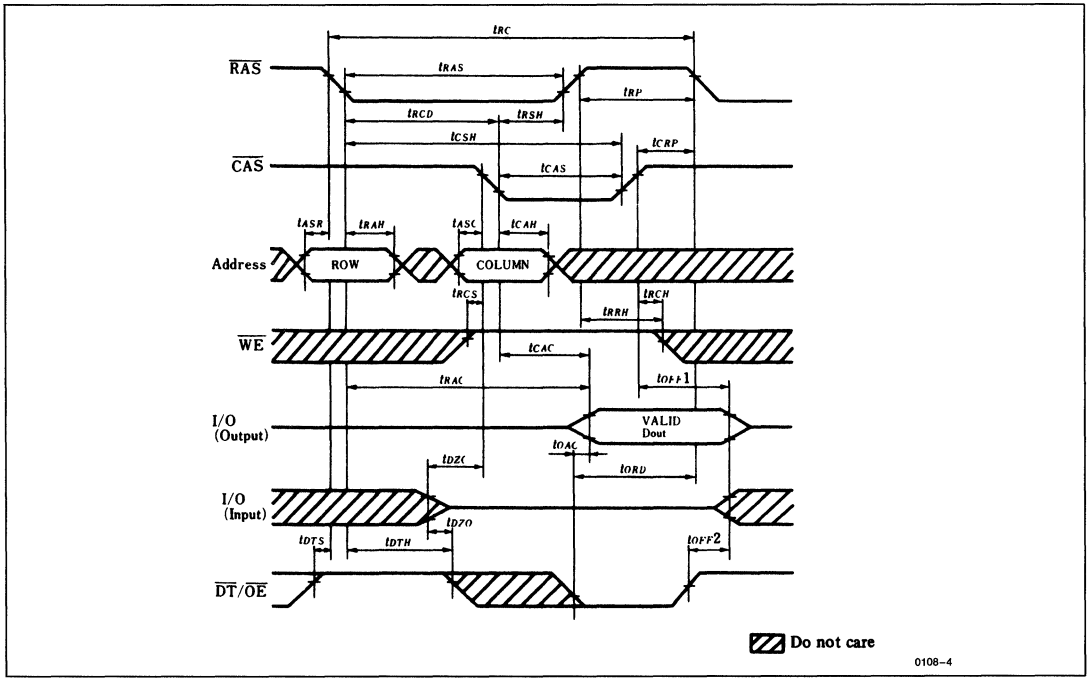
(T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 10, 11] (continued)

Parameter	Symbol	HM53461-10		HM53461-12		HM53461-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
SC Pulse Width	t_{SC}	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	ns	
Serial Data-out Hold Time after SC High	t_{SOH}	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{SOE}$	t_{SEZ}	0	25	0	25	0	30	ns	
Serial Data-in Setup TIme	t_{SIS}	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	25	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time (Read Transfer Cycle)	t_{RDH}	80	—	90	—	110	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	—	15	—	20	—	ns	
$\overline{DT}$ to $\overline{CAS}$ Hold Time	t_{CDH}	20	—	30	—	45	—	ns	
Last SC to $\overline{DT}$ Delay Time	t_{SDD}	5	—	5	—	10	—	ns	
First SC to $\overline{DT}$ Hold Time	t_{SDH}	25	—	25	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Delay Time	t_{DTR}	10	—	10	—	10	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	20	—	ms	
I/O to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	ns	
I/O to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	20	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	75	ns	
$\overline{SC}$ to $\overline{RAS}$ Setup Time	t_{SRS}	30	—	40	—	45	—	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	—	30	—	35	—	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	—	60	—	75	—	ns	
Serial Data Input to $\overline{DT}$ Delay Time	t_{SZD}	0	—	0	—	0	—	ns	
$\overline{SOE}$ to $\overline{RAS}$ Setup Time	t_{ES}	0	—	0	—	0	—	ns	
$\overline{SOE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	—	15	—	20	—	ns	
Serial Write Enable Setup Time	t_{SWS}	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	t_{SWH}	35	—	35	—	55	—	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	35	—	35	—	55	—	ns	
$\overline{DT}$ to Sout in Low-Z Delay Time	t_{DLZ}	5	—	10	—	10	—	ns	

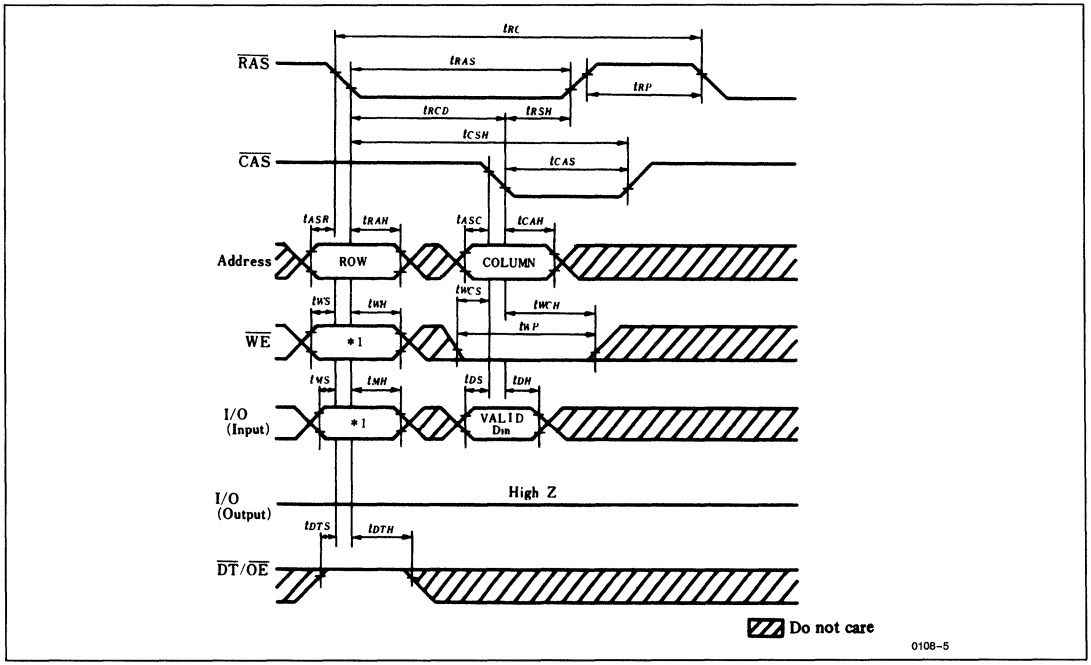
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
10. Measured with a load circuit equivalent to 2 TTL and 50 pF.
11. An initial pause of 100 μs is required after power-up. Then execute at least 8 initialization cycles.

■ TIMING WAVEFORMS

• Read Cycle

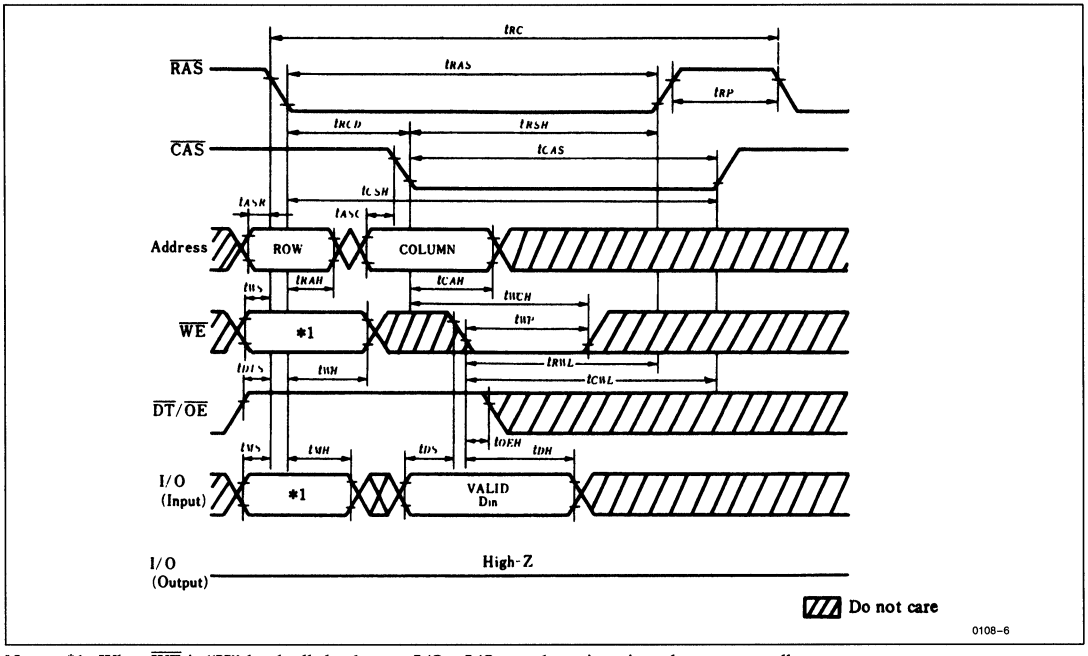


• Early Write Cycle



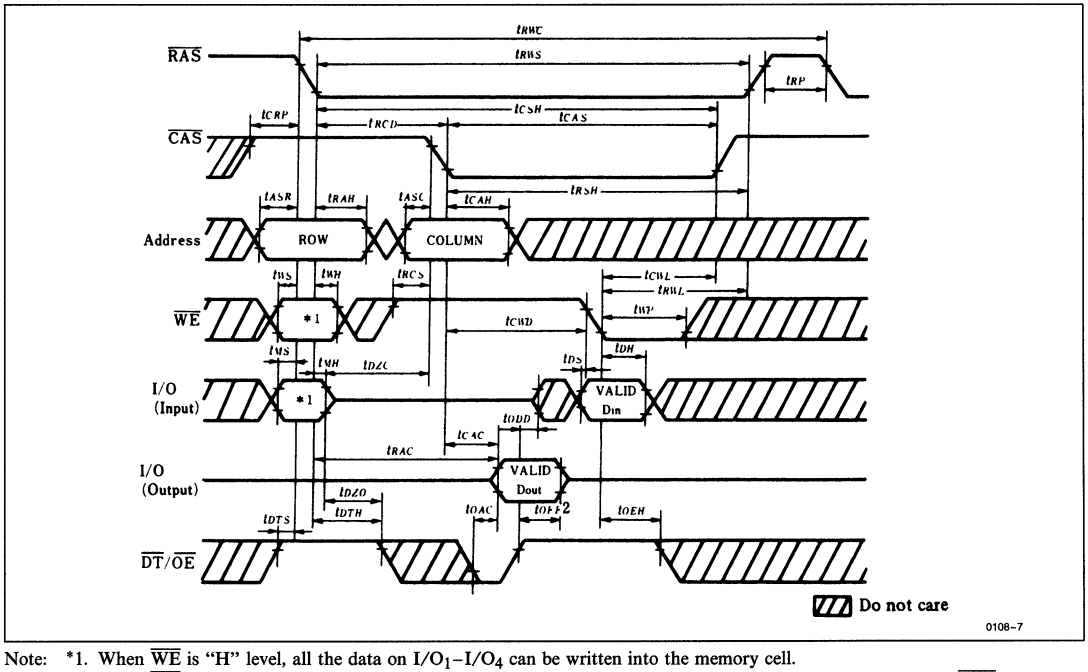
Note: *1. When $\overline{WE}$ is "H" level, all the data on the I/O can be written into the cell.
When $\overline{WE}$ is "L" level, the data on the I/O are not written except for when I/O is "high" at the falling edge of $\overline{RAS}$.

• **Delayed Write Cycle**



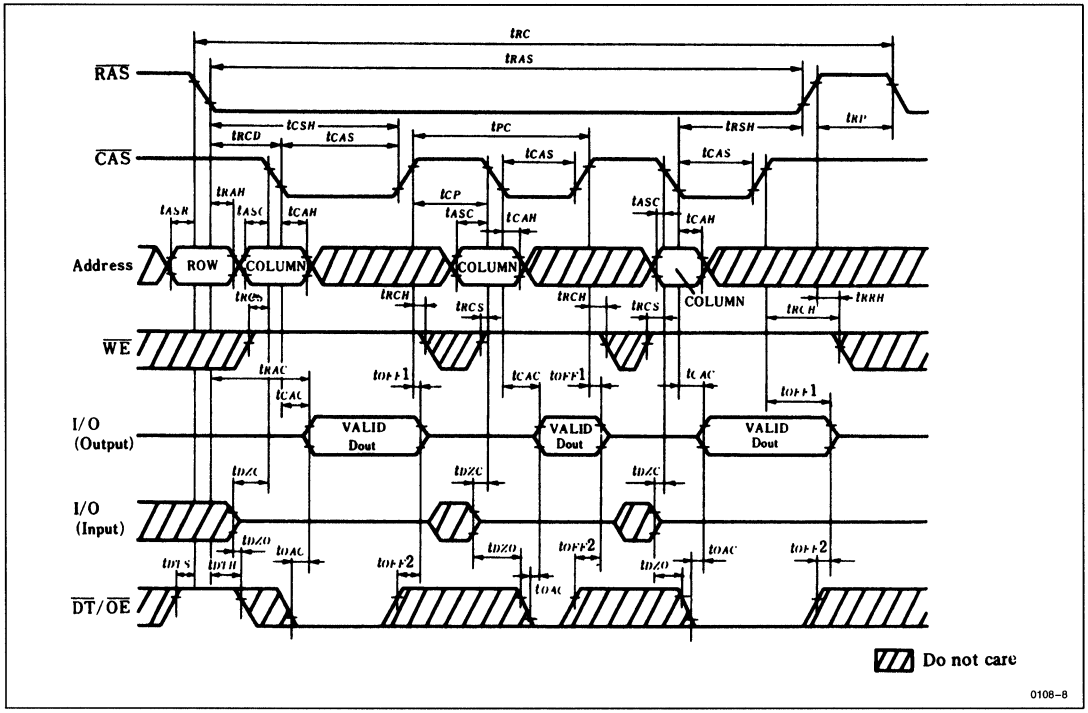
Note: *1. When $\overline{WE}$ is "H" level, all the data on I/O_1–I/O_4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

• **Read-Modify-Write Cycle**

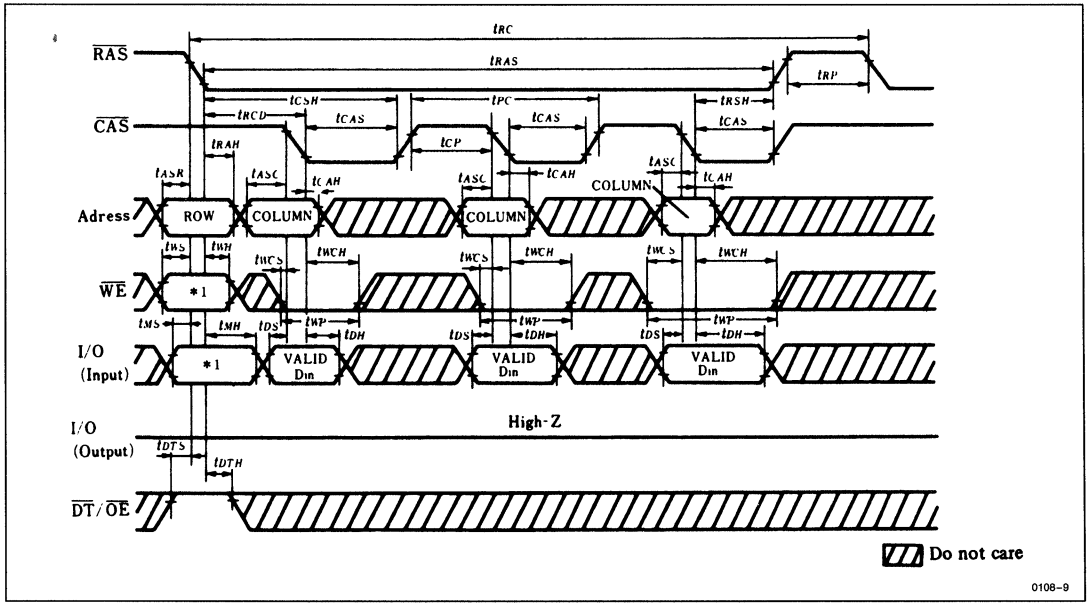


Note: *1. When $\overline{WE}$ is "H" level, all the data on I/O_1–I/O_4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

• **Page Mode Read Cycle**

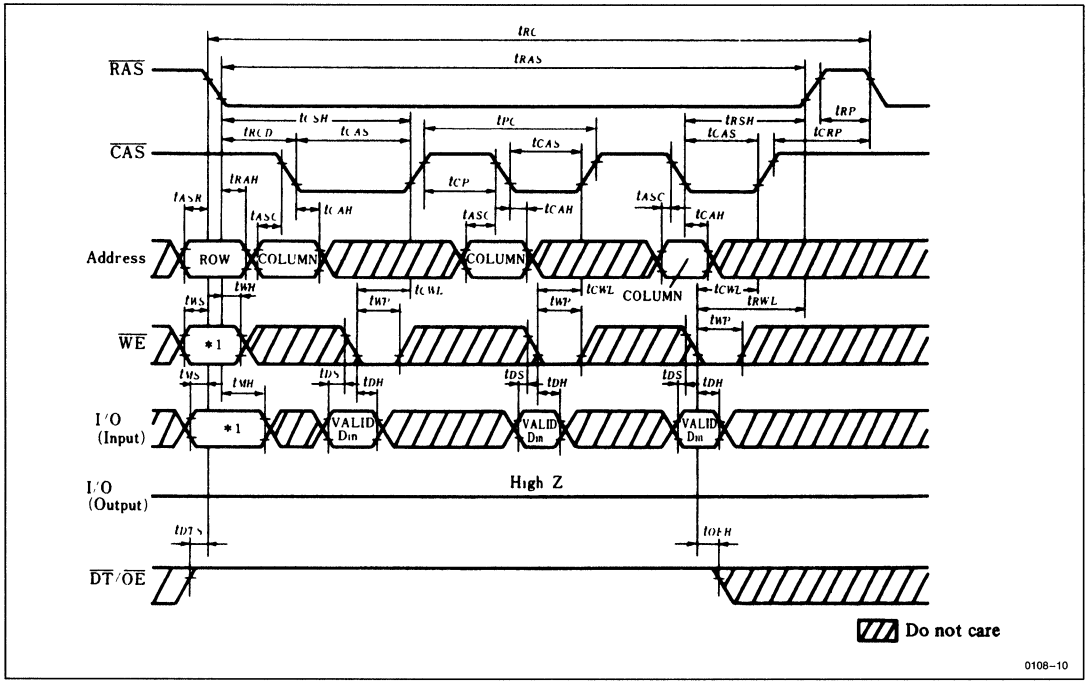


• **Page Mode Write Cycle (Early Write)**



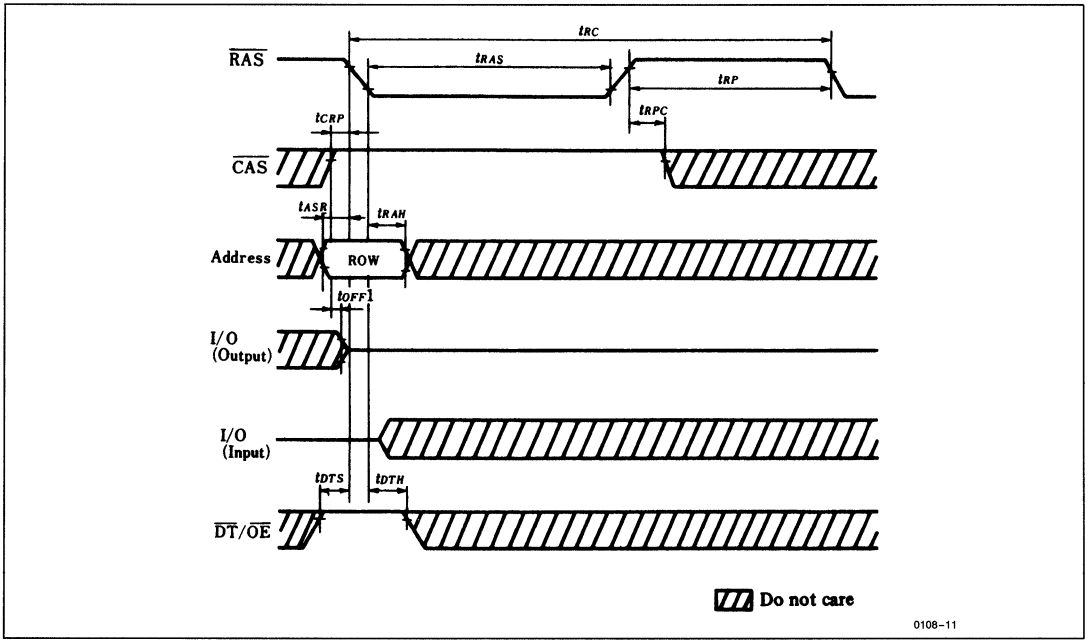
Note: *1. When $\overline{WE}$ is "H" level, all the data on I/O_1–I/O_4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

• **Page Mode Write Cycle (Delayed Write)**

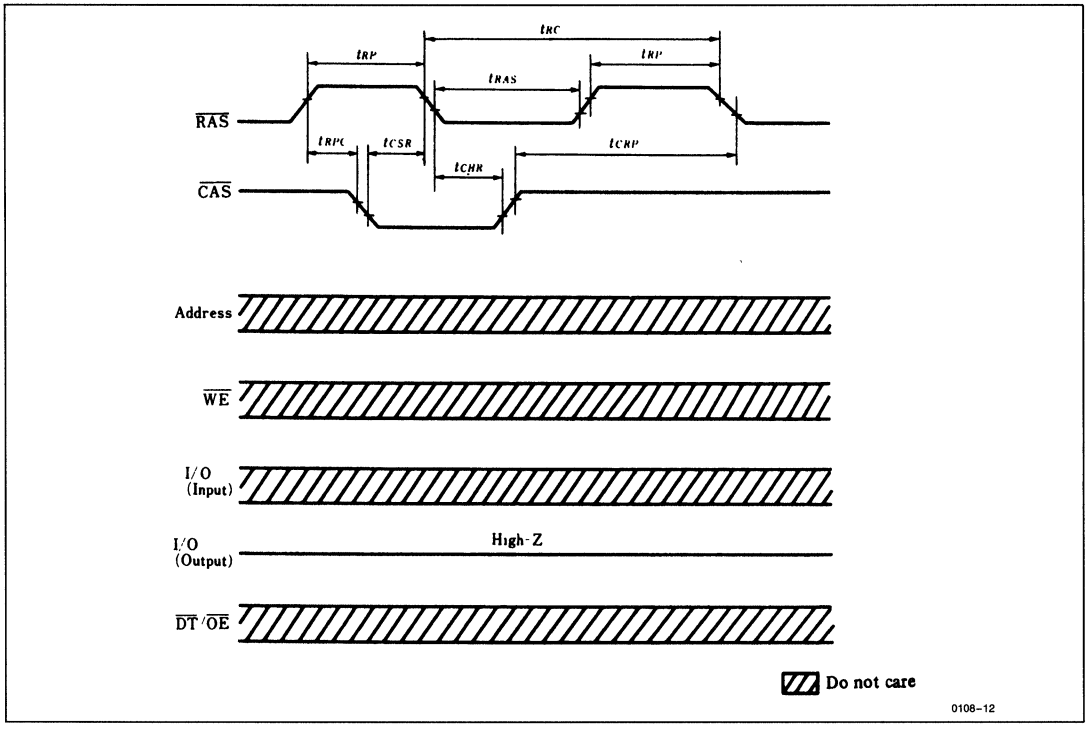


Note: *1. When $\overline{WE}$ is "H" level, all the data on I/O_1–I/O_4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

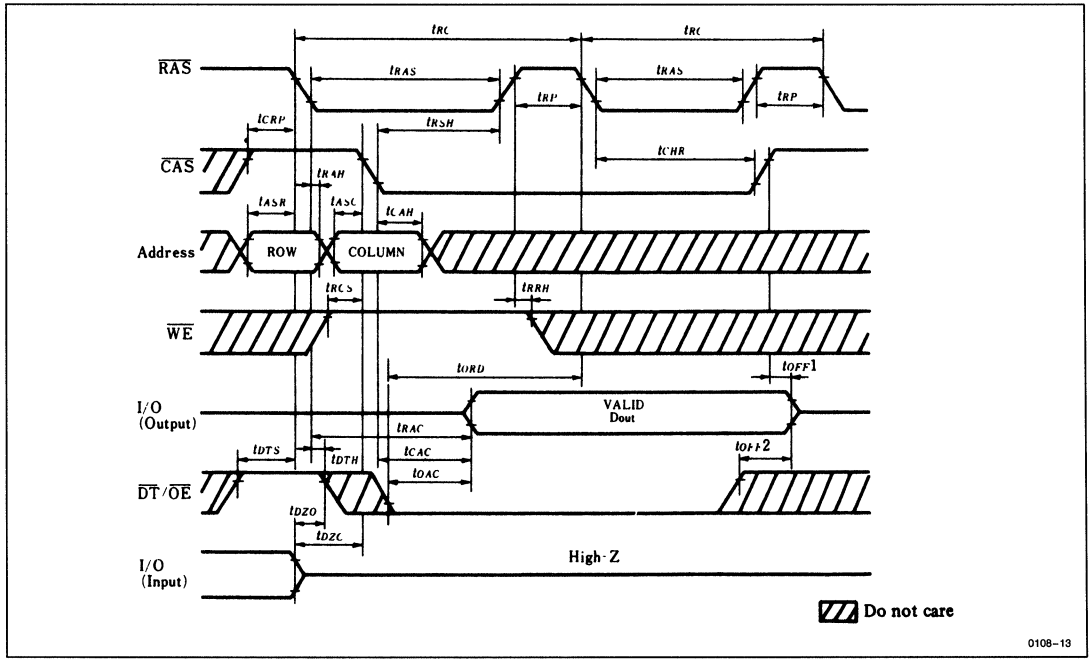
• **$\overline{RAS}$ Only Refresh Cycle**



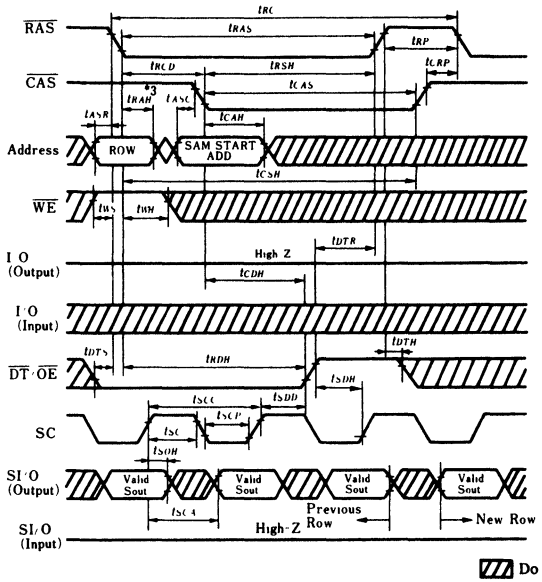
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• Hidden Refresh Cycle

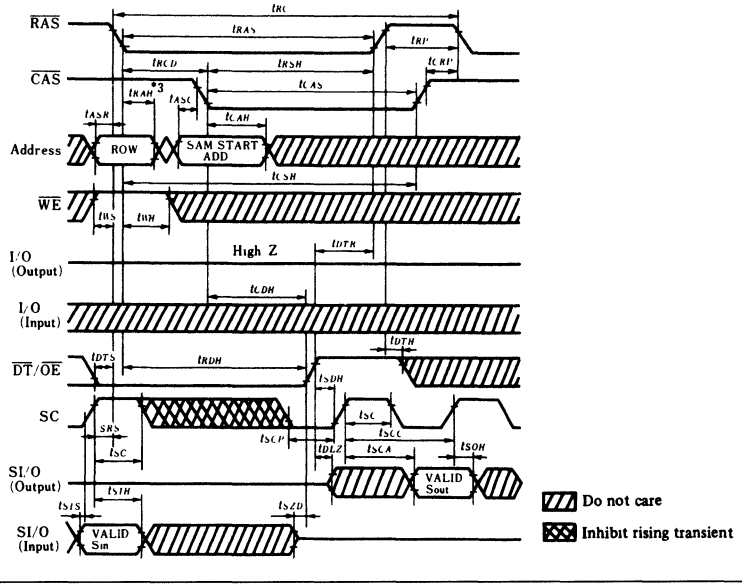


• Read Transfer Cycle (1)*1, *2



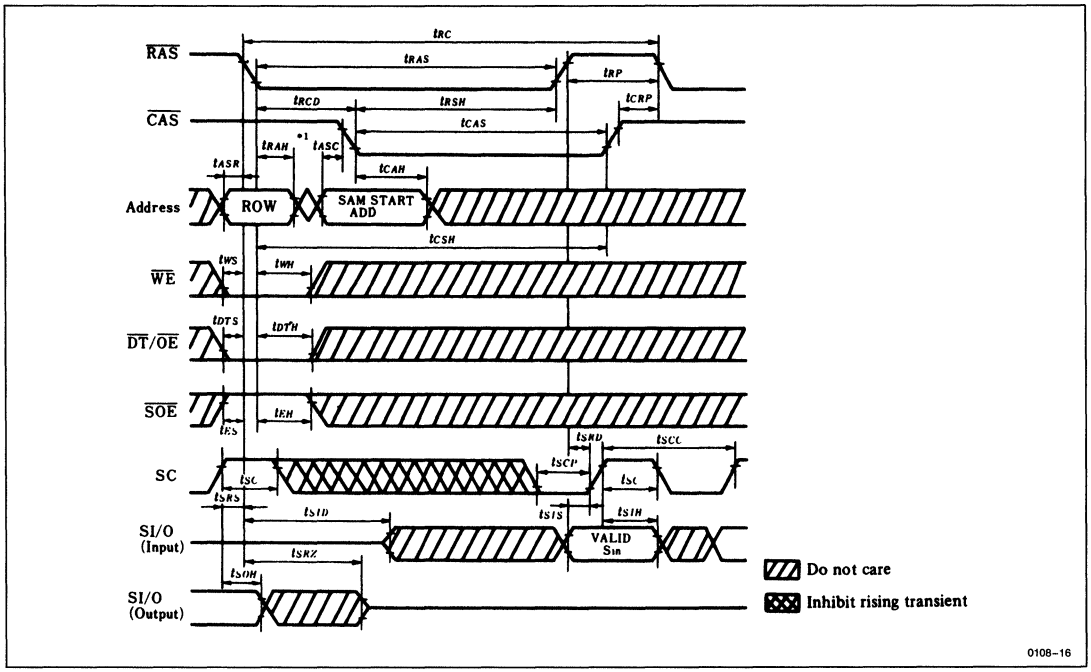
Notes: *1. In the case that the previous data transfer cycle was read transfer.
*2. Assume that $\overline{SOE}$ is "L" level.
*3. $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• Read Transfer Cycle (2)*1, *2



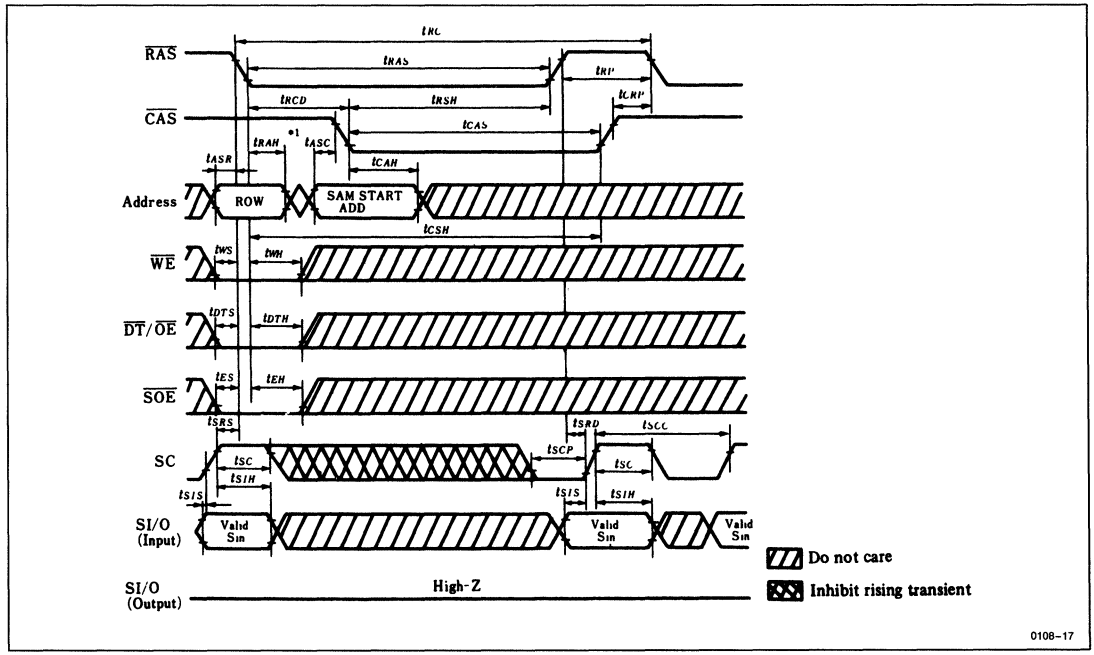
Notes: *1. In the case that the previous data transfer cycle was write transfer or pseudo transfer.
*2. Assume that $\overline{SOE}$ is "L" level.
*3. $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• **Pseudo Transfer Cycle**



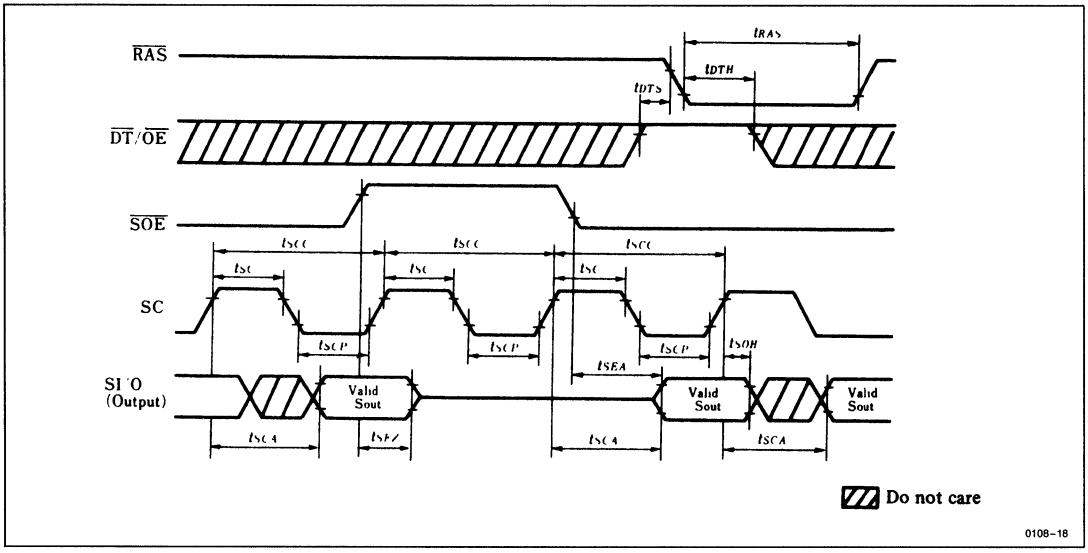
Note: *1. $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• **Write Transfer Cycle**

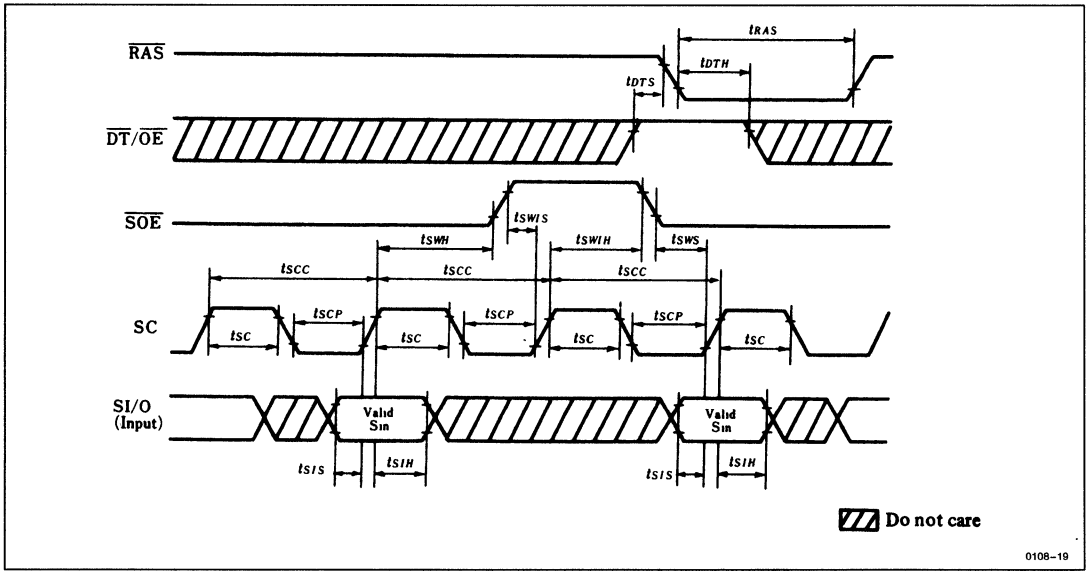


Note: *1. $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• **Serial Read Cycle**



• **Serial Write Cycle**



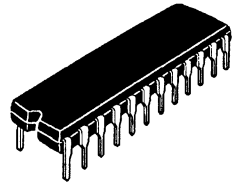
HM53462 Series

65,536-Word x 4-Bit Multiport CMOS Video RAM (with Logic Operation Mode)

■ DESCRIPTION

The HM53462 is a 262,144-bit multiport memory equipped with a 64k-word x 4-bit Dynamic RAM port and a 256-word x 4-bit Serial Access Memory (SAM) port. The SAM port is connected to an internal 1,024-bit data register through a 256-word x 4-bit serial read or write access control. In the read transfer cycle, the memory cell data is transferred from a selected word line of the RAM port to the data register. The RAM port has a write mask capability in addition to the conventional operation mode. Write bit selection out of 4 data bit can be achieved. RAM port has another new function, logic operation capability. By this function logic operation between memory data and input data can be done in one cycle. Utilizing the Hitachi 2 μm CMOS process, fast serial access operation and low power dissipation are realized. All inputs and outputs, including clocks, are TTL compatible.

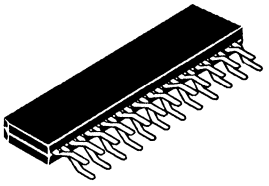
HM53462P Series



3DDP24A

(DP-24A)

HM53462ZP Series



3DZP24

(ZP-24)

■ FEATURES

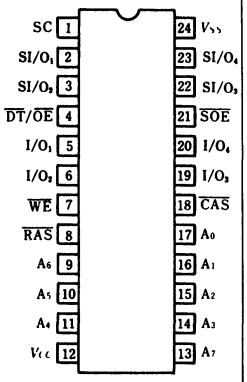
- Multiport Organization
  (RAM; 64k-word x 4-bit and SAM; 256-word x 4-bit)
- Double Layer Polysilicon/Polyicide N-Well CMOS Process
- Single 5V (±10%)
- Low Power
  - Active RAM ..... 380 mW (max)
  - SAM ..... 220 mW (max)
  - Standby ..... 40 mW (max)
- Access Time
  - RAM ..... 100 ns/120 ns/150 ns
  - SAM ..... 40 ns/40 ns/60 ns
- Cycle Time
  - Random Read or Write Cycle Time (RAM) ..... 190 ns/220 ns/260 ns
  - Serial Read or Write Cycle Time (SAM) ..... 40 ns/40 ns/60 ns
- TTL Compatible
- 256 Refresh Cycles ..... 4 ms
- Refresh Function
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Bidirectional Data Transfer Operation (RAM ⟷ SAM)
- Fast Serial Access Operation Asynchronized with RAM Port except Data Transfer Cycle
- Real Time Read Transfer Capability
- Write Mask Mode Capability
- Logic Operation Capability between D_{in} and D_{out}
- SAM Organization Can Be Changed to 1024 x 1

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM53462P-10	100 ns	400 mil 24-pin
HM53462P-12	120 ns	Plastic DIP
HM53462P-15	150 ns	(DP-24A)
HM53462ZP-10	100 ns	24-pin
HM53462ZP-12	120 ns	Plastic DIP
HM53462ZP-15	150 ns	(ZP-24)

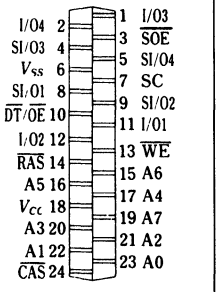
■ PIN OUT

HM53462P Series



(Top View)

HM53462ZP Series

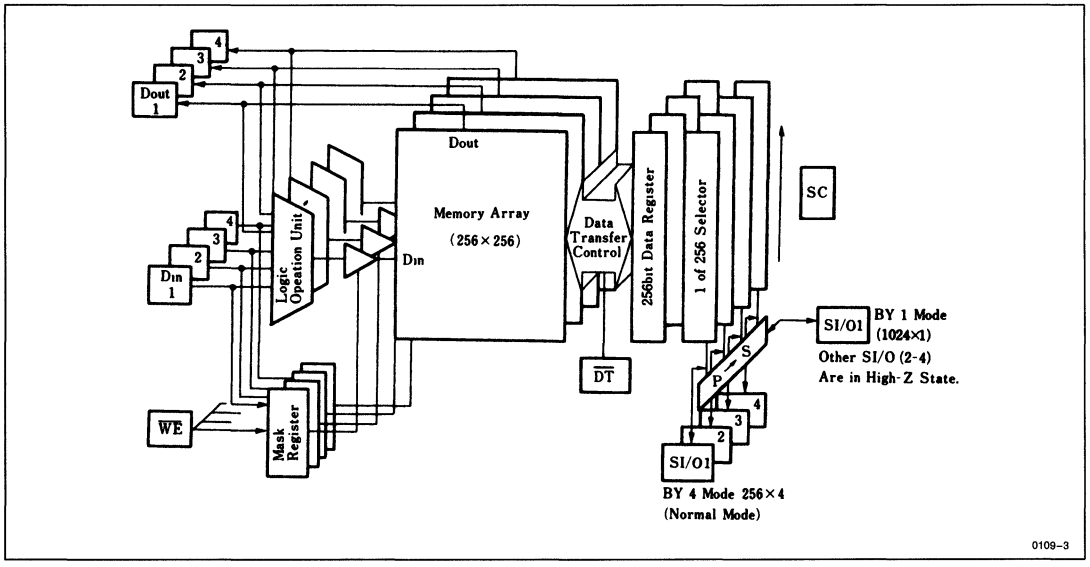


(Bottom View)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_7	Address Input
I/O_1–I/O_4	RAM Port Data Input/Output
SI/O_1–SI/O_4	SAM Port Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
SC	Serial Clock
$\overline{WE}$	Write Enable
$\overline{DT/OE}$	Data Transfer/Output Enable
$\overline{SOE}$	SAM Port Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	− 1.0 to + 7.0	V
Power Supply Voltage Relative to V_{SS}	V_{CC}	− 0.5 to + 7.0	V
Operating Temperature	T_{opr}	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W

■ INPUT/OUTPUT CAPACITANCE

Parameter	Symbol	Typ	Max	Unit	Note
Address	C_{I1}	—	5	pF	
Clocks	C_{I2}	—	5	pF	
I/O, SI/O	$C_{I/O}$	—	7	pF	

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.4	—	6.5	V	
Input Low Voltage	V_{IL}	− 0.5	—	0.8	V	2

Notes: 1. All voltages referenced to V_{SS}.
2. − 3.0V for pulse width ≤ 10 ns.

• DC Electrical Characteristics (T_A = 0 to + 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

RAM Port	Symbol	SAM Port		HM53462 -10	HM53462 -12	HM53462 -15	Unit	Note
		Standby	Active					
Operating Current $\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = min	I_{CC1}	—	×	70	60	50	mA	
	I_{CC7}	×	—	110	100	80	mA	
Standby Current $\overline{RAS}$, $\overline{CAS}$ = V_{IH}	I_{CC2}	—	×	7	7	7	mA	
	I_{CC8}	×	—	40	40	30	mA	
$\overline{RAS}$ Only Refresh Current $\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling t_{RC} = min	I_{CC3}	—	×	60	50	40	mA	
	I_{CC9}	×	—	100	90	70	mA	
Page Mode Current $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling t_{PC} = min	I_{CC4}	—	×	50	40	35	mA	
	I_{CC10}	×	—	90	80	65	mA	
CBR Refresh Current $\overline{RAS}$ Cycling t_{RC} = min	I_{CC5}	—	X	60	50	40	mA	
	I_{CC11}	×	—	100	90	70	mA	
Data Transfer Current $\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = min	I_{CC6}	—	×	75	65	55	mA	
	I_{CC12}	×	—	115	105	85	mA	

Parameter	Symbol	Min	Max	Unit	Note
Input Leakage	I_{LI}	− 10	10	μA	
Output Leakage	I_{LO}	− 10	10	μA	
Output High Voltage I_{OH} = − 2 mA	V_{OH}	2.4	—	V	
Output Low Voltage I_{OL} = 4.2 mA	V_{OL}	—	0.4	V	

• Electrical Characteristics and Recommended AC Operating Conditions

(T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)[1, 10, 11]

Parameter	Symbol	HM53462-10		HM53462-12		HM53462-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	190	—	220	—	260	—	ns	
Read-Modify-Write Cycle Time	t_{RWC}	260	—	300	—	355	—	ns	
Page Mode Cycle Time	t_{PC}	70	—	85	—	105	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	50	—	60	—	75	ns	3, 4
Outout Buffer Turn-off Delay Referenced to $\overline{CAS}$	t_{OFF1}	0	25	0	30	0	40	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
$\overline{RAS}$ Precharge Time	t_{RP}	80	—	90	—	100	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	50	25	60	30	75	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	50	—	60	—	75	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	25	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	35	—	40	—	45	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	35	—	40	—	45	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	25	—	25	—	30	—	ns	8, 9
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	
$\overline{RAS}$ Pulse Width (Read-Modify-Write Cycle	t_{RWS}	170	10000	200	10000	245	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	85	—	100	—	125	—	ns	8
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CHR}	20	—	25	—	30	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	15	—	20	—	ns	
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	35	—	40	ns	
Output Buffer Turn-off Delay Referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	25	—	30	—	40	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	15	—	20	—	ns	

• Electrical Characteristics and Recommended AC Operating Conditions (continued)

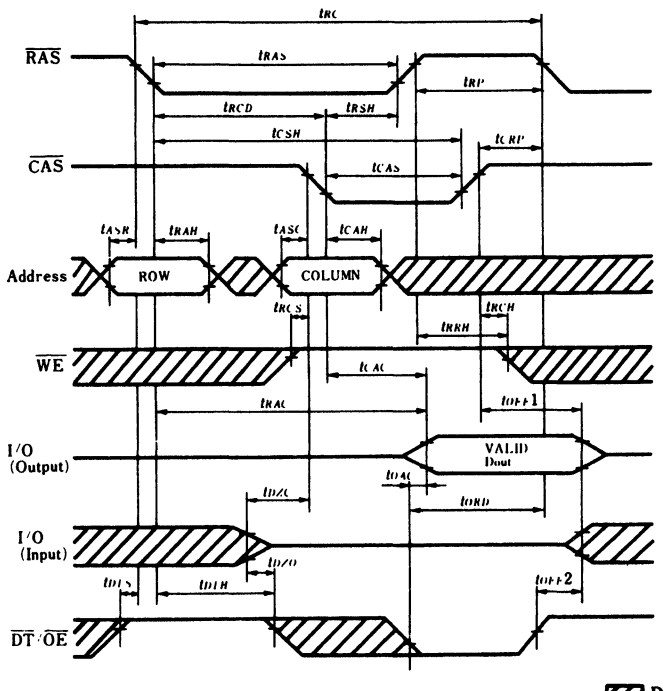
(T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)[1, 10, 11]

Parameter	Symbol	HM53462-10		HM53462-12		HM53462-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	0	—	ns	
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{OE}$ to $\overline{RAS}$ Delay Time	t_{ORD}	35	—	40	—	45	—	ns	
Serial Clock Cycle Time	t_{SCC}	40	—	40	—	60	—	ns	
Access Time from SC	t_{SCA}	—	40	—	40	—	60	ns	10
Access Time from $\overline{SOE}$	t_{SEA}	—	25	—	30	—	40	ns	10
SC Pulse Width	t_{SC}	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	ns	
Serial Data-out Hold Time after SC High	t_{SOH}	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{SOE}$	t_{SEZ}	0	25	0	25	0	30	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	25	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time (Read Transfer Cycle)	t_{RDH}	80	—	90	—	110	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	—	15	—	20	—	ns	
$\overline{DT}$ to $\overline{CAS}$ Hold Time	t_{CDH}	20	—	30	—	45	—	ns	
Last SC to $\overline{DT}$ Delay Time	t_{SDD}	5	—	5	—	10	—	ns	
First SC to $\overline{DT}$ Hold Time	t_{SDH}	25	—	25	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Delay Time	t_{DTR}	10	—	10	—	10	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	20	—	ns	
I/O to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	ns	
I/O to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	20	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	75	ns	
SC to $\overline{RAS}$ Setup Time	t_{SRS}	30	—	40	—	45	—	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	—	30	—	35	—	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	—	60	—	75	—	ns	
Serial Data Input to $\overline{DT}$ Delay Time	t_{SZD}	0	—	0	—	0	—	ns	
$\overline{SOE}$ to $\overline{RAS}$ Setup Time	t_{ES}	0	—	0	—	0	—	ns	
$\overline{SOE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	—	15	—	20	—	ns	
Serial Write Enable Setup Time	t_{SWS}	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	t_{SWH}	35	—	35	—	55	—	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	35	—	35	—	55	—	ns	
$\overline{DT}$ to Sout in Low-Z Delay Time	t_{DLZ}	5	—	10	—	10	—	ns	

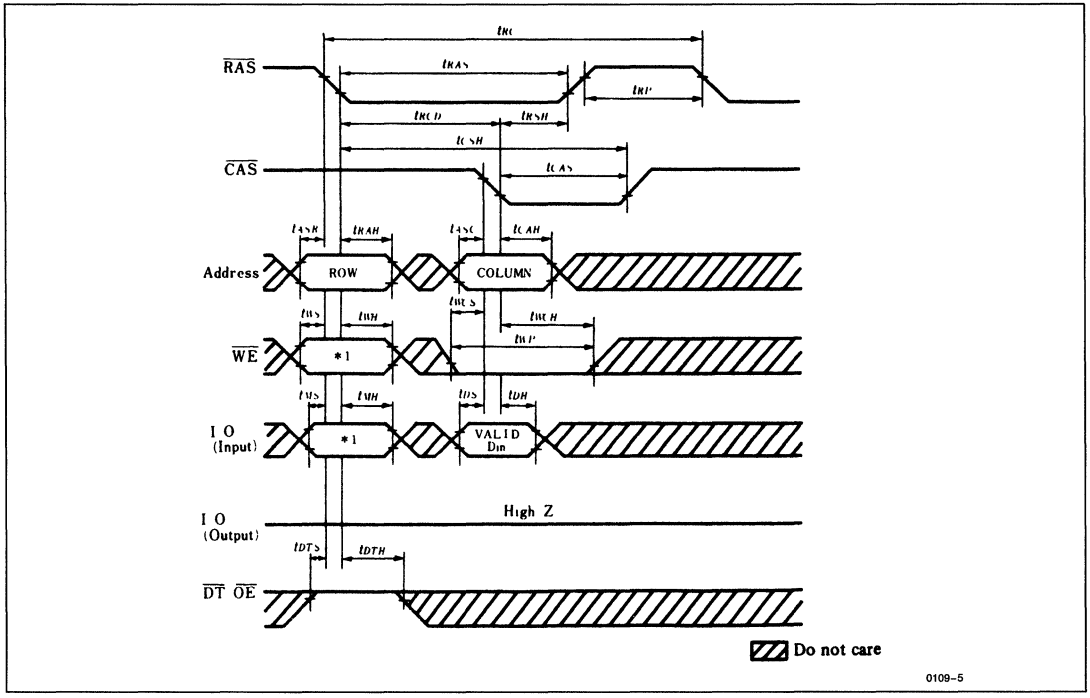
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WC}, and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycle and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. Measured with a load circuit equivalent to 2 TTL and 100 pF.
11. After power-up, pause for more than 100 μs and execute at least 8 initialization cycles. Then execute at least one logic reset cycle including write mask reset (on the falling edge of $\overline{RAS}$, $\overline{WE}$ = "Low" and I/O_I–I/O = "High"), and execute one or more transport cycle for initiation of SAM port.

■ TIMING WAVEFORMS

• Read Cycle

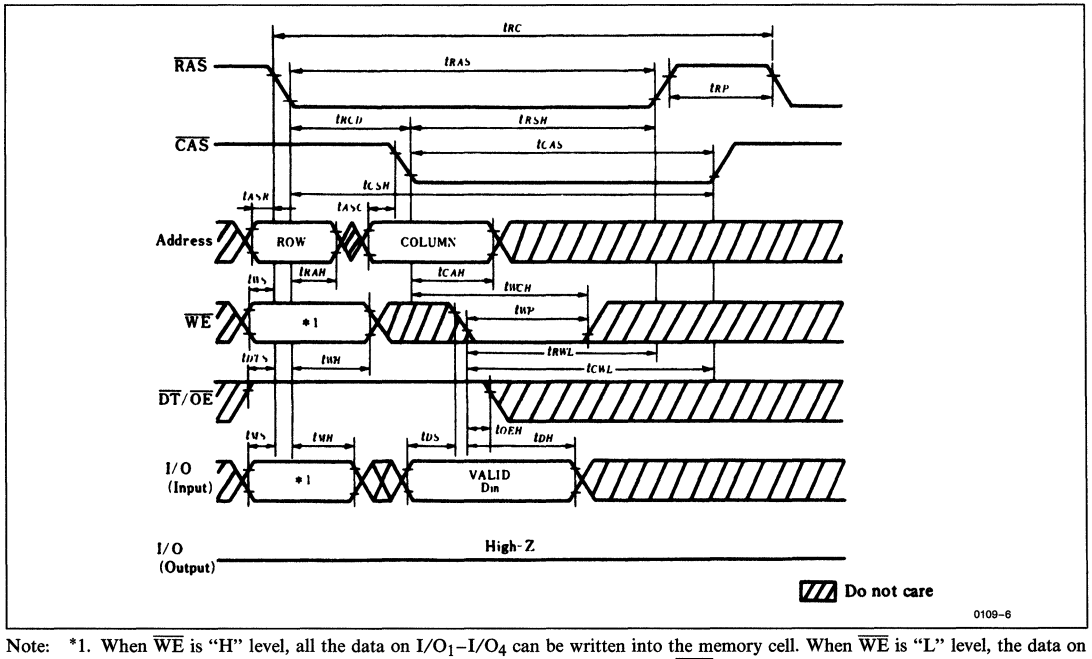


• Early Write Cycle



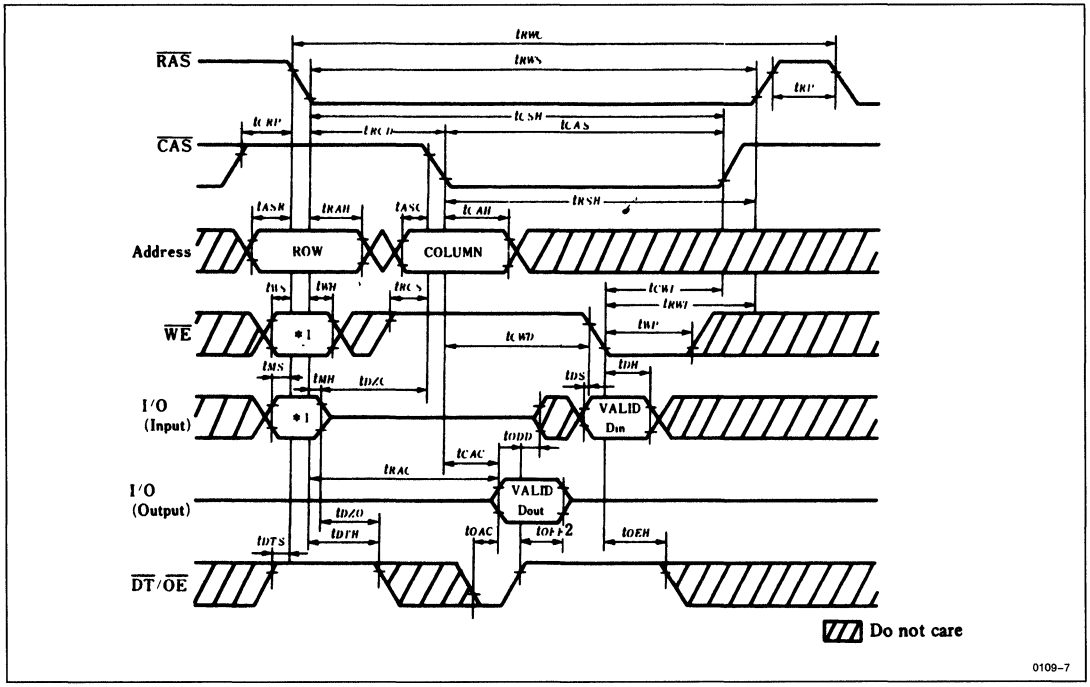
Notes: *1. When $\overline{WE}$ is "H" level, then all data on the I/O can be written into the cell. When $\overline{WE}$ is "L" level, the data on the I/O are not written except for when I/O is "H" level at the falling edge of $\overline{RAS}$.

• Delayed Write Cycle



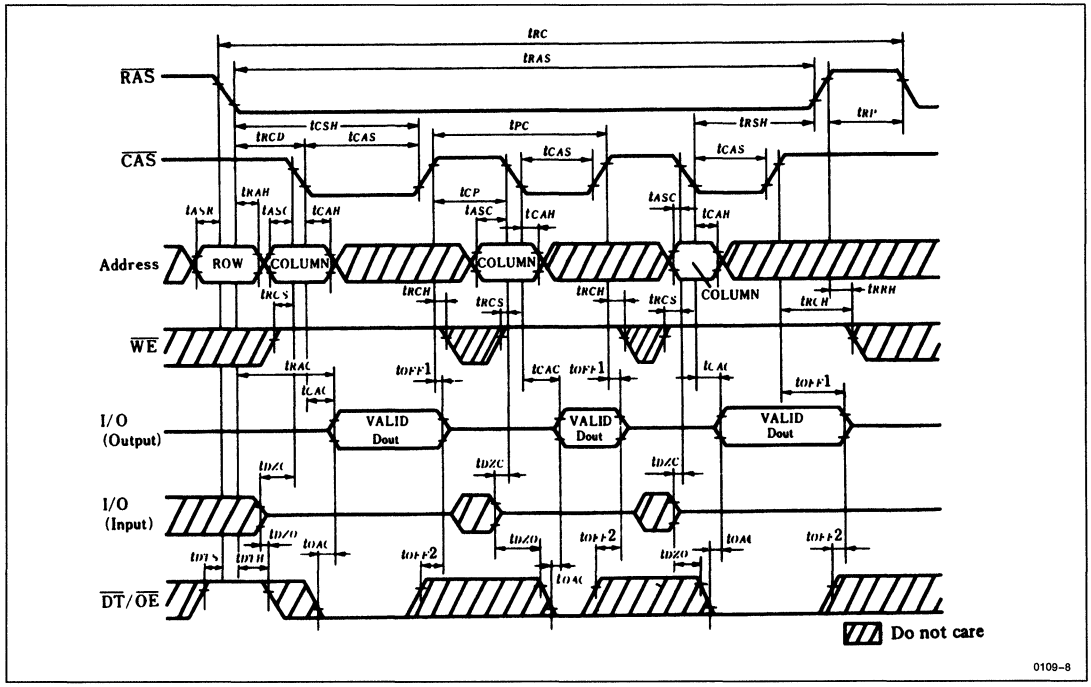
Note: *1. When $\overline{WE}$ is "H" level, all the data on I/O_1–I/O_4 can be written into the memory cell. When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

• **Read-Modify-Write Cycle**

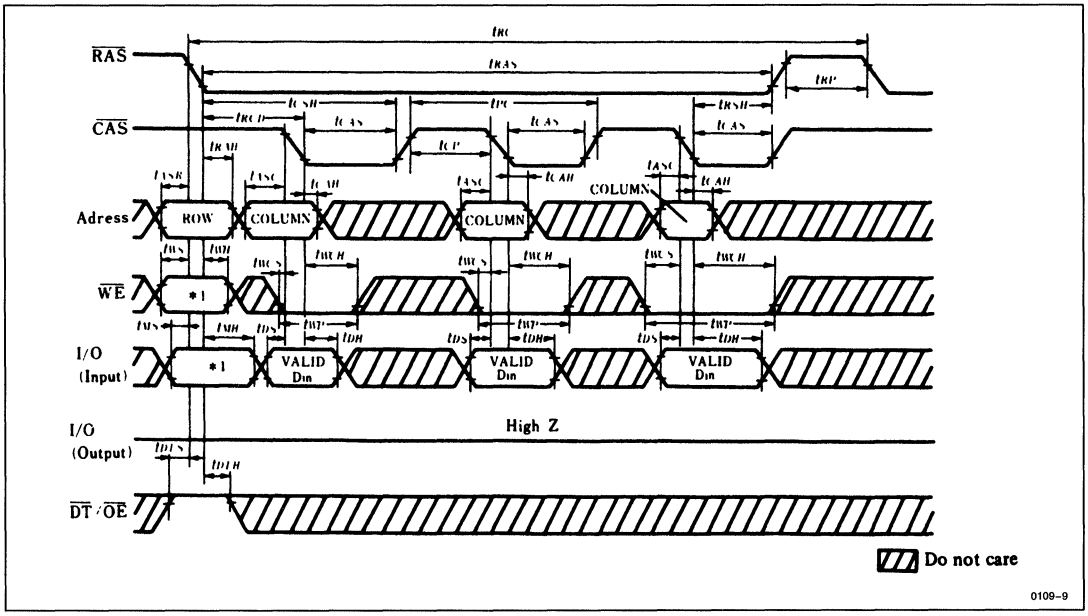


Note: *1. When $\overline{WE}$ is "H" level, all the data on I/O_1–I/O_4 can be written into the memory cell. When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

• **Page Mode Read Cycle**

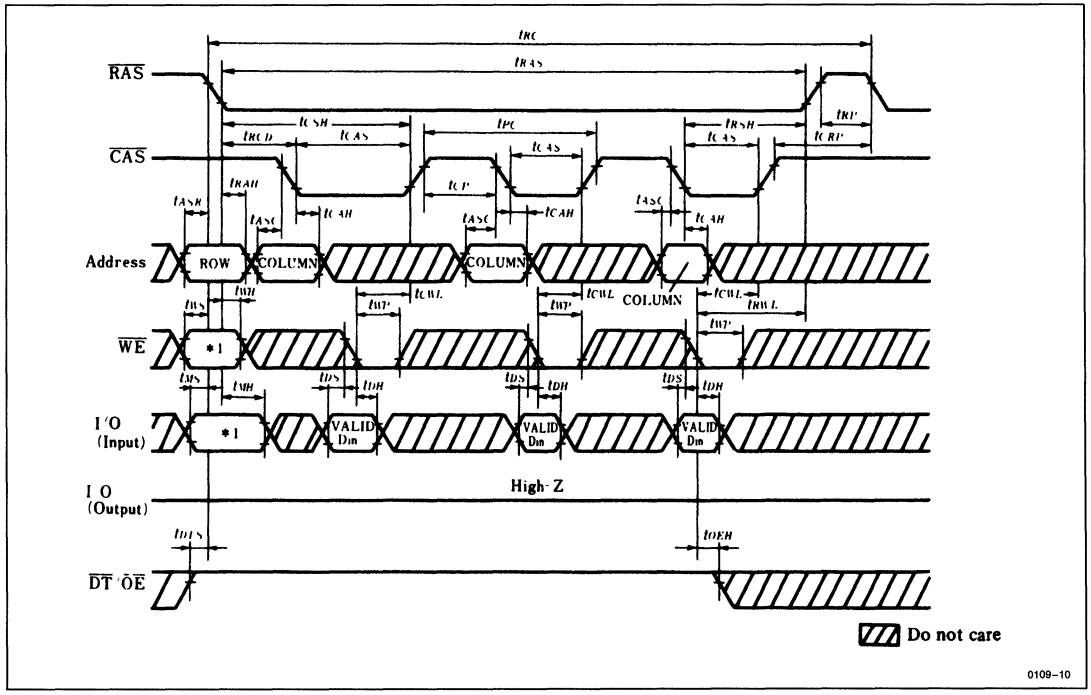


• **Page Mode Write Cycle (Early Write)**



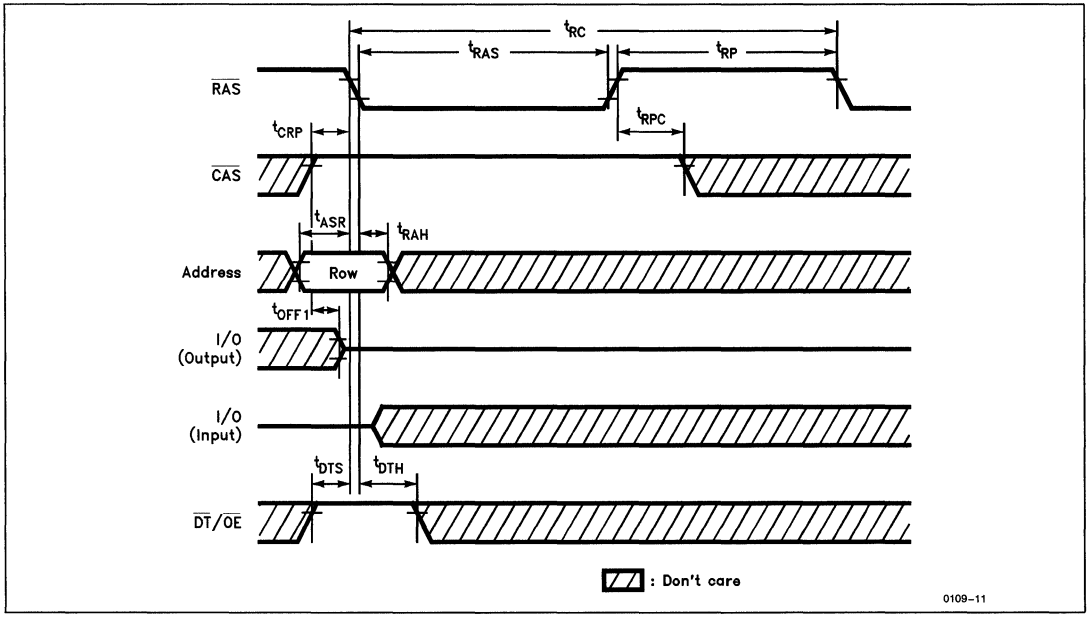
Note: *1. When $\overline{WE}$ is "H" level, all the data on I/O_1–I/O_4 can be written into the memory cell. When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

• **Page Mode Write Cycle (Delayed Write)**

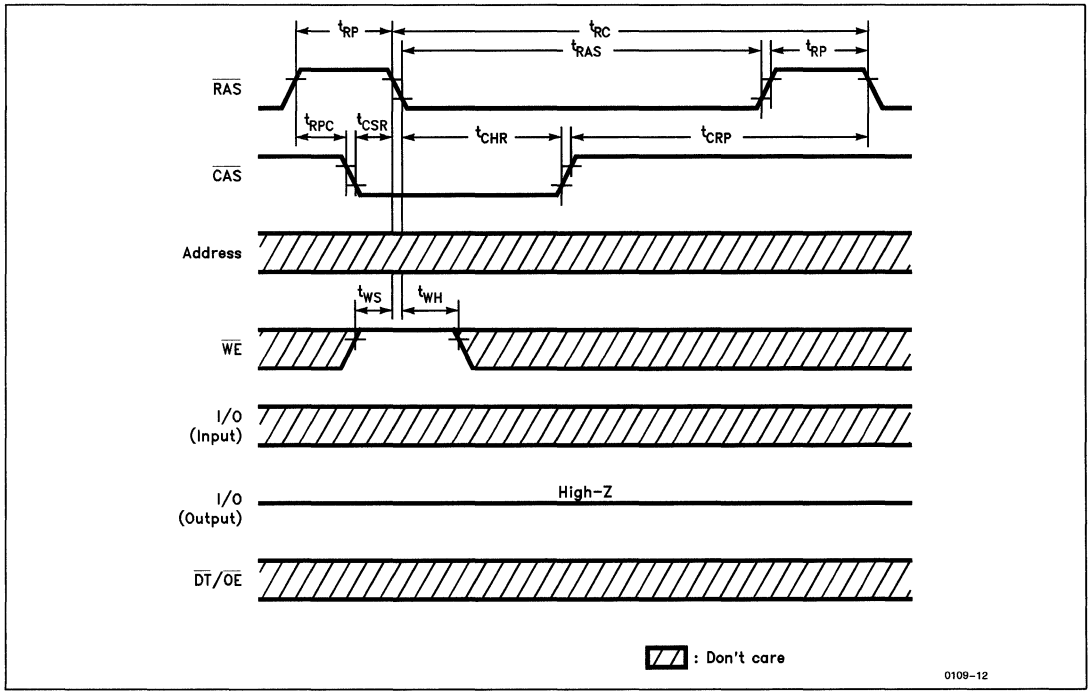


Note: *1. When $\overline{WE}$ is "H" level, all the data on I/O_1–I/O_4 can be written into the memory cell. When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

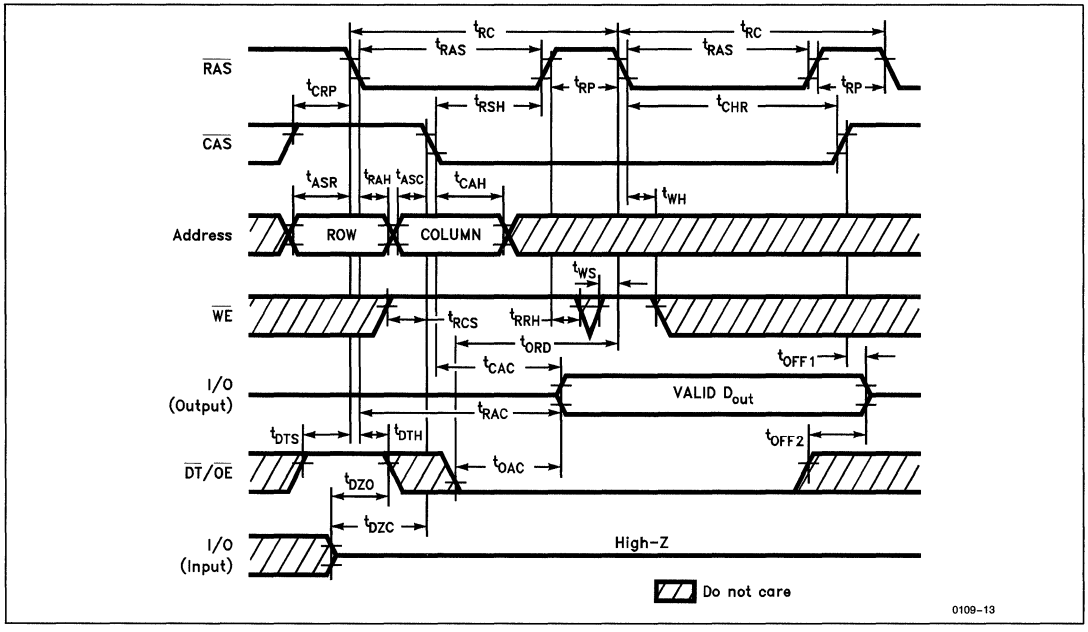
• $\overline{RAS}$ Only Refresh Cycle



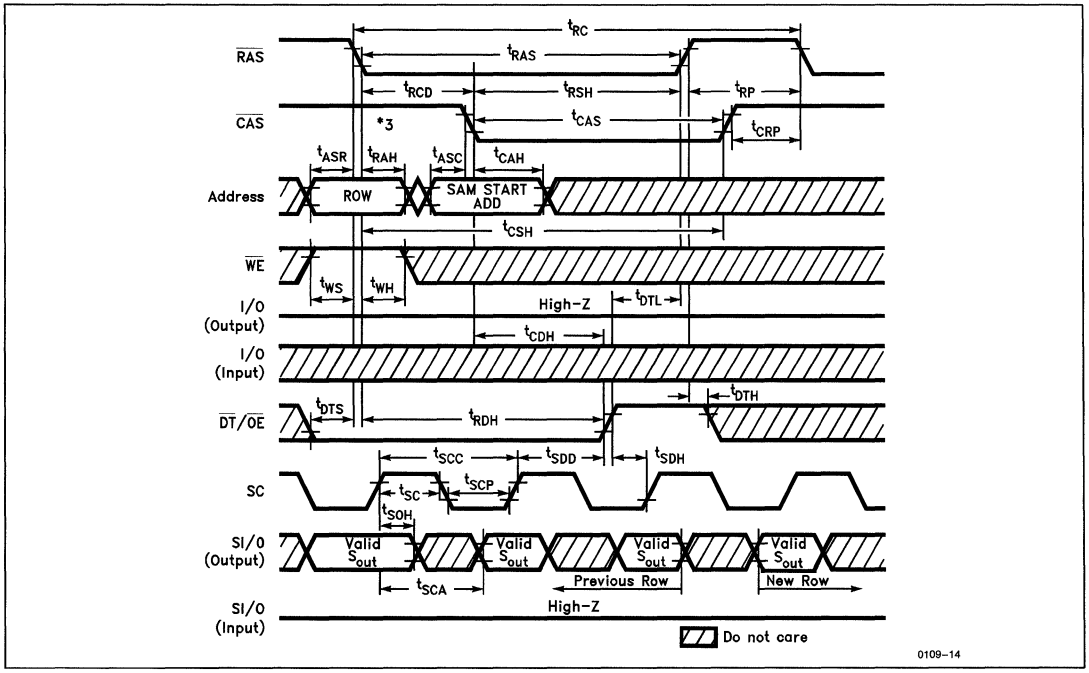
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• Hidden Refresh Cycle

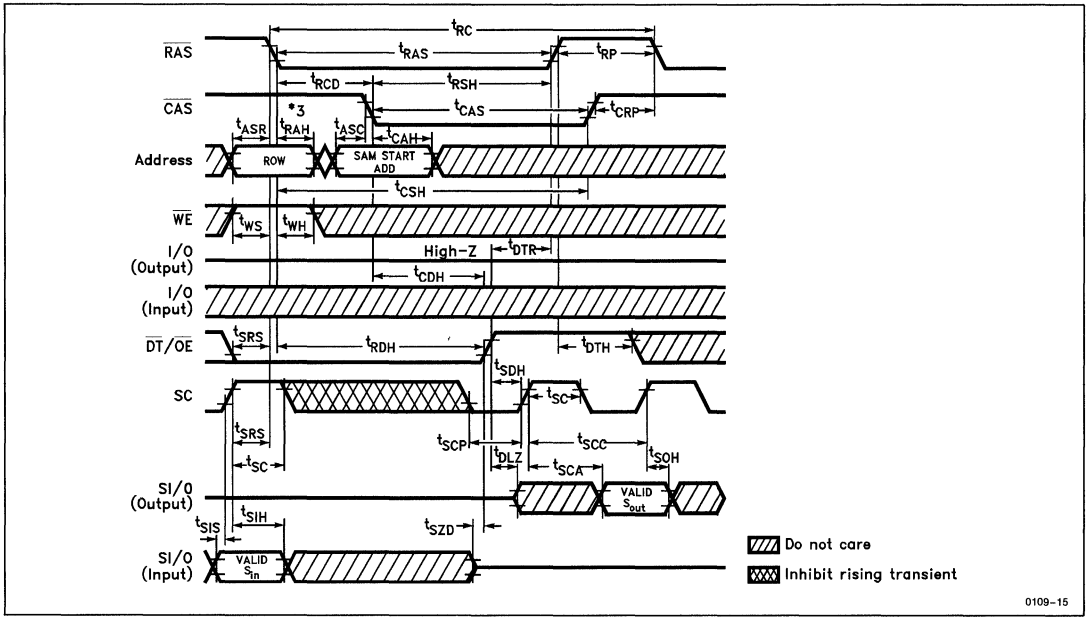


• Read Transfer Cycle (1)*1, *2



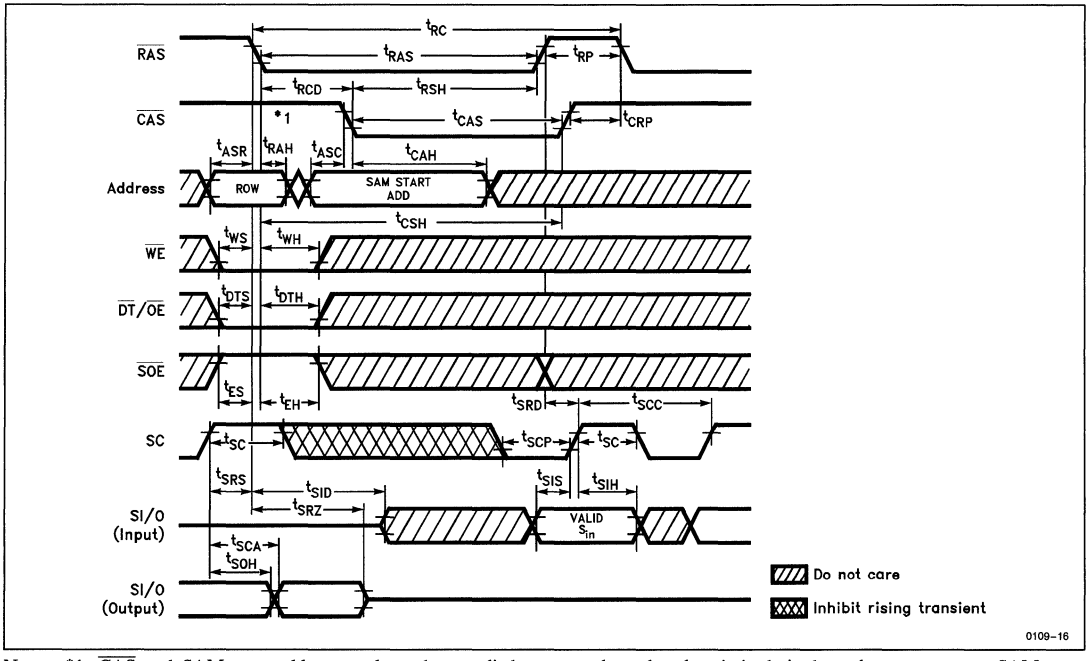
Notes: *1. In the case that the previous data transfer cycle was read transfer.
*2. Assume that $\overline{SOE}$ is "Low".
*3. $\overline{CAS}$ and SAM start Address need not be supplied every cycle, only when it is desired to change to a new SAM start Address.

• Read Transfer Cycle (2)*1, *2



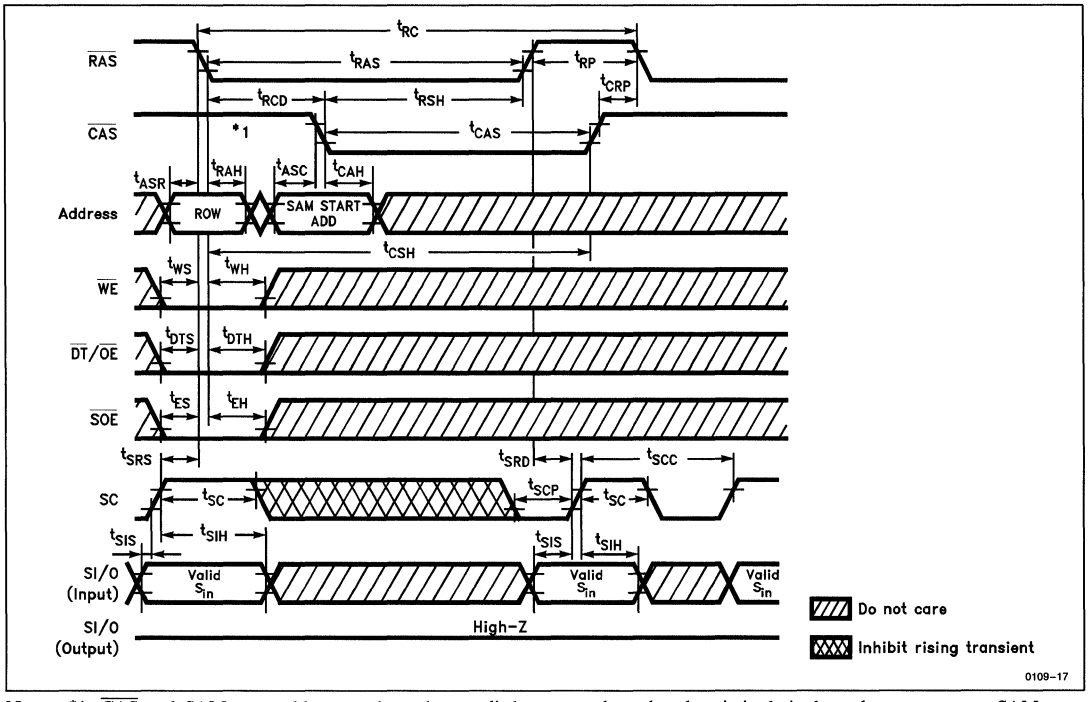
Notes: *1. In the case that the previous data transfer cycle was read transfer.
*2. Assume that $\overline{SOE}$ is "Low".
*3. $\overline{CAS}$ and SAM start Address need not be supplied every cycle, only when it is desired to change to a new $\overline{SAM}$ start Address.

• Pseudo Transfer Cycle



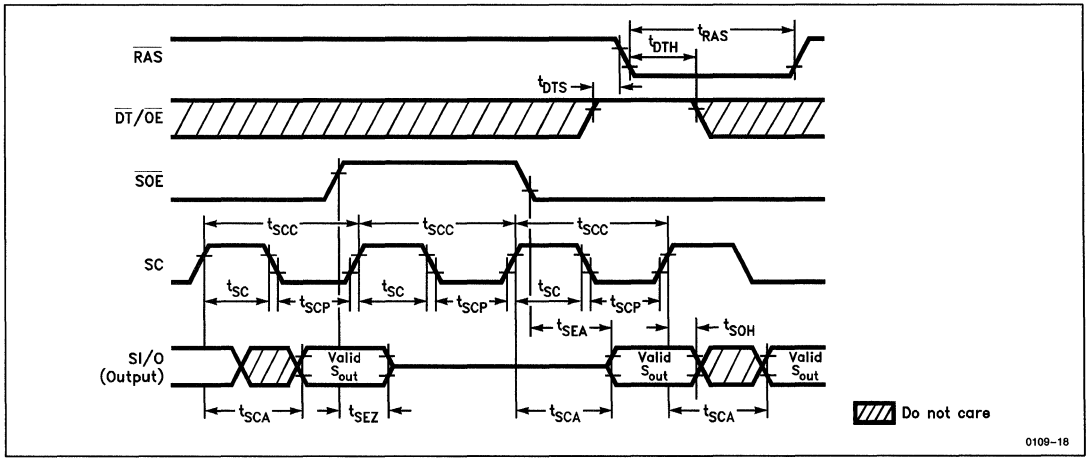
Note: *1. $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• Write Transfer Cycle

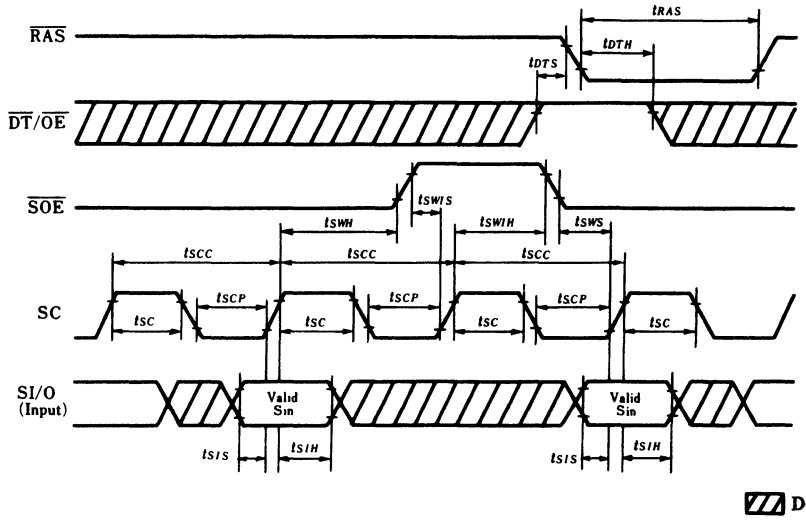


Note: *1. $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• Serial Read Cycle



• **Serial Write Cycle**



• **Electrical AC Characteristics** (Logic Operation Mode)

Parameter	Symbol	HM53462-10		HM53462-12		HM53462-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{FRC}	230	—	265	—	310	—	ns	
$\overline{RAS}$ Pulse Width in Write Cycle	t_{RFS}	140	10000	165	10000	200	10000	ns	
$\overline{CAS}$ Pulse Width in Write Cycle	t_{CFS}	80	10000	95	10000	105	10000	ns	
$\overline{CAS}$ Hold Time in Write Cycle	t_{FCSH}	140	—	165	—	200	—	ns	
$\overline{RAS}$ Hold Time in Write Cycle	t_{FRSH}	80	—	95	—	105	—	ns	
Page Mode Cycle Time (Write Cycle)	t_{FPC}	100	—	120	—	135	—	ns	
$\overline{CAS}$ Hold Time (Logic Operation Set/Reset Cycle)	t_{FCHR}	90	—	100	—	120	—	ns	
$\overline{CAS}$ Hold Time from $\overline{RAS}$ Precharge (x4 → x1 Set Cycle)	t_{PSCH}	10	—	10	—	10	—	ns	

• **Logic Code** (FC0–3 are AX0–AX3 in Logic Operation Set Cycle)

FC3	FC2	FC1	FC0	LOGIC	
				Symbol	Write Data
0	0	0	0	0	Zero
0	0	0	1	AND1	Di•Mi
0	0	1	0	AND2	$\overline{Di}$•Mi
0	0	1	1	X4 → X1	—
0	1	0	0	AND3	Di•$\overline{Mi}$
0	1	0	1	THROUGH	Di
0	1	1	0	EOR	$\overline{Di}$•Mi + Di•$\overline{Mi}$
0	1	1	1	OR1	Di + Mi
1	0	0	0	NOR	$\overline{Di}$•$\overline{Mi}$
1	0	0	1	ENOR	Di•Mi + $\overline{Di}$•$\overline{Mi}$
1	0	1	0	INV1	$\overline{Di}$
1	0	1	1	OR2	$\overline{Di}$ + Mi
1	1	0	0	INV2	$\overline{Mi}$
1	1	0	1	OR3	Di + $\overline{Mi}$
1	1	1	0	NAND	$\overline{Di}$ + $\overline{Mi}$
1	1	1	1	1	ONE

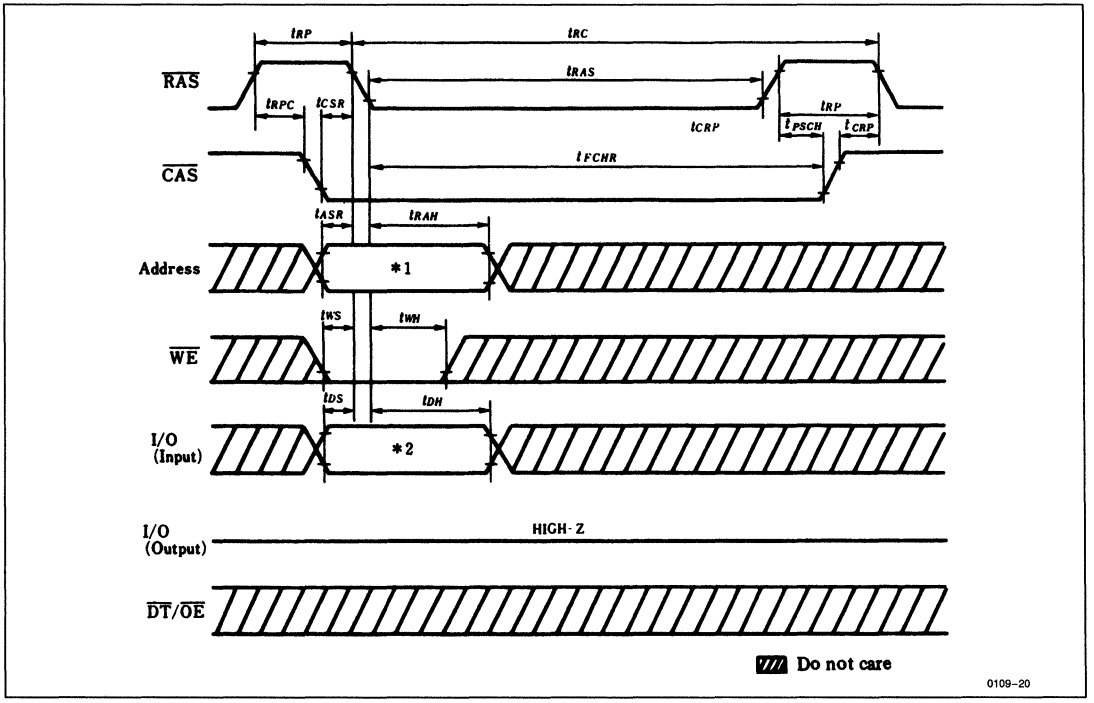
→ SAM Organization Changes to 1024 x 1

→ Logic Operation Mode Reset

Di :External Data-in

Mi :The Data of the Memory Cell

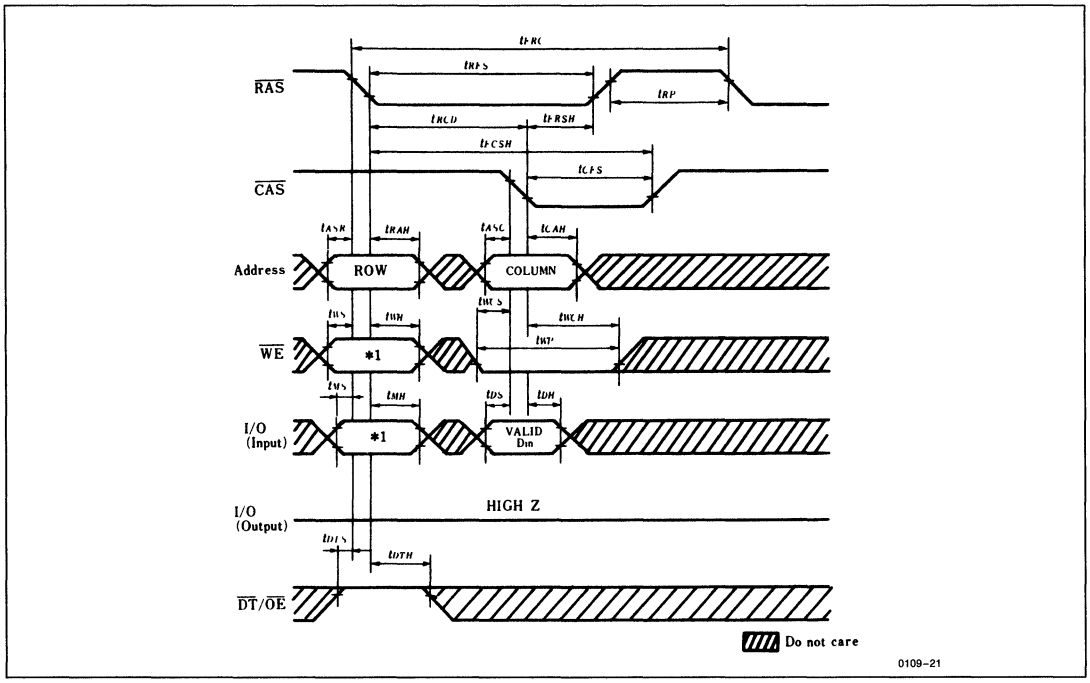
• **Logic Operation Set Reset Cycle** (With $\overline{CAS}$ Before $\overline{RAS}$ Refresh)



Notes: *1. Logic code A_0–A_3 (A_4–A_7: don't care)
*2. Write mask data.

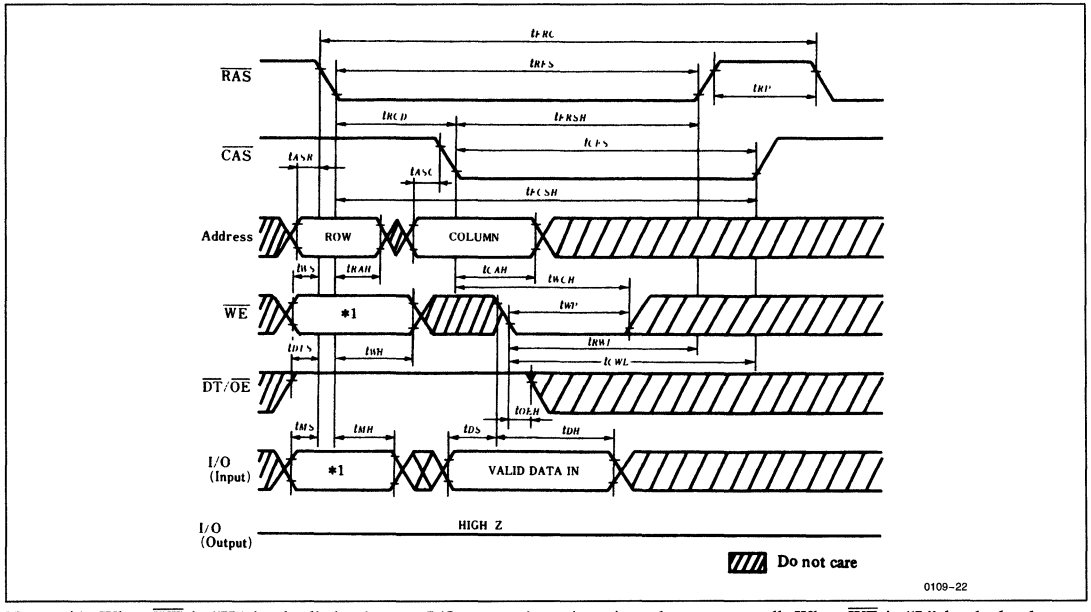
■ LOGIC OPERATION MODE

• Early Write Cycle



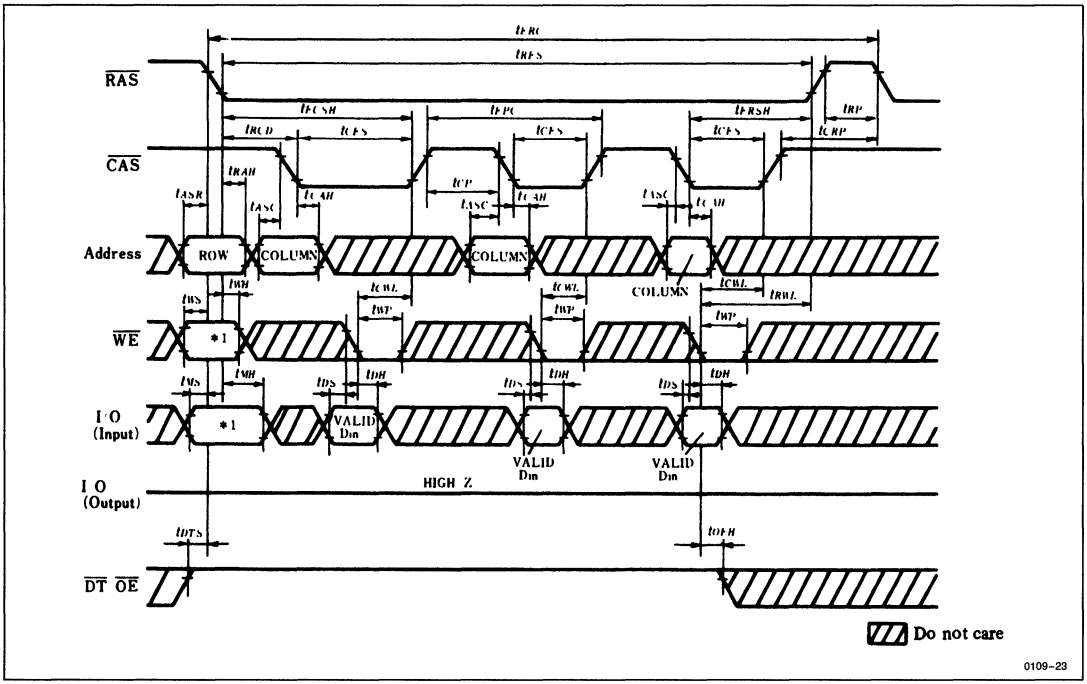
Note: *1. When $\overline{WE}$ is "high", the all data on the I/O can be written into the cell. When $\overline{WE}$ is "low", the data on the I/O are not written except for when I/O is "high" at the falling edge of $\overline{RAS}$.

• Delayed Write Cycle



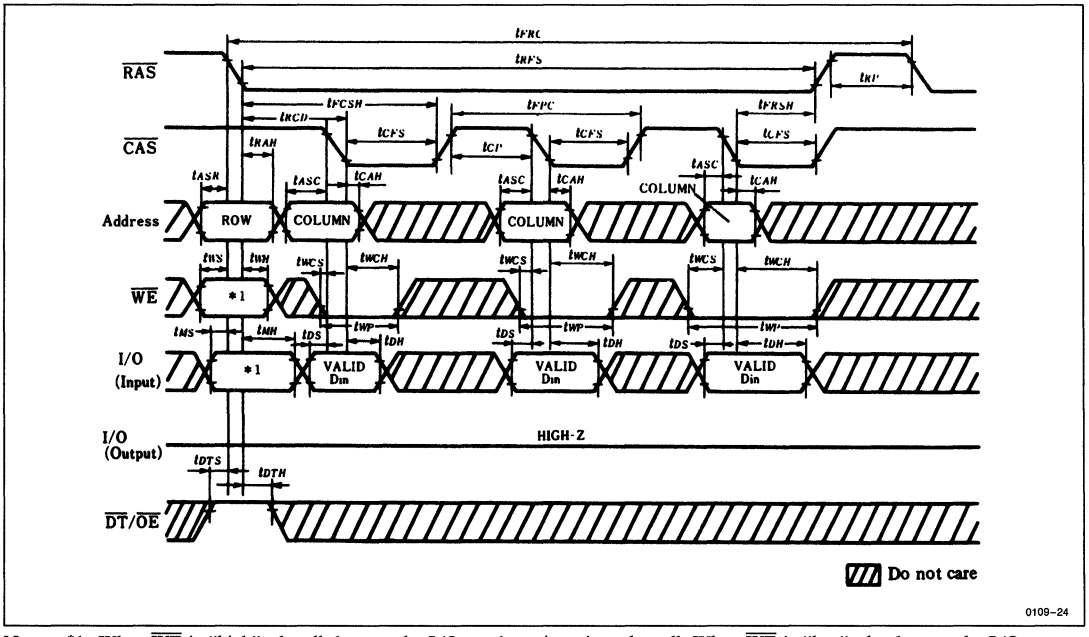
Note: *1. When $\overline{WE}$ is "H" level, all the data on I/O_{1-4} can be written into the memory cell. When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

• **Page Mode Write Cycle** (Delayed Write)



Note: *1. When $\overline{WE}$ is "high", the all data on the I/O can be written into the cell. When $\overline{WE}$ is "low", the data on the I/O are not written except for when I/O is "high" at the falling edge of $\overline{RAS}$.

• **Page Mode Write Cycle (Early Write)**



Note: *1. When $\overline{WE}$ is "high", the all data on the I/O can be written into the cell. When $\overline{WE}$ is "low", the data on the I/O are not written except for when I/O is "high" at the falling edge of $\overline{RAS}$.

■ DESCRIPTION

1. LOGIC OPERATION MODE

HM53462 has an internal logic operation unit which makes a process of graphics simple. The logic is determined in "Logic operation set/reset cycle", and the operation is executed in every write cycle succeeding to the logic operation set/reset cycle. In this mode the internal read-modify-write operation is executed and the cell data is converted into the new data given by the logic operation between D_{in} and the old cell data.

2. LOGIC OPERATION SET/RESET CYCLE

A logic operation set/reset cycle is performed by bringing $\overline{CAS}$ and $\overline{WE}$ low when $\overline{RAS}$ falls (Fig. 1). The logic code and the bits to be masked are determined respectively by AX0–3 state and I/O_{1-4} state at the falling edge of $\overline{RAS}$. Furthermore, in this cycle $\overline{CAS}$ before $\overline{RAS}$ refresh operation is executed, too. In this case of executing the conventional $\overline{CAS}$ before $\overline{RAS}$ refresh operation, $\overline{WE}$ must be high when $\overline{RAS}$ falls.

2.1 Logic Code

The logic code is shown in Table 1. When power is turned on, at least one logic reset cycle including write mask reset is required to initialize logic code. If the logic code is (AX3, AX2, AX1, AX0) = (0, 0, 1, 1), the SAM organization is changed converter (Fig. 2). In the case that the SAM organization is changed to 1024 x 1, one data transfer cycle is needed to initialize the SAM selector.

One the SAM organization is changed to 1024 x 1, this code is maintained unless power is turned off.

2.2 Write Mask

HM53462 has two kinds of mask registers (register 1, 2). The register 1 is set by bringing $\overline{WE}$ low at the falling edge of $\overline{RAS}$ during the write cycle, and the mask data is available only in this cycle. The register 2 is set by level of I/O in the logic operation set/reset cycle, and the mask data is available until the next logic operation set/reset cycle. If the register 1 is set during the current logic operation mode, the mask data of the register 1 is preferred (that of the register 2 is ignored) and the logic becomes "THROUGH" only in this cycle (Fig. 3).

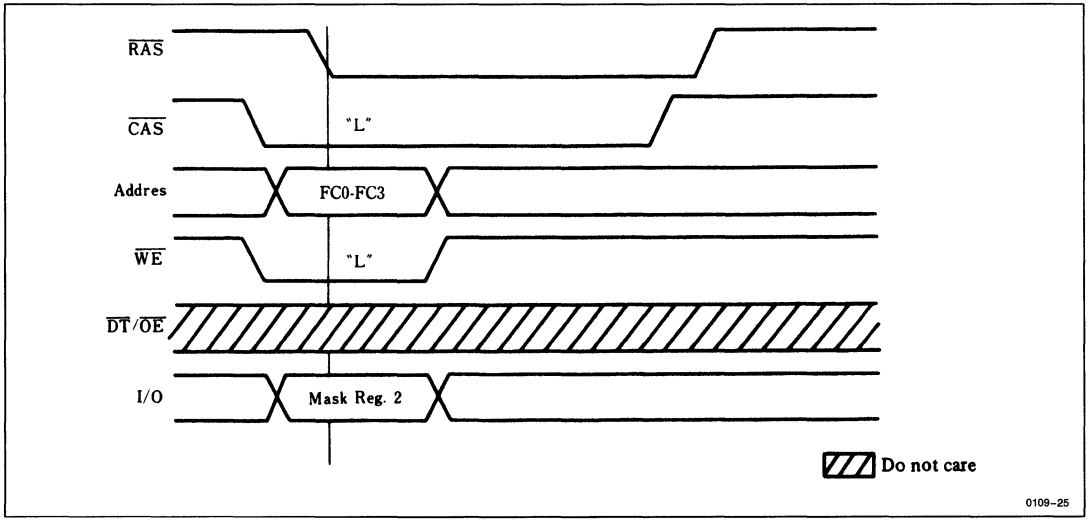


Figure 1. Logic Operation Set/Reset Cycle

• Table 1. Logic Code (FC0–FC3 are AX0–AX3 in Logic Operation Set Cycle)

FC3	FC2	FC1	FC0	LOGIC	
				Symbol	Write Data
0	0	0	0	0	Zero
0	0	0	1	AND1	Di•Mi
0	0	1	0	AND2	$\overline{Di}$•Mi
0	0	1	1	X4 → X1	—
0	1	0	0	AND3	Di•$\overline{Mi}$
0	1	0	1	THROUGH	Di
0	1	1	0	EOR	$\overline{Di}$•Mi + Di•$\overline{Mi}$
0	1	1	1	OR1	Di + Mi
1	0	0	0	NOR	$\overline{Di}$•$\overline{Mi}$
1	0	0	1	ENOR	Di•Mi + $\overline{Di}$•$\overline{Mi}$
1	0	1	0	INV1	$\overline{Di}$
1	0	1	1	OR2	$\overline{Di}$ + Mi
1	1	0	0	INV2	$\overline{Mi}$
1	1	0	1	OR3	Di + $\overline{Mi}$
1	1	1	0	NAND	$\overline{Di}$ + $\overline{Mi}$
1	1	1	1	1	ONE

→ SAM Organization Changes to 1024 x 1

→ Logic Operation Mode Reset

Di :External Data-in

Mi :The Data of the Memory Cell

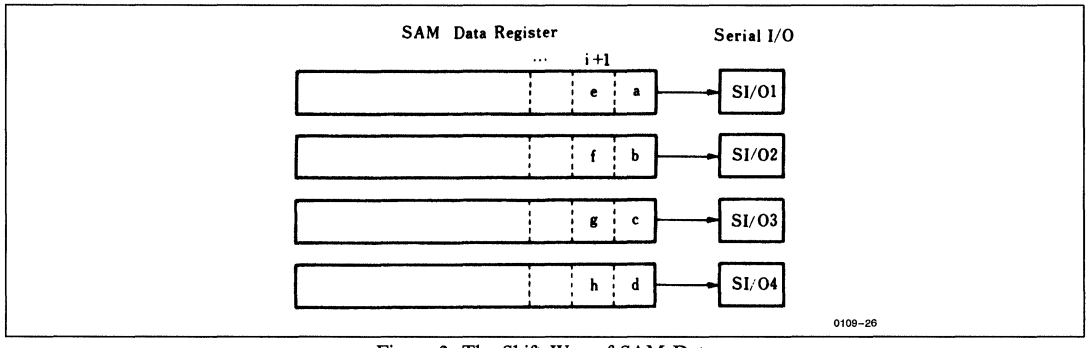
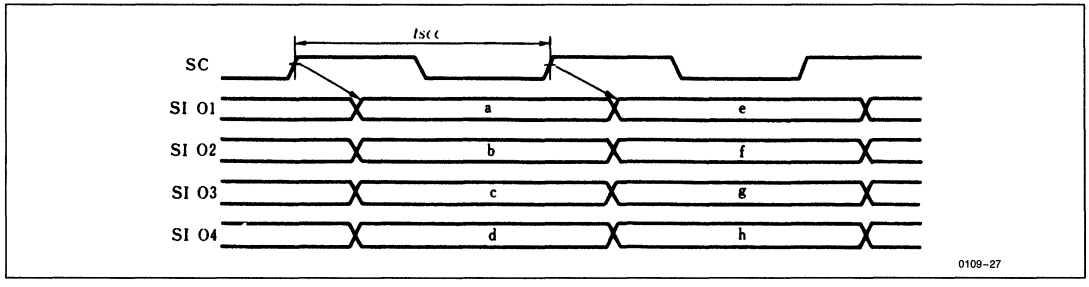
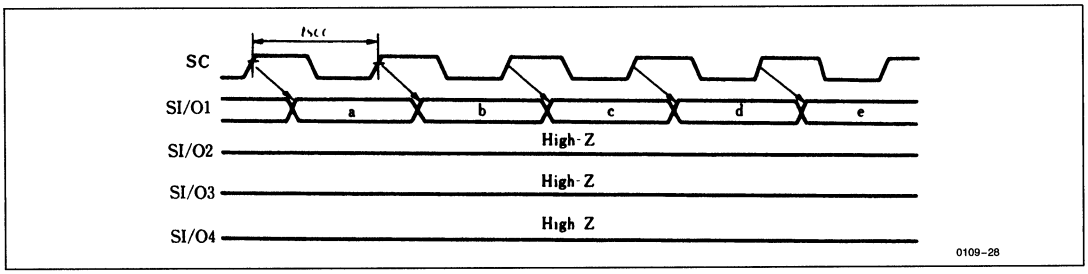


Figure 2. The Shift Way of SAM Data

1) By 4 Mode (SAM Organization: 256 x 4)



2) By 1 Mode (SAM Organization: 1024 x 1)



	Logic operation set/reset cycle	Write cycle	Write cycle	Write cycle	Write cycle
$\overline{RAS}$					
$\overline{CAS}$	"L"	"H"	"H"	"H"	"H"
$\overline{WE}$	"L"	"H"	"L"	"H"	"H"
I/O1		"0" Write	Masked	"1" Write	"0" Write
I/O2		Masked	"1" Write	Masked	Masked
I/O3		Masked	"0" Write	Masked	Masked
I/O4		"1" Write	Masked	"0" Write	"1" Write
Logic	—	AND1	THROUGH	AND1	AND1
	Mask reg.2 is set I O2,3 :Masked Assume that the logic is set to "AND1".		Mask reg.1 is set, and valid only in this cycle. I O1,4:Masked		

0109-29

Figure 3. Example of Logic Operation Mode

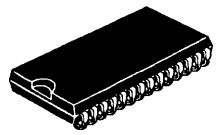
HM534251 Series

262,144 x 4-Bit Multiport CMOS Video Random Access Memory

■ DESCRIPTION

The HM534251 is a 1-Mbit multiport video RAM equipped with a 256k-word x 4-bit dynamic RAM and a 512-word x 4-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has a write mask function. It is suitable for a graphic processing buffer memory.

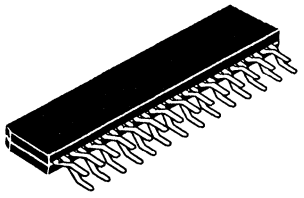
HM534251JP Series



3DCP28D

(CP-28D)

HM534251ZP Series



3DZP28

(ZP-28)

■ FEATURES

- Multiport Organization
  - Asynchronous and Simultaneous Operation of RAM and SAM Capability
  - RAM: 256k-word x 4-bit and SAM: 512-word x 4-bit
- Access Time
  - RAM .....100 ns/100 ns/120 ns/150 ns (max)
  - SAM .....30 ns/35 ns/40 ns/50 ns (max)
- Cycle Time
  - RAM .....190 ns/190 ns/220 ns/260 ns (min)
  - SAM .....30 ns/40 ns/40 ns/60 ns (min)
- Low Power
  - Active
    - RAM .....385 mW (max)
    - SAM .....358 mW (max)
  - Standby .....40 mW (max)
- High-Speed Page Mode Capability
- Mask Write Mode Capability
- Bidirectional Data Transfer Cycle between RAM and SAM Capability
- Real Time Read Transfer Capability
- 3 Variations of Refresh (8 ms/512 Cycles)
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- TTL Compatible

■ ORDERING INFORMATION

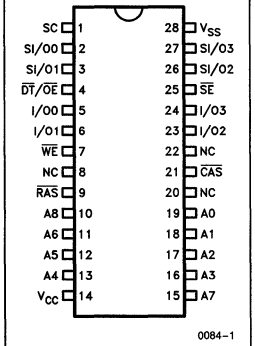
Part No.	Access Time	Package
HM534251JP-10	100 ns	400 mil
HM534251JP-11	100 ns	28-pin
HM534251JP-12	120 ns	Plastic SOJ
HM534251JP-15	150 ns	(CP-28D)
HM534251ZP-10	100 ns	400 mil
HM534251ZP-11	100 ns	28-pin
HM534251ZP-12	120 ns	Plastic ZIP
HM534251ZP-15	150 ns	(ZP-28)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Inputs
I/O_0–I/O_3	RAM Port Data Inputs/Outputs
SI/O_0–SI/O_3	SAM Port Data Inputs/Outputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
SC	Serial Clock
$\overline{SE}$	SAM Port Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	Non Connection

■ PIN OUT

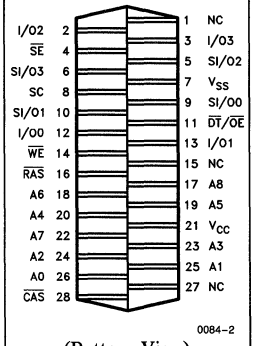
HM534251JP Series



0084-1

(Top View)

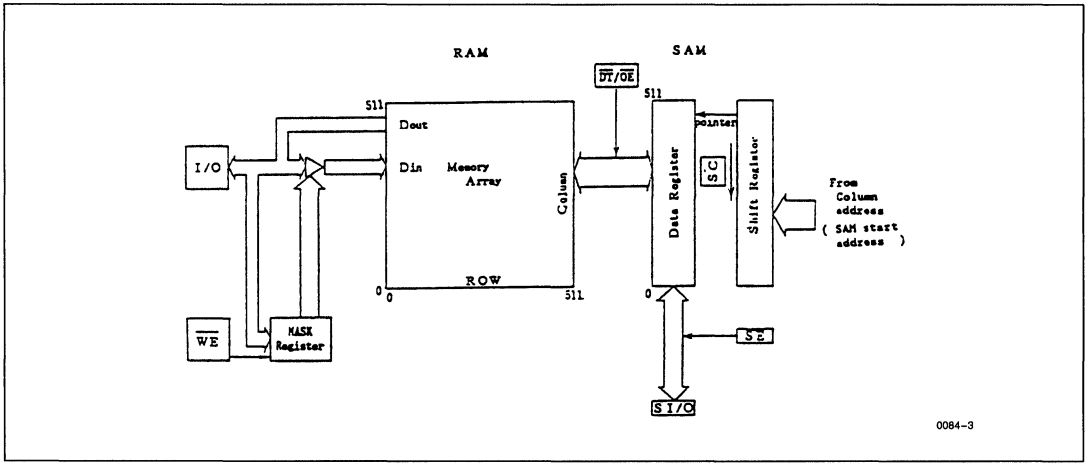
HM534251ZP Series



0084-2

(Bottom View)

■ BLOCK DIAGRAM



■ PIN FUNCTION

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in Table 1 are input at the falling edge of $\overline{RAS}$. The input level of those signals determine the operation cycle of the HM534251.

• Table 1. Operation Cycles of the HM534251

Input Level at the Falling Edge of $\overline{RAS}$				Operation Cycle
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SE}$	
H	H	H	X	RAM Read/Write
H	H	L	X	Mask Write
H	L	H	X	Read Transfer
H	L	L	H	Pseudo Transfer
H	L	L	L	Write Transfer
L	X	X	X	CBR Refresh

Note: X: Don't care.

$\overline{CAS}$ (input pin): Column address is put into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A_0–A_8 (input pins): Row address is determined by A_0–A_8 level at the falling edge of $\overline{RAS}$. Column address is determined by A_0–A_8 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM534251 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O_0–I/O_3 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only on high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data is output from an SI/O pin synchronously with the rising edge of SC,. In a serial write cycle, data on an SI/O pin at the rising edge of SC is put into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not put into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O_0–SI/O_3 (input/output pins): SI/O's are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle of write transfer cycle, SI/O inputs data.

■ OPERATION OF HM534251

• Operation of RAM Port

RAM Read Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high, at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data is output through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write) ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after $\overline{RAS}$ is set low, a write cycle is executed and I/O data is written at the selected addresses. When all 4 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling edge. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables write after read to execute in the same address cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and setting $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is preserved. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is preserved during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle and is higher than the standard page mode cycle by 70–80%. This product is based on static column mode, therefore, address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 256-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 μs).

• Transfer Operation

HM534251 provides the read transfer cycle, pseudo transfer cycle, and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$.

They have the following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)

(2) Determine direction of data transfer

(a) Read transfer cycle: RAM → SAM

(b) Write transfer cycle: RAM ← SAM

(3) Determine input or output of SAM I/O pin (SI/O)

Read transfer cycle: SI/O output

Pseudo transfer cycle, write transfer cycle: SI/O input

(4) Determine first SAM address to access (SAM start address) after transferring at column address.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by setting $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address data (512 x 4-bit) determined by this cycle is transferred synchronously at the rising of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address decided by column address.

This cycle can execute SAM access serially even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) is specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge, and t_{SDH} (min) between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge (see Figure 1).

If read transfer cycle is executed, SI/O becomes output state. When the previous transfer cycle is either pseudo transfer cycle or write transfer cycle and SI/O is in input state, uncertain data is output after t_{RLZ} (min) after the $\overline{RAS}$ falling edge. Before that, input should be set high impedance to avoid data contention.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle is available for switching SI/O from output state to input state because data in RAM isn't rewritten. This cycle starts when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high, at the falling edge of $\overline{RAS}$. The output buffer in SI/O becomes high impedance within t_{SRZ} (max) from the $\overline{RAS}$ falling edge. Data should be input to SI/O later than t_{SID} (min) to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC should not be raised.

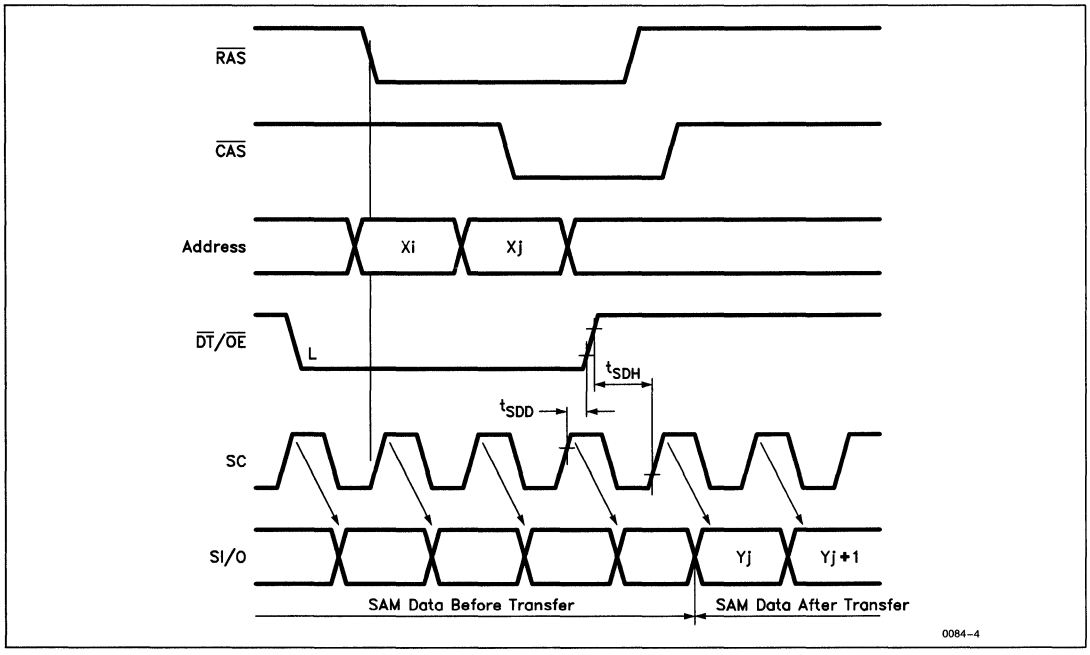


Figure 1. Real Time Read Transfer

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address to serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC should not be raised.

• SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. If $\overline{SE}$ is set high SI/O becomes high impedance and internal pointer is incremented at the SC rising edge.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is programmed into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't input into data register. Internal pointer is incremented according to the SC rising edge, so $\overline{SE}$ high can mask data for SAM.

• Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is performed by accessing all 512 row addresses every 8 ms. There are three refresh cycles: (1) $\overline{RAS}$ only refresh cycle, (2) $\overline{CAS}$ before $\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required for accessing all row addresses every 8 ms.

$\overline{RAS}$ Only Refresh Cycle: $\overline{RAS}$ only refresh cycle is performed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high by inputting the row address (= refresh address) from external circuits. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ should be high at the falling edge of $\overline{RAS}$.

CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.

Hidden Refresh Cycle: Hidden refresh cycle performs refresh by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register, selector), organized as fully static circuitry, don't require refresh.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Note
Terminal Voltage	V_T	1.0 to +7.0	V	1
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V	1
Power Dissipation	P_T	1.0	W	
Operating Temperature	T_{opr}	0 to +70	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

Note: 1. Relative to V_{SS}

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−0.5	—	0.8	V	1, 2

Notes: 1. All voltage referenced to V_{SS}.
2. −3.0V for pulse width ≤ 10 ns.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Test Conditions		Note
		Min	Max	Min	Max	Min	Max	Min	Max		RAM Port	SAM Port	
Operating Current	I_{CC1}	—	70	—	70	—	60	—	55	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	$\overline{SE}$ = V_{IH}, SC = V_{IL}	1, 2
	I_{CC7}	—	120	—	120	—	100	—	85	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Standby Current	I_{CC2}	—	7	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	$\overline{SE}$ = V_{IH}, SC = V_{IL}	1
	I_{CC8}	—	65	—	55	—	55	—	40	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	70	—	70	—	60	—	55	mA	$\overline{RAS}$ Cycling $\overline{CAS}$ = V_{IH} t_{RC} = Min	$\overline{SE}$ = V_{IH}, SC = V_{IL}	2
	I_{CC9}	—	120	—	120	—	100	—	85	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Page Mode Current	I_{CC4}	—	80	—	80	—	70	—	60	mA	$\overline{CAS}$ Cycling $\overline{RAS}$ = V_{IL} t_{RC} = Min	$\overline{SE}$ = V_{IH}, SC = V_{IL}	1, 3
	I_{CC10}	—	130	—	130	—	110	—	90	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC5}	—	60	—	60	—	50	—	40	mA	$\overline{RAS}$ Cycling t_{RC} = Min	$\overline{SE}$ = V_{IH}, SC = V_{IL}	
	I_{CC11}	—	110	—	110	—	90	—	70	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Data Transfer Current	I_{CC6}	—	95	—	95	—	90	—	85	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	$\overline{SE}$ = V_{IH}, SC = V_{IL}	2
	I_{CC12}	—	135	—	135	—	125	—	115	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	−10	10	μA			
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	−10	10	μA			
Output High Voltage	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V	I_{OH} = −2 mA		
Output Low Voltage	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA		

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

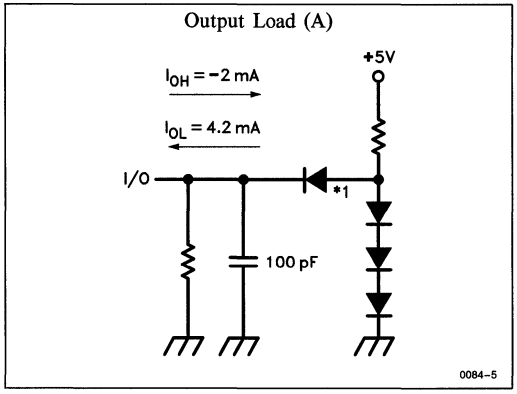
• **Capacitance** (T_A = 25°C, V_{CC} = 5V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, Address = V_{SS})

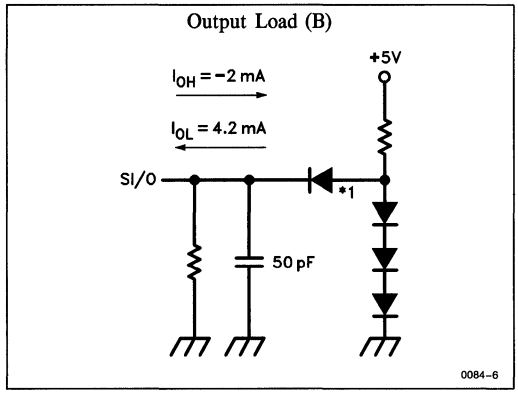
Parameter	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clocks	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 11]

Test Conditions

Input Rise and Fall Time	5 ns
Output Load	See Figures
Input Timing Reference Levels	0.8V, 2.4V
Output Timing Reference Levels	0.4V, 2.4V





Note: 1. Including Scope & Jig.

Common Parameters

Parameter	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	190	—	190	—	220	—	260	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	80	—	80	—	90	—	100	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	30	10000	30	10000	35	10000	40	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	15	—	20	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	70	25	70	25	85	30	110	ns	5, 6
$\overline{RAS}$ Hold Time	t_{RSH}	30	—	30	—	35	—	40	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise to Fall)	t_T	3	50	3	50	3	50	3	50	ns	8
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	ms	

Common Parameters (continued)

Parameter	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	—	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	—	15	—	15	—	20	—	ns	
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	0	—	0	—	ns	
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	0	—	0	—	ns	

Read Cycle (RAM), Page Mode Read Cycle

Parameter	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	3, 5
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	45	—	55	—	70	ns	3, 6
Output Buffer Turn-off Delay Referenced to $\overline{CAS}$	t_{OFF1}	—	25	—	25	—	30	—	40	ns	7
Output Buffer Turn-off Delay Referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	7
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	0	—	ns	12
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20	55	20	55	20	65	25	80	ns	5, 6
Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	20	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	—	75	ns	
$\overline{RAS}$ Pulse Width in Page Mode	t_{RASP}	0.1	100	0.1	100	0.12	100	0.15	100	μs	

Write Cycle (RAM), Page Mode Write Cycle

Parameter	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	9
Write Command Hold Time	t_{WCH}	25	—	25	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	25	—	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	
Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	20	—	ns	
$\overline{RAS}$ Pulse Width in Page Mode	t_{RASP}	0.1	100	0.1	100	0.12	100	0.15	100	μs	

Read-Modify-Write Cycle

Parameter	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	255	—	255	—	295	—	350	—	ns	
$\overline{RAS}$ Pulse Width	t_{RWS}	165	10000	165	10000	195	10000	240	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	65	—	65	—	75	—	90	—	ns	9
Column Address to $\overline{WE}$ Delay	t_{AWD}	80	—	80	—	95	—	120	—	ns	9
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	25	—	25	—	30	—	40	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	3, 5
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	45	—	55	—	70	ns	3, 6
$\overline{RAS}$ to Column Address Delay	t_{RAD}	20	55	20	55	20	65	25	80	ns	5, 6

Read-Modify-Write Cycle (continued)

Parameter	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Output Buffer Turn-off Delay Referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	25	—	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	

Refresh Cycle

Parameter	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CHR}	20	—	20	—	25	—	30	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

Transfer Cycle

Parameter	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
$\overline{SE}$ to $\overline{RAS}$ Setup Time	t_{ES}	0	—	0	—	0	—	0	—	ns	
$\overline{SE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	—	15	—	15	—	20	—	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	—	30	—	30	—	35	—	ns	
$\overline{SC}$ to $\overline{RAS}$ Setup Time	t_{SRS}	30	—	40	—	40	—	45	—	ns	

Transfer Cycle (continued)

Parameter	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{DT}$ Hold Time from $\overline{RAS}$	t_{RDH}	80	—	90	—	90	—	110	—	ns	
$\overline{DT}$ Hold Time from $\overline{CAS}$	t_{CDH}	20	—	30	—	30	—	45	—	ns	
Last SC to DT Delay Time	t_{SDD}	5	—	5	—	5	—	10	—	ns	
First SC to DT Hold Time	t_{SDH}	20	—	25	—	25	—	30	—	ns	
DT to RAS Lead Time	t_{DTL}	50	—	50	—	50	—	50	—	ns	
DT Hold Time Referenced to $\overline{RAS}$ High	t_{DTHH}	20	—	25	—	25	—	30	—	ns	
DT Precharge Time	t_{DTP}	30	—	35	—	35	—	40	—	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	—	60	—	60	—	75	—	ns	
Serial Data Input to $\overline{RAS}$ Delay Time	t_{SZR}	—	10	—	10	—	10	—	10	ns	
Serial Output Buffer Turn-off Delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	60	10	75	ns	7
$\overline{RAS}$ to S_{out} (Low-Z) Delay Time	t_{RLZ}	5	—	10	—	10	—	10	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Serial Clock Cycle Time	t_{SCC2}	40	—	40	—	40	—	60	—	ns	13
Access Time from SC	t_{SCA}	—	30	—	35	—	40	—	50	ns	4
Serial Data-out Hold Time	t_{SOH}	7	—	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	20	—	25	—	ns	

Serial Read Cycle

Parameter	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Access Time from SC	t_{SCA}	—	30	—	35	—	40	—	50	ns	4
Access Time from $\overline{SE}$	t_{SEA}	—	25	—	30	—	30	—	40	ns	4
Serial Data-out Hold Time	t_{SOH}	7	—	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{SE}$	t_{SEZ}	—	25	—	25	—	25	—	30	ns	7

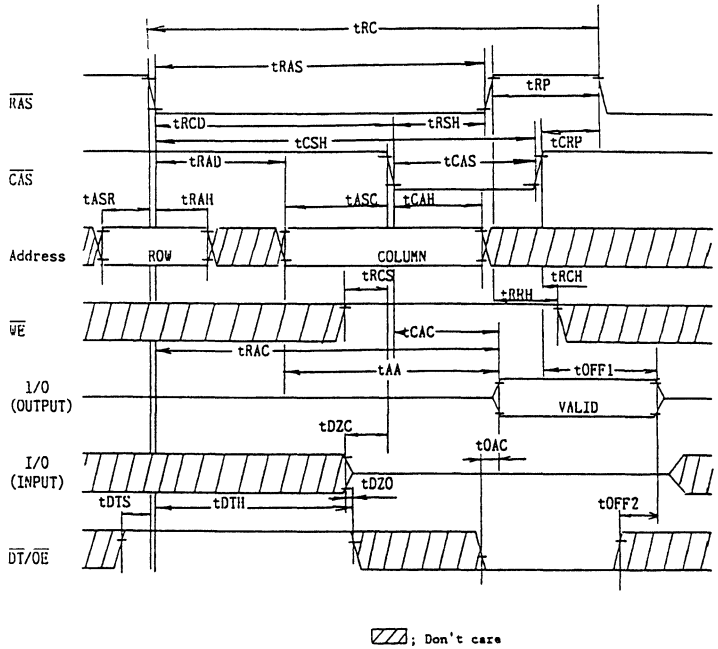
Serial Write Cycle

Parameter	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	20	—	25	—	ns	
Serial Write Enable Setup Time	t_{SWS}	0	—	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	t_{SWH}	30	—	35	—	35	—	50	—	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	—	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	30	—	35	—	35	—	50	—	ns	

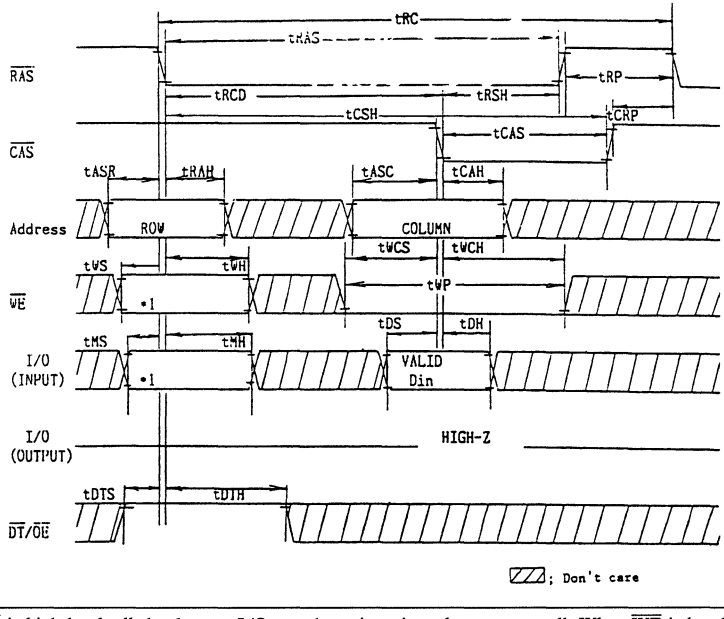
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
5. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
6. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
7. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition ($V_{OH} - 200$ mV, $V_{OL} + 200$ mV).
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
9. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-modify-write cycle; the data of the selected address is read out from a data output pin and input data is written into the selected address. In this case, impedance on I/O pins is controlled by $\overline{OE}$.
10. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles or to $\overline{WE}$ falling edge in delayed write or a read-modify-write cycles.
11. After power-up, pause for 100 μs or more and execute at least 8 initialization cycles (normal memory cycles or refresh cycles), then start operation.
12. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.
13. t_{CC2} is defined as the last SAM cycle time before read transfer in read transfer cycle (1).

■ TIMING WAVEFORMS

• Read Cycle

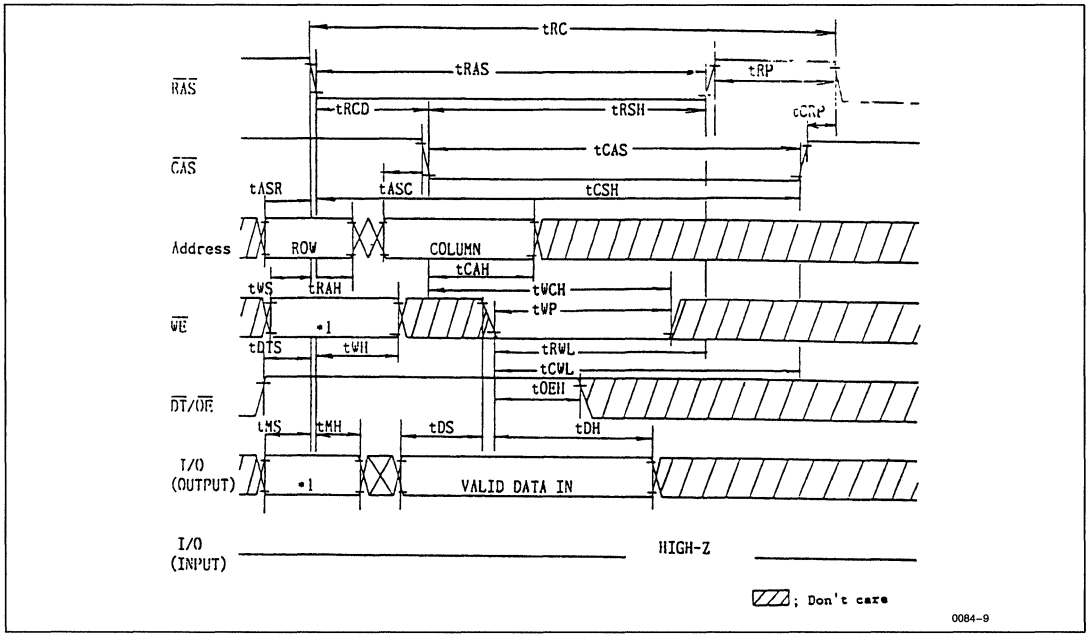


• Early Write Cycle



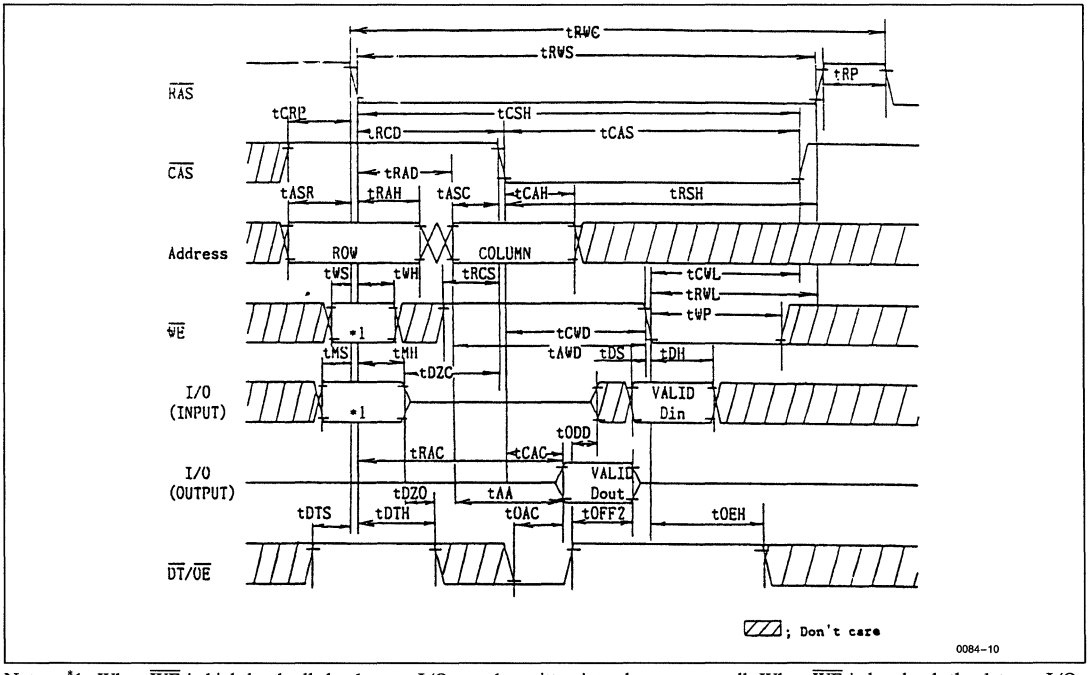
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Delayed Write Cycle**



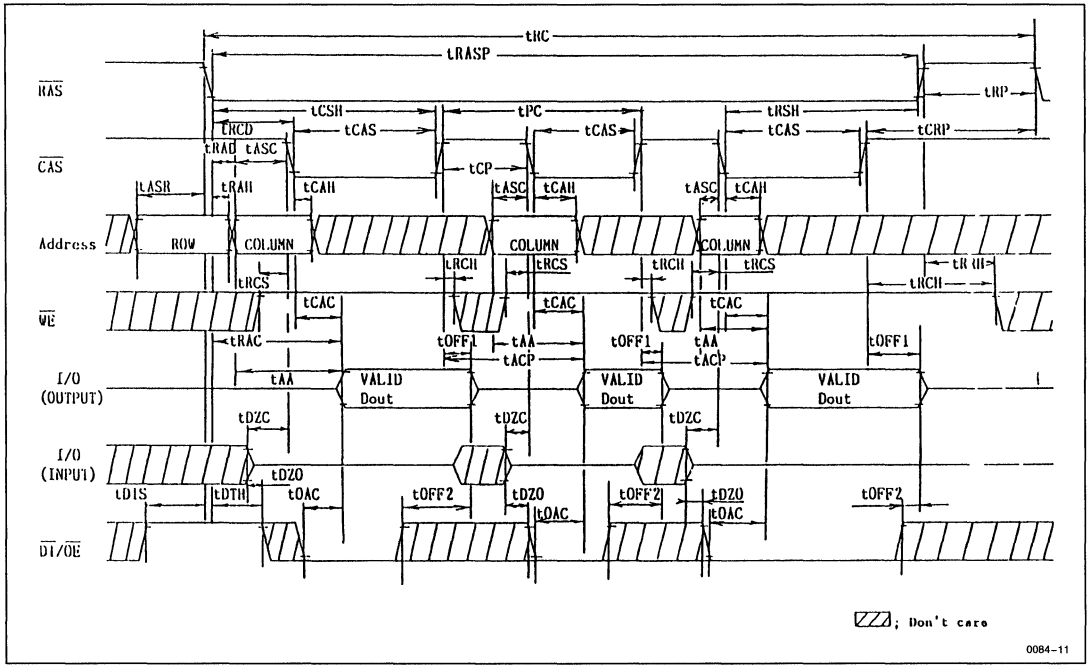
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Read-Modify-Write Cycle**

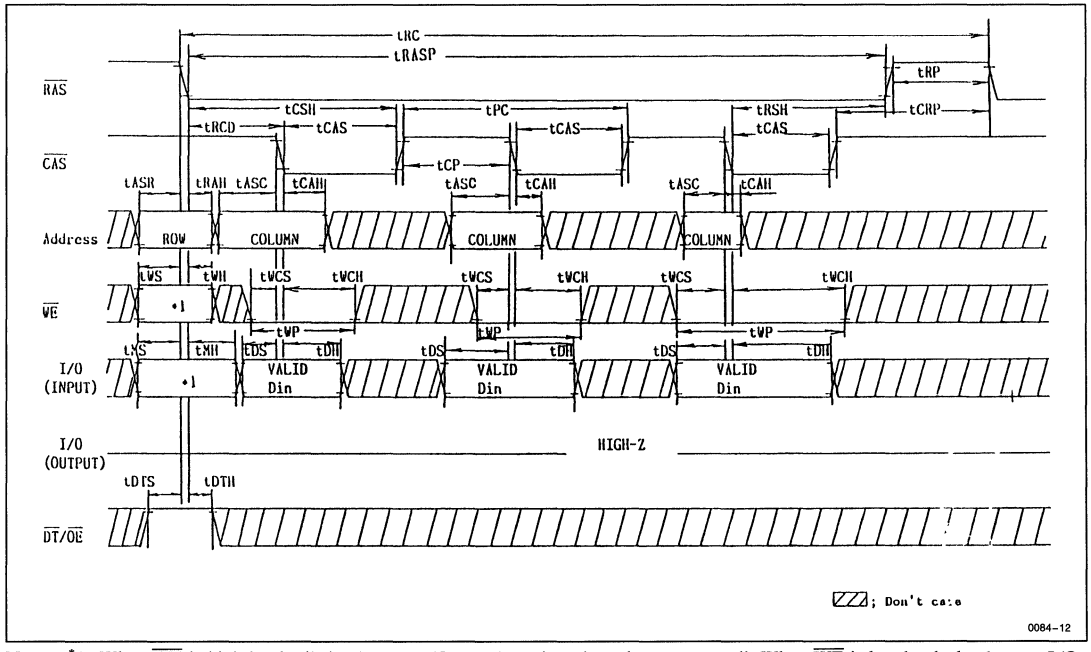


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Page Mode Read Cycle**

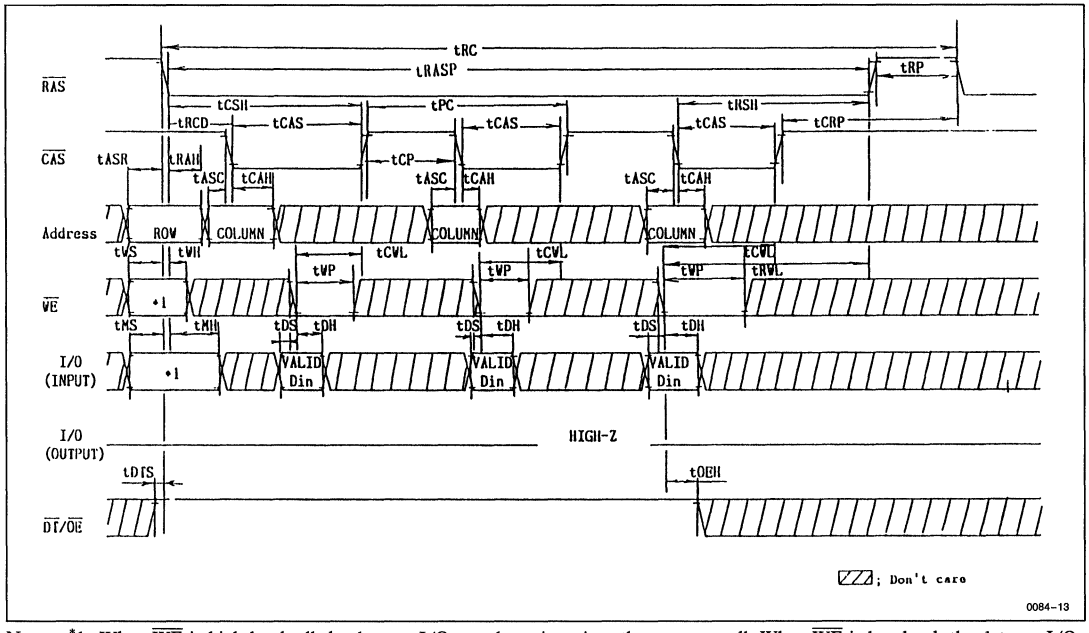


• **Page Mode Write Cycle (Early Write)**



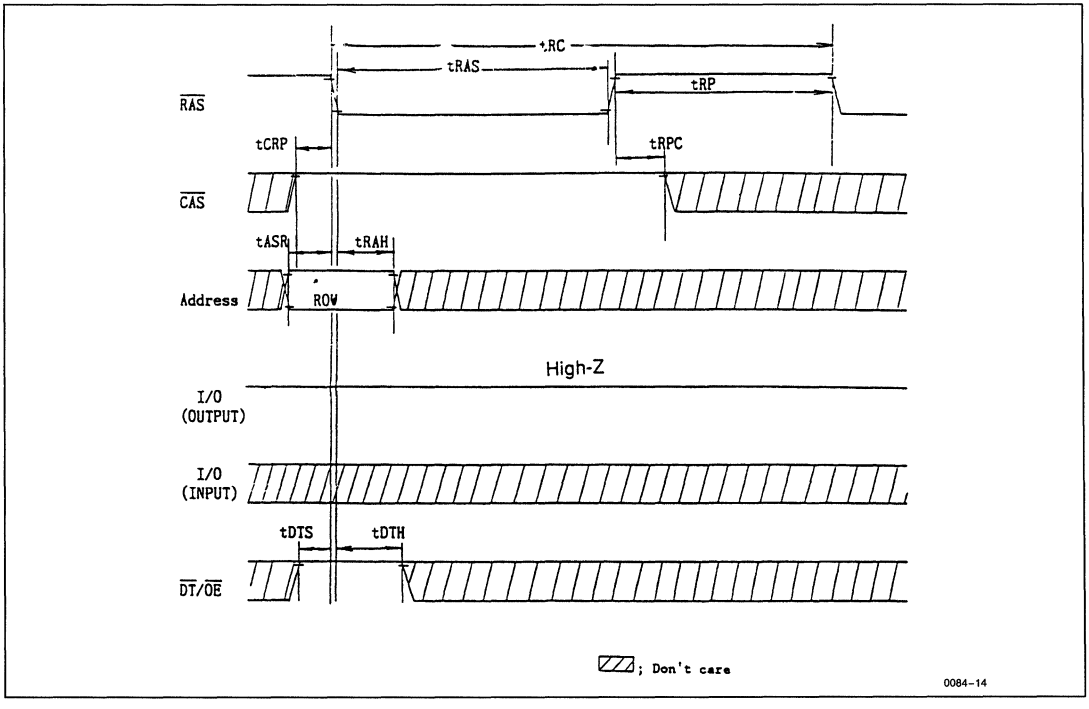
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Page Mode Write Cycle (Delayed Write)**

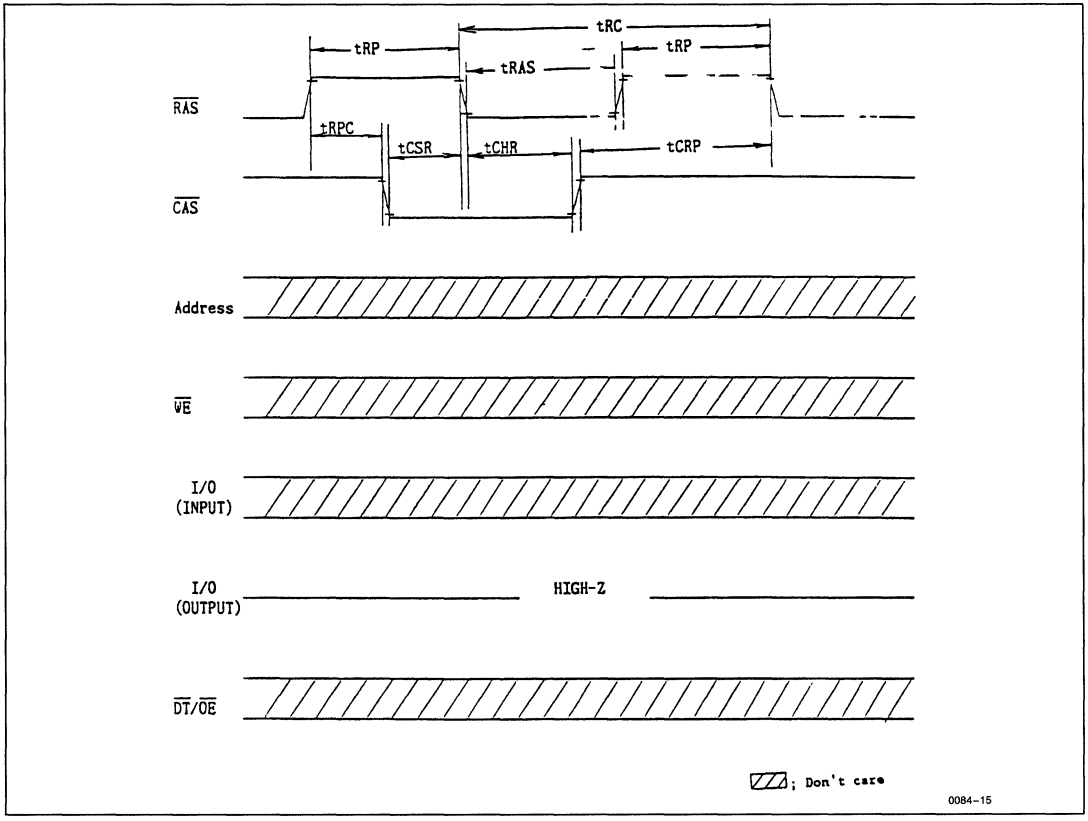


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

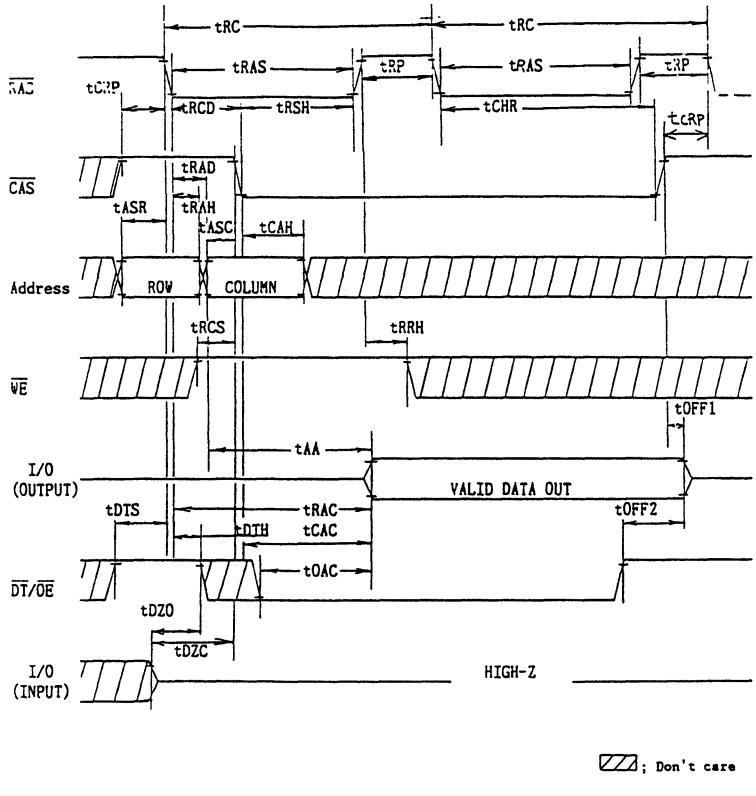
• **$\overline{RAS}$ Only Refresh Cycle**



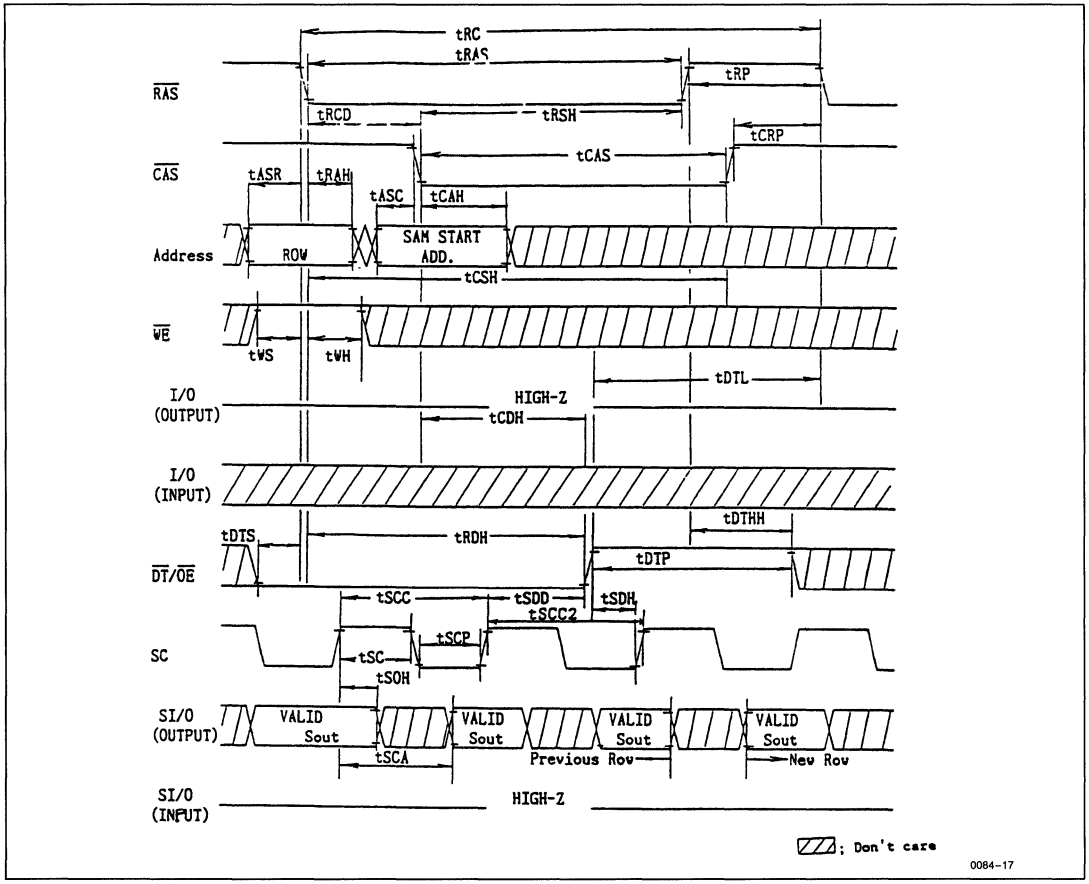
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• **Hidden Refresh Cycle**

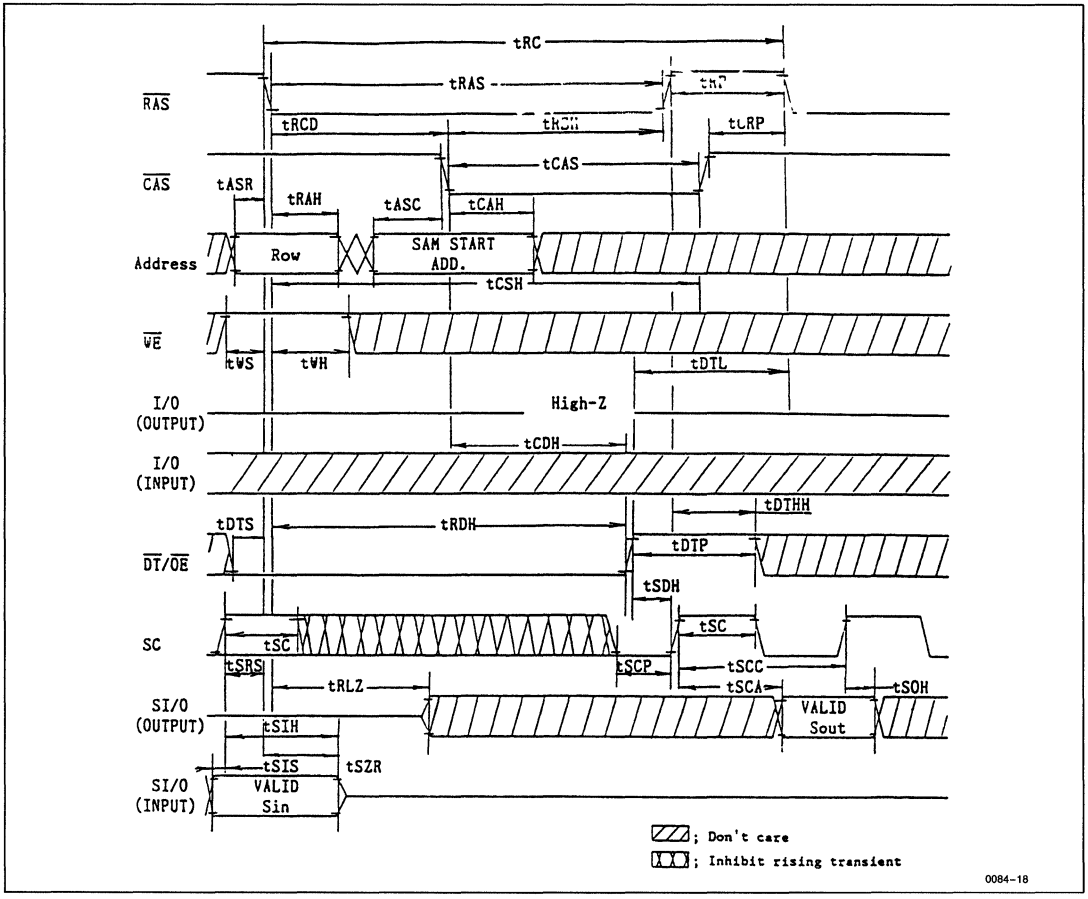


• **Read Transfer Cycle (1)**[1, 2]



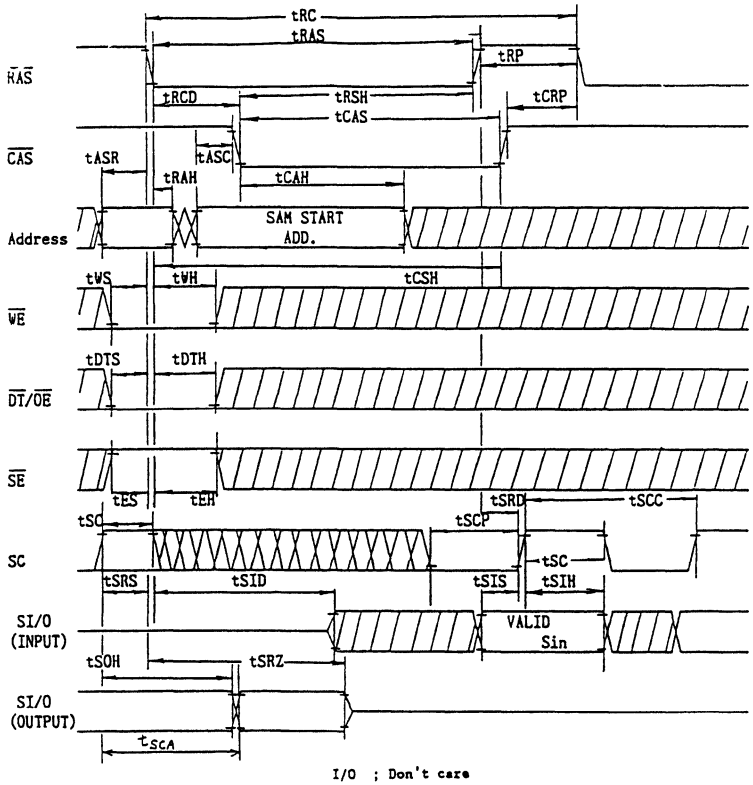
Notes: 1. When the previous data transfer cycle is a read transfer cycle, it is defined as read transfer cycle (1).
2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)

• **Read Transfer Cycle (2)**

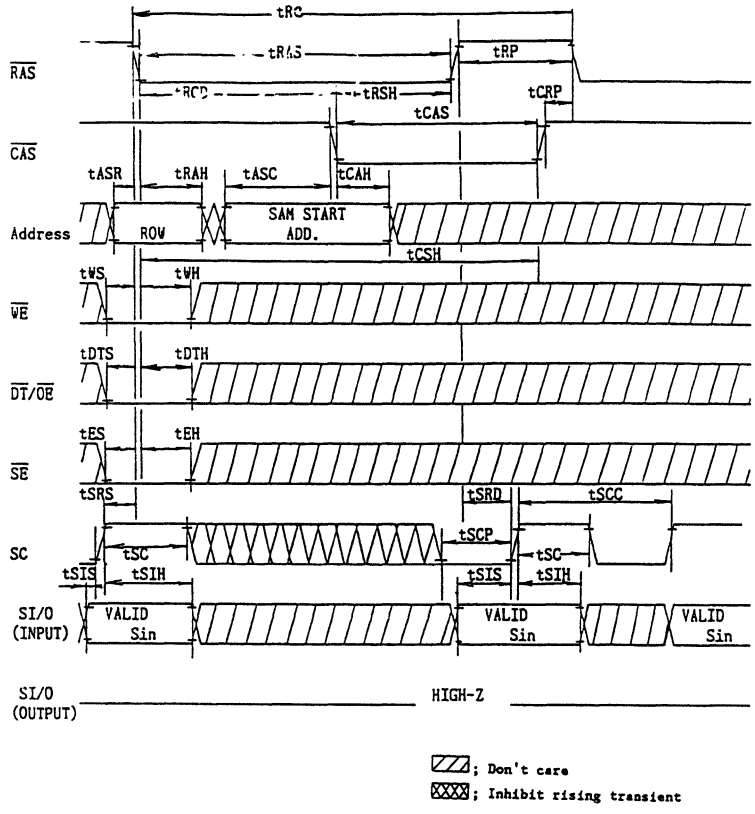


Notes: 1. When the previous data transfer cycle is a write or pseudo transfer cycle, it is defined as read transfer cycle (2).
2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)

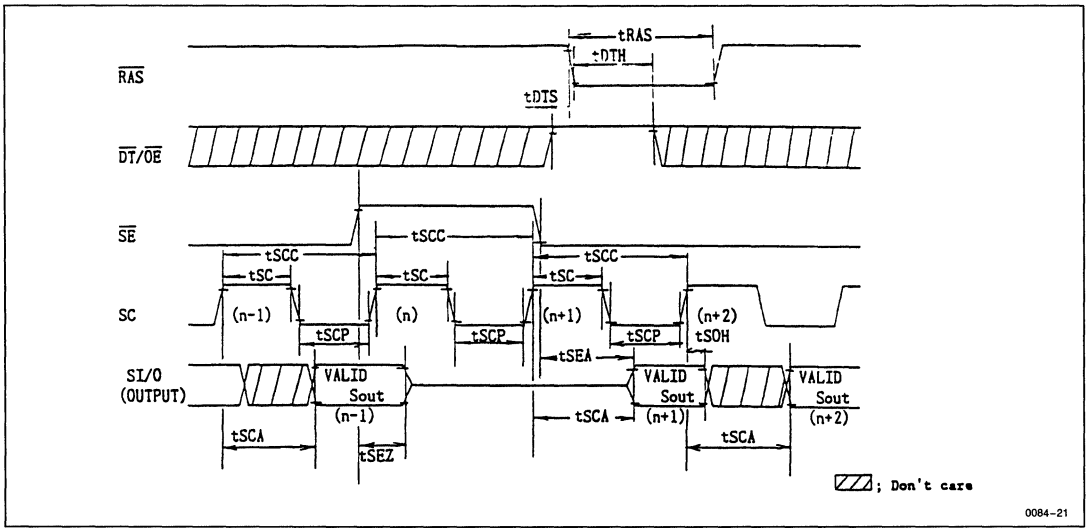
• **Pseudo Transfer Cycle**



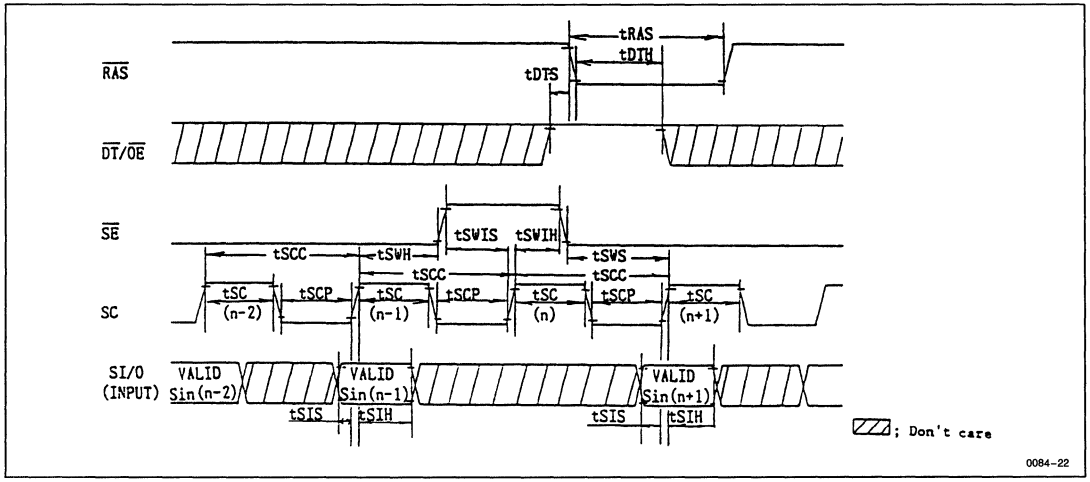
• **Write Transfer Cycle**



• **Serial Read Cycle**



• **Serial Write Cycle**



Notes: 1. When $\overline{SE}$ is high level in a serial write cycle, data is not written into SAM, however, the pointer is incremented.
2. Address 0 is accessed next to address 511.

HM534251A Series

262,144-Word x 4-Bit Multiport CMOS Video RAM

■ DESCRIPTION

The HM534251A is a 1-Mbit multiport video RAM equipped with a 256k-word x 4-bit dynamic RAM and a 512-word x 4-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has write mask function.

■ FEATURES

- Multiport Organization
  - Asynchronous and Simultaneous Operation of RAM and SAM Capability
  - RAM ..... 256k-word x 4-bit
  - SAM ..... 512-word x 4-bit
- Access Time
  - RAM ..... 80 ns/100 ns (max)
  - SAM ..... 25 ns/25 ns (max)
- Cycle Time
  - RAM ..... 150 ns/190 ns (min)
  - SAM ..... 30 ns/30 ns (min)
- Low Power
  - Active RAM ..... 360 mW (max)
  - SAM ..... 280 mW (max)
  - Standby ..... 38.5 mW (max)
- High-speed Page Mode Capability
- Mask Write Mode Capability
- Bidirectional Data Transfer Cycle Between RAM and SAM Capability
- Real Time Read Transfer Cycle Capability
- 3 Variations of Refresh ..... (8 ms/512 cycles)
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- TTL Compatible

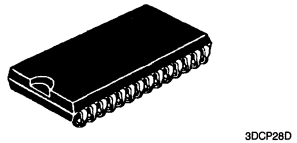
■ ORDERING INFORMATION

Part No.	Access Time	Package
HM534251AJ-8 HM534251AJ-10	80 ns 100 ns	400 mil 28-pin Plastic SOJ (CP-28D)
HM534251AZ-8 HM534251AZ-10	80 ns 100 ns	400 mil 28-pin Plastic ZIP (ZP-28)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Inputs
I/O_0–I/O_3	RAM Port Data Inputs/Outputs
SI/O_0–SI/O_3	SAM Port Data Inputs/Outputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{DT/OE}$	Data Transfer/Output Enable
SC	Serial Clock
$\overline{SE}$	SAM Port Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

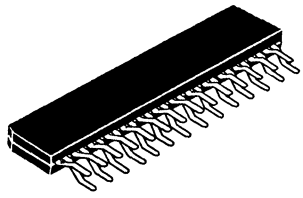
HM534251AJ Series



3DCP28D

(CP-28D)

HM534251AZ Series

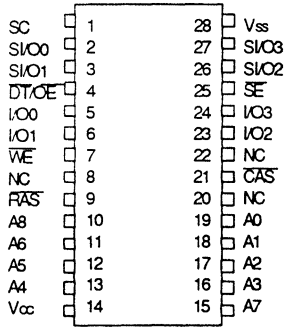


3DZP28

(ZP-28)

■ PIN OUT

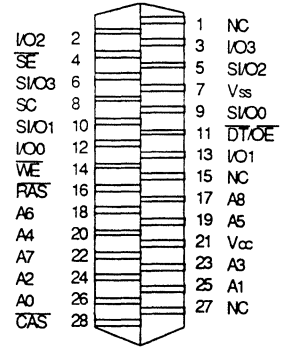
HM534251AJ Series



0083-1

(Top View)

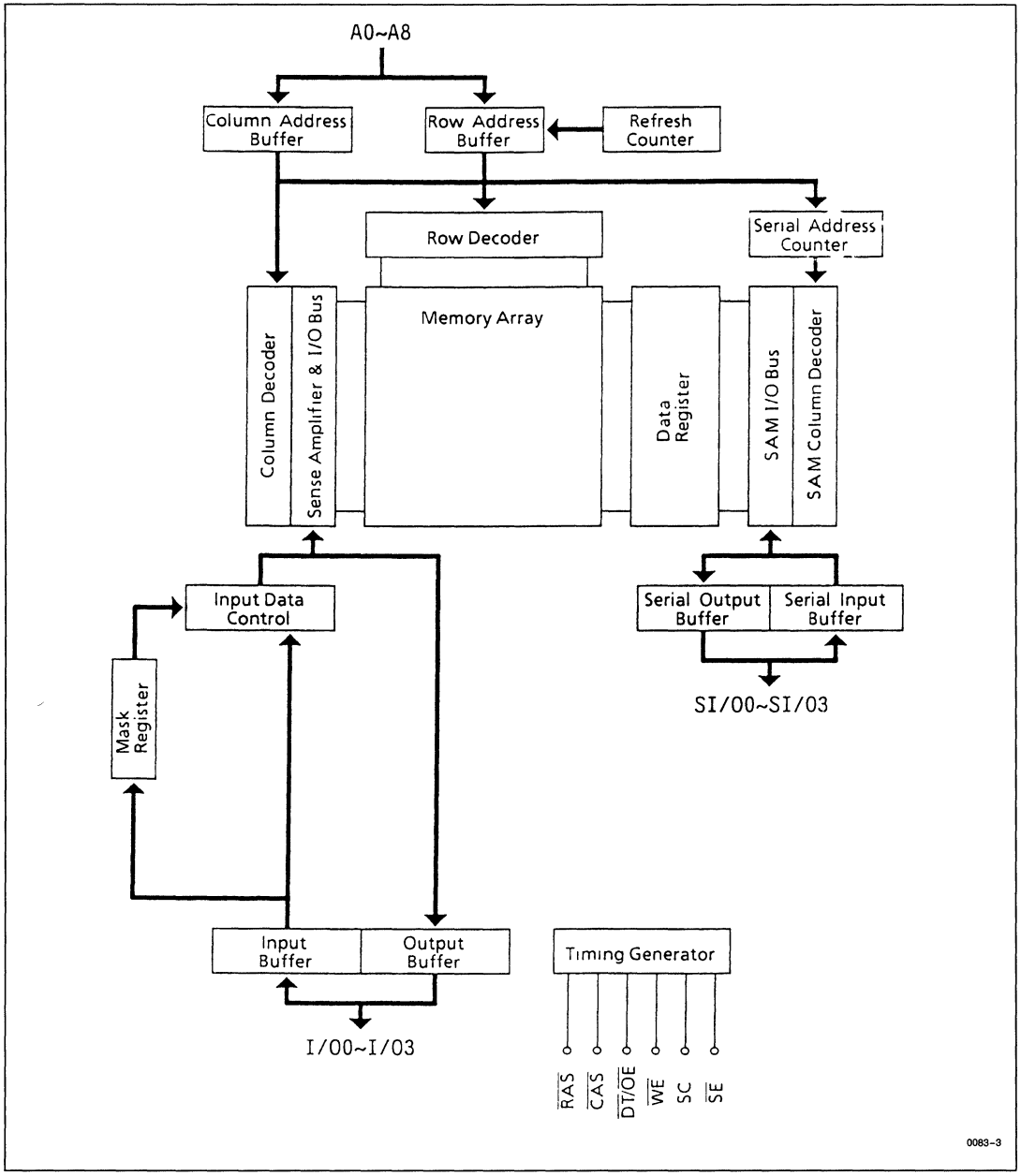
HM534251AZ Series



0083-2

(Bottom View)

■ BLOCK DIAGRAM



■ PIN FUNCTIONS

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of these signals determine the operation cycle of the HM534251A.

• Table 1. Operation Cycles of HM534251A

Input Level at the Falling Edge of $\overline{RAS}$				Operation Mode
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SE}$	
L	X	X	X	CBR Refresh
H	L	L	L	Write Transfer
H	L	L	H	Pseudo Transfer
H	L	H	X	Read Transfer
H	H	L	X	Read/Mask Write
H	H	H	X	Read/Write

$\overline{CAS}$ (input pin): Column address is fetched into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A_0–A_8 (input pins): Row address is determined by A_0–A_8 level at the falling edge of $\overline{RAS}$. Column address is determined by A_0–A_8 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM534251A turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O_0–I/O_3 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only to high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is fetched into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not fetched into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O_0–SI/O_3 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

■ OPERATION OF HM534251A

RAM Read Cycle ($\overline{DT}/\overline{OE}$ high and $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write) ($\overline{DT}/\overline{OE}$ high and $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after driving $\overline{RAS}$ low, a write cycle is executed and I/O data is written in the selected addresses. When all 4 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes in high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables read/write at the same address in one cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is retained. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is retained during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high and $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and the access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 μs).

• Transfer Operation

The HM534251A provides the read transfer cycle, pseudo transfer cycle and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{CAS}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)

Read transfer cycle: RAM to SAM
Write transfer cycle: SAM to RAM

(2) Determine SI/O state

Read transfer cycle: SI/O output
Pseudo transfer cycle and write transfer cycle: SI/O input

(3) Determine first SAM address to access after transferring at column address (SAM start address).

SAM start address must be determined by read transfer cycle or pseudo transfer cycle after power on, and determined for each transfer cycle.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address data (512 x 4-bit) determined by this cycle is transferred to SAM data register synchronously at the rising edge of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address determined by column address. In read transfer cycle, $\overline{DT}/\overline{OE}$ must be risen to transfer data from RAM to SAM.

This cycle can access SAM even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge and t_{SDH} (min) specified between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge must be satisfied. (See figure 1.)

When read transfer cycle is executed, SI/O becomes output state by first SAM acess. Input must be set high impedance before t_{SZS} (min) of the first SAM access to avoid data contention.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle switches SI/O to input state and set SAM start address without data transfer to RAM.

This cycle starts when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$. Data should be input to SI/O later than t_{SID} (min) after $\overline{RAS}$ becomes low to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC must not be risen.

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address for serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC must not be risen.

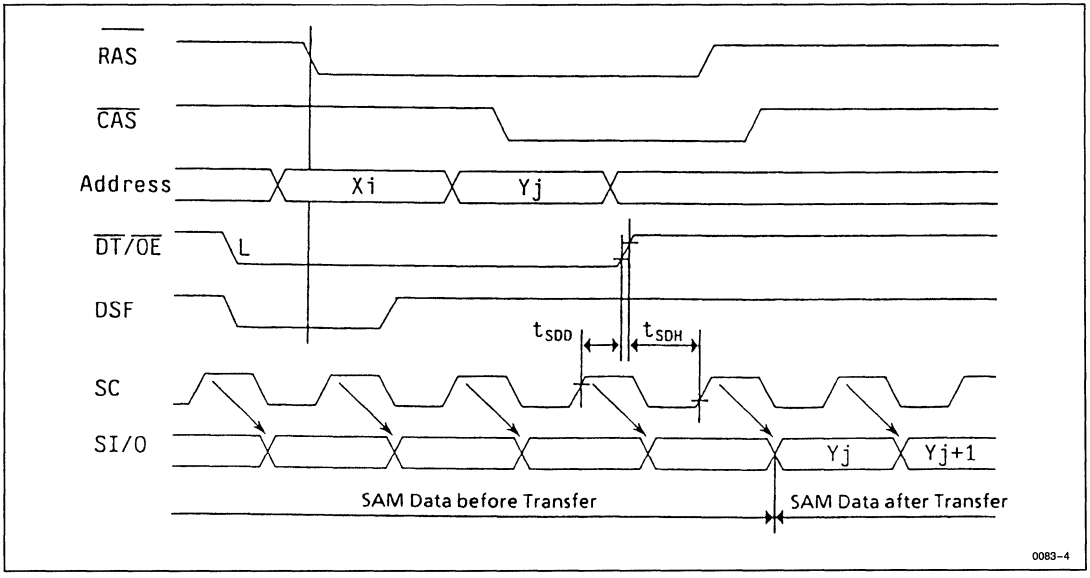


Figure 1. Real Time Read Transfer

Data transferred to SAM by read transfer cycle can be written to other address of RAM by write transfer cycle. However, the address to write data must be the same MSB of row address (AX8) as that of the read transfer cycle.

• SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When $\overline{SE}$ is set high, SI/O becomes high impedance, and the internal pointer is incremented by the SC rising. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is fetched into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't fetched into data register. Internal pointer is incremented by the SC rising, so $\overline{SE}$ high can be used as mask data for SAM. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

• Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is executed by accessing all 512 row addresses within 8 ms. There are three refresh cycles: (1) $\overline{RAS}$ only refresh cycle, (2) $\overline{CAS}$ before $\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required when all row addresses are accessed within 8 ms.

(1) $\overline{RAS}$ Only Refresh Cycle: $\overline{RAS}$ only refresh cycle is executed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high after inputting the row address (= refresh address) from external circuits. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ must be high at the falling edge of $\overline{RAS}$.

(2) CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.

(3) Hidden Refresh Cycle: Hidden refresh cycle executes CBR refresh with the data output by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register and selector), organized as fully static circuitry, require no refresh.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Terminal Voltage	V_T	−1.0 to +7.0	V	1
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V	1
Power Dissipation	P_T	1.0	W	
Operating Temperature	T_{opr}	0 to +70	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

Note: 1. Relative to V_{SS}.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−0.5	—	0.8	V	1, 2

Notes: 1. All voltages referenced to V_{SS}.
2. −3.0V for pulse width ≤ 10 ns.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM534251A-8		HM534251A-10		Unit	Test Conditions	
		Min	Max	Min	Max		RAM Port	SAM Port
Operating Current	I_{CC1}	—	65	—	50	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7}	—	115	—	100	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min
Standby Current	I_{CC2}	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC8}	—	50	—	50	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min

• **DC Electrical Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V) (continued)

Parameter	Symbol	HM534251A-8		HM534251A-10		Unit	Test Conditions	
		Min	Max	Min	Max		RAM Port	SAM Port
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	65	—	50	mA	$\overline{RAS}$ Cycling $\overline{CAS}$ = V_{IH} t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC9}	—	115	—	100	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min
Page Mode Current	I_{CC4}	—	70	—	65	mA	$\overline{CAS}$ Cycling $\overline{RAS}$ = V_{IL} t_{PC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10}	—	120	—	115	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC5}	—	55	—	40	mA	$\overline{RAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC11}	—	105	—	90	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min
Data Transfer Current	I_{CC6}	—	75	—	60	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC12}	—	125	—	110	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min
Input Leakage Current	I_{LI}	−10	10	−10	10	µA		
Output Leakage Current	I_{LO}	−10	10	−10	10	µA		
Output High Voltage	V_{OH}	2.4	—	2.4	—	V	I_{OH} = −2 mA	
Output Low Voltage	V_{OL}	—	0.4	—	0.4	V	I_{OL} = 4.2 mA	

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.

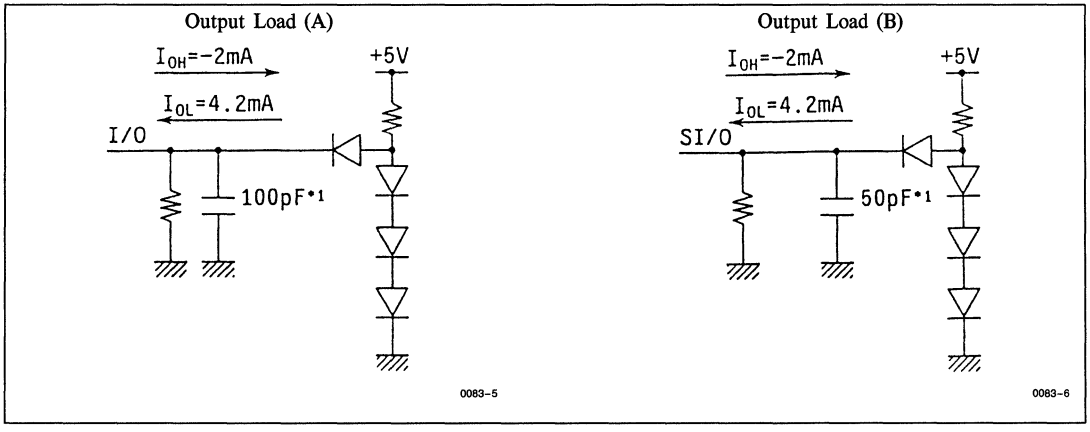
• **Capacitance** (T_A = 25°C, V_{CC} = 5V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O, QSF	$C_{I/O}$	—	—	7	pF

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 16]

Test Conditions

Input Rise and Fall Time:	5 ns
Output Load:	See Figures
Input Timing Reference Levels:	0.8V, 2.4V
Output Timing Reference Levels:	0.4V, 2.4V



Note: *1. Including scope & jig.

Common Parameter

Parameter	Symbol	HM534251A-8		HM534251A-10		Unit	Note
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	150	—	190	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	—	25	—	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	60	25	75	ns	2
$\overline{RAS}$ Hold Time Referenced to $\overline{CAS}$	t_{RSH}	20	—	25	—	ns	
$\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$	t_{CSH}	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	ns	
Transition Time (Rise to Fall)	t_T	3	50	3	50	ns	3
Refresh Period	t_{REF}	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	10	—	15	—	ns	
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	ns	4
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	ns	4
Output Buffer Turn-off Delay Referenced to $\overline{CAS}$	t_{OFF1}	—	20	—	25	ns	5
Output Buffer Turn-off Delay Referenced to $\overline{OE}$	t_{OFF2}	—	20	—	25	ns	5

Read Cycle (RAM), Page Mode Read Cycle

Parameter	Symbol	HM534251A-8		HM534251A-10		Unit	Note
		Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	25	ns	7, 8
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	25	ns	7
Address Access Time	t_{AA}	—	40	—	45	ns	7, 9
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	ns	10
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	ns	10
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	40	20	55	ns	2
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	ns	
Column Address to $\overline{CAS}$ Lead Time	t_{CAL}	40	—	45	—	ns	
Page Mode Cycle Time	t_{PC}	50	—	55	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	45	—	50	ns	
Page Mode $\overline{RAS}$ Pulse Width	t_{RASP}	80	100000	100	100000	ns	

Write Cycle (RAM), Page Mode Write Cycle

Parameter	Symbol	HM534251A-8		HM534251A-10		Unit	Note
		Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	ns	11
Write Command Hold Time	t_{WCH}	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	ns	12
Data-in Hold Time	t_{DH}	15	—	20	—	ns	12
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	10	—	15	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	10	—	15	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	20	—	25	—	ns	
Page Mode Cycle Time	t_{PC}	50	—	55	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
$\overline{CAS}$ to Data-in Delay Time	t_{CDD}	20	—	25	—	ns	13
Page Mode $\overline{RAS}$ Pulse Width	t_{RASP}	80	100000	100	100000	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM534251A-8		HM534251A-10		Unit	Note
		Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	200	—	250	—	ns	
$\overline{RAS}$ Pulse Width (Read-Modify-Write Cycle)	t_{RWS}	130	10000	160	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	45	—	55	—	ns	14
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	65	—	75	—	ns	14
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	20	—	25	—	ns	12
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	25	ns	7, 8
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	25	ns	7
Address Access Time	t_{AA}	—	40	—	45	ns	7, 9
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	40	20	55	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	ns	12
Data-in Hold Time	t_{DH}	15	—	20	—	ns	12
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM534251A-8		HM534251A-10		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CHR}	15	—	20	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	ns	

Read Transfer Cycle

Parameter	Symbol	HM534251A-8		HM534251A-10		Unit	Note
		Min	Max	Min	Max		
$\overline{DT}$ Hold Time Referenced to $\overline{RAS}$	t_{RDH}	70	10000	90	10000	ns	
$\overline{DT}$ Hold Time Referenced to $\overline{CAS}$	t_{CDH}	20	—	25	—	ns	
$\overline{DT}$ Hold Time Referenced to Column Address	t_{ADH}	30	—	35	—	ns	
$\overline{DT}$ Precharge Time	t_{DTP}	40	—	45	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Delay Time	t_{DRD}	70	—	90	—	ns	
SC to $\overline{RAS}$ Setup Time	t_{SRS}	30	—	30	—	ns	
1'st SC to $\overline{RAS}$ Hold Time	t_{SRH}	85	—	105	—	ns	
1'st SC to $\overline{CAS}$ Hold Time	t_{SCH}	30	—	35	—	ns	
1'st SC to Column Address Hold Time	t_{SAH}	50	—	55	—	ns	
Last SC to $\overline{DT}$ Delay Time	t_{SDD}	5	—	5	—	ns	
1'st SC to $\overline{DT}$ Hold Time	t_{SDH}	15	—	15	—	ns	
Serial Data-in to 1'st SC Delay Time	t_{SZS}	0	—	0	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	30	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	ns	
SC Precharge Time	t_{SCP}	10	—	10	—	ns	
SC Access Time	t_{SCA}	—	25	—	25	ns	15
Serial Data-out Hold Time	t_{SOH}	5	—	5	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	40	20	55	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	ns	
$\overline{DT}$ High Hold Time to $\overline{RAS}$ Precharge Time	t_{DTHH}	25	—	30	—	ns	

Pseudo Transfer Cycle, Write Transfer Cycle

Parameter	Symbol	HM534251A-8		HM534251A-10		Unit	Note
		Min	Max	Min	Max		
$\overline{SE}$ Setup Time Referenced to $\overline{RAS}$	t_{ES}	0	0	0	0	ns	
$\overline{SE}$ Hold Time Referenced to $\overline{RAS}$	t_{EH}	10	—	15	—	ns	
SC Setup Time Referenced to $\overline{RAS}$	t_{SRS}	30	—	30	—	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	—	25	—	ns	
Serial Output Buffer Turn-off Time Referenced to $\overline{RAS}$	t_{SRZ}	10	45	10	50	ns	
$\overline{RAS}$ to Serial Data-in Delay Time	t_{SID}	45	—	50	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	30	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	ns	
SC Precharge Time	t_{SCP}	10	—	10	—	ns	
SC Access Time	t_{SCA}	—	25	—	25	ns	15
$\overline{SE}$ Access Time	t_{SEA}	—	25	—	25	ns	15
Serial Data-out Hold Time	t_{SOH}	5	—	5	—	ns	
Serial Write Enable Setup Time	t_{SWS}	5	—	5	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	ns	

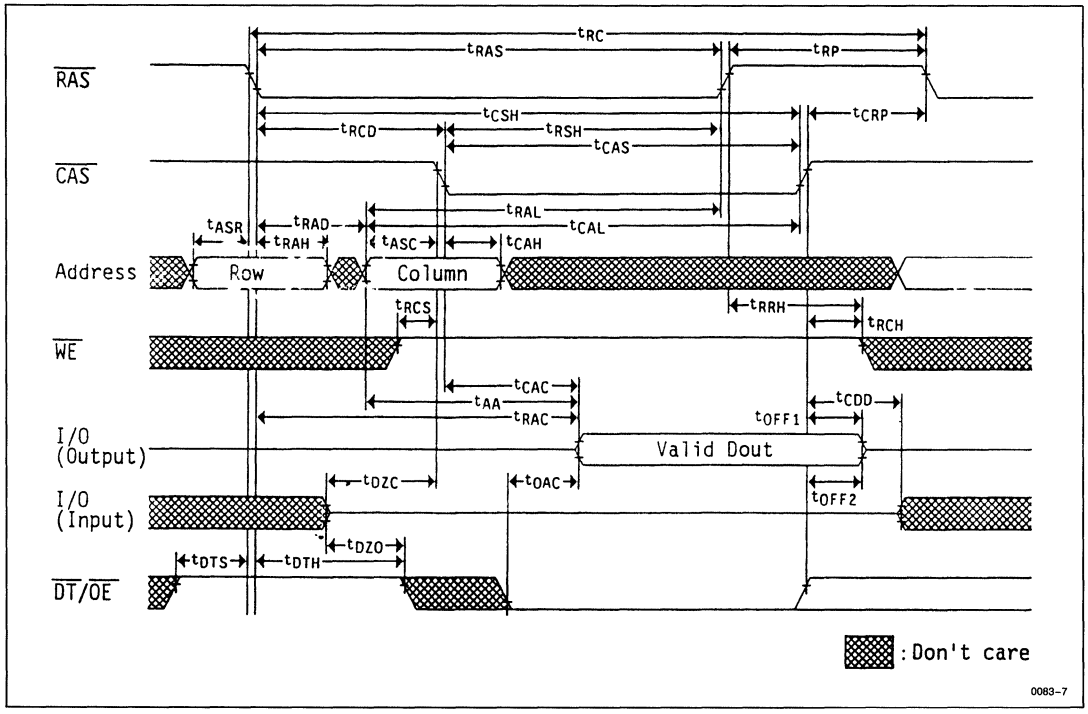
Serial Read Cycle, Serial Write Cycle

Parameter	Symbol	HM534251A-8		HM534251A-10		Unit	Note
		Min	Max	Min	Max		
Serial Clock Cycle Time	t_{SCC}	30	—	30	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	ns	
Access Time from SC	t_{SCA}	—	25	—	25	ns	15
Access Time from $\overline{SE}$	t_{SEA}	—	25	—	25	ns	15
Serial Data-out Hold Time	t_{SOH}	5	—	5	—	ns	
Serial Output Buffer Turn-off Time Referenced to $\overline{SE}$	t_{SEZ}	—	20	—	25	ns	5
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	ns	
Serial Write Enable Setup Time	t_{SWS}	5	—	5	—	ns	
Serial Write Enable Hold Time	t_{SWH}	15	—	20	—	ns	
Serial Write Disable Setup Time	t_{SWIS}	5	—	5	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	15	—	20	—	ns	

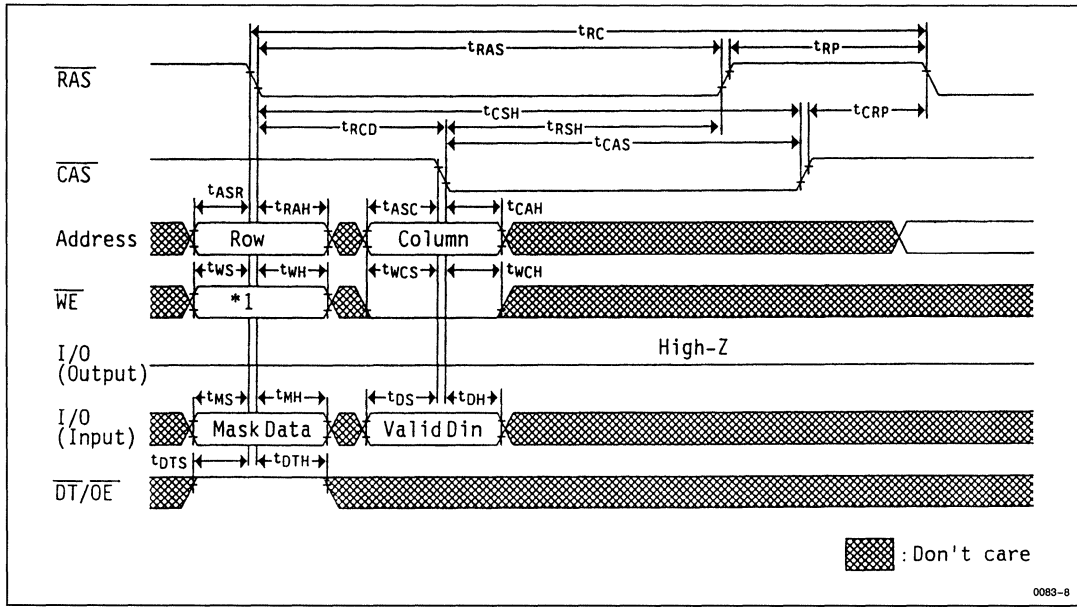
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. When $t_{RCD} > t_{RCD}$ (max) and $t_{RAD} > t_{RAD}$ (max), access time is specified by t_{CAC} or t_{AA}.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input singals. Transition time t_T is measured between V_{IH} and V_{IL}.
4. Data input must be floating before output buffer is turned on. In read cycle, read-modify-write cycle and delayed write cycle, either t_{DZC} (min) or t_{DZO} (min) must be satisfied.
5. t_{OFF1} (max), t_{OFF2} (max) and t_{SEZ} (max) are defined as the time at which the output achieves the open circuit condition (V_{OH} − 200 mV, V_{OL} + 200 mV).
6. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
8. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
9. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
10. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.
11. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
12. These parameters are specified by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
13. Either t_{CDD} (min) or t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{CAS}$ or $\overline{OE}$ prior to applying data to the device when output buffer is on.
14. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min) in read-modify-write cycle, the data of the selected address outputs to an I/O pin and input data is written into the selected address. t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{OE}$ prior to applying data to the device.
15. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
16. After power-up, pause for 100 μs or more and execute at least 8 initialization cycle (normal memory cycle or refresh cycle), then start operation.

■ TIMING WAVEFORMS

• Read Cycle

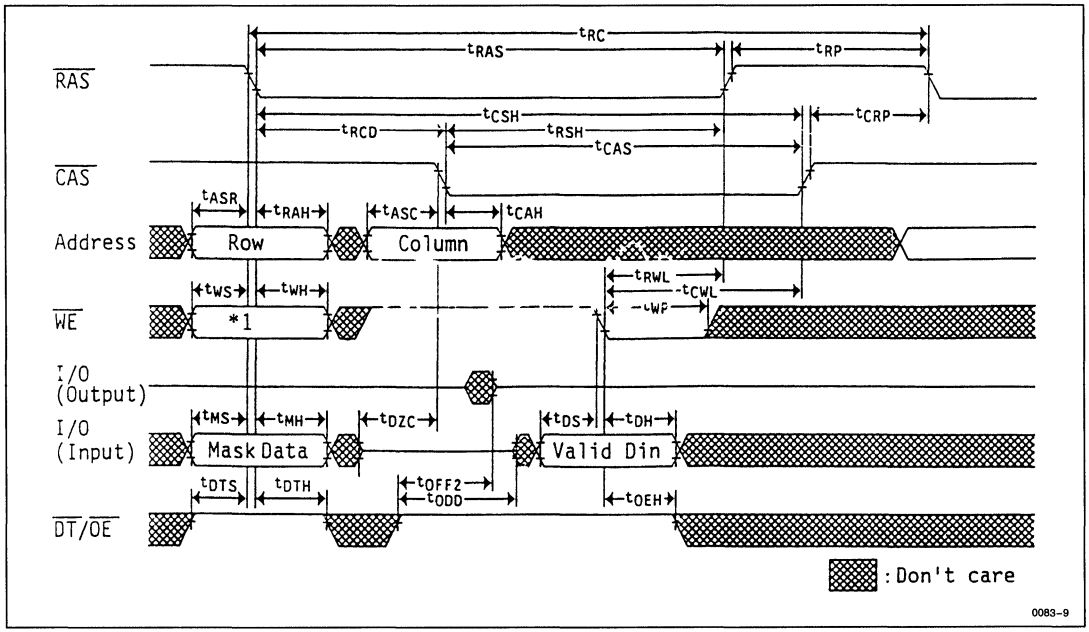


• Early Write Cycle



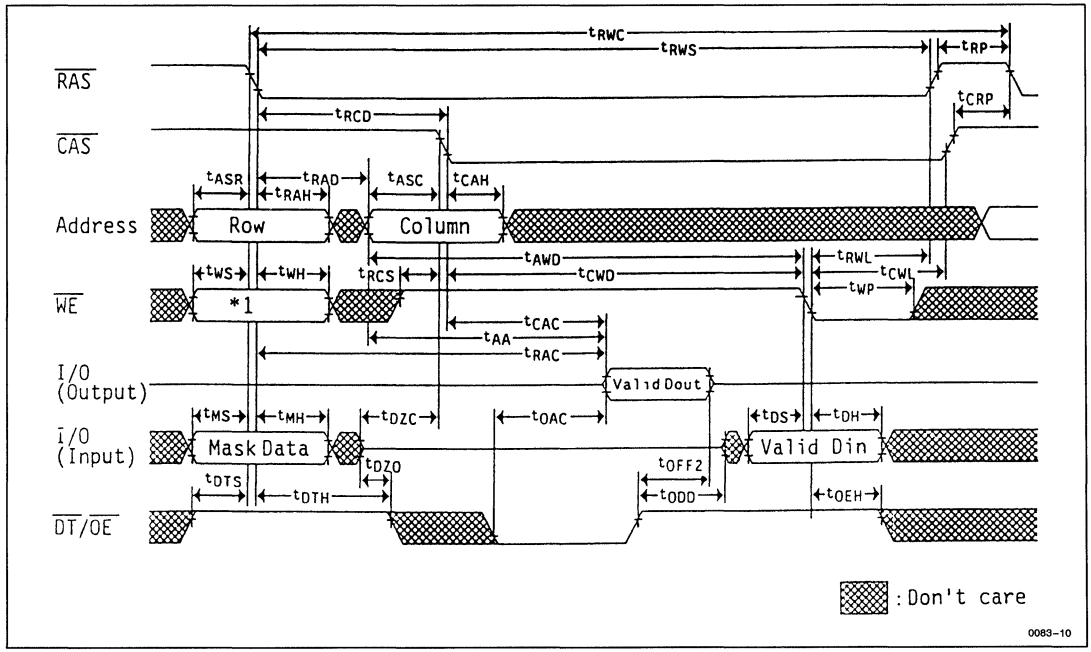
Note: *1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

• **Delayed Write Cycle**



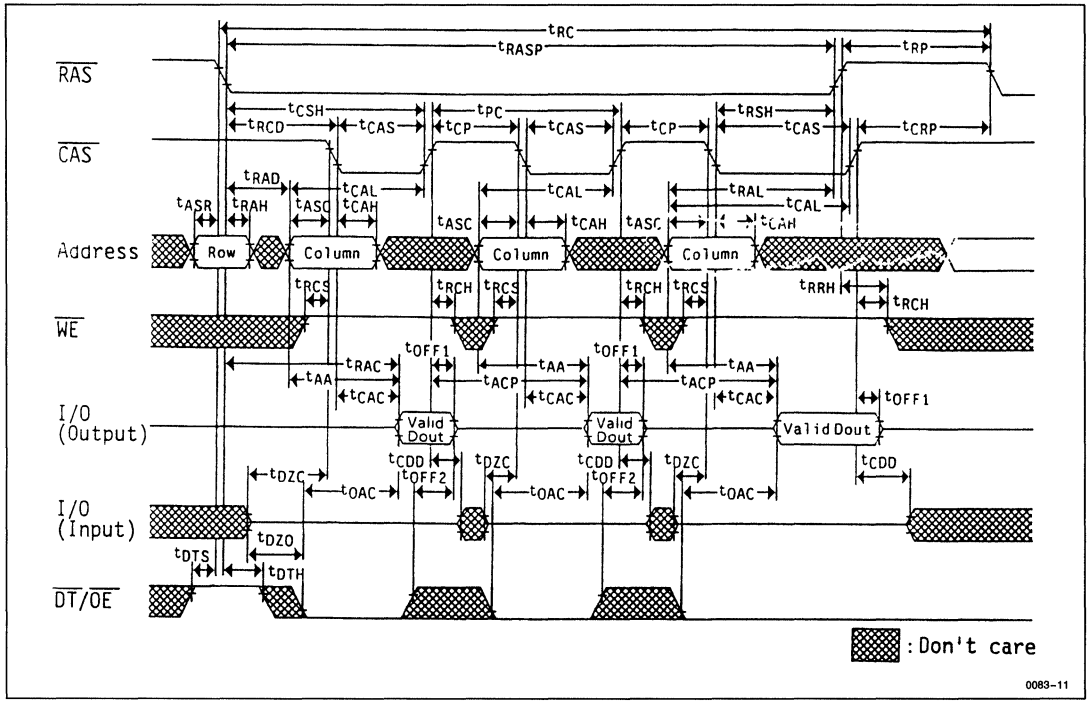
Note: *1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

• **Read-Modify-Write Cycle**

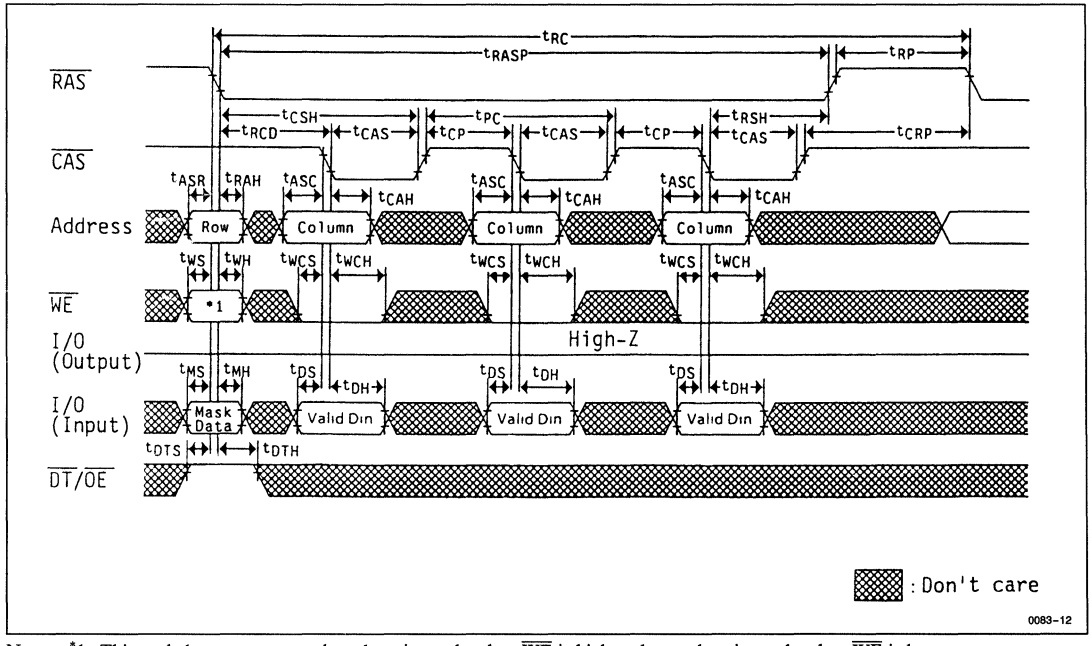


Note: *1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

• **Page Mode Read Cycle**

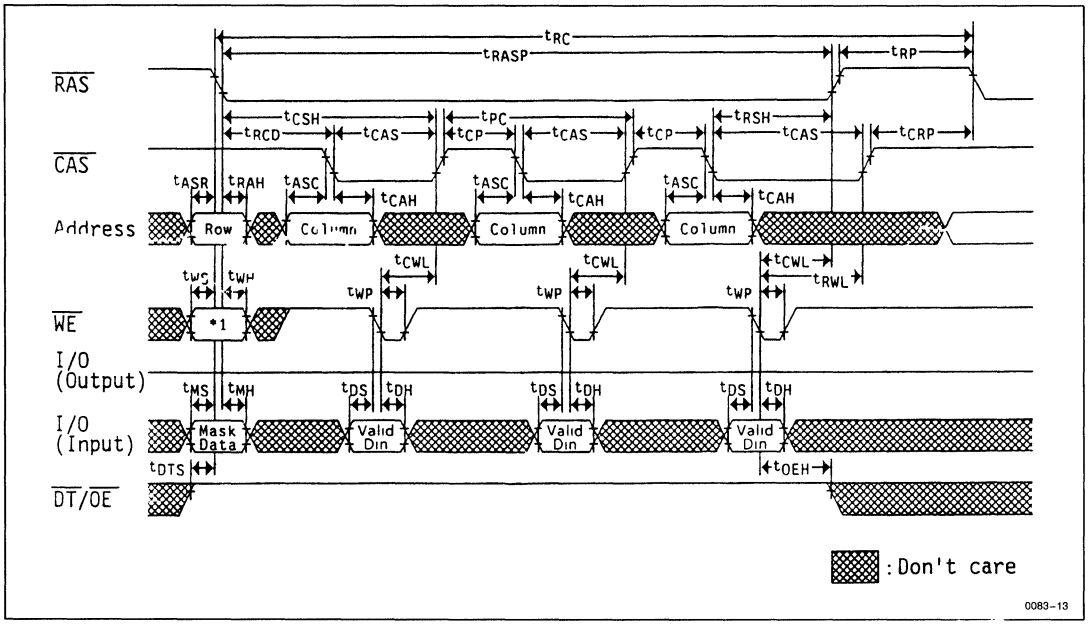


• **Page Mode Write Cycle (Early Write)**



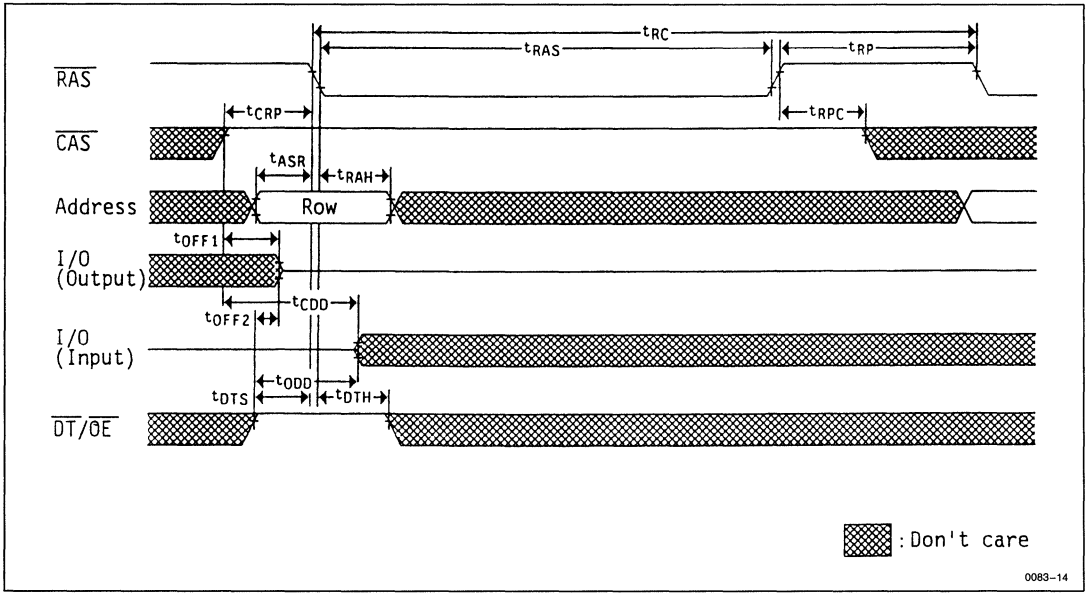
Note: *1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

• **Page Mode Write Cycle (Delayed Write)**

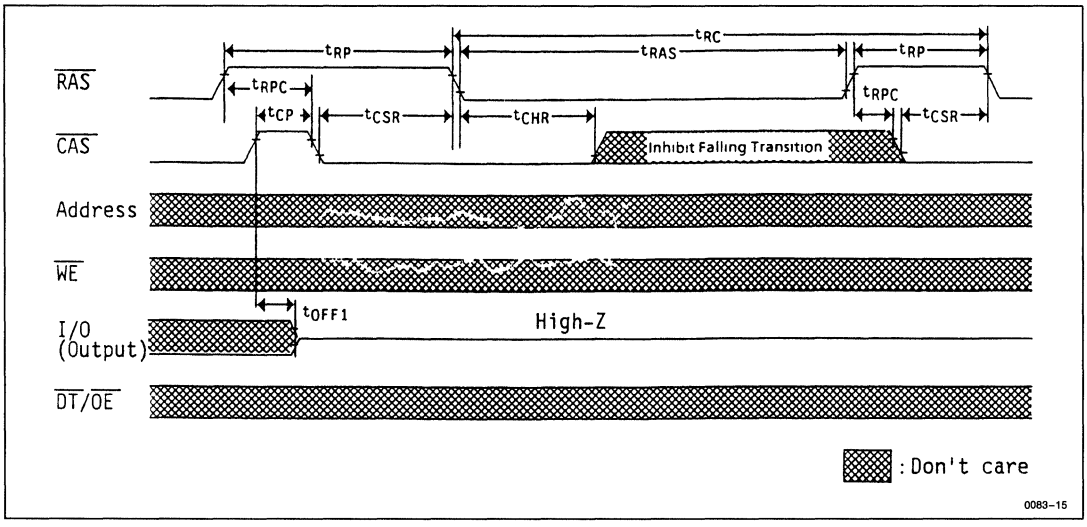


Note: *1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

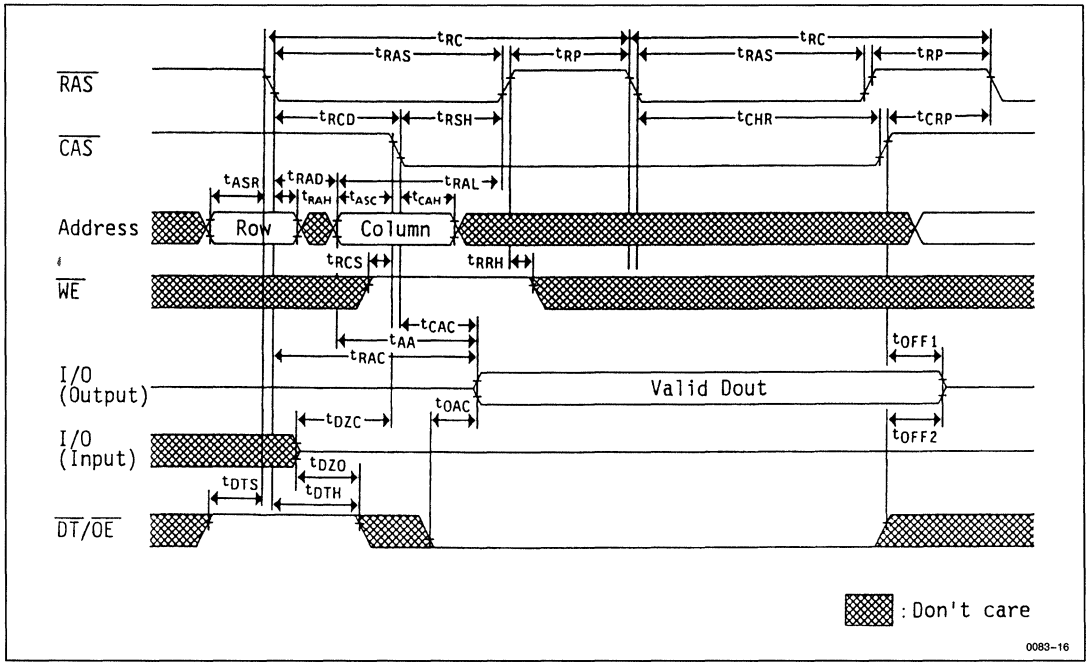
• **$\overline{RAS}$ Only Refresh Cycle**



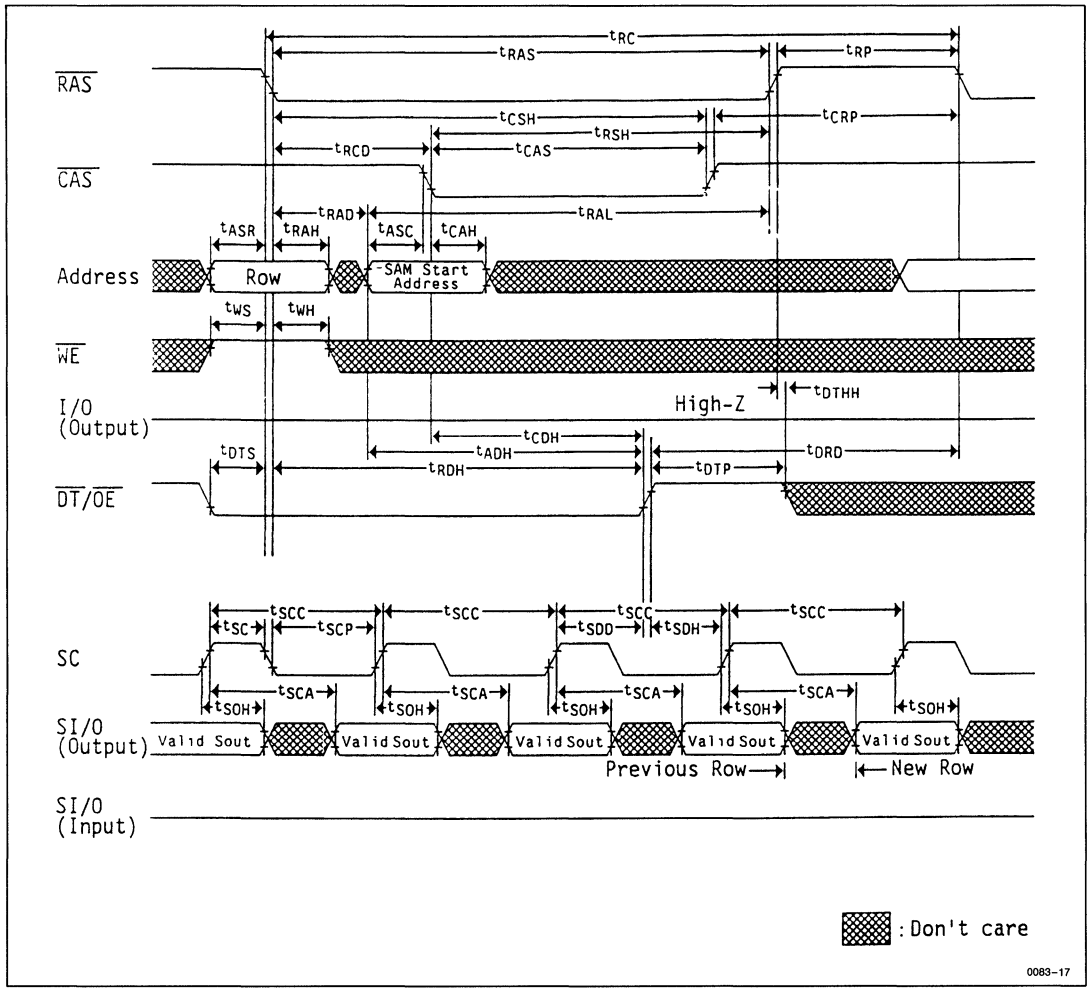
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



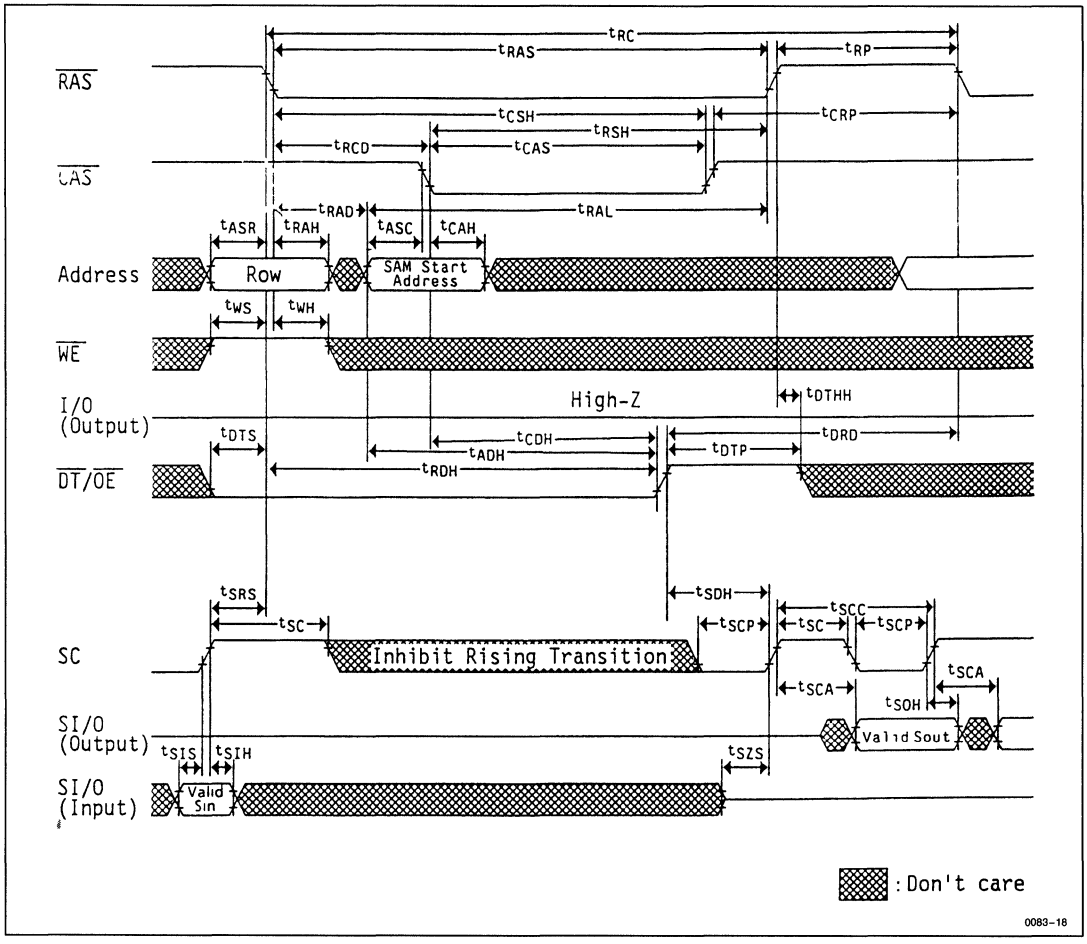
• Hidden Refresh Cycle



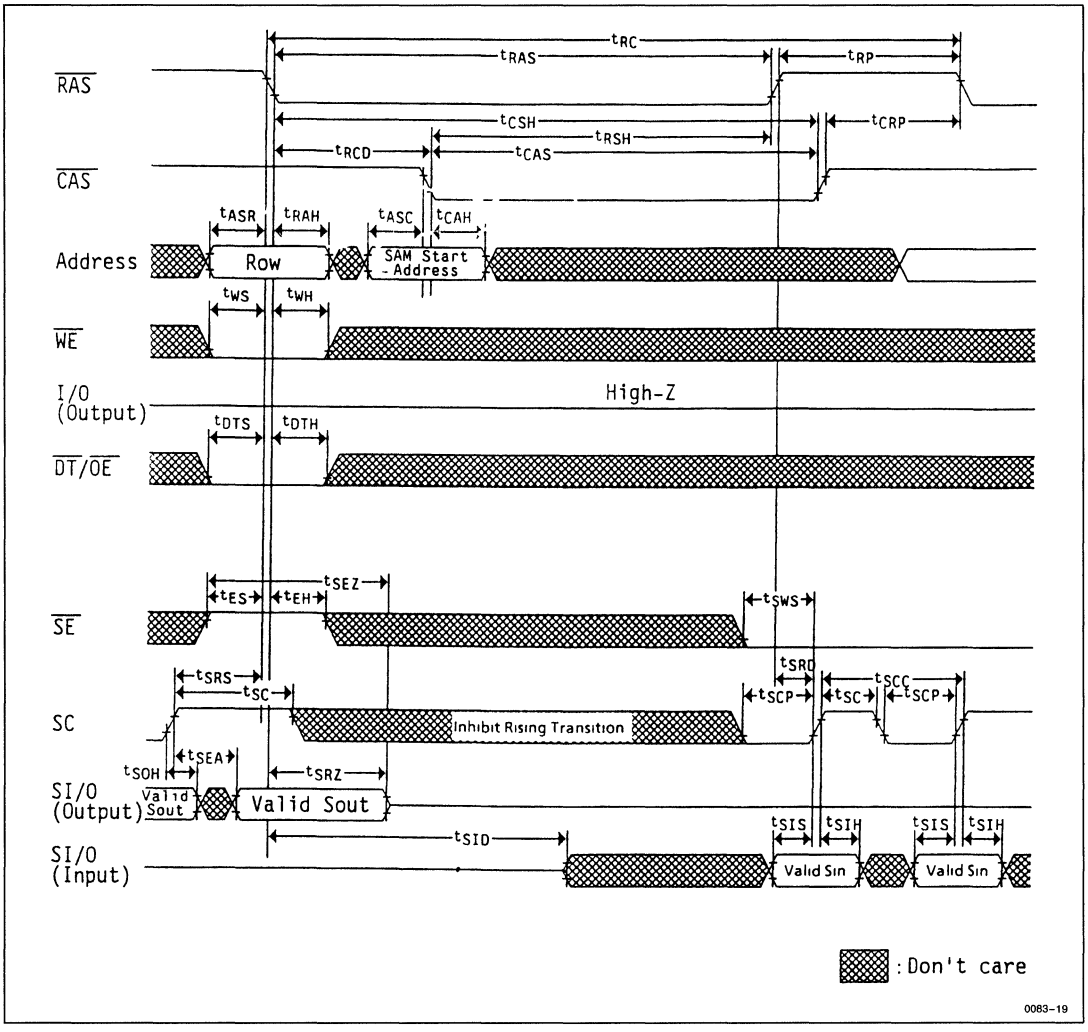
• **Read Transfer Cycle (1)**



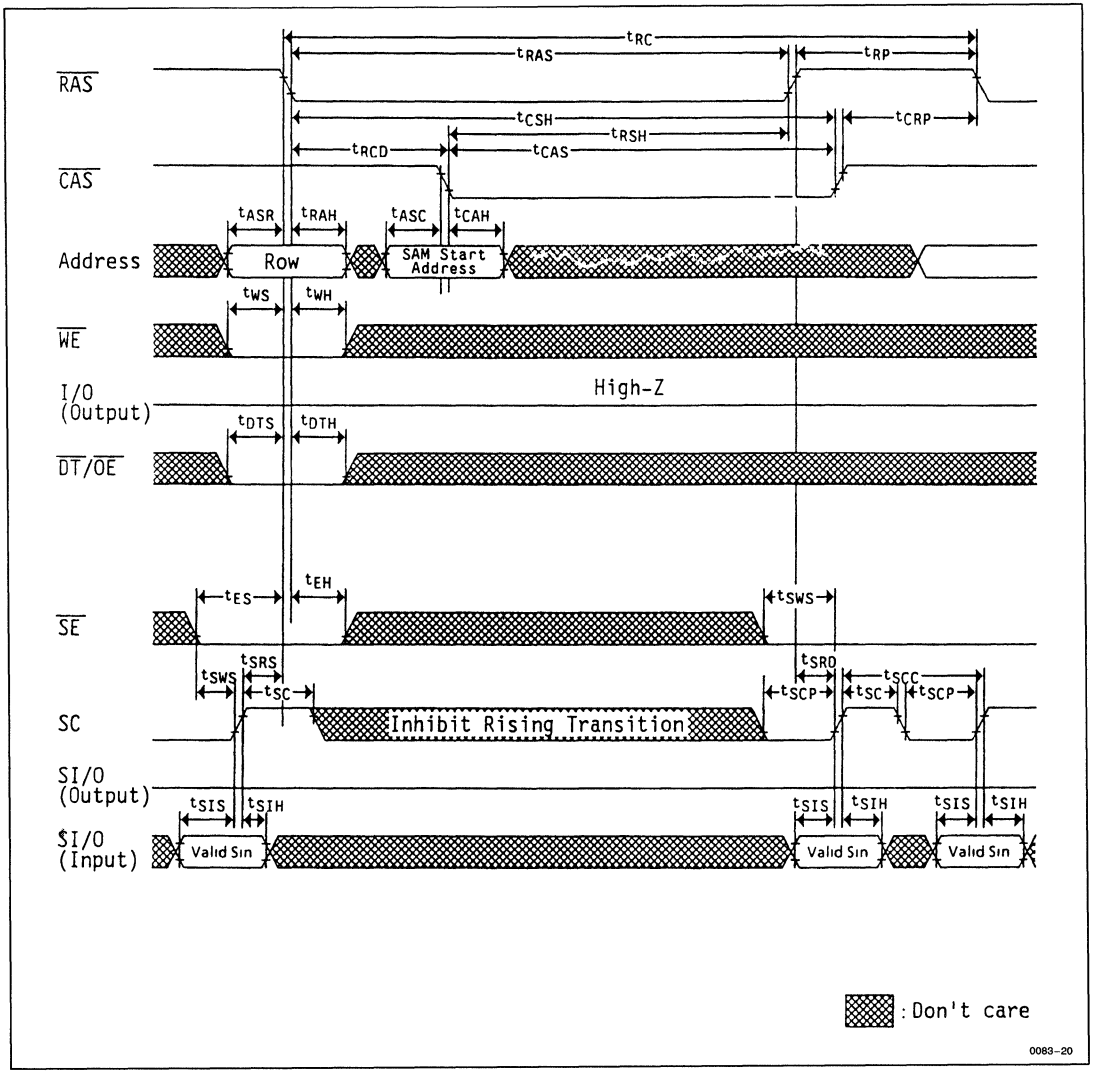
• **Read Transfer Cycle (2)**



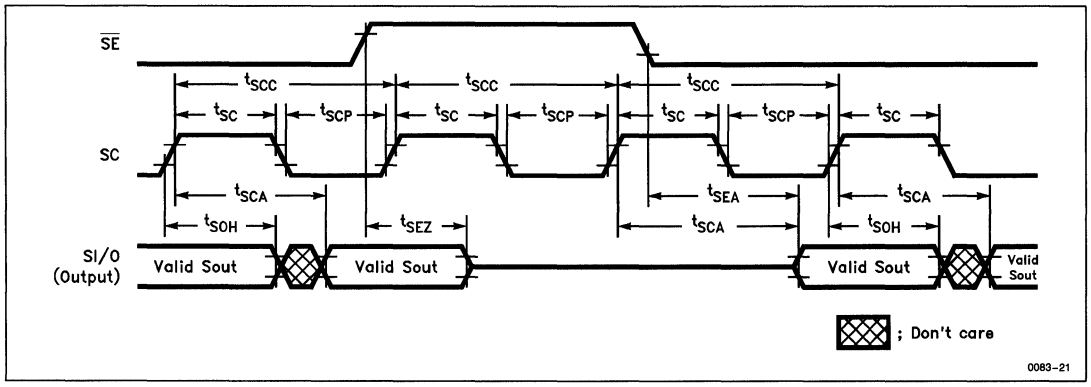
• **Pseudo Transfer Cycle**



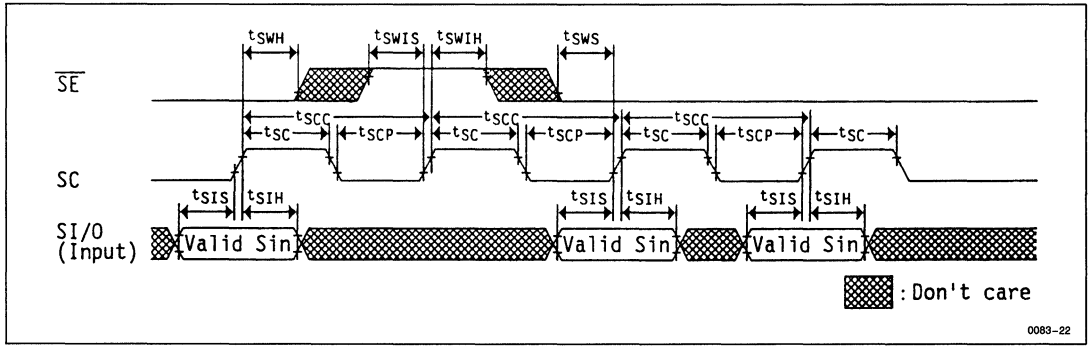
• **Write Transfer Cycle**



• **Serial Read Cycle**



• **Serial Write Cycle**



HM534252 Series

262,144-Word x 4-Bit Multiport CMOS Video RAM

■ DESCRIPTION

The HM534252 is a 1-Mbit multiport video RAM equipped with a 256k-word x 4-bit dynamic RAM and a 512-word x 4-bit SAM (serial access memory).

Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has a write mask function.

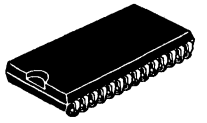
It also provides logic operation mode to simplify its operation. In this mode, logic operation between memory data and input data can be executed by using internal logic-arithmetic unit.

■ FEATURES

- Multiport Organization
  - Asynchronous and Simultaneous Operation of RAM and SAM Capability
  - RAM .....256k-word x 4-bit
  - SAM .....512-word x 4-bit
- Access Time
  - RAM .....100 ns/100 ns/120 ns/150 ns (max)
  - SAM .....30 ns/40 ns/40 ns/50 ns (max)
- Cycle Time
  - RAM .....190 ns/190 ns/220 ns/260 ns (max)
  - SAM .....30 ns/40 ns/40 ns/60 ns (max)
- Low Power
  - Active
    - RAM .....385 mW (max)
    - SAM .....358 mW (max)
  - Standby .....40 mW (max)
- High-speed Page Mode Capability
- Logic Operation Mode Capability
- 2 Types of Mask Write Mode Capability
- Bidirectional Data Transfer Cycle between RAM and SAM Capability
- Real Time Read Transfer Capability
- 3 Variations of Refresh (8 ms/512 Cycles)
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- TTL Compatible

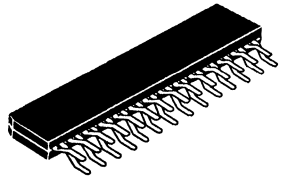
■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Inputs
I/O_0–I/O_3	RAM Port Data Inputs/Outputs
SI/O_0–SI/O_3	SAM Port Data Inputs/Outputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{DT/OE}$	Data Transfer/Output Enable
SC	Serial Clock
$\overline{SE}$	SAM Port Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection



3DCP28D

(CP-28D)

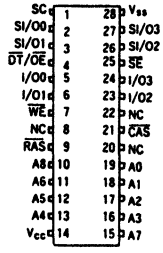


3DZP28

(ZP-28)

■ PIN OUT

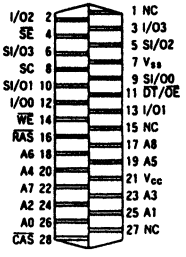
HM534252JP Series



0112-1

(Top View)

HM534252ZP Series



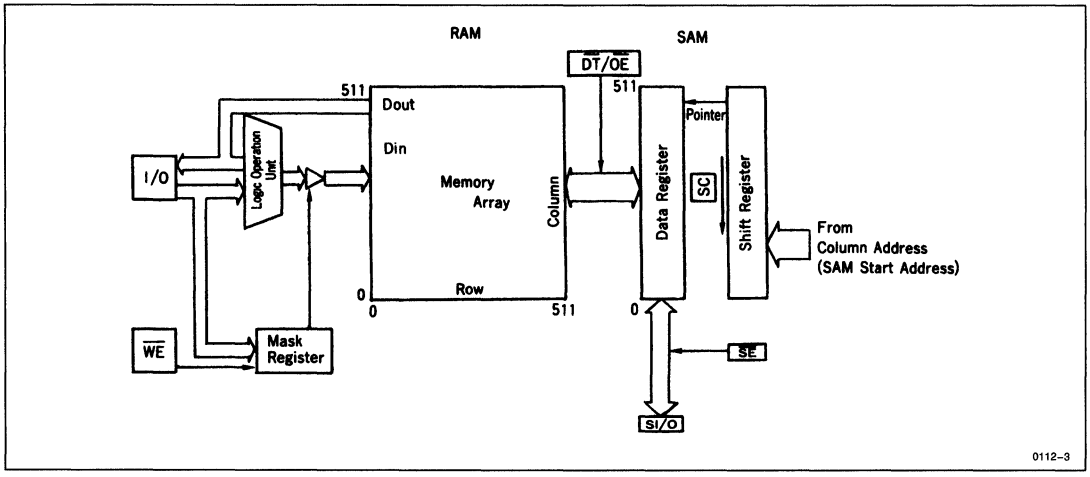
0112-2

(Bottom View)

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM534252JP-10	100 ns	400 mil
HM534252JP-11	100 ns	28-pin
HM534252JP-12	120 ns	Plastic SOJ
HM534252JP-15	150 ns	(CP-28D)
HM534252ZP-10	100 ns	400 mil
HM534252ZP-11	100 ns	28-pin
HM534252ZP-12	120 ns	Plastic ZIP
HM534252ZP-15	150 ns	(ZP-28)

■ BLOCK DIAGRAM



■ PIN FUNCTION

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of those signals determine the operation of the HM534252.

• Table 1. Operation Cycles of the HM534252

Input Level at the Falling Edge of $\overline{RAS}$				Operation Cycle
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SE}$	
H	H	H	X	RAM Read/Write
H	H	L	X	Mask Write
H	L	H	X	Read Transfer
H	L	L	H	Pseudo Transfer
H	L	L	L	Write Transfer
L	X	H	X	CBR Refresh
L	X	L	X	Logic Operation Set/Reset

Note: X; Don't care.

$\overline{CAS}$ (input pin): Column address is put into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A_0–A_8 (input pins): Row address is determined by A_0–A_8 level at the falling edge of $\overline{RAS}$. Column address is determined by A_0–A_8 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM534252 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O_0–I/O_3 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only on high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is put into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not put into the SAM data register in a serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O_0–SI/O_3 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

■ OPERATION OF HM534252

• Operation of RAM Port

RAM Read Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high, at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through I/O pin. At the falling edge of RAS, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write) ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after $\overline{RAS}$ is set low, a write cycle is executed and I/O data is written at the selected addresses. When all 4 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling edge. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables write after read to execute in the same address cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and setting $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is preserved. This mask data is effective during the $\overline{RAS}$ cycle, So, in high-speed page mode cycle, the mask data is preserved during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle and is higher than the standard page mode cycle by 70–80%. This product is based on static column mode, therefore address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RAS} max (10 μs).

Transfer Operation

The HM534252 provides the transfer cycle, pseudo transfer cycle, and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$.

They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)

(2) Determine direction of data transfer
  (a) Read transfer cycle:RAM → SAM
  (b) Write transfer cycle:RAM ← SAM

(3) Determine input or output of SAM I/O pin (SI/O)
  Read transfer cycle: SI/O output
  Pseudo transfer cycle,
  write transfer cycle: SI/O input

(4) Determine first SAM address to access (SAM start address) after transferring at column address. When SAM start address is not changed, neither CAS nor address need to be set because SAM start address can be latched internally.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, WE high at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address data (512 x 4-bit) determined by this cycle is transferred synchronously at the rising edge of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address determined by column address.

This cycle can access SAM serially even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) is specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge, and t_{SDH} (min) between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge (see figure 1).

If read transfer cycle is executed, SI/O becomes output state. When the previous transfer cycle is either pseudo transfer cycle or write transfer cycle and SI/O is in input state, uncertain data outputs after t_{RLZ} (min) after the $\overline{RAS}$ falling edge. Before that, input should be set high impedance to avoid data contention.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle is available for switching SI/O from output state to input state because data in RAM isn't rewritten. This cycle starts when $\overline{CAS}$ is high $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high, at the falling edge of $\overline{RAS}$. The output buffer in SI/O becomes high impedance within t_{SRZ} (max) from the $\overline{RAS}$ falling edge. Data should be input to SI/O later than t_{SID} (min) to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC should not be raised.

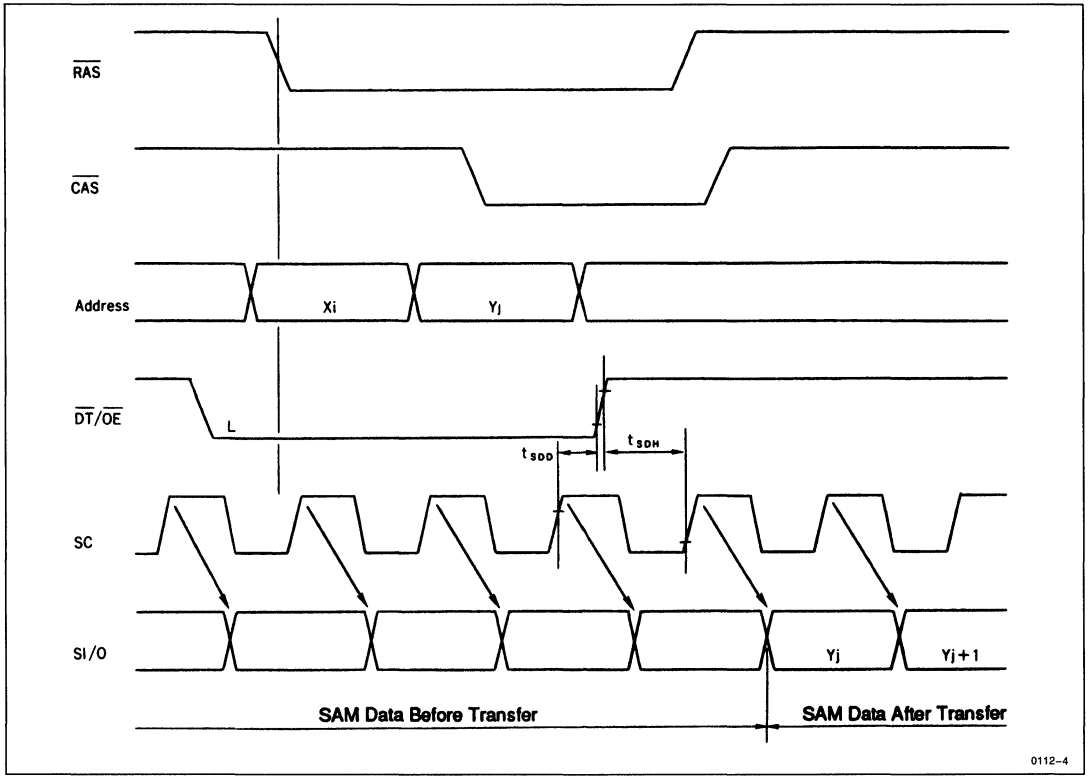


Figure 1. Real Time Read Transfer

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address to serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC should not be raised.

• SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. If $\overline{SE}$ is set high SI/O becomes high impedance and internal pointer is incremented at the SC rising edge.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is programmed into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't input into data register. Internal pointer is incremented according to the SC rising edge, so $\overline{SE}$ high can mask data for SAM.

• Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is performed by accessing all 512 row addresses every 8 ms. There are three refresh cycles: (1) $\overline{RAS}$ only refresh cycle, (2) $\overline{CAS}$ before $\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required for accessing all row addresses every 8 ms.

$\overline{RAS}$ Only Refresh Cycle: $\overline{RAS}$ only refresh cycle is performed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high by inputting the row address (= refresh address) from external circuits. In this cycle, output is high-impedance and power dissipation is less than that of normal read/write cycles because $\overline{CAS}$ internal circuits don't operate. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ should be high at the falling edge of $\overline{RAS}$.

CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address does not need to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered like in $\overline{RAS}$ only refresh cycles because $\overline{CAS}$ circuits don't operate. To distinguish this cycle from logic operation set/reset cycle, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$.

Hidden Refresh Cycle: Hidden refresh cycle performs refresh by reactivating RAS when DT/OE and CAS keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register, selector), organized as fully static circuitry, don't require refresh.

Logic Operation Mode

The HM534252 supports logic operation capability on RAM port. It performs logic operations between the memory cell data and input data in logic operation mode cycle, and writes the result into the memory cell (read modify write). This function realizes high speed raster operations and simplifies peripheral circuits for raster operations.

Logic Operation Set/Reset Cycle ($\overline{CAS}$ and $\overline{WE}$ Low at the falling edge of $\overline{RAS}$)

In logic operation set/reset cycle, the following operations are performed at the same time; (1) Selection of logic operations and logic operation mode set/reset, (2) Mask data programming, (3) $\overline{CAS}$ before $\overline{RAS}$ refresh.

Figure 2 shows the timing for logic operation set/reset cycle. This cycle starts when $\overline{CAS}$ and $\overline{WE}$ are low at the falling edge of $\overline{RAS}$. In this cycle, logic operation codes and mask data are programmed by row address and I/O pin at the falling edge of $\overline{RAS}$ respectively. When write cycle is performed after this cycle, the logic operation write cycle starts. In the logic operation mode, the specification of cycle time is longer than that of normal mode because read-modify-write cycle is performed internally. In this cycle, logic operation codes and mask data programmed are available until reprogrammed. In normal mode, mask data is available only for one $\overline{RAS}$ cycle. Here, the mask data programmed in normal mode is named as "temporary mask data" and the one programmed in logic operation set/reset cycle is named as "mask data".

(1) Selection of logic operations and logic operation mode set/reset

Table 2 shows the logic operations. One operation is selected among sixteen ones by combinations of A0–A3 levels at the falling edge of $\overline{RAS}$. (A4–A8 are Don't care.) Logic operation codes (A3, A2, A1, A0) = (0, 1, 0, 1) resets the logic operation mode. When write cycle is performed after than, normal write cycle starts. However, even in this case, mask data is still available. I/O should be at high level at the falling edge of $\overline{RAS}$ in logic operation set/reset cycle when mask data is not used.

(2) Mask data programming

High/low level of I/O at the falling edge of $\overline{RAS}$ functions as mask data. When I/O is high, the data is written in write cycle. When I/O is low, the input data is masked and the same memory cell data remains. Mask data, programmed in this cycle, is available until reprogrammed. It is advantageous when the same mask data continues.

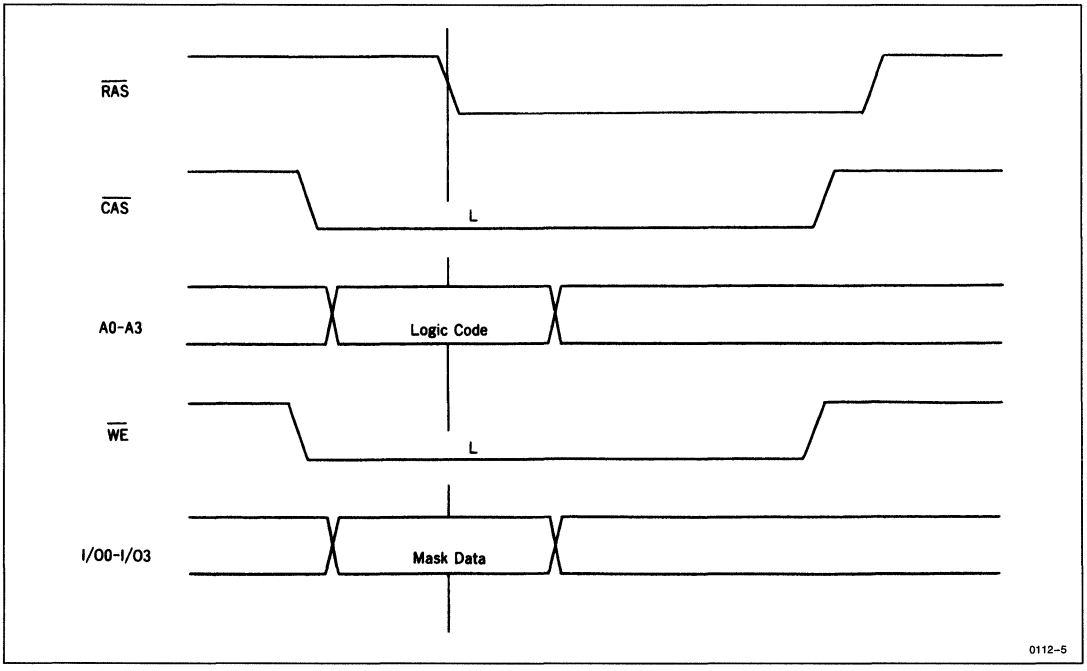


Figure 2. Logic Operation Set/Reset

• Table 2. Logic Code

Logic Code				Symbol	Write Data	Note
A3	A2	A1	A0			
0	0	0	0	Zero	0	Logic Operation Mode Set
0	0	0	1	AND1	Di • Mi	
0	0	1	0	AND2	$\overline{Di}$ • Mi	
0	0	1	1	—	Mi	
0	1	0	0	AND3	Di • $\overline{Mi}$	
0	1	0	1	THROUGH	Di	Logic Operation Mode Reset
0	1	1	0	EOR	$\overline{Di}$ • Mi + Di • $\overline{Mi}$	Logic Operation Mode Set
0	1	1	1	OR1	Di • Mi	
1	0	0	0	NOR	$\overline{Di}$ • $\overline{Mi}$	
1	0	0	1	ENOR	Di • Mi + $\overline{Di}$ • $\overline{Mi}$	
1	0	1	0	INV1	$\overline{Di}$	
1	0	1	1	OR2	$\overline{Di}$ + Mi	
1	1	0	0	INV2	$\overline{Mi}$	
1	1	0	1	OR3	Di + $\overline{Mi}$	
1	1	1	0	NAND	$\overline{Di}$ + $\overline{Mi}$	
1	1	1	1	One	1	

Notes: Di; External data-in
Mi; The data of the memory cell

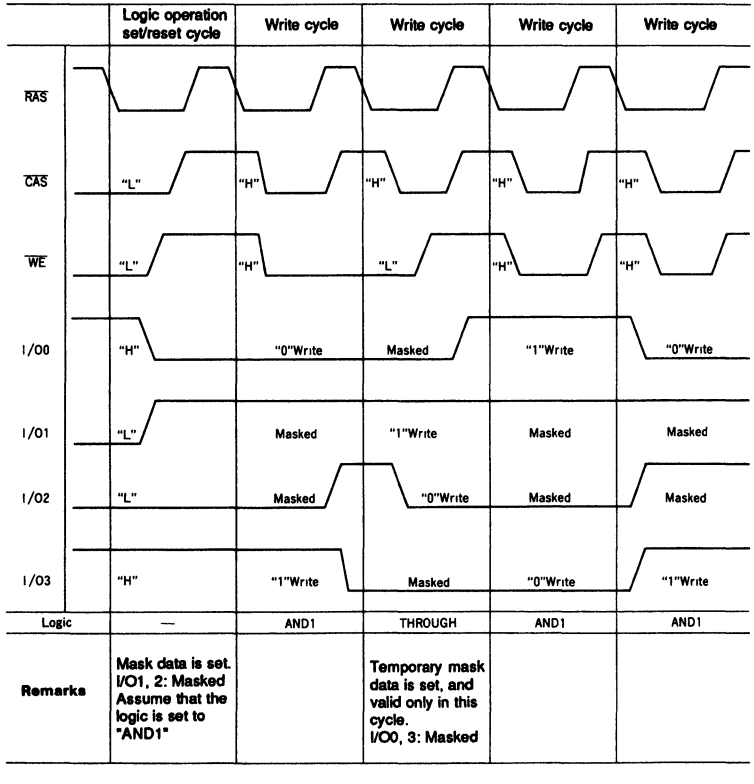


Figure 3. 2 Types of Mask Write Function and Logic Operation Function

Also, temporary mask data is programmed by falling $\overline{WE}$ at the falling edge of $\overline{RAS}$ in logic operation mode cycle after mask data is programmed in logic operation set/reset cycle. In this case, temporary mask data is available only for one cycle.

Logic operation is reset during temporary mask write cycle. It means that external input data is written into I/O when temporary mask data is set. Figure 4 shows write mask and logic operations. These functions are useful when RAM port is divided into frame buffer area and data area, as they save the need to reprogram logic operation codes and mask data.

Write Cycle in Logic Operation Mode (Early Write, Delayed Write, Page Mode)

Write cycle after logic operation set cycle is logic operation mode cycle. In this cycle, the following read-modify-write operation is performed internally.

(1) Reading memory data in given address into internal bus.

(2) Performing operation between input data and memory data.

(3) Writing the result of (2) into address given by (1).

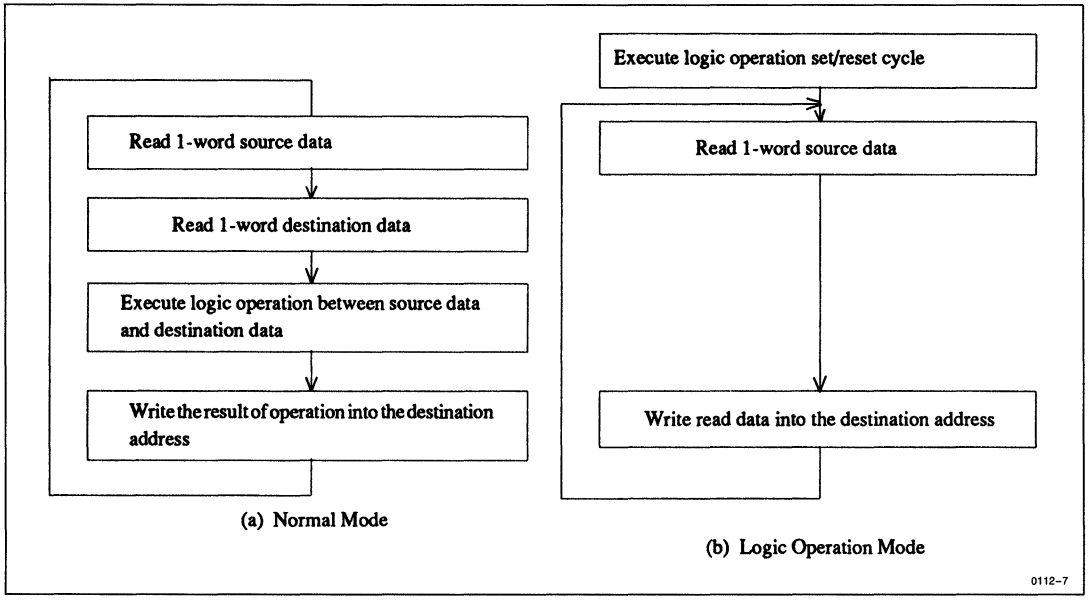


Figure 4. Sequence of Raster Operation

Figure 4 shows sequence of raster operation. Raster operation which needs 3 cycles (destination read, operation, destination write) in normal mode can be executed in one write cycle of logic operation mode. It makes raster operation faster and simplifies peripheral hardware for raster operation.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Note
Terminal Voltage	V_T	−1.0 to +7.0	V	1
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V	1
Power Dissipation	P_T	1.0	W	
Operating Temperature	T_{opr}	0 to +70	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

Note: 1. Relative to V_{SS}.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−0.5	—	0.8	V	1, 2

Notes: 1. All voltages referenced to V_{SS}.
2. −3.0V for pulse width ≤ 10 ns.

• **DC Characteristics** (T_A = 0 to 70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Test Conditions		Note
		Min	Max	Min	Max	Min	Max	Min	Max		RAM Port	SAM Port	
Operating Current	I_{CC1}	—	70	—	70	—	60	—	55	mA	$\overline{RAS}$,	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC7}	—	120	—	120	—	100	—	85	mA	$\overline{CAS}$ Cycling t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	1, 2
Standby Current	I_{CC2}	—	7	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC8}	—	65	—	55	—	55	—	40	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	1
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	70	—	70	—	60	—	55	mA	$\overline{RAS}$ Cycling	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC9}	—	120	—	120	—	100	—	85	mA	$\overline{CAS}$ = V_{IH} t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	2
Page Mode Current	I_{CC4}	—	80	—	80	—	70	—	60	mA	$\overline{CAS}$ Cycling	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC10}	—	130	—	130	—	110	—	90	mA	$\overline{RAS}$ = V_{IL} t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	1, 3
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC5}	—	60	—	60	—	50	—	40	mA	$\overline{RAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC11}	—	110	—	110	—	90	—	70	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Data Transfer Current	I_{CC6}	—	95	—	95	—	90	—	85	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC12}	—	135	—	135	—	125	—	115	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	2
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	−10	10	μA			
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	−10	10	μA			
Output High Voltage	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V	I_{OH} = −2 mA		
Output Low Voltage	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA		

Notes: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

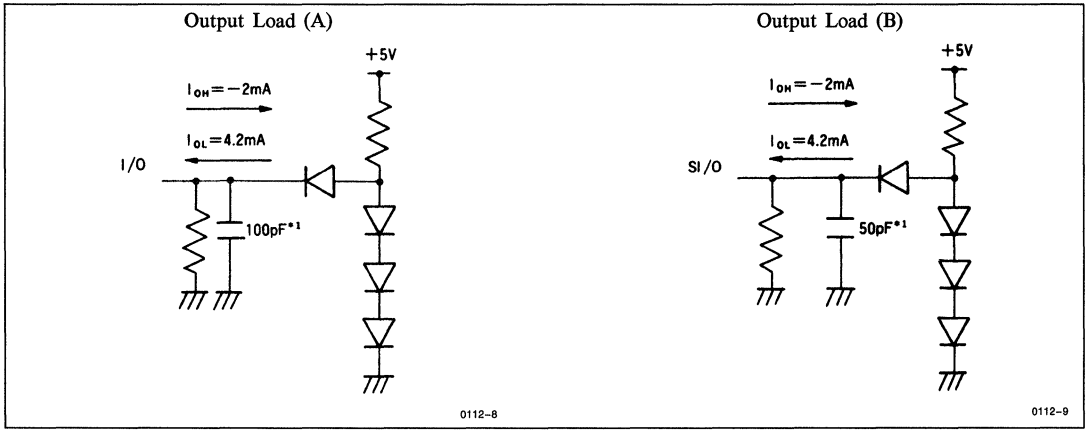
• **Capacitance** (T_A = 25°C, V_{CC} = 5V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, Address = V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

• AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 11]

Test Conditions

Input Rise and Fall Time	5 ns
Output Load	See figures
Input Timing Reference Levels	0.8V, 2.4V
Output Timing Reference Levels	0.4V, 2.4V



Note: *1. Including scope & jig.

Common Parameter

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	190	—	190	—	220	—	260	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	80	—	80	—	90	—	100	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	30	10000	30	10000	35	10000	40	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	15	—	20	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	70	25	70	25	85	30	110	ns	5, 6
$\overline{RAS}$ Hold Time	t_{RSH}	30	—	30	—	35	—	40	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise to Fall)	t_T	3	50	3	50	3	50	3	50	ns	8
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	—	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	—	15	—	15	—	20	—	ns	
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	0	—	0	—	ns	
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	0	—	0	—	ns	

Read Cycle (RAM), Page Mode Read Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	3, 5
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	45	—	55	—	70	ns	3, 6
Output Buffer Turn-off Delay Referenced to $\overline{CAS}$	t_{OFF1}	—	25	—	25	—	30	—	40	ns	7
Output Buffer Turn-off Delay Referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	7
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	0	—	ns	12
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20	55	20	55	20	65	25	80	ns	5, 6
Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	20	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	—	75	ns	

Write Cycle (RAM), Page Mode Write Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	9
Write Command Hold Time	t_{WCH}	25	—	25	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	25	—	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	
Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	20	—	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Modify Write Cycle Time	t_{RWC}	255	—	255	—	295	—	350	—	ns	
$\overline{RAS}$ Pulse Width	t_{RWS}	165	10000	165	10000	195	10000	240	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	65	—	65	—	75	—	90	—	ns	9
Column Address to $\overline{WE}$ Delay	t_{AWD}	80	—	80	—	95	—	120	—	ns	9
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	25	—	25	—	30	—	40	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	3, 5
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	45	—	55	—	70	ns	3, 6
$\overline{RAS}$ to Column Address Delay	t_{RAD}	20	55	20	55	20	65	25	80	ns	5, 6
Output Buffer Turn-off Delay Referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	25	—	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	

Refresh Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CHR}	20	—	20	—	25	—	30	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

Transfer Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
$\overline{SE}$ to $\overline{RAS}$ Setup Time	t_{ES}	0	—	0	—	0	—	0	—	ns	
$\overline{SE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	—	15	—	15	—	20	—	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	—	30	—	30	—	35	—	ns	
SC to $\overline{RAS}$ Setup Time	t_{SRS}	30	—	40	—	40	—	45	—	ns	
DT Hold Time from $\overline{RAS}$	t_{RDH}	80	—	90	—	90	—	110	—	ns	
DT Hold Time from $\overline{CAS}$	t_{CDH}	20	—	30	—	30	—	45	—	ns	
Last SC to DT Delay Time	t_{SDD}	5	—	5	—	5	—	10	—	ns	
First SC to DT Hold Time	t_{SDH}	20	—	25	—	25	—	30	—	ns	
DT to $\overline{RAS}$ Lead Time	t_{DTL}	50	—	50	—	50	—	50	—	ns	
DT Hold Time Referenced to $\overline{RAS}$ High	t_{DTHH}	20	—	25	—	25	—	30	—	ns	
DT Precharge Time	t_{DTP}	30	—	35	—	35	—	40	—	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	—	60	—	60	—	75	—	ns	
Serial Data Input to $\overline{RAS}$ Delay Time	t_{SZR}	—	10	—	10	—	10	—	10	ns	
Serial Output Buffer Turn-off Delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	60	10	75	ns	7
$\overline{RAS}$ to S_{out} (Low-Z) Delay Time	t_{RLZ}	5	—	10	—	10	—	10	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Serial Clock Cycle Time	t_{SCC2}	40	—	40	—	40	—	60	—	ns	13
Access Time from SC	t_{SCA}	—	30	—	40	—	40	—	50	ns	4
Serial Data-out Hold Time	t_{SOH}	7	—	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	20	—	25	—	ns	

Serial Read Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Access Time from SC	t_{SCA}	—	30	—	40	—	40	—	50	ns	4
Access Time from $\overline{SE}$	t_{SEA}	—	25	—	30	—	30	—	40	ns	4
Serial Data-out Hold Time	t_{SOH}	7	—	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{SE}$	t_{SEZ}	—	25	—	25	—	25	—	30	ns	7

Serial Write Cycle

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	20	—	25	—	ns	
Serial Write Enable Setup Time	t_{SWS}	0	—	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	t_{SWH}	30	—	35	—	35	—	50	—	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	—	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	30	—	35	—	35	—	50	—	ns	

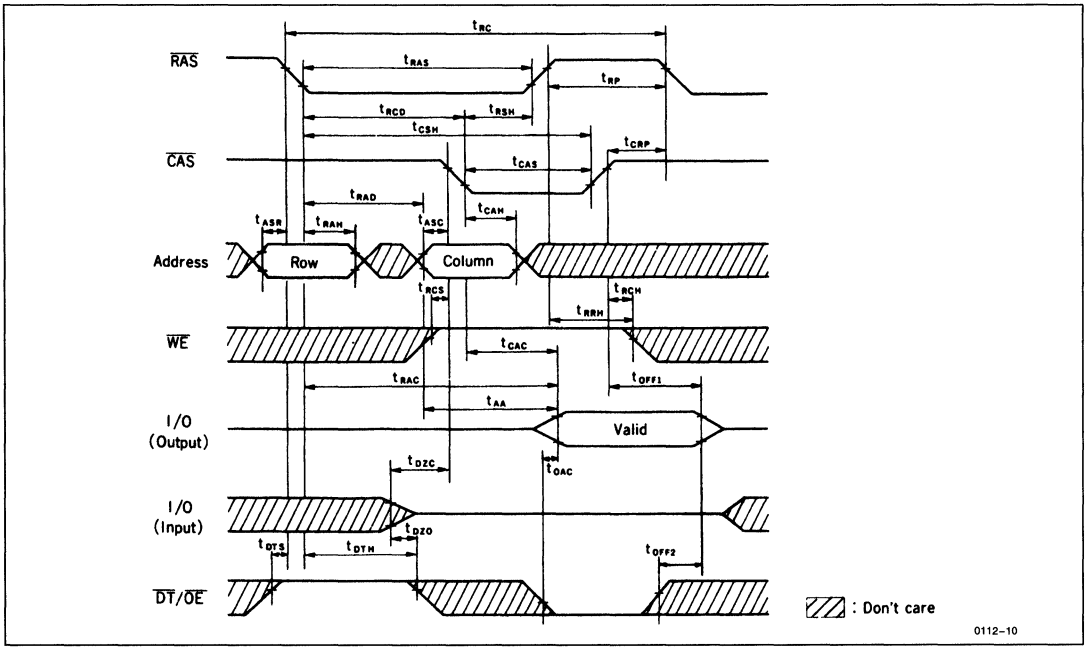
Logic Operation Mode

Parameter	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Hold Time (Logic Operation Set/Reset Cycle)	t_{FCHR}	90	—	90	—	100	—	120	—	ns	
$\overline{RAS}$ Pulse Width in Write Cycle	t_{RFS}	140	10000	140	10000	165	10000	200	10000	ns	
$\overline{CAS}$ Pulse Width in Write Cycle	t_{CFS}	60	10000	60	10000	70	10000	80	10000	ns	
$\overline{CAS}$ Hold Time in Write Cycle	t_{FCSH}	140	—	140	—	165	—	200	—	ns	
$\overline{RAS}$ Hold Time in Write Cycle	t_{FRSH}	60	—	60	—	70	—	80	—	ns	
Write Cycle Time	t_{FRC}	230	—	230	—	265	—	310	—	ns	
Page Mode Cycle Time (Write Cycle)	t_{FPC}	85	—	85	—	100	—	120	—	ns	

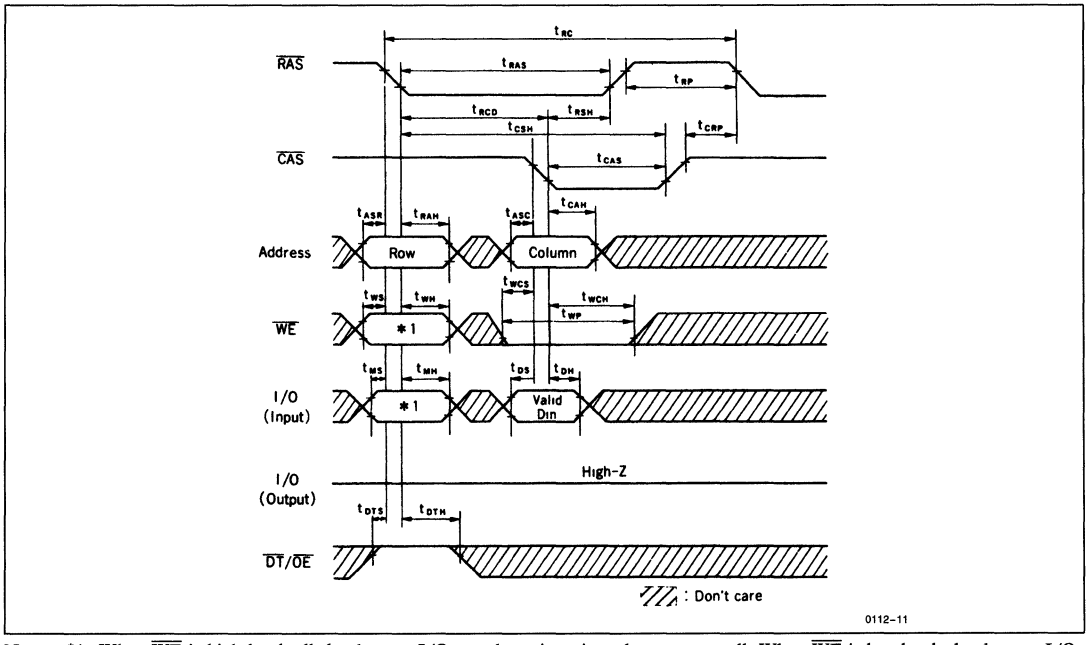
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds that value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
5. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
6. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
7. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition (V_{OH} − 200 mV, V_{OL} + 200 mV).
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
9. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-modify-write cycle; the data of the selected address is read out from a data output pin and input data is written into the selected address. In this case, impedance on I/O pins is controlled by $\overline{OE}$.
10. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles or to $\overline{WE}$ falling edge in delayed write or read-modify-write cycles.
11. After power-up, pause for 100 μs or more and execute at least 8 initialization cycles (normal memory cycles or refresh cycles), then start operation.
12. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.
13. t_{SCC2} is defined as the last SAM cycle time before read transfer in read transfer cycle (1).

■ TIMING WAVEFORMS

• Read Cycle

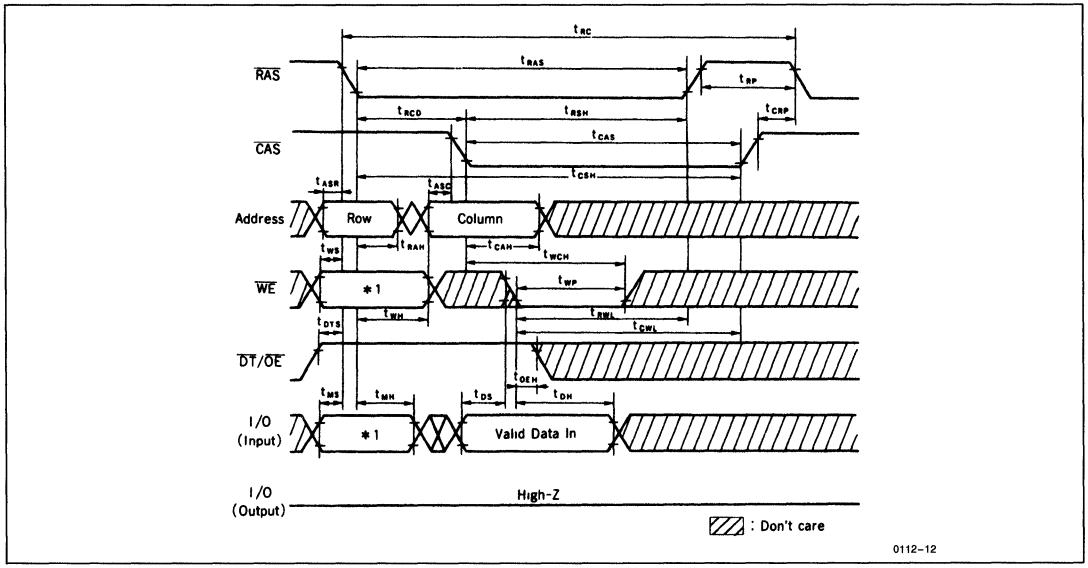


• Early Write Cycle



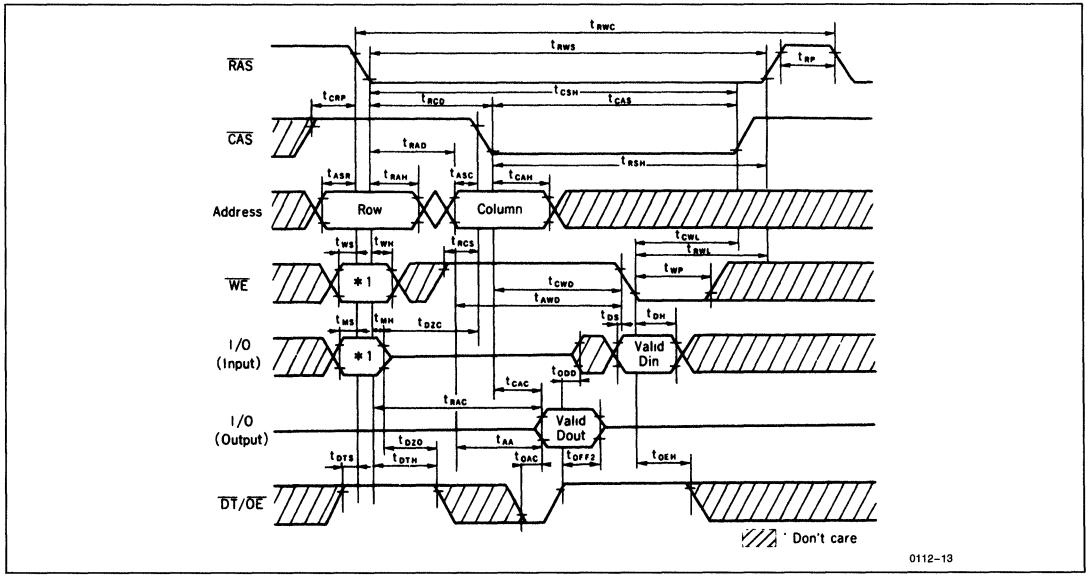
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Delayed Write Cycle**



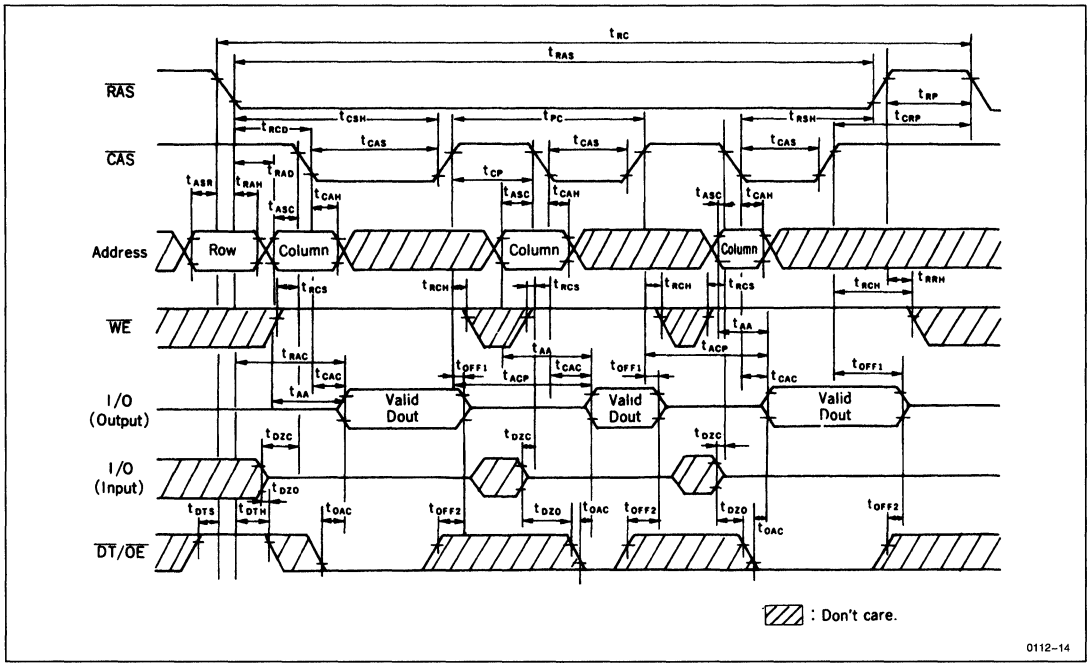
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Read-Modify-Write Cycle**

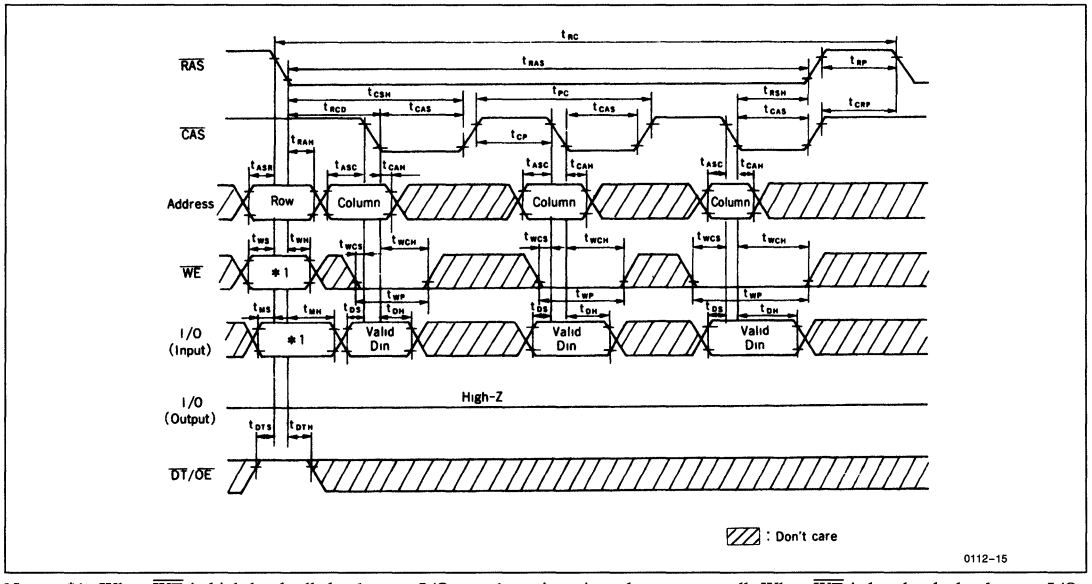


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Page Mode Read Cycle**

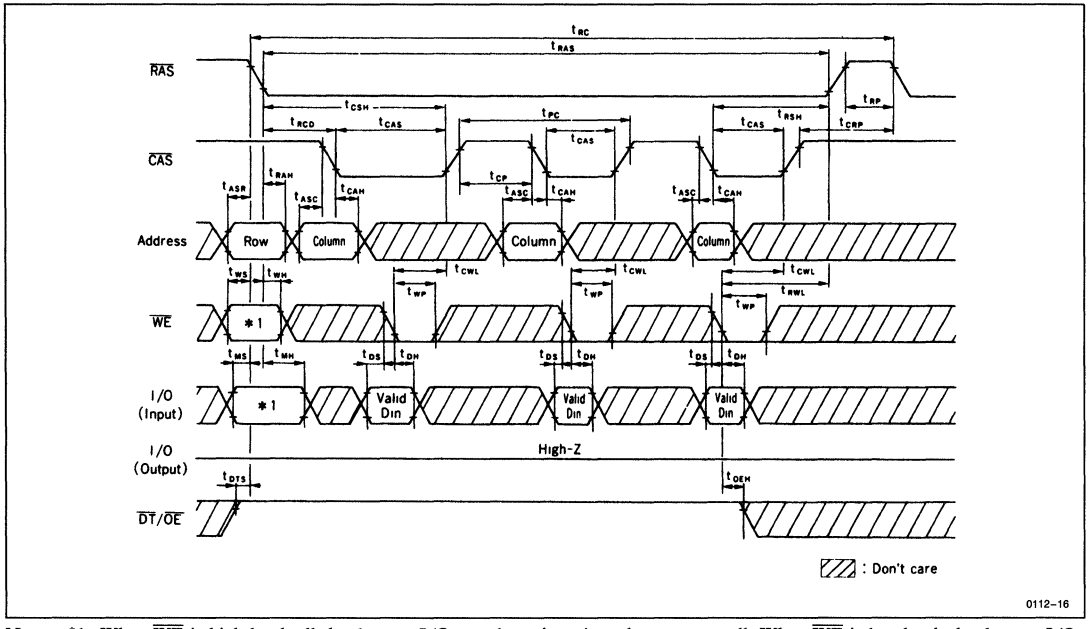


• **Page Mode Write Cycle (Early Write)**



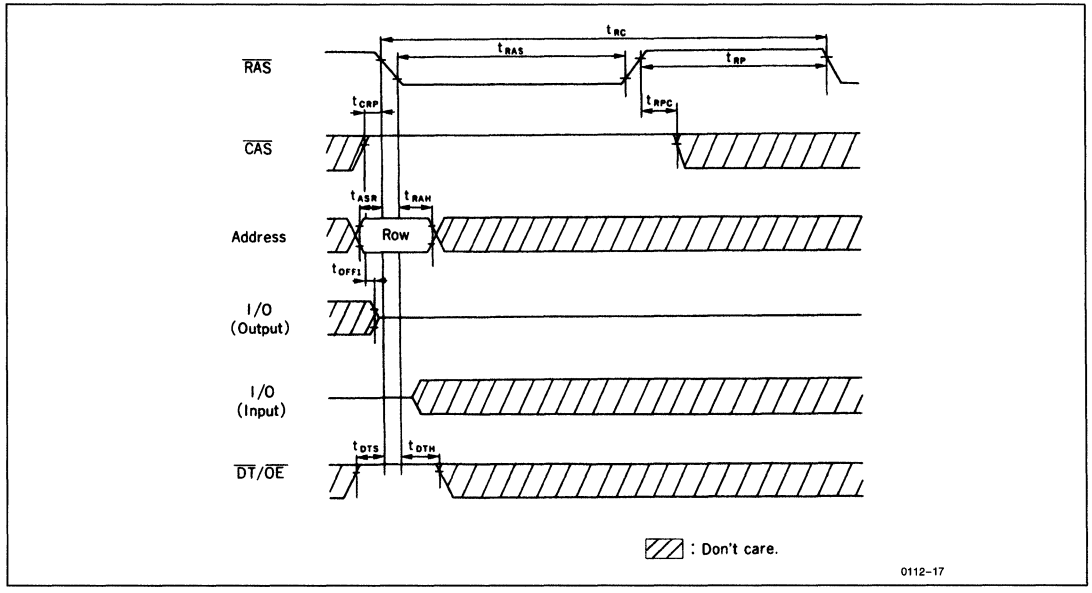
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• Page Mode Write Cycle (Delayed Write)

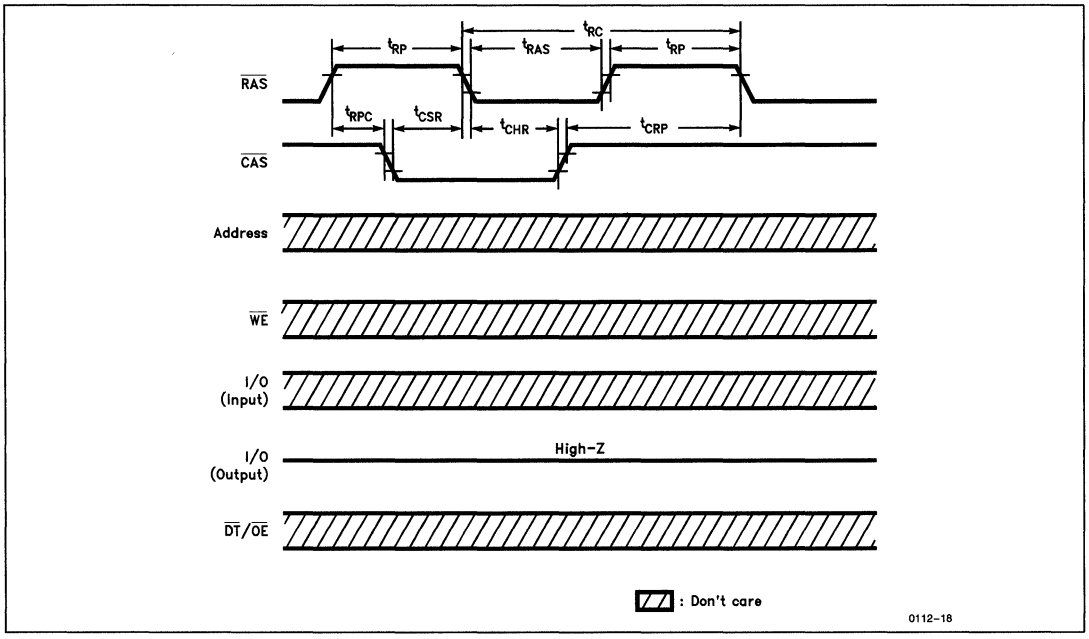


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

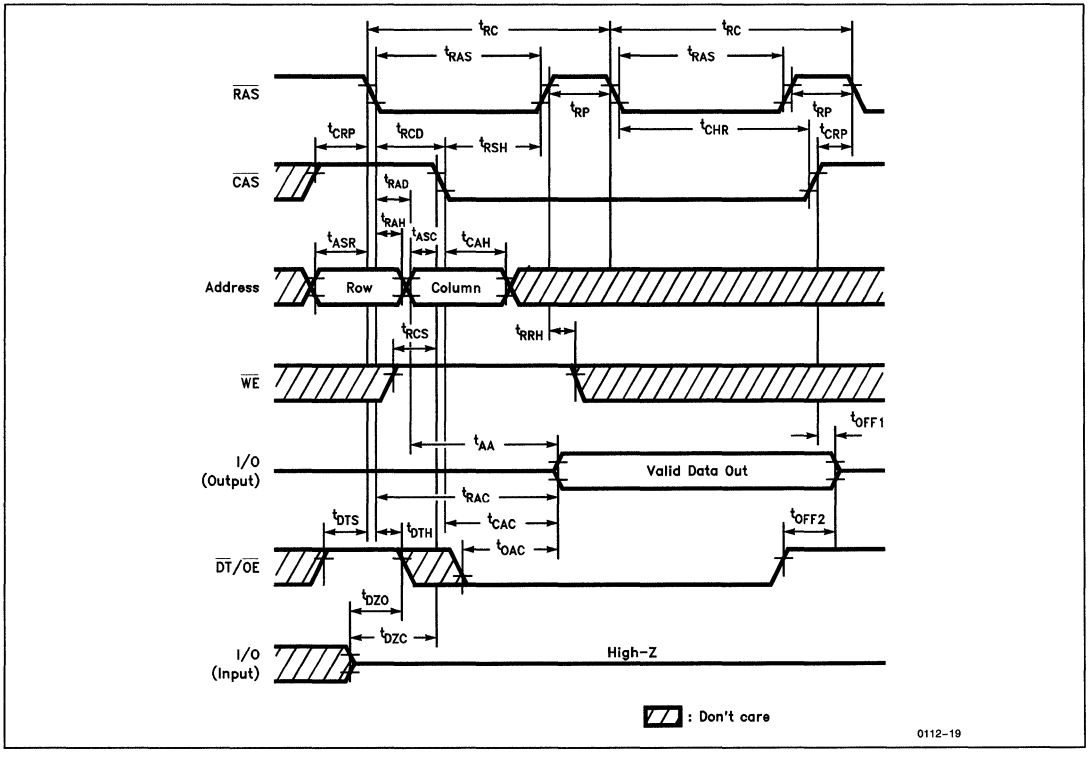
• $\overline{RAS}$ Only Refresh Cycle



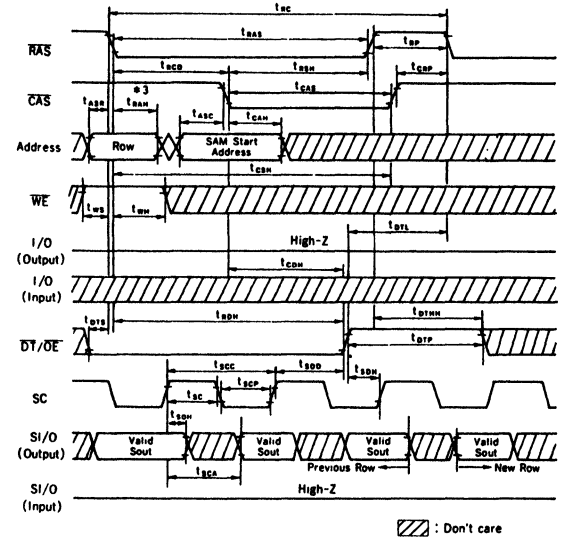
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• Hidden Refresh Cycle

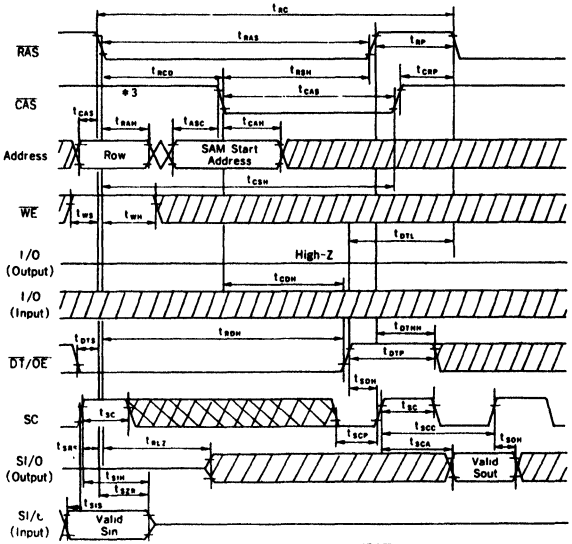


• Read Transfer Cycle (1)*1, *2



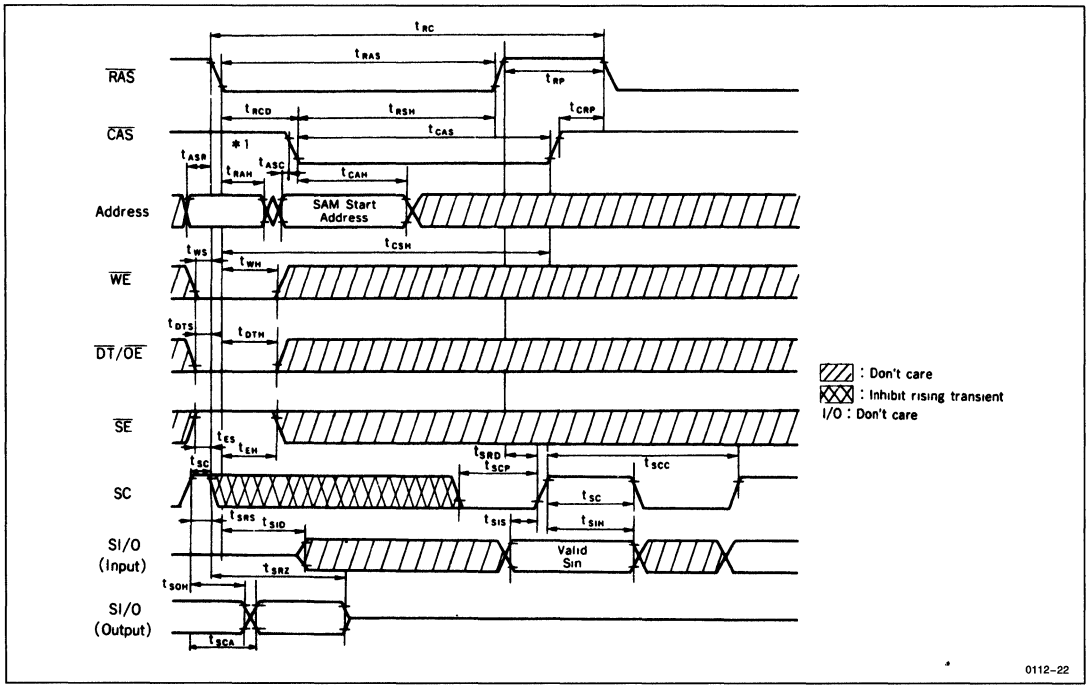
Notes: *1. When the previous data transfer cycle is a read transfer cycle, it is defined as read transfer cycle (1).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• Read Transfer Cycle (2)*1, *2



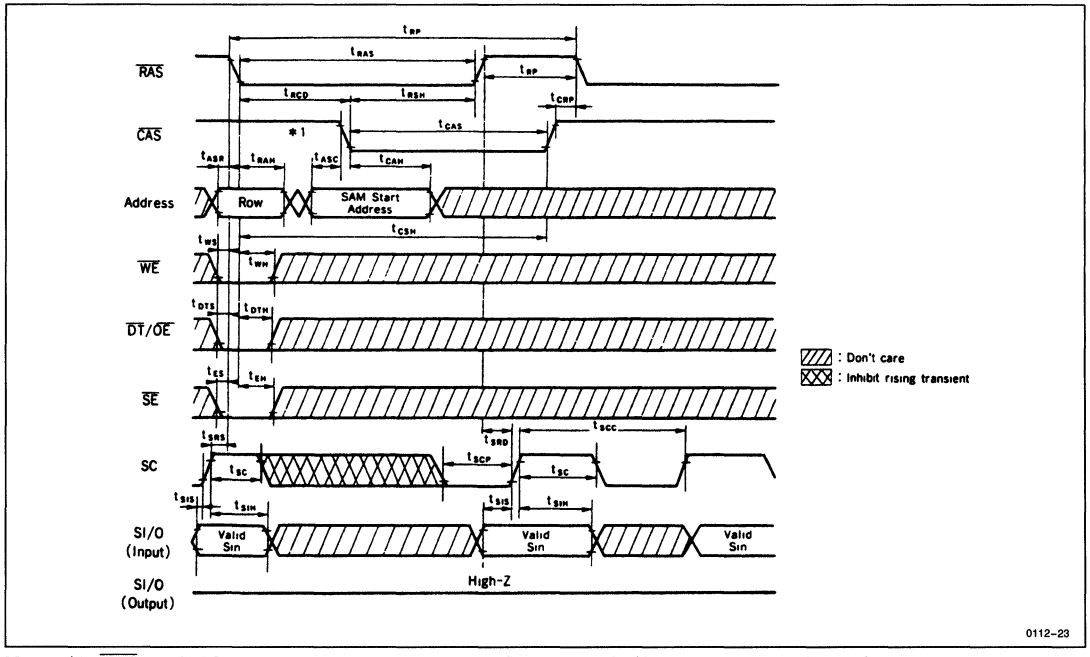
Notes: *1. When the previous data transfer cycle is a write or pseudo transfer cycle, it is defined as read transfer cycle (2).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• **Pseudo Transfer Cycle**



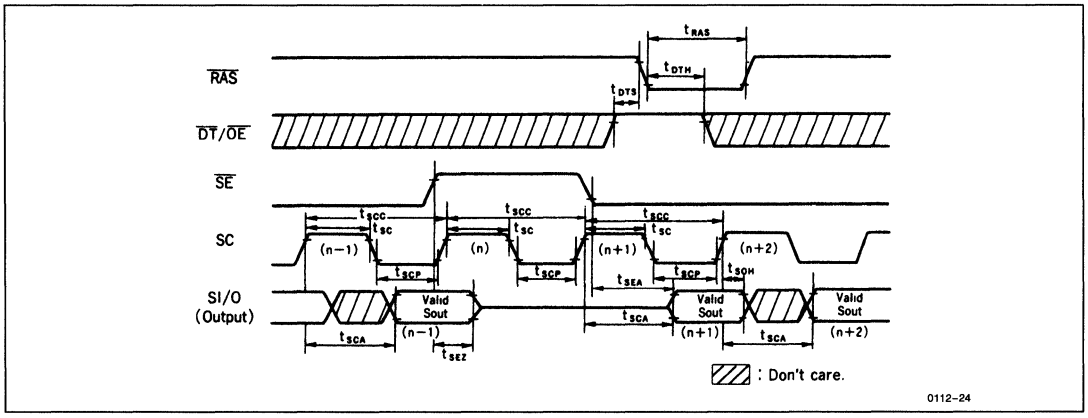
Note: *1. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• **Write Transfer Cycle**

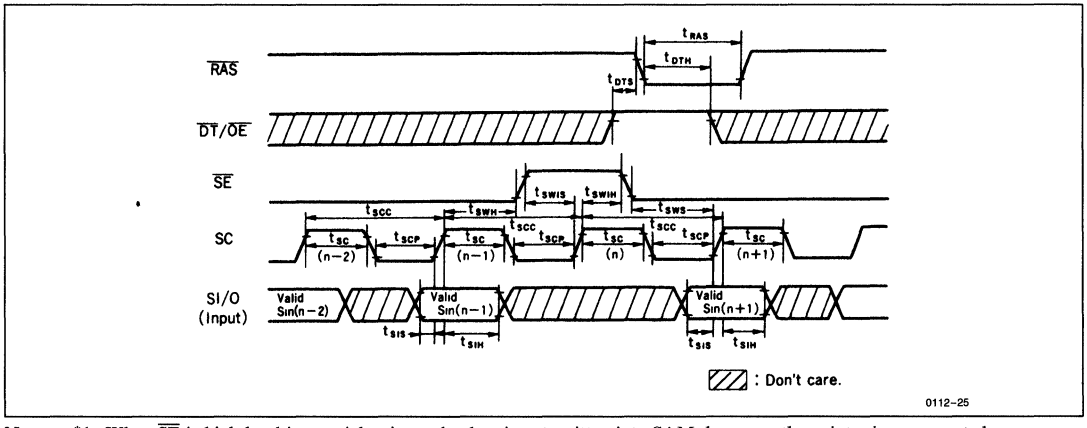


Note: *1. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• **Serial Read Cycle**

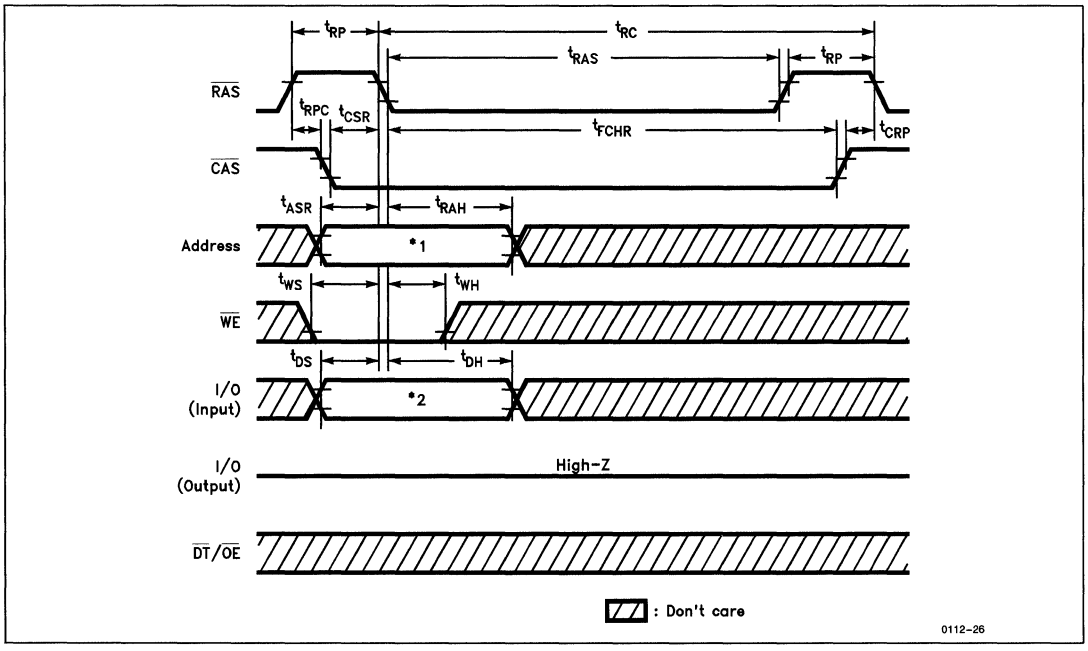


• **Serial Write Cycle**



Notes: *1. When $\overline{SE}$ is high level in a serial write cycle, data is not written into SAM, however, the pointer is incremented.
*2. Address 0 is accessed next to address 511.

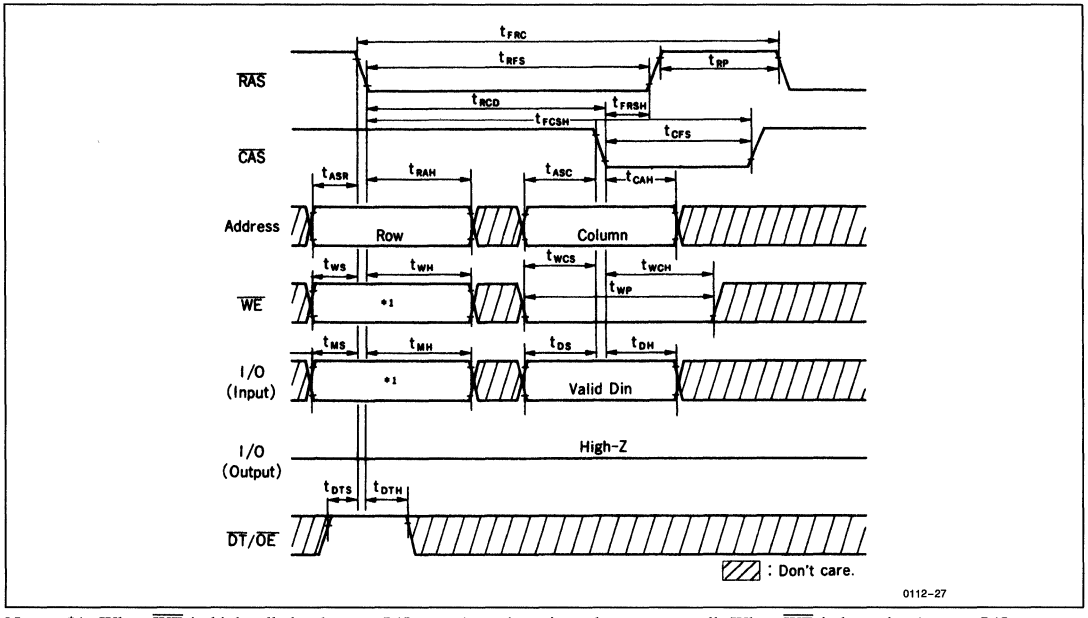
• **Logic Operation Set/Reset Cycle**



Notes: *1. Logic code A0–A3.
*2. Write mask data.

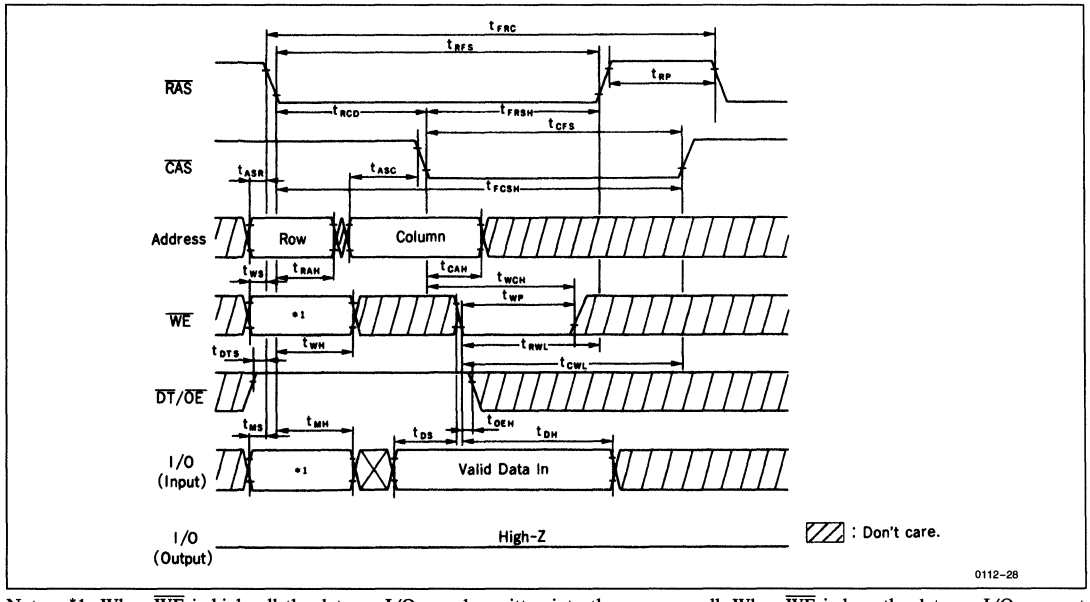
■ LOGIC OPERATION MODE TIMING WAVEFORMS

• Early Write Cycle



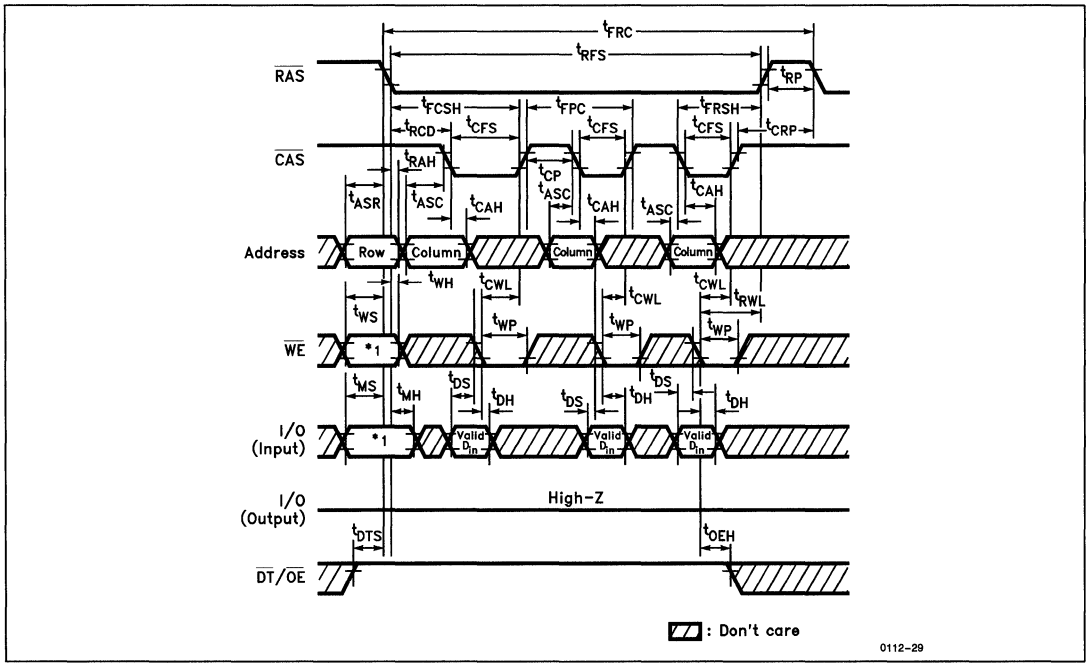
Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• Delayed Write Cycle



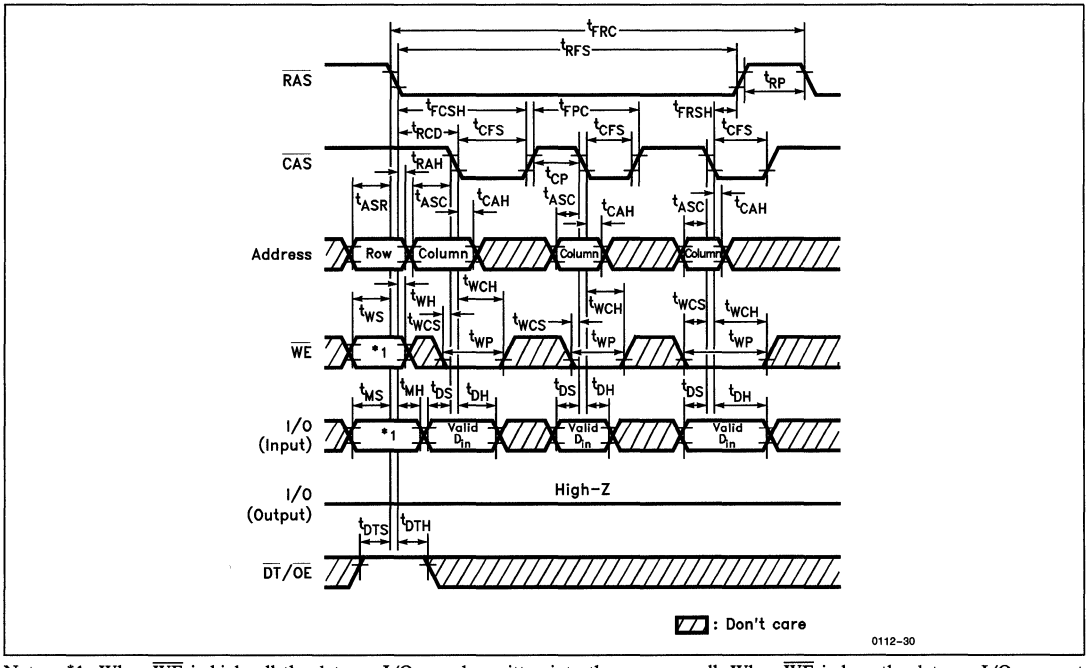
Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Page Mode Write Cycle (Delayed Write)**



Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Page Mode Write Cycle (Early Write)**



Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

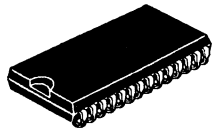
HM534253 Series

262,144-Word x 4-Bit Multiport CMOS Video RAM

■ DESCRIPTION

The HM534253 is a 1-Mbit multiport video RAM equipped with a 256k-word x 4-bit dynamic RAM and a 512-word x 4-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has a write mask function. In addition, it has two new functions. Flash write clears the data of one row in one cycle in RAM. Special read transfer internally detects that the last address in SAM is read and transfers the next data of one row automatically from RAM if a transfer cycle has previously been executed. These functions make it easier to use the HM534253.

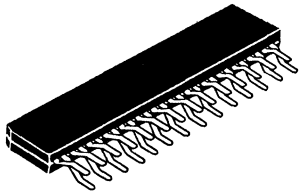
HM534253JP Series



3DCP28D

(CP-28D)

HM534253ZP Series



3DZP28

(ZP-28)

■ FEATURES

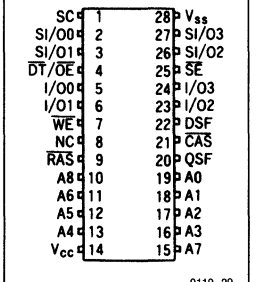
- Multiport Organization
  - Asynchronous and Simultaneous Operation of RAM and SAM Capability
  - RAM ..... 256k-word x 4-Bit
  - SAM ..... 512-word x 4-Bit
- Access Time RAM ..... 100 ns/120 ns/150 ns (max)
- SAM ..... 30 ns/40 ns/50 ns (max)
- Cycle Time RAM ..... 190 ns/220 ns/260 ns (min)
- SAM ..... 30 ns/40 ns/60 ns (min)
- Low Power
  - Active RAM ..... 385 mW (max)
  - SAM ..... 275 mW (max)
  - Standby ..... 40 mW (max)
- High-Speed Page Mode Capability
- Mask Write Mode Capability
- Bidirectional Data Transfer Cycle Between RAM and SAM Capability
- Special Read Transfer Cycle Capability
- Flash Write Cycle Capability
- 3 Variations of Refresh (8 ms/512 cycles)
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- TTL Compatible

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM534253JP-10	100 ns	400 mil 28-pin
HM534253JP-12	120 ns	Plastic SOJ
HM534253JP-15	150 ns	(CP-28D)
HM534253ZP-10	100 ns	400 mil 28-pin
HM534253ZP-12	120 ns	Plastic ZIP
HM534253ZP-15	150 ns	(ZP-28)

■ PIN OUT

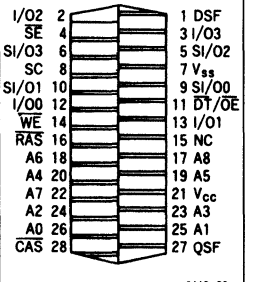
HM534253JP Series



0119-29

(Top View)

HM534253ZP Series



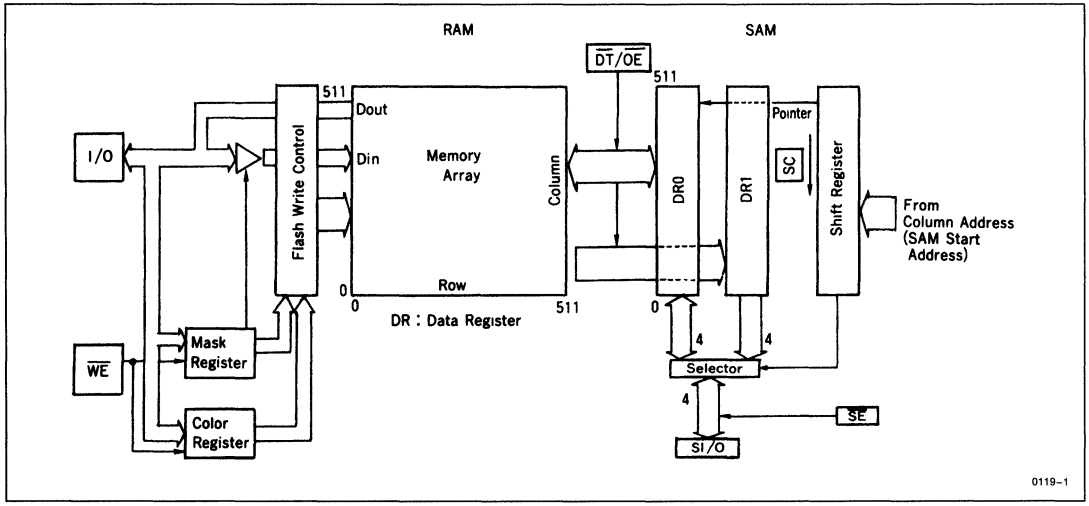
0119-30

(Bottom View)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Inputs
I/O_0–I/O_3	RAM Port Data Inputs/Outputs
SI/O_0–SI/O_3	SAM Port Data Inputs/Outputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{DT/OE}$	Data Transfer/Output Enable
SC	Serial Clock
$\overline{SE}$	SAM Port Enable
DSF	Special Function Input Flag
QSF	Data Register Empty Flag
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



■ PIN FUNCTION

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of those signals determine the operation cycle of the HM534253.

• Table 1. Operation Cycles of the HM534253

Input Level at the Falling Edge of $\overline{RAS}$					Operation Cycle
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SE}$	DSF	
H	H	H	X	L	RAM Read/Write
H	H	H	X	H	Color Register Set
H	H	L	X	L	Mask Write
H	H	L	X	H	Flash Write
H	L	H	X	L	Special Read Initialization
H	L	H	X	H	Special Read Transfer
H	L	L	H	X	Pseudo Transfer
H	L	L	L	X	Write Transfer
L	X	X	X	X	CBR Refresh

Note: X: Don't care.

$\overline{CAS}$ (input pin): Column address is put into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A_0–A_8 (input pins): Row address is determined by A_0–A_8 level at the falling edge of $\overline{RAS}$. Column address is determined by A_0–A_8 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM534253 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O_0–I/O_3 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write and flash write mode). Data is written only on high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data is output from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is put into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not put into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O_0–SI/O_3 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a special read transfer cycle or special read initialization cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

DSF (input pin): DSF is a special data input flag pin. It is set to high when new functions such as color register set, special read transfer, and flash write, are used.

QSF (output pin): The HM534253 has a double buffer organization which includes two SAM data registers to relax the restriction of timings of $\overline{DT}/\overline{OE}$ and SC in real time transfer cycle. QSF flag turns high when output from one of SAM data registers finished (data register empty flag). If the condition is detected and special read transfer cycle is executed, data is transferred to the empty register. SC (serial clock) and data transfer cycle can be set asynchronously because detection of the last address in SAM and change of data register are executed automatically in the chip. It makes the system design flexible.

■ OPERATION OF HM534253

• Operation of RAM Port

RAM Read Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high, DSF low at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data is output through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Early Write, Delayed Write, Read Modify Write) ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high, DSF low at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after driving $\overline{RAS}$ low, a write cycle is executed and I/O data is written in the selected addresses. When all 4 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read modify write cycle and enables read/write to execute in the same address cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is preserved. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is preserved during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high, DSF low at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle and is higher than the standard page mode cycle by 70–80%. This product is based on static column mode, therefore, address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RAS} max (10 μs).

• Flash Write Function (See figure 1)

- Color Register Set Cycle ($\overline{CAS}$•$\overline{DT}/\overline{OE}$•$\overline{WE}$ high, DSF high at the falling edge of $\overline{RAS}$)

In color register set cycle, color data is set to the internal color register used in flash write cycle. 4 bits of internal color register are provided at each I/O. This register is composed of static circuits, so once it is set, it preserves the data until reset. The data set is just as same as in the usual write cycle except that DSF is set high at the falling edge of $\overline{RAS}$, and early write and delayed write cycle can be executed. In this cycle, memory array access is not executed, so it is unnecessary to give row and column addresses.

- Flash Write Cycle ($\overline{CAS}$•$\overline{DT}/\overline{OE}$ high, $\overline{WE}$ low, DSF high at the falling edge of $\overline{RAS}$)

In a flash write cycle, a row of data (512 x 4 bit) is cleared to 0 or 1 at each I/O according to the data of color register mentioned before. It is also possible to mask I/O in this cycle. When $\overline{CAS}$•$\overline{DT}/\overline{OE}$ is set high, $\overline{WE}$ is low, and DSF is high at the falling edge of $\overline{RAS}$, this cycle starts. Then, the row address to clear is given to row address and mask data is to I/O. Mask data is as same as that of a RAM write cycle. High I/O is cleared, low I/O is not cleared and the internal data is preserved. Cycle time is the same as those of RAM read/write cycles, so all bits can be cleared in 1/512 of the usual cycle time.

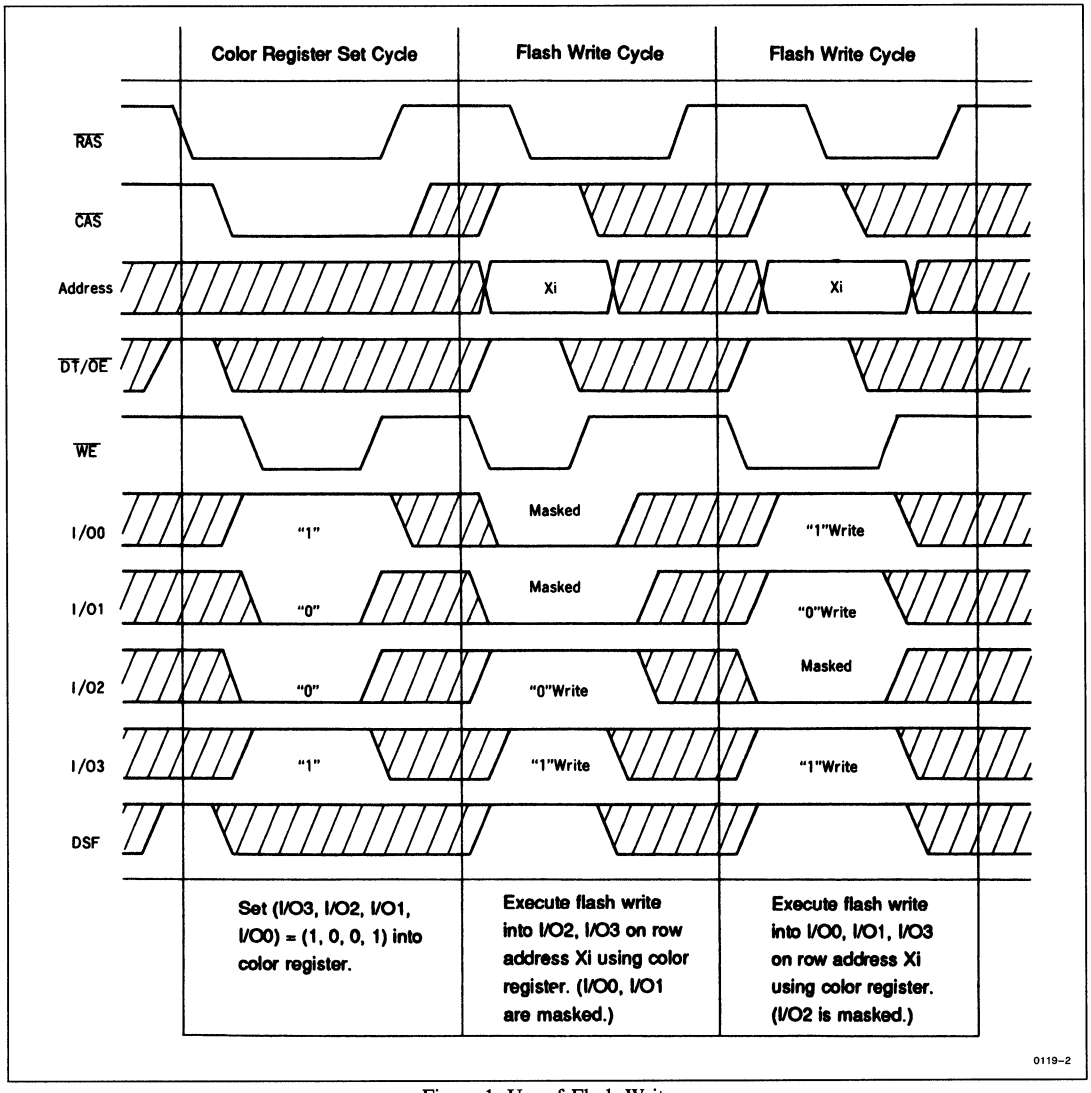


Figure 1. Use of Flash Write

• Transfer Operation

The HM534253 provides the special read initialization cycle, special read transfer cycle, pseudo transfer cycle, and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$. They have the following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)

(2) Determine direction of data transfer

(a) Special read initialization cycle,

Special read transfer cycle: RAM → SAM

(b) Write transfer cycle: RAM ← SAM

(3) Determine input or output of SAM I/O pin (SI/O) Special read initialization cycle: SI/O output

Pseudo transfer cycle, write transfer cycle: SI/O input

(4) Determine first SAM address to access (SAM start address) after transferring at column address. When SAM start address is not changed, neither $\overline{CAS}$ nor address need to be set because SAM start address can be latched internally.

Special Read Initialization Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high, DSF low at the falling edge of $\overline{RAS}$)

If $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ is low, $\overline{WE}$ high, and DSF low at the falling edge of $\overline{RAS}$, this cycle becomes a special read initialization cycle. Special read initialization is used (1) to start special read transfer operation and (2) to switch SAM input/output pin (SI/O), set in input state by pseudo transfer cycle or write transfer cycle, to output state.

If the clock is set as mentioned before, address of SAM transfer word line is set to row address and first SAM address to access (SAM start address) to column address, it becomes possible to execute SAM read after t_{SRD} (min) after $\overline{RAS}$ is high. In this cycle, SI/O outputs uncertain data after the $\overline{RAS}$ falling edge. So when SAM is in input state before executing this cycle, it is necessary to stop input before the $\overline{RAS}$ falling edge.

SAM access is inhibited while $\overline{RAS}$ is low in this cycle. SC should not be raised during $\overline{RAS}$ low.

Special Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high, DSF high at the falling edge of $\overline{RAS}$)

Ordinary multiport video RAM has some problems; (1) severe limitation on timings between processor clock $\overline{DT}/\overline{OE}$ and CRT clock SC, (2) complicated external control circuit to detect SAM last address externally and to insert transfer cycle synchronously. Special read transfer cycle makes it possible to relax the timing limitations and to set serial clock (SC) and transfer cycle perfectly synchronously.

Figure 2 shows the block diagram for a special read transfer. SAM double buffers are composed of two data registers (DR). When data is read out from DR0 serially, special read transfer cycle transfers a row of RAM data, which will be read from SAM next, to DR1.

The end of data read from DR0 is detected internally and data register switching circuit automatically switches to DR1 output. So data can be output continuously.

Figure 3 shows special read transfer operation sequence. QSF flag indicates that reading out from data register has finished (data register empty flag), and special read transfer can be executed while QSF is high. At first, special read operation starts by executing a special read initialization cycle. So QSF becomes high, the processor gives row address and SAM start address, which is need next, to the memory, and inserts a special read transfer cycle. Data register becomes full after a special read transfer cycle, so QSF becomes low during the cycle. When the last SAM address is accessed, QSF becomes high and the data register, which outputs from the next SAM address, changes, and serial access can be executed.

By executing these handshakes, serial clock and transfer cycle can be executed perfectly asynchronously, and flexibility of the system design is improved.

Special read transfer cycle is set by making $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high, and DSF high at the falling edge of $\overline{RAS}$ (same as for special read initialization cycle except DSF). Like in other transfer cycles, the address of the word line to transfer into data register is specified by row address and SAM start is specified by column address. When the last SAM address data is output, the next data is output from the SAM start address specified by this $\overline{RAS}$ cycle. This transfer cycle can be executed asynchronously with SAM cycle. However, it is necessary to execute SAM access after $\overline{RAS}$ becomes high after SAM start address is specified by $\overline{RAS}$ cycle. (See figure 4.)

QSF should be high at the falling edge of $\overline{RAS}$ to execute a special read transfer cycle. A cycle whose QSF is low is neglected (refresh is executed). When the previous transfer cycle is a pseudo transfer or write transfer cycle and SI/O is in input state, special read transfer cycle cannot be used (neglected). Special read initialization cycle is required to switch SI/O to output state.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle is available for switching SI/O from output state to input state because data in RAM isn't rewritten. This cycle starts when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high, at the falling edge of RAS. The output buffer in SI/O becomes high impedance within t_{SRZ} (max) from the $\overline{RAS}$ falling edge. Data should be input to SI/O later than t_{SID} (min) to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high, like in the special read initialization cycle. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC should not be raised.

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address to serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC should not be raised.

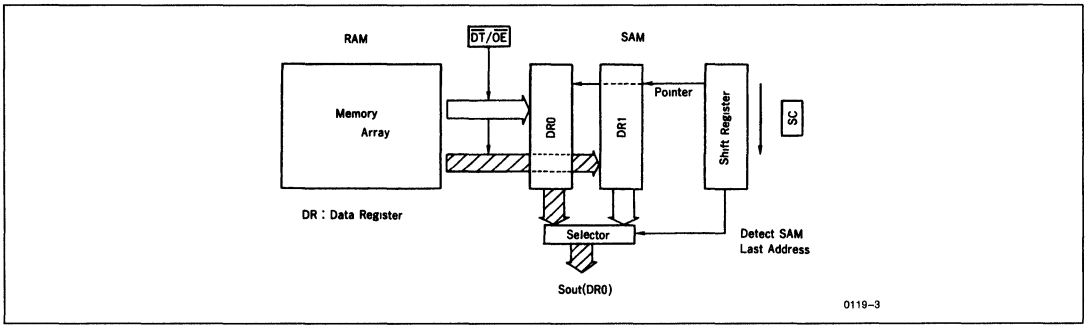


Figure 2. Block Diagram for Special Read Transfer

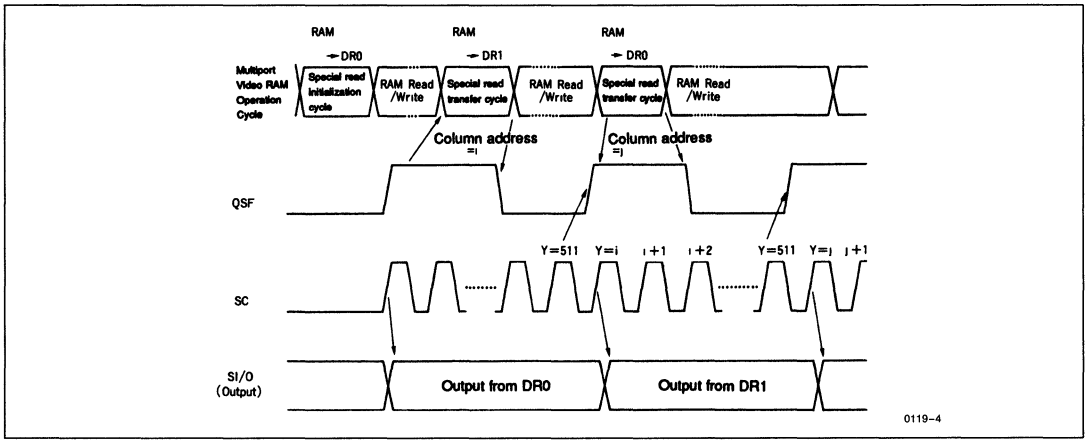


Figure 3. Special Read Transfer Operation Sequence

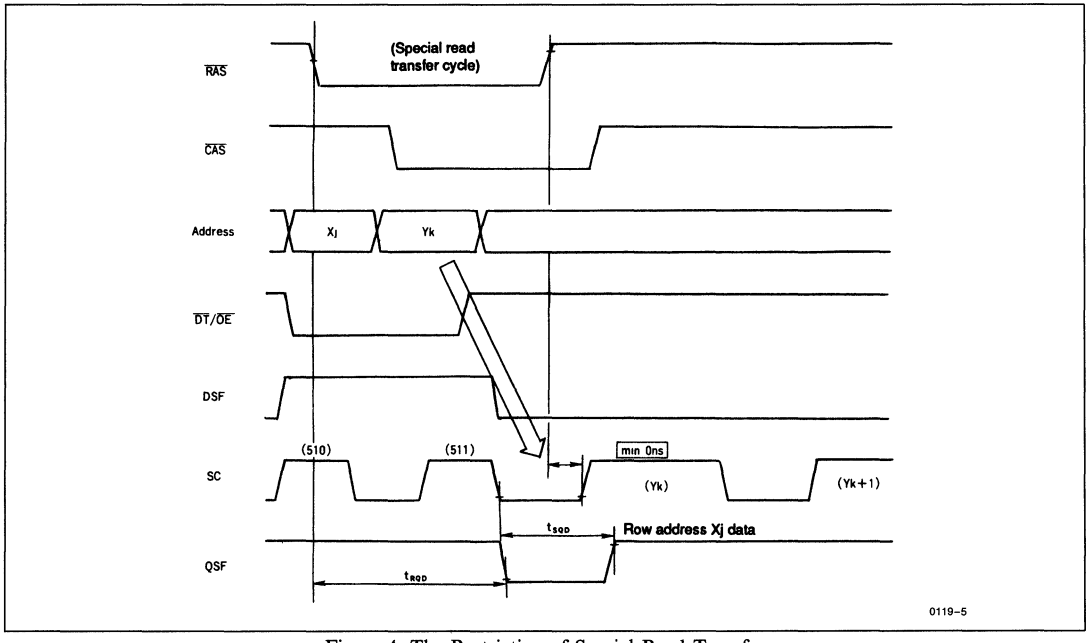


Figure 4. The Restriction of Special Read Transfer

■ SAM PORT OPERATION

• Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is special read initialization cycle or special read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When the last address is accessed at the state of QSF low (data register is full), it is signaled to external circuits that special read transfer is enabled by making QSF high. Next, after SAM access, output data register is switched, then the row address data given by previous special read transfer cycle is output from the SAM start address. If special read transfer isn't performed (QSF high), the column address 0 of the same row address is accessed after the last address is accessed.

• Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is programmed into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't input into data register. Internal pointer is incremented according to the SC rising edge, so $\overline{SE}$ high can be used to mask data for SAM.

■ REFRESH

• RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is performed by accessing all 512 row addresses every 8 ms. There are three refresh cycles: (1) $\overline{RAS}$ only refresh cycle, (2) $\overline{CAS}$ before $\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required for accessing all row addresses every 8 ms.

$\overline{RAS}$ Only Refresh Cycle: $\overline{RAS}$ only refresh cycle is performed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high by inputting the row address (= refresh address) from external circuits. In this cycle, output is high-impedance and power dissipation is less than that of normal read/write cycles because $\overline{CAS}$ internal circuits don't operate. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ should be high at the falling edge of $\overline{RAS}$.

CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered like in $\overline{RAS}$ only refresh cycles because $\overline{CAS}$ circuits don't operate.

Hidden Refresh Cycle: Hidden refresh cycle performs refresh by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

• SAM Refresh

SAM parts (data register, shift register, selector), organized as fully static circuitry, don't require refresh.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Note
Terminal Voltage	V_T	−1.0 to +7.0	V	1
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V	1
Power Dissipation	P_T	1.0	W	
Operating Temperature	T_{opr}	0 to +70	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

Note: 1. Relative to V_{SS}

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−0.5	—	0.8	V	1, 2

Notes: 1. All voltages referenced to V_{SS}.
2. −3.0V for pulse width ≤ 10 ns.

• **DC Electrical Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM534253-10		HM534253-12		HM534253-15		Unit	Test Conditions		Note
		Min	Max	Min	Max	Min	Max		RAM Port	SAM Port	
Operating Current	I_{CC1}	—	70	—	60	—	50	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC7}	—	120	—	100	—	80	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Standby Current	I_{CC2}	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC8}	—	50	—	40	—	30	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	60	—	50	—	40	mA	$\overline{RAS}$ Cycling $\overline{CAS}$ = V_{IH} t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC9}	—	110	—	90	—	70	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Page Mode Current	I_{CC4}	—	65	—	55	—	45	mA	$\overline{CAS}$ Cycling $\overline{RAS}$ = V_{IL} t_{RC} = Min	SC, $\overline{SE}$ = V_{IH}	
	I_{CC10}	—	115	—	95	—	75	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC5}	—	60	—	50	—	40	mA	$\overline{RAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC11}	—	110	—	90	—	70	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Data Transfer Current	I_{CC6}	—	90	—	90	—	90	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC12}	—	125	—	125	—	125	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	μA			
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	μA			
Output High Voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = −2 mA		
Output Low Voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA		

• **Capacitance** (T_A = 25°C, V_{CC} = 5V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, Address = V_{SS})

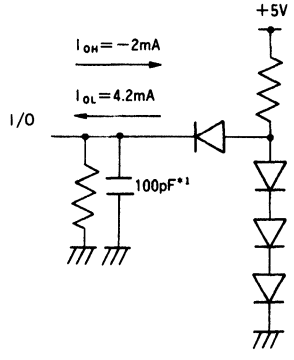
Parameter	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

• AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 11]

Test Conditions

Input Rise and Fall Time	5 ns
Output Load	See Figures
Input Timing Reference Levels	0.8V, 2.4V
Output Timing Reference Levels	0.4V, 2.4V

Output Load (A)



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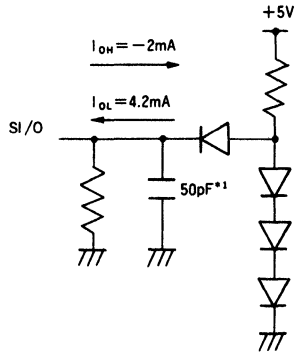
Output Load (B)



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Note: *1. Including scope & jig.

Common Parameters

Parameter	Symbol	HM534253-10		HM534253-12		HM534253-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	190	—	220	—	260	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	80	—	90	—	100	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	30	10000	35	10000	40	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	70	25	85	30	110	ns	5, 6
$\overline{RAS}$ Hold Time	t_{RSH}	30	—	35	—	40	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Transition Time (Rise to Fall)	t_T	3	50	3	50	3	50	ns	8
Refresh Period	t_{REF}	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	—	15	—	20	—	ns	
DSF to $\overline{RAS}$ Setup Time	t_{SPS}	0	—	0	—	0	—	ns	
DSF to $\overline{RAS}$ Hold Time	t_{SPH}	25	—	25	—	30	—	ns	
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	0	—	ns	
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	0	—	ns	

Read Cycle (RAM), Page Mode Read Cycle

Parameter	Symbol	HM534253-10		HM534253-12		HM534253-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	—	35	—	40	ns	3, 5
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	55	—	70	ns	3, 6
Output Buffer Turn-off Delay Referenced to $\overline{CAS}$	t_{OFF1}	0	25	0	30	0	40	ns	7
Output Buffer Turn-off Delay Referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	7
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	12
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20	55	20	65	25	80	ns	5, 6
Page Mode Cycle Time	t_{PC}	55	—	65	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	15	—	20	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	60	—	75	ns	

Write Cycle (RAM), Page Mode Write Cycle, Color Register Set Cycle

Parameter	Symbol	HM534253-10		HM534253-12		HM534253-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	9
Write Command Hold Time	t_{WCH}	25	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	35	—	40	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	15	—	20	—	ns	
Page Mode Cycle Time	t_{PC}	55	—	65	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	15	—	20	—	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM534253-10		HM534253-12		HM534253-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	255	—	295	—	350	—	ns	
$\overline{RAS}$ Pulse Width	t_{RWS}	165	10000	195	10000	240	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	65	—	75	—	90	—	ns	9
Column Address to $\overline{WE}$ Delay	t_{AWD}	80	—	95	—	120	—	ns	9
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	25	—	30	—	40	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	—	35	—	40	ns	3, 5
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	55	—	70	ns	3, 6
$\overline{RAS}$ to Column Address Delay	t_{RAD}	20	55	20	65	25	80	ns	5, 6
Output Buffer Turn-off Delay Referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	35	—	40	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	15	—	20	—	ns	

Refresh Cycle

Parameter	Symbol	HM534253-10		HM534253-12		HM534253-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CHR}	20	—	25	—	30	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

Transfer Cycle

Parameter	Symbol	HM534253-10		HM534253-12		HM534253-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	20	—	ns	
$\overline{SE}$ to $\overline{RAS}$ Setup Time	t_{ES}	0	—	0	—	0	—	ns	
$\overline{SE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	—	15	—	20	—	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	—	30	—	35	—	ns	
SC to $\overline{RAS}$ Setup Time	t_{SRS}	30	—	40	—	45	—	ns	
$\overline{RAS}$ to QSF Delay Time	t_{RQD}	—	100	—	120	—	150	ns	4
$\overline{RAS}$ to QSF (high) Delay Time	t_{RQH}	—	TBD	—	TBD	—	TBD	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	—	60	—	75	—	ns	
Serial Data Input to $\overline{RAS}$ Delay Time	t_{SZR}	—	10	—	10	—	10	ns	
Serial Output Buffer Turn-off Delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	75	ns	7
$\overline{RAS}$ to S_{out} (Low-Z) Delay Time	t_{RLZ}	5	—	10	—	10	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	60	—	ns	
Access Time from SC	t_{SCA}	—	30	—	40	—	50	ns	4
Serial Data-out Hold Time	t_{SOH}	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	25	—	ns	

Serial Read Cycle

Parameter	Symbol	HM534253-10		HM534253-12		HM534253-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	60	—	ns	
Access Time from SC	t_{SCA}	—	30	—	40	—	50	ns	4
Access Time from $\overline{SE}$	t_{SEA}	—	25	—	30	—	40	ns	4
Serial Data-out Hold Time	t_{SOH}	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{SE}$	t_{SEZ}	0	25	0	25	0	30	ns	7
Last SC to QSF Delay Time	t_{SQD}	—	TBD	—	TBD	—	TBD	ns	4

Serial Write Cycle

Parameter	Symbol	HM534253-10		HM534253-12		HM534253-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	60	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	25	—	ns	
Serial Write Enable Setup Time	t_{SWS}	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	t_{SWH}	30	—	35	—	50	—	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	—	0	—	0	—	ns	
Serial Write Disable Hold time	t_{SWIH}	30	—	35	—	50	—	ns	

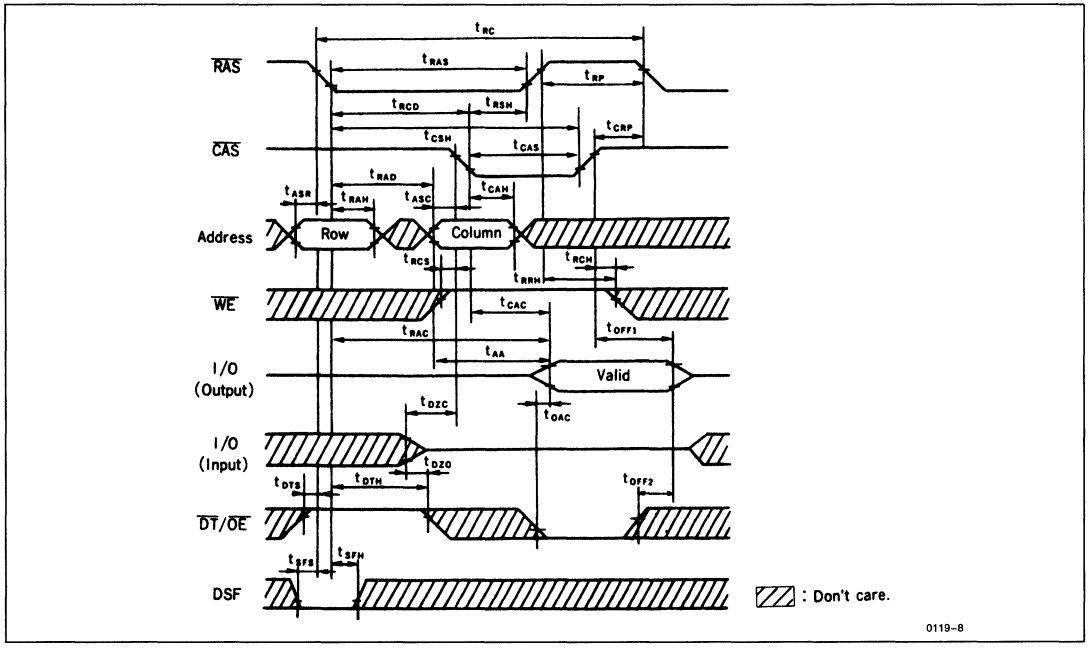
Flash Write Cycle

Parameter	Symbol	HM534253-10		HM534253-12		HM534253-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Flash Write Cycle Time	t_{RCFW}	230	—	265	—	310	—	ns	
$\overline{RAS}$ Pulse Width	t_{RCSFW}	140	—	165	—	200	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	20	—	ns	
$\overline{CAS}$ High Level Hold Time Referenced to $\overline{RAS}$	t_{CHHR}	20	—	25	—	30	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	20	—	ns	

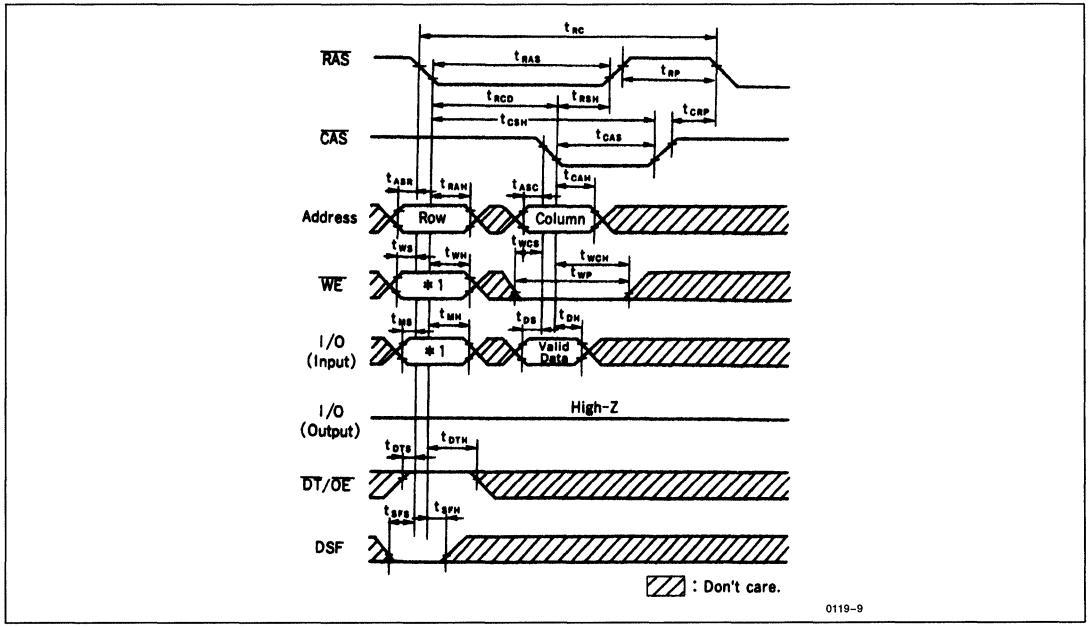
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
5. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
6. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
7. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition ($V_{OH} - 200$ mV, $V_{OL} + 200$ mV).
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
9. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-modify-write cycle; the data of the selected address is read out from a data out pin and input data is written into the selected address. In this case, impedance on I/O pins is controlled by $\overline{OE}$.
10. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles or to $\overline{WE}$ falling edge in delayed write or read-modify-write cycles.
11. After power-up, pause for 100 μs or more and execute at least 8 initialization cycles (normal memory cycles or refresh cycles), then start operation.
12. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.

■ TIMING WAVEFORMS

• Read Cycle

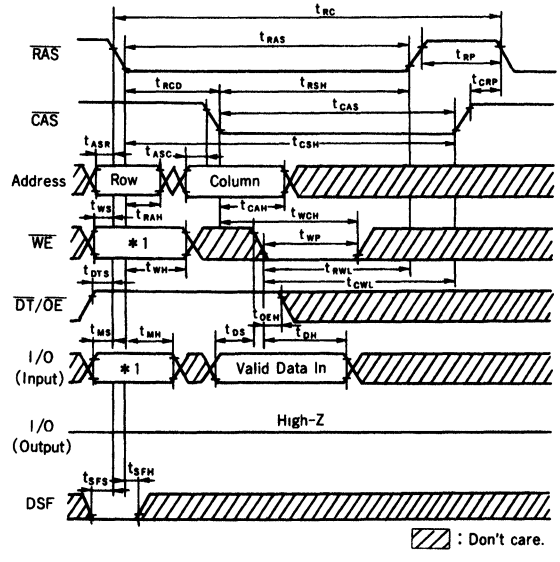


• Early Write Cycle



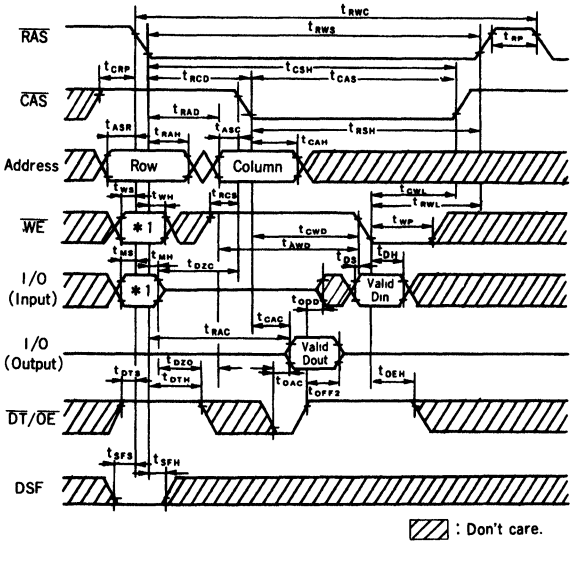
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Delayed Write Cycle**



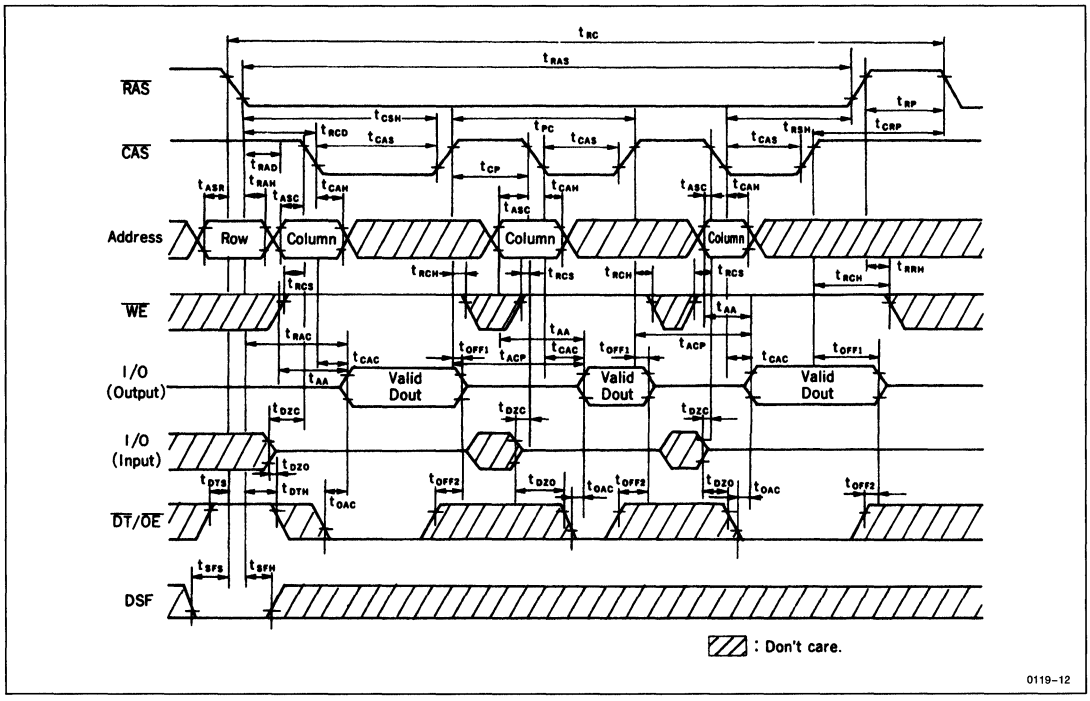
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Read-Modify-Write Cycle**

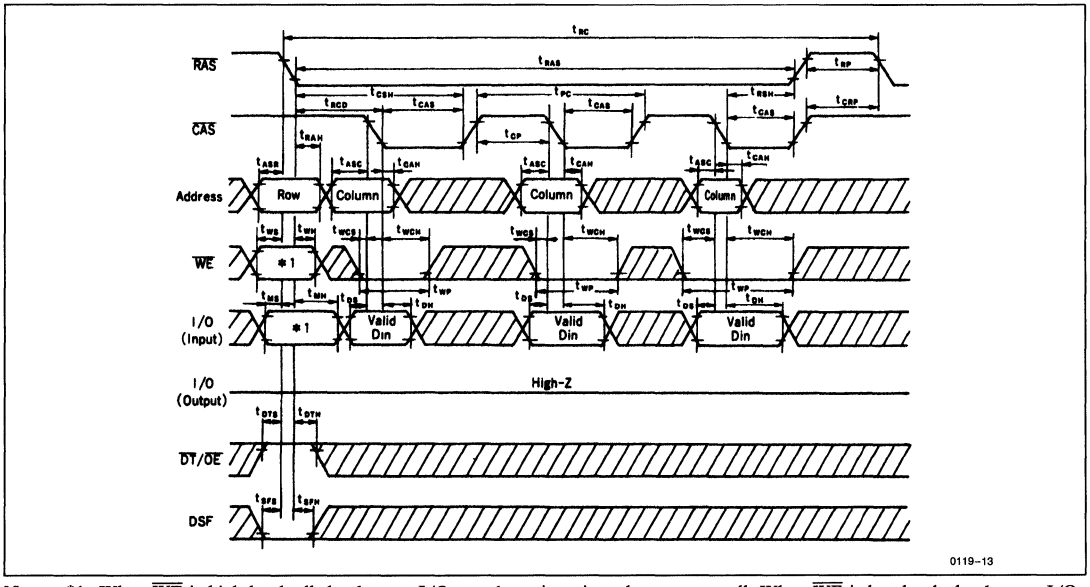


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Page Mode Read Cycle**

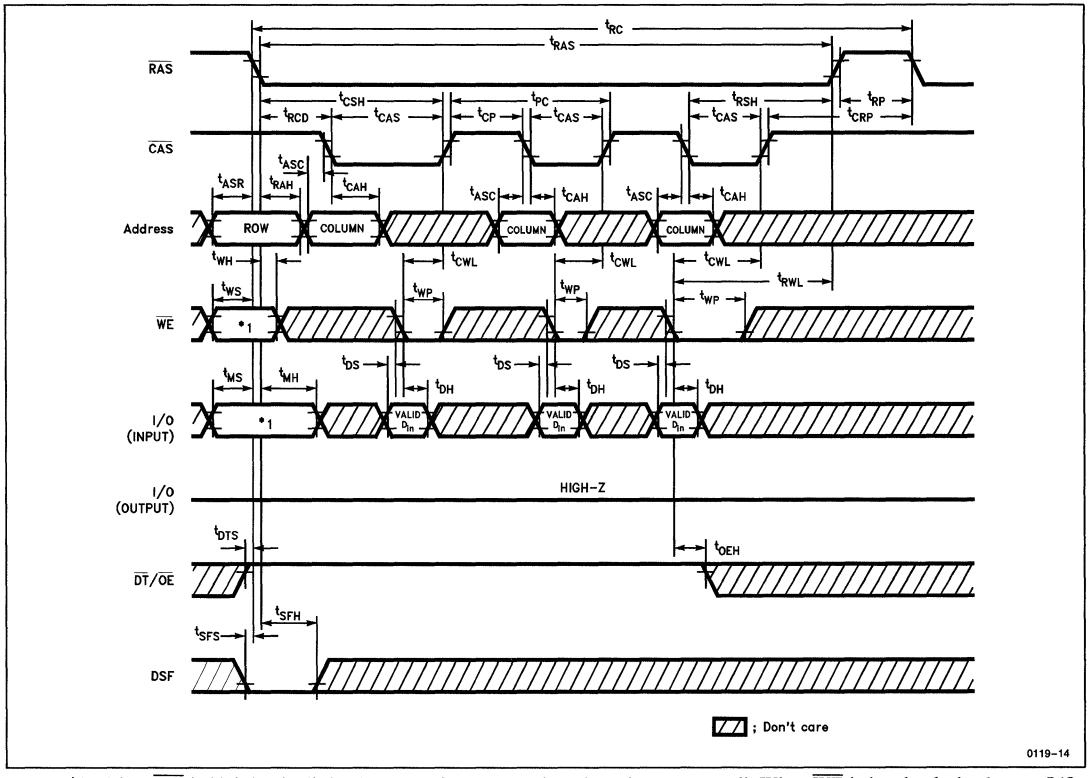


• **Page Mode Write Cycle (Early Write)**



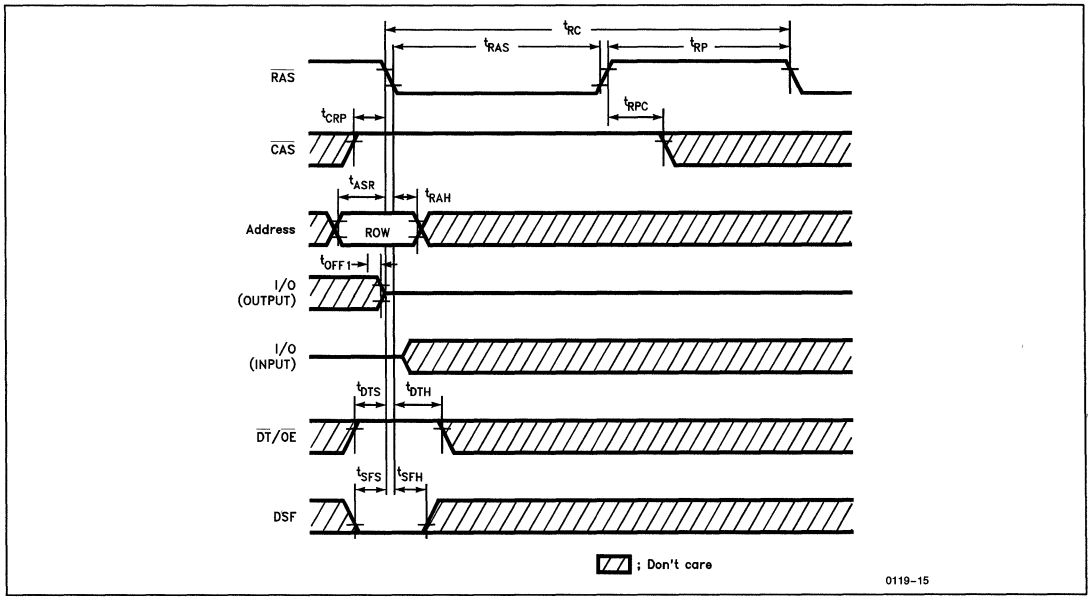
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• Page Mode Write Cycle (Delayed Write)

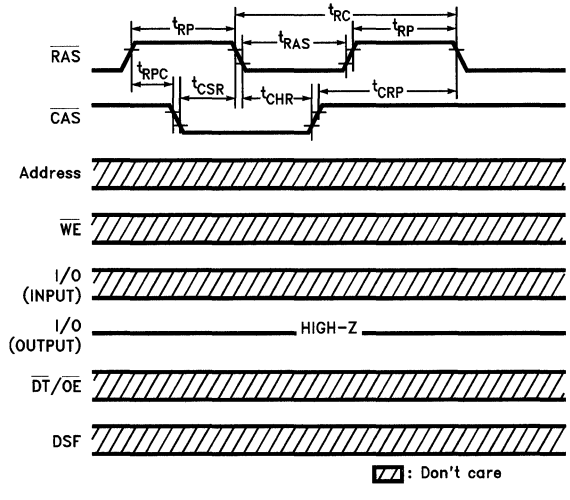


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

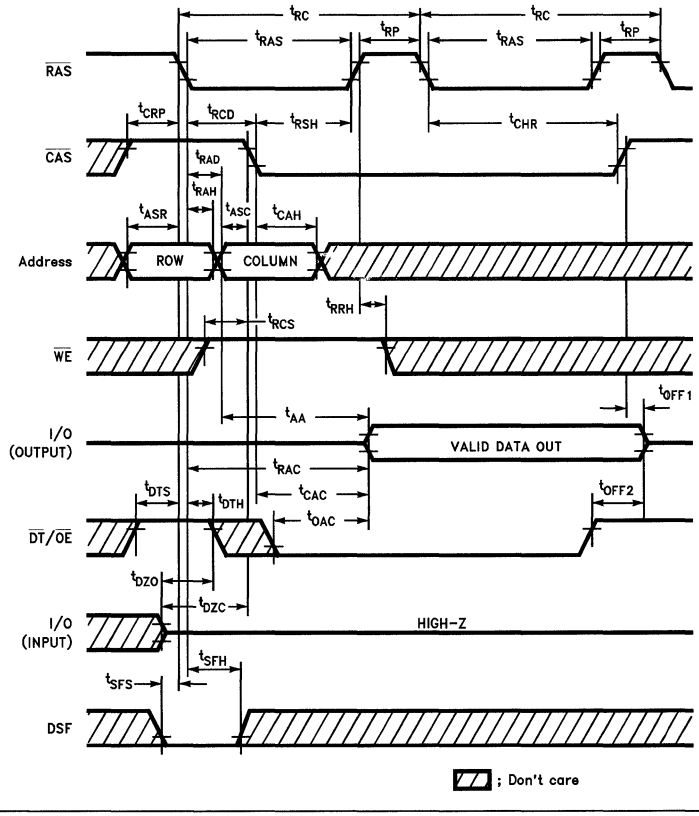
• $\overline{RAS}$ Only Refresh Cycle



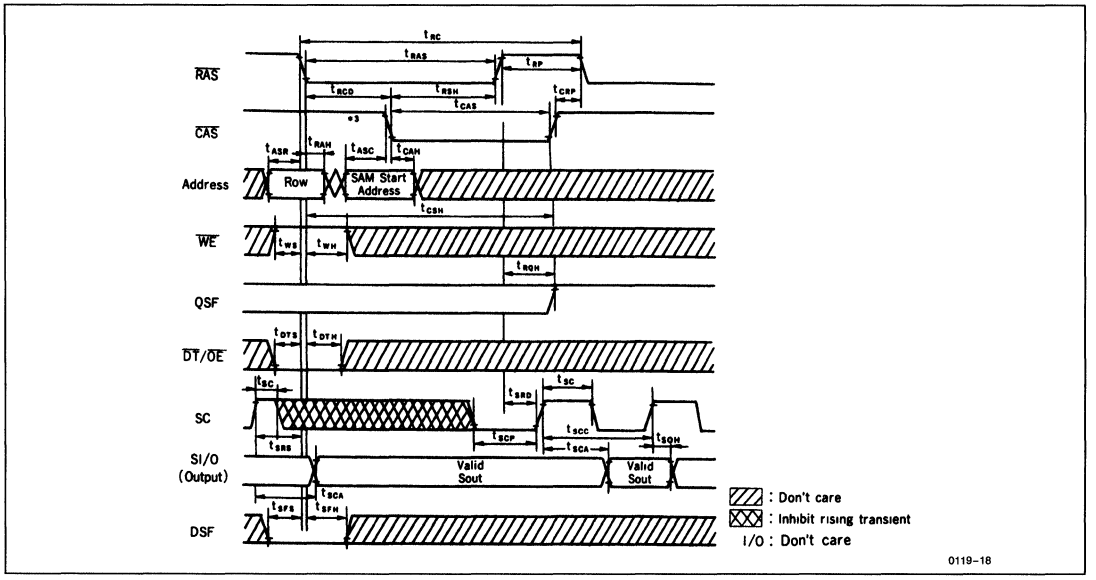
• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**



• **Hidden Refresh Cycle**

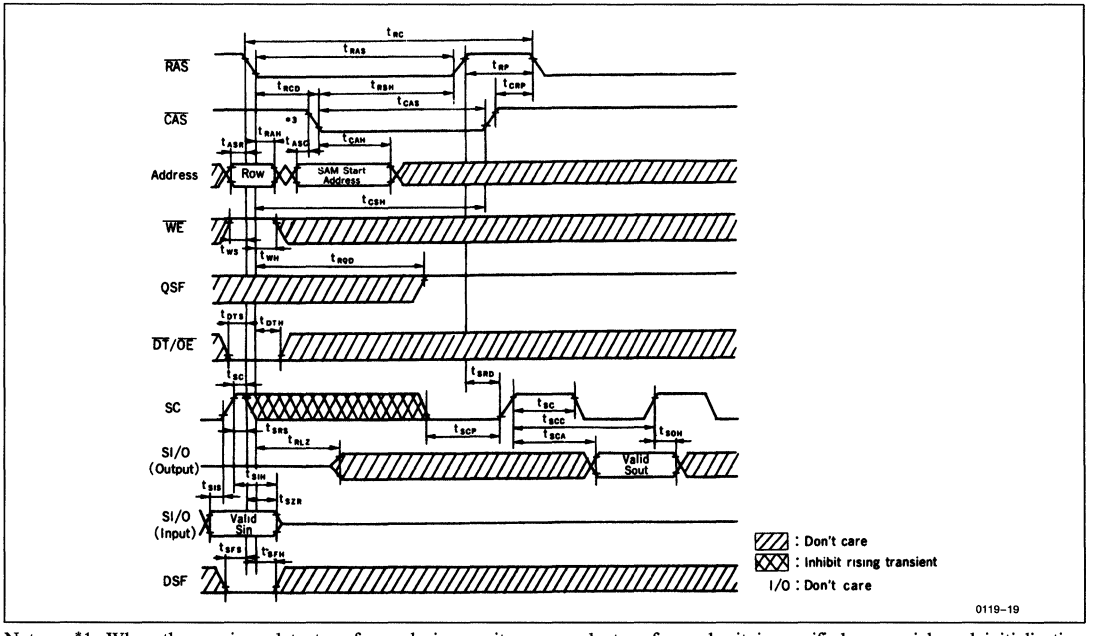


• Special Read Initialization Cycle (1)*1, *2



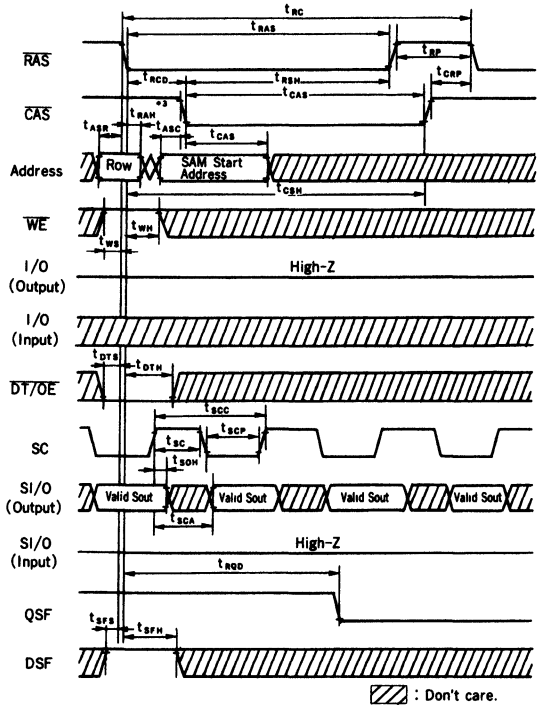
Notes: *1. When the previous data transfer cycle is a special read transfer cycle or special read initialization cycle, it is specified as special read initialization cycle (1).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance state.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• Special Read Initialization Cycle (2)*1, *2



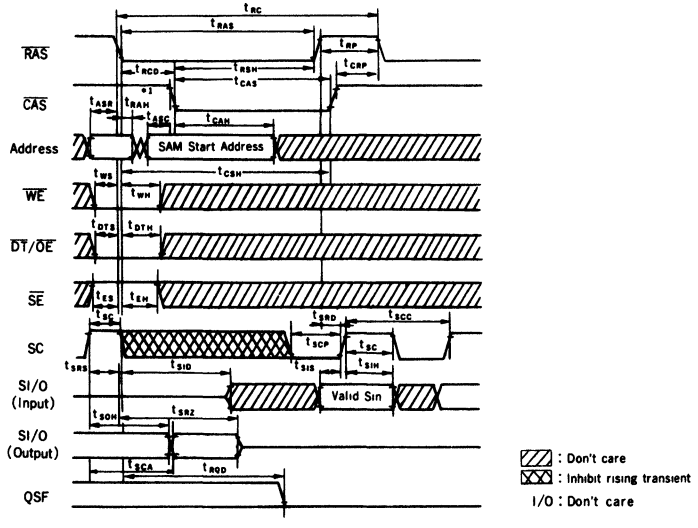
Notes: *1. When the previous data transfer cycle is a write or pseudo transfer cycle, it is specified as special read initialization cycle (2).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance state.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• Special Read Transfer Cycle*1, *2



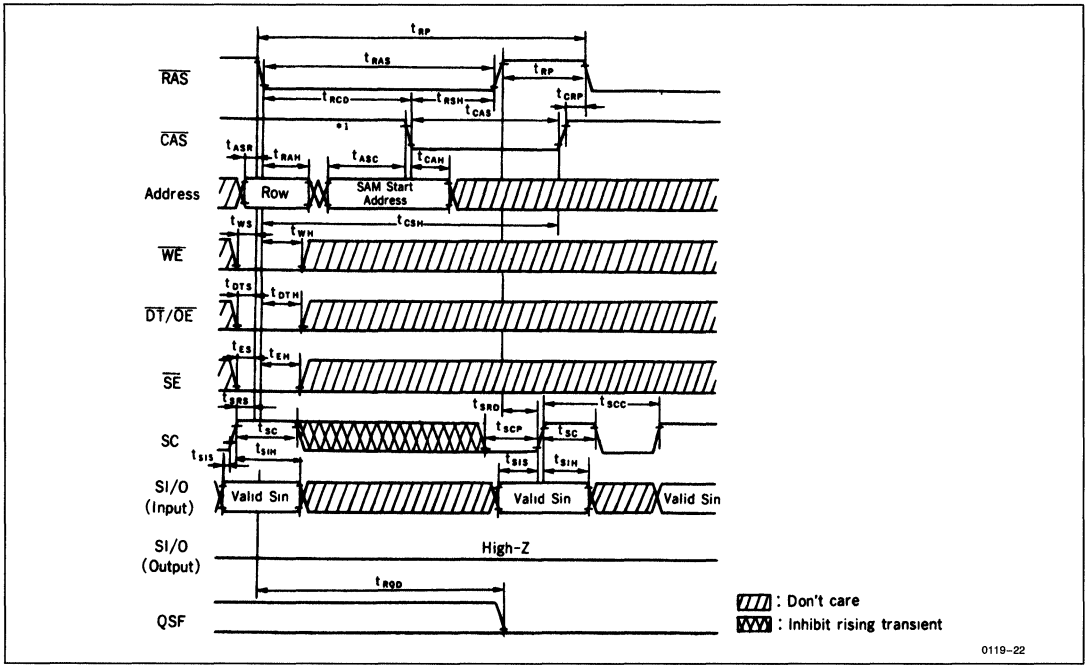
Notes: *1. When QSF in low level at the faling edge of RAS, the special read transfer cycle is not performed.
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance state.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• Pseudo Transfer Cycle



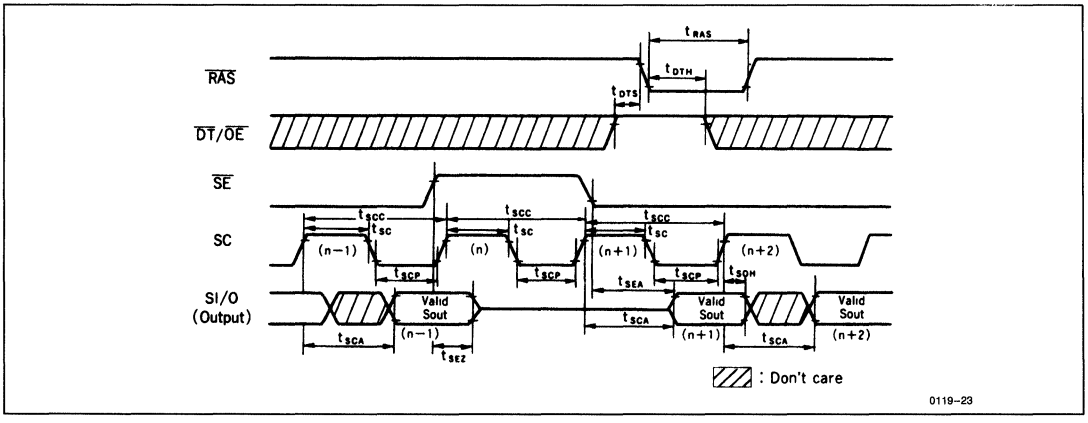
Note: *1. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• **Write Transfer Cycle**

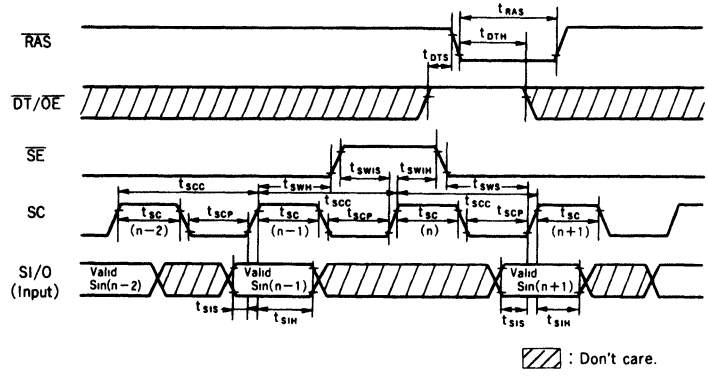


Note: *1. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• **Serial Read Cycle**

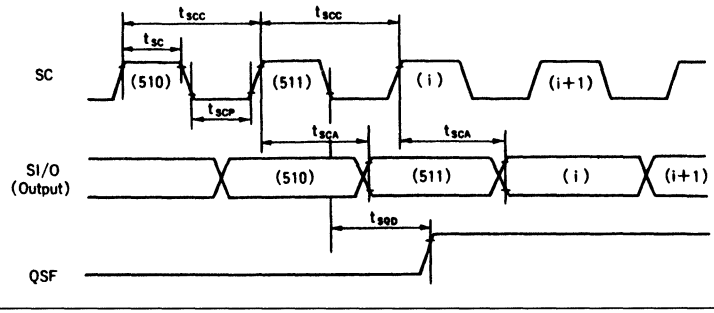


• **Serial Write Cycle**



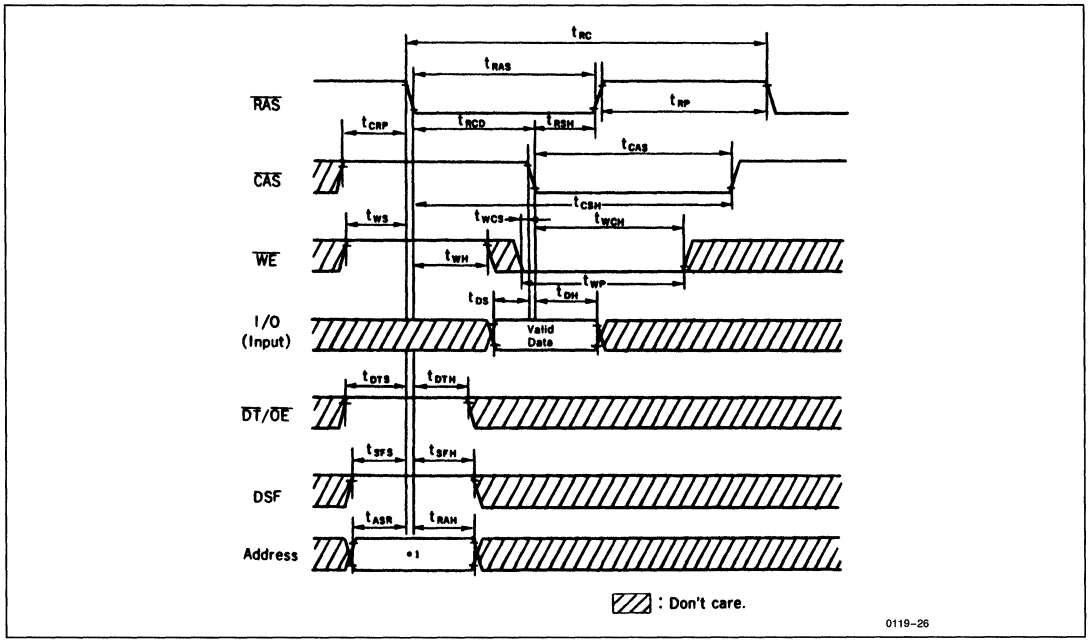
Notes: *1. When $\overline{SE}$ is high level in a serial write cycle, data is not written into SAM, however, the pointer is incremented.
*2. Address 0 is accessed next to addres 511.

• **Serial Read Cycle (Around Address 511 in SAM)**



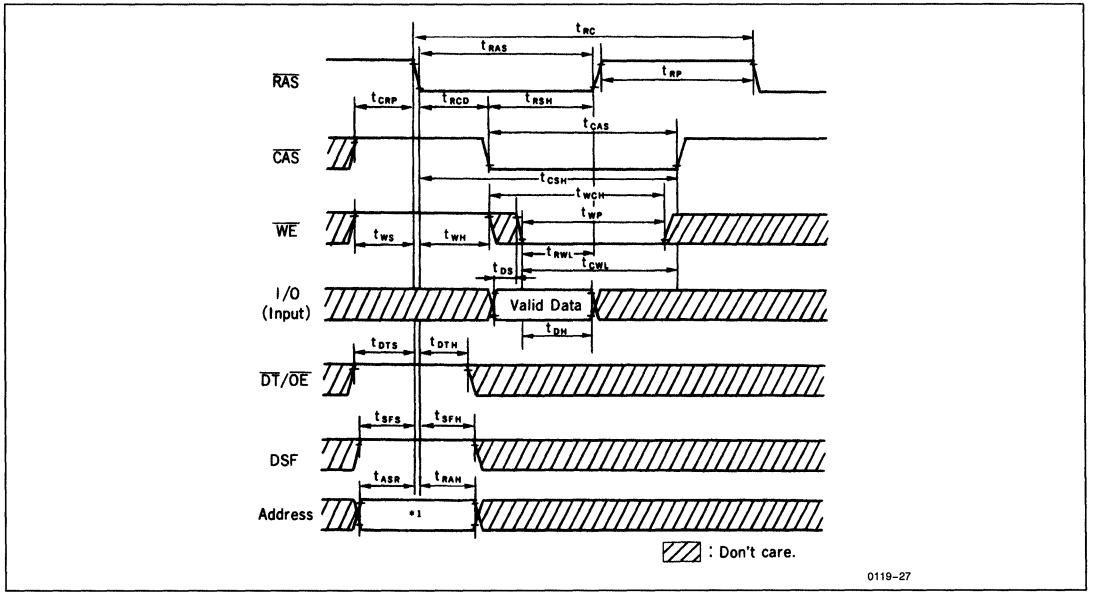
Note: *1. Address (i) is the SAM start address provided in the previous special read transfer cycle. When special read transfer cycle isn't executed (QSF remains in high level), address 0 is accessed next to address 511.

• **Color Register Set Cycle (Early Write)**



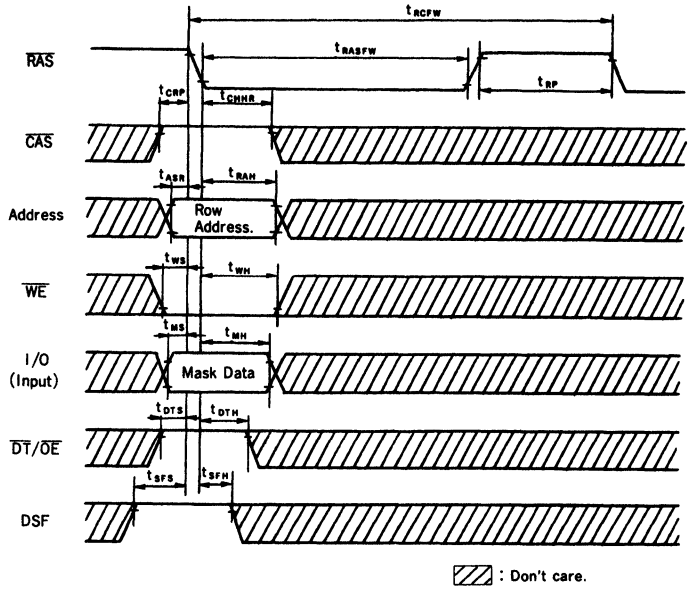
Note: *1. The level of address pin is don't care, but cannot be changed in this period.

• **Color Register Set Cycle (Delayed Write)**



Note: *1. The level of address pin is don't care, but cannot be changed in this period.

• **Flash Write Cycle**



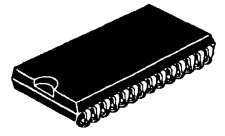
HM534253A Series — Preliminary

262,144-Word x 4-Bit Multiport CMOS Video RAM

■ DESCRIPTION

The HM534253A is a 1-Mbit multiport video RAM equipped with a 256k-word x 4-bit dynamic RAM and a 512-word x 4-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has a logic operation mode by internal logic-arithmetic unit and a write mask function. In addition, it has two modes to realize fast writing in RAM. Block write and flash write modes clear the data of 4-word x 4-bit and the data of one row (512-word x 4-bit) respectively in one cycle of RAM. And the HM534253A makes split transfer cycle possible by dividing SAM into two split buffers equipped with 256-word x 4-bit each. This cycle can transfer data to SAM which is not active, and enables a continuous serial access.

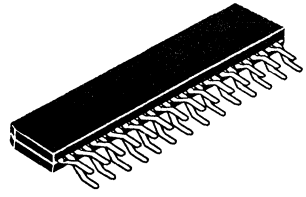
HM534253AJ Series



3DCP28D

(CP-28D)

HM534253AZ Series



3DZP28

(ZP-28)

■ FEATURES

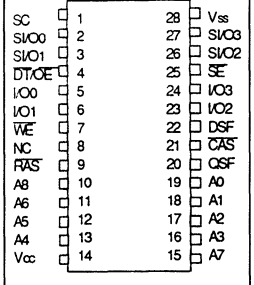
- Multiport Organization
  - Asynchronous and Simultaneous Operation of RAM and SAM Capability
  - RAM: 256k-word x 4-bit and SAM: 512-word x 4-bit
- Access Time
  - RAM ..... 80 ns/100 ns (max)
  - SAM ..... 25 ns/25 ns (max)
- Cycle Time
  - RAM ..... 150 ns/190 ns (min)
  - SAM ..... 30 ns/30 ns (min)
- Low Power
  - Active RAM ..... 360 mW (max)
  - SAM ..... 275 mW (max)
  - Standby ..... 38.5 mW (max)
- High-Speed Page Mode Capability
- Logic Operation Mode Capability
- Mask Write Mode Capability
- Bidirectional Data Transfer Cycle between RAM and SAM Capability
- Split Transfer Cycle Capability
- Block Write Mode Capability
- Flash Write Mode Capability
- 3 Variations of Refresh (8 ms/512 cycles)
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- TTL Compatible

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Inputs
I/O_0–I/O_3	RAM Port Data Inputs/Outputs
SI/O_0–SI/O_3	SAM Port Data Inputs/Outputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{DT/OE}$	Data Transfer/Output Enable
SC	Serial Clock
$\overline{SE}$	SAM Port Enable
DSF	Special Function Input Flag
QSF	Special Function Output Flag
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ PIN OUT

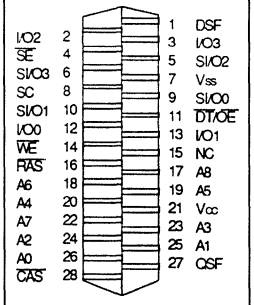
HM534253AJ Series



0086-1

(Top View)

HM534253AZ Series



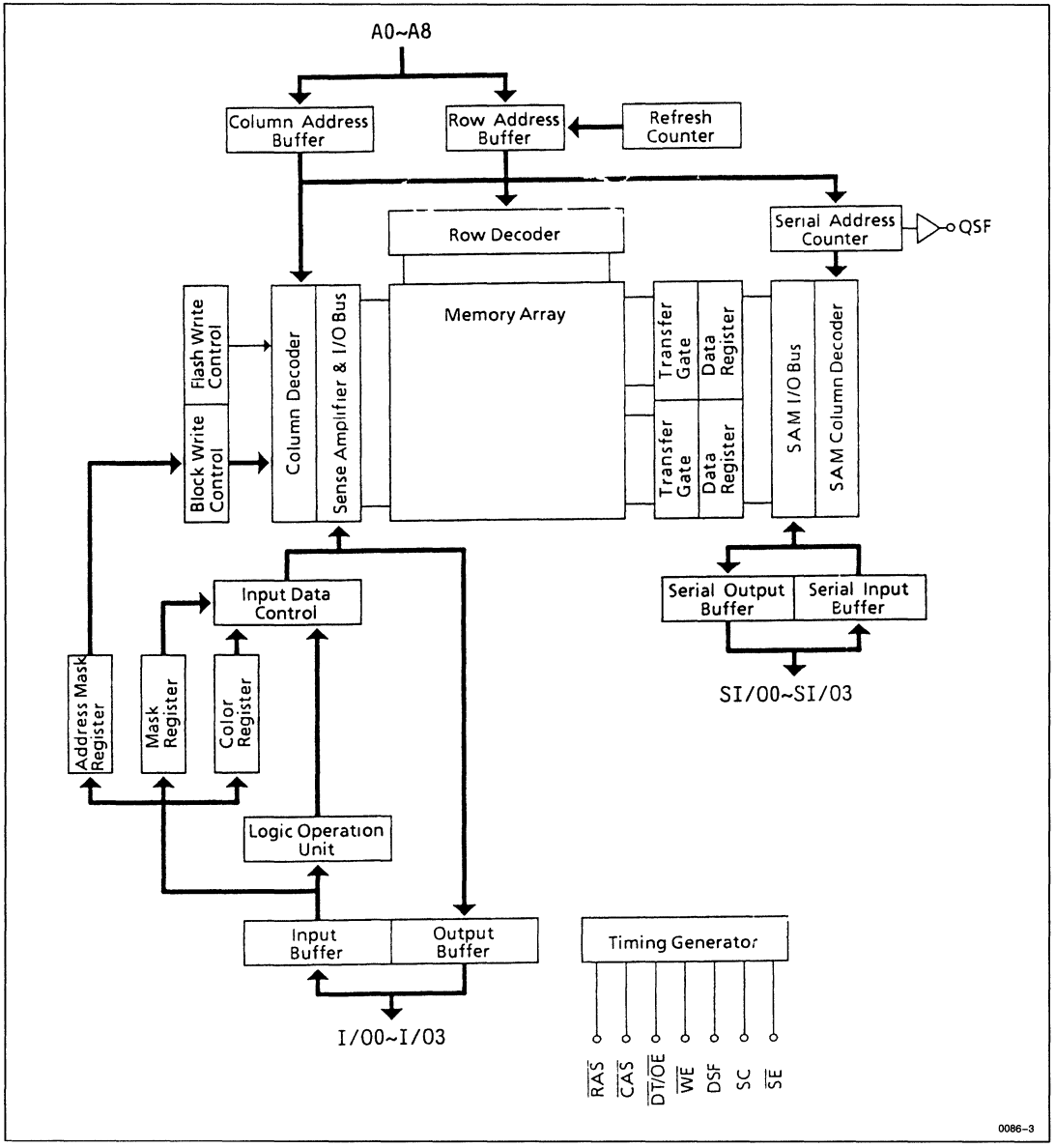
0086-2

(Bottom View)

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM534253AJ-8 HM534253AJ-10	80 ns 100 ns	400 mil 28-pin Plastic SOJ (CP-28D)
HM534253AZ-8 HM534253AZ-10	80 ns 100 ns	400 mil 28-pin Plastic ZIP (ZP-28)

■ BLOCK DIAGRAM



■ PIN FUNCTIONS

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of these signals determine the operation cycle of the HM534253A.

$\overline{CAS}$ (input pin): Column address and DSF signal are fetched into chip at the falling edge of $\overline{CAS}$, which determines the operation mode of HM534253A. $\overline{CAS}$ controls output impedance of I/O in RAM.

A_0–A_8 (input pins): Row address is determined by A_0–A_8 level at the falling edge of $\overline{RAS}$. Column address is determined by A_0–A_8 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM534253A turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O_0–I/O_3 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only to high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM. In block write cycle, they function as address mask data at the falling edge of $\overline{CAS}$.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is fetched into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not fetched into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O_0–SI/O_3 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

DSF (input pin): DSF is a special function data input flag pin. It is set to high at the falling edge of $\overline{RAS}$ when new functions such as color register read/write, split transfer, and flash write, are used. DSF is set to high at the falling edge of $\overline{CAS}$ when block write is executed.

QSF (output pin): QSF outputs data of address A8 in SAM. QSF is switched from low to high by accessing address 255 in SAM and from high to low by accessing 511 address in SAM.

• Table 1. Operation Cycles of the HM534253A

Input Level at the Falling Edge of $\overline{RAS}$					DSF at the Falling Edge of $\overline{CAS}$	Operation Mode
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SE}$	DSF		
L	X	L	X	X	—	Logic Operation Set/Reset
L	X	H	X	X	—	CBR Refresh
H	L	L	L	L	X	Write Transfer
H	L	L	H	L	X	Pseudo Transfer
H	L	L	X	H	X	Split Write Transfer
H	L	H	X	L	X	Read Transfer
H	L	H	X	H	X	Split Read Transfer
H	H	L	X	L	L	Read/Mask Write
H	H	L	X	L	H	Mask Block Write
H	H	L	X	H	X	Flash Write
H	H	H	X	L	L	Read/Write
H	H	H	X	L	H	Block Write
H	H	H	X	H	X	Color Register Read/Write

Note: X; Don't care.

■ OPERATION OF HM534253A

• RAM Read Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF low at the falling edge of $\overline{RAS}$, DSF low at the falling edge of $\overline{CAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

• RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write)

($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF low at the falling edge of $\overline{RAS}$, DSF low at the falling edge of ($\overline{CAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after driving $\overline{RAS}$ low, a write cycle is executed and I/O data is written in the selected addresses. When all 4 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes in high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables read/write at the same address in one cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is retained. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode, the mask data is retained during the page access.

• High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF low at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle. In this cycle, read, write, and block write cycles can be mixed. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 μs).

• Color Register Set/Read Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ high and DSF high at the falling edge of $\overline{RAS}$)

In color register set cycle, color data is set to the internal color register used in flash write cycle or block write cycle. 4 bits of internal color register are provided at each I/O. This register is composed of static circuits, so once it is set, it retains the data until reset. Color register set cycle is just as same as the usual write cycle except that DSF is set high at the falling edge of $\overline{RAS}$, and read, early write and delayed write cycle can be executed. In this cycle, HM534253A refreshes the row address fetched at the falling edge of $\overline{RAS}$.

• Flash Write Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ low and DSF high at the falling edge of $\overline{RAS}$)

In a flash write cycle, a row of data (512-word x 4-bit) is cleared to 0 or 1 at each I/O according to the data of color register mentioned before. It is also necessary to mask I/O in this cycle. When $\overline{CAS}$ and $\overline{DT}/\overline{OE}$ is set high, $\overline{WE}$ is low, and DSF is high at the falling edge of $\overline{RAS}$, this cycle starts. Then, the row address to clear is given to row address and mask data is given to I/O. Mask data is as same as that of a RAM write cycle. High I/O is cleared, low I/O is not cleared and the internal data is retained. Cycle time is the same as those of RAM read/write cycles, so all bits can be cleared in 1/512 of the usual cycle time. (See figure 1.) If this cycle is executed in logic operation mode described later, the logic operation mode is reset only in the cycle and masked data in this cycle is written.

• Block Write Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high and DSF low at the falling edge of $\overline{RAS}$, DSF high at the falling edge of $\overline{CAS}$)

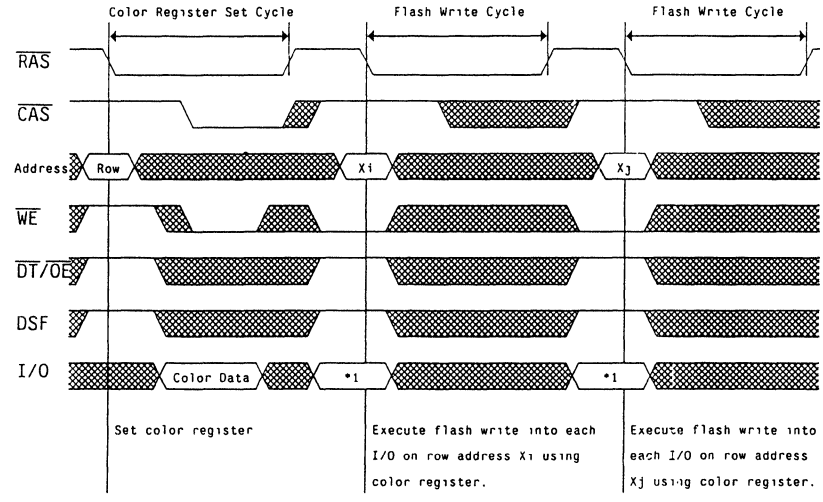
In a block write cycle, 4 columns of data (4-word x 4-bit) is cleared to 0 or 1 at each I/O according to the data of color register. Column addresses A0 and A1 are disregarded. The data on I/Os and addresses can be masked. I/O level at the falling edge of $\overline{CAS}$ determines the address to be cleared. (See figure 2.) If this cycle is executed in logic operation mode described later, the logic operation mode is reset only in the cycle and masked data in this cycle is written.

- Normal Mode Block Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

The data on 4 I/Os are all cleared when $\overline{WE}$ is high at the falling edge of $\overline{RAS}$.

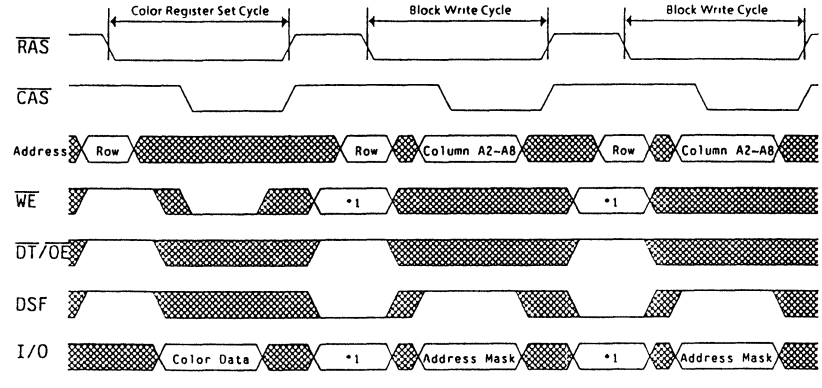
- Mask Block Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, HM534253A starts mask block write mode to clear the data on an optional I/O. The mask data is the same as that of a RAM write cycle, High I/O is cleared, low I/O is not cleared and the internal data is retained. The mask data is available in the $\overline{RAS}$ cycle. In page mode block write cycle, the mask data is retained during the page access.



Note: *1. I/O Mask Data
Low: Mask
High: Non Mask

Figure 1. Use of Flash Write



Note: *1

$\overline{WE}$	I/O	Mode
Low	I/O Mask Data	Mask
High	Don't Care	Non Mask

I/O Mask Data
Low: Mask
High: Non Mask

Address Mask Data

I/O_0	Column0 (A0 = 0, A1 = 0) Mask Data	Low: Mask
I/O_1	Column1 (A0 = 1, A1 = 0) Mask Data	
I/O_2	Column2 (A0 = 0, A1 = 1) Mask Data	High: Non Mask
I/O_3	Column3 (A0 = 1, A1 = 1) Mask Data	

Figure 2. Use of Block Write

• Transfer Operation

The HM534253A provides the read transfer cycle, split read transfer cycle, pseudo transfer cycle, write transfer cycle and split write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{CAS}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle).

Read transfer cycle and split read transfer cycle: RAM to SAM

Write transfer cycle and split write transfer cycle: SAM to RAM

(2) Determine SI/O state (except for split read transfer cycle and split write transfer cycle).

Read transfer cycle: SI/O output

Pseudo transfer cycle and write transfer cycle: SI/O input

(3) Determine first SAM address to access after transferring at column address (SAM start address).

SAM start address must be determined by read transfer cycle or pseudo transfer cycle (split transfer cycle isn't available) before SAM access, after power on, and determined for each transfer cycle.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high and DSF low at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high and DSF low at the falling edge of $\overline{RAS}$. The row address data (512 x 4-bit) determined by this cycle is transferred to SAM data register synchronously at the rising edge of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address determined by column address. In read transfer cycle, $\overline{DT}/\overline{OE}$ must be risen to transfer data from RAM to SAM.

This cycle can access SAM even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge and t_{SDH} (min) specified between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge must be satisfied. (See figure 3.)

When read transfer cycle is executed, SI/O becomes output state by first SAM access. Input must be set high impedance before t_{SZS} (min) of the first SAM access to avoid data contention.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, $\overline{SE}$ high and DSF low at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle switchs SI/O to input state and set SAM start address without data transfer to RAM.

This cycle starts when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ low. $\overline{WE}$ low, $\overline{SE}$ high and DSF low at the falling edge of $\overline{RAS}$. Data should be input to SI/O later than t_{SID} (min) after $\overline{RAS}$ becomes low to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC must not be risen.

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, $\overline{SE}$ low and DSF low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address for serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC must not be risen. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by write transfer cycle. However, the address to write data must be the same as that of the read transfer cycle or the split read transfer cycle (row address AX8).

Split Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high and DSF high at the falling edge of RAS)

To execute a continuous serial read by real time read transfer, HM534253A must satisfy SC and $\overline{DT}/\overline{OE}$ timings and requires an external circuit to detect SAM last address. Split read transfer cycle makes it possible to execute a continuous serial read without the above timing limitation. Figure 4 shows the block diagram for a split transfer. SAM data register (DR) consists of 2 split buffers, whose organizations are 256-word x 4-bit each. Let us suppose that data is read from upper data register DR1 (The row address AX8 is 0

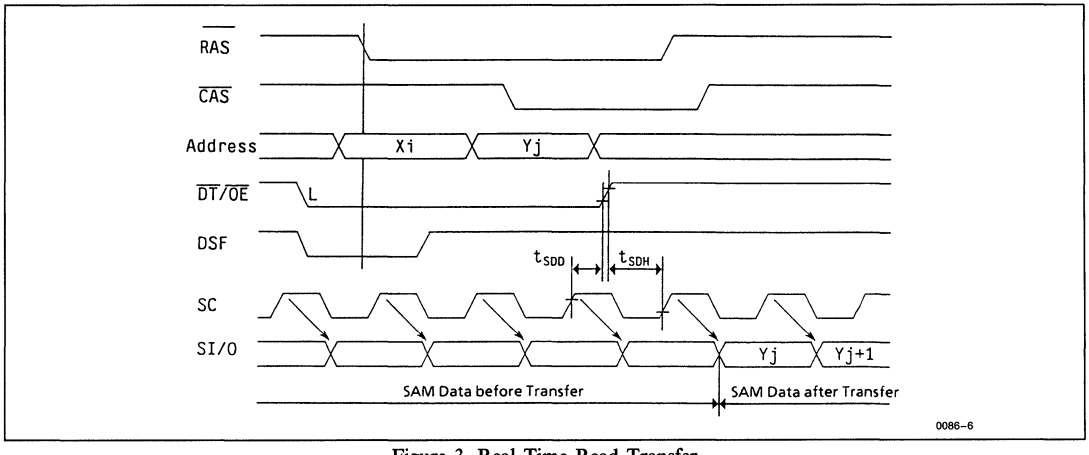


Figure 3. Real Time Read Transfer

and SAM address A8 is 1). When split read transfer is executed setting row address AX8 0 and SAM start addresses A0 to A7, 256-word x 4-bit data are transferred from RAM to the lower data register DR0 (SAM address A8 is 0) automatically. After data are read from data register DR1, data start to be read from SAM start addresses of data register DR0. If the next split read transfer isn't executed while data are read from data register DR0, data start to be read from SAM start address 0 of DR1 after data are read from data register DR0. If split read transfer is executed setting row address AX8 1 and SAM start addresses A0 to A7 while data are read from data register DR1, 256-word x 4-bit data are transferred to data register DR2. After data are read from data register DR1, data start to be read from SAM start addresses of data register DR2. If the next split read transfer isn't executed while data are read from data register DR2, data start to be read from SAM start address 0 of data register DR3 after data are read from data register DR2. In this time, SAM data is the one transferred to data register DR3 finally while row address AX8 is 1. In split read data transfer, the SAM start address A8 is automatically set in the data register which isn't used.

The data on SAM address A8, which will be accessed next, outputs to QSF, QSF is switched from low to high by accessing SAM last address 255 and from high to low by accessing address 511.

Split read transfer cycle is set when $\overline{CAS}$ is high, $\overline{DT/OE}$ is low, $\overline{WE}$ is high and DSF is high at the falling edge of $\overline{RAS}$. The cycle can be executed asynchronously with SC. However, HM534253A must be satisfied t_{STS} (min) timing specified between SC rising and $\overline{RAS}$ falling. SAM start address must be accessed, satisfying t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings specified between $\overline{RAS}$ or $\overline{CAS}$ falling and column address. (See figure 5.)

In split read transfer, SI/O isn't switched to output state. Therefore, read transfer must be executed to switch SI/O to output state when the previous transfer cycle is pseudo transfer or write transfer cycle.

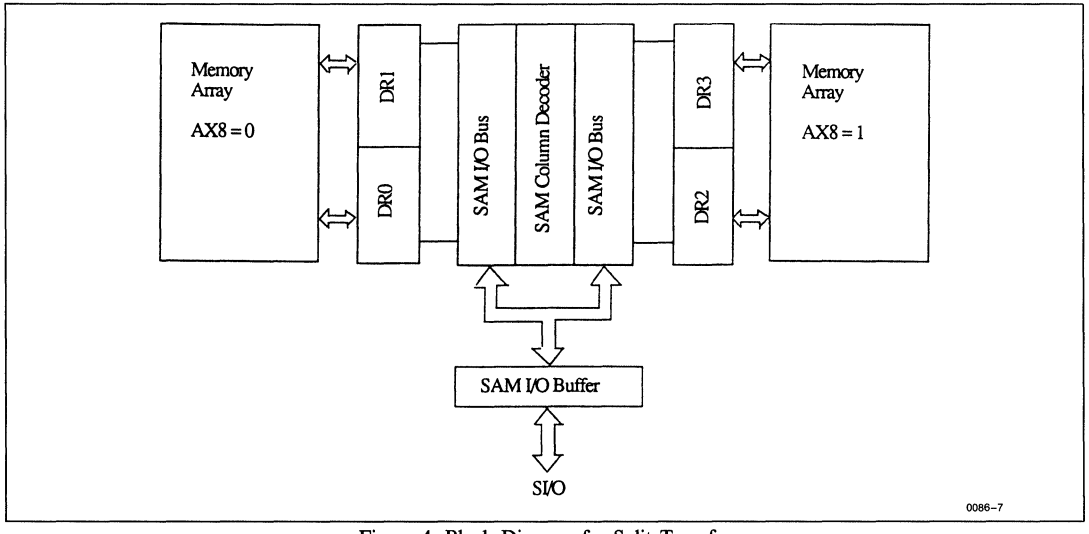


Figure 4. Block Diagram for Split Transfer

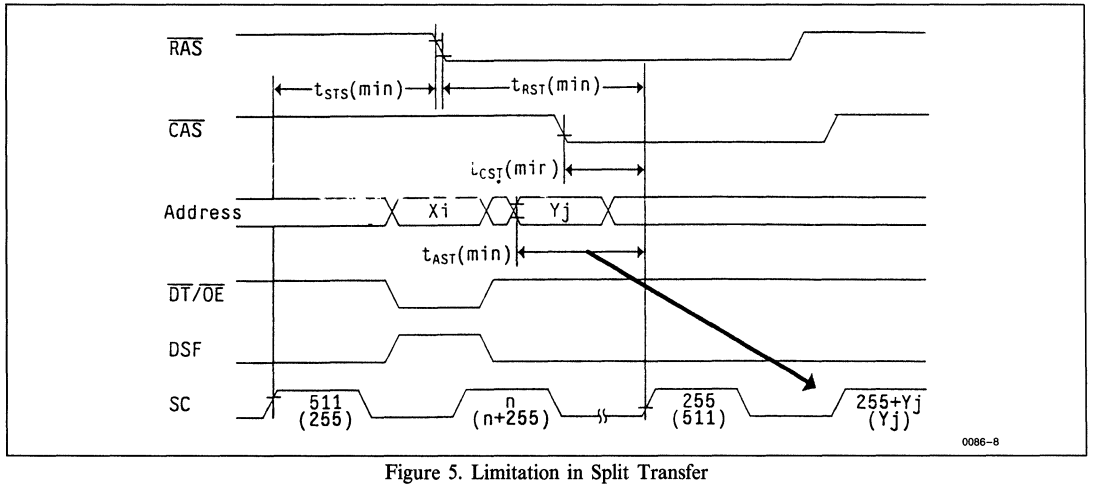


Figure 5. Limitation in Split Transfer

Split Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and DSF high at the falling edge of $\overline{RAS}$).

A continuous serial write cannot be executed because accessing SAM is inhibited during $\overline{RAS}$ low in write transfer. Split write transfer cycle makes it possible. In this cycle, t_{STS} (min), t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings must be satisfied like split read transfer cycle. And it is impossible to switch SI/O to input state in this cycle. If SI/O is in output state, pseudo transfer cycle should be executed to switch SI/O into input state. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by split write transfer cycle. However, pseudo transfer cycle must be executed before split write transfer cycle. And the MSB of row address (AX8) to write data must be the same as that of the read transfer cycle or the split read transfer cycle.

• SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When $\overline{SE}$ is set high, SI/O becomes high impedance, and the internal pointer is incremented by the SC rising. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is fetched into data register at the SC rising edge like in the serial read cycle. If SE is high, SI/O data isn't fetched into data register. Internal pointer is incremented by the SC rising, so SE high can be used as mask data for SAM. After indicating the last address (address 511), the internal pointer indicates address 0 at the next access.

• Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is executed by accessing all 512 row addresses within 8 ms. There are three refresh cycles: (1) $\overline{RAS}$ only refresh cycle, (2) $\overline{CAS}$ before $\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required when all row addresses are accessed within 8 ms.

(1) $\overline{RAS}$ Only Refresh Cycle: $\overline{RAS}$ only refresh cycle is executed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high after inputting the row address (= refresh address) from external circuits. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ must be high at the falling edge of $\overline{RAS}$.

(2) CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.

To distinguish this cycle from logic operation set/reset cycle, $\overline{WE}$ must be high at the falling edge of $\overline{RAS}$.

(3) Hidden Refresh Cycle: Hidden refresh cycle executes CBR refresh with the data output by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register and selector), organized as fully static circuitry, require no refresh.

• Logic Operation Mode

The HM534253A supports logic operation capability on RAM port. It executes logic operation between the memory cell data and external input data in logic operation mode write cycle, and writes the result into the memory cell (read-modify-write). This function realizes high speed raster operations and simplifies peripheral circuits for raster operations.

Logic Operation Set/Reset Cycle ($\overline{CAS}$ low and $\overline{WE}$ low at the falling edge of $\overline{RAS}$).

In logic operation set/reset cycle, the following operations are executed at the same time; 1. Selection of logic operations and logic operation mode set/reset, 2. Mask data programming, 3. CBR refresh.

Figure 6 shows the timing for logic operation set/reset cycle. This cycle starts when $\overline{CAS}$ and $\overline{WE}$ are low at the falling edge of $\overline{RAS}$. In this cycle, logic operation codes and mask data are programmed by row address and I/O pin respectively at the falling edge of $\overline{RAS}$. When write cycle is executed after this cycle, the logic operation write cycle starts. In the logic operation mode, the specification of cycle time is longer than that of normal mode because read-modify-write cycle, which writes the operation result of external data and memory cell data into memory cell, is executed internally. In this cycle, logic operation codes and mask data programmed are available until reprogrammed. Mask data is available only for one $\overline{RAS}$ cycle, in mask write cycle, mask block write cycle and flash write cycle. Here, the mask data programmed in mask write cycle, mask block write cycle and flash write cycle is named as "temporary mask data" and the one programmed in logic operation set/reset cycle is named as "mask data".

- Selection of Logic Operations and Logic Operation Mode Set/Reset

Table 2 shows the logic operations. One operation is selected among sixteen ones by combinations of A0–A3 levels at the falling edge of $\overline{RAS}$. (A4-A8 are Don't care.) Logic operation codes (A3, A2, A1, A0) = (0,1,0,1)(THROUGH) resets the logic operation mode. When write cycle is executed after that, normal write cycle starts. However, even in this case, mask data is still available. I/O must be at high level at the falling edge of $\overline{RAS}$ in logic operation set/reset cycle when mask data is not used.

• Mask Data Programming

High/low level of I/O at the falling edge of $\overline{RAS}$ functions as mask data. When I/O is high, the data is written in write cycle. When I/O is low, the input data is masked and the same memory cell data remains. Mask data, programmed in this cycle, is available until reprogrammed. It is advantageous when the same mask data continues.

Also, temporary mask data can be programmed by falling $\overline{WE}$ at the falling edge of $\overline{RAS}$ in logic operation mode cycle, after mask data is programmed. The temporary mask data is available only for one cycle.

Logic operation is reset during temporary mask write cycle. It means that external input data is written into I/O whose temporary mask data is 1. (See figure 7.) These functions are useful when RAM port is divided into frame buffer area and data area, as they save the need to reprogram logic operation codes and mask them.

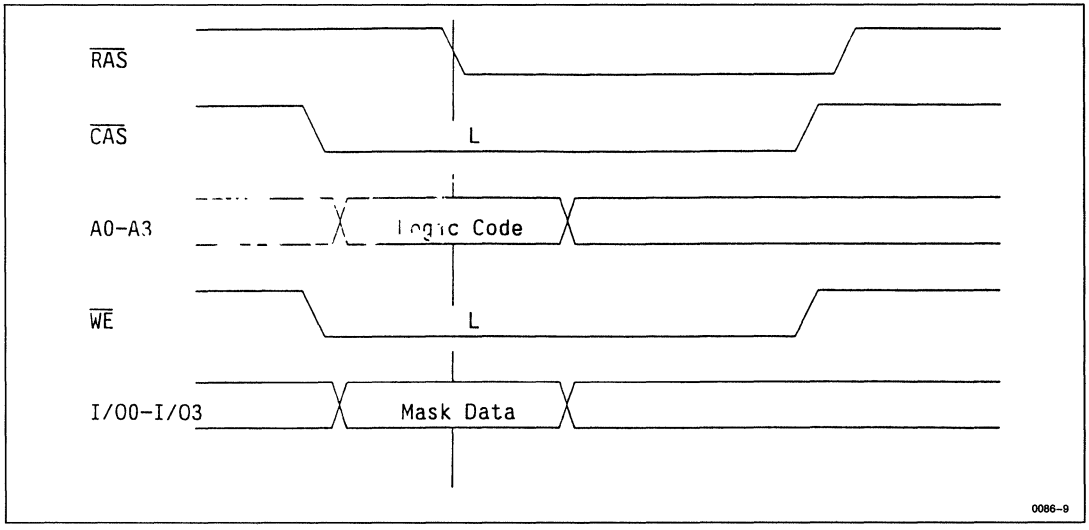


Figure 6. Logic Operation Set/Reset

• Table 2. Logic Code

Logic Code				Symbol	Write Data	Note
A3	A2	A1	A0			
0	0	0	0	ZERO	0	Logic Operation Mode Set
0	0	0	1	AND1	Di•Mi	
0	0	1	0	AND2	$\overline{Di}$•Mi	
0	0	1	1	—	Mi	
0	1	0	0	AND3	Di•$\overline{Mi}$	
0	1	0	1	THROUGH	Di	Logic Operation Mode Reset
0	1	1	0	EOR	$\overline{Di}$•Mi + Di•$\overline{Mi}$	Logic Operation Mode Set
0	1	1	1	OR1	Di + Mi	
1	0	0	0	NOR	$\overline{Di}$•$\overline{Mi}$	
1	0	0	1	ENOR	Di•Mi + $\overline{Di}$•$\overline{Mi}$	
1	0	1	0	INV1	$\overline{Di}$	
1	0	1	1	OR2	$\overline{Di}$ + Mi	
1	1	0	0	INV2	$\overline{Mi}$	
1	1	0	1	OR3	Di + $\overline{Mi}$	
1	1	1	0	NAND	$\overline{Di}$ + $\overline{Mi}$	
1	1	1	1	ONE	1	

Notes: Di: External Data-in.
Mi: The data of the memory cell.

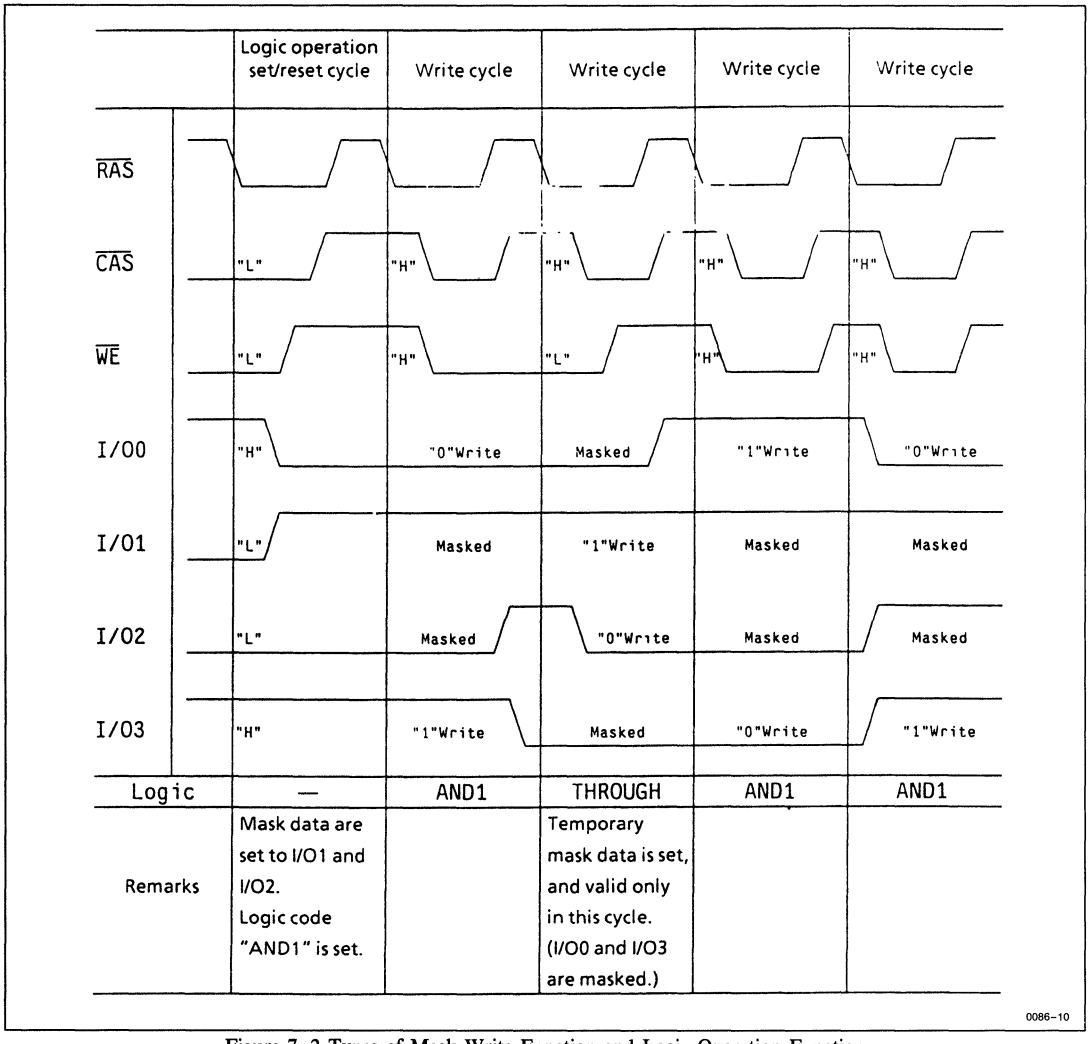


Figure 7. 2 Types of Mask Write Function and Logic Operation Function

Logic Operation Mode Write Cycle (Early Write, Delayed Write and Page Mode)

Write cycle after logic operation set cycle is logic operation mode write cycle. However, this mode is reset in block write, mask block write, flash write, and mask write cycle. In logic operation mode write cycle, the following read-modify-write operation is executed internally.

(1) Reading memory cell data in given address into internal bus.

(2) Executing operation between the data given in I/O pin and memory cell data.

(3) Writing the result of (2) into address given by (1).

Figure 8 shows the sequence of raster operation. Raster operation which needs 3 cycles (destination read, operation and destination write) in normal mode can be executed in one write cycle of logic operation mode. It makes raster operation faster and simplifies peripheral hardware for raster operation.

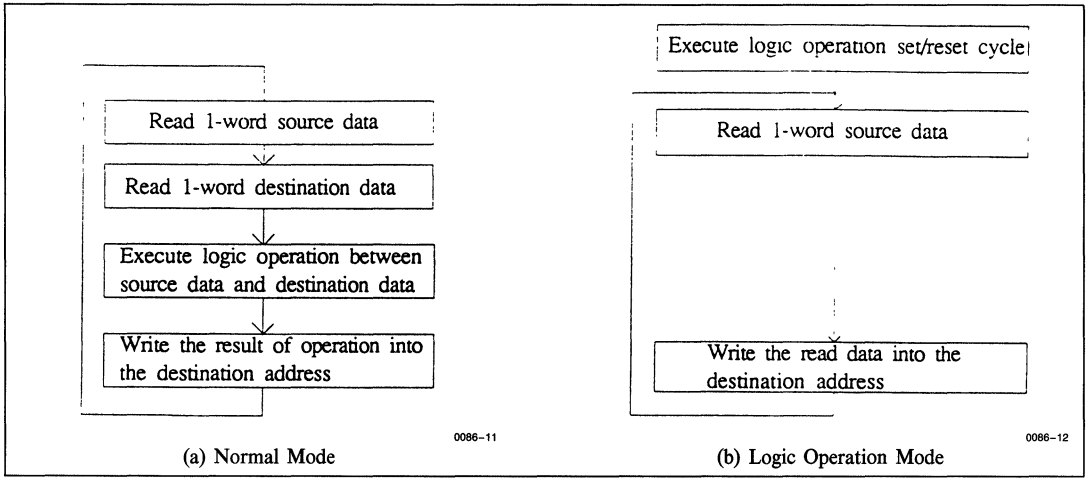


Figure 8. Sequence of Raster Operation

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Note
Terminal Voltage	V_T	−1.0 to +7.0	V	1
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V	1
Power Dissipation	P_T	1.0	W	
Operating Temperature	T_{opr}	0 to +70	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

Note: 1. Relative to V_{SS}.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−0.5	—	0.8	V	1, 2

Notes: 1. All voltages referenced to V_{SS}.
2. −3.0V for pulse width ≤ 10 ns.

• **DC Electrical Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM534253A-8		HM534253A-10		Unit	Test Conditions	
		Min	Max	Min	Max		RAM Port	SAM Port
Operating Current	I_{CC1}	—	65	—	50	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	$SC = V_{IL}$, $\overline{SE} = V_{IH}$
	I_{CC7}	—	115	—	100	mA		$\overline{SE} = V_{IL}$, SC Cycling t_{SOC} = Min
Standby Current	I_{CC2}	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	$SC = V_{IL}$, $\overline{SE} = V_{IH}$
	I_{CC8}	—	50	—	50	mA		$\overline{SE} = V_{IL}$, SC Cycling t_{SOC} = Min
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	65	—	50	mA	$\overline{RAS}$ Cycling $\overline{CAS} = V_{IH}$ t_{RC} = Min	$SC = V_{IL}$, $\overline{SE} = V_{IH}$
	I_{CC9}	—	115	—	100	mA		$\overline{SE} = V_{IL}$, SC Cycling t_{SOC} = Min
Page Mode Current	I_{CC4}	—	70	—	65	mA	$\overline{CAS}$ Cycling $\overline{RAS} = V_{IL}$ t_{PC} = Min	$SC = V_{IL}$, $\overline{SE} = V_{IH}$
	I_{CC10}	—	120	—	115	mA		$\overline{SE} = V_{IL}$, SC Cycling t_{SOC} = Min
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC5}	—	55	—	40	mA	$\overline{RAS}$ Cycling t_{RC} = Min	$SC = V_{IL}$, $\overline{SE} = V_{IH}$
	I_{CC11}	—	105	—	90	mA		$\overline{SE} = V_{IL}$, SC Cycling t_{SOC} = Min
Data Transfer Current	I_{CC6}	—	75	—	60	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	$SC = V_{IL}$, $\overline{SE} = V_{IH}$
	I_{CC12}	—	125	—	110	mA		$\overline{SE} = V_{IL}$, SC Cycling t_{SOC} = Min
Input Leakage Current	I_{LI}	−10	10	−10	10	µA		
Output Leakage Current	I_{LO}	−10	10	−10	10	µA		
Output High Voltage	V_{OH}	2.4	—	2.4	—	V	I_{OH} = −2 mA	
Output Low Voltage	V_{OL}	—	0.4	—	0.4	V	I_{OL} = 4.2 mA	

Note: 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.

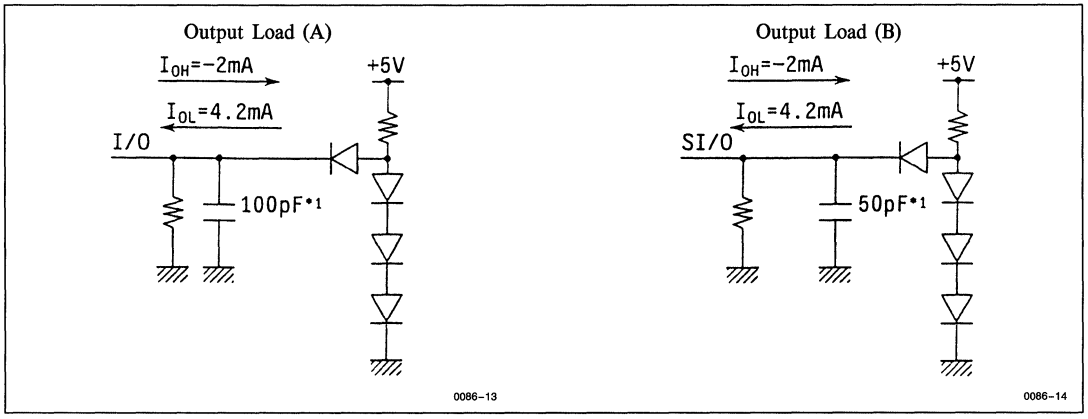
• **Capacitance** (T_A = 25°C, V_{CC} = 5V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, Address = V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O, QSF	$C_{I/O}$	—	—	7	pF

• AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 16]

Test Conditions

Input Rise and Fall Time	5 ns
Output Load	See figures
Input Timing Reference Levels	0.8V, 2.4V
Output Timing Reference Levels	0.4V, 2.4V



Note: *1. Including scope and jig.

Common Parameter

Parameter	Symbol	HM534253A-8		HM534253A-10		Unit	Note
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	150	—	190	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	—	25	—	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	60	25	75	ns	2
$\overline{RAS}$ Hold Time Referenced to $\overline{CAS}$	t_{RSH}	20	—	25	—	ns	
$\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$	t_{CSH}	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	ns	
Transition Time (Rise to Fall)	t_T	3	50	3	50	ns	3
Refresh Period	t_{REF}	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	10	—	15	—	ns	
DSF to $\overline{RAS}$ Setup Time	t_{FSR}	0	—	0	—	ns	
DSF to $\overline{RAS}$ Hold Time	t_{RFH}	10	—	15	—	ns	
DSF to $\overline{CAS}$ Setup Time	t_{FSC}	0	—	0	—	ns	
DSF to $\overline{CAS}$ Hold Time	t_{CFH}	15	—	20	—	ns	
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	ns	4
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	ns	4
Output Buffer Turn-off Delay Referenced to $\overline{CAS}$	t_{OFF1}	—	20	—	25	ns	5
Output Buffer Turn-off Delay Referenced to $\overline{OE}$	t_{OFF2}	—	20	—	25	ns	5

Read Cycle (RAM), Page Mode Read Cycle

Parameter	Symbol	HM534253A-8		HM534253A-10		Unit	Note
		Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	25	ns	7, 8
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	25	ns	7
Address Access Time	t_{AA}	—	40	—	45	ns	7, 9
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	ns	10
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	ns	10
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	40	20	55	ns	2
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	ns	
Column Address to $\overline{CAS}$ Lead Time	t_{CAL}	40	—	45	—	ns	
Page Mode Cycle Time	t_{PC}	50	—	55	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	45	—	50	ns	
Page Mode $\overline{RAS}$ Pulse Width	t_{RASP}	80	100000	100	100000	ns	

Write Cycle (RAM), Page Mode Write Cycle, Color Register Set Cycle

Parameter	Symbol	HM534253A-8		HM534253A-10		Unit	Note
		Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	ns	11
Write Command Hold Time	t_{WCH}	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	ns	12
Data-in Hold Time	t_{DH}	15	—	20	—	ns	12
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	10	—	15	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	10	—	15	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	20	—	25	—	ns	
Page Mode Cycle Time	t_{PC}	50	—	55	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
$\overline{CAS}$ to Data-in Delay Time	t_{CDD}	20	—	25	—	ns	13
Page Mode $\overline{RAS}$ Pulse Width	t_{RASP}	80	100000	100	100000	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM534253A-8		HM534253A-10		Unit	Note
		Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	200	—	250	—	ns	
$\overline{RAS}$ Pulse Width (Read-Modify-Write Cycle)	t_{RWS}	130	10000	160	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	45	—	55	—	ns	14
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	65	—	75	—	ns	14
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	20	—	25	—	ns	12
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	25	ns	7, 8
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	25	ns	7
Address Access Time	t_{AA}	—	40	—	45	ns	7, 9
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	40	20	55	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	ns	12
Data-in Hold Time	t_{DH}	15	—	20	—	ns	12
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM534253A-8		HM534253A-10		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	20	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	ns	

Flash Write Cycle, Block Write Cycle

Parameter	Symbol	HM534253A-8		HM534253A-10		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ to Data-in Delay Time	t_{CDD}	20	—	25	—	ns	13
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	20	—	25	—	ns	13

Read Transfer Cycle

Parameter	Symbol	HM534253A-8		HM534253A-10		Unit	Note
		Min	Max	Min	Max		
$\overline{DT}$ Hold Time Referenced to $\overline{RAS}$	t_{RDH}	70	10000	90	10000	ns	
$\overline{DT}$ Hold Time Referenced to $\overline{CAS}$	t_{CDH}	20	—	25	—	ns	
$\overline{DT}$ Hold Time Referenced to Column Address	t_{ADH}	30	—	35	—	ns	
$\overline{DT}$ Precharge Time	t_{DTP}	40	—	45	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Delay Time	t_{DRD}	70	—	90	—	ns	
SC to $\overline{RAS}$ Setup Time	t_{SRS}	30	—	30	—	ns	
1st SC to $\overline{RAS}$ Hold Time	t_{SRH}	85	—	105	—	ns	
1st SC to $\overline{CAS}$ Hold Time	t_{SCH}	30	—	35	—	ns	
1st SC to Column Address Hold Time	t_{SAH}	50	—	55	—	ns	

Read Transfer Cycle (continued)

Parameter	Symbol	HM534253A-8		HM534253A-10		Unit	Note
		Min	Max	Min	Max		
Last SC to $\overline{DT}$ Delay Time	t_{SDD}	5	—	5	—	ns	
1st SC to $\overline{DT}$ Hold Time	t_{SDH}	15	—	15	—	ns	
$\overline{RAS}$ to QSF Delay Time	t_{RQD}	—	95	—	115	ns	15
$\overline{CAS}$ to QSF Delay Time	t_{CQD}	—	35	—	40	ns	15
$\overline{DT}$ to QSF Delay Time	t_{DQD}	—	25	—	30	ns	15
QSF Hold Time Referenced to $\overline{RAS}$	t_{RQH}	20	—	25	—	ns	
QSF Hold Time Referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	ns	
QSF Hold Time Referenced to $\overline{DT}$	t_{DQH}	5	—	5	—	ns	
Serial Data-in to 1st SC Delay Time	t_{SZS}	0	—	0	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	30	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	ns	
SC Precharge Time	t_{SCP}	10	—	10	—	ns	
SC Access Time	t_{SCA}	—	25	—	25	ns	15
Serial Data-out Hold Time	t_{SOH}	5	—	5	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	40	20	55	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	ns	
$\overline{DT}$ High Hold Time to $\overline{RAS}$ Precharge	t_{DTHH}	25	—	30	—	ns	

Pseudo Transfer Cycle, Write Transfer Cycle

Parameter	Symbol	HM534253A-8		HM534253A-10		Unit	Note
		Min	Max	Min	Max		
$\overline{SE}$ Setup Time Referenced to $\overline{RAS}$	t_{ES}	0	—	0	—	ns	
$\overline{SE}$ Hold Time Referenced to $\overline{RAS}$	t_{EH}	10	—	15	—	ns	
SC Setup Time Referenced to $\overline{RAS}$	t_{SRS}	30	—	30	—	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	—	25	—	ns	
Serial Output Buffer Turn-off Time Referenced to $\overline{RAS}$	t_{SRZ}	10	45	10	50	ns	
$\overline{RAS}$ to Serial Data-in Delay Time	t_{SID}	45	—	50	—	ns	
$\overline{RAS}$ to QSF Delay Time	t_{RQD}	—	95	—	115	ns	15
$\overline{CAS}$ to QSF Delay Time	t_{CQD}	—	35	—	40	ns	15
QSF Hold Time Referenced to $\overline{RAS}$	t_{RQH}	20	—	25	—	ns	
QSF Hold Time Referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	30	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	ns	
SC Precharge Time	t_{SCP}	10	—	10	—	ns	
SC Access Time	t_{SCA}	—	25	—	25	ns	15
$\overline{SE}$ Access Time	t_{SEA}	—	25	—	25	ns	15
Serial Data-out Hold Time	t_{SOH}	5	—	5	—	ns	
Serial Write Enable Setup Time	t_{SWS}	5	—	5	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	ns	

Split Read Transfer Cycle, Split Write Transfer Cycle

Parameter	Symbol	HM534253A-8		HM534253A-10		Unit	Note
		Min	Max	Min	Max		
Split Transfer Setup Time	t_{STS}	20	—	25	—	ns	
Split Transfer Hold Time Referenced to $\overline{RAS}$	t_{RST}	80	—	100	—	ns	
Split Transfer Hold Time Referenced to $\overline{CAS}$	t_{CST}	20	—	25	—	ns	
Split Transfer Hold Time Referenced to Column Address	t_{AST}	40	—	45	—	ns	
SC to QSF Delay Time	t_{SQD}	—	25	—	30	ns	15
QSF Hold Time Referenced to SC	t_{SQH}	5	—	5	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	30	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	ns	
SC Precharge Time	t_{SCP}	10	—	10	—	ns	
SC Access Time	t_{SCA}	—	25	—	25	ns	15
Serial Data-out Hold Time	t_{SOH}	5	—	5	—	ns	
Serial Data-out Setup Time	t_{SIS}	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	40	20	55	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	ns	

Serial Read Cycle, Serial Write Cycle

Parameter	Symbol	HM534253A-8		HM534253A-10		Unit	Note
		Min	Max	Min	Max		
Serial Clock Cycle Time	t_{SCC}	30	—	30	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	ns	
Access Time from SC	t_{SCA}	—	25	—	25	ns	15
Access Time from $\overline{SE}$	t_{SEA}	—	25	—	25	ns	15
Serial Data-out Hold Time	t_{SOH}	5	—	5	—	ns	
Serial Output Buffer Turn-off Time Referenced to $\overline{SE}$	t_{SEZ}	—	20	—	25	ns	5
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	ns	
Serial Write Enable Setup Time	t_{SWS}	5	—	5	—	ns	
Serial Write Enable Hold Time	t_{SWH}	15	—	20	—	ns	
Serial Write Disable Setup Time	t_{SWIS}	5	—	5	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	15	—	20	—	ns	

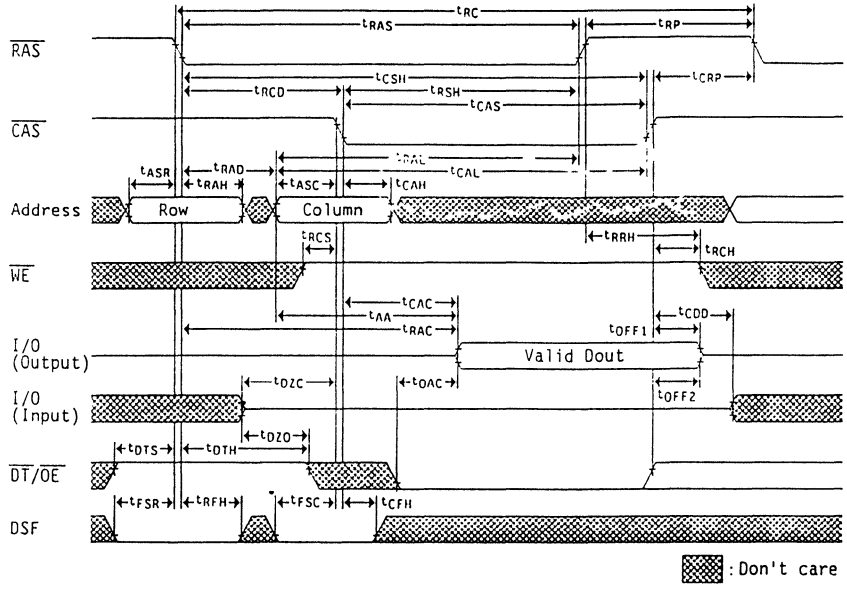
Logic Operation Mode

Parameter	Symbol	HM534253A-8		HM534253A-10		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$)	t_{CHR}	15	—	20	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	ns	
Write Cycle Time	t_{FRC}	170	—	215	—	ns	
$\overline{RAS}$ Pulse Width	t_{FRS}	100	10000	125	10000	ns	
Page Mode Cycle Time	t_{FPC}	70	—	80	—	ns	
$\overline{CAS}$ Pulse Width	t_{FCS}	40	—	50	—	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{CAS}$	t_{FRSH}	40	—	50	—	ns	
$\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$	t_{FCSH}	100	—	125	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{FRA}	60	—	70	—	ns	
Column Address to $\overline{CAS}$ Lead Time	t_{FCA}	60	—	70	—	ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	40	20	55	ns	
Write Command Setup Time	t_{WCS}	0	—	0	—	ns	
Write Command Hold Time	t_{WCH}	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	ns	12
Data-in Hold Time	t_{DH}	15	—	20	—	ns	12
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	10	—	15	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	10	—	15	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{DEH}	20	—	25	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	

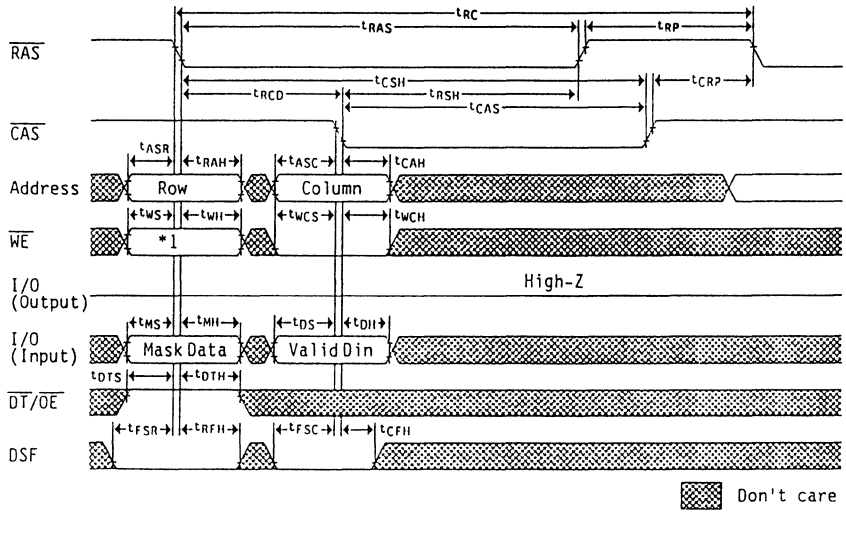
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. When $t_{RCD} > t_{RCD}$ (max) or $t_{RAD} > t_{RAD}$ (max), access time is specified by t_{CAC} or t_{AA}.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition time t_T is measured between V_{IH} and V_{IL}.
4. Data input must be floating before output buffer is turned on. In read cycle, read-modify-write cycle and delayed write cycle, either t_{DZC} (min) or t_{DZO} (min) must be satisfied.
5. t_{OFF1} (max) t_{OFF2} (max) and t_{SEZ} (max) are defined as the time at which the output achieves the open circuit condition ($V_{OH} - 200$ mV, $V_{OL} + 200$ mV).
6. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
8. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
9. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
10. If either t_{RCH} of t_{RRH} is satisfied, operation is guaranteed.
11. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
12. These parameters are specified by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
13. Either t_{CDD} (min) or t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{CAS}$ or $\overline{OE}$ prior to applying data to the device when output buffer is on.
14. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min) in read-modify-write cycle, the data of the selected address outputs to an I/O pin and input data is written into the selected address. t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{OE}$ prior to applying data to the device.
15. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
16. After power-up, pause for 100 μs or more and execute at least 8 initialization cycle (normal memory cycle or refresh cycle), then start operation.

■ TIMING WAVEFORMS

• Read Cycle

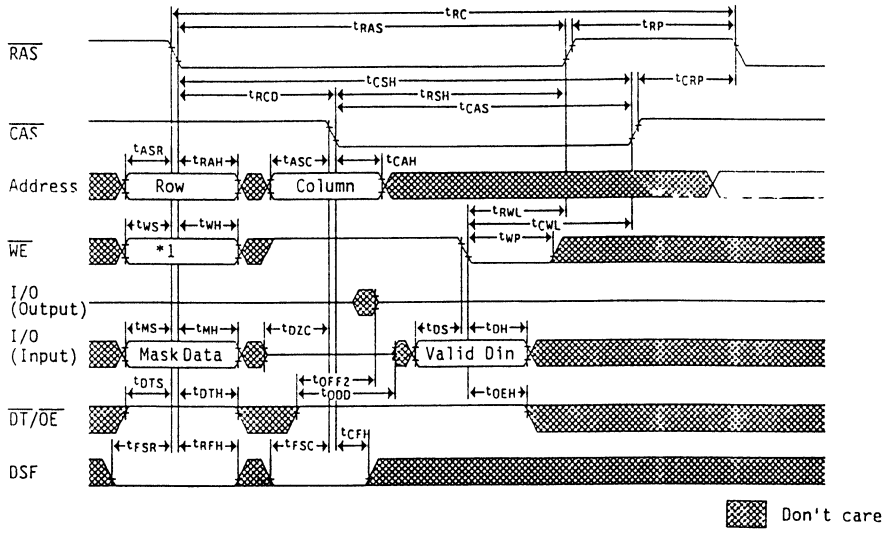


• Early Write Cycle



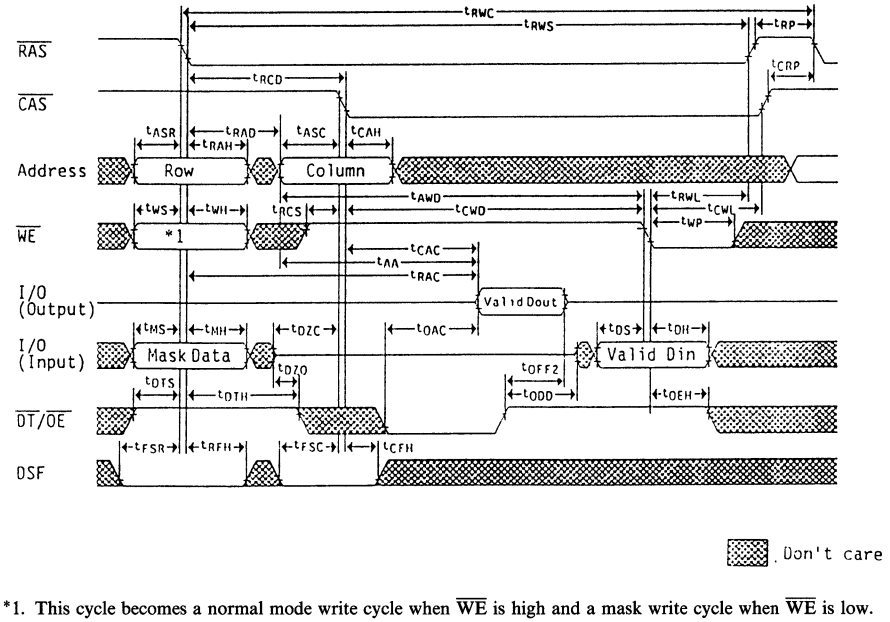
Note: *1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

• **Delayed Write Cycle**



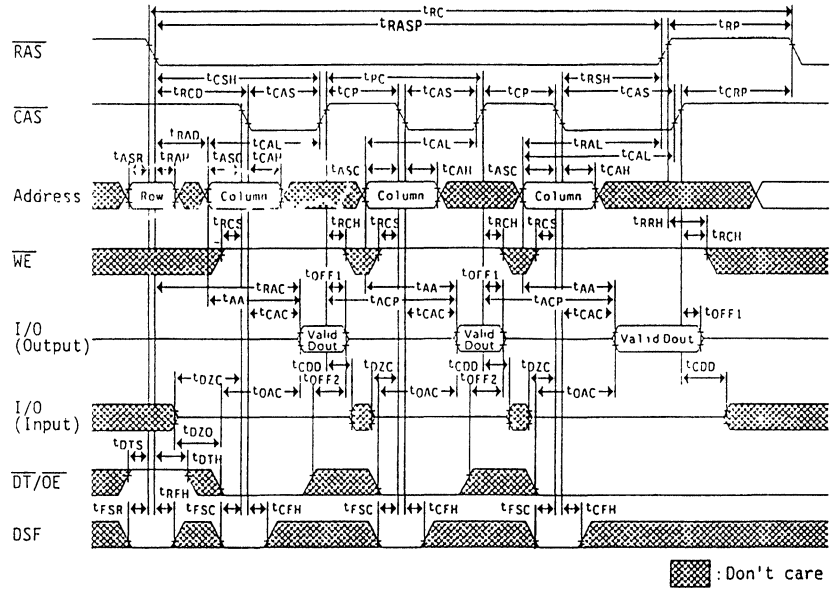
Note: *1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

• **Read-Modify-Write Cycle**

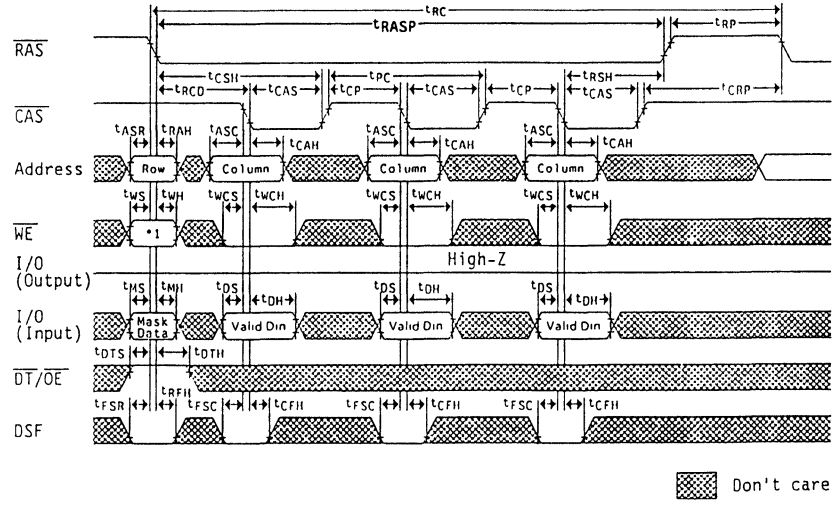


Note: *1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

• **Page Mode Read Cycle**

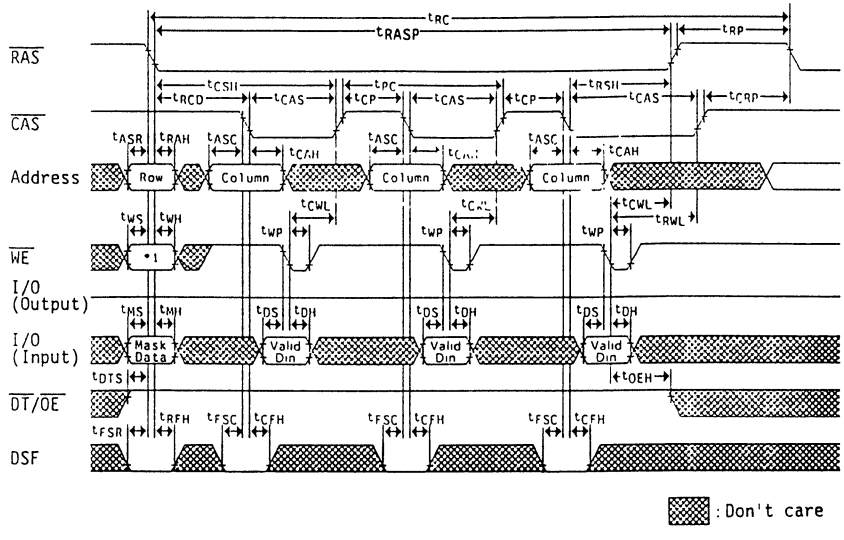


• **Page Mode Write Cycle (Early Write)**



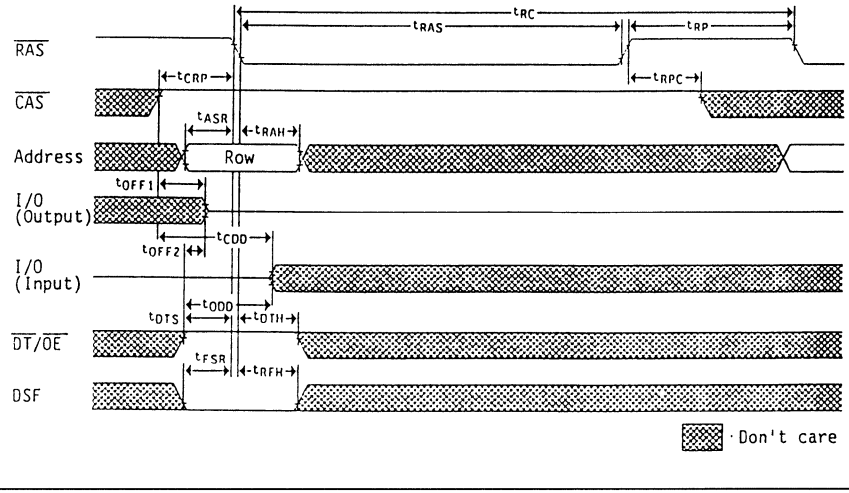
Note: *1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

• **Page Mode Write Cycle (Delayed Write)**

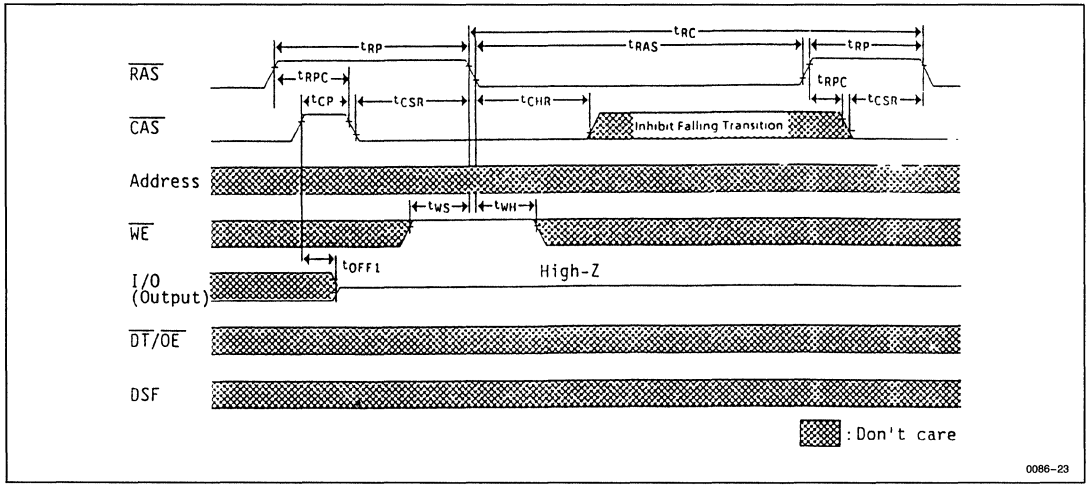


Note: *1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

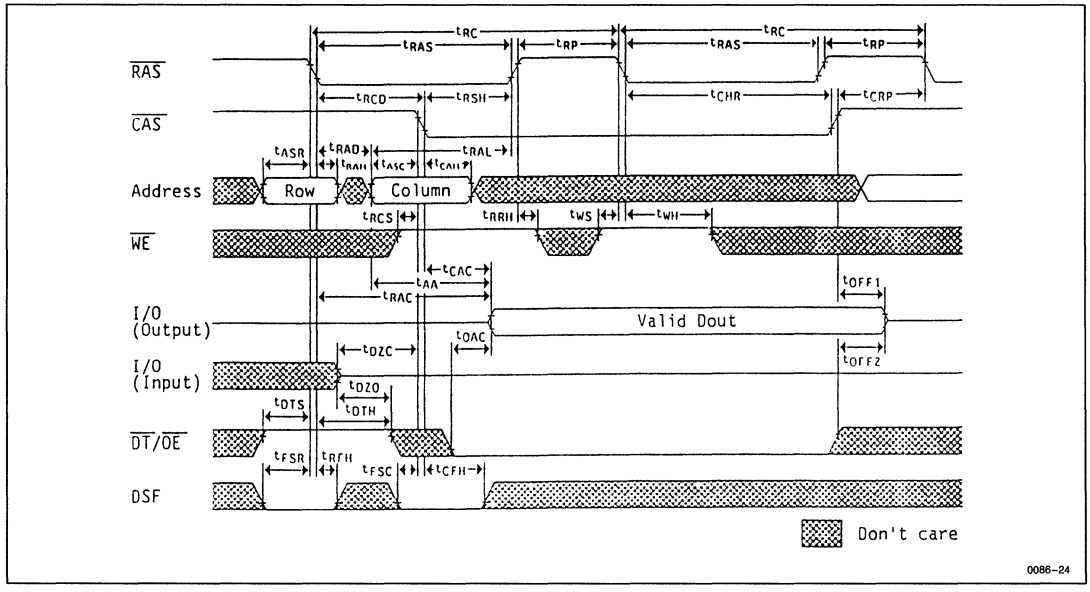
• **$\overline{RAS}$ Only Refresh Cycle**



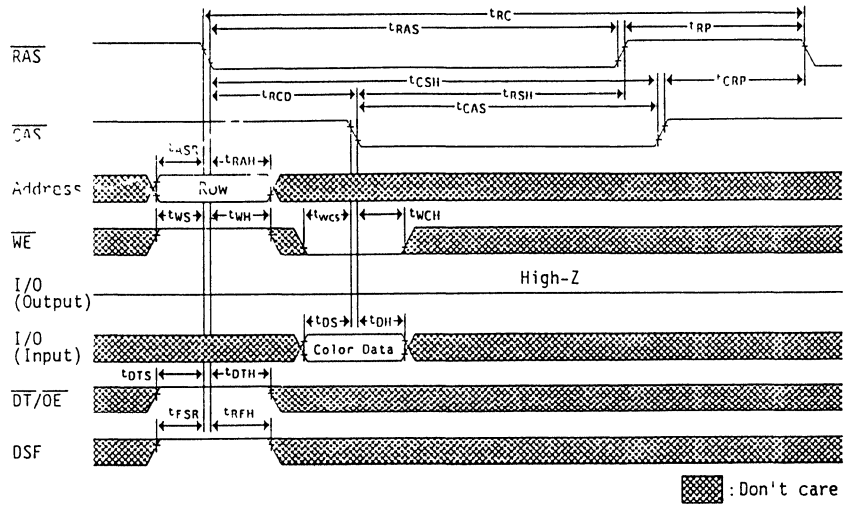
• **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**



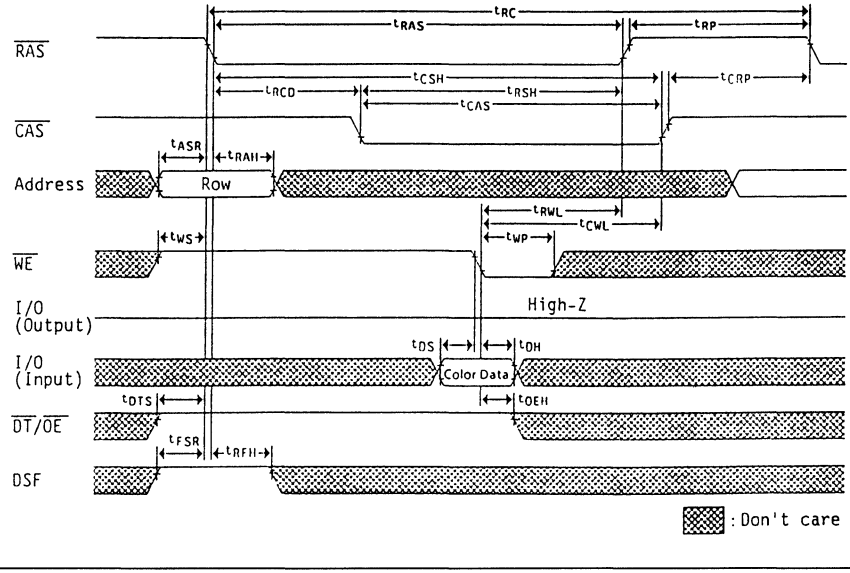
• **Hidden Refresh Cycle**



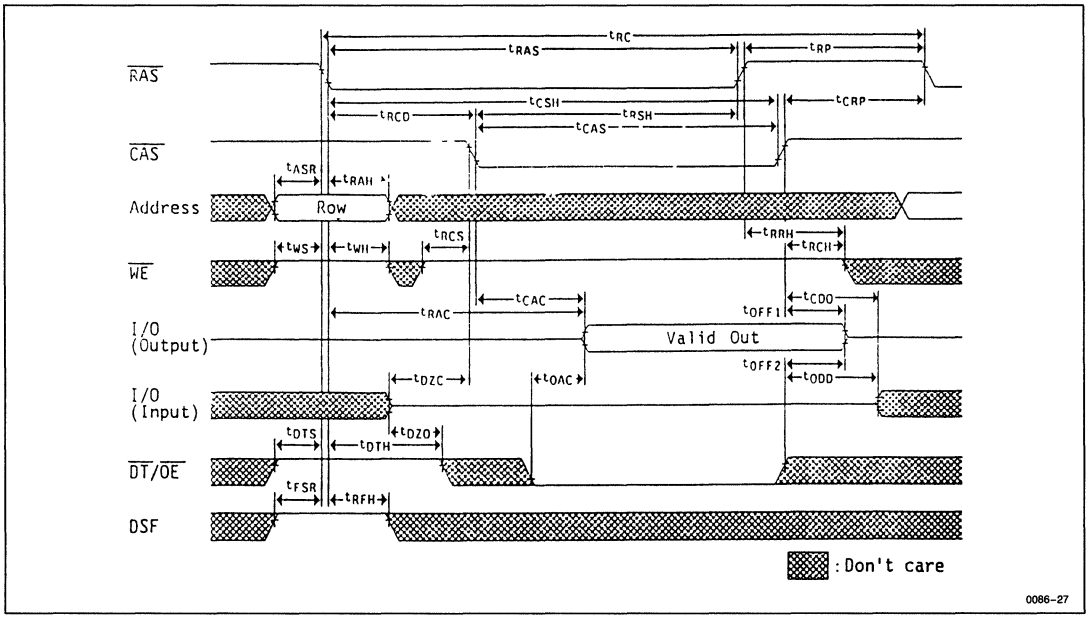
• **Color Register Set Cycle (Early Write)**



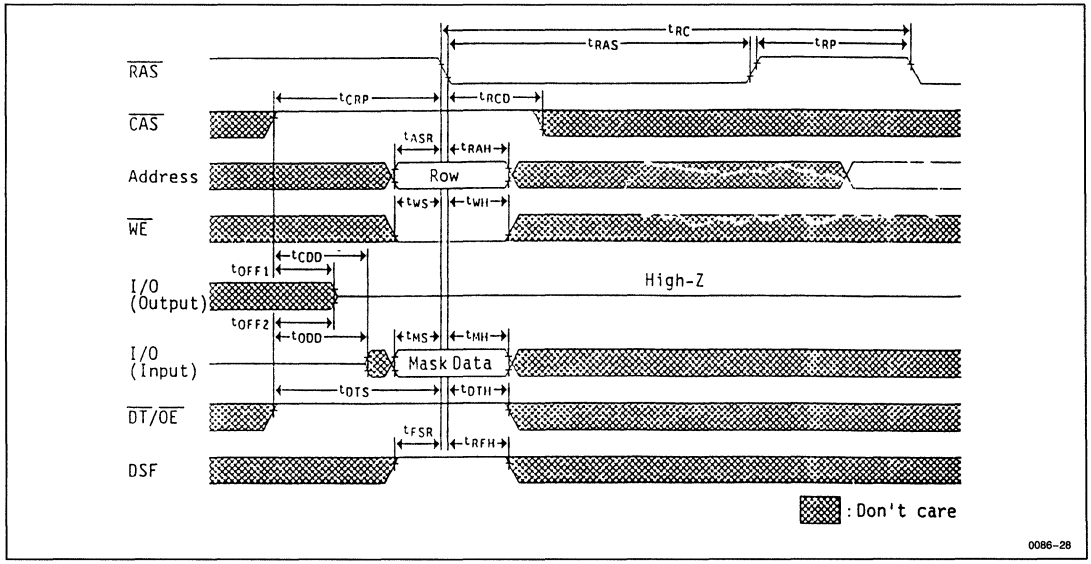
• **Color Register Set Cycle (Delayed Write)**



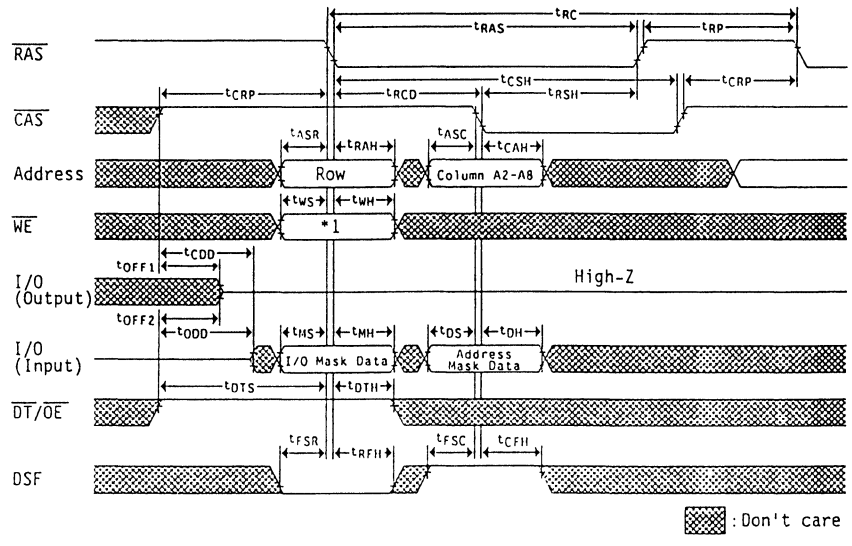
• **Color Register Read Cycle**



• **Flash Write Cycle**

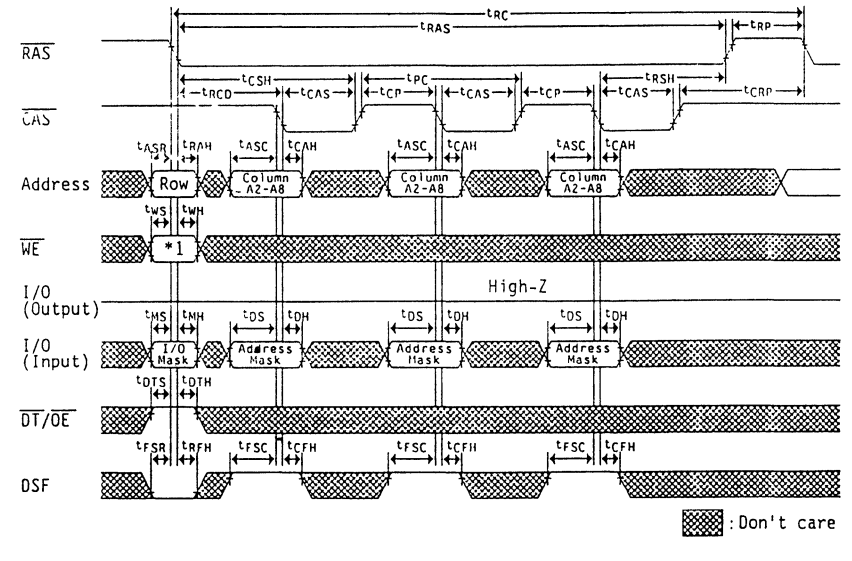


• **Block Write Cycle**



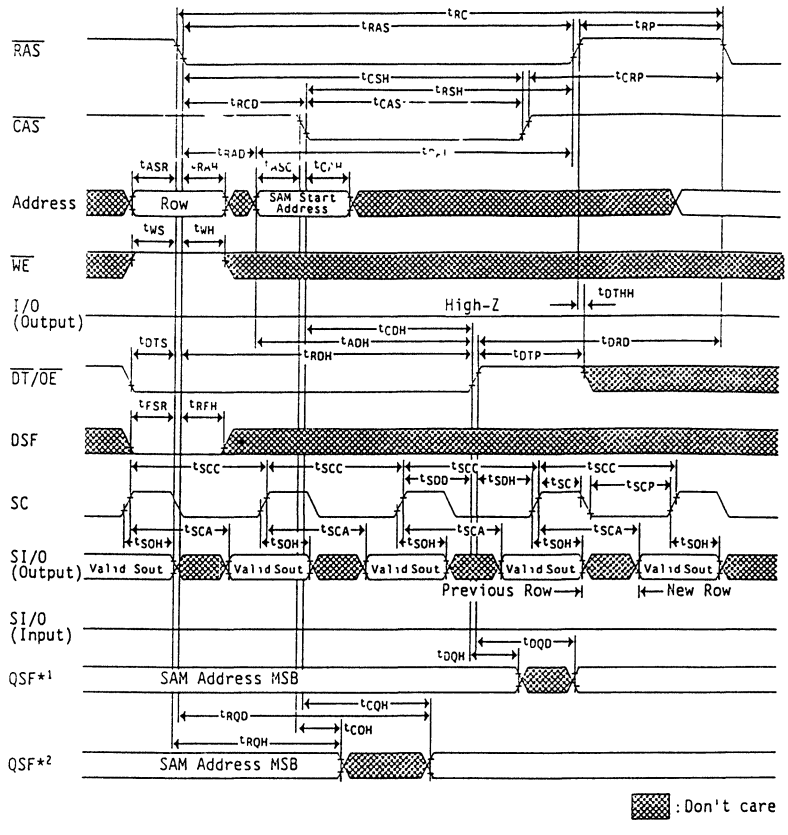
Note: *1. This cycle becomes a normal block write cycle when $\overline{WE}$ is high and a mask block write cycle when $\overline{WE}$ is low.

• **Page Mode Block Write Cycle**



Note: *1. This cycle becomes a normal block write cycle when $\overline{WE}$ is high and a mask block write cycle when $\overline{WE}$ is low.

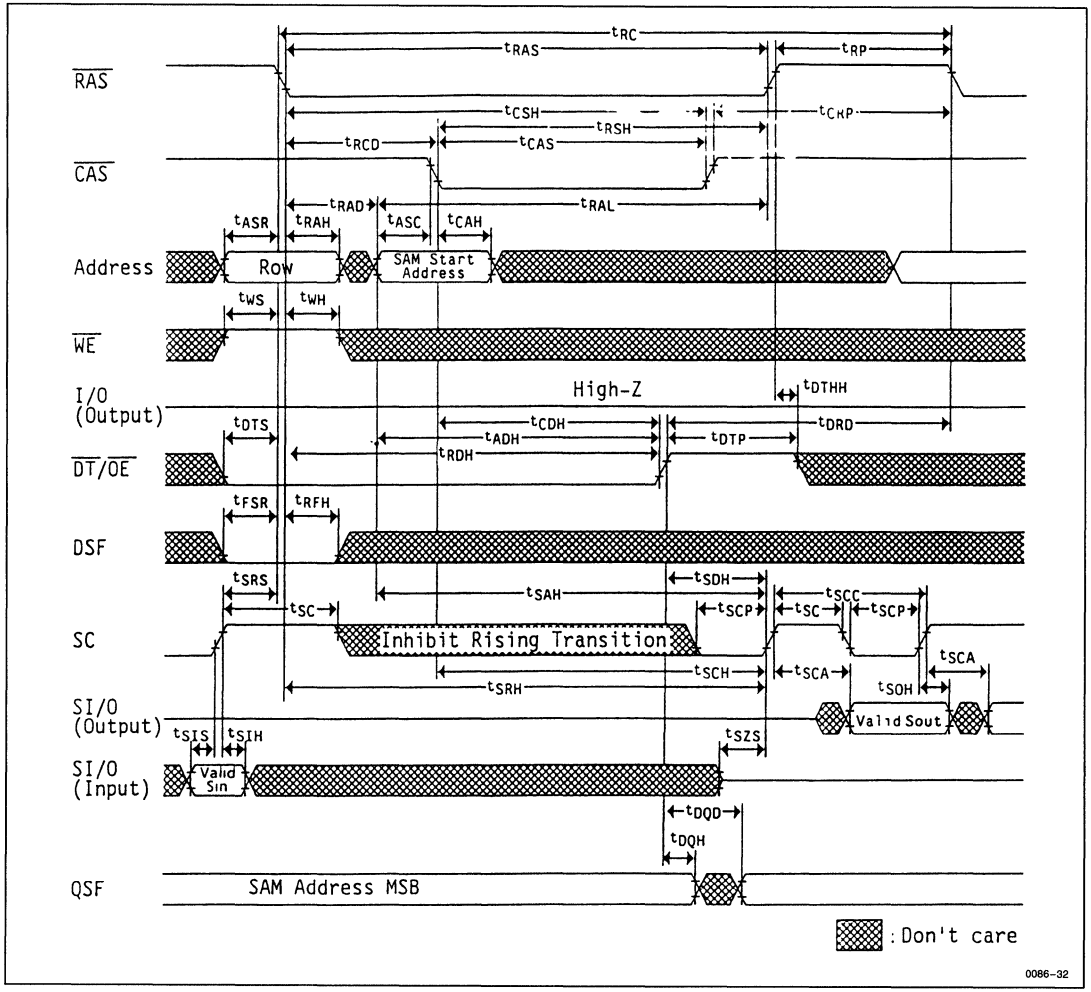
• Read Transfer Cycle (1)



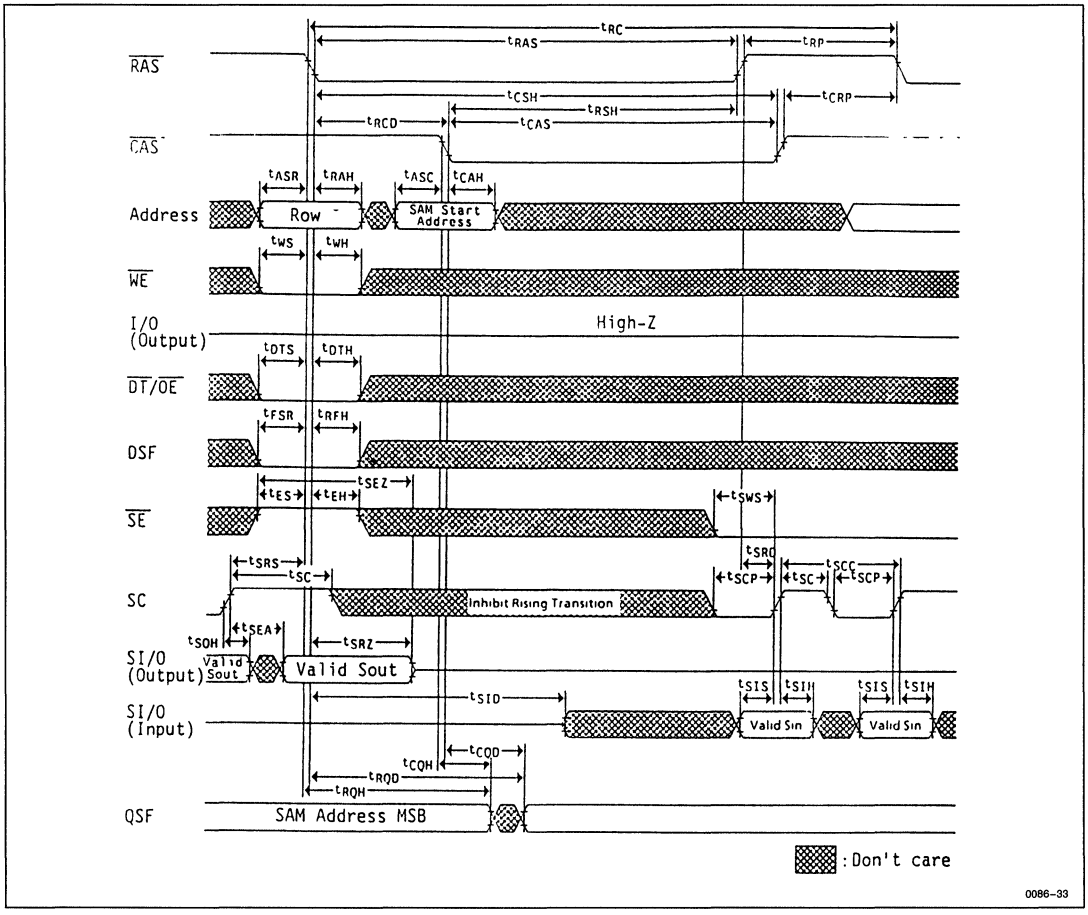
Notes: *1. This QSF timing is referred when SC is risen once or more between the previous transfer cycle and $\overline{CAS}$ falling edge of this cycle (QSF is switched by $\overline{DT}$ rising).

*2. This QSF timing is referred when SC isn't risen between the previous transfer cycle and $\overline{CAS}$ falling edge of this cycle (QSF is switched by $\overline{RAS}$ or $\overline{CAS}$ falling).

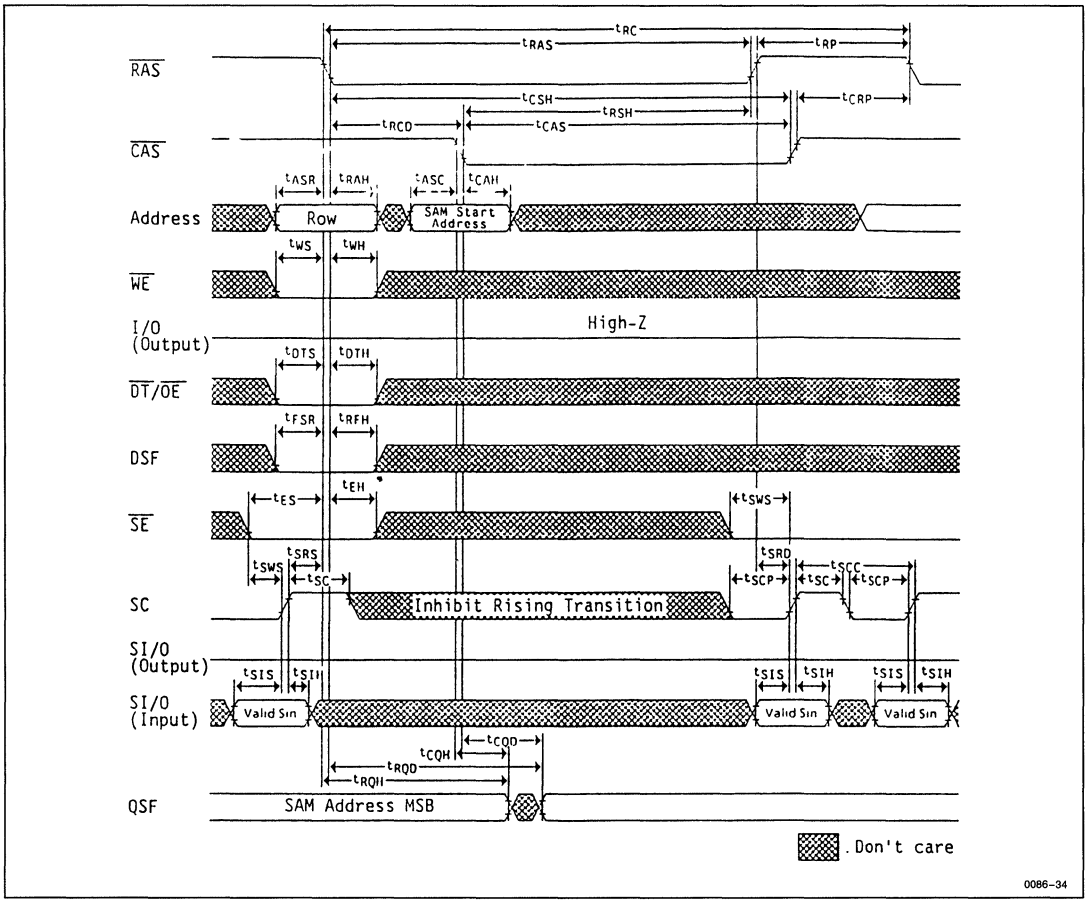
• **Read Transfer Cycle (2)**



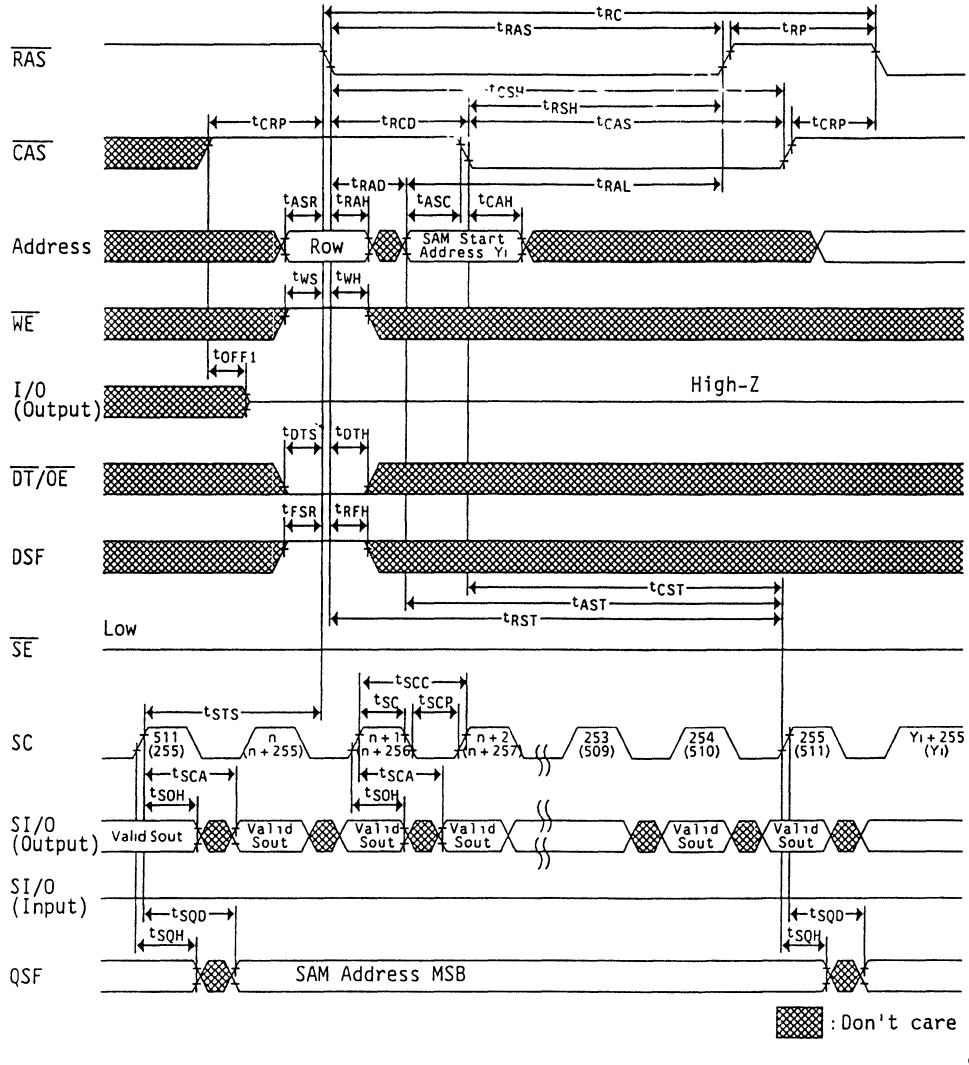
• **Pseudo Transfer Cycle**



• **Write Transfer Cycle**



• **Split Read Transfer Cycle**



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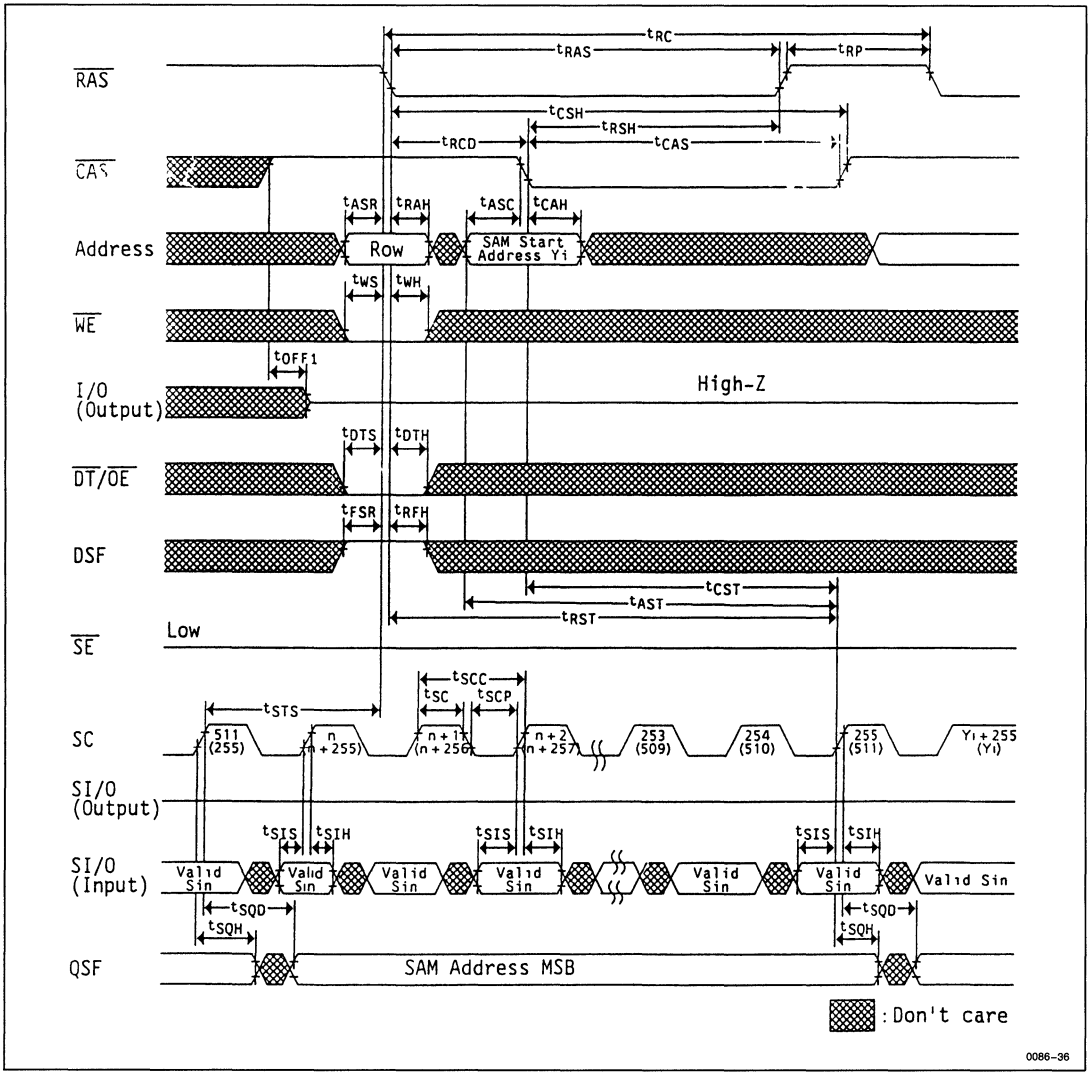
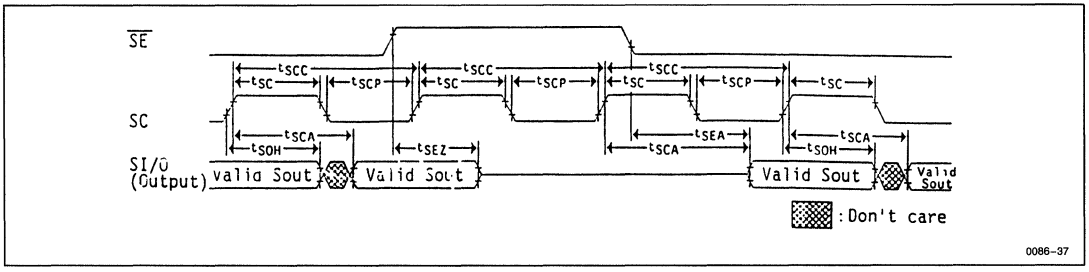
Note: *1. If the next transfer cycle after read transfer cycle is split read transfer cycle, one or more access to SC are required between read transfer cycle and split read transfer cycle.

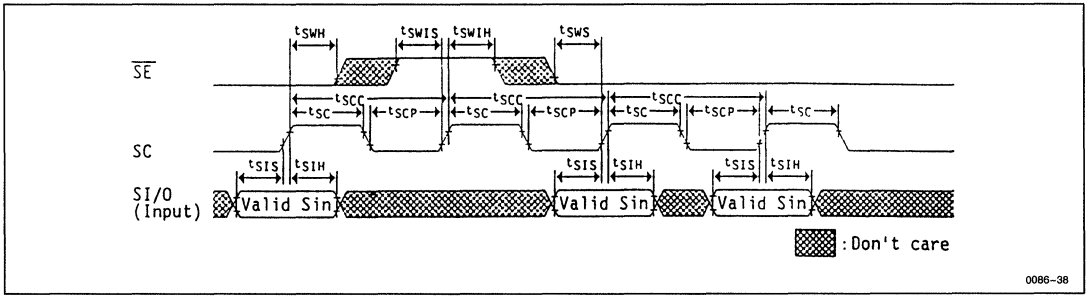
• **Split Write Transfer Cycle**



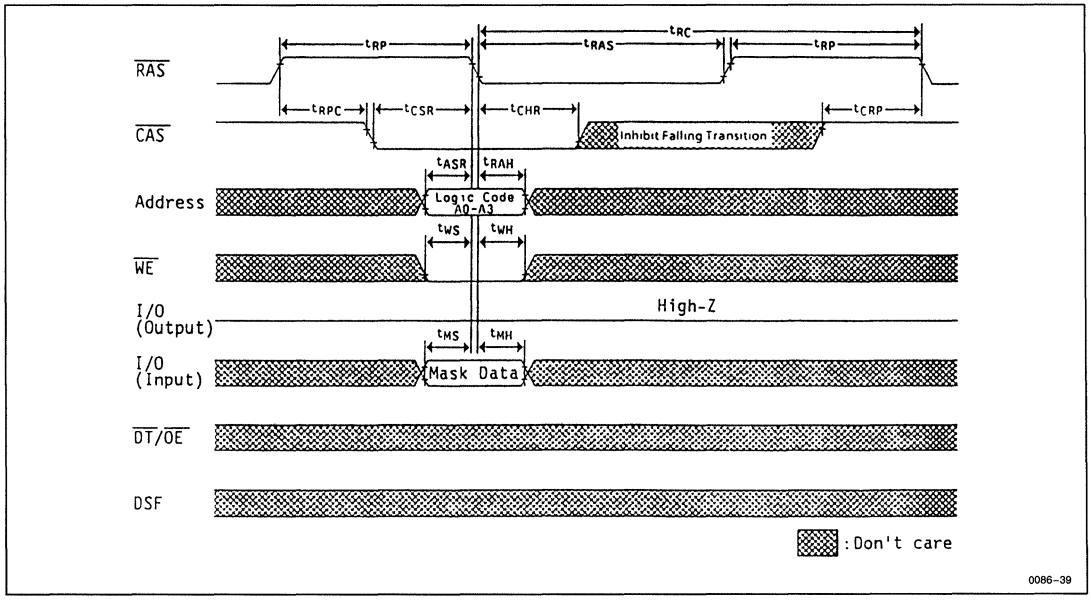
• **Serial Read Cycle**



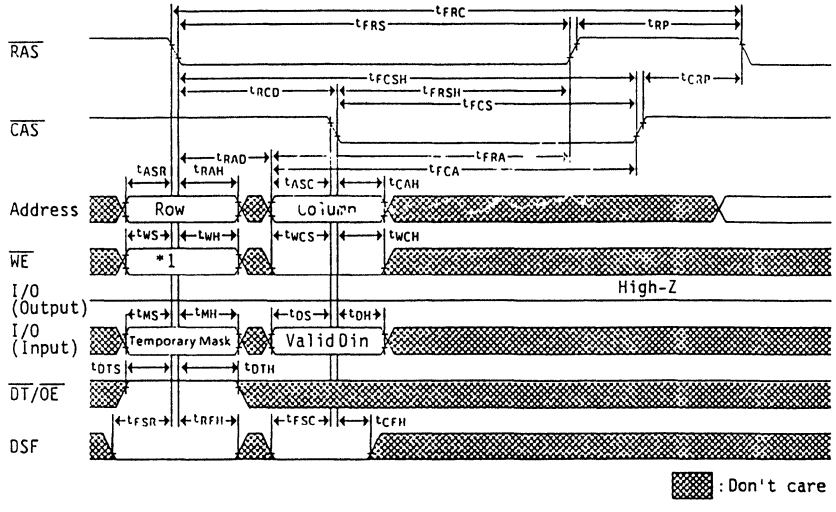
• **Serial Write Cycle**



• **Logic Operation Set/Reset Cycle**

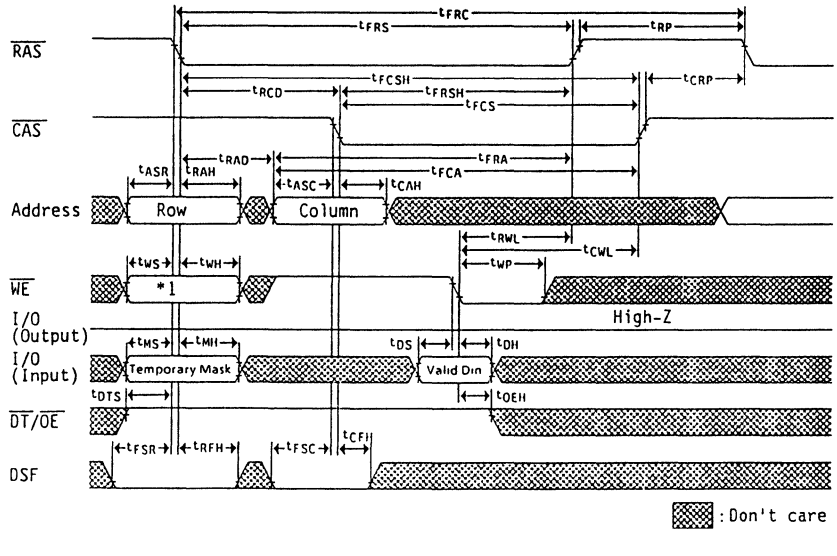


• **Logic Operation Mode Early Write Cycle**



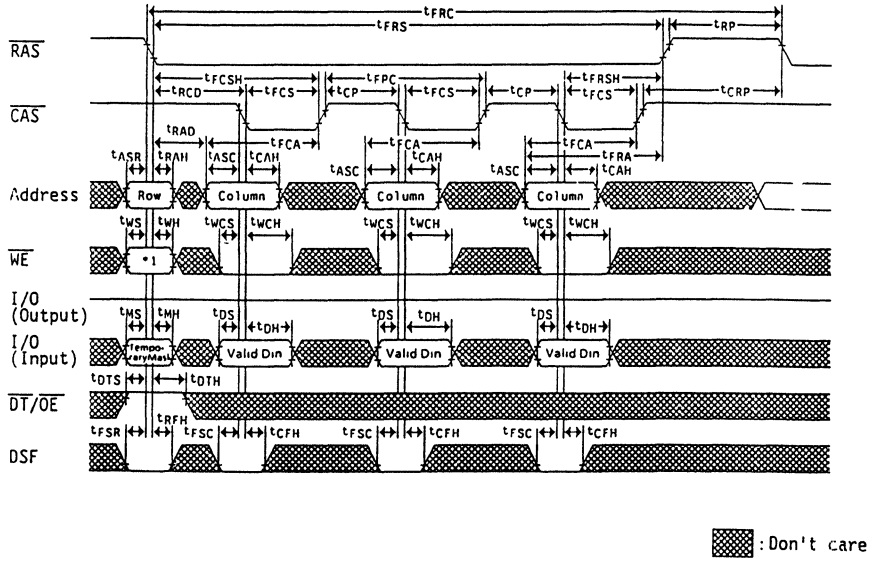
Note: *1. When $\overline{WE}$ is high, this cycle enters a logic operation mode. When $\overline{WE}$ is low, logic operation mode is reset, and a temporary mask write cycle starts.

• **Logic Operation Mode Delayed Write Cycle**



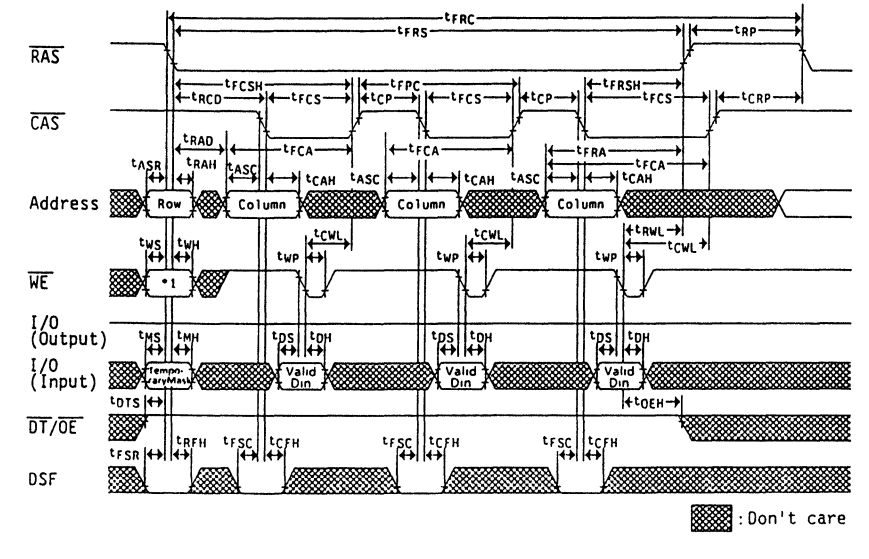
Note: *1. When $\overline{WE}$ is high, this cycle enters a logic operation mode. When $\overline{WE}$ is low, logic operation mode is reset, and a temporary mask write cycle starts.

• **Logic Operation Mode Page Mode Write Cycle (Early Write)**



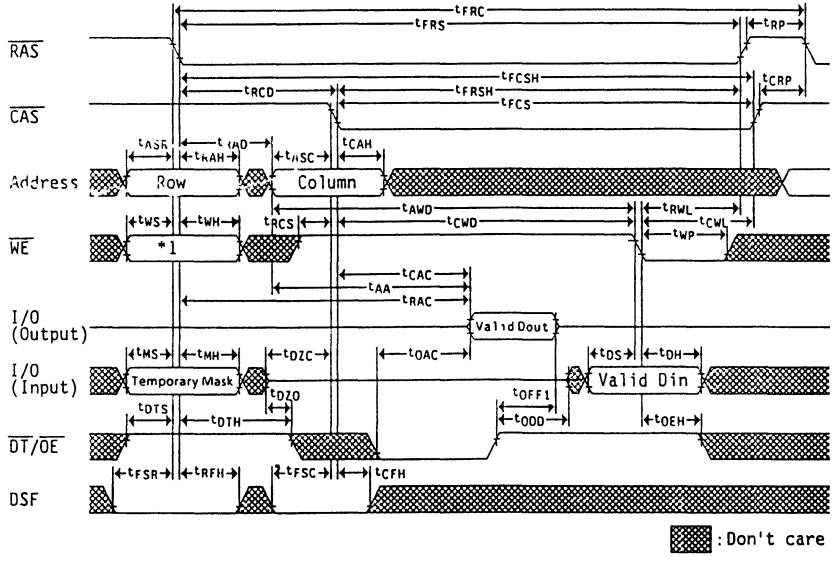
Note: *1. When $\overline{WE}$ is high, this cycle enters a logic operation mode. When $\overline{WE}$ is low, logic operation mode is reset, and a temporary mask write cycle starts.

• **Logic Operation Mode Page Mode Write Cycle (Delayed Write)**



Note: *1. When $\overline{WE}$ is high, this cycle enters a logic operation mode. When $\overline{WE}$ is low, logic operation mode is reset, and a temporary mask write cycle starts.

• **Logic Operation Mode Read-Modify-Write Cycle**



Note: *1. When $\overline{WE}$ is high, this cycle enters a logic operation mode. When $\overline{WE}$ is low, logic operation mode is reset, and a temporary mask write cycle starts.

HM538121 Series — Preliminary

131,072 x 8-Bit Multiport CMOS Video Random Access Memory

■ DESCRIPTION

The HM538121 is a 1-Mbit multiport video RAM equipped with a 128k-word x 8-bit dynamic RAM and a 256-word x 8-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has a write mask function. It is suitable for a graphic processing buffer memory.

■ FEATURES

- Multiport Organization
  - Asynchronous and Simultaneous Operation of RAM and SAM Capability
  - RAM: 128k-word x 8-bit and SAM: 256-word x 8-bit
- Access Time
  - RAM .....100 ns/100 ns/120 ns/150 ns (max)
  - SAM .....30 ns/35 ns/40 ns/50 ns (max)
- Cycle Time
  - RAM .....190 ns/190 ns/220 ns/260 ns (min)
  - SAM .....30 ns/40 ns/40 ns/60 ns (min)
- Low Power
  - Active
    - RAM .....495 mW (max)
    - SAM .....468 mW (max)
  - Standby .....40 mW (max)
- High-Speed Page Mode Capability
- Mask Write Mode Capability
- Bidirectional Data Transfer Cycle between RAM and SAM Capability
- Real Time Read Transfer Capability
- 3 Variations of Refresh (8 ms/512 Cycles)
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- TTL Compatible

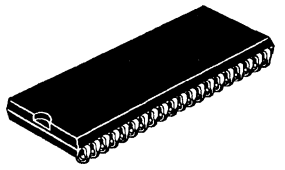
■ ORDERING INFORMATION

Part No.	Access Time		Package
	RAM	SAM	
HM538121JP-10	100 ns	30 ns	400 mil
HM538121JP-11	100 ns	35 ns	40-pin
HM538121JP-12	120 ns	40 ns	Plastic SOJ
HM538121JP-15	150 ns	50 ns	(CP-40D)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Inputs
I/O_0–I/O_7	RAM Port Data Inputs/Outputs
SI/O_0–SI/O_7	SAM Port Data Inputs/Outputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
SC	Serial Clock
$\overline{SE}$	SAM Port Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	Non Connection

HM538121JP Series

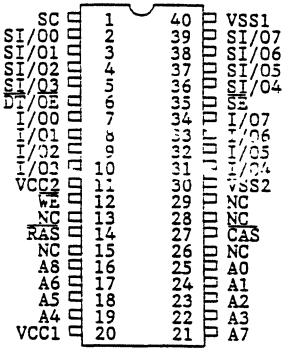


3DCP40D

(CP-40D)

■ PIN OUT

HM538121JP Series



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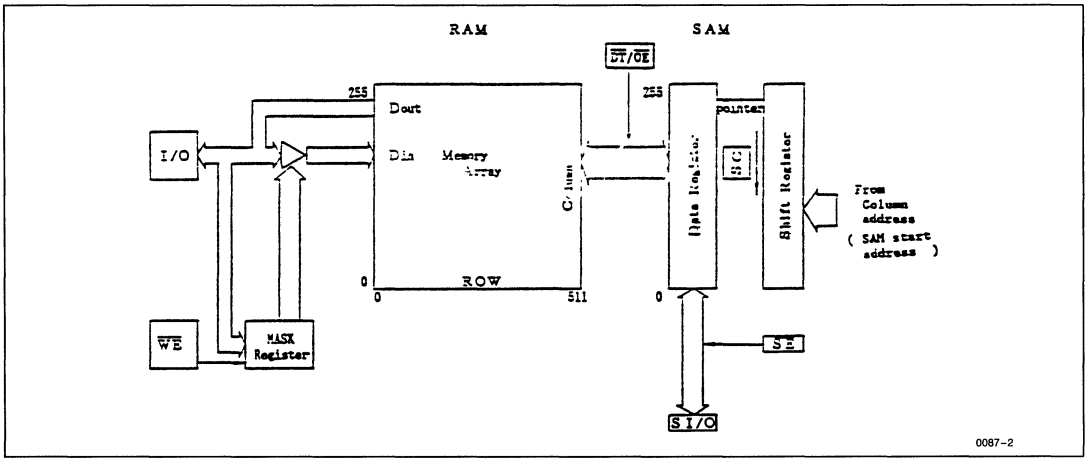
(Top View)

■ BLOCK DIAGRAM



■ PIN FUNCTION

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in Table 1 are input at the falling edge of $\overline{RAS}$. The input level of those signals determine the operation cycle of the HM538121.

• Table 1. Operation Cycles of the HM538121

Input Level at the Falling Edge of $\overline{RAS}$				Operation Cycle
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SE}$	
H	H	H	X	RAM Read/Write
H	H	L	X	Mask Write
H	L	H	X	Read Transfer
H	L	L	H	Pseudo Transfer
H	L	L	L	Write Transfer
L	X	X	X	CBR Refresh

Note: X: Don't care.

$\overline{CAS}$ (input pin): Column address is put into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A_0–A_8 (input pins): Row address is determined by A_0–A_8 level at the falling edge of $\overline{RAS}$. Column address is determined by A_0–A_7 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538121 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O_0–I/O_7 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only on high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data is output from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is put into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not put into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O_0–SI/O_7 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

■ OPERATION OF HM538121

• Operation of RAM Port

RAM Read Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high, at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data is output through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write) ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after $\overline{RAS}$ is set low, a write cycle is executed and I/O data is written at the selected addresses. When all 8 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling edge. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables write after read to execute in the same address cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and setting $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is preserved. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is preserved during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle and is higher than the standard page mode cycle by 70–80%. This product is based on static column mode, therefore, address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 256-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 μs).

• Transfer Operation

HM538121 provides the read transfer cycle, pseudo transfer cycle, and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$.

They have the following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)

(2) Determine direction of data transfer

(a) Read transfer cycle: RAM → SAM

(b) Write transfer cycle: RAM ← SAM

(3) Determine input or output of SAM I/O pin (SI/O)

Read transfer cycle: SI/O output

Pseudo transfer cycle, write transfer cycle: SI/O input

(4) Determine first SAM address to access (SAM start address) after transferring at column address.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by setting $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address data (256 x 8-bit) determined by this cycle is transferred synchronously at the rising of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address decided by column address.

This cycle can execute SAM access serially even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) is specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge, and t_{SDH} (min) between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge (see Figure 1).

If read transfer cycle is executed, SI/O becomes output state. When the previous transfer cycle is either pseudo transfer cycle or write transfer cycle and SI/O is in input state, uncertain data is output after t_{RLZ} (min) after the $\overline{RAS}$ falling edge. Before that, input should be set high impedance to avoid data contention.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle is available for switching SI/O from output state to input state because data in RAM isn't rewritten. This cycle starts when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high, at the falling edge of $\overline{RAS}$. The output buffer in SI/O becomes high impedance within t_{SRZ} (max) from the $\overline{RAS}$ falling edge. Data should be input to SI/O later than t_{SID} (min) to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC should not be raised.

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address to serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC should not be raised.

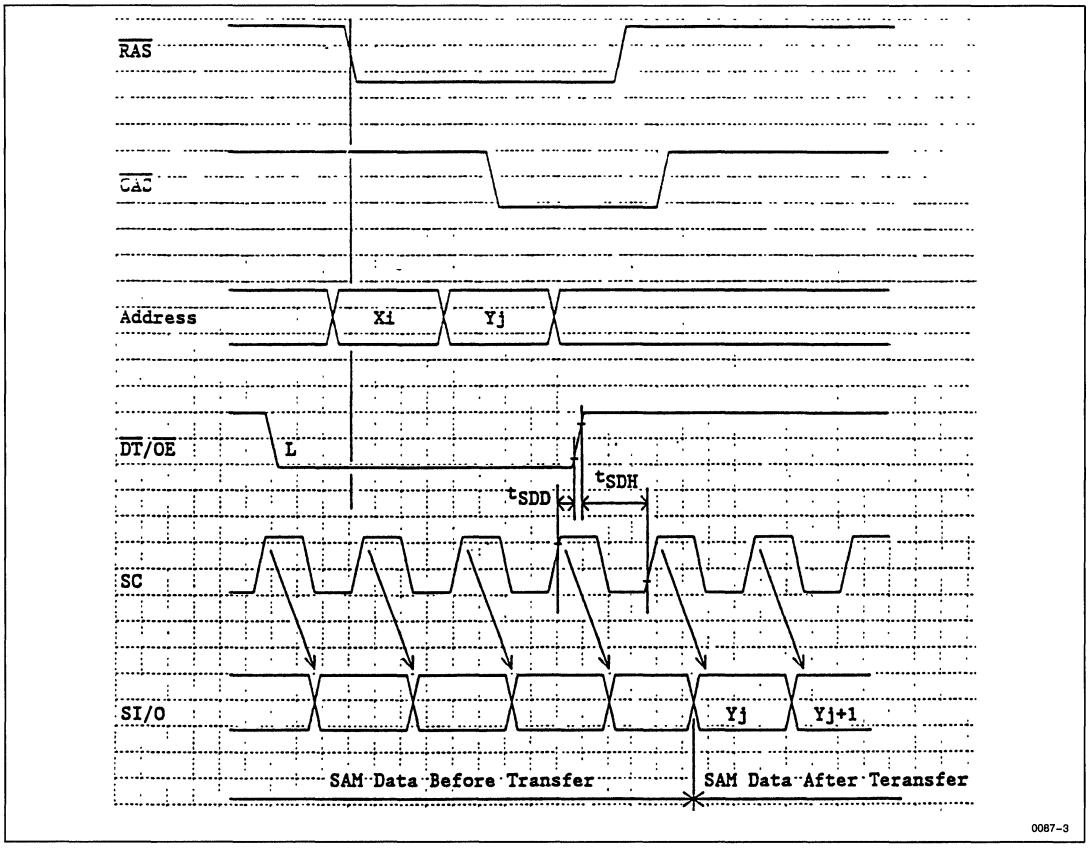


Figure 1. Real Time Read Transfer

• SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. If $\overline{SE}$ is set high SI/O becomes high impedance and internal pointer is incremented at the SC rising edge.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is programmed into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't input into data register. Internal pointer is incremented according to the SC rising edge, so $\overline{SE}$ high can mask data for SAM.

• Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is performed by accessing all 512 row addresses every 8 ms. There are three refresh cycles: (1) $\overline{RAS}$ only refresh cycle, (2) $\overline{CAS}$ before $\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required for accessing all row addresses every 8 ms.

$\overline{RAS}$ Only Refresh Cycle: $\overline{RAS}$ only refresh cycle is performed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high by inputting the row address (= refresh address) from external circuits. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ should be high at the falling edge of $\overline{RAS}$.

CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.

Hidden Refresh Cycle: Hidden refresh cycle performs refresh by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register, selector), organized as fully static circuitry, don't require refresh.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Note
Terminal Voltage	V_T	−1.0 to +7.0	V	1
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V	1
Power Dissipation	P_T	1.0	W	
Operating Temperature	T_{opr}	0 to +70	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

Note: 1. Relative to V_{SS}.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−0.5	—	0.8	V	1, 2

Notes: 1. All voltages referenced to V_{SS}.
2. −3.0V for pulse width ≤ 10 ns.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM538121-10		HM538121-11		HM538121-12		HM538121-15		Unit	Test Conditions		Note
		Min	Max	Min	Max	Min	Max	Min	Max		RAM Port	SAM Port	
Operating Current	I_{CC1}	—	90	—	90	—	80	—	70	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	$\overline{SE}$ = V_{IH}, SC = V_{IL}	1
	I_{CC7}	—	160	—	160	—	140	—	120	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Standby Current	I_{CC2}	—	7	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	$\overline{SE}$ = V_{IH}, SC = V_{IL}	1
	I_{CC8}	—	85	—	70	—	70	—	55	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	90	—	90	—	80	—	70	mA	$\overline{RAS}$ Cycling $\overline{CAS}$ = V_{IH} t_{RC} = Min	$\overline{SE}$ = V_{IH}, SC = V_{IL}	1
	I_{CC9}	—	150	—	150	—	130	—	110	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Page Mode Current	I_{CC4}	—	115	—	115	—	105	—	95	mA	$\overline{CAS}$ Cycling $\overline{RAS}$ = V_{IL} t_{PC} = Min	$\overline{SE}$ = V_{IH}, SC = V_{IL}	1
	I_{CC10}	—	185	—	185	—	160	—	140	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC5}	—	80	—	80	—	70	—	60	mA	$\overline{RAS}$ Cycling t_{RC} = Min	$\overline{SE}$ = V_{IH}, SC = V_{IL}	1
	I_{CC11}	—	130	—	130	—	110	—	90	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Data Transfer Current	I_{CC6}	—	115	—	115	—	110	—	100	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	$\overline{SE}$ = V_{IH}, SC = V_{IL}	1
	I_{CC12}	—	185	—	185	—	160	—	140	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	−10	10	μA			
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	−10	10	μA			
Output High Voltage	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V	I_{OH} = −2 mA		
Output Low Voltage	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA		

Notes: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition ($I_{I/O}$ = $I_{SI/O}$ = 0 mA).
2. Address can be changed less than three times in one $\overline{RAS}$ cycle.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. Address must be fixed.

• **Capacitance** (T_A = 25°C, V_{CC} = 5V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, Address = V_{SS})

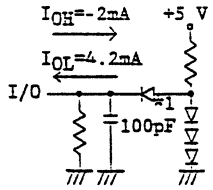
Parameter	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clocks	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

• **AC Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 11]

Test Conditions

Input Rise and Fall Time .....5 ns
Output Load .....See Figures
Input Timing Reference Levels 0.8V, 2.4V
Output Timing Reference Levels 0.4V, 2.4V

Output Load (A)



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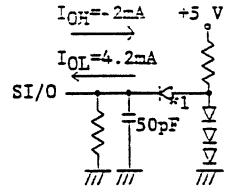
Output Load (B)



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Note: 1. Including Scope and Jig.

Common Parameters

Parameter	Symbol	HM538121-10		HM538121-11		HM538121-12		HM538121-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	190	—	190	—	220	—	260	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	80	—	80	—	90	—	100	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	30	10000	30	10000	35	10000	40	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	15	—	20	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	70	25	70	25	85	30	110	ns	5, 6
$\overline{RAS}$ Hold Time	t_{RSH}	30	—	30	—	35	—	40	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Pre-charge Time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise to Fall)	t_T	3	50	3	50	3	50	3	50	ns	8
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	ms	

Common Parameters (continued)

Parameter	Symbol	HM538121-10		HM538121-11		HM538121-12		HM538121-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	—	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	—	15	—	15	—	20	—	ns	
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	0	—	0	—	ns	
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	0	—	0	—	ns	

Read Cycle (RAM), Page Mode Read Cycle

Parameter	Symbol	HM538121-10		HM538121-11		HM538121-12		HM538121-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	3, 5
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	45	—	55	—	70	ns	3, 6
Output Buffer Turn-off Delay Referenced to $\overline{CAS}$	t_{OFF1}	—	25	—	25	—	30	—	40	ns	7
Output Buffer Turn-off Delay Referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	7
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	0	—	ns	12
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20	55	20	55	20	65	25	80	ns	5, 6
Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	20	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	—	75	ns	
$\overline{RAS}$ Pulse Width in Page Mode	t_{RASP}	0.1	100	0.1	100	0.12	100	0.15	100	μs	

Write Cycle (RAM), Page Mode Write Cycle

Parameter	Symbol	HM538121-10		HM538121-11		HM538121-12		HM538121-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	9
Write Command Hold Time	t_{WCH}	25	—	25	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	25	—	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	
Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	20	—	ns	
$\overline{RAS}$ Pulse Width in Page Mode	t_{RASP}	0.1	100	0.1	100	0.12	100	0.15	100	μs	

Read-Modify-Write Cycle

Parameter	Symbol	HM538121-10		HM538121-11		HM538121-12		HM538121-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	255	—	255	—	295	—	350	—	ns	
$\overline{RAS}$ Pulse Width	t_{RWS}	165	10000	165	10000	195	10000	240	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	65	—	65	—	75	—	90	—	ns	9
Column Address to $\overline{WE}$ Delay	t_{AWD}	80	—	80	—	95	—	120	—	ns	9
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	25	—	25	—	30	—	40	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	3, 5
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	45	—	55	—	70	ns	3, 6

Read-Modify-Write Cycle (continued)

Parameter	Symbol	HM538121-10		HM538121-11		HM538121-12		HM538121-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to Column Address Delay	t_{RAD}	20	55	20	55	20	65	25	80	ns	5, 6
Output Buffer Turn-off Delay Referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	25	—	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	

Refresh Cycle

Parameter	Symbol	HM538121-10		HM538121-11		HM538121-12		HM538121-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CHR}	20	—	20	—	25	—	30	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

Transfer Cycle

Parameter	Symbol	HM538121-10		HM538121-11		HM538121-12		HM538121-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
$\overline{SE}$ to $\overline{RAS}$ Setup Time	t_{ES}	0	—	0	—	0	—	0	—	ns	
$\overline{SE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	—	15	—	15	—	20	—	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	—	30	—	30	—	35	—	ns	

Transfer Cycle (continued)

Parameter	Symbol	HM538121-10		HM538121-11		HM538121-12		HM538121-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
SC to $\overline{RAS}$ Setup Time	t_{SRS}	30	—	40	—	40	—	45	—	ns	
$\overline{DT}$ Hold Time from $\overline{RAS}$	t_{RDH}	80	—	90	—	90	—	110	—	ns	
$\overline{DT}$ Hold Time from $\overline{CAS}$	t_{CDH}	20	—	30	—	30	—	45	—	ns	
Last SC to $\overline{DT}$ Delay Time	t_{SDD}	5	—	5	—	5	—	10	—	ns	
First SC to $\overline{DT}$ Hold Time	t_{SDH}	20	—	25	—	25	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Lead Time	t_{DTL}	50	—	50	—	50	—	50	—	ns	
$\overline{DT}$ Hold Time Referenced to $\overline{RAS}$ High	t_{DTHH}	20	—	25	—	25	—	30	—	ns	
$\overline{DT}$ Precharge Time	t_{DTP}	30	—	35	—	35	—	40	—	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	—	60	—	60	—	75	—	ns	
Serial Data Input to $\overline{RAS}$ Delay Time	t_{SZR}	—	10	—	10	—	10	—	10	ns	
Serial Output Buffer Turn-off Delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	60	10	75	ns	7
$\overline{RAS}$ to S_{out} (Low-Z) Delay Time	t_{RLZ}	5	—	10	—	10	—	10	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Serial Clock Cycle Time	t_{SCC2}	40	—	40	—	40	—	60	—	ns	13
Access Time from SC	t_{SCA}	—	30	—	35	—	40	—	50	ns	4
Serial Data-out Hold Time	t_{SOH}	7	—	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	20	—	25	—	ns	

Serial Read Cycle

Parameter	Symbol	HM538121-10		HM538121-11		HM538121-12		HM538121-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Access Time from SC	t_{SCA}	—	30	—	35	—	40	—	50	ns	4
Access Time from $\overline{SE}$	t_{SEA}	—	25	—	30	—	30	—	40	ns	4
Serial Data-out Hold Time	t_{SOH}	7	—	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{SE}$	t_{SEZ}	—	25	—	25	—	25	—	30	ns	7

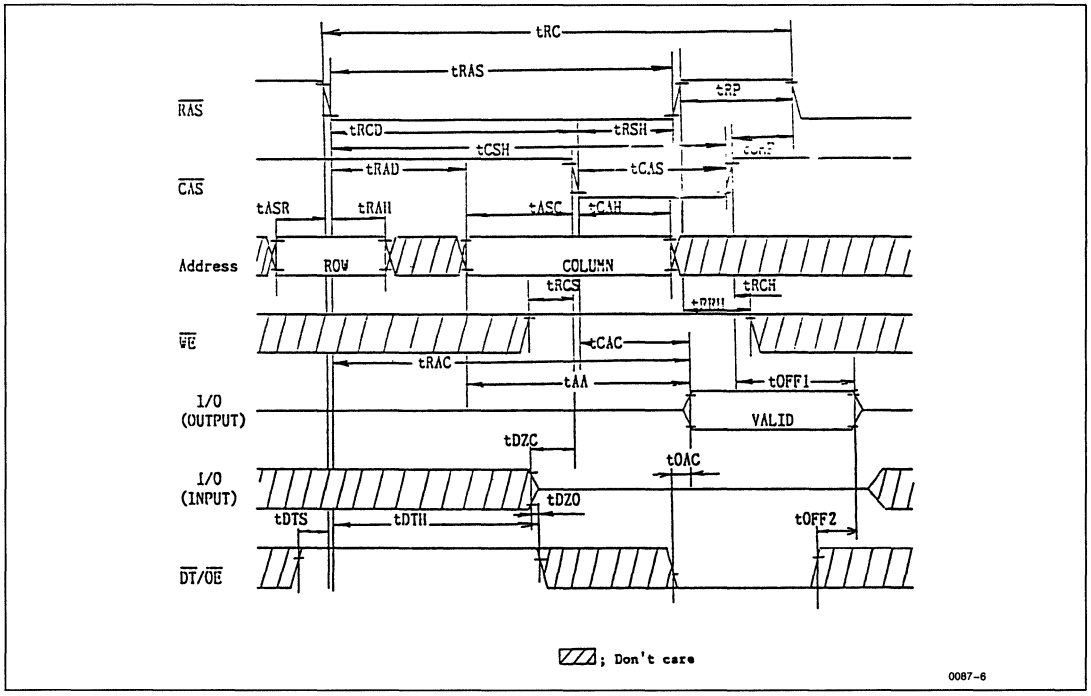
Serial Write Cycle

Parameter	Symbol	HM538121-10		HM538121-11		HM538121-12		HM538121-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	20	—	25	—	ns	
Serial Write Enable Setup Time	t_{SWS}	0	—	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	t_{SWH}	30	—	35	—	35	—	50	—	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	—	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	30	—	35	—	35	—	50	—	ns	

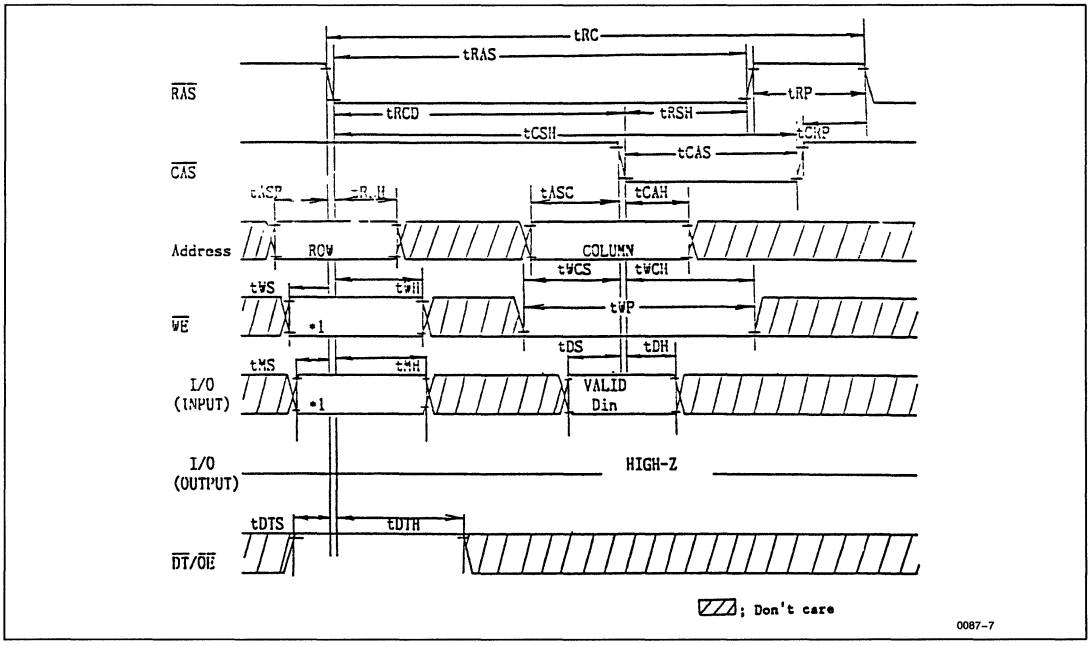
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
5. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
6. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
7. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition ($V_{OH} - 200$ mV, $V_{OL} + 200$ mV).
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
9. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-modify-write cycle; the data of the selected address is read out from a data output pin and input data is written into the selected address. In this case, impedance on I/O pins is controlled by $\overline{OE}$.
10. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles or to $\overline{WE}$ falling edge in delayed write or a read-modify-write cycles.
11. After power-up, pause for 100 μs or more and execute at least 8 initialization cycles (normal memory cycles or refresh cycles), then start operation.
12. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.
13. t_{CC2} is defined as the last SAM cycle time before read transfer in read transfer cycle (1).
14. When I/O or SI/O is in the output state, data input signals must not be applied to I/O or SI/O.
15. When $\overline{SE}$ is low after power on, SI/O is in the output state. Data input signals must not be applied to SI/O in this time.
16. When $\overline{CAS}$ and $\overline{DT}/\overline{OE}$ are both low after power on, it is possible that I/O is in the output state. Data input signals must not be applied to I/O in this time.

■ TIMING WAVEFORMS

• Read Cycle

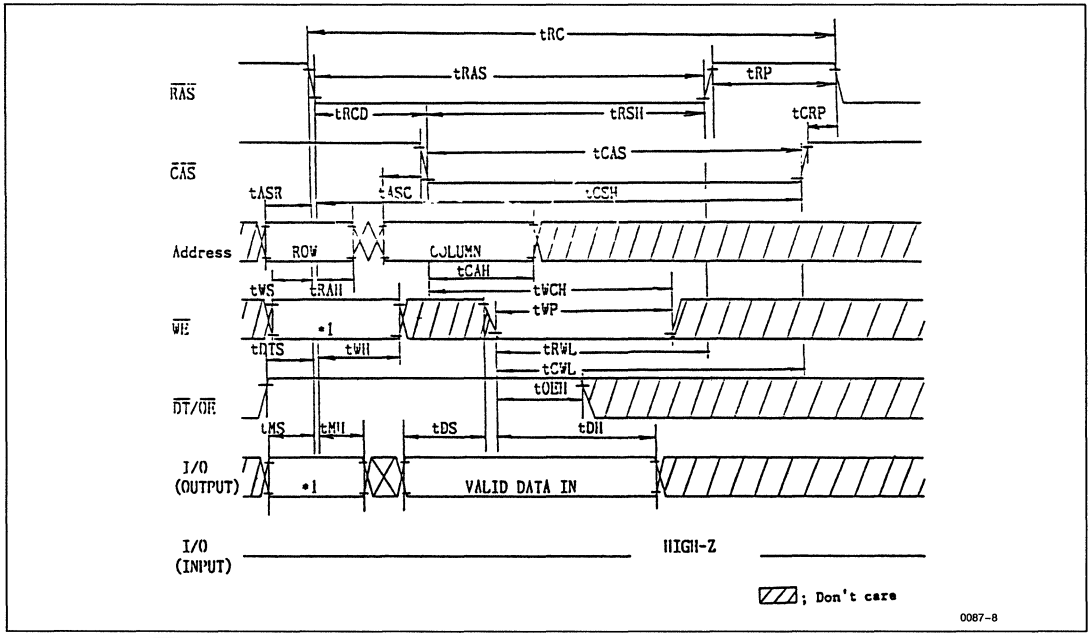


• Early Write Cycle



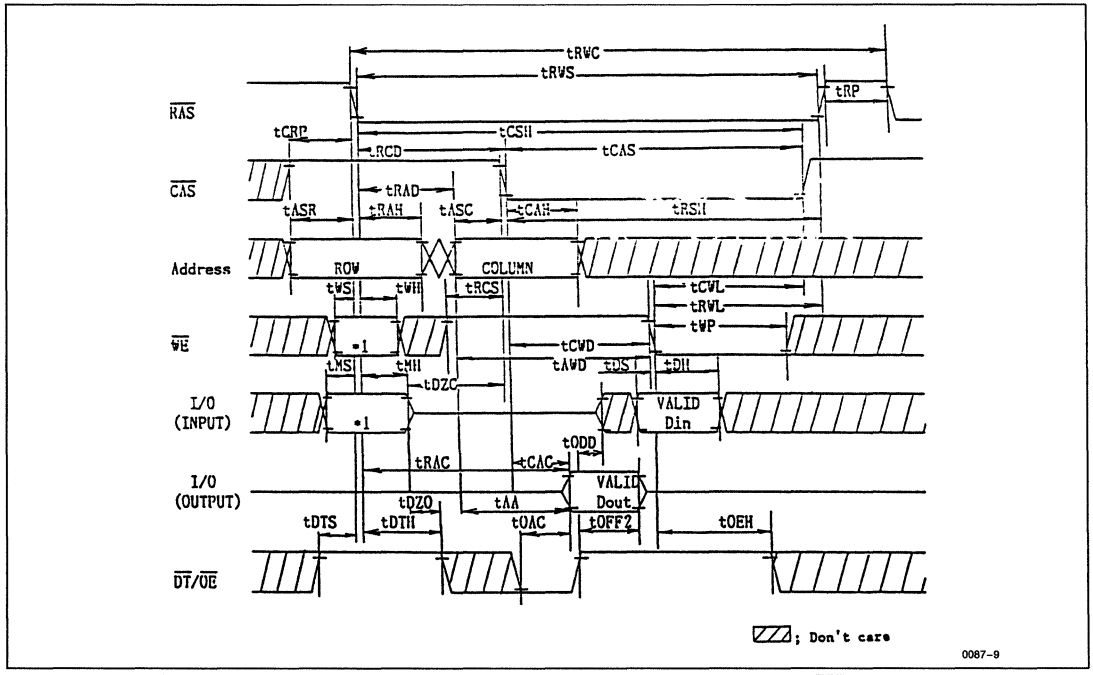
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Delayed Write Cycle**



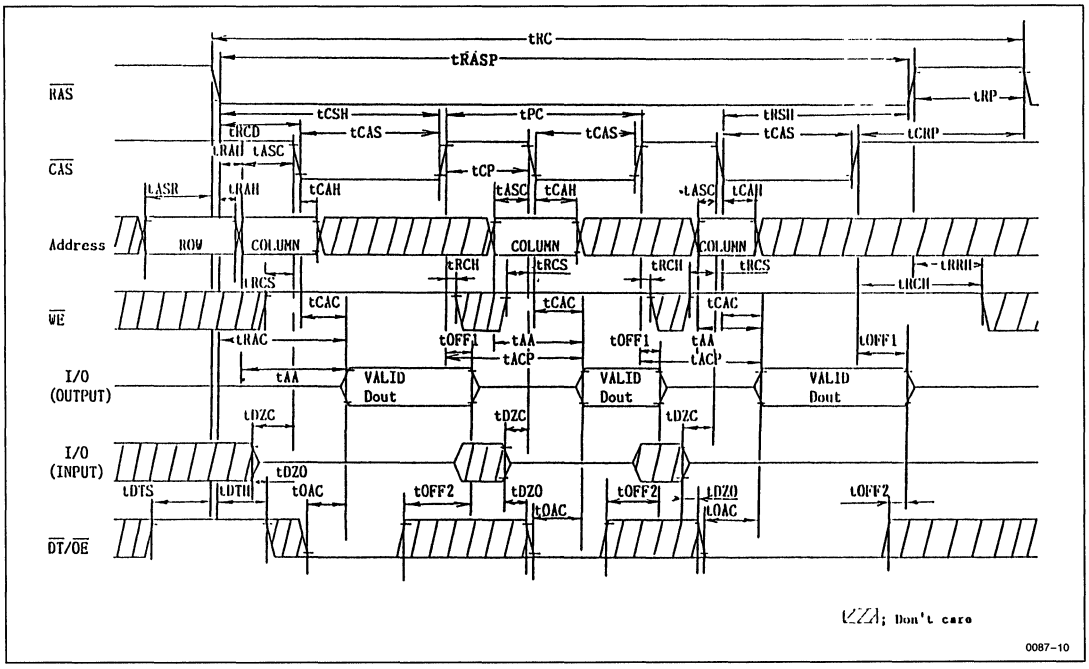
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Read-Modify-Write Cycle**

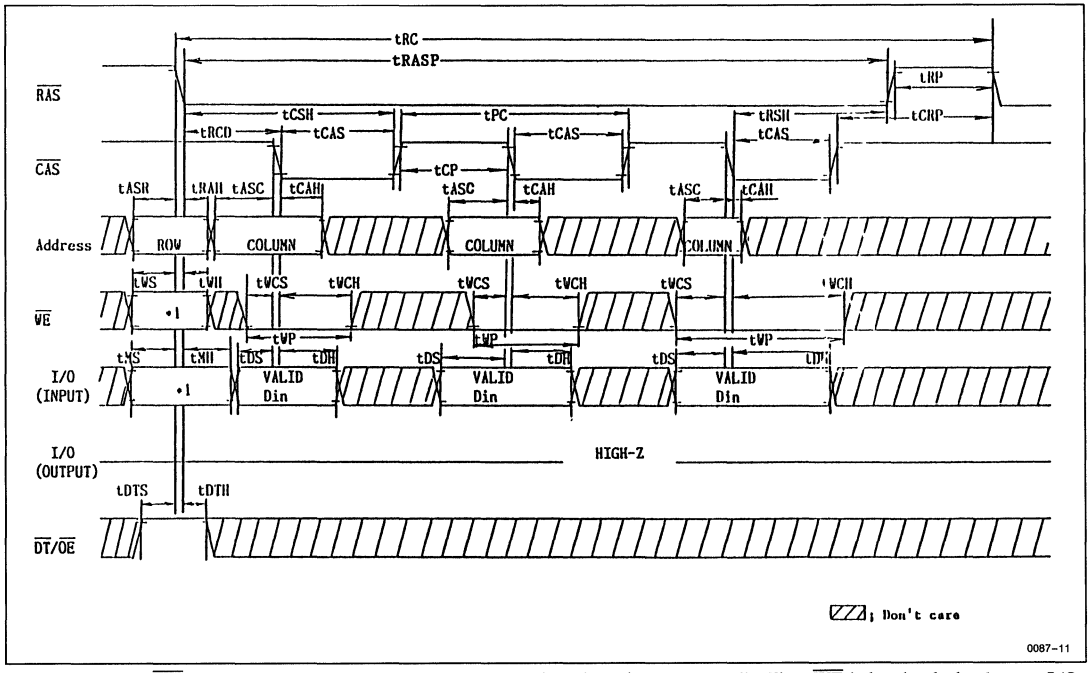


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Page Mode Read Cycle**

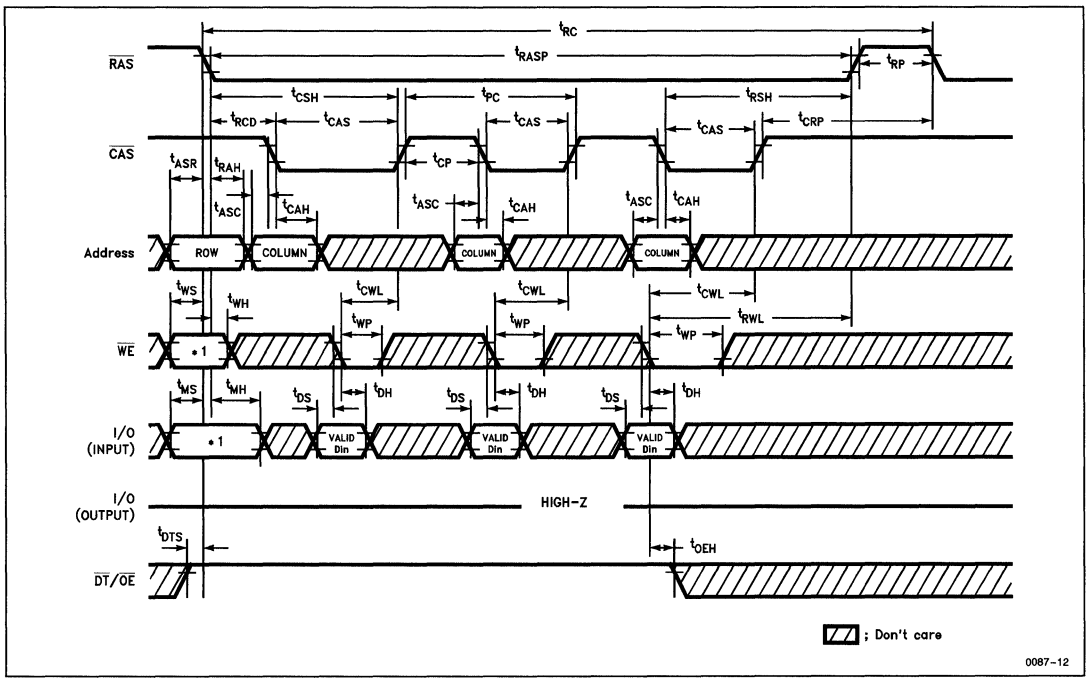


• **Page Mode Write Cycle (Early Write)**



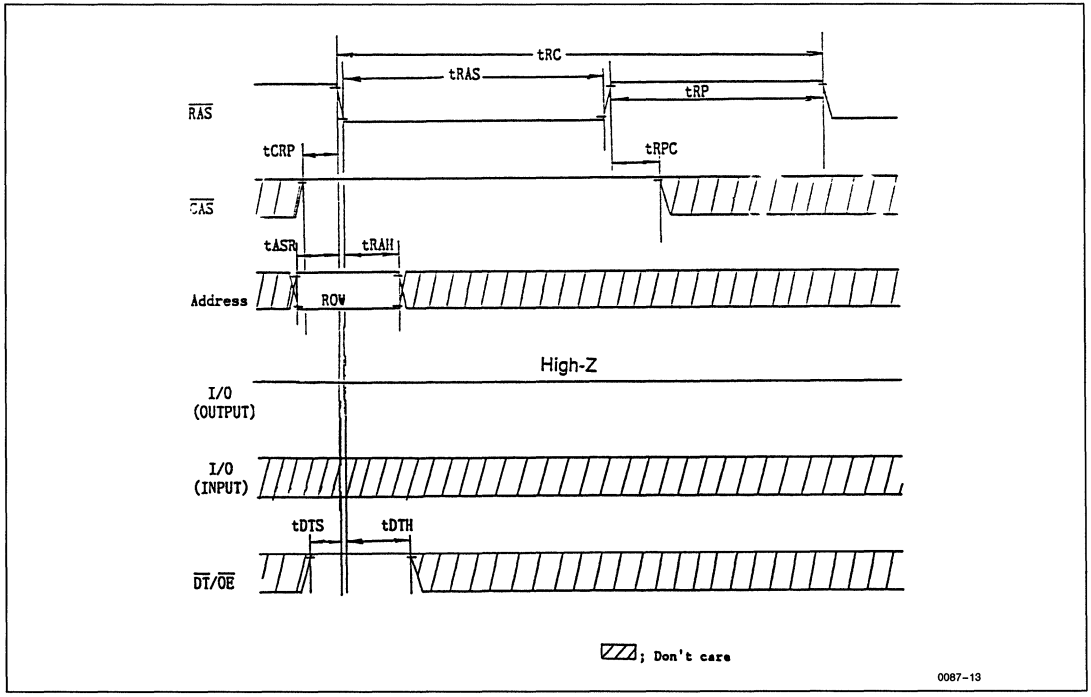
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• Page Mode Write Cycle (Delayed Write)

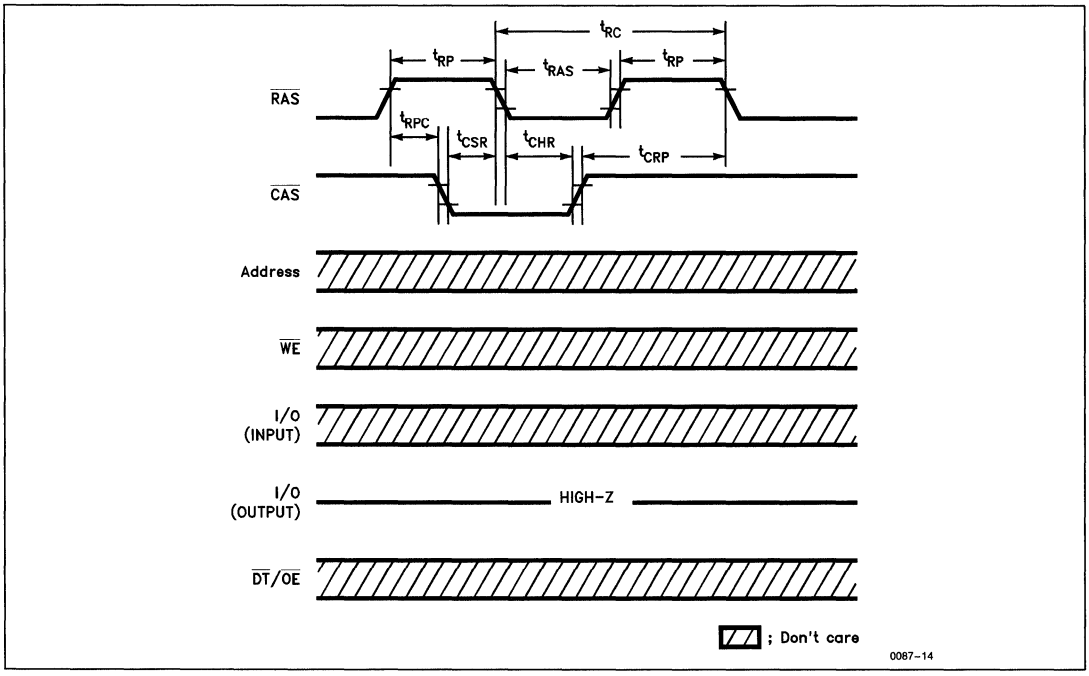


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

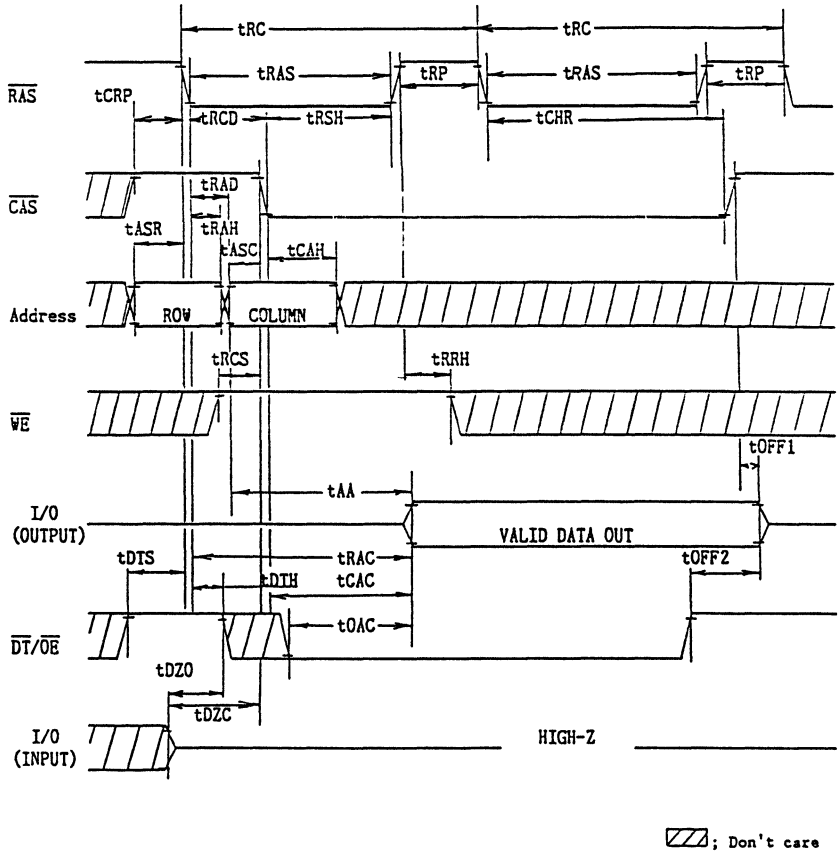
• $\overline{RAS}$ Only Refresh Cycle



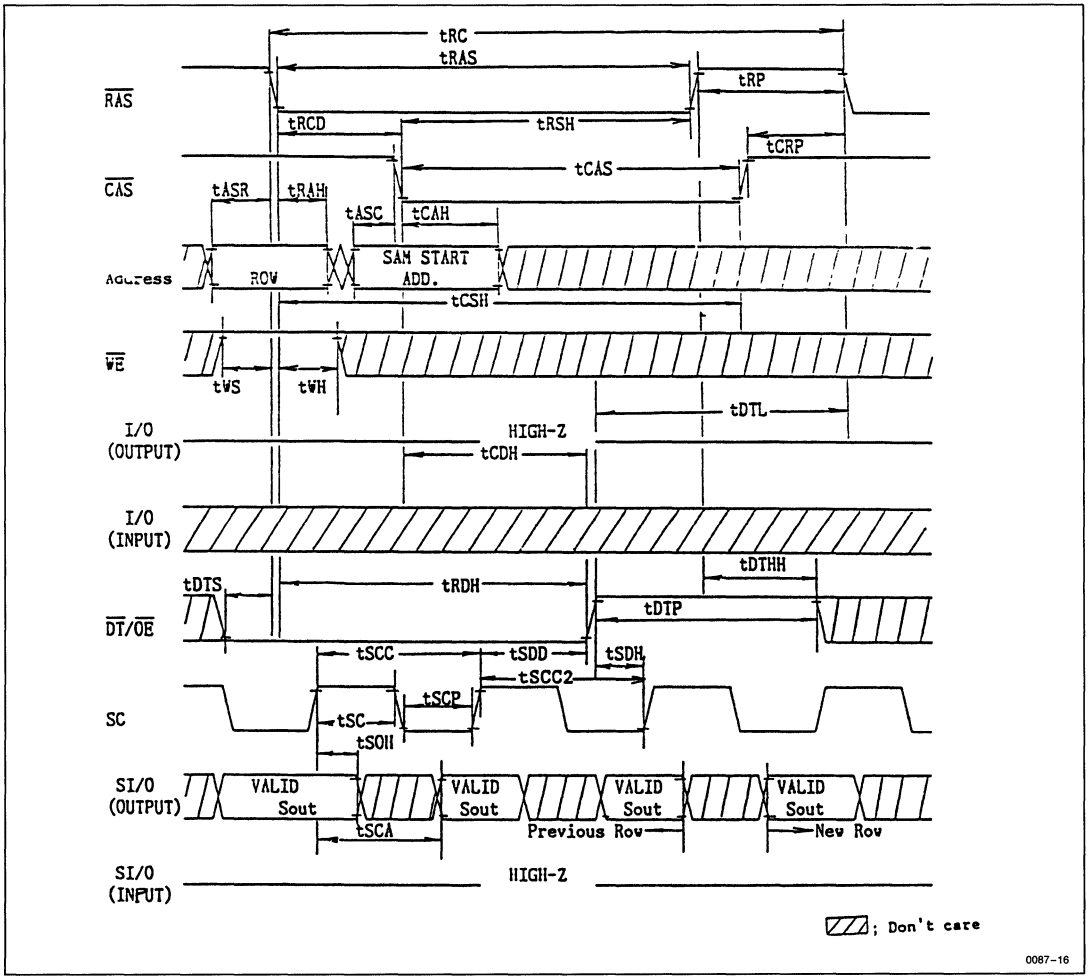
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• **Hidden Refresh Cycle**

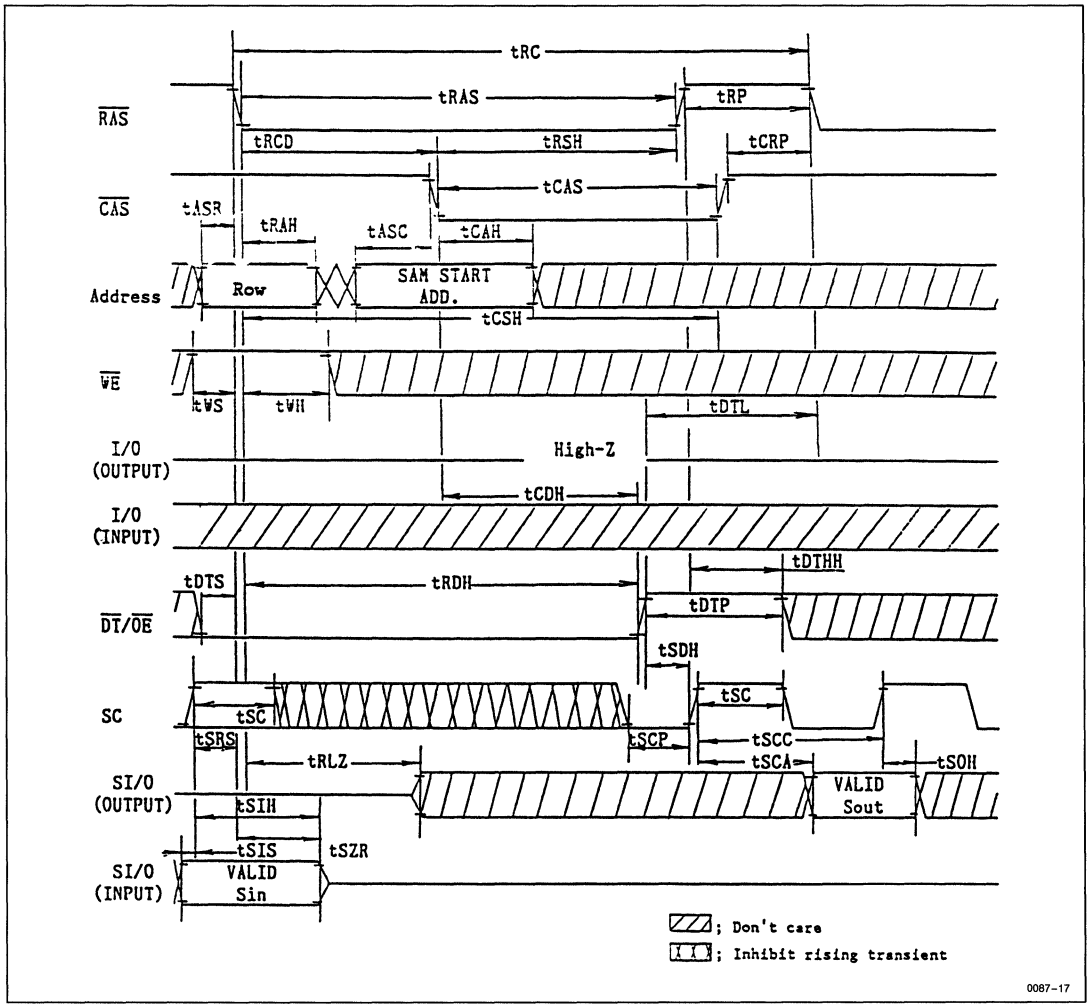


• **Read Transfer Cycle (1) 1, 2**



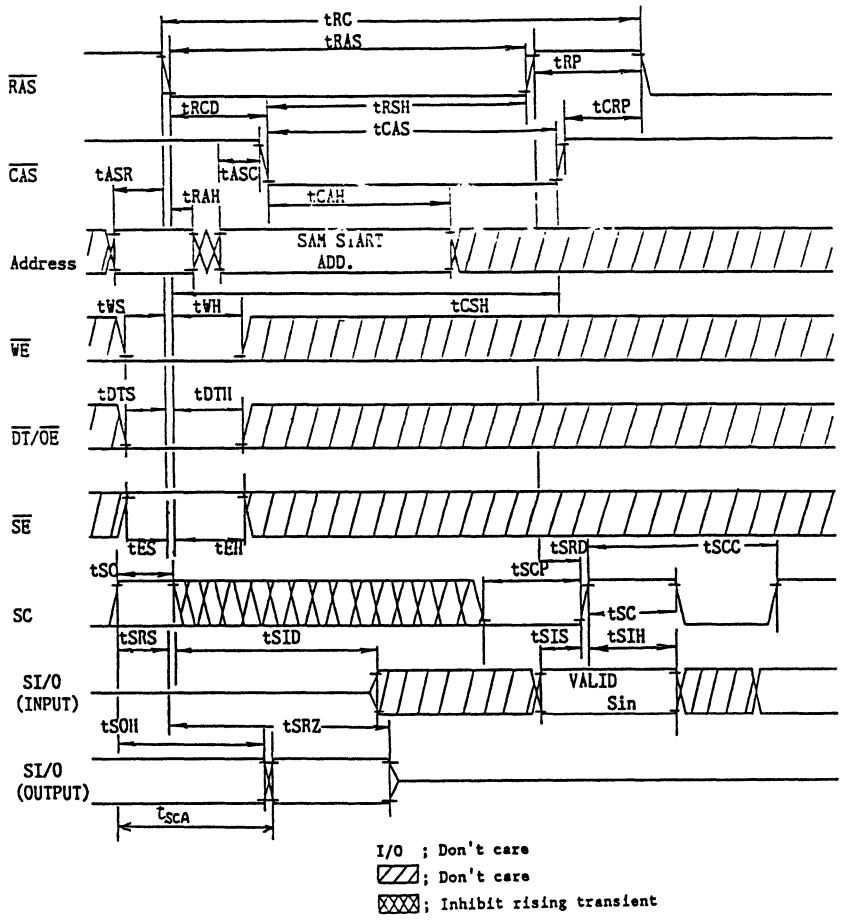
Notes: 1. When the previous data transfer cycle is a read transfer cycle, it is defined as read transfer cycle (1).
2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)

• **Read Transfer Cycle (2) 1, 2**

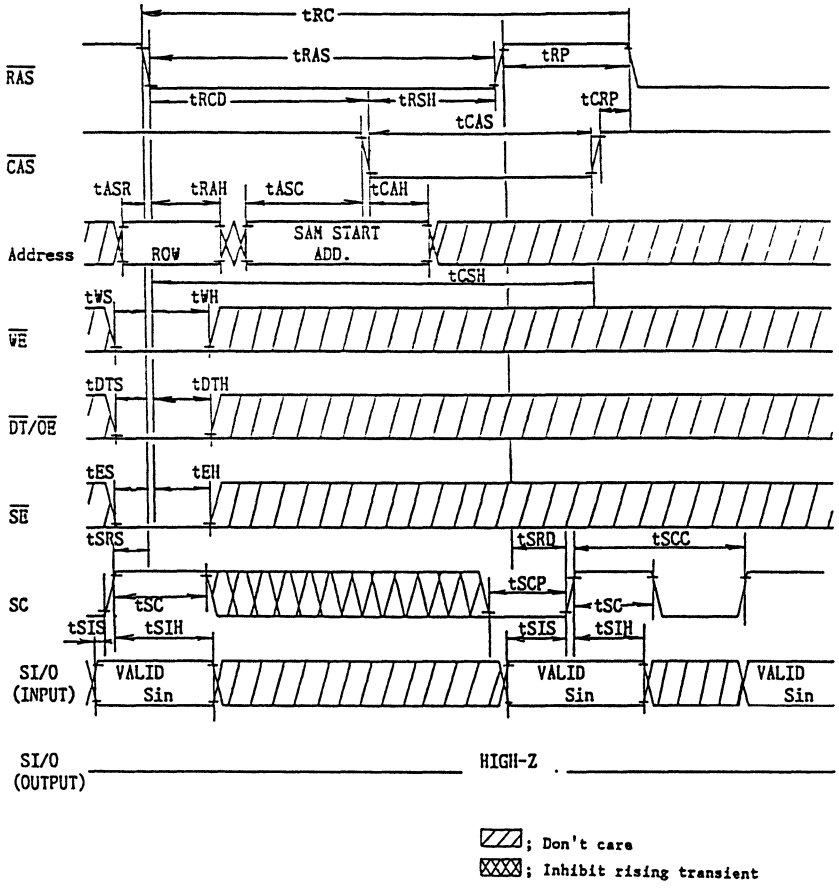


Notes: 1. When the previous data transfer cycle is a write or pseudo transfer cycle, it is defined as read transfer cycle (2).
2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)

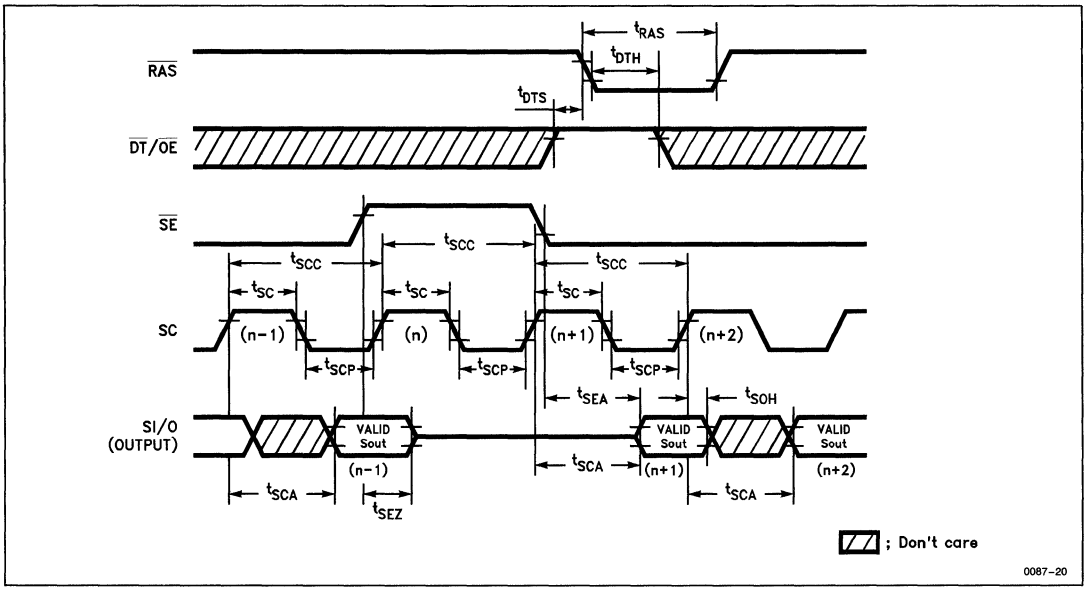
• **Pseudo Transfer Cycle**



• **Write Transfer Cycle**

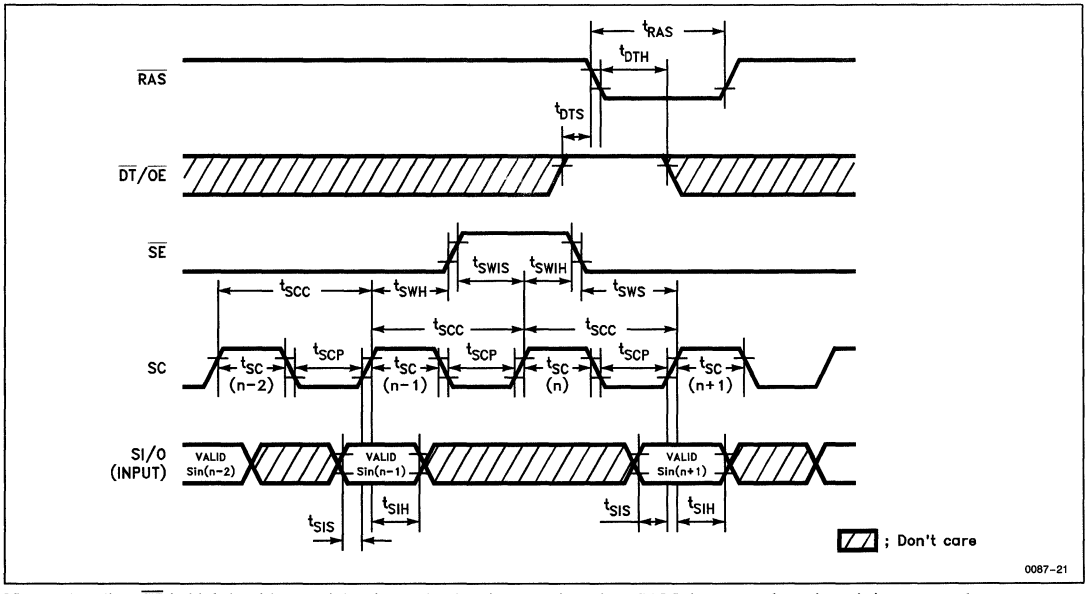


• **Serial Read Cycle**



Note: 1. Address 0 is accessed next to address 255.

• **Serial Write Cycle**



Note: 1. When $\overline{SE}$ is high level in a serial write cycle, data is not written into SAM, however, the pointer is incremented.
2. Address 0 is accessed next to address 255.

HM538121A Series — Preliminary

262,144-Word x 4-Bit Multiport CMOS Video RAM

■ DESCRIPTION

The HM538121A is a 1-Mbit multiport video RAM equipped with a 128k-word x 8-bit dynamic RAM and a 256-word x 8-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has write mask function.

■ FEATURES

- Multiport Organization
  - Asynchronous and Simultaneous Operation of RAM and SAM Capability
  - RAM: 128k-word x 8-bit and SAM: 256-word x 8-bit
- Access Time RAM .....80 ns/100 ns (max)
  SAM .....25 ns/25 ns (max)
- Cycle Time RAM.....150 ns/190 ns (min)
  SAM .....30 ns/30 ns (min)
- Low Power
  - Active RAM .....360 mW (max)
    SAM .....280 mW (max)
  - Standby.....38.5 mW (max)
- High-Speed Page Mode Capability
- Mask Write Mode Capability
- Bidirectional Data Transfer Cycle between RAM and SAM Capability
- Real Time Read Transfer Cycle Capability
- 3 Variations of Refresh (8 ms/512 cycles)
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- TTL Compatible

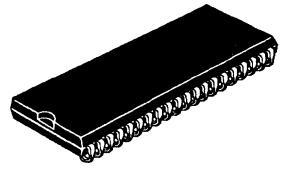
■ ORDERING INFORMATION

Part No.	Access Time	Package
HM538121AJ-8 HM538121AJ-10	80 ns 100 ns	400 mil 40-pin Plastic SOJ (CP-40D)
HM538121AZ-8 HM538121AZ-10	80 ns 100 ns	475 mil 40-pin Plastic ZIP (ZP-40)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Inputs
I/O_0–I/O_7	RAM Port Data Inputs/Outputs
SI/O_0–SI/O_7	SAM Port Data Inputs/Outputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{DT/OE}$	Data Transfer/Output Enable
SC	Serial Clock
$\overline{SE}$	SAM Port Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

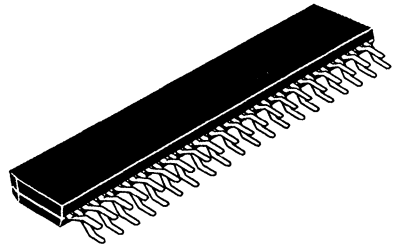
HM538121AJ Series



3DCP40D

(CP-40D)

HM538121AZ Series

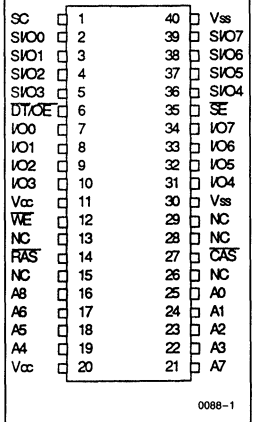


3DZP40

(ZP-40)

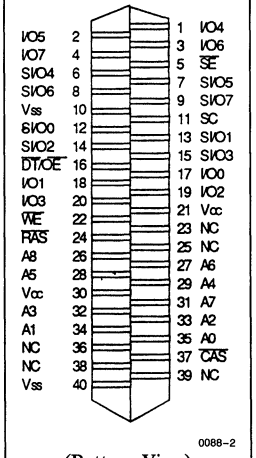
■ PIN OUT

HM538121AJ Series



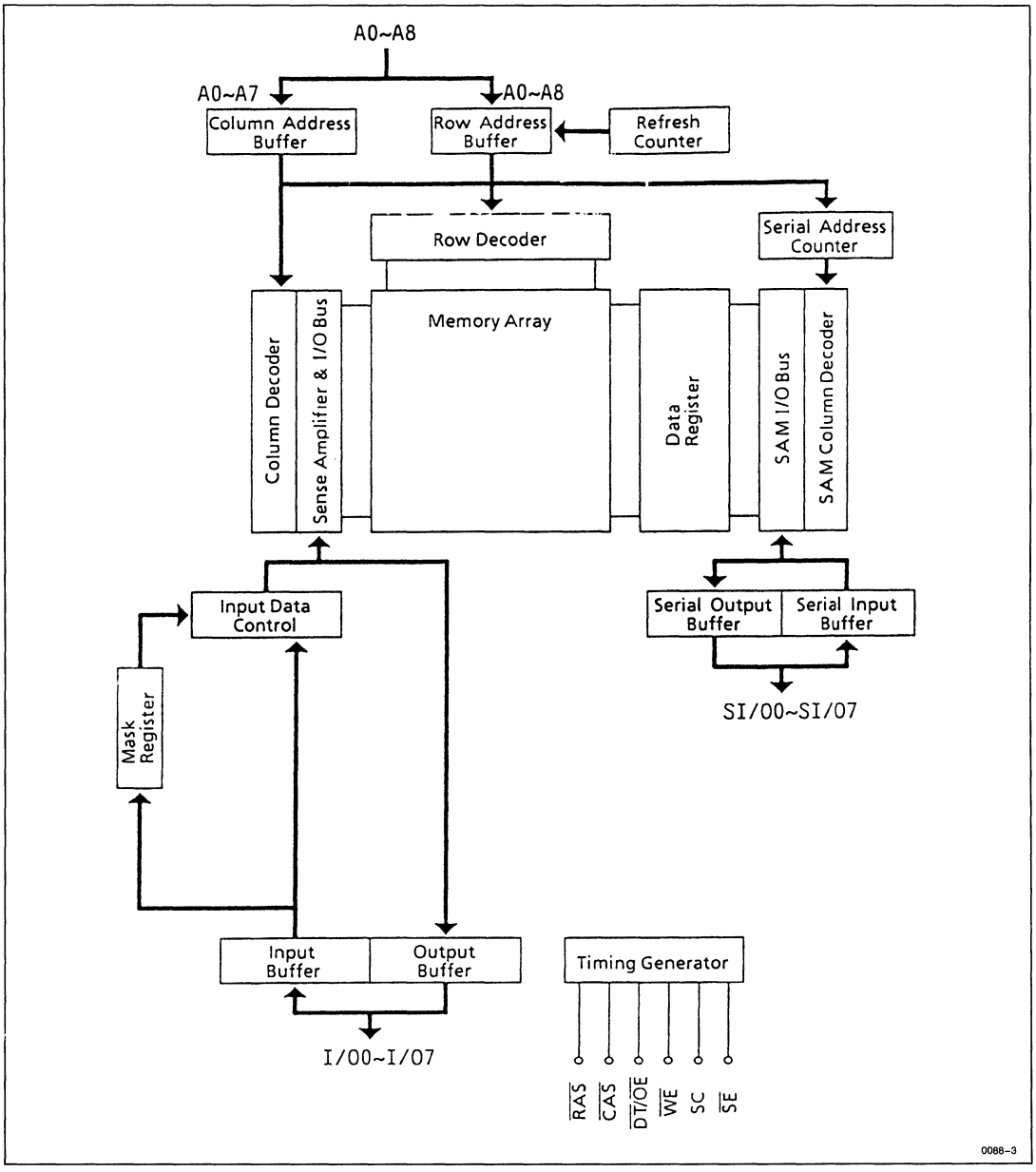
(Top View)

HM538121AZ Series



(Bottom View)

■ BLOCK DIAGRAM



■ PIN FUNCTIONS

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of these signals determine the operation cycle of the HM538121A.

• Table 1. Operation Cycles of the HM538121A

Input Level at the Falling Edge of $\overline{RAS}$				Operation Mode
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SE}$	
L	X	X	X	CBR Refresh
H	L	L	L	Write Transfer
H	L	L	H	Pseudo Transfer
H	L	H	X	Read Transfer
H	H	L	X	Read/Mask Write
H	H	H	X	Read/Write

Note: X: Don't care.

$\overline{CAS}$ (input pin): Column address is fetched into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A_0–A_8 (input pins): Row address (AX_0–AX_8), is determined by A_0–A_8 level at the falling edge of $\overline{RAS}$. Column (AY_0–AY_7) address is determined by A_0–A_8 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538121A turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O_0–I/O_3 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only to high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is fetched into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not fetched into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O_0–SI/O_7 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

■ OPERATION OF HM538121A

• RAM Read Cycle ($\overline{DT}/\overline{OE}$ high and $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

• RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write) ($\overline{DT}/\overline{OE}$ high and $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after driving $\overline{RAS}$ low, a write cycle is executed and I/O data is written in the selected addresses. When all 8 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes in high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables read/write at the same address in one cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is retained. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is retained during the page access.

• High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high and $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 256-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 μs).

• Transfer Operation

The HM538121A provides the read transfer cycle, pseudo transfer cycle and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{CAS}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle).

Read transfer cycle: RAM to SAM

Write transfer cycle: SAM to RAM

(2) Determine SI/O state

Read transfer cycle: SI/O output

Pseudo transfer cycle and write transfer cycle: SI/O input

(3) Determine first SAM address to access after transferring at column address (SAM start address).

SAM start address must be determined by read transfer cycle or pseudo transfer cycle after power on, and determined for each transfer cycle.

• Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address data (256 x 8-bit) determined by this cycle is transferred to SAM data register synchronously at the rising edge of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address determined by column address. In read transfer cycle, $\overline{DT}/\overline{OE}$ must be risen to transfer data from RAM to SAM.

This cycle can access SAM even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge and t_{SDH} (min) specified between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge must be satisfied. (See figure 1.)

When read transfer cycle is executed, SI/O becomes output state by first SAM access. Input must be set high impedance before t_{SZS} (min) of the first SAM access to avoid data contention.

• Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle switches SI/O to input state and set SAM start address without data transfer to RAM.

This cycle starts when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$. Data should be input to SI/O later than t_{SID} (min) after $\overline{RAS}$ becomes low to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC must not be risen.

• Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address for serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC must not be risen.

Data transferred to SAM by read transfer cycle can be written to other address of RAM by write transfer cycle. However, the address to write data must be the same MSB of row address (AX8) as that of the read transfer cycle.

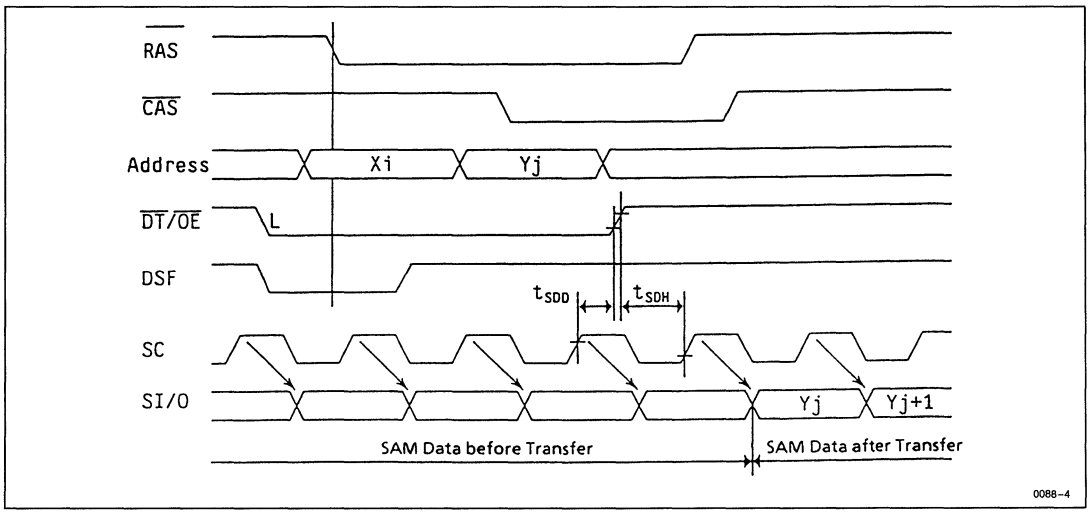


Figure 1. Real Time Read Transfer

• SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When $\overline{SE}$ is set high, SI/O becomes high impedance, and the internal pointer is incremented by the SC rising. After indicating the last address (address 255), the internal pointer indicates address 0 at the next access.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is fetched into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't fetched into data register. Internal pointer is incremented by the SC rising, so $\overline{SE}$ high can be used as mask data for SAM. After indicating the last address (address 255), the internal pointer indicates address 0 at the next access.

• Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is executed by accessing all 512 row addresses within 8 ms. There are three refresh cycles: (1) $\overline{RAS}$ only refresh cycle, (2) $\overline{CAS}$ before $\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required when all row addresses are accessed within 8 ms.

(1) $\overline{RAS}$ Only Refresh Cycle: $\overline{RAS}$ only refresh cycle is executed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high after inputting the row address (= refresh address) from external circuits. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ must be high at the falling edge of $\overline{RAS}$.

(2) CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.

(3) Hidden Refresh Cycle: Hidden refresh cycle executes CBR refresh with the data output by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register and selector), organized as fully static circuitry, require no refresh.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Note
Terminal Voltage	V_T	−1.0 to +7.0	V	1
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V	1
Power Dissipation	P_T	1.0	W	
Operating Temperature	T_{opr}	0 to +70	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

Note: 1. Relative to V_{SS}.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−0.5	—	0.8	V	1, 2

Notes: 1. All voltages referenced to V_{SS}.
2. −3.0V for pulse width 10 ns.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM538121A-8		HM538121A-10		Unit	Test Conditions	
		Min	Max	Min	Max		RAM Port	SAM Port
Operating Current	I_{CC1}	—	65	—	50	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC7}	—	115	—	100	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min
Standby Current	I_{CC2}	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC8}	—	50	—	50	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	65	—	50	mA	$\overline{RAS}$ Cycling $\overline{CAS}$ = V_{IH} t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC9}	—	115	—	100	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min

• **DC Electrical Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V) (continued)

Parameter	Symbol	HM538121A-8		HM538121A-10		Unit	Test Conditions	
		Min	Max	Min	Max		RAM Port	SAM Port
Page Mode Current	I_{CC4}	—	70	—	65	mA	$\overline{CAS}$ Cycling, $\overline{RAS}$ = V_{IL}, t_{PC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC10}	—	120	—	115	mA		$\overline{SE}$ = V_{IL}, SC Cycling, t_{SCC} = Min
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC5}	—	55	—	40	mA	$\overline{RAS}$ Cycling, t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC11}	—	105	—	90	mA		$\overline{SE}$ = V_{IL}, SC Cycling, t_{SCC} = Min
Data Transfer Current	I_{CC6}	—	75	—	60	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}
	I_{CC12}	—	125	—	110	mA		$\overline{SE}$ = V_{IL}, SC Cycling, t_{SCC} = Min
Input Leakage Current	I_{LI}	−10	10	−10	10	µA		
Output Leakage Current	I_{LO}	−10	10	−10	10	µA		
Output High Voltage	V_{OH}	2.4	—	2.4	—	V	I_{OH} = −2 mA	
Output Low Voltage	V_{OL}	—	0.4	—	0.4	V	I_{OL} = 4.2 mA	

Note: 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.

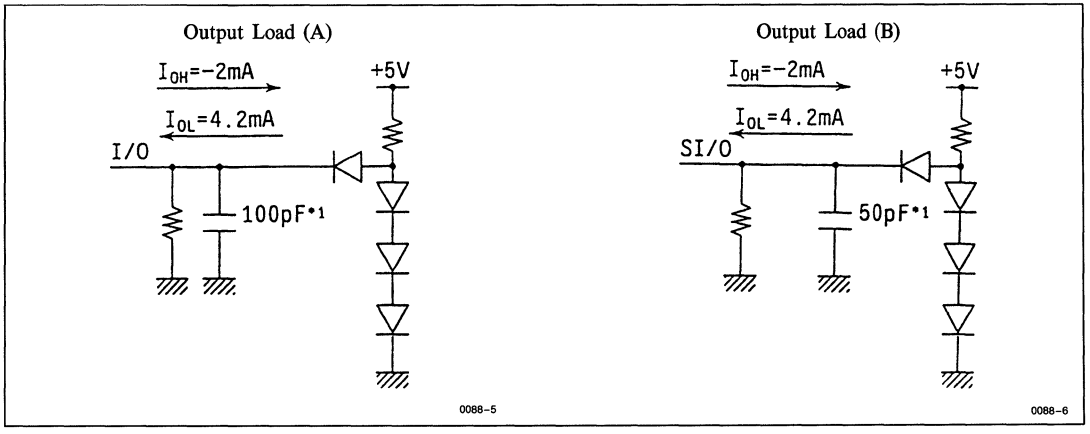
• **Capacitance** (T_A = 25°C, V_{CC} = 5V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, Address = V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O, QSF	$C_{I/O}$	—	—	7	pF

• **AC Electrical Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 16]

Test Conditions

Input Rise and Fall Time	5 ns
Output Load	See figures
Input Timing Reference Levels	0.8V, 2.4V
Output Timing Reference Levels	0.4V, 2.4V



Note: *1. Including scope and jig.

Common Parameter

Parameter	Symbol	HM538121A-8		HM538121A-10		Unit	Note
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	150	—	190	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	—	25	—	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	60	25	75	ns	2
$\overline{RAS}$ Hold Time Referenced to $\overline{CAS}$	t_{RSH}	20	—	25	—	ns	
$\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$	t_{CSH}	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	ns	
Transition Time (Rise to Fall)	t_T	3	50	3	50	ns	3
Refresh Period	t_{REF}	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	10	—	15	—	ns	
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	ns	4
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	ns	4
Output Buffer Turn-off Delay Referenced to $\overline{CAS}$	t_{OFF1}	—	20	—	25	ns	5
Output Buffer Turn-off Delay Referenced to $\overline{OE}$	t_{OFF2}	—	20	—	25	ns	5

Read Cycle (RAM), Page Mode Read Cycle

Parameter	Symbol	HM538121A-8		HM538121A-10		Unit	Note
		Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	25	ns	7, 8
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	25	ns	7
Address Access Time	t_{AA}	—	40	—	45	ns	7, 9
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	ns	10
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	ns	10
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	40	20	55	ns	2
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	ns	
Column Address to $\overline{CAS}$ Lead Time	t_{CAL}	40	—	45	—	ns	
Page Mode Cycle Time	t_{PC}	50	—	55	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	45	—	50	ns	
Page Mode $\overline{RAS}$ Pulse Width	t_{RASP}	80	100000	100	100000	ns	

Write Cycle (RAM), Page Mode Write Cycle

Parameter	Symbol	HM538121A-8		HM538121A-10		Unit	Note
		Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	ns	11
Write Command Hold Time	t_{WCH}	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	ns	12
Data-in Hold Time	t_{DH}	15	—	20	—	ns	12
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	10	—	15	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	10	—	15	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	20	—	25	—	ns	
Page Mode Cycle Time	t_{PC}	50	—	55	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
$\overline{CAS}$ to Data-in Delay Time	t_{CDD}	20	—	25	—	ns	13
Page Mode $\overline{RAS}$ Pulse Width	t_{RASP}	80	100000	100	100000	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM538121A-8		HM538121A-10		Unit	Note
		Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	200	—	250	—	ns	
$\overline{RAS}$ Pulse Width (Read-Modify-Write Cycle)	t_{RWS}	130	10000	160	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	45	—	55	—	ns	14
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	65	—	75	—	ns	14
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	20	—	25	—	ns	12
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	25	ns	7, 8
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	25	ns	7
Address Access Time	t_{AA}	—	40	—	45	ns	7, 9
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	40	20	55	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	ns	12
Data-in Hold Time	t_{DH}	15	—	20	—	ns	12
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM538121A-8		HM538121A-10		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	15	—	20	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	ns	

Read Transfer Cycle

Parameter	Symbol	HM538121A-8		HM538121A-10		Unit	Note
		Min	Max	Min	Max		
$\overline{DT}$ Hold Time Referenced to $\overline{RAS}$	t_{RDH}	70	10000	90	10000	ns	
$\overline{DT}$ Hold Time Referenced to $\overline{CAS}$	t_{CDH}	20	—	25	—	ns	
$\overline{DT}$ Hold Time Referenced to Column Address	t_{ADH}	30	—	35	—	ns	
$\overline{DT}$ Precharge Time	t_{DTP}	40	—	45	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Delay Time	t_{DRD}	70	—	90	—	ns	
SC to $\overline{RAS}$ Setup Time	t_{SRS}	30	—	30	—	ns	
1st SC to $\overline{RAS}$ Hold Time	t_{SRH}	85	—	105	—	ns	
1st SC to $\overline{CAS}$ Hold Time	t_{SCH}	30	—	35	—	ns	
1st SC to Column Address Hold Time	t_{SAH}	50	—	55	—	ns	
Last SC to $\overline{DT}$ Delay Time	t_{SDD}	5	—	5	—	ns	
1st SC to $\overline{DT}$ Hold Time	t_{SDH}	15	—	15	—	ns	
Serial Data-in to 1st SC Delay Time	t_{SZS}	0	—	0	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	30	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	ns	
SC Precharge Time	t_{SCP}	10	—	10	—	ns	
SC Access Time	t_{SCA}	—	25	—	25	ns	15
Serial Data-out Hold Time	t_{SOH}	5	—	5	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	40	20	55	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	ns	
$\overline{DT}$ High Hold Time to $\overline{RAS}$ Precharge	t_{DTHH}	25	—	30	—	ns	

Pseudo Transfer Cycle, Write Transfer Cycle

Parameter	Symbol	HM538121A-8		HM538121A-10		Unit	Note
		Min	Max	Min	Max		
$\overline{SE}$ Setup Time Referenced to $\overline{RAS}$	t_{ES}	0	—	0	—	ns	
$\overline{SE}$ Hold Time Referenced to $\overline{RAS}$	t_{EH}	10	—	15	—	ns	
SC Setup Time Referenced to $\overline{RAS}$	t_{SRS}	30	—	30	—	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	—	25	—	ns	
Serial Output Buffer Turn-off Time Referenced to $\overline{RAS}$	t_{SRZ}	10	45	10	50	ns	
$\overline{RAS}$ to Serial Data-in Delay Time	t_{SID}	45	—	50	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	30	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	ns	
SC Precharge Time	t_{SCP}	10	—	10	—	ns	
SC Access Time	t_{SCA}	—	25	—	25	ns	15
$\overline{SE}$ Access Time	t_{SEA}	—	25	—	25	ns	15
Serial Data-out Hold Time	t_{SOH}	5	—	5	—	ns	
Serial Write Enable Setup Time	t_{SWS}	5	—	5	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	ns	

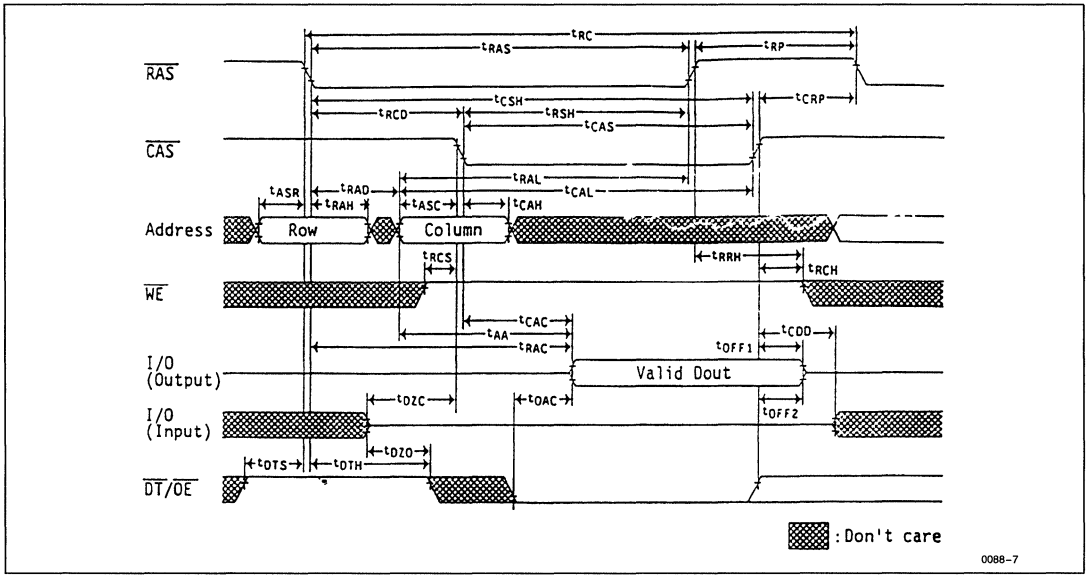
Serial Read Cycle, Serial Write Cycle

Parameter	Symbol	HM538121A-8		HM538121A-10		Unit	Note
		Min	Max	Min	Max		
Serial Clock Cycle Time	t_{SCC}	30	—	30	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	ns	
Access Time from SC	t_{SCA}	—	25	—	25	ns	15
Access Time from $\overline{SE}$	t_{SEA}	—	25	—	25	ns	15
Serial Data-out Hold Time	t_{SOH}	5	—	5	—	ns	
Serial Output Buffer Turn-off Time Referenced to $\overline{SE}$	t_{SEZ}	—	20	—	25	ns	5
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	ns	
Serial Data-in Hold time	t_{SIH}	15	—	20	—	ns	
Serial Write Enable Setup Time	t_{SWS}	5	—	5	—	ns	
Serial Write Enable Hold Time	t_{SWH}	15	—	20	—	ns	
Serial Write Disable Setup Time	t_{SWIS}	5	—	5	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	15	—	20	—	ns	

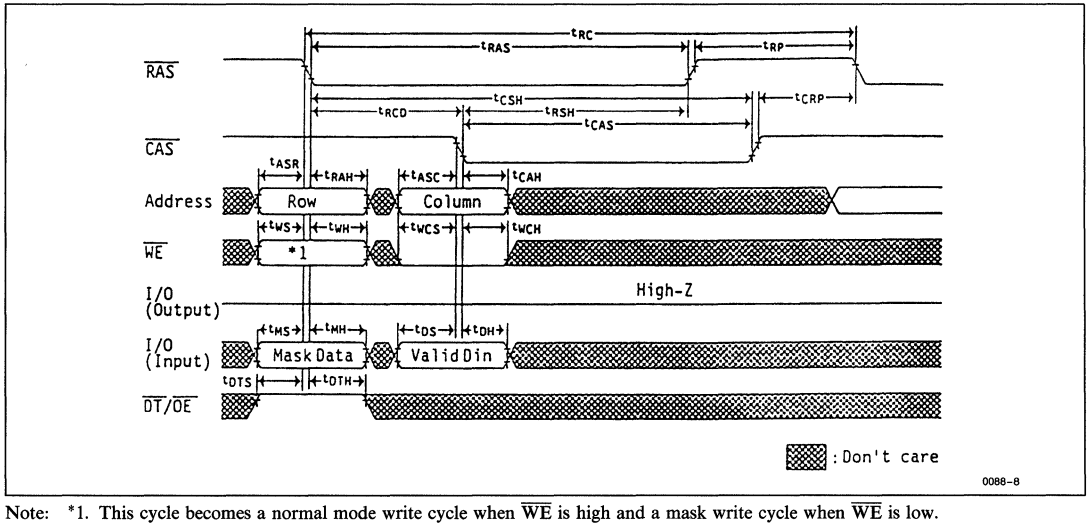
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. When $t_{RCD} > t_{RCD}$ (max) or $t_{RAD} > t_{RAD}$ (max), access time is specified by t_{CAC} or t_{AA}.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition time t_T is measured between V_{IH} and V_{IL}.
4. Data input must be floating before output buffer is turned on. In read cycle, read-modify-write cycle and delayed write cycle, either t_{DZC} (min) or t_{DZO} (min) must be satisfied.
5. t_{OFF1} (max), t_{OFF2} (max) and t_{SEZ} (max) are defined as the time at which the output achieves the open circuit condition ($V_{OH} - 200$ mV, $V_{OL} + 200$ mV).
6. Assume that $t_{RCD} > t_{RCD}$ (max) and $t_{RAD} > t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
8. When $t_{RCD} > t_{RCD}$ (max) and $t_{RAD} > t_{RAD}$ (max), access time is specified by t_{CAC}.
9. When $t_{RCD} > t_{RCD}$ (max) and $t_{RAD} > t_{RAD}$ (max), access time is specified by t_{AA}.
10. If either t_{RCH} of t_{RRH} is satisfied, operation is guaranteed.
11. When $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
12. These parameters are specified by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
13. Either t_{CDD} (min) or t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{CAS}$ or $\overline{OE}$ prior to applying data to the device when output buffer is on.
14. When $t_{AWD} > t_{AWD}$ (min) and $t_{CWD} > t_{CWD}$ (min) in read-modify-write cycle, the data of the selected address outputs to an I/O pin and input data is written into the selected address. t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{OE}$ prior to applying data to the device.
15. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
16. After power-up, pause for 100 μs or more and execute at least 8 initialization cycles (normal memory cycle or refresh cycle), then start operation.

■ TIMING WAVEFORMS

• Read Cycle

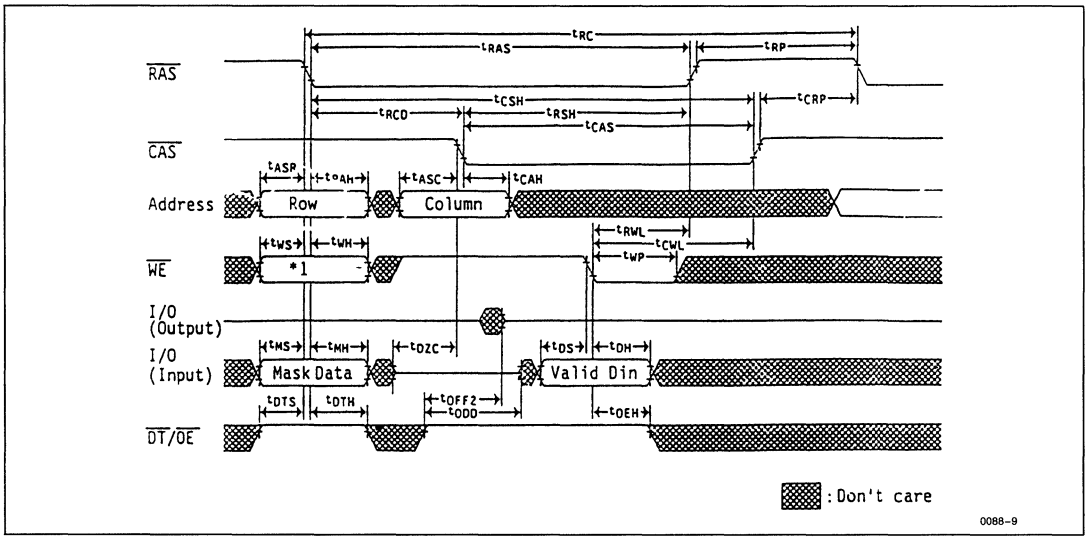


• Early Write Cycle



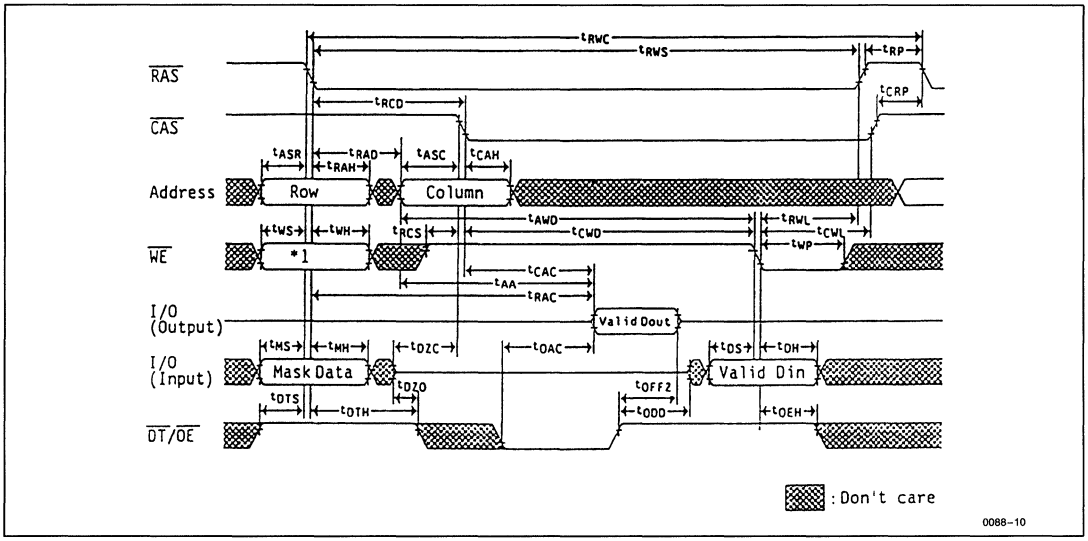
Note: *1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

• **Delayed Write Cycle**



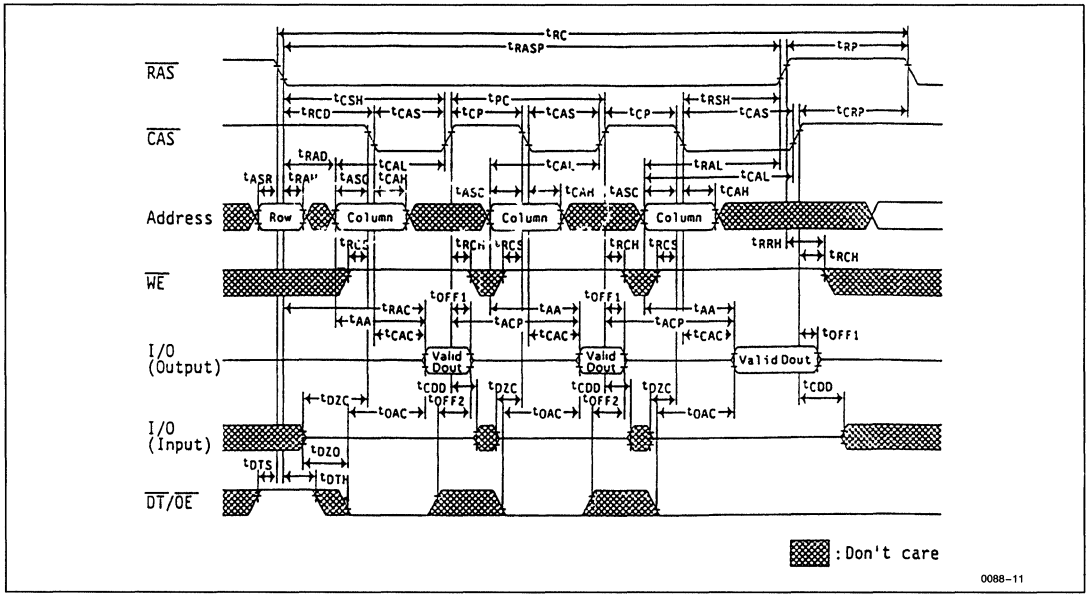
Note: *1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

• **Read-Modify-Write Cycle**

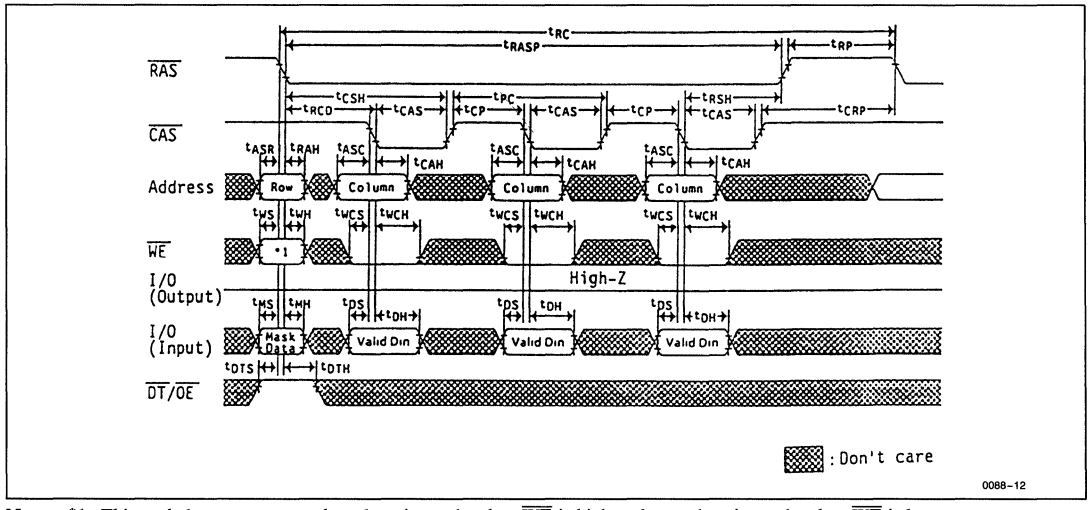


Note: *1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

• **Page Mode Read Cycle**

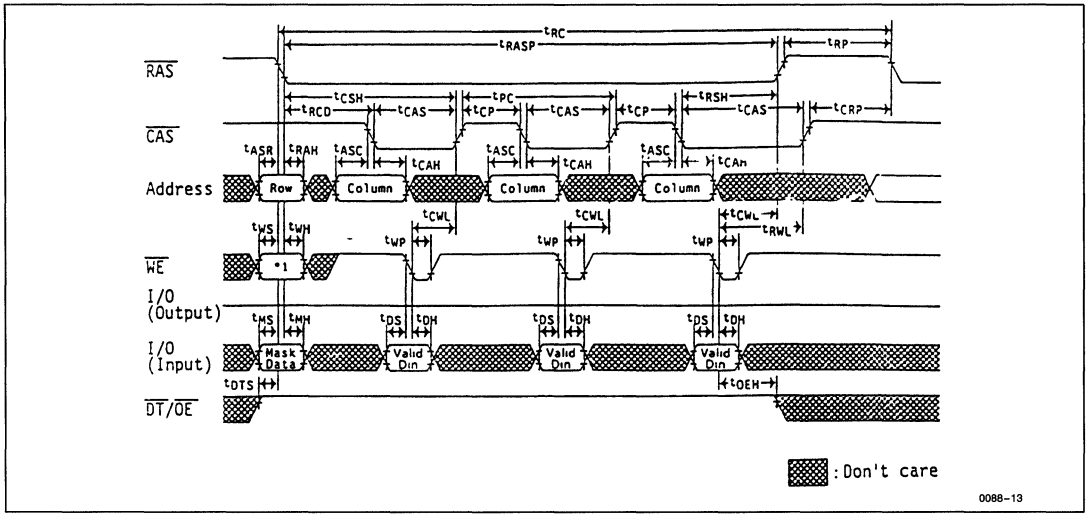


• **Page Mode Write Cycle (Early Write)**



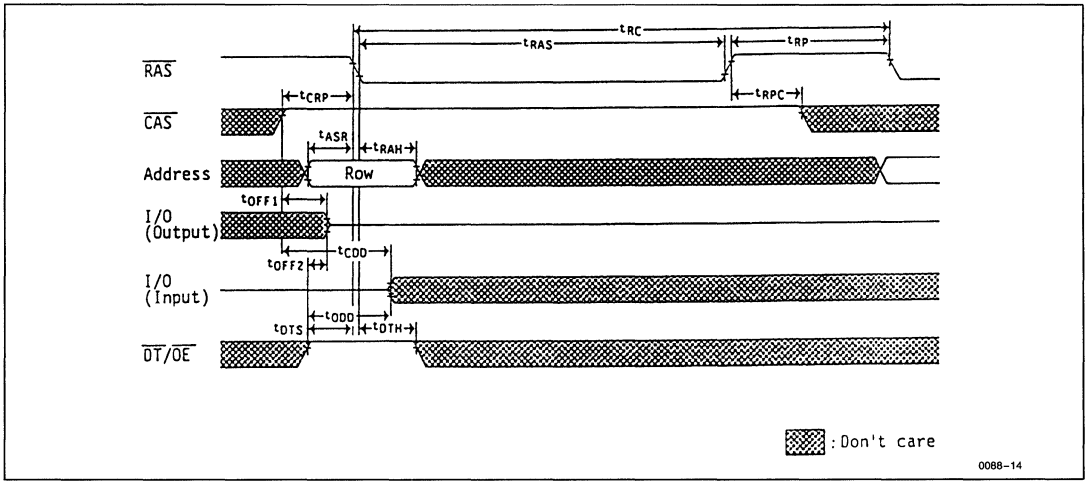
Note: *1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

• **Page Mode Write Cycle (Delayed Write)**

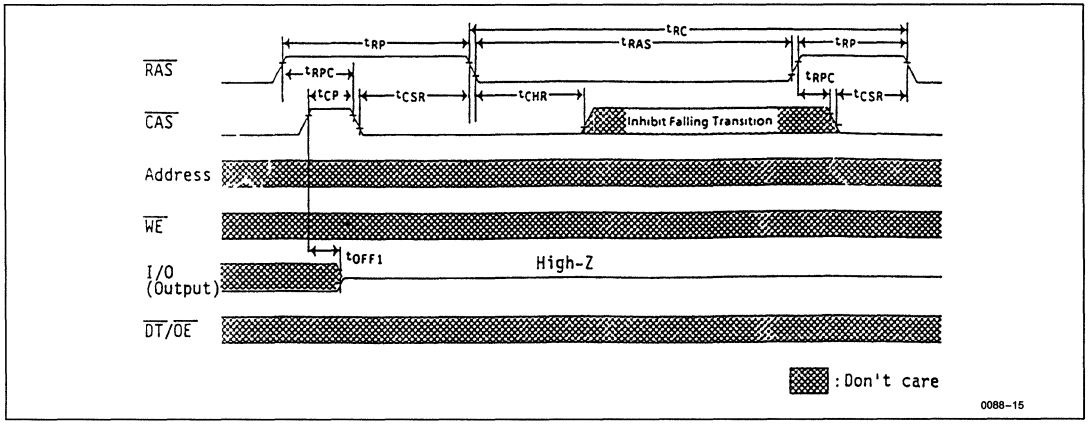


Note: *1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

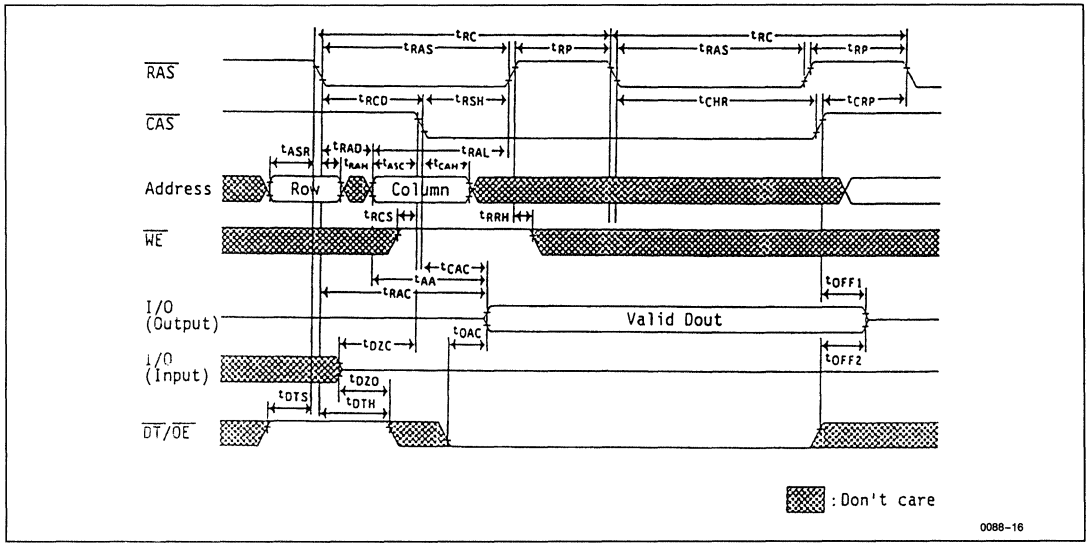
• **$\overline{RAS}$ Only Refresh Cycle**



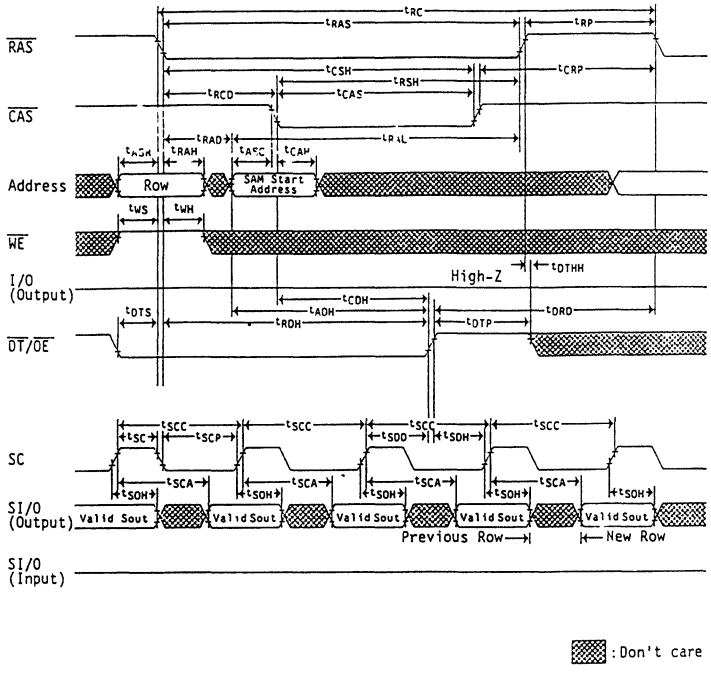
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



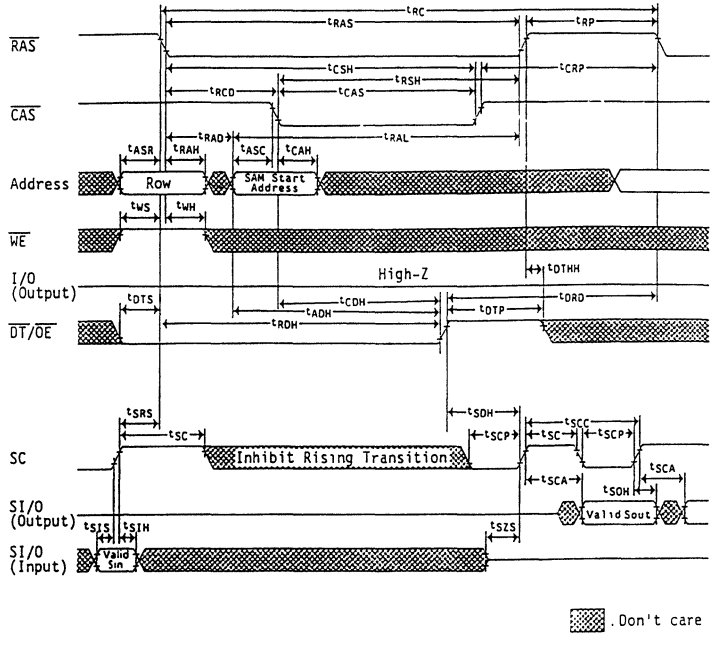
• Hidden Refresh Cycle



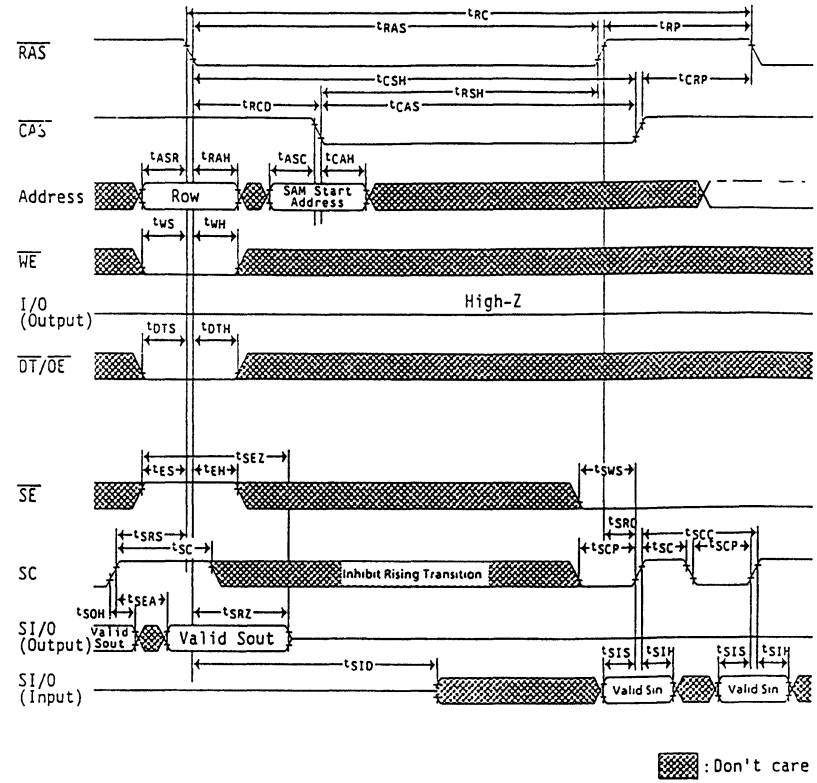
• **Read Transfer Cycle (1)**



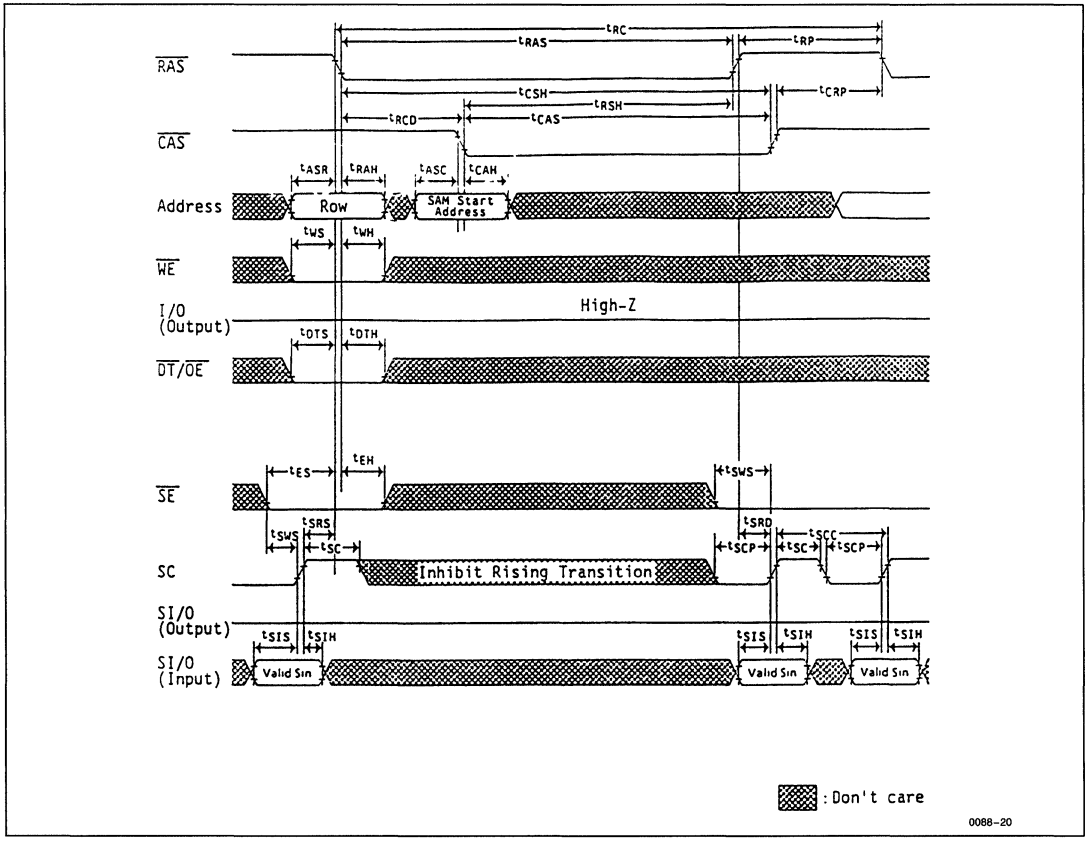
• **Read Transfer Cycle (2)**



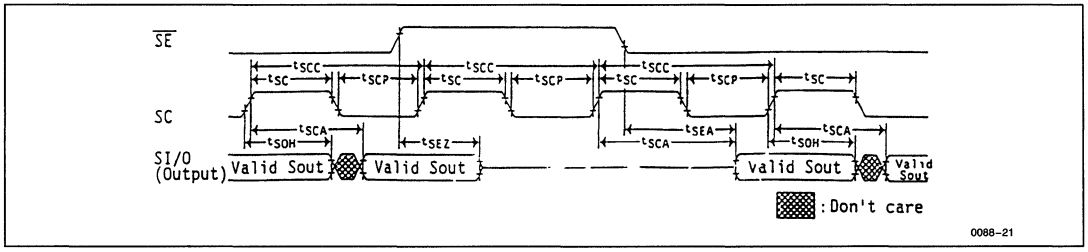
• **Pseudo Transfer Cycle**



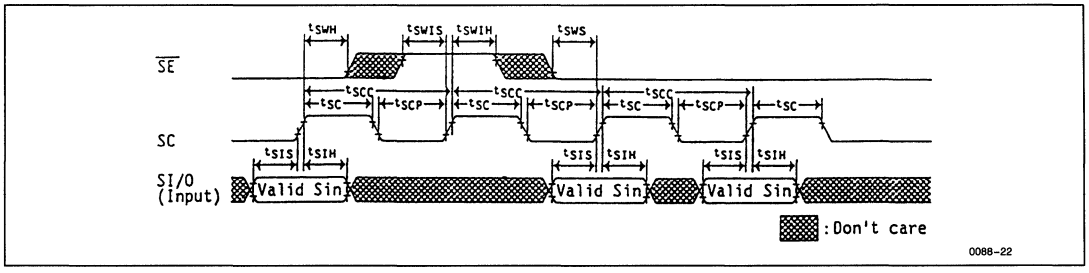
• **Write Transfer Cycle**



• **Serial Read Cycle**



• **Serial Write Cycle**



HM538122 Series — Preliminary

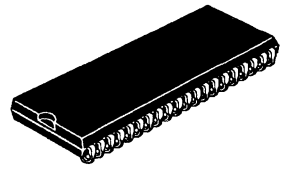
131,072 x 8-Bit Multiport CMOS Video Random Access Memory

■ DESCRIPTION

The HM538122 is a 1-Mbit multiport video RAM equipped with a 128k-word x 8-bit dynamic RAM and a 256-word x 8-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has a write mask function.

It also provides logic operation mode to simplify its operation. In this mode, logic operation between memory data and input data can be executed by using internal logic-arithmetic unit.

HM538122JP Series



3DCP40D

(CP-40D)

■ FEATURES

- Multiport Organization
  - Asynchronous and Simultaneous Operation of RAM and SAM Capability
  - RAM ..... 128k-word x 8-Bit
  - SAM ..... 256-word x 8-Bit
- Access Time RAM ..... 100 ns/100 ns/120 ns/150 ns (max)
  - SAM ..... 30 ns/35 ns/40 ns/50 ns (max)
- Cycle Time RAM ..... 190 ns/190 ns/220 ns/260 ns (min)
  - SAM ..... 30 ns/40 ns/40 ns/60 ns (min)
- Low Power
  - Active RAM ..... 495 mW (max)
  - SAM ..... 468 mW (max)
  - Standby ..... 40 mW (max)
- High-Speed Page Mode Capability
- Logic Operation Mode Capability
- 2 Types of Mask Write Mode Capability
- Bidirectional Data Transfer Cycle between RAM and SAM Capability
- Real Time Read Transfer Capability
- 3 Variations of Refresh (8 ms/512 Cycles)
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- TTL Compatible

■ ORDERING INFORMATION

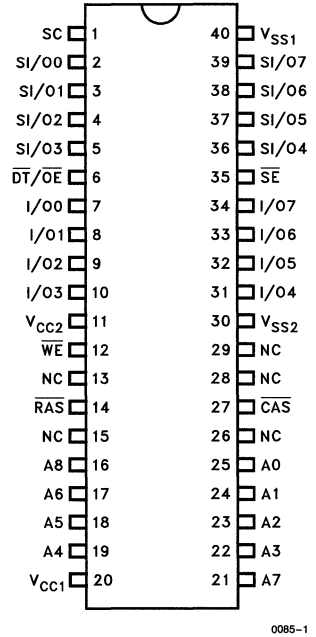
Part No.	Access Time		Package
	RAM	SAM	
HM538122JP-10	100 ns	30 ns	400 mil
HM538122JP-11	100 ns	35 ns	40-pin
HM538122JP-12	120 ns	40 ns	Plastic SOJ
HM538122JP-15	150 ns	50 ns	(CP-40D)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Inputs
I/O_0–I/O_7	RAM Port Data Inputs/Outputs
SI/O_0–SI/O_7	SAM Port Data Inputs/Outputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
$\overline{DT/OE}$	Data Transfer/Output Enable
SC	Serial Clock
$\overline{SE}$	SAM Port Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	Non Connection

■ PIN OUT

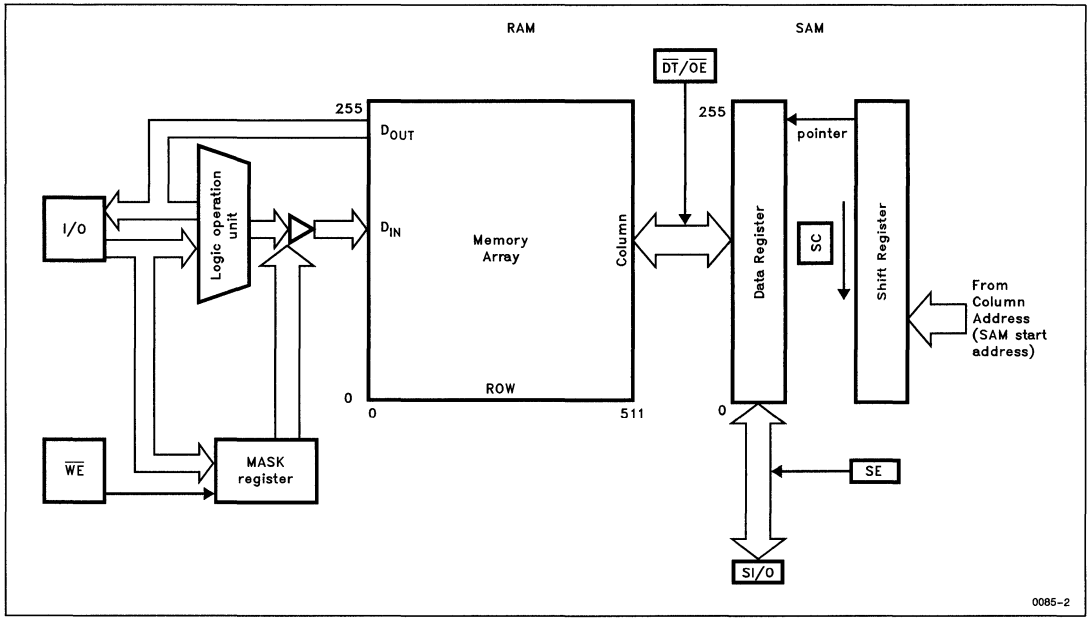
HM538122JP Series



0085-1

(Top View)

■ BLOCK DIAGRAM



■ PIN FUNCTION

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of those signals determine the operation cycle of the HM538122.

• Table 1. Operation Cycles of the HM538122

Input Level At The Falling Edge of $\overline{RAS}$				Operation Cycle
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SE}$	
H	H	H	X	RAM Read/Write
H	H	L	X	Mask Write
H	L	H	X	Read Transfer
H	L	L	H	Pseudo Transfer
H	L	L	L	Write Transfer
L	X	H	X	CBR Refresh
L	X	L	X	Logic Operation Set/Reset

Note: X: Don't care.

$\overline{CAS}$ (input pin): Column address is put into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A_0–A_8 (input pins): Row address is determined by A_0–A_8 level at the falling edge of $\overline{RAS}$. Column address is determined by A_0–A_7 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538122 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O_0–I/O_7 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only on high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data is output from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is put into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not put into the SAM data register in serial

write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O_0–SI/O_7 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

■ OPERATION OF HM538122

• Operation of RAM Port

RAM Read Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high, at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data is output through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write)

($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after $\overline{RAS}$ is set low, a write cycle is executed and I/O data is written at the selected addresses. When all 8 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling edge. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables write after read to execute in the same address cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and setting $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is preserved. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is preserved during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle and is higher than the standard page mode cycle by 70%–80%. This product is based on static column mode, therefore address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 256-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 μs), t_{RFSP} max (100 μs).

• Transfer Operation

HM538122 provides the transfer cycle, pseudo transfer cycle, and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$.

They have the following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)

(2) Determine direction of data transfer

(a) Read transfer cycle: RAM → SAM

(b) Write transfer cycle: RAM ← SAM

(3) Determine input or output of SAM I/O pin (SI/O)

Read transfer cycle: SI/O output

Pseudo transfer cycle, write transfer cycle: SI/O input

(4) Determine first SAM address to access (SAM start address) after transferring at column address.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address data (256 x 8-bit) determined by this cycle is transferred synchronously at the rising of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address determined by column address.

This cycle can access SAM serially even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) is specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge, and t_{SDH} (min) between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge (see figure 1).

If read transfer cycle is executed, SI/O becomes output state. When the previous transfer cycle is either pseudo transfer cycle or write transfer cycle and SI/O is in input state, uncertain data is output after t_{RLZ} (min) after the $\overline{RAS}$ falling edge. Before that, input should be set high impedance to avoid data contention.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle is available for switching SI/O from output state to input state because data in RAM isn't rewritten. This cycle starts when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high, at the falling edge of $\overline{RAS}$. The output buffer in SI/O becomes high impedance within t_{SRZ} (max) from the $\overline{RAS}$ falling edge. Data should be input to SI/O later than t_{SID} (min) to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC should not be raised.

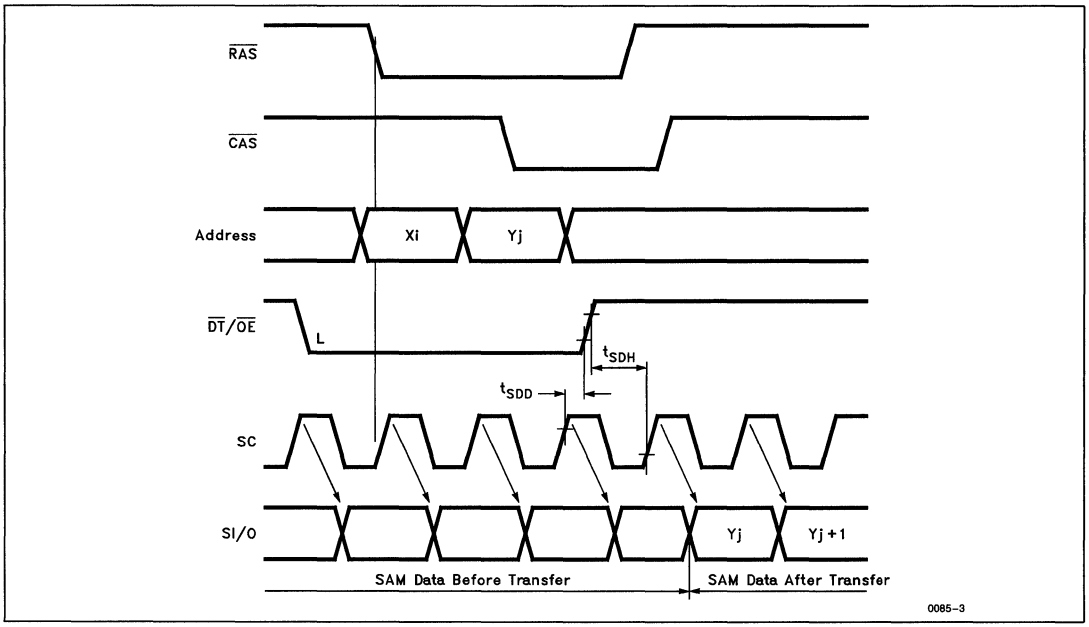


Figure 1. Real Time Read Transfer

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address to serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC should not be raised.

• SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. If $\overline{SE}$ is set high SI/O becomes high impedance and internal pointer is incremented at the SC rising edge.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is programmed into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't input into data register. Internal pointer is incremented according to the SC rising edge, so $\overline{SE}$ high can mask data for SAM.

• Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is performed by accessing all 512 row addresses every 8 ms. There are three refresh cycles: (1) $\overline{RAS}$ only refresh cycle, (2) $\overline{CAS}$ before $\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required when all row addresses every 8 ms.

$\overline{RAS}$ Only Refresh Cycle: $\overline{RAS}$ only refresh cycle is performed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high by inputting the row address (= refresh address) from external circuits.
To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ should be high at the falling edge of $\overline{RAS}$.

CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.
To distinguish this cycle from logic operation set/reset cycle, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$.

Hidden Refresh Cycle: Hidden refresh cycle performs refresh by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register, selector), organized as fully static circuitry, don't require refresh.

• Logic Operation Mode

The HM538122 supports logic operation capability on RAM port. It performs logic operations between the memory cell data and input data in logic operation mode cycle, and writes the result into the memory cell (read-modify-write). This function realizes high speed raster operations and simplifies peripheral circuits for raster operations.

Logic Operation Set/Reset Cycle ($\overline{CAS}$ and $\overline{WE}$ Low at the falling edge of $\overline{RAS}$)

In logic operation set/reset cycle, the following operations are performed at the same time; 1. Selection of logic operations and logic operation mode set/reset, 2. Mask data programming, 3. $\overline{CAS}$ before $\overline{RAS}$ refresh.

Figure 2 shows the timing for logic operation set/reset cycle. This cycle starts when $\overline{CAS}$ and $\overline{WE}$ are low at the falling edge of $\overline{RAS}$. In this cycle, logic operation codes and mask data are programmed by row address and I/O pin at the falling edge of $\overline{RAS}$ respectively. When write cycle is performed after this cycle, the logic operation write cycle starts. In the logic operation mode, the specification of cycle time is longer than that of normal mode because read-modify-write cycle is performed internally. In this cycle, logic operation codes and mask data programmed are available until reprogrammed. In normal mode, mask data is available only for one $\overline{RAS}$ cycle. Here, the mask data programmed in normal mode is named as "temporary mask data" and the one programmed in logic operation set/reset cycle is named as "mask data".

(1) Selection of logic operations and logic operation mode set/reset

Table 2 shows the logic operations. One operation is selected among sixteen ones by combinations of A_0–A_3 levels at the falling edge of $\overline{RAS}$. (A_4–A_8 are Don't care.) Logic operation codes (A3, A2, A1, A0) = (0, 1, 0, 1) resets the logic operation mode. When write cycle is performed after that, normal write cycle starts. However, even in this case, mask data is still available. I/O should be at high level at the falling edge of $\overline{RAS}$ in logic operation set/reset cycle when mask data is not used.

(2) Mask data programming

High/low level of I/O at the falling edge of $\overline{RAS}$ functions as mask data. When I/O is high, the data is written in write cycle. When I/O is low, the input data is masked and the same memory cell data remains. Mask data, programmed in this cycle, is available until reprogrammed. It is advantageous when the same mask data continues.

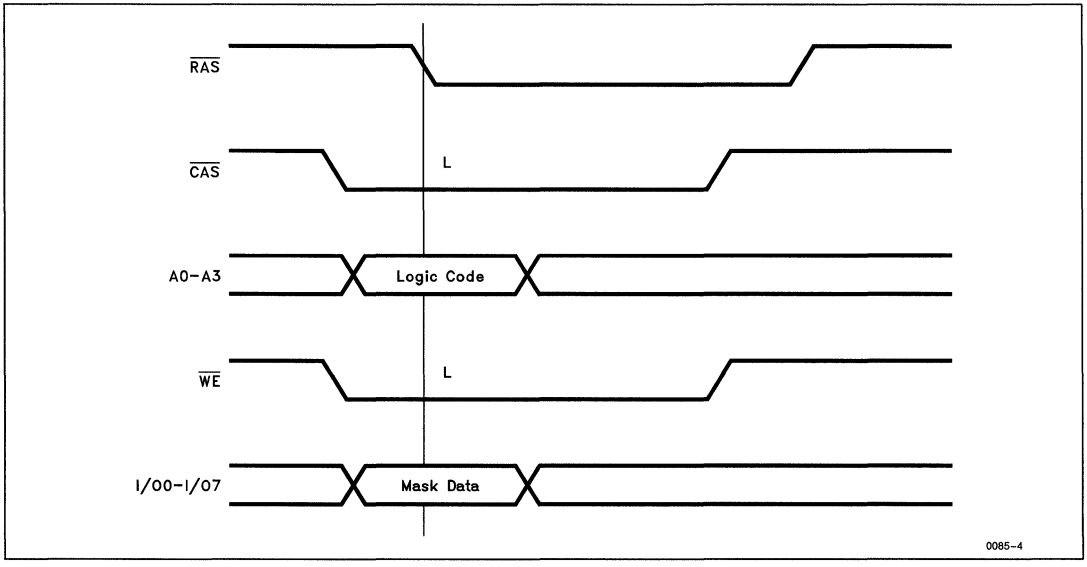


Figure 2. Logic Operation Set/Reset

• Table 2. Logic Code

Logic Code				Symbol	Write Data	Notes
A3	A2	A1	A0			
0	0	0	0	Zero	0	Logic Operation Mode Set
0	0	0	1	AND1	$Di \cdot Mi$	
0	0	1	0	AND2	$\overline{Di} \cdot Mi$	
0	0	1	1	—	Mi	
0	1	0	0	AND3	$Di \cdot \overline{Mi}$	
0	1	0	1	THROUGH	Di	Logic Operation Mode Reset
0	1	1	0	EOR	$\overline{Di} \cdot Mi + Di \cdot \overline{Mi}$	Logic Operation Mode Set
0	1	1	1	OR1	$Di + Mi$	
1	0	0	0	NOR	$\overline{Di} \cdot \overline{Mi}$	
1	0	0	1	ENOR	$Di \cdot Mi + \overline{Di} \cdot \overline{Mi}$	
1	0	1	0	INV1	$\overline{Di}$	
1	0	1	1	OR2	$\overline{Di} + Mi$	
1	1	0	0	INV2	$\overline{Mi}$	
1	1	0	1	OR3	$Di + \overline{Mi}$	
1	1	1	0	NAND	$\overline{Di} + \overline{Mi}$	
1	1	1	1	One	1	

Notes: Di: External data-in
Mi: The data of the memory cell

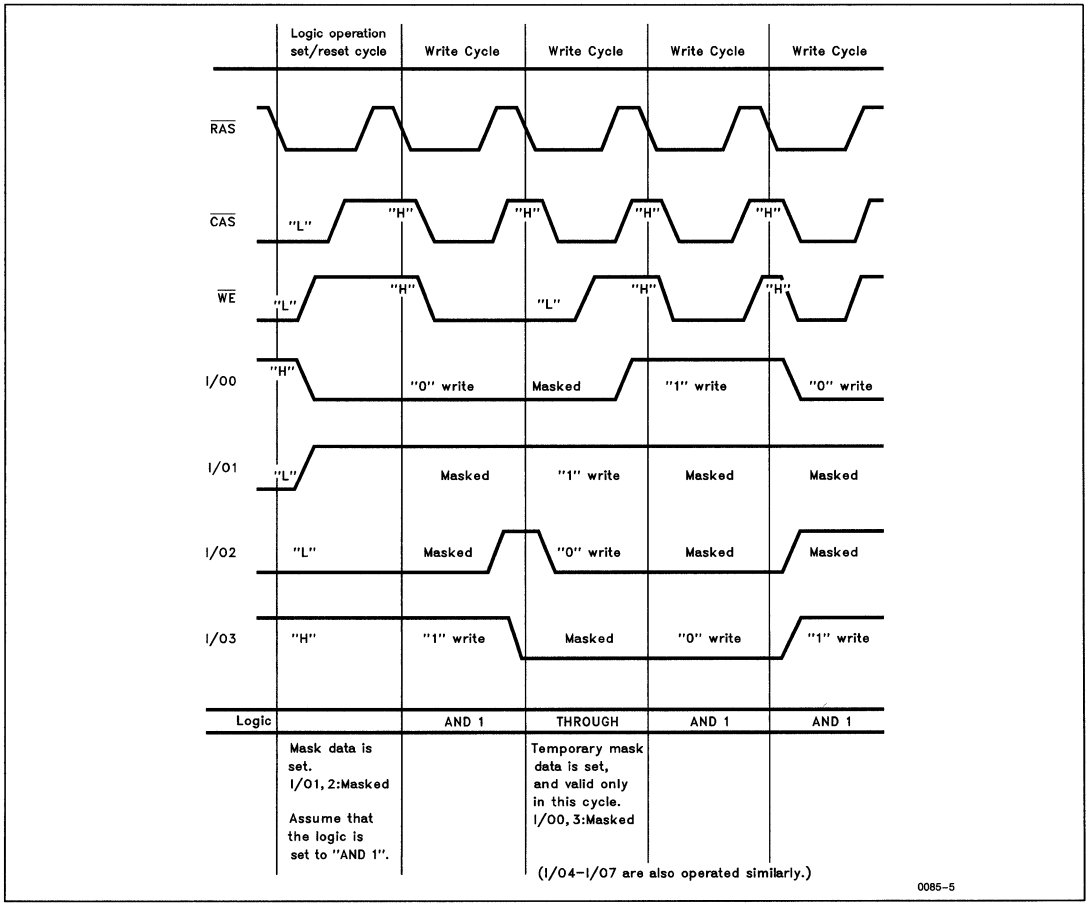


Figure 3. 2 Types of Mask Write Function and Logic Operation Function

Also, temporary mask data is programmed by falling $\overline{WE}$ at the falling edge of $\overline{RAS}$ in logic operation mode cycle after mask data is programmed in logic operation set/reset cycle. In this case, temporary mask data is available only for one cycle.

Logic operation is reset during temporary mask write cycle. It means that external input data is written into I/O when temporary mask data is set. Figure 4 shows write mask and logic operations. These functions are useful when RAM port is deviced into frame buffer area and data area, as they save the need to reprogram logic operation codes and mask data.

Write Cycle in Logic Operation Mode (Early Write, Delayed Write, Page Mode)

Write cycle after logic operation set cycle is logic operation mode cycle. In this cycle, the following read-modify-write operation is performed internally.

(1) Reading memory data in given address into internal bus

(2) Performing operation between input data and memory data

(3) Writing the result of (2) into address given by (1)

Figure 4 shows sequence of raster operation. Raster operation which needs 3 cycles (destination read, operation, destination write) in normal mode can be executed in one write cycle of logic operation mode. It makes raster operation faster and simplifies peripheral hardware for raster operation.

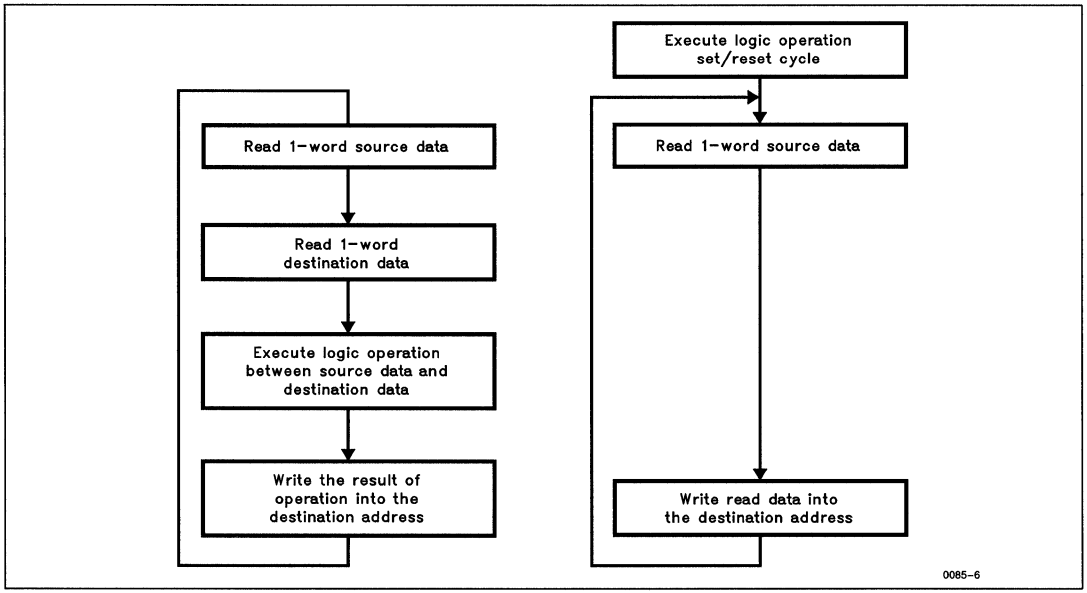


Figure 4. Sequence of Raster Operation

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Note
Terminal Voltage	V_T	−1.0 to +7.0	V	1
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V	1
Power Dissipation	P_T	1.0	W	
Operating Temperature	T_{opr}	0 to +70	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

Note: 1. Relative to V_{SS}.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−0.5	—	0.8	V	1, 2

Notes: 1. All voltages referenced to V_{SS}.
2. −3.0V for pulse width 10 ns.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM538122-10		HM538122-11		HM538122-12		HM538122-15		Unit	Test Conditions		Note
		Min	Max	Min	Max	Min	Max	Min	Max		RAM Port	SAM Port	
Operating Current	I_{CC1}	—	90	—	90	—	80	—	70	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	1, 2
	I_{CC7}	—	160	—	160	—	140	—	120	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Standby Current	I_{CC2}	—	7	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}	1
	I_{CC8}	—	85	—	70	—	70	—	55	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	90	—	90	—	80	—	70	mA	$\overline{RAS}$ Cycling $\overline{CAS}$ = V_{IH} t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	1, 2
	I_{CC9}	—	150	—	150	—	130	—	110	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Page Mode Current	I_{CC4}	—	115	—	115	—	105	—	95	mA	$\overline{CAS}$ Cycling $\overline{RAS}$ = V_{IL} t_{PC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	1, 3
	I_{CC10}	—	185	—	185	—	160	—	140	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC5}	—	80	—	80	—	70	—	60	mA	$\overline{RAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	1
	I_{CC11}	—	130	—	130	—	110	—	90	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Data Transfer Current	I_{CC6}	—	115	—	115	—	110	—	100	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	1, 2
	I_{CC12}	—	185	—	185	—	160	—	140	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	−10	10	μA			
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	−10	10	μA			
Output High Voltage	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V	I_{OH} = −2 mA		
Output Low Voltage	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA		

Notes: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition ($I_{I/O}$ = $I_{SI/O}$ = 0 mA).
2. Address can be changed less than three times in one $\overline{RAS}$ cycle.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. I_{CC2} and I_{CC8} are measured with address fixed.

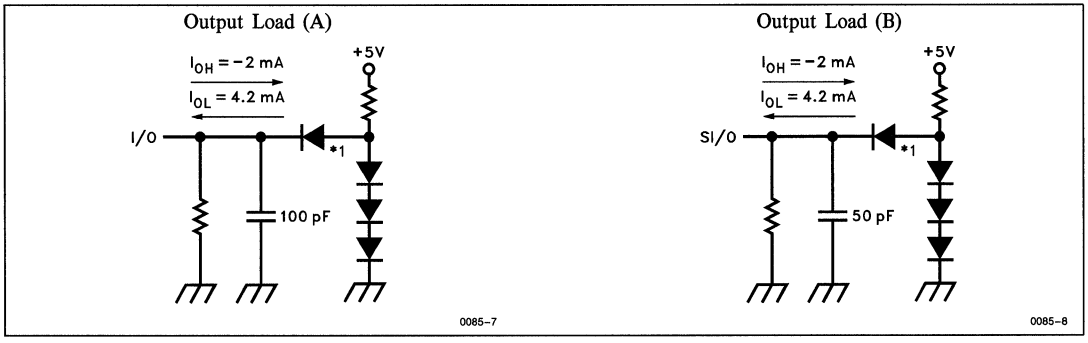
• **Capacitance** (T_A = 25°C, V_{CC} = 5V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, Address = V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clocks	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

• **AC Electrical Characteristics** (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 11]

Test Conditions

Input Rise and Fall Time	5 ns
Output Load	See figures
Input Timing Reference Levels	0.8V, 2.4V
Output Timing Reference Levels	0.4V, 2.4V



Note: *1. Including scope and jig.

Common Parameter

Parameter	Symbol	HM538122-10		HM538122-11		HM538122-12		HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	190	—	190	—	220	—	260	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	80	—	80	—	90	—	100	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	30	10000	30	10000	35	10000	40	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	15	—	20	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	70	25	70	25	85	30	110	ns	5, 6
$\overline{RAS}$ Hold Time	t_{RSH}	30	—	30	—	35	—	40	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise to Fall)	t_T	3	50	3	50	3	50	3	50	ns	8
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	—	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	—	15	—	15	—	20	—	ns	
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	0	—	0	—	ns	
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	0	—	0	—	ns	

Read Cycle (RAM), Page Mode Read Cycle

Parameter	Symbol	HM538122-10		HM538122-11		HM538122-12		HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	3, 5
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	45	—	55	—	70	ns	3, 6
Output Buffer Turn-off Delay Referenced to $\overline{CAS}$	t_{OFF1}	—	25	—	25	—	30	—	40	ns	7
Output Buffer Turn-off Delay Referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	7
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	0	—	ns	12
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20	55	20	55	20	65	25	80	ns	5, 6
Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	20	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	—	75	ns	
$\overline{RAS}$ Pulse Width in Page Mode	t_{RASP}	0.1	100	0.1	100	0.12	100	0.15	100	μs	

Write Cycle (RAM), Page Mode Write Cycle

Parameter	Symbol	HM538122-10		HM538122-11		HM538122-12		HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	9
Write Command Hold Time	t_{WCH}	25	—	25	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	25	—	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	
Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	20	—	ns	
$\overline{RAS}$ Pulse Width in Page Mode	t_{RASP}	0.1	100	0.1	100	0.12	100	0.15	100	μs	

Read-Modify-Write Cycle

Parameter	Symbol	HM538122-10		HM538122-11		HM538122-12		HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	255	—	255	—	295	—	350	—	ns	
$\overline{RAS}$ Pulse Width	t_{RWS}	165	10000	165	10000	195	10000	240	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	65	—	65	—	75	—	90	—	ns	9
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	80	—	80	—	95	—	120	—	ns	9

Read-Modify-Write Cycle (continued)

Parameter	Symbol	HM538122-10		HM538122-11		HM538122-12		HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	25	—	25	—	30	—	40	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	3, 5
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	45	—	55	—	70	ns	3, 6
$\overline{RAS}$ to Column Address Delay	t_{RAD}	20	55	20	55	20	65	25	80	ns	5, 6
Output Buffer Turn-off Delay Referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Write Command Pulse Width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	25	—	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	

Refresh Cycle

Parameter	Symbol	HM538122-10		HM538122-11		HM538122-12		HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	30	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

Transfer Cycle

Parameter	Symbol	HM538122-10		HM538122-11		HM538122-12		HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	15	—	20	—	ns	
$\overline{SE}$ to $\overline{RAS}$ Setup Time	t_{ES}	0	—	0	—	0	—	0	—	ns	
$\overline{SE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	—	15	—	15	—	20	—	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	—	30	—	30	—	35	—	ns	
SC to $\overline{RAS}$ Setup Time	t_{SRS}	30	—	40	—	40	—	45	—	ns	
$\overline{DT}$ Hold Time from $\overline{RAS}$	t_{RDH}	80	—	90	—	90	—	110	—	ns	
$\overline{DT}$ Hold Time from $\overline{CAS}$	t_{CDH}	20	—	30	—	30	—	45	—	ns	
Last SC to $\overline{DT}$ Delay Time	t_{SDD}	5	—	5	—	5	—	10	—	ns	
First SC to $\overline{DT}$ Hold Time	t_{SDH}	20	—	25	—	25	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Lead Time	t_{DTL}	50	—	50	—	50	—	50	—	ns	

Transfer Cycle (continued)

Parameter	Symbol	HM538122-10		HM538122-11		HM538122-12		HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{DT}$ Hold Time Referenced to $\overline{RAS}$ High	t_{DTHH}	20	—	25	—	25	—	30	—	ns	
$\overline{DT}$ Precharge Time	t_{DTP}	30	—	35	—	35	—	40	—	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	—	60	—	60	—	75	—	ns	
Serial Data Input to $\overline{RAS}$ to Delay Time	t_{SZR}	—	10	—	10	—	10	—	10	ns	
Serial Output Buffer Turn-off Delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	60	10	75	ns	7
$\overline{RAS}$ to S_{out} (Low-Z) Delay Time	t_{RLZ}	5	—	10	—	10	—	10	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Serial Clock Cycle Time	t_{SCC2}	40	—	40	—	40	—	60	—	ns	13
Access Time from SC	t_{SCA}	—	30	—	35	—	40	—	50	ns	4
Serial Data-out Hold Time	t_{SOH}	7	—	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	20	—	25	—	ns	

Serial Read Cycle

Parameter	Symbol	HM538122-10		HM538122-11		HM538122-12		HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Access Time from SC	t_{SCA}	—	30	—	35	—	40	—	50	ns	4
Access Time from $\overline{SE}$	t_{SEA}	—	25	—	30	—	30	—	40	ns	4
Serial Data-out Hold Time	t_{SOH}	7	—	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{SE}$	t_{SEZ}	—	25	—	25	—	25	—	30	ns	7

Serial Write Cycle

Parameter	Symbol	HM538122-10		HM538122-11		HM538122-12		HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	20	—	25	—	ns	
Serial Write Enable Setup Time	t_{SWS}	0	—	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	t_{SWH}	30	—	35	—	35	—	50	—	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	-	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	30	—	35	—	35	—	50	—	ns	

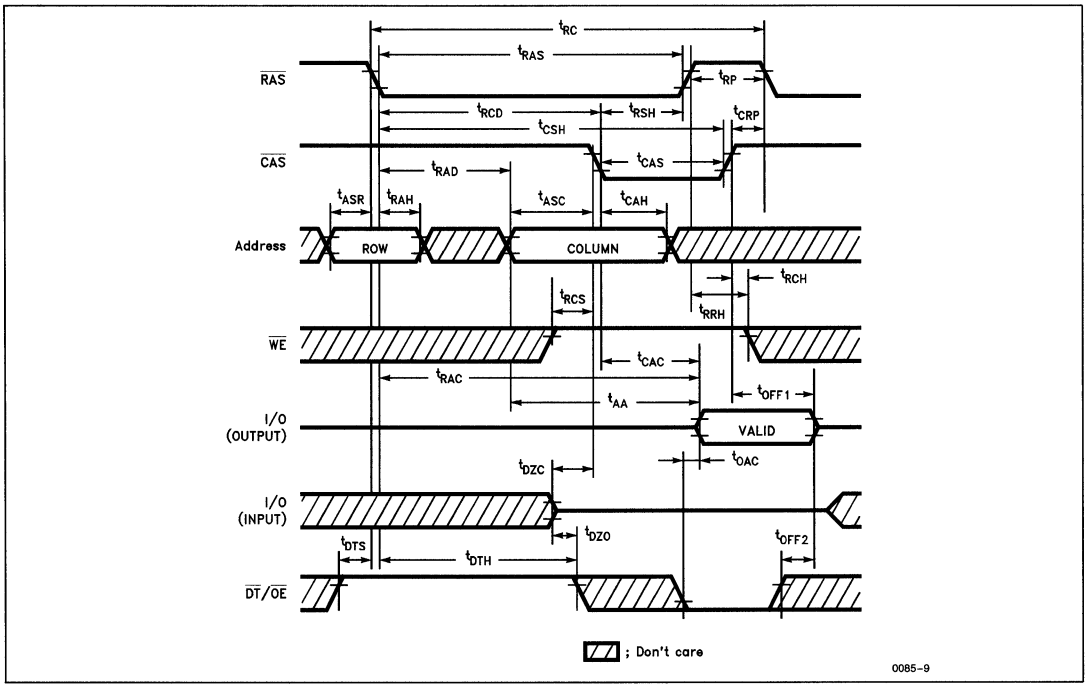
Logic Operation Mode

Parameter	Symbol	HM538122-10		HM538122-11		HM538122-12		HM538122-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Hold Time (Logic Operation Set/Reset Cycle)	t_{FCHR}	90	—	100	—	100	—	120	—	ns	
$\overline{RAS}$ Pulse Width in Write Cycle	t_{RFS}	140	10000	165	10000	165	10000	200	10000	ns	
$\overline{CAS}$ Pulse Width in Write Cycle	t_{CFS}	60	—	70	—	70	—	80	—	ns	
$\overline{CAS}$ Hold Time in Write Cycle	t_{FCSH}	140	—	165	—	165	—	200	—	ns	
$\overline{RAS}$ Hold Time in Write Cycle	t_{FRSH}	60	—	70	—	70	—	80	—	ns	
Write Cycle Time	t_{FRC}	230	—	265	—	265	—	310	—	ns	
Page Mode Cycle Time (Write Cycle)	t_{FPC}	85	—	100	—	100	—	120	—	ns	
Pulse Width in Page Mode	t_{RFSP}	0.14	100	0.14	100	0.165	100	0.2	100	μs	

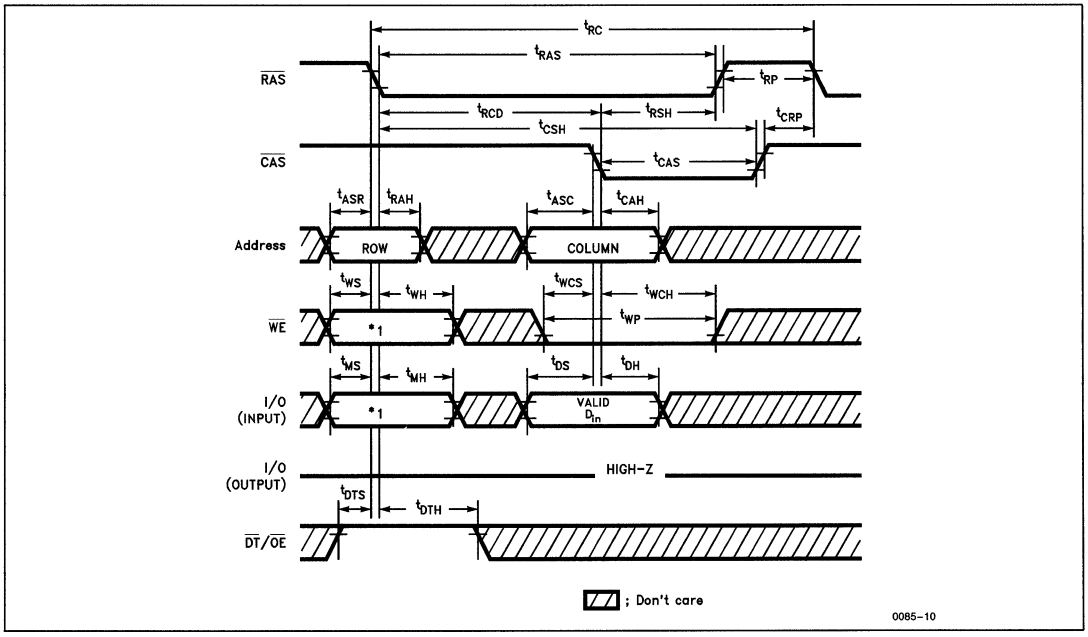
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
5. When $t_{RCD} \geq t_{RCD}$ (max) or $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
6. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
7. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition (V_{OH} − 200 mV, V_{OL} + 200 mV).
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
9. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
   When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-modify-write cycle; the data of the selected address is read out from a data output pin and input data is written into the selected address. In this case, impedance on I/O pins is controlled by $\overline{OE}$.
10. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles or to $\overline{WE}$ falling edge in delayed write or read-modify-write cycles.
11. After power-up, pause for 100 μs or more and execute at least 8 initialization cycles (normal memory cycles or refresh cycles), then start operation.
12. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.
13. t_{SCC2} is defined as the last SAM cycle time before read transfer in read transfer cycle (1).
14. When I/O or SI/O is in the output state, data input signals must not be applied to I/O or SI/O.
15. When $\overline{SE}$ is low after power on, SI/O is in the output state. Data input signals must not be applied to SI/O in this time.
16. When $\overline{CAS}$ and $\overline{DT}/\overline{OE}$ are both low after power on, it is possible that I/O is in the output state. Data input signals must not be applied to I/O in this time.

■ TIMING WAVEFORMS

• Read Cycle

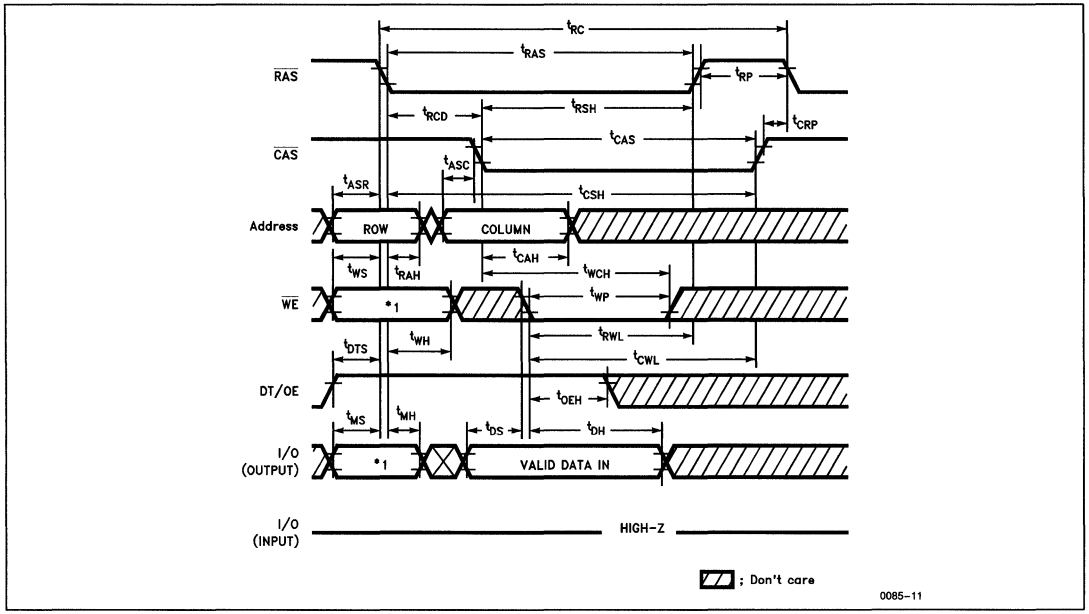


• Early Write Cycle



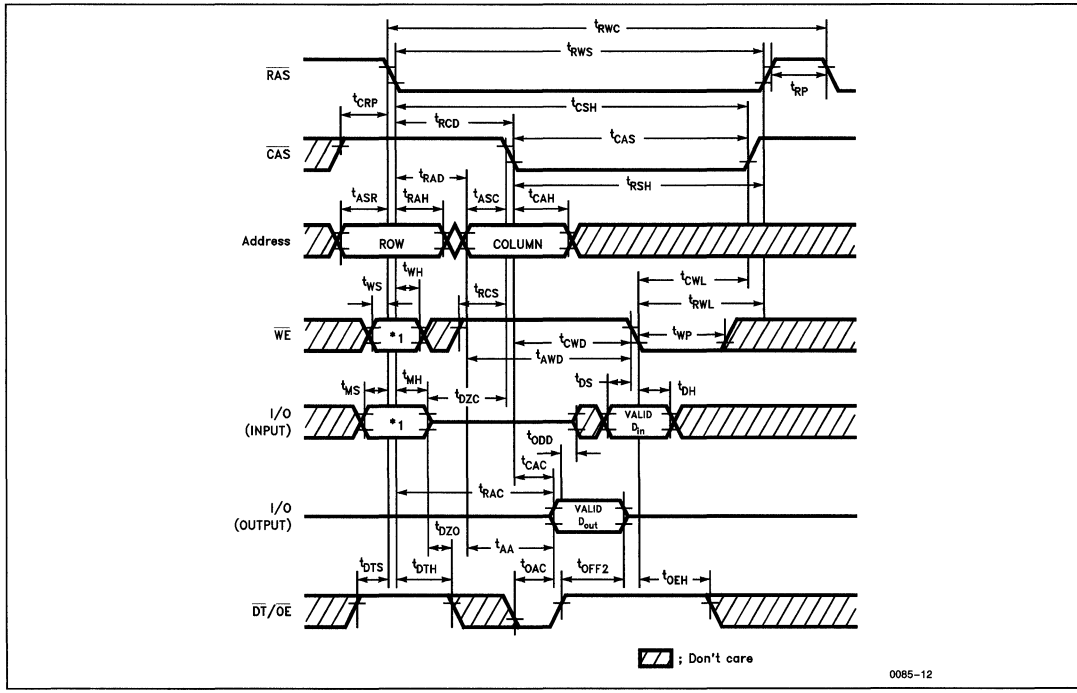
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case the I/O is high at the falling edge of $\overline{RAS}$.

• Delayed Write Cycle



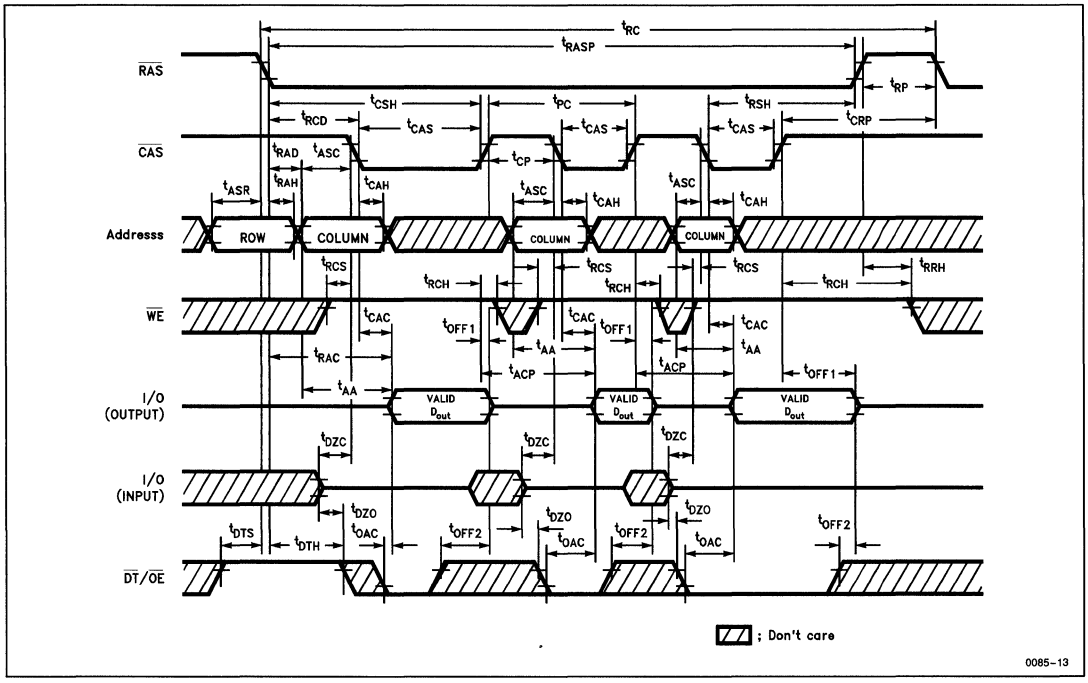
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• Read-Modify-Write Cycle

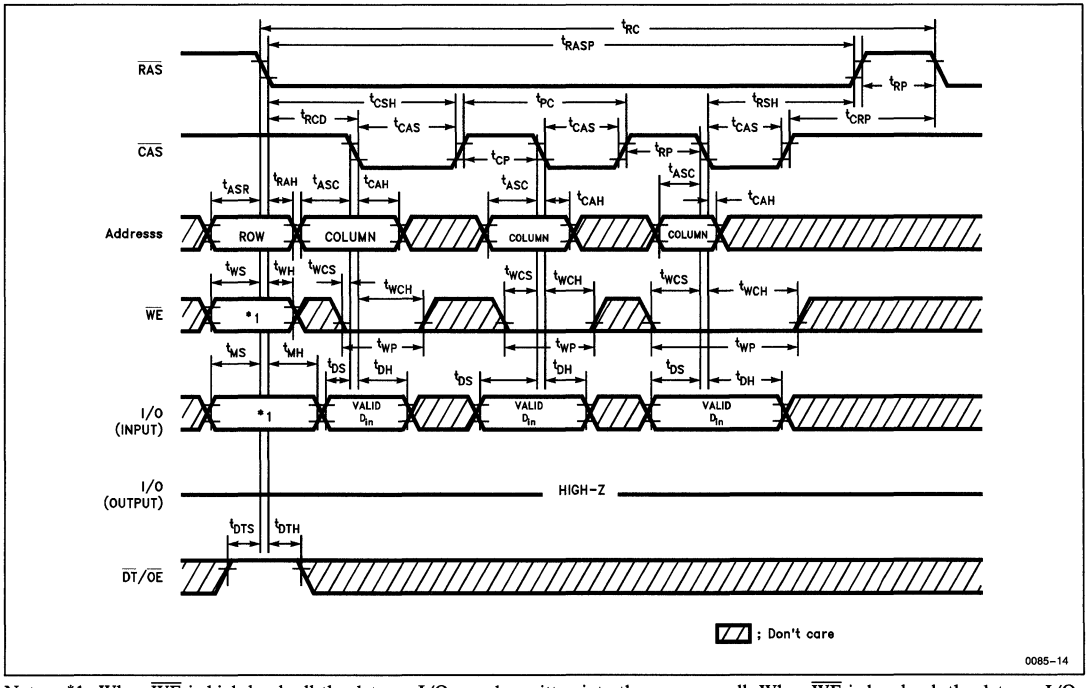


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Read Cycle

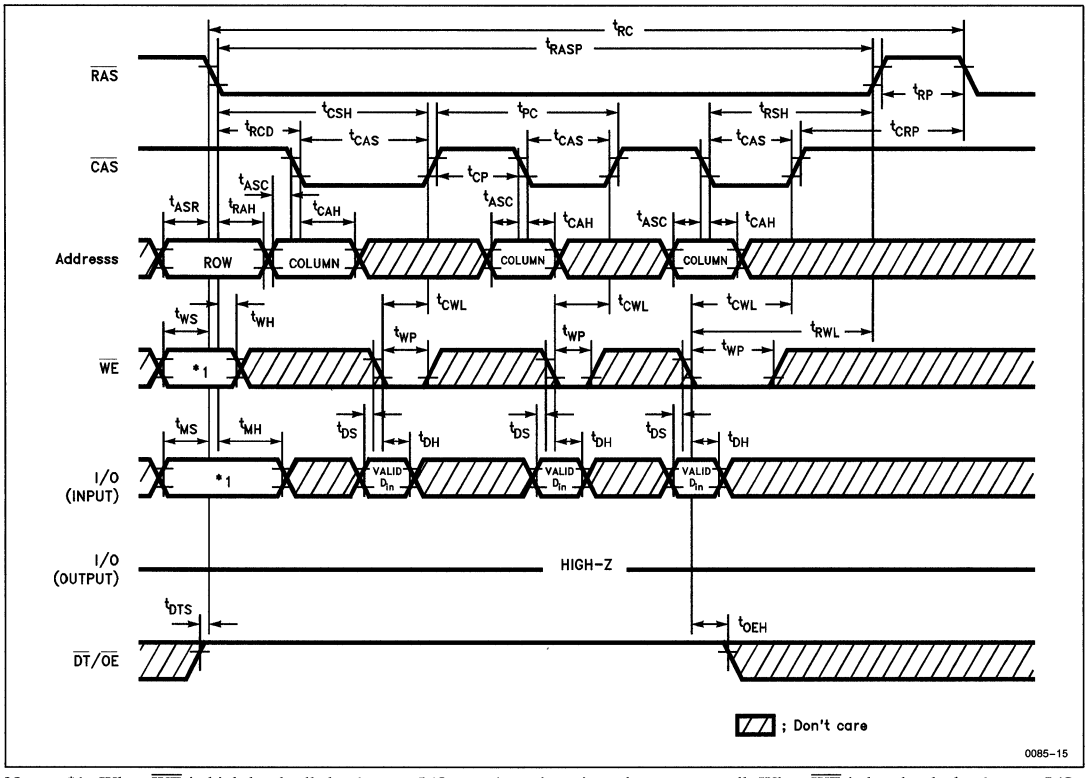


Page Mode Write Cycle (Early Write)



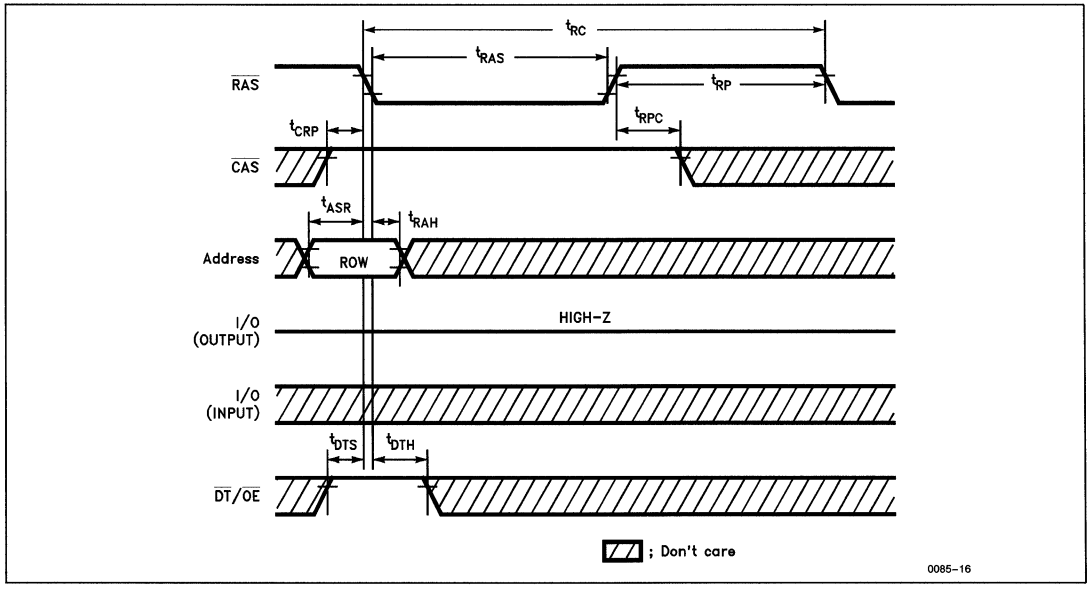
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Delayed Write)

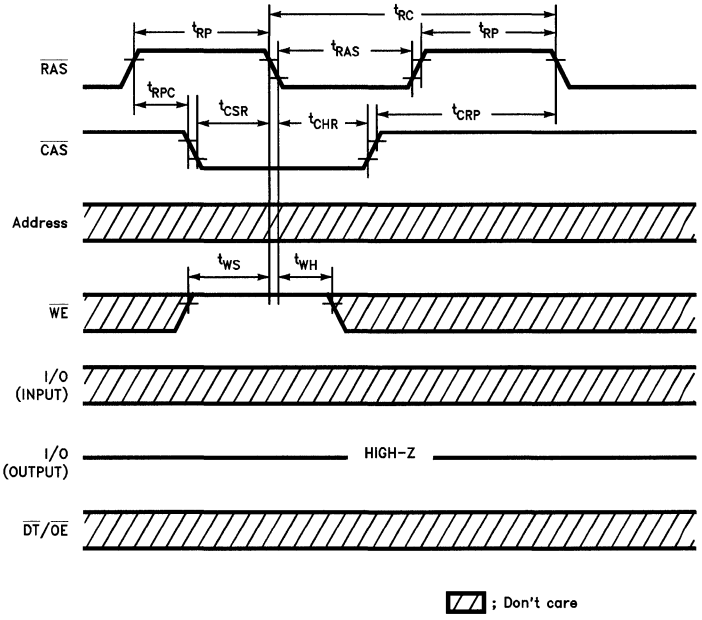


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

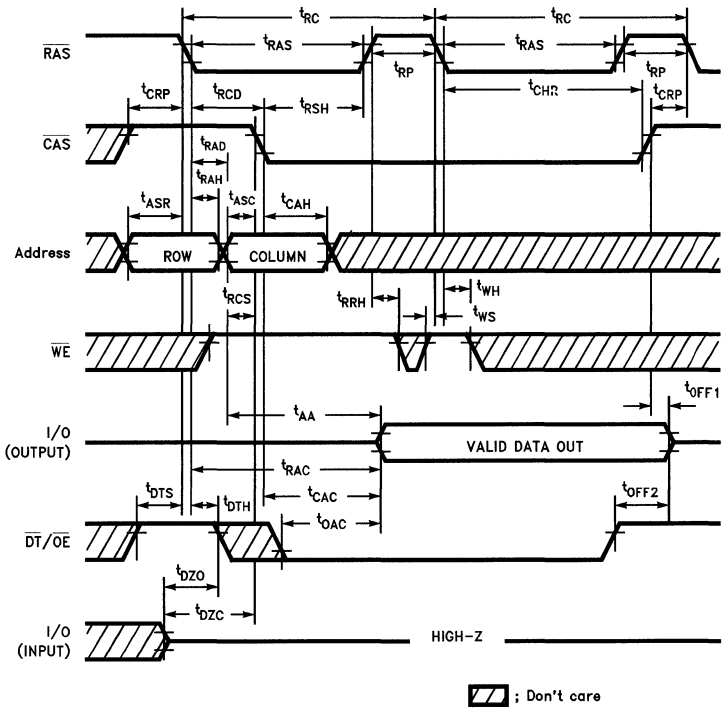
• $\overline{RAS}$ Only Refresh Cycle



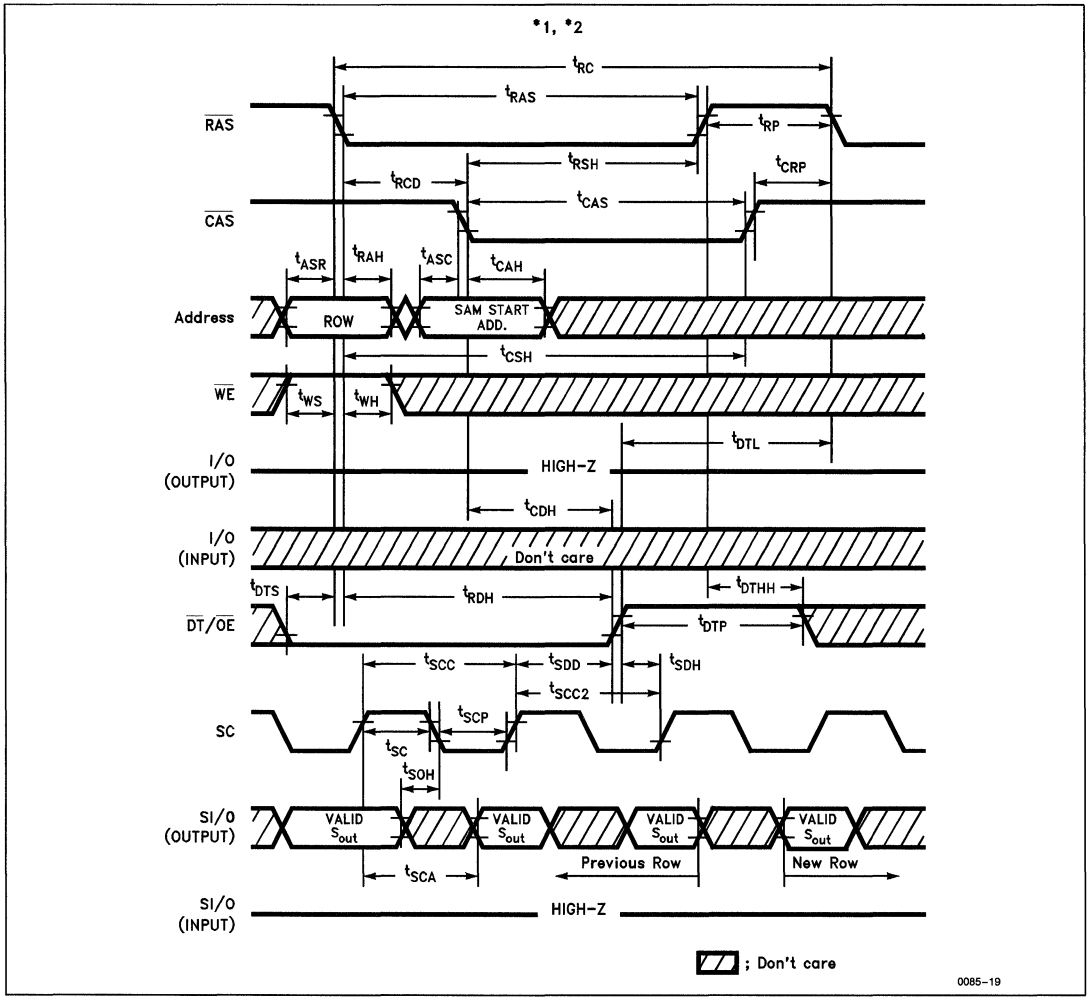
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• Hidden Refresh Cycle

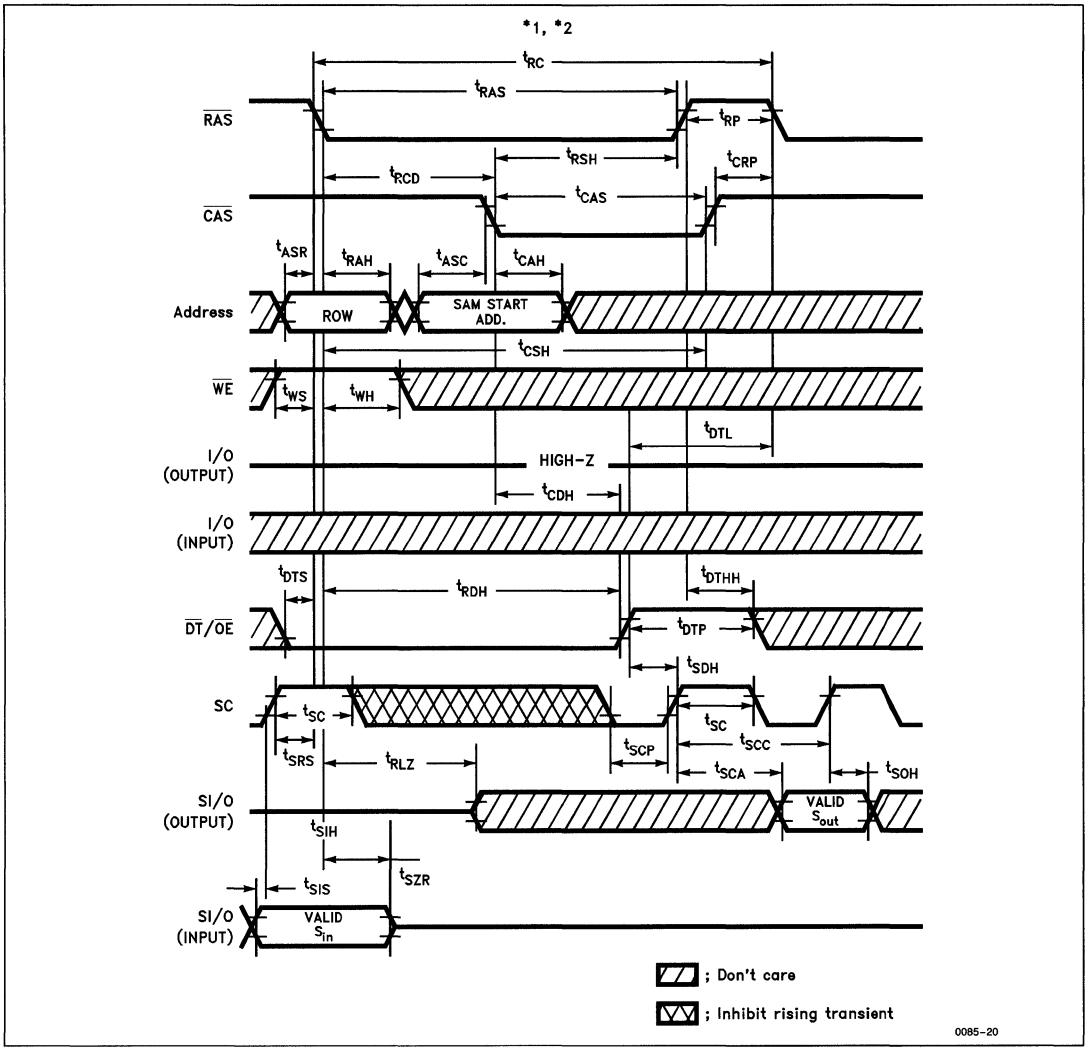


• Read Transfer Cycle (1)



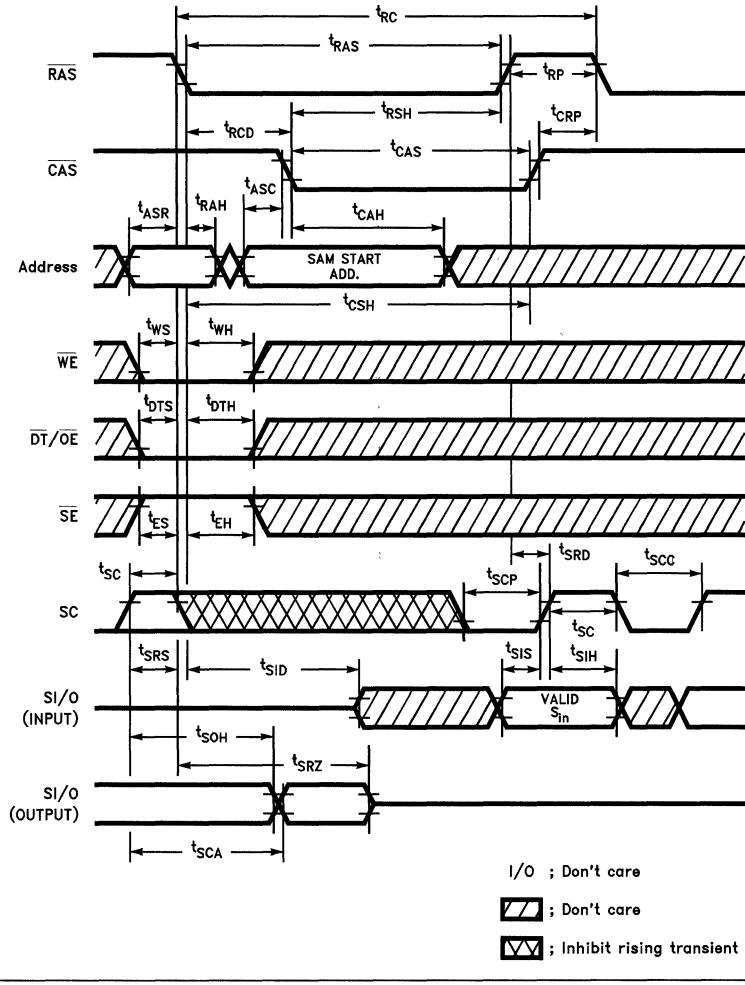
Notes: *1. When the previous data transfer cycle is a read transfer cycle, it is defined as read transfer cycle (1).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)

• **Read Transfer Cycle (2)**

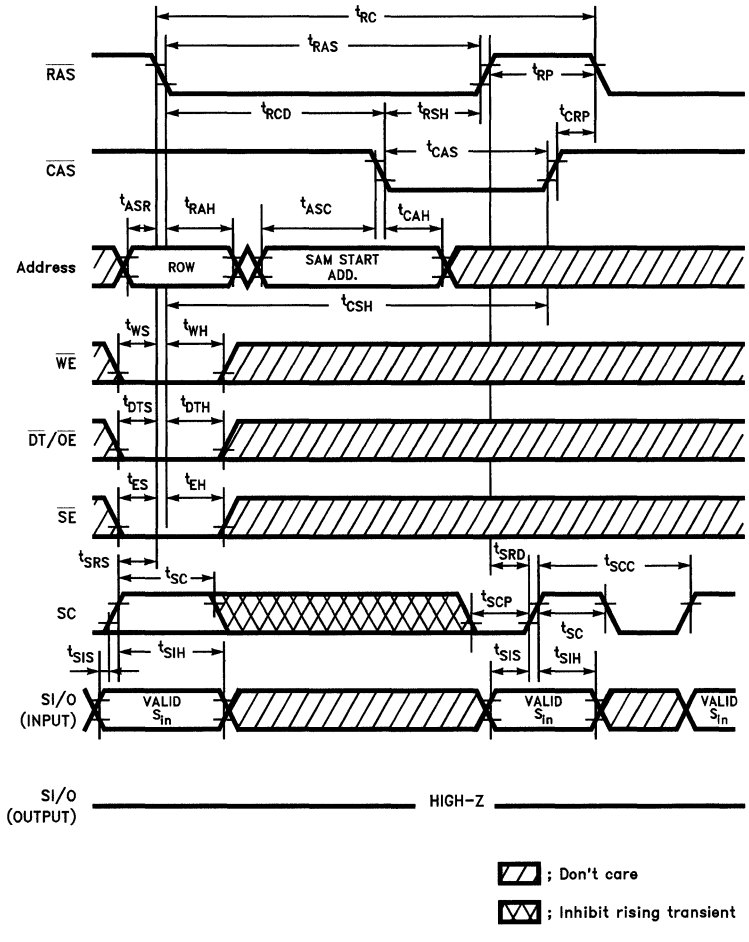


Notes: *1. When the previous data transfer cycle is a write or pseudo transfer cycle, it is defined as read transfer cycle (2).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)

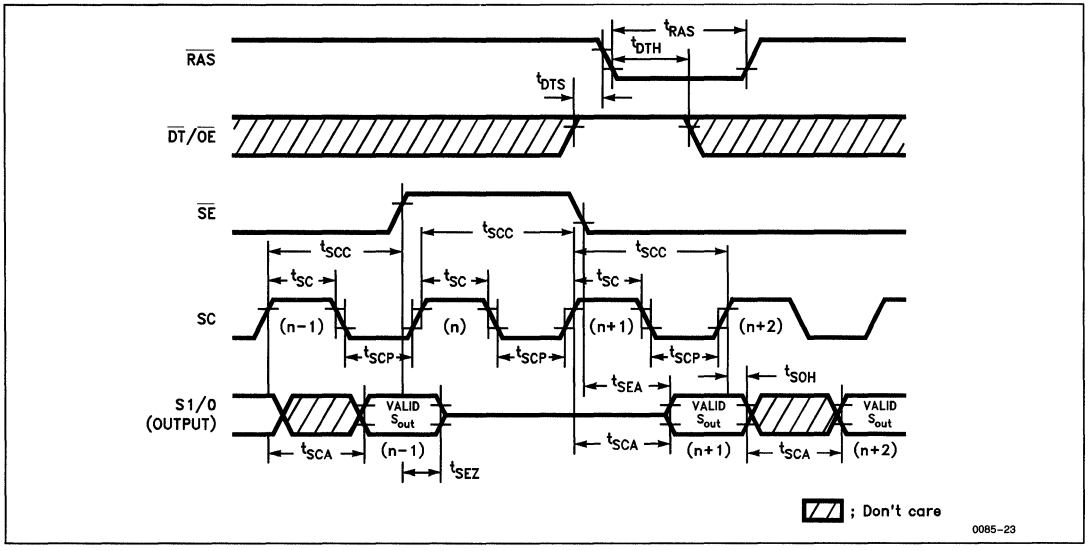
• **Pseudo Transfer Cycle**



• **Write Transfer Cycle**

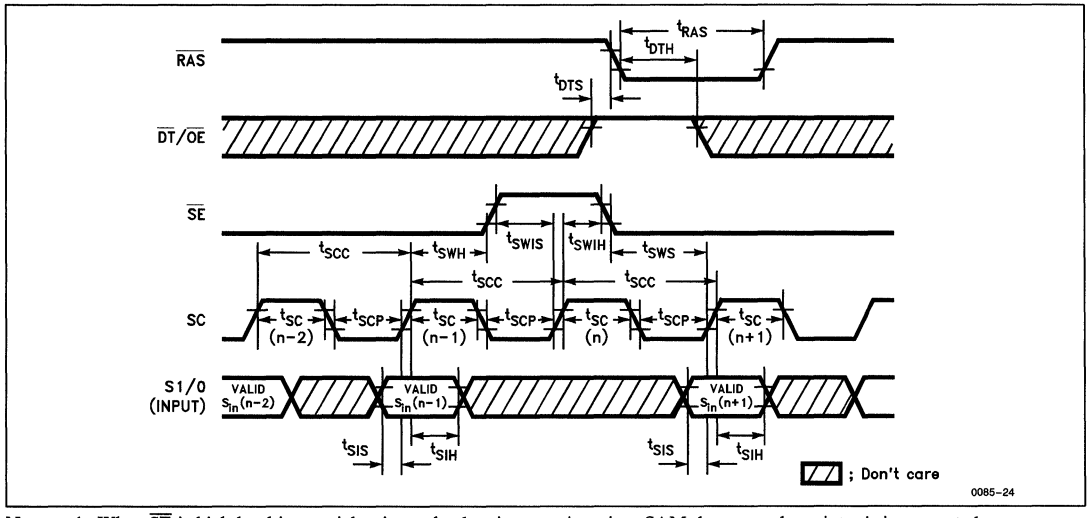


• **Serial Read Cycle**



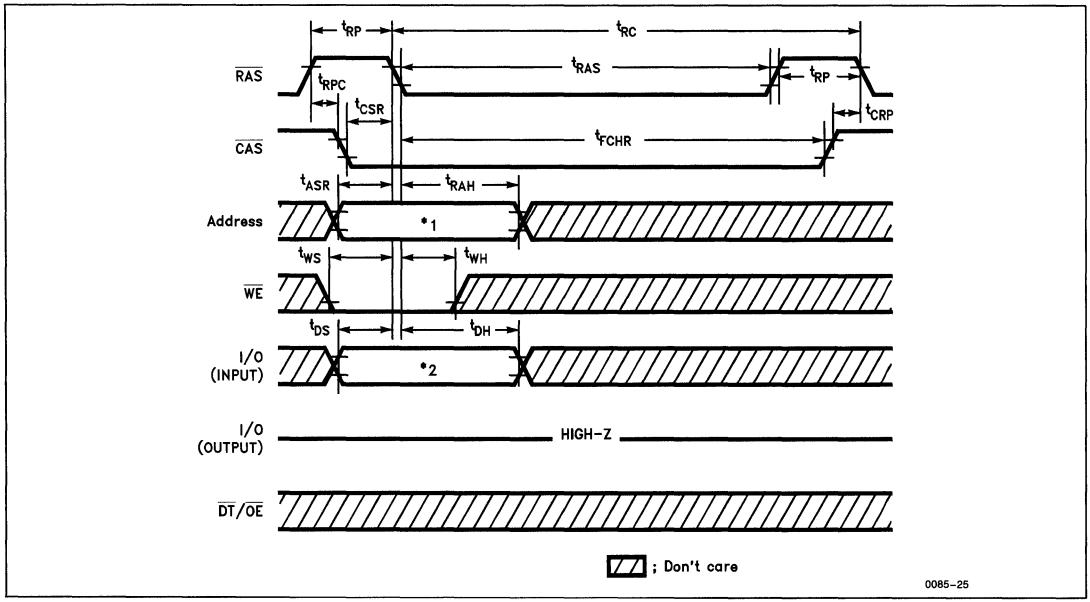
Note: 1. Address 0 is accessed next to address 255.

• **Serial Write Cycle**



Notes: 1. When $\overline{SE}$ is high level in a serial write cycle, data is not written into SAM, however, the pointer is incremented.
2. Address 0 is accessed next to address 255.

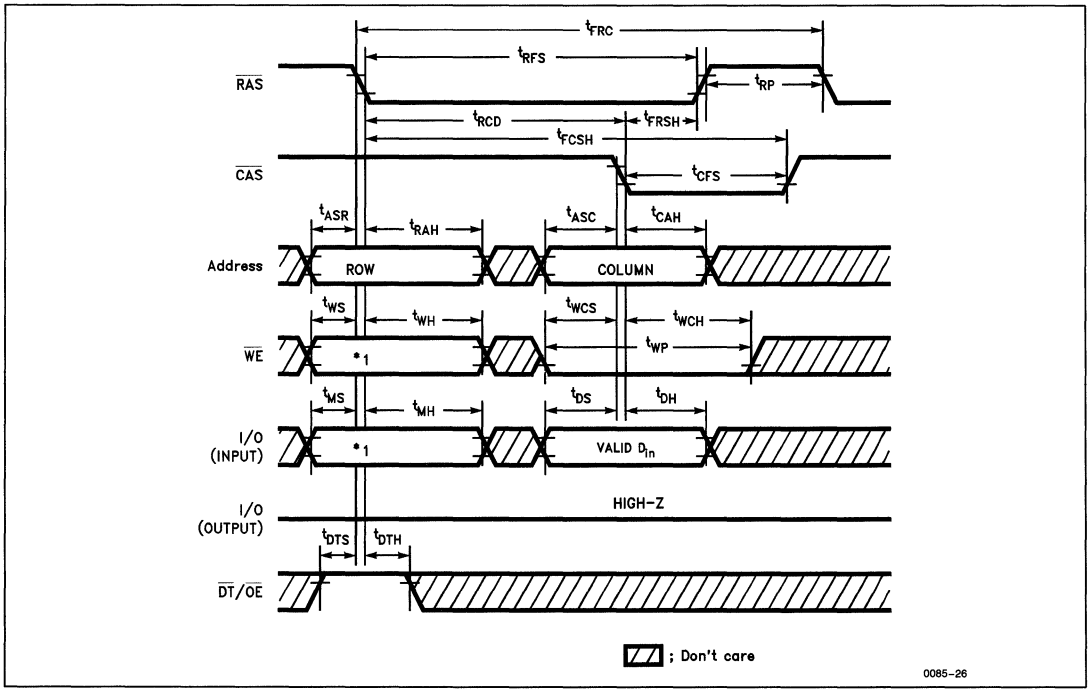
• Logic Operation Set/Reset Cycle



Notes: *1. Logic code A_0–A_3.
*2. Write mask data.

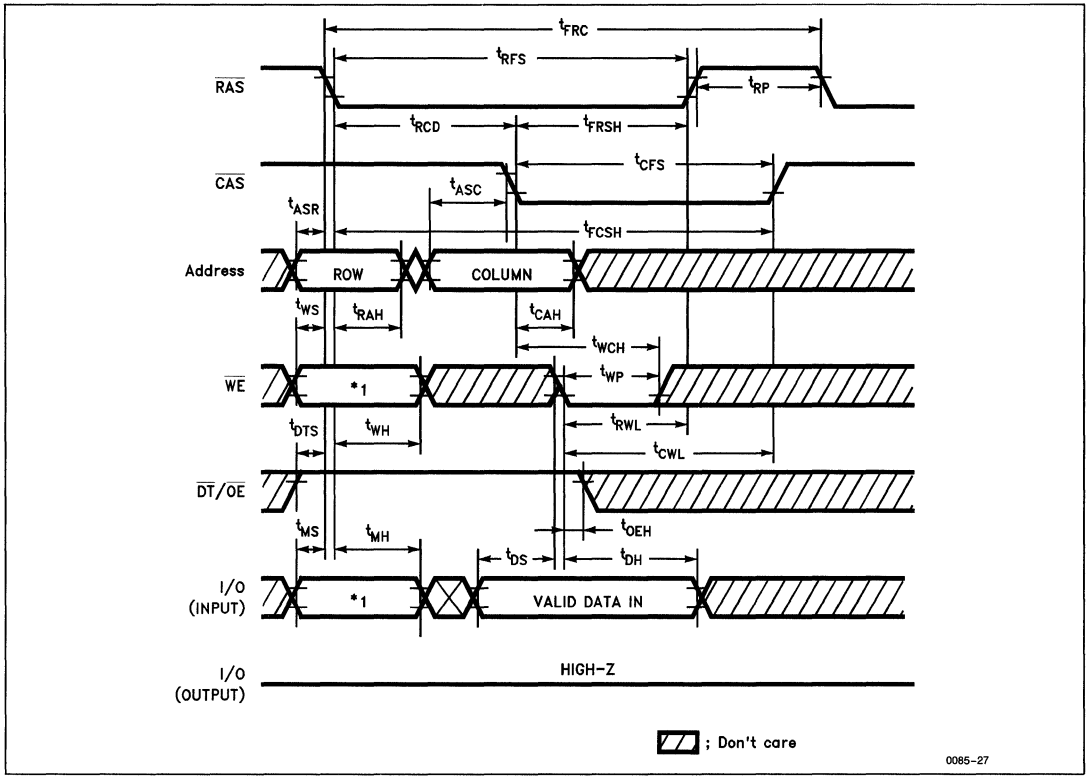
• Logic Operation Mode Timing Waveforms

Early Write Cycle



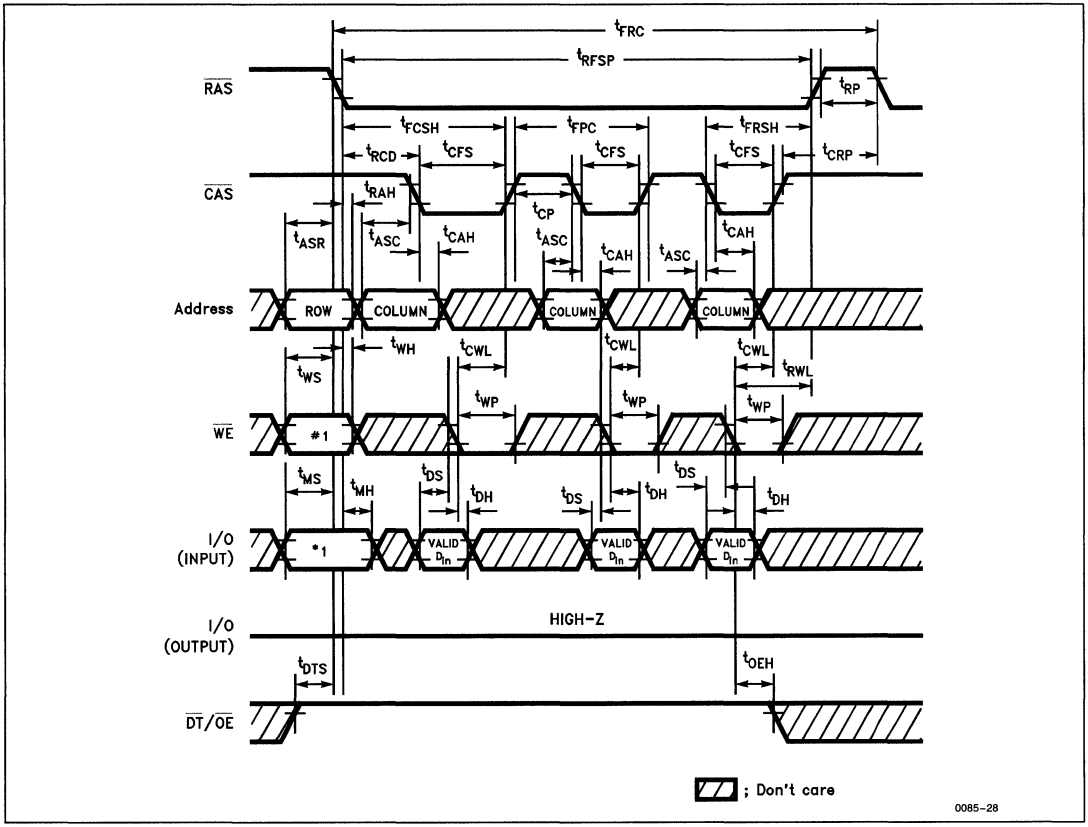
Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Delay Write Cycle



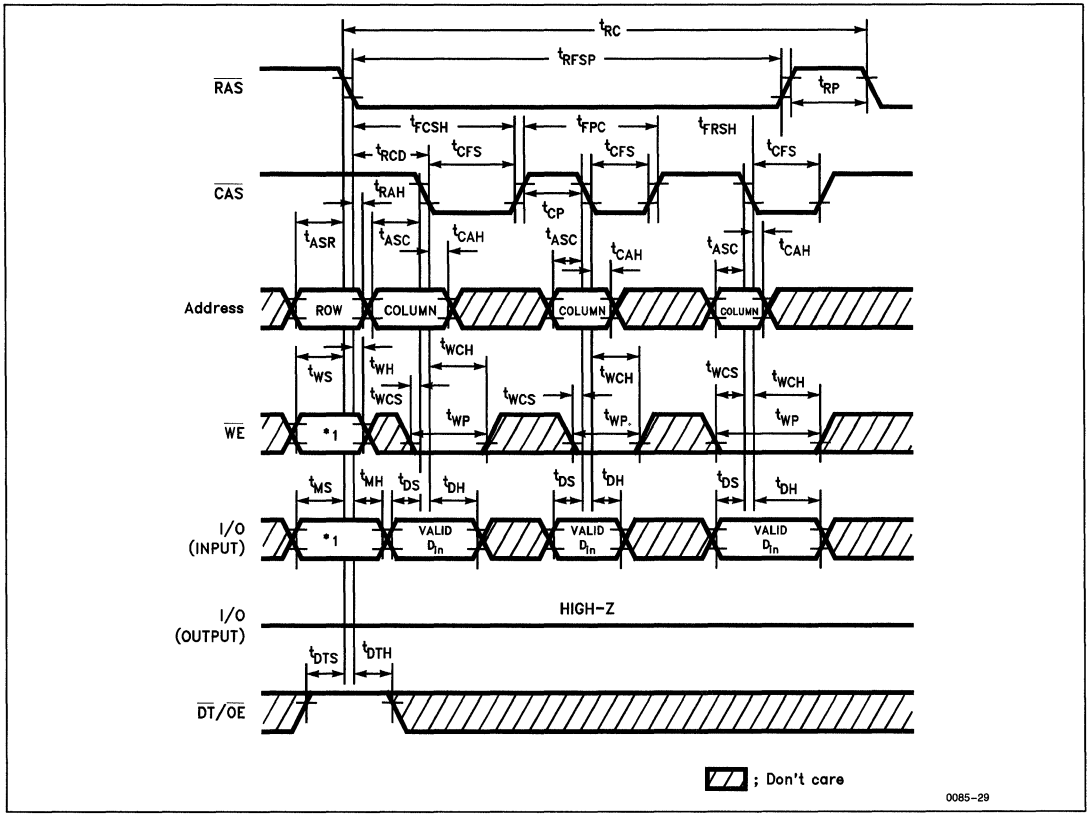
Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Delayed Write)



Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Early Write)



Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

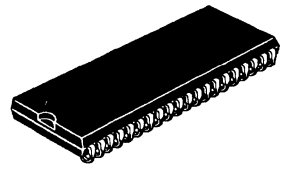
HM538123 Series

131,072-Word x 8-Bit Multiport CMOS Video RAM

■ DESCRIPTION

The HM538123 is a 1-Mbit multiport video RAM equipped with a 128k-word x 8-bit dynamic RAM and a 256-word x 8-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has a write mask function. In addition, it has two new functions. Flash write clears the data of one row in one cycle in RAM. Special read transfer internally detects that the last address in SAM is read and transfers the next data of one row automatically from RAM if a transfer cycle has previously been executed. These functions make it easier to use the HM538123.

HM538123 Series



3DCP40D

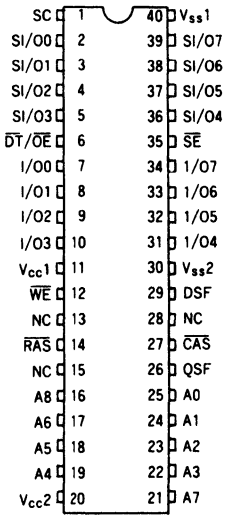
(CP-40D)

■ FEATURES

- Multiport Organization
  - Asynchronous and Simultaneous Operation of RAM and SAM Capability
  - RAM ..... 128k-word x 8-bit
  - SAM ..... 256-word x 8-bit
- Access Time
  - RAM ..... 100 ns/120 ns/150 ns (max)
  - SAM ..... 30 ns/40 ns/50 ns (max)
- Cycle Time
  - RAM ..... 190 ns/220 ns/260 ns (min)
  - SAM ..... 30 ns/40 ns/60 ns (min)
- Low Power
  - Active
    - RAM ..... 385 mW (max)
    - SAM ..... 275 mW (max)
  - Standby ..... 40 mW (max)
- High-Speed Page Mode Capability
- Mask Write Mode Capability
- Bidirectional Data Transfer Cycle between RAM and SAM Capability
- Special Read Transfer Cycle Capability
- Flash Write Cycle Capability
- 3 Variations of Refresh (8 ms/512 Cycles)
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- TTL Compatible

■ PIN OUT

HM538123JP Series



0111-1

(Top View)

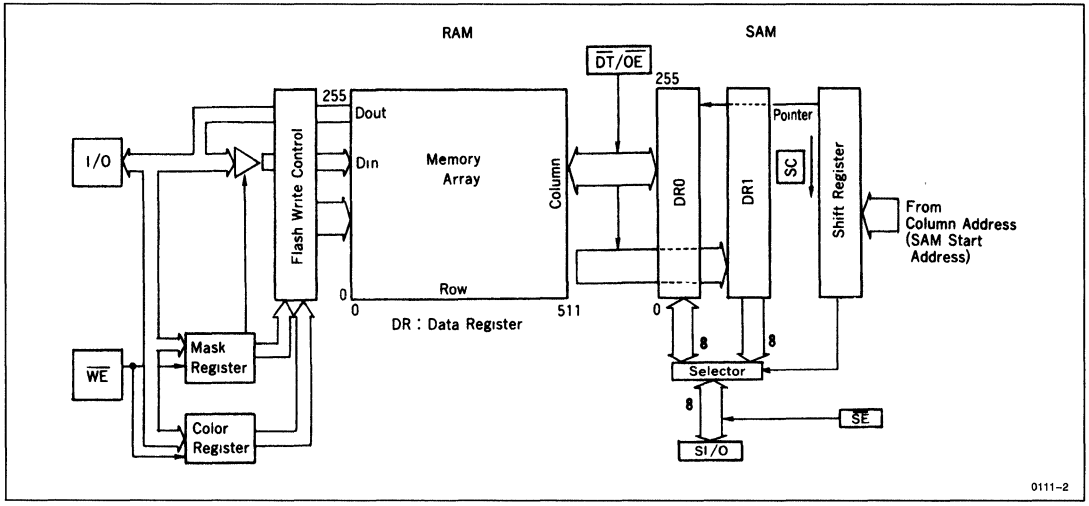
■ ORDERING INFORMATION

Part No.	Access Time	Package
HM538123JP-10	100 ns	400 mil
HM538123JP-12	120 ns	40-pin
HM538123JP-15	150 ns	Plastic SOJ (CP-40D)

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Inputs
I/O_0–I/O_7	RAM Port Data Inputs/Outputs
SI/O_0–SI/O_7	SAM Port Data Inputs/Outputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{DT/OE}$	Data Transfer Output Enable
SC	Serial Clock
$\overline{SE}$	SAM Port Enable
DSF	Special Function Input Flag
QSF	Data Register Empty Flag
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



■ PIN FUNCTION

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in Table 1 are input at the falling edge of $\overline{RAS}$. The input level of those signals determine the operation cycle of the HM538123.

• Table 1. Operation Cycles of the HM538123

Input Level at the Falling Edge of $\overline{RAS}$					Operation Cycle
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SE}$	DSF	
H	H	H	X	L	RAM Read/Write
H	H	H	X	H	Color Register Set
H	H	L	X	L	Mask Write
H	H	L	X	H	Flash Write
H	L	H	X	L	Special Read Initialization
H	L	H	X	H	Special Read Transfer
H	L	L	H	X	Pseudo Transfer
H	L	L	L	X	Write Transfer
L	X	X	X	X	CBR Refresh

Note: X; Don't care.

$\overline{CAS}$ (input pin): Column address is put into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A_0–A_8 (input pins): Row address is determined by A_0–A_8 level at the falling edge of $\overline{RAS}$. Column address is determined by A_0–A_7 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538123 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O_0–I/O_7 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write and flash write mode). Data is written only on high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data is output from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is put into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not put into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O_0–SI/O_7 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a special read transfer cycle or special read initialization cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

DSF (input pin): DSF is a special data input flag pin. It is set to high when new functions such as color register set, special read transfer, and flash write, are used.

QSF (output pin): The HM538123 has a double buffer organization which includes two SAM data registers to relax the restriction on timings of $\overline{DT}/\overline{OE}$ and SC in real time transfer cycle. QSF flag turns high when output from one of SAM data registers finished (data register empty flag). If the condition is detected and special read transfer cycle is executed, data is transferred to the empty register. SC (serial clock) and data transfer cycle can be set asynchronously because detection of the last address in SAM and change of data register are executed automatically in the chip. It makes the system design flexible.

■ OPERATION OF HM538123

• Operation of RAM Port

RAM Read Cycle ($\overline{DT}/\overline{OE}$ High, $\overline{CAS}$ High, DSF Low at the Falling Edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data is output through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle

(Early Write, Delayed Write, Read Modify Write) ($\overline{DT}/\overline{OE}$ High, $\overline{CAS}$ High, DSF Low at the Falling Edge of $\overline{RAS}$)

- Normal Mode Write Cycle

($\overline{WE}$ High at the Falling Edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after driving $\overline{RAS}$ low, a write cycle is executed and I/O data is written in the selected addresses. When all 8 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes in high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read modify write cycle and enables read/write to execute in the same address cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

- Mask Write Mode

($\overline{WE}$ Low at the Falling Edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is preserved. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is preserved during the page access.

High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ High, $\overline{CAS}$ High, DSF Low at the Falling Edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle and is higher than the standard page mode cycle by 70–80%. This product is based on static column mode, therefore, address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 256-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RAS} max (10 μs).

Flash Write Function (See Figure 1)

- Color Register Set Cycle ($\overline{CAS}$-$\overline{DT}/\overline{OE}$-$\overline{WE}$ High, DSF High at the Falling Edge of $\overline{RAS}$)

In color register set cycle, color data is set to the internal color register used in flash write cycle. 8 bits of internal color register are provided at each I/O. This register is composed of static circuits, so once it is set, it preserves the data until reset. The data set is just as same as in the usual write cycle except that DSF is set high at the falling edge of $\overline{RAS}$, and early write and delayed write cycle can be executed. In this cycle, memory array access is not executed, so it is unnecessary to give row and column addresses.

- Flash Write Cycle ($\overline{CAS}$-$\overline{DT}/\overline{OE}$ High, $\overline{WE}$ Low, DSF High at the Falling Edge of $\overline{RAS}$)

In a flash write cycle, a row of data (256 x 8 bit) is cleared to 0 or 1 at each I/O according to the data of color register mentioned before. It is also possible to mask I/O in this cycle. When $\overline{CAS}$-$\overline{DT}/\overline{OE}$ is set high, $\overline{WE}$ is low, and DSF is high at the falling edge of $\overline{RAS}$, this cycle starts. Then, the row address to clear is given to row address and mask data is to I/O. Mask data is as same as that of a RAM write cycle. High I/O is cleared, low I/O is not cleared and the internal data is preserved. Cycle time is the same as those of RAM read/write cycles, so all bits can be cleared in 1/512 of the usual cycle time.

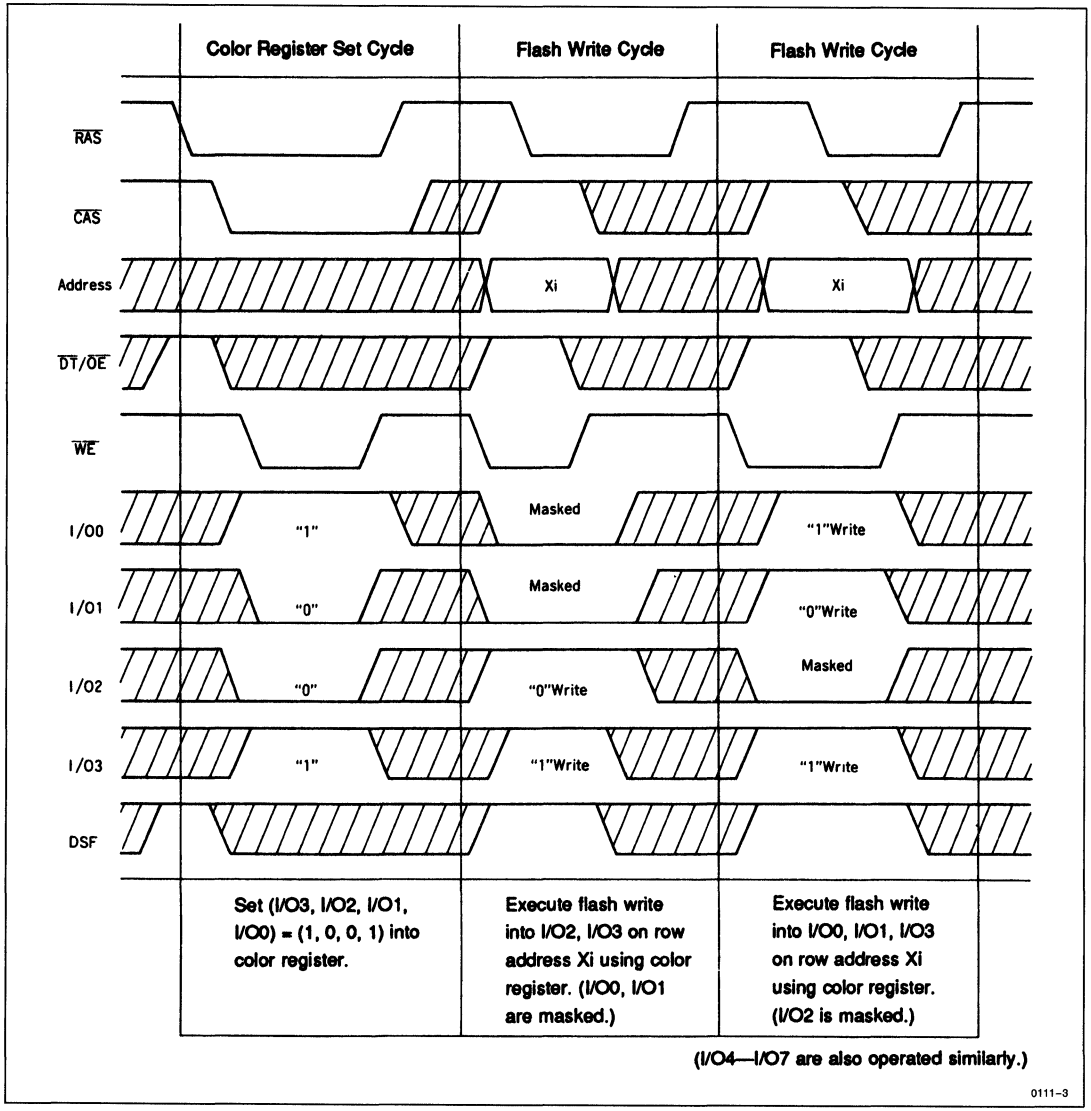


Figure 1. Use of Flash Write

• Transfer Operation

The HM538123 provides the special read initialization cycle, special read transfer cycle, pseudo transfer cycle, and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)

(2) Determine direction of data transfer

(a) Special read initialization cycle, Special read transfer cycle: RAM → SAM
(b) write transfer cycle: RAM ← SAM

(3) Determine input or output of SAM I/O pin (SI/O)
Special read initialization cycle: SI/O output
Pseudo transfer cycle, write transfer cycle: SI/O Input

(4) Determine first SAM address to access (SAM start address) after transferring at column address. When SAM start address is not changed, neither $\overline{CAS}$ nor address need to be set because SAM start address can be latched internally.

Special Read Initialization Cycle ($\overline{CAS}$ High, $\overline{DT}/\overline{OE}$ Low, $\overline{WE}$ High, DSF Low at the Falling Edge of $\overline{RAS}$)

If $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ is low, $\overline{WE}$ high, and DSF low at the falling edge of $\overline{RAS}$, this cycle becomes a special read initialization cycle. Special read initialization is used (1) to start special read transfer operation and (2) to switch SAM input/output pin (SI/O) set in input state by pseudo transfer cycle or write transfer cycle, to output state.

If the clock is set as mentioned before, address of SAM transfer word line is set to row address and first SAM address to access (SAM start address) to column address, it becomes possible to execute SAM read after t_{SRD} (min) after $\overline{RAS}$ is high. In this cycle, SI/O outputs uncertain data after the $\overline{RAS}$ falling edge. So when SAM is in input state before executing this cycle, it is necessary to stop input before the $\overline{RAS}$ falling edge.

SAM access is inhibited while $\overline{RAS}$ is low in this cycle. SC should not be raised during $\overline{RAS}$ low.

Special Read Transfer Cycle ($\overline{CAS}$ High, $\overline{DT}/\overline{OE}$ Low, $\overline{WE}$ High, DSF High at the Falling Edge of $\overline{RAS}$)

Ordinary multiport video RAM has some problems; (1) severe limitation on timings between processor clock $\overline{DT}/\overline{OE}$ and CRT clock SC, (2) complicated external control circuit to detect SAM last address externally and to insert transfer cycle synchronously. Special read transfer cycle makes it possible to relax the timing limitations and to set serial clock (SC) and transfer cycle perfectly synchronously.

Figure 2 shows the block diagram for a special read transfer. SAM double buffers are composed of two data registers (DR). When data is read out from DR0 serially, special read transfer cycle transfers a row of RAM data, which will be read from SAM next, to DR1.

The end of data read from DR0 is detected internally and data register switching circuit automatically switches to DR1 output. So data can be output continuously.

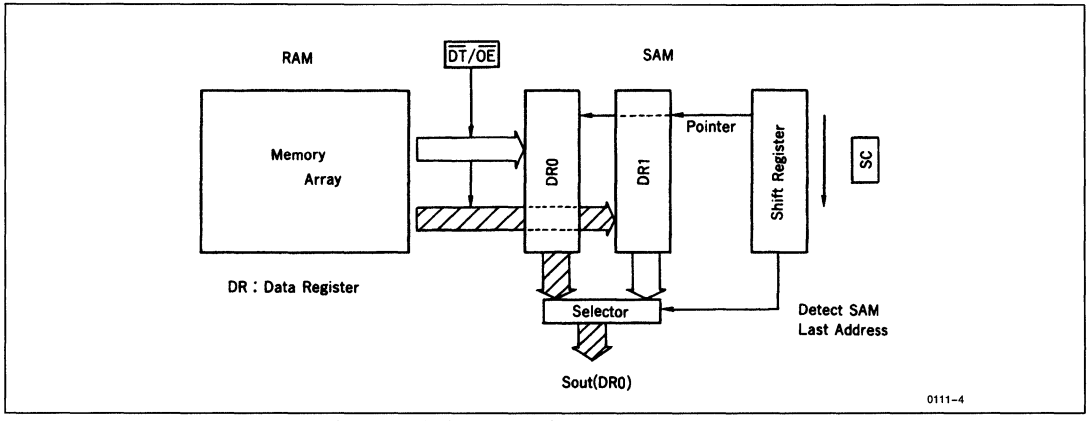


Figure 2. Block Diagram for Special Read Transfer

Figure 3 shows special read transfer operation sequence. QSF flag indicates that reading out from data register has finished (data register empty flag), and special read transfer can be executed while QSF is high. At first, special read operation starts by executing a special read initialization cycle. So QSF becomes high, the processor gives row address and SAM start address, which is needed next, to the memory, and inserts a special read transfer cycle. Data register becomes full after a special read transfer cycle, so QSF becomes low during the cycle. When the last SAM address is accessed, QSF becomes high and the data register, which outputs from the next SAM address, changes, and serial access can be executed.

By executing these handshakes, serial clock and transfer cycle can be executed perfectly asynchronously, and flexibility of the system design is improved.

Special read transfer cycle is set by making $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high, and DSF high at the falling edge of RAS (same as for special read initialization cycle except DSF). Like in other transfer cycles, the address of the word line to transfer into data register is specified by row address and SAM start is specified by column address. When the last SAM address data is output, the next data is output from the SAM start address specified by this RAS cycle. This transfer cycle can be executed asynchronously with SAM cycle. However, it is necessary to execute SAM access after $\overline{RAS}$ becomes high after SAM start address is specified by $\overline{RAS}$ cycle. (See Figure 4).

QSF should be high at the falling edge of $\overline{RAS}$ to execute a special read transfer cycle. A cycle whose QSF is low is neglected (refresh is executed). When the previous transfer cycle is a pseudo transfer or write transfer cycle and SI/O is in input state, special read transfer cycle cannot be used (neglected). Special read initialization cycle is required to switch SI/O to output state.

Pseudo Transfer Cycle ($\overline{CAS}$ High, $\overline{DT}/\overline{OE}$ Low, $\overline{WE}$ Low, and $\overline{SE}$ High at the Falling Edge of $\overline{RAS}$)

Pseudo transfer cycle is available for switching SI/O from output state to input state because data in RAM isn't rewritten. This cycle starts when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high, at the falling edge of $\overline{RAS}$. The output buffer in SI/O becomes high impedance within t_{SRZ} (max) from the $\overline{RAS}$ falling edge. Data should be input to SI/O later than t_{SID} (min) to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high, like in the special read initialization cycle. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC should not be raised.

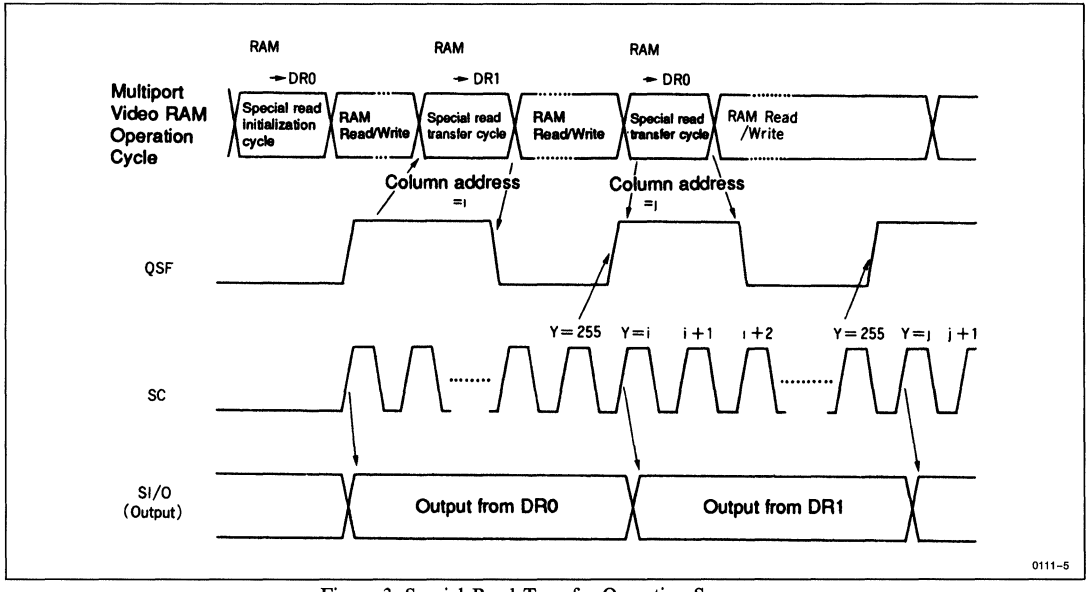


Figure 3. Special Read Transfer Operation Sequence

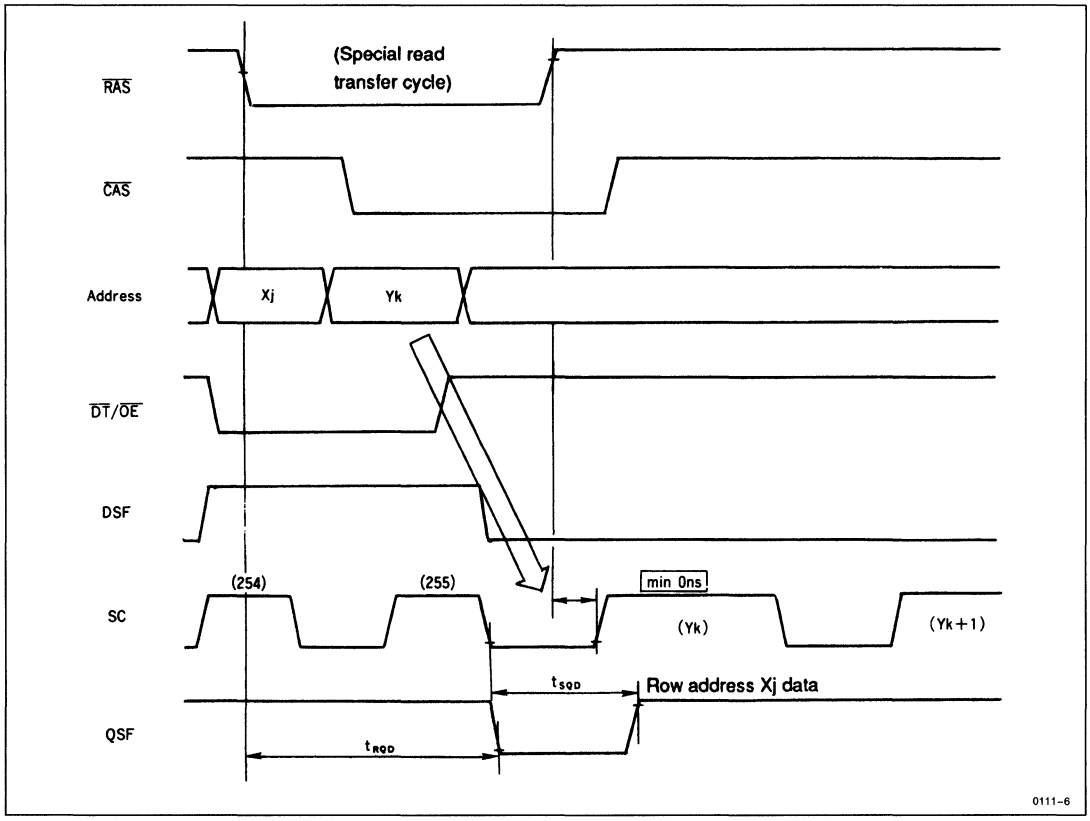


Figure 4. The Restriction of Special Read Transfer

Write Transfer Cycle ($\overline{CAS}$ High, $\overline{DT}/\overline{OE}$ Low, $\overline{WE}$ Low, and $\overline{SE}$ Low at the Falling Edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address to serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC should not be raised.

• SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is special read initialization cycle or special read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When the last address is accessed at the state of QSF low (data register is full), it is signaled to external circuits that special read transfer is enabled by making QSF high. Next, after SAM access, output data register is switched, then the row address data given by previous special read transfer cycle is output from the SAM start address. If special read transfer isn't performed (QSF high), the column address 0 of the same row address is accessed after the last address is accessed.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is programmed into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't input into data register. Internal pointer is incremented according to the SC rising edge, so SE high can be used to mask data for SAM.

• Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is performed by accessing all 512 row addresses every 8 ms. There are three refresh cycles: (1) $\overline{RAS}$ only refresh cycle, (2) $\overline{CAS}$ before $\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required for accessing all row addresses every 8 ms.

$\overline{RAS}$ Only Refresh Cycle: $\overline{RAS}$ only refresh cycle is performed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high by inputting the row address (= refresh address) from external circuits. In this cycle, output is high-impedance and pow-

er dissipation is less than that of normal read/write cycles because $\overline{CAS}$ internal circuits don't operate. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ should be high at the falling edge of $\overline{RAS}$.

CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered like in $\overline{RAS}$ only refresh cycles because $\overline{CAS}$ circuits don't operate.

Hidden Refresh Cycle: Hidden refresh cycle performs refresh by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register, selector), organized as fully static circuitry, don't require refresh.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Terminal Voltage	V_T	−1.0 to +7.0	V	1
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V	1
Power Dissipation	P_T	1.0	W	
Operating Temperature	T_{opr}	0 to +70	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

Note: 1. Relative to V_{SS}.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−0.5	—	0.8	V	1, 2

Notes: 1. All voltages referenced to V_{SS}.
2. −3.0V for pulse width ≤ 10 ns.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Test Conditions		Note
		Min	Max	Min	Max	Min	Max		RAM Port	SAM Port	
Operating Current	I_{CC1}	—	70	—	60	—	50	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC7}	—	120	—	100	—	80	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Standby Current	I_{CC2}	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC8}	—	50	—	40	—	30	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	60	—	50	—	40	mA	$\overline{RAS}$ Cycling $\overline{CAS}$ = V_{IH} t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC9}	—	110	—	90	—	70	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Page Mode	I_{CC4}	—	65	—	55	—	45	mA	$\overline{CAS}$ Cycling $\overline{RAS}$ = V_{IL} t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC10}	—	115	—	95	—	75	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC5}	—	60	—	50	—	40	mA	$\overline{RAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC11}	—	110	—	90	—	70	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Data Transfer Current	I_{CC6}	—	90	—	90	—	90	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC12}	—	125	—	125	—	125	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	µA		
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	µA		
Output High Voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = −2 mA	
Output Low Voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA	

• Capacitance (T_A = 25°C, V_{CC} = 5V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, Address = V_{SS})

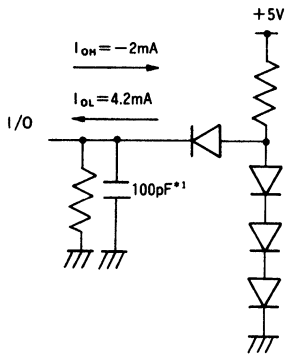
Item	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

• AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 11]

Test Conditions

Input Rise and Fall Time:	5 ns
Output Load:	See Figures
Input Timing Reference Levels:	0.8V, 2.4V
Output Timing Reference Levels:	0.4V, 2.4V

Output Load (A)



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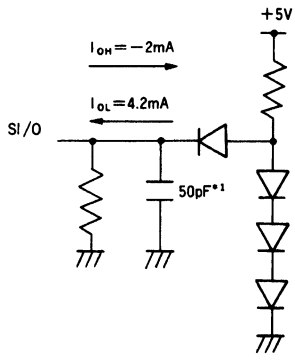
Output Load (B)



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Note: 1. Including scope & jig.

Common Parameter

Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	190	—	220	—	260	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	80	—	90	—	100	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	10000	100	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	30	10000	35	10000	40	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	70	25	85	30	110	ns	5, 6
$\overline{RAS}$ Hold Time	t_{RSH}	30	—	35	—	40	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Transition Time (Rise to Fall)	t_T	3	50	3	50	3	50	ns	
Refresh Period	t_{REF}	—	8	—	8	—	8	ns	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	—	15	—	20	—	ns	
DSF to $\overline{RAS}$ Setup Time	t_{SFS}	0	—	0	—	0	—	ns	
DSF to $\overline{RAS}$ Hold Time	t_{SFH}	25	—	25	—	30	—	ns	
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	0	—	ns	
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	0	—	ns	

Read Cycle (RAM), Page Mode Read Cycle

Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	—	35	—	40	ns	3, 5
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	55	—	70	ns	3, 6
Output Buffer Turn-off Delay Referenced to $\overline{CAS}$	t_{OFF1}	0	25	0	30	0	40	ns	7
Output Buffer Turn-off Delay Referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	7
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	12
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	20	55	20	65	25	80	ns	5, 6
Page Mode Cycle Time	t_{PC}	55	—	65	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	15	—	20	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	60	—	75	ns	

Write Cycle (RAM), Page Mode Write Cycle, Color Register Set Cycle

Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	9
Write Command Hold Time	t_{WCH}	25	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	35	—	40	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	15	—	20	—	ns	
Page Mode Cycle Time	t_{PC}	55	—	65	—	80	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	15	—	20	—	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	255	—	295	—	350	—	ns	
$\overline{RAS}$ Pulse Width	t_{RWS}	165	10000	195	10000	240	10000	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{CWD}	65	—	75	—	90	—	ns	9
Column Address to $\overline{WE}$ Delay	t_{AWD}	80	—	95	—	120	—	ns	9
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	25	—	30	—	40	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	30	—	35	—	40	ns	3, 5
Access Time from $\overline{OE}$	t_{OAC}	—	30	—	35	—	40	ns	3
Address Access Time	t_{AA}	—	45	—	55	—	70	ns	3, 6
$\overline{RAS}$ to Column Address Delay	t_{RAD}	20	55	20	65	25	80	ns	5, 6
Output Buffer Turn-off Delay Referenced to $\overline{OE}$	t_{OFF2}	0	25	0	30	0	40	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	30	—	35	—	40	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	30	—	35	—	40	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	25	—	25	—	30	—	ns	10
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	20	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	20	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	10	—	15	—	20	—	ns	

Refresh Cycle

Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CHR}	20	—	25	—	30	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

Transfer Cycle

Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	20	—	ns	
$\overline{SE}$ to $\overline{RAS}$ Setup Time	t_{ES}	0	—	0	—	0	—	ns	
$\overline{SE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	—	15	—	20	—	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	—	30	—	35	—	ns	
SC to $\overline{RAS}$ Setup Time	t_{SRS}	30	—	40	—	45	—	ns	
$\overline{RAS}$ to QSF Delay Time	t_{RQD}	—	100	—	120	—	150	ns	4
$\overline{RAS}$ to QSF (High) Delay Time	t_{RQH}	—	TBD	—	TBD	—	TBD	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	—	60	—	75	—	ns	
Serial Data Input to $\overline{RAS}$ Delay Time	t_{SZR}	—	10	—	10	—	10	ns	
Serial Output Buffer Turn-off Delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	75	ns	7
$\overline{RAS}$ to S_{out} (Low-Z) Delay Time	t_{RLZ}	5	—	10	—	10	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	60	—	ns	
Access Time from SC	t_{SCA}	—	30	—	40	—	50	ns	4
Serial Data-out Hold Time	t_{SOH}	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	25	—	ns	

Serial Read Cycle

Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	60	—	ns	
Access Time from SC	t_{SCA}	—	30	—	40	—	50	ns	4
Access Time from $\overline{SE}$	t_{SEA}	—	25	—	30	—	40	ns	4
Serial Data-out Hold Time	t_{SOH}	7	—	7	—	7	—	ns	4
SC Pulse Width	t_{SC}	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-off Delay from $\overline{SE}$	t_{SEZ}	0	25	0	25	0	30	ns	7
Last SC to QSF Delay Time	t_{SQD}	—	TBD	—	TBD	—	TBD	ns	4

Serial Write Cycle

Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Serial Clock Cycle Time	t_{SCC}	30	—	40	—	60	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	25	—	ns	
Serial Write Enable Setup Time	t_{SWS}	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	t_{SWH}	30	—	35	—	50	—	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	30	—	35	—	50	—	ns	

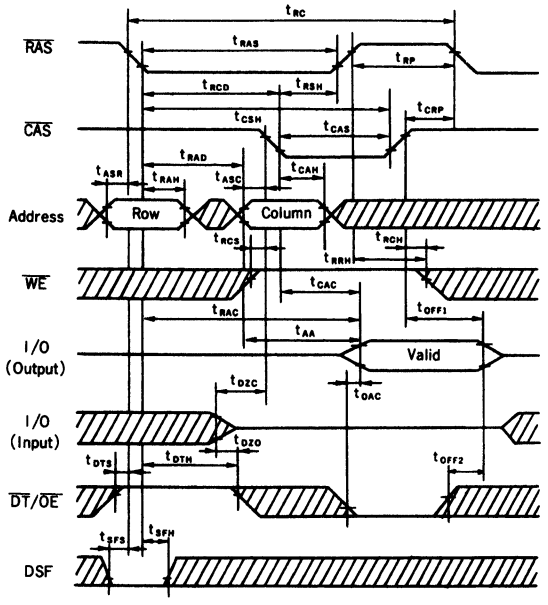
Flash Write Cycle

Parameter	Symbol	HM538123-10		HM538123-12		HM538123-15		Unit	Note
		Min	Max	Min	Max	Min	Max		
Flash Write Cycle Write	t_{RCFW}	230	—	265	—	310	—	ns	
$\overline{RAS}$ Pulse Width	t_{RCSFW}	140	—	165	—	200	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	—	15	—	20	—	ns	
$\overline{CAS}$ High Level Hold Time Reference to $\overline{RAS}$	t_{CHHR}	20	—	25	—	30	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	15	—	15	—	20	—	ns	

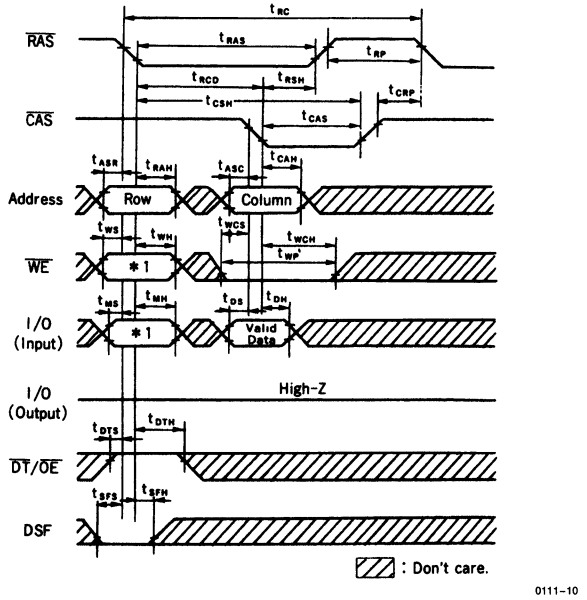
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL load and 100 pF.
4. Measured with a load circuit equivalent to 2 TTL load and 50 pF.
5. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
6. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
7. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition (V_{OH} − 200 mV, V_{OL} + 200 mV).
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
9. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-modify-write cycle; the data of the selected address is read out from a data out pin and input data is written into the selected address. In this case, impedance on I/O pins is controlled by $\overline{OE}$.
10. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles or to $\overline{WE}$ falling edge in delayed write or read-modify-write cycles.
11. After power-up, pause for 100 μs or more and execute at least 8 initialization cycles (normal memory cycles or refresh cycles), then start operation.
12. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.

■ TIMING WAVEFORMS

• Read Cycle

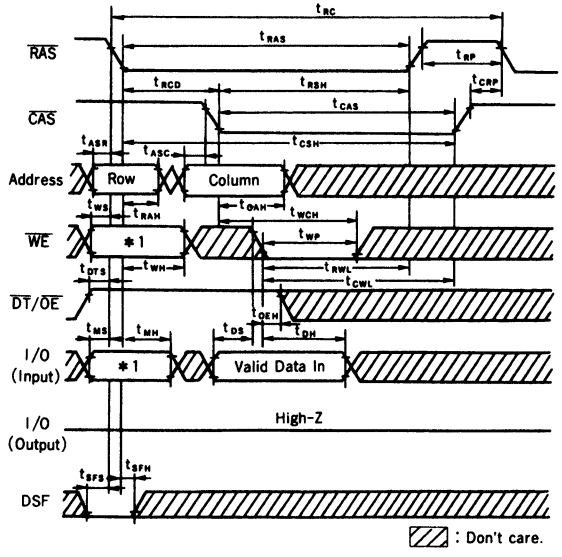


• Early Write Cycle



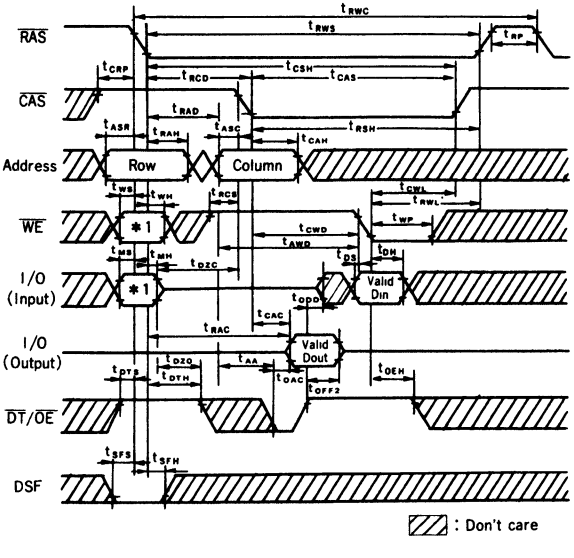
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Delayed Write Cycle**



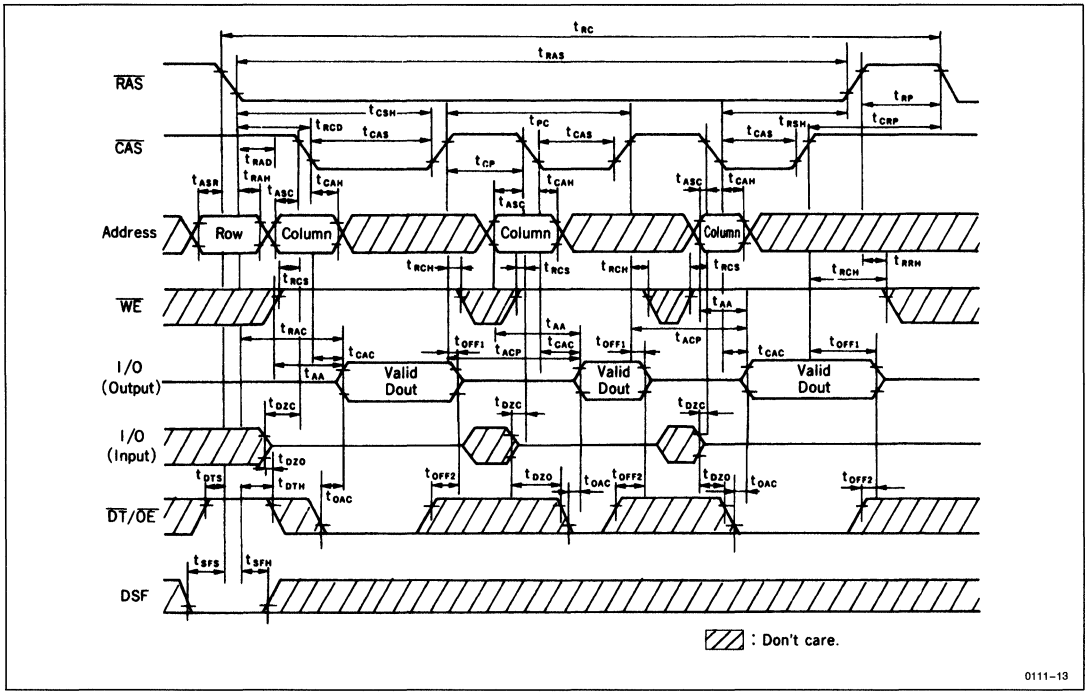
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• **Read-Modify-Write Cycle**

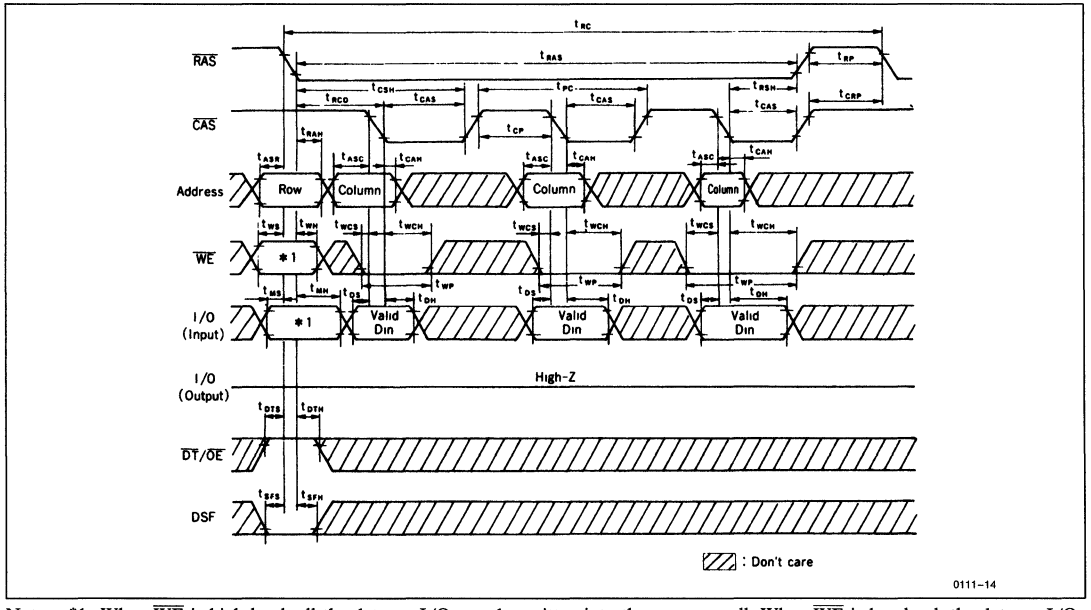


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• Page Mode Read Cycle

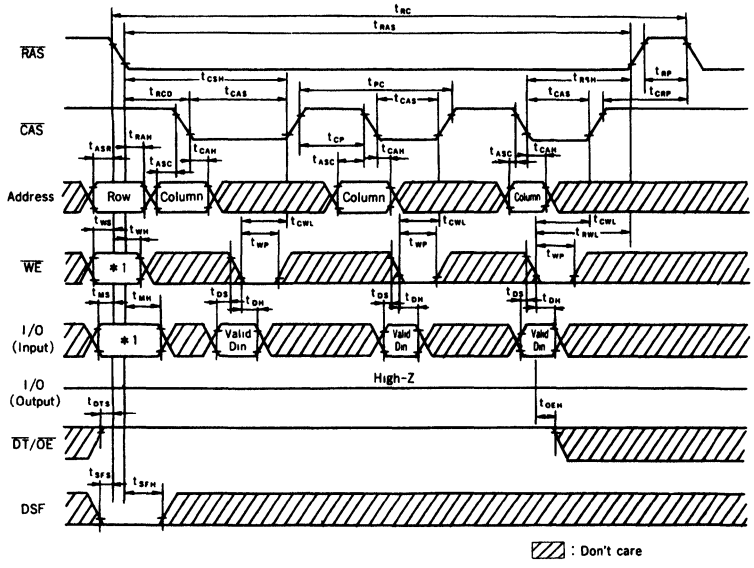


• Page Mode Write Cycle (Early Write)



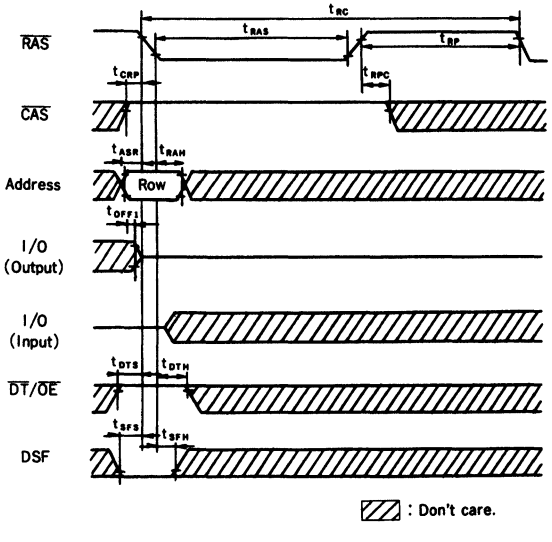
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

• Page Mode Write Cycle (Delayed Write)

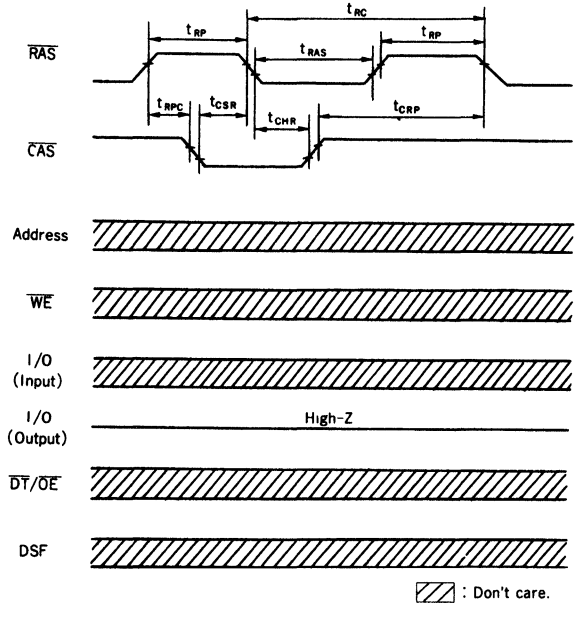


Note: 1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

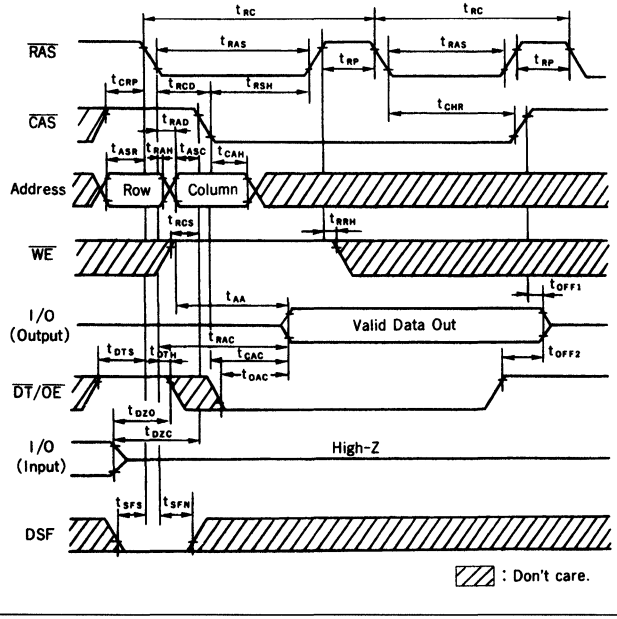
• $\overline{RAS}$ Only Refresh Cycle



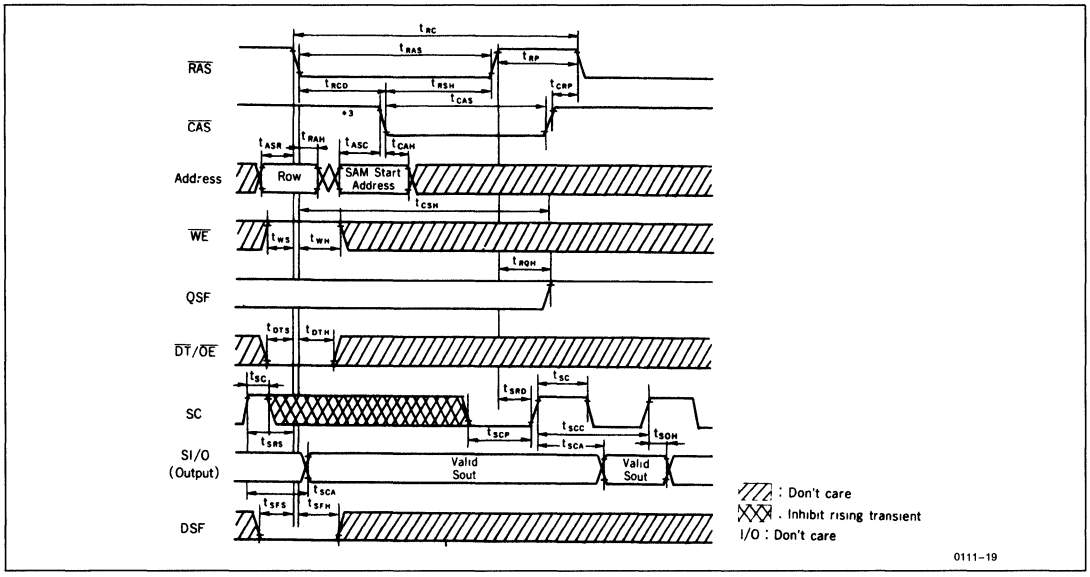
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



• Hidden Refresh Cycle

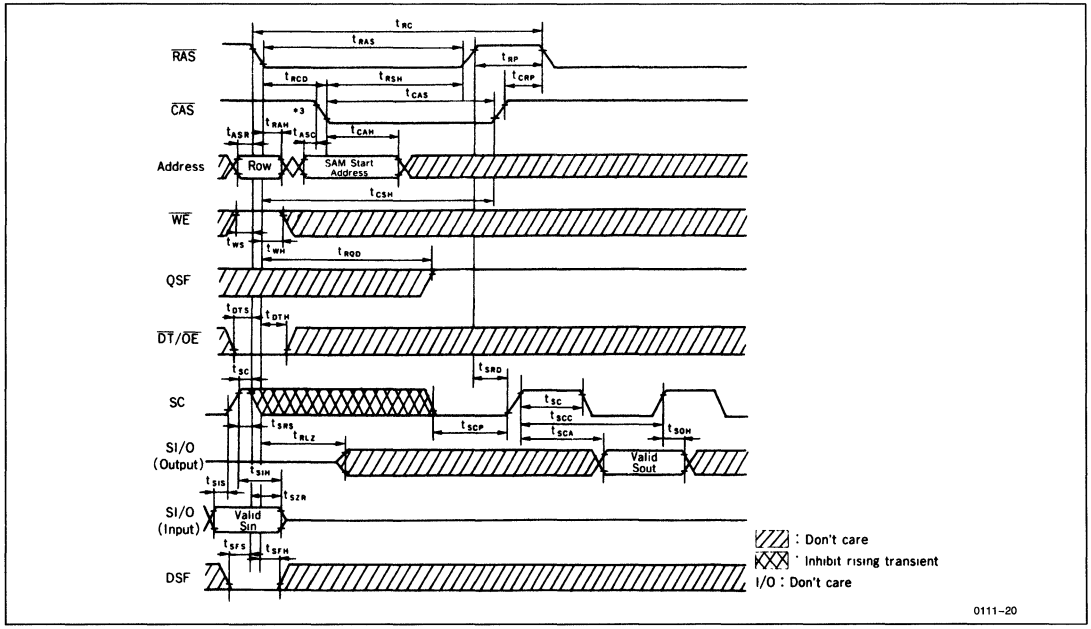


• Special Read Initialization Cycle (1)*1, *2



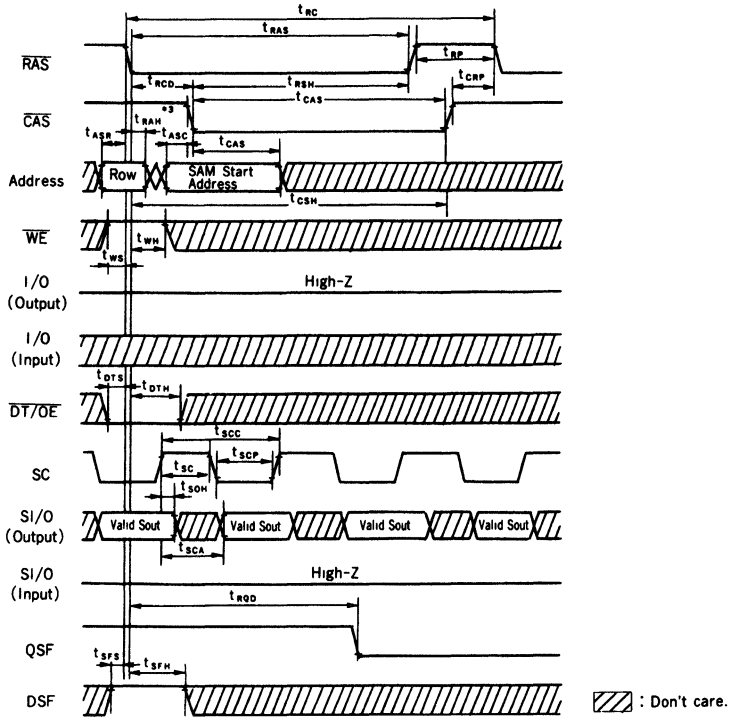
Notes: *1. When the previous data transfer cycle is a special read transfer cycle or special read initialization cycle, it is specified as special read initialization cycle (1).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance state.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• Special Read Initialization Cycle (2)*1, *2



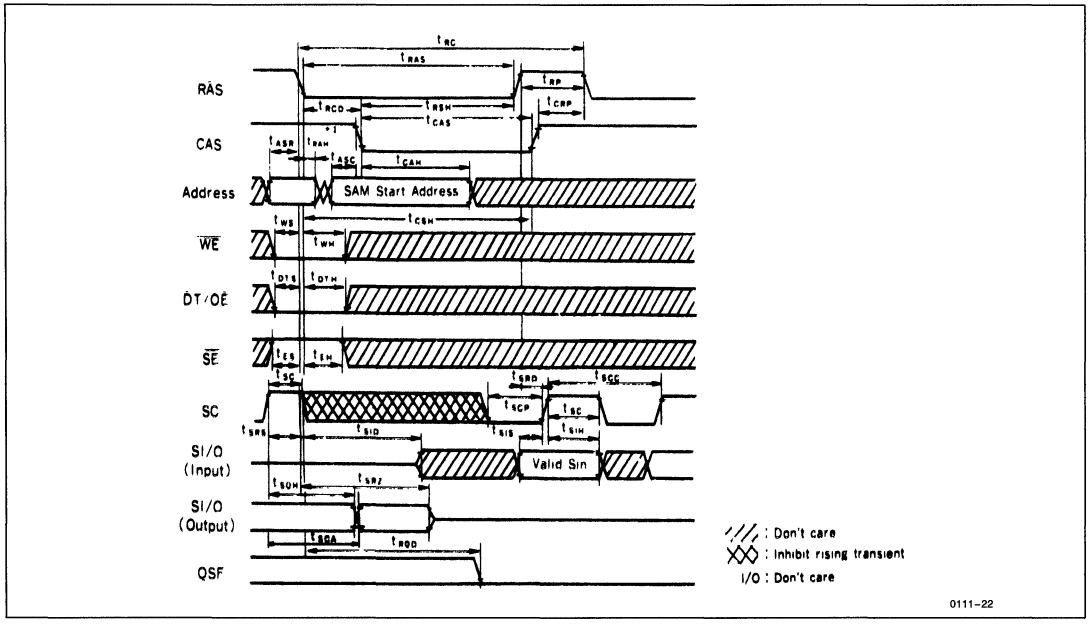
Notes: *1. When the previous data transfer cycle is a write or pseudo transfer cycle, it is specified as special read initialization cycle (2).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance state.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• Special Read Transfer Cycle *1, *2



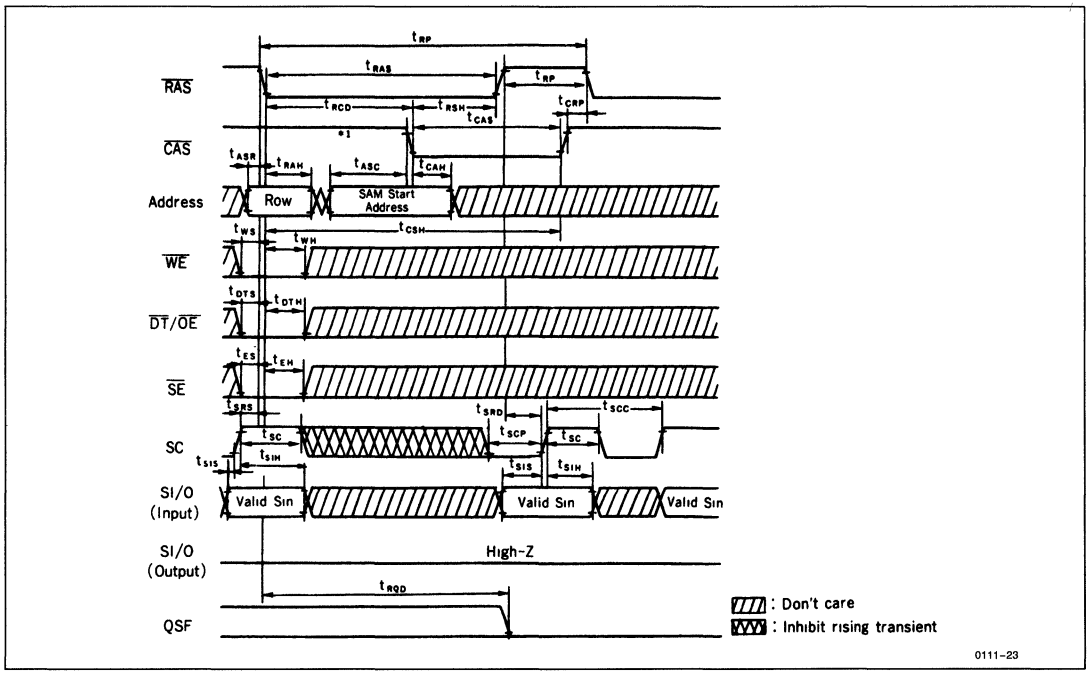
Notes: *1. When QSF is low level at the falling edge of $\overline{RAS}$, the special read transfer cycle is not performed.
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance state.)
*3. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• **Pseudo Transfer Cycle**



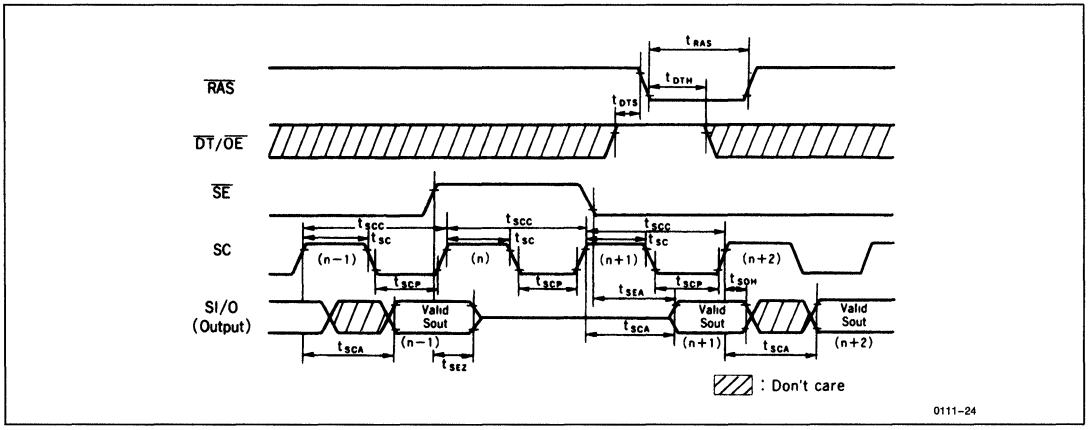
Note: *1. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• **Write Transfer Cycle**

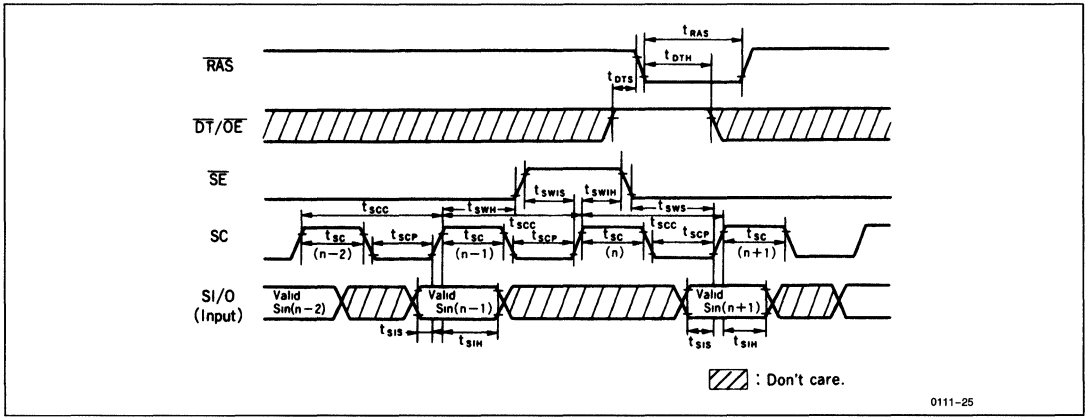


Note: *1. $\overline{CAS}$ and SAM start address don't need to be specified every cycle, if SAM start address is not changed.

• **Serial Read Cycle**

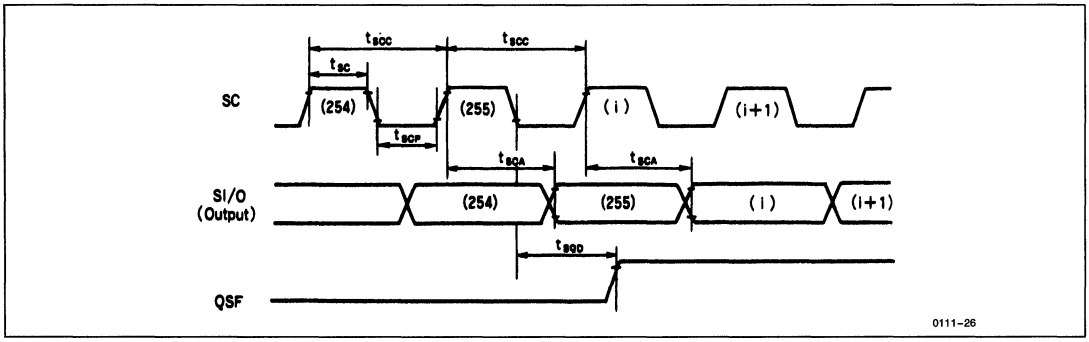


• **Serial Write Cycle** *1, *2



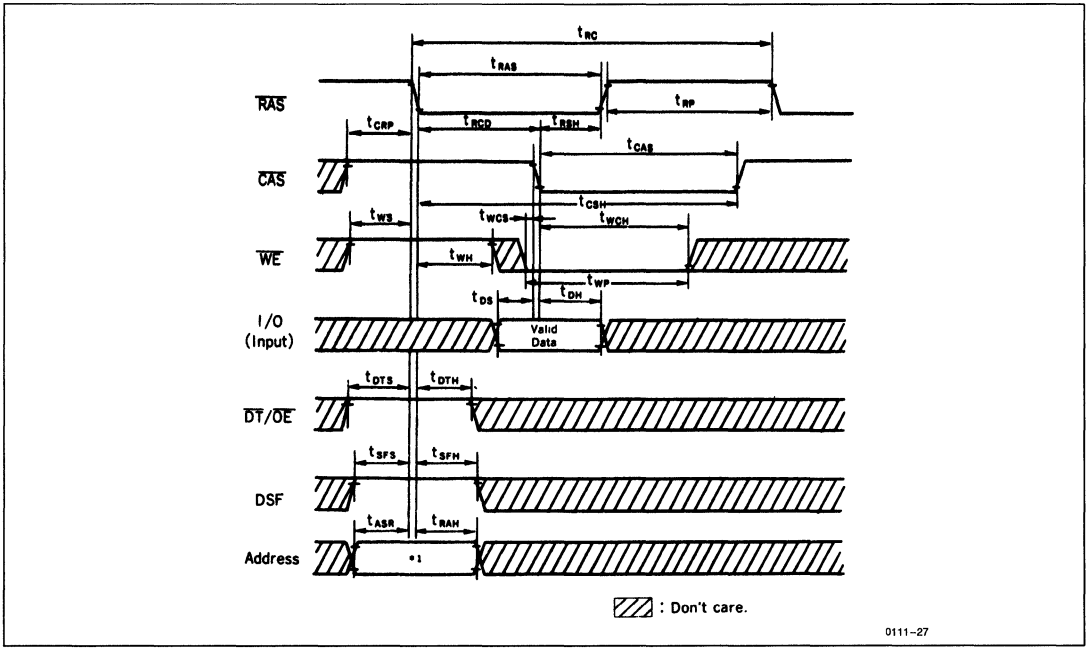
Note: *1. When $\overline{SE}$ is high level in a serial write cycle, data is not written into SAM, however, the pointer is incremented.
*2. Address 0 is accessed next to address 255.

• **Serial Read Cycle (Around Address 255 in SAM)**



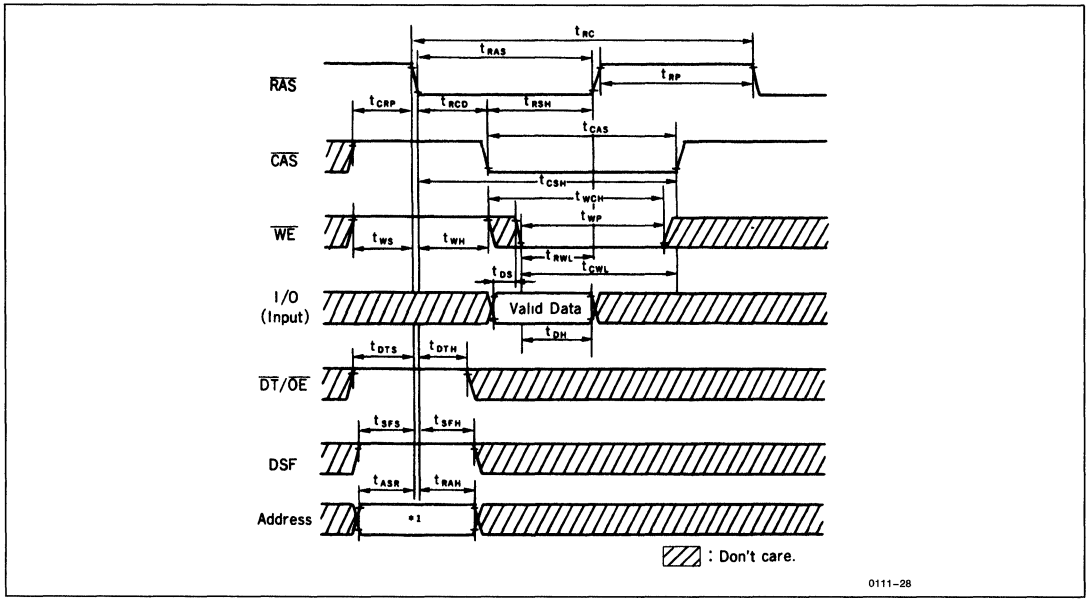
Note: *1. Address (i) is the SAM start address provided in the previous special read transfer cycle. When special read transfer cycle isn't executed (QSF remains in high level), address 0 is accessed next to address 255.

• **Color Register Set Cycle (Early Write)**



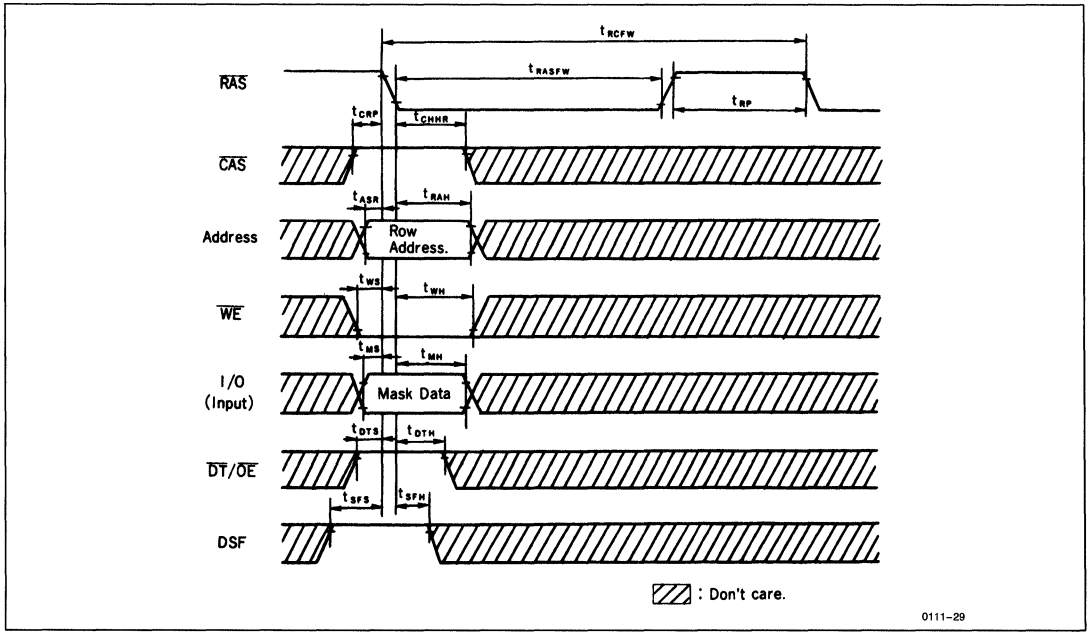
Note: *1. The level of address pin is don't care, but cannot be changed in this period.

Color Register Set Cycle (Delayed Write)



Note: *1. The level of address pin is don't care, but cannot be changed in this period.

• Flash Write Cycle



HM538123A Series

Preliminary

131,072-Word x 8-Bit Multiport CMOS Video RAM

■ DESCRIPTION

The HM538123A is a 1-Mbit multiport video RAM equipped with a 128k-word x 8-bit dynamic RAM and a 256-word x 8-bit SAM (serial access memory). Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has a logic operation mode by internal logic-arithmetic unit and a write mask function. In addition, it has two modes to realize fast writing in RAM. Block write and flash write modes clear the data of 4-word x 8-bit and the data of one row (256-word x 8-bit) respectively in one cycle of RAM. And the HM538123A makes split transfer cycle possible by dividing SAM into two split buffers equipped with 128-word x 8-bit each. This cycle can transfer data to SAM which is not active, and enables a continuous serial access.

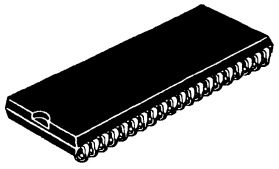
■ FEATURES

- Multiport Organization
  - Asynchronous and Simultaneous Operation of RAM and SAM Capability
  - RAM: 128k-word x 8-bit and SAM: 256-word x 8-bit
- Access Time RAM .....80 ns/100 ns (max)
  SAM.....25 ns/25 ns (max)
- Cycle Time RAM.....150 ns/190 ns (min)
  SAM .....30 ns/30 ns (min)
- Low Power
  - Active RAM.....360 mW (max)
    SAM .....280 mW (max)
  - Standby.....38.5 mW (max)
- High-Speed Page Mode Capability
- Logic Operation Mode Capability
- Mask Write Mode Capability
- Bidirectional Data Transfer Cycle between RAM and SAM Capability
- Split Transfer Cycle Capability
- Block Write Mode Capability
- Flash Write Mode Capability
- 3 Variations of Refresh (8 ms/512 cycles)
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
  - Hidden Refresh
- TTL Compatible

■ PIN DESCRIPTION

Pin Name	Function
A_0–A_8	Address Input
I/O_0–I/O_7	RAM Port Data Inputs/Outputs
SI/O_0–SI/O_7	SAM Port Data Inputs/Outputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{DT/OE}$	Data Transfer/Output Enable
SC	Serial Clock
$\overline{SE}$	SAM Port Enable
DSF	Special Function Input Flag
QSF	Special Function Output Flag
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

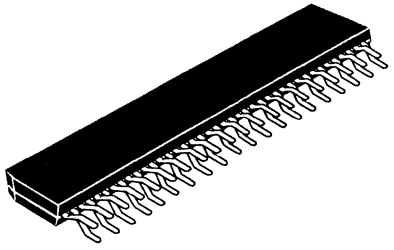
HM538123AJ Series



3DCP40D

(CP-40D)

HM538123AZ Series

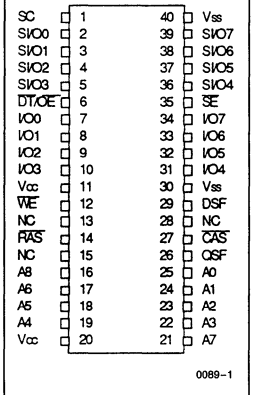


3DZP40

(ZP-40)

■ PIN OUT

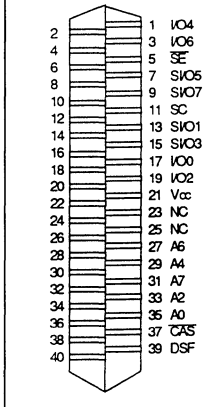
HM538123AJ Series



0089-1

(Top View)

HM538123AZ Series



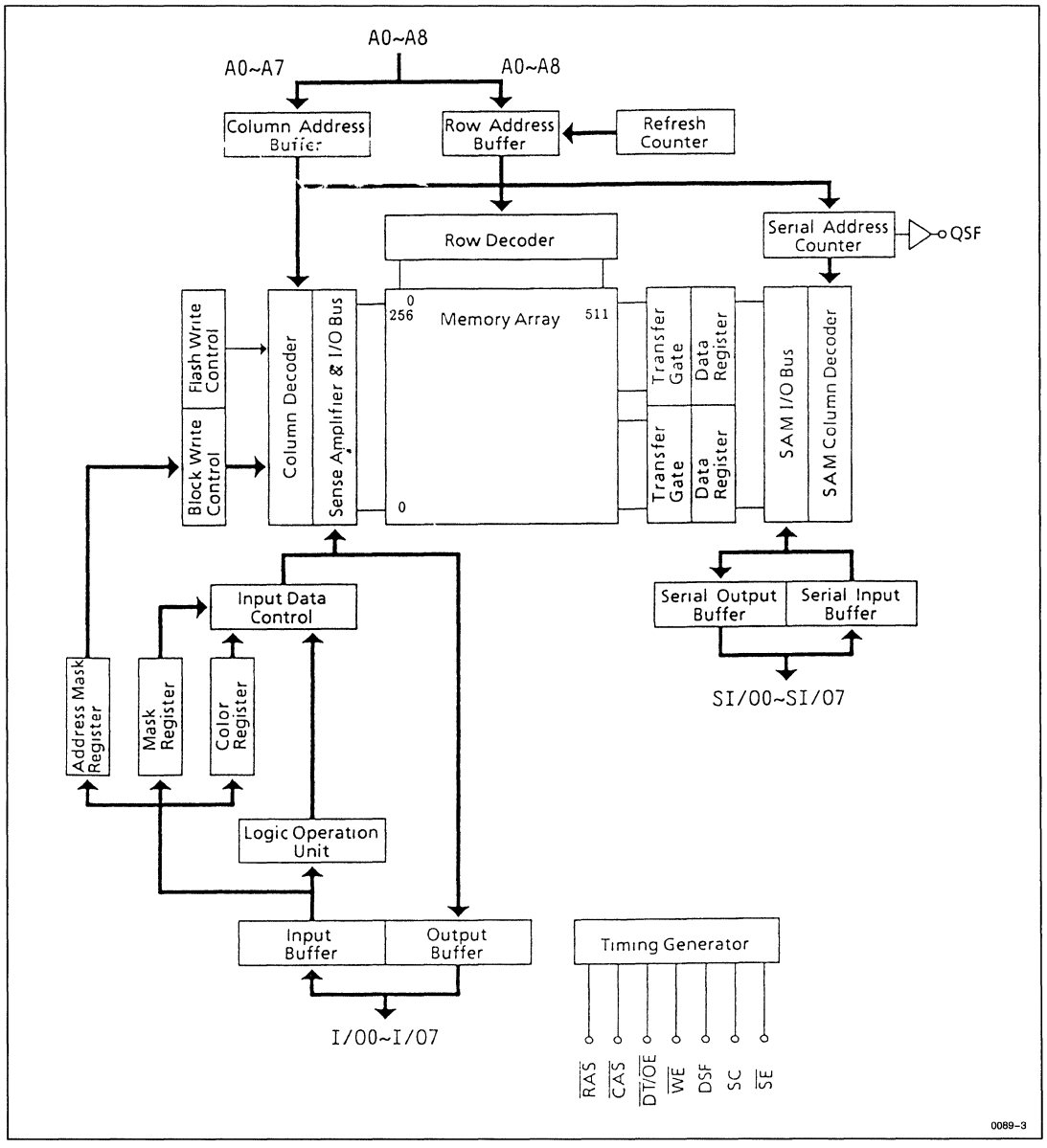
0089-2

(Bottom View)

■ ORDERING INFORMATION

Part No.	Access Time	Package
HM538123AJ-8 HM538123AJ-10	80 ns 100 ns	400 mil 28-pin Plastic SOJ (CP-28D)
HM538123AZ-8 HM538123AZ-10	80 ns 100 ns	475 mil 28-pin Plastic ZIP (ZP-40)

■ BLOCK DIAGRAM



■ PIN FUNCTIONS

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of these signals determine the operation cycle of the HM538123A.

$\overline{CAS}$ (input pin): Column address and DSF signal are fetched into chip at the falling edge of $\overline{CAS}$, which determines the operation mode of HM538123A. $\overline{CAS}$ controls output impedance of I/O in RAM.

A_0–A_8 (input pins): Row address (AX_0–AX_8) is determined by A_0–A_8 level at the falling edge of $\overline{RAS}$. Column address (AY_0–AY_7) is determined by A_0–A_7 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM538123A turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O_0–I/O_7 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only to high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM. In block write cycle, they function as address mask data at the falling edge of $\overline{CAS}$.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is fetched into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not fetched into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O_0–SI/O_7 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

DSF (input pin): DSF is a special function data input flag pin. It is set to high at the falling edge of $\overline{RAS}$ when new functions such as color register read/write, split transfer, and flash write, are used. DSF is set to high at the falling edge of $\overline{CAS}$ when block write is executed.

QSF (output pin): QSF outputs data of address A_7 in SAM. QSF is switched from low to high by accessing address 127 in SAM and from high to low by accessing 255 address in SAM.

• Table 1. Operation Cycles of the HM538123A

Input Level at the Falling Edge of $\overline{RAS}$					DSF at the Falling Edge of $\overline{CAS}$	Operation Mode
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SE}$	DSF		
L	X	L	X	X	—	Logic Operation Set/Reset
L	X	H	X	X	—	CBR Refresh
H	L	L	L	L	X	Write Transfer
H	L	L	H	L	X	Pseudo Transfer
H	L	L	X	H	X	Split Write Transfer
H	L	H	X	L	X	Read Transfer
H	L	H	X	H	X	Split Read Transfer
H	H	L	X	L	L	Read/Mask Write
H	H	L	X	L	H	Mask Block Write
H	H	L	X	H	X	Flash Write
H	H	H	X	L	L	Read/Write
H	H	H	X	L	H	Block Write
H	H	H	X	H	X	Color Register Read/Write

Note: X: Don't care.

■ OPERATION OF HM538123A

• RAM Read Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF low at the falling edge of $\overline{RAS}$, DSF low at the falling edge of $\overline{CAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

• RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write) ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF low at the falling edge of $\overline{RAS}$, DSF low at the falling edge of $\overline{CAS}$)

- Normal Mode Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after driving $\overline{RAS}$ low, a write cycle is executed and I/O data is written in the selected addresses. When all 8 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes in high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables read/write at the same address in one cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and driving $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

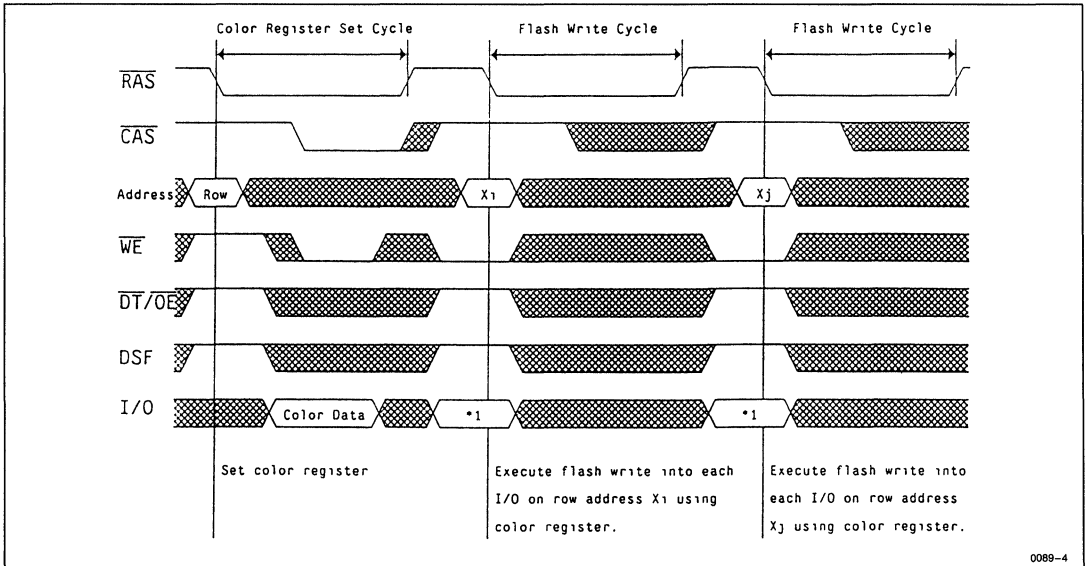
If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is retained. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode, the mask data is retained during the page access.

• High-Speed Page Mode Cycle ($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high and DSF low at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle. In this cycle, read, write, and block write cycles can be mixed. Note that address access time (t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 256-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 μs).

• Color Register Set/Read Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ high and DSF high at the falling edge of $\overline{RAS}$)

In color register set cycle, color data is set to the internal color register used in flash write cycle or block write cycle. 8 bits of internal color register are provided at each I/O. This register is composed of static circuits, so once it is set, it retains the data until reset. Color register set cycle is just the same as the usual write cycle except that DSF is set high at the falling edge of $\overline{RAS}$, and read, early write and delayed write cycle can be executed. In this cycle, HM538123A refreshes the row address fetched at the falling edge of $\overline{RAS}$.



*1 I/O Mask Data
Low: Mask
High: Non Mask

Figure 1. Use of Flash Write

• **Flash Write Cycle** ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high, $\overline{WE}$ low and DSF high at the falling edge of $\overline{RAS}$)

In a flash write cycle, a row of data (256-word x 8-bit) is cleared to 0 or 1 at each I/O according to the data of color register mentioned before. It is also necessary to mask I/O in this cycle. When $\overline{CAS}$ and $\overline{DT}/\overline{OE}$ is set high, $\overline{WE}$ is low, and DSF is high at the falling edge of $\overline{RAS}$, this cycle starts. Then, the row address to clear is given to row address and mask data is given to I/O. Mask data is the same as that of a RAM write cycle. High I/O is cleared, low I/O is not cleared and the internal data is retained. Cycle time is the same as those of RAM read/write cycles, so all bits can be cleared in 1/256 of the usual cycle time. (See figure 1.) If this cycle is executed in logic operation mode described later, the logic operation mode is reset only in the cycle and masked data in this cycle is written.

• **Block Write Cycle** ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ high and DSF low at the falling edge of $\overline{RAS}$, DSF high at the falling edge of $\overline{CAS}$)

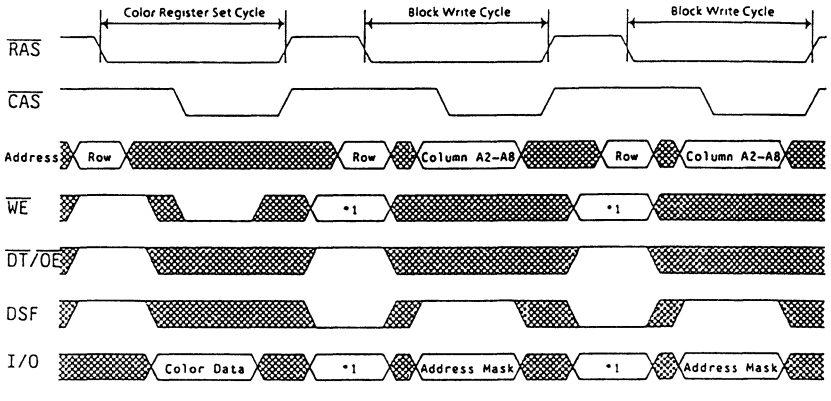
In a block write cycle, 4 columns of data (4-word x 8-bit) is cleared to 0 or 1 at each I/O according to the data of color register. Column addresses A0 and A1 are disregarded. The data on I/Os and addresses can be masked. I/O level at the falling edge of $\overline{CAS}$ determines the address to be cleared. (See figure 2.) If this cycle is executed in logic operation mode described later, the logic operation mode is reset only in the cycle and masked data in this cycle is written.

• Normal Mode Block Write Cycle ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

The data on 8 I/Os are all cleared when $\overline{WE}$ is high at the falling edge of $\overline{RAS}$.

• Mask Block Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, HM538123A starts mask block write mode to clear the data on an optional I/O. The mask data is the same as that of a RAM write cycle. High I/O is cleared, low I/O is not cleared and the internal data is retained. The mask data is available in the $\overline{RAS}$ cycle. In page mode block write cycle, the mask data is retained during the page access.



Note *1

$\overline{WE}$	I/O	Mode
Low	I/O Mask Data	Mask
High	Don't Care	Non Mask

I/O Mask Data
Low: Mask
High: Non Mask

Address Mask Data

I/O_0	Column0 ($A_0 = 0, A_1 = 0$) Mask Data	Low: Mask
I/O_1	Column1 ($A_0 = 1, A_1 = 0$) Mask Data	
I/O_2	Column2 ($A_0 = 0, A_1 = 1$) Mask Data	High: Non Mask
I/O_3	Column3 ($A_0 = 1, A_1 = 1$) Mask Data	

Figure 2. Use of Block Write

• Transfer Operation

The HM538123A provides the read transfer cycle, split read transfer cycle, pseudo transfer cycle, write transfer cycle and split write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{CAS}$ high and $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$. They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle).

Read transfer cycle and split read transfer cycle: RAM to SAM

Write transfer cycle and split write transfer cycle: SAM to RAM

(2) Determine SI/O state (except for split read transfer cycle and split write transfer cycle).

Read transfer cycle: SI/O output

Pseudo transfer cycle and write transfer cycle: SI/O input

(3) Determine first SAM address to access after transferring at column address (SAM start address).

SAM start address must be determined by read transfer cycle or pseudo transfer cycle (split transfer cycle isn't available) before SAM access, after power on, and determined for each transfer cycle.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high and DSF low at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high and DSF low at the falling edge of $\overline{RAS}$. The row address data (256 x 8-bit) determined by this cycle is transferred to SAM data register synchronously at the rising edge of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address determined by column address. In read transfer cycle, $\overline{DT}/\overline{OE}$ must be risen to transfer data from RAM to SAM.

This cycle can access SAM even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge and t_{SDH} (min) specified between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge must be satisfied. (See figure 3.)

When read transfer cycle is executed, SI/O becomes output state by first SAM access. Input must be set high impedance before t_{SZS} (min) of the first SAM access to avoid data contention.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, $\overline{SE}$ high and DSF low at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle switches SI/O to input state and set SAM start address without data transfer to RAM.

This cycle starts when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, $\overline{SE}$ high and DSF low at the falling edge of $\overline{RAS}$. Data should be input to SI/O later than t_{SID} (min) after $\overline{RAS}$ becomes low to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC must not be risen.

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, $\overline{SE}$ low and DSF low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address for serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC must not be risen. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by write transfer cycle. However, the address to write data must be the same as that of the read transfer cycle or the split read transfer cycle (row address AX_8).

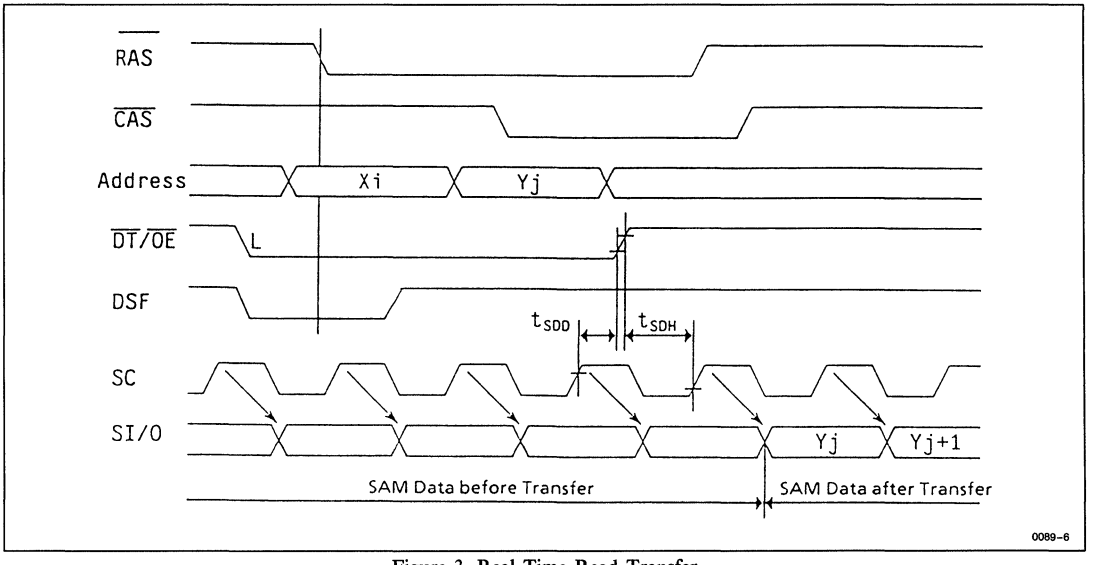


Figure 3. Real Time Read Transfer

Split Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high and DSF high at the falling edge of $\overline{RAS}$)

To execute a continuous serial read by real time read transfer, HM538123A must satisfy SC and $\overline{DT}/\overline{OE}$ timings and requires an external circuit to detect SAM last address. Split read transfer cycle makes it possible to execute a continuous serial read without the above timing limitation. Figure 4 shows the block diagram for a split transfer. SAM data register (DR) consists of 2 split buffers, whose organizations are 128-word x 8-bit each. Let us suppose that data is read from upper data register DR1 (the row address AX_8 is 0 and SAM address A_7 is 1). When split read transfer is executed setting row address AX_8 0 and SAM start addresses A_0 to A_6, 128-word x 8-bit data are transferred from RAM to the lower data register DR0 (SAM address A_7 is 0) automatically. After data are read from data register DR1, data start to be read from SAM start addresses of data register DR0. If the next split read transfer isn't executed while data are read from data register DR0, data start to be read from SAM start address 0 of DR1 after data are read from data register DR0. If split read transfer is executed setting row address AX_8 1 and SAM start addresses A_0 to A_6 while data are read from data register DR1, 128-word x 8-bit data are transferred to data register DR2. After data are read from data register DR1, data start to be read from SAM start addresses of data register DR2. If the next split read transfer isn't executed while data is read from data register DR2, data start to be read from SAM start address 0 of data register DR3 after data are read from data register DR2. In this time, SAM data is the one transferred to data register DR3 finally while row address AX_8 is 1. In split read data transfer, the SAM start address A_7 is automatically set in the data register which isn't used.

The data on SAM address A_7, which will be accessed next, outputs to QSF, QSF is switched from low to high by accessing SAM last address 127 and from high to low by accessing address 255.

Split read transfer cycle is set when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ is low, $\overline{WE}$ is high and DSF is high at the falling edge of $\overline{RAS}$. The cycle can be executed asynchronously with SC. However, HM538123A must be satisfied t_{STS} (min) timing specified between SC rising and $\overline{RAS}$ falling. SAM start address must be accessed, satisfying t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings specified between $\overline{RAS}$ or $\overline{CAS}$ falling and column address. (See figure 5.)

In split read transfer, SI/O isn't switched to output state. Therefore, read transfer must be executed to switch SI/O to output state when the previous transfer cycle is pseudo transfer or write transfer cycle.

Split Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low and DSF high at the falling edge of $\overline{RAS}$)

A continuous serial write cannot be executed because accessing SAM is inhibited during $\overline{RAS}$ low in write transfer. Split write transfer cycle makes it possible. In this cycle, t_{STS} (min), t_{RST} (min), t_{CST} (min) and t_{AST} (min) timings must be satisfied like split read transfer cycle. And it is impossible to switch SI/O to input state in this cycle. If SI/O is in output state, pseudo transfer cycle should be executed to switch SI/O into input state. Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other addresses of RAM by split write transfer cycle. However, pseudo transfer cycle must be executed before split write transfer cycle. And the MSB of row address (AX_8) to write data must be the same as that of the read transfer cycle or the split read transfer cycle.

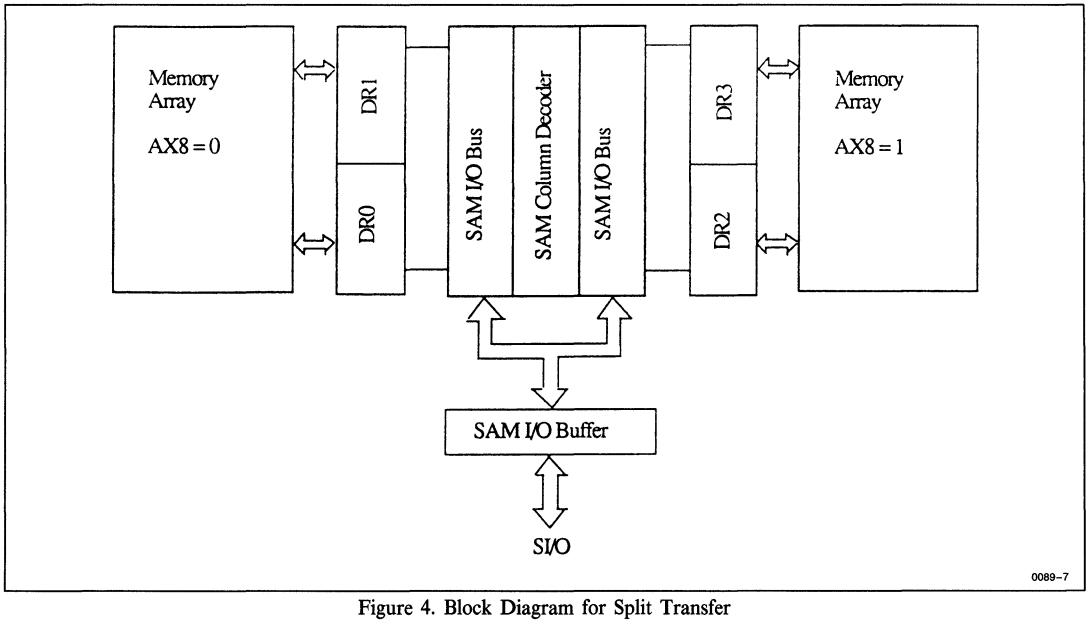


Figure 4. Block Diagram for Split Transfer

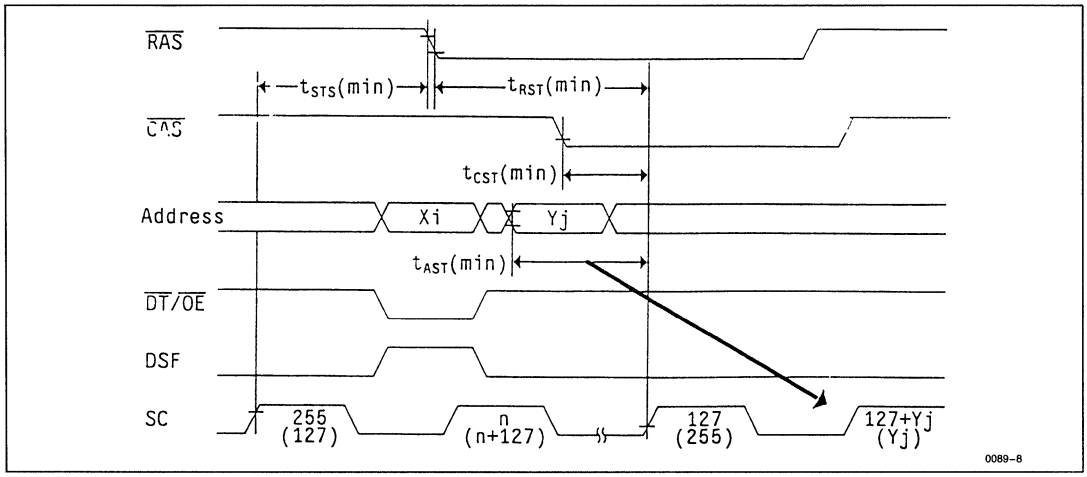


Figure 5. Limitation in Split Transfer

• SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. When $\overline{SE}$ is set high, SI/O becomes high impedance, and the internal pointer is incremented by the SC rising. After indicating the last address (address 255), the internal pointer indicates address 0 at the next access.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is fetched into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't fetched into data register. Internal pointer is incremented by the SC rising, so $\overline{SE}$ high can be used as mask data for SAM. After indicating the last address (address 255), the internal pointer indicates address 0 at the next access.

• Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is executed by accessing all 512 row addresses within 8 ms. There are three refresh cycles: (1) $\overline{RAS}$ only refresh cycle, (2) $\overline{CAS}$ before $\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required when all row addresses are accessed within 8 ms.

(1) $\overline{RAS}$ Only Refresh Cycle: $\overline{RAS}$ only refresh cycle is executed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high after inputting the row address (= refresh address) from external circuits. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ must be high at the falling edge of $\overline{RAS}$.

(2) CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.

To distinguish this cycle from logic operation set/reset cycle, $\overline{WE}$ must be high at the falling edge of $\overline{RAS}$.

(3) Hidden Refresh Cycle: Hidden refresh cycle executes CBR refresh with the data output by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register and selector), organized as fully static circuitry, require no refresh.

• Logic Operation Mode

The HM538123A supports logic operation capability on RAM port. It executes logic operation between the memory cell data and external input data in logic operation mode write cycle, and writes the result into the memory cell (read-modify-write). This function realizes high speed raster operations and simplifies peripheral circuits for raster operations.

Logic Operation Set/Reset Cycle ($\overline{CAS}$ low and $\overline{WE}$ low at the falling edge of $\overline{RAS}$)

In logic operation set/reset cycle, the following operations are executed at the same time; 1. Selection of logic operations and logic operation mode set/reset, 2. Mask data programming, 3. CBR refresh.

Figure 6 shows the timing for logic operation set/reset cycle. This cycle starts when $\overline{CAS}$ and $\overline{WE}$ are low at the falling edge of $\overline{RAS}$. In this cycle, logic operation codes and mask data are programmed by row address and I/O pin respectively at the falling edge of $\overline{RAS}$. When write cycle is executed after this cycle, the logic operation write cycle starts. In the logic operation mode, the specification of cycle time is longer than that of normal mode because read-modify-write cycle, which writes the operation result of external data and memory cell data into memory cell, is executed internally. In this cycle, logic operation codes and mask data programmed are available until reprogrammed. Mask data is available only for one $\overline{RAS}$ cycle, in mask write cycle, mask block write cycle and flash write cycle. Here, the mask data

programmed in mask write cycle, mask block write cycle and flash write cycle is named as "temporary mask data" and the one programmed in logic operation set/reset cycle is named as "mask data".

- Selection of Logic Operations and Logic Operation Mode Set/Reset

Table 2 shows the logic operations. One operation is selected among sixteen ones by combinations of A_0–A_3 levels at the falling edge of $\overline{RAS}$. (A_4–A_8 are Don't care.) Logic operation codes (A_3,A_2,A_1,A_0) = (0,1,0,1)(THROUGH) resets the logic operation mode. When write cycle is executed after that, normal write cycle starts. However, even in this case, mask data is still available. I/O must be at high level at the falling edge of $\overline{RAS}$ in logic operation set/reset cycle when mask data is not used.

- Mask Data Programming

High/low level of I/O at the falling edge of $\overline{RAS}$ functions as mask data. When I/O is high, the data is written in write cycle. When I/O is low, the input data is masked and the same memory cell data remains. Mask data, programmed in

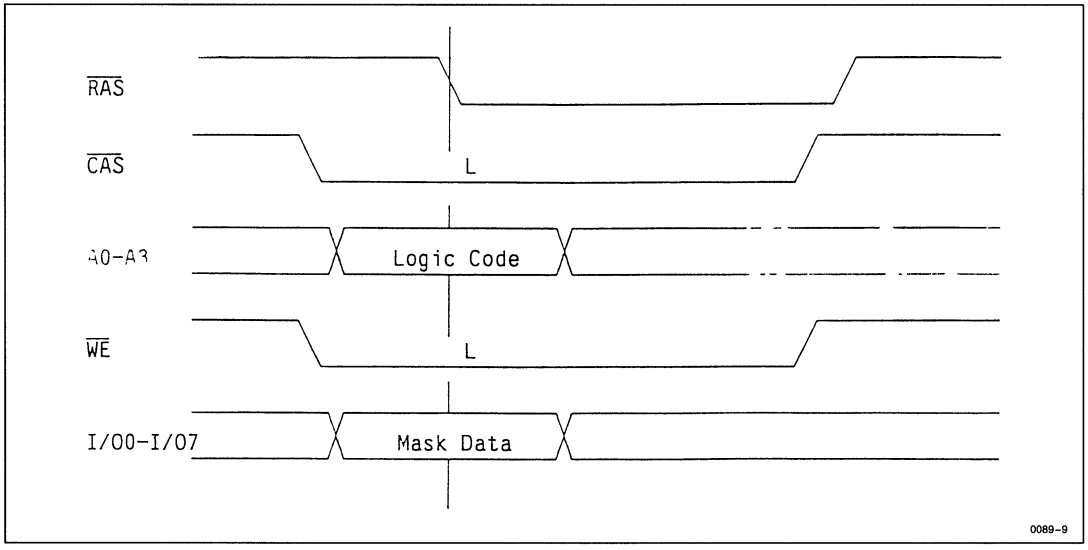


Figure 6. Logic Operation Set/Reset

• Table 2. Logic Code

Logic Code				Symbol	Write Data	Note
A_3	A_2	A_1	A_0			
0	0	0	0	ZERO	0	Logic Operation Mode Set
0	0	0	1	AND1	Di•Mi	
0	0	1	0	AND2	$\overline{Di}$•Mi	
0	0	1	1	—	Mi	
0	1	0	0	AND3	Di•$\overline{Mi}$	
0	1	0	1	THROUGH	Di	Logic Operation Mode Reset
0	1	1	0	EOR	$\overline{Di}$•Mi + Di•$\overline{Mi}$	Logic Operation Mode Set
0	1	1	1	OR1	Di + Mi	
1	0	0	0	NOR	$\overline{Di}$•$\overline{Mi}$	
1	0	0	1	ENOR	Di•Mi + $\overline{Di}$•$\overline{Mi}$	
1	0	1	0	INV1	$\overline{Di}$	
1	0	1	1	OR2	$\overline{Di}$ + Mi	
1	1	0	0	INV2	$\overline{Mi}$	
1	1	0	1	OR3	Di + $\overline{Mi}$	
1	1	1	0	NAND	$\overline{Di}$ + $\overline{Mi}$	
1	1	1	1	ONE	1	

Note: Di: External Data-in.
Mi: The data of the memory cell.

this cycle, is available until reprogrammed. It is advantageous when the same mask data continues.

Also, temporary mask data can be programmed by falling $\overline{WE}$ at the falling edge of $\overline{RAS}$ in logic operation mode cycle, after mask data is programmed. The temporary mask data is available only for one cycle.

Logic operation is reset during temporary mask write cycle. It means that external input data is written into I/O whose temporary mask data is 1. (See figure 7.) These functions are useful when RAM port is divided into frame buffer area and data area, as they save the need to reprogram logic operation codes and mask them.

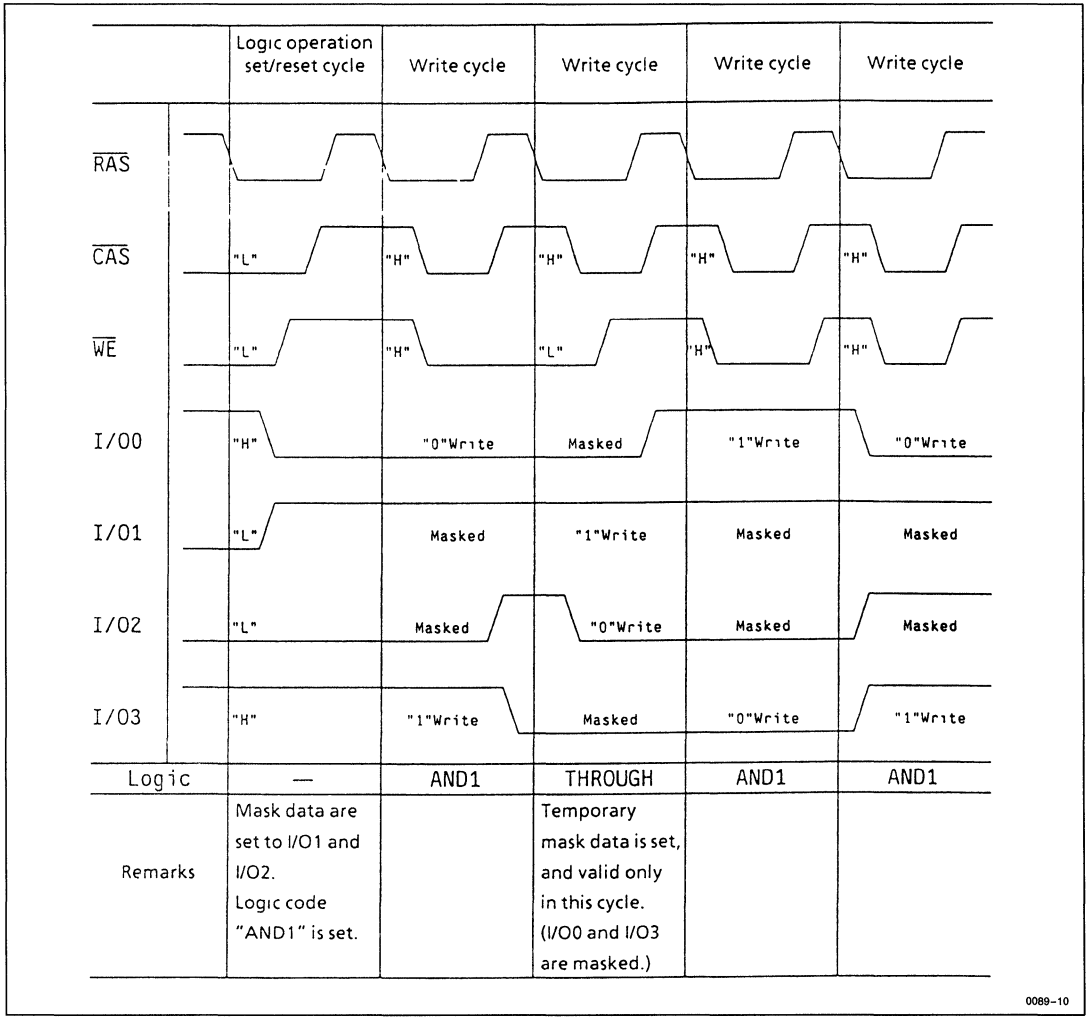


Figure 7. 2 Types of Mask Write Function and Logic Operation Function

Logic Operation Mode Write Cycle (Early Write, Delayed Write and Page Mode)

Write cycle after logic operation set cycle is logic operation mode write cycle. However, this mode is reset in block write, mask block write, flash write, and mask write cycle. In logic operation mode write cycle, the following read-modify-write operation is executed internally.

(1) Reading memory cell data in given address into internal bus.

(2) Executing operation between the data given in I/O pin and memory cell data.

(3) Writing the result of (2) into address given by (1).

Figure 8 shows the sequence of raster operation. Raster operation which needs 3 cycles (destination read, operation and destination write) in normal mode can be executed in one write cycle of logic operation mode. It makes raster operation faster and simplifies peripheral hardware for raster operation.

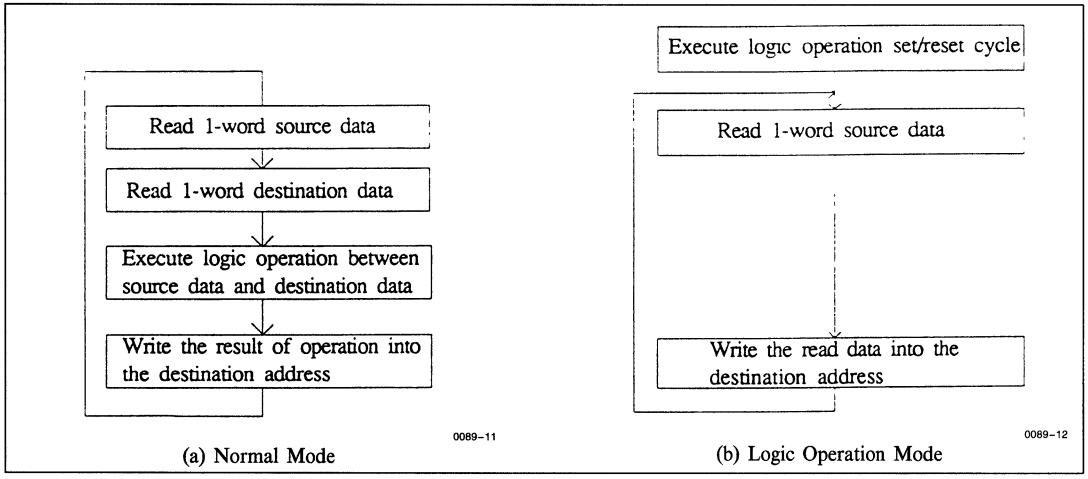


Figure 8. Sequence of Raster Operation

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Note
Terminal Voltage	V_T	− 1.0 to + 7.0	V	1
Power Supply Voltage	V_{CC}	− 0.5 to + 7.0	V	1
Power Dissipation	P_T	1.0	W	
Operating Temperature	T_{opr}	0 to + 70	°C	
Storage Temperature	T_{stg}	− 55 to + 125	°C	

Note: 1. Relative to V_{SS}.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	− 0.5	—	0.8	V	1, 2

Notes: 1. All voltages referenced to V_{SS}.
2. − 3.0V for pulse width ≤ 10 ns.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	HM538123A-8		HM538123A-10		Unit	Test Conditions		Note
		Min	Max	Min	Max		RAM Port	SAM Port	
Operating Current	I_{CC1}	—	65	—	50	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC7}	—	115	—	100	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Standby Current	I_{CC2}	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC8}	—	50	—	50	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	65	—	50	mA	$\overline{RAS}$ Cycling $\overline{CAS}$ = V_{IH} t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC9}	—	115	—	100	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Page Mode Current	I_{CC4}	—	70	—	65	mA	$\overline{CAS}$ Cycling $\overline{RAS}$ = V_{IL} t_{PC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC10}	—	120	—	115	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC5}	—	55	—	40	mA	$\overline{RAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC11}	—	105	—	90	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Data Transfer Current	I_{CC6}	—	75	—	60	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC12}	—	125	—	110	mA		$\overline{SE}$ = V_{IL}, SC Cycling t_{SCC} = Min	
Input Leakage Current	I_{LI}	−10	10	−10	10	µA			
Output Leakage Current	I_{LO}	−10	10	−10	10	µA			
Output High Voltage	V_{OH}	2.4	—	2.4	—	V	I_{OH} = −2 mA		
Output Low Voltage	V_{OL}	—	0.4	—	0.4	V	I_{OL} = 4.2 mA		

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.

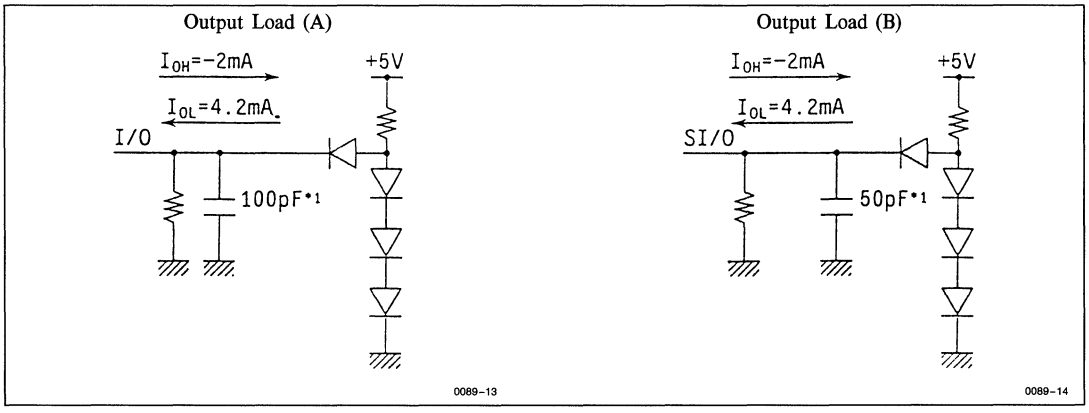
• Capacitance (T_A = 25°C, V_{CC} = 5V, f = 1 MHz, Bias: Clock, I/O = V_{CC}, Address = V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Address	C_{11}	—	—	5	pF
Clock	C_{12}	—	—	5	pF
I/O, SI/O, QSF	$C_{I/O}$	—	—	7	pF

• AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[1, 16]

Test Conditions

Input Rise and Fall Time	5 ns
Output Load	See figures
Input Timing Reference Levels	0.8V, 2.4V
Output Timing Reference Levels	0.4V, 2.4V



Note: *1. Including scope and jig.

Common Parameter

Parameter	Symbol	HM538123A-8		HM538123A-10		Unit	Note
		Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	150	—	190	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	—	25	—	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	60	25	75	ns	2
$\overline{RAS}$ Hold Time Referenced to $\overline{CAS}$	t_{RSH}	20	—	25	—	ns	
$\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$	t_{CSH}	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	ns	
Transition Time (Rise to Fall)	t_T	3	50	3	50	ns	3
Refresh Period	t_{REF}	—	8	—	8	ms	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	10	—	15	—	ns	
DSF to $\overline{RAS}$ Setup Time	t_{FSR}	0	—	0	—	ns	
DSF to $\overline{RAS}$ Hold Time	t_{RFH}	10	—	15	—	ns	
DSF to $\overline{CAS}$ Setup Time	t_{FSC}	0	—	0	—	ns	
DSF to $\overline{CAS}$ Hold Time	t_{CFH}	15	—	20	—	ns	
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	ns	4
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	ns	4
Output Buffer Turn-off Delay Referenced to $\overline{CAS}$	t_{OFF1}	—	20	—	25	ns	5
Output Buffer Turn-off Delay Referenced to $\overline{OE}$	t_{OFF2}	—	20	—	25	ns	5

Read Cycle (RAM), Page Mode Read Cycle

Parameter	Symbol	HM538123A-8		HM538123A-10		Unit	Note
		Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	25	ns	7, 8
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	25	ns	7
Address Access Time	t_{AA}	—	40	—	45	ns	7, 9
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	ns	10
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	ns	10
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	40	20	55	ns	2
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	ns	
Column Address to $\overline{CAS}$ Lead Time	t_{CAL}	40	—	45	—	ns	
Page Mode Cycle Time	t_{PC}	50	—	55	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	45	—	50	ns	
Page Mode $\overline{RAS}$ Pulse Width	t_{RASP}	80	100000	100	100000	ns	

Write Cycle (RAM), Page Mode Write Cycle, Color Register Set Cycle

Parameter	Symbol	HM538123A-8		HM538123A-10		Unit	Note
		Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	ns	11
Write Command Hold Time	t_{WCH}	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	ns	12
Data-in Hold Time	t_{DH}	15	—	20	—	ns	12
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	10	—	15	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	10	—	15	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	20	—	25	—	ns	
Page Mode Cycle Time	t_{PC}	50	—	55	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
$\overline{CAS}$ to Data-in Delay Time	t_{CDD}	20	—	25	—	ns	13
Page Mode $\overline{RAS}$ Pulse Width	t_{RASP}	80	100000	100	100000	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM538123A-8		HM538123A-10		Unit	Note
		Min	Max	Min	Max		
Read-Modify-Write Cycle Time	t_{RWC}	200	—	250	—	ns	
$\overline{RAS}$ Pulse Width (Read-Modify-Write Cycle)	t_{RWS}	130	10000	160	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	45	—	55	—	ns	14
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	65	—	75	—	ns	14
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	20	—	25	—	ns	12

Read-Modify-Write Cycle (continued)

Parameter	Symbol	HM538123A-8		HM538123A-10		Unit	Note
		Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	ns	6, 7
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	25	ns	7, 8
Access Time from $\overline{OE}$	t_{OAC}	—	20	—	25	ns	7
Address Access Time	t_{AA}	—	40	—	45	ns	7, 9
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	40	20	55	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	ns	12
Data-in Hold Time	t_{DH}	15	—	20	—	ns	12
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM538123A-8		HM538123A-10		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CHR}	15	—	20	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	ns	

Flash Write Cycle, Block Write Cycle

Parameter	Symbol	HM538123A-8		HM538123A-10		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ to Data-in Delay Time	t_{CDD}	20	—	25	—	ns	13
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	20	—	25	—	ns	13

Read Transfer Cycle

Parameter	Symbol	HM538123A-8		HM538123A-10		Unit	Note
		Min	Max	Min	Max		
$\overline{DT}$ Hold Time Referenced to $\overline{RAS}$	t_{RDH}	70	10000	90	10000	ns	
$\overline{DT}$ Hold Time Referenced to $\overline{CAS}$	t_{CDH}	20	—	25	—	ns	
$\overline{DT}$ Hold Time Referenced to Column Address	t_{ADH}	30	—	35	—	ns	
$\overline{DT}$ Precharge Time	t_{DTP}	40	—	45	—	ns	
$\overline{DT}$ to $\overline{RAS}$ Delay Time	t_{DRD}	70	—	90	—	ns	
SC to $\overline{RAS}$ Setup Time	t_{SRS}	30	—	30	—	ns	
1st SC to $\overline{RAS}$ Hold Time	t_{SRH}	85	—	105	—	ns	
1st SC to $\overline{CAS}$ Hold Time	t_{SCH}	30	—	35	—	ns	
1st SC to Column Address Hold Time	t_{SAH}	50	—	55	—	ns	
Last SC to $\overline{DT}$ Delay Time	t_{SDD}	5	—	5	—	ns	
1st SC to $\overline{DT}$ Hold Time	t_{SDH}	15	—	15	—	ns	

Read Transfer Cycle (continued)

Parameter	Symbol	HM538123A-8		HM538123A-10		Unit	Note
		Min	Max	Min	Max		
$\overline{RAS}$ to QSF Delay Time	t_{RQD}	—	95	—	115	ns	15
$\overline{CAS}$ to QSF Delay Time	t_{CQD}	—	35	—	40	ns	15
$\overline{DT}$ to QSF Delay Time	t_{DQD}	—	25	—	30	ns	15
QSF Hold Time Referenced to $\overline{RAS}$	t_{RQH}	20	—	25	—	ns	
QSF Hold Time Referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	ns	
QSF Hold Time Referenced to $\overline{DT}$	t_{DQH}	5	—	5	—	ns	
Serial Data-in to 1st SC Delay Time	t_{SZS}	0	—	0	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	30	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	ns	
SC Precharge Time	t_{SCP}	10	—	10	—	ns	
SC Access Time	t_{SCA}	—	25	—	25	ns	15
Serial Data-out Hold Time	t_{SOH}	5	—	5	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	40	20	55	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	ns	
$\overline{RAS}$ Precharge to $\overline{DT}$ High Hold Time	t_{DTHH}	25	—	30	—	ns	

Pseudo Transfer Cycle, Write Transfer Cycle

Parameter	Symbol	HM538123A-8		HM538123A-10		Unit	Note
		Min	Max	Min	Max		
$\overline{SE}$ Setup Time Referenced to $\overline{RAS}$	t_{ES}	0	—	0	—	ns	
$\overline{SE}$ Hold Time Referenced to $\overline{RAS}$	t_{EH}	10	—	15	—	ns	
SC Setup Time Referenced to $\overline{RAS}$	t_{SRS}	30	—	30	—	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	—	25	—	ns	
Serial Output Buffer Turn-off Time Referenced to $\overline{RAS}$	t_{SRZ}	10	45	10	50	ns	
$\overline{RAS}$ to Serial Data-in Delay Time	t_{SID}	45	—	50	—	ns	
$\overline{RAS}$ to QSF Delay Time	t_{RQD}	—	95	—	115	ns	15
$\overline{CAS}$ to QSF Delay Time	t_{CQD}	—	35	—	40	ns	15
QSF Hold Time Referenced to $\overline{RAS}$	t_{RQH}	20	—	25	—	ns	
QSF Hold Time Referenced to $\overline{CAS}$	t_{CQH}	5	—	5	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	30	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	ns	
SC Precharge Time	t_{SCP}	10	—	10	—	ns	
SC Access Time	t_{SCA}	—	25	—	25	ns	15
$\overline{SE}$ Access Time	t_{SEA}	—	25	—	25	ns	15
Serial Data-out Hold Time	t_{SOH}	5	—	5	—	ns	
Serial Write Enable Setup Time	t_{SWS}	5	—	5	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	ns	

Split Read Transfer Cycle, Split Write Transfer Cycle

Parameter	Symbol	HM538123A-8		HM538123A-10		Unit	Note
		Min	Max	Min	Max		
Split Transfer Setup Time	t_{STS}	20	—	25	—	ns	
Split Transfer Hold Time Referenced to $\overline{RAS}$	t_{RST}	80	—	100	—	ns	
Split Transfer Hold Time Referenced to $\overline{CAS}$	t_{CST}	20	—	25	—	ns	
Split Transfer Hold Time Referenced to Column Address	t_{AST}	40	—	45	—	ns	
SC to QSF Delay Time	t_{SQD}	—	25	—	30	ns	15
QSF Hold Time Referenced to SC	t_{SQH}	5	—	5	—	ns	
Serial Clock Cycle Time	t_{SCC}	30	—	30	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	ns	
SC Precharge Time	t_{SCP}	10	—	10	—	ns	
SC Access Time	t_{SCA}	—	25	—	25	ns	15
Serial Data-out Hold Time	t_{SOH}	5	—	5	—	ns	
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	40	20	55	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	ns	

Serial Read Cycle, Serial Write Cycle

Parameter	Symbol	HM538123A-8		HM538123A-10		Unit	Note
		Min	Max	Min	Max		
Serial Clock Cycle Time	t_{SCC}	30	—	30	—	ns	
SC Pulse Width	t_{SC}	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	ns	
Access Time from SC	t_{SCA}	—	25	—	25	ns	15
Access Time from $\overline{SE}$	t_{SEA}	—	25	—	25	ns	15
Serial Data-out Hold Time	t_{SOH}	5	—	5	—	ns	
Serial Output Buffer Turn-off Time Referenced to $\overline{SE}$	t_{SEZ}	—	20	—	25	ns	5
Serial Data-in Setup Time	t_{SIS}	0	—	0	—	ns	
Serial Data-in Hold time	t_{SIH}	15	—	20	—	ns	
Serial Write Enable Setup Time	t_{SWS}	5	—	5	—	ns	
Serial Write Enable Hold Time	t_{SWH}	15	—	20	—	ns	
Serial Write Disable Setup Time	t_{SWIS}	5	—	5	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	15	—	20	—	ns	

Logic Operation Mode

Parameter	Symbol	HM538123A-8		HM538123A-10		Unit	Note
		Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$)	t_{CHR}	15	—	20	—	ns	

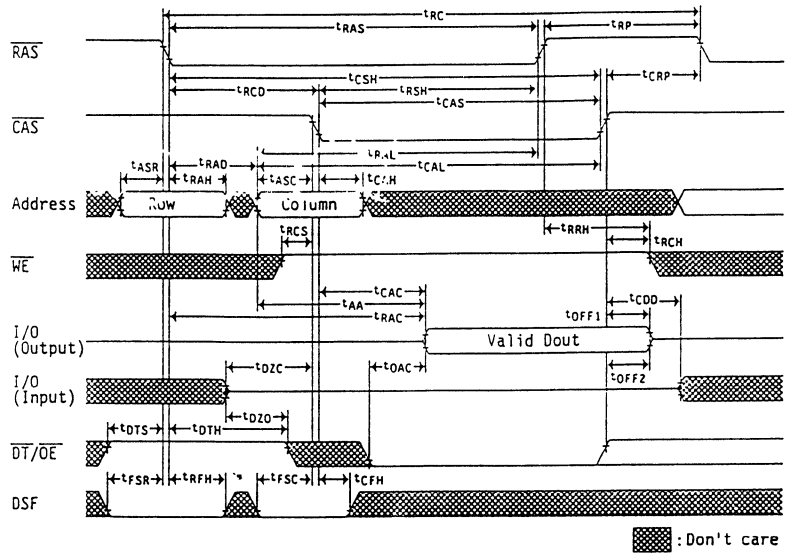
Logic Operation Mode (continued)

Parameter	Symbol	HM538123A-8		HM538123A-10		Unit	Note
		Min	Max	Min	Max		
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	ns	
Write Cycle Time	t_{FRC}	170	—	215	—	ns	
$\overline{RAS}$ Pulse Width	t_{FRS}	100	10000	125	10000	ns	
Page Mode Cycle Time	t_{FPC}	70	—	80	—	ns	
$\overline{CAS}$ Pulse Width	t_{FCS}	40	—	50	—	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{CAS}$	t_{FRSH}	40	—	50	—	ns	
$\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$	t_{FCSH}	100	—	125	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{FRA}	60	—	70	—	ns	
Column Address to $\overline{CAS}$ Lead Time	t_{FCA}	60	—	70	—	ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	40	20	55	ns	
Write Command Setup Time	t_{WCS}	0	—	0	—	ns	
Write Command Hold Time	t_{WCH}	15	—	20	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	25	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	ns	12
Data-in Hold Time	t_{DH}	15	—	20	—	ns	12
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	10	—	15	—	ns	
Mask Data to $\overline{RAS}$ Setup Time	t_{MS}	0	—	0	—	ns	
Mask Data to $\overline{RAS}$ Hold Time	t_{MH}	10	—	15	—	ns	
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{DEH}	20	—	25	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	

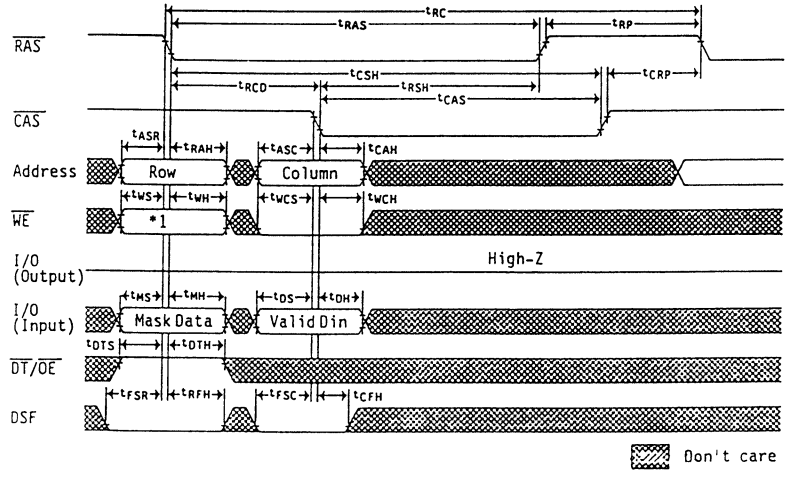
Notes:
1. AC measurements assume $t_T = 5$ ns.
2. When $t_{RCD} > t_{RCD}$ (max) or $t_{RAD} > t_{RAD}$ (max), access time is specified by t_{CAC} or t_{AA}.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition time t_T is measured between V_{IH} and V_{IL}.
4. Data input must be floating before output buffer is turned on. In read cycle, read-modify-write cycle and delayed write cycle, either t_{DZC} (min) or t_{DZO} (min) must be satisfied.
5. t_{OFF1} (max), t_{OFF2} (max) and t_{SEZ} (max) are defined as the time at which the output achieves the open circuit condition ($V_{OH} - 200$ mV, $V_{OL} + 200$ mV).
6. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
7. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
8. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
9. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
10. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.
11. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
12. These parameters are specified by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
13. Either t_{CDD} (min) or t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{CAS}$ or $\overline{OE}$ prior to applying data to the device when output buffer is on.
14. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min) in read-modify-write cycle, the data of the selected address outputs to an I/O pin and input data is written into the selected address. t_{ODD} (min) must be satisfied because output buffer must be turned off by $\overline{OE}$ prior to applying data to the device.
15. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
16. After power-up, pause for 100 μs or more and execute at least 8 initialization cycles (normal memory cycle or refresh cycle), then start operation.

■ TIMING WAVEFORMS

• Read Cycle

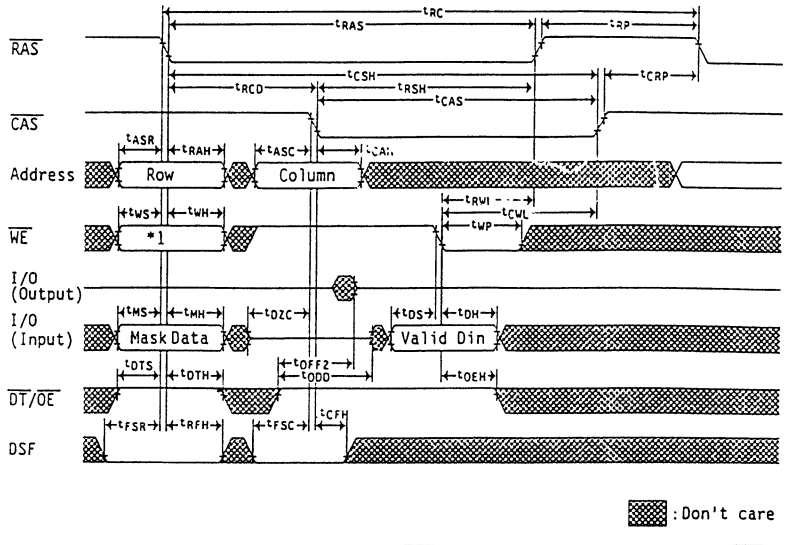


• Early Write Cycle



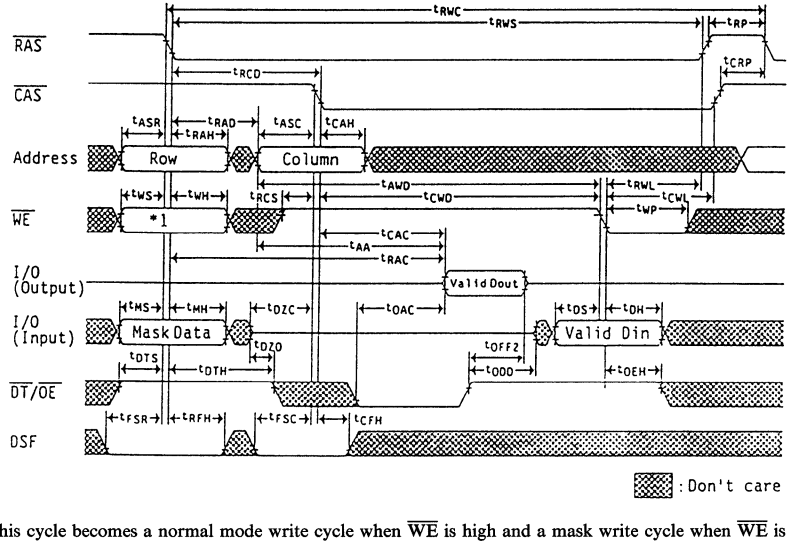
Note: *1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

• **Delayed Write Cycle**



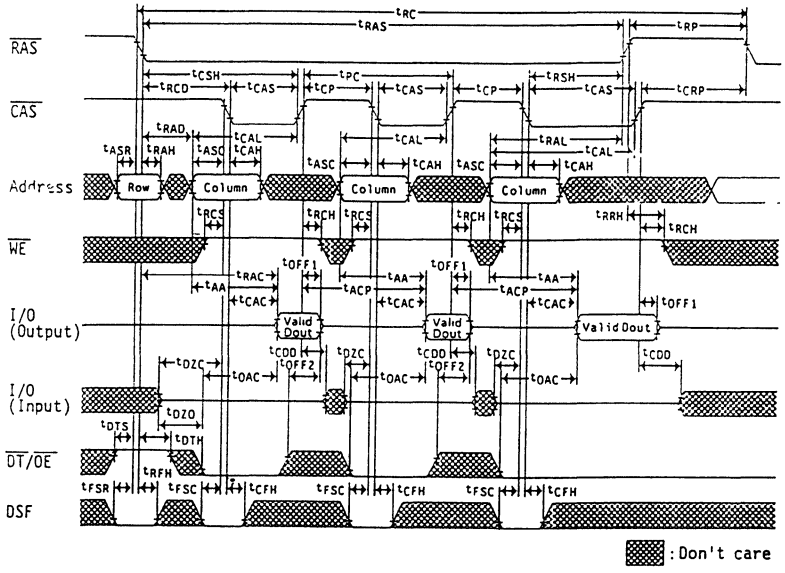
Note: *1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

• **Read-Modify-Write Cycle**

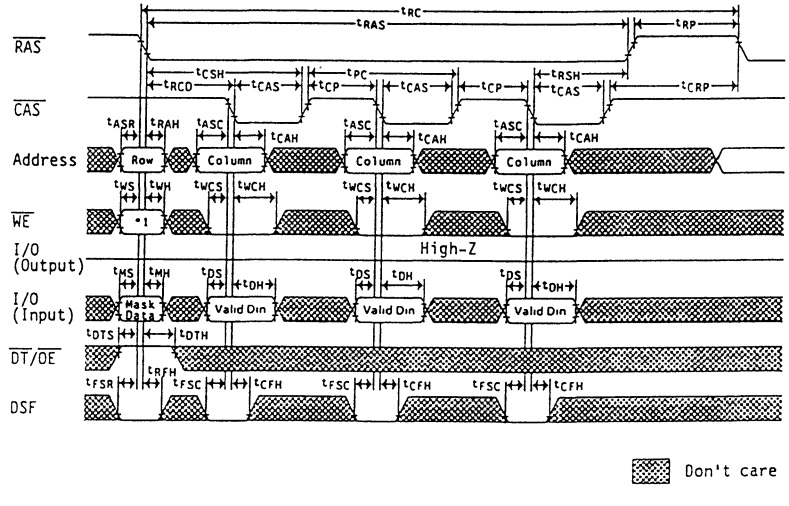


Note: *1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

• **Page Mode Read Cycle**

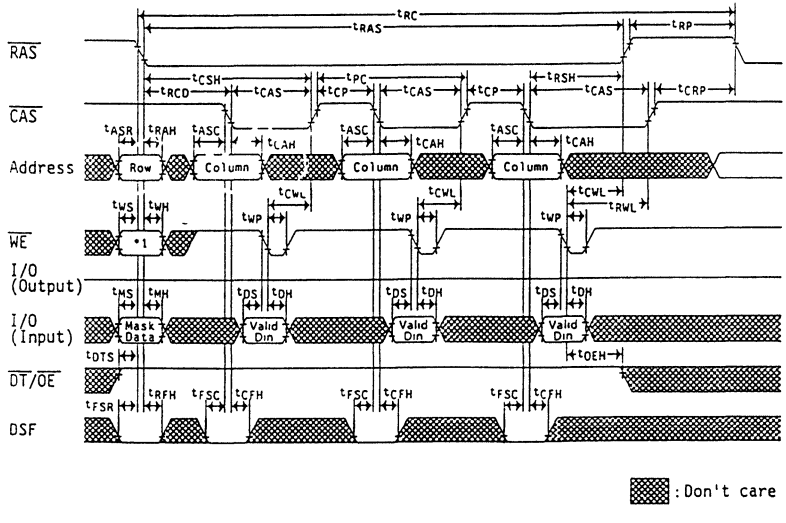


• **Page Mode Write Cycle (Early Write)**



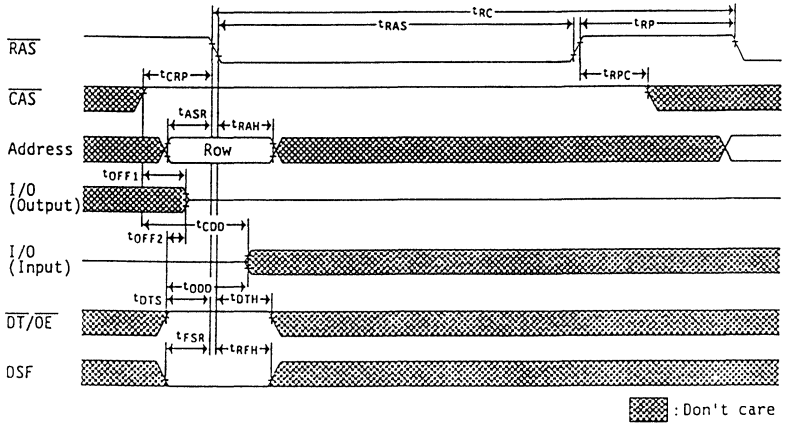
Note: *1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

• **Page Mode Write Cycle (Delayed Write)**

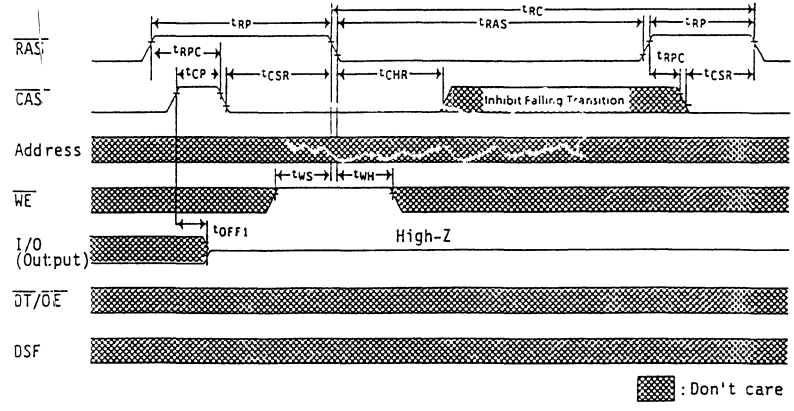


Note: *1. This cycle becomes a normal mode write cycle when $\overline{WE}$ is high and a mask write cycle when $\overline{WE}$ is low.

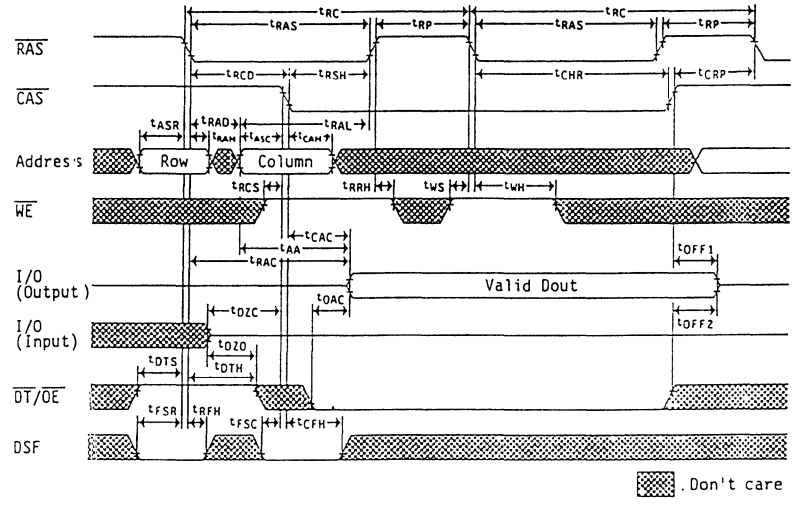
• **$\overline{RAS}$ Only Refresh Cycle**



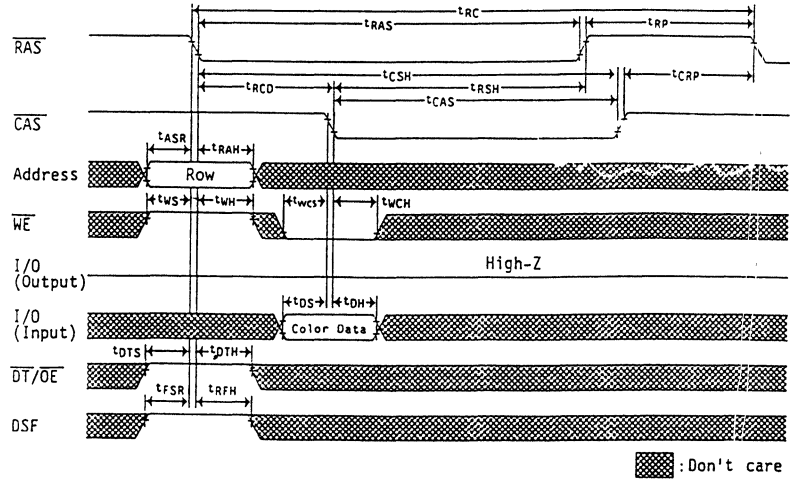
• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



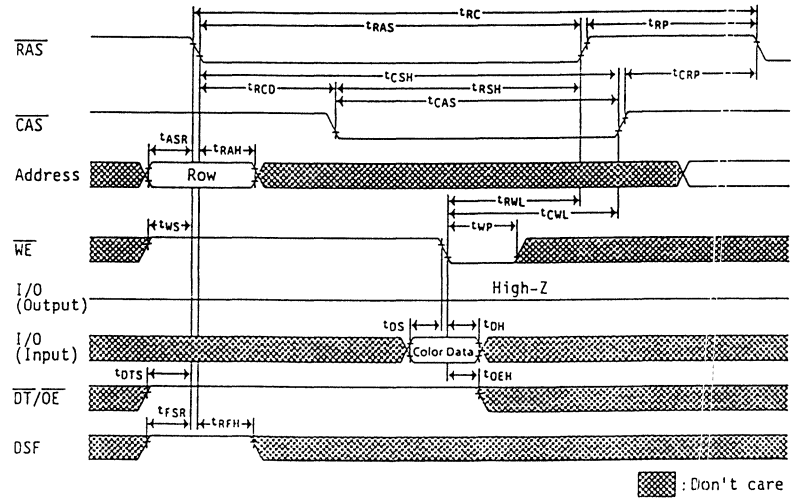
• Hidden Refresh Cycle



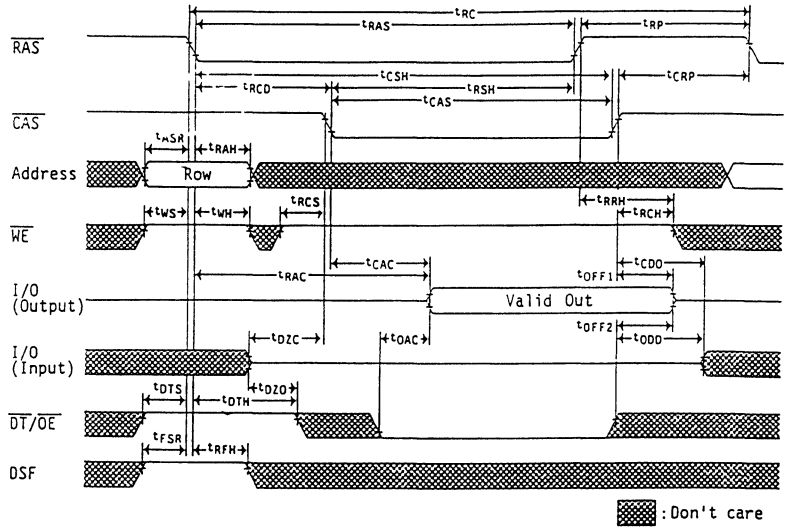
• **Color Register Set Cycle (Early Write)**



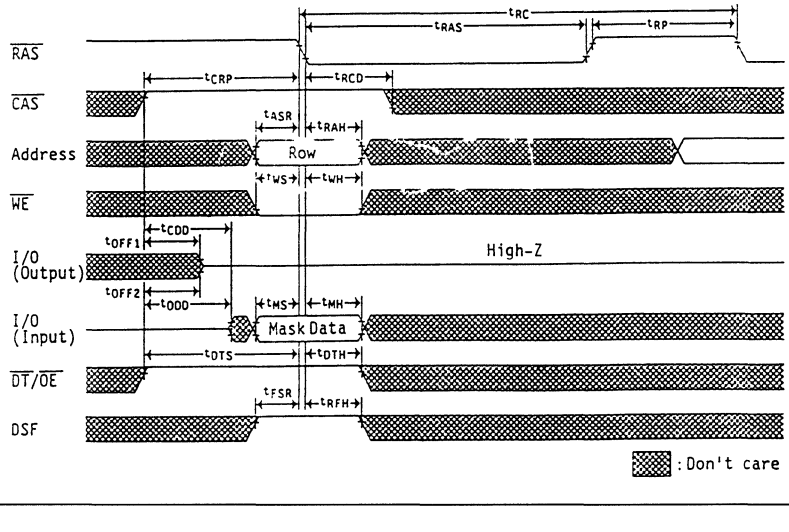
• **Color Register Set Cycle (Delayed Write)**



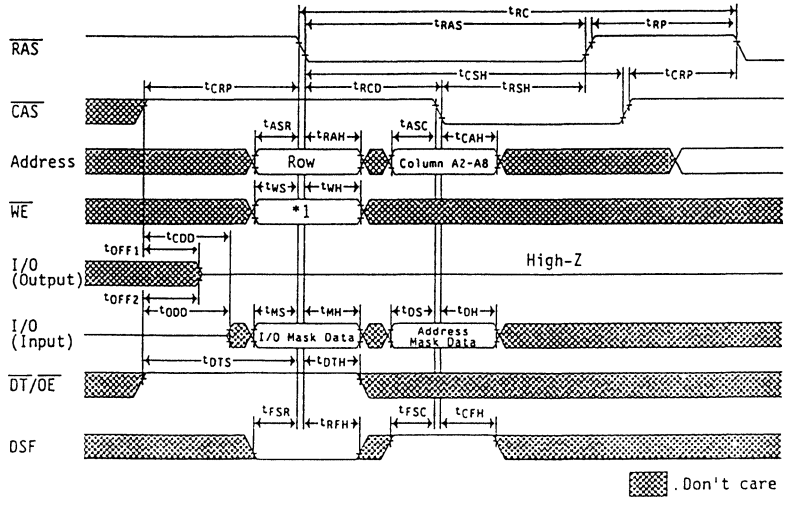
• **Color Register Read Cycle**



• **Flash Write Cycle**

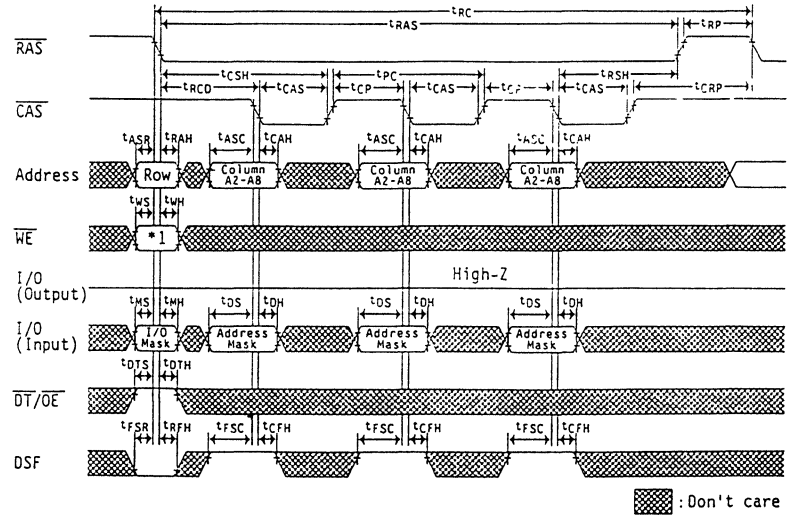


• **Block Write Cycle**



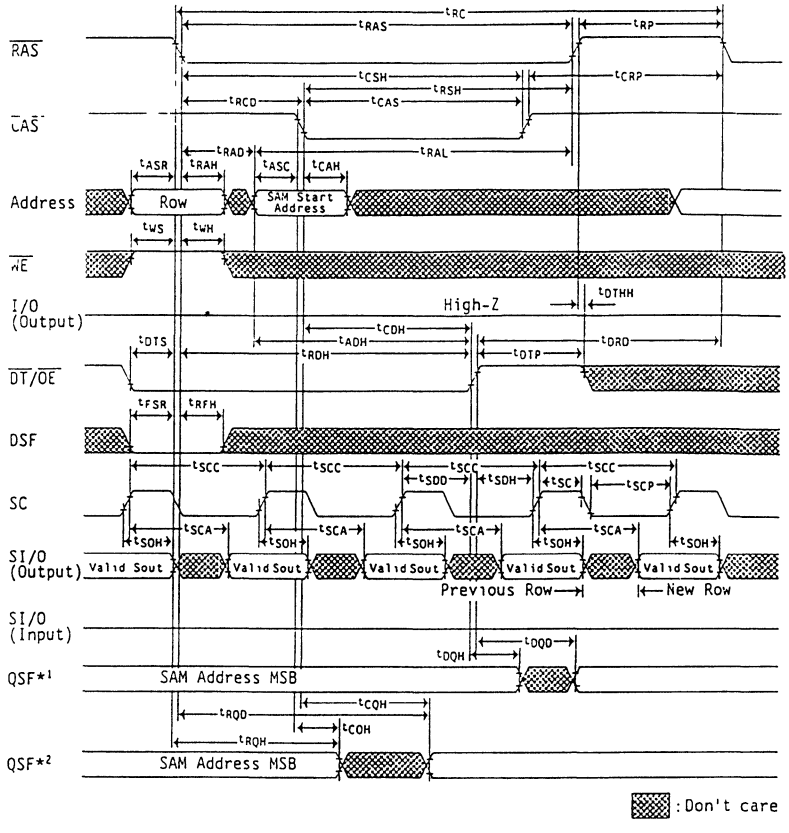
Note: *1. This cycle becomes a normal block write cycle when $\overline{WE}$ is high and a mask block write cycle when $\overline{WE}$ is low.

• **Page Mode Block Write Cycle**



Note: *1. This cycle becomes a normal block write cycle when $\overline{WE}$ is high and a mask block write cycle when $\overline{WE}$ is low.

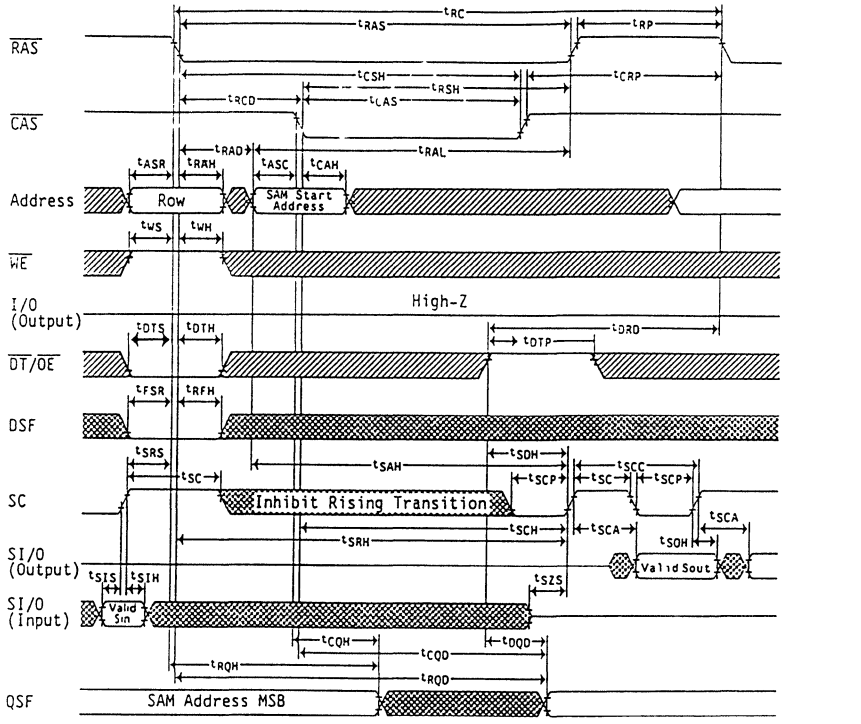
• Read Transfer Cycle (1)



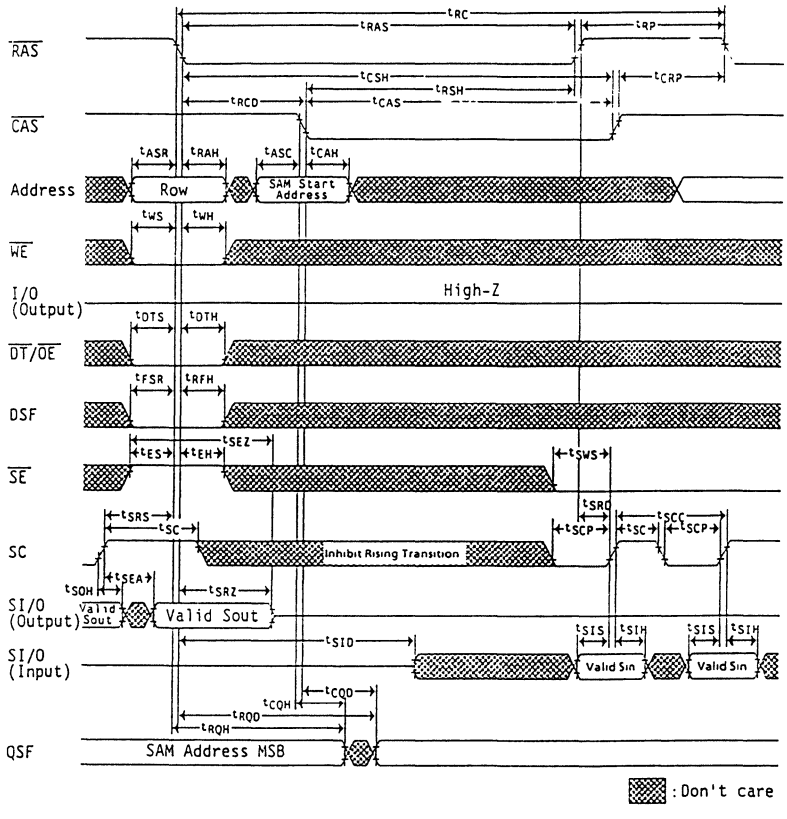
Notes: *1. This QSF timing is referred when SC is risen once or more between the previous transfer cycle and $\overline{CAS}$ falling edge of this cycle (QSF is switched by $\overline{DT}$ rising).

*2. This QSF timing is referred when SC isn't risen between the previous transfer cycle and $\overline{CAS}$ falling edge of this cycle (QSF is switched by $\overline{RAS}$ or $\overline{CAS}$ falling).

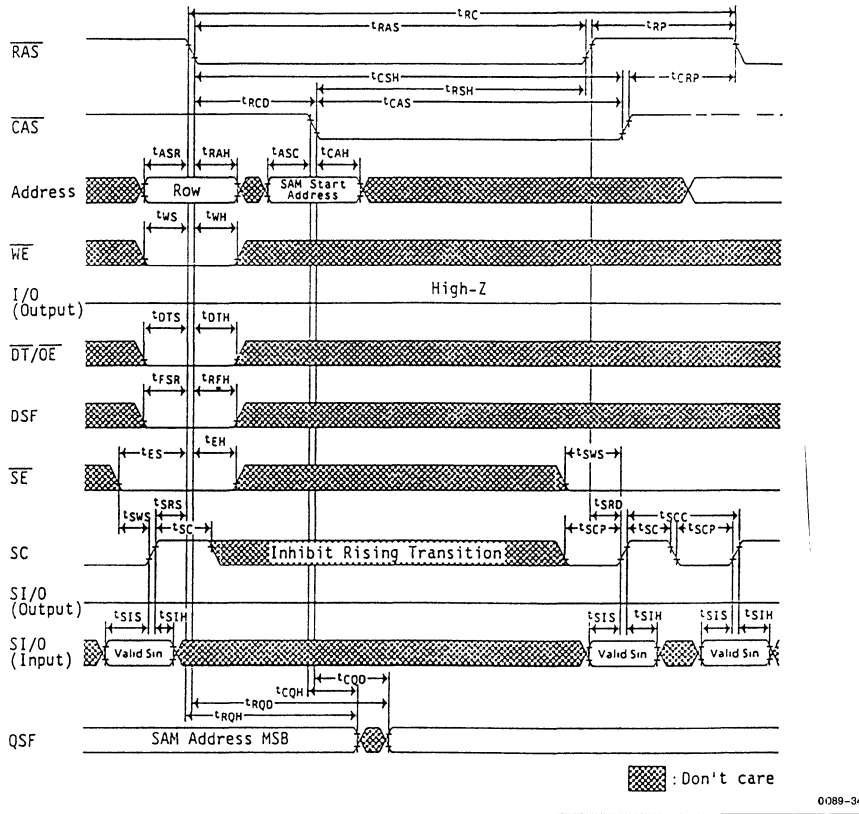
• **Read Transfer Cycle (2)**



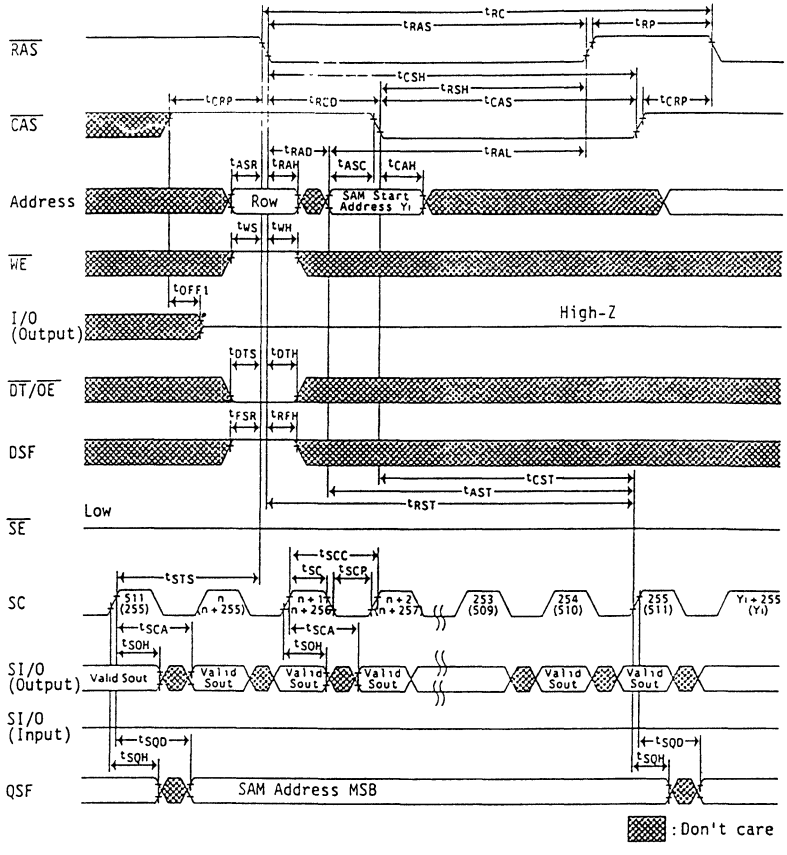
• **Pseudo Transfer Cycle**



• Write Transfer Cycle

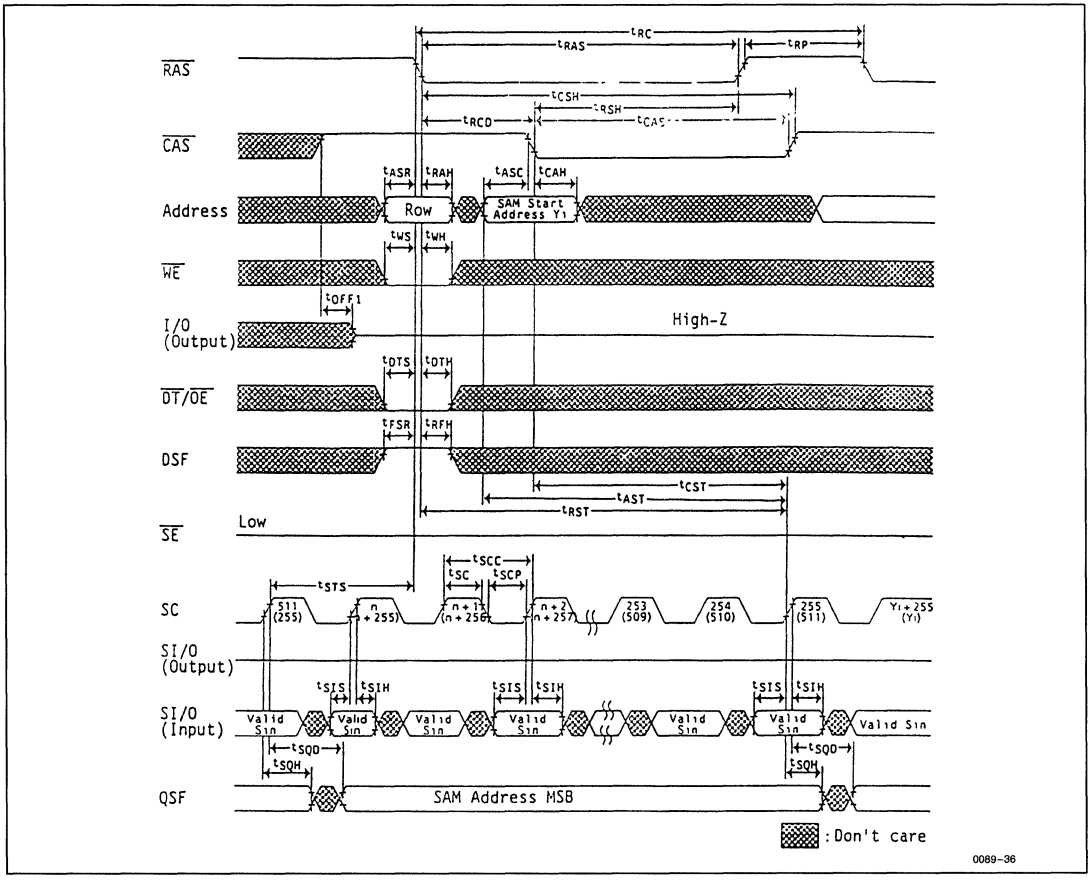


• **Split Read Transfer Cycle**

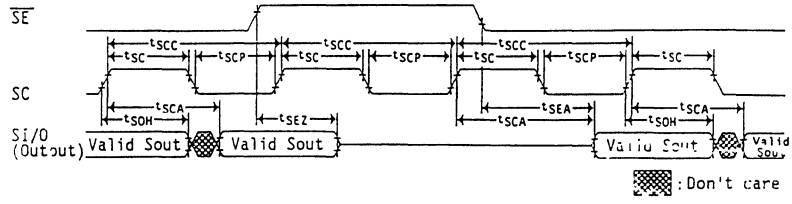


Note: *1. If the next transfer cycle after read transfer cycle is split read transfer cycle, one or more access to SC are required between read transfer cycle and split read transfer cycle.

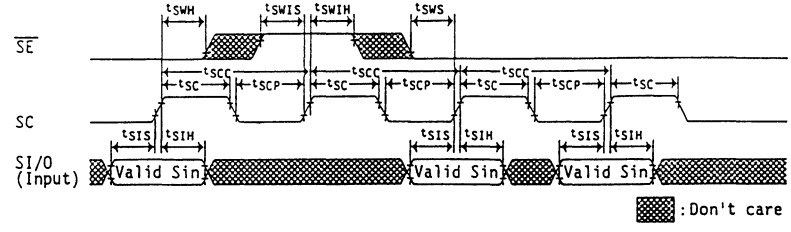
• **Split Write Transfer Cycle**



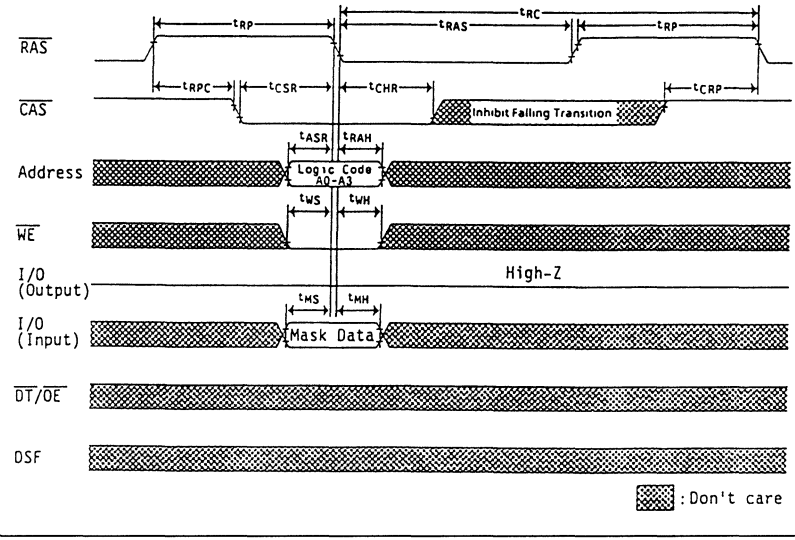
• **Serial Read Cycle**



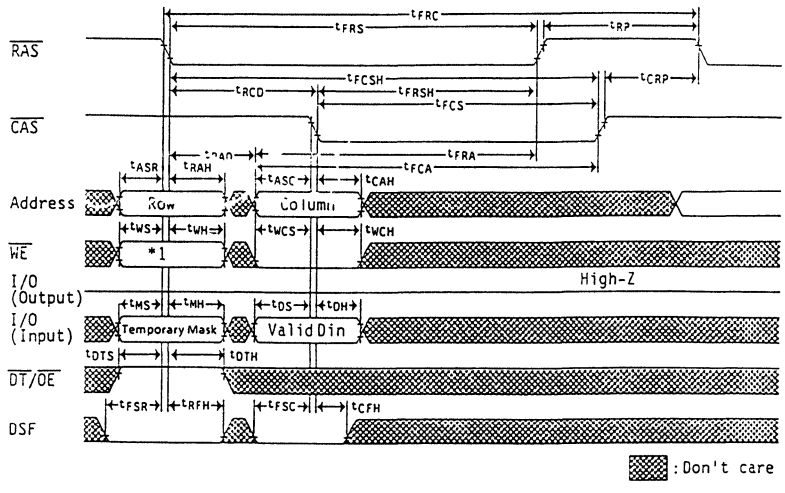
• **Serial Write Cycle**



• **Logic Operation Set/Reset Cycle**

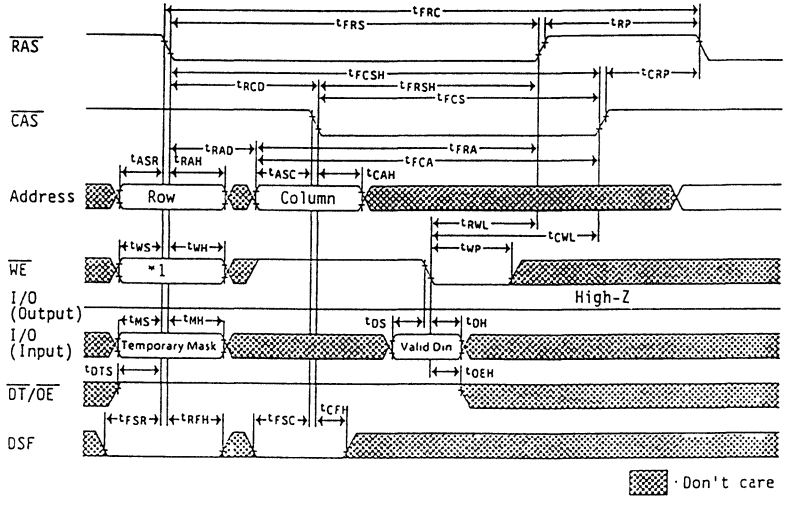


• Logic Operation Mode Early Write Cycle



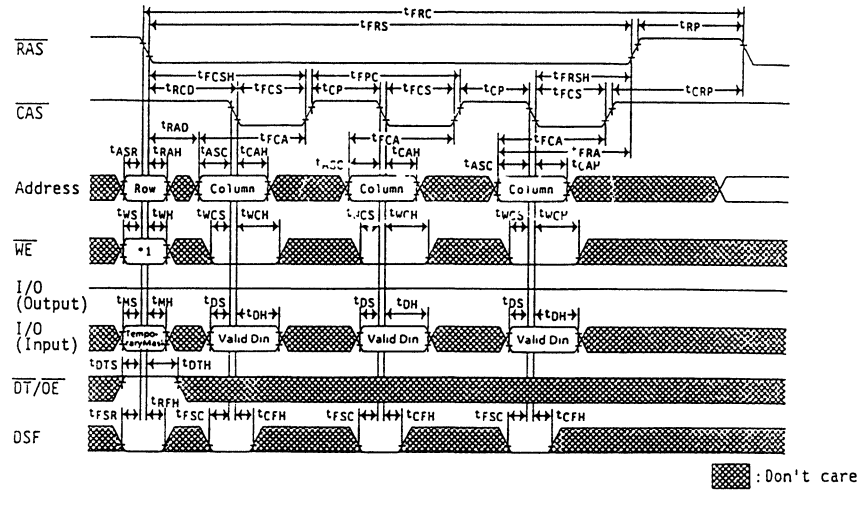
Note: *1. When $\overline{WE}$ is high, this cycle enters a logic operation mode. When $\overline{WE}$ is low, logic operation mode is reset, and a temporary mask write cycle starts.

• Logic Operation Mode Delayed Write Cycle



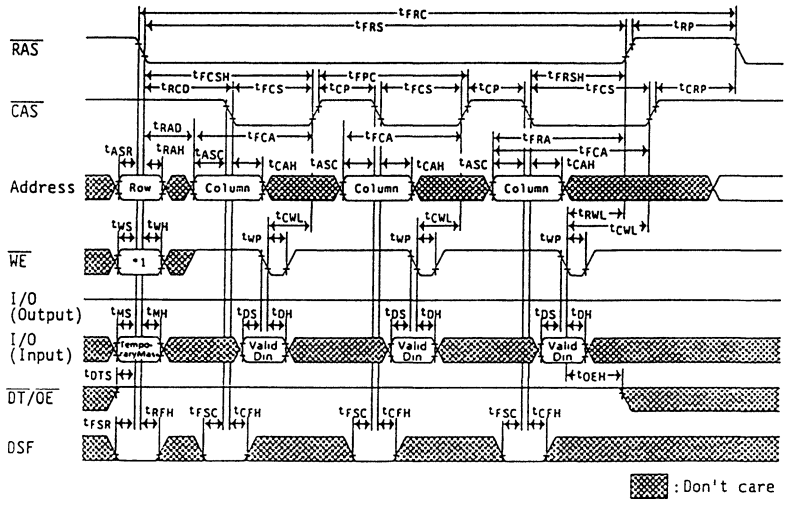
Note: *1. When $\overline{WE}$ is high, this cycle enters a logic operation mode. When $\overline{WE}$ is low, logic operation mode is reset, and a temporary mask write cycle starts.

• **Logic Operation Mode Page Mode Write Cycle (Early Write)**



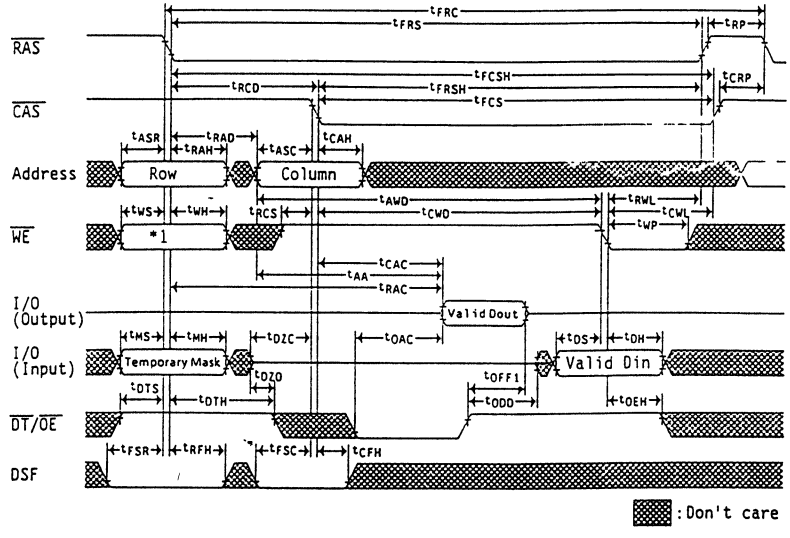
Note: *1. When $\overline{WE}$ is high, this cycle enters a logic operation mode. When $\overline{WE}$ is low, logic operation mode is reset, and a temporary mask write cycle starts.

• **Logic Operation Mode Page Mode Write Cycle (Delayed Write)**



Note: *1. When $\overline{WE}$ is high, this cycle enters a logic operation mode. When $\overline{WE}$ is low, logic operation mode is reset, and a temporary mask write cycle starts.

• **Logic Operation Mode Read-Modify-Write Cycle**



Note: *1. When $\overline{WE}$ is high, this cycle enters a logic operation mode. When $\overline{WE}$ is low, logic operation mode is reset, and a temporary mask write cycle starts.

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