IBM Customer Engineering

Instruction-Reference

1410 System Fundamentals

Contents

IBM

Instruction–Reference

1410 System Fundamentals

Preface

This publication, Form 223-2589, obsoletes and contains information formerly found in the following Customer Engineering Instruction-Reference manuals: *IBM 1410 System Fundamentals and 1411 Functional Units,* Form R23-2589; *IBM 1410 Component Circuits,* Form R23-9776; *IBM 1410 Timing Charts and Second Level Diagrams,* Form R23-9774-1; and *IBM 1410 Data Processing System,* Form 225-6549-1.

The information formerly contained in the 1410 System Fundamentals and 1410 Component Circuits manual remains unchanged, but the 1410 Timing Chart and Second Level Diagrams manual has been revised. The revised portion eliminates many diagrams that can now be found in their related manuals. For example, diagrams for Input-Output or Console Operations can be found in *IBM 1410 Input-Output Operations,* Form R23-2692, or in *IBM 1415 Console,* Form R23-2648.

Copies of this and other IBM publications can be obtained through IBM Branch Offices.
Address comments concerning the contents of this publication to:
IBM Corporation, CE Manuals, Dept. B96, PO Box 390, Poughkeepsie, N.Y.

Illustration List

The IBM 1410 Data Processing System is an intermediate-range computer that has a variety of storage capacities, optional features, and input-output devices designed to meet customer needs. To process data, the 1410:

1. Receives data and instructions from an input device: card reader, paper tape reader, etc.
2. Stores the data and instructions until they are needed.
3. Adds, compares, edits, or performs other data operations.
4. Delivers the results of these operations to an output device: card punch, printer, etc.

The 1410 is made up of five functional units: input, storage, control, operational, and output. These units, controlled by instructions, process data.

Operation of Functional Units

The five functional units of the 1410 operate as follows (Figure 1):

1. An *input device*, such as a card reader, feeds data and instructions into the computer. Data consists of alphameric information on which specific operations are performed by the computer. Instructions consist of characters that determine the operations according to a particular code utilized by the 1410. The character A, used as the first character of an instruction, signifies an add operation.

2. The *storage unit* receives both the data and the instructions and retains them for use as they are needed. Each unit of information is stored in a numbered location, called an address, in storage. The 1410 uses a five-character-position address, i.e., 04322, 06744, etc. If the contents of a specific area in storage are needed for an operation, these contents are read out and sent to the appropriate unit.

3. The *control unit* receives the instructions, one character at a time, from storage. The control unit interprets each instruction to determine appropriate action. When interpreting the A (add) instruction, for example, the control unit requests the storage unit to read out the data to be added together and sends it to the operational unit. The address of the data to be added is in another part of the instruction.

4. The *operational unit* contains all units necessary to add, compare, edit or move data. This unit performs these operations, which are specified by the instruction,

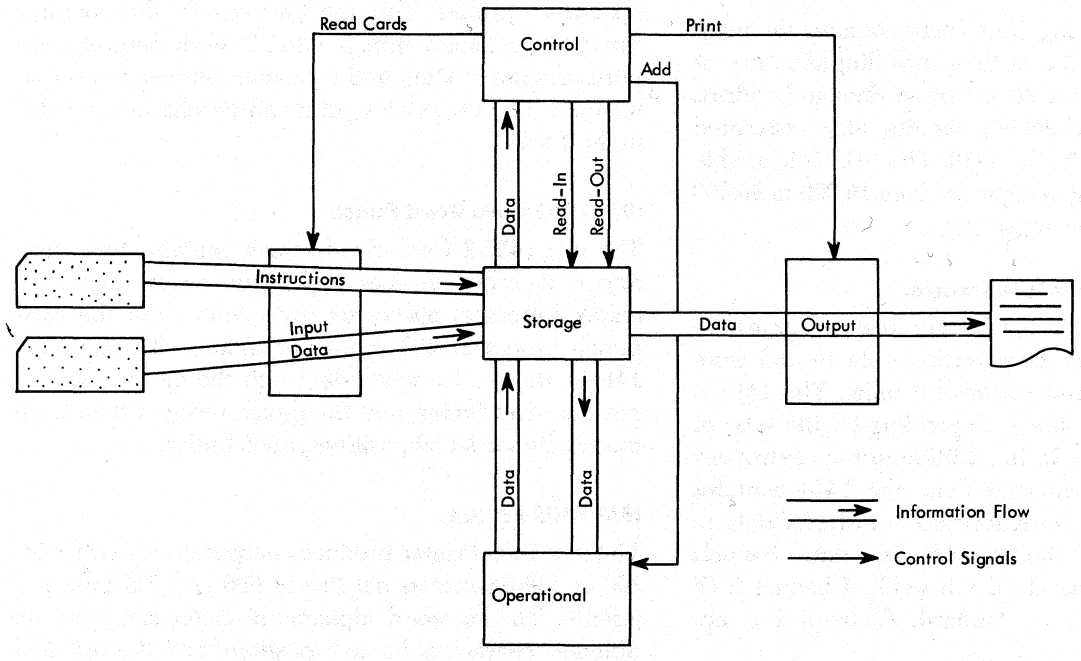


Figure 1. Operation of Functional Units

under command of the control unit. The results are returned to storage.

5. Obeying a subsequent instruction, the control unit requests the storage unit to read out the results of a particular operation. These results are then sent to an *output device*, such as a printer or a card punch.

Operating Fundamentals of a Computer System

With the add operation as an example, note these important fundamentals of computer operation:

1. A single instruction causes the computer to execute only one operation, i.e., add, compare, edit, or print. To perform a payroll operation, for example, the computer must be given many instructions. A group of sequential instructions with the objective of performing a particular job is called a program.

2. All five functional units are interdependent. The control unit cannot function without the storage unit as a source of instructions. The adder, which is part of the operational unit, depends on storage as a source of data. The units of a computer thus work together as parts of a complete system that processes data.

3. All information entering or leaving the computer must pass through storage. Input data cannot go directly from the input unit to the adder; results cannot go directly from the adder to the output unit.

1410 Components

IBM 1411 Processing Unit

The IBM 1411 Processing Unit (CPU) contains the magnetic core storage unit and the controlling circuitry of the IBM 1410 system, as well as various data and address registers, logic and checking circuits, etc., associated with the flow of data in the 1410. The 1411 is available in five models ranging in capacity from 10,000 to 80,000 positions of magnetic-core storage.

IBM 1414 Input-Output Synchronizer

The IBM 1414 Input-Output Synchronizer contains the circuitry necessary for transmitting data to and from the processing unit and various I-O units. The 1414 is available in several models, depending on the type of I-O units used (Figure 2). In addition to the control circuitry necessary to transmit data, the 1414 contains checking circuits to insure accurate transfer of data to and from the CPU and the I-O units. Two data channels are available: Channel 1 (E Channel), Channel 2 (F Channel). (Channel 1 is standard; Channel 2 is optional.)

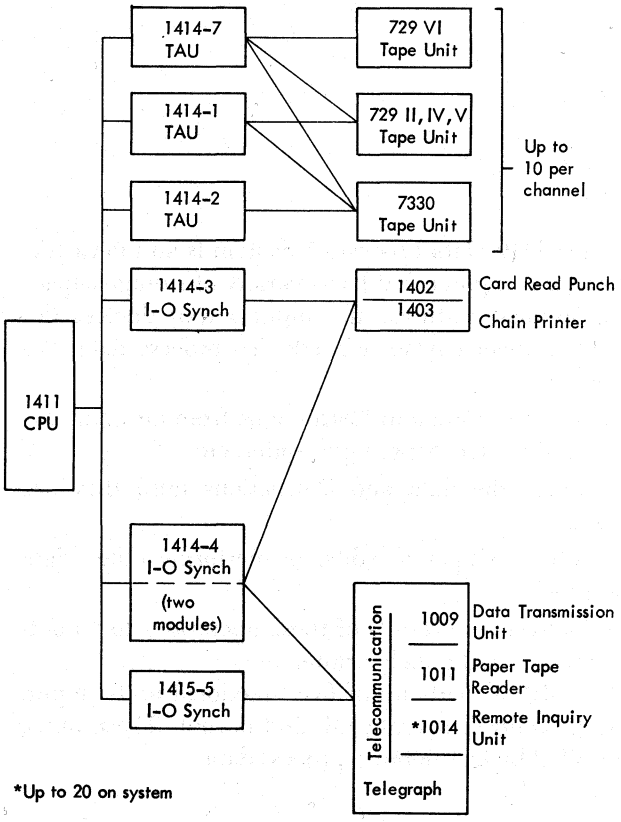


Figure 2. Synchronizer Models Required for Each I-O Device

IBM 1415 Console and Input-Output Printer

The IBM 1415 Console provides operator communication with the 1410 System. The console consists of a control section containing the keys and switches that control the 1410 System, an indicator panel, and the system I-O printer. Through the console, the operator can enter or display storage data. Console controls simplify program testing and customer engineering maintenance. The I-O printer prints all 64 characters valid in the 1410.

IBM 1402 Card Read Punch

The IBM 1402-2 Card Read Punch contains two separate unit-record devices under one cover. The card reader processes 800 cards per minute, and the card punch processes 250 cards per minute. Through the 1414-3, the reader sends data into the CPU via an 80-position read buffer, and the punch receives data from the system via an 80-position punch buffer.

IBM 1403 Printer

The IBM 1403 Printer produces output documents with 100 or 132 characters per line at 600 or 1,285 lines per minute. The standard alphameric chain can print 48 different characters in each position, and the optional

numeric chain feature can print 16 characters in each position. With this feature installed, the 1403 printing speed increases to 1,285 lines per minute.

A dual-speed carriage controlled by a closed loop of paper tape permits skipping at 33 inches per second (low speed) or at 75 inches per second (high speed), depending on the length of the skip.

IBM 729 and IBM 7330 Magnetic Tape Units

Four models (II, IV, V, or VI) of the IBM 729 Magnetic Tape Unit or the IBM 7330 Tape Unit can be attached to the 1410 System. The 729 Tape Units are used when the goal is high volume and high speed. The 7330 Tape Units are used where volume and speed justify a lower cost tape system. All units have dual recording densities (characters per inch), enabling transfers of tape reels from one IBM system to another.

IBM 1405 Disk Storage

The IBM 1405 Disk Storage can retain 20 million characters of information, maximum. Data are stored in the form of magnetized spots on the surface of the circular disks that are coated with a magnetic oxide material. Storage disks are mounted on a vertical shaft that turns at a speed of 1,200 revolutions per minute. Data can be recorded on both sides of each disk.

Read-write heads, mounted on movable access arms, read and write on the disk faces. The arms seek specified records in the disk-storage unit by moving up or down and in or out to the desired record. Maximum character rate is approximately 25,000 characters per second.

IBM 1301 Disk Storage

The IBM Disk Storage can retain as many as 56 million characters of information on circular disks similar to those of the 1405. In the 1301, however, each surface has its own read-write head. This reduces maximum access time to 180 milliseconds. Disk rotation of 1,800 rpm results in a maximum character rate of 90,000 characters per second.

IBM 1412 and IBM 1419 Magnetic Character Readers

Attaching an IBM 1412 or IBM 1419 Magnetic Character Reader to a 1410 System provides banks with a time-saving method of reading and processing large numbers of daily transactions. These machines handle card or paper documents (or both intermixed) inscribed with the E13B type font designated by the American Bankers Association.

Documents can be read into the 1410 System at a maximum rate of 950 per minute with the 1412, or 1,600 per minute with the 1419. While the data entering the 1410 via the magnetic character reader are being processed, the actual documents are stacked in pockets selected by the stored program.

Two 1412 readers or two 1419 readers can be attached to a 1410 System. Each magnetic character reader, however, must be connected to a different data channel. A single magnetic character reader can be attached to either channel 1 or channel 2.

IBM 7750 Programmed Transmission Control

The IBM 7750 Programmed Transmission Control serves as a buffer and telecommunications message control unit that links the 1410 System with a variety of remote transmitting and receiving terminal devices. The 7750 stored program assembles messages, distributes messages under priority to and from the network, converts codes, edits, checks messages for validity, etc., while directing data at high character rates to and from the host 1410.

One 7750 can be assigned to a system, provided the system has a 1411 Processing Unit having an A-suffixed model number, a control adapter, and the priority and processing overlap features.

IBM 1009 Data Transmission Unit

The IBM 1009 Data Transmission Unit is the intermedium for high-speed two-way communication between the 1410 System and another 1009 (or a 1009 simulated by a 7750 Programmed Transmission Control) attached to any 1400- or 7000-series data processing system. Data are transmitted or received over message-service or leased-wire circuits at fixed character rates ranging from 75 to 300 per second.

The 1414-4 or 1414-5 I-O Synchronizer allows the 1410 System to continue processing during a 1009 operation. Data are transferred to or from the processing unit via two 80-position buffers.

IBM 1011 Paper Tape Reader

One IBM 1011 Paper Tape Reader can be attached to a 1410 System providing for data sources stored on paper tape. Data can be read at up to 500 characters per second. The paper tape can be in the widths commonly used for five-, six-, seven-, or eight-track tape, in strips, reels, or rolls that feed from the center, and can be chad or chadless.

The 1414-4 or 1414-5 I-O Synchronizer allows the system to continue processing during a paper tape reading operation. Data are read into the processing unit via an 80-position buffer.

IBM 1014 Remote Inquiry Unit

A 1410 System containing one or more IBM 1014 Re-

mote Inquiry Units can reply to remote or local requests for information. Each 1014, whether installed locally or remotely, receives and prints almost instantaneous replies from the 1410 and prints both the inquiry and the reply at character rates up to 12½ per second for the inquiry and 15½ per second for the reply. A modified 1-0 printer is used.

An adapter, in a 1414-4 or 1414-5 1-0 Synchronizer, controls and sequences the acceptance by the 1410 of request messages from as many as ten 1014 remote inquiry units. Either one or two adapters can be installed in the 1414 to handle up to ten remote inquiry units each. With two adapters, two 1014 remote inquiry units controlled by separate adapters can transmit or receive at the same time.

The 1414 also allows the system to continue processing during a 1014 operation. Inquiries and replies are transferred to and from the processing unit via two 80-position buffers, one for input and one for output, in each adapter.

Program Addressable Clock

The program addressable clock, which can be installed in the 1415 Console, provides a method of logging system time. Clock time can be obtained by the program for recording any start or stop point or other event. Time is indicated in 24-hour (continental) style, and each hour is graduated in hundredths.

Among the many uses or aids provided by the program addressable clock are:

1. Better scheduling of system time through time studies of previous jobs.
2. Determining exact processing time, system setup time, program testing time, maintenance time, and idle time.
3. Distributing more accurate job charges to users of the system.
4. Logging the time of the telecommunication messages.

Telegraph Input-Output

Installation of the telegraph input-output feature in a 1414-4 or 1414-5 permits connection of a telegraph network to the 1410 System. Data can thus be accepted directly by the 1410 from any station in the network or transmitted directly from the 1410, through local telegraph terminals, to any or all of the stations.

The 1414 1-0 Synchronizer allows the system to continue processing during a transfer to or from the telegraph network. The feature consists of one input adapter and one output adapter in the 1414. One or two more adapters can be added; these additional adapters can consist of one input or output adapter (or both), or two input or two output adapters. Data are transferred to and from the telegraph via 80-position buffers, one for each input or output adapter.

1410 Fundamentals

Machine Language

Normally, individual units of a coding system are referred to as bits of information or "bits." All components in a computer are always in one of two possible states: a line is active or inactive, a latch is on or off, a trigger is set or reset, a magnetic core is magnetized in one direction or the other. Components that operate in this manner—on or off, set or reset—are called binary. When a latch is on, it represents the presence of a bit; when it is off, it represents the absence of a bit. The three coding systems used by the 1410 use this principle. Various bit combinations represent all alphameric characters valid to the system.

BINARY CODED DECIMAL

In the binary coded decimal (BCD) system, the numeric values are expressed in combinations of four bits (Figure 3). Each of these bits is assigned a value of 1, 2, 4, or 8. Combinations of these bits make up any of the 10 digits. A 5 would be represented by a 1 bit and a 4 bit; a 7 would be represented by a 1, 2, and 4 bit. Two additional bit positions, B and A, handle the zone information of alphabetic and special characters. The combination of B and A bit represents the 12-zone portion of a character. The B bit only represents the 11 zone; the A bit only represents the 0 zone.

1410 System reliability is improved by checking each character to insure that an odd number of bits is present. Because many bit combinations do not naturally contain an odd number of bits, a seventh bit position is made available in which a check or C bit can be stored when necessary to make the total bit count odd. The proper number of bits for any given character is the *parity* of that character. The checking of bit count per character is *parity checking*.

TWO-OUT-OF-FIVE CODE

The two-out-of-five code (2/5) as used by the 1410 is strictly a numeric code (Figure 4). Numeric values are expressed in combinations of two out of the five bits (0, 1, 2, 4, and 8) used to make up this code. Therefore, a 5 is a bit 4 and bit 1 combination; a 7 is a bit 8 and bit 4 combination. An important advantage of the 2/5 code is convenient error checking. Because every digit is expressed by only two bits, any digit position with more or fewer than two bits is in error and a validity check light is turned on to indicate an invalid bit combination.

1 Collating Number	2 Graphics	3 Card Code			4 BCD Code						5
					B	A	8	4	2	1	
00	Blank	No Punches			No Bits						
01	.	12	3	8	B	A	8		2	1	
02	¤)	12	4	8	B	A	8	4			
03	[	12	5	8	B	A	8	4		1	
04	<	12	6	8	B	A	8	4	2		
05	‡	12	7	8	B	A	8	4	2	1	GM
06	& +	12			B	A					
07	$	11	3	8	B		8		2	1	
08	*	11	4	8	B		8	4			
09	]	11	5	8	B		8	4		1	
10	;	11	6	8	B		8	4	2		
11	Δ	11	7	8	B		8	4	2	1	MC
12	-	11			B						
13	/	0	1			A				1	
14	,	0	3	8		A	8		2	1	
15	% (	0	4	8		A	8	4			
16	Y	0	5	8		A	8	4		1	WS
17	\	0	6	8		A	8	4	2		
18	##	0	7	8		A	8	4	2	1	SM
19	↑		2	8		A					SB
20	# =		3	8			8		2	1	
21	@ '		4	8			8	4			
22	:		5	8			8	4		1	
23	>		6	8			8	4	2		
24	✓		7	8			8	4	2	1	TM
25	?	12	0		B	A	8		2		PZ
26	A	12	1		B	A				1	
27	B	12	2		B	A			2		
28	C	12	3		B	A			2	1	
29	D	12	4		B	A		4			
30	E	12	5		B	A		4		1	
31	F	12	6		B	A		4	2		
32	G	12	7		B	A		4	2	1	
33	H	12	8		B	A	8				
34	I	12	9		B	A	8			1	
35	!	11	0		B		8		2		MZ
36	J	11	1		B					1	
37	K	11	2		B				2		
38	L	11	3		B				2	1	
39	M	11	4		B			4			
40	N	11	5		B			4		1	
41	O	11	6		B			4	2		
42	P	11	7		B			4	2	1	
43	Q	11	8		B		8				
44	R	11	9		B		8			1	
45	‡	0	2	8		A	8		2		RM
46	S	0	2			A			2		
47	T	0	3			A			2	1	
48	U	0	4			A		4			
49	V	0	5			A		4		1	
50	W	0	6			A		4	2		
51	X	0	7			A		4	2	1	
52	Y	0	8			A	8				
53	Z	0	9			A	8			1	
54	0		0				8		2		
55	1		1							1	
56	2		2						2		
57	3		3						2	1	
58	4		4					4			
59	5		5					4		1	
60	6		6					4	2		
61	7		7					4	2	1	
62	8		8				8				
63	9		9				8			1	

Figure 3. Standard BCD Interchange Code

2/5 Bits

	0	1	2	4	8
0			X		X
1	X	X			
2	X		X		
3		X	X		
4	X			X	
5		X		X	
6			X	X	
7				X	X
8	X				X
9		X			X

Figure 4. Two-Out-of-Five Code

QUI-BINARY CODE

1410 arithmetic units use qui-binary representation of numeric characters (Figure 5). The qui-binary code offers more advantages than BCD in numeric addition and carry generation. During operations involving the arithmetic unit, data in BCD form is translated into qui-binary, treated arithmetically, and retranslated into BCD. To translate from BCD to qui-binary, the 1 bit becomes a binary 1 (B1). The 2, 4 and 8 bits become a quinary 0, 2, 4, 6, or 8 (Q0, Q2, Q4, Q6, or Q8). For example a 9 in qui-binary is a B1 and a Q8; an 8 is a B0 and Q8; a 1 is a B1 and Q0; etc.

Packaging and Component Parts

All units of the IBM 1410 System use the standard modular system (SMS) concept of design. Electronic circuitry is completely solid-state, using transistors and magnetic cores. Maximum usage is made of saturating drift transistor registor logic (SDTRL) circuits. These circuits are used because of their reliability, high speed, and low cost. All circuitry is in the form of plugable cards containing transistors and their associated circuits.

Card Code	BCD	True Add	Complement Add
0	8.2	Q0 B0	Q8 B1
1	1	Q0 B1	Q8 B0
2	2	Q2 B0	Q6 B1
3	1.2	Q2 B1	Q6 B0
4	4	Q4 B0	Q4 B1
5	1.4	Q4 B1	Q4 B0
6	2.4	Q6 B0	Q2 B1
7	1.2.4	Q6 B1	Q2 B0
8	8	Q8 B0	Q0 B1
9	1.8	Q8 B1	Q0 B0

Figure 5. Qui-Binary Code

Storage Principles

Magnetic core storage is used in the IBM 1411 Central Processing Unit. Characters are stored in the core-storage unit in binary-coded decimal (BCD) form. This requires seven bit locations, or core planes (C, B, A, 8, 4, 2, 1) for each character position. An eighth core plane provides for the storage of word marks (see "Word Mark").

ADDRESSING

Core-storage units are available with 10,000, 20,000, 40,000, 60,000, or 80,000 character positions. The arrays are arranged so that each character position can be individually addressed.

Each core-storage address is five character positions. Valid addresses for a machine with 10,000 characters of storage are 00000 to 09999. Valid addresses for a machine with 20,000 characters of storage are 00000 to 19999. Valid addresses for a maximum-capacity machine with 80,000 characters of storage are 00000 to 79999.

An attempt to use an invalid address results in an error. The numeric portion of the five-character address must consist only of valid numbers from 0 to 9. An attempt to use special character or blank codes in addresses results in an error-stop (address validity). The zone bits over the tens and hundreds positions are reserved for index tags as explained in "Indexing." The units-, thousands-, and ten-thousands-positions must contain a no-zone indication, or an error stop results.

Core storage addressing is as follows:

1. To address an instruction in core storage, specify the location of the high-order character (operation code).

2. Data fields to be moved from one core storage area to another, or fields to be operated on arithmetically, are addressed by specifying the location of the low-order character of the field. Characters are moved or operated on arithmetically in a low- to high-order sequence.

3. For all data movements that originate or terminate outside the core storage, and for record moves within core storage, the data is addressed by specifying the location of the high-order character. Therefore, data addresses of all input-output operations, including the file, specify the location of the high-order character. On an I-O operation, characters are moved from high to low order.

NOTE: Low order and high order refer to the positions of an instruction word or a data word as they would appear on a printed form or as a field in a card. Do not confuse these terms with the storage addresses which are numbered left to right, low to high in relation to a data word or an instruction word.

DATA WORD

A data word is one complete unit of information that is comparable to a field in a card, such as an account number.

VARIABLE WORD LENGTH

A data word may be a single character, or a group of characters. Words are not limited to any fixed number of character positions in the storage unit.

WORD MARK

To define the length of a word, a word mark is stored as a single bit in the eighth core plane of storage in the high-order position of that word. This word-mark core-plane is in all storage positions. Thus, the high-order position of a word can be placed at any storage address.

SCANNING

The core-storage unit can read out only one character at a time. A whole word must be read out character by character. The order in which these characters are read out is determined by the machine. For example, when two fields are added together, the units position of the fields must be read out first to determine the signs of the fields. Information read out to an output machine is read out high order to low order.

The treatment of these words, character by character, is known as scanning. Reverse scanning is the reading out from high order to low order, as in reading out to I-O machines. Forward scanning is the reading out of the low-order position first.

Stored Programming

The IBM 1410 System is controlled entirely by stored programming. A sequence or program routine of operations is stored or loaded in the core-storage unit before the system processes data. The processing unit then proceeds, step by step, through the stored-program routine, analyzing each instruction and performing the function called for before proceeding to the next instruction.

Just as program routines or jobs in the machines using control panels can be changed by changing control panels, a stored-program routine can be changed by loading a new routine into the storage unit via an input machine.

INSTRUCTION WORD

The instructions in core storage consist of a variable number of alphameric characters that combine to make up an instruction word. Valid instruction words vary in length from 1 to 12 characters, depending on the amount of information that the operation requires.

Valid instruction formats are:

O
O d
O XXX d
O AAAAA
O AAAAA d
O XXX BBBBB d
O AAAAA BBBBB
O AAAAA BBBBB d

O signifies the single-character operation code; AAAAA is the five-character address of the A field. BBBBB is the five-character address of the B field. XXX is the three character I-O unit and control field, and d is the operation modifier.

The instruction words are arranged sequentially in core storage. Subsequent instructions are located in higher-numbered storage positions. Each instruction word must have a word mark with its operation code. Any other word marks will result in a machine-stop when the word reads out. A word mark must also be in the location immediately to the right of the low-order character of the instruction word. Usually this is the operation code for the next instruction.

The address of an instruction is the location of its operation code. No operation code has two valid lengths that differ by only one character. Instruction-length checking insures that the instruction length as read out of storage is one of the valid lengths for the particular operation code. The add op code, for example, has three valid lengths: 1, 6, or 11 characters.

Control

The central processing unit (CPU) is made up of four major areas: a storage unit, an address unit, an operational unit, and a control unit.

1. The storage unit is the center of all data flow in the 1410. Information reads into storage from the assembly channel and reads out through a B data register to the B channel. A five-position address is fed to the storage unit to control the position of storage to be used.

2. The address unit stores and modifies the five-position addresses that locate the position of storage to be used.

3. The operational unit contains all the units necessary to edit, compare, move or add data.

4. The control unit contains registers, cycle controls, and a clock that are necessary to perform the various functions of the CPU.

The operation of the IBM 1410 System is controlled by the program routine stored in the core-storage unit. The completion of each program step requires two phases: instruction (I) phase and execute (E) phase.

INSTRUCTION PHASE

I phase is the first portion of the program step that is required to read the instruction word out of storage. The instruction word is made up of addresses, op code, op modifier, and control characters for I-O operations. As the characters read out during I phase, they are stored in registers in the control or address units. A storage cycle is required to read each character out onto the B channel. Because the length of the instruction words is variable, the number of cycles in I phase is variable.

I phase is further divided into I cycles. To identify which character of the instruction word is reading out of storage during an I cycle, an I ring counts the characters or cycles. The I ring consists of 13 triggers labelled I ring op, and I ring 1 through I ring 12 (Figure 6).

As the first I cycle of I phase is taken, the I ring is set to I ring op time to identify this character as the op code. The I ring then advances to I ring 1-time to identify the next character that reads out as either a modifier, or the ten-thousands position of an address, depending on the op code character that has already been read out and recognized.

An example of I phase is a data move instruction word which can consist of the op code, followed by an A field and B field address and a d modifier character:

D AAAAA BBBBB d

At I ring op time, the op code reads out of the storage unit and is set into the op register in the control unit. The op register is decoded to identify the next five characters as the A field address.

I rings 1 through 5 gate the characters into the proper positions of an address register, located in the address unit, called the A address register.

I rings 6 through 10 gate the next five characters to the B address register in the address unit. The character read out at I ring 11 time is the d modifier. It is stored in the op-modifier (op mod) register in the control unit. During I ring 12 time, the next character is read out to insure that a word mark is located in the next position of storage.

EXECUTE PHASE

At the completion of I phase, the machine is ready to perform the actual operation. This portion of the program step is the execute phase (E phase). The length and complexity of E phase depends on the type of op code. E phase can consist of A, B, C, D, E, or F cycles, with storage either forward- or reverse-scanned. Each cycle length varies from 4.5 to 7.5 (4.0-6.67) microseconds. At the completion of E phase, the machine normally returns to I phase to initiate the next instruction.

Data Flow

The center of data flow in the IBM 1411 Central Processing Unit is the core-storage unit that receives data from the IBM 1405 Disk Storage Unit, the IBM 1415 Console, or the IBM 1414 Input-Output Synchronizer (Figures 7 and 8). When processing is complete, the data can be sent to the 1405, 1415, or 1414.

The 1414 I-O Synchronizer controls the various input-output units that are used in conjunction with the 1410 System. The 1414 includes the integrated synchronizer, print storage, and tape adapter units.

The integrated synchronizer is an input-output control unit that contains up to eight 80-character magnetic-core storage units. These units provide independent buffering for all associated I-O units. A data transfer between the CPU and the card read punch or paper tape reader takes place through the integrated synchronizer. Processing time is saved because the CPU does not have to wait for a mechanical unit to pick up speed, etc.

The print storage unit contains a 132-position core-storage unit that is an intermediate storage device between the CPU and the IBM 1403 Printer. Included in the print area is the circuitry necessary to control the carriage for forms handling.

The tape adapter units provide a control system for the various tape units that may be used with the 1410 System.

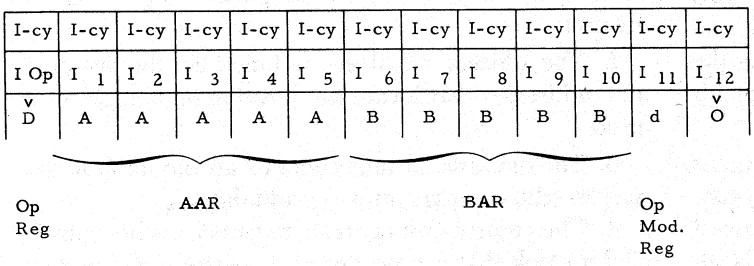


Figure 6. Instruction Phase

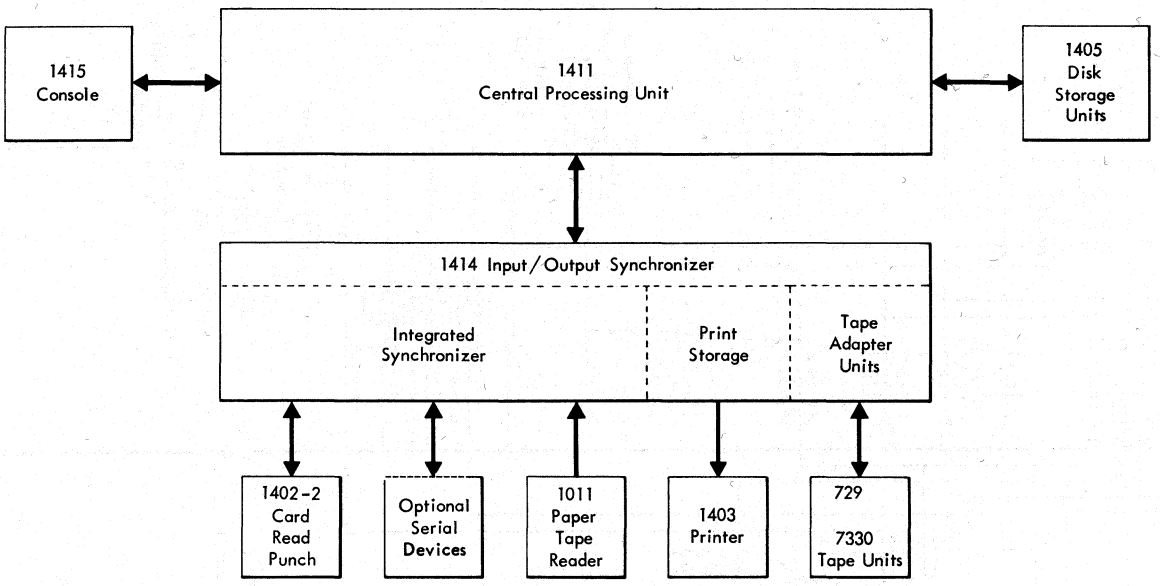


Figure 7. Data Flow

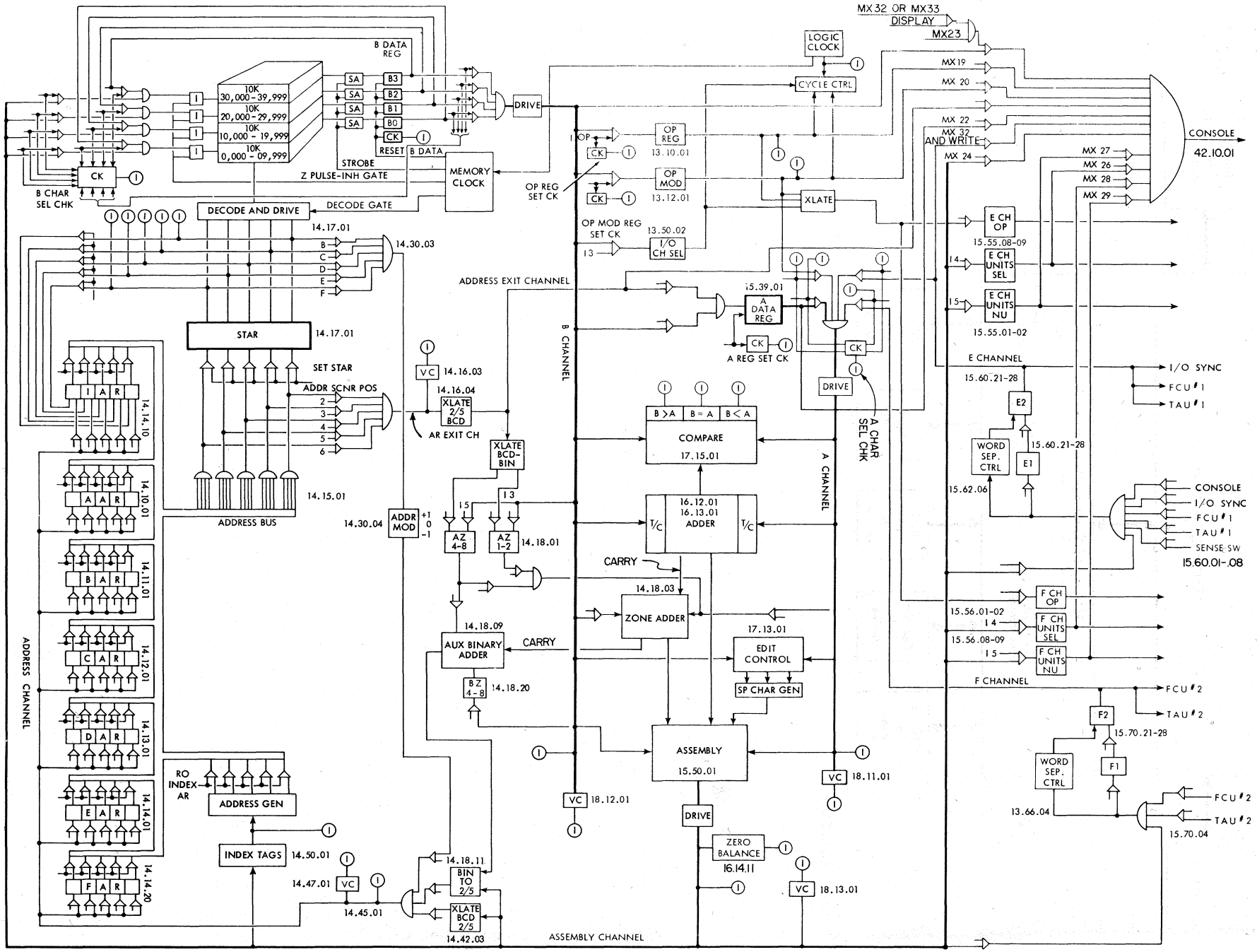


Figure 8. CPU Data Flow

The IBM 1411 Central Processing Unit is the hub of all 1410 System operations. Four frames form the integral units of the basic 1411. Frame A contains power supplies, circuit breakers, and relays necessary for power control and distribution throughout the system. Frame B contains the magnetic core storage unit. Instructions that define operations to be performed and the data to be operated upon can be stored in this unit indefinitely. Frame B also contains the SMS transistor cards that make up the address unit circuitry. The address unit stores the five-position addresses that locate positions in core storage to be used.

Frame C contains logic clock circuitry that generates timing pulses for the 1411 and also contains the cycle control unit. The adder and assembly circuits are also located in frame C. Internal data flow in the 1411 is controlled partially by the assembly unit. Operation decode circuits in frame D analyze each instruction word to determine the what, where, when, and how of any operation. Also in frame D are the compare and edit control units. Input-output circuits necessary for the flow of data into and out of the 1411 are located in both C and D frames.

Control Unit

The logic clock generates timed impulses that are used to form gates that control all functional units of the 1411.

Logic Clock

Various 1410 System operations require different length storage cycles. These cycles range from six to ten pulses; the number of pulses depend on the type of operation being performed. The pulses are called logic gates A through K. The logic clock circuit uses a free-running crystal-controlled oscillator and a ten-trigger ring to develop the number of logic gate pulses required (Figure 9).

The oscillator drives a binary input trigger called the clock pulse trigger. The outputs of the clock pulse trigger are called "first clock pulse" (1CP) and "second clock pulse" (2CP). The clock is normally stopped with the stop latch that, by collector pullover, clamps the clock pulse trigger at 1CP. The logic gate A trigger is also on. When the stop latch is reset, the clock pulse trigger is advanced by the oscillator. At the end of 2CP, the ring is advanced from logic gate A (LGA) to logic gate B (LGB). Since clock pulses are .375 (.333) microseconds long, the ring advances every .750 (.666) microseconds (Figure 10).

Cycle length is defined by controlling the point at which the ring stops advancing and returns to its starting position. Type of cycle and type of operation control cycle length by conditioning the "stop at F, H, J, or K line." This line combines with the corresponding logic gate pulse to bring up "last logic gate (LLG)." LLG sets the logic gate Z latch that gates the ring back to LGA. To stop the clock at the end of a cycle, the stop latch is set on by the 2CP of the last logic gate. The stop latch combines with 1CP to clamp the clock pulse trigger at 1CP, LGA (Figure 11).

UNOVERLAP OPERATION

All I-O commands (except F or K) can be executed one of two ways: unoverlapped or overlapped. An unoverlapped command causes the CPU to take E cycles (channel 2) or F cycles (channel 2), as required, to read in or read out each I-O character. Because the CPU reads in or reads out characters at a faster rate than any I-O machine, the CPU must wait between each E or F cycle until the I-O device sends, or is able to receive, another character.

During E phase of an unoverlapped I-O instruction, "compute disable cycle" comes up to stop the clock by preventing (by collector pullover) the LGA trigger from coming on. The clock pulse trigger continues to advance. When an I-O cycle is needed, "E, or F cycle required" overrides "compute disable cycle" to allow the ring to advance through the cycle. Logic gate Z that gates LGA on is reset by LGA. As long as "compute disable cycle" prevents LGA from setting, LGZ remains on until another I-O cycle is required (Figure 12).

OVERLAP OPERATION

An overlapped I-O instruction allows the CPU to use the time between E or F cycles for compute cycles.

Six triggers, added to the clock circuits, form a logic gate extension ring. These are triggers LGR through LGW. When an overlapped I-O cycle is taken, the extension ring is used instead of the normal logic-clock ring (Figure 13).

Logic gate Z gates on both LGA and LGR. When "E or F cycle required" is up in an overlapped operation, it

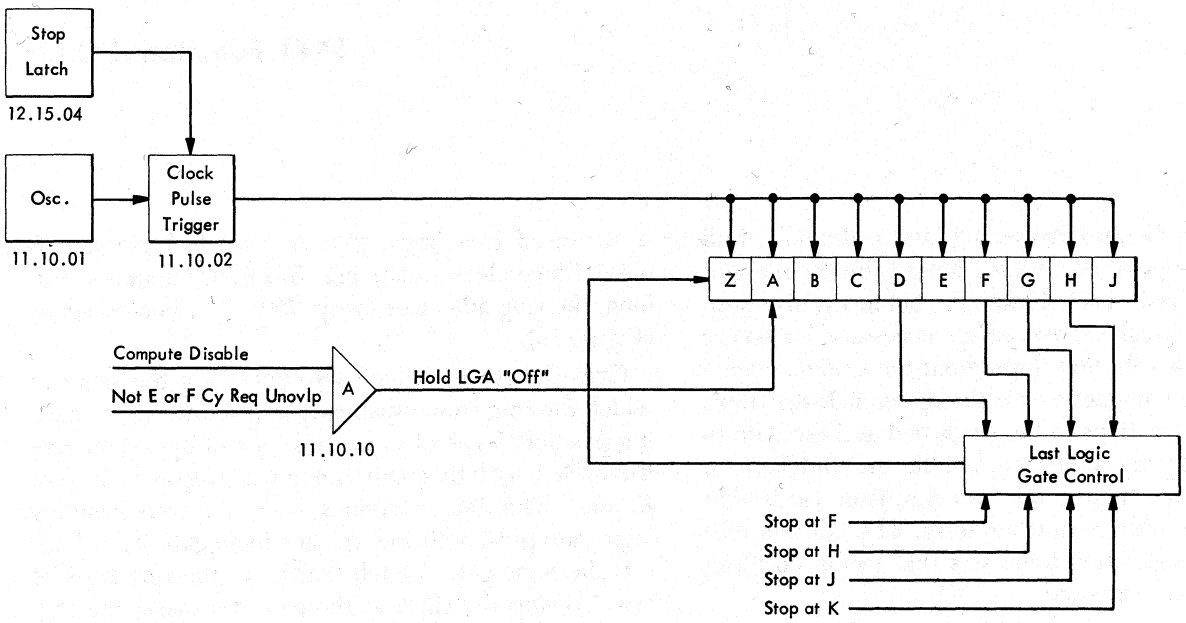


Figure 9. Logic Clock

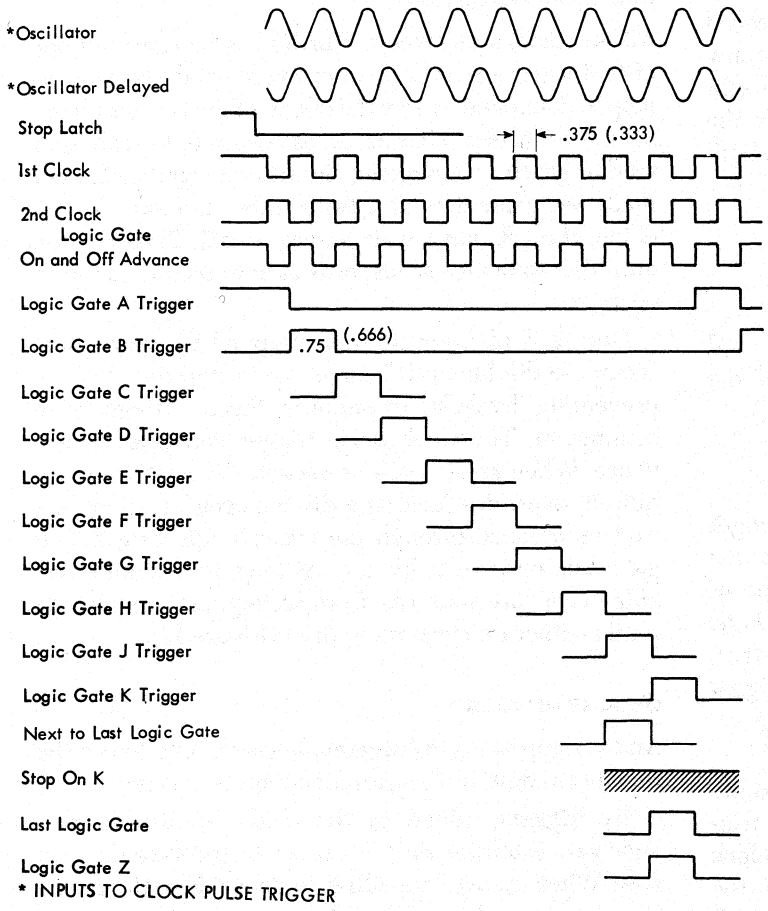


Figure 10. Logic Clock Pulses and Gates

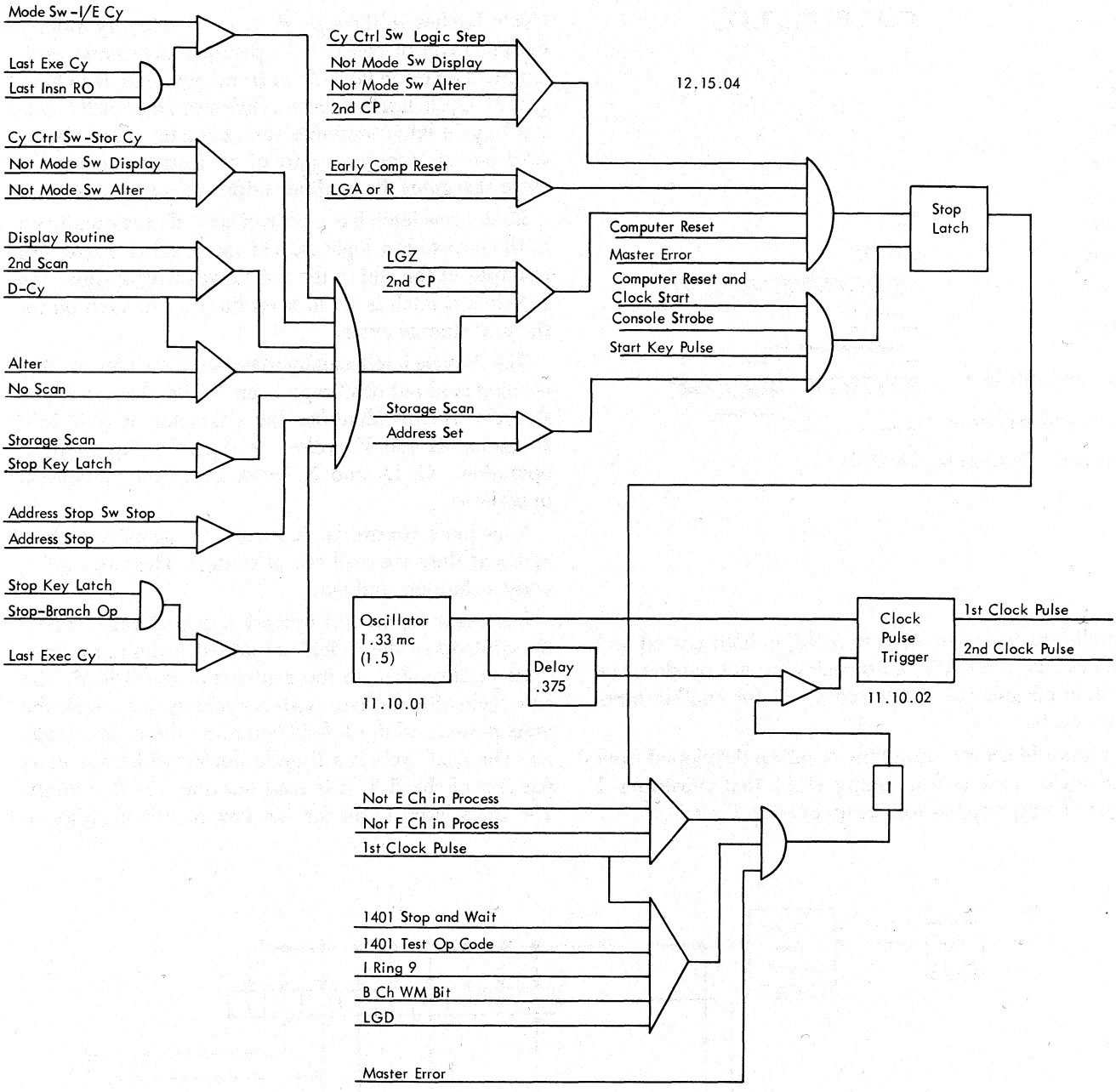


Figure 11. 1410 CPU Clock Control

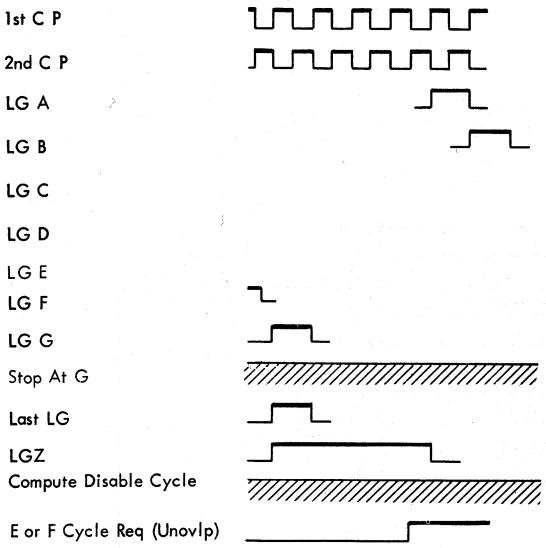


Figure 12. Compute Disable Cycle

conditions "compute disable cycle" to hold LGA off and allows LGR to set. When I-O cycles are not needed, LGR is held off and LGA is allowed to set for another compute cycle.

Figure 14 shows a sampling of pulses developed from the logic clock and a timing chart that illustrates I phase being stopped to take an overlap E cycle.

Cycle Control

Cycle latches A through F, I, or W identify storage cycles. Type of cycle and operation determine cycle length. The cycle latch is on from logic gate B to logic gate B. Cycle latches control different areas of the CPU; the I cycle latch identifies the character that is being read out of storage as part of an instruction word. I cycle also gates the modified address into the IAR.

Each cycle latch has a control latch that is usually set at the next-to-last logic gate of the previous cycle. For example, at the end of the I cycle at I ring op-time, the I cycle ctrl latch is set to keep the I cycle latch on for the next storage cycle.

The A cycle latch usually identifies the character that is being read out of storage as an A field character. The B cycle usually identifies the character as a B field character. E and F cycles are used for input-output operations. C, D, and X cycles are used for special operations.

Four more control latches assist in identifying characters as they are read out of storage. They are: units, body, extension, and MQ.

For example, an add operation is performed where the contents of the A field are added, a digit at a time, units position first, to the contents of the B field. The first cycle after I phase is an A cycle during which the units position of the A field is set into the A data register. The next cycle is a B cycle during which the units position of the B field is read out onto the B channel. The units latch is set for the first A and B cycles to

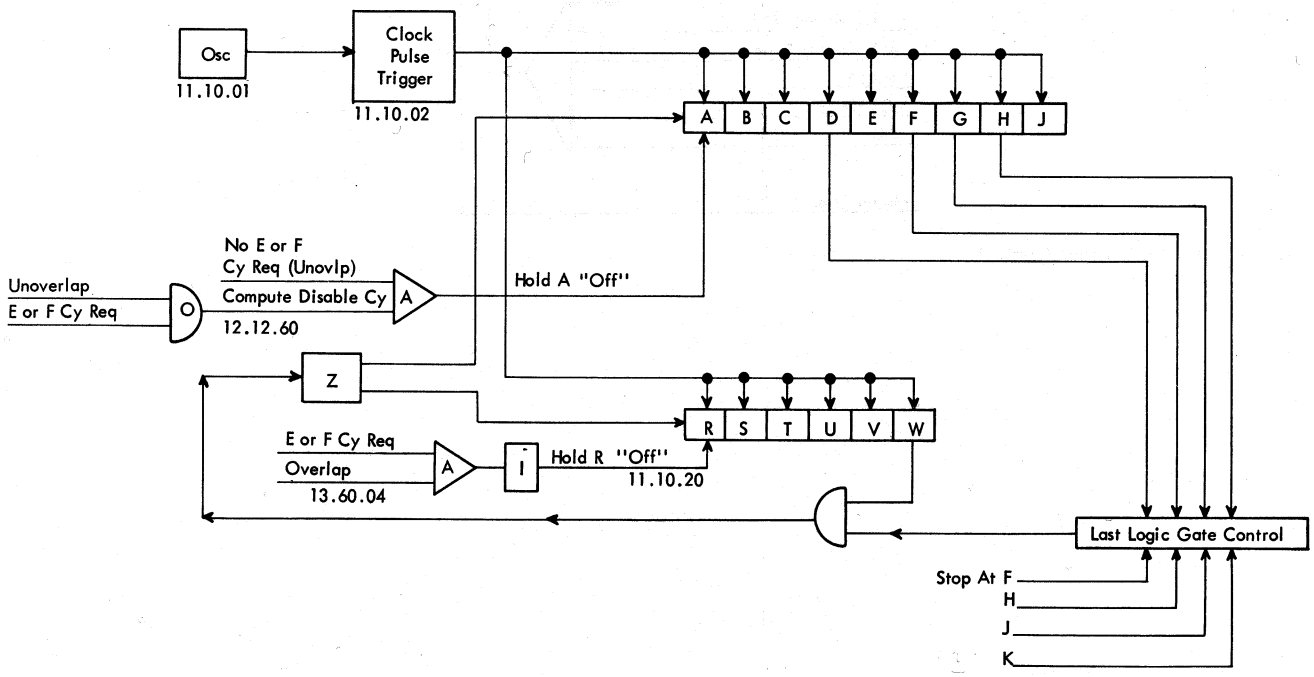


Figure 13. Overlap

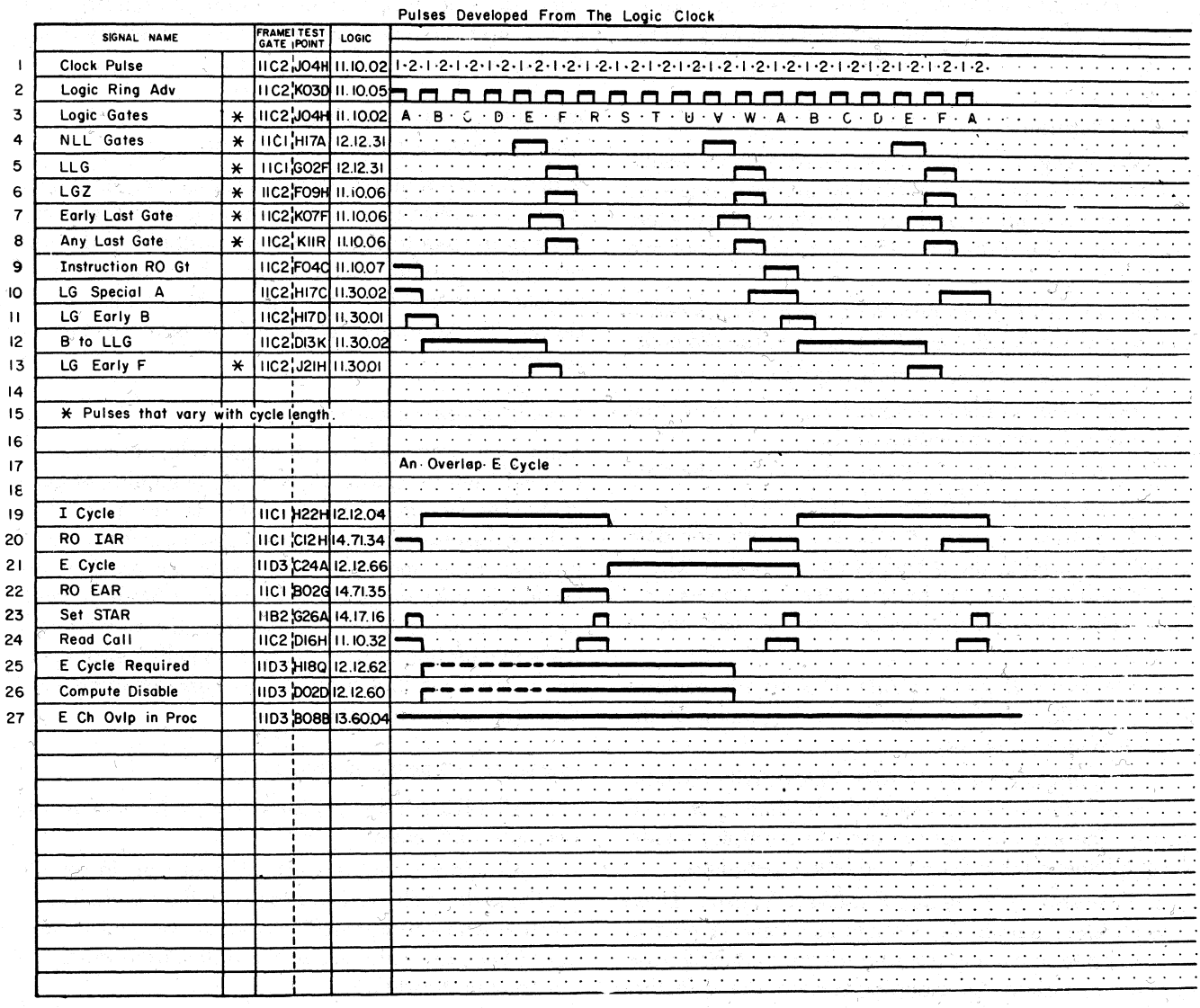


Figure 14. Logic Clock Pulse Timings

identify the characters as units-position characters because that is where the signs of the fields are located.

The body latch is set after the units position is set and stays on until the end of the A field. The extension latch identifies the remaining B field characters that have no corresponding A field characters (Figure 15).

	EXT	BODY	UNITS+
A-Field		0 1 2 9	0
B-Field	0 2	1 9 8 7	0
	0 2	2 1 1 6	0

Figure 15. Control Latches

The MQ latch is used in multiplication and division to identify a character as a position of the multiplier or quotient. The MQ latch is also used in edit and zero suppress op codes.

Address Unit

The address unit, which stores and modifies the five-position addresses that locate the position of storage to be used, contains eight address registers. One of these, the storage address register (STAR) is used as an output of the address unit that is fed to the core-storage unit. The STAR is read into from any one of the seven other address registers (labeled A through F, and I), or from the address generator (used for indexing). The address unit also contains an address modifier that is used to

add one or subtract one from the address in STAR to obtain the address of the next position of storage (Figure 8).

Address Registers

An address register (AR) is a temporary storage device that reads in or out the five-digit addresses that are required to locate information in core storage. Characters are stored in the address registers in the two-out-of-five code.

Each address register position has five latches corresponding to the 0, 1, 2, 4 and 8 bits used in the 2/5 code.

The functions of these address registers are:

1. *Instruction Address Register (IAR).* This is used to locate and scan instruction words.

2. *A Address Register (AAR).* This locates the data word to be used as the A field of an instruction.

3. *B Address Register (BAR).* This locates the data word to be used as the B field of an instruction. The A and B field addresses are read into the AAR and BAR, respectively, when an instruction word is read out of storage.

4. *C Address Register (CAR).* This usually contains the same address as the AAR at the beginning of the execute phase (E phase).

5. *D Address Register (DAR).* This usually contains the same address as the BAR at the beginning of the E phase. The CAR and DAR are used in multiply, divide, recomplement, table search, and other operations.

6. *E Address Register and F Address Register.* These two registers contain the storage locations for characters going to or coming from I-O machines during overlapped operations. Overlapping is an optional feature and is discussed in "Overlap."

READ INTO ADDRESS REGISTERS (IAR, AAR, BAR, CAR, DAR, EAR, AND FAR)

Circuits for all address registers are very similar. For example, the 8 bit latch in the hundreds position (HP 8B) of the BAR is shown in Figure 16.

Before BAR is read into, the BAR reset line resets all latches off. If the "address channel 8 bit" line is up (active), the top leg of the AND circuits of all AR 8B latches is up. "Set AR HP" is up on the second leg of all hundred position latches of all address registers. "Set BAR" is up to complete the coincidence necessary to set this latch.

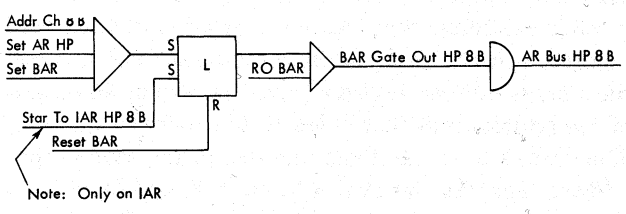


Figure 16. Address Register Latch (14.11.03)

READ OUT OF ADDRESS REGISTERS (IAR, AAR, BAR, CAR, DAR, EAR, AND FAR)

When the CPU requires the next character of the B field word, "read out BAR (RO BAR)" gates the output of every latch in the BAR to the AR bus. All positions of the BAR read out in parallel. "Set STAR" sets the storage address register with the bits received on the AR bus, which causes the addressed character to be read out of storage.

STORAGE ADDRESS REGISTER

Since every CPU cycle is a storage cycle, STAR is set in parallel from the address bus at the beginning of each cycle. The storage address register has no "reset" line as have the other seven address registers; it is reset by a program reset operation only. Using the previous example, the STAR HP 8B latch is turned on or off depending on the status of the bit lines from the address bus. An active bit line turns on its corresponding STAR latch; an inactive bit line turns off its corresponding STAR latch (if that latch was on).

SUMMARY OF ADDRESS REGISTERS

1. All 1410 address registers store addresses in the two-out-of-five code.

2. All address registers except STAR read in serially via the address channel starting with the ten-thousands position when an instruction word is read out of storage. (The IAR is also set in a parallel from STAR. See "Instruction Read-Out."

3. All address registers read out in parallel.

4. STAR is used as an output of the address unit. The output of any one of the other address registers is gated in parallel via the address bus to STAR at the beginning of each storage cycle.

Address Modification

The address in the address registers (AR) locate, in storage, the first character of the next word to be read out. This character is the units position of the field if the word is to be forward-scanned, or the high-order position of the field if the word is to be reverse-scanned. For every character read out of storage, the address of that character must first be read into STAR. To develop the address of the next character in the word, the machine takes the address of the character now being read out of storage and modifies it by plus or minus one (depending on whether the word is being reverse- or forward-scanned). Adding or subtracting one from the

address in STAR to develop the address of the next character is called address modification.

The address modifier must be able to:

1. Subtract one from the address when forward-scanning.
2. Add one to the address when reverse-scanning.
3. Recognize when it is subtracting one from a zero in order to borrow one from the next higher position.
4. Recognize when it is adding one to a nine in order to carry one into the next higher position.

OPERATION

Address modification must be completed during the shortest storage cycle; 4.5 (4.0) microseconds (Figure 17). During storage cycles longer than 4.5 (4.0) microseconds, address modification is still completed from logic gates B through F.

During a cycle where the A address register (AAR) is used to read out a data word, the address in the AAR is set into STAR (Figure 18) on the second clock pulse of logic gate A. The AAR resets on the first clock pulse of logic gate B, while the units position of STAR is gated to the address modifier.

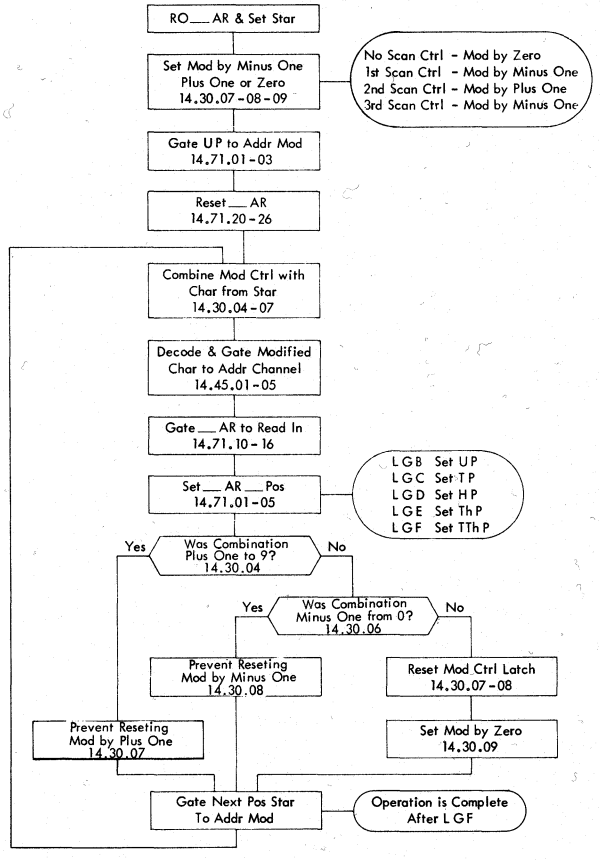


Figure 17. Address Modify Operation

The address modifier controls are set to modify by minus one by first scan control. The CPU contains four scan-control latches. The first or third scan latches are on when scanning storage from units to the high-order positions. The second scan latch is on when scanning from high- to low-order positions. The no scan latch is on when the address of the character is not to be changed.

Modify by minus one and the 0 from STAR combine to bring up 8 bit and 1 bit lines which are gated into the units position of the AAR on the second clock pulse of logic gate B.

When the address modifier subtracts 1 from 0, it keeps the mod by minus one latch on to borrow one from the next position. The 2 in the tens position of STAR is gated to the address modifier at logic gate C and combines with modify by minus one to send a 1 to the tens position of the AAR.

The modifier controls are set to modify by zero, which passes the rest of the address unaltered through the modifier.

CIRCUIT OBJECTIVES

1. Reset the address register, depending on the type of cycle. For example, A cycle reads the modified result into the AAR, B cycle reads the address into the BAR; I cycle reads into the IAR.
2. Set modifier controls and after modifying the units position, controls are set to mod by zero except when minus one and a combination of 2 and 8 bits (borrow one) or plus one and a combination of 1 and 8 bits (carry). (See Figure 19.)
3. Gate STAR to address modifier.
4. Combine mod controls and character.
5. Gate result to address register.

NOTE: Objectives 2 through 5 are repeated for all five positions.

Figure 20 shows address modify timings involved during an instruction read-out operation.

ADDRESS MODIFY CIRCUIT DESCRIPTION

Refer to Figure 18 when following this description.

1. Reset the address register.

SIGNAL	CONTROL	LOGIC
Reset AAR	A Cycle Ctrl	14.71.20

2. Set modifier controls.

Addr Mod Set to Minus One	1st Scan Ctrl	14.71.41
Set Mod by Minus One	Addr Mod Set to Minus One	14.30.08
Mod by Minus One	Set Mod by Minus One	14.30.08

3. Gate STAR to address modifier.

Mem AR UP 2B to Addr Mod	Mem AR 2B Latch LGB	14.17.02

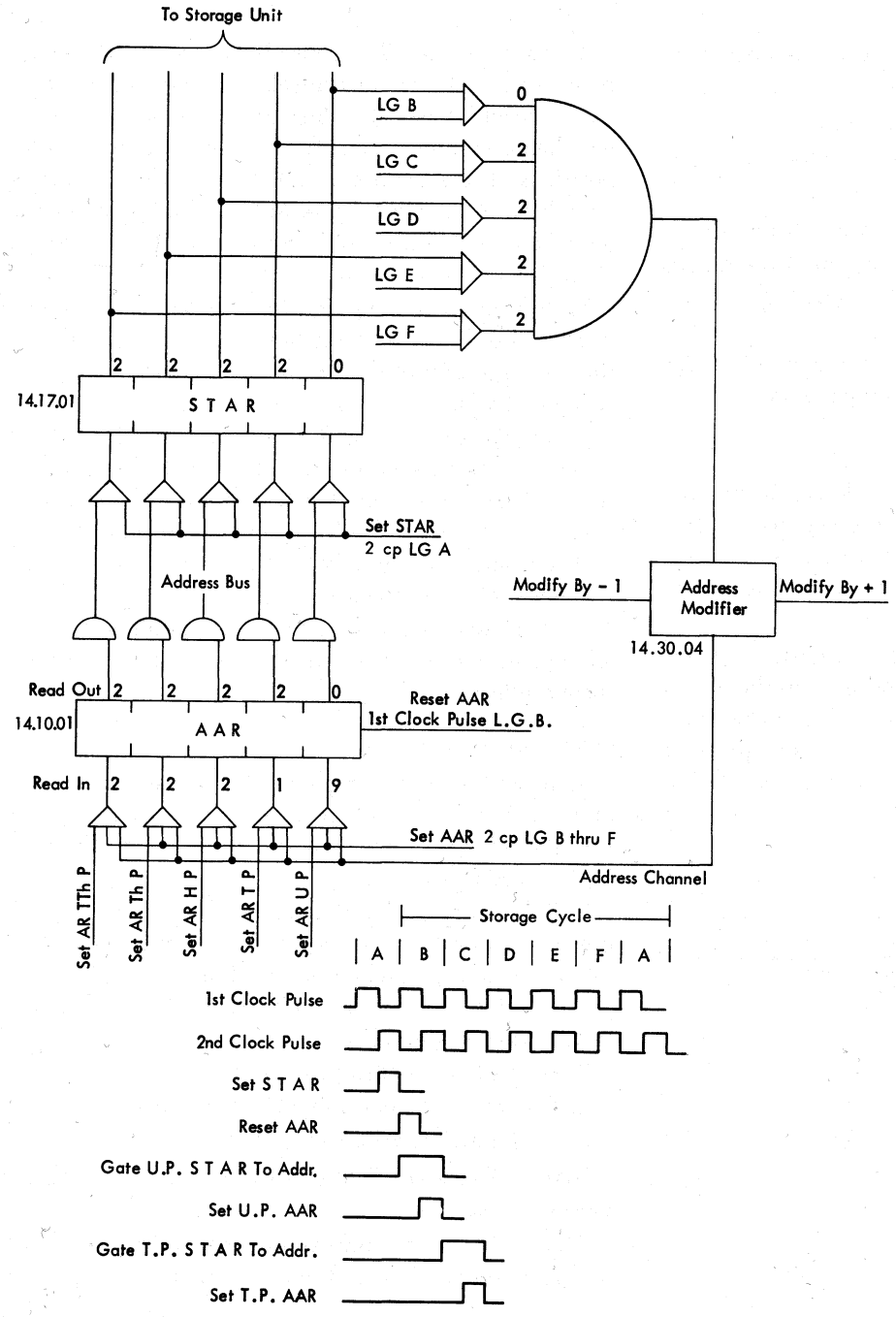


Figure 18. Address Modification of ARR

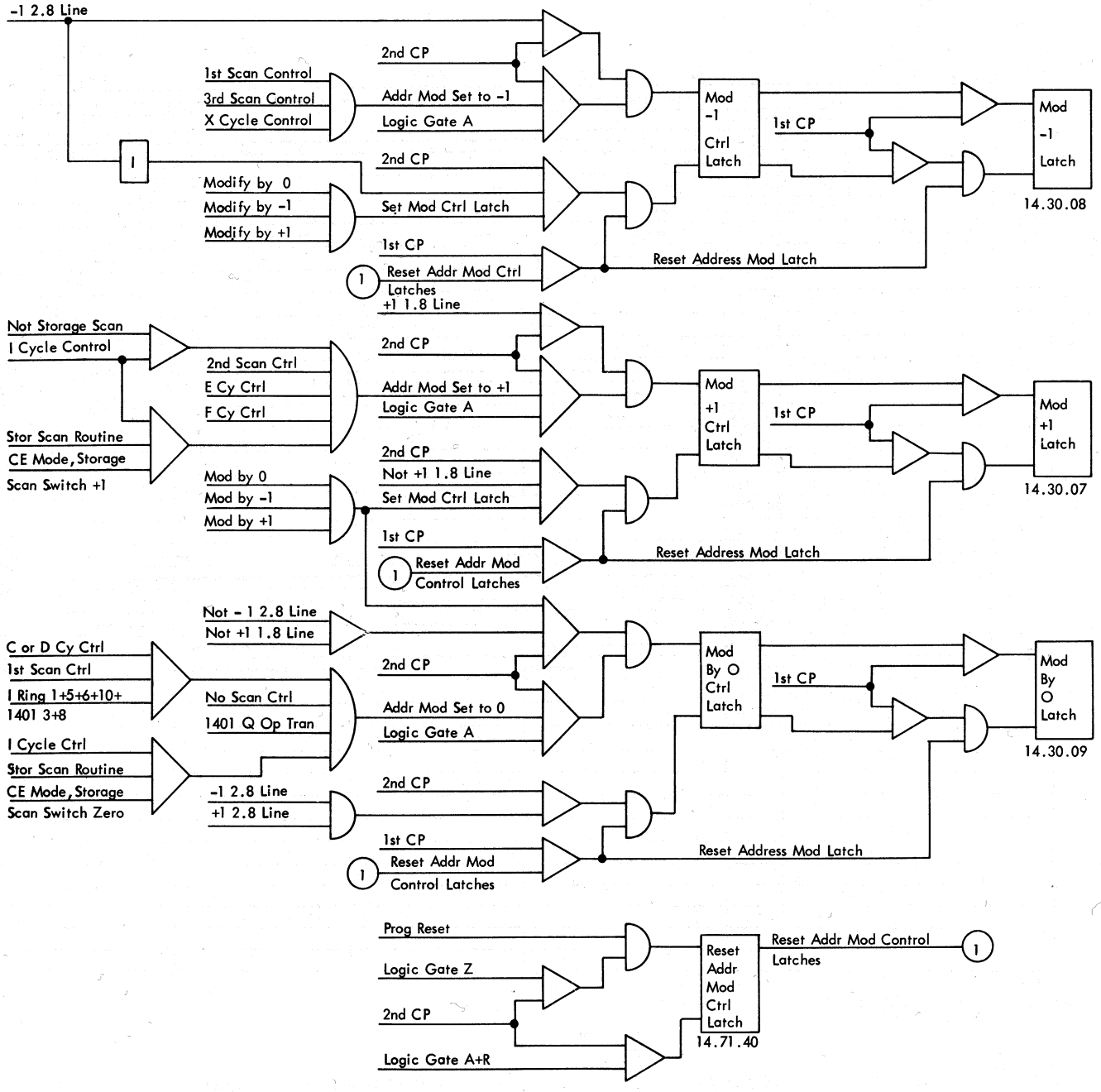


Figure 19. Address Modify Latches

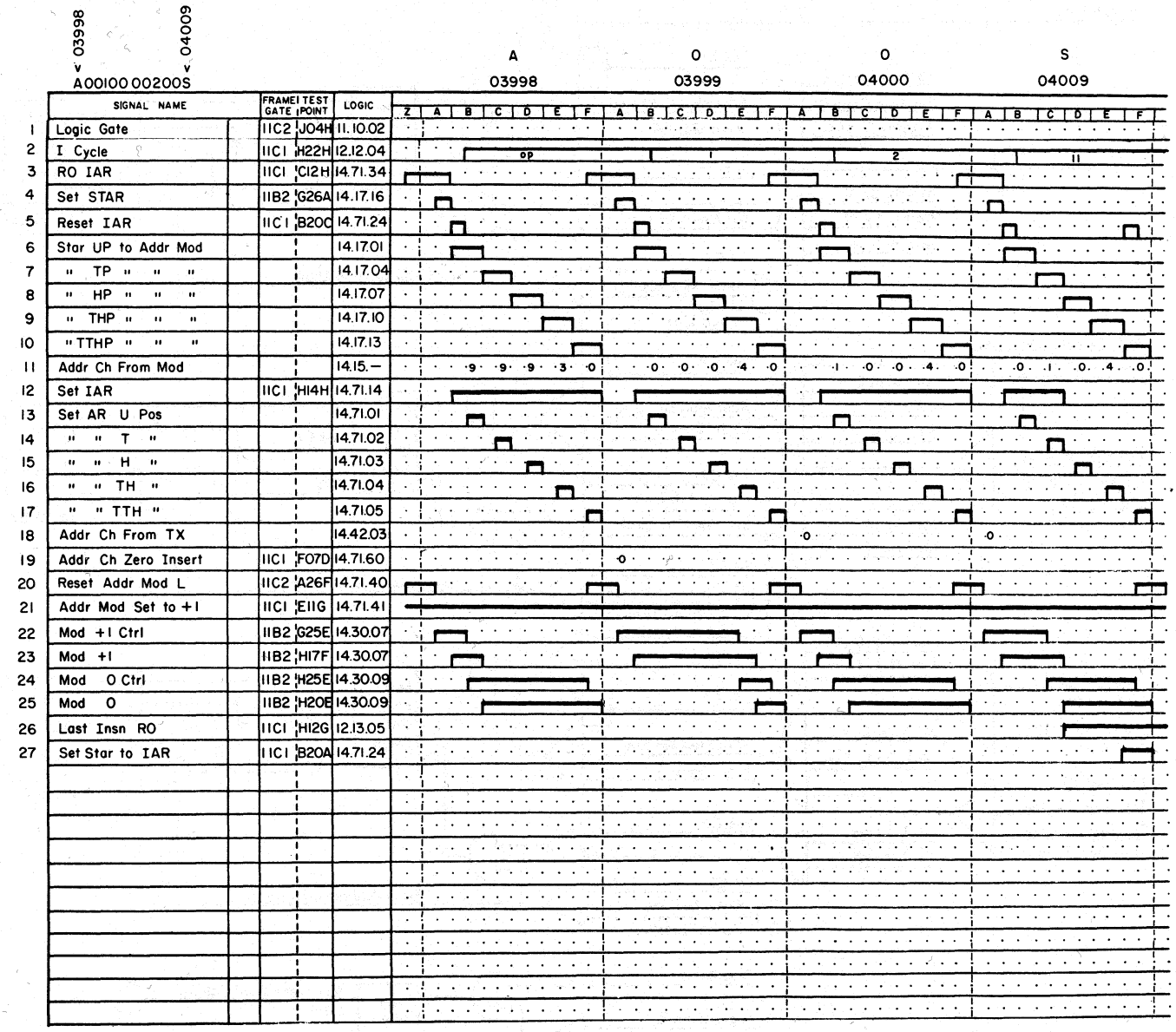


Figure 20. Address Modify Timing

4. Combine mod controls and characters.

Minus One 2 and 8 Line	Mem AR 2B 8B and Mod by Minus One	14.30.06
Addr Mod 1B and 8B	Minus One 2 and 8 Line	14.30.06
Addr Ch 1B * AAR-UP1B	Addr Mod 1 and 8B	14.45.02
Addr Ch 8B * AAR-UP8B	Addr Mod 1 and 8B	14.45.05

5. Gate result to address register.

Set AAR	A Cycle LG-B, C, D, E & F	14.71.10
Set ARU Pos	LGB-2nd CP	14.71.01

6. Set modify controls.

Set Mod Ctrl Latches	Mod by Minus One	14.30.07

Set Mod Ctrl Latches tries to reset Mod by minus one and set Mod by Zero but Minus one 2 and 8 line prevents it.

7. Gate STAR to address modifier.

Mem AR TP2B to Addr Mod	Mem AR 2B Latch LGC	14.17.05

8. Combine mod controls and character.

Addr Mod 0 and 1 Bit	Mem AR TP 2B, 0B and Mod Minus One	14.30.04
Addr Ch 1B * AAR TP1B	Addr Mod 0 and 1 Bit	14.45.02

9. Gate result to address register.

Set AAR	A Cycle, LGB C	14.71.10
Set AR 7 Pos	LGC and 2nd CP	14.71.02

10. Set modifier controls.

Mod by Zero	Set Mod Ctrl Latches, Not Minus One 2 and 8 Line	14.30.09

The rest of the address is fed through the modifier with no alterations.

Address Exit-Channel Validity Check

The CPU uses two validity check (vc) circuits to validate the characters in the core-storage addresses. One vc circuit insures the validity of the characters when they are read in on the address channel; the other checks the characters when they are gated from the address bus to the address exit channel.

OPERATION

Every valid character that is gated on the address exit channel falls into one of the two vc groups (Figure 21). If the character is invalid because a bit was dropped, neither of the vc groups are conditioned. If the character has an extra bit, both vc groups are conditioned at the same time. The vc groups gate on the error trigger when they are either both down or up. If the trigger is on at the end of the cycle (error sample time), addr exit error is gated to stop the CPU with this error (master error).

The input to the vc circuit must be a valid character on every storage cycle. When the exit channel is not in use, zeros are inserted on the channel to satisfy the circuit.

The check test lines in Figure 21 are controlled by three momentary switches on the console CE panel. These switches, labeled first, second, and third check test, force error conditions to insure that the transistors in the check circuits are working properly.

Check the circuits by pressing a check test switch and the start key. The CPU takes a cycle and should stop with every check-indicator light on.

The first check test conditions both vc groups to cause an error. The second check test blocks the zero inserted on the exit channel to cause both vc groups to be down. The third check test gates the error trigger on. Every transistor in the check circuit must operate correctly or the error light will not come on.

Address-Channel Validity Check

The circuit for this vc is similar to the exit-channel circuit except that a new character is gated on the channel every logic gate instead of one character each cycle. An error must be stored until the error sample line comes up at the end of the storage cycle.

OPERATION

Each character falls into one of two vc groups. If both or neither group is up, an error must be detected. Because there is a new character on each logic gate, the circuit must allow time for the character to arrive on the channel and to be decoded into one of the two groups before the vc group lines can be sampled. The circuit allows time by controlling a trigger with collector pullover.

The circuit (3H in Figure 22) shares a common load resistor with the OFF side of the error trigger. Before the trigger can be set on, the transistor in the AND circuit must be cut off. Once the trigger is set on, the OFF side goes minus and blocks the circuits to the block 3H circuit. Regardless of the validity of the remaining characters that are gated onto the address channel, the trigger remains on, because the gate for the off input is tied to −12, and at the end of the cycle address channel error is gated to stop the CPU.

On storage cycles longer than 4.5 (4.0) microseconds, a 0 is inserted on the address channel to satisfy the vc circuit. The second check test blocks the 0 to force both vc groups down in order to cause a vc error.

Operational Unit

The operational unit of the 1411 contains the functional units that are necessary to compare data, perform arithmetic operations, edit data, and to perform other data handling operations. There are two channels that feed data to the operational units; A channel and B channel. There is one output from the operational unit called the assembly channel. Data on the assembly channel go to the console or some other output device or back to core storage (Figure 23).

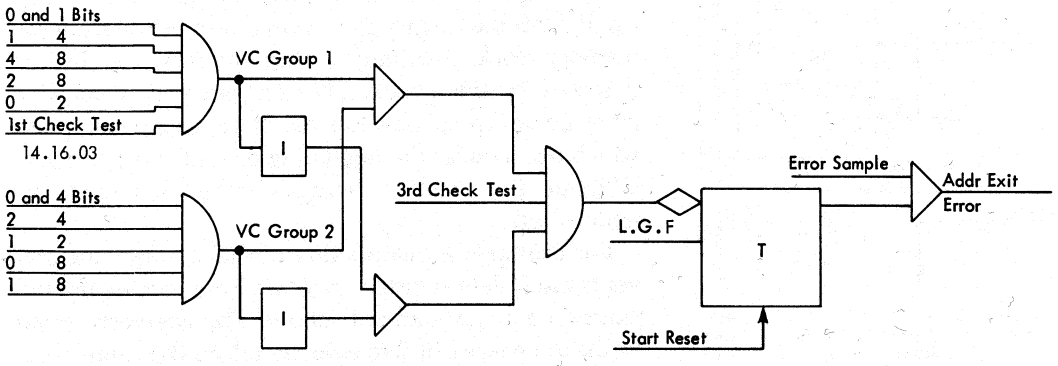


Figure 21. Address Exit Channel Validity Check (18.14.02)

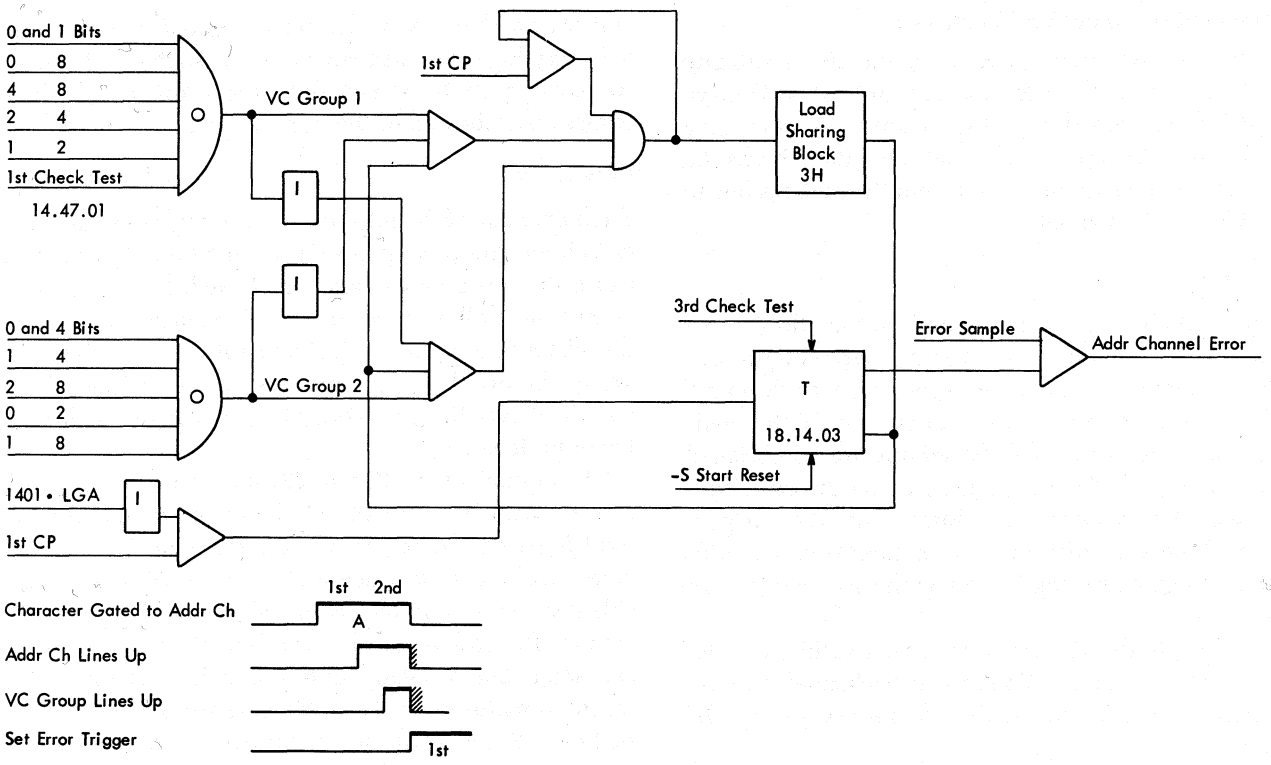


Figure 22. Address Channel Validity Check (18.14.03)

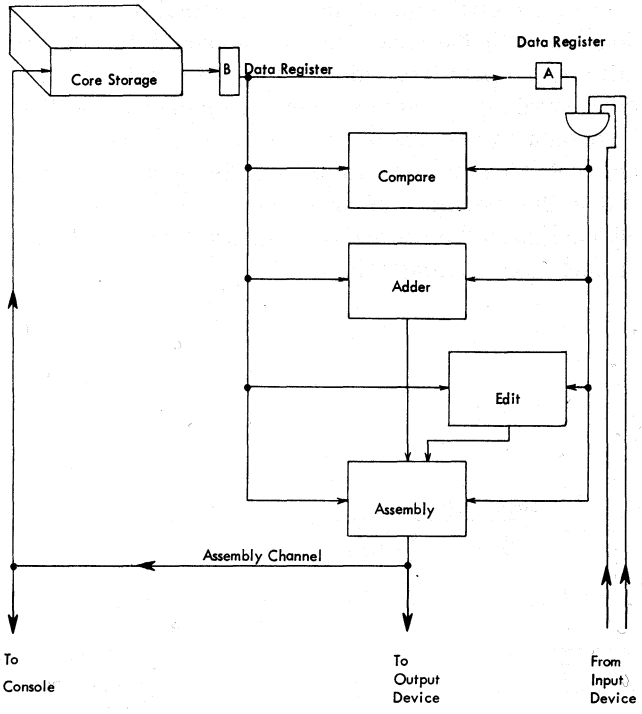


Figure 23. Operational Unit

B Data Register

Depending on the size of storage, two to eight characters are read out of core storage into the B data registers. The ten-thousands position of STAR selects which register is to read out onto the B channel. If the storage cycle is taken only to read out a character all of the B data registers are read back into storage (regenerated). If the storage cycle is taken to write a new character into storage, the B data registers that are not selected are gated back into storage while the selected character is read in from the assembly channel.

B Register Set Check

The B register set check insures that on every storage cycle the B data register receives a reset pulse from the memory clock. A failure to start the memory clock is detected by this check. The start memory clock line must come up to develop the B register reset pulse which occurs near the beginning of each storage cycle. Without this check, a storage malfunction could go undetected.

For example, a malfunction in the storage unit prevents the B data register reset line from coming up and causes a storage read-out failure. The character gated to the B channel in this case would be the same character that was gated on the previous storage cycle.

Without the B data register set check this type of error would go undetected. For more information on the B register set check refer to *IBM 1410 Core Storage Customer Engineering Instruction-Reference,* Form R23-2555.

B Channel

When the selected character is gated out of the B data register onto the B channel, it is available to most of the units throughout the CPU. For example, when a character is read out during I cycles at I op time, it is gated from the B channel to the op register. At op modifier-character time, the character is gated to the op mod register.

During execute cycles, if the character is a B field character, it can be gated to the B channel side of the compare matrix, of the adder, of the edit unit, or of the assembly unit. If the character is an A field character it usually is gated to the A data register where it is retained for later use.

B Character Select Check

Depending on the capacity of the core storage unit, two to eight characters are read out of the cores into the B data registers. The B character select check ensures that *only* one character (as selected by the high-order position of the address) is gated onto the B channel. For more information on the B character select check, refer to *IBM 1410 Core Storage Customer Engineering Instruction-Reference,* Form R23-2555.

B Channel Validity Check

During every storage cycle, the selected character is gated from the B data register to the B channel where it is checked for an odd number of bits by the B channel validity check (VC) circuit. The B channel VC circuit must be satisfied on every storage cycle or an error is indicated and the machine stops.

OPERATION

To check the validity of an eight-bit character (Figure 24), the character is first considered as four groups of two bits each. The 1 bit and 8 bit lines combine to produce a "1 and 8 bit odd" or a "1 and 8 bit even," depending on the input status of the individual bit lines. The other three groups (2 and 4 bit lines, A and B bit lines, C and WM bit lines) combine to produce an odd or an even number of bits as the result of their respective groups.

In the numeric portion, two of the four digits-odd or digits-even lines will be active and will produce a numerics-odd or a numerics-even result. Similarly, the zones-odd or zones-even and the WM and C odd or even lines combine to produce zone and WM and C-bit odd or zone and WM and C-bit even results.

In the next stage, the VC circuits check two of the resultant four lines: numerics odd or even, or zone, WM, C odd or even. This combination will produce a character odd or character even result. If character even comes up, a VC error will occur when error sample comes up at the end of the storage cycle. Since character odd is a valid result, it will not cause an error at error sample time.

The line names in Figure 24 describe results in the logical operation of a VC circuit which is applicable to the B, A, and assembly channels. Except for the bit inputs, most of the line names used in the figure will not appear on systems diagrams. As an example, the zone and WM and C bit even line in systems diagrams is called validity check not numeric C bit line (except in the assembly channel VC circuits).

In systems diagrams this line is labeled to meet the requirements of the assembly unit inputs. The numeric C bit and zone C bit necessary to maintain odd parity for the individual portions of a character gated to assembly are generated in VC circuits of the B and A channels.

Using an invalid combination of bits such as 1, not 2, 4, not 8, A, B, not C and not WM, follow the character through the validity check circuit. Taking the numeric portion first, the 1 bit and not 8 bit will result in a 1 and 8 odd; not 2 bit and 4 bit will result in a 2 and 4 odd. Numeric even will come up when 1 and 8 odd and 2 and 4 odd combine.

On the zone portion of the character, the A bit and B bit produce A and B even; not C bit and not WM bit produce C and WM even. Zone and WM and C even will come up when A and B even and C and WM even combine. An invalid character is indicated when numeric even and zone and WM and C even combine to produce character even which combines with error sample to stop the machine with a VC error.

An error is indicated if the character is either even or not odd. Errors detected by character even are:

1. Bit configuration even.
2. Any bit with not bit and bit lines both up or both down.
3. Any transistor failure in the check circuit which brings a character even line up.

Errors detected by character not odd are:

1. Any transistor failure that prevents the digits-odd or digits-even lines from coming up.
2. Second check test conditions both numerics odd and numerics even. These combine with zones, WM, C odd or zones WM, C even to bring up both character odd or character even.

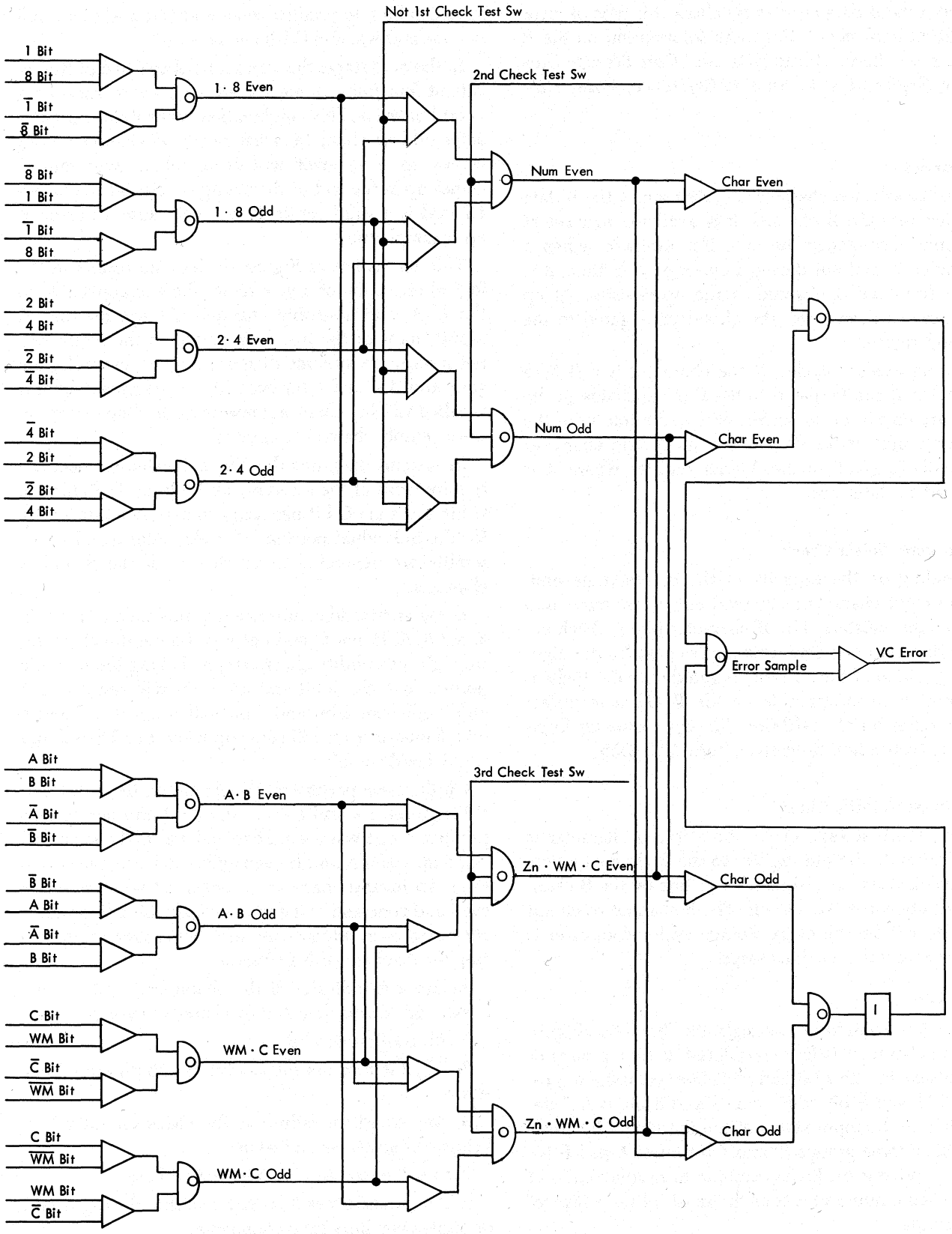


Figure 24. Validity Check Operation (B, A and Assembly Channels)

3. Third check test conditions both zones, WM, C odd and zones, WM, C even to combine with numerics odd or numerics even to bring up both character odd and character even.

A Data Register

Characters are read into the A data register from storage via the B channel, or from an address register via the AR exit channel (Figure 25). A single BCD coded character with or without word marks can be stored in the A data register until the corresponding character of the B field is available on the B channel, so that the two characters can be compared or added. The A data register is reset (all off except the C bit to maintain parity) before it can be read in.

A Register Set Check

The A register set check insures that the A data register receives a reset pulse before it is read in. This check is necessary to insure that, on a cycle when a new character reads in, the register first receives a reset pulse and also to insure that a character is not destroyed by an erroneous reset pulse if the character is needed on a later cycle.

Two binary input triggers (Figure 26) must both be off or on at the end of every cycle or an error occurs. One trigger is impulsed whenever "sw B ch to A reg" or "sw AR exit ch to A reg" are up. The other check trigger must receive the "reset A data reg" impulse before the end of the cycle or the error stops the machine.

A Channel

Information is gated to the A channel from one of four registers: A, E, F data registers, or the op-mod register (Figure 27). The A channel feeds data to the A side of the adder, compare, and assembly units.

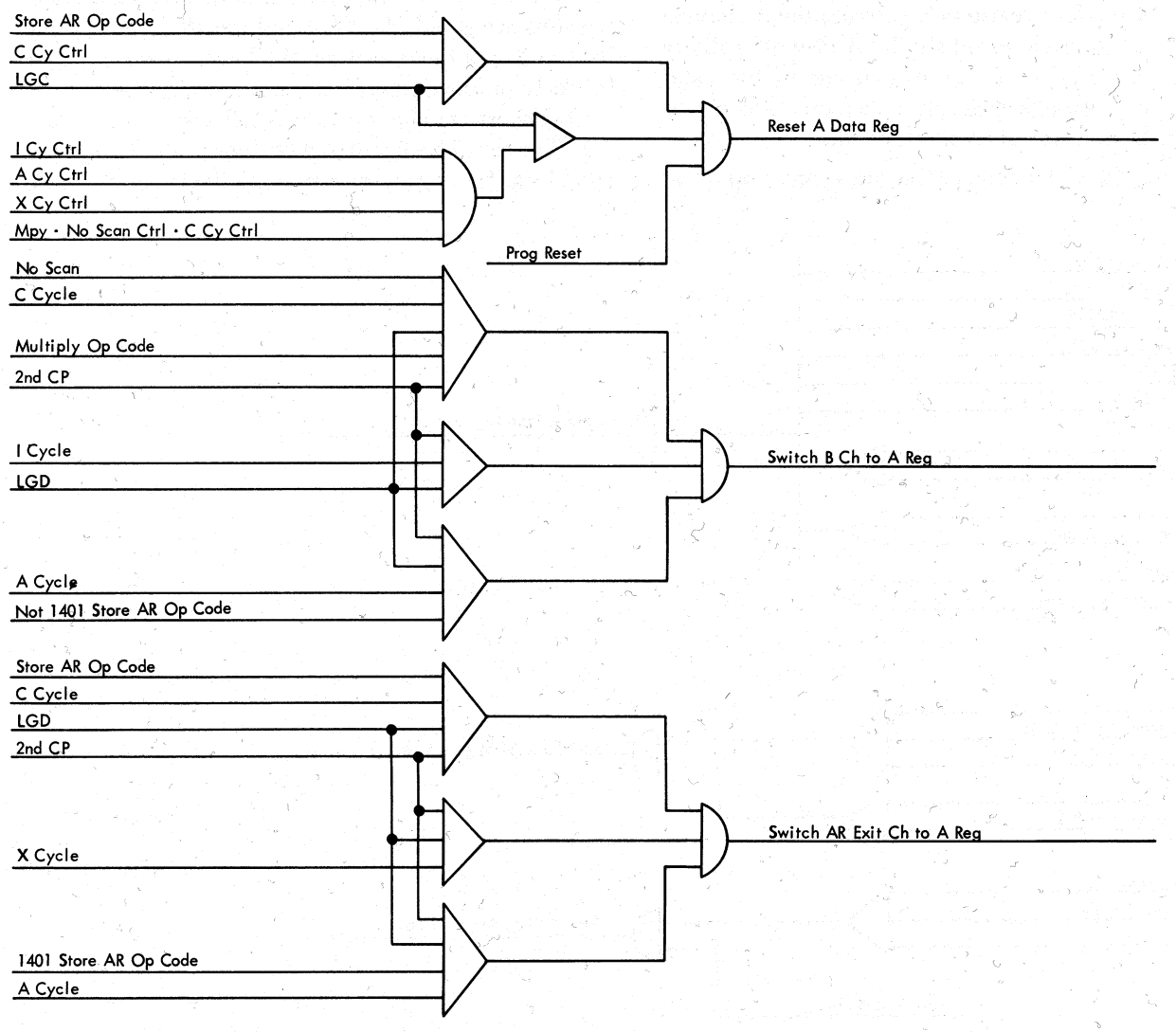


Figure 25. A Data Register Reset and Switching

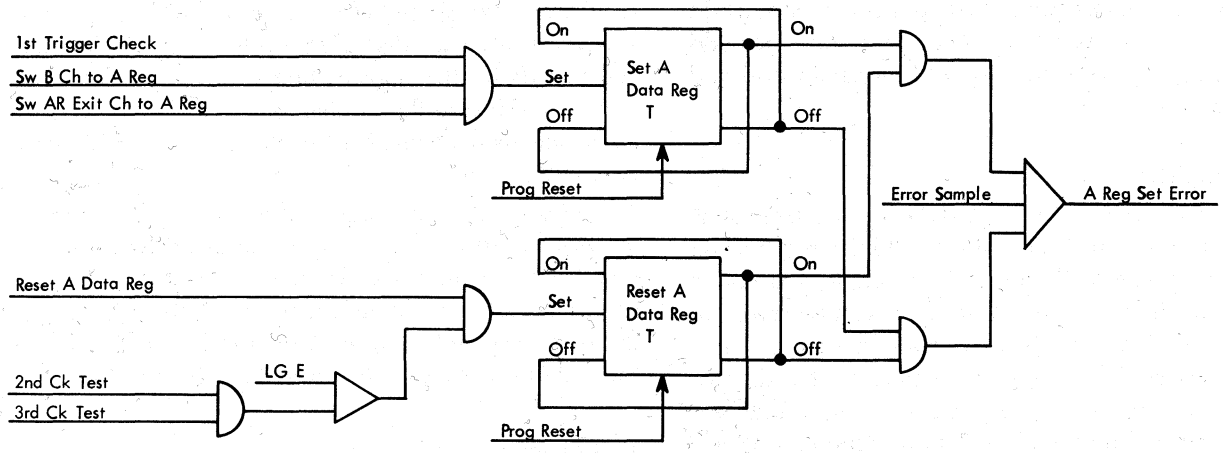


Figure 26. A Register Set Check (18.14.07)

A Character Select Check

The A character select check (Figure 28) insures that only one of the four registers is gated to the A channel on each storage cycle to satisfy the A channel validity check circuit. If none or more than one of the gates comes up on a storage cycle, an A character select error will stop the machine at error sample time.

In a cycle in which none of the gates comes up, none of the AND blocks will produce an output, the lowest OR will not have an active output, and an error will be gated at the end of the cycle. If both F2 and E2 data registers are gated, the third and fourth OR blocks will have active outputs, making the lower of the two AND blocks to produce an error at error sample time.

Check test switches operate as follows:

1. The first check test switch blocks the four input AND blocks forcing an error through the lower OR block.

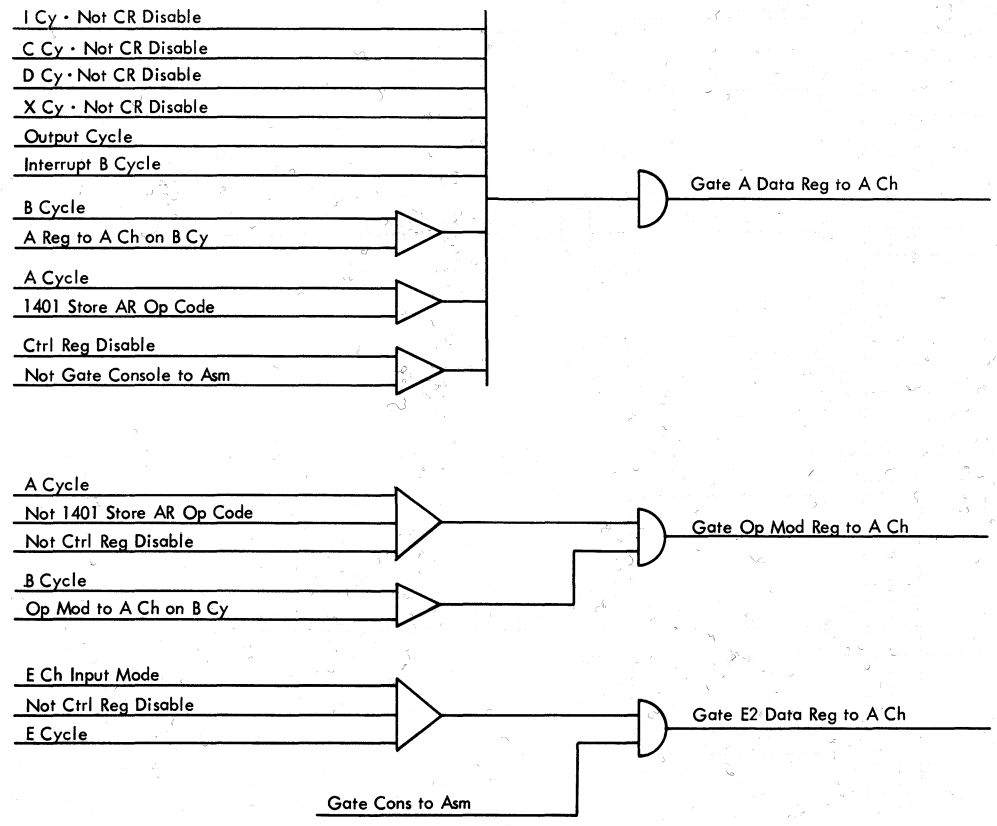


Figure 27. A Channel Gating (15.38.02 & 03)

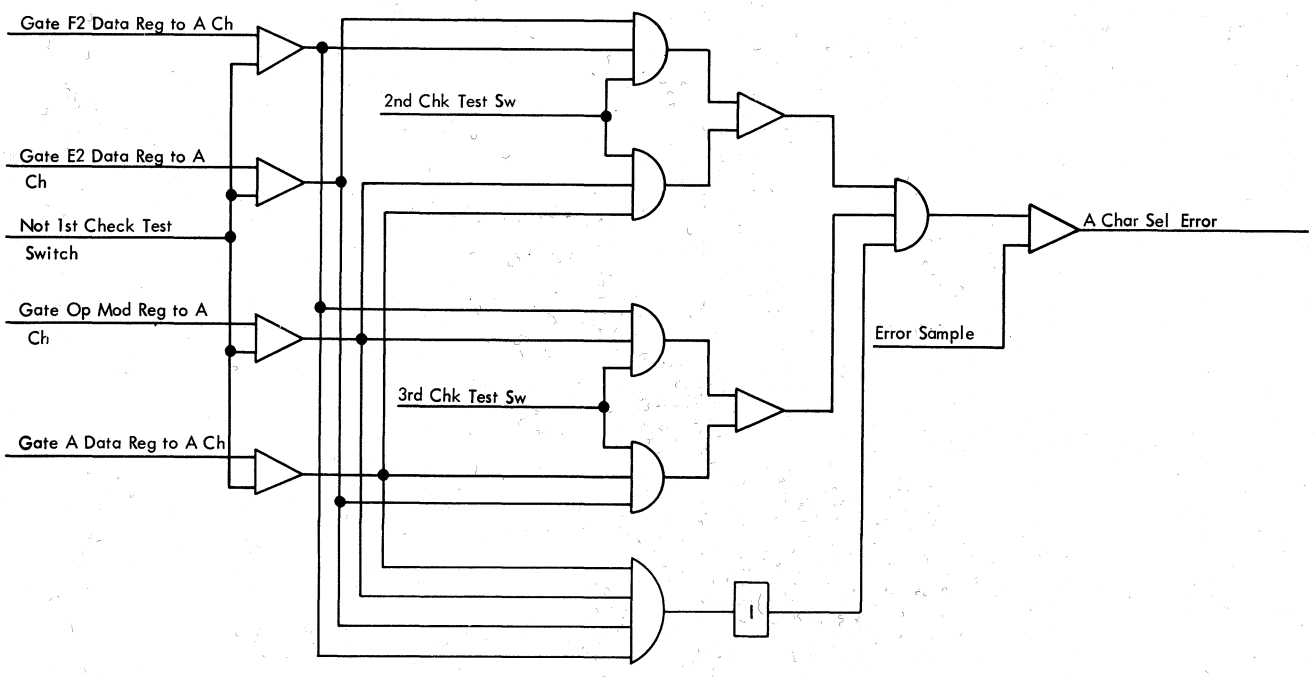


Figure 28. A Character Select Check (18.14.01)

2. The second check test switch forces an error through the upper of the two AND blocks.

3. The third check test switch forces an error through the lower of the two AND blocks.

A Channel Validity Check

The A channel validity check circuit (Figure 29) must be satisfied on every cycle. Refer to "B Channel Validity Check" for a description. The A channel VC circuit uses non-inverting AND circuits. Inverting NAND and AND circuits are used in the B channel VC circuits. Inverting plus OR circuits are used throughout the VC circuits of the B, A, and assembly channels.

Assembly

The assembly unit receives data from five areas of the CPU and combines the data as determined by the operation. The five inputs to the assembly are the A and B channels, the adder, the special-character generator, and the zone adder used for 1401 compatibility.

For example, when two characters are added together in the adder, only the digit portions of the characters are combined. Any zones or word marks that appear over the B field character are read back into storage unaltered. The assembly unit combines the adder output with the B channel zones and word mark, and gates the new B field character back to storage.

During I phase, every instruction-word character that is read out of storage is gated from the B channel to the A data register, then to the A channel. The assembly unit gates the A channel zones, numeric bits, and the word mark onto the assembly channel. When the control unit identifies a character as an address, the assembly channel is gated to the address channel, where the character is set into the desired position of an address register.

For input operations, characters are gated into the E or F data registers from the input machine. The character on the E or F channel is gated to core storage via the A channel, and the assembly unit. For output operations, characters that come from storage on the B channel are gated through the assembly to set the E or F data registers. The E or F channel is gated to the output machine that is selected by the instruction word.

OPERATION

In the assembly (Figures 30 through 36) each character has three parts: The numeric part (1, 2, 4, and 8-bits), the zones (A and B bits), and the word mark. To gate a character through the assembly requires three controls: numeric, zones, and word marks. For example, assume an input operation where the data enters the CPU as an 80-character record. The storage locations into which the record is to be placed contain word marks that define the fields of the record. The assembly is controlled to "use A ch num," "use A ch zones," and "use B ch WM." When a word mark from storage is placed on the B channel, the assembly unit combines it with the input character on the A channel. The A channel char-

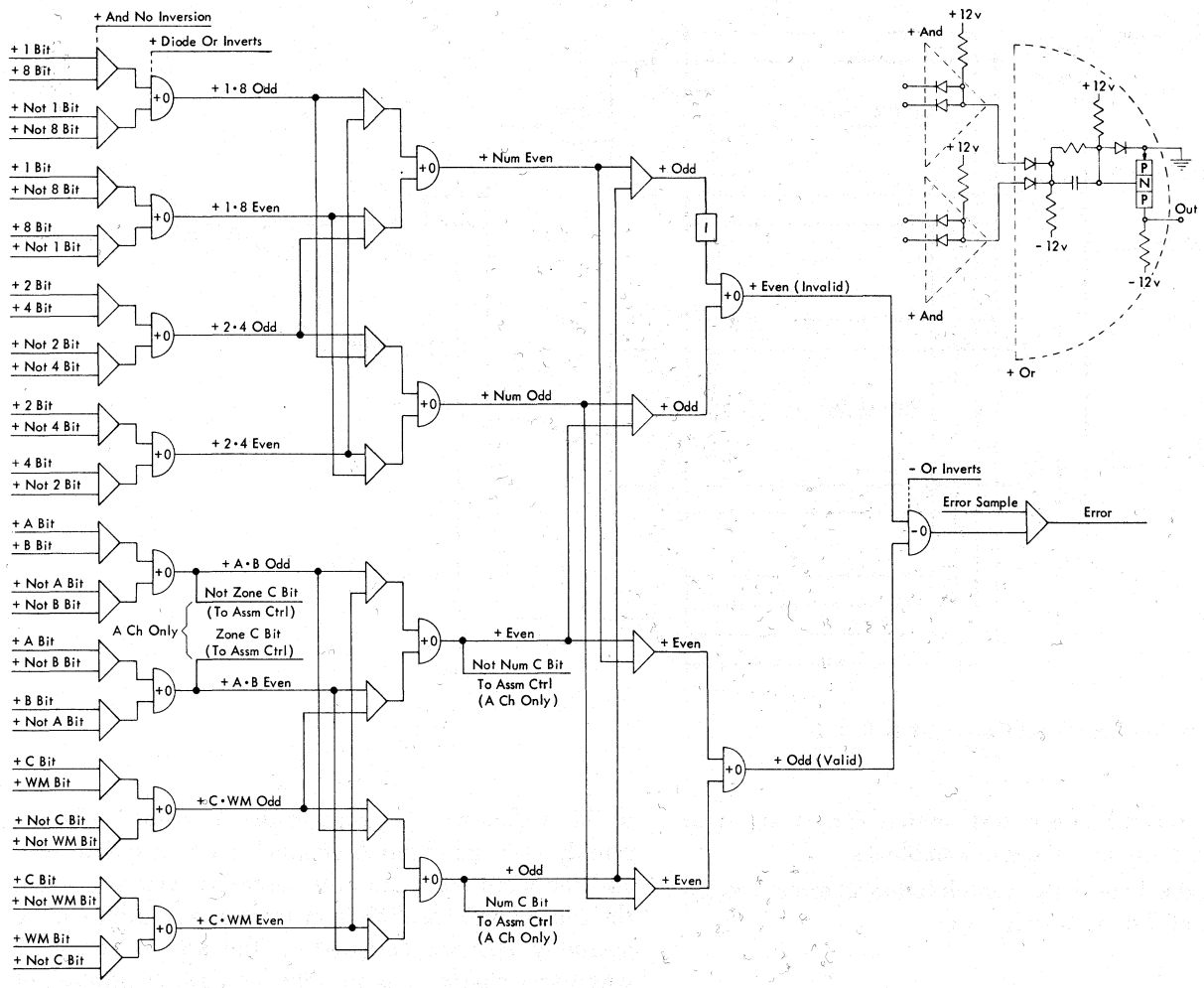


Figure 29. A Channel Validity Check (18.11.01-03)

acter with a word mark is put on the assembly channel where it is read into storage.

During an arithmetic operation, a character can be the combination of the adder ("use adder nu"), the sign stored in the sign latches ("use sign latches"), and a word mark from the B-channel.

To maintain the proper parity of the new character,

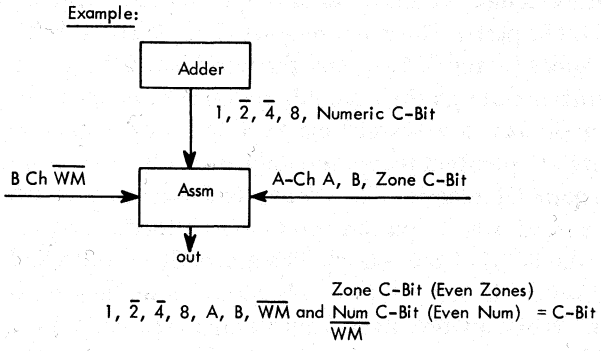


Figure 30. Assembly Operation

the assembly must generate a C bit depending on the number of bits in the three parts of the new character. To assist in determining whether a C bit is required, the numeric and zone portions, at the inputs to the assembly, contain other bits called the numeric C bit and zone C bit. These C bits retain odd parity for their respective portions of the character. For example, the adder output generates a numeric C bit along with the 1 and 8 bits for a nine. The numeric and zone C bits for the A and B channels are developed in their respective validity-check circuits (Figure 24). As assembly controls select the portions of the characters to be gated through the assembly, they also select the numeric and zone C bits that are to be combined with the WM bit to develop an assembly-channel C bit.

ASSEMBLY CONTROLS

The following is a list of assembly controls:

Use B ch WM
Use B ch zones

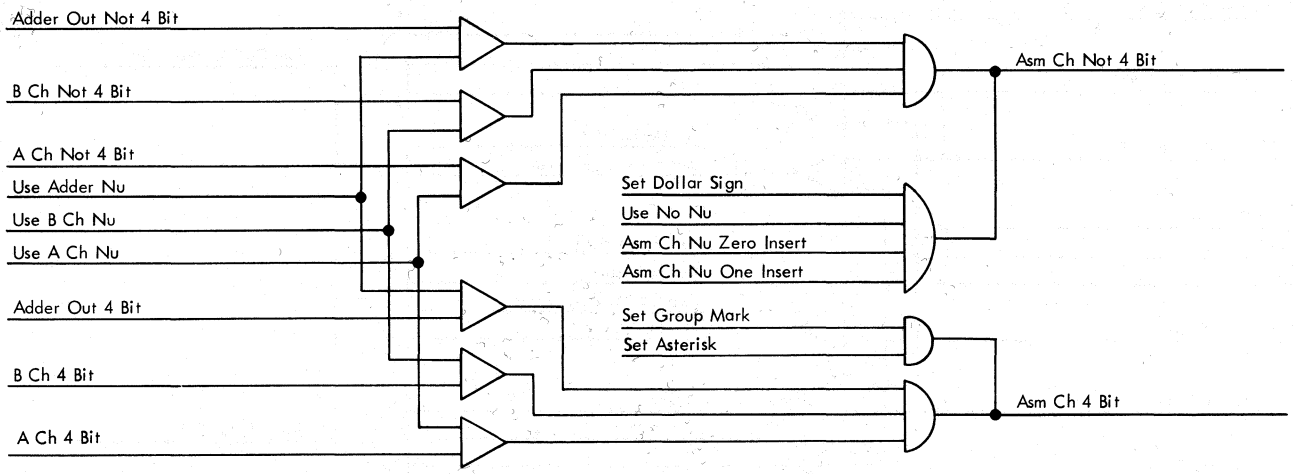


Figure 31. Numeric Assembly 4 Bit (15.50.03)

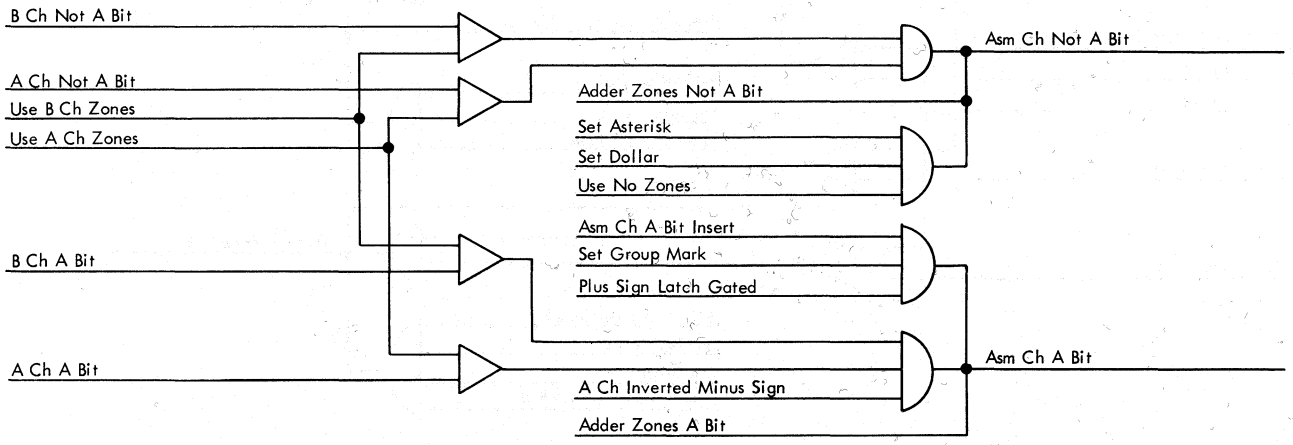


Figure 32. Zone Assembly A Bit (15.50.05)

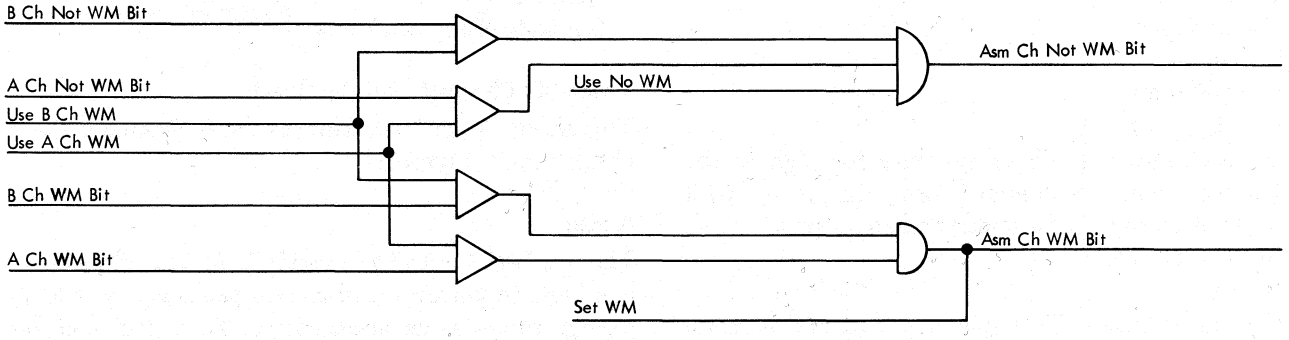


Figure 33. WM Assembly (15.50.08)

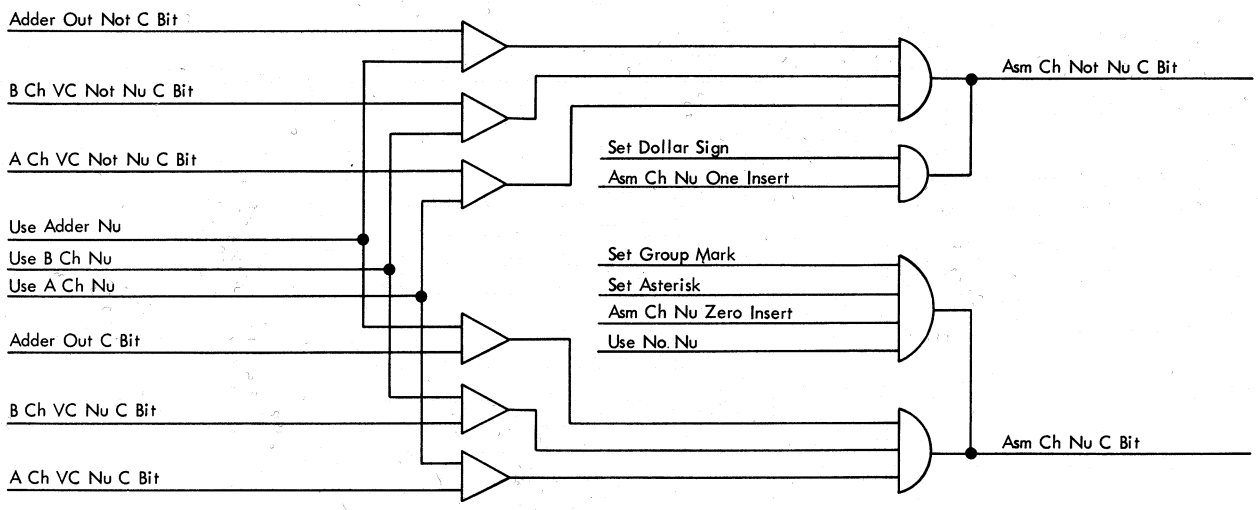


Figure 34. Numeric C Bit Assembly (15.50.09)

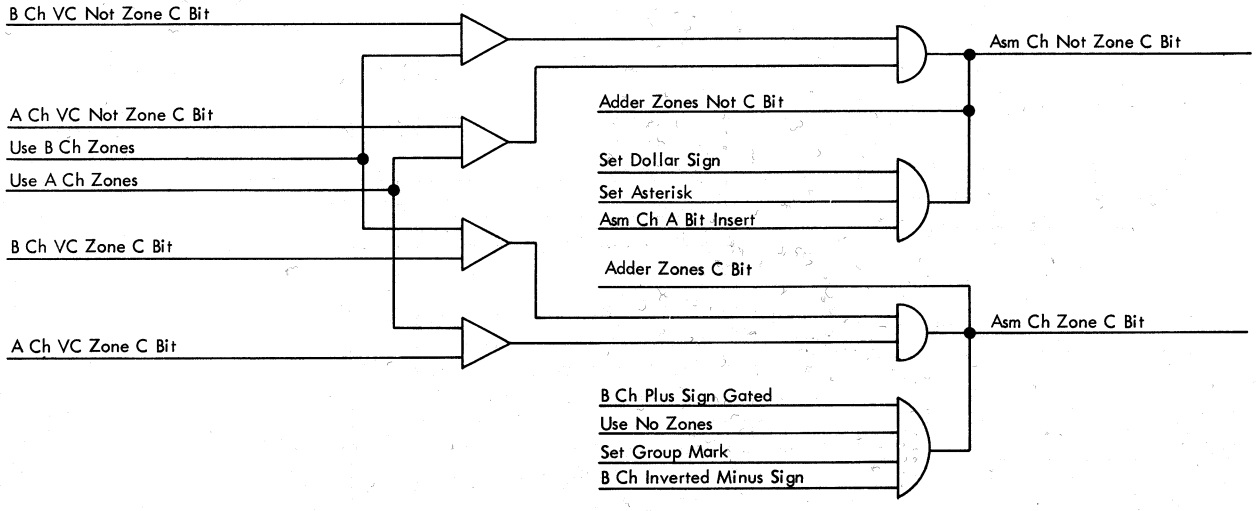


Figure 35. Zone C Bit Assembly (15.50.10)

Use B ch nu
Use A ch WM
Use A ch zones
Use A ch nu
Use no WM
Use no zones
Use no nu
Use adder nu
Use sign latch
Use A ch sign
Use B ch sign
Invert A ch sign
Invert B ch sign
} These generate the sign in the standard form, that is, a BĀ-bit for minus and AB for plus.
Set WM
Use assm 0 insert (This generates 8, 2, and numeric C bits)
Generate num one (This generates 1 not numeric C bit)
Generate A bit (This generates A not zone C bit)
Generate dollar sign
Generate asterisk
Generate group mark WM
} These require no other assembly controls.

Assembly Channel Validity Check

This check circuit is the same as the A channel validity check circuit (Figure 24).

Adder

The IBM 1411 Central Processing Unit uses add-to-storage logic to perform arithmetic operations. A field in storage serves as an accumulator. The adder receives data from the A and B channels and combines them

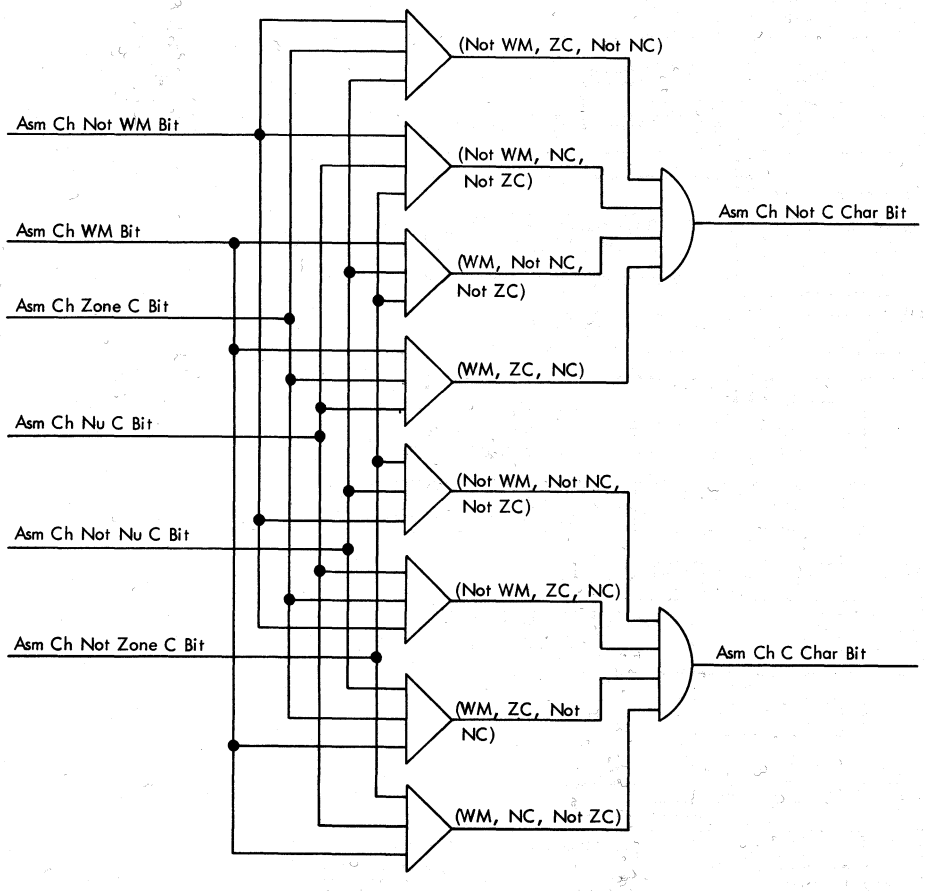


Figure 36. C Bit Assembly (15.50.07)

algebraically. Results are sent to the assembly unit and then back to storage.

To perform its function of combining two factors algebraically, the adder:

1. Analyzes the signs of the two fields (positive or negative).
2. Analyzes the operation code.
3. Translates A and B channel digits from BCD to qui-binary code, true or complement form (Figure 5), as determined by the results of steps 1 and 2.
4. Combines binary portions of the digits along with a "carry in" if required.
5. Combines quinary portions of the digits.
6. Results of the combinations are translated from qui-binary back to BCD.
7. If the results of the combinations produce an adder carry out, the carry latch is set.

Figure 37 shows the adder operation for an add or subtract op code. The type of operation and the signs of the fields determine whether the operation is to be a true add or a complement add (Figure 38).

True/complement controls determine the translation of BCD to qui-binary and control the setting of the carry or no carry latch in the units position. (For further explanation see "Add" or "Subtract" in "Arithmetic Operations.")

The sign is indicated by zone bits over the units position of the factor. The four combinations of these zones are:

12 zone	A and B bits	Positive Sign
11 zone	B bit only	Negative Sign
0 zone	A bit only	Positive Sign
No zones	Neither A nor B bits	Positive Sign

When translating BCD to qui-binary true form, the 1 bit becomes a binary 1 (B1); the 2 bit becomes a quinary 2 (Q2); the 4 bit becomes a quinary 4 (Q4); a 2 and 4 bit becomes a quinary 6 (Q6); an 8 bit becomes a quinary 8 (Q8). Eight bits in special characters are ignored by the adder translator circuits. Zone bits except for the sign position are also ignored. For example, an 8 and 4 bit combination is treated as a 4 bit only; the character F is treated as a 6 only.

Figure 39 shows qui-binary combination of two fields as it is performed by the adder. Figure 40 shows the adder circuits in intermediate level form.

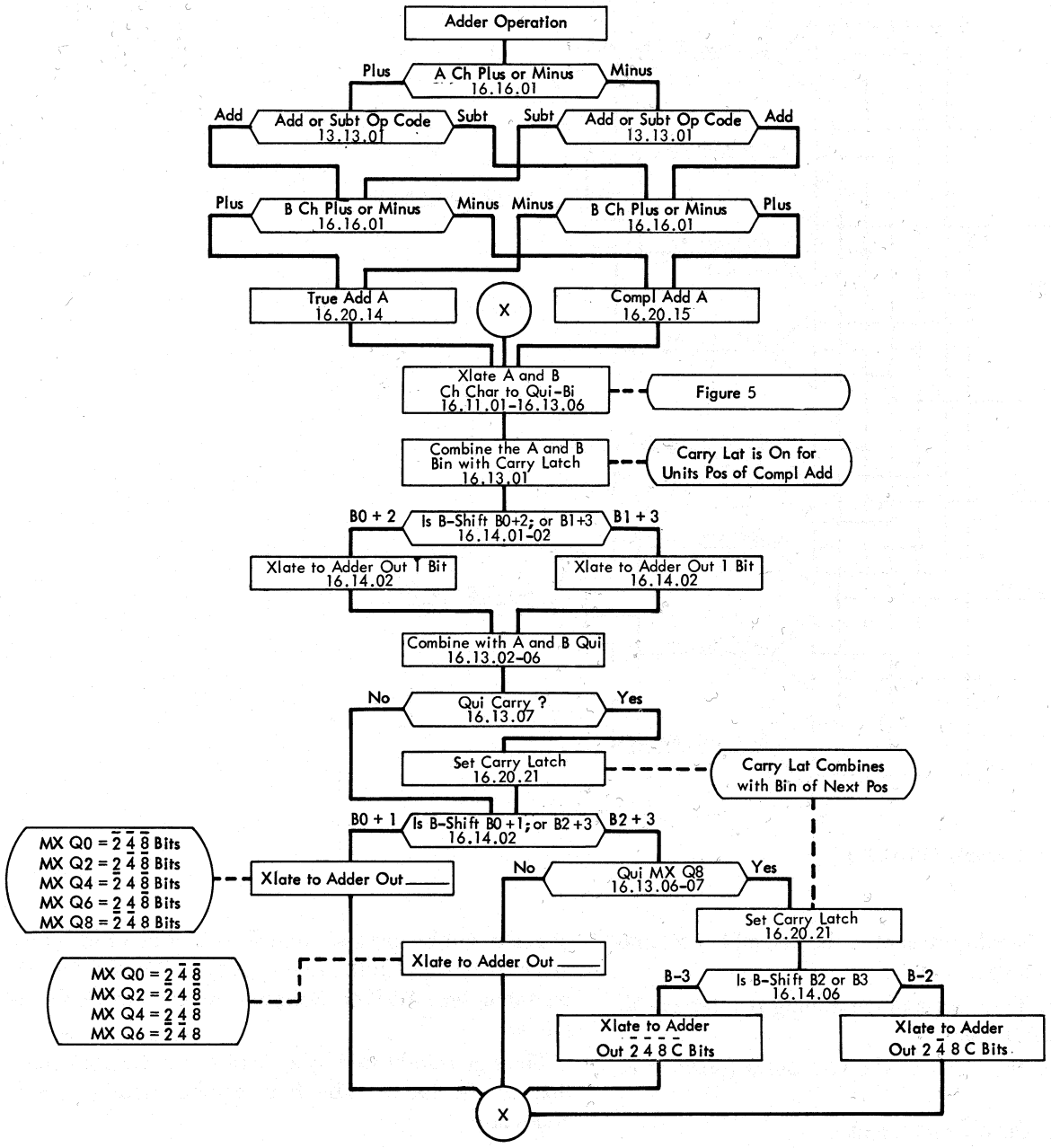


Figure 37. Adder Operation

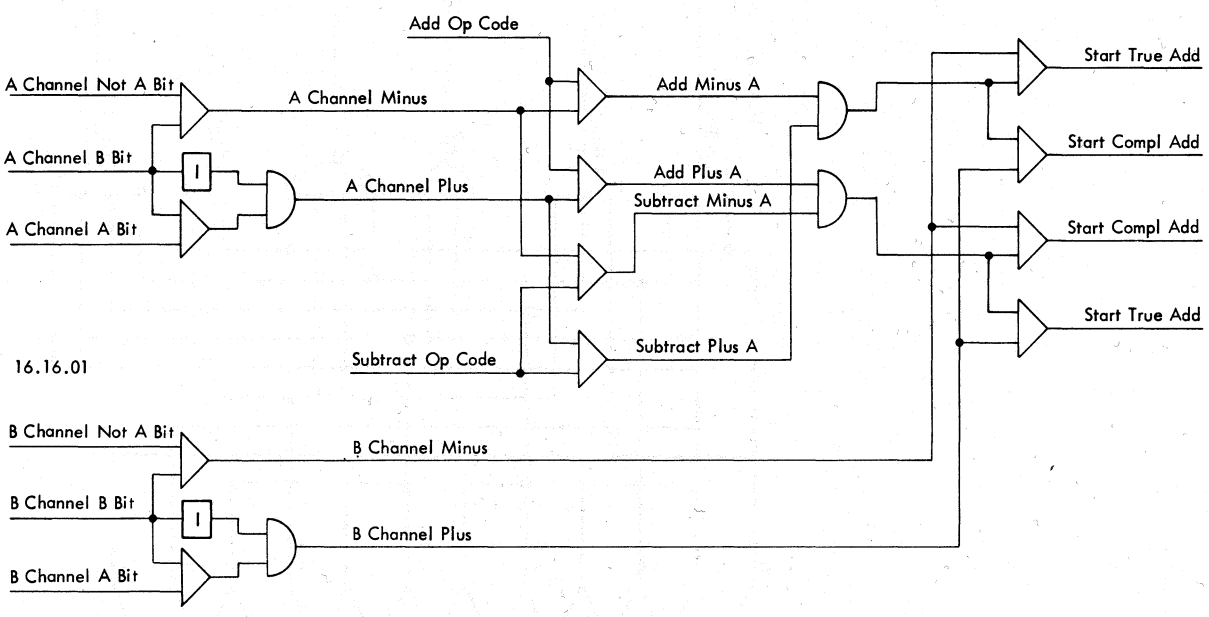


Figure 38. True Complement Controls (16.20.12)

Compare Unit

The compare unit receives information from the A and B channels. The two characters are compared to determine whether the B channel character is greater than (>), equal to (=), or smaller than (<) the A channel character. Figure 41 shows the characters and codes in the collating sequence from low to high character. The result of the compare sets either a high, low, or equal latch that can be tested by later program instruction.

OPERATION

The two characters are fed to both the compare and adder units. In the compare unit, the characters are translated into one of the three groups: alphameric (AN), special character (SC), or non-numeric (NN) (Figure 41). Also, in the compare unit, the zones are compared. In the adder, the digits are combined to determine whether the B channel digit is greater than, equal to, or smaller than the A channel digit.

The compare unit first analyzes the characters to place them in groups. For example, if one character is AN and the other is either NN or SC, the AN character is high regardless of the zones or digits involved.

If the groups alone do not reveal the relationship of the two characters, the comparison of the zones is analyzed.

If the relationship of the character is still unknown, the result of the adder comparison must be considered.

The adder compares the two digits by subtracting the A channel digit from the B channel digit.

A carry or no-carry is developed when the quinary portions of the A and B channel characters are combined, except when the result is a quinary 8. If a carry is called for, it signals that the B channel character is larger than the A channel character. Example (B character, 5; A character, 3):

B	Q4	B1	
A	Q6	B0	(9's complement)
		Carry	(1st cycle of the CA forces a carry)
	Q0	B2	

Carry signifies B > A

If no-carry is brought up, the B channel character is smaller than the A character. Example (B character, 3; A character, 7):

B=	Q2	B1
A=	Q2	B0
		Carry
	Q4	B2

No-Carry signifies B < A

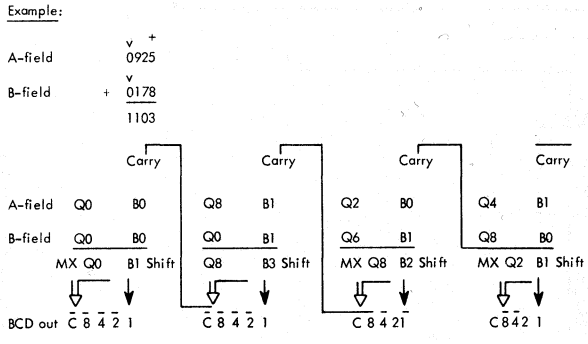


Figure 39. Qui-Binary Combination

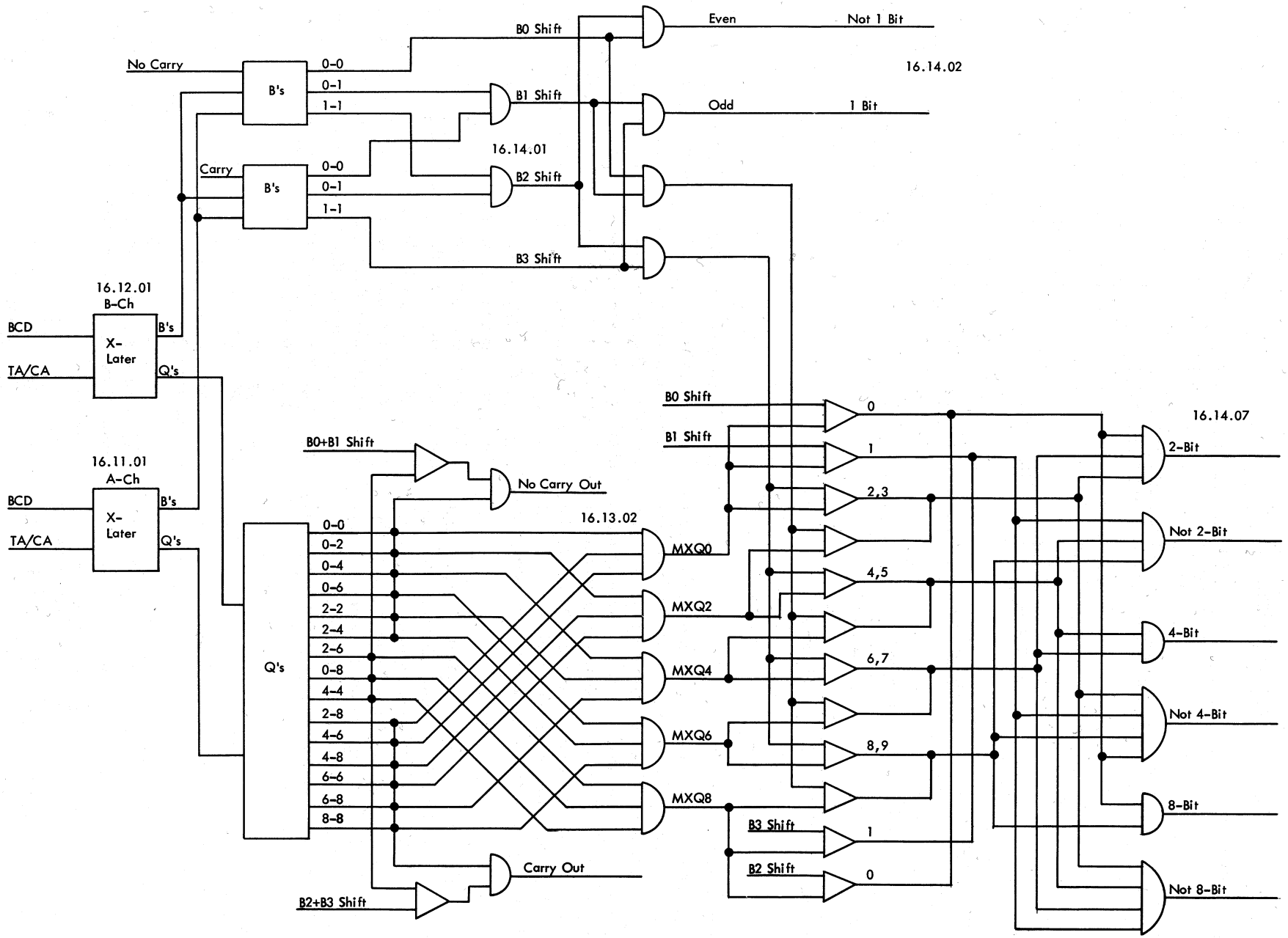


Figure 40. 1410 Adder

	1 Collating Number	2 Graphics	3 Card Code			4 BCD Code						5
						B	A	8	4	2	1	
NN	00	Blank	No Punches			No Bits						
	01	.	12	3	8	B	A	8		2	1	
	02	日)	12	4	8	B	A	8	4			
SC	03	[	12	5	8	B	A	8	4		1	
	04	<	12	6	8	B	A	8	4	2		
	05	‡	12	7	8	B	A	8	4	2	1	GM
NN	06	& +	12			B	A					
	07	s	11	3	8	B		8		2	1	
	08	*	11	4	8	B		8	4			
SC	09	]	11	5	8	B		8	4		1	
	10	;	11	6	8	B		8	4	2		
	11	Δ	11	7	8	B		8	4	2	1	MC
NN	12	-	11			B						
	13	/	0	1			A				1	
	14	,	0	3	8		A	8		2	1	
SC	15	% (	0	4	8		A	8	4			
	16	Y	0	5	8		A	8	4		1	WS
	17	\	0	6	8		A	8	4	2		
	18	⋕	0	7	8		A	8	4	2	1	SM
NN	19	↑		2	8		A					SB
	20	# =		3	8			8		2	1	
SC	21	@ '		4	8			8	4			
	22	:		5	8			8	4		1	
	23	>		6	8			8	4	2		
	24	✓		7	8			8	4	2	1	TM
	25	?	12	0		B	A	8		2		PZ
	26	A	12	1		B	A				1	
	27	B	12	2		B	A			2		
	28	C	12	3		B	A			2	1	
	29	D	12	4		B	A		4			
	30	E	12	5		B	A		4		1	
	31	F	12	6		B	A		4	2		
	32	G	12	7		B	A		4	2	1	
	33	H	12	8		B	A	8				
	34	I	12	9		B	A	8			1	
	35	!	11	0		B		8		2		MZ
	36	J	11	1		B					1	
	37	K	11	2		B				2		
	38	L	11	3		B				2	1	
	39	M	11	4		B			4			
	40	N	11	5		B			4		1	
	41	O	11	6		B			4	2		
	42	P	11	7		B			4	2	1	
	43	Q	11	8		B		8				
AN	44	R	11	9		B		8			1	
	45	‡	0	2	8		A	8		2		RM
	46	S	0	2			A			2		
	47	T	0	3			A			2	1	
	48	U	0	4			A		4			
	49	V	0	5			A		4		1	
	50	W	0	6			A		4	2		
	51	X	0	7			A		4	2	1	
	52	Y	0	8			A	8				
	53	Z	0	9			A	8			1	
	54	0		0				8		2		
	55	1		1							1	
	56	2		2						2		
	57	3		3						2	1	
	58	4		4					4			
	59	5		5					4		1	
	60	6		6					4	2		
	61	7		7					4	2	1	
	62	8		8				8				
	63	9		9				8			1	

Figure 41. Collating Sequence

When the quinary result is a Q8, the combined binary portion of the character determines the result of the compare. Example (B character, 6; A character, 6):

B=	Q6	B0
A=	Q2	B1
		Carry
	Q8	B2 signifies A = B

Example (B character, 8; A character, 9):

B=	Q8	B0
A=	Q0	B0
		Carry
	Q8	B1 signifies B < A

Example (B character, 5; A character, 1):

B=	Q4	B1
A=	Q4	B1
		Carry
	Q8	B3 signifies B > A

Special characters 8-3 through 8-7 are added as a 3 through 7 respectively.

To determine whether the compare unit operates correctly, select two characters and follow them through the flow chart (Figure 42). The translation of the A field character into the three groups is the same as shown for the B channel character.

Instruction Read-Out

Instruction read-out and indexing are the two divisions of the instruction phase or I phase of an operation. The indexing operation interrupts instruction read-out, changes the contents of one of the address registers, then allows instruction read-out to continue. A detailed discussion of indexing follows the description of the instruction read-out operation.

During instruction read-out, characters in the instruction word are set into the proper registers as determined by the decoding of the first character in the word which is the operation code. Operation decode circuits bring up common op code grouping lines which control the rest of instruction read-out and the execution of the operation.

Operating Principles

1. The first character read out of storage must have a word mark (WM) since this character should be an op code.

2. The op code character must be a valid 1410 op code or an instruction check will stop the CPU.

3. If an input-output op code is decoded, the X field characters must be gated to the I-O select registers.

4. Common op code grouping lines brought up by the op decode circuits determine whether the first address reads into the AAR, BAR, CAR and DAR; the AAR and CAR only; or the CAR only.

5. There must not be any zones over the ten-thousands, thousands, or units positions of an address or an address check stops the CPU.

6. Zones over the hundreds and tens position of an address are set into the index tag latches to control the indexing operation. (See "Indexing.")

7. Each instruction word must be one of the correct lengths for that operation code or an instruction check stops the CPU.

OPERATION

The instruction read-out operation (Figures 43 and 44) is normally initiated by the last execute cycle of the previous operation. Last execute cycle brings up I cycle control and I ring control at LGZ (Figure 45). Instruc-

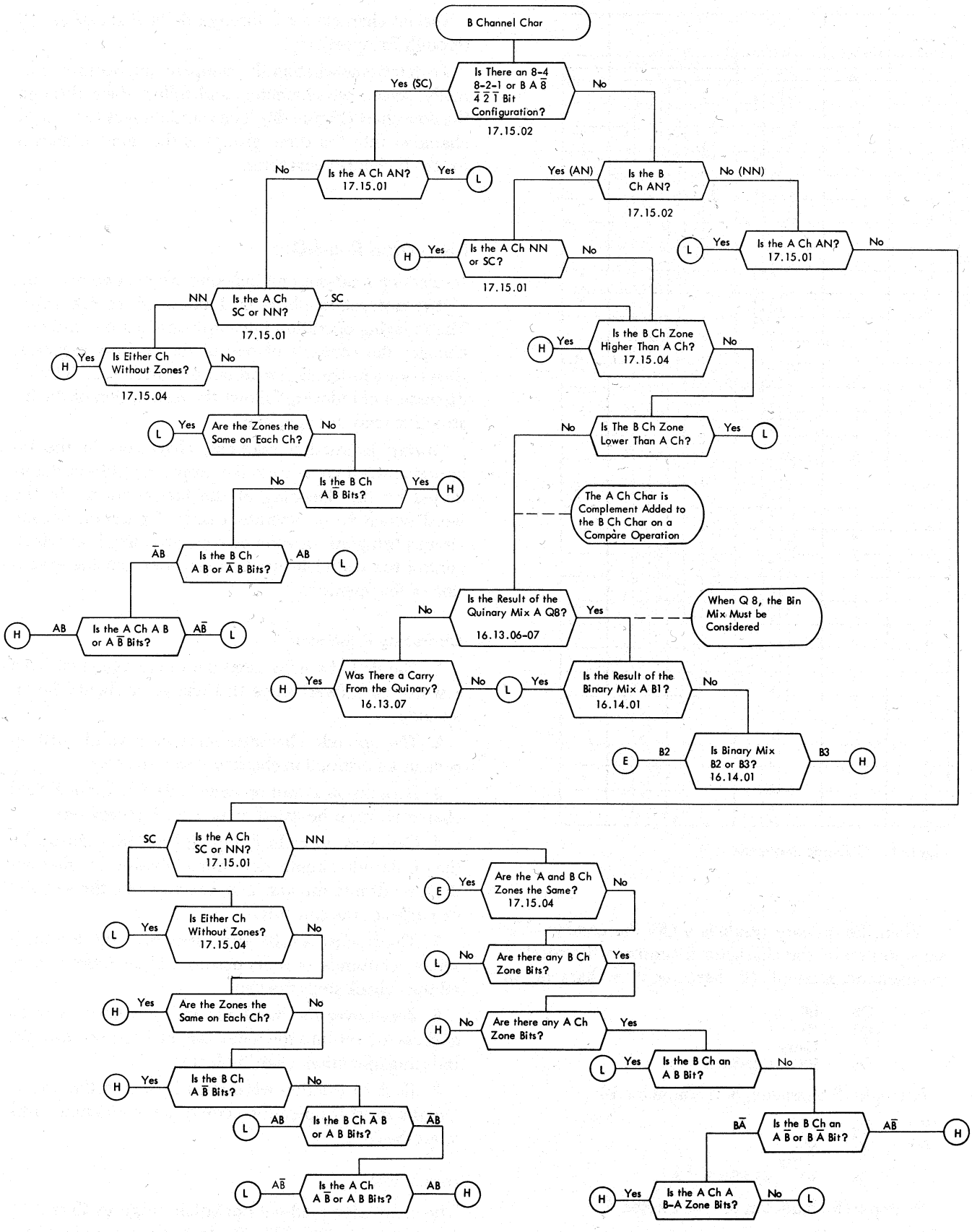


Figure 42. Compare Unit Operation (17.15.01-07)

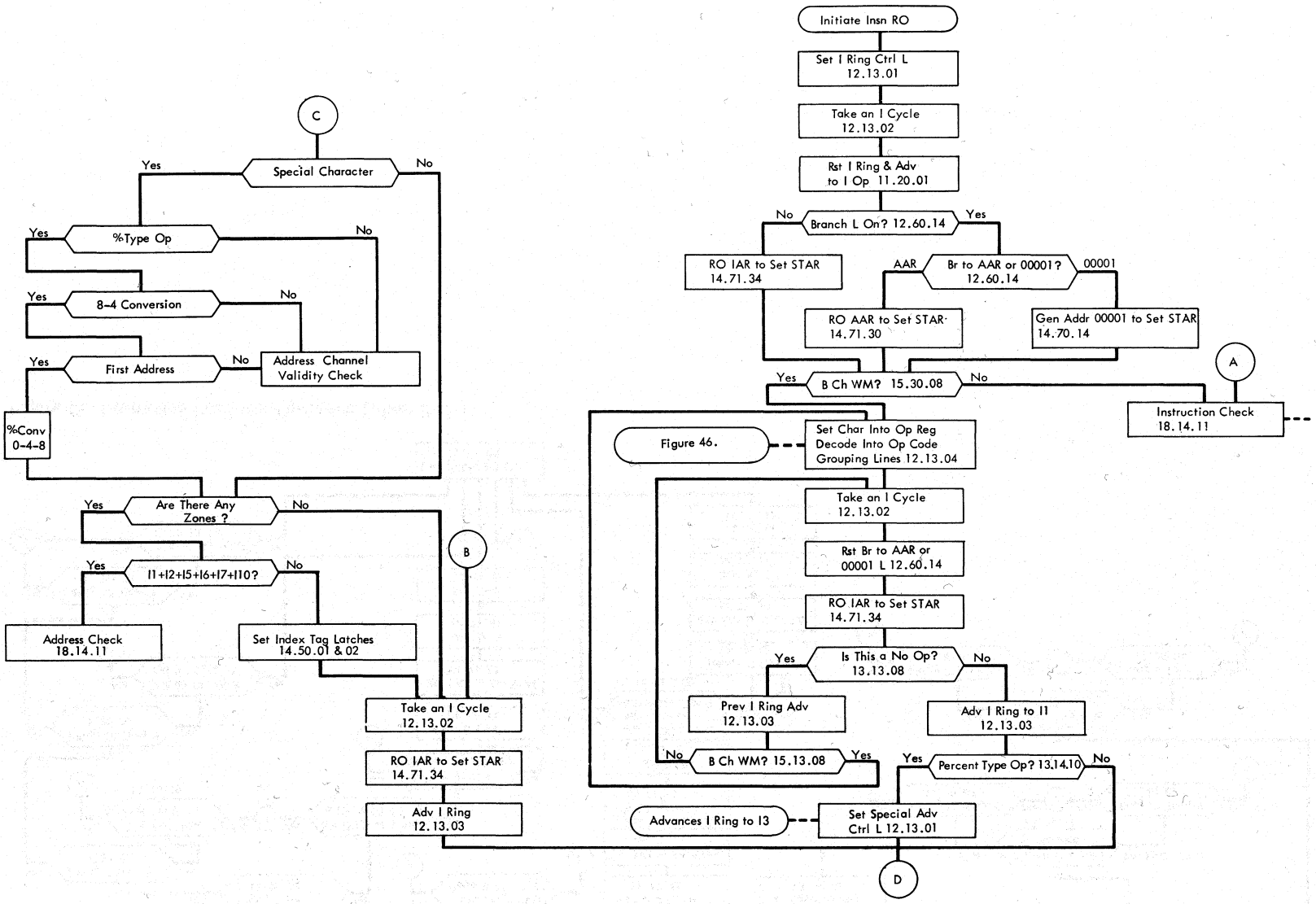


Figure 43. Instruction Read-Out Operation (Sheet 1 of 3)

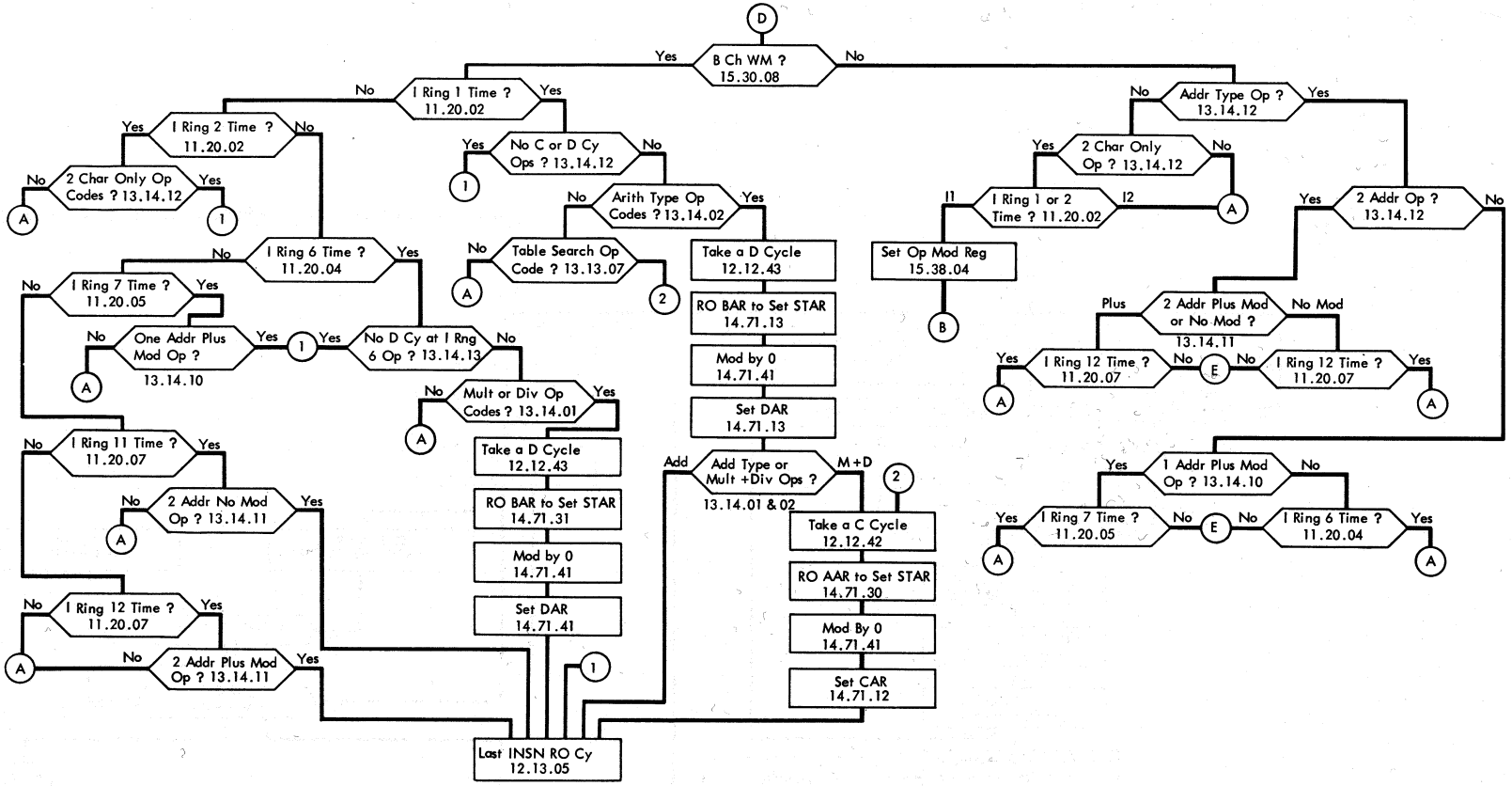


Figure 43. Instruction Read-Out Operation (Sheet 2 of 3)

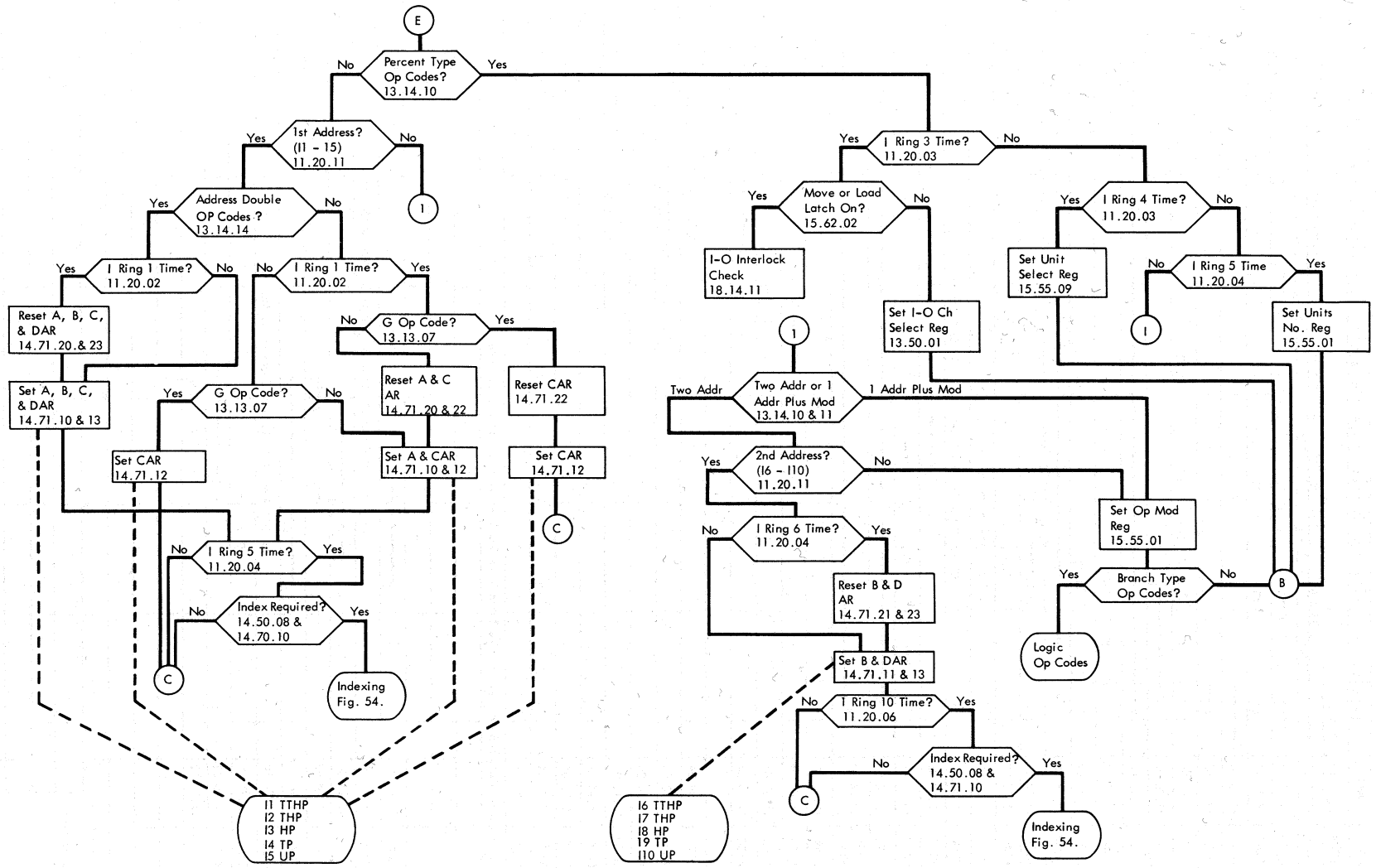


Figure 43. Instruction Read-Out Operation (Sheet 3 of 3)

Figure 44. Instruction Read-Out Timings

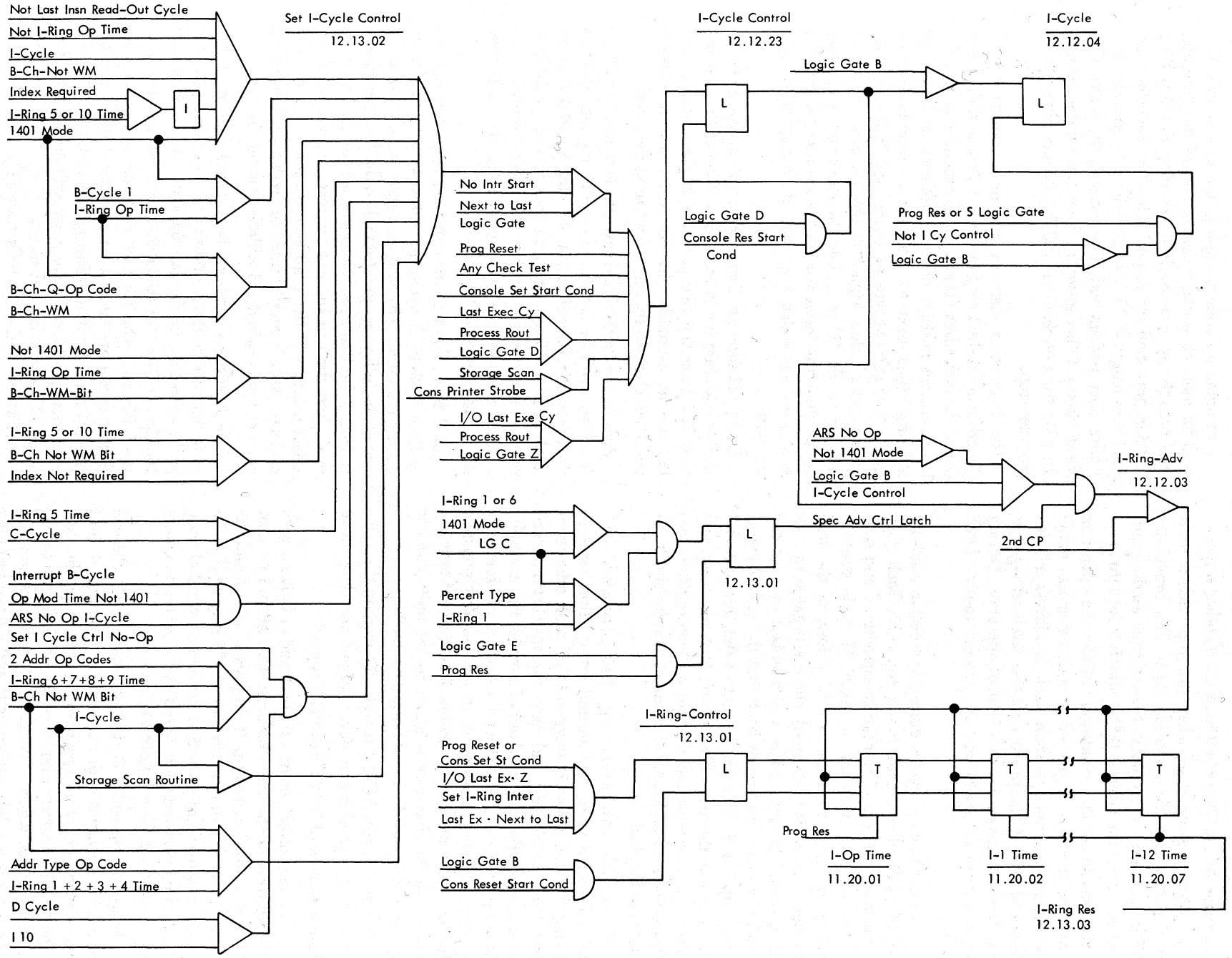


Figure 45. I Phase Latches

tion read-out can also be initiated in two other ways:

1. After program reset, when the stop latch is reset by the start key, the operation starts. The branch-to-00001 latch (reset on) blocks the IAR from reading out, and generates the address 00001 which is set into STAR.

2. Console set start condition initiates the operation when the start key is pressed to start I-E or run mode following a manual operation, such as address set, display and alter. (The process routine latch off signifies that the last operation was a manual operation. During I-E or run mode operation, the process routine latch is on.)

I Cycles: Storage cycles during instruction read-out are 4.5 (4.0) microseconds long (stop at F). Each character that reads out of storage is regenerated and storage is scanned from left to right. "I cycle control" brings up "addr mod set to +1." (None of the scan latches is on during I cycles.) The IAR is gated to STAR (2CP, LGA). The STAR address is modified by plus one from LGB to LGF and reads back into the IAR. "I cycle" brings up "sw B ch to A reg," "gate A data reg to A ch," and controls the assembly to "use A ch nu, zones and WM." Characters are gated to the address registers and the A channel and assembly channel validity check circuits are satisfied.

I Ring: The instruction ring (I ring) consists of 13 triggers called I ring op time and I ring 1 time through I ring 12 time. These 13 triggers "and" with other control lines to identify and gate the instruction word characters as they are read out of storage. For example, at I ring 5 time the character read out of storage is gated to the units position of specific address registers for not percent-type op codes. For percent-type op codes, the I5 character is gated to the units number register of one of the input-output channels.

Instruction Read-Out Example: To explain the operation of a typical instruction read-out, the data move instruction word $\overset{v}{D}$ 12345 67890 T is used.

"I cycle control" brings up ROIAR and STAR is set with the address of the first character (D) at 2nd CP LGA. "I-ring control" brings up "I ring reset" at LGB and the I ring is set to I ring op time by the "I ring adv" pulse at 2CP LGB to identify the first instruction word character as the operation code. The I cycle latch also comes up at LGB time. (See Figure 44.)

When the op code "D" is gated onto the B channel around LGD (varies with memory clock timing) it must have a WM bit or an instruction check stops the CPU. The WM is necessary also to set the op code into the op register at LGE where it is decoded to determine if the character is a valid 1410 op code and if so to bring up the common op code grouping lines associated with it (Figure 46).

A common op code grouping line is a control line used for more than one op code. One of the grouping lines brought up as a result of decoding the D will be "2 addr plus mod op codes." This line identifies the maximum length of 12 characters for a D op code. The 2 addr plus mod op code line controls the instruction check circuit. Other grouping lines control the remainder of instruction read-out and the execute-phase of the program step.

The instruction read-out operation continues with the advance of the I ring to I ring 1 time and the read-out of the next instruction word character which is the ten-thousands position of the A address. At 1st CP LGB of I ring 1 time the AAR's and CAR's are reset under control of "not percent type op codes" and "not addr double op codes." (See Figure 43, sheet 3 of 3.) At LGA of this I cycle the "1" is set into the AAR's and CAR's. Also at LGA time, the index tag latches are reset in case the A address has index tags over its hundreds or tens position.

During I2 time the thousands position character "2" will be read into the thousands position of the AAR and CAR. For these first two positions of the address, zone bits on the assembly channel will cause an address check which stops the CPU with a program error.

Zone bits over the hundreds and tens position of the A address will be set into the index tag latches from the assembly channel at LGA of I ring 3 and 4 time respectively. At I5 time the units position of the address reads out of storage and into the units position of the AAR and CAR. No zone bits should be present at I5 time or an address check stops the CPU.

At I5 time, if any of the index tag latches are on (set at I3 or I4 time) X cycles are taken to perform the indexing operation. The I5 time trigger stays on until the end of the indexing operation when the I ring advances to I6 and the B address starts to read out. At 1st CP LGB of I6 time, the BAR and DAR are reset and the ten thousands position of the B address (6) reads into the BAR and DAR. Also during I6 time, the index tag latches are reset at LGA in case the B address is to be indexed.

The B address read-out is performed in much the same manner as the A address read-out using the BAR and DAR instead of the AAR and CAR. At LGD of I8 time the op-modifier-register latches are reset all off except the C bit latch which is reset on to maintain parity. Indexing cycles are taken after I10 time if index tags are present over the B address digits. During I11 time the operation modifier register is set with the op mod character (T) which is used to control the operation (see "Data Move" under "1410 Operations").

After the last instruction word character reads out, one additional I cycle is taken to read out the next

1410 OP CODES

	COMMON OP CODE GROUPING LINES	?	!	A	S	@	%	E	Z	C	W	V	/	.	,	¤	U	D	J	B	R	X	G	T	M	L	K	F	N
Instruction	Percent Type Op Codes																X								X	X			
Read-Out	Not Percent Type Op Codes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X	X	X		X					
	Addr Dbl Op Codes	X	X	X	X								X		X	X			X		X	X							
	Not Addr Dbl Op Codes					X	X	X	X	X	X	X		X			X	X		X			X	X	X	X	X	X	
	1 Addr Plus Mod Op Codes																X		X		X	X	X						
	2 Addr No Mod Op Codes	X	X	X	X	X	X	X	X	X			X		X	X													
	2 Addr Plus Mod Op Codes										X	X						X		X				X	X	X			
	2 Address Op Codes	X	X	X	X	X	X	X	X	X	X	X	X		X	X		X		X				X	X	X			
	Addr Type Op Codes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X			
	2 Char Only Op Codes																										X	X	
	C Cycle Op Codes					X	X																	X					
	No C or D Cy Op Codes							X	X	X	X	X	X	X	X	X		X	X	X									
	No D Cy at I Ring 6 Ops	X	X	X	X			X	X	X	X	X	X	X	X	X		X		X				X					
	No Index On 1st Addr Ops																X						X		X	X			
Operational	Reset Type Op Codes	X	X																										
	Add or Subt Op Codes			X	X																								
	Mpy or Div Op Codes					X	X																						
	Add Type Op Codes	X	X	X	X																								
	Arith Type Op Codes	X	X	X	X	X	X																						
	E or Z Op Codes							X	X																				
	Compare Type Op Codes									X										X				X					
	Branch Type Op Codes *										X	X	X	X					X	X	X	X							
	No Branch Op Codes	X	X	X	X	X	X	X	X	X					X	X	X	X					X	X	X	X	X	X	
	Word Mark Op Codes														X	X													
	M or L Op Codes																								X	X			
Control	1st Scan First Op Codes	X	X	X	X	X	X	X	X	X	X	X	X		X	X				X			X	X					
	A Cy First Op Codes	X	X	X	X	X	X	X	X	X					X	X		X						X					
	Std A Cycle Op Codes	X	X	X	X	X	X	X	X	X								X						X					
	B Cy First Op Codes										X	X	X							X									
	A Reg to A Ch On B Cy Ops	X	X	X	X	X	X	X	X	X			X	X	X	X		X						X					
	Op Mod to A Ch On B Cy Ops										X	X					X		X	X	X	X					X	X	
	Load Mem On B Cy Op Codes	X	X	X	X	X	X	X	X									X											
	Rgen Mem On B Cy Op Codes									X	X	X		X					X	X	X	X		X			X	X	
	Stop at F on B Cy Op Codes	#	#			#	#						X	X				#	X		X	X							
	Stop at H on B Cy Ops										X	X								X									
	Stop at J on B Cy Op Codes	X	X			X	X	X	X									X											
	RO B AR On Scan B Cy Ops							X	X	X	X	X	X	X	X	X		X	X	X	X	X		X					
	RO A AR On A Cy Ops	X	X	X	X			X	X	X					X	X		X											

* Not a Line Name, a Grouping Only

\# Indicates Accelerator Feature Timing

Figure 46. IBM 1410 Common Op Code Grouping Lines (13.14.01-14)

character in storage ("addr mod set to +1" is still up at I11 time). During this last I cycle (last instruction read-out cycle, LIROC) there must be a B ch WM if the instruction is the correct length. Because this character is usually the op code of the next-sequential instruction (NSI), it must be read out during I op time of the NSI read-out.

As this character with a WM is read out during LIROC, the address in STAR is being modified by plus one to be read into the IAR (normal operation). When the WM identifies this cycle as the last I cycle (around LGD), the gate to set the IAR from the address channel is dropped and the IAR is reset at 1st CP, LGF. "Set mem AR to IAR" is brought up at LGF to gate the address of the NSI (the address of the op code) which is still in STAR, to the IAR.

In this manner, the address of the NSI is gated to the IAR during LIROC. When I phase is required for the NSI, the IAR already contains the address of the NSI and instruction read-out and execution continue through the program routine.

To satisfy the address-channel-validity-check circuits during I phase, zeros must be inserted on the address channel at LGA of the three cycles when no instruction-word character is gated to the address channel. These three times are I op time, op mod character time and last-instruction-read-out cycle. All address-position characters and X-control field characters are gated onto the address channel. X control field characters with 8 and 4 bit combinations are translated to a 4; zone bits are ignored by the translator.

COMMON OP-CODE GROUPING LINES

Common op-code grouping lines consist of three groups: instruction read-out, operational, and control (Figure 46). The instruction read-out group controls the remainder of I phase. E phase is controlled by the operational and control groups.

If the op decode is a no op, none of the common op-code grouping lines is brought up, the I ring is not advanced, and I cycle control causes the storage to read out characters until another character with a WM is detected. The B channel WM sets this character into the op register where it should be decoded as a valid op code or an instruction check will stop the CPU. The instruction read-out operation continues with the advance of the I ring to I ring 1 time, and the next character is read out of storage.

If the op decode is neither an N nor a G, one of three common op-code grouping lines must come up.

Percent-Type Op Codes: Input-output operations are controlled by percent-type op codes. Move, load, and the unit control op codes make up this group. Move and load op codes also bring up "2 addr plus mod op code" while the U op code brings up "one address plus mod op codes."

A three position field, called the X control field, follows the op code character in percent-type instruction words. Characters in this X control field control the selection of: the I-O channel (E or F), the type of I-O unit (tape, printer, etc.), and the specific I-O unit (tape unit number six, for example).

The three-position X control field replaces what normally would be a five-position address in the instruction word of not percent type op codes. To account for the two positions not used, the percent type op code line causes two quick advances of the I ring during the second I cycle (Figure 43). "I ring 1 time" and "percent type op code" bring up the special advance control latch which gates an additional I-ring advance at 2nd CP LGC and at 2nd CP LGD. I ring 3 time comes up at 2nd CP of LGD of this second I cycle.

The character read out at I-3 time is the I-O channel-select character which is set into the I-O channel select register at LGE. During I4 time, the unit-select character reads out of storage and is set into the E or F channel units-select register depending on the contents of I-O channel-select register. At I5 time the character is set into the E or F channel units number register.

Because of the special advance of the I ring, the characters gated at I6 through I10 time for two address plus mod op codes (M or L) are the second address characters. For one address plus mod op codes (U), the character gated at I6 time is the op mod character. Thus, normal instruction read-out gating is used from I ring 6 time.

Not Percent-Type Op Codes: Only these op codes (except R and X) can be chained. Three more common op code grouping lines identify the maximum length of these op codes. "One address plus mod op codes, 2 addr no mod op codes, and 2 addr plus mod op codes" insure that there are word marks at I7, I11, or I12 time, respectively.

Two-Character-Only Op Codes: For two-character-only op codes (K and F), the character at I ring 1 time must be the op modifier, and it must not have a word mark over it or an instruction check results. At I2 time, the next character reads out to insure that there is a word mark over it.

INSTRUCTION READ-OUT CIRCUIT DESCRIPTION

1. Initiate instruction read-out; read out op code character.

SIGNAL	CONTROL	LOGIC
Set I Cycle Ctrl	Last Execute Cycle, NLLG	12.03.02
I Cycle Ctrl	Set I Cycle Ctrl, NLLG	12.12.23
RO IAR	I Cycle Ctrl, Special LGA	14.71.34
Set Mem AR Gated	LGA or LGR, 2nd CP	14.17.16

SIGNAL	CONTROL	LOGIC

2. Start I ring at I op time.

I Ring Ctrl	Last Execute Cycle and Next to Last LG	12.13.01
I Ring Reset	I Ring Ctrl, LGB	12.13.03
I Ring Adv	I Cycle Ctrl, LGB, 2nd CP	12.13.03
I Ring Op Time	I Ring Ctrl, I Ring Adv	11.20.01

3. Set op code into op register.

I Cycle	I Cycle Ctrl, LGB	12.12.04
Set Op Register	I Cycle, I Ring Op Time, B Ch WM	12.13.04

4. Advance I ring to I1 time.

Set I Cycle Ctrl	I Ring Op Time, B Ch WM	12.13.02
I Cycle Ctrl	Set I Cycle Ctrl, NLLG	12.12.23
I Ring Adv	I Cycle Ctrl, LGB, 2nd CP	12.13.03
I Ring 1 Time	I Ring Op Time, 1 Ring Adv	11.20.02

5. Read out next character.

RO IAR	I Cycle Ctrl, Special LGA	14.71.34
Set Mem AR Gated	LGA, 2nd CP	14.17.16

Percent Type Op Codes (U, M, L 13.14.10)

6. Advance I ring to I3 time.

Spl Adv Ctrl Lat	%Type Op Codes,I1, LGC	12.13.01
I Ring Adv	Spl Adv Ctrl Lat, 2nd CP	12.13.03
Spl Adv Ctrl Lat "Off"	LGE	12.13.01

7. Set I-O channel select register.

Set I-O Ch Sel Reg	I Cycle, I3 % Type Op, LGE, B Ch 8, 2, 4, 1	13.50.01

Sets %, @, □, or * Latch

8. Advance I ring to I4 time.

Set I Cycle Ctrl	Addr Type Op Code, I3, Not B Ch WM	12.13.02
I Cycle Ctrl	Set 1 Cycle Ctrl, NLLG	12.12.23
I Ring Adv	I Cycle Ctrl, LGB, 2nd CP	

9. Read out next character.

RO IAR	I Cycle Ctrl, Special LGA	14.71.34
Set Mem AR Gated	LGA or R, 2nd CP	14.17.16

10. Set character into units select register.

Sw B Ch to A Reg	I Cycle, LGD, 2nd CP	15.38.01
Gate A Data Reg to A Ch	I Cycle	15.38.02
Use A Ch Nu	I Cycle	15.49.03
Use A Ch Zones	I Cycle	15.49.03
Set E Ch Unit Sel Reg	% or @, I4, Last LG	15.55.09

SIGNAL	CONTROL	LOGIC

11. Advance I ring to I5 time.

Set Cycle Ctrl	Addr Type Op Code, I3, Not B Ch WM	12.13.02
I Cycle Ctrl	Set I Cycle Ctrl, NLLG	12.12.23
I Ring Adv	I Cycle Ctrl, LGB, 2nd CP	

12. Read out next character.

RO IAR	I Cycle Ctrl, Special L.G.A.	14.71.34
Set Mem AR Gated	L.G.A. or R, 2nd CP	14.17.36

13. Set character into number select register.

Switch Character from B Ch to Assembly the same step as step 8.

Set E Ch Unit Nu Reg	% or @, I5, Last LG	15.55.01

14. Advance I ring to I6 time.

Set I Cycle Ctrl	Index Not Required, Not B Ch WM, I5	12.13.02
I Cycle Ctrl	Set I Cycle Ctrl, NLLG	12.12.23
I Ring Adv	I Cycle Ctrl, LGB, 2nd CP	12.13.03

15. Read out next character.

RO IAR	I Cycle Ctrl, Special LGA	14.71.34
Set Mem AR Gated	LGA or R, 2nd CP	14.17.16

This character is the op modifier for a U op code or the first character of the B field address for an M or L op code.

16. Set op modifier register (U op code).

Set Op Mod Reg	I Cycle, I6, 1 Addr Plus Mod Op Codes, B Ch Not WM, LGF	15.38.04

17. Adv I ring to I7.

Op Mod Char Time	I6 1 Addr Plus Mod Op Codes B Ch Not WM, I Cycle	15.38.04
Set I Cycle Ctrl	Op Mod Char Time	12.13.02
I Cycle Ctrl	Set I Cycle Ctrl NLLG	12.12.23
I Ring Adv	I Cycle Ctrl, LGB, 2nd CP	12.13.03

18. Read out next character.

RO IAR	I Cycle Ctrl, Special LGA	14.71.34
Set Mem AR Gated	LGA or R, 2nd CP	14.17.16

19. End instruction read-out.

Last Insn RO Cycle	B Ch WM, I7, 1 Addr Plus Mod Op	12.13.05

20. Set IAR with address in STAR.

Last I Cycle	B Ch WM, I7, 1 Addr Plus Mod Op	12.13.05
Reset IAR	Last I Cycle, Early LGF 1st Clk Pulse	14.71.24
Set Mem AR to IAR	Last I Cycle, LGF	14.71.24

Not percent type op codes (all codes but U, M, L, F, K, G and N).

Steps 1 through 5 are the same as percent type.

6. Set the I1 time character into the ten-thousands position of the AAR, BAR, CAR, and DAR (A not address double op code reads into the AAR and CAR only).

SIGNAL	CONTROL	LOGIC
Reset AAR	I1, B Ch WM, Not 2 Char Only	14.71.20
Reset CAR	% Type or Store Addr Reg Op codes 1st CP	
Reset BAR	I1, LG Early F, B Ch WM	14.71.21
Reset DAR	Address Dbl Type Op Code	
Rd 1st Addr to AAR and CAR	B Ch WM, Not % Type Op codes	12.13.06
1st Address	I1 and I2, I3, I4, I5	11.20.11
Insn RO Gate	I Cycle, LGA, B Ch WM	11.10.07
Set AAR and CAR	Rd 1st Addr to A and CAR, 1st Address, Insn RO Gate	14.71.10
Rd 1st Addr to BAR and DAR	Addr Double Op Codes, B Ch WM	12.13.06
1st Addr Set BAR and DAR	Rd 1st Addr to BAR and DAR, 1st Address, Insn RO Gate	14.71.11
Set AR T Th Pos	I1 or 6, LGA or R, 1 Cycle 2nd CP	14.71.05

At I ring 2 time the thousands position receives the character and at I3, the hundreds position receives the character, etc.

At I ring 6 time the character read out of storage can be either an op modifier or the ten-thousands position of the B field.

The B field address is read into the BAR and DAR in the same way the A-field address is read in.

CHAINING

At the end of E phase, if the contents of the A and B address registers contain addresses of the next fields to be processed, another complete instruction word is not necessary. The op code, alone, can be given and the contents of the address registers from the previous operation are used to specify the fields to be used for the new operation. Connecting instructions together in this manner is called "chaining." This method saves storage space used for instructions and saves instruction read-out time.

Two items affect an op code when it is chained:

1. Some two-address-type op codes, when chained to use a single address, use this address as both the A and B field address. These op codes are called "address double-type op codes." "Not address double-type op codes" use the contents remaining in the BAR at the completion of the previous E phase for the B field address.

2. Some op codes require the A and C, or the B and D address registers to contain the same address before the E phase can start.

Address Double-Type Op Codes: The A field of an address double-type op code is read into the AAR's, BAR's, CAR's, and DAR's so that if a WM is read out at "I ring 6 time," the single address is used as both the A and B field addresses. The A field of not address double-type op codes is read into the AAR's and CAR's only.

Arithmetic Op Codes: If an arithmetic op code is chained at I ring 1 time, the CPU takes a D cycle during which the address in the BAR is set into STAR, modified by zero, and read into the DAR (the BAR's and DAR's must contain the same address). Chaining multiply, divide, and table look-up op codes at I ring 1 time initiates a C cycle to update the CAR.

CHAINING CIRCUIT DESCRIPTION

SIGNAL	CONTROL	LOGIC
Same as steps 1 through 5 of Insn RO.		
6. Initiate D cycle.		
Set D Cycle Ctrl	I1, B Ch WM, I Cycle Arith Type Op Codes	12.12.21
D Cycle Ctrl	Set D Cycle Ctrl, NLLG	12.12.21
7. Reset DAR and RO BAR to set STAR.		
Reset DAR	D Cycle Ctrl, LG Early B	14.71.23
RO BAR	D Cycle Ctrl, I1, LG Spec A	14.71.41
Set Mem AR Gated	LGA or R, 2nd CP	14.17.16
8. Set modify controls to Zero.		
Addr Mod Set To Zero	C or D Control, I1	14.71.41
9. Set address into DAR.		
D Cycle	D Cycle Control, LGB	12.12.07
Set DAR	D Cycle Ctrl, LGB and LGC	14.71.13
Set DAR	D Cycle, LGD, LGE, and LGF	14.71.13
10. End instruction read-out.		
Last Insn RO Cycle	D Cycle, I1, Add Type Op Codes	12.13.05
11. When the op code is multiply or divide, a C cycle must be taken to update the CAR.		
Set C Cycle Ctrl	D Cycle, Mult or Div Op codes I1	12.12.42
C Cycle Ctrl Lat	Set C Cycle, Ctrl. NLLG	12.12.20
C Cycle Latch	C Cycle Ctrl LGB	12.12.06

Op Register Set Check

The op register set check insures that the op register receives a set impulse during I op time. The conditions that cause set op reg also bring up "check op register set" (Figure 47). Set op reg and check op register set

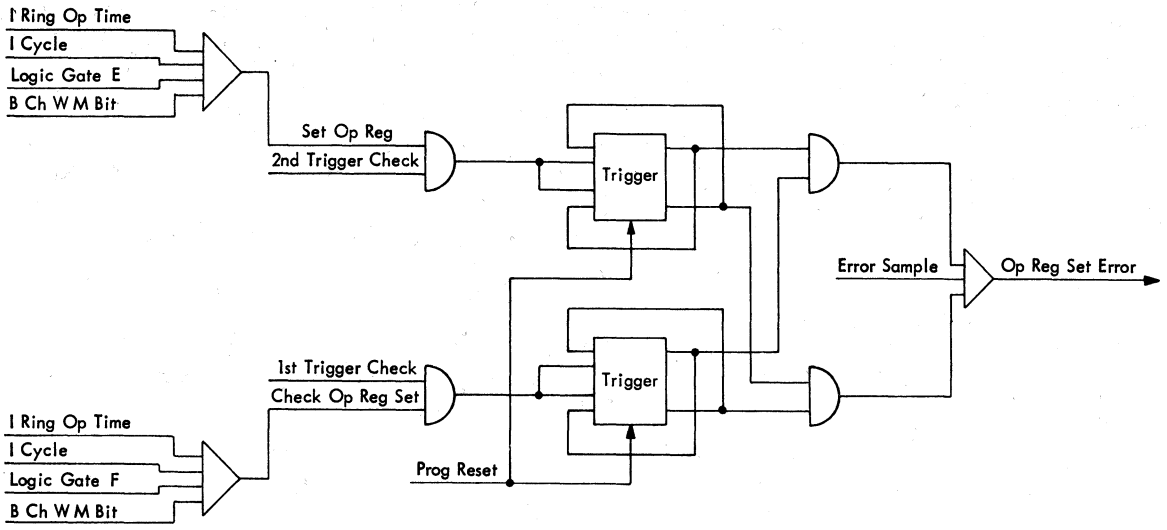


Figure 47. Op Register Set Check (18.14.04)

impulse two triggers that must be both on or both off at error sample time, or an op register set error stops the CPU.

Op Modifier Register Set Check

The op modifier register set check insures that the op modifier register receives a set impulse at op modifier character time for op codes with modifiers. The conditions that cause set op mod reg also bring up check op mod set (Figure 48). Set op mod reg and check op mod set impulse two triggers that must be both on or both off at error sample time or an op mod reg error stops the CPU.

Instruction Check

The instruction check circuit detects the following programming errors:

1. Addressing an op code without a word mark.
2. Using an undefined op code or an IBM 1401 Data Processing System op code when not in the 1401 mode.
3. Using an instruction word that is not a proper length. (Proper lengths are shown in Figure 49.)
4. Failure to have a word mark immediately to the right of the instruction word.
5. A table search op with 8, A, or B bits in the d modifier.

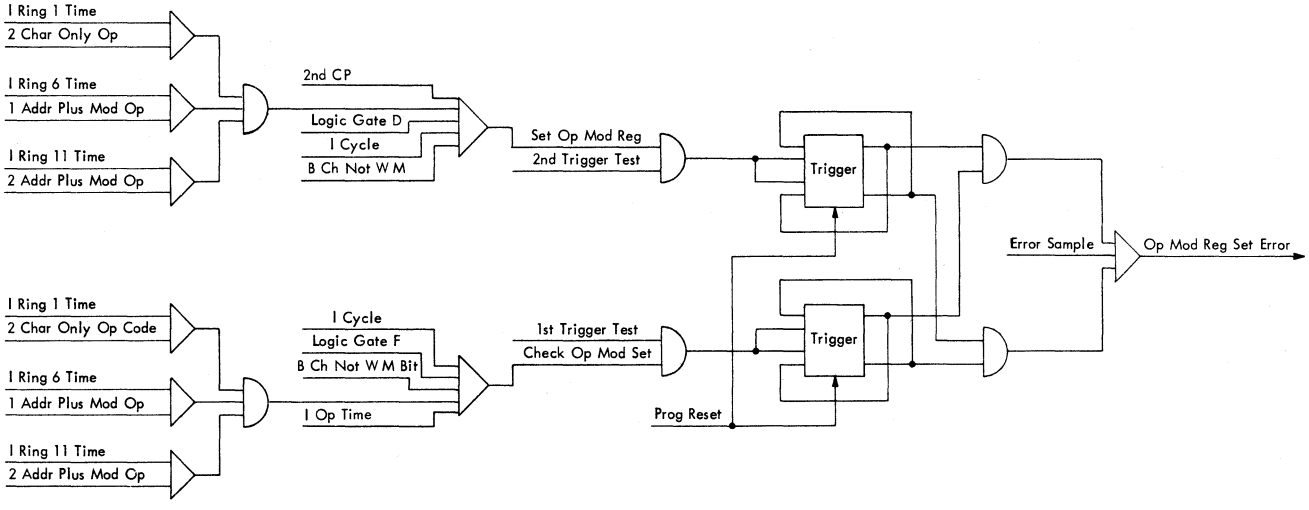


Figure 48. Op Mod Register Set Check (18.14.05)

OP CODE/INSTR	FUNCTION	ACCEPTABLE LENGTHS		
A (A) (B)	Add	1	6	11
S (A) (B)	Subtract	1	6	11
? (A) (B)	Zero and Add	1	6	11
! (A) (B)	Zero and Subtract	1	6	11
@ (A) (B)	Multiply	1	6	11
% (A) (B)	Divide	1	6	11
J (I) d	Branch if Internal Ind On	1	7	
R (I) d	Branch if I/O Status Ind On (Ch 1)		7	
X (I) d	Branch if I/O Status Ind On (Ch 2)		7	
B (I) (B) d	Branch if Char Equal	1	6	12
W (I) (B) d	Branch if Bit Equal	1	6	12
V (I) (B) d	Branch on WM and/or Zone	1	6	12
D (A) (B) d	Move Data	1	6	12
Z (A) (B)	Move Char and Suppr Zeros	1	6	11
E (A) (B)	Move Char and Edit	1	6	11
C (A) (B)	Compare	1	6	11
T (A) (B) d	Table Lookup	1	6	12
G (C) d	Store Addr Reg		7	
, (A) (B)	Set Word Mark	1	6	11
¤ (A) (B)	Clear Word Mark	1	6	11
/ (I) (B)	Clear Storage and Branch	1	6	11
. (I)	Halt and Branch	1	6	
N	No Op	-	-	-
M (X) (B) R/W	Read or Write without WM			10
L (X) (B) R/W	Read or Write with WM			10
U (X) d	Control Unit		5	
K d	Stacker Sel and Feed	2		
F d	Control Carriage	2		

Figure 49. Op Code Lengths

The circuit also detects these system failures:

1. Failure to set a cycle-control latch for the next cycle.
2. Failure to control the length of the storage cycle.

OPERATION

During every cycle, conditions must be met to set the cycle-control latch for the next cycle (Figure 50). If none of the cycle-control latches are set, the instruction check gate is conditioned, and at error sample time the CPU is stopped. During every I cycle the WM bit on the B channel is used to condition last insn RO cycle or the cycle-control latch for the next cycle. Last insn RO cycle is usually used to condition the cycle-control latch for the first cycle of E phase.

For example, there must be a B ch WM at I ring op time to set the I cycle ctrl latch for the next character of the instruction.

If the programmer uses an undefined op code, the op register decode does not condition any common op code grouping lines that are necessary to set the cycle-control latch for the I cycle at I ring 1 time.

Since I-O commands can be overlapped, the E and F cycle-control latches cannot be used in the check circuit. When the commands are overlapped, the I cycle-control latch is set during last instruction RO cycle. When the command is unoverlapped not E and not F ch unovlap in process (set by status sample A that is conditioned by a B ch WM) prevent an instruction check. The process routine line prevents an error during manual operations.

Any transistor failure that prevents a cycle-control latch from setting is detected by this check circuit.

The instruction check gate is also conditioned by the no-last-gate latch. This latch is set on, if either logic-clock ring is advanced to last position without getting a last logic gate. Without the check circuit, the next clock pulse would advance the clock past the end of the ring.

Address Check

The address-check circuit insures that there are no zones over the units, thousands, and ten-thousands positions of an address field in an instruction word.

If the assembly channel contains an A or B bit at I ring 1, 2, 5, 6, 7, or 10 time of an I cycle, the address latch is set on and the CPU stops at error sample time (Figure 51). The not op mod character time prevents an address check on the modifier character read out at I1 or I6.

The address-check circuit also insures that during a scan the address is not modified past the last or first position of storage (wrap-around condition).

The wrap-around condition varies with the size of the storage.

1. On a 10K machine, the mod by plus one latch that is still on at logic gate F (ten-thousands position being modified) indicates that the address is 9,999. The address-check latch is turned on and the CPU is stopped at error sample time.
2. Also on a 10K machine, the mod by minus one latch that is still on at logic gate F indicates that the address is 0,000.
3. On a 20K machine, a 0 bit and a 2 bit on the address channel at logic gate F indicate the address is modified from 19,999.
4. On a 40K machine, a 0 bit and a 4 bit on the address channel at logic gate F indicate the address modified is 39,999.
5. On a 60K machine, a 2 bit and a 4 bit on the address channel at logic gate F indicate the address modified is 59,999.
6. On an 80K machine, a 0 bit and an 8 bit on the address channel at logic gate F indicate the address modified is 79,999.
7. On 20K, 40K, 60K, or 80K machines, a 1 bit and an 8 bit on the address channel at logic gate F indicate the address modified is 00,000.

A wrap-around condition during a move or load op code or a clear op code does not cause an error.

The M or L op codes are always stopped at the last position of storage.

Indexing

Indexing, which is a standard feature in the IBM 1410, conserves storage space used for instructions. For ex-

* Set I Cycle Control (12.13.02)

1.	B Ch WM	I Op		Not 1401 Mode
2.				Set I Cy Ctrl No Op
3.				ARS No Op • I Cycle
4.				Op Mod Time • Not 1401
5.	B Ch Not WM	I 1 + 2 + 3 + 4	I Cy	Address Type Op Codes
6.		I 5	C Cy	
7.	B Ch Not WM	I 5 + 10		Index Not Required
8.	B Ch Not WM	I 6 + 7 + 8 + 9	I Cy	Two Address Type Op Codes
9.		I 10	D Cy	

* This line can be set by any of the nine conditions.

* Last Insn RO Cycle (12.13.05)

1.		I 1	C Cy	C Cycle Op Codes
2.		I 1	D Cy	Add Type Op Codes
3.	B Ch WM	I 1		No C or D Cycle Op Codes
4.	B Ch WM	I 2		2 Char Only Op Codes
5.		I 6	D Cy	Mult + Divide Op Codes
6.	B Ch WM	I 6		No D Cy at I6 Op Codes
7.	B Ch WM	I 7		I Addr Plus Mod Op Codes
8.	B Ch WM	I 11		2 Addr No Mod Op Codes
9.	B Ch WM	I 12		2 Addr Plus Mod Op Codes

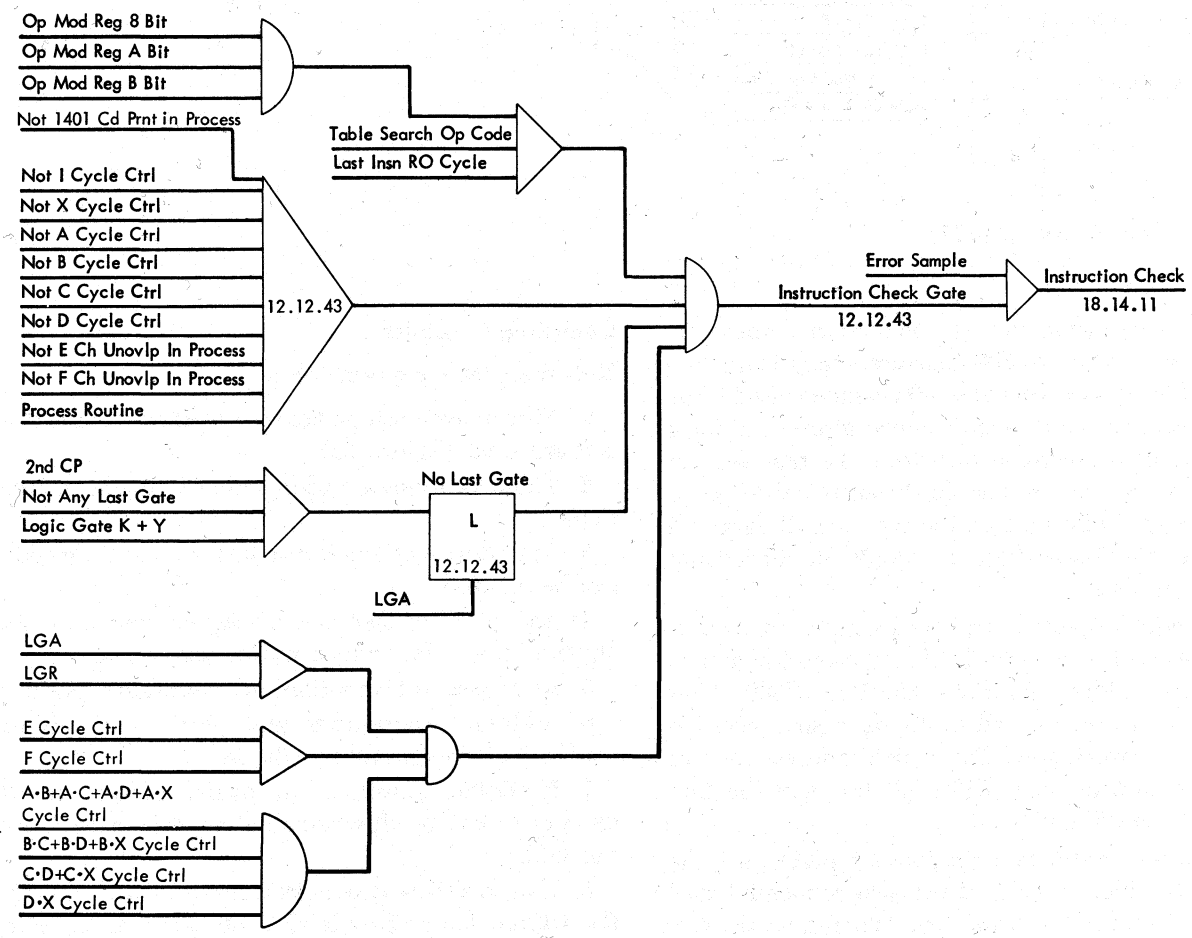


Figure 50. Instruction Check

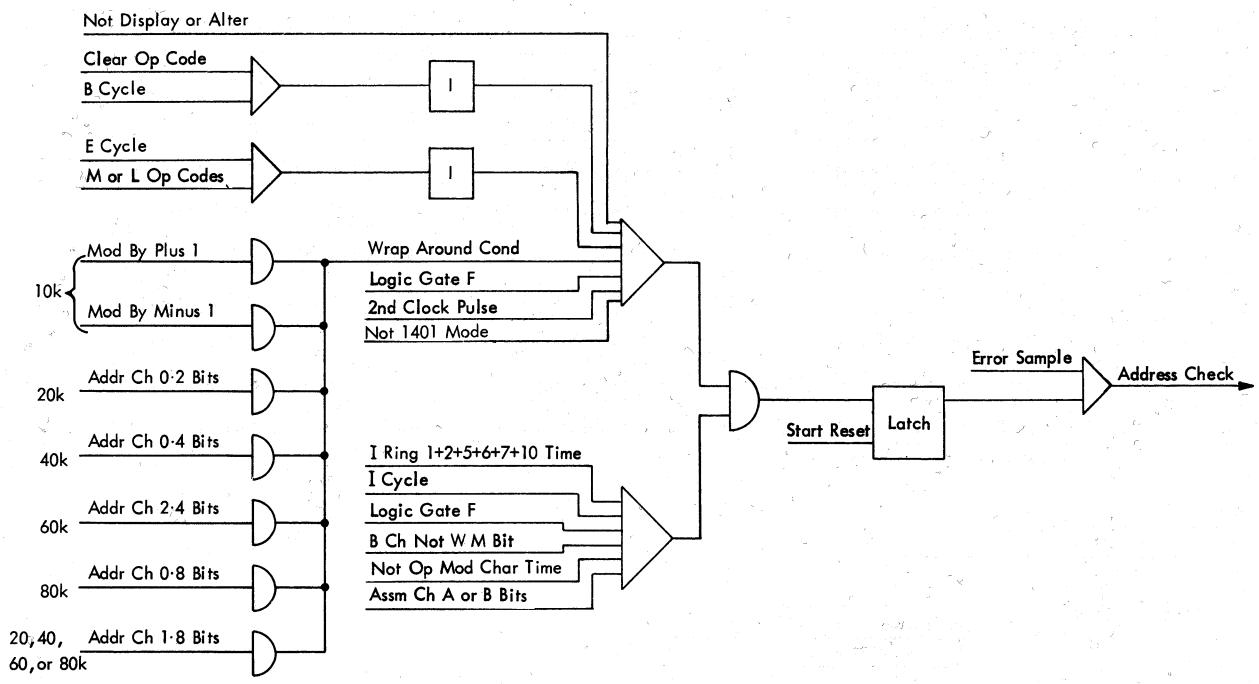


Figure 51. Address Check (18.14.11)

ample, the indexing feature can be used in a tape operation. Tape records are 800 characters long consisting of 10 card images or records of 80 characters each. The CPU processes the card records one at a time and must move each card record in turn from the tape read-in area to a work area in storage. From the work area, operations are performed on the card record data; the results are stored elsewhere in storage for subsequent output operations.

Using index register 2 (IR2) for example, the operation begins with zeros in IR2. The tape read-in area is contained in address positions 07001 to 07800. After the first tape record is read in, the first card record is moved to the work area. The A field address for this data move instruction is 070!1 (B bit over the tens position "0" specifies IR2).

After card record data operations are performed, the factor 80 is added to IR2 and the next sequential card record is moved to the work area. When the card record data move instruction is read out this time, the A field address will be indexed by +80 by IR2 and the card record at location 07081 will be moved.

Each time the program goes through this loop, +80 will be added to IR2 and the next sequential card record area will be used the next time. When writing such a program, additional steps are necessary to determine when the last card record of a tape record is used, so that a new tape record would be read in and IR2 would be reduced to zero for the start of the next series of operations.

Operating Principles

Note these indexing principles:

1. Fifteen five-position fields or registers in core storage are used (Figure 52).
2. These locations are addressable as any other location.
3. Any address of any instruction (except G op code) can be indexed.
4. An index register can be signed and is added algebraically to an address in the instruction.
5. Addresses in instructions are considered positive.
6. Addition occurs after units position of address reads out of storage and into the AR.
7. If addition results in an invalid address, an address error will result when an attempt is made to use this address.
8. If an overflow occurs as a result of the addition, the arithmetic overflow latch is not set, and the carry is lost.
9. Zones (other than in the units positions) and word marks in the index registers are ignored by indexing, but are not disturbed.
10. Neither the contents of the index register nor the address originally stored in core storage as part of the intsruction word is affected by the operation.
11. Zone bits over the tens and hundreds position of the address in the instruction are used as tags to specify whether the address is to be indexed, and if so which index register is to be used (Figure 53).

Index Register	Locations	
	From	To
1	00025	00029
2	30	34
3	35	39
4	40	44
5	45	49
6	50	54
7	55	59
8	60	64
9	65	69
10	70	74
11	75	79
12	80	84
13	85	89
14	90	94
15	95	99

Figure 52. Index Register Locations

OPERATION

As the hundreds and tens positions of the addresses are read out during instruction read-out (Figures 54 and 55) the zones from the assembly area set the index-tag latches (Figure 43, sheet 1 of 3). There are A, B, and C tag latches for each of the two positions of index tags, that correspond to the A, B, or zone C bits (the zone C bit is generated in the A-channel validity-check circuit in order to make the number of zone-bits odd).

If the index-tag latches indicate that there are no index tags, "index not required" allows instruction read-out to continue.

When the index-tag latches indicate that there are index tags, an "index required" line:

1. Prevents an I ring advance, after the units position of the address is read into the address register (I ring 5 or 10 time).

SIGNIFICANCE OF TAG BITS

Hundreds Position B-Bit	Hundreds Position A-Bit	Tens Position B-Bit	Tens Position A-Bit	Index with Register
8	4	2	1	
			X	1
		X		2
		X	X	3
	X			4
	X		X	5
	X	X		6
	X	X	X	7
X				8
X			X	9
X		X		10
X		X	X	11
X	X			12
X	X		X	13
X	X	X		14
X	X	X	X	15

Figure 53. Index Tag

2. Causes the machine to take five X cycles.

During the five X cycles, the five positions of the index register read out of storage onto the B channel. The five digits add units position first, to the address in either the CAR or DAR, depending on which field is being indexed (I5, index A field; I10, index B field). A six-position ring called the A ring is used to identify and gate the five positions of the address.

The A ring 1 time trigger is set at logic gate F of the I cycle at I5 or I10 time when indexing is required. A ring 1 time and the index tag latches combine to generate the address of the units position of the selected index register. This address is gated onto the address bus at logic gate A and STAR is set at 2nd CP LGA.

"Index required" and "I cycle" bring up "X cycle control" and the first X cycle starts at LGB time. Also at LGB of this first X cycle, the A ring advances to A ring 2 time and the address register (CAR or DAR) is gated onto the address bus.

During A2 time, the units position of the address bus is gated to the AR exit channel, to the A data register and onto the A channel, then to the adder where it combines with the units position of the index register that is read out of storage onto the B channel. The sign over the units position of the IR determines whether the B side of the adder is true-added or complement-added.

The result from the adder is gated through the assembly to the address channel where it is set into the AAR or BAR. If the op code is an address-double-type op code the indexed A field address reads into the AAR, BAR, and DAR in case there is no B field address.

A ring 2 and the index tag latches are combined to generate the address of the tens position of the index register. The CPU takes another X cycle and advances the A ring to A 3 time and the tens position is added and stored the same as the units position.

When the A ring is at A 6 time, the last or ten thousands position is combined. At the end of this X cycle the CPU takes a C or D cycle, depending on the address being indexed, in order to update the CAR or DAR with the new indexed address. During this indexing operation the I ring is not advanced. At the completion of the C or D cycle, the CPU takes I cycles to complete instruction read-out.

INDEXING CIRCUIT DESCRIPTION

SIGNAL	CONTROL	LOGIC
1. Set index tag latches.		
Set H Pos Index Tags	I3, or 8 LGA (Not) No Index on 1st Addr Ops	14.70.12
Set T Pos Index Tags	I4, or 9, LGA (Not) No Index on 1st Addr Ops	14.70.12

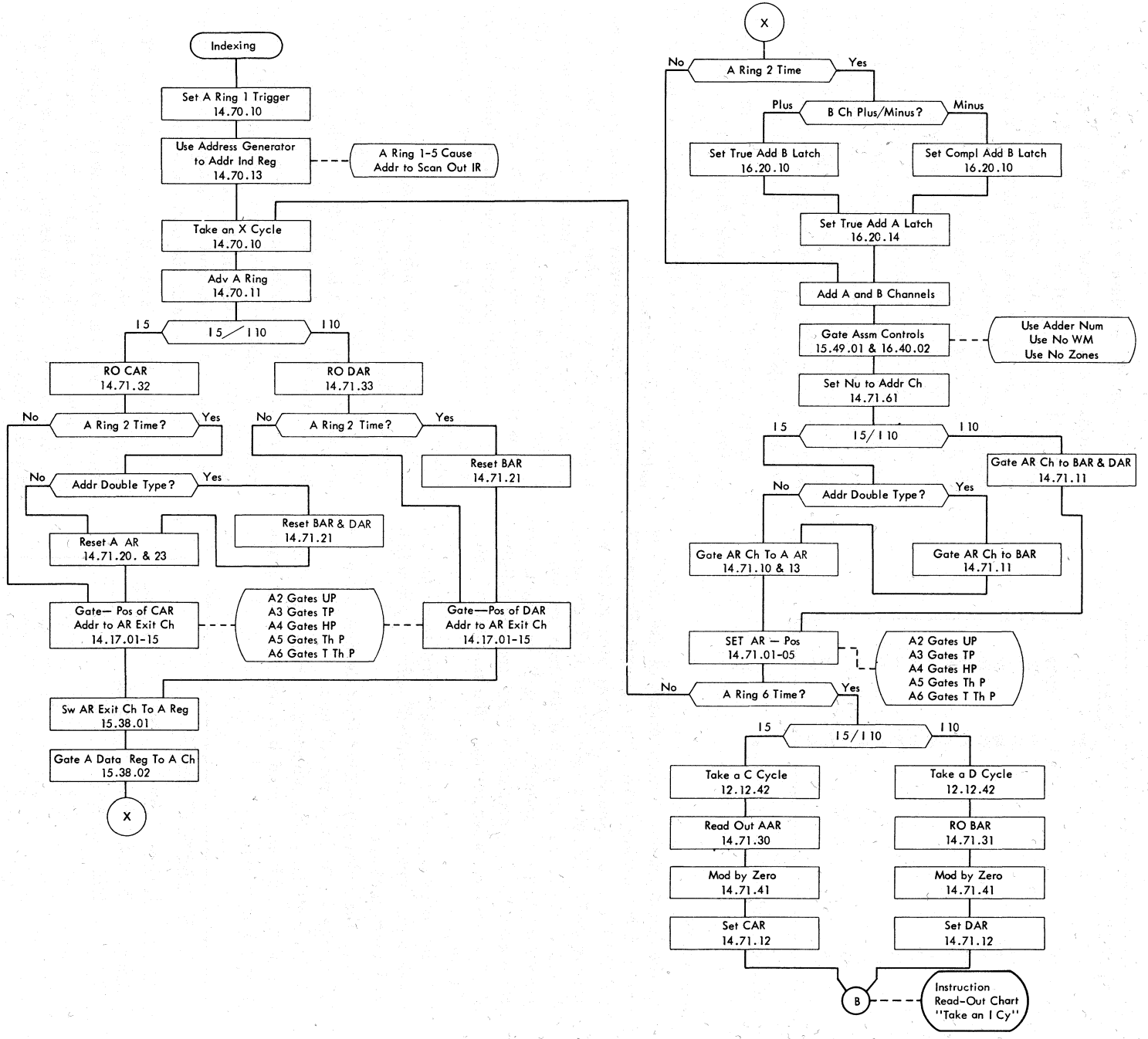


Figure 54. Indexing Operation

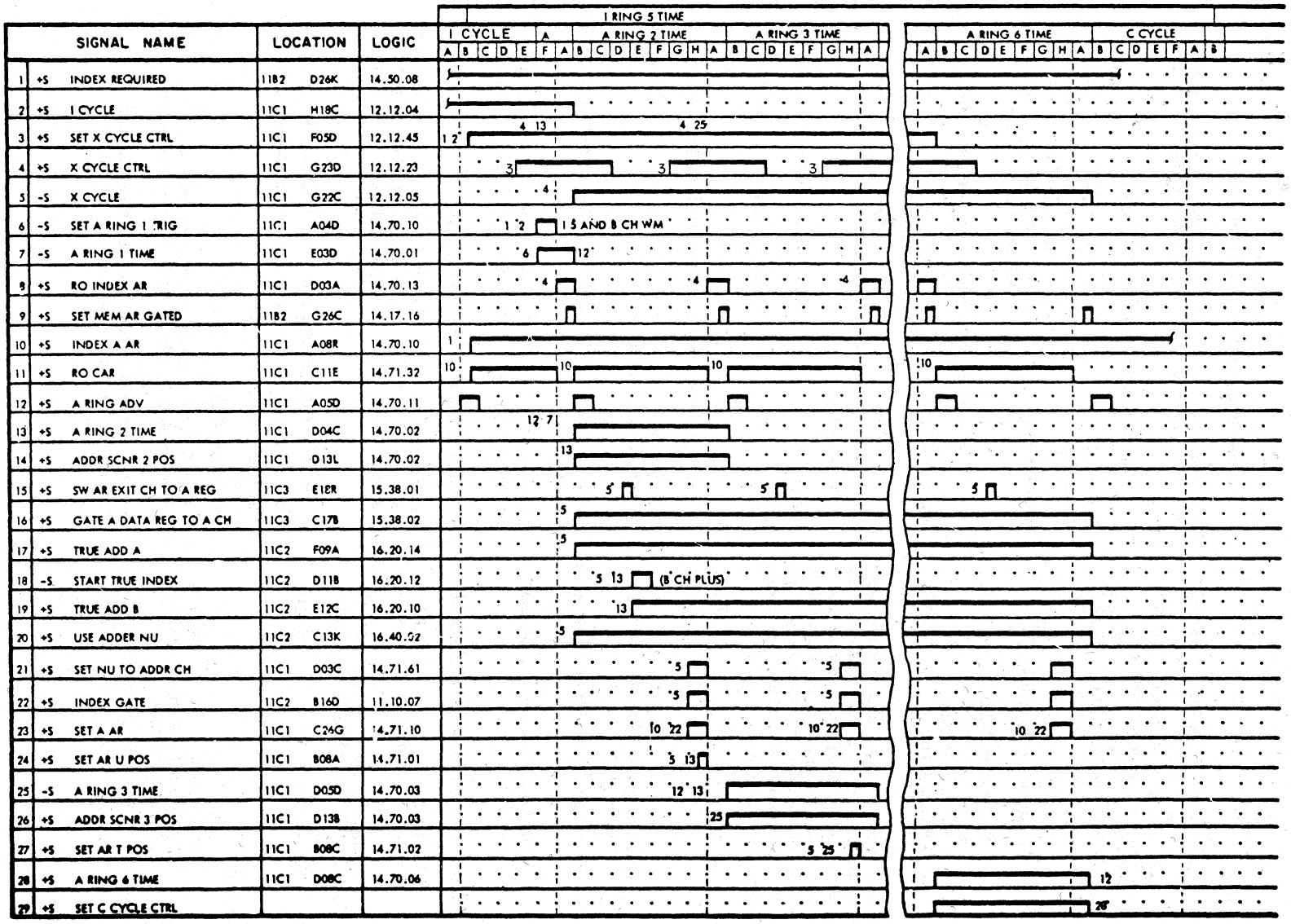


Figure 55. Indexing Timings

SIGNAL	CONTROL	LOGIC

2. Initiate indexing.

Index Required	(Any A or B Index Tag Latch "On" 1.)	14.50.08
Set X Cycle Ctrl A	1 Cycle, I5 or 10, Index Required, B Ch Not WM	14.70.10
Set X Cycle Ctrl	Set X Cycle Ctrl A	12.12.45
X Cycle Ctrl Lat	Set X Cycle Ctrl, NLLG	12.12.23
X Cycle Latch	X Cycle Ctrl Lat LG B	12.12.05

3. Read out the Units Position of the Index Field

Set A Ring 1 Trig	Index Required B Ch Not WM, I Cycle I Ring 5 or 10 Time	14.70.01
A Ring 1 Time	Set A Ring 1 Trig	14.70.01
RO Index AR	X Cycle Ctrl 1, LGA	14.70.13

RO index AR gates the outputs of the hundreds position index tag latches to bring up the tens position of the index register address (Systems 14.50.05 and 14.50.06). RO index AR and A Ring 1 through 5 time gate the tens position latch outputs to bring up the units position of the index register address (Systems 14.50.04). The high positions of the address are always zero (Systems 14.15.08 through 14.15.13).

Set Mem AR Gated	LGA, 2nd CP	14.17.16

4. RO CAR

Index AAR	Index Required I Ring 5 time	14.70.10

NOTE: Index BAR is also brought up if addr double type op code.

RO CAR	Index AAR, LGB to Last LG	14.71.32

5. Gate units position of CAR address to A channel.

A ring Adv	LGB	14.70.11
A Ring 2 Time	A Ring Adv A Ring 1 Time	14.80.02
Addr Scan 2 Pos	A Ring 2 Time	14.70.02
Sw AR Exit Ch to A Reg	X Cycle Latch, LGD 2nd CP	15.38.01
Gate A Data Reg to A Ch	X Cycle Latch	15.38.02

6. Set adder controls.

True Add A	X Cycle Latch	16.20.14
Start True Index	X Cycle Latch, A Ring 2 Time, B Ch Plus	16.20.12

NOTE: B Ch Sign Ctrls B Ch True or Complement Add.

True Add B Lat	Start True Index	16.20.10

SIGNAL	CONTROL	LOGIC

7. Gate adder out to address channel.

Use Adder Nu	X Cycle Latch	16.40.02
Set Nu to Addr Ch	X Cycle Latch, LGH	14.71.61

8. Reset AAR and read in units position.

Reset AAR	Index AAR, A2, LGF	14.71.20
Index Gate	X Cycle Latch, LGH	11.10.07
Set AAR	Index AAR, Index Gate	14.71.10
Set AR U Pos	X Cycle Latch A2, LGH 2nd CP	14.71.01

9. Read out the tens position of the index field.

Set X Cycle Ctrl	X Cycle Latch, A 2, 3 4 5 Time	12.12.45
RO Index AR	X Cycle Ctrl, LGA	14.70.13

10. RO CAR

Index AAR	Index Required, I Ring 5 Time	14.70.10
RO CAR	Index AAR, LGB to last LG	15.71.72

11. Gate tens position of CAR address to A channel.

A Ring 3 Time	A Ring 3 Time	14.70.03
Switch AR to A Ch	Same as step 5	

12. Adder controls are set, gate adder to address channel.

Use Adder Nu	X Cycle Latch	16.40.02
Set Nu to Addr Ch	X Cycle Latch, LGH	14.71.61

13. Read in tens position of AAR

Index Gate	X Cycle Latch, LGH	11.10.07
Set AAR	Index AAR, Index Gate	14.71.10
Set AR T Pos	X Cycle Latch, A 3, LGH, 2nd CP	14.31.02

14. The remaining positions are similar to tens position. At A ring 6 time the indexed address in the AAR must be set into the CAR.

Set C Cycle Ctrl	A 6, I 5	12.12.42

C cycle is the same as in instruction read out.

If the B field is indexed set D cycle ctrl comes up a A ring 6 and I ring 10 time.

If the op code is an address double type, the AAR, BAR, and DAR read in the indexed address from the adder.

The IBM 1410 Data Processing System requires a 3-phase 208- or 230-volt ac source of voltage. The main-line voltage feeds to the 1411A frame of the CPU. The power-on key on the console controls the tape frames, RAMAC® files, reader-punch, and printer except when they are off-line for independent operation. The independent control must be manually set for the peripheral equipment.

Power is brought to a circuit-breaker-distribution panel (Figure 56) in the 1411A frame of the CPU. The ac voltage feeds from the circuit breakers into ferroresonant regulators where it is changed to a regulated ac voltage. These regulated ac voltages are distributed to the dc supply modules, where ac is converted into regulated dc voltages.

The circuits that use the incoming voltage without regulation, motors, etc., feed directly from the source through the circuit breakers and to the units.

The various power supply voltages that are distributed from the main power source are: +6 vdc, −6 vdc, +12 vdc, −12 vdc, +30 vdc, −36 vdc, −48 vdc, +60 VM, 115 vac and 208 vac.

These voltages from the individual power supplies are brought to a laminar bus in each frame. The laminar bus makes all the various voltages available for easy access to the SMS card bases for wiring.

Regulation

The ferroresonant regulators used by the power supply consist of special transformers and capacitors. The capacitors and the transformers are packaged into separate modules for flexibility in mounting. The regulators are available in several output ratings, ranging from 250 to 1,840 watts.

The ac regulator changes the line voltage to a regulated voltage of approximately 133 vac for the dc power-supply modules.

The dc power-supply module consists of an isolation transformer, solid-state rectifiers, associated filter networks, and a magnetic-type circuit breaker for overcurrent protection. The dc power supply incorporates a series regulator (that consists of an SMS pluggable-amplifier card), power transistors, and filters. These provide a dc voltage with ±2% regulation.

Special-Voltage Power-Supply Unit

Special voltages are required to supply core-driver circuits. Two voltages are developed from the two supplies 7 and 8 that feed through the ferroresonant regulator 2 from circuit breaker 5. Both power supplies 7 and 8 have a separate control for setting their output voltage. PS7 supplies +25 vdc at 4 amperes and PS8 supplies +60 vdc at 6 amperes.

Power-On Sequence

The master circuit breaker that is located on the 1411A power-supply frame controls the incoming power to the system (Figure 57). When the master circuit breaker is on, power is supplied to a 24 vac transformer. This transformer (T2) supplies the power to pick MPK relay that closes the MPK contacts 1, 2, 3.

With power on at the circuit-breaker panel, pressing the power-on key on the console starts the power-on sequence (Figure 58).

Emergency Off

Pulling the emergency-off switch drops relay MPK and opens the circuit at the multiple circuit breaker. MPK points 1, 2, 3, are in series with the CB panel. This also drops the power to other peripheral equipment that have their own line cords.

The emergency-off switch is mechanically interlocked so that once it has been operated, it can not be reset from outside the console.

To reset the emergency-off switch, the control-unit cover must be removed from outside the console, and the contact locking spring must be lifted.

Relay 76 provides the emergency power control for special features that can be added to the system.

DC-Off

Pressing the dc-off key on the console drops all the dc power to the units (Figure 59). The system-power-off, memory-heater, and file-ready relays are not affected by the dc-off operation. The dc-off sequence starts when the machine drops R5, and then steps down to a complete dc power-off condition on the system (Figure 60).

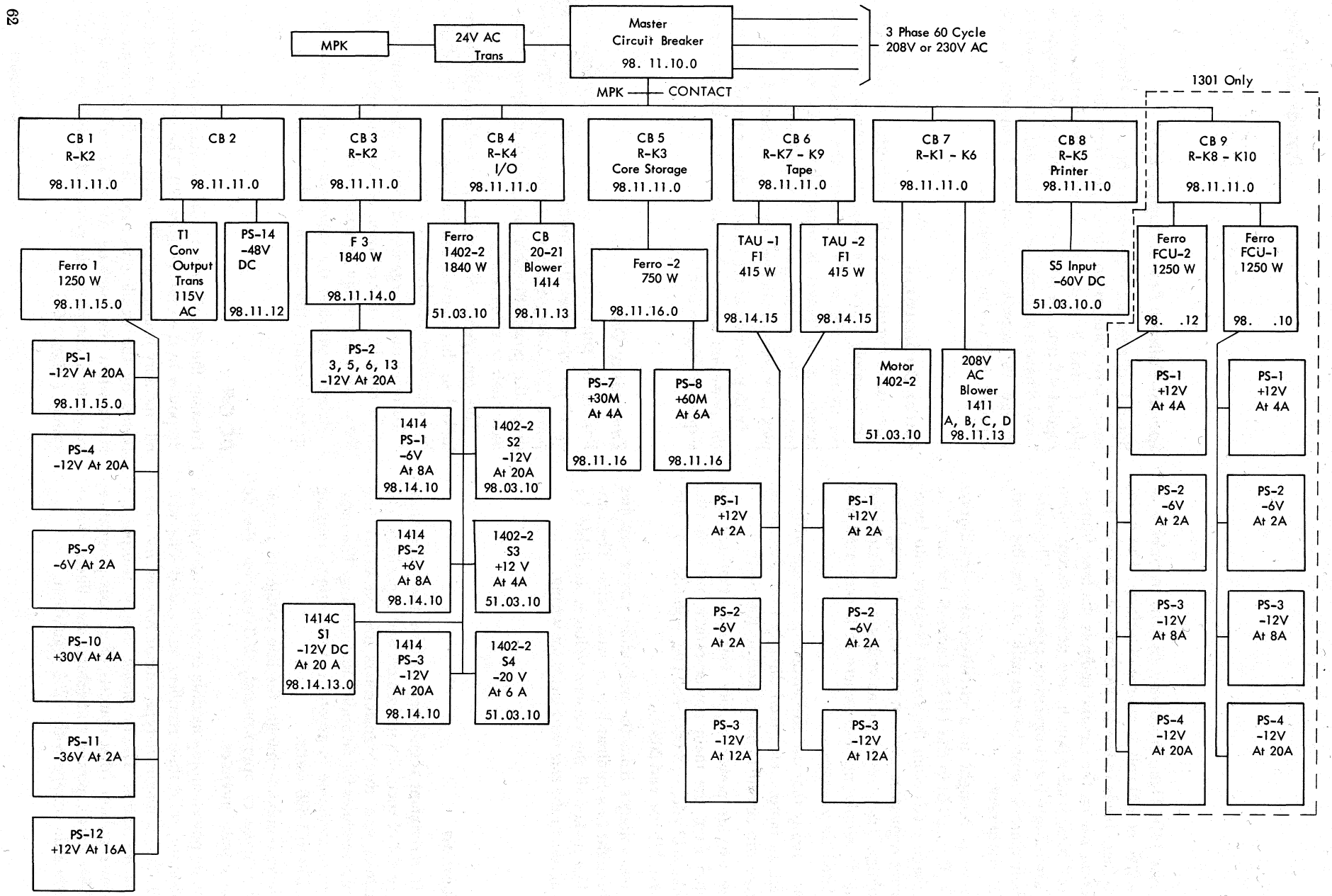


Figure 56. IBM 1410 Power Distribution

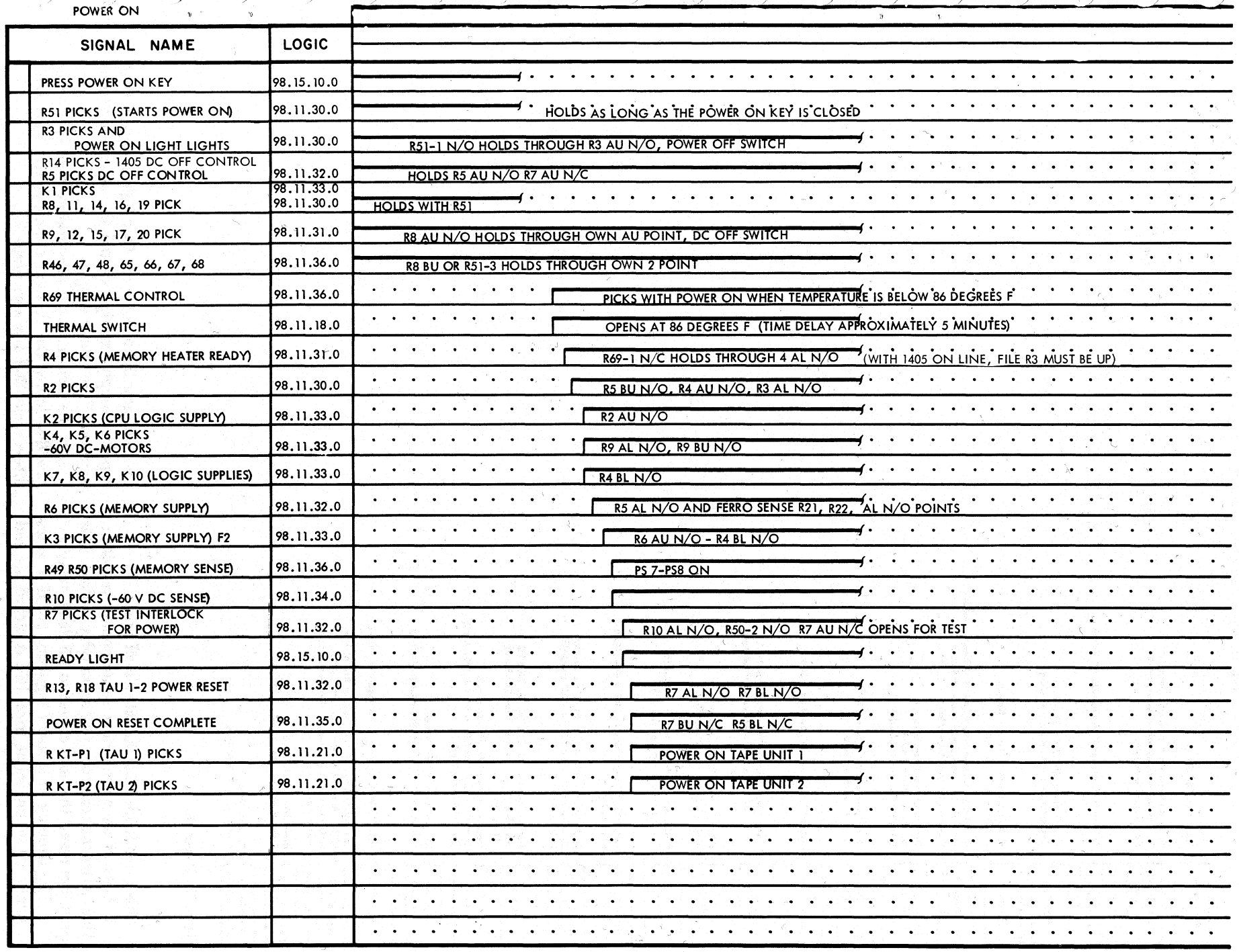


Figure 57. Power-On Timing Chart

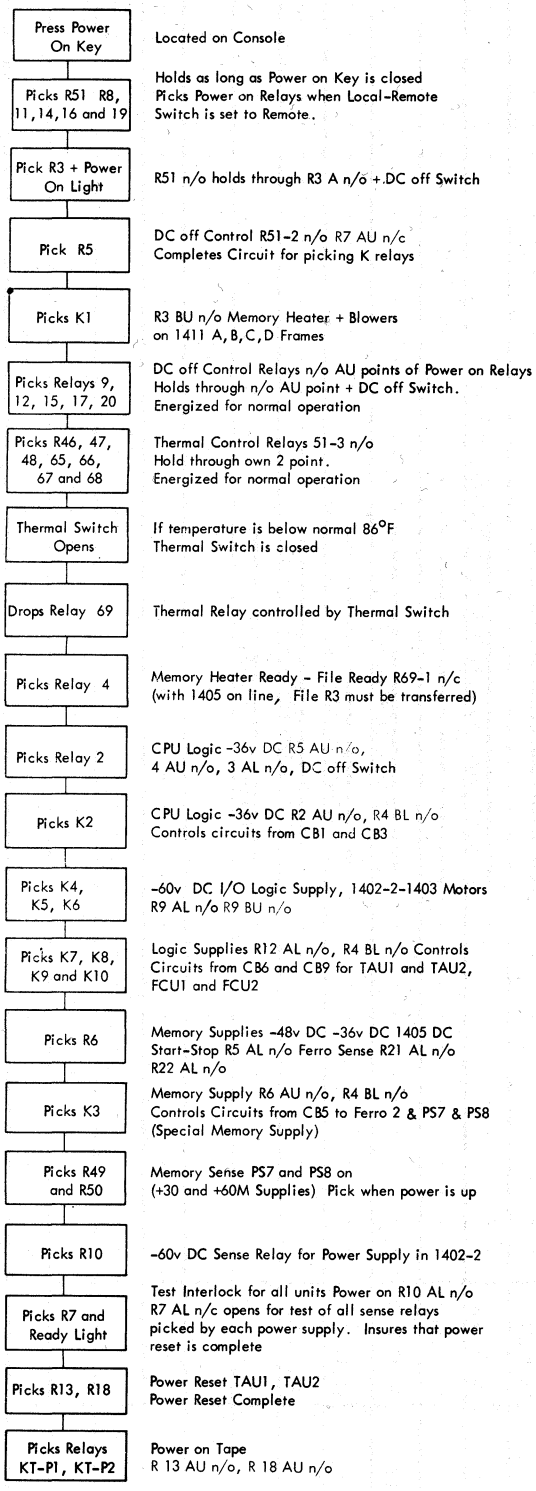


Figure 58. Power On

Other conditions that initiate dc-off are:

1. Loss of an output of a ferroresonant regulator. This causes the corresponding sense relay to drop. This condition opens the hold circuit to R5 dc-off relay.

2. The tripping of a series regulator CB. If a series regulator CB in any frame trips, R53 is picked up, and two indicator lights come on. One light indicates that a power supply CB tripped, and the other shows the location of the power supply.

3. If the memory-array temperature goes below the specified limits, the thermal switch closes. This condition picks R69 and also drops R5.

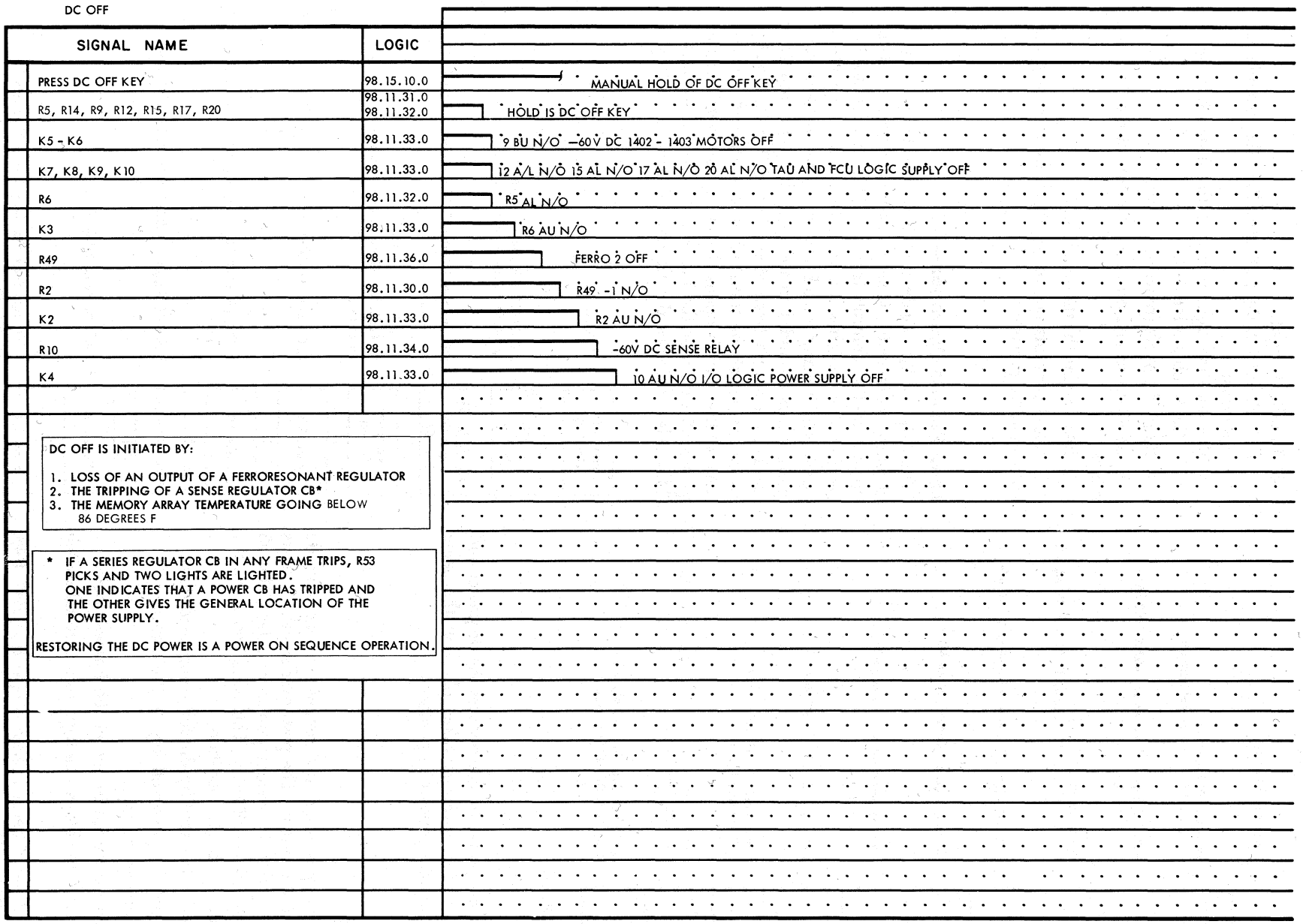


Figure 59. DC Off Timing Chart

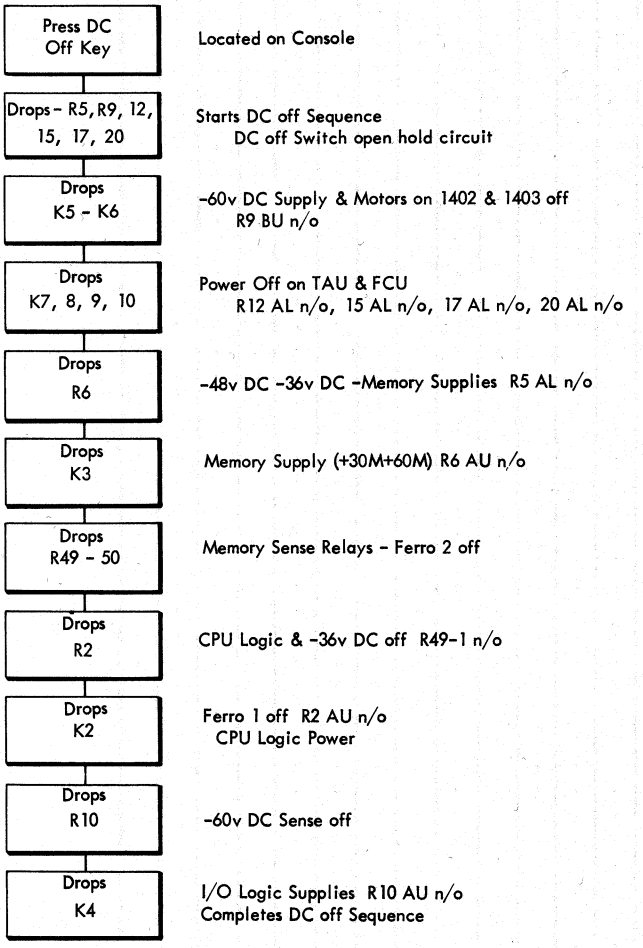


Figure 60. DC Off

Pressing the power-on key restores the dc power and the sequence for power-on takes place in the same order as a normal power-on operation.

Power-Off

Pressing the power-off key removes all ac and dc power from the system. The power-off sequence starts by dropping the R3 system power-off relay. The R3 AL drops the R5 dc-off relay. This condition starts the machine into a dc-off condition.

Power off is initiated by the following conditions:

1. Pressing the power-off key on the console.
2. Any blower CB trips.
3. A thermal switch in one of the frames opens.

When either the blower CB trips, or a thermal switch opens:

1. One of these thermal relays drops: R46, R47, R48, R65, R66, R67, R68.
2. A latch relay, R45, picks and latches up.
3. Two lights light:
   a. A thermal light indicates that the trouble is thermal.
   b. A location light indicates the frame in which the trouble is located.
4. R45-1 drops R3 (power-off relay).
5. R45-2 opens and prevents resetting of the thermal relays.
6. R45-3 lights the thermal lights.
7. R45-4 prevents any of the lights from coming on with an initial power-on.

Local Remote Operation—I-O

When the off-line mode switch on the 1414 I-O synchronizer (Figure 61) is set in any other position than normal, on-line controls from the 1411 CPU are not effective. This switches the I-O units to an independent operation. Pressing the off-line key on the 1414 console picks relays 54 and 1 in the 1411 CPU. This transfers the 115 vac supply from R4 BL, through 1AN/C, directly to the output of the transformer, and through 1AN/O. The off-line switch opens the circuit to short out the power-off switch on the 1414 and to make it operative. This relay switches the dc control from the console

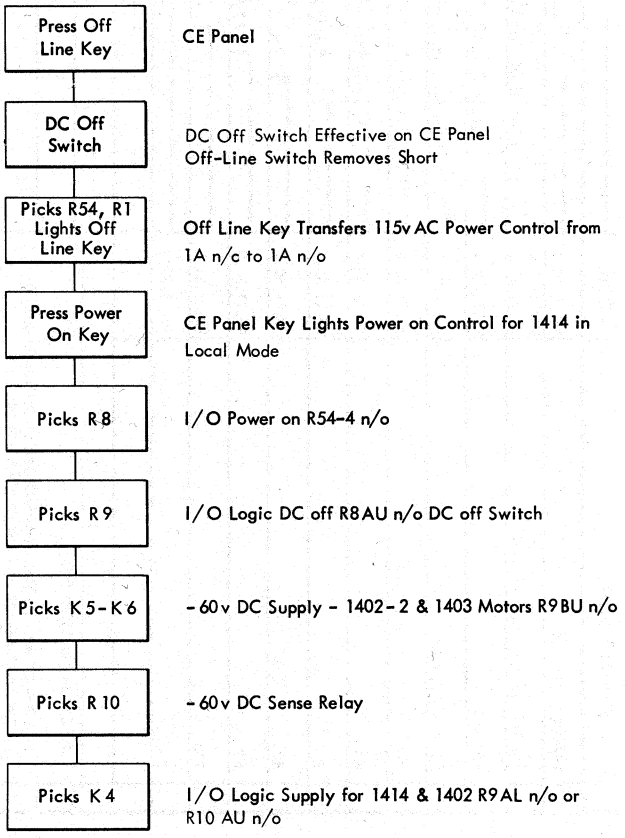


Figure 61. Input-Output Synchronizer (Power On)

unit to the 1414 CE panel on and off switches. The light on the console indicates the status of the units for local or remote operation. The off-line light is on when the unit is selected for local operation. In this mode the power for the synchronizer is under the control of the power-on and off keys that are located on the CE panel of the synchronizer.

If the switch is transferred from remote to local after the power is on the system, the dc power is not lost to the synchronizer. Pressing the power-off key that is located on the CE console drops relays 9 (I-O logic dc-off) and 24 (ferrosense).

TAU Off-Line Operation—Local Remote Switch

The local-remote switch on the CE panel of the TAU units selects each unit for on-line or off-line operation (Figure 62). With the switch set to remote mode, the unit is on line with the system. In local mode, the unit is off line and has independent dc-on, dc-off operation from the CE panel.

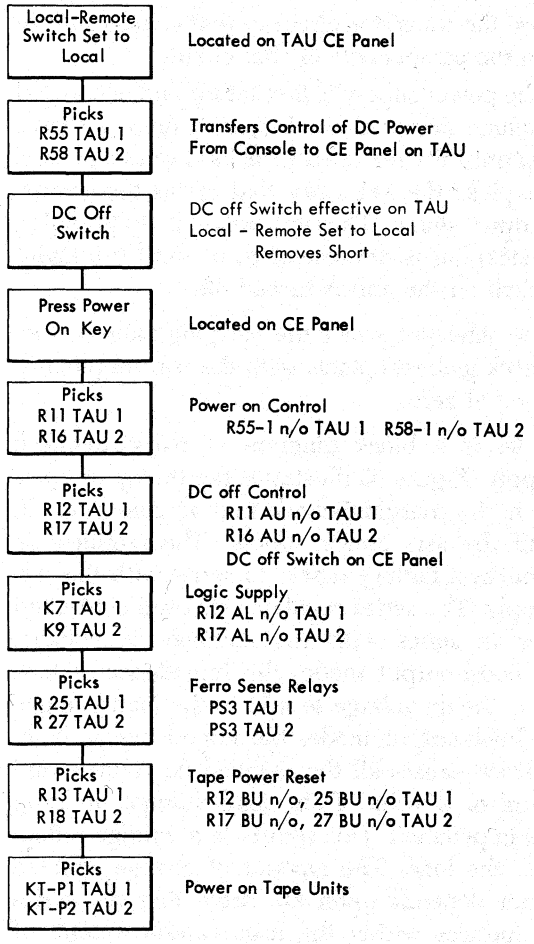


Figure 62. Power On, Tape Units

1301 File Control Unit (FCU) Off-Line Operation-Local-Remote

The local-remote switch on the CE panel provides manual control (similar to the TAU) for selecting the FCU for on-line-with-the-system operations, or for off-line-for-checking-and-servicing operations (Figure 63).

1405 FCU Off-Line Operation

The 1405 local-remote switch puts sequencing of the 1405 under control of 1405 circuits when in the local position. CPU can operate normally without 1405. When on line, or in remote position, the sequencing of 1405 is still under control of 1405, but CPU cannot cycle up until file is ready.

Power-Fault Indicators

The loss of power from any ac or dc supply is detected by the picking of relay 53 in the 1411A frame. Picking of relay 53 opens the circuits to dc-off control for the

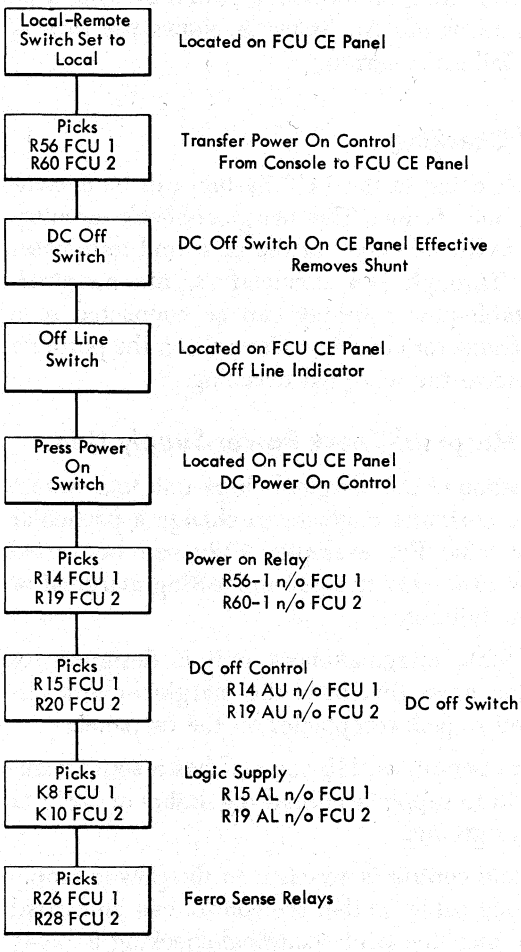


Figure 63. Power On, File Units (1301 Only)

system, and indicates the type of failure and unit location by lights on the 1411A control panel. The failure can be classified as one of the following types.

Thermal Reset

This condition latches up thermal relay 45. This isolates the power-on circuit until the thermal-relay latch is reset. Pressing the thermal-reset key on the 1411 CE panel-latch trips relay 45, and restores the circuitry to normal.

Overcurrent Failure

This type of failure trips the circuit breaker on the particular power-supply module that is involved. This condition is caused by overloading the power supply because of a circuit-component failure. A light on the control panel of the 1411A unit indicates the general location of the power unit.

Overvoltage Failure

The overvoltage type of failure is detected by an overvoltage protection device that is set for a maximum voltage range. When the voltage-protection device senses an overvoltage condition, a circuit breaker trips and power turns off. An indicator shows the section where the failure occurred.

Marginal Checking

Marginal checking in the 1410 System can be accomplished on any frame. The marginal-check circuitry is brought to the CE panels of the units and terminates at a jack. Through jack connections, the marginal-check portable-power supply can be connected to a particular frame for checking. Controls on the portable supply perform the marginal checking.

Portable Marginal-Check Power-Supply Unit

The application of the marginal-check unit to a system permits the customer engineer to change a particular voltage by ±3v. For example, +12v can be varied from a +9v to a +15v to assist in locating marginal or intermittent failures.

The portable marginal-check unit is designed for use with machines that have the marginal-check circuitry wired to jack receptacles on the CE panels.

The unit operates on 115 vac and has a series regulator built in to supply a normal regulation of ±2% in reference to ground.

The remote control is attached to the power supply unit by a long cable, so that the control can be carried around the machine while marginal-checking is being performed.

Remote control permits full control of the marginal power-supply unit. The variable control has an off position for turning the output off, and a potentiometer to control the output voltage from 0 to 3 volts. A toggle switch on the unit gives a setting to select either *buck* or *boost* voltage.

The power unit has a power-supply attachment cord for input voltage from any available 115 vac outlet. The output cord has a plug to connect the power supply to the jack receptacle on the CE panel of the unit by means of the marginal-check jack receptacles.

The unit is protected from overload voltage by a 6-ampere circuit breaker that is located on the component panel in the power-supply unit. The marginal-check unit circuit-breaker trips, if the remote control switch is set to the boost position, and if the jack plug is not inserted in a marginal-check jack receptacle when power is on.

The main-line switch is located on the top near an indicator light. The light gives a visual indication that the power is on when the unit is in use.

A safety control is built into the marginal check unit. The control insures that the potentiometer is set at zero when the unit is attached. This prevents any surge of current into the transistor circuitry that could result in damage to the components of that circuit.

When the power supply is first set up and connected to the machine marginal-check jack, it does not have any output until the remote control has been set to zero. This steps picks the RY1 relay that opens the power-supply output shunt. The RY1 relay is self-holding until the jackplug is disconnected, or until the main-power switch on the unit is turned off.

CAUTION: Always extract the jackplug from a marginal-check jack receptacle with the control potentiometer set at zero.

Figure 64 is a block diagram of marginal-check power supply. Figure 65 illustrates the theory of operation when the marginal-check unit is connected in series with the SMS power supply. The rectified dc voltage acts as a battery that is in series with the SMS power supply. The series regulator effects a controlled impedance in series with the rectified dc voltage. When in boost-output mode, the impedance is low. This allows the dc voltage to add to the load voltage. When in buck-output mode, the impedance is high. This condition causes all the rectified dc voltage, and a maximum of 3 volts of the load voltage, to drop across the impedance. This results in a voltage reduction across the load. The amount of change effected by this unit depends upon the drive that the series regulator induces within the maximum-load limit of 5 amperes.

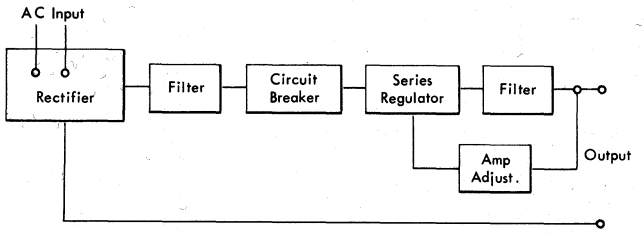


Figure 64. Marginal-Check Power Supply (Portable Unit)

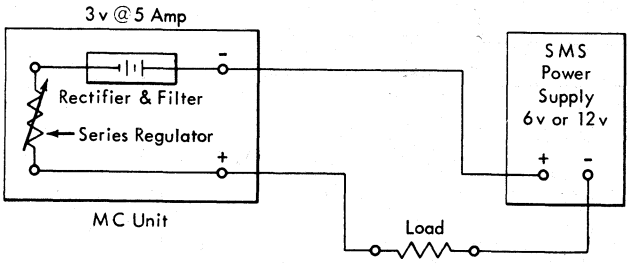


Figure 65. Marginal-Check Unit in Series with SMS Power Supply

The SMS series regulator-control card plugs into the receptacle in the power-supply unit.

CAUTION: When the unit is in use do not block the ventilating fan airflow through the ends of the power supply unit.

Power Unit Locations

Figure 66 shows the location on the front of the 1411A frame of the following: the power-supply unit, circuit breakers, cable connectors, K relays, controls, indicator lights, and marginal-check jacks.

Figure 67 shows the location on the rear of the 1411A frame of the following: the relay gate assembly, terminal blocks, control transformers, and power supply.

Frame and Chassis Designations

Figure 68 is a chart that shows the voltage designations for the laminated bus pins.

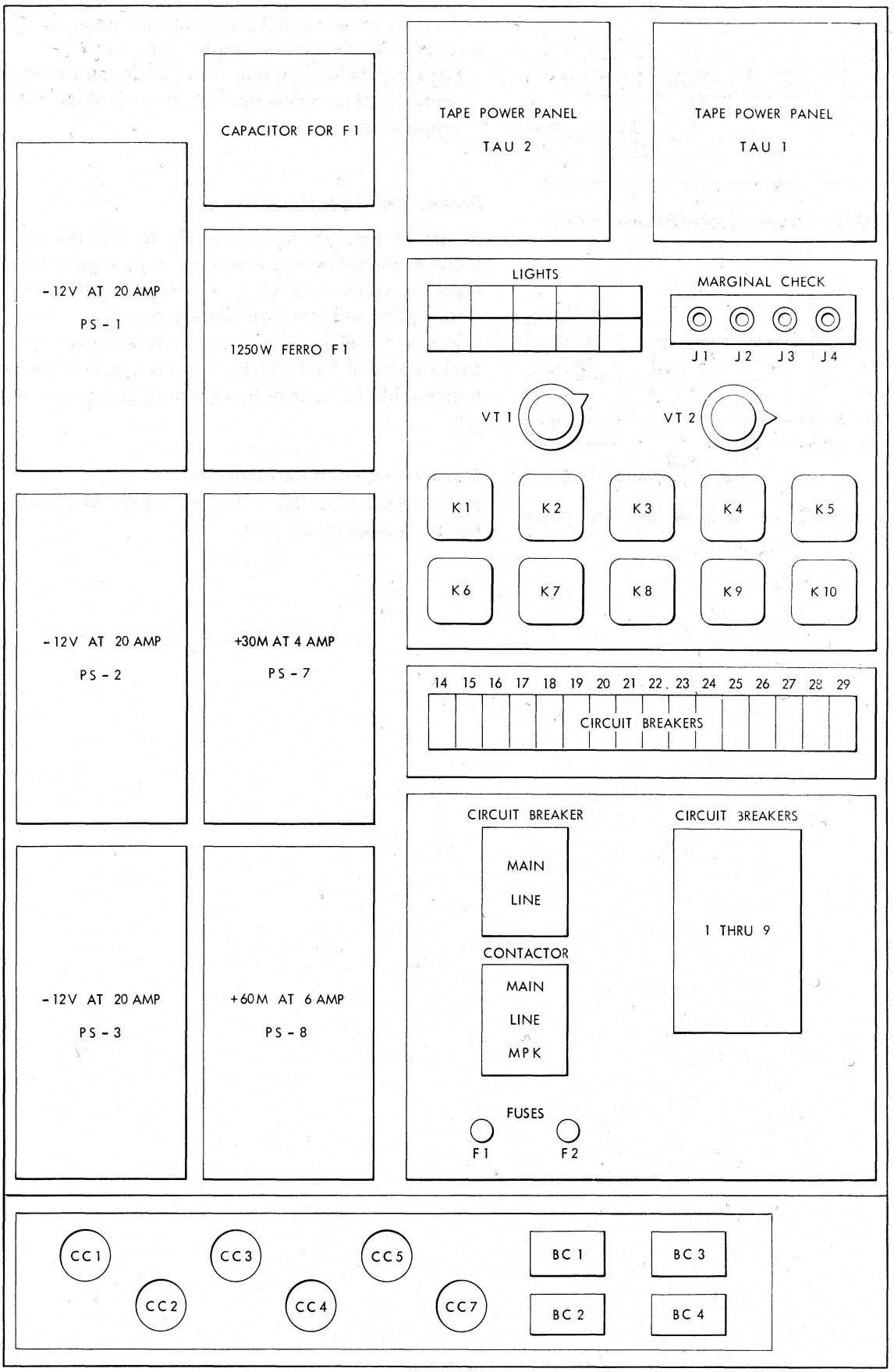


Figure 66. IBM 1411 A Frame Front

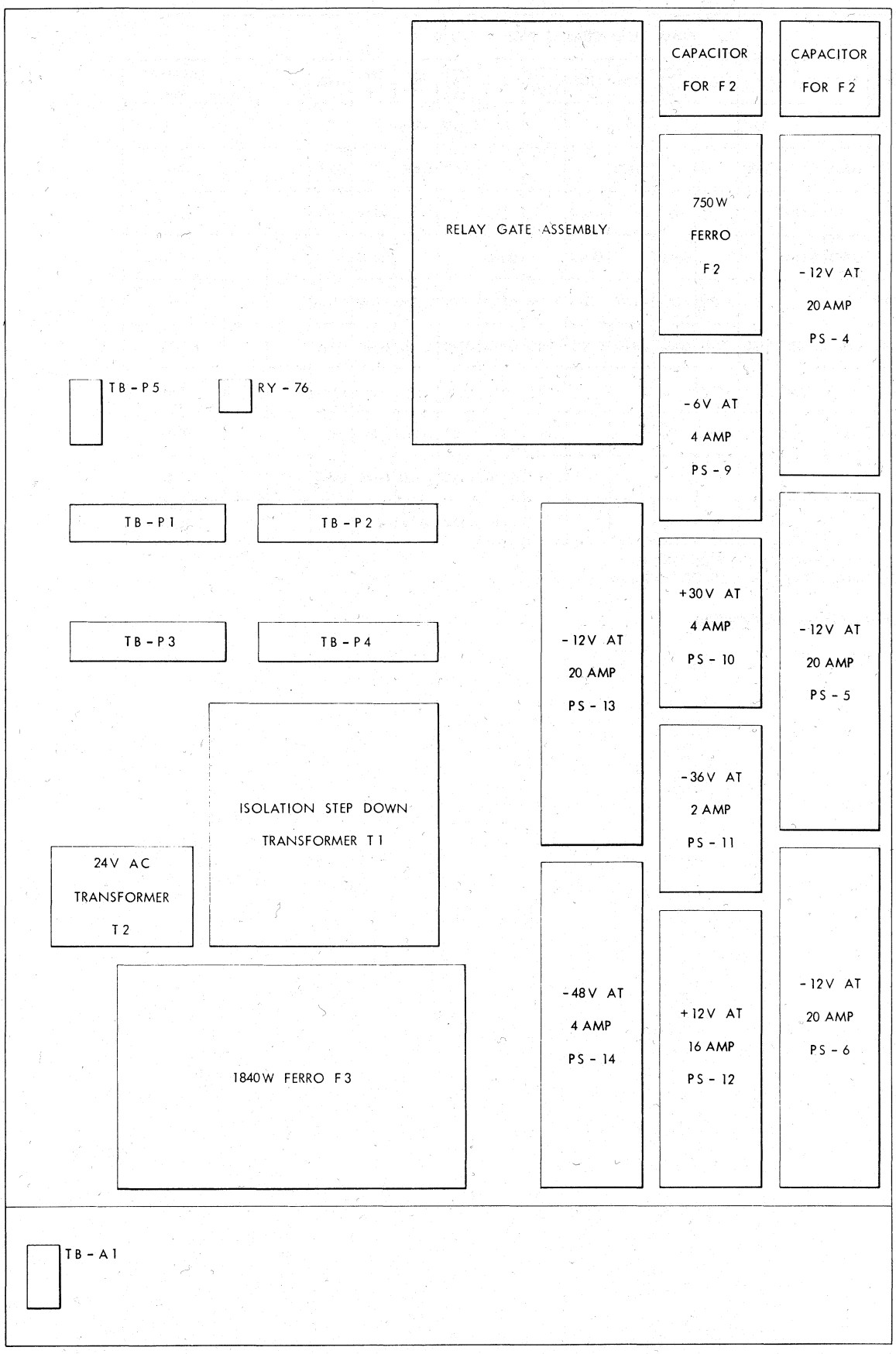


Figure 67. IBM 1411 A Frame Rear

	FRAME AND CHASSIS DESIGNATION																
LAMINAR BUS	11B2	11B3	11B4	11C1	11C2	11C3 11C4	11D1	11D2	11D3 11D4	14A1	14A2 14A3 14A4	14C *	14C **	14D			LAMINAR BUS
1-G	-12V			-12V			-12V				-12V	-12V		-12V			1-G
2-H	GND	GND	GND	GND			GND				GND	GND		GND			2-H
3-J		-12V	-12V			-12V		-12V		-12V			-12V				3-J
4-K		GND	GND			GND		GND		GND			GND				4-K
5-L	+12M			+12M	+12M	+12M	+12M	+12M	+12M	+12M	+12M	+12M	+12M	+12M			5-L
6-M	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND			6-M
7-N		+12M	+12M		-12V				-12V	+6V	+6V	+6V	+6V	+12V			7-N
8-P	-6V	-6V	-6V		GND				GND	-6V	-6V	-6V	-6V	-6V			8-P
9-Q										GND	GND	GND	GND	GND			9-Q
10-R										+12V	+12V	-20V	-20V				10-R

* = 1414C CHASSIS 4, 5, 6 AND ROWS E, F OF CHASSIS 3
** = 1414C CHASSIS 1 AND ROWS A, B, C, D OF CHASSIS 3

Figure 68. Frame and Chassis Designation

Logic Families

Saturated drift transistor resistor logic (SDTRL) and saturated drift transistor diode logic (SDTDL) increase circuit speeds economically. Although current-switching diffused-base transistor logic developed for STRETCH is faster than either SDTRL or SDTDL, it is not economically feasible for smaller systems. A fair comparison can be made, however, between complimentary transistor resistor logic (CTRL) and SDTRL. SDTRL provides increases in circuit switching and recovery times at approximately the same cost as CTRL.

SDTDL provides basic logic circuits in both high and medium speed ranges where cost varies linearly according to speed. The SDTDL family provides compatibility for a broad range of systems with a minimum of circuit types.

Although the IBM 1410 Data Processing System uses several families of logic, most of its circuits are SDTRL. Figure 69 illustrates the need for more than one family of logic.

To obtain an output at Q (Figure 69), simultaneous inputs to block 5 from blocks 4 and 8 are required. If the correct outputs from block 6 are available for only several microseconds, the circuit delays in path X must be overcome in the same time as those delays in path Y to condition block 5. This necessitates either the use of faster logic in path X or additional delay in path Y. Because additional delay would decrease the speed of the operation, higher speed circuits in path X are employed.

Automated Logic Diagrams

Automated logic diagrams (ALD's) aid in understanding various logic operations, simplify logic tracing, and locate circuit components. Standard blocks and symbols are used to represent specific circuit configurations. ALD's (printed out by the 704 and the 705) permit standardized diagrams between all personnel and plant locations.

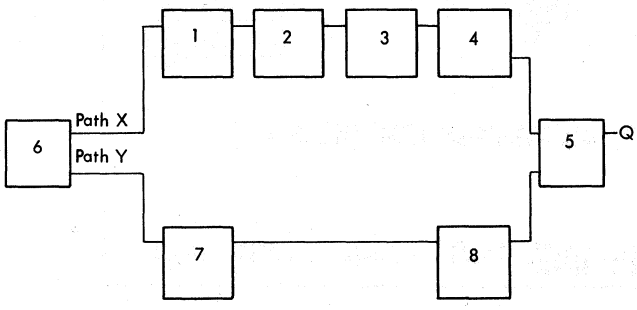


Figure 69. Two Logic Families in One Operation

PAGE LAYOUT

An automated logic diagram consists of page identification, edge information, logic blocks and their connecting lines, and an area for comments at the bottom of the page. Figure 70 shows a typical logic page from the 1410 System.

PAGE IDENTIFICATION

As shown in Figure 70, the following information is shown at the top of the systems page:

1. Page part number, which is used for ordering a specific page.
2. Title, which is a description of the logic contained on the systems page.
3. Machine number, which is the number assigned to a given frame or machine (e.g., 1411-CPU).
4. Logic page number, which is a seven-digit number assigned to the logic page.
5. Comments at the bottom of the page include listed edge connector locations used for the entry and exit lines on the logic page, and the area reserved for comments. Any pertinent information concerning the logic on the systems page is noted here. Engineering changes affecting the logic page are also shown in this location.

SIGNAL LINES

1. All lines entering or leaving a systems page are labeled and correspond to the symbol and sign of the logic block they connect. (Early 1410 ALD's show several blocks that contradict this general rule. These cases should be recognized as errors.)
2. Lines enter on the left side of the systems page and leave on the right side of the page.
3. If a line leaves a systems page and goes to several locations on another page, the line is usually distributed on the "to" page and not the "from" page.
4. If a line leaves a page and goes to several pages, but carries the same line name, it can be shown as in Figure 71.
5. When a line performs a function with the active

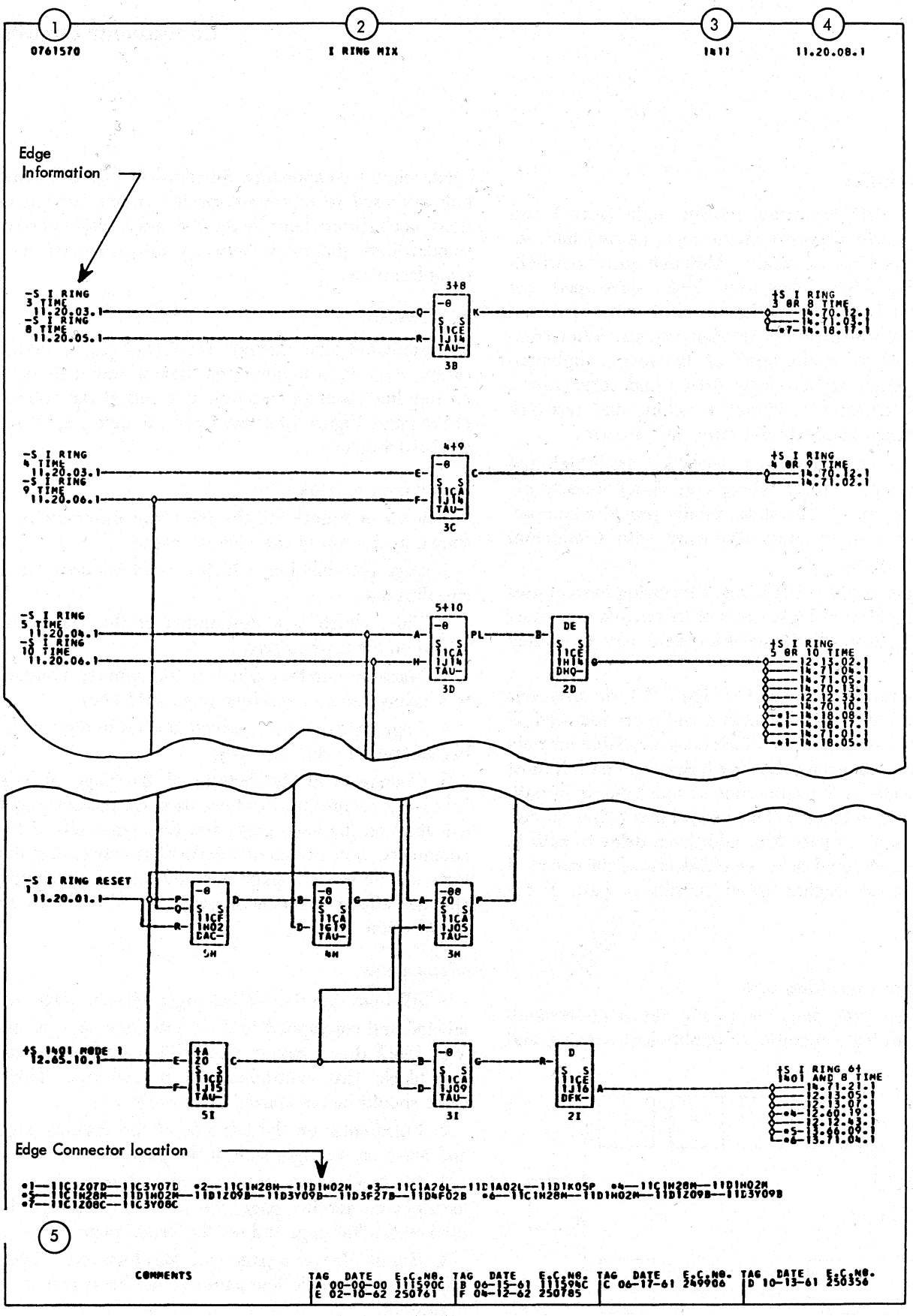


Figure 70. Typical 1410 Automated Logic Diagram

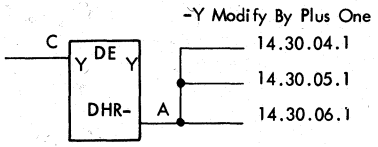


Figure 71. Multiple Outputs—Same Line Name

and inactive states, the two functions are described in the line name on the "from" page. (Active state of a line refers to that state required to produce the desired [active] output.)

EDGE INFORMATION

Edge information is located on the extreme right and left sides of logic pages. Edge information can consist of three 15 character lines that specify the input and output line names and the logic page from which the line has come or to which the line goes. On some ALD's the coaxial shield or twisted-pair reference wire of the signal line is shown entering or leaving a page. The letters "cs" for coaxial shield and "tw" for twisted-pair are used to indicate the coaxial shield or twisted-pair line.

EDGE CONNECTORS

When a signal or service wire enters or leaves a panel, it may be routed through an edge connector. Signal lines connected to edge connectors are indicated by a symbol and a number or letter located on an entry line or exit line. See Figure 70. These notations refer the reader to the bottom of the ALD page for actual edge-connector location and pin number.

REFERENCE DRAWING

All locations that identify core arrays, resistors, and other components mounted on a gate are given on a reference drawing. Signal lines on the systems pages refer to these drawings for locations. Reference drawings are easily identified by noting the logic page number. The seven-digit number always ends in zero for these drawings (xx.xx.xx.0).

LOGIC BLOCK

To simplify the systems pages, logic blocks are used to represent the basic electronic circuits of the machine. A basic electronic function is usually represented by a single block. Some functions, however, may require more than one block (e.g., triggers). When several circuits are located on one SMS card, each circuit is represented by a separate logic block. The size of the block allows for the printing of four characters across the box and for six vertical lines. The standard format of the logic block is shown in Figure 72.

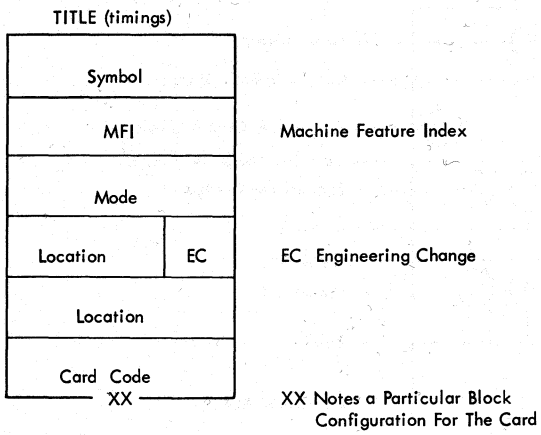


Figure 72. Logic Block Format

Title: Over each logic block a ten-character name can be printed. However, only special circuits such as triggers, latches, single shots, etc. are named. The units of time used in the title are abbreviated as follows:

Sec	Seconds
Msec	Milliseconds
Usec	Microseconds
Nsec	Nanoseconds

Functional Symbol: The symbol that appears on line 1 of the block consists of a sign (where used) and the standard letter(s) that represent the circuit.

Machine Feature Index: The machine feature index (MFI) code is shown on the second line of a logic block and indicates a circuit not normally used in the standard equipment. Two dots indicate a block used in the basic system.

Mode: The third line of a logic block contains symbols that indicate the input and output line levels that connect the logic block. Outputs from the upper half of the block indicate out-of-phase signals, while outputs from the lower half of the block indicate in-phase signals.

Card Location and Engineering Change Level: The first three positions on line four and all positions on line five of a logic block note the location of the SMS card on which the circuit is packaged. Figure 73 shows how a card can be located using the information on the logic block.

Card Code: Information on line six identifies the SMS card type on which the circuit represented by the logic block is located.

Logic Block Terminal Pins: Input, output, and tie-down terminal pins are indicated alphabetically in the two character spaces between the logic block and the input or output line. See Figure 74. The input and output pins are the terminals that are wired to the signal lines. Tie-down pins are terminals that are jum-

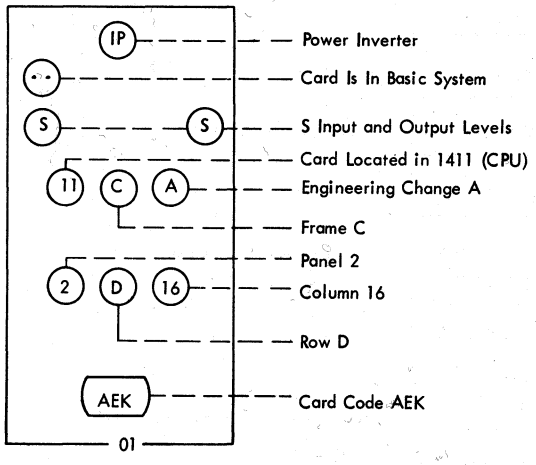


Figure 73. Typical 1410 Logic Block

pered by back panel wiring to input or output pins. Coaxial shields or twisted-pair reference wires tied to a terminal pin are shown in Figure 74.

EXTENDERS

To provide additional inputs to a logic block, extender cards are used. The symbol "E" is used in the extender block and dashed lines are used to show the extender card. See Figure 75.

LIMITERS

The blocks representing coupling networks or clamp diodes that limit or terminate the outputs of a circuit are connected to the driver output as shown in Figure 76. Limiters and terminators do not have output lines.

"DOT" FUNCTIONS

Under certain conditions, outputs of similar levels can be tied together to share a common load. This connection provides a second level of logic in the output circuit and is referred to as a "dot" function. When the "dot" function is performed, an additional letter is shown with the standard functional symbol to indicate the logic performed by the output circuit. Figure 77

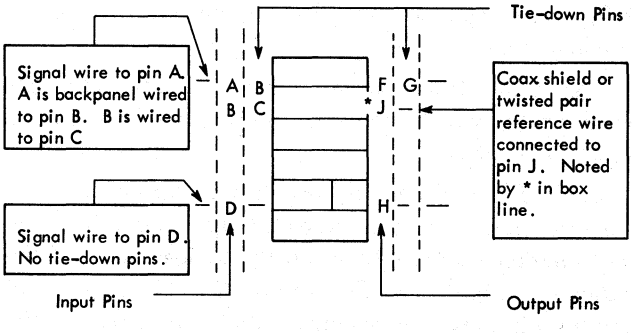


Figure 74. Logic Block Pin Connections

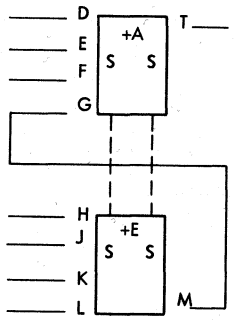


Figure 75. Extender Application

illustrates the block representations of the +AO and −OA DOT functions.

Line Levels

SDTRL (NOR) circuits, in most cases, are driven by S lines. The voltage excursion of an S line is approximately twelve volts with a positive level of 0 to −.65 volt and a negative level of −6.87 to −12.48 volts. Effective NOR circuit switching can occur only when the maximum load holds the output below −6.87 volts.

SDTDL (NAND) circuits are usually driven by Y lines. The voltage excursion of a true Y line is approximately six volts with a positive level of 0 to −.65 volt and a negative level of −5.81 to −6 volts. A Y line can be modified, however, to have a greater negative swing. Effective NAND circuit switching can be accomplished only when the maximum load does not allow the output to go above −5.81 volts.

The negative levels of S, Y, and modified Y lines are determined by the loads that their respective circuits drive. No-load allows the negative swings to fall to their most negative voltages.

Since an S line has a negative swing that varies between −6.87 and −12.48 volts, both NOR and NAND circuits can be driven by S lines. A true Y line can only

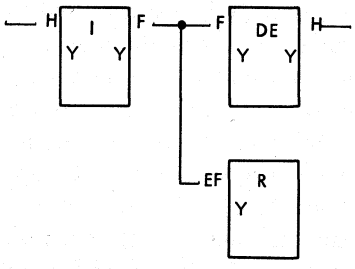


Figure 76. Limiters (Terminators)

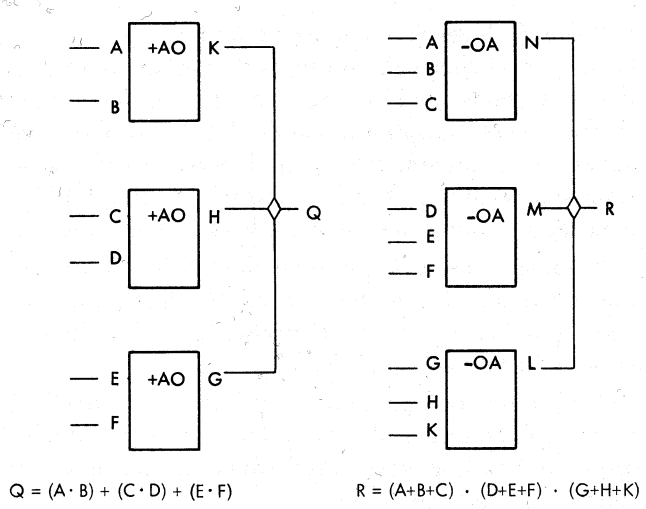


Figure 77. Dot Functions

drive NAND circuits since the negative level of a true Y line does not go below −6 volts. A modified Y line, like an S line, can drive NOR and NAND circuits since the negative level of a modified Y line varies between −5.81 volts and some value less than −6.87 volts. See Figure 78.

The symbols for true and modified Y lines are the same. Their identities can only be established by the functions that they perform. Only a modified Y line can drive NOR circuits effectively.

Most outputs from, and inputs to the 1411, 1414, and equipment that can be operated off-line, are current-mode C lines. A C line is an output from a line driver (usually a DED card) and must feed a standard cable terminator (usually a DFZ card). The current flow on a C line varies from approximately 0 ma (when the voltage level of the line is at its positive limit) to 13.5 ma (when the voltage level of the line is at its negative limit). The active and inactive states of a C line are referenced to the current flow on the line rather than to the voltage level of the line.

Characteristics of lines used in the 1410 System are listed in the table in Figure 79.

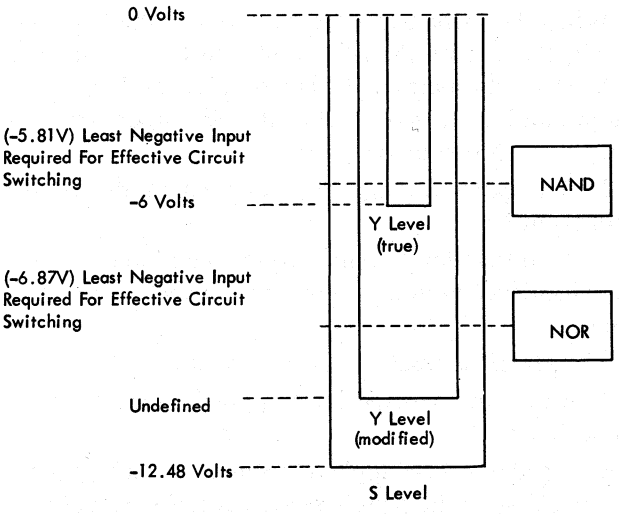


Figure 78. NOR and NAND Driving Requirements

Basic Circuits

Although logic families use different electrical components to perform operations, the conditions and end products of the operation do not change. The components only determine the time in which the function is accomplished. To illustrate this point, an AND function requires all active inputs to yield an active output. Only the delay in obtaining the output, after the input has been satisfied, varies.

The following paragraphs contain general transistor operation and fundamental circuit principles. The examples and descriptions included represent SDTRL and SDTDL circuits. Many of the principles, however, can be applied to CTRL circuits.

In the following examples, the most positive excursion of lines are called positive levels; the most negative excursion, the negative levels.

Positive AND — Negative OR (SDTRL)

A positive AND circuit requires all positive inputs to produce a negative output. A negative OR circuit re-

Circuit Type	Line Symbol	Voltage Reference	Voltage Levels (Nom)		Current Levels	
			Positive	Negative	Positive	Negative
Current Switching	+N	0	+0.8	- 0.8		
	+P	-6	- 5.2	- 6.8		
CTDL	+T	0	+6.0	- 6.0		
	+U	-6	0.0	-12.0		
CTRL	+R	0	+12.0	0.0		
SDTRL	+S	0	0.0	-12.48		
SDTDL	+Y	0	0.0	- 6.0		
Indicators	M		0.0	-36.0		
Relays	+W		0.0	+48.0		
Cores	+Z	-6	+6.0	- 6.0		
Special	+C				0 ma	13.5 ma

Figure 79. Line Characteristics

quires only one negative input to produce a positive output. See Figure 80.

The logic function (+A, −O) is performed by the input resistor network; the invert function, by the transistor. The base of the transistor is biased by the voltage developed across the input divider network. When +S levels are applied in coincidence to input pins A and B, a positive voltage is formed at the base of the transistor. The transistor is reverse-biased off as its emitter is returned to ground. Current flow from the −12V supply through the 1K collector resistor to the load divided network gives a −S output level. This condition satisfies the positive AND function.

When either input at pin A or B drops negative, the transistor becomes forward-biased on. Current flows through the transistor and raises the output to the +S level. This condition satisfies the negative OR function.

Negative AND — Positive OR — Inverter (SDTDL)

A negative AND circuit requires all negative inputs to produce a positive output. A positive OR circuit requires only one positive input to produce a negative output. An inverter produces an output level out-of-phase with the input level. See Figure 81.

Note the single level circuit in Figure 81 with none of the dashed line connections made. Five components make up the low speed inverter: R1, R2, R3, R4, and the transistor. When a negative level is applied to input pin C, the transistor conducts. The output at pin D is clamped to approximately 0 volt. When the input is negative, the output is positive.

When the input rises to 0 volt, the transistor cuts off because of the slightly positive bias caused by the voltage divider action of R2 and R3. With no external load on the circuit, the output level at D is −6V. External loading causes the output level to become more negative.

When "speed-up" components C1 and D1 are added to the single-level circuit, it becomes a high-speed block. Capacitor C1 shorts R2 during both positive and negative transitions, and the base of T1 receives much sharper level transitions. Diode D1 holds the base voltage at approximately ground potential when the transistor is cut off. Therefore, less time (turn-on delay) is needed to bring the transistor back into conduction.

In some cases, a single input diode (D2) is used in the invert circuit. In these cases, the input is at B, and input C is not used; otherwise, there is no difference in the operation of the circuit.

The circuit configuration of a positive OR is identical to the configuration of a negative AND. Input diodes are used; pin C is never used when an AND or an OR function is performed.

Assume that the inputs at pins A and B are negative. Diodes D2 and D3 may or may not be conducting, depending on the input voltages. With negative levels in, however, the R2/R3 junction will be negative. This negative voltage is felt at the base of the transistor; hence, the transistor is conducting. Pin D is held at approximately ground potential due to the low resistance of the transistor.

When the input at pin A rises to 0 volt, D2 is reverse-biased due to the positive voltage coupled through D3. The positive change is also coupled through C1 and/or R2, and the transistor is cut off. The output at pin D goes to approximately −6 volts. Therefore, a negative output level is obtained when the input at pin A or pin B is positive; a positive output level is obtained only when the inputs at pin A and pin B are negative.

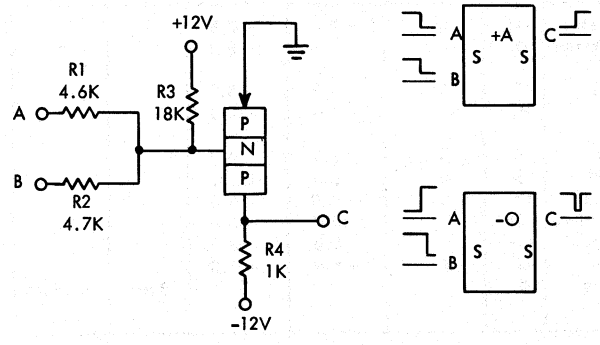


Figure 80. SDTRL Positive AND—Negative OR

Trigger (SDTDL)

The SDTDL bi-stable voltage mode trigger has two complementary outputs and up to six inputs. See Figure 82.

When the SDTDL trigger is set, the on output (pin A) is negative (−6V); the off output (pin B) is positive (0 volt). A reset condition yields a positive level at the on output and a negative level at the off output. The circuit is set in one of two ways:

1. A negative voltage level applied to the DC set input (pin D).

2. A positive level applied to the gate input (pin G) in coincidence with a positive shift at the AC set input (pin E).

The circuit is reset in one of two ways:

1. A negative voltage level applied to the DC reset input (pin C).

2. A positive level applied to the gate input (pin H) in coincidence with a positive shift at the AC reset input (pin F).

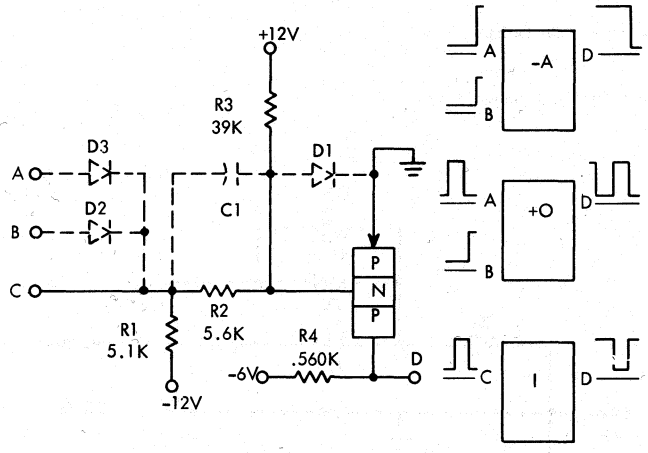


Figure 81. SDTDL Negative AND — Positive OR — Inverter (Single Level)

When a negative level is applied to the DC set input (pin D), resistors R8 and R6 form a voltage divider from −6 to +12 volts. The junction of R8 and R6 (base of T2) is negative; T2 is forced into conduction. The off output (pin B) is forced to approximately 0 volt. This potential is coupled through R3 to the base of T1. If the DC reset input (pin C) is positive (0 volt), the base of T1 is positive due to the +12 volts applied to R5 and the 0 volt applied to R3 (from the off output). The positive bias prevents the conduction of T1 and allows the on output to fall negative. The clamp diode D1 prevents the negative level from falling below approximately −6 volts.

When the DC set input (pin D) returns to 0 volt, the status of the trigger will not change. The base of T2 is held negative by the negative on output.

The off gate input (pin H) and the AC reset input (pin F) can now be used to reset the trigger. The gate input must be positive prior to (150 nsec) the arrival of the AC input. The positive level applied to the gate input may be obtained from the positive off output (self gating) or from some external circuit. (For complete self gating, pin B is connected to pin H, and pin A is connected to pin G.) Coupling diode D6 is reverse-biased before a positive level is applied to the off gate input (pin H); a +6 volts shift (−6 volts to 0 volt) through C3 will not pass through D6. With 0 volts at the off gate, however, a +6 volts shift (minimum +5.39 volts in 70 nsec) through C3 forward-biases D6 and drives the base of T2 positive. This action cuts off T2 so that the off output goes negative. Coupling from the off output to the base of T1 brings T1 into conduction giving approximately 0 volts at the on output. As before, cross-coupling holds the trigger in this state after the inputs are removed.

For binary operation (each input reverses the state of the trigger), self gating is employed, and the AC set input (pin E) and the AC reset input (pin F) are tied together. With these conditions, the AC shift is coupled to the base of the conducting transistor.

Emitter Follower (SDTRL)

The emitter follower circuit is shown in Figure 83.

The emitter follower circuit serves as a non-translating current amplifier that drives additional logic or branching circuits. Emitter followers also serve as buffer devices to match impedances or provide isolation.

Diode D3 conducts at all times to maintain a slightly negative potential at the cathode of D2. When the input at pin A is negative, the transistor conducts through R2, dropping the output to a negative level and cutting off D2. D1 is also cut off by the base-to-emitter drop of the transistor.

When a positive level is applied to the input (pin A), the transistor tends to cut off because the output line capacity (charged negative) tries to hold the emitter negative. Under these conditions, D1 conducts to provide a low impedance path to discharge line capacity. If the output tries to go above ground potential, D2 is forward-biased. Current flow from −12 volts through D2 to +12 volts holds the output below 0 volt.

Single Shot (SDTRL)

The SDTRL single shot (Figure 84) provides an output pulse of a definite time duration. With no inputs (pins A, B, and C positive), T1 is cut off and T3 is conducting. T3 is held in conduction by the voltage divider from −12 volts to +12 volts through D3.

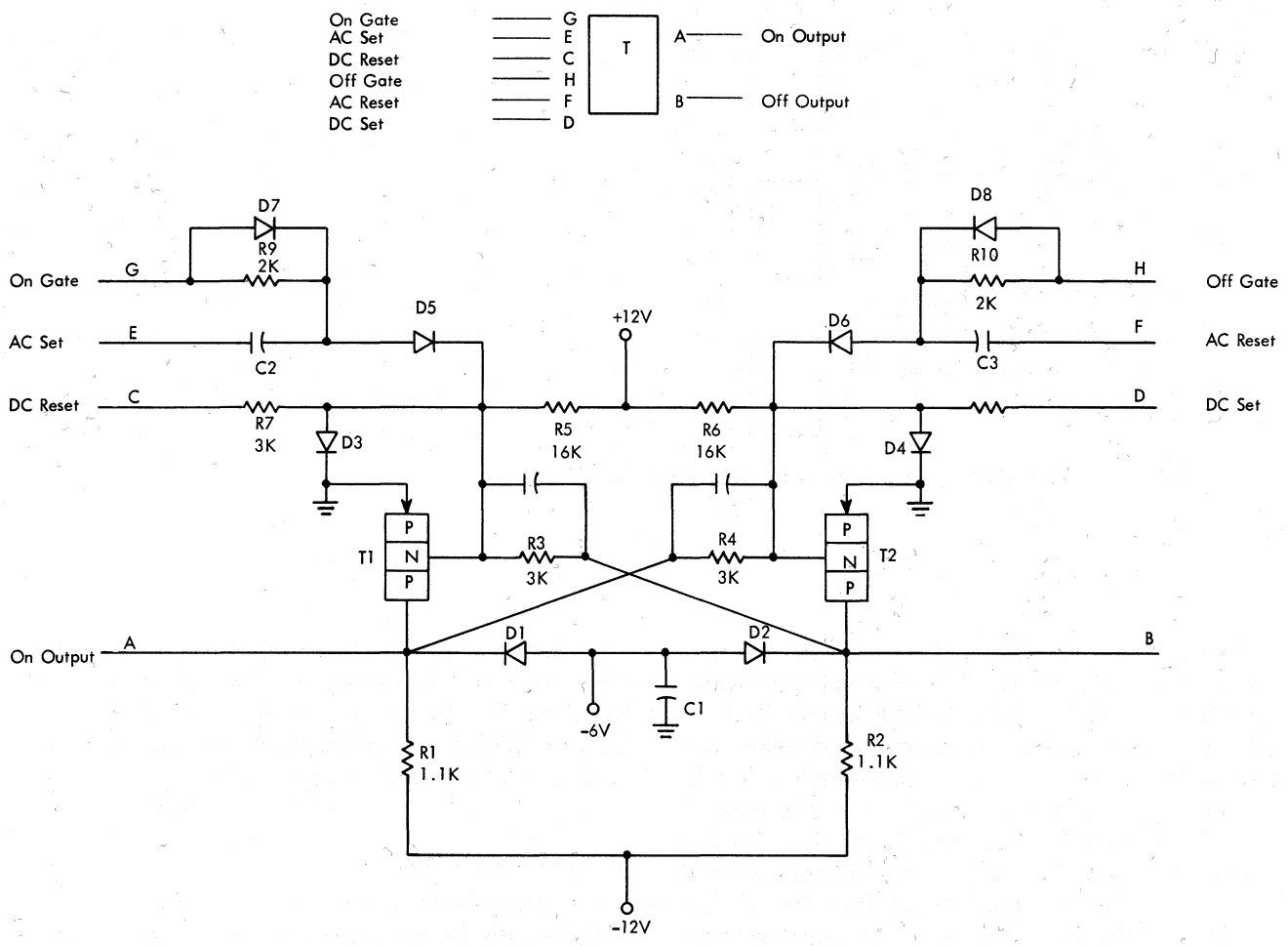


Figure 82. SDTDL Trigger

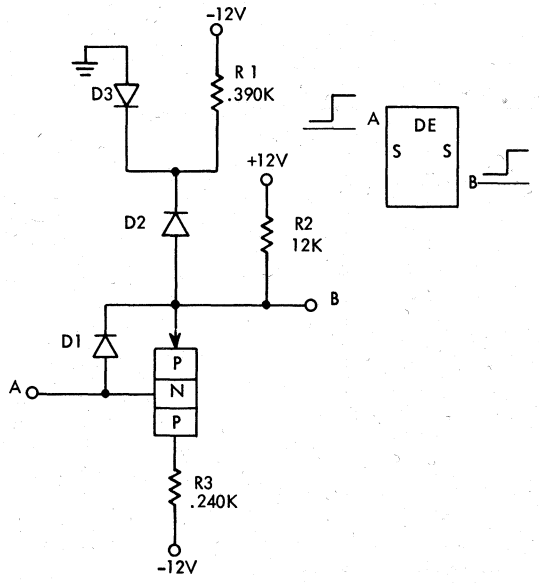


Figure 83. SDTRL Emitter Follower

If any input goes negative, T1 conducts. A portion of the T1 current comes from −12 volts through the timing resistors, timing capacitor, and D2. The resultant drop across the timing resistors reverse-biases D3 so that T3 is cut off by the voltage drop across D4. As the capacitor charges, the voltage across the timing resistors diminishes, and the cathode of D3 goes more negative. Eventually, the capacitor charging current through the timing resistors cannot hold D3 cut off. When D3 conducts, the voltage divider in the base circuit of T3 (between +12 volts and −12 volts) is re-established. T3 now conducts and the output returns to the positive level.

A negative level applied to the input (pins A, or B, or C) causes a negative pulse on the output. Because the charging current of the timing capacitor cannot flow when T1 is not conducting, T1 must be held in conduction for the timing duration of the circuit. This means that either the input level must be of greater duration than the output pulse, or the output must be tied back as one of the inputs.

When all inputs are again positive, T1 is cut off and the T1 collector and T2 base tend to drop to −12 volts. Current flows from −12 volts through T2, the capacitor, D3, and T3 (base-to-emitter) to ground. The timing capacitor is thus quickly charged to approximately 12 volts in preparation for the next timing cycle.

Drift Sense Amplifier

The drift sense amplifier (Figure 85) consists of a two-stage, direct-coupled differential amplifier, the output of which is rectified and delivered to a special Schmitt trigger. The input to the circuit is the sense line from a memory plane. The differential amplifier has a gain of 50 and a bandwidth of 5.2 MC. The amplifier has 32 decibels of dc feedback.

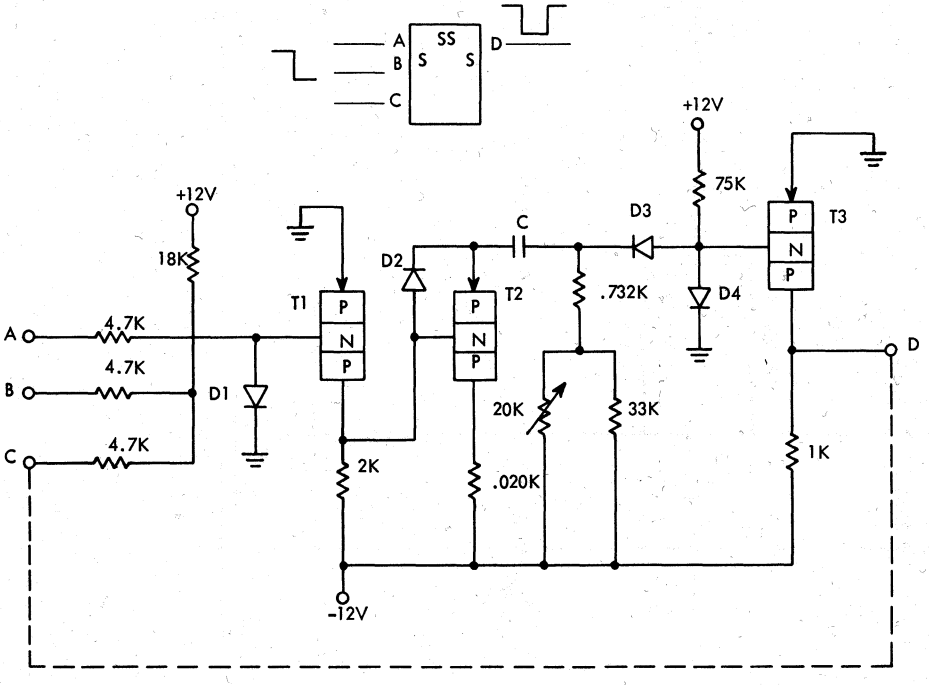


Figure 84. SDTRL Single Shot

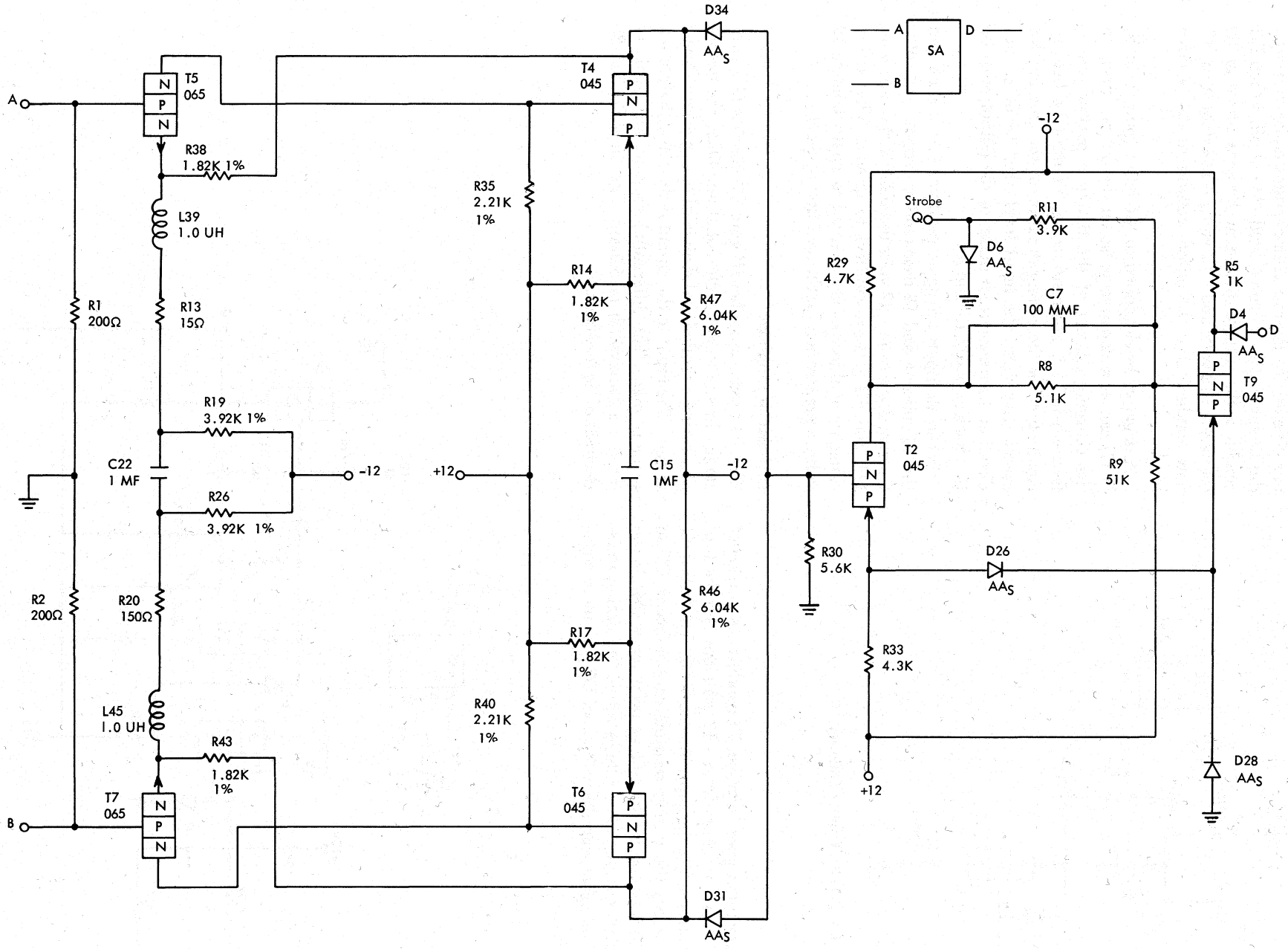


Figure 85. Drift Sense Amplifier

Transistors T4, T5, T6, and T7 comprise the differential amplifier and operate in a small signal region. Resistors R13 and R20 provide emitter degeneration. Resistors R38 and R43 provide dc feedback. Inductors L39 and L45 provide gain-phase correction at high frequencies. Capacitors C15 and C22 provide ac bypasses. Resistors R1, R2, R19, R26, R14, R35, R40, R46, R17, and R47 are bias resistors. Diodes D31 and D34 provide rectification, passing only negative signals. Transistors T2 and T9 make up the Schmitt trigger.

Transistor T2 is normally off and T9 saturated. The negative signal at the base of T2 turns T2 on. The collector of T2 swings positive, and the base of T9 follows, turning T9 off. As T9 turns off, however, it draws less current through D26, and the emitter of T2 goes positive forcing T2 further into conduction.

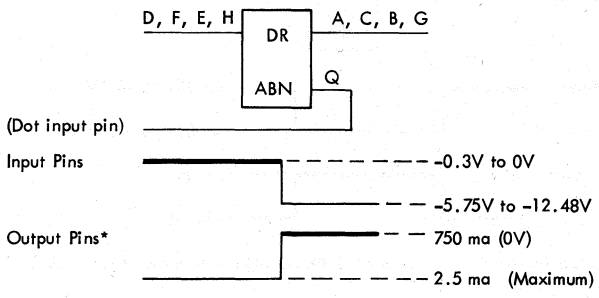
The strobe signal swings between −10 volts and ground and must be at its positive level when the Schmitt trigger is to be set. Capacitor C7 is a speed up device in the regeneration loop. Diode D26 and resistor R8 are also parts of the regeneration loop. Diodes D28 and D26 keep the emitter of T2 near ground when T9 is conducting, thus stabilizing the threshold of the Schmitt trigger. Diode D6 clamps the strobe signal. Resistor R11 couples the strobe to the base of T9. Resistors R5, R9, R29, R30, and R33 are bias resistors. Diode D4 is used to "OR" two sense amplifiers.

Card Descriptions

The component layouts of cards used in the IBM 1410 Data Processing System are included in the instruction automated logic diagrams and the SMS Card Diagrams (volumes 1 and 2). This section describes the general functions and input-output requirements of selected card types.

ABN

The functional coil drivers on the ABN card (Figure 86) are current drivers with maximum output capabilities of 750 ma. There are four circuits per ABN card.



*Circuit delay is not shown.

Figure 86. ABN Card

AEK

An inverting power driver on the AEK card (Figure 87) is used to drive up to 40 SDTRL circuits. There are three circuits per AEK card.

When a circuit on the AEK card is "dotted" with another circuit, pin E, G, or B is used as one of the two inputs to the circuit. The inverted output is available at pin C, A, or H.

CD--

The CD-- card (Figure 88) consists of 3 three-way nontranslating circuits used for repowering and level setting. Each circuit performs a basic logical function (+A, −O) and inverts the S input signal.

CRZV

The CRZV card (Figure 89) houses four one-way NPN circuits. Each circuit on the card translates an S level input to an out-of-phase T output. Extender pins N and B permit additional inputs to control two circuits on the CRZV card.

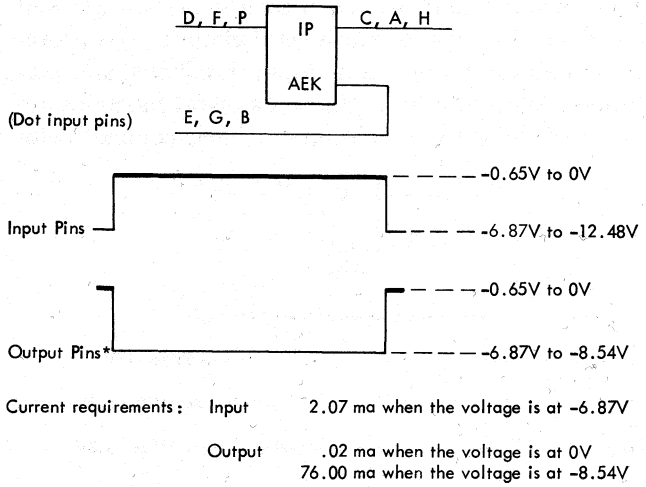
DBX

The drift sense amplifier card (Figure 90) consists of a two-stage, direct-coupled differential-amplifier, the output of which is rectified and delivered to a special Schmitt trigger. A sense line and sense strobe from a memory plane are inputs to the card.

The differential amplifier has 32 decibels of dc feedback and a gain of 50. The bandwidth of the amplifier is 5.2 MC.

DEA

The indicator driver on the DEA card (Figure 91) provides the necessary current to illuminate a 10 ESB indi-



*Circuit delay is not shown.

Figure 87. AEK Card

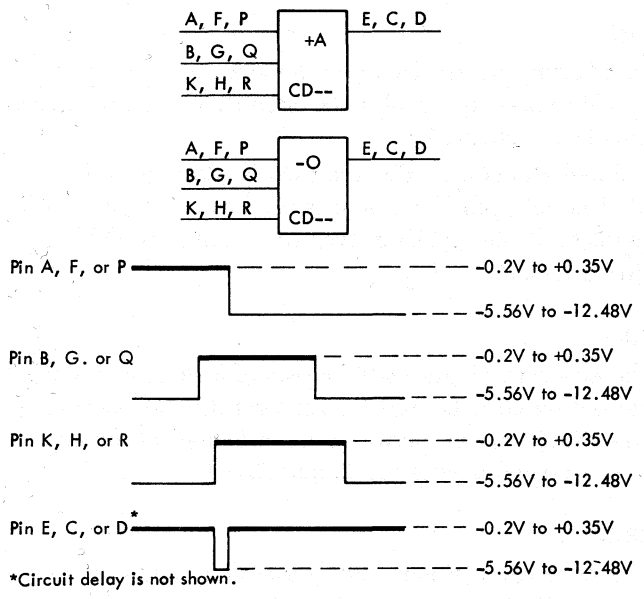


Figure 88. CD Card

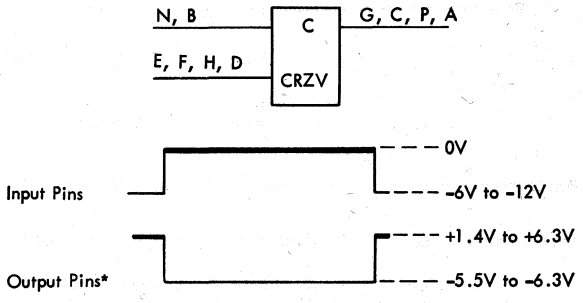
cator when the input to the driver is negative. There are six circuits per DEA card.

DED

The circuit on the standard cable driver (DED) card (Figure 92) accepts an SDTRL input and converts it to a C level to drive a transmission line with 91 to 120 ohms characteristic impedance. The line must be terminated with a standard cable terminator card. There are four circuits per DED card.

DEF	**DEJ**	**DGT**	**DGV**	**DGY**
DEG	**DEK**	**DGU**	**DGW**	**DGZ**
DEH	**DEL**		**DGX**	**DHA**

The SDTDL high and low speed circuits on these cards (Figures 93 and 94) accept negative inputs to perform −AND invert functions. When their collectors are tied common with other similarly used circuits, +OR operations following the −AND input functions are performed. With positive inputs, +OR invert functions are executed. When the collectors are tied common with



*Circuit delay is not shown.

Figure 89. CRZV Card

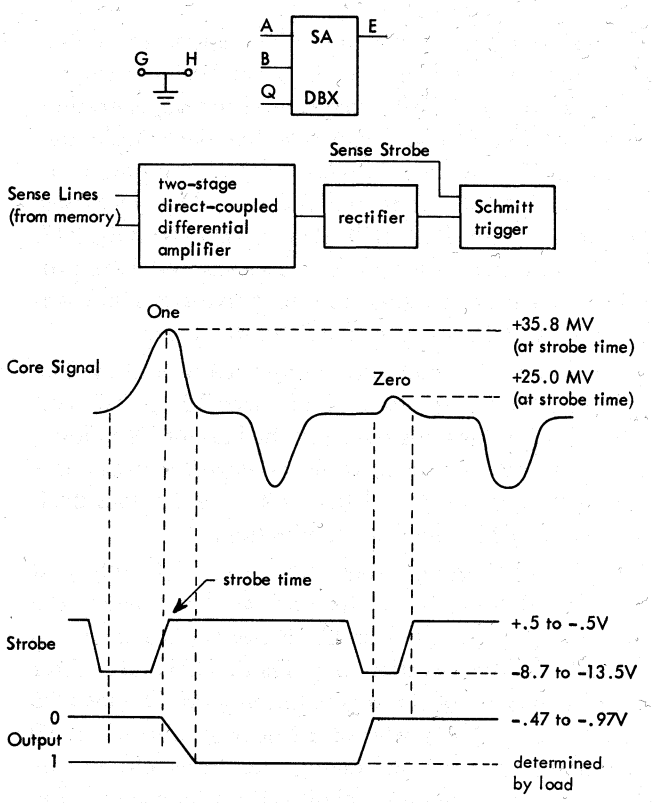


Figure 90. DBX Card

other similarly used blocks, −AND operations following the input +OR functions are performed. The circuit can also function as a latch.

The circuit arrangements on each of these cards differ in:

1. the number of inputs required to produce an active output
2. the speed at which the operation is performed
3. some can be "dotted" (collector load resistors), others cannot.

The fundamental principles of −AND and +OR operations can be applied to each card.

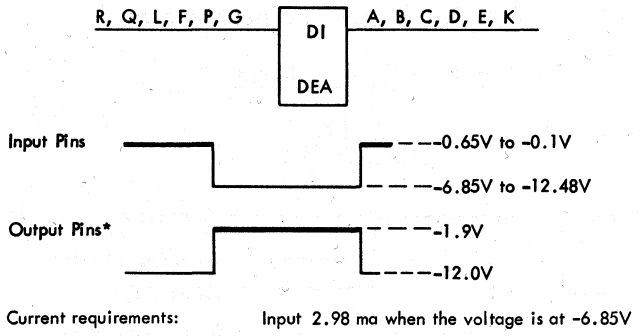
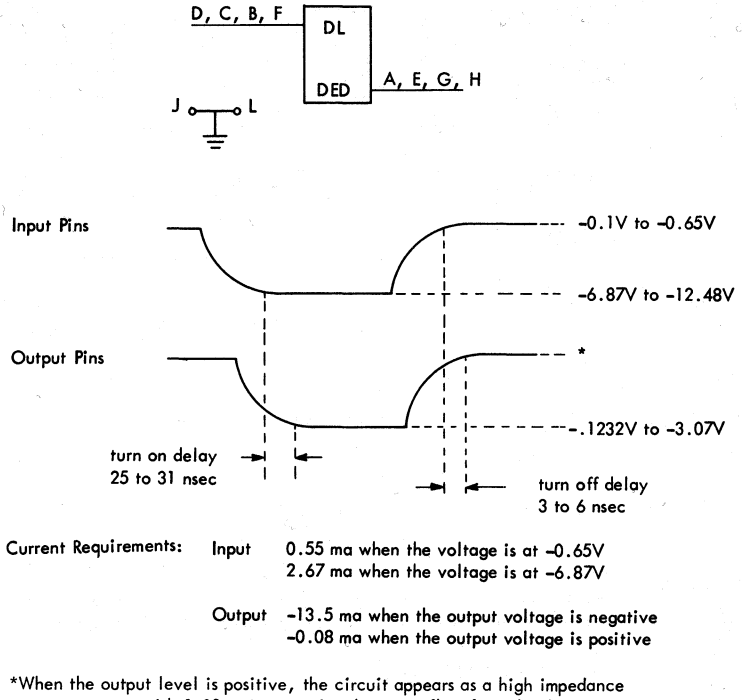


Figure 91. DEA Card



Current Requirements: Input 0.55 ma when the voltage is at -0.65V
2.67 ma when the voltage is at -6.87V

Output -13.5 ma when the output voltage is negative
-0.08 ma when the output voltage is positive

*When the output level is positive, the circuit appears as a high impedance current source with 0.08 ma conventional current flow from the driver.

Figure 92. DED Card

DEM

An SDTDL bi-stable voltage mode trigger is located on the DEM card (Figure 95). The trigger may be used in binary operation with both ac inputs common, or it may be used with separate ac inputs. The ac inputs respond to positive voltage shifts. The gates are conditioned by positive levels. The dc set and reset inputs require negative levels. The gates can either be driven sparately or tied to their respective collectors. The dc set and reset inputs are tied to ground when not in use.

Gate levels must be up for 150 to 200 nsec before the set pulse arrives (Figure 96). The set pulses must swing positive at least 5.16 volts in 70 nsec. A noise pulse that swings 1.5 volts or more on a set input in 20 nsec may change the trigger state.

DEQ

The SDTRL multiple unit package #3 on the DEQ card (Figure 97) consists of a +AND (−OR) driving a power inverter. There are three circuits per DEQ card. From one of the three circuits, the output from the input +AND (−OR) function is available.

Card	Circuit Speed	Number of Inputs	Collector Load	Circuits per Card
DEF	high	2	Yes	4
DEG	high	2	No	4
DEH	high	3	Yes	3
DEJ	high	3	No	3
DEK	high	2	Yes	2
DEL	high	2	No	2
DGT	low	2	Yes	4
DGU	low	2	No	4
DGV	low	3	Yes	3
DGW	low	3	No	3
DGX	low	5	Yes	2
DGY	low	5	No	2
DGZ	low	10	Yes	1
DHA	low	10	No	1

Figure 93. High and Low Speed SDTDL Circuits

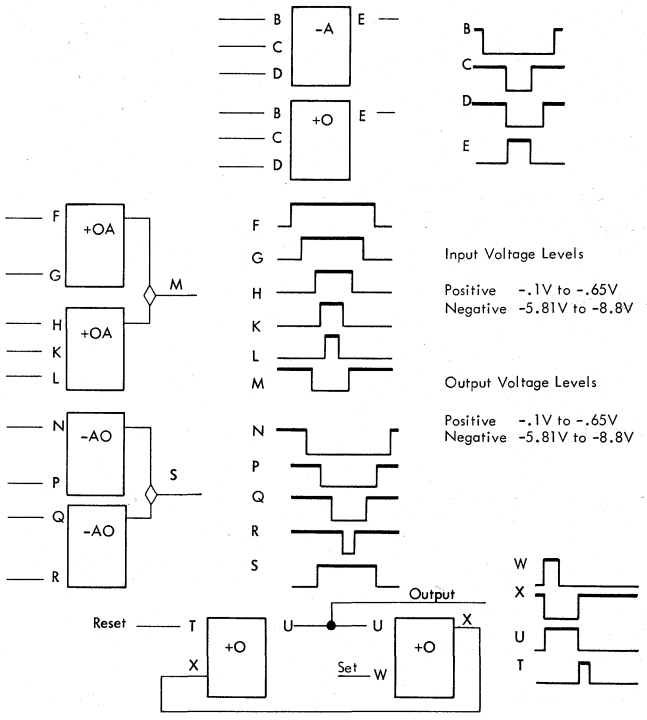
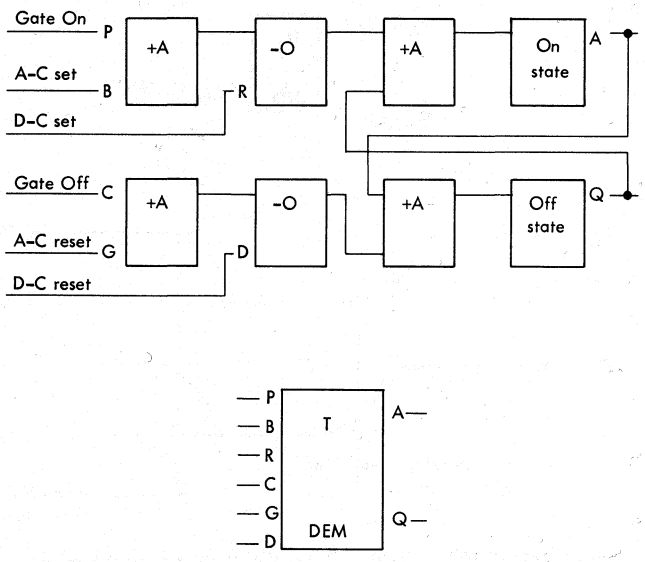


Figure 94. SDTDL Circuits



Pin A is positive when the trigger is on; negative when the trigger is off.
Pin Q is positive when the trigger is off; negative when the trigger is on.

Figure 95. DEM Trigger

DEY

The SDTRL multiple unit package #10 on the DEY card (Figures 98 and 99) consists of a drift binary trigger with both the ON and OFF outputs connected to low power inverters. An isolated +AND (−OR) circuit with three inputs is also available on the DEY card. The second level diagram represents the general operation of the trigger-inverter circuit.

DEZ

The AC sets for the on and off states of the drift binary trigger on the DEZ card are common (Figure 100). Each state must be gate gated separately, however. The second level diagram represents the general operation of the trigger when all of its inputs are used. (See Figure 101 for timings.)

DFK

The circuit on the DFK card is an emitter follower that powers several logic loads without inverting the input signal (Figure 102). There are six circuits per DFK card.

DFS

The SDTRL low power inverter on the DFS card (Figure 103) is used to provide drive for up to ten SDTRL logic blocks. Five circuits are located on a DFS card. The collector outputs of up to three low power inverters can be "dot-OR'ed" if one of the inverters has a collector load resistor (one input on pin Q or P).

DFV

The X-Y memory driver circuit on the DFV card (Figure 104) provides a portion of the drive current necessary to switch a core in the load sharing matrix switch.

DFW

The DFW card (Figure 105) packages a memory driver inhibit circuit. A −AND function at the input of the circuit must be satisfied to meet the necessary driver input condition.

DFY

On a DFY card is located a drift power gate circuit that gates current from four X-Y drivers through switch cores. The circuit has a +AND function at its input. When simultaneous positive levels are applied to input pins A and B (Figure 106), a negative output level is available at pin D.

DFZ

A standard cable terminator circuit is packaged on the DFZ card. The circuit provides compatibility with any standard cable driver, and the proper termination for any standard transmission cable. There are four identical circuits on one DFZ card (Figure 107).

DGK

The 370 nanosecond tapped delay line on the DGK card (Figure 108) is driven by an "S" level from a low power inverter. The delay line drives one low power noninverting driver. The delay line is tapped at 310, 330, and 350 nanoseconds. The output is terminated by a

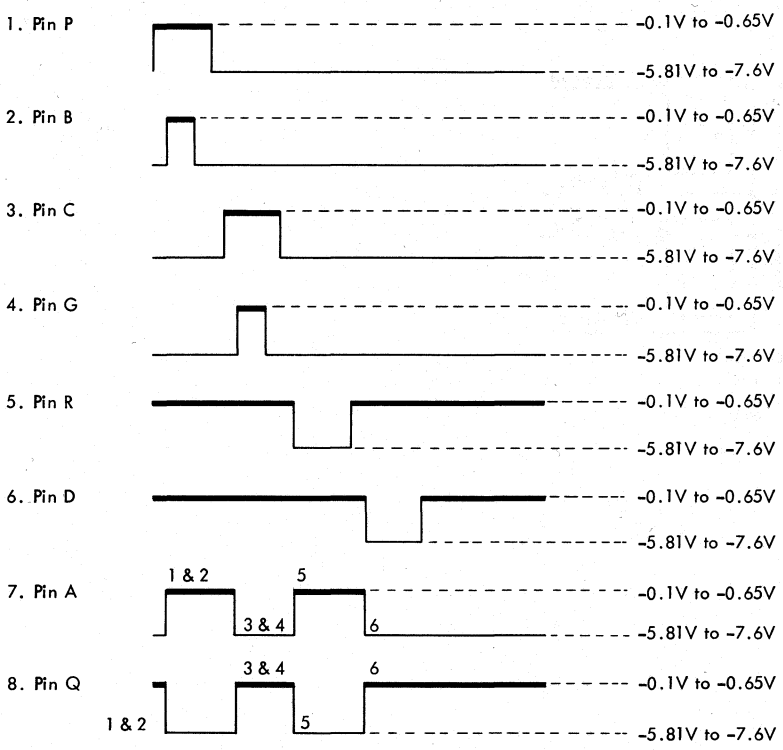
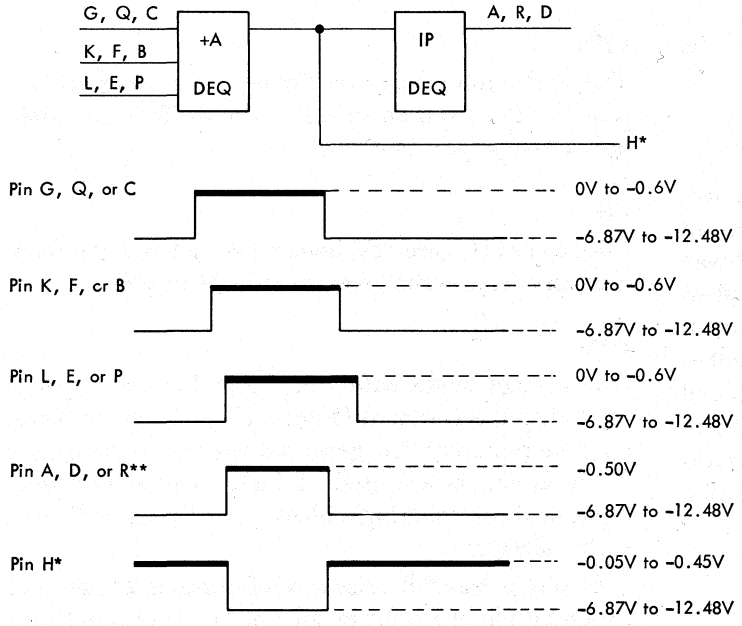
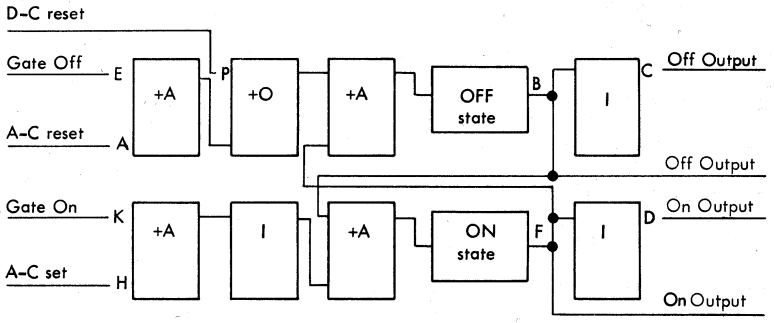


Figure 96. DEM Timings



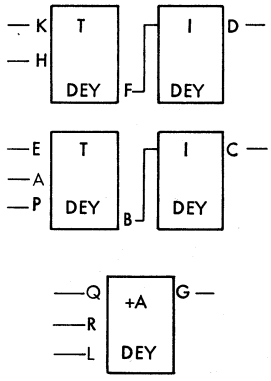
*Output is available only if input pins G, K, and L are used.
** Circuit delay is not shown

Figure 97. DEQ Card



Pin B is positive when the trigger is off; negative when the trigger is on.
Pin F is positive when the trigger is on; negative when the trigger is off.

EQUIVALENT TRIGGER-INVERTER CIRCUIT ON DEY CARD



ALD REPRESENTATIONS OF CIRCUITS ON DEY CARD

Figure 98. DEY Card

resistor equal to the characteristic impedance of the delay line.

DGM

The DGM card (SDTDL) multiple package #1, modified, packages two identical circuits. Each circuit makes up a latch configuration (Figure 109) that drives two 2-way SDTDL blocks. The "set" sides of the latches consist of double level diode logic, and the "set" diode appears at the output of the memory sense amplifier card (DHM).

A negative input to the "set" pin (F) of the latch will turn the latch on. A negative level will be applied to pin 2. If either input at pin Q or R is negative, a positive level will appear at the corresponding output pin. A positive level at pin L will reset the latch.

DHE

The SDTRL single shot circuit on the DHE card (Figure 110) provides an output pulse of a desired duration independent of the input pulse width. A timing range of 0.15 usec to 65 msec is available.

DHN

The drift strobe driver on the DHN card (Figure 111) provides the required signal to strobe 32 sense amplifiers at the proper time.

KG

The KG card (Figure 112) houses two isolated, but identical, CTRL read-write voltage mode #2 drivers.

TAM

One voltage mode, saturating drift, binary trigger is located on the TAM card (Figure 113). The second level diagram represents the general operation of the trigger when all inputs are used. A logic inverter and two-input or three-input logic blocks may be "dotted" with each collector.

A noise pulse with a rise time of less than 20 nsec and an amplitude of 2 volts or greater on an ac input may cause the trigger to change states if the gate input is positive. A noise pulse that allows the dc set input to shift 2 volts or more below ground may also cause the trigger to switch states. Figure 114 shows TAM timings.

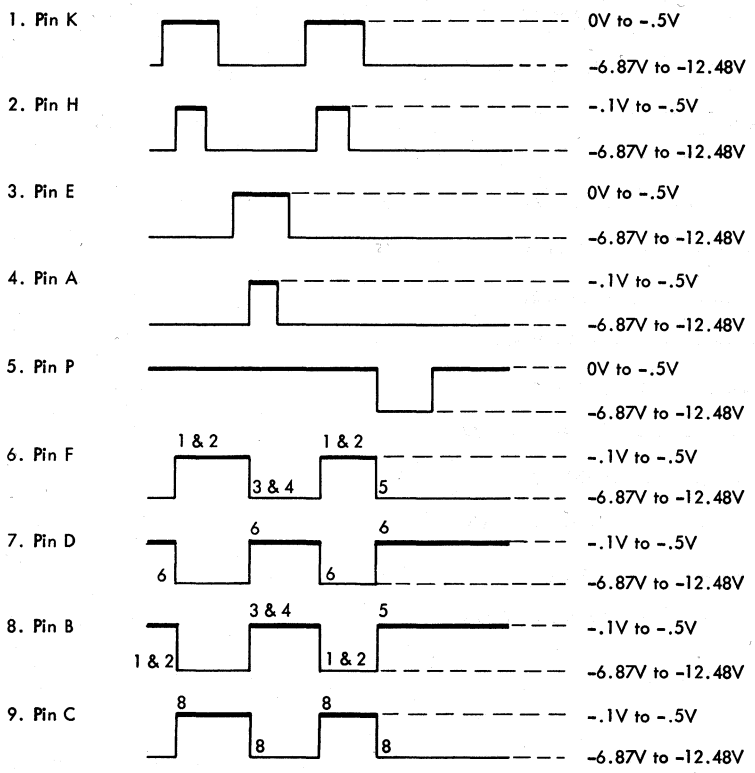
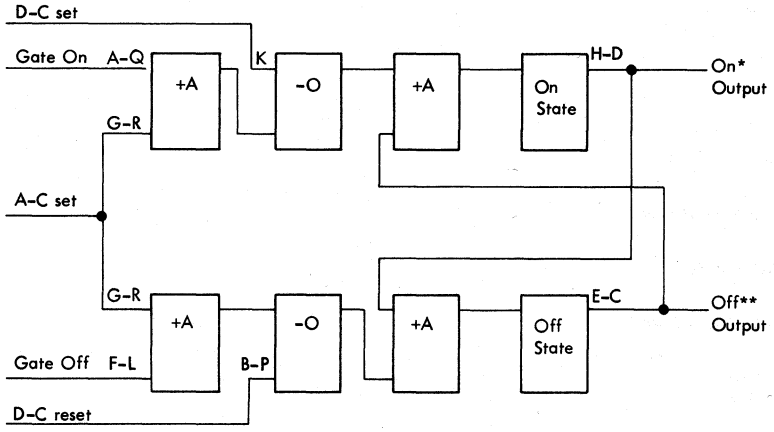
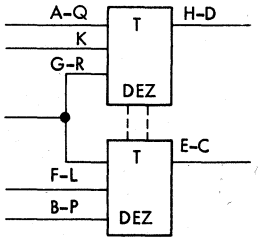


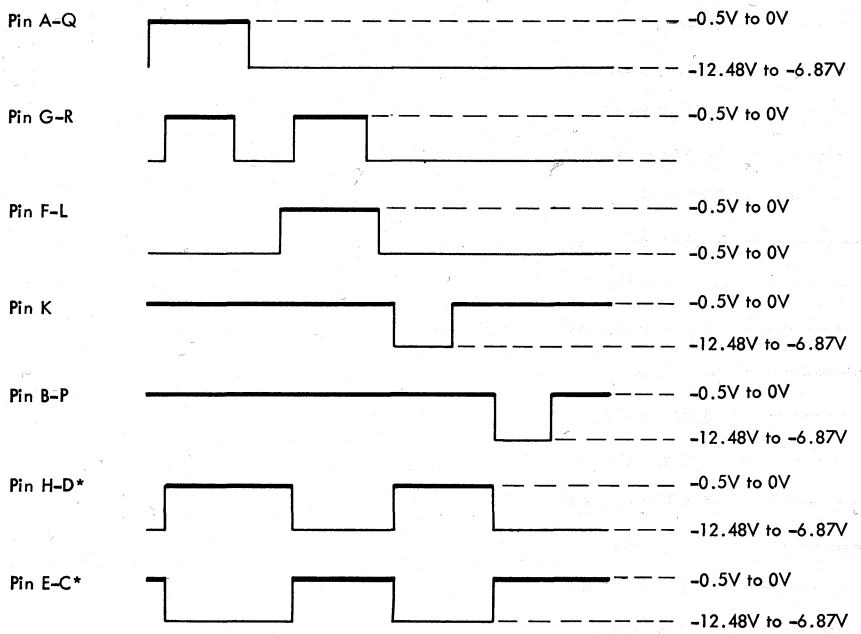
Figure 99. DEY Card Timings





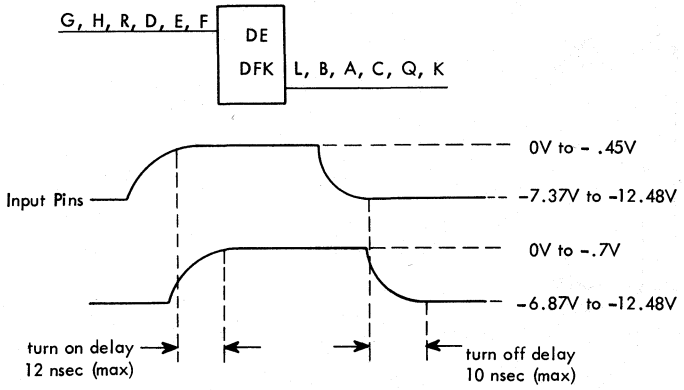
* On output is positive when the trigger is on; negative when the trigger is off.
** Off output is negative when the trigger is on; positive when the trigger is off.

Figure 100. DEZ Card



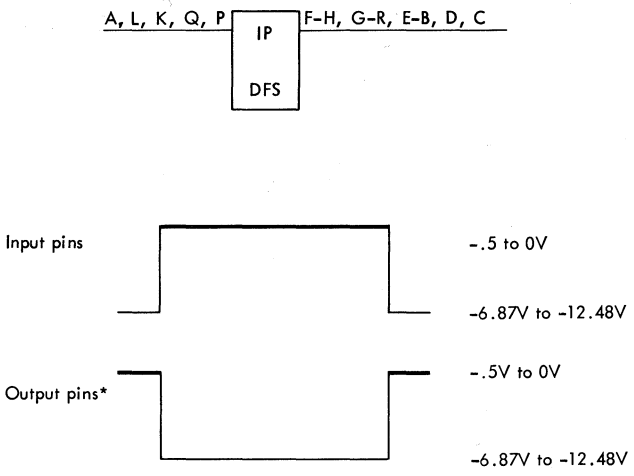
*Circuit delay is not shown.

Figure 101. DEZ Timings



Current requirements: Input 0.61 ma when the voltage is at -7.37V
Output 14.8 ma when the voltage is at -6.87V

Figure 102. DFK Card

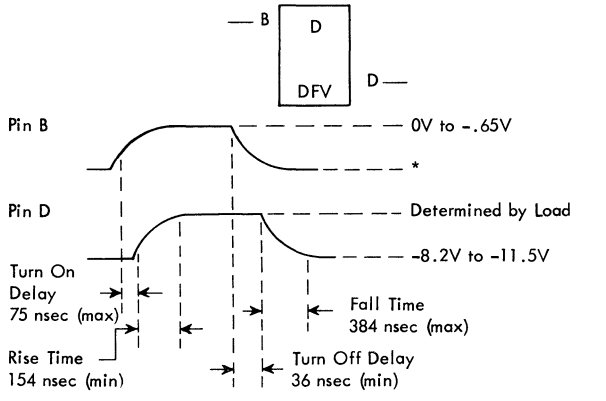


Current requirements: Input - .67 ma when the voltage is at -.50V
- 2.68 ma when the voltage is at -6.87V

Output -14.43 ma when the voltage is at -6.87V
-48.30 ma when the voltage is at -.50V

*Circuit delay is not shown.

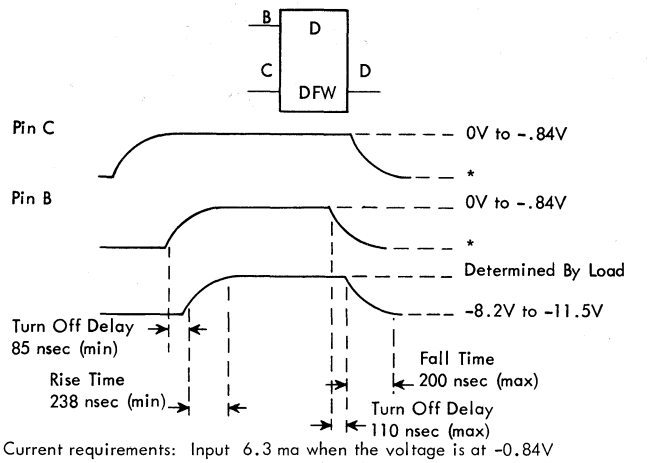
Figure 103. DFS Low Power Inverter



Current requirements: Input 12 ma when the voltage is at -.65V
0 ma when the voltage is at negative level

*When the input level is negative, the driving transistor (which has no load resistor) is off.

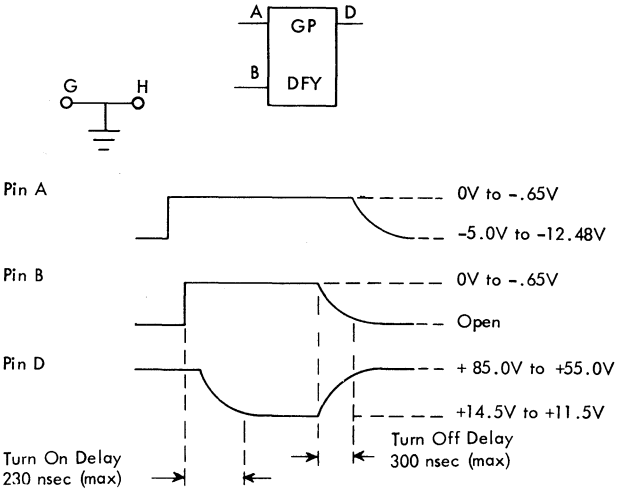
Figure 104. DFV Memory Driver



Current requirements: Input 6.3 ma when the voltage is at -0.84V
0 ma when the voltage is at negative level

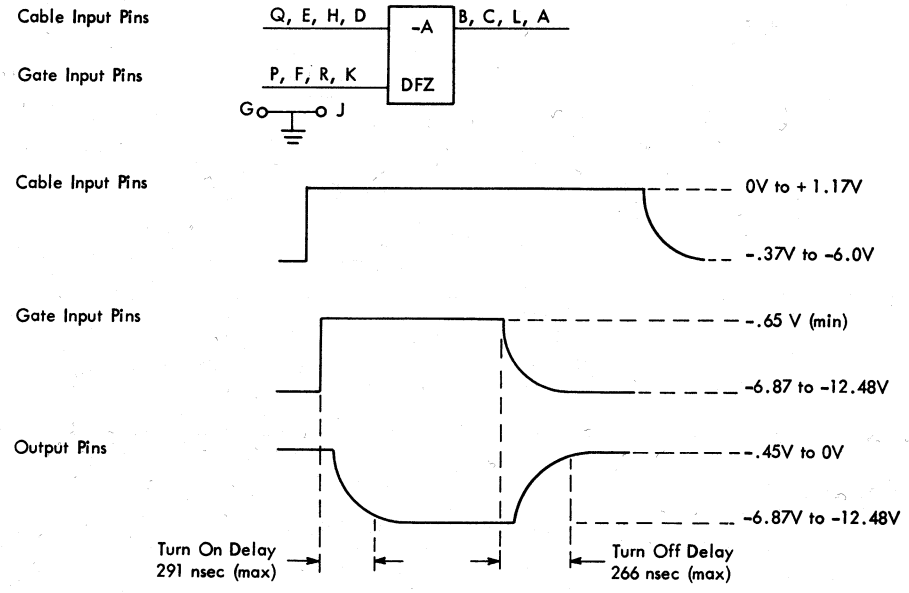
*When the input levels are negative, the circuit is off and has no load resistor.

Figure 105. DFW Memory Inhibit Driver



Current requirements: Input (Pin A) 0 to 1 ma when the voltage is at -.65V
3.9 ma when the voltage is at -5.0V
(Pin B) 6.3 ma when the voltage is at -.65V
0 ma when voltage is at negative level

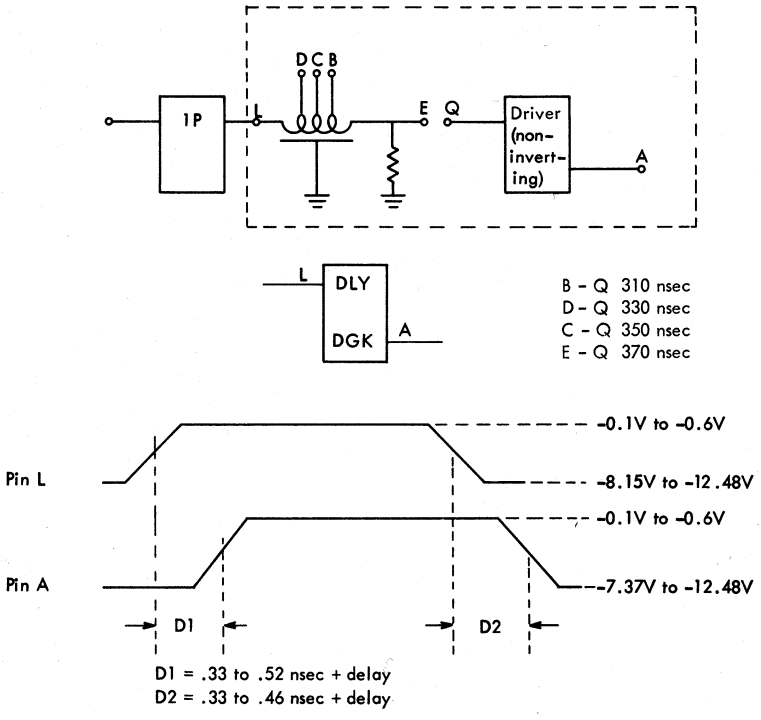
Figure 106. DFY Power Gate



Current requirements: Input (cable input) 13.44 ma when the voltage is at -.37V
(gate input) 1.13 ma when the voltage is at -6.87V

Output 4.44 ma when the voltage is at -6.87V

Figure 107. DFZ Cable Terminator



Current requirements: Input 8.37 ma when the voltage is at -8.15V
Output 0.61 ma when the voltage is at -7.37V

Figure 108. DGK Delay Line

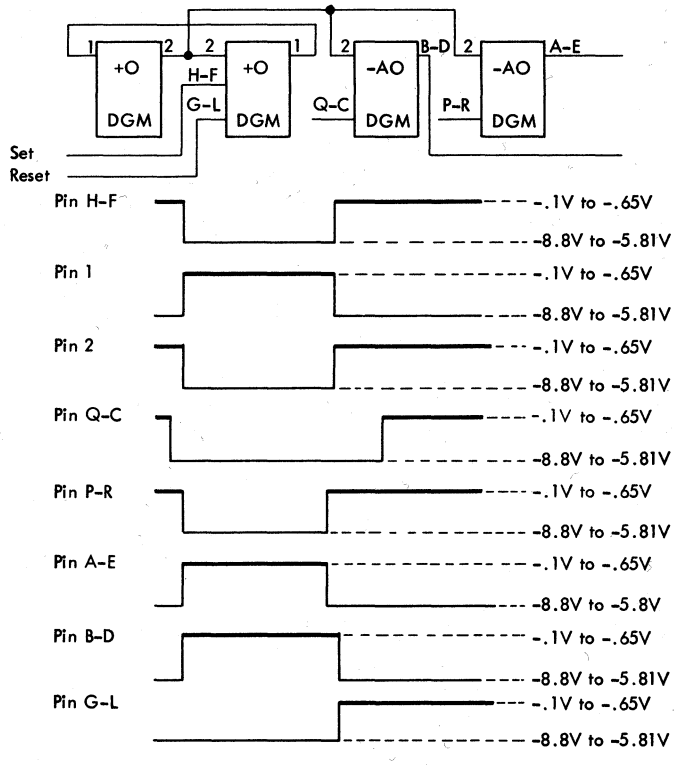
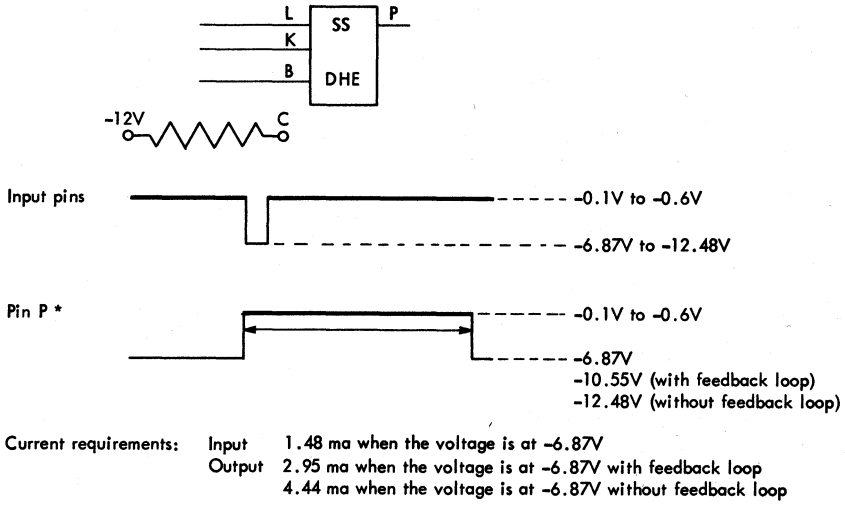


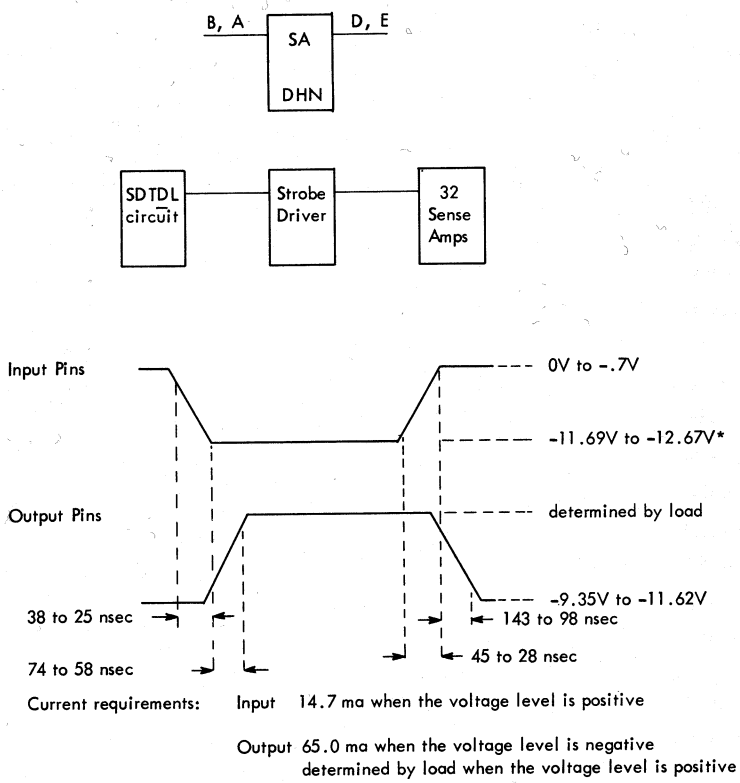
Figure 109. DGM Card



Current requirements: Input 1.48 ma when the voltage is at -6.87V
Output 2.95 ma when the voltage is at -6.87V with feedback loop
4.44 ma when the voltage is at -6.87V without feedback loop

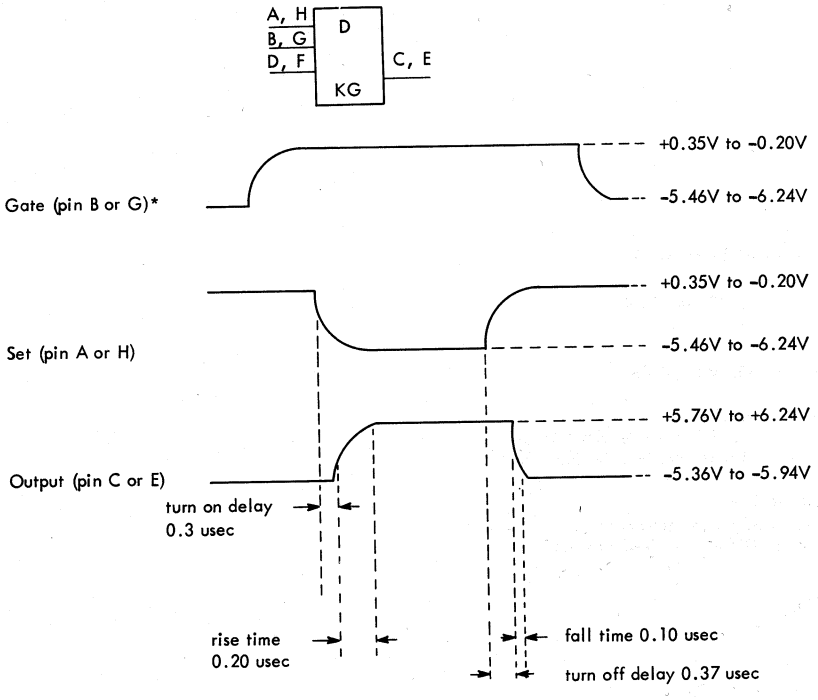
*Circuit delay is not shown

Figure 110. DHE Single Shot



*The driver is a SDTDL block without a collector load.

Figure 111. DHN Card



*Gate input must be conditioned 0.5 usec before the set pulse is applied.

Figure 112. KG Card

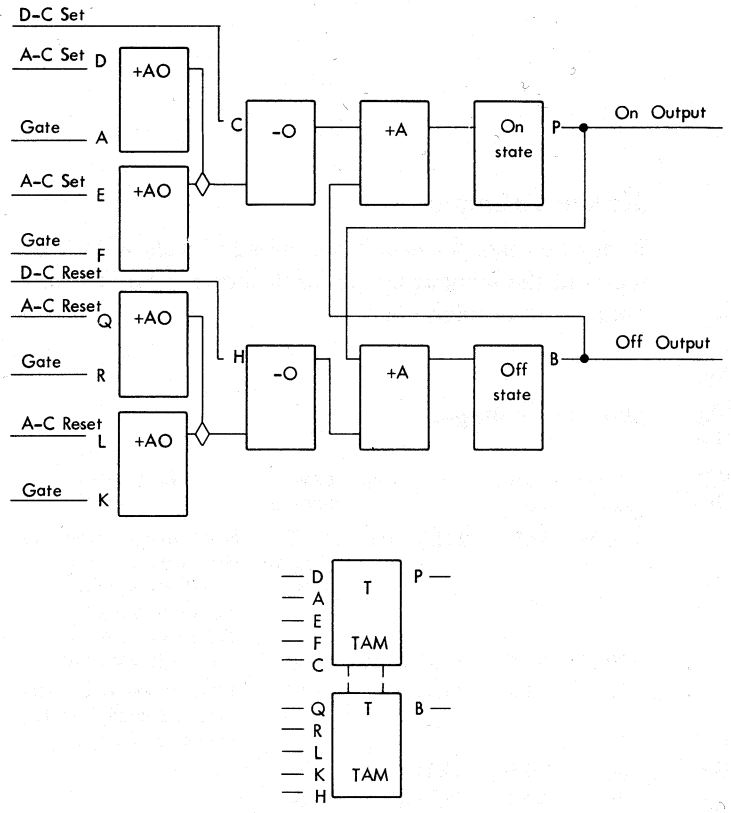


Figure 113. TAM Logic

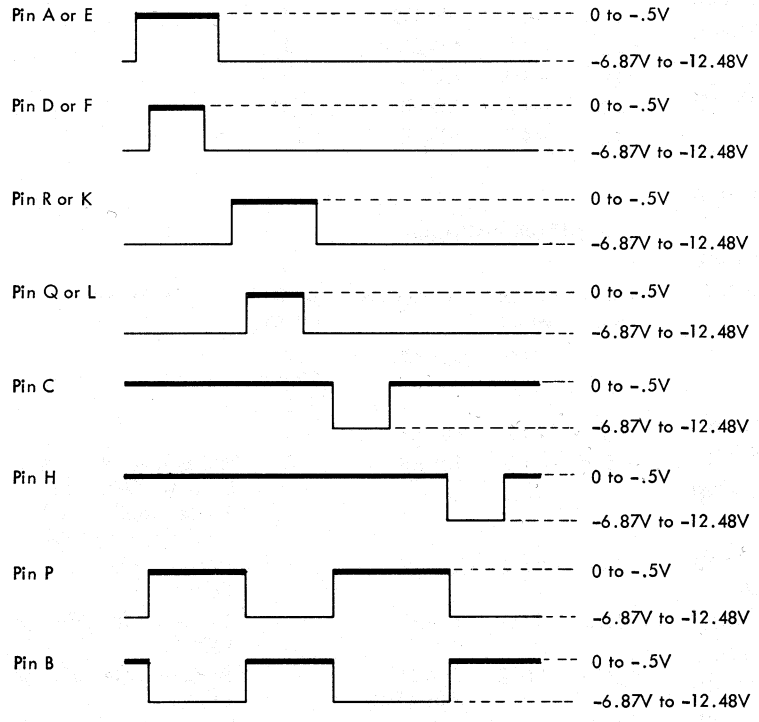


Figure 114. TAM Timings

IBM 1411 CE Console

Address Display

Manual controls on the CE console (Figure 115) display the addresses in the registers for checking purposes. A rotary switch selects the particular register for display. After the switch setting selects the register, pressing the address-display switch on the CE console starts the move and display operation. The selected-address register is gated out to the address bus and set into the STAR, where the latch outputs turn on the indicator.

Another control impulse, which the address-display switch initiates, inhibits the other registers that are not selected by the rotary address-selector switch.

B Character Select Switch

The B character select switch permits gating out any one of the four positions of the B data register to the B channel indicator for visual checking. The switch must be reset to normal position (1) for normal operation or a B character-select error occurs (Systems 15.30.01).

Portable Controls

The portable controls plug into the six-position pin jack on the CE panel to provide a portable control for cycling the 1411 CPU.

This control permits single-cycle operation to be executed for CE checking purposes.

Start: The start key operation is normal.

Stop: The portable stop key parallels the console stop key in function.

Reset: The reset key is on the portable control unit. The control that this key initiates is parallel to the console computer-reset function.

Address Stop and Scope Sync

The storage-address stop switch and sync-control rotary switches (Figure 116) provide manual control for selecting a particular address location to initiate a stop or a scope sync signal.

A toggle switch controls the address stop for ON or OFF operation. The sync hub is effective at all times.

The address-selection switches are effective through the four low-order positions of the storage address register. The stop, or scope signal, can be further conditioned by a scan-gate switch (Figure 117) for the scan mode desired (Systems 14.17.17-19).

System Voltages

Every two months check the voltage levels with a dc meter at the laminar bus on each frame. Re-adjust any voltage out of tolerance.

IBM 1411 Voltages

VOLTAGE	TOLERANCE	LOCATION	POWER SUPPLY	REMARKS
+30 M	±4%	11B3 J01L	7 (Figure 118)	Each storage unit has the +30 and +60 volts set at an optimum working voltage. Tolerance is ±4% from this voltage.
+60 M	±4%	11B3 E01Q	8	
+30	±4%	TB11-B9	10	TB11 is located under the core array on the card side of 1411.
−36	±4%	TB11-B8	11	
−48	±4%	TB11-B1	14	
+12 (Marg.)	±4%	LB (All frames)	12	PS12 also feeds +12 to sense amps. This is not marginal.
− 6	±4%	LB-B8 (Figure 3)	9	
−12	±4%	LB-B1	1	
−12	±4%	LB-C1 & D1	2	
−12	±4%	LB-D3	3	
−12	±4%	LB-B3	4	
−12	±4%	LB-C3	5	
−12	±4%	LB-C7	6	
−12	±4%	LB-D7	13	

IBM 1414A Voltages

VOLTAGE	TOLERANCE	LOCATION	POWER SUPPLY	REMARKS
− 6	±4%	LB-A8	1 (Figure 119)	
+ 6	±4%	LB-A7	2	
−12	±4%	LB-A3	3	PS3 is used with 1414 IV only. Otherwise, A3 is wired to A1 (−12 from 1402-2).
−12	±4%	LB-A1		PS on right side of 1402-2.
+12 M	±4%	LB-A5		PS on left side of 1402-2.
−20	20-22	14A2 A28 (J-R)		PS on left side of 1402-2.
−60	58-60	1402-2 CE Panel		PS on rear of 1402-2.

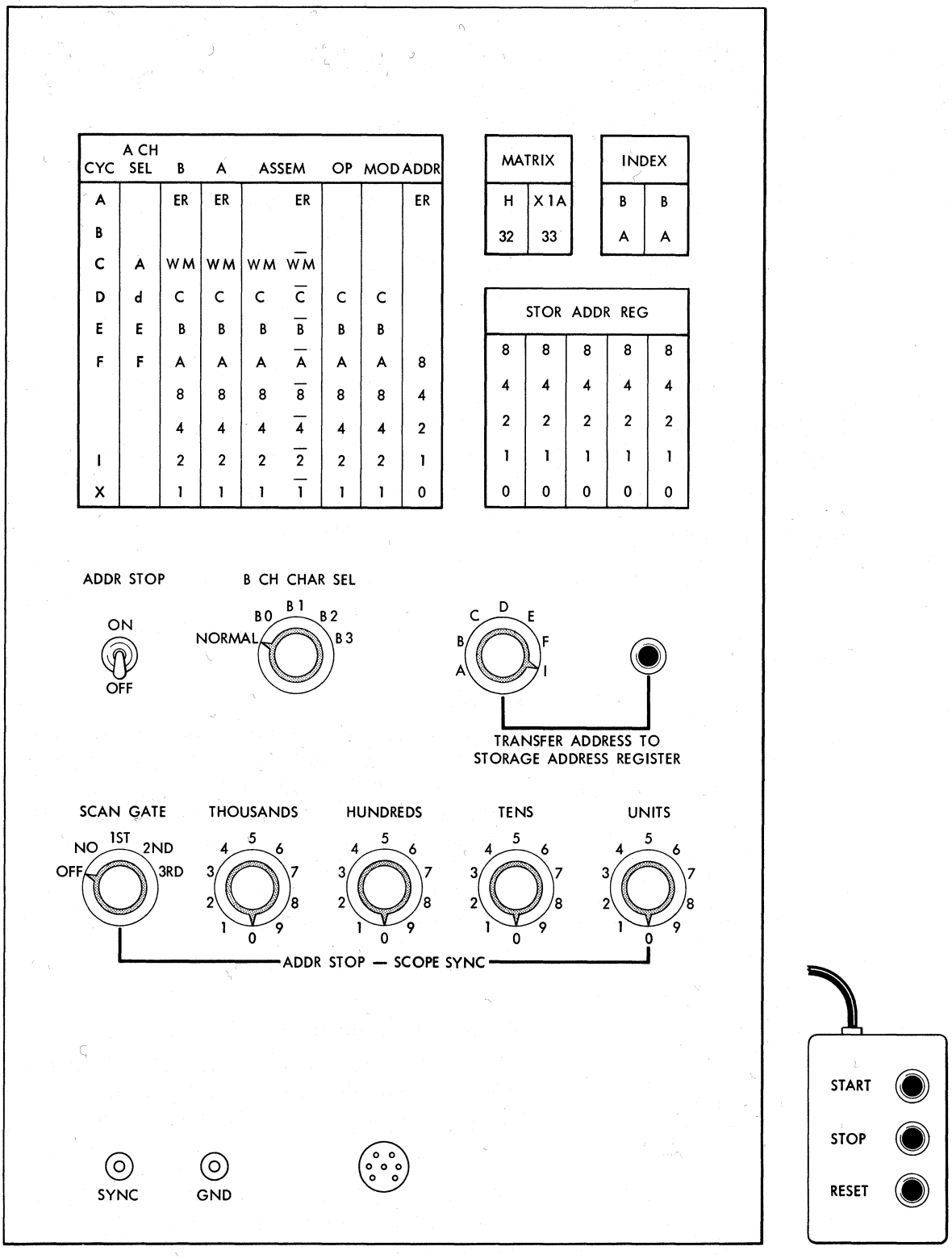


Figure 115. IBM 1411 CE Panel

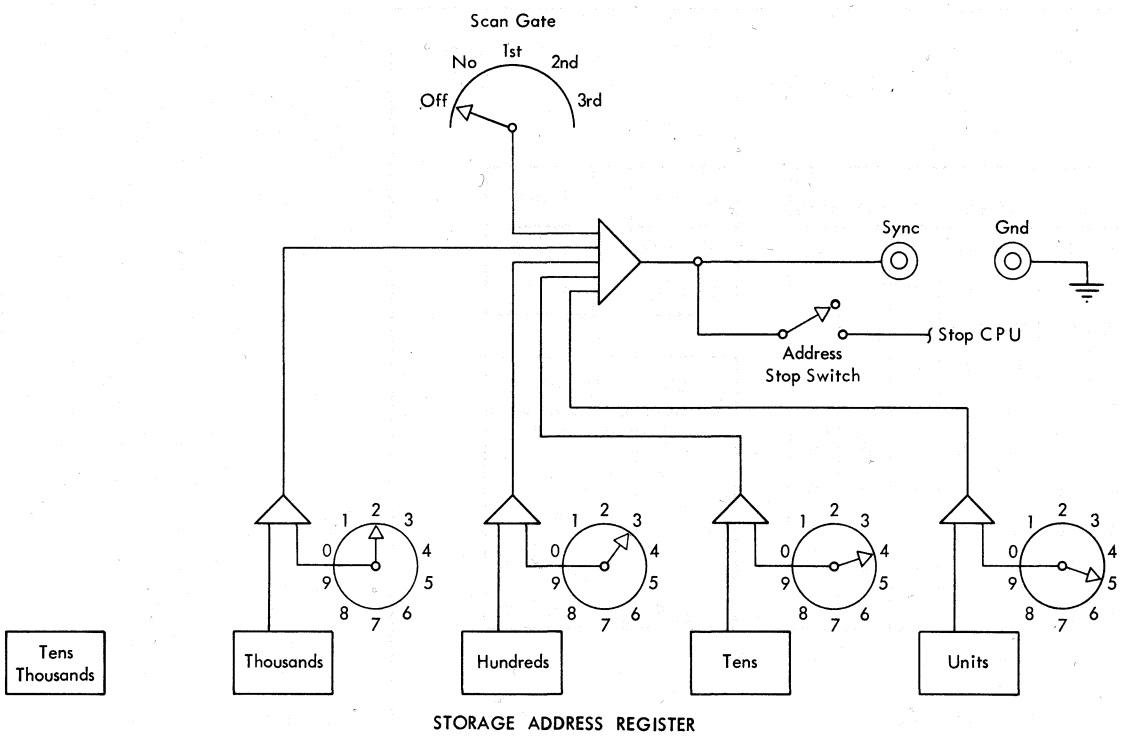


Figure 116. Address Stop or Scope Sync

TAU Voltages

VOLTAGE	TOLERANCE	LOCATION	REMARKS
− 6	±4%	LB-D8	Right side, card side of TAU.
−12	±4%	LB-D1	Left side, card side of TAU.
+12 M	±4%	LB-D5	Wiring side of TAU.
+12	±4%	LB-D7	Same power supply for both +12 M and +12.

IBM 1405 Voltages

VOLTAGE	TOLERANCE	LOCATION	REMARKS
+30	±4%	N Laminar Bus on file electronic gate.	See Figure 119 for PS locations.
+ 6 M	±4%	Q	
−12 M	±4%	R	
− 6	±4%	K	
−36	±4%	P	
−48	±4%	B 13 N	−48 supply is located behind relay gate.

Check Test

Before any tests are run during scheduled maintenance, be sure that the error-detection circuits are functioning properly. Do this by completing the check test.

Procedure

With the system in the run mode, press the computer reset. Then, while pressing check-test-1 switch, press the start key. All check lights should come on, and an error type-out should occur. Press program reset. Then, while pressing check-test-2 switch, press the start key. Again, all check lights should come on, and an error type-out should occur. Repeat the procedure with check-test-3 switch. The same results should occur as for the previous tests.

Marginal Voltage Tests

The following tests should be done every two months. Every six months these same tests should be run with the marginal supplies increased instead of reduced.

SYSTEM TESTS

1. Reduce the 1411-C frame marginal supply (marginal-check jack J-3) to 3 volts below nominal. Check that display and alter modes operate correctly.

2. Reduce the marginal supply to 3 volts below nominal and run the following programs:

FRAME	PROGRAM	TIME	APPLICABLE TO
1411 (J1, J3, and J4)	CS39-46	3 min.	All systems.
1411 C and D (J3 and J4)	M001B	3 min.	All systems.
1414 A (MCA)	M001B	3 min.	1414 III or IV.
1414 C (MCC)	M001B	3 min.	1414 IV.
1414 D	T004B	1 pass	1414 I or II.

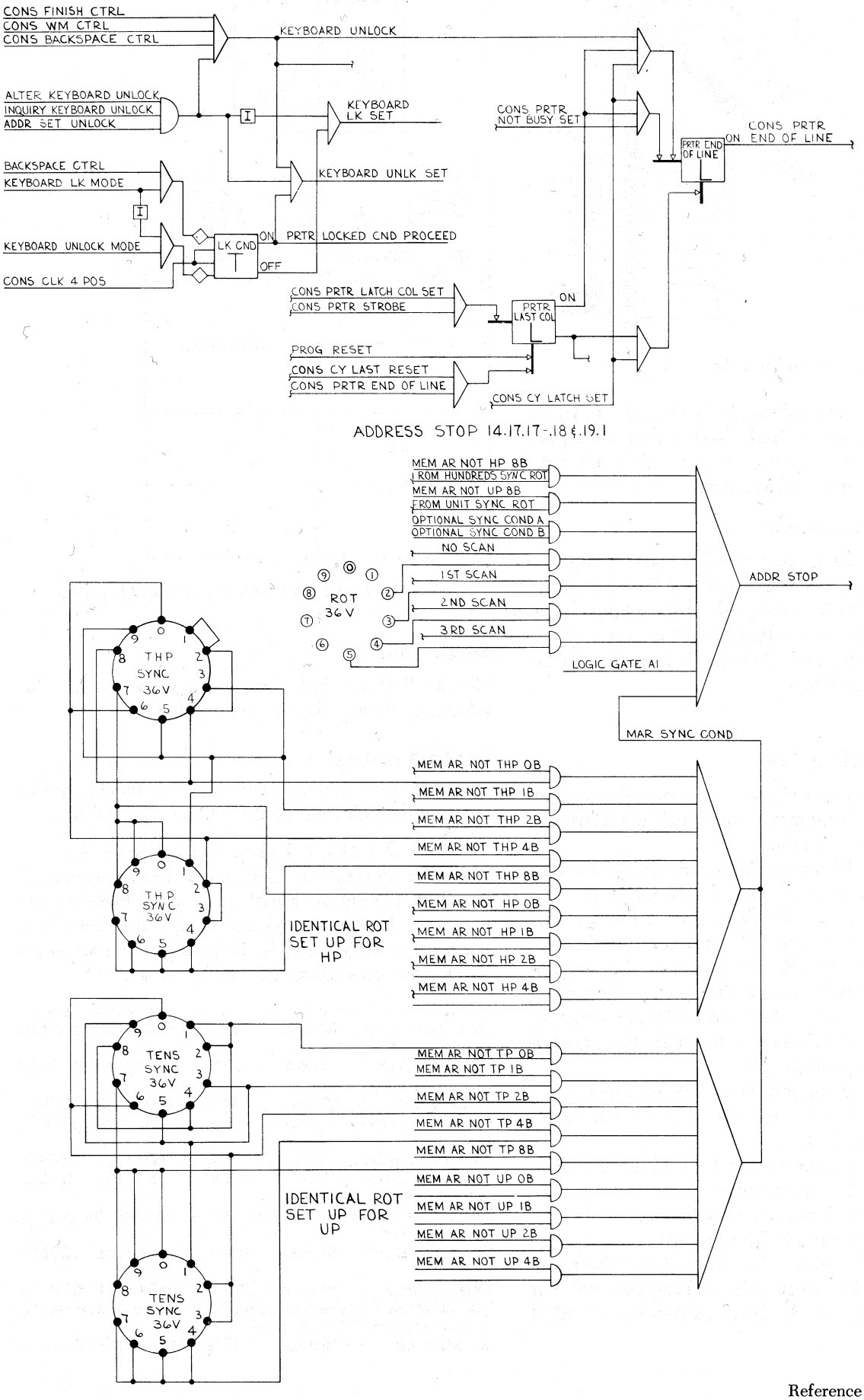


Figure 117. 1411 CE Panel Address Stop and Keyboard Control

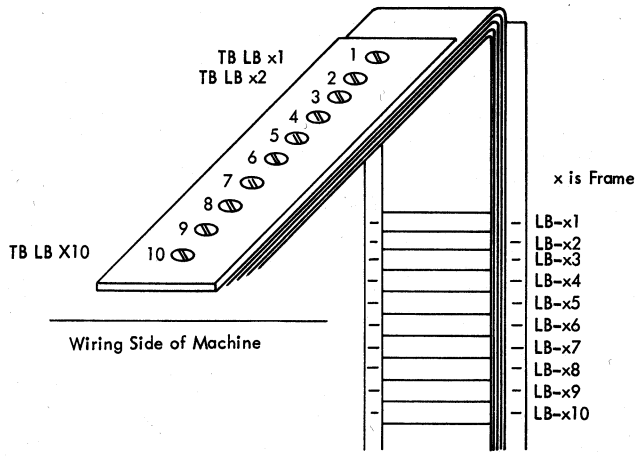


Figure 118. Laminar Bus Pin Locations

3. Reduce the marginal supply (+6M and −12M) 1.2 volts below nominal on each 1405 and run program D004B for 5 minutes for each voltage. Only one voltage per 1405 can be varied at a time.

IBM 1411 CORE STORAGE TEST

1. Reduce the +12 marginal supply to +9 volts and run diagnostic program CS39-46 (Memory Worst Pattern). While the program is running adjust the +60 and +30 volt supplies ±6%, one voltage at a time, for approximately two minutes each. The 6% is figured from the optimum working voltage.

Marginal Frequency Test

Once every six months check system operations at increased oscillator frequency for marginal characteristics.

Test procedure is as follows:

1. Substitute a 1.5 mc oscillator card for the standard oscillator card in chassis 1411 C 2, location H 07.
2. Adjust the clock pulse delay-line so that the first and second clock pulses are 333 ±40 nanoseconds wide. The interval from the 10% point of the rising edge of the second clock pulse to the 10% point of the rising edge of the first clock pulse is 333 ±80 nanoseconds. The clock pulses should be measured at the output of the clock-pulse trigger inverters.
3. Run diagnostic program CS39-46 for 3 minutes at marginal voltages of 1.5 volts above and below nominal, using J1, J3, and J4.
4. Replace the standard oscillator card and re-adjust the clock pulse delay-line so that:
   a. the second clock pulse is 375 ±50 nsec.
   b. the first clock pulse is 375 ±50 nsec.
   c. the interval between the 10% point of the rising edge of the 2nd clock pulse and the 10% point of the rising edge of the 1st clock pulse is 375 ±100 nsec.

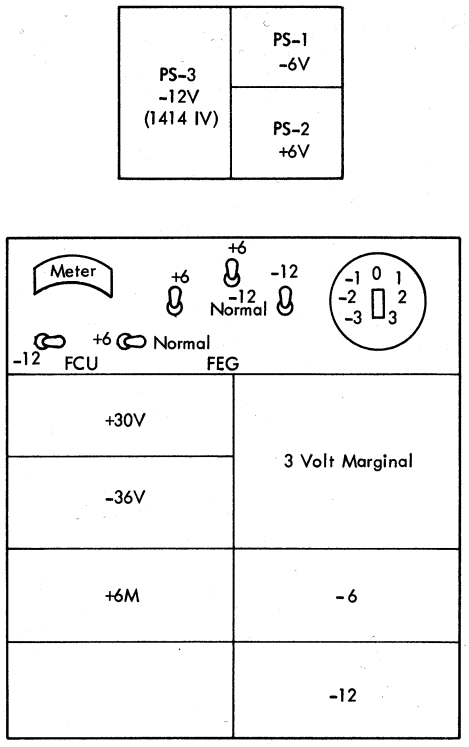


Figure 119. IBM 1405 and 1414A Power-Supply Locations

Single Shot

Check all single-shot timings every six months. Readjust any timings that are out of tolerance.

IBM 1411 Timings

Six of the nine single-shot timings can be checked by entering the following program in position 00001.

U % U 1 M 2 F J M % TO 201 W B 002 .

Starting in position 00201, enter a short record followed by a group-mark with word-mark. Place the system in the 1401 mode and have a tape drive set to unit one on channel one. Ready the 1403 printer and set the check-control switch to RESET and RESTART.

SINGLE SHOT	TIMING	TOLERANCE	TEST POINT	LOGIC
Unit Control Insn RO delay	25 μsec	±20%	11D3 H11P	13.71.04
First I/O Cycle Ctrl	6 μsec	±20%	11D3 J12P	13.70.03
Forms Stacker Go	20 μsec	±20%	11D3 C26P	13.70.04
Cons Check Strobe Interlock	20 msec	±20%	11C4 B06P	45.50.01
1401 Stop and Wait	3 μsec	±20%	11D1 K20P	12.60.20
Automatic Computer Reset	1 μsec	±20%	11D3 J16P	13.42.10
The following two single shots can be checked by pressing computer reset.				
Comp Rst Clock Start	25 μsec	±20%	11C4 B26P	12.65.01
Delayed Reset	20 msec	±20%	11C4 B17P	12.65.01
The last single shot can be checked by using the address display operation on the 1411 CE panel.				
Set Mem AR	25 msec	±20%	11B2 B27P	14.17.16

IBM 1402-2 Attachment Timings

These timings can be checked off-line by using the selected read buffer off-line mode.

SINGLE SHOT	TIMING	TOLERANCE	TEST POINT	LOGIC
Rd Request Dly	100 μsec	±20%	14A4 F11G	52.10.07
Pch Request Dly	1 msec	±20%	14A4 C04R	52.10.14
Brush Driver	250 μsec	±20%	14A4 F10G	52.10.07
1401 Mode	7.5 msec	±10%	14A4 F12G	52.10.08

IBM 1403 Attachment Timings

These timings can be checked off-line by using the printer-selected off-line mode.

SINGLE SHOT	TIMING	TOLERANCE	TEST POINT	LOGIC
PSS-Trigger	500 μsec	+10	14A3 G12C	53.30.02
Gate		−25 μsec		
PSS Set Line	325 μsec	±20 μsec	14A3 G13C	53.30.02
Blanking				
Emitter	1 msec	±50 μsec	14A3 G11C	53.52.02
Single Space	As specified on tag		14A3 D14C	53.55.01
(See Note 1.)	located on T-frame.			

NOTE 1: Set carriage switch to single space. Check single-space SS and set for optimum horizontal print alignment (4 to 6 msec). If this SS is readjusted, check the decelerate SS.

Double Space	9 msec	± .5 msec	14A3 D13C	53.55.01
(See Note 2.)				

NOTE 2: Set carriage switch to double space.

Triple Space	15 msec	± .5 msec	14A3 D12C	53.55.01
(See Note 3.)				

NOTE 3: Set carriage switch to double space. Wire D13L to D12L.

Decelerate	See note 4.		14A3 G10C	53.55.03

NOTE 4: Before timing the decelerate SS, make certain that the single-space SS has been set properly. Set carriage switch to single space. The decelerate SS is then set for the shortest time consistent with good horizontal print alignment (approximately 16 msec).

Tape Adapter Unit Timings

All of these timings can be checked using any write operation off-line.

SINGLE SHOT	TIMING	TOLERANCE	TEST POINT	LOGIC
Start	2 msec	±15%	14D1 D14P	60.58.10
CE Pulse	10 μsec	±15%	14D1 D15P	60.58.10
Delay	50 μsec	±15%	14D1 D16P	60.58.10
Erase	10 μsec	±15%	14D1 D21P	60.58.10
RC 7 reset	.4 μsec	±10%	14DB F03P	B9.10.31
Delay Counter Reset	1.5 μsec	±10%	14DB F04P	B9.30.31
WDD 60	1.5 μsec	±10%	14DB F05P	B9.30.50
WDD 20	1.5 μsec	±10%	14DB F06P	B9.30.51

IBM 1011 Attachment Timings

These timings can be checked off-line by using paper-tape-reader (option 4) selected off-line mode.

SINGLE SHOT	TIMING	TOLERANCE	TEST POINT	LOGIC
End of Scan	2 μsec	±10%	14C5 F12P	55.10.05
Pt Scan Req	10 μsec	±10%	14C5 F11P	55.10.07
Ready (See note.)	5 μsec	±10%	14C5 F13P	55.10.06

NOTE: Wire F17B to F13B. Press reset and start to impulse Ready single-shot.

Delay Lines

Check all delay-line timings once every six months. Replace the delay line for any timing out of tolerance. The clock pulse delay-line is adjusted as explained under *Marginal Frequency Test*, step 4.

The timings and tolerances below refer only to the delay line itself (pins L to E). The transistor circuits following the delay line (pins Q to A) introduce additional delay.

INPUT	OUTPUT	TIMING	TOLERANCE	LOGIC
11B4 H14L	H14E	425 nsec	±5%	39.10.01
11B4 H11L	H11E	280 nsec	±5%	39.10.01
11B4 J09L	J09E	1100 nsec	±5%	39.10.01
11B4 K10L	K10E	280 nsec	±5%	39.10.02
11B4 K03L	K03E	150 nsec	±5%	39.10.02
11B4 G07L	G07E	1200 nsec	±5%	39.10.02
11B4 J12L	J12E	280 nsec	±5%	39.10.03
11B4 J15L	J15E	See note.	±5%	39.10.03
11B4 K13L	K13E	425 nsec	±5%	39.10.03

NOTE: The timing of this delay line depends on which pin is wired to pin Q. L to Q is 0 nsec, B to Q is 50 nsec, C to Q is 100 nsec, D to Q is 150 nsec, and E to Q is 200 nsec.

Service Aids

General

STOPPING ON ERRORS

If it is desirable to stop the CPU clock on a specific condition, remove the output of the STOP latch from the clock circuit. The clock may then be wired to stop on the desired condition. *Never allow the clock to stop with the second clock pulse on, because core storage resistors may be damaged.*

CAUTION: Be sure to restore the circuit to normal to prevent undetected errors.

FORCING SIGNALS

It is permissible to force a solid +S signal by wiring the required pin to ground. However, if a −S level is desired, the specified pin must not be tied directly to a −12 voltage. Instead, a 4,700-ohm resistor must be placed in the jumper circuit to provide the required load to the circuit.

VOLTAGE JUMPERS

Exercise care when working around the wiring side of any chassis to prevent dislodging any voltage jumpers. These can be easily dislodged because they have clip-on terminals.

SHORTED DE LOGIC BLOCKS

When a shorted DE block is encountered, always check the preceding card. If the short was caused by a down level, the preceding circuit may be damaged.

LOGIC LEVELS

Never ignore slight variations in levels. A poor level may cause intermittent failures. Marginal checking will help locate this type of failure. Any +S level lower than −.75 volts, and any −S level higher than −6.85 volts may cause failures and should be corrected.

PULSE WIDTHS

Very short voltage spikes *(glitches)* cannot be displayed reliably on the Tektronix 310 oscilloscope. The Tektronix 310 is not capable of handling pulses shorter than approximately 90 nanoseconds.

OSCILLOSCOPE SYNCHRONIZING

Both the 1411 and 1414 I-O synchronizer CE oscilloscope sync hubs may be further conditioned by any desired signal to develop the necessary sync for a specific problem. In the 1411, address stop may be conditioned by some other signal to stop the CPU early. Refer to the logic diagrams for the pin locations.

Operations

ALTER

If you make a mistake during an alter operation, first press the stop key, then press the start key. This allows the alter operation to be started at the beginning again without doing a display operation.

LOGIC STEP

When operating the system in logic step, remember that the character appears in the B data register at the end of LGA.

DISPLAY (FOR ALTER)

When displaying to set the ALTER FULL LINE CONDITION latch, move the right-hand margin stop closer to the left-hand margin stop to save time.

I-O SYNCHRONIZER CE MODES

Before returning the system to a customer, be sure to clear any storage unit that has been addressed from the CE panel. This is necessary because it is possible to leave a unit (card reader, PT reader) in the ready status with erroneous information in the associated storage unit.

OFF-LINE TROUBLE SHOOTING

If an I-O unit associated with the integrated synchronizer develops trouble when operating on-line, be sure to test the unit off-line. It is easier to locate troubles if the I-O unit is operated separately from the system. The integrated-buffer REGEN and LOAD functions are especially useful because the storage unit can be operated one storage cycle at a time.

IBM 1402-2 CE PANEL

Be sure to turn all 1402-2 CE controls off before attempting to address the reader or punch, either on- or off-line. If any of these switches are left ON, erroneous feeding or reading may result.

I-O Printer

INCORRECT SELECTION OF CHARACTERS

Incorrect selection of characters may be caused by:

1. Output-solenoid armature not seated properly at pivot point.
2. *Shift Complete* line conditioned early by C-3 or C-4 contacts out of time (intermittent).
3. Print head out of home position.

INCORRECT TRANSFERS

Transferring invalid characters to storage may be caused by:

1. Transmitting contacts either dirty or out of adjustment.
2. C-1 out of time. (Transmitting contacts must make 5° before C-1.)

CARRIAGE RETURN

A failure to initiate a carriage return may be caused by:

1. The right-hand margin stop finger riding over the top of the slide on the carrier.
2. The end-of-line contact not making properly. Adjust the contact to .030″ when the right-hand margin-stop finger is riding on the bottom of the rise on the slide. Enter one character and the contact should make. Enter one more character and the carriage should return.

MISSING PRINT-OUT IDENTIFICATION CHARACTER

Failure to print the print-out identification character may be caused by the carriage return interlock contact not unlatching. This may occur more often after a short carriage-return where the speed of the carrier is not as great as during a long carriage-return operation.

OPERATIONAL FUNCTION FAILURE

Failure to perform an operational function (space, backspace, carriage return) on output may be caused by the linkage between the operational solenoid and the operational interposer binding or being too long.

Card Read-Punch Operations

BRUSH TIMING

Always remove the punch- and read-brush connectors in the 1402-2 before checking brush timing with the 1402-2 CE panel. This prevents damage to the brush current-limiting resistors.

READ-IN FAILURES

To help isolate read-in failures, first check the row-bit fuse cards. If the fuses are not blown, try reading in with the buffer-inhibit drivers pulled.

CLOCK OR RING FAILURES

To locate an I-O synchronizer clock error, make the ring reset inoperative by wiring −S CLOCK ERROR (Systems 51.30.03) to ground and allowing the ring to run continuously. Synchronize the oscilloscope with the 000-010 trigger output and observe the other trigger outputs. The outputs should occur at one-microsecond intervals.

To locate ring errors, make the ring reset inoperative and synchronize the oscilloscope with the off side of the end-of-scan trigger. Observe the ring-trigger outputs (units and tens rings).

SENSE AMPLIFIER SCOPING

It is not possible to use the oscilloscope on the sense-amplifier inputs because the oscilloscope is internally grounded while the sense-amplifier input is not referenced to ground.

PUNCH MAGNET DRIVERS

When a punch magnet driver is off, its output swings from 0 to −20 volts at each cycle point due to the action of the circuit breaker. When the driver is on, its output remains at 0 volt *only* during the cycle point when the driver is energized.

IBM 1403 Printer Operations

DELAY LATCH

If the cables are removed from the 1403, the print integrated-buffer off-line mode may be used, provided the DELAY latch is OFF (Systems 53.23.03).

HAMMER DRIVER MATRIX

Never attempt to use the oscilloscope on the hammer-driver matrix, because it is very easy to damage the core storage unit when probing in this unit. All points on the matrix are accessible at other locations.

CARRIAGE TYPE

If there are less than eight spaces between holes in a given channel of a carriage tape, erratic carriage operation may result.

Magnetic Tape Operations

ON-LINE TROUBLE DIAGNOSIS

If it is necessary to service a tape failure on-line, set up sample instructions with fields as short as possible to simplify the operation. The IN PROCESS latch (Systems 13.60.04, 13.64.08) provides a good synchronization point for this type of failure.

TAPE DRIVE POWER

Power should be ON for all tape drives in a particular string. To remove power from a single tape-drive while continuing operation of the rest of the tape drives, remove the single drive completely and wire the cables around to complete the string. This is necessary to insure correct operation of the rest of the units.

Locations and Voltage Changes

Component Locations

There are three different frame configurations in the IBM 1410 Data Processing System. The large-chassis frames are shown in Figure 120. The tape adapter units use the small-chassis frames (Figure 121). The small-chassis frames are also used for some models of the IBM 1414 Input-Output Synchronizer (Figure 122).

A CE panel on any frame is referred to as *chassis 8* of that frame.

Input Voltage Change

To change input voltage, change the transformer taps at various transformers throughout the system. Be sure the power-cord plugs have been removed from their wall receptacles.

TRANSFORMER DESCRIPTION	LOCATION	TRANSFORMER TAP NUMBERS 208v OPERATION	230v OPERATION
Ferroresonant Supply	1411, 1414 TAU, 1402-2, 1414 I/O Sync on systems w/o 1402-2	1 and 4	1 and 5
48V Supply	1411	1 and 4	1 and 5
24V Control	1411	1 and 3	1 and 4
115V Convenience outlet supply	1411	4 and 5	3 and 5
60V Supply	1402-2	Connect wire from TB 2 to terminal 4 on terminal strip VR1.	Connect wire from TB 2 to terminal 5 on terminal strip VR1.

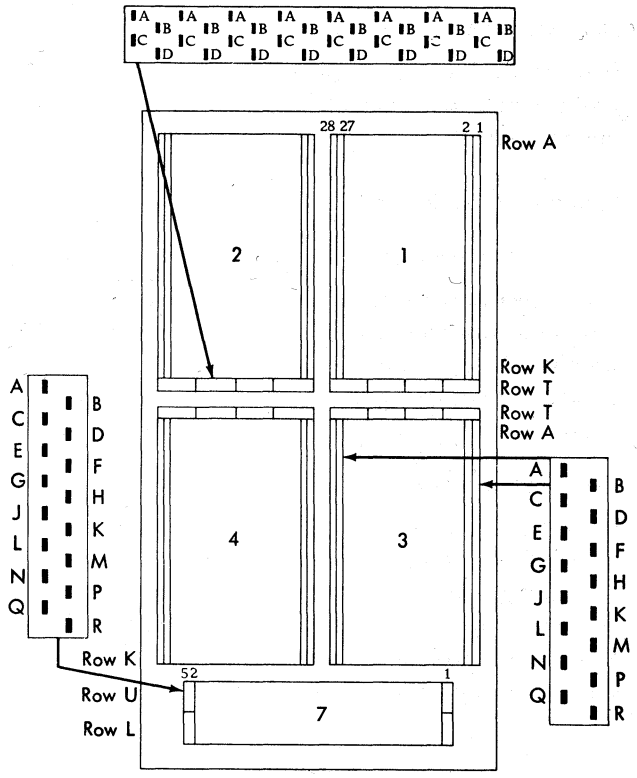


Figure 120. Frame Designation Large Chassis (Wiring Side)

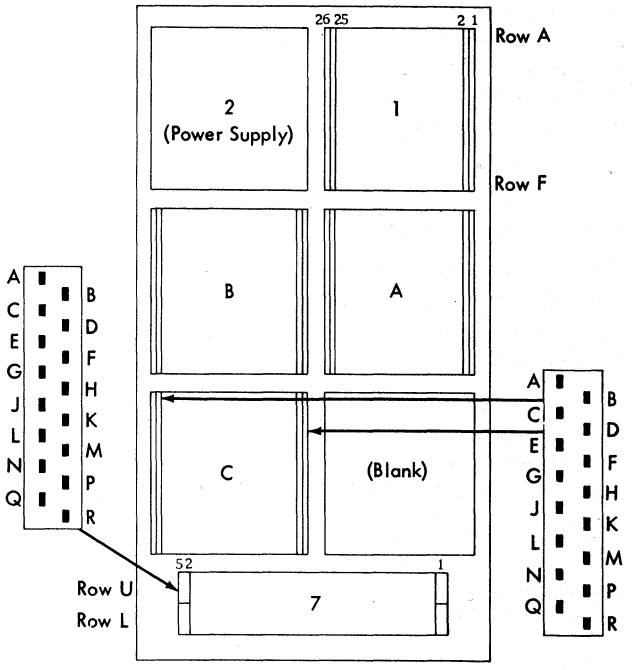


Figure 121. Frame Designation, Tape Adapter Unit (Wiring Side)

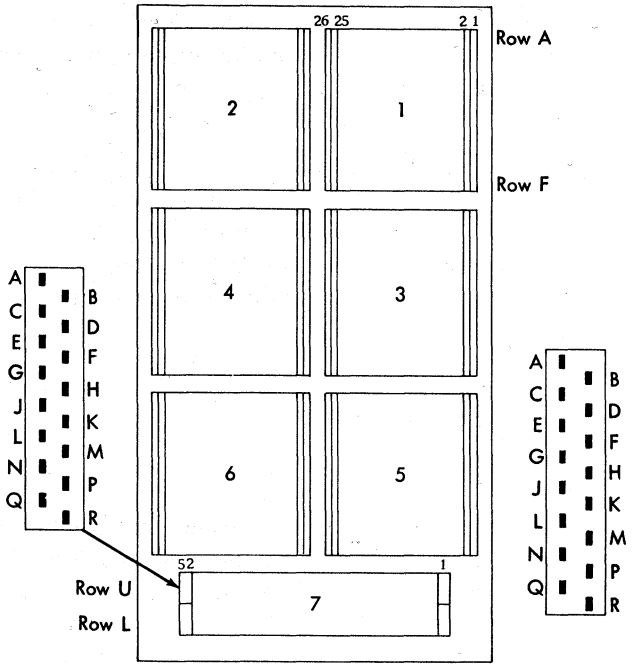


Figure 122. Frame Designation, I/O Synchronizer (Wiring Side)

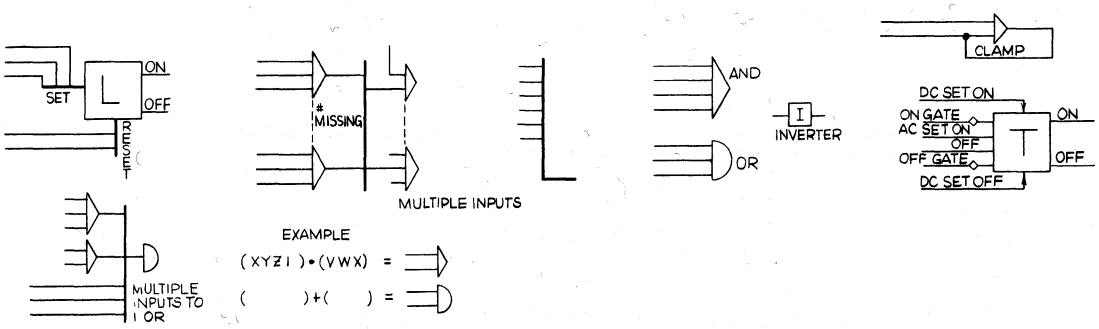


Figure 123. 1410 Second Level Diagram Configurations

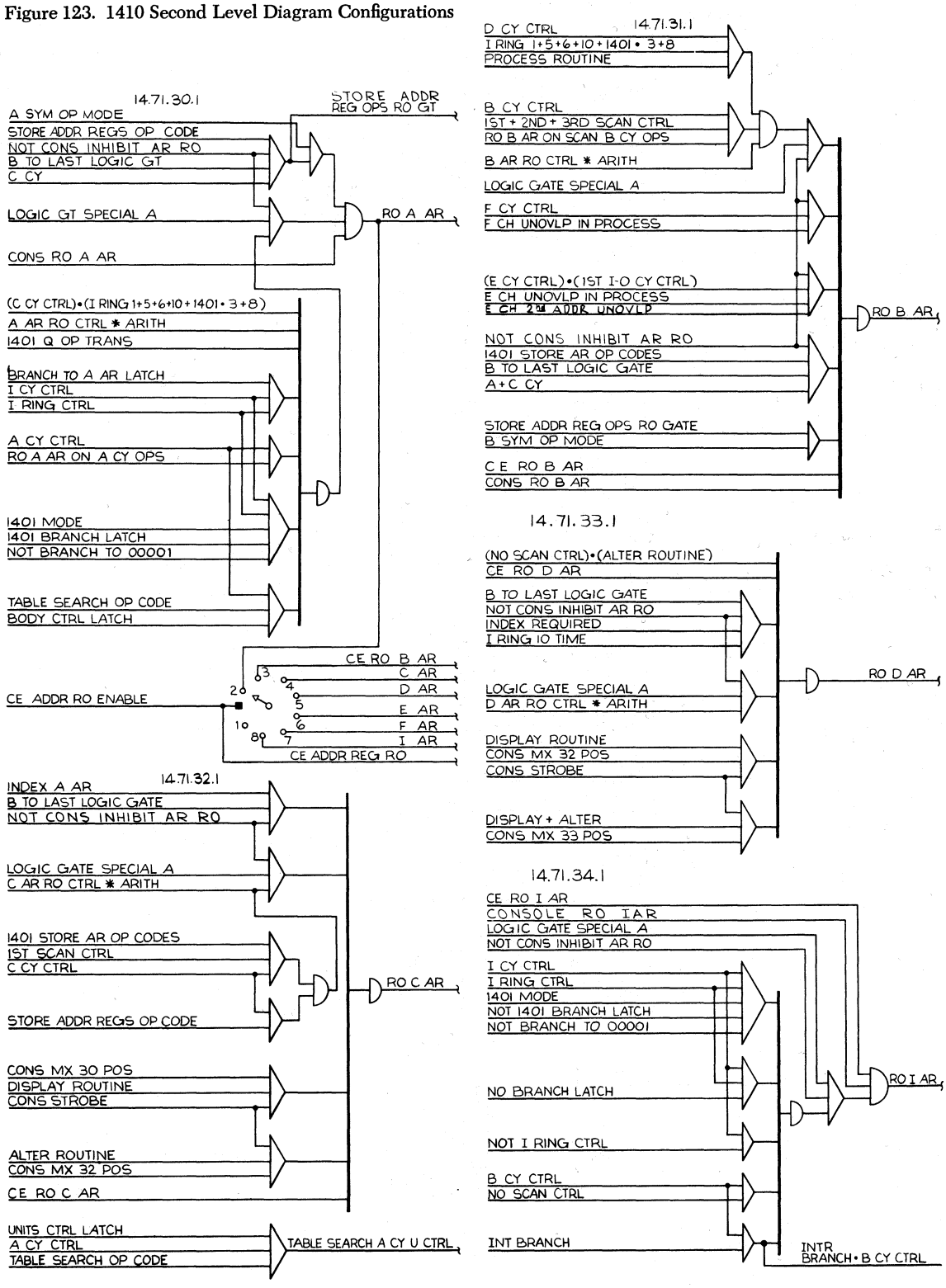


Figure 124. ADDR Registers Read-Out CTRLS

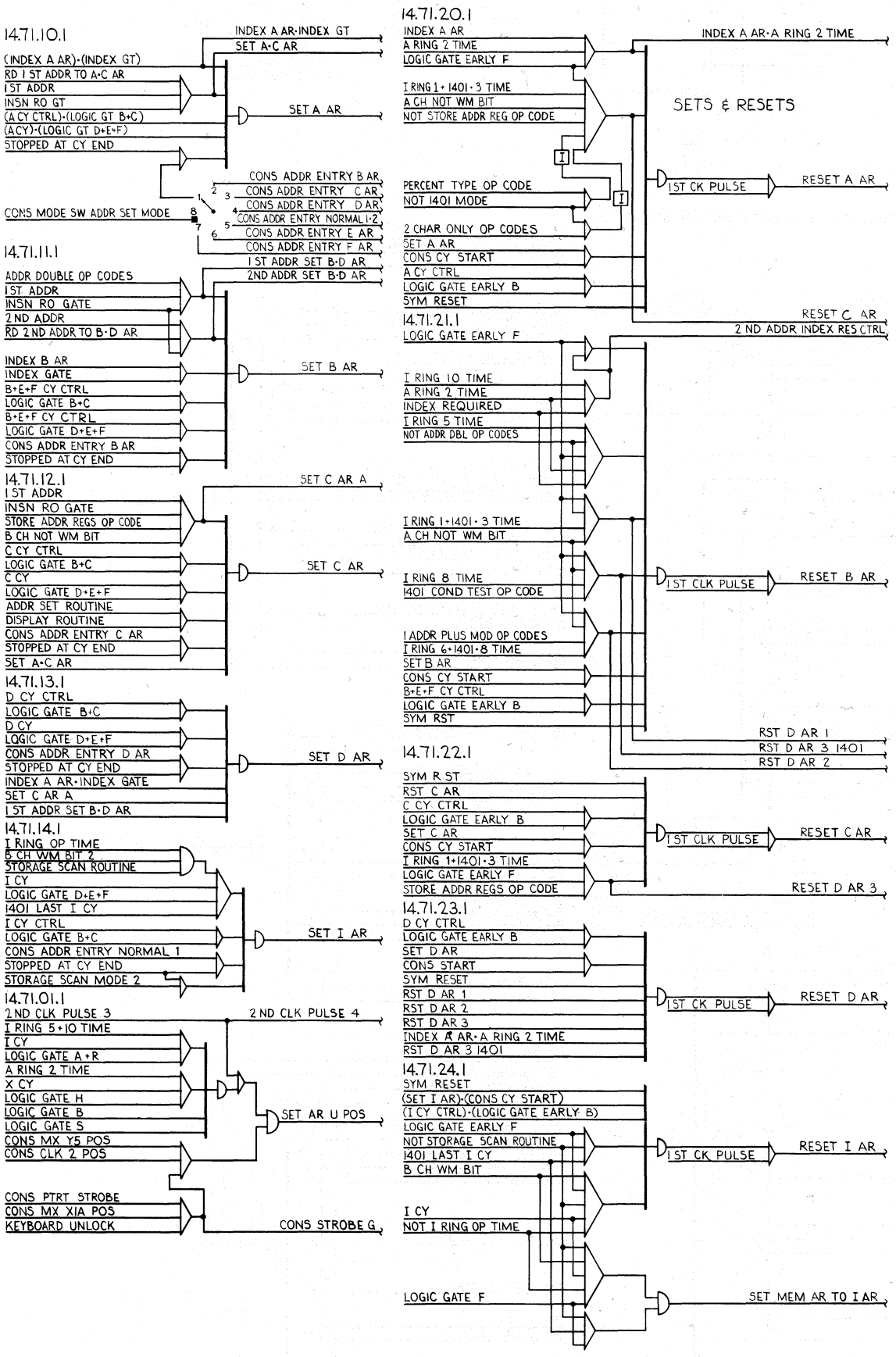


Figure 125. Address Register Sets and Resets

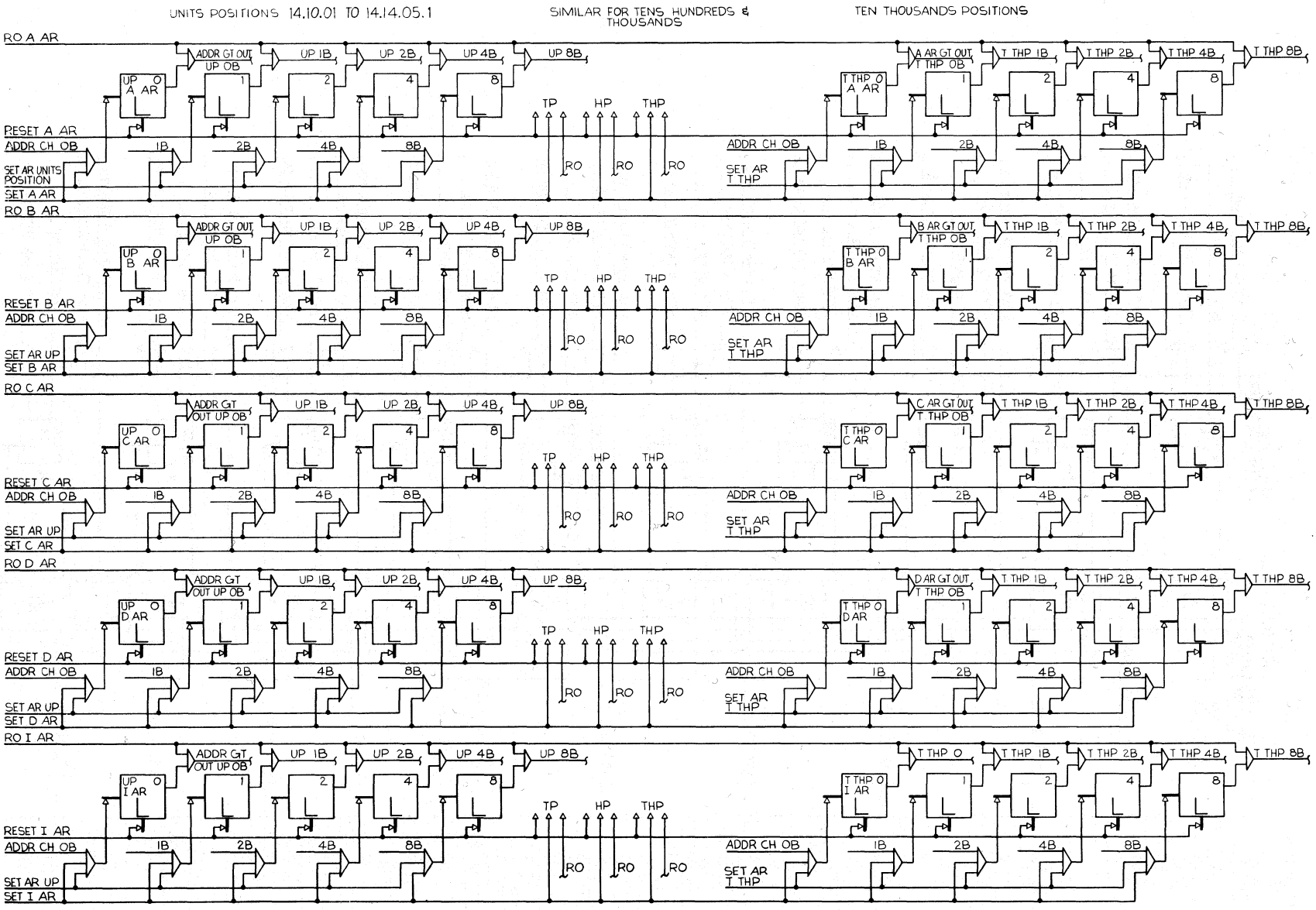


Figure 126. AAR, BAR, CAR, DAR, and IAR Latches

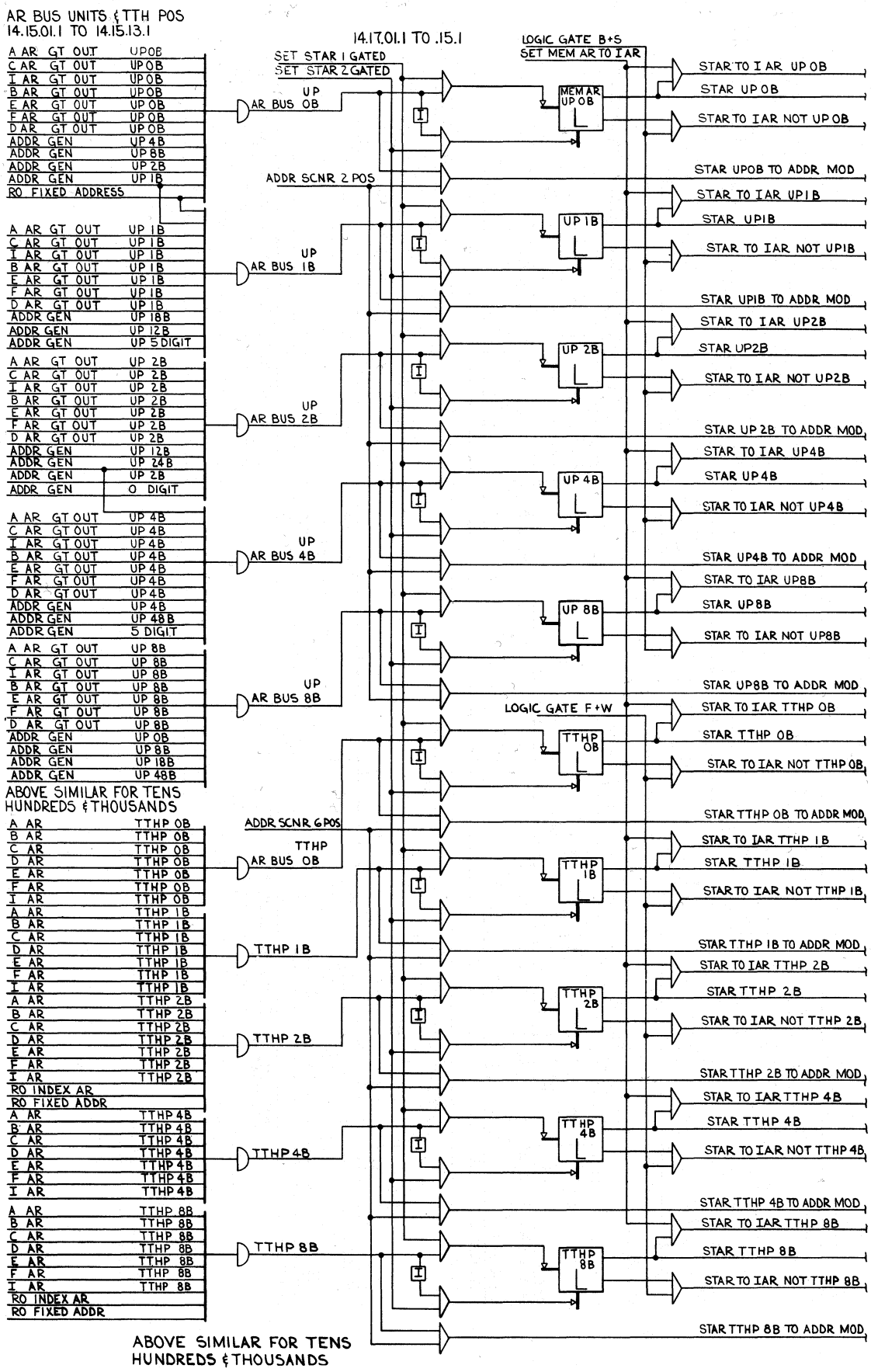


Figure 127. AR Bus and MEM AR to IAR Latches

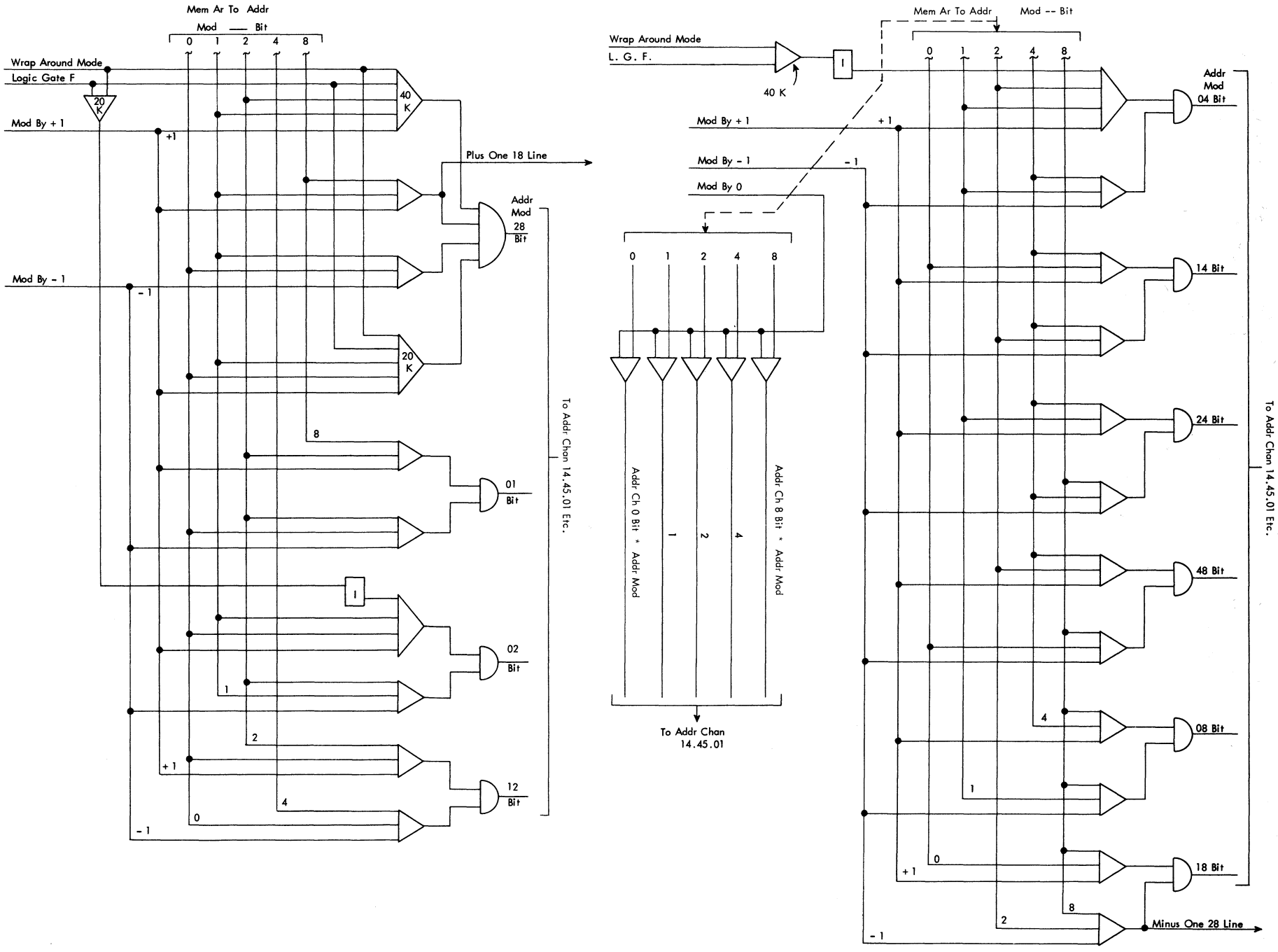


Figure 128. Address Modification

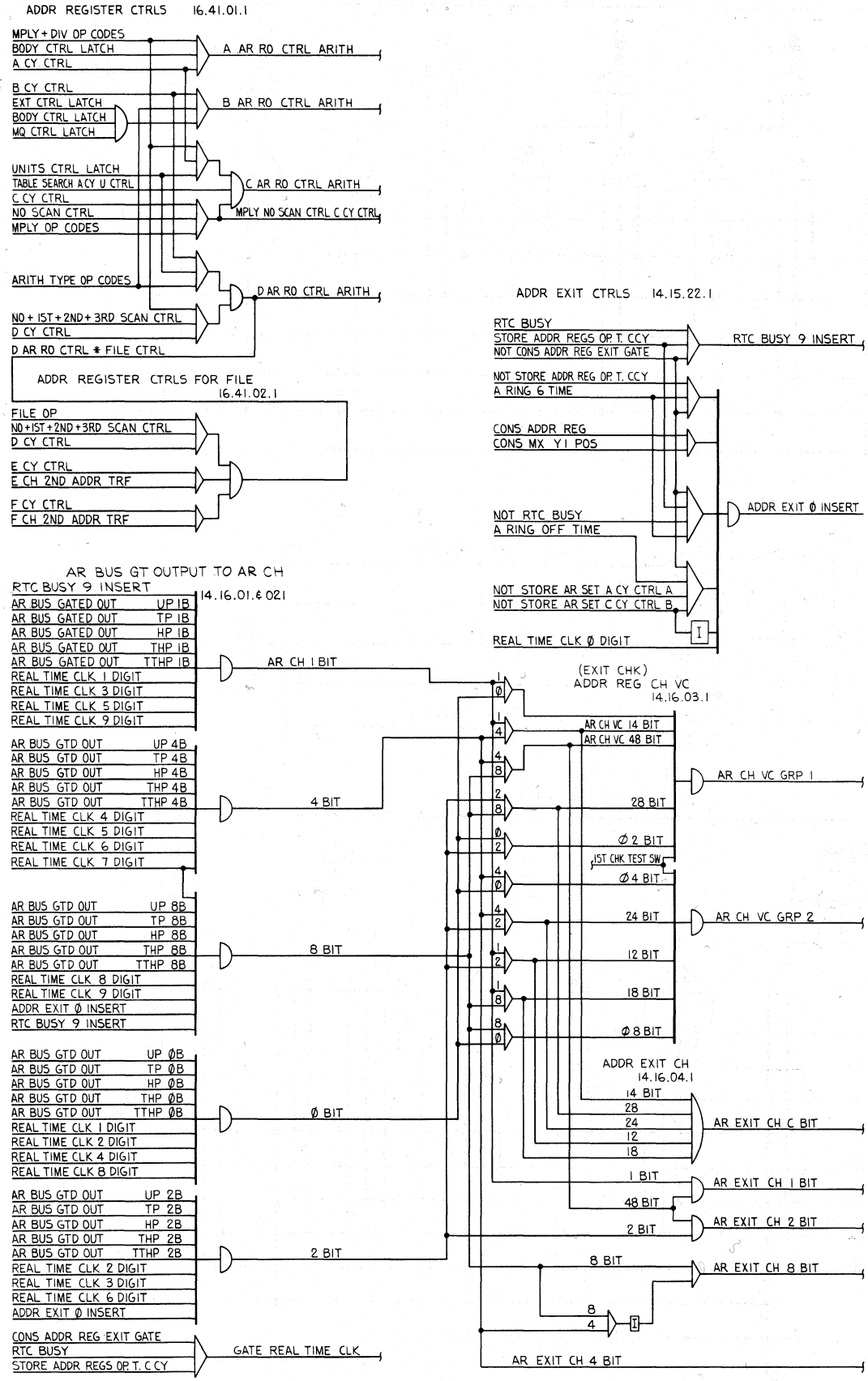


Figure 129. ADDR REG CTRLS, ADDR Bus Gated, ADDR EX CH and EX CHK

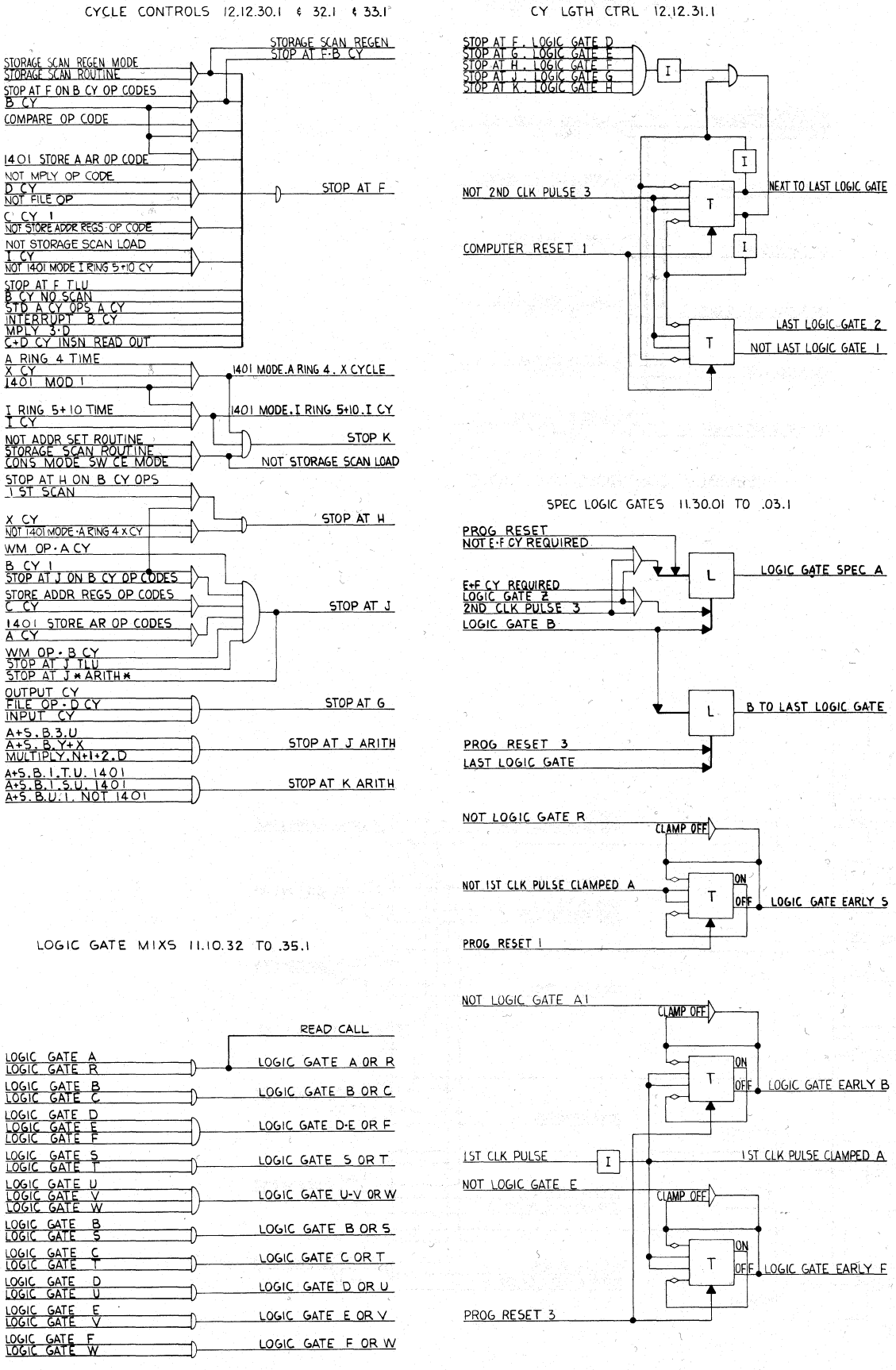
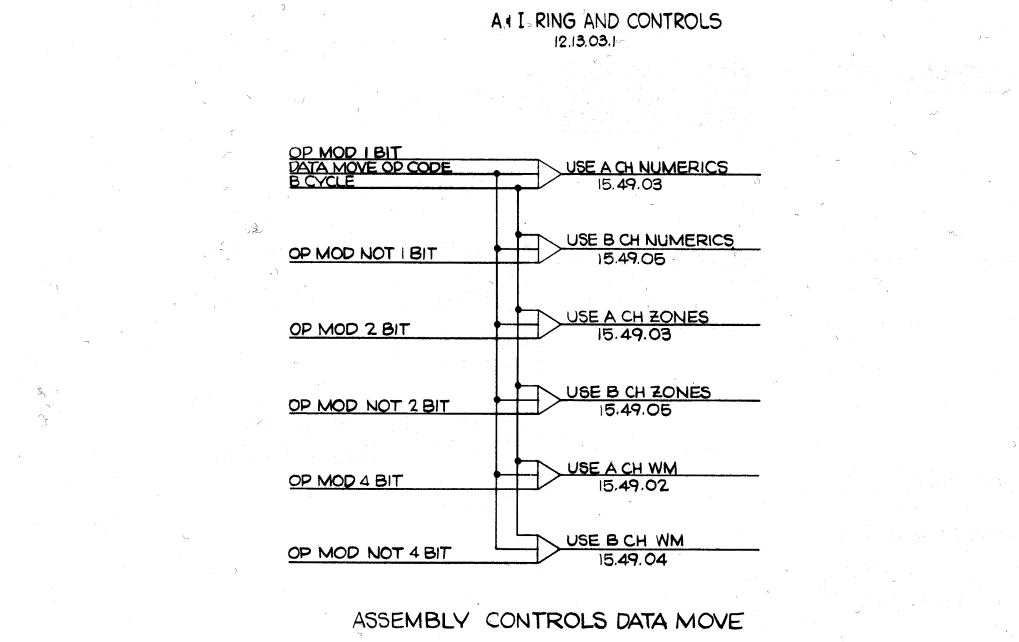


Figure 130. Cycle CTRLS, Cycle Length CTRLS, and Special Logic Gates



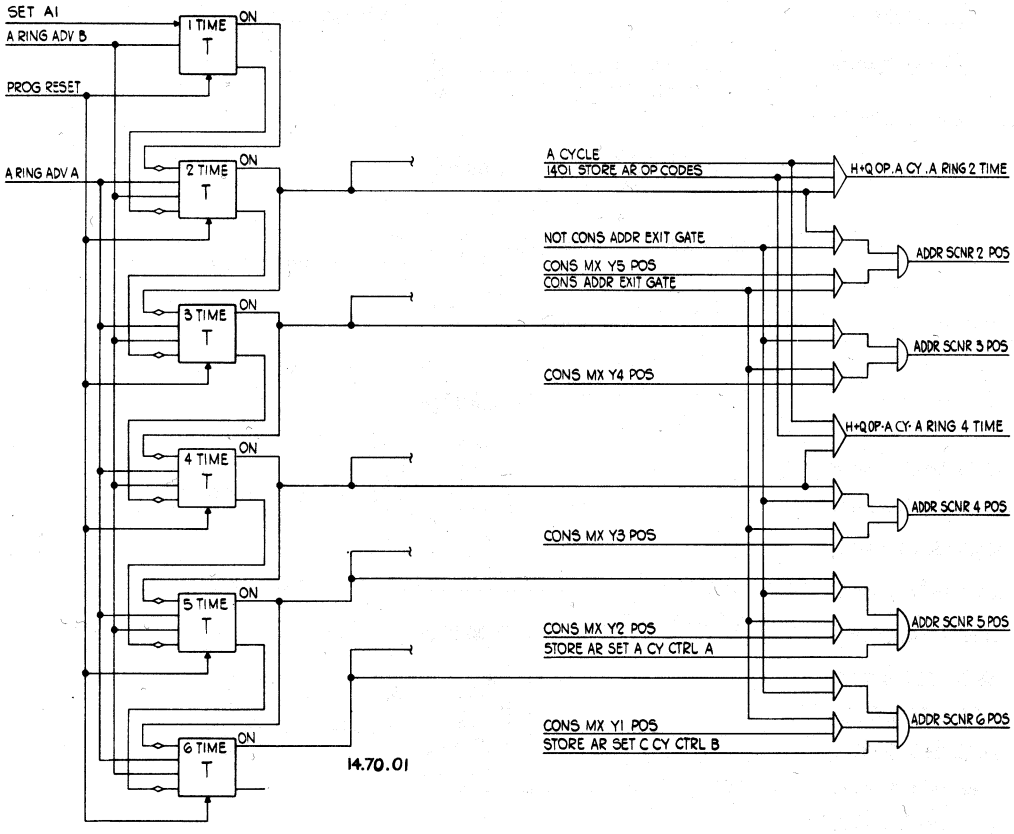


Figure 131. A and I Ring Controls

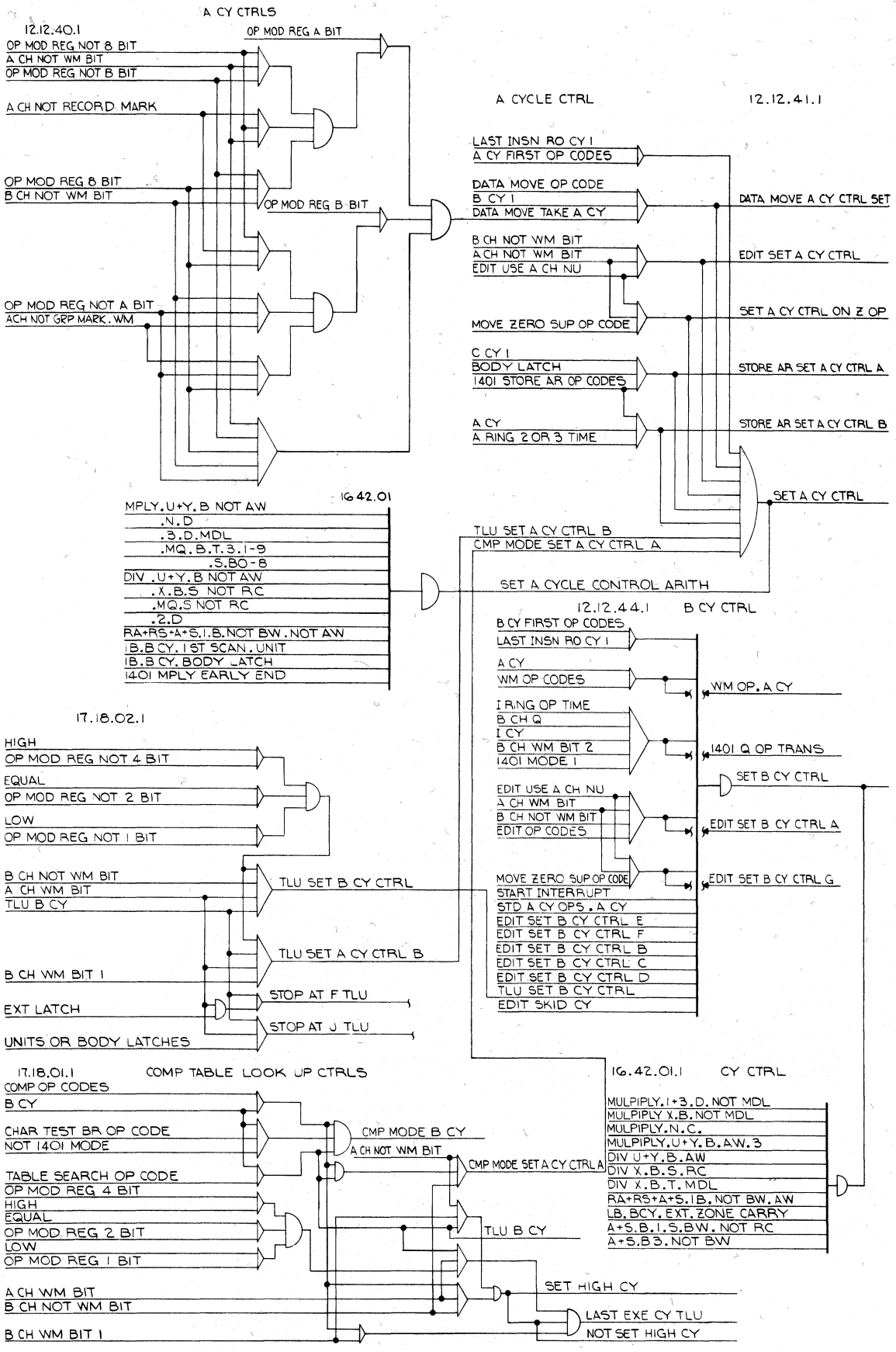


Figure 132. A and B Cycle Controls

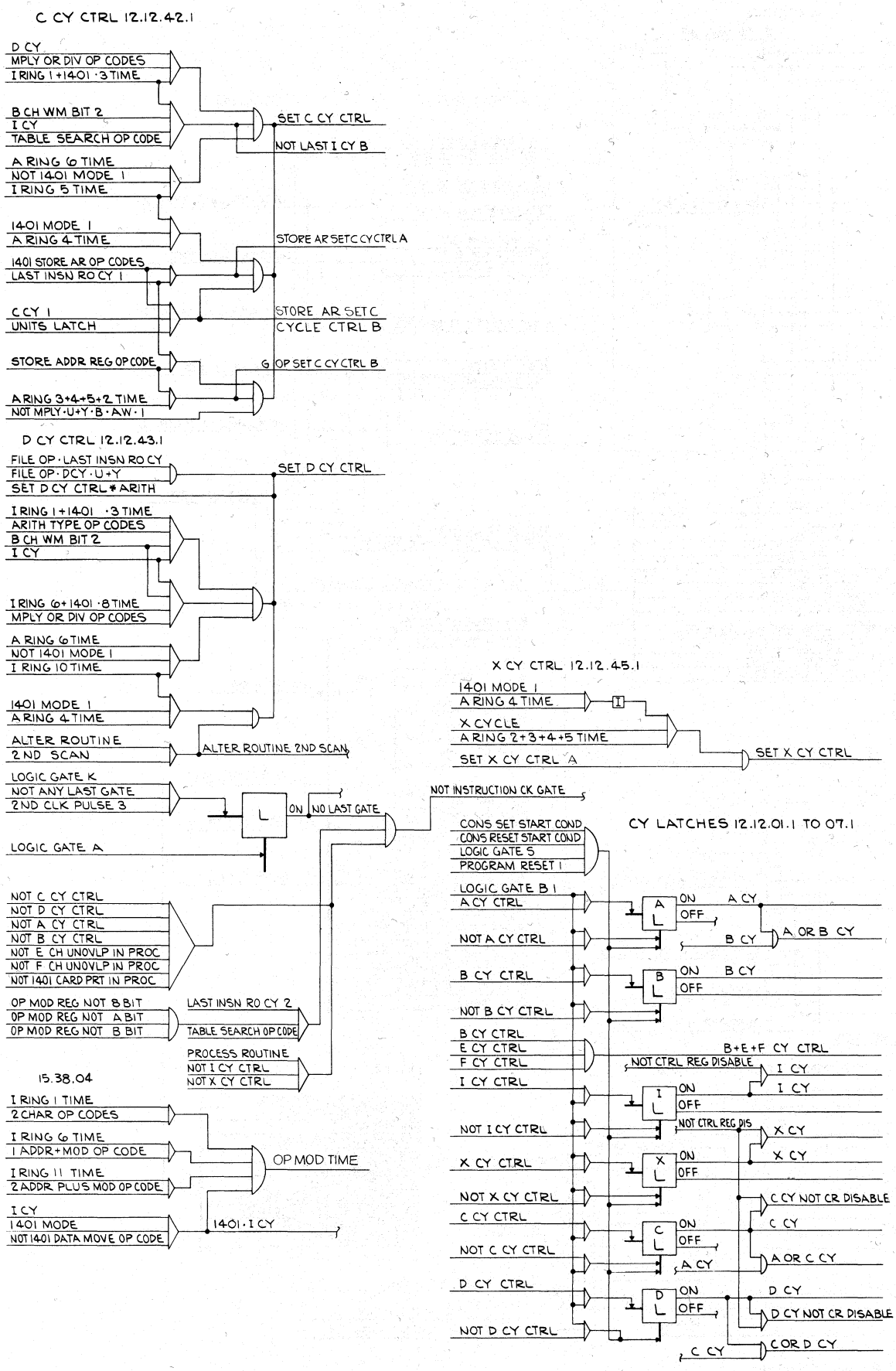


Figure 133. C, D, I, X Cycle Controls

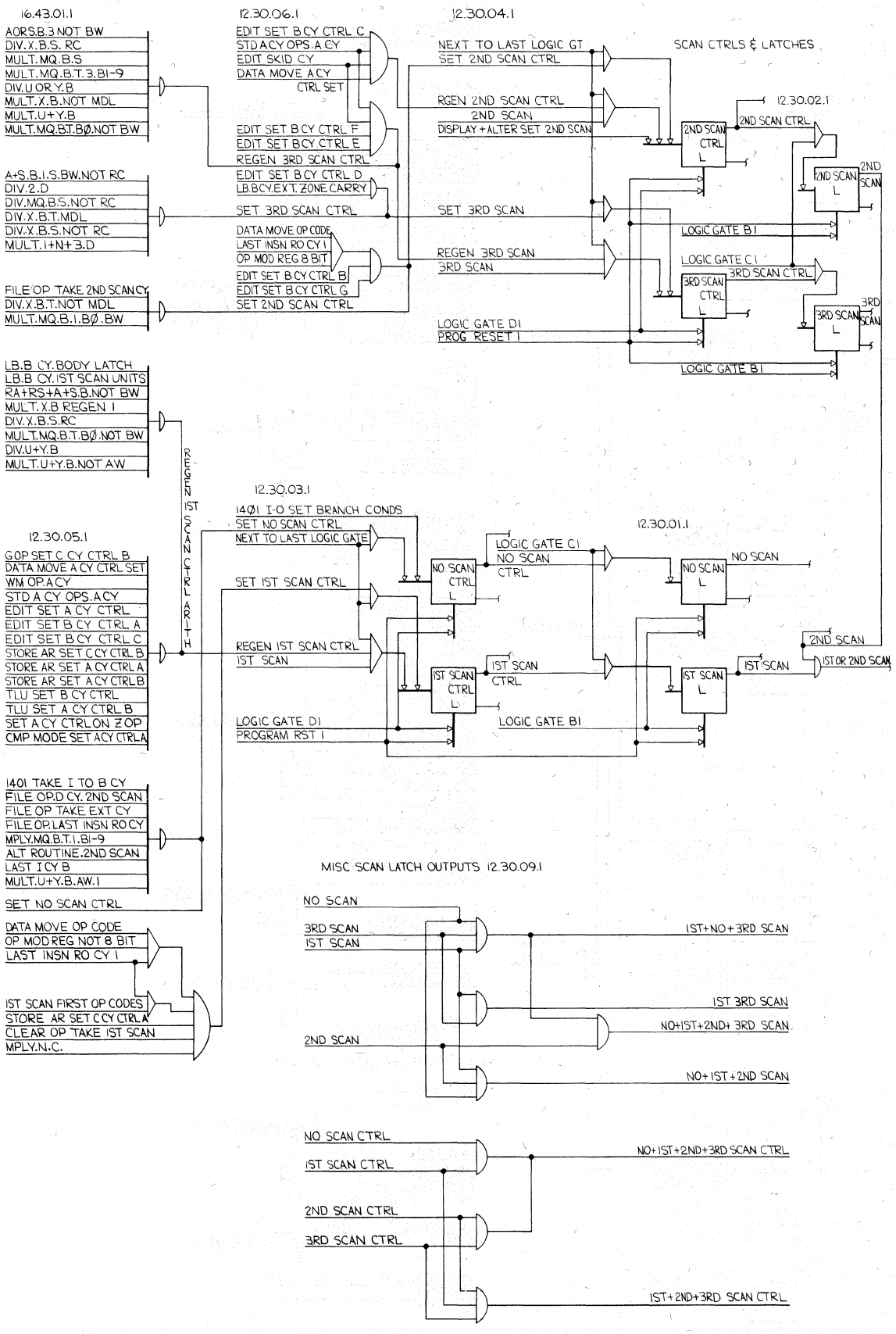


Figure 134. Scan Controls and Latches

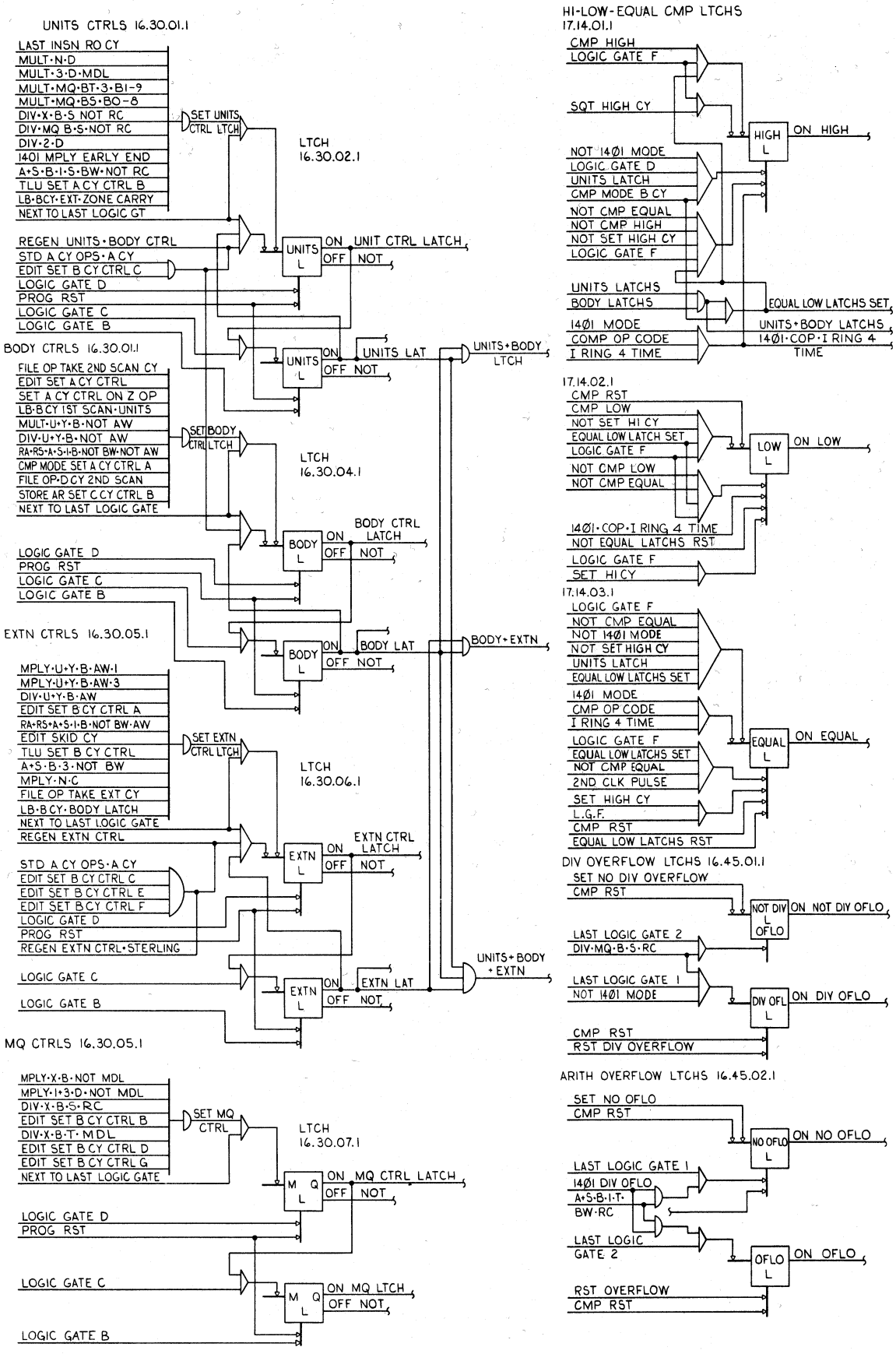


Figure 135. Units, Body, Extension, MQ Controls, and Divide and Arith Overflow Latches

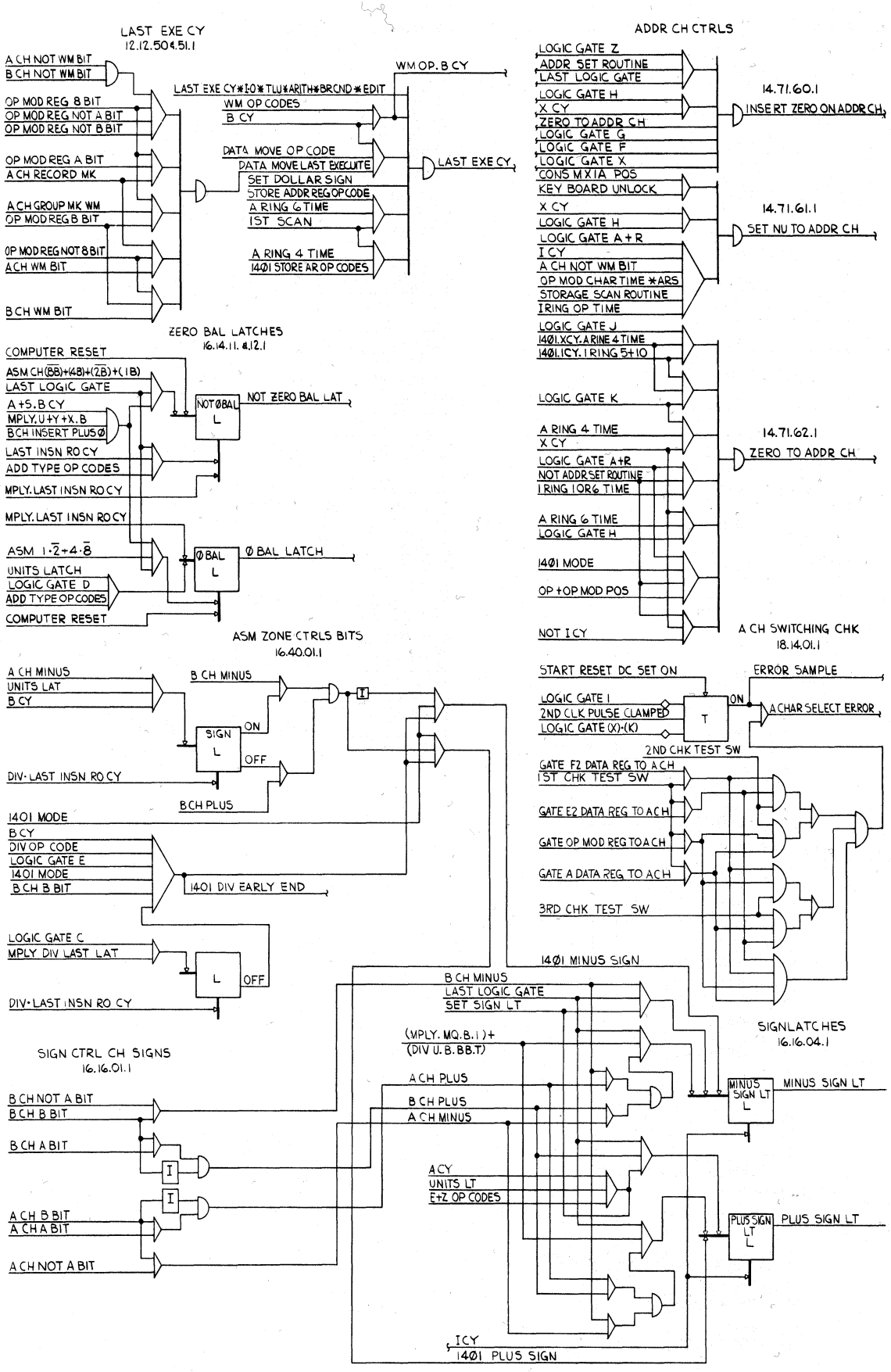


Figure 136. Address Channel Controls, Last Execute Cycle, Balance Zero and Sign Controls, and Latches

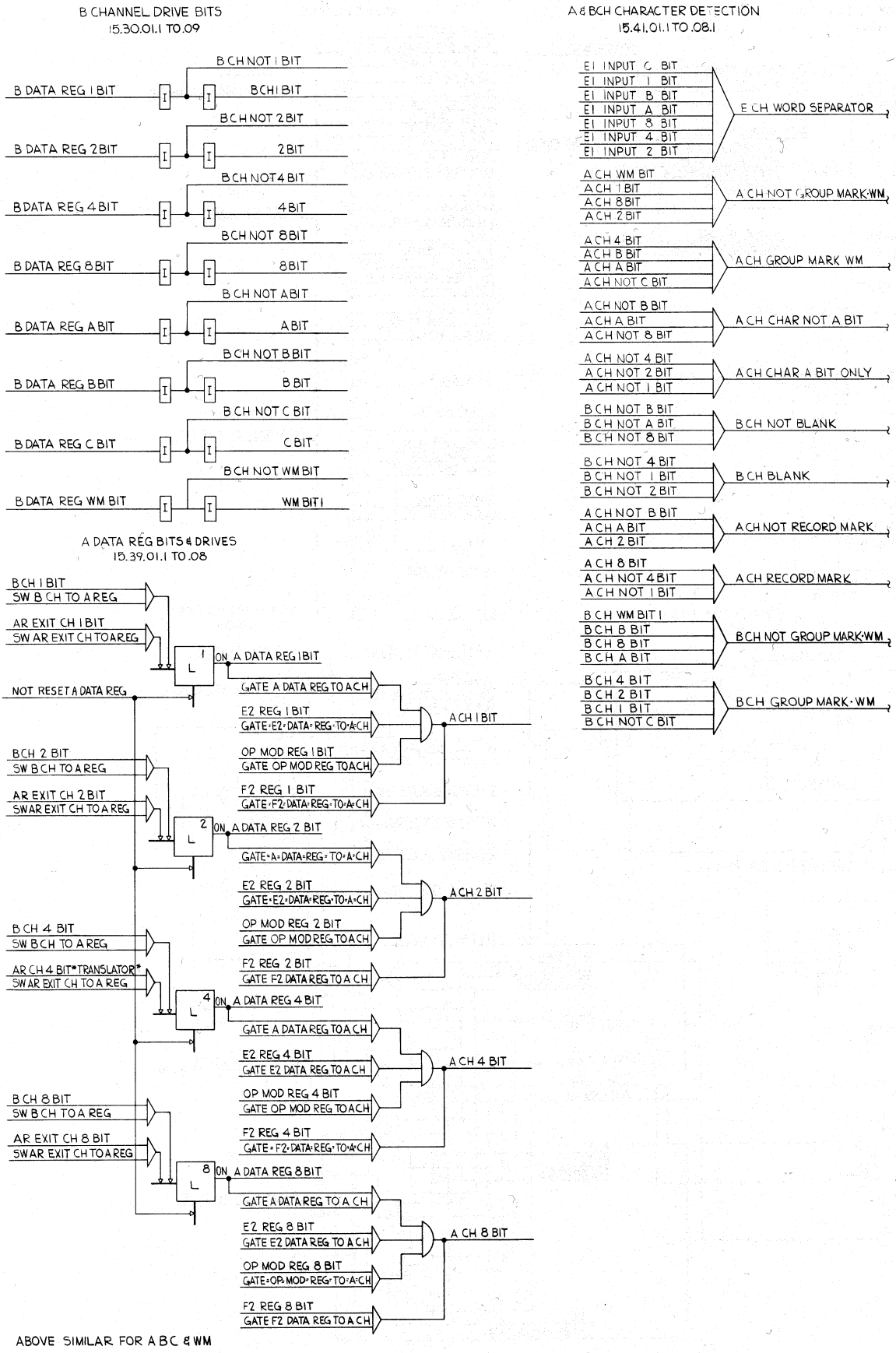


Figure 137. A and B Bits, Drives and Channel Characters

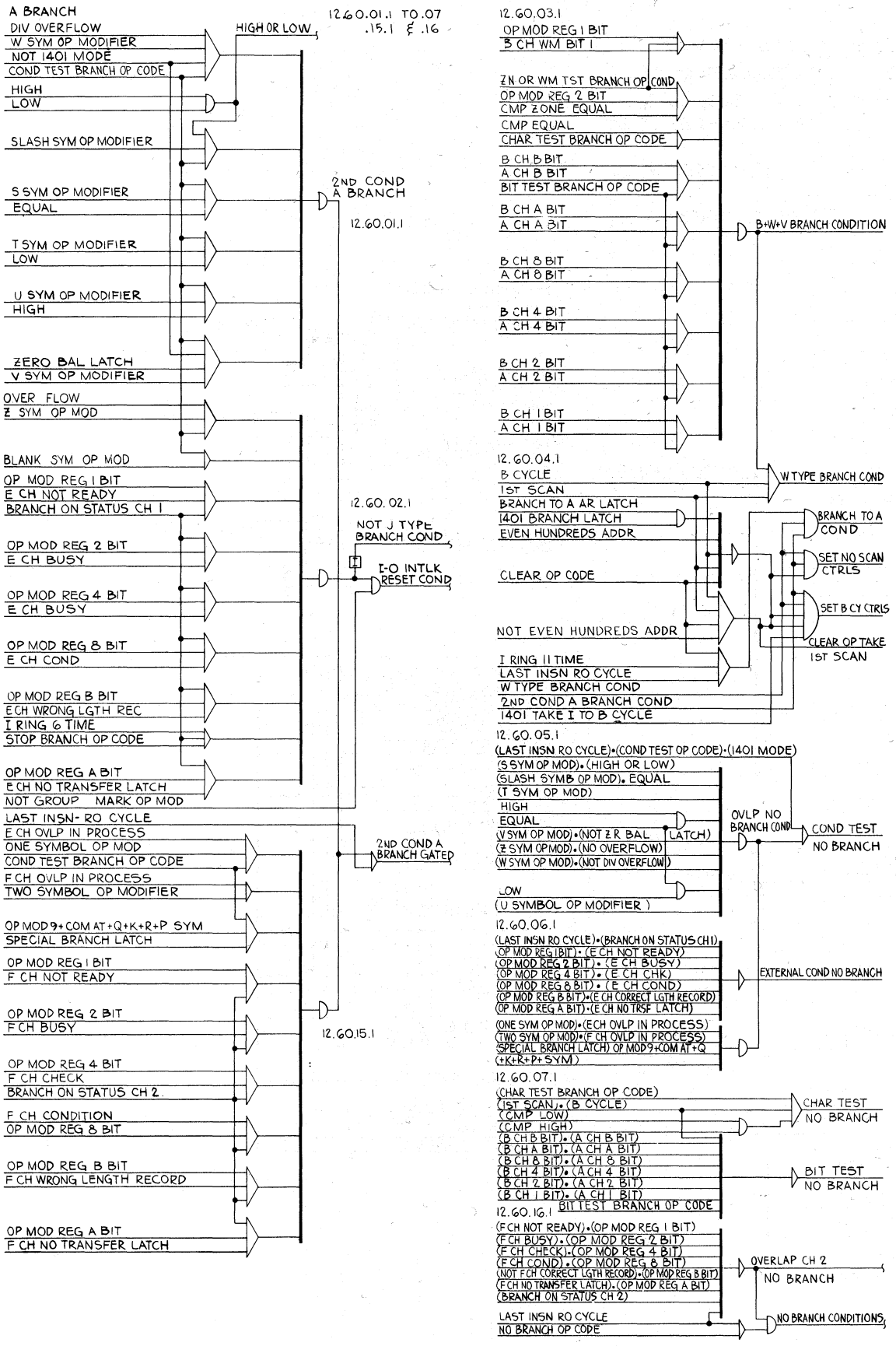


Figure 138. Branch Conditions

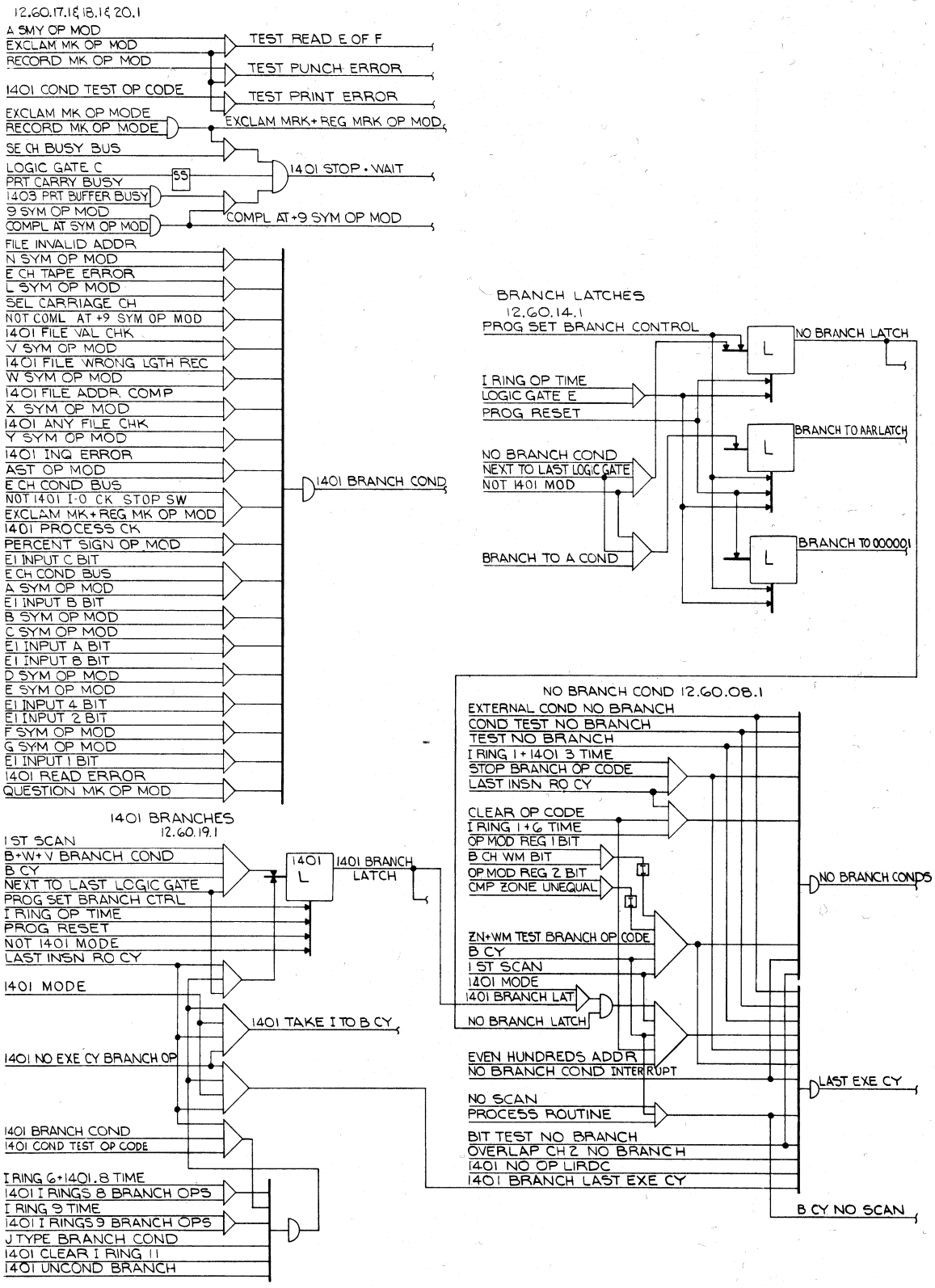
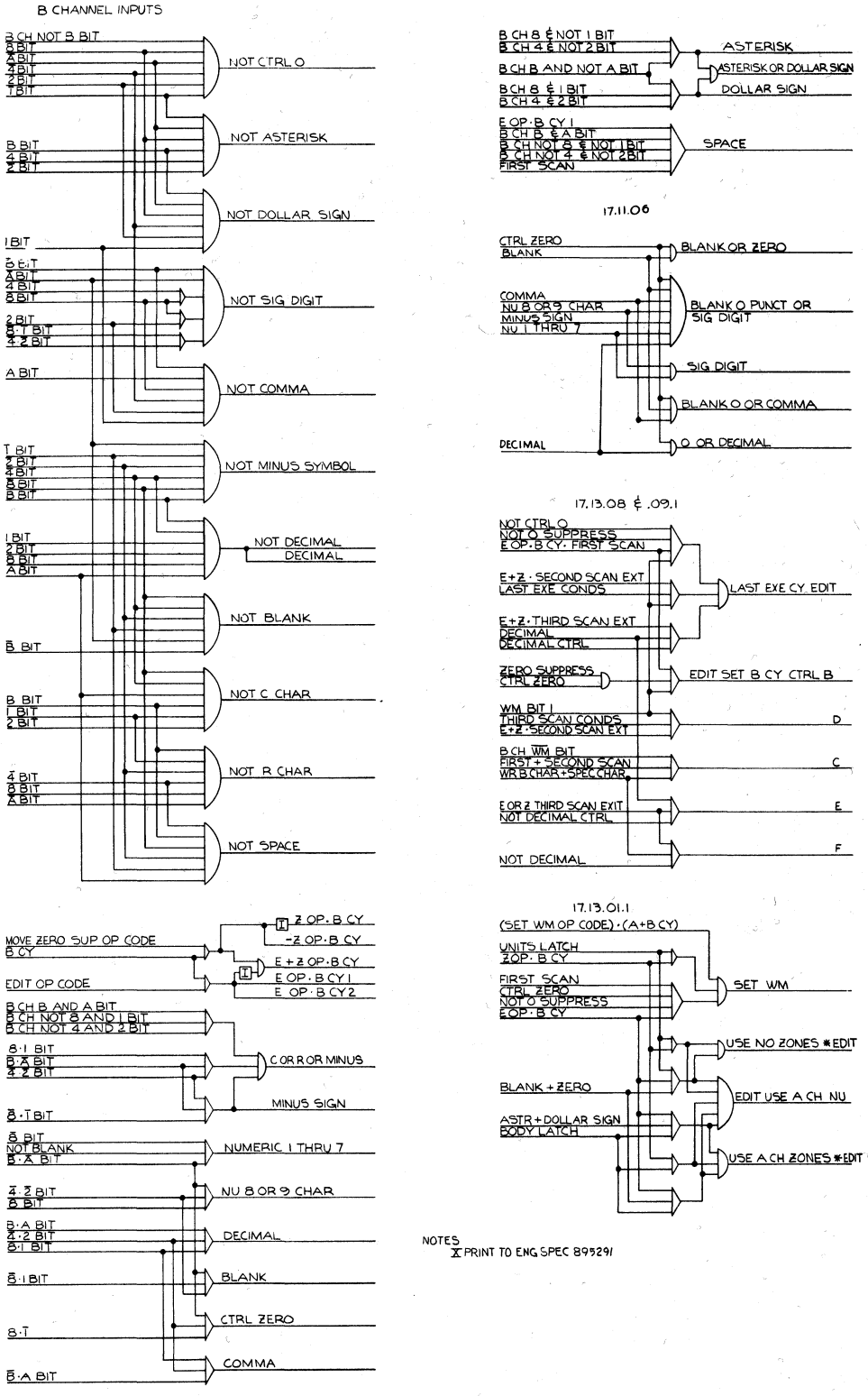


Figure 139. 1401 Branch and No Branch Conditions



NOTES
X PRINT TO ENG SPEC 89529/

Figure 140. Edit Translator and Controls

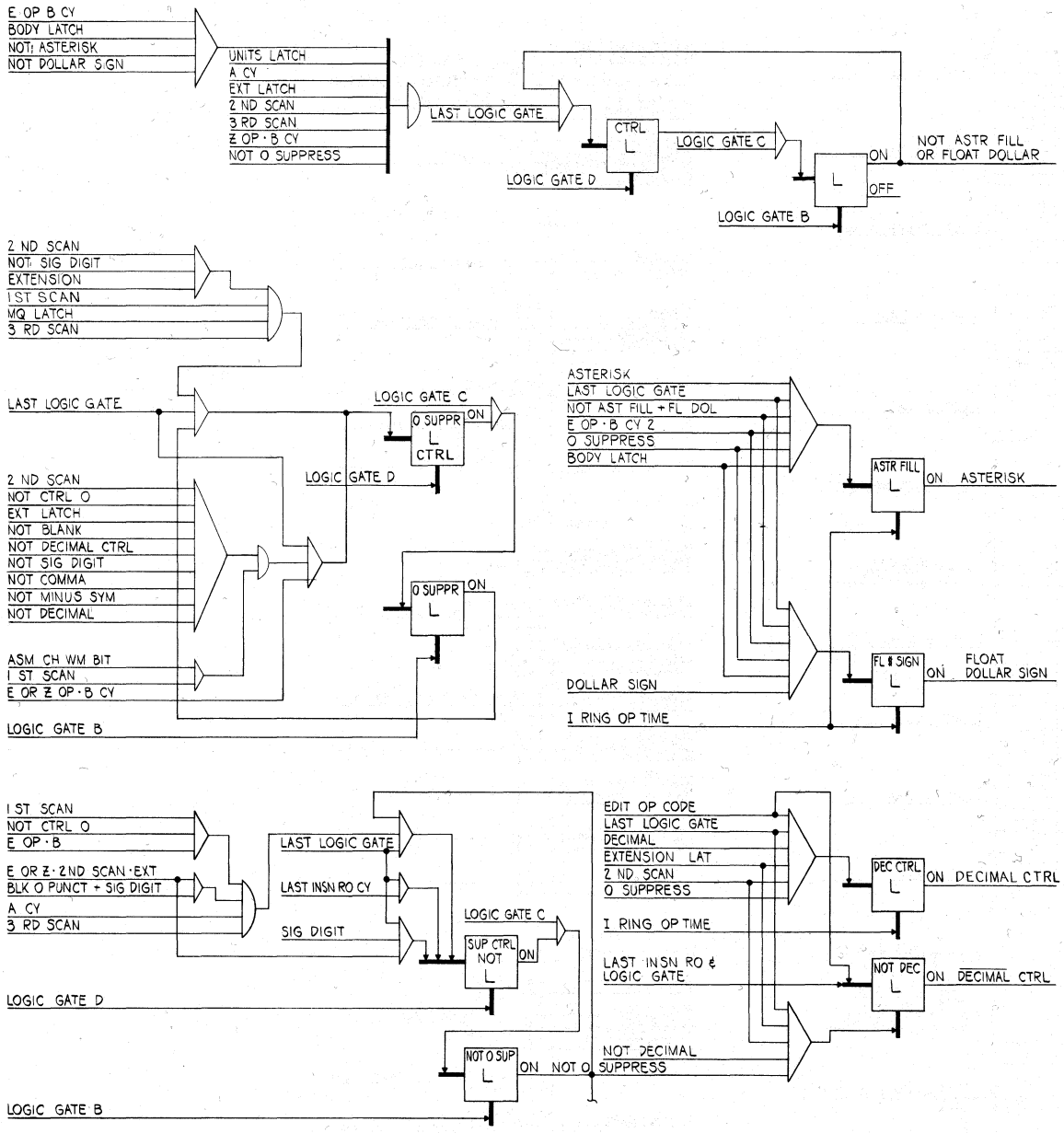


Figure 141. Edit Latches

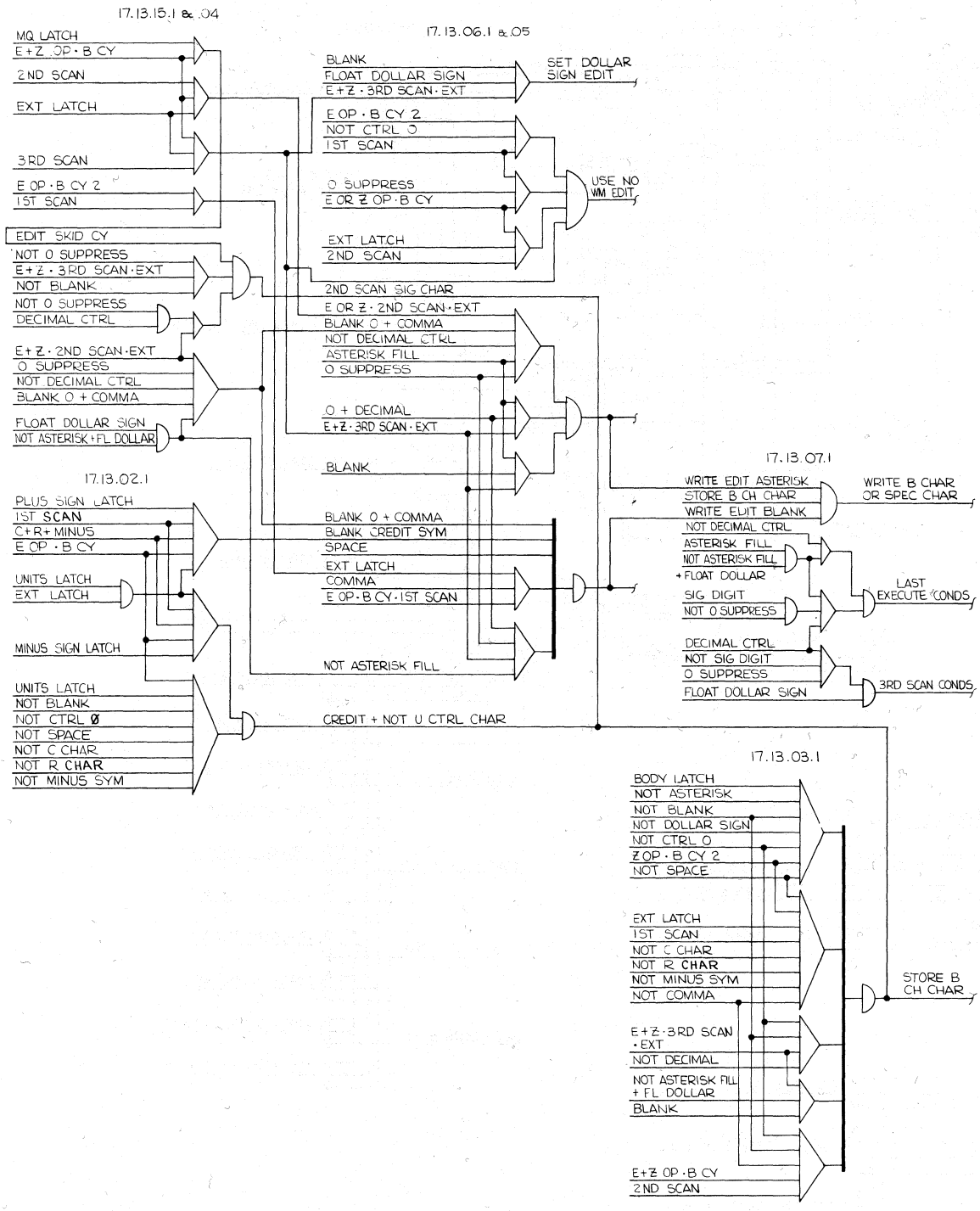


Figure 142. Edit Controls

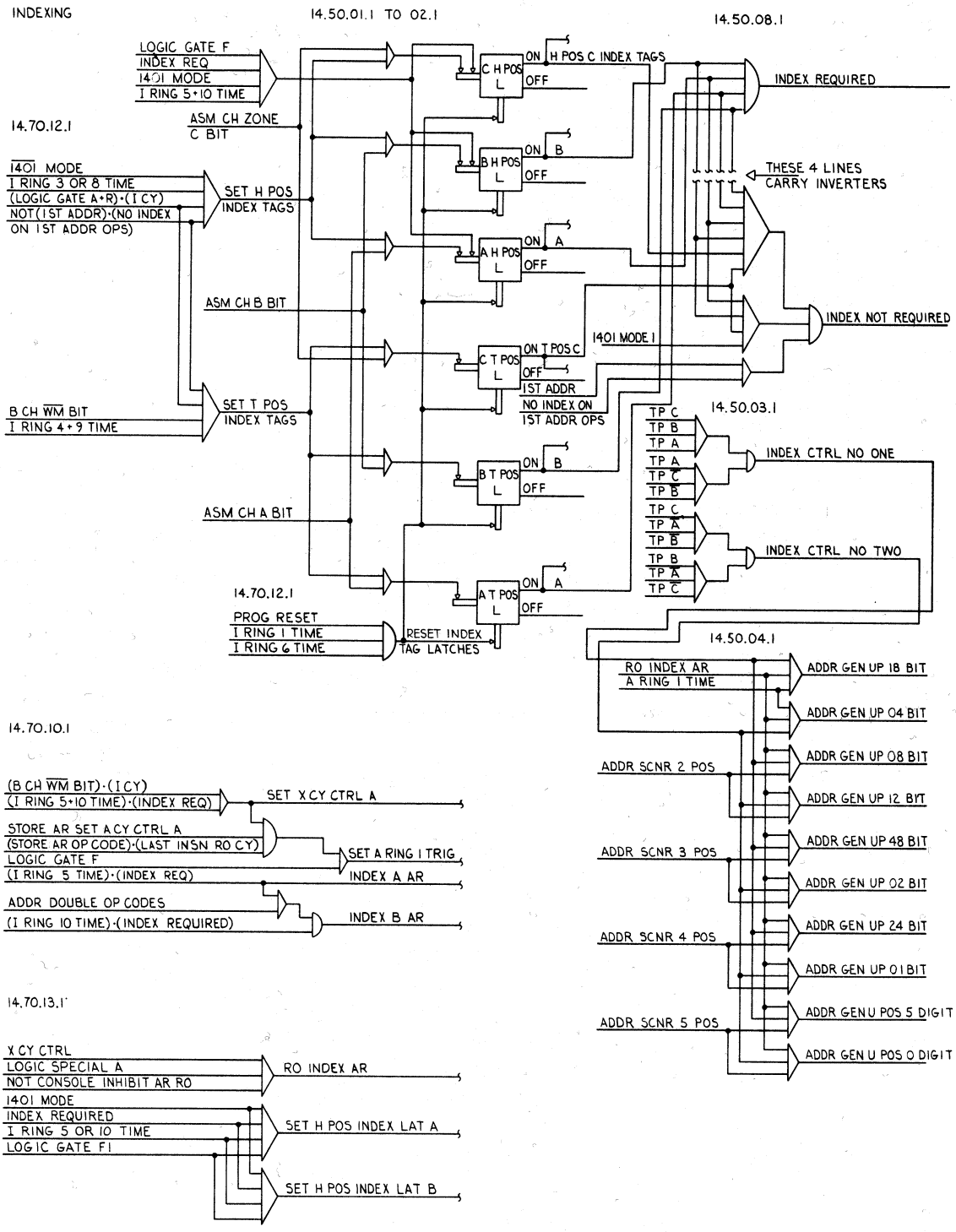


Figure 143. Indexing

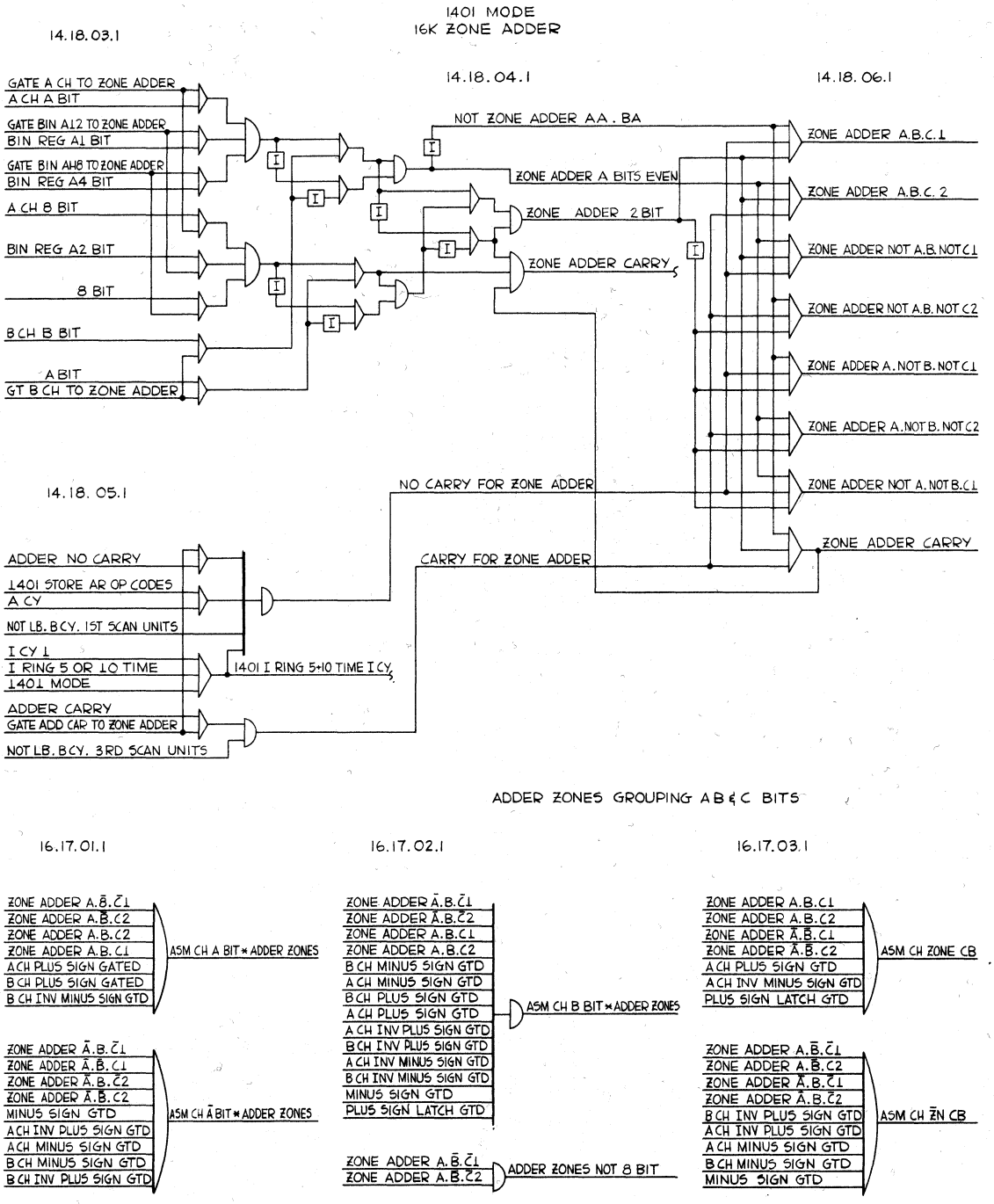


Figure 144. 16K Zone Adder and Grouping

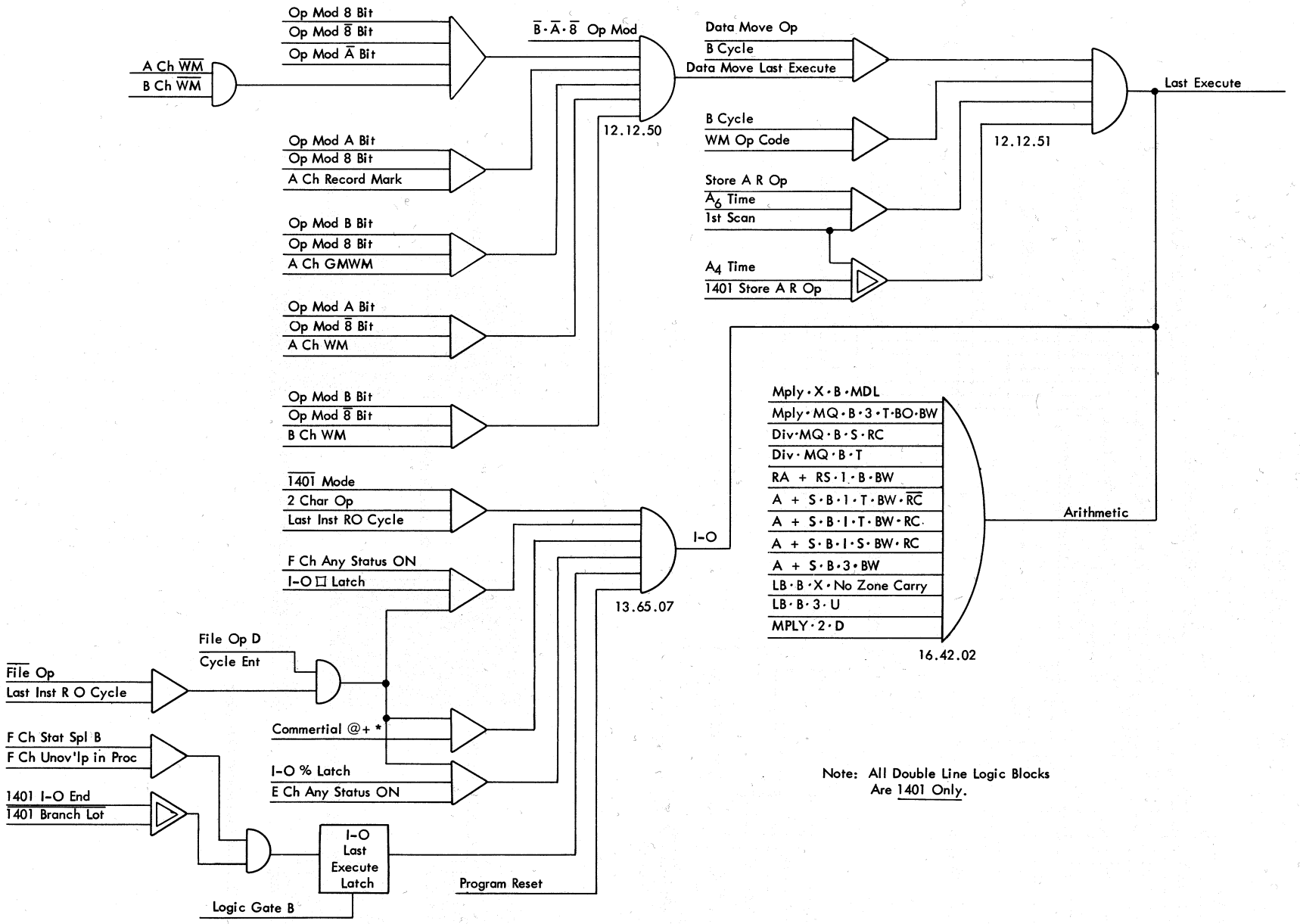


Figure 145. Last Execute (Sheet 1 of 2)

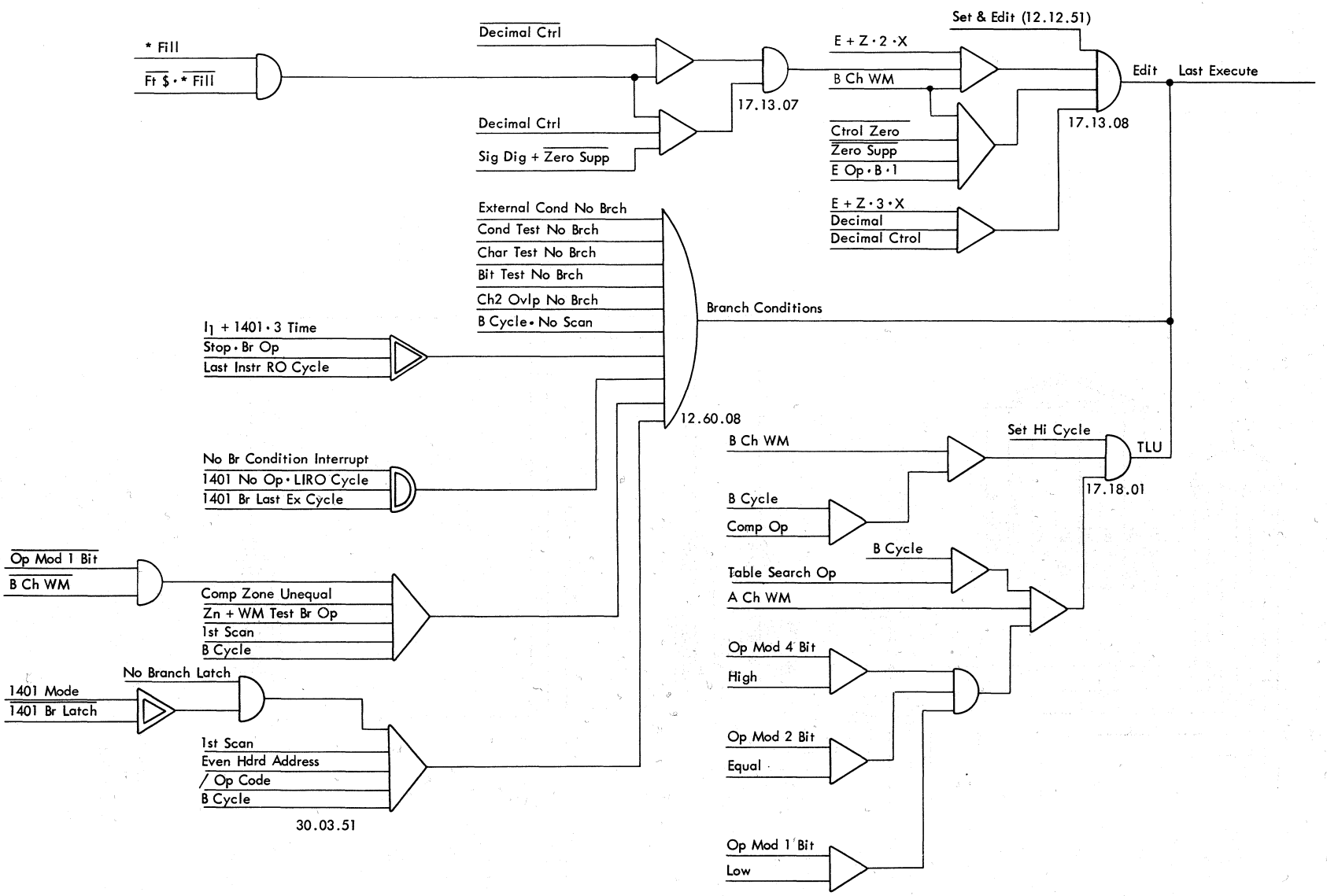
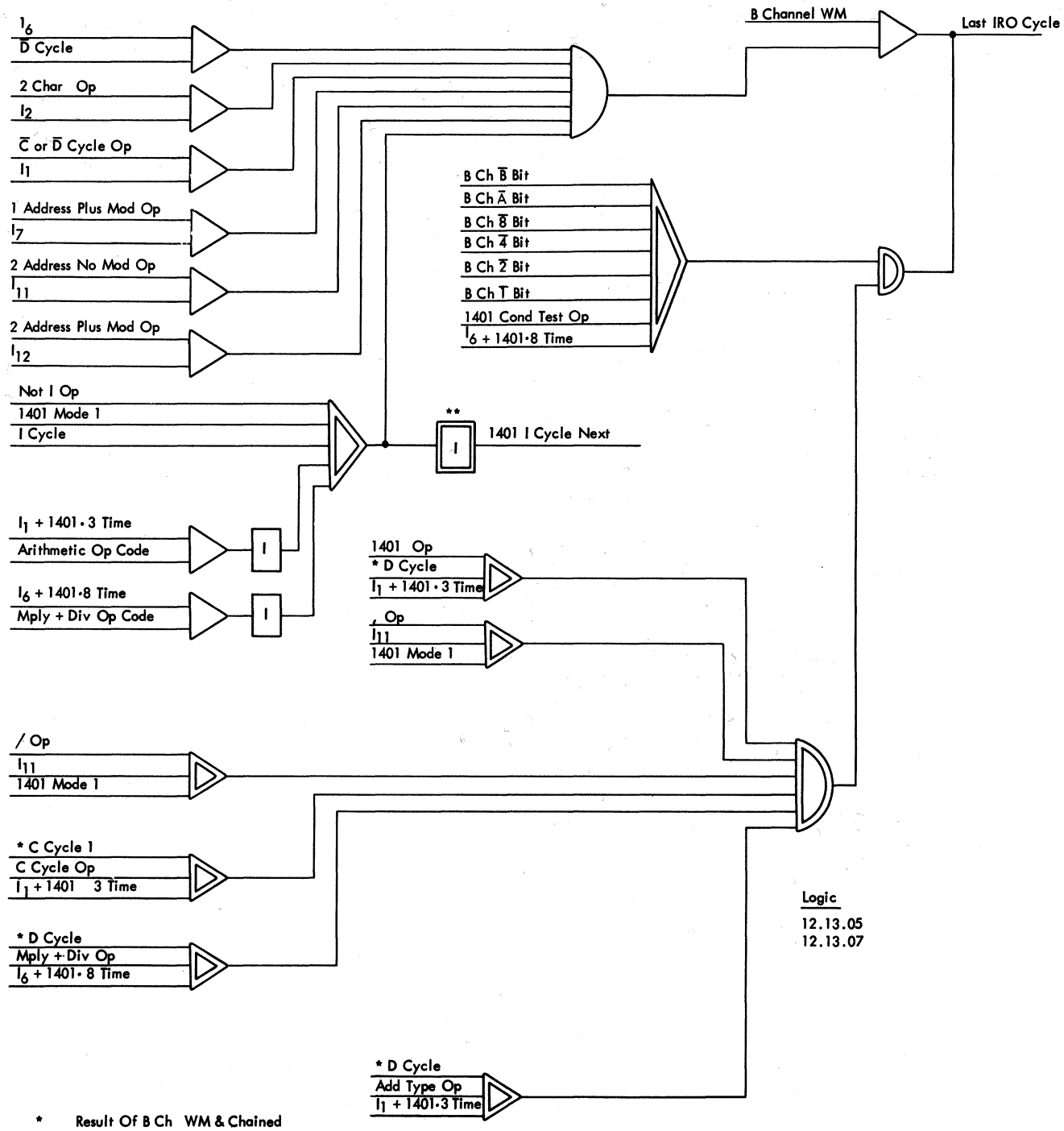


Figure 145. Last Execute (Sheet 2 of 2)



* Result Of B Ch WM & Chained Op Code

** Voltage Inverter

Note: All Double Line Logic Blocks Are 1401 Only

Figure 146. Last Instruction Read-Out

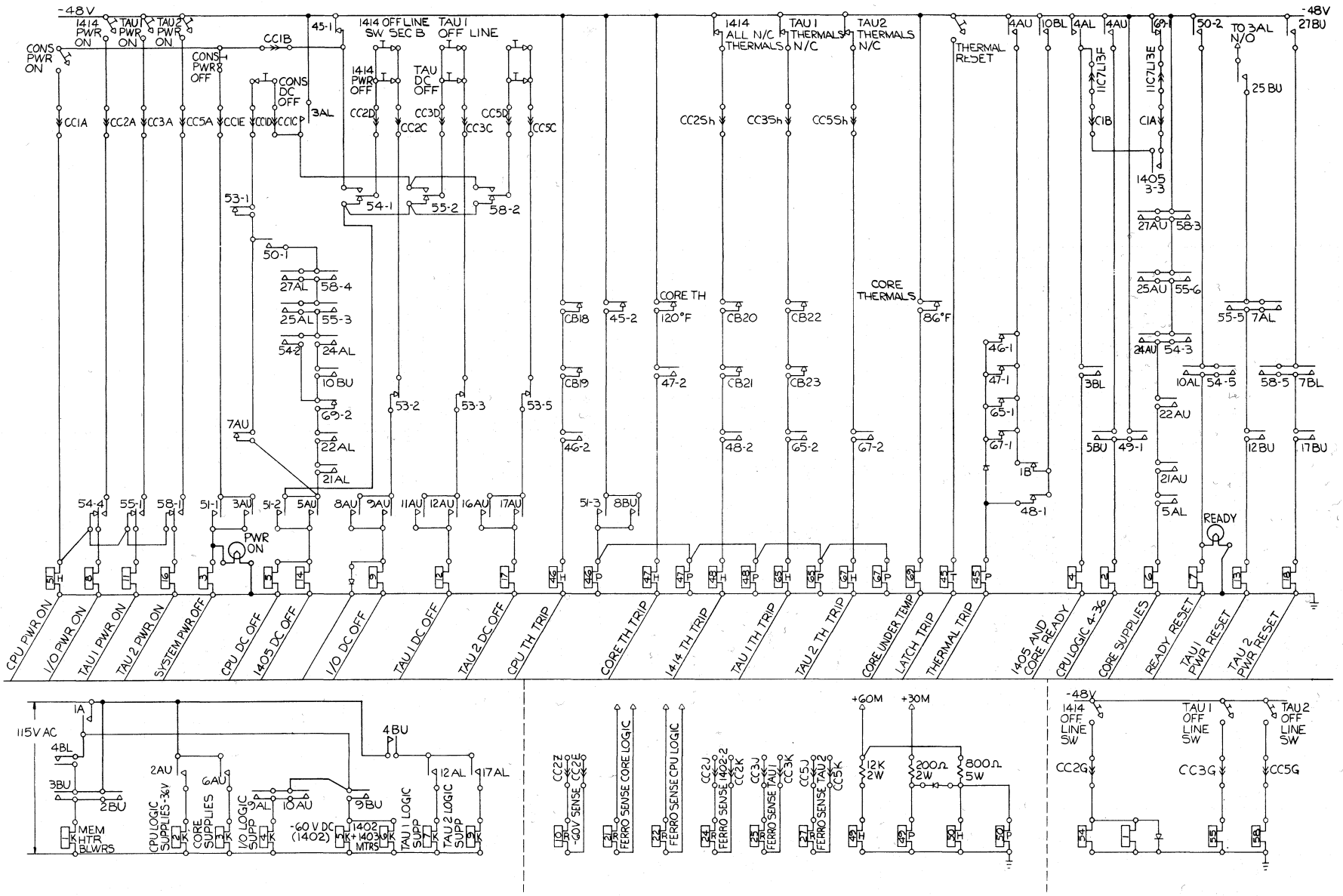


Figure 147. 1410 Power Distribution

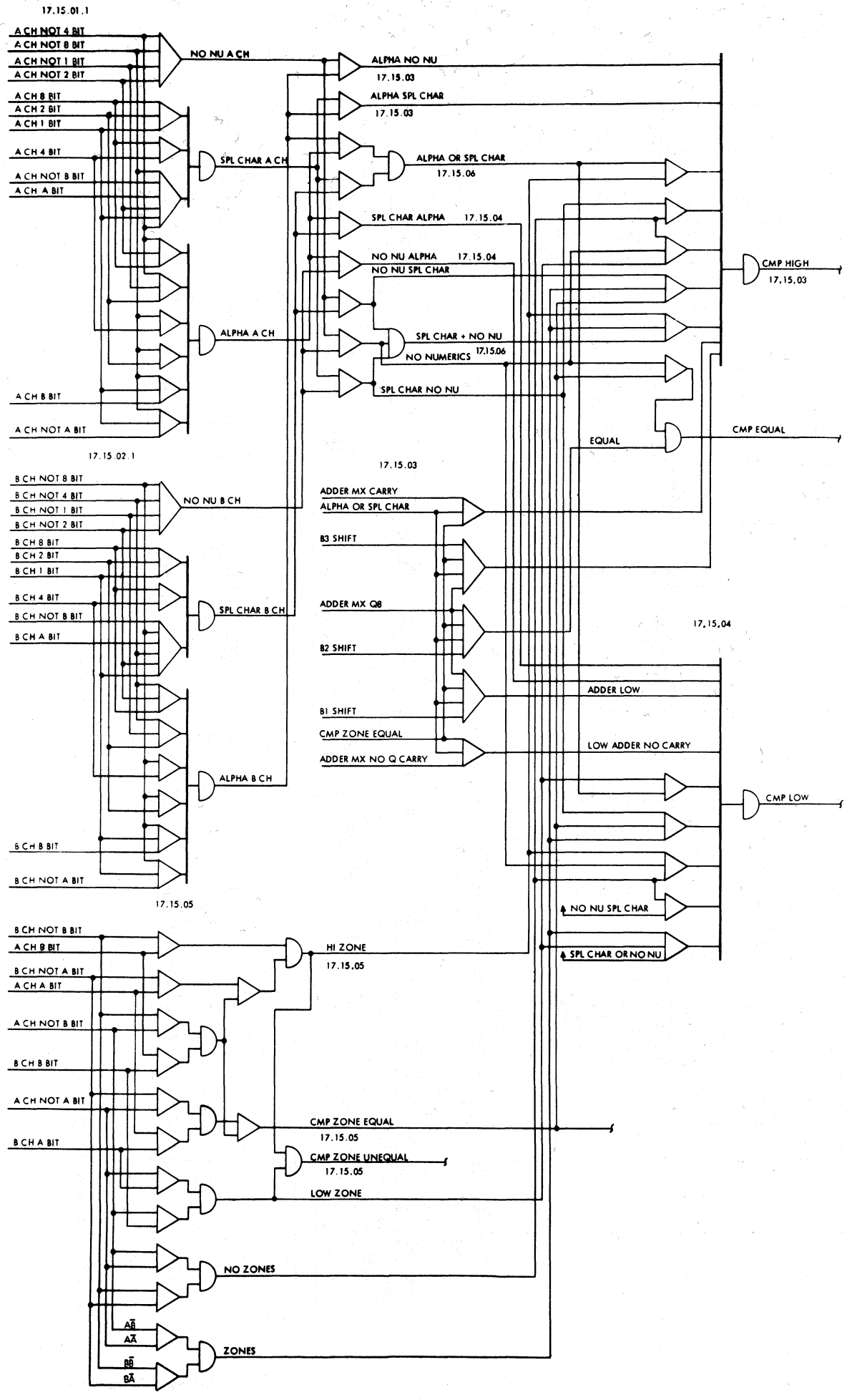


Figure 148. Compare Matrix

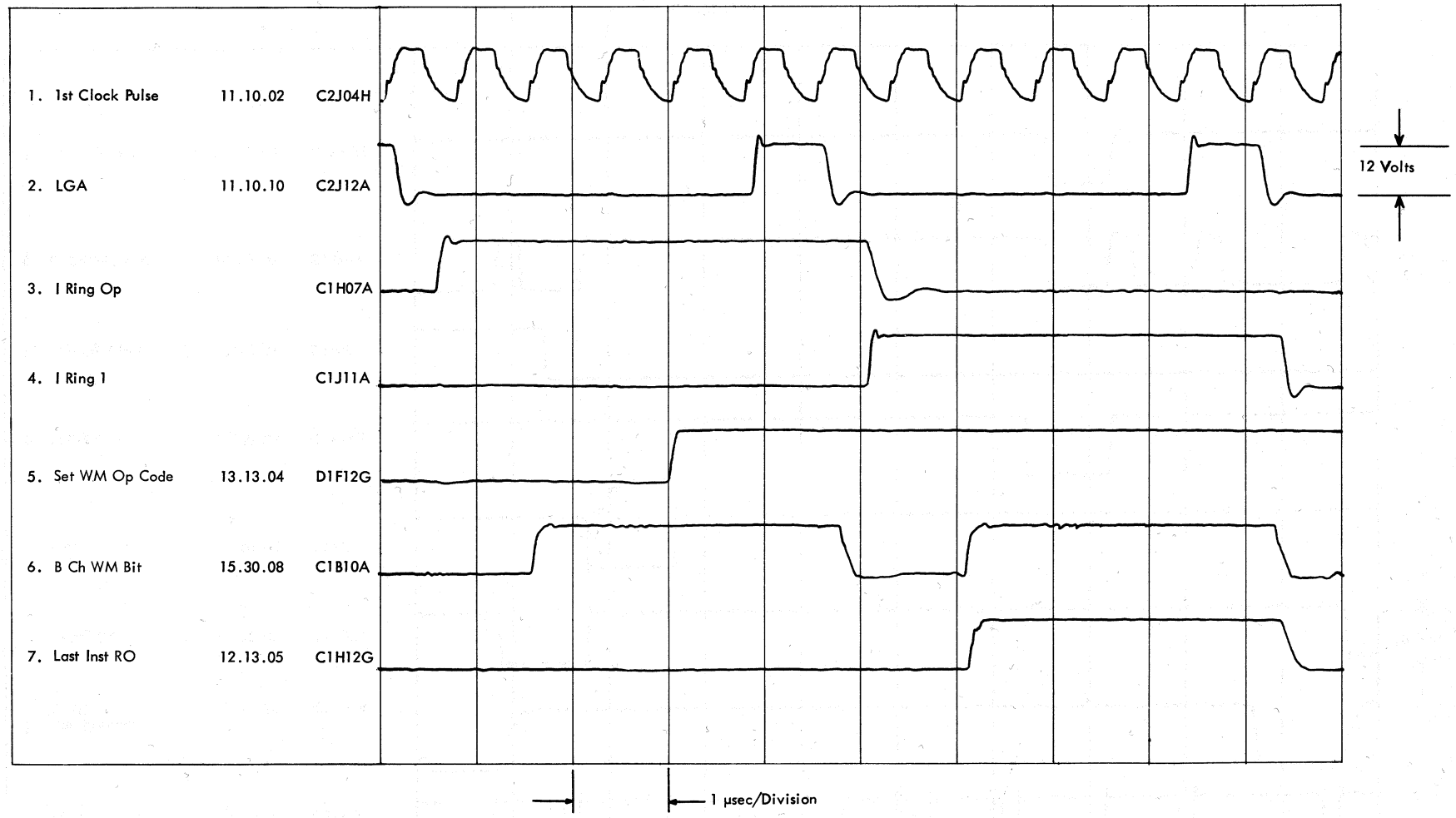


Figure 149. One Character Instruction Read-Out Op Code

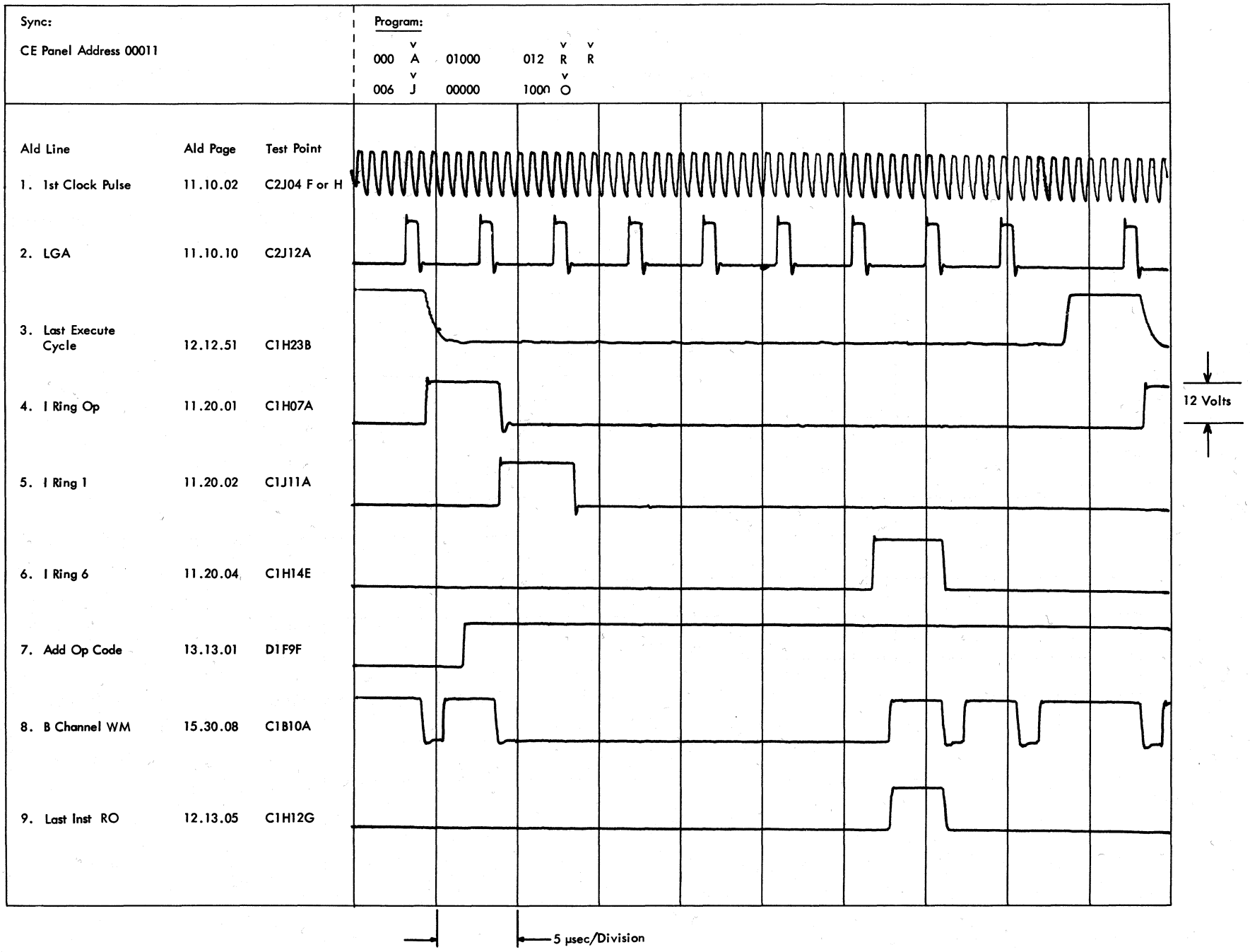


Figure 150. Six Character Instruction Read-Out Op Code

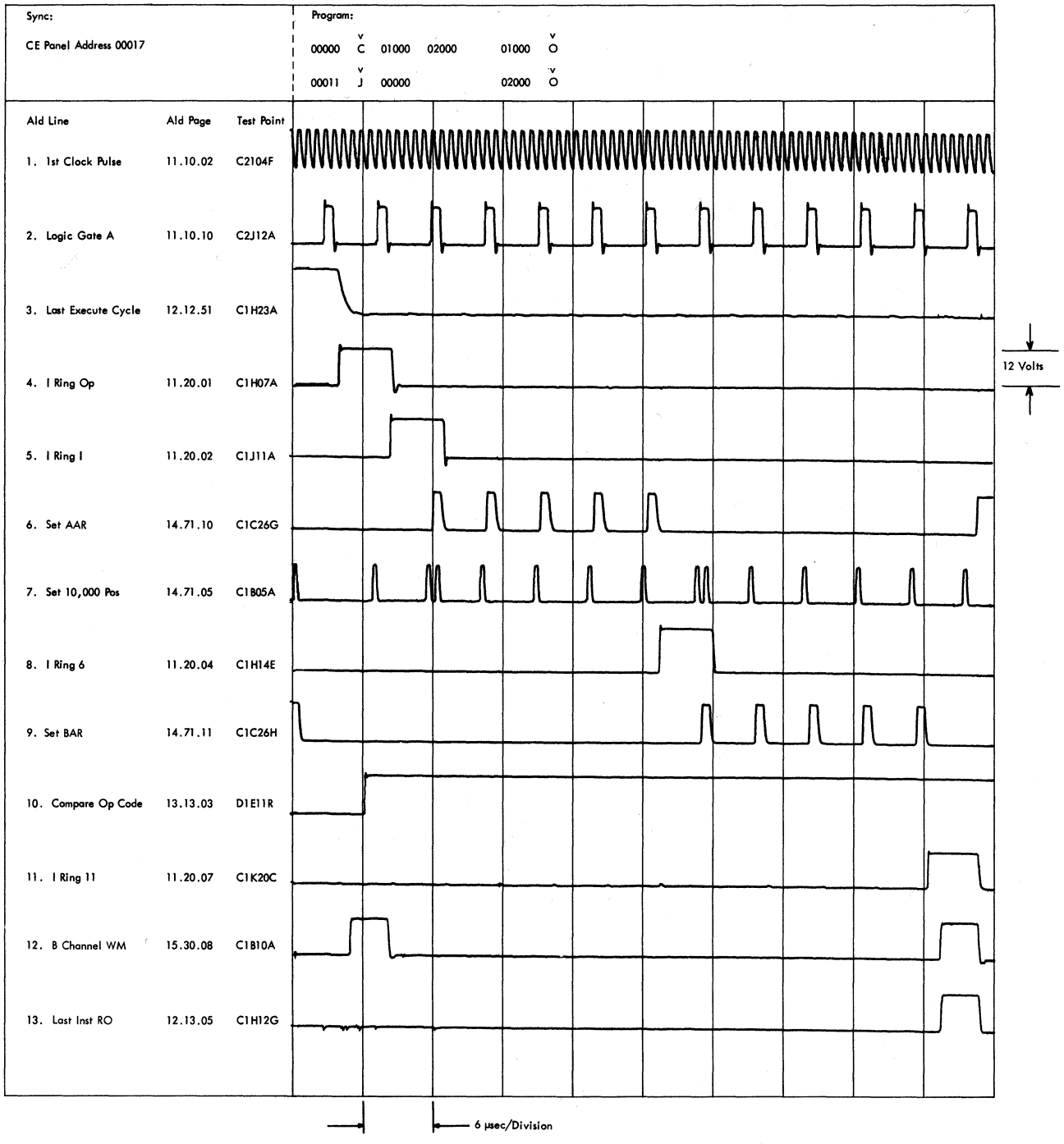


Figure 151. Eleven Character Instruction Read-Out Op Code

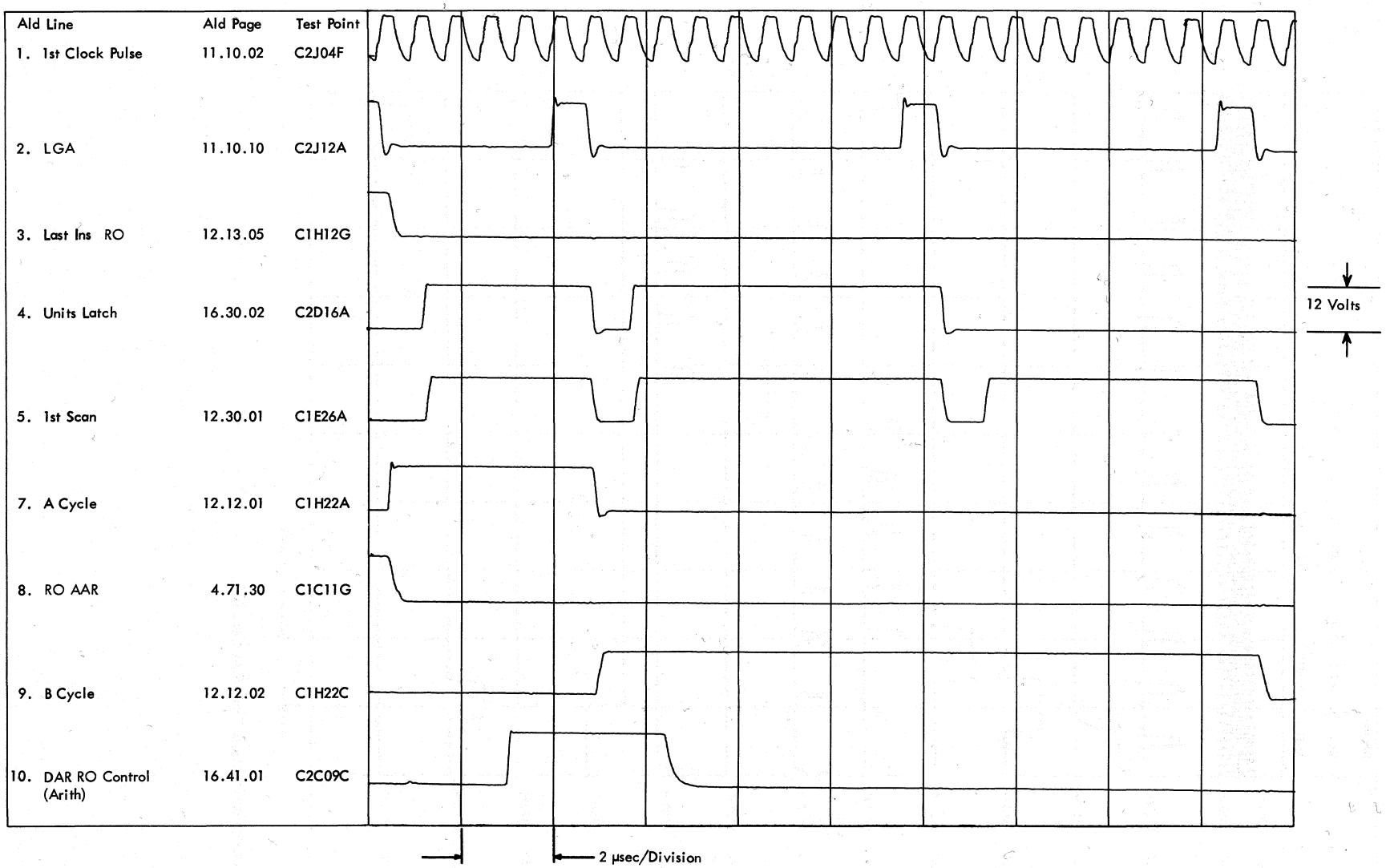


Figure 152. Add Execute Phase Op Code (Sheet 1 of 2)

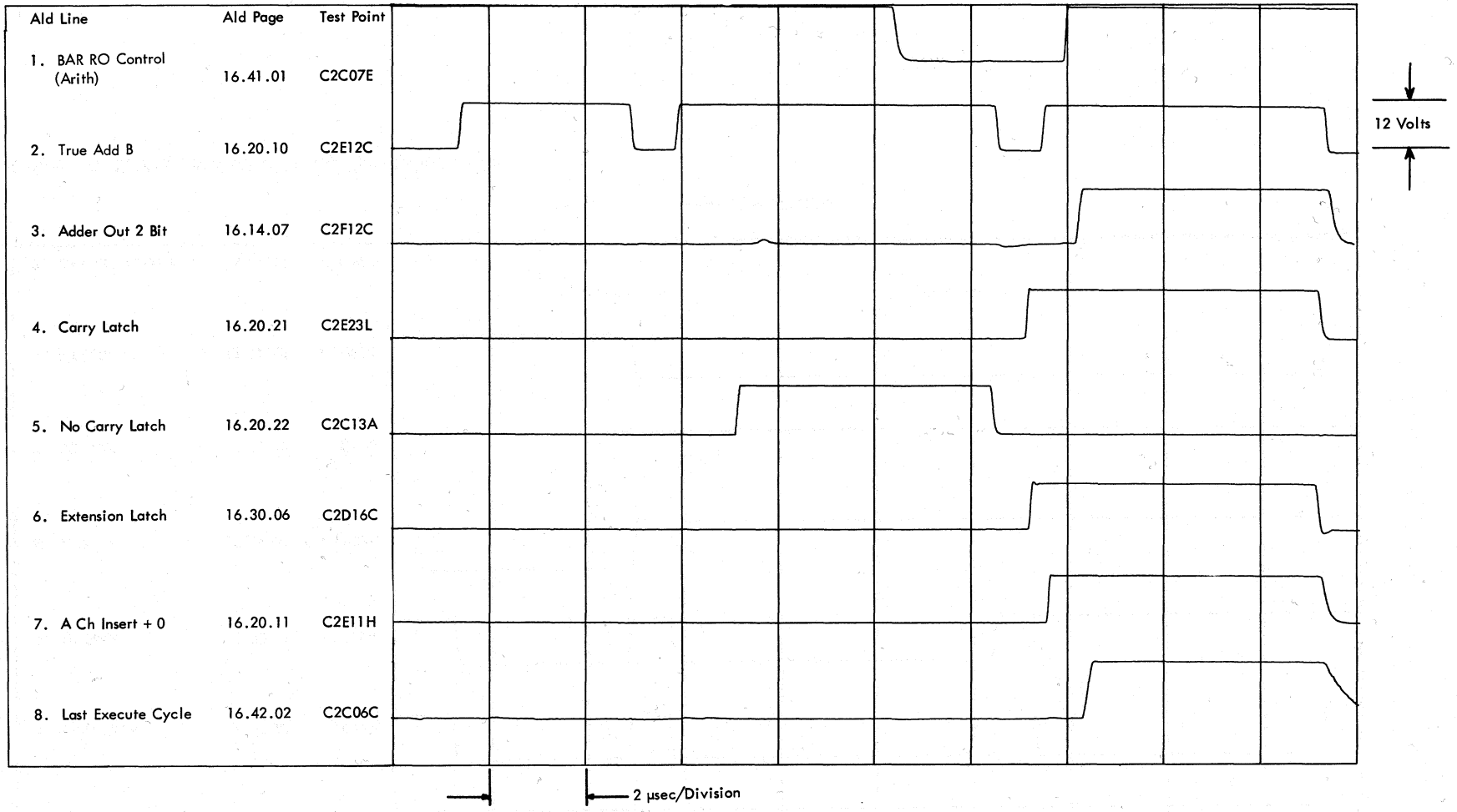


Figure 152. Add Execute Phase Op Code (Sheet 2 of 2)

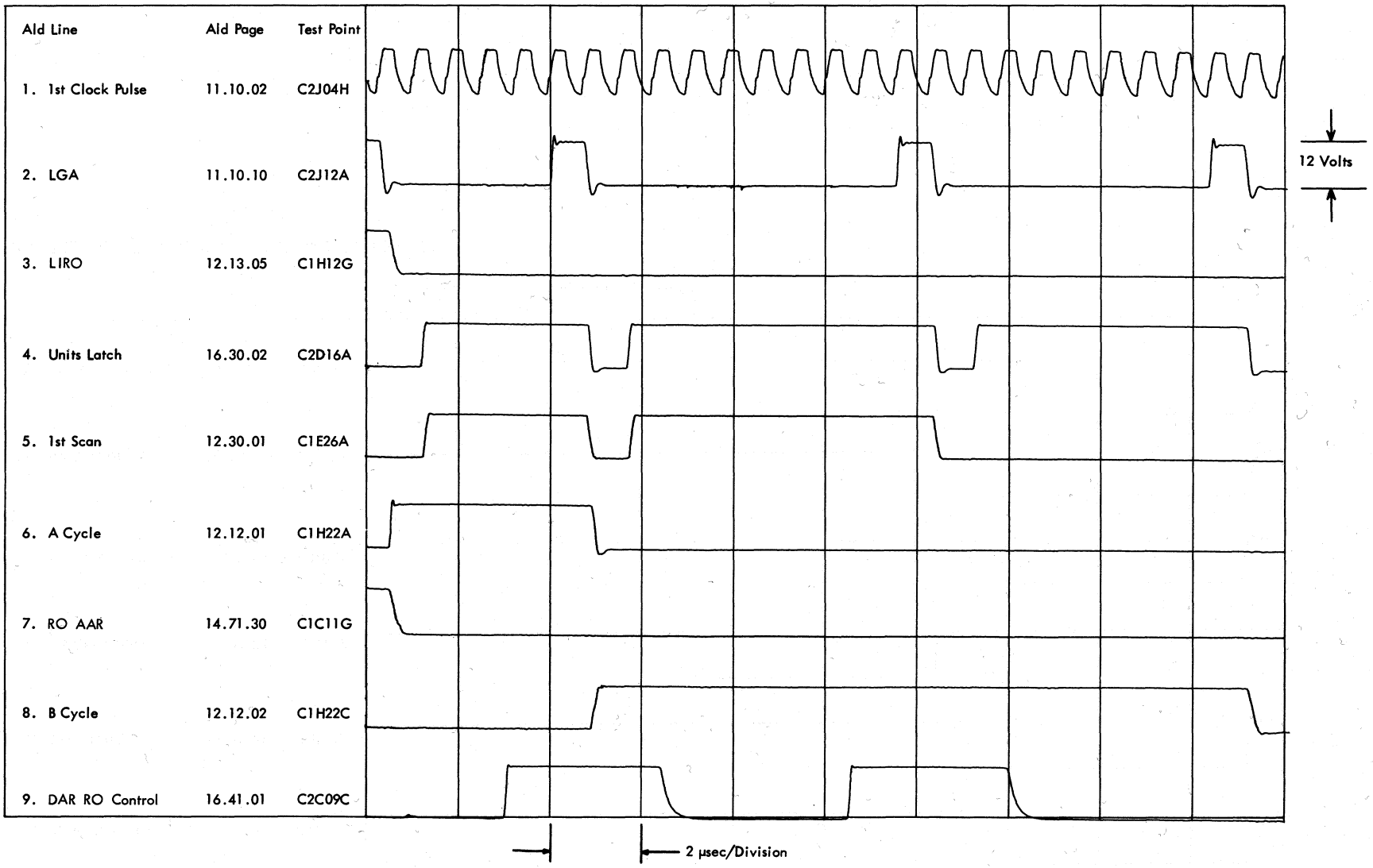


Figure 153. Subtract Execute Phase Op Code (Sheet 1 of 2)

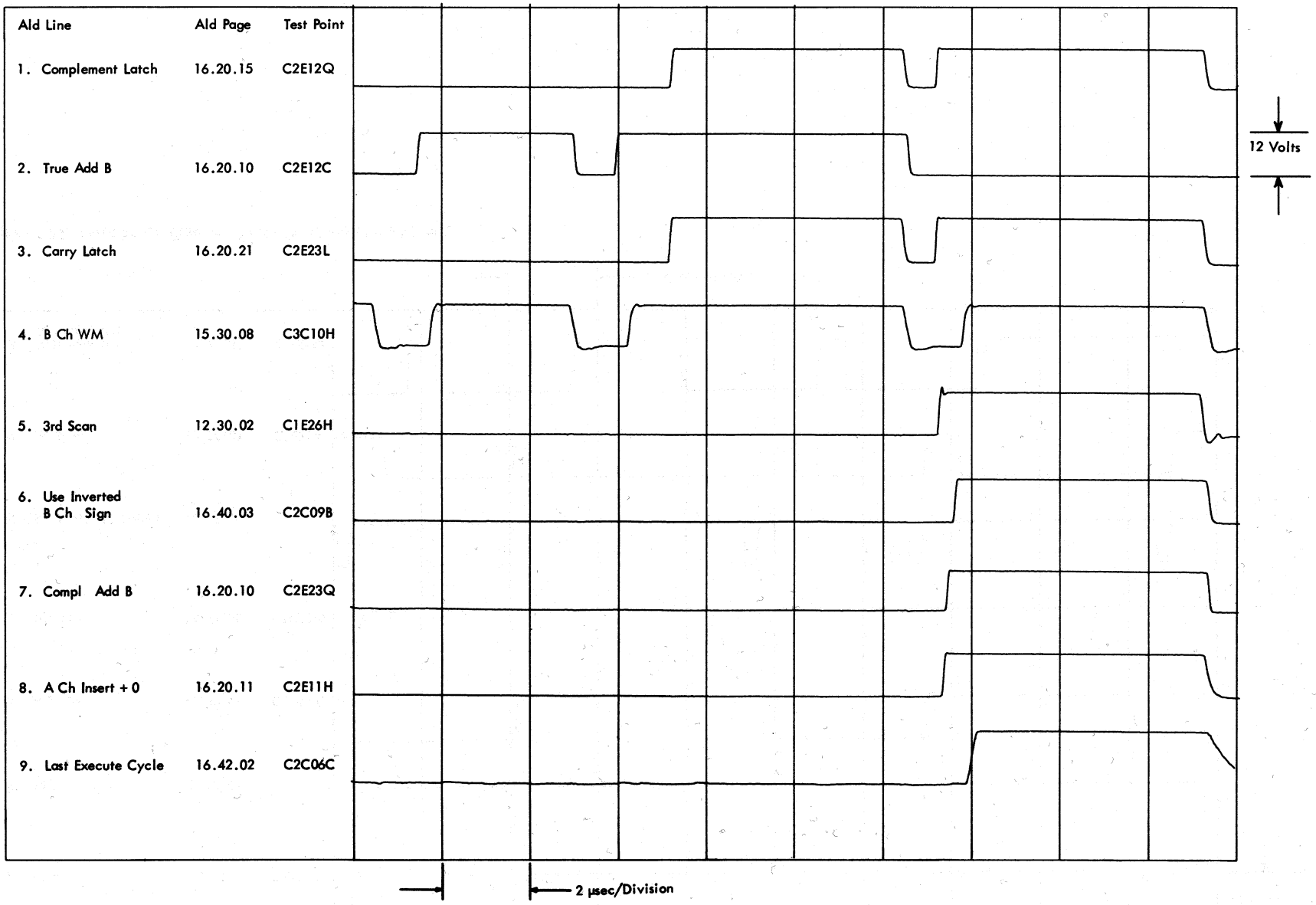


Figure 153. Subtract Execute Phase Op Code (Sheet 2 of 2)

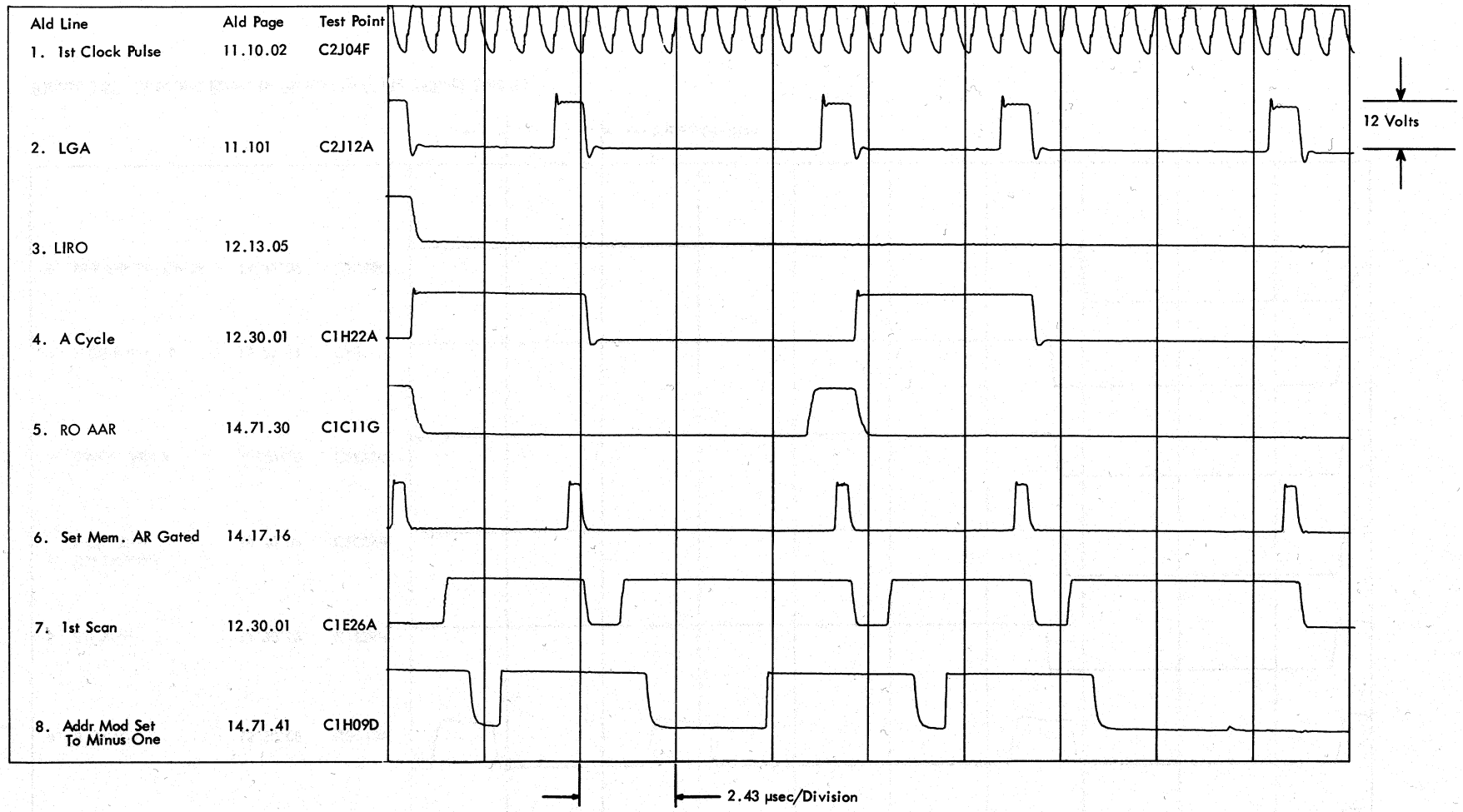


Figure 154. Data Move Execute Phase Op Code (Sheet 1 of 2)

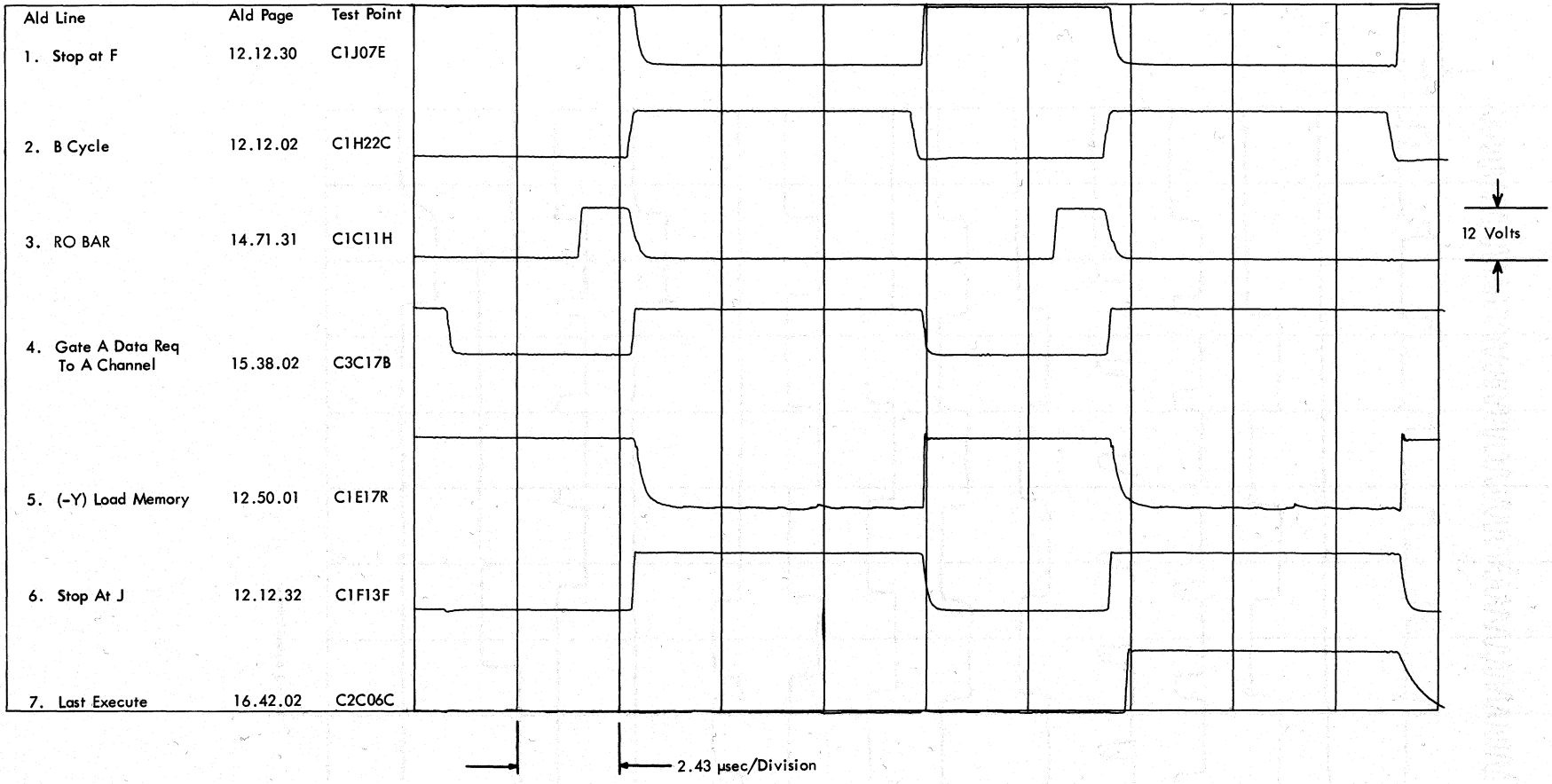


Figure 154. Data Move Execute Phase Op Code (Sheet 2 of 2)

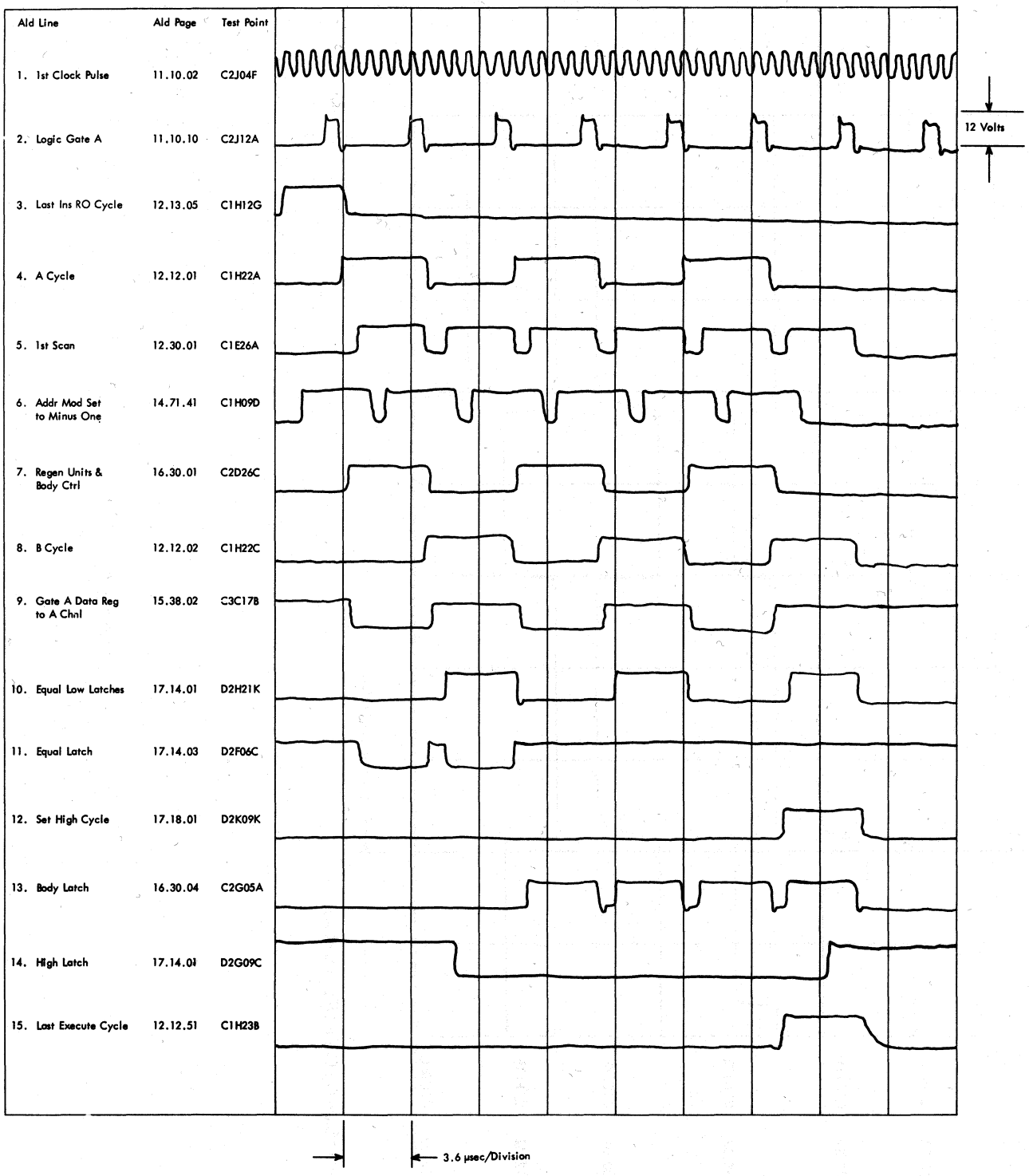


Figure 155. Compare Execute Phase

COMMENT SHEET

IBM 1410 SYSTEM FUNDAMENTALS

Customer–Engineering Instruction–Reference, S223-2589

FROM

NAME _____

OFFICE NO. _____

FOLD

CHECK ONE OF THE COMMENTS AND EXPLAIN IN THE SPACE PROVIDED

FOLD

☐ SUGGESTED ADDITION (PAGE , TIMING CHART, DRAWING, PROCEDURE, ETC.)

☐ SUGGESTED DELETION (PAGE)

☐ ERROR (PAGE)

EXPLANATION

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FOLD

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FOLD FOLD

FIRST CLASS
PERMIT NO. 81
POUGHKEEPSIE, N. Y.

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NO POSTAGE STAMP NECESSARY IF MAILED IN U. S. A.

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IBM CORPORATION
P.O. BOX 390
POUGHKEEPSIE, N.Y.

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