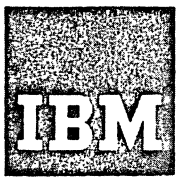
File No. 1800-19
Order No. GA26-3591-3



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IBM 1801 and 1802 Processor-Controllers Original Equipment Manufacturers' Information

This Original Equipment Manufacturers' Information (OEMI) manual provides the definitions and functional descriptions of the interface lines for the IBM 1801/1802 I/O Interface. In addition, it contains electrical, mechanical, and cabling considerations and specifications of this interface. It is assumed that the reader of this manual is engineering oriented and understands computer engineering techniques and terminology.

Preface

This document provides information of interest to designers and manufacturers of equipment to be attached to the IBM 1801/1802 Processor-Controllers. The responsibility of IBM resulting from such an attachment is defined in the *Multiple Supplier System Bulletin,* Order No. G120-6648.

The 1801/1802 I/O interface is a communication link between channel elements and I/O adapters in the IBM 1800 System. It provides an information format and control signal sequence capability as well as a uniform means of attaching and controlling various types of I/O devices.

Information in the form of data, status and sense information, control signals and I/O device addresses, is transmitted in both directions over the signal control lines of this interface. All transmissions are interlocked with corresponding response signals permitting the processor-controller (independent of the I/O transfer) to continue execution of other instructions.

The design of this interface provides these important features:

- Ease of input/output programming over a wide range of control units.
- Ready connection of both IBM and non-IBM designed control units to the IBM 1800 System.
- Ability to accommodate all future control units designed with the parameters of this interface.
- An interlocked interface operation that is not time-dependent; this permits broad ranges of control unit attachments.
- An operation uniformly applicable to both multiplex and data channel operations as well as to channel-to-channel transmission and control operations.

This Original Equipment Manufacturers' Information (OEMI) manual provides a functional description of these lines together with the electrical, mechanical and cabling considerations, and specifications of the interface. It defines the interfaces between the I/O adapters in the 1801/1802 and the I/O devices.

All descriptions and data in this manual are subject to modification as a result of engineering developments.

Related Literature

The *IBM 1800 Data Acquisition and Control System Bibliography*, Order No. GA26-5921 lists the available reference publications for the 1800 System and associated I/O devices.

The *IBM 1800 Installation Manual-Physical Planning,* Order No. GA26-5922 contains additional information and descriptions concerning process I/O interfaces.

Fourth Edition (March 1970)

This publication Order No. GA26-3591-3 is a major revision, replacing and making obsolete GA26-3591-2. This revision covers additional features added to the 1800 system. This publication has been completely revised and should be reviewed for changes.

Significant changes or additions to the specifications contained in this publication are continually being made. When using this publication in connection with the operation of IBM equipment, check the latest SRL Newsletter for revisions or contact the local IBM branch office.

Manuals referred to in this publication that have an Order No. with a four character prefix are identical in content to the same manual without the initial prefix character. (e.g., GA26-xxxx-Y is the same in content as A26-xxxx-Y.)

The illustrations in this manual have a code number in the lower corner. This is a publishing control number and is not related to the subject matter.

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This manual was prepared by the IBM Systems Development Division, Product Publications, Department G24, San Jose, California 95114. Send comments concerning the contents of this manual to this address.

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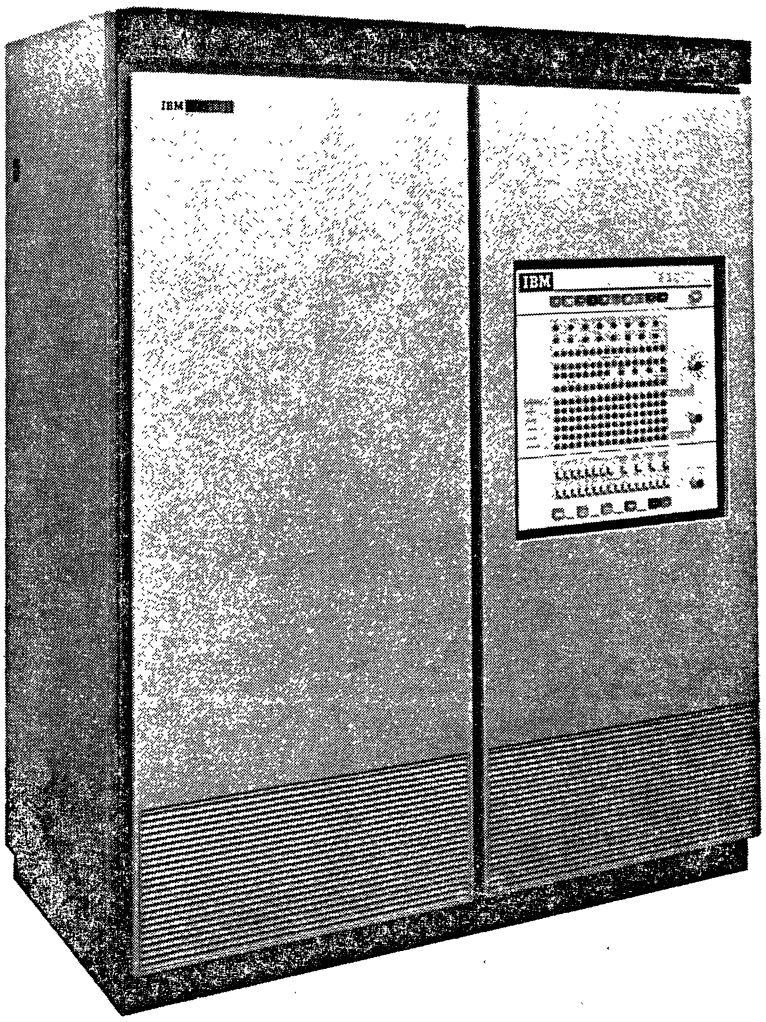


IBM 1801/1802 Processor-Controller

Introduction

The 1801 and 1802 Processor-Controllers (P-C) are available in several models, depending upon the core storage capacity and cycle time desired. Five core storage sizes are available in the 1801 or 1802 — 4096; 8192; 16,384; 24,576; 32,768 words — with storage cycle times of 2 or 4 microseconds (2.25 microseconds with the additional storage feature).

Additional storage is available in the 1803 core storage unit in increments of 8192 words, with a combined system maximum of 65,536 words. With the additional storage feature, the 1801 or 1802 contains 24,576 words, and the additional 16,384 to 40,960 words are located in the 1803.

In addition to the many special features available, the standard features include: three data channels, three index registers, three interval timers, 12 levels of interrupt, operations monitor, storage protection, power failure protection, parity, double precision arithmetic, multiply-divide, and an operator's console. The IBM 1802 provides magnetic tape control in addition to the above mentioned features.

IBM 1803 CORE STORAGE UNIT

The IBM 1803 Core Storage Unit is a free standing unit designed to allow for expansion of core storage size above the 32,768 words available in the 1801 or 1802 Processor-Controller. With the additional storage feature, 24,576 core storage words are contained in the 1801 or 1802 with the additional storage in the 1803. The 1803 is available with 16,384 to 40,960 core storage words, in increments of 8192 words, for a maximum system core storage capacity of 65,536 words.

I/O CHANNEL

Input/output devices are attached to the I/O channel via I/O adapters which interface to the I/O channel (Figure 1). The adapters, which can be located physically within the I/O device or the P-C, provide the logical capability necessary to operate and control the devices, and adapt the characteristics of the device to the standard controls provided by the I/O channel. Usage of the I/O channel is on an assigned priority basis, with the P-C having the lowest priority.

The processor-controller I/O channel provides for communication between the P-C and the I/O adapters. All data transfers between the P-C core storage and the I/O devices require the use of the I/O channel.

Data Channel

Data channels control high speed data transfer, via the I/O channel, between I/O devices and core storage by a method called cycle-stealing. Each data channel has a fixed priority for usage of the I/O channel.

Assignment of an I/O device to a data channel assigns the priority level (for usage of the I/O channel) of the I/O device. Three data channels are standard and 12 additional are optional.

Interrupt

Twelve levels of interrupt are standard in the 1801 or 1802. Twelve additional levels are available in groups of six. Sixteen separate interrupts can be assigned to each level. These interrupts are generated by programmed instruction; the data processing I/O units, process I/O units and features, and the attachment circuitry. The customer can assign interrupts to any priority level, thus determining the priority of interrupts of the I/O device on the system. Interrupt levels are wired by IBM according to the information supplied on the Interrupt Level Assignment Form.

Operations Monitor

The operations monitor is a device which causes a contact to close upon completion of a preset timeout period (selectable between 5 and 30 seconds ±10%), or in event of an 1801/1802 power failure. It notifies the process operator when the processor-controller is not executing a predetermined sequence of instructions. The customer is to furnish the alarm device and its power. Power is limited to 30 volts (ac or dc) and 1 ampere maximum. Two wire terminations (external "sync" terminals 14 and 15), using number 8 barrier type terminals, are provided in a customer accessible location in the machine.

PROCESS I/O

The process I/O is divided into four general categories: analog input, digital input, digital output, and analog output. (For additional process I/O information refer to *IBM 1800 Installation Manual-Physical Planning,* Order No. GA26-5922.)

Analog Input

The following features associated with analog input are installed in the 1801 or 1802. Customer terminations for analog input are made to the 1851 terminals mounted in 1828 enclosures.

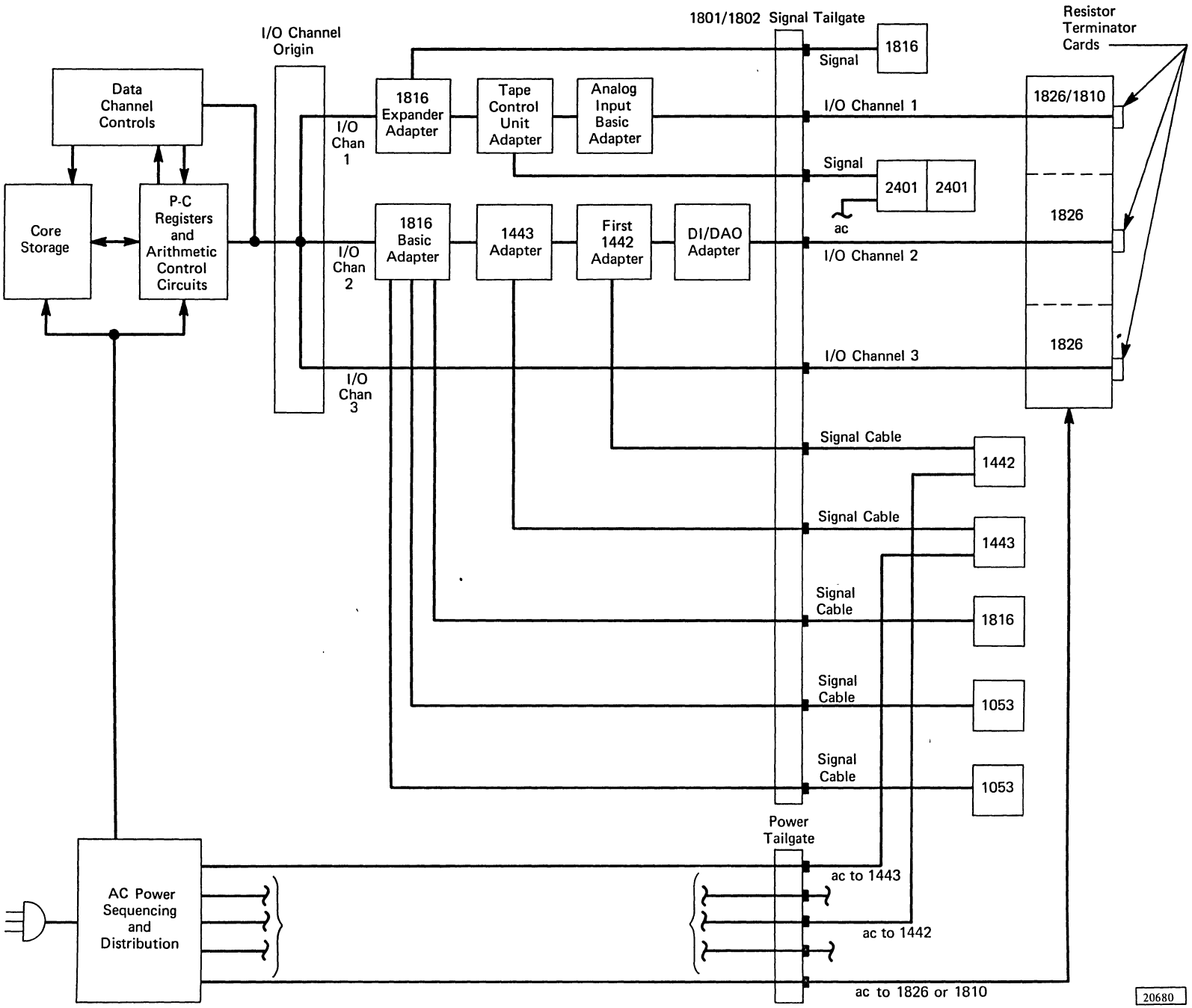


Figure 1. Input/Output Channel, Signal and Power Paths

Analog-Digital Converter, Mod 1. This feature converts analog signals to digital values with the following characteristics:

Input Type	Voltage, bipolar
Input Level	0 to ±5 volts
Input Impedance	10 megohms or greater
Output Value	8, 11 or 14 bits plus sign
ADC Conversion Time	29, 36 or 44 microseconds

The number of output bits is program selected. The ADC includes a buffer amplifier.

Conversions can be synchronized from an external signal. After a point is addressed, a "ready" condition is transmitted to an external customer device; this device provides a "sync" pulse which either starts conversion for relay points or starts multiplexing for solid state points. Sync and ready signal termination are in the 1801, 1802, 1826 with AI Expander, or 1827.

Analog-Digital Converter, Mod 2. This feature converts analog signals to digital values with the following characteristics:

Input Type	Voltage, bipolar
Input Level	0 to ±5 volts
Input Impedance	100K ohms
Output Value	8, 11, or 14 bits plus sign
ADC Conversion Time	29, 36, or 44 microseconds

The program selects the number of output bits. The ADC includes a sample and hold amplifier to allow higher conversion rates, and can be synchronized from an external signal.

After a point is addressed, a "ready" condition is transmitted to an external customer device. This device provides a "sync" pulse which starts conversion for relay points or starts multiplexing for solid state points.

Comparator: This feature performs automatic range checking on digital values developed by the Analog-Digital Converter Mod 1 or Mod 2. High and low limits are obtained from the processor-controller core storage via the data channel that transmits their addresses for the analog input operation (random mode only). An out-of-limits condition alerts the processor-controller with an interrupt that permits the address of that input signal to be obtained under direct program control.

Multiplexer Overlap: Provides for overlap (simultaneous selection) of multiplexer/R (relay) and multiplexer/S (solid state) analog input multiplexer points. This allows high speed scanning and conversion of the multiplexer/S points to occur while the slower multiplexer/R points are being selected.

Multiplexer/R Control: This feature provides the necessary circuitry to operate up to 16 multiplexer/R groups.

Multiplexer/S Control: Multiplexer/S control provides circuitry to operate up to 16 multiplexer/S high-level single-ended groups.

Digital Input

The following digital input features may be installed in the 1801 or 1826. The number of each of the following available in an 1801 is dependent on the particular combination of features ordered and/or the termination capacity. When an 1802 is used on a system these features are located exclusively in the 1826.

Digital Input – Contact: Each group provides the status sensing circuitry and the terminals for up to 16 customer isolated, dry contacts.

Digital Input – Voltage: Each group provides the status sensing circuitry and the terminals for up to 16 customer voltage levels. A high speed option with unfiltered inputs allows switching rates up to 100 kc.

Pulse Counter (8-bit or 16-bit): Each pulse counter group provides two 8-bit or one 16-bit counter for counting pulse inputs.

External Synchronization

Digital input and pulse counter reading can be synchronized from an external signal. Digital input addressing can generate a "ready" signal which is transmitted to an external customer device. This device provides a "sync" pulse which initiates entry of digital input data into the processor-controller. Synchronization terminals are located in the 1801, 1802, or 1827.

Process Interrupt – Contact: Each group provides terminals for the customer and the latching circuits for sensing and interrupting when a change occurs in the status of up to 16 customer isolated, dry contacts.

Process Interrupt – Voltage: Each group provides the customer with terminals and the latching circuits for sensing and interrupting when a change occurs in the status of up to 16 voltage level inputs.

Digital Output

The following digital output features may be installed in either the 1801 or the 1826. The number of groups of each that are available for the 1801 is dependent on the particular combination of features ordered and/or the termination capacity. When an 1802 is used on a system these features are located exclusively in the 1826.

Electronic "Contact" Operate: Each group provides terminals for the customer and circuits for the electronic switching and latching of 16 customer lines carrying customer-supplied power up to 48 vdc at 0.45 amps.

Pulse Output: Each group provides terminals and circuits for momentary electronic switching of 16 customer lines, each carrying customer-supplied power up to 48 vdc at 0.45 amps with a duration of 3 milliseconds.

Register Output: Each register output group provides terminals and the circuitry for transmitting 16-bit words of binary data at repetitive speeds up to 500,000 words per second to customer registers. Voltage outputs are +3 volts for binary 1 and 0 volts for binary 0.

Analog Output

The 1801 or 1802 can provide the adaptation circuitry and cabling attachment for analog output features which are housed in 1856 terminals mounted in 1828 enclosures.

External Synchronization

A digital or analog output function can be synchronized from an external signal. Addressing of DAO can generate a "ready" signal which is transmitted to an external customer device. This device generates a "sync" pulse which initiates the output function. Termination is in the 1801, 1802, or 1827.

DATA PROCESSING INPUT/OUTPUT

The following DP I/O units can be attached to the 1801 or 1802:

- 2 – 1816 Printer-Keyboard
- 8 – 1053 Output Printer (6 with 2 – 1816s installed)
- 1 – 1054 Paper Tape Reader
- 1 – 1055 Paper Tape Punch
- 2 – 1442 Card Read-Punch, Model 6 or 7 (1 – 1442 if 1054 or 1055 or Data Channel Expander in system)
- 1 – 1627 Plotter, Model 1 or 2
- 1 – 1443 Printer, Model 1 or 2
- 1 – 1810 Disk Storage, Model A1, A2, A3, B1, B2, or B3
- 8 – 2311 Disk Storage Drives with one 2841 Storage Control
- 4 – Communication Adapters (2 Line Adapters per CA)
- 2 – 2790 Adapters

In addition, the 1802 will accommodate either:

- 1 or 2 – 2401 Magnetic Tape Units, Model 1, 2, or 3 or
- 1 – 2402 Magnetic Tape Unit, Model 1, 2 or 3

MACHINE LANGUAGE

The binary system enables the representation of numbers by any bi-stable means such as the on or off state of a flip-flop, the up or down level of a signal line, or the direction of the field about a magnetic device. In core storage, each bit value is stored in a magnetic core; in data registers each bit value is stored as the on/off condition of a flip-flop or flip-latch.

The binary representation of data best facilitates the parallel manipulation of fixed-length words and is the most efficient method of processing scientific data.

Data Format

In the 1800 system, the standard, or single-precision data word (Figure 2) is 16 bits in length. Bit positions 0 through 15 represent decimal values of 2^{15} through 2^0 respectively.

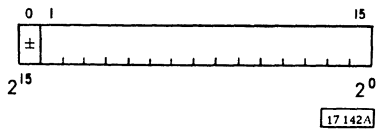


Figure 2. Single Precision Data Word

Positive numbers are represented in true binary form, whereas negative numbers are in two's complement form. The sign bit (position 0) is always 0 for positive numbers and 1 for negative numbers. The two's complement of a binary number is defined as its one's complement increased by one. The one's complement of a binary number is that number that results by replacing each 1 in the number with a 0, and each 0 with a 1.

The largest single-precision positive number that can be represented is $2^{15}-1$, or 32,767 (a sign bit of 0, and 1's in all other bit positions). The largest negative number is -2^{15} or -32,768 (a sign bit of 1, and 0's in all bit positions). The number 0 is represented by all bits being 0; there is no negative 0.

A double-precision number of 32 bits can be used to give a number range from +2,147,483,647 to -2,147,483,648 ($2^{31}-1$ to -2^{31}). Two adjacent words must be used in storage with the high-order word at an even address, and the low-order word at the next higher odd address (Figure 3).

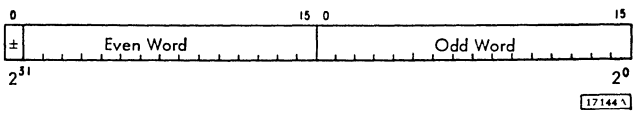


Figure 3. Double Precision Data Word

Instruction Format

The instruction defines the basic operation to be performed and contains the factors necessary for developing a core storage address. This core storage address is called the effective address (EA).

Two basic instruction formats are used: a single-word instruction (Figure 4) and a two-word instruction (Figure 5). The two-word instruction contains the full core storage address in the 16 bits of the low order word. The single-word instruction is used when it is not necessary to furnish the full core storage address, but only to modify (displace) a base address already existing in a designated 16-bit register. The displacement bits, 8 through 15, can be used to address a range of core storage locations from 127 addresses above the base address to 128 addresses below the base address.

The address portion of a two-word instruction can also be modified by adding to the contents of a designated 16-bit index register.

The bits within the instruction are used in the following manner:

Op Code: The operation to be performed by the instruction is defined by these five bits. There are 26 valid op codes.

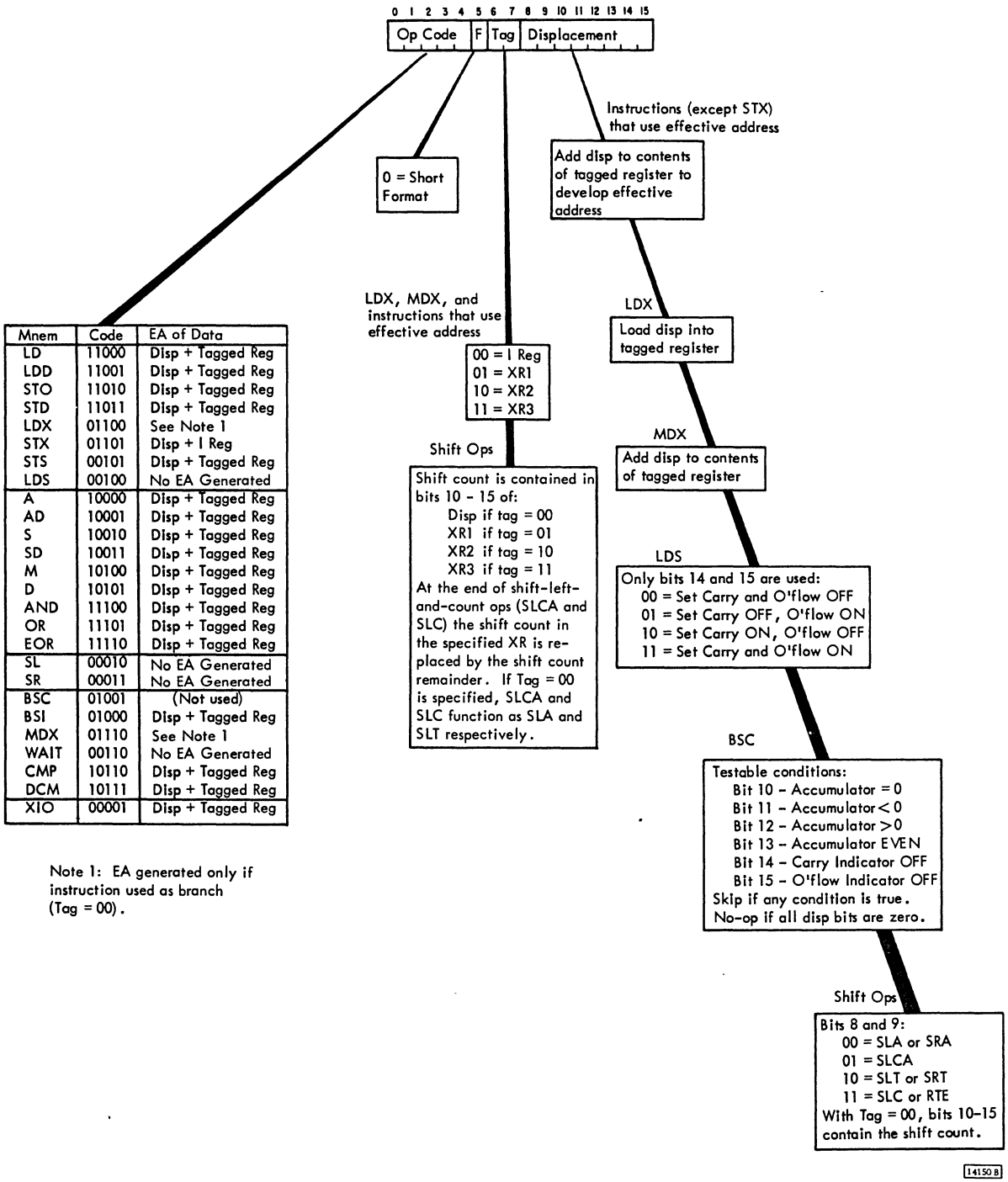
Format (F): This bit selects the instruction format. A "0" indicates a single-word instruction and a "1" indicates a two-word instruction.

Tag (T): These are the index tag bits used to select a register for address modification.

Displacement: These eight bits define the displacement value and are added to the register specified by the tag bits to develop the effective address (EA).

Displacement may be in either a positive or negative direction as determined by the sign of the displacement value. A negative displacement value will be in two's complement form with a bit in position 8.

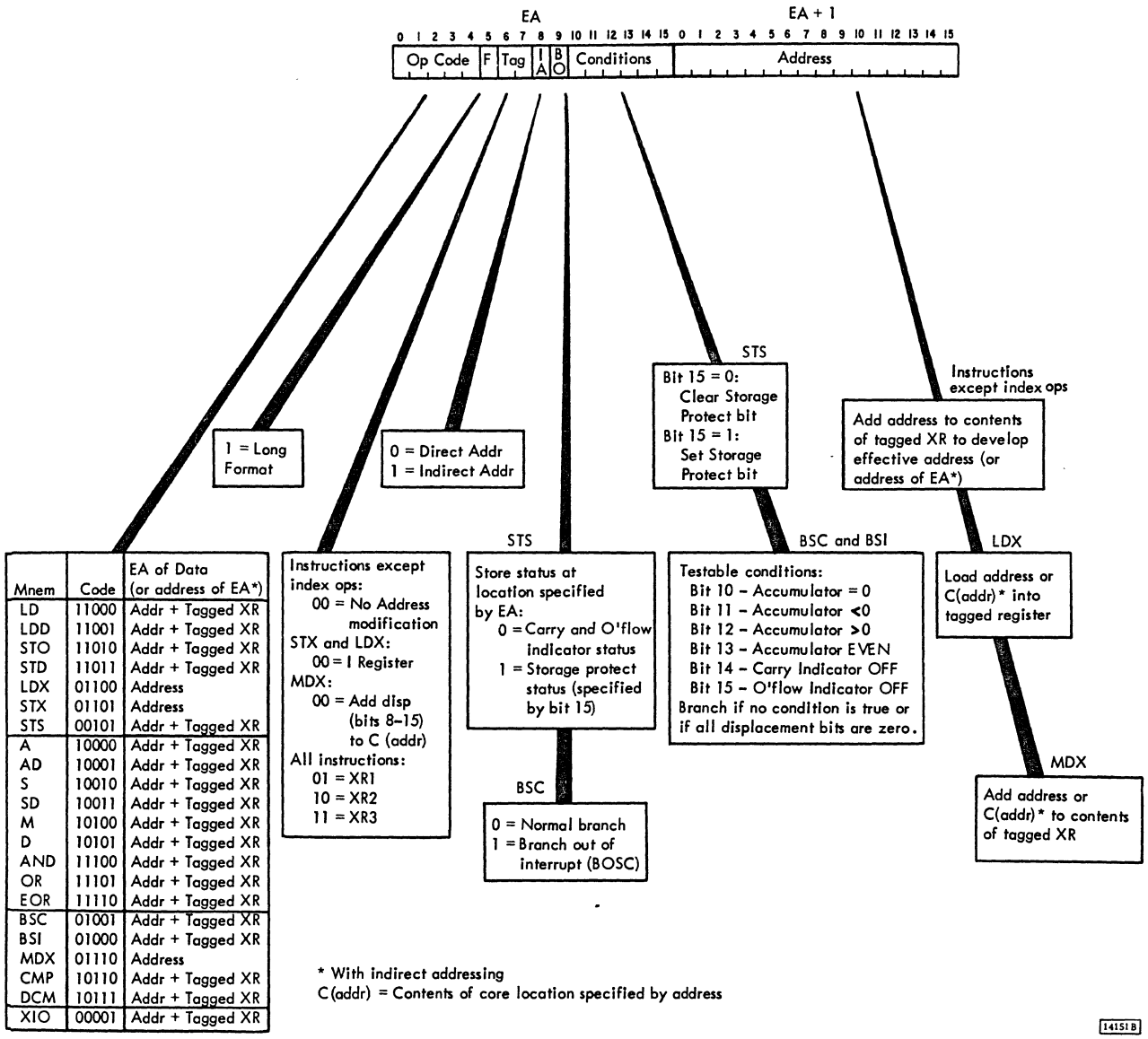
Indirect Address (IA): This is the indirect address bit in the two-word instruction format except in the modify-index-and-skip instruction with a tag 00 specified. If "0", addressing is direct. If "1", addressing is indirect.



Mnem	Code	EA of Data
LD	11000	Disp + Tagged Reg
LDD	11001	Disp + Tagged Reg
STO	11010	Disp + Tagged Reg
STD	11011	Disp + Tagged Reg
LDX	01100	See Note 1
STX	01101	Disp + I Reg
STS	00101	Disp + Tagged Reg
LDS	00100	No EA Generated
A	10000	Disp + Tagged Reg
AD	10001	Disp + Tagged Reg
S	10010	Disp + Tagged Reg
SD	10011	Disp + Tagged Reg
M	10100	Disp + Tagged Reg
D	10101	Disp + Tagged Reg
AND	11100	Disp + Tagged Reg
OR	11101	Disp + Tagged Reg
EOR	11110	Disp + Tagged Reg
SL	00010	No EA Generated
SR	00011	No EA Generated
BSC	01001	(Not used)
BSI	01000	Disp + Tagged Reg
MDX	01110	See Note 1
WAIT	00110	No EA Generated
CMP	10110	Disp + Tagged Reg
DCM	10111	Disp + Tagged Reg
XIO	00001	Disp + Tagged Reg

Note 1: EA generated only if instruction used as branch (Tag = 00).

Figure 4. Single-Word Instruction Format



Mnem	Code	EA of Data (or address of EA*)
LD	11000	Addr + Tagged XR
LDD	11001	Addr + Tagged XR
STO	11010	Addr + Tagged XR
STD	11011	Addr + Tagged XR
LDX	01100	Address
STX	01101	Address
STS	00101	Addr + Tagged XR
A	10000	Addr + Tagged XR
AD	10001	Addr + Tagged XR
S	10010	Addr + Tagged XR
SD	10011	Addr + Tagged XR
M	10100	Addr + Tagged XR
D	10101	Addr + Tagged XR
AND	11100	Addr + Tagged XR
OR	11101	Addr + Tagged XR
EOR	11110	Addr + Tagged XR
BSC	01001	Addr + Tagged XR
BSI	01000	Addr + Tagged XR
MDX	01110	Address
CMP	10110	Addr + Tagged XR
DCM	10111	Addr + Tagged XR
XIO	00001	Addr + Tagged XR

Figure 5. Double-Word Instruction Format

Branch Out (BO): This bit is used to specify that the branch-or-skip-on-condition instruction is to be interpreted as "branch-out-of-interrupt routine."

Conditions: These six bits specify the indicators to be tested on a branch-or-skip-on-condition instruction.

Address: These 16 bits usually specify a core storage address in a two-word instruction. The address can be modified by the contents of an index register or used as an indirect address if the IA bit is on.

Instruction Set

The 1800 instruction set is shown in Figure 6. Each instruction falls into one of five classes. Note that the instructions which may be modified with indirect addressing are indicated in the indirect addressing column. Some instructions perform multiple uses as specified by their control bits.

ADDRESSING

Indirect Addressing

Indirect addressing is used only in double-word instructions (F=1). The direct address can be generally defined as the

Class	Instruction	Indirect Addressing	Mnemonic
Load and Store	Load Accumulator	Yes	LD
	Double Load	Yes	LDD
	Store Accumulator	Yes	STO
	Double Store	Yes	STD
	Load Index	**	LDX
	Store Index	Yes	STX
	Load Status	No	LDS
	Store Status	Yes	STS
Arithmetic	Add	Yes	A
	Double Add	Yes	AD
	Subtract	Yes	S
	Double Subtract	Yes	SD
	Multiply	Yes	M
	Divide	Yes	D
	And	Yes	AND
	Or	Yes	OR
	Exclusive Or	Yes	EOR
Shift	Shift Left Instructions		
	Shift Left Logical (A) *	No	SLA
	Shift Left Logical (AQ)*	No	SLT
	Shift Left and Count (AQ)*	No	SLC
	Shift Left and Count (A)*	No	SLCA
	Shift Right Instructions		
	Shift Right Logical (A)*	No	SRA
	Shift Right Arithmetically (AQ)*	No	SRT
	Rotate Right (AQ)*	No	RTE
Branch	Branch and Store I	Yes	BSI
	Branch or Skip on Condition	Yes	BSC(BOSC)
	Modify Index and Skip	**	MDX
	Wait	No	WAIT
	Compare	Yes	CMP
	Double Compare	Yes	DCM
I/O	Execute I/O	Yes	XIO

* Letters in parentheses indicate registers involved in shift operations.
** See the section for the individual instruction (MDX and LDX)

17151 D

Figure 6. Instruction Set

location of data in core storage. An indirect address can then be defined as the address of a direct address. For most instructions, the effective address that is generated during I1 and I2 cycles is a direct address.

However, the presence of a "1" in the bit-8 position of a long format instruction indicates that the effective address is really an indirect address. This indirect address is the core storage location of a direct address.

Only one level of indirect addressing is available in the 1800 system. This means that the indirect address of an instruction always selects a direct address, never another indirect address.

Indirect addressing requires an additional I cycle, called the IA cycle. The IA cycle reads the direct address from the core storage location specified by the indirect address and places the direct address in the accumulator.

Indexing

Indexing enables the use of one instruction to operate on data stored in various core storage locations without altering the instruction word itself. When specified by the instruction word tag bits, the contents of the specified index register are added to the instruction address during the instruction cycle. Therefore, at the beginning of the execute cycle, the effective address that is in the accumulator has been modified by the index register.

There are instructions that load, store, and modify any of the three index registers.

REGISTERS

Index Registers (XR)

There are three 16-position index registers. They are used to index an instruction causing the contents of the specified index register to be added to the instruction address to form the desired effective address for that instruction.

Machine Registers

There are seven basic machine registers which are used by the CPU to provide the results specified by the program.

A (Accumulator Register): The accumulator is a 16-position register with unique connections that enable arithmetic and shift operations. It is used to store one factor of an arithmetic or logical operation; the D register contains the other factor. The result of any arithmetic operation is contained in the accumulator. The contents can be shifted to the right or left.

The accumulator can be loaded from core storage by a load accumulator instruction. This operation is executed to set up a data word to be shifted.

An XIO instruction with a sense command can load the accumulator with a sense word from an I/O adapter. The program can then analyze the sense word by a shift operation.

The accumulator contents can be stored into core storage by a store accumulator instruction.

B (Storage Buffer Register): The B register is a 16-position register. It is used to buffer all instruction and data words read from or written into core storage.

D (Arithmetic Factor Register): The D register is a 16-position register. It is used to store one factor for arithmetic and logical operations; the other factor is in the accumulator (A register). The D register and the accumulator have unique interconnections that implement arithmetic and logical operations.

I (Instruction Address Register): This 16-position register is a counter to maintain the address of the next instruction. The contents are transferred to the M register to address core storage. The contents of the I register are then increased by one for the next sequential address. The contents are transferred to the accumulator for effective address generation during each one-word instruction cycle.

M (Storage Address Register): This 16-position register is used to address core storage. It is loaded from the I register or the accumulator. The output of position 15 is forced on during double precision instructions or for fetching an Input Output Control Command (IOCC).

Q (Accumulator Extension Register): This 16-position register is used as an extension of the accumulator for arithmetic operations.

U (Temporary Accumulator Register): This 16-position register is used for temporary storage of the contents of the accumulator. It does not contain the ability to perform arithmetic operations. It is used to store the contents of the accumulator while the accumulator is being used by another operation such as generating an effective address.

Control Registers

Op Code (Operation Code Register): This five-position register decodes the operation code and controls the gating of information from the B register to other registers.

F (Format Register): This one-position register defines the operation as a one or two word instruction.

Tag Register: This two-position register specifies if one of the three index registers is to be used during this instruction.

SC (Shift Counting): This six-position counter is loaded at the beginning of every cycle to control the number of cycles to be taken. It is loaded at the beginning of a shift instruction to control the number of positions to be shifted. It is decremented each execute cycle and when the shift count = 0 the operation is ended.

C/OF (Carry and Overflow Registers): This two-bit register is set to indicate either a carry or overflow condition of the accumulator.

Modifier Registers

IA (Indirect Addressing Register): This one-position register specifies (if a "1") and controls indirect addressing for this instruction.

BO (Branch Out Register): This one-position register controls the branch-or-skip-on-condition instruction to cause it to be interpreted as a "branch-out-of-interrupt routine".

BASIC PROCESSOR-CONTROLLER DATA FLOW

The first machine cycle of an operation or after a reset is an instruction cycle. The purpose of the first instruction cycle of any operation is to analyze the instruction word to determine the operation to be performed and to set up the registers that control the operation. These control registers are loaded with the contents of the B register during the first half of the cycle (Figure 7).

The control registers include the operation register, the format and tag registers, the shift counter, and the modifier register. A decode of the operation code activates the lines that gate information from the B register to other registers. The format register defines the operation as a one word or two word instruction. The tag register specifies one of the three index registers or the I register to be used during this instruction.

The shift counter is a dual-purpose register. For most instructions, it is loaded by hardware means, rather than from the B register, to indicate the number of cycles necessary for the specified operation. For shift operations, it is loaded from the B register or from an index register to control the number of shifts to be performed. It is decremented with each cycle or with each shift to accomplish its function.

The modifier register (bit 8-IA and bit 9-BO) is used by some operations to specify various functions to be performed by one op code.

Being a stored-program system, the 1800 system must execute instructions, stored in core storage, in a prescribed sequence. A register must be provided to keep track of the address of the next instruction to be performed. This register is the instruction register (I register). At the beginning of each instruction cycle, when an instruction word must be read from core storage, the contents of the I register are transferred to the M register. Immediately after I is transferred to M, the I register is incremented one address, so that it always contains the address of the next instruction to be performed.

If the address that is to be used to address core storage, the effective address, is to be generated during one I cycle, it is generated by adding part of the instruction word contained in the B register to the contents of the I register, or to the contents of one of the three index registers. An adder of some sort is therefore required. All additions are made to the accumulator. An additional register is required to contain the other factor of an add operation. This arithmetic factor register is called the D register.

Unique circuit connections and controls between the D register and the accumulator enable add and subtract operations.

To generate an effective address in one I cycle for a short format instruction, the CPU must be able to transfer the contents of the I register or one of the index registers to the accumulator. The other factor of the addition is a part of the instruction word contained in the B register, therefore,

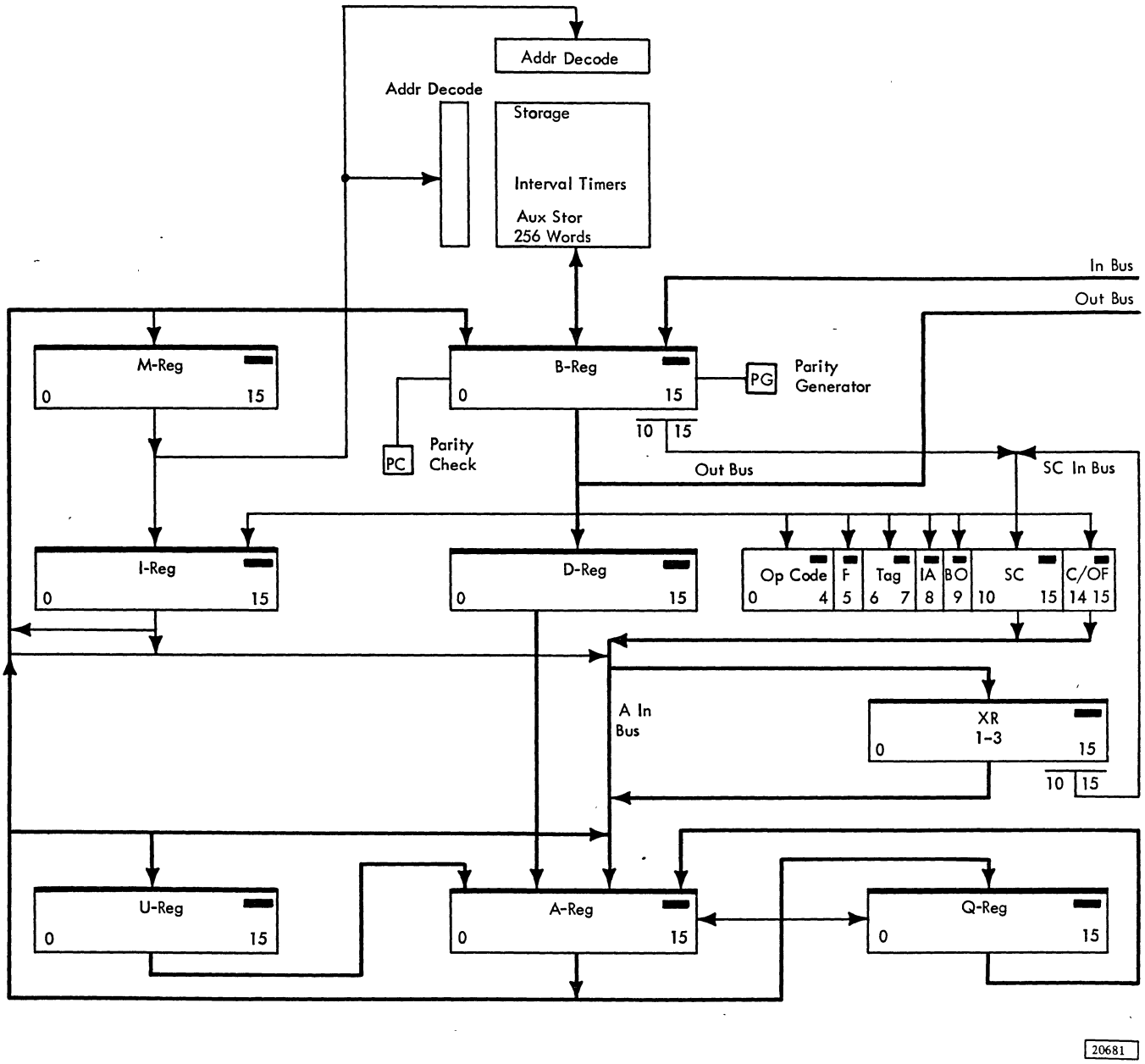


Figure 7. Processor–Controller Data Flow

the D register is located between the B register and the accumulator. The contents of the D register are then added to the contents of the accumulator and the result (effective address) remains in the accumulator at the end of the I cycle.

At the beginning of the cycle which uses this effective address, the contents of the accumulator are transferred to the M register to address core storage.

Some instructions require that more than 16 bits be operated upon during the E cycles of one instruction. Therefore, another 16–bit register is connected to the accumulator. This register is called the accumulator extension register or Q register. Binary bits in the accumulator can be shifted from the low order position of the accumulator into the Q register, or the entire 16–bit word can be transferred from the accumulator to the Q register, or from the Q register to the accumulator.

The objectives of some operations are to modify a data word that has been previously loaded into the accumulator. Because the accumulator is used to generate an effective address during the I cycle, a temporary storage is needed for the accumulator word. This temporary storage register is

called the U register. Sixteen-bit words can be transferred from the accumulator to the U register, and from the U register to the accumulator.

The basic data flow for internal CPU operations consists of the 16 data bits that are sensed in core storage and set into the B register and into the Op, format, tag, and modifier registers during the instruction cycle. The contents of these registers determine what will happen during succeeding cycles.

During execution cycles, data is manipulated between the B, D, A, Q, and U registers and then written into a predetermined core storage location, or left in the accumulator.

The next instruction, specified by the I register, is addressed by the M register and read from core storage and the program continues.

Some instructions require only one I cycle to perform the complete operation. For example, the load status instruction sets the condition of the carry and overflow indicators according to the information contained in two positions of the B register. The second half of the I cycle merely gates positions 14 and 15 of the B register into the carry and overflow indicators and the operation is complete.

Other instructions require an instruction cycle followed by an execution cycle. For example, the load accumulator instruction generates an effective address during the I cycle and reads a data word from core storage and places that word in the 16-bit accumulator during the E cycle.

MACHINE CYCLES

Clock

There are two clocks furnishing all timings in the 1800 system. Only one clock is running at any time. The two clocks are; the T clock which furnishes all timings to control CPU operations and direct program controlled I/O operations, and the X clock which controls the data channel operations.

The clocks generate timing pulses T0, T1, T2, through T7 or X0, X1, X2, etc., depending on which clock is running. The timing pulses are grouped into machine cycles. One machine cycle is from T0 through T7 or X0 through X7. The time for one machine cycle is 2, 2.25, or 4 μsec depending on the 1800 configuration.

When certain arithmetic and shift operations require more steps than one cycle provides, the clock is stepped to T7 and then clock advances are prevented, extending T7 while the phase flip-flop output provides timing pulses for the operation. Advancement from T7 requires the absence of any of the clock extending conditions.

Channel Timing Pulses

The clock timing pulses T0 through T7 or X0 through X7 are ANDed together to generate three basic timing pulses which are sent to the I/O adapters via the I/O channel interface. The three timing pulses are; timing pulse A, timing pulse B, and timing pulse C. The three timing pulses, A, B, and C can be combined in the I/O adapter to generate all eight timing pulses.

I (Instruction Cycles)

In the performance of stored program instruction operations, the computer proceeds through instruction time (I-cycles), and generally through execution time (E cycles) for each operation. The functions of instruction time are to read the instruction from core storage, store the instruction in the control registers, decode the registers to set up the necessary controls for the operation, and to develop an effective address.

Six types of instructions and the machine cycles required for each type are:

	Cycles Required		
Type of Instruction	I1	I2	IA
Single-Word	X		
Single-Word with Indexing	X		
Double-Word	X	X	
Double-Word with Indexing	X	X	
Double-Word with Indirect Addressing	X	X	X
Double-Word with Indexing and Indirect Addressing	X	X	X

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I1 (Instruction Cycle)

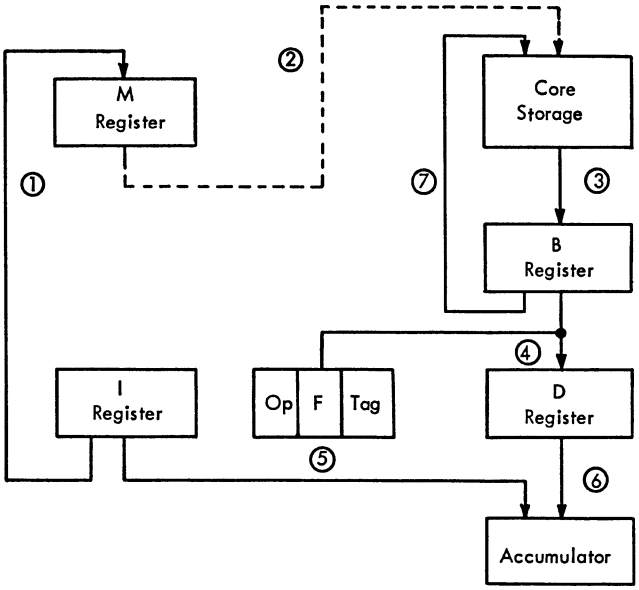
This cycle is used by all instructions. It reads the instruction data from core storage at the address specified by the instruction (I) address register. The core storage word is read into the B register, distributed to the various control registers, and decoded to indicate the operation to be performed.

There are four types of I1 cycles. Each type performs specific functions to generate or help generate the effective address. The four types of I1 cycles and their functions are shown in Figures 8, 9, 10, and 11.

I2 (Instruction Cycle)

This cycle is used by all long format instructions. It is used to read the second word of the instruction and load it into the accumulator (Figure 12). The second word in a long format instruction is the effective address unless it is modified by indexing or indirect addressing. The I register contents, loaded into the accumulator during the I1 cycle, are not used.

If the instruction specifies an index register, the contents of that index register were loaded into the accumulator during the I1 cycle. The I2 cycle then reads the address word from core storage and adds it to the index register contents in the accumulator.



1. Transfer instruction address from I to M.
2. Address core storage from M register.
3. Read instruction word from core storage; load into B register.
4. Load operation, format, and tag registers with B register bits 0-7. Load D register with B register bits 8-15. Extend displacement sign (bit 8) in D register.
5. Transfer I register to Accumulator.
6. Add D register to Accumulator. Effective address is now in Accumulator.
7. Write-back instruction word into core storage.

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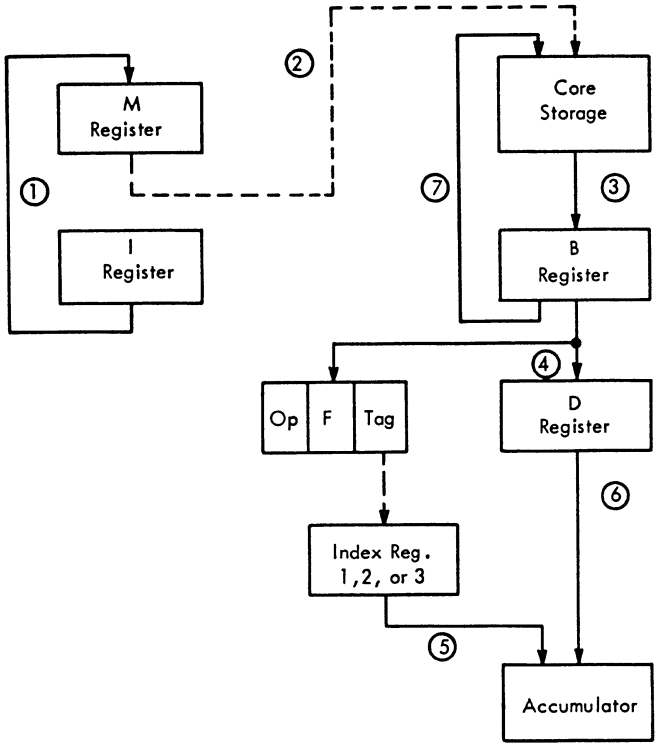
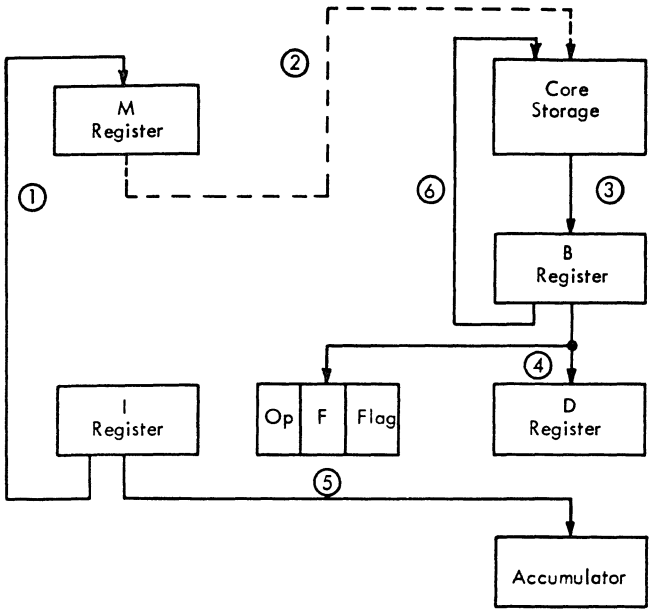
Figure 8. I1 Cycle, Single Word, Without Indexing



1. Transfer instruction address from I to M.
2. Address core storage from M register.
3. Read instruction word from core storage; load into B register.
4. Load operation, format, and tag registers with B register bits 0-7. Load D register with B register bits 8-15. Extend displacement sign (bit 8) in D register.
5. Transfer Index register, selected by Tag bits, to Accumulator.
6. Add D register to Accumulator. Effective address is now in Accumulator.
7. Write-back instruction word into core storage.

24245

Figure 9. I1 Cycle, Single Word, With Indexing

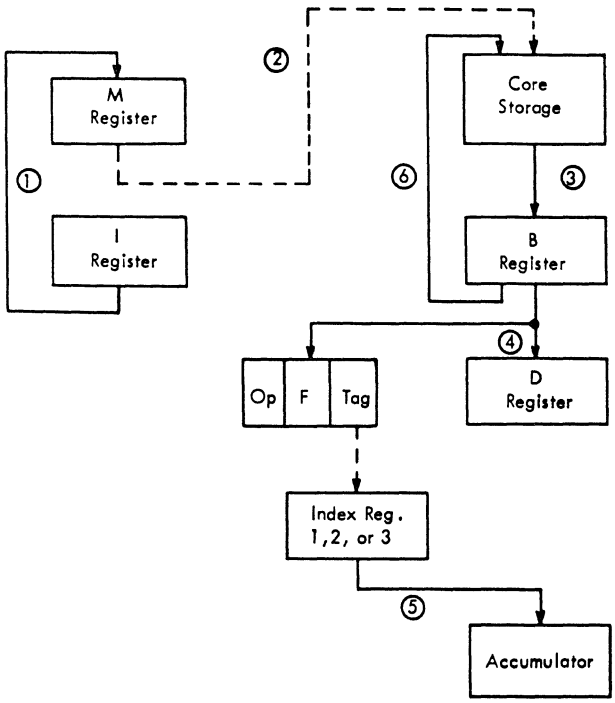


1. Transfer instruction address from I to M.
2. Address core storage from M register.
3. Read instruction word from core storage; load into B register.
4. Load operation, format, and tag registers with B register bits 0-7. Load D register with B register bits 8-15. Extend displacement sign (bit 8) in D register.
5. Transfer I register to Accumulator.
6. Write-back instruction word into core storage.

D register and Accumulator Contents will not be used. I2 cycle will read address word from core storage and place it in the Accumulator.

24246

Figure 10. I1 Cycle, Double Word, Without Indexing

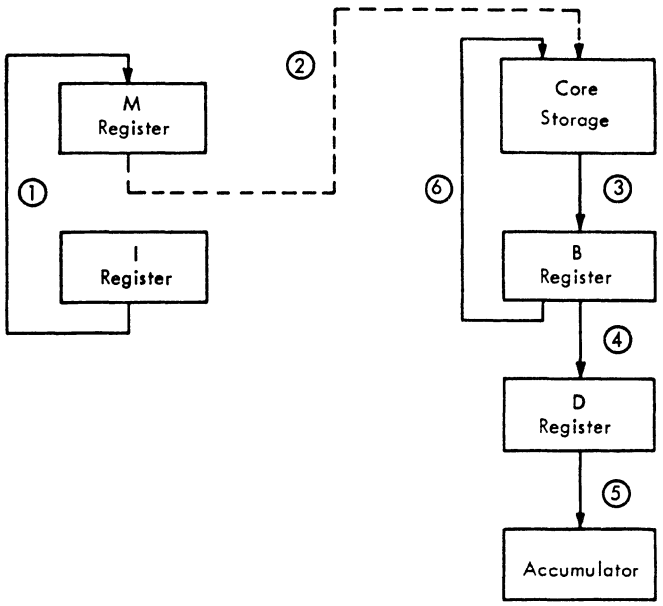


1. Transfer instruction address from I to M.
2. Address core storage from M register.
3. Read instruction word from core storage; load into B register.
4. Load operation, format, and tag registers with B register bits 0-7. Load D register with B register bits 8-15. Extend displacement sign (bit 8) in D register.
5. Transfer Index register, selected by Tag bits, to Accumulator.
6. Write-back instruction word into core storage.

D register contents will not be used. I2 cycle will read the address word into the D register and add it to the index word in the accumulator.

24247

Figure 11. I1 Cycle, Double Word, With Indexing



1. Transfer address-word address from I to M.
2. Address core storage from M register.
3. Read address word from core storage; load into B register.
4. Transfer B to D.
5. Transfer D (address word) to Accumulator.
6. Write-back address word into core storage.

24248

Figure 12. I2 Cycle, Double Word, Without Indexing

IA (Indirect Addressing Cycle)

This cycle is used only by double word instructions. A direct address can be generally defined as the location of data in core storage. An indirect address can then be defined as the address of a direct address. For most instructions, the effective address that is generated during I1 and I2 cycles is a direct address.

However, the presence of a "one" in the bit 8 position of the instruction indicates that the effective address is really an "indirect" address.

This "indirect" address is the core storage location of a "direct" address.

The preceding I2 cycle loaded the indirect address into the accumulator. This indirect address may be the address word (Figure 11) or the address word plus the contents of an index register (Figure 12). The IA cycle loads the indirect address into the M register, reads the direct address from the core storage location specified by M, and transfers the direct address to the accumulator via B and D registers (Figure 13).

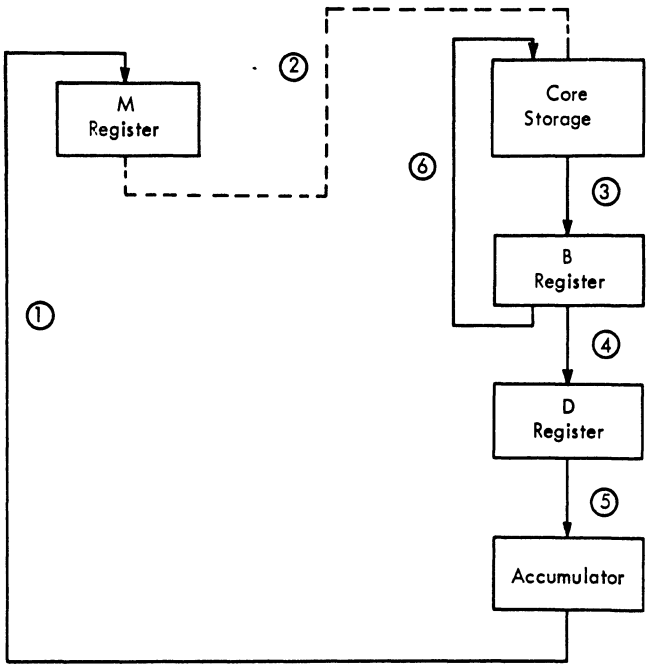
Only one level of indirect addressing is available in the 1800 system. This means that the indirect address of an instruction always selects a direct address, never another indirect address.

E (Execution Cycle)

The performance of a computer operation is normally divided into two parts, instruction time (I cycles) and execution time (E cycles).

Each execution time is preceded by its associated instruction time during which the instruction is read from core storage and interpreted.

The function of execution time is to accomplish the objectives of the particular operation specified by the instruction. The required number of machine cycles depends upon the specific operation to be performed (Figure 14).



1. Transfer indirect address, loaded into accumulator during I2 cycle, to M register.
2. Address core storage from M register.
3. Read direct address from core storage; load into B register.
4. Transfer B to D.
5. Transfer D to A.
6. Write-back direct address into core storage.

24249

Figure 13. IA Cycle

The following instructions are complete at the end of their instruction time and require no execution cycles.

1. Wait.
2. Shift right/left.
3. Load status.
4. Branch or skip on condition.
5. Load index if no index register is specified.

OP	CYCLE					
	I1	I2	IA	E1	E2	E3
WAIT	X	-	-	-	-	-
XIO	X	/	/	X	X	/
SLA	X	-	-	-	-	-
SRA	X	-	-	-	-	-
LDS	X	-	-	-	-	-
STS	X	/	/	X	-	-
BSI	X	/	/	X	-	-
BSC	X	/	/	-	-	-
LDX	X	/	/	-	-	-
STX	X	/	/	X	-	-
MDX	X	/	/	/	/	-
A	X	/	/	X	-	-
AD	X	/	/	X	X	-
S	X	/	/	X	-	-
SD	X	/	/	X	X	-
M	X	/	/	X	-	-
D	X	/	/	X	X	-
CMP	X	/	/	X	-	-
DCM	X	/	/	X	X	-
LD	X	/	/	X	-	-
LDD	X	/	/	X	X	-
STO	X	/	/	X	-	-
STD	X	/	/	X	X	-
AND	X	/	/	X	-	-
OR	X	/	/	X	-	-
EOR	X	/	/	X	-	-

X Cycle is used.
- Cycle is not used.
/ Cycle may or may not be used.

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Figure 14. Instruction Usage of I and E Cycles

When the execution time for an operation is complete, the computer is directed to enter the instruction time for the next instruction in sequence.

E1, E2, and E3 (Execution Cycles)

The functions of individual E-cycles are described as they are used to accomplish the objectives of the various operations. However, each has normal functions and objectives. These normal functions and objectives are performed each E-cycle except during the cycles that they are specifically blocked. These normal functions objectives are:

T0: Transfer the effective address that was generated during I-cycles from the accumulator to the M register and read core storage. Load core storage word into B register.

T1:

1. Transfer the contents of the temporary accumulator storage register (U) to the accumulator (A). (The contents of A are placed in U at the beginning of instruction time, and are returned to A at the beginning of the first E cycle of an instruction.)
2. Decrement the shift counter. The shift counter is set during instruction time for the number of cycles required to complete the operation.

T2: Transfer B to D.

T3: Set arith ctrl and add flip-flops if required.

T4:

1. Store the contents of B back into the core storage location specified by M.
2. Depending upon the operation code; transfer, compare, or add D to the contents of the accumulator, or, store or shift the contents of the accumulator.

T5, T6, T7:

1. Continue the compare, shift, or add operation if required.
2. Extend T7 time if required (if add or subtract and $D \neq 0$, or if shift and shift counter $\neq 0$).

The sequential advance from one numbered E-cycle to another is controlled by operation code gating.

XIO Control and XIO Data Cycles

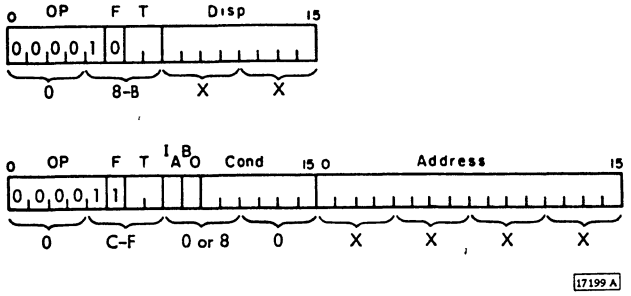
Execution of the XIO instruction consists of control and data cycles. The first E cycle (E1) is designated the XIO control cycle. All I/O commands require a control cycle to transfer the IOCC control word to the I/O adapters.

The second E cycle (E2) is designated the XIO data cycle except for read or write command when the third E cycle (E3) is designated the XIO data cycle. Control, sense interrupt, and sense device commands transfer control or sense data on the second E cycle (E2) designated the XIO data cycle. Read and write commands use the second E cycle (E2) to read the IOCC address word from core storage and load it into the accumulator to address core storage for the data word. The third E cycle (E3) of the read and write commands transfers the data word and is therefore the XIO data cycle.

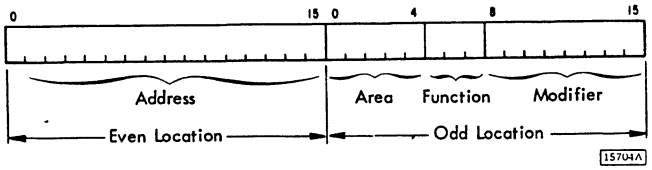
The initialize read and initialize write commands read the IOCC address word from core storage and load it into the channel address register (CAR) during the second E cycle (E2) designated the XIO data cycle. Data is transferred during cycle-steal cycles for these two commands.

EXECUTE I/O (XIO)

This instruction is used for all I/O operations; it may be either one or two words in length, as specified by the F-bit. In the two-word instruction, the address is either a direct or indirect address, as specified by the IA bit. For proper operation, the effective address (EA) must be an even address. The effective address is used to select a two-word I/O control command (IOCC) from storage.



I/O Control Commands



The I/O control command (IOCC) consists of an address word at EA and a control word at EA + 1. The control word, consisting of the area, function, and modifier, is placed on the out bus first during the E-1 cycle. The area, function, and modifier bits are decoded at each I/O device to set up the necessary controls for the operation.

Address

The address word is read from core storage during the E-2 cycle.

The meaning of this 16-bit field is dependent upon the function of the I/O control command and the device adapter. Some examples are:

1. If the function is initialize write (101) or initialize read (110), the address specifies the starting address of a table in storage (an I/O block). This table contains data words and control information. Initialize write and initialize read functions are used only with data channel control.
2. If the function is control (100), and the area specifies a disk storage device, the address indicates the number of tracks the access must be moved.
3. If the function is sense device (111) or sense interrupt (011), the address field is ignored. Instead, an increment of time, equivalent to a core storage cycle, is taken during which the selected I/O device or interrupt level places its status code into the P-C accumulator.
4. If the function is write (001) or read (010), the address specifies the core storage location of the data word. These functions are used only with direct program control. The basic differences between a direct program control operation and a data channel operation are shown in Figure 15.

Cycle	Direct Program Control	Data Channel
E1	Transfer Control Word to I/O Adapter	Same
E2	Address word to Accumulator	Address word to Channel Address Register (CAR). Terminate Op.
E3	Transfer data word to or from I/O Adapter using M register address. Op complete. Interrupt to I/O subroutine for subsequent data word transfers	None
Cycle Steal	None	Transfer data word to or from I/O Adapter using CAR address. Take C.S. cycles when needed for subsequent data word transfers.

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Figure 15. Direct Program Control and Data Channel Operations

Area

This five-bit field specifies the device to be used in the I/O operation. In some cases, the area specifies a group of devices (magnetic tape units, printers, etc.), and the modifier field then designates the specific device.

Function

The following eight basic I/O functions can be specified by the three-bit function code.

Code	Function
000--	CE Mode This command places the selected device in the CE mode if modifier bit 15 is a one; it removes the device from the CE mode if bit 15 is a zero. The CE mode indicates, through the DSW, that the device is being checked by one of the diagnostic features.

Code	Function
	The CE mode also causes the device to interrupt on the CE-interrupt level (lowest priority) rather than on the assigned level.
001--	Write This code is used to transfer a single word from core storage to an I/O unit. The address of the core storage location is provided by the address field of the I/O control command.
010--	Read This code is used to transfer a single word from an I/O unit to core storage. The address of the core storage location is provided by the address field of the I/O control command.
011--	Sense Interrupt This code directs the I/O devices requesting interrupt recognition on the interrupt level specified by the modifier field of the I/O control command to make their interrupt status available.
100--	Control This code causes the selected device to interpret the modifier or address field as a specific control action.
101--	Initialize Write This code initiates a write operation on a device or unit which will subsequently make data transfers from core storage via a data channel.
110--	Initialize Read This code initiates a read operation from a device or unit which will subsequently make data transfers to core storage via a data channel.
111--	Sense Device This code directs the selected device to make its current indicator status available for automatic placement into the P-C accumulator.

Modifier

This field is used to extend or qualify the meaning of the area or function codes.

XIO Instruction Execution

I Cycle: Loads the accumulator with the effective address (see I cycle description). An XIO effective address (EA) must be an even address.

E1 Cycle: Transfers EA to the M register and activates the output of M_{15} bit flip-flop. This causes the core storage location at EA + 1 (odd address) to be selected. The word at this location, which is the control word of the I/O control command, is loaded into the B register. The control word contains the area, function, and modifier bits. This word is placed on the out-bus to be analyzed by the I/O adapter.

E2 Cycle: The address word at EA is loaded into the B register, placed on the out-bus and loaded into the channel address register (CAR) associated with the data channel to be used. A CAR check is made at this point to check for proper loading of CAR. The XIO operation is then terminated.

Direct Program Controlled Operation

There are two types of I/O device controls. They are direct program control and data channel (cycle steal) control. Direct program control is initiated by an execute I/O control command (IOCC) function of control, sense interrupt, sense device, read or write.

Each data transfer or control operation requires an individual XIO instruction.

I/O devices operating under direct program control in the 1800 system include:

1816 Printer Keyboard	Console Bit Switches
1053 Printer	Analog Input
1627 Plotter	Digital Input
1054 Paper Tape Reader	Analog and Data Output
1055 Paper Tape Punch	

Read/Write Function

When the function specified is a read or write, the address word provides the storage address, from or to which data will be transferred. At the conclusion of the storage cycle for data transfer, the XIO instruction is terminated and the next sequential instruction is executed.

E1 Control Cycle: Transfers EA to the M register and forces on the M_{15} bit. This causes the core storage location at EA + 1 (odd address) to be selected. The word at this location is loaded into the B register. This word (EA + 1) is the control word for the I/O control command; it contains the area, function, and modifier bits. It is placed on the out bus to be analyzed by the I/O adapters.

E2 Cycle: Loads the accumulator with the address word portion of the IOCC (located at EA).

E3 Data Cycle: Transfers the address word from the accumulator (loaded during E2 Cycle) to the M register. Using this M register address, the data word is transferred to or from the I/O adapter via the out or in bus.

Normally, transmission of several words is required to complete the data or message transfer. This is accomplished by allowing the P-C to respond to an interrupt request from the device when the device cycle has been completed and a subsequent data word is required. At an appropriate time, the P-C acknowledges the interrupt, identifies the request with a particular device, and by another XIO instruction, transmits the next sequential word of the message as specified by the IOCC.

It is the responsibility of the program subroutine answering the device interrupt request to modify the address word of the IOCC, provide table look-up to translate to the device character set if required, and maintain a program word count to indicate the end of message if necessary. At the completion of each interrupt subroutine sequence, the program must exit from the subroutine, utilizing a branch or skip on condition instruction with B9 = 1 (BOSC) which branches out of the interrupt program to the mainline program. This is necessary to restore the interrupt logic so that future interrupt requests at the same or lower interrupt levels can be acknowledged.

Control Function

With a specified function of control, the modifier field specifies to the device, the particular control operation to be executed. Examples of such control operations are start pulse-output timer, feed card, load interrupt mask register.

I Cycle: Same as read/write function.

E1 Control Cycle: Same as read/write. Set up area, function, and modifier decode circuits in I/O adapter. Some I/O adapters use this cycle to perform a particular control function.

E2 Data Cycle: Certain I/O adapters interpret the address word at EA to determine the particular function and initiate that function during this cycle. For other I/O adapters, this may be a dummy cycle.

E3 Cycle: Not used with a control function.

Sense Interrupt

This command transfers the active interrupt level status word (ILSW) to the P-C accumulator. The ILSW represents the status of the interrupts assigned to the specified level. The P-C program analyzes the ILSW to determine the area or device requesting the interrupt. Modifier bits 10 through 15 are placed on the out bus by the interrupt circuits during the sense ILSW instruction.

I-Cycle: Same as other functions.

E1 Control Cycle: Same as other functions.

E2 Data Cycle: The interrupt level status word, placed on the in-bus by the I/O adapter is loaded into the B register, then transferred to the accumulator.

E3 Cycle: Not used with the sense interrupt function.

Sense Device

After the device causing an interrupt has been identified from data in the interrupt level status word (ILSW), it is necessary to determine the indicator(s) within the particular device causing the interrupt. This is accomplished by issuing a subsequent XIO sense device command with an area assignment corresponding to that of the device being interrogated.

Modifier bit 15 = 1 causes the status indicators associated with that particular device to be reset after the information has been gated onto the in-bus. The information gated onto the bus and loaded into the accumulator in this instance is referred to as the device status word (DSW). The DSW contains one bit of information for each indicator within the device.

It is possible for a device to contain many conditions which may cause an interrupt on the same interrupt level. When this condition exists, it is usual that each of the interrupt conditions is logically ORed and then gated to a particular bit of the in-bus. The identification of the interrupting condition within the device is accomplished by sensing the device status word and then analyzing it with the shift left and count instructions or a shift left and BSC combination.

I Cycle: Same as for other XIO functions.

E1 Control Cycle: Same as for other XIO functions.

E2 Data Cycle: The device status word, placed on the in bus by the device adapter, is loaded into the B register, then transferred to the accumulator.

E3 Cycle: Not used with the sense device command.

Interrupt

Some condition, external to the mainline program, causes an automatic branch to a subroutine that results in correcting or servicing the condition.

Interrupts are grouped into priorities, 12 levels of which are standard and 12 additional levels, in groups of six.

Interrupt levels can be masked and unmasked by the program.

When an interrupt condition exists, and the bus lines can transfer the request, the assigned interrupt level is activated in a priority circuit. When the present program instruction is completed, the highest priority interrupt level that is active initiates a branch to an interrupt subroutine.

This branch is implemented by a hardware-generated branch-and-store instruction-register (BSI) instruction. This forced BSI contains a hardware-generated indirect address that specifies a position of a table of direct address. The instruction register, containing the location of the next instruction in the main line program, is stored at the core

storage location specified by the direct address (EA) and the branch is executed to EA +1. EA + 1 is the location of the first instruction in the subroutine that services the interrupting device.

At the completion of the sequence of interrupt service subroutines, an indirect-address branch is executed with the indirect address being EA. Because EA contains the instruction register contents that were stored during the BSI, the effective address of this branch is the next instruction in the main line program. In addition to the 24 customer interrupt levels, three levels are used for internal or CE functions.

1. Internal (check) interrupt is sub-zero level (highest priority) and is initiated by an invalid op code, a parity check, a CAR check, or a storage protect violation.
2. Trace level is a lower level priority than any customer assigned level. It causes a branch prior to each program instruction.
3. CE interrupt level enables the initiation of an interrupt by the CE interrupt key on the console.

The interrupt function provides an automatic branch in the normal program sequence based upon an external condition. Examples of conditions which would normally be utilized to cause interrupts follow:

1. The internal timer has concluded the recording of a preset time interval.
2. The magnetic tape unit has completed a required data transfer and signals the P-C with a scan complete.
3. An undefined operation code has been detected during the P-C instruction readout and therefore cannot be executed (internal level).
4. The device operating on direct program control has completed the transfer of the previous character and requests a subsequent character.
5. An external process condition has been detected which requires an immediate change in the program execution.

As shown in Figure 16 a maximum of 24 external interrupt levels are available. Twelve external interrupt levels are standard, as are the internal, trace, and CE interrupt levels. Note that the priority level of each interrupt, as well as its unique core storage address, is listed in decimal form. Note also that all but the trace and CE interrupts have an interrupt level status word (ILSW). The ILSW, which is explained in detail later, is used to identify the specific condition causing its interrupt level to request service. No external interrupt can occur at the end of an XIO or BSI instruction (until another instruction is taken).

The internal interrupt cannot be masked. However, an XIO or BSI instruction prevents the internal interrupt for one instruction. Its ILSW is reset when it is sensed to determine the interrupting condition. The four error conditions are assigned to the ILSW as follows:

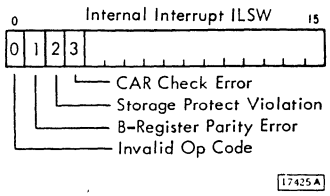
Interrupt	Priority Level	Core Storage Location		ILSW	
		Decimal	Hex		
Internal	1	8	8	Yes	Basic
Trace	26	9	9	No	
** CE	27	10	A	No	
*External 0	2	11	B	Yes	
1	3	12	C	Yes	
2	4	13	D	Yes	
3	5	14	E	Yes	
4	6	15	F	Yes	
5	7	16	10	Yes	
6	8	17	11	Yes	
7	9	18	12	Yes	
8	10	19	13	Yes	
9	11	20	14	Yes	
10	12	21	15	Yes	
11	13	22	16	Yes	
12	14	23	17	Yes	Special Feature Group 1
13	15	24	18	Yes	
14	16	25	19	Yes	
15	17	26	1A	Yes	
16	18	27	1B	Yes	
17	19	28	1C	Yes	
18	20	29	1D	Yes	Special Feature Group 2
19	21	30	1E	Yes	
20	22	31	1F	Yes	
21	23	32	20	Yes	
22	24	33	21	Yes	
23	25	34	22	Yes	

* External interrupt cannot occur at the end of an XIO or BSI instruction.

** A CE interrupt stores the return link in core storage location /000A and starts execution at core storage location /0001. Interrupts are prevented in the same manner as for the standard forced BSI.

17424C

Figure 16. Interrupt Levels



Interrupt Level Masking

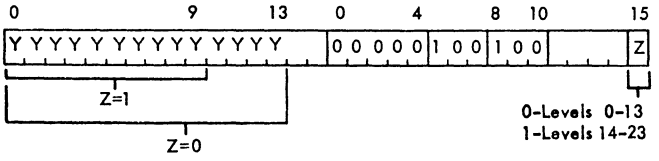
A mask register exists for the masking and unmasking of external interrupt levels. An interrupt level that is masked cannot initiate a request for service until it has been unmasked.

Programmed interrupts will not occur if the corresponding interrupt is masked prior to the time the XIO command for programmed interrupt is executed.

Device status words (DSW) and process interrupt status words (PISW) are not affected by the mask operation.

The XIO control command is used to simultaneously mask and unmask external interrupt levels 0–13 or 14–23, depending on modifier bit 15 of the IOCC. Two XIO control commands are required to mask/unmask the maximum of 24 external interrupts. (All external interrupts are automatically masked when electrical power is first applied to the P-C.) The execution of this instruction does not affect the contents of the accumulator.

The IOCC for the mask instruction is shown below:



Note that the area is 00000 and that modifier bits 8–10 must be 100.

The status of address bit positions 0–13 or 0–9, depending on modifier bit 15 (Z), determine whether external interrupt levels 0–13 or 14–23 are masked or unmasked:

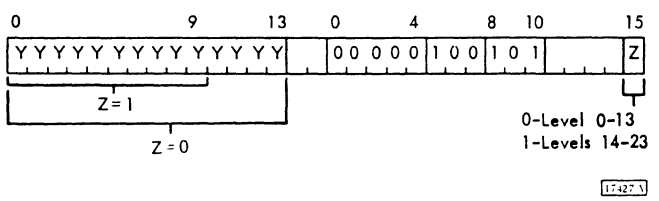
A 1-bit masks the corresponding interrupt level.
A 0-bit unmasks the corresponding interrupt level.

External Interrupt Polling

Two polling cycles are required to sample all 24 interrupt level requests. Interrupt levels 0 through 13 are polled, as a group, on one cycle, and interrupt levels 14 through 23 are polled, as a group, on another cycle. The group that is polled on any given cycle is not readily predictable because the first group polled after an interrupt will be the group that was being polled when the interrupt occurred. Therefore, unmasking an interrupt level for one instruction, that takes only one core-storage cycle (MDX, LDX, LDS, etc.), would not poll all 24 interrupt level requests. This one core-storage cycle instruction would poll only one group, and the group could be either 0–13 or 14–23.

Programmed Interrupts

External interrupt levels can be programmed. An XIO control command is used to turn on individual external interrupt levels within either of two groups 0–13 or 14–23, depending on the status of modifier bit position 15 of the IOCC. Two instructions must be executed to turn on interrupt levels in both of these groups. The IOCC is shown below:



Note that the area is 00000 and that modifier bits 8–10 must be 101.

The status of address bits 0–9 or 0–13, depending on modifier bit 15 (Z), determine whether individual interrupts within priority levels 0–13 and 14–23 will be turned on:

A 1-bit turns on the corresponding external interrupt level.
A 0-bit does not turn on the corresponding external interrupt level.

Programmed interrupts will not occur if the corresponding interrupt level is masked prior to the time the XIO command is executed.

If a programmed interrupt level is turned on but the hardware forced BSI instruction has not occured, an XIO instruction to mask or unmask any interrupt level will turn the programmed interrupt level off. Another programmed-interrupt XIO instruction would be needed to reinitiate the programmed interrupt after the specified interrupt level is unmasked.

Status Words

The I/O devices of the 1800 system and some of the system features contain "status" indicators. The on/off condition of each status indicator reveals to the operating program an operational status or condition of the device in which the indicator is located. Status indicators are also contained in the process being monitored and/or controlled by the 1800 system. These indicators, both system and process oriented, project their individual conditions into the system via the in-bus. Those process and system indicators assigned to interrupt levels initiate interrupt requests when they are turned on.

An XIO sense device command, which specifies a particular device, is used to read into the accumulator the on/off condition of each indicator located in the specified device. Once the indicators of the specified device are read into the accumulator, the contents of the accumulator are considered a device status word (DSW) or a process interrupt status word (PISW), depending on whether the device is located within the system or in the process. The content of the accumulator is considered a DSW when the bits represent the status of indicators from a system device. The content of the accumulator is considered a PISW when the bits represent the status of the process interrupts.

DSW Indicators: DSW indicators usually fall into three general categories:

1. Error or exception interrupt conditions.
2. Normal data or service required interrupts.
3. Routine status conditions.

All DSW's are shown in the Appendix.

When the DSW indicators are read into the accumulator by an XIO sense device command, bit position 15 of the IOCC referenced by the XIO sense device command determines whether the indicators are reset when their status is read into the accumulator. If a bit is present in position 15 of the IOCC, the indicators are reset.

Interrupt Level Status Word

The interrupt facility includes one 16-position interrupt level status word (ILSW) for each interrupt level. (The Trace and CE interrupts are exceptions; they are unique interrupts and require no ILSW.) Like the PISW and the DSW, the ILSW is not actually a word until it is read into the accumulator. Prior to its entry into the accumulator, an ILSW is simply 16 signal lines, each of which has OR'ed to it indicators from a status word (PISW or DSW).

Each interrupt level requests service when any one of the 16 bits in its ILSW is turned on. When the P-C program recognizes the interrupt request, it executes an XIO sense interrupt command to read the ILSW of the requesting interrupt level into the accumulator. The P-C program then determines which bit position in the ILSW caused the interrupt. This bit position identifies the DSW or PISW that has the interrupt initiating indicator. The DSW or PISW is then analyzed by the P-C program to determine which indicator in the DSW or PISW caused the interrupt.

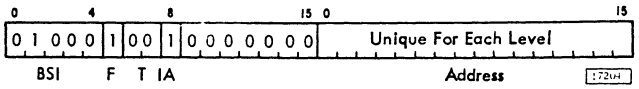
The programmer does not specify the ILSW in the XIO sense interrupt command used to read the ILSW into the accumulator. This specification is fixed; that is, each ILSW is hardware assigned to its interrupt level. The sense interrupt operation provides the ILSW of the highest priority level requesting service. Except for the P-C internal interrupts, none of the DSW and/or PISW interrupt indicators ORed into ILSW bit positions are reset when the ILSW is read into the accumulator. The indicators are not reset until their respective DSW or PISW is read into the accumulator with an XIO sense device command.

Programmed Operations

In general, an interrupt request is recognized at the completion of the instruction being executed when the interrupt request occurs. Exceptions to this practically instantaneous recognition occur when:

1. The instruction being executed when the interrupt request occurs is either an interrupt forced or normal branch and store instruction register (BSI) instruction or an XIO instruction. These instructions effectively mask all interrupts during their execution and the execution of the next instruction.
2. The interrupt request level is masked. The request will be retained by the device — not the 1800 — for recognition when the interrupt level is unmasked. (Programmed interrupts are not retained if masked prior to their execution.)
3. The interrupt request is of the same or a lower priority level than an interrupt level being serviced.

When an interrupt request is recognized, the P-C inhibits the normal access to core storage and generates into the B-register a BSI, indirect-address, instruction. The format of this forced hardware instruction is:



Data Channel Controlled Operation (Cycle Stealing)

The data channels (Figure 17) provide for the control of the I/O channel for the higher speed I/O devices on the system. They consist of priority controls, channel address registers and buffers, and cycle-steal controls.

Fifteen data channels are available, three standard and twelve optional. (For a simplified diagram see Appendix.)

Data channels control information transfer to or from core storage by a method called "cycle stealing". Cycle stealing means blocking P-C operations for one or more machine cycles to transfer data between core storage and an I/O device.

One word of data is transferred during each machine cycle (cycle-steal cycle). Processor controller operations are delayed one cycle for each cycle-steal cycle taken.

Other than delay, cycle-steal cycles do not affect P-C operation. A data channel may effect data transfer (cycle-steal cycle) after any T clock cycle or during extended T7 time.

Data channel operation is initiated by the execution of an XIO instruction which references an I/O control command (IOCC) having a function of initialize write or initialize read. Once started, the I/O adapter has the responsibility for controlling the quantity and destination of all data transmitted between core storage and the attached I/O device. Because of the independent operation of the data channel, blocks of data can be transferred between core storage and an I/O device while program instructions are being performed.

Since the P-C and data channels share core storage, the execution of the main-line program is automatically suspended for a minimum of one cycle each time the data channel is activated by a cycle-steal request from the I/O adapter.

The operation of the data channel does not interfere with data contained in the internal P-C registers since each data channel contains its own storage address register. Word count of the data words transferred is maintained in the I/O adapter.

A maximum of 15 data channels are available with the 1800 system. The data channel controls include a priority system to prevent multiple data channels from accessing core storage simultaneously. The priority of a device is

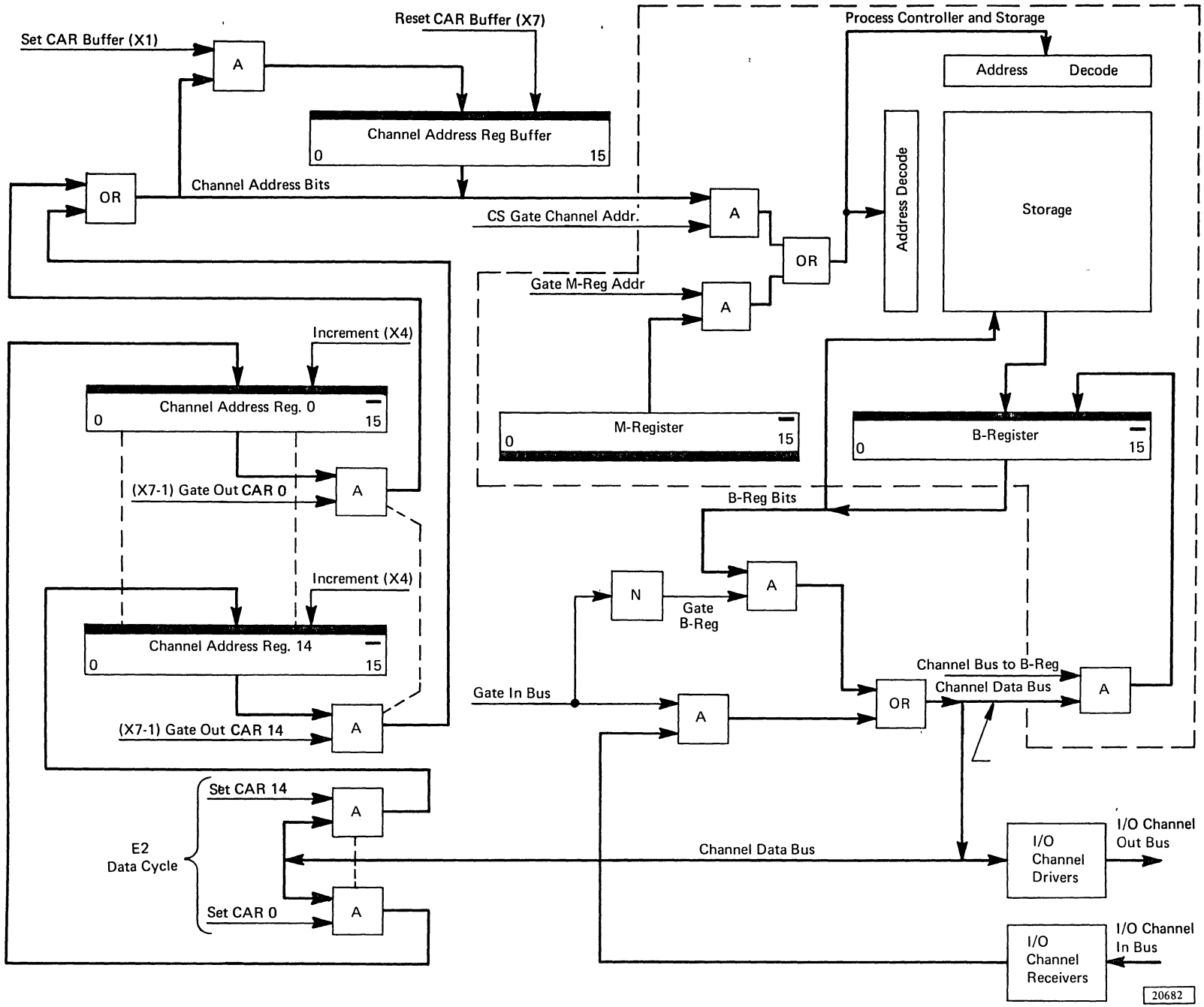
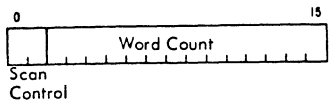


Figure 17. Data Channel Storage Addressing

assigned by the user, by assigning each data channel using device to the data channel with the desired priority.

After data channel operations are initialized with an XIO instruction, the first cycle-steal data word transfer reads the word count and scan control bits from core storage and transfers this information to the word count register (WCR) and the scan control register (SCR) in the device adapter. The word count and scan control bits are contained in a single 16-bit word (Figure 18).



Bit 0	Bit 1	
0	0	Single scan and stop with an interrupt at the end of the data table.
0	1	Single scan and stop with no interrupt.
1	0	Continuous scan (chaining) with an interrupt at the end of this data table.
1	1	Continuous scan (chaining) with no interrupt.

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Figure 18. Data Channel Word Count Format

The ability to chain in a continuous scan of the same or several different tables is a function of the individual device. A device need not have the chaining function in order to interrupt at the conclusion of the data transmission in the table.

The device requests references to core storage at a rate depending upon its requirements and independently of program execution. The data channel in response to the request, utilizes the next available core storage cycle and sends, via the I/O channel, the contents of the addressed location. During this cycle the address is incremented and the word count (if required) in the device adapter is decremented by one.

The above sequence continues until the data channel makes the last core-storage reference of the current message. This last reference is sensed by the word count becoming zero during the cycle or through some indicator in the device. If the device does not have chaining ability, no more requests for core storage reference are made until the device is reinitialized.

For a device with chaining ability, another request is made if a continuous scan is indicated by the scan control register. The data which comes from storage is the address of the next message. This address may be the starting address of the same data table or that of a new data table. Instead of incrementing the address, the data from core storage is loaded into the channel address register.

The chaining control then requests the first word of the new message. This word must be the address of its own core storage location. This address is compared with the contents of the specified channel address register. If they are not equal, a CAR check is indicated. The chaining control requests a third cycle-steal cycle to read out the second word of the data table. This word contains a word count and two bits for scan control. The word count is loaded into the word count register and the two bit control field is stored in the scan control register for use at the end of the data table. If the word count as read from storage is zero, the operation is terminated immediately.

The length of time between data transfer cycles on a chaining operation is a maximum of three P–C cycles on a device connected to cycle steal priority zero. (This is either 6, 6.75, or 12 μsec depending upon cycle speed.) It may be greater than this for devices of lower cycle steal priorities.

Priority Controls

Data channels have fixed cycle-steal priority levels to prevent multiple data channels from addressing core storage simultaneously. Cycle-steal level 0 is the highest in priority and level 14 is the lowest in priority.

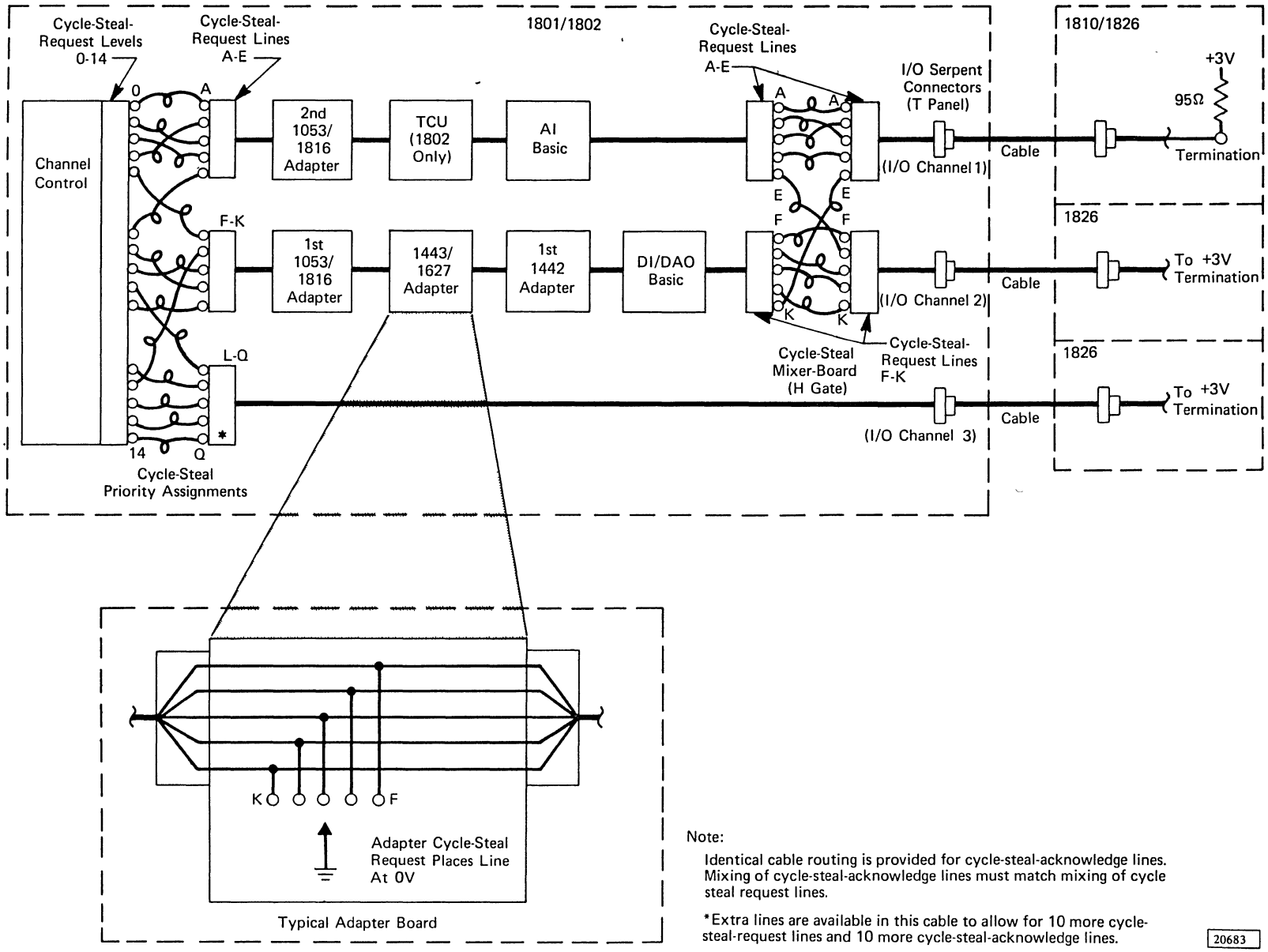
When an I/O device requires a cycle-steal cycle, the device activates its cycle-steal request line. The cycle-steal request line sets the associated cycle-steal priority flip-flop in the data channel to initiate the cycle-steal cycle. The following functions are performed by the priority circuits during a cycle-steal cycle:

1. Channel address register (CAR) is gated to channel address buffer (CAB) and core storage by time pulses 7, 0, and 1 of the cycle steal (X) clock.
2. CAR is set into CAB at X1 time to maintain core storage addressing.
3. CAR is incremented at X4 time.

The cycle-steal request line (Figure 19) is activated by the I/O device, indicating that the device requires a data transfer. At the fall of T6 or X6 time, the priority flip-flop is set. If a device of a higher priority is also requesting service, the active line for the lower level request(s) is inhibited. The active level is returned to the requesting I/O device, via the wired logic as the cycle-steal acknowledge signal to indicate that the next machine cycle is the data word transfer requested by the device.

Scan Control

A scan control register is provided in each device that has chaining ability. Scan control bits must be stored in the first word of the first data table (bit positions 0 and 1) and in the second word (bit positions 0 and 1) of the second data



Note:

Identical cable routing is provided for cycle-steal-acknowledge lines. Mixing of cycle-steal-acknowledge lines must match mixing of cycle steal request lines.

*Extra lines are available in this cable to allow for 10 more cycle-steal-request lines and 10 more cycle-steal-acknowledge lines.

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Figure 19. Cycle-Steal Example (1801/1802 With Data Channel Expander – 15 Data Channels)

table and all subsequent data tables in a chain. The following is a list of the devices that have a scan control register.

I/O Device
2401/2402
Digital or pulse counter input
Digital-analog output
Analog input

The scan control register controls the I/O device and the data channel operation at the end of the data table as follows:

Bit 0	Bit 1	
0	0	Single scan of data table and stop with an interrupt.
0	1	Single scan of data table and stop (no interrupt).
1	0	Continuous scan of this data table or a different data table with an interrupt at the end of this table.
1	1	Continuous scan of this data table or a different data table with no interrupt.

Operational Sequence

The numbered steps that follow correlate with the circled numbers in Figures 20 and 21. These steps apply to either non-chaining devices or the first data table of a chaining device.

1. XIO references the IOCC word.
2. The area code and modifier select the I/O device. Function specifies the type of operation (initialize read or initialize write, etc.).

3a. The address portion of the IOCC word is stored in CAR for the selected data channel (I/O device).

b. CAR check made between selected CAR and B-register.

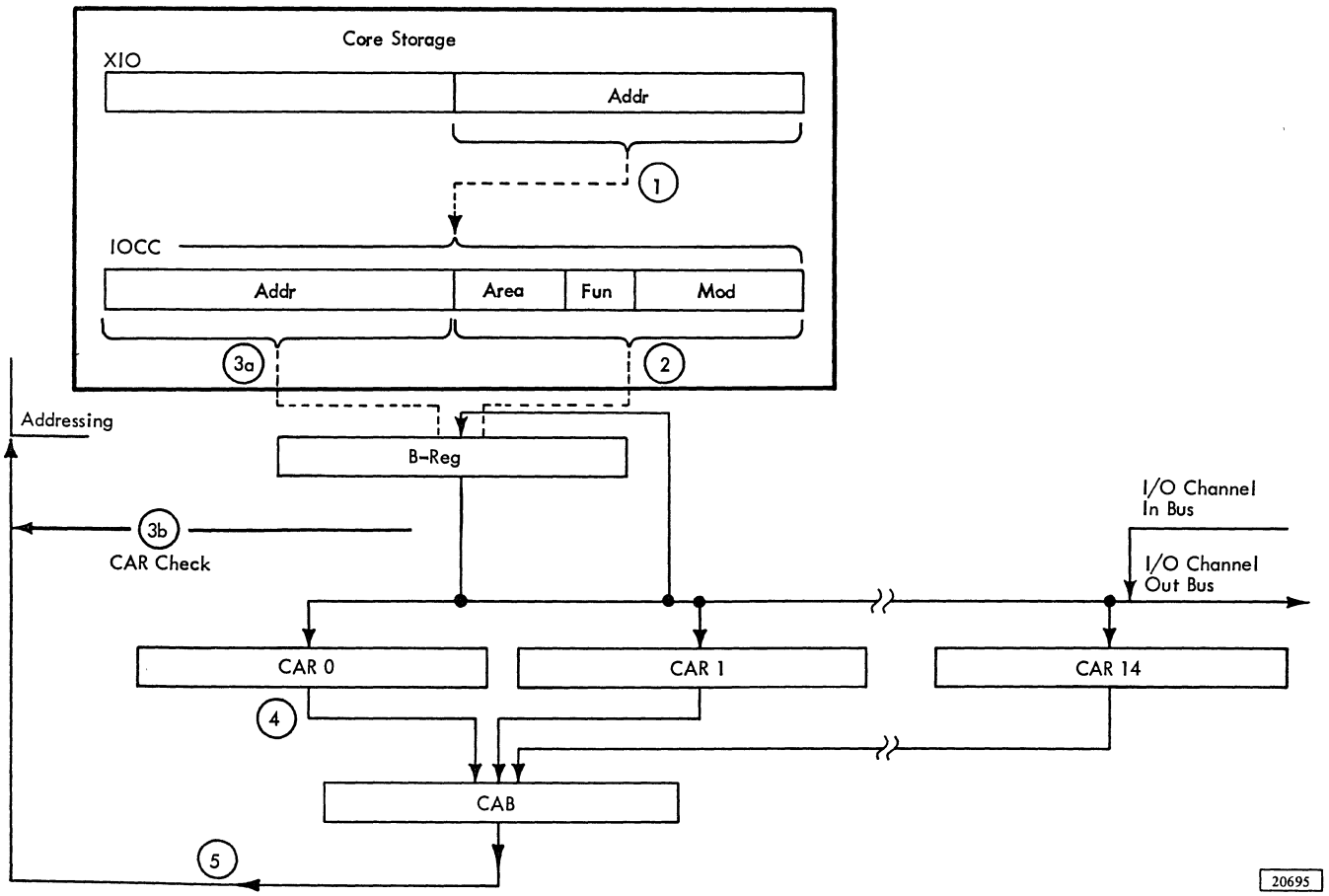


Figure 20. Data Channel Operation

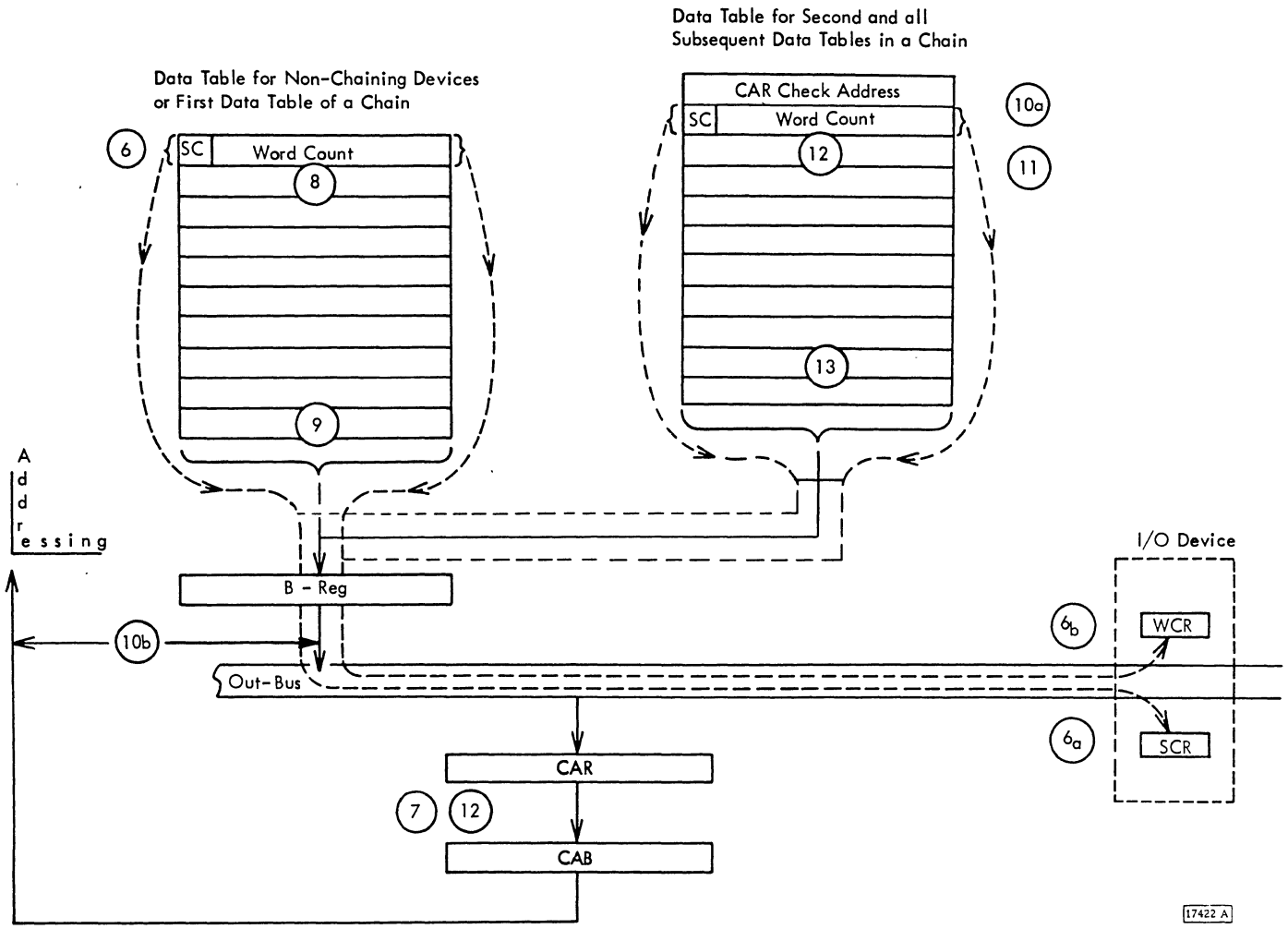


Figure 21. Data Channel Chaining

4. Cycle steal requested by I/O device. CAR addresses core storage during X0, X1, and X2 time.
5. CAR is transferred to CAB. CAB addresses core storage while CAR is incremented.
6. The first word of the data table contains
   a. Scan control bits (bit positions 0 and 1)
   b. Word count (bit positions 2–15)
   These are transferred to their respective registers in the I/O device. This is the end of the first cycle-steal cycle.
7. When another cycle-steal request occurs, CAR, which was incremented in step 5, now transfers the next higher address to CAB. CAB then addresses core storage while CAR is being incremented.
8. The first *data* word is transferred to or from the I/O device via the B-register and data channel. The word count in the I/O device is decreased by one. This is the end of the second cycle-steal cycle.

Steps 7 and 8 now continue on a device request basis; that is, they occur as the I/O device requests data transfers. Between cycle steals, the P-C continues program operation. The CAR is incremented with each data transfer and the word count is decremented. This sequence continues until the last data word of the data table is transferred. The last word transfer is sensed by the word count reaching zero or through some indicator in the device. If the device does not have chaining ability, no more demands for data transfer are made until the device is reinitialized with another XIO instruction.

Data Chaining

When a continuous scan is indicated by the scan control register (SCR) in a device having chaining ability, the I/O device holds the request line active until the data channel has taken three cycles after the word count has reached

zero at the end of the first data table. The first cycle is used to transfer the word following the data table to the CAR. The address in this word is the address of the next table of data and is loaded into CAR. The second cycle addresses the first word of the data table and performs the CAR check. The first word of the data table must contain its own address. The third cycle addresses the second word of the data table and transfers its contents (word count and scan control) to their respective registers. The I/O device then requests additional cycles as required for data transfer. In this manner the I/O device can operate in a scatter read-write mode. This method of using the data channel in a continuous mode is called "data chaining" because the data tables are essentially connected together. The length of time between data transfer cycles on a data chaining operation is a maximum of three core-storage cycles on a device connected to the highest priority data channel. It may be greater than this for devices of lower cycle-steal priorities, depending on whether they must wait for higher priority data channels to be serviced.

Data Channel Operation (Chaining)

If the scan control register contains the bits for a continuous scan, the following numbered steps correlate to the circled numbers in Figure 21. These steps are for the second and all subsequent data tables. See the previous operational sequence for steps 1 through 8 (first data table).

9. The contents of the word following the last data word in the first data table are transferred to CAR. This word must contain the address of the next data table.

10a. When the next cycle is requested, CAR addresses core storage, then CAR is transferred to CAB. CAB addresses core storage while CAR is incremented. The contents of the first word of the next data table are transferred to the B-register. This word must contain the address of itself.

b. CAR check is performed by comparing CAB with the B-register.

Chain CAR Check: When a data table is being chained, the first word in that table must contain its own core storage address. This first word is read from core storage and compared with the contents of the channel address register. If these two addresses do not compare, a CAR check is indicated in the cycle-stealing I/O device adapter. The chain CAR check is initiated by the cycle-steal-control 0, 1, and 2 lines from the adapter.

11. When the next cycle steal is requested, CAR is transferred to CAB and CAB addresses core storage. The scan control bits and word count bits are transferred from the second word of the data table to their respective registers. CAR is incremented by one.
12. Data is transferred to the I/O device on a cycle-steal basis via the B-register and the I/O channel. CAB addresses core storage to transfer a data word to the B-register. Each time CAB addresses core storage, CAR is incremented by one. When the next cycle-steal request occurs, CAR is transferred to CAB. The word count register is decremented for each word transferred.
13. When the last data character is transferred (word count is decremented to zero), operation will continue as specified by the scan control register.

Data Table

Figure 22 is an illustration of two data tables with scan control (SC) bits to initiate chaining from the first data table to the second data table.

Cycle-Steal Cycle

Whenever an I/O unit requires core storage access, it activates a cycle-steal-request signal. The CS-level flip-flop, assigned to the level used by that I/O unit, is turned on at T7 time of any operation. The channel clock (X clock) begins advancing at the end of T7 if the P-C is in run or single-step mode and any cycle-steal level is active.

One cycle is required to complete a normal cycle-steal operation; therefore, the T clock is blocked for one cycle. (The interval-time cycle-steal operation requires two cycles.) The M register output is blocked to permit core storage addressing from the data channel. From X0 to X2 core storage is addressed directly from the CAR associated with the highest priority level requesting a cycle steal. At X1 the contents of CAR are transferred to channel address buffer (CAB) and from X2 to X7 core storage is addressed from the CAB. The channel address buffer is used so that CAR can be incremented (at X4 time) to maintain the next address to be used by that level. The output of CAR is placed directly on the address-in bus to avoid the effect of circuit delays in loading CAB.

During the first cycle-steal cycle, the address in CAR is the location of the word count. (The 1442 operation does not use a word count.) The word count is placed on the out-bus and loaded into the adapter word count register.

During subsequent cycle-steal cycles, the data word is either read from core storage at the CAR address and placed

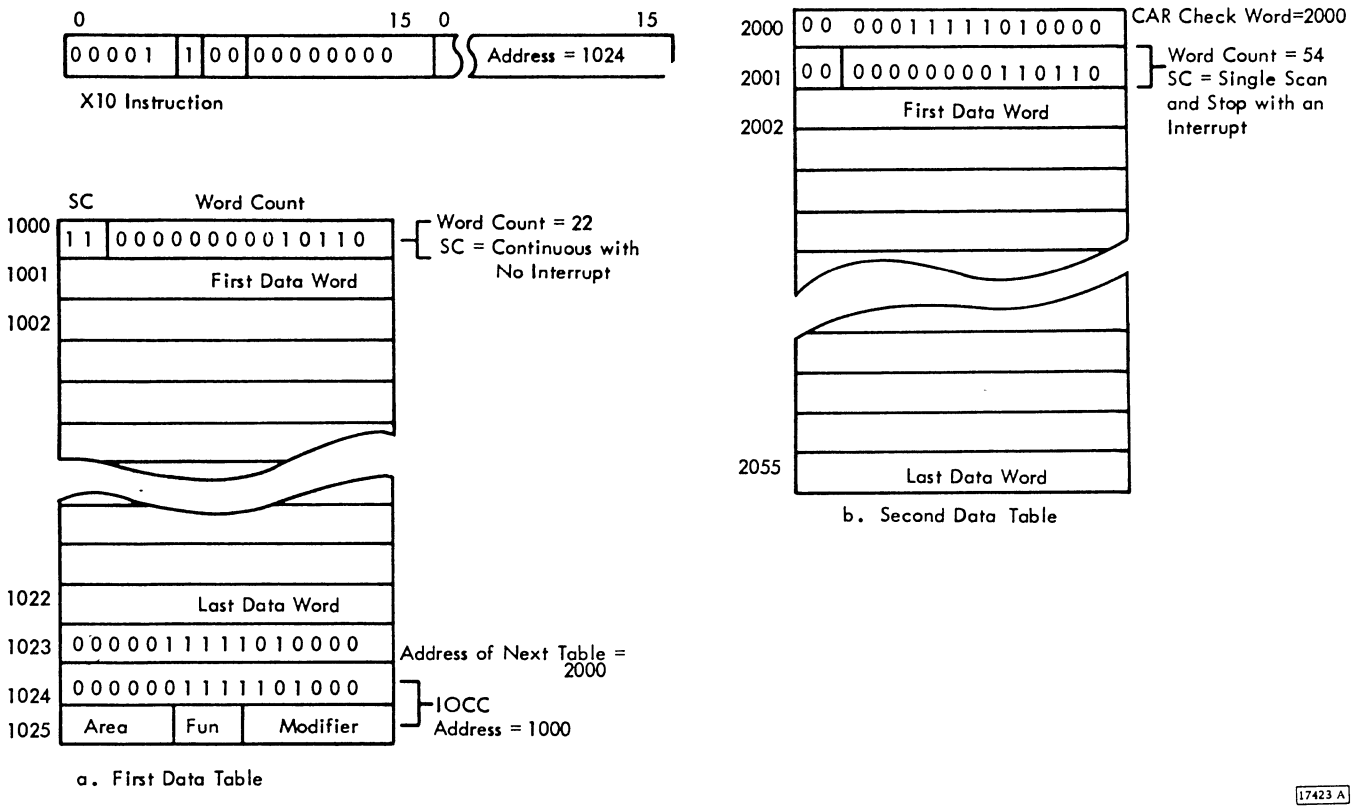


Figure 22. Data Tables for Chaining

on the out-bus (initialize-write function) or it is taken from the in-bus and stored at the CAR address (initialize-read function).

The word count register is decremented and tested for a zero condition. If the word count equals zero, an interrupt request is made to signal the end of the data table. If another cycle-steal level flip-flop is on, that level will be serviced (highest priority level first) before returning to the program operation.

The lines which control the set, increment, and reset of CAR are generated by the cycle-steal sequence controls. These lines are controlled by the I/O devices attached to the data channel. The I/O device also controls the generation of the chain CAR check. The CAR check compares the data on the channel data bus to the contents of CAB and generates a check signal if the data does not compare. The I/O device controls the action taken by controlling the cycle-steal control 0, 1, and 2 lines. Figure 23 lists these lines and their functions.

Cycle-Steal Control Levels			ANDing Conditions	Channel Control Action
0	1	2		
0	0	-	X4	Increment CAR
0	-	1	Any Cycle-Steal	Gate IN Bus (to OUT Bus)
0	1	-	T/X 3	Reset CAR
0	1	-	T/X 1234	Set CAR
-	0	1	X3	I/O to B-Reg Gate
1	0	0	X4	Increment CAR
1	1	0	CAR Check & T6	Set CAR Check FF
1	1	0	CAR Check & T/X 5	CAR Check/Parity Error to I/O
1	1	-	X4	Increment CAR

- Indicates that this bit can be 0 or 1

24243B

Figure 23. Cycle-Steal Control Lines

Environmental Conditions

Temperature and Relative Humidity Limits

Condensation must not be permitted on components of the system. The 1801/1802 will operate reliably if the ambient air conditions do not exceed the following limits:

Operating Environment - -
Temperature: 40° to 122°F* (4.4° to 50°C)
Rel. Humidity: 8% to 95%
Max. Wet Bulb: 85°F (29.4°C)

Note: The conditions shown must exist in the area before machine power is turned on.

Air Conditioning

Basic units of the 1800 system have drip and splash proof type enclosures.

Components of most units of the system are internally cooled by blower-circulated air. Dust filters are provided at each air input. Warm air exhausts from the top of each unit.

IBM recommends installation of an air conditioning system to maintain control of temperature, humidity, air contamination and for personnel comfort and optimum system performance.

Heat loads generated by the 1800 system are relatively small. Machine heat dissipation loads are given on the specification pages for each unit and in the specification summary.

To determine the air conditioning capacity necessary for a complete installation the following factors must be considered; machine heat dissipation, personnel, latent load, fresh air introduction, machine room sensible heat load, and lighting. Optimum design conditions are 75°F (24°C) and 40 to 50% relative humidity. This design provides the largest buffer, in terms of system operation, if the air conditioning fails or malfunctions. Under normal operation this design condition can be controlled within limits of ±2°F (1°C) and ±5% relative humidity with standard air-conditioning controls.

Room Pressurization

Make-up air should be brought into the air conditioning system to maintain a positive pressure within the 1800 system room. A pressure of approximately 0.1 to 0.2 inches (0,254 to 0,508 cm) of water above that of the surrounding environment is usually sufficient. The source of this air should be as free from particulate and gaseous contamination as possible. Air volume should be kept to a minimum, consistent with good engineering practice for pressurization and oxygen content.

Air Filtration

Particulate Filtration: A filter rated according to the following specifications should be installed to filter air to the computer room.

Mechanical and electrostatic air cleaners operate on two entirely different principles, therefore, it is necessary to specify a different efficiency rating for each type.

1. Mechanical Air Filter: This type must be rated at a minimum of 20% efficiency by the Bureau of Standards discoloration test using atmospheric dust. This rating applies to a clean filter and must be maintained throughout the life of the filter.
2. Electrostatic Plate Type Filter: This type must be rated at a minimum of 85 to 90% efficiency by the Bureau of Standards discoloration test using atmospheric dust.

Special filtration is necessary where installations are exposed to corrosive gases or liquids, salt air, or unusual dirt or dust conditions.

Atmospheric Contaminants

Many industrial processes increase the amount of particulate and liquid or gaseous material in the atmosphere. These materials can affect system performance by increasing wear of mechanical parts and chemical corrosion of components, thus exposing the system to excessive maintenance activity or to premature end-of-life.

These harmful elements can be reduced to levels which minimize the exposure to the 1800 system or its units by implementation of the following recommended guides:

1. *Gaseous Filtration:* When filtering is necessary to remove gases, all air handled by the air conditioning system (make-up and recirculated), should pass through a chemical control filtration system such as an activated carbon filter. The number of filter stages and the arrangement of the filters will be dictated by the conditions at a particular location and the filter media selected.

   When activated carbon filters are used, each stage should contain a minimum of 40 to 45 pounds of carbon per 1000 cfm of air handled. Special impregnation for specific gases is readily available. This impregnation significantly improves retentivity of the activated carbon filter media for the specific gases. These filters are

*105°F (41.6C) if a 2790, 1803, selector channel, communication adapter, or data channel expander are installed on the system.

readily available and their use should be considered. Proper installation and maintenance of these filters is essential. This includes the use of high efficiency particulate filters (rated at a minimum of 85% efficiency by the Bureau of Standards discoloration test using atmospheric dust) ahead of the activated carbon.

2. *Relative Humidity:* Control is essential to reduce the rate of corrosion. Relative Humidity should be limited to 50% with efforts made to control to 35%.
3. *Room Maintenance:* The area should be kept clean and free of particulate contaminants. Personnel traffic should be minimized through the area. The use of a vestibule with door closers, as an air lock, should be considered.
4. *Facility Support Maintenance:* The customer must institute an active and aggressive maintenance program, particularly with respect to filter maintenance and humidity control.

Recorders and Indicators

Temperature/relative humidity recorders, room and filter pressure manometers should be installed to permit rapid determination of the history of these parameters.

Lighting

A minimum average illumination of 40 foot-candles measured at 30 inches above the floor should be maintained in the general machine room area or at remote locations where printed material is to be used by operator personnel.

Direct sunlight should be avoided, since lower levels of illumination are necessary to observe various console and signal lights. Lighting should be sectionally controlled by switches so that the general illumination level can be reduced as desired.

Vibration

The 1800 system will be installed in many locations where it is subject to minor vibrations. Usually the intensity of vibrations in the normal control room environment is well below the allowable limits for the 1800 system.

Vibration can be either sustained (5 seconds or longer duration) or intermittent (less than 5 seconds duration). Three terms are commonly used to specify vibration intensity: frequency in cycles per second, amplitude in inches (rms, peak, or peak-to-peak), and acceleration in G's (rms or peak). The relationship between these factors is $G = 0.103\ AF^2$ where A is the displacement in inches from the mean and F is the frequency in hertz.

The maximum allowable source vibration intensities for the 1801, 1802, 1803, 1826, 1827, 1828, 1810, 1816, and 1053 as applied to the mounting structure of each unit are:

1. Sustained vibration at frequencies less than 14 Hz, 0.0035 inch rms (0.01 inch peak-to-peak).
2. Sustained vibration at frequencies of 14 Hz and higher, 0.07 G rms (0.1 G peak).
3. Intermittent vibration at frequencies less than 7 Hz, 0.035 inch rms (0.1 inch peak-to-peak).
4. Intermittent vibration at frequencies of 7 Hz and higher, 0.18 G rms (0.25 G peak).

For units not floor mounted, the customer will consider the potential translation and amplification of G forces in the mountings he provides so as to assure that these specifications are not exceeded.

The specified limits for source vibration intensity for all 1800 system units are usually not exceeded for:

1. Sustained vibrations that are perceptible, but not annoying or distracting.
2. Intermittent vibrations that are annoying or distracting, but not intolerable. When in doubt, accurate measurements should be made. This requires special instruments and the services of a professional structural engineer.

Hazardous Locations

The 1800 system is not designed for installation in hazardous locations as described in NEC 70 Article 500. Where installation in such locations is encountered it is recommended that the control room be air purged or otherwise declassified.

PRIMARY ELECTRICAL POWER REQUIREMENTS

Specifications

1801, 1802, 1827: 208/230 Vac (+10%, -8%), 60 ±1/2 Hz, three-phase four-wire (consists of three phase leads and equipment ground).

These units are available for use in countries using 50 Hz power sources with the following specifications: 195, 220, 235, 380, or 408 Vac (+10%, -8%); 50 ±1/2 Hz; 3 phase.

1053, 1816: 208/230 Vac (±10%) at 60 ±1/2 Hz, three-wire (consists of two phase leads and equipment ground) or 115 Vac (±10%) at 60 ±1/2 Hz, single-phase three-wire (consists of phase and neutral leads and equipment ground). The 1053 and 1816 are available for use in countries using 50 Hz power sources with the following specifications: 112.5, 123.5, 195, 220, or 235 Vac; ±10%; 50 ±1/2 Hz; single phase. If the 1053 and/or 1816 is in the same room as the system, it should be powered from the same source and be consistent with the system voltage.

Power Distribution (60 Hz Figure 2 -50 Hz Figure 3)

Installation of a separate isolation transformer fed from the highest primary source readily available is recommended.

The isolation transformer should have taps on both the primary and secondary sides so that power line and load variations can be compensated.

Both the isolation transformer and its feeding line should have capacity sufficient to handle initial start up current lasting approximately 10 cycles and still maintain output voltage regulation within the operation specifications.

The isolation transformer should be located as near to the system as possible. Distances of less than 100 feet are preferable.

No leads other than the control system leads should be connected to the transformer secondary. In some installations where devices containing arcing contacts and/or large inductive loads are connected to the transformer primary feeder, it may be necessary to provide additional electrical isolation through the use of the line filters or a motor alternator set. The power feeder to the system should be protected by a main line circuit breaker. Individual branch circuits should be protected by circuit breakers derated according to manufacturer's specifications. The circuit breaker panel should be located in an unobstructed well-lighted portion of the machine room; preferably near an exit door. Branch circuits should terminate within 10 feet of the 1801, 1802, and 1827, and within 6 feet of the 1816 or 1053 units. Rigid conduit or metallic shielding is recommeded for maximum isolation from electrical noise. 1053 units located outside the 1801 or 1802 area can be powered from a separate power source.

Grounding (60 Hz Figure 2 – 50 Hz Figure 3)

Each input power cord supplied with the 1800 system is equipped with a grounding type-plug. An insulated equipment grounding conductor is connected between the machine frame ground and the grounding pin of the power cord plug. Each equipment grounding conductor should be connected to a common grounding conductor at the room Power Distribution Panel through the customer's branch circuits. This common grounding conductor shall then be carried directly to the nearest stable grounding electrode.

This grounding method provides a common electrical reference plane for high-speed low-level electronic signal circuitry (both customer instrumentation and IBM system), a low impedance shunt path for high frequency electrical noise filtration provided with the 1800 system, as well as equipment safety ground.

All grounding conductors should be insulated. The grounding system should be electrically isolated from power distribution grounded neutral conductors except for such interconnections as may be required by local code and safety regulations. Conduit must not be used as the only grounding medium.

Grounding Electrode Types

Underground Cold Water Piping System: May be used when no nonmetallic couplings are used in the piping system and no electrical current flow is induced on the piping system from other equipment.

Building Steel Framing: May be used if bonded joints are used in construction. Use of building steel should be avoided if electrical current flow can be induced by other equipment.

Note: Resistance measurements should be taken to ensure electrical continuity of the grounding system.

Made Electrodes: A driven rod, 0.625" (1, 5 cm) or larger, driven into permanently moist earth to a minimum depth of 12 feet (3, 5 m) or direct burial metallic plate, grid or mesh equivalent to 16 square feet (1, 5 m^2) embedded in permanently moist earth can be used.

"Made Electrode" resistance to earth may be improved by the addition of charcoal or non-reactive salt around the electrode. A resistance to ground of less than three ohms is recommended. Supplementary or separate (where permitted) grounding electrodes should be located as far from other grounds and as close to the 1800 system as practical. A spacing of less than 50 feet from the 1800 system and at least 50 feet (15 meters) from other grounding electrodes is recommended.

All connections should be protected from corrosion. Welded construction is preferred. Any mechanical connections (bolts, etc.) should be accessible for periodic inspections.

Internal System DC Grounding

Analog Input Multiplexer/Relay inputs are isolated from dc system ground. All other signal circuits, 1800 system or external, are connected to a common dc reference point. The use of multiple grounding points on input signal wiring should be avoided as these can create voltage differences that will cause electrical noise.

Modern high-speed low-level circuits are particularly susceptible to electrical noise transients, often of microsecond or less duration, entering the system on signal lines, power lines, or grounding media. Selective filtering and decoupling methods have been employed to minimize the susceptibility of the 1800 system. Whenever filtering is done, the noise is shunted to the grounding circuit which provides a short circuit to these transients. Conductors that are effective short circuits to dc may present high impedance to high frequency electrical noise. The installation should suppress, shield, or isolate by placing on separate circuits any arcing contacts or similar devices which create such interference. Since it is rarely possible to achieve complete suppression

or isolation, the grounding system must provide minimum impedance to a stable reference plane such as moist earth. The grounding system should have sufficient isolation from electrical noise sources so that it will not be the medium for transmitting electrical noise into the system.

Phase Rotation

The three-phase power receptacle must be wired for proper phase rotation. Looking at the face of the receptacle and running counterclockwise from the grounding pin, the sequence will be phase one, phase two, and phase three.

Lightning Protection

Installation of lightning protection on the customer's power secondary is recommended if any of these conditions exist:

- Primary power is supplied by an overhead power service.
- The area is subject to electrical storms or equivalent-type power surges.
- Lightning protection is installed on the primary power service.

Lightning protection should also be installed on all signal lines that are exposed to lightning.

Signal lines that are run in grounded metal conduit or metal enclosed raceway, grounded at intermediate points, should provide sufficient protection.

Convenience Outlets

A suitable number of convenience outlets should be installed in the computer room and the CE room for use by building maintenance personnel, customer engineers, etc.

UNIT SPECIFICATIONS

Plan views illustrated use the symbols shown below.

The customer cable entry areas in the machine top are supplied with bolt-in steel cover panels. The top panel material is 0.060" (0, 15 cm) thick.

Panels are not supplied for the cable entry areas in the base of the 1801.

Figure 24 contains a summary of specifications. Figure 25 contains a summary of specifications in metric.


IBM Cable Raised Floor Cutout


Caster


Floor Leveler

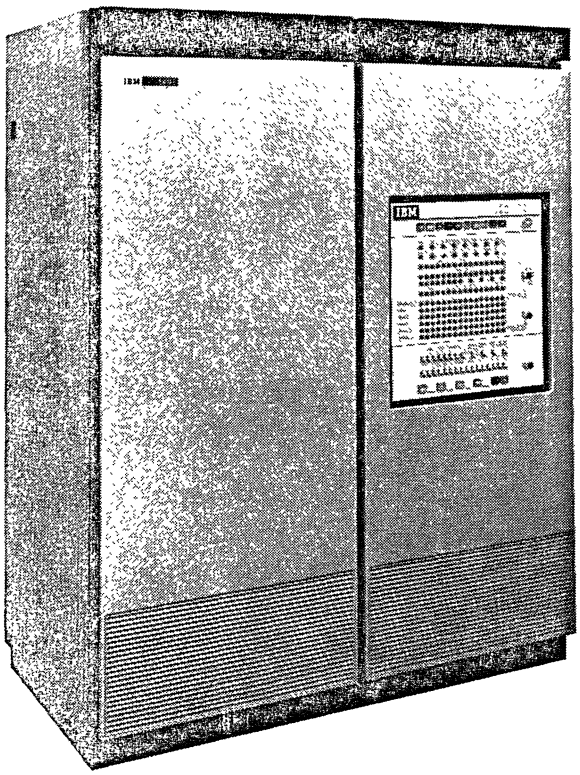

Customer Cable Entry, Machine Base


Customer Cable Entry, Machine Top


Floor Level Cable Exit


Power Cable Exit

IBM 1801 AND 1802 PROCESSOR-CONTROLLER



Dimensions--	Width (*1)	Depth (*2)	Height (*3)
Inches:	62	33	76.5
Centimeters:	157	84	194

Service Clearances--	Front	Rear	Left (*4)	Right (*4)
Inches:	36	36	30	30
Centimeters:	91	91	76	76

Maximum Weight-- 2,000 lb (907 kg)

Heat Output/hr.-- 9,500 BTU (2,394 kcal)

Air Flow-- 650 cfm (18,4 m^3/m) maximum

Electrical Requirements--

60 Hertz	50 Hertz
Phases: 3	Phases: 3
kVA: 3.0	kVA: 3.0
Plug: R & S 7328	Power Cord Style: E5
Receptacle: R & S 7324	
Connector:--R & S 7428	

Operating Environment--
Temperature: 40° to 122°F (4.4° to 50°C)
Rel. Humidity: 8% to 95%
Max. Wet Bulb: 85°F (29.4°C)

Nonoperating Environment--
Temperature: 40° to 122°F (4.4° to 50°C)
Rel. Humidity: 8% to 95%
Max. Wet Bulb: 85°F (29.4°C)

*Notes:
1. With side covers removed: 60.0" (152 cm)
2. With rear covers removed: 31.0" (79 cm)
3. 72.5" (184 cm) on shipping casters with top cover removed.
4. When not abutted to 1826 or 1828.

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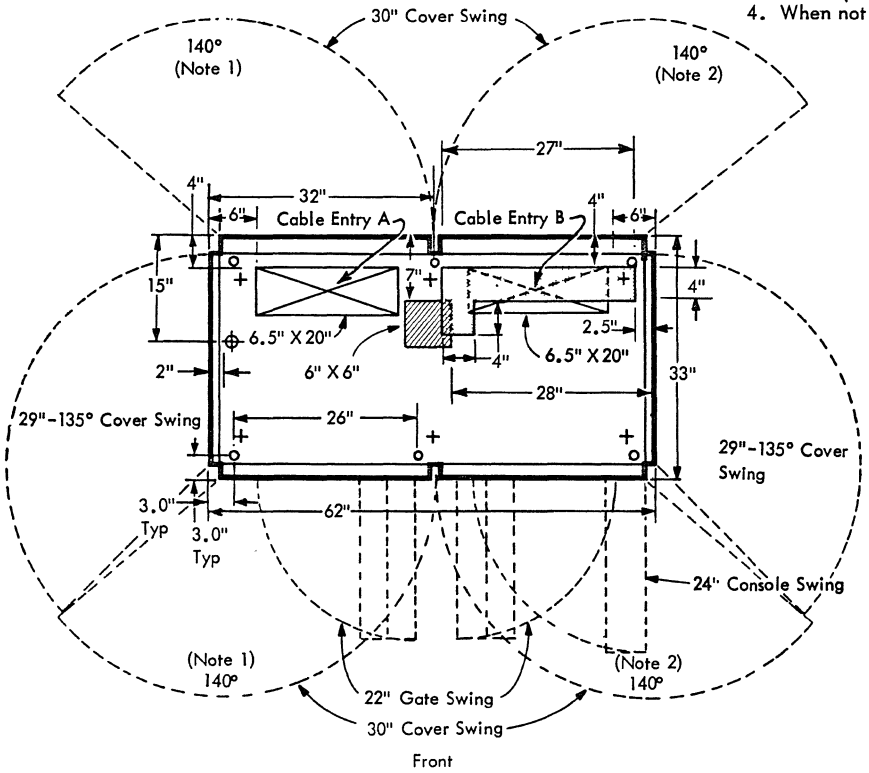

Inches = Centimeters	
2.0	5,0
2.5	6,3
3.0	7,6
4.0	10,1
6.0	15,2
6.5	16,5
7.0	17,7
15.0	38,1
20.0	50,8
22.0	55,8
24.0	60,9
26.0	66,0
27.0	68,5
28.0	71,1
29.0	73,6
30.0	76,2
32.0	81,2
33.0	83,8
62.0	157,4

Notes:
1. 100° if a unit is abutted to the left.
2. 100° if a unit is abutted to the right.
3. Front and/or rear kick strips may be removed when required for non-raised floor cable exits.

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Type	Model	Name	Electrical		Environmental		Weight (lbs)	Dimensions (inches)			Service Clearances (inches)				Notes
			kVA	Conn. Type*	BTU/hr.	ft^3/min		Width	Depth	Height	F	R	L	Rt	
1053	3	Printer	0.1	G or H	335	-	35	23	11.5	9	12	12	12	12	
1054	2	Paper Tape Reader	0.1	-	335	-	20	22.75	13	6.6	12	12	12	12	1
1055	2	Paper Tape Punch	0.1	-	335	-	26	15.38	17.13	8.25	12	12	12	12	1
1442	6 & 7	Card Read-Punch	0.7	-	1,800	50	520	43	24	49	36	30	18	6	1
1443	1 & 2	Printer	1.1	-	2,450	416•	731	55.9	43	46	36	36	30	36	1
1627	1	Plotter	0.1	-	375	-	33	18	15	10	12	12	12	12	1
1627	2	Plotter	0.1	-	375	-	55	40	15	10	12	12	12	12	1
1801	-	Processor-Controller	3.0	E	9,500	650	2,000	62	33	76.5	36	36	30	30	4,6
1802	-	Processor-Controller	3.0	E	9,500	650	2,000	62	33	76.5	36	36	30	30	4,6
1803	-	Core Storage Unit	0.7	-	1,800	490	968	32	33	76.5	36	36	30	30	3,4
1810	A1 & B1	Disk Storage	0.83	-	2,840	150	850	32	33	76.5	36	36	32	32	1
1810	A2 & B2	Disk Storage	1.16	-	3,960	225	930	32	33	76.5	36	36	32	32	1
1810	A3 & B3	Disk Storage	1.5	-	5,120	300	1,010	32	33	76.5	36	36	32	32	1
1816	-	Printer-Keyboard	0.1	G or H	335	-	65	23	19.75	9	12	12	12	12	
1826	1	Data Adapter Unit	1.5	-	4,600	490	968	32	33	76.5	36	36	30	30	2,3,4
1826	2	Data Adapter Unit	0.8	-	2,500	490	968	32	33	76.5	36	36	30	30	3,4
1826	3	Data Adapter Unit	0.7	-	1,800	490	968	32	33	76.5	36	36	30	30	3,4
1827	-	Data Control Unit	3.3	E	9,140	490	1,000	32	33	76.5	36	36	30	30	3,4,6
1828	1	Enclosure	-	-	-	-	642	32	33	76.5	36	36	30	30	4
1828	2	Enclosure	-	-	-	-	567	32	33	76.5	36	36	30	30	4
1851	1 & 2	Multiplexer Term	Nil	-	Nil	-	88	Mount inside the 1828							
1856	1 & 2	Analog Output Term	0.4	-	1,160	490	140								
2311	-	Disk Storage Drive	0.75	-	2,000	100	390	30	24	38	36	36	30	30	
2401	1,2 & 3	Magnetic Tape Unit	1.6	-	3,500	500	800	30	29	60	36	36	30	30	1
2402	1,2 & 3	Magnetic Tape Unit	3.2	-	7,000	1,000	1,600	60	29	60	36	36	30	30	1
2841	-	Storage Control Unit	1.1	D	3,100	1,000	750	32	45.5	60	30	30	48	30	

*Connector type specifies the IBM-supplied power-cord plug, the customer-provided receptacle (or in-line connector), and the branch circuit specifications.

Conn. Type	Plug ‡	Receptacle ‡	In-Line Connector ‡	Branch Circuit			
				Voltage	Amps.	Phase	Wires †
D	Russell & Stoll FS3760	Russell & Stoll FS3754	Russell & Stoll FS3934	208/230	30	3	4
E	Russell & Stoll SC7328	Russell & Stoll SC7324	Russell & Stoll SC7428	208/230	60	3	4
G	Pass & Seymour #5266	Pass & Seymour #5261 or #5262	Pass & Seymour #5269	115	15	1	3
H	Hubbell #5666	Hubbell #5661	Hubbell #5669	208/230	15	1	3

‡ IBM supplies the listed (or equivalent) plug. The customer provides the listed (or equivalent) receptacle or connector.
† Includes equipment ground (green) wire. See primary Electrical Power Requirements for details.

Phase Distribution Within 1801/1802	
Type	Phases Used
1054	1,3
1055	1,3
1442	2,3
1443	2,3
1627	1,3
1803	1,2
1810	1,3
1826	1,2,(3) Note 5
1828	1,2,(3)
2401/2	1,2,3

Notes:

1. Power supplied by 1801/1802. Add kVA of attached units. Single phase loads are distributed on 3 phase primary power input at 1801/1802.
2. KVA = 1.6 without AI Expander, BTU = 4250 without AI Expander.
3. Ft^3/min and Weight with all features installed.
4. Right and left service clearance when not abutted to another unit of the system.
5. Phases 1 and 2 are used for the first unit. Phases are rotated between additional units.
6. This unit is equipped with radio frequency interference control circuitry and requires a good wired earth ground or an adequate building ground. Total resistance of the ground conductor, measured between the receptacle and the building ground point, may not exceed 3 ohms. For proper operation, all components of the system must have the same ground reference. Conduit is not an adequate means of grounding.

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Figure 24. Summary of Specifications

Type	Model	Name	Electrical		Environmental		Weight (kg)	Dimensions (centimeters)			Service Clearances (centimeters)				Notes
			kVA	Power Cord Style	kcal/hr	m^3/min		Width	Depth	Height	F	R	L	Rt	
1053	3	Printer	0.1	G1	,084	-	16	58	29	23	30	30	30	30	
1054	2	Paper Tape Reader	0.1	-	,084	-	9	57	33	17	30	30	30	30	1
1055	2	Paper Tape Punch	0.1	-	,084	-	12	39	44	21	30	30	30	30	1
1442	6&7	Card Read-Punch	0.7	-	,454	1,4	236	109	61	124	91	76	46	15	1
1443	1&2	Printer	1.1	-	,617	11,8	332	142	109	117	91	91	76	91	1
1627	1	Plotter	0.1	-	,095	-	15	46	38	25	30	30	30	30	1
1627	2	Plotter	0.1	-	,095	-	25	102	38	25	30	30	30	30	1
1801	-	Processor-Controller	3.0	E5	2,393	18,4	907	157	84	194	91	91	76	76	4,5
1802	-	Processor-Controller	3.0	E5	2,394	18,4	907	157	84	194	91	91	76	76	4,5
1803	-	Core Storage Unit	0.7	-	,454	14	439	81	84	194	91	91	76	76	3,4
1810	A1 & B1	Disk Storage	0.83	-	,716	4,2	386	81	84	194	91	91	81	81	1
1810	A2 & B2	Disk Storage	1.16	-	,998	6,4	422	81	84	194	91	91	81	81	1
1810	A3 & B3	Disk Storage	1.5	-	1,290	8,5	458	81	84	194	91	91	81	81	1
1816	-	Printer-Keyboard	0.1	G1	,084	-	30	56	50	23	30	30	30	30	
1826	1	Data Adapter Unit	1.5	-	1,159	14	439	81	84	194	91	91	76	76	2,3,4
1826	2	Data Adapter Unit	0.8	-	,630	14	439	81	84	194	91	91	76	76	3,4
1826	3	Data Adapter Unit	0.7	-	,454	14	439	81	84	194	91	91	76	76	3,4
1827	-	Data Control Unit	3.3	E5	2,303	14	453	81	84	194	91	91	76	76	3,4,5
1828	1	Enclosure	-	-	-	-	291	81	84	194	91	91	76	76	4
1828	2	Enclosure	-	-	-	-	258	81	84	194	91	91	76	76	4
1851	1&2	Multiplexer Terminal	Nil	-	Nil	-	40	Mounts inside the 1828							
1856	1&2	Analog Output Term	0.4	-	,292	14	64								
2311	-	Disk Storage Drive	0.75	-	,504	3	177	76,2	61	96,5	91	91	76	76	
2401	1,2&3	Magnetic Tape Unit	1.6	-	,882	14,2	362	76	74	152	91	91	76	76	1
2402	1,2&3	Magnetic Tape Unit	3.2	-	1,764	28,3	725	152	74	152	91	91	76	76	1
2841	-	Storage Control Unit	1.1	D2	,781	28	340	81,3	115,6	152,4	76	76	122	76	

Notes:

1. Power supplied by 1801/1802. Add kVA of attached units. Single phase loads are distributed on 3 phase primary power input at 1801/1802.
2. KVA = 1.6 without AI Expander. kcal = 1071 without AI Expander.
3. Weight and m^3/min with all features installed.
4. Right and left service clearances when not abutted to another unit of the system.
5. This unit is equipped with radio frequency interference control circuitry and requires a good wired earth ground or an adequate building ground. Total resistance of the ground conductor, measured between the receptacle and the building ground point, may not exceed 3 ohms. For proper operation, all components of the system must have the same ground reference. Conduit is not an adequate means of grounding.

Power Cord Style	Service Size Rating *	Cable O.D.			Conductor		
		(in.)	(cm)	Shield	Quantity	Nominal O.D. (in.)	(cm)
D2	30 amp, 3 phase, 5 wire	0.75	2,0	1	5	0.102	0,300
E5	60 amp, 3 phase, 5 wire	1.44	3,66	1	5	0.400	1,020
G1	15 amp, 1 phase, 3 wire				3	0.040	0,102

* The number of wires includes one insulated grounding conductor (green with yellow trace).

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Figure 25. Summary of Specifications (Metric)

Power and Signal Interfaces

CABLES

Two cable connector panels are located at the rear of the P–C (Figure 26). These panels supply power and/or signals to the various I/O devices which are attached to the P–C. Connector panel A supplies power to the 1442, 1443, 1810, 1826, 1828, and 2401 (Figure 27). The connectors for the 1054, 1055, and 1627 devices provide both power and signals. The 1443-1A connector provides emergency power off (EPO) signaling. Connector panel B can contain a maximum of 27 IBM serpent connectors which provide interface connections to the I/O devices attached to the 1800 system.

Each I/O device in the 1800 system has one or more cables which supply the required signals and power to the device. These cables are shown in Figures 28 and 29. Cables from a device are assigned group numbers to facilitate ordering. The group numbers can indicate one or more physical cables between a device and the P–C; but do not combine cables of unrelated I/O device features within the group, e.g., Cable groups 3, 4, 5, 6, 9, and 31 contain cables with identical part numbers.

POWER CABLING

The processor–controller requires a 208/230 V, 60 Hz, 60 amp, 3 phase service. This service supplies power to the P–C as well as the data processing I/O devices (2401, 2402, 1442, 1443, 1054, 1055, 1627, and 1810), and the system process I/O adapters housed in 1826 and 1828 units. Power cabling connectors for the DP I/O adapters are located on connector panel A (Figure 27).

In addition to supplying the required voltages to the adapters, connector panel A also supplies the data and control lines to the 1627 plotter, the 1054 paper tape reader, and the 1055 paper tape punch. Therefore, the data and control lines for these devices are included in the power connector tables.

1801/1802 Power

Power is supplied to the P–C via a four-wire (60 Hz) or five-wire cable (50 Hz). Three wires in this cable supply the 60 Hz, 208 volt, 3 phase, 60 amp service; the fourth wire provides a no-current equipment ground (figure 31).

1803, 1810, 1826, and 1828 Power Connectors

The 1803, 1810, 1826, and 1828 units receive power from the P–C. These units contain dc power supplies and do not require dc voltages from the P–C. Figure 32 lists the voltages and pin connections for these units. The connectors for these units are shown in Figure 30.

2401/2402 Power Connector

The 2401/2402 magnetic tape units receive three phase, 30 amp, 208 V, 60 cycle power from the P–C. These units contain their own dc power supplies. Figure 30 shows the power connector and Figure 33 lists the pin connections.

1442 Power Connector

The 1442 card read–punch receives both ac and dc power from the P–C. The 18–pin connector is similar in appearance to the connector used for 1826 power. Figure 34 lists the voltages and pin connections for this unit.

Emergency Power Off and Power Connectors to the 1443

The emergency power off connector lines are listed in Figure 35. Figure 36 lists the power connector and associated pin assignments.

Power Connectors to the 1054, 1055, and 1627

Both power and signals are supplied to the 1054, 1055, and 1627 via the respective power connectors. Figures 37, 38, and 39 list the power and signal connections for the 1054, 1055, and 1627, respectively.

1053 Cables

Eight–foot lengths of 1053 cable (group #22) are supplied at no charge. Lengths greater than 8' (2, 4 m) are priced per foot for cables up to a maximum of 2,000 feet (609 m). If customer supplied cable is to be used in lieu of IBM cable, the following specifications must be adhered to:

1. 30 individual conductors (twisted pair not recommended); planetary lay is satisfactory.
2. Maximum resistance per line to 1053 load = 15.4Ω
3. Line capacitance = not critical
   Insulation = 300 V
4. The IBM–supplied cable consists of 37 conductors (30 used), AWG #18 (0, 824 mm^2) stranded.

Short length cables, for connection to customer–supplied cables, are available from IBM by special order (RPQ), or the customer may cut the IBM cable and provide suitable junction(s) to reconnect the cable.

Cable Connectors

Figure 30 shows the cable connectors used in the 1800 system. The dimensions given for the connectors are maximum overall measurements and may be used in calculations concerning subfloor clearances.

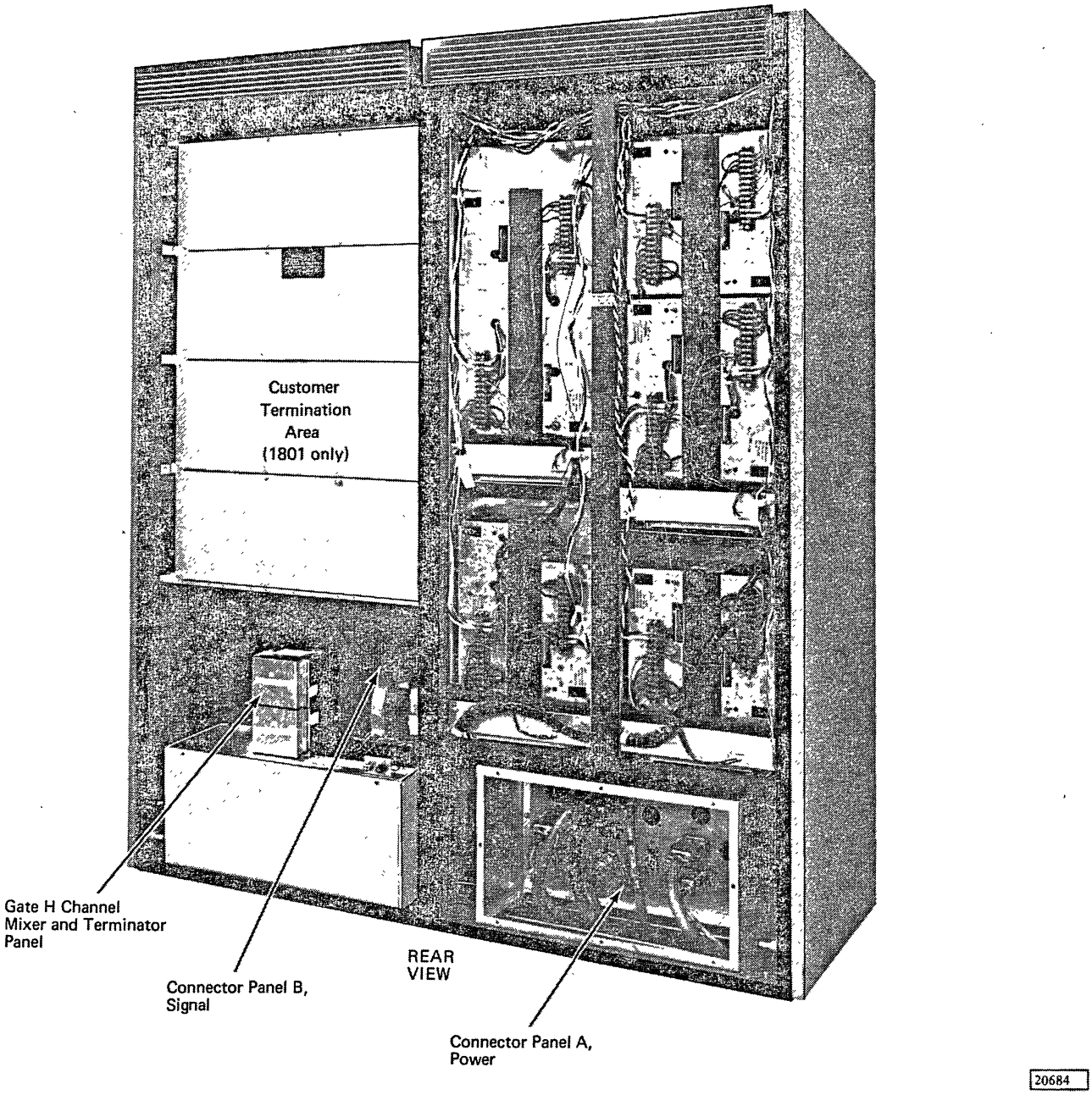


Figure 26. 1801/1802 Connector Panels

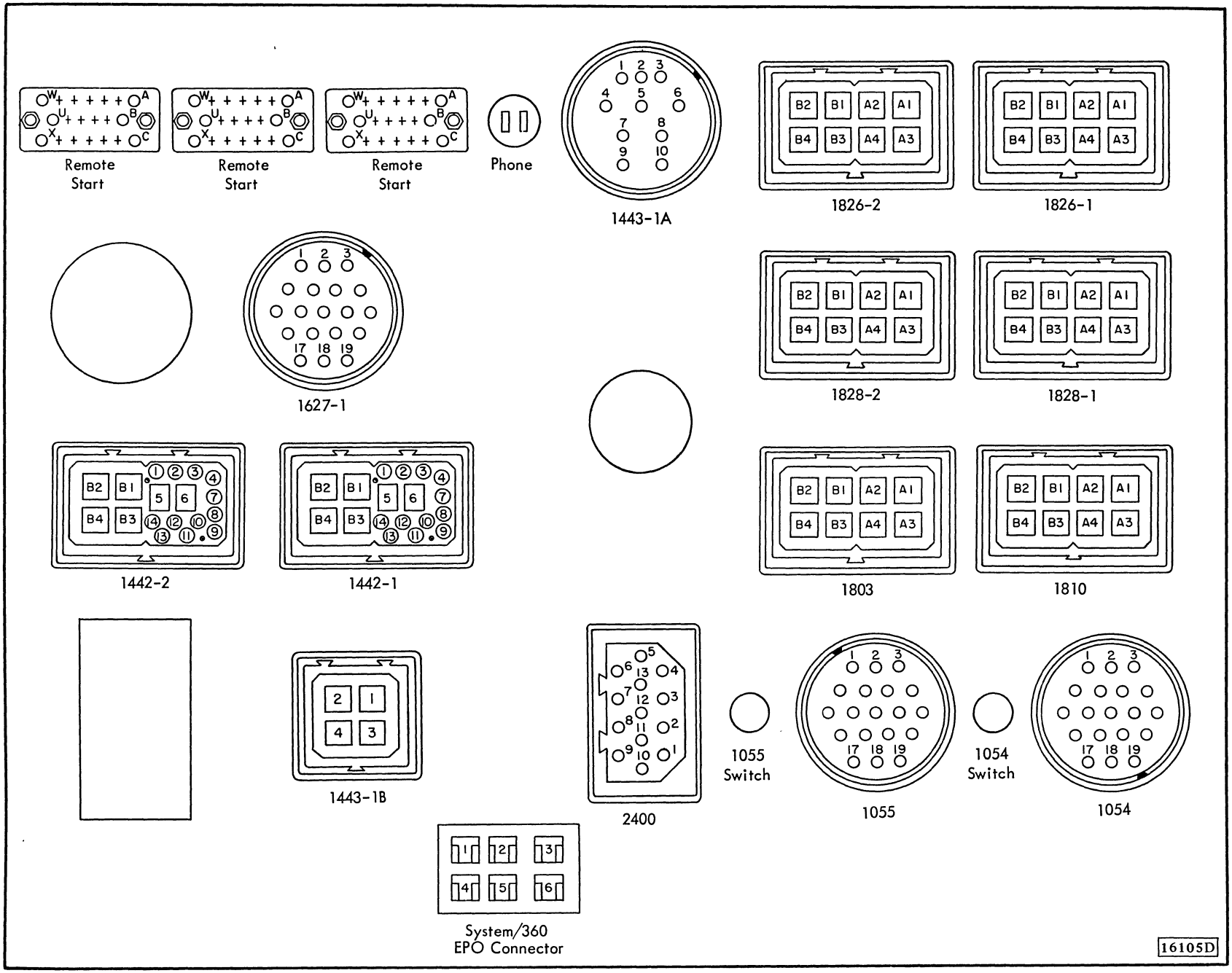
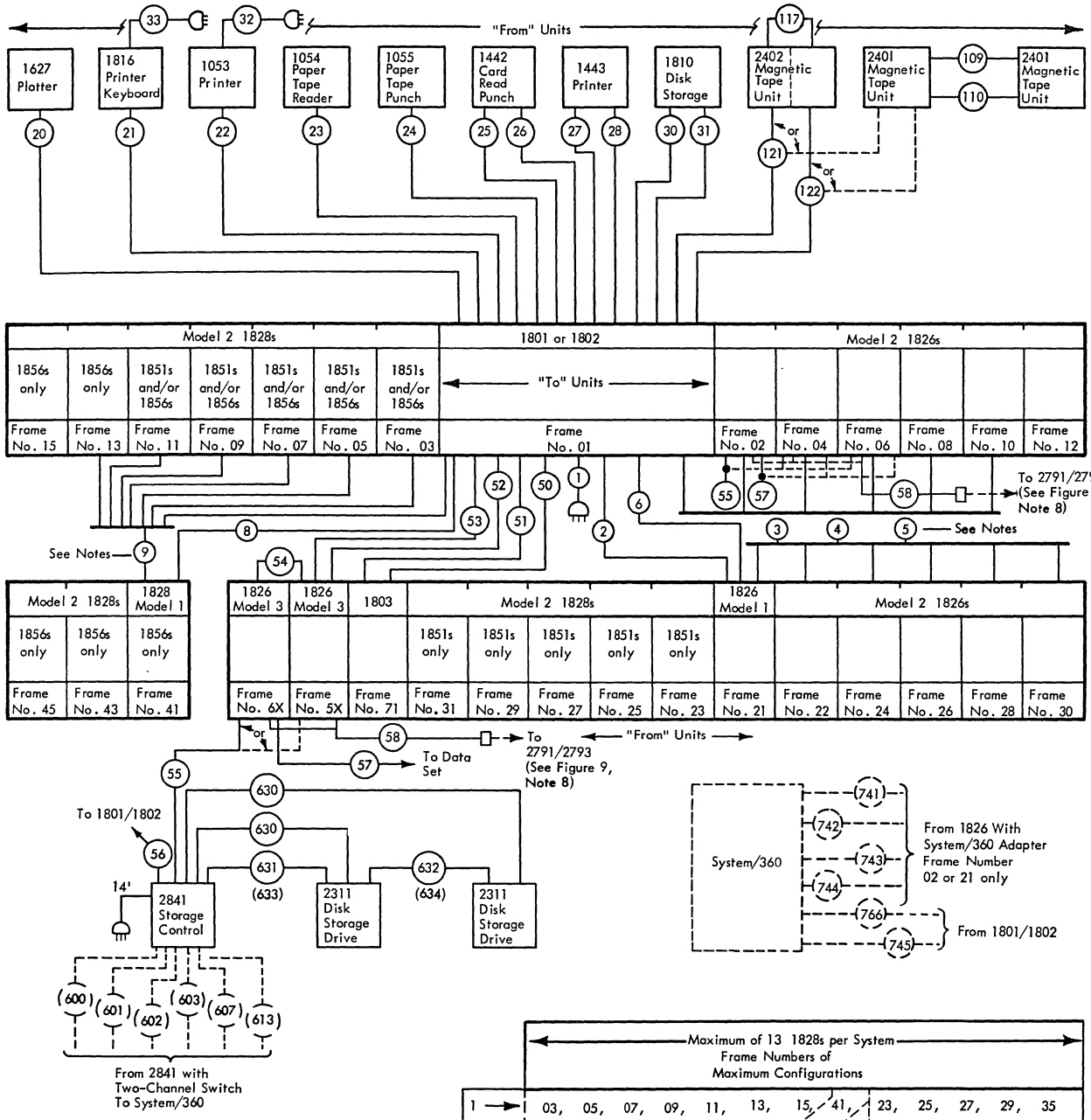


Figure 27. Connector Panel A, Power



	Maximum of 13 1828s per System — Frame Numbers of Maximum Configurations												
1 →	03,	05,	07,	09,	11,	13,	15,	41,	23,	25,	27,	29,	35
2 →	03,	05,	07,	09,	11,	13,	41,	43,	23,	25,	27,	29,	35
3 →	03,	05,	07,	09,	11,	41,	43,	45,	23,	25,	27,	29,	35
	Model 2 Units Abutted to 1801 or 1802						Model 1 Units	Model 2 Units Abutted to Model 1	Model 2 Units Abutted to 1826 Model 1				

Notes:

Cable Groups (3), (4), (5), and (9) are individually ordered once per system.

Cable (9) (Analog Output) will always connect to frame number 41 (1828 Model 1) of the "FROM" units and will be routed to the highest numbered frame (in the "TO" units) that contains an 1856 (In 1828 Model 2 or frame 01 if no 1856 in "TO" units).

Cable group number (3) (Process Interrupt) or (4) (Digital Input), or (5) (Digital Output) will connect to the highest numbered "TO" frame that contains the feature and will be routed from the lowest numbered "FROM" frame that contains the respective feature. If the feature does not appear in the "TO" units the cable will connect to frame 01.

Cable groups 600-603, 607, 613, 741-745, and 766 are listed in System/360: Cable Order Form and Installation Manual — Physical Planning

Cable groups 630-634 are listed as part of 1800 System (see Figure 9)

Cable groups 52, 53, and 54 are ordered for 1826-3 features: 9311, 9312, and 9313 with following exceptions:

1. 9311 cannot be used if any model 1810 is configured. Frame number for first 1826-3 is 51; second 1826-3 is 61.
2. 9312 cannot be used if 1826-1 with S/360 adapter or analog input expander is configured. Frame number for first 1826-3 is 52; second 1826-3 is 62.
3. 9313 is only applicable if configuration includes a data channel expander Frame number for first 1826-3 is 53; second 1826-3 is 63.

23176.1C

Figure 28. 1800 System Cabling Schematic

Figure 29. 1800 System Cabling Specifications (Part 1 of 2)

1801 or 1802

Cable Group Number	Cable Qty	Standard Length**	Maximum X Length (Feet)	Cable Diameter (Inches)	Cable Bending Radius (Inches)	FROM Unit	TO UNIT Unit	TO UNIT Connector Code No.*	Function	Feature Information	Notes
1	1	14	14 (fixed)	1.500	7.5	Power Outlet	1801 or 1802	1	Power		
2	2	50	100	0.880	4.0	1826 Model 1	1801 or 1802	6	Power		
		50	100	0.500	2.0	1826 Model 1	1801 or 1802		Control		
3	2	50	100	1.000	3.0	Frame #_____	Frame #_____	3	Signal, Process Interrupt	5710	1,2
		50	100	1.000	3.0	Frame #	Frame #	3	Signal, Process Interrupt		
4	1	50	100	1.000	3.0	Frame #	Frame #	3	Signal, Digital Input	3262 or 5861	1
5	1	50	100	1.000	3.0	Frame #	Frame #	3	Signal, Digital Output	3296	1
6	2	50	100	1.000	3.0	1826 Model 1	1801 or 1802	3	Signal, Analog Input Expander	1237 or 7720	
		50	100	1.000	3.0	1826 Model 1	1801 or 1802	3	Signal, Analog Input Expander	(1 only)	
8	2	50	100	0.875	3.0	1828 Model 1	1801 or 1802	6	Power		
		50	100	0.500	2.0	1828 Model 1	1801 or 1802		Control		
9	1	50	100	1.000	3.0	1828 Model 1	Frame #	3	Signal, Analog Out		1
20	1	20	20	0.525	2.0	1627	1801 or 1802	5	Power and Signal		
21	2	20	50	0.600	2.0	1816 Ptr. #1 or 2	1801 or 1802	3,8	Signal		
		20	50	0.475	2.0	1816 Kybd.	1801 or 1802	3,7	Signal		
22	1	8	2000	0.600	2.0	Each 1053	1801 or 1802	3,8	Signal		
23	1	20	20	0.750	3.0	1054	1801 or 1802	5	Power and Signal		
24	1	20	20	0.405	2.0	1055	1801 or 1802	5	Power and Signal		
25	1	20	20	0.750	3.0	1442 1st or 2nd	1801 or 1802	6	Power		
26	1	20	20	1.090	3.0	1442 1st or 2nd	1801 or 1802	3 (2)	Signal		
27	2	25	25	0.750	3.0	1443	1801 or 1802	5	Power Sequence		
		25	25	0.560	2.0	1443	1801 or 1802	2	Power		
28	1	25	25	0.750	3.0	1443	1801 or 1802	3	Signal		
30	1	20	20	0.750	3.0	1810	1801 or 1802	6	Power		
31	2	20	20	1.000	3.0	1810	1801 or 1802	3	Signal		
		20	20	1.000	3.0	1810	1801 or 1802	3	Signal		
32	1	8	8 (fixed)	0.400	2.0	Power Outlet	1053		Power		
33	1	8	8 (fixed)	0.400	2.0	Power Outlet	1816		Power		
50	1	16	16	0.880	4.0	1803	1801 or 1802		Power		
51	2	13	13	1.005	4.0	1803	1801 or 1802		Signal		
		13	13	1.005	4.0	1803	1801 or 1802		Signal		
52	2	25	Note 5	1.000	3.0	1826 Model 3	1801 or 1802		Signal		
		25	Note 5	1.000	3.0	1826 Model 3	1801 or 1802		Signal		
53	1	25	Note 5	0.880	4.0	1826 Model 3	1801 or 1802		Power		
54	3	5	Note 5	1.000	3.0	1826 Model 3	1826 Model 3		Signal		
		5	Note 5	1.000	3.0	1826 Model 3	1826 Model 3		Signal		
		5	Note 5	0.880	4.0	1826 Model 3	1826 Model 3		Power		
55	2	50	100	1.000	3.0	2841	1826 Model 2 or 3		Signal	7710 on 1826	
			100	1.000	3.0	2841	1826 Model 2 or 3		Signal		
56	1	50	100	0.500	2.0	2841	1801 or 1802		E.P.O.	7710 on 1826	
57	1	25	50	0.500	2.0	Data Set	1826 Model 2 or 3	12	Signal	7751 on 1826	
58	1	40	40	0.750	3.0	Junction	1826 Model 2 or 3	13	Signal	7570 on 1826	8,10
121	1	25	100	0.750	3.0	2401 or 2402	1802	4	Power		3
122	1	25	100	1.000	3.0	2401 or 2402	1802	3 (3)	Signal		3
109	1	5	Note 3	1.000	3.0	2nd 2401	1st 2401		Signal		3
110	1	5	Note 3	0.750	3.0	2nd 2401	1st 2401	4	Power		3
117	1	Fixed	Fixed	1.000	3.0	1/2 2402	1/2 2402		Jumper Signal Cable		
630	1	25	50	1.000	3.0	2311	2841	9	Power		
631	2	25	Note 6	1.000	3.0	2311	2841	10	Power		7,9
(633)				1.000	3.0	2311	2841	11	Signal		
632	2	10	Note 6	1.000	3.0	2311	2311	10	Power		7
(634)				1.000	3.0	2311	2311	11	Signal		

23178.0M

1827

71	1	14	14 (fixed)	1.500	7.5	Power Outlet	1827	1	Power		
72	2	50	100	0.880	4.0	1826 Model 1	1827	6	Power		
		50	100	0.500	2.0	1826 Model 1	1827		Control		
74	1	50	100	1.000	3.0	Frame #	Frame #	3	Signal, Digital Input	3262 or 5861	1
75	1	50	100	1.000	3.0	Frame #	Frame #	3	Signal, Digital Output	3296	1
78	2	50	100	0.875	3.0	1828 Model 1	1827	6	Power		
		50	100	0.500	2.0	1828 Model 1	1827		Control		
79	1	50	100	1.000	3.0	1828 Model 1	Frame #	3	Signal, Analog Out		1

* Connectors code numbers are identified for each connector illustrated in the System Cable Connector figure.

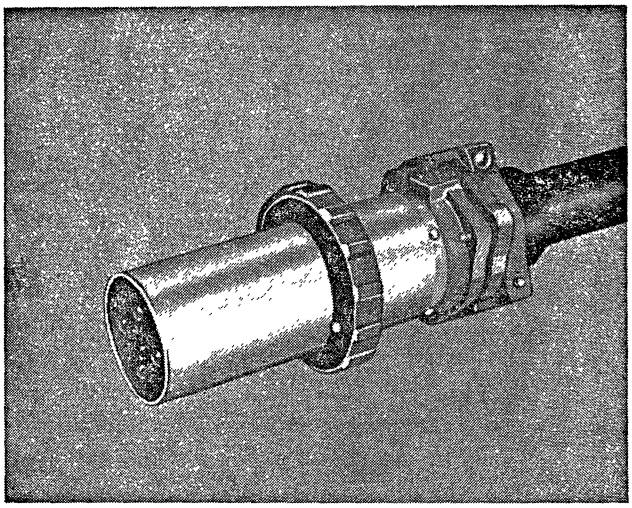
** Standard length cables will be shipped unless a cable order form is received 120 days prior to scheduled delivery.

Notes:

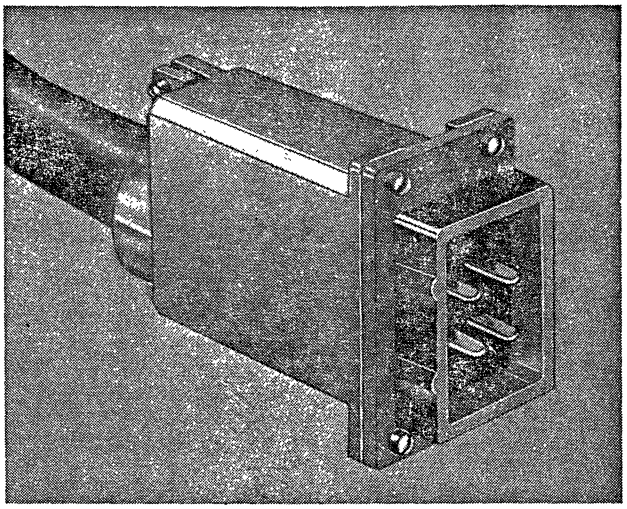
1. Frame number for cable routing ("FROM" unit - "TO" unit) can be determined from the information supplied in the System Cabling Schematic figure.
2. The second cable in Cable Group 3 will be routed to the same frame number as designated for the first cable of that group.
3. Total length of 100 feet available for sum of group 121 + group 110 or group 122 + group 109 when two 2401s are used.
4. Where the "TO" unit is 1801 or 1802 all Code 3 connectors use cable entry point B, all other connectors use cable entry A.
5. Maximum X length of group 52 plus 54 is 40 ft. maximum X length of group 53 plus 54 is 60 ft.
6. Maximum X length of group 631 plus 632 is 100 ft.
7. Cable group numbers in ( ) are ordered for 50 Hz systems.
8. Cable 58 is terminated with four IBM-provided type 283B plugs. The mating connectors are customer-provided Western Electric type 404B surface mounted or Western Electric type 493A flush mounted or equivalent jacks. See 2790 Physical Planning, A27-3017.
9. Cable group 631 (633) includes end-of-line terminator.
10. Order one cable group 58 for each 7570 feature installed. Maximum: two per system.

23178.1M

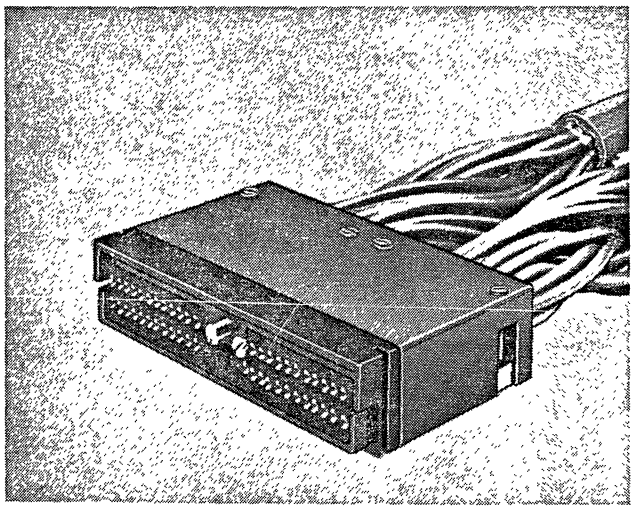
Figure 29. 1800 System Cabling Specifications (Part 2 of 2)



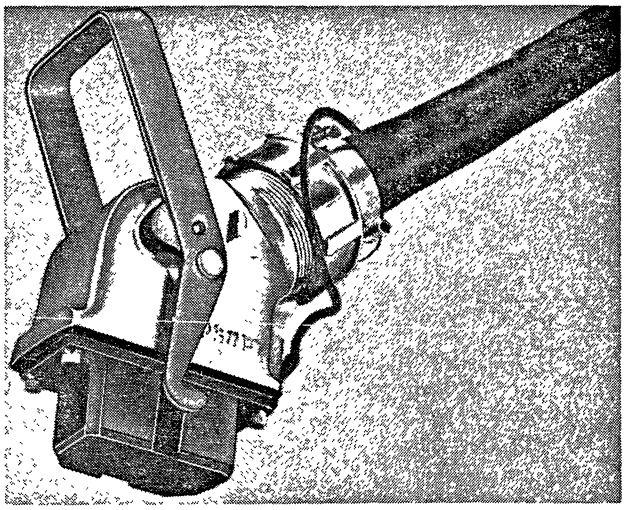
Power Cord Connector (3-phase, 60-amp, 4-wire, O.D. 3.75 inches, 9 inches long) Code 1



Power Connector (1.7 inches high, 1.42 inches wide, 3.28 inches deep) Code 2



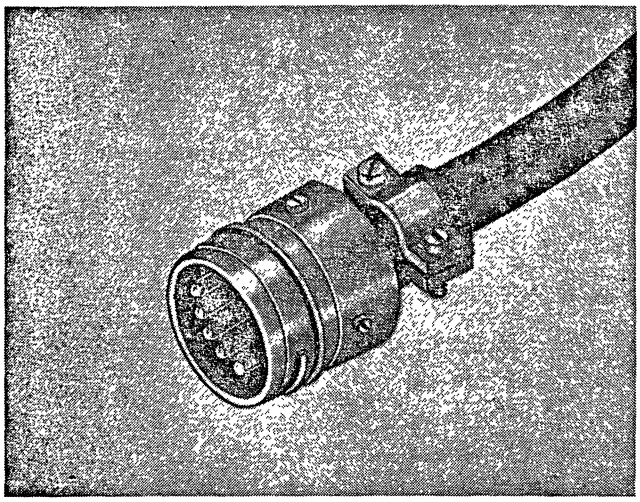
1800 System Interface Connector (3 inches high, 4 inches wide, 1 inch deep) Code 3



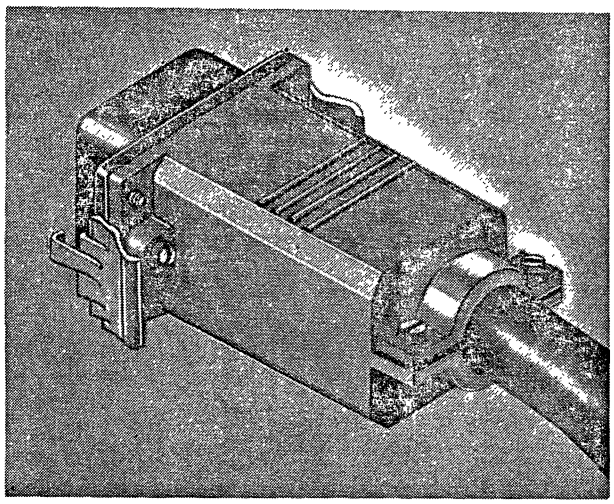
Tape Power Cable Connector (3.62 inches high, 4.5 inches deep, 2.06 inches wide) Code 4

30124.0

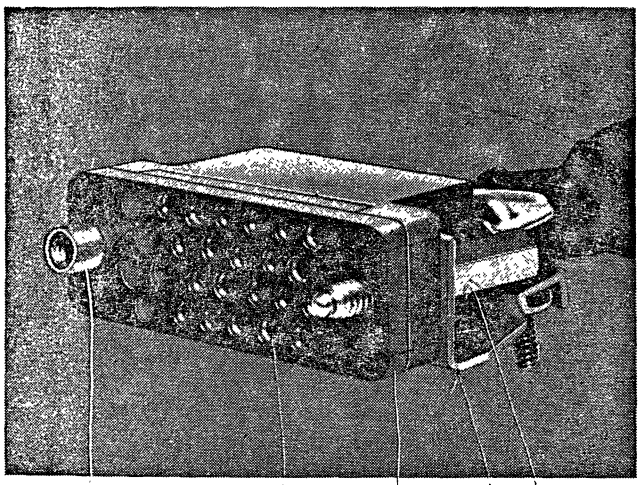
Figure 30. 1800 System Cable Connectors (part 1 of 3)



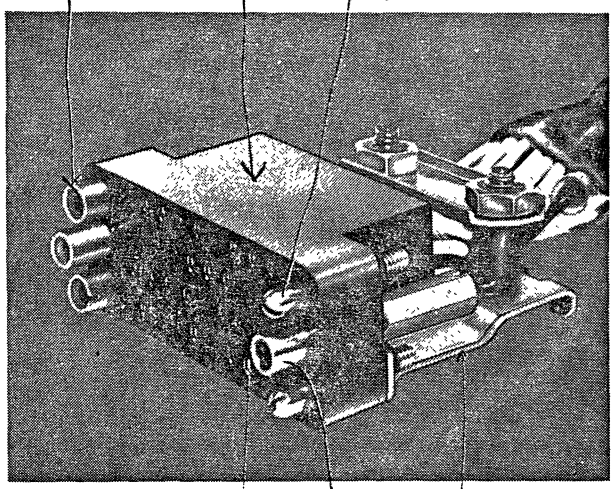
Power and Signal Connector
(1.5 inches diameter, 1.2 inches long) Code 5



Power Connector (1.6 inches high, 1.5 inches wide, 4 inches deep) Code 6



1816 Signal Connector
(0.62 inches high, 1.62 inches wide, 1.00 inch deep) Code 7



1053 Signal Connector
(0.75 inches high, 2.00 inches wide, 1.00 inch deep) Code 8

male
2123031

strain relief asm.
224 2425
30124.1

jack screw
2123030 (2)

terminal (30)
2122261

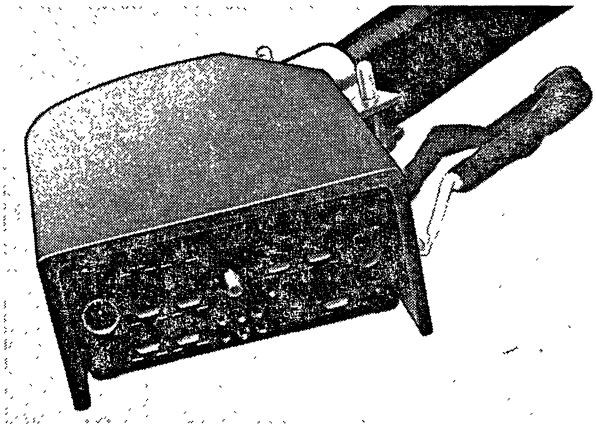
female
2123030

strain relief asm
2198251

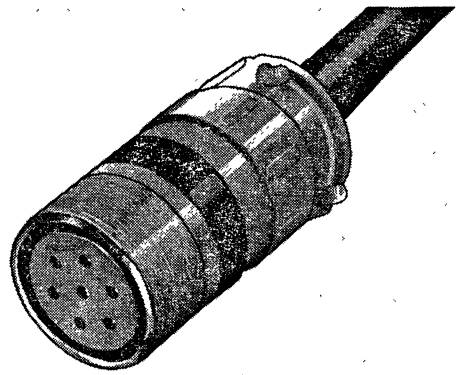
connector
2122537

terminal
2122257 (21)

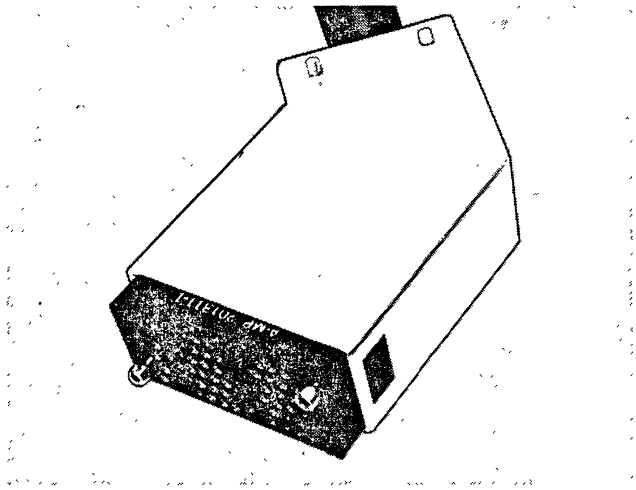
Figure 30. 1800 System Cable Connectors (part 2 of 3)



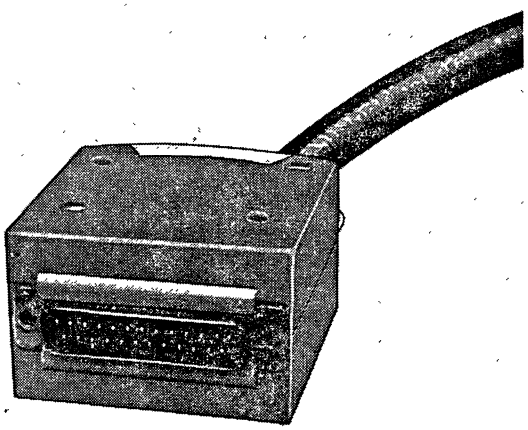
2311 DC Connector (1.5 inches high, 2.7 inches wide, 4 inches deep) Code 9



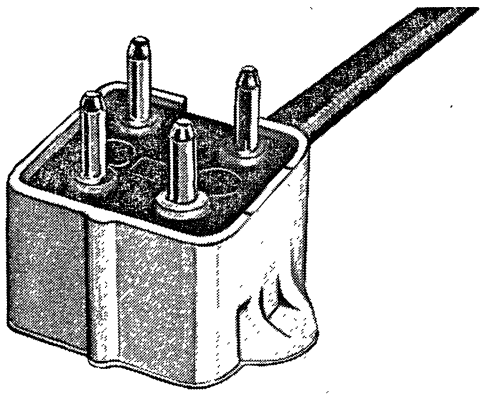
2311 AC Connector (1.5 inches diameter, 3.25 inches long) Code 10



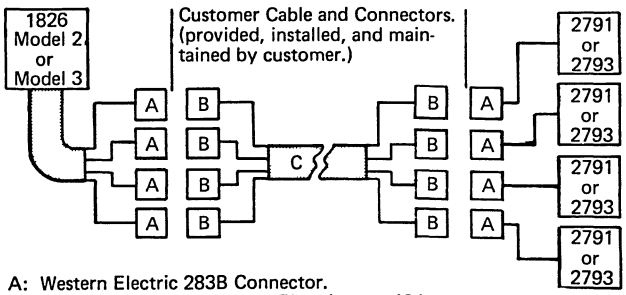
2311 Signal Connector (1.25 inches high, 2.75 inches wide, 5 inches deep) Code 11



Data Set Signal Connector (1.38 inches high, 2.19 inches wide, 2.62 inches deep) Code 12



2790 Signal Connector (1.32 inches high, 1.80 inches wide, 0.90 inches deep) Code 13



A: Western Electric 283B Connector.
B: Customer provided Western Electric type 404B surface-mounted or 493A flush-mounted, or equivalent connectors.
C: For cabling information, see 2790 Data Communication System Installation Manual ---- Physical Planning, Order No. GA27-3017.

30124.2A

Figure 30. 1800 System Cable Connectors (part 3 of 3)

Voltage	Phase	Plug Pin Number
208	1	3
208	2	2
208	3	1
Equipment Ground	-	G

16108

Figure 31. 1801 and 1802 Power Input, Connector Code 1

Floor to Frame Clearance

The minimum floor-to-frame clearance (standing on casters) is 4 inches (10, 1 cm) for the 1801, 1802, 1826, 1827, and 1828 units.

SIGNAL CABLING

Connector panel B (Figure 40) contains up to 31 signal connectors. These connectors are the IBM serpentine type (Figure 41) and provide input/output signals to the I/O devices which can be attached to the 1800 System.

All adapters used with the 1800 system connect to the I/O channel through a standard interface. The interface consists of two signal connectors. Figures 42 and 43 illustrate the pin assignments for I/O channel 1 connector interface. Figures 42 and 44 illustrate the connector interface for I/O channel 2, and Figures 42 and 45 illustrate the connector interface for I/O channel 3. The connector locations given in the figure titles refer to the signal connector panel illustrated in Figure 28. Data channels (1 – 15 are identified in system diagrams as CS Req (cycle-steal request) and CS Ack (cycle steal acknowledge) as 0 – 14 respectively. To assign any I/O adapter to a data channel the respective CS Req and CS Ack is jumpered at the I/O channel origin to one of the lines A through E, F through K, or L through G. The CS Req and the CS Ack lines are also jumpered through the CS mixer board (H-A1). At the I/O adapter the CS Req and CS Ack are in turn jumpered to the selected line.

Non-IBM devices which are to be connected to the 1800 system should interface to the standard I/O channel. The use of the I/O channel provides maximum control and flexibility to engineering personnel designing the control adapter for the non-IBM device or devices.

The basic model of the 1801 P-C contains the 1816/1053, digital/analog output, and the digital input adapters. The basic model of the 1802 P-C includes the 1801 P-C adapters and adds the magnetic tape adapter. Since the 1816, 1053, and 2401/2402 magnetic tape unit are always located separately from the P-C, signal connectors are provided at connector panel B for these devices.

In addition to the basic data processing adapters, the P-C includes the following basic digital/analog interfaces: digital input and output, and, analog output. These interfaces and the standard 1800 system I/O channel interface are available in the basic P-C, but do not appear at connector panel B unless the customer has ordered the 1826-1 or -3, 1828-1, or the 1810. The 1826-2 and 1828-2 units, when abutted to the P-C, utilize internal cabling and, thus, do not require connectors at the connector panel. Connections from the P-C standard I/O channel interface are required for the 1826-1 or -3 and the 1810. When these units are ordered, the I/O channel interface connectors are installed at the connector panel and the interfaces terminate in these units. The interface lines must be terminated with their characteristic impedance at the final unit. Cables for the various units are ordered with the unit and are not a part of the P-C.

60 Hz MACHINES

Pin Number	1826/1803		1828		1810	
	Voltage	Phase	Voltage	Phase	Voltage	Phase
A1	208	1	208	1	208	3
A2	208	2	208	2	208	1
A3	208	3	208	3	—	—
A4	Frame Ground	—	Frame Ground	—	Frame Ground	—
B1	115 ac	—	115 ac	—	115 ac	—
B2	115 ac	—	115 ac	—	115 ac	—
B3	24 ac	—	24 ac	—	—	—
B4	24 ac	—	24 ac	—	—	—

*208V or 230V

50 Hz MACHINES

Pin Number	1826/1803		1828		1810	
	Voltage	Phase	Voltage	Phase	Voltage	Phase
A1	220	1	220	1	220	2
A2	220	2	220	2	220	3
A3	220	3	220	3	—	—
A4	Frame Ground	—	Frame Ground	—	Frame Ground	—
B1	*220	1	*220	1	*220	1
B2	*220	2	*220	2	*220	2
B3	24 ac	—	24 ac	—	—	—
B4	24 ac	—	24 ac	—	—	—

*Input voltage is connected to pins B1 and B2

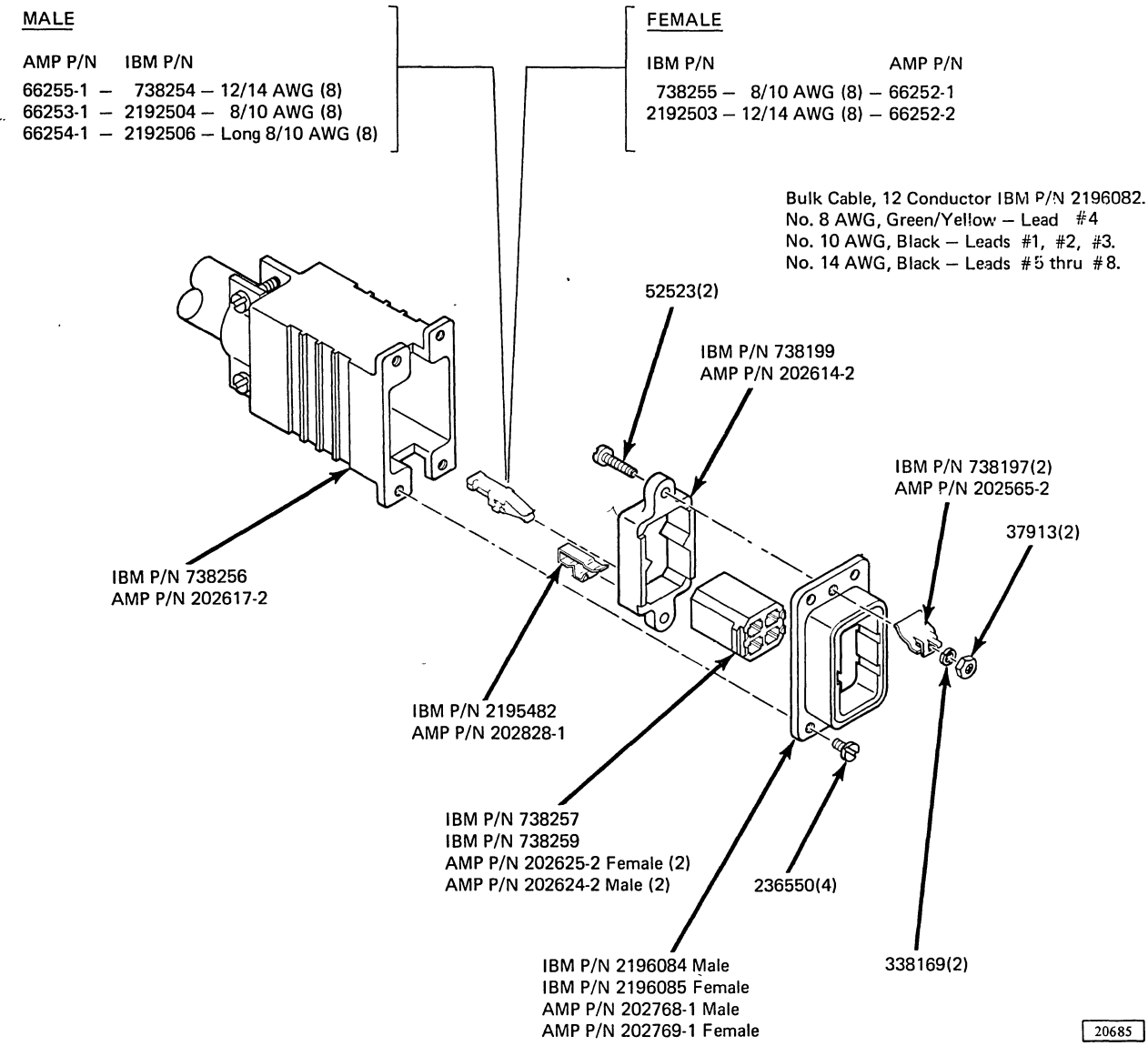


Figure 32. Power Connectors to the 1810, 1803, 1826, 1828, Connector Code 6

Pin	Voltage	Phase
1	115	-
2	115	-
3	Frame Ground	-
4 thru 10	Not Used	-
11	208/230	1
12	208/230	2
13	208/230	3

16143A

Figure 33. Power Connector to the 2401/2402, Connector Code 4

Pin Number	Voltage	Pin Number	Voltage	Pin Number	Voltage
A1	----	A7	115 ac	A13	115 ac
A2	7.5 ac	A8	-----	A14	115 ac
A3	7.5 ac	A9	Frame Ground	B1	+ 6 dc
A4	115 ac	A10	-----	B2	DC Ground
A5	Shield Ground	A11	208 Ø3*	B3	-3 dc
A6	-----	A12	208 Ø2*	B4	+3 dc
* 208 or 230					

16114B

Figure 34. Power Connector to the 1442, Connector Code 6

Pin	1	2	3	4 - 10
Voltage	24 ac	24 ac	24 ac common	Not used

16115A

Figure 35. Emergency Power Off Connector to the 1443, Connector Code 5

50 cycle machines

Pin	Voltage	Phase
A1	—	—
A2	220	3
S3	220	1
A4	Frame Ground	—

60 cycle machines

Pin	Voltage	Phase
A1	—	—
A2	208/230	2
A3	208/230	3
A4	Frame Ground	—

23208A

Figure 36. Power Connector to 1443, Connector Code 2

Pin Number	Voltage or Signal Name	Comments
1	1 Bit Reader	+12V level
2	2 Bit Reader	+12V level
3	4 Bit Reader	+12V level
4	8 Bit Reader	+12V level
5	C Channel Sense	+12V level
6	A Channel Sense	+12V level
7	B Channel Sense	+12V level
8	8 Channel Sense	+12V level
9	Reader Strobe	+12V level
10	Reader Not Ready	+12V level
11	Reader Clutch	0V level
12	--------	
13	--------	
14	Frame Ground	
15	--------	
16	+48 dc	Clutch Magnet
17	115 ac*	Motor Power
18	115 ac Common**	Motor Power
19	+12 dc	Sense Voltage
* 220V L1 on 50 cycle machines ** 220V L2 on 50 cycle machines		

16116A

Figure 37. Power and Signal Connector to the 1054, Connector Code 5

Pin Number	Voltage or Signal Name	Comments
1	1 Punch	0V level
2	2 Punch	0V level
3	4 Punch	0V level
4	8 Punch	0V level
5	C Channel Punch	0V level
6	A Channel Punch	0V level
7	B Channel Punch	0V level
8	8 Channel Punch	0V level
9	-----	
10	Punch Ready	+12V level
11	Punch Clutch	
12	DC Ground	
13	-----	
14	Frame Ground	
15	DC Ground	
16	+48 dc	Punch Clutch
17	115 ac*	Motor Power
18	115 ac Common**	Motor Power
19	+12 dc	Ready Punch
* 220V L1 on 50 cycle machines ** 220V L2 on 50 cycle machines		

16117A

Figure 38. Power and Signal Connector to the 1055, Connector Code 5

Pin Number	Voltage or Signal Name	Comments
1	-----	
2	-----	
3	-----	
4	-----	
5	Drum Up	0V level
6	Drum Down	0V level
7	Carriage Left	0V level
8	Carriage Right	0V level
9	-----	
10	-----	
11	Pen Up	0V level
12	Pen Down	0V level
13	-----	
14	Frame Ground	
15	DC Ground	
16	Plotter Ready	-24V level
17	115 ac *	Motor Power
18	115 ac Common **	Motor Power
19	-----	-----

* 220V L1 on 50 cycle machines
** 220V L2 on 50 cycle machines

16130A

Figure 39. Power and Signal Connector to the 1627, Connector Code 5

Viewed From Rear of 1801/1802

	T	S	R	Q	P
1				I/O Channel 2	DI Channel 1826
2				I/O Channel 2	PI Channel 1826
3				DO Channel 1826	PI Channel 1826
4				AO Channel 1828	
5		8th Printer 1053	4th Printer 1053	2401/2402	2nd 1442
6	I/O Channel 3	7th Printer 1053	3rd Printer 1053	2401/2402	2nd 1442
7	I/O Channel 3	6th Printer 1053	2nd Printer 1053	2401/2402	1443
8	1803	2nd Keyboard 1816	1st Keyboard 1816	I/O Channel 1	1st 1442
9	1803	5th Printer 1053 or 1816	1st Printer 1053 or 1816	I/O Channel 1	1st 1442

16106D

Figure 40. Connector Panel B, Signal

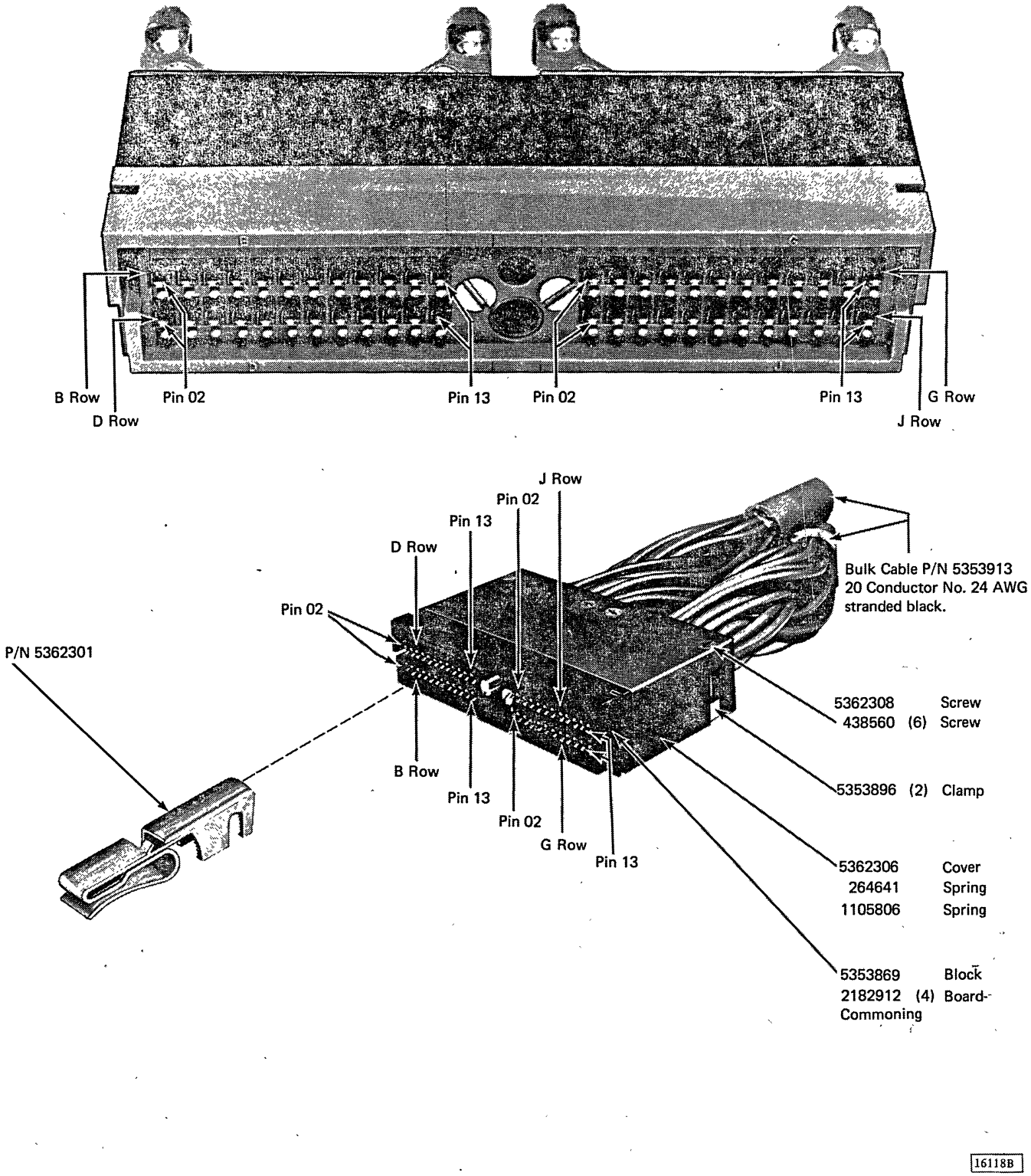


Figure 41. 1800 System Serpent Connector Pin Locations (Signal)

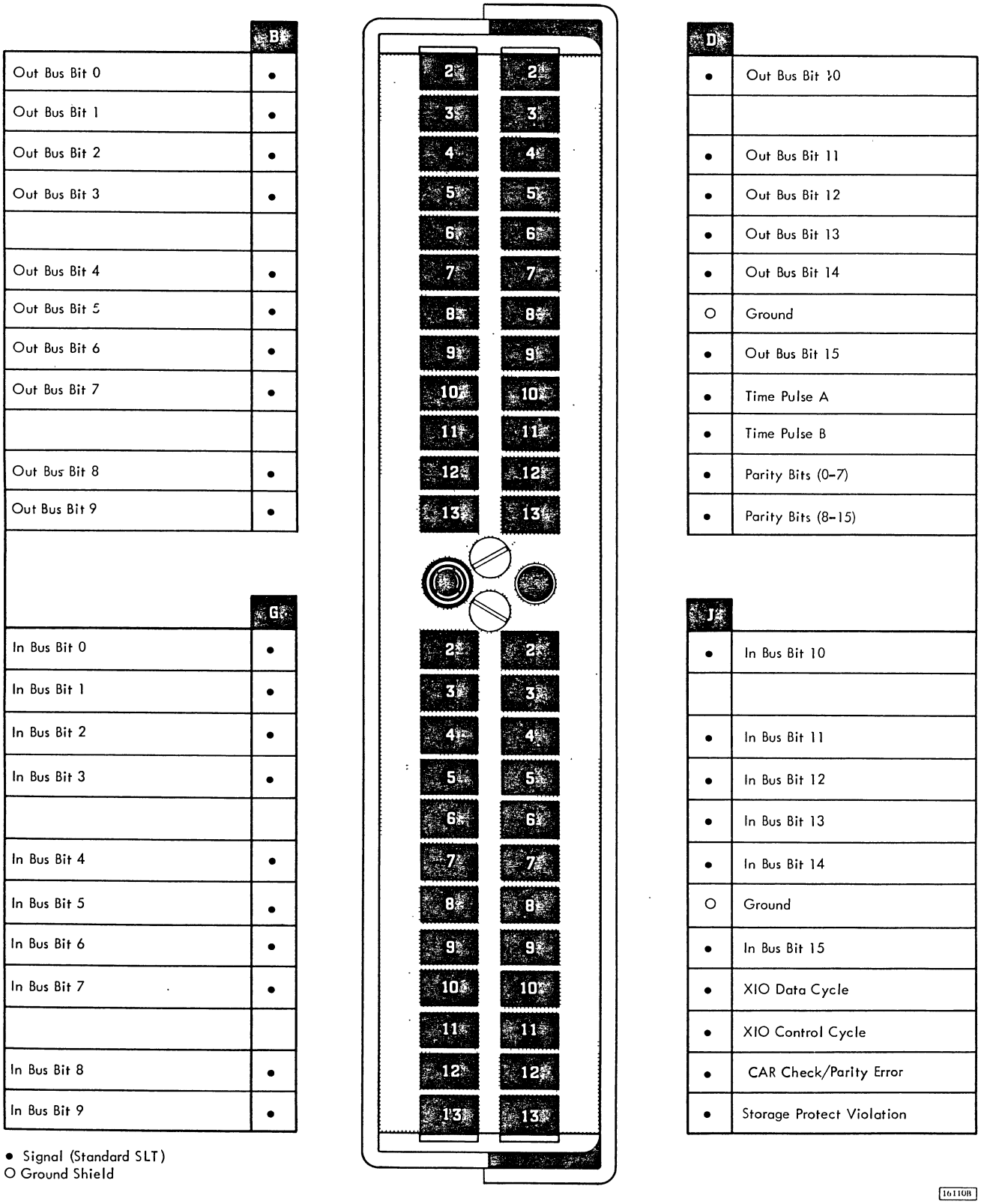


Figure 42. I/O Channel Interface Pin Assignments, Connector Location Q8 (I/O Channel 1), Q2 (I/O Channel 2), or T6 (I/O Channel 3)

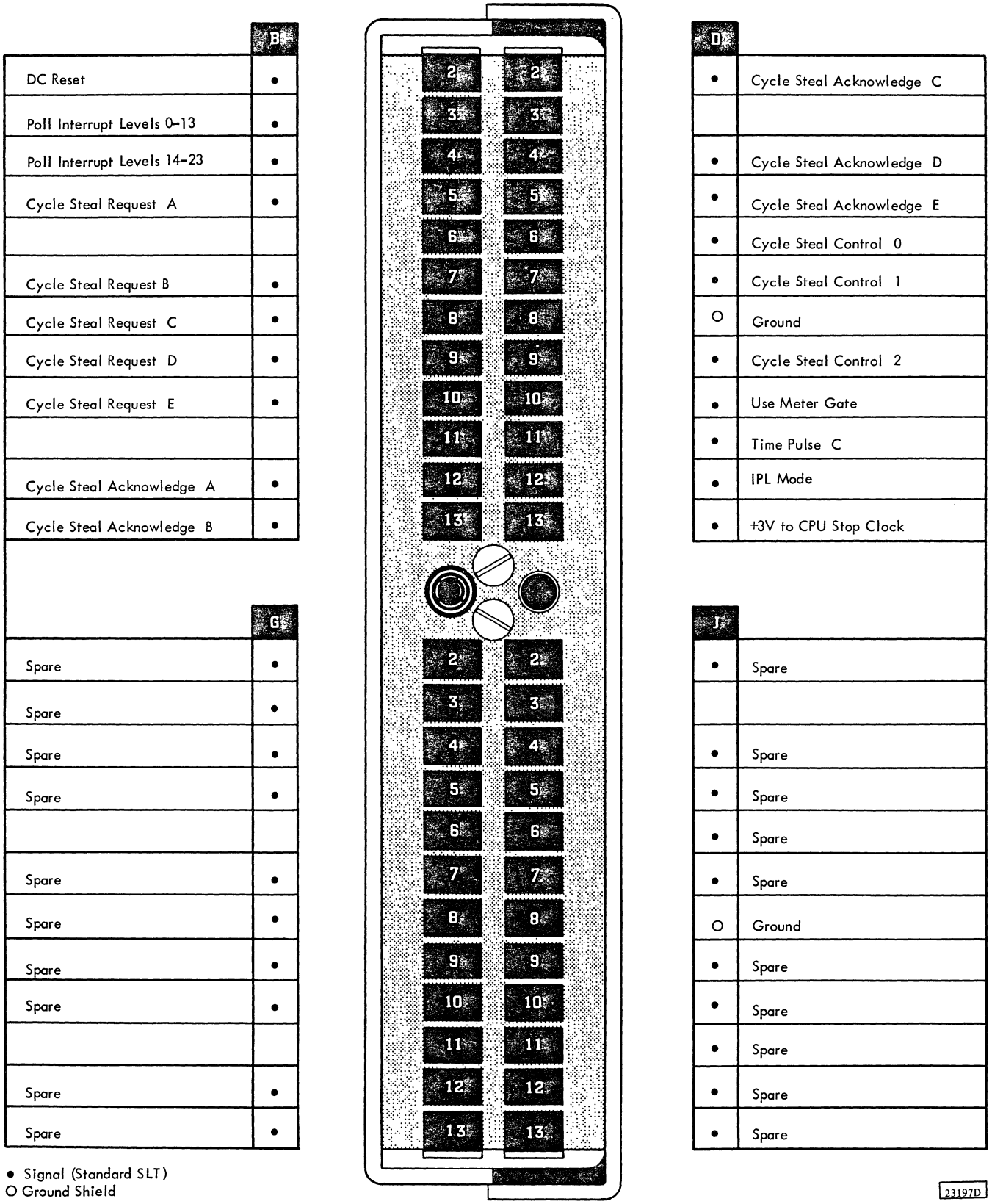


Figure 43. I/O Channel Interface Pin Assignments, Connector Q9 (I/O Channel 1)

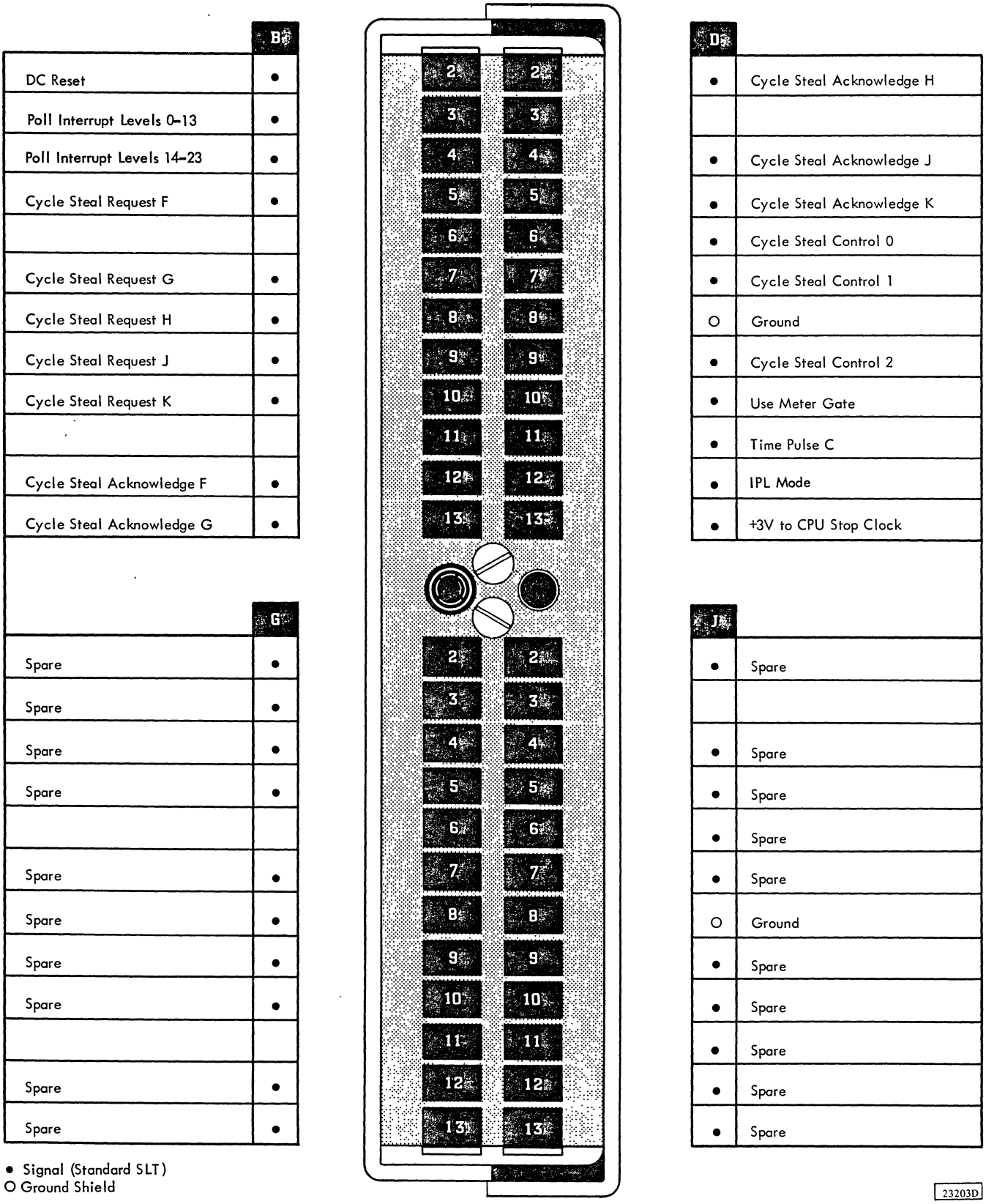


Figure 44. I/O Channel Interface Pin Assignments, Connector Q1 (I/O Channel 2)

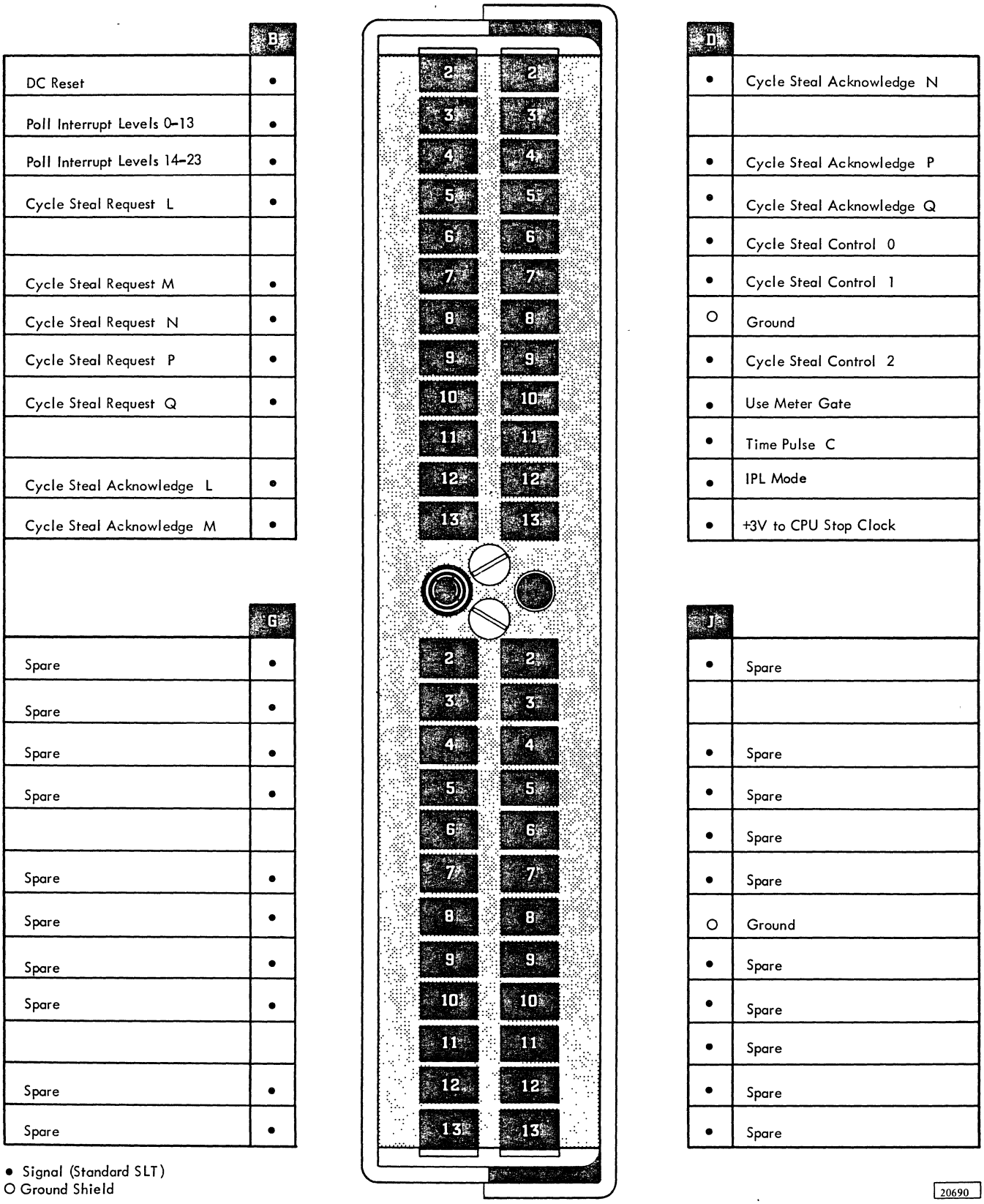


Figure 45. I/O Channel Interface Pin Assignments, Connector T7 (I/O Channel 3)

Input/Output Channel Interface

The I/O channel for the P-C consists of two sets of 60 signal and control lines (three sets with data channel expander). These lines connect logically to each I/O adapter in the 1800 system. Each adapter receives all 60 lines, uses the lines it requires, and exits all 60 lines to the next adapter in the series. The adapters are connected in parallel (Figure 46). Thus, no adapter can block the transmission of signals or controls to the next adapter.

The I/O channel exits the P-C via three pairs of serpent connectors at connector panel B. These exits are: I/O channel 1, I/O channel 2, and I/O channel 3. A single serpent connector contains the input and output data buses, time pulse (A and B), parity, parity error, storage protect, XIO data cycle, and XIO control cycle lines. The second I/O channel serpent connector also contains fixed lines. The reset, interrupt polling (A and B), cycle-steal control, use meter, time pulse C, and initial program load lines are the fixed lines in the second serpent connector. The five cycle-steal request and cycle-steal acknowledge lines are normally assigned by IBM for optimum system operation unless the customer has a special requirement (Figure 47).

Figure 46 shows the prescribed I/O cable routing sequence. In this diagram, an example of a cycle-steal-request line is shown connected from the channel control wired-logic terminals, through the internal adapters, and the mixer board (gate H), and to the external adapters. The lines not shown, follow the same route. However, they are jumpered straight through the mixer board.

I/O Channel Interface Lines

Out Bus

The out bus is a set of sixteen lines used to transmit information from the P-C to the devices. The interpretation of the information depends on the type of channel cycle. Bits are numbered 0 through 15 and correspond directly to the numbering of the P-C bits.

In Bus

The sixteen in bus lines are used to transfer data to the P-C. The type of information depends on the type of cycle in progress. The bits are numbered in the same manner as the out bus bits.

Parity Bits

These two lines transmit the parity bits for both input and output operations. The left-half parity bit line contains the odd parity for data bits 0–7 and the right-half parity line contains the odd parity for data bits 8–15. The utilization of the parity bits on the output bus is defined in the specifications for each adapter connecting to the output bus. The input bus must be provided with an odd parity bit for each half of the data word except during a sense function. The destination of the word on the input bus during an XIO instruction with a sense function is the accumulator. Since the accumulator has no parity bit, a check of the bus parity is not made.

CPU Stop Clock

This line stops the CPU T and X clocks and prevents them from stepping. The line is used by the I/O devices when a power off or other catastrophic condition exists in the device and it will effect processing.

Cycle-Steal Request

These lines are used by the device to request a cycle steal from the P-C. The request must be removed from the line by X4 time of the last desired cycle. The cycle-steal acknowledge (on the line which corresponds to the request) is the signal that the requested cycle-steal cycle is being performed.

Cycle-Steal Acknowledge

These signals indicate which data channel is active during the present storage cycle. This line must be activated by the device to indicate which CAR is to be loaded during the present XIO instruction. These lines are each activated by the active channel during cycle-steal cycles to indicate to the device that it has usage of the I/O channel during the current cycle.

Cycle-Steal Control

The three cycle-steal control lines indicate to the channel control the type of action that must occur during the present cycle-steal cycle. The lines are driven in the device and decoded by the channel control. The codes and functions are:

000 Write

This decode is used by the device to cause the selected CAR to be incremented and the contents of the B register to be gated to the channel data bus and the channel out bus.

001 Read

This decode is used by the device to cause the P–C to load the B register with the information on the in bus at X4 time. The core storage location addressed by the CAR is loaded with the contents of the B register.

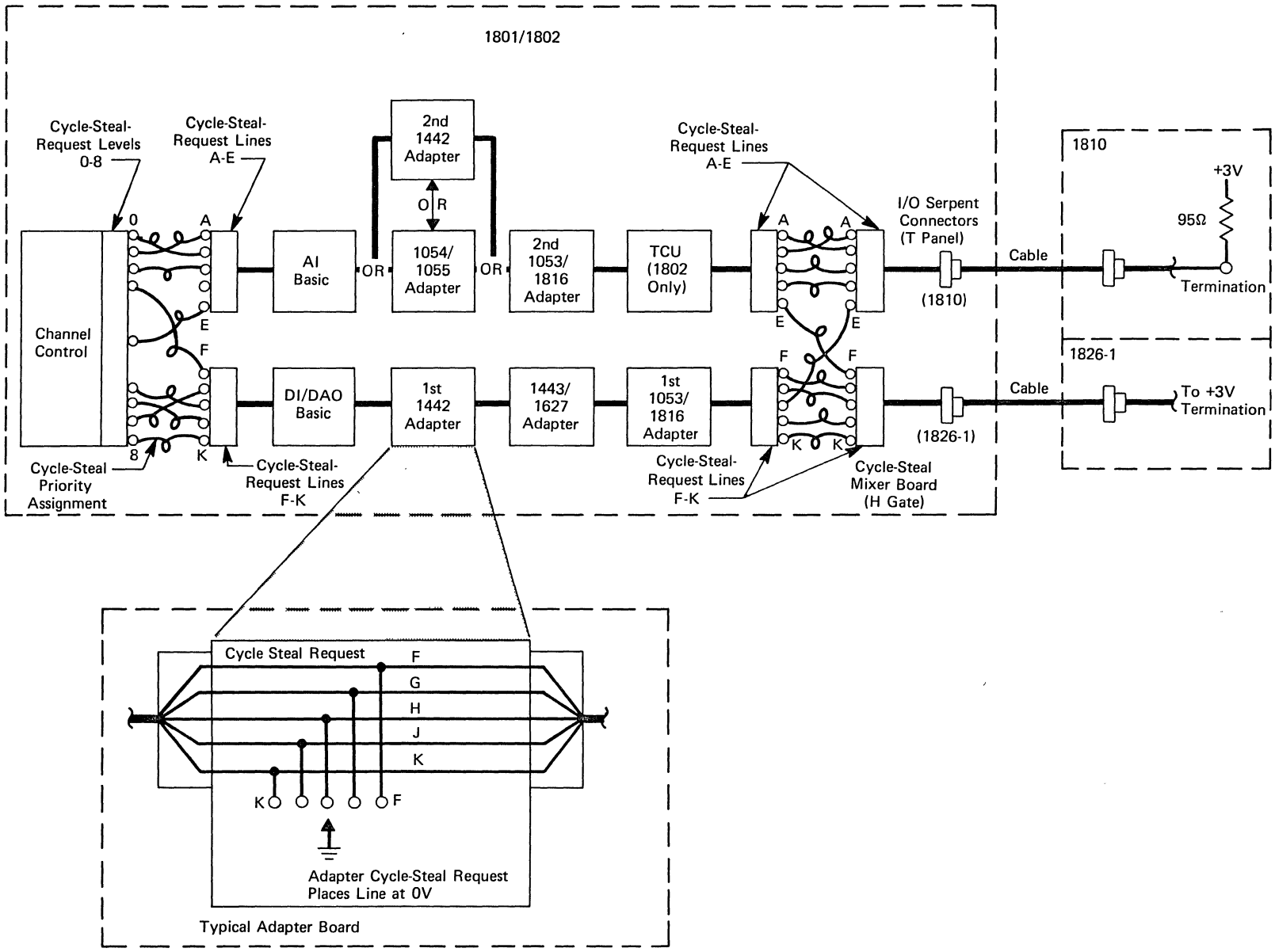


Figure 46. I/O Cable Routing, Cycle Steal Example (1801/1802 Without Data Channel Expander – 9 Data Channels) (1 of 2)

Note: Identical cable routing is provided for cycle-steal-acknowledge lines. Mixing of cycle-steal-acknowledge lines must match mixing of cycle-steal-request lines.

Cable routing for the other lines is identical but mixing is not provided.

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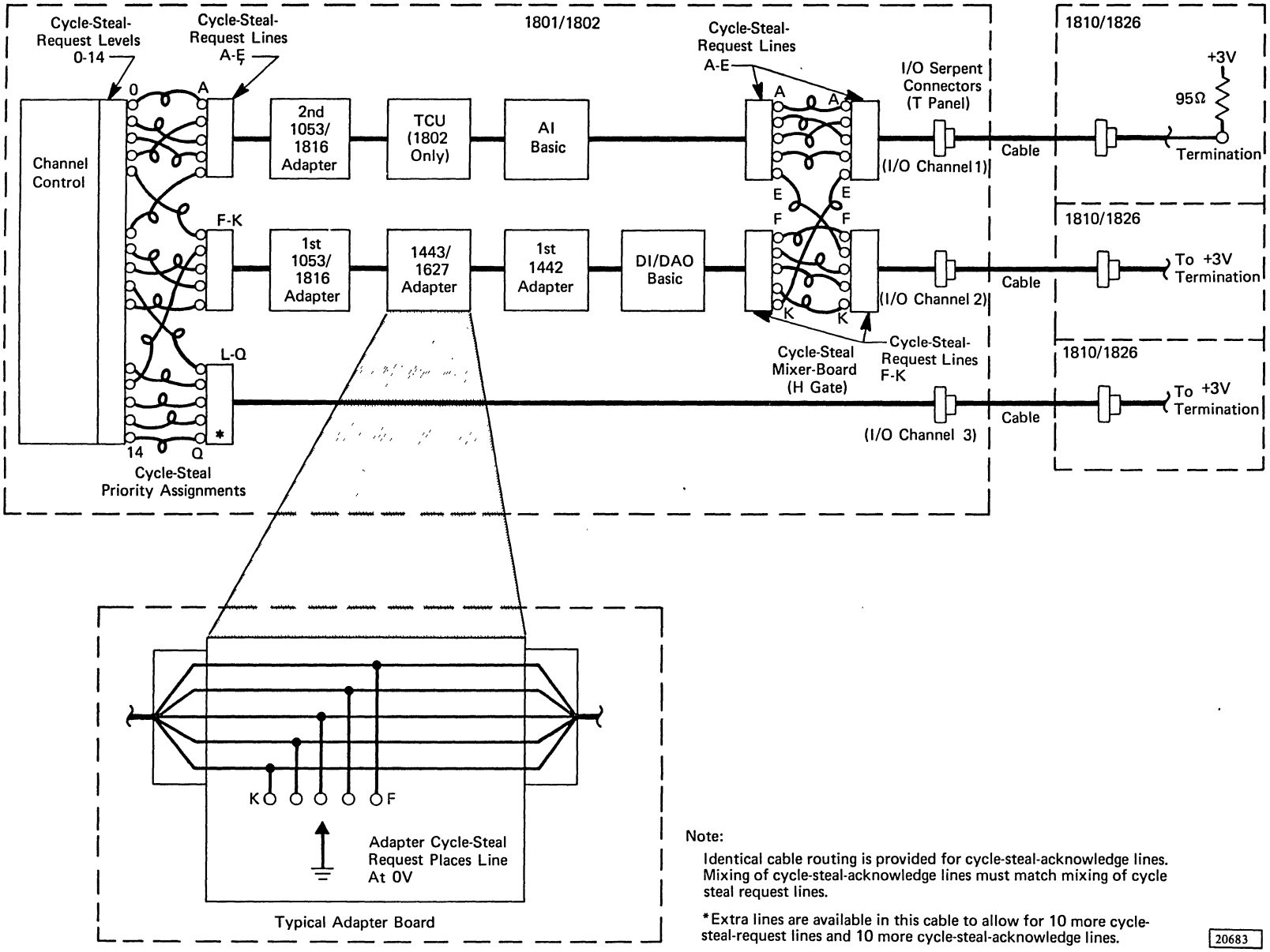

Note:

Identical cable routing is provided for cycle-steal-acknowledge lines. Mixing of cycle-steal-acknowledge lines must match mixing of cycle steal request lines.

*Extra lines are available in this cable to allow for 10 more cycle-steal-request lines and 10 more cycle-steal-acknowledge lines.

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Figure 46. I/O Cable Routing, Cycle-Steal Example (1801/1802 With Data Channel Expander – 15 Data Channels) (2 of 2)

010 Set Address Register

This decode from the device causes the word in the B register to be loaded into the CAR selected by the cycle steal acknowledge line.

011 In Bus to Address Register

This decode causes the data on the in bus to be gated to the channel data bus. The output of the B register is blocked. This allows a device to load its CAR. This operation must be done only during a cycle-steal operation. The storage location which was addressed during this operation is not changed.

101 Block Address Increment

This decode inhibits the incrementing of all CARs and allows multiple references to a single storage cell. This command is used to transfer packed data, or for comparison to check the correct loading of data to core.

110 CAR Check Request

This decode is activated by the device to cause the P-C to compare the contents of the core storage location addressed by CAR with the contents of CAR. If they do not compare a check signal is generated.

Interrupt Poll A and B

The interrupt levels are turned on by requests from the devices. The in bus is used to transmit the request to the P-C. Any storage cycle which is not a cycle-steal cycle, an XIO instruction, or a BSI instruction is utilized as an interrupt poll cycle.

This cycle is divided into two parts. These parts are 1 or 2 microseconds (μsec) in length (depending on the memory speed, 2, 2.25, or 4 μsec). The interrupt poll lines signal the device that it can request an interrupt by activating the corresponding bit on the in bus. The timing of the polling lines is controlled by the channel and must not be affected by the devices.

IPL Mode

This line is used during the initial program load sequence. The program load key on the operator's console activates this line. The P-C loads data into core per the contents of the I register and successive core locations when requested. Bit 15 on the in bus signals a request to store data and, if bit 14 is activated at least 250 nanoseconds (ns) before bit 15, the IPL line is deactivated. The P-C then executes the instruction at core location zero.

Metering

This line is used to indicate the status of the P-C to the I/O devices. At every T1 or X1 of a storage cycle which is not a time cycle, this line is activated. Four hundred (400) milliseconds (ms) after the last attempt to activate, the line is deactivated.

Time Pulse A, B, and C

These three lines are generated by the processor-controller (T) clock and the channel (X) clock. The lines are used by the I/O adapters to synchronize the device operations to the processor-controller operations. The timings of these three lines are such that any of the eight clock times can be decoded by the adapters.

Parity Error

The parity generated from the B register is utilized in the same manner by the XIO data cycle and the cycle-steal cycle. If the function is an XIO write or cycle-steal-write cycle, the generated parity from the left-half word and right-half word is transmitted with the data word on the output bus. The adapter regenerates parity bits for each of the half-words. The regenerated parity is compared against the parity received with the half words. If the parity conditions do not compare, an error indicator is set in the receiving adapter during the cycle in which the error occurred. When the indicator is off, it assures each device of correct data from the B register on each data transmission. When the indicator is on, it indicates a parity error within the data transmission cycle.

If the function is an XIO read or a cycle-steal-read cycle, the left-half odd parity and right-half odd parity is gated on the input bus with the data word. The left- and right-half parity bits are then exclusive ORed at the P-C and set in the B register. This data word with parity is then written into core storage. During the write to storage, parity is generated on the 16 bits in the B register and is compared to the parity written into core. If the parity does not compare, a parity error signal is sent out the I/O channel indicating to the adapter that a parity error was detected at the B register, and setting the adapter indicator. When off, this indicator assures each device that correct data was received by the B register for each data transmission. When set, it indicates a parity error occurred during the data transmission.

XIO Data Cycle

During this cycle, data is transferred between the device and the P-C as specified by the function code.

If the function is initialize write (101), or, if the function is initialize read (110), the address then specifies the starting address of a table in storage (an I/O block). This table consists of data words and control information.

If the function is control (100), and, if area specifies a group of units (e.g., magnetic tape), the modifier specifies the particular tape unit, and directs the selected unit to rewind or backspace, etc.

If the function is sense (011) or (111), the address field is ignored. Instead, a non-storage-use machine cycle is

Name of Line	Logic Line Title	Uses
Out Bus Bit 0 through 15	Out Bus Bit 0 through 15	Bus-Out - Used to transmit information (data, I/O device address, commands, control orders) from the channel to the control unit.
In Bus Bit 0 through 15	In Bus Bit 0 through 15	Bus-In - Used to transmit information (data, selected I/O device identification, status information, sense data and interrupt requests) from the control unit to the channel.
Parity Bit 0 to 7 Parity Bit 8 to 15	Parity Bit 0 to 7 Parity Bit 8 to 15	Bidirectional lines which are used to transmit parity data to and from the P-C.
Cycle Steal Request A through Q	CS Request A - Q	Used by I/O device adapter to request cycle-steal cycles for data transfer. Also assigns priority level. Maximum of 5 lines per I/O channel.
Cycle Steal Acknowledge A through Q	CS Acknowledge A - Q	Bidirectional - Activated by I/O device adapter during XIO initialize data cycle to load proper CAR. Activated by data channel controls on cycle-steal cycles to indicate when and which level is active. Maximum of 5 lines per I/O channel.
Cycle Steal Control 0, 1, 2	CS Control 0 through 2	Channel Controls - Activated by I/O device adapter. Condition of these lines determines action to be taken on a cycle-steal cycle (load CAR, gate in bus, gate out bus, increment CAR, block CAR increment, etc.)
Interrupt Poll A Interrupt Poll B	Poll Int Level 0 - 13 Poll Int Level 14 - 23	Selection Controls - Used for the scanning of attached I/O devices for interrupt requests.
Initial Program Mode	IPL Mode	Selection Controls - Used to cause the IPL device to load core storage.
Use Meter Gate	Use Meter Gate	Use Meter - Used for the conditioning of the elapsed time meter.
Time Pulse A Time Pulse B Time Pulse C	Time Pulse A Time Pulse B Time Pulse C	Timing Pulses - Used to synchronize device adapter operation with the P-C operation and for special sequences.
Parity Error, Storage Protect Violation	Parity Error Storage Protect Violation	Used to indicate invalid P-C operations.
XIO Control Cycle XIO Data Cycle	XIO Control Cycle XIO Data Cycle	Control - Used to indicate the portion of the XIO instruction in progress.
Reset	DC Reset	Control - Used to reset the adapters and I/O devices.

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Figure 47. Input/Output Interface Lines and Uses

taken. During this time, the selected I/O device or interrupt level places its status word in the accumulator.

If the function is write (001) or if the function is read (010), the address then specifies storage location of the data word.

If the function is CE mode (000), the adapter specified by area is set in the mode using modifier 15 and is reset using no modifier 15. Address is not used.

XIO Control Cycle

This cycle transmits area and function information to all devices on the channel. The function codes are listed in a following subparagraph.

Area: This 5-bit field specifies a unique segment of I/O which may be a single device (1442 card read-punch, 1443 printer, etc.) or a group of several units (magnetic tape drives, serial I/O units, contact sense units, etc.) Figure 48 lists the area codes for the various I/O devices.

I/O Device	Area Code
Console	00000
1st 1816 and 1053s (first 4)	00001
2nd 1816 and 1053s (second 4)	01111
1st 1442 Card Read Punch	00010
2nd 1442 Card Read Punch	10001
1054 and 1055 Paper Tape	00011
1st 1810 Disk Storage Drive	00100
1627 Plotter	00101
1443 Printer	00110
Reserved by IBM	00111
2nd 1810 Disk Storage Drive	01000
3rd 1810 Disk Storage Drive	01001
Analog Input	01010
Analog Input Expander	10000
Digital Input (Pulse Counter and Digital Inputs)	01011
Digital and Analog Output (DO, ECO, RO, AO)	01100
System/360 Adapter	01101
2401 to 2402 Magnetic Tape	01110
Selector Channel	10010
1st Communication Adapter	10101
2nd Communication Adapter	10110
3rd Communication Adapter	10111
4th Communication Adapter	10100
1st 2790	00111
2nd 2790	10011

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Figure 48. I/O Device Area Codes

Area 00000 is used to address devices internal to the system. When area 00000 is specified, the console status, interrupt, mask register, or interval timer may be selected.

Function: The primary I/O functions are specified by the 3-bit function code:

000 Sets I/O units in or out of CE mode.

001 Write
This code transfers a single word from storage to an I/O device. The address of the storage location is provided by the address field of the IOCC.

010 Read
This code transfers a single word from an I/O device to storage. The address of the storage location is provided by the address field of the IOCC.

011 Sense Interrupt Level
This code directs the I/O device requesting interrupt recognition, on the interrupt level in progress, to make the device interrupt status available.

100 Control
This code causes the selected device to interpret the modifier and/or the address field as a specific control action.

101 Initialize Write
This code initiates a write operation on a device or unit which will subsequently make data transfers from storage using data channel cycle sealing.

110 Initialize Read
This code initiates a read operation from a device or unit which will subsequently make data transfers to storage using data channel cycle stealing.

111 Sense Device
This code causes the selected device to make its current status available in the accumulator as the device status word.

Storage Protect Violation

During an XIO read instruction or a cycle-steal-request read, while the data cycle takes place, the word contained in storage is checked for the presence or absence of a storage protection bit. If the bit is absent, execution proceeds without change and the read information is set into the B register where it is written into storage. If the protect bit is present, the read information is not set into the B register, and the storage protection violation line on the I/O channel device is conditioned. This signal is detected by the adapter which caused the storage violation and it must turn on an indicator.

Reset: This signal is present as long as the reset key on the console is pressed, unless the P-C is in run mode. This line is also active during the power on sequence.

Signal Cable Termination

All I/O channel lines must be terminated. If no external adapters (outside the 1801/1802) are installed, the I/O channel signal cables are terminated at the mixer panel (gate H). If external adapters are installed, the I/O channel signal cables are terminated at the last active adapter board on the I/O channel.

The resistor terminator cards supply the +3V "off" level, through a 95Ω resistor, for each line in the I/O channel. The active level of a line is represented by 0V, the I/O channel must be continuous from the channel origin to the terminator cards. If the terminator cards are installed in an 1810 or an 1826, power must be on at that unit to supply the + 3V terminating voltage. The IBM part number for the terminator card is 5800320 (5803172).

I/O Channel Timing

Timings for I/O channel operations are shown in Figures 49, 50, and 51.

ELECTRICAL SPECIFICATIONS

Physical Considerations

The 1800 system signal lines between the P-C and the various adapters consist of flat transmission cables, printed wire, coaxial cables, twisted pair, or any combination of the four provided that the maximum resistance and delay time limitations are not exceeded. Transmission lines in the 1800 system can be driven by single or multiple drivers and can feed single or multiple receivers. All transmission lines must terminate with their characteristic impedance.

Single Driver and Receiver

When a transmission line is supplied by a single driver and feeds a single receiver, the driver and receiver must be located at the extreme ends of the lines. Drivers and receivers can be located beyond the line terminator, provided that the distance between the terminator and the end-of-line driver or receiver is less than 6 inches.

Multiple Drivers and Receivers

The I/O channel transmission line in the 1800 system can supply a maximum of eight receivers. Drivers driving onto the transmission line must be unloaded, as the I/O channel transmission line is terminated with the proper impedance at each end.

Multiple receivers on a line should not be less than 3 feet apart. However, no minimum spacing requirements have been set for the distance between drivers, between an end-of-line terminator and a driver, or between an end-of-line terminator and a receiver. If a line with multiple drivers and/or receivers is not terminated at the extreme end, the terminator must be within 6 inches of the end-of-line driver or receiver.

General Electrical Considerations

Current Flow

The direction of current flow (conventional) is minus if it is flowing into a component or plus if flowing out of it.

Voltage Levels

The positive level on a line denotes a logical zero and the more negative level denotes a logical one. See *Specific Electrical Requirements – Receiver, Driver.*

Impedance

Lines must have a characteristic impedance of 95 ohms, plus or minus 10 ohms. Lines must terminate at each end (except as noted above) with their characteristic impedance.

Noise

The maximum noise coupled onto any signal line within a cable due to any combination of changes external to that line must not exceed 300 millivolts.

Fault Conditions

The signal line may be grounded with no damage to drivers, receivers, or terminators.

Loss of power at either end does not cause any damage.

Loss of power at any terminator will cause stopping of the CPU clocks.

Loss of power at both terminators results in generation of logical ones, irrespective of information input.

Line operation is unaffected where power is off in any device adapter, except the terminating adapter.

Specific Electrical Requirements

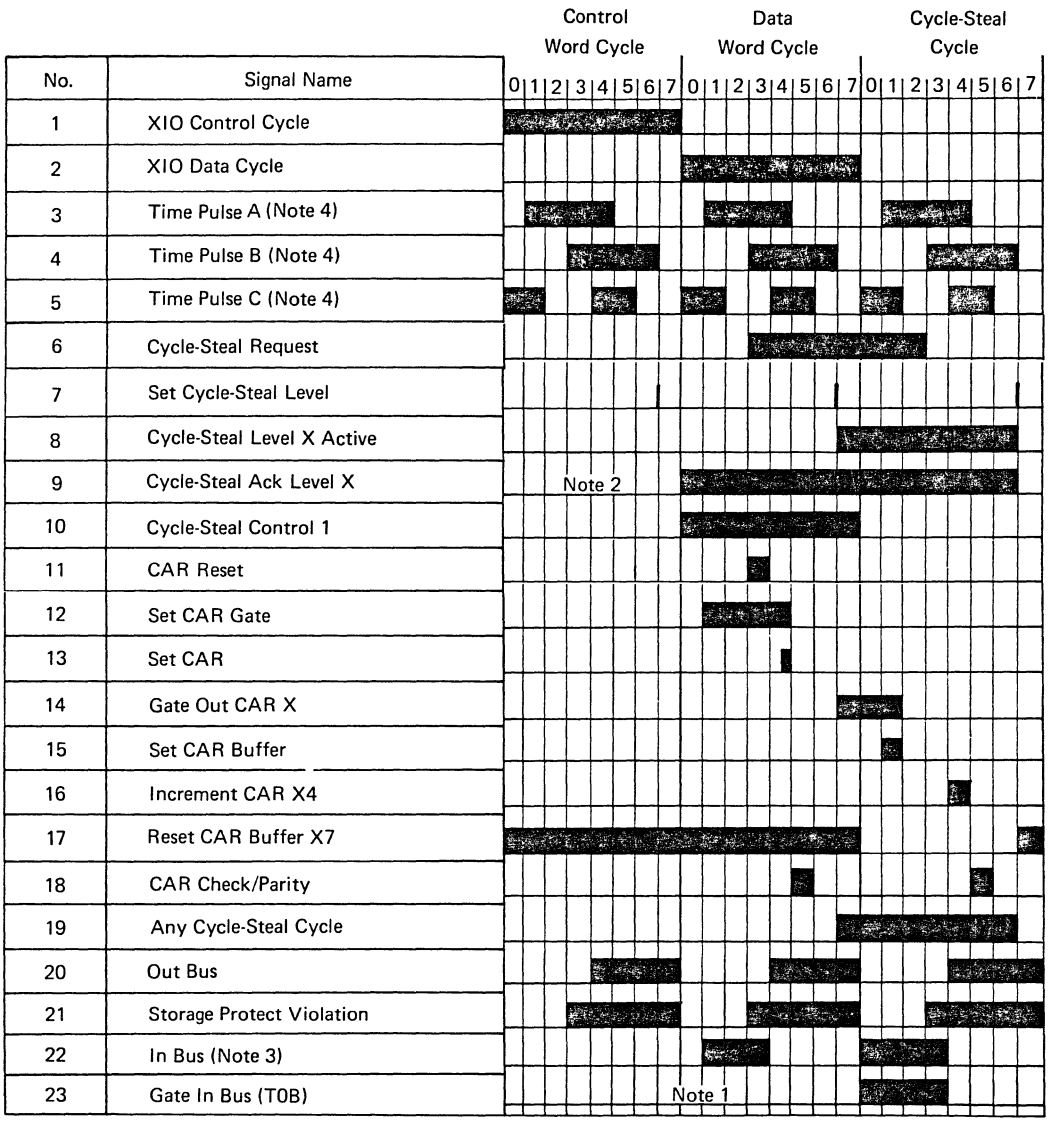
Receiver

The output must be interpreted as a logical one for the more negative line signal, and as a logical zero for either a plus line signal or an open input.

Receivers (Figure 52) must not require a switching level more positive than +2.52 volts for a logical zero or more negative than +1.42 volts for a logical one.

Receivers must not be damaged by a most positive direct current up level of 3.4 volts or most negative direct current down level of 0 volts.

Receiver input must not require positive current greater than 0.35 milliampere at the most positive up level of 3.4 V. Positive current required must not be greater than that taken by a 15.4K ohm resistor network connected to a 6.24 -V supply. Input impedance of each receiver should be made as high as possible, but never lower than 4.0K ohms.



No.	Signal Name
1	XIO Control Cycle
2	XIO Data Cycle
3	Time Pulse A (Note 4)
4	Time Pulse B (Note 4)
5	Time Pulse C (Note 4)
6	Cycle-Steal Request
7	Set Cycle-Steal Level
8	Cycle-Steal Level X Active
9	Cycle-Steal Ack Level X
10	Cycle-Steal Control 1
11	CAR Reset
12	Set CAR Gate
13	Set CAR
14	Gate Out CAR X
15	Set CAR Buffer
16	Increment CAR X4
17	Reset CAR Buffer X7
18	CAR Check/Parity
19	Any Cycle-Steal Cycle
20	Out Bus
21	Storage Protect Violation
22	In Bus (Note 3)
23	Gate In Bus (T0B)

Items 1-19 show timing sequences for an XIO initialize read or write where the device adapter requests a cycle-steal cycle during the XIO Data Cycle.

NOTES:

1. This line active only during in bus operations.
2. C.S. Ack forced by device adapter during data word cycle; by data channel control during CS cycle. This signal is undefined from 6B to 7B time.
3. Minimum required width at CPU. Optimum width is 0-5 time inclusive.
4. These lines active whenever T or X clocks are at the indicated times. (Not dependent on run mode.)

All Rise and Fall Times are Subject to ±100 nsec Skew.

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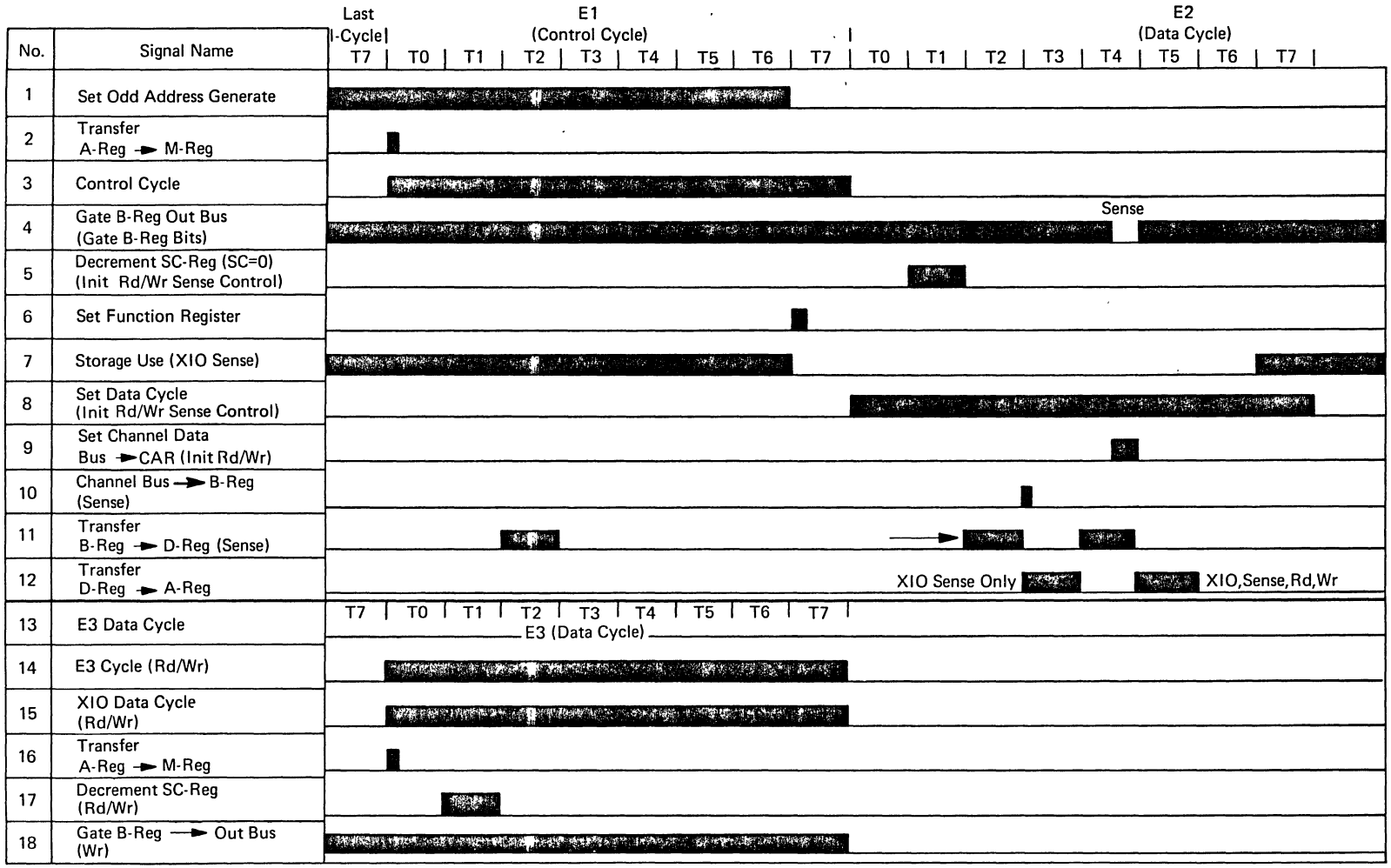
Figure 49. I/O Channel Control Timing

Figure 50. Execute I/O (XIO) Timing



NOTES:

Timings are shown to give relationship to machine cycles and not to a specific XIO operation.

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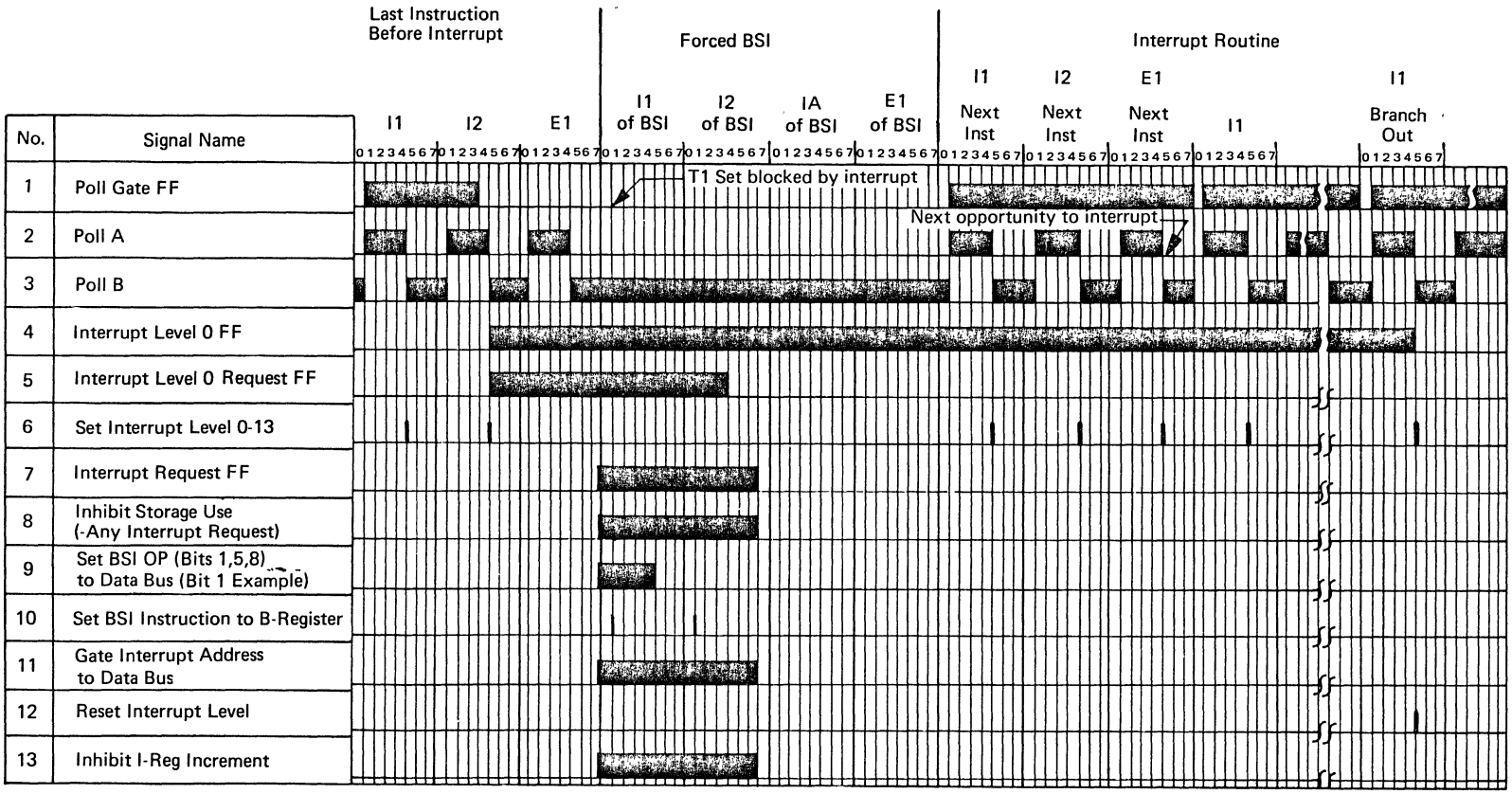

No.	Signal Name
1	Poll Gate FF
2	Poll A
3	Poll B
4	Interrupt Level 0 FF
5	Interrupt Level 0 Request FF
6	Set Interrupt Level 0-13
7	Interrupt Request FF
8	Inhibit Storage Use (-Any Interrupt Request)
9	Set BSI OP (Bits 1,5,8) to Data Bus (Bit 1 Example)
10	Set BSI Instruction to B-Register
11	Gate Interrupt Address to Data Bus
12	Reset Interrupt Level
13	Inhibit I-Reg Increment

NOTES:

1. Example shows interrupt (0) occuring during a normal instruction execution. No wait, XIO, or CS occur during this example.
2. IA and E1 of forced BSI are the same as in normal BSI cycles.
3. During a wait instruction, oscillator pulses cause polling to continue with the poll A and poll B pulses longer in duration.
4. Poll A may occur either T1-T4 or T5-T7, T0 and poll B may occur at either T5-T7, T0 or T1-T4.
5. Polling gate FF set at I1T1 (except interrupt) and reset at X1 cycle-steal cycle T4 XIO or BSI instruction to end OP all other instructions.

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Figure 51. Interrupt Request Timing

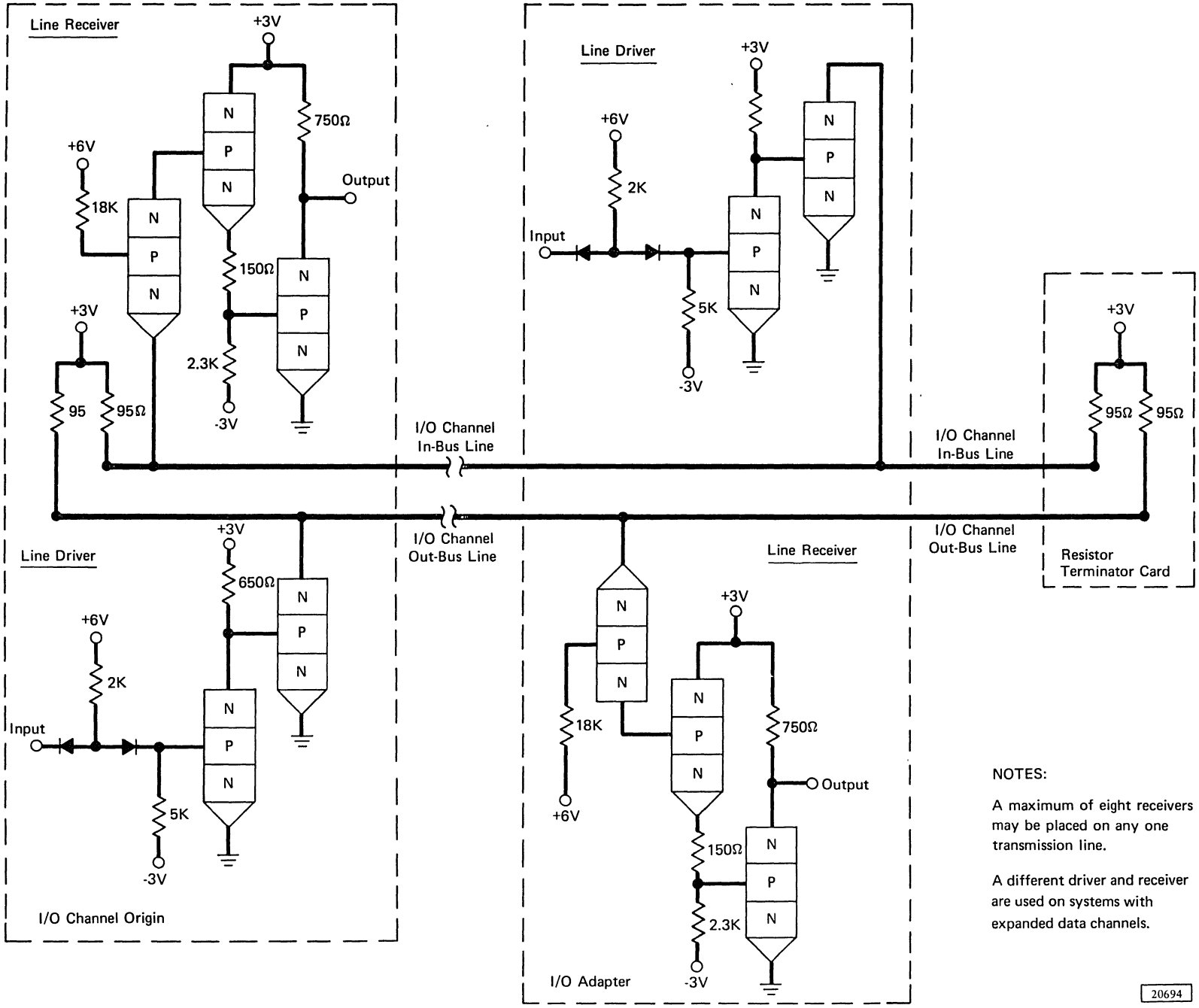

Figure 52. I/O Channel Line Drivers and Receivers

Terminator

The terminator is viewed as a two-terminal network consisting of resistors and power supplies, and must meet the following requirements.

The terminal connected to the signal line must present an open-circuit voltage between +2.88 volts and +3.4 volts. Impedance between the terminals must not be less than 90 ohms nor greater than 105 ohms. Current is measured at the terminal that is connected to the cable and must not be greater than 22.8 milliamperes flowing out of the component at +1.12 volts. One terminal of the terminator is connected to ground, the other to the signal line.

Driver

To transmit a logical zero, voltage source drivers (Figure 52) must pull less than 100 microamperes from the line.

To transmit a logical one, the driver conducts. The driver must be capable of accepting 56.0 milliamperes from a 0.33 V source when in the conducting state.

If the driver output is open-circuited when conducting, the voltage must not fall below 0.00 V.

Cable

Cable length is limited by a maximum cable resistance of 26 ohms, including contact resistance. A maximum of 0.25 ohm contact resistance per control unit or channel is allowed, including connections to and from the external cables. The cable may consist of any combination of flat cable, coaxial cable, and printed wire within the above limitation. The maximum allowable internal cable resistance offered by any control unit or channel on the interface is 1.5 ohms. The measurement of this value is made between the external connector pins.

The characteristic impedance ranges from 82 to 102 ohms.

Connectors

The maximum coupled noise due to all connectors in each control unit, including external connectors, is 250 millivolts.

Alterations and Attachments

If lessees are considering the special application of IBM leased machines in conjunction with associated equipment, they should review the Alterations and Attachments clause of the Agreement for IBM Machine Service. Under this clause, IBM must receive written notice prior to any alterations or attachments to the machines or units. If the alteration or attachment interferes with the normal operation or maintenance of any of the IBM machines or units or substantially increases the cost of maintenance, the customer must remove the alteration or attachment and restore the machines and units to their normal condition upon notice from IBM.

The customer is responsible for the design, procurement, installation, repair, and service of the alteration or attachment. In the event that an alteration or attachment causes interference with the installation of an engineering change which is considered necessary to effect an improvement in the operation or maintenance of an IBM machine, the customer will be required to eliminate such interference.

When a lease is terminated, the customer is required to remove all alterations or attachments and restore the machine to its normal condition before its return to IBM.

Any liability, personal or otherwise, arising from the alteration or attachment or its effect on IBM equipment, rests with the customer.

IBM cannot treat information pertaining to alterations and attachments as secret or confidential.

The rights arising out of the alterations or attachments are to be measured and defined by the patent protection that may be given under the applicable patent laws or under valid patents issued upon such alterations or attachments. IBM is to have all the rights that the public would have with respect to the alterations or attachments.

IBM service or maintenance of alterations or attachments does not constitute an approval of the alteration or attachment, or a waiver of the right of IBM to discontinue such service.

Power Supplies and Control

The 1800 system operates from one three-phase line cord (Figure 53) with inputs of 208/230 volts at 60 Hz or 195/220/235/308/408 volts at 50 Hz.

Primary power enters the 1801 or 1802 through a line filter and a 50-amp mainline power circuit breaker (CB1) and is sequenced to all system units except the 1053 printer and the 1816 printer-keyboard. The 1053 and 1816 have their own power cords.

DC power supplies (Figures 54 and 55) provide system service voltages and special voltages for core storage and process I/O features. Interlocks are provided for critical voltages.

Power-On Sequence

Three-phase primary power is supplied through CB1 to contactor K1 which is controlled by the emergency power off (EPO) switch, and to transformer T1 which provides the 24V ac sequencing voltage. The 24V ac sequencing voltage is supplied to the 1828 (for the 1856 units) through isolation transformer T6.

From K1, primary power is distributed to contactors K2, K3, K4, and to transformer T3. Transformer T3 supplies 115V ac to convenience outlets in the 1801 or 1802, 1810, 1826, 1828, 1442, and 2401 or 2402.

Pressing the ON button turns on the power on lamp and starts the power-on sequence:

1. Supply primary power via K3 to CB2 (1826) and CB3 (1828).
2. Supply primary power via K2 to
   (a) gate blowers and power supply fans in the processor-controller;
   (b) 1442, 1443, 1810, and CB4 (2401 or 2402);
   (c) transformer T2: 115V ac power to 1054 and 1055 (via switches on P-C power tailgate), 1627, and gate fans in the 1442;
   (d) transformer T4; 7.5-Vac lamp voltage to P-C console and 1442;
   (e) transformer T7; power-failure-protect circuit;
   (f) power supplies, 1, 2, 3, 6, 7, 8, 9, 10, 11, 12, 13, and 15 in the processor-controller
3. When voltages are available at power supplies 1, 2, 3, 7, 9, 10, 12, 13 and 15, supply primary power via K4 to power supplies 5, 14, 16, 17, and 18 in the processor-controller.

The power-on reset line is held at 0V (active level) during the power-on and power-off sequences. The power-on reset ends approximately 1.7 seconds after pressing the ON button, at which time the Ready lamp turns on to indicate that dc voltages are present.

Resistors are employed in the output circuits of ADC power supplies 8(+30V), 11(-30V), and 14(+12V) to limit the initial surge current. When the ready condition is reached, the current limiting resistors are shunted by relay RY19 points.

Power-Off Sequence

The OFF push button is used to power-down the 1800 system. Pressing the OFF button drops all power in the system with the exception of the 115V ac convenience outlets and the 24V ac sequencing voltage.

The use of the OFF push button ensures that power supplies will be cycled down in the following order:

1. Power supply 18 (+48V magnet voltage).
2. Power supply 14 (+12V ADC), and power supplies 5, 16, and 17 (core storage).
3. All other power supplies.

Power supplies in items 1 and 2 are controlled by K4, which is the last contactor to pick and the first to drop. The +48V is removed before other voltages by opening the output of power supply 18 with relay points. Power supplies in item 3 are controlled by K2 and loss of any of these voltages (except supply 6, 8, or 11) will immediately drop K4.

Loss of dc voltage from any P-C power supply, except supplies 6, 8, 11, 14, and 18, will drop system power in the same manner as operating the OFF switch. Loss of voltage from supply 6, 8, 11, 14, or 18 will not drop system power and will be indicated only by program detection of failure or by visual observation.

Power supplies 8 and 11 (+30V and -30V) are interlocked so that loss of either supply will drop the output of both these supplies and will also drop supply 14 (+12V).

If loss of voltage is caused by tripping the over-current circuit breaker in any MPS (medium power standard) power supply, the condition will be indicated by turning on the DC CKT BKR TRIP lamp on the I/O monitor interface panel.

Power Failure Protect Circuit

This circuit ensures proper cycling down of the power supplies after loss of primary power. The power-failure-protect circuit operates from a three-phase transformer (T7) on the load side of contactor K2. The circuit senses the loss of power in any one of the three phases and responds by generating a +3V signal.

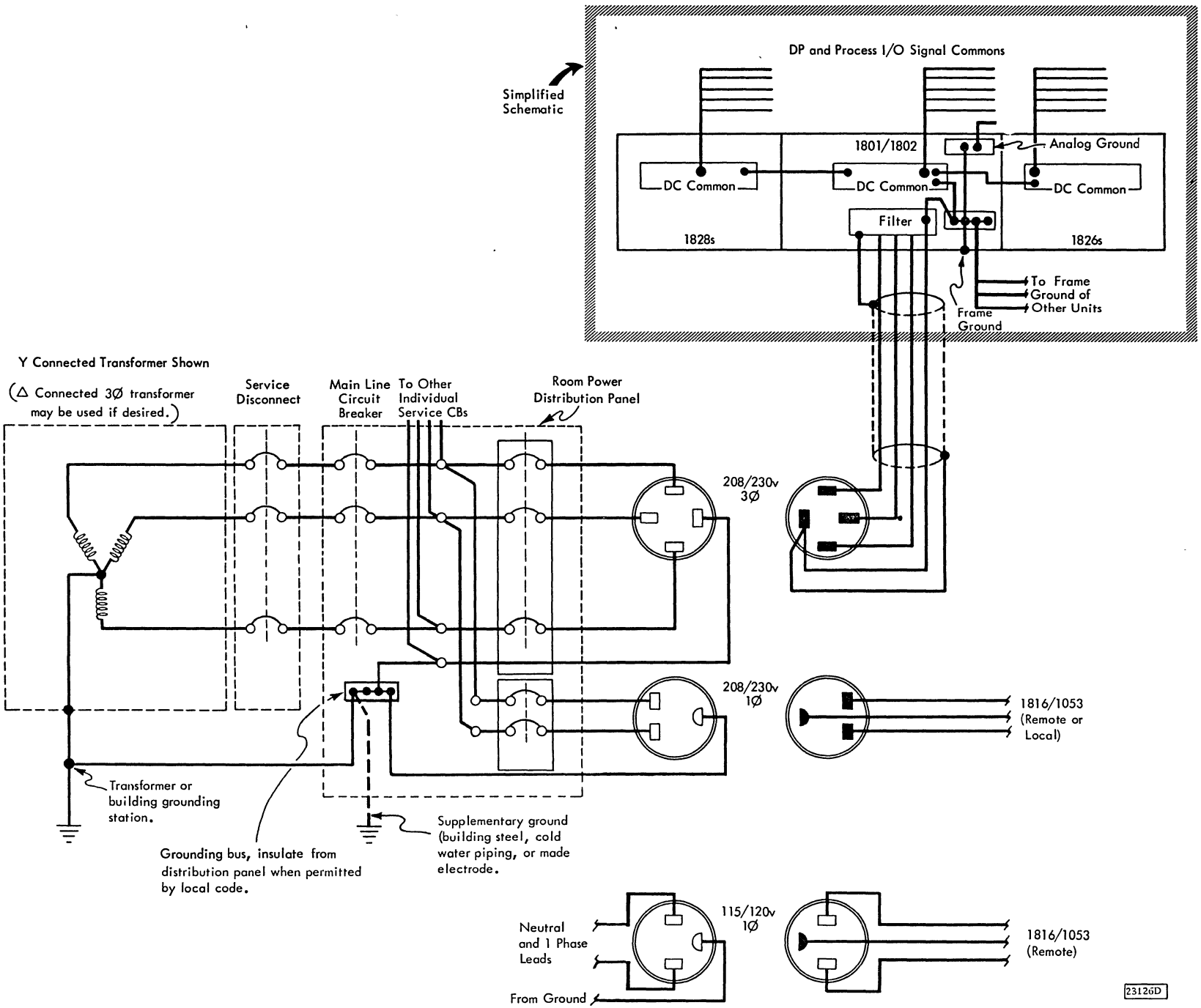

Figure 53. 1800 System Power Distribution and Grounding (60 Hz) (Part 1 of 2)

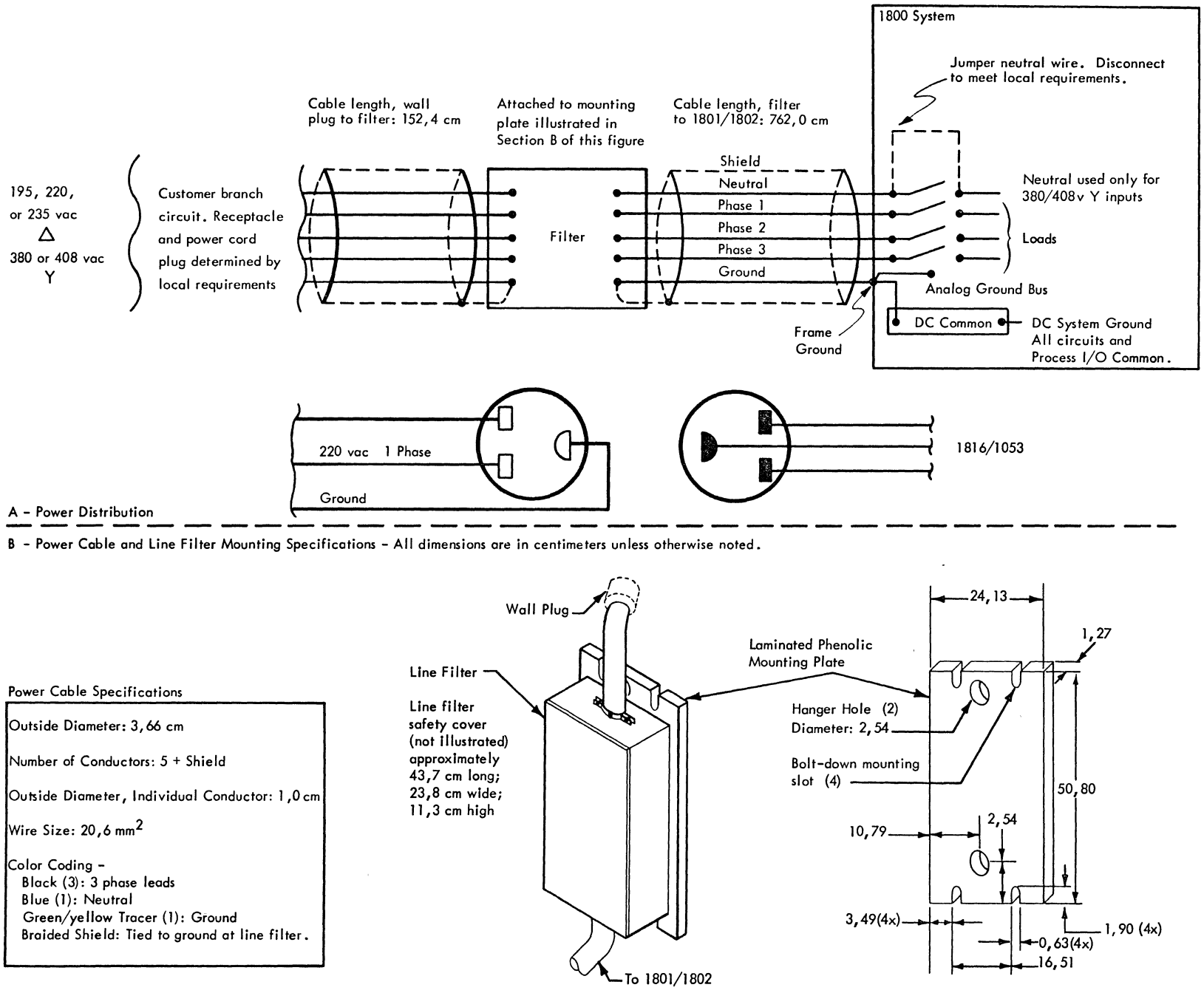

Figure 53. 1800 System Power Distribution and Grounding (50 Hz) (Part 2 of 2)

The signal triggers a circuit that drops relay RY1 to initiate the power-off sequence. The +3V signal also gives an immediate-stop signal to reset the system at T7/X7.

The processor-controller remains in a power-on state for power drops to the system up to one cycle in duration (15 to 17 ms). The power failure sequencing enables the processor to complete the core storage cycle that is in progress at the time of failure.

Emergency Power Off (EPO)

This switch is for emergency use only. If pulled off, all electrical power (except 24V ac sequencing voltage) is immediately removed from all system units except the 1053 printer and 1816 printer-keyboard, which have their own power cords. Pulling the emergency power off switch drops contactor K1 and removes voltage from the power supply sense relays that are holding relay 1 energized.

Power Supply Number	Rating	Power Supply Number	Rating
1	+6V @ 18A	10	+3V @ 16A
2	+3V @ 16A	11	-30V @ 2A
3	+6V @ 18A	12	+6V @ 18A
4	0-3V, Power Failure Protect	13	+6V @ 18A
		14	+12V @ 2.5A
5	+12V @ 5A	15	-3V @ 16A
6	1801 - +36V @ 3A	16	15V 2 μsec Memory
	1802 - -12V @ 2.5A	17	-9V to -12V 2 μsec Memory
7	+3V @ 16A	18	+48V @ 6A
8	+30V @ 2A		
9	+3V @ 12A		

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Figure 54. Power Supplies and Ratings

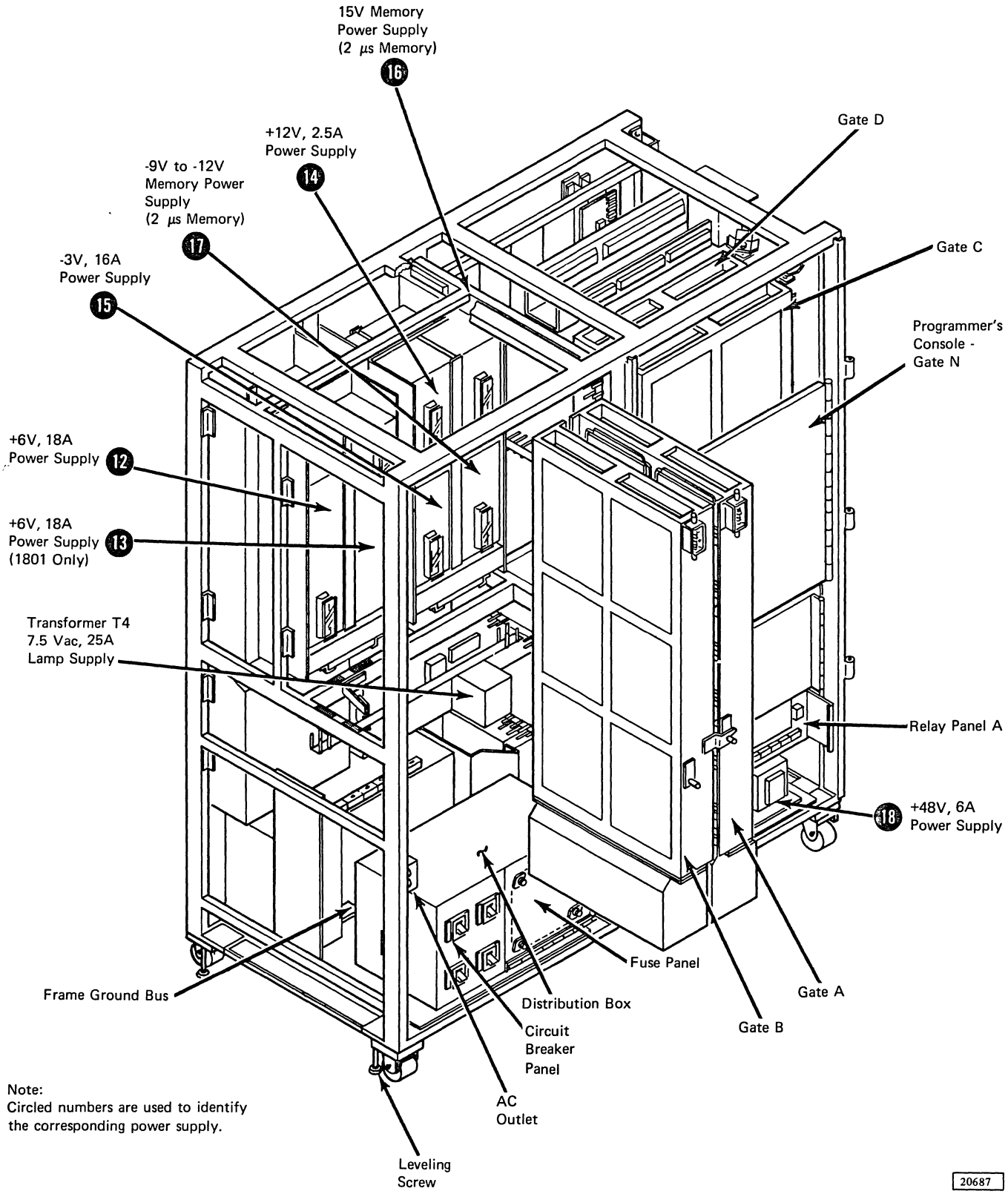
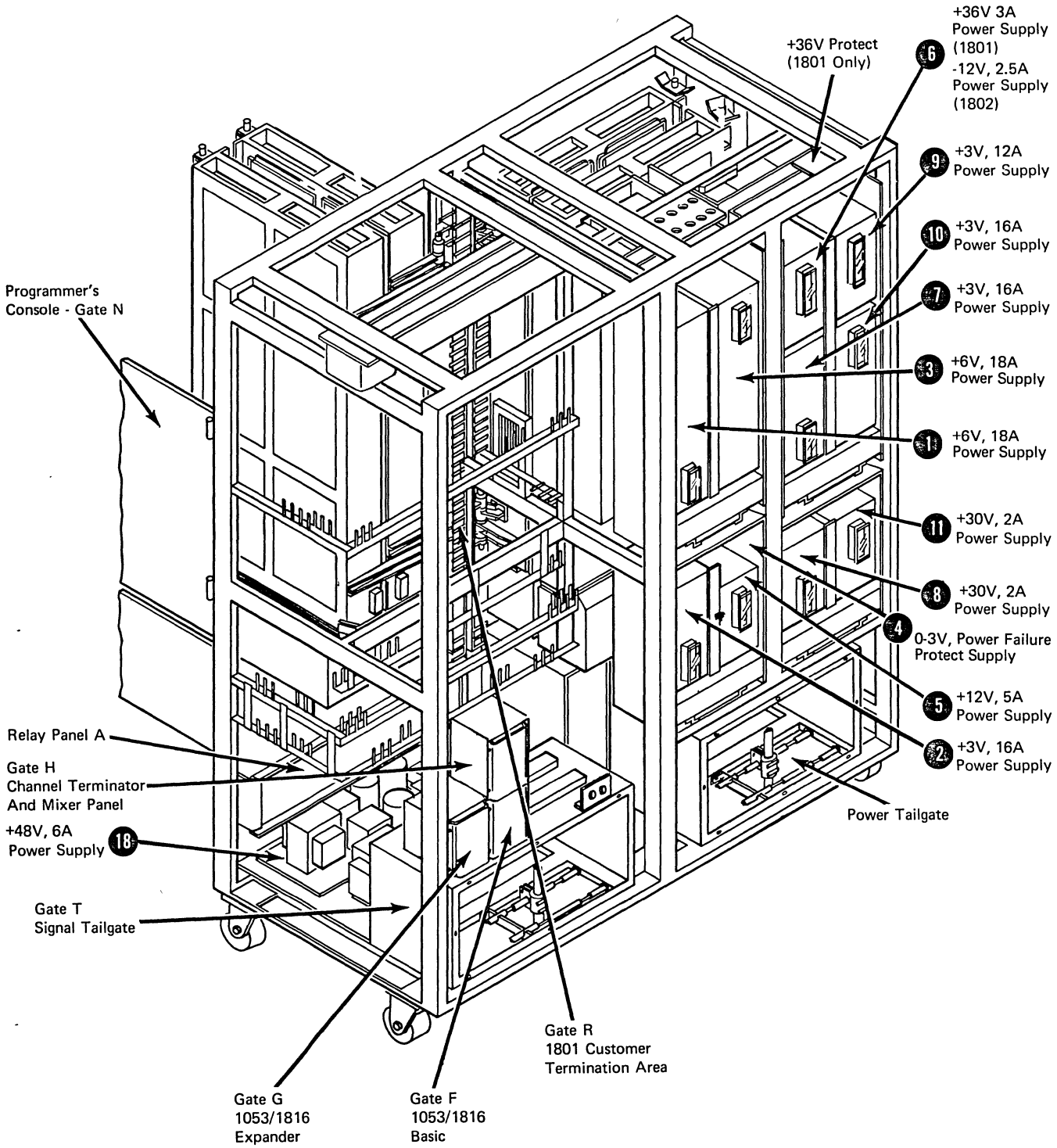


Figure 55. 1801/1802 Processor Controller (Front) (Part 1 of 2)



Note:
Circled numbers are used to identify the corresponding power supply.

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Figure 55. 1801/1802 Processor-Controller (Rear) (Part 2 of 2)

Appendix B. I/O Channel, Simplified Data Channel (Cycle — Stealing) Operation

DATA CHANNEL OPERATIONS UTILIZING CYCLE-STEAL

Objectives: The XIO operations of initialize read or initialize write are used to set up the data channel controls. Data channel controls supervise the data flow to or from multiple I/O units which must time share a single In or Out bus.

Each I O unit has a program assigned data table area in main storage, and an assigned Channel Address Register (CAR) which addresses core storage during cycle-steal cycles.

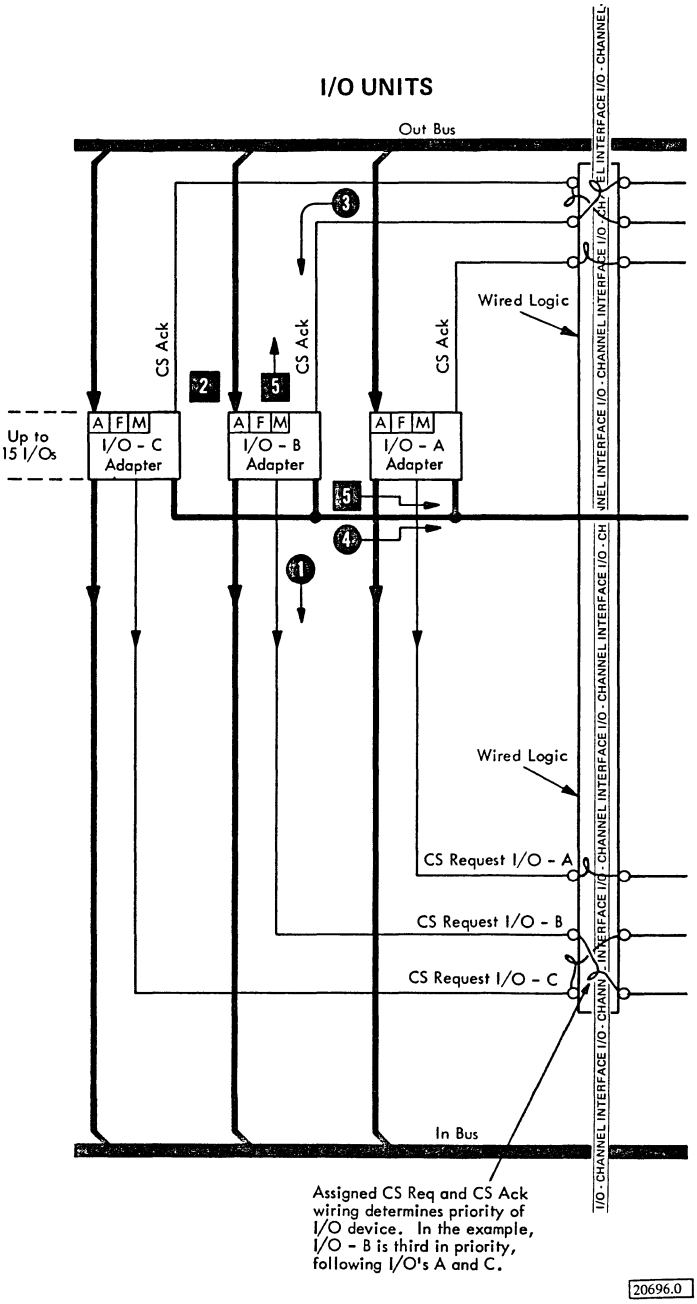
The data channel operation is divided into two parts:

INITIALIZATION The I/O unit is selected by data contained in a 16-bit control word (IOCC) which is transferred via the Out Bus and accepted by the designated I/O unit. Once selected, the I/O operation (read a card, for example) can start. During the following cycle the Channel Address Register assigned to the I/O unit is set with the address in storage of the first data word to be addressed when the I/O unit needs access to storage. The data channel control circuits wait for a cycle steal request signal from the I/O unit. See A

CYCLE STEAL During the main-line program, the T-clock runs. When a cycle steal occurs, the T-clock stops at the end of the cycle in progress. All P-C registers continue to hold the values set during the main-line program. The X-clock runs during one or more cycle steals to time the channel operation. Following the cycle steal, the T-clock restarts and the main-line program resumes.

The following sequence takes place:

- Set Up Cycle Steal
  When the I/O unit needs data or needs to send data, a cycle steal request signal to the channel controls, delays execution of the main-line program. Provided no higher priority cycle steal takes precedence, the requested cycle steal operation occurs.
- Transfer Data
  Storage is addressed by the previously set contents of the assigned CAR. A single word is transferred (via the In or Out Bus) to or from the I/O unit.
- Increment Address in CAR
  The address in the assigned CAR is set to CAB to core storage. CAR is then incremented by one preparing it for the next cycle steal operation.
- Resume P-C Program
  Unless cycle steal request is waiting, the T-clock restarts and the main-line program resumes. See B

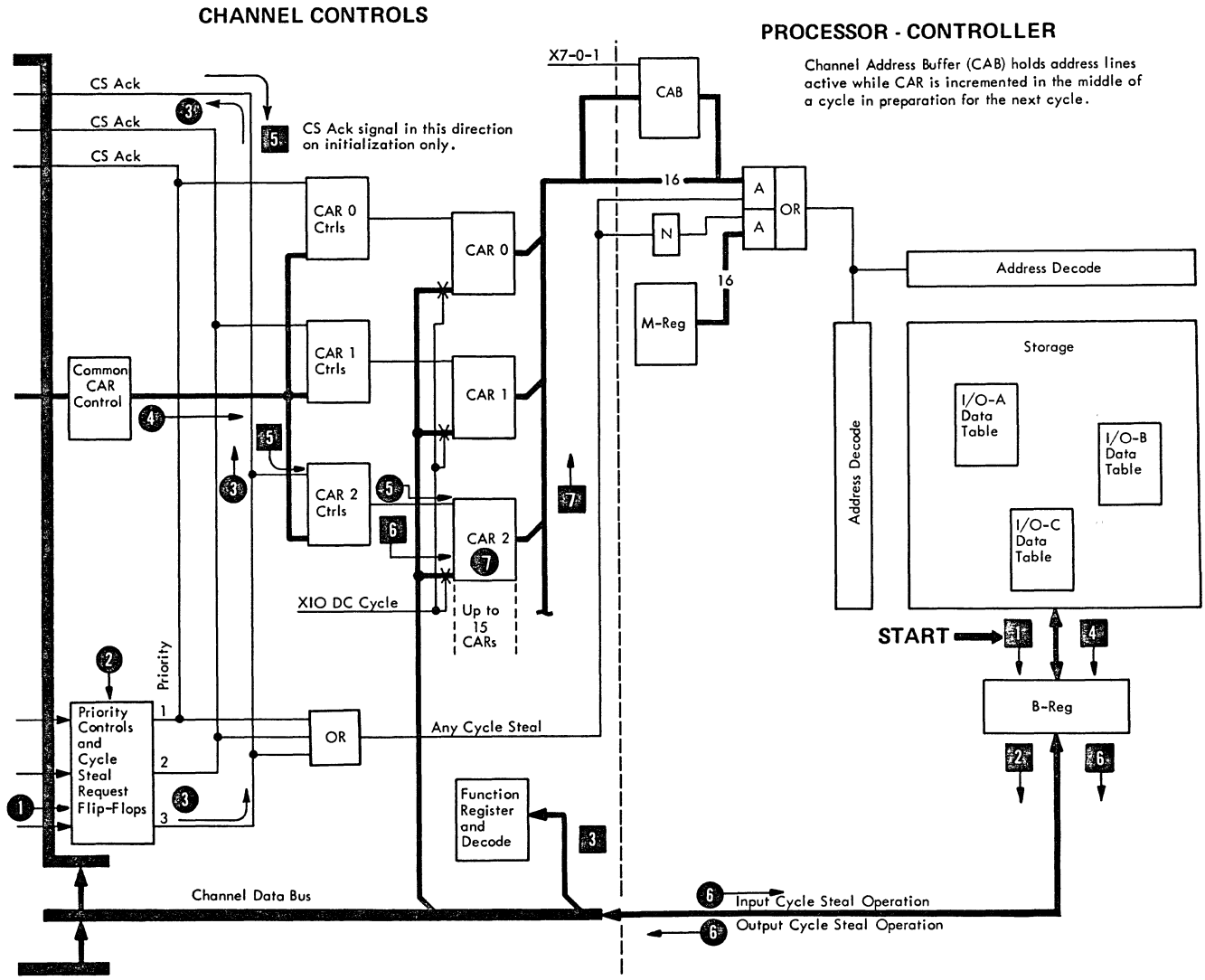


A INITIALIZATION

XIO Instruction | | Address of IOCC |

IOCC | Address Word: Data Table Address | Control Word: Area | Funct | Modifier |

E-Cycles of XIO Instruction	
E1 XIO Control Cycle	E2 XIO Data Cycle
1 XIO Control word read out to B-register	4 IOCC address word read out to B-register
2 Area, Function and Modifier transferred via Channel Data Bus to Out-Bus to select I/O	5 Selected I/O unit sends back CS Ack and CS control signals which select CAR as determined by wired logic
3 Function transferred to Function Register in channel controls	6 B-register output (IOCC Data Table Address) gated into selected CAR
	7 CAR now ready to address 1st data table word in storage when CS is requested by I/O unit.



B CYCLE STEAL

1. When data is needed, I/O - B generates Cycle Steal Request.
2. If higher priority is active, no acknowledge to I/O - B until all higher priority I/O's are serviced.
3. Acknowledge signal sent from channel controls to I/O - B.
4. I/O - B returns CS control signal (s) to Channel Controls.
5. CAR 2 control lines cause CAR 2 to address storage.
6. If I/O - B is an output device, data from storage is placed in the B-Reg and transferred via the Out Bus to I/O - B.
   If I/O - B is an input device, data from I/O - B is transferred via the In Bus to the B-Reg and written into storage.
7. CAR controls cause CAR 2 to be incremented for access to next data word.

20696.1

DATA CHANNEL OPERATION

Objectives: The 1442 cycle steal request and acknowledge are shown. The flow chart is drawn with the assumption that the 1442 is wired to use CAR 2.

Assume XIO Operation
- Initialize Read or
- Initialize Write

} Channel operations involving cycle steal.

INITIALIZATION:

E1, XIO Control Cycle

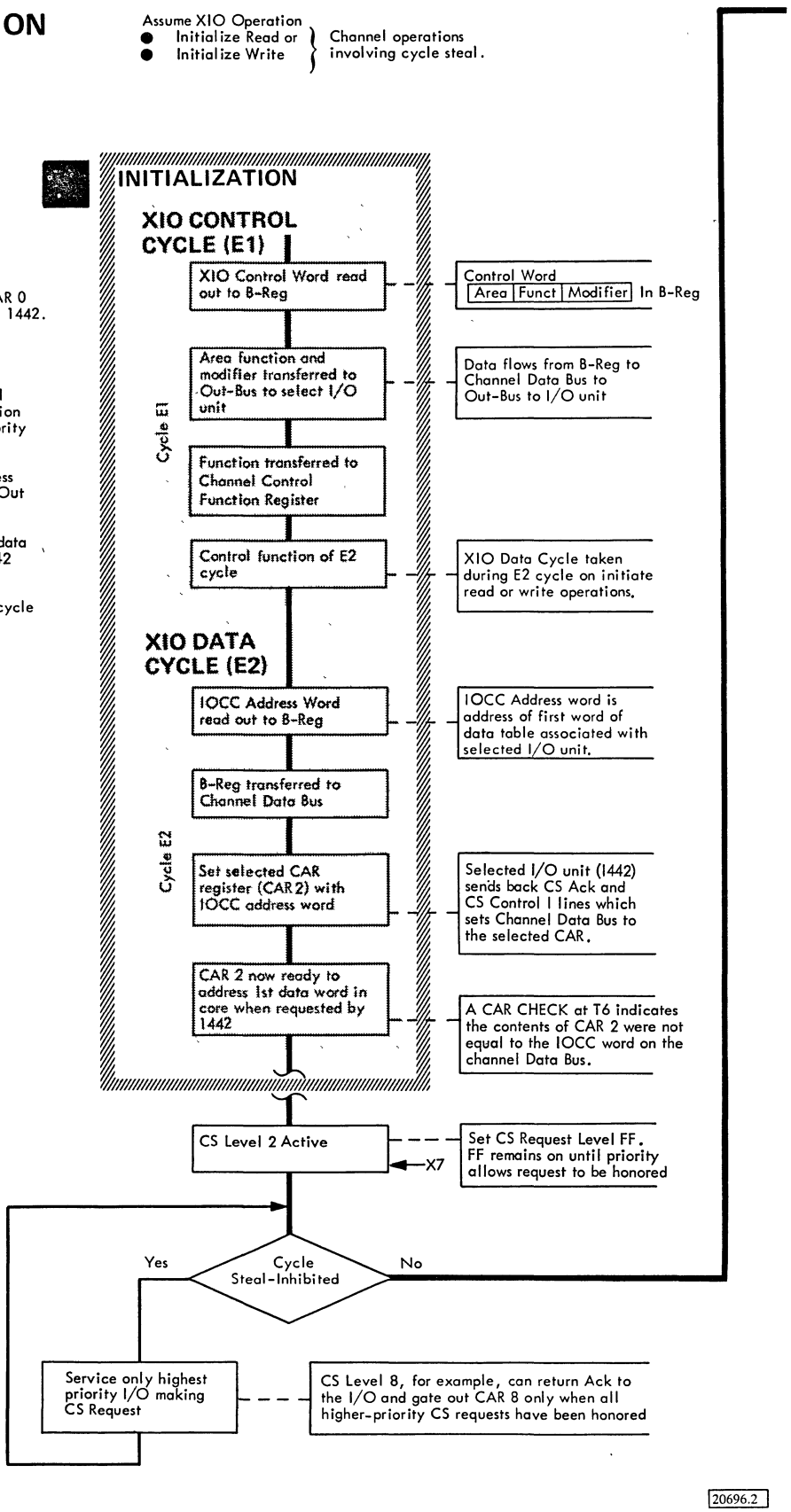
- Select I/O unit and load channel function register.

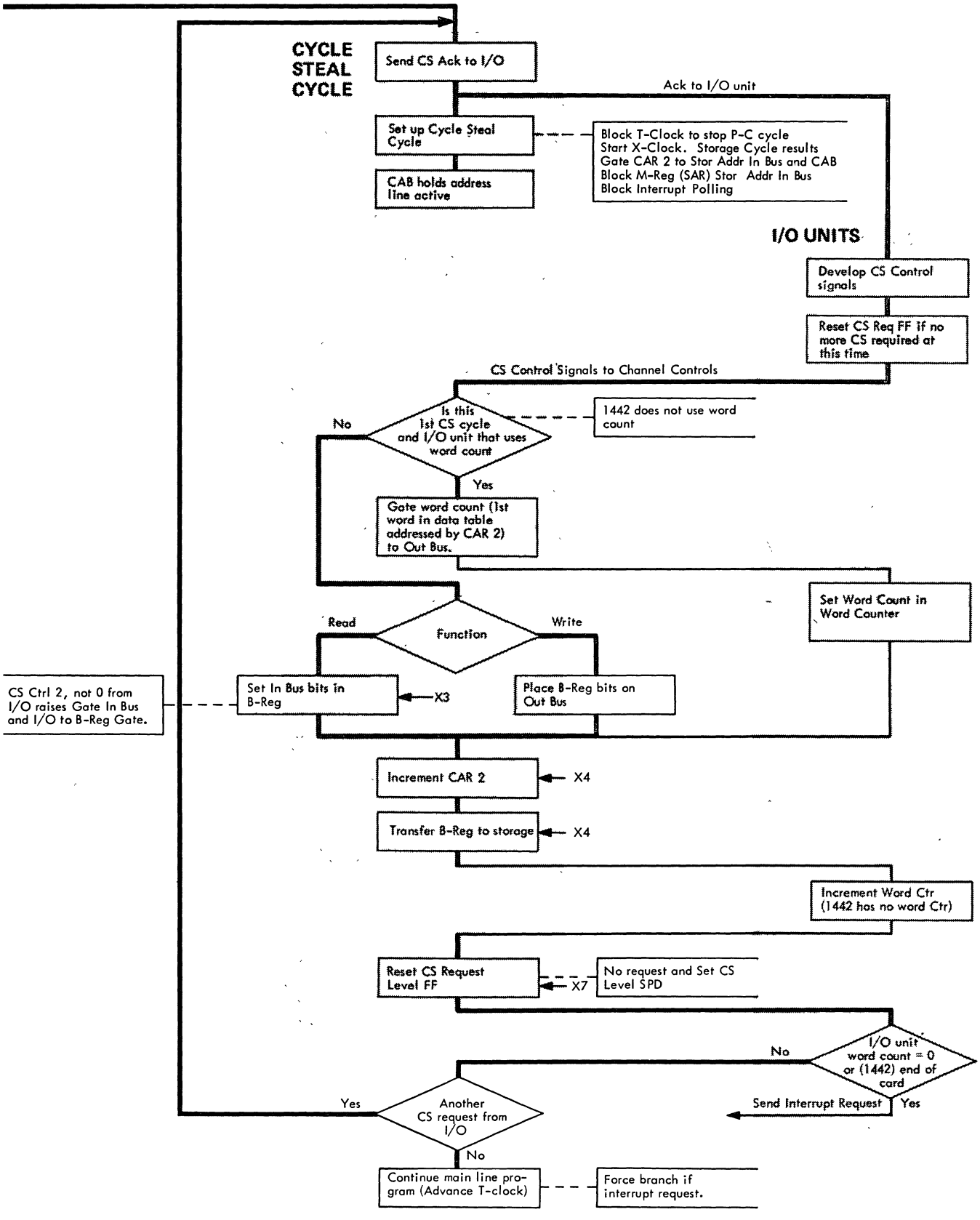
E2, XIO Data Cycle

- Read out IOCC address word and load in CAR 0 as address of first data word associated with 1442.

CYCLE STEAL:

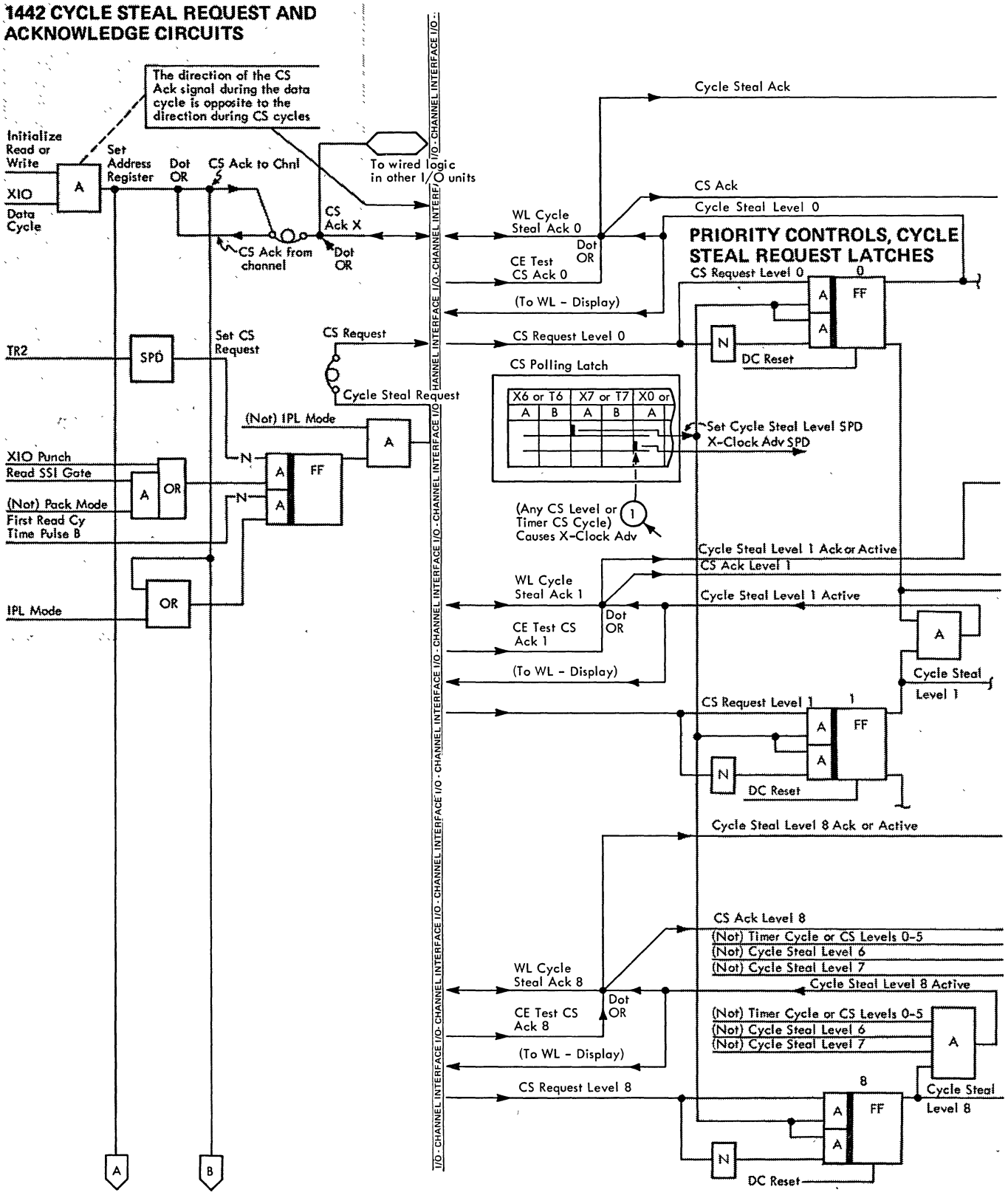
- When 1442 needs data access, a cycle steal request to channel controls causes interruption of P-C cycling provided that no higher priority requests are waiting.
- Data is transferred to or from the core address that is addressed by CAR 2 via either In or Out bus.
- Incrementing of CAR 2 takes place so next data table location will be addressed on next 1442 cycle steal cycle.
- Normal P-C cycling resumes at the end of cycle steal unless another CS request is waiting.




CYCLE STEAL CYCLE
Send CS Ack to I/O
Ack to I/O unit
Set up Cycle Steal Cycle
Block T-Clock to stop P-C cycle
Start X-Clock. Storage Cycle results
Gate CAR 2 to Stor Addr In Bus and CAB
Block M-Reg (SAR) Stor Addr In Bus
Block Interrupt Polling
CAB holds address line active
I/O UNITS
Develop CS Control signals
Reset CS Req FF if no more CS required at this time
CS Control Signals to Channel Controls
Is this 1st CS cycle and I/O unit that uses word count
1442 does not use word count
No
Yes
Gate word count (1st word in data table addressed by CAR 2) to Out Bus.
Set Word Count in Word Counter
Read
Function
Write
CS Ctrl 2, not 0 from I/O raises Gate In Bus and I/O to B-Reg Gate.
Set In Bus bits in B-Reg
X3
Place B-Reg bits on Out Bus
Increment CAR 2
X4
Transfer B-Reg to storage
X4
Increment Word Ctr (1442 has no word Ctr)
Reset CS Request Level FF
X7
No request and Set CS Level SPD
I/O unit word count = 0 or (1442) end of card
No
Yes
Send Interrupt Request
Another CS request from I/O
Yes
No
Continue main line program (Advance T-clock)
Force branch if interrupt request.
20696.3

DATA CHANNEL CIRCUITS

1442 CYCLE STEAL REQUEST AND ACKNOWLEDGE CIRCUITS



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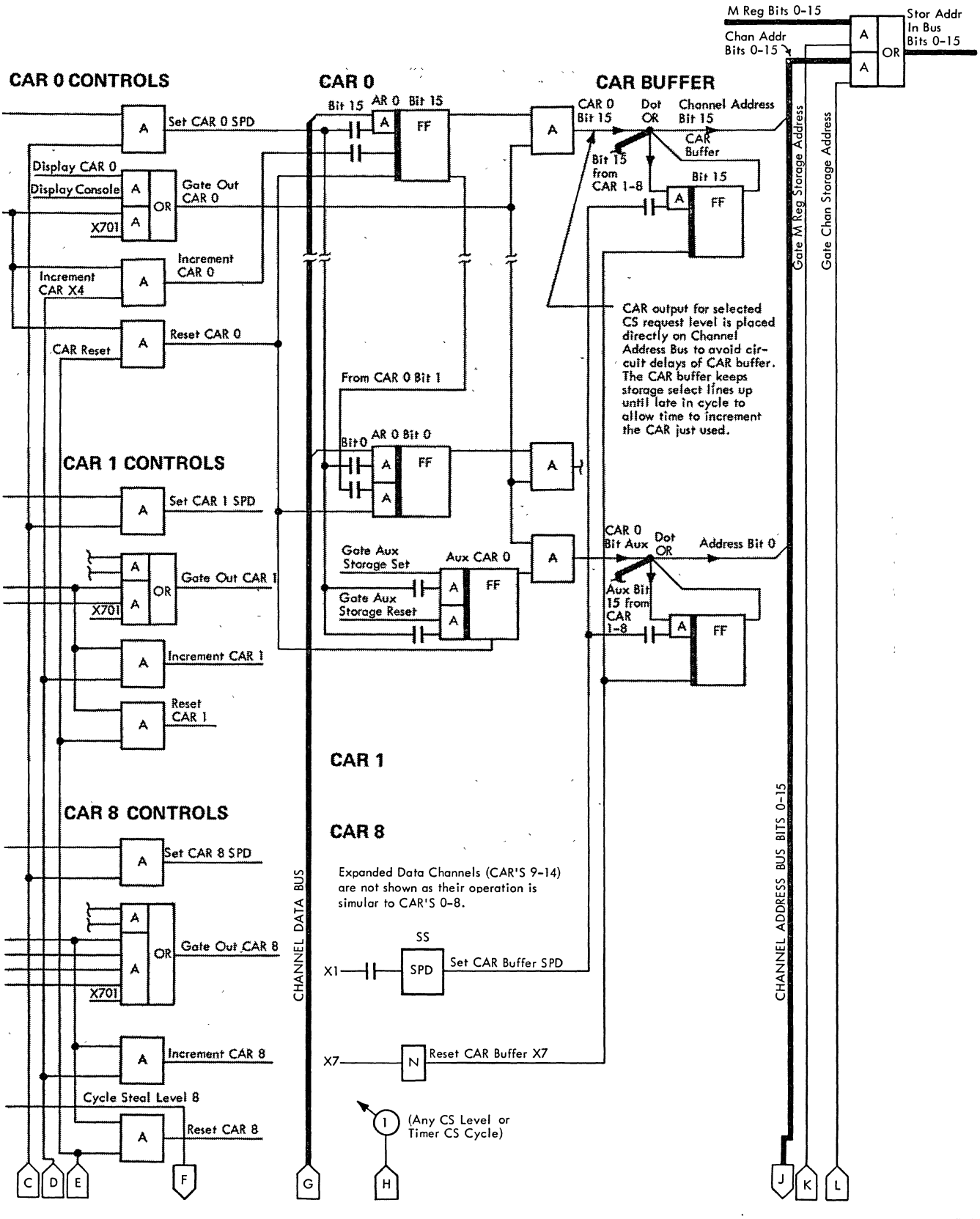
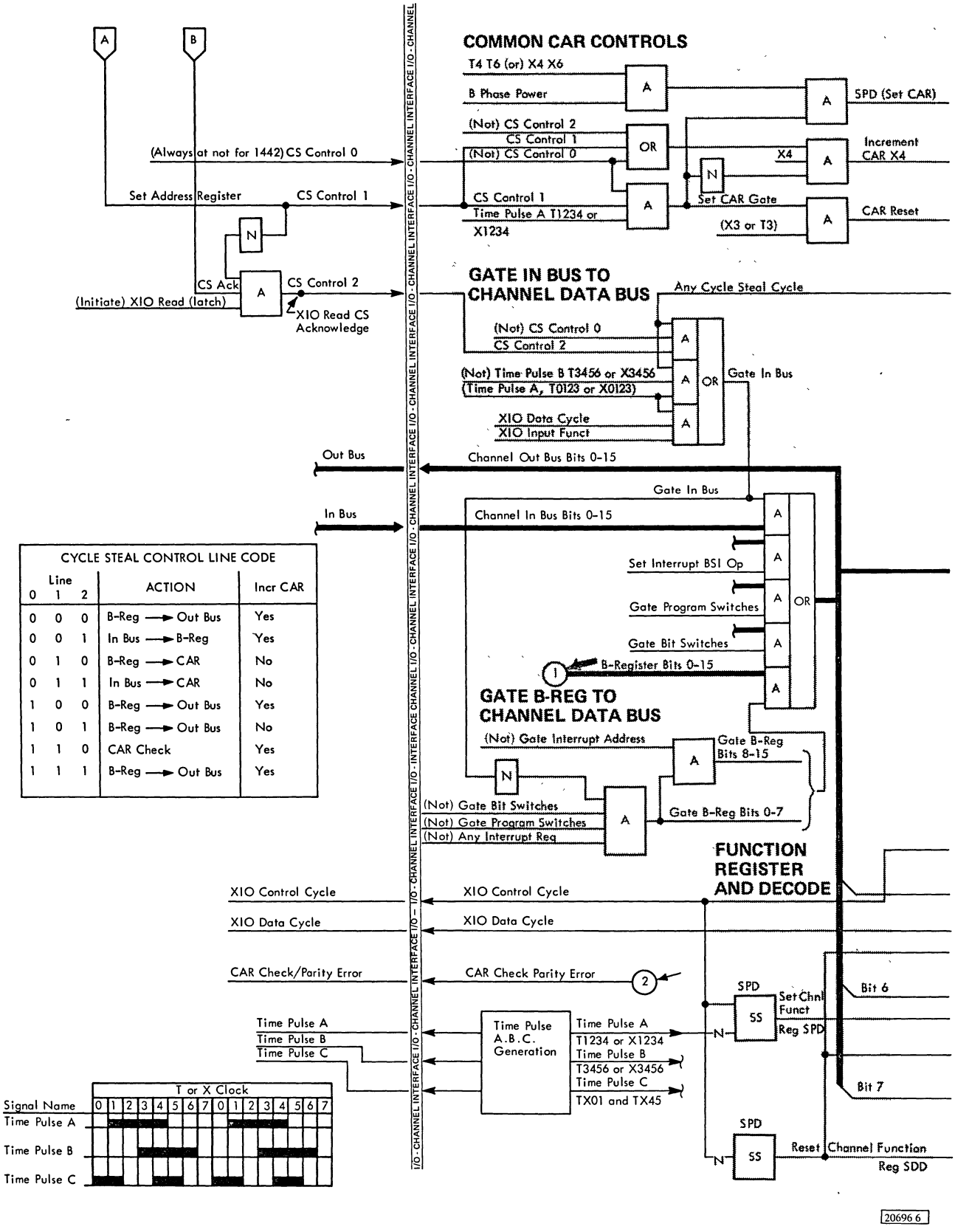
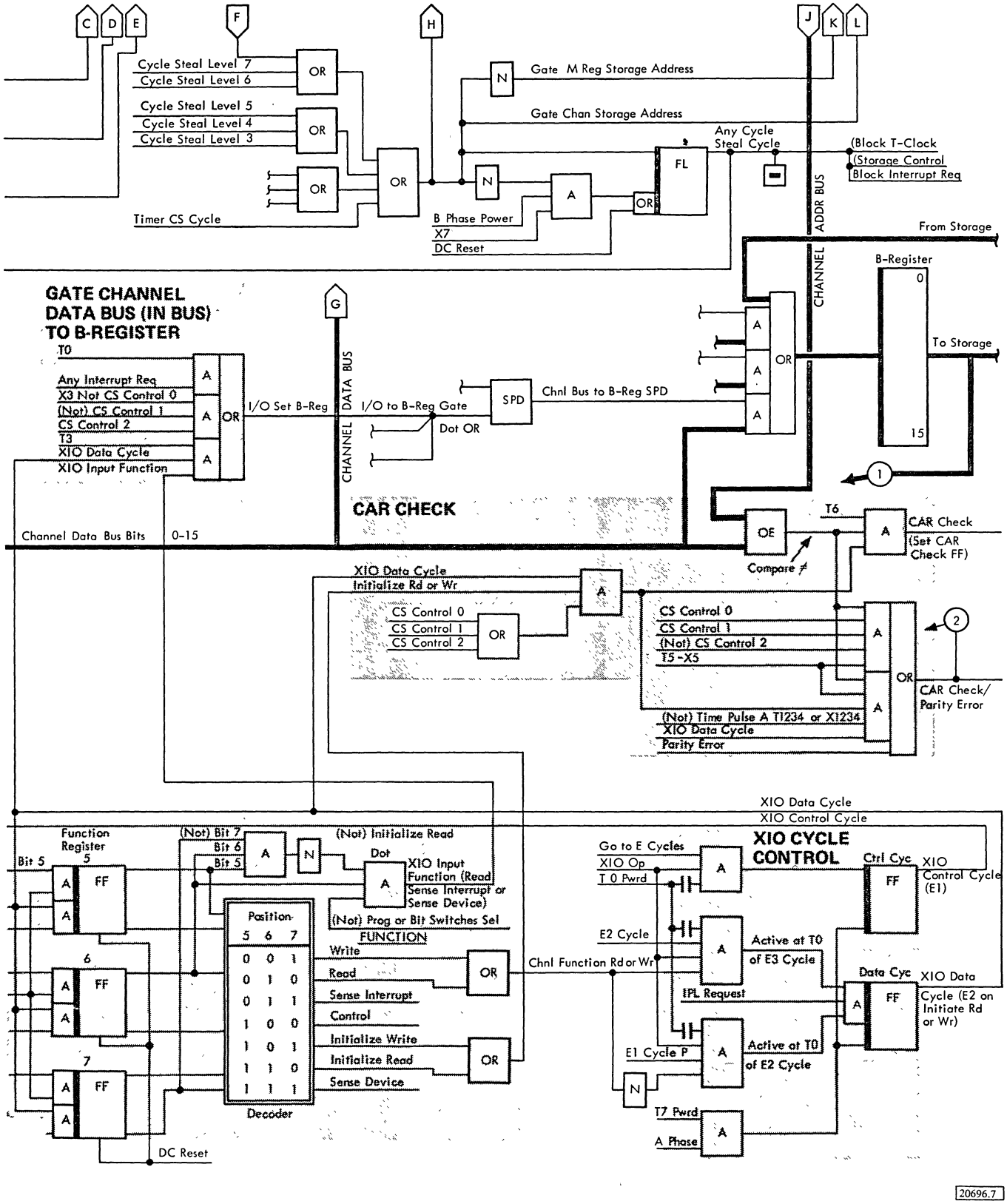

CAR 0 CONTROLS
CAR 0
CAR BUFFER
M Reg Bits 0-15
Chan Addr Bits 0-15
Stor Addr In Bus Bits 0-15
Set CAR 0 SPD
Display CAR 0
Display Console
Gate Out CAR 0
X701
Increment CAR 0
Increment CAR X4
Reset CAR 0
CAR Reset
Bit 15
AR 0 Bit 15
FF
CAR 0 Bit 15
Dot OR
Channel Address Bit 15
CAR Buffer
Bit 15 from CAR 1-8
Gate M Reg Storage Address
Gate Chan Storage Address
CAR output for selected CS request level is placed directly on Channel Address Bus to avoid circuit delays of CAR buffer. The CAR buffer keeps storage select lines up until late in cycle to allow time to increment the CAR just used.
From CAR 0 Bit 1
Bit 0
AR 0 Bit 0
CAR 1 CONTROLS
Set CAR 1 SPD
Gate Out CAR 1
Increment CAR 1
Reset CAR 1
Gate Aux Storage Set
Aux CAR 0
Gate Aux Storage Reset
CAR 0 Bit Aux
Address Bit 0
Aux Bit 15 from CAR 1-8
CAR 1
CAR 8 CONTROLS
Set CAR 8 SPD
Gate Out CAR 8
Increment CAR 8
Cycle Steal Level 8
Reset CAR 8
CAR 8
Expanded Data Channels (CAR'S 9-14) are not shown as their operation is simular to CAR'S 0-8.
SS
X1
SPD
Set CAR Buffer SPD
X7
Reset CAR Buffer X7
(Any CS Level or Timer CS Cycle)
CHANNEL DATA BUS
CHANNEL ADDRESS BUS BITS 0-15
C
D
E
F
G
H
J
K
L
20696.5

DATA CHANNEL CIRCUITS (Cont.)



CYCLE STEAL CONTROL LINE CODE

Line 0	1	2	ACTION	Incr CAR
0	0	0	B-Reg → Out Bus	Yes
0	0	1	In Bus → B-Reg	Yes
0	1	0	B-Reg → CAR	No
0	1	1	In Bus → CAR	No
1	0	0	B-Reg → Out Bus	Yes
1	0	1	B-Reg → Out Bus	No
1	1	0	CAR Check	Yes
1	1	1	B-Reg → Out Bus	Yes


C
D
E
F
H
J
K
L
Cycle Steal Level 7
Cycle Steal Level 6
Cycle Steal Level 5
Cycle Steal Level 4
Cycle Steal Level 3
OR
Timer CS Cycle
N
Gate M Reg Storage Address
Gate Chan Storage Address
Any Cycle Steal Cycle
FL
A
B Phase Power
X7
DC Reset
(Block T-Clock
(Storage Control
Block Interrupt Req
ADDR BUS
From Storage
CHANNEL
B-Register
0
15
To Storage
GATE CHANNEL DATA BUS (IN BUS) TO B-REGISTER
G
T0
Any Interrupt Req
X3 Not CS Control 0
(Not) CS Control 1
CS Control 2
T3
XIO Data Cycle
XIO Input Function
I/O Set B-Reg
DATA BUS
I/O to B-Reg Gate
Dot OR
SPD
Chnl Bus to B-Reg SPD
CHANNEL
CAR CHECK
Channel Data Bus Bits
0-15
OE
Compare ≠
T6
CAR Check
(Set CAR Check FF)
XIO Data Cycle
Initialize Rd or Wr
CS Control 0
CS Control 1
CS Control 2
(Not) CS Control 2
T5 -X5
CAR Check/ Parity Error
(Not) Time Pulse A T1234 or X1234
XIO Data Cycle
Parity Error
XIO Data Cycle
XIO Control Cycle
Function Register
Bit 5
FF
(Not) Bit 7
Bit 6
Bit 5
(Not) Initialize Read
Dot
XIO Input Function (Read Sense Interrupt or Sense Device)
(Not) Prog or Bit Switches Set
FUNCTION
Position
5 6 7
0 0 1
0 1 0
0 1 1
1 0 0
1 0 1
1 1 0
1 1 1
Write
Read
Sense Interrupt
Control
Initialize Write
Initialize Read
Sense Device
Decoder
DC Reset
XIO CYCLE CONTROL
Go to E Cycles
XIO Op
T 0 Pwrd
Ctrl Cyc
XIO Control Cycle (E1)
E2 Cycle
Chnl Function Rd or Wr
Active at T0 of E3 Cycle
IPL Request
Data Cyc
XIO Data Cycle (E2 on Initiate Rd or Wr)
E1 Cycle P
Active at T0 of E2 Cycle
T7 Pwrd
A Phase
20696.7

Appendix C. Device Status Words

AREA	FEATURE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Console Interrupt	* Interrupt Request															
	Interval Timers	* Timer A	* Timer B	* Timer C													
	Data Entry Switches	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	Sense Switches	← Sense →				← Program →				← CE Sense →							
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1 (1st) 15 (2nd)	1816 Printer-Keyboard 1053 Printer	* Printer Service Response	* Keyboard Service Response (1816)	* Keyboard Request (1816)		Printer Busy	Printer Not Ready	Keyboard Not Ready (1816)	Storage Protect Violation (1816)	Keyboard Parity Error (1816)	Printer Parity Error			†CE Busy	†CE Not Ready		
2 (1st) 17 (2nd)	1442 Card Read Punch			Error	Last Card	* Operation Complete	Parity Error	Storage Protect Violation	Feed Check Read Station					†CE Busy	†CE Not Ready	Busy	Not Ready
3	1054/1055 Paper Tape Reader/Punch	PT Reader Any Error	* PT Reader Service Request	PT Punch Parity Error	* PT Punch Service Request	PT Reader Busy	PT Reader Not Ready	PT Punch Busy	PT Punch Not Ready	PT Reader Parity Error	PT Reader Storage Protect	†CE PT Reader Busy	†CE PT Reader Not Rdy	†CE PT Punch Busy	†CE PT Punch Not Rdy		
4 8 9	1810 Disk Storage 1st Drive 2nd Drive 3rd Drive	Any Error	* Operation Complete	Disk Not Ready	Disk Busy (R/W or Ctrl)	Carriage Home	Parity Error	Storage Protect Error	Data Error	Write Select Error	Data Overrun		†CE Not Ready	†CE Busy		Sector Count High	Sector Count Low
5	1627 Plotter	* Service Response	Parity Error											†CE Busy	†CE Not Ready	Busy	Not Ready
6	1443 Printer	* Transfer Complete	Error	* Printer Complete	Channel 9	Channel 12	Channel 1	Parity				†CE Carriage Busy	†CE Printer Busy	†CE Printer Not Ready	Carriage Busy	Printer Busy	Printer Not Ready
10 (1st) 16 (2nd)	Analog Input	* End of Table	* DPC SS Conv Complete	* DPC Rly Conv Complete	* Storage Protect Violation	* Parity Control Error	* Parity Data Error	* Overload	* Overlap Conflict	Cyc Steal SS, AMAR Busy	DPC Relay Busy						Any Error
	Comparator	* High Out of Limit	* Low Out of Limit	* Overload	AMAR SS MPX			AMAR 512	AMAR 256	AMAR 128	AMAR 64	AMAR 32	AMAR 16	AMAR 8	AMAR 4	AMAR 2	AMAR 1
11	Digital Input	* Parity Error	* Storage Protect Violation	* DI Scan Complete	* Command Reject												DI Busy
	PISW	← Process Interrupt Points (Customer Assigned Groups) →															
12	Digital and Analog Output	* Parity Error	Pulse Output Timer	* D & A Out Scan Complete	* Command Reject	Data Channel Active											D/AO Busy
13	S/360 Adapter	* Command Reject	1800 Command Stored	* 360 Command Stored	* Halt	* Data Check	* Storage Protect Violation	* Transfer End	* End of Table	← 360 Command Byte →							
	Adapter Word Counter			← Word Count →													
14	Tape Control Unit		Tape Unit 1 Select	* Command Reject	* End of Table	Chain Stop	Storage Protect Violation Stop	Tape Data Error	Data Bus Out or P-C Parity Error	Data Overrun Error	* Operation Complete	CE Diagnostic Indicator	Wrong Length Record	At Load Point	Tape Indicator or Mark	Tape Busy or Rewind	Tape Busy or Not Ready
	TCU Word Counter	00 = True Count 11 = 1's Complement	← Word Count →														

* Interrupt Conditions

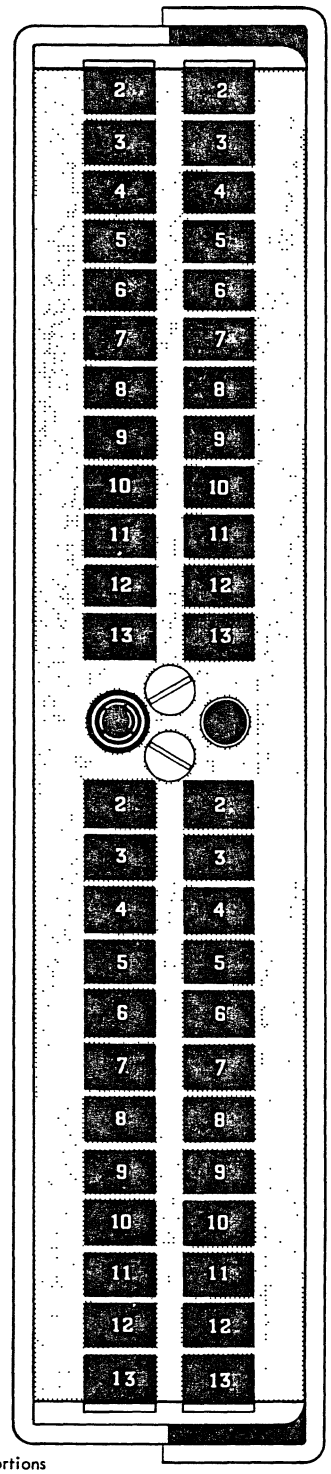
† Active Only in CE Mode

14092D

Appendix D. 1801/1802 I/O Adapter Interfaces

B	
End of Line	+12V
Ready	+12V
CRLFT (Carrier Return Line Feed Tab)	+12V
Upper Case Contact	+12V
Motor On	+12V
Printer Cam	+12V
+48V	+48V
+48V	+48V

G	
Backspace	0V
R2	0V
Line Feed	0V
Space	0V
Tab	0V
Carrier Return	0V
Aux	0V
T1	0V
T2	0V
+12V	+12V



D	
+48V	+48V
+48V	+48V
O	Ground

J	
0V	R1
0V	R5
0V	R2A
0V	Upper Case
0V	Lower Case
O	Ground
0V	Drop Motor Relay
0V	Red
0V	Black

O Ground Shield

Note: Internal drivers that appear in the G and J portions of the interface are 0V when turned on and 48V when turned off.

1801 or 1802 Signal Panel Connector Locations

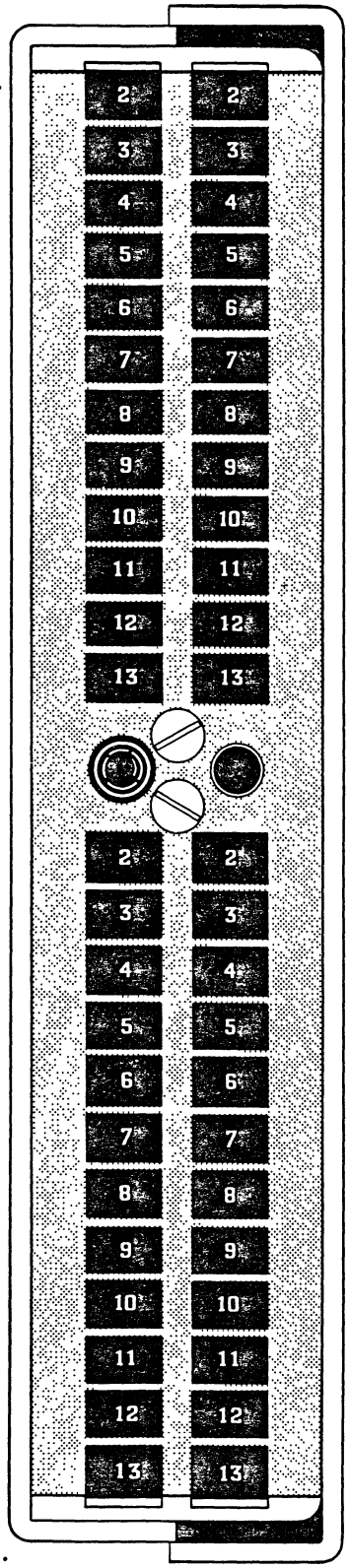
Printer Unit	Connector
1st, 1816 or 1053	R9
2nd, 1053	R7
3rd, 1053	R6
4th, 1053	R5

Printer Unit	Connector
5th, 1816 or 1053	S9
6th, 1053	S7
7th, 1053	S6
8th, 1053	S5

16111D

B	
Kybd Reenter Field	+12V
Kybd Contact 12	+12V
Kybd Contact 11	+12V
Kybd Contact 0	+12V
Kybd Contact 1	+12V
Kybd Contact 2	+12V
Kybd Contact 3	+12V
Kybd Contact 4	+12V
Keyboard Restore Magnet	0V
Kybd Contact 5	+12V
Kybd Contact 6	+12V

G	



D	
+12V	Kybd Contact 7
0V	Keyboard Proceed Lamp
+12V	Kybd Contact 8
+12V	Kybd Contact 9
+12V	Kybd Space
+12V	Kybd End Field
O	Ground
+12V	Kybd Reenter Char
+12V	Kybd Interrupt Req Key
+12V	Kybd Restore Key
+12V	Kybd Ready

J	

O Ground
1816 Keyboard signals are +12V (up) and -12V (down).
1801 or 1802 Signal Panel Connector Locations:

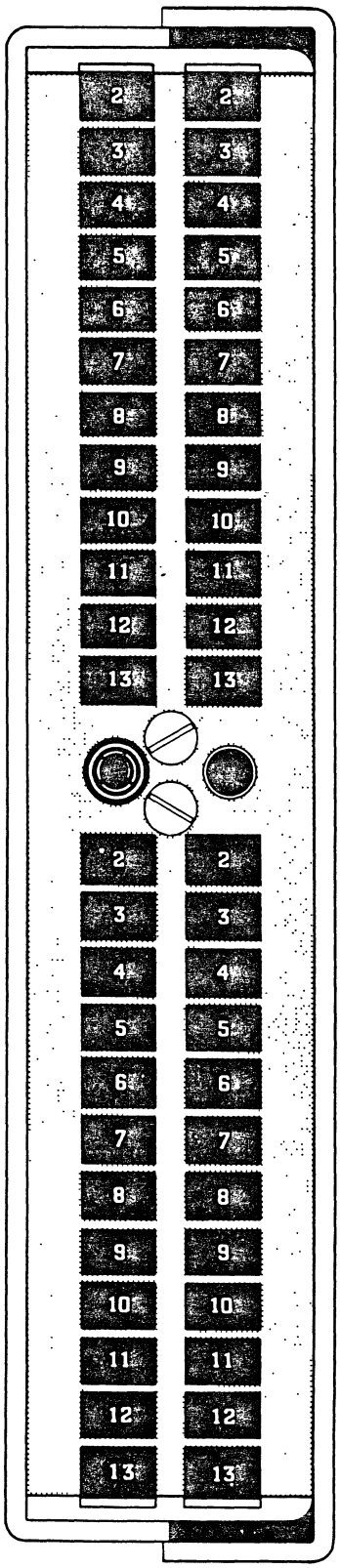
1st 1816 Keyboard, Connector R8
2nd 1816 Keyboard, Connector S8

16119B

Keyboard Interface Pin Assignments, 1816

B	
DO Bus Address Bit 15	•
DO Bus Address Bit 14	•
DO Bus Address Bit 13	•
DO Bus Address Bit 12	•
DO Bus Address Bit 11	•
DO Bus Address Bit 10	•
DO Bus Address Bit 9	•
Spare	•
Spare	•
Spare	•

G	
DO Bus Data Bit 0	•
DO Bus Data Bit 1	•
DO Bus Data Bit 2	•
DO Bus Data Bit 3	•
DO Bus Data Bit 4	•
DO Bus Data Bit 5	•
DO Bus Data Bit 6	•
DO Bus Data Bit 7	•
DO Bus Data Bit 8	•
DO Bus Data Bit 9	•



D	
•	DO Bus Data Load
•	DO Bus Data Reset
•	DO Bus Master Reset
•	DO Bus Load AO Output
•	DO Bus Pulse Output Reset
O	Ground
•	Spare
•	Spare
•	Spare
•	Spare
•	Spare

J	
•	DO Bus Data Bit 10
•	DO Bus Data Bit 11
•	DO Bus Data Bit 12
•	DO Bus Data Bit 13
•	DO Bus Data Bit 14
O	Ground
•	DO Bus Data Bit 15
•	Spare
•	Spare
•	Spare
•	Spare

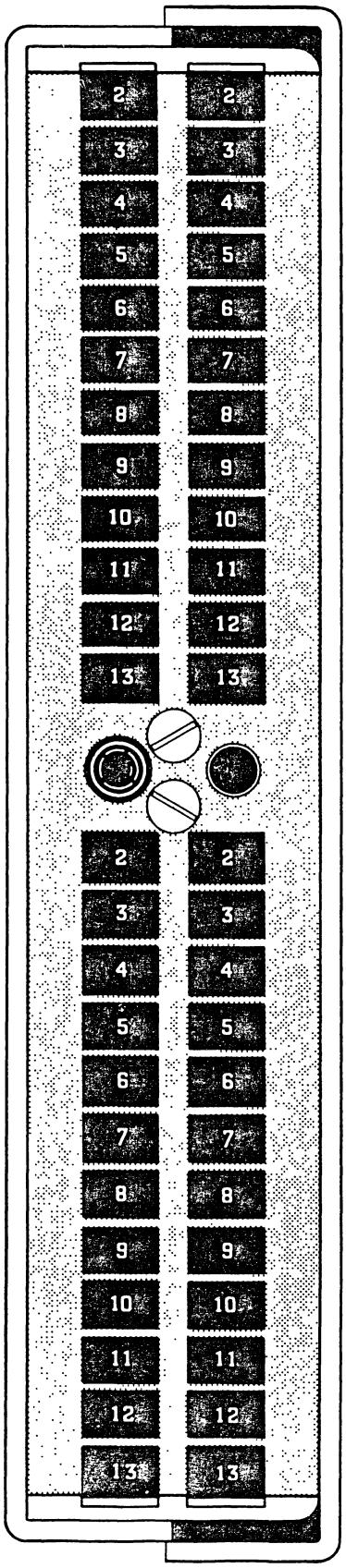
• Signal (Standard SLT)
O Ground Shield

23205

Digital Output Interface Pin Assignments, Connector Q3

B	
AO Bus Address Bit 15	•
AO Bus Address Bit 14	•
AO Bus Address Bit 13	•
AO Bus Address Bit 12	•
AO Bus Address Bit 11	•
AO Bus Address Bit 10	•
AO Bus Address Bit 9	•
Spare	•
Spare	•
Spare	•

G	
AO Bus Data Bit 0	•
AO Bus Data Bit 1	•
AO Bus Data Bit 2	•
AO Bus Data Bit 3	•
AO Bus Data Bit 4	•
AO Bus Data Bit 5	•
AO Bus Data Bit 6	•
AO Bus Data Bit 7	•
AO Bus Data Bit 8	•
AO Bus Data Bit 9	•



D	
•	AO Bus Data Load
•	AO Bus Data Reset
•	AO Bus Master Reset
•	AO Bus Load AO Output
•	AO Bus Pulse Output Reset
O	Ground
•	Spare
•	Spare
•	Spare
•	Spare
•	Spare

J	
•	AO Bus Data Bit 10
•	AO Bus Data Bit 11
•	AO Bus Data Bit 12
•	AO Bus Data Bit 13
•	AO Bus Data Bit 14
O	Ground
•	AO Bus Data Bit 15
•	Spare
•	Spare
•	Spare
•	Spare

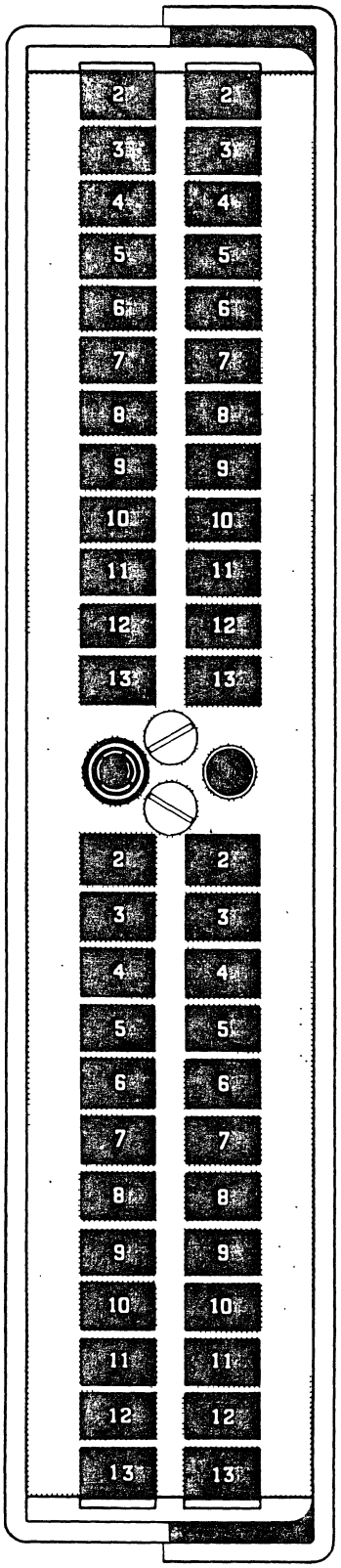
• Signal (Standard SLT)
O Ground Shield

23206

Analog Output Interface Pin Assignments, Connector Q4

B	
DC Reset to Read Point	•
Address Valid	•
Pulse Counter Reset	•
Spare	•
Spare	•
Spare	•
Spare	•
Spare	•
Spare	•
Spare	•

G	
Digital Input Not Bit 0	•
Digital Input Not Bit 1	•
Digital Input Not Bit 2	•
Digital Input Not Bit 3	•
Digital Input Not Bit 4	•
Digital Input Not Bit 5	•
Digital Input Not Bit 6	•
Digital Input Not Bit 7	•
Digital Input Not Bit 8	•
Digital Input Not Bit 9	•



D	
•	Read Address Bit 10
•	Read Address Bit 11
•	Read Address Bit 12
•	Read Address Bit 13
•	Read Address Bit 14
O	Ground
•	Read Address Bit 15
•	Spare
•	Spare
•	Spare
•	Spare

J	
•	Digital Input Not Bit 10
•	Digital Input Not Bit 11
•	Digital Input Not Bit 12
•	Digital Input Not Bit 13
•	Digital Input Not Bit 14
O	Ground
•	Digital Input Not Bit 15
•	Spare
•	Spare
•	Spare
•	Spare

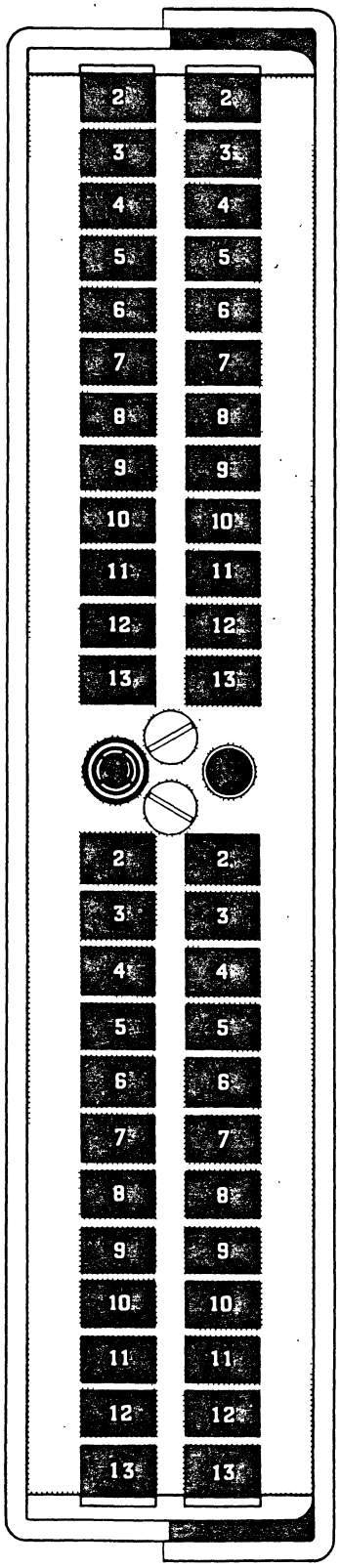
• Signal (Standard SLT)
O Ground Shield

16121A

Digital Input Interface Pin Assignments, Connector P1

B	
Out Bus Bit 0 to Process Interrupt	•
Out Bus Bit 1 to Process Interrupt	•
Out Bus Bit 2 to Process Interrupt	•
Out Bus Bit 3 to Process Interrupt	•
Out Bus Bit 4 to Process Interrupt	•
Out Bus Bit 5 to Process Interrupt	•
Out Bus Bit 6 to Process Interrupt	•
Out Bus Bit 7 to Process Interrupt	•
Out Bus Bit 8 to Process Interrupt	•
Out Bus Bit 9 to Process Interrupt	•

G	
Process Interrupt Bit 0	•
Process Interrupt Bit 1	•
Process Interrupt Bit 2	•
Process Interrupt Bit 3	•
Process Interrupt Bit 4	•
Process Interrupt Bit 5	•
Process Interrupt Bit 6	•
Process Interrupt Bit 7	•
Process Interrupt Bit 8	•
Process Interrupt Bit 9	•



D	
•	Out Bus Bit 10 to Process Interrupt
•	Out Bus Bit 11 to Process Interrupt
•	Out Bus Bit 12 to Process Interrupt
•	Out Bus Bit 13 to Process Interrupt
•	Out Bus Bit 14 to Process Interrupt
O	Ground
•	Out Bus Bit 15 to Process Interrupt
•	Device Sense Operation Gate
•	ILSW Operation Gate
•	DC Reset to Process Interrupt
•	Interrupt Address Bit 11

J	
•	Process Interrupt Bit 10
•	Process Interrupt Bit 11
•	Process Interrupt Bit 12
•	Process Interrupt Bit 13
•	Process Interrupt Bit 14
O	Ground
•	Process Interrupt Bit 15
•	Interrupt Address Bit 12
•	Interrupt Address Bit 13
•	Interrupt Address Bit 14
•	Interrupt Address Bit 15

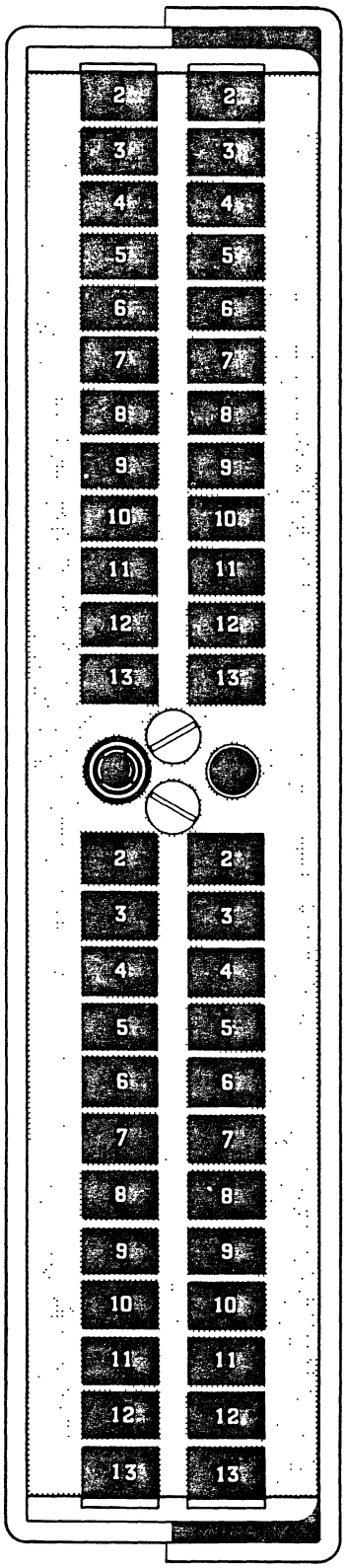
• Signal (Standard SLT)
O Ground Shield

16122A

Process Interrupt Interface Pin Assignments, Connector P2

B	
Process Interrupt 0	•
Process Interrupt 1	•
Process Interrupt 2	•
Process Interrupt 3	•
Process Interrupt 4	•
Process Interrupt 5	•
Process Interrupt 6	•
Process Interrupt 7	•
Process Interrupt 8	•
Process Interrupt 9	•

G	
Process Interrupt 12	•
Process Interrupt 13	•
Process Interrupt 14	•
Process Interrupt 15	•
Process Interrupt 16	•
Process Interrupt 17	•
Process Interrupt 18	•
Process Interrupt 19	•
Process Interrupt 20	•
Process Interrupt 21	•



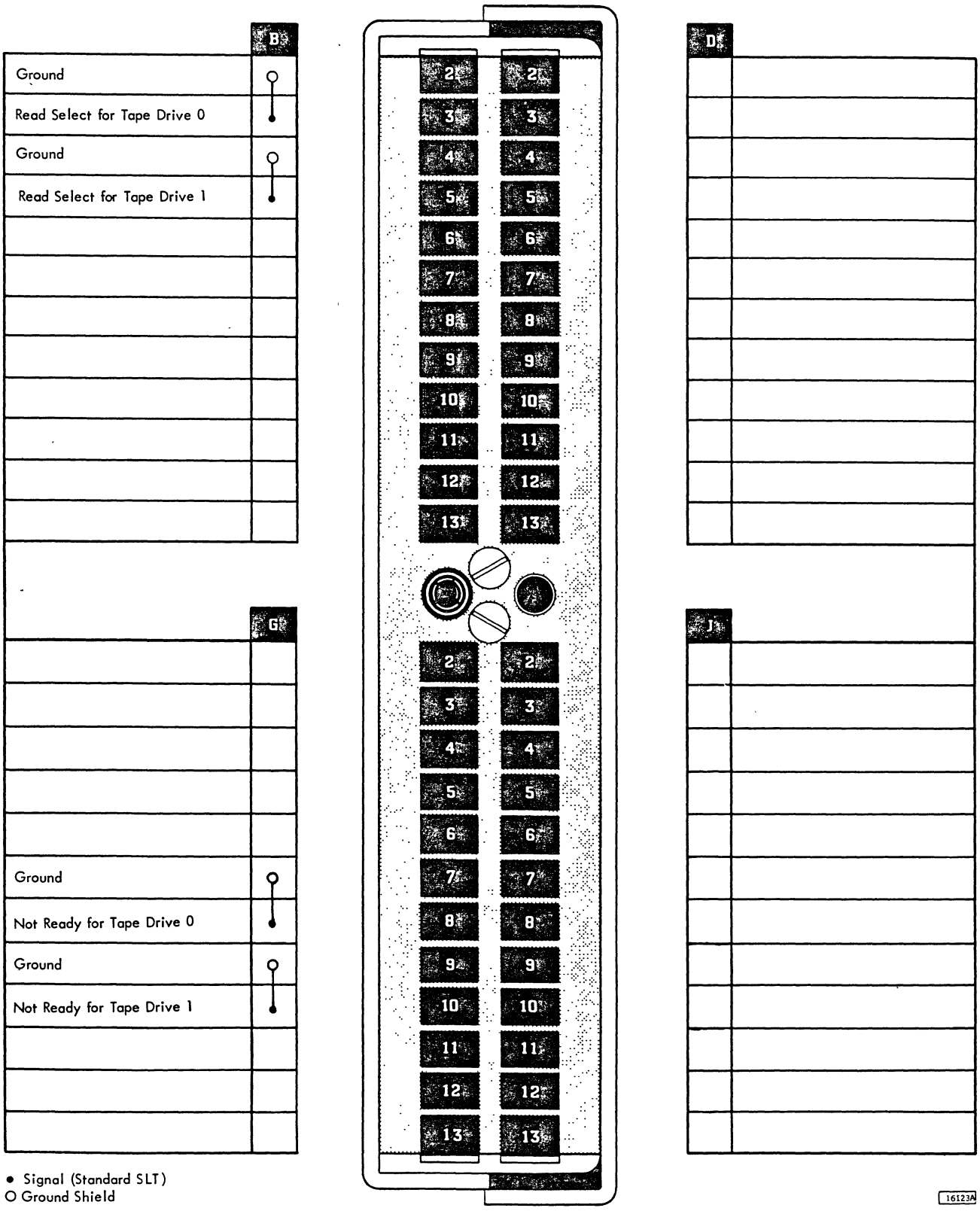
D	
•	Process Interrupt 10
•	Process Interrupt 11
•	Spare
•	Spare
•	Spare
○	Ground
•	Spare
•	Spare
•	Spare
•	Spare
•	Spare

J	
•	Process Interrupt 22
•	Process Interrupt 23
•	Spare
•	Spare
•	Spare
○	Ground
•	Spare
•	Spare
•	Spare
•	Spare
•	Spare

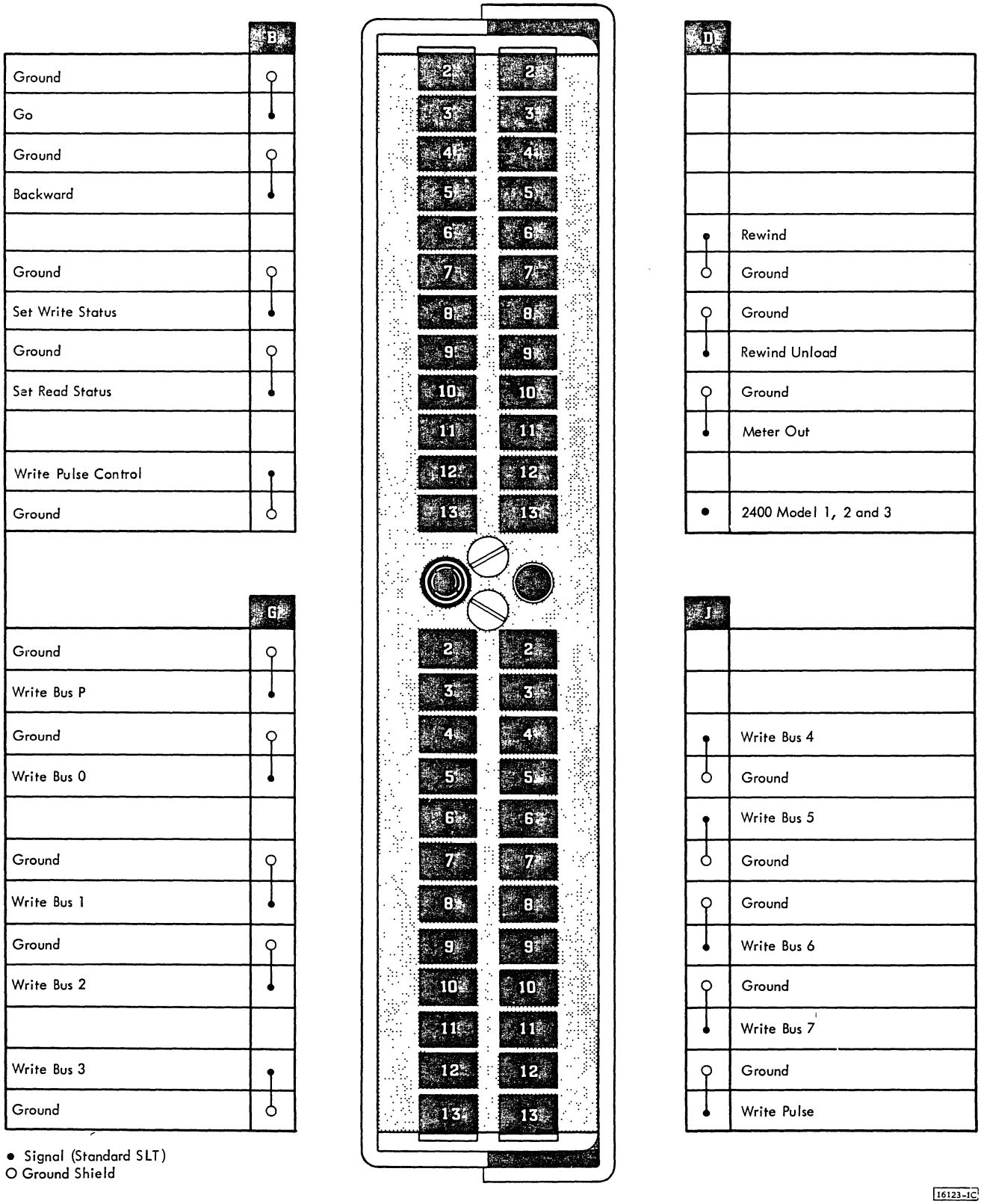
• Signal (Standard SLT)
○ Ground Shield

16122-1

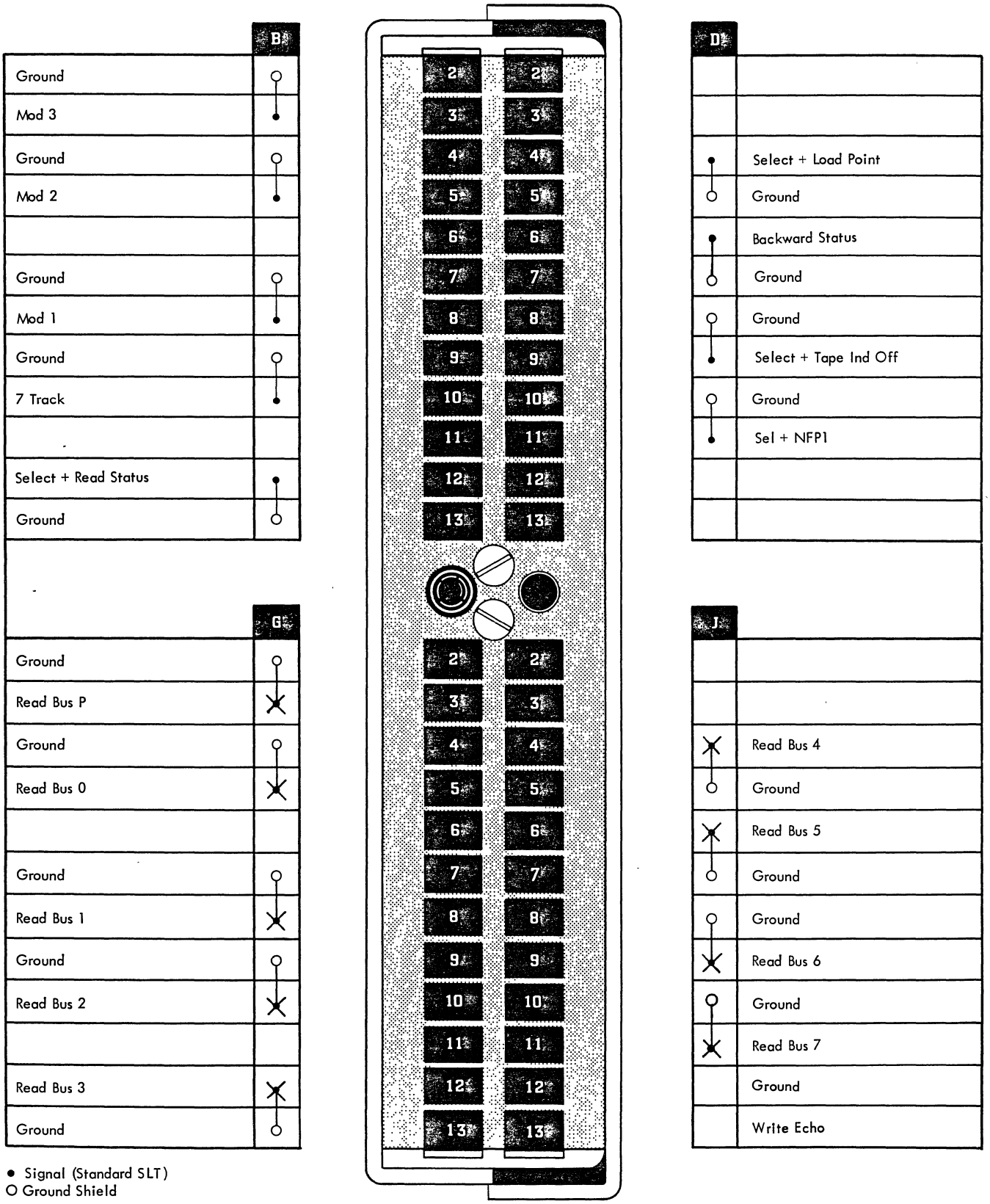
Process Interrupt Interface Pin Assignments, Connector P3



Magnetic Tape Interface Pin Assignments, Connector Q5



Magnetic Tape Interface Pin Assignments, Connector Q6



• Signal (Standard SLT)
O Ground Shield

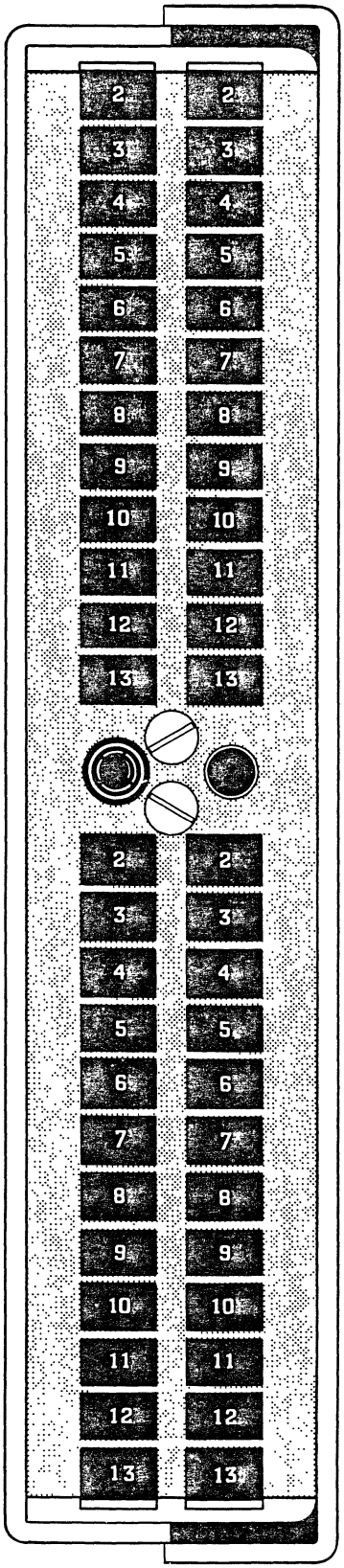
✕ Amplifier Analog Signal approximately 10V peak to peak.

16123-2C

Magnetic Tape Interface Pin Assignments, Connector Q7

B	
Read SCA 12	•
Read SCA 0	•
Read SCA 1	•
Read SCA 3	•
Read SCA 6	•
Read SCA 8	•
Read SCA 9	•
Card Feed CB 1	•
Card Feed CB 3	•
Card Feed CB 4	•

G	
Punch CB 2	•
Incr Drive CB B	•
Punch Lamp Dark	•
Punch Check Amp 11	•
Punch Check Amp 2	•
Punch Check Amp 4	•
Punch Check Amp 5	•
Punch Check Amp 7	•
Start Switch	+5V
NPRO Switch	+5V



D	
•	Read SCA 11
•	Read SCA 2
•	Read SCA 4
•	Read SCA 5
•	Read SCA 7
O	Ground
•	Read Emitter 1
•	Card Feed CB 2
•	Punch CB 1

J	
•	Incr Drive CB A
•	Punch Check Amp 12
•	Punch Check Amp 0
•	Punch Check Amp 1
•	Punch Check Amp 3
O	Ground
•	Punch Check Amp 6
•	Punch Check Amp 8
•	Punch Check Amp 9
-3V	Stop Switch
+5V	Hopper Empty Switch

• Signal (Standard SLT)
O Ground Shield

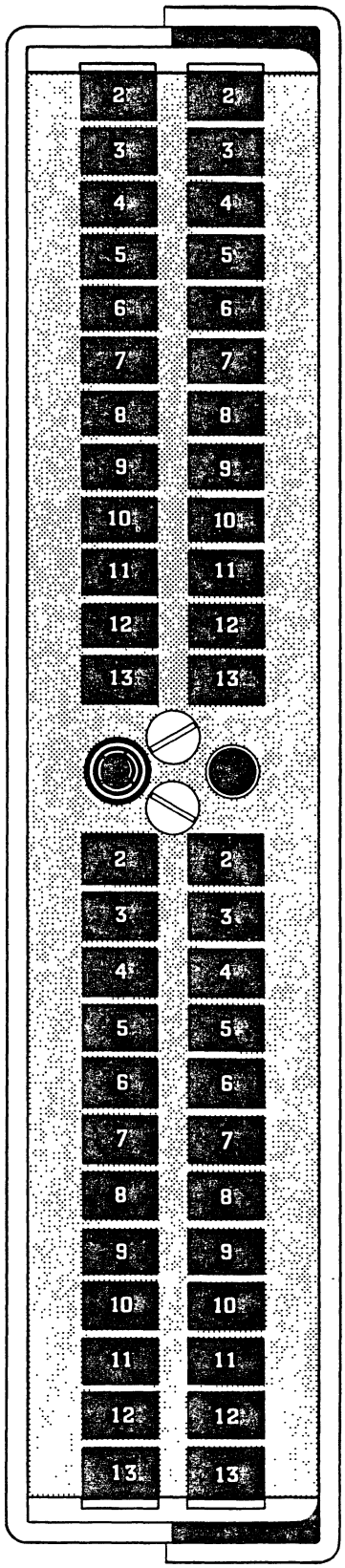
Note: G 12 & 13, and J 12 & 13 Switch Levels are +5V (up) and -3V (down).

Connector P8(1442 #1) or P5(1442 #2)

16124B

B	
Stacker Jam Switch	-3V
Punch Magnet 12	•
Punch Magnet 0	•
Punch Magnet 2	•
Punch Magnet 4	•
Punch Magnet 6	•
Punch Magnet 8	•

G	
Ready Indicator	•
Misfeed Indicator	•
Punch Station Jam Indicator	•
Read Error Indicator	•
Data Overrun	•
Stacker Sel Magnet	•
Motor Relay	•
Incr Drive Magnet A	•



D	
-3V	Idle Relay Contact
•	Punch Magnet 11
•	Punch Magnet 1
•	Feed Clutch Misfeed Indicator
•	Punch Magnet 3
O	Ground
•	Punch Magnet 5
•	Punch Magnet 7
•	Punch Magnet 9

J	
•	Check Indicator
•	Read Station Jam Indicator
•	Stacker Jam Indicator
•	Punch Error Indicator
O	Ground
•	Process Meter
•	Idle Relay
•	Feed Clutch Relay
•	Incr Drive Magnet B

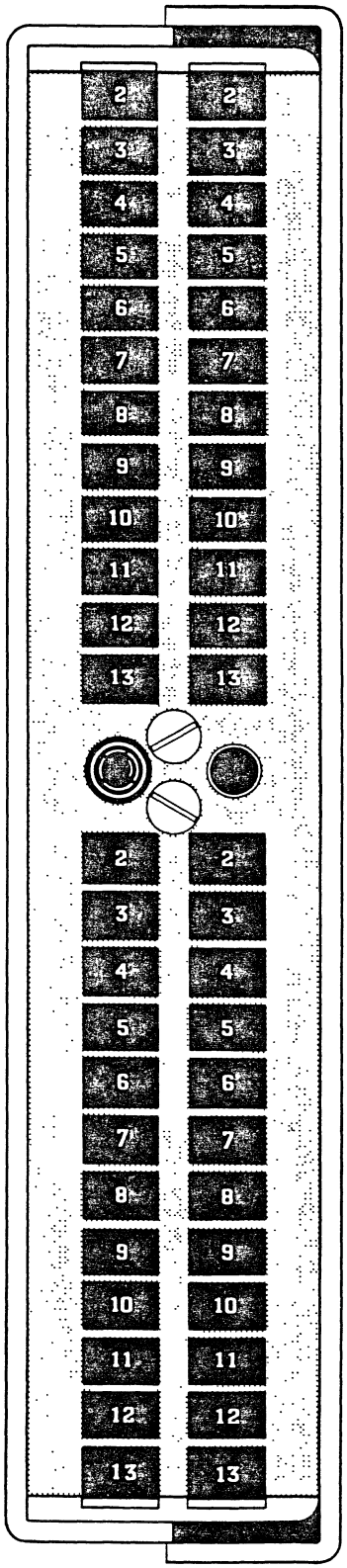
• Signal (Standard SLT)
O Grour. ⁴ Shield

16124-1C

1442 Card Read-Punch Interface Pin Assignments, Connector P9 (1442 #1) or P6 (1442 #2)

B	
Process Bit C	•
Process Bit A	•
Process Bit 4	•
Carriage Control	•
Space Suppress	•
Print Clock Control Trigger	•

G	
Time 015 - 030	•
Time 105 - 000	•
End of Form	•
Carriage Channel 12	•
Process Release	•
Print Check	•
Time 090 - 000	•



D	
•	Process Bit B
•	Process Bit 8
•	Process Bit 2
•	Process Bit 1
O	Ground
•	Meter On
•	Process + D Cycle

J	
•	Time 060 - 090
•	Print Check Reset
•	Carriage Busy
•	Carriage Channel 9
O	Ground
•	Carriage Channel 1
•	Print Ready
•	Reset SCM
•	Inhibit Print Clock Reset

• Signal (Standard SLT)
O Ground Shield

16125

1443 Printer Interface Pin Assignments, Connector P7

Appendix E. Analog Input Interfaces

Connector A-A2N7

B		D	
Spare	2	+6V	X06
	3		
Spare	4	+6V	X07
Spare	5	+6V	X08
	6	+6V	X09
X00 +6V	7	+6V	X10
X01 +6V	8	O	Ground
X02 +6V	9	+6V	X11
X03 +6V	10	+6V	X12
	11	+6V	X13
X04 +6V	12	+6V	X14
X05 +6V	13	+6V	X15

• Signal (Standard SLT)
O Ground Shield

16133A

1851 Solid State Multiplexer X Drive Lines

Connector A-A2N6

B		D	
Spare	2	0V	Y096-111
	3		
Spare	4	0V	Y112-127
Spare	5	0V	Y128-143
	6	0V	Y144-159
Y000-015 0V	7	0V	Y160-175
Y016-031 0V	8	O	Ground
Y032-047 0V	9	0V	Y176-191
Y048-063 0V	10	0V	Y192-207
	11	0V	Y208-223
Y064-079 0V	12	0V	Y224-239
Y080-095 0V	13	0V	Y240-255

• Signal (Standard SLT)
O Ground Shield

16132A

1851 Solid State Multiplexer Y Drive Lines

Connector A-A2A7

B		D	
	2	+12V	X06
	3		
Relay BS X Drive +12V	4	+12V	X07
	5	+12V	X08
	6	+12V	X09
X00 +12V	7	+12V	X10
X01 +12V	8		
X02 +12V	9	+12V	X11
X03 +12V	10	+12V	X12
	11	+12V	X13
X04 +12V	12	+12V	X14
X05 +12V	13	+12V	X15

• Signal (Standard SLT)
O Ground Shield

16138A

1851 Relay Multiplexer X Drive Lines

Connector A-A2A6

B		D	
Spare	2	0V	Y096-111
	3		
Spare	4	0V	Y112-127
Spare	5	0V	Y128-143
	6	0V	Y 144-159
Y000-015 0V	7	0V	Y160-175
Y016-031 0V	8	O	Ground
Y032-047 0V	9	0V	Y176-191
Y048-063 0V	10	0V	Y192-207
	11	0V	Y208-223
Y064-079 0V	12	0V	Y224-239
Y080-095 0V	13	0V	Y240-255

• Signal (Standard SLT)
O Ground Shield

16137A

1851 Relay Multiplexer Y Drive Lines, 000 to 255

Connector A-A2A5

B		D	
Spare	2	0V	Y352-367
	3		
Spare	4	0V	Y368-383
Spare	5	0V	Y384-399
	6	0V	Y400-415
Y256-271 0V	7	0V	Y416-431
Y272-287 0V	8	O	Ground
Y288-303 0V	9	0V	Y432-447
Y304-319 0V	10	0V	Y448-463
	11	0V	Y464-479
Y320-335 0V	12	0V	Y480-495
Y336-351 0V	13	0V	Y496-511

• Signal (Standard SLT)
O Ground Shield

16136A

1851 Relay Multiplexer Y Drive Lines, 256 to 511

Connector A-A2A4

B		D	
Spare	2	0V	Y608-623
	3		
Spare	4	0V	Y624-639
Spare	5	0V	Y640-655
	6	0V	Y656-671
Y512-527 0V	7	0V	Y672-687
Y528-543 0V	8	O	Ground
Y544-559 0V	9	0V	Y688-703
Y560-575 0V	10	0V	Y704-719
	11	0V	Y720-735
Y576-591 0V	12	0V	Y736-751
Y592-607 0V	13	0V	Y752-767

• Signal (Standard SLT)
O Ground Shield

16135A

1851 Relay Multiplexer Y Drive Lines, 512 to 767

Connector A-A2A3

B		D	
Spare	2	0V	Y864-879
	3		
Spare	4	0V	Y880-895
Spare	5	0V	Y896-911
	6	0V	Y912-927
Y768-783 0V	7	0V	Y928-943
Y784-799 0V	8	O	Ground
Y800-815 0V	9	0V	Y944-959
Y816-831 0V	10	0V	Y960-975
	11	0V	Y976-991
Y832-847 0V	12	0V	Y992-1007
Y848-863 0V	13	0V	Y1008-1023

• Signal (Standard SLT)
O Ground Shield

16134A

1851 Relay Multiplexer Y Drive Lines, 768 to 1023

Connector A-B2A7

B		D	
+6 Vdc Current Limited +6V	2	+6V	+6 Vdc Current Limited
	3		
Spare	4		Spare
Spare	5		Spare
	6		Spare
Ground O	7	O	Ground
Ground O	8	O	Ground (Not Used)
Spare	9		Spare
+30 Vdc Service +30V	10	+30V	+30 Vdc Service
	11		Spare
Spare	12		Spare
-30 Vdc Service -30V	13	-30V	-30 Vdc Service

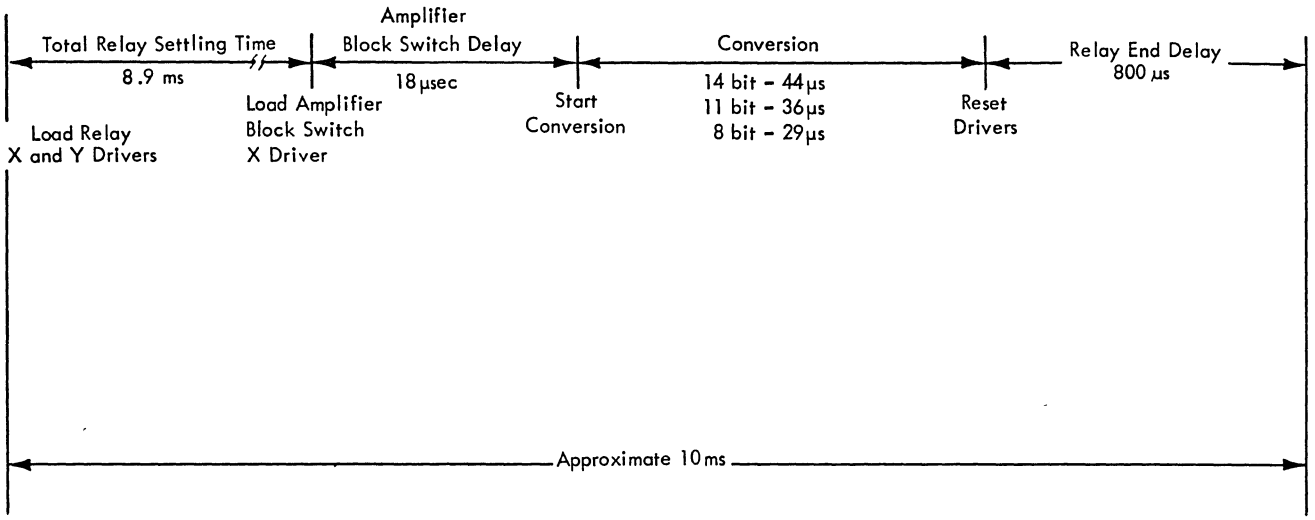
• Signal (Standard SLT)
O Ground Shield

16139A

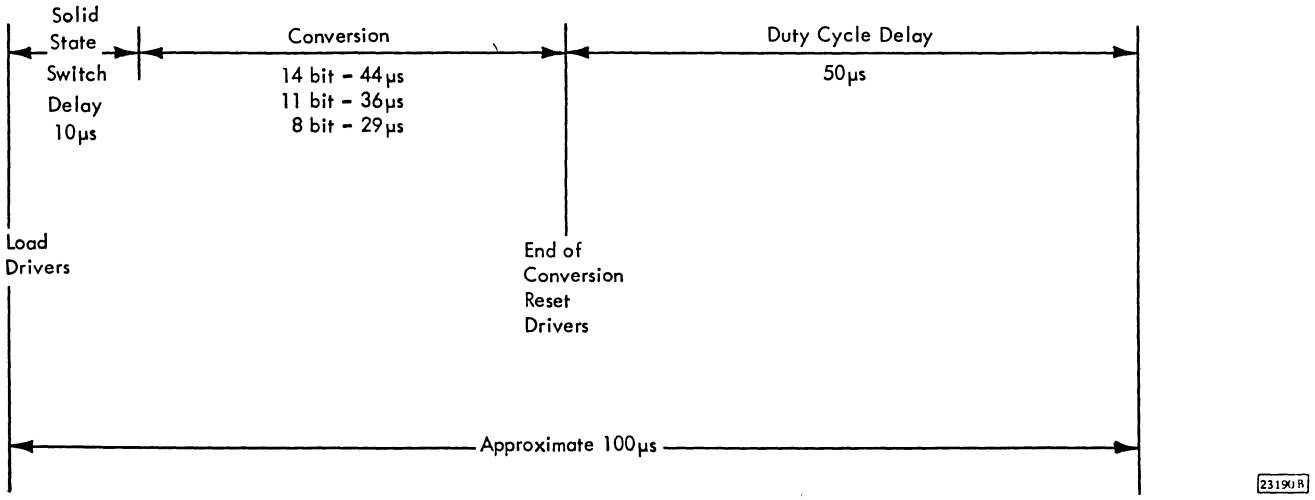
1851 Multiplexer Power Cable

ANALOG INPUT INTERFACE TIMING

Relay Multiplexer

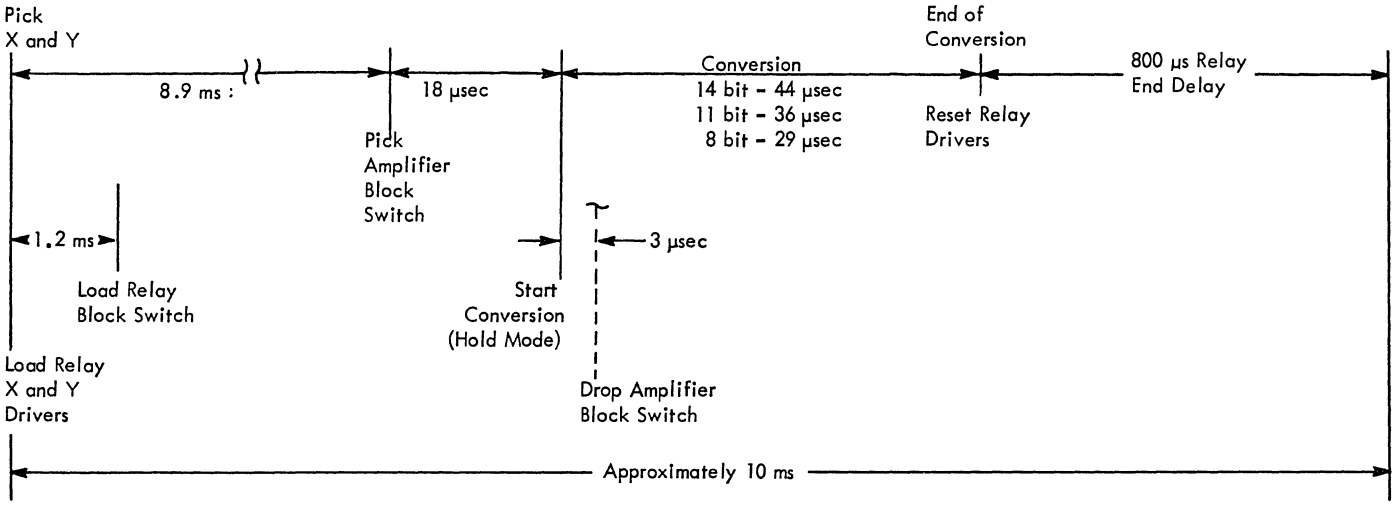


Solid State Multiplexer

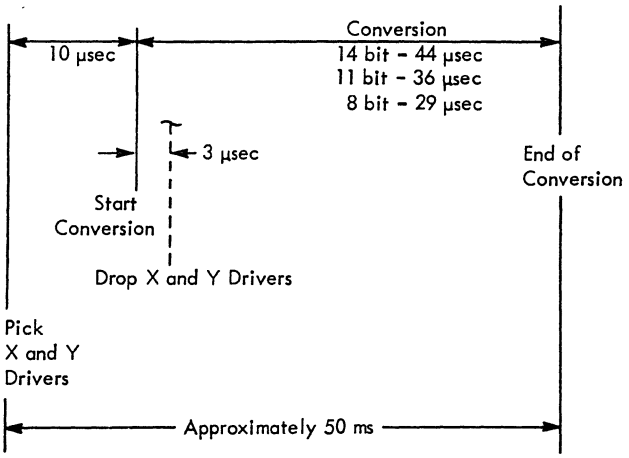


ADC Model 1 Timing

Relay Multiplexer



Solid State Multiplexer



ADC Model 2 Timing

A

B

C

D