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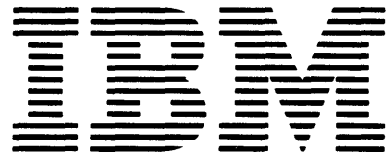
2740 Communication Terminal Model 1
2740 Communication Terminal Model 2
2741 Communication Terminal
Theory of Operation

IBM Maintenance Library

2740 Communication Terminal Model 1
2740 Communication Terminal Model 2
2741 Communication Terminal
Theory of Operation

PREFACE

This manual describes the theory of operation of the IBM 2740 Model 1 (2740-1), 2740 Model 2 (2740-2), and 2741 Communication Terminal and special features. To use this manual, the reader must be thoroughly familiar with these publications:

1. SLT Packaging and Documentation, SR23-2916
2. Introduction to Teleprocessing, Z25-2522
3. Common-Carrier Facilities for Teleprocessing, Z25-2529
4. 2740/2741 Communication Terminal, Operator's Guide, GA27-3001
5. IBM Line Adapters (Modems), S226-3003

In addition, the reader must completely understand the operation of the Selectric ® I/O.

The 2740/41 Communication Terminal Model 1, 2740 Communication Terminal Model 2, FE Diagram Manual, SY27-0014, is required to follow the explanations in the "Functional Units," "Principles of Operation," and "Features" sections of this manual.
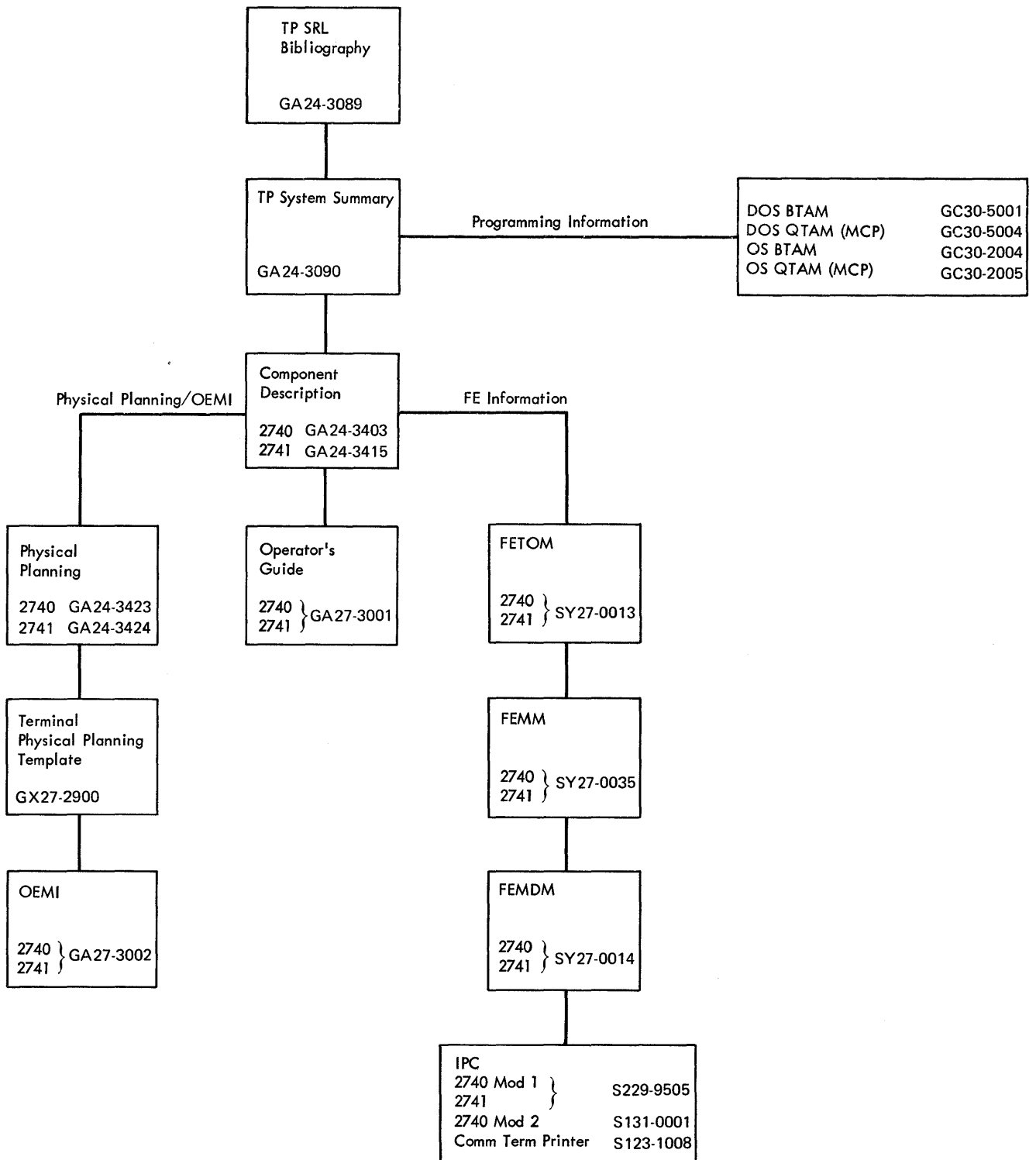
All figures in this manual are positive logic--that is, a positive level is required to condition ANDs, ORs, etc. Triggers and latches also require a positive level to be turned on or off.

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                                                     │ 2740 Mod 2     S131-0001│
                                                     │ Comm Term Printer  S123-1008│
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CONTENTS

ABBREVIATIONS

Adr.	Address	Modem	Modulator-Demodulator
Ans.	Answer	MPLX	Multiplexer
Attn.	Attention	MS	Millisecond
Auto	Automatic	Neg	Negative
BAT	Buffer Address Time	O	Operate
BCD	Binary Coded Decimal	O'flow	Overflow
Bfr.	Buffer	Par. , Pty.	Parity
Bksp.'	Backspace	PPI	Probe Position Indicator
CA	Control Address Mode	Pr.	Print
CAS	Control Address Selected Mode	PRE	Prefix
CASS	Control Address Selected Slave Mode	RCAB	Receive Check Answerback Mode
Central	Central Computer or Remote Multiplexer	RCS	Receive Check Slave Mode
Ck.	Check	Rec.	Receive
COMM	Communicate	Reg.	Register
CR	Carrier-Return	Res.	Reset
CR	Control Receive Mode	Rev.	Reverse
CS	Control Selected Mode	RT	Receive Text Mode
CSS	Control Selected Slave Mode	RTS	Receive Text Slave Mode
Ctr. , Cntr.	Counter	SC	Station Control
Ctrl.	Control	SD	Serdes
Cur.	Current	SDI	Serial Data In
EOB	End-of-Block	SDO	Serial Data Out
EOS	End-of-State	SLT	Solid Logic Technology
EOT	End of Transmission	SP	Stop Bit
Err.	Error	S-Register	Shift Register
Fwd	Forward	ST	Start Bit
H	Horizontal	Tab	Tabulator
HD	Half Duplex	TC	Transmit Control
HICG	Horizontal Current Control Gate	TOM	Typamatic
HISG	Horizontal Current Source Gate	TNS	Text Non-Selected Mode
H-reg.	Horizontal Register	TPAB	Transmit Poll Answerback Mode
I	Integrator	Trans.	Transmit
IB	Inhibit Interrupt	TSAB	Transmit
IIC	Image Index Counter	TT	Transmit Text
Interm.	Intermediate	UC	Uppercase
I/O	Input/Output	V	Vertical
IPM	Intermediate Polling Mode	VICG	Vertical Current Control Gate
I1	IIC Position One	VISG	Vertical Current Source Gate
I2	IIC Position Two	VRC	Vertical Redundancy Check
LC	Lowercase	V-reg.	Vertical Register
LF	Line Feed	1B-Register	First Buffer Register
LOC	Local	1 CH	One Cycle Halt
LRC	Longitudinal Redundancy Check	2B-Register	Second Buffer Register

2740 COMMUNICATION TERMINAL, MODEL 1

- Communicates with other terminals or a computer.

- Retains all Selectric® typewriter functions.

- Can be used off-line as a Selectric typewriter.

- Can be connected point-to-point or multipoint.

- Requires a line adapter (common-carrier data set or IBM modem).

The IBM 2740 Communication Terminal, Model 1 (Figure 1-1) is a device that enables data to be exchanged almost instantly between points far removed from each other. An operator can send (transmit) or receive information in typewritten form as it is needed. The exchange of information can be with another terminal or via a multiplexer, with a computer. When connected to a computer, the terminal can enter information into the computer, request information from the computer (remote inquiry), or have problems that occur in one area solved by a computer that is located in another area.

Figure 1-1 Communication Terminal (2740-1)

The 2740 is designed for simplicity of operation. All controls are located on the Selectric keyboard (Figure 1-2). Standard Selectric keys perform the same operations for the terminal as for a standard Selectric typewriter (except repetitive functions).

In addition to the standard Selectric keys, the 2740-1 terminal has a group of keys to the left of the keyboard and a group of keys and lights to the right of the keyboard. (Note that not all of the keys to the left of the terminal keyboard are presently used.) The added keys allow the 2740 to perform the additional operations required for communications. The lights show the status of the 2740 when in communicate mode. When the terminal is not needed for communications, a Local/Communicate switch allows the Selectric typewriter to be used off-line. Complete operating instructions for the terminal are in the Operators Guide, Form A27-3001, and are not covered in this manual.

Terminals can be connected to a communication system in one of two configurations: point-to-point or multipoint. Point-to-point configuration is the connection of a terminal to another terminal or to a multiplexer by a single communication line (Figure 1-3). Multipoint configuration is the connection of more than two terminals on a single communication line (Figure 1-3). If multipoint configuration is used without the station-control special feature, all terminals on the line receive the message from any terminal in use. Only one terminal can send at a time.

The 2740 terminal uses solid logic technology (SLT), permitting the terminal logic to be contained in one compact enclosure.

Information can be exchanged over short distances (room-to-room, building-to-building) or over long distances (state-to-state, coast-to-coast). Terminals cannot be directly connected to each other. To connect a terminal to another terminal or multiplexer, a line adapter is needed. The line adapter can be either a common-carrier data set or an IBM modem (modulator-demodulator). The 2740 can communicate over privately owned or common-carrier lines. When privately owned lines are used, an IBM modem connects the terminal to the line. When common-carrier lines are used, either an IBM modem or a common-carrier data set can be used. The Western Electric 103A and 103F data sets serve as examples.

Figure 1-2 Keyboard (2740-1)
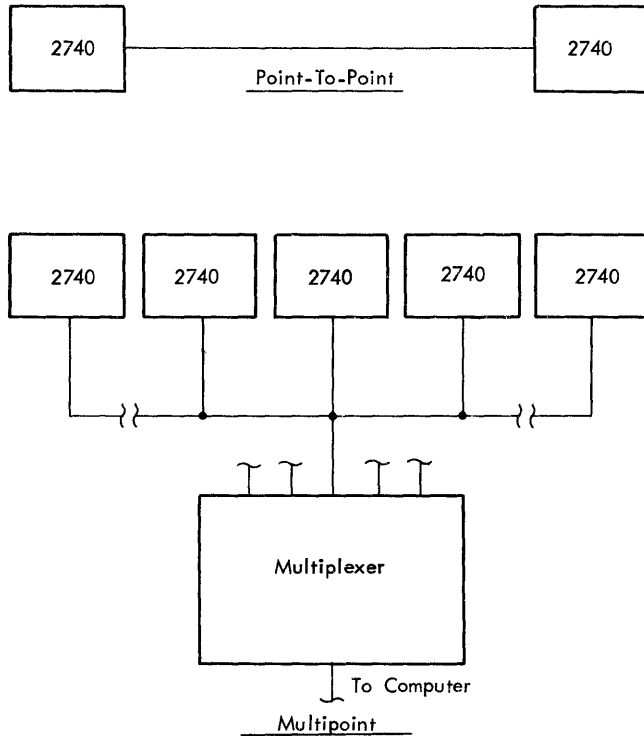
Figure 1-3 2740 Terminal Configurations

MODES OF OPERATION

Local

In local mode the I/O printer can be used as a Selectric typewriter.

Communicate

When a terminal is turned on (power up), the terminal goes into control-receive mode. Control-receive mode enables the terminal to accept and act on control characters. The control characters for basic-machine operation (no special features) are the bid character Ⓓ and end-of-transmission (EOT) character Ⓒ. The Ⓓ character places the sending terminal into transmit mode and the receiving terminal into receive mode. The Ⓒ character returns both terminals to control-receive mode.

When an operator sends a message, he presses the Bid key on the terminal keyboard. This causes the terminal logic to go into transmit mode and to generate and send the Ⓓ character. The Ⓓ character is received at the other terminal, which then goes into receive mode. The operator at the sending terminal keys in the message exactly as he would on a standard typewriter. When the message is completed, the operator presses the EOT key at the sending terminal. This causes a Ⓒ character to be generated and sent, and returns the sending terminal to control-receive mode. The Ⓒ character is received at the receiving terminal and returns the terminal to control-receive mode. Either terminal can now "bid" for the line and start sending information.

SPECIAL FEATURES (2740-1)

Many special features are available for the 2740. These allow the 2740 to be used with a dial-telephone system, or allow more than one 2740 to be used on a single communication line. With the record-checking feature, the 2740 can check and verify all incoming data.

Record-Checking

● VRC checks each character.

● LRC checks blocks of data.

● Data is checked in the receiving terminals.

With this feature, the 2740 checks all data it receives for validity. (This feature is not available for the 2741.) Data is checked in two ways: vertical redundancy check (VRC) and longitudinal redundancy check (LRC). VRC checks each character for odd-bit parity; LRC checks the entire message to insure that all characters are sent and received. In LRC checking, a special check character is generated by both the sending and receiving 2740's.

During the sending operation, the operator periodically presses the EOB key on the sending 2740.

This causes the generated LRC check character to be sent over the line to the receiving 2740. The receiving 2740 then compares the check character it receives with the one it has generated. If an error is detected, the Restart light turns on, indicating to the operator than an error has occurred.

When a VRC-error occurs, a dash is printed in place of the error character and the message continues. When an LRC-error is detected, a dash is printed, the Restart light comes on, and the terminal keyboard locks until the Restart key is pressed.

Automatic EOB

● Checks data each time the Carrier-Return key is pressed.

The automatic EOB feature causes data to be checked every time the Carrier-Return key is pressed on the sending 2740. Thus, each print line is checked and, in the event of an error, can be resent as soon as the error is detected.

Dial-Up

● Connects a 2740 to another 2740 or to a computer by using a dial-telephone data set.

The dial-up feature allows the 2740 to communicate, via the common-carrier dial detwork, with another 2740 or with a computer. The entire telephone common-carrier system is available for use by the terminals. This feature reduces common-carrier communication costs to a minimum; a charge is made for the line only during the time the terminal is actually connected to the line. This feature is used with the Western Electric 103A dial data set or equivalent. The operator dials a telephone number to connect the terminal to another terminal equipped with the same feature.

Transmit Control

● Allows the computer to control the sending or receiving status of the terminal.

The dial-up feature is a prerequisite for this feature. the transmit-control feature allows the computer to control the sending or receiving status of a remote terminal. Thus, the 2740 with this feature is under complete control of the computer. (This feature is not needed for the 2741.)

Station Control

● Allows more than one 2740 to be on the same communication line without contention.

● A single 2740, a group of 2740's or all 2740's on the line can be addressed to receive data.

● Each 2740 on the line is separately polled to send data.

The station-control feature allows more than one 2740 to be connected to a single communication line without contention (more than one terminal attempting to transmit at the same time). (This feature is not available for the 2741.) The communication line can be either a private in-house line or a leased common-carrier line. A special system of addressing and polling allows a computer to control the send or receive status of each terminal on the communication line.

Addressing is an operation by which the computer calls a terminal to send data to it. Each 2740, a pre-determined group of 2740's, or every 2740 on the line can be addressed to receive the message through the use of special addressing codes.

Polling is an operation by which a particular 2740 is notified that it alone can send data. If the polled 2740 is not ready to send data after a given length of time, another 2740 on the same line is polled.

Both the polling and addressing operations use a special sequence of control characters to allow operation to begin. These control characters are explained in Chapter 4.

2760 Attachment

● Allows the attachment of one IBM 2760 Optical Image Unit to a 2740, Model 1

The record-checking feature is a prerequisite for this feature. Neither the station control nor the transmit control feature can be installed on the 2740-1, and the 2740-1 must have serial number 15000 or higher. The attachment feature allows one IBM 2760 Optical Image Unit to be attached to the 2740-1. The 2760 utilizes the control circuitry of the 2740-1 to transmit data to, and receive data from, a multiplexer. When the 2760 is attached, the 2740-1 is always in terminal-to-multiplexer mode of operation.

IBM 2741 COMMUNICATION TERMINAL

● The 2741 communicates only with a computer.

● The 2741 operations are controlled by computer programming.

The 2741 can communicate only point-to-point with a computer (Figure 1-4). The sending or receiving status of the 2741 is controlled by computer programming. The primary use of the 2741 is in the IBM Administrative Terminal System (ATS).

The 2741 uses most of the same sending and receiving circuits as the 2740 and communicates by means of a data set or modem. The main physical difference between the 2741 and the 2740 is the Selectric keyboard. On the 2741, no keys or lights are added to the standard Selectric keyboard, but the Index key is replaced with the Attention key (Figure 1-5). Another difference is that all special features available for the 2740 are not available for the 2741. The standard 2741 uses a different typing element from the 2740, require the use of a different character code for the print characters, called a correspondence code.
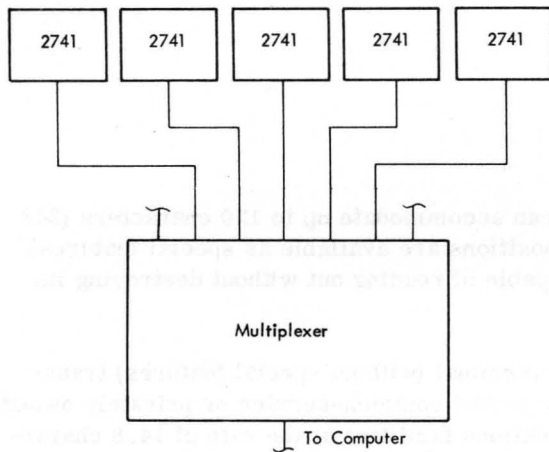
Figure 1-4 Terminal Configurations (2741)

SPECIAL FEATURES (2741)

Dial Up

The Dial-Up feature for the 2741 performs the same functions as for the 2740.

Receive Interrupt

The Receive Interrupt feature allows the 2741 operator to interrupt the reception of a message from the computer so that he can send instructions.

Transmit Interrupt

The Transmit Interrupt feature allows the computer to interrupt the transmission of text from the 2741.

Typamatic

The Typamatic feature permits the operator to automatically repeat the space, backspace, and underscore/hyphen operations by pressing this key.

Print Inhibit CPU Control

The Print Inhibit CPU Control feature enables the CPU to inhibit the 2741 from printing transmitted or received data.
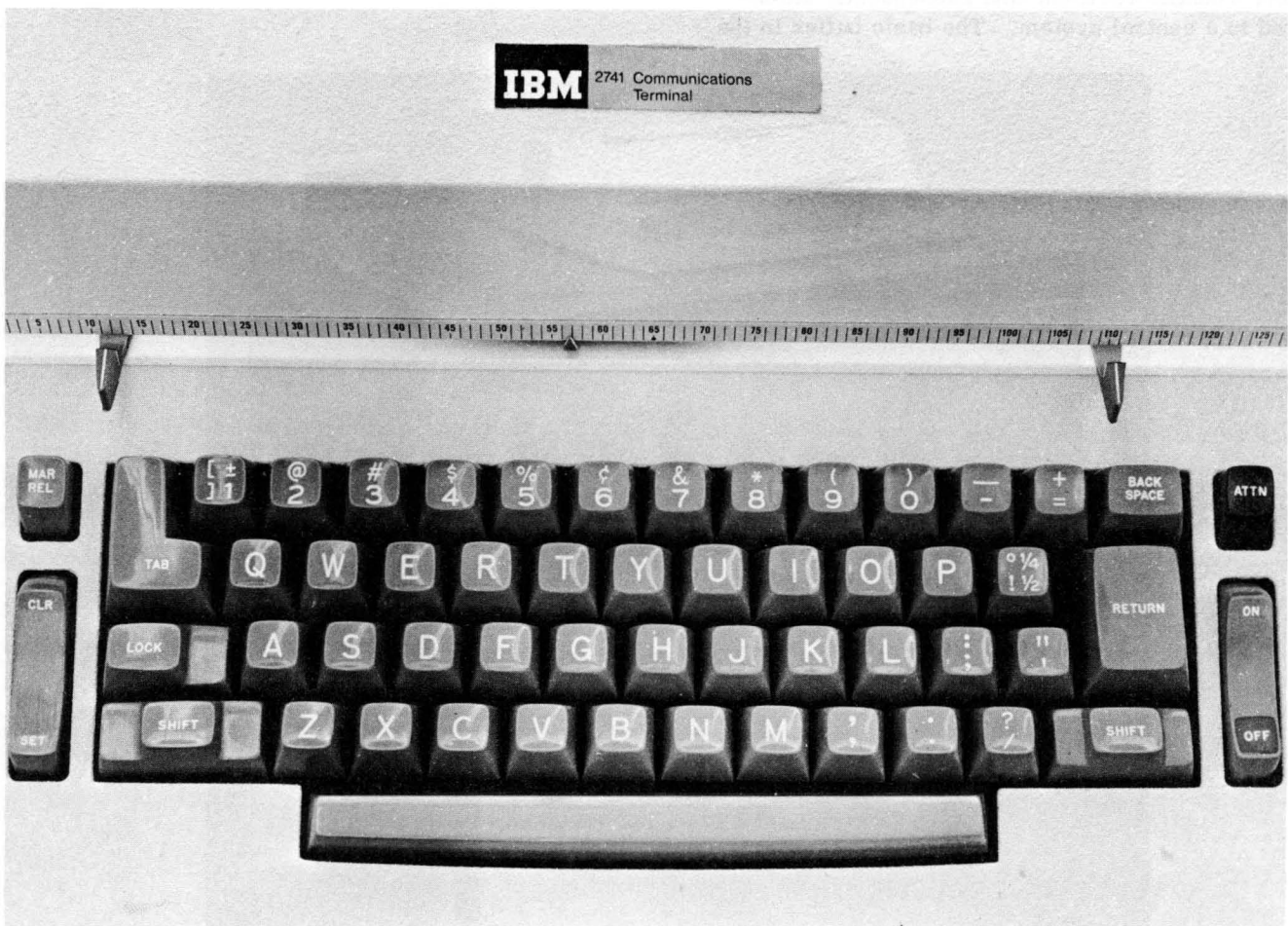
Figure 1-5 Keyboard (2741)

● Faster transmission speed.

● Visual verification before transmission.

● Clean copy output.

● Ease in correction of keying errors.

● Automatic retransmission, if Record Checking feature is installed

● Flexibility in selection of communications facilities.

The IBM 2740 Communications Terminal Model 2 is a buffered version of the 2740 Model 1. Model 2 (Figure 1-6) enables key input from the typewriter keyboard (Figure 1-7) to be printed, stored in a buffer, visually verified, and subsequently transmitted to a central system. The basic buffer in the Model 2 can accommodate up to 120 characters (248 and 440 positions are available as special features), and is capable of reading out without destroying its contents.

The 2740 terminal (without special features) transmits over leased common-carrier or privately owned communications facilities at the rate of 14.8 characters per second (134.5 bits per second). Station control is a standard function in the basic 2740 terminal. The line-control characters used by the Model 1 remain unchanged for the Model 2.

Model 2 is designed to be used in a wide variety of applications, such as: payment entry, journal entry, inquiries, administrative messages, file updating, and renewals. The terminal can also be used off-line for normal typewriter applications.
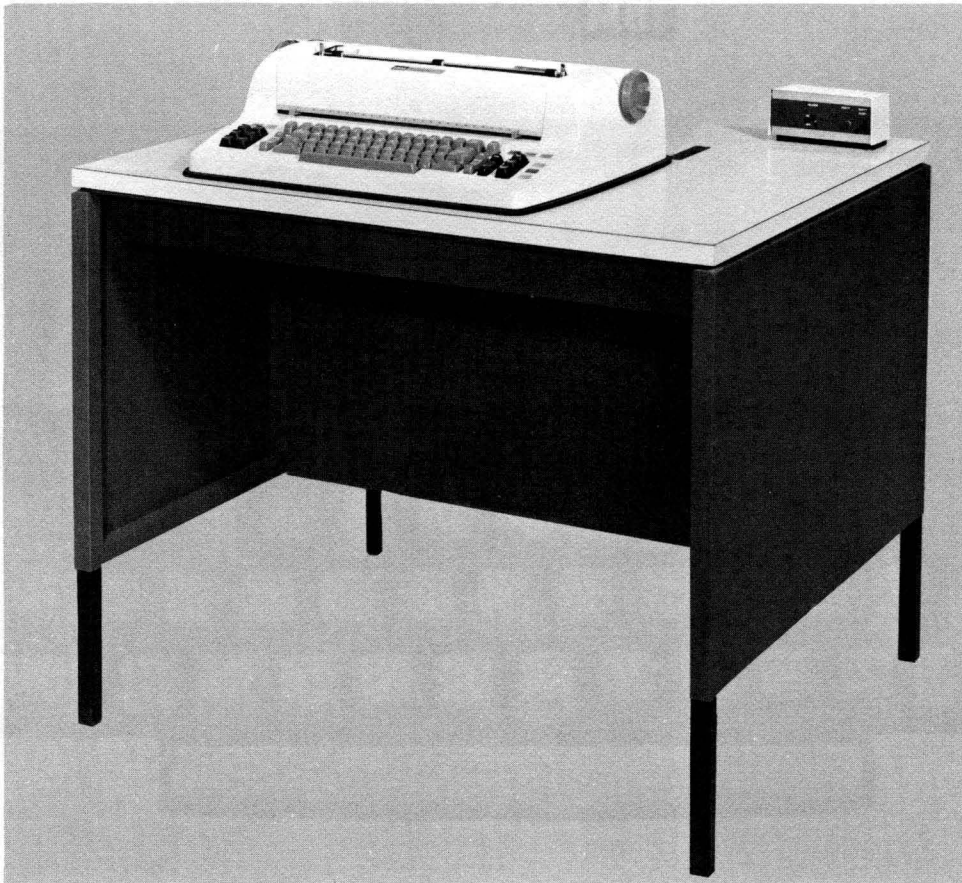
Figure 1-6 Communication Terminal (2740-2)
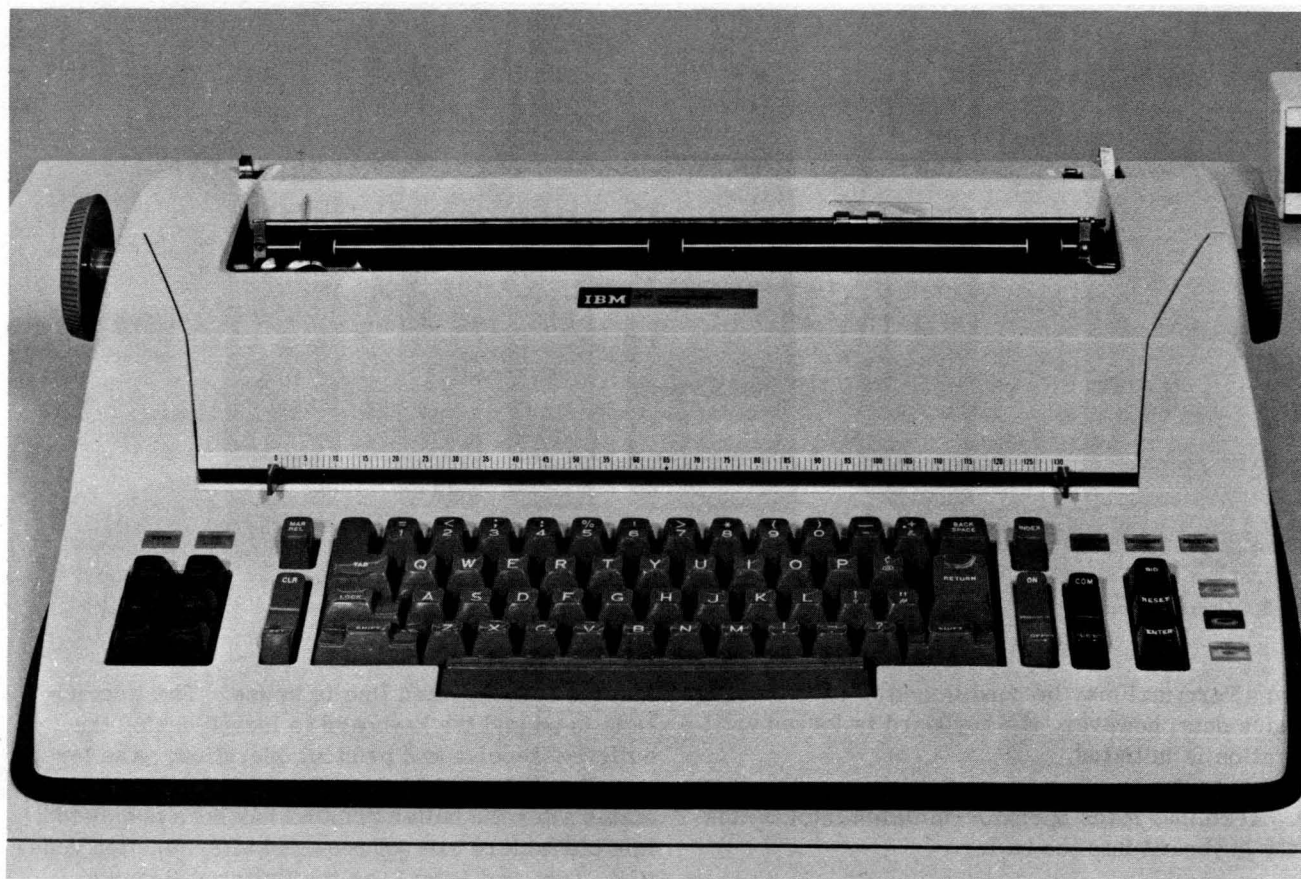
Figure 1-7 Keyboard (2740-2)

The operation of the Model 2 is basically the same as the Model 1, with the following changes (see Figure 1-8) :

- Addition of Enter key (in location formerly occupied by Dial Disc key).

- Addition of Attention light

- Addition of Enter light (in location formerly occupied by Dial Connect light)

- Elimination of EOB key

- Elimination of EOT key

- Elimination of Dial Disc key and Dial Connect light in the Model 2

- RST (Restart) key renamed Reset key

- RST (Restart) light renamed Reset light

- Additional functions of Bid key

MODES OF OPERATION

The IBM 2740 Model 2 can operate in either local or communicate mode.

Local

In local mode, the terminal will be in one of three status conditions:

Enter. Keyboard-entered data will be loaded into the buffer.

Buffer Print. The contents of the buffer will print out with each operation of the Bid key.

Typewriter. The terminal may be used for normal office typing without entering or affecting the buffer (Enter key not operated prior to typing).

Communicate

When operating in communicate mode, the terminal will be in one of five status conditions:
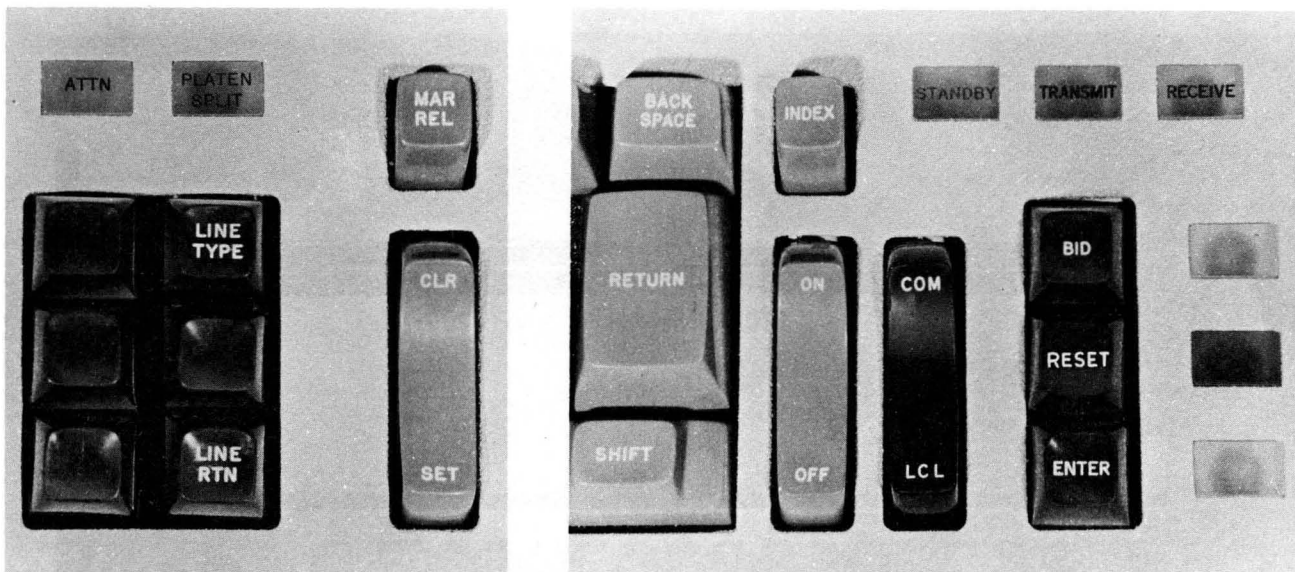
Figure 1-8   Operator Controls

Standby: Terminal may be conditioned to enter, send or receive data; however, the keyboard is locked until an operation is initiated.

Enter.   Terminal loads operator-initiated information from the keyboard into the buffer.

Bid.   Operator has pressed the Bid key and terminal is waiting to be polled in order to transmit the data residing in the buffer.

Transmit.   Terminal transmits the data from the buffer to the communications line, after being successfully polled.

Receive.   After being successfully addressed, the terminal receives data from the communications line and prints the received data.

SPECIAL FEATURES (2740-2)

Buffer Expansion

The buffer capacity can be increased from 120 to 248 or 440 characters.

Buffered Receive

This feature permits the 2740-2 terminal to receive data into the buffer from the communications line. A printout of the buffer takes place after the message is received and stored, thereby reducing the time

that the transmission line is in use.   The Receive light is on and the keyboard is locked during the buffered-receive and printout operation.   The terminal switches from a receive status to a standby status after the buffer printout has been completed. Idle characters are not required after function codes (CR, Tab, and Index), as the Buffered Receive feature will stop for the function to be completed before continuing the printout.   This reduces the number of characters to be transmitted.   The length of transmission cannot exceed the capacity of the buffer (120, 248, or 440 positions).   If a buffer overflow occurs, the Reset light turns on.   The buffer receive feature must be installed with any high speed line adapter or data set.

Telegraph Line Adapter

This feature provides an adapter that enables the 2740-2 to be used with a 75-bps leased private-line telegraph service.   With this feature, the terminal can operate over leased common-carrier or equivalent privately owned 75-bps telegraph channels. When using this feature, the transmission rate is 8.33 characters per second (cps).

Speed Base--600 bps

This feature provides for operating over leased common-carrier private-line telephone serive or equivalent privately owned facilities at 600 bps (66.7 cps).   The Buffered Receive feature is a prerequisite.

Header Control

This feature allocates up to 28 positions of the buffer for storing repetitive header information. Starting with position 1, increments of four positions (up to 28 maximum) are assigned during installation. A Header switch controls operation. With the Header switch in the OFF position, data typed at the keyboard can be entered into the header area of the buffer (Enter key operated). This data is available every time the buffer reads out to the line. Changes in data in the header area of the buffer must be made by retyping the entire area. Once header data has been entered, turning the Header switch to the ON position allows subsequent data entered to automatically start at the end of the header area of the buffer. Transmission will be from the beginning of the header area to the end of information stored in the buffer. All positions of the header area must be filled with characters and/or spaces. If the terminal power is turned off, the buffer information will be lost. Data keyed into the buffer (including the header area) can be printed out for verification by entering the data while in local-enter mode (with Header switch in OFF position) and pressing the Bid key after all data has been entered. If the Buffered Receive feature is installed, the positions used for header control are not available to receive data from the line when the Header switch is set to the ON position.

Edit

The Edit feature, which simplifies the correction of typing errors entered into the buffer, is controlled by the following keys:

Enter Key. Pressing this key while in the enter mode causes the buffer address to be reset to the first position and the terminal to remain in enter mode.

Line Type Key. The Line Type key is operative only in enter-local or enter-communicate mode. Operating this key immediately after the buffer is restored to position 1 by the Enter key causes the buffer to print out to and perform the next carrier return stored in the buffer. The Line Type key becomes inoperative after typing a character or reaching the character where the Enter key was operated.

Line Return Key. This key is operative only when the terminal is in the enter-local or enter-communicate mode. Pressing the Line Return key immediately following the use of the Line Type key or a

keyboard operation causes the buffer to back up and erase all characters up to and including, the first character of the present line.

Edit Operation

If an error occurs in the present line of typing, the correction procedure is as follows:

1. Press CR/LF key (moves print element to left margin and next line).
2. Press Line Return key to back up the buffer to the beginning of the line.
3. Rekey the entire line.

If the error is not in the present line of typing, the correction procedure is as follows:

1. Press CR/LF key (moves print element to left margin and next line).
2. Press Enter key (restores buffer to position 1). This is the second operation of the Enter key since this key was operated to put the terminal into enter mode before typing was started.
3. Press Line Type key. Advance the buffer line by line until the end of the line to be corrected is reached.
4. Press Line Return key.
5. Retype the line in error and all succeeding lines of the message.

The stored information can be verified by switching to local mode and pressing the Bid key or by repeating the Line Type operation. This causes the contents of the buffer to be printed. If the message is correct, switch to communicate mode and press the Bid key. Transmission occurs when the terminal is polled.

Document Insertion

The Document Insertion feature provides a means of inserting ledger cards in front of the typewriter platen without using the platen knobs.

Operation

To insert ledger card, push down on the Release button (Figure 1-9, Part A) and simultaneously pull the post toward the front of the terminal (Part B). When the card guide is tilted forward, the feed rolls are opened and the card can be inserted (Part C).

After the card is inserted, the guide can be moved toward the rear of the machine. The card can still be moved at this time, and can now be positioned for

Document Insertion-Release Button

Line-Position Indicator
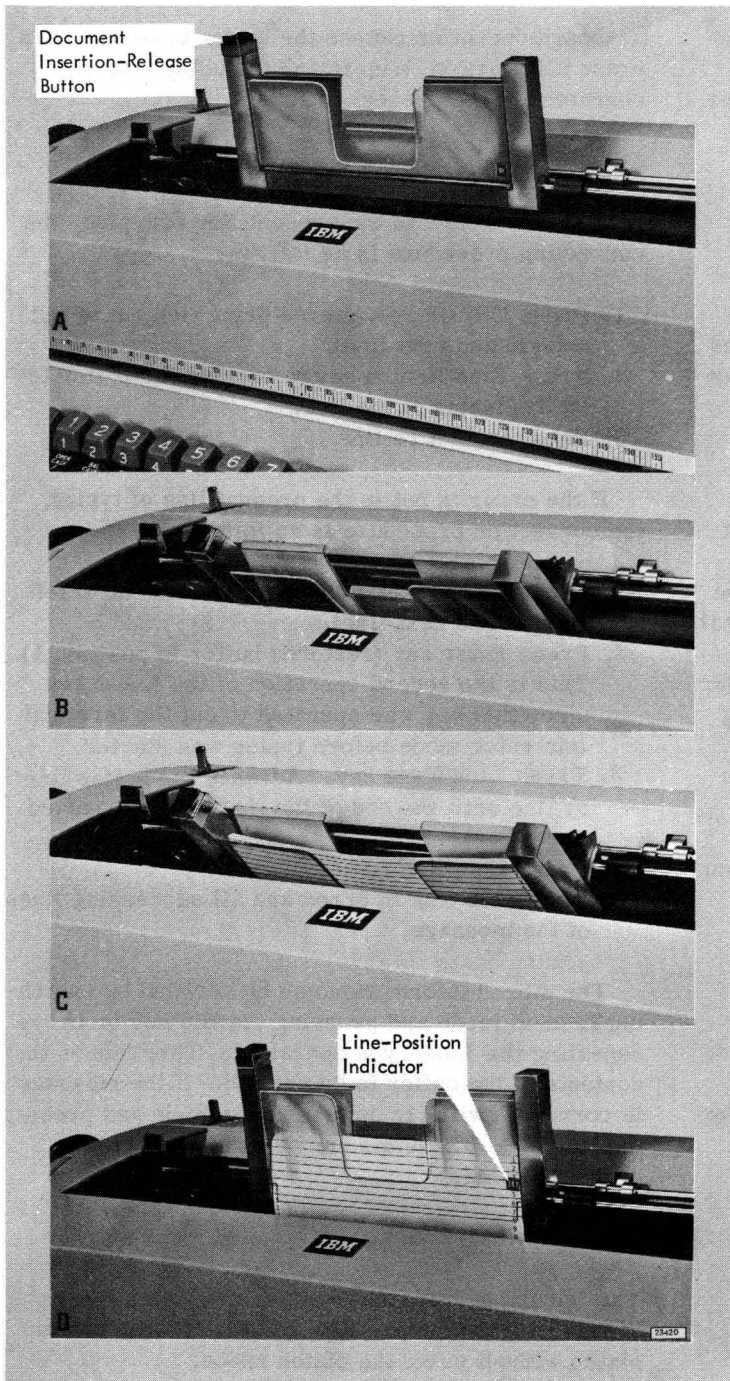
Figure 1-9   Document Insertion Feature

printing using the Line-Position indicator located on the plastic guide (Part D). The guide is locked in position by again pushing down on the Release button. The feed roll mechanism closes the feed rolls and the card is held securely in place, ready to receive the printed data. An interlock locks the keyboard when the guide is not in home position.

Split Platen

A Split Platen is available to further enhance the forms-handling capability of the IBM 2740-2 terminal (provided the Document Insertion feature is installed). The two sections of the platen may be manually disengaged by pulling the left platen knob. The sections will remain disengaged until the left platen knob is manually pushed in. When the platen is split (disengaged), only the right-hand portion will be indexed by the Index key, the CPU, or the platen knobs. When the platen is not split (engaged), both sections are indexed in the normal manner. The platen is split so that 5 1/2 inches of the printing line is available on the left-hand portion. The print position that would print directly on the split in the platen should not be used since it may not be legible.

The Platen Split indicator light, located to the left of the keyboard, is on whenever the platen is in a split condition. The keyboard locks while the platen is split, and unlocks when the platen is restored to normal (engaged).

Record Checking

The Record Checking feature for the 2740-2 is the same as for the 2740-1.

DATA REPRESENTATION

- Data is represented in the 2740-1 and 2740-2 by by BCD code.

- Data is represented in the 2741 by correspondence code.

- The check bit maintains odd parity for checking.

The 2740-1 and 2 use Binary Coded Decimal (BCD) system (Figure 1-10). Which consists of six information bits and a check bit arranged as follows:

B	A	8	4	2	1	C
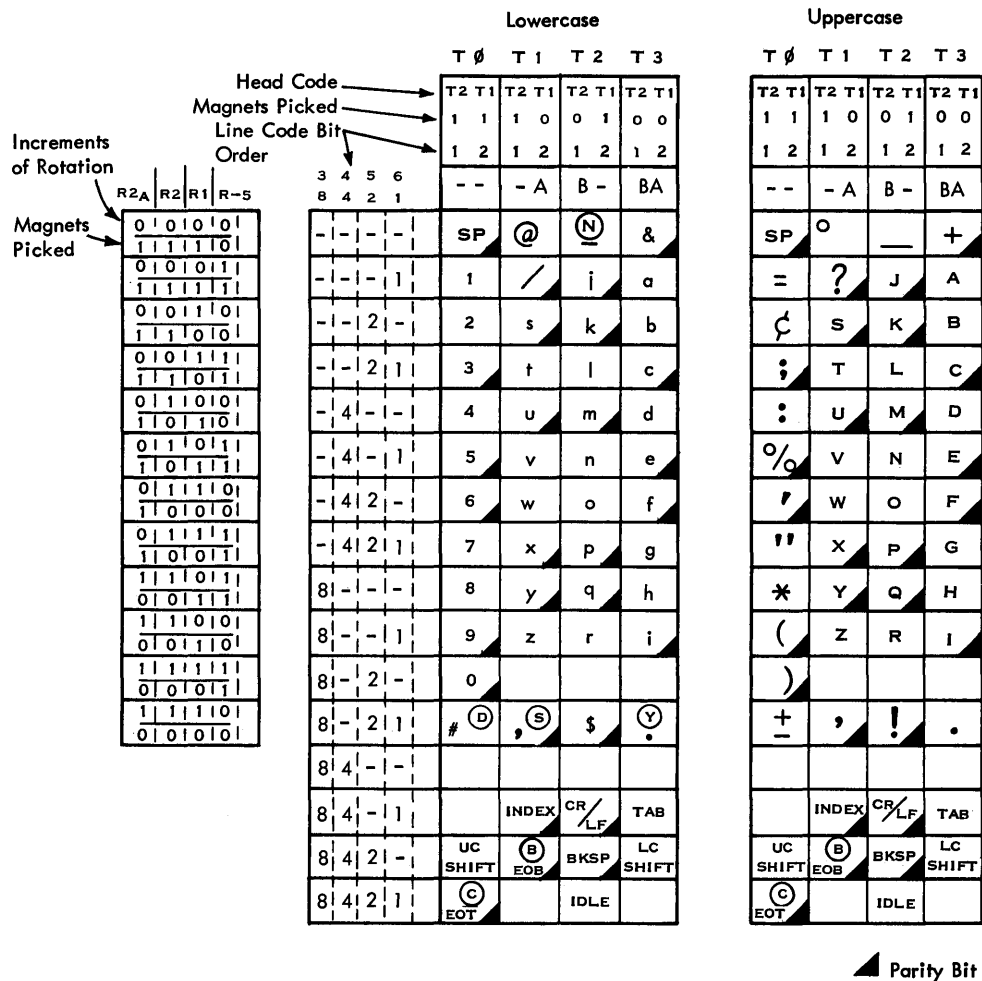
Figure 1-10 2740-1/2740-2 Printer Code Conversion

The six information bits (B, A, 8, 4, 2, 1) identify all alpha-numeric characters for the Selectric I/O as well as all control codes needed to maintain semi-automatic operation during communication. The check bit maintains odd parity. A valid character contains an odd number of bits; any character code that is not odd is given a check bit.

A 2740 character, generated by the transmit contacts in the I/O device, is translated into BCD before leaving the I/O device. This is accomplished in a diode matrix in the I/O device. The BCD code, as received from the line, is used throughout the 2740 and is decoded into the proper tilt and rotate, or function code, necessary to operate the I/O device. Upon special request, the 2740 (Models 1 and 2) can be equipped for correspondence code (Figure 1-11).

The 2741 uses correspondence code. The 2741 sends and receives characters in the same bit order as the 2740. However, the bit configurations for the same characters are different. For example, the

letter "A" in the 2740 is a BA1; in the 2741 the bit configuration for the letter "A" is a B421. Upon special request, the 2741 can be equipped for BCD code.

Mechanical changes to the I/O device are required to change from BCD code to correspondence code, and vice versa. No circuit changes are required.

Character Format

● The start of a 2740/2741 character is identified with a start (ST) bit and the end with a stop (SP) bit.

● The start bit is always a 0-bit (no-bit).

● The stop bit is always a 1-bit (bit).

A BCD character consists of seven data bits. In order to use this character as the input or output of the terminal, it is necessary to add two bit positions to the character
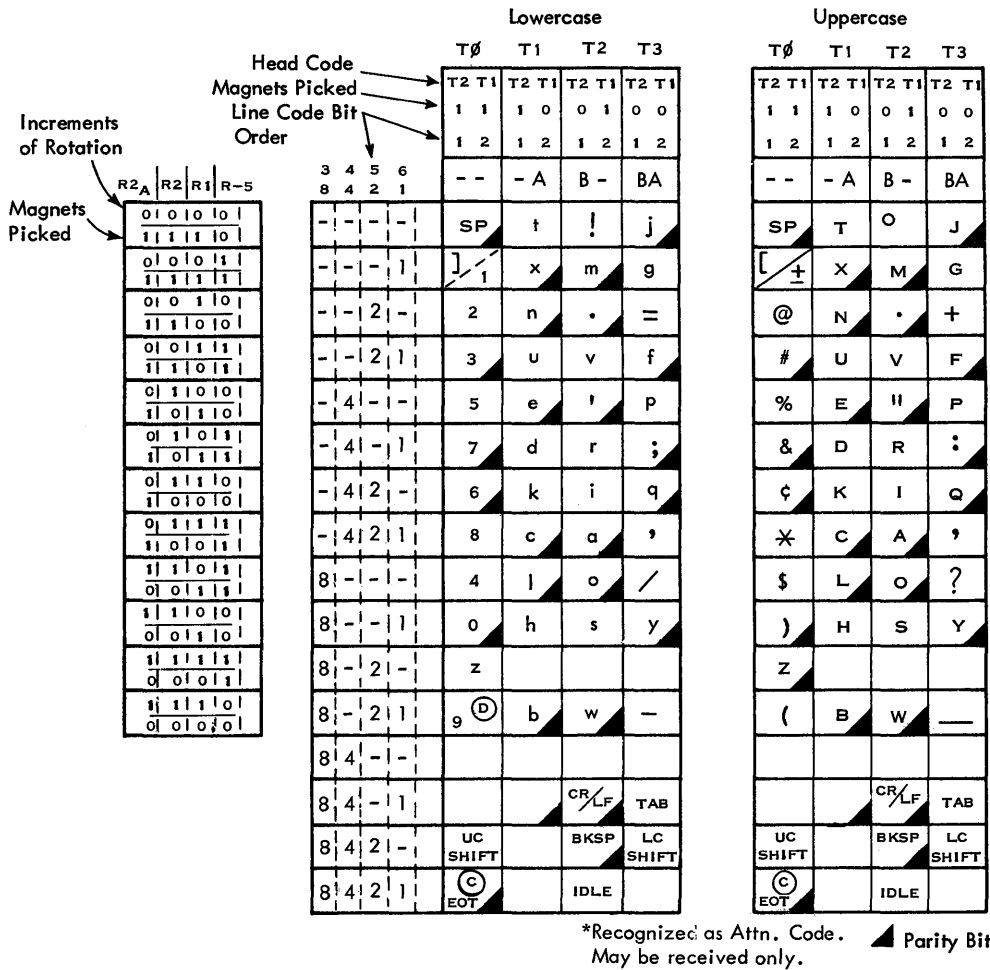
Figure 1-11 2741 Printer Code Conversion (Correspondence)

Increments of Rotation (Line Code Bit Order)				Lowercase T0 (--)	Lowercase T1 (- A)	Lowercase T2 (B -)	Lowercase T3 (BA)	Uppercase T0 (--)	Uppercase T1 (- A)	Uppercase T2 (B -)	Uppercase T3 (BA)
3/8	4/4	5/2	6/1								
-	-	-	-	SP	t	!	j	SP	T	o	J
-	-	-	1	]/1	x	m	g	[/±	X	M	G
-	-	2	-	2	n	•	=	@	N	•	+
-	-	2	1	3	u	v	f	#	U	V	F
-	4	-	-	5	e	'	p	%	E	"	P
-	4	-	1	7	d	r	;	&	D	R	:
-	4	2	-	6	k	i	q	¢	K	I	Q
-	4	2	1	8	c	a	'	*	C	A	'
8	-	-	-	4	l	o	/	$	L	O	?
8	-	-	1	0	h	s	y	)	H	S	Y
8	-	2	-	z				Z			
8	-	2	1	9 (D)	b	w	-	(	B	W	—
8	4	-	-								
8	4	-	1			CR/LF	TAB			CR/LF	TAB
8	4	2	-	UC SHIFT		BKSP	LC SHIFT	UC SHIFT		BKSP	LC SHIFT
8	4	2	1	C EOT		IDLE		C EOT		IDLE	

*Recognized as Attn. Code. May be received only.
◢ Parity Bit

the start bit (ST) and stop bit (SP). The start bit will always be a space (no-bit) and the stop bit will always be a mark (bit).

The start bit is added to the character so that the terminal can recognize the start of a new character. The stop bit separates characters.

ST	B	A	8	4	2	1	C	SP
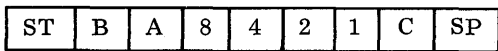
DATA FLOW (2740-1/2741)

● Transmit data flow is from the I/O device to the 1B-register, to the S-register, and then to the line.

● Receive data flow is from the line to the S-register, to the 1B-register, to the 2B-register, and then to the I/O device.

● The 2B-register is not used for sending operations.

● Control characters are identified at the 1B-register.

Data flow through the 2740-1/2741 is shown in Figure 1-12. With the terminal in transmit mode, a data character is generated from the keyboard of the I/O device and loaded into the 1B-register. From the 1B-register, the character transfers to the S-register where, under control of the serdes clock, the parallel character is serialized (changed from parallel to serial form) out to the communication line. The serialized character goes through the data-set adapter within the terminal, to either a common-carrier data set or a built-in IBM modem and then to the line.

With the terminal in receive mode, a character is received in serial form from the line by the data
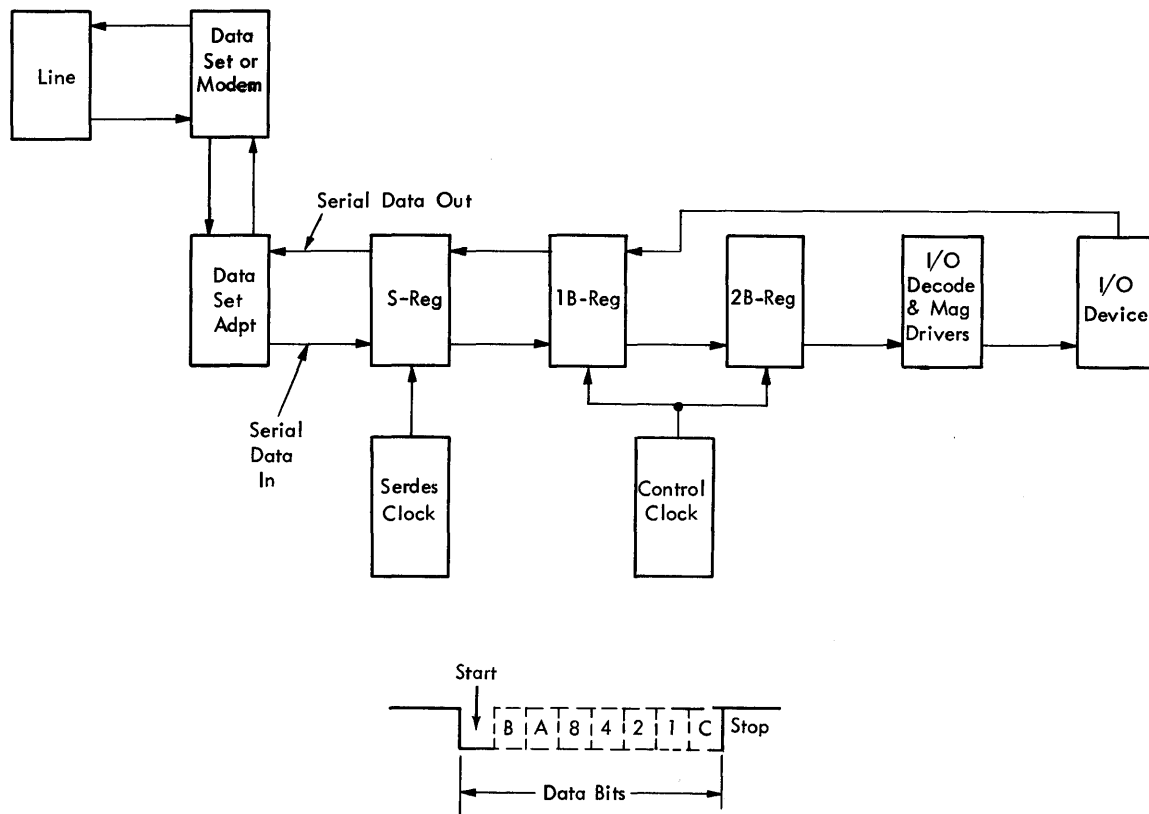
Figure 1-12 2740-1/2741 Data Flow

set or modem. The character passes through the data-set adapter and is serially loaded into the S-register under control of the serdes clock. When the character has been completely deserialized (changed from serial to parallel form) by the S-register, the control clock gates the character into the 1B-register and then into the 2B-register. While in the 1B-register, the character is examined to see whether it is a control character. If it is, the character does not transfer to the 2B-register, but performs the necessary control operation.

Once the character reaches the 2B-register, it is examined to determine whether it is a print or function character. If it is a print character, the character is gated to the print-decode circuit and then to the I/O device to be printed. If the character is a function character, the character is gated into the function-decode circuit and from there into the I/O device to perform the function. The 2B-register is used only for receiving operations.

In summary, the received serial character is deserialized by the S-register, under control of the serdes clock. Then, under control of the control clock, the character transfers from the S-register

to the 1B-register and then from the 1B-register to the 2B-register, and on to the I/O device. With the terminal in transmit mode, the parallel character is loaded directly into the 1B-register, transferred to the S-register, serialized, and sent out on the line.

DATA FLOW (2740-2)

The 2740-2 Communication terminal is basically a 2740 with buffer storage.

All functional units contained in the 2740-1 are used in the 2740-2 terminal, but because of the addition of buffer storage, the data flow is different. The following explanation describes the basic data flow for each operation.

Enter (Figure 1-13)

Pressing the Enter key places the terminal in the enter mode and allows the operator to key in an input message. The buffer is restored to the first character position, the typewriter motor turns on, and the keyboard unlocks and shifts to lower case.

As the operator enters the message, the I/O prints each character. The individual characters are transferred to the 2B-register and then bit-by-bit to the control unit buffer. Figure 1-13 shows the enter data flow.

Each time the operator presses a key on the I/O printer, the contacts transfer the bit configuration of the character representing the key pressed. This bit configuration (character) is transferred to the 2B-register. From the 2B-register, the character is "scanned" bit-by-bit into buffer storage. Buffer storage then advances to accept the next character. This process continues until the entire message is entered into buffer storage. Typewriter functions (tab, carrier return, upper or lower case shift, index) are entered into buffer storage as characters. The backspace function is not entered into storage as a character, but instead, causes buffer to back up one position. This allows correction of a typing error immediately after it occurs.

As each character is entered into buffer storage, a parity check is made to ensure that an odd number of bits is present for the character. An out-of-parity character causes a data check condition (the keyboard locks and the reset light turns on).

Enter Timeout

The 15-second time-out circuit is active during enter operation if the terminal is in communicate mode and the circuit is enabled. The circuit is enabled by the first transmit answerback after the terminal is turned on. The purpose of the enter time-out is to assure that the terminal will be available to receive messages if the operator inadvertently leaves the terminal in enter mode or if there is too great a time lapse (15 seconds) between two consecutive operator actions during communicate-enter operations.

When the time-out occurs, a reset line is brought up to reset the buffer, reset the rekey latch (if set), turn off the Reset light (if on), and return the terminal to not enter status. The same time delay and time-out circuitry is also used for power-on garble or terminal "hang up" conditions.

Transmit (Figure 1-14)

When the input message is complete, the operator presses the Bid key to request that the stored information be transmitted to the central processor. If the terminal is in upper case when the Bid key is pressed, the character code for lower case is entered into the next position of buffer and the keyboard shifts to lower case.

The terminal enters a ⓒ (ⓑ with Record Checking) into the buffer position after the last message

character and the terminal "bids" for the line. When the terminal is polled, it switches to transmit mode, sends a ⓓ as a reply to the poll, returns the buffer to the first position, and begins transmitting the contents of the buffer (Figure 1-14).

Each character from buffer storage is "scanned" into the 1B-register. From the 1B-register, the character is transferred to the S register and shifted serially by bit to the communication line exactly as in the 2740-1 terminal.

Receive (Figure 1-15)

The 2740-2 Communication Terminal, without the Buffered Receive special feature, receives and prints an incoming message from the central processor like the 2740-1 terminal. The data, received serially by bit from the communications line, is shifted into the S-register (shift register). From the S-register the character transfers to the 1B register, then to the 2B-register and finally is decoded and sent to the I/O printer.

Buffer Print (Figure 1-16)

When the Local/Communication switch is at Local the terminal can print out the contents of buffer storage. If the data was entered while in communicate mode and the terminal is then switched to Local, pressing the Bid key causes the message to print out. Data can also be entered while the terminal is in Local. The procedure is the same as when in communicate: the Enter key is pressed, the message is typed, and the Bid key is pressed. Instead of being transmitted, however, the message is printed out. When the complete message has been printed out, the terminal returns to enter mode and more data can be typed. The terminal is taken out of enter when the Reset key is pressed.

The characters are taken, one at a time, from buffer storage and loaded into the 2B-register. Once in the 2B-register, the characters are decoded and printed the same as for a receive operation.

BUFFER STORAGE

The 2740-2 does not immediately transmit information entered from the I/O keyboard but stores the input, character-by-character, in buffer storage. The term "buffer" describes the ability to store characters at high or low speed and later read out these characters at a uniform rate. The character rate from the I/O printer is not uniform, and is not the same as the character rate of the communication line. Storing data characters in the buffer allows the buffer to read out and transmit these characters

Figure 1-13 Enter Data Flow
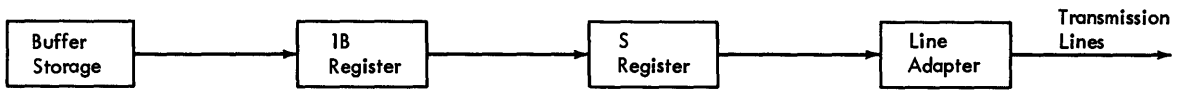
Figure 1-14 Transmit Data Flow (2740-2)

Figure 1-15 Receive Data Flow (2740-2)
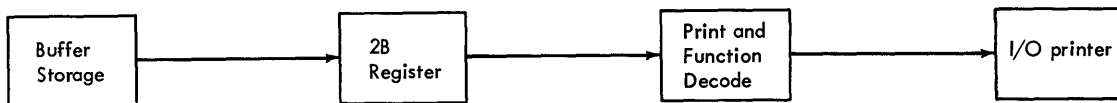
Figure 1-16 Buffer Print Data Flow (2740-2)

at a constant rate--the speed of the communication line. Thus, input can be at the operator's speed (which varies), and not interfere with efficient use of the communication line.

Storage Operation

Buffer storage receives input from the 2B-register and delivers output to the 1B-register or the 2B-register (Figure 1-16). There are three operator controls over buffer storage (Figure 1-8): Enter (which causes storing), Reset (which cancels Enter and effectively clears buffer storage), and Bid (which causes readout to the communication line or to the I/O printer). The sequence for sending a message is:

1. Press the Enter key until the Enter light comes on. If the I/O printer is in upper case, it automatically downshifts.
2. Type message information on the I/O printer keyboard. Each character is entered into buffer storage as it is typed (Figure 1-17).

   (a) In case of a typing error, backspace and retype the incorrect character. The backspace code is not stored.
   (b) If an I/O printer function is erroneously keyed, backspacing effectively erases the function character in buffer storage but does not place the carrier or paper in the correct position to continue typing (Figure 1-18).

(c) One backspace operation effectively erases a stored function code (shift, tab, CR, or index). Instead of backspacing when an entry error involves a function, start over. Press the Reset key and then the Enter key to start over.

3. Press the Bid key. If the I/O is in upper case, it automatically downshifts and the LC shift code stores. The stop code Ⓒ (Ⓑ with Record Check) stores automatically.

   (a) When in communicate the 2740-2 waits for a poll and sends the message (Figure 1-17).
   (b) When in local, the I/O prints out the stored information and stops where the stop code character is (Ⓒ or Ⓑ) stored (Figure 1-17). The Enter light comes on again. The operator has three choices:

      (1) Continue entering from the I/O keyboard. (A downshift will be the last stored character if the last printed character was in upper case.)
      (2) Clear buffer storage and start over.
      (3) Send the message by going to communicate and pressing the Bid key.

Character Storage Concepts

The optional capacities of buffer storage are 128, 256, or 448 characters; however, because the I/O
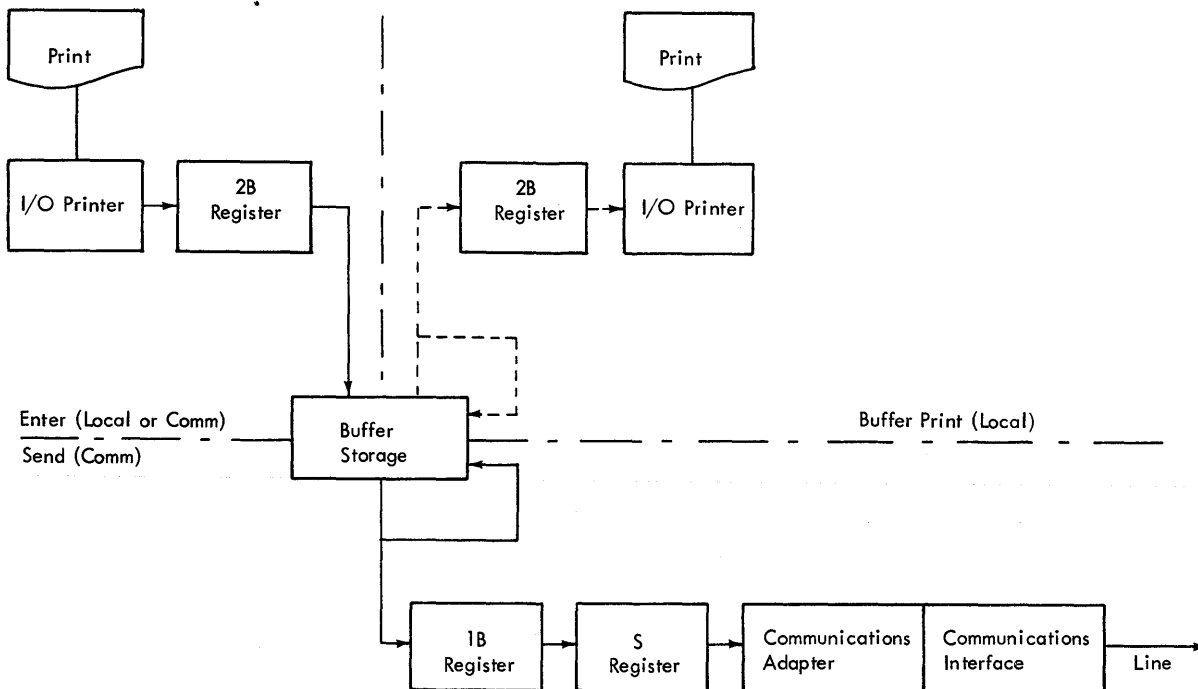
Figure 1-17 Overall Flow of Outgoing Message (2740-2)

keyboard locks 8 characters from the end of memory during an enter operation, the usable capacity is 120, 248, or 440 characters. Consider buffer storage as an assembly of locations where information can be placed. Each of the locations has a specific designation called its address (Figure 1-18). Storing and retrieving is done sequentially.

It can be seen that buffer storage requires the following to do its job:

1. Locations for storing characters (cores).
2. Identification of character locations (address).

3. A way to put a character in or take it from a location (store or read-out).
4. A method of clocking so that information is always stored on time when entering, or made available on time when sending (memory clock).

In the 2740-2, magnetic core storage provides all these capabilities (Figure 1-19).

Each 2740-2 buffer character is made up of 7-bits. Each bit requires one magnetic core, so there are 128x7=896, 256x7=1792, or 448x7=3136

Enter and carrier return, then type — — R. U. Jones   984030Y — — Printout or send

Margin   Tab Stop

Note: Press Bid Key after "Y" is Keyed.

Character address	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
Stored in buffer storage	CR	UC shift	r	.	sp.	u	.	sp.	i	LC shift	o	n	e	s	tab	9	8	4	0	3	0	UC shift	y	LC shift	End

Note: Backspace backs the carrier one space and backs buffer storage one character location.

Figure 1-18 Comparison of Typed and Stored Message
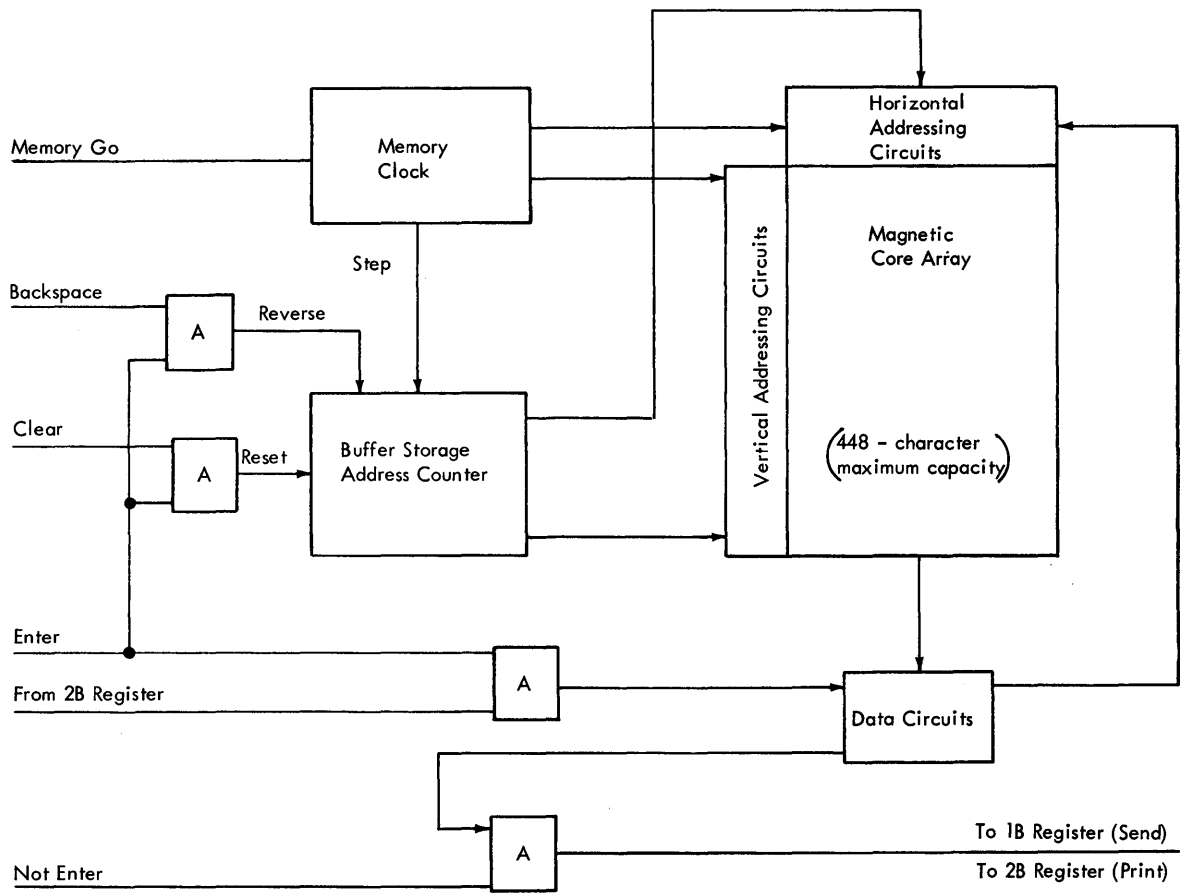
Figure 1-19 Buffer Storage
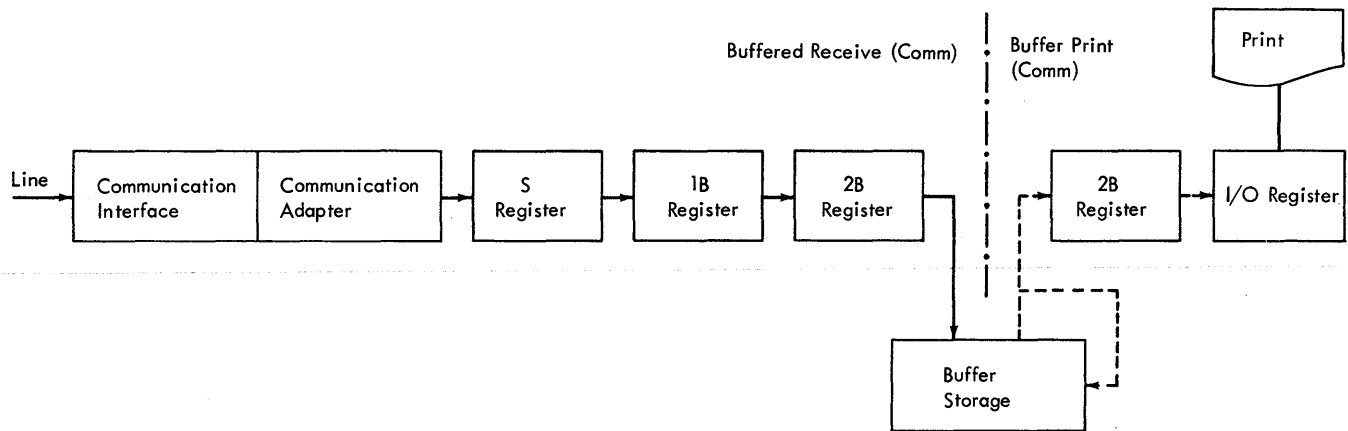
Figure 1-20 Overall Flow of Buffered Receive Incoming Message

cores in the core array. The methods of entering characters into the cores or retrieving characters from the cores are described in the "Buffer Storage" section of "Chapter 2, Functional Units."

Buffered Receive Feature

During receive the received characters are entered into buffer storage from the 2B register and printing is inhibited (Figure 1-20). As soon as the message is complete, the contents of buffer storage are read out and the I/O prints the message. Buffer storage can operate much faster than the electro-mechanical I/O printer, so a faster line rate can be used with buffer storage on-line than with the printer on-line.

With a Buffered Receive terminal, (Figures 1-17 and 1-20), there are four basic data flow routes at three character rates, as shown in the following table:

Operation	Data Flow	Rate
Enter	I/O⟶2B⟶Buffer storage	Typing--variable and slow
Transmit	Buffer storage⟶1B⟶S⟶line	Communication line--relatively fast
Receive	Line⟶S⟶1B⟶2B⟶Buffer storage	
Buffer Print	Buffer storage⟶2B⟶I/O	I/O printer--maximum printing speed

TRANSMIT STATUS/ANSWERBACK (2740-2)

- Two character answerback to addressing sequence sent by 2740-2 (sense character and Ⓝ or Ⓨ).

- Four error conditions stored by the terminal for the qualified Ⓨ answerback (Figure 1-21).

- Program has the option to have messages retransmitted when errors exist.

- Three status and three operational error conditions transmitted as a qualified Ⓝ (Figure 1-21).

When addressed by the CPU, the 2740-2 responds with a two-character answerback. The first character is a "sense character" for a specific definition of the terminal status or error condition. The second character is a Ⓨ if there is receive status or a Ⓝ if there is not receive status.

Four types of failures are detected and stored by the 2740-2. Once the terminal (with receive status) is readressed, it responds with the two-character (qualified Ⓨ) answerback. The answerback is for the highest priority error type detected, followed by the Ⓨ. The sense character response to the CPU does not cause automatic retransmission, but it is intended for error condition statistics. For example, if a message received by the 2740-2 (without Record Checking) has an error, the CPU is not informed until the terminal is addressed again. Then, at the option of the program, the message can be retransmitted to correct the previous error condition. The CPU program has the same option when the text received by the CPU contains an error.

Four latches are used to store the four types of error conditions, each assigned a priority. In priority order, with highest first, the four conditions are:

1. Electronic hardware (buffer) error in the last message received;
2. I/O printer error in the last message received;
3. Line VRC error during the last message received;
4. A terminal-induced VRC error during the last message transmitted.

If an error condition latch has been set, it generates the sense character when a positive (qualified Ⓨ) answerback is transmitted. When multiple errors occur, the character transmitted defines only the condition which has the highest assigned priority. For a "no error" condition, a space is transmitted as the sense character.

The error condition latches are reset when the sense character of a two-character positive answerback has been transmitted. The latches are not

affected by a negative answerback. When a terminal without receive status is addressed, it transmits the qualified Ⓝ without sensing or resetting the error condition latches. Error information, existing when the negative answerback is sent, is retained until the terminal with receive status is readdressed.

A qualified Ⓝ response to addressing is transmitted by a terminal without receive status. In this case, the sense character defines the condition which causes the Ⓝ response to the addressing sequence. Three of these are considered as status conditions. They are:

1. Bid latch on.
2. In enter mode.
3. Buffer print in communicate mode.

For the first two conditions, it is assumed that a message is being prepared. Thus, the program should continue with other processing and poll the terminal for the message before readdressing it. For buffer-print-communicate mode, the program should continue with processing and readdress the terminal later.

Three other conditions are considered to be operational error (rather than status) conditions because they require operator intervention before the terminal is ready for operation. They are:

1. Terminal in local mode.
2. Ready except out of paper.
3. Ready except document device down.

When the addressed terminal responds with the qualified Ⓝ the Attention light comes on and the alarm sounds to alert the operator. Regaining status causes the Attention light to turn off again.

If the terminal is polled or addressed when the terminal or data set has power turned off, there is no response to the CPU. However, the CPU times out and it should post this as an error condition to the user.

2740-2 With Receive Status Addressed by CPU	
Error Condition	Answer Back
No Error Stored	Space Ⓨ
Electronic Hardware	/ Ⓨ
I/O Error Received	S Ⓨ
Parity Error Received	U Ⓨ
Parity Error Trans.	Y Ⓨ

2740-2 Without Receive Status Addressed by CPU	
Terminal Status	Answer Back
Enter Communicate	1 Ⓝ
Bid Latch On	2 Ⓝ
Bfr. Print Comm.	4 Ⓝ
Local Mode	8 Ⓝ
Out of Paper	9 Ⓝ
Document Device Down	@ Ⓝ
Power Off	None

Figure 1-21. Transmit Status Answerback Characters

S-REGISTER

● Converts parallel bits to serial (serialization).

● Converts serial bits to parallel (deserialization).

● Has a trigger for each of the BCD bits and the start and stop bits.

● Receives data from: (1) the 1B-register when the terminal is sending, (2) from the 'serial data in' line when the terminal is receiving.

All data entering or leaving the 2740/2741 is in serial-by-character, serial-by-bit form. To be usable in the terminal, the data must be in parallel-by-bit form. Therefore, data must be converted from serial to parallel form for a receiving operation and vice versa for a sending operation. The conversion processes, which are called serialization and deserialization, are performed by the S-register (shift register).

The S-register consists of nine triggers--one each for the start, B, A, 8, 4, 2, 1, C, and stop bits--and the appropriate gating circuits (Diagram 4-1). The S-register is loaded with data from either the 1B-register (sending) or from the 'serial data in' line (receiving).

Serialization (Sending)

During sending operations, data from the I/O device (or buffer, Mod 2) transfers to the 1B-register. From the 1B-register, the data is loaded into the S-register and serialized to the 'serial data out' line. The data transfers from the S-register in parallel-by-bit form.

Before receiving the character from the 1B-register, the S-register is restored by turning all triggers on. To load the character then, those triggers that represent a no-bit in the character must turn off.

Seven ANDs form the transmit-mode input to the S-register. One input to each of these ANDs is conditioned by the absence of a bit in the associated position of the 1B-register. The common gating line, 'S0 reset,' completes conditioning the ANDs, causing the character in the 1B-register to transfer to the S-register. Bringing up "S0 reset" also turns off 'S0' and enters the start bit for the character into the S-register. 'S8' is turned on by 'S register restore.' When 'S0 reset' comes up (loading the

character into the S-register) no input is applied to 'S8, ' so the stop bit is present for the character. The entire character is now in the S-register and must be serialized to the 'serial data out' line.

Diagram 4-1 shows that each S-register trigger provides gating to turn the next trigger on or off. For example, if 'S8' is on, a gate is applied to turn 'S7' on. If 'S8' is off, a gate is applied to turn 'S7' off. If 'S7' is on, a gate is applied to turn 'S6' on. If 'S7' is off, a gate is applied to turn 'S6' off, etc. This arrangement allows a bit or no-bit condition in an upper trigger to be shifted down to the next trigger.

The bits are shifted down through the S-register under control of the 'SDAC' output of the serdes clock. The 'SDAC' pulse is applied to each of the ac-set and ac-reset inputs of the S-register triggers. Each time a 'SDAC' pulse arrives, the condition of the upper trigger transfers to the next lower trigger. As the character shifts down through the S-register, the 'S0' trigger turns on or off. The output of the 'S0' trigger is applied directly to an AND. The other line to condition this AND is 'send'. The output of the AND is the 'serial data out' line. The character, now serialized, is sent over the communication line, a bit at a time, to a terminal or multiplexer. While the character is being shifted down through the S-register, 'S8' remains off because the gate to turn off 'S8' is held up.

When the complete character has been shifted through the S-register, all triggers are off. The absence of bits in the S-register is detected, informing the terminal logic that shifting is completed.

Deserialization (Receiving)

Data arrives at the 2740/2741 on the 'serial data in' line in serial form. The S-register is restored to all triggers on before data arrives. The start bit (no-bit) arrives first and this deconditions 'AND 1' (see Diagram 4-1). By deconditioning 'AND 1, ' the gate to turn on 'S8' is deconditioned, while the gate to turn off 'S8' is conditioned. The start bit also starts the serdes clock and the first 'SDAC' pulse from the serdes clock turns 'S8' off.

For this explanation, the character "A" is used. "A" consists of B-, A-, and 1-bits; therefore, after the start bit, the next bit received is a B-bit. The condition of the 'serial data in' line now reverses, conditioning 'S8' to turn on. The next 'SDAC' pulse transfers the start bit in 'S8' to 'S7, ' and the B-bit

is loaded into 'S8.' The next received bit is the
A-bit. The 'serial data in' line remains up. The
start bit transfers to 'S6', the B-bit transfers to
'S7', and the A-bit is loaded into 'S8.' The next
received bit should be an 8-bit; since the letter "A"
is being received, however, an 8-bit is not present
(no-bit). The 'serial data in' line goes into a no-bit
condition, conditioning 'S8' to turn off. The pre-
viously received bits are again stepped down one
trigger position. This process repeats until the
entire character has been serially loaded into and
shifted down through the S-register.

When the start bit reached the 'S0' trigger, the
'S0' trigger turns off. 'S0' off and 'S8' on (presence
of a stop bit) notifies the terminal circuits that the
S-register is now completely loaded with the charac-
ter, and the character can transfer to the 1B-regis-
ter for further use.

SERDES CLOCK

● Provides clock pulses to shift data through the
  S register.

● Runs continuously for a sending operation.

● Runs only during character time for a receiving
  operation.

  For the 2740-2, one of three oscillator output
  frequencies available (300 Hz, 539 Hz, 9.6 KHz).

For data to be shifted through the S-register, a
clocking pulse must be developed. The clocking
pulse is the SDAC pulse generated by the serdes
clock. With the terminal in transmit mode, the
serdes clock runs continuously. In receive mode,
the serdes clock runs only during the time that a
character is being received. The arrival of a valid
Start bit starts the serdes clock; the generation of an
'S-register restore' pulse stops the clock.

The serdes clock consists of four triggers: 'SD1,'
'SD2,' 'SD3,' and 'SD4' (Diagram 4-2). 'SD1' pro-
vides gating to 'SD2,' 'SD2' provides gating to both
'SD1' and 'SD3,' and 'SD3' provides gating to 'SD4.'
This gating,plus the output from the oscillator,
allows the serdes clock to be cycled. Serdes clock
operation depends upon whether the oscillator is
gated or degated. If the oscillator is gated, the
serdes clock runs; if the oscillator is degated, the
serdes clock does not run. The outputs of the
oscillator are the 'SDCAC1' and 'SDCAC2' pulses.
These pulses, are applied to triggers 'SD1', 'SD2,'
and 'SD3'.

The oscillator can be gated in two ways (Diagram
4-2). (1) When the terminal is in transmit mode,

'send' holds the oscillator gated until the mode
changes. (2) When in a receiving operation, the
arrival of a start bit brings up 'not line.' If 'not
line' is up for at least half-a-bit time, 'SD4' turns
on, holding the oscillator gated until turned off by S-
register restore. 'Not mode change' prevents the
oscillator from being gated during a mode change.
Although different methods are used to gate the
serdes clock for sending and receiving operations,
once gated, the clock cycles in the same manner
for both operations. The difference is that the clock
is stopped between characters during receiving
operations. The following paragraphs describe the
cycling sequence for a receiving operation (see
Diagram 4-2).

Whenever the oscillator is not gated on, 'not
clock run' holds the 'SD1' and 'SD2' triggers off and
the 'SD3' trigger on. 'SD4' would have been pre-
viously turned off by 'S-register restore.' When the
Start bit is received, the oscillator is gated on,
developing the 'SDCAC' pulses and dropping 'not
clock run'. The first 'SDCAC2' pulse turns on
'SD1'. 'SD1' and 'SDCAC1' turns on 'SD2..' 'SD2,'
'SD3' (already on), and 'SDCAC1' turn off 'SD3.'
'SD3' turning off turns on 'SD4'. 'SD4' wraps
aroung to the input of the oscillator and takes over
the oscillator gating.

It takes half-a-bit time from the drop of the
'serial data in' line until 'SD4' turns on. If the drop
is caused by line noise, 'serial data in' generally
comes up before 'SD4' turns on and degates the
oscillator. Thus, line noise is prevented from
cycling the serdes clock and being recognized as a
character. The serdes clock continues to cycle
until the character is completely received and 'S
register restore' comes up. 'S-register restore'
turns off 'SD4,' degating the oscillator and stopping
the serdes clock. The inverted output of 'SD3' be-
comes the 'SDAC' pulse that drives the S-register.

The timing chart (Diagram 4-2) shows that the
serdes clock acts as a frequency divider of the ser-
des oscillator. Because of clock timing, the 'SDAC'
pulse comes up midway through a bit time so that
slight variations in bit-time lengths do not cause
character recognition errors.

The 2740-2 can be used with 75, 150, or 600
Baud lines (when a 150 Baud line is used, the ter-
minal actually operates at 134.5 Baud). To comply
with these operating speeds, the correct serdes
oscillator must be used. The oscillator used is
determined by the line speed. For the 75 Baud rate
(75 Baud line) a 300 Hz oscillator is used as input
to the serdes clock triggers, for the 134.5 Baud rate
(150 Baud line), a 539 Hz oscillator is used. For
the 600 Baud rate, however, a oscillator frequency
of 9.6 KHz is used. This frequency is too fast

for the 600 Baud line-rate so a frequency divider (insert of Diagram 4-2) reduces the frequency by four to 2.4 Hz before inputing to the serdes triggers. This serdes oscillator also acts as the control clock oscillator. Thus, by changing the oscillator frequencies, the 2740-2 can operate with the 75 Baud telegraph line adapter, the 150 Baud data sets or IBM modems, or with the 600 Baud data sets or IBM modems.

CONTROL CLOCK

- Provides timing for register-to-register transfers.

Once in the S-register, the character transfers to the 1B-register and then to the 2B-register. The time allowed to transfer the character is less than the time to load the S-register since a character must transfer through the registers during the time between characters. Therefore, a control clock that runs at a faster rate than the serdes clock is provided.

The control clock consists of a continually running 18 KHz or 9.6 KHz oscillator, two triggers, and associated gating circuits (Diagram 4-3). The 18KHz oscillator is used with the 75 and 150 Baud lines; the 9.6 KHz oscillator is used with the 600 Baud lines. The outputs of the oscillator, 'CC1' and 'CC2' provide the ac-set and ac-reset pulses for the two control-clock triggers. 'CC1' and 'CC2' also provide ac pulses for other triggers throughout the terminal.

When terminal power first comes up, the 'C1' trigger is turned off by 'power on reset.' 'C1' off causes 'C2' to turn off. 'C1' provides gating to 'C2;' 'C2' wraps around and provides the turn-off gate for 'C1.' To start the control clock, a gate is provided to turn on 'C1.' The AND/OR circuits at the left side of Diagram 4-3 show the gating used for 'C1.' When the gate is present, 'CC1' turns on the 'C1' trigger. 'C1' and the next 'CC2' pulse turn on 'C2.' Both 'C1' and 'C2' are now on. 'C2' and the next 'CC1' pulse turn off 'C1.' 'C1' (off) and the next 'CC1' pulse turn off 'C2.' The control-clock cycle is completed.

Each time 'C1' turns on, the clock cycles ("C chain"). The cycle ends and both 'C1' and 'C2' are off. The 'C1' and 'C2' outputs provide the timing necessary to transfer the characters from the S-register to the 1B-register (then to the 2B-register for 2740-1/2741) during receive operations; and resets the 1B-register during sending operations. As shown in Diagram 4-3, the 'C1' pulse has a duration of 50 microseconds and the 'C2' pulse has a duration of 75 microseconds

(using the 18 KHz osc); the pulse time is caused by the sequence of operation of the control-clock triggers. The control-clock 'C1' and 'C2' output sequence is:

1. 'not C1' and 'not C2'
2. 'C1' and ' not C2, '
3. 'C1' and 'C2, '
4. 'not C1' and 'C2.'

It is this sequence that allows the registers to be set and reset in the proper order and accomplishes the orderly transfer of characters from register to register.

1B-REGISTER (2740-1/2741)

- Loaded from the S-register during receiving operations.

- Loaded directly from the I/O device during sending operations.

- Control characters loaded into 1B by the '1B generate' line.

The 1B-register is the intermediate storage register for the receiving operation and the main storage register for the sending operation. The 1B-register is loaded with a character from the S-register during receive operations. During transmit operations, the 1B-register can be loaded in three ways: (1) directly from the I/O device transmit contacts (print or function characters), (2) by bringing up the '1B generate line' (control characters), and (3) by $\Diamond$ (delta) inputs for some special features (Diagram 4-4). Only the basic-terminal inputs are explained in this section.

With the terminal in transmit mode when a key is pressed on the I/O keyboard, the I/O device takes a cycle. During the cycle, the transmit contacts for the desired character transfer, and a 1B-register gating pulse develops. This gating pulse is called 'strobe.' 'Strobe' tells the terminal that the I/O device is far enough along in its cycle to correctly transfer the character from the transmit contacts to the 1B-register. Diagram 4-4 shows this input. The input from the I/O transmit contacts ('integrated printer' 1-7) partially conditions the seven 1B-register input ANDs. When the 'strobe' line comes up, conditioning of the ANDs is completed, and the desired character is loaded into the 1B-register. The character then transfers, under control of the control clock, to the S-register for serialization.

Another group of ANDs loads the control characters. When the operator presses either the EOT or the bid key, the '1B generate' line comes up. '1B generate' conditions the ANDs to the '1B3,' '1B4' '1B5,' '1B6,' and '1B7' latches. If the operator presses the Bid key, the 'not bid' line (active for every operation but bid) deconditions the ANDs to the '1B4' and '1B7' latches, and a Ⓓ character (821) is loaded into the 1B-register. If the operator presses the EOT key, the Ⓒ character (8421C) is loaded into the 1B-register. Once in the 1B-register, the control character transfers to the S-register and is serialized.

With the terminal in receive mode the 1B-register is reset before receiving a character and again after the character is transferred to the 2B-register. The input to the 1B-register is from the S-register. A group of ANDs, one for each latch, is conditioned by 'not send,' '1B set,' and the output from the associated S-register trigger. The main gating factor is the '1B-set' line. After transferring to the 1B-register, the character then transfers to the 2B-register for printing or the desired function. The dotted line in Diagram 4-4 are for special features and are discussed in Chapter 4.

1B-REGISTER (2740-2)

- Loaded from the S-register during receive operations.

- Loaded from buffer storage during transmit operations.

- Control characters except Ⓒ (or Ⓑ with R.C.) loaded by bringing up '1B Generate'.

The 1B-register receives characters from the S-register during receive operations, and from buffer storage during transmit operations. Control characters except Ⓒ (or Ⓑ with Record Checking) are loaded directly into 1B during transmit operations and do not come from buffer storage.

Control characters are analyzed while in the 1B-register to determine further terminal operations during both receive and transmit operations.

The 1B-register (Diagram 4-5) consists of seven latches, one for each of the data bits and check bit. The latches are turned on to load the register with bits from three sources: (1) the output of the S-register, (2) the output of buffer storage, and (3) by special circuits for control characters.

During receive operations, when a complete character is in the S-register, the control clock is started. The control clock outputs bring up 1B set,

which, with 'not send' and the S-register output, transfers the character to the 1B-register.

During transmit operations, the 1B-register is loaded a character at a time from buffer storage. 'Memory buffer' and the outputs from the buffer address clock, "scan" the character into the register serially by bit.

Generated Data

The control characters except Ⓒ (or Ⓑ with Record Check) are loaded into the 1B-register without passing through another register or buffer storage. The control characters are used to control the terminal mode. The Ⓒ (Ⓑ with R. C.) character is loaded into buffer from the 2B-register and ends the terminal transmit operation.

The control characters that are loaded into the 1B-register (except for the Ⓝ and sense characters) are primarily the result of bringing up the '1B generate' line. The Ⓝ character does not require '1B generate.' 'Transmit answerback' and '1B set not EOT' bring up 'initiate 1B1-B bit.' The Ⓝ is delayed until the 'not 1st status character answerback' allows the 1B1-B bit to be set as the second character of the two character answerback. The sense characters are loaded into the 1B-register primarily as a result of bringing up the 'load 1st character answerback' line.

'1B generate' is brought up in various ways and is discussed in the "Principles of Operation" section of this manual. However, it should be noted that '1B generate' is delayed for one character time to allow Ⓨ to be set as the second character of the qualified Ⓨ (two character) answerback. The controlling logic shown in Diagrams 4-5 and 5-22 is not explained here, but it is shown for servicing assistance and convenience for the reader.

2B-REGISTER (2740-1/2741)

- Stores a character until the I/O device is ready to accept it.

- Is used only for a receiving operation.

The 2B-register is the input to the print-and-function decode circuits. The received character is stored in the 2B-register until the I/O device is ready to accept the character. The 2B-register is not used for a sending operation (transmitted characters go directly to the 1B-register).

The 2B-register consists of seven latches (Diagram 4-6). During a receiving operation, characters transfer from the 1B-register to the 2B-

register. Before a character is loaded into the 2B-register, the '2B reset' line is made active to reset the entire register. The condition needed to load the 2B-register is '2B set' and 'not 2B inhibit' ANDed with the outputs of the 1B-register latches.

The '2B inhibit' line is present only on those 2740's equipped with the record-checking feature. If an error occurs, the '2B inhibit' line becomes active, blocking the transfer of a new character into the 2B-register. A special input to the '2B1' latch, '◊2B1,' turns on the latch. The presence of a bit in the '2B1' latch causes the I/O device to print a dash in place of the error character.

The output of the 2B-register is gated to the I/O device through the print- or function-decode circuits.

2B-REGISTER (2740-2)

● For receive operations, the 2B-register is loaded from the 1B-register.

● To end the enter (and later the transmit) operations, a stop code (Ⓒ or Ⓑ) is generated at and loaded into 2B and then stored in buffer storage as the last character.

● For enter operations, 2B is loaded from the output of the I/O printer transmit contacts.

● For buffer print operations (local mode or buffered receive feature) the output of buffer storage is transferred to 2B for printing on the I/O printer.

The 2B-register (Diagram 4-7) receives characters (1) from the 1B-register during receive operations, (2) from the I/O printer transmit contacts during enter operations, and (3) from buffer storage during buffer print operations. The stop code (Ⓒ or Ⓑ) is generated at 2B for storage at the end of enter operations.

During receive operations, a character received from the transmission line at the S-register is transferred from the S-register, through the 1B-register, to the 2B-register. Once the character is in 2B, the S-register is available to receive another character. Meanwhile, the character in 2B is decoded and printed. The character is loaded into 2B when '2B set' is brought up.

During enter operations, characters come from the I/O printer transmit contacts. This is accomplished during the I/O cycle when strobe comes up.

When the contents of buffer storage are to be printed, 'buffer print,' 'memory buffer,' and the memory clock outputs "scan" the character into 2B, a bit at a time. The character is then decoded and printed.

Generated Data

When the enter operation ends (Bid key pressed), a stop code is loaded as the last character in memory. This character (Ⓒ or Ⓑ) is generated by logic, and does not come from the I/O printer transmit contacts. 'Store stop code' and 'read' turn on the proper latches. The stop code then transfers to buffer storage.

PRINT AND FUNCTION DECODE, (ALL MODELS)

Print Decode

● Translates print characters to I/O code and starts a print cycle.

● Identifies print characters by a non 8-4 combination in their bit structure.

The purpose of the print-decode circuit (Diagram 4-8) is (1) to decode the received print characters to the proper tilt and rotate I/O code, (2) to activate the proper magnet drivers, and (3) to cause the characters to be printed. The print-decode circuit consists of various AND/OR circuits that input to the magnet drivers. These AND/OR circuits are conditioned by the output of the 2B-register to activate the magnets needed to print the characters.

Two gating lines are used to gate the 2B-register character to the print-decode circuit: 'print out' and 'print.' The 'print' line indicates that the character to be decoded is a print character. This line comes up when an 8-4 combination is not present in the character. The combination of an 8 and 4 in the character designates a function character, causing the function-decode circuit to be gated. The 'print out' line comes up when '2B register full' (indicating that the 2B-register is completely loaded with a character) and 'not I/O cycle' come up. 'Not I/O cycle' indicates that the I/O device is not presently printing a character or performing a function and is therefore ready to receive the incoming character. If the I/O device is operating, the 'not I/O cycle' line is down, blocking 'print out' line. When the character has completed printing, the 'not I/O cycle' line becomes active, allowing the character in the 2B-register to be decoded and to start another print cycle. For example, character "A" consists of the BCD code B, A, and 1. The I/O code requires that rotate magnets 2A, 2, 1, and -5 be picked. Diagram 4-8 shows that the indicated magnets are picked by the BCD code of character "A". When the magnets are picked, the I/O prints the character.

Function Decode

- Translates function characters to I/O code and starts the function cycle.

- Identifies function characters by an 8-4 combination in their bit structure.

The function-decode circuit operates similarly to the print-decode circuit, yet the presence of an 8-4 combination activates the function-decode circuit. If the character contains an 8 and 4, the 'non-print function' line comes up. The character code is again decoded into the necessary I/O code to activate the proper function magnet. The same 'print out' line used by the print-decode circuit gates the function-decode circuit.

Each of the six I/O functions requires a different combination of bits in BCD code to be activated. For example, for a backspace, the BCD code is B, 8, 4, and 2. Diagram 4-8 shows that these conditions activate the backspace-magnet driver. This in turn causes the I/O device to perform a backspace operation. When the backspace operation starts, the 'print out' line drops. Dropping the 'print out' line prevents the printing of a print character or the performing of another function operation until the present operation has been completed.

STROBE AND I/O CYCLE (ALL MODELS)

- I/O printer timing for terminal logic.

- Signals originate through I/O printer contacts.

- Two signals from printer: IOC (I/O cycle) and strobe.

- Terminal logic generates four signals:

1. 'I/O Cycle' (latch)--same timing as IOC contacts.
2. 'Strobe O' (trigger)--same as electrical signal, 'strobe,' clipped by CC1 and conditioned by 'enter.'
3. 'Strobe' (trigger)--same as 'strobe O,' offset 25 usec later (CC2).
4. 'I/O check strobe' latch--same as electrical signal, 'strobe,' enabled by 'I/O check enable.'

Two I/O timing signals, IOC (I/O cycle) and strobe, originate by transfer of contacts. Basically, IOC means that a cycle has started, and strobe means that transmitting contacts can be sampled.

Two chains of transfer contacts complete the circuit for the I/O timing signals (Diagram 4-9). One contact in each chain transfers for any one operation. The C5/6 contact is common to both chains.

Depending upon the function, printer ('C') contact(s) transfer with each mechanical cycle. The IOC and strobe N/O signal are generated as soon as the N/O contact(s) transfer.

Note that the timing charts (Diagram 4-9) indicate that the IOC N/O contacts mechanically make with or before the strobe N/O contacts and open with or after the strobe N/O opens. This is done to insure that the transmit contacts have had time to settle before they are sampled.

The strobe, strobe O and IOC contacts provide the proper timing conditions for the transfer of data from the I/O printer contacts to the 2B-register.

'I/O cycle' and 'I/O check strobe' allow checking of the I/O printer during 'buffer print and communicate,' or 'receive text and not receive text buffer.' Either of these modes brings up 'I/O check enable.'

I/O cycle provides the proper timing conditions to transfer the character to be printed from the 2B-register into the I/O check enable and I/O check registers.

'I/O check strobe' provides the proper timing conditions to allow data from the I/O printer contacts to control the set and/or reset of the I/O check register as printing is done.

COMMUNICATE/LOCAL AND STATUS

- 2740 status allows mode changes necessary for communicate operations.

- Local operation drops status.

- Paper present can be mechanically by-passed on the 2740-1.

Communicate/Local

- Communicate operation for transmit, receive (or 2740-2 enter).

- Local operation for use of I/O printer as a typewriter.

- Local operation for 2740-2 enter or buffer print.

The following communicate conditions drop status: out of paper, line adapter not operative, or waiting to transmit. On the 2740-2 enter, buffer print, or document insertion guide in insert position will also drop status.

The Communicate/Local switch controls the 'comm-local' trigger. Changing the switch position to Local is ineffective unless the 2740 is not printing

from buffer storage and is in the text non-selected mode or control receive mode (Diagram 4-11).

The comm-local trigger turns on (local) at CC2 when these conditions are met. However, the trigger will turn off (communicate) at the next CC2 after changing the switch to Comm.

Local drops status and causes the I/O printer motor to run.

Status

● Status can change at any CC2 except during transmit answerback.

● Status conditions are those necessary for receiving.

The status conditions gate the 'status' trigger on or off at every CC2 (Diagram 4-11). A change in status is prevented only during transmit answerback (when prevailing status is sent-- Ⓨ for status, Ⓝ for not-status). The operator is responsible for the condition of the terminal since the time that a message will be received is unknown. Status circuits drop status if any lack of capability for receiving is detected.

If the terminal does not have status during a normal address sequence, the 2740 will respond with Ⓝ and ring the alarm bell. The 2740-2 will turn on the message light also.

OPERATE TRIGGER (ALL MODELS)

● Prevents the terminal from leaving transmit or receive mode until the operation is complete.

The function of the 'operate' trigger is to indicate to the terminal that a character is (1) being printed, (2) being acted upon by the terminal (receive mode), or (3) in the process of being shifted through the S-register to the 'serial data out' line (transmit mode). The 'operate' trigger prevents the terminal from leaving transmit or receive mode until the operation is complete. The status of the mode triggers cannot change until the 'operate' trigger turns off.

The 'operate' trigger (Diagram 4-10) is turned on by any of the following conditions: 'I/O cycle' 'communicate, ' and 'not send, ' 'not strobe O reset gate' and 'not send, ' '2B set set gate, ' '2B set, ' 'not 2B empty, ' or 'not S register empty. '

With the terminal in receive mode, when a character (1) is about to be loaded into the 2B-register (2B set set gate'), (2) is presently being loaded into the 2B-register ('2B set'), or (3) is in the 2B-register ('not 2B empty'), the 'operate' trigger turns on. If a character is being printed or a function being

performed, the 'operate' trigger is turned on by either 'I/O cycle' or 'not strobe O reset gate. ' As soon as these conditions are removed, the 'operate' trigger turns off.

When the terminal is in transmit mode, and a character is in or being shifted through the S-register, the 'operate' trigger is turned on by 'not S register empty. ' As soon as the character has completely shifted out of the S-register, 'not S register empty' drops and the 'operate' trigger is turned off by 'not SD1, ' 'SD2, ' 'SD3' and 'send. '

BUFFER STORAGE (2740-2)

● Magnetic Core storage device has a maximum of 3,136 cores (448 characters).

● Processes a bit (one core) at a time using a one position 'memory buffer' trigger.

● Bit counter, address register, and 'read-write' trigger are used for timing and addressing system.

● Store (write) characters during enter or buffer receive character cycles.

● Readout (read and regenerate) characters during send or buffer print character cycles.

The 2740-2 buffer storage is a magnetic core storage device with optional 128-, 256-, or 448-character capacity. Buffer storage is an intermediate point in the flow of data characters from the I/O keyboard to the communication line (Figure 2-1). ENTER stores input characters sequentially in buffer storage, and SEND retrieves characters sequentially from buffer storage to transmit them. BUFFER PRINT retrieves characters to print them.

The description of buffer storage begins with a brief explanation of coincident-current, magnetic-core-storage theory; then functional units of buffer storage are explained. The functional units are:

1. Bit counter (character cycle)
2. Buffer address register (chooses character location in buffer storage)
3. Buffer storage circuits (control data input and output from buffer storage)

Magnetic Core Theory

● A magnetic core is a small ferrite (powdered iron) ring.

- A core can be magnetized in either of two directions; one represents binary zero (no bit), the other binary one (bit).

- Each core represents one bit of data.

- A core is magnetized by passing electric current through its center.

- Two wires, each carrying 1/2 magnetizing current, pass through each core (coincident current system).

- One wire is horizontal, the other vertical.

- A third wire for sensing core flip goes through all cores.

- A read pulse and a write pulse are generated for each bit time.

- At read time, the selected core is reset to zero.

- At write time, the selected core can be flipped to binary one.

A magnetic core is a small ring of ferromagnetic material, a few hundredths of an inch in diameter. It is a mixture of ferric oxide powder and other materials, pressed and baked to form a ferrite ring.

Important advantages of the core are its size, speed, power requirements, and its ability to retain a magnetized state after current flow through the wire(s) stops. Hundreds of characters may be stored in cores mounted on one plane on a small pluggable card. The magnetic state of a core can be changed by a short pulse of current passing through the ring. The duration of the magnetizing current pulse is only a few millionths of a second, but the core retains its magnetism indefinitely.
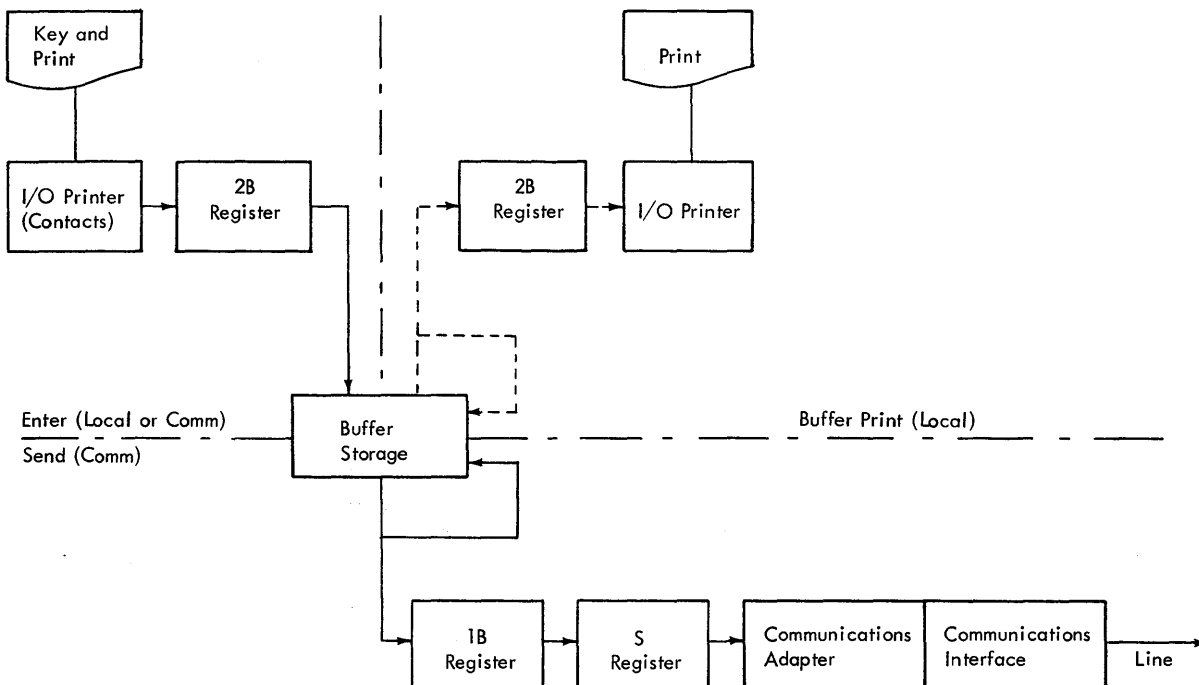
Figure 2-1. Overall Flow of Outgoing Message

A number of ferrite cores placed like beads on a single wire are magnetized when a sufficient amount of current is passed through the wire (Figure 2-2A). The direction of the current flow determines the polarity or magnetic state of the core. It retains the magnetic state after the current stops and reverses its magnetic state when the current is applied in the opposite direction (Figure 2-2B). Consequently, these two states can be used to represent 0 or 1, plus or minus, yes or no, on or off, bit or no bit conditions.

Current is Applied   Core is Magnetized   Current is reversed; the core reverses its magnetic state
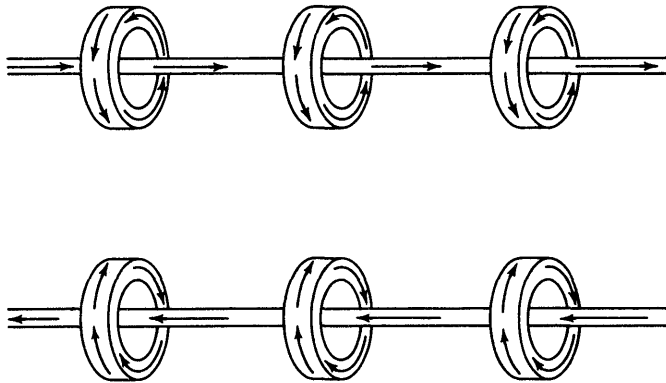
A. Polarity of Magnetic Cores

B. Reversing a Core (Flip)

Selected Core

1/2 Current

1/2 Current
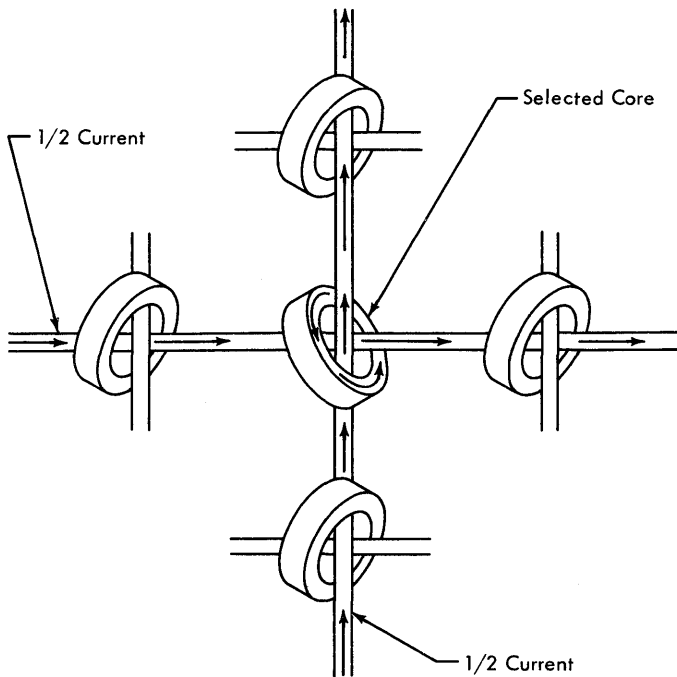
C. Selecting a Core (Addressing)
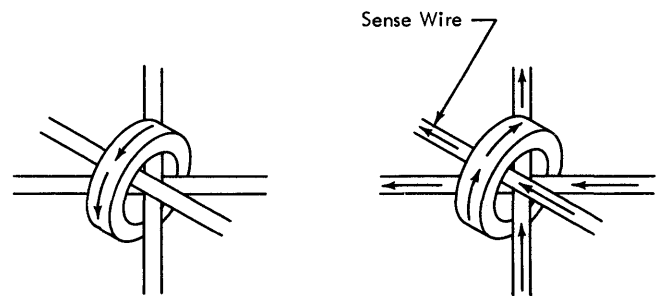
Sense Wire

D. Core Flip and Sense

Figure 2-2. Core Theory

A system of addressing must be devised to access each core. To accomplish this, the one wire passing through each core is replaced by two wires (Figure 2-2C). If half the required current passes through each of two wires the effect is the same as one wire carrying the required current. A large number of cores can be strung on a screen of wires and any one core in the screen can be selected. This is done by applying one-half current to only two wires. The core affected is the one at the intersection of these two current carrying wires. No other core, even on the "half current" carrying wires, is affected. Using this principle, the number of cores in an array can vary from a few hundred to more than a million.

When the current in a pair of wires through a core is coincident, the core assumes a definite magnetic polarity. If the coincident current is reversed, the magnetic state is suddenly reversed and the core is said to flip (flux reversed). One magnetic state has been predetermined to represent a bit (one) and the other a no bit (zero). Storing a bit of information is referred to as writing; retrieving, as reading. Each time the core is addressed the cycle consists of read time first and then write time. During read time the circuits attempt to flip the selected core from a "one" state to a "zero" state. If the core was in the "one" state prior to read time, the data is detected (read) by resetting the one to zero. Therefore, the core is reset, and readout is destructive. At write time the same core may be flipped from a "zero" to a "one" state.

A third wire is threaded through the core for the purpose of sensing a pulse at read time (Figure 2-2D). When the magnetic state of the core is reversed, the abrupt core flip (flux reversal) is of sufficient magnitude to induce a voltage and generate a pulse. Only one sense wire is needed for an entire core plane, because only one core is selected and read at a time. Even though a pulse is induced in the sense wire each time a core flips at read time and write time, the output circuits monitor the sense wire at read time only.

To retain the information in buffer after it is read-out, it must be rewritten. Each bit sensed in storage may be restored immediately after it is read by allowing it to be rewritten into buffer at the following write time. This process, referred to as regeneration, is automatic in the buffered terminal. The bits are not regenerated at any time that new data is to be placed in buffer.

Odd-Even Core Scheme

● Cores are strung on wires that cross at right angles.

● Each wire carries current individually.

● Each wire can carry current in either direction.

● Vertical current direction selects odd or even core.

The two current carrying wires used in buffer storage are the vertical wire and horizontal wire. A core is selected for read or write by coincident current flow in these vertical and horizontal wires passing through the addressed core. Figure 2-3A illustrates how the magnetic cores in a terminal buffer are strung on wires that cross at each core. This method of arraying the cores provides the selection system. The third (sense) wire is not shown in the figure.

Assume that the heavy lines in the figure represent the active current lines, each carrying one-half current required to flip a core. All the cores strung on the active vertical and horizontal wires are subjected to the effect of this one-half current. One-half current is not sufficient to affect the magnetic state of a core, but two of the cores are subjected to both the horizontal and the vertical current carrying wires. At this point the current direction is important and determines which of the two cores will flip.

A schematic representation of current flow (Figure 2-3B) is used to show the current flow relationships. Assume that right-to-left horizontal current is read current, and left-to-right horizontal current is write current. Since the vertical wire through the odd and even core columns is the same wire, the terminology "read even or write odd" and "read odd or write even" is used to define the direction of vertical current flow.

At read time, the vertical read odd current flow down through the odd core coincides with the horizontal read current at the odd core. The same vertical current loops back up through even core and cancels the effect of the horizontal circuits. Thus, the odd core is selected to read, while the even core is not affected.

At write time, both the horizontal and vertical currents reverse. Again the odd core is selected to be flipped while the even core is not affected.

During read and write time the horizontal current flow is controlled without regard to odd or even core selection. Selecting the even core to read and write is a matter of starting the vertical current read-write sequence with read-even and completing it with write-even. The horizontal and vertical current coincide at the even core and cancel at the odd core to read and then write (regenerate) the even core only.
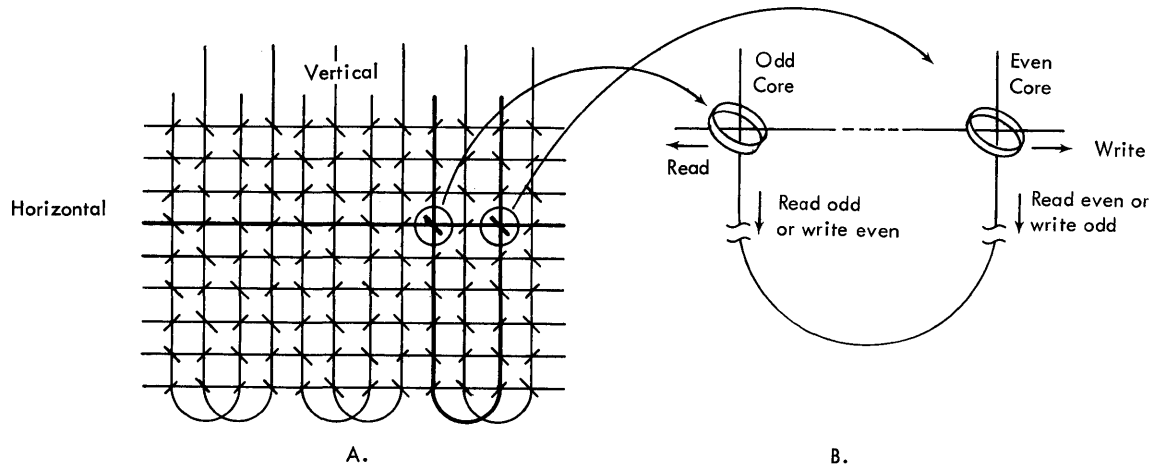
Figure 2-3. Addressing by Current Coincidence and Cancellation

Selection of either of the two cores where the wires cross has been made possible by controlling the phase relationship of vertical current to the horizontal current. This odd-even core scheme reduces the number of current carrying circuits required to address core in the buffer storage array. One of the Buffer Address positions ('BA5') is used to control the vertical current direction. When 'BA5' is off the vertical current wire selects read odd and write odd; when 'BA5' is on, read even and write even.

Character Cycle

● Basic buffer storage cycle.

● Processes one character.

● Eight bit times (0 through 7).

● Starts from 2B full when storing, 2B empty on printout, or 1B empty when sending.

● Runs for a minimum 1.56 ms with 18 KHz oscillator; 2.92 MS with 9.6 KHz oscillator (600 Baud).

Seven cores represent a 2740-2 character in buffer. One character cycle spans all timings needed to store or retrieve one character.

Each character cycle has eight bit times (Figure 2-4). Bit times 0-6 correspond to character bits 1 through 7. The eighth bit time is used for end-of-character or idle timings.

Each bit time has a read time and a write time (Figure 2-4). Read-time horizontal and vertical currents allow flipping the selected core from binary one to binary zero. Write time horizontal and vertical currents allow flipping the selected core from binary zero to binary one.

The entire character cycle is 1.56 milliseconds long and begins with a demand to store a character (enter or buffered receive) or to retrieve a character buffer print or send).

NOTE: With the Speed Base-600 bps feature, a 9.6 KHz oscillator is used to time buffer storage. A character cycle is then 2.92 milliseconds long.

Buffer Storage Address Counter

● Counts in binary

● Consists of two parts: buffer address register and bit counter.

The buffer storage address counter controls the selection of a specific magnetic core. This involves selecting a vertical array line, a vertical current read-write sequence (odd or even), and a horizontal
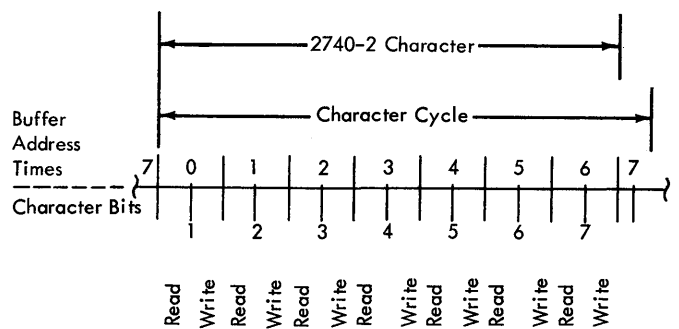
Figure 2-4. Buffer Storage Character Cycle

array line (Figures 2-3 and 2-6). This counter also provides sequential selection of every core in the array.

Buffer Address (BA) 1, 2, and 3 make up the bit counter. Positions 4-12 of the buffer storage address counter make up the buffer address register. This register can count from zero to 511, but automatically skips certain counts when it advanced beyond 256 (See Diagram 4-15). The decimal values of the buffer address register positions, as shown in Figure 2-5, add up to the character address in the buffer. In the example, the binary ones have decimal values (right-to-left) of 4+8+32+64+128=236. The 236th character is addressed during that cycle.

Bit Counter (Diagram 4-14)

● Initially reset on (BA1, 2, and 3).

● Steps at end of each write time.

● Counts from 0 through 6 each character cycle (bits 1 through 7).

● Character cycle ends when count is 7 (BA1, 2, and 3 on).

At the beginning of each character cycle the bit counter steps from 7 to 0 (first bit position). At the end of each subsequent read-write cycle, the bit counter advances sequentially through address bit positions two through seven (bit times 1 through 6). Bit time seven ends the character cycle. The output of the bit counter controls selection of one of seven horizontal switches (Figure 2-6).

Buffer Address Register (Diagram 4-15)

● Initially reset off (zero).

● Steps binarily at the start of each character cycle.

● May contain seven, eight, or nine triggers.

● When maximum nine triggers (BA 4-12) are present, 64 counts are skipped.

● Can step backward (reverse).

● Count of zero identifies 'buffer address empty.'

● All triggers on identifies 'buffer overflow.'

Character addresses originate from BA 4 through 10 (128-character), BA 11 (256-character), or BA

12 (448-character) of the buffer storage address counter. Counting is in the normal binary manner when BA 12 is not present.

Buffer address register triggers 4 through 10, 11, or 12 comprise a binary counter. Each trigger has gates for turn-off that enable the counter to count either forward (normal) or backward (reverse). Diagram 4-15 illustrates each set of gating conditions that causes a buffer address register trigger to turn on or off. Read down the chart for normal counting, and up the chart for reverse counting.

'Buffer address 11' is used only with the 256- and 448-character core arrays, and is not present with the 128-character core array. Also, 'buffer address 12' is used only with the 448-character array.

Buffer address positions 4 and 6 select one of 4 vertical drivers. BA7, 8, and 11 select one of 8 vertical switches. BA9, 10, and 12 select one of 7 horizontal drivers (Figures 2-5 and 2-6).

Buffer address position 5 is used to define vertical current direction (phase) and select the odd or even core in the odd-even core selection scheme. With BA5 off, the odd core is selected; and with BA5 on, the even core is selected.

Address Register Control (Diagram 4-15)

● 'Buffer counter ac input' steps address register.

● Address steps normal (forward) or reverse (backward).

● Address register resets to zero automatically:

1. When Enter key is pressed.
2. At start of buffer print.
3. At end of transmit text.
4. At start of transmit text.
5. When Reset key is pressed.

● Buffered Receive feature adds three more resets:

1. At the end of on-line buffer print.
2. At the start of receive text.
3. At the start of retransmission from central.

Address Register Advance

The character address steps normal or reverse, one address at a time. The step results from gating shown in Diagram 4-15 and takes place when the 'buffer counter ac input' line comes up (Diagram 4-16). This line may rise from two sources:

1. The 'buffer address 3' trigger turns off and is a forward (normal) advance from the memory clock. Because a character cycle ends with 'buffer address 1, 2, and 3' on, and 'read-write' off (write), the next character cycle begins when 'read-write' turns on (read) and 'buffer address 1, 2, and 3' turn off. Therefore, the buffer address register steps normal at the very biginning of a character cycle.

2. The 'reverse counter sequence control' trigger turns on at 'CC1'. This is a reverse step, usually caused by a backspace operation when entering from the I/O printer keyboard. A reverse-count requires 'reverse counting sequence' and 'not buffer address empty'. The 'reverse counting sequence' trigger is on for 50 usec starting at the end of 'strobe' time. There is no character cycle at the time because 'reverse counting sequence' inhibits the turn on of the 'read/write' trigger (Diagram 4-18).

'Buffer address time 7' allows the 'buffer 2B reset' trigger to operate. The backspace code is reset from 2B at 'CC2', and 'memory go' drops without starting a character cycle.

A second reverse count condition occurs when changing from buffer print to enter, at the end of an off-line (local) printout. The operator may choose to continue entering, so the stored stop code must be replaced by the next character entered. The 'edit control 3' trigger turns on when the stored stop code appears in 2B. The same stop code resets the 'buffer print' trigger, and the 'reverse counting sequence' trigger turns on. The 'enter' trigger turns on, too, but the same series of events described in the preceding paragraph prevents a character cycle. The stop code resets out of 2B, leaving the character address ready to step to the stop code address when the next character is entered.
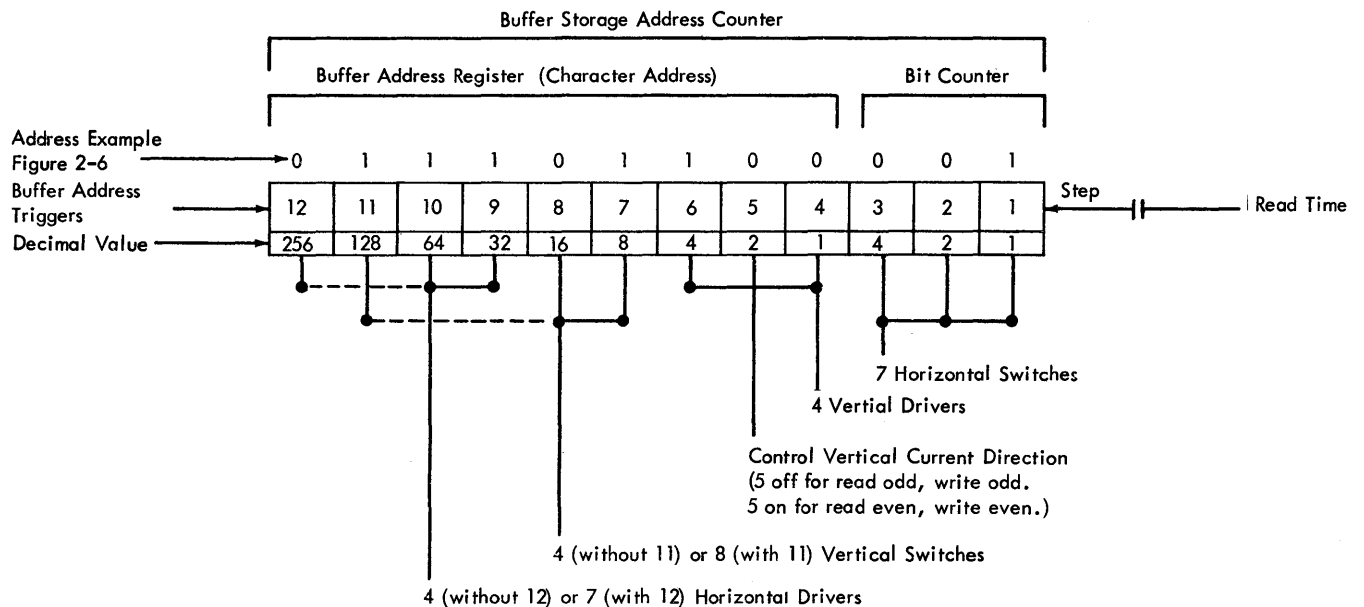
Note: 128-character array uses address trigger 1-10.
Trigger 11 is added for 256 characters and trigger 12 for 448 characters.

Figure 2-5. Buffer Storage Address Counter
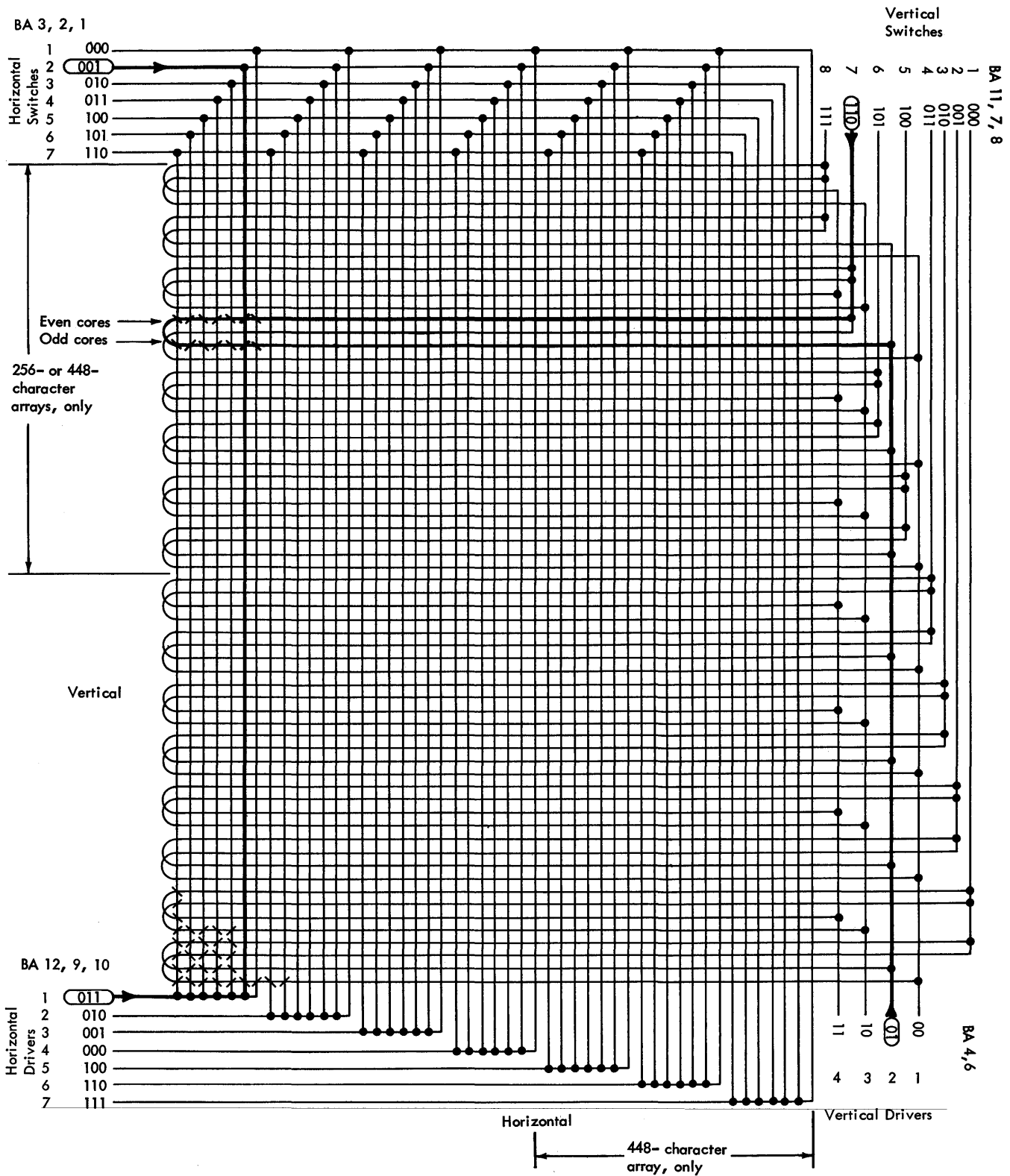
Note: This drawing illustrates the whole array, but is a schematic and does not show actual wiring.
The circled address examples also appear in Figure 2-5.

Figure 2-6. Array Wiring and Addressing

Address Register Reset

The 'reset buffer address' trigger (Diagram 4-16) turns on to reset the buffer address register and the bit counter. The address register resets to zero and the bit counter to seven. The turn-on gate for 'reset buffer address' offers several ways to reset the address, with additional provisions when the 2740-2 has the Buffered Receive feature. All ways are listed here (unique Buffered Receive resets identified by asterisks):

1. The Enter key is pressed and the 'enter' trigger turns on. This resets the buffer address at the very beginning of an enter operation.
2. When the Reset key is pressed with the 'enter' trigger on. (The only other action of the Reset key is to reset the 'enter' trigger.)
3. The 'buffer print' trigger turns on. This action occurs off-line (local) when the Bid key is pressed with the 'enter' trigger on. The resulting stop cod e (Diagram 4-18) turns on the 'buffer print' trigger and the 'reset bufffer address' trigger (Diagram 4-16).

   *On a Buffered Receive machine, 'buffer print' turns on after Ⓒ is received. This is the signal for the 2740-2 to read out the message stored and print it on the I/O. The buffer address register and bit counter reset just as they do at the start of off-line buffer print.
4. Transmit text starts. The mode change to transmit text resets the address so that the first character sent is the first character in buffer storage.
5. Transmit text ends with an affirmative acknowledgment. This reset prevents manual retransmission of the stored message. If an affirmative answerback (Ⓨ) is not received, the address does not reset.

   When the message acknowledgment is Ⓓ , directing the 2740-2 to receive a message, buffer address resets.
*6. On-line (communicate) buffer print ends. This reset prevents unintentional transmission of the received and printed m essage by accidental depression of the Send key.
*7. Receive text buffer starts. The mode change to receive text resets the address so that the first character received stores at the first character address in buffer storage.
*8. Receive text buffer begins without the previous message having been printed out (no Ⓒ). This case comes up when the 2740-2 sends a negative acknowledgment to a received message and central retransmits the message. The retransmission must be stored starting at the first character address in buffer storage.

Buffer Storage Array and Addressing (Figure 2-6)

- 16 or 32 vertical lines, 4 drivers and 4 or 8 switches.

- 28 or 49 horizontal lines, 4 or 7 drivers and 7 switches.

- Card-mounted array, diodes on array card.

- Diodes at switch end of lines, only.

- Current source is positive, current sink is negative.

- Each driver or switch has a source and a sink.

- Vertical and horizontal lines coincide at two cores, even and odd.

- 'Buffer address 5' trigger controls odd or even core selection (vertical current direction).

A set of vertical and a set of horizontal lines form the matrix that is the buffer storage core array. The address in the buffer address register, plus the decoded bit count, selects one driver and one switch for each set of lines.

Line selection is complete when a positive source and a negative sink are selected; only then can current flow. To provide for this polarity selection, each driver and each switch contains a positive source and a negative sink. The positive source is conditioned by one gate and the negative sink is conditioned by the other gate.

Positive or negative polarity gating affects all drivers or all switches, either horizontal or vertical. The horizontal and vertical gates have two purposes: (1) to provide timing, (2) to select the correct driver and switch polarities. Thus, the gates control the timing and direction of array currents. In addition, the 'horizontal driver write gate' controls whether a bin (binary one) will be written into the selected core.

Memory Clock (Diagram 4-18)

- Is timed by 'CC1' and 'CC2' pulses.

- Provides 7 read-write sequences each character cycle.

- Times array currents and advances bit counter.

- Consists of three triggers: 'read-write,' 'VICG' (vertical current control gate), and 'HICG' (horizontal current control gate).

The memory clock controls array currents and advances the bit counter, which in turn advances the address register. The clock starts when the 'memory go' signal is up and 'read set gate' is not inhibited. It runs in a read-write loop until 'buffer address 7 time' ends the character cycle. Controlling conditions for 'memory go' assure a full character cycle and no more.

The vertical and horizontal array currents flow only when the two controlling clock triggers are on. The 'VICG' (vertical current control gate) trigger times vertical current, and the 'HICG' (horizontal current control gate) trigger times horizontal current. The terminal clock 'CC1' and 'CC2' pulses operate these two triggers and the 'read-write' trigger which controls current time in the read-write sequence (Diagram 4-18).

The 'memory go' line rises when a character cycle is needed. When inhibiting conditions are not present, the 'read set gate' line rises. The 'read-write' trigger turns on to 'read' at 'CC1' for the first read-write sequence, the bit counter steps from 7 to 0 and the buffer address register (character address) advances to the new character address. 'VICG' turns on to gate vertical read current at 'CC2' and "HICG' turns on at the following 'CC1' to gate horizontal read current. 'VICG' and 'HICG' turn off at 'CC2' and 'read-write' turns off to Write at the next 'CC1.' 'VICG' turns on again at 'CC2' to gate vertical write current, and 'HICG' turns on at 'CC1' to gate horizontal write current. 'VICG' and 'HICG' turn off at 'CC2.' The 'read set gate' line rises again and the next 'CC1' starts another read-write sequence. The read-write sequence is 222 usec--111 usec for read and 111 usec for write.

NOTE: With the Speed Base--600 bps feature, the read-write sequence is 417 usec.

Buffer Data Control

- Single-position data register, called 'memory buffer.'

- One sense amplifier.

- Storage operation degates the sense amplifier.

- Bit is stored by gating horizontal current.

- Addressed bit regenerates during readout.

- 'Memory buffer' provides input to 1B-register during transmit, 2B-register during buffer print.

- Data bit comes from 2B-register on enter.

- Character is checked for odd parity during buffer print or enter.

'Memory Buffer' Trigger (Diagram 4-18). This is a one-position storage data register which allows bit-by-bit storage input or output. The bit timer disassembles characters from 2B-register into bits for 'memory buffer' when storing and assembles bits from 'memory buffer' into characters when reading out to the 1B-or 2B-register.

The main condition for storing new data is Enter (or 'receive text buffer with Buffered Receive). During write time any bit sensed is ignored or lost by blocking the output of the sense amplifier.

'Receive text buffer' or 'enter' and 'buffer address time' (0-6) condition the 'memory buffer' trigger to accept a data bit from 2B at 'CC2.' The memory buffer output controls the 'horizontal driver write gate' line, so the core is either left in the reset (zero) state when 'memory buffer' is off, or set to a binary one when 'memory buffer' is on.

Without the enter condition, sense amplifier output is gated to 'memory buffer' and the bit is available as 1B or 2B input. The same 'buffer address time' (0-6) (DD021, DD023) that addressed the core, gates its binary value to the appropriate 1B- or 2B-register position. The bit also controls the 'horizontal driver write gate' line as it did during enter. Thus, the bit value is regenerated in the addressed core.

Sense Line Output. The sense signal, a relatively weak signal,is induced by a core flipping to either polarity. Signals from other than a resetting core may also appear on the sense line--for example, the signal induced by the beginning or end of vertical current (vertical lines run parallel to the sense line), or the signal induced by a core setting to binary one during write time. An accurate readout requires detection, amplification, and discrimination.

The first sense amplifier stage is basically a detector. The detected signal undergoes voltage and current amplification by the second stage to increase it to the strength required by ordinary SLT logic circuits.

Discrimination between the core-read output signal and the extraneous sense line signals is a

matter of timing. The read condition eliminates sensing of a core-write sense line signal. The 'current control 2' line (Diagram 4-18) comes up with horizontal current gating and is delayed to make the active level coincide in time with the switching of a core. Thus, the output of the sense amplifier can be accepted only if a core resets from one to zero at the normal time during enter read. This output enters Memory Buffer where it represents the binary value that was stored in the addressed core.

Summary of Buffer Storage Operation

● Buffer storage is an intermediate point in overall 2740-2 transmit data flow (Figure 2-1).

● Buffer data control provides input.

● Enter-data flow ends at buffer storage.

● Send-data flow and buffer print data flow begin at buffer storage.

● The buffer storage addressing and timing circuits operate the same on enter, receive text buffer, send, and buffer print.

Store

Assume that a new character is to be stored in buffer storage. At this moment, the cores where the character is to be stored may already contain binary ones, the buffer address register has not yet advanced, and the bit counter is at 7. The presence of the new input character in 2B starts the memory clock. The bit counter steps to 0 and the character address advances. Seven read-write sequences ensue, and the bit counter advances from 0 to 7.

Follow the logic and timing of the enter operation for one character (Diagram 4-18). The appearance of a character in 2B-register raises the 'memory go' signal. The 'read set gate' line comes up and drops with each bit time, allowing the 'read-write,' 'VICG,' and 'HICG' triggers to flip on and off.

Assume that 'buffer address 5' is off. This is a read odd/write odd condition. The 'read odd-write even' line is active in read time and the 'read even-write odd' line is active in write time. (When 5 is on, these two lines switch times for the read even/write even condition.) With the turn-on of 'VICG' (vertical current control gate) for read, vertical current flows from the selected vertical driver (negative) to the selected vertical switch (positive). 'HICG' (horizontal current control gate) turns on 25 usec later, and horizontal current flows from the selected horizontal switch (negative) to the selected horizontal driver

(positive). The selected core resets to zero and its contents are destroyed by not being admitted to 'memory buffer'. Instead, a bit value from 2B is gated to 'memory buffer.' Horizontal and vertical read currents end at 'CC2' when the controlling triggers turn off.

Write time reverses current flow in the selected vertical line. The selected vertical driver becomes positive and the vertical switch becomes negative. Vertical current flows when 'VICG' (vertical current control gate) turns on for write. Again, 'HICG' turns on 25 usec later, if 'memory buffer' contains a bit. Then, the selected horizontal switch is positive, the selected horizontal driver becomes negative, and horizontal current flows. The coincident current sets the selected core to binary one. If horizontal current does not flow (no bit in the 2B position or in 'memory buffer'), there is no effect on the core and it remains at zero. Both currents cease at 'CC2' when the controlling triggers turn off.

The following 'CC1' flips 'read-write' to 'read' again and the bit counter advances. The read-write sequence repeats, this time using a different horizontal switch, a different horizontal line, a different core, and a different bit from 2B.

The 'VICG' and 'HICG' triggers do not operate during buffer address time 7. The bit counter stops at seven, 'read-write' turns off to 'write', 'memory go' drops, and the character cycle ends. The input character is stored.

Readout

A send or buffer print character cycle is similar to the end character cycle. In this case, however, the cycle starts with the demand to retrieve a character for transmission or for printing. With a not-enter condition, the sense amplifier output can gate a binary one from the 'sense' line and set the one into 'memory buffer.' Input from 2B is inhibited. 'Memory buffer' again controls horizontal current, and any bit read out is regenerated in the core during write.

During a readout operation, buffer storage reads out the seven-bit character and this character is assembled bit-by-bit in the 1B-register for transmit or in the 2B-register for a print operation. The advancing bit counter selects each core sequentially, and gates the matching register position (Figure 2-7). Again, the eighth count ends the character cycle.

Temperature Compensation (Figure 2-7)

● Temperature compensation regulates array currents.

Magnetic cores require higher current for switching when they are cold, so low array temperature is offset by increased array currents. As the switching activity and high currents warm the array, the current is reduced. The cores switch more easily as they warm, thus temperature compensation maintains uniform core switching time. This contributes to the accuracy and efficiency of buffer storage operation.

The core array enclosure contains a temperature-sensitive resistor called a thermistor that allows higher array currents when the array is cold; lower currents when the array is warm. Thermistor output controls the 'TEMP. COMP. V' circuit DD011 directly, and the I CONTROL circuits indirectly.

Figure 2-7. Buffer Data and Addressing
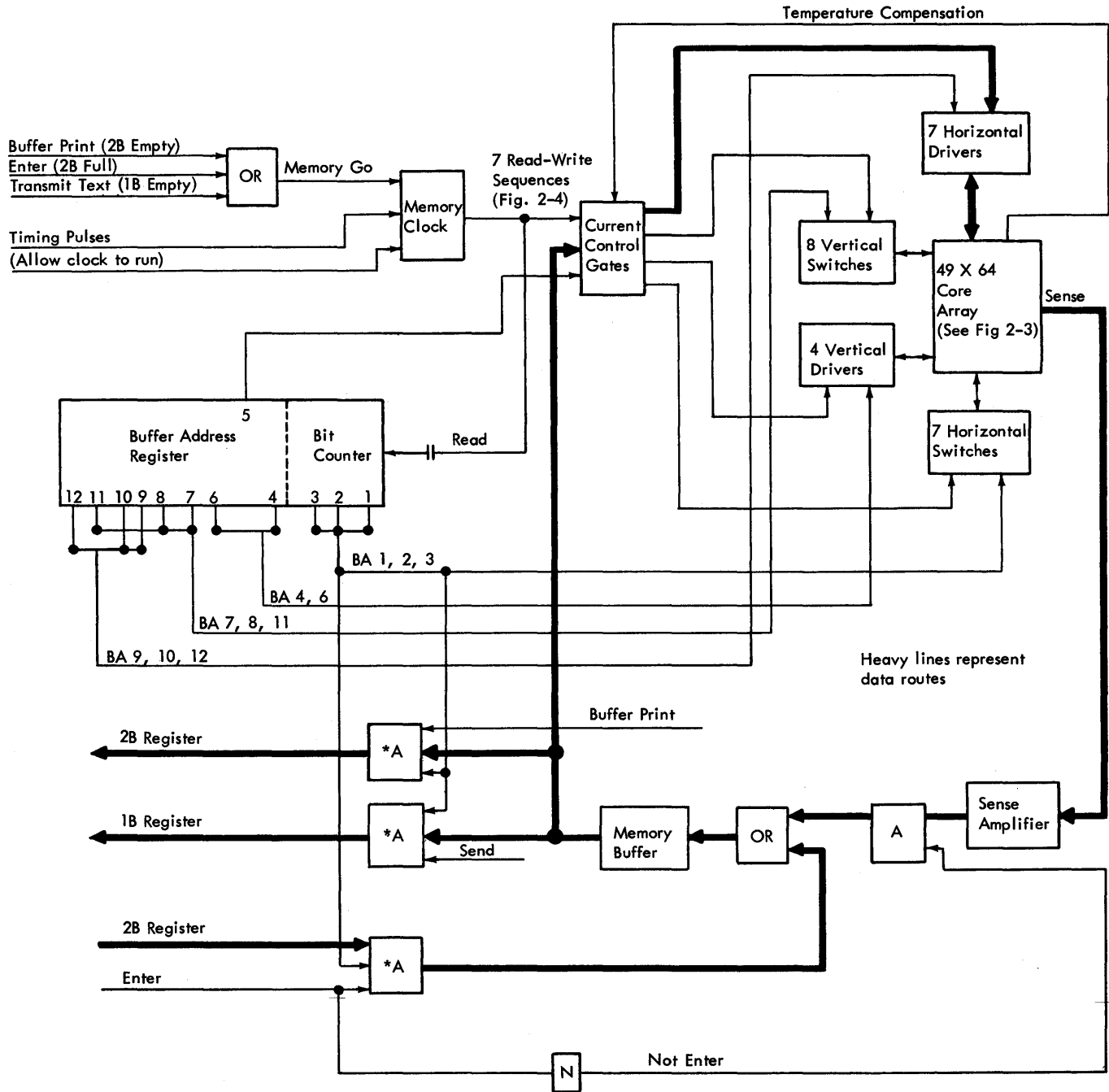
*Note: Multiple ANDs; One for each 2740-2 character bit.

2740 COMMUNICATION TERMINAL, MODEL 1

BASIC-TERMINAL MODE CONTROL

- All terminal operations are determined by the terminal mode.

- The basic-2740 mode is determined by the condition of mode triggers 'A' and 'B.'

- In the basic 2740 there are three modes: (1) 'A' and 'B' on (control receive mode), (2) 'A' on and 'B' off (transmit text mode), and (3) 'A' off and 'B' on (receive text mode).

The mode in the basic 2740 is determined by the condition of two triggers: the 'A' trigger and the 'B' trigger. When both the 'A' and 'B' triggers are on, the 2740 is in control receive mode. While in control receive mode, the 2740 can receive any of the control characters, such as the bid character Ⓓ. When only the 'A' trigger is on, the 2740 is in transmit text mode. When only the 'B' trigger is on, the 2740 is in receive text mode. If the 2740 is equipped with some of the special features, many more modes are possible with the addition of other mode triggers. For this explanation, however, just the basic 2740 is discussed.

When machine power first comes up in the 2740, the 'power on reset' line turns both the 'A' and 'B' mode triggers on, putting the 2740 into control receive mode (Diagram 5-1).

To send data, the 2740 is placed into transmit text mode. This is accomplished by turning off the 'B' mode trigger. The operator presses the Bid key to turn on the 'bid' trigger. 'A,' 'B,' and 'bid' bring up the 'B reset gate' line, which turns off the 'B' mode trigger. An AND connected to the mode-trigger outputs determines whether the 2740 is in transmit or in receive mode. If the AND is conditioned by 'A' on and 'B' off, the 'send' line comes up. If any other condition exists, the 'not send' line is active.

'B reset gate' also conditions an OR that turns on the 'mode change' trigger. Every time a change in modes occurs, the 'mode change' trigger turns on to provide a reset to some of the 2740 circuits. The 'mode change' trigger then gates itself off with the next 'CC1' pulse.

When the bid character Ⓓ is received at the receiving terminal, the 'A' trigger turns off, putting the 2740 in receive text mode. The 'A' trigger is turned off by the conditions: 'status,' ' Ⓓ , ' 'B,' and 'A.' These conditions bring up the 'A reset gate' line.

To stop sending, the sending terminal operator presses the EOT key. A Ⓒ is sent and the terminal goes into control receive mode. The mode change is accomplished by turning on the 'B' mode trigger. 'Send,' ' Ⓒ , ' 'not operate,' 'not EOT,' and 'end-of-state' bring up the 'B set gate,' returning the terminal to control receive mode.

When the 2740 is in receive text mode and the end-of-transmission character Ⓒ is received, the 'A' trigger turns on to return the 2740 to control receive mode. An AND feeding an OR brings up the 'A set gate' line, which turns the 'A' trigger on. This line is brought up by the conditions: 'not send,' 'not operate,' and ' Ⓒ .' If a loss of status occurs while the terminal is in receive text mode, 'not A' and 'not status' bring up 'A set gate.' Thus, the 2740 returns to control receive mode.

The status of the 2740 is determined by the condition of the 'status' trigger (see Diagram 5-1). As long as the 'status' trigger is on, the 2740 is capable of receiving or sending data. The 'status' trigger turns on when (1) paper is in the terminal, (2) the terminal is in communicate mode, and (3) the data set has status (power on, able to communicate). Failure to have any of these conditions turns the 'status' trigger off. If, while 'status' is off, a Ⓓ character is received, an AND--conditioned by 'not status,' 'not C1,' 'A,' 'B,' and ' D '--rings the alarm bell. 'Status' is also needed to illuminate the Standby light.

TRANSMIT (POINT-TO-POINT)

The 2740 is capable of sending control and text characters. The control characters are sent when the operator presses the Bid or EOT keys and text characters, when any of the print or function keys on the I/O keyboard are pressed.

A character is loaded into the 1B-register in one of two ways: if the character is a control character, the '1B generate' line provides input to the 1B-register; if the character is a text character, the I/O transmit contacts provide the input. The flow-chart (Diagram 5-2) shows the sending sequence.

Load Control Characters Into 1B-Register

- Control characters are developed by bringing up '1B generate.'

- Ⓓ is developed by gating the '1B3,' '1B5,' and '1B6' triggers.

- Ⓒ is developed by gating the '1B3' through '1B7' triggers.

- Control characters are loaded by bringing up '1B set.'

The control character inputs to the 1B-register are shown in Figure 3-1. To start sending, the operator presses the Bid key. If (1) the 2740 is in control receive mode, (2) the Local/Communicate switch is in the COMM position, and (3) the serdes clock is not running, the 'bid' trigger turns on. The 'bid' trigger on and the 'send' line up bring up '1B generate.' '1B generate' conditions one leg of the ANDs to the '1B3,' '1B4,' '1B5,' '1B6,' and '1B7' triggers of the 1B-register. '1B generate' also gates on the control clock. '1B set' comes up when both the 'C1' and 'C2' outputs of the control clock are active, the 'send' line is up, and the 'enter serdes' trigger is off. '1B set' completes conditioning the ANDs to the '1B3,' '1B5,' and '1B6' triggers. The 'bid' trigger prevents turning on the '1B4' and '1B7' triggers. Thus, the Ⓓ character (821) is loaded into the 1B-register.

To stop sending, the operator presses the EOT key to return the sending and receiving terminals to control receive mode. This is accomplished by generating and sending the EOT character Ⓒ. When the EOT key is pressed, one leg of an AND to turn on the EOT trigger is conditioned (see Figure 3-1). The other conditions are 'send,' '1B empty,' 'not 1B generate,' 'not strobe O,' and 'not operate.' These conditions ensure that:

1. The 2740 is in transmit mode.
2. The 1B-register is empty.
3. The Bid key has not been pressed. (The '1B generate' input acts as an interlock, preventing both bid and EOT characters from attempting to load the 1B-register at the same time.)
4. The I/O device is not presently going through a cycle.
5. The 2740 is not presently transferring a character through logic.

The 'EOT' trigger coming on causes '1B generate' to come up (similar to 2740 sending a bid character). The '1B generate' conditions one leg of five ANDs to

the 1B-register. '1B generate' also starts the control clock to provide the '1B set' pulse. '1B set' completes conditioning the ANDs, loading the Ⓒ character (8421C) into the 1B-register.

Load Text Characters Into 1B-Register

- Text characters originate at the I/O transmit contacts.

- Text characters are loaded into the 1B-register by the 'strobe' line.

When the operator presses a key on the I/O keyboard, transmit contacts in the I/O device transfer into the bit configuration of the desired character. When gated, these contacts condition the ANDs that load the desired character into the 1B-register (Figure 3-2). As the I/O device goes through its cycle, 'C7' (in the I/O device) makes, bringing up the 'strobe N/O 1' line. 'Strobe N/O 1'--ANDed with 'send,' 'not 1B generate,' and '1B empty'--turns on the 'strobe O' trigger. 'Strobe O' gates on the 'strobe' trigger, which loads the text character into the 1B-register. The strobe circuit insures that the I/O device has had enough time to properly transfer the transmit contacts before gating through them to the 1B-register. The control clock is not started at this time; the character is loaded into the 1B-register without need of the control clock outputs.

Transfer Characters from 1B-Register to S-Register

- S-register restored by 'S register empty.'

- 'Enter serdes' transfers the character in the 1B-register to the S-register.

- 1B reset by the control clock.

Once in the 1B-register, all characters (control or text) transfer to the S-register in the same manner. When a character is in the 1B-register, '1B full' comes up. If the 'S register empty' trigger is on and the I/O device is not presently going through a cycle (noted by 'not strobe O'), the 'enter serdes gate' turns on (Diagram 5-3). The 'enter serdes gate' trigger allows the 'S register restore' pulse to occur before a new character is loaded. 'S register restore' is accomplished by delaying the turning on of the 'enter serdes' trigger. When the previous character is shifted out of the S-register, the 'S register empty' trigger turns on. 'S register empty' turns on the 'enter serdes gate' trigger and, ANDed with 'SD1' and 'send', applies the restore pulse to the S-register. 'Enter serdes gate' and the
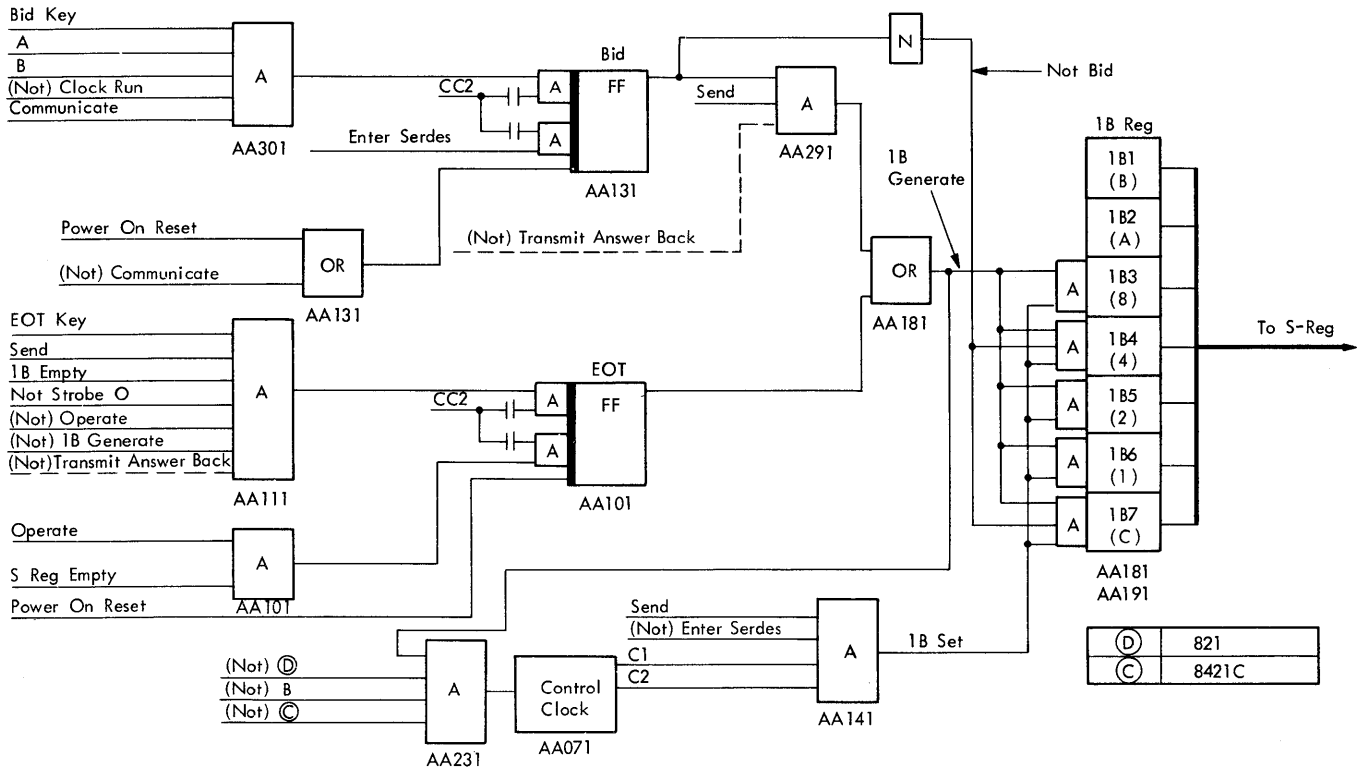
Figure 3-1. Generate Control Characters

next 'SDAC' pulse turn the 'enter serdes' trigger on and the 'S register empty' trigger off.

'Enter serdes' -- along with '1B full,' 'not C2,' and 'send' -- conditions an AND the output of which, 'S0 reset,' is the gating pulse that transfers the character from the 1B-register to the S-register. 'S0 reset' also goes directly to the 'S0' trigger, turning it off, which loads the start bit for the character. 'S register empty' ANDed with 'send' has already loaded the stop bit. When 'S0' turns off, the control clock starts. The control clock outputs, 'C1' and 'C2,' turn off the 'enter serdes' trigger and reset the 1B-register.

The complete character is now in the S-register and must be serialized to the 'serial data out' line.

S-Register to 'Serial Data Out' Line (Diagram 5-3)

During sending operations, the serdes clock is continuously running, providing 'SDAC' pulses to the S-register. When the character is received in the S-register, it immediately begins to shift down

through the S-register, bit-by-bit, to an AND. The AND is conditioned by 'send.' The output of the AND is the 'serial data out' line. When the character has completely shifted down through and out of the S-register, the 'S register empty' trigger turns on, and the S-register is restored.

End-of-Transmission

When an EOT character is generated and sent, it causes the sending and receiving terminals to go into control receive mode. In the sending terminal, the EOT character is detected when it is in the 1B-register. The EOT character brings up the line ' Ⓒ .' The ' Ⓒ ' line turns on the end-of-state' latch and, after the Ⓒ is transmitted, the 'B' mode trigger. The 'end-of-state' latch prevents the 1B-register from resetting, since the terminal mode cannot change until the complete EOT character is sent. When the 'B' mode trigger turns on, a mode change occurs. This resets the 1B-register.
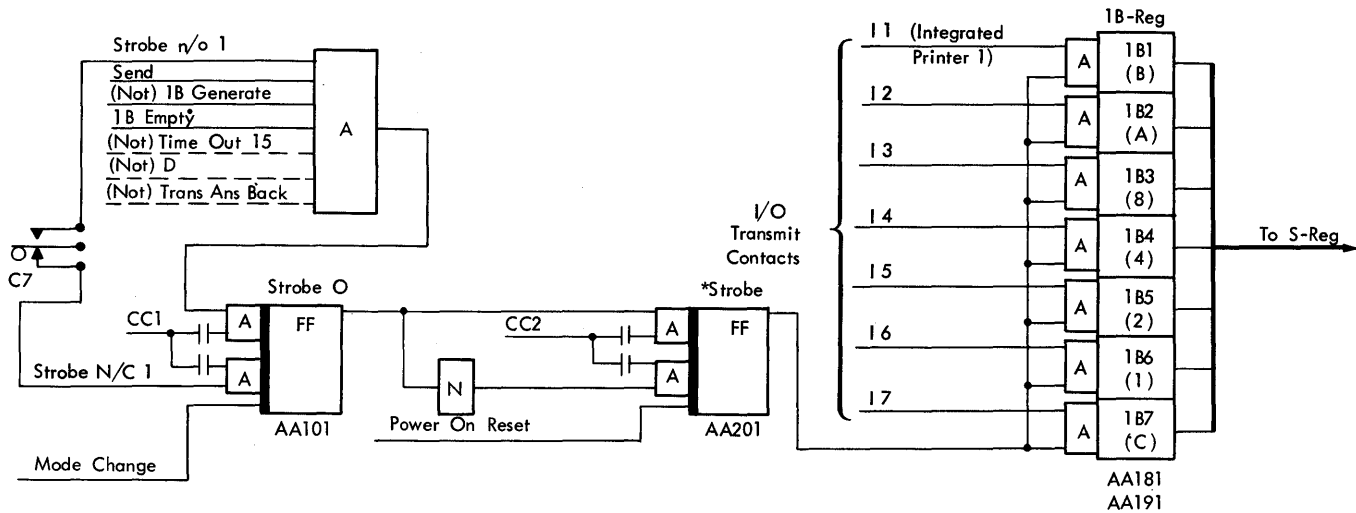
Figure 3-2. Transmit Text Characters

RECEIVE (POINT-TO-POINT)

- The 2740 receives either control or text characters.

- Control characters change mode operation.

- Text characters either print or cause a function to occur.

The 2740 is initially in control receive mode and is able to receive any character into the 1B-register. If the character is anything but a ⒟ character, nothing occurs. If, however, the character is a ⒟ , the 2740 goes into receive mode. The following paragraphs explain the receiving operation, starting with receipt of the ⒟ character, then the text characters, and finally the end-of-transmission character ⒞ . The flowchart (Diagram 5-5) shows the receiving sequence.

Receive Bid Character ⒟

- Receipt of ⒟ causes 2740 to go into receive mode.

- ⒟ is detected in 1B-register.

When the 2740 is to receive a message, the sending terminal sends the bid character ⒟ . The ⒟ character is received and detected, putting the receiving terminal into receive mode. If any character other than a ⒟ is received, the terminal remains in control receive mode.

The first bit to arrive on the communication line is the start bit. The serdes clock does not run continuously during receiving operations; therefore, the start bit starts the serdes clock. The start bit arrives (on the 'serial data in' line) at an AND conditioned by 'not send' (Diagram 5-6). 'Not send' is up for receive and control receive modes. The start bit turns off the 'S8' trigger and starts the serdes clock. (The S-register was previously restored to all-triggers-on when power was brought up or when the mode changed.) The start bit, along with 'not send' and 'S0,' also conditions an AND to turn on the 'enter serdes gate' trigger. The 'enter serdes gate' trigger gates on the 'enter serdes' trigger. After the character received by the S-register is transferred to the 1B-register, the 'enter serdes' and 'enter serdes gate' triggers cause the S-register to be restored.

Meanwhile, the bits arriving on the 'serial data in' line are gated into 'S8' and from there are shifted

down through the S-register until the start bit reaches the 'S0' trigger. The 'S0' trigger off (ANDed with 'enter serdes' and 'not C1') starts the control clock. The sequence of the control clock pulses is 'not C1' and 'not C2,' 'C1' and 'not C2,' 'C1' and 'C2,' and 'not C1' and 'C2.' 'C1' and 'not C2' reset the 1B-register <u>before</u> the character transfers; 'C1' and 'C2' provide the '1B set' pulse to transfer the character from the S-register to the 1B-register.

'1B set' is brought up by an AND (Diagram 5-6)-- the main conditions of which are 'C1,' 'C2,' 'S8,' and 'not S0.' ('S8' and 'not S0' indicate that a complete character is in the S-register.) 'C2,' 'not send,' and 'not 2B set' turn off the 'enter serdes gate' trigger, bringing up one condition of an AND to the 'S register restore.' The other conditions are 'not send' and the 'enter serdes' trigger on. When the 'enter serdes gate' trigger goes off, it conditions an AND to gate off the 'enter serdes' trigger. The time between the turning off of the 'enter serdes gate' trigger and the turning off of the 'enter serdes' trigger is 'S register restore' time. The character is now in the 1B-register; the S-register has been restored and is ready to accept the next character.

Because this is the first character sent, a Ⓓ is in the 1B-register. The Ⓓ character is detected (Diagram 5-6) and the 2740 goes into receive mode. The mode change resets the Ⓓ from the 1B-register.

Receive Text Characters

● Text characters are received up to the 1B-register the same as control characters.

● Text characters transfer to the 2B-register.

● Characters are checked to determine whether they are function or print characters, and are gated to the appropriate circuit.

The 2740 is now in receive mode. The Ⓓ character has been reset from the 1B-register and the terminal is ready to receive the first text character. The first text character arrives on the 'serial data in' line, shifts down through the S-register, and transfers to the 1B-register like the Ⓓ character. When the character is in the 1B-register, the '1B full line' comes up. If (1) 2B is empty, (2) the character in 1B is a valid character, and (3) 2B is not resetting (main conditions), the '2B set' trigger turns on (Diagram 5-6). '2B set' transfers the character from the 1B-register to the 2B-register. '2B set' also starts the control clock. '2B set' and the 'C1' and 'C2' outputs of the control clock reset the 1B-register a

second time (the first time before the character was set into the 1B-register).

The output of the 2B-register inputs to both the print-decode and function-decode circuits. At this point, the character is checked to see if it is a print or function character. The appropriate circuit is then gated by either 'print' or 'non print function.' To transfer the character to the gated circuit, the 'print out' line must come up. When the character transferred to the 2B-register, the '2B full' line came up. '2B full' and 'not I/O cycle' bring up the 'print out' line, decoding the character and transferring it to the gated print or function circuit.

Once the character has started the operation of the I/O device, the 2B-register is reset in preparation for receipt of the next character. The condition of the I/O device is indicated by the 'I/O cycle' latch. The 'IOC N/O 1' line from the I/O device turns on the 'I/O cycle' latch. '2B full,' 'not 2B set,' 'not 2B reset gate,' and the 'I/O cycle' latch turn on the '2B reset' trigger. The '2B reset' trigger output conditions one leg of an AND to the '2B reset' line (Diagram 5-6) and, with 'I/O cycle,' provides a gate to turn on the '2B reset gate' trigger. The output completes conditioning the AND, causing 2B to reset. The '2B reset' trigger turns itself off at the next 'CC2' pulse, but '2B reset gate' stays on until 'I/O cycle' goes down. This prevents unwanted '2B resets.'

Receive End-of-Transmission Character Ⓒ

● Receipt of Ⓒ character causes 2740 to go into control-receive mode.

● Ⓒ character is detected in the 1B-register.

At the end of the message, the EOT character Ⓒ is received. The Ⓒ character causes the receiving 2740 to go into control receive mode.

The Ⓒ character is received exactly like the Ⓓ character. When the Ⓒ character is in the 1B-register, it is detected (Diagram 5-6), and the terminal goes into control receive mode. The mode change does not occur until the operation of the previously received character is completed (when 'EOS and not O' comes up). The mode change brings up 'mode change,' which resets the Ⓒ character from the terminal registers. The terminal is now free to send or receive data.

2B Overflow Reset

● Detects characters being supplied to printer at excessive rate.

• Resets the 2B-register.

• The character in 2B is lost.

Characters can arrive at the 2740 at a faster rate than the printer can print them. In this error condition, the 2B-register is reset and the character is lost. The excessive line rate activates the overflow-reset circuit.

'Overflow reset' comes up when characters are in the 1B- and 2B-registers ('1B full,' '2B full') and a character has shifted down through the S-register to the point that the 'S1' trigger is turned off by the start bit. 'SD1,' 'SD2,' 'SD3,' and 'not 2B set' and 'not 2B reset gate' complete conditioning an AND (Diagram 5-6) to develop the 2B overflow reset. '2B overflow reset' resets the 2B-register by bringing up both the '2B reset' and '2B reset gate' triggers, developing '2B reset.'

POWER-ON RESET (2740-1/2741)

• The terminal is reset when power comes up.

• Power supply relay (K1) provides the power-on reset.

• The terminal is also reset if 'data set ready' drops.

When power comes up, the 2740 goes into control receive mode. Most triggers and all registers should be reset. The reset state can be either off or on, depending upon circuit requirements. The triggers and registers are reset either directly by the 'power on reset' line or, following the mode change, by the 'mode change' line.

When the Off-On switch is turned on, ac power is applied to the dc power supply (Diagram 4-10). At the same time, ac power is supplied to relay K1. The dc power is present some milliseconds before the pick of K1 is completed. Power-on reset occurs during this time.

The K1-3 operating point is connected to ground. The N/C point goes to a converter. As soon as dc power comes up, the output of the converter brings up the 'power on reset -X' line, conditioning the OR to the 'power on reset' line. When the pick of K1 is completed, the 'power on reset -X' line drops, completing power-on reset.

'Power on reset' also turns on the 'mode change' trigger, bringing up 'mode change.' Between 'power on reset' and 'mode change,' the terminal triggers and registers reset; the terminal goes into control

receive mode, ready to start sending or receiving. As shown in Figure 3-3, lack of 'data set ready' causes a power-on reset. If the terminal has the dial-up feature, loss of carrier causes a power-on reset.

I/O MOTOR CONTROL (2740-1/2741)

• In communicate mode, the I/O motor runs only when the terminal can send or receive text characters.

• The I/O motor runs continuously in local mode.

In control-receive mode, the terminal must be ready to receive information without operator assistance. In this mode, the I/O device can be inactive for several hours at a time. The I/O motor should not run during these standby periods because of the unnecessary heat and wear. The circuit shown in Diagram 4-10 controls the motor contactor and provides for the several conditions under which the I/O motor must turn on. If any of the input conditions to the OR are met, the I/O motor turns on. The conditions to run the I/O motor (for the basic terminal) are:

1. 'Not comm'--runs motor when the terminal is in local mode.
2. 'Not A' or 'not B'-- runs motor when the terminal is in any mode but control-receive.
3. 'Initial lowercase' and 'I/O cycle'--allow the I/O device to be shifted if, when first turned on, it is in uppercase. ('I/O cycle' acts as an overlap to keep the motor running until the shift is complete.)

KEYBOARD LOCK (2740-1/2741)

• Locks keyboard to prevent unintentional pressing of keys.

• Locks keyboard during carrier-return, tab, receive mode, control-character generation, and for one second at beginning of transmit mode.

The keyboard-lock circuit prevents operation of the I/O keyboard during the times when an error results if a key is unintentionally pressed. These times are:

1. When a long function (carrier-return or tab operation) occurs.
2. When the terminal first goes into transmit mode. A 1-second delay prevents operation

of the keyboard until the motor comes up to speed.
3. When the terminal is in receive mode.
4. When a control character is generated.
5. When the line adapter cannot accept data.

The logic needed to generate keyboard lock during these conditions is shown in Diagram 4-10. The keyboard is locked for a carrier return or tab by the 'long function' line. This line inputs to 'OR 1.' 'OR 1' can also be conditioned by the output of an AND. One condition to the AND is the 'not local' line. 'Not local' holds the AND deconditioned when the terminal is in local mode, thus holding the keyboard unlocked. The other leg of the AND is from 'OR 2.' 'OR 2' can be conditioned by the output from the 'time-out 1' latch, '1B generate,' ' Ⓒ ,' or 'not send.' The 'time-out 1' latch inserts a 1-second delay before unlocking the keyboard when the terminal goes into transmit mode. When the 'B' trigger goes off, an AND is conditioned to the input of a 1-second delay. The output of the delay goes to an AND that turns on the 'time-out 1' latch. One second after the 'B mode' trigger turns off, the 'time-out 1' latch turns on. During this one second, the keyboard remains locked.

Whenever a control character is to be sent, the '1B generate' line comes up. During this time, the keyboard remains locked. If the control character is a Ⓒ , the keyboard must be locked until the terminal returns to control receive mode. '1B generate' and ' Ⓒ ' immediately lock the keyboard and keep it locked until the mode change is completed.

When the terminal is in receive mode, the keyboard is held locked by the 'not send' line.

If the line adapter (data set or modem) cannot accept data, the 'not clear to send' line keeps the keyboard locked.

INITIAL LOWERCASE (2740-1/2741)

● Causes the I/O device to shift to lowercase, when in control-receive mode.

This circuit insures that the I/O device begins each operation in lowercase. The I/O shift mechanism is designed for both manual and electrical operation. Either the keyboard shift-lock or the latching of the shift magnets can lock the I/O device in uppercase. The initial lowercase circuit will shift the I/O device to lowercase for either condition.

The keyboard shift-trip mechanism in the I/O device is operated by the logic shown in Diagram 4-10. When an uppercase condition exists during control receive mode and communicate, the 'initial lowercase' flip latch turns on and conditions the shift-trip magnet driver. The shift-trip magnet moves the keyboard shift-lock pawl from its keeper. During the shift-down operation, the flip latch holds the pulse on the magnet until the I/O device returns to lowercase. When it does, the 'UC1' signal deconditions the flip latch and the pulse is removed from the magnet.

If the I/O device is latched in uppercase by the shift-magnet armature latch, the above operation does not restore the I/O device to lowercase. The I/O device must be shifted to lowercase by pulsing the shift magnet. 'Initial lowercase' inputs to an OR to the shift-magnet driver. With 'initial lowercase' conditioned, the shift-magnet driver is conditioned and the lowercase magnet is picked.

INCORRECT CASE (2740-1/2741)

● If the I/O device is in the same shift as the received shift character, 'incorrect case' comes up.

● 'Incorrect case' causes a hyphen to be printed.

When the sending terminal sends an uppercase or lowercase shift character, the receiving terminal shifts into the desired case. However, the terminal may already be in the desired case. If this occurs, the previously sent characters might have been printed in the wrong case. The operator must be notified of an error. Figure 3-3 shows the circuit used to indicate this error.

When the shift character is in the 2B-register, the condition of the case contacts, located in the I/O device, is sampled. If the I/O device is in uppercase and receives an uppercase character, the 'incorrect case' line comes up. The same thing occurs if the I/O device is in lowercase and receives a lowercase character. 'Incorrect case' causes the T1 and R5 magnet drivers to be activated, printing a hyphen, which indicates to the operator that an error has occurred. The 'incorrect case' line also degates the ANDs to the shift magnet driver to prevent a shift attempt.

If the terminal is equipped with the record-checking feature, 'incorrect case' also turns on the 'error' trigger. When the receiving terminal performs an EOB-check, the condition of the 'error' trigger informs the sending terminal of the error.
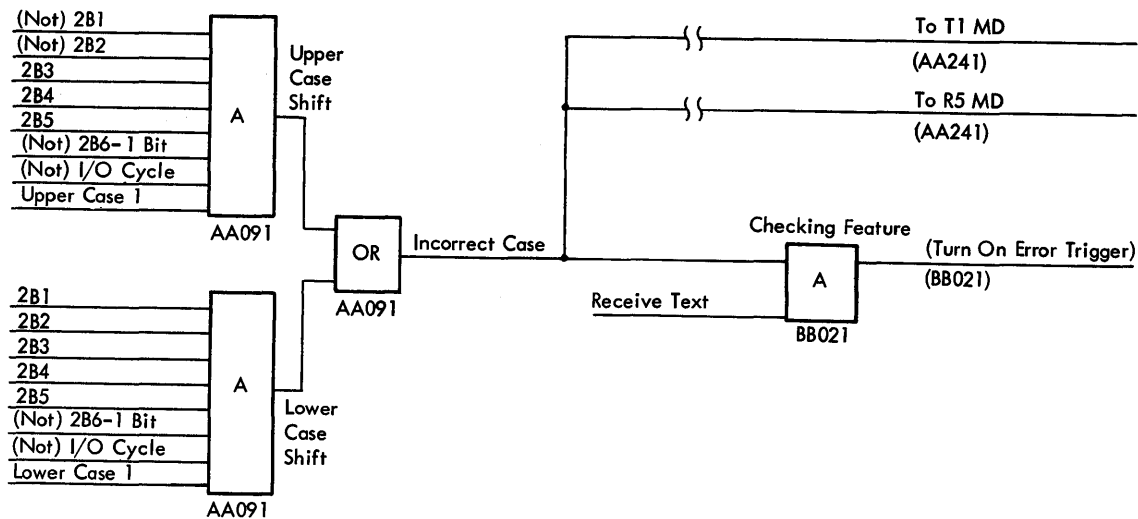
Figure 3-3. Incorrect Case

2741 COMMUNICATION TERMINAL

- Basic 2741 sending and receiving circuits are the same as in the 2740-1.

- Control receive mode with the Local/Communicate switch at COMM causes the terminal to go into transmit text mode and to send a Ⓓ .

- Pressing either the Carrier-Return or Attention key causes the terminal to send a Ⓒ and to go into receive control mode.

- In receive control mode, receipt of a Ⓒ puts the terminal into control receive mode; receipt of a Ⓓ puts the terminal into receive text mode.

The 2741 Communication Terminal is designed to be used only with a computer. The terminal operates point-to-point with the computer multiplexer.

The 2741 keyboard does not use the same control keys as the 2740. The only difference between the 2741 keyboard and a standard SELECTRIC® keyboard is the Attention key, which replaces the Index key. The standard character code used by the 2741 is correspondence code, although BCD code is available.

The basic 2741 sending and receiving circuits are identical to those of the 2740 except for the Ⓓ and Ⓒ control characters. As in the 2740, operations are controlled by the terminal modes: control-receive, transmit-text, receive-text, and receive-control.

Operation starts when the terminal is turned on. (Diagram 5-8). As in the 2740, a power-on reset places the 2741 into control receive mode. When the terminal is in control receive mode with 'communicate,' not 'initial lower case,' and not 'operate,' the 'bid' trigger turns on, loading a Ⓓ into 1B and placing the terminal into transmit text mode. The Ⓓ is sent to the multiplexer and informs the multiplexer that the terminal is on-line and in transmit text mode. The 2741 operator can send data until he presses the Attention key or the Carrier-Return key. A Ⓒ is then sent to the multiplexer, and the terminal goes into receive control mode.

In receive control mode, the terminal can receive either a Ⓓ or a Ⓒ . If a Ⓓ is received, the terminal goes into receive text mode, and the multiplexer sends its message. If a Ⓒ is received, the terminal first goes into control receive mode, loading a Ⓓ into 1B; and then to transmit-text mode, sending the Ⓓ . The operator can now send a message. After sending a Ⓒ , the terminal goes into receive control mode.

The primary objective of the following operation is to recognize the control character and then to change the terminal mode.

When (1) the terminal is in control receive mode, (2) the terminal is shifted to lowercase, (3) no operation is taking place, and (4) the Local/Communicate switch is at COMM, the 'bid' trigger

turns on (Diagram 5-9). The 'bid' trigger operates exactly as in the 2740 terminal, bringing up '1B generate,' which loads a Ⓓ character into the 1B-register. The 'B reset gate' comes up to place the terminal into transmit text mode and to send the Ⓓ. A message can now be sent in exactly the same manner as with the 2740.

When the operator presses the Carrier-Return or the Attention key, the 'EOT' trigger turns on. If the operator presses the Attention key, 'Attn 1' (Attention key N/O contacts) and the other conditions to 'AND 1' turn on the 'EOT' trigger. If the operator presses the Carrier-Return key, the carrier-return character is loaded into the 1B-register in the normal manner. The carrier-return code is recognized by 'AND 2' and (with 'send,' 'enter serdes,' and 'C1') turns on the 'auto EOT' trigger. 'Auto EOT' and 'not operate' turn on the EOT trigger when the carrier return is completed. The 'EOT' trigger operates exactly as in the 2740, bringing up '1B generate,' which loads a Ⓒ into the 1B-register.

Because the Shift key is not interlocked with any other key, the Carrier-Return key and the Shift key can be pressed at the same time. This causes the 1B-register to be loaded with an error character.

To ensure that the carrier-return character is generated and sent properly, the 'CR' latch turns on when the carrier-return contact (C6 N/O) makes. The 'CR' latch prevents the loading of bits into 1B-register positions 1B2 and 1B5. When '1B generate' comes up to load the Ⓒ character into 1B, the 'CR' latch turns off. The Ⓒ is detected and brings up 'A reset gate' (placing the terminal in receive-control mode), and turns off the 'auto EOT' trigger.

In receive control mode, the terminal can receive either a Ⓓ or a Ⓒ character. If a Ⓒ is received, the A and B set gates are brought up by 'not send,' 'not operate,' and ' Ⓒ ,' putting the terminal into control receive mode. A Ⓓ is loaded into 1B, and the mode changes to transmit text. The Ⓓ is then sent.

If a Ⓓ is received, the terminal goes into receive text mode. The 'B set gate' is brought up by 'not send,' 'not B,' and ' Ⓓ .' The multiplexer then sends its message and, when the message is completed, sends a Ⓒ . If the Communicate/Local switch is turned to LOCAL during any mode, the terminal returns to control receive mode by bringing up the A and B set gates.

TERMINAL MODE OPERATION

- All terminal operations are controlled by the terminal mode.

- Station control is standard on 2740-2.

- The terminal mode is determined by the conditions of the 'A,' 'B,' 'E,' and 'F' triggers.

- The terminal modes are the same as those for 2740-1 with Station Control.

Many of the circuits in the 2740-2 are the same as those used in the 2740-1 and its features. Therefore 2740-2 circuit explanations will be given only for those circuits that are:

1. Used differently from the 2740-1.
2. In addition to those of 2740-1.
3. Require special emphasis or review.

For the explanation of station control (standard on 2740-2), refer to "Station Control", Section 5 of Chapter 4.

Control Unit

- Contains the logic circuits, power supply, and the electronic buffer.

- Transmits a Ⓝ answerback character to the central processor when a station is polled and has nothing to send.

- Transmits Ⓓ followed by text if a bid has been made for the line and the station is polled by the processor.

- When addressed by the processor, the control unit responds with an Ⓨ indication if the station is prepared to receive the processor message.

- If the station is not ready when addressed by the processor, the control unit responds with a Ⓝ , ~~sets the attention indicator, and sounds the~~ audible alarm.

- When the terminal has finished receiving the message, it will transmit either a Ⓝ or Ⓨ indication to the processor if record checking is installed.

ENTER (2740-2)

- The terminal does not have status (status inhibit) during enter.

- Enter may be initiated in either local or communicate.

- Enter is established when the Enter key is pressed or (in Local) when buffer print ends.

- Enter unlocks the keyboard in communicate.

- Enter ends when the Bid key or the Reset key is pressed.

- While in enter, the backspace key will back buffer address one character position.

The purpose of the enter operation is to store a message that will be sent to the central computer location. Enter uses the I/O printer, the 2B register, buffer storage, and controlling circuits. Three definite phases of enter occur:

1. The initiation of enter starts with the pressing of the Enter key or the end of off-line buffer print and ends with the Enter indicator comes on.
2. Message is stored character-by-character.
3. The end of enter starts when the Bid key or the Reset key is pressed and ends when the Enter indicator goes off.

The following text describes the enter operation by sequence: start enter, enter characters, and end enter.

Start Enter

- Press Enter key.

- Reset buffer storage address.

- Shift printer to lower case if in upper case.

- Turn on 'enter' trigger and Enter light.

- Turn off standby indicator and drop 'status.'

- Start printer motor and unlock printer keyboards (communicate).

The two ways to start enter are: (1) press the Enter key to begin storing a message; (2) automatically at

the end of off-line (local) buffer print allow the operator to continue entering. To begin, press the Enter key if the Reset indicator is not on (if it is on, press the Reset key). This action brings up the 'Enter 1' line (Diagram 5-30). 'Enter 1' resets the buffer storage address and downshifts the I/O printer if it is in upper case. The 'ILC' (initial lower case) latch starts the motor, downshifts the printer, and turns off when the printer is in lower case. 'Lower case' and 'buffer address empty' are the main conditions needed for 'enter 1' to turn on the 'enter' trigger.

The 'enter' trigger will condition all the controlling circuits that transfer character codes from the I/O printer transmitting contacts to the 2B-register and into buffer storage. The 'enter' trigger inhibits status (Diagram 5-30), which allows the printer motor to continue running, and unlocks the keyboard. The Enter light comes on, the Standby light goes off.

Enter Characters

- Keyed action on I/O printer transfers the printer transmit contacts.

- Character code is set into the 2B-register through transferred printer transmit contacts.

- '2B reset' clears 2B latches that are not forced on.

- 'Strobe' and 'I/O cycle' timings control the set and reset of 2B, and delay the start of memory timing until the character is in 2B.

- '2B full' starts memory timing in enter.

- Memory timing runs for eight bit times 'buffer address time 0-7.'

- The character stores from 2B during the first seven bit times.

- Character parity is checked after storing.

- The 'buffer 2B reset' trigger operates at the eighth bit time.

- 'Buffer 2B reset' resets the 2B-register and drops '2B full.'

- Bell rings and enter light blinks 16-8 characters before end of buffer.

- Keyboard locks 8 characters before end of buffer.

- Check parity of all characters entering buffer.

- Backspace operation backs the character address one position and inhibits memory timing.

Circuit operation for storing a character is identical for every character that is stored. The printer cycles whenever a print character or a function is keyed. This cycle not only operates the transmit contacts, which provide circuits for each bit of the character code (Diagram 5-30), but also operates cycle timing contacts, which provide circuits for 'strobe' and 'I/O cycle' timing. The circuits for character bits enter terminal logic as I lines. Printer timings enter terminal logic as 'I/O cycle N/C,' 'I/O cycle N/O,' 'strobe N/C,' and 'strobe N/O.'

Load 2B from I/O:

1. Print or function is keyed.
2. Terminal 'strobe' sets the character bits into the 2B-register.
3. '2B full' and 'I/O cycle' turn on the '2B reset' trigger, which turns on the '2B reset gate' trigger. 2B latches not held on by input from the I lines are reset by '2B reset.' The '2BR' trigger turns off when 'I/O cycle' ends. 2B now contains the bits that represent the keyed character.
4. The 'memory go' line comes up, but memory timing cannot start until the 'strobe' line drops.

Store Character into Buffer from 2B (Diagram 5-30)

1. 'Strobe' drops 'memory go' comes up, and memory timing begins.
2. The bit counter steps from 7 to 0 and the character address advances one.
3. 'Buffer address time 0' sets the B-bit (2B1) into the 'memory buffer' trigger. The 'buffer odd parity' trigger flips if the B-bit is a binary "one."
4. The B-bit stores at the new character address and the 'memory buffer' trigger resets.
5. The bit counter steps, and steps 3 and 4 repeat as follows:

Buffer Address Time 1	A-bit (2B2)
Buffer Address Time 2	8-bit (2B3)
Buffer Address Time 3	4-bit (2B4)
Buffer Address Time 4	2-bit (2B5)
Buffer Address Time 5	1-bit (2B6)
Buffer Address Time 6	C-bit (2B7)

6. When the C-bit has been stored, the 'buffer odd parity' trigger should be on. An error is indicated if it is not on, the bell rings, and the keyboard locks.
7. In case of an error, press the Reset key to put out the light and unlock the keyboard. Backspace and retype the bad-parity character.

(Memory timing does not start on a backspace operation, and nothing is stored.) Even if the error occurred on a function, such as shift, backspace is necessary to back up the character address in buffer storage. Backspace effectively erases the bad-parity character code because the next character entered stores in place of the bad one at the same address.

8. The 'buffer 2B reset' trigger operates at 'buffer address time,' resetting the 'buffer odd parity' trigger and the 2B-register, and dropping the 'memory go' line.

9. Every keyed print operation or printer function stores its representative character code in the same manner.

End Enter

- Three ways out of enter: (1) automatic 15-second time-out, (2) press Reset key, (3) press Bid key.

- Reset key resets the buffer storage character address, the 'enter' trigger, the 'rekey' latch, and reset light.

- Reset key and communicate sets terminal to text non-selected mode.

- Pressing Bid downshifts the printer and stores the LC shift character if the printer is in upper case, stores the stop code (Ⓒ or Ⓑ), and resets the 'enter' trigger.

- Stop code stores just like a character code, except that Ⓒ or Ⓑ is automatically generated in 2B and the printer does not cycle.

- Bid in local mode does not set the 'bid' trigger. The 'buffer print' trigger turns on instead.

- 'Bid' and 'buffer address empty' will reset enter, no stop code is stored.

The 'enable enter time-out' latch allows the terminal to return to not enter status after 15 seconds of inactivity while in enter-communicate mode. 'Power on reset' resets the 'enable enter time-out' latch and the timer is inactive until the terminal transmits an address answerback or negative answerback to polling. 'Transmit answerback' sets the 'enable enter time-out' latch to activate the time-out circuits for current and/or subsequent enter operations (Diagram 4-13). If the Enter key is pressed and released in communicate mode the 15-second time delay is started by 'enable enter time-out,' 'enter,' 'communicate,' '2B empty,' 'not enter 1,' 'not line return N/C1,' and 'not line type N/C1.' Each time a character is entered through the

2B-register, '2B empty' drops to inhibit the time-out and to restart the time delay for another possible 15 seconds. The time-out is also inhibited by 'enter 1,' 'line return N/C1,' or 'line type N/C1' each time the Enter, Line Return, or Line Type key is pressed. (The Line Type and Line Return keys are not present on machines without the Edit feature.)

When the 15-second time-out occurs, '15 sec' 'not 1 cycle halt' and the condition which started the time delay are ANDed to set the 'time-out 15' latch. 'Time-out 15' and 'enable enter time-out' bring up a special 'reset N/O' line to reset the buffer, 'enter' trigger, and 'rekey' latch (if set). The Reset light (if on) is turned off when the terminal returns to not enter status.

Pressing the Reset key resets the buffer address (unless a character is still being entered) and then turns off the 'enter' trigger.

When the Bid key is pressed, conditions must be set up either to print out the stored message (local buffer print) or to send the stored message (communicate). The preparations for printout and for transmit are nearly identical (Diagrams 5-33 and 5-36).

The Bid key brings up the 'bid 1' line. 'Bid 1' downshifts the printer (if it is in upper case). If the printer shifts, the LC shift code stores in the same manner as any other character code (see "Enter Characters"). As soon as the printer is in lower case, the 'store stop code' trigger operates to generate the stop code (Ⓒ or Ⓑ) in the 2B-register. 'Memory go' rises immediately and is held up by '2B full' and 'enter.' The stop code enters buffer storage as the bit counter steps through 'buffer address time 0' through 6. At 'buffer address time 7,' the stop code in 2B turns off the 'enter' trigger and operates the 'buffer 2B reset' trigger to reset the 2B-register and the 'buffer odd parity' trigger. With '2B empty' and 'enter' off, 'memory go' drops, the Enter indicator goes out, and the enter operation is complete.

The following sequence summarizes the events at the end of enter:

1. Press Bid key.
2. Printer downshifts and LC shift code stores if printer is in upper case.
3. Stop code (Ⓒ or Ⓑ) is generated in 2B and stored in buffer storage.
4. The 'enter' trigger resets and the Enter indicator goes out.

NOTE: If no message is stored (buffer address empty) and the bid key is pressed with the Enter indicator on, no stop code is stored, and 'enter' ends with no further action. The 'enter' trigger resets and the Enter indicator goes out.

End Enter to Transmit

The 'bid' trigger sets to provide for the transition
from enter to transmit (Diagram 5-30). Gated by
the decoded stop code, 'buffer address time 7,' 'read'
and 'enter,' the 'CC2' pulse turns on the 'bid' trigger
and turns off the 'enter' trigger. 'Status' comes up
(is no longer inhibited), the keyboard locks, and the
motor stops. The 'bid' trigger stays on until the
first transmission character enters the S-register,
and indicates that the terminal has a message to send.

End Enter to Buffer Print

Buffer print occurs in Local mode when the Bid key
is pressed. 'Local' holds the 'bid' trigger off, but
allows the 'buffer print' trigger to turn on at 'buffer
address time 6' of the stop code. 'Status' is still
inhibited and the motor continues to run, but the key-
board locks for buffer print. The buffer print opera-
tion begins immediately (see "Buffer Print").

TRANSMIT (2740-2)

● A Ⓓ is generated and transmitted as the first
  message character.

● The contents of buffer storage are transferred, a
  character at a time, to the 1B-register.

● Each character is parity checked as it is read out
  of buffer.

● The character in 1B is transferred to the S-
  register and serialized to the transmission line.

● The final character from memory is a Ⓒ or Ⓑ .

● With Record Check installed, Ⓑ is followed by
  an LRC character which is generated by the LRC
  register.

This section explains the operation of the terminal
after it has been successfully polled. The procedure
for polling the terminal and placing it in transmit
text mode is explained under "Station Control"
Chapter 4, Section 5.

Generate and Transmit Ⓓ

The first character that the terminal sends to the
central processor (Ⓓ) does not come from buffer
storage, but is generated and loaded directly into
the 1B-register (the same as 2740-1). Operation of
buffer storage is prevented until after transmission
of this character.

Transmit Text Characters

Once in the 1B-register, all characters, whether
generated or from buffer storage, are transmitted
in the same manner as the 2740-1. The buffer cir-
cuits are activated for read out by 'transmit text'
and '1B empty (Diagram 4-18).

Transmit Ⓒ or Ⓑ

Each character is transmitted until the stop code
character, Ⓒ or Ⓑ , is detected in the 1B-register.
This character turns on the 'end of state' trigger.
'End of state' prevents a '1B reset' until a mode
change occurs. The transmission of the Ⓒ will
return the terminal to the control receive mode.
The Ⓑ will place the terminal in the transmit LRC
mode (record checking).

RECEIVE (2740-2)

● The 2740-2 receives either control or text char-
  acters.

● Control characters change mode operation.

● Text characters either print or cause a function
  to occur.

● Receive in the 2740-2 is identical to the 2740-1
  receive with Station Control (Diagram 5-6).

BUFFER PRINT (2740-2)

● The terminal does not have status (status inhibit)
  during buffer print.

● Buffer print is initiated manually by pressing the
  Bid key while in Local-Enter mode.

● Buffer print ends when the stop code at the end
  of the stored message is reached.

● The end of buffer print, local, automatically sets
  the terminal back to enter.

● Buffer print communicate takes place only on
  terminals with the Buffered Receive feature, but
  is explained here because it is similar to Local
  buffer print.

The purpose of the buffer print operation is to print
out the contents of buffer storage.

The buffer print operation has three phases:

1. The transition into buffer print--from local enter or from receive text buffer on terminals with the Buffered Receive feature.
2. The buffer print operation, during which the I/O printer prints the characters and performs the functions.
3. The transition out of buffer print--to enter, if in Local mode or to the Standby condition (TNS or CR) from buffer print, communicate, on terminals with the Buffered Receive feature.

Start Buffer Print

● Pressing the Bid key (local) places the printer in lower case and stores the shift character (if necessary) and then generates the Ⓒ or Ⓑstop code in 2B.

● Stop code turns on 'buffer print' and turns off 'enter.'

● Buffer Address resets as 'buffer print' sets.

● Buffer print (Communicate) takes place on terminals with the Buffered Receive feature and begins when Ⓒ is received.

Buffer print, local or communicate mode, begins when a stop code is decoded in the 2B-register. The generated Ⓒ or Ⓑ stop code starts local buffer print; the received Ⓒ stop code starts communicate buffer print.

Transition to Buffer Print from Receive Text Buffer (Buffered Receive)

A receive text buffer message may end with a Ⓑ and LRC if Record Check is installed. This control character does not store nor does it cause the stored message to print out. Printout begins only when the Ⓒ is received and stored. The Ⓒ control character turns on the 'set buffer print' latch and decodes as a stop code in the 2B-register. The memory timings used to store the Ⓒ allow the 'set buffer print' latch to turn on the 'buffer print' trigger and reset the buffer address. The 2B-register resets and the 'memory go' line comes up. The 'buffer print' or 'enter' line comes up and the standby indicator goes out. The keyboard remains locked, but 'status inhibit' comes up and the I/O printer motor starts (Diagram 5-36).

Buffer Print Operation

● Reads out character codes from buffer.

● Memory timing times readout of the seven bits that make up each character code.

● I/O cycle times 'memory go' and '2B reset.'

● Character code parity is checked on readout.

The transition to buffer print ends with the 'buffer print' trigger on and the 'memory go' line up. Buffer storage timing starts as soon as the buffer address is reset. The sense amplifier sets a binary one from a core into the 'memory buffer' trigger, and character-bits begin to set into the 2B-register.

As each binary one sets into the 'memory buffer' trigger during buffer print, the 'buffer odd parity' trigger flips (Diagram 4-18). Each character code contains an odd count so the 'buffer odd parity' trigger should be on when the character code has been completely read out at the end of 'buffer address time 6.' If not, the 'rekey' latch turns on, the bell rings, and the Reset indicator comes on. There is no assurance of what will print for the error character. The 'buffer odd parity' trigger resets to its initial off condition when the 2B-register resets.

An "incorrect case" in the stored message inhibits the shift function and prints a hyphen (-) in its place (Diagram 5-36).

At 'buffer address time 7', the '2B full' line comes up and the character code in 2B is decoded for tilt-and-rotate or function input to the I/O printer. 'Memory go' drops and the printer starts a cycle. The 'I/O cycle' timing signifies that the printer has begun its cycle and no longer needs the decoded output of the 2B-register. The '2B reset' trigger turns on, followed by the '2B reset gate' trigger and 2B resets. The '2B reset' trigger turns off, but '2B reset gate' stays on until the 'I/O cycle' line drops. This prevents repetitive reset of the 2B-register, and allows it to be used again immediately.

The 'memory go' line comes up again after 2B resets, and memory timing starts again. The next character code reads out to the 2B-register. The '2B full' line comes up again and 'memory go' drops, with a new character code in 2B (even though the printer has just begun to print or perform the function demanded by the previous character code).

NOTE: It takes only about 2° of the printer cycle to read a character code out of buffer storage.

The 2B reset circuits cannot operate again until the 'I/O cycle' line drops and comes up again so the unprinted character waits in 2B. When the 'I/O cycle' line drops, the new character is decoded for tilt-and-rotate or function and the printer continues from one cycle directly into the next. The 'I/O cycle' line rises; 2B resets; 'memory go' comes up; the readout-and-print repeats for the next character.

Printout continues, character-by-character, until a stop code appears (Ⓑ or Ⓒ in 2B, or end-of-memory in the address register). The stop code initiates the transition out of buffer print.

End Buffer Print

- Turn off 'buffer print' trigger.

- In local buffer print, return to enter and reverse buffer address one character (the stop code is effectively erased).

- In communicate buffer print, reset buffer address and turn on the Standby indicator.

The decode of a stop code in the 2B-register at the end of 'buffer address time 6, ' turns off the 'buffer print' trigger and the 'buffer print' line drops.

Transition from Buffer Print to Enter (Local, Diagram 5-36)

This transition returns terminal logic to enter. The stored stop code is automatically erased by backing up the buffer storage character address. When the stop code is complete in 2B, the next 'CC1' (start of write, 'buffer address time 6') turns on the 'edit control 3' trigger (Diagram 4-16). The 'buffer print' trigger turns off at the end of 'buffer address time 6' and the 'rev ctg seq' (reverse counting sequence) trigger turns on at the next 'CC2' (the same 'CC2' that turns on 'buffer 2B reset' to reset the stop code in 2B). 'Rev ctg seq' turns on 'reverse counter sequence control' at 'CC1' time to furnish the 'bfr. cntr. ac input' and back up the address. 'Rev ctg seq' turns itself off and the buffer storage address backs up one character location. Thus, the next character stored obliterates the stored stop code.

After the 'buffer print' trigger is turned off and the printer is in lower case, the next 'CC2' will turn on the 'enter' trigger. The 'edit control 3' trigger is on momentarily, and turns off at 'CC1' after 'enter' is turned on.

The keyboard unlocks, the I/O printer motor continues to run, and the Enter indicator comes on. The terminal is back in enter, with the only carry-over from buffer print being the possibility that an LC shift code was automatically stored and the printer downshifted immediately before the stop code. Upper case entry can be continued by simply shifting the printer from the keyboard.

Transition from Buffer Print to Standby (Buffered Receive Feature)

This transition returns the terminal logic to standby status and resets the buffer storage address. The resetting of the 'buffer print' trigger drops the 'status inhibit' line, the motor stops, and the Standby indicator comes on (if TNS or CR mode). The keyboard remains locked. The terminal logic can be manually switched to Local only after buffer print has ended (Diagram 5-9).

INITIAL LOWERCASE (2740-2)

- Causes the I/O printer to shift to lower case prior to entering, sending, or receiving.

This circuit insures that the I/O printer begins entering, sending, or receiving in lower case, so that the central processor can know what case the I/O printer is in at the beginning of a sending or receiving operation. The I/O printer is placed in lower case at the beginning of enter for operator convenience.

The I/O shift mechanism is designed for both manual and electrical operation. Either the keyboard shift-lock or the latching of the shift magnets can lock the I/O printer in upper case. The initial lower case circuit will shift the I/O printer to lower case for either condition

The keyboard shift-trip mechanism in the I/O printer is operated (Diagram 4-10) when an upper case condition exists:

1. At the beginning of enter;
2. At the end of enter (before transmission begins);
3. While the terminal is in control receive or text non-selected mode; or
4. When the terminal is addressed, but before receive text mode (control address selected mode),

the 'initial lower case' flip latch turns on and conditions the shift-trip magnet driver. The shift-trip magnet moves the keyboard shift-lock pawl from its keeper. During the shiftdown operation, the flip latch holds the pulse on the magnet until the I/O printer returns to lower case. When it does, the 'UC1' signal deconditions the flip latch and the pulse is removed from the magnet.

If the I/O printer is latched in upper case by the shift-magnet armature latch, the above operation does not restore the I/O printer to lower case. The I/O printer must be shifted to lower case by pulsing the shift magnet. 'Initial lower case' inputs to an OR to the shift-magnet driver. With 'initial lower case' conditioned, the shift-magnet driver is conditioned and the lower case magnet is picked.

INCORRECT CASE (2740-2)

- If the terminal is in the same shift as the received shift-character, 'incorrect case' comes up.

- Incorrect case causes a hyphen to be printed.

When the terminal receives a shift character, it shifts to the desired case. If already in that case, the previously received characters might have been printed in the wrong case and the operator must be notified. Diagram 2-2 shows the circuit that indicates this error.

When the shift character is in the 2B-register, the condition of the case contacts, located in the I/O printer, is sampled. If the I/O printer is in upper case and receives an upper case character, the 'incorrect case' line comes up. The same thing occurs if the I/O printer is in lower case and receives a lower case character. 'Incorrect case' causes the T1 and R5 magnet drivers to be activated, printing a hyphen, which indicates to the operator that an error has occurred. The 'incorrect case' line also degates the ANDs to the shift magnet driver to prevent a shift attempt, and turns on the 'error' trigger. During transmit check answerback, the 'error' trigger is sampled, causing a Ⓝ to be transmitted to the central processor.

KEYBOARD LOCK (2740-2)

- Locks keyboard to prevent unintentional pressing of keys.

The keyboard-lock circuit prevents operation of the I/O keyboard during the times when an error results if a key is unintentionally pressed or when it is undesirable to print a character. These times are:

1. When a long function (carrier-return or tab) occurs.
2. During buffer print operations.
3. Eight characters before end-of-memory (enter mode).
4. When an error occurs.

5. During ledger card insertion.
6. When the platen is split.
7. During any non-enter condition in communicate.

The logic needed to generate keyboard lock is shown in Diagram 4-10. The keyboard is locked for a carrier return or tab by the 'long function' line. 'Buffer print' locks the keyboard during buffer print operations. 'Enter' and the buffer address value shown in Diagram 4-10 lock the keyboard eight characters before the end of memory. 'Rekey' locks the keyboard when an error occurs; the keyboard cannot be unlocked until the Reset key is pressed. During ledger card insertion, the keyboard is locked when the card chute is not closed. This is accomplished by bringing up the 'insert card,' 'drive down,' and 'drive up lines.' Any time the platen is split, the keyboard is locked by 'platen shift.' In communicate, the only time the I/O keyboard is unlocked is when the terminal is in enter. 'Not enter' and 'communicate' lock the keyboard at all other times.

I/O MOTOR CONTROL (2740-2)

- In communciate mode, the I/O motor runs only when the terminal can send or receive text characters.

- The I/O motor runs continually in local mode.

In text non-selected and control receive modes, the terminal must be ready to receive information without operator assistance. In this mode, the I/O printer can be inactive for several hours at a time. The I/O motor should not run during these standby periods because of the unnecessary heat and wear. The circuit shown in Diagram 4-10 controls the motor contactor and provides for the conditions under which the I/O motor must turn on. If any of the input conditions to the ORs are met, the I/O motor turns on. The I/O motor runs for the following conditions:

1. For initial lower case operations.
2. When the terminal is in local mode (off-line).
3. When the terminal is in receive text mode.
4. For enter and buffer print operations (status inhibit).
5. During a long function (carrier return, tab).
6. To complete an I/O cycle.
7. Control selected, transmit status answerback, and control selected modes--to get motor up to speed before going to receive text mode.

8. Transmit check answerback mode--to carry
   motor over to receive text mode.
9. During ledger card insertion.
10. Receive check answerback mode.
11. Transmit text mode.

LINE PARITY ERROR (2740-2)

● Light indicates transmit or receive parity error.

● A Line parity error does not alter terminal
  operation.

● Parity-Reset latch (light) must be reset by
  parity-reset switch.

The purpose of the Parity light is to indicate that the
terminal has detected a receive or transmit parity
error. The light and associated switch are operative
with or without the Record Checking feature.

In transmit mode 'SD3', 'not S-register empty'
and 'serial data out' bring up 'Xmit parity AC set'
and flip the 'Xmit odd parity' trigger(Diagram 2-2).
If this trigger is not on at the end of a transmitted
character, the 'parity error' latch will turn on.

During a receive text operation, several condi-
tions may set the 'parity error or not S8' latch
(Diagram 2-2). The latch output, 'not L' and
'receive text' sets the 'parity error' latch.

The 'parity error' latch and the Parity light will
stay on until reset by operating the Parity-Reset
switch. The latch being on does not alter the
terminal operation.

STORAGE LATCHES FOR ERROR RESPONSES
(2740-2)

● Electronic error latch is set for buffer VRC errors
  when the terminal with Buffered Receive feature
  is in (1) buffer print and communicate, or (2) re-
  ceive text buffer mode.

● I/O error latch is set when a printer error is de-
  tected by integrated printer feedback.

● Electronic errors on terminals without Buffered
  Receive feature cause the I/O error latch to be
  set.

● Receive parity error latch is set when the terminal
  receives a character (1) with VRC error or (2)
  without a stop bit in receive text mode.

● Transmit parity error latch is set when the term-
  inal transmits a character with a VRC error.

● When error or buffer busy conditions exist, the
  CPU is notified by a qualified Ⓨ sent by a ter-
  minal with receive status and a qualified Ⓝ sent
  by a terminal without receive status.

● A "no error" condition is indicated by a space,
  Ⓨ answerback.

● All error latches are reset when the qualified
  Ⓨ response is sent by the terminal.

● Error latches are not reset when a qualified Ⓝ
  is sent.

Electronic Error Latch

The parity of characters going into and out of buffer
are checked by the 'buffer odd parity' latch. If the
latch is not on at 'buffer address time 6,' 'vertical
current control gate,' and 'write' bring up the
'buffer VRC' line. 'Buffer VRC' and 'receive text'
set the 'error' latch (Diagram 2-2). 'Buffer VRC'
is also ANDed with 'receive text' or 'buffer print
and communicate' to set the 'electronic error'
latch. When the error latches are used to set up
the sense character answerback, the electronic
error has highest priority. Electronic errors do
not set the 'electronic error' latch if the Buffered
Receive feature is not installed.

I/O Error Latch

The I/O error latch is set when printer errors are
detected, if the terminal is in buffer print and
communicate mode for terminals with Buffered
Receive feature, or in receive text and not receive
text buffer mode for terminals without Buffered
Receive. Feedback information comes from the
transmit contacts in the I/O printer to control the
I/O check register which has a latch for each of
the seven bits. This register and an I/O check en-
able register are set by bits in the 2B-register at
print time. The two registers make it possible to
check for extra or missing feedback bits during the
actual print operation.

For simplicity of explanation let us assume that a
numeric "1" is to be printed and the 'I/O check 6
enable' and 'I/O check 6' latches will be used.
These two latches are used to detect a missing bit,
but the other six I/O check latches are needed in
order to check for extra bits.

The print cycle is initiated by the character '1'
in the 2B-register and the 'I/O cycle' line comes up.
The '2B reset' latch is turned on by 'I/O Cycle'
at 'CC2' time, and '2B reset' and 'I/O cycle'
bring up 'set I/O latches' before the 2B-register is

reset. 'Set I/O latches' and '2B6' set 'I/O check 6 enable' and 'I/O check 6.'

'Receive text and not receive text buffer' or 'buffer print and communicate' bring up 'I/O check enable' to allow the actual checking to be done. 'I/O check enable' and 'strobe N/O 1' set the 'I/O check strobe' latch which ANDs with 'integrated printer 6-1 bit' and 'I/O check 6 enable' to reset the 'I/O check 6' latch when printing is proper. If the 'integrated printer 6-1 bit' is missing, the 'I/O check 6' latch is left on during 'I/O error sample' time to indicate an error. Any extra bit, sensed by an integrated contact output, will set the respective I/O check latch. This is done by the integrated printer contact output, 'I/O check strobe' and not 'I/O check enable' latch (not set by 2B-register). Thus, an extra bit also leaves an I/O check register latch set during 'I/O error sample' time.

Reset of the I/O Check and the I/O Check Enable registers, the 'I/O error sample' and the set of the 'I/O error' latch are under the control of the 'I/O check control 1' and I/O check control 2' sequence started by 'I/O check strobe.' 'I/O check strobe' allows 'CC1' to set 'I/O check control 1' trigger which stays on until the 'CC1' pulse after 'I/O check control 2' comes on. After 'I/O check strobe' is reset by 'strobe N/C 1' 'I/O check control 2' is set at 'CC2' time by 'I/O check control 1' and 'not I/O check strobe.' At this time the strobe operation is complete, the I/O check register is set (for errors only) and 'I/O error sample' is brought up by 'I/O check control 1' and 'I/O check control 2.' For any missing or extra bit 'I/O check register full' and 'I/O error sample' set 'I/O error' latch. 'I/O check enable' and 'not I/O check inhibit' are also necessary to allow 'I/O error' set.

'Rekey I/O error' is set or inhibited under the same condition that control the 'I/O error set' as described above.

If either an 'incorrect case' error or a '2B overflow reset' condition has occurred, the error latch is set. Either of these conditions along with 'I/O check enable' will set the 'I/O check inhibit' latch and inhibit an I/O error condition.

At the end of the I/O check operation, the I/O check and I/O check enable registers are reset by 'reset I/O latches' brought up by 'I/O check control 2 and not control 1.'

If the Buffered Receive feature is not installed, the 'I/O error' latch is set indirectly by an electronic error as well as an I/O print error. For example, an electronics failure may cause a printable evenparity character to be set into the 2B-register and, in turn. into the I/O check and I/O check enable register. A parity difference is sensed, due to the odd parity of the feedback contacts, when the char-

acter is printed. Therefore, the 'I/O error' latch is set instead of the 'electronic error' latch and the I/O error becomes the highest priority error condition with added significance. When the terminal with receive status is addressed after an electronic failure, the positive answerback sense character indicates that an I/O error has occurred. The importance of and the additional possible cause of such an error indication should not be overlooked.

If the Buffered Receive feature is installed, the I/O error has a priority second to electronic error when a qualified ⓨ answerback is sent by an addressed terminal with receive status.

When the 'rekey' latch is set because of an I/O error, it can be reset only by pressing the Reset key.

Receive Parity Error Latch

The receive parity error latch is set when the terminal receives a character with a VRC error or if the S8-stop bit is missing. Either of these two conditions sets the 'parity error or not S8' latch (Diagram 2-2). 'Receive text,' 'not L mode latch,' and 'parity error or not S8' set the 'receive parity error' latch. The same conditions set the 'parity error' latch which turns on the Parity Error light.

Receive parity error has third priority when a qualified ⓨ answerback is sent by the terminal.

Transmit Parity Error Latch

The transmit parity error latch is set when a character with a VRC error is transmitted by the terminal. The 'serial data out' is checked by 'transmit odd parity' trigger which should be on to indicate proper transmission. If it is not on, 'not transmit odd parity' and 'not S-register full' set the 'transmit parity error' latch. This error condition has lowest priority when the 1B-register is set by 'load 1st character answerback.'

TRANSMIT-STATUS/ANSWERBACK

A terminal with receive status sends a qualified ⓨ , two-character answerback, when it is addressed. If any errors have been sensed and stored during the previous communication operation the 'load 1st character answerback' loads the 1B-register with the character which represents highest priority error sensed. '1B generate' is delayed while this character is sent, so the ⓨ will be the second character transmitted.

If the terminal has status, all error latches are reset after '1st status character answerback' drops.

Status and Operational Error Conditions

If an addressed terminal is not ready to receive data, a qualified (N) will be transmitted as the answerback. Any error conditions stored because of previous operations will not be affected.

If the addressed terminal is in 'enter and communicate,' or 'bid' mode, the computer program should poll the terminal before readdressing it. Otherwise the terminal would continue to send the qualified (N) as a response and it would not return to receive status.

When the terminal has bid status, 'bid latch' and 'load 1st character answerback' set a 2 bit in the 1B-register and the 2, (N) are sent as the answerback. When the terminal has enter status in communicate mode, 'communicate,' 'enter,' and 'load 1st character answerback' set a 1 bit in the 1B-register and 1, (N) are sent.

If the terminal is addressed while in 'buffer print and communicate' a 4 bit is set in 1B-register to be sent as a response to the CPU. The 4 bit is set into the 1B-register by 'buffer print,' 'communicate,' and 'load 1 st character answerback.'

If the terminal is out of paper, in local mode, or has the document insertion device down, the terminal is considered to have an operational error condition and a qualified (N) is transmitted to notify the CPU program. The Attention light comes on and the alarm sounds. When the terminal regains status the Attention light goes off. A9, (N) is sent for an out-of-paper condition; 8, (N) for local mode; and @, (N) for insertion device down.

When the terminal is out of paper, 'not status inhibit,' 'not bid latch,' 'not paper,' and 'load 1st character answerback' set the 1 bit, 8 bit, and C bit in the 1B-register for the sense character answerback.

When the terminal is in local mode, the 8 bit is set in 1B-register by 'not communicate,' and 'load 1st character answerback.'

If paper is in the feed and the insert device is down, an @ is set in 1B-register by 'paper,' 'not bid latch,' 'not status inhibit,' 'insert card,' and 'load 1st character answerback.'

TERMINAL TO LINE-ADAPTER INTERFACE (ALL MODELS)

- Line adapters connect terminals to communication lines.

- The connections between the line adapter and the terminal form the interface.

Because dc voltage is used by the 2740/2741 terminal, data cannot be sent directly to another terminal. The bits making up a character musr be changed to another form for transmission, by connecting the terminal output to a line adapter. The line adapter can be either a common-carrier data set or an IBM modem (modulator-demodulator). The connecting circuits and lines between the line adapter and the terminal are the interface.

The following paragraphs explain the function of the interface lines in the 2740/2741 terminals. For some of the line adapters the descriptions might vary in use due to the use of half duplex, full duplex, special features and operation with multiplexers. Diagram 5-47 shows the interface for all line adapters used with the terminals.

Signal Ground-AB

This line serves as the signal voltage reference between the line adapter and the terminal.

Transmitted Data (Serial Data Out)-BA

This is the data-out line from the terminal to the line adapter. Data generated in the terminal is sent out on this line.

Received Data (Serial Data In)-BB

This is the data-in line from the line adapter to the terminal. Data received by the terminal arrives on this line.

Data Set Ready-CC

This line from the line adapter indicates to the terminal that the line adapter has power and can communicate.

Request to Send-CA

This line from the terminal tells the line adapter that the terminal is prepared to send data. In the adapter, this line usually generates the carrier frequency.

Clear To Send-CB

When the line adapter is in a condition to send data, 'clear to send' comes up to allow the terminal to begin sending.

Carrier-CF

This line comes up when 'carrier' from the sending line adapter is received and detected by the receiving line adapter. 'Carrier' coming up allows the terminal to receive data.

Originate (Used Only for 103 F Data Set)-CY

This line puts the 103 F data set into answer mode. For half-duplex operation, data sets on both ends of the line are in originate mode. In order to send data, one of the data sets must be put into answer mode. The 'originate' line serves this purpose. When 'request to send' is brought up in the terminal, the 'originate' line, normally held up, drops. For full-duplex operation, the 'originate' line is held down, keeping one set of communication lines in answer mode and the other in originate mode.

Data Terminal Ready (Used Only for 103A Data Set)-CD

This line from the terminal to the line adapter controls the operation of the 103A data set. If the line is up (indicating that the terminal has status and the Dial-Disconnect key has not been pressed), the dial connection is maintained; if the line drops, a dial disconnect begins.

SECTION 1. RECORD-CHECKING (2740-1/2740-2)

INTRODUCTION

● Data is checked vertically and longitudinally.

● Parity errors (VRC) are indicated by a hyphen printed at the receiving terminal.

● Sending terminal starts the EOB-check.

● Response to EOB-check indicates accuracy of reception.

Record-checking is a method whereby the great majority of sending and receiving errors are detected. Each character received is checked vertically for odd parity (vertical redundancy check); the entire message is checked longitudinally by maintaining an odd-even count of each bit position as the characters are sent and received (longitudinal redundancy check). This latter count (LRC) is maintained at each terminal. The receiving terminal's response to periodic sending-terminal inquiries indicates the accuracy of data received.

Vertical Redundancy Check (VRC)

VRC uses the odd-bit count of each character received to test the accuracy of received data. If the bit count of a character is even, the gain or loss of a bit is indicated; a hyphen is printed at the receiving terminal to alert the operator of an error. Also, an error trigger within the terminal turns on to later advise the sending terminal (or central processor) of an error.

Longitudinal Redundancy Check (LRC)

LRC uses an odd-even count of bits in each bit position to develop a 7-bit LRC-character. This character is developed in the sending terminal during transmission. The receiving terminal (or central processor) also develops an LRC-character at the same time.

The presence of a bit within the LRC-character indicates that an odd number of bits has been sent in that position; the absence of a bit indicates an even number of bits has been sent. Because the same data generates the LRC-character at both terminals, the characters should be identical. No comparison between the LRC-characters is made,

however, and no LRC-error can be recognized until an end-of-block check is made.

End-of-Block (EOB) Check (2740-1)

During the sending operation, the sending terminal receives no indication of errors. Periodically, the sending terminal operator checks the receiving terminal (or central processor) for accuracy of reception by pressing the EOB key on the I/O keyboard. This automatically compares the LRC-characters developed at each location and checks the 'error' trigger at the receiving location. Any terminal error is then indicated at the sending terminal by printing a hyphen, ringing the alarm bell, and locking the terminal.

Operation: When a block of information is to be checked, the sending terminal initiates the EOB-check. A Ⓑ character, followed by the LRC-character, is sent to the receiving location. The LRC-characters are then compared to determine whether a longitudinal error has occurred.

Sending the Ⓑ character places the terminal into transmit-LRC mode. In transmit-LRC mode, the terminal sends the LRC-character, after which the terminal goes into receive-check/answerback mode. In this mode, the Receive light, Restart light, and motor are on; and the terminal waits for an answer from the receiving location.

If a Ⓨ answerback is received (message received correctly), the terminal returns to transmit-text mode and transmission continues. If a code other than a Ⓨ is received, the terminal prints a hyphen, rings the alarm bell, and shifts to transmit-text/lock mode. In this mode, the keyboard is locked and the Transmit light, Restart light, and motor are on. The lock condition exists until either the EOT or Restart key is pressed. The restart operation returns the terminal to transmit-text mode. The EOT operation sends a Ⓒ and places the terminal into control-receive mode. If the terminal is receiving the message, the EOB check is initiated at the other location.

The terminal, upon reception of the Ⓑ character, goes into receive-LRC mode. This mode conditions the terminal circuits to recognize the next character as an LRC-character. The motor and the Receive light are on, and the parity-error circuit is inhibited. The circuit is inhibited because the LRC-

character can correctly have either an odd or even bit count. Reception of the LRC-character places the receiving terminal into transmit-check/answerback mode. In this mode, the received LRC-character is compared to the LRC-character developed within the receiving terminal. If the characters do not compare, the 'error' trigger turns on, and a hyphen is printed.

The condition of the 'error' trigger also determines the response that is returned to the sending location. With the 'error' trigger on, a Ⓝ negative response is sent; with the 'error' trigger off, a Ⓨ positive response is sent. In either case, the receiving terminal returns to receive text mode.

End-of-Block (EOB) Check (2740-2)

For the 2740-2, the end-of-block check is performed with every transmission. If an error is detected at the central processor, the terminal is notified and the message is retransmitted until either the message is received correctly or the central processor tells the terminal to quit sending. If the latter occurs, the Reset light turns on and the alarm bell rings.

Operation: The last Character of each buffer message is the Ⓑ which is generated when the Bid key is pressed. Following the transmission of the Ⓑ , the developed LRC character is sent. The modes used to accomplish this are the same as for the 2740-1. The 2740-2 then goes to receive check answerback mode.

If the 2740-2 receives a Ⓨ answerback, a Ⓒ is generated and transmitted and the terminal goes to control receive mode. If any character other than a Ⓨ or Ⓒ is received, the terminal returns to transmit text mode and resends the message. Retransmission continues until either the message is received correctly (Ⓨ answerback) or a Ⓒ is received. Reception of a Ⓒ while in receive check answerback mode causes:

1. The Reset light to turn on
2. The keyboard to lock
3. The alarm bell to ring
4. The terminal to go to control receive mode

If the 2740-2 is receiving a message, the EOB check is initiated by the central processor like the 2740-1.

NOTE: The hyphen is not printed on terminals equipped with Buffered Receive.

FUNCTIONAL UNITS

Parity Error (VRC)

- The 'parity error' trigger ('receive odd parity' trigger in 2740-2) is first turned on at start bit time.

- Each data bit changes the state of the 'parity error' trigger.

- Stop bits are not checked.

- The 'parity error' trigger on at the end of a character indicates a parity error.

- A parity error turns on the 'parity error or not S8' latch.

The parity-error circuit is used only in receive mode. The 'parity error' trigger ('receive odd parity' trigger in 2740-2) first turns on when the start bit arrives. Each succeeding data bit turns the 'parity error' trigger on or off. When a complete in-parity character is received, the 'parity error' trigger is off. When a character containing a parity error is received, the 'parity error' trigger is on.

The input to the parity-error circuit is the output of the 'S-register' trigger, 'S8.' 'AND 1' (Diagram 2-1) is conditioned by 'S8,' 'not send,' the 'parity error' trigger off, and 'not L' ('not L' disables the parity-error circuit when the LRC-character is received). 'AND 2' is conditioned by 'S8,' 'not send,' and the 'parity error' trigger on. If the 'parity error' trigger is off, it is turned on by the next bit; if the 'parity error' trigger is on, it is turned off by the next bit.

The parity check starts when the start bit is received by the S-register. Because the 'parity error' trigger is first turned off and 'S8' trigger turned on by 'S-register restore,' the SDAC that gates the start bit to 'S8' turns the 'parity error' trigger on. The 'parity error' trigger turns on and off as the bits are received. If the received character is in parity, the 'parity error' trigger will be off at stop-bit time. The condition of the 'parity error' trigger is tested when the start bit reaches 'S0.' 'Not S0' signals the terminal that the complete character has been received. Because of this timing, the stop bit is not included in the parity check.

If the stop bit is absent from the character (usually caused by line trouble), the 'S8' trigger is off. Because the stop bit should turn the 'S8' trigger on, the absence of a bit in 'S8' indicates loss of the stop bit.

Either the 'parity error' trigger on or the absence of a stop bit turns on the 'parity error or not S8' latch. 'Parity error or not S8,' ANDed with 'not L' and 'receive text,' turns on the 'error' trigger. The 'error' trigger is tested during the EOB-operation.

> NOTE: The 2740-2, with or without Record Checking, always parity checks received characters. Without Record Checking an out of parity character turns on the Parity light; the central processor is not notified of the error. With Record Checking, the 2740-2 operates as previously explained and the Parity light turns on.

Error Trigger

The 'error' trigger (Diagram 2-1, 2-2) informs the terminal when one of the following errors has occurred:

1. An LRC-error
2. The absence of a stop bit
3. A parity error
4. A 2B overflow reset
5. Incorrect case
6. Buffer VRC error (2740-2 only)

The condition of the 'error' trigger, when sampled, indicates an error to the terminal.

LRC-Register

- The LRC-character is developed in the LRC-register.

- Characters enter the LRC-register from the 1B-register.

- All text characters and the Ⓑ character form the LRC-character.

- Comparing is accomplished when the transmitted LRC-character is entered into the LRC-register.

- If any LRC-register triggers are on after the comparison, an error is indicated.

The LRC-register (Diagram 4-12), consists of seven triggers, one for each data-bit position. The input to the LRC-register is from the 1B-register. Each LRC-register trigger is turned on or off by the input data bit. If the trigger is on, it turns off; if the trigger is off, it turns on. Thus, an account of each data-bit position is kept. Figure 4-1 shows the theory of LRC-register operation. Note that if an odd number of any given data bit is gated to an LRC-register trigger, the trigger is on for the check

Transmission Characters

LRC Latch	I		B	M	2	7	4	Ⓑ	Generated LRC-Char
L1	B ↑	B ↓	B ↑						B
L2	A ↑	A ↓						A ↑	A
L3	8 ↑							8 ↓	
L4				4 ↑		4 ↓	4 ↑	4 ↓	
L5			2 ↑		2 ↓	2 ↑		2 ↓	
L6	1 ↑					1 ↓			
L7	C ↑			C ↓				C ↑	C

↑ Turn On LRC-Register Latch
↓ Turn Off LRC-Register Latch
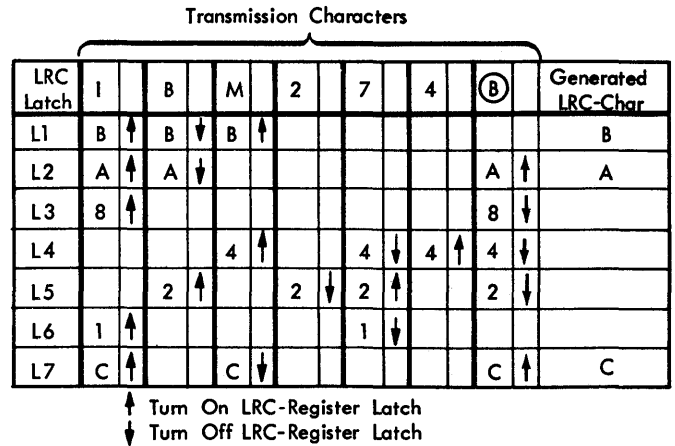
Figure 4-1. LRC Register Operation

character; if the number of bits is even, the trigger is off.

If the terminal is sending, the LRC character is developed and sent when the EOB operation is initiated. If the terminal is receiving, the LRC character is developed and compared when the LRC is received from the sending location. To compare characters, the transmitted LRC-character is received and entered into the LRC-register. All triggers that are on should turn off and none should turn on. If any triggers are left on, 'LRC error' comes up (see Diagram 4-12).

Control of the LRC-register is shown in Figure 4-2. All characters sent or received while the terminal is in a "text" mode are entered into the LRC-register. In transmit-text mode, when 'enter serdes,' 'C1,' and 'time-out 1' are up, the 'set LRC' trigger turns on. 'Set LRC' gates the character from the 1B-register to the LRC-register. The 'set LRC' trigger then gates itself off. Another AND, conditioned by 'transmit text,' 'enter serdes,' 'C1,' and 'not Ⓓ ,' also turns on the 'set LRC' trigger. 'Not Ⓓ ' prevents the Ⓓ character from entering the LRC-register. For the model 2 the 'not Ⓓ ' line is replaced by 'transmit Ⓓ .' The 'transmit Ⓓ ' trigger does not turn on until after the first character (Ⓓ) is transmitted.

In receive-text mode, 'receive text,' 'C1,' and 'not 2B set,' turn on the 'set LRC' trigger. 'Set LRC' occurs at the same time as '1B set.'

The LRC-register is reset by the 'reset LRC' trigger. The trigger turns on when the 'L' mode trigger is off and the mode changes. The 'reset LRC' trigger then turns itself off. The 'L' trigger input allows the Ⓑ character to be set into the LRC-register.
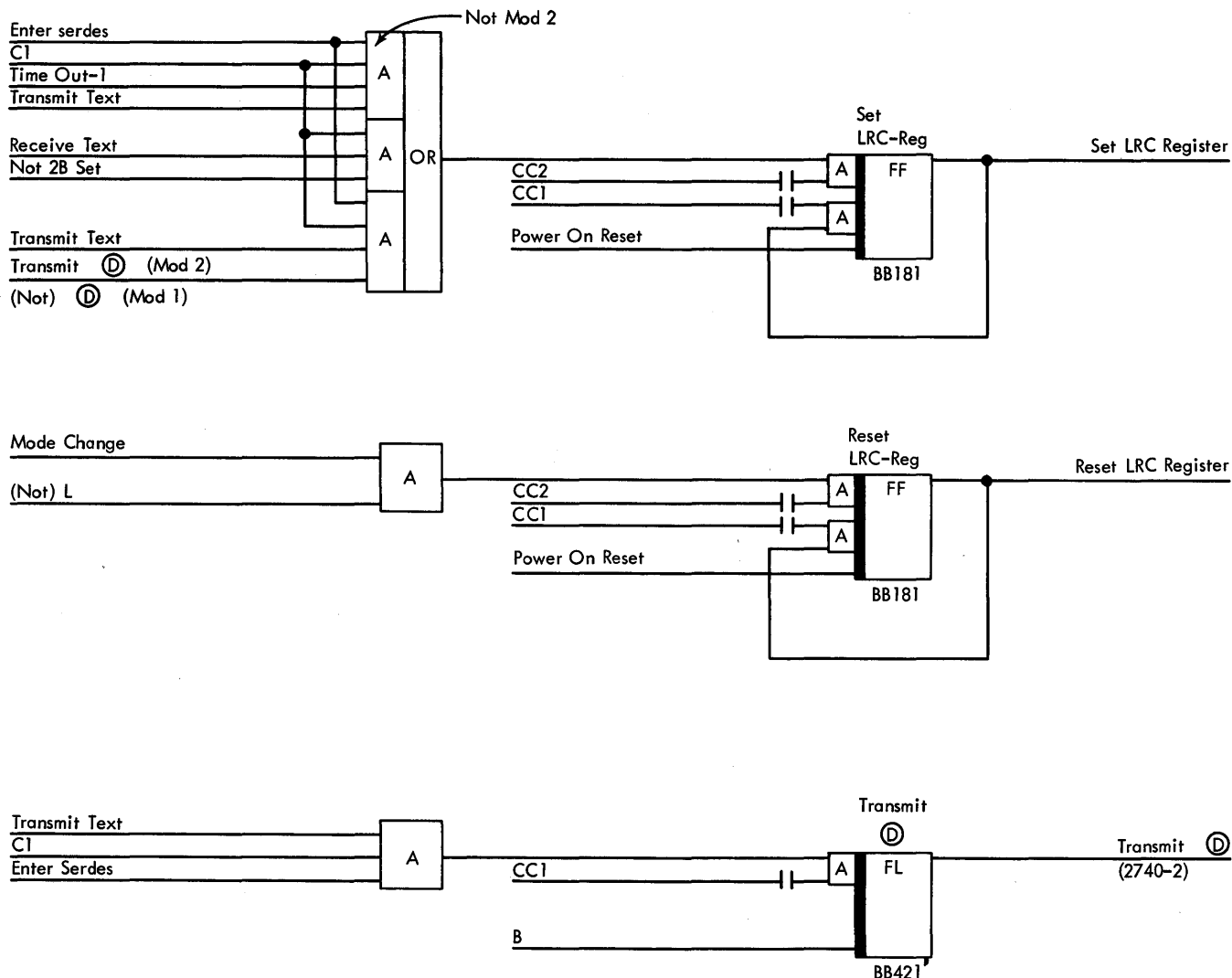
Figure 4-2. LRC Register Control

Mode Control

- Additional mode triggers are required for Record Checking.

The terminal mode determines the action the terminal performs. To enable the terminal to change to the additional modes needed for the Record Checking feature, more mode triggers are required. Diagram 5-12 shows all the mode trigger inputs for the 2740-1. Diagram 5-28 shows all the mode trigger inputs for the 2740-2.

The terminal mode is determined by various combinations of mode triggers on. Figure 4-3 defines the mode trigger(s) that turn on for each mode. Control receive, transmit text, and receive text modes are the same as for the basic terminals.

The additional modes used for Record Checking perform the following functions:

Transmit LRC--causes the terminal to send the contents of the LRC register (LRC character).

Receive LRC--allows the terminal to accept the LRC character and compare it with the one it has developed.

Transmit check answerback--causes the terminal to sample the 'error' latch and to return the result ((Y) or (N)).

Receive check answerback--allows the terminal to accept the answerback character ((Y) , (N) , or (C)).

Transmit text lock (2740-1 Only)--Causes the terminal to lock up if a negative answerback ((N)) is received.

TRANSMITTING TERMINAL

MODES	A	B	D	F	L
Control-Receive	1	1	0	0	0
		↓			
Transmit-Text	1	0	0	0	0
				↓	↓
Transmit-LRC	1	0	1	0	1
					↓
Receive-Check/Answerback	1	0	1	0	0
See Note 1				↓	
Transmit-Text/Lock	1	0	1	1	0
See Note 2 and 3			↓	↓	
Transmit-Text	1	0	0	0	0
		↓			
Control-Receive	1	1	0	0	0

Note 1: Depending on response, the transmitting terminal may go to either transmit-text/lock or transmit-text mode.

Note 2: From transmit-text/lock mode the transmitting terminal may go to either transmit-text mode (Restart key depressed) or to control-receive mode (EOT key depressed.)

Note 3: 2740-2 does not use Transmit-Text/Lock mode.

RECEIVING TERMINAL

MODES	A	B	D	F	L
Control-Receive	1	1	0	0	0
		↓			
Receive-Text	0	1	0	0	0
					↓
Receive-LRC	0	1	0	0	1
				↓	↓
Transmit-Check/Answerback	0	1	1	0	0
				↓	
Receive-Text	0	1	0	0	0
	↓				
Control-Receive	1	1	0	0	0

Figure 4-3. Sequence of Mode Operation, Record Checking

Figure 4-3 shows the sequence of operation of the mode triggers for both transmitting and receiving operations.

PRINCIPLES OF OPERATION

Transmit EOB-Character (2740-1)

- Pressing the EOB key at the sending terminal starts the operation.

- The Ⓑ character (A842C) is placed in the 1B-register by '1B generate' and '1B set.'

- From the 1B-register the character is sent normally.

- Sending the Ⓑ changes the terminal to transmit-LRC mode.

Sending the EOB-character (Ⓑ) is much the same as sending the Ⓓ and Ⓒ characters. Pressing the EOB key while the terminal is in the transmit-text mode turns on the 'EOB' trigger(Diagram 5-14). The 'EOB gate' trigger interlocks the 'EOB' trigger to ensure that a single EOB-operation is performed regardless of the length of time the EOB key is held.

'EOB' coming on produces '1B generate.' Because the I/O device is inactive during this operation, '1B generate' is required to place the Ⓑ in the 1B-register. Similarly, because the 'strobe' signal is not produced, '1B set' must be developed. '1B generate' starts the control clock, producing the '1B set' pulse. '1B generate' and '1B set' place the Ⓑ into the 1B-register. From the 1B-register, the Ⓑ transfers to the S-register and is sent the same as any other character. '1B full' conditions 'enter serdes gate' to turn on; 'enter serdes gate' turns on 'enter serdes,' which starts the transferring sequence. 'Enter serdes' turns off the 'EOB' trigger, dropping '1B generate.' 'EOB gate' turns off when the operator releases the EOB key. The Ⓑ is also loaded into the LRC register.

While the Ⓑ is in the 1B-register, it is detected and, with 'enter serdes,' turns on the 'end-of-state' latch (Diagram 5-14). The 'end-of-state' latch prevents the reset of the 1B-register. When the operation is completed, the 'operate' trigger turns off. End of state and not operate ('EOS and not O') and ' Ⓑ ' turn on the 'D' and 'L' mode triggers. 'A,' 'D,' and 'L' mode triggers put the terminal into transmit-LRC mode. 'Mode change' resets the Ⓑ from the terminal registers.

Transmit EOB Character (2740-2)

For the 2740-2, the Ⓑ is generated and loaded into buffer storage when the Bid key is pressed. The EOB operation does not begin until the Ⓑ is detected in the 1B-register during transmission. Following recognition of the Ⓑ , the EOB operation for the 2740-2 is exactly the same as for the 2740-1.

Transmit LRC-Character

- 'Transmit LRC' brings up the 'transmit answer-back' line.

- 'Transmit answerback' and '1B empty' start the control clock.

- '1B set' transfers the LRC-character to the 1B-register.

- '1B full' is forced up by 'parity error or not S8.'

- The LRC-character is placed into the S-register and sent normally.

- Sending the LRC-character changes the mode to receive-check/answerback.

The change to transmit-LRC mode brings the 'transmit LRC' and 'transmit answerback' lines up (Diagram 5-14). 'Transmit answerback' and '1B empty' start the control clock to produce the '1B set' pulse. 'Transmit LRC' and '1B set' transfer the LRC-character from the LRC-register to the 1B-register.

After the LRC-character transfers to the 1B-register, the '1B full' signal must be produced to transfer the character to the S-register. The LRC-character can contain any bit configuration, including the combination in which all 1B-register triggers are off. To ensure that '1B full' is brought up under this condition, the 'parity error or not S8' latch is turned on by the '1B set' pulse, forcing up '1B full.'

The character is transferred to the S-register and transmitted normally.

The 'end-of-state' latch is turned on by 'transmit answerback' ('transmit LRC'), 'enter serdes,' and 'C1.' When character time is completed, 'EOS and not O' change the mode from transmit-LRC to receive-check/answerback by turning off the 'L' mode trigger. Mode change resets the LRC character from the 1B-register.

The sending terminal has now sent the EOB- and LRC-characters and is in receive-check/answerback mode, awaiting an answerback from the receiving location. The keyboard is locked.

Receive-Check/Answerback (2740-1)

- The EOB-check response is received in the normal manner.

- A positive response ($\textcircled{Y}$) changes the mode to transmit-text.

- A negative response ($\textcircled{N}$) prints a hyphen and changes the mode to transmit-text/lock.

- No response causes the terminal to lock in receive-check/answerback mode.

While in receive-check/answerback mode, the sending terminal receives the response to the EOB-check from the receiving location. Reception of the response character occurs normally. When the response character is in the 1B-register, the character is analyzed to determine subsequent action.

The $\textcircled{Y}$ character (BA821) is recognized as a positive response and brings the ' $\textcircled{Y}$ ' line up (Diagram 5-15). The $\textcircled{Y}$ character turns off the 'D' mode trigger, which places the terminal into transmit-text mode. The mode change resets the $\textcircled{Y}$ from the terminal registers. The $\textcircled{Y}$ is not printed because the mode change occurs before the character transfers to the 2B-register.

Any other response character is recognized as a not $\textcircled{Y}$, or negative response. This results in the development of a '2B set' pulse. 'Not $\textcircled{Y}$ ' and 'receive answerback' bring up '2B inhibit,' which blocks all normal inputs to the 2B-register. '2B1,' however, is turned on by '2B set' and 'receive answerback' (Diagram 5-15). A hyphen (B-bit) is entered into the 2B-register and the hyphen is printed. When the operation is complete, the 'operate' trigger turns off. (The 'end-of-state' latch turned on when '2B set' came up.) 'EOS and not O,' 'receive answer-back,' and 'D' mode trigger on turn on the 'F' mode trigger.

The 'A,' 'D,' and 'F' mode triggers (on) develop transmit-text/lock mode. The mode change resets the negative response character from the terminal registers. The terminal keyboard is locked. The operable control keys are the EOT and RST (Restart) keys. If the operator presses the EOT key, the terminal goes into control-receive mode. If the operator presses the Restart key, the terminal goes into transmit-text mode, and data transmission can continue.

It is possible that neither a positive nor a negative response is received as a result of the receiving location being off at the time the EOB-check is performed. In this case, the terminal remains in receive-check/answerback mode, with the keyboard locked until the Restart key or EOT key is pressed.

Restart

- Returns the sending terminal to transmit-text mode following an error response from the receiving location.

- Pressing the Restart key turns on the 'restart' trigger.

- The 'restart' trigger gates off the 'D' and 'F' mode triggers.

When an error response is received from the receiving location, the terminal goes into transmit-text/lock mode. To return the terminal to transmit-text mode, the operator must press the Restart key to turn on the 'restart' trigger. Figure 4-4 shows conditions. If the 'D' and 'F' mode triggers are on (transmit-text/lock mode) the 'restart' trigger provides a gate to turn the triggers off. The resulting mode change then turns off the 'restart' trigger.

Reverse Transmission: Terminals connected to a multiplexer are equipped with reverse transmission which causes the terminal to go into receive-text mode if a ⒟ is received in place of the response character. The circuit is shown in the dotted area on Diagram 5-15.

When the terminal is in receive-check/answerback mode and a ⒟ is received from the multiplexer, the 'B' mode trigger turns on, and the 'A' and 'D' mode triggers turn off.

Receive Check Answerback (2740-2)

- A ⓨ answerback returns the terminal to transmit text mode to transmit a ⓒ .

- A Ⓝ answerback returns the terminal to transmit text to retransmit the message.

- A ⓒ answerback on any transmission causes an error indication and a return to control receive mode.

- A ⒟ answerback places the terminal into receive text mode.

After transmission of the message, the terminal goes to receive check answerback mode. In this mode, a character is received from the central processor to indicate if the message was received correctly. If the terminal receives a ⓨ for an answerback, it returns to transmit text mode, transmits a ⓒ , then goes to control receive mode.

If the message was not received correctly at the central processor, it returns a Ⓝ character. This character causes the terminal to return to transmit text and to retransmit the message. The number of retransmissions is controlled by the central processor program.

The central processor could return a ⓒ as the answerback following any transmission; the terminal would go to control receive mode after indicating an error (the bell rings and the Reset light turns on).

If, after receiving the transmission, the central processor wishes to place the terminal into receive text mode without going through the addressing procedure (reverse transmission), a ⒟ is returned as the answerback character. This character places the terminal in receive text mode.

Refer to Diagram 5-16. The answerback character is received in the S-register and transferred to the 1B-register. If the transmission was received correctly at the central processor, a ⓨ char-
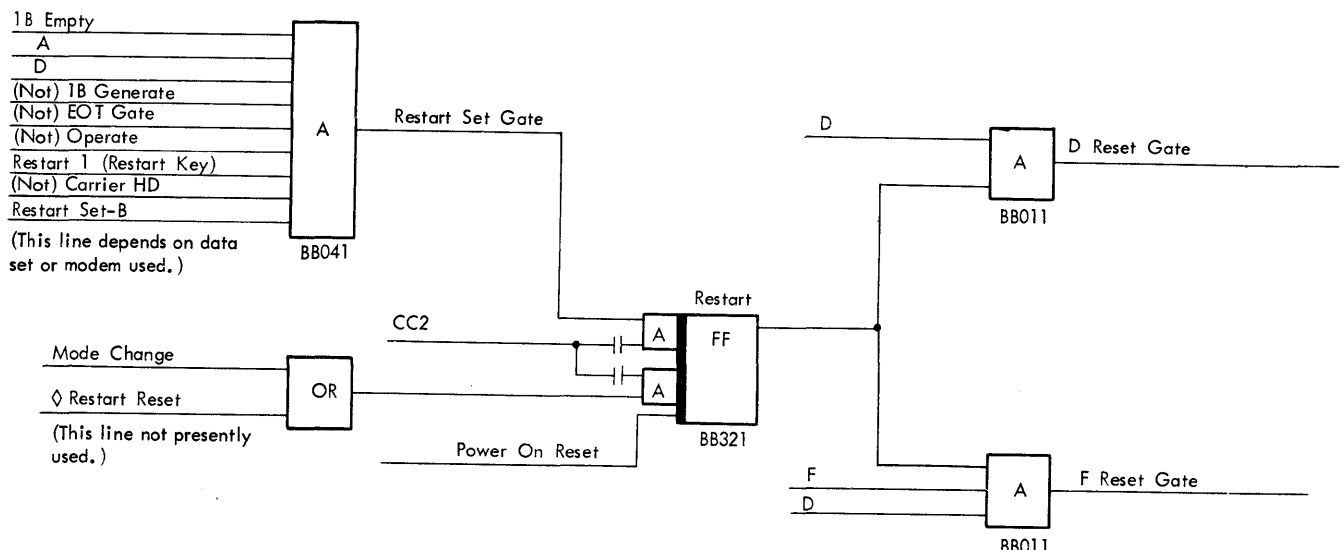

Figure 4-4. Restart Circuit

acter is now in the 1B-register. ' Ⓨ ,' 'Receive answerback,' and 'not C2' bring up 'D reset gate,' causing the terminal to return to transmit text mode. The terminal returns a Ⓒ character to the central processor and then goes to control receive mode.

If the message was not received correctly by the central processor, the terminal receives a negative answerback. 'Not Ⓨ ,' 'not Ⓒ ,' 'receive answer-back,' and '1B full' bring up 'receive negative answer-back'--which with 'not C1'--brings up 'D reset gate,' placing the terminal into transmit text mode. The terminal again transmits the message (except the Ⓓ) and returns to receive check answerback mode. If the message is received correctly by the central processor, a Ⓨ is returned; the terminal returns to transmit text mode, transmits a Ⓒ and then goes to control receive mode. If the message is not received correctly, the central processor may again return a Ⓝ character. Retransmission continues until the central processor returns a Ⓨ or a Ⓒ for the answerback. If a Ⓒ is received, 'receive ans-werback,' ' Ⓒ ' and 'not C1' turn on the 'rekey' latch. The 'rekey' latch turns on the Reset light, rings the alarm bell, locks the keyboard, disables the Bid and Enter keys, and blocks the status set gate (see Diagram 4-11). At the same time, 'set control receive' is brought up by 'not send,' 'not operate,' ' Ⓒ ,' 'not C2,' and 'not C1,' placing the terminal into control receive mode. The terminal remains locked until the Reset key is pressed. The operator can press the Bid key and, once polled, send the contents of buffer again or start over and re-enter the message.

Receive EOB-Character

- The Ⓑ character is received normally and puts the terminal into receive-LRC mode.

- '2B inhibit' prevents the transfer of the Ⓑ to the 2B register.

The EOB-character is received normally by the receiving terminal and is placed into the 1B-register. While in the 1B-register, the Ⓑ is detected and conditions an AND to turn on the 'L' mode trigger (Diagram 5-17). 'L' on puts the terminal into receive-LRC mode, conditioning the terminal to re-cognize the next character as the LRC-character. The Ⓑ is added to the LRC-register to complete the receiving-terminal LRC-character. The Ⓑ also brings up '2B inhibit,' which prevents the transfer of the Ⓑ to the 2B-register and the I/O device.

Receive LRC-Character

- The parity circuit is disabled for the LRC-character.

- The LRC-character is added to the LRC-register for comparison.

- Failure to compare turns on the 'error' trigger.

- The 'error' trigger is sampled; if the trigger is off, the mode changes directly to transmit-check/ answerback; if the trigger is on, the hyphen prints and the mode changes to transmit-check/ answerback.

Receive-LRC mode (1) disables the parity-check circuit for the LRC-character, (2) disables the '1B OK'circuit so that the LRC-character is not recog-nized as a control character (the LRC-character can be any bit configuration), and (3) forces up 'invalid character' to prevent a normal '2B set.'

The LRC-character is received and loads into the 1B-register. When 'set LRC' comes up, the LRC-character is added to the LRC-register. If the trans-mit and receive LRC-characters are the same, all LRC-register triggers turn off. This results in dropping the 'LRC error' line (Diagram 5-17). If an LRC-error has occurred, the LRC-characters do not compare, and one or more of the LRC-register triggers remain on. The 'LRC error' line remains up, indicating an LRC-error.

At this point '2B set' is brought up by forcing the 'parity error' or 'not S8' latch up. 'L,' 'not A,' 'not 2B set,' and 'C1' turn on the 'parity error or not S8' latch. 'Parity error or not S8' and other conditions shown on Diagram 5-17 bring up '2B set set gate,' turning on the '2B set' trigger. If the 'LRC error' line is up, '2B set' turns on the 'error' trigger. The 'error' trigger might already be on because of a previous error (parity error, no stop bit, etc.). '2B set' also turns the 'end-of-state' latch on.

If the LRC-characters compare, the 'error' trigger does not turn on; the terminal goes into transmit-check/answerback mode. If the 'error' trigger is on, a hyphen is printed, and the terminal goes into transmit-check/answerback mode. The circuit for printing the hyphen is as follows: '2B inhibit' prevents normal entry to all 2B-register triggers, except '2B1.' In the event of an error, the '2B1' trigger is turned on by '2B set,' the 'L' trigger on, 'receive text,' and 'C1' (Diagram 5-17). The B-bit is entered into the 2B-register and a hyphen is printed.

At the end of the printing operation, the 'operate' trigger turns off and 'EOS and not O' comes up. The 'D' mode trigger turns on, the 'L' mode trigger turns off, and the terminal goes into transmit-check/answerback mode. Depending upon the state of the 'error' trigger, the receiving terminal now returns either a Ⓨ or Ⓝ to the sending terminal.

Transmit-Check/Answerback

● Puts receiving terminal into a sending condition.

● Positive response (Ⓨ) sent if 'error' trigger is off.

● Negative response (Ⓝ) sent if 'error' trigger is on.

● After sending either response, the terminal returns to receive-text mode.

Transmit-check/answerback mode places the receiving terminal into a sending condition. Depending upon the condition of the 'error' trigger, a positive or negative response returns to the sending terminal.

The 'send' line is brought up by the 'D' and 'B' mode triggers. The 'send' line starts the serdes clock (Diagram 5-18), allowing the response character to be serialized to the 'serial data out' line.

The terminal now enters the correct response character into the 1B-register.

If the 'error' trigger is off, '1B generate' is brought up by 'D,' 'transmit answerback,' 'not L,' and 'not error.' '1B generate' provides gating to the '1B2,' '1B3,' '1B4,' '1B5,' '1B6,' and '1B7' latches. The control clock is started and brings up '1B set.' The Ⓨ (B, A, 8, 2, 1) is entered into the 1B-register. Note that the '1B4' and '1B7' latches are degated by 'not transmit answerback'; therefore, for a positive response, '1B set' turns on the '1B1,' '1B2,' '1B3,' '1B5,' and '1B6' latches. '1B1' is brought up by '1B set,' 'transmit answerback,' and 'not transmit LRC,' regardless of which response is sent.

If the 'error' trigger is on, '1B generate' does not come up. The control clock is started instead by 'not C2,' 'transmit answerback,' 'D,' and '1B empty,' which condition the 'Δ C1 gate' line. The control clock pulses again bring up '1B set.' But because '1B generate' is down, only the '1B1' latch turns on, and the Ⓝ negative response is sent.

When either response has been sent, the 'operate' trigger turns off. The 'end-of-state' latch was turned on by 'transmit answerback,' 'C1,' and 'enter serdes.' 'EOS and not O,' along with 'transmit answerback' and 'not transmit LRC,' turn the 'D' mode trigger off (Diagram 5-18). The receiving terminal now returns to receive-text mode, ready to receive data.

SECTION 2. AUTOMATIC EOB (2740-1)

- Record-checking feature is a prerequisite.

- Carrier-Return key generates carrier-return and starts EOB-sequence.

- Check switch selects auto-EOB off, terminal-to-terminal, or terminal-to-multiplexer.

- A second carrier-return is forced by a negative response to EOB-check.

- If the Auto-Check switch is in TERM, the second carrier-return character is sent; if the Auto-Check switch is at MPLX, the second carrier-return character is not sent.

The automatic-EOB feature starts the EOB checking sequence whenever the operator presses the Carrier-Return key. A switch permits the terminal operator to select any one of three auto-checking modes: OFF, TERM, or MPLX. The Check switch must be at either TERM or MPLX for the automatic-EOB feature to be used.

Diagram 5-13 illustrates the auto-EOB function. When the terminal is in transmit-text mode and the Check switch is at TERM or MPLX, a carrier-return started by the terminal operator causes a carrier-return character and the EOB- and LRC-characters to be sent. The LRC-character is sent and the terminal goes into receive check answerback mode. If a (Y) answerback is received, the terminal goes into transmit text mode. If a (N) answerback is received, a hyphen is printed to indicate the error response, and the terminal goes into transmit text lock mode.

If a restart is initiated by the operator, the terminal goes into transmit text mode; and a second carrier-return is performed. The second carrier-return, which occurs only when there is an error response to the EOB-check, synchronizes the communicating terminals to print subsequent data from the left margin. The second carrier-return character is sent if the terminal is connected to another terminal (TERM); the carrier-return is not sent if the terminal is connected to a multiplexer (MPLX).

When the operator presses the Carrier-Return key the I/O transmit contacts are strobed, transferring the carrier-return character to the 1B-register. The carrier-return code is detected and brings up the 'carrier return code' line (Diagram 5-19). The carrier-return character is sent normally as the carrier-return function is performed.

The 'auto EOB' trigger must turn on in order to generate the EOB-character. 'CR code' ANDed with 'auto check,' (transmit text), 'not auto EOB,' 'enter serdes,' and 'C2' turns on the 'auto EOB' trigger. Auto check is active when the check switch is at TERM or MPLX. 'Auto EOB' brings up 'EOB gate,' which turns on the 'EOB' trigger and starts the normal EOB/LRC transmit sequence.

After sending the LRC-character, the terminal goes into receive check answerback mode, awaiting a response from the receiving terminal. If a (Y) response is received, the terminal goes into transmit text mode. The mode change resets the 'auto EOB' trigger.

If the response is not a (Y), the terminal prints a hyphen and goes into transmit text lock mode. When the operator presses the RST key, the terminal goes into transmit text mode; and a second carrier-return is performed. The second carrier-return is caused by the 'force CR' latch. 'Receive answerback' and '2B set,' the same conditions that cause the hyphen to print, turn on the 'force CR' latch. 'Force CR,' 'ANDed with 'transmit text' (comes up when the RST key is pressed) and 'not I/O cycle,' pick the carrier-return magnet, performing the carrier-return.

'Strobe' transfers the carrier-return character to the 1B-register; if the Auto-Check Switch is at TERM, the character is sent. If the Check switch is at MPLX, 'C1 gate' comes up starting the control clock. The control clock outputs cause the carrier return character to be reset from 1B (Diagram 5-19). The 'auto EOB' trigger is reset by 'auto EOB,' 'CR code,' and 'C2.' The 'auto EOB' trigger off and 'CR code' reset the 'force CR' latch.

If the operator presses the EOT key instead of the RST key, the terminal goes into control receive mode. The 'auto EOB' trigger is then turned off by 'B'.

SECTION 3. DIAL-UP (2740-1/2741)

- Allows Western Electric 103A (or equivalent)to connect terminal to common-carrier communication system.

- Terminal is disconnected from system when Dial-Disconnect key is pressed.

The Dial-Up feature permits the 2740-1/2741 terminal to use the Western Electric 103A data set (or equivalent) to communicate over the common-carrier network (normal dial-telephone service). The terminal operator simply dials the telephone number of the terminal or multiplexer with which communication is desired; once the connection is established, messages can be sent or received. When carrier is received from the data set while the terminal is in control receive mode, the Dial-Connect light indicates that a connection has been established.

Figure 4-5 shows the interface from the terminal to the 103A data set. Note that most interface lines are similar to those used by other line adapters. One difference is that the 'clear to send' line is brought up (with a 45 ms delay for 2740-1, and 330 ms for 2741) when 'send' ('request to send') comes up. For an explanation of these common lines. see "Terminal to Line Adapter Interface."
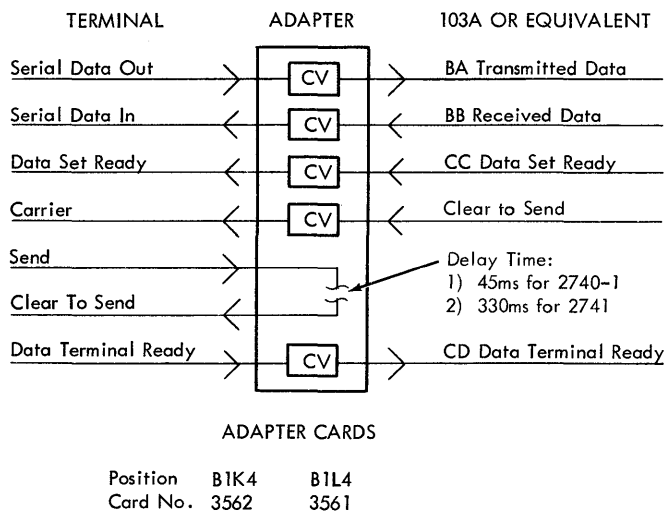
Figure 4-5. Dial-up Interface (103A)

The following "handshaking" procedure establishes a connection to another terminal or multiplexer data set.

Originating Data Set	Answering Data Set
Lift receiver and dial. * ──────►	Answer. *
	Auto answer or press data button. * (103A goes into and remains in data mode if 'data terminal ready' is up and remains up.)
	↓
	Wait 1.5 seconds for toll billing.
	↓
Receive F2M. ◄────────	Turn on F2M (answer carrier tone).
↓	
Push data button. *	
↓	
Wait 150 milliseconds; monitor F2M.	
↓	
Unclamp 'receive data' line.	
↓	
Wait 1.5 seconds (remove echo suppressors).	
↓	
Turn on F1M. ────────	► Receive F1M.
↓	↓
Wait 200 milliseconds (turn around time).	Wait 150 milliseconds, monitor F1M.
↓	↓
Bring up 'data carrier detect' and 'clear to send.'	Unclamp 'receiver data' line.
	↓
	Wait 200 milliseconds (turn around time).
	↓
	Bring up 'data carrier detect' and 'clear to send.'
	↓

Once the connection is established, the terminal operates point-to-point.

*Operator action

Dial-Disconnect

Because a charge is made for the common-carrier line only while in use, the terminal should be disconnected from the communication line when data cannot be sent or received. Therefore, the status of the terminal controls the data set. A loss of terminal status disconnects the terminal from the communication line. The disconnection is caused by the terminal dropping 'data terminal ready,' which signals the data set to disconnect. The terminal is also disconnected if the operator presses the Dial-Disconnect key on the I/O keyboard.

A special feature is available from the common carrier that permits both ends of the communication line to be disconnected when 'data terminal ready' drops. This feature requires no changes to the terminal.

The condition of 'data terminal ready' is determined by both the condition of the 'status' trigger and the 'dial disconnect' latch (see Diagram 5-47, Sheet 2). If the 'status' trigger is off (lack of paper, local mode, or loss of data-set status) 'data terminal ready' drops. Turning on the 'dial disconnect' latch (operator pressing the Dial-Disconnect key) also drops 'data terminal ready.'

Dial Up (2741)

The Dial-Up feature for the 2741 operates like the 2740, except when 'send' ('request to send') comes up, 'clear to send' is delayed 330 ms. The delay is needed for turn-around time. In the 2740, turn-around (from receive to transmit) is accomplished when the operator presses the Bid key. Operator action takes enough time to allow for the turn-around. In the 2741, the computer causes turn-around; additional time must be allowed before data can be sent.

SECTION 4. TRANSMIT CONTROL (2740-1)

- Allows a computer to control the sending or receiving status of the terminal.

- The terminal goes into receive mode when a Ⓓ is received.

- The terminal goes into transmit mode when a 2-character sequence (slash-space) is received.

- If, during a period of 15 seconds, no key is pressed, the 'time-out 15' latch turns on, causing the terminal to go into control-receive mode.

The transmit-control feature allows a computer to control the sending or receiving status of a terminal. The dial-up feature is a prerequisite. The terminal goes into receive mode when the multiplexer sends a Ⓓ character. This operation is identical to basic terminal operation.

The terminal goes into transmit mode when the multiplexer sends a special 2-character sequence (Diagram 5-25), which consists of a slash (/) followed by a space. Receipt of this 2-character sequence places the terminal into transmit mode and automatically causes a Ⓓ character to be returned to the multiplexer. Once the terminal is in either transmit or receive mode, it operates like a basic terminal.

The terminal goes into transmit text mode (Diagram 5-26) when the slash is received by the terminal. It is detected, and turns on the 'F' mode trigger. Turning the 'F' mode trigger on (with the 'A' and 'B' mode triggers already on) puts the terminal into intermediate control-receive mode, which conditions the terminal to receive the space character. The space is detected by an AND, the output of which, 'space,' goes to several AND's shown on Diagram 5-26. Space and 'intermediate control receive' turn off the 'F' and 'B' mode triggers and turn on the 'bid' trigger. This places

the terminal into transmit mode and causes a Ⓓ character to be sent. When the Ⓓ is sent, (1) the alarm bell rings, (2) the motor turns on, and (3) the keyboard unlocks. If the second character is not a space, the 'F' trigger turns off and the terminal returns to control-receive mode.

When the terminal is in transmit mode and the operator does not press any key for 15 seconds, the terminal returns to control receive mode. Diagram 5-26 shows the circuit. 'Not 1B generate,' 'send,' 'not test,' 'not strobe O,' 'not operate,' and '1B empty' condition an AND. This AND indicates that no operation is taking place. The output of the AND enters a 15-second time delay. If no operation occurs for 15 seconds, the time delay times out, and its output turns on the 'time-out 15' latch. The output of the latch turns on the 'B' mode trigger and blocks an AND to the input of the 'strobe O' trigger (to prevent further operations). The control clock must run in order to generate pulses to change the mode. The clock is gated on by the 'C1 gate.' The conditions to bring up this line are 'multiplexer transmit control,' 'not garble,' 'not C1,' and 'time-out 15' latch on. Transmission with the Transmit Control feature is ended normally by sending a Ⓒ character.

A 2-position switch is mounted on the side of the terminal. This switch can be in either the MTC (multiplexer transmit control) or the OFF position. While at OFF, the terminal operates normally, except the time-out 15 feature is retained.

Any telephone in the country can call a terminal and be connected. Therefore, the terminal must not become tied up if a non data-type telephone makes a connection. Only a data set or modem is capable of generating carrier; a standard telephone is not. Note on Diagram 5-26 that an AND inputs to the 'time-out 15' latch, the conditions of which are 'data set ready' and 'not carrier.' If 'data set ready' is up and no carrier is received for 15 seconds, the 'time-out 15' latch turns on. 'Time-out 15' and 'not-carrier' cause a dial-disconnect to disconnect the data set from the common-carrier lines.

SECTION 5. STATION CONTROL (2740-1/2740-2)

INTRODUCTION

● Allows more than one terminal to be connected to a computer (via a multiplexer) by a single communication line (Figure 4-6).

● A terminal is addressed to receive data.

● A single terminal, a group of terminals, or all terminals on the communication line can be addressed.

● A terminal is polled to send data.

● Only one terminal is polled at a time.

● Feature is standard on 2740-2.

A single communication line greatly reduces the cost of communication facilities to the customer. In order for terminals to communicate with the computer without contention (more than one terminal attempting to use the communication line at the same time), a special addressing and polling scheme is used.

Addressing prepares a terminal or group of terminals to receive data.

Polling informs an individual terminal that it alone can send data. Each terminal is polled in a predetermined order that is controlled by computer programming. To send data, the operator presses the Bid key before the next poll. When polled, the terminal goes into transmit text mode; the operator can then send a message.
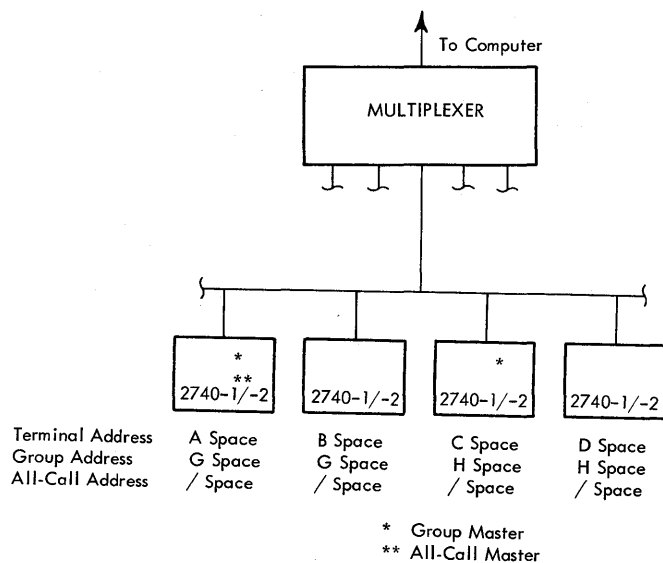
Addressing and polling are accomplished by sending a special sequence of characters to the terminal (Figure 4-7). Note that the Ⓓ, Ⓒ, Ⓝ, and Ⓨ characters are the same as used in other terminal operations. The Ⓢ (comma, A821C) identifies the addressing operation.

Each terminal is assigned three addresses: an individual terminal address, a group address, and an all-call address (Figure 4-6). The terminal address consists of an alphabetic character and a space. The terminal address is used for both polling and addressing, and identifies each terminal. A group address, which also consists of an alphabetic character and a space, is assigned to two or more terminals. Both terminal and group addresses are wired into the terminal (using jumpers) by the Customer Engineer. The group address, used only for addressing, allows all terminals in the addressed group to receive the computer message. The all-call address (not wired) is a slash (/)-space, and enables all terminals on the communication line to receive the computer message.

When either a group or all-call address is used, one terminal in the group is assigned the role of master (all other being slaves). For the all-call address, only one terminal on the communication line is designated master. For the group address, one terminal in each group is designated master. A master is designated by Customer-Engineer wiring (using jumpers). The all-call or group master responds to the addressing sequence by informing the multiplexer of the status of the terminal. Only the status of the master terminal is sent to the multiplexer; if a slave terminal does not have status, the terminal does not receive the message.

Figure 4-6. Station Control, Terminal Configuration

Figure 4-7. Addressing and Polling, Character Sequence

Addressing Mode Sequence

Terminal operation with station control is dependent upon the terminal mode (Figure 4-8). The terminal is first placed in text non selected mode when power comes up. In text non selected mode, only receipt of a Ⓒ can cause a mode change. The Ⓒ places the terminal in control receive mode, where the terminal can recognize a Ⓓ, Ⓢ, or any alphabetic address-character. Because an addressing sequence is being received, the next character received is the Ⓢ. The Ⓢ indicates that the terminal is being addressed (not polled) and places the terminal in control address mode. In control address mode, the terminal can recognize a Ⓒ, Ⓓ, terminal address, group address, or an all-call address. This explanation assumes that a terminal address is being received.

Terminal Address

The terminal address is recognized and places the terminal in control address selected mode. Only the terminal that is wired for the received address-character changes mode; unselected terminals remain in control address mode until either a Ⓒ or Ⓓ is received.

Transmit Status Answerback (2740-1)

The address character is followed by a space in the addressing sequence. The space character causes the terminal to go into transmit status answerback mode. In this mode the status of the terminal is

MODES	A	B	E	F
Text Non-selected	1	1	1	0
			↓	
Control-Receive	1	1	0	0
	↓			
Control-Address	0	1	0	0
				↓
Control-Address/Selected	0	1	0	1
	↓			
Transmit-Status/Answerback	1	1	0	1
	↓		↓	
Control-Selected	0	1	1	1
				↓
Receive-Text	0	1	1	0
	↓		↓	
Control-Receive	1	1	0	0

Figure 4-8. Addressing, Mode Sequence

checked and a response returns to the multiplexer in the form of a Ⓝ or Ⓨ character.

The Ⓝ indicates to the multiplexer that the terminal does not have status and that the computer message should not be sent. The alarm bell rings to notify the operator that the terminal was addressed. If a Ⓨ is sent by the terminal, status is indicated and the multiplexer can send its message.

Transmit Status Answerback (2740-2)

The address character is followed by a space in the addressing sequence. The space character causes the terminal to go into transmit status answerback mode. In this mode the status of the terminal is checked and a two-character response returns to the multiplexer in the form of a qualified Ⓝ or a qualified Ⓨ (Figure 4-7). Thus, the 2740-2 has a two-character positive or negative answerback when addressed.

The Ⓝ or Ⓨ is qualified by a sense character which is generated by an error condition stored in error latches, status condition of the terminal, or by no error condition (Figure 1-21).

Receive Text. If the qualified Ⓨ is sent by the terminal, status is indicated, and the multiplexer can send its message. The terminal is placed in control selected mode when the positive answerback is sent. In this mode the terminal waits for the first character of the message (Ⓓ). (However, the multiplexer can send a Ⓒ, in which case the terminal returns to control receive mode.) Receipt of the Ⓓ places the selected terminal into receive text mode and the unselected terminals into text non-selected mode. Should the terminal lose status during the message, the terminal is returned to text non-selected mode.

When the message is completed the multiplexer sends a Ⓒ, which informs the terminal that the message is completed and causes the terminal to go into control receive mode.

Negative Response. If the Ⓝ or qualified Ⓝ is sent to the multiplexer, it indicates that the terminal does not have status and that the computer message should not be sent. The alarm bell rings and the Attention light comes on to notify the operator that the terminal was addressed. The 2740-2 encodes and sends a sense character to inform the CPU program of the status or operator error condition which caused the terminal to be without receive status. The program should go to other business before readdressing the terminal, and if

bid or enter in communicate mode were indicated, the program should poll the terminal before read-dressing it.

After the Ⓝ has been transmitted, 'not 1st or 2nd status character answerback' allows the reset of the A and F triggers (Diagram 5-22, 3), and the terminal goes into control-address mode.

Operator action is required if the terminal is in local mode, out of paper, or the document insertion device is down. Gaining status turns off the Atten-tion light and conditions the terminal to make a positive response to the next address.

Group or All-Call Address

When a group or all-call address is received, the sequence up to control address mode is the same as for the terminal address. In control address mode, however, the group or all-call address is recognized by more than one terminal. Only the master terminal can send an answerback; all other terminals (slaves) must not send an answerback. The master of the group performs like an individual terminal address is received. All other terminals become slaves and perform differently.

While in control address mode, the status of the slave terminal is checked. If the terminal has status, the terminal goes into control address selected-slave mode; if the terminal does not have status, the terminal remains in control address mode and is inactive until either Ⓒ or Ⓓ is received, at which time the terminal goes into either text non selected or control receive mode.

Polling-Mode Sequence

As in addressing, the terminal is first placed in text non selected mode when power comes up (Figure 4-9). Receipt of the Ⓒ in the polling sequence places the terminal into control receive mode. As in addressing, a Ⓒ , Ⓓ , Ⓢ or station address character can be received in control receive mode. Because this is a polling operation, the character received is the station address character. The address character places the terminal into intermediate polling mode.

When the terminal is in intermediate polling mode, the space is received, and the Bid key has been pressed, the terminal goes into transmit text mode. A Ⓓ is returned to the multiplexer. The operator can then send the message. If the Bid key has not been pressed, the terminal goes into transmit poll answerback mode. A Ⓝ is sent to notify the multi-plexer that the terminal has no message. The ter-minal then returns to control receive mode.

When the operator finishes the message, he presses the EOT key to send a Ⓒ and return the

MODES	A	B	E	F
Text Non-selected	1	1	1	0
			↓	
Control-Receive	1	1	0	0
			↓	↓
Intermediate Polling	1	1	1	1
See note.		↓		
Transmit-Poll/Answerback	1	0	1	1
		↓		↓
Transmit-Text	1	0	1	0
		↓	↓	
Control-Receive	1	1	0	0

Note:
At this point the terminal can go to either transmit-poll/answerback (Bid key not pressed) or to transmit-text (Bid key pressed).
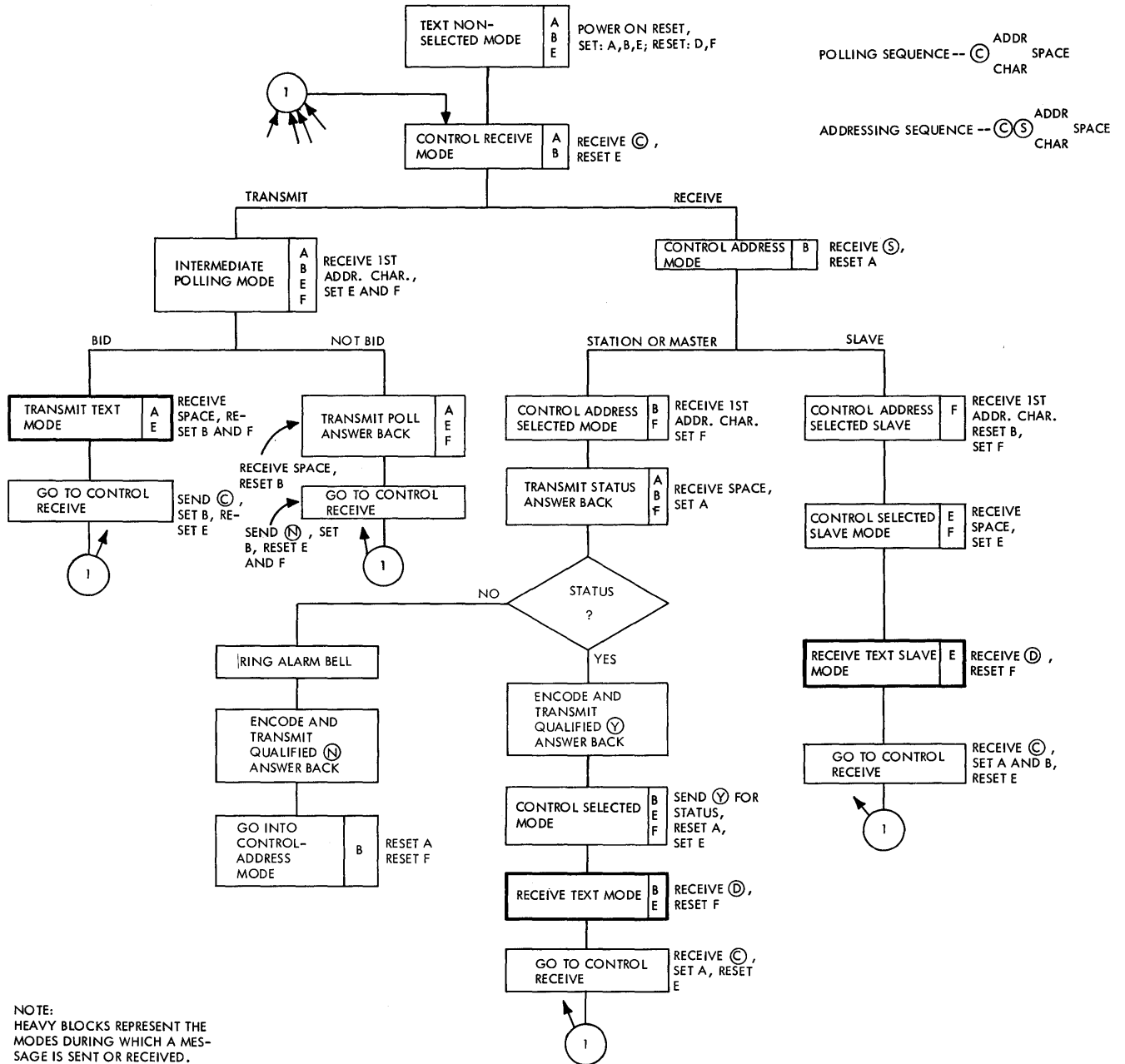
Figure 4-9. Polling, Mode Sequence

terminal to control receive mode. The terminal is now available to be polled or addressed. Figure 4-10 shows the normal mode change sequences.

FUNCTIONAL UNITS

Garble

When the terminal is first turned on, it can receive data in mid-character (garble). If this occurs, the terminal might interpret the incomplete character(s) as a valid control character. Furthemore, the terminal might achieve a status that would interfere with proper operation of the line. In order to pre-vent the unpredictable effects of garble, the terminal is prevented from responding to line data for 15 seconds after power is turned on. Within 15 seconds, the 'S0' and 'S8' relationship to the start and stop bits of the received character is correct.

When power first comes up, the 'power on reset' line turns on the two garble triggers (Diagram 4-13). The garble circuit (1) blocks the '1B set' line, and (2) prevents recognition of a character as a parity error or not S8 error (no stop bit). The output of the garble circuit, ANDed with 'not repeat' and 'not power on reset, ' starts a 15-second time delay. Fifteen seconds after the time delay is conditioned, the 'time-out 15' latch turns on. The output of the 'time-out 15' latch, ANDed with 'not C1' and 'not C2, ' turns off the 'garble 2' trigger (see Diagram 4-13). The 'garble 2' trigger turns off the 'garble 1' trigger and the 'time-out 15' latch, allowing the terminal to receive data.

TEXT NON-SELECTED MODE | A B E — POWER ON RESET, SET: A,B,E; RESET: D,F

POLLING SEQUENCE -- Ⓒ ADDR / SPACE / CHAR

CONTROL RECEIVE MODE | A B — RECEIVE Ⓒ, RESET E

ADDRESSING SEQUENCE -- ⒸⓈ ADDR / SPACE / CHAR

TRANSMIT

RECEIVE

INTERMEDIATE POLLING MODE | A B E F — RECEIVE 1ST ADDR. CHAR., SET E AND F

CONTROL ADDRESS MODE | B — RECEIVE Ⓢ, RESET A

BID

NOT BID

STATION OR MASTER

SLAVE

TRANSMIT TEXT MODE | A E — RECEIVE SPACE, RE-SET B AND F

TRANSMIT POLL ANSWER BACK | A E F

CONTROL ADDRESS SELECTED MODE | B F — RECEIVE 1ST ADDR. CHAR. SET F

CONTROL ADDRESS SELECTED SLAVE | F — RECEIVE 1ST ADDR. CHAR. RESET B, SET F

GO TO CONTROL RECEIVE — SEND Ⓒ, SET B, RE-SET E

RECEIVE SPACE, RESET B

GO TO CONTROL RECEIVE

TRANSMIT STATUS ANSWER BACK | A B F — RECEIVE SPACE, SET A

CONTROL SELECTED SLAVE MODE | E F — RECEIVE SPACE, SET E

SEND Ⓝ, SET B, RESET E AND F

①

①

STATUS ?

NO

RECEIVE TEXT SLAVE MODE | E — RECEIVE Ⓓ, RESET F

RING ALARM BELL

YES

ENCODE AND TRANSMIT QUALIFIED Ⓨ ANSWER BACK

GO TO CONTROL RECEIVE — RECEIVE Ⓒ, SET A AND B, RESET E

ENCODE AND TRANSMIT QUALIFIED Ⓝ ANSWER BACK

①

CONTROL SELECTED MODE | B E F — SEND Ⓨ FOR STATUS, RESET A, SET E

GO INTO CONTROL-ADDRESS MODE | B — RESET A RESET F

RECEIVE TEXT MODE | B E — RECEIVE Ⓓ, RESET F

GO TO CONTROL RECEIVE — RECEIVE Ⓒ, SET A, RESET E

NOTE:
HEAVY BLOCKS REPRESENT THE MODES DURING WHICH A MESSAGE IS SENT OR RECEIVED. ALL OTHERS ARE USED FOR ANSWERBACK OR LINE CONTROL.

①

TO COMPUTER

MULTIPLEXER

2740
*
**
A SPACE
G SPACE
/ SPACE

TERMINAL ADDRESS
GROUP ADDRESS
ALL-CALL ADDRESS

2740
B SPACE
G SPACE
/ SPACE

2740
*
C SPACE
H SPACE
/ SPACE

* GROUP MASTER
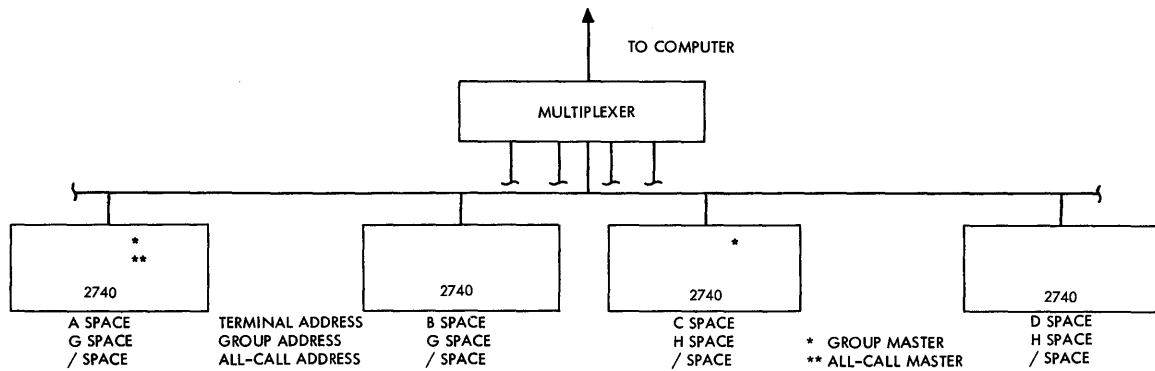** ALL-CALL MASTER

2740
D SPACE
H SPACE
/ SPACE

Figure 4-10. Normal Mode Flow

Time-Out 15

The time-out 15 circuit (see Diagram 4-13) operates the same as in transmit control. It returns the terminal to control receive mode if more than 15 seconds elapse between depressions of the I/O-device keys while in transmit text mode. For example, if 2740-2 memory "hangs up" 'send,' 'not 1B generate' 'not strobe O,' 'not operate,' 'not test (modem),' and '1B empty' condition the 15 second time delay circuit. If all of the preceding conditions exist for 15 seconds (indicating the failure to transmit a character) the 'time-out 15' latch turns on. 'Transmit text' and 'time-out 15' turn on the 'EOT' trigger, causing a Ⓒ to be generated and transmitted and the terminal to switch to control receive mode (freeing the communciation line).

If it has been enabled, time-out 15 is active for enter operations performed in communicate mode. Pressing the Enter key ('enter 1') inhibits time-out until the key is released. When the Enter key is released the first operation must be within 15 seconds and the time lapse between subsequent operations must be less than 15 seconds. 'Time-out 15' resets the terminal to not enter status if no character is keyed or function performed (tab carrier return, etc.); or if the Line Return, Line Type, or Enter key is not pressed for 15 seconds.

When power is first turned on, the timer is inactive until the terminal transmits an address answerback or a negative answerback to polling. When enter time-out does occur, the 'reset N/O' line is brought up to reset the buffer, reset the rekey latch (if set) and return the terminal to not enter status. The reset light is turned off when the 'rekey' latch is reset by enter time-out.

PRINCIPLES OF OPERATION

Addressing

- Ⓒ places the terminal into control receive mode.

- Ⓢ places the terminal into control address mode.

- Station address character places the selected terminal into control address selected mode; unselected terminals remain in control-address mode.

- Space character places the selected terminal into transmit status answerback mode.

- Ⓓ places the selected terminal into receive text mode; unselected terminals to text non selected mode.

The terminal is first placed into text non selected mode when power comes up (Diagram 5-20). The terminal waits in text non selected mode until the addressing sequence begins. When the Ⓒ is received and detected in the 1B-register, the terminal goes into control receive mode. ' Ⓒ ', 'not send,' and 'not operate' condition 'set control receive' which brings up the 'E reset gate' and 'set TNS or CR' lines (Diagram 5-21). 'Set TNS or CR' turns on the 'A' and 'B' mode triggers and turns off the 'D' and 'F' mode triggers. The terminal is now in control receive mode, awaiting reception of the Ⓢ character.

The Ⓢ is received and detected in the 1B-register, bringing up 'A reset gate' (Diagram 5-21), which places the terminal into control address mode. The reception of the Ⓢ character indicates that the operation is to be addressing and not polling. While the terminal is in control address mode, a Ⓓ, Ⓒ, terminal address, group address, or all-call address can be received.

If the all-call address (/) is received, the operation is as follows: The 'F set gate' line comes up, and the terminal goes into control address selected mode. The conditions bringing up 'F set gate' are slash character detection, '1B OK,' and control address mode. When the terminal is in control address mode, it must be determined whether it is a master or a slave. If the terminal is a master, only 'F set gate' comes up; if it is a slave with status, 'B reset gate' and 'F reset gate' both come up. Whether the terminal is a master or a slave depends upon whether the all-call master jumper is wired.

If the jumper is wired, the terminal goes into control address selected mode. If the jumper is not wired, the terminal goes into control address selected slave mode. (The difference between all-call master and slave modes is that for the master, the 'B' mode trigger is on; for the slave, it is off.)

If the group address is received, the preceding operation repeats. Again, determine whether the terminal is a slave or a master. Although different circuits are used, the master is determined the same.

If the terminal address is received, no slave or master determination is necessary; the terminal always reacts as a master. As with the group or all-call masters. 'F set gate' comes up.

While the terminal is in control address selected mode, the space character is received in the 1B-register. 'Space,' 'B,' and control address selected mode bring up 'A set gate,' putting the terminal into transmit status answerback mode. In control address selected mode, the terminal can receive a Ⓓ or Ⓒ instead of space. If a Ⓓ is received, the terminal returns to text non selected mode. If a Ⓒ is received, the terminal returns to control receive mode. If a character other than a space, Ⓓ or Ⓒ (for example, parity error) is received, the

'F reset gate' and 'B set gate' lines come up to return the terminal to control address selected mode.

Transmit-Status/Answerback (2740-1)

- Terminal with status sends a Ⓨ .

- Terminal without status sends a Ⓝ .

With the terminal in transmit status answerback mode, the individual terminal (terminal address) or the master (all-call, group address) checks its status and returns an answer to the multiplexer. If the terminal has status, a Ⓨ is loaded into the 1B-register and sent to the multiplexer. If the terminal does not have status, a Ⓝ is loaded into 1B and sent.

Transmit status answerback mode actually changes the terminal from a receiving to a sending condition. The 'send' line comes up and causes the serdes clock to run continuously as in any transmit mode. Also, if the terminal does not have status, the alarm bell rings to notify the operator that the terminal has been addressed.

If the terminal has status, the '1B generate' line is brought up by 'transmit answerback, ' 'status, ' 'B, ' and 'not D'. The control clock is started by the conditions shown on Diagram 5-22. The control clock outputs, 'C1' and 'C2, ' bring up '1B set. ' '1B set, ' '1B generate, ' and the other conditions shown on Diagram 5-22 load the Ⓨ character into the 1B-register. The character then transfers to the S-register. When 'enter serdes' and 'C1' come up, the 'end-of-state' trigger turns on. As in basic machine operation, the 'end-of-state' latch prevents the 1B-register from resetting until the Ⓨ has caused a mode change.

While Ⓨ is in the 1B-register, it is detected and 'B, ' 'not D, ' 'EOS and not O, ' and 'transmit answerback' bring up the 'E set gate'. 'Transmit answerback, ' 'EOS and not O, ' and 'B' also bring up the 'A reset gate' lines, putting the terminal into control selected mode. Reception of a Ⓨ indicates to the multiplexer that the terminal has status; the multiplexer returns a Ⓓ . The Ⓓ is detected and, with 'control selected, ' brings up 'F reset gate' to place the terminal in receive text mode (Diagram 5-21). The terminal is now conditioned to receive the computer message.

If a terminal does not have status, a hyphen (B-bit) is loaded into the 1B-register. Whether the terminal has status or not, a B-bit is always loaded into 1B (Diagram 5-22). Because the terminal does not have status, '1B generate' does not come up, thus preventing any other 1B- latch from turning on. The control clock is started and the 'C1' and

'C2' outputs bring up '1B set, ' loading the B-bit into the 1B-register. The fact that a Ⓝ and not a Ⓨ is in the 1B-register is detected. 'Not Ⓨ , ' 'B, ' 'not D, ' 'EOS and not O, ' and 'transmit answerback' bring up 'F reset gate'; 'B, ' 'EOS and not O, ' and 'transmit answerback' bring up 'A reset gate; the terminal goes into control address mode.

The terminal remains in control address mode until either a Ⓓ or Ⓒ is received. The terminal then goes to either text non selected or control receive mode.

Transmit-Status/Answerback (2740-2)

- Terminal with status sends a qualified Ⓨ .

- Terminal without status sends a qualified Ⓝ .

With the terminal in transmit status answerback mode, the individual terminal (terminal address) or the master (all-call, group address) checks its status and returns an answer to the multiplexer. If the terminal has status, a qualified Ⓨ is loaded into the 1B-register and sent to the multiplexer. If the terminal does not have status, a qualified Ⓝ is loaded into 1B and sent.

In the addressing sequence the Ⓒ is received first, the E mode trigger is reset, and the terminal goes into control receive mode. The Ⓢ is received next, A mode latch is reset, and the terminal goes into control address mode. The first address character received by the terminal sets the F mode latch for control address selected, and the space places the terminal in transmit status answerback mode.

This mode actually changes the terminal from a receiving to a sending condition. The 'send' line comes up and causes the serdes clock to run continuously as it does in any other transmit mode. Also, if the terminal does not have status, the alarm bell rings to notify the operator that the terminal has been addressed.

The 2740-2 transmits two status-answerback characters. 'Space, ' 'B, ' and 'control address selected' set the '1st status character answerback' latch. ('Not B' prevents this latch from being set for slave terminals.) 'Transmit answerback, ' 'not C2, ' '1B empty, ' 'B, ' and 'not D' bring up the C1/C2 chain necessary for '1B set. ' '1B set not EOT, ' 'transmit answerback, ' and '1st status character answerback' bring up the 'load 1st character answerback' line. The conditions determined by the error storage latches or the terminal status (Diagrams 4-5 and 5-22) are ANDed with 'load 1st character answerback' to bring up the lines required to set the first character into the 1B-register (Figure 4-11).

		1st Status Character Set In 1B-Register															
Latches and Bits		1B2 (A)		1B3 (8)			1B4 (4)		1B5 (2)		1B6 (1)			1B7 (C)		Char.	Bit Configuration
Diagram 4-5 AND Blocks		1	2	1	2	3	1	2	1	2	1	2	3	1	2		
Terminal Without Receive Status (Buffer Busy Condition)	Status Inhibit		not	not								not	not			—	———
	Bid Latch		not	not						X		not	not			2	2
	No Paper		not	X								X	X			9	1 8 C
	Insert Device Down	X														@	A
	Local				X											8	8
	Buffer Print							X								4	4
	Communicate							X				X				—	———
	Enter											X				1	1
Terminal With Receive Status	Status	X		X			X		X		X				X	—	Space
	Electronic Error	⊗		not			not		not		X				*	/	A 1 C
	I/O Error	⊗		not			not		X						*	S	A 2 C
	Receive Parity Error	⊗		not			X								*	U	A 4 C
	Trans. Parity Error	⊗		X											*	Y	A 8 C
Load 1st Character Ans. back		X	X	X	X	X	X	X	X	X	X	X	X	X	X	—	———

Note: ⊗ Any error condition through an OR block with receive status.
   * The C Bit is set because the terminal has receive status.

Figure 4-11. 1st Status Character Set in 1B-Register

The control clock is started and 'send' brings up serdes clock (Diagram 5-22) to transmit the '1st status character answerback.'

With the first character in the 1B-register, '1B full' caused the response character to be set into S-register and serialized out to the communications line. 'Transmit answerback,' 'enter serdes,' and 'C1,' set the 'EOS' latch. 'Transmit answerback,' 'EOS and not O,' 'not enter serdes,' and '1st status character answerback' bring up '1B reset' to clear the status sense character from the 1B-register. '1B reset,' 'end of state,' and '1st status character answerback' set the '2nd status character answerback' latch.

If the terminal has receive status, the no error or error condition of the previous message is defined by the 1st status character answerback which precedes the Ⓨ . If the terminal is without receive status, the "non-status" condition is defined by the sense character followed by a Ⓝ .

'Transmit answerback,' 'B,' 'not D,' 'not C2,' and '1B empty' start a second C1/C2 chain for the 2nd character. 'C1,' and '2nd status character

answerback reset the '1st status character answerback' latch and the second character response is set into 1B-register by 'not 1st status character answerback' and either 'initiate 1B1-B bit' (Ⓝ) or 'initiate 1B generate' (Ⓨ). The '2nd status character answerback' latch is reset when the Ⓝ or Ⓨ is set into the S-register.

Mode changes are allowed only by the signal, 'not 1st or 2nd status character answerback', which comes up after the 2nd character response. If the 1st response character precedes a Ⓝ ,'1st or 2nd status character answerback' inhibits 'A reset gate' and 'F reset gate' until the terminal sends the Ⓝ (Diagram 5-22). After the Ⓝ is transmitted the terminal goes to control-address mode.

After the Ⓨ is sent by a terminal with status, it goes to control-selected mode. 'Not 1st or 2nd status character answerback,' and 'EOS and not O' bring up 'end of status answerback.' 'EOS answerback,' ' Ⓨ ,' 'B,' 'transmit answerback', and 'not D' bring up 'E set gate.' 'A reset gate' is brought up the same as after a Ⓝ response.

Thus the error conditions stored, and the status

and mode of the terminal are used to set up the qualified Ⓝ or Ⓨ answerback for the CPU program. The program decodes the status sense character to determine what processing should follow. For example, the program may retransmit the previous message or poll the terminal for a message before readdressing it.

Polling

- Ⓒ places the terminal into control receive mode.

- The station address character places the selected terminal into intermediate polling mode.

- If the Bid key has been pressed, the space character places the terminal into transmit text mode and a Ⓓ is sent.

- If the Bid key has not been pressed, the space character places the terminal into transmit poll answerback mode.

- In transmit poll answerback mode, a Ⓝ returns to the multiplexer.

As in addressing, the terminal is first placed in text non selected mode when power comes up (see Diagram 5-20). The first polling-sequence character, Ⓒ, places the terminal in control receive mode (Diagram 5-23). In control receive mode the terminal can receive a Ⓒ, Ⓓ, Ⓢ, or station address character. Because this is a polling oper-

ation, a station address character is received and is recognized to place the selected terminal into intermediate polling mode.

The next polling-sequence character, space, arrives. If any character other than a space or Ⓒ is received, the terminal returns to text non-selected mode. A Ⓒ causes it to go to control-receive mode. If the operator has pressed the Bid key (indicating a desire to transmit), the space places the terminal into transmit text mode by bringing up 'F reset gate' and 'B reset gate'. Because the 'bid' trigger is on, a Ⓓ returns to the multiplexer. The Ⓓ is sent exactly as it is in the basic terminal.

If the operator has not pressed the Bid key, the space places the terminal into transmit poll answerback mode by bringing up 'B reset gate'.

Transmit Poll Answerback

Transmit poll answerback mode indicates to the terminal that the operator has not pressed the Bid key; therefore, a Ⓝ (B-bit) returns to the multiplexer. The Ⓝ is loaded into 1B when '1B set' is brought up by the control clock (Diagram 5-24). The control clock is started by 'transmit answerback,' 'not B,' '1B empty,' and 'not C2'. When 'enter serdes' comes up, the 'end-of-state' latch turns on to prevent the reset of 1B until the character has been sent. When the Ⓝ has been sent, 'not B,' 'transmit answerback,' 'not D,' and 'EOS and not O' causes the terminal to return to control receive mode.

SECTION 6. RECEIVE INTERRUPT (2741)

- While in receive mode, the terminal sends a 200 ms "space" to the multiplexer to allow the terminal to go into transmit mode before completion of the multiplexer message.

- The terminal must be connected to the multiplexer on full-duplex lines.

This feature is used only when the terminal is in the receive-text mode. If the operator wishes to stop the multiplexer from sending, he presses the Attention key to place a 200 ms "space" on the 'serial data out' line. The multiplexer senses the long space and sends a Ⓒ character back to the terminal. This places the terminal into transmit text mode and the terminal sends a Ⓓ . The operator can now send new instructions to the multiplexer.

Diagram 5-10 shows the interrupt logic. If the operator presses the Attention key while the terminal is in receive text mode, the 'interrupt' trigger turns on. 'Interrupt' and 'not power on reset' start a 200 ms single shot. The output of the single shot, ANDed with 'not A' and 'B, ' transmits the 200 ms "space" to the multiplexer. When the Attention key is released, the N/C contact makes, turning off the 'interrupt' trigger and the '1B' latch. The '1B' (inhibit interrupt) latch acts as an interlock to prevent the terminal from sending a "space" when the Attention key is pressed (to send a Ⓒ) while the terminal is in transmit text mode.

The 'halt 1' line is also an interlock. 'Halt 1' prevents the terminal from going from transmit text mode to receive control mode. The 'EOT' trigger is not allowed to turn on until the 'interrupt' trigger is reset by releasing the Attention key. Otherwise the terminal would hang up in receive control mode.

In order to use this feature, the terminal must be connected to the multiplexer on full-duplex lines. This is necessary so that the terminal can send the "space" at the same time that it is receiving data.

SECTION 7. TYPAMATIC (2741)

● Permits automatic repeating of space, under-score/dash, or backspace.

● Repeating is accomplished by circuitry.

● The transmission character is loaded into 2B.

● I/O device is synchronized with the S-register.

The typamatic feature causes the 2741 to automatically repeat I/O cycles if any of the typamatic keys are held depressed. For example, if the operator presses and holds the Space key, the I/O device continues to space until the Space key is released. If any typamatic key is pressed, but not held, a single I/O cycle occurs. In the standard SELECTRIC® repeating is made possible by mechanical changes to the SELECTRIC. For the I/O SELECTRIC, however, repeating is accomplished by circuitry. Circuits must be used because the unrestricted speed of the I/O device can overrun the terminal logic. Therefore, the I/O device must by synchronized with the operation of the S-register.

During a sending operation, the character that is set up in the I/O transmit contacts is loaded into the 1B-register. From the 1B-register the character is loaded into the S-register and sent. With the Typamatic feature installed, the character is also loaded into the 2B-register (Figure 4-12). The character in 2B, however, does not print until the 'print-out' line comes up. During a sending operation, the 'print-out' line can come up only when the operator presses and holds a typamatic key.
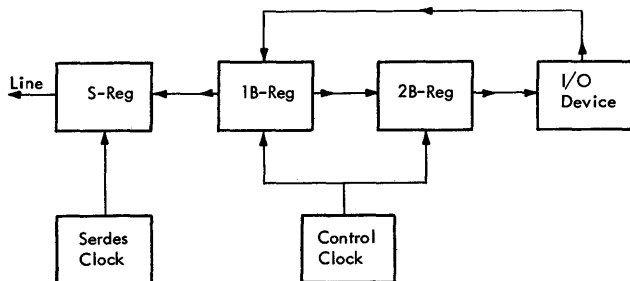
Figure 4-12. Typematic Data Flow

The character in 1B is loaded into 2B at the same time as the character is loaded into the S-register. '2B set' is brought up by the conditions shown on Diagram 5-11. The principle condition is 'enter serdes, ' which is also the principle condition to load the S-register.

In addition to the normal set of contacts, the typamatic keys have another set of contacts for typamatic operation (the Underscore/Dash and Backspace keys share the same set of typamatic contacts). For the typamatic operation to begin, the key must be held at least 100 ms. The 100 ms delay, in addition to ensuring that the key has been held and not just pressed, ensures that any character in 2B has had time to reset.

When a typamatic key is pressed and held, the 100 ms delay times out and, with 'not I/O cycle' and '2B full, ' turns on the 'type' trigger (Diagram 5-11). The 'type' trigger does three things: (1) frees the printout circuit, (2) disables the 2B-overflow reset circuit, and (3) brings up 'incorrect case' to prevent any shift during the typamatic operation.

The character is printed normally the first time. As soon as the operation is completed (indicated by 'not I/O cycle'), the 'type' trigger turns on and the 'print-out' line comes up, transferring the character in 2B to the I/O magnets, just as in a receiving operation. The cycle repeats as long as the 'type' trigger is on. When the typamatic key is released and the last character is transferred out of 2B, the 'type' trigger turns off.

The Typamatic feature also causes one other change in basic 2741 logic. In addition to the normal 2B-reset conditions, the 'TOM (typamatic) 2B reset' trigger is added (Diagram 5-11). The 'TOM 2B reset' trigger causes the 2B-register to reset during the following times:

1. When the Attention key is pressed during a sending operation (transmit EOT).
2. When the terminal is in control receive mode.
3. When the terminal is placed into local (off-line) while sending.
4. When the Carrier-Return key is pressed (causing an automatic EOT) during a sending operation.

SECTION 8. BUFFER EXPANSION (2740-2)

- Increases buffer capacity from 128 to 256 or 448 characters.

- See "Buffer Address Register" in Functional Units chapter.

SECTION 9. BUFFERED RECEIVE (2740-2)

- 600 bps Speed Base feature is required.

- Characters received from the communication line are stored in buffer storage.

- There is no printing while receiving from the line.

- 'Parity error or not S8' rings the bell and turns on 'error' while receiving. A "-" stores in place of the error character.

- No incorrect case error detection while receiving.

- The message is not printed if an error is received.

The Buffered Receive feature adds circuits to inhibit printing and enable storing during receive text and provides for three additional buffer address resets: (1) at the beginning of receive text, (2) when © does not follow a received message, and (3) at the end of on-line buffer print starts only when © is received.

Buffered receive from the 2B-register into buffer storage is described in this section (Refer to "Receive" in Chapter 3 for the receive operation from the communication line to the 2B-register.) Section 3, "Buffer Print," describes the transition from buffered receive to buffer print.

Store Received Characters (Diagram 5-38)

- Buffered receive is similar to enter.

- 'Receive text buffer' is the main control line.

- Functions of 'receive text buffer':

  a. Inhibit printout from 2B
  b. Gate 'memory go' line
  c. Gate 2B to 'memory buffer' trigger
  d. Inhibit incorrect case error.
  e. Gate 'buffer 2B reset' trigger

- Characters received in receive text mode except Ⓑ are stored.

- Parity checked in store circuits and by VRC circuits.

Buffered receive differs from receive text after the received character enters the 2B-register. The '2B full' line, which normally causes an I/O cycle by gating the decoded contents of 2B to the printer magnets, raises the 'memory go' line instead (Diagram 5-38). 'Inhibit print out' prevents the I/O cycle. The buffer storage address resets during the mode change to receive text so the first character cycle stores the first received character at the first buffer storage character address.

The 'memory go' line starts buffer storage timing by stepping the bit counter to zero and advancing the character address to 1. Buffer address time 0' gates the B-bit from '2B1' to the 'memory buffer' trigger. The read time of 'buffer address time 0' clears the first core at character address 1; a binary one in 'memory buffer' sets a 1 in the core during write time (Diagram 4-18). The 'memory buffer' trigger resets at 'CC2' when write current stops. The other six character bits follow.

The 'buffer 2B reset' trigger turns on at 'buffer address time 7' and 2B resets; the '2B full' line drops and 'memory go' goes down (Diagram 5-38). The buffer storage character cycle ends in 'buffer address time 7' and memory circuits wait for receive circuits to set another character into 2B.

There is little chance that the 2B overflow reset will ever function with the Buffered Receive feature installed.

Receive Text Buffer to Buffer Print

- Buffered Receive stores only characters received in receive text mode.

- Ⓑ is not stored; © is stored.

- © Starts buffer print (refer to "Buffer Print" in Chapter 3.)

When the 2740-2 acknowledges the received message with Ⓝ during transmit check answerback, the central processor does not respond with © . Instead, the central processor immediately begins to retransmit the message. The 2740-2 changes modes to receive text and, because the 'reset buffer address' trigger is on, resets the buffer address. 'Receive text buffer' again causes the storing of received characters in buffer storage, starting at character address 1.

SECTION 10. HEADER CONTROL (2740-2)

- Allows repetitive header information to be transmitted at the beginning of each message.

- Predetermined number of positions (28 maximum) wired to customers requirements.

- Buffer address register reset to zero in transmit text mode.

- Buffer address register reset to wired value in all other operations.

- Normal operation with Header switch off.

The terminal operator may wish to transmit the same information at the beginning of each message. When the Header Control feature is used, it is necessary to key in desired data only once. Information changes in this area must be made by rekeying the entire header. Once the header has been keyed, switch control allows the buffer to automatically start at the end of the header area for subsequent keying. Transmissions include the data in the header area. All positions of the header must be filled with characters and/or spaces. If the terminal power is turned off, the buffer information is destroyed.

The customer determines the fixed number of positions to be reserved at the beginning of buffer for header information. The machine is wired accordingly, with a maximum of 28 (groups of 4). This is done by using 6 jumper positions, three of which control the set of 'buffer address' triggers 6, 7, and 8 (binary values of 4, 8, and 16 respectively).

The three other positions are used to wire the 'not buffer address' lines and redefine 'buffer address empty' (Diagram 5-45). The 'buffer address empty' must be satisfied for information to be entered. During a header control operation the buffer address is not zero when the first character is entered. Therefore, the proper 'not buffer address' jumper positions are wired for the 'buffer address empty' to be satisfied with the desired header address set in the address register.

The 'header storage buffer address set' trigger is turned on by 'reset buffer address' if the Header switch is on and the terminal is not in transmit text mode. During any enter operation, other than transmit, this trigger causes the address of the first non-header character to be set in the buffer address register. With the switch off 'not header N/O 1' holds the trigger off for normal terminal operation and keyed data may be entered into the header area of the buffer and read back for verification. Turning the switch on prevents entering characters into the header area. 'Transmit text' resets the 'header storage buffer address set' trigger and allows the address to reset to zero for transmission of all data.

SECTION 11. DOCUMENT INSERTION (2740-2)

● Provides automatic mechanical actions.

● Status is down from beginning to end of document insertion.

The four mechanical functions involved in the I/O printer document insertion are as follows:

1. Document guide is opened manually to guide the insertion of a ledger card from the front of the platen.
2. Feedrolls that are lowered automatically.
3. Document guide is manually closed to process document.
4. Feedrolls that are raised automatically.

In the I/O printer, a mechanical feedroll latch identifies the feedroll positions. A feedroll cam drives the feedrolls up or down. The positions of the document guide and feedroll latch control 'insert card' and 'latch in' lines to generate associated document insertion functions (Diagram 5-46).

When the document guide is opened, 'insert card' comes up. This turns on 'drive down' because the feedrolls are still up and 'latch in' is up. 'Drive down' starts the I/O motor, drops status, locks the keyboard, and energizes the cycle magnet. 'Insert card' and 'not drive up' energize the feedroll latch magnet. The feedroll cam rotates and the mechanical latch comes out--the feedrolls are lowered. With the mechanical latch out 'drive down' turns off. After the card is inserted and aligned, the guide is closed. 'Drive up' is turned on with not 'insert card' and not 'latch in'. The cycle magnet is energized again to raise the feedrolls. 'Latch in' comes up when the feedrolls are up and turns off 'drive up'.

'Drive up,' 'drive down,' and 'insert card' overlap so that at least one of them at all times is up during document insertion. These lines are ORed to hold status down, keep the keyboard locked, and cause the I/O motor to run during the entire operation.

SECTION 12. SPLIT PLATEN (2740-2)

● Provides a two-section platen on the I/O printer.

The Split Platen is a two-section platen that facilitates dual-document printing. It allows independent line-spacing of the right-hand document, controlled by the central processor. The left knob is pulled out to split the platen, and pushed in to re-join it. The right knob operates the conventional platen vernier.

The mechanical operation of the Split Platen feature is explained in Appendix D. The 'split platen' latch (Diagram 5-46) turns on when the left hand platen knob is pulled out. The latch turns on the Split Platen light and locks the keyboard. The terminal returns to normal when the platen is rejoined by pushing in the left hand platen knob.

SECTION 13. TELEGRAPH (2740-2)

● Enables the 2740-2 to be used over telegraph
  systems.

The Telegraph feature requires two changes to
normal 2740-2 circuits: (1) the serdes oscillator
frequency is reduced to 300 Hz to match the 75 bps
line, and (2) a special telegraph line adapter is
used (Diagram 5-47, Sheet 5).

The telegraph line adapter consists of two relays:
receive and transmit. The receive relay coil is
connected in series with the transmit relay N/C con-
tacts, across the telegraph line. The telegraph line
adapter operates on a current loop line. Current
flowing indicates a mark level (or bit); no current
flowing indicates a space level (or no bit).

The receive relay monitors the line, and is
picked when current is flowing. This causes the
receive relay N/C contacts to open and a bit is
indicated to the terminal logic. The normal con-
dition of the telegraph line (no data being sent or
received) is current flowing.

When the terminal is sending data, the transmit
relay coil follows the inverted condition of the
'Serial Data Out' line, that is, a bit does not pick
the relay but a no-bit does. Picking the relay
causes the N/C contacts to transfer, putting a no-bit
on the line; not picking the relay allows current to
flow and a bit is put on the line.

> NOTE: The removal of the relay will open the current loop to
> all terminals on that line. A manual shunt switch, installed
> on the adapter, will provide an alternate current path, when
> operated. This switch must be operated to 'shunt' anytime
> the relay is to be removed.

SECTION 14. SPEED BASE--600 BPS (2740-2)

● Allows transmission and reception of data at
  600 bps.

● One oscillator is used for both the serdes and
  control clocks.

● Frequency to the serdes clock is reduced by a
  high speed frequency divider circuit.

The Speed Base feature increases the transmission
and receiving speed of the 2740-2 terminal. This
enables increased throughput for the system and
reduces the time that each terminal ties up the
communication line. This feature requires three
changes: (1) the frequency of the serdes and control
clocks is changed,(2) a higher speed line adapter is
used, and (3) buffer receive must be installed.

A single oscillator, running at 9.6 KHz, is used for
both the serdes and control clocks. The output of this
oscillator is fed directly to the control clock, and while
it is slower than normal oscillator frequency, it is
still fast enough to operate the terminal logic. The
output of the oscillator is not fed directly to the serdes
clock. A frequency reduction network is inserted
between the oscillator output and the serdes driving
pulse ('SDMV')--dotted area on Diagram 4-2. This
network reduces the oscillator frequency by four to
2.4 KHz, allowing 600 bps operation.

IBM Limited Distance Type 2, an IBM Leased Line,
or a Western Electric 202D (or equivalent) data set
is used for attachment to the communication line. The
interface is shown in Diagram 5-47, Sheet 5.

SECTION 15.   EDIT (2740-2)

- Line Type key causes a single print line to type out.

- Line Return key causes the memory address to go back to the beginning of a print line to be erased from memory.

- Enable enter time out is effective only after an address answerback or a negative answerback to polling.

The Edit feature allows the terminal operator to verify and correct message data before it is transmitted. By pressing the Line Type key, the operator can initiate a line-by-line printout of the message entered. If an error is discovered following an enter or line type operation, memory can be backed up to the previous carrier return by pressing the Line Return key. The error can then be corrected by retyping the error line. If line return is used during the line type operation all subsequent lines of the message must also be retyped. After the operator is sure the message is correct, the Bid key is pressed and the message is transmitted when the terminal is polled. The Edit featu.. is operable in the local or communicate mode.

Once enabled, a 15-second timeout is effective for enter operations in communicate mode. Therefore, if the Edit feature is to be used, the timeout must be considered and the operator must perform an operation within 15 seconds. A character must be typed, function performed, or the Line Type or Line Return key pressed to prevent a terminal reset to not enter status. Holding the Line Type key or Line Return key depressed inhibits the timer from timing out. If the operator wishes to inhibit the enter time-out (while talking, etc.) she should hold the Line Type key pressed if the Edit feature is installed. Pressing the Enter key inhibits the time out, but it also resets the buffer.

When the terminal is initially powered on, the timer is inactive until the terminal transmits an address answerback or negative answerback to polling. The buffer address is reset, 'rekey' latch reset (if set), and 'enter' trigger reset by a time-out condition. The reset light is turned off when the 'rekey' latch is reset by the timer.

LINE TYPE

- Stores stop code and resets buffer starting position by pressing Enter key while in enter mode.

- Pressing Line Type key causes the buffer to read out and print until a carrier return character is reached.

- '2B upper case' keeps track of the shift of printed characters.

The line type operation is performed as follows: the operator initially presses the Enter key and types a message. Press Enter key again. This stores the stop code, resets the buffer to the starting position and sets up the line type circuits.

Pressing the Line Type key causes circuits to print a line of characters and to search for a carrier-return or a stop code. When either is reached, the operation ends. Another depression of the Line Type key causes another search (assuming a carrier return and not a stop code ended the previous operation). When the stop code is reached, the enter trigger is turned on and further depressions of the Line Type key have no effect. The Bid key can be pressed following any line type operation, and the message, as printed, up to that point is transmitted.

Refer to Diagrams 5-39 and 5-40 for the following. With the terminal in enter mode, pressing the Enter key causes the 'reset buffer' trigger to turn on. 'Reset buffer' initiates a check of the I/O printer shift. If the I/O printer is in upper case, it shifts to lowercase. The 'strobe' signal is inhibited, however, so the lowercase character is not stored. 'Reset buffer' also turns off the '2B upper case' latch to ensure that the I/O printer and the terminal are synchronized. The 'store stop code' trigger turns on causing a stop code to load in the next position of memory. 'Reset buffer' and '2B full' (the stop code in 2B) turn off the 'line type inhibit' latch to allow the line type operation to be performed. Upon completion of the shift (if one was required), 'reset buffer address' turns on causing the buffer to reset to the starting position. The terminal is now prepared to do a line type operation.

Pressing the Line Type key turns on the 'line type' trigger. 'Line type' causes the 'buffer print' trigger to turn on and then the 'enter' trigger to turn off. 'Buffer print' and '2B empty' bring up 'memory go', causing a character to read out of memory and load into the 2B-register. While in the 2B-register, the character is examined to see if it is an uppercase shift, lowercase shift, carrier return, or a stop code character. If none of these, the character is printed. If the character is an uppercase character, the '2B upper case' latch turns on and the I/O shifts to uppercase.. If the character is a lowercase character, the '2B upper case' latch turns off and the I/O shifts to lowercase. '2B upper case' keeps track of the shift of the characters as they are

printed. After the character is reset from the 2B-register the next character is read out of memory.

Detect Carrier Return

The preceding operation is repeated until a carrier return or stop code character is detected in the 2B-register. If the CR character is reached the 'edit control 3' trigger turns on. The carrier return occurs. 'Edit control 3' then turns off the 'buffer print' trigger. If the I/O is in uppercase, it shifts to lower case. When the I/O is in LC, the 'enter' trigger turns on. 'Enter' and 'edit control 3' then turn off the 'line type' trigger, following which, 'edit control 3' turns off. The circuits are still set up for line type, and pressing the Line Type key will cause printing until another carrier return is detected.

Detect Stop Code

When the stop code character is reached, the 'edit control 3' trigger turns on. 'Edit control 3' and 'stop code' then turns on the 'line type inhibit' latch. Because a stop code was detected, back up the buffer one position for the next entered character to store in place of the stop code. The stop code, however, remains in storage until another character is entered. 'Stop code', 'line type' and 'bfr. adr. time 7' turn on the 'reverse count sequence' trigger which causes the memory to backup one position. Following the backup of memory, (1) the 'buffer print' trigger turns off, (2) the I/O shifts to lower case (if in upper case), and (3) the 'enter' trigger turns on. The 'line type' trigger then turns off and one "CC" pulse later, 'edit control 3' turns off.

At the end of any line type operation, the Bid key can be pressed. If the terminal is in communicate mode, the information printed out up to that point is transmitted. If the terminal is in local mode, the information is printed. To meet the conventions of terminal operation, insert a lowercase shift character prior to the stop code if the preceding information is in uppercase. If the last printed character was in uppercase, the '2B upper case' latch will be on. Depression of the Bid key causes the 'store stop code' trigger to turn on. 'Store stop code' and '2B upper case turn on the 'store lowercase code' latch, which brings up 'edit 3'.

'Edit 3' causes the following:

1. The lowercase character loads directly into the 'memory buffer' trigger.
2. The 'memory buffer gate' is blocked so that the stop code sitting in 2B can not yet be stored.
3. The buffer parity circuit is blocked.

When storing of the lowercase character is completed, the stop code, held in the 2B-register is stored. The '2B uppercase' latch is reset followed by 'store lowercase code'. The buffer resets to the starting position and normal buffer print or transmit operation can begin.

LINE RETURN

● Buffer initially backs up one address position and goes forward one position to read out the character.

● Following the initial back up, buffer backs up two address positions and forward one position to readout.

● Back up ends when a carrier return is detected or beginning of memory is reached.

Following an enter or line type operation, memory can be backed up to the previous carrier return by pressing the Line Return key. Subsequent depressions of the Line Return key cause memory to back up one line at a time, until the beginning of memory is reached. The buffer address is initially stepped back one position and then read forward so the character can be examined to determine if it is an uppercase or lowercase shift character. The first character read out (last character of print line could be a carrier return; if so, detection is prevented by the 'reverse count once' latch.) The character is read out to be examined. The buffer is then backed up two positions and a character read out. Again the character is examined. This process continues, back up two and read out one, until a carrier return is detected. Information can then be entered to correct any errors. Figure 4-13 shows the sequence of buffer operation for line return.

Operation

If the 'line return enable' latch is set, pressing the Line Return key turns on the 'line return' trigger which then turns on the 'line type or line return' latch (Diagram 5-43). If the I/O is in uppercase, it shifts to lowercase. The strobe pulse from the I/O is inhibited, however, so the shift character is not stored.

Before the 'line return' trigger turned on, both 'edit control 1' and 'edit control 2' were held off. When the 'line return' trigger turns on, 'edit control 1' turns on at the next 'CC1' pulse. 'Edit control 1' causes the 'reverse count sequence' trigger to turn on and, with the 'reverse count once' latch off, turns on the 'edit control 2' latch. The 'reverse count
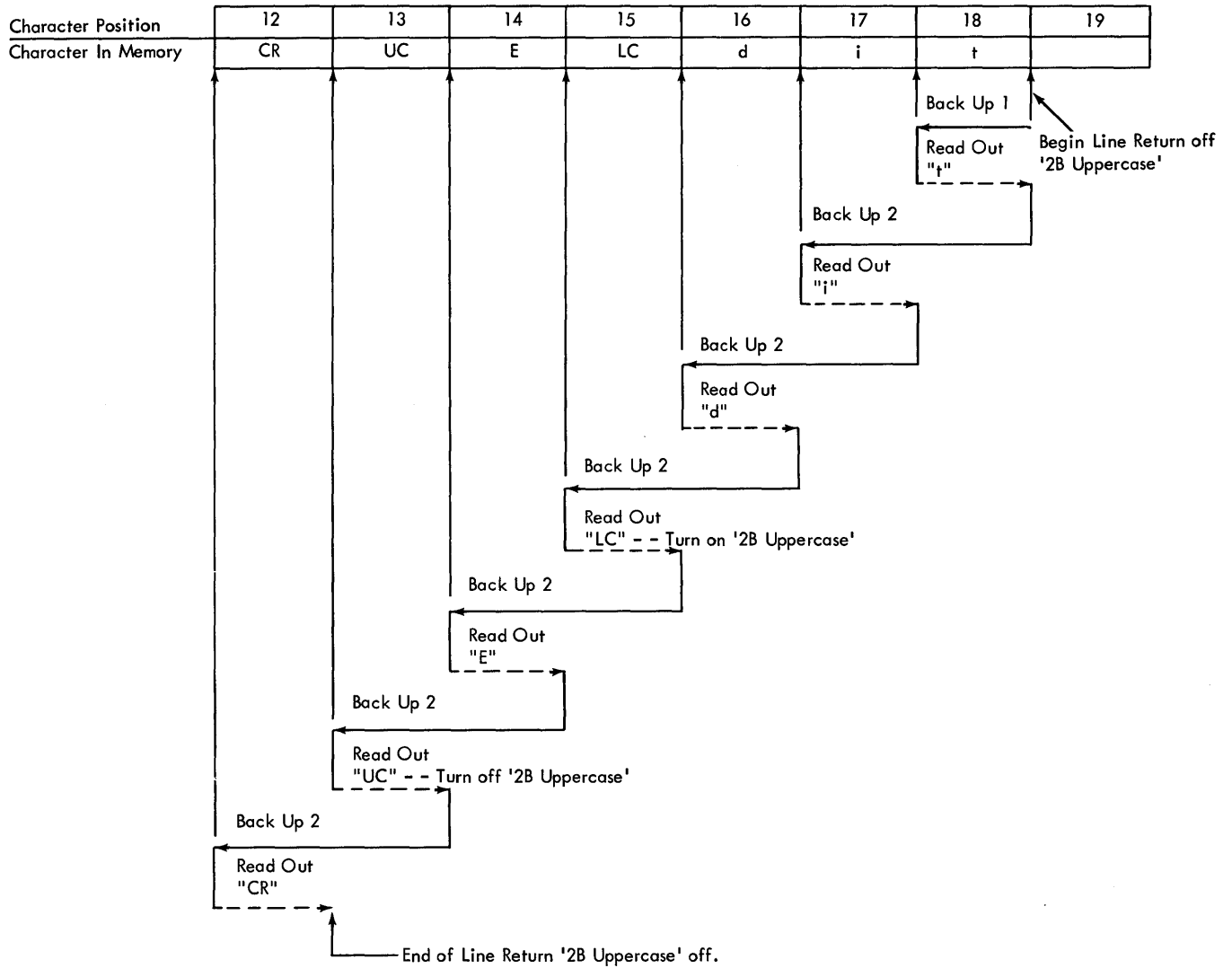
Character Position	12	13	14	15	16	17	18	19
Character In Memory	CR	UC	E	LC	d	i	t	

Back Up 1

Read Out "t" --- Begin Line Return off '2B Uppercase'

Back Up 2

Read Out "i"

Back Up 2

Read Out "d"

Back Up 2

Read Out "LC" -- Turn on '2B Uppercase'

Back Up 2

Read Out "E"

Back Up 2

Read Out "UC" -- Turn off '2B Uppercase'

Back Up 2

Read Out "CR"

End of Line Return '2B Uppercase' off.

Figure 4-13. Line Return Buffer Operation

once' latch off, allows buffer to back up only one address for the first character to be read out. 'Line type or line return,' 'lower case 1,' and 'not edit control 1' (with other conditions) turns on the 'buffer print' trigger. 'Buffer print'(main condition) then turns off the 'enter'trigger. 'Buffer print' and '2B empty' bring up 'memory go' and a character is read out of memory and loaded into the 2B-register. The character is examined and if the character is:

1. An uppercase shift, the '2B upper case' latch turns off;
2. A lower case shift, the '2B upper case' latch turns on;
3. A carrier return, the operation is not ended--recognition of the character is prevented (explained later).

Following read out of the first character, allow buffer to back up two address positions so the character just read will be skipped and the next character addressed to be read. The 'reverse count once' latch is turned on and further operations of 'edit control 2' and 'edit control 1' result in a back up of two positions.

Back Up Control

The back up operation is as follows: When the character from storage is in the 2B-register, the 'buffer 2B reset' trigger turns on. This causes the character to reset from 2B and the 'edit control 2' trigger to turn off. The first 'CC1' pulse following the turn off of 'edit control 2' turns on 'edit control 1'. The next 'CC2' pulse turns on 'reverse count sequence'.

'Reverse count sequence', 'not buffer address empty', and the next 'CC1' pulse turn on 'reverse count sequence control', which supplies the buffer back up pulse (Diagram 4-16). As long as 'edit control 1' is on, pulses to back up the buffer are generated . For the initial back up 'reverse count once' and 'edit control 1' on turn on 'edit control 2', allowing only one back up pulse. For all back ups after this, another circuit turns on 'edit control 2'. The sequence for backing up two positions differs in one way: the turn on of 'edit control 2' is delayed enough to allow another back up pulse to occur. During the back up operations, 'edit

control 1' on 'not edit control 2' block 'memory go' preventing the read out of a character. The details of this operation are shown on the timing chart (Diagram 5-44).

Detect Carrier Return

When a carrier return is read out of memory and loaded into 2B, it is detected and turns on the 'edit control 3' trigger. If this is the first character read out of memory, 'edit control 3' is prevented from turning on by '2B6 or rev ct once'.

SECTION 16. 2760 ATTACHMENT FEATURE

INTRODUCTION

- The 2760 attachment feature provides the necessary interface and control signals between the 2740-1 and the 2760.

- The feature allows the attached 2760 to use the control circuitry of the 2740-1.

- The 2760 is an I/O device attached to an IBM 2740-1, serial number 15000 or higher.

- Certain features cannot be installed on an IBM 2740-1 if the 2760 attachment feature is used.

The 2760 attachment feature allows one IBM 2760 Optical Image Unit to be attached to an IBM 2740-1. The 2760 utilizes the control circuitry of the 2740-1 to transmit data to, and receive data from, a central processing unit, via a multiplexer. When the 2760 is attached, the 2740-1 is always in terminal-to-multiplexer mode of operation. The 2760 can be placed on a customer-provided desk or table located at a distance of up to 8 feet from the 2740-1. All signals between the 2740-1 and the 2760 are at dc levels. The ac power required by the 2760 is provided by a cable from the 2740-1.

IBM 2740-1 Communication Terminal, Serial 15000 or Higher, with Record Checking

The IBM 2760 Optical Image Unit is an I/O device used with an IBM 2740-1 Communication Terminal. Basically, it is a data entry device that operates on-line, in conversational mode, with a programmed computer system. Only one 2760 can be attached to each 2740-1, and in order for this to be done, the 2740-1 must have serial number 15000 or higher and must already have the record-checking feature installed.

Special Features

The IBM 2760 Optical Image Unit attachment will operate with any of the following special features installed on the 2740 terminal:

Record Checking (prerequisite)
Auto EOB
Auto Disconnect (World Trade only)
Dial-Up Adapter
IBM Line Adapters
IBM Modems

The station control and transmit control special features cannot be installed on the 2740 terminal if the 2760 attachment is used.

IBM 2760 OPTICAL IMAGE UNIT

- An operator-oriented component used to communicate with a remote central processing unit via the IBM 2740-1.

- Interlocking allows alternate operation of the 2760 and the I/O Selectric without interference.

- Screen and probe used for on-line data selection and transmission in conversational mode.

- Data is represented on an overlay and an image projected on the screen.

- Response points are defined by coordinates and represent specific data in each program.

- Projected information is stored on a 16mm filmstrip contained in a cartridge.

- Film movement is under computer program control.

- Manual Frame Advance allows film movement by the operator also.

- An Image Index Counter permits the central processing unit to check film movement accuracy.

The IBM 2760 Optical Image Unit (Figure 4-14) is an input/output, operator-oriented component used with an IBM 2740 Communication Terminal, Model 1. Only one IBM 2760 is attachable to each IBM 2740-1. The operator need not have any keyboard skill or any knowledge of programming. Card punching and
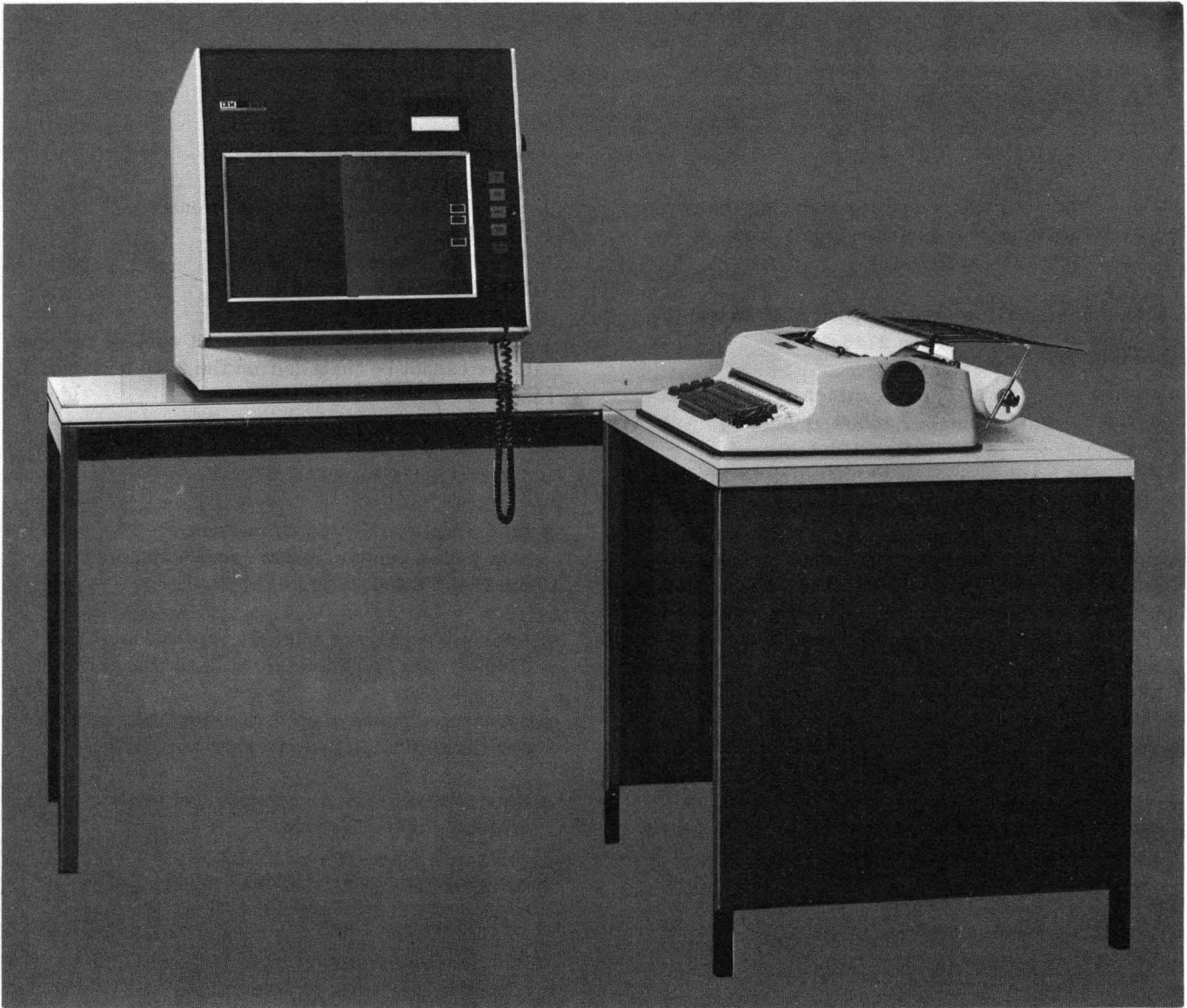
Figure 4-14. IBM 2760 Optical Image Unit Attached to IBM 2740-1 Communication Terminal

processing are also eliminated. The user has the capability of communicating directly with a remotely located computer by using illustrations or any combination of numbers, letters, words, phrases, and sentences in his own language. The lack of computer or program knowledge has no effect upon the proficiency of an Optical Image Unit operator as he selects items or operations properly displayed in words, numbers, and/or pictures.

Interlocking

The 2760 input occurs when the operator presses the spring-loaded tip of the RF probe on one of the 243 response points. Three of these are utility

response points (labeled, as shown in Figure 4-15), and the other 240 points are for data entry. The 2740-1 keyboard is also used for data entry, but any given input message must come from only one of the two sources. These two I/O units share the 2740-1 terminal control unit and they cannot operate simultaneously.

The sequence of the alternate operations is planned by the system designer and placed under control of the CPU program. While either unit is operating, the other unit is interlocked to assure completion of the operation in process. The control unit must be released before subsequent operations can be initiated.

Figure 4-15. Probe, Screen, and Operator's Console

Response Point Coordinates

The vertical (V) and horizontal (H) coordinates are given character assignments for transmission and application program definition purposes. These coordinates are stored in V (vertical) and H (horizontal) registers until transmitted.

Figure 4-16 shows the V and H coordinates assigned to each of the 240 possible data response points on the entire screen (the projection screen plus the auxiliary screen). The V coordinate is transmitted first over the communications line.

Filmstrip Motion Control

Images are stored on 16-millimeter filmstrips, in individual plastic cartridges which are manually loaded by the operator as required by the application.

The Optical Image Unit handles only one cartridge at a time, selecting and displaying images under processor control.

The application program for a given filmstrip is called into computer storage when the filmstrip is identified by the operator's (title) frame of the filmstrip. Subsequent images are selected and displayed in a sequence specified by the application program for given operator responses. Each filmstrip may contain up to 128 images.

Film movement is under computer program control, and the 2760 is equipped with an electronic Image Index Counter that permits the stored program to check the accuracy of film movement.

The CPU program has the capability of allowing the operator to manually move film, one frame at a time. The Image Index Counter still maintains image count information for the CPU program.

Horizontal Positions

(V)	1	2	3	4	5	6	7	8	9	10		11	12	13	14	15	16	17	18	19	20	21	
L	l5	ld	lm	lu	l4	lc	ll	lt	l3	lb	1	lk	ls	l2	la	lj	l/	ll	l&	l-	l@		
T	t5	td	tm	tu	t4	tc	tl	tt	t3	tb	2	tk	ts	t2	ta	tj	t/	tl	t&	t-	t@		
3	35	3d	3m	3u	34	3c	3l	3t	33	3b	3	3k	3s	32	3a	3j	3/	31	3&	3-	3@		
B	b5	bd	bm	bu	b4	bc	bl	bt	b3	bb	4	bk	bs	b2	ba	bj	b/	bl	b&	b-	b@		
K	k5	kd	km	ku	k4	kc	kl	kt	k3	kb	5	kk	ks	k2	ka	kj	k/	kl	k&	k-	k@	k space	UNLOAD
S	s5	sd	sm	su	s4	sc	sl	st	s3	sb	6	sk	ss	s2	sa	sj	s/	sl	s&	s-	s@	s space	LOAD
2	25	2d	2m	2u	24	2c	2l	2t	23	2b	7	2k	2s	22	2a	2j	2/	21	2&	2-	2@		
A	a5	ad	am	au	a4	ac	al	at	a3	ab	8	ak	as	a2	aa	aj	a/	al	a&	a-	a@	a space	END ENTRY
J	j5	jd	jm	ju	j4	jc	jl	jt	j3	jb	9	jk	js	j2	ja	jj	j/	jl	j&	j-	j@		
/	/5	/d	/m	/u	/4	/c	/l	/t	/3	/b	10	/k	/s	/2	/a	/j	//	/l	/&	/-	/@		
1	15	1d	1m	1u	14	1c	1l	1t	13	1b	11	1k	1s	12	1a	1j	1/	11	1&	1-	1@		
&	&5	&d	&m	&u	&4	&c	&l	&t	&3	&b	12	&k	&s	&2	&a	&j	&/	&l	&&	&-	&@		
(H)	5	D	M	U	4	C	L	T	3	B		K	S	2	A	J	/	1	&	-	@		

(V) Vertical Coordinates* Auxiliary Screen Vertical Positions Image Screen (H) Horizontal Coordinates*

* Shown in upper case for ease of reading. The 2760 operates in lower case shift automatically. No case shift characters are required or permitted in messages to or from the unit.

Figure 4-16. Vertical (V) and Horizontal (H) Response Points

Image Index Counter

The Image Index Counter is standard on the IBM 2760. It is a two-position electronic counter used, together with the CPU program routine, to ensure the accuracy of film movement. This counter, located inside the 2760 and controlled by feedback impulses from the film drive motor, increments or decrements in step with the movement of the filmstrip. Therefore, the Image Index Counter contains a continuous record of the image being viewed by the operator. The counter is provided with read-out circuitry to transmit its contents to the CPU. This read-out occurs at the beginning of every message from the 2760 to the CPU.

The Image Index Counter read-out characters are designated I_1 and I_2 and are always the first two characters following a PRE (prefix), o (alphabetic o) sequence in the message transmitted from the 2760 to the CPU. Figure 4-17 shows the various characters used to represent the numerical contents of the counter.

If the 2760 receives instructions from the CPU to move the filmstrip beyond its last frame, an "interlock" is activated to stop film movement. This, in turn, prevents any further operation of the counter, thereby providing a method of indicating improper operation to the CPU. (A subsequent move reverse will deactivate the "interlock" and activate the Image Index Counter.)

MESSAGE FORMAT

● Messages received from the CPU contain filmstrip motion instructions for the 2760.

● The Function Control (F) character in the received message sets manual or automatic EOM mode in the 2760.

● The F (Function Control) character enables or disables the Manual Frame Advance switch.

● Transmission of a message is initiated by a probe operation.

● The probe point data is defined for the CPU by the V and H coordinate characters transmitted in the message.

Frames of Film Movement		Film Control Character Transmitted	Image Position Count In Image Index Counter	
A-1 in V Reg.	A-2 in H Reg.		I-1	I-2
0	0	(Space)	0	0
32	1	@	32	1
64	2	–	64	2
96	3	&	96	3
128	4	1	128	4
160	5	/	160	5
192	6	J	192	6
224	7	A	224	7
256	8	2	256	8
288	9	S	288	9
320	10	K	320	10
352	11	B	352	11
384	12	3	384	12
416	13	T	416	13
448	14	L	448	14
480	15	C	480	15
——	16	4	——	16
——	17	U	——	17
——	18	M	——	18
——	19	D	——	19
——	20	5	——	20
——	21	V	——	21
——	22	N	——	22
——	23	E	——	23
——	24	6	——	24
——	25	W	——	25
——	26	O	——	26
——	27	F	——	27
——	28	Z	——	28
——	29	X	——	29
——	30	P	——	30
——	31	G	——	31
Bit Configuration and Value In Counter and Registers				
A2,I2		16	8	4	2	1
A1,I1			256	128	64	32
BCD	8	4	2	1	B	A

● Figure 4-17. Decimal Values of Character Transmitted for Film Control

Receive Format

The message format for the CPU to the 2760 is: Ⓓ , PRE, o, F A_1, A_2, Ⓑ , LRC, and the format to the 2740-1 is Ⓓ , (text), Ⓑ , LRC; PRE, o, F, A_1, A_2 form the text part of the 2760 message.

The PRE, o sequence indicates to the terminal control unit: (1) that the message is intended for the 2760, and (2) that the three characters following will define the function and the number of filmstrip frames to be moved by the filmstrip transport unit.

The F character determines: (1) mode of operation, (2) direction of film movement, and (3) whether the Manual Frame Advance switch is enabled or disabled (Figure 4-18.) The F character bit code cannot have an 8-bit, but the presence or absence of the A- or B-bit has no effect on the function. A summary of the bit relation to the functions is as follows:

1-Bit	Move Forward
Not 1-Bit	Move Reverse
2-Bit	Set Manual EOM Mode
Not 2-Bit	Set Auto EOM Mode
4-Bit	Enable Local Move switch
Not 4-Bit	Disable Local Move switch

The A_1 and A_2 characters are stored in the vertical and horizontal registers in complement form. They specify the amount of filmstrip movement necessary to display the next I/O image in the application routine (Figure 4-17). The filmstrip movement is initiated after the message is properly received.

Transmit Format

● Automatic EOM Mode is used for transmission of one entry per message.

● Manual EOM mode is used for transmission of multiple entries within a given message.

● The Local Move switch is enabled, for operator control of filmstrip movement.

● The Local Move switch is disabled, for filmstrip motion under control of the CPU program only.

Char.	Bit Config.	Move		Mode Set To		Local Move Switch	
		1-Bit	(Not) 1	2-Bit	(Not) 2	4-Bit	(Not) 4
1	1	Fwd			Auto		Disabled
2	2		Rev	Manual			Disabled
3	1, 2	Fwd		Manual			Disabled
4	4		Rev		Auto	Enabled	
5	1, 4	Fwd			Auto	Enabled	
6	2, 4		Rev	Manual		Enabled	
7	1, 2, 4	Fwd		Manual		Enabled	
Space			Rev		Auto		Disabled

NOTE: Thirty two combinations are possible with 1, 2, 4, A, and B Bits. The presence or absence of the A or B bits has no effect, but an 8-Bit must not be present.

Figure 4-18. Function (F) Control Character

The basic 2760-to-CPU message format is: $\textcircled{D}$, PRE, o, I_1, I_2, V, H, $\textcircled{B}$, LRC. In the variations of this format, the I_1, I_2 characters keep the same significance. These characters are transmitted to the CPU to assure proper indentification of the image The bit configurations of these characters and their respective decimal values are the same as the A_1, A_2 characters in the CPU-to-2760 message format (Figure 4-17).

The filmstrip motion control varies from format to format. The direction of automatic motion and the use of the Local Move switch are defined in the F character of the message previously received from the CPU. A VH coordinate point is transmitted to the CPU in each message, in the form of two characters. These characters, representing the data part of the message, are transmitted from the vertical register and the horizontal register. The character combinations define 243 possible probe response points on the 2760 screen (Figure 4-16). At least one entry (VH coordinate) is transmitted in each message, but in the Manual EOM mode, there may be more than one entry.

Auto EOM Mode

Auto EOM mode is set by the F character (not 2-bit) in the message previously received from the CPU. Only one entry is made in the text of each message transmitted, and the end of message routine ($\textcircled{B}$, LRC) is automatically initiated. Completion of the entry is signaled to the operator when the positive

answerback ($\textcircled{Y}$) is received. (The audible tone sounds and the On-Line light goes off.) Automatic retransmission occurs if a negative ($\textcircled{N}$) answerback is received.

The Auto EOM mode format (2760-to-processor; $\textcircled{D}$, PRE, o, I_1, I_2, V, H, $\textcircled{B}$, LRC) is briefly explained as follows:

$\textcircled{D}$ --Standard 2740-1 bid character.
PRE, o--Prefix, alphabetic o, special character sequence. It
    (1) defines the message as coming from the 2760
    (2) indicates that the next two characters will be I_1, I_2
I_1, I_2--Read-out of the Image Index Counter; defines image defines for the CPU program.
V, H--Response point coordinates; represents data presented on the image defined by I_1, I_2.
$\textcircled{B}$, LRC--Standard end-of-message routine; the record-checking character is generated.

An audible tone is produced to notify the operator that the message was properly received and that additional messages may be transmitted.

Manual EOM Mode

Manual EOM mode is set by the F character (2-bit) in the message previously received from the CPU. If the F character does not contain a 4-bit, the

Manual Frame Advance switch is disabled and the filmstrip motion is under CPU program control. Several entries may be made from a single image, after which the end-of-message is signaled by a utility response point probed by the operator (usually End Entry).

Description of a sample Manual EOM Mode format (Ⓓ , PRE, o, I_1, I_2, V, H, V, H, V, H, V, H, Ⓑ , LRC) is as follows:

Ⓓ--Standard 2740-1 bid character.

PRE, o--Prefix, alphabetic o, sequence is automatically inserted when the first response point is probed. It
   (1) defines the message as coming from the 2760
   (2) indicates that the next two characters will be I_1, I_2

I_1, I_2--Read-out of the Image Index Counter; allows the CPU program to identify the image probed.

V, H --First data entry; an audible tone indicates only that the coordinate characters were transmitted.

V, H --Second data entry; an audible tone indicates proper transmission (Several data entry points may be probed.)

V, H --Last data entry; an audible tone indicates proper transmission.

V, H --Utility response point probed (usually End Entry); coordinates transmitted and EOM routine initiated.

Ⓑ, LRC--End-of-message routine initiated by the previously probed point; Ⓑ and check character are generated and transmitted; an audible tone indicates that the entire message was properly received by the CPU.

Manual Frame Advance

Manual Frame Advance is enabled by a 4-bit in the F character of the previous message received from the CPU. This gives the operator the option to move the filmstrip, one frame at a time, in either direction. The operator is allowed to select the image or images from which entries are to be made. The Image Index Counter is updated by each image change, to assure transmission of a proper count number (I_1, I_2). The count is transmitted the first time any image is probed, after the filmstrip has moved.

Manual Frame Advance enabled allows operational flexibility, and for proper explanation, certain operational assumptions must be made. Thus, let us assume:

1. Manual EOM mode is set and Manual Frame Advance is enabled by the command (F character) from the CPU.

2. The operator views three images and probes six response points for data entry.
3. The operator probes End Entry utility response point to initiate an EOM.

Under these conditions, a sample message format (Ⓓ , PRE, o, I_1, I_2, V, H, V, H; PRE, o, I_1, I_2, V, H, V, H, V, H, V, H, Ⓑ , LRC) is discussed as follows:

Ⓓ , PRE, o, I_1, I_2, V, H--This part of the message is generated and transmitted when the first response point is probed on the first image.

V, H--Second data entry from the first image.

(Semicolon)--Operator manually moves the filmstrip by using the Local Move switch (enabled). Index Count is updated, but no transmission takes place. The operator may move several frames (one at a time) before an entry is made.

PRE, o, I_1, I_2, V, H--This part of the message is transmitted when the first and only point is probed on the second image.

(Semicolon)--No transmission, the Local Move switch is operated for selection of another image; Index Count is updated.

PRE, o, I_1, I_2, V, H--First entry response point is probed on the third image.

V, H--Second data entry from the third image.

V, H--Third data entry from the third image.

V, H--End Entry utility response point initiates the EOM routine.

Ⓑ , LRC--Standard termination of message. Positive answerback causes the audible tone to sound, for indication that a proper message was received by the CPU.

OPERATION

● A film cartridge is inserted and a program is initialized by the 2760 operator.

● Mode and instruction information are received from the central processing unit.

● Data is transmitted by the 2760.

● Appropriate responses are received from the CPU.

To start a program, the operator inserts a film cartridge into the 2760 and probes the Load utility response point. The contents of the Image Index Counter and the VH coordinates for Load are transmitted to the CPU. The T (Transmit) light on the

typewriter and the On-Line light on the 2760 turn
on while the message is being transmitted.

The message received by the Optical Image Unit
contains instructions for film movement and also
sets the mode of operation of the terminal. The
start of the execution of the instruction is at the end
of the message, at which time the 2760 is inter-
locked. During the execution of the instruction, an
incoming message for the 2760 will set the 2740
'error' trigger and a negative reply will be sent at
EOB time. Messages to and from the I/O printer
are allowed, however.

The first (title) image displayed for the operator
contains an appropriate probe response point to
identify the filmstrip in use and the program to be
used. When the operator probes this point, the
information is transmitted to the CPU, and the
application program is called into CPU storage.
Detail data may now be transmitted to the CPU and
appropriate responses received from the CPU until
the operation is terminated by the CPU program or
the operator.

Receive Text from CPU to 2760

- The 2760 receives Ⓓ , PRE, o, F, A_1, A_2,
EOB, LRC.

- The PRE, o, F, A_1, A_2 sequence is the text.

- PRE, o directs the message to the 2760.

- F, A_1, A_2 furnish instructions for the 2760.

Receiving a Ⓓ from the CPU activates the terminal
and prepares it to receive the message. The first
text character of the message intended for the 2760
is a PRE, which is received by the serdes register
(S-register) and transferred to the 1B-register,
where it is decoded for the 2760. The '1B Reg bits',
ANDed with 'invalid character', bring up the 'prefix'
line to the 2760.

The o (alphabetic o, BCD B42), following the PRE,
goes to the 2760 via the 2B-register bit lines in the
2740-1. These bit lines are decoded in the 2760,
which prepares to receive the message as follows:

1. The 2760 sends 'inhibit print OIU' to the 2740-1,
   to turn off the I/O motor and inhibit printout.
2. The 2B-register is reset by '2B reset OIU' and
   is prepared to receive the F character which
   follows.
3. The F, A_1, A_2, instruction message is received
   via S-register, 1B-register, 2B-register, and
   2B-register bit lines to the 2760.

4. The message is ended by EOB character re-
   ceived, and the LRC routine is initiated to
   check the message validity.

An error in the 2760 brings up 'error set gate
OIU' to set the 'error' trigger in the 2740 which
generates a negative answerback. The 'error'
trigger is also set when errors are detected by the
2740-1.

If either the PRE or the "o" are missing from the
message, the 2740-1 is enabled and the message is
directed to the I/O printer.

Transmit Message to CPU from 2760

- Message format is Ⓓ , PRE, o, I_1, I_2, V, H,
EOB, LRC.

- A probe operation initiates message from the
2760 to the CPU via the 2740-1.

- 'Bid N/O OIU' comes from the 2760, which
waits for 'clear to send'.

- PRE, o is generated to identify the message as
being from the 2760.

- The position counter in the 2760 controls genera-
tion and gate-out of characters to 1B-register
bit lines to the 2740.

- A basic 2740-1 sequence transfers the char-
acters from the 1B-register to the S-register
for serialized transmission.

- 'EOB N/O OIU' initiates the ending and record-
checking sequences.

- An error message retransmission is initiated
by an automatic 'restart OIU' from the 2760
in Auto EOM mode.

- An operator probe operation is required for
'restart OIU' if the 2760 is in Manual EOM mode.

The operator probes a response point on the 2760
screen to initiate a message transmission from the
2760. During the transmission, 'keyboard lock OIU'
from the 2760 locks the I/O printer keyboard to pre-
vent 2740-1 operations.

A proper probe operation starts the oscillator,
sets the 'send' latch, and brings up 'bid N/O' in the
2760, which waits for 'clear to send.' The 2740-1
accepts the 'bid N/O OIU' from the 2760 to initiate
the bid, and send the Ⓓ . When 'clear to send'

goes back to the 2760 via the 2740-1, 'on-line' is brought up in the 2760 to allow 'gate out', 'gate out bus', and position counter advance.

The 2760 (in Auto EOM mode) requires only one probe operation to send the PRE, o, I_1, I_2, V, H, EOB, LRC message. As the position counter advances, the PRE and "o" characters are generated to identify the sender for the CPU.

These characters are followed by I_1, I_2 (index counter) and V and H (register) characters gated to the output bus. The output bus is gated to '(bit) transmit out' lines by 'gate output bus.' During each character time (except LRC), the 'transmit out' bits become input to message parity transmit logic, and 'C transmit out' is brought up, if needed for odd parity.

The transmit-out bit lines from the 2760 are gated into the 1B-register in the 2740. During each character time, defined by the 2760 position counter, 'gate out' comes up to bring up 'gate out strobe OIU' which sets the 'strobe O' latch in the 2740. 'Strobe O' sets 'strobe', and 'strobe' gates the character into the 1B-register.

A basic 2740-1 transmission sequence transfers the characters from the 1B-register to the S-register, where they are serialized to the transmission line.

At the proper position count, 'EOB N/O OIU' from the 2760 brings up 'EOB-1', and the message-end and LRC-check sequence follows. If an error is detected, the 'F-mode' latch is set in the 2740 and 'F mode latch OIU' is sent to the 2760. In the 2760, 'F-mode,' 'clear to send,' and 'not restore keyboard' bring up ' Ⓝ '. 'Auto EOT' and ' Ⓝ ' bring up 'restart to 2740', and the message is automatically retransmitted.

While the 2740 is in transmit LRC mode, 'on line,' 'A mode,' 'D mode,' and 'L mode' set the 'rec ansbk' latch in the 2760. 'Rec ansbk' and the appropriate 2740 mode latch lines decode as Ⓒ , Ⓓ , or Ⓨ to terminate the transmission. For example, 'rec ansbk,' 'not B mode,' 'not D mode,' and 'not F mode' bring up ' Ⓨ ', which first becomes 'EOT N/O OIU' and then 'EOT-1' in the 2740. 'EOT-1' brings up '1-B generate' to send EOT, and the message is complete.

If the 2760 is in Manual EOM mode, the operator must manually reset the error condition and probe again to retransmit the message. Manual EOM mode allows more than one probe operation within a message, but the registers retain only the characters for the last probe point; therefore, the operator must reconstruct the entire message after an error is detected in Manual EOM mode.

SECTION 17. TRANSMIT INTERRUPT (2741)

● A 2741 in transmit text mode receives a 200 ms "space" from the multiplexer and is forced to the receive control mode.

● The terminal must be connected to the multiplexer on full-duplex lines.

This feature is used only when the terminal is in transmit text mode. If the 2741 is transmitting text and a "space" condition occurs for 200 ms on the receive data line, the 2741 is forced to the receive control mode. In receive control mode the keyboard is locked and the terminal monitors the line until a (D) takes the terminal to receive text or a (C) takes the terminal to transmit text.

The multiplexer must transmit a minimum of one character time of "mark" signal following the 200 ms of "space" to allow the 2741 to properly recognize the next character received.

The printed data at the 2741 is not necessarily identical to the transmitted data for the print line during which the interrupt occurs. Thus, the interrupt is considered as a terminating condition which voids the entire print line.

The logic for the transmit interrupt feature is on AA671. A 200 ms "space" signal on the 'serial data in' line ANDed with the B mode latch off (transmit mode) fires a 100 ms time delay that beings up 'A reset gate'. Reset forces the terminal to control receive mode to receive the next control character from the multiplexer.

The terminal must be connected to the multiplexer on full-duplex lines to use the transmit interrupt feature. This enables the terminal to receive the "space" at the same time that it is transmitting data.

SECTION 18. PRINT INHIBIT CPU CONTROL (2741)

- Enables the CPU to inhibit the 2741 from printing transmitted or received data.

- Codes used are 'bypass' (A 8 4) and 'restore' (B 8 4).

When the 2741 receives a "bypass" code, all further printing is inhibited until a "restore" code is received, or the 2741 is powered off and on. All printed characters received or keyed from the keyboard while the terminal is in print suppression mode cause the print element to function, but not print.

All function codes are recognized as they are received.

'Power on reset' sets the 'bypass restore' latch and resets the 'print inhibit' latch (AA691). When the terminal is in receive text mode and a "bypass" code is received, the 'bypass restore' latch is reset. The reset of the 'bypass restore' latch and '(not) IO cycle' sets the 'print inhibit' latch which picks and holds the non print magnet until a "restore" code and receive text mode set the 'bypass restore' latch. The 'bypass restore' latch and '(not) IO cycle' resets the 'print inhibit' latch and drops the non print magnet.

Figure 5-1 is a block diagram of the 2740/2741 power supply and input voltages for domestic and World Trade use. The different voltages and cycles are accommodated by using a different transformer, different taps on the transformer, or both. Internally, the power supply functions the same for all inputs. The outputs of the power supply are: +48 volts dc, +12 volts dc, and -12 volts dc. The +48 volts is used in the I/O device. The +12 and -12 volts are used by the SLT logic. The power supply also supplies the power-on reset, described in Chapter 3.

Although similar to the 2740 power supply in every other respect, the 2741 power supply does not contain an alarm bell.

CAUTION
Terminals wired for 115VAC, 60 cycle do not use the same transformer as terminals wired for 208/230 VAC. If the power supply is wired for 208/230 VAC (Transformer taps 11 or 12), it must not be changed to the 115 VAC wiring (tap 10), or vice versa, or the supply will be damaged.

The proper transformer should be used for the available line voltage.

ac Input	Old Style (All Models)	New Style (2740-2)
Domestic 60 Cycle	115 208/230	100/115 200/208/230
World Trade 50 Cycle	112.5 123.5 195 220 235	100 110 123.5 200 220 235
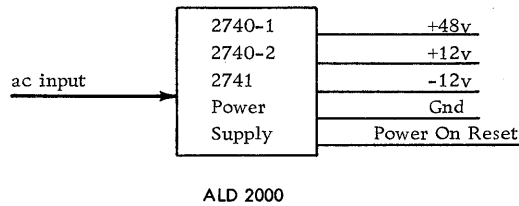
Figure 5-1. 2740/2741 Power Supply

ALD 2000

CE AID BOX

- Used for dynamic troubleshooting.

- Shows condition of 1B-register, mode triggers, and 'parity error or not S8' trigger.

- 2B-register can also be displayed on 2740-2.

- Allows terminal to be single-cycled.

- Contains a Space character generator.

The CE Aid Box helps the Customer Engineer diagnose terminal failures under dynamic conditions. The CE can observe the contents of the 1B-register (also 2B-register on 2740-2),the condition of the mode triggers, and the condition of the 'parity error or not S8' latch (P). A single-cycle circuit that allows the terminal to be cycled through its operations is incorporated into the CE Aid Box. In addition, the reception of a Space character can be simulated using the space generator circuit. The space generator causes the terminal to receive Spaces continuously so that the CE can check the terminal.

The CE Aid Box is an external device that is plugged into a receptacle on the terminal gate. All power for the CE Aid Box is provided by the terminal power supply. Figure 6-1 shows the location of the CE Aid Box lights and switches.

Figure 6-1. CE Aid Box

Single Cycle

- Character is held in the register(s) until CE presses Cycle (pushbutton).

By setting the 1CH (single-cycle halt) switch on the CE can single-cycle the terminal. With the switch in the off position, the terminal operates normally.

2740-1/2740-2/2741

During transmit operations, the character is held in the 1B-register. Pressing the cycle pushbutton causes the character to be transferred to the S-register for transmission. The next character is then loaded into 1B.

For receive operations each character is received in the S-register and transferred to the 1B-register. The character is held in 1B until the cycle button is pressed. It then transfers to 2B and prints.

2740-2

NOTE: EC306818 must be installed on the CE Aid Box to enable 1CH functions to operate with the Model 2.

The 2B-register may be displayed on the 2740-2 by moving the paddle card on the B board from location C1 to D1. The 2740-2 has the following additional single-cycle capabilities:

1. Enter
2. Buffer print
3. Buffered receive

During Enter, a character is loaded into the 2B-register. The operation of the cycle pushbutton increments buffer address and stores the character in buffer. A second depression of the cycle button is required to reset 2B and allow another character to be entered.

Buffer print gates the character to 2B-register. The cycle button allows the character print and 2B reset.

Receive with Buffered Receive feature is initially the same as any receive operation. The first depression of the cycle button transfers the character from 1B-register to 2B-register and from 2B-register into buffer. The second operation of the cycle button

resets 2B-register and allows a new character to be accepted from the line.

Operation

Figure 6-2 shows the single-cycle circuit. With the 1CH switch at ON the '1cycle halt' line activates the single-cycle circuit. For an enter operation, when 'strobe' and 'not strobe O' come up, an AND is conditioned to turn on the 'stop clock' trigger. 'Stop clock' degates the control oscillator inputs to the control-clock triggers. The character is now in 2B. The control clock must run to enter the character into buffer storage.

For the control clock to run, the CE must press the Cycle pushbutton. This causes 'cycle N/O 1' to come up to turn on the 'cycle' trigger. The 'cycle' trigger on and the 'cycle interlock' latch off (turned off when 'stop clock' came up) condition an AND to bring up 'stop clock reset gate', turning off the

'stop clock' trigger. The 'stop clock' trigger off and the 'cycle N/O' line still up turn on the 'cycle interlock' latch. The 'cycle interlock' latch degates 'stop clock reset gate.' The Cycle pushbutton must be released and again pressed to cycle the terminal.

When the CE releases the Cycle pushbutton, 'cycle N/C' comes up and turns off the 'cycle' trigger; the 'cycle interlock' latch remains on until the 'stop clock' trigger is again turned on.

During receiving operation, when 'C1' 'not 2B reset,' and 'S-register empty' come up (indicating that a character is in 1B), the 'stop clock' trigger turns on. The procedure to cycle the terminal is the same as for the transmit operation, except the data transfer is to 2B and printer instead of the line.

The operation with the 2740-2 is identical to the above description with the following exception: the control clock is stopped at the end of each buffer character cycle (Top AND to turn on 'stop clock' trigger, Figure 6-2). This circuit is required
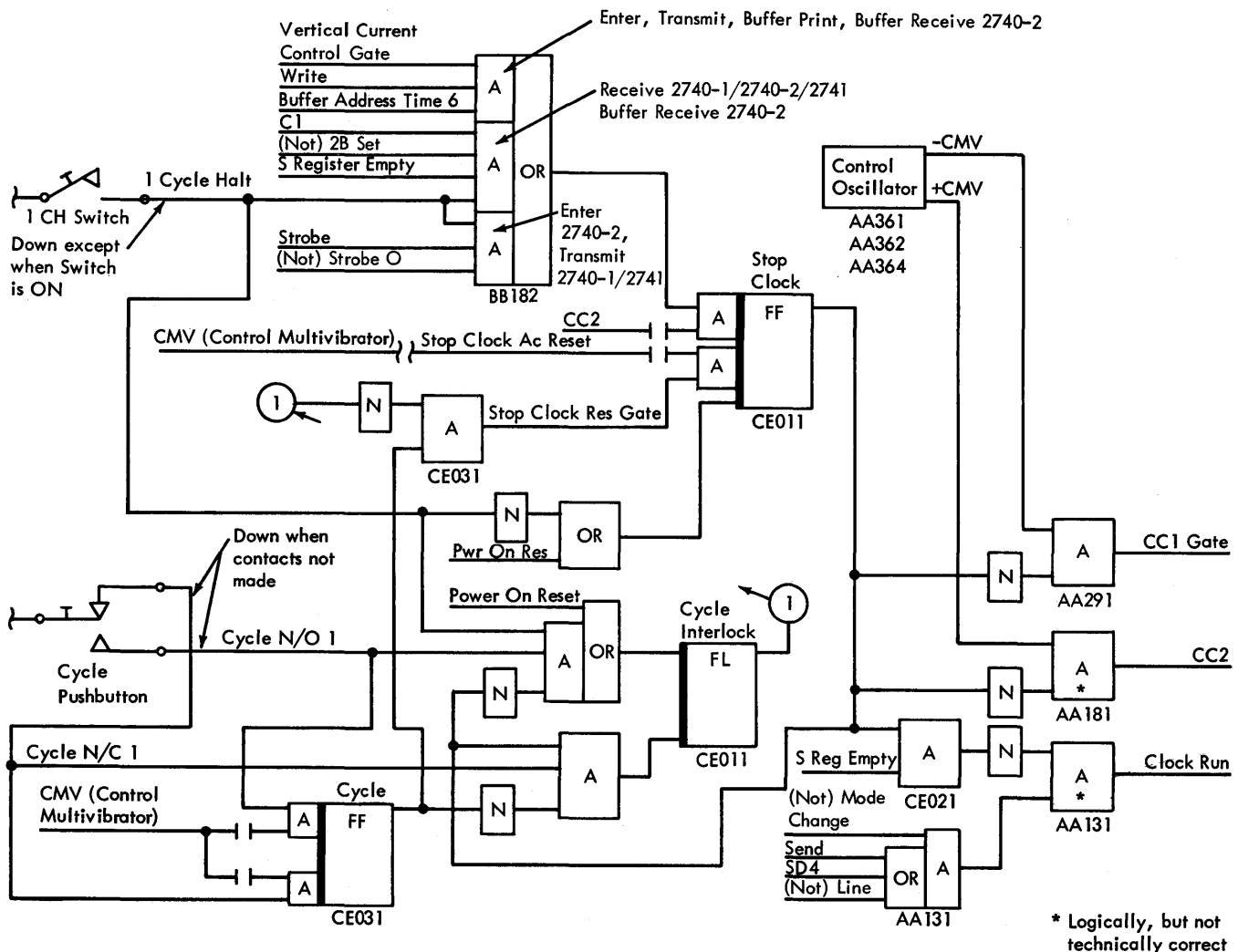
Figure 6-2. Single Cycle

during buffer print and transmit since the data source is the buffer. However, the circuit effects operation during enter and buffer receive.

During both enter and buffer receive, the character is transferred to buffer with the first depression of the cycle button. As the character is loaded into buffer, 'vertical current control gate', 'write' and 'BAT 6' turn on the 'stop clock' trigger. A second depression of the cycle button is required to reset 2B-register and allow the next character to be set into 2B-register.

Space Generator

● Continuously loads Space characters into the S-register.

● Simulates carrier.

● Blocks power-on reset.

The space generator continuously simulates Space characters (C-bit only) on the 'serial data in' line. Thus the CE can check the operation of the terminal and I/O device while in receive mode without using another terminal. Figure 6-3 shows the space generator sequence. Figure 6-4 shows the logic that generates the Space character.

Normally, the 'received data' line from the line adapter is in a "marking" or up condition when data is not being received. An AND, conditioned by 'received data' and 'not space N/O' is the source of the 'serial data in' line. When the CE turns on the Space switch, the AND is deconditioned and 'serial data in' drops. This simulates a start bit and starts the serdes clock.

The S-register loads with no-bits until the start bit reaches 'S2;' 'not S2' brings up the 'serial data in' line. With the start bit in 'S2,' the timing is such that when the 'serial data in' line comes up, a C-bit is loaded into the S-register. The next bit shifted into 'S2' is a no-bit; therefore, 'serial data in' remains up and loads the stop bit.

Once the complete character is in the S-register, the character transfers to the 1B-register and '1B7' comes up. '1B7' continues to hold the 'serial data in' line up mark condition. When the character in 1B transfers to the 2B-register, '1B7' drops and the loading of another space character begins. The '1B7' input prevents the terminal from generating spaces faster than the I/O printer can use them. Also, when the CE turns on the Space switch, 'space N/O' coming up simulates 'carrier,' which allows the terminal to operate in receive mode without line-adapter carrier. 'Space N/O' also blocks the power-on reset circuit.

CHECK LOOP (2740-1/2741 only)

● Permits the I/O device to be checked dynamically off-line.

● The strobe circuit is forced up to gate the transmit contacts to 1B.

● '2B set' is forced up to transfer 1B to 2B.

● The character in 2B then restarts the I/O device.

The check-loop circuit allows the CE to check the I/O device off-line. To check the I/O device, the CE causes the device to repeatedly print any I/O character or perform any I/O function except shift. When the CE presses the Bid key on the 2740-1 or the Attention key on the 2741 while the terminal is in local mode, the check-loop circuit is activated. Pressing any other key on the I/O keyboard causes the character to be printed or the function to be performed continuously until the Bid key is released. Data flow is shown on Figure 6-5.

When 'not send,' not clock run,' '1B empty,' and 'local' are up, pressing the Bid key turns on the 'repeat' trigger (Figure 6-6). Before the 'repeat' trigger comes on, the 1B-register is reset by 'mode change,' which is forced up by 'not repeat,' 'not send,' 'local,' and 'bid 1.' Pressing an I/O key starts the I/O cycle, during which the transmit contacts are set up in the configuration of the character. When the 'strobe N/O' contacts make, the 'strobe O' trigger turns on to start the normal sequence that gates the contents of the transmit contacts to the 1B-register and '1B full' comes up. As soon as 'strobe' drops, the '2B set' trigger turns on to transfer the character to the 2B-register. Just as in a receiving operation, the character in 2B is gated to the I/O magnets, causing the I/O to recycle. To stop the operation, the CE releases the Bid key. When the present cycle ends, the 'repeat' trigger turns off.

During check-loop operation the following occurs:

1. The 1B OK circuit is disabled to prevent recognition of any control characters.
2. The power-on reset circuit is disabled.
3. The 'local/communicate' trigger is held in local.
4. The 'serial data in' line is held at mark level to prevent the reception of data.

If the station-control feature is installed in the terminal, 'repeat' holds the terminal in text non-selected mode, holds the 'garble' trigger on, and blocks the turn-on of the 'time-out 15' latch.

When the terminal is in communicate mode, the 'repeat' trigger is held off.
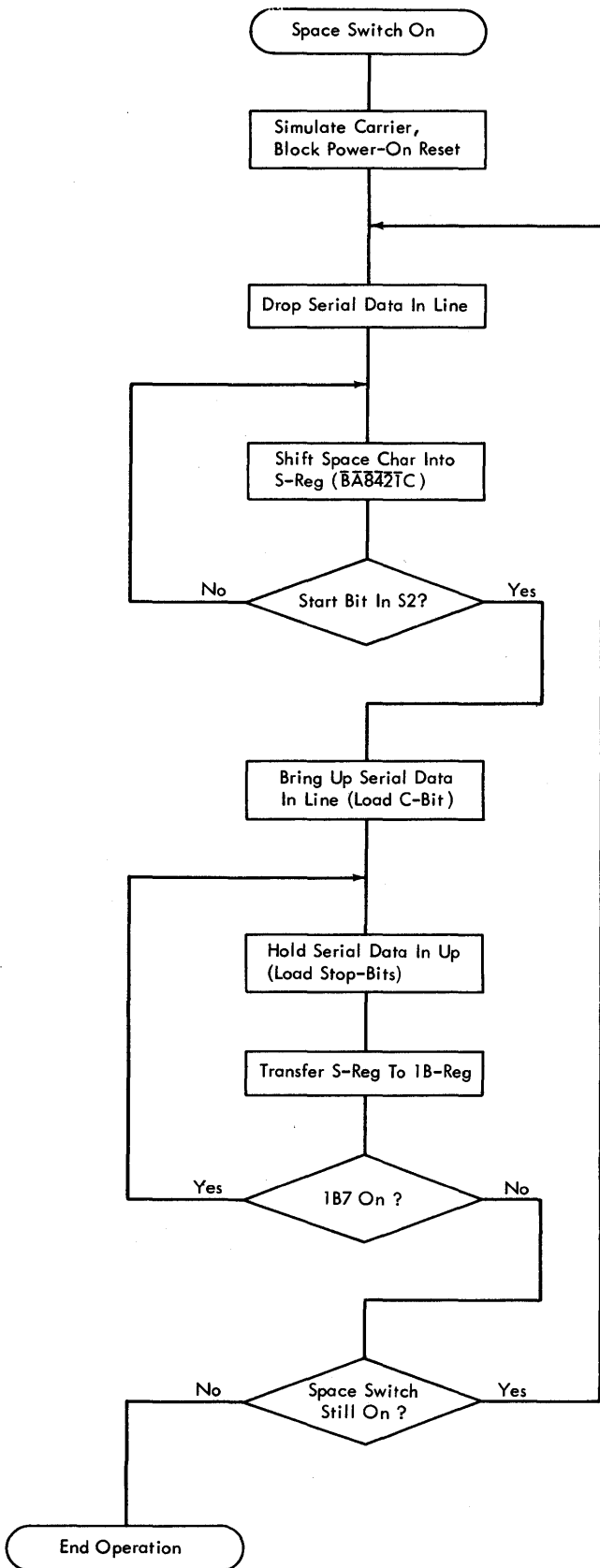
Figure 6-3. Space Generator Flowchart
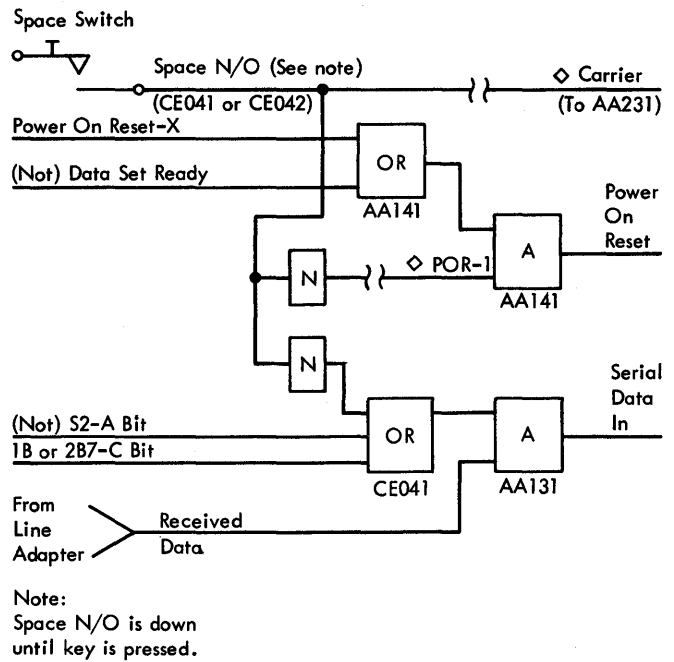
Figure 6-4. Space Generator

Note:
Space N/O is down
until key is pressed.
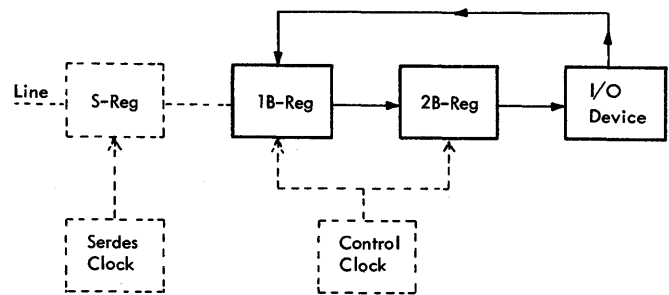
Figure 6-5. Check Loop Data Flow
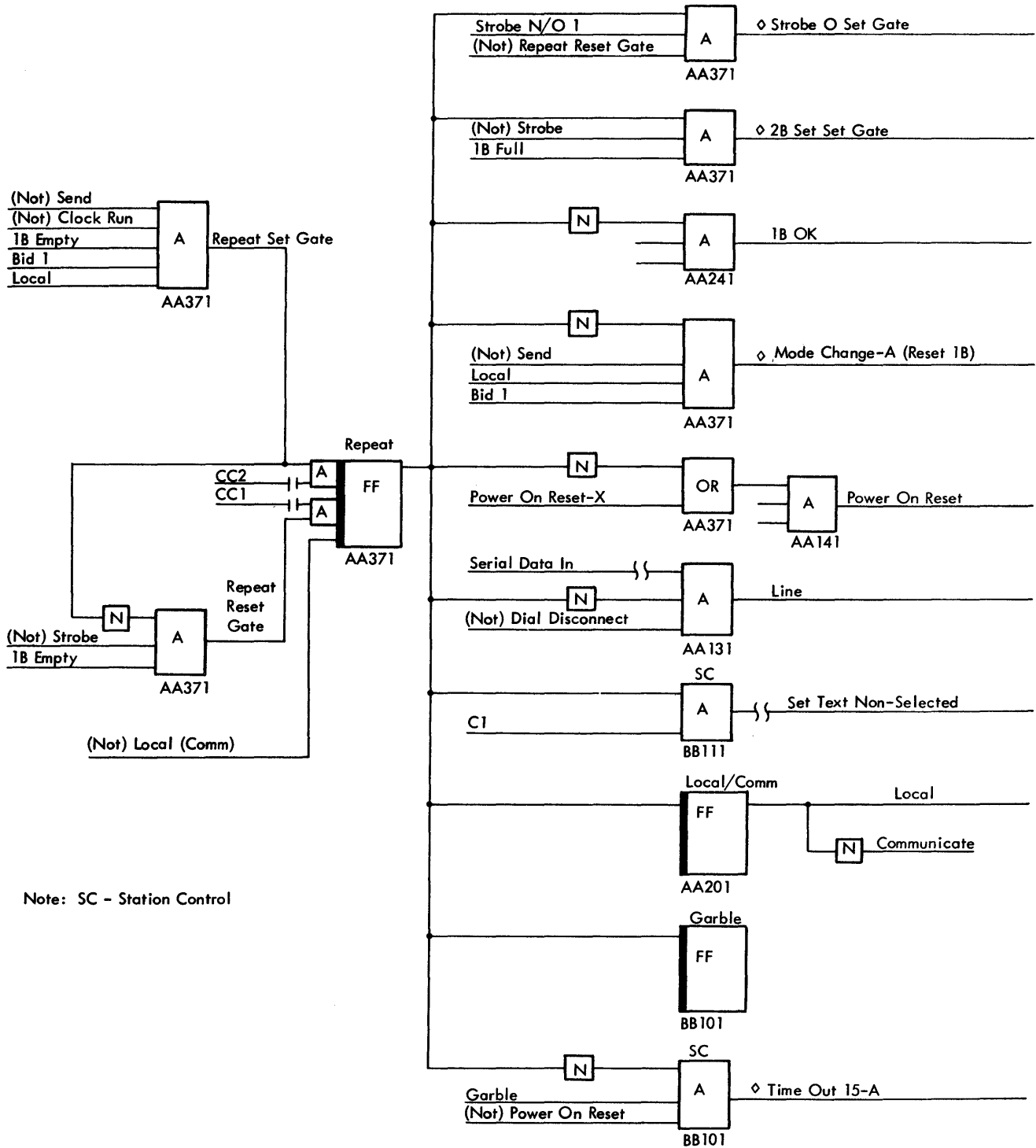
Note: SC - Station Control

Figure 6-6. Check Loop

COMMUNICATIONS TERMINALS 2740-1/2741

Dimensions: Width 28 3/4"
             Depth 25 1/4"
             Height (Overall) 36 1/2"
             Height (Desk-Top) 29"

Maximum Weight: 196 lbs

Service Clearances: Front 30"
                     Rear 42"
                     Left 18"
                     Right 18"

Electrical Requirements:
    Voltage   115 or 208/230 $\pm$ 10%
    Service   15 amps
    Frequency   60 $\pm$ 1/2
    Phases   1
    KVA   0.15

Temperature Range:
    +50 F. to +100 F.

Humidity Range:
    10% RH to 80% RH

Maximum Wet Bulb Temperature:
    85 F

The 2740/2741 can communicate with other terminals or System/360 over these facilities:

● Common-carrier switched telephone network with Western Electric Data Set 103A (or equivalent).

● Common-carrier switched 150-baud teletype-writer exchange (TWX) network with Western Electric Data Set 103A (or equivalent).

● Common-carrier leased private-line telephone service with Western Electric Data Set 103F (or equivalent), IBM Leased Line Adapter, or IBM Shared Line Adapter (or equivalents).

    NOTE: Common-carrier data sets and IBM Line Adapters cannot be mixed in the same network.

● Common-carrier leased private-line telegraph service (telephone company 150-baud, schedule 3A channel) with appropriate channel termination.

● Western Union Class D (180-baud) channel with Western Union Data Loop Transceiver 1183-A (or equivalent).

● Western Union Class E channel with IBM Leased Line Adapter, or IBM Shared Line Adapter (or equivalents).

● Privately owned communications facilities with other modulator/demodulator equipment similar to IBM Line Adapters or common carrier data sets incorporating the proper interface.

● Local or in-plant customer installed or common-carrier wiring with IBM Limited-Distance Line Adapter Type 1 (for distances up to 4.75 miles) or IBM Limited Distance Line Adapter Type 2 (for distances up to 8.25 miles).

COMMUNICATIONS TERMINAL MODEL 2

Dimensions

    Width: 36 in.; Depth: 29 1/2 in.;
    Height (Overall): 36 1/2 in.;
    Height (Desk-Top): 28 7/8 in.

Maximum Weight

    200 lbs (90.7 kg)

Service Clearances

    Front: 30 in.; Rear: 42 in.;
    Left: 18 in.; Right: 18 in.

Electrical Requirements

    Voltage: 115 or 208/230 $\pm$ 10%
    Frequency: 60 $\pm$ 1/2 Hz
    Phases: 1
    kva: 0.15
    Service Amperes: 15
    Plug Types:
      Hubbell or Pass & Seymour 5267 (115v, non lock)
      Hubbell or Pass & Seymour 4720 (115v, locking)
      Hubbell 5666 (208/230v, non lock)
      Hubbell or Pass & Seymour 4770 (208/230v, locking)
    Receptacles: Customer provides matching receptacles--Hubbell or Pass and Seymour 5262 for 5267

plug; 4700 for 4720 plug; 5662 for 5666 plug; and 4750 for 4770 plug.

Circuit: Circuit should be separate three-wire, single-phase branch circuit from power distribution panel, with green wire connected to ground, not current neutral.

Environmental Specifications

BTU/hr: 400 (101 kcal/hr)

Temperature: 50-110°F (10-43°C), Operating and Nonoperating;

Relative humidity: 8-80%, Operating and Nonoperating

Wet Bulb Temperature: 85°F (29°C) max, Operating and Nonoperating.

Shipping Temperature: For shipping, temperature limits are -40° to +150°F (-40° to +66°C)

Conversion Table

Inches (in.)	Centimeters (cm)	Feet (ft)	Meters (m)
18	45,7	6	1,83
28 7/8	73,9	8	2,44
29 1/2	74,9		
30	76,2		
36	91,4		
36 1/2	92,7		
42	106,7		

Communications Facilities

The IBM 2740 Model 2 can communicate with a System/360 over the following facilities:

- Telephone Company leased private-line telephone service, Western Union Class E or G channels, or equivalent privately owned communications facilities, using an IBM Leased-Line or Shared-Line Adapter.

- Telephone Company leased private-line telephone service with Western Electric Data Set 103F2 or 202D1 or equivalents.

- Western Union Class D (180-baud) channel using a Western Union Data Loop Transceiver 1183-A or equivalent.

- Telephone Company Type 1006 (150-baud) private-line telegraph service with appropriate channel termination.

- Telephone Company Type 1005 (75-baud) or Western Union Class C (75-baud) channel.

- Local or in-plant customer-installed or common-carrier facilities with IBM Limited-Distance Line Adapter Type 1 (for distance up to 4.75 miles) or IBM Limited-Distance Line Adapter Type 2 (for distance up to 8.25 miles).

- Equivalent privately owned communications facilities with IBM Line Adapters or other modulator/demodulator equipment similar to IBM Line Adapters or common-carrier data sets incorporating the proper interface.

NOTE: Common-carrier data sets and IBM Line Adapters cannot be mixed on the same channel. For additional information on IBM Line Adapters, see the publication, Planning and Installation of a Data Communications System Using IBM Line Adapters, Form A24-3435-2 or later edition.

Signal-Cable Chart

Signal Cable	Length	Diameter	Connector Supplied by IBM	Matching Connector Supplied by Customer
From 2740 to Data Set	8 ft	3/8 in. (0,95 cm)	EIA RS-232A or equivalent	Supplied with Data Set by Common Carrier.
From IBM Line Adapter (Special Feature) to Communications Line	8 ft	3/8 in. (0,95 cm)	Western Electric 283B plug or equivalent	Western Electric 404B (or equivalent for Surface Mounting, or Western Electric 493A (or equivalent) for Flush Mounting.
From Telegraph Line Adapter (IBM Special Feature) to Communications Line	8 ft	5/16 in. (0,79 cm)	#8 Ring Lugs	Attaches to Common-Carrier Terminal Board.

SPECIAL CIRCUITS ON CARD AT LOCATION A1M4
(Figure B-1)

Voltage Reference (Block 2H)

● Fixed voltage for sense-amplifier-sensitivity
reference.

● Fixed voltage for temperature-compensation
reference.

Temperature-Compensation Voltage (Block 3H)

● Thermistor resistance to ground varies inversely
with temperature change.

● Thermistor input to compensation circuit modi-
fies reference voltage.

● Compensated reference voltage at A1M4D09 regu-
lates forward bias of current-control circuits.

The fixed-reference voltage and the thermistor out-
put comprise the inputs necessary to provide a pre-
cise current-control reference voltage that varies
with array temperature. The voltage level at
A1M4D06 becomes more positive as array tempera-
ture drops and less positive as array temperature
rises. It is pre-adjusted at a given temperature and
locked at the factory. This level clamps the inputs
to the I Control blocks (3C) to limit forward bias.

Differential Amplifier, Strobe AND, and Strobe
Delay (Blocks 3D, 2E, and 4D respectively)

● Operates on a difference in voltage on the two
ends of the Sense line.

● Output at A1M4D04 is positive, regardless of
sense input, until the strobe delay elapses.

● Strobe AND satisfied when horizontal current
starts.

● Strobe delay allows time before sampling for the
core to start resetting in response to coincident
array currents.

The sense amplifier has two parts. The first is a
differential amplifier, which senses and amplifies a
voltage difference between the ends of the array sense
winding. The second, a clamp circuit, allows the

differential amplifier to operate only when certain
conditions are satisfied. These conditions are: 'not
enter, ' 'read, ' 'horizontal current, ' and '200N delay.'
The delay begins at the start of horizontal current
and times out at the time when a resetting core has
started to change magnetic states. Thus, the sample
for a changing core is on the steep part of the Sense
line signal (Figure B-1).

SPECIAL CIRCUITS ON CARDS AT LOCATIONS
A1G4 AND A1G5 (Figure B-1).

Current Control (I Control, Blocks 3C)

● Provide gating to drivers and switches.

● Regulate current-carrying capability of sinks
(negative).

As explained under "Temperature-Compensation
Voltage, " the I Control input at pin B08 limits for-
ward bias at a level that varies with array tempera-
ture. The other I Control inputs are logical, having
to do with array line-current direction and timing.
    Transistors in the current-control circuits are
cascade-connected to transistors in the current sinks
(I Control transistor collector to current-sink trans-
istor emitter). Thus, limited forward bias in the
current-control circuit limits the amount of current
that can be conducted by the sink.
    When an array line carries current, a source is
conditioned at the positive end and a sink at the nega-
tive end. The source can conduct no more current
than the sink will provide, so array line current is
limited. By this means, temperature-compensation
circuits allow for higher array currents when the
array is cold, lower currents when it is warm.
    The ANDed inputs and corresponding outputs
from the current-control blocks are as follows:

AND Input Pins	AND Output Pins
B08, D12, B13	D10
B08, D12, D02	D06

Whenever either AND is satisfied, the current line
at D07 rises from ground to its positive value. This
level rises because of its electrical function as a
negative emitter source in the current-control circuit
and a negative collector return for the current sinks.
The positive level at D07 serves the logical function

Figure B-1. Current and Data Controls

-MEMORY BUFFER RESET GATE

-POWER ON RESET

-MEMORY BUFFER SET GATE

- CC2

THERMISTOR
V REFERENCE
(FROM FIG. B-2)

SPEC
V25AC
B-A1M4
2H-SA

B07

B07 X

TEMP COMP V

*SPEC
V25AB
B-A1M4
3H-SB

D06 X

D09

SENSE LINE 1
SENSE LINE 2

DIFF. AMPL.
G08
J06
AR-DF
V07AZ
B-A1M4
3D-SH

G05

G13
G07 N

*A
V20AB
B-A1M4
5B-SC

D11

*OR
V20AC
B-A1M4
6B-SD

MEM. BFR.

*FL
V20AD
B-A1M4
7B-SE

J13*

J10

+ MEMORY BUFFER

-MEMORY BUFFER

J07
J09 N

*A
V20AB
B-A1M4
5C-SG

D13

*OR
V20AC
B-A1M4
6C-SF

D04 SENSE AMP BIT

B13 STROBE DELAY

J04 HORIZONTAL CURRENT

+VERTICAL CURRENT SOURCE GATE
- ENTER

J12
D07
J05
J04
G10

TD 200NS
*SPEC
V45DF
B-A1M4
2E-SJ

KB13

G05

JMPR
S61AF
B-A1M4
4D-SK

D04

J06/G08 DIFFERENTIAL
+HORIZONTAL CURRENT
+VERTICAL CURRENT
VERTICAL SWITCH READ GATE
VERTICAL DRIVER WRITE GATE

-RECEIVE TEXT BUFFER

+READ ODD-WRITE EVEN

+VERTICAL CURRENT CONTROL GATE

D12
B13

A
V03CM
B-A1G5
2C-AA

B08

I CONTROL
*SPEC
V25AD
B-A1G5
3C-AF

D07
D10
D06

B13
B04

A
V32AC
B-A1G5
2F-AC

D09

VERTICAL DRIVER READ GATE

D12
D02

A
V03CM
B-A1G5
2D-AB

D02
B04

A
V32AC
B-A1G5
2G-AD

B07

VERTICAL SWITCH WRITE GATE

+ READ EVEN-WRITE ODD

+ READ
+MEMORY GO

- HORIZONTAL SWITCH READ GATE
- HORIZONTAL DRIVER WRITE GATE

+ WRITE
+HORIZONTAL CURRENT CONTROL GATE

D12
B13

A
V03CM
B-A1G4
2C-AA

B08

I CONTROL
*SPEC
V25AD
B-A1G4
3C-AF

D07
D10
D06

B13
B04

A
V32AC
B-A1G4
2F-AC

D09

- HORIZONTAL DRIVER READ GATE

+MEMORY BUFFER

D12
B05
D02

A
V03CM
B-A1G4
2D-AB

D02
B04

A
V32AC
B-A1G4
2G-AD

B07

- HORIZONTAL SWITCH WRITE GATE

NOTE:
SEE DIAGRAM 4-18 FOR LOGIC OF
DIFF. AMPL., MEM. BFR., AND
I CONTROL. V REFERENCE IS A
CONSTANT VOLTAGE SOURCE,
AND TEMP. COMP. V CONTROLS
ARRAY CURRENTS. ARRAY CURRENT
DECREASES AS TEMPERATURE RISES.

ALD PAGES:
DD011
DD012
DD013

of timing sense-amplifier strobe in reference to horizontal current (block 2E).

SPECIAL CIRCUITS ON CARDS AT LOCATIONS A1H6, A1H7, A1J3, A1J4, A1J5, A1J6, A1J7 (Figure B-2)

Current Sources and Current Sinks (Blocks 4B, 3C, 4L and 3M)

- These circuits conduct array line current

- Driver and switch circuits are identical; each contains a positive source and a negative sink.

- Source and sink outputs are common in driver circuit.

- Source and sink outputs are diode-isolated in switch circuit; diodes are on array card.

The electron flow of array current is from a negative sink to a positive source. The negative origin is the current line at A1D6D07 (horizontal) or A1D5D07 (vertical). The positive termination is a resistor to +12 volts A1D5D04, horizontal; A1D6D04, vertical.

Array-current timing, direction (selection of source or sink), and amount are determined by current-control inputs to the driver and switch circuits. Addressing takes effect at the driver or switch, so that only one element of each group conducts--i.e., one horizontal driver, one horizontal switch, one vertical driver, and one vertical switch. Selection of a source or sink conduct current is equivalent to a logical AND, as follows:

Source

ANDed Inputs	Output
+ on Address lines - on Gate line	+ (Driver, or Switch Out)

Sink

ANDed Inputs	Output
+ on Address lines - on Gate line	- (Driver, or Switch In)

SPECIAL CIRCUITS ON CARD AT LOCATION A1L4 (Figure B-2)

Core-Array Current Lines (Blocks 4B and 4E)

- Connections to vertical and horizontal lines.

- Switch In and Switch Out line-isolation diodes are on array card A1L4.

- Branching of driver and switch lines to form the array matrix is land-pattern wiring on the array card.

Array Sense Winding (Block 4H)

- Passes through each and every core.

- Crossovers tend to cancel unwanted signals.

- Change in magnetic state of a core induces potential difference (approximately 30 millivolts) between ends of sense winding.

- Ends of sense winding connect to differential amplifier.

Thermistor (Block 4K)

- Mounted on array card inside array cover.

- Temperature-sensitive resistor; increases resistance with temperature drop, decreases with temperature rise.

- One end grounded, other end connects to temperature-compensation circuit.

Figure B-2. Core Array Circuits

CURRENT SOURCE   CURRENT SINK

	S12	HORIZONTAL SWITCH 1 IN	U12	◇HORIZONTAL SWITCH 1 OUT BEX
HORIZONTAL SWITCH 2 IN	S04		S07	◇HORIZONTAL SWITCH 2 OUT BEX
HORIZONTAL SWITCH 3 IN	U13		S13	◇HORIZONTAL SWITCH 3 OUT BEX
HORIZONTAL SWITCH 4 IN	S09		S08	◇HORIZONTAL SWITCH 4 OUT BEX
HORIZONTAL SWITCH 5 IN	B03		B05	◇HORIZONTAL SWITCH 5 OUT BEX
HORIZONTAL SWITCH 6 IN	B09		B08	◇HORIZONTAL SWITCH 6 OUT BEX
HORIZONTAL SWITCH 7 IN	B02		D02	◇HORIZONTAL SWITCH 7 OUT BEX

*ARRAY B-A1L4 4E-SB

HORIZONTAL SWITCH 1 OUT

HORIZONTAL DRIVER 1	G04
HORIZONTAL DRIVER 2	G03
HORIZONTAL DRIVER 3	G02
HORIZONTAL DRIVER 4	B13
HORIZONTAL DRIVER 5	B12
HORIZONTAL DRIVER 6	M05
HORIZONTAL DRIVER 7	G10

HORIZONTAL SWITCH WRITE GATE

HORIZONTAL SWITCH READ GATE

+ HORIZONTAL CURRENT

+ BUFFER ADDRESS TIME 0

+12 VOLTS
R 561KW
B-A1G4 2L-AE

A V03CJ
B-A1J7 2B-AA

*SPEC V32AD
B-A1J7 4B-AJ

*SPEC V32AE
B-A1J7 3C-AE

VERTICAL SWITCH 1 IN	S02		S03	◇VERTICAL SWITCH 1 OUT BEX
VERTICAL SWITCH 2 IN	M13		M12	◇VERTICAL SWITCH 2 OUT BEX
VERTICAL SWITCH 3 IN	D04		B07	◇VERTICAL SWITCH 3 OUT BEX
VERTICAL SWITCH 4 IN	D09		B10	◇VERTICAL SWITCH 4 OUT BEX
VERTICAL SWITCH 5 IN	U11		U10	VERTICAL SWITCH 5 OUT
VERTICAL SWITCH 6 IN	U06		S05	VERTICAL SWITCH 6 OUT
VERTICAL SWITCH 7 IN	D07		D10	VERTICAL SWITCH 7 OUT
VERTICAL SWITCH 8 IN	D06		B04	VERTICAL SWITCH 8 OUT

*ARRAY B-A1L4 4B-SA

VERTICAL DRIVER 1	P05
VERTICAL DRIVER 2	M03
VERTICAL DRIVER 3	M02
VERTICAL DRIVER 4	G12

CURRENT SOURCE

+ BUFFER ADDRESS 9 AND 10   B04

- BUFFER ADDRESS 12   D13

- HORIZONTAL DRIVER READ GATE

A V03CJ
B-A1J4 2L-SJ

*SPEC V32AD
B-A1J4 4L-SH

CURRENT SINK

HORIZONTAL DRIVER WRITE GATE

+ HORIZONTAL CURRENT

*SPEC V32AE
B-A1J4 3M-SG

ARRAY TERMINAL D73

A1L4J04

D71

A1L4J05

ARRAY B-A1L4 4H-SC

| J05 | SENSE LINE 1 |
| J04 | SENSE LINE 2 |

HORIZONTAL SWITCH 1 IN   A1L4S12

HORIZONTAL SWITCH 1 OUT   A1L4U12

A3 ARRAY TERMINAL

C3 ARRAY TERMINAL

A1L4G04 HORIZONTAL DRIVER 1

(PARALLEL TO VERTICAL)

R S61KX
B-A1L4 4K-SD

| S10 | THERMISTOR |

TO FIG. B-1

A1L4U08   A1L4S10

TEMPERATURE UP/RESISTANCE DOWN
TEMPERATURE DOWN/RESISTANCE UP

NOTE: 'GATE' LINES ARE EMITTER SOURCES SWITCHED BY 'I CONTROL' (FIG. B-1)

The World Trade version of the IBM 2740 is func-
tionally the same as the domestic machine. There
are some logic changes, particularly Auto-Discon-
nect with the IBM 3976-2 Modem and the circuits for
generating and printing the slash (/) instead of the
dash (-). These two changes are described and
illustrated here.

Auto-Disconnect With IBM 3976-2 Modem

- Causes for disconnect:
  (a) No bid within 15 seconds after connection.
  (b) No character sent within 15- to 30-second
    period.
  (c) No character received within 15-second
    period.
  (d) No bid within 15 seconds after EOT.
  (e) Out of paper.
  (f) Data set (modem) not operational.
  (g) Manual disconnect by either operator.

- Indications of disconnect:

  NOTE: (a) and (b) do not happen when the
  data set (modem) becomes not operational.

  (a) Transmit and Receive lights on, Dial Con-
    nect light off.
  (b) Bell sounds once.
  (c) Modem "Data" light off.

A dialed connection establishes communication
between two terminals, as though on a leased line,
until disconnected. Disconnection occurs when the
Dial Disconnect key is pressed, by loss of terminal
status, by not following EOT with a bid, or by failure
of the sending terminal to maintain carrier and a
stream of transmitted characters. All disconnects
except Dial Disconnect key depression or loss of
status occur only after a 15-second waiting period
has timed out. The delay is controlled by a 15-
second timer and a latch.

Once a connection is completed, the 15-second
timer and 'time-out 15' latch will respond to any one
of several potential reasons for disconnection
(Figure C-1), if it continues uninterrupted for 15
seconds. These are:
1. Data set capable of data operation (ready) but
   no carrier present (AA431 and BB291).
2. No character being sent (mainly 'send' and '1B
   empty', AA311).
3. No character being received (AA431--'data set
   ready', 'not send', and 'not inhibit time-out'.

The 'inhibit time-out' trigger turns on only for
good-parity characters with S∅.)

NOTE: Since the 15-second time delay is a
leading edge delay, only, there is no carryover from
one timing period to another. If carrier has been off
and momentarily comes on again, or if a character
is sent or received, the 'TO15' latch and the 15-
second timer are reset. A new 15-second timeout
period begins.
When a connection is made and neither terminal
bids for the line, timeout for auto-disconnect occurs
because no character has been sent or received. The
garble timeout (BB101) is not present in dial-up
machines.

When a reason for disconnecting prevails for 15
seconds and the 'TO15' latch turns on, the 'dial dis-
connect' latch turns on. Timeout, with 'not-send
(receive)' or 'not-carrier', sets the 'dial disconnect'
latch. Operator-initiated disconnect (dial disconnect
key) also turns on the 'dial disconnect' latch and
works like auto-disconnect throughout the remainder
of disconnect circuit operation. The 'dial discon-
nect' latch resets when disconnection is accom-
plished and the data set becomes not-ready.
Dial disconnect not only signals the 3976-2 to
disconnect (by dropping the 'data terminal ready'
line, Figure C-1), but also turns on the 'auto-
disconnect indicate' latch. The disconnect operation
turns off carrier (if it is not already off), the trans-
mit and receive lights turn on, and the bell sounds
once. The intended method of resetting these indica-
tions of auto-disconnect is to press the EOT key.
Machine operation is normal if this is done. If the
'dial disconnect indicate' latch remains on because
EOT has not been pressed, a new connection can
still be dialed. Carrier comes on and turns out the
lights, but a momentary loss of carrier during the
new connection will flash the lights and sound the
bell without actually disconnecting.
Notice that loss of status also causes disconnec-
tion. This occurs without the 15-second timeout, and
is caused by running out of paper or loss of data set
readiness (Figure C-1). Disconnection caused by
data set not ready does not turn on the lights or
sound the bell.
To summarize, a disconnect may occur because
of loss of carrier, failure to send characters often
enough or soon enough, operator pressing the dial
disconnect key, a terminal running out of paper, or
a modem becoming non-operational. In each case,
except the last, the transmit and receive lights come

on and the bell sounds once. The proper method of turning off the lights is to press the EOT key. Then a new connection can be dialed and normal operation resumed. The 'TO15' and 'dial disconnect' latches reset automatically, and the 'auto disconnect indicate' latch is reset manually.

Generate and Print the Slash (/)

- Incorrect case error prints " / ". World Trade circuits pick T2, R1, R2, R2A, and R5 for " / ".

- LRC error prints " / ".

- 2B overflow prints " / ".

- Receiving error prints " / ".

- Domestic 2740 circuits set 2B1 for " - ". Added World Trade circuits reset 2B1 and set 2B2, 2B6, and 2B7 for " / ".

The " / " that prints in place of the " - " is generated as described earlier in this manual. The modification necessary for World Trade is to clear from 2B the domestic code for " - " (2B1) and insert in its place the World Trade code for " / " (2B2, 2B6, and 2B7). Since all errors except incorrect case are detected before print time, this can be done as shown in Figure C-2.

The incorrect case error, which can be detected only after the previous printout operation is complete, does not allow time to insert the " / " in 2B before printing. Instead, tilt and rotate for the " / " are generated directly in the print decoding circuits and shifting is inhibited (Figure C-2). World Trade machines use print decoding circuits that provide the correct tilt and rotate; that is, T2, R1, R2, R2A, and R5.

Figure C-1. Disconnect Logic

Figure C-2. Error Print Logic

Added mechanisms in the I/O printer provide for front-insertion and independent spacing of the ledger card. A manually-operated guide chute lowers to direct the ledger card under and around the platen from the front. This releases the feedrolls automatically. When returned to the raised position, the guide holds the card against the platen in the printing area and automatically raises the feedrolls. The platen can be split manually by pulling to the left on the left-hand platen knob. When the platen is split, the left platen section does not rotate, but the right section can be rotated in the usual ways. The platen vernier is released by the right-hand platen knob on the Split Platen.

DOCUMENT INSERTION MECHANISM

Document Insertion Guide Assembly

- Swings forward and down when released.

- Attached to hollow paper bail shaft.

- Document guide lower link operates document insertion switch via paper bail center shaft.

The document insertion guide (Figure D-1) is attached to the paper bail shaft. The shaft is in two concentric parts; the hollow shaft carries the paper bail rolls and the insertion guide mounts, the center
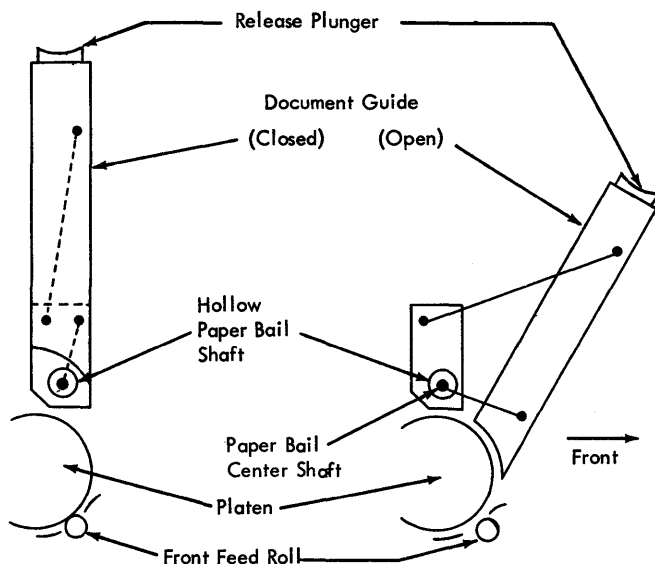
Figure D-1. Schematic of Document Guide Mechanism

shaft operates the document insertion switch (Figures D-2 and D-3). Press down on the plunger and swing the guide forward and down for document insertion (Figure D-1).

Lowering the document guide automatically lowers the feedrolls and positions the guide so that an inserted document passes between the feedrolls and the platen from the front. The document insertion switch transfers as the guide opens, which activates the terminal circuits that cause the feedroll lowering mechanism to operate (Diagram 5-46).

Closing the document guide retains the card in position for printing and automatically raises the feedrolls. Again, it is the document insertion switch that begins the operation of raising the feedrolls against the card and platen.

Split Platen Assembly

- Designed for dual-document use.

- Allows independent spacing of right-hand document.

- Keyboard locks when platen is split and ledger card inserted.

The Split Platen is a two-section platen that facilitates dual-document printing. The main purpose is to allow independent line-spacing of the right-hand document, controlled by the central processor. The left knob is pulled out to split the platen, and pushed in to re-join it. The right knob operates the conventional platen vernier.

The left (platen split) pushrod (Figure D-4) detents in two positions. As it moves from one position to the other, it moves the shift collar and left section driver laterally. The pins that connect these parts move through slots in the hollow platen shaft. The ball bearing causes the locking clutch to move laterally, and also allows independent rotation of the locking clutch and the shift collar.

With the pushrod detented to the left (as shown Figure D-4), the locking clutch (which is engaged with the left platen section) meshes with the stationary left platen bearing. This holds the left platen section stationary, but allows the platen shaft to rotate. The right platen section and the index ratchet are disengaged only by the platen vernier, so an indexing operation line-spaces the right-hand document.

With the pushrod detented to the right, the locking clutch unmeshes from the left platen bearing and the left section driver meshes with the left platen section. Now, an indexing operation rotates the platen shaft and line-spaces both platen sections.

FEEDROLL LOWERING MECHANISM

● Feedrolls drop to allow document insertion.

● Feedrolls raise to hold inserted document for printing.

● Document brake holds journal paper during document insertion.

● Clutch-controlled cam operates feedroll mechanism.

● Magnet-controlled latch acts as an interposer to hold feedrolls in raised position.
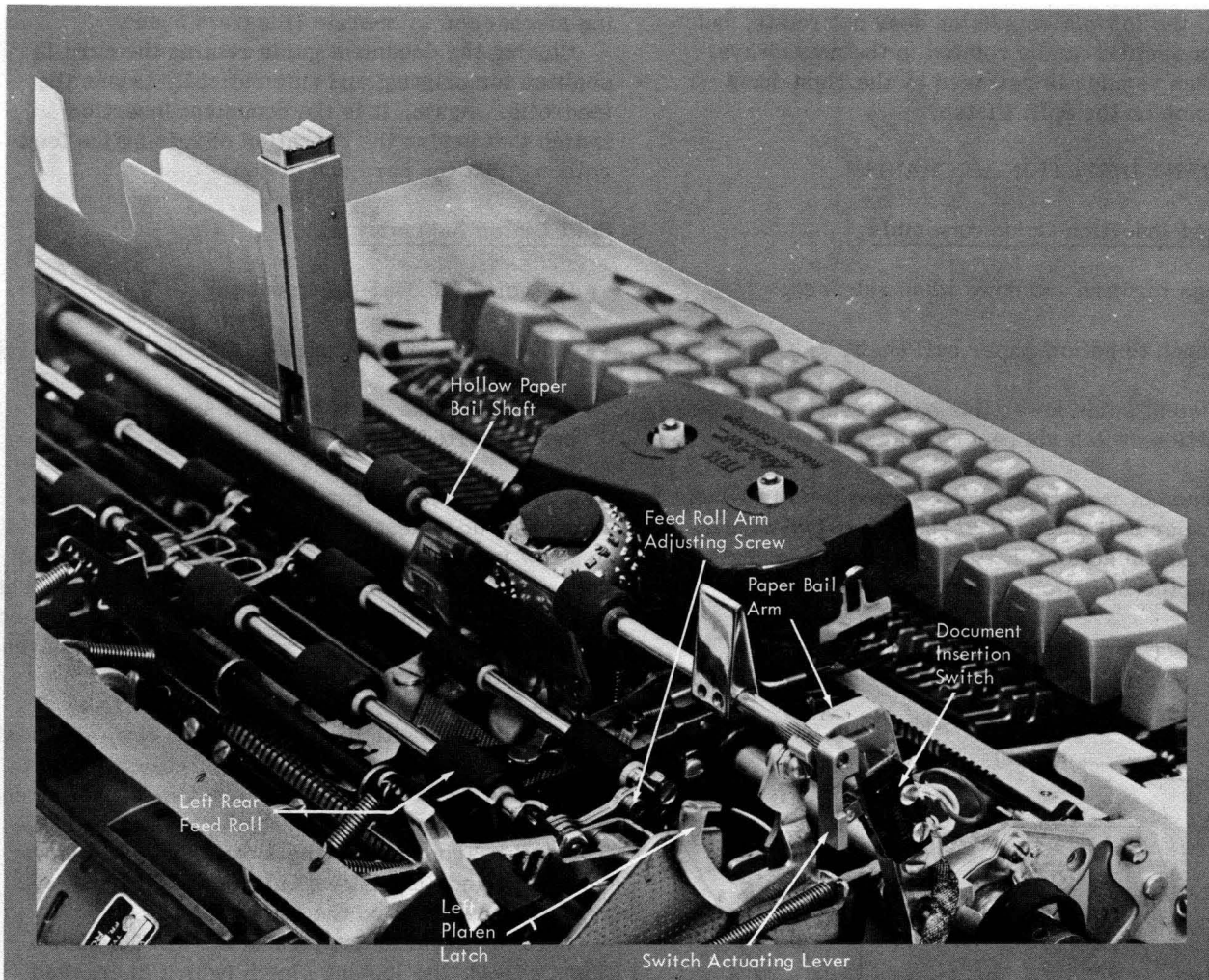
Figure D-2. Document Insertion Guide Closed

Cam Cycle Assembly

● Operates to lower or raise the feedrolls.

● The cam cycles when the document insertion guide is opened or closed.

● The feedroll cam follower operates the feedroll tension spring bail.

Figure D-5 shows the feedrolls in the normal, raised position. In this position, the feedroll tension springs, through linkage, press the feedrolls against the platen. Manual feedroll release rotates the feedroll arm shaft, stretching the tension springs and lowering the feedrolls. Automatic feedroll lowering relaxes the tension springs by rotating the spring bail, thus allowing the feedrolls to drop.
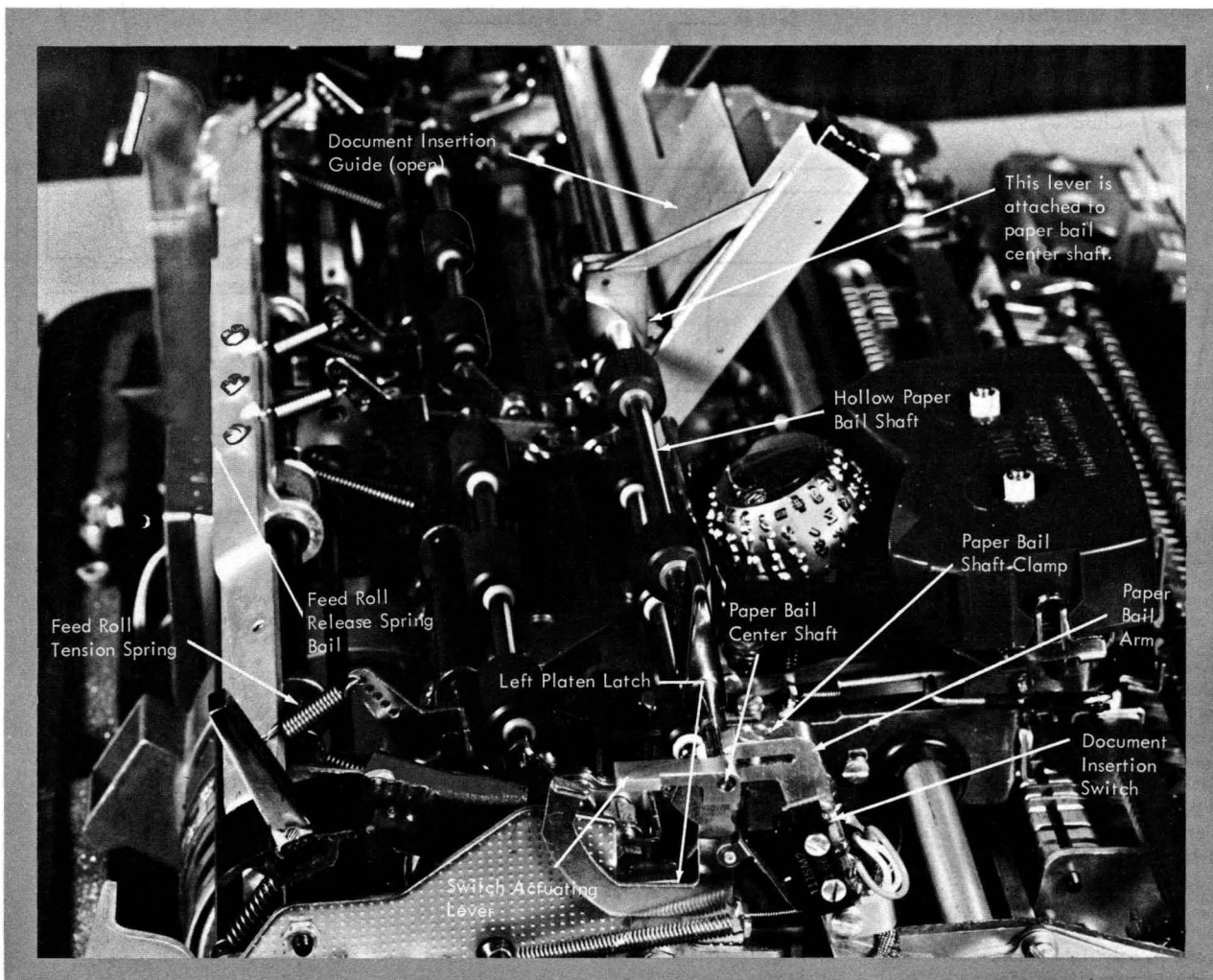
Figure D-3. Document Insertion Guide Open

In Figure D-5, assume that the feedroll cam takes a 360° cycle. (The feedroll cam clutch, Figure D-6 , is a conventional assembly and is similar to the other operational cams.) As the cam rotates, it operates the follower slightly. This stretches the tension springs a little as the pushrod moves upward. The latch, now free of pressure, can be withdrawn while the cam follower supports the pushrod. As

the cam continues to rotate, the cam follower rides the surface of the cam until the pushrod comes to rest against the power frame base. As the pushrod moves down, the spring bail rotates, the springs relax, and the feedrolls drop away from the platen. As the feedrolls drop, a rubber-tipped stop rises to press the journal paper (left-hand document)
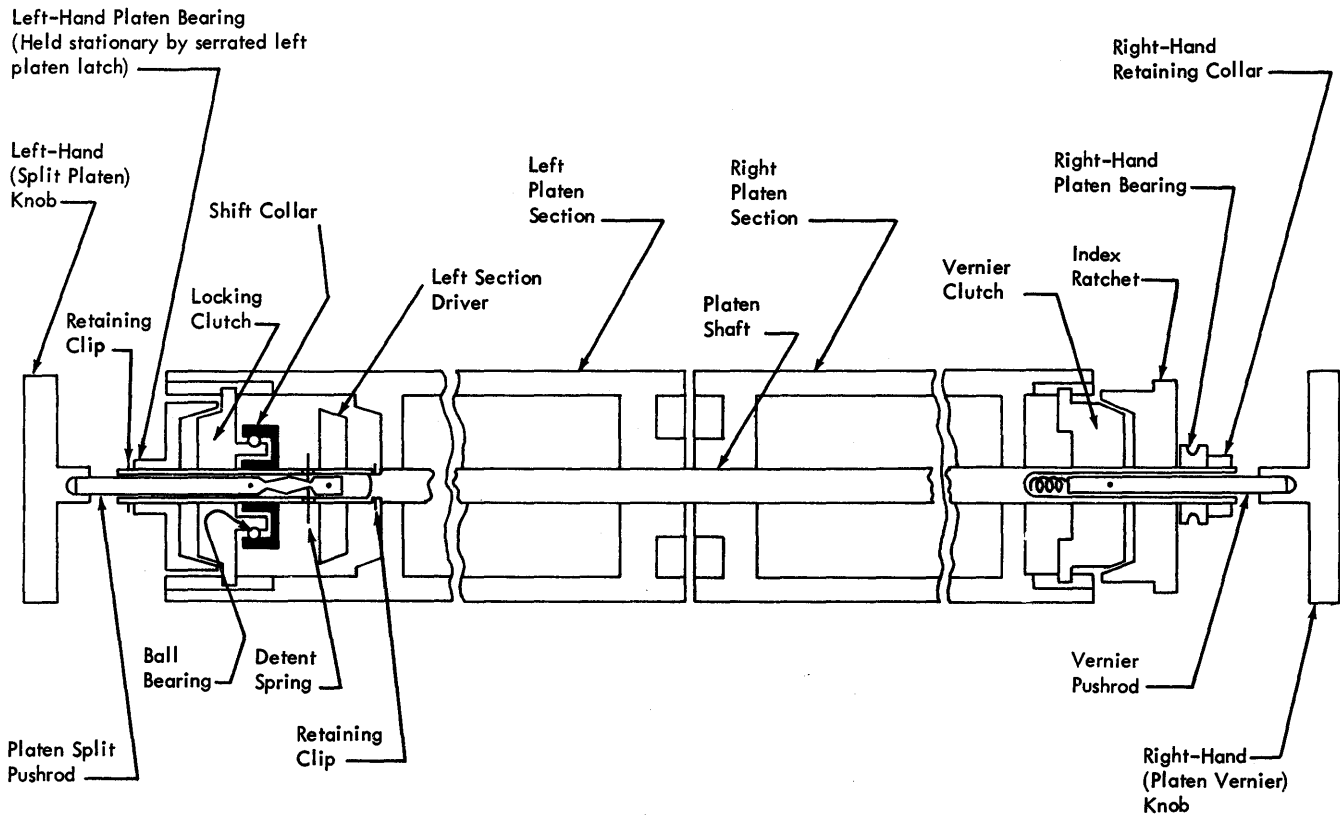
Always rotates with platen shaft:
  Platen knobs and pushrods
  Shift collar
  Left section driver
  Detent spring
  Right platen section
  Vernier clutch
  Right-hand retaining collar

Stationary with platen split:
  Left-hand platen bearing
  Locking clutch
  Left platen section

Note:
  Vernier affects only right platen section when platen is split. This drawing shows the platen split.

Figure D-4. Cross Section of Split Platen

against the platen and hold it in proper printing position. The cam completes its cycle with the latch out and the feedrolls lowered.

To raise the feedrolls, the cam takes another 360° cycle. The cam follower raises the pushrod, rotates the spring bail, places tension on the springs, raises the feedrolls against the platen, and lowers the journal stop. The latch slides into place under the pushrod and the cam follower lowers the pushrod onto the latch. The cam follower comes to reset, and the cam completes its cycle to the position illustrated in Figure D-5.

Refer to Figures D-6 (near right end of operational shaft) and D-7 (right rear corner) for photographs of feedroll lowering mechanism components in the I/O printer. Notice the cam release magnet position and the link to the release arm. Also note the latch, pushrod, and spring bail.

Latch Assembly

● Controlled by magnet on right side of keyboard.

● Latch in: feedrolls up; latch not in: feedrolls down.

The feedroll latch acts as an interposer under the pushrod, to hold the feedrolls up against the platen. When the feedroll cam follower raises the pushrod off the latch, the energized feedroll latch magnet can move the latch out from under the pushrod. The armature attracts, the bellcrank rotates, and the long link (Figure D-5) moves the latch aside. The bellcrank also operates the latch switch (Figure D-8) which signals terminal logic when the latch is in (under the pushrod). Refer to Figure D-7 for a photograph of the latch under the pushrod. As seen in this photograph, the latch rotates clockwise to move out from under the pushrod. Obviously, then, the schematic (Figure D-5) does not show the actual movement. The effect is the same, however.

● Stationary pivot
o Moving pivot
→ Direction of Motion to lower

Figure D-5. Schematic Feedroll Lowering Mechanism
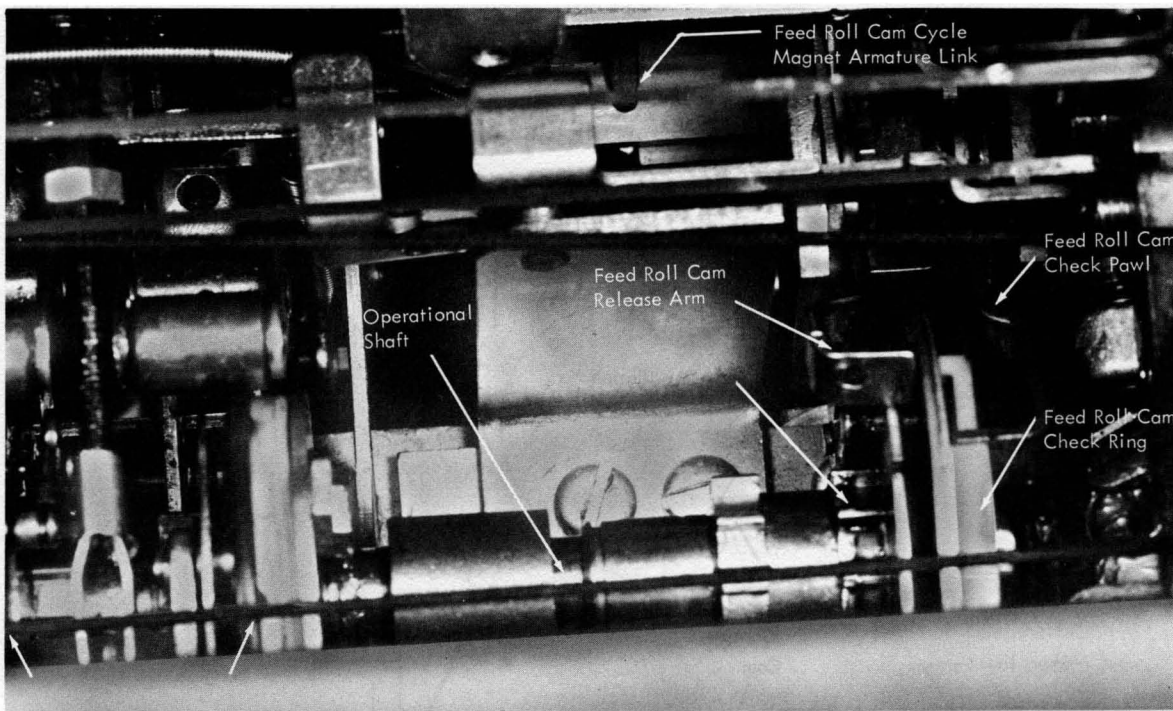
Figure D-6. Feedroll Cam and Clutch
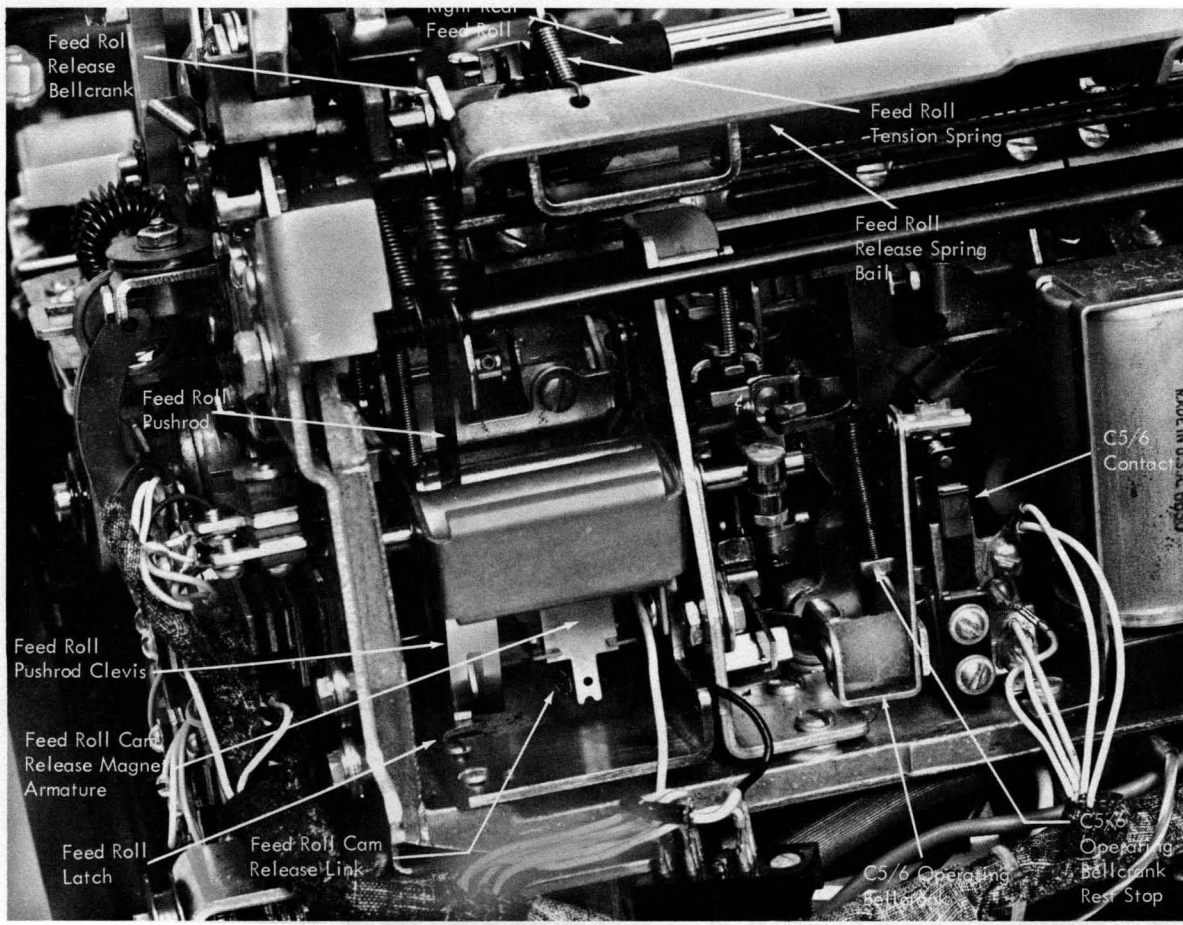
Figure D-7. Feedroll Cam Magnet and Feedroll Latch

Feed Roll Latch Magnet Armature Link

Feed Roll Latch Bellcrank

Feed Roll Latch Switch

Upper Case Magnet

Feed Roll Latch Magnet

Feed Roll Latch Long Link Clevis
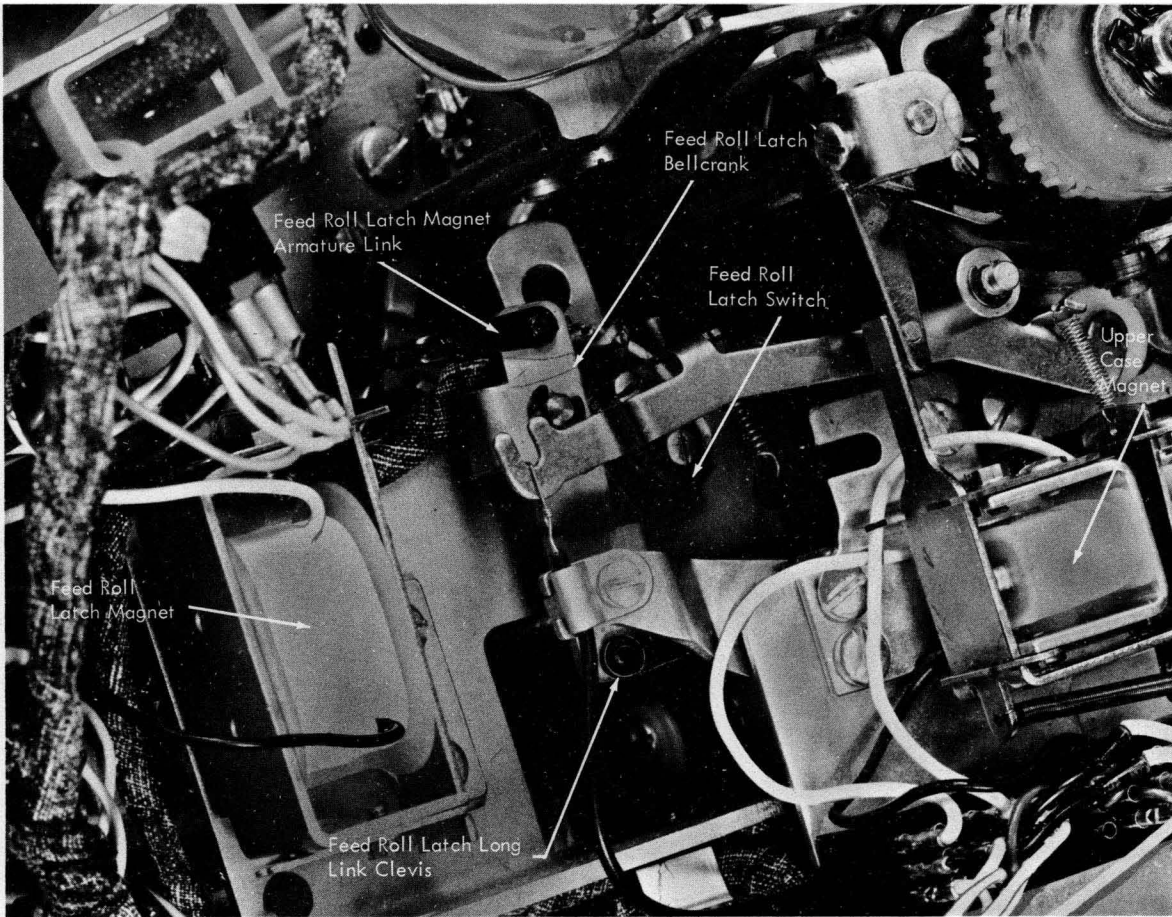
Figure D-8. Feedroll Latch Magnet

VERTICAL REDUNDANCY CHECK ONLY (RPQ 858083)

● Checks parity (VRC) of each transmitted and received character.
● No LRC checking.

● Prints a hyphen (-) to indicate an error.

The 2740-2 Record-Checking feature (described in Chapter 4, Section 1) provides for both vertical and longitudinal redundancy checks (VRC and LRC) with an answerback after each EOB-LRC transmitted. If desired, RPQ 858083 provides for VRC only (parity check without LRC). With this RPQ installed, the terminal operates similar to a 1971 terminal. The answerback (after EOB) indicates whether a parity error existed in the transmitted message and a hyphen (-) is printed to indicate any VRC error.

Removal of the 2740-2 Record Checking feature is prerequisite.

VRC Only (WTC)

● Checks for parity error only.

● Prints slash (/) to indicate an error.

The RPQ described above provides for "VRC only" for WTC terminals also. The only difference is the WTC terminal prints a slash (/) instead of a hyphen (-) to indicate a parity error.

950 BAUD (RPQ 858092)

● Receive and Transmit at 950 bps (105.5 cps)

The 950 baud RPQ equips the terminal with a faster oscillator to increase the line speed to 105.5 characters per second.

The terminals having this RPQ installed will operate only with a WE202D data set.

The Buffered Receive feature is a prerequisite.

NEGATIVE ANSWERBACK OVERRIDE (RPQ 858084)

● Allows status answerback without paper in the terminal I/O printer.

● Special addressing sequence used (ⒸＣ , ⒮Ｓ , terminal identification, and idle character).

Installation of the "negative answerback override RPQ" allows the use of a special addressing sequence (ⒸＣ , ⒮Ｓ , terminal identification, and idle or invalid character) to bring up status without paper in the I/O printer.

When the special addressing sequence is used for a master terminal, the idle (invalid) character is used with 'control address selected' mode to satisfy conditions to turn on the 'paper switch cheater' latch (ALD BB301). The output of this latch brings up the 'paper-X' line and turns on the 'space' latch. Status is brought up and the output of the 'space' latch is treated as a space in the addressing sequence. Thus, a master terminal goes to transmit status answerback mode and transmits a 2 character answerback (qualified Ⓨ) to allow the system to proceed.

Slave terminals in 'control address' mode with 'not message' bring up 'paper' to allow the terminal to go to control address selected slave mode. 'Control address selected' with 'space' and 'not B' bring up 'E set gate' to place the terminal in control selected slave mode.

The special addressing sequence is used at the option of the programmer, possibly after the first normal addressing sequence received a negative response.

There are no prerequisites for this RPQ.

RETRANSMIT ONCE RECEIVE CHECK ANSWERBACK (RPQ 858095)

● Turn on 'retransmit' latch with first transmission.

● A Ⓨ answerback returns the terminal to transmit text mode.

- A $\widehat{N}$ answerback (after first transmission) returns the terminal to transmit text to retransmit message.

- A second $\widehat{N}$ answerback causes the Reset light to turn on, the alarm to ring, and the terminal to be placed in control receive mode.

- A $\widehat{C}$ answerback for either transmission causes the Reset light to turn on, the alarm to ring and the terminal to return to control receive mode.

The 'retransmit' latch is turned on with the transmission of the first message. After transmission of the message, the terminal goes to receive check answerback mode. In this mode, a character is received from the central processor to indicate if the message was received correctly. If so, the terminal receives a $\widehat{Y}$ for an answerback, returns to transmit text mode, transmits a $\widehat{C}$, and goes to control receive mode.

answerback, returns to transmit text mode, transmits a $\widehat{C}$, and goes to control receive mode.

If the message was not received correctly at the central processor, it returns a $\widehat{N}$ character. This causes the terminal to return to transmit text, retransmit the message, and turn off the retransmit latch. If the message is again received in error, the central processor again returns a $\widehat{N}$, which with 'not retransmit' causes the terminal to return to transmit text mode, transmit a $\widehat{C}$, indicate an error (ring alarm, turn on Reset light) and then go into control receive mode. The central processor can be programmed to return a $\widehat{C}$ as the answerback following either transmission to place the terminal in control receive mode after indicating an error by turning on Reset light and ringing the alarm.

The prerequisite for the Retransmit Once RPQ is the Record Checking Feature (regular or VRC only).

For a more detailed description of "Receive Check Answerback" refer to Chapter 4, Section 1.

ERROR-RECOVERY PROCEDURES

The charts in Tables 1 through 7 illustrate various error conditions. They indicate the line response (if any), the indicator(s) turned on, and the procedure for recovery.

1. Receive Operation--without Record Checking
2. Receive Operation--with Record Checking
3. Transmit Operation--Buffer to Communications Line
4. Enter Status--Local or Communicate Mode
5. Buffer Printout--Local Mode
6. Terminal Addressed by CPU
7. Terminal Polled by CPU

Table F-1. Receive Operation--without Record Checking Feature

Type of Error	Buffered Receive	Indicator	Terminal Response to next Add. Seq.	Recovery
Buffer print parity error.	Yes	Reset light ON, character may or may not be printed, and alarm sounds.	/ (Y)	Send message to request retransmission.
Incorrect case. Detected during buffer print.	Yes	Printed hyphen.	None	
Buffer overflow.	Yes	Garbles message. (At 600 or 950 BAUD the operator may not see the Reset light.)	None	
Lose forms while receiving from line.*	With or Without	Receive light turns OFF and Standby light fails to turn ON.	9 (N)	Insert forms and send message to request retransmission.
Lose forms while printing out from buffer.*	Yes	Standby light fails to turn ON after message is printed out.	9 (N)	
Incorrect case.	No	Print hyphen. Reset light ON until (C) is received.	None	Send message to request retransmission
Overflow printer.	No	Characters omitted. Reset light ON until (C) is received.	None	
Receive parity error.	With or Without	Parity light on. Reset light ON until (C) is received.	U (Y)	Press parity reset switch. Send message to request retransmission.

* Forms must be missing when the terminal is addressed for 9 (N) response.

Table F-2. Receive Operation--with Record Checking Feature

Type of Error	Buffered Receive	Indicator	Terminal Response To EOB-LRC	To next Add. Seq.	Recovery
Parity error.	Yes	Reset light ON until response is sent. Line Parity light ON. Insert hyphen in buffer. Message will not buffer print.	(N)	U (Y)	CPU retransmits message.
No stop bit.					
LRC error.	Yes	Reset light ON until response is sent. Message will not buffer print.	(N)		
Parity error.	No	Line Parity light ON. Reset light ON until response is sent. Print hyphen.	(N)	U (Y)	CPU retransmits message.
No stop bit.					
LRC error.	No	Reset light ON until response is sent.	(N)		
Lose forms while receiving data from line. *	With or Without	Receive light turns OFF and Standby light fails to turn ON.	None (CPU times out)	9 (N)	Insert forms. Post conditions to user.
Lose forms while printing out from buffer. *	Yes	Standby light fails to turn ON after message has printed out.	None	9 (N)	Insert forms and send message to request retransmission.
Buffer overflow.	Yes	Message will not buffer print. Reset light ON until turned off by (C) answerback. (The operator may not see the light.)	(C)	None	Post error message to user.
Overflow printer.	No	Reset light ON. Characters omitted and hyphen printed at LRC check.	(C)	None	Post error message to user.
Buffer parity error while printing out message.	Yes	Reset light ON. Alarm sounds. Character may or may not be printed.	None	/ (Y)	Press Reset key. Send error message to CPU.
Incorrect case (detect during print-out).	Yes	Print hyphen.	None	None	Send error message to CPU.
Incorrect case.	No	Print hyphen. Reset light ON (turned off by (C) answerback).	(C)	None	Post error message to user.
Buffer error while receiving.	Yes	Reset light ON until reset by (N) response. Message will not buffer print.	(N)	/ (Y)	CPU retransmits message.
Receive parity error.	With or Without	Parity light ON. Reset light ON until response is sent.	(N) **	U (Y)	Press parity reset switch to turn off parity light.
I/O Error while printing.	Without	Reset light ON.	(N)	S (Y)	CPU retransmits message.

* Forms must be missing when the terminal addressed for 9 (N) response.
** The same conditions that set the 'receive parity error' latch also set the 'error' trigger.

Table F-3. Transmit Operation--Buffer to Communications Line

Type of Error	Record Checking	Indicator	Response from CPU	Term. Response to next Add.		Recovery
Buffer VRC error.	Yes	Reset light ON. Alarm sounds.	(N) or (C)	Y	(Y) *	Press Local switch. Press Reset key. Rekey message.
Buffer VRC error.	No	Reset light ON. Alarm sounds.	None	Y	(Y) *	Press Local switch. Press Reset key. Rekey message. Post system error to user.
No error detected in 2740.	Yes	None	(N) or garbles answerback	Space	(Y)	Automatic retransmission of message.
		Alarm sounds. Reset light ON.	(C)	Space	(Y)	Press Reset key, press Bid key, and wait to be polled.
		Reset light ON and Receive light ON.	No response	Space	(Y)	Press Local switch, then Reset key, and switch back to communicate mode.
Transmit parity error.	No	Parity light ON.	None	Y	(Y)	Press parity reset switch to turn off the parity light.
Transmit parity error.	Yes	Parity light ON	(N)	Y	(Y)	Press parity reset. Message retransmission is automatic.

*Note: Buffer VRC error should also cause a transmit parity error which will force a Y (Y) response.

Table F-4. Enter Status--Local or Communicate Mode

Type of Error	Indicator	Recovery
Buffer parity error.	Reset light ON. Keyboard locked. Alarm sounds	Press Reset key, press Enter key, and rekey message.
Buffer overflow.	Alarm sounds eight characters before end of buffer, and keyboard locks at end of buffer.	Message can be sent as is, or press Reset and Enter keys to reload message.
Lose forms while entering data.	None.	Load forms if hard copy is desired.
No forms.	Enter light fails to turn ON when Enter key is pressed.	Load forms.

Table F-5. Buffer Printout--Local Mode

Type of Error	Indicator	Recovery
Buffer parity error.	Reset light ON and keyboard locked. Alarm sounds.	Press Reset key, press Enter key, and rekey message.
Incorrect case.	Print hyphen.	Use backspace or edit keys, or rekey message.

Table F-6. Status/Answerback when Terminal with Receive Status is Addressed by CPU

Terminal Condition	Buffered Receive	Terminal Response*	Recovery Procedure
No Error Stored	With or Without	Space ⓨ	None required
Electronic hardware error on last message	With	/ ⓨ	Note: When messages are received in error by terminals without Record Checking, the CPU is not informed. However, at the option of the program, the previous message may be retransmitted upon receipt of the addressing response.
I/O Error on last message received	With or Without**	S ⓨ	
Line VRC error during last message received	With or Without	U ⓨ	
Terminal induced VRC error during a transmitted message	With or Without	Y ⓨ	Message retransmitted at the programs option.

Note: *The qualified ⓨ response to the CPU is intended for condition statistics. All of the first characters except space should be stored or printed for error analysis.
  **Without Buffered Receive Feature a parity error in the 1B or 2B register will cause the I/O error latch to be set.

Table F-7. Status/Answerback when Terminal without Receive Status is Addressed by CPU

Terminal Status	See Note	Indication at Terminal	Terminal Response	Recovery Procedure
Bid Latch is on	*	Attention light on	2 Ⓝ	Wait to be polled or go to local mode and press Reset key.
In Enter while in Communicate mode	*		1 Ⓝ	Complete entering, press Bid key and wait to be polled or press Reset key
Buffer print in Communicate mode	*		4 Ⓝ	
In Local mode	**	Gaining status will turn off attention light	8 Ⓝ	Switch to Communicate mode.
Ready except out of paper	**		9 Ⓝ	Load paper
Ready except document device is down	**		@ Ⓝ	Raise document device
No power on terminal or data set		None	None (CPU times out)	Turn power on. CPU should post error condition to user.

Note: *Should be considered status or buffer busy conditions. Program should go to other business and also poll the terminal before re-addressing for bid, or enter in communicate mode.
  ** Should be considered as operator errors. Program should retry twice and then post an error condition to user.

Table F-8. Terminal Polled by CPU

Terminal Status	Terminal Response to Poll	Recovery
Enter or buffer print.	Ⓝ	For Enter Mode, Press Communicate switch, press Bid key, and wait to be polled. Normal condition. System should continue polling.
Not in communicate mode.	Ⓝ	Press Enter key and key message. Press Communicate switch. Press Bid key and wait to be polled. Normal condition. System should continue polling.
Bid key not operated.	Ⓝ	Press Communicate switch. Press Bid key if message has been entered. Normal condition. System should continue polling.
No power on terminal or data set	None	Turn power on. System should repoll twice. After second retry, post condition to user (what the condition is and when it occurred).

2740 Communication Terminal Model 1
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Theory of Operation

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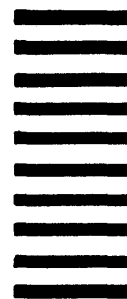
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