IBM Field Engineering Handbook

IBM Confidential

System/360, General Section

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Third Edition
This edition, Z22-2851-2, is a revision of Z22-2851-1, which it obsoletes.

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CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power AC and DC when removing or assembling major components, working in immediate area of power supplies, performing mechanical inspection of power supplies and installing changes in machine circuitry.
3. Wall box power switch when turned off should be locked or tagged in off position. "Do not Operate" tags, form 229-1266, affixed when applicable. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, the following precautions must be followed:
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Rings, wrist watches, chains, bracelets, metal cuff links, shall not be worn.
   c. Only insulated pliers and screwdrivers shall be used.
   d. Keep one hand in pocket.
   e. When using test instruments be certain controls are set correctly and proper capacity, insulated probes are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc. — use suitable rubber mats purchased locally if necessary).
5. Safety Glasses must be worn when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Parts cleaning, using solvents, sprays, cleaners, chemicals, etc.
   f. All other conditions that may be hazardous to your eyes. REMEMBER, THEY ARE **YOUR** EYES.
6. Special safety instructions such as handling Cathode Ray Tubes and extreme high voltages, must be followed as outlined in CEM's and Safety Section of the Maintenance Manuals.
7. Do not use solvents, chemicals, greases or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Lift by standing or pushing up with stronger leg muscles — this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
11. All safety devices such as guards, shields, signs, ground wires, etc. shall be restored after maintenance.

KNOWING SAFETY RULES IS NOT ENOUGH
AN UNSAFE ACT WILL INEVITABLY LEAD TO AN ACCIDENT
USE GOOD JUDGMENT — ELIMINATE UNSAFE ACTS

229-1264-1

12. Each Customer Engineer is responsible to be certain that no action on his part renders product unsafe or exposes hazards to customer personnel.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. All machine covers must be in place before machine is returned to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it (i.e., under desk or table).
16. Avoid touching mechanical moving parts (i.e., when lubricating, checking for play, etc.).
17. When using stroboscope — do not touch ANYTHING — it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CE's and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machines while performing and after completing maintenance.

Artificial Respiration

GENERAL CONSIDERATIONS

1. **Start Immediately, Seconds Count**
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim or apply stimulants.
2. **Check Mouth for Obstructions**
   Remove foreign objects — Pull tongue forward.
3. **Loosen Clothing — Keep Warm**
   Take care of these items after victim is breathing by himself or when help is available.
4. **Remain in Position**
   After victim revives, be ready to resume respiration if necessary.
5. **Call a Doctor**
   Have someone summon medical aid.
6. **Don't Give Up**
   Continue without interruption until victim is breathing without help or is certainly dead.

Reprint Courtesy Mine Safety Appliances Co.

Rescue Breathing for Adults
Victim on His Back Immediately

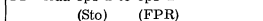
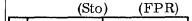
1. **Clear throat** of water, food, or foreign matter.
2. **Tilt head back** to open air passage.
3. **Lift jaw up** to keep tongue out of air passage.
4. **Pinch nostrils** to prevent air leakage when you blow.
5. **Blow** until you see chest rise.
6. **Remove your lips** and allow lungs to empty.
7. **Listen** for snoring and gurglings, signs of throat obstruction.
8. **Repeat mouth to mouth breathings** 10-20 times a minute.

Continue rescue breathing until he breathes for himself.

Thumb and finger positions

Final mouth to mouth position

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Add	A	5A	RX	R1, R2	Add opr 2 to opr 1 (Sto) (GPR)	Adr Spec Exp Oflo	0 Sum = 0 1 Sum < 0 2 Sum > 0 3 Overflow
Add	AR	1A	RR	R1, R2	Add opr 2 to opr 1 (GPR) (GPR)	Exp Oflo	0 Sum = 0 1 Sum < 0 2 Sum > 0 3 Overflow
Add Decimal	AP	FA	SS	D1, (L1, B1), D2(L2, B2)	Add dec opr 2 to opr 1 (Sto) (Sto) (Right to left byte by byte) (Opr 1 and 2 must be in packed) (Fields can overlap if low-order bytes coincide) (If opr 1 and opr 2 refer to same field, the field is doubled)	Prot Adr Data Dec Oflo	0 Sum = 0 1 Sum < 0 2 Sum > 0 3 Overflow
Add Halfword	AH	4A	RX	R1, D2(X2, B2)	Add opr 2 to opr 1 (Sto) (GPR) (High-order 16 bits expanded) opr 2	Adr Spec Exp Oflo	0 Sum = 0 1 Sum < 0 2 Sum > 0 3 Overflow
Add Logical	AL	5E	RX	R1, D2(X2, B2)	Add log opr 2 to opr 1 (Sto) (GPR)	Adr Spec	0 Sum = 0 1 Sum ≠ 0 2 Sum = 0 3 Sum ≠ 0
Add Logical	ALR	1E	RR	R1, R2	Add log opr 2 to opr 1 (GPR) (GPR)		0 Sum = 0 1 Sum ≠ 0 2 Sum = 0 3 Sum ≠ 0

Add Normalized (Long)	AD	6A	RX	R1, D2(X2, B2)	FP Add opr 2 to opr 1 (Sto) (FPR)  	Adr Spec Sign Exp Oflo Exp Uflo	0 Fract = 0 1 Fract < 0 2 Fract > 0 3 Exp Oflo
Add Normalized (Long)	ADR	2A	RR	R1, R2	FP Add opr 2 to opr 1 (FPR) (FPR)	Spec Sign Exp Oflo Exp Uflo	0 Fract = 0 1 Fract < 0 2 Fract > 0 3 Exp Oflo
Add Normalized (Short)	AE	7A	RX	R1, D2(X2, B2)	FP Add opr 2 to opr 1 (Sto) (FPR)  (Low-order FPR ignored and unchanged)	Adr Spec Sign Exp Oflo Exp Uflo	0 Fract = 0 1 Fract < 0 2 Fract > 0 3 Exp Oflo
Add Normalized (Short)	AER	3A	RR	R1, R2	FP Add opr 2 to opr 1 (FPR) (FPR)	Spec Sign Exp Oflo Exp Uflo	0 Fract = 0 1 Fract < 0 2 Fract > 0 3 Exp Oflo
Add Unnormalized (Long)	AW	6E	RX	R1, D2(X2, B2)	FP Add opr 2 to opr 1 (Sto) (FPR)	Adr Spec Sign Exp Oflo	0 Fract = 0 1 Fract < 0 2 Fract > 0 3 Exp Oflo
Add Unnormalized (Long)	AWR	2E	RR	R1, R2	FP Add opr 2 to opr 1 (FPR) (FPR)	Spec Sign Exp Oflo	0 Fract = 0 1 Fract < 0 2 Fract > 0 3 Exp Oflo
Add Unnormalized (Short)	AU	7E	RX	R1, D2(X2, B2)	FP Add opr 2 to opr 1 (Sto) (FPR) (Low-order FPR ignored and unchanged)	Adr Spec Sign Exp Oflo	0 Fract = 0 1 Fract < 0 2 Fract > 0 3 Exp Oflo

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Add Unnormalized (Short)	AUR	3E	RR	R1, R2	FP Add opr 2 to opr 1 (FPR) (FPR)	Spec Sign Exp Oflo	0 Fract = 0 1 Fract < 0 2 Fract > 0 3 Exp Oflo
AND	N	54	RX	R1, D2(X2, B2)	Place the product of both opr's into opr 1	Adr Spec	0 Result = 0 1 Result ≠ 0
AND	NC	D4	SS	D1(L, B1), D2(B2)	Place the product of both opr's into opr 1 (Left to right byte by byte) (Max number of bytes ANDed: 256)	Prot Adr	0 Result = 0 1 Result ≠ 0
AND	NR	14	RR	R1, R2	Place the product of both opr's into opr 1	None	0 Result = 0 1 Result ≠ 0
AND	NI	94	SI	D1(B1), I2	AND the 1 byte from the instruction stream (8-15) to opr 2	Prot Adr	0 Result = 0 1 Result ≠ 0
Branch and Link	BAL	45	RX	R1, D2(X2, B2)	Store PSW 32-63 into opr 1 Branch to adr of opr 2 (If opr 2 = 0) Store • $\overline{\text{Branch}}$	None	Unchanged
Branch and Link	BALR	05	RR	R1, R2	Store PSW 32-63 in opr 1 Branch to adr of opr 2 (If opr 2 = 0) Store • $\overline{\text{Branch}}$	None	Unchanged
Branch on Condition	BC	47	RX	M1, D2(X2, B2)	Compare opr 1 with cond code (Mask) 8-11 (Mask = 7) Branch on non-zero (Mask = 15) Uncond branch (Mask = 8) Cond code 00 (Mask = 4) Cond code 01 (Mask = 2) Cond code 10 (Mask = 1) Cond code 11 (NOP if cond not met)	None	Unchanged

Branch on Condition	BCR	07	RR	M1, R2	Compare opr 1 with cond code Branch to opr 2 adr if cond met (If opr 2 = 0) NOP	None	Unchanged
Branch on Count	BCT	46	RX	R1, D2(X2, B2)	Reduce opr 1 by 1 and branch to opr 2 adr (If opr 1 = 1) Reduce • $\overline{\text{Branch}}$	None	Unchanged
Branch on Count	BCTR	06	RR	R1, R2	Reduce opr 1 by 6 and branch to opr 2 adr (If opr 2 = 0) Reduce • $\overline{\text{Branch}}$	None	Unchanged
Branch on Index High	BXH	86	RS	R1, R3, D2(B2)	Add opr 3 to opr 1 Sum compared to opr 3 if opr 3 adr is odd Sum compared to opr 3 = 1 if opr 3 adr is even Branch to opr 2 adr if sum opr 3/opr 3+1	None	Unchanged
Branch on Index Low or Equal	BXLE	87	RS	R1, R3, D2(B2)	Same as Branch On Index High Branch to opr 2 adr if sum opr 3/opr 3+1	None	Unchanged
Compare	C	59	RX	R1, D2(X2, B2)	Compare opr 1 algebraically to opr 3 (GPR)	Adr Spec	0 opr's = 1 1st < 2 1st >
Compare	CR	19	RR	R1, R2	Compare opr 1 algebraically to opr 2	None	0 opr's = 1 1st < 2 1st >
Compare Decimal	CP	F9	SS	D1(L1, B1), D2(L2, B2)	Compare opr 1 to opr 2 (binary right to left) byte by byte (Opr's must be packed) (Fields can overlap if low-order bytes coincide) (The shorter opr is extended with high-order zeros)	Adr Data	0 opr's = 1 1st < 2 1st >
Compare Halfword	CH	49	RX	R1, D2(X2, B2)	Compare opr 1 algebraically to opr 2 (Hi-order 16 bits expanded) opr 2	Adr Spec	0 opr's = 1 1st < 2 1st >

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Compare Logical	CL	55	RX	R1, D2(X2, B2)	Compare opr 1 to opr 2 (binary left to right) (Terminates if/when ≠ found)	Adr Spec	0 opr's = 1 1st < 2 1st >
Compare Logical	CLC	D5	SS	D1(L, B1), D2(B2)	Compare opr 1 to opr 2 (binary left to right) (Terminated if/when ≠ found) (opr length max 256 bytes)	Adr	0 opr's = 1 1st < 2 1st >
Compare Logical	CLI	95	SI	D1(B1), I2	Compare opr 1 to opr 2 (Imm) (Sto) (binary left to right) (Terminates if/when ≠ found)	Adr	0 opr's = 1 1st < 2 1st >
Compare Logical	CLR	15	RR	R1, R2	Compare opr 1 to opr 2 (binary left to right) (Terminates if/when ≠ found)	None	0 opr's = 1 1st < 2 1st >
Compare (Long)	CD	69	RX	R1, D2(X2, B2)	Compare opr 1 algebraically to opr 2 (FPR) (Equalize and subtract)	Adr Spec	0 opr's = 1 1st < 2 1st >
Compare (Long)	CDR	29	RR	R1, R2	Compare opr 1 algebraically to opr 2 (FPR) (Equalize and subtract)	Spec	0 opr's = 1 1st < 2 1st >
Compare (Short)	CE	79	RX	R1, D2(X2, B2)	Compare opr 1 algebraically to opr 2 (FPR) (Sto) (Low-order FPR ignored and unchanged)	Adr Spec	0 opr's = 1 1st < 2 1st >
Compare (Short)	CER	39	RR	R1, R2	Compare opr 1 algebraically to opr 2 (FPR) (FPR) (Low-order FPR ignored and unchanged)	Spec	0 opr's = 1 1st < 2 1st >
Convert to Binary	CVB	4F	RX	R1, D2(X2, B2)	Convert opr 2 (packed decimal) (Double-word bounds) to binary and put in opr 1	Adr Spec Data Exp Div	Unchanged

Convert to Decimal	CVD	4E	RX	R1, D2(X2, B2)	Convert opr 1 (binary) (double-word bounds) to packed decimal and put in opr 2	Prot Adr Spec	Unchanged
Diagnose	---	83	SI	See Principles of Operation, Form A22-6821	See Principles of Operation, Form A22-6821	Privileged Op Prot Spec Adr	Unpredict- able
Divide	D	5D	RX	R1, D2(X2, B2)	Divide opr 1 by opr 2 (even and odd GPRs) (Sto) Opr 1 becomes quotient and remainder	Adr Spec Exp Div	Unchanged
Divide	DR	1D	RR	R1, R2	Divide opr 1 by opr 2 Dividend: even and odd pair GPR's Opr 1 becomes quotient and remainder (full word only)	Spec Exp Div	Unchanged
Divide Decimal	DP	FD	SS	D1(L1, B1), D2(L2, B2)	Divide opr 1 by opr 2 Opr 1 becomes quotient and remainder (left justified) Dividend: at least 1 leading zero, max size 31 digits and sign Divisor: max size 15 digits and sign, numerically larger than dividend Both opr's packed format Remainder size = divisor size (Fields can overlap if low-order bytes coincide.)	Prot Adr Spec Data Dec Div	Unchanged
Divide (Long)	DD	6D	RX	R1, D2(X2, B2)	FP Divide opr 1 by opr 2 (FPR) (Sto) Opr 1 becomes quotient (prenormalized)	Adr Spec Exp Oflo FP. Div	Unchanged

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Divide (Long)	DDR	2D	RR	R1, R2	FP Divide opr 1 by opr 2 Prenormalize (FPR) (FPR) (Dividend) (Divisor) Opr 1 becomes quotient	Spec Exp Oflo Exp Uflo FP Div	Unchanged
Divide (Short)	DE	7D	RX	R1, D2(X2, B2)	FP Divide opr 1 by opr 2 Prenormalize (Dividend) (Divisor) Opr 1 becomes quotient (Low-order FPR ignored and unchanged)	Adr Spec Exp Oflo Exp Uflo FP Div	Unchanged
Divide (Short)	DER	3D	RR	R1, R2	FP Divide opr 1 by opr 2 Prenormalize (FPR) (FPR) (Dividend) (Divisor) Opr 1 becomes quotient (Low-order FPR ignored and unchanged)	Spec Exp Oflo FP Div	Unchanged
Edit	ED	DE	SS	D1(L, B1), D2(B2)	Opr 1 = pattern, opr 2 = source Opr 2 is changed from packed to zoned and edited under control of opr 1. Opr's processed left to right Zero digit and S Tgr off: Store fill char in pattern field. Blank and S Tgr off: Pattern char unchanged. Digit and S Tgr on: (if sig digit) Unpack source digit and store in pattern field. "c" significance start char "b" blank "j" field separate char "d" digit select char (Fill char is 1st char in pattern field unless it is a digit/select/significance-start char.) (Opr 1 terminates operation)	Prot Adr Data	Result 0 field = 0 1 field < 0 2 field > 0

Edit and Mark	EDMK	DF	SS	D1(L, B1), D2(B2)	Same as Edit (Adr of 1st significant result digit recorded in GPR 1)	Prot Adr Data	Result 0 field = 0 1 field < 0 2 field > 0
Exclusive OR	X	57	RX	R1, D2(X2, B2)	Exclusive-OR opr 2 and opr 1 and the modulo-two sum placed in opr 1	Adr Spec	0 Result = 0 1 Result ≠ 0
Exclusive OR	XC	D7	SS	D1(L, B1), D2(B2)	Exclusive-OR opr 2 and opr 1 and the modulo-two sum placed in opr 1 (Left to right byte by byte) (Max opr length is 256 bytes)	Prot Adr	0 Result = 0 1 Result ≠ 0
Exclusive OR	XI	97	SI	D1(B1), I2	The 1 byte from the instruction stream (8-15) is exclusive-ORed with opr 1 and the modulo-two sum placed in opr 1	Prot Adr	0 Result = 0 1 Result ≠ 0
Exclusive OR	XR	17	RR	R1, R2	Exclusive-OR logical opr 2 and opr 1 and the modulo-two sum placed in opr 1.	None	0 Result = 0 1 Result ≠ 0
Execute	EX	44	RX	R1, D2(X2, B2)	Execute the instruction at the branch-to adr (modified by ORing opr 1 8-15 with R1 24-31) (If R1 = 0, execute - no ORing)	Execute Adr Spec	Set by subject instruction
Halt I/O	HIO	9E	SI	D1(B1)	Current I/O operation of specified sub-channel or channel is terminated. (CSW 32-47 are stored) (Privileged instruction)	Privileged Oper	0 Chan or sub-chan working 1 CSW stored 2 NOP
Halve (Long)	HDR	24	RR	R1, R2	Fraction shifted right 1, opr 2 placed in opr 1 (FPRs) (char and sign unchanged)	Spec	Unchanged
Halve (Short)	HER	34	RR	R1, R2	Fraction shifted right 1, opr 2 placed in opr 1 (FPRs) (Low-order half of opr 1 unchanged, char and sign unchanged)	Spec	Unchanged

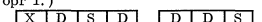
Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Insert Character	IC	43	RX	R1, D2(X2, B2)	Opr 2's char placed into opr 1, 24-31 (High-order bits unchanged)	Adr	Unchanged
Insert Storage Key	ISK	09	RR	R1, R2	Opr 2, 8-20 fetches sto key byte. This byte is placed in opr 1, 24-27. (opr 2, 0-7 and 21-27 ignored, 28-31 must = 0)	Privileged Oper Adr Spec	Unchanged
Load	L	58	RX	R1, D2(X2, B2)	Load opr 2 into opr 1	Spec Adr	Unchanged
Load	LR	18	RR	R1, R2	Opr 2 into opr 1	None	Unchanged
Load Address	LA	41	RX	R1, D2(X2, B2)	Opr 2, 12-31 to opr 1, 8-31. Opr 1, 0-7 set to zero (no storage reference made)	None	Unchanged
Load and Test	LTR	12	RR	R1, R2	Opr 2 into opr 1 (When opr 1 = opr 2: same as LTDR)	None	0 Result = 0 1 Result < 0 2 Result > 0
Load and Test (Long)	LTDR	22	RR	R1, R2	Opr 2 into opr 1 (FPR) (FPR) (When opr 1 and opr 2 specify same reg result is test without data transfer.)	Spec	Result 0 Fract = 0 1 Result < 0 2 Result > 0
Load and Test (Short)	LTER	32	RR	R1, R2	Opr 2 into opr 1 (FPR) (FPR) (Low-order half of opr 1 unchanged) (When opr 1 = opr 2: same as LTDR)	Spec	Result 0 Fract = 0 1 Result < 0 2 Result > 0
Load Complement	LCR	13	RR	R1, R2	2's complement of opr 2 into opr 1 (overflow when max negative number is complemented)	Exp Oflo	0 Result = 0 1 Result < 0 2 Result > 0 3 Overflow

Load Complement (Short)	LCER	33	RR	R1, R2	Opr 2 into opr 1 (FPR) (FPR) (Opr 1 sign inverted, low-order half unchanged) (Opr 2 sign inverted)	Spec	Result 0 Fract = 0 1 Result < 0 2 Result > 0
Load Complement	LCDR	23	RR	R1, R2	Same as LCER	Same as LCER	Same as LCER
Load Halfword	LH	48	RX	R1, D2(X2, B2)	Opr 2 low-order halfword into opr 1 (High-order expanded)	Adr Spec	Unchanged
Load (Long)	LD	68	RX	R1, D2(X2, B2)	Opr 2 into opr 1 (Sto) (FPR)	Adr Spec	Unchanged
Load (Long)	LDR	28	RR	R1, R2	Opr 2 into opr 1 (FPR) (FPR)	Spec	Unchanged
Load Multiple	LM	98	RS	R1, R3, D2(B2)	Opr 2 into GPRs in ascending order Starting reg specified by opr 1, ending reg specified by opr 3 (Reg wrap-around possible)	Adr Spec	Unchanged
Load Negative	LNR	11	RR	R1, R2	2's complement of opr 2 into opr 1 (GPR) (GPR) (If opr 2 contains a (-) number or zero, the number is unchanged)	None	0 Result = 0
Load Negative (Long)	LNDR	21	RR	R1, R2	Opr 2 into opr 1 (FPR) (FPR) (Both opr's made negative)	Spec	Result 0 Fract = 0 1 Result < 0
Load Negative (Short)	LNER	31	RR	R1, R2	Opr 2 into opr 1 (Both opr's made negative) (Low-order half of opr 1 unchanged)	Spec	Result 0 Fract = 0 1 Result < 0

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Load Positive	LPR	10	RR	R1, R2	Opr 2 into opr 1 (Negative numbers are complemented) (Overflow occurs when the max negative number is complemented)	Exp Oflo	0 Result = 0 2 Result > 0 3 Overflow
Load Positive (Long)	LPDR	20	RR	R1, R2	Opr 2 into opr 1 (FPR) (FPR) (Both opr's made positive)	Spec	Result 0 Fract = 0 2 Result > 0
Load Positive (Short)	LPER	30	RR	R1, R2	Opr 2 into opr 1 (Both opr's made positive) (Low-order half of opr 1 unchanged)	Spec	Result 0 Fract = 0 2 Result > 0
Load PSW	LPSW	82	SI	D1(B1)	Opr 1 into PSW (Opr 1 low-order 3 bit adr must = 0) (Instruction used to enter the problem or wait state)	Privileged Oper	Set by new PSW 34 and 35
Load (Short)	LE	78	RX	R1, D2(X2, B2)	Opr 2 into opr 1 (Sto) (FPR) (Low-order half of opr 1 unchanged)	Adr Spec	Unchanged
Load (Short)	LER	38	RR	R1, R2	Opr 2 into opr 1 (FPR) (FPR) (Low-order half of opr 1 unchanged)	Spec	Unchanged
Move	MVC	D2	SS	D1(L, B1), D2(B2)	Opr 2 to opr 1 (Left to right byte by byte) (Max number of bytes moved: 256) (No restriction on overlapping fields)	Prot Adr	Unchanged
Move	MVI	92	SI	D1(B1), I2	Move the 1 byte from the instruction stream (8-15) to opr 2	Prot Adr	Unchanged

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Multiply	MR	1C	RR	R1, R2	Multiply opr 1 by opr 2 Product: even and odd pair of GPRs Opr 1 becomes the product. (Opr 1 must specify an even-numbered reg) (Sign bit extended to 1st significant product digit)	Spec	Unchanged
Multiply Decimal	MP	FC	SS	D1(L1, B1), D2(L2, B2)	Multiply opr 1 by opr 2 Multiplier: 8 bytes max size and shorter than the multiplicand. Multiplicand: must have high-order zeros equal to or greater than the size of the multiplier. (Both opr's in packed format) (Right to left byte by byte) Product: must contain at least 1 high-order zero.	Prot Adr Spec Data	Unchanged
Multiply Halfword	MH	4C	RX	R1, D2(X2, B2)	Multiply opr 1 by opr 2 (Opr 2 is expanded to a 32-bit integer) (Only the low-order 32 bits of the product are retained)	Adr Spec	Unchanged
Multiply (Long)	NMD	6C	RX	R1, D2(X2, B2)	Multiply opr 1 by opr 2 (FPR) (Sto) Product: prenormalizes the opr's and post-normalizes the intermediate product. (If all fraction digits (14) = zero: the product sign and char are made zero.) (The intermediate product fraction is truncated before left-shifting.)	Adr Spec Exp Oflo Exp Uflo	Unchanged

Multiply (Long)	NMDR	2C	RR	R1, R2	Multiply opr 1 by opr 2 (FPR) (FPR) Product: prenormalizes the opr's and post-normalizes the intermediate product. (If all fraction digits (14) = 0: the product sign and char are made zero.) (The intermediate product fraction is truncated before left-shifting.)	Spec Exp Oflo Exp Uflo	Unchanged
Multiply (Short)	NME	7C	RX	R1, D2(X2, B2)	Multiply opr 1 by opr 2 (FPR) (FPR) Product: prenormalizes the opr's and post-normalizes the intermediate product. (If all fraction digits (14) = 0: the product sign and char are made zero.) (The intermediate product fraction is truncated before left-shifting.) (The 2 low-order fraction digits of the product always = zero.)	Adr Spec Exp Oflo Exp Uflo	Unchanged
Multiply (Short)	NMER	3C	RR	R1, R2	Multiply opr 1 by opr 2 (FPR) (FPR) Product: prenormalizes the opr's and post-normalizes the intermediate product. (If all fraction digits (14) = 0: the product sign and char are made zero.) (The intermediate product fraction is truncated before left-shifting.)	Spec Exp Oflo Exp Uflo	Unchanged
OR	O	56	RX	R1, D2(X2, B2)	The ORed sum of both opr's into opr 1	Adr Spec	0 Result = 0 1 Result ≠ 0
OR	OC	D6	SS	D1(L, B1), D2(B2)	The ORed sum of both opr's into opr 1 (Left to right byte by byte) (Max number of bytes ORed: 256)	Prot Adr	0 Result = 0 1 Result ≠ 0

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
OR	OR	16	RR	R1, R2	The ORed sum of both opr's into opr 1	None	0 Result = 0 1 Result ≠ 0
OR	OI	96	SI	D1(B1), I2	OR the 1 byte from the instruction stream (8-15) to opr 2	Prot Adr	0 Result = 0 1 Result ≠ 0
Pack	PACK	F2	SS	D1(L1, B1), D2(L2, B2)	Change opr 2 from zoned to packed format and place into opr 1. (Right to left byte by byte) (No restriction on overlapping fields) (Opr 2 may be extended with hi-order zeros if opr 1 too long, thereby inserting zeros in opr 1.) 	Prot Adr	Unchanged
Read Direct	RDD	85	SI	D1(B1), I2	The 1 byte from the instruction stream (8-15) is placed on the timing-signal bus-out, in a form of 8 timing pulses, along with a 9th pulse at the read-out line. The 8 bit lines at the direct-control bus-in lines are stored in opr 1.	Privileged Oper Prot Adr	Unchanged
Set Program Mask	SPM	04	RR	R1	Opr 1 (2-7) replaces the cond code and program mask bits of the current PSW (34-39) (Bits 0, 1 and 8-31 are ignored and unchanged.)	None	Set by bits 2 and 3
Set Storage Key	SSK	08	RR	R1, R2	Opr 1 (24-27) replaces the storage key specified by the opr 2 (Opr 1 bits 0-23 and 28-31 are ignored) (Opr 2 bits 0-7 and 21-27 are ignored) (Bits 28-31 must be zero)	Privileged Oper Adr Spec	Unchanged
Set System Mask	SSM	80	SI	D1(B1)	Opr 1 (1 byte) replaces the system mask bits of the current PSW (0-7).	Privileged Oper Adr	Unchanged

Shift Left Double	SLDA	8F	RS	R1, D2(B2)	Opr 1 (even and odd GPRs) is shifted left the number of times equal to opr 2 (low-order 6 bits).	Spec Exp Oflo	0 Result = 0 1 Result < 0 2 Result > 0 3 Overflow
Shift Left Double Logical	SLDL	8D	RS	R1, D2(B2)	Opr 1 (even and odd GPRs) is shifted left the number of times equal to opr 2 (low-order 6 bits).	Spec	Unchanged
Shift Left Single	SLA	8B	RS	R1, D2(B2)	Opr 1 is shifted left the number of times equal to opr 2 (low-order 6 bits).	Exp Oflo	0 Result = 0 1 Result < 0 2 Result > 0 3 Overflow
Shift Left Single Logical	SLL	89	RS	R1, D2(B2)	Opr 1 is shifted left the number of times equal to opr 2 (low-order 6 bits)	None	Unchanged
Shift Right Double	SRDA	8E	RS	R1, D2(B2)	Opr 1 (even and odd GPRs) is shifted right the number of times equal to opr 2 (low-order 6 bits).	Spec	0 Result = 0 1 Result < 0 2 Result > 0
Shift Right Double Logical	SRDL	8C	RS	R1, D2(B2)	Opr 1 (even and odd GPRs) is shifted right the number of times equal to opr 2 (low-order 6 bits). (Vacated bits are replaced with zeros) (Hi-order bit participates in the shift)	Spec	Unchanged
Shift Right Single	SRA	8A	RS	R1, D2(B2)	Opr 1 is shifted right the number of times equal to opr 2 (low-order 6 bits). (Shifting (+) numbers: vacated bits are replaced with zeros.) (Shifting (–) numbers: vacated bits are replaced with ones.)	None	0 Result = 0 1 Result < 0 2 Result > 0
Shift Right Single Logical	SRL	88	RS	R1, D2(B2)	Opr 1 is shifted right the number of times equal to opr 2 (low-order 6 bits). (Vacated bits are replaced with zeros) (Hi-order bit participates in the shift)	None	Unchanged

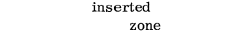
Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond code
Start I/O	SIO	9C	SI	D1(B1)	Opr 1 (21-31) identifies the selected chan, ctl unit and I/O device to perform write, read, read bkwd, control or sense oper. The CAW at loc 48 is fetched, which locates the first CCW. The SIO is initiated providing the addressed chan, ctl unit and I/O device are available without pending interrupt errors, exceptional conditions pending.	Privileged oper	0=I/O oper initiated 1=CSW stored 2=Chan or ctl unit busy 3=Not operational
Store	ST	50	RX	R1, D2(X2, B2)	Opr 1 is stored into opr 2	Prot Adr Spec	Unchanged
Store Character	STC	42	RX	R1, D2(X2, B2)	Opr 1 (24-31) replaces the character at opr 2's address.	Prot Adr	Unchanged
Store Halfword	STH	40	RX	R1, D2(X2, B2)	Opr 1 (16 low-order bits) is stored at opr 2's location. (Hi-order bits ignored and unchanged)	Adr Prot Spec	Unchanged
Store (Long)	STD	60	RX	R1, D2(X2, B2)	FP. opr 1 to opr 2's location	Adr Prot Spec	Unchanged
Store Multiple	STM	90	RS	R1, R3, D2(B2)	Opr 1 thru opr 3 are stored at opr 2's location in ascending order. Starting reg specified by opr 1, ending reg specified by opr 3. (Reg wrap-around possible)	Adr Prot Spec	Unchanged
Store (Short)	STE	70	RX	R1, D2(X2, B2)	FP. opr 1 is stored at opr 2's location. (Low-order FPR ignored and unchanged)	Adr Prot Spec	Unchanged

Subtract	S	5B	RX	R1, D2(X2, B2)	Subtract opr 2 from opr 1 and place the difference into opr 1	Adr Spec Exp Oflo	0 Dif = 0 1 Dif < 0 2 Dif > 0 3 Overflow
Subtract	SR	1B	RR	R1, R2	Subtract opr 2 from opr 1; difference placed into opr 1.	Exp Oflo	0 Dif = 0 1 Dif < 0 2 Dif > 0 3 Overflow
Subtract Decimal	SP	FB	SS	D1(L1, B1), D2(L2, B2)	Subtract dec opr 2 from opr 1; difference stored into opr 1. (Right to left byte by byte) (Both opr's must be in packed format) (Fields can overlap if low-order bytes coincide)	Prot Adr Data Dec Oflo	0 Dif = 0 1 Dif < 0 2 Dif > 0 3 Overflow
Subtract Halfword	SH	4B	RX	R1, D2(X2, B2)	Subtract opr 2 from opr 1 ; difference placed into opr 1. (Opr 2 hi-order 16 bits expanded)	Adr Spec Exp Oflo	0 Dif = 0 1 Dif < 0 2 Dif > 0 3 Overflow
Subtract Logical	SL	5F	RX	R1, D2(X2, B2)	Subtract opr 2 from opr 1; difference placed into opr 1.	Adr Spec	0 1 Dif ≠ 0 2 Dif = 0 3 Dif ≠ 0
Subtract Logical	SLR	1F	RR	R1, R2	Subtract opr 2 from opr 1; difference placed into opr 1.	None	0 1 Dif ≠ 0 2 Dif = 0 3 Dif ≠ 0
Subtract Normalized (Long)	NSD	6B	RX	R1, D2(X2, B2)	FP. Subtract opr 2 from opr 1 and the difference placed into opr 1. (The sign of opr 2 is inverted before the addition.)	Adr Spec Sign Exp Oflo Exp Uflo	Result 0 Fract = 0 1 Result < 0 2 Result > 0 3 Exp Oflo

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Subtract Normalized (Long)	NSDR	2B	RR	R1, R2	FP. Subtract opr 2 from opr 1 (FPR) (FPR) (The sign of opr 2 is inverted before the addition.)	Spec Sign	Result 0 Fract = 0 1 Result < 0 2 Result > 0 3 Exp Oflo
Subtract Normalized (Short)	NSE	7B	RX	R1, D2(X2, B2)	FP. Subtract opr 2 from opr 1 (The sign of opr 2 is inverted before the addition.) (Low-order FPR ignored and unchanged	Adr Spec Sign Exp Oflo Exp Uflo	0 Result Fract = 0 1 Result < 0 2 Result > 0 3 Exp Oflo
Subtract Normalized (Short)	NSER	3B	RR	R1, R2	Subtract opr 2 from opr 1 (The sign of opr 2 is inverted before the addition.) (Low-order FPRs ignored and unchanged)	Spec Sign Exp Oflo Exp Uflo	Result 0 Fract = 0 1 Result < 0 2 Result > 0 3 Exp Oflo
Subtract Unnormalized (Long)	SW	6F	RX	R1, D2(X2, B2)	FP. Subtract opr 2 from opr 1 (Sto) (FPR)	Adr Spec Sign Exp Oflo	0 Result Fract = 0 1 Result < 0 2 Result > 0 3 Exp Oflo
Subtract Unnormalized (Long)	SWR	2F	RR	R1, R2	FP. Subtract opr 2 from opr 1 (FPR)	Spec Sign Exp Oflo	0 Result Fract = 0 1 Result < 0 2 Result > 0 3 Exp Oflo
Subtract Unnormalized (Short)	SU	7F	RX	R1, D2(X2, B2)	FP. Subtract opr 2 from opr 1 (Sto) (FPR) (Low-order FPR ignored and unchanged)	Adr Spec Sign Exp Oflo	0 Result Fract = 0 1 Result < 0 2 Result > 0 3 Exp Oflo

Subtract Unnormalized (Short)	SUR	3F	RR	R1, R2	FP. Subtract opr 2 from opr 1 (FPR) (FPR) (Low-order FPRs ignored and unchanged)	Spec Sign Exp Oflo	0 Result Fract = 0 1 Result < 0 2 Result > 0 3 Exp Oflo
Supervisor Call	SVC	OA	RR	I	Immediate bits (8-15) replace (24-31) of the old PSW which is stored as a result of the interrupt. (16-23) are made zero. (Old PSW at loc 32) (New PSW from loc 96)	None	Unchanged
Test and Set	TS	93	SI	D1(B1)	Hi-order bit of 1st opnd adr sets cond code. Entire byte then set to 1's	Prot Adr	0 Hi-order bit = 0 1 Hi-order bit = 1 2 --- 3 ---
Test Channel	TCH	9F	SI	D1(B1)	Opr 1 (21-23) identifies the tested channel. (Bits 24-31 are ignored.) (Instruction checks the channel's status and sets appropriate cond code.)	Privileged Oper	0 Chan Avl 1 Int Pending 2 Chan in Burst Mode 3 Chan not Operational

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Test I/O	TIO	9D	SI	D1(B1)	Opr 1 (21-31) identifies the tested channel, control unit, and I/O device. Used to clear an interrupt pending in the control unit. (CSW stored at loc 64): Control unit contains a pending interrupt. I/O device contains a pending interrupt. Control unit or I/O device is executing a previous operation or a pending channel-end/control unit-end for another I/O device. Channel or I/O device equipment error.	Privileged Oper	0 Available 1 CSW stored 2 Channel or Ctl Unit Busy 3 Not Operational
Test Under Mask	TM	91	SI	D1(B1), I2	Immediate bits (8-15) used as a mask to compare against opr 1. Mask 1 bit: storage bit tested. Mask 0 bit: storage bit ignored.		0 Selected bits all zero (mask is all zero) 1 Selected bits mixed 0's and 1's 3 Selected bits all 1's
Translate	TR	DC	SS	D1(L, B1), D2(B2)	Opr 1 (argument byte) added to the initial adr of opr 2 (24-31). This adr now is the loc of the function byte which replaces the original argument byte (left to right byte by byte) (All data is valid) (Oper is terminated when opr 1 field is exhausted)	Protection Addressing	Unchanged

Translate and Test	TRT	DD	SS	D1(L, B1), D2(B2)	(Same as TR) When the function byte is a zero the next argument byte is translated. Both opr's remain unchanged. When the function byte is a non-zero the operation is completed. The generated argument adr is placed into GPR 1. The function byte is placed into GPR 2. (Left to right byte by byte) If opr 1 is exhausted before a non-zero cond, the opr is completed and GPRs 1 and 2 remain unchanged.	Addressing	00 - All function bytes 0 01 - Non-0 function byte met 10 - Last function byte non-0 11 - Not used
Unpack	UNPK	F3	SS	D1(L1, B1), D2(L2, B2)	Change opr 2 from packed to zoned format and place into opr 1. (Right to left byte by byte) (No restrictions on overlapping fields) (Opr 2 may be extended with hi-order zeros if opr 1 exceeds the length of opr 2, thereby inserting zeros in opr 1.) (If PSW bit 12 = 1) ASCII Zone code (If PSW bit 12 = 0) EBCDIC zone code inserted 	Adr Prot	Unchanged
Write Direct	WRD	84	SI	D1(B1), I2	The 1 byte from the instruction stream (8-15) is placed on the timing-signal bus-out, in a form of 8 timing pulses, along with a 9th pulse at the write-out line. The 8 bit lines at the direct-control bus-out lines are brought up by opr 1.	Privileged Oper Adr	Unchanged

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Zero and Add	ZAP	F8	SS	D1(L1, B1), D2(L2, B2)	Opr 1 cleared and opr 2 placed in opr 1 (Low-order opr's may coincide) (Opr 2 must be in packed format) (Opr 1 field must be large enough for all opr 2 significant digits)	Prot Adr Data Dec Oflo	0 Result = 0 1 Result < 0 2 Result > 0 3 Overflow

EXTENDED IBM CARD CODE TO HEXADECIMAL

Digits	Bl	T	E	O	TEO	TE	TO	EO
				(Zones)				
Bl	40	50	60	F0	70	6A	C0	D0
1	F1	C1	D1	61	B1	91	81	H1
2	F2	C2	D2	E2	B2	92	82	A2
3	F3	C3	D3	E3	B3	93	83	A3
4	F4	C4	D4	E4	B4	94	84	A4
5	F5	C5	D5	E5	B5	95	85	A5
6	F6	C6	D6	E6	B6	96	86	A6
7	F7	C7	D7	E7	B7	97	87	A7
8	F8	C8	D8	E8	B8	98	88	A8
9	F9	C9	D9	E9	B9	99	89	A9
18	79	49	59	69	B0	90	80	A0
28	7A	4A	5A	E0	BA	9A	8A	AA
38	7B	4B	5B	6B	BB	9B	8B	AB
48	7C	4C	5C	6C	BC	9C	8C	AC
58	7D	4D	5D	6D	BD	9D	8D	AD
68	7E	4E	5E	6E	BE	9E	8E	AE
78	7F	4F	5F	6F	BF	9F	8F	AF
19	31	01	11	21	71	51	41	E1
29	32	02	12	22	72	52	42	62
39	33	03	13	23	73	53	43	63
49	34	04	14	24	74	54	44	64
59	35	05	15	25	75	55	45	65
69	36	06	16	26	76	56	46	66
79	37	07	17	27	77	57	47	67
89	38	08	18	28	78	58	48	68
189	39	09	19	29	30	10	00	20
289	3A	0A	1A	2A	FA	DA	CA	EA
389	3B	0B	1B	2B	FB	DB	CB	EB
489	3C	0C	1C	2C	FC	DC	CC	EC
589	3D	0D	1D	2D	FD	DD	CD	ED
689	3E	0E	1E	2E	FE	DE	CE	EE
789	3F	0F	1F	2F	FF	DF	CF	EF

Bl = Blank
T = Twelve
E = Eleven
O = Zero

American Standard Code for Information Interchange (ASCII)
Extended to Eight Bits

Bit Positions → 76 / X5 / 4321	00	01	10	11
0000	NULL	DC_0		
0001	SOM	DC_1		
0010	EOA	DC_2		
0011	EOM	DC_3		
0100	EOT	DC_4 STOP		
0101	WRU	ERR		
0110	RU	SYNC		
0111	BELL	LEM		
1000	BKSP	S_0		
1001	HT	S_1		
1010	LF	S_2		
1011	VT	S_3		
1100	FF	S_4		
1101	CR	S_5		
1110	SO	S_6		
1111	SI	S_7		

4321 \ 76	00	01	10	11
0000	b blank	0		
0001	!	1		
0010	"	2		
0011	#	3		
0100	$	4		
0101	%	5		
0110	&	6		
0111	'	7		
1000	(	8		
1001	)	9		
1010	*	:		
1011	+	;		
1100	,	<		
1101	-	=		
1110	.	>		
1111	/	?		

4321 \ 76	00	01	10	11
0000			@	P
0001			A	Q
0010			B	R
0011			C	S
0100			D	T
0101			E	U
0110			F	V
0111			G	W
1000			H	X
1001			I	Y
1010			J	Z
1011			K	[
1100			L	\
1101			M	]
1110			N	↑
1111			O	←

4321 \ 76	00	01	10	11
0000				P
0001			a	q
0010			b	r
0011			c	s
0100			d	t
0101			e	u
0110			f	v
0111			g	w
1000			h	x
1001			i	y
1010			j	z
1011			k	
1100			l	
1101			m	
1110			n	ESC
1111			o	DEL

HEXADECIMAL AND DECIMAL CONVERSION

To find the decimal number, locate the Hex number and its decimal equivalent for each position. Add these to obtain the decimal number. To find the Hex number, locate the next lower decimal number and its Hex equivalent. Each difference is used to obtain the next Hex number until the entire number is developed.

BYTE				BYTE				BYTE			
0123		4567		0123		4567		0123		4567	
HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC
0	0	0	0	0	0	0	0	0	0	0	0
1	1,048,576	1	65,536	1	4,096	1	256	1	16	1	1
2	2,097,152	2	131,072	2	8,192	2	512	2	32	2	2
3	3,145,728	3	196,608	3	12,288	3	768	3	48	3	3
4	4,194,304	4	262,144	4	16,384	4	1,024	4	64	4	4
5	5,242,880	5	327,680	5	20,480	5	1,280	5	80	5	5
6	6,291,456	6	393,216	6	24,576	6	1,536	6	96	6	6
7	7,340,032	7	458,752	7	28,672	7	1,792	7	112	7	7
8	8,388,608	8	524,288	8	32,768	8	2,048	8	128	8	8
9	9,437,184	9	589,824	9	36,864	9	2,304	9	144	9	9
A	10,485,760	A	655,360	A	40,960	A	2,560	A	160	A	10
B	11,534,336	B	720,896	B	45,056	B	2,816	B	176	B	11
C	12,582,912	C	786,432	C	49,152	C	3,072	C	192	C	12
D	13,631,488	D	851,968	D	53,248	D	3,328	D	208	D	13
E	14,680,064	E	917,504	E	57,344	E	3,584	E	224	E	14
F	15,728,640	F	983,040	F	61,440	F	3,840	F	240	F	15
6		5		4		3		2		1	

HEXADECIMAL ADDITION

	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
2	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11
3	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
4	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
5	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
6	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15
7	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16
8	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
9	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19
B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A
C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B
D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D
F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

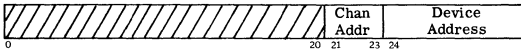
1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	04	06	08	0A	0C	0E	10	12	14	16	18	1A	1C	1E
3	06	09	0C	0F	12	15	18	1B	1E	21	24	27	2A	2D
4	08	0C	10	14	18	1C	20	24	28	2C	30	34	38	3C
5	0A	0F	14	19	1E	23	28	2D	32	37	3C	41	46	4B
6	0C	12	18	1E	24	2A	30	36	3C	42	48	4E	54	5A
7	0E	15	1C	23	2A	31	38	3F	46	4D	54	5B	62	69
8	10	18	20	28	30	38	40	48	50	58	60	68	70	78
9	12	1B	24	2D	36	3F	48	51	5A	63	6C	75	7E	87
A	14	1E	28	32	3C	46	50	5A	64	6E	78	82	8C	96
B	16	21	2C	37	42	4D	58	63	6E	79	84	8F	9A	A5
C	18	24	30	3C	48	54	60	6C	78	84	90	9C	A8	B4
D	1A	27	34	41	4E	5B	68	75	82	8F	9C	A9	B6	C3
E	1C	2A	38	46	54	62	70	7E	8C	9A	A8	B6	C4	D2
F	1E	2D	3C	4B	5A	69	78	87	96	A5	B4	C3	D2	E1

PERMANENT STORAGE ASSIGNMENT

ADDRESS DEC	ADDRESS HEX	ADDRESS BINARY	LENGTH	PURPOSE
0	0	0000 0000	double-word	Initial program loading PSW
8	8	0000 1000	double-word	Initial program loading CCW1
16	10	0001 0000	double-word	Initial program loading CCW2
24	18	0001 1000	double-word	External old PSW
32	20	0010 0000	double-word	Supervisor call old PSW
40	28	0010 1000	double-word	Program old PSW
48	30	0011 0000	double-word	Machine-check old PSW
56	38	0011 1000	double-word	Input/output old PSW
64	40	0100 0000	double-word	Channel status word
72	48	0100 1000	word	Channel address word
76	4C	0100 1100	word	Unused
80	50	0101 0000	word	Timer
84	54	0101 0100	word	Unused
88	58	0101 1000	double-word	External new PSW
96	60	0110 0000	double-word	Supervisor call new PSW
104	68	0110 1000	double-word	Program new PSW
112	70	0111 0000	double-word	Machine-check new PSW
120	78	0111 1000	double-word	Input/output new PSW
128	80	1000 0000	(1)	Diagnostic scan-out area

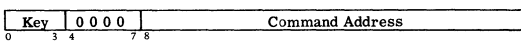
(1) The size of the diagnostic scan-out area depends on the particular model and I/O channels; for models 30 through 75, maximum size is 256 bytes.

SI Format

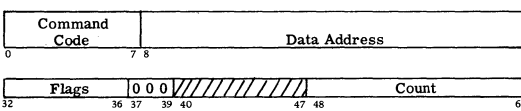


D1(B1)
S1
} HIO, SIO, TCH, TIO

CHANNEL ADDRESS WORD



CHANNEL COMMAND WORD



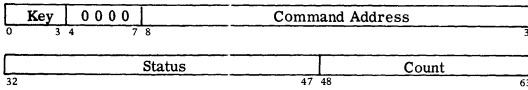
Command Code assignments are listed in the following table. The symbol X indicates that the bit position is ignored; M identifies a modifier bit.

CODE	COMMAND
MMMM 0 1 0 0	Sense
XXXX 1 0 0 0	Transfer in channel
MMMM 1 1 0 0	Read backward
MMMM MM0 1	Write
MMMM MM1 0	Read
MMMM MM1 1	Control

Bits 0-7 specify the command code.
Bits 8-31 specify the location of a byte in main storage.
Bits 32-36 are flag bits; refer to OPERATION CODE tables for flag bit assignments.
- Bit 32 causes the address portion of the next CCW to be used.
- Bit 33 causes the command code and data address in the next CCW to be use
- Bit 34 causes a possible incorrect length indication to be suppressed.
- Bit 35 suppresses the transfer of information to main storage.
- Bit 36 causes an interruption as Program Control Interrupt

Bits 37-39 must contain zeros.
Bits 40-47 are ignored.
Bits 48-63 specify the number of bytes in the operation.

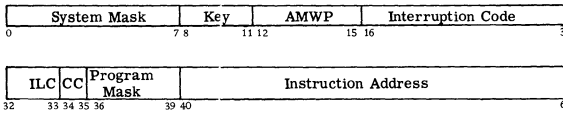
CHANNEL STATUS WORD



32 Attention
33 Status modifier
34 Control unit end
35 Busy
36 Channel end
37 Device end
38 Unit check
39 Unit exception
40 Program-controlled interruption
41 Incorrect length
42 Program check
43 Protection check
44 Channel data check
45 Channel control check
46 Interface control check
47 Chaining check

Count: Bits 48-63 form the residual count for the last CCW used.

PROGRAM STATUS WORD



0-7 System mask
0 Multiplexer channel mask
1 Selector channel 1 mask
2 Selector channel 2 mask
3 Selector channel 3 mask
4 Selector channel 4 mask
5 Selector channel 5 mask
6 Selector channel 6 mask
7 External mask
8-11 Protection key
12 ASCII mode (A)
13 Machine check mask (M)
14 Wait state (W)
15 Problem state (P)
16-31 Interruption code
32-33 Instruction Length code (ILC)
34-35 Condition code (CC)
36-39 Program mask
36 Fixed-point overflow mask
37 Decimal overflow mask
38 Exponent underflow mask
39 Significance mask
40-63 Instruction address

Interruption	Interruption Code (PSW Bits 16-31)	PSW Mask Bit	ILC	How Instruction Execution Is Finished
Machine Check	00000000 00000000	13	u	Terminated
Program				
Operation	00000000 00000001	-	1, 2, 3	Suppressed
Privileged operation	00000000 00000010	-	1, 2	Suppressed
Execute	00000000 00000011	-	2	Suppressed
Protection	00000000 00000100	-	0, 2, 3	Suppressed/Term
Addressing	00000000 00000101	-	1, 2, 3	Suppressed/Term
Specification	00000000 00000110	-	1, 2, 3	Suppressed
Data	00000000 00000111	-	2, 3	Suppressed/Term
Fixed-point overflow	00000000 00001000	36	1, 2	Completed
Fixed-point divide	00000000 00001001	-	1, 2	Suppressed/Comp
Decimal overflow	00000000 00001010	37	3	Completed
Decimal divide	00000000 00001011	-	3	Suppressed
Exponent overflow	00000000 00001100	-	1, 2	Terminated
Exponent underflow	00000000 00001101	38	1, 2	Completed
Significance	00000000 00001110	39	1, 2	Completed
Floating-point divide	00000000 00001111	-	1, 2	Suppressed
Supervisor Call	00000000 rrrrrrrr	-	1	Suppressed

External				
External signal 7	00000000 uuuuuuu1	7	u	Completed
External signal 6	00000000 uuuuuu1u	7	u	Completed
External signal 5	00000000 uuuuu1uu	7	u	Completed
External signal 4	00000000 uuuu1uuu	7	u	Completed
External signal 3	00000000 uuu1uuuu	7	u	Completed
External signal 2	00000000 uu1uuuuu	7	u	Completed
INTERRUPT pushbutton	00000000 u1uuuuuu	7	u	Completed
Timer	00000000 1uuuuuuu	7	u	Completed
I/O				
Multiplexor channel	00000000 aaaaaaaa	0	u	Completed
Selector channel 1	00000001 aaaaaaaa	1	u	Completed
Selector channel 2	00000010 aaaaaaaa	2	u	Completed
Selector channel 3	00000011 aaaaaaaa	3	u	Completed
Selector channel 4	00000100 aaaaaaaa	4	u	Completed
Selector channel 5	00000101 aaaaaaaa	5	u	Completed
Selector channel 6	00000110 aaaaaaaa	6	u	Completed

NOTES: u: Unpredictable
r: R1 and R2 fields of Supervisor Call instruction
a: I/O device address

OPERATOR PANEL INDICATORS

System Operating	Manual	Wait	CPU	I/O
Off	Off	Off	Invalid with Power on	
Off	Off	On	Waiting	Not Operating
Off	On	Off	Stopped	Not Operating
Off	On	On	Stopped and Waiting	Not Operating
* On	Off	Off	Running	Undetermined
* On	Off	On	Waiting	Operating
* On	On	Off	Stopped	Operating
* On	On	On	Stopped and Waiting	Operating

* Customer/CE meter should be operating.

Section number is determined by using the second, third and fourth positions of the diagnostic identification. For example, for diagnostic F124S, the section number is 124.

The "S" in the fifth position indicates the location of the diagnostic level in the identification.

Diagnostic sections followed by an asterisk (*) test the instruction set used by DMA8 (F024S).

Refer to System/360 General Service Aid 4 for additional information.

The meanings of the prefix (P1) are as follows:

F - Diagnostic used by all models

E - Diagnostics used by more than one but not all models

3 - Used by Model 30

4 - Used by Model 40

5 - Used by Model 50

6 - Used by Model 65

7 - Used by Model 75

F010S	DM1	F161S	AL,SL	F1B7S	SW
3020S	DMA4	F163S*	M	F1BAS	HER
F020S	DMA4	F165S	D	F1BBS	HDR
F024S	DMA8	F167S	CVD	F1C0S	MER
F050S	DMC	F16BS*	LPR,LNR	F1C1S	MDR
F060S	I/O SCOPE		LTR,LCR	F1C2S	ME
F0FAS	IPL 2311	F16CS	ALR,SLR	F1C3S	MD
F0FDS	80C CONV	F16DS	MR	F1C6S	DER
F0FES	DISK GEN	F170S	DR	F1C7S	DDR
F0FFS	UTILITY	F172S*	BXH,BXLE	F1C8S	DE
F101S*	LA	F174S	BRANCH	F1C9S	DD
F102S*	L	F177S*	SRDL,SRDA	F1CCS	MER,MDR
F103S*	ST		SLDL,SLDA		ME,MD
F104S*	A	F179S*	NC	F1CDS	DER,DE
F105S*	S,C	F17AS	OC		DDR,DD
F106S*	CL	F17BS*	XC	F1CES	FPT.ADDER
F107S*	N	F17CS	MVO	F1D0S	EX
310AS	DMA4 MSG	F17DS	MVN	F1D4S	EX
F110S*	LR	F17ES	MVZ	F1D5S	EX
F111S*	LR	F180S	UNPK	F1D7S	PGM.,INT
F112S*	LR	F181S	PACK	F1D9S	EX.,INT
F113S*	LR	F183S	TR	F1E1S	AP
F114S*	AR	F185S	TRT	F1E2S	AP
F115S*	SR,CR	F186S	BOUNDS TS	F1E3S	SP
F116S*	CLR	F187S	EX	F1E4S	CP
F117S*	NR	F188S	EX	F1E5S	ZAP
F118S*	OR	F189S	STD SET 2	F1E6S	CVD,AP,SP
F119S*	XR	F18AS	STD SET 2	F1E8S	MP
F120S*	BC,BCR	F18BS	PGM.,INT	F1E9S	MP
F121S*	BAL,BALR	F18DS	EX.,INT	F1EBS	DP
F122S*	BCT,BCTR	F18FS	SCRAMBLE	F1ECS	DP
F124S*	SVC,SPM	F191S	LE,STE	F1EES	ED
	LPSW,SSM	F192S	LD,STD	F1F0S	EDMK
F126S*	LH,STH,SH	F193S	CE	F1F2S	EX
	AH,CH	F194S	CD	F1F4S	PGM.INT
F127S*	MH	F195S	LER,CER	F1F6S	EX.INT
F12BS*	STM	F196S	CDR,LDR	4200S	BRING.UP
F12CS*	STM,LM	F198S	LTER	3201S	STD1.1
F12DS*	STM,LM	F199S	LTDR	3202S	STD1.2
F131S*	SRL,SRA	F19AS	LCER	3261S	STD2.1
	SLL,SLA	F19BS	LCDR	3262S	STD2.2
F132S	STD SET 1	F19CS	LPER	3263S	STD2.3
F134S*	TM	F19DS	LPDR	3264S	STD2.4
F135S*	CLI	F19ES	LNER	3291S	FP SEC1
F136S*	MVI	F19FS	LNDR	3292S	FP SEC2
F137S*	NI	F1A3S	AER	3293S	FP SEC3
F138S*	OI	F1A4S	ADR	32E1S	DEC ARITH
F139S*	XI	F1A5S	AE	32E2S	DEC ARITH
F140S*	IC,STC	F1A6S	AD	5340S	DIAG.ER
	ISK,SSK	F1A7S	AUR	6340S	DIAGN 62
F141S*	CLC,MVC	F1A8S	AWR	7340S	DIAGNOSE
F144S	EX	F1A9S	AU	4341S	DIAGNOSE
F146S*	EX	F1AAS	AW	5341S	DIAG.ER
F147S*	EX	F1B0S	SER	6341S	LOG OUT
F148S*	EX	F1B1S	SDR	7341S	LOG OUT
F14AS*	PGM INT	F1B2S	SE	4342S	CPU CKERS
F14BS	PGM INT	F1B3S	SD	5342S	DIAG.ER
F14CS	PGM INT	F1B4S	SUR	6342S	LOG OUT
F14DS	INV OPS	F1B5S	SWR	7343S	ERR-CK
F14ES	EX INTS	F1B6S	SU	6347S	DIAGNOSE

5348S	13 MICRO	343AS	CH FCT.10	F5F2S	2403 GAPL
5350S	ROS RIPPL	E441S	SEL CHAN	F5F3S	2403 GAPL
4358S	1.2 MICRO	E442S	SEL CHAN	F5F4S	2803 SAGE
31S	TIMER 60	E443S	SEL CHAN	F5F5S	2803 SAGE
382S	TIMER 60	E444S	SEL CHAN	F5F6S	2803 SAGE
E383S	TIMER 50	E445S	SEL COMP	F5F7S	BURROUGHS
E384S	TIMER 60	E446S	SEL CHAN	F5F8S	BURROUGHS
738DS	GMT/CLOCK	3447S	1ST SEL	F5F9S	BURROUGHS
738ES	GMT/CLOCK	3449S	1ST SEL	E5FDS	TAPE,BIT
F38FS	METER PGM	344AS	2ND SEL	F5FES	RD/WR VAR
338FS	USE METER	E451S	2860 CH	F5FFS	RD/WR VAR
90S	M2 D,E,F.	E452S	2860 CH	F600S	2841/2311
391S	STORAGE	E453S	2860 CH	F601S	2841/2311
5391S	STORAGE	E454S	2860 CH	F602S	2841/2311
4392S	STORAGE	E455S	2860 CH	F603S	2841/2311
5392S	STORAGE	E456S	CHAN FCT	F604S	2841/2311
4393S	STORAGE	F4D0S	CHAN/CHAN	F605S	2841/2311
5393S	STORAGE	F4D1S	CHAN/CHAN	F606S	2841/2311
4394S	STORAGE	F4E1S	D.C. A	F607S	2841/2311
94S	STORAGE	34E1S	DIRECT CTL	F608S	2841/2311
395S	STORAGE	F501S	2400/2800	F609S	2841/2311
5395S	STORAGE	F502S	2400/2800	F610S	2311
4396S	STORAGE	F503S	2400/2800	F611S	2311
5396S	STORAGE	F504S	2400/2800	F612S	2311
4397S	STORAGE	F505S	2400/2800	F613S	2311
5397S	STORAGE	F506S	2400/2800	F616S	2841/2311
E3A1S	2365 STOR	F507S	2400/2800	F617S	2841/2311
43C1S	LOCAL ST	F508S	2400/2800	F618S	2841/2311
53C1S	LOCAL ST	F509S	2400/2800	F619S	2841/2311
43C2S	ROS EXER	F50AS	2400/2800	F61AS	2841/2311
53C4S	BUMP ST	F50BS	2400/2800	F61BS	2841/2311
43C8S	SPLS WC	F50CS	2400/2800	F620S	2841/2302
33C9S	SP FEAT	F50DS	2400/2800	F621S	2841/2302
E3C9S	STG. PRO.	F50ES	2400/2800	F622S	2841/2302
E3CAS	STG	F50FS	2400/2800	F623S	2841/2302
63CCS	STORAGE	F510S	2400/2800	F624S	2841/2302
53D1S	SHAR STG.	F519S	2400/2800	F625S	2841/2302
E3E1S	2361/1,2	F51AS	2400/2800	F626S	2841/2302
E3E2S	2361/1,2	F51BS	2400/2800	F627S	2841/2302
E3E3S	2361/1,2	F521S	2400/2800	F628S	2841/2301
21S	MPX CHAN	F522S	2400/2800	F629S	2841/2302
422S	MPX CHAN	3523S	8K IRG	F630S	2302
E423S	MPX CHAN	3524S	8K IRG	F636S	2841/2302
E424S	MPX CHAN	F529S	2404/2804	F637S	2841/2302
E425S	MPX CHAN	F530S	2802 TAPE	F638S	2841/2302
E426S	MPX CHAN	F53AS	2802 TAPE	F639S	2841/2302
4427S	MX CH CKR	F53ES	TIM60/70	F63AS	2841/2302
E428S	MXCH 2540	E53ES	2802	F63BS	2841/2302
29S	MXCH 2540	F53FS	TIM40/50	F640S	2841/2321
42AS	MXCH 2540	E53FS	2802	F641S	2841/2321
E42BS	MXCH 2540	F54AS	2816 1/2	F642S	2841/2321
3430S	CHAN FCT.	F5E0S	RCA/581 T	F643S	2841/2321
3431S	CH FCT.U	F5E1S	RCA/581 T	F644S	2841/2321
3432S	CH FCT.2	F5E2S	RCA/581 T	F645S	2841/2321
3433S	CH FCT.3	F5E3S	RCA/581 T	F646S	2841/2321
3434S	CH FCT.4	F5E4S	RCA/581 T	F647S	2841/2321
436S	CH FCT.6	F5E5S	NON-DATA	F648S	2841/2321
437S	CH FCT.7	F5EBS	RCA/581 T	F649S	2841/2321
3438S	CH FCT.8	F5F0S	2403 GAPL	F64AS	2841/2321
3439S	CH FCT.9	F5F1S	2403 GAPL	F650S	2321

F656S	2841/2321	F805S	2821/2540	FA14S	1419 DOC
F657S	2841/2321	F808S	2821/1403	FA1ES	1419 LOGIC
F658S	2841/2321	F809S	2821/1403	FA20S	1418 FUNC.
F659S	2841/2321	F80CS	2821.1403	FA21S	1418 FUNC.
F65AS	2841/2321	F80DS	2821/1403	FA22S	1418 FUNC.
F65BS	2841/2321	F810S	2540 RDR	FA30S	1418 REJ.
F680S	2841 2 CH	F811S	2540 RDR	FA32S	1418 STK.
F681S	2841 2 CH	F815S	2540 RDR	FA34S	1418 DOC
F682S	2841 2 CH	F817S	2540 RDR	FA36S	1418 DRUM
E691S	2820/2860	F820S	2540 PCH	FA3ES	1418 LOGIC
E692S	2820	F821S	2540 PCH	FA40S	1412 FUNC.
E693S	2820/2301	F823S	2540 PCH	FA41S	1412 FUNC.
E694S	2820/2301	F825S	2540 PCH	FA50S	1412 REJ.
E695S	2820/2301	F830S	1403 PRT	FA52S	1412 STK.
E696S	2820/2301	F831S	1403 PRT	FA60S	1428 FCT.
E697S	2820/2301	F832S	1403 PRT	FA61S	1428 FCT.
E699S	2820/2301	F833S	1403 PRT	FA62S	1428 FCT.
E69AS	2820/2301	F836S	1403 RIP	FA70S	1428 REJ.
F69BS	2820/2301	F838S	1403 CARR	FA72S	1428 STK.
F700S	2848/2260	F839S	1403 CARR	FA74S	1428 DOC.
F701S	2848/2260	F83FS	1403 SEL	FA76S	1428 DRUM
F702S	2848/2260	F850S	1404 PRT.	FA7CS	1428 DATA
F703S	2848/2260	F851S	1404 PRT.	FA7ES	1428 LOGIC
F704S	2848/2260	F852S	1404 PRT.	FA90S	1231-N1
F705S	2848/2260	F870S	1442 N1	FB10S	2701 FEAT
F706S	2848/2260	F871S	1442 N1	FB11S	2701 FEAT
F707S	2848/2260	F872S	1442 N1	FB12S	2701 FEAT
F708S	2848/2260	F873S	1442 N1	FB13S	2701 FEAT
F709S	2848/2260	F876S	1442 N1	FB14S	2701 FEAT
E741S	1016 CU	F880S	PRINTER	FB15S	2701 FEAT
E742S	1016 CU	F881S	PRINTER	FB16S	2701 FEAT
E743S	1016 CU	F882S	PRINTER	FB20S	2701 FEAT
E744S	1015 IDT	F883S	PRINTER	FB21S	2701 FEAT
E745S	1015 IDT	F884S	CARR FCT	FB22S	2701 FEAT
F750S	2250-1	F885S	CARR FCT	FB23S	2701 FEAT
F751S	2250-1	F888S	1443 SCAN	FB24S	2701 FEAT
F752S	2250-1	F88BS	1443 SUGN	FB25S	2701 FEAT
F753S	2250-1	F8C0S	2501-B1/B2	FB30S	2701/TTY2
F756S	2250-1	F8C1S	2501-B1/B2	FB31S	2701/TTY2
F757S	2250-1	F8C2S	2501-B1/B2	FB32S	2701/TTY2
F758S	2250-1	F8D0S	2520-B1	FB33S	2701/TTY2
F759S	2250-1	F8D1S	2520-B1	FB34S	2701/TTY2
F75AS	2250-1	F8D2S	2520-B1	FB40S	2701 FEAT
F75BS	2250-1	F8D3S	2520-B1	FB41S	2701 FEAT
F760S	2250-1	F8D4S	2520-B1	FB42S	2701 FEAT
F761S	2250-1	F8D5S	2520-B1	FB43S	2701 FEAT
F762S	2250-1	F8D6S	2520-B1	FB44S	2701 FEAT
F763S	2250-1	F8D7S	2520-B1	FB45S	2701 FEAT
F764S	2250-1	F900S	1052 FCT	FB60S	2701 FEAT
F766S	2250-1	F901S	1052 FCT	FB61S	2701 FEAT
F767S	2250-1	F902S	1052 FCT	FB62S	2701 FEAT
F768S	2250-1	FA00S	1419 FUNC.	FB63S	2701 FEAT
F769S	2250-1	FA01S	1419 FUNC.	FB64S	2701 FEAT
F76AS	2250-1	FA04S	1419 REJ.	FB65S	2701 FEAT
F76BS	2250-1	FA05S	1419 STK	FB90S	2701 DAU
F76CS	2250-1	FA06S	1419 DOC	FB91S	2701 DAU
F801S	2821/2540	FA07S	1419/32	FB92S	2701 DAU
F802S	2821/2540	FA0FS	1419 LOGIC	FBA0S	2701/SDA
F803S	2821/2540	FA10S	1419 REJ.	FBA1S	2701/SDA
F804S	2821/2540	FA12S	1419 STK.	FBA2S	2701/SDA

FBA3S	2701/SDA	FE38S	Z71186	4F20S	1410/7010
FBA4S	2701/SDA	FE39S	Z71186	6F21S	7074 EMUL
FBA6S	2701/SDA	FE3AS	Z71186	6F22S	7074 EMUL
EC81S	2702	FE3BS	Z71186	6F23S	7074 EMUL
EC82S	2702	FE3DS	2701/857	6F24S	7074 EMUL
EC83S	2702	FE3ES	2701/857	6F25S	7074 EMUL
EC84S	2702	FE3FS	2701/857	6F26S	7074 EMUL
EC85S	2702	FE40S	2701/857	6F27S	7074 EMUL
EC86S	2702	FE4AS	2701/NASA	6F28S	7074 EMUL
EC87S	2702	FE4BS	2701/NASA	6F29S	7074 EMUL
EC88S	2702	FE4CS	2701/NASA	6F2AS	7074 EMUL
EC91S	7770-3	FE56S	RCA/2701	6F2BS	7074 EMUL
EC92S	7770-3	FE57S	RCA/2701	4F30S	1410/7010
EC93S	7770-3	FE58S	RCA/2701	6F31S	7080 EMUL
FC94S	7770-3	6E89S	RPQ...	6F32S	7080 EMUL
FC95S	7770-3		F12788 and	6F33S	7080 EMUL
FC96S	7770-3		F12996		RPQ.W16484
FCA0S	7772	6E8AS	7074 RPQ	3F40S	1620 COMP
FCA1S	7772	6E8B	RPQ...	3F41S	1620 I/O
FCA2S	7772		F12996	6F41S	7090 EMUL
FCA3S	7772	3F00S	14XX COMP	3F42S	1620 20K
FCA4S	7772	3F01S	14XX COMP	6F42S	7090 EMUL
FCA5S	7772	4F01S	1401 COMP	3F43S	1620/360
4E05S	RPQW12561	5F01S	1410/7010	3F44S	1620/360
4E06S	RPQW12561	3F02S	14XX COMP	3F45S	1620/360
4E08S	RPQW12561	4F02S	1401 COMP	3F46S	1620 CPU
4E09S	RPQW13518	5F02S	1410/7010	3F47S	1620 DISK
FE10S	2403 GAPL	3F03S	14XX COMP	3F48S	1620 DISK
FE11S	2403 GAPL	4F03S	1401 COMP	3F49S	1620 DISK
FE12S	2403 GAPL	5F03S	1410/7010	3F4AS	1620 DISK
FE13S	2403 GAPL	3F04S	14XX COMP	3F4BS	1620 DISK
EE20S	PROC CHAN	4F04S	1401 COMP	3F4CS	1620 FLAGS
	RPQ.W15994	5F04S	1410/7010	5F80S	SEREP
EE21S	PROC CHAN	3F05S	14XX COMP	6F80S	SEREP/62
	RPQ.W15994	4F05S	1401/1311	7F80S	SEREP
EE22S	PROC CHAN	5F05S	1401/1311	4F81S	SEREP B C
	RPQ.W15994	3F06S	14XX PMS	6F81S	SEREP/65
FE30S	2701/PA	3F07S	1402 RD	FF90S	EREP
FE31S	2701/PA	3F08S	1402 PFR		OBR/SDR
FE32S	2701/PA	3F09S	1402 COL	3FC1S	SYS TEST
FE33S	2701/PA	3F0CS	1403 PRT	3FC2S	SYS TEST
FE34S	2702	3F10S	1442 RD.	3FD0S	HEX LDR
	RPQ.M27370	4F10S	1410/7010	3FE1S	SEREP
	2702/8A1TT	3F13S	1443 PR.	5FE5S	ROS RIPPL
FE35S	2701/DSA	3F16S	MAG TAPE	FFF0S	2311 INIT
FE36S	2701/DSA	3F19S	2311/1311	FFF2S	2302 INIT
FE37S	2701/DSA	3F1CS	CONSOLE	FFF4S	2321 INIT

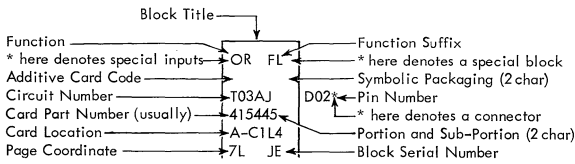
CIRCUIT DATA

Definitions of ALD Page Number Prefixes

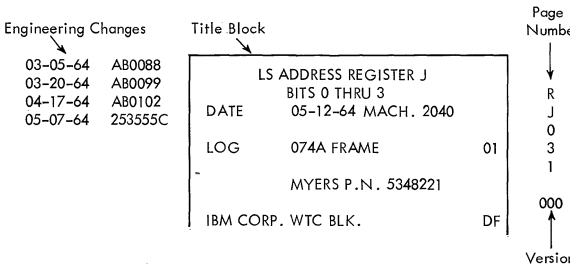
I.	Adders	
	1. Addressing Adder	AA-AB
	2. IC Incrementer	AC-AD
	3. Exponent Adder	AE-AF
	4. Main Adder	AM-AQ
	5. Serial Adder	AS
	6. VFL and DEC Adder	AV-AW
II.	Decoders	
	1. Op Decoders	DN
	2. FLP and Gen. Decoder	DP
	3. Addressing and Pre FTH	DA
	4. Trap Decode	DB
	5. Reg Decode	DG
	6. ROM Decode	DR-DS
III.	Counters	
	1. Instruction Ctrs	CA-CB
	2. Local Store Address Ctr	CC-CD
	3. Misc. Ctr	CE-CZ
IV.	Busing (Excluding Memory Bus)	BA-BZ
V.	Registers	
	1. A Reg	RA
	2. B Reg (BOP REG, Mod 70)	RB
	3. D Reg	RD
	4. E Reg (PSW for Mod 70)	RE
	5. F Reg (I/O Reg, Mod 70)	RF
	6. G Reg (Gen Purpose, Mod 70)	RG
	7. H Reg	RH
	8. J Reg	RJ
	9. K Reg	RK
	10. L Reg	RL
	11. M Reg	RM
	12. N Reg (Op Code Reg, Mod 70)	RN
	13. P Reg (FLT Pt Reg, Mod 70)	RP
	14. Q Reg (FLT Pt Reg, Mod 70)	RQ
	15. R Reg (Reg Bus Latch, Mod 70)	RR
	16. S Reg (Shift Ctr and Exp in, Mod 70)	RS
	17. T Reg	RT
	18. U Reg	RU
	19. V Reg	RV
	20. W Reg	RW
	21. X Reg	RX
	22. VFL and Decoder Reg, Mod 70	RY
	23. Direct Data Reg	RZ

VI.	Main Storage Registers and Controls in CPU (Includes SDR Registers, Storage Buses, SAR, SBI "OR", M and N Registers in Mod 30)	MA-MC
VII.	Controls	
	1. Advance or Seq Cntls	KA
	2. Branch and IC Cntls	KB
	3. Clock Cntls	KC
	4. I Exec (Mod 70) I Fetch and Exec (Mod 60)	KD
	5. Chan Cntls	KE
	6. Fix Seq Cntls	KF
	7. Gen Reg Cntls	KG
	8. FLT Cntls	KH
	9. ROS Cntls	KK
	10. Local Store Cntls	KL
	11. Priority and Interrupt Cntls	KM
	12. I/O Instr Cntls	KN
	13. VFL Cntls	KP
	14. VFL Cntls	KQ
	15. Check Triggers	KR
	16. Status Triggers	KS
	17. VFL Cntls and Decimal Cntls	KY
	18. Any Misc. Cntls such as FP	KT-KU
	19. Fixed Pt, Storage Protect, Real Time clk, Status Cntls	KW-KZ
VIII.	Consoles	PA-PE, PJ-PZ
	1052 Console Adapter	PF,PG,PH
IX.	Local Store	LS-LT
X.	TROS	EA-EC
XI.	CROS	ED-EF
XII.	Spec Features	XA-XZ
XIII.	Hardware Oriented Pages	ZA-ZZ
IV.	I/O Channels	
	Multiplex Channel	FA-FZ
	Selector Channel No. 1	GA-GZ
	Selector Channel No. 2	HA-HZ
	Direct Data	JA-JZ
XV.	ROS Flow charts	QA-QZ
XVI.	Power Supplies	YA-YZ

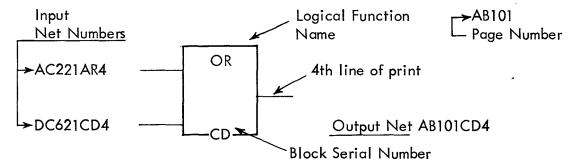
SLT ALD Logic Block



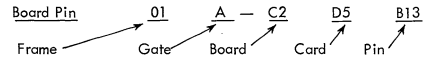
ALD Title Block, Page Number and Version, and Engineering Changes

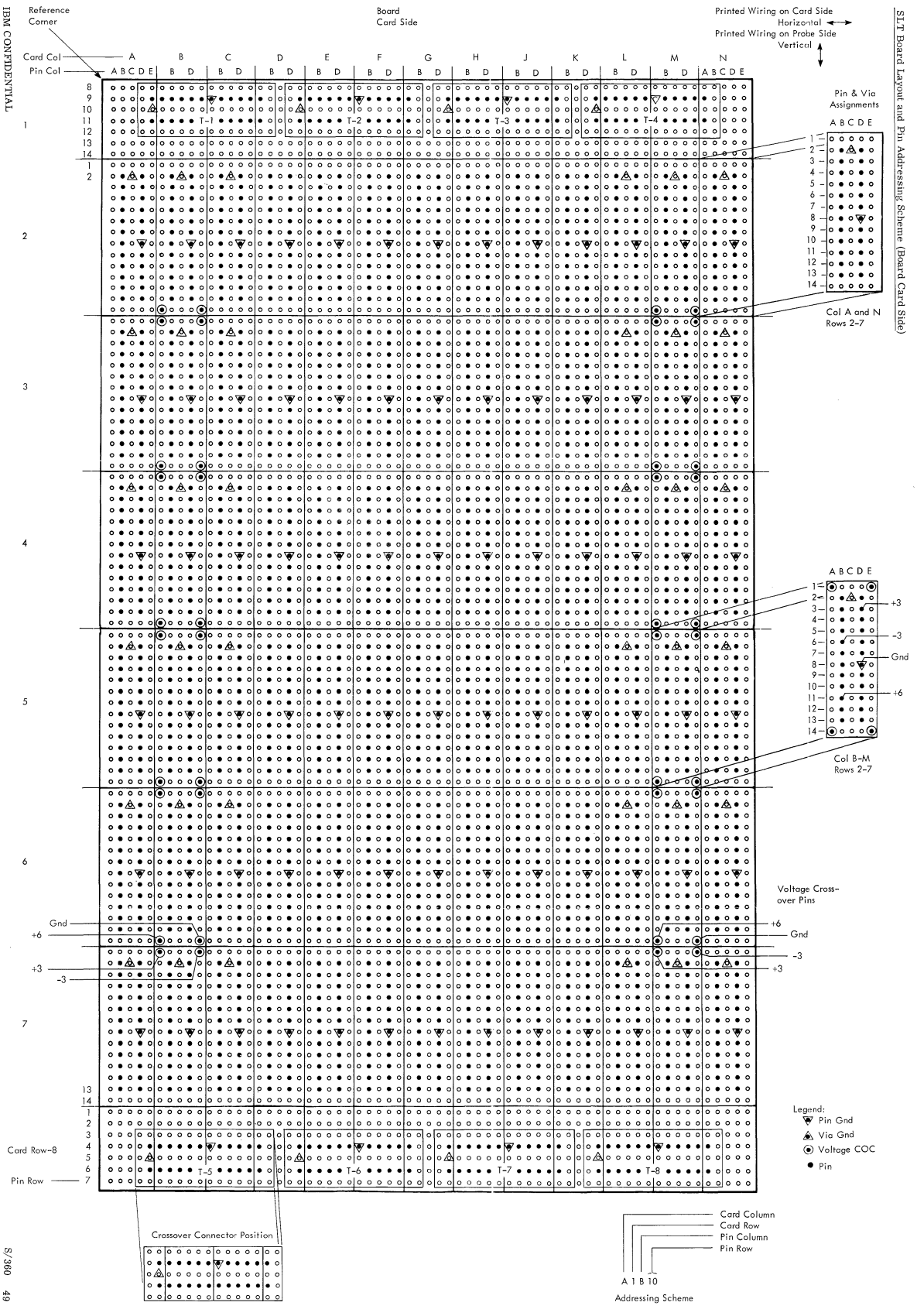


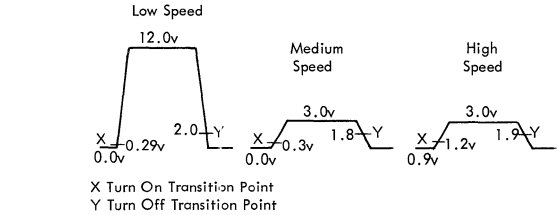
Net Numbers



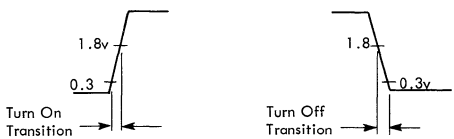
Connector Location Designations

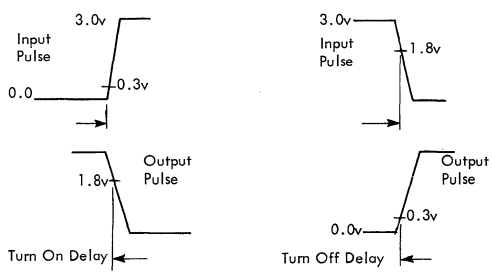


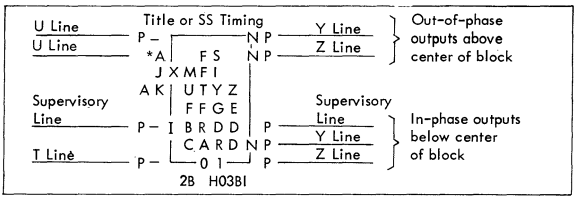

Reference Corner
Board Card Side
Printed Wiring on Card Side Horizontal
Printed Wiring on Probe Side Vertical
Card Col
Pin Col
A B C D E
B D
T-1
T-2
T-3
T-4
T-5
T-6
T-7
T-8
Pin & Via Assignments
Col A and N Rows 2-7
+3
-3
Gnd
+6
Col B-M Rows 2-7
Voltage Cross-over Pins
Card Row-8
Pin Row
Crossover Connector Position
Legend:
Pin Gnd
Via Gnd
Voltage COC
Pin
Card Column
Card Row
Pin Column
Pin Row
A 1 B 10
Addressing Scheme



X Turn On Transition Point
Y Turn Off Transition Point







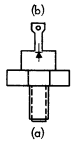
FS - Functional symbol (up to four characters -A, -TO, SS, ---)
MFI - Machine feature index or special note (up to four characters)
UT - Line type in
YZ - Line type out
FF - Frame (01 - 99)
G - Sliding gate (A, B, C, D) or module (A, B, C, ---)
E - Engineering change level tag (A, B, C, ---)
B - Chassis (1 - 6) or swinging gate (1 - 8)
R - Chassis Row (A - K) or swinging gate column (A - F)
DD - Chassis column (01 - 28) or swinging gate row (01 - 26)
P - Card socket pin (single card:A-R; double, Stan-Pac, or twin:A-8)
*A - Edge Connector, Test Point given in Note A
JX - Shield lead connected to pin J (X = twisted pair; * = coaxial cable)
AK - Pin A backpanel wired to pin K
CARD - Card code
2B - Page coordinates
H03BI - For engineering use; block identification (circuit type)
01 - For engineering use; block configuration (01, 02, 03, ---)
N - When used means normal (not supervisory) output, load in this block.
I - One of six symbols:
- 3 - Third level input, load in this block
- ◊ - Third level input, load elsewhere
- S - Split level input, load in this block
- 2 - Split level input, load elsewhere
- C - Cascode level input, load in this block
- H - Cascode level input, load elsewhere

SMS Line Levels

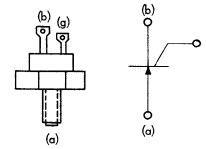
Line Type	Ideal Swing (volts)	Down Levels (volts)		Up Levels (volts)		Application
		Low	High	Low	High	
B	0 to + 6	+ 0.1	+ 0.3	+2.7	+6.8	DDTL, Uncompensated
B	0 to + 6	+ 0.1	+ 0.3	+5.6	+6.8	DDTL, Compensated
B	0 to + 6	- 0.8	+ 0.8	+3.2	+6.8	DDTL, DE Chain
C	0 to 15 ma	- 4.1	- 0.3	+0.6	+3.1	Std Interface DL, DT
D	-2.5 to +2.5	- 5.0	- 0.7	+0.7	+5.0	DEFL
E	-6 to +6	- 25.0	- 3.0	+3.0	+25.0	EIA Std Data Sets
E_s	+0.0 to -12.6	- 3.09	-12.6	+0.2	-0.0	SMAL Logic
N	± from 0 ref	- 3.0	- 0.4	+0.4	+1.2	Alloy Current Sw
N	± from 0 ref	- 0.9	- 0.4	+0.4	+0.6	Diffused Current Sw
P	± from -6 ref	- 7.2	- 6.4	-5.6	-3.0	Alloy Current Sw
P	± from -6 ref	- 6.6	- 6.4	-5.6	-5.2	Diffused Current Sw
Q	0 to 40 ma	- 3.8	- 0.5*	+0.6	+2.4	DL and DT
R	0 to +12	- 0.4	+ 0.2	+5.6	+12.5	CTRL
S	-12 to 0	-12.5	- 5.6	-0.2	+0.4	CTRL
S	-12 to 0	-12.5	- 6.9	-0.5	0.0	SDTRL
S'	-6 to 0	- 6.9	- 5.9	-0.5	0.0	Clamped SDTDL and SDTRL (7074)
T	-6 to +6	- 6.2	- 0.7	+1.4	+6.2	CTDL
U	-12 to 0	-12.5	- 7.4	-5.3	+0.2	CTDL
V	Any					Special
W	# 0 to -48	-53.0	- 43.0	-2.0	0.0	Relays
X	-30 to +10	-60.0	- 18.3	+5.5	+40.0	Tubes
Y	-6 to 0	- 8.8	- 5.8	-0.7	-0.1	SDTDL
Z	-6 to +6	- 7.0	- 4.2	+3.0	+6.2	Magnetic Shift Cores

* High down level can go to +0.1 on some circuits
\# 0 to relay source voltage; typically, 0 to -48

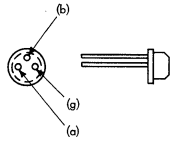
Diode (Stud Mount)



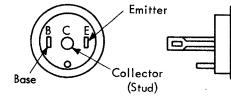
Stud Mount Style SCR



Top Hat Style SCR

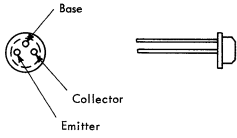


Cast Style Transistor
Type: 022, 108, etc.



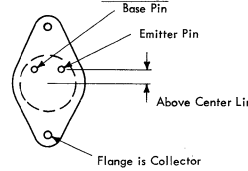
Bottom View Side View

Top Hat Style Transistor
Type: 026, 028, etc.

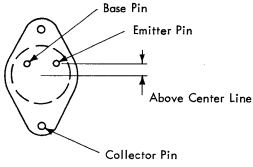


Bottom View Side View

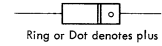
Flange Style Transistor - Type: 042, etc.
Bottom View



Flange Style Transistor - Type: 036, etc.
Bottom View

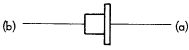


Axial Lead Capacitor



Ring or Dot denotes plus

Axial Lead Diode
Top Hat Style

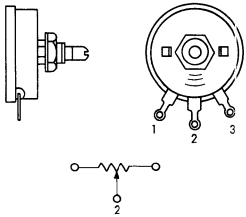


Rim of Top Hat is (a) side

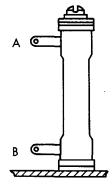
Axial Lead Diode
Glass Type

Symbol points to (a) or dot denotes (a) side

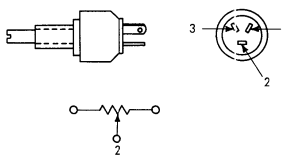
Potentiometer



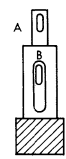
Ceramic Resistor



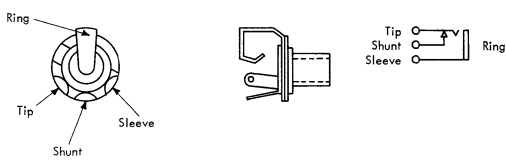
Potentiometer



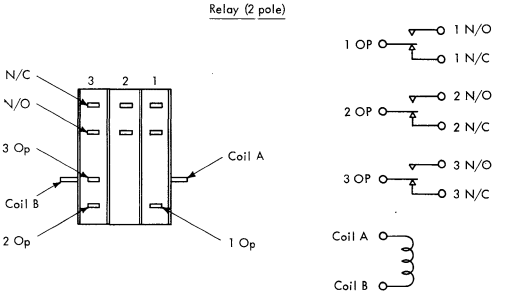
Fuse Holder



Jack



Relay (2 pole)



ADDRESS CARDS

1052/2150

1. These cards located at
   X - X1 - D2 and
   X - X1 - G2

2. Groups labeled "OUT" are used to decode the bus-out lines for address match

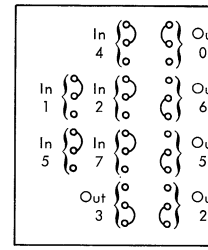
3. Groups labeled "IN" are those which generate the address to bus-in lines

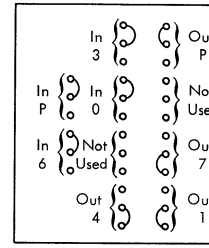
4. Jumper as shown for address "FF"

5. Maintain odd parity

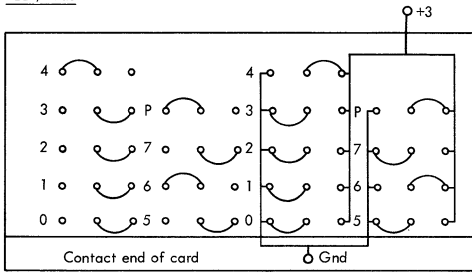
6. Card P/N 5800529

7. See "1052-2150 Locations"





1442/1443



1. This half of card used to sample bus-out lines for address match

2. Wire from center to left for bit desired

3. Wire from center to right for all other bits

4. Maintain odd parity

1. This half used to generate address to bus-in lines

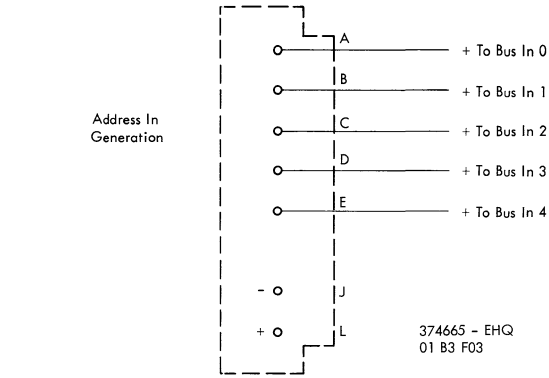
2. Wire from center to right for bits desired

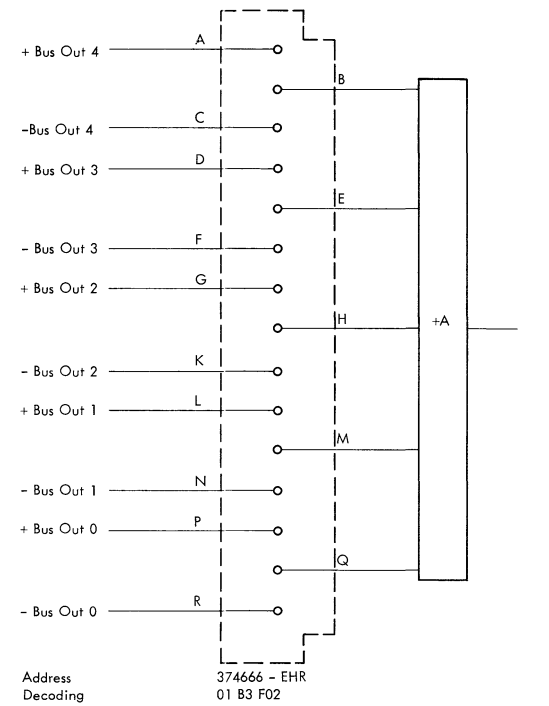
3. Jumper from center to left for all other bits

4. Maintain odd parity

Note: Example shown above is jumpered for address 0A, card P/N - 5804095.

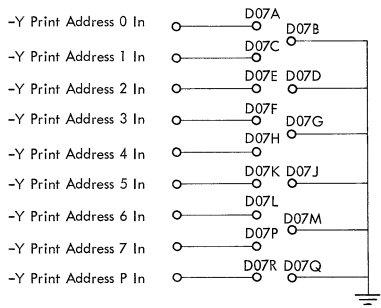
Locations:
1442 - A B1 D2
1443 - A1 H06


Address In
Generation
A
B
C
D
E
J
L
+ To Bus In 0
+ To Bus In 1
+ To Bus In 2
+ To Bus In 3
+ To Bus In 4
374665 - EHQ
01 B3 F03


+ Bus Out 4
-Bus Out 4
+ Bus Out 3
- Bus Out 3
+ Bus Out 2
- Bus Out 2
+ Bus Out 1
- Bus Out 1
+ Bus Out 0
- Bus Out 0
A
B
C
D
E
F
G
H
K
L
M
N
P
Q
R
+A
Address
Decoding
374666 - EHR
01 B3 F02

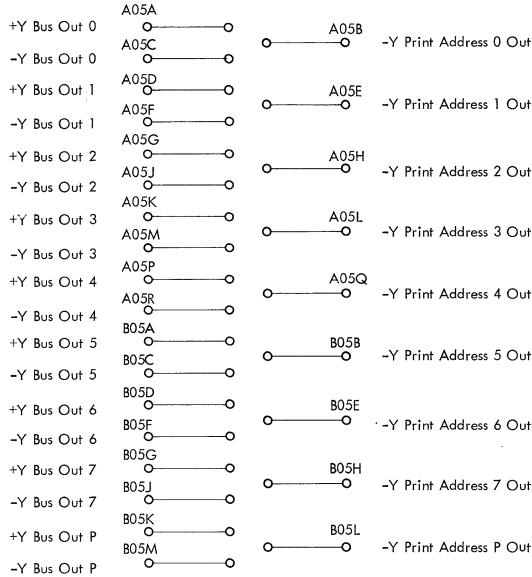
Printer Address Card Address In 21A1D07

To generate address:
Allow -Y Print Address In lines to float for those bits which should be present.
Jumper other lines to ground.



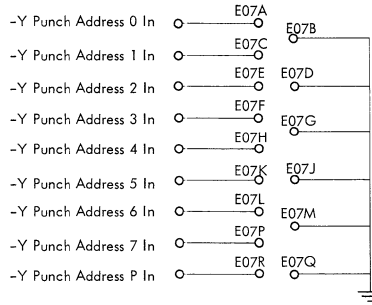
Address Out 21A3A05, B05

To recognize correct address: Jumper -Y Bus Out to -Y Print Address Out for those bits which should be present.
Jumper +Y Bus Out to -Y Print Address Out for those bits which should not be present.

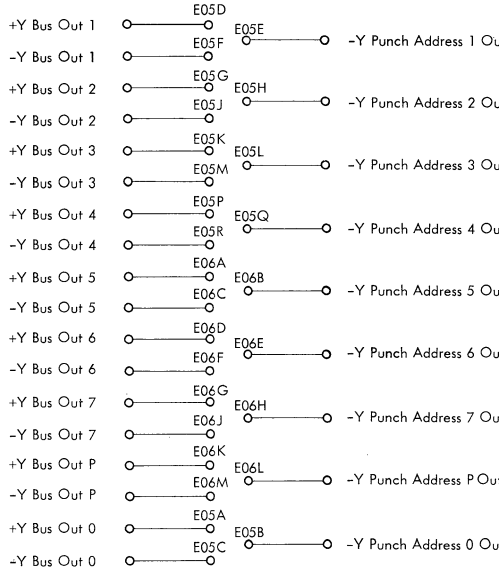


Punch Address In - Address Out (2821)

Address In 21B1E07
To generate address:
Allow -Y Punch Address In lines to float for those bits which should be present. Jumper other lines to ground.

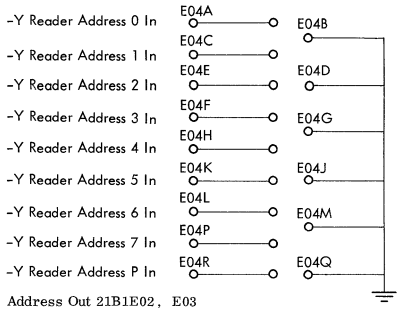


Address Out 21B1E05, E06
Jumper: -Y Bus Out to -Y Punch Address Out for those bits which should be present.
Jumper: +Y Bus Out to -Y Punch Address Out for those bits which should not be present.



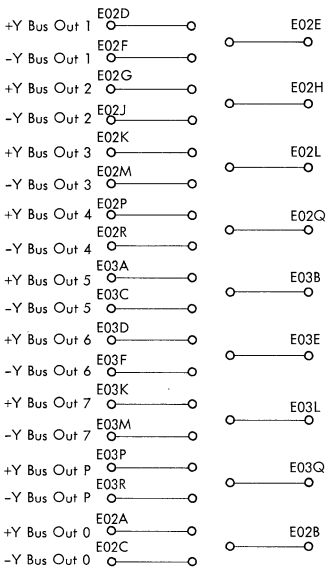
Reader Address In - Address Out (2821)

Address In 21AB1E04
To generate address:
Allow -Y Reader address In lines to float for those bits which should be present. Jumper other lines to ground.



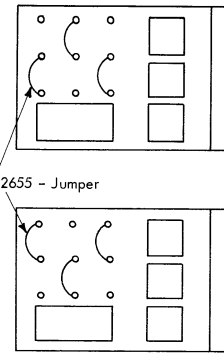
Address Out 21B1E02, E03

To recognize correct address: Jumper -Y Bus Out to -Y Reader Address Out for those bits which should be present
Jumper +Y Bus Out to -Y Reader Address Out for those bits which should not be present.



PRIORITY JUMPER CARD

To propagate select out (lowest priority) wire as shown at right



To propagate select in (highest priority) wire as shown at right

Card P/N - 5800385 or 5803081
Locations:
1052 - X - X1 - B6
1442 - A - A1 - C7
1443 - A - M4

For 2821

SMS card YPM, P/N 372680

To propagate select out (lowest priority), plug card at 21A1F09

To propagate select in (highest priority), plug card at 21A1F08

For 24XX/28XX Tape Control

SMS card EHR, P/N 374666

To propagate select out (lowest priority), plug: Q → R
M → N
H → K

To propagate select in (highest priority), plug: Q → P
M → L
H → G

Locations:

2403/2803	01A3E02	TC 40.12.2
2404/2804	01A1A13	TA 40.12.2 (IF A)
	01A1A14	TB 40.12.2 (IF B)

Collating Sequence	Graphics 8 Bit	Graphics BCD	8 Bit Code 0	1	2	3	4	5	6	7	BCD B	A	8	4	2	
00	blank	blank	0	1	0	0	0	0	0	0	0	0	0	0	0	
01	.	.	0	1	0	0	1	0	1	1	1	1	1	0	1	1
02	←	X)	0	1	0	0	1	1	0	0	1	1	1	1	0	0
03	(	□	0	1	0	0	1	1	0	1	1	1	1	1	0	1
04	+	<	0	1	0	0	1	1	1	0	1	1	1	1	1	0
05	GM	GM	0	1	0	0	1	1	1	1	1	1	1	1	1	
06	&	& +	0	1	0	1	0	0	0	0	1	1	0	0	0	0
07	$	$	0	1	0	1	1	0	1	1	1	0	1	0	1	1
08	*	*	0	1	0	1	1	1	0	0	1	0	1	1	0	0
09	)	⌐	0	1	0	1	1	1	0	1	1	0	1	1	0	1
10	;	;	0	1	0	1	1	1	1	0	1	0	1	1	1	
11	MC	MC	0	1	0	1	1	1	1	1	1	0	1	1	1	
12	-	-	0	1	1	0	0	0	0	0	1	0	0	0	0	0
13	/	/	0	1	1	0	0	0	0	1	0	1	0	0	0	1
14	,	,	0	1	1	0	1	0	1	1	0	1	1	0	1	1
15	%	% (	0	1	1	0	1	1	0	0	0	1	1	1	0	0
16	WS	WS	0	1	1	0	1	1	0	1	0	1	1	1	0	1
17	↑	\	0	1	1	0	1	1	1	0	0	1	1	1	1	0
18	SM	SM	0	1	1	0	1	1	1	1	0	1	1	1	1	1
19	↹	↹	0	1	1	1	1	0	1	0	0	1	0	0	0	0
20	"	"=	0	1	1	1	1	0	1	1	0	0	1	0	1	1
21	@	@ '	0	1	1	1	1	1	0	0	0	0	1	1	0	0
22	▽	:	0	1	1	1	1	1	0	1	0	0	1	1	0	1
23	=	>	0	1	1	1	1	1	1	0	0	0	1	1	1	0
24	TM	TM	0	0	0	1	0	0	1	1	0	0	1	1	1	
25	ö	ö	1	1	0	0	0	0	0	0	1	1	1	0	1	0
26	A	A	1	1	0	0	0	0	0	1	1	1	0	0	0	1
27	B	B	1	1	0	0	0	0	1	0	1	1	0	0	1	0
28	C	C	1	1	0	0	0	0	1	1	1	1	0	0	1	1
29	D	D	1	1	0	0	0	1	0	0	1	1	0	1	0	
30	E	E	1	1	0	0	0	1	0	1	1	1	0	1	0	
31	F	F	1	1	0	0	0	1	1	0	1	1	0	1	1	0
32	G	G	1	1	0	0	0	1	1	1	1	1	0	1	1	1

33	H	H	1	1	0	0	1	0	0	0	1	1	1	0	0	0
34	I	I	1	1	0	0	1	0	0	1	1	1	1	0	0	1
35	ō	ō	1	1	0	1	0	0	0	0	1	0	1	0	1	0
36	J	J	1	1	0	1	0	0	0	1	1	0	0	0	0	1
37	K	K	1	1	0	1	0	0	1	0	1	0	0	0	1	0
38	L	L	1	1	0	1	0	0	1	1	1	0	0	0	1	1
39	M	M	1	1	0	1	0	1	0	0	1	0	0	1	0	0
40	N	N	1	1	0	1	0	1	0	1	1	0	0	1	0	1
41	O	O	1	1	0	1	0	1	1	0	1	0	0	1	1	0
42	P	P	1	1	0	1	0	1	1	1	1	0	0	1	1	1
43	Q	Q	1	1	0	1	1	0	0	0	1	0	1	0	0	0
44	R	R	1	1	0	1	1	0	0	1	1	0	1	0	0	1
45	RM	RM	1	1	1	0	0	0	0	0	0	1	1	0	1	0
46	S	S	1	1	1	0	0	0	1	0	0	1	0	0	1	0
47	T	T	1	1	1	0	0	0	1	1	0	1	0	0	1	1
48	U	U	1	1	1	0	0	1	0	0	0	1	0	1	0	0
49	V	V	1	1	1	0	0	1	0	1	0	1	0	1	0	1
50	W	W	1	1	1	0	0	1	1	0	0	1	0	1	1	0
51	X	X	1	1	1	0	0	1	1	1	0	1	0	1	1	1
52	Y	Y	1	1	1	0	1	0	0	0	0	1	1	0	0	0
53	Z	Z	1	1	1	0	1	0	0	1	0	1	1	0	0	1
54	0	0	1	1	1	1	0	0	0	0	0	0	1	0	1	0
55	1	1	1	1	1	1	0	0	0	1	0	0	0	0	0	1
56	2	2	1	1	1	1	0	0	1	0	0	0	0	0	1	0
57	3	3	1	1	1	1	0	0	1	1	0	0	0	0	1	1
58	4	4	1	1	1	1	0	1	0	0	0	0	0	1	0	0
59	5	5	1	1	1	1	0	1	0	1	0	0	0	1	0	1
60	6	6	1	1	1	1	0	1	1	0	0	0	0	1	1	0
61	7	7	1	1	1	1	0	1	1	1	0	0	0	1	1	1
62	8	8	1	1	1	1	1	0	0	0	0	0	1	0	0	0
63	9	9	1	1	1	1	1	0	0	1	0	0	1	0	0	1

*BCD code for blank is:
C bit for odd parity
C and A bits for even parity

Character in Order of Sequence on the Chain (Standard)	BCD Code in PCG					
	B	A	8	4	2	1
1						1
2					2	
3					2	1
4				4		
5				4		1
6				4	2	
7				4	2	1
8			8			
9			8			1
0			8		2	
#			8		2	1
@			8	4		
/		A				1
S		A			2	
T		A			2	1
U		A		4		
V		A		4		1
W		A		4	2	
X		A		4	2	1
Y		A	8			
Z		A	8			1
&		A	8		2	
,		A	8		2	1
%		A	8	4		
J	B					1
K	B				2	
L	B				2	1
M	B			4		
N	B			4		1
O	B			4	2	
P	B			4	2	1
Q	B		8			
R	B		8			1
—	B		8		2	
$	B		8		2	1
*	B		8	4		
A	B	A				1
B	B	A			2	
C	B	A			2	1
D	B	A		4		
E	B	A		4		1
F	B	A		4	2	
G	B	A		4	2	1
H	B	A	8			
I	B	A	8			1
+	B	A	8		2	
.	B	A	8		2	1
←	B	A	8	4		

1052 PRINTER-KEYBOARD

Commands

Command	Bit 0	1	2	3	4	5	6	7
Write without Carrier Return	0	0	0	0	0	0	0	1
Write with Carrier Return	0	0	0	0	1	0	0	1
Read	0	0	0	0	1	0	1	0
Control Alarm	0	0	0	0	1	0	1	1
No-op	0	0	0	0	0	0	1	1
Test I/O	0	0	0	0	0	0	0	0
Sense	0	0	0	0	0	1	0	0

Status Byte

Bit	Name	Description
0	Attention	Request Button
1	Not Used	
2	Not Used	
3	Busy	
4	Channel End	
5	Device End	
6	Unit Check	Defined by Sense Byte
7	Unit Exception	Read Cancel Button

Sense Byte

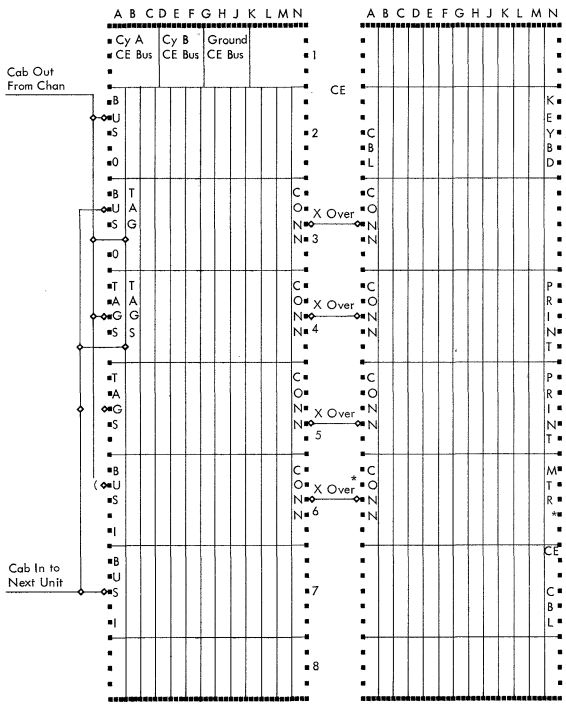
Bit	Name	Description
0	Command Reject	Invalid Command
1	Intervention Required	Not Ready
2	Bus-Out Check	Parity Error on Bus Out
3	Equipment Check	Typewriter Parity Error

X Board	
System	Location
2040	01BC1
2050	01CD4
2060	01ED1
2150	01AB1

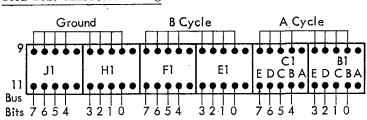
X Board (Card Side)

Y Board	
System	Location
2040	01BD1
2050	01CE4
2060	01EE1
2150	01AC1

Y Board (Card Side)



1052 Test Character Wiring



Bus	A Cycle	B Cycle	
0	1	1	Desired EBCDIC character and/or 1052 control function goes in this chart for layout purposes
1	0	1	
2	1	0	
3	0	1	
4	0	0	
5	1	1	
6	1	0	
7	0	0	"W" "M"

After layout:

-On Back Panel-		-On Back Panel-	
If AB = 00 (EX 4, 7)	Jumper Corresponding Bus Position to Ground	If AB = 10 (EX 2, 6)	Jumper Corresponding Bus Position to A Cycle
If AB = 01 (EX 1, 3)	Jumper Corresponding Bus Position to B Cycle	If AB = 11	Leave Bus Pos. Open

8A 84 21 6 Bit Code	LC	Print/ Function	01 23 45 67 8 Bit Code	UC	Print/ Function	01 23 45 67 8 Bit Code
00 00 01	1	1	11 11 00 01	=	=	01 11 11 10
00 00 10	2	2	11 11 00 10	<	<	01 00 11 00
00 00 11	3	3	11 11 00 11	;	;	01 01 11 10
00 01 00	4	4	11 11 01 00	:	:	01 11 10 10
00 01 01	5	5	11 11 01 01	%	%	01 10 11 00
00 01 10	6	6	11 11 01 10	♥	♥	01 11 11 01
00 01 11	7	7	11 11 01 11	>	>	01 10 11 10
00 10 00	8	8	11 11 10 00	*	*	01 01 11 00
00 10 01	9	9	11 11 10 01	(	(	01 00 11 01
00 10 10	0	0	11 11 00 00	)	)	01 01 11 01
11 00 01	a	a	10 00 00 01	_	_	01 00 00 01
11 00 10	b	b	10 00 00 10	B	B	01 00 00 10
11 00 11	c	c	10 00 00 11	C	C	11 00 00 11
11 01 00	d	d	10 00 01 00	D	D	11 00 01 00
11 01 01	e	e	10 00 01 01	E	E	11 00 01 01
11 01 10	f	f	10 00 01 10	F	F	11 00 01 10
11 01 11	g	g	10 00 01 11	G	G	11 00 01 11
11 10 00	h	h	10 00 10 00	H	H	11 00 10 00
11 10 01	i	i	10 00 10 01	I	I	11 00 10 01
10 00 01	j	j	10 01 00 01	J	J	11 01 00 01
10 00 10	k	k	10 01 00 10	K	K	11 01 00 10
10 00 11	l	l	10 01 00 11	L	L	11 01 00 11
10 01 00	m	m	10 01 01 00	M	M	11 01 01 00
10 01 01	n	n	10 01 01 01	N	N	11 01 01 01
10 01 10	o	o	10 01 01 10	O	O	11 01 01 10

8A 84 21 6 Bit Code	LC	Print/ Function	01 23 45 67 8 Bit Code	UC	Print/ Function	01 23 45 67 8 Bit Code
10 01 11	p	p	10 01 01 11	P	P	11 01 01 11
10 10 00	q	q	10 01 10 00	Q	Q	11 01 10 00
10 10 01	r	r	10 01 10 01	R	R	11 01 10 01
01 00 10	s	s	10 10 00 10	S	S	11 10 00 10
01 00 11	t	t	10 10 00 11	T	T	11 10 00 11
01 01 00	u	u	10 10 01 00	U	U	11 10 01 00
01 01 01	v	v	10 10 01 01	V	V	11 10 01 01
01 01 10	w	w	10 10 01 10	W	W	11 10 01 10
01 01 11	x	x	10 10 01 11	X	X	11 10 01 11
01 10 00	y	y	10 10 10 00	Y	Y	11 10 10 00
01 10 01	z	z	10 10 10 01	Z	∠	11 10 10 01
10 00 00	-	-	01 10 00 00	—	|	01 10 11 01
11 00 00	&	&	01 01 00 00	+	+	01 00 11 10
01 00 00	@	@	01 11 11 00	¢	¢	01 00 10 10
10 10 11	$	$	01 01 10 11	!	!	01 01 10 10
00 10 11	#	#	01 11 10 11	"	"	01 11 11 11
01 10 11	'	'	01 10 10 11	|	|	01 00 11 11
11 10 11	.	.	01 00 10 11	¬	¬	01 01 11 11
01 00 01	/	/	01 10 00 01	?	?	01 10 11 11
11 11 01	Tab	Tab	00 00 01 01	TAB	TAB	00 00 01 01
10 11 10	Bksp	Backspace	00 01 01 10	Bksp	Backspace	00 01 01 10
01 11 01	LF	Line Feed	00 10 01 01	LF	Line Feed	00 10 01 01
00 00 00	SP	Space	01 00 00 00	SP	Space	01 00 00 00
10 11 01	NL	New Line	00 01 01 01	NL	New Line	00 01 01 01

Commands

Command	Bit P	0	1	2	3	4	5	6	7
Test I/O	1	0	0	0	0	0	0	0	0
Sense	0	0	0	0	0	0	1	0	0
Read Backwards	P	0	0	M	M	1	1	0	0
Write (Diag Only)	0	0	0	0	0	0	0	0	1
Read	P	0	0	M	M	0	0	1	0
Control	P	M	M	M	M	1	1	1	1
No Op	1	0	0	0	0	0	0	1	1

Control Commands

Command	Bit P	0	1	2	3	4	5	6	7	
Select Stacker A	1	1	0	1	0	1	1	1	1	
B	0	1	0	1	1	1	1	1	1	
0	1	0	0	0	0	1	1	1	1	
1	0	0	0	0	1	1	1	1	1	
2	0	0	0	1	0	1	1	1	1	
3	1	0	0	1	1	1	1	1	1	
4	0	0	1	0	0	1	1	1	1	
5	1	0	1	0	1	1	1	1	1	
6	1	0	1	1	0	1	1	1	1	
7	0	0	1	1	1	1	1	1	1	
8	0	1	0	0	0	1	1	1	1	
9	1	1	0	0	1	1	1	1	1	
R	1	1	1	0	0	1	1	1	1	
Pocket Light Control	1	1	1	1	1	1	1	1	1	(1419 Only)
Engage	0	1	1	1	0	1	1	1	1	
Disengage	0	1	1	0	1	1	1	1	1	

Status Byte

Bit	Name	Meaning
0		Not Used
1		Not Used
2		Not Used
3	Busy	Control unit and device busy to all commands except Test I/O
4	Channel End	Data transfer complete
5	Device Check	Control unit and device are ready for a new command
6	Unit Check	Error condition in control unit or device
7	Unit Exception	A Read command has been given but no document is in position to be read

1412 Sense Byte 1

Bit	Name	Meaning
0	Command Reject	Two read commands without intervening stacker select; stacker select command on an auto select document. If stacker select is accepted and another is issued for same document, invalid control command or a write command.
1	Intervention Required	Jam, motor not running, film stop, full pocket, empty hopper or sort compare.
2	Bus Out Check	Bus out parity error.
3	Not Used	
4	Data Check	Select field not read correctly.
5	Overrun	Channel did not accept character in allotted time.
6	Late Read	Document under read head without read backward command.
7	Document Spacing Error	Document spacing too small or document too long.

1412 Sense Byte 2

Bit	Name	Meaning
0		Not Used
1		Not Used
2		Not Used
3	Amount Field Error	Unreadable character, special symbol missing or sequence error, field missing and read field key depressed, overrun in field, field length invalid, and late read indicator on.
4	Process Control Field Error	
5	Account Number Field Error	
6	Transit Routing Field Error	
7	Serial Number Field Error	

1419 Sense Byte 1

Bit	Name	Meaning
0	Command Reject	Two reads without an intervening stacker select; a stacker select issued for an auto-select document. If a stacker select is accepted and another is issued for same document, invalid control command and a write command when not in diagnostic mode.
1	Intervention Required	Jam, motor not running, film stop, full pocket, empty hopper, sort compare or endorser stop condition.
2	Bus Out Check	Bus out parity error.
3		Not Used
4	Data Check	Selected field not read correctly.
5	Overrun	Character not accepted in allotted time and late stacker select command.
6	Auto Select	Document rejected because late read, document spacing and overlength errors.
7	Document Spacing	Document spacing error

1419 Sense Byte 2

Bit	Name	Meaning
0	Not Used	
1	Not Used	
2	Document under Read Head	Set on or off depending on location of document when sense command is given.
3	Amount Field Valid	Field is read without error, including symbols, when read field key is operated.
4	Process Control Field Valid	
5	Account Number Field Valid	
6	Transit Field Valid	
7	Serial Number Field Valid	

Commands

Command	Bit 0	1	2	3	4	5	6	7
Read	-	-	-	x	x	x	1	0
Write	-	-	-	x	x	x	0	1
Control	-	-	x	x	x	x	1	1
Test I/O	0	0	0	0	0	0	0	0
Sense	x	x	0	0	0	1	0	0
No-Op	0	0	x	x	x	x	1	1
Punch Diag	x	x	1	1	0	1	0	0
Read Diag	x	x	0	1	0	1	0	0
Modifiers								
Eject	1	-	-	x	x	-	-	-
Select Stacker 2	-	1	-	x	x	-	-	-
Card Image	-	-	1	x	x	x	-	-

x is "don't care" bit

Status Byte

Bit	Name	Description
3	Busy	
4	Channel End	
5	Device End	
6	Unit Check	-- further explained by sense byte
7	Unit Exception	-- EOF and last card has been read

Sense Byte

Bit	Name	Description
0	Command Reject	
1	Intervention Required	-- not ready
2	Bus-Out Check	
3	Equipment Check	-- reader check, punch check, invalid card code punched and data error on CE read or write.
4	Data Check	-- invalid card code on read
5	Overrun Check	

Commands

Command	Bit 0	1	2	3	4	5	6	7
Write	M	M	M	M	M	0	0	1
Control (Skip or Space)	M	M	M	M	M	0	1	1
Test I/O	0	0	0	0	0	0	0	0
Sense	0	0	0	0	0	1	0	0
Diagnostic Read	0	0	0	0	1	1	0	0
Diagnostic Write	1	0	0	0	1	1	0	1
Diagnostic Control	1	0	1	1	0	1	1	1

Modifiers for Write and Control

Operation	Bit 0	1	2	3	4
Space 1 Line	0	0	0	0	1
Space 2 Lines	0	0	0	1	0
Space 3 Lines	0	0	0	1	1
Skip to Channel 1	1	0	0	0	1
Skip to Channel 2	1	0	0	1	0
Skip to Channel 12	1	1	1	0	0

Carriage Operation on a Write is a space or skip after print. On a Control, it is an immediate.

Status Byte

Bit	Name	Description
0,1,2	Not Used	
3	Busy	Command stored or status stacked.
4	Channel End	
5	Device End	
6	Unit Check	Channel 9 sensed in carriage tape.
7	Unit Exception	Channel 12 sensed in carriage tape.

Sense Byte

Bit	Names	
0	Command reject	Because read-backward command was received, or because more than 3 line spaces were requested, or because skip to channel 0, 13, 14, or 15 was received.
1	Intervention required	Printer not ready because forms check-ran out or jammed, or stop key or carriage stop key pressed, or cover interlock open.
2	Bus-Out Check	Parity error on bus-out during initial selection with command-out tag up, or data transfer with service-out tag up.
3	Equipment Check	Printer malfunction because of buffer register parity error or typebar synchronization error.
4 & 5	Typebar Selection	Changed only by repositioning the typebar-character indicator switch. 0 0 52-character set 0 1 13-character set 1 0 39-character set 1 1 63-character set
6	Channel 9	Hole sensed in channel 9 of carriage control tape during last write or control command.
7	Channel 12	Hole sensed in channel 12 of carriage control tape during last write or control command.

Commands	Bit 0	1	2	3	4	5	6	7	Hex	Options Required
Control										
No Operation	0	0	0	0	0	0	1	1	03	
Set BAC and Stop	0	0	0	0	0	1	1	1	07	1
Set Audible Alarm	0	0	0	0	1	0	1	1	0B	
Insert Cursor	0	0	0	0	1	1	1	1	0F	2
Set Prog Fcn Indicators	0	0	0	1	1	0	1	1	1B	3
Remove Cursor	0	0	0	1	1	1	1	1	1F	2
Set BAC and Start	0	0	1	0	0	1	1	1	27	1
Write	0	0	0	0	0	0	0	1	01	
Read										
Read Direct	0	0	0	0	0	0	1	0	02	
Read Buffer	0	0	0	0	0	0	1	0	02	1
Read Cursor	0	0	0	0	0	1	1	0	06	2
Read Manual Input	0	0	0	0	1	1	1	0	0E	4
Read X-Y	0	0	0	1	0	0	1	0	12	
Sense										
Test I/O	0	0	0	0	0	0	0	0	00	
Sense	0	0	0	0	0	1	0	0	04	

Note: Option Codes - 1 - Buffer
2 - Buffer, Character Generator and A/N Keyboard
3 - Program Function Keyboard
4 - Alpha/Numeric or Program Function Keyboard

Summary of Status and Sense Information

Status Byte

Bit	Name
0	Attention
1, 2	Unused
3	Busy
4	Chan End
5	Device End
6	Unit Check
7	Unused

Sense Byte 0

Bit	Name
0	Command Reject
1	Intervention Required
2	Bus Out Check
3	Equipment Check
4-7	Unused

Sense Byte 1

Bit	Name
0	Light Pen Detect
1	End Order Sequence
2	Character Mode
3-7	Unused

Sense Byte 2

Bit	Name
0, 1, 2	Unused
3-7	Hi-order Buffer Address Ctr

Sense Byte 3

Bit	Name
0-5	Lo-order Buffer Address Ctr
6, 7	Unused

Note: Sense byte 2 and 3 will be zero if the buffer is running when the sense command is issued.

Command Decoding

Channel Command	2702 Command	Command Byte Input to 2702 (Bus In)								LCW Command Field				LCW Mode Field			LCW TC Field	
		P	0	1	2	3	4	5	6	7	4	5	6	7	4	2	1	2	1
Sense	Sense	0	0	0	0	0	0	1	0	0	0	1	0	0					
Write	Write	0	0	0	0	0	0	0	0	1	0	0	0	1					
	Auto Wrap	1	0	0	0	0	0	1	0	1	0	1	0	1					
	Dial*	0	0	0	1	0	1	0	0	0	0	0	1	1	0	1	0		
	Break	0	0	0	0	0	1	1	0	1	1	1	0	1					
	Poll	1	0	0	0	0	1	0	0	1	1	0	0	1					
Read	Read	0	0	0	0	0	0	0	1	0	0	0	1	0					
	Prep Rd	1	0	0	0	0	0	1	1	0	0	1	1	0					
	Inhibit	1	0	0	0	0	1	0	1	0	1	0	1	0					
	Search	0	0	0	0	0	1	1	1	0	1	1	1	0					
Control	SADZER	0	0	0	0	1	0	0	1	1	0	0	1	1	0	0	0	0	0
	SADONE	1	0	0	0	1	0	1	1	1	0	0	1	1	0	0	0	0	1
	SADTWO	1	0	0	0	1	1	0	1	1	0	0	1	1	0	0	0	1	0
	SADTHREE	0	0	0	0	1	1	1	1	1	0	0	1	1	0	0	0	1	1
	Enable	1	0	0	1	0	0	1	1	1	0	0	1	1	0	0	1		
	Disable	0	0	0	1	0	1	1	1	1	0	0	1	1	0	1	1		
	No-Op	1	0	0	0	0	0	0	1	1									
	Pseudo										1	1	1	1					

* Decoded by channel as write command and by 2702 as control command.

Mode Control Codes from Control-Type Command, Bits 3, 4, and 5

Mode Name	Mode Field Position		
	4	2	1
No further definition required	0	0	0
Enable	0	0	1
Dial	0	1	0
Disable	0	1	1

Mode Control Codes from Terminal Controls

Mode Field Pos.	Mode Name			
	IBM Type I	IBM Type II	TTY Type I	TTY Type II
000	Control Mode	Control Mode	LTRS Mode	Not Used
001	Text In Downshift Mode	Text In Mode	FIGS Mode	
010	Text Out Downshift Mode	Text Out Mode	LTRS Search Mode	
011	Not Used	Not Used	FIGS Search Mode	
100	Not Used	Not Used	Not Used	
101	Not Used	Not Used	Not Used	
110	Text Out Upshift Mode	Not Used	Not Used	
111	Not Used	Not Used	Not Used	

Sequence Control Cards

Sequence Field Position			IBM Terminal Control Type I		IBM Terminal Control Type II		TTY Terminal Control Type I WTC Terminal Control		TTY Terminal Control Type II	
1	2	1	Receive	Transmit	Receive	Transmit	Receive	Transmit	Receive	Transmit
0	0	0	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset
0	0	1	Not Used	Data	Not Used	Data	Data	Data	Not Used	Data
0	1	0	Receiving	Halt	Receiving	Halt	Receiving	Halt	Receiving	Halt
0	1	1	Timeout	Prep End	Timeout	Prep End	Timeout	Prep End	Timeout	Prep End
1	0	0	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
1	0	1	LRC	LRC	Not Used	Not Used	FIGS H	Not Used	Not Used	Not Used
1	1	0	Not Used	Not Used	Not Used	Not Used	A	Not Used	Not Used	Not Used
1	1	1	End	End	End	End	End	End	End	End

Status Bytes (Initial and Ending)

Bit	Name	Description
0	Attention	(2702 does not set this bit in the status byte).
1	Status Modifier	Test I/O instruction decoded on initial selection. Unit busy or machine reset (power on, manual, or interface reset) while in initial selection.
2	Control Unit End	Unit busy or machine reset while in initial selection.
3	Busy	Unit busy or machine reset while in initial selection.
4	Channel End	No-op decoded during initial selection. Receive operation in progress when write-type command is about to be inserted. End sequence set in a send/receive operation.
5	Decode End	No-op decoded during initial selection. Receive operation in progress when write-type command is about to be inserted. End sequence set in a send/receive operation. If stacked on initial selection and other than Test I/O or No-op.
6	Unit Check	Parity check on command byte during initial selection. Invalid command byte decoded during initial selection. Channel End and Device End (4 and 5) and one of the following: not operate, equipment check, bus-out parity, timeout, overrun, command reject, and data check. Receive operation in progress when write-type command is about to be inserted.
7	Unit Exception	End sequence on a write poll command. Receive (C) while in sequence 2 of a read command. Negative answer to poll from 1050 in control mode of a receive operation.

Sense Byte

Bit	Name	Description
0	Command Reject	Invalid command decoded during initial selection.
1	Intervention Required	Phone line becomes not operational during a read or write operation in other than sequence 0 or 7.
2	Bus-Out Parity Check	Parity check detected (during initial selection) in command byte. Parity check detected during service cycle.
3	Equipment Check	Serial data bit and line adapter transmitter do not match (write operations only).
4	Data Check	Terminal controls signaled stop time for a character (in read operation only), but the line was not in mark state.
5	Overrun	In read operation, one character (or more) was destroyed because channel failed to service when requested.
6	Receiving	Timeout in progress, and space is received. As long as command field does not hold control code, space is received and bit count and strobe count fields are all 0's.
7	Timeout	When timeout runs for 28 sec, (strobe count and bit count fields are all 1's). When short timeout expires (2 sec for 1050 DCS during sequence 0 of a read operation).

Command	0	1	2	3	4	5	6	7
Test I-O	X	X	X	X	X	0	0	0
Sense	X	X	X	X	0	1	0	0
Read Backward	X	X	X	X	1	1	0	0
Write	X	X	X	X	X	X	0	1
Read	X	X	X	X	X	X	1	0
Control	0	0	C	C	C	1	1	1
Mode Set	D	D	M	M	M	0	1	1

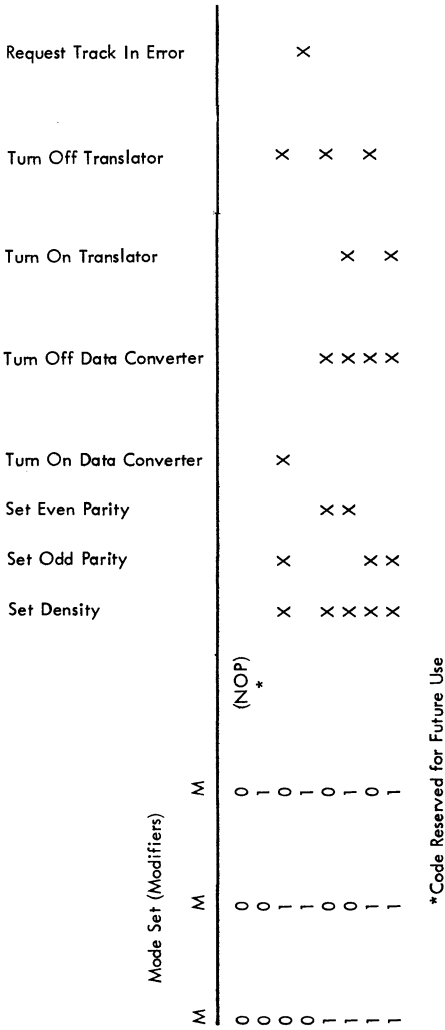
Control Code	C	C	C
Rewind	0	0	0
Rewind and Unload	0	0	1
Erase Gap	0	1	0
Write Tape Mark	0	1	1
Backspace Record	1	0	0
Backspace File	1	0	1
Forward Space Record	1	1	0
Forward Space File	1	1	1

Mode Set (Density)	D	D
200 bpi	0	0
556 bpi	0	1
800 bpi	1	0
800 bpi*	1	1

*

Applies to 7 track op only. 9 track op overrides but does not reset 7 track mode setting.

All 9 track operations force 800 bpi and odd parity.


Request Track In Error
Turn Off Translator
Turn On Translator
Turn Off Data Converter
Turn On Data Converter
Set Even Parity
Set Odd Parity
Set Density
Mode Set (Modifiers)
M
M
M
(NOP)
*
*Code Reserved for Future Use

Status Byte

Bit	Name	Description
0	Attention	Not used.
1	Status Modifier	Present with busy to indicate TCU busy.
2	Control Unit End	Signaled by the TCU: (a) At completion of operations during which a TCU busy was indicated. (b) At the completion of a control immediate operation during which a unit check or unit exception is detected.
3	Busy	When presented without bit 1 (status modifier bit), indicates that the tape unit is busy.
4	Channel End	Indicates that a read, read backward, write, mode set or sense has been completed, or that a control command has been accepted.
5	Device End	Indicates that the tape unit has completed operation at TU level of command. Device end indicated with channel end at the completion of command.
6	Unit Check	Set whenever: (a) Any bit is on in sense byte 0. (b) Tape unit performing read backward, backspace record or backspace file into or at load point. (c) A rewind and unload is completed at the TCU level.
7	Unit Exception	Set when: (a) A write, WTM or ERG operation is performed in the end of tape area. (b) A tape mark is sensed during a read, read backward, forward space record, or backspace record.

Sense Bytes

Sense Byte 0

Bit	Name	Description
0	Command Reject	Set when a write, write tape mark, or erase command is addressed to a file protected tape unit, or a data converter on mode set command is recognized on a TCU without the data converter feature. In this case the mode set is executed for parity, density, and translator.
1	Intervention Required	Set whenever status A is inactive. See "Sense Byte 2."
2	Bus-out Check	Set whenever even parity appears on bus-out during data transfer in initial selection or write operations.
3	Equipment Check	Set whenever an equipment check occurs. See "Sense Byte 5."
4	Data Check	Set when a data check occurs. See "Sense Byte 4."
5	Overrun	Set if service is requested, but data cannot be transferred during a read, write, or read backward operation.
6	Word Count Zero	Set during a write operation if transfer of data is prevented before the first byte of data.
7	Data Converter Check	See "Data Conversion Feature."

Sense Byte 1

Bit	Name	Description
0	Noise	
1	Status A	The meanings and responses of status A and status B are:
2	Status B	

Tape Unit Status A	Tape Unit Status B	Tape Unit Status	Response to Initial Selections
0	0	Non-existent TU	Unit check
0	1	Not ready	Unit check
1	0	Ready and not rewinding	Clear status
1	1	Ready and rewinding	Busy

3	Seven-Track	The selected tape unit has the seven-track feature installed.
4	Load Point	The selected tape unit is at load point.
5	Selected and Write Status	The selected tape unit is in write status.
6	File Protect	The selected tape unit is in the file protected status.
7		The selected TU is not compatible.

Sense Byte 2

This sense byte contains the track-in-error indicator bits that are set at the end of a read, or read backward command if a data check has been encountered. Bits 6 and 7 on together indicate either more than one error or no error found.

Sense Byte 3

Bit	Name	Description
0	R/W VRC	A VRC check occurred during a read or read backward operation. Indicator is not set after an over-run or after receipt of a stop command.
1	LRCR	An LRCR check occurred during write, write tape mark, read and read backward.
2	Skew	Excessive skew detected during a read back check on a write, write tape mark or erase operation.

Sense Byte 3 (Cont'd)

Bit	Name	Description
3	CRC	A cyclic redundancy check occurred during a read or read backward operation.
4	Skew Register VRC	A character with incorrect parity detected in skew register during write, write tape mark, and erase operation.
5		1,600 BPI set in TU.
6	Backward	
7	C Compare	C compare is an equipment check.

NOTE: Data checks include bits 0-4. Any will set data check in sense byte 1 (bit 4).

Sense Byte 4

Bit	Name	Description
0	Echo	The tape unit failed to generate an echo pulse in response to a write pulse.
1	Reject TU	Selected tape unit failed to respond to set read or set write status when instructed, or became not ready during execution of a tape motion operation.
2, 3, 4	Read Clock, Write Clock, Delay Counter	Associated clock has malfunctioned.
5, 6, 7	Sequence Indicators C, B, and A	These indicators are maintenance aids. They set only in the event of a machine failure and cause a unit check.

NOTE: Sense byte 4 and bit 7 of sense byte 3 are equipment checks and are normally the result of machine failure.

Timings in Microseconds unless Milliseconds (ms) Indicated

Timings

800 CPI Read Clock	Logic Page	Model 1	Model 2	Model 3
RC 0	60.41.2	0- 1.5	0- 1.4	0- 1.2
RC 2	60.41.2	3.8- 5.9	1.8- 3.6	1.3- 2.9
RC 4	60.41.1	7.6-10.4	3.7- 5.8	2.7- 4.5
RC 6	60.41.1	11.4-14.9	5.5- 8.1	4.0- 5.7
RC 7	60.41.1	13.3-17.2	6.4- 9.2	4.7- 6.6
RC 9	60.41.1	17.1-20.6	8.3-10.6	6.2- 7.1
RC Reset	60.41.1	14.0-17.9	7.2- 9.9	5.2- 8.1
Read Skew Gate	60.41.1	19.0-22.9	9.2-11.7	6.7- 8.0
Reset Wr Skew Gate Set	60.41.2	9.5-12.7	4.6- 7.0	4.0- 5.7
Rise of Skew Gate to RC 7 (Minimum)	60.41.1	2.6	1.6	0.6
RC Reset Write	60.41.1	19.0-22.9	9.2-11.7	6.7- 8.0

556 CPI Read Clock	Logic Page	Model 1	Model 2	Model 3
RC 0	60.41.2	0- 1.5	0- 1.4	0- 1.3
RC 2	60.41.2	5.4- 7.7	2.7- 4.5	1.8- 3.2
RC 4	60.41.1	10.8-14.1	5.4- 7.6	3.8- 5.4
RC 6	60.41.1	16.3-20.3	8.1-10.7	5.7- 7.6
RC 7	60.41.1	19.0-23.5	9.5-12.3	6.6- 8.7
RC 9	60.41.1	24.5-28.7	12.2-14.5	8.6- 9.9
RC Reset	60.41.1	19.7-24.3	10.2-13.1	7.1-10.2
Read Skew Gate	60.41.1	27.2-31.9	13.6-16.1	9.5-11.0
Reset Wr Skew Gate Set	60.41.2	10.8-13.3	5.4- 7.6	3.8- 5.4
Rise of Skew Gate to RC 7 (Minimum)	60.41.1	8.0	4.0	2.6
RC Reset Write	60.41.1	27.2-31.9	13.6-16.1	9.5-11.0

200 CPI Read Clock	Logic Page	Model 1	Model 2	Model 3
RC 0	60.41.2	0- 1.8	0- 1.7	0- 1.5
RC 2	60.41.2	16.9-19.8	7.8-10.8	5.4- 7.8
RC 4	60.41.1	33.9-37.8	15.6-19.8	10.8-14.0
RC 6	60.41.1	50.9-55.7	23.4-28.7	16.2-20.0
RC 7	60.41.1	59.4-64.7	27.3-33.2	18.9-23.2
RC 9	60.41.1	75.7-81.7	35.1-41.2	26.6-30.2
RC Reset	60.41.1	60.1-65.5	28.0-34.0	19.4-24.7
Read Skew Gate	60.41.1	84.0-90.7	39.0-45.7	27.1-31.7
Reset Wr Skew Gate Set	60.41.2	33.9-37.7	15.6-19.6	10.8-14.0
Rise of Skew Gate to RC 7 (Minimum)	60.41.1	25.0	11.5	8.0
RC Reset Write	60.41.1	84.0-90.7	39.0-45.7	27.1-31.7

Note: All timings measured with reference to Start Read Clock (60.31.1).

800 BPI Write Clock	Logic Page	Model 1	Model 2	Model 3
WC 2	60.81.1	Reference	Reference	Reference
WC 5	60.81.1	6.2- 7.0	3.0- 3.6	2.0- 2.3
Write Pulse	60.81.1	8.2- 8.8	4.1- 5.0	2.8- 3.8
Write Pulse Width	60.81.1	10.0-11.9	4.8- 6.7	3.4- 4.0
Stop and WC 14 & 15	60.81.1	24.8-25.5	12.3-13.0	8.3- 8.6
WC 2	60.81.1	33.1-33.6	16.4-16.7	11.0-11.3

556 BPI Write Clock	Logic Page	Model 1	Model 2	Model 3
WC 2	60.81.1	Reference	Reference	Reference
WC 5	60.81.1	8.8- 9.5	4.4- 5.0	2.9- 3.2
Write Pulse	60.81.1	11.8-12.5	5.9- 6.5	3.9- 4.4
Write Pulse Width	60.81.1	14.4-16.5	7.1- 8.5	4.9- 6.3
Stop and WC 14 & 15	60.81.1	35.4-36.4	17.8-18.5	11.9-12.3
WC 2	60.81.1	47.2-48.3	23.8-24.5	15.9-16.2

200 BPI Write Clock	Logic Page	Model 1	Model 2	Model 3
WC 2	60.81.1	Reference	Reference	Reference
WC 5	60.81.1	24.9- 25.5	12.4-13.0	8.3- 8.6
Write Pulse	60.81.1	33.2- 34.8	16.6-17.2	11.0-11.5
Write Pulse Width	60.81.1	41.2- 43.1	20.5-22.4	13.8-15.2
Stop and WC 14 & 15	60.81.1	99.7-100.3	49.9-50.5	33.2-33.4
WC 2	60.81.1	132.9-133.6	66.5-67.2	44.3-44.6

Timings in Microseconds unless Milliseconds (ms) Indicated

800 BPI Delay Counter usec	Logic Page	Model 1	Model 2	Model 3
WDD 27-30 Reset Write Reg	70.42.1	55.8- 60.2	27.8- 30.1	18.7- 21.1
WDD 35-42 Shift CRCR	70.42.1	72.4- 76.8	36.0- 38.4	24.2- 26.7
WDD 47-78 CRC to Write Bus	70.42.1	97.2-101.8	48.4- 50.9	32.5- 34.9
WDD 47-76 Write CRC P Bit	70.42.1	97.2-101.8	48.4- 50.9	32.5- 34.9
Set Wr Pulse Control	70.31.1	97.2-101.8	48.4- 50.9	32.5- 34.9
WDD 47 or 95		196.6-201.6	97.8-100.8	65.8- 68.3
WDD 51-58 Write Pulse CRC	70.31.1	105.5-110.1	52.5- 55.0	35.3- 37.0
End WDD and Write Check Char	70.31.1	109.7-114.2	54.5- 57.1	36.7- 37.8
WDD 53 or 117		242.1-247.4	120.5-123.7	
WDD 403	70.31.1			*198.7-200.5
RDD 17-30 Lost Character	70.41.1	35.3- 66.5	17.6- 33.3	11.5- 22.2
RDD 27-30 Shift CRCR and EPR	70.42.1	55.8- 59.9	27.8- 30.1	18.7- 21.1
RDD 36 Set 1st Check Char	70.21.1	74.5- 78.9	37.0- 39.4	24.9- 27.4
RDD 95 Set 2nd Check Char	70.42.1	196.6-201.6	97.8-100.8	65.8- 68.3
RDD 83-86 Shift CRC and EPR	70.42.1	171.8-176.6	85.4- 88.3	57.2- 60.0
RDD 95-98 EPR to Read Reg	70.42.1	196.6-201.6	97.8-100.8	65.8- 68.3
RDD 99-102 Reset EPR	70.42.1	204.9-209.9	101.9-105.0	68.6- 71.1
RDD 103-106 Set 1 in EPR	70.42.1	213.2-218.2	106.0-109.1	71.3- 73.9
RDD 111-142 Gate to Find Track	70.42.1	229.7-234.9	114.3-117.4	76.9- 79.4
RDD 169-172 Sample LRCR	70.42.1	349.8-355.5	174.0-177.8	117.1-118.5
RDD 171 Disconnect	70.51.1	353.9-359.7	176.1-179.8	118.5-119.7
RDD 91-94 Reset Read Reg	70.42.1	188.3-193.3	93.7- 96.6	60.3- 65.5
FSD 511 Disconnect (Rd Op)	70.51.1	1.05-1.06 ms	526.3-533.4	354.1-356.6
556 BPI Delay Counter usec				
WDD 47 or 95	70.31.1	138.6-146.5	70.0- 73.5	46.9- 50.0
Set Wr Pulse Control		280.2-290.0	141.5-145.5	94.9- 98.0
End WDD and Write Check Char-WDD 53	70.31.1	156.3-164.5	78.9- 82.5	52.0- 56.0
RDD 17-30 Lost Character	70.41.1	51.0- 96.0	25.2- 47.6	16.9- 32.2
RDD 36 Set 1st Check Char	70.21.1	106.2-113.6	53.6- 57.0	35.9- 39.0
RDD 95 Set 2nd Check Char	70.42.1	280.2-294.0	141.5-145.5	94.9- 98.0
RDD 169-172 Sample LRCR	70.42.1	*498.5-511.3	251.8-256.5	168.0-172.0
RDD 171 Disconnect	70.51.1	504.4-517.3	254.7-259.5	170.8-173.0
FSD 511 Disconnect (Rd Op)	70.51.1	1.5-1.53 ms	761.3-769.5	510.4-513.0
200 BPI Delay Counter usec				
WDD 47 or 95	70.31.1	390.5-407.6	195.5-204.0	139.1-136.7
Set Wr Pulse Control		789.4-806.1	395.2-404.2	263.1-269.7
End WDD & Write Check Char - WDD 53	70.31.1	440.4-457.0	220.4-229.0	143.5-154.0
RDD 17-30 Lost Character	70.41.1	141.0-267.0	70.7-137.0	47.0- 89.0
RDD 36 Set 1st Check Char	70.21.1	299.1-315.9	149.7-158.5	99.7-106.3
RDD 95 Set 2nd Check Char	70.42.1	789.4-807.0 ms	395.2-404.5	263.1-269.7
RDD 169-172 Sample LRCR	70.42.1	1.4- 1.42 ms	703.0-713.1	468.1-473.6
RDD 171 Disconnect	70.51.1	1.42- 1.44 ms	711.3-721.6	473.6-479.1
FSD 511 Disconnect (Rd Op)	70.51.1	4.24- 4.27 ms	2.12- 2.14 ms	1.41- 1.47 ms

* Measure From WDD 117

Note: Delay counter timings are measured with reference to the rise of "+ Microsecond Control" (60.71.1).

2803 TAPE CONTROL (Continued)

Delay Counter Milliseconds 240/1/2/3/4

Model 1	Logic Page	Function	Reference	9-Track	7-Track
End WDD	70.31.1	Reset Go on Write	See Note 2	Check Char (ms)	Check Char (ms)
D40 or 53 MS Not LP	70.31.1	End WD Not LP	Rise of Go 70.71.1	11.7-16.0	11.7-16.0
D160 TA	70.41.1	Set Go in Bkwd	Fall of M1 Rev Dly 70.71.1	25.5-26.5	25.5-26.5
D96 TA	70.41.1	Set Bkwd Read or Write	+MS Control 70.61.1	37.4-40.2	37.4-40.2
End Read Delay	70.41.1	End RD Not LP RD17-RD31	Rise of Go 70.71.1	6.8 - 7.6	12.4-13.2
		End RD Bkwd RD5	Rise of Go 70.71.1	2.0 - 2.8	2.0 - 2.8
		End RD LP RD 103	Rise of Go 70.71.1	41.1-42.0	41.1-42.0
Bksp Reset RD Cond	70.21.1	Reset Read Cond & Go RDD14-RDD24	+RDD 70.61.1	5.6 - 6.4	9.6 -10.4
WD 320	70.42.1	End WD LP WD 215	Rise of Go 70.71.1	85.9-86.8	85.9-86.8
WD 17	70.81.1	Set Read Cond on Write	Rise of Go	6.8 - 7.6	6.8 - 7.6
Model 2					
End WDD	70.31.1	Reset Go on Write	See Note 2	Check Char (ms)	Check Char (ms)
D40 or 53 MS Not LP	70.31.1	End WD Not LP	Rise of Go 70.70.1	6.3 - 6.8	6.3 - 6.8
D160 TA	70.41.1	Set Go In	Rise of TA 70.65.1	30.4-32.4	30.4-32.4
D96 TA	70.41.1	Set Bkwd Read or Write	Rise of TA 70.65.1	19.1-19.6	19.1-19.6
End Read Delay	70.41.1	End RD Not LP	Rise of Go 70.71.1p	3.4 - 3.8	5.9 - 6.6
		End RD Bkwd RD8	Rise of Go 70.71.1	1.6 - 2.0	1.6 - 2.0
		End RD LP RD103	Rise of Go 70.71.1	20.5-21.0	20.5-21.0
Bksp Reset Read Cond	70.21.1	Reset Read Cond & Go RDD11-RDD21	+RDD 70.61.1	2.2 - 2.6	4.2- 4.6
WD 215 + 320	70.42.1	End WD LP WD 215	Rise of Go 70.71.1	43.0-43.4	43.0-43.4
WD 17	70.81.1	Set Read Cond on Write	Rise of Go 70.71.1	3.4 - 3.8	3.4 - 3.8
Model 3					
End WDD	70.31.1	Reset Go on Write	+MS Control 70.61.1	See Note 1	1.7 - 2.0
D30+32+53MS Not LP	70.31.1	End WD not LP	Rise of Go 70.71.1	5.3 - 5.5	5.3 - 5.5
D160 TA	70.41.1 70.42.1	Set Go in Bkwd	+MS Control 70.61.1	16.0-16.2	16.0-16.2
D96 TA	70.41.1 70.42.1	Set Bkwd Read or Write	+MS Control 70.61.1	9.5 - 9.8	9.5 - 9.8
End Read Delay	70.41.1	End RD not RD15-RD28	Rise of Go 70.71.1	1.5 - 1.7	2.8 - 3.0
		End RD Bkwd RD12	Rise of Go 70.71.1	1.2 - 1.4	1.2 - 1.4
		End RD LP	Rise of Go 70.71.1	15.9-16.2	15.9-16.2
Bksp Reset Read Cond	70.21.1	Reset RD Cond	+RDD 70.61.1	.69- .90	1.9 - 2.1
WD 215 + 320	70.42.1	End WD LP	Rise of Go 70.71.1	31.9-32.2	31.9-32.2
WD 32	70.81.1	Set Read Cond on Write	Rise of Go	3.2 - 3.4	3.2 - 3.4

NOTE 1: End WDD for 9-Track Mod 3 occurs at WDD 403
NOTE 2: WDD ends with the reset of write trigger release. Go falls with the set of 1st check char with Mod 1 or Mod 2.

Gate 01A, Panel 2 2400 Bit 9 0729 Bit 7		P C	0	1	2 B	3 A	4 8	5 4	6 2	7 1
Designation	Card									
Read Bus	01A2	B17E	B15E	B13E	B11E	B09E	B07E	B05E	B03E	B01E
2400 Preamps	01A1	F09	F08	F07	F06	F05	F04	F03	F02	F01
Read Delay Order*										
Yellow (Forward)	01A1	C09N	C08N	C07N	C06N	C05N	C04N	C03N	C02N	C01N
Black (Backward)	01A1	C09R	C08R	C07R	C06R	C05R	C04R	C03R	C02R	C01R
Write Delay Order**	01A1	F26A	F26C	F26B	F25D	F25A	F25C	F25B	F24A	F24B
Assymmetry	01A1	D29	D28	D27	D26	D25	D24	D23	D22	D21

* Read Delay Order: C Row A, B, C, D, E, F
** Write Delay Order: G23, G24, G25, G26, ABC, D, E, F, G, H, K, L, M, N, P, Q, R

NOTE: Mechanical skew, seven-track, use bits P and 7
Mechanical skew, nine-track, use bits 4 and 5

Commands

Command	Bit 0	1	2	3	4	5	6	7
Test I/O	0	0	0	0	0	0	0	0
Sense	0	0	0	0	0	1	0	0
No-op	0	0	0	0	0	0	1	1
Printer								
Write	X	X	X	X	X	0	0	1
Control (Skip Space)	X	X	X	X	X	0	1	1
Read (1404)	1	1	0	0	0	0	1	0
Reader								
Read	Y	Y	Y	0	0	0	1	0
Control (Feed)	Y	Y	Y	0	0	0	1	1
Punch								
Write	Z	Z	Z	0	0	0	0	1
Read (Punch Feed Read)	Z	Z	0	0	0	0	1	0

Modifiers

Printer	Bit X 0	X 1	X 2	X 3	X 4
Space 1	0	0	0	0	1
Space 3	0	0	0	1	1
Skip to Chan 1	1	0	0	0	1
Skip to Chan 12	1	1	1	0	0

On Write, Carriage Operation is after Print. On Control, it is immediate.

Reader	Bit Y 0	Y 1	Y 2
Data Mode 1 (Read)	Y	Y	0
Data Mode 2 (Read)	Y	Y	1
Read & Feed & Stacker R1	0	0	Y
Read & Feed & Stacker R2	0	1	Y
Read & Feed & Stacker RP3	1	0	Y
Read (No Feed No Stacker Sel)	1	1	Y
Feed & Stacker R1 (Control)	0	0	1
Feed & Stacker R2 (Control)	0	1	1
Feed & Stacker RP3 (Control)	1	0	1

	Bit		
	Z	Z	Z
Punch	0	1	2
Data Mode 1 (Write)	Z	Z	0
Data Mode 2 (Write)	Z	Z	1
Write & Feed & Stacker P1	0	0	Z
Write & Feed & Stacker P2	0	1	Z
Write & Feed & Stacker P3	1	0	Z

Status Byte

Bit	Name	Description
0	Not Used	
1	Not Used	
2	Not Used	
3	Busy	
4	Channel End	
5	Device End	
6	Unit Check	Further defined by Sense Byte
7	Unit Exception	Reader--last card Read and Stacked Printer--Channel 12 sensed-- further defined by Sense Byte

Sense Byte

Bit	Name	Description
0	Command Reject	
1	Intervention Required	Not Ready
2	Bus Out Parity	Parity of command on Bus Out
3	Equipment Check	Parity Error in Control Unit or Device
4	Data Check	On Reader Invalid Card Code. On PFR also.
5	UCS Parity	Printer UCS Parity Error.
6		Reader 2 reads no feed. Punch Only PFR. Printer Channel 9.
7		Reader Punch--not used. Printer--Channel 9

Commands

Command Type	Command Name	Hex Code	
		Single Track	Multi-Track
Control	Seek (BB CC HH)	07	--
	Seek Cylinder (CC HH)	0B	--
	Seek Head (HH)	1B	--
	Recalibrate	13	--
	No Operation	03	--
	Set File Mask	1F	--
	Space Count	0F	--
	Restore (2321 only)	17	--
Sense	Test I/O	00	--
	Sense I/O	04	--
Read	Read Data	06	86
	Read Key-Data	0E	8E
	Read-Count-Key-Data	1E	9E
	Read Home Address	1A	9A
	Read R0	16	96
	Read Count	12	92
	Read IPL	02	--
Write	Write Data	05	--
	Write Key-Data	0D	--
	Write-Count-Key-Data	1D	--
	Write Home Address	19	--
	Write R0	15	--
	** Write (Special) Count-Key-Data	01	--
	Erase	11	--
Search	Search Equal ID	31	B1
	Search High ID	51	D1
	Search Equal-Hi-ID	71	F1
	Search Equal Key	29	A9
	Search High Key	49	C9
	Search Equal-Hi Key	69	E9
	Search Equal HA	39	B9
	*** Search Equal Key Data	2D	AD
	*** Search High Key Data	4D	CD
	*** Search Hi-Eq Key Data	6D	ED
	**** Continue Scan Equal	25	A5
	**** Continue Scan High	45	C5
	**** Continue Scan Hi Eq	65	E5
	**** Continue Scan, No Compare	55	D5
	**** Continue Scan, Set Compare	75, 35	F5, B5
Switching	* Reserve Device	B4	--
	* Release Device	94	--

* Special feature used with Two-Channel Switch.

** Special feature used with Record Overflow.

*** Special feature used with File Scan.

**** Used with File Scan with Record Overflow.

Seek Address

Type	Cell Number		Cylinder Number		Head Number	
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
2311	0	0	0	0-202	0	0-9
2302 Models 3 and 4	0	0	0	0-249	0	0-45
2303	0	0	0	0-79	0	0-9
2321	0	0-9	0-19 Subcell	0-9 Strip	0-4 Bar	0-19 Head No.
2314	0	0	0	0-202	0	0-19

File Protection

The significance of the file mask bits is:

B0	B1	
0	0	Inhibit Write Home Address and Write R0
0	1	Inhibit all write commands
1	0	Inhibit Write Home Address - Inhibit Write R0 - Inhibit Write Count, Key, and Data
1	1	Permit all write commands

B3	B4	
0	0	Permit all seek and restore commands
0	1	Permit Seek CCHH and HH CCWs
1	0	Permit Seek HH CCW
1	1	Inhibit all seek commands

B2	B5	B6	B7
0	0	0	0

Status Byte

Bit	Name	Note
0	Attention	Not Used
1	Status Modifier	Used with Search and Control Unit Busy.
2	Control Unit End	The control unit has finished an operation.
3	Busy	Indicates addressed access mechanism is moving; or used in conjunction with Status Modifier to indicate Control Unit Busy.
4	Channel End	The control unit has received all the data from the channel needed to do the operation called for and the channel is freed.
5	Device End	Indicates that an access mechanism is free to be used.
6	Unit Check	Indicates that a control unit or programming error or device hardware check has been detected.
7	Unit Exception	End-of-File.

Sense Information Summary

Sense Bit:
Position — Condition

Byte 0
Bit

0	Command Reject includes Invalid Command, Invalid Sequence, and File Protected.
1	Intervention Required
2	Bus Out Parity
3	Equipment Check
4	Data Check
5	Overrun
6	Track Condition Check
7	Seek Check

Byte 1
Bit

0	Data check in count field; also causes Byte 0, Bit 4 (Data Check) to be turned on.
1	Track Overrun. Indicated on Write.
2	End of Cylinder
3	Invalid Sequence also causes Command Reject (Byte 0, Bit 0) to be turned on.
4	No Record Found
5	File Protected also causes Command Reject (Byte 0, Bit 0)
6	Missing Address Marker also causes Data Check (Byte 0, Bit 4)
7	Overflow Incomplete

Byte 2
Bit

0	Unsafe	
1	Not Used	
2	Serializer/Deserializer Check	Also turn on Equipment Check Byte 0, Bit 3
3	Not Used	
4	ALU Check	
5	Unselected Status	

Byte 3

Bit	2311	2321	2302	2303	2314
0	Ready	Drive Ready	Access Ready		Busy
1	On Line	Drive Operative	Access Operative		On Line
2	Unsafe	Read Safety	Read Safety		Unsafe
3	----------	Write Safety	Write Safety		Not Used
4	On Line	Strip Ready	On Line	On Line	Pack Change
5	End of Cylinder	Invalid Address	----------		End of Cylinder
6	----------	Auto Restore	----------		Not Used
7	Seek Incomplete	CE Cell Located	CE Cylinder Located		Seek Incomplete

Byte 4

This byte is all zeros. It is included for compatibility with other control units.

Sense Information Summary (Continued)

Byte 5

This byte is zero at all times except when overflow incomplete occurs (Byte 1, Bit 7). When overflow incomplete occurs, this byte has one of the following configurations:

00000110 - A read command was in progress when the overflow incomplete interrupt occurred.

00000101 - A non-formating write command was in progress.

00100101 - A search equal key data command was in progress, and the compare is equal to this point.

01000101 - A search high key data command was in progress, and the compare is equal to this point.

01100101 - A search high or equal key data command was in progress, and the compare is equal to this point.

01010101 - Any search key data was in progress and the compare is low, or a search equal key data was in progress and the compare is unequal to this point (i. e., it has already been determined that no status modifier would be set on the entire logical record.)

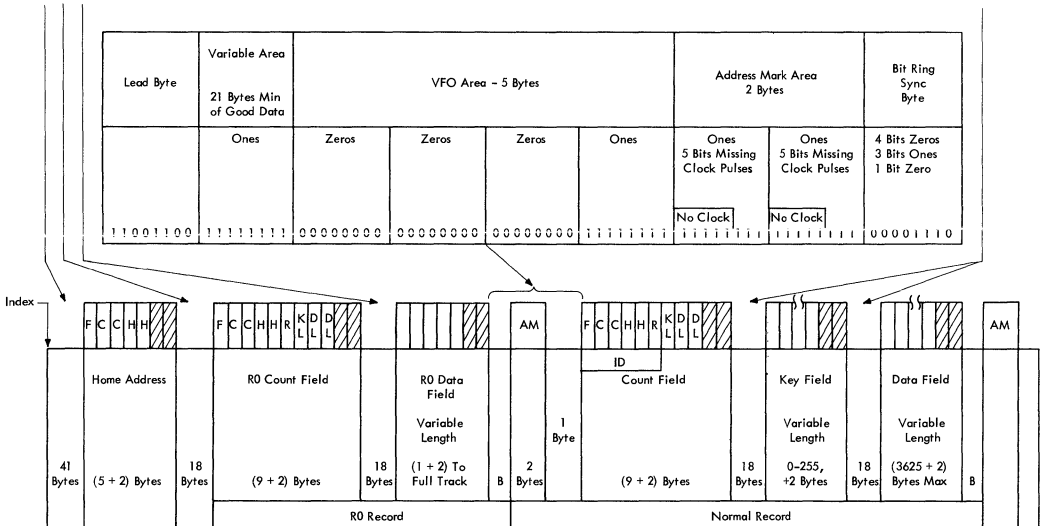
01110101 - A search high or high-equal key data command was in progress, and the compare is high to this point (i.e., it has already been determined that a status modifier would be set on the logical record).

Data Format (2302)

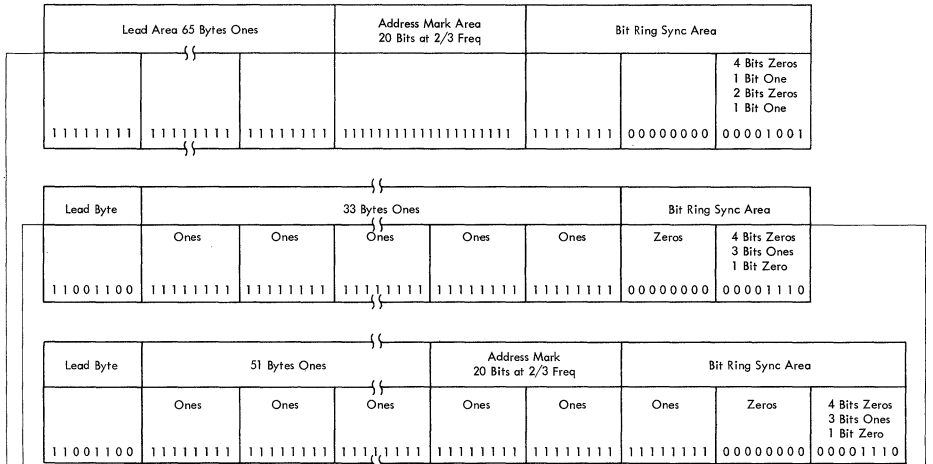
Lead Area - 36 Bytes			VFO Area - 4 Bytes				Bit Ring Sync Area 1 Byte
Zeros	Zeros	Zeros	Zeros	Zeros	Zeros	Ones	4 Bits Zeros 3 Bits Ones 1 Bit Zero
00000000	00000000	00000000	00000000	00000000	00000000	11111111	00001110

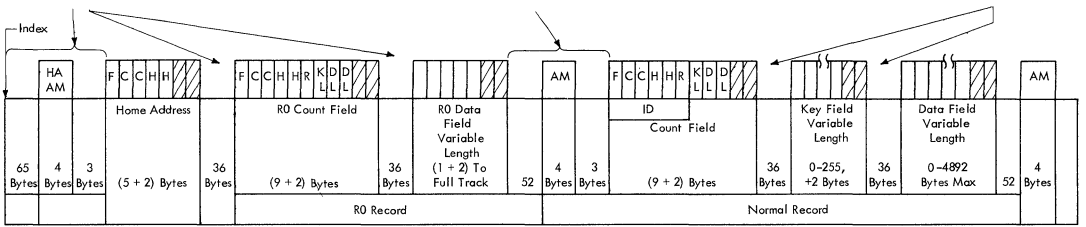
Lead Byte	Lead Area - 12 Zeros		VFO Area - 4 Bytes				Bit Ring Sync Area 1 Byte
	Zeros	Zeros	Zeros	Zeros	Zeros	Ones	4 Bits Zeros 3 Bits Ones 1 Bit Zero
11001100	00000000	00000000	00000000	00000000	00000000	11111111	00001110

Lead Byte	Lead Area - 9 Ones		VFO Area - 7 Bytes				Bit Ring Sync Area 1 Byte
			6 Bytes Zeros				
	Ones	Ones	Zeros	Zeros	Zeros	Ones	4 Bits Zeros 3 Bits Ones 1 Bit Zero
11001100	11111111	11111111	00000000	00000000	00000000	11111111	00001110

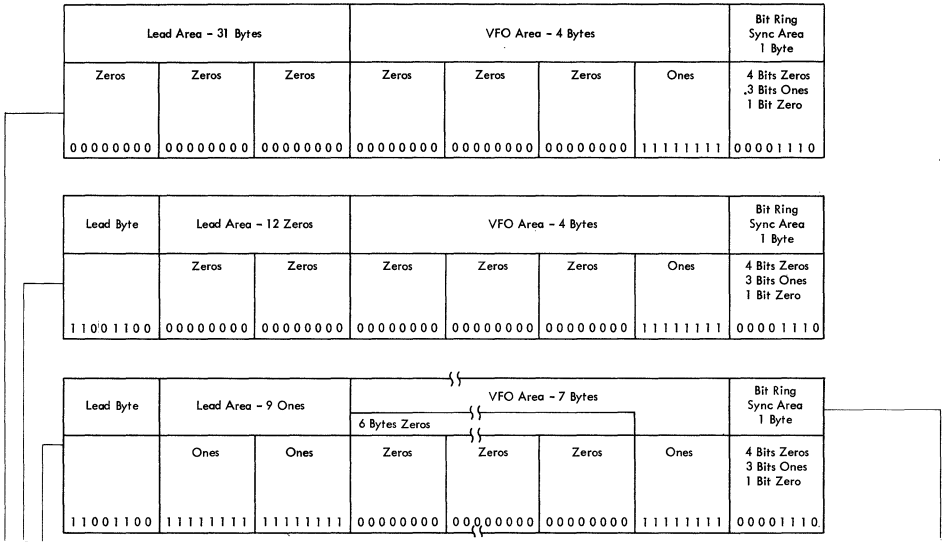

Lead Byte
Variable Area
21 Bytes Min of Good Data
VFO Area – 5 Bytes
Address Mark Area 2 Bytes
Bit Ring Sync Byte
Ones
Zeros
Zeros
Zeros
Ones
Ones 5 Bits Missing Clock Pulses
Ones 5 Bits Missing Clock Pulses
4 Bits Zeros 3 Bits Ones 1 Bit Zero
No Clock
No Clock
11001100
11111111
00000000
00000000
00000000
11111111
11111111
11111111
00001110
Index
F C C H H
F C C H H R K L D L D L
AM
F C C H H R K L D L D L
AM
ID
Home Address
R0 Count Field
R0 Data Field
Variable Length
1 Byte
Count Field
Key Field
Variable Length
Data Field
Variable Length
41 Bytes
(5 + 2) Bytes
18 Bytes
(9 + 2) Bytes
18 Bytes
(1 + 2) To Full Track
B
2 Bytes
(9 + 2) Bytes
18 Bytes
0–255, +2 Bytes
18 Bytes
(3625 + 2) Bytes Max
B
R0 Record
Normal Record

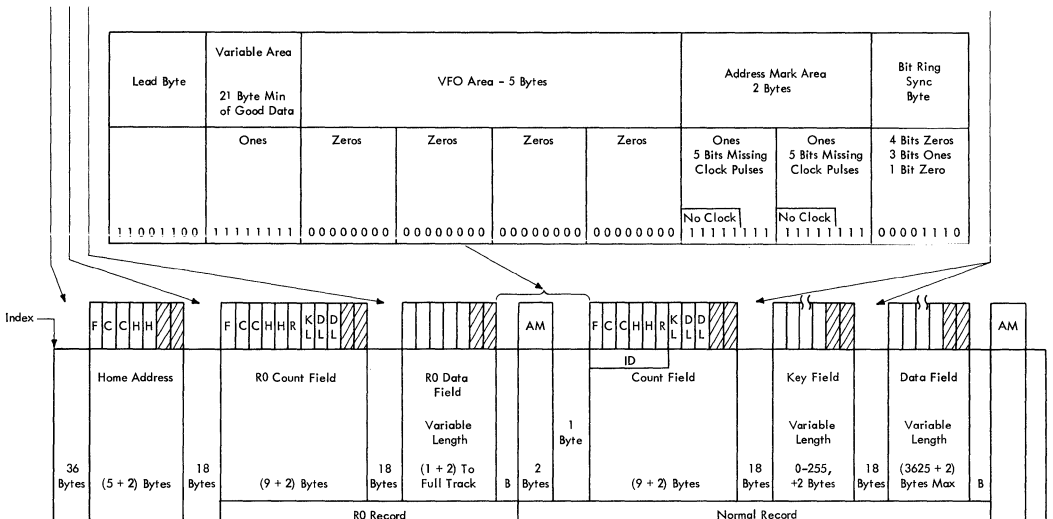
Data Format (2303)



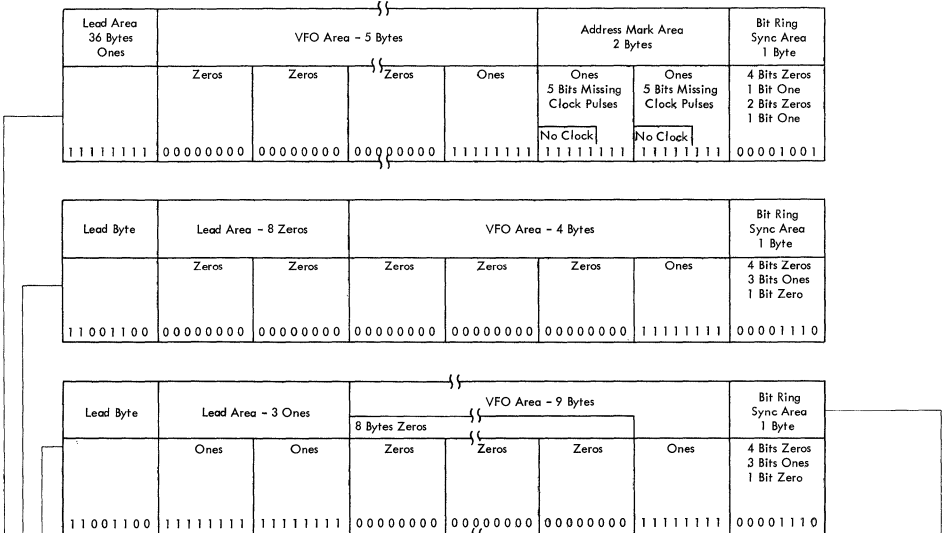

Index
HA AM
F C C H H
Home Address
R0 Count Field
F C C H H R K D D L L L
R0 Data Field Variable Length (1 + 2) To Full Track
AM
F C C H H R K D D L L L
ID
Count Field
Key Field Variable Length
Data Field Variable Length
AM
65 Bytes
4 Bytes
3 Bytes
(5 + 2) Bytes
36 Bytes
(9 + 2) Bytes
36 Bytes
52
4 Bytes
3 Bytes
(9 + 2) Bytes
36 Bytes
0-255, +2 Bytes
36 Bytes
0-4892 Bytes Max
52
4 Bytes
R0 Record
Normal Record

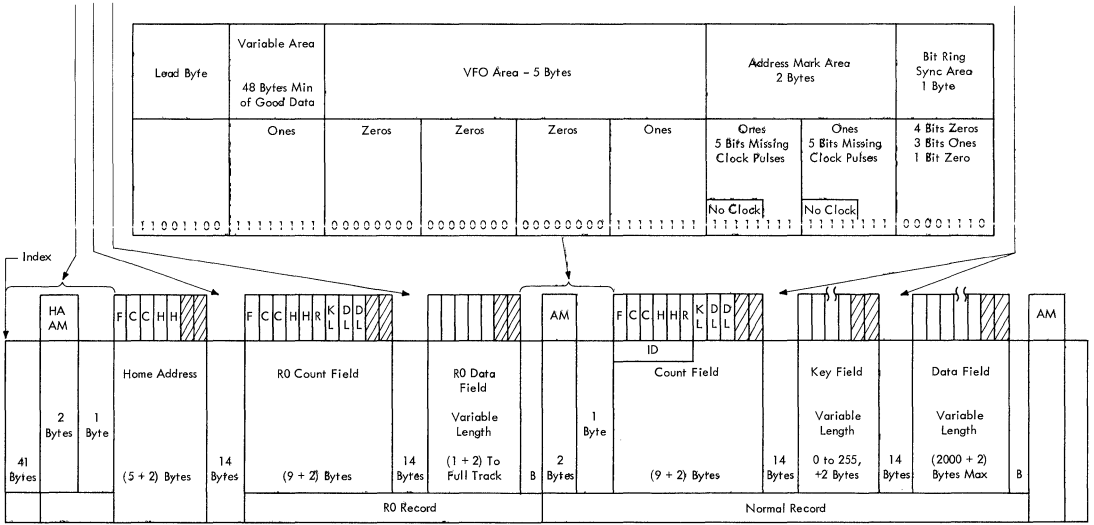
Data Format (2311)




Lead Byte
Variable Area
21 Byte Min of Good Data
VFO Area - 5 Bytes
Address Mark Area 2 Bytes
Bit Ring Sync Byte
Ones
Zeros
Zeros
Zeros
Zeros
Ones 5 Bits Missing Clock Pulses
Ones 5 Bits Missing Clock Pulses
4 Bits Zeros 3 Bits Ones 1 Bit Zero
No Clock
No Clock
11001100
11111111
00000000
00000000
00000000
00000000
11111111
11111111
00001110
Index
F C C H H
F C C H H R K L D L
AM
F C C H H R K L D L
ID
AM
Home Address
R0 Count Field
R0 Data Field
Variable Length
Count Field
Key Field
Variable Length
Data Field
Variable Length
1 Byte
36 Bytes
(5 + 2) Bytes
18 Bytes
(9 + 2) Bytes
18 Bytes
(1 + 2) To Full Track
B
2 Bytes
(9 + 2) Bytes
18 Bytes
0-255, +2 Bytes
18 Bytes
(3625 + 2) Bytes Max
B
R0 Record
Normal Record

Data Format (2321)




Lead Byte
Variable Area
48 Bytes Min of Good Data
VFO Area – 5 Bytes
Address Mark Area 2 Bytes
Bit Ring Sync Area 1 Byte
Ones
Zeros
Zeros
Zeros
Ones
Ones 5 Bits Missing Clock Pulses
Ones 5 Bits Missing Clock Pulses
4 Bits Zeros 3 Bits Ones 1 Bit Zero
No Clock
No Clock
11001100
11111111
00000000
00000000
00000000
11111111
11111111
11111111
00001110
Index
HA AM
F C C H H
F C C H H R K L D D L
AM
F C C H H R K L D D L
AM
ID
41 Bytes
2 Bytes
1 Byte
Home Address
(5 + 2) Bytes
14 Bytes
R0 Count Field
(9 + 2) Bytes
14 Bytes
R0 Data Field
Variable Length
(1 + 2) To Full Track
B
2 Bytes
1 Byte
Count Field
(9 + 2) Bytes
14 Bytes
Key Field
Variable Length
0 to 255, +2 Bytes
14 Bytes
Data Field
Variable Length
(2000 + 2) Bytes Max
B
R0 Record
Normal Record

Data Format (2314)

Lead Byte (Except HA)	Variable Area		VFO Area - 5 Bytes			AM Area - 2 Bytes		Bit Ring Sync Area 1 Byte
204_{10}	Ones	Ones	Zeros	Zeros	Ones	Ones 5 Bits Missing Clock Pulses	Ones 5 Bits Missing Clock Pulses	See Below
1 1 1 0 1 1 0 0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	

Bit Ring Sync Byte Configuration

HA Sync Byte	R0 Count Sync Byte	R0 Data Sync Byte	RN Count Sync Byte	Key Sync Byte	RN Data Sync Byte
13_{10}	11_{10}	9_{10}	14_{10}	10_{10}	9_{10}
0 0 0 0 1 1 0 1	0 0 0 0 1 0 1 1	0 0 0 0 1 0 0 1	0 0 0 0 1 1 1 0	0 0 0 0 1 0 1 0	0 0 0 0 1 0 0 1

Index

	Home Address		R0 Count Field		R0 Data Field		Count Field		Key Field		Data Field	
F C C H H B B			F C C H H R K D D B B		B B		F C C H H R K D D B B		B B		B B	
73 Bytes	(5 + 2) Bytes	45 Bytes	(9 + 2) Bytes	43 Bytes	Variable (8 + 2) To Full Track	G0	(9 + 2) Bytes	43 Bytes	0-255 Bytes	43 Bytes	7294 Max Bytes	GN

G0 = 45 bytes if R0 Data Length is 8 bytes
G0 = 45 + 0.043 (DL) if R0 Data Length 8 bytes
GN = 45 + 0.043 (KL + DL)

Commands

Command Format	Bit 0	1	2	3	4	5	6	7
Test I/O	0	0	0	0	0	0	0	0
*Write (Including Read Checking)	0	0	M	M	0	M	0	1
*Read	0	0	0	M	0	0	1	0
*Read Backward	0	0	0	M	1	1	0	0
Sense	0	0	0	0	0	1	0	0
Control	0	0	C	C	C	C	1	1
No Operation (does not reset Sense)	0	0	0	0	0	0	1	1
Set Density (Reset Sense bits)	0	D	Ø	1	Ø	0	1	1
Tape Positioning								
Backspace	0	0	1	0	0	1	1	1
Backspace File	0	0	1	0	1	1	1	1
Space	0	0	1	1	0	1	1	1
Space File	0	0	1	1	1	1	1	1
**Rewind	0	0	0	0	0	1	1	1
Cartridge Operations								
**Rewind and Change Cartridge	0	0	0	0	1	1	1	1
**Change Cartridge and Rewind	0	0	0	0	1	0	1	1
**Change Cartridge	0	0	1	0	0	0	1	1
**File Protect On	0	0	1	0	1	0	1	1
Tape Demarcation								
Erase Long Gap	0	0	0	1	0	1	1	1
Write Tape Mark	0	0	0	1	1	1	1	1

*These commands carry density and diagnostic-mode information coded in bits positions 0-5.
**Free-Running
M = Diagnostic Modifier
D = Density Modifier (1 = high or 3022 bpi density)
C = Control Operation Code
Ø = Ignored, may be 0 or 1

Diagnostic Modifiers

	Bit Position 0	1	2	3	4	5	Meaning
Read or Read-backward	0	0	0	1	0	0	Interrupt on Correctable Error
	0	0	0	0	0	0	No Interrupt on Correctable Error
Write	0	0	0	0	0	0	Write Start-Stop
	0	0	0	0	0	1	Write Continuous
	0	0	1	0	0	0	*‡Write Clock Fast - On
	0	0	0	0	0	0	Write Clock Fast - Off
	0	0	0	1	0	0	*Loop Write to Read - On
	0	0	0	0	0	0	Loop Write to Read - Off

* Diagnostic modifier

‡ Forces Loop Write to Read On

Sense Bits

Byte 0, Bit 0 - Command Reject is set when:

A Write, WTM, or Erase Command is addressed to a File Protected Drive or a drive at EOT (End of Tape)

A Read, Space, Space File or Read Backward Command is addressed to a tape drive at EOT (End of Tape)

A Read Backward, Backspace Record, or Backspace File is addressed to tape drive at BOT (Beginning of Tape)

Any tape motion into either BOT or EOT occurs, except during a free-running operation.

Byte 0, Bit 1 - Intervention Required is set when:

A command other than Sense, Test I/O, or Write with a Loop Write to Read modifier bit is addressed to a tape drive that is Not Ready or Nonexistent.

The 2802 could not properly perform the previous command and will not be able to do so until some sort of manual intervention is performed. For example, Change Cartridge to a drive without a Ready Cartridge Loader.

Byte 0, Bit 2 - Bus-Out Check is set when a parity error is detected on Bus-Out except during Address Out.

Byte 0, Bit 3 - Equipment Check is set whenever improper machine functioning is detected. This includes improper response from the drive to control unit commands.

Byte 0, Bit 4 - Data Check is set whenever any Sense Byte 3 bit other than 5 or 6 is set, and whenever any byte 3 is set when an "Interrupt on Correctable Error" modifier is effective.

Byte 0, Bit 5 - Overrun is set during a Read, Read Backward, or Write Operation whenever the channel does not respond to a Service In within the allotted time. Overrun cannot occur during a Sense, Control, or Test I/O operation.

Byte 0, Bit 6 - Word Count Zero is set during a Write Operation when the operation has been terminated without any byte of data transferred between the 2802 and the channel.

Byte 0, Bit 7 - Spare

Byte 1, Bit 0 - Selected Drive at EOT is set whenever the Selected drive indicates End of Tape.

Byte 1, Bit 1 - Selected TD Status A and B will be set to the condition of tape drive status lines that are used to decide the responses to Initial Selection. The bits reflect the status of the drive at the moment Sense Byte 2 is assembled. The meanings and the responses during Initial Selection are listed below:

TD Status A (Sel and Rdy)	TD Status B (Not Rdy or Busy or Switched*)	TD Status	Response to Initial Selection
0	0	Non existent TD	Unit Check
0	1	Not Ready	Unit Check-Arm for Device End
1	0	Ready, Not Busy, Not Switched	Clean Status
1	1	Ready and (Busy or Switched)	Busy-Arm for Device End

* Switched indicates the TD is selected by some other Control Unit under control of a Tape Unit Switch.

Note: The following bits refer only to the Selected drive which may or may not be the drive referred to by the remaining status.

Byte 1, Bit 3 - Spare

Byte 1, Bit 4 - Selected Drive at BOT is set whenever the Selected drive indicates Beginning of Tape.

Byte 1, Bit 5 - Selected Drive in Write Status is set whenever the Selected drive indicates Write Status.

Byte 1, Bit 6 - Selected Drive File Protected is set whenever the Selected drive indicates that the currently loaded cartridge is File Protected.

Byte 1, Bit 7 - Selected Drive in EWA is set whenever the Selected drive indicates End of Warning Area.

Byte 2, Bits 0, 1, and 7 - Spares

Byte 2, Bits 2-6 - These Data Check Detail bits are set whenever:
The last drive operation was Write, Read, or Read Backward.
An error (s) has occurred as defined in the section of the 2802 specifications describing these commands.

Byte 3, Bits 0-5 - Reserved for diagnostic information.

Byte 3, Bit 6 - Last Operation Low Density will be set whenever the last operation affecting the tape drive included a Low Density modifier. If the last drive operation was a Control, this bit will never be present since low density is not specified for Control. If the last drive operation was a Read or Write, this bit will reflect the density setting at which the operation was performed.

Byte 3, Bit 7 - IRG Control Latch On is set whenever a Write Continuous is programmed and remains on as long as program reinstruct is possible. This bit is included so that the timing of the reinstruct singleshot can be checked by program means to insure that it is not too short, which will shorten the program reinstruct interval, nor too long, which exceeds the specification of the tape drive.

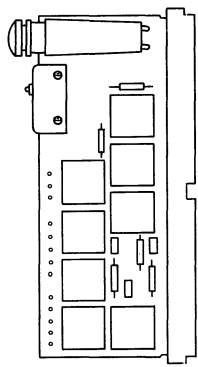
CE INDICATOR LATCH CARD

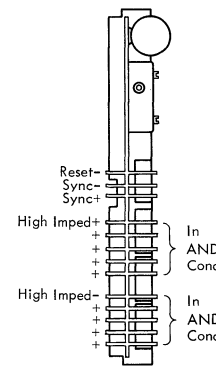
The CE indicator latch card P/N 5801358 can be used for two purposes:

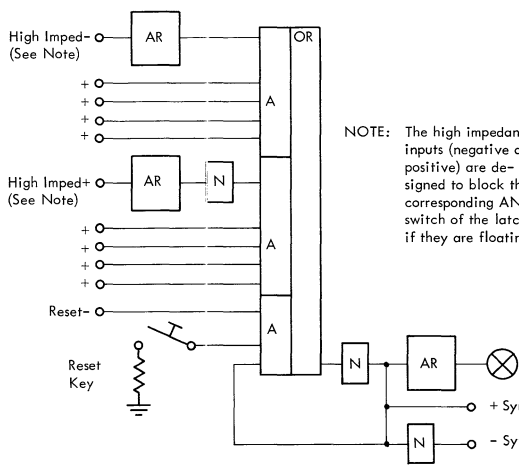
1. As a monitor to detect erroneous pulses and/or conditions

2. As an AND switch to select a sync signal for a scope

The latch on the card can be set by either negative or positive levels. A reset key is provided on the card so that the latch can be reset manually if desired. If the Indicator Latch card is to be used as an AND switch to select a certain sync signal for scoping, a reset signal must be provided to ensure correct triggering of the scope.







NOTE: The high impedance inputs (negative and positive) are designed to block the corresponding AND-switch of the latch if they are floating.

INTERRUPT CONDITIONS

I. Channel Working (SIO started and now working)

Exec. Inst.	CC	CSW Stored?	Comments
SIO any CU	2	No	No I/O opn starts
TIO any CU	2	No	No status transfers
HIO any CU	2	No	Irpts after halting current operation.
TCH	2	No	Status per CC (burst)

II. Channel End Pending *Channel Masked Off

*SIO any CU	2	No	Chan won't start I/O opn and will not clear the Irpt
TIO (to unit pending)	1	Yes	Clear Irpt store entire CSW
*TIO (other CU)	2	No	Chan untouched
HIO (any CU)	0	No	Chan stopped already
TCH	1	No	CC says Irpt pending

*Note: Dev End can be stacked back to device level on SIO, TIO (to other) so operation can start, CC = 0

III. Channel Clear Device End In Device

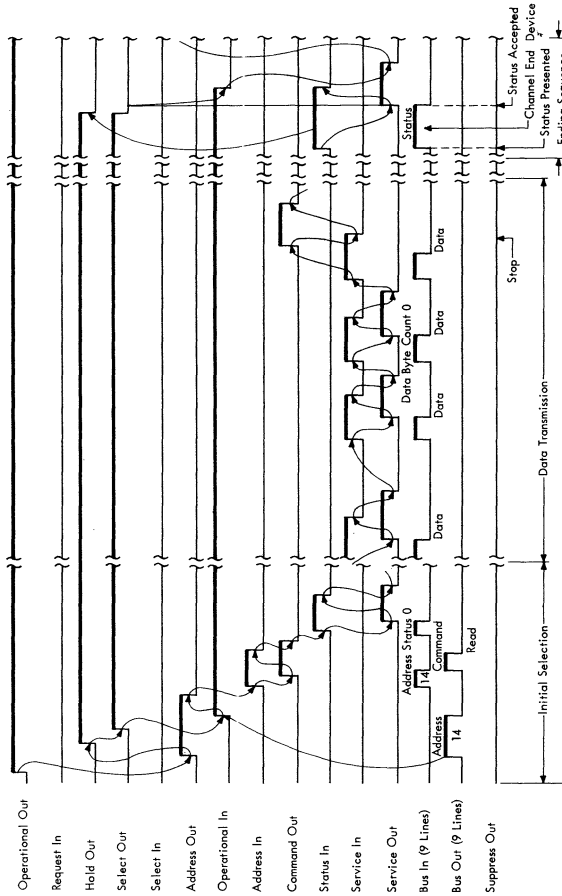
SIO (to unit 1 pending)	1	Yes (busy bit)	No I/O opn starts; Irpt is cleared
SIO (to other unit or dev)	0	No	I/O opn starts
TIO (to unit pending)	1	Yes	Irpt cleared
TIO (other unit or CU)	0	No	
HIO (any CU)	1	Yes	All Zero status
TCH	0	No	Under these conditions normally Device Poll Irpt

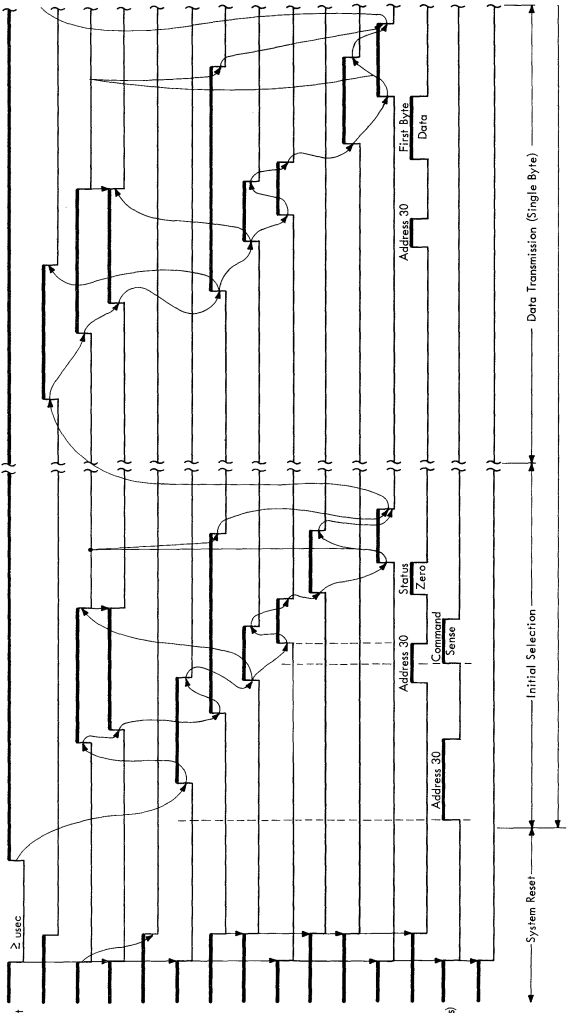
IV. Channel Clear but Irpt Pending in CU
(Dev End with other cond (unit check, etc)

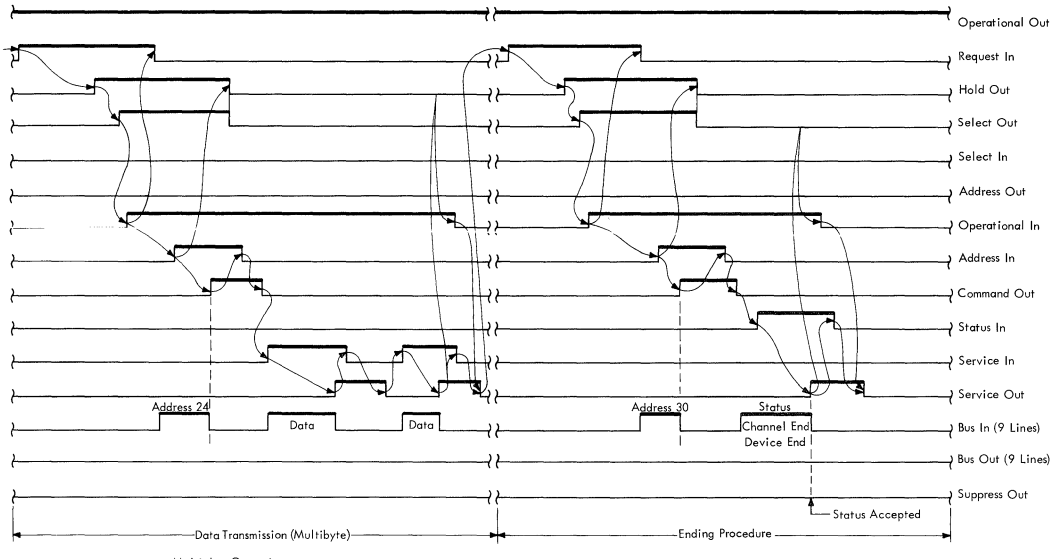
SIO (unit pending)	1	Yes (busy bit)	No I/O opn starts, but clears Irpt
SIO (to other dev same CU)	1	Yes	Status says CU busy
SIO (other CU)	0	No	I/O opn starts
TIO (Device pending)	1	Yes	Clear Irpt
TIO (other dev same CU)	1	Yes (busy bit)	Status says CU busy
TIO (other CU)	0	No	

V. Polling Interrupt In Channel (No Irpt Response from CPU yet)

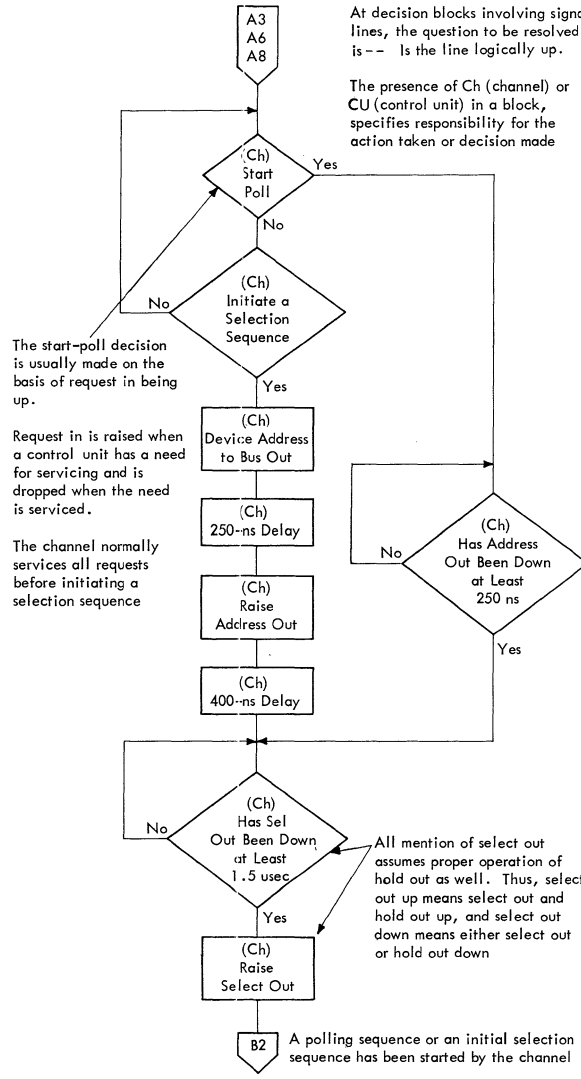
SIO, TIO, HIO } Any of these starting cause polled in status to be stacked back into the CU. (Command Out response to the Status In)


Operational Out
Request In
Hold Out
Select Out
Select In
Address Out
Operational In
Address In
Command Out
Status In
Service In
Service Out
Bus In (9 Lines)
Bus Out (9 Lines)
Suppress Out
Address 14
Command Read
Status 0
Data
Data Byte Count 0
Status
Stop
Status Accepted
Channel End
Device End
Status Presented
Ending Sequence
Initial Selection
Data Transmission
Normal Input Operation Channel Forced Burst Mode Selector Channel


Operational Out
Request In
Hold Out
Select Out
Select In
Address Out
Operational In
Address In
Command Out
Status In
Service In
Service Out
Bus In (9 Lines)
Bus Out (9 Lines)
Suppress Out
≥ usec
Address 30
Address 30
Address 30
Status Zero
Command Sense
First Byte Data
System Reset
Initial Selection
Data Transmission (Single Byte)


Operational Out
Request In
Hold Out
Select Out
Select In
Address Out
Operational In
Address In
Command Out
Status In
Service In
Service Out
Bus In (9 Lines)
Bus Out (9 Lines)
Suppress Out
Address 24
Data
Data
Address 30
Status
Channel End
Device End
Status Accepted
Data Transmission (Multibyte)
Ending Procedure
Multiplex Operation

Initiation of Polling or Selection



At decision blocks involving signal lines, the question to be resolved is-- Is the line logically up.

The presence of Ch (channel) or CU (control unit) in a block, specifies responsibility for the action taken or decision made

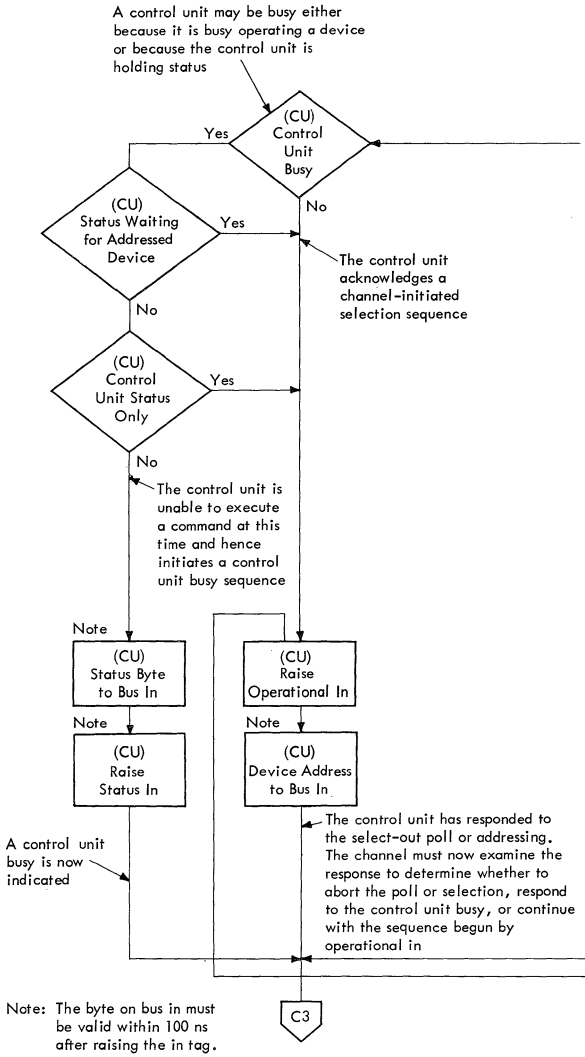
The start-poll decision is usually made on the basis of request in being up.

Request in is raised when a control unit has a need for servicing and is dropped when the need is serviced.

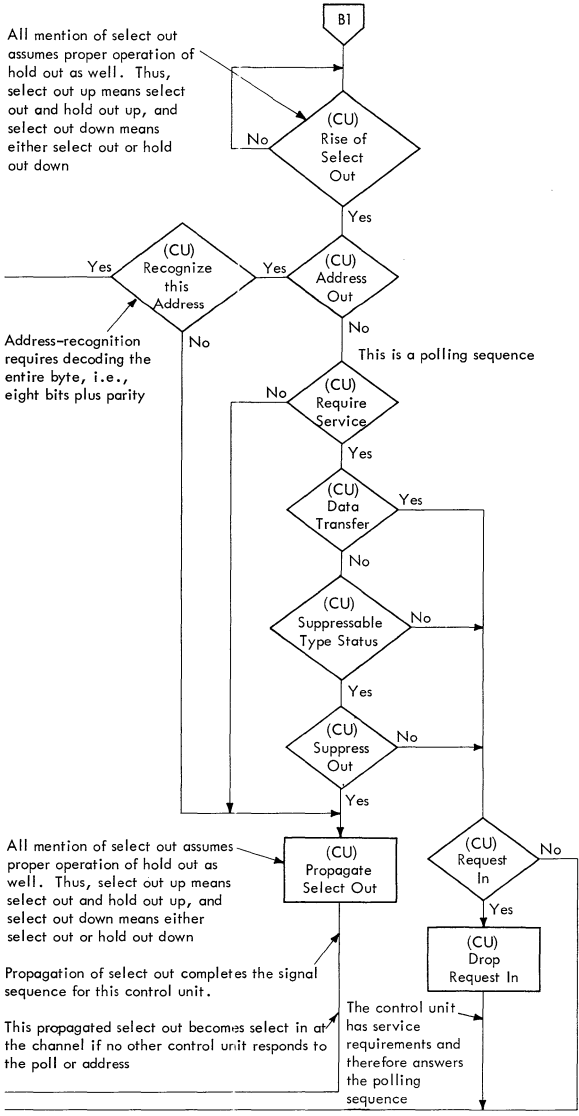
The channel normally services all requests before initiating a selection sequence

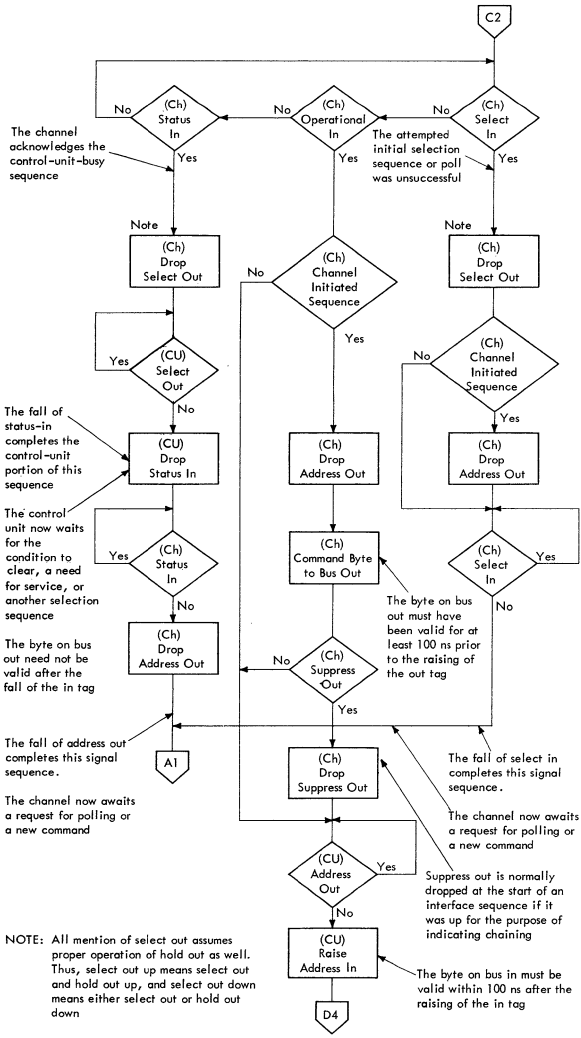
All mention of select out assumes proper operation of hold out as well. Thus, select out up means select out and hold out up, and select out down means either select out or hold out down

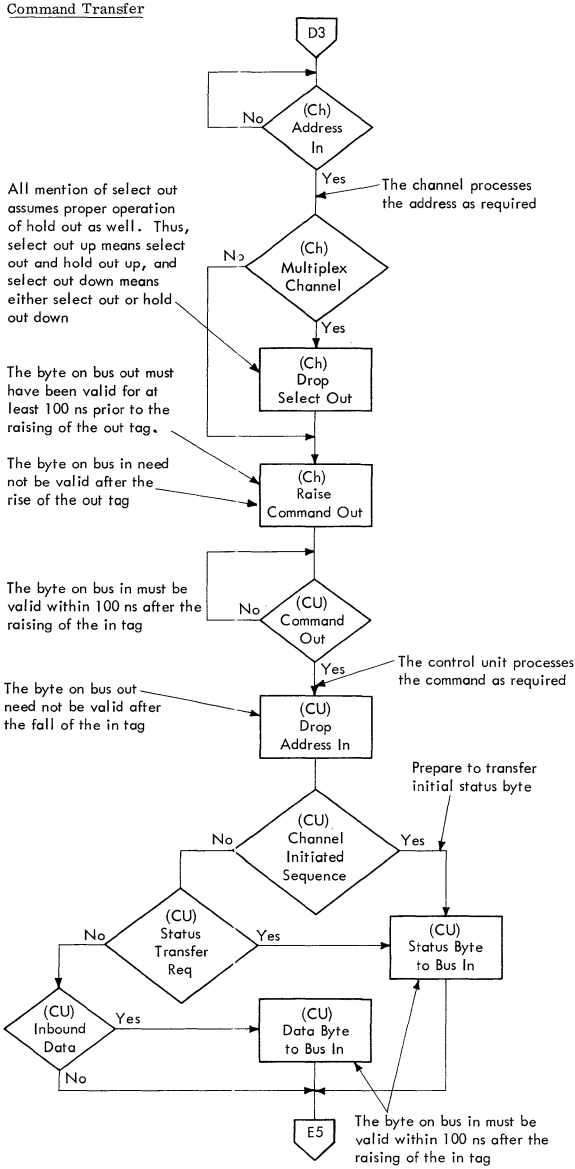
A polling sequence or an initial selection sequence has been started by the channel

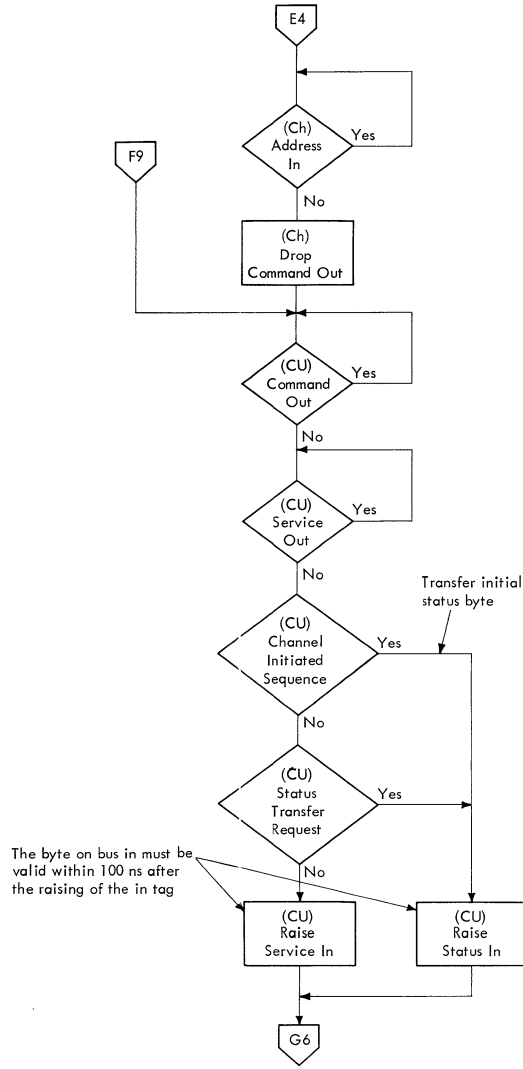


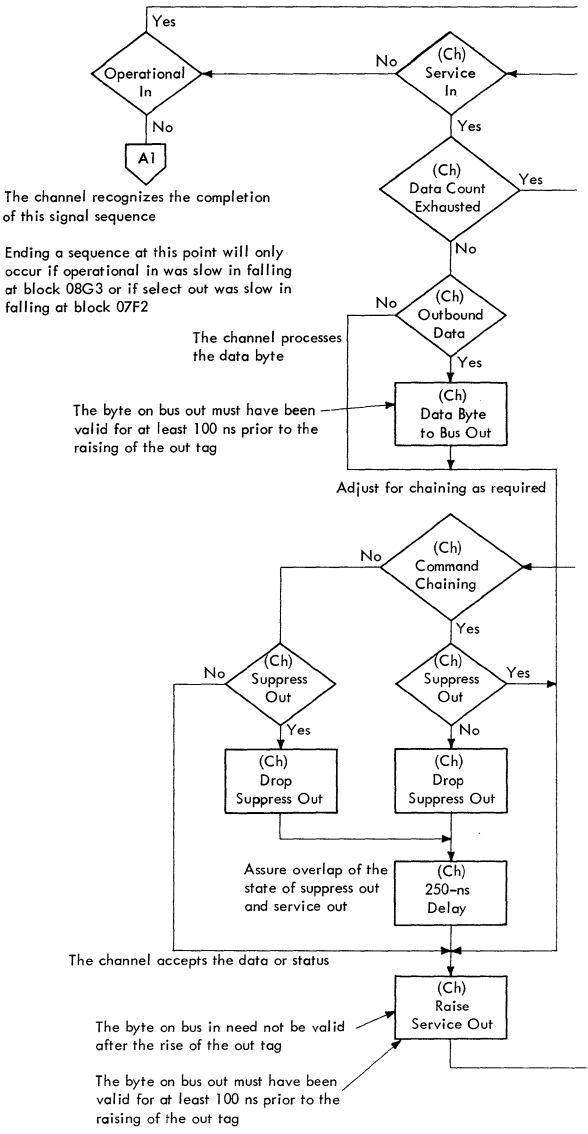
Note: The byte on bus in must be valid within 100 ns after raising the in tag.

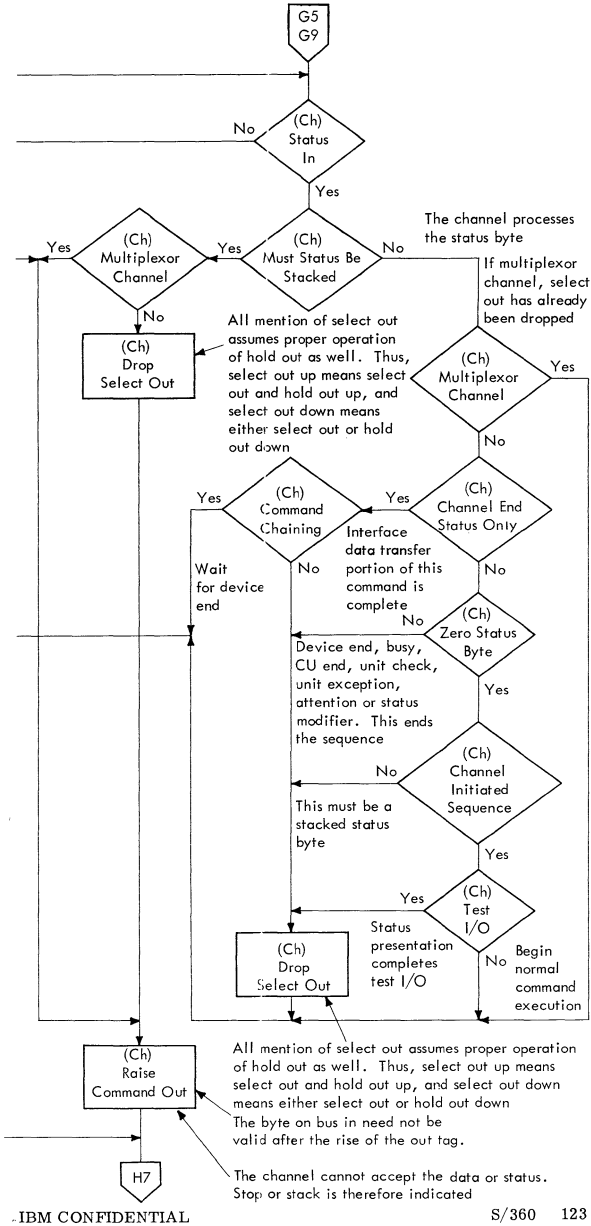

B1
All mention of select out assumes proper operation of hold out as well. Thus, select out up means select out and hold out up, and select out down means either select out or hold out down
(CU) Rise of Select Out
No
Yes
(CU) Address Out
Yes
(CU) Recognize this Address
Yes
No
Address-recognition requires decoding the entire byte, i.e., eight bits plus parity
This is a polling sequence
(CU) Require Service
No
Yes
(CU) Data Transfer
Yes
No
(CU) Suppressable Type Status
No
Yes
(CU) Suppress Out
No
Yes
All mention of select out assumes proper operation of hold out as well. Thus, select out up means select out and hold out up, and select out down means either select out or hold out down
(CU) Propagate Select Out
(CU) Request In
No
Yes
(CU) Drop Request In
Propagation of select out completes the signal sequence for this control unit.
This propagated select out becomes select in at the channel if no other control unit responds to the poll or address
The control unit has service requirements and therefore answers the polling sequence

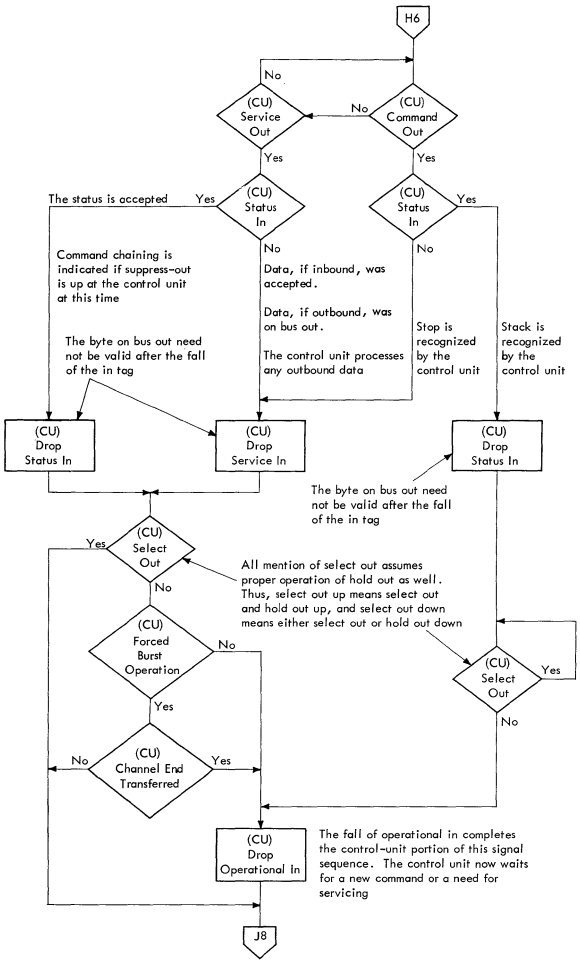

C2
(Ch) Status In
No
Yes
(Ch) Operational In
No
Yes
(Ch) Select In
No
Yes
The channel acknowledges the control-unit-busy sequence
The attempted initial selection sequence or poll was unsuccessful
Note
(Ch) Drop Select Out
(Ch) Channel Initiated Sequence
No
Yes
Note
(Ch) Drop Select Out
(CU) Select Out
Yes
No
(Ch) Channel Initiated Sequence
No
Yes
The fall of status-in completes the control-unit portion of this sequence
(CU) Drop Status In
(Ch) Drop Address Out
(Ch) Drop Address Out
The control unit now waits for the condition to clear, a need for service, or another selection sequence
(Ch) Status In
Yes
No
(Ch) Command Byte to Bus Out
(Ch) Select In
Yes
No
The byte on bus out must have been valid for at least 100 ns prior to the raising of the out tag
The byte on bus out need not be valid after the fall of the in tag
(Ch) Drop Address Out
(Ch) Suppress Out
No
Yes
The fall of address out completes this signal sequence.
A1
(Ch) Drop Suppress Out
The fall of select in completes this signal sequence.
The channel now awaits a request for polling or a new command
The channel now awaits a request for polling or a new command
(CU) Address Out
Yes
No
Suppress out is normally dropped at the start of an interface sequence if it was up for the purpose of indicating chaining
NOTE: All mention of select out assumes proper operation of hold out as well. Thus, select out up means select out and hold out up, and select out down means either select out or hold out down
(CU) Raise Address In
The byte on bus in must be valid within 100 ns after the raising of the in tag
D4

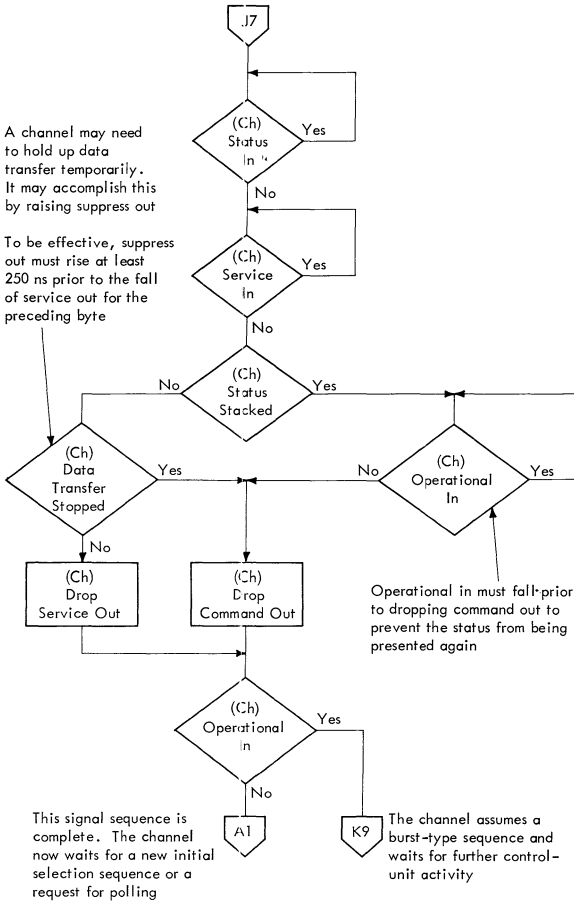

D3
(Ch) Address In
No
Yes
The channel processes the address as required
All mention of select out assumes proper operation of hold out as well. Thus, select out up means select out and hold out up, and select out down means either select out or hold out down
(Ch) Multiplex Channel
No
Yes
(Ch) Drop Select Out
The byte on bus out must have been valid for at least 100 ns prior to the raising of the out tag.
The byte on bus in need not be valid after the rise of the out tag
(Ch) Raise Command Out
The byte on bus in must be valid within 100 ns after the raising of the in tag
(CU) Command Out
No
Yes
The control unit processes the command as required
The byte on bus out need not be valid after the fall of the in tag
(CU) Drop Address In
Prepare to transfer initial status byte
(CU) Channel Initiated Sequence
No
Yes
(CU) Status Transfer Req
No
Yes
(CU) Status Byte to Bus In
(CU) Inbound Data
Yes
No
(CU) Data Byte to Bus In
E5
The byte on bus in must be valid within 100 ns after the raising of the in tag


E4
(Ch) Address In
Yes
No
F9
(Ch) Drop Command Out
(CU) Command Out
Yes
No
(CU) Service Out
Yes
No
Transfer initial status byte
(CU) Channel Initiated Sequence
Yes
No
(CU) Status Transfer Request
Yes
No
The byte on bus in must be valid within 100 ns after the raising of the in tag
(CU) Raise Service In
(CU) Raise Status In
G6

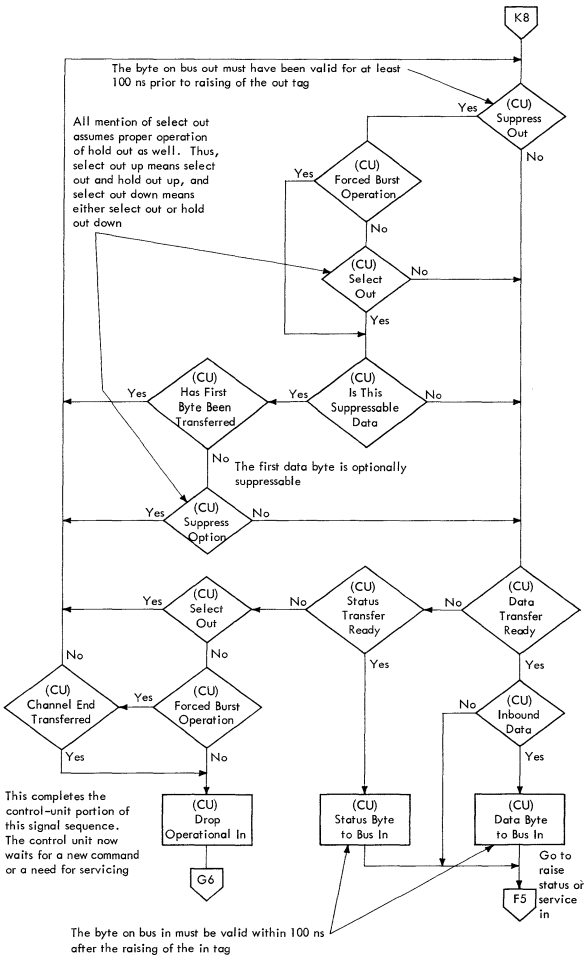

Yes
Operational In
No
A1
No
(Ch) Service In
Yes
(Ch) Data Count Exhausted
Yes
No
The channel recognizes the completion of this signal sequence
Ending a sequence at this point will only occur if operational in was slow in falling at block 08G3 or if select out was slow in falling at block 07F2
No
(Ch) Outbound Data
Yes
The channel processes the data byte
(Ch) Data Byte to Bus Out
The byte on bus out must have been valid for at least 100 ns prior to the raising of the out tag
Adjust for chaining as required
No
(Ch) Command Chaining
Yes
No
(Ch) Suppress Out
Yes
(Ch) Suppress Out
Yes
No
(Ch) Drop Suppress Out
(Ch) Drop Suppress Out
Assure overlap of the state of suppress out and service out
(Ch) 250-ns Delay
The channel accepts the data or status
(Ch) Raise Service Out
The byte on bus in need not be valid after the rise of the out tag
The byte on bus out must have been valid for at least 100 ns prior to the raising of the out tag


G5
G9
(Ch)
Status
In
No
Yes
(Ch)
Must Status Be
Stacked
Yes
No
The channel processes
the status byte
(Ch)
Multiplexor
Channel
Yes
No
If multiplexor
channel, select
out has already
been dropped
(Ch)
Drop
Select Out
All mention of select out
assumes proper operation
of hold out as well. Thus,
select out up means select
out and hold out up, and
select out down means
either select out or hold
out down
(Ch)
Multiplexor
Channel
Yes
No
(Ch)
Channel End
Status Only
Yes
No
(Ch)
Command
Chaining
Yes
No
Interface
data transfer
portion of this
command is
complete
Wait
for device
end
(Ch)
Zero Status
Byte
No
Yes
Device end, busy,
CU end, unit check,
unit exception,
attention or status
modifier. This ends
the sequence
(Ch)
Channel
Initiated
Sequence
No
Yes
This must be a
stacked status
byte
(Ch)
Test
I/O
Yes
No
Status
presentation
completes
test I/O
(Ch)
Drop
Select Out
Begin
normal
command
execution
(Ch)
Raise
Command Out
All mention of select out assumes proper operation
of hold out as well. Thus, select out up means
select out and hold out up, and select out down
means either select out or hold out down
The byte on bus in need not be
valid after the rise of the out tag.
H7
The channel cannot accept the data or status.
Stop or stack is therefore indicated

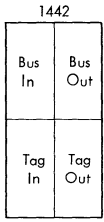

H6
No
(CU) Service Out
No
(CU) Command Out
Yes
Yes
The status is accepted
Yes
(CU) Status In
(CU) Status In
Yes
No
No
Command chaining is indicated if suppress-out is up at the control unit at this time
Data, if inbound, was accepted.
Data, if outbound, was on bus out.
The control unit processes any outbound data
Stop is recognized by the control unit
Stack is recognized by the control unit
The byte on bus out need not be valid after the fall of the in tag
(CU) Drop Status In
(CU) Drop Service In
(CU) Drop Status In
The byte on bus out need not be valid after the fall of the in tag
Yes
(CU) Select Out
All mention of select out assumes proper operation of hold out as well. Thus, select out up means select out and hold out up, and select out down means either select out or hold out down
No
(CU) Forced Burst Operation
No
(CU) Select Out
Yes
Yes
No
No
(CU) Channel End Transferred
Yes
(CU) Drop Operational In
The fall of operational in completes the control-unit portion of this signal sequence. The control unit now waits for a new command or a need for servicing
J8

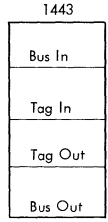

J7
(Ch) Status In
Yes
No
A channel may need to hold up data transfer temporarily. It may accomplish this by raising suppress out
To be effective, suppress out must rise at least 250 ns prior to the fall of service out for the preceding byte
(Ch) Service In
Yes
No
(Ch) Status Stacked
No
Yes
(Ch) Data Transfer Stopped
Yes
No
(Ch) Operational In
Yes
No
(Ch) Drop Service Out
(Ch) Drop Command Out
Operational in must fall prior to dropping command out to prevent the status from being presented again
(Ch) Operational In
Yes
No
This signal sequence is complete. The channel now waits for a new initial selection sequence or a request for polling
A1
K9
The channel assumes a burst-type sequence and waits for further control-unit activity

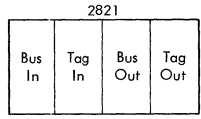
Burst Mode Waiting Loop

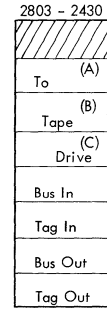


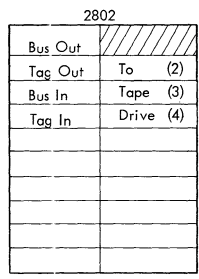
INTERFACE CONNECTORS

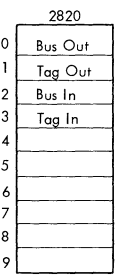


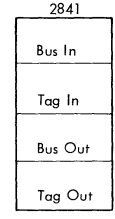


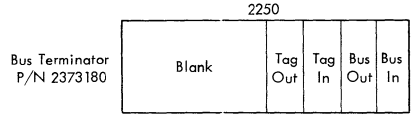












	B	D	Connector 1	Connector 2
2	O	O		
3	•	+3	Bus Out P	Operational In
4	O	•	Bus Out 0	Status In
5	•	O	Bus Out 1	Address In
6	-3	•	Bus Out 2	Service In
7	O	O		
8	•	O	Bus Out 3	Select In
9	O	•	Bus Out 4	Select Out
10	•	O	Bus Out 5	Address Out
11	+6	•	Bus Out 6	Command Out
12	•	O	Bus Out 7	Suppress Out
13	O	•		Service Out

O Ground Shield
• Signal

	G	J	Connector 1	Connector 2
2	O	O		
3	•	+3	Bus In P	Clock Out
4	O	•	Bus In 0	Metering Out
5	•	O	Bus In 1	Metering In
6	-3	•	Bus In 2	Request In
7	O	O		
8	•	O	Bus In 3	
9	O	•	Bus In 4	
10	•	O	Bus In 5	
11	+6	•	Bus In 6	
12	•	O	Bus In 7	Hold Out
13	O	•		Operational Out

Move Numerics	MVN	D1	SS	D1(L, B1), D2(B2)	The 4 low-order bits of opr 2 into the 4 low-order bits of opr 1. (Left to right byte by byte) (Max number of bytes moved: 256). (High-order bits of each byte of both opr's unchanged.) (No restriction on overlapping fields.)	Prot Adr	Unchanged
Move with Offset	MVO	F1	SS	D1(L1, B1), D2(L2, B2)	Opr 2 to the left of and adjacent to the low-order 4 bits of opr 1. (Right to left byte by byte) (Data can be packed, unpacked, or binary format) (No restriction on overlapping fields) (Processing terminated by high-order bit in opr 1) (If opr 2 field shorter than opr 1, insert leading zeros in opr 1.)	Prot	Unchanged
Move Zones	MVZ	D3	SS	D1(L, B1), D2(B2)	The 4 high-order bits of opr 2 into the 4 high-order bits of opr 1. (Left to right byte by byte) (Max number of bytes moved: 256) (Low-order bits of each byte of both opr's unchanged.) (No restriction on overlapping fields)	Prot Adr	Unchanged
Multiply	M	5C	RX	R1, D2(X2, B2)	Multiply opr 1 by opr 2 Product: even and odd pair GPRs opr 1 becomes the product. (Opr 1 must specify an even-numbered reg) (Sign bit extended to 1st significant product digit)	Adr Spec	Unchanged

CUT ALONG DOTTED LINE

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