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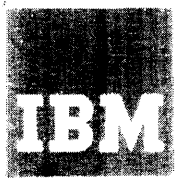
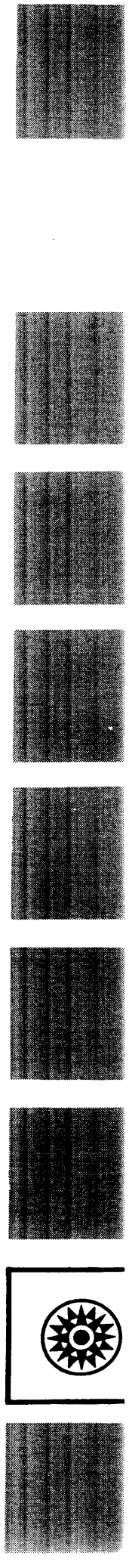


Systems Reference Library

IBM System/360 Model 20 Functional Characteristics

This manual contains a description of the complete Model 20 System and a detailed description of the processing unit and console. A detailed description of operation codes and operator information is included.



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Form No	Pages	Dated
N26-0179	15, 16	January 4, 1967
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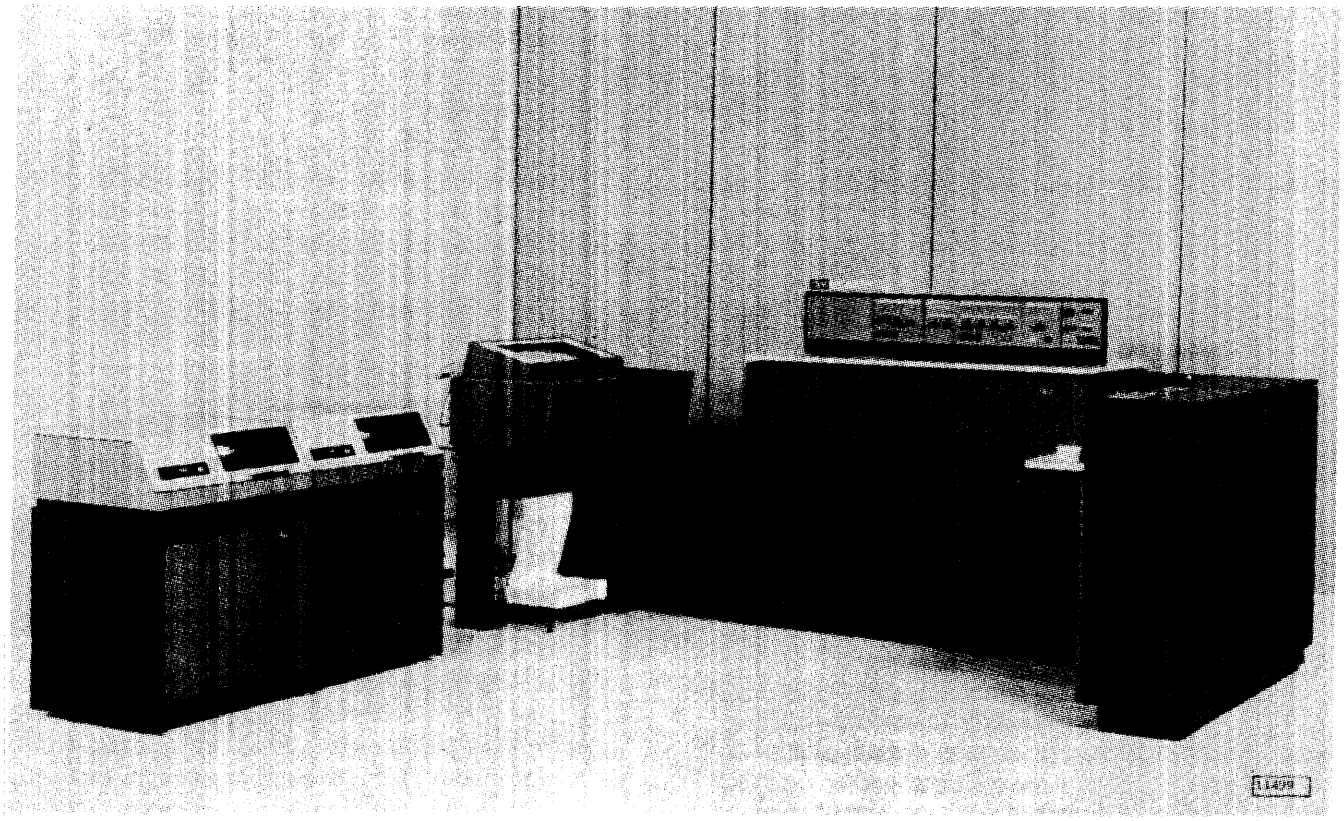


System/360 Model 20

The IBM System/360 Model 20 represents a major advance in low cost, high reliability data processing systems. New dimensions of performance, flexibility, and reliability are offered to the punched card, magnetic tape, or direct access storage user.

The System/360 Model 20 is a powerful, productive, and practical extension of the IBM System/360. The System/360 Model 20 offers users the functional capabilities of large data processing systems at performance and cost levels tailored to the individual user's needs.

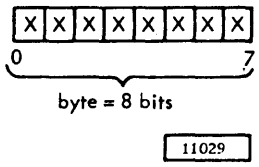
The IBM System/360 Model 20 consists of a group of interconnected functional units operating under the control of a series of instructions, called a program, stored in the Central Processing Unit (CPU). Figure 1 shows a typical configuration of units. The IBM 2020 Central Processing Unit is the central figure in the group, and attached to it are various card reading, card punching, magnetic tape, disk storage drive, and printing units to provide input to the system and output from the system.

The purpose of this reference manual is to provide detailed information on the operation and characteristics of the Central Processing Unit. The IBM "System/360 Model 20 Bibliography" (Form A26-3565) lists all related publications.

CENTRAL PROCESSING UNIT (CPU)

Main Storage

Main Storage consists of 4,096; 8,192; 12,288; and 16,384 positions of magnetic core storage. Each position has an address and contains an eight-bit unit of information referred to as a byte. Coded combinations of bits within a byte can represent alphabetic, numeric, binary, or logical data.



Main storage is used to hold all the data that is to be operated upon, or processed, at a given time. It also holds the instructions, or program, which control the operation of the system. For each individual job performed by the system, certain portions

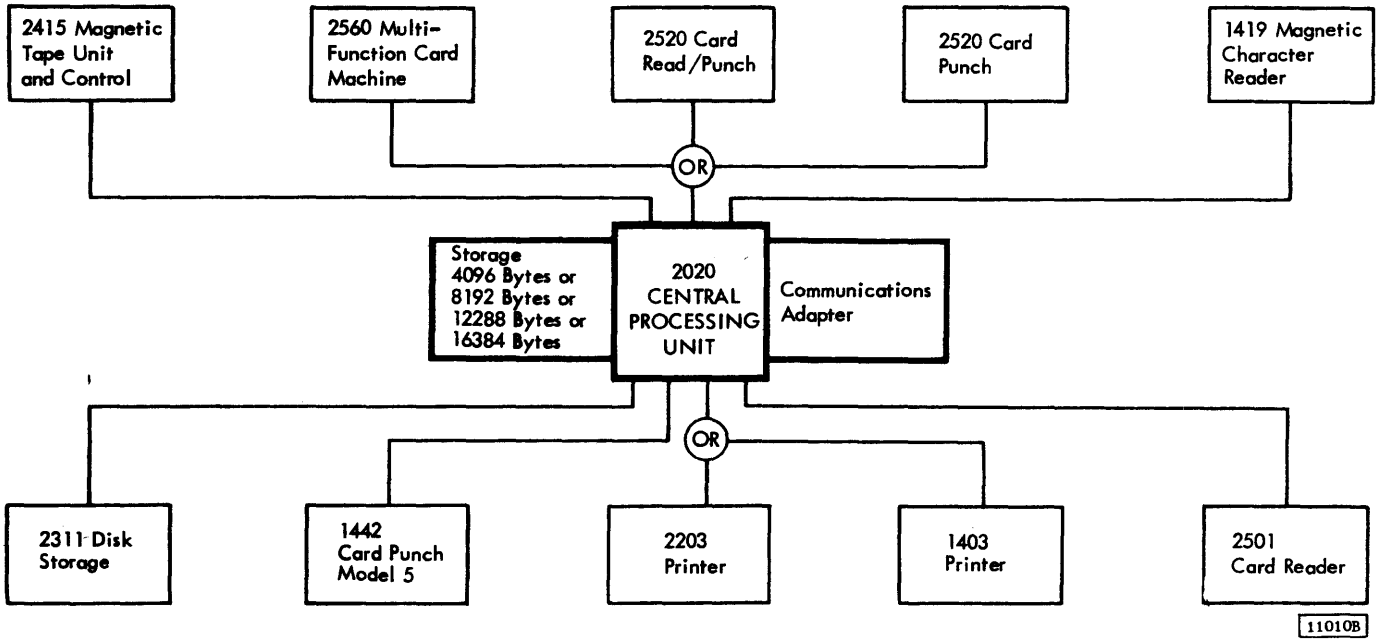


Figure 1. System/360 Model 20

NOTE: The illustrations in this manual have a code number in the lower corner. This is a publishing control number and is unrelated to the subject matter.

of main storage are assigned to store instructions, and certain portions to store data to be processed.

General Registers

Eight general purpose registers, small auxiliary storage units, are provided for temporary storage of small amounts of data. Each register is the equivalent of two bytes (one halfword) and is loaded or unloaded under the control of the stored program. Information may flow from register to register, main storage to register, or from register to main storage.

The registers are numbered 8-15 and are selected by the four-bit R or B field of an instruction.

Parity Checking

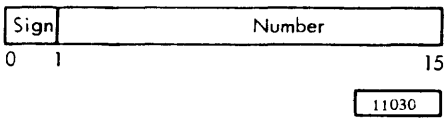
To ensure the accurate transfer of data, an extra (parity) bit is generated for each four bits transferred to or from main storage or register storage. The parity bit is added during transfer, if it is needed, to maintain an odd number of bits. The bit count is monitored continuously, and any missing or extra bits which result in an even number of bits cause a CPU parity error.

Data Formats

The basic unit of addressable data is an eight-bit byte. Each address contains eight bits of data and can be considered a byte boundary.

The byte is divided into two sections of four bits each. A check (parity) bit is provided for each four bits.

Halfword Binary Number

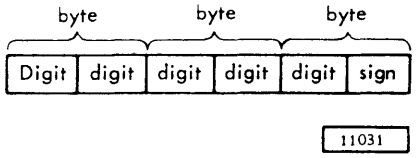


A halfword binary number has a fixed length of two bytes (16 bits). The leftmost bit is reserved for sign (+ or -) control.

Decimal Number

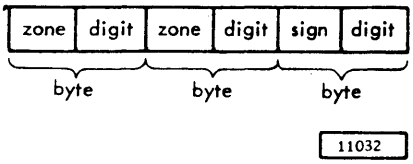
A decimal number may be in either of two forms: packed decimal or zoned decimal.

Packed Decimal: This format allows two numeric digits to be stored within one eight-bit byte.



An eight-bit byte may contain two numeric digits, except in the case of the rightmost byte, which has a sign to the right. Variable field length in this format allows for fields up to 16 bytes in length.

Zoned Decimal: This format contains one digit in the rightmost four positions of each byte.



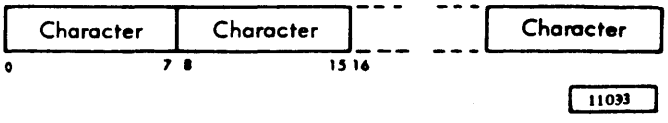
The left four bits of each byte in this format are called zone bits, and are not used except for the low-order (rightmost) byte which uses them for the sign. Zone bits do not affect the value of the numeric digit contained in the right four bits of the byte.

Logical Data

Logical data may be contained in the instruction or it may reside in core storage as an operand (an operand is data contained in or addressed by the instruction and used to execute the instruction). Logical data may have a fixed length of one byte or may be variable in length up to a maximum of 256 bytes.

Fixed-Length Logical Data

Variable-Length Logical Data



Instruction Format

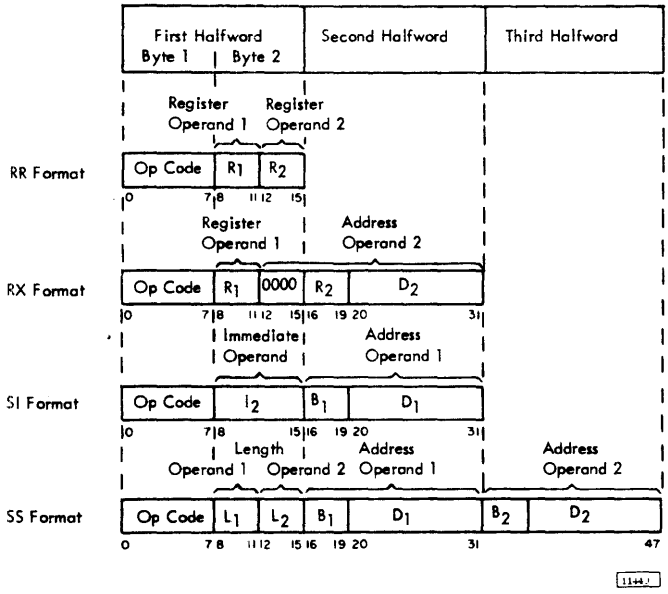
The instruction format specifies the length of the instruction and the type of operation to be performed. The length of the instruction can be one, two, or three halfwords. The types of instruction formats are RR, RX, SI, and SS.

RR Format: Denotes a register-to-register operation.

RX Format: Denotes a register-to-storage or a storage-to-register operation. In this format, bits 12 through 15 must be zero.

SI Format: Denotes a storage-immediate operation. In this format the I2 field of the instruction is the second operand.

SS Format: Denotes a storage-to-storage operation.



In each format, the first instruction halfword consists of two parts. The first byte contains the operation code (op code). The length and format of an instruction are specified by the first two bits of the operation code. The second byte may be used to contain data, specify operand lengths, or specify registers to be used by the operation.

Instruction Execution

For purposes of describing the execution of instructions, operands are designated as first and second operands.

These names refer to the manner in which the operands participate. The operand to which a field in an instruction format applies is generally denoted by the number following the code name of the field, for example, R1, B1, L2, D2. Normally, the operation of the CPU is controlled by instructions taken in sequence. An instruction is fetched from a location specified by the current instruction address. The current instruction address itself is located in the Program Status Word (PSW). After the fetch operation, the current instruction address is increased by the number of bytes in the fetched instruction to enable addressing of the next instruction in sequence.

The instruction is then executed by adding, subtracting, multiplying etc., both operands with each other. The result that is thus obtained usually replaces operand 1. Upon the execution of certain instructions, a condition code, which reflects the nature of the result, is set into the PSW.

Subsequently, the updated address in the PSW is used to read out the next instruction from the main storage and the processing continues.

Information Positioning

Byte locations in storage are consecutively numbered from 0; each number being considered the address of the corresponding byte. Bytes may be handled singly or strung together in fields. A group of two consecutive bytes is called a "halfword." The location of any field or group of bytes is specified by the address of the leftmost byte.

Information positioned in storage may be in fixed-length format or variable-length format. The length of fields is either implied by the operation to be performed or stated explicitly as part of the instruction. When the length is implied, the information is said to have a fixed length, which can be one, two, or four bytes.

Fixed-length fields must be located in main storage on an integral (halfword) boundary (Figure 2) for that unit of information. A boundary is called integral for a unit of information when its storage

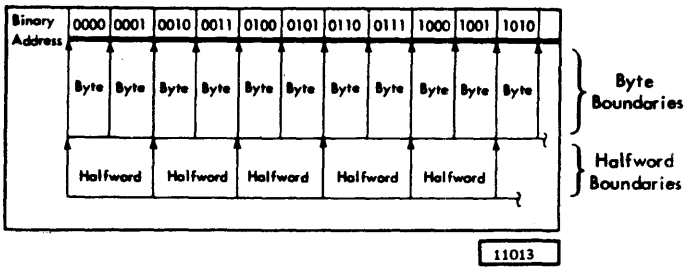


Figure 2. Integral Boundaries

address is a multiple of the length of the unit in bytes. For example, a halfword (two bytes) must have an address that is a multiple of the number 2.

In the 2020, all instructions and all data with fixed word length (operands addressed by RX-format instructions) must begin on a halfword boundary. An instruction (or data with fixed word length) is properly located at a halfword boundary when its address is even or, in other words, when the low order bit of the address is zero. An improperly placed instruction causes an error stop.

When the length of a field is not implied by the operation code, but is stated explicitly, the information is said to have variable-length field.

Within any instruction format or any fixed-length operand format, the bits are consecutively numbered from left to right starting with bit number 0.

Variable-length fields are not restricted to halfword boundaries, and may contain up to 256 bytes. Length is variable in increments of one byte.

ADDRESSING

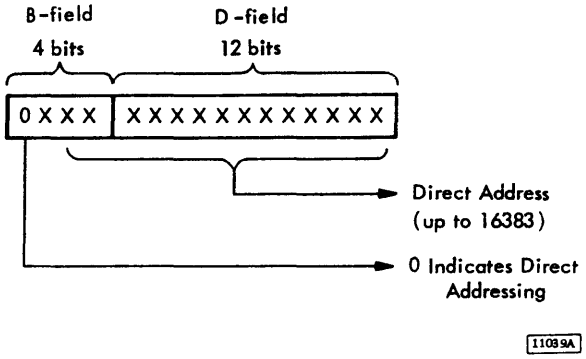
Byte locations in storage are expressed in binary form and consecutively numbered from 0000 to the upper limit of available storage. Appendix D explains the binary number system, and Appendix E contains the hexadecimal representation for addresses 0000 to 4095. The first 144 bytes (Bytes 0000-0143) are reserved for internal CPU control and are not available to the program. The location of any field or group of bytes is specified by the address of the leftmost byte.

An address used to refer to main storage may be specified by either of two methods; direct addressing or effective address generation.

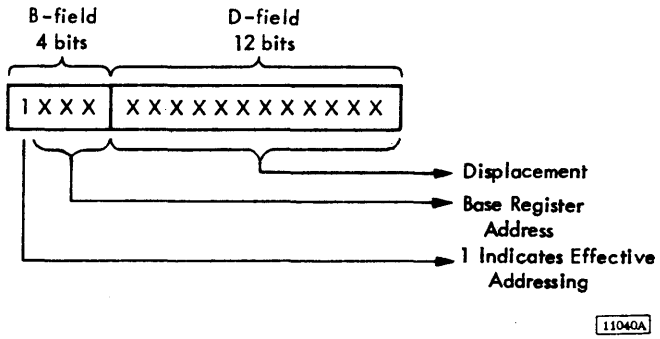
NOTE: Neither a direct address nor an effective address must be zero, because zero is regarded as a specification error. The CPU checks all direct or effective addresses for validity and stops on a specification error if these addresses are zero, or pertain to the protected area or exceed the storage capacity.

Direct Addressing: Direct addressing is used when the high-order bit in the B-field of an instruction is zero.

When the direct addressing method is employed, the low-order 14 bits of the combined B- and D-fields are used to refer directly to byte locations in main storage. The 12 binary bits in the D-field allow an address specification of up to 4095. To address additional (optional) storage, the adjacent two bits in the low-order position of the B-field are used, allowing address specification of up to 16383.



Effective Addressing: Effective addressing is used when the high-order bit in the B-field of an instruction is one.



In the effective-address generation method, the contents of the general register specified by the B-field of an instruction, are added to the contents of the D-field of the instruction to form the effective address. The content of the general register specified by the B-field is referred to as the "base address." The content of the D-field is referred to as the "displacement." (This type of address modification is commonly referred to as indexing.) Effective addressing may be either in a positive or a negative direction, and is determined by the sign of the base address. Caution should be exercised because a resultant effective address that is negative or that refers to the first 144 bytes of main storage results in an error condition.

Any of the eight general registers, 8 through 15, may be specified in the B-field as the location of the base address for effective-address generation.

If there are zeros in either the general register specified, or in the displacement field of the instruction when effective-address generation is specified, the effective address generated is the same as direct addressing with the nonzero component.

Effective addressing is useful for program routines which require address modification.

OPERANDS

For addressing purposes, operands can be grouped in three classes: explicitly addressed operands in main storage, immediate operands placed in main storage as part of the instruction stream, and operands located in the general registers.

Explicitly Addressed Operands

An explicitly addressed operand is selected from a main-storage location not related to the location of the instruction referring to it. It is always specified by means of a storage address. When the operand contains more than one byte, the address gives the location of the first byte of the field, subsequent bytes being located in higher addresses. Both the first and second operands of an instruction can be explicitly addressed.

Explicitly addressed operands can be of fixed length or variable length. The length of variable-field-length operands is specified in the L-field of the instruction. The L-field, either four or eight bits long, specifies the length in terms of the number by bytes to the right of the addressed byte, and thus can specify a maximum field length of 256 bytes.

Immediate Operands

An immediate operand consists of one eight-bit byte of data which is located in the instruction itself. Only the instructions in the SI format contain immediate data. The immediate data is always the second operand; the first operand is located in the main-storage location specified by the B1-D1 field.

Operands in Registers

Information referred to by an instruction may be located in one of eight general registers. The registers are identified by numbers 8-15 and are selected by the four-bit R or B field of an instruction. The registers are not designated by main-storage addresses.

An operand located in a register has a fixed length of one halfword, or 16 bits.

TIME SHARING

The 2020 has the ability to operate in a mode referred to as "time sharing." Time sharing is a means of overlapping input/output operations with each other and with processing. Time sharing is based on a system of monitoring the operation of input/output devices and sequencing the transfer of data to or from the I/O devices so as to make the most efficient use of processing time.

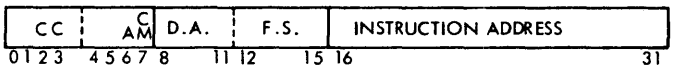
Processing operations in the CPU are time shared with the transfer of data between main storage and the I/O devices. When an I/O device requests service, processing is suspended only for the time required to send or to accept the input/output data.

Time sharing allows the CPU to perform useful processing functions while card or forms movement is taking place. A system of signaling that the I/O device is finished with the data transfer to or from the CPU is referred to as an "interruption" system.

Program Status Word (PSW)

The PSW contains the information necessary for proper program execution. It is located in an internal register in the CPU and is not directly addressable. The programmer can change the PSW by means of a Set PSW instruction. The PSW has a fixed-length format of two halfwords.

PSW Format



0 - 1	Not used
2 - 3	Condition Code
4 - 5	Not used
6	* ASCII MODE BIT
7	Channel Mask
8 - 11	Device Address
12 - 15	Function Specification
16 - 31	Instruction Address

* American Standard Code for Information Interchange

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The PSW is used to control instruction sequencing and to hold and indicate the status of the system in relation to the program being executed. The active or controlling PSW is called the "current PSW."

By storing the current PSW during an interrupt, the status of the CPU can be preserved for subsequent inspection. By loading a new PSW or part of a PSW, the state of the CPU can be initialized or changed. The functions of the PSW are described in detail later in this publication.

When the current PSW is stored during an input/output interruption, the status of the CPU and the next sequential address are preserved for use after the interruption is serviced. An instruction to load a new PSW is equivalent to an unconditional branch to the instruction address contained in the new PSW.

Operation of the Program Load key or System Reset key causes the condition code (bits 2-3), the ASCII mode bit (bit 6), and the channel mask bit (bit 7) of the current PSW to be reset to zero.

Interruption

In the 2020, an automatic interrupt system is provided to make optimum use of the I/O devices and available processing time. The I/O devices signal the CPU to store an end condition when a data transfer has been terminated. Upon completion of the execution of each instruction, during the time that the CPU is in an interruptible mode, the CPU checks the various end conditions according to a built-in priority sequence. The first end condition thus found causes the actual interrupt. The interrupt is an automatic branch from the main program to a subroutine. This subroutine may be designed to test the received data for validity or to perform some other action. Since the interrupt occurs at the earliest moment possible after a data transfer has been completed, it is the primary means of controlling I/O operations.

The branch to the subroutine is accomplished by replacing the current PSW with a new PSW which contains the start address of the subroutine in its instruction address portion. The former current PSW is stored into a particular core-storage location and thus becomes the old PSW. During the transfer, the old PSW is furnished with the device address and the function specification of the I/O unit that caused the interrupt.

By making the last instruction in the subroutine a branch with the address of the old PSW specified as the branch address, the normal course of the main program is resumed because the next sequential instruction of the main program is specified in the old PSW. The entire exchange of the program status words (PSWs) is fully automatic, however, the channel mask bit in the PSW, which determines whether the CPU is interruptible or not,may be set or reset under program control. The CPU is interruptible when the channel mask bit is set to 1; it is not interruptible if the channel mask bit is 0. The channel mask bit is zero when the CPU is in a reset state.

The arithmetic and logical operations are employed to process binary numbers of fixed length, decimal numbers of variable length, and logical information of either fixed or variable length.

Arithmetic and logical operations performed by the CPU fall into three classes: binary arithmetic, decimal arithmetic, and logical operations. These three classes differ in the data formats used, the registers involved, the operations provided, and in the way the field length is stated.

BINARY ARITHMETIC

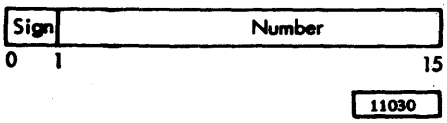
The binary arithmetic operand is the 16-bit binary halfword. The binary instructions perform binary arithmetic on operands serving as addresses, index quantities, and counts, as well as binary data. One operand is always in a general register. The second operand may be either in main storage or in a general register.

Data Format

Binary numbers occupy a fixed length format consisting of a one-bit sign followed by the 15-bit binary field. When held in one of the general registers, a binary quantity has a 15-bit binary field and occupies all 16 bits of the register.

Binary data in main storage also occupies a 16-bit halfword, with a binary field of 15 bits. This data must be located on integral storage boundaries for this unit of information, i.e., the low-order binary address bit is zero.

Halfword Binary Number



Number Representation

All binary operands are treated as signed numbers. Positive numbers are represented in true binary notation with the sign bit set to 0. Negative numbers are represented in two's-complement notation with a 1 in the sign bit. The two's complement of a number is obtained by inverting each bit of the number and adding a one in the low-order bit position.

The number obtained by inverting each binary bit represents the one's complement of the original number. To represent the two's complement, a one must be added to the low-order position of the one's complement.

```
0 1 1 1 0 1 0 1 0 0 1 0 1 1 1 0  =  original number
1 0 0 0 1 0 1 0 1 1 0 1 0 0 0 1  =  one's complement
1 0 0 0 1 0 1 0 1 1 0 1 0 0 1 0  =  two's complement
↑
└── sign position
```

Two's-complement notation does not include a negative zero. It has a number range in which the set of negative numbers is one larger than the set of positive numbers. The maximum positive number consists of an all-one integer field with a sign bit of zero, whereas the maximum negative number consists of an all-zero integer field with a 1 bit for sign.

The CPU cannot represent the complement of the maximum negative number. When an operation, such as a subtraction from zero, produces the complement of the maximum negative number, the number remains unchanged, and a binary overflow condition is recognized. An overflow does not result, however, when the number is complemented and the final result is within the representable range. An example of this case is a subtraction from minus one.

The sign bit is leftmost in a number. An overflow carries into the sign-bit position and changes the sign.

Figure 3 illustrates some sample values of 16-bit binary integers and their equivalents in decimal form.

Number	Signed Decimal	S - - - - - - - - - INTEGER - - - - - - - - -
$2^{15}-1$	= 32767 =	0111 1111 1111 1111
2^{8}	= 256 =	0000 0001 0000 0000
2^{0}	= 1 =	0000 0000 0000 0001
0	= 0 =	0000 0000 0000 0000
-2^{0}	= -1 =	1111 1111 1111 1111
-2^{1}	= -2 =	1111 1111 1111 1110
-2^{8}	= -256 =	1111 1111 0000 0000
$-2^{15}+1$	= -32767 =	1000 0000 0000 0001
-2^{15}	= -32768 =	1000 0000 0000 0000

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Figure 3. Binary Representation

Condition Code

The results of binary add, subtract, and compare operations are used to set the condition code in the Program Status Word (PSW). All other binary operations leave this code undisturbed. The condition code can be used for decision-making by subsequent branch-on-condition instructions.

The condition code is set to reflect three types of results for binary arithmetic. For most operations, the states 0(00), 1(01), or 2(10) indicate a zero, less than zero, or greater than zero content of the result register. An overflow results in a Binary Overflow Check condition.

For a compare operation, the states 0, 1, or 2 indicate that the first operand is equal, low, or high compared to the second operand. Condition code settings are shown in Figure 4.

	0	1	2
Compare Halfword	equal	low	high
Add Halfword	zero	< zero	> zero
Subtract Halfword	zero	< zero	> zero
Add	zero	< zero	> zero
Subtract	zero	< zero	> zero

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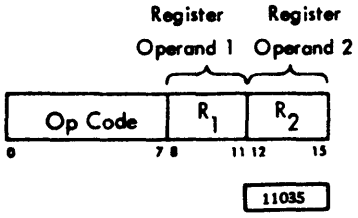
Figure 4. Condition Code Settings for Binary Arithmetic

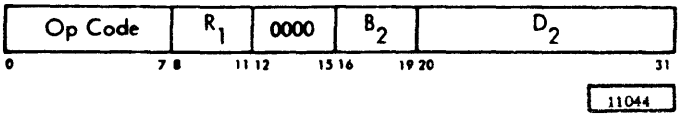
Instruction Format

Binary instructions use the following two formats:

RR Format



RX Format



In these formats, R_1 specifies the address of the general register containing the first operand. The second operand location, if any, is defined differen for each format.

In the RR format, the R2 field specifies the address of the general register containing the second operand.

In the RX format, the address which designates the storage location of the second operand is derived from the contents of the B2 and D2 fields of the instruction. As described in the section on Addressing, this address may be taken directly from the B2 and D2 fields, or an effective address may be formed by adding the contents of the general register specified by the B2 field to the contents of the D2 field.

Bits 12 through 15 of the RX format must be zero. The second operand, addressed by B2-D2, must begin on a halfword boundary, i.e., its address must be even, otherwise a program error stop occurs.

Results of operations replace the first operand except for a store operation. The result replaces the second operand for the store operation.

An instruction can specify the same general register both for address modification and for operand location. Address modification is always completed before execution of the operation.

The contents of all general registers and storage locations participating in the addressing or execution part of an operation remain unchanged, except for the storing of the final result.

Instructions

The binary arithmetic instructions and their mnemonics, formats, and operation codes are listed in Table 1.

Table 1. Binary Instructions

NAME	MNEMONIC	FORMAT	OPERATION CODE
Load Halfword	LH	RX	48
Add Halfword	AH	RX	4A
Subtract Halfword	SH	RX	4B
Compare Halfword	CH	RX	49
Store Halfword	STH	RX	40
Add	AR	RR	1A
Subtract	SR	RR	1B

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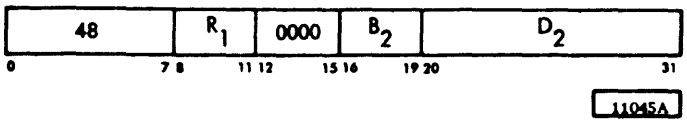
Load Halfword

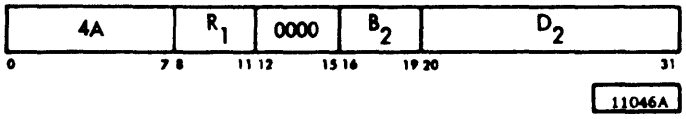
LH RX



The second operand is placed in the first operand location. The instruction uses RX format and provides for loading a halfword from the main-storage location specified by the B2-D2 fields into the register specified by the R1 field. The condition code is not changed.

Add Halfword

AH RX

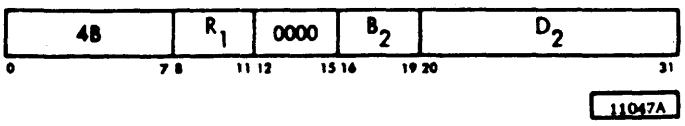


The second operand is added to the first operand and the sum is placed in the first operand location. Both operands are halfword length. The first operand is contained in the register specified by the R1 field. The second operand is located at a main-storage location specified by the B2-D2 fields of the instruction.

Addition is performed by adding all 16 bits of both operands. If the "carries" out of the sign-bit position and the high-order numeric bit position agree, the sum is satisfactory; if they disagree, an overflow occurs. The sign bit is not changed after the overflow. A positive overflow yields a negative final sum, and a negative overflow results in a positive sum. The overflow causes a binary-overflow-check condition. The condition code is set to 00, 01, or 10 to indicate that the result is zero, or greater than zero.

Subtract Halfword

SH RX

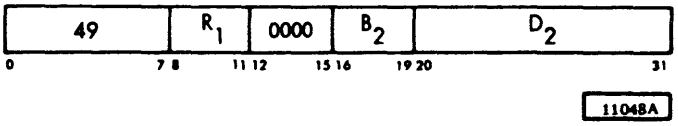


The second operand is subtracted from the first operand and the difference is placed in the first operand location. Both operands are halfword length. The first operand is contained in the register specified by the R1 field. The second operand is located at a main-storage location specified by the B2-D2 fields of the instruction.

Subtraction is performed by adding the two's complement of the second operand to the first operand. All 16 bits of both operands participate, as in ADD. If the "carries" out of the sign-bit position and the high-order numeric bit position agree, the difference is satisfactory; if they disagree, an overflow occurs, resulting in a binary-overflow-check condition. The condition code is set to 00, 01, or 10 to indicate that the result is zero, less than zero, or greater than zero.

Compare Halfword

CH RX



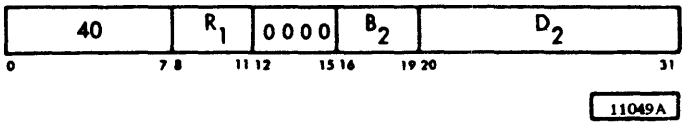
The first operand is compared with the second operand, and the result of the compare is indicated by the setting of the condition code in the PSW. The first operand is contained in the register specified by the R1 field. The second operand is located at a main-storage location specified by the B2-D2 fields of the instruction.

Comparison is algebraic, treating both comparands as 16-bit signed integers. Operands in registers or storage are not changed as a result of the operation.

The condition code is 00 if the operands are equal, 01 if the first operand is lower than the second operand, and 10 if the first operand is higher than the second.

Store Halfword

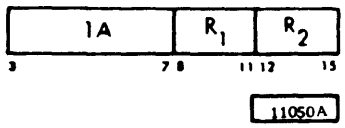
STH RX



The first operand is stored at the second operand location. The instruction uses RX format and provides for storing a halfword from the register specified by the R1 field into the main-storage location specified by the B2-D2 fields of the instruction. The condition code remains unchanged.

Add

AR RR

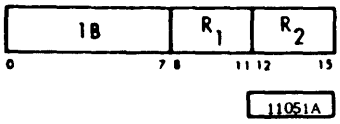


The second operand is added to the first operand, and the sum is placed in the first operand location. The halfword contained in the register specified by the R1 field is added to the halfword contained in the register specified by the R2 field and the sum replaces the contents of the register specified by R1.

Addition is performed by adding all 16 bits of both operands. If the carries out of the sign-bit position and the high-order numeric bit position agree, the sum is satisfactory; if they disagree, an overflow occurs. The sign bit is not changed after the overflow. A positive overflow yields a negative final sum, and a negative overflow results in a positive sum. The overflow causes a binary-overflow-check condition. The condition code is set to 00, 01, or 10 to indicate that the result is zero, less than zero, or greater than zero.

Subtract

SR RR



The second operand is subtracted from the first operand, and the difference is placed in the first operand location.

The halfword contained in the register specified by the R2 field is subtracted from the halfword contained in the register specified by the R1 field and the difference replaces the contents of the register specified by R1.

Subtraction is performed by adding the two's complement of the second operand to the first operand. All 16 bits of both operands participate, as in ADD. If the "carries" out of the sign-bit position and the high-order numeric bit position agree, the difference is satisfactory; if they disagree, an overflow occurs. The overflow causes a binary-overflow-check condition. The condition code is set to 00, 01, or 10 to indicate that the result is zero, less than zero, or greater than zero.

Binary Arithmetic Error Conditions

Error conditions which may occur during the instruction or execution phase of binary operations are:

1. Operation Code Invalid
2. Addressing Error
   a. An instruction address or an operand address refers to the protected first 144 bytes of main storage (addresses 0 to 143).
   b. An instruction address or an operand address is outside available storage.
   c. The last (highest) main-storage position contains any part of an instruction that is to be executed.
   d. The R1 or R2 fields of a binary instruction contain binary values 0 through 7.
3. Specification Error
   a. The low-order bit of an instruction address is one.
   b. The half-word second operand is not located on a 16-bit boundary.
   c. Bits 12 through 15 of an RX format instruction are not all zero.
4. Binary Overflow Check
5. CPU Parity Error

DECIMAL ARITHMETIC

Decimal arithmetic operations include addition, subtraction, multiplication, division, and comparison. Both operands and results are located in storage.

All decimal arithmetic operations are performed with data in the packed mode for optimum use of storage. Since data is often communicated to or from peripheral devices in the zoned form, operations are provided for changing from zoned to packed format and vice versa.

Operand fields can be located on any byte boundary, except for the first 144 bytes of main storage, which are protected. They can have a length of up to 31 digits and sign, except for multiplier and divisor operands which are limited to 15 digits.

Each address specifies the leftmost byte of an operand. Associated with each address is a length field which indicates the number of additional bytes that the operand extends beyond the first byte.

Data Format

Decimal operands reside in main storage only. They occupy fields that may start at any byte address and are composed of one to 16 eight-bit bytes. All operations use a two-address format.

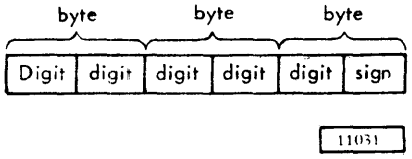
Lengths of the two operands specified in the instruction need not be the same. Regardless of length, the two operands are treated as if the rightmost integers were aligned before the operation begins. For example, in an add operation, the rightmost integers must be aligned to ensure that units are added to units, tens are added to tens, hundreds to hundreds, etc. The programmer may add high-order zeros as needed, to ensure that the result field is always large enough to contain all the digits of the result.

Processing takes place from right to left, as in simple manual arithmetic operations, treating the rightmost position of each operand as the units position, the next position to the left as the tens position, etc.

Lost carries or lost digits from arithmetic operations are signalled by a decimal-overflow condition. Operands are either in the packed or zoned format. Negative numbers are carried in true form.

Packed Decimal Number

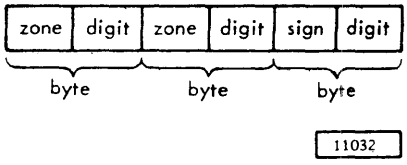
In the packed format, each eight-bit byte can contain the binary equivalents to two decimal digits, except for the rightmost four bits of the rightmost byte of the field, which represent the sign. Decimal digits 0 through 9 are equivalent to binary values 0000 through 1001.



The decimal digits range from 0 to 9 while any value from 10 to 15 (in hexadecimal representation 'A' to 'F') is regarded as a valid sign. In decimal arithmetic, all numbers must be arranged in the packed format. By means of the Pack instruction, it is possible to change zoned decimal numbers into packed numbers. Decimal number fields may overlap only when their rightmost bytes are identical. During the execution of all decimal arithmetic instructions, all data is checked for validity. A sign code found in any other but the sign position leads to an error stop as does a decimal value that is found in the sign position.

Zoned Decimal Numbers

In the zoned format, each eight-bit byte can contain one decimal digit in the right four bits and a zone code in the left four bits. However, the right most byte of a zoned decimal number field contains the digit in the right half and the sign in the left half.



The zone bits act only as fill characters and do not affect the value of the decimal digits. The zoned format is needed for decimal data that is sent to character-set sensitive I/O devices. Similarly, all decimal data that is received from card I/O devices comes in the zoned format. The zone is either 15 (F) in the Extended Binary-Coded-Decimal Interchange Code (EBCDIC) or 5 in the ASCII. Since the zone F is identical with one of the general plus signs, all data received from punched cards is recognized as positive unless it is explicitly specified as negative data. Data can be changed from the packed to the zoned format by means of the Unpack instruction. During unpacking, the correct zone is automatically supplied by the CPU. It depends on the mode bit in the PSW as to which zone is used If the mode bit is zero, the EBCDIC-zone F is used, if the mode bit is one, the ASCII-zone 5 is used.

Automatic Sign Standardization

During the processing of all arithmetic instructions that handle decimal data, the CPU supplies the final result with the correct sign according to the rules of algebra. The resultant sign is either an ASCII

plus or minus sign, or an EBCDIC plus or minus sign. Whether the result sign is standardized in the ASCII or in the EBCDIC mode depends on the mode bit in the PSW. For example, if the result sign is positive and the mode bit is zero, the sign code 1100 is selected. If the result sign is negative and the mode bit is one, the sign code 1011 is selected. Thus, the result can have only an ASCII- or an EBCDIC sign.

	Valid Sign Codes	ASCII	EBCDIC
Standardization	(A) 1010 +	+	
	(B) 1011 -	-	
	(C) 1100 +		+
	(D) 1101 -		-
	(E) 1110 +		
	(F) 1111 +		

11444

Condition Code

The results of all add-type and comparison operations are used to set the condition code in the PSW. All other decimal arithmetic operations leave the code unchanged. The condition code can be used for decision making by subsequent Branch-on-Condition instructions.

The condition code is set to reflect the types of results for decimal arithmetic. Four different result types can occur:

1. The result is zero, indicated by condition code 00.
2. The result is less than zero (negative), indicated by condition code 01.
3. The result is more than zero (positive), indicated by condition code 10.
4. The result does not fit into the result field (overflow) indicated by condition code 11.

For the comparison operation, the condition code settings 0, 1, and 2 indicate that the first operand compared equal, low, or high as shown in Table 2.

Table 2. Condition Code Settings for Decimal Operations

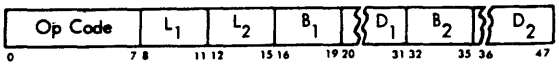
	0	1	2	3
Add Decimal	zero	< zero	> zero	overflow
Compare Decimal	equal	low	high	
Subtract Decimal	zero	< zero	> zero	overflow
Zero and Add	zero	< zero	> zero	

11018

Instruction Format

Decimal instructions use the following format:

SS Format



11052

In this format, the address which specifies the core storage location of the leftmost byte of the first operand field is derived from the contents of the B1 and D1 fields of the instruction. The number of operand bytes to the right of this byte is specified by the L1 field of the instruction. Therefore, the length in bytes of the first operand field is 1 to 16 corresponding to a length code in L1 of 0000 to 1111. The second operand field is specified similarly by the L2, B2, and D2 instruction fields.

As described in the section on Addressing, the address of each operand may be taken directly from the respective B and D fields of the instruction, or effective addresses may be formed by adding the contents of the general register specified by the B field to the contents of the D field.

Results of operations replace the first operand field. The result is never stored outside the field specified by the address and length. The second operand field remains unchanged, except in those cases where overlapping fields, which are permitted, actually occur. The contents of the general registers remain unchanged.

Instructions

The decimal arithmetic instructions and their mnemonics and operation codes are shown in Table 3.

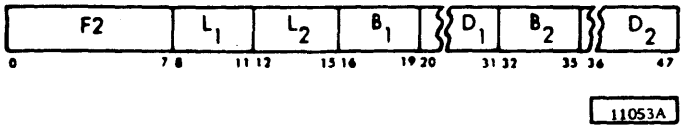
Table 3. Decimal Instructions

Name	Mnemonic	Format	OPERATION CODE
Pack	PACK	SS	F2
Unpack	UNPK	SS	F3
Move with offset	MVO	SS	F1
Zero and Add	ZAP	SS	F8
Add Decimal	AP	SS	FA
Subtract Decimal	SP	SS	FB
Compare Decimal	CP	SS	F9
Multiply Decimal	MP	SS	FC
Divide Decimal	DP	SS	FD

11019A

Pack

PACK SS



The format of the second operand is changed from zoned to packed, and the result is placed in the first operand location.

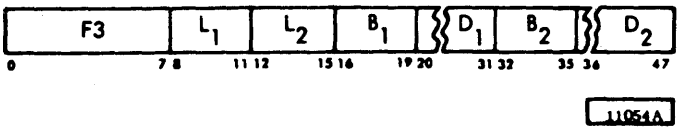
The second operand is assumed to have the zoned format. All zones are ignored, except the zone over the low-order digit, which is assumed to represent a sign. The sign is placed in the right four bits of the low-order byte, and the digits are placed adjacent to the sign and to each other in the remainder of the result field. The sign and digits are moved unchanged to the first operand field and are not checked for valid codes.

The fields are processed right to left. If the second operand does not fill the first operand completely, the remaining high-order positions of the first operand are filled with zeros. If the first operand field is too short to contain all the significant digits of the second operand field, the remaining digits are ignored. Overlapping fields may occur and are processed by storing each result byte immediately after the necessary operand bytes are fetched.

The condition code remains unchanged.

Unpack

UNPK SS



The format of the second operand is changed from packed to zoned, and the result is placed in the first operand location.

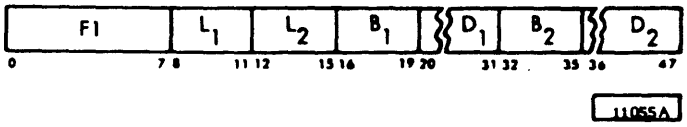
The digits and sign of the packed operand are placed unchanged in the first operand location, using the zoned format. Zones with coding 1111 in the binary-coded-decimal mode and coding 0101 in the ASCII mode are supplied for all bytes except the low-order byte, which receives the sign of the packed operand. The operand sign and digits are not checked for valid codes.

The fields are processed right to left. If the second operand does not fill the first operand completely, the remaining high-order bytes of the first operand are each filled with a zero and a zone. If the first operand field is too short to contain all significant digits of the second operand, the remaining digits are ignored. The first and second operand fields may overlap and are processed by storing a result byte immediately after the necessary operand bytes are fetched.

The condition code remains unchanged.

Move with Offset

MVO SS



The second operand is placed to the left of and adjacent to the low-order four bits of the first operand.

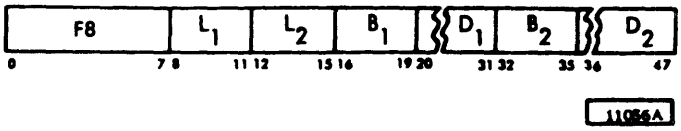
The low-order four bits of the first operand are attached as low-order bits to the second operand, the second operand bits are offset by four bit positions, and the result is placed in the first operand location. The first and second operand bytes are not checked for valid codes.

The fields are processed right to left. If necessary, the second operand is extended with high-order zeros. If the first operand field is too short to contain all bytes of the second operand, the remaining information is ignored. Overlapping fields may occur and are processed by storing a result byte as soon as the necessary operand bytes are fetched.

The condition code remains unchanged.

Zero and Add

ZAP SS



The second operand is placed in the first operand location.

The operation is equivalent to an addition to zero. The sign code is made 1100 for positive and 1101 for

negative results in the binary-coded-decimal mode, and 1010 for positive and 1011 for negative results in the ASCII mode. A zero result is always positive.

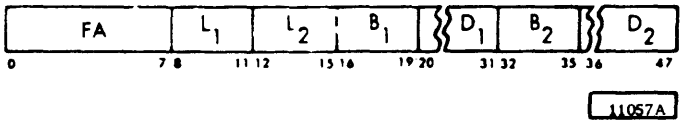
When the length of the second operand (L2) is greater than the length of the first operand (L1) a specification error stop occurs. The instruction is not executed.

The second operand is checked for valid sign and digit codes. Extra high-order zeros are supplied if needed. The first and second operand fields may overlap when the rightmost byte of the first operand field is coincident with or to the right of the rightmost byte of the second operand.

The condition code is set to 00, 01, or 10 to indicate that the result is zero, less than zero, or greater than zero.

Add Decimal

AP SS



11057A

The second operand is added to the first operand, and the sum is placed in the first operand location.

When the length of the second operand (L2) is greater than the length of the first operand (L1), a specification-error stop occurs. The instruction is not executed.

Addition is algebraic, taking into account the sign and all digits of both operands. All signs and digits are checked for validity. If necessary, high-order zeros are supplied for the second operand.

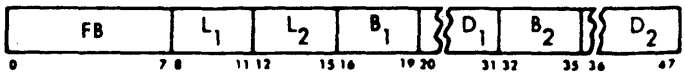
The first and second operand fields may overlap when their low-order bytes coincide; therefore, it is possible to add a number to itself.

The sign of the result is determined by the rules of algebra. A zero sum is always positive. When high-order digits are lost because of an overflow, a zero result has the sign of the correct sum.

The condition code is set to 00, 01, 10 or 11 to indicate that the result is zero, less than zero, greater than zero, or overflow. A decimal overflow is not considered to be an error.

Subtract Decimal

SP SS



11058A

The second operand is subtracted from the first operand, and the difference is placed in the first operand location.

When the length of the second operand (L2) is greater than the length of the first operand (L1) a specification error stop occurs. The instruction is not executed.

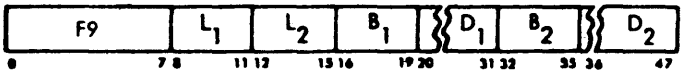
Subtraction is algebraic, taking into account the sign and all digits of both operands. The Subtract Decimal instruction is similar to Add Decimal instruction, except that the sign of the second operand is changed from positive to negative or from negative to positive after the operand is obtained from storage and before the arithmetic operation.

The sign of the result is determined by the rules of algebra. A zero difference is always positive. When high-order digits are lost because of overflow, a zero result has the sign of the correct difference.

The operands of a Subtract instruction may overlap when their low-order bytes coincide even when their lengths are unequal. This property may be used to make an entire field or the low-order part of a field zero. The condition code is set to 00, 01, 10, or 11 to indicate that the result is zero, less than zero, greater than zero, or an overflow condition. A decimal overflow is not considered to be an error.

Compare Decimal

CP SS



11059A

The first operand is compared with the second, and the condition code indicates the comparison result.

When the length of the second operand (L2) is greater than the length of the first operand (L1), a specification-error stop occurs. The instruction is not executed.

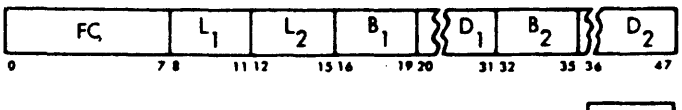
Comparison is right to left, taking into account the sign and all digits of both operands. All signs and digits are checked for validity. If the second operand field is shorter in length than the first operand field, the second operand field is extended with high-order zeros. A positive zero compares equal to a negative zero. Neither operand is changed as a result of the operation. Overflow cannot occur in this operation.

The first and second fields may overlap when their low-order bytes coincide. It is possible, therefore, to compare a number to itself.

A Decimal Compare instruction differs in several respects from a Logical Compare instruction. Signs, zeros, and invalid characters are considered and fields are extended when unequal in length. The condition code is made 00 if the operands are equal, 01 if the first operand is low, and 10 if the first operand is high.

Multiply Decimal

MP SS



11060A

The product of factor one (the first operand) times factor two (the second operand) replaces the first operand. A multiplication can be performed only on data in the packed format. The length codes contained in the L1 and L2 fields specify the number of bytes that extend to the left of the units byte. The units byte is the rightmost byte of a packed decimal operand and it contains one digit and the sign. Factor two is limited to a size of 15 digits plus the sign, or in other words, the length code of factor two must not be greater than 7. Furthermore, the length code of factor two must always be smaller than the length code of factor 1. If L2 is greater or equal to L1, or if L2 exceeds 7, a program error stop occurs.

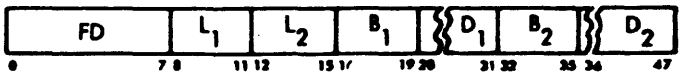
Factor one is limited to a size of 16 bytes (length code 15). The main storage location of factor one is specified by the B1-D1 field according to the rules for direct or effective-address generation. Similarly, the location of factor two is specified by the B2-D2 field.

Since the number of digits in the product (the result) is the sum of the number of digits in both operands, factor one must have as many leading (high order) zero bytes as factor two has data bytes (L2 +1). This requirement for the factor 1 field ensures that no product overflow can occur. If factor 1 has insufficient high order zeros, a program error stop occurs. The sign of the product is developed from the signs of both operands according to the rules of algebra. This is true also when one or both operands are zero. If the larger of the two factors is 15 digits or less, the most efficient use of this instruction is realized when the larger factor is used in the second operand.

The factor two field may overlap the product field when the low-order bytes of both fields coincide. The condition code is not changed by a Multiply Decimal instruction.

Divide Decimal

DP SS



11061A

The dividend (the first operand) is divided by the divisor (the second operand) and is replaced by the quotient and remainder. A divide operation must be performed on data in the packed format only. Length codes, contained in the L1 and L2 fields, specify the number of bytes to the left of the units byte. Each byte contains two arithmetic digits, except the units byte which contains one digit and a sign. The location of the dividend is specified by the B1-D1 field, and the location of the divisor is specified by the B2-D2 field. The result consists of the quotient and the remainder.

The quotient field is placed leftmost in the first operand field. The remainder field is placed rightmost in the first operand field and has a size equal to the divisor size. Together, the quotient and remainder occupy the entire former dividend field; therefore, the address of the quotient field is the address of the first operand. The size of the quotient field in eight -bit bytes is L1−L2, and the length code for this field is one less (L1−L2−1). When the divisor length code is larger than seven (15 digits and sign) or larger than or equal to the dividend length code, the operation is not executed and an error stop occurs.

The dividend, divisor, quotient, and remainder are all signed integers, right-aligned in their fields

The sign of the quotient is determined by the rules of algebra from dividend and divisor signs. The sign of the remainder is the same as the dividend sign. These rules are true even when quotient or remainder is zero.

A divide check occurs when the quotient is larger than the number of digits allowed for it, or if the dividend does not have at least one leading zero. If a divide check occurs, the operation is not executed and a decimal-divide-error stop occurs. Divisor and dividend remain unchanged in their storage locations.

The divisor and dividend fields may overlap only if their low-order bytes coincide.

The condition code remains unchanged for division, and overflow cannot occur.

Programming Notes

The maximum dividend size is 30 digits and sign (16 packed bytes). Since the smallest remainder size is one digit and sign, the maximum quotient size is 29 digits and sign.

The condition for a divide check can be determined by a trial subtraction. The leftmost digit of the divisor field is aligned with the leftmost-plus-one digit of the dividend field. When the divisor, so aligned, is less than or equal to the dividend, a quotient overflow is indicated.

By programming a Divide Decimal instruction so that the dividend field (the first operand) has a number of high-order zero digits equal to the field size of the divisor field (the second operand), a divide check occurs only when a division by zero is attempted.

Decimal Arithmetic Error Conditions

The following error conditions may occur during the instruction or execution phases of decimal arithmetic operations:

1. Operation Code Invalid
2. Addressing Error
   a. An instruction address or an operand address refers to the protected first 144 bytes of main storage.
   b. An instruction address or an operand address is outside available storage.
   c. An instruction occupies the last two (highest) main-storage positions.
3. Specification Error
   a. The low-order bit of an instruction address is 1.
   b. For Zero and Add, Compare Decimal, Add Decimal, and Subtract Decimal instructions, the length code L2 is greater than the length code L1.
   c. For Multiply Decimal and Divide Decimal instructions, the length code L2 is greater than 7 or greater than or equal to the length code L1.
4. Data Error
   a. A sign or digit code of an operand in the Zero and Add, Compare Decimal, Add Decimal, Subtract Decimal, Multiply Decimal, or Divide Decimal instruction is incorrect, or the operand fields in these instructions overlap incorrectly.
   b. The factor one field (first operand) in a Multiply Decimal instruction has insufficient high-order zeros.
5. Decimal Divide Check
   a. The resultant quotient in a Divide Decimal instruction exceeds the specified data field instruction (including division by zero) or the dividend has no leading zero.
6. CPU Parity Error.

LOGICAL OPERATIONS

A set of operations is provided for the logical manipulation of data. Generally the operands are treated as characters, eight bits at a time. In a few cases the left or right four bits of a byte are treated separately. The operands are either in storage or are introduced from the instruction stream.

Processing of data in storage proceeds left to right through fields which may start at any byte position.

Except for the Edit instruction, data is not treated as numbers in this section. Editing provides a transformation from packed decimal digits to alphameric characters.

The set of logical operations include move, comparison, editing, testing, and bit-connective operations.

The condition code is set as a result of all logical connective, comparison, editing, and testing operations.

Data Format

Data resides in storage, or is introduced from the instruction itself. The data size may be a single character, or variable in length. When two operands participate they have equal length, except in the Edit instruction.

In storage-to-storage operations, data has a variable field-length format, starting at any byte address (except for the first 144 storage-protected bytes) and continuing to a maximum of 256 bytes. Processing is left to right.

Operations which introduce data from the instruction into storage are restricted to an eight-bit byte. Only one byte is introduced from the instruction, and only one byte in storage participates.

Editing requires a packed decimal field; otherwise no internal data structure is required and all bit configurations are considered valid.

In storage-to-storage operations, the operand fields may be defined in such a way that they overlap. The effect of this overlap depends upon the operation. When the operands remain unchanged, as in compare, overlapping does not affect the execution of the operation. In the case of move and edit operations, one operand is replaced by new data, and the execution of the operation may be affected by the amount of overlap and the manner in which data is fetched or stored. For purposes of evaluating the effect of overlapped operands, it can be considered that data is always handled one eight-bit byte at a time. All overlapping fields are considered valid, but in the edit operations overlapping fields give unpredictable results.

Condition Code

The results of most logical operations are used to set the condition code. The move operations leave this code undisturbed. The condition code can be used for decision-making by subsequent branch on condition instructions.

There are four types of condition code settings for logical instructions. For the Edit instruction the codes 00, 01, and 10 indicate a zero, less than zero, and greater than zero content of the last result field.

For the logical connective operations, the codes 00 and 01 indicate a zero or nonzero result field.

For the Test Under Mask instruction, the codes 00, 01, and 11 indicate a zero, mixed zero and one, and all-one result field.

For the Compare Logical instruction, the codes 00, 01, and 10 indicate that the first operand compared equal, low or high. Table 4 shows the condition code for logical operations.

Table 4. Condition Code Settings for Logical Operations

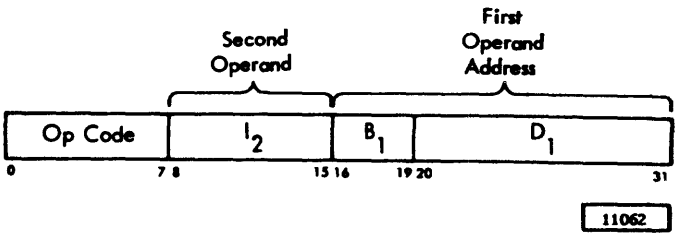
Condition Code	00	01	10	11
Test under Mask	zero	mixed	- -	one
And	zero	not zero	- -	- -
Compare Logical	equal	low	high	- -
Or	zero	not zero	- -	- -
Edit	zero	< zero	> zero	- -

11020

Instruction Format

Logical instructions use the SI or SS formats.

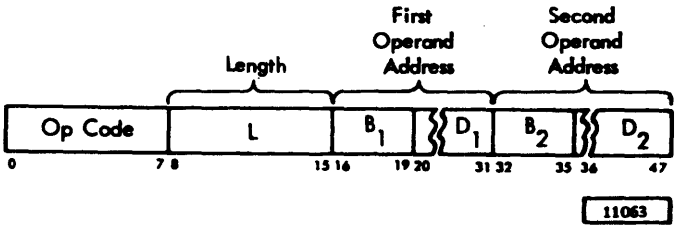
SI Format



In the SI format, the address which specifies the core storage location of the first operand field is derived from the contents of the B1-D1 fields of the instruction. The address may be taken directly from the B1-D1 Fields (direct addressing) or an effective address may be formed by adding the contents of the general register specified by the B1 field to the contents of the D1 field (effective addressing).

Results replace the first operand. The contents of the general registers are not changed.

SS Format



The address which specifies the core-storage location of the first operand field is derived from the B1-D1 fields of the instruction. The B2-D2 fields specify the leftmost byte of the second operand field. The first and second operand fields are the same length. The number of bytes extending to the right of the first byte is specified by the L field of the instruction.

The address of each operand may be derived by either direct or effective addressing. The result of the operation replaces the first operand, and is never stored outside the field specified by the address and length fields of the instruction. The contents of the general registers remain unchanged.

Instructions

The logical instructions, their mnemonics, formats, and operation codes are shown in Table 5.

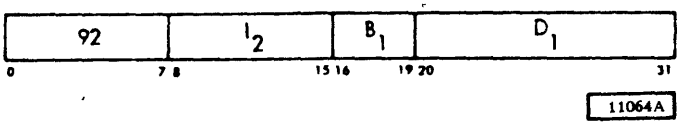
Table 5. Logical Instructions

Name	Mnemonic	Format	Operation Code
Move	MVI	SI	92
Move	MVC	SS	D2
Move Numerics	MVN	SS	D1
Move Zones	MVZ	SS	D3
Compare Logical	CLI	SI	95
Compare Logical	CLC	SS	D5
Edit	ED	SS	DE
And	NI	SI	94
Or	OI	SI	96
Test under Mask	TM	SI	91
Halt & Proceed	HPR	SI	99
Translate	TR	SS	DC

11021A

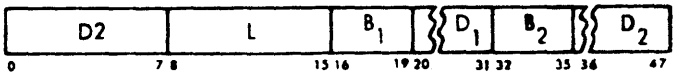
Move

MVI SI



11064A

MVC SS



11065A

The second operand is placed in the first operand location.

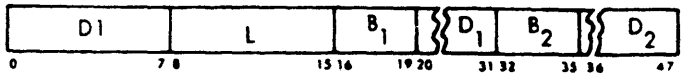
The SS format is used for a storage-to-storage move. The SI format introduces one eight-bit byte from the instruction stream.

In storage-to-storage movement, the fields may overlap in any desired way. Movement is left to right through each field, a byte at a time.

The bytes to be moved are not changed or inspected. The condition code remains unchanged. It is possible to propagate one character through an entire field by having the first operand field start one character to the right of the second operand field.

Move Numerics

MVN SS



11066A

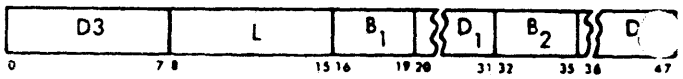
The low-order four bits of each byte in the second operand field, the numerics, are placed in the low-order bit positions of the corresponding bytes in the first operand field.

The instruction is storage-to-storage. Movement is left to right through each field, one byte at a time, and the fields may overlap in any desired way.

The numerics are not changed or checked for validity. The high-order four bits of each byte, the zones, remain unchanged in both operand fields. The condition code remains unchanged.

Move Zones

MVZ SS



11067A

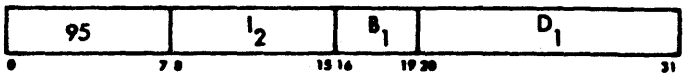
The high-order four bits of each byte in the second operand field, the zones, are placed in the high-order four bit positions of the corresponding bytes in the first operand field.

The instruction is storage-to-storage. Movement is left to right through each field one byte at a time, and the fields may overlap in any desired way.

The zones are not changed or checked for validity. The low-order four bits of each byte, the numerics, remain unchanged in both operand fields. The condition code remains unchanged.

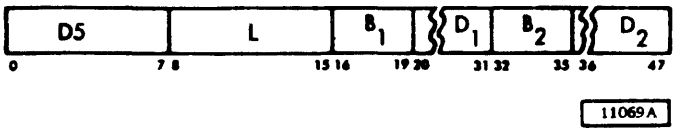
Compare Logical

CLI SI



11068A

CLC SS



The first operand is compared with the second operand, and the result is indicated in the condition code.

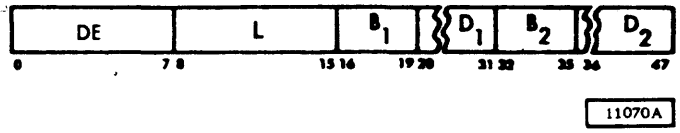
The instructions allow comparisons that are instruction-to-storage, and storage-to-storage.

Comparison is binary, and all codes are valid. The operation proceeds left to right and terminates as soon as an inequality is found. The condition code is made 00 if the operands are equal, 01 if the first operand is low compared to the second operand, and 10 if the first operand compares high.

In the Compare Logical instruction, all bits are treated alike as part of an unsigned binary quantity. In the variable length storage-to-storage operation, comparison is left to right and may extend to field lengths of 256 bytes. This instruction may be used for alphameric comparison.

Edit

ED SS



The format of the source (the second operand) is changed from packed to zoned and is edited under control of the pattern (the first operand). The edited result replaces the pattern.

Editing includes sign and punctuation control and the suppressing and protecting of leading zeros. It also facilitates programmed blanking of all-zero fields. Several numbers may be edited in one operation, and numeric information may be combined with text.

The length field applies to the pattern (the first operand). The pattern has the unpacked format and may contain any character. The source (the second operand) has the packed format and must contain valid decimal digit and sign codes. The left four bits of a byte must be 0000-1001. The right four bits are recognized as either a sign or a digit.

Both operands are processed left to right, one character at a time. Overlapping pattern and source fields give unpredictable results.

The character to be stored in the first operand field is determined by three things; the digit obtained from the source field, the pattern character, and the state of a trigger, called the S trigger. One of three actions may be taken:

1. The source digit is expanded to zoned format and is stored into the first operand.
2. The pattern character is left unchanged.
3. A fill character is stored into the first operand.

S Trigger: The S trigger is used to control the storing or replacing of source digits and pattern characters. Digits to be stored in the result, whether zero or not, are termed significant. Pattern characters are replaced or stored when they are significance-dependent (such as punctuations) or sign-dependent (such as credit symbols). The S trigger is also used to record the sign of the source and it sets the condition code accordingly.

The S trigger is set to the 0 state at the start of the operation and is subsequently changed depending upon the source number and the pattern characters.

Pattern Character: Three pattern characters have a special use in editing. They are the digit-select character, the significance-start character, and the field-separation character. These three characters are replaced, either by a source digit or by a fill character; their encoding is shown in Table 6.

1. The digit-select character causes either a source digit or the fill character to be inserted in the result field.
2. The significance-start character has the same function but also indicates, by setting the S trigger, that the following digits are significant.
3. The field-separation character identifies individual fields in a multiple-field editing operation. The character is replaced by the fill character. The S trigger is set to zero, and testing for a zero-field is reinitiated.
4. All other pattern characters are treated in a common way; if the S trigger is 1, the pattern character is left unchanged; if the S trigger is 0, the pattern character is replaced by the fill character.

If the pattern character is either a digit-select or a significance-start character, the source digit is examined. The source digit replaces the pattern character if the S trigger is 1 or if the source digit is nonzero. If a nonzero digit is inserted when the S trigger is 0, the S trigger is set to 1 to indicate that the subsequent digits are significant. If the S

Table 6. Edit Characteristics

Character Code	Name and Purpose	Examine Digit	Trigger Status	Digit Status	Result Character	Trigger Set
0010 0000	digit select	yes	s = 1		digit	
			s = 0	d not 0	digit	s = 1
			s = 0	d = 0	fill	
0010 0001	significance start	yes	s = 1		digit	
			s = 0	d not 0	digit	s = 1
			s = 0	d = 0	fill	s = 1
0010 0010	field separator	no			fill	s = 0
other	message insertion	no	s = 1		leave	
			s = 0		fill	

NOTES:

d	Source digit
s	S trigger (1: minus sign, digits, or pattern used; 0: plus sign, fill used)
digit	A Source digit replaces the pattern character.
fill	The fill character replaces the pattern character.
leave	The pattern character remains unchanged.

11022

trigger and the source digit are both 0, the fill character is substituted for the pattern character.

Source Digit: When the source digit is stored in the result, its code is expanded from the packed to the zoned format by attaching a zone. The zone code is 1111 in the binary-coded-decimal mode and 0101 in the ASCII mode. It depends on the mode bit of the PSW as to which type of zone is used. For example, if the mode bit is 0, 1111 (the EBCDIC zone) is used.

The source digits are examined only once during an editing operation. They are selected eight bits at a time from the second operand field. The leftmost four bits are examined first, and the rightmost four bits remain available for the next pattern character which calls for a digit examination. However, the rightmost four bits are inspected for a sign code immediately after the leftmost four bits are examined.

Any of the plus-sign codes 1010, 1100, 1110, or 1111 sets the S trigger to 0 after the digit is inspected, whereas the minus-sign codes 1011 and 1101 leave the S trigger unchanged. When one of these sign codes is encountered in the four right-most bits, these bits no longer are treated as a digit, and a new character is fetched from storage for the next digit to be examined.

A plus sign sets the S trigger to 0 even if the trigger was set to 1 for a nonzero digit in the same source byte or by a significance-start character for that digit.

Fill Character: The fill character is obtained from the pattern as part of the editing operation. The first character of the pattern is used as a fill character and is left unchanged in the result field, except when it is the digit-select or significance-start character. In the latter cases, a digit is examined and, when nonzero, inserted.

Result Condition: To facilitate the blanking of all-zero fields, the condition code is used to indicate the sign and zero status of the last field edited. All digits examined are tested for the code 0000. The presence or absence of an all-zero source field is recorded in the condition code at the termination of the editing operation.

1. The condition code is made 0 for a zero source field, regardless of the state of the S trigger.
2. For a nonzero source field and an S trigger of 1, the code is made 1 to indicate less than zero.
3. For a nonzero source field and an S trigger of 0, the code is made 2 to indicate greater than zero.

The condition-code setting pertains to fields as specified by the field-separator characters, regardless of the number of signs encountered.

For the multiple-field editing operations, the condition-code setting reflects only the field following the last field-separator character. When the last character of the pattern is a field-separator character, the condition code is made 0.

Table 6 gives the details of the edit operation. The leftmost columns give the pattern character and its code. The next columns show the states of the digit and the S trigger used to determine the resulting action. The rightmost column shows the new setting of the S trigger.

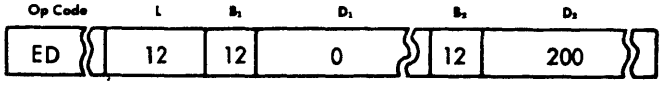
The following example shows the step-by-step editing of a packed field with a length specification of four against a pattern 13 bytes long. The following symbols are used:

Symbol	Meaning
b	blank character
((hexadecimal 21)	significance-start character
) (hexadecimal 22)	field-separation character
d (hexadecimal 20)	digit-select character

Assume:

Loc 1000-1012 (first operand)	bdd, dd(. ddbCR
Loc 1200-1203 (second operand)	02 57 42 6+
Reg 12 (decimal equivalent)	1000

The instruction is:



and provides the following

Pattern	Digit	S Trigger	Rule	Location 1000-1012
b		0	leave(1)	bdd, dd(. ddbCR
d	0	0	fill	bdd, dd(. ddbCR
d	2	1	digit	bb2, dd(. ddbCR(2)
,		1	leave	same
d	5	1	digit	bb2, 5d(. ddbCR
d	7	1	digit	bb2, 57(. ddbCR
(	4	1	digit	bb2, 574. ddbCR
.		1	leave	same
d	2	1	digit	bb2, 574. 2dbCR
d	6+	0	digit	bb2, 574. 26bCR(3)
b		0	fill	same
C		0	fill	bb2, 574. 26bbR
R		0	fill	bb2, 574. 26bbb

Thus:

Loc 1000-1012 (after) bb2, 574. 26bbb

NOTES

1. This character is saved as the fill character.
2. First nonzero digit sets S trigger to 1.
3. Plus sign in this same byte sets S trigger to zero.

Condition code = 2; result greater than zero.

If the second operand in location 1200-1203 is 00 00 02 6-, the following results are obtained:

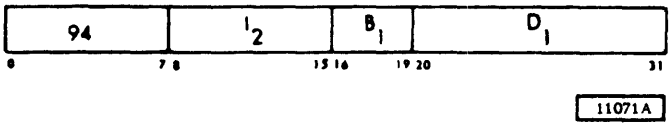
Loc 1000-1012 (before)	bdd, dd(. ddbCR
Loc 1000-1012 (after)	bbbbbb. 26bCR

Condition code = 1; result less than zero

In this case the significance-start character in the pattern causes the decimal point to be left unchanged. The minus sign does not reset the S trigger so that the CR symbol is also preserved.

And

NI SI



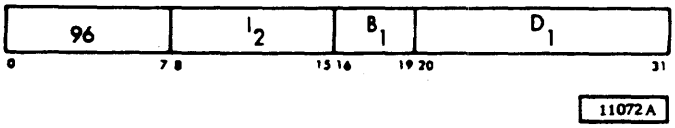
This instruction uses the SI format, which provides a single character instruction-to-storage operation. This instruction may be used to set a bit to 0.

The logical product (And) of the bits of the first and second operand is placed in the first operand location.

Operands are treated as unstructured logical quantities, and the connective And is applied bit by bit. All operands and results are valid. The condition code is set to zero (00) or not zero (01) according to the result of the operation. (See Table 4.)

Or

OI SI



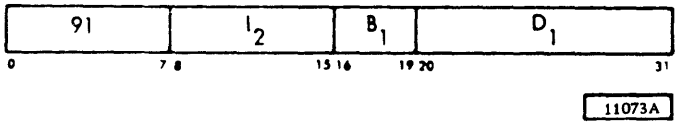
This instruction uses the SI format, which provides a single character instruction-to-storage operation. This instruction may be used to set a bit to 1.

The logical sum (Or) of the bits of the first and second operand is placed in the first operand location. The condition code is set to zero (00) or not zero (01) according to the result of the operation. (See Table 4.)

Operands are treated as unstructured logical quantities, and the connective inclusive Or is applied bit by bit. All operands and results are valid.

Test Under Mask

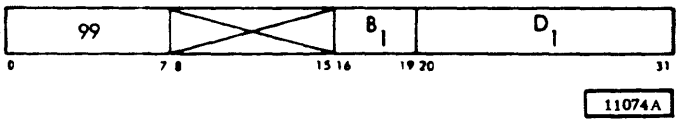
TM SI



This instruction inspects the first operand bits and compares them with the I2 field, which is the mask. If the first operand has 1 bits in exactly the same positions as the mask, the condition code is set to 11. If the 1 bits in the mask match some of the 1 bits in the first operand, the condition code is set to 01. If none of the 1 bits match or if the mask is zero, the condition code is set to 00. Neither the first operand nor the mask is changed.

Halt and Proceed

HPR SI



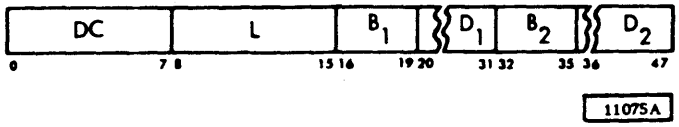
The Halt and Proceed instruction is used to stop the CPU. All input/output operations in progress are continued to completion.

When the CPU has been stopped by the Halt and Proceed instruction, the program may be resumed with the next sequential instruction by operating the Start key on the CPU console.

This instruction uses the SI format in which the I2 field is ignored. The direct or effective address derived from the B1-D1 fields may be used to identify the Halt and Proceed instruction. The condition code remains unchanged.

Translate

TR SS



The first operand contains the data that is to be translated. The second operand represents the translating list. The first operand is selected byte by byte proceeding from left to right. The binary value of each operand 1 byte (the argument) is added to the second operand (left byte) address. The resultant new address is used to select an appropriate byte from the translating list (second operand) which contains the function bytes. The selected function byte replaces the original argument byte in the first operand.

All data is valid. The operation proceeds until the first operand field is exhausted. It is permissible for the list and the first operand field to overlap. The condition code remains unchanged.

Error Conditions

Error conditions which may occur during the instruction or execution phase of logical operations are:

1. Operation Code Invalid
2. Addressing Error
   a. An instruction address or an operand address refers to the protected first 144 bytes of main storage (addresses 0 to 143).
   b. An instruction address or an operand address is outside available storage.
   c. The last (highest) main-storage position contains any part of an instruction that is to be executed.
3. Specification Error
   a. The low-order bit of an instruction address is 1.
4. Data Error
   a. An invalid digit code is contained within the second operand field of an Edit operation.
5. CPU Parity Error.

BRANCHING

Instructions are performed by the CPU primarily in the sequential order of their locations. A departure from this normal sequential operation may occur when branching is performed. The branching instructions provide a means for making a two-way choice, to reference a subroutine, or to repeat a segment of coding, such as a loop.

Branching is peformed by introducing a branch address as a new instruction address.

The branch address may be obtained from one of the general registers or it may be the address specified by the instruction. The branch address is independent of the updated instruction address. Branching may be conditional or unconditional. Unconditional

branches always replace the updated instruction address with the branch address. Conditional branches may use the branch address or may leave the updated instruction address unchanged. When branching takes place, the instruction is called successful; otherwise, it is called unsuccessful.

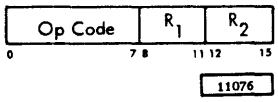
Whether a conditional branch is successful depends on the result of operations preceding the branch. An example is the Branch on Condition instruction, which inspects the condition code that reflects the result of a previous arithmetic or logical operation.

During a branching operation, the rightmost half of the PSW, the updated instruction address, may be stored before the instruction address is replaced by the branch address. The stored information may be used to link the new instruction sequence with the preceding sequence.

Instruction Format

Branching instructions employ the RR, RX, and the SI formats.

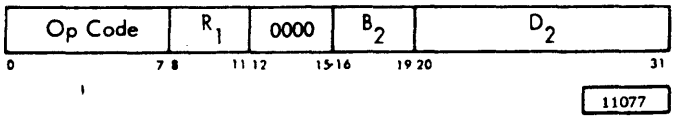
RR Format



The R1 field may specify a general register into which the updated instruction address is to be stored as link information, or may contain a mask which is employed to identify the bit values of the condition code.

The R2 field specifies the general register which contains the branch address.

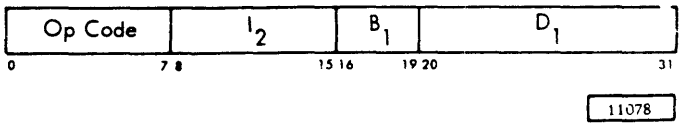
RX Format



The R1 field may specify a general register into which the updated instruction address is to be stored as link information, or may contain a mask which is employed to identify the bit values of the condition code.

The direct or effective address derived from the B2-D2 fields is the branch address.

SI Format



The SI format is employed by only one branching instruction, Set PSW. The direct or effective address derived from the B1-D1 fields specifies the location of a word in main storage which is to replace the Program Status Word (PSW); the contents of the I2 field are ignored.

Instructions

The branch instructions, their operation codes, formats, and mnemonics are shown in Table 7.

Table 7. Branch Instructions

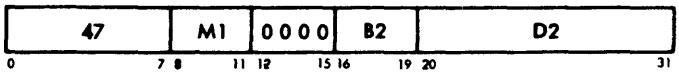
Name	Op Code	Format	Mnemonic
Branch on Condition	07	RR	BCR
Branch on Condition	47	RX	BC
Branch & Store	0D	RR	BASR
Branch & Store	4D	RX	BAS
Set PSW	81	SI	SPSW

11023A

Branch on Condition

BCR RR

BC RX



The updated instruction address is replaced by the branch address if the state of the condition code is

as specified by M1; otherwise, normal instruction sequencing proceeds with the updated instruction address.

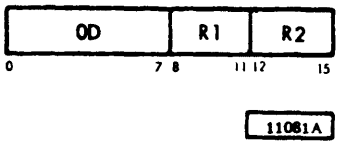
The M1 field is used as a 4-bit mask. The four bits of the mask correspond, left to right, with the four condition codes, 0, 1, 2, and 3, as shown in the following table. The branch is successful whenever the condition code has a corresponding mask bit of one. The condition code is not changed.

Condition Code	Instruction Bits
0 (0 0)	8
1 (0 1)	9
2 (1 0)	10
3 (1 1)	11

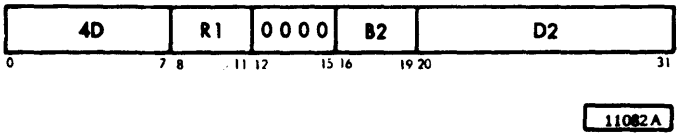
When all four mask bits are ones, the branch is unconditional. When all four mask bits are zero or when the R2 field in the RR format contains zero, the branch instruction is equivalent to a no operation. Refer to Appendix G for a table of all operations which affect the condition codes.

Branch and Store

BASR RR



BAS RX



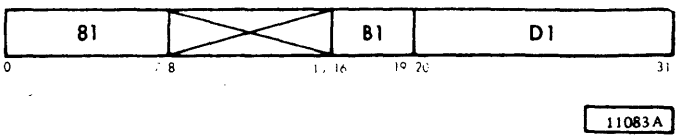
The rightmost 16 bits of the PSW, the updated instruction address, are stored as link information in the general register specified by R1. Simultaneously the instruction address is replaced by the branch address.

The condition code remains unchanged.

When in the RR format, the R2 field contains zero, the link information is stored without branching.

Set PSW

SPSW SI

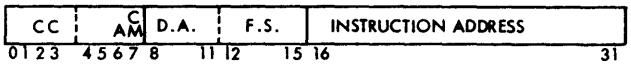


The 32-bit word (four eight-bit bytes), located in main storage with the leftmost byte at the first operand address, replaces the program Status Word (PSW).

Bits 8-15 in the Set PSW instruction are ignored.

The PSW has a fixed length format of one word. It is located in an unaddressable register in the CPU and is employed as an internal control. Since the PSW contains the address of the next sequential instruction, the Set PSW instruction is equivalent to a branch operation.

PSW Format



0 - 1	Not used
2 - 3	Condition Code
4 - 5	Not used
6	* ASCII MODE BIT
7	Channel Mask
8 - 11	Device Address
12 - 15	Function Specification
16 - 31	Instruction Address

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Programming Notes

1. The instruction address portion of the word which is transferred from main storage to the PSW by the Set PSW instruction should:
   a. Not refer to the protected first 144 bytes of main storage,
   b. Have the least significant bit zero, and
   c. Be within the limits of available storage.

   If these conditions are not satisfied, an addressing or specification error stop will occur.
2. The condition code is set by the Set PSW instruction to the value contained in the word transferred from main storage to the PSW.
3. Main-storage boundaries are not required of the first operand address in the Set PSW instruction.

4. The condition code, ASCII mode bit, and channel mask in the PSW are zero when the CPU is in the reset state. The instruction address portion of the PSW is not changed when the CPU is reset.

Error Conditions

Error conditions which may occur during a branching operation are:

1. Operation Code invalid.
2. Addressing Error.
   a. An instruction address or a branch address refers to the protected first 144 bytes of main storage.
   b. An instruction address or a branch address is outside available storage.
   c. The R1 field of a Branch and Store instruction contains binary values 0 through 7, or the R2 field of an RR format branch instruction contains binary values 1 through 7.
   d. An instruction part is located in the last (highest) two main storage positions.
3. Specification Error.
   a. The low-order bit of an instruction address is 1.
   b. Bits 12 through 15 of an RX format instruction are not all 0.
4. CPU Parity Error.

CPU CONSOLE

The CPU console (Figure 5) provides the switches, keys, and lights necessary to operate and control the system.

Additional switches and indicators are located on the various input/output devices which are included in the system. These switches and indicators control functions or indicate conditions peculiar to the input/output unit on which they are located, and are not considered as system controls.

Operating Keys and Indicators

Process Indicator

The CPU stops with the Process indicator on when an error occurs in the CPU. This condition may be reset only by operating the System Reset key.

Card I/O Device No. 1 Indicator

A condition which requires operator intervention exists on card I/O device No. 1, the IBM 2501 Card Reader, when this indicator is on.

Card I/O Device No. 2 and No. 3 Indicators

The same as for I/O Device No. 1 indicator, but for the input/output device designated by the indicator.

Register Display Indicators

The eight primary data registers in the CPU are displayed on the console.

Printer Indicator

A condition which requires the attention of the operator exists on the printer when this indicator is on. Refer to the Operating Conditions section of this manual for further details.

System Reset Key

Operation of the System Reset key stops the CPU immediately, including all I/O operations which may be in progress. All error conditions are reset. The condition code, channel mask, and the mode bit in the Program Status Word (PSW) are reset to zero. A system reset sets the mode to EBCDIC. The instruction address portion of the PSW is not changed. All registers displayed on the console are reset to zero, i.e., all bit-lights are off except the parity bits (P). The system reset function is also performed when the power on or program load sequences are initiated.

Start Key

The Start key is used to start or resume operation of the CPU.

Stop Key

Operation of this key stops the CPU at the completion of the execution of the instruction in progress when the key was depressed. All time-shared I/O operations in progress continue to completion.

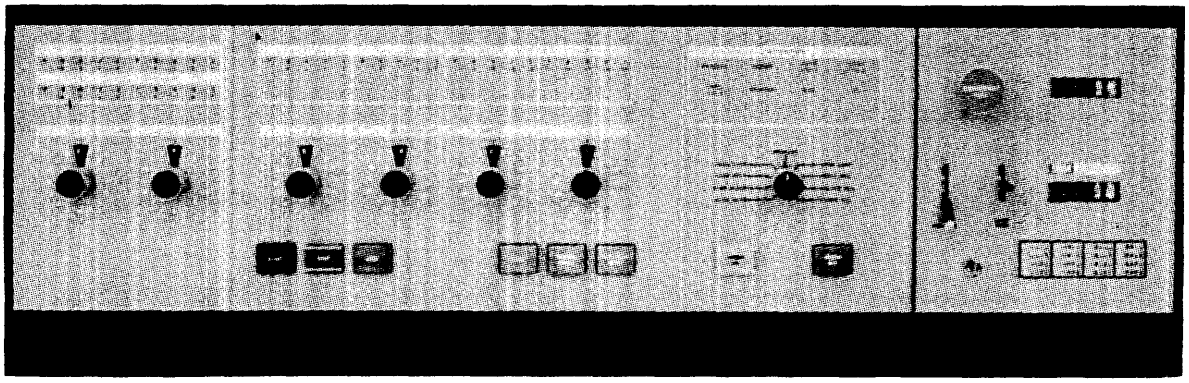

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Figure 5. CPU Console

Stop Key Indicator

The Stop Key indicator is on when the CPU is stopped any condition.

Program Load Key

The following conditions must be established before the program load function is operable:

1. The Mode switch on the CPU console must be in the Process, Address Stop, or Instruction Step position.
2. Card I/O No. 1 device must be in a Ready Condition.

When these conditions are established, operation of the Program Load key initiates the system reset function, followed by a read-card operation starting at the main-storage location set in the Address/ Register Data switches.

If the Mode switch is in any position other than Process, Address Stop, or Instruction Step when the Program Load key is operated, the CPU performs the system reset function and stops.

The IBM System/360 Model 20 may include one or two card I/O devices capable of reading cards.

In order that common program load routines may be employed on systems with different card I/O equipment, device 2 responds to the device 1 (2501 Card Reader) instruction when device 1 is not included in the system.

The device 1 instructions to which device 2 responds are the following:

Device 2 Response	Device 1 Instruction
Read (Primary feed if 2560)	Read Card
Branch if Reader Busy	Branch if Reader Busy
Branch if Reader Error	Branch if Reader Error

A device 2 instruction in a system which does not include device 2 is treated as a no-operation.

I/O Check Reset Key

Operation of the I/O Check Reset key resets all program testable I/O error indicators. Further details are provided in the section on Operating Conditions.

Power On Key

The power-on sequence is initiated when this key is operated if power is not on. Operation of the Power On key has no effect if power is on.

Power Off Key

Operation of the Power Off key removes power from the system.

Attention Indicators

The Attention indicators show the particular condition or the particular I/O device that has caused the system to stop. In this manner the operator is guided quickly to the respective device and an inspection of its console defines the stop condition in detail.

Process: This indicator shows that an error has occurred within the CPU. All operations are halted immediately and usually the attention of a Customer Engineer is required. However, operations can be resumed by first pressing the System Reset key and then loading the program again.

Power: This indicator shows that a power failure has occurred in either the CPU or in an I/O device such as the IBM 2415 Magnetic Tape Unit. A power failure is defined as the loss of any of the voltages that are generated by the power supply or as an overheating condition in any of the gates in the CPU or I/O devices. Restore power by first pressing the System Reset key and then the Power On key.

Card I/O 1: This indicator shows an unusual condition in the IBM 2501 Card Reader. These conditions can be a filled stacker, an empty hopper, an open machine cover, a read check, a feed check, or a machine check. Machine checks usually require action from a Customer Engineer.

Card I/O 2: This indicator shows an unusual condition in either the IBM 2560 Multi-Function Card Machine or in the IBM 2520 Reader/Punch (whichever is attached). The condition can be filled stacker, empty hopper, open machine cover, feed check, read check, punch check as well as machine check.

Card I/O 3: This indicator relates to the IBM 1442 Card Punch, Model 5. Conditions such as feed check, empty hopper, full stacker etc. cause this indicator to light.

Printer: This indicator shows an unusual condition in either the IBM 2203 Printer or the IBM 1403 Printer. These conditions can be mis-firing of hammers, sync check, or forms check.

SIOC: This indicator shows that either the serial I/O channel or the device that operates through this channel such as the IBM 1419 Magnetic Character Reader has an error condition. For example, a jam or sort check in the 1419 causes the SIOC-light to come on.

IOC: This indicator shows that either the input/output channel or the device that operates through this channel has an error condition. For example, a programing error that involves the IBM 2415 Magnetic Tape Units, or an interface parity error causes the IOC-light to come on.

Emergency Off Switch

In an emergency, this switch may be pulled to immediately disconnect all power from the system. This switch must be manually reset by a Customer Engineer before power may be restored to the system.

Control Switches

Mode Switch

Process: In the Process position, the CPU operates under control of the stored program. Further details are provided in the section on Operating Conditions.

Address Stop: The CPU stops when the program has reached the instruction which is located at the main storage address indicated on the Address/Register Data switches, otherwise the same as process mode. When an interrupt occurs and the stop address set up on the Address/Register/Data switches is identical with the instruction address contained in the new PSW the CPU does not stop on this address.

Instruction Step: In this mode of operation, the CPU executes one complete instruction for each operation of the Start key. Since the interrupt condition is always tested prior to the execution of an instruction, it is possible that an interrupt occurs when the Start key is pressed; in this case, the CPU stops after the instruction that is designated by the address in the new PSW is executed.

Storage Display: The eight-bit byte of data located in main storage at the address indicated on the Address/Register Data switches is displayed in the U-L register when the Start key is operated. The address of this byte of data is displayed in the E-S-T-R registers.

Storage Alter: To alter the contents of a main-storage byte, the operator must set the Address/Register Data switches to the desired location and select the bit configuration of the eight-bit byte of data to be entered by setting the two Data switches. When the Start key is operated, the byte indicated on the Data switches is entered. The byte which was entered is displayed in the U-L registers and the address of this byte is displayed in the E-S-T-R registers.

The eight-bit byte of data is represented in hexadecimal notation on the Data Switches. Data switch 1 selects the configuration of bits 0 1 2 3 and Data switch 2 selects the configuration of bits 4 5 6 7.

Register Display: The contents of the eight general registers and also the contents of certain address registers may be displayed in this mode of operation. The register to be displayed must first be selected by Data switch 1 according to Table 8.

The operator may then display the contents of the selected register in the E-S-T-R registers by operating the Start key. The number of the register selected is displayed as a four-bit binary number in the P register.

The first halfword of the last instruction executed (Op Code plus byte two of the instruction) may be displayed in the E-S-T-R registers in this mode when Register 0 is selected (Table 8).

Register Alter: The contents of the eight general registers and certain address registers may be altered in this mode of operation. The register to be altered must first be selected by Data switch 1 as shown in Table 8. The data to be entered into the selected register is set on the four Address/Register Data switches. When the Start key is operated, the data is entered into the selected register. The data which was entered is displayed in the E-S-T-R registers and the number of the selected register is displayed as a four-bit binary number in the P register.

Table 8. Data Switch 1

Data Switch 1		Register Selected
0	(0000)	First two bytes of previous instruction
1	(0001)	I-Recall Address Register
2	(0010)	PSW (bits 0-15)
3	(0011)	PSW (bits 16-31)
4	(0100)	- -
5	(0101)	- -
6	(0110)	- -
7	(0111)	- -
8	(1000)	General Register 8
9	(1001)	General Register 9
A	(1010)	General Register 10
B	(1011)	General Register 11
C	(1100)	General Register 12
D	(1101)	General Register 13
E	(1110)	General Register 14
F	(1111)	General Register 15

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Storage Scan: In this mode of operation, the CPU starts at the address indicated on the Address/Register Data switches when the Start key is operated. It scans through main storage (from low to high) until a parity error is detected or the Stop key is operated. If the end of main storage is reached during the scan, the scan continues from the beginning of main storage.

Storage Fill: In this mode of operation, the CPU enters the contents of Data switches 1 and 2 into all positions of main storage, starting at the address indicated by the Address/Register Data switches. Operation of the Start key causes the loading of storage to begin. The loading proceeds from low address locations to high address locations, and wraps around from the high end of main storage to the low end of main storage. The loading operation is terminated by operation of the Stop key.

If the Mode switch is turned from the Process or Address Stop positions to any other position except Instruction Step while the CPU is operating under control of the stored program, operation of the CPU continues as if in the Process mode until a programmed stop or an error stop occurs, or until the Stop or System Reset key is operated. If the Mode switch is turned to the Instruction Step position while the CPU is operating, the central processing unit stops in the same manner as if the Stop key had been operated.

Data Switches

Data switches 1 and 2 are physically located on the CPU console below the U and L registers. They are 16-position rotary switches with hexadecimal notation. Data switch 1 selects the configuration of bits 0 1 2 3 and Data switch 2 selects the configuration of bits 4 5 6 7 in an eight-bit byte of data in Storage Alter mode. Data switch 1 is also used for register selection in the Register Display and Register Alter modes. The hexadecimal representation for all bit combinations of an eight-bit byte is shown in Appendix E.

The position of the Data switches may be changed without disturbing CPU operation.

Address/Register Data Switches

The four 16-position rotary Address/Register Data switches are numbered 1, 2, 3, 4 from left to right and are physically arranged on the CPU console directly below the E-S-T-R registers. These switches have hexadecimal notation. A hexadecimal-decimal conversion table is presented in Appendix E. Refer to the Address Stop, Register Display, and Register Alter modes for the functions of the Address/Register Data switches.

The position of the Address/Register Data switches may be changed without disturbing CPU operation, except that a stop may occur if in the Address Stop mode.

Time-Sharing Switch

When this switch is on, the execution of input/output operations is time-shared with other CPU operations When the switch is off, each input/output operation is completely executed before the CPU continues with the next sequential instruction.

Lamp Test Switch

This switch may be employed to visually check for burned out indicator lamps. All indicators should be on when the Lamp Test switch is on, except the indicators on the IBM 1403 Printer.

Operating Conditions

During normal operation of the CPU under control of the stored program, the Stop indicator on the CPU console is turned off. This indicator is on for all stop conditions of the CPU. Three types of stop conditions may occur.

1. Process check — A process check indicates some fault in the CPU such as an even parity. It can be reset by operating the System Reset key.
2. A normal stop — In this case, only the Stop indicator is on.
3. A programming error stop — In this case, the Stop indicator as well as an error number display in data register I is on. The error number in data register I is displayed in the binary coded form. For example, the code 0111 represents the number 7 and indicates that the second operand of a decimal instruction is equal to or greater in size (field length) than the first operand.

For normal stop conditions other than a programmed halt operation, the operation code of the Next Sequential Instruction (NSI) is displayed in the U-L registers and the address of the NSI is displayed in the E-S-T-R registers on the CPU console.

For a programmed halt operation, the halt operation code is displayed in the U-L registers and the

direct or effective address derived from the B1 and D1 fields of the instruction is displayed in the E-S-T-R registers.

For programming error stop conditions, the operation code of the instruction in which the error condition occurred is displayed in the U-L registers, and the address of this instruction is displayed in the E-S-T-R registers.

Normal Stop Conditions

A normal stop of the CPU occurs as a result of:

1. Operation of the Stop key.
2. A programmed halt operation.
3. An address stop in the Address Stop mode.
4. Operation in the Instruction Step mode.

The CPU is also in a normal stop condition following operation of the System Reset key or when power is first applied, but all register displays are blank (0000).

The CPU starts with the instruction located at the address contained in the program status word (bits 16-31) when the Start key is operated. The Program Status Word (PSW) contains the address of the NSI when the CPU stops as a result of one of the conditions listed above.

All input/output operations in progress when the CPU stops as a result of the conditions listed above are completely executed. All input/output operations in progress are terminated when the System Reset key is operated.

Programming Error Stop Conditions

A programming error stop occurs as a result of the conditions listed below. With each condition is a four-bit binary number which is displayed in the I register when a stop due to the error condition occurs.

1. Operation Code Invalid (0001)
2. Addressing Error
   a. An instruction address or an operand address refers to the protected first 144 bytes of main storage (0100).
   b. An instruction address or an operand address is outside available storage (0101).
   c. The R1 or R2 fields of an RR or an RX format binary instruction contain binary values 0 through 7, the R1 field in a Branch and Store instruction contains binary values 0 through 7, or the R2 field of an RR format branch instruction contains binary values 1 through 7 (0101).
   d. An instruction byte is located at the last available storage position (0101).
3. Specification Error
   a. An instruction address is not located on a half-word boundary of main storage (0110).
   b. A binary operand is not located on a specified boundary of main storage (0110).
   c. For Decimal Add, Decimal Subtract, Zero and Add, and Decimal Compare instructions, the length code L2 is greater than the length code L1 (0110).
   d. For Decimal Multiply and Decimal Divide instructions, the length code L2 is greater than 7 or greater than or equal to the length code L1 (0110).
   e. Bits 12 through 15 of an RX format instruction are not all zero (0110).
   f. A 2560 Write Card instruction is encountered in the program and there is no card in the punch or print station or no print head has been selected (0110).
   g. The field length specified in an input/output instruction is zero or is greater than the maximum allowable number for the I/O device addressed (0110).
4. Binary Overflow Check (1000)
5. Data Error
   a. A sign or digit code of an operand in the decimal instructions Zero and Add, Add, Subtract, Compare, Multiply, or Divide is incorrect or the operand fields in these operations overlap incorrectly (0111).
   b. The multiplicand field (first operand) in a Decimal Multiply instruction has insufficient high-order zeros (0111).
   c. An invalid digit code is contained within the second operand field of an Edit operation (0111).
6. Decimal Divide Check (1011)

If the Start key is operated before the error condition is corrected, the CPU again attempts to execute the instruction in which the error occurred.

If the error is corrected without altering the contents of the program status word, the CPU executes the instruction in which the error occurred and continues with the program when the Mode switch is placed in the Process or Address Stop position and the Start key is operated. Caution must be exercised in the case of error conditions that occur during the

actual processing of data. A second attempt to execute an instruction which has previously been partially executed without reconstructing the first operand causes erroneous results.

All input/output operations in progress when the central processing unit stops as a result of a programming error condition are completely executed.

If an address which is outside available storage is encountered during an input/output data transfer, the transfer and the input/output operation are terminated as if the complete data field as specified in the input/output instruction had been transferred; an error condition does not occur.

Process Error Stop Conditions

When an internal parity error occurs in the central processing unit, the CPU stops immediately. All input/output operations in progress are terminated.

The Process indicator on the CPU console will be on. The process error condition must be reset by operation of the System Reset key on the CPU console.

After a process error, the restart procedure cannot be used. The program must be loaded again and started either from the beginning or at a check point.

Transfers of information to main storage from sources external to the CPU and from main storage to external destinations are referred to as input/output operations. There are three types of instructions for input/output operations; Transfer, Control, and Test I/O and Branch instructions.

A Transfer instruction (XIO) controls the transfer of data between main storage and the input/output device.

A Control instruction (CIO) directs an input/output device to perform a specified function; e.g., select a stacker pocket or initiate a carriage skip.

A Test I/O and Branch instruction (TIOB) causes an inquiry to an input/output device for a particular condition (e.g., reader busy or end of form); if the tested indicator is on, the program branches to the specified address.

If the Time-Sharing switch is on, processing operations in the CPU are time-shared with the transfer of data between main storage and the input/output devices. When an input/output device requests service, processing is suspended only for the time required to send or accept the input/output data.

Data Format

Input/output data is located in eight-bit bytes in main storage in variable-length fields. Input/output data may be in the zoned, binary, or packed format. The data format in which an input/output device may accept or present data is, however, a characteristic of the device.

Input data is translated from the code form of the input device to the Extended-Binary Coded Decimal Interchange Code employed by the CPU internally as the data is received. Output data is translated from the internal CPU code to the code form of the output device as the data is transferred.

Condition Code

The status of an I/O device addressed by a Transfer I/O instruction, and under certain conditions, a Control I/O instruction, is used to set the condition code of the PSW at the time the execution of the instruction is completed. The condition code indicates whether or not the I/O device has initiated the operation specified, and if not, the reason for the rejection. The condition code can be used for decision making by subsequent branching operations.

The condition code is set to 00, 01, or 11 by an instruction to indicate the status of the I/O device addressed. The condition code 10 does not occur.

Condition Code	Status
00	Available (A)
01	Working (W)
11	Not Operational (N)

Available: Indicates that the addressed I/O device is operational, does not contain data or error check conditions, and is not busy with a previously initiated operation.

Working: Indicates that the addressed I/O device is executing a previously initiated operation.

Not Operational: Indicates that the addressed I/O device is in a not ready status, or an error or a data check condition exists on the device.

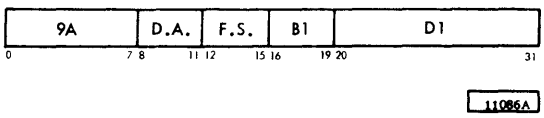
The operation specified by an XIO or CIO instruction is initiated only when the addressed I/O device is in the available state. If an I/O device is specified which is not a part of the system, a no-operation occurs, and the condition code is not changed.

Instruction Format

The three input/output instructions and their formats are as follows:

Test I/O and Branch

TIOB IO



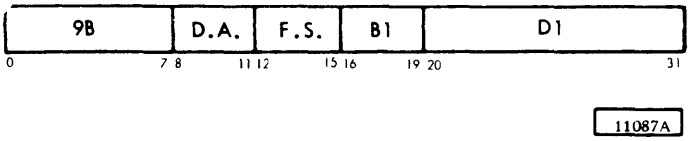
The Device Address (DA) specifies the I/O device in which a condition is to be tested.

The Function Specification (FS) specifies the particular condition or indicator to be tested in the I/O device addressed.

If the condition tested in the addressed I/O device is on, the updated instruction address is replaced by the branch address derived from the B1-D1 fields; otherwise, normal instruction sequencing continues with the updated instruction address.

Control I/O

CIO IO



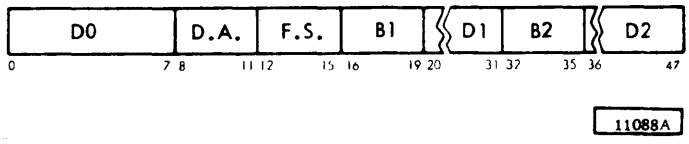
The Device Address (DA) specifies the I/O device in which a control function is to be performed.

The Function Specification (FS) specifies the particular component (it may also specify the primary function of that component) in the I/O device addressed.

A detailed specification of the control function to be performed is derived from the contents of the B1-D1 fields, according to the rules for direct or effective address generation. If the detailed specification derived from the B1-D1 field is all zero, a no-operation occurs.

Transfer I/O

XIO IO



The Device Address (DA) specifies the I/O device to which output data is to be transmitted, or from which input data is to be received.

The Function Specification (FS) specifies the input or output function to be performed on the I/O device addressed, and also the particular component of the addressed device (when required).

The main-storage location of the first byte in the input or output data field is derived from the contents of the B1 - D1 fields according to the rules for direct or effective address generation.

The field or record length of the input or output data in main storage is derived from the contents of the B2 - D2 fields.

The field length specifications for input or output data fields in main storage is the actual number of bytes in the field. Whereas for variable field length processing operations, the field length specification is the number of bytes extending beyond the first byte.

Error Conditions

Error conditions which may occur in the CPU during the instruction or service phases of input/output operations are listed below. Error conditions which may occur in I/O devices are included in the IBM Systems Reference Library publication for the respective device.

1. Operation Code Invalid
2. Addressing Error
   a. An instruction address or the address of an input/output data field refers to the protected first 144 bytes of main storage.
   b. An instruction address, the address of an input/output data field, or a branch address is outside available storage.
   c. An instruction part is located in the last two main-storage positions.
3. Specification Error
   a. The low-order bit of an instruction address is one.
   b. A 2560 Write Card instruction is encountered in the program and there is no card in the punch or print station, or when no print head has been selected.
   c. The field length specified for an input/output data field is zero or is greater than the maximum allowable number for the I/O device addressed.
4. CPU Parity Error

An input/output instruction containing an I/O device address which specifies a device not attached to the system is treated as a no-operation.

Interruption

Interruption is the general term applied to an automatic branch in the CPU program. The branch is automatic in the sense that it occurs when the condition exists, and is independent of a programmed branch instruction.

In the System/360 Model 20, interruption is provided only for the channel end input/output condition. Channel end condition of an input/output device is defined as the time (in the mechanical cycle of the device) at which the data transfer has been completed.

In the time-shared mode of operation of the CPU and the input/output devices, the transfer of data between the input/output devices and main storage in the CPU is asynchronous with respect to processing operations. Thus, the channel end condition of an input/output data transfer operation may occur at any time in the instruction or execution phase of any processing operation. It is also possible that more than one input/output device would reach the channel end condition during a specific processing operation. The channel end conditions are stored

in the form of interrupt bits. These bits are reset when the respective interrupts occur or are reset by a system reset or load operation.

The CPU is in an interruptible state when the channel mask bit in the Program Status Word (PSW) is 1, and is in a non-interruptible state when this bit is 0. The channel mask bit is reset to 0 by operation of the System Reset or Program Load key. The channel mask bit may be altered by a Set PSW instruction or by an interruption.

When the CPU is in the interruptible state (channel mask bit is 1), a test is performed by the CPU at the end of each processing operation to determine whether or not a channel end condition exists for any input/output device. (The instruction and start phases of input/output operations are also considered as processing operations.)

The test for a channel end condition is performed in an established priority sequence. The program continues with the next sequential instruction if no channel end conditions exist. When one or more end conditions exist, the first one encountered in the priority sequence causes an interruption to occur. The channel end condition which causes the interruption is reset. The interruption is performed by storing the PSW in fixed main-storage location 144 and obtaining a new PSW from another fixed main-storage location (148) before the program continues. Since the new PSW contains the address of the next sequential instruction, the interrupt is equivalent to a branch operation. The PSW which is stored in main storage location 144 is referred to as the old PSW.

The old PSW (stored at main storage location 144 when an interrupt occurs) contains the device address of the I/O device which caused the interruption (bits 8-11); the primary function which the device was performing (bits 12-15); the address of the next sequential instruction, and the condition code. Primary functions are read, punch, or print; not included are details such as which feed was in use for a read operation on the MFCM.

The following is a list of device addresses and function specifications contained in bits 8 to 15 of the old PSW stored at main-storage location 144 when an interruption due to the corresponding channel end condition occurs. The list is in the priority sequence for these interruptions.

Channel End Condition	DA	FS
1419 Read	0110	0110
2501 Read Card	0001	0010
2520 or 2560 Read Card	0010	0010
1403 or 2203 Print	0100	0000
CA Receive or Transmit	0101	0110
2560 Punch Card	0010	0100
1442 Punch Card	0011	0100
2560 Write Card	0010	0000
2520 Punch Card	0010	0100
Input/Output Channel	0111	0000
Disk Storage 1	1000	0000
Disk Storage 2	1000	0000
CC2 Interrupt	1111	0000

The channel mask bit in the new PSW (obtained from main-storage location 148) may be used to disable further interruptions in the routine which begins at the next sequential instruction address specified in the new PSW. As a means of returning to the point in the program at which the interruption occurred, a Set PSW instruction, in which the specified address is 144, may be used as the last instruction in the routine.

CC2 Interrupt

High-speed I/O devices that operate in burst mode only (such as the IBM 2415 Magnetic Tape Unit and the IBM 2311 Disk Storage Drive), cannot operate simultaneously with the other I/O devices that operate in time-sharing mode (such as card machines, communications adapter). However, if the program issues an instruction that addresses a burst-mode device while time-shared operations are in progress, the condition code (CC) is set to 2 (binary 10) and the program continues with the next sequential instruction. Due to this particular condition code, a special CC2 interrupt occurs when all time-shared operations (including stacker selection) are completed, provided that the channel mask bit in the PSW is present and no interrupt request with a higher priority is pending. Because the CC2 interrupt has the lowest priority, the program can branch back to start the previously-ignored burst-mode operation when the CC2 interrupt occurs; this is the earliest moment possible at which the CPU is available for burst-mode operations.

Last Card Control

Each card I/O device which has a card reading unit is provided with a testable Last Card indicator.

The last card condition in the 2501 Card Reader is set when a Read Card instruction for the 2501 is encountered in the program and there is no card at the read station. The channel end condition is set and the 2501 is placed in a not-ready status. The Last Card indicator may be tested and is reset by a Test I/O and Branch instruction in which the device address is 1 and the function specification is 4. The Last Card indicator is also reset when a new deck of cards is run in on the 2501 and the first Read Card instruction is encountered in the program; or it can be reset by the system reset function of the CPU.

The Last Card indicator in the IBM 2520 Card Read Punch is set when a Read Card instruction for the 2520 is encountered in the program and there is no card at the pre-read station. The channel end condition is set immediately and a card at the punch station is ejected to the stacker. The 2520 becomes not ready when both the pre-read and the pre-punch stations are empty while a Transfer I/O instruction is in progress. The indicator may be tested, and is reset by a Test I/O and Branch instruction in which the device address is 2 and the function specification is 4. The Last Card indicator is also reset when a new deck of cards is run in on the 2520 and the first Read Card instruction is encountered in the program; or it can be reset by the system reset function of the CPU.

The Last Card indicator in the 2560 MFCM is set when a Read Card instruction for the 2560 is encountered in the program and there is no card at the read station of the specified feed. The channel end condition is set immediately and cards remaining in the specified feed are advanced one station. The feed which is empty remains in a ready status in order that a Write Card instruction may be executed for the last card and in order that a subsequent Read Card instruction may be employed to advance the last card to the stacker. The Last Card indicator may be tested and is reset by a Test I/O and Branch instruction in which the device address is 2 and the function specification is 4. The Last Card indicator is also reset when a new deck of cards is run in on the empty feed of the 2560 and the first Read Card instruction for that feed is encountered in the system program; or it can be reset by the system reset function of the CPU.

IBM 1442 CARD PUNCH, MODEL 5

Introduction

The IBM 1442 Card Punch, Model 5 provides punched card output for the System/360 Model 20. The 1442-5 consists of a card hopper, a serial punch station, and one radial stacker. Card punching is done serially at a maximum rate of 160 columns/second. The card punching rate depends upon the number of columns specified in the Punch instruction. Punching speed may range from 265 cards/minute for punching columns 1-10, to 91 cards/minute for punching columns 1-80.

The 1442-5 has a 1200 card hopper capacity and a 1300 card stacker capacity.

1442 Card Punch Instructions

Transfer Instructions (XIO)

Function	Op Code	DA	FS
Punch and Feed	D0	3	6

The direct or effective address (derived from the B1-D1 fields of the instruction) specifies the left-most byte of the output data field in main storage. The length of the output field is derived from the B2-D2 fields of the instruction.

The field length specification is restricted to binary values equal to or less than 80.

Upon completion of a Punch and Feed instruction, the card which was punched is ejected to the stacker and the next card is fed from the hopper to the punch station.

Test I/O and Branch Instructions (TIOB)

Function	Op Code	DA	FS
Test Punch Busy	9A	3	2
Test Punch Error	9A	3	3
Test Feed Error	9A	3	5

Test Punch Busy: The Punch Busy indicator is tested. If this condition exists, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address.

Test Punch Error: The Punch Check indicator is tested. If this indicator is on, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address. The Punch Check indicator is reset by the branch test.

Test Feed Error: The Feed Check indicator is tested. If this indicator is on, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address.

If a feed cycle is in progress when this instruction is encountered in the program, the CPU is interlocked until the cycle is completed, at which time the test is performed.

Condition Code

The condition code is set to 00, 01, or 11 at the time the execution of an XIO instruction is completed to indicate that the 1442 Card Punch is available, working, or not operational.

The data transfer as specified in an XIO instruction for the 1442 is initiated only when the 1442 is in the available state.

The 1442 is available when the Ready indicator is on, the Punch Check indicator is not on, and the data transfer portion of a 2560 MFCM punch or punch and feed operation is not in progress.

The 1442 is working or busy during the execution of a previous 1442 punch operation or during the data transfer portion of a 2560 MFCM punch or punch and feed operation.

The 1442 is not operational when the Ready indicator is off or when the Punch Check or Feed Check indicators are on.

Control I/O Instructions (CIO)

A Control I/O instruction issued to the 1442 results in a no-operation.

IBM 2501 CARD READER, MODELS A1 and A2

Introduction

The 2501 Card Reader consists of one hopper, a serial read station, and one stacker.

The 2501 Card Reader, Model A1 has a maximum rate of 600 cards per minute, and the 2501 Card Reader, Model A2 has a maximum rate of 1,000 cards per minute.

2501 Card Reader Instructions

Transfer Instructions (XIO)

Function	Op Code	DA	FS
Read Card	D0	1	2

The direct or effective address (derived from the B1-D1 fields of the instruction) specifies the left-most main-storage location of the field where the input data will be located. The length of the input field is derived from the B2-D2 fields of the instruction.

The field length specification is restricted to binary values equal to or less than 80.

Test I/O and Branch Instructions (TIOB)

Function	Op Code	DA	FS
Test Reader Busy	9A	1	0
Test Reader Error	9A	1	1
Test Last Card	9A	1	4

Test Reader Busy: The Reader Busy indicator is tested. If this condition exists, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address.

Test Reader Error: The Read Check indicator is tested. If this indicator is on, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address. The Read Check indicator is reset by the branch test.

Test Last Card: The Last Card condition is tested. If this condition exists, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address. The Last Card condition is reset by the branch test.

Control I/O Instructions (CIO)

A control instruction which specifies the 2501 is treated as a no-operation.

Condition Code

The condition code is set 00, 01, or 11 when the execution of an XIO instruction is initiated. At this time the status of the respective I/O device is checked and the result of the check determines the setting of the condition code; 00 indicates available status, 01 indicates working status, and 11 indicates a not operational status.

A data transfer specified by an XIO instruction for the 2501 Card Reader is initiated only when the 2501 is in the available state. The 2501 is in the available state when the ready indicator is on, the read check indicator is not on, and a previously initiated Read Card instruction is not in progress.

The 2501 is working (condition code 01) during the execution of a previously initiated Read Card XIO instruction. It cannot accept a new instruction until the previous instruction has been executed and the 2501 has been returned to the available state (condition code 00). The 2501 is considered to be in the working state during the data transfer portion of a Card Read instruction on the 2560 MFCM or the 2520 Card Read Punch.

The 2501 is not operational when the ready indicator is off, or when the feed check or read check indicators are on.

IBM 2520 CARD READ PUNCH and CARD PUNCH

Introduction

The 2520 Card Read Punch, Model A1 reads cards serially at a maximum speed of 500 cards per minute and punches parallel at the same rate. Reading and punching may be overlapped to provide reading, computing, and punching at the maximum throughput speed. Reading without punching and punching without reading are also possible with the 2520-A1. All 2520s have two stackers. The 2520 Card Punch, Models A2 and A3 consists of the same basic mechanical unit as the 2520-A1, but have no read unit. Maximum punching rates are 500 cards per minute, or 300 cards per minute, depending on the model.

2520 Card Read Punch, Model A1 — 500 cpm read/punch

2520 Card Punch, Model A2	500 cpm punch
2520 Card Punch, Model A3	300 cpm punch

2520 Card Read Punch Instructions

Transfer Instructions (XIO)

Function	Op Code	DA	FS
Read Card	D0	2	2
Punch Card	D0	2	4
Punch and Feed	D0	2	6

Read Card: The direct or effective address, derived from the B1-D1 fields of the instruction, specifies the leftmost core storage location of the field where the input data will be stored. The length of the input field is derived from the B2-D2 fields of the instruction.

The field length specification is restricted to binary values equal to or less than 80.

The data transfer begins with the data read from column 1 of the card and continues until the specified number of bytes have been transferred from the reader to main storage.

When the input-field length is larger than the available space in main storage, the data transfer ends when the highest available storage position has been reached. No data error occurs when data is "left over."

Punch Card or Punch and Feed: The direct or effective address, derived from the B1-D1 fields of the instruction, specifies the leftmost byte of the output data field in the main storage. The length of the output field is derived from the B2-D2 fields of the instruction.

When the input-field length is larger than the available space in main storage, the data transfer ends when the highest available storage position has been reached. No data error occurs when data is "left over."

The field length specification is restricted to binary values equal to or less than 80.

The Card Read Punch has a parallel punch unit. The data transfer consists of a total of 13 scans of the output field, during which the data is not only transferred to the punch unit, but is also compared with echo data to ensure correct punching.

Upon completion of the Punch Card or Punch and Feed instruction, the card which was punched is ejected to the stacker. For the Punch Card instruction, the card at the read station does not advance to the punch station. For the Punch and Feed instruction, however, the card at the read station advances to the punch station without being read, and the next card is fed from the hopper to the read station.

When a Punch Card or a Punch and Feed instruction, which is preceded by a Punch Card instruction, is encountered in the program, the card at the read station advances to the punch station without being read, and the next card is fed from the hopper to the read station before punching begins.

In order to perform simultaneous reading and punching operations on the Card Read Punch, the Punch Card instruction must occur first in sequence in the program.

Test I/O and Branch Instructions (TIOB)

Function	Op Code	DA	FS
Test Reader Busy	9A	2	0
Test Reader Error	9A	2	1
Test Punch Busy	9A	2	2
Test Punch Error	9A	2	3
Test Last Card	9A	2	4
Test Feed Error	9A	2	5

Test Reader Busy: The Reader Busy condition is tested. If this condition exists, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address.

Test Reader Error: The Read Check indicator is tested. If this indicator is on, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address. The Read Check indicator is reset by the branch test.

If a read error occurs while a Read instruction is in progress, the Read Error and the Feed Error indicators are both turned on.

Test Punch Busy: The Punch Busy condition is tested. If this condition exists, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address.

Test Punch Error: The Punch Check indicator is tested. If this indicator is on, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address. The Punch Check indicator is reset by the branch test.

A card which is punched in error is automatically directed to stacker pocket 2.

Test Last Card: The Last Card condition is tested. If this condition exists, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address. The Last Card condition is reset by the branch test. When the Last Card indicator is set, the ready status is lost and an interrupt is requested. This action occurs in two cases:

1. The Last Card condition is set when a Read instruction is issued while a card is registered in the prepunch station and the preread station is empty.
2. The Last Card condition is set when a Read instruction is issued while the preread and prepunch stations are empty.

Test Feed Error: The Feed Check indicator is tested. If this indicator is on, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address.

If a feed cycle is in progress when this instruction is encountered in the program, the CPU is interlocked until the cycle is completed, at which time the test is performed.

Error conditions which can occur in the 2520 are read check, punch check, feed check, or machine check. These conditions are indicated individually on the 2520. The feed check and the machine check conditions turn off the Ready indicator.

The read check or punch check conditions can be reset by the I/O Check Reset key or the Load key on the CPU console or by Test I/O and Branch instructions in the program. The feed check and the machine check condition can be reset only by the Non-Process Runout (NPRO) key on the 2520 after the cards have been removed from the hopper. (A machine check may also require Customer Engineer action.)

The Card I/O No. 2 indicator on the CPU console is turned on when the read check, punch check, feed check or machine check conditions exist on the 2520 or when a Read Card, Punch Card, or Punch and Feed instruction is encountered in the program and the Ready indicator is not on.

NOTE: The feed check condition is set, together with the Attention indicator, when the cover is opened during a 2520 XIO operation or during a card run-in or NPRO cycle. Both conditions can be reset by closing the cover and operating the NPRO key.

Control I/O Instructions (CIO)

Function	Op Code	DA	FS
Stacker Select	9B	2	0

Stacker pocket 2 may be selected for the card in the punch station with this instruction. Stacker pocket 1 is the normal pocket, for which a Stacker Select instruction is not required. The proper location in the program sequence for the Stacker Select instruction is preceding the Read, Punch, or Punch and Feed instruction which causes the card in the punch station to be ejected to the stacker.

The direct or effective detailed specification (derived from the B1-D1 fields of the Stacker Select instruction) is inserted in the stacker control circuits. Only the low-order two bits are involved; the remaining high-order bits are ignored.

Bits		
30	31	Pocket Selected
0	1	1
1	0	2

A stacker select instruction in which bits 30 and 31 are both zero is treated as a no-operation.

Condition Code

The condition code is set to 00, 01, or 11 at the time the execution of a 2520 XIO instruction is completed to indicate that the 2520 is in the available, working, or not operational state.

The I/O operation and the data transfer as specified in a 2520 XIO instruction is initiated only when the 2520 is in the available state.

Available: The 2520 is available for a Read Card XIO instruction when:

1. The Ready indicator is on.
2. The Read Check and Punch Check Indicators are not on.
3. A previous 2520 Read or Punch and Feed instruction is not in progress.
4. The data transfer portion of a 2501 Read instruction is not in progress.

The 2520 is available for a Punch or Punch and Feed XIO instruction when:

1. The Ready indicator is on.
2. The Read Check and Punch Check indicators are not on.
3. A previous 2520 operation is not in progress.

Condition Code

The condition code is set to 00, 01, or 11 at the time the execution of a 2520 Card Punch XIO instruction is completed to indicate that the 2520 is in the available, working, or not operational state.

The I/O operation and the data transfer as specified in a 2520 XIO instruction is initiated only when the 2520 is in the available state.

Available: The 2520 is available for a Punch or Punch and Feed XIO instruction when:

1. The Ready indicator is on.
2. Punch Check indicator is not on.
3. A previous 2520 operation is not in progress.

Working: The 2520 is working or busy when a Punch, or Punch and Feed instruction for the 2520 is encountered in the program if a previous 2520 operation is in progress.

Not Operational: The 2520 is not operational when the Ready indicator is off or when the Punch Check or Feed Check indicators are on.

Working: The 2520 is working or busy when a Read Card XIO instruction for the 2520 is encountered in the program if:

1. A previous 2520 Read or Punch and Feed instruction is in progress.
2. The data transfer portion of a 2501 Read instruction is in progress.

The 2520 is working or busy when a Punch or Punch and Feed instruction for the 2520 is encountered in the program if a previous 2520 operation is in progress.

Not Operational: The 2520 is not operational when the Ready indicator is off or when the Read Check, Feed Check, or Punch Check indicators are on.

2520 Card Punch Instructions (2520-A2 and A3)

Transfer Instructions (XIO)

Function	Op Code	DA	FS
Punch and Feed	D9	2	6

The direct or effective address (derived from the B1-D1 fields of the instruction) specifies the leftmost byte of the output data field in main storage. The length of the output field is derived from the B2-D2 fields of the instruction.

The field length specification is restricted to binary values equal to or less than 80.

The Card Punch has a parallel punch unit. The data transfer consists of a total of 13 scans of the output field, during which the data is not only transferred to the punch unit but is also compared with echo data to ensure correct punching.

Upon completion of a punch card operation, the card which was punched is ejected to the stacker and the next card is fed from the hopper to the punch station.

When the input field length is larger than the available space in main storage, the data transfer ends when the highest available storage position has been reached. No data error occurs when data is "left over."

Test I/O and Branch Instructions (TIOB)

Function	Op Code	DA	FS
Test Punch Busy	9A	2	2
Test Punch Error	9A	2	3
Test Feed Error	9A	2	5

Test Punch Busy: The punch busy condition is tested. If this condition exists, the updated instruction address is replaced by the branch address: otherwise, normal instruction sequencing proceeds with the updated instruction address.

Test Punch Error: The Punch Check indicator is tested. If this indicator is on, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address. The Punch Check indicator is reset by the branch test. A card which is punched in error is automatically directed to stacker pocket 2.

Test Feed Error: The Feed Check indicator is tested. If this indicator is on, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address.

If a feed cycle is in progress when this instruction is encountered in the program, the CPU is interlocked until the cycle is completed, at which time the test is performed.

Control I/O Instructions (CIO)

Function	Op Code	DA	FS
Stacker Select	9B	2	0

Stacker pocket 2 may be selected for the card in the punch station with this instruction. Stacker pocket 1 is the normal pocket, for which a Stacker Select instruction is not required. The proper location in the program sequence for the Stacker Select instruction is preceding the Punch and Feed instruction. This causes the card in the punch station to be ejected to the selected stacker.

The direct or effective detail specification (derived from the B1-D1 fields of the Stacker Select instruction) is inserted in the stacker control circuits. Only the two low-order bits are involved; the remaining high-order bits are ignored.

Bits		
30	31	Pockets Selected
0	1	1
1	0	2

A stacker select instruction in which bits 30 and 31 are both zero is treated as a no-operation.

IBM 2560 MULTI-FUNCTION CARD MACHINE

Introduction

The 2560 provides full card-file maintenance abilities as well as an optional six line card document printing feature. Cards are fed from either of two hoppers through a serial read station, a serial punch station, and a serial print station after which they may be directed to any one of five stackers. The reading speed is 500 cards per minute, punching speed is 160 columns per second, and card printing speed is 140 characters per second.

Unit record functions such as Reproduce, Gang Punch, Summary Punch, Collate and Decollate may all be performed on the 2560. The optional printing feature may consist of two, four, or six print heads which may be positioned by the operator to print on any of the 25 lines of a card. Up to 64 characters may be printed on each line.

2560 Multi-Function Card Machine (MFCM) Instructions

Transfer Instructions (XIO)

Function	Op Code	DA	FS
Read Primary Card	D0	2	2
Read Secondary Card	D0	2	3
Punch Primary Card	D0	2	4
Punch Secondary Card	D0	2	5
Punch & Feed Primary Card	D0	2	6
Punch & Feed Secondary Card	D0	2	7
Write Card	D0	2	0

Read Card: The direct or effective address (derived from the B1-D1 fields of the instruction) specifies the leftmost main-storage location of the field where the input data will be located. The length of the input field is derived from the B2-D2 fields of the instruction.

The field length specification is restricted to binary values equal to or less than 80 .

The data transfer begins with the data read from column 1 of the card and continues until the specified number of bytes have been transferred from the reader to main storage.

Punch Card or Punch and Feed: The direct or effective address (derived from the B1-D1 fields of the instruction) defines the leftmost main-storage location of the output data. The length of the output field is derived from the B2-D2 fields of the instruction.

The field length specification is restricted to binary values equal to or less than 80.

If the input field is greater than the space available in main storage, the data transfer ends when the highest available storage position has been reached. No data error occurs when data is "left over."

A punch operation always begins at column 1 of the card from the specified feed, and continues until the specified number of columns have been punched. The number of columns punched corresponds to the number of bytes transferred from main storage.

Upon completion of a Punch and Feed instruction, all cards in the specified feed advance one station. The card which advances through the read station is not read.

Write Card: The optional printing feature may consist of two, four, or six print heads which may be positioned individually by the operator to print on any of the 25 lines of a card. Up to 64 characters may be printed on each line.

The output data which is to be printed on a card is located in adjacent 64 byte blocks of main storage. The number of adjacent 64 byte blocks corresponds to the number of 1s in the detailed specification of the print head select control instruction.

For the instruction which specifies card printing, the direct or effective address derived from the B1-D1 fields defines the leftmost main-storage location of the first 64 byte block of the output data. The first block is printed on the first print head selected, the second block on the next sequential print head selected, etc. The length of the block containing the greatest number of bytes is derived from the B2-D2 fields of the instruction. Each block or line which is shorter than the longest block must contain sufficient blank bytes to the right of the last character to be printed within the block to extend the block to the length of the longest block.

The field length specification in the write card instruction is restricted to binary values less than 65.

Test I/O and Branch Instructions (TIOB)

Function	Op Code	DA	FS
Test Reader/Punch Busy	9A	2	0
Test Reader/Punch Error	9A	2	1
Test Card Printer Busy	9A	2	2
Test Last Card	9A	2	4
Test Feed Error	9A	2	5

Test Reader/Punch Busy: The reader or punch busy condition is tested. If this condition exists, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address.

Test Reader/Punch Error: The Read Check and the Punch Check indicators are tested. If either indicator is on, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address. Both the Read Check and the Punch Check indicators are reset by the branch test. If a feed error occurs during a Read instruction, the Read Check and the Feed Check indicators are both turned on.

Test Last Card: The last card condition is tested. If this condition exists, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address. The last card condition is reset by the branch test.

Test Card Printer Busy: The card printer busy condition is tested. If this condition exists, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address.

Test Feed Error: The Feed Check indicator is tested. If this indicator is on, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address.

If a feed cycle or an eject cycle is in progress when this instruction is encountered in the program, the CPU is interlocked until the cycle is completed, at which time the test is performed.

The contents of the 2560 MFCM stacker registers are transferred to main-storage locations 152 through 154 when this instruction is encountered in the program to facilitate program restart procedures.

Control I/O Instructions (CIO)

Function	Op Code	DA	FS
Primary Card Stacker Select	9B	2	0
Secondary Card Stacker Select	9B	2	1
Punch Card Stacker Select	9B	2	2
Print Head Select	9B	2	3

Stacker Selection: There are five stackers on the MFCM. The Stacker Select instructions provide the means for directing cards from the primary feed, secondary feed, and punch station to any of the five stackers. Stacker 1 is the normal pocket for cards in the primary feed, and stacker 5 is the normal pocket for cards in the secondary feed. Stacker Select instructions are required only when it is desired to direct cards to pockets other than normal.

The MFCM stacker controls contain three program addressable stacker registers: the primary feed stacker register, the secondary feed stacker register, and the punch feed stacker register. By us of these registers the destination of a card can be assigned between the time the card has passed throug the read station and the time it leaves the print statio

The direct or effective detailed specificatior (derived from the B1-D1 fields of the Stacker Selec instruction) is inserted in the stacker register specified by the function specification field of the instruction. Only the low-order three bits of the detailed specification are involved; they are the following:

Bits			
29	30	31	Stacker Selected
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	1
1	1	1	1

A stacker select instruction in which bits 29, 30, and 31 are all zero is treated as a no-operation.

Programming Notes

The proper location in the program sequence to speci fy a stacker pocket other than normal is after the Read instruction for that card, if any, but before the next Read, Punch, and Punch and Feed instruction

which specifies the same feed. The Stacker Select instruction specifies the destination of a card while the card is in the primary feed, the secondary feed, or the punch station.

The stacker pocket destination for a card from either the primary or secondary feed may be changed by a Punch Card Stacker Select instruction while that card is in the punch unit or requested at the print station.

Print Head Selection: Any one or any combination of the print heads installed may be selected for a write card operation. This selection is made by a Print Head Select instruction, which must precede the Write Card instruction in the program sequence. If the same combination of lines is to be printed throughout the program, the control instruction must appear only once, before the first Write Card instruction.

The low-order six bits of the detailed specification in the Print Head Select instruction indicate which print heads are selected for a subsequent write card operation as shown below:

Bit Number	26	27	28	29	30	31
Print Head	1	2	3	4	5	6

When a bit corresponding to a print head is 1, the head is selected; when the bit is 0, the head is not selected.

At least one print head must be selected, otherwise the next card print operation results in a programming error stop condition.

Condition Code

The condition code is set to 00, 01, or 11 at the time the execution of a 2560 XIO instruction is completed to indicate that the 2560 is in the available, working, or not operational state.

The I/O operation and data transfer, as specified in a 2560 XIO instruction, is initiated only when the 2560 is in the available state.

Available: The 2560 is available for a Read Card XIO instruction when:

1. The Ready indicator for the specified feed is on.
2. The Read Check and Punch Check indicators are not on.
3. A previous 2560 operation is not in progress.
4. The data transfer portion of a 2501 read card operation is not in progress.

The 2560 is available for a Punch or Punch and Feed XIO instruction when:

1. The Ready indicator for the specified feed is on.
2. The Read Check and Punch Check indicators are not on.
3. A previous 2560 read, punch, or punch and feed operation is not in progress.
4. The data transfer portion of a 1442 punch operation is not in progress.
5. A card is either in the pre-punch or pre-read station of the specified feed.

The 2560 is available for a Write Card XIO instruction when:

1. The Ready indicator for either feed is on.
2. The Read Check and Punch Check indicators are not on.
3. A previous 2560 operation is not in progress.
4. A card is located in the punch or print station.

Working: The 2560 is working or busy when a Read Card XIO instruction for the 2560 is encountered in the program if:

1. A previously issued 2560 operation is in progress.
2. The data transfer portion of a 2501 read card operation is in progress.

The 2560 is working or busy when a Punch or Punch and Feed XIO instruction for the 2560 is encountered in the program if:

1. A previously issued 2560 read, punch, or punch and feed operation is in progress.
2. The data transfer portion of a 1442 punch operation is in progress.

The 2560 is working or busy when a Write Card XIO instruction for the 2560 is encountered in the program if a previously issued 2560 operation is in progress.

Not Operational: The 2560 is not operational for a Read, Punch, or Punch and Feed XIO instruction when Ready indicator for the specified feed is not on or when the Read Check, Punch Check, or Feed Check indicators are on.

The 2560 is not operational for a Write Card XIO instruction when the Ready indicators for both feeds are off, when the Read Check, Punch Check, or Feed Check indicators are on.

IBM 2203 PRINTER

Introduction

The 2203 Printer provides output for the System/360 Model 20 at up to 750 lines per minute. Interchangeable typebars allow the operator to select a type style and character set for a specific printing job. Four character sets are available for the 2203 Printer. The 13-character set has 10 numeric and 3 special characters; the character sets with 39, 52, and 62 characters have 26 alphabetic, 10 numeric, and 3, 16, and 26 special characters, respectively.

The printing speed for any one application depends on the total number of lines printed; the amount of processing required for each printed line; and the character set used.

The complete range of speeds available with the IBM 2203 Printer is shown in the table below.

Character Set	lpm	Cycle Time (ms)
13	750	80
39	425	141
52	350	171
62	300	200

A 120-character line, at 10 characters to the inch, is standard. An additional 24 positions are available as a special feature. Vertical spacing of six or eight lines per inch can be manually selected by the operator. Single, double, and triple spacing of lines, plus skipping to a predetermined point, are performed by the tape-controlled carriage, directed by the CPU. The sequence and arrangement of data printed are also controlled by the stored program; a line to be printed is assembled in core storage in exactly the same sequence it is to appear as output.

The Dual-Feed Carriage special feature permits independent and simultaneous control of two sets of forms.

2203 Printer Instructions

Transfer Instructions (XIO)

Function	Op Code	DA	FS
Print	D0	4	0
Print & Space Suppress	D0	4	1

The direct or effective address (derived from the B1-D1 fields of the instruction) specifies the leftmost byte of the output data field in main storage. The length of the output field is derived from the B2-D2 fields of the instruction.

The field length specification is limited to binary values equal to or less than 144 for the 2203 Printer.

At the completion of the Print instruction, the carriage performs an automatic single space unless otherwise directed by the program. The automatic single space does not occur following a Print and Space Suppress operation.

Test I/O and Branch Instructions (TIOB)

Function	Op Code	DA	FS
Test Printer Busy	9A	4	0
Test Printer Error	9A	4	1
Test Channel 9	9A	4	2
Test Channel 12	9A	4	3
Test Carriage Busy	9A	4	6

Test Printer Busy: The printer busy condition is tested. If this condition exists, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address.

Test Printer Error: The Print Check indicator is tested. If this indicator is on, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with updated instruction address.

Test Channel 9: The carriage channel 9 condition is tested. If this condition exists, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address. The carriage channel 9 condition is reset by the branch test, or is reset when the carriage moves to or beyond channel 1.

Test Channel 12: The carriage channel 12 condition is tested. If this condition exists, the updated instruction address is replaced by the branch address; otherwise normal instruction sequencing proceeds with the updated instruction address. The carriage channel 12 condition is reset by the branch test, or is reset when the carriage moves to or beyond channel 1.

If a print operation which includes carriage motion after printing is in progress when either the Test Channel 9 or the Test Channel 12 instructions are encountered in the program sequence, the CPU is interlocked until the completion of the print operation; at this time the test is performed and the program continues.

Test Carriage Busy: The carriage busy condition is tested. If this condition exists, the updated instruction address is replaced by the branch address; otherwise normal instruction sequencing proceeds with the updated instruction address.

Control I/O Instruction (CIO)

Function	Op Code	DA	FS
Control Carriage, Immediate Space	9B	4	4
Control Carriage, Immediate Skip	9B	4	5
Control Carriage, Delayed Space	9B	4	6
Control Carriage, Delayed Skip	9B	4	7

A control carriage instruction in which bits 28, 29, 30, and 31 are all zero is treated as a no-operation.

The direct or effective detailed specification, derived from the B1-D1 fields of the Control Carriage instruction, indicates the particular line or carriage channel to which the carriage is to advance. Only the lowest order four bits of the detailed specification (bits 28-31) are required; the remaining higher order bits are ignored. Carriage channel selection is as follows:

Bits				
28	29	30	31	Specification
0	0	0	1	Single Space or Channel 1
0	0	1	0	Double Space or Channel 2
0	0	1	1	Triple Space or Channel 3
0	1	0	0	Channel 4
0	1	0	1	Channel 5
0	1	1	0	Channel 6
0	1	1	1	Channel 7
1	0	0	0	Channel 8
1	0	0	1	Channel 9
1	0	1	0	Channel 10
1	0	1	1	Channel 11
1	1	0	0	Channel 12

NOTE: After a skip operation (for example, a skip to channel 1), the form is stopped on the particular line to which it was to advance (for example, line 77). If the control tape contains a punch on line 78 in some other channel (for example, channel 2), the programmer can move the form to this next line by issuing a single-space instruction. However, if a Skip to Channel 2 instruction is issued instead, the skip operation is automatically altered into a single-space instruction and the form advances only to the next line.

Dual-Feed Carriage

A dual-feed carriage is available as a special feature for the 2203 Printer. The function specification in the Control Carriage instruction is expanded to permit the upper and lower carriage feeds to be controlled independently or as a single feed, as follows:

Function Specification		Function	Feed
4	(0 1 0 0)	Immediate Space	Lower
5	(0 1 0 1)	Immediate Skip	Lower
6	(0 1 1 0)	Delayed Space	Lower
7	(0 1 1 1)	Delayed Skip	Lower
8	(1 0 0 0)	Immediate Space	Upper
9	(1 0 0 1)	Immediate Skip	Upper
A	(1 0 1 0)	Delayed Space	Upper
B	(1 0 1 1)	Delayed Skip	Upper
C	(1 1 0 0)	Immediate Space	Both
D	(1 1 0 1)	Immediate Skip	Both
E	(1 1 1 0)	Delayed Space	Both
F	(1 1 1 1)	Delayed Skip	Both

The format of the detailed specification (derived from the B1-D1 fields of the Control Carriage instruction) for the dual-feed carriage has six carriage channels. These six channels are numbered 1, 2, 3, 4, 9, and 12; only detailed specifications of corresponding binary values are valid for the upper carriage.

A delayed carriage command for either feed (or both) may be cancelled and replaced with another carriage command before the next Print instruction is encountered in the program.

A Print instruction on a 2203 Printer with dual-feed carriage is followed by an automatic single space on either or both carriages in the absence of delayed Carriage Control instructions for the respective carriages.

This automatic single space does not occur on either carriage following a Print and Space Suppress instruction. The Print and Space Suppress instruction does not cancel a previously issued delayed Control Carriage instruction for either carriage.

The testable Carriage Channel 9 and Carriage Channel 12 indicators are completely independent for each carriage. The function specification of the Test I/O and Branch instruction for the 2203 Printer is expanded when the dual-feed carriage is installed to permit testing of these indicators for the upper carriage as well as for the lower carriage. The function specification for the lower carriage of the dual-feed carriage is the same as for a single-feed carriage.

Function Specification		Condition Tested	Carriage
2	(0 0 1 0)	Channel 9	Lower
3	(0 0 1 1)	Channel 12	Lower
4	(0 1 0 0)	Channel 9	Upper
5	(0 1 0 1)	Channel 12	Upper

An "Upper-Lower " Carriage Select switch is provided with the dual-feed carriage to select the carriage to which the Carriage Space and Carriage Restore functions apply when the respective key is operated.

The Carriage Stop key is effective for either carriage at all times.

The Forms Check, End of Forms, and Carriage Interlock indicators are common to both carriages.

Condition Code

XIO Instruction: The condition code is set to 00, 01, or 11 at the time the execution of an XIO instruction for the printer is completed to indicate that the printer is in the available, working, or not operational state.

The I/O operation and data transfer as specified in an XIO instruction for the printer is initiated only when the printer is in the available state.

The printer is available when the Ready indicator is on and a previous print operation, including carriage motion, is not in progress.

The printer is working or busy during the execution of a previous print operation, including carriage motion after printing.

The printer is not operational when the Ready indicator is not on. The Ready indicator is off when the carriage control tape is not installed. If a Print instruction or Control Carriage instruction is issued when the control tape is missing, the condition code is set to 11 (not operational) and the program continues with the next sequential instruction.

On a printer that is equipped with the dual-feed carriage, both carriage control tapes must be installed even if only one feed is used.

CIO Instruction: The condition code is set to 00, 01, or 11 at the time the execution of a Control Carriage instruction is completed to indicate that the carriage is in the available, working, or not operational state.

The carriage operation specified is initiated only when the carriage is in the available state.

The carriage is available when the printer Ready indicator is on if a previous print operation (which includes carriage motion after printing) or a previous carriage operation is not in progress.

The carriage is working or busy during the execution of a previous print operation (which includes carriage motion after printing) or during the execution of a previous carriage operation.

The carriage is not operational when the printer Ready indicator is not on. The Ready indicator is off when the carriage control tape is not installed. If a Print instruction or Control Carriage instruction is issued when the control tape is missing, the condition code is set to 11 (not operational) and the program continues with the next sequential instruction.

On a printer that is equipped with the dual-feed carriage, both carriage control tapes must be installed even if only one feed is used.

IBM 1403 PRINTER, MODELS 2, 7, AND N1

Introduction

The IBM 1403 Printer provides output for the System/360 Model 20 at a rate of 600 lines per minute for the 1403-2 and 1403-7, and 1100 lines per minute for the 1403-N1. If the 1403-N1 is equipped with Universal Character Set (UCS) special feature, the print speed is 1400 lines per minute. If the 1403-2 is equipped with UCS, the print speed is 750 lines per minute.

The 1403-2 and 1403-N1 have a print line width of 132 characters and the 1403-7 has a print line width of 120 characters. Vertical spacing of six or eight lines to the inch can be manually selected by the operator. Single, double, and triple spacing of lines, plus skipping to a predetermined point are performed by the tape-controlled carriage, under control of the CPU stored program. The 1403-2 has a dual-speed carriage that permits high-speed skipping at approximately 75 inches per second on skips over eight lines.

Each print position can print 48 different characters; however, with the UCS special feature, each print position can print up to 240 characters. The printing format is controlled by the stored program. The 1403-2 and 1403-7 have the characters assembled in a chain; the 1403-N1 uses the IBM 1416 Interchangeable Train Cartridge. As the chain (or train) travels in a horizontal plane, each character is printed as it is positioned opposite a magnet-driven hammer that presses the form against the chain (or train).

As each character is printed, checking circuits are set up to ensure that the character printed is correct. Checks are also made to ensure that overprinting does not occur. If an error is detected, the machine stops and the associated check light turns on.

Universal Character Set (1403-2 and -N1)

The UCS special feature allows the printing of any set of graphics (up to 240 different characters) by a 1403-2 or N1 Printer attached to the IBM System/360 Model 20. The graphics can be arranged in any desired sequence on the print chain (1403-2) or print train (1403-N1).

Selective Tape Listing

The Selective Tape Listing special feature allows simultaneous printing on either eight narrow (1.5" width) or four wide (3.1" width) paper tape rolls or folding forms. The 1403-2 and -7 use paper tape rolls and the 1403-N1 uses folding forms. Each tape is controlled individually, one space at a time; spacing occurs after a line has been printed. The operation of this feature is controlled by a switch on the printer. For detailed descriptions of the various printer models, operating procedures, optional features as well as information on character sets, refer to IBM 1403 Component Description (Form A24-3073).

1403 Printer Instructions

Transfer Instructions (XIO)

Function	Op Code	DA	FS
Print	D0	4	0
Print & Space Suppress	D0	4	1
Load Chain Buffer and Disable Folding	D0	4	2
Load Chain Buffer and Enable Folding	D0	4	3

The direct or effective address (derived from the B1-D1 fields of the instruction) specifies the leftmost byte of the output data field in main storage. The length of the output field is derived from the B2-D2 fields of the instruction.

The field length specification is limited to binary values equal to or less than 132 for the 1403-2 and N1, or 120 for the 1403-7.

At the completion of the Print instruction, the carriage performs an automatic single space unless otherwise directed by the program. The automatic single space does not occur following a Print and Space Suppress instruction.

Test I/O and Branch Instructions (TIOB)

Function	Op Code	DA	FS
Test Printer Busy	9A	4	0
Test Printer Error	9A	4	1
Test Channel 9	9A	4	2
Test Channel 12	9A	4	3
Test Carriage Busy	9A	4	6

Test Printer Busy: The printer busy condition is tested. If this condition exists, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address. The printer busy condition and the carriage busy condition (see "Test Carriage Busy") are of the same duration.

Test Printer Error: The Print Check indicator is tested. If this indicator is on, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address. With an IBM 1403 Printer attached to the system, the print check indicates mis-firing of hammers, or sync check.

Test Channel 9: The carriage channel 9 condition is tested. If this condition exists, the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address. The carriage channel 9 condition is reset by the branch test, and is reset when the carriage moves to or beyond channel 1.

Test Channel 12: The carriage channel 12 condition is tested. If this condition exists; the updated instruction address is replaced by the branch address; otherwise, normal instruction sequencing proceeds with the updated instruction address. The carriage channel 12 condition is reset by the branch test, and is reset when the carriage moves to or beyond channel 1.

If a print operation which includes carriage motion after printing is in progress when either the Test Channel 9 or the Test Channel 12 instructions are encountered in the program sequence, the CPU is interlocked until the completion of the print operation; at this time the test is performed and the program continues.

Test Carriage Busy: The carriage busy condition is tested. If this condition exists, the updated instruc-

tion address is replaced by the branch address; otherwise normal instruction sequencing proceeds with the updated instruction address. The carriage busy condition and the printer busy condition are of the same duration.

Control I/O Instruction (CIO)

Function	Op Code	DA	FS
Control Carriage, Immediate Space	9B	4	4
Control Carriage, Immediate Skip	9B	4	5
Control Carriage, Delayed Space	9B	4	6
Control Carriage, Delayed Skip	9B	4	7

A Control Carriage instruction in which bits 28, 29, 30, and 31 are all zero is treated as a no-operation.

The direct or effective detailed specification (derived from the B1-D1 fields of the Control Carriage instruction) indicates the particular line or carriage channel to which the carriage is to advance. Only the lowest-order four bits of the detailed specification (bits 28-31) are required; the remaining higher-order bits are ignored. Carriage channel selection is as follows:

Bits				
28	29	30	31	Specification
0	0	0	1	Single Space or Channel 1
0	0	1	0	Double Space or Channel 2
0	0	1	1	Triple Space or Channel 3
0	1	0	0	Channel 4
0	1	0	1	Channel 5
0	1	1	0	Channel 6
0	1	1	1	Channel 7
1	0	0	0	Channel 8
1	0	0	1	Channel 9
1	0	1	0	Channel 10
1	0	1	1	Channel 11
1	1	0	0	Channel 12

NOTE: After a skip operation (for example, a skip to channel 1), the form is stopped on the particular line to which it was to advance (for example, line 77). If the control tape contains a punch on line 78 in some other channel (for example, channel 2), the programmer can move the form to this next line by issuing a single-space instruction. However, if a Skip to Channel 2 instruction is issued instead, a regular skip operation to the next form is performed and the carriage is stopped on line 78 of this form. Therefore, if this skip operation is a skip to channel 9 or a skip to channel 12, then the channel 9 indicator (or the channel 12 indicator) is set when the carriage has arrived at channel 9 (or channel 12) of the next form.

Selective Tape Listing: When the switch for this feature is ON, any carriage control I/O instruction has the effect of a delayed single space, regardless of the function specification setting. The function specification, derived from the B1-D1 fields, controls the tapes in the following manner:

Bits	24	25	26	27	28	29	30	31
Tapes	8	7	6	5	4	3	2	1

For example, if bit 24 is a 1 bit, tape 8 is advanced for one space after printing. The wide tape (3.1" width) covers the positions of two narrow tapes requiring that both positions be set to 1 bits to space the double width tape properly. If more than one Control Carriage instruction is interpreted before a Print instruction, only the last one is executed.

Condition Code

XIO Instruction: The condition code is set to 00, 01, or 11 at the time the execution of an XIO instruction for the printer is completed to indicate that the printer is in the available, working, or not operational state.

The I/O operation and data transfer as specified in an XIO instruction for the printer is initiated only when the printer is in the available state.

The printer is available when the Ready indicator is on and a previous print operation, including carriage motion, is not in progress.

The printer is working or busy during the execution of a previous print operation, including carriage motion after printing.

The printer is not operational when the Ready indicator is not on.

CIO Instruction: The condition code is set to 00, 01, or 11 at the time the execution of a Control Carriage instruction is completed to indicate that the carriage is in the available, working, or not operational state.

The carriage operation specified is initiated only when the carriage is in the available state.

The carriage is available when the printer Ready indicator is on if a previous print operation which includes carriage motion after printing, or a previous carriage operation is not in progress.

The carriage is working or busy during the execution of a previous print operation which includes carriage motion after printing, or during the execution of a previous carriage operation.

The carriage is not operational when the printer Ready indicator is not on, or when the carriage control tape is not inserted.

IBM 2415 MAGNETIC TAPE DRIVE AND CONTROL UNIT

INTRODUCTION

The IBM 2415 Magnetic Tape Drive and Control Unit is designed to meet the low-cost magnetic tape requirements of System/360. Six models of the IBM 2415 are available with the System/360 Model 20. The 2415-1, -2, and -3 use the Non-Return-to-Zero-IBM (NRZI) method of recording and the 2415-4, -5, and -6 use the Phase Encoding (PE) method. The IBM System/360 Model 20 operates with either NRZI or PE type tape drives through the Input/Output Channel (IOC).

The user can select from three different models of either NRZI or PE type tape drives. The three different models consist of modules containing 2, 4, or 6 tape drives that operate independently but share a common control unit. The IOC can operate one control unit.

Each tape drive can be addressed by the program, and has its own keys and indicator lights for manual control.

Table 9 shows the performance of the various models. The tape drives are normally equipped with 9-track read/write heads; however, 7-track heads can be installed. For example, a 2415-2 may be equipped with two 9-track heads and two 7-track heads.

Table 9. IBM 2415 Characteristics

	Model	Size	Density	Bytes/Sec	Tape Speed
NRZI (9-Track)	1	two tape drives	800 Bpi	15000	18.75 inch/sec
	2	four tape drives	800 Bpi	15000	18.75
	3	six tape drives	800 Bpi	15000	18.75
PE (9-Track)	4	two tape drives	1600 Bpi	30000	18.75
	5	four tape drives	1600 Bpi	30000	18.75
	6	six tape drives	1600 Bpi	30000	18.75
The 7-Track Compat. Feature for all Models allows densities of 200,556, and 800 Bpi NRZI					
The 9-Track Compat. Feature for Models 4,5,6 allows 800 Bpi NRZI Operation					

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The 7-track heads, however, require installation of the 7-track compatibility feature in the control unit of that model (For details, see Optional Features).

All models can read backwards, but the operation is only error-free when the tape that is read backwards, was written on an IBM 2415, 2401, 2402, 2403, or 2404 magnetic tape drive. Error detection is accomplished by immediate read-back after writing via the second gap of the read/write head. The PE-type tape units are equipped with the automatic "in flight" error correction for a single track. The automatic correction becomes effective during read operations when the error is in only one track. All errors (single or multiple track) are detected on all models and where automatic error correction is not possible, the "Input/Output Control System for Tapes" (an IBM designed program) uses a special recovery procedure.

Input/Output Channel (IOC)

The IOC is a device which allows the CPU to communicate with up to two tape control units. The IOC is connected to these control units via the IBM System/360 input/output channel-to-control-unit-interface. The arrangement provides considerable flexibility because programs can be designed according to standard procedures, independent of the actual I/O devices attached. The System/360 Model 20 channel operates in burst mode only. Although the channel uses CPU facilities during the transfer of data, the CPU is free for other processing during a rewind, rewind/unload, forward or backspace block, and forward or backspace file operation.

Control Unit

The control unit regulates the data transfer between the channel and the tape drives. It accepts the commands, decodes them, and transmits them to the respective tape drives. The control unit also transmits the status of a selected tape drive to the channel and it subsequently requests data. The program can then elect to send data or not, depending on the status of the device (unit status). However, all control commands are executed as soon as they are accepted by the control unit because they are "control immediate" type commands.

2415 INSTRUCTIONS

Channel Commands

The channel is programmed by means of modified transfer I/O instructions and one or more channel command words which are placed in main storage. The XIO instruction initiates all input/output operations on the devices attached to the channel while the Channel Command Word (CCW) specifies the exact operation that is to be performed.

Mode 1 Set commands set the addressed tape drives to 200, 556, or 800 bpi NRZI; at the same time, the commands set the drive to odd or even parity mode, data converter on or off, and translator on or off, depending on the setting of bits 2, 3, and 4 of the Mode 1 Set command. For example, if 200 bpi is specified, it is possible to set simultaneously odd parity, data converter off, and translator on by setting the bits 2, 3, and 4 of the command to 111 (Case H in the table).

Mode 1 Set

CCW Bits	0	1	2	3	4	5	6	7
Set 200 Bpi	0	0	-	-	-	0	1	1
Set 556 Bpi	0	1	-	-	-	0	1	1
Set 800 Bpi (Reset)	1	0	-	-	-	0	1	1

CCW Bits	2	3	4
Case A	0	0	0
B	0	0	1
C	0	1	0
D	0	1	1
E	1	0	0
F	1	0	1
G	1	1	0
H	1	1	1

Turn Off Translator	Turn On Translator	Turn Off Data Converter	Turn On Data Converter	Set Even Parity	Set Odd Parity	Set Density	Case	
							A	NOP 7 and 9 track (Reserved)
							B	Diagnostic Use (7 and 9 tr)
X			X		X	X	C	*(7-track only)
							D	Sense Status Reset (NOP)
X		X		X		X	E	(7-track only)
	X	X		X		X	F	(7-track only)
X		X			X	X	G	**(7-track only)
	X	X			X	X	H	(7-track only)

Note: 9-track operation overrides but does not reset 7-track mode setting.

All 9-track operations force odd parity. A Read Backward Command overrides a "Data Converter on" Mode Setting.

* Reset condition for control unit with 7-track and data conversion feature.

** Reset condition for control unit with 7-track but without data conversion feature.

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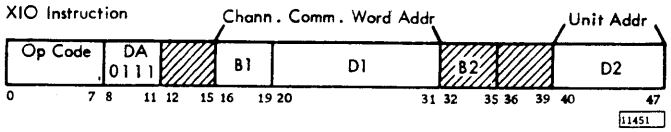
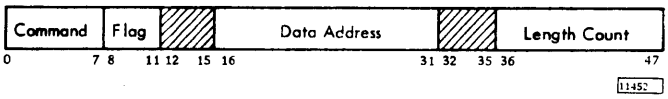
XIO Instruction



The op code (bits 0-7) specifies transfer I/O. The device address (bits 8-11) contains 0111 which identifies the input/output channel. The B1-D1 field specifies the main-storage address of a channel command word according to the rules for direct or effective addressing (indexing). The last portion of the D-field (bits 40-47) specifies the address of the control unit and/or device to which the instruction applies, according to the rules for direct or effective addressing (indexing). This address must not be zero. Bits 12-15 are always ignored. Bits 32-39 are ignored after direct or effective address generation.

The CCW has a dual function, it specifies the channel operation and the control unit operation that is to be performed.

Channel Command Word (CCW)



Bits 0-7 specify the desired channel or control unit operations. The bits 2, 3, and 4 represent the tape motion code in the control commands. The flag field is used for chaining. Bit 8 specifies that the following CCW is to be chained with this command. The data address specifies the address of the first (leftmost) byte of an input or output data field in the main storage while the length count specifies the true number of bytes which constitute this field. Bits 12-15 and 32-35 are ignored. The field length can vary from a minimum of 1 to a maximum of 4,095 bytes. The following table shows the channel commands for the IBM 2415 tape units.

Channel Commands	CCW Bits							
	0	1	2	3	4	5	6	7
Invalid	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	1	0
Read Backward	0	0	0	0	1	1	0	0
Write	0	0	0	0	0	0	0	1
Sense	0	0	0	0	0	1	0	0
Transfer in Channel	0	0	0	0	1	0	0	0

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During decoding, the channel checks only the four low order bits of the CCW. If all four bits are zero the command is invalid. (See Channel Units Command.) When the control unit detects a control instruction, the instruction is further decoded because the bits 2, 3, and 4 specify the desired operation in detail.

Control Commands	CCW Bits							
	0	1	2	3	4	5	6	7
Rewind	0	0	0	0	0	1	1	1
Rewind/Unload	0	0	0	0	1	1	1	1
Erase Gap	0	0	0	1	0	1	1	1
Write Tape Mark	0	0	0	1	1	1	1	1
Backspace Block	0	0	1	0	0	1	1	1
Backspace File	0	0	1	0	1	1	1	1
Forwardspace Block	0	0	1	1	0	1	1	1
Forwardspace File	0	0	1	1	1	1	1	1

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In addition to the channel commands and the control commands, two groups of mode set commands are used to operate the 7-track and 9-track compatibility features. The Mode 1 Set commands can be used for all models of 2415 to set different reading and writing densities. The Mode 2 Set commands are used only for 2415-4, -5, or -6 units to set different recording densities. However, all mode set commands are effective only when the correct compatibility feature is installed in the control unit (see "Optional Features"). Mode set commands issued to units without the compatibility feature are treated as no-operation.

Mode 2 Set commands set the addressed tape drive to 800 bits per inch (bpi) NRZI or to 1600 bpi PE.

Mode 2 Set Commands	CCW Bits							
	0	1	2	3	4	5	6	7
Set 1600 bpi	1	1	0	0	0	0	1	1
Set 800 bpi	1	1	0	0	1	0	1	1

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Read

The Read command affects the tape unit specified in the XIO instruction that initiates the operation. Normally, the leftmost byte of the input area in main storage is specified in the CCW. However, in Read Backward commands, the rightmost byte of the input area must be specified, because the incoming data is stored in main storage in descending order.

The Read command causes the addressed tape unit to move the tape in the specified direction to the next interblock gap and stop. As the tape moves over the read head, data is read and sent to the channel. The data transfer begins with the first byte read and it continues until the specified number of bytes have been transferred or until the tape unit ends the operation, whichever occurs first. Programming Note: Read Backward operation requires de-skewed characters and therefore, only tapes that were written on an IBM 2415, 2401, 2402, 2403, or 2404 Tape Drive can be read backward successfully. The programmer should avoid read backward operations which violate protected storage. Data can be placed in protected storage, addresses 0-143, by a read backward operation without error indication, but attempts to recover the data in this area result in an error.

Write

The Write command affects the unit specified in the unit address field of the Transfer I/O instruction that initiated the Write command. The data address field of the command word always specifies the left-most byte of the output field in main storage. The operation begins with the first byte transferred to the I/O device and continues until the specified number of bytes has been transferred. To facilitate noise recognition, a minimum block of 18 bytes should be written. No minimum is required for the PE type tape units. Data is written on the tape in form of blocks. The blocks are separated by interblock gaps which are created as the tape is written. Blocks may consist of any number of bytes, limited only by the length count.

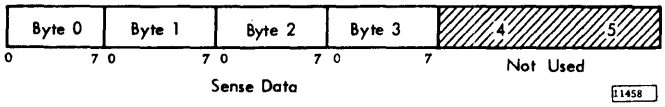
Control

The Control command affects the unit that is specified in the unit address field of the XIO instruction which initiated this command. The control unit decodes bits 0, 1, 2, 3, and 4 and starts the required action in the addressed tape drive. (See Control Commands.)

Sense

The Sense command is essentially a read operation. However, instead of reading data from a tape, status indicator bits are read and transferred to main storage. The data address field of the command word specifies the leftmost byte of the input field into which the indicator bits are to be stored.

The status bits represent detailed information about the last operation and the status of the selected device. The Sense command is used to obtain supplementary data after a unit check has occurred. This allows analysis of the conditions which caused the unit check. The Sense command can read in a total of 6 bytes or less as indicated by the length count. Two of those bytes are not used (all zero).



Command Chaining

The program initiates action in an I/O device by issuing an XIO instruction. The XIO reads out a CCW which specifies the operation to be performed. Upon completion of the operation, the activity can be continued on the same I/O device by automatically fetching the next CCW. This is called chaining. Chaining becomes effective when the chaining flag in the preceding CCW is turned on.

The channel executes chaining by adding six bytes to the main storage address of the previous CCW. Therefore, CCWs that are to be chained must be located in successive core-storage positions. All chained CCWs pertain to the I/O device specified in the initiating XIO instruction. In case of errors or other unusual conditions such as unit check, control unit end, or incorrect length, the chaining is stopped. To resume operations, a new XIO instruction must be issued.

Transfer in Channel (TIC)

This command can be used to skip from one chain of command words to another. The TIC command is an unconditional branch. The data address field of the CCW designates the main-storage location of another CCW. During the execution of Transfer in Channel (TIC), the new CCW is fetched from main storage. The TIC command is executed regardless of the status of the chaining flag, and the new CCW can be located anywhere in main storage outside the protected area (first 144 bytes). A data transfer between I/O devices and the channel does not occur during the TIC command.

Table 10. Sense Data Table

Sense Data Table

Byte zero (all Models)	Byte two (all Models)
Bits 0 = Command Reject 1 = Intervention Required 2 = Bus - Out Check 3 = Equipment Check 4 = Data Check 5 = Overrun 6 = Word Count Zero 7 = Data Converter Check (Unit Check)	Bits 0 = Not used 1 = Not used 2 = Not used 3 = Not used 4 = Not used 5 = Not used 6 = } Unconditionally 7 = } forced on
Byte one (Models 1,2,3)	**Byte one (Models 4,5,6)**
Bits 0 = Interblock Gap Noise 1 = Tape Unit Status A 2 = Tape Unit Status B 3 = 7-Track 4 = At Load Point → Unit check during all operations except rewind or rew/unload 5 = Write Status 6 = File Protect 7 = Not used	Bits 0 = Same (as for Models 1,2,3) 1 = Same 2 = Same 3 = Same 4 = Same 5 = Same 6 = Same 7 = Not Capable → Unit Check
Byte three (Models 1,2,3)	**Byte three (Models 4,5,6)**
Bits 0 = Data Register VRC 1 = LRCR - Error 2 = Skew Error 3 = Not used 4 = Read Register VRC (Data Check) 5 = Not used 6 = Backward Memory 7 = C-compare → Equipment Check	Bits 0 = Same (as for Models 1,2,3) 1 = Multiple Track Error/LRCR 2 = Same 3 = End Data Check 4 = Read Register VRC/Envelope Check (Data Check) 5 = 1600 Bpi 6 = Same 7 = Same → Equipment Check

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NOTE: The following restrictions must be observed: The first CCW designated by an XIO instruction must not specify transfer in channel, it must be some other command. The new CCW, which is obtained via a TIC cannot specify TIC again, this must also be some other command. When these restrictions are violated, a program check occurs.

Control Unit Commands

Rewind

Rewind causes the addressed tape drive to rewind to load point. The load point is a reflective marker attached to the tape at the beginning of the tape reel. Load point is sensed by a photo cell. When the load point is reached during a rewind operation, the device end signal is generated and maintained in the device until the signal is accepted by the channel.

Rewind and Unload

This command causes the selected tape drive to rewind the tape to load point and to unload the tape. When the tape is unloaded, the tape unit becomes "not ready" and device end, control unit end, and unit check are generated. Device end is generated again when a new tape is loaded.

Erase Gap

This command causes the selected tape unit to erase the tape for a distance corresponding to the load poin delay. The delay is 217 msec. Device end is generated when the operation is completed.

Backspace Block

This command moves tape in a backward direction to the next interblock gap or to the load point, whichever comes first. The tape unit remains in backward status until a forward command, such as write, is received. No data is transferred during this operation. Device end is generated when the operation is completed. If the load point is encountered, unit check is set.

Backspace File

This command moves the tape in a backward direction to the interblock gap beyond the next tape mark or to the load point, whichever comes first. No data is transferred and device end is generated when the operation is completed. This command does not cause unit exception but if the load point is encountered, unit check is set.

Forwardspace Block

This command moves the tape forward to the next interblock gap without transferring data. Device end is generated when the operation is completed. If the load point is encountered, unit check is set.

Forwardspace File

This command moves the tape forward to the interblock gap beyond the next tape mark or to the load point, whichever comes first. No data is transferred and device end is generated when the operation is completed. This command does not cause unit exception but if the load point is encountered, unit check is set.

NOTE: On all backward-type commands, the tape unit remains in the backward status until a command that requires forward status is received.

Write Tape Mark

This command writes a tape mark after the load point delay has timed out. Tape moves in a forward direction. The tape mark for phase encoding is a block of 40 characters with transitions in all tracks except 1, 3, and 4. For 9-track NRZI and 7-track operations,

the tape mark is a single character with its check character. Device end is generated when the operation is completed.

Mode 1 Set Commands

The Mode 1 Set commands are used to set a particular tape drive to 200, 556, or 800 bpi density for a 7-track tape; these density settings are valid for read and write operations. A particular density setting is retained until a new mode set command is issued. The density can be changed at any time, independent of the position of the tape. In addition to density setting, the data converter, the translator, and the parity can be set (see previous "Channel Commands"). When the mode set command is completed, channel end and device end is set.

The Mode 1 Set commands can be used for all models of 2415, provided that these units are equipped with the 7-track compatibility feature and one (or more) 7-track read/write heads. The compatibility feature is needed to read 7-track tape; the 2415-1, -2, and -3 units normally read 9-track tape at 800 bpi NRZI, and the 2415-4, -5, and -6 units normally read 9-track tape at 1600 bpi PE. When a 7-track tape is read on a 2415-1, -2, or -3 unit that is equipped with 9-track heads only, or when a 9-track tape is read on a 7-track head, a data check occurs (Table 11). When a Mode 1 Set command specifies data converter on, and the 7-track compatibility feature is installed without a data converter, command reject is set.

Mode 2 Set Commands

The Mode 2 Set commands are used for the 2415 models 4, 5, and 6 to change the recording density and method from 1600 bpi PE to 800 bpi NRZI or vice versa. However, the Mode 2 Set commands are only effective when the magnetic tape unit is equipped with the 9-track compatibility feature. If a 9-track tape (written at 800 bpi NRZI) is read on a 2415-4, -5, or -6 that has no 9-track compatibility feature, the not capable bit is set and unit check occurs; an attempt to read a 7-track tape on such a unit has the same effect (Table 11).

When a Mode 2 Set command is completed, channel end and device end is set. The density setting is retained until a new mode set command is given. However, a system or selective reset results in a recording density setting of 1600 bpi. The mode setting is effective only for write-type operations such as Write, Write Tape Mark, and Erase Gap commands. The mode setting can only be changed when the tape is at load point. The mode setting is transferred to the selected tape drive when the tape leaves from load point. The tape drive is automatically set to 1600 bpi when the tape returns to load point, regardless of the status set in the control unit. This automatic reset to 1600 bpi enables the tape drive to assume the correct mode for any subsequent read operation.

Table 11 Mode Setting Table

Tape Used	Head on Selected Drive	Control Unit Feature	Tape Unit Model	Response
1600 bpi 9-track	9-track	None	4, 5, 6	OK
800 bpi 9-track	9-track	None	4, 5, 6	Not capable
800 bpi 7-track	9-track	None	4, 5, 6	Not capable
556 bpi 7-track	9-track	None	4, 5, 6	Not capable
200 bpi 7-track	9-track	None	4, 5, 6	Not capable
1600 bpi 9-track	9-track	7-track NRZI	4, 5, 6	OK
800 bpi 9-track	9-track	7-track NRZI	4, 5, 6	Not capable
800 bpi 7-track	9-track	7-track NRZI	4, 5, 6	Data check
800 bpi 7-track	7-track	7-track NRZI	4, 5, 6	OK
556 bpi 7-track	7-track	7-track NRZI	4, 5, 6	OK
200 bpi 7-track	7-track	7-track NRZI	4, 5, 6	OK
1600 bpi 9-track	7-track	7-track NRZI	4, 5, 6	Data check
1600 bpi 9-track	9-track	9-track NRZI	4, 5, 6	OK
800 bpi 9-track	9-track	9-track NRZI	4, 5, 6	OK
800 bpi 7-track	9-track	9-track NRZI	4, 5, 6	Data check
1600 bpi 9-track	9-track	None	1, 2, 3	Data check
800 bpi 9-track	9-track	None	1, 2, 3	OK
800 bpi 7-track	7-track	7-track NRZI	1, 2, 3	OK
556 bpi 7-track	7-track	7-track NRZI	1, 2, 3	OK
200 bpi 7-track	7-track	7-track NRZI	1, 2, 3	OK
200 bpi 7-track	9-track	7-track NRZI	1, 2, 3	Data check

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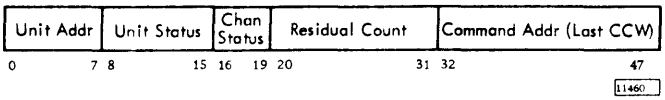
Read operations are adjusted automatically to the correct mode by sensing the formatting information that is written on the tape immediately after load point. A coded burst of bytes after load point indicates that the data on the tape is recorded at 1600 bpi. The absence of the burst of bytes indicates the data on the tape is recorded at 800 bpi, and the drive is set automatically to the 800 bpi mode.

Channel Status Word

Whenever the operation, or (in case of chaining) the sequence of operations initiated by an XIO instruction has been executed, the channel as well as the particular I/O device generates status conditions. These status conditions provide the basis for logical decisions which can be made after the completion of an operation. The program is informed about the completion of a transfer I/O instruction by the setting of the condition code in the PSW to 01. The completion of the

operation at the device may or may not coincide with the completion of the XIO. A check upon the unit status portion of the channel command word shows whether the device has ended its operation. However, when a device finished later (after the XIO), interrupt is requested. The interrupt program uses the information in the channel status word.

Channel Status Word



The unit address identifies the control unit and the tape drive specified in the XIO instruction that initiated the operation. The unit status shows the conditions detected in the control unit and in the device. The channel status shows all possible error conditions that might have occurred in the channel or in the interface. The residual count contains a number which represents the number of bytes that were not transferred because the I/O device ended the operation prematurely due to an incorrect length count. The command address is the address of the channel command word which specified the last operation. In case of chaining, the channel status word represents the status for the last operation in the chain that was attempted or executed.

Unit Status Bits

Bit 8 – Attention: This bit is not used with the IBM 2415 Tape Units.

Bit 9 – Status Modifier: This bit modifies the meaning of the "busy" bit and it can only appear together with this bit. Both bits on indicates "control unit busy." The status modifier bit is set together with the busy bit when an initial selection encounters a busy control unit. A typical example is the command Backspace File, which causes the control unit to remain busy after it has signaled "channel end." A new command is not accepted in this situation and therefore the status modifier and the busy bit are presented. Both bits are also presented when the control unit is addressed while it is executing a command or when "stack" is on and an address other than the stacked one is received. Stack is an internal holding of a unit status (and device address) for channel acceptance. When the status modifier and the busy bit are on, chaining is stopped.

Bit 10 – Control Unit End: This bit is turned on when the control unit detected an unusual condition while busy but after the channel end signal was accepted by the channel. Control unit end is also set when the control unit busy condition ends.

Bit 11 – Busy: Busy can occur only during an initial selection sequence. It indicates that the I/O device or control unit cannot execute a command because it is still executing a previously initiated command. Busy alone pertains to the tape drive; busy together with status modifier pertains to the control unit.

Bit 12 – Channel End: This bit is turned on when the action started by a Read, Read Backward, Write, Sense, or Mode Set command has been completed. All control commands such as Forwardspace Block, Erase Gap, Write Tape Mark, etc., set the channel end condition as soon as the command has been accepted by the control unit. The exact time at which channel end is generated depends on the operation and on the device used, however, it can be generated only after the operation has been started.

Bit 13 – Device End: This bit is generated when a tape drive (device) has completed an operation. Data transfer operations (read, write) cause simultaneous generation of device end and channel end upon completion of the data transfer. The Mode Set commands also generate simultaneous channel end and device end. Control operations cause device end when the operation is completed, which may be at a time when channel end is generated or later. For example, device end is generated when the tape reaches load point during a rewind.

Device end also indicates that further action can be initiated in the tape drive. For example, if a tape drive was addressed while it was not ready but subsequently becomes ready, then device end is set. Or, when the tape is unloaded (Rewind/Unload), device end is set although the unit is not ready. When the new tape is loaded, the unit becomes ready and device end is set once more. In all cases, the device end signal is maintained in the device until it is accepted by the channel on subsequent polling. Other units can operate while a pending device end is held in the device.

Bit 14 – Unit Check: This bit is set as a summary indication for nine individual error conditions. Any or all of them can set this bit. The exact meaning of this bit can be obtained by a subsequent Sense command which transfers the sense bytes 0 and 1 to the CPU for inspection. (See Sense Data Table.) For

example, any read backward, backspace block, or backspace file operation that runs up to or into the load point causes unit check. Data that was received during such an operation is considered invalid even when there is no separate data check.

Unit check is also set when a rewind/unload operation is completed at the control unit level. (This is no error.)

Bit 15 – Unit Exception: This bit is used to indicate an unusual condition, such as a write tape mark, write, or erase gap operation that runs into the "end of tape area." If that happens, the Tape Indicate light on the respective tape drive is turned on. Unit exception is also set when a tape mark is sensed during a read, read backward, forwardspace block, or backspace block operation.

Channel Status Bits

Bit 16 – Channel Data Check: This bit is set when a parity error is detected during a read or a sense operation.

Bit 17 – Interface Control Check: When the channel detects an invalid signal, other than data, the interface control check bit is turned on. This bit indicates that the channel output and input addresses failed to match. The check can also indicate a control unit malfunction. Operations are stopped immediately, and the IOC-light on the CPU console is turned on. An error number is displayed in data register E to aid the Customer Engineer in tracing the error.

Bit 18 – Incorrect Length: This bit indicates that the transferred record length differs from the length specified in the command word. Input operations can be either too long or too short while output operations (write) are only termed incorrect when the device ends the operation with a residual count.

Bit 19 – Program Check: This bit is turned on by all specification errors, such as invalid data address, invalid command code, invalid count (data length zero), or invalid sequence (initial CCW specifies TIC). A program check turns on the IOC-light on the CPU console.

NOTE: Data transfer operations are initiated only when no programming or equipment errors are detected during the initial selection sequence. The addressed device must respond with a "clear status" (all bits zero). If any bit is on while the channel is attempting an operation, the command is rejected.

Condition Code (CPU)

After the execution of a transfer I/O instruction, the condition code is set to allow the program to make logical decisions based on the result of the previous operation. Channel operations set the condition codes 01, 10, or 11. The code 00 is not set by any IOC condition.

Condition Code 01: This condition code is set when a new (updated) Channel Status Word (CSW) has been stored. An updated CSW is stored when an instruction has either been executed, rejected, or terminated for any reason by the control unit. At that time, the program is expected to check the CSW because errors detected by the channel as well as control unit or device busy conditions also set this condition code.

Condition Code 10: This condition code is set when the channel has rejected an instruction because of a channel busy condition. The channel is busy when the CPU is processing time shared operations, i.e. servicing other I/O devices. The CSW is not updated.

Condition Code 11: This condition code is set when the channel has a "not-operational" condition. Not operational exists when a control unit fails to recognize the unit address that is specified in the XIO instruction (no control unit attached, power off).

Interrupt

Interrupt is requested when the device end signal comes after the channel end signal. This is the case with all control operations in the IBM 2415 Tape Drives. All data transfer operations (which generate simultaneous channel end and device end) do not request interrupt. The commands that cause a request for interrupt are: Forwardspace Block, Forwardspace File, Backspace Block, Backspace File, Rewind, Rewind/Unload, Write Tape Mark, and Erase Gap. No request for interrupt can be made during the execution of chained commands. Only the last command in a chain can request interrupt, provided that it is a control command (such as Rewind, etc.).

Interrupt is also requested by the control unit end signal. The request for interrupt is only honored when the channel mask bit in the PSW is 1 and when no higher priority interrupt request exists. As long as the interrupt request is not honored, it remains pending. If a tape drive is addressed while it has an interrupt pending, the status is cleared from that unit and stored in the CSW.

A channel interrupt is identified by the device address 7 that is stored in the old PSW. The actual operation and device that requested the interrupt are identified in the CSW.

Sense Data Description

Sense Byte 0

Bit 0 – Command Reject: This bit is set when a write, write tape mark, or erase operation addresses a file-protected tape. It is also set when a "Data Converter On" Mode command is sent to a 7-track tape on a control unit with the 7-track compatibility feature without the Data Converter special feature.

Bit 1 – Intervention Required: This bit indicates that a condition exists in the addressed tape drive which requires manual intervention. This bit is also set if the addressed tape drive is not physically attached.

Bit 2 – Bus Out Check: This bit indicates that the bus out line has even parity which is an error.

Bit 3 – Equipment Check: This bit indicates that either a counter check or a C-compare check has occurred. If the C-compare check is not present, the equipment check was caused by a counter check.

Bit 4 – Data Check: This bit is a summary indication for data reg.VRC, LRCR, skew, read reg.VRC, multi-track, and end data checks. Any or all of these conditions result in a data check.

Bit 5 – Overrun: Overrun can occur only during a read, read backward, or a write operation. The check bit is set when the time limit for data transfer operations is exceeded.(See timing in Appendix.)

Bit 6 – Word Count Zero: This bit is set when the channel stops a write operation before the first character was transferred.

Bit 7 – Data Converter Check: During a read operation with data conversion (7-track), four tape characters are normally transferred as three bytes. When less than four characters are read and the packing effect cannot be achieved due to the structure of the tape character, the packing byte is filled with zeros and the data converter check is set. The check allows the program to take corrective action. (See Optional Features.)

Sense Byte 1

Bit 0 – Interblock Gap Noise: This bit is set when bits are found in the gap between the data block during a write, write tape mark, or erase gap operation. This causes neither a data nor a unit check.

Bits 1 and 2 – Tape Unit Status A and B: These two bits reflect the status of the addressed tape unit and decide on the response to an initial selection. When both bits are zero, the unit check is set because the tape unit is assumed to be non-existent (power off). A off, B on indicates that the device is not ready (which causes unit check when the device is addressed). A on, B off indicates that the unit is ready and not rewinding and therefore a "clear status" is sent in response to an initial selection.

Bit 3 – 7-Track: This bit indicates that the selected tape drive is a 7-track unit.

Bit 4 – At Load Point: This bit indicates that the tape in the selected unit is at the load point. This causes a unit check during all operations except during rewind.

Bit 5 – Write Status: This bit indicates that the selected tape drive is in write status.

Bit 6 – File Protect: This bit indicates that the tape in the selected unit is protected from writing or erasing (because the file protect ring is off the reel).

Bit 7 – Not Capable: This bit is used only when PE-type tape units are attached (2415-4, -5, or -6). It is further used only during read or read backward operations. The not capable bit is set when the following conditions exist:

1. Tape is read on unit equipped with 9-track head.
2. No identification burst is detected (either because 800 bpi is specified or because tape is faulty).
3. Control unit has no compatibility feature that can take care of 800 bpi 9-track (NRZI) operations.

Sense Byte 2

Bits 6 and 7: Only the bits 6 and 7 of sense byte 2 are used. Both bits are always on because they are forced unconditionally for compatibility reasons. The bits simulate a multiple track error which forces a program (which tests these bits) to automatically repeat the previous operation.

Sense Byte 3

Bit 0 – Data Register VRC: This bit indicates a vertical redundancy check. This means that data with faulty parity was set into the data register during a read or read backward operation.

Bit 1 – LRC Error/Multiple Track Error: This bit has a dual function. It indicates a Longitudinal Redundancy Check (LRCR) for NRZI operations and multiple track errors for PE operations.

1. LRCR Error: This bit indicates that the longitudinal parity of the record read does not agree with the check character of that record. The LRCR check monitors write, write tape mark, read, and read backward operations.
2. Multiple Track Error. This bit is set during read operations when more than one track has dropped below the acceptable amplitude for reading. Data is not corrected and therefore, the program must attempt the read operation again. The multiple track error may or may not be accompanied by a vertical redundancy check.

NOTE: If only one track contains an error, the automatic "in flight" error correction sends the correct data to the channel without stopping the tape.

Bit 2 – Skew Error: This bit indicates that excessive skew has been encountered during a write or write tape mark operation. Skew errors are detected because the two-gap read/write head in the IBM 2415 Tape Drive allows reading immediately after writing for check purposes.

Bit 3 – End Data Check: This bit is turned on when the synchronizing burst which follows the data is not recognized (2415-4, -5, or -6 only).

Bit 4 – Read Register VRC/Envelope Check: This bit has a dual function. It indicates a vertical redundancy check for NRZI operations or an envelope check for PE operations.

1. Read Register VRC: This indicates that a character with incorrect parity has been read into the read register. The check is effective during write operations.
2. Envelope Check: This check is set during write operations to indicate that at least one track has failed to reach an acceptable amplitude. If this check bit is on, the write operation must be repeated.

NOTE: The data register VRC and the read register VRC are both suppressed after a stop or overrun. Data checks occurring before stop or overrun are registered in the unit status byte as unit check. The LRCR check, however, remains active at all times.

Bit 5 – 1600 BPI: This bit indicates that the selected unit has a 9-track read/write head and is not set to any NRZI mode (2415-4, -5, or -6 only).

Bit 6 – Backward Memory: This bit indicates that the tape unit is in the backward state from a previous backward operation.

Bit 7 – C-Compare: This bit indicates that a parity difference was recognized during either one of the following operating modes.

- Data transfer in 9-track mode or data transfer in 7-track mode with data translator off. (See Data Translator.)
- Data transfer in data converter mode. The parity difference exists between the three eight-bit bytes and the four six-bit bytes (parity over 24 bits). (See Data Conversion section of this manual.)

Optional Features

9-Track Compatibility Special Feature (for IBM 2415-4, -5, and -6 only)

The 9-track NRZ feature permits a PE-type tape unit to read and write 9-track tape at 800 bpi using the NRZI method of recording. The change from the normal 1600 bpi-PE mode to the 800 bpi-NRZI mode is achieved by means of the respective Mode 2 Set command. The Mode 2 Set command affects write operations only. Read operations adjust themselves to the correct mode automatically. All mode setting occurs only when the tape is at load point. A coded burst of bytes on the tape located between the load point and the first data block, identifies the 1600-bpi-PE mode for read operations. The absence of this burst identifies the 800 bpi mode. The mode setting for write operations is determined by commands.

Read backward is possible only with tapes generated on IBM 2415, 2401, 2402, 2403, 2404 tape units.

7-Track Compatibility Feature (for IBM 2415 -1, -2, -3, -4, -5, and -6)

This feature permits the tape unit to read or write 7-track tape compatible with the current IBM 729/ IBM 7330 Tape Drives. The feature provides operation at densities of 200, 556, or 800 bpi, in even or odd redundancy mode with 0.725 inch nominal interblock gap using NRZI recording format. A part of this feature is a data translator which translates EBCDIC eight-bit code to BCD six-bit code or vice versa. The 7-track feature may not be used with read backward unless the tape being read was recorded on one of the following tape units - 2415, 2401, 2402, 2403, or 2404.

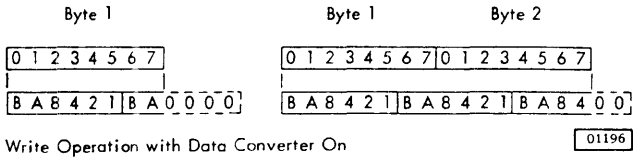
Data Conversion

The data conversion feature expands the capability of the 7-track compatibility feature. With the data converter on, it is possible to write any System/360 data (entire EBCDIC) on 7-track tape with maximum packing efficiency. Data conversion cannot be used, however, during read backward operations.

Eight-bit bytes are written on 7-track tape as six-bit characters with odd parity, in the following manner.

A single byte is converted into two characters, with the four low-order bits of the second character automatically written as zeros. Two bytes are converted to three characters, whereby the two low-order bits of the third character are automatically written as zeros. Three bytes are converted into

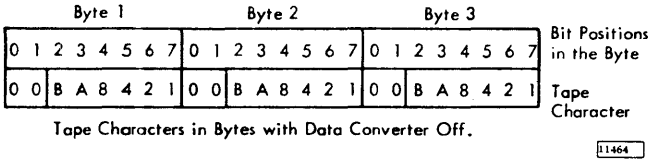
four characters without rest. When a converted tape is read with the data converter on, the bytes are reassembled in original form, the character bit zeros being automatically removed.



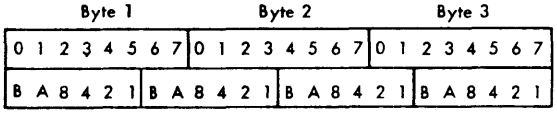
Write Operation with Data Converter On

If a 7-track tape was written on another system (for example, IBM 1401 Processing Unit), reading is as follows.

During a read operation with the data converter off, every tape character (BCD) is set into the low-order six bit positions of the byte and the high-order two bits are set to zeros. During a read operation with the data converter on, four tape characters are packed into three bytes.

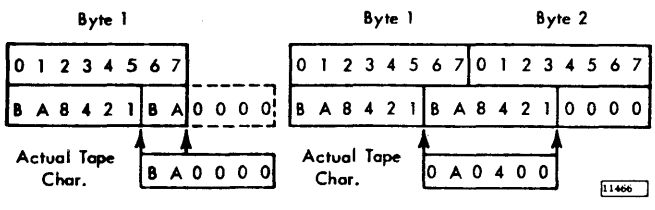


Tape Characters in Bytes with Data Converter Off.

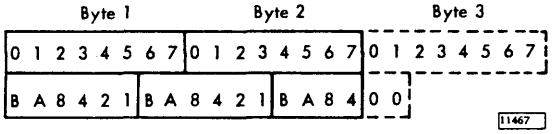


Tape Characters in Bytes with Data Converter On.

Whenever less than four characters are transferred, a special packing arrangement is employed. For example, two tape characters are packed into one byte if the character bits 8, 4, 2, 1 are all zeros. However, when the bits 8, 4, 2, 1 are not all zero, the two characters are set into two bytes with the bits 4, 5, 6, 7 of the second byte set to zero and the data converter check turned on.



When successfully packed characters are read back, zeros must be added to retrieve the original character. The data converter check indicates that zeros must be subtracted to obtain the original character. Three tape characters are packed into two bytes if bits 2 and 1 of the third character are zero; if they are not, a third byte is used with the bits 2, 3, 4, 5, 6, and 7 set to zero. The data conversion



check is set to indicate that zeros must be subtracted to obtain the original character bit configuration. The same holds true for one tape character because it also does not fill one byte completely. One tape character is transmitted as one byte with the bits 6 and 7 of that byte set to zero and the data converter check turned on.

Retrieval (write back) of the packed tape characters is accomplished by using:

Input Record Length In bytes	Bit Position of last bit from Tape Byte	Bit	Number of zero bits to be added or subtracted
1	2	3	+4
1 with Data Conv Check	1	5	-2
2	3	1	+2
2 with Data Conv Check	2	3	-4
0 (3)	3	7	-0
0 (3) with Data Conv Check	3	1	-6

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IBM 2311 DISK STORAGE, MODELS 11 AND 12

The IBM 2311 Disk Storage, with easily interchanged IBM 1316 Disk Packs, affords the user the programming flexibility of large on-line storage capacity and virtually unlimited off-line storage capacity. As with magnetic tape, a virtually unlimited volume of data can be written on 1316 disk packs, separated from the 2311, and stored off-line until needed.

Two models of the IBM 2311 Disk Storage (model 11 and model 12) are available for use with the System /360 Model 20. Up to two 2311 Disk Storage Drives, (either 2311-11 or 2311-12) can be attached and controlled by the Storage Control special feature; however, both models cannot be attached to the same system.

Disk packs written on a 2311 model 11 may be read on a 2311 model 11 attached to any System/360 Model 20. Disk packs written by a 2311 model 12 can also be read by a 2311 model 12 attached to any System/360 Model 20. Compatibility between 2311 model 11 and model 12 is limited to the extent that the 2311-11 reads and writes over 200 cylinders on the disk pack and the 2311-12 reads and writes on only the outer 100 cylinders.

The 2311-11 and the 2311-12 differ only in the number of track positions available. Each track position comprises a ten-high stack of disk surfaces and read/write heads, forming a cylinder of data. The 2311-11 has 200 cylinders of data available; the 2311-12 has 100 cylinders available (Figure 6).

	2311 Model 11	2311 Model 12
Storage Capacity	5.4 Million Bytes	2.7 Million Bytes
Data Transfer Rate	156,000 Bytes/Sec	156,000 Bytes/Sec
Data Bytes/Sector	270 Bytes	270 Bytes
Sectors/Track	10	10
Data Bytes/Track	2700 Bytes	2700 Bytes
Data Bytes/Cylinder	27,000 Bytes	27,000 Bytes
Data Cylinders	200	100
Alternate Cylinders	3	3
Maximum Access Time	135 ms	90 ms
Average Access Time	75 ms	60 ms
Minimum Access Time	25 ms	25 ms
Disk Rotation Time	25 ms	25 ms

11472

Figure 6. IBM 2311 Disk Storage Characteristics

Storage Capacity

Storage capacity for the 2311 model 11 is 5.4 million bytes. It is based on the use of 200 of the total 203 cylinders for data and 3 cylinders for use as alternates (spares for use in the event of surface damage to a data track). Storage capacity for the 2311 model 12 is 2.7 million bytes. It is based on the use of 100 of the total 103 cylinders for data and 3 cylinders for alternates.

Device Description

The IBM 2311 Disk Storage consists of two main components: the 2311 Disk Storage Drive and the IBM 1316 Disk Pack.

Storage Medium (1316 Disk Pack)

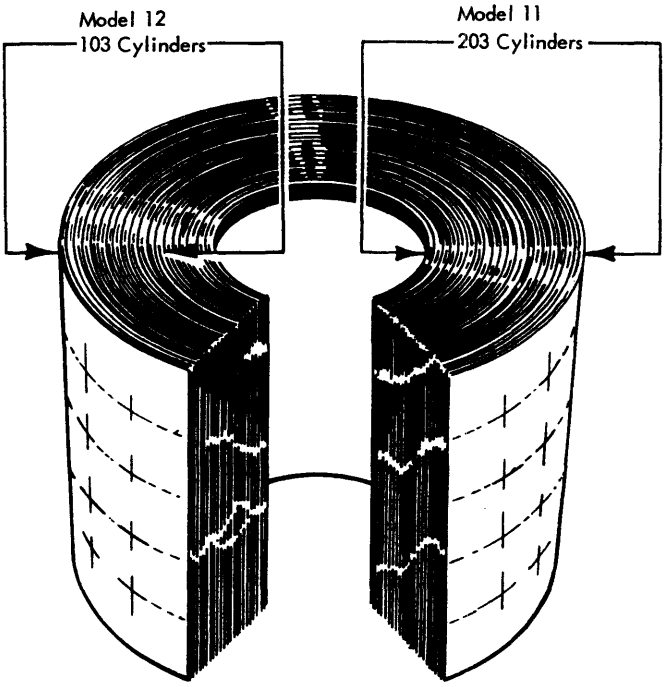
Each disk pack consists of six 14-inch disks, mounted 1/2 inch apart on a central hub. Data is recorded on the inside ten disk surfaces. The two outer surfaces are covered by protective plates. The entire assembly of disks, hub, and protective plates is rotated at 2,400 revolutions per minute (25 ms per revolution). Each disk pack weighs about ten pounds.

The two-piece plastic cover is designed to protect disks against damage. A built-in handle on the top cover makes carrying easy and efficient. A self-locking device in the handle permits removal of the top cover only when the pack is mounted on the disk storage drive.

Access Mechanism

When the 1316 Disk Pack is mounted in the 2311 Disk Storage Drive, information is written on and read from the ten disk surfaces by magnetic read/write heads. These ten read/write heads are mounted in pairs between each two disks on a movable comb-like access mechanism. When in operation, the read/write heads float over the disk surfaces on a thin film of air.

The 2311 model 11 access mechanism can be moved horizontally to any of 203 discrete track positions; the 2311 model 12 can be moved to 103 track positions. Since all ten read/write heads are moved together by the access mechanism, a vertical cylinder of ten data tracks is formed at each track position.



Cylinder Concept

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Access Time

Cylinder-to-cylinder (horizontal) access time varies according to the number of cylinders traversed. Access time from a cylinder to an adjacent cylinder is 25 ms. For the 2311 model 11 the maximum access

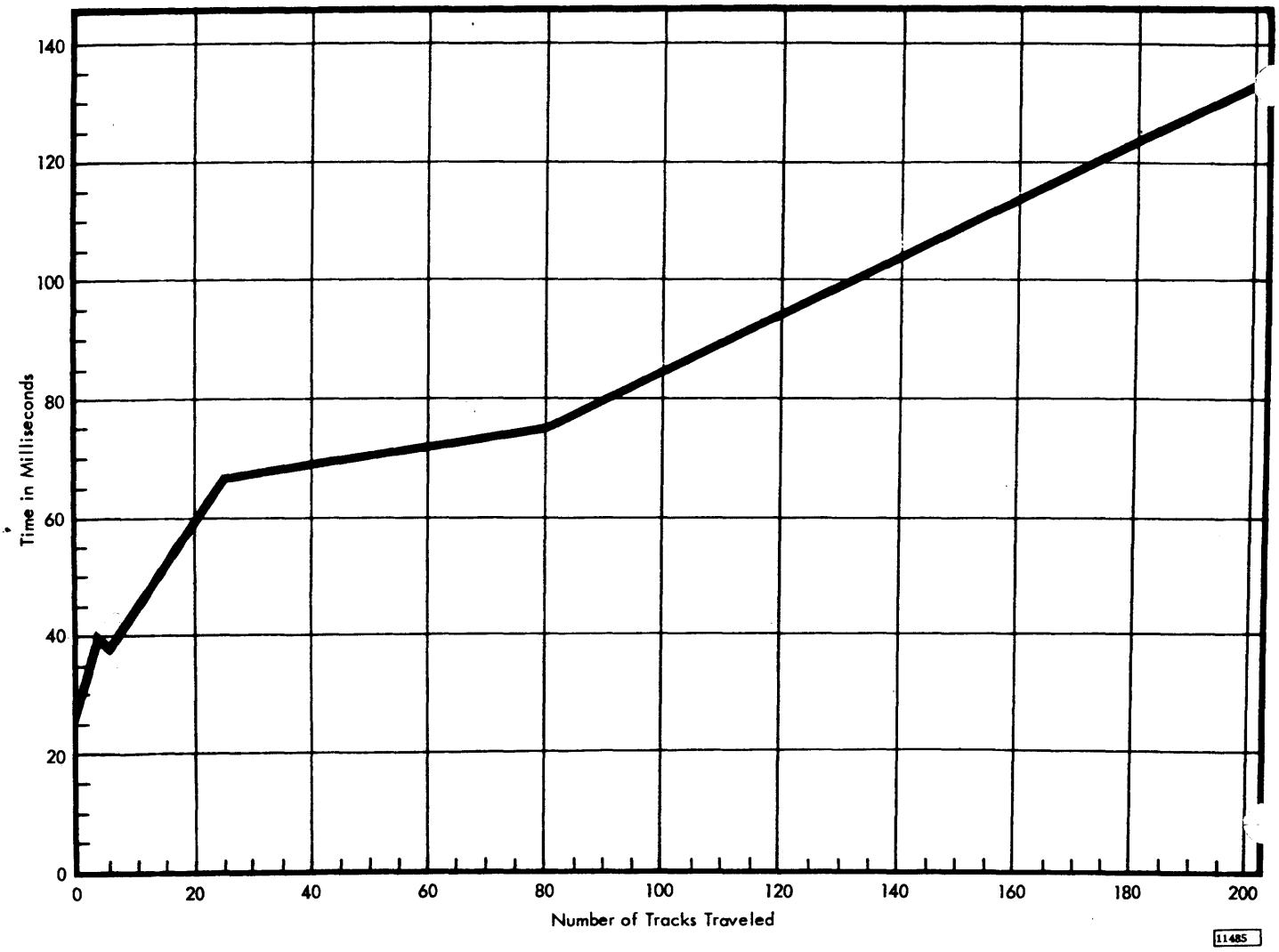


Figure 7. Access Time

time (from cylinder 202 to cylinder 000) is 135 ms., and the average time for "random" accesses is approximately 75 ms. For the 2311-12 the maximum access time (from cylinder 102 to cylinder 000) is 90 ms, and the average time for random accesses is approximately 60 ms (Figure 7).

Once the access mechanism has reached a cylinder position, additional time is required for disk rotation to the desired record. At 2,400 revolutions per minute, rotation time is 25 ms, and one-half revolution (12.5 ms) is the average rotational delay.

Figure 7 shows the approximate time for access mechanism movement in either direction, excluding rotational delay. This may be used as an aid in programming for the most efficient utilization of the storage device.

Operator Controls and Indicators

Start/Stop Switch: This switch is on when it is in the Start position.

With the 2311 attached to a System/360 Model 20, press this switch to the Start position to supply power to the disk drive motor and other 2311 components. When the disk drive motor has come to speed, and other components are ready for operation, the read/write heads are moved into position and the access mechanism performs an automatic seek cycle.

Pressing the Start/Stop switch to the Stop position causes the access mechanism to retract from the disk pack and removes power from the disk drive motor. Automatic braking stops disk pack rotation in a few seconds. Approximately 2 minutes are required

from the time the switch is set to Stop until a disk pack can be removed, replaced, and ready for operation.

Select Lock Indicator: When on, this indicates a machine condition which requires the attention of an IBM Customer Engineer. This condition causes the disk storage drive to be disabled and stops the usage meter.

Enable/Disable Switch: When the CPU is in the stopped state, this switch enables or disables the communication of the storage drive with the CPU. It also enables or disables the 2311 usage meter.

If the CPU is running when the switch setting is changed, the storage drive and usage meter operating status are not changed until the CPU is placed in the stopped state. (See also Select Lock Indicator.)

Disk Pack Handling

Each disk pack is protected in transit by special carton inserts and special protective material.

When received, examine the carton closely. If its condition is acceptable, remove the disk pack and store it. Keep the carton and inserts; you may need them later.

If the carton or its contents show any unusual shipping damage, do not use the disk pack. Retain the damaged carton and disk pack in its "as received" condition and notify an IBM Customer Engineer immediately.

Disk packs have been designed for ease of transport from location to location.

For best shipping results:

1. Be sure the pack is secure in its two-piece cover.
2. Use only the specially designed IBM shipping carton with its special protective padding properly inserted. If the original carton is worn or damaged, a new carton may be ordered from an IBM office.

Handle a disk pack only with its cover on.

If the disk pack is accidentally dropped, or receives a sharp impact of any kind, call an IBM Customer Engineer before using it.

Disk Pack Labeling: For positive identification, small adhesive-backed labels can be placed on the disk pack center hub. Labels in this location can be read through the transparent disk pack cover.

The following operating procedures should be followed when labeling disk packs:

1. Use adhesive-backed labels which can be applied and removed easily.
2. Use a writing implement, like a pen or felt-tip marker, which does not produce loose residue. Do not use a lead pencil.
3. Write on the label before it is applied to the disk pack.
4. Place the label only on the center hub, not on the disk pack cover or top disk surface.
5. Use a new label if changes are necessary. Never use an eraser because microscopic eraser particles can damage disk surfaces and read/write heads.

Disk Pack Loading and Unloading: Follow these procedures for rapid, effective disk pack changing.

Loading:

1. Open the 2311 cover.
2. Remove the bottom disk pack cover by turning the bottom locking knob.
3. Place the 1316 Disk Pack (still contained in top cover) on the 2311 spindle.
4. Turn the top cover in direction of ON arrow until firm resistance is met.

5. Lift the top cover from the disk pack.
6. Close the 2311 cover.
7. Press the 2311 Start key.
8. Reassemble the top and bottom covers of the disk pack to keep the interior clean.
9. Store the covers in a clean cabinet or on a clean shelf.

CAUTION: Do not leave disk pack top cover inside disk drive.

Unloading:

1. Press the 2311 Stop key.
2. Wait for the disk pack to stop rotating.
3. Separate the top and bottom disk pack covers.
4. Open the 2311 cover.
5. If necessary, move the brushes gently clear of the disk pack.
6. Place the disk pack top cover over the disk pack.
7. Turn the top cover in direction of OFF arrow at least two full turns.
8. Lift the top cover, now containing the disk pack, from the spindle.
9. Fasten the bottom cover to disk pack firmly.
10. Close the 2311 cover.
11. Store the disk pack in a clean cabinet or on a clean shelf.

Disk Pack Storage: To ensure maximum disk pack life and reliability:

1. Store the disk packs flat, not on edge.
2. Each pack should rest on a shelf, not on another disk pack.
3. Store in a clean, enclosed metal cabinet or a similar fire-resistant container; never in direct sunlight.
4. Store disk packs in a machine-room atmosphere (60°F to 90°F, 10% to 80% humidity).
5. If disk packs must be stored in a different environment, allow two hours for adjustment to machine room atmosphere before use.

DATA TRANSFER

Information is transferred between the Central Processing Unit (CPU) and the Storage Control feature one byte at a time (in parallel). Information is transferred between the Storage Control feature and the selected 2311 Disk Storage one bit at a time (in serial). Thus, the Storage Control feature translates serial data from disk storage into parallel data for internal CPU processing, and translates parallel data from the CPU into serial data for entry into disk storage (Figure 8).

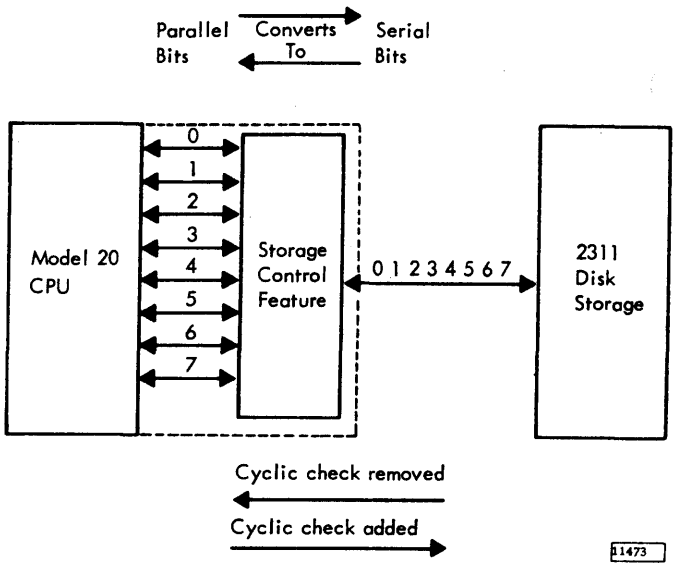


Figure 8. Data Transfer

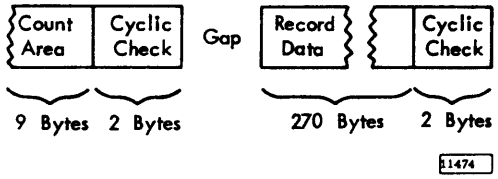
Data Records

A group of related bytes is called a "field." A series of related fields is called a "record." The data length of each record is fixed at 270 bytes. If the actual data length to be written in a record is less than 270 bytes, it is the responsibility of the programmer to add sufficient zeros or fill characters to make the data length equal to 270 bytes.

Data Checking

Storage Control Feature -- Cyclic Check

In direct access storage devices controlled by the System/360 Model 20 Storage Control feature, data is stored and retrieved in areas. Checking accuracy in data transfer (to or from attached storage) is done by associating two check bytes with each area.



As data is transferred from the CPU to an attached storage device, the storage control computes two cyclic check bytes which are added to the end of each area. The two cyclic check bytes are arithmetically coded to represent the data in the associated area.

During a transfer from a storage device, all areas read are inspected by the Storage Control

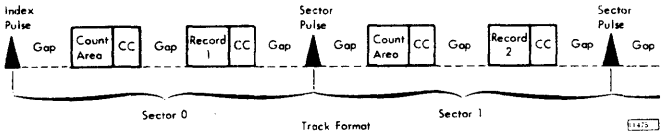
feature. Cyclic check bytes are recalculated for each area and compared with those retrieved from storage. An unequal comparison will set data check error indicators.

The cyclic check code detects the following types of errors:

1. All errors occurring within a 16-bit span.
2. All errors involving an odd number of bits over any span.

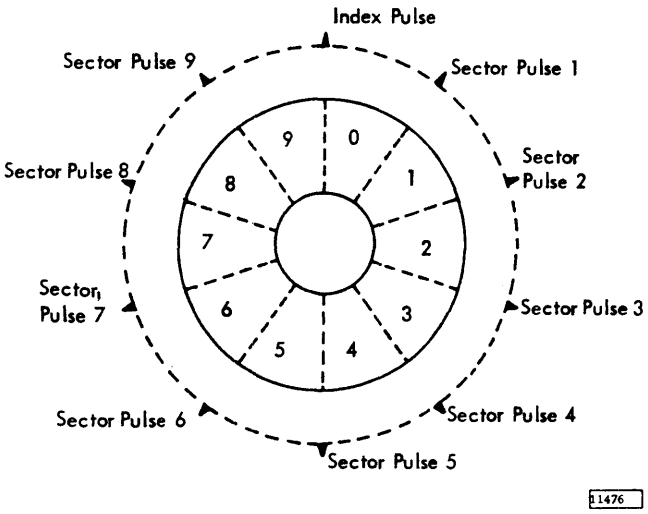
TRACK FORMAT

Data is stored in the IBM 2311 Disk Storage in a track format defined by the storage control feature in the System/360 Model 20 CPU. Each track has ten equal divisions called sectors, which are identical in length and format.



Sector Format

The ten sectors on each track are marked by physical points on the disk periphery which are sensed as sector pulses as the disk assembly rotates.

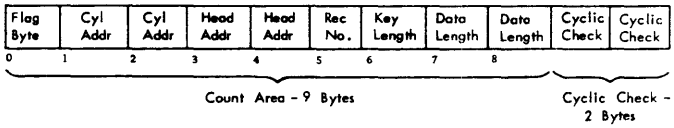


One of the sector pulses is called the index pulse and is used as a physical beginning point for the data on the track. For the purpose of description, a track is treated as a ten-sector group of data, beginning and ending with an index pulse. The data, as it is written on disk storage, is actually in the form of discrete, concentric circular tracks stacked ten high in the form of cylinders. Each sector is divided into two parts, the count area and the data area.

Count Area

The count area is a convenient means for uniquely identifying each 270-byte data record in disk storage. A count area precedes each data area, identifying it by cylinder number, head number, and sector number. Information about the condition of the track is also contained in the count area.

There are ten count areas per track; each contains nine bytes of information plus two cyclic check bytes.



Flag Byte: This byte is used to indicate the condition of the track. The three possible states of a track are:

0000 0000 -- Original good track
0000 0010 -- Defective track
0000 0001 -- Alternate track

Cylinder Address: Identifies the cylinder location of the data to be used in the operation. The cylinder address is two bytes long. The high-order byte (adjacent to the flag byte) must be zero.

Head Address: Identifies the head location of the head on the access mechanism. The heads on the access mechanism are numbered sequentially from 0-9. The head address is two bytes long. The high-order byte must be zero.

Record Number: Identifies the number of the record on the track. Each sector contains one record.

Key Length: This byte must be zero.

Data Length: These two bytes must contain the number 270 to represent the fixed data length of each sector.

Cyclic Check: These two bytes are appended to the nine-byte count area and are used only for error detection.

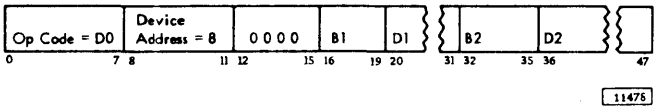
Data Area

The data area is a continuous, fixed-length area 270 bytes long. Two bytes of cyclic check follow the 270 bytes of data.

INSTRUCTIONS

Transfer I/O (XIO)

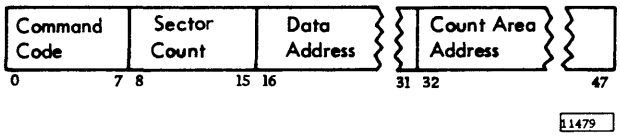
All input/output operations between the System/360 Model 20 CPU and 2311 Disk Storage are initiated by a Transfer I/O Instruction (XIO). An XIO instruction specifies the devices to be used in the operation and the core storage address of the Channel Command Word (CCW) which contains further information about the operation to be performed.



Bit Position	Function
0-7	Operation code - Op code is D0 for all XIO instructions.
8-11	Device address - 8 for the storage control.
12-15	Not used - must be set to zero.
16-31	Contains direct or effective address of the Channel Command Word (CCW) to be used for the operation.
32-47	Contains the direct or effective address of the disk unit to be used for the operation. After effective address generation, only the last eight bits (bits 40-47) are used. If used as a direct address, only the last eight bits represent this address. If the entire field (bits 32-47) is zero, the CPU stops on a specification error. If bits 40-47 are zero, the program check bit (bit 19) in the CSW is set.

Channel Command Word (CCW)

The CCW specifies the command to be executed, the number of sectors to be used, and the main storage addresses of the data and count areas involved in the operation. The address of the CCW is derived from the B1-D1 fields of the preceding XIO instruction.



Bit Position	Function
0-7	Command code - specifies exact operation to be performed.
8-15	Sector count - specifies the number of sectors to be used in the operation. Not used for seek, sense, or recalibrate operations.
16-31	Data address - specifies the leftmost main storage location of three different information fields, depending on the command code: 1. For read, write, and verify operations, the data address specifies the 270-byte field for the first sector. 2. For seek operations, the data address specifies the six-byte seek-address field. 3. For sense operations, the data address specifies the five-byte field into which the sense information is stored. 4. For scan operations, the data address specifies the compare field.
32-47	Count Area address - specifies the leftmost main storage location of the nine-byte count area for the first sector.

Command Code (Figure 9)

The command code in the CCW, in bit positions 0-7, specifies to the storage control the exact operation to be performed. The command pertains to the disk storage drive identified in the unit address portion of the initiating XIO instruction. The operations performed and the command codes are shown below. The command codes are in hexadecimal form.

Function	Command Code
Seek	03
Recalibrate	0B
Read Data	02
Read Count	32
Read Count and Data	12

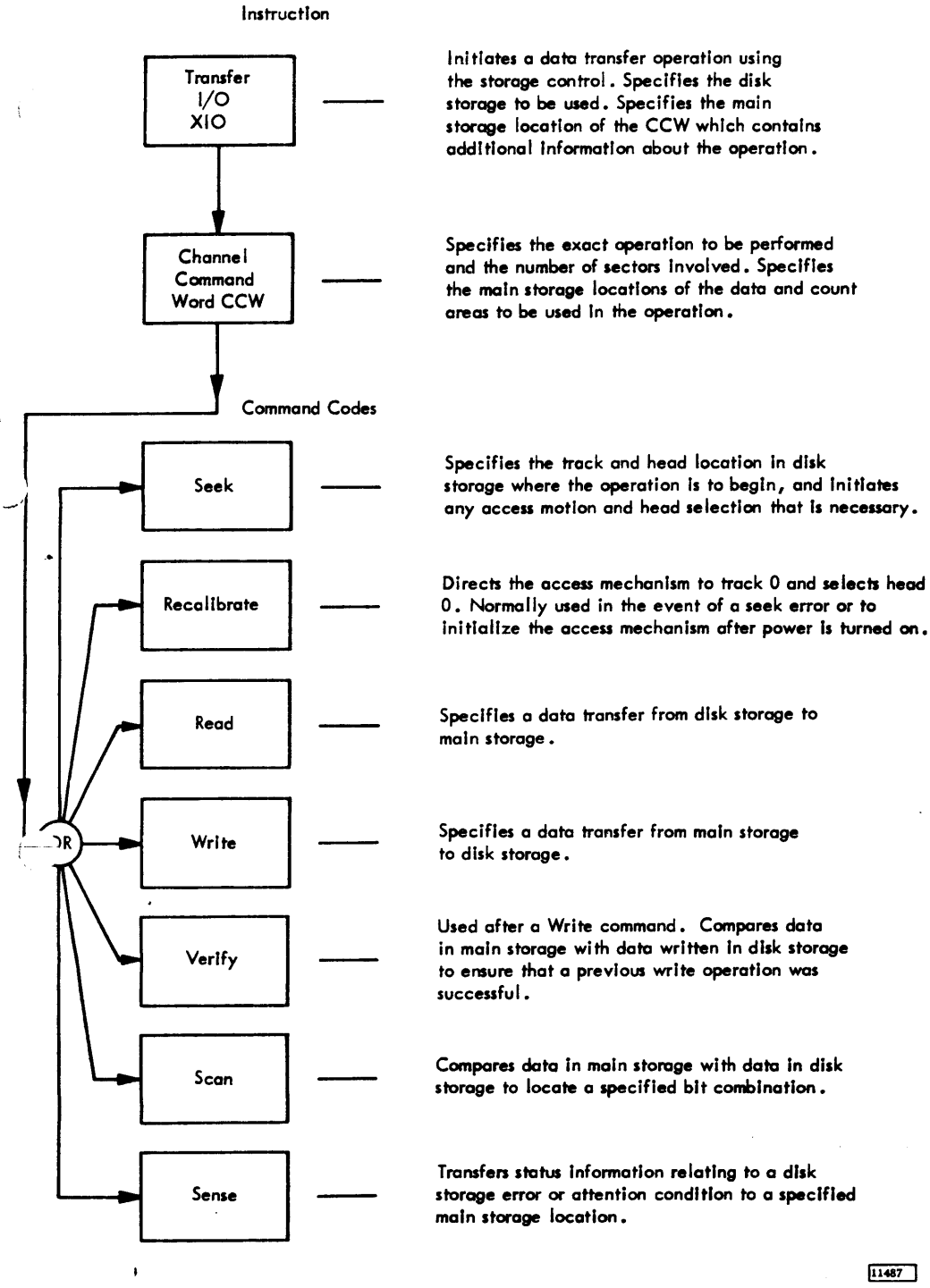
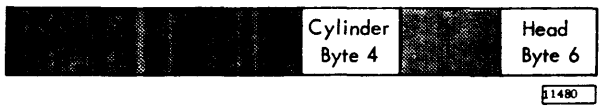


Figure 9. Instructions and Command Codes

Function	Command Code
Write Data	01
Write Count and Data	11
Verify Data	41
Verify Count and Data	C1
Scan Low or Equal	51
Scan Equal	61
Scan High or Equal	71
Sense	04

Seek: A Seek command specifies the track and head location in disk storage where an operation is to begin, and initiates any access motion and head selection that is necessary. The data address portion (bits 16-31) of the CCW specifies the leftmost main-storage location of a six-byte seek address; the sector count and count area portions of the CCW are not used for a seek operation. The seek address has the following format:



Byte 4 specifies the track location of the cylinder in which the data is located. If an IBM 2311 Disk Storage Drive, Model 12 is attached, this byte may contain any number from 0 to 102. If a 2311 model 11 is attached this byte may contain any number from 0 to 202. If the cylinder number is greater than the number of cylinders available, the program check bit in the CSW is set. Byte 6 specifies the head to be selected and may contain any number from 0 to 9; a number greater than 9 in this byte position causes the program check bit in the CSW to be set. Bytes 1, 2, 3, 5, and the high order four bits of byte 6 are not used, but they must all be set to 0. When the seek operation is decoded from the command code in the CCW, the storage control uses the seek address specified in main storage and the present address stored by the storage control to compute the direction of motion and the number of tracks to be moved. Access motion then begins and the CPU is released to resume normal processing operations. When the specified cylinder address is reached, the storage control issues an interrupt request to the CPU. Seek access motion can be overlapped with normal CPU processing or it can be overlapped with a seek operation on another disk storage drive.

Recalibrate: A Recalibrate command is used to direct the access mechanism to cylinder 0 and select head 0. A Recalibrate command is usually used only if the present location of the access mechanism is unknown, as would be the case if a previous seek operation was not successfully completed. The sector count portion (bits 8-15), the data address portion (bits 16-31), and the count area address portion (bits 32-47) of the CCW are not used for a recalibrate operation and are ignored.

When a recalibrate operation is decoded from the command code in the CCW, the storage control initiates access motion in the direction of cylinder 0 and releases the CPU for normal processing or I/O operations. When cylinder 0 is located, the storage control issues an interrupt request to the CPU.

The storage control is busy for the first 15 milliseconds of a recalibrate operation and rejects any disk storage operations during this period; however, CPU processing operations can be performed during this period. A seek operation on one disk storage drive can be completely overlapped with a recalibrate operation on another disk storage drive if the seek operation is issued first.

Read Data: A Read Data command is used to transfer data from a sector in disk storage to a specified location in main storage. The data address portion of the CCW specifies the leftmost main-storage location where the input data is to be stored. Data is placed in storage in successively higher main-storage addresses. The length of the input data from disk storage is fixed at 270 bytes for each sector read.

The number of sectors specified for the operation can range from a single sector to an entire cylinder (100 sectors); however, since a complete cylinder in disk storage contains more data than the entire main storage can accommodate, the programmer must keep track of available main-storage space and tailor disk storage operations accordingly. For multiple sector operations, the data for sequential sectors is located in sequentially higher-numbered addresses in main storage in groups of 270 bytes. The sector count portion of the CCW specifies the number of records to be read during this operation.

The count area address in the CCW specifies the leftmost main-storage location of the nine-byte count area for the first sector to be read.

NOTE: Although the last previous seek operation has specified a head to be selected, final head selection is performed under control of the count area that is used for the read data operation, provided the flag byte is not 0000 0001. The cylinder that is used is determined by the last previous Seek command.

A multiple sector read data operation can begin at any sector within a cylinder, and requires only one count area in main storage. The record number in

the count area is updated by one automatically for each sector, and the head address is also increased by one when the record number changes from 9 to 0. At the end of the operation, the head and record portions of the count area in main storage are restored to their initial values.

When a read data operation is decoded from the command code in the CCW, the storage control does an automatic compare on the count area in main storage with the count area recorded on the track until the correct sector is located. When the correct sector is located, the data area of the sector is transferred to a main-storage location specified by the data address portion of the CCW. On multiple sector reads, the count area of each successive sector is compared to the updated count area in main storage before the data for that sector is transferred.

Multiple sector read data operations can begin at any sector within a cylinder, but are valid only for consecutive sectors within that cylinder. During multiple sector read operations the operation is terminated at the end of any sector in which a data error is detected.

Read Count: A Read Count command is used to transfer data from a count area in disk storage to a specified location in main storage. The count area address portion of the CCW specifies the leftmost main-storage location where the input count area is to be stored. The count area length is always 9 bytes.

NOTE: The head and cylinder that are used for the read count operation are specified by the last previous Seek command.

A read count operation is limited to the boundary of one track (10 sectors). The sector count portion of the CCW can be any number from 1 to 10; however, the read count operation stops after the first count area that is read successfully, regardless of the number in the sector count. The number of unread count areas on the track is placed in the residual count area portion of the Channel Status Word (CSW) by the storage control when the read count operation is stopped.

A read count operation begins in the first sector after index point with the first count area on the track. The operation continues on that track until either a count area has been successfully transferred to main storage or until all ten count areas on the track have been attempted without success. If the read count operation has been attempted on all ten sectors without a successful transfer, a no-record-found condition is set in the CSW by the storage control.

The data address portion of the CCW is not used in a read count operation, but it is checked for validity and must be within available storage and it must not refer to the protected first 144 bytes of main storage. Data at this address is not altered. The sector count portion is also not used for a read count operation, but the count is checked for validity and must be a number between 1 and 10.

Read Count and Data: A Read Count and Data command is used to transfer count and data information from a track in disk storage to specified locations in main storage. The CCW specifies the leftmost main-storage locations where the input count and data are to be stored. The length of the count area is nine bytes and the data area is 270 bytes for each sector read. The number of sectors to be read is specified in the sector count portion of the CCW and can be from 1 to 10 sectors.

NOTE: The head and cylinder that are used during the read count and data operation are specified by the last previous Seek command.

The read count and data operation begins in the first sector after index point and continues until the specified number of sectors on that track has been read. (The operation is terminated at the end of any sector in which a read error is detected.) For multiple sector operations, the count information for sequential sectors is located in sequentially higher-numbered addresses in main storage in groups of nine bytes per sector; data is stored similarly but separately in groups of 270 bytes per sector.

Write Data: A Write Data command is used to transfer data from a specified main-storage location to a sector in disk storage. The data address portion of the CCW specifies the leftmost main-storage location of the area containing the data to be transferred to disk storage. The length of the output data area in main storage is 270 bytes for each sector to be written in disk storage. The number of sectors to be written is specified in the sector count portion of the CCW.

The number of sectors specified for the operation can range from a single sector to an entire cylinder (100 sectors); however, since a complete cylinder in disk storage contains more data than the entire main storage can accommodate, the programmer must keep track of available main-storage space and tailor disk storage operations accordingly. For multiple sector operations, the data for sequential sectors is located in sequentially higher-numbered addresses in main storage in groups of 270 bytes.

The count area address portion of the CCW specifies the leftmost main-storage location of the nine-byte count area for the first sector of data to be written.

NOTE: Although the last previous seek operation has specified a head to be selected, final head selection is performed under control of the count area that is used for the write data operation, provided the flag byte is not 0000 0001. The cylinder that is used is determined by the last previous Seek command.

A multiple sector write data operation can begin at any sector within a cylinder, and requires only one count area in main storage. The record number in the count area is updated by one automatically for each sector, and the head address is also increased by one when the record number changes from 9 to 0. At the end of the operation, the head and record portions of the count area in main storage are restored to their initial values.

Multiple sector write data operations may begin at any sector within a cylinder, but are valid only for consecutive sectors within that cylinder. During a multiple sector write operation, the operation is terminated at the end of any sector in which a data error is detected.

Write Count and Data: A write count and data operation is used to transfer one complete track, 10 sectors of count and data information, from main storage to disk storage. The sector count portion of the CCW must specify 10 for this operation or an error is detected. This operation begins in the first sector after index point and transfers ten count and data areas from separate main-storage locations to a track in disk storage.

The data address portion of the CCW specifies the leftmost main-storage location of the 2700 bytes (10 sectors x 270 bytes per sector) of data to be transferred to disk storage; the count area address portion of the CCW specifies the leftmost main-storage location of the 90 bytes (10 sectors x 9 bytes per sector) of count information to be transferred to disk storage.

NOTE: The head and cylinder that are used for the write count and data operation are specified by the last previous Seek command.

All of the ten count areas on the track must contain identical flag bytes. In addition, the count area must be identical for all ten sectors, except for the record number. The record numbers must be in sequence, and the first count area should contain record number 0 through the tenth count area which must contain record number 9.

Verify Data: A Verify Data command is a means for performing a bit-by-bit comparison of data in main storage with data residing in disk storage. It is normally used after a write operation to ensure that the data was written correctly and can be retrieved (read) correctly from disk storage. A verify operation is a convenient means for the programmer to check data integrity in disk storage while the original data is still available in main storage.

The count area address and the data address portions of the CCW specify the leftmost main-storage locations of the count area and data area respectively. The length of the data area is 270 bytes for each sector to be verified; the length of the count area is always nine bytes. The number in the sector count portion of the CCW specifies the number of sectors to be used for the operation.

NOTE: Although data errors occur only rarely, it is strongly recommended that all data written on disk storage be verified by using the Verify Data command. At the time when a data error is detected by the verify data operation, the information needed for the subsequent re-write operation is still available in main storage, thus facilitating error correction. At a later time, the correction of a non-detected write error may cause untimely interruptions and may necessitate the retrieval and processing of original data.

Verify Count and Data: A verify count and data operation performs a bit-by-bit compare of the data in main storage with the data written on disk storage. This command is a means for comparing data residing on disk with data in main storage and serves to check that a previous write count and data operation was successful. The count area address and the data address portion of the CCW specify the leftmost main-storage locations of the count and data areas respectively. Data in storage is located in successively higher numbered main-storage addresses. The length of the input data area is 2700 bytes. The length of the count area is 90 bytes. A verify count and data operation is a full track operation so the number in the sector count portion of the CCW, bits 8 through 15, must specify ten. This operation begins at the first count area on the track and verifies all count and data areas on a single track. If the sector count contains any number other than 10, the program check bit in the CSW is set.

Scan Low or Equal: The Scan Low or Equal command compares a 270-byte area in main storage with data stored on disk storage. The programmer may block the compare of any portion of the 270-byte area in

main storage simply by establishing a mask consisting of all 1 bits for the portion to be blocked. The comparison is made only on bytes which are not masked out by 1 bits in main storage. The data area length, however, must always be 270 bytes regardless of the mask involved or the number of sectors to be scanned. If only ten bytes are to be scanned, the data area in main storage must contain an additional 260 mask characters completely set to 1 bits.

The data address of the CCW specifies the leftmost main-storage location of the area containing the data to be compared with the data on disk storage. The number in the sector count portion of the CCW (bits 8-15) specifies the number of sectors to be used for the operation. A maximum of one cylinder (100 sectors) can be scanned with one command.

The count area address in the CCW specifies the leftmost main-storage location of the nine-byte count area for the first sector to be scanned.

NOTE: Although the last previous seek operation has specified a head to be selected, final head selection is performed under control of the count area that is used for the scan operation, provided the flag byte is not 0000 0001. The cylinder that is used is determined by the last previous Seek command.

For multiple sector scans, the count area is updated between sectors by the storage control. The scan low or equal operation begins when an equal compare between the count area in main storage and the count area on the disk storage is detected. The operation terminates when a data area on the disk is found which is lower than, or equal to, the data area in main storage, or the number of sectors called for in the operation have been scanned without finding a low or equal condition. The operation also terminates at the end of any sector in which a data error is detected. The status modifier (bit 9 in the CSW) is set to indicate that the scan was successful. If an equal compare occurs, only bit 9 of the status modifier is set to 1.

If a low compare occurs, the status modifier (bit 9 in the CSW) and not equal scan (bit 8 in the CSW) are both set to 1. In addition, the count area for the sector on which the compare occurred is now located in main storage at the location of the original count area. When the scan operation is unsuccessful (no compare), the count area in main storage contains the count field of the last sector scanned.

Scan Equal: The Scan Equal command compares a 270-byte area in main storage with data stored on disk storage. The programmer may block the compare of any portion of the 270-byte area in main storage simply by establishing a mask consisting of all one bits for the portion to be blocked. The comparison is made only on bytes which are not masked out by 1 bits in main storage. The length however, must always be 270 bytes, regardless of the mask involved or the number of sectors to be scanned. If only ten bytes are to be scanned, the data area in main storage must contain an additional 260 mask characters completely set to 1 bits.

The data address of the CCW specifies the leftmost main-storage location of the area containing the data to be compared with the data on disk storage. The number in the sector count portion of the CCW (bits 8-15) specifies the number of sectors to be used for the operation. A maximum of one cylinder (100 sectors) can be scanned with one command. Multiple sector scans may start at any sector but are valid only for sequentially numbered sectors in the cylinder. The count area address in the CCW specifies the leftmost main-storage location of the nine-byte count area for the first sector to be scanned.

NOTE: Although the last previous seek operation has specified a head to be selected, final head selection is performed under control of the count area that is used for the scan operation, provided the flag byte is not 0000 0001. The cylinder that is used is determined by the last previous Seek command.

For multiple sector scans the count area is updated between sectors by the storage control. The scan equal operation begins when an equal compare between the count area in main storage and the count area on the disk storage is detected. The operation terminates when the data area on the disk is found, which is equal to the data area in main storage or the number of sectors called for in the operation have been scanned without finding an equal condition. The operation also terminates at the end of any sector in which a data error is detected. The status modifier (bit 9 in the CSW) is set to one to indicate that the scan was successful. In addition, the count area for the sector on which the equal compare occurred, is now located in main storage at the location of the original count area. When the scan operation is unsuccessful (no compare), the count area in main storage contains the count field of the last sector scanned.

Scan High or Equal: The Scan High or Equal command compares a 270-byte area in main storage, with data stored on disk storage. The programmer

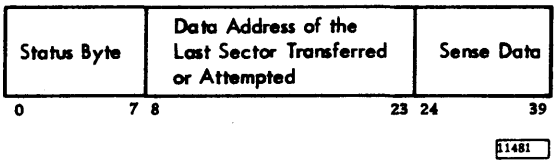
may block the compare of any portion of the 270-byte area in main storage simply by establishing a mask consisting of all 1 bits for the portion to be blocked. The comparison is made only on bytes which are not masked out by 1 bits in main storage. The field length however, must always be 270 bytes in length, regardless of the mask involved or the number of sectors to be scanned. If only ten bytes are to be scanned, the data area in main storage must contain an additional 260 mask characters completely set to 1 bits. The data address of the CCW specifies the leftmost main-storage location of the area containing the data to be compared with the data on disk storage. The number in the sector count portion of the CCW (bits 8-15) specifies the number of sectors to be used for the operation. A maximum of one cylinder (100 sectors) can be scanned with one command. Multiple sector scans may start at any sector but are valid only for sequentially numbered sectors in the cylinder. The count area address in the CCW specifies the left most main-storage location of the nine-byte count area for the first sector to be scanned.

NOTE: Although the last previous seek operation has specified a head to be selected, final head selection is performed under control of the count area that is used for the scan operation, provided the flag byte is not 0000 0001. The cylinder that is used is determined by the last previous Seek command.

For multiple sector scans, the count area is updated between sectors by the storage control. The scan high or equal operation begins when an equal compare between the count area in main storage, and the count area on the disk storage is detected. The operation terminates when a data area on the disk is found, which is higher than or equal to the data area in main storage, or the number of sectors called for in the operation have been scanned without finding a high or an equal condition.

The operation also terminates at the end of any sector in which a data error is detected. The status modifier (bit 9 in the CSW) is set to indicate that the scan was successful. If an equal compare occurs, only the status modifier is set to one. If a high compare occurs, the status modifier (bit 9 in the CSW) and not equal scan (bit 8 in the CSW) are both set to one. In addition, the count area for the sector in which the high or equal compare occurred, is now located in main storage at the location of the original count area. When the scan operation is unsuccessful (no compare), the count area in main storage contains the count field of the last sector scanned.

Sense: A Sense command transfers a five-byte field to main storage which indicates the status of the storage control and the status of the selected disk storage drive at the completion of the previous disk storage operation (other than sense). The data address area of the CCW (bits 16-31) specifies the leftmost main storage location of the five-byte field in which the status information is to be stored. Bits 8-15 and bits 32-47 of the CCW are not used for a sense operation. The status data stored by a sense operation has the following format.



Bit Position	Function
0	Not used - set to zero.
1	Intervention Required - this bit set to 1 indicates that the previous operation could not be executed because the specified disk storage was not up to operating speed or was not turned on.
2	End of Cylinder - this bit set to 1 indicates that the operation was terminated because the end of the cylinder was reached. Bit positions 24-39 contain head number 10 and record number 0.
3	Equipment Check - this bit set to 1 indicates that an equipment malfunction was detected during the previous operation.
4	Data Check - this bit set to 1 indicates that a read error was detected during the previous operation or an unequal compare was detected during the previous verify record operation.
5	Seek Check - this bit set to 1 indicates that the last seek attempted did not come to a normal end. Recovery can be accomplished by doing a recalibrate operation and then repeating the seek attempt.
6	No Record Found - this bit set to 1 indicates that the first sector specified in a data operation cannot be located on the track; or after any sector is transferred during a multiple sector operation, a subsequent sector is not in sequence; or during a read count operation all count areas on the track had errors.
7	Track Condition Check - this bit set to 1 indicates that the flag byte of the count area in main storage is not identical to the flag byte recorded on the track during a data operation. The operation is terminated when this condition is detected. This condition cannot occur on a count and data operation or a read count operation.

Operation	Timing (Average)
Read Data	145 usec + 180 usec + 2.5 (N) ms + 12.5 ms*
Read Count and Data	145 usec + 180 usec + 2.5 (N) ms + 12.5 ms*
Read Count	145 usec + 180 usec + 12.5 ms* + 40 usec + 2.5 (C) ms
Write Data	145 usec + 180 usec + 2.5 (N) ms + 12.5 ms*
Write Count and Data	37.825 ms (for ten sectors)
Verify Count and Data	37.825 ms (for ten sectors)
Verify Data	145 usec + 180 usec + 2.5 (N) ms + 12.5 ms*
Seek	145 usec + 220 usec + Access Motion Time
Recalibrate	145 usec + 100 usec + Access Motion Time
Sense	275 usec
Scan Low or Equal	145 usec + 180 usec + 12.5 ms* + 40 usec + 2.5 (N_1) ms
Scan Equal	145 usec + 180 usec + 12.5 ms* + 40 usec + 2.5 (N_1) ms
Scan High or Equal	145 usec + 180 usec + 12.5 ms* + 40 usec + 2.5 (N_1) ms

N = Number of sectors. Each Sector requires 2.5 ms
* = This factor of 12.5 ms represents the average rotational delay incurred during a large number of operations
C = Number of count areas unsuccessfully attempted
N_1 = Number of sectors unsuccessfully scanned 01198

IBM 2311 Operations Timing Table

Bits 8-23 of the status data stored by a sense operation contain the main-storage address of the last sector to be transferred or attempted. For a single sector operation the data address is always the same as the data address in the CCW which initiated the operation. For multiple sector operations the data address is always the data address for the start of the last sector transferred or attempted. The highest available main-storage location cannot be used for data because the storage control increments the data address in the CCW before it detects the end of sector indication. If the highest available main-storage location is used, a false program check indication may be set in the channel status word.

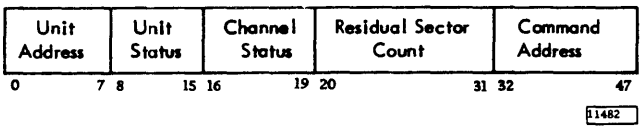
The contents of bit positions 24-39 of the data stored by a sense operation are determined by the type of operation performed immediately prior to the sense operation. The following shows the contents of bit positions 24-39 after each type of operation.

Previous Command	Contents of Bit Positions 24-39
Read, Write, Verify Data (successfully initiated)	Head and record number of the last count area operated upon.
Scan (successfully initiated)	Head and record number of the original sector.
Read, Write, Verify Count and Data (successfully initiated)	Count area address of the last sector transferred or attempted.
Read Count (successfully completed)	Count area address of the last sector transferred or attempted.
Seek, Recalibrate, unsuccessful Read Count, or any operation not initiated because of a busy or not ready condition.	Indeterminate; contents should not be used.

Information stored on a sense operation always applies to the last operation executed. For example, a read operation on disk storage drive number 1, followed by a write on disk storage drive number 2, followed by a sense operation would store the status at the completion of the write operation. The sense information for the read operation would be lost. The unit address portion (bits 40-47) of the XIO command for a sense operation is checked to ensure that it is a valid operation and that it is for a device actually attached to the system. If the unit address is not a valid address (0000 0000) the program check bit in the Channel Status Word (CSW) is set. If the unit address specifies a disk storage drive not attached to the system, the operation is terminated and the condition code in the CSW is set to 11.

Channel Status Word (CSW)

The channel status word is located in main storage, starting at location 156 and is six bytes long (bytes 156-161). The CSW has the following format.



Bits 0-19 of the CSW are replaced by new status information, under the following conditions:

1. At the time a seek or recalibrate operation is initiated or rejected.
2. At the time a data transfer or sense operation is rejected, terminated, or completed.
3. At the time a seek or recalibrate operation is completed and the interrupt is accepted and cleared.

At the time a data transfer (other than sense) is rejected, terminated, or completed, bits 20-47 of the CSW are also stored. Bits 24-31 indicate the residual sector counts, i.e., the number of sectors which were not satisfactorily completed during the data transfer operation. Bits 20-23 are set to zero. Bits 32-47 indicate the address of the CCW of the last command initiated. On a seek, recalibrate, or sense operation, bits 20-31 of the CSW are set to zero. The residual sector count is the actual number of sectors not satisfactorily completed. If the sector count in the CCW was 8 (indicating 8 sectors) and no sectors were successfully completed, the residual sector count is 8. When the CSW is stored, bits 0-7 identify the 2311 Disk Storage for which the CSW applies:

Unit Address: This unit address, in bit positions 0-7, identifies the 2311 Disk Storage for which the CSW applies:

Bit Position	Function
0-5	Not used - set to zero
6	Disk Storage number 2 - this bit set to 1 indicates that 2311 Disk Storage number 2 has been selected.
7	Disk Storage number 1 - this bit set to 1 indicates that 2311 Disk Storage number 1 has been selected.

For all operations other than sense operations, the unit address in the CSW is identical to the unit address which was specified in the B2-D2 fields of the last XIO command. For a sense operation, the unit address in the CSW identifies the last 2311 Disk Storage selected prior to the sense operation.

A unit address which is all zeros is invalid and results in a program check condition.

0000 0001 = drive 1
0000 0010 = drive 2

Unit Status: The unit status, bits 8-15 in the CSW, contains the following information.

Bit Position	Function
8	Not Equal Scan - this bit is set to 1 when a low or high condition, specified by a scan low or equal or scan high or equal respectively, is satisfied.
9	Status Modifier - this bit is set to 1 when any condition specified by a scan operation is satisfied. This bit is set to 1 with bit 11 (busy bit) to indicate control unit busy. A control unit busy condition is indicated at any time a disk storage operation is attempted during the first 15 milliseconds of a previously initiated recalibrate operation.
10	Not used - set to zero.
11 Busy 12 Channel End 13 Device End	Combinations of these 3 bits are used to indicate specific conditions encountered during the operation. Refer to the following list for detailed conditions.
11=0 12=0 13=1	This combination indicates that a program interruption due to the completion or termination of a seek or recalibrate operation has occurred. A seek or recalibrate operation is terminated if the disk storage is turned off.
11=0 12=1 13=0	This combination indicates that a seek or recalibrate operation requiring access motion was successfully initiated.

Bit Position	Function
11=0 12=1 13=1	This combination indicates that a data or sense operation was completed, or that a seek operation which requires no access motion was completed.
11=1 12=0 13=0	This combination indicates that the specified disk storage drive is busy executing a previously initiated seek or recalibrate operation.
11=1 12=0 13=1	This combination indicates that the selected disk storage drive had a seek or recalibrate interruption pending that was masked off. The specified command is not initiated; the pending interrupt is serviced and the request is cleared.
14	Unit Check - this bit is set to 1 to indicate that one of the following conditions exists on the selected disk storage. Manual intervention or programming may be necessary due to: 1. Data Check. 2. No record found. 3. Intervention required. 4. Track condition check. 5. Equipment check. 6. End of cylinder. 7. Seek check. A Sense command can be used to determine which of the above seven conditions caused this bit to be set.
15	Not used - set to 0.

Channel Status: The channel status, bits 16-19 in the CSW, contains the following information:

Bit Position	Function
16	Not used - set to zero
17	Not used - set to zero
18	Not used - set to zero
19	Program Check - this bit is set to one to indicate any of the following conditions: 1. Bit positions 40-47 (unit address) of the number derived from the B2-D2 fields of an XIO instruction contained all zeros. 2. Bit positions 0-7 (command code) of the CCW contained an invalid command. 3. Bit positions 8-15 (sector count) of the CCW were greater than ten for a read count and data operation, or were not equal to ten for a write count and data or a verify operation, or were zeros. 4. Bit Positions 16-31 (data address) of the CCW exceeded the limit of available main storage or referred to the protected first 144 bytes of main storage. 5. Byte 4 of the seek address (cylinder number) in main storage exceeded 202 for a 2311 model 11 or 102 for a 2311 model 12. 6. Byte 6 of the seek address (head number) exceeded nine, or the head number specified in the count area for a data or scan operation exceeded nine. 7. An address encountered during the operation exceeded the limit of available storage. This overflow condition also sets the channel end and device end in the CSW.

CONTROL I/O AND TEST I/O AND BRANCH INSTRUCTIONS

A Control I/O or a Test I/O and Branch instruction with a device address of 8 is treated as a no-operation. A CSW is not stored and the condition code is not affected.

Condition Code

The condition code in the Program Status Word (PSW) is set at the time a data transfer operation is rejected, terminated, or completed, or at the time a seek operation is rejected or initiated. The condition code is also set on a sense operation.

Condition Code Set to 01: The condition code is set to 01 at the time a data transfer or a sense operation is rejected, terminated, or completed, or at the time a seek or recalibrate operation is rejected or initiated to indicate that the CSW was stored.

Condition Code Set to 10: The condition code is set to 10 at the time a data transfer operation (other than sense) is rejected, due to a channel busy condition. Channel busy is the condition existing when time shared System/360 Model 20 input/output operations are in progress. No CSW is stored under this condition.

Condition Code Set to 11: The condition code is set to 11 at the time a data transfer, sense, recalibrate, or seek operation is rejected due to a not operational condition. A not operational condition is defined as one in which the unit address in the XIO command calls for a disk storage address greater than 2, or one in which the addressed disk drive is not attached. No CSW is stored under this condition.

Interrupt

A request for interruption of the System/360 Model 20 program by the storage control can occur at the

completion or termination of the seek or recalibrate operation. An interruption can occur in the 2020 only when the channel mask bit (bit 7 in the PSW) is 1 and after the execution of the current instruction is completed. A burst mode I/O data transfer is the same as a processing operation in this respect. An established priority among requests for interruptions exists. A request for interruption from disk storage on the storage control, remains pending until an interruption due to that request occurs. When a disk storage attached to the System/360 Model 20 causes an interruption, the storage control is identified by device address 8 in bits 8-11 of the old PSW stored in main storage, starting at location 0144. The type of operation or function completed is not identified in bits 12-15 of the old PSW. These bits are set to 0. The disk storage that caused the interruption is identified in bits 0-7 of the CSW.

ERROR CONDITIONS

Error conditions associated with operations controlled by the storage control can be determined by examining one or more of the following indications:

1. Programming error stop.
2. Condition code in the PSW.
3. Channel status word settings.
4. Sense information.

Programming Error Stop

A programming error stop occurs under the following conditions:

1. The direct or effective address derived from the B1-D1 fields of the XIO instruction exceeds the limit of available main storage or refers to the protected 144 bytes of main storage.
2. The number derived from the B2-D2 fields in the XIO instruction contained all zeros.

Condition Code in the PSW

The condition code in the PSW has the following three valid settings:

1. Condition code set to 01. This setting indicates that a CSW was stored and should be examined.

   This setting also indicates that the disk storage specified could be attached to the system and that the operation was attempted with no interference from other System/360 Model 20 time shared input/output operations.
2. Condition code set to 10. This setting indicates that a data transfer operation (other than a sense operation) was rejected by the storage control because a System/360 Model 20 time shared input/output operation was in progress. No CSW is stored for this condition code setting.
3. Condition code set to 11. This setting indicates that the unit address (bit positions 40-47) portion of the XIO command specifies a disk storage numbered higher than 2, which is the maximum number of disk storage drives that can be attached to a System/360 Model 20.

Channel Status Word Settings

A condition code setting of 01 in the PSW indicates that a CSW was stored because of a condition detected during the operation. Examination of the contents of the CSW is a convenient means for the programmer to check for the following conditions:

1. The operation was rejected because the selected disk storage was busy executing a previously initiated seek or recalibrate operation. Bit position 11 (busy) is the only unit status bit set to 1.
2. The operation specified was rejected because the selected disk storage had a seek or recalibrate interruption pending. The interruption was then accepted and cleared. The unit status bit positions 11 (busy) and 13 (device end) are set to 1.
3. A seek or recalibrate operation requiring access motion was initiated. Bit position 12 (channel end) is the only unit status bit set to 1.
4. The data transfer or sense operation was successfully completed or if a seek operation was specified, no access motion was required. Bit positions 12 (channel end) and 13 (device end) in the unit status are set to 1.
5. A seek or recalibrate interruption occurred and was accepted by the storage control. Unit status bit position 13 (device end) is set to 1.
6. A successful equal scan operation is indicated by bit positions 9 (status modifier), 12 (channel end), and 13 (device end) in the unit status being set to 1.
7. A successful high or low scan operation is indicated by bit positions 8 (not equal scan), 9 (status modifier), 12 (channel end), and 13 (device end) in the unit status being set to 1.
8. An operation is terminated by the detection of a program error. Bit position 19 (program check) in the channel status is set to 1.
9. An operation was rejected by the storage control because a previously initiated recalibrate operation is in progress. During the first 15 ms of a recalibrate operation the storage control is busy,

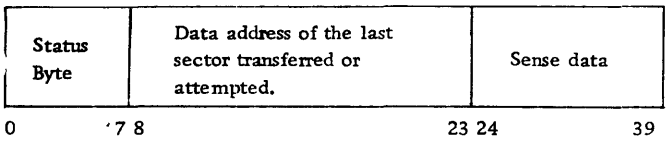
and if an operation is rejected during this 15 ms interval, unit status bit positions 9 (status modifier) and 11 (busy) are both set to 1.

10. An error occurred which prevented the successful completion of the operation. Detailed information about the error condition can be obtained by performing a sense operation. Unit status bit position 14 (unit check) is set to 1; other bit positions may or may not be set to 1.

Sense Information

A sense operation is a convenient means for the programmer to determine what happened during the previous operation to cause an error condition.

A sense operation transfers a five-byte field to main storage to indicate the status of the storage control and the status of the selected disk storage at the completion of the previous disk storage operation (other than sense). The data address area of the CCW, bits 16-31, specifies the leftmost main-storage location of the five-byte field in which the status information is to be stored. Bits 8-15 and bits 32-47 of the CCW are not used for a sense operation. The status data stored by a sense operation has the following format.



Bit Position	Function
0	Not used - set to zero
1	Intervention required
2	End of cylinder
3	Equipment check
4	Data check
5	Seek check
6	No record found
7	Track condition check

Intervention Required and Equipment Check: If the status byte has bit position 1 (intervention required) or bit position 3 (equipment check) set to 1, the program should retry the operation eight to ten times. If the error condition persists, the program should be halted, and the operator should turn off the associated disk storage and then turn it back on to reset any unsafe conditions that might exist. Retry the operation another eight to ten times. If the error condition persists, further operation on this disk storage should not be attempted until the cause of the error has been corrected.

For this type of error, the condition code in the PSW is set to 01 and unit status bit positions 12 (channel end), 13 (device end), and 14 (unit check) in the CSW are set to 1. If a multiple sector operation was in progress when the error condition occurred, any data preceding the address in bit positions 8-23 of the sense data is valid.

Data Check: If the status byte has bit position 4 (data check) set to 1, a data error was detected in data read from disk storage, or during a verify operation, the data in main storage is not identical with the data recorded on disk. For a read operation error, the program should retry the read eight to ten times. If the error persists, an audit trail procedure may be necessary to recover the data.

For a verify operation error, the program should retry the verify eight to ten times. If the error persists, the program should repeat the previous write operation and retry the verify eight to ten more times. If the error persists, the track should be considered defective and flagged as such. (See Data Recovery and Flagging Procedures.)

For a data check, the condition code in the PSW is set to 01 and unit status bit positions 12 (channel end), 13 (device end), and 14 (unit check) in the CSW are set to 1.

If a multiple sector operation was in progress when the error condition occurred, any data preceding the address in bit positions 8-23 of the sense data is valid.

No Record Found: If the status byte has bit position 6 (no record found) set to 1 during a data operation, one of three conditions may exist:

1. The first sector could not be found on the track.
2. On a multiple sector operation, after the first sector has been found, one of the subsequent sectors was not in sequence.
3. On a count and data operation a read or verify error was detected in a count area.

If the first sector could not be found, the residual count in the CSW is the same as the sector count in the CCW that initiated the operation.

The program should retry the operation eight to ten times. If the error persists, the program should do a recalibrate operation, then reseek to the same address and retry the operation eight to ten more times. If the error persists, a read count and data operation should be done and the count area examined to determine if the seek operation was successful. If the seek operation was unsuccessful the cause should be located and corrected.

If the seek was successful, and the count area for the sector is wrong, the track should be rewritten using a write count and data operation. Do a verify operation next to ensure that the track is not defective. If the verify operation is unsuccessful, the track should be considered defective and flagged as such. (See Data Recovery and Flagging Procedures.)

If this type of error occurs after the first sector of a multiple sector operation, the residual count in the CSW is less than the original sector count in the CCW. Bit positions 24-39 of the sense data contain the address of the sector in which the error occurred.

For this type of error, the condition code in the PSW is set to 01 and unit status bit positions 12 (channel end), 13 (device end), and 14 (unit check) in the CSW are set to 1.

Track Condition Check: If the status byte has bit position 7 (track condition check) set to 1, a data operation was attempted but the track condition bits in the flag byte in main storage are not identical to the track condition bits in disk storage. This error could mean that the track is either a defective or an alternate track, and a read count operation should be done to get the alternate track address.

This error does not occur as a result of the condition of the track. This error indicates only that the track condition bits in the flag byte in main storage are not identical to track condition bits recorded in disk storage.

For this type of error the condition code in the PSW is set to 01 and unit status bit positions 12 (channel end), 13 (device end), and 14 (unit check) in the CSW are set to 1.

End of Cylinder: If the status byte has bit position 2 (end of cylinder) set to 1, a multiple sector scan or data operation was attempted with a sector count greater than the available sectors in the cylinder. All sectors within the cylinder were handled successfully. A seek operation is necessary if the programmer wishes to continue processing in another cylinder.

For this type of error, the condition code in the PSW is set to 01 and unit status bit positions 12 (channel end), 13 (device end), and 14 (unit check) in the CSW are set to 1.

Seek Check: If the status byte has bit position 5 (seek check) set to 1, the disk storage did not successfully complete the seek operation. A recalibrate operation followed by another seek operation should correct this condition.

For this type of error the condition code in the PSW is set to 01 and unit status bit position 14 (unit check) in the CSW is set to 1. At the time this condition is detected, the storage control does not indicate a seek check. Seek check is indicated when the next operation is attempted on the same disk storage.

Defective Surfaces

With the high density magnetic recording techniques used in the 2311, minute particles of contamination can cause disk surface damage during the life of the disk pack. While experience with magnetic recording surfaces indicates that surface damage resulting in unreadable areas is a rare occurrence, a means for identifying these defective areas is provided in the flag byte of the count area.

An entire track can be flagged as defective by setting the track condition bits in the flag byte of the count area. There are three possible settings of the track condition bits:

1. Usable original track. Track condition bits are set to 00. In this case, the track address portion of the count area is identical to the actual address of the track in disk storage.

2. Defective original track. Track condition bits are set to 10. In this case, the track address portion of the count area is identical to the actual address of the alternate track. All ten sectors on the track are flagged as defective, and all ten sectors contain the alternate track address in the count area.
3. Usable alternate track. Track condition bits are set to 01. In this case, the track address portion of the count area is identical to the actual address of the original defective track.

Data Recovery and Flagging Procedures

If a track contains a defective area, either during initial formatting of the track or on a subsequent attempt to read or verify data written on the track, the following procedures may be used to recover data, flag the track, and assign an alternate track.

Data Recovery

If the defective track was detected during a verify operation after a write count and data operation, the data to be written should still be available in main storage. Sectors which were written and verified successfully, prior to the sector in which the error occurred, can be recovered by a read operation.

If the defective track was detected during a read operation, the data for the sector in which the error occurred cannot be recovered from disk storage. In this case, data recovery may require the use of an audit trail procedure to reconstruct the data.

If the defect was in the count area, the data may be recovered by using a read count and data operation. If the status byte has bit position 6 (no record found) set to 1 and all other bit positions in the byte set to 0 (after the read count and data operation) the count area is unreliable, but the data area is good. The count area for that sector may be reconstructed, using an audit trail procedure, and the remaining sectors may be recovered by using a read data operation.

Assigning an Alternate Track: The assignment of data tracks and alternate tracks is flexible and the user can allocate data and alternate tracks as needed within the total available. The 2311 model 11 has 203 tracks available; the 2311 model 12 has 103 tracks available. A typical assignment of data tracks for a 2311 model 11 and 2311 model 12 is:

	2311 Model 11	2311 Model 12
Data Cylinder Address	0-199	0-99
Alternate Cylinder Address	200-202	100-102

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Any data track determined to be defective can be assigned an alternate track address. Spare tracks, not already assigned as data or alternate tracks, can be determined by keeping a table of available tracks.

Copying Data On an Alternate Track: The data from the defective track should be set up in main storage with the count area identical to the actual address of the original track. The track condition bits in the associated flag byte should be set to 01. Since heads are selected from the count area in main storage during data operations, care must be taken to ensure that the head address in the count area written on the alternate tracks is identical to the head address in use. Write count and data operations can be used to copy the data onto the alternate track. If the head used for the alternate track is different from the head used for the defective track, the programmer must store the defective track head address in main storage to ensure that the program can resume disk storage operation in the right location.

Flagging a Defective Track

The defective track may be flagged by setting up the count and data areas in main storage to write 270 bytes of zeros for the data area; for the count area in main storage, set the track condition bits in the flag byte to 10 and set in the alternate track address. All of the ten sectors on the track must be written in this format, using a write count and data operation.

Typical Alternate Track Procedure

During normal disk storage operations the track condition bits of the flag byte in main storage should be set to 00 for a usable original track. If the status byte has bit position 7 (track condition check) set to 1 during the operation, the track has been flagged as a defective track. In this case, the programmer should do a read count operation to recover the alternate track address; then do a seek operation to the alternate address derived from the count area of the defective track. The data on the alternate track can now be processed as if it were on the original track.

The track condition bits of the flag byte in main storage must be set to 01 to process the data on an alternate track, and the head address in the count area in main storage should be identical to the head address in use. After processing an alternate track, disk storage operations can continue by doing a seek operation to the next track to be processed.

IBM 1419 MAGNETIC CHARACTER READER

The 1419 Magnetic Character Reader can be attached to a System/360 Model 20 through a Serial Input/Output Channel (SIOC). The 1419 reads into the system the magnetically inscribed information on checks and other banking documents at speeds as high as 1,600 documents per minute. Documents can be sorted into as many as 13 classifications as they are read. All magnetic inscriptions can be checked for validity.

Documents read by the 1419 Magnetic Character Reader may be of intermixed sizes and thicknesses, as typically encountered in check-handling operations. The standard minimum length is six inches; shorter documents, such as the 51-column postal money order, can be read into the System/360 Model 20 at a maximum rate of 1,960 documents per minute. Shorter documents (which may be intermixed with standard-length documents) can be sorted if the optional (no charge) feature for this purpose is installed.

Many special features are available for the 1419, including an endorser that prints a full endorsement on the back of each document at no reduction in operating speed.

Instructions

The 1419 Magnetic Character Reader operates through the Serial I/O Channel (SIOC) of the System/360 Model 20. The SIOC is identified by a device address of 6.

An Engage 1419 instruction must be given to start document feeding. A Read From 1419 instruction notifies the CPU to accept information as it is available from the document. A Select Stacker Pocket instruction must precede the arrival of a document at photocell number 6. A Disengage 1419 instruction stops the flow of documents.

Transfer Instruction (XIO)

OP Code	DA	FS	Function
D0	6	2	Read From 1419

The direct or effective address is derived from the B1-D1 fields of the instruction and specifies the rightmost data location in core storage. Length of the data transferred is derived from the B2-D2 fields of the instruction.

When the Read From 1419 instruction is terminated, the low order byte (residual count) of the field length specification is stored in main-storage location 155.

A Read From 1419 instruction causes a serial transfer of characters from the 1419 to the CPU. The CPU accepts each character as the 1419 makes it available. The CPU is free for other processing during a read operation except for 55 microseconds per character.

The first character or symbol transferred is placed in the rightmost (highest) core-storage position specified by the instruction and subsequent characters enter successively lower core-storage locations.

The read operation is terminated by an end of data signal which occurs when the trailing edge of a document passes the read head (or when a specified character count has been exceeded) whichever occurs first. An end of data signal also occurs as a result of a jam or stop delay during a read operation. Therefore, a separate Read From 1419 instruction is required for each document.

Failure to provide a Read From 1419 instruction before the leading edge of a document is sensed at the read head causes the document to be rejected. An interrupt is requested when a read operation is terminated.

An early interrupt occurs when the leading edge of a document is sensed at Photo Document Sensor 5 (PDS 5) if a read operation is still in progress for that document. This interrupt indicates that approximately six inches of a document have passed the read head, but this does not end the read operation. The early interrupt is used for establishing the stacker pocket destination for the document.

Condition Code Setting

The condition code is set to 00, 01, or 11 at the time the execution of an XIO instruction for the SIOC is completed to indicate that the SIOC is available, working, or not operational.

The transfer of data, as specified in the XIO instruction, is initiated only when the SIOC is in the available state. The SIOC is available when the 1419 is attached, no previous read or write operation is in progress, no read transmission error condition exists, and the 1419 is ready for operation.

The 1419 is ready for operation when a Read From 1419 instruction is issued and no jam or stop delay is present, and at least one of the following conditions exists;

Separator on.
Document between separator and PDS 3.
Document recognized at PDS 4.

The SIOC is working or busy when a previous read or write operation is in progress.

The SIOC is not operational if the I/O device (the 1419) is not attached or is not ready for operation.

Test I/O and Branch Instruction (TIOB)

OP Code	DA	FS	Function
9A	6	1	Document to be read
9A	6	2	Document under read head
9A	6	3	Amount field valid
9A	6	4	Process control field valid
9A	6	5	Account No. field valid
9A	6	6	Transit field valid
9A	6	7	Serial No. field valid
9A	6	8	Auto Select
9A	6	9	Read transmission error
9A	6	A	Jam/sort check

By means of the TIOB instruction, the line defined by the function specification is tested; if the condition indicated by the line exists, the updated instruction address is replaced by the branch address. If the condition does not exist, normal instruction sequencing proceeds with the updated instruction address.

Document to be Read: This indicator is on when there is a document between the separator and the read head. It turns off when a document leaves the read head, but no trailing document is between the separator and the read head. The indicator remains off until another document leaves the separator. The indicator is also turned off by a right or left feed jam.

Document Under the Read Head: This indicator turns on when the leading edge of a document is sensed by photocell 4 (at the read head). It turns off when the trailing edge of the same document passes the read head. It is also turned off when a document jams between the separator and the read head.

Valid Amount Field: This indicator turns on when the amount field has been completely read without errors. The indicator turns off when the leading edge of the next document is sensed at the read head.

The indicator does not turn on if:

1. Any of the characters in the amount field (including the amount-field special symbols) are unreadable.
2. Amount field symbols are missing or out of sequence.
3. The field is missing.
4. The field length is invalid.

Valid Process-Control Field: The indicator turns on when the process-control field has been completely read without errors. It turns off when the leading edge of the next document is sensed at the read head.

The indicator does not turn on if:

1. Any of the characters in the process-control field (including the special symbol) are unreadable.
2. The field is missing.
3. Special symbols are out of sequence or missing.
4. The field length is invalid (fixed-field lengths only).

Valid Account-Number Field: This indicator turns on when the account-number field is read correctly. It turns off when the leading edge of the next document is sensed at the read head.

The indicator does not turn on if:

1. Any of the characters in the account-number field (including the special symbol) are unreadable.
2. Special symbols are missing or out of sequence.
3. The field is missing.
4. The field length is invalid (fixed-lengths only).
5. The self-checking account-number device (special feature) indicates the account number is in error.

Valid Transit-Number Field: This indicator turns on when the transit-number field is read correctly. It turns off when the leading edge of the next document is sensed at the read head.

The indicator does not turn on if:

1. Any of the characters in the transit-number field (including the special symbols) are unreadable.
2. Special symbols (except the dash) are missing or out of sequence.
3. The field is missing.
4. The field length is invalid.

Valid Serial-Number Field: This indicator turns on when the serial-number field is read correctly. It turns off when the leading edge of the next document sensed at the read head.

The indicator does not turn on if:

1. Any of the characters in the serial-number field (including the special symbols) are unreadable.
2. Special symbols (except the dash) are missing or out of sequence.
3. The field is missing.

Auto Select: The Auto Select indicator is off if a Stacker Selection command can be executed correctly. The auto select bit is set on when a document is not acceptable due to spacing (too close together), a late read, or extreme mutilation.

The auto select bit is also turned on when a document reaches the select station prior to the issuing of a Stacker Select command. A good programming practice is to test the setting of the auto select bit immediately prior to the issuing of a Stacker Select command. After the Stacker Select command is accepted, the auto select bit is turned off, thus preventing two Stacker Select commands from being issued for the same document.

All auto select documents are routed to the reject pocket.

Read Transmission Error: This indicator is turned on when the data transmitted from the 1419 to the CPU has incorrect parity. The indicator is reset by the Test instruction.

Jam or Sort Check: This check bit (and its associated indicator light) indicates a right or left feed jam or a sort check condition. The bit remains on until the operator clears the jam and resets the condition using the Stop/Restore key.

Control I/O Instructions (CIO)

OP Code	DA	FS	DS	Function
9B	6	0	0	No operation
9B	6	0	1	Select or Light Pocket A
9B	6	0	2	Select or Light Pocket B
9B	6	0	3	Select or Light Pocket 0
9B	6	0	4	Select or Light Pocket 1
9B	6	0	5	Select or Light Pocket 2
9B	6	0	6	Select or Light Pocket 3
9B	6	0	7	Select or Light Pocket 4
9B	6	0	8	Select or Light Pocket 5
9B	6	0	9	Select or Light Pocket 6
9B	6	0	A	Select or Light Pocket 7
9B	6	0	B	Select or Light Pocket 8
9B	6	0	C	Select or Light Pocket 9
9B	6	0	D	Select Reject or Batch Number Update
9B	6	0	E	Pocket Light and/or Batch Number Control
9B	6	0	F	No operation
9B	6	1	0	No operation
9B	6	1	1	Engage 1419
9B	6	1	2	Disengage 1419

The CPU sends control information on the line specified by the function specification and detail specification fields of the control instruction.

NOTE: A Disengage command given when the separator is off is effective immediately and it terminates the previous Engage instruction.

Program Sort Mode: The purpose of this mode is to provide CPU control of pocket selection and to permit transmission of data from documents to the CPU.

1. An Engage 1419 instruction starts document feeding.
2. A Disengage 1419 instruction stops the flow of documents.
3. A read from 1419 prepares the CPU for accepting information as it becomes available from each document.
4. A Select Stacker instruction should precede the arrival of each document at PDS6.
5. Information on validity of transmitted data and end of document is presented to the CPU as soon as available.
6. The Read Field keys on the 1419 determine which fields of data are to be transmitted.

Pocket Selection Time

The program must make a stacker selection before the document reaches the select station. The pocket selection must not be executed until it is known that the document is no longer under the read head. There are 23.62 (-0.95, + 0.0) milliseconds available between the time the early interrupt is generated and the latest point at which a Stacker Selection command must be given. If a pocket decision is not made before the document reaches the select station, the document is rejected and the Auto-Select indicator is turned on.

Program Control for Pocket Lights: When the Program Control for Pocket Lights special feature is installed, it is possible to light the pocket lights (A through 9) in the 1419 with the use of program instructions. The correct sequence of operations is as follows:

1. Disengage.
2. Handle follow-up items in normal manner.
3. Issue Pocket Light and/or Batch Number Control command.
4. Issue Stacker Select commands for the appropriate pocket lights.
5. Engage to restart document feeding.

NOTE: During program testing, avoid unnecessary stops. Do not issue CIO instructions for the Program Control for Pocket Lights (PCPL) special feature when it is not installed on a 1419 with Batch Numbering special feature. If the PCPL feature is inadvertently instructed, document feeding is stopped; however, the motor continues to run. To resume normal operation, press the 1419 Stop key, turn the power off and then back on, and press the 1419 Start key. No error condition should be indicated.

Batch Numbering: The installation of this special feature allows documents to be numbered on the reverse side for audit purposes. This number may be advanced by one under program control. The same timing restrictions that apply to proper stacker selection apply to batch number updating. When the batch number update is issued in conjunction with the stacker select for a given document, the updated number is printed on the document. Two CIO instructions are required for the operation as follows:

1. The Pocket Light and/or Batch Number control instruction which prepares the numbering device to accept the updating instruction.
2. The Reject and/or Batch Number updating instruction which advances the batch number.

NOTE: these instructions must be given in the sequence shown in order for the 1419 to properly recognize the dual functions of these instructions.

Document feeding is suspended if more than one advance sequence is given within three seconds. Feeding is suspended, resulting in a reduction of throughput, for the remainder of the three-second interval. The 1419 resumes feeding automatically, unless a Disengage 1419 instruction is issued. An advance check stop occurs if the Advance Check On switch is on and the batch numbering device has failed to respond to the updating instruction.

System Stops

1. System stops should be initiated by depressing the 1419 Stop/Restore key prior to stopping the CPU.
2. When the system is stopped by any other key or by a system error stop, document feeding is terminated. Documents in flight that have not been stacker selected are directed to the reject pocket.
3. Jams prior to the read head do not affect previously read documents.
4. For jams after the read head, the operator must examine the print-out and properly distribute any items which stop prior to or in the selector unit, based on the print-out.
5. Sort check stops are caused by a malfunction in the equipment and cannot be caused by the program. This stop occurs if no stacker has been activated for a document that reaches the select station, or if more than one stacker has been activated for a document at the select station. When a sort check stop occurs, the 1419 stops feeding and the remaining documents in process (one to five may be in the feed) are read, stacker selected, and processed. The 1419 Sort Check indicator and the Stop/Restore key are turned on. The Jam/Sort Check indicator bit is turned on also.

   When a sort check occurs, the error document is found in the reject pocket.

   The operator must examine the print-out of the items and properly distribute the item involved.

   The 1419 Stop/Restore key must be depressed to reset the sort check condition.
6. End-of-Transport Stop: An End-of-Transport Sense switch stops document feeding if a document in the transport fails to enter a pocket. When an end-of-transport stop occurs, both the 1419 Left Feed light and the Ready light come on.

   The operator removes the document and determines its proper distribution in the manner prescribed by the operation currently in progress.

   The Left Feed light is reset by depressing the Stop/Restore key.
7. Film Stop: The write head and the read head are each protected from excessive wear and damage by thin metal tapes called head-film tapes. When either film tape breaks, or when its supply runs out, the Film light turns on and an immediate stop occurs.

The operator corrects the film stop condition and follows the jam error recovery procedures.

8. Non-Error Stops: If the following 1419 stops occur, the operator should inspect the machine and take corrective action.
   a. Full pocket stop.
   b. Empty feed hopper stop.
   c. Hopper feed failure stop.
   d. Operator stops.
9. Unreadable Documents: If for any reason the 1419 cannot read and transmit any selected information correctly, the indicators provided can be tested to determine the reason.
10. Endorse Stop Condition: This condition can occur only when the endorser feature (optional) is installed and the customer has the Endorse Checking switch turned on.

    An endorse stop condition causes the 1419 to stop with the Endorse Stop indicator and the Stop/Restore key lighted.

    The operator must examine the last few documents processed for proper endorsements and handle them in a manner prescribed by the operation currently in progress.

    The 1419 Stop/Restore key must be pressed to reset the endorse stop condition.
11. Advance Check Stop: This condition can occur only when the Batch Numbering special feature is installed and the Advance Check switch is in the On position. The advance check stop condition causes the 1419 to stop feeding with the Advance Check indicator and the Stop/Restore key lighted. This stop is caused by a failure to advance the number device.

COMMUNICATIONS ADAPTER

INTRODUCTION

The Communications Adapter (CA) special feature enables the System/360 Model 20 processor to function as a remote terminal capable of point-to-point transmission under stored-program control. The device allows communication with all standard synchronous transmitter receiver units such as the IBM 1009 Data Transmission Unit, the IBM 7701 and 7702 Magnetic Tape Transmission Terminals, the IBM 1013 Card Transmission Terminal as well as the IBM 7710 and 7711 Data Communication Units.

The System/360 Model 20 with the Communications Adapter special feature is fully compatible with the synchronous transmitter receiver devices used with System/360 equipment and is the primary means of data interchange between the System/360 Model 20 and another System/360 Model 20, or System/360 Models 30, 40 etc. equipped with an IBM 2701 with a synchronous data adapter type 1.

Data transmission can only be between two stations at a time (point-to-point). Stations can be connected either by permanent private or leased lines or by common carrier (dial) network. The Communications Adapter operates in half duplex mode on either two- or four-wire telephone lines. Four-wire operation results in a shorter line turn around time.

The Communications Adapter is programmed in much the same way as any other I/O device used with the System/360 Model 20. Transmission operations are time-shared with other primary input/output and processing operations. The communications adapter also uses the System/360 Model 20 interrupt feature to signal the CPU that an instruction has been completed or that acknowledgment for a transmitted record has been received. The transmission time rates depend on the line facilities available and on the type of modem used. Up to 600 bytes per second (4800 baud) can be transmitted or received. Data is transmitted in the 4-of-8 code and it must therefore be translated from or into EBCDIC. Either the Translate instruction or an IBM utility program can be used for this translation. Transfer instructions must be issued for each record transmitted. The instruction specifies the direction of transfer, the length of the assigned record area in main storage, and the leftmost address of the record in storage. Keys, lights, and switches are located on an operator panel adjacent to the CPU console.

CA INSTRUCTIONS

The following instructions are used to program the CA:

Type	Op Code	DA	FS
CIO	9B	5	1 Set Transmit Mode CIO
CIO	9B	5	0 Set Receive Mode
CIO	9B	5	2 Send EOT
CIO	9B	5	3 Inhibit Audible Alarm
XIO	D0	5	4 Transmit
XIO	D0	5	2 Receive
TIOB	9A	5	1 Test for current message in error
TIOB	9A	5	0 Test for CA busy
TIOB	9A	5	5 Test for EOT received
TIOB	9A	5	4 Test and Branch on BCD

Summary of TIOB Instructions

The use of the TIOB instructions is summarized in the following text and later under "Operating Principle" and "Transmit Operations".

Test for Current Message in Error

An error condition in the CA indicates that a faulty record has been either sent or received. However, the error condition does not stop the CA or render it non-operational; the only effect is that the faulty data is not set into core storage. To facilitate immediate retransmission, the error condition is testable. If the error condition is found to be on, the program branches to a subroutine that initiates retransmission; if the error condition is off, the program continues with the next sequential instruction (the address of this instruction is contained in the PSW).

If the programmer intends to check each message, he must use the Test for Current Message in Error instruction at interrupt time. If the CA is transmitting (send run status), the error condition means that a non-4-of-8 code was sent out. If the CA is receiving (receive run status), the error condition means that one of the following faults has occurred:

1. A non-4-of-8-code character was received
2. The odd/even counts do not match
3. The received record exceeded the length that was specified in the Receive instruction
4. The incoming character was not serviced by the micro-program
5. The longitudinal redundancy check shows an error.

If the same faulty message is transmitted (or received) two more times, the CA stops and the ready status is lost. At that time, the check lights indicate the type of error for the last transmission (or reception). The status of the CA (send or receive) is not affected.

The error condition is reset with the next XIO instruction (Transmit or Receive) that is issued, regardless of whether the error is corrected or not. The error condition is also reset by the next error-free message that is received.

Test for CA Busy

The busy condition is testable so that the program may avoid issuing one instruction while another is still in progress. The CA becomes busy when an instruction is issued and it remains busy until that instruction has ended. When the busy condition is found to be on, the program branches to a subroutine; if the busy condition is off, the program continues with the next sequential instruction.

When either of the Set Mode (CIO) instructions is issued, or when the Transmit (XIO) instruction is issued, the CA remains busy until a reply from the other station is received. However, character phase (synchronization) must be established between both stations before a reply can be received. Thus it is possible for the CA to remain busy indefinitely because of loss of character phase. The CA remains busy indefinitely also when the other station has received the same message three times in error and has, therefore, a check stop condition.

When a Receive (XIO) instruction is issued, the CA remains busy until either the End of Transmittal Record (EOTR) signal or an acknowledge signal is received from the transmitting station. In all cases, the busy condition is reset at interrupt time.

Note, however, the following exception: When the Set Receive Mode instruction is issued while the Auto Answer/Disconnect switch is in the auto answer position, the CA gets no busy condition; the program can then proceed with the next instruction. The Test on CA Busy instruction has a different function to that described previously when the switch is in the auto answer position; the instruction disables the Auto Answer/Disconnect feature (when issued) and no branch occurs.

Test for EOT Received

The End of Transmission (EOT) condition is testable so that the program can take appropriate action when an EOT signal is received. The Test for EOT Received instruction should be part of the interrupt routine because an EOT signal can be expected at any time and the interrupt time is the earliest possible moment at which the reply from the other station can be tested. When an EOT signal is received, the run status of the CA (either send or receive) is dropped and the program must change its normal course; for example, it must restore the run status if continued transmission (or reception) is desired. The EOT condition indicates that the other station has terminated the data exchange. If one station sends the EOT signal, the other station responds with EOT automatically and, therefore, the EOT condition can also indicate a positive acknowledgement.

When the EOT condition is found to be on, the program branches to a subroutine; when the EOT condition is off, the program continues with the next sequential instruction. The EOT condition is reset when the next Set Mode instruction is issued.

Test and Branch on BCD

To allow the CA to communicate with Synchronous Transmitter/Receiver (STR) devices that use only 63 characters (such as the IBM 1030 Data Collection System), the Binary/BCD switch must be in the BCD position. When the CA is transmitting data to such a device, the EBCDIC codes 0100 0000 (space) and 0111 1010 (colon) must both be translated into the same 4-of-8 code, that is, code 0842; when the CA is receiving data from an STR device, the 4-of-8 code NXOR is recognized as invalid (data check) and code 0842 must be translated into EBCDIC code 0100 0000 (space). In this way, the 64- and 63-character sets are made compatible.

The translating program caters for these deviations from the normal one-for-one translating pattern by using the Test and Branch on BCD instruction to find out whether the Binary/BCD switch is in the BCD position. If the switch is so, the translating program branches to a routine which translates the codes "colon" and "space" as described.

Operating Principle

To explain the basic operating principle an inquiry/answer routine is described. One CA is termed "local", another "remote", and automatically produced control signals are denoted "auto" in this example.

Description: When line connection is established between two CAs, both devices send idle characters (auto) for the purpose of obtaining synchronization. The local program issues a Set Transmit Mode (CIO) instruction to get the local CA into send run status. Send run status is only obtained when synchronization is established (indicated by the Character Phase light).

Meanwhile, the remote program has issued a Set Receive Mode (CIO) instruction to get the remote station into receive run status. The receive run status can also only be obtained when synchronism exists. Therefore, the Set Mode instructions can be issued either before or after synchronization because they are only completed if and when synchronization exists.

When the local CA is in send run status, an inquiry signal (auto) goes to the remote station. This inquiry signal initiates an interrupt in the remote station.

The remote station subsequently issues a Receive (XIO) instruction which causes the acknowledge 2 (ACK 2) signal (auto) to be sent back. The ACK 2 signal represents the answer to the inquiry and it initiates an interrupt in the local CA.

The local program then issues a Transmit (XIO) instruction which causes a start of record 1 (SOR 1) signal (auto) to go to the remote station. SOR 1 is immediately followed by data. The end of the data record is marked by an end of transmittal record (EOTR) signal which contains the Longitudinal Redundancy Check (LRC) character (auto).

The reception of the EOTR causes interrupt in the remote CA. The remote program then issues another Receive (XIO) instruction which causes the acknowledge 1 signal (auto) to be sent back as a reply if the record was received correctly. Otherwise, an error signal is sent.

Reception of ACK 1 causes an interrupt in the local CA and thus either a new Transmit (XIO) or a Send End of Transmission (CIO) instruction may be issued. If EOT is received at the remote CA, the remote CA answers also with EOT and that ends all transmissions. The automatic signals that precede each record alternate with each transmission, that is, the first record is preceded by SOR 1, the next by SOR 2, the following by SOR 1 again and so on. The acknowledgement alternates correspondingly with ACK 1, ACK 2, ACK 1. Since both stations keep track of this odd/even count no record can be "lost" unnoticed. The control signals (SOR 1, ACK 1, EOTR etc.) are not transferred to the main storage.

Transmit Operations

Set Transmit Mode Instruction (CIO)

The CA must be in send run status to be able to transmit. To get it into send run status, the Set Transmit Mode instruction must be issued. Normally this instruction is used only once per transmittal batch. An inquiry signal is sent out to the remote terminal and the instruction can be completed only when the ACK 2 signal is received. When this signal is received, the CA is in the send run state and interrupt is requested.

The Set Transmit Mode instruction can be issued before or after synchronization (character phase) is established, however, the instruction can only be processed when synchronization exists. Synchronization is indicated by the turned on Character Phase light (not by interrupt). The CA busy condition is turned on when the instruction is started and it is turned off upon completion.

Transmit Instruction (XIO)

The interrupt after the Set Transmit Mode instruction indicates to the program that now the transmit instruc-

tion can be issued. All odd numbered records are automatically preceded by the SOR 1 signal and all even numbered records are preceded by SOR 2. After the execution of the Transmit instruction has been initiated, the CA busy condition is turned on and it stays on until the record has been transmitted and a reply (ACK 1, ACK 2) has been received at the local CA.

When a reply is received, interrupt is requested. At interrupt time, the CA error condition and the EOT condition should be tested to find out what type of reply has been received. The conditions can be tested by the respective TIOB instructions. If none of these conditions exist, the last message was received free of errors at the remote station and therefore the program can issue the next Transmit instruction, or the End of Transmission instruction. One of these instructions must be issued within 3 seconds or a processor time out occurs.

If the error bit is on, the CA retains the send run status and the previous record can be transmitted again by issuing the previous Transmit instruction. It is possible that the remote station operator has stopped his CA and pressed the EOT-key. In that

case the EOT bit is on and the local CA is out of send run status. To resume transmitting, the program must issue Set Transmit Mode again. The Set Mode instruction resets the EOT condition. Similarly, the error condition is reset by the next Transmit instruction.

Send EOT Instruction (CIO)

The Send EOT instruction is used to indicate the end of the transmission of a single batch of messages (records).

The local CA must be in send run to be able to transmit the EOT signal.

The CA busy condition is turned on when the instruction is executed and it stays on until an EOT signal is received in response.

When it is received, the local CA drops out of send run and an interrupt is requested.

At interrupt time, the EOT and the error condition should be tested by the respective Test I/O and Branch instruction.

A turned on EOT condition confirms the correct reception of the EOT signal at the remote station.

If the error condition is on, the send EOT instruction must be issued again because the previous was not received correctly.

Receive Operations

Set Receive Mode Instruction (CIO)

The CA must be in receive run status to be able to receive.

To get into the receive run condition, the Set Receive Mode instruction must be issued.

The instruction can be issued before or after synchronization is established but it can be processed only when synchronization (character phase) exists.

The Set Receive Mode instruction is completed when an inquiry signal is received. When the inquiry signal is received, the CA is in receive run status and interrupt is requested.

Receive Instruction (XIO)

The interrupt, caused by the reception of an inquiry signal, informs the program that now a Receive instruction can be issued. This Receive instruction automatically sends an ACK 2 signal to the inquiring station. The CA busy condition is turned on when the Receive instruction is started and it stays on until the instruction is completed. The instruction is completed when the End of Transmittal Record (EOTR) signal is received. This EOTR signal is sent automatically when the field length counter in the transmitting station goes to zero.

When the EOTR signal is received, interrupt is requested. In the interrupt program the Error as well as the EOT condition should be tested. If none of these conditions are on, the record was received correctly and the program can proceed with the data translation. When the received data has been processed, a Receive instruction must be issued to send back the acknowledgement which the transmitting station is expecting. If the received record was odd numbered (the first, third, fifth etc.) the ACK 1 signal is sent back; otherwise, it is the ACK 2 signal.

If the EOT condition is on, an EOT signal was received and therefore the receive run status is dropped. However, an EOT signal is sent back automatically as acknowledgement.

If the error condition is found to be on, a faulty record was received. The receiving station keeps the receive run status when the error bit is on. Next, a Receive instruction must be issued to send back the expected acknowledgement. The acknowledgement (in that case) is an Error signal which informs the transmitting station that a repeat of the previous record is expected.

Error Conditions	Detected by
• Invalid Character Transmitted (non - 4 of 8 - character)	Transmitting CA
• Invalid Character Received (non - 4 of 8 - character)	Receiving CA
• Lost Record (odd/even counts don't match)	Receiving CA
• Wrong Length Record (more characters were received than specified in the Receive instruction)	Receiving CA
• Overrun (character was not serviced)	Receiving CA
• LRC Error (longitudinal redundancy check error)	Receiving CA

If the error occurs within the transmitting station, an error counter is set to one.

If the program repeats that same faulty transmission two more times (the error counter is at 3), the transmitting station stops with the Check Stop light and the alarm on but it keeps its run status. The ready status is lost.

When the same message has been received in error three times in succession, the error counter is at 3 and a check stop condition occurs. The Check Stop light and a combination of other check lights is on as well as the alarm. The ready status is lost, however, the run status is retained.

When the receiving station has a check stop condition (due to faulty transmission lines etc.), the transmitting station remains busy if the fault occurred somewhere outside the transmitter.

Programming Errors

The CA instructions are subject to the normal restrictions, that is, addresses that are derived from the B/D fields must not refer to the protected area in main storage (0-143), or exceed storage capacity. No instruction part may be located in the last main-storage position. Either the B-field of an instruction or the D-field can be zero but not both. Violation of these rules leads to a CPU stop.

The CA instructions must be issued in the correct sequence and at the correct time. When a sequence error occurs, the CPU is stopped and the CA Interlock light, the audible alarm and the error number 0110 in data register I is on. The error number identifies the CA. An interlock is caused by:

- Failure to issue Set Transmit Mode command prior to the first Transmit instruction.
- Failure to issue Set Receive Mode command prior to the first Receive instruction.
- Issuing a Set Mode instruction when the CA is in a run status.
- Issuing a Set Mode instruction while a message is still being received, or transmitted.

Other Errors: When a CA instruction is issued and the CA-Start key has not been pressed, no operation occurs and the alarm is sounded due to a not operational condition. When the CE-switches are not in the normal position, the audible alarm is sounded and data errors are incurred. When the Binary/BCD switch is not set to the mode in which the other terminal transmits, errors can occur. An instruction causes an error if the previous instruction resulted in a storage wrap-around.

NOTE: The program may neglect the testing of the error bit after a record has been received. However, it must be understood that only the "good" portion of a record is transferred to main storage. Since the CA keeps its run status when the error bit is on, a new instruction can be issued and that will reset the error bit. To avoid a processor time out condition, an instruction must be issued within three seconds after acknowledgement.

Condition Code

Prior to the execution of any CA instruction the condition of the CA is tested. If the CA is available, i.e., ready and not busy, the condition code is set to 00 and the instruction is executed. If the CA is busy (processing a previously issued instruction), it is considered to be not operational and the condition code is set to 11. The CA is also not operational when the CA-Start key was not pressed, when the operation switch is in the Off position, or when the data set or modem is not on. In that case no operation occurs and the audible alarm is sounded.

Audible Alarm

The purpose of the audible alarm is to notify the operator of conditions that require his attention. The alarm can be silenced by pressing the CA-Stop key. The ready status is then lost. The following conditions sound the alarm:

- CA programming error stop condition of the CPU (such as B/D-field of the CA instruction all ze[illegible], addressing the protected area etc.).
- CA check stop condition (three faulty messages transmitted or received).
- More than three seconds interval between instructions (processor time out).

  This alarm condition can be suppressed by the Inhibit Alarm instruction.
- CPU Process Check (indicates an error, such as faulty parity etc. within the CPU).
- Received EOT signal.
- Received TEL signal.
- CA in run status but character phase (synchronization) is lost. Alarm sounds until synchronization is obtained or until the CA-Stop key is pressed.
- CA not ready when any instruction that requires data transmission over the lines is issued.

NOTE: When the alarm is sounded the ready status lost.

An exception is the processor time out condition which retains the ready status. The ready status is restored and the check lights are reset by pressing the CA-Start key.

Inhibit Audible Alarm (CIO)

The Inhibit Audible Alarm instruction suppresses the automatic alarm, which normally occurs three seconds after the completion of a CA operation if another is not initiated within that interval. This suppression is cancelled when the next Receive Record, Transmit Record, or Send EOT instruction is issued.

The instruction does not silence the audible alarm under any manually-resettable error conditions, or during an auto answer disconnect cycle. The execution of this instruction does not cause an interrupt and it does not turn off the busy condition.

Check Lights

Check Light Interpretation

Interlock Light	Check Stop Light	Data Light	Processor Light	Record Light	Interpretation
	X	X			Invalid character transmitted to remote terminal.
		X			Invalid character received in message.
				X	Incorrect longit. Redundancy check comparison
		X	X	X	Overrun of main storage area for incoming data.
		X	X		Overrun of received character (char. not serviced).
	X	X		X	Message Parity (Start of Record signal fails to match odd/even count).
X			X		Previous Transmit Instruction caused Storage Wrap-Around

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Interlock Light

The Interlock light indicates a CA programming error stop. When a program error stop has occurred, the display lights of data register U and L (on the CPU console) show the Op code and the display lights E, S, T, R show the address of the CA instruction in which the error has occurred. Data register 1 displays the error number 0110 to identify the stop as a CA-program error.

Processor Check Light

NOTE: This light is not to be confused with the Process Check light on the CPU. The processor check condition has no effect on the operation of the CPU.

A processor check occurs under the following conditions:

- When the CA has received a message and is prepared to send a reply, it initiates an interrupt. If after three seconds (processor timeout) the program has not come up with a Receive instruction (which constitutes the reply), the Processor Check light is turned on.
- The same condition arises when the CA has transmitted a message and received a reply upon which it initiates an interrupt. If after three seconds the program has failed to respond with a Transmit instruction, the Processor Check light is turned on.

In addition, the audible alarm is normally turned on. If the Inhibit Audible Alarm instruction is executed before the processor check condition signal drops, the audible alarm is suppressed. However, as soon as the processor check signal drops, the Processor Check light is turned on. The CA does not loose its ready status when a processor check occurs.

The Processor Check light is turned off only when the required program instruction (Receive, or Transmit) is executed.

Data Light/Record Light

These two lights are used in combination with the other lights to distinguish the various errors from each other.

Check Stop Light

During transmissions, the validity of all messages is constantly being monitored. An error count of 3 messages turns on the Check Stop light and the audible alarm while the start latch is being turned off. (Ready goes off.)

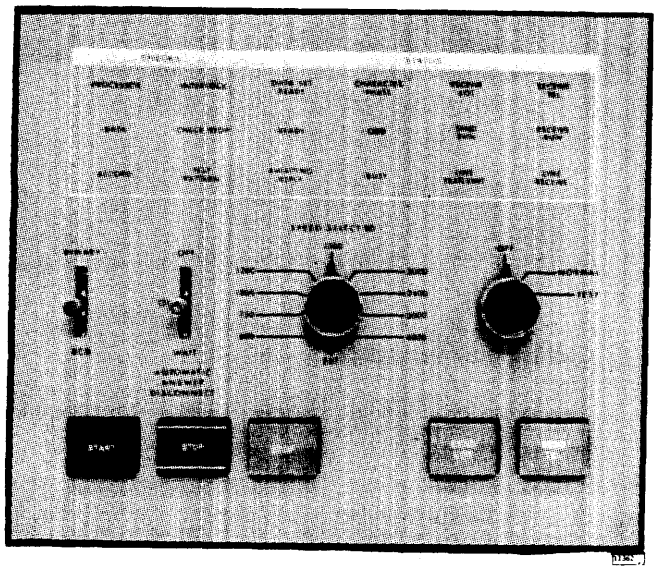
The audible alarm can be silenced by operating the Stop key. Pressing the Start key will turn off the Check Stop light and reset the error counter to zero. Reception of a good message has the same effect, i.e., the ready status is restored. Since the CA can attempt three repetitions of the bad message before it turns on the Check Stop light, this light in combination

with the Data, Processor, or Record lights indicates the type of error for the third attempt.

Test Pattern Light

Indicates that a continuous sequence of control leader signals from the remote terminal has been received.

Status Indicators



Data Set Ready

Indicates that power is on in the data set, the line is connected, and the switches are not in Test position.

Ready

Indicates that power is on in the System/360 Model 20 CPU, the CA CE switches are in the normal operating position, the data set is ready (not required for a Set Receive Mode instruction), and that the CA Start key has been operated.

The CA Ready indicator is turned off by any of the following:

- CA Stop Key. Any operation that is in progress when the stop key is pressed continues to completion.
- CA Check stop.
- Received TEL signal. (The alarm is sounded.)

Awaiting Reply

Indicates that the CA has transmitted an EOTR sig and is waiting for a reply from the receiver.

Character Phase

Indicates that synchronism with the remote station, a prerequisite for all operations, has been achieved. The CA attempts to achieve character phase when system power is turned on if the CA Operational Switch is in the Normal position. Character Phase is achieved when the data set is ready.

Busy

Indicates that an operation which causes data exchange over the line is in progress.

Odd

Indicates the odd/even count of records received or transmitted; it provides the primary method of checking for the loss of a complete record.

Receive EOT

Indicates that an EOT signal originated remotely or a remote reply to a locally originated EOT signal been received. With the Auto Answer Disconnect switch on, the line is disconnected 30 seconds after this light comes on unless the program continues the operation before this time has elapsed. The alarm is sounded when an EOT signal is received.

Receive TEL

Indicates that a telephone (TEL) signal from a remote station or a remote reply to a TEL signal (originated at the CA) has been received. This means that one operator wants to get into voice communication with the other operator. All operations are halted and the ready status is lost when the Receive TEL light is on. The audible alarm is sounded.

Send Run

Indicates that the CA is set as a transmitting terminal.

Receive Run

Indicates that the CA is set as a receiving terminal.

Line Transmit and Line Receive

Indicate that data or control characters are actually on the line.

Stop

Indicates that the CA is not in a ready status.

Keys and Switches

Operation Switch

A rotary switch with three positions, NORMAL, OFF, and TEST. NORMAL and OFF are the "in use/out of use" setting for the CA. In Test position, a continuous sequence of control leader signals is transmitted. The CA can be reset by turning this switch to Off and back to ON. This also silences the alarm.

Start Key

Used to place the CA in a ready status and under certain conditions to turn off the audible alarm.

Stop Key

The Stop key is used to remove the CA from the ready status and under certain conditions it also silences the audible alarm. If the Stop key is operated while the CA is in the process of transmitting or receiving a message, the transmission is allowed to continue to completion. However, the CA does not send a reply in response to the last message and it does not start a new message; the CA keeps its run condition.

After the Stop key has been operated, the CA cannot be automatically disconnected. This allows check stop analysis or other manual interventions, such as changing programs etc.

Speed Select Switch

This switch determines the transmission rate. It must be set to a speed which is agreeable to the line facilities that are available. The speed ratings are calibrated in terms of baud.

Baud Rate	Characters Per Second
600	75
750	93.75
1000	125
1200	150
1500	187.5
2000	250
2400	300

The EXT position must be selected if a data set with internal clock is to be used.

NOTE: Although the CA is capable of receiving and transmitting at a rate of 4,800 Baud, i.e., 600 characters/second, the speeds above 300 char/sec can at present not be utilized due to limitations on available common carrier line facilities.

Auto Answer/Disconnect Switch

Enables the Auto Answer/Disconnect special feature.

Binary/BCD Switch

Setting determines the number of valid 4-of-8 code combinations for transmission or reception and the performance of intermediate Longitudinal Redundancy Checks (LRC).

In the Binary position, 64 code combinations are valid and no intermediate LRC is performed.

In the BCD position, 63 code combinations are valid for reception; code ROXN is invalid and code 2480 is decoded as "space". Intermediate LRC is performed after line codes 148N or 280N. For transmission, both codes ROXN and 2480 are encoded as 2480.

Refer to the Tables in the Appendix for code conversion. The purpose of the BCD mode is to avoid as much line turn around time as possible. This is accomplished by sending as long a record as possible. The intermediate LRCs are transmitted to allow the program on the receiving end to use portions of a long record while the transmission is still in progress. Any portion that checks out as valid can thus be processed.

Send EOT Key

Permits the operator to manually initiate transmission of an EOT signal. This function is independent of the run condition and is operative when the CA is ready but not busy. In normal operation the program terminates the transmission by using the send EOT instruction. In certain cases an operator may wish to initiate the same function manually. If due to the program, the not busy periods between CA instructions are very short, it is advisable that the operator first press the CPU-Stop key and then the EOT key to get the signal through. However, it must be understood that the transmitting CA stays in the run condition and does not get an interrupt when the EOT response from the receiving station is received.

Send TEL Key

When operated, originates a TEL signal to inform the remote operator that verbal communication is requested. This signal is returned automatically to the originating CA; the returned signal turns on the TEL indicator.

Reset

The CA can be reset by turning the Operation switch to the Off position. The CA is also reset when the CPU-Reset key is pressed. Otherwise the execution of the Set Receive Mode or Set Transmit Mode instructions establishes all necessary originating conditions in the CA.

Code Translation

The 4-of-8 code is translated to the internal machine code (the EBCDIC in the System/360 Model 20) by means of the IBM program "Communications Adapter Input/Output Control System (CIOCS)." This macro routine is an IBM designed and tested program which relieves the customer of the translation task. The CPU presents the translated character to the CA for transmission and the CA checks the character for 4-of-8 validity. During reception, the reverse operation takes place.

Auto Answer/Disconnect Operation

This feature is used for three different purposes, for automatically answering an incoming call (auto answer), for automatically disconnecting the line 30 seconds after transmissions are ended (auto disconnect), and for keeping the CPU in a wait state allowing processing only after a call has come in (wait).

Auto Answer

The auto answer operation is enabled by the program when the Auto Answer Disconnect switch is in the On position and a Set Receive Mode instruction is issued. The program can continue with the next instruction immediately since the CA is not busy although the Set Receive Mode instruction has not been completed.

When a call comes in, the data set answers automatically and completes the connection. The CA then attempts to obtain synchronization for 30 seconds. If synchronization is not obtained within that time, the data set disconnects the line and the alarm is sounded. Interrupt is not requested after disconnection. When synchronization is established, the Set Receive Mode instruction is completed and interrupt is requested.

After the program has enabled the auto answer feature by issuing a Set Receive Mode instruction (with the switch in Auto Answer position) it can also disable the feature. To do this the program must issue a Test CA Busy (CIO) instruction.

If the data set has not started to answer a call when the Test For Busy instruction is executed, the CA prevents the data set from answering and the program does not branch. If the data set has started to answer a call during the execution of the instruction, the program branches because it is too late to stop the auto answer feature and the call must be accepted. In the On position, the CA is disconnected 30 seconds after it has received a call if it could not get into the receive run status within that time. It is also disconnected 30 seconds after issuing or receiving an EOT signal. Disconnection also occurs when check conditions that require manual intervention arise.

If an auto answer receiver wants to permit other calls to come through after a previous operation, his program must provide an idle loop for 35 seconds after EOT and then issue another Set Receive Mode instruction. The loop makes certain that the previous line is disconnected.

Auto answer receive programs must make use of the System/360 Model 20 interrupt feature to detect that a call has come in. A Test and Branch on Busy command cannot be used for this purpose because of its modified meaning.

Auto Answer Wait

When the Auto Answer/Disconnect switch is in the Wait position, operation is the same as when this switch is in the Auto Answer position except that the program cannot continue with the next sequential instruction after executing a Set Receive Mode instruction. The CPU enters a waiting state and awaits an incoming call. When the call is received, the program continues.

The CPU process meter does not run during the waiting state. The CPU may also be removed from the waiting state by operating the Stop key or System Reset key on the CPU console. The CA does not automatically branch back into the wait state. If desired, the programmer may cause a branch back to the Set Receive Mode instruction to enter the wait state.

When the Auto Answer/Disconnect switch is in the Off position, the auto answer/disconnect functions are disabled.

Operating Procedures

Start for Transmitting Without Auto Answer

1. Press CPU Power On key, press all I/O Start keys to get all I/O devices ready. CA Operation switch must be in Normal position.
2. Load program, then press CPU Start key to execute program.
3. Turn on data set, press CA Start key, check all switch settings.
4. Dial receiving party, when voice communication has been established, switch data set from talk to data mode. Hang up telephone receiver.

Start for Transmitting with Auto Answer On at Remote CA

1. When transmitting, the Auto Answer switch must always be OFF at the local CA.
2. Get CPU and all I/Os Ready. Load program and start execution just as before.
3. Turn on data set, press CA Start key, check all switch settings.
4. Dial receiving party but do not use voice communication.
5. Avoid pressing TEL key because this causes a Stop at the remote terminal. (Remote station may be unattended.)
6. After dialing, switch data set to data mode and hang up telephone receiver without using voice communication.

Start for a Receive Operation Without Auto Answer

1. Press CPU power On key, get I/Os ready.
2. When call comes in, get into voice communication with the remote operator.
3. Turn on data set, set CA switch to Normal, make certain that the Auto Answer switch is OFF.
4. Switch data set from talk to data mode.
5. Load program, press CPU and CA Start keys.

Start for Receive Operation with Auto Answer On at Local CA

1. Press CPU Power On Key, get system ready.
2. Load Program.
3. Start CA, turn on data set, check all switches, set Auto Answer switch to ON.
4. Press CPU Start key to execute program.

Wait with Auto Answer On at Local CA

Starting procedure is the same as for receive with auto answer except the Auto Answer switch must be in Wait position.

CA Timing Conditions

Instruction and Execute Phase

XIO	Transmit	190 usec
XIO	Receive	190 usec
TIOB	Busy	120 usec
TIOB	Error	120 usec
TIOB	EOT	115 usec
CIO	Set Receive Mode	150 usec
CIO	Set Transmit mode	135 usec
CIO	Send EOT	135 usec
CIO	Inhibit Aud. Alarm	120 usec

The service phase time is 70 μsec per character (maximum). The code translation which is handled by the CIOCS can be calculated as follows: 250 + 54 N = μsec.

250 is a factor which takes care of address calculations (indexing). N represents the number of characters in the record (254 characters maximum). Thus the maximum time for translating 254 characters is 14 ms.

Time Sharing

All standard speeds which can be selected by the Speed Selection switch allow the CA to operate simultaneously with the other I/O devices and processing operations.

Line Turn-Around Delay

In half duplex lines, the effective data transmission speed depends on turn-around delay. This turn-around delay varies with the lines used, but turn-around delays of 250 ms per change of direction can be considered standard. After a record has been transmitted, the remote station "turns around" to acknowledge after which the local station turns around to transmit again.

During this total turn-around time of 500 ms, processing or I/O functions can be performed.

The CA also allows "full duplex" operation, which is, however, actually half duplex on four wires. Even in this case there is a maximum time loss of two characters where each change of direction is from 3.3 ms up to 26.0 ms depending on the line speed selected. With the higher speed lines in "full duplex", turn-around time can practically be disregarded in connection with long records.

COLUMN BINARY FEATURE

The IBM punched card is a permanent data storing device that contains 80 storage positions (card columns). When the standard IBM card code (Figure 10) is used, each punched column contains either one digit or one character. The capacity of a card is increased to 160 storage positions, however, when the column binary code (Figure 10) is used; each punched column can then contain two digits or two characters in six-bit BCD code. A column binary card cannot be read like an ordinary punched card because the meaning of the usual zones and digits (12, 11, 0, 1, 2, etc) is changed to correspond to the bits of the BCD code. The punches in one card column represent the BCD bits B, A, 8, 4, 2, 1, and B, A, 8, 4, 2, 1 from top to bottom.

To enable the card I/O devices that can be attached to the System/360 Model 20 to read column binary cards, the Column Binary feature must be installed. This feature reads each BCD character into one byte of core storage. Since the six-bit BCD character cannot fill a byte, the character is placed into bits 2 - 7 of the byte, and bits 0 and 1 of the byte are forced to zero. Column binary reading is performed from top to bottom of the card column, proceeding by columns from left to right (Figure 11).

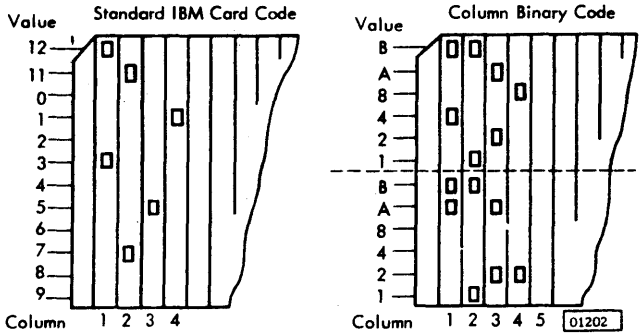
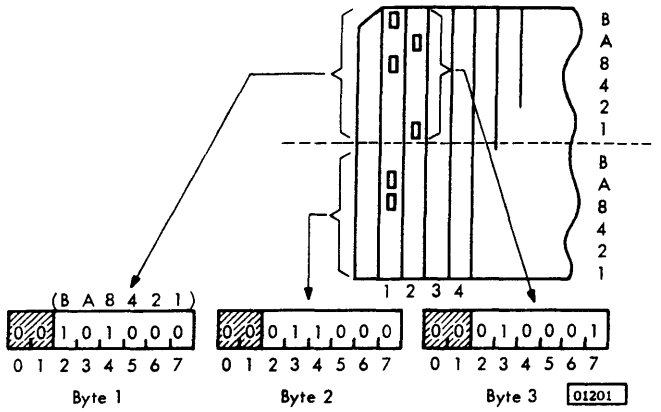


Figure 10. IBM Punched Card Codes



● Figure 11. Column Binary Reading

The programmer must know that, when the 80 columns of a card punched in Column Binary mode are read, 160 adjacent bytes of core storage are needed. The field length specification derived from the B2 and D2 fields of the XIO instruction (issued to read a column binary card) pertains to the number of BCD characters that are to be read. The field length must therefore be greater than zero and not more than 160.

The programmer can specify an odd number of characters (odd field length). When this occurs, reading always stops after the upper half of the last card column has been read. If the storage capacity is exceeded during a column binary read operation, reading stops when the highest storage position is reached, regardless of whether the field length is exhausted or not. No error indication is given.

The column binary feature is activated by an additional bit in the FS field of the XIO instruction. When bit 12 of the instruction (this is the 8-bit of the FS field) is present, the reader reads in column binary mode; when bit 12 of the instruction is zero (not present), the reader reads column-by-column. Thus, the column binary mode of reading is specified when the value of the FS is increased by eight.

The following list gives all read instructions, with the regular FS and the column binary FS, for all card I/O devices to which the column binary feature is applicable.

2501 Card Reader

DA	FS	Function	Mode
1	2	Read Card	EBCDIC
1	10	Read Card	Column Binary

2560 MFCM

DA	FS	Function	Mode
2	2	Read Primary Card	EBCDIC
2	3	Read Secondary Card	EBCDIC
2	10	Read Primary Card	Column Binary
2	11	Read Secondary Card	Column Binary

2520 Card Read Punch

DA	FS	Function	Mode
2	2	Read Card	EBCDIC
2	10	Read Card	Column Binary

COMPATIBILITY

The organization of the System/360 Model 20 is in most respects identical with that of other System/360 models. The data and instruction formats are a compatible subset. The majority of operations in the System/360 Model 20 instruction set are compatible. There are instructions and features which are different in the System/360 Model 20 from those in System/360s. These differences deserve programming consideration and are described in this section.

The System/360 Model 20 CPU exerts direct control over all the I/O devices attached to it. However, I/O operations are initiated, halted, or tested by program instructions, which select the unit to be used. The I/O instructions determine what operation is performed (read, write, etc.) and where the data is stored.

Operation Codes

The operation codes of all System/360 Model 20 instructions other than Halt and Proceed, Set PSW, Branch and Store, and Input/Output controls are the same as those assigned in other System/360 models. The operation codes of these instructions are unassigned in other models.

General Registers

The System/360 Model 20 has eight general registers. They are numbered 8-15 and correspond to the same registers in other System/360 models. They are one halfword in length compared to full word length on other System/360 models. Results of valid System/360 Model 20 binary operations are identical to corresponding operations in other System/360 models except for the recognition of an overflow condition.

Main Storage Addressing

The first 144 bytes of main storage are protected and program reference to this area results in an error condition.

Addressing

An address used to refer to main storage in the System/360 Model 20 may be specified by either of two methods; direct addressing or effective-address generation. Direct addressing is indicated when the high-order bit in the B field of an instruction is zero. The address from this method is derived from the binary value of the low-order 14 positions (for addresses up to 16383) of the combined B and D fields. Effective-address generation is automatically performed when the B field refers to general registers 8-15; in forming this address, the System/360 Model 20 operates identically to other System/360 models.

INTRODUCTION

Telecommunication, the ability to exchange up-to-date information between remote locations, is a valuable asset in the fast-paced modern business world of industry and commerce. Therefore, powerful tools such as electronic data processing systems should not be limited to strictly local input and output. Nowadays, as business activities expand and companies establish branches further afield, the rapid exchange and processing of vital data is of ever-increasing importance. Thus, more and more emphasis is being placed on Tele-processing, which offers interesting prospects to all users of data processing systems.

The IBM Binary Synchronous Communication Adapter (BSCA) for the System/360 Model 20 is a Tele-processing device which is virtually independent of such restricting factors as the necessity for code translation (due to a limited character set), complex synchronizing procedures, slow transmission speeds, etc. The adapter can be field installed in the Model 20 and adds to the capabilities of this system, since any type of binary data can be transmitted and received in time-sharing mode (at speeds up to 2,400 bits per second) with other Input/Output (I/O) and processing operations. At transmission speeds above 2,400 bits per second, the BSCA operates in burst mode.

The BSCA meets the requirements of medium- and high-speed communication systems by offering the following:

1. Transmission of the entire Extended Binary-Coded-Decimal Interchange Code (EBCDIC).
2. Transmission of the entire American Standard Code of Information Interchange (ASCII).
3. Transmission of any binary data (entire programs in any language, packed decimal data, random data, etc).
4. Transmission speeds from 600 to 50,000 bits per second.
5. Block-dividing of messages to adapt to optimal conditions on telephone lines of a given quality.
6. Powerful error-checking methods.
7. Optional features that allow a variety of different operating modes.

The BSCA can communicate with the synchronous adapter units of the IBM 2701 Data Adapter Unit and the IBM 2703 Transmission Control (equipped with the corresponding synchronous features) that provide the primary means of data exchange with System/360 Models 30, 40, 50, etc. A Model 20 equipped with the BSCA can also communicate with another Model 20 that is fitted with the BSCA.

The BSCA operates over two-wire or four-wire telephone lines that may be either privately-owned, leased, or switched (that is, part of a common carrier dial-up network*). The transmission technique is half-duplex (that is, in one direction only at a time). The adapter can communicate in point-to-point or in multipoint fashion. In point-to-point operation, data exchange is between two stations; in multipoint operation, a master station can select or poll one of a number of slave stations that are interconnected on a leased or private line.

The Binary Synchronous Communication Adapter is fully program-controlled by means of nine basic instructions. These instructions are similar to the other I/O instructions of the Model 20 which are described in this manual and, to the Model 20, the BSCA is a further I/O device. However, considerable flexibility is introduced into the program by the binary synchronous philosophy; this philosophy features precisely-defined control character sequences that "frame" each message at its beginning and end. Such a message, with its control sequences at both ends, is moved byte-by-byte from main storage in the Central Processing Unit (CPU) to a buffer from where it is transmitted bit-by-bit (serially) to the remote terminal. Here, the stream of bits enters a similar buffer where the data is re-assembled into characters and moved eventually into main storage. The control characters trigger certain actions in both stations so that each message actually controls its own mode of transmission. Thus, the main controlling elements are the control character sequences which enable each message to function as a self-controlling entity.

Transmission Codes and Interfaces

When ordering a BSCA for the System/360 Model 20, the customer must specify either the ASCII or the EBCDIC as his line code; one line code only is permissible on any adapter.

Two interfaces, the data set interface and the data station interface, are available for connecting the BSCA to a modem. (The modem converts dc signal output from the BSCA into modulated carrier signals suitable for transmission over telephone lines.) The data set interface complies with the Electronic Industry of America (EIA) requirement RS 232B; the interface allows U.S. data sets, the IBM 3977 Modem or equivalent equipment to be connected. These devices allow operation on voice-grade telephone lines at speeds ranging from 600 to 2,400 bits per second.

The data station interface (also termed digital interface) is part of the BSCA High Speed Feature and is used only when that feature is installed.

* All references in this section to switched networks apply at present to U.S.A. only.

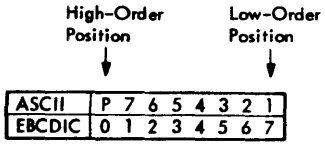


Figure 12. Sequential Numbering of Bit Positions in ASCII and EBCDIC 01256

American Standard Code of Information Interchange

This code consists of seven data bits and one parity bit (Figure 12). Thus, an eight-bit character is formed which must have odd parity. The parity bit is supplied automatically by the BSCA as needed and, therefore, the parity bit position must always be zero in all ASCII characters that are to be transmitted from main storage. The automatically-supplied parity bit is transmitted over the line; in the receiving BSCA, however, the bit is removed automatically and entered into main storage as a zero bit. The ASCII character is transmitted low-order bit (bit 1) first, bit 2 next and so on, ending with the parity bit. The ASCII-table in Appendix L shows all bit configurations; the characters within thick lines are control characters, while those in the shaded areas cause line turnaround (change of transmission direction) whenever they are preceded by the control character DLE. This operation is explained later under "Control Sequences (Basic BSCA)."

Extended Binary Coded Decimal Interchange Code

This code consists of eight data bits (Figure 12). EBCDIC characters are transmitted low-order bit (bit 7) first, bit 6 next and so on, ending with bit 0. The EBCDIC table in Appendix L shows all bit configurations; the thick lines enclose the control characters, while the shaded areas contain characters that cause line turnaround (change of transmission direction) when they are preceded by the control character DLE. See "Control Sequences (Basic BSCA)."

Table 12. Instruction Set

Type[1]	Format	Op Code	DA	FS	Function
XIO	SS	DO	5	0	Transmit and Receive
XIO	SS	DO	5	1	Receive Initial
XIO	SS	DO	5	4	Receive
CIO	SI	9B	5	2	Enable BSCA
CIO	SI	9B	5	3	Disable BSCA
CIO	SI	9B	5	6	Store Current Address
CIO	SI	9B	5	7	Store Sense Information
TIOB	SI	9A	5	0	Test and Branch on Any Indicator Set
TIOB	SI	9A	5	8	Test and Branch on Busy

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Table 13. EBCDIC Control Character Codes

Bit Position 0 1 2 3 4 5 6 7	Mnemonic	Function
0 0 0 0 0 0 0 1	SOH	Start of Heading
0 0 0 0 0 0 1 0	STX	Start of Text
0 0 0 0 0 0 1 1	ETX	End of Text
0 0 1 0 0 1 1 0	ETB	End of Transmittal Block
0 0 1 1 0 1 1 1	EOT	End of Transmission
0 1 1 *	Column 3	Change of Direction Modifier
0 0 1 1 1 1 0 1	NAK	Negative Acknowledgement
0 0 1 0 1 1 0 1	ENQ	Enquiry
0 0 0 1 0 0 0 0	DLE	Data Link Escape
0 0 1 1 0 0 1 0	SYN	Synchronization Character

* "Do not care" positions.
These bits are used at the discretion of the programmer

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DESCRIPTION (BASIC BSCA)

Instruction Set and Control Characters (Summary)

The instruction set for the basic BSCA is shown in Table 12, while EBCDIC and ASCII control characte codes are given in Tables 13 and 14 respectively.

Operating Principle

Operations in the BSCA are started by initialization, that is, by bidding for the line. The initialization assigns the right to begin transmission to one or the other station. If the BSCA gets the line, it can begin

Table 14. ASCII Control Character Codes

Bit Position P 7 6 5 4 3 2 1	Mnemonic	Function
P 0 0 0 0 0 0 1	SOH	Start of Heading
P 0 0 0 0 0 1 0	STX	Start of Text
P 0 0 0 0 1 0 0	EOT	End of Transmission
P 0 0 0 0 0 1 1	ETX	End of Text
P 0 0 1 0 1 1 1	ETB	End of Transmittal Block
P 0 1 1 *	Column 3	Change of Direction Modifier
P 0 0 1 0 1 0 1	NAK	Negative Acknowledgement
P 0 0 0 0 1 0 1	ENQ	Enquiry
P 0 0 1 0 1 1 0	SYN	Synchronization Character
P 0 0 1 0 0 0 0	DLE	Data Link Escape

* "Do not care" positions.
These bits are used at the discretion of the programmer

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to transmit; if, however, it does not get the line, it must first receive the bid from the other station before it can start its transmission. The actual data exchange is accomplished with Transmit and Receive instructions that are issued in both stations. Before each XIO instruction (Transmit/Receive) is executed, the condition code is set to indicate to the program whether the instruction can be executed or not. After each XIO instruction is executed, an interrupt is requested to provide a means for checking the results. If an error occurs, details of the cause for rejection (in the form of sense information) are available at interrupt time.

Initialization at Transmitting Station

The actual wire connection between two stations is either permanent (on private and leased lines) or it must be established by a dialing procedure (in switched networks). Dialing can also be accomplished under program control. (See "Automatic Calling Feature.")

After connection is established, an initialization procedure must be used. For reasons that are explained later in "XIO Instructions" under "Transmit and Receive", the initialization is accomplished by two different methods that ensure the proper rhythm of data exchange between the two stations. The method used depends on the intentions of the user of a particular station. If he intends first to send data to a remote station, he must use one method; if he intends first to receive data from the remote station, he must use the other method. Thus, initialization can be likened to starting on "one foot or the other", one station using one method and the other station using the opposite method; neither method represents an advantage or a disadvantage because, after initialization, each station transmits in turn.

Before any other action, the BSCA is enabled by issuing an Enable BSCA instruction. This instruction produces a positive level on the signal line 'data terminal ready' that runs from the BSCA to the modem or data set; this positive level is needed for the modem to become operational. No other preparation is needed because the BSCA has power on when the CPU has power on.

The transmitting BSCA then bids for the telephone line by issuing a Transmit and Receive instruction. The instruction reads out the actual bid from the CPU main storage and transmits it to the remote station. In the simplest form, the bid consists of an Enquiry (ENQ) character that is interpreted by the recipient as "Who are you?" A more sophisticated bid consists of some identification followed by the ENQ character which is interpreted as "I am xxx, who are you?"

The BSCA reacts to the Transmit and Receive instruction that is issued to send the bid by setting a condition code to inform the program how it may proceed:

Condition Code	Function
0 (binary 00)	BSCA is "available" and has accepted the instruction
1 (binary 01)	BSCA is "working" (it is still processing a previously-issued XIO instruction)
3 (binary 11)	Manual intervention is required because the modem or data set is not operational

If the BSCA was not enabled, a program error stop occurs when the Transmit and Receive instruction is issued. In this example, it is assumed that the BSCA has accepted the instruction; therefore, transmission over the telephone line begins with two automatically-supplied Synchronization (SYN) characters that provide synchronization with the other station, the actual bid follows next, and an automatically-supplied pad character (sent behind the ENQ character in the bid) ends the transmission. At this point, however, the instruction has not ended because the ENQ character causes the BSCA to turnaround, and to "listen" for a response from the remote station. Normally, the Transmit and Receive instruction ends only when a reply is received.

However, the BSCA spends only a limited amount of time on awaiting a reply. As soon as turnaround occurs, a receive timeout delay of 3-sec duration starts running. This timeout delay ensures that the BSCA cannot be hung-up indefinitely and unnoticed. The timeout delay is reset by every non-synchronizing character that is received immediately after a SYN character. Since the BSCA automatically inserts a SYN character after a certain time interval during transmit operations, the 3-sec timeout delay (started in the receiving BSCA) normally cannot elapse when SYN characters are detected in the data stream. It is only if either all SYN characters, or all data, or nothing, is received that a timeout occurs to end the instruction. The SYN characters are not entered into main storage.

The end of a Transmit and Receive instruction is indicated by a request for an interrupt. As explained later, tests performed in the interrupt routine reveal the ending status of the instruction. With the acceptance of the Transmit and Receive instruction, the BSCA becomes busy; when the interrupt occurs, this busy condition ends.

Initialization at the Receiver

The receiving station prepares its BSCA to receive a bid from the transmitting station by issuing a Receive Initial instruction. Prior to this instruction, the BSCA must have been enabled, otherwise a

program error stop occurs when Receive Initial is issued. The BSCA reacts to the Receive Initial instruction by setting a condition code to inform the program how it may proceed.

NOTE: If the modem has power off, the condition code for a Receive Initial instruction is set to 00 (available) and, therefore, modem power off is not noticed immediately.

In this example, it is assumed that the Receive Initial instruction is accepted. Thus, the BSCA listens for a bid. However, the BSCA does not become busy; the busy condition begins only with the actual arrival of data from the other station. With switched networks and the Receive Initial instruction, the timeout delay of 3 sec is started when the line connection is established, that is, when the modem sends the 'data set ready' signal to the BSCA; at this moment, the BSCA becomes busy and searches automatically for synchronization; if this cannot be obtained within 3 sec, a timeout occurs. With leased or privately-owned lines, the 3-sec timeout delay is started when synchronization (character phase) is established between two basic BSCA stations; however, a timeout occurs under any of the following conditions to avoid a permanent hang-up of the BSCA:

1. If no data is received
2. If a constant stream of SYN characters arrives
3. If data is received that does not contain a character (such as ENQ) to cause turnaround.

Since the BSCA is not busy when it awaits a bid (after the Receive Initial instruction was issued), a burst operation (tape, or disk storage) can interfere.

The end of a Receive Initial instruction is indicated by a request for an interrupt. This interrupt request is made under any of the following conditions:

1. When a bid has been received and stored in main storage
2. When a timeout occurs
3. When an interfering burst operation ends.

Interrupt

The interrupt indicates that an XIO instruction has ended. The BSCA interrupt is identified by the device address 5 and the function specification 6 that are stored in the old program status word. Since it is not known how a particular instruction has ended, the program must test certain indicators at interrupt time to find out whether the instruction has ended in normal or in abnormal fashion. The testing is simplified by use of the TIOB On Any Indicator Set instruction. If no indicator is set, the previous instruction has ended without errors, which means that either a bid, or a positive or negative acknowledgement, or a regular message, has been received. If one (or more) indicators are on, it is necessary to retrieve them from the unit in which they were generated and to store them into a main storage location where they can be inspected by the program. The Store Sense Information instruction is used for this task.

If an instruction has ended with timeout, the timeout flag in the sense information would be on. If a Receive Initial instruction has been interfered with by a burst operation that coincided with an incoming bid, the overrun flag in the sense information would be on. For details of all error situations, see "Sense Information."

If the error testing at interrupt time reveals that the initialization was successful, the data exchange may begin with the issue of a Transmit and Receive instruction.

The individual transmit and receive portions in corresponding instructions of both stations mutually overlap. This overlapping creates the proper rhythm of data exchange which is shown later in Figure 16.

Contention

On privately-owned or leased lines, it is possible for two stations to vie for the line at the same time. Therefore, priority is assigned to one station. The station with priority keeps repeating its bid for the line until a positive acknowledgement is recognized and, therefore, ignores bids from other stations. However, any other station that is bidding eventually receives the priority-bid when it has sent its own bid, and subsequently turns around to listen.

In switched networks, contention is normally not possible because, on other than on leased lines, the two stations are only connected when transmission is desired and in switched networks, the calling station has priority. However, if one station replies to a receive bid with an acknowledgement which indicates that reception cannot continue, contention is possible on switched lines too, because both stations remain connected after such a reply. For details, see "Control Sequences."

INSTRUCTIONS (BASIC BSCA)

XIO Instructions

Transfer I/O instructions occupy six bytes of main storage and consist of the operation code, the device address, the function specification, the address of the first (leftmost) byte of the main-storage input or output field, and the field length. The B1-D1 field can be used as the direct address of the input/output field, or an effective address may be generated by adding the contents of a genera' register (defined by B1) to the displacement (D1).

The address thus derived must not exceed the storage capacity or violate the protected area, and must not be equal to zero as this causes a specification error. The field length is similarly derived from the B2-D2 field of the instruction and represents the true field length. The field length is variable from 1 to 4,095 bytes.

All XIO instructions set the condition code prior to execution and request an interrupt after execution.

Receive Initial

This instruction prepares the BSCA to receive an initial sequence (a bid) from the other station. When this instruction is issued, the BSCA remains available until synchronization is achieved (on leased lines) or until a bid arrives (on switched lines). When synchronization is established, or when the bid arrives, the BSCA becomes busy and the bid is stored into the main-storage field defined by the B1-D1 address. An interrupt is requested and the busy condition ends when the bid is stored or when a timeout occurs due to a faulty message (all SYN characters, or all data, or nothing) being received.

If the BSCA has accepted a Receive Initial instruction but a burst mode operation (tape, or disk storage) is started by the CPU before an initial sequence is received, it is possible that an incoming bid coincides with that burst operation. The instruction ends with an interrupt that occurs when the burst mode operation (with its interrupt) is completed. At that time, the sense information overrun flag is on. A receive initial operation can be cancelled by the Disable BSCA instruction, provided that this instruction is issued before an initial sequence is received.

On switched networks, because the BSCA does not become busy and since the timeout is not started when the Receive Initial instruction is issued until a call comes in, Receive Initial can be used for automatic answering. The Auto Answer Wait switch on the BSCA console panel (see Figure 24) must be set to ON to prepare the BSCA for the type of operation that is provided for unattended stations on switched networks. With the switch on, the CPU is ready but the use meter is not running (which represents a waiting state). In this state, the Receive Initial instruction can be issued and thus the BSCA is prepared for answering if a call comes in. The use meter (and the CPU) are started by such a call.

Transmit and Receive

In the half-duplex mode of data exchange that is used by the BSCA, transmission occurs in one direction only at a time. To avoid confusion, note that each station fulfils a primary function during data exchange, independent of the individual actions that occur in each station: the primary function of one station is to serve as a transmitter, while the primary function of the other station is to serve as a receiver. Because both stations employ the Transmit and Receive instruction to correspond with each other, two names are used in the following explanation to distinguish clearly between the primary functions and the actual operations of a specific station; one station is referred to as the "donor", the other is called the "recipient."

This clarification is especially necessary when two stations are both System/360 Model 20's equipped with the BSCA. The situation is somewhat different when one station is a Model 20 but the other station is a System/360 Model 30, 40, 50 etc; these latter models operate through the 2701 Data Adapter Unit or the 2703 Transmission Control, both of which feature the channel concept. With the channel concept, actions are started by a Start I/O instruction that basically reads out a channel command word which has a read or write function. These functions, however, are identical with the transmit and receive functions of the BSCA. Further explanations are, therefore, based on Model 20 operations.

The Transmit and Receive instruction serves a dual purpose as the name indicates, that is, it causes the BSCA to transmit and subsequently to turn around to receive. This dual function is needed because of the extremely fast response coming from the other station. The B1-D1 field of the Transmit and Receive instruction defines the leftmost byte of a main-storage field that represents an output area as well as an input area, while the field length (defined by B2-D2) pertains to the total length of this combined output/input field. The length is variable from 1 to 4,095 bytes, any portion of which may be chosen as the output field, with the remaining portion representing the input field. The donor station assigns the message that is to be transmitted to the output portion of the combined field, and reserves the input portion for the reply from the recipient. The recipient usually replies with any of the standard acknowledgements. See "Control Sequences (Basic BSCA)."

The recipient uses the Transmit and Receive instruction in a similar way, but for a different purpose; the recipient assigns its reply to the output area of the combined field and reserves the input area for the next message that it expects to receive.

Any message that is to be transmitted or received must be framed by control characters on both ends. These control characters activate certain functions in the BSCA when the message is read out from the main storage of the donor and, subsequently, they activate the same functions in the recipient upon arrival. See "Control Characters (Basic BSCA)."

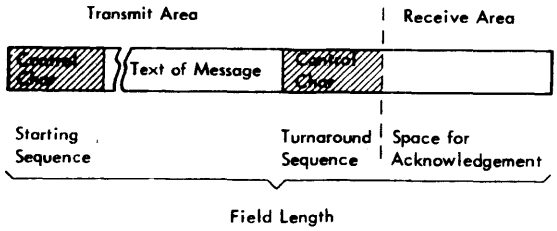

Figure 13. Transmit and Receive Instruction used by Donor 01264

Figure 13 shows a combined field as it appears in the main storage of the donor and Figure 14 shows the corresponding field as it is used by the recipient.

When a Transmit and Receive instruction is issued, the output portion (transmit area) of the combined field is always dealt with first. For the donor, this means that the message is sent out bit-by-bit until the control character at the end of the message is detected. This control character triggers the turnaround function in the donor BSCA which means that, from that moment onwards, the donor temporarily becomes a receiver. The turnaround character thus marks the boundary between output and input areas.

With the detection of the turnaround character, the 3-sec timeout is started to prevent a hang-up situation in the event that nothing is received. The BSCA becomes busy when the Transmit and Receive instruction is accepted and this condition lasts until interrupt occurs. Interrupt is normally requested only when the reply has been received and stored into the input portion (receive area) of the combined field. As explained later, interrupt is also requested when certain abnormal conditions are detected.

A Transmit and Receive instruction is processed in exactly the same way in the recipient as in the donor. The only difference is in the logical purpose for which the instruction is used by the recipient; the recipient sends an acknowledgement first after which it turns around to receive the next message. Again, an interrupt is requested when this new message has been stored or when the timeout delay has elapsed if nothing was received.

From the foregoing explanation, it may seem that the donor has an advantage over the recipient, in that the donor may send messages of any length while the recipient is limited to sending standard acknowledgements. However, this is not so; the recipient is allowed to send a message of any length in reply, provided that it has received the previous donor-message free of errors. This type of operation is termed "tête-à-tête" to distinguish it from the method of replying with standard acknowledgements.

Tête-à-tête is a French expression meaning "head-to-head" in reference to a private conversation. In the operation of the BSCA, the term characterizes the full data exchange in the foregoing sense. The tête-à-tête operation speeds up overall throughput, because a message sent by the recipient implies that the previous reception was free of errors, thus omitting the actual acknowledgement. Only when a previous reception was faulty must the recipient send a negative acknowledgement to the donor. Figure 15 shows the main-storage field for a Transmit and Receive instruction that is used in tête-à-tête operations.

Since Transmit and Receive instructions are used by both stations, a conflict must be avoided; this is achieved by using two different initialization procedures. The donor starts with a Transmit and Receive instruction while the recipient begins with a Receive Initial instruction. Thus, an offset in the rhythm of data exchange is produced to ensure that the transmit portion of a given instruction is always faced with a receive portion at the other station (Figure 16). The Transmit and Receive instructions used in both stations are not necessarily mirror images of each other. However, two types of errors (short record, and storage wraparound) must be avoided.

The short record error arises when the message that is to be transmitted, or the message that is being received, is longer than the field length specified in the Transmit and Receive instruction. When

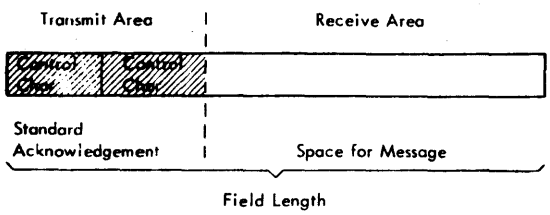

Figure 14. Transmit and Receive Instruction used by Recipient 01265

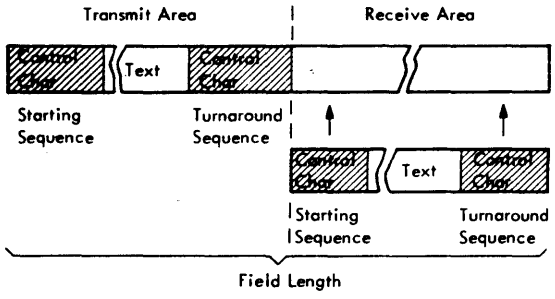

Figure 15. Transmit and Receive Instruction used in Tête-à-Tête Operations 01266

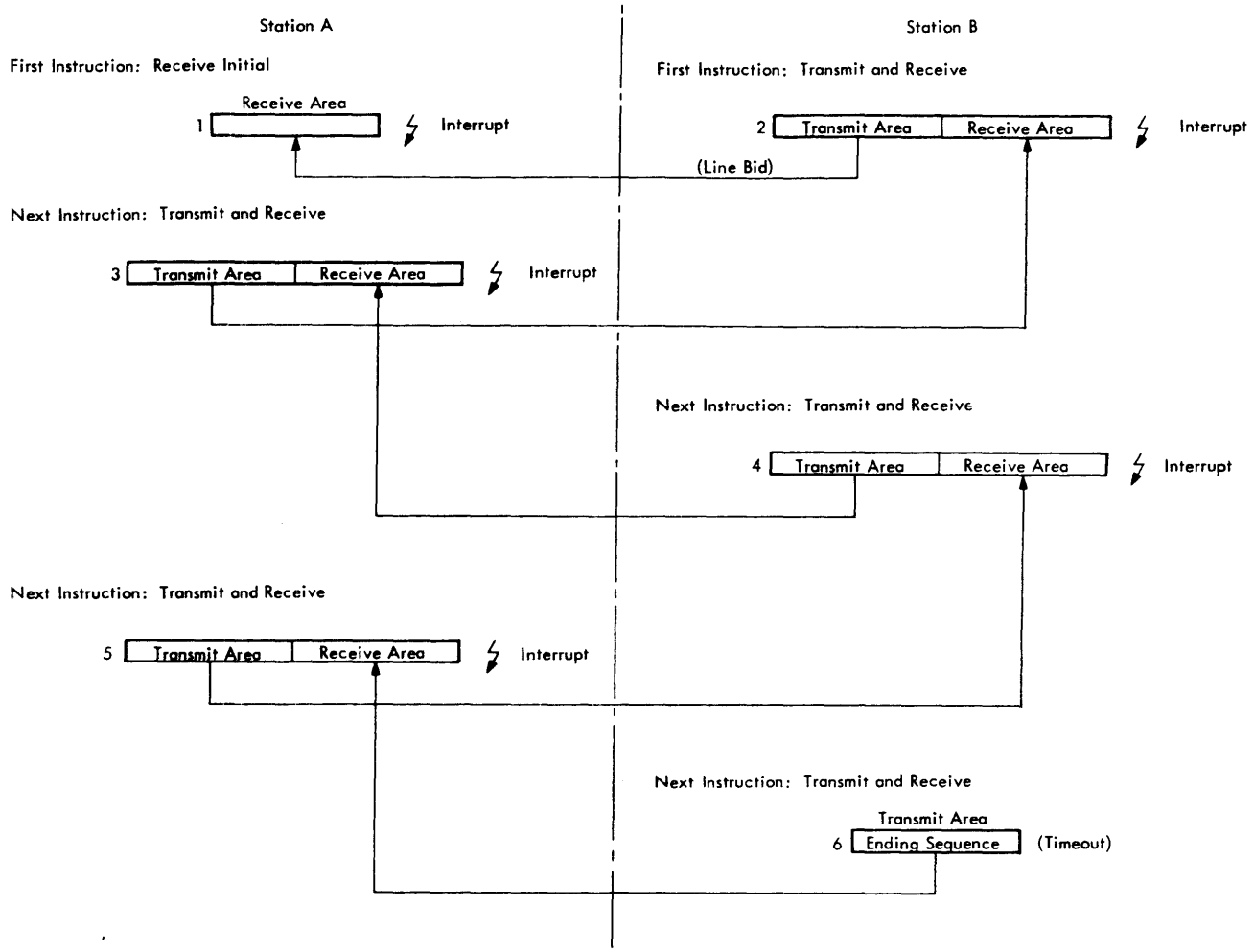

Figure 16. Data Exchange via Transmit and Receive

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a short record is detected, an interrupt request is generated immediately. The storage wraparound error arises when the storage capacity is exceeded during a transmit or receive operation. For this error, the interrupt request is also generated immediately. Both error cases are registered in the sense information, which is available at interrupt time.

Receive

The Receive instruction sets the BSCA to receive mode and the 3-sec timeout is started. The instruction is used when a previously-issued Transmit and Receive instruction has ended with timeout and the receiving BSCA assumes that the transmitter is only delayed temporarily, but will start sending again eventually. Thus, the Receive instruction serves as a timeout extender. When the instruction ends with timeout again, nothing is received. The Receive instruction can be issued as often as desired. The BSCA becomes busy when it has accepted this instruction, and the busy condition lasts until an interrupt occurs.

CIO Instructions

Control I/O instructions occupy four bytes of main storage and consist of the operation code, the device address, the function specification, and the B1-D1 field; this field further specifies the control function that is to be performed in the BSCA according to the rules for direct or effective addressing. These rules are given previously in this manual in "System/360 Model 20" under "Addressing." When a Control I/O instruction is issued, it is executed immediately and no condition code is set. However, if the BSCA is working (that is, processing a previously-issued XIO instruction), the Control I/O instruction enters the I/O-busy loop and is executed when the BSCA becomes available.

Enable BSCA

The Enable BSCA control instruction has a general "turn on" function, and is a prerequisite for all BSCA operations. When the instruction is issued, the control signal line 'data terminal ready' that runs from the BSCA to the modem or data set becomes positive; this positive level makes the modem operational. The Enable BSCA instruction must be issued prior to a Transmit and Receive, Receive, or Receive Initial instruction, or otherwise a program error stop occurs when any of these instructions are issued.

Disable BSCA

The Disable BSCA control instruction, when issued, makes the 'data terminal ready' signal line negative. The instruction can be used to withdraw from an intended data exchange that was started, provided it is issued prior to the reception of the bid or acknowledgement from the other station. If Disable BSCA is issued while a transmission is in progress, the current operation continues to completion and all operations then cease because the BSCA enters a reset state.

Store Current Address

The current address is the address of the last-received byte, updated by plus one. Thus, it defines the beginning of the next combined input/output field in main storage or the end of the previous message. The Store Current Address instruction moves the current address to the storage location addressed by the B1-D1 field of the instruction. By means of this instruction, search operations can be avoided and, therefore, inspection of the last-received message is simplified.

Store Sense Information

At interrupt time, information on the ending status of the previously-executed XIO instruction is available. When a TIOB on Any Indicator Set instruction shows that the previous XIO instruction was ended by an abnormal condition, the Store Sense Information instruction can be used to retrieve the error indications from the inaccessible auxiliary storage and to store these indications into that byte of main storage that is addressed by the B1-D1 field of the Store Sense Information instruction. The following conditions can thus be stored:

1. Transmit/receive mode error
2. Short record
3. Storage wraparound
4. Overrun
5. Timeout
6. Cyclic or longitudinal redundancy (CRC/LRC) check
7. Parity check.

For explanations of these checks, see "Sense Information."

TIOB Instructions

Test I/O and Branch instructions occupy four bytes of main storage and consist of the operation code, the device address, the function specification, and a B1-D1 field from which the branch address can be derived according to the rules for direct or effective addressing. The TIOB instructions test for a particular condition in the BSCA and if the condition is present, the program branches to the address defined by B1-D1. If the particular condition is not present, the program continues with the next sequential instruction address located in the program status word. When TIOB instructions are issued, no condition code is set.

TIOB on Any Indicator Set

The TIOB on Any Indicator Set instruction can be used to find out whether an instruction was ended by an abnormal condition. If any of the check conditions that are contained in the sense information (timeout, overrun, etc.) are present, the program branches. In this manner, the program can determine whether it is necessary to store the sense information. The instruction is executed immediately, except when the BSCA is processing a previously-issued XIO instruction. In that case, the TIOB on Any Indicator Set instruction enters the I/O-busy loop and is executed as soon as the BSCA becomes available.

TIOB on Busy

The TIOB on Busy instruction is used to find out whether the BSCA is busy (that is, processing a previously-issued XIO instruction); if so, the program branches. The BSCA becomes busy when it has accepted an XIO instruction. The busy condition ends when an interrupt occurs. Thus, the BSCA-busy condition is identical with the BSCA-working condition, except for the following difference in the use that is made of both indications:

1. The condition code for "working" is set, after the XIO instruction has been attempted, to inform the program why the attempt was unsuccessful.
2. The TIOB on Busy instruction can be performed to find out whether an XIO instruction would be successful if it were issued.

The TIOB on Busy instruction is always executed immediately, regardless of the BSCA condition.

Control Characters (Basic BSCA)

The control characters are used either singly or in groups of two consecutive characters (thus forming a control sequence) to cause certain actions in the BSCA. These actions may be divided into two categories, namely setting the BSCA to data mode, and setting the BSCA to control mode. When the BSCA has been called by another station or when it has called another station, it is in control mode. In control mode, all control characters (and/or sequences) are effective. However, certain control characters set the BSCA to data mode and, in this mode, most characters (and/or sequences) lose their control functions and can therefore be used as data. Only specific control characters cause the BSCA to return to control mode. The return to control mode is always accompanied by turnaround so that the other station has an opportunity to reply.

The control characters and their bit positions are listed in Tables 13 and 14.

Start of Heading (SOH)

The SOH character sets the BSCA to data mode and indicates that the data which follows is an identification of the message that will follow eventually. The heading can be a name, a text or a number. In data mode, SOH is recognized as normal data with no other function.

Start of Text (STX)

The STX character sets the BSCA to data mode and indicates that the data that follows is the actual text of the message. In data mode, STX is recognized as normal data with no other function.

End of Text (ETX)

The ETX character causes the BSCA to leave data mode, thereby effecting turnaround. ETX is commonly used to mark the boundary between the transmit area and the receive area of the combined output/input field that is addressed by a Transmit and Receive instruction. After ETX is sent, both stations remain connected.

End of Transmittal Block (ETB)

The ETB character is an alternate for ETX. ETB can be used to divide a message into blocks to achieve optimal block length for a telephone line of a given quality. The function of ETB is identical to that of ETX; ETB causes the BSCA to leave data mode, but it indicates that more data is to come.

End of Transmission (EOT)

The EOT character can only be used in control mode to indicate that the transmitter does not intend to continue the current transmission. EOT causes turnaround so that the receiver has an opportunity to start its own transmission. Both stations remain connected after EOT is sent. If EOT is sent in data mode, the character is recognized as normal data with no other function.

Negative Acknowledgement (NAK)

The NAK character can only be used in control mode to indicate that the received message cannot be accepted because it was faulty. NAK causes turnaround and both stations remain connected. If NAK is sent in data mode, the character is recognized as normal data with no other function.

Enquiry (ENQ)

The ENQ character can be used in data mode or in control mode. ENQ causes turnaround and both stations remain connected. When ENQ is sent in data mode, the BSCA returns to control mode. The enquiry character is used for abandoning a transmission and also as initial sequence. The program in the receiving BSCA should react to an ENQ by sending information that indicates whether transmission can continue or not.

Data Link Escape (DLE)

The DLE character is used in control sequences only. In data mode, this character is recognized as normal data with no other function. See "Control Sequences (Basic BSCA)."

Synchronization Character (SYN)

The SYN character is automatically inserted into the data stream at the proper time to establish and maintain synchronization. The program has no influence on this character and SYN does not enter main storage.

Control Sequences (Basic BSCA)

Control sequences are formed by two consecutive control characters with no other data in between. They may be divided into three groups, namely, standard affirmative replies, turnarounds, and ending sequences. All control sequences are effective only when used in control mode; the sequences are recognized as normal data with no other function when used in data mode.

Standard Affirmative Replies

In normal data exchange, it is customary to acknowledge each received message with an affirmative reply. If the reply cannot be positive because the received message was faulty, a NAK character must be used as reply. The character sequence STX/EOT can be used if the recipient wants the transmission to be terminated.

Odd-numbered messages (first, third, fifth, etc.) are acknowledged by ACK-1 and even-numbered messages are acknowledged by ACK-0. The abbreviation ACK stands for Acknowledgement, but the actual acknowledgement is realized by the DLE character as the leader, followed by specific bit combinations as the trailer. A third positive acknowledgement, which has a special meaning is Wait before Transmit (WABT); WABT indicates to the transmitting station that the receiver has a temporary not-ready condition.

Figure 17 shows the three standard affirmative replies in ASCII and EBCDIC. The question mark shown is a regular ASCII character, while the digits in the EBCDIC configuration are not numbers but represent a bit configuration in hexadecimal notation. The actual bit configuration for the question mark is the same as that for WABT (see Figure L-1 in Appendix L). For the actual bit configuration of the hexadecimal expressions, see Appendix E.

All standard replies cause turnaround. Standard affirmative replies, however, need not necessarily be used; the customer may prefer to operate in tête-à-tête mode. In this case, another message is used as the positive reply, provided the previous transmission was received correctly. However, when the previous transmission was received in error, the NAK character must be used as the negative reply. Standard affirmative replies as well as NAK can only be used outside of data mode.

Start of Block Sequences

Since there are no alternating acknowledgements in tête-à-tête operations, two sequences are used as a programming convention to identify each message. These sequences can either precede the heading or they can be used in the heading. They represent the functions Start of Block (SOB)-1 and SOB-2. The sequences consist of the DLE character followed by a trailer character; for the bit configuration of the trailer, see the ASCII and EBCDIC tables in Appendix L. Both sequences activate no function in the BSCA, but concern only the program.

Function	ASCII		EBCDIC	
ACK-0	DLE	0	DLE	/70/
ACK-1	DLE	1	DLE	/61/
WABT	DLE	?	DLE	/7F/
	↑ Leader	↑ Trailer	↑ Leader	↑ Trailer

Figure 17. Standard Affirmative Reply Sequences 01258

Turnaround Sequences

Turnaround sequences are used to effect turnaround when the BSCA is in control mode. In data mode, these sequences are recognized as normal data with no other function. The sequences consist of the DLE character followed by any of the "Column 3" characters. Column-3 characters are located in the third column of the ASCII table in Appendix L, and are shown also in the shaded areas of the EBCDIC table in the same appendix. The Column-3 characters alone have no effect.

The character sequence DLE/Column 3 can be used as an acknowledgement to which a special meaning may be assigned by agreement. In addition, the low-order bits of these characters are "do not care" bits, that is, the bits can be used by the programmer, provided that the total character retains odd parity in ASCII and in EBCDIC. If such a character is turned, even by insertion of bits into the "do not care" area, it loses its control function.

Ending Sequences

Ending sequences can be used only in control mode, otherwise they are recognized as normal data. The character sequence STX/EOT is an acknowledgement which indicates to the transmitter that the last message was received free of errors, but that reception cannot continue. Both stations remain connected after STX/EOT is sent and turnaround occurs. The character sequence DLE/EOT is used to announce End of Transmission. After DLE/EOT, the line is disconnected (in switched networks) or operations cease (on private and leased lines).

Programmed Halts

Since the Model 20 equipped with the BSCA is a rather complex terminal, it is quite possible that a programmed halt occurs due to a not-ready condition in one of its I/O devices. Such halts can be caused by card jams, forms check, empty hopper, etc., and they interfere with BSCA operations. To avoid stopping the BSCA without giving any indication of the reason for this, the Model 20 program must

	Valid Combination	Valid Combination	Valid Combination	Valid Combination
High Speed Feature	Installed	No	No	No
Station Selection Feature	No	Installed	No	Allowed if no Auto Calling Feature
Automatic Calling Feature	No	No	Installed	Allowed if no Station Selection Feature
Internal Clocking Feature	No	Allowed	Allowed	Installed
Full Transparency Feature	Allowed	Allowed	Allowed	Allowed
Intermediate Block Checking Feature	No	Allowed	Allowed	Allowed

Figure 18. Optional Features Configuration 01269

send an ending sequence to the remote BSCA prior to issuing the halt instruction.

If the local BSCA is the donor, STX/ENQ (or data ending with ENQ) must be sent. To this, the recipient responds with NAK. When NAK is recognised, the donor must send EOT (or DLE/EOT on switched lines) and then the halt instruction can be issued.

If a condition requiring a halt comes up in the recipient, the recipient must send EOT (or DLE/EOT) after it has received the ending character (ETB or ETX) of the current message. After that, the halt instruction can be given.

The BSCA can receive the EOT even after the CPU has stopped. The received EOT causes the BSCA to enter the reset state. Enable BSCA must be given before operations can be resumed. However, the first BSCA-XIO instruction that is issued (after a received EOT) is rejected, and the condition code is set to 3 (binary 11). This condition code reminds the program to check the EOT bit that is on in the sense information.

Initialization Sequence

The initialization sequence is used to bid for the line and is actually an indirect control sequence since it only initiates data exchange. The sequence consists either of an ENQ character alone which is interpreted as "Who are you?", or of some identification followed by ENQ which is interpreted as "I am xxx, who are you?" The sending of an initialization sequence does not set the BSCA to data mode.

BSCA OPTIONAL FEATURES

To accommodate special needs, optional features are provided for the Binary Synchronous Communication Adapter. All of these features can be field-installed, but the installation of some features excludes others. Figure 18 lists features and shows valid combinations for the same BSCA; the shaded areas provide a guide to which features can be added when a specific feature is already installed.

With the installation of certain features, instructions and control characters, additional to those described previously for the basic BSCA, are provided to operate them. The additional instructions (Figure 19) can be used only when the corresponding feature is installed. If an instruction is issued when the feature is not installed, the condition code is set to 3 (binary 11), meaning not operational, and a programming error stop occurs with error number 6 displayed in data register I on the CPU console.

Type	Format	Op Code	DA	FS	Function
XIO	SS	D0	5	2	Address Prepare
XIO	SS	D0	5	3	Auto Call
CIO	SI	9B	5	0	Disable ITB
CIO	SI	9B	5	1	Enable ITB
CIO	SI	9B	5	8	Store ITB Address

EBCDIC

Bit Position 0 1 2 3 4 5 6 7	Mnemonic	Function
0 0 0 1 1 1 1 1	ITB	Intermediate Block (Unit Separator)

ASCII

Bit Position P 7 6 5 4 3 2 1	Mnemonic	Function
P 0 0 1 1 1 1 1	ITB	Intermediate Block (Unit Separator)

Figure 19. Additional Instructions for Optional Features 01268

Internal Clocking Feature

The Internal Clocking Feature supplies the clock pulses that are required for establishing and maintaining bit synchronization. The feature provides for transmission speeds of 600, 1,200, 2,000 or 2,400 bits per second, the required speed being set by the customer engineer when the feature is installed.

This feature is required whenever the modem or data set does not provide the clock pulses. The feature is required also if the other station (or stations) on the same network use internal clocking; conversely, if the BSCA is equipped with the internal clocking feature, the other stations must be similarly equipped. When the feature is installed, four SYN characters are automatically supplied in addition to the two regular SYN characters to establish and maintain bit synchronization.

High Speed Feature

The High Speed Feature is required for transmission speeds above 4,800 bits per second (such as 19,200 or 40,800 bits per second), up to a maximum of 50,000 bits per second. One part of this feature is the data station interface (digital interface). At speeds above 2,400 bits per second, the BSCA executes all XIO-type instructions in burst mode, which means that all other operations in the Model 20 are excluded for the duration of the burst mode operation. However, in the Model 20 burst mode operations can be processed only when the CPU is not processing any time-shared operations. When a BSCA-XIO instruction is issued while time-shared operations are in progress, the condition code is set to 2 (binary 10) and the program continues with the next sequential instruction. On completion of all current time-shared operations, the CC2 interrupt occurs (identified by device address 15) and the burst mode operation can be executed because the CPU is then free.

Automatic Calling Feature

The Automatic Calling Feature enables the BSCA to originate dial calls by program control. The program-generated call is delivered to an externally-attached automatic calling unit that executes the dialing. Automatic calling units are used only in switched networks.

Prior to initiating a call, the Enable BSCA instruction must be issued to make the modem operational. The dialing information (the number of the desired subscriber) is transmitted to the automatic calling unit by means of the Auto Call instruction. When this instruction is issued, the condition code is set to 1 (binary 01) if the BSCA is processing a previously-issued XIO instruction. If the automatic calling unit has power off, or if the data key on the connected telephone set was not pressed, the condition code is set to 3 (binary 11).

When the Auto Call instruction is accepted, the four low-order bits of each byte of the output field (addressed by B1-D1) are transmitted to the calling unit. The number of half-bytes that are thus transmitted is specified by the field length. After transmission, an interrupt is requested. If no error flag is on, connection is established; if the timeout flag is on, the connection cannot be made because either the line is busy, or the wrong number was used.

Station Selection Feature

The Station Selection Feature is required whenever the BSCA is to be incorporated into a centralized multipoint network on leased or privately-owned lines. In a centralized multipoint network, all operations are initiated by the master station. The master station transmits to one or more slave stations by selecting them, and receives from a slave station by polling it. Thus, the initiative rests with the master station; the slave stations cannot begin to transmit without having been requested to do so. In a multipoint network, all stations involved must have the same speed, transmission code, and optional features. The Model 20 has no master station capability.

At initialization time, and always after the end of a transmission from a slave station, the master station has the sole right to transmit. The master station uses two different initial sequences, either a selection sequence or a polling sequence. The selection sequence causes a specific slave station to serve as the receiver, and the polling sequence requests a specific slave station to transmit to the master station. The configurations of both sequences are alike and consist of a station address, followed by data (that represents an identification) and by the ENQ character (Figure 20). To distinguish between

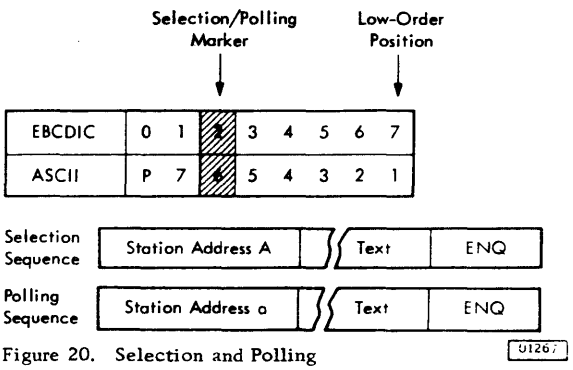


Figure 20. Selection and Polling

polling and selection, bit position 2 (in EBCDIC) and bit position 6 (in ASCII) are treated as "do not care" bit positions by the address decoding circuits. These bit positions are used to mark polling or selection. The BSCA is equipped with an address decoder for the station address. The station address is set up by the customer engineer when the feature is installed.

To gain access to the multipoint network, the BSCA must be enabled and the modem must be ready. The Address Prepare instruction must then be issued. This instruction causes the BSCA to search for synchronization, but the BSCA does not become busy until it is polled or selected. After Address Prepare, a burst mode operation can interfere during the not-busy period.

When synchronization is achieved, the BSCA monitors the line for the EOT character. An EOT character within a stream of data has no effect on the BSCA; an EOT that is sent (outside of data mode) to indicate an end of transmission, however, puts the monitoring BSCA into control mode. In control mode, the BSCA monitors the line for either of its addresses. No data is transferred to main storage during monitoring operations. If either of the BSCA addresses (polling or selection) is recognized, the BSCA enters select mode and becomes busy until the initialization sequence from the master station is received. The select mode is indicated on the BSCA console (see Figure 24) and pertains to both polling and selection; its meaning is, therefore, that the BSCA has been addressed by the master station. After the initialization sequence has been received, interrupt is requested. In the interrupt, the sequence must be examined for selection or polling (an agreement on the marker bit must exist among the sub-subscribers). If the station was polled, it must transmit to the master. With every starting sequence (SOH, and STX), the BSCA enters data mode; with every turnaround sequence, the BSCA returns to control mode. When an EOT character is sent or received in select mode, all stations on the network return to control mode.

Intermediate Block Checking Feature

The Intermediate Block Checking Feature allows the programmer to divide a message into small blocks, so that each block is checked separately. Turnaround (with acknowledgement of each intermediate block) is not needed and, therefore, overall throughput is increased. Without this feature, a check is performed only after the entire message has been transmitted.

The length of the intermediate blocks can be freely chosen. A block-divided message can be processed by the receiver while transmission is still in progress because each block (that is received free of errors) is made available by means of an intermediate interrupt. This interrupt is requested only in the receiving BSCA and it is identified by the function specification 2. The final interrupt (function specification 6) occurs only at the end of the entire message, that is, when turnaround occurs.

The intermediate block checking feature is automatically activated when the Power On key on the CPU console is pressed. If intermediate block checking is not desired, the Disable ITB instruction must be issued. After this instruction, the feature can be activated at any time by issuing the Enable ITB instruction. These instructions are executed immediately except that, when the BSCA is busy, they enter the I/O-busy loop and are executed as soon as the BSCA becomes available.

The message is divided into blocks by the Intermediate Block (ITB) character as shown in Figure 21. The ITB characters are recognized as normal data with no other function when the feature is not enabled.

When the intermediate interrupt occurs in the receiving BSCA, the last-received block can be used directly without testing for any errors. The error testing is superfluous because the intermediate interrupt is requested only when the received block is error-free; in addition, the TIOB on Any Indicator Set instruction cannot be used because the BSCA remains busy for the duration of the entire message and, therefore, the test instruction would be locked in the I/O-busy loop. If a block is faulty, no intermediate interrupt occurs for this and all following blocks. At final interrupt time (end of message), error testing can be performed.

During ITB operations, the receiving BSCA stores automatically the address of each ITB character. This address is updated by every block that is received free of errors, and thus it shows where the

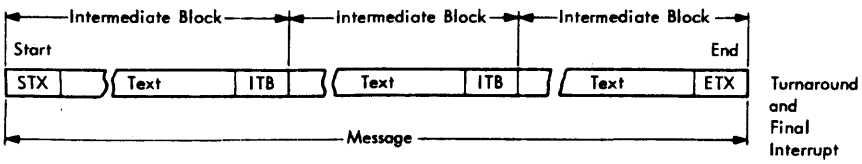


Figure 21. ITB Message

ITB character of the last-received error-free block is located in the main storage. If an error occurs, the ITB address is not updated but remains unaltered so that the address of the last "good" block can be made available at final interrupt time. The address is made available by issuing the Store ITB Address instruction. The instruction is executed immediately (even though the BSCA is busy) and moves the ITB address to the main-storage position addressed by B1-D1.

The block in which an error is detected is stored into main storage as if it were a good block, but any further blocks that belong to the message are not stored, even if they are received free of errors. However, the ending sequence of the message is stored into the byte next to the last byte of the faulty block.

All blocks that belong to a message must be transmitted with one Transmit and Receive instruction. Transmitting a single block defeats the purpose of block checking and, if a single block does not end with the ETX character, a timeout occurs because there is no turnaround after ITB.

Intermediate block checking is inhibited by the Disable ITB instruction. Intermediate block checking can be used only at speeds up to 2,400 bits per second. Above this speed, there is insufficient time for the interrupt requests to be serviced.

Full Transparency Feature

The Full Transparency Feature allows the BSCA to transmit (free of restriction) any kind of binary data. The feature is required for the transmission of packed decimal data, entire programs, random data, etc. Transmission of this binary data is accomplished by making all control characters available for use as data; thus, a message becomes transparent.

The feature is activated by sending or receiving the starting sequence DLE/STX. This sequence places the BSCA into data mode and into transparent mode at the same time. When transparent mode is set, the following characteristic changes occur:

1. The BSCA recognizes neither individual control characters nor control sequences as anything but data with no other associated function.
2. All inserted SYN characters are automatically preceded by a DLE character.
3. A second DLE is automatically attached to every "data-DLE" to mark the data-DLE as such. This second DLE, and the inserted DLE/SYN's, are automatically deleted upon reception and do not enter main storage. (Therefore, the program must not insert SYN characters as "fillers" as these will enter main storage.)

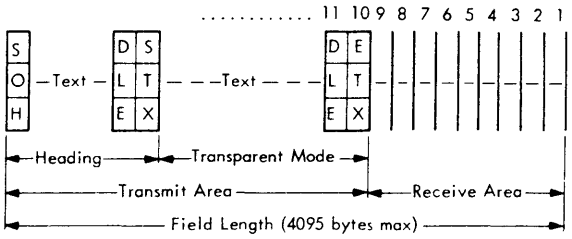


Figure 22. Transparent Message 01270

To leave transparent mode, the following ending sequences are available: DLE/ETX, DLE/ETB, DLE/ITB, and DLE/ENQ. These sequences are recognized as escape signals only when they coincide with two specific values in the field length counter of the transmitting station. DLE must coincide with the counter value 11 (decimal) and the associated ETX, ETB, ITB, or ENQ must coincide with the counter value 10 (decimal). As Figure 22 shows, a transparent message may be of any length up to 4,095 bytes; however, due to the fixed location at which the escape sequence must appear, a reply of not greater than nine-bytes length is required. Longer replies, such as used in tête-à-tête operations, are not permitted, but a tête-à-tête-type reply that is limited to nine bytes in length is allowed.

All escape sequences (except DLE/ITB) that are used to leave transparent mode cause the BSCA to return to control mode. In addition, all of them (except DLE/ITB) cause turnaround. DLE/ITB is used to end a transparent block when the intermediate block checking feature is enabled together with the full transparency feature. When transparent intermediate blocks are to be transmitted, there must be a Transmit and Receive instruction for each transparent block.

Each transparent intermediate block is started with DLE/STX and ended with DLE/ITB. After each transparent intermediate block, the transmitting BSCA sends SYN characters for 3 sec to retain synchronization. To avoid timeout, the transmitter must send the next block before 3 sec have elapsed.

The sequence DLE/SOH does not set transparent mode, it is accepted as strictly SOH. The sequence DLE/EOT has no transparency function. DLE/EOT is the disconnect sequence for switched networks.

SENSE INFORMATION

The sense information is a collection of check bits which indicates the type of error that occurred. These bits are available at final interrupt time and must be moved from auxiliary storage (where they are generated) to a main-storage position where they can be examined by the program. The Store

Sense Information instruction is designed explicitly for the retrieval of this information. After the execution of this instruction, or after acceptance of the next XIO instruction, the sense information is reset. (See Figure L-3 in Appendix L.)

Check Bits

The individual bits are described in the following text.

Bit Zero - Transmit/Receive Mode Error

Bit zero indicates whether the error occurred during transmission or during reception. When this bit is present (binary 1), the error occurred during receive operations. When it is not present (binary 0), the error occurred in transmit operations.

Bit One - EOT Received

This bit indicates that the remote BSCA station was forced to stop transmission or reception due to an I/O condition that required a programmed halt. Thus, this bit indicates that operations will resume when the halt condition has been corrected in the other station.

Bit Two - CRC/LRC Check

Bit two is set when either the Cyclic Redundancy Checking (CRC) circuits or the Longitudinal Redundancy Checking (LRC) circuits have detected an error. Both checking circuits can be installed in the BSCA. The checking circuits are activated in both stations with each starting sequence (SOH, STX) and they accumulate a block check character by way of arithmetic operations. After each ending sequence (ETX, ETB, or ITB), the transmitter sends its Block Check Character (BCC) to the receiver where it is compared with the BCC generated by the receiver. Thus, only the receiver detects CRC/LRC errors. These errors are caused by noise on the telephone line. (The efficiency of a noisy telephone line can be greatly increased when messages are divided into blocks that reduce the error probability by way of smaller individual lengths.)

Bit Three - Timeout

Bit three is turned on in the receiving BSCA only when the BSCA is in receive mode and if either:

1. The BSCA does not receive a SYN character, interspersed at the proper time interval
2. The BSCA does not receive a turnaround sequence before 3 sec have elapsed
3. The BSCA receives constant SYN characters for 3 sec.

If the timeout bit is set during an Auto Call instruction, it indicates that the telephone line was busy or that the connection cannot be made (wrong number, etc).

Bit Four - Short Record

Bit four indicates that the field length specification of a Transmit and Receive instruction is smaller than the size of the combined output/input field in main storage that is addressed by the instruction. During processing of an instruction with insufficient field length, the field length counter in the BSCA runs down to zero prior to the detection of the turnaround character (ETX or ETB).

The short record bit is also turned on under the following circumstances:

1. When the field length specification is correct but the turnaround character is either not detected or missing.
2. If the escape sequence in transparent data does not coincide with field length counter values 11 (decimal) and 10 (decimal).

Bit Five - Storage Wraparound

Bit five is turned on when the combined output/input field (addressed by a Transmit and Receive instruction) exceeds the upper limit of the main storage of the CPU. Depending on the main-storage size, the upper limit is either 4,095, 8,191, 12,287, or 16,383 positions; beyond these limits, storage wraparound occurs.

Bit Six - Parity Check

Bit six covers two different types of parity check:

1. The bit is turned on when a parity error is detected within the data path of the transmitting BSCA. This parity error is indicated only in the transmitting BSCA, and requires the attention of a customer engineer.
2. The bit is set only in the receiving BSCA when ASCII is used as the basic code and the full transparency feature is not installed. The bit indicates a vertical redundancy error (invalid ASCII character) detected during receive operations.

Bit Seven - Overrun

Bit seven is turned on when a burst mode operation (tape, or disk) overlaps the reception of an initial sequence (a bid) that was invited by a Receive Initial instruction or an Address Prepare instruction. The overrun bit is also set in the event that a BSCA

malfunction prevents the micro-program from servicing BSCA requests; this fault must be corrected by a customer engineer.

Burst mode operations end with an interrupt. After such an interrupt, a BSCA interrupt can follow in which the overrun bit is on, which indicates that an initial sequence was received during the burst mode operation. Therefore, an acknowledgement must be sent back within 3 sec, otherwise timeout occurs.

BSCA REJECT CONDITIONS

To avoid program error stops during BSCA operation, the following basic requirements must be met:

1. The BSCA must be enabled (to supply the 'data terminal ready' signal for the modem)
2. The modem must have power on and must not be in a test state (so that it can supply the 'data set ready' signal for the BSCA)
3. Instructions must not be issued for optional features which are not installed.

The BSCA instructions are subject to the same rules and restrictions that apply to Model 20 instructions, that is, they must be located on even boundaries in main storage, and addresses must neither violate the protected area nor exceed storage capacity. Field length specifications in excess of 4,095 bytes can be stated; however, only the 12 low-order bits of the field length are used. Burst mode operations (tape, or disk) that interfere with either a Receive Initial instruction or an Address Prepare instruction must not interfere more than once, and new burst mode operations must be inhibited until the initial sequence is received and a reply has been sent.

Figure 23 shows the reject conditions of the BSCA.

ERROR CHECKING METHODS

Three error checking methods are used in the BSCA: CRC, LRC, and Vertical Redundancy Checking (VRC). The methods are used in the following circumstances:

Circumstances	Checking Methods
When EBCDIC is used as the transmission code.	CRC
When ASCII is used as the transmission code and the full transparency feature is not installed in the BSCA.	LRC and VRC
When ASCII is used as the transmission code and the full transparency feature is installed in the BSCA.	CRC

BSCA CONSOLE

The BSCA console (Figure 24) is located adjacent to the Model 20 CPU console and contains all indicator lights that are required to show the current state of the BSCA. The following indicator lights are provided:

BUSY: Indicates that an XIO type instruction is being processed.

REC MODE: Indicates that the BSCA has turned around to receive.

TSM MODE: Indicates that the BSCA is set as a transmitter.

REC LINE: Indicates that a message is being received on the telephone line.

TSM LINE: Indicates that a message is being transmitted over the telephone line.

CHAR PHASE: Indicates that the BSCA is in synchronism with another station.

DATA MODE: Indicates that a control character sequence has set the BSCA to data mode.

TRANSP MODE: Indicates that the BSCA is set to transparent mode.

REC IN OR ADPREP: Indicates that the BSCA was set to receive mode by a Receive Initial instruction or an Address Prepare instruction.

ANY CHECK COND: Indicates that any of the indicators that are testable at interrupt time have been set by an abnormal condition.

DIAGNOSE: Indicates that the BSCA is in test mode.

CONTROL MODE, SELECT MODE: Both indicators are provided when the station selection feature is installed. CONTROL MODE indicates when the BSCA is monitoring. SELECT MODE indicates when the BSCA has been addressed by the master station.

ACU POWER, ACU CALL REQUEST: Both indicators are provided when the automatic calling feature is installed. ACU POWER indicates that the externally-attached automatic calling unit has power on. ACU CALL REQUEST indicates that the BSCA has sent dialing information to the automatic calling unit.

Affected Instructions	Error Type	Result
Enable ITB Disable ITB Auto Call Address Prepare	Feature not installed	Program error stop (6 displayed in Data Register 1)
Auto Call	BSCA not enabled (Data Terminal Ready off)	Program error stop (6 displayed in Data Register 1)
Auto Call	Auto Call Unit power off or Data key on connected telephone set not pressed	Condition code 3 (not operational)
Receive Initial	BSCA not enabled (Data Terminal Ready off)	Program error stop (6 displayed in Data Register 1)
Receive Initial	Modem Power Off	Condition Code 00 (available)
Address Prepare	BSCA not enabled (Data Terminal Ready off)	Program error stop (6 displayed in Data Register 1)
Address Prepare	Modem not operational (Data Set Ready off)	Condition code 3 (not operational)
Transmit and Receive, or Receive	BSCA not enabled (Data Terminal Ready off)	Program error stop (6 displayed in Data Register 1)
Transmit and Receive, or Receive	Modem not operational (Data Set Ready off)	Condition code 3 (not operational)
All XIO instructions	BSCA busy with processing of previous XIO instruction	Condition code 1 (working)
All CIO and TIOB instructions, except Test on Busy and Store ITB Address	BSCA busy with processing of previous XIO instruction	Enter I/O - Busy Loop, wait for available, then execute instruction

Figure 23. BSCA Reject Conditions 01272

DATA SET READY: On private or leased lines, DATA SET READY indicates that the modem is operational and is not in a test mode. On switched lines, DATA SET READY indicates that the line connection is established.

DATA TERMINAL READY: Indicates that the BSCA has been enabled.

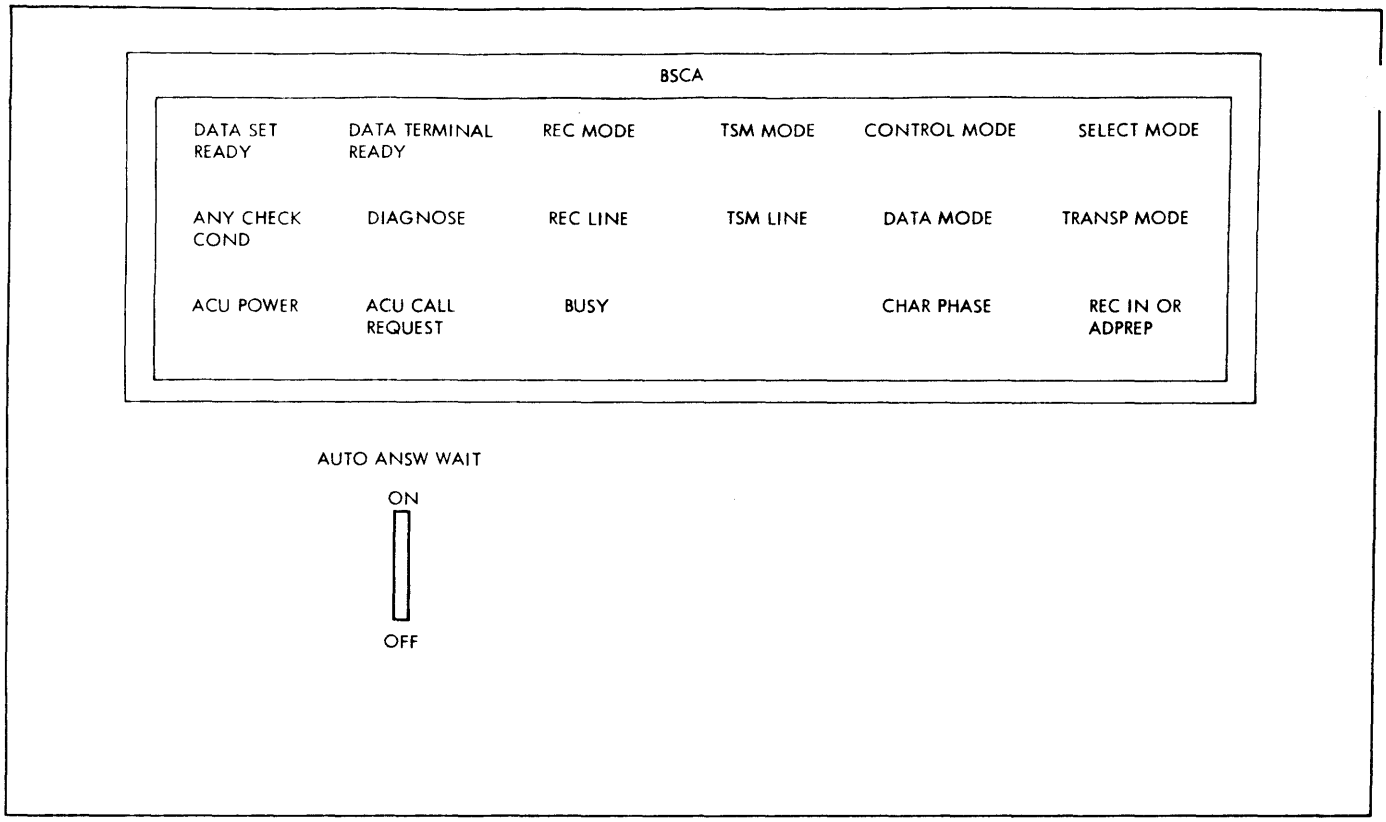


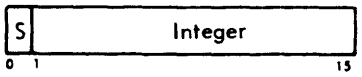
Figure 24. BSCA Console

01260

DATA FORMATS

Binary Number

Halfword Binary Number



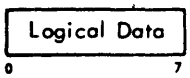
Decimal Numbers

Packed Decimal Number

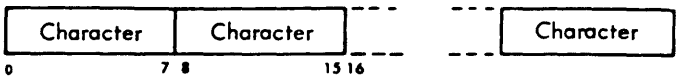
Zoned Decimal Number

Logical Information

Fixed-Length Logical Information

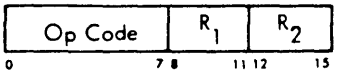


Variable-Length Logical Information

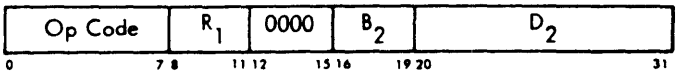


INSTRUCTIONS BY FORMAT TYPE

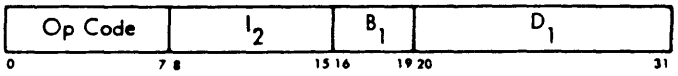
RR Format



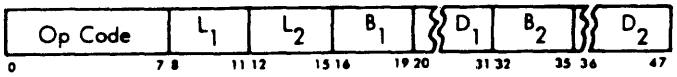
RX Format



SI Format

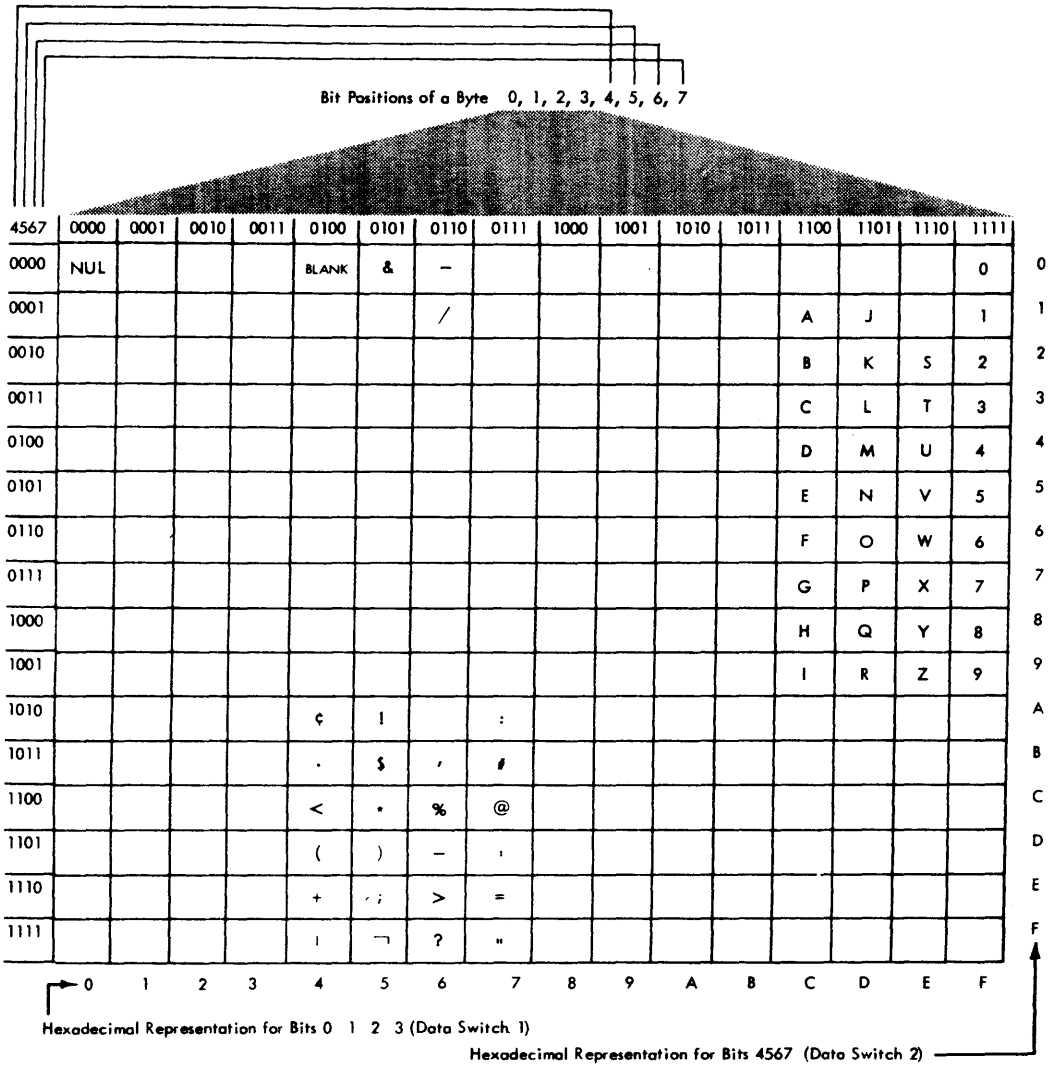


SS Format



APPENDIX B EBCDIC AND ASCII CHARTS

Extended Binary-Coded-Decimal Interchange Code (EBCDIC)



4567	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
0000	NUL				BLANK	&	–									0	0
0001							/						A	J		1	1
0010													B	K	S	2	2
0011													C	L	T	3	3
0100													D	M	U	4	4
0101													E	N	V	5	5
0110													F	O	W	6	6
0111													G	P	X	7	7
1000													H	Q	Y	8	8
1001													I	R	Z	9	9
1010					¢	!		:									A
1011					.	$	,	#									B
1100					<	*	%	@									C
1101					(	)	–	'									D
1110					+	;	>	=									E
1111					|	¬	?	"									F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

American Standard Code for Information Interchange (ASCII)
Extended to Eight Bits

Bit Positions →76 / X5 / 4321	00	01	10	11
0000	NUL	DLE		
0001	SOH	DC1		
0010	STX	DC2		
0011	ETX	DC3		
0100	EOT	DC4		
0101	ENQ	NAK		
0110	ACK	SYN		
0111	BEL	ETB		
1000	BS	CAN		
1001	HT	EM		
1010	LF	SS		
1011	VT	ESC		
1100	FF	FS		
1101	CR	GS		
1110	SO	RS		
1111	SI	US		

01	00	01	10	11
0000	SP	0		
0001	!	1		
0010	"	2		
0011	#	3		
0100	$	4		
0101	%	5		
0110	&	6		
0111	'	7		
1000	(	8		
1001	)	9		
1010	*	:		
1011	+	;		
1100	,	<		
1101	-	=		
1110	.	>		
1111	/	?		

10	00	01	10	11
0000			\	P
0001			A	Q
0010			B	R
0011			C	S
0100			D	T
0101			E	U
0110			F	V
0111			G	W
1000			H	X
1001			I	Y
1010			J	Z
1011			K	[
1100			L	~
1101			M	]
1110			N	^
1111			O	_

11	00	01	10	11
0000			@	P
0001			a	q
0010			b	r
0011			c	s
0100			d	t
0101			e	u
0110			f	v
0111			g	w
1000			h	x
1001			i	y
1010			j	z
1011			k	{
1100			l	¬
1101			m	}
1110			n	|
1111			o	DEL

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2^n	n	2^{-n}
1	0	1.0
2	1	0.5
4	2	0.25
8	3	0.125
16	4	0.062 5
32	5	0.031 25
64	6	0.015 625
128	7	0.007 812 5
256	8	0.003 906 25
512	9	0.001 953 125
1 024	10	0.000 976 562 5
2 048	11	0.000 488 281 25
4 096	12	0.000 244 140 625
8 192	13	0.000 122 070 312 5
16 384	14	0.000 061 035 156 25
32 768	15	0.000 030 517 578 125
65 536	16	0.000 015 258 789 062 5
131 072	17	0.000 007 629 394 531 25
262 144	18	0.000 003 814 697 265 625
524 288	19	0.000 001 907 348 632 812 5
1 048 576	20	0.000 000 953 674 316 406 25
2 097 152	21	0.000 000 476 837 158 203 125
4 194 304	22	0.000 000 238 418 579 101 562 5
8 388 608	23	0.000 000 119 209 289 550 781 25
16 777 216	24	0.000 000 059 604 644 775 390 625
33 554 432	25	0.000 000 029 802 322 387 695 312 5
67 108 864	26	0.000 000 014 901 161 193 847 656 25
134 217 728	27	0.000 000 007 450 580 596 923 828 125
268 435 456	28	0.000 000 003 725 290 298 461 914 062 5
536 870 912	29	0.000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0.000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0.000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0.000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0.000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0.000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0.000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0.000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0.000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0.000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0.000 000 000 001 818 989 403 545 856 475 830 078 125

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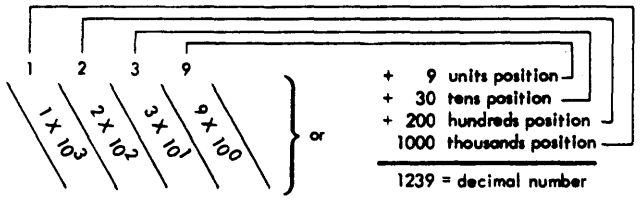
APPENDIX D BINARY AND HEXADECIMAL NUMBER NOTATION

Binary Number Notation

A binary number system, such as is used in System/360 uses a base of two. The concept of using a base of two can be compared with the base of ten (decimal) number system.

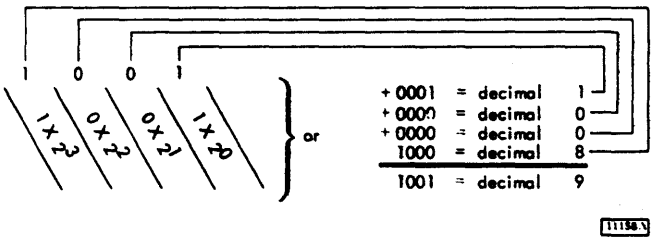
decimal number		binary number
0	=	0
1	=	1
2	=	10
3	=	11
4	=	100
5	=	101
6	=	110
7	=	111
8	=	1000
9	=	1001

Example of a decimal number



As shown above, the decimal number system allows counting to ten in each position-from units to tens to hundreds to thousands etc. The binary system allows counting to two in each position. Register displays in the System/360 are in binary form: a bit light on is a "one" a bit light off is a "zero".

Example of a binary number



Hexadecimal Number System

as been noted that binary numbers require about three times as many positions as decimal numbers to express the equivalent number. This is not much of a problem to the computer; however, in talking and writing or in communicating with the computer, these binary numbers are bulky. A long string of 1's and 0's cannot be effectively transmitted from one individual to another. Some shorthand method is necessary.

The hexadecimal number system fills this need. Because of the simple relationship of hexadecimal to binary, numbers can be converted from one system to another by inspection. The base or radix of the hexadecimal system is 16. This means there are 6 symbols: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F. The letters A, B, C, D, E, and F represent the 10-base system values of 10, 11, 12, 13, 14, and 15, respectively.

Four binary positions are equivalent to one hexadecimal position. The following table shows the comparable values of the three number systems.

Decimal	Binary	Hexadecimal
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

At this point, all 16 symbols have been used, and a carry to the next higher position of the number is necessary.

16	0001 0000	10
17	0001 0001	11
18	0001 0010	12
19	0001 0011	13
20	0001 0100	14
21	0001 0101	15

and so on.

Remember that as far as the internal circuitry of the computer is concerned, it only understands binary. But an operator can look at a series of lights on the computer console showing binary 1's and 0's, for example: 0001 1110 0001 0011, and say that the lights represent the hexadecimal value 1E13 which is easier to state than the string of 1's and 0's.

APPENDIX E HEXADECIMAL – DECIMAL CONVERSION TABLES

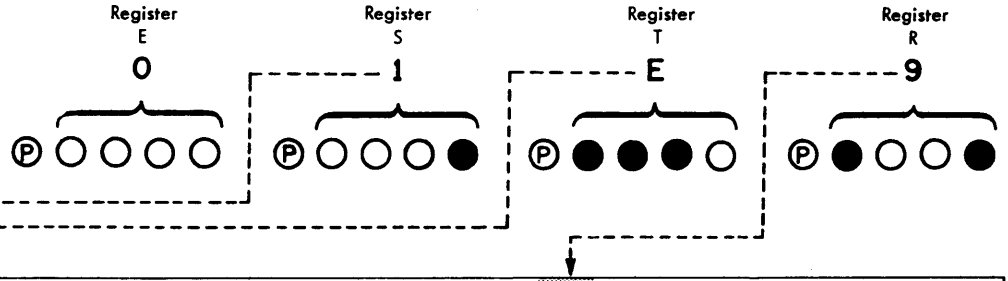
The table in this appendix provides for direct conversion of decimal and hexadecimal numbers in these ranges:

Hexadecimal	Decimal
000 to FFF	000 to 4095

For numbers outside the range of the table, add the following values to the table figures:

Hexadecimal	Decimal
1000	4096
2000	8192
3000	12288
4000	16384

Hexadecimal	Decimal
5000	20480
6000	24576
7000	28672
8000	32768
9000	36864
A000	40960
B000	45056
C000	49152
D000	53248
E000	57344
F000	61440



	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00 _	0000	0001	0002	0003	0004	0005	0006	0007	0008	0009	0010	0011	0012	0013	0014	0015
01 _	0016	0017	0018	0019	0020	0021	0022	0023	0024	0025	0026	0027	0028	0029	0030	0031
02 _	0032	0033	0034	0035	0036	0037	0038	0039	0040	0041	0042	0043	0044	0045	0046	0047
03 _	0048	0049	0050	0051	0052	0053	0054	0055	0056	0057	0058	0059	0060	0061	0062	0063
04 _	0064	0065	0066	0067	0068	0069	0070	0071	0072	0073	0074	0075	0076	0077	0078	0079
05 _	0080	0081	0082	0083	0084	0085	0086	0087	0088	0089	0090	0091	0092	0093	0094	0095
06 _	0096	0097	0098	0099	0100	0101	0102	0103	0104	0105	0106	0107	0108	0109	0110	0111
07 _	0112	0113	0114	0115	0116	0117	0118	0119	0120	0121	0122	0123	0124	0125	0126	0127
08 _	0128	0129	0130	0131	0132	0133	0134	0135	0136	0137	0138	0139	0140	0141	0142	0143
09 _	0144	0145	0146	0147	0148	0149	0150	0151	0152	0153	0154	0155	0156	0157	0158	0159
0A _	0160	0161	0162	0163	0164	0165	0166	0167	0168	0169	0170	0171	0172	0173	0174	0175
0B _	0176	0177	0178	0179	0180	0181	0182	0183	0184	0185	0186	0187	0188	0189	0190	0191
0C _	0192	0193	0194	0195	0196	0197	0198	0199	0200	0201	0202	0203	0204	0205	0206	0207
0D _	0208	0209	0210	0211	0212	0213	0214	0215	0216	0217	0218	0219	0220	0221	0222	0223
0E _	0224	0225	0226	0227	0228	0229	0230	0231	0232	0233	0234	0235	0236	0237	0238	0239
0F _	0240	0241	0242	0243	0244	0245	0246	0247	0248	0249	0250	0251	0252	0253	0254	0255
10 _	0256	0257	0258	0259	0260	0261	0262	0263	0264	0265	0266	0267	0268	0269	0270	0271
11 _	0272	0273	0274	0275	0276	0277	0278	0279	0280	0281	0282	0283	0284	0285	0286	0287
12 _	0288	0289	0290	0291	0292	0293	0294	0295	0296	0297	0298	0299	0300	0301	0302	0303
13 _	0304	0305	0306	0307	0308	0309	0310	0311	0312	0313	0314	0315	0316	0317	0318	0319
14 _	0320	0321	0322	0323	0324	0325	0326	0327	0328	0329	0330	0331	0332	0333	0334	0335
15 _	0336	0337	0338	0339	0340	0341	0342	0343	0344	0345	0346	0347	0348	0349	0350	0351
16 _	0352	0353	0354	0355	0356	0357	0358	0359	0360	0361	0362	0363	0364	0365	0366	0367
17 _	0368	0369	0370	0371	0372	0373	0374	0375	0376	0377	0378	0379	0380	0381	0382	0383
18 _	0384	0385	0386	0387	0388	0389	0390	0391	0392	0393	0394	0395	0396	0397	0398	0399
19 _	0400	0401	0402	0403	0404	0405	0406	0407	0408	0409	0410	0411	0412	0413	0414	0415
1A _	0416	0417	0418	0419	0420	0421	0422	0423	0424	0425	0426	0427	0428	0429	0430	0431
1B _	0432	0433	0434	0435	0436	0437	0438	0439	0440	0441	0442	0443	0444	0445	0446	0447
1C _	0448	0449	0450	0451	0452	0453	0454	0455	0456	0457	0458	0459	0460	0461	0462	0463
1D _	0464	0465	0466	0467	0468	0469	0470	0471	0472	0473	0474	0475	0476	0477	0478	0479
1E _	0480	0481	0482	0483	0484	0485	0486	0487	0488	0489	0490	0491	0492	0493	0494	0495
1F _	0496	0497	0498	0499	0500	0501	0502	0503	0504	0505	0506	0507	0508	0509	0510	0511

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	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
20 _	0512	0513	0514	0515	0516	0517	0518	0519	0520	0521	0522	0523	0524	0525	0526	0527
21 _	0528	0529	0530	0531	0532	0533	0534	0535	0536	0537	0538	0539	0540	0541	0542	0543
22 _	0544	0545	0546	0547	0548	0549	0550	0551	0552	0553	0554	0555	0556	0557	0558	0559
23 _	0560	0561	0562	0563	0564	0565	0566	0567	0568	0569	0570	0571	0572	0573	0574	0575
24 _	0576	0577	0578	0579	0580	0581	0582	0583	0584	0585	0586	0587	0588	0589	0590	0591
25 _	0592	0593	0594	0595	0596	0597	0598	0599	0600	0601	0602	0603	0604	0605	0606	0607
26 _	0608	0609	0610	0611	0612	0613	0614	0615	0616	0617	0618	0619	0620	0621	0622	0623
27 _	0624	0625	0626	0627	0628	0629	0630	0631	0632	0633	0634	0635	0636	0637	0638	0639
28 _	0640	0641	0642	0643	0644	0645	0646	0647	0648	0649	0650	0651	0652	0653	0654	0655
29 _	0656	0657	0658	0659	0660	0661	0662	0663	0664	0665	0666	0667	0668	0669	0670	0671
2A _	0672	0673	0674	0675	0676	0677	0678	0679	0680	0681	0682	0683	0684	0685	0686	0687
2B _	0688	0689	0690	0691	0692	0693	0694	0695	0696	0697	0698	0699	0700	0701	0702	0703
2C _	0704	0705	0706	0707	0708	0709	0710	0711	0712	0713	0714	0715	0716	0717	0718	0719
2D _	0720	0721	0722	0723	0724	0725	0726	0727	0728	0729	0730	0731	0732	0733	0734	0735
2E _	0736	0737	0738	0739	0740	0741	0742	0743	0744	0745	0746	0747	0748	0749	0750	0751
2F _	0752	0753	0754	0755	0756	0757	0758	0759	0760	0761	0762	0763	0764	0765	0766	0767
30 _	0768	0769	0770	0771	0772	0773	0774	0775	0776	0777	0778	0779	0780	0781	0782	0783
31 _	0784	0785	0786	0787	0788	0789	0790	0791	0792	0793	0794	0795	0796	0797	0798	0799
32 _	0800	0801	0802	0803	0804	0805	0806	0807	0808	0809	0810	0811	0812	0813	0814	0815
33 _	0816	0817	0818	0819	0820	0821	0822	0823	0824	0825	0826	0827	0828	0829	0830	0831
34 _	0832	0833	0834	0835	0836	0837	0838	0839	0840	0841	0842	0843	0844	0845	0846	0847
35 _	0848	0849	0850	0851	0852	0853	0854	0855	0856	0857	0858	0859	0860	0861	0862	0863
36 _	0864	0865	0866	0867	0868	0869	0870	0871	0872	0873	0874	0875	0876	0877	0878	0879
37 _	0880	0881	0882	0883	0884	0885	0886	0887	0888	0889	0890	0891	0892	0893	0894	0895
38 _	0896	0897	0898	0899	0900	0901	0902	0903	0904	0905	0906	0907	0908	0909	0910	0911
39 _	0912	0913	0914	0915	0916	0917	0918	0919	0920	0921	0922	0923	0924	0925	0926	0927
3A _	0928	0929	0930	0931	0932	0933	0934	0935	0936	0937	0938	0939	0940	0941	0942	0943
3B _	0944	0945	0946	0947	0948	0949	0950	0951	0952	0953	0954	0955	0956	0957	0958	0959
3C _	0960	0961	0962	0963	0964	0965	0966	0967	0968	0969	0970	0971	0972	0973	0974	0975
3D _	0976	0977	0978	0979	0980	0981	0982	0983	0984	0985	0986	0987	0988	0989	0990	0991
3E _	0992	0993	0994	0995	0996	0997	0998	0999	1000	1001	1002	1003	1004	1005	1006	1007
3F _	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023

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40 _	1024	1025	1026	1027	1028	1029	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039
41 _	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055
42 _	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071
43 _	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087
44 _	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103
45 _	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119
46 _	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135
47 _	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151
48 _	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167
49 _	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183
4A _	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199
4B _	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215
4C _	1216	1217	1218	1219	1220	1221	1222	1223	1224	1225	1226	1227	1228	1229	1230	1231
4D _	1232	1233	1234	1235	1236	1237	1238	1239	1240	1241	1242	1243	1244	1245	1246	1247
4E _	1248	1249	1250	1251	1252	1253	1254	1255	1256	1257	1258	1259	1260	1261	1262	1263
4F _	1264	1265	1266	1267	1268	1269	1270	1271	1272	1273	1274	1275	1276	1277	1278	1279
50 _	1280	1281	1282	1283	1284	1285	1286	1287	1288	1289	1290	1291	1292	1293	1294	1295
51 _	1296	1297	1298	1299	1300	1301	1302	1303	1304	1305	1306	1307	1308	1309	1310	1311
52 _	1312	1313	1314	1315	1316	1317	1318	1319	1320	1321	1322	1323	1324	1325	1326	1327
53 _	1328	1329	1330	1331	1332	1333	1334	1335	1336	1337	1338	1339	1340	1341	1342	1343
54 _	1344	1345	1346	1347	1348	1349	1350	1351	1352	1353	1354	1355	1356	1357	1358	1359
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56 _	1376	1377	1378	1379	1380	1381	1382	1383	1384	1385	1386	1387	1388	1389	1390	1391
57 _	1392	1393	1394	1395	1396	1397	1398	1399	1400	1401	1402	1403	1404	1405	1406	1407
58 _	1408	1409	1410	1411	1412	1413	1414	1415	1416	1417	1418	1419	1420	1421	1422	1423
59 _	1424	1425	1426	1427	1428	1429	1430	1431	1432	1433	1434	1435	1436	1437	1438	1439
5A _	1440	1441	1442	1443	1444	1445	1446	1447	1448	1449	1450	1451	1452	1453	1454	1455
5B _	1456	1457	1458	1459	1460	1461	1462	1463	1464	1465	1466	1467	1468	1469	1470	1471
5C _	1472	1473	1474	1475	1476	1477	1478	1479	1480	1481	1482	1483	1484	1485	1486	1487
5D _	1488	1489	1490	1491	1492	1493	1494	1495	1496	1497	1498	1499	1500	1501	1502	1503
5E _	1504	1505	1506	1507	1508	1509	1510	1511	1512	1513	1514	1515	1516	1517	1518	1519
5F _	1520	1521	1522	1523	1524	1525	1526	1527	1528	1529	1530	1531	1532	1533	1534	1535

11314

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62_	1568	1569	1570	1571	1572	1573	1574	1575	1576	1577	1578	1579	1580	1581	1582	1583
63_	1584	1585	1586	1587	1588	1589	1590	1591	1592	1593	1594	1595	1596	1597	1598	1599
64_	1600	1601	1602	1603	1604	1605	1606	1607	1608	1609	1610	1611	1612	1613	1614	1615
65_	1616	1617	1618	1619	1620	1621	1622	1623	1624	1625	1626	1627	1628	1629	1630	1631
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67_	1648	1649	1650	1651	1652	1653	1654	1655	1656	1657	1658	1659	1660	1661	1662	1663
68_	1664	1665	1666	1667	1668	1669	1670	1671	1672	1673	1674	1675	1676	1677	1678	1679
69_	1680	1681	1682	1683	1684	1685	1686	1687	1688	1689	1690	1691	1692	1693	1694	1695
6A_	1696	1697	1698	1699	1700	1701	1702	1703	1704	1705	1706	1707	1708	1709	1710	1711
6B_	1712	1713	1714	1715	1716	1717	1718	1719	1720	1721	1722	1723	1724	1725	1726	1727
6C_	1728	1729	1730	1731	1732	1733	1734	1735	1736	1737	1738	1739	1740	1741	1742	1743
6D_	1744	1745	1746	1747	1748	1749	1750	1751	1752	1753	1754	1755	1756	1757	1758	1759
6E_	1760	1761	1762	1763	1764	1765	1766	1767	1768	1769	1770	1771	1772	1773	1774	1775
6F_	1776	1777	1778	1779	1780	1781	1782	1783	1784	1785	1786	1787	1788	1789	1790	1791
70_	1792	1793	1794	1795	1796	1797	1798	1799	1800	1801	1802	1803	1804	1805	1806	1807
71_	1808	1809	1810	1811	1812	1813	1814	1815	1816	1817	1818	1819	1820	1821	1822	1823
72_	1824	1825	1826	1827	1828	1829	1830	1831	1832	1833	1834	1835	1836	1837	1838	1839
73_	1840	1841	1842	1843	1844	1845	1846	1847	1848	1849	1850	1851	1852	1853	1854	1855
74_	1856	1857	1858	1859	1860	1861	1862	1863	1864	1865	1866	1867	1868	1869	1870	1871
75_	1872	1873	1874	1875	1876	1877	1878	1879	1880	1881	1882	1883	1884	1885	1886	1887
76_	1888	1889	1890	1891	1892	1893	1894	1895	1896	1897	1898	1899	1900	1901	1902	1903
77_	1904	1905	1906	1907	1908	1909	1910	1911	1912	1913	1914	1915	1916	1917	1918	1919
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79_	1936	1937	1938	1939	1940	1941	1942	1943	1944	1945	1946	1947	1948	1949	1950	1951
7A_	1952	1953	1954	1955	1956	1957	1958	1959	1960	1961	1962	1963	1964	1965	1966	1967
7B_	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983
7C_	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999
7D_	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015
7E_	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031
7F_	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047

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80_	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063
81_	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079
82_	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095
83_	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111
84_	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127
85_	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143
86_	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159
87_	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175
88_	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191
89_	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207
8A_	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223
8B_	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239
8C_	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255
8D_	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271
8E_	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287
8F_	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303
90_	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319
91_	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335
92_	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351
93_	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367
94_	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383
95_	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399
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97_	2416	2417	2418	2419	2420	2421	2422	2423	2424	2425	2426	2427	2428	2429	2430	2431
98_	2432	2433	2434	2435	2436	2437	2438	2439	2440	2441	2442	2443	2444	2445	2446	2447
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9A_	2464	2465	2466	2467	2468	2469	2470	2471	2472	2473	2474	2475	2476	2477	2478	2479
9B_	2480	2481	2482	2483	2484	2485	2486	2487	2488	2489	2490	2491	2492	2493	2494	2495
9C_	2496	2497	2498	2499	2500	2501	2502	2503	2504	2505	2506	2507	2508	2509	2510	2511
9D_	2512	2513	2514	2515	2516	2517	2518	2519	2520	2521	2522	2523	2524	2525	2526	2527
9E_	2528	2529	2530	2531	2532	2533	2534	2535	2536	2537	2538	2539	2540	2541	2542	2543
9F_	2544	2545	2546	2547	2548	2549	2550	2551	2552	2553	2554	2555	2556	2557	2558	2559

11315

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A0 _	2560	2561	2562	2563	2564	2565	2566	2567	2568	2569	2570	2571	2572	2573	2574	2575
A1 _	2576	2577	2578	2579	2580	2581	2582	2583	2584	2585	2586	2587	2588	2589	2590	2591
A2 _	2592	2593	2594	2595	2596	2597	2598	2599	2600	2601	2602	2603	2604	2605	2606	2607
A3 _	2608	2609	2610	2611	2612	2613	2614	2615	2616	2617	2618	2619	2620	2621	2622	2623
A4 _	2624	2625	2626	2627	2628	2629	2630	2631	2632	2633	2634	2635	2636	2637	2638	2639
A5 _	2640	2641	2642	2643	2644	2645	2646	2647	2648	2649	2650	2651	2652	2653	2654	2655
A6 _	2656	2657	2658	2659	2660	2661	2662	2663	2664	2665	2666	2667	2668	2669	2670	2671
A7 _	2672	2673	2674	2675	2676	2677	2678	2679	2680	2681	2682	2683	2684	2685	2686	2687
A8 _	2688	2689	2690	2691	2692	2693	2694	2695	2696	2697	2698	2699	2700	2701	2702	2703
A9 _	2704	2705	2706	2707	2708	2709	2710	2711	2712	2713	2714	2715	2716	2717	2718	2719
AA _	2720	2721	2722	2723	2724	2725	2726	2727	2728	2729	2730	2731	2732	2733	2734	2735
AB _	2736	2737	2738	2739	2740	2741	2742	2743	2744	2745	2746	2747	2748	2749	2750	2751
AC _	2752	2753	2754	2755	2756	2757	2758	2759	2760	2761	2762	2763	2764	2765	2766	2767
AD _	2768	2769	2770	2771	2772	2773	2774	2775	2776	2777	2778	2779	2780	2781	2782	2783
AE _	2784	2785	2786	2787	2788	2789	2790	2791	2792	2793	2794	2795	2796	2797	2798	2799
AF _	2800	2801	2802	2803	2804	2805	2806	2807	2808	2809	2810	2811	2812	2813	2814	2815
B0 _	2816	2817	2818	2819	2820	2821	2822	2823	2824	2825	2826	2827	2828	2829	2830	2831
B1 _	2832	2833	2834	2835	2836	2837	2838	2839	2840	2841	2842	2843	2844	2845	2846	2847
B2 _	2848	2849	2850	2851	2852	2853	2854	2855	2856	2857	2858	2859	2860	2861	2862	2863
B3 _	2864	2865	2866	2867	2868	2869	2870	2871	2872	2873	2874	2875	2876	2877	2878	2879
B4 _	2880	2881	2882	2883	2884	2885	2886	2887	2888	2889	2890	2891	2892	2893	2894	2895
B5 _	2896	2897	2898	2899	2900	2901	2902	2903	2904	2905	2906	2907	2908	2909	2910	2911
B6 _	2912	2913	2914	2915	2916	2917	2918	2919	2920	2921	2922	2923	2924	2925	2926	2927
B7 _	2928	2929	2930	2931	2932	2933	2934	2935	2936	2937	2938	2939	2940	2941	2942	2943
B8 _	2944	2945	2946	2947	2948	2949	2950	2951	2952	2953	2954	2955	2956	2957	2958	2959
B9 _	2960	2961	2962	2963	2964	2965	2966	2967	2968	2969	2970	2971	2972	2973	2974	2975
BA _	2976	2977	2978	2979	2980	2981	2982	2983	2984	2985	2986	2987	2988	2989	2990	2991
BB _	2992	2993	2994	2995	2996	2997	2998	2999	3000	3001	3002	3003	3004	3005	3006	3007
BC _	3008	3009	3010	3011	3012	3013	3014	3015	3016	3017	3018	3019	3020	3021	3022	3023
BD _	3024	3025	3026	3027	3028	3029	3030	3031	3032	3033	3034	3035	3036	3037	3038	3039
BE _	3040	3041	3042	3043	3044	3045	3046	3047	3048	3049	3050	3051	3052	3053	3054	3055
BF _	3056	3057	3058	3059	3060	3061	3062	3063	3064	3065	3066	3067	3068	3069	3070	3071

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C0 _	3072	3073	3074	3075	3076	3077	3078	3079	3080	3081	3082	3083	3084	3085	3086	3087
C1 _	3088	3089	3090	3091	3092	3093	3094	3095	3096	3097	3098	3099	3100	3101	3102	3103
C2 _	3104	3105	3106	3107	3108	3109	3110	3111	3112	3113	3114	3115	3116	3117	3118	3119
C3 _	3120	3121	3122	3123	3124	3125	3126	3127	3128	3129	3130	3131	3132	3133	3134	3135
C4 _	3136	3137	3138	3139	3140	3141	3142	3143	3144	3145	3146	3147	3148	3149	3150	3151
C5 _	3152	3153	3154	3155	3156	3157	3158	3159	3160	3161	3162	3163	3164	3165	3166	3167
C6 _	3168	3169	3170	3171	3172	3173	3174	3175	3176	3177	3178	3179	3180	3181	3182	3183
C7 _	3184	3185	3186	3187	3188	3189	3190	3191	3192	3193	3194	3195	3196	3197	3198	3199
C8 _	3200	3201	3202	3203	3204	3205	3206	3207	3208	3209	3210	3211	3212	3213	3214	3215
C9 _	3216	3217	3218	3219	3220	3221	3222	3223	3224	3225	3226	3227	3228	3229	3230	3231
CA _	3232	3233	3234	3235	3236	3237	3238	3239	3240	3241	3242	3243	3244	3245	3246	3247
CB _	3248	3249	3250	3251	3252	3253	3254	3255	3256	3257	3258	3259	3260	3261	3262	3263
CC _	3264	3265	3266	3267	3268	3269	3270	3271	3272	3273	3274	3275	3276	3277	3278	3279
CD _	3280	3281	3282	3283	3284	3285	3286	3287	3288	3289	3290	3291	3292	3293	3294	3295
CE _	3296	3297	3298	3299	3300	3301	3302	3303	3304	3305	3306	3307	3308	3309	3310	3311
CF _	3312	3313	3314	3315	3316	3317	3318	3319	3320	3321	3322	3323	3324	3325	3326	3327
D0 _	3328	3329	3330	3331	3332	3333	3334	3335	3336	3337	3338	3339	3340	3341	3342	3343
D1 _	3344	3345	3346	3347	3348	3349	3350	3351	3352	3353	3354	3355	3356	3357	3358	3359
D2 _	3360	3361	3362	3363	3364	3365	3366	3367	3368	3369	3370	3371	3372	3373	3374	3375
D3 _	3376	3377	3378	3379	3380	3381	3382	3383	3384	3385	3386	3387	3388	3389	3390	3391
D4 _	3392	3393	3394	3395	3396	3397	3398	3399	3400	3401	3402	3403	3404	3405	3406	3407
D5 _	3408	3409	3410	3411	3412	3413	3414	3415	3416	3417	3418	3419	3420	3421	3422	3423
D6 _	3424	3425	3426	3427	3428	3429	3430	3431	3432	3433	3434	3435	3436	3437	3438	3439
D7 _	3440	3441	3442	3443	3444	3445	3446	3447	3448	3449	3450	3451	3452	3453	3454	3455
D8 _	3456	3457	3458	3459	3460	3461	3462	3463	3464	3465	3466	3467	3468	3469	3470	3471
D9 _	3472	3473	3474	3475	3476	3477	3478	3479	3480	3481	3482	3483	3484	3485	3486	3487
DA _	3488	3489	3490	3491	3492	3493	3494	3495	3496	3497	3498	3499	3500	3501	3502	3503
DB _	3504	3505	3506	3507	3508	3509	3510	3511	3512	3513	3514	3515	3516	3517	3518	3519
DC _	3520	3521	3522	3523	3524	3525	3526	3527	3528	3529	3530	3531	3532	3533	3534	3535
DD _	3536	3537	3538	3539	3540	3541	3542	3543	3544	3545	3546	3547	3548	3549	3550	3551
DE _	3552	3553	3554	3555	3556	3557	3558	3559	3560	3561	3562	3563	3564	3565	3566	3567
DF _	3568	3569	3570	3571	3572	3573	3574	3575	3576	3577	3578	3579	3580	3581	3582	3583

11316

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E0_	3584	3585	3586	3587	3588	3589	3590	3591	3592	3593	3594	3595	3596	3597	3598	3599
E1_	3600	3601	3602	3603	3604	3605	3606	3607	3608	3609	3610	3611	3612	3613	3614	3615
E2_	3616	3617	3618	3619	3620	3621	3622	3623	3624	3625	3626	3627	3628	3629	3630	3631
E3_	3632	3633	3634	3635	3636	3637	3638	3639	3640	3641	3642	3643	3644	3645	3646	3647
E4_	3648	3649	3650	3651	3652	3653	3654	3655	3656	3657	3658	3659	3660	3661	3662	3663
E5_	3664	3665	3666	3667	3668	3669	3670	3671	3672	3673	3674	3675	3676	3677	3678	3679
E6_	3680	3681	3682	3683	3684	3685	3686	3687	3688	3689	3690	3691	3692	3693	3694	3695
E7_	3696	3697	3698	3699	3700	3701	3702	3703	3704	3705	3706	3707	3708	3709	3710	3711
E8_	3712	3713	3714	3715	3716	3717	3718	3719	3720	3721	3722	3723	3724	3725	3726	3727
E9_	3728	3729	3730	3731	3732	3733	3734	3735	3736	3737	3738	3739	3740	3741	3742	3743
EA_	3744	3745	3746	3747	3748	3749	3750	3751	3752	3753	3754	3755	3756	3757	3758	3759
EB_	3760	3761	3762	3763	3764	3765	3766	3767	3768	3769	3770	3771	3772	3773	3774	3775
EC_	3776	3777	3778	3779	3780	3781	3782	3783	3784	3785	3786	3787	3788	3789	3790	3791
ED_	3792	3793	3794	3795	3796	3797	3798	3799	3800	3801	3802	3803	3804	3805	3806	3807
EE_	3808	3809	3810	3811	3812	3813	3814	3815	3816	3817	3818	3819	3820	3821	3822	3823
EF_	3824	3825	3826	3827	3828	3829	3830	3831	3832	3833	3834	3835	3836	3837	3838	3839
F0_	3840	3841	3842	3843	3844	3845	3846	3847	3848	3849	3850	3851	3852	3853	3854	3855
F1_	3856	3857	3858	3859	3860	3861	3862	3863	3864	3865	3866	3867	3868	3869	3870	3871
F2_	3872	3873	3874	3875	3876	3877	3878	3879	3880	3881	3882	3883	3884	3885	3886	3887
F3_	3888	3889	3890	3891	3892	3893	3894	3895	3896	3897	3898	3899	3900	3901	3902	3903
F4_	3904	3905	3906	3907	3908	3909	3910	3911	3912	3913	3914	3915	3916	3917	3918	3919
F5_	3920	3921	3922	3923	3924	3925	3926	3927	3928	3929	3930	3931	3932	3933	3934	3935
F6_	3936	3937	3938	3939	3940	3941	3942	3943	3944	3945	3946	3947	3948	3949	3950	3951
F7_	3952	3953	3954	3955	3956	3957	3958	3959	3960	3961	3962	3963	3964	3965	3966	3967
F8_	3968	3969	3970	3971	3972	3973	3974	3975	3976	3977	3978	3979	3980	3981	3982	3983
F9_	3984	3985	3986	3987	3988	3989	3990	3991	3992	3993	3994	3995	3996	3997	3998	3999
FA_	4000	4001	4002	4003	4004	4005	4006	4007	4008	4009	4010	4011	4012	4013	4014	4015
FB_	4016	4017	4018	4019	4020	4021	4022	4023	4024	4025	4026	4027	4028	4029	4030	4031
FC_	4032	4033	4034	4035	4036	4037	4038	4039	4040	4041	4042	4043	4044	4045	4046	4047
FD_	4048	4049	4050	4051	4052	4053	4054	4055	4056	4057	4058	4059	4060	4061	4062	4063
FE_	4064	4065	4066	4067	4068	4069	4070	4071	4072	4073	4074	4075	4076	4077	4078	4079
FF_	4080	4081	4082	4083	4084	4085	4086	4087	4088	4089	4090	4091	4092	4093	4094	4095

11317

Operation Codes					
Name	Mnemonic	Op Code		Class	Format
		Hexadecimal	Binary		
Branch on Condition	BCR	07	0000 0111	Branching	RR
Branch and Store	BASR	0D	0000 1101	Branching	RR
Add	AR	1A	0001 1010	Binary	RR
Subtract	SR	1B	0001 1011	Binary	RR
Store Halfword	STH	40	0100 0000	Binary	RX
Branch on Condition	BC	47	0100 0111	Branching	RX
Load Halfword	LH	48	0100 1000	Binary	RX
Compare Halfword	CH	49	0100 1001	Binary	RX
Add Halfword	AH	4A	0100 1010	Binary	RX
Subtract Halfword	SH	4B	0100 1011	Binary	RX
Branch and Store	BAS	4D	0100 1101	Branching	RX
*Diagnostic		83	1000 0011	Special	SI
Test under Mask	TM	91	1001 0001	Logical	SI
Move	MVI	92	1001 0010	Logical	SI
Set PSW	SPSW	81	1000 0001	Branching	SI
And	NI	94	1001 0100	Logical	SI
Compare	CLI	95	1001 0101	Logical	SI
Or	OI	96	1001 0110	Logical	SI
Halt & Proceed	HPR	99	1001 1001	Logical	SI
Test I/O and Branch	TIOB	9A	1001 1010	Input/Output	IO
Control I/O	CIO	9B	1001 1011	Input/Output	IO
Transfer I/O	XIO	D0	1101 0000	Input/Output	IO
Move Numerical	MVN	D1	1101 0001	Logical	SS
Move Characters	MVC	D2	1101 0010	Logical	SS
Move Zone	MVZ	D3	1101 0011	Logical	SS
Compare	CLC	D5	1101 0101	Logical	SS
Edit	ED	DE	1101 1110	Logical	SS
Move with Offset	MVO	F1	1111 0001	Decimal	SS
Pack	PACK	F2	1111 0010	Decimal	SS
Unpack	UNPK	F3	1111 0011	Decimal	SS
Zero and Add	ZAP	F8	1111 1000	Decimal	SS
Compare Decimal	CP	F9	1111 1001	Decimal	SS
Add Decimal	AP	FA	1111 1010	Decimal	SS
Subtract Decimal	SP	FB	1111 1011	Decimal	SS
Multiply Decimal	MP	FC	1111 1100	Decimal	SS
Divide Decimal	DP	FD	1111 1101	Decimal	SS
Translate	TR	DC	1101 1100	Logical	SS

* The Diagnostic instruction is used in special programs by the IBM Customer Engineer to verify the proper functioning of the CPU and to assist in locating faulty components. It is not intended for use in programs for normal applications and its use should be avoided, because the status of the CPU, the condition code, the contents of registers and main storage, and the progress of I/O operations may be affected.

11160B

APPENDIX G CONDITION CODE

Instruction	Condition Code Setting			
	00	01	10	11
Add	zero	< zero	> zero	--
Subtract	zero	< zero	> zero	--
Compare Halfword	equal	low	high	--
Add Halfword	zero	< zero	> zero	--
Subtract Halfword	zero	< zero	> zero	--
Zero & Add	zero	< zero	> zero	--
Compare Decimal	equal	low	high	--
Add Decimal	zero	< zero	> zero	overflow
Subtract Decimal	zero	< zero	> zero	overflow
Test under Mask	zero	mixed	--	all one
And	zero	not zero	--	--
Compare Logical	equal	low	high	--
Or	zero	not zero	--	--
Edit	zero	< zero	> zero	--
Transfer I/O	available	working	--	not operational

11161

Processing Operation	Format	Mnemonic	Timing (Average in microseconds with Time Sharing Switch On)
Branch on Condition	RR	BCR	78
Branch and Store	RR	BASR	94
Add	RR	AR	174
Subtract	RR	SR	183
Store Halfword	RX	STH	117
Branch on Condition	RX	BC	110
Load Halfword	RX	LH	124
Compare Halfword	RX	CH	223
Add Halfword	RX	AH	209
Subtract Halfword	RX	SH	216
Branch and Store	RX	BAS	124
Test Under Mask	SI	TM	132
Move	SI	MVI	104
Set PSW	SI	SPSW	149
And	SI	NI	123
Compare Logical	SI	CLI	122
Or	SI	OI	130
Halt and Proceed	SI	HPR	105
Move Numerical	SS	MVN	137 + 16N
Move Characters	SS	MVC	137 + 16N
Move Zone	SS	MVZ	137 + 16N
Compare Logical	SS	CLC	126 + 24B
Edit	SS	ED	$165 + 26N_1$
Move with Offset	SS	MVO	$170 + 10.2N_1 + 7.8N_2$ (if $N_1 > N_2$) $170 + 18.0N_1$ (if $N_1 \geq N_2$)
Translate	SS	TR	$148 + 53N_2$
Pack	SS	PACK	* $182 + 27N_2(\frac{N_2 + P_3}{2} - 1) + 16.8P_1 + 9.6N_1 - 4.8N_2$ * Use 182, if $2N_1 - (N_2 + 1)$ is > 0 Use 161, if $2N_1 - (N_2 + 1)$ is < 0
Unpack	SS	UNPK	$178 + 9.6N_1 + 8.4N_2 + P_4 (5 + 4.4N_1 - 8.4N_2)$
Compare Decimal	SS	CP	$312 + 13.2N_2 + (N_2 - 1)(69 + 15P_8) + (N_1 - N_2)$ $(38 + 9P_8) + 12P_6$
Add Decimal Subtract Decimal	SS SS	AP SP	$312 + 13.2N_2 + (N_2 - 1)(69 + 15P_5) + (N_1 - N_2)$ $(38 + 9P_5) + 12P_6 + P_7 (15 + 57N_1)$ (The formula is the same for both instructions)
Multiply Decimal	SS	MP	$215 + 20N_2 + (N_1 - N_2)(70 + 9.6N_2) + \Sigma Opl_{dig}$ $(39 + 9.6N_1 + 44N_2)$
Divide Decimal	SS	DP	$325 + 250N_2 + (N_1 - N_2)(150 + 250N_2) + \Sigma Q$ $(100 + 50N_2)$
Zero and Add	SS	ZAP	$210 + 10.2N_1 + 13.2N_2$

Notes: With time sharing switch OFF, and 22 usec to each instruction.
When effective address generation (Indexing) is used, add 56 usec for each generated address.

Symbols used in the timing formulas:

N	= Number of bytes in field (defined by coupled field length)
N_1	= Number of bytes in the first operand
N_2	= Number of bytes in the second operand
B	= Total number of bytes processed
ΣQ	= Sum of quotient digits
ΣOpl_{dig}	= Sum of operand 1 digits

The following constants must be placed into the respective formulas in the positions indicated by P_1 through P_8:

P_1 = 1 if $2N_1 - (N_2 + 1)$ is odd 0 if $2N_1 - (N_2 + 1)$ is even	P_4 = 1 if $N_1 + 1 - 2N_2$ is < 0 0 if $N_1 + 1 - 2N_2$ is ≥ 0	P_6 = 1 if $L_1 > L_2$ 0 if $L_1 = L_2$
P_2 = 1 if $N_1 = N_2 = 1$ 0 if other	P_5 = For Add: 1 if the signs of Oprd 1 and Oprd 2 differ 0 if the signs of both Oprds are alike For Subtract: 1 if the signs of both Oprds are alike 0 if the signs of Oprd 1 and 2 differ	P_7 = 1 if Recomplement desired 0 if No Recomplement desired
P_3 = 1 if N_2 is odd 0 if N_2 is even		P_8 = 1 if the signs of Oprd 1 and Oprd 2 are alike 0 if the signs of the Oprds differ

01205

Average CPU Time Required for Time-Shared Input/ Output Operations (Time in Milliseconds)

Machine	Operation	Timing Formula
2501	Card Read	0.065 · F
2520	Card Read	0.065 · F
2520	Card Punch	8.0
2560	Card Read	0.065 · F
2560	Card Punch	0.061 · F
2560	Card Print	H · 0.065 · F
2203	Print	TB · 0.0047 · F
1442	Card Punch	0.061 · F
1419	Read or Write	0.055 · F
CA	Transmit or Receive	0.070 · F

Symbols: F = Input/Output Field Length Specified in XIO Instruction.
H = Number of Print Heads Selected for Printing
TB = Number of Characters in the typebar.

11360B

I/O Device	Input/Output Operation	Format	Mnemonic	Timing (Average) in Microseconds
2501	Read Card	IO	XIO	186
2501	Test Reader Busy	IO	TIOB	112
2501	Test Reader Error	IO	TIOB	112
2520	Read Card	IO	XIO	190
2520	Punch Card	IO	XIO	172+24F+7(80-F)
2520	Punch and Feed	IO	XIO	172+24F+7(80-F)
2520	Test Reader Busy	IO	TIOB	112
2520	Test Reader Error	IO	TIOB	112
2520	Test Punch Busy	IO	TIOB	112
2520	Test Punch Error	IO	TIOB	112
2520	Test Last Card	IO	TIOB	112
2520	Test Feed Error	IO	TIOB	112
2520	Stacker Select	IO	CIO	112
2560	Read Card	IO	XIO	220
2560	Punch Card	IO	XIO	216
2560	Punch and Feed	IO	XIO	216
2560	Write Card	IO	XIO	224
2560	Test Rdr/Pch Busy	IO	TIOB	112
2560	Test Rdr/Pch Error	IO	TIOB	112
2560	Test Printer Busy	IO	TIOB	112
2560	Test Last Card	IO	TIOB	112
2560	Test Feed Error	IO	TIOB	136
2560	Stacker Select	IO	CIO	118
2560	Print Head Select	IO	CIO	116
1442	Punch Card	IO	XIO	183
1442	Test Punch Busy	IO	TIOB	112
1442	Test Punch Error	IO	TIOB	112
1442	Test Feed Error	IO	TIOB	112
2203	Print	IO	XIO	2100+45.2F
2203	Test Printer Busy	IO	TIOB	115
2203	Test Printer Error	IO	TIOB	115
2203	Test Chan 9 or 12	IO	TIOB	115
2203	Test Carriage Busy	IO	TIOB	115
2203	Control Carriage	IO	CIO	125
1403	Print (48 Char)	IO	XIO	2400+6.6F
1403	Print (Numeric)	IO	XIO	2400+10.5F
1403	Test Printer Busy	IO	TIOB	115
1403	Test Printer Error	IO	TIOB	115
1403	Test Chan 9 or 12	IO	TIOB	115
1403	Control Carriage	IO	CIO	120
1419	Read I/O Device	IO	XIO	187
1419	Write I/O Device	IO	XIO	204
1419	Test I/O Trans Line	IO	TIOB	112
1419	Unit Select	IO	CIO	112
1419	I/O Select	IO	CIO	110
Comm Adapter	Transmit	IO	XIO	190
	Receive	IO	XIO	190
	Test for Busy	IO	TIOB	120
	Test for Error	IO	TIOB	120
	Test EOT	IO	TIOB	115
	Test on BCD	IO	TIOB	115
	Receive Mode	IO	CIO	150
	Transmit Mode	IO	CIO	135
	Send EOT	IO	CIO	135
	Inhibit Aud Alarm	IO	CIO	120

01199

The following examples illustrate the use of System/360 instructions. Note that these examples closely approximate machine language to best illustrate the operation of the system. For clarity, the mnemonic for each operation code is used instead of the actual machine code. In addition, whenever possible, the contents of registers, storage locations, and so on, are given in decimal notation rather than the actual binary formats. When binary formats are used, they are segmented into bytes (eight bits) for ase of visual comparison.

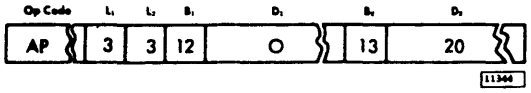
Decimal Add

The signed, packed decimal field at location 500-503 is to be added to the signed, packed decimal field at location 2000-2003.

Assume:

Reg 12	20 00
Reg 13	04 80
Loc 2000-2003 (before)	00 38 46 0-
Loc 500-503	01 12 34 5+

The instruction is:



Loc 2000-2003 (after) 00 73 88 5+
Condition code = 2; sum is greater than zero.

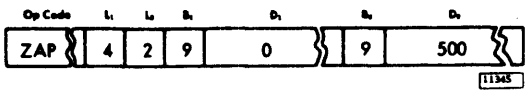
Zero and Add

The signed, packed decimal field at location 4500-4502 is to be moved to location 4000-4004 with four leading zeros in the result field.

Assume:

Reg 9	40 00
Loc 4000-4004 (before)	12 34 56 78 90
Loc 4500-4502	38 46 0-

The instruction is:



Loc 4000-4004 (after) 00 00 38 46 0-
Condition code = 1; sum is less than zero.

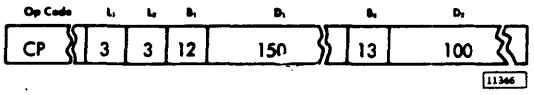
Compare Decimal

The contents of location 700-703 are to be compared algebraically with the contents of location 500-503.

Assume:

Reg 12	05 50
Reg 13	04 00
Loc 700-703	17 25 35 6+
Loc 500-503	06 72 14 2+

The instruction is:



Condition code = 2; first operand is high.

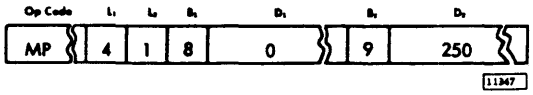
Multiply Decimal

The signed, packed decimal field in location 1200-1204 is to be multiplied by the signed, packed decimal field in location 500-501, and the product is to be placed in location 1200-1204.

Assume:

Reg 8	12 00
Reg 9	02 50
Loc 1200-1204 (before)	00 00 38 46 0-
Loc 500-501	32 1-

The instruction is:



Loc 1200-1204 (after) 01 23 45 66 0+
Condition code: unchanged.

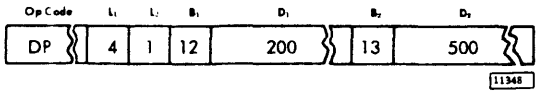
Divide Decimal

The signed, packed decimal field at location 2000-2004 is to be divided by the packed decimal field at location 3000-3001.

Assume:

Reg 12	18 00
Reg 13	25 00
Loc 2000-2004 (before)	01 23 45 67 8+
Loc 3000-3001	32 1-

The instruction is:



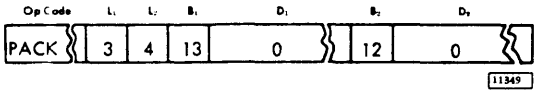
Loc 2000-2004 (after) 38 46 0- 01 8+
where the quotient is 38460-and the remainder is 018+
Condition code: unchanged.

Pack

Assume locations 1000-1004 contain the following:
Z1 Z2 Z3 Z4 S5
where Z = four-bit zone code
S = four-bit sign code
The field is to be in packed format with two leading zeros and placed in location 2500-2503.

Reg 12	10 00
Reg 13	25 00
Loc 1000-1004	Z1 Z2 Z3 Z4 S5
Loc 2500-2503 (before)	A B C D

The instruction is:



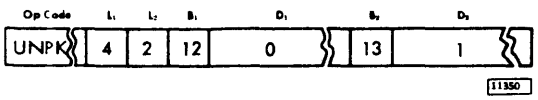
Loc 2500-2503 (after) 00 12 34 5S
Condition code: unchanged.

Unpack

Assume locations 2501-2503 contains the following fields:
12 34 5S
This field is to be put into zoned format and placed in the locations 1000-1004 where: S is a four-bit sign code.

Reg 12	10 00
Reg 13	25 00
Loc 2501-2503	12 34 5S
Loc 1000-1004 (before)	A B C D E

The instruction is:



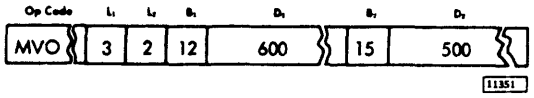
and results in
Loc 1000-1004 (after) Z1 Z2 Z3 Z4 S5
where Z is a four-bit zone code.
Condition code: unchanged.

Move with Offset

The unsigned three-byte field at location 4500-4502 is to be moved to location 5600-5603 and given the sign of the one byte field location at 5603.
Assume:

Reg 12	50 00
Reg 15	40 00
Loc 5600-5603 (before)	77 88 99 0+
Loc 4500-4502	12 34 56

The instruction is:



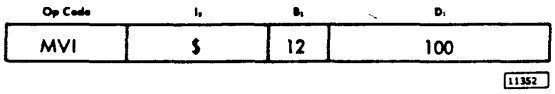
Loc 5600-5603 (after) 01 23 45 6+
Condition code: unchanged.

Move Immediate

A dollar sign ($) is to be placed in location 2100, leaving locations 2101-2105 unchanged. Let Z represent a four-bit zone.
Assume:

Reg 12	20 00
Loc 2100-2105 (before)	Z0 Z1 Z2 Z3 Z5 Z0

The instruction is:



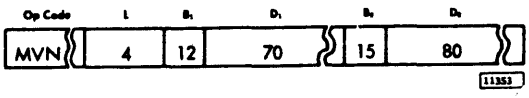
Loc 2100-2105 (after) $ Z1 Z2 Z3 Z5 Z0
Condition code: unchanged.

Move Numeric

Let Z and Y represent four-bit zones. The numeric parts of the eight-bit characters in the field at locations 6070-6074 are to be replaced by the numeric parts of eight-bit characters at locations 8080-8084.
Assume:

Reg 12	60 00
Reg 15	80 00
Loc 6070-6074 (before)	Y1 Y2 Y3 Y4 Y5
Loc 8080-8084	Z3 Z6 Z9 Z7 Z8

The instruction is:



Loc 6070-6074 (after) Y3 Y6 Y9 Y7 Y8
Condition code: unchanged.

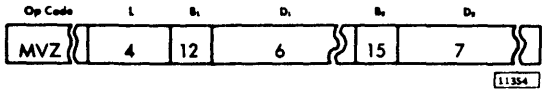
ve Zones

Let Z and Y represent four-bit zones in the eight-bit characters making up the fields at location 2006-2010 and 3007-3011, respectively. The zones of the field at 2006-2010 are to be replaced by the zones from location 3007-3011.

Assume:

Reg 12	20 00
Reg 15	30 00
Loc 2006-2010 (before)	Z1 Z4 Z7 Z8 Z5
Loc 3007-3011	Y8 Y7 Y4 Y6 Y8

The instruction is:



Loc 2006-2010 (after) Y1 Y4 Y7 Y8 Y5
Condition code: unchanged.

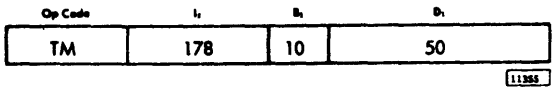
Test Under Mask

Test bit positions 0, 2, 3, and 6 of a given byte in storage to determine if all of these bit positions contain 1s. A Test Under Mask instruction with a mask of $10110010 = 178_{10}$ is used. The byte to be tested is stored at location 1250 and contains 01101101.

Assume:

Reg 10	12 00

The instruction is:



Mask from TM	10110010
Byte tested	01101101
Selected result	00100000

Condition code = 1; some selected bits are 0, some selected bits are 1 (mixed).

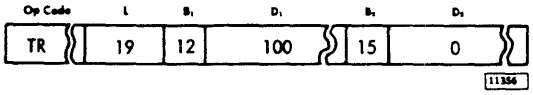
Translate

Assume a stream of 20 characters comes into location 2100 in EBCDIC. Translate to ASCII-8.

Assume:

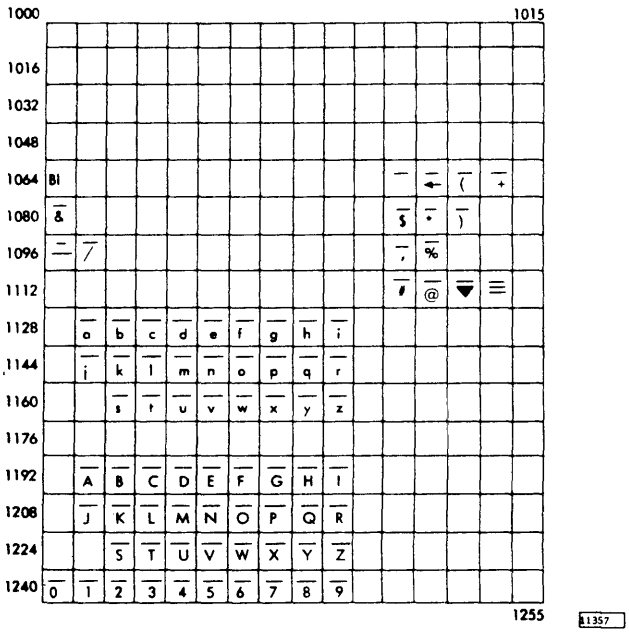
Reg 12	20 00
Reg 15	10 00
Loc 2100-2119 (before)	JOHN JONES 257 W.95

The instruction is:



Loc 2100-2119 (after) JOHN JONES 257 W. 95
where the overbar means the same graphic in ASCII-8
Condition code: unchanged.

Translate Table



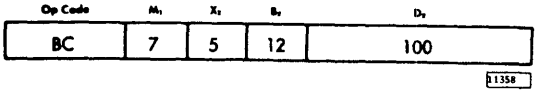
Branch On Condition

Assume a prior operation has been performed which resulted in setting the condition code in the PSW. The program is to branch if the result of the previous operation is nonzero.

The Branch On Condition instruction with a mask of $0111 = 7_{10}$ in the M_1 field becomes a Branch-on-Nonzero instruction.

Reg 5	00 00 01 00
Reg 12	00 04 00 00

The instruction is:



and causes a branch to location 410, provided the condition code is not zero.
Condition code setting is unchanged.

APPENDIX J 4-OF -8/EBCDIC CONVERSION TABLE

Graphic	4 of 8	EBCDIC
	NXOR 8 4 2 1	0 1 2 3 4 5 6 7
'	0 0 0 0 1 1 1 1	0 1 1 1 1 1 0 1
7	0 0 0 1 0 1 1 1	1 1 1 1 0 1 1 1
#	0 0 0 1 1 0 1 1	0 1 1 1 1 0 1 1
"	0 0 0 1 1 1 0 1	0 1 1 1 1 1 1 1
=	0 0 0 1 1 1 1 0	0 1 1 1 1 1 1 0
X	0 0 1 0 0 1 1 1	1 1 1 0 0 1 1 1
,	0 0 1 0 1 0 1 1	0 1 1 0 1 0 1 1
?	0 0 1 0 1 1 0 1	0 1 1 0 1 1 1 1
:	0 0 1 0 1 1 1 0	0 1 1 1 1 0 1 0
+	0 0 1 1 0 1 1 0	0 1 0 0 1 1 1 0
>	0 0 1 1 1 0 1 0	0 1 1 0 1 1 1 0
;	0 0 1 1 1 1 0 0	0 1 0 1 1 1 1 0
P	0 1 0 0 0 1 1 1	1 1 0 1 0 1 1 1
$	0 1 0 0 1 0 1 1	0 1 0 1 1 0 1 1
¬	0 1 0 0 1 1 0 1	0 1 0 1 1 1 1 1
-	0 1 0 0 1 1 1 0	0 1 1 0 0 0 0 0
(	0 1 0 1 0 1 1 0	0 1 0 0 1 1 0 1
_	0 1 0 1 1 0 1 0	0 1 1 0 1 1 0 1
)	0 1 0 1 1 1 0 0	0 1 0 1 1 1 0 1
C	0 1 1 0 0 0 1 1	1 1 0 0 0 0 1 1
E	0 1 1 0 0 1 0 1	1 1 0 0 0 1 0 1
F	0 1 1 0 0 1 1 0	1 1 0 0 0 1 1 0
I	0 1 1 0 1 0 0 1	1 1 0 0 1 0 0 1
¢	0 1 1 0 1 0 1 0	0 1 0 0 1 0 1 0
<	0 1 1 0 1 1 0 0	0 1 0 0 1 1 0 0
A	0 1 1 1 0 0 0 1	1 1 0 0 0 0 0 1
B	0 1 1 1 0 0 1 0	1 1 0 0 0 0 1 0
D	0 1 1 1 0 1 0 0	1 1 0 0 0 1 0 0
H	0 1 1 1 1 0 0 0	1 1 0 0 1 0 0 0
G	1 0 0 0 0 1 1 1	1 1 0 0 0 1 1 1
.	1 0 0 0 1 0 1 1	0 1 0 0 1 0 1 1
!	1 0 0 0 1 1 0 1	0 1 0 0 1 1 1 1

Graphic	4 of 8	EBCDIC
	NXOR 8 4 2 1	0 1 2 3 4 5 6 7
&	1 0 0 0 1 1 1 0	0 1 0 1 0 0 0 0
3	1 0 0 1 0 0 1 1	1 1 1 1 0 0 1 1
5	1 0 0 1 0 1 0 1	1 1 1 1 0 1 0 1
6	1 0 0 1 0 1 1 0	1 1 1 1 0 1 1 0
9	1 0 0 1 1 0 0 1	1 1 1 1 1 0 0 1
0	1 0 0 1 1 0 1 0	1 1 1 1 0 0 0 0
@	1 0 0 1 1 1 0 0	0 1 1 1 1 1 0 0
T	1 0 1 0 0 0 1 1	1 1 1 0 0 0 1 1
V	1 0 1 0 0 1 0 1	1 1 1 0 0 1 0 1
W	1 0 1 0 0 1 1 0	1 1 1 0 0 1 1 0
Z	1 0 1 0 1 0 0 1	1 1 1 0 1 0 0 1
none	1 0 1 0 1 0 1 0	1 1 1 0 0 0 0 0
%	1 0 1 0 1 1 0 0	0 1 1 0 1 1 0 0
/	1 0 1 1 0 0 0 1	0 1 1 0 0 0 0 1
S	1 0 1 1 0 0 1 0	1 1 1 0 0 0 1 0
U	1 0 1 1 0 1 0 0	1 1 1 0 0 1 0 0
Y	1 0 1 1 1 0 0 0	1 1 1 0 1 0 0 0
L	1 1 0 0 0 0 1 1	1 1 0 1 0 0 1 1
N	1 1 0 0 0 1 0 1	1 1 0 1 0 1 0 1
O	1 1 0 0 0 1 1 0	1 1 0 1 0 1 1 0
R	1 1 0 0 1 0 0 1	1 1 0 1 1 0 0 1
!	1 1 0 0 1 0 1 0	0 1 0 1 1 0 1 0
*	1 1 0 0 1 1 0 0	0 1 0 1 1 1 0 0
J	1 1 0 1 0 0 0 1	1 1 0 1 0 0 0 1
K	1 1 0 1 0 0 1 0	1 1 0 1 0 0 1 0
M	1 1 0 1 0 1 0 0	1 1 0 1 0 1 0 0
Q	1 1 0 1 1 0 0 0	1 1 0 1 1 0 0 0
1	1 1 1 0 0 0 0 1	1 1 1 1 0 0 0 1
2	1 1 1 0 0 0 1 0	1 1 1 1 0 0 1 0
4	1 1 1 0 0 1 0 0	1 1 1 1 0 1 0 0
8	1 1 1 0 1 0 0 0	1 1 1 1 1 0 0 0
blank	1 1 1 1 0 0 0 0	0 1 0 0 0 0 0 0

01209

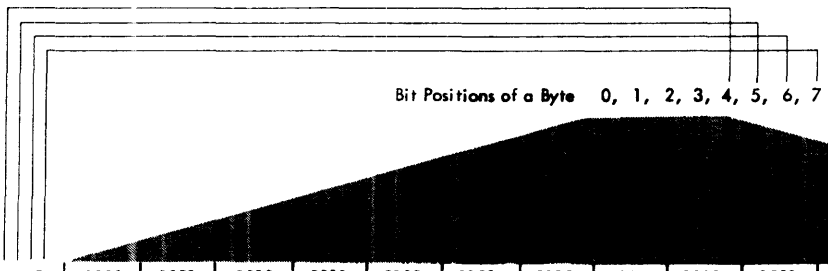
Graphic	EBCDIC	4 of 8
	0123 4567	NXOR 8421
blank	0100 0000	1111 0000
¢	0100 1010	0110 1010
.	0100 1011	1000 1011
<	0100 1100	0110 1100
(	0100 1101	0101 0110
+	0100 1110	0011 0110
!	0100 1111	1000 1101
&	0101 0000	1000 1110
!	0101 1010	1100 1010
$	0101 1011	0100 1011
*	0101 1100	1100 1100
)	0101 1101	0101 1100
;	0101 1110	0011 1100
¬	0101 1111	0100 1101
-	0110 0000	0100 1110
/	0110 0001	1011 0001
,	0110 1011	0010 1011
%	0110 1100	1010 1100
–	0110 1101	0101 1010
>	0110 1110	0011 1010
?	0110 1111	0010 1101
:	0111 1010	0010 1110
#	0111 1011	0001 1011
@	0111 1100	1001 1100
'	0111 1101	0000 1111
=	0111 1110	0001 1110
"	0111 1111	0001 1101
A	1100 0001	0111 0001
B	1100 0010	0111 0010
C	1100 0011	0110 0011
D	1100 0100	0111 0100
E	1100 0101	0110 0101

Graphic	EBCDIC	4 of 8
	0123 4567	NXOR 8421
F	1100 0110	0110 0110
G	1100 0111	1000 0111
H	1100 1000	0111 1000
I	1100 1001	0110 1001
J	1101 0001	1101 0001
K	1101 0010	1101 0010
L	1101 0011	1100 0011
M	1101 0100	1101 0100
N	1101 0101	1100 0101
O	1101 0110	1100 0110
P	1101 0111	0100 0111
Q	1101 1000	1101 1000
R	1101 1001	1100 1001
none	1110 0000	1010 1010
S	1110 0010	1011 0010
T	1110 0011	1010 0011
U	1110 0100	1011 0100
V	1110 0101	1010 0101
W	1110 0110	1010 0110
X	1110 0111	0010 0111
Y	1110 1000	1011 1000
Z	1110 1001	1010 1001
0	1111 0000	1001 1010
1	1111 0001	1110 0001
2	1111 0010	1110 0010
3	1111 0011	1001 0011
4	1111 0100	1110 0100
5	1111 0101	1001 0101
6	1111 0110	1001 0110
7	1111 0111	0001 0111
8	1111 1000	1110 1000
9	1111 1001	1001 1001

11340A

APPENDIX K CARD CODE TABLE

Extended Binary-Coded Decimal Interchange Code (EBCDIC) Card Code Table



4567	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
0000	TO9 18	TE9 18	EO9 18	TEO9 18	Blank	T &	E -	TEO	TO 18	TE 18	EO 18	TEO 18	TO	EO	O 28	O 0	0
0001	T9 1	E9 1	O9 1	9 1	TO9 1	TE9 1	01 /	TEO9 1	TO 1	TE 1	EO 1	TEO 1	T1 A	E1 J	EO9 1	1 1	1
0010	T9 2	E9 2	O9 2	9 2	TO9 2	TE9 2	EO9 2	TEO9 2	TO 2	TE 2	EO 2	TEO 2	T2 B	E2 K	02 S	2 2	2
0011	T9 3	E9 3	O9 3	9 3	TO9 3	TE9 3	EO9 3	TEO9 3	TO 3	TE 3	EO 3	TEO 3	T3 C	E3 L	03 T	3 3	3
0100	T9 4	E9 4	O9 4	9 4	TO9 4	TE9 4	EO9 4	TEO9 4	TO 4	TE 4	EO 4	TEO 4	T4 D	E4 M	04 U	4 4	4
0101	T9 5	E9 5	O9 5	9 5	TO9 5	TE9 5	EO9 5	TEO9 5	TO 5	TE 5	EO 5	TEO 5	T5 E	E5 N	05 V	5 5	5
0110	T9 6	E9 6	O9 6	9 6	TO9 6	TE9 6	EO9 6	TEO9 6	TO 6	TE 6	EO 6	TEO 6	T6 F	E6 O	06 W	6 6	6
0111	T9 7	E9 7	O9 7	9 7	TO9 7	TE9 7	EO9 7	TEO9 7	TO 7	TE 7	EO 7	TEO 7	T7 G	E7 P	07 X	7 7	7
1000	T9 8	E9 8	O9 8	9 8	TO9 8	TE9 8	EO9 8	TEO9 8	TO 8	TE 8	EO 8	TEO 8	T8 H	E8 Q	08 Y	8 8	8
1001	T9 18	E9 18	O9 18	9 18	T 18	E 18	O 18	18	TO 9	TE 9	EO 9	TEO 9	T9 I	E9 R	09 Z	9 9	9
1010	T9 28	E9 28	O9 28	9 28	T28 ¢	E28 !	TE 28	28 .	TO 28	TE 28	EO 28	TEO 28	TO9 28	TE9 28	EO9 28	TEO9 28	A
1011	T9 38	E9 38	O9 38	9 38	T38 .	E38 $	O38 ,	38 (	TO 38	TE 38	EO 38	TEO 38	TO9 38	TE9 38	EO9 38	TEO9 38	B
1100	T9 48	E9 48	O9 48	9 48	T48 <	E48 +	O48 %	48 @	TO 48	TE 48	EO 48	TEO 48	TO9 48	TE9 48	EO9 48	TEO9 48	C
1101	T9 58	E9 58	O9 58	9 58	T58 (	E58)	O58 _	58 '	TO 58	TE 58	EO 58	TEO 58	TO9 58	TE9 58	EO9 58	TEO9 58	D
1110	T9 68	E9 68	O9 68	9 68	T68 +	E68 ;	O68 >	68 =	TO 68	TE 68	EO 68	TEO 68	TO9 68	TE9 68	EO9 68	TEO9 68	E
1111	T9 78	E9 78	O9 78	9 78	T78 |	E78 ¬	O78 ?	78 "	TO 78	TE 78	EO 78	TEO 78	TO9 78	TE9 78	EO9 78	TEO9 78	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

Hexadecimal Representation for Bits 0 1 2 3 (Data Switch 1)

Hexadecimal Representation for Bits 4567 (Data Switch 2)

The numbers contained in the blocks represent row punches in the card.
"T" indicates a twelve zone punch.
"E" indicates an eleven zone punch.
EBCDIC graphic characters are shown in the shaded areas.

01207

ASCII Table

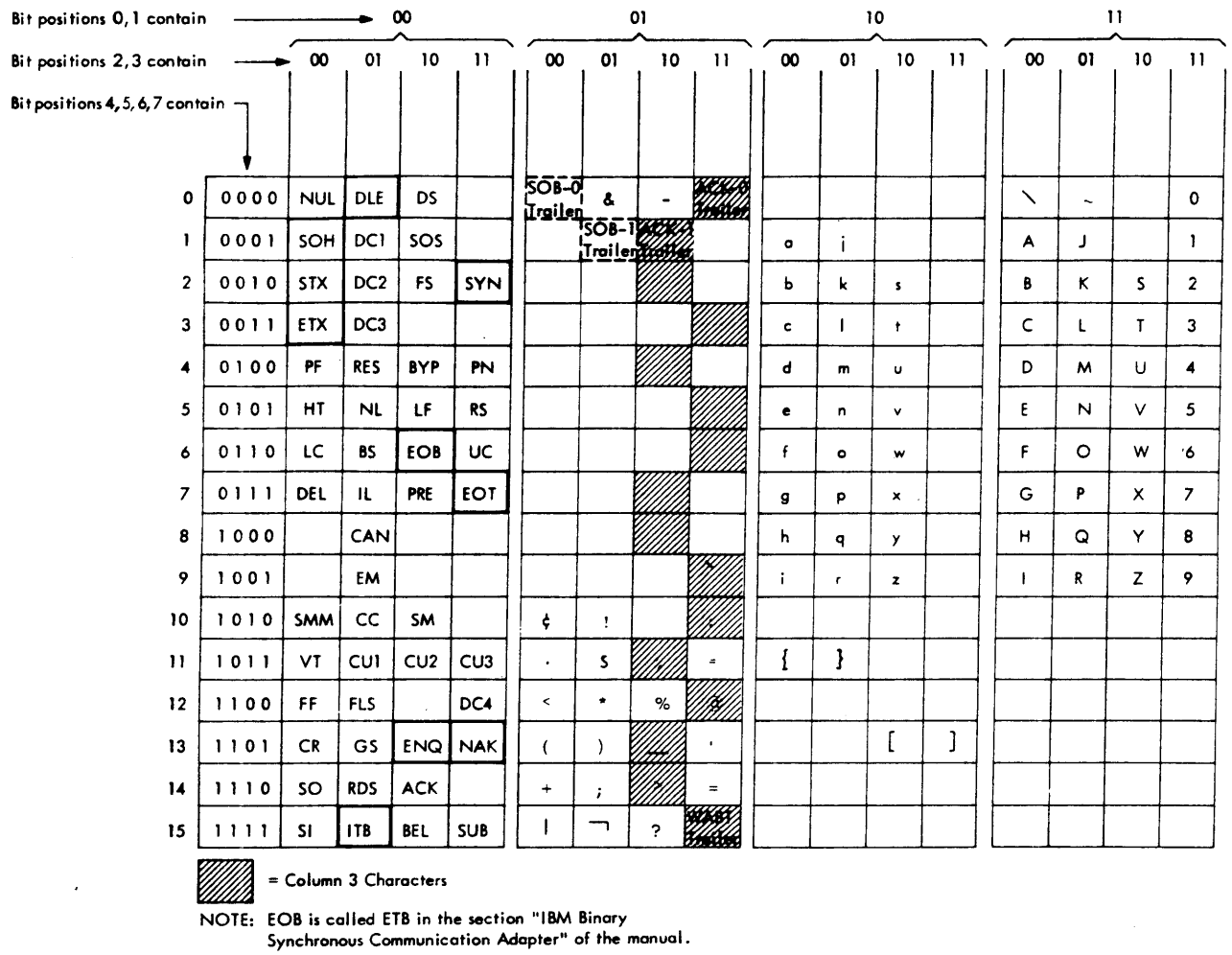
Row \ Column	0	1	2	3	4	5	6	7
Bits → 765 / 4321	000	001	010	011	100	101	110	111
0	0000 NUL	DLE	SOB-0 Trailer	ACK-0 Trailer	\	P	@	p
1	0001 SOH	DC1	SOB-1 Trailer	ACK-1 Trailer	A	Q	a	q
2	0010 STX	DC2	"	2	B	R	b	r
3	0011 ETX	DC3	#	3	C	S	c	s
4	0100 EOT	DC4	$	4	D	T	d	t
5	0101 ENQ	NAK	%	5	E	U	e	u
6	0110 ACK	SYN	&	6	F	V	f	v
7	0111 BEL	ETB	'	7	G	W	g	w
8	1000 BS	CAN	(	8	H	X	h	x
9	1001 HT	EM	)	9	I	Y	i	y
10	1010 LF	SS	*	:	J	Z	j	z
11	1011 VT	ESC	+	;	K	[	k	{
12	1100 FF	FS	,	<	L	~	l	¬
13	1101 CR	GS	-	=	M	]	m	}
14	1100 SO	RS	.	>	N	^	n	|
15	1111 SI	ITB	/	WACK Trailer	O	_	o	DEL

= Column 3 Characters

Figure L-1. ASCII Table

01259

EBCDIC Table



NOTE: EOB is called ETB in the section "IBM Binary Synchronous Communication Adapter" of the manual.

Figure L-2. EBCDIC Table

01261

Bit Position		Valid on XIO Insn during		Valid with Auto Call Insn
		TSM	REC	
0	TSM/REC Mode Error		X	
1	EOT Received		X	
2	CRC/LRC Check		X	
3	Timeout		X	X
4	Short Record (Field Length Zero)	X	X	
5	Storage Wraparound	X	X	X
6	Parity Check (VRC or BSCA Check)	X	X	
7	Overrun	X	X	

Figure L-3. BSCA Sense Byte Table

01257