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Systems

7070/7074 Compatibility Feature for IBM System/370 Models 165, 165 II, and 168

IBM

Preface

The IBM 7070/7074 Compatibility Feature, operating with a complementary set of programs, constitutes the 7074 emulator. Basically, the emulator is a hardware-aided simulator program. It operates much like an interpretive-routine simulator program, but at a speed about five times faster. With the emulator, System/370 Models 165, 165 II, and 168 can run 7070 and 7074 programs at speeds that, in general, equal or exceed those of the original systems.

PREREQUISITE PUBLICATIONS

The reader of this publication should be familiar with the information contained in the following publications:

IBM 7070-7074 Principles of Operation, GA22-7003
IBM System/370 System Summary, GA22-7001
IBM System/370 Principles of Operation, GA22-7000
7074 OS Emulator on System/370 Reference, GC27-6948.

ORGANIZATION OF THIS PUBLICATION

The information in this manual is organized as follows:

Following the Contents is a list of abbreviations and notation forms used in this publication.

The Introduction contains a general description of emulation and provides basic information on the compatibility feature and the emulator program.

The section "Emulator Organization" describes the functions of the compatibility feature and of the emulator program and their relationship to each other. This section also includes information on acceptable data formats and program/feature communication.

The section "Emulator Instruction Set" describes the format, application, and action of each instruction provided by the compatibility feature.

The Appendix contains information concerning conversion of graphics and internal codes.

Second Edition (June 1973)
This major revision obsoletes GA22-6958-0 and Technical Newsletter GN22-0428, and expands the scope of this manual to include System/370 Models 165 II and 168. Any significant technical change (addition, deletion, or revision) is indicated by a vertical bar to the left of the change.

Changes are periodically made to the specifications herein; before using this publication in connection with the operation of IBM systems, refer to the latest *IBM System/360 and System/370 Bibliography,* GA22-6822 and associated technical newsletters for the editions that are applicable and current.

Requests for copies of IBM publications should be made to your IBM representative or to the IBM branch office serving your locality.

This manual has been prepared by the IBM System Products Division, Product Publications, Dept. B98, PO Box 390, Poughkeepsie, N.Y. 12602. A form for readers' comments is provided at the back of this publication. If the form has been removed, comments may be sent to the above address. Comments become the property of IBM.

Contents

Abbreviations and Notation Forms

The abbreviations (other than the mnemonics of the instructions) and notation forms used in this manual are:

ADDR	operand address
B2, D2	second-operand base and displacement , respectively, of RS instruction format
BCD	binary-coded decimal
CS	control storage
C(x)	contents of x [example: C(GR 2)]
EBCDIC	extended binary-coded decimal interchange code
EOP	end of operation
FD	field definition
FPR	floating-point register
GM	group mark
GR	general register
hex	hexadecimal
I-unit	instruction unit
I/O	input/output
IC	instruction counter
IX	index word
K	= 1,024 (in System/370)
LLRR	long-length record runout
nRx	n times the contents of Rx (example: 8R1)
op code or OP	operation code
OS	operating system
PWL	partial word length
RDW	record definition word
RR	System/370 register-to-register instruction format
RM	recordmark
RS	System/370 register-and-storage instruction format
R1	first operand register of RR and RS instruction formats
R2	second operand register of the RR instruction format
R3	third operand register of the RS instruction format
S	sign
SM	segment mark
SS	System/370 storage-to-storage instruction format
TM	tapemark
WCS	writable control storage

When used with the emulator program, the IBM 7070/7074 compatibility feature facilitates the transition from IBM 7070 or 7074 Data Processing Systems to System/370. The compatibility feature adds special instructions to System/370. The emulator program employs these instructions, along with the System/370 universal instruction set to simulate 7070 and 7074 instructions. The compatibility feature and the emulator program together comprise the emulator.

With the emulator, each System/370 Model 165, 165 II, or 168 becomes, in effect, a 7074 that interprets and executes programs written for the 7070 or 7074. The term "7074" is used in this publication when no distinction is being made between the IBM 7070/7074 Data Processing Systems. Any 7070 programs which are not executable on a 7074 are also not executable with this emulator.

Installation of the 7074 compatibility feature does not affect normal operation of System/370 Model 165, 165 II, or 168.

PURPOSE OF THE EMULATOR

The 7074 emulator allows 7070 and 7074 users to reprogram gradually. The emulator is not intended as a substitute for reprogramming 7074 programs when reprogramming is economically justified. By designing new programs specifically for System/370, the user can take full advantage of the advanced features of System/370.

Emulator Organization

COMPATIBILITY-FEATURE COMPONENTS AND FUNCTIONS

The compatibility feature may be considered as having four major components: the operation-code converter, the address converter, the emulator instruction set, and the data translator. In addition, the compatibility feature provides associated indicators which can be displayed on the system microfiche viewer.

Operation-code Converter

The operation-code converter analyzes each 7074 operation code and develops from it a System/370 24-bit binary address. This address and the branch table relocate factor (FPR 0 bytes 4-7) are added, and the result is used to fetch the emulator program routine address from the branch table and to load it into GR 6. The simulated 7074 storage and 7074 instruction subroutines are separately relocatable under OS control. In this manner, each 7074 operation code causes the emulator program to begin execution at the unique address associated with that operation code. The addresses produced by the operation-code converter are on word boundaries.

Address Converter

The address converter analyzes the contents of the address portion of each 7074 instruction as it is fetched, and then develops a corresponding System/370 converted 24-bit binary address from it. The 10,000 decimal addresses require a block of 10,234 doublewords. Consecutive decimal addresses are not necessarily converted to consecutive doubleword addresses, but odd decimal addresses are converted to odd doubleword addresses, and even decimal addresses are converted to even doubleword addresses. The conversion process includes a self-check of the address converter and validity test of the 7074 address to be converted. An address-converter error results in a machine-check interruption; a non-decimal digit in the address to be converted results in a program interruption because of invalid data.

When a System/370 is operating in relocate mode, any System/370 address generated by the emulator is a virtual address.

Emulator Instruction Set

The emulator instruction set contains (1) interpretive instructions that operate on 7074 data or instructions to make them usable by System/370 and (2) instructions that are direct counterparts of certain 7074 instructions. Examples of the first type of instruction are DIL (Do Interpretive Loop), ECA (Convert Address), and ELB (Load Buffer). Examples of the second type are EBIX (Branch Incremented Index), ERG (Record Gather), and ELL (Lookup Lowest).

Data Translator

This component translates extended binary-coded decimal interchange code (EBCDIC) to 7074 code (for tape read) and 7074 code to EBCDIC (for tape write). (See Figures A4 and A5). In either case, 7074-to-EBCDIC or EBCDIC-to-7074, an intermediate code is generated by the translator. The value is added to the original value, producing the desired translation.

Indicators

The compatibility feature provides indicators that are used during emulation. These are displayed on the system microfiche viewer.

Model 165 Indicators

Displayed	*Microfiche Frame B6 Line*
Writable control storage (WCS) bits 108-125	B
Status valid, STATW, STATX, STATY, STATZ, and Misc 4 to LSAL	D
WCS parity error	K

Model 165 II and 168 Indicators

Displayed	*Microfiche Frame B6 Line*
Control Storage (CS) bits 108-125	B
Status valid, STATW, STATX, STATY, STATZ, and Misc 4 to LSAL	D
Page checks	H
Page remembers	J
CS checks	K

EMULATOR PROGRAM FUNCTIONS

The emulator program is an interpretive simulator that uses the compatibility feature and other System/370 facilities. It includes appropriate routines for interpreting and simulating 7074 instructions and for providing the control and communication facilities required by the emulator. The emulator program uses the emulator instruction set and the universal instruction set to provide routines that simulate the execution-time actions of those 7074 instructions that are emulated. These routines are entered via the operation-code converter (described earlier). In general, communication between the emulator program and the compatibility feature is through the general registers (GR's) and the floating-point registers (FPR's), and an area of main storage defined as the communication region. The use of most registers depends on the instruction being executed; however, certain register assignments are fixed by the design of the compatibility feature.

REGISTER ASSIGNMENTS

The general and floating-point registers are used by the compatibility feature for communicating with the emulator program. GR's 12-15 are not used by the compatibility feature. The assignments of the remaining registers are as follows:

GR's 0-1

These two registers are used as result registers by the load buffer and unload buffer instructions.

GR 2

This register contains the binary address of the index word specified in positions 4 and 5 of the 7074 instruction. On load or unload buffer instructions, GR 2 contains the binary address of the buffer being used.

GR 3

This register contains the binary address of the 7074 word addressed by the modified 7074 instruction. On either a load or unload buffer instruction, GR 3 contains the count of the bytes in the System/370 buffer.

GR's 4-5

Each of these two registers is used as a pointer by the ETMB instruction (described later).

GR 6

This register contains the routine address upon completion of the DIL instruction.

GR 7

This register is used as a base register for addressing the simulated accumulators in simulated 7074 storage. GR 7 will contain the address of accumulator 1. Accumulators 2 and 3 may be addressed using GR 7 as a base with displacements of 8 and 16, respectively.

Note: Simulated 7074 storage locations 9994-9997 may be used as work areas by certain instructions. These locations can be addressed using GR 7 as a base register and adding the appropriate displacement.

GR's 8-9

These registers are used to store record definition words (RDW's) in table lookup, load buffer, unload buffer, record gather, record scatter, and all edit instructions.

GR's 10-11

These registers contain the 7074 instruction currently being simulated. GR 10 contains the contents of digits 0-5 of the 7074 instruction; GR 11 contains the 7074 effective operand address and the sign of the 7074 instruction.

FPR 0

This register contains the flags, counters, and factors shown in Figure 1.

FPR 2

This register simulates the 7074 overflow, sign change, and high-low-equal indicators. Each indicator is simulated by one byte of the register. Figure 1 illustrates the register format for indicator simulation. Each byte has four possible settings, as illustrated in Figure 2.

FPR 4

This register contains the interrupt routine address and 7074 storage relocation factor, as shown in Figure 1.

7074 PROGRAM ERROR CHECKING

The emulator includes checking for the following 7074 program errors by the specified instructions. For all program errors, the operation is terminated and a System/370 branch takes place to the address formed by adding decimal 64 to the contents of FPR 4 bytes 1-3.

Field Start Greater Than Stop: Digit four of the 7074 word in GR's 10 and 11 is larger than digit five of the 7074 word.

Instructions affected: EFD, EFST, ELL, ELE, ELEH, EMAD.

For the definitions of the mnemonics, see Figure 5.

FPR	Byte 0 0 1 2 3 4 5 6 7	Byte 1 8 9 10 11 12 13 14 15	Byte 2 16 17 18 19 20 21 22 23	Byte 3 24 25 26 27 28 29 30 31	Byte 4 32 33 34 35 36 37 38 39	Byte 5 40 41 42 43 44 45 46 47	Byte 6 48 49 50 51 52 53 54 55	Byte 7 56 57 58 59 60 61 62 63
0	DIL Trap and Count Flags	DIL Counter	7074 Instruction Counter (IC)		00	7074 Op Code Branch Table Relocation Factor		
2	Acc 1 Overflow	Acc 2 Overflow	Acc 3 Overflow	Sign Change	Field Overflow	High Compare	Equal Compare	Low Compare
4	00	Interrupt Routine Address			00	7074 Storage Relocation Factor		
6	Compatibility Feature Working Register							

Figure 1. Floating-point Register Assignments

Byte Setting	Corresponding Indicator Setting	7074 Mode
00	Off	Sense
0F	Off	Halt
F0	On	Sense
FF	On	Halt

Figure 2. FPR 2 Indicator Settings

RDW Start Greater Than Stop: Decimal address in digits 2-5 of the RDW is larger than the decimal address in digits 6-9 of the same RDW (7074 format). The RDW can be any in a sequential list of RDW's, the first of which is specified by the decimal address in digits 6-9 of the 7074 word in GR 10 and GR 11.

Instructions affected: ERG, ERS, ELL, ELE, ELEH, EAN, ENA, ENB, ENS.

RDW Alpha Sign: Any of the 7074 format RDW's described in "RDW Start Greater Than Stop," having an alpha sign (1110).

Instructions affected: Same as "RDW Start Greater Than Stop."

Noneven Word Count on Edit RDW: An RDW in which the difference between the decimal stop address (digits 6-9) and the decimal start address (digits 2-5) is a multiple of two.

Instructions affected: EAN, ENA, ENB, and ENS.

Instruction Word Alpha: The 7074 word fetched via the 7074 instruction counter has an alpha sign.

Instruction affected: DIL.

Increment Factor in Location 0098 Equals Zero: Digits 6-9 of the 7074 word are equal to zero.

Instructions affected: ELL, ELE, and ELEH.

Index Word Zero: Digits 4 and 5 of the 7074 word in GR 10 and GR 11 are equal to zero.

Instructions affected: EAN, ENA, ENB, ENS, ESC (Shift Left and Count only), EBDX, EBIX, EXA, EXS, ERG, ERS.

Shift Greater Than Ten: Digits 8 and 9 of the 7074 word in GR 10 and GR 11 have a decimal value greater than 10.

Instruction affected: ESC.

Invalid Shift Instruction: Digit 7 of 7074 shift instruction not 0, 1, 2, or 3.

Instruction affected: ESC.

Index Word Alpha: The 7074 index word fetched during DIL has an alpha sign.

Instruction affected: DIL.

Abort Routine: See the EUB and EUBR instructions.

DATA REPRESENTATION

The IBM 7074 uses an internal 2-out-of-5 code to represent a decimal digit; IBM System/370 uses four bits to represent a decimal digit, packed two per byte. Therefore, each 7074 2-out-of-5-code digit is represented by a corresponding System/370 packed decimal digit with zero represented as 0000 in binary. The checking that the 2-out-of-5 code provided in the 7074 is replaced by the parity checking in System/370. The only "loss" incurred by simulating digit-for-digit rather than bit-for-bit is the ability to simulate the diagnostic instructions of the 7074.

Numeric data is represented in packed decimal format (Figure 3) where each 4-bit digit corresponds to a 7074 digit. Alphameric data is also represented in packed decimal format. However, two 4-bit BCD digits are required to represent a correponding two-digit 7074 alphameric character. The sign character is 1100 for plus, 1101 for minus, and 1110 for alpha. System/370 must be in the EBCDIC mode. Bits 0-3 of byte 6 are always 0000.

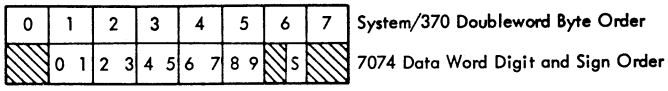


Figure 3. Data Word Format

Instruction data is also represented by "4-bit binary-coded decimal" (BCD) digits, packed two per byte (Figure 4).

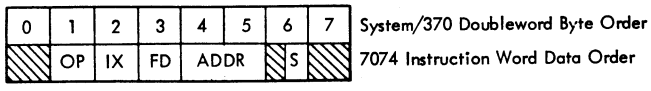


Figure 4. Instruction Word Format

Bits 0-3 of byte 6 are always 0000. The operation code (OP) is in byte 1, the index word (IX) is in byte 2, the field definition (FD) in byte 3, the operand address (ADDR) in bytes 4 and 5, and the sign (S) in bits 4-7 of byte 6.

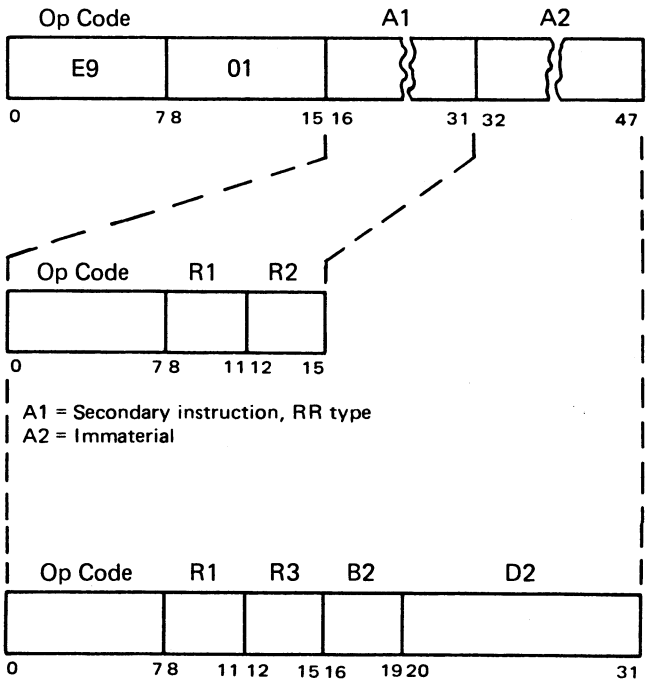
Exceptions

Four types of exceptions are referred to in this publication: operation, specification, data, and access. For the Model 165, access exceptions include both the protection and addressing exceptions. For Models 165 II and 168, access exceptions include not only the protection and addressing exceptions but also the segment-translation, page-translation, and translation-specification exceptions.

This section contains the formats and descriptions of the primary and secondary instructions, and types of exceptions to which these instructions are susceptible. Figure 5 summarizes the secondary instructions.

EMU (Emulator-Feature Instruction)

SS Format



A1 + A2 = Secondary instruction, RS type

Exceptions:

Access
Operation
Specification

System/370 Models 165, 165 II, and 168 emulate 7074 instructions via the emulator instruction (EMU). This System/370 instruction, the only primary instruction of this feature, has a special SS format. The first byte contains the op code, the second byte contains the emulator flag, and the next four bytes contain any of the RR- or RS-format secondary instructions. The first two bytes are, in effect, a prefix for each of the secondary instructions.

The EMU instruction causes a specification exception if it is the subject of the System/370 Execute (EX) instruction.

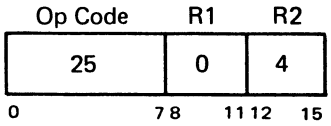
Before executing a secondary instruction, the EMU instruction examines the emulator status trigger. If it is on, EMU proceeds directly to the secondary instruction. If it is off, EMU examines bits 8-15; if these bits contain 0000 0001 (hex 01), the EMU status valid trigger is turned on, and the instruction then proceeds to a secondary instruction. If the bits do not contain hex 01, a specification exception (Model 165) or operation exception (Model 165 II or 168) occurs.

The secondary instructions, in conjunction with the System/370 instruction set, perform the 7074 functions as instructions listed in Figure 5. The R1, R2, and R3 fields are used in some of these instructions as modifiers to the operation code. Many instructions require some fixed value to ensure operation.

If a secondary instruction turns an indicator on or off, the indicator is noted at the end of the instruction description. An indicator can be a light, or it can be a byte in an FPR; differentiation is made by identifying the indicator lights.

DIL (Do Interpretive Loop)

RR Format



Exceptions:

Access
Data

Description

The DIL instruction provides control over the emulation process. It simulates the operation of the 7074 instruction counter (IC) by fetching and initiating operations as they occur in the 7074 systems. DIL replaces the subroutine that a programmed simulator would use to:

1. Access the simulated IC.
2. Convert the simulated IC address to the address of the storage location that contains the next instruction to be interpreted.
3. Fetch the next 7074 instruction.

Secondary Instructions	Mnemonic	Type	Op Code	R1	R2 or R3	Exceptions
Do Interpretive Loop	DIL	RR	25	0	4	a, d
Add	EA	RS	B6		0	a, d
Branch Decremented Index	EBDX	RS	AC	A	1	a, d
Branch Incremented Index	EBIX	RS	AC	A	0	a, d
Branch on Indicator	EBI	RR	10			d
Compare	EC	RS	B6		2	a, d
Convert Address	ECA	RS	AE	0	0	a, d
Edit Alphameric to Numeric	EAN	RS	B5	8	4	a, d
Edit Numeric to Alphameric	ENA	RS	A9	8	0	a, d
Edit Numeric to Alpha with Blank Insertion	ENB	RS	A9	8	2	a, d
Edit Numeric to Alpha with Sign Control	ENS	RS	A9	8	1	a, d
Field Definition	EFD	RS	BD		A	a, d
Field Store	EFST	RS	AB	A	ctrl	a, d
Index Add	EXA	RS	BA	A	0	a, d
Index Subtract	EXS	RS	BA	A	1	a, d
Load Buffer	ELB	RS	A0	8	X	a, d
Load Buffer, Record Mark Control	ELBR	RS	A1	8	X	a, d
Load Buffer with Zero Elimination	ELBZ	RS	A2	8	X	a, d
Load Buffer with Zero Elimination and per Record Mark	ELBC	RS	B8	8	X	a, d
Lookup Equal or High	ELEH	RS	BF	8	2	a, d
Lookup Equal Only	ELE	RS	BF	8	1	a, d
Lookup Lowest	ELL	RS	BF	8	0	a, d
Move Accumulator Digits	EMAD	RS	AB	A	C	a, d
Record Gather	ERG	RS	AF	8	8	a, d
Record Scatter	ERS	RS	AF	8	9	a, d
Set Instruction Counter	SIC	RR	11			d
Shift Control	ESC	RS	AD	B	X	a, d
Subtract	ES	RS	B6		1	a, d
Test Under Mask and Branch	ETMB	RS	B3			a
Transfer Condition to Indicator	ETCI	RR	20	2		
Unload Buffer	EUB	RS	AA	8	0	a, d
Unload Buffer per Record Mark	EUBR	RS	AA	8	1	a, d
Unsigned Decimal Add	EUNA	RS	A3			a, d
Unsigned Decimal Subtract	EUNS	RS	B0			a, d

a Access exception
d Data exception
x Don't care

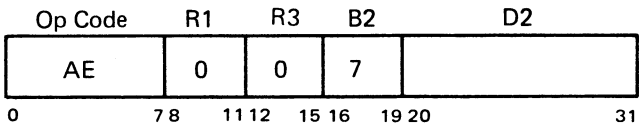
Figure 5. Emulator Instruction Set Summary

4. Update and restore the simulated IC.
5. Perform any indexing required for the 7074 instruction.
6. Convert the effective address obtained to the address of the storage location containing the 7074 operand.
7. Interpret the 7074 instruction op code, and branch to the appropriate simulator routine which simulates the instruction.

A description of the DIL instruction operation is shown schematically in Figure 6. In the execution of the DIL instruction, both the 7074 instruction-word sign and the index-word sign are examined. If either is an alpha, a 7074 program error condition is raised. The execution of the DIL is then terminated, and a branch is made to the 7074 interrupt routine address plus decimal 64. The 7074 IC and the DIL counter are then updated, and the 7074 instruction is loaded into GR 10 and GR 11.

ECA (Convert Address)

RS Format



Source Address = B2 + D2
Destination Address = GR 10
Exceptions:
Access
Data

Description

The decimal address from digits 6-9 of the 7074 source word is converted to a System/370 binary address (with a 7074 storage relocation factor) and stored in GR 10.

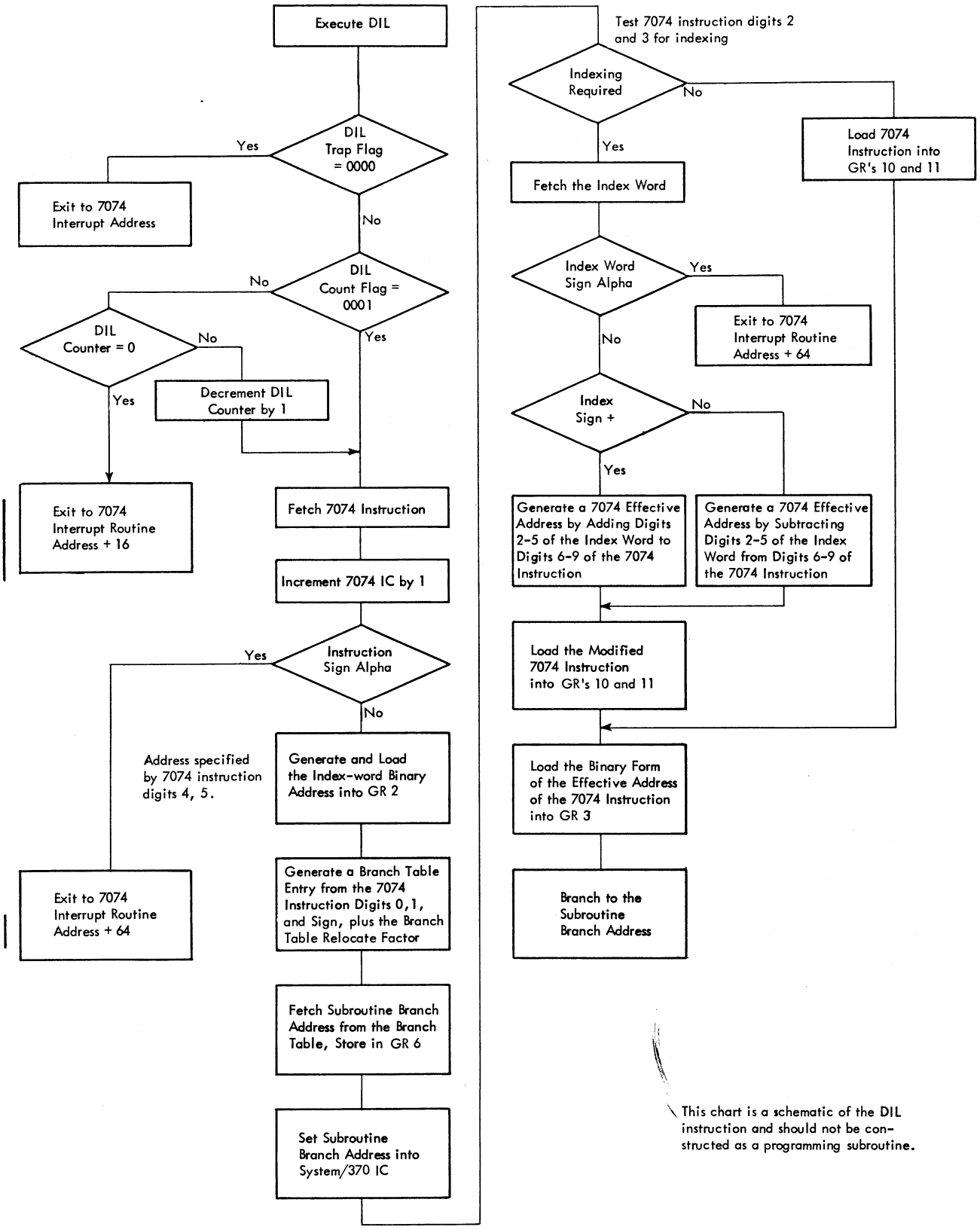
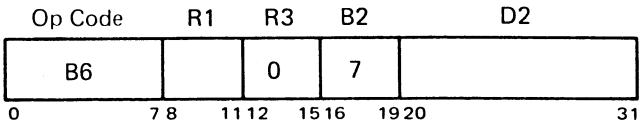


Figure 6. DIL Instruction Internal Logic

EA (Add)

RS Format



Source Address = B2 + D2
Destination Address = 8R1 + C(GR 7)
Exceptions:
Access
Data

Description

The source word is added to the destination word, and the sum is stored at the destination address. If either word has an alpha sign, the word is considered positive for the addition, but the result is given an alpha sign.

If the signs are unlike and either is minus, the source word is complemented and added to the destination word. If the magnitude of the source word was larger than the magnitude of the destination word, the result is recomplemented and the destination sign is changed, unless it is alpha.

If the result is zero, then the destination sign is changed, provided neither sign is alpha and the EMAD overflow indicator (byte 3 of GR 11) is on.

Indicators

The 7074 indicators in FPR 2 are set as shown in Figure 7.

Indicators	R1 Field	D2 Field (÷8)	Additional Conditions
0 (Acc 1 Overflow)	0000	00xx	Carry from high-order digit
1 (Acc 2 Overflow)	0001	00xx	Carry from high-order digit
2 (Acc 3 Overflow)	0010	00xx	Carry from high-order digit
4 (Field Overflow)	0100	00xx.	Carry from high-order digit
3 (Sign Change)	0100	00xx	(See note 1)
3 (Sign Change)	0100	00xx	(See note 2)
3 (Sign Change)	0100	00xx	(See note 3)

Note 1: The destination sign must be alpha, the source sign must be minus for EA but plus for ES, the magnitude of the source word must be greater than the magnitude of the destination word, and the destination field may not extend from positions 0 to 9.

Note 2: The source sign must be alpha and the destination sign must be plus or minus.

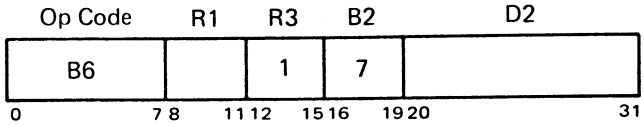
Note 3: The source and destination signs must be unlike for EA but alike for ES, neither sign may be alpha, the result of the addition must be zero, and the EMAD indicator must be on.

Figure 7. Indicators for the EA and ES Instructions

If an accumulator overflow indicator (0, 1 or 2) is set by this instruction while the 7074 image is in halt mode, a System/370 branch is made to an address which is 80 plus the contents of FPR 4 bytes 1-3. In all other cases, the next sequential System/370 instruction follows.

ES (Subtract)

RS Format



Destination Address = 8R1 + C(GR 7)
Source Address = B2 + D2
Exceptions:
Access
Data

Description

The subtract instruction is the same as the add instruction except that the sign of the source word is changed for the addition. A plus or alpha is considered to be minus (an alpha sets the result to alpha) and a minus is set to plus.

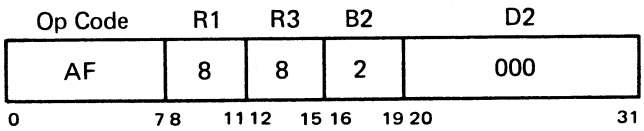
Indicators

The 7074 indicators in FPR 2 are turned on in accordance with Figure 7.

If an accumulator overflow indicator (0, 1 or 2) is set by this instruction while that indicator is in halt mode, a System/370 branch is made to an address which is 80 plus the contents of FPR 4 bytes 1-3. In all other cases, the next sequential System/370 instruction follows.

ERG (Record Gather)

RS Format



Exceptions:
Access
Data

Description

This instruction gathers source data (scattered at different locations within the 7074 simulated storage area of the System/370 storage, as specified by the RDW's) and assembles it into a destination block, according to the destination address.

The index word address (in binary form in GR 2) is used to fetch the index word containing the decimal destination address (positions 2-5 of the 7074 index word or bytes 2-3 of storage). The decimal destination address is then placed in GR 3.

The binary address in GR 3 is used to fetch the first RDW. The decimal address located in bytes 0-1 of GR 11 is updated one and loaded back into GR 11 whenever an RDW is fetched. This decimal address, after converting to binary, is used to fetch the next RDW in the list. GR 8 and GR 9 are used for storing the current RDW.

The RDW is transferred from storage to obtain the decimal start address (bytes 2 and 3), and the decimal stop address (bytes 4 and 5). The RDW sign is located in bit positions 4-7 of byte 6. The original decimal start address is translated from decimal to binary and used to fetch the source word. It is simultaneously incremented by one (decimal) and loaded into GR 8 for later use.

The source data word is stored at the destination address (located at GR 3), after the address has been translated from decimal to binary. The destination address is simultaneously incremented by one (decimal), and loaded into GR 3.

The operation continues sequentially until the RDW working address is equal to the stop address. At that time a check for an RDW with a minus (–) sign is made. A plus (+) sign causes the next RDW to be fetched, after which the operation continues. A minus (–) sign terminates the operation.

Registers Used

GR 2
In initial setup, this register is loaded with the binary address of the index word.

GR 3
Initially, GR 3 is loaded with the 7074 effective address in binary (the starting address of the RDW list). During instruction execution, GR 3 is loaded with the left half of the index word. At the end of instruction execution, GR 3 is loaded with zeros.

GR 8
During instruction execution, GR 8 is loaded with the left half of the RDW.

GR 9
In initial setup, GR 9 is loaded with zeros.

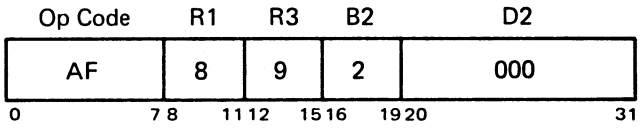
GR's 10-11
In initial setup, GR 10 and GR 11 are loaded with a 7074 instruction having a 7074 effective address. During instruction execution, the updated RDW list address is stored in GR 11 bytes 0-1. At the end of instruction execution, GR 11 bytes 0-1 contain one plus the decimal address of the last RDW.

Input/Output (I/O) and External Interruption Abilities

Whenever a subject word is completely processed and stored in the destination storage address, a test for pending I/O and external interruptions is executed. If the test is positive, the interruption is allowed and its execution is transparent to the operation of the current instruction.

ERS (Record Scatter)

RS Format



Exceptions:
Access
Data

Description

This instruction scatters a 7074 word from a single block in the simulated storage area to destination areas specified by RDW's.

The binary index word address from GR 2 is used to fetch the index word with the decimal source address (in positions 2-5 of the 7074 index word or in bytes 2-3 of storage) and to load source address into GR 3.

The decimal source address in GR 3 is translated from decimal to binary and is used to fetch the first source data word.

The decimal RDW address in GR 11 bytes 0-1 is incremented by one, and is loaded back into GR 11 each time an RDW is fetched. After conversion to binary, this address is used to fetch the next RDW in the list. In each RDW are the parameters of the first destination area: the decimal start address (in bytes 2-3), the decimal stop address (in bytes 4-5), and the sign (byte 6 bits 4-7).

The source word is stored at the destination binary address. The destination address is subsequently incremented by one (decimal) and saved for later use. The operation continues sequentially until the RDW start address is equal to the stop address. At that time a check for an RDW minus (–) sign is made. A plus (+) sign causes the next RDW to be fetched, after which the operation continues. A minus (–) sign terminates the operation.

Registers Used

GR 2
In initial setup, this register is loaded with the binary address of the index word.

GR 3
Initially, GR 3 is loaded with the 7074 effective address in binary (the starting address of the RDW list). During

instruction execution, GR 3 is loaded with the left half of the index word. At the end of instruction execution, GR 3 is loaded with zeros.

GR 8
During instruction execution, GR 8 is loaded with the left half of the RDW.

GR 9
In initial setup, GR 9 is loaded with zeros.

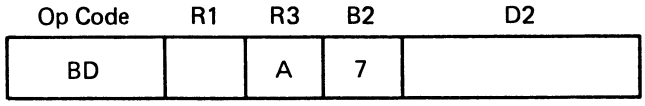
GR's 10-11
In initial setup, GR 10 and GR 11 are loaded with a 7074 instruction having a 7074 effective address. During instruction execution, the updated RDW list is stored in GR 11 bytes 0-1. At the end of instruction execution, GR 11 bytes 0-1 contain one plus the decimal address of the last RDW.

I/O and External Interruption Abilities

Whenever a subject word is completely processed and stored in the destination storage address, a test for pending I/O and external interruptions is executed. If the test is positive, the interruption is allowed and its execution is transparent to the operation of the current instruction.

EFD (Field Definition)

RS Format



Source Word Address = Contents of GR specified by R1 (normally R1 = GR 3)
Destination Word Address = B2 + D2
Exceptions:
Access
Data

Description

Digits are extracted from the 7074 source word (under control of the field definition in GR 10 bits 24-31) and linked together with the sign of the source word. The result is stored at the destination address.

This instruction is an exact simulation of the 7074 zero-add instruction (ZA1, ZA2, or ZA3).

Registers Used

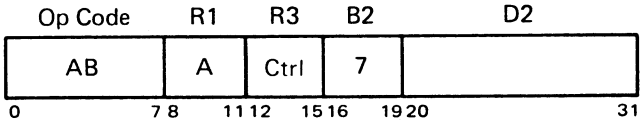
R1
Contains the binary System/370 address of a 7074 word to be fetched.

GR 7
Base address for the destination word.

GR 10
Bits 24-31 are the field definition of a 7074 instruction.

EFST (Field Store)

RS Format



Destination Word Address = C(GR 3)
Source Word Address = B2 + D2
Exceptions:
Access
Data

Description

The field of the destination word, as defined by digits 4 and 5 of the 7074 instruction word in GR 10 and GR 11 is replaced by an equivalent number of digits from the low-order positions of the source word.

Bit 12 of the instruction must be zero. Bit 13 controls the setting of the field overflow indicator. Bits 14 and 15 are used to control setting of the destination sign and the setting of the sign change indicator. (See Figure 8.)

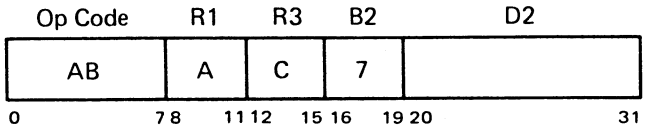
R3 Field	Conditions	Action Taken
01xx	Field overflow	Set indicator 4 to F.
0x1x, 0xx1	Unconditional	Set destination sign equal to source sign.
0x11	Destination sign not equal to source sign	Set indicator 3 to F.
0x01	Destination sign not equal to source sign and not 0-9 field	Set indicator 3 to F.
0x00	Unconditional	Destination sign not changed. Indicator 3 is not changed.
x = Don't care		

Figure 8. Indicator Settings After EFST

If either indicator 3 (sign change) or 4 (field overflow) is turned on by this instruction or by a prior instruction, and that indicator is in halt mode, then a System/370 branch takes place (at the conclusion of this instruction) to the address C (FPR 4 bytes 1-3) plus 80.

EMAD (Move Accumulator Digits)

RS Format



Destination Word Address = 7074 address 9994
Source Word Address = B2 + D2
Exceptions:
Access
Data

Description

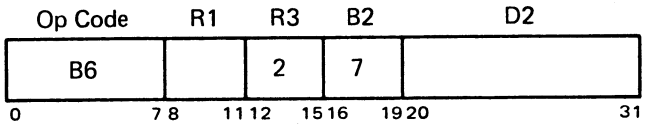
The number of digits specified by field definition in GR 10 is moved from the source word starting with digit 9. The sign of the source word is placed in the destination word.

Indicator 4 (field overflow) can be turned on by this instruction. Halt mode will not be checked during this instruction. If an overflow occurs, byte 3 of GR 11 is set to FF as an EMAD overflow indicator.

Programming Note: This instruction *must* be followed by EA or ES.

EC (Compare)

RS Format



First Word Address = 8 x R1 + C(GR 7)
Second Word Address = B2 + D2
Exceptions:
Access
Data

Description

The first word is compared with the second word for a high, low or equal condition. The following are the relative values of signs and digits:

Highest Numeric	+99999 99999
	to
	+00000 00000
	−00000 00000
	to
Lowest Numeric	−99999 99999
Highest Alphameric	99999 99999
	to
Lowest Alphameric	00000 00000

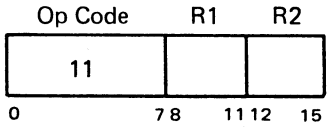
Indicators

Indicators 0-4 are not changed by this instruction. Indicators 5, 6, and 7 are set as follows:

Indicator			*Conditions*
5	*6*	*7*	
FF	00	00	The first word is higher than the second word.
00	FF	00	The first word is equal to the second word.
00	00	FF	The first word is less than the second word.

SIC (Set IC)

RR Format



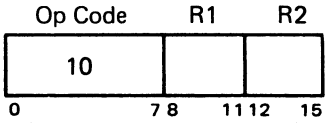
R1 identifies a general register
R2 bit 12 contains 0 or 1
bits 13-15 contain 0-7
Exception:
Data

Description

Bytes 0-1 of the general register specified by R1 contain the new 7074 IC. This IC is modified by the value contained in bits 13-15. If bit 12 is 0, the new IC is incremented; if bit 12 is 1, it is decremented. The modified new 7074 IC is then loaded into FPR 0 bytes 2-3.

EBI (Branch on Indicator)

RR Format



R1 Identifies a general register.
R2 contains the number of the indicator that is to be tested for the conditional branch
Exception:
Data

Description (See Figure 2, FPR 2 Indicator Settings.)

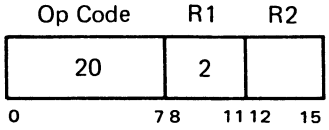
If bits 0-3 of the indicator byte specified by R2 are not all zeros, then the decimal storage address in bytes 0-1 of the R1-specified general register is stored in the 7074 IC (FPR 0 bytes 2-3). If the bits are zeros, then the 7074 IC remains unchanged.

Indicators

Indicators 5, 6, and 7 are never changed by the Branch on Indicator instruction. If the indicator specified by R2 is 0, 1, 2, 3, or 4, then bits 0-3 of the specified byte are set to zero by this instruction. Bits 4-7 of the indicator are not changed.

ETCI (Transfer Condition to Indicator)

RR Format



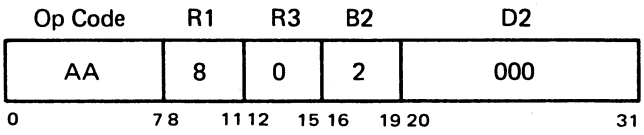
Description

This instruction sets simulated 7074 indicators 5, 6, and 7 from the System/370 condition code as follows:

System/370	*7070/7074 Indicators*		
Condition Code	*5*	*6*	*7*
00	00	FF	00
01	00	00	FF
10	FF	00	00
11	00	00	00

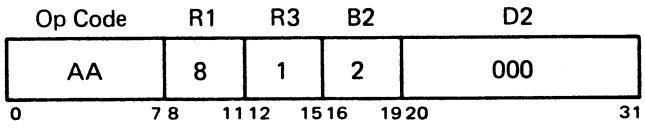
EUB (Unload Buffer)

RS Format



EUBR (Unload Buffer, Record Mark Control)

RS Format



Exceptions:

Access
Data

Description

These instructions perform a buffer transfer which moves information from a System/370 input area and converts it to 7074 word format in the simulated 7074 storage area, under control of the RDW and the buffer byte count.

When instruction execution is begun, GR's 8-9 are checked for presence of a valid RDW, indicated by GR 8 not containing 0 (hex 00000000) and GR 9 not containing either 0 or 1 (hex 00000001). If an RDW is present, GR 1 bits 16-23 (mode and word length) are tested. If bits 16-19 are zero, the mode is alphameric; if nonzero, it is numeric. If bits 20-23 are nonzero, then a partial word is located in GR's 0-1.

If no RDW is present, then the decimal address of the RDW from GR 11 is converted to binary, and a relocation factor from FPR 4 is added to this converted address.

In the conversion and transfer operations, a System/370 doubleword is fetched from the buffer located at the address in GR 2, converted byte-to-byte to its 7074 equivalent, and stored in the simulated 7074 storage area specified by the decimal address in GR 8 bytes 2-3. Subsequent System/370 doublewords are fetched from the buffer area, converted to 7074 word format, and stored under RDW control.

The mode is changed during instruction execution if a mode change character (5F) is the first character either:

1. in the System/370 buffer after completion of a 7074 word, or
2. on initial entry to the instruction.

Alphameric words, composed of five characters from the buffer and converted to 7074 format, have a sixth character added to them (the alpha sign), thus completing them.

Determination of word end in numeric mode is made by encountering a signed digit (not a hex F in the left half of the byte) from the buffer. A 7074 numeric word, which converts five to ten characters (from the buffer) to ten decimal digits (in 7074 format), is filled with high-order zeros if five to nine digits are present when word end is encountered.

If GR 9 byte 3 is set to 01 prior to starting an EUB or EUBR instruction, then either instruction suppresses storing in simulated 7074 storage and comparing the RDW working address to the RDW stop address. (This is termed a long-length record runout, or LLRR.)

The instruction terminates when either:

1. the System/370 buffer byte count reaches zero, or
2. on a EUBR instruction, the fifth character of an alphameric word with a minus-signed RDW is detected as a record mark.

The next sequential RDW is fetched and used if:

1. the fifth character is a record mark but the RDW sign is not minus, or
2. a. the RDW start and stop addresses are equal,
   b. the RDW sign is not minus, and
   c. the instruction is not under LLRR control.

The operation continues until one of the following occurs. They are listed in order of priority.

A. *Branch to the Abort Routine:* Any condition which results in a non-zero status in GR 1 bits 28-31 causes a branch to be taken to the address formed by adding decimal 48 to the base address contained in FPR 4 bytes 1-3. This branch is also taken when the System/370 buffer byte count in GR 3 is reduced to zero and the RDW list is not complete.

When this exit takes place, no partial words are stored in the simulated 7074 storage area.

The following describes the significance of "on" GR 1 status bits.

Mode	*Status Bit On (=1)*	*Significance*
Alphameric	28, 29	None
Alphameric	30	A mode-change character (delta) present in the alphameric word.
Alphameric	31	Undefined character present in a 7074 alphameric word.
Numeric	28	Numeric word of less than five digits is assembled.
Numeric	29	Assembly attempted of a numeric word of more than ten digits.
Numeric	30	Sign of the numeric word is not valid.
Numeric	31	Invalid decimal digit present in the 7074 partial word.

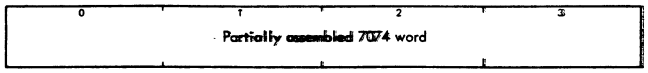
B. *RDW List Completion:* This can be a result of (1) the working address in GR 8 being equal to the stop address in GR 9 and the sign of the 7074 RDW in GR 9 being minus, or (2) a record mark detected as the fifth character of an alpha word on Unload Buffer, Record Mark Control (EUBR) operations and the sign of the 7074 RDW in GR 9 being minus. The next sequential System/370 instruction follows this type of operation.

Note: To facilitate discussion of the unload buffer instructions, these two terminations (the "branch to the abort routine" and "RDW list completion") are referred to as the type A and type B terminations, respectively.

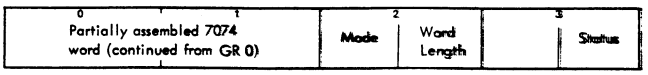
Registers Used

The following registers are used at instruction execution time:

GR 0

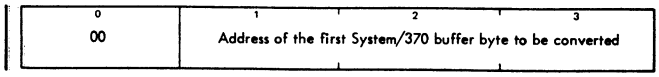


GR 1

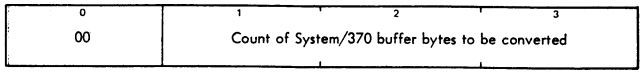


At instruction entry GR 0 must contain zero. GR 1 must also contain zero, excepting bits 16-19, which indicate the mode at entry time. GR 0 bytes 0-3 and GR 1 bytes 0-1 are used for storage of a partially assembled 7074 word, left-adjusted. GR 1 bits 16-19 (left half of byte 2) indicate the current mode of operation: zero for alphameric mode, nonzero for numeric. Bits 20-23 (right half of byte 2) indicate the length of any partially assembled word. The length indicator gives the number of bytes (if the mode is alphameric) or the number of four-bit digits (if the mode is numeric). GR 1 bits 24-31 (byte 3) are used by the microprogram and should not be altered. The latter four bits (28-31) are status bits indicating any errors which occurred during instruction execution.

GR 2



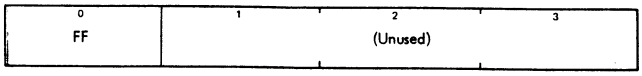
GR 3



GR's 8-9

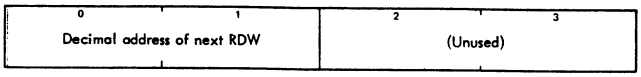
GR 8 and GR 9 contain an RDW in 7074 word format if the RDW is left by a previous EUB or EUBR instruction. GR 9 byte 3 is usually zero except on a long-length record runout (LLRR), when it is hex 01. Except for LLRR information, GR 8 and GR 9 must contain zero for initial entry into the EUB or EUBR instruction.

GR 10

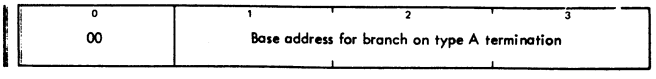


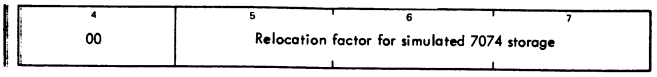
Byte 0 must be set to hexadecimal FF prior to an initial EUB or EUBR instruction execution. Bytes 1-3 may have any value at initial execution time.

GR 11



FPR 4

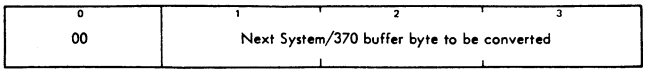




The contents of registers at termination are described next.

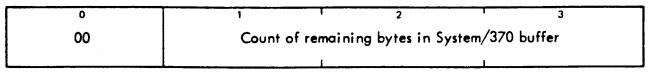
GR's 0-1
For type A terminations, GR 0 and GR 1 contain the post-execution information shown earlier. For type B terminations, GR 1 bits 16-19 indicate the mode of operation at termination: zero for alphameric mode, nonzero for numeric mode. The remainders of GR 0 and GR 1 are undefined for type B terminations.

GR 2



This address is the next buffer byte that would be processed, had the instruction not been terminated. For type A terminations, this byte follows the one which contains any existing errors. If the termination was caused by the GR 3 buffer count going to zero, this address points to the byte following the last byte of the System/370 buffer.

GR 3



GR's 4-7
Not used.

GR's 8-9
For both type A and B terminations, GR 8 and GR 9 contain an RDW in 7074 word format. GR 9 byte 3, normally zero, contains 01 if an LLRR is performed.

For type A terminations, the working address in GR 8 is the decimal address where the next 7074 word is stored. GR 8 byte 0, normally zero, contains hexadecimal FF if the RDW was fetched but not used. GR 9 contains the right half of the RDW in the 7074 word format.

For type B terminations, the working address in GR 8 is the decimal address of the last 7074 word stored. GR 9 contains the stop address and the sign of the last RDW.

GR 10
For type A terminations, GR 10 bytes 2 and 3 contain one plus the decimal address of the previously used RDW working address, if GR 10 byte 0 is zero. If this byte is not zero, then a complete 7074 word has not been assembled.

GR 11
Bytes 0 and 1 contain one plus the decimal address of the last RDW fetched from 7074 storage.

GR's 12-15
Not used.

FPR's 0, 2, 4
Unchanged.

If a new EUB or EUBR instruction is to be executed on the same tape record after a type A termination has occurred, then the GR's should be set up as follows:

1. If termination was due to buffer count runout (a type A termination with zero status in GR 1 bits 28-31) in GR 3, then GR's 0, 1, 8, 9, 10, and 11 must be restored to their pretermination values. GR 2 should be set to the new buffer address and GR 3 should be set to the new buffer byte count, with byte 0 set to zero.
2. If termination was due to a correctable error, then GR's 0-4 and 8-11 should be restored to their pretermination values, with the exception of the partial word length in GR 1 and buffer area address in GR 2 (which should be decremented by 1) and the byte count in GR 3 (which should be incremented by 1). This assures that the corrected byte will be reprocessed. Uncorrected errors make proper instruction execution unpredictable.

After a type B termination, if a new EUB or EUBR (with LLRR specified) is to be performed on the same tape record, the GR's should be set up as follows:

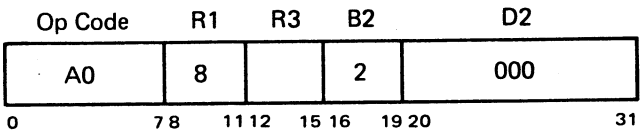
1. GR's 0, 1, 2, 3, 9, and 11 should be restored to the value they contained at termination.
2. The RDW working address in GR 8 at termination should be incremented by decimal 1 and restored to GR 8.

I/O and External Interruption Abilities

Whenever a subject word is completely processed and stored in the destination storage address, a test for pending I/O and external interruptions is executed. If the test is positive, the interruption is allowed and its execution is transparent to the operation of the current instruction.

ELB (Load Buffer)

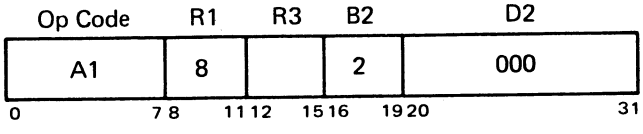
RS Format



R3 = Don't Care

ELBR (Load Buffer, Record Mark Control)

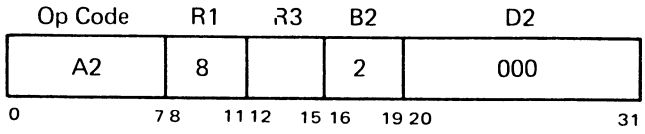
RS Format



R3 = Don't Care

ELBZ (Load Buffer, Zero Elimination)

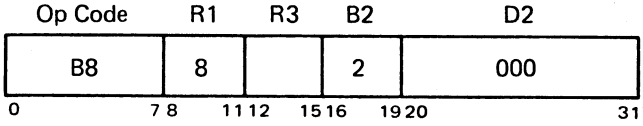
RS Format



R3 = Don't Care

ELBC (Load Buffer, Zero Elimination, Record Mark Control)

RS Format



R3 = Don't Care
Exceptions:

Access
Data

Description

The load buffer instructions load a tape image into the System/370 buffer from the simulated 7074 storage area, under control of the RDW and the buffer byte count.

When instruction execution begins, GR's 8-9 are checked for a valid RDW, indicated by nonzero register contents. If an RDW is present, GR 0 bits 4-7 are tested for mode, and bits 28-31 are tested for a partial word. If bits 28-31 are nonzero, then a partial word is in the previous System/370 buffer. (Data is fetched a doubleword at a time.)

If no RDW is present, the decimal address of the RDW (from GR 11) is converted to binary, and the relocation factor from FPR 4 is added to this converted address. The RDW from this address is then stored in GR's 8-9. (Alphameric mode is assumed.)

In the conversion and transfer operations, the 7074 word is fetched from the RDW start address specified in GR 8. The next digit or character is converted as dictated by the mode and partial word length (PWL) and then stored in the System/370 buffer area designated by GR 2. Subsequent 7074 words are fetched and translated under RDW control. For each word, the RDW working address in GR 8 is incremented by one.

Mode changes are controlled by the 7074 word signs. Each time the mode changes from alphameric to numeric or vice-versa, a delta character (hex 5F) is stored in the System/370 buffer area.

In ELBC and ELBZ zero-elimination operations (in numeric mode), up to five high-order insignificant zeros per word are eliminated.

The next sequential RDW is fetched and used if:

1. the RDW sign is not minus, and
2. a. the RDW stop address equals the RDW start address, or
   b. a record mark is the fifth character of an alphameric word (on ELBR and ELBC instructions).

The operation proceeds until one of the following termination types occur:

A. The RDW working address in GR 8 equals the RDW stop address in GR 9, and the sign of the RDW is minus.
B. In record-mark control operations (ELBR and ELBC) a record mark is encountered as the last character of an alphameric word, and the sign of the RDW is minus.
C. The buffer segment is filled (GR 3 contains zero).
D. An invalid alphameric character is detected in alphameric mode.

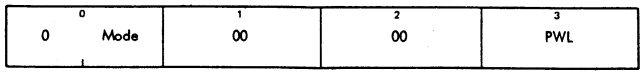
Type A and B terminations are followed by the next sequential System/370 instruction. Type C and D terminations cause a branch to the instruction whose address is decimal 32 plus the base address in FPR 4 bytes 1-3.

Registers Used

The following registers are used at instruction execution time:

GR 0

On initial entry to the load buffer instruction, GR 0 must contain zero. When left by a previous load buffer instruction, GR 0 is as follows:



Byte 0 bits 4-7 indicate whether the current mode of operation is numeric (nonzero contents) or alphameric (zero contents). Byte 3 indicates the length of any partially assembled word that has been formed and stored in the System/370 buffer area. If an invalid alphameric character is present, then the partial word length (PWL) does not include the byte in error. The PWL indicates the number of digits or characters, depending on the mode.

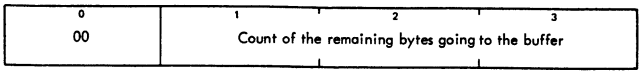
GR 1

This register is used by the compatibility feature.

GR 2

This register contains the address of the first byte of the System/370 buffer to be filled.

GR 3



Bytes 1-3 contain the count of bytes remaining to be filled in the System/370 buffer.

GR's 8-9
On initial entry to the load buffer instruction, these two registers must contain zero. They may contain an RDW in 7074 word format left by a previous load buffer instruction.

GR 11
Bytes 0 and 1 contain the decimal address of the next RDW to be used.

FPR 4
Bytes 0-3 contain the base address for a branch when the buffer byte count equals zero or when an error exists, and bytes 4-7 contain the relocation factor for simulated 7074 storage.

The contents of the registers at termination are described next.

GR 0
For type C or D terminations, GR 0 contains the information described earlier. For type A or B terminations, the contents of GR 0 are undefined.

GR 1
The contents of this register are undefined for all terminations.

GR 2
This register contains the byte address of the System/370 buffer position holding the last valid character or digit inserted, plus one. If an invalid alphameric character is translated, the contained address is that of the byte which holds the translated invalid character.

GR 3
This register contains the count of the bytes remaining to be filled in the System/370 buffer. If an invalid alphameric character has been translated, this count does not reflect the invalid character.

GR's 4-7
Not used.

GR's 8-9
These two registers contain an RDW in 7074 word format. GR 8 byte 0 and GR 9 byte 3 are undefined. GR 8 byte 1 is zero.

For type C or D terminations, the decimal address in GR 8 is that of the current or next word to be translated. For a type D termination, the alphameric character in error is contained in the 7074 word to which this address points. The byte that contains the error is equal to PWL plus one. GR 9 always contains the stop address and the sign of the RDW.

GR 10
Not used.

GR 11
Bytes 0 and 1 contain one plus the decimal address of the last RDW fetched.

GR's 12-15
Not used.

FPR's 0, 2, and 4
Unchanged.

If a new load buffer operation is to be performed on the same tape record after a type C or D termination, the GR's should be set up as follows:

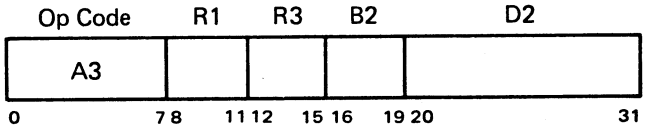
1. For a type C termination, GR 2 should be set to the new buffer address and GR 3 should be set to the new buffer byte count. GR 3 byte 0 must be zero. All other registers used by this instruction must be restored to the values they contained at termination.
2. For a type D termination, all registers used by this instructions must be restored to the values they contained at termination. Additionally, the alphameric character in error must be corrected in the simulated 7074 storage area.

I/O and External Interruption Abilities

Whenever a subject word has been completely processed and stored in the destination storage address, a test for pending I/O and external interruptions is executed. If the test is positive, the interruption is allowed and its execution is transparent to the operation of the current instruction.

EUNA (Unsigned Decimal Add)

RS Format



R3 = Length of operands (in bytes) minus one
R1 = First operand address (binary)
B2 + D2 = Second operand address
Exceptions:
Access
Data

Description

The second operand is added to the first operand and the sum is placed in the first operand. This instruction is similar to the System/370 Add Decimal, with the following exceptions and restrictions:

1. The length of the first operand must equal the length of the second operand.

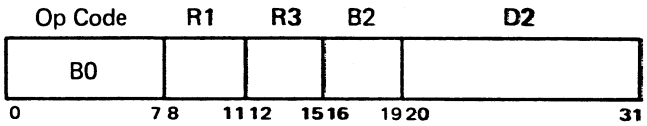
2. Neither operand may cross doubleword boundaries.
3. Operand fields may not overlap.
4. Operand format is packed decimal without signs. The low-order digit is in the *right* half of the low-order byte.
5. The sign is considered positive for both operands.
6. Overflow may result only from a carry out of the high-order byte.
7. There is no program interruption for overflow.
8. The total number of bytes to be added is determined only by the operand byte length. If the starting byte of either or both operands is less than R3, the operation continues from the most significant byte (byte 0) to the least significant byte (byte 7) of the operand that crosses a doubleword boundary.

Resulting Condition Codes

0 - Zero result.
2 - Result greater than zero.
3 - Overflow. Carry from high-order byte.

EUNS (Unsigned Decimal Subtract)

RS Format



R3 = Length of operands (in bytes) minus one
R1 = First operand address (binary)
B2 + D2 = Second operand address
Exceptions:
Access
Data

Description

The second operand is subtracted from the first operand and the result is placed in the first operand. This instruction is similar to the System/370 Subtract Decimal, with the following exceptions and restrictions:

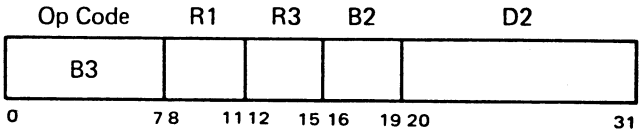
1. The length of the first operand must equal the length of the second operand.
2. Neither operand may cross doubleword boundaries.
3. Operand fields may not overlap.
4. Operand format is packed decimal without signs. The low-order digit is in the *right* half of the low-order byte.
5. The sign is considered positive for both operands.
6. Overflow is not possible.
7. The result has no sign, but a negative result is indicated by the condition code.
8. The total number of bytes to be subtracted is determined only by the operand byte length. If the starting byte of either or both operands is less than R3, the operation continues from the most significant byte (byte 0) to the least significant byte (byte 7) of the operand that crosses a doubleword boundary.

Resulting Condition Codes

0 - Zero result.
1 - Difference is less than zero.
2 - Difference is greater than zero.

ETMB (Test Under Mask and Branch)

RS Format



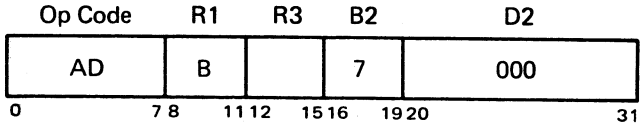
R1 and R3 together form the immediate (I) byte
Source Word = C(B2) + D2
Exceptions:
Access

Description

The single byte addressed by the source word address is ANDed with the contents of the immediate (I) byte. The result is then added to the contents of GR 5. The byte fetched from the resulting address is then multiplied by eight and added in binary to the contents of GR 4. The result of this addition is used as an unconditional branch address. The contents of both GR 4 (which must be a multiple of eight) and GR 5 are not changed by the execution of this instruction.

ESC (Shift Control)

RS Format



R3 = Don't care
Exceptions:
Access
Data

Description

This instruction performs the 7074 uncoupled shift operations (Shift Right Accumulator #, Shift Right and Round Accumulator #, Shift Left Accumulator # and Shift Left and Count Accumulator #).

The next sequential System/370 instruction follows the execution of this instruction.

Registers Used

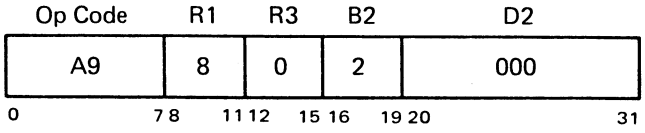
GR 2
On shift and count operations, the number of places shifted replaces digits 4 and 5 of the 7074 word at the location given by this register.

GR 7
Used as address of accumulator 1.

GR 11
Byte 0 is used to specify the accumulator number and type of shift as per digits 6 and 7 of the 7074 instruction word. Byte 1 designates the number of positions to be shifted except for shift and count.

ENA (Edit Numeric to Alphameric)

RS Format



Exceptions:
Access
Data

Description

This instruction performs the functions of the 7074 ENA instruction. There must be an even number of words specified in each RDW, the last address must be greater than the first address, and the RDW sign must not be alpha. The execution of the instruction continues until the working address equals the stop address and the current RDW has a minus sign.

Registers Used

GR 2
In initial setup, this register is loaded with the binary address of the index word.

GR 3
Initially, GR 3 is loaded with the 7074 effective address in binary (the starting address of the RDW list). During instruction execution, GR 3 is loaded with the left half of the index word. At the end of instruction execution, GR 3 is loaded with zeros.

GR 8
During instruction execution, GR 8 is loaded with the left half of the RDW.

GR 9
In initial setup, GR 9 is loaded with zeros.

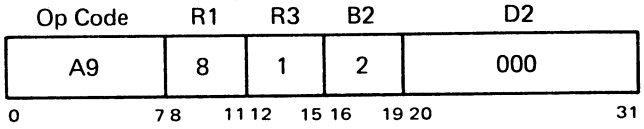
GR's 10-11
In initial setup, GR 10 and GR 11 are loaded with a 7074 instruction having a 7074 effective address. During instruction execution, the updated RDW list address is stored in GR 11 bytes 0-1. At the end of the instruction execution, GR 11 bytes 0-1 contain one, plus the decimal address of the last RDW.

I/O and External Interruption Abilities

Whenever a subject word is completely processed and stored in the destination storage address, a test for pending I/O and external interruptions is executed. If the test is positive, the interruption is allowed and its execution is transparent to the operation of the current instruction.

ENS (Edit Numeric to Alphameric With Sign Control)

RS Format



Exceptions:
Access
Data

Description

This instruction performs the functions of the 7074 ENS instruction. As in the ENA instruction, the operation continues until all RDW lists are completed.

Registers Used

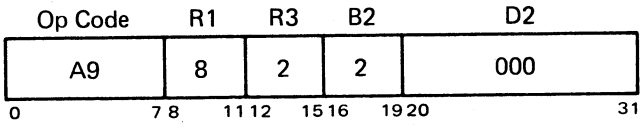
Same as with the Edit Numeric to Alphameric (ENA) instruction.

I/O and External Interruption Abilities

Whenever a subject word is completely processed and stored in the destination storage address, a test for pending I/O and external interruptions is executed. If the test is positive, the interruption is allowed and its execution is transparent to the operation of the current instruction.

ENB (Edit Numeric to Alphameric With Blank Insertion)

RS Format



Exceptions:
Access
Data

Description

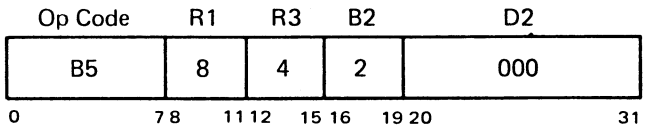
This instruction performs the functions of the 7074 ENB instruction. As in the ENA instruction, the operation continues until all RDW lists are completed.

Registers Used

Same as with the Edit Numeric to Alphameric (ENA) instruction.

EAN (Edit Alphameric to Numeric)

RS Format



Exceptions:

Access
Data

Description

This instruction performs the functions of the 7074 EAN instruction. As in the ENA instruction, the operation continues until all RDW lists are completed.

Registers Used

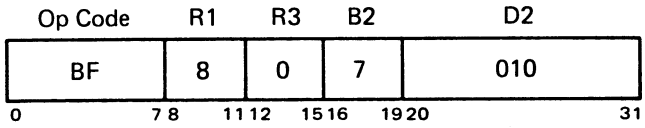
Same as with the Edit Numeric to Alphameric (ENA) instruction.

I/O and External Interruption Abilities

Whenever a subject word is completely processed and stored in the destination storage address, a test for pending I/O and external interruptions is executed. If the test is positive, the interruption is allowed and its execution is transparent to the operation of the current instruction.

ELL (Lookup Lowest)

RS Format



Exceptions:

Access
Data

Description

This instruction performs the functions of the 7074 Lookup Lowest (LL) instruction. Accumulator 2 is *not* used as a working register.

Registers Used

GR 2
During instruction execution, GR 2 is a microprogram working register.

GR 3
In initial setup, GR 3 is loaded with the 7074 effective address in binary (the starting address of the RDW list); at the end of instruction execution, it is loaded with zeros.

GR 8
This register is loaded with the left half of the RDW during instruction execution.

GR 9
This register is loaded with zeros in initial setup, but is loaded with the right half of the RDW during instruction execution.

GR's 10-11
In initial setup, both these registers are loaded with the 7074 instruction having a 7074 effective address. During instruction execution, the updated RDW list is stored in GR 11 bytes 0-1. At the end of instruction execution, GR 11 bytes 0-1 contain one plus the decimal address of the last RDW.

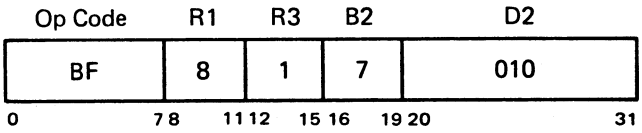
FPR 0
If a "table word found" condition exists at the end of instruction execution, the 7074 IC (FPR 0 bytes 2-3) is incremented by 1.

I/O and External Interruption Abilities

Whenever a subject word is completely processed and stored in the destination storage address, a test for pending I/O and external interruptions is executed. If the test is positive, the interruption is allowed and its execution is transparent to the operation of the current instruction.

ELE (Lookup Equal Only)

RS Format



Exceptions:

Access
Data

Description

This instruction performs the functions of the 7074 instruction of the same name. 7074 accumulator 2 is *not* used as a working register.

Registers Used

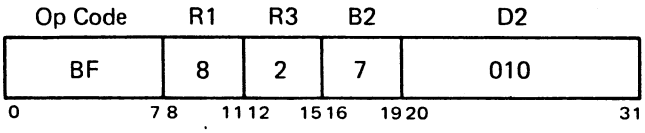
Same as with the Lookup Lowest (ELL) instruction.

I/O and External Interruption Abilities

Whenever a subject word is completely processed and stored in the destination storage address, a test for pending I/O and external interruptions is executed. If the test is positive, the interruption is allowed and its execution is transparent to the operation of the current instruction.

ELEH (Lookup Equal or High)

RS Format



Exceptions:
Access
Data

Description

This instruction performs the functions of the 7074 instruction of the same name. Accumulator 2 (7074) is *not* used as a working register.

Registers Used

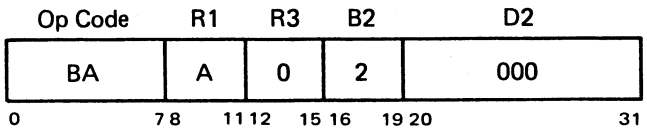
Same as with the Lookup Lowest (ELL) instruction.

I/O and External Interruption Abilities

Whenever a subject word is completely processed and stored in the destination storage address, a test for pending I/O and external interruptions is executed. If the test is positive, the interruption is allowed and its execution is transparent to the operation of the current instruction.

EXA (Index Word Add)

RS Format



Exceptions:
Access
Data

Description

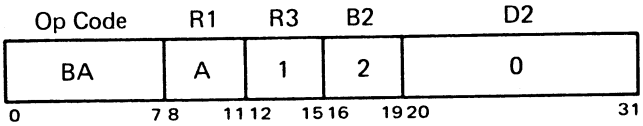
The four-digit number in GR 11 bytes 0-1 (considered plus) is added algebraically to digits 2-5 of the 7074 word whose binary address is in GR 2. The result replaces digits 2-5 of the 7074 word specified by GR 2; the sign of that word is replaced with the sign of the result. An alpha-signed index word remains alphameric.

Registers Used

GR 2
This register contains the binary address of the index word.

EXS (Index Word Subtract)

RS Format



Exceptions:
Access
Data

Description

The four-digit number in GR 11 bytes 0-1 (considered plus) is algebraically subtracted from digits 2-5 of the 7074 word whose binary address is in GR 2. The result and the sign of the result replaces digits 2-5 and the sign of the 7074 word addressed by GR 2. An alpha-signed index word remains alphameric.

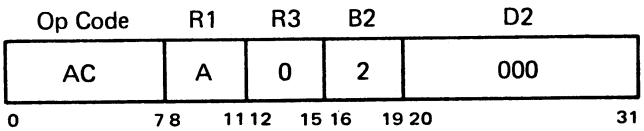
Registers Used

GR 2
This register contains the binary address of the index word.

GR 11
Bytes 0-1 of this register are subtracted from the index word.

EBIX (Branch Incremented Index Word)

RS Format



Exceptions:
Access
Data

Description

The absolute value of digits 2-5 of the 7074 index word (specified by the binary address in GR 2) is increased by one. The result replaces digits 2-5 of that word in simulated 7074 storage. If the incremented value of digits 2-5 is not greater than the absolute value of digits 6-9 of the same word, GR 11 bytes 0 and 1 replace the address in FPR 0 bytes 2 and 3. If the incremented value is greater, FPR 0 is not changed.

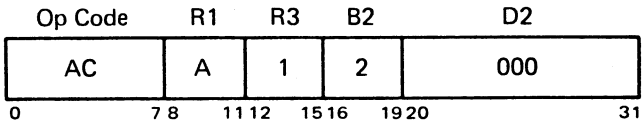
Registers Used

GR 2
This register contains the binary address of the index word to be incremented.

GR 11
On a branch, bytes 0-1 of this register contain the decimal address that replaces the contents of the 7074 instruction counter.

EBDX (Branch Decremented Index Word)

RS Format



Exceptions:
Access
Data

Description

Digits 6-9 of the 7074 index word, specified by the binary address in GR 2, are subtracted from digits 2-5 of the same word. The result replaces digits 2-5 of that word in the simulated 7074 storage.

A branch is taken only if the result is greater than zero. If the result is less than zero, the sign is tested. The sign remains unchanged if it is alpha, but is reversed if it is numeric; in either case, the result is in true form.

Result	*Sign Test*	*Branch*
Greater than zero	No	Yes
Zero	No	No
Less than zero	Yes	No

Registers Used

GR 2
This register contains the binary address of the index word to be decremented.

GR 11
On a branch, bytes 0-1 contain the decimal address that replaces the contents of the 7074 instruction counter.

Appendix

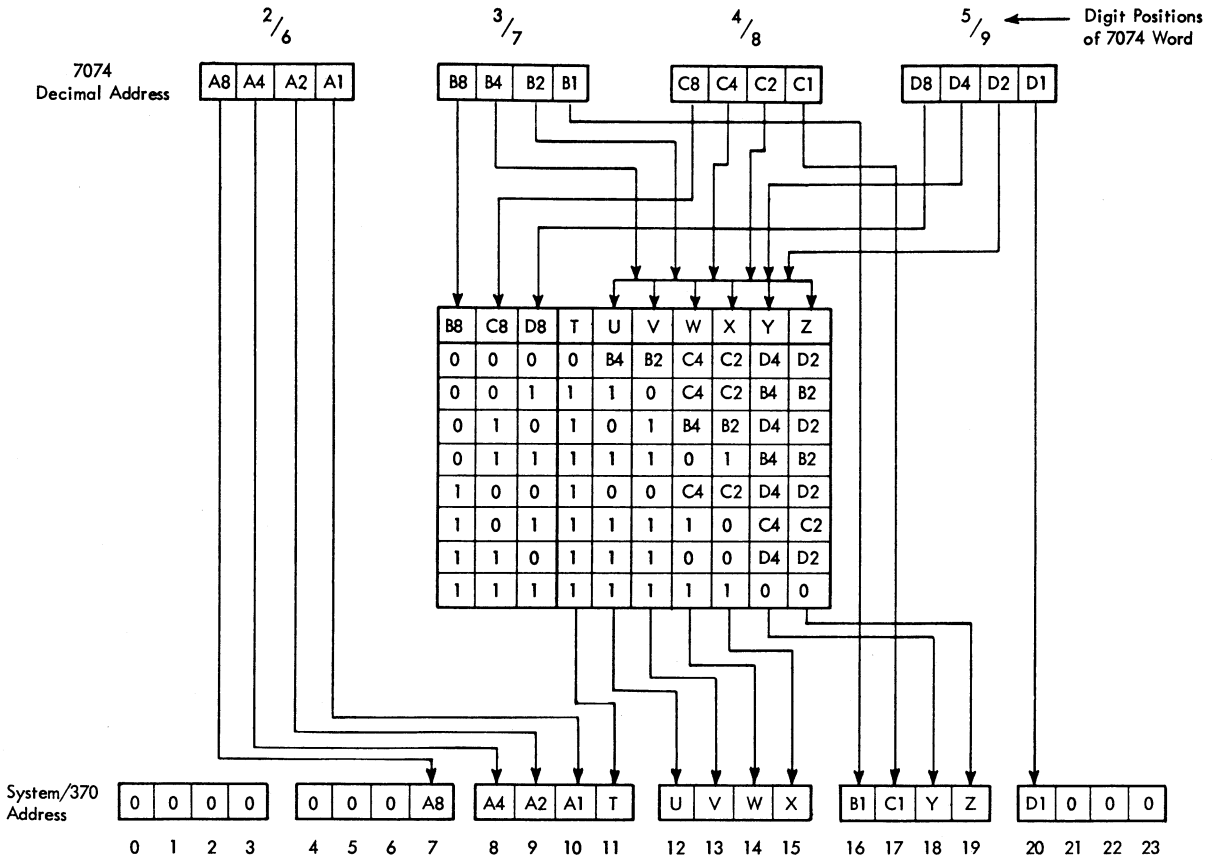
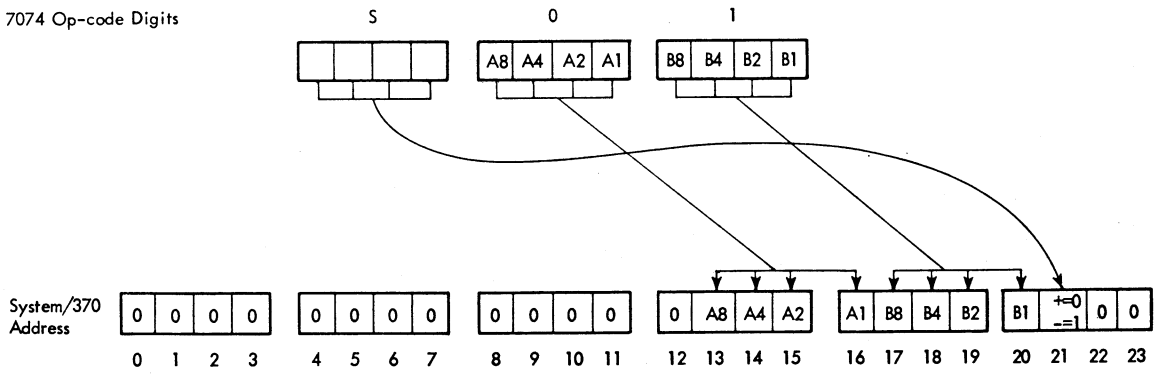


Figure A1. 7074 to System/370 Address Conversion



S = 0 for +, 1 for -

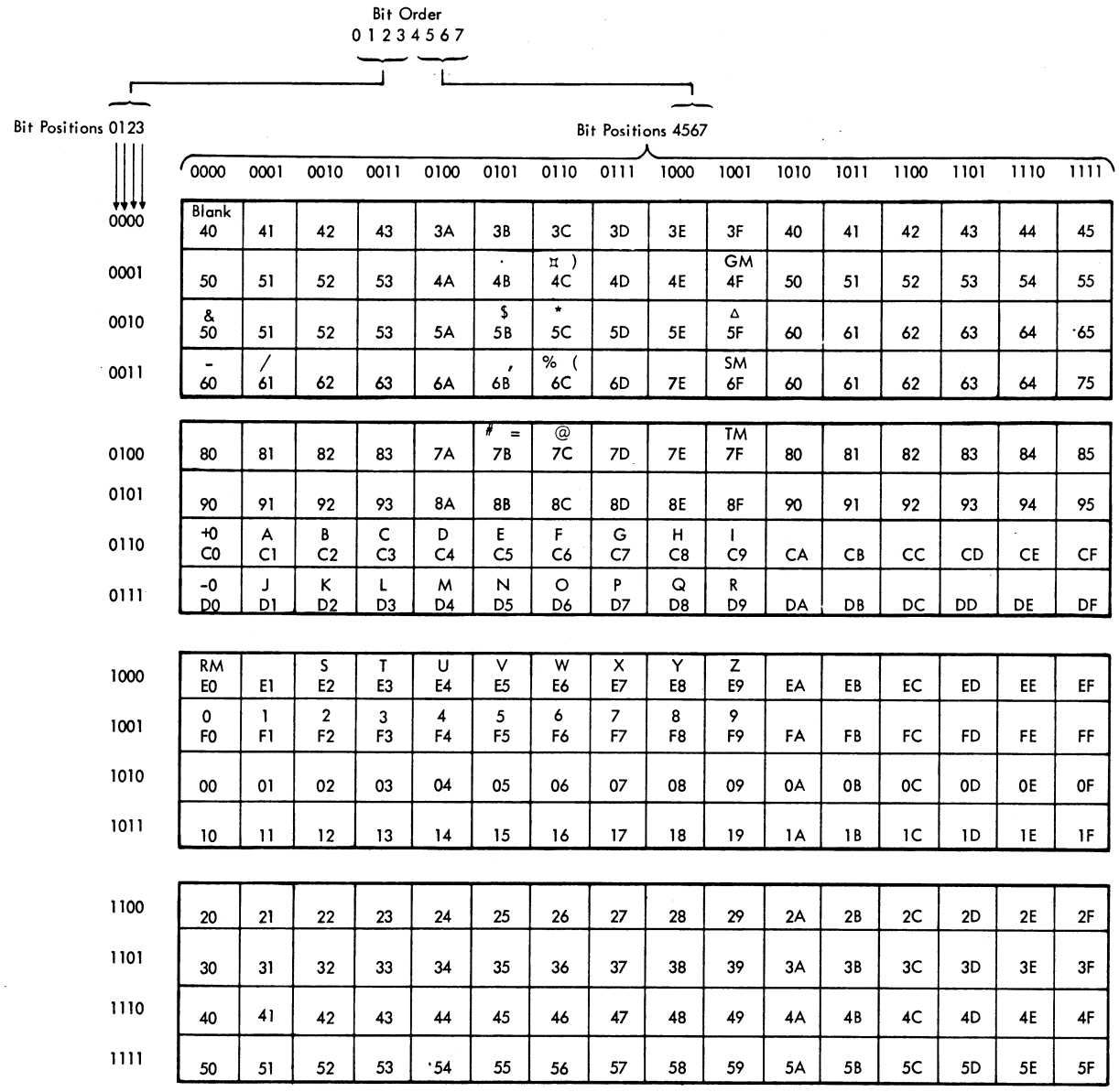
Figure A2. Operation-code Conversion–7074 to System/370

Low-order Op-code Digit

High-order Op-code Digit	0	1	2	3	4	5	6	7	8	9
+0	000000	000008	000010	000018						
-0	000004	00000C		00001C						
+1	000080	000088	000090	000098	0000A0	0000A8	0000B0	0000B8	0000C0	0000C8
-1	000084	00008C	000094	00009C	0000A4	0000AC	0000B4	0000BC	0000C4	
+2	000100	000108	000110	000118	000120	000128			000140	000148
-2	000104	00010C	000114	00011C	000124				000144	
+3	000180	000188	000190	000198	0001A0	0001A8			0001C0	0001C8
-3	000184	00018C	000194	00019C	0001A4				0001C4	
+4	000200	000208			000220	000228	000230	000238	000240	000248
-4	000204	00020C		00021C	000224	00022C	000234	00023C	000244	00024C
+5	000280	000288		000298	0002A0	0002A8	0002B0	0002B8		
-5	000284			00029C			0002B4	0002BC		
+6	000300	000308	000310	000318	000320	000328	000330	000338	000340	000348
-6		00030C	000314			00032C				
+7	000380	000388		000398	0003A0	0003A8	0003B0	0003B8		
-7	000384			00039C	0003A4	0003AC	0003B4	0003BC		
+8		000408	000410	000418	000420					
-8		00040C	000414	00041C	000424					
+9		000488	000490			0004A8				
-9		00048C	000494			0004AC				

(Blanks indicate unused op codes.)

Figure A3. Conversion of 7074 Op Codes to System/370 Model 165, 165 II, and 168 Addresses



	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	Blank 40	41	42	43	3A	3B	3C	3D	3E	3F	40	41	42	43	44	45
0001	50	51	52	53	4A	. 4B	¤) 4C	4D	4E	GM 4F	50	51	52	53	54	55
0010	& 50	51	52	53	5A	$ 5B	* 5C	5D	5E	Δ 5F	60	61	62	63	64	65
0011	- 60	/ 61	62	63	6A	, 6B	% (6C	6D	7E	SM 6F	60	61	62	63	64	75
0100	80	81	82	83	7A	# = 7B	@ 7C	7D	7E	TM 7F	80	81	82	83	84	85
0101	90	91	92	93	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95
0110	+0 C0	A C1	B C2	C C3	D C4	E C5	F C6	G C7	H C8	I C9	CA	CB	CC	CD	CE	CF
0111	-0 D0	J D1	K D2	L D3	M D4	N D5	O D6	P D7	Q D8	R D9	DA	DB	DC	DD	DE	DF
1000	RM E0	E1	S E2	T E3	U E4	V E5	W E6	X E7	Y E8	Z E9	EA	EB	EC	ED	EE	EF
1001	0 F0	1 F1	2 F2	3 F3	4 F4	5 F5	6 F6	7 F7	8 F8	9 F9	FA	FB	FC	FD	FE	FF
1010	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
1011	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
1100	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
1101	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
1110	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
1111	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F

In each block, the lower entry is an EBCDIC 2-digit code; any upper entry is an EBCDIC character.

Figure A4. 7074-Code to EBCDIC Conversion

EBCDIC Bit Order
0 1 2 3 4 5 6 7

Bit Positions 0123

Bit Positions 4567

	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	C0	C1	C2	C3	C4	C5	C6	C7	8E	8F	80	D5	D6	D7	D8	BRTC D9
0001	E0	E1	E2	E3	E4	E5	E6	E7	9E	9F	90	E5	E6	E7	E8	E9
0010	F0	F1	F2	F3	F4	F5	F6	F7	AE	AF	A0	F5	F6	F7	F8	F9
0011	00	01	02	03	04	05	06	07	BE	BF	B0	05	06	07	08	09
0100	Blank 00	01	02	03	04	05	06	07	CE	CF	D0	. 15	¤) 16	17	18	GM 19
0101	& 20	21	22	23	24	25	26	27	DE	DF	E0	$ 25	* 26	27	28	Δ 29
0110	- 30	/ 31	32	33	34	35	36	37	EE	EF	F0	, 35	% (36	37	38	SM 39
0111	40	41	42	43	44	45	46	47	FE	FF	Blank 00	# = 45	@ 46	47	48	TM 49
1000	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
1001	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
1010	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
1011	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
1100	+0 60	A 61	B 62	C 63	D 64	E 65	F 66	G 67	H 68	I 69	6A	6B	6C	6D	6E	6F
1101	-0 70	J 71	K 72	L 73	M 74	N 75	O 76	P 77	Q 78	R 79	7A	7B	7C	7D	7E	7F
1110	RM 80	81	S 82	T 83	U 84	V 85	W 86	X 87	Y 88	Z 89	8A	8B	8C	8D	8E	8F
1111	0 90	1 91	2 92	3 93	4 94	5 95	6 96	7 97	8 98	9 99	9A	9B	9C	9D	9E	9F

In each block, the lower entry is a 7074 2-digit code; any upper entry is a 7074 character.

Figure A5. EBCDIC to 7074-Code Conversion

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