Systems

A Guide to the IBM System/370 Model 155

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This guide presents hardware, programming systems, and other pertinent information about the IBM System/370 Model 155 that describes its significant new features and advantages. Its contents are intended to acquaint the reader with the Model 155 and to be of benefit in planning for its installation.

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First Edition (June 1970)

This guide is intended for planning purposes only. It will be updated from time to time to reflect system changes; however, the reader should remember that the authoritative sources of system information are the Systems Reference Library (SRL) publications for the Model 155, its associated components and its programming support. These publications will first reflect such changes.

Copies of this and other IBM publications can be obtained through IBM branch offices.

A form has been provided at the back of this publication for readers' comments. If this form has been removed, address comments to: IBM Corporation, Technical Publications Department, 112 East Post Road, White Plains, New York 10601.

PREFACE

It is assumed that the reader of this document is familiar with System/360. The reader should have a general knowledge of System/360 architecture, channels, I/O devices, and programming systems support. This guide highlights only those Model 155 hardware, I/O, and programming systems features that are different from those of System/360 models and discusses their significance. Additional, more detailed information regarding System/370 Model 155 hardware and programming systems support can be found in the following SRL publications:

IBM System/370 Model 155 Functional Characteristics (GA22-6942)

IBM System/370 Model 155 Channel Characteristics (GA22-6962)

IBM System/370 System Summary (GA22-7001)

IBM System/370 I/O Configurator (GA22-7002)

IBM System/370 Principles of Operation (GA22-7000)

IBM 3210 Console Printer-Keyboard Model 2 Component Description (GA24-3552)

IBM 3215 Console Printer-Keyboard Model 1 Component Description (GA24-3550)

Component Summary: 3803 Storage Control, 3330 Disk Storage (GA26-1592)

IBM System/360 Component Description: 2835 Storage Control and 2305 Fixed Head Storage Module (GA26-1589)

3211 Printer and 3811 Control Unit Component Description (GA24-3543)

IBM Component Description: 3803/3420 Magnetic Tape Subsystem (GA32-0020)

Form-Design Considerations - System Printers (GA24-3488)

Emulating the IBM 1401, 1440, and 1460 on IBM System/370 Models 145 and 155 using OS/360 (GC27-6945)

Emulating the IBM 1410 and 7010 on IBM System/370 Models 145 and 155 using OS/360 (GC27-6946)

IBM System/360 Operating System:

- Planning for the IBM 3211 Printer Data Management Macro Instructions and Services (GC21-5008)
- Program Planning Guide for DOS Emulator on IBM System/370 Models 145 and 155 (GC24-5076)

Emulating the IBM 1410 and 7010 on IBM System/370 Models 145 and 155 using DOS/360 (GC33-2005)

Emulating the IBM 1401, 1440, and 1460 on IBM System/370 Models 145 and 155 using DOS/360 (GC33-2004)

IBM System/360 Disk Operating System:

- IBM 3211 Printer Program Planning Guide (GC24-5085)
- Program Planning Guide for MCAR/CCH Function for IBM System/370 Model 155 (GC24-5084)

CONTENTS

FIGURES

TABLES

SECTION 01: SYSTEM HIGHLIGHTS

The System/370 Model 155 is designed to enhance, extend, and broaden the successful concepts of System/360 architecture. It is a general purpose growth system for System/360 Model 50 and large Model 40 users that provides significant price performance improvement without the necessity of major reprogramming. The System/370 Model 155 retains and extends the wide range of data processing capabilities offered by System/360 Models 40 and 50. It is compatible with the System/370 Model 165.

Transition from System/360 models to the System/370 Model 155 can be accomplished with a minimum of effort because most current System/360 user programs, I/O devices, and programming systems are upward compatible with the new system. Additional capabilities will be added to OS and DOS to support new features of the Model 155, thereby providing proven operating system performance as well as continuity.

Transition with little or no reprogramming also is provided for 1401/1440/1460 and 1410/7010 users who are presently emulating on System/360. Improved emulators are provided for these systems that operate under OS or DOS control on the Model 155.

DOS users who wish to install OS on their Model 155 can ease the transition by installing the new OS/DOS Compatibility Feature. An OS DOS Emulator program is provided that supports emulation of a DOS multiprogramming system under OS control.

Highlights of the Model 155 are as follows:

- Upward compatibility with most System/360 architecture and programming has been maintained.

- Internal performance is approximately three and one-half to four times that of the Model 50 for a typical instruction mix.

- The following are CPU features of the Model 155.

  The Model 155 standard instruction set includes new general purpose instructions in addition to the powerful System/360 instruction set. These instructions enhance decimal arithmetic performance, eliminate the need for multiple move or compare instructions or move subroutines, and facilitate record blocking and deblocking, field padding, and storage clearing.

  Extended precision floating-point is available to provide precision of up to 28 hexadecimal digits, equal to approximately 34 decimal digits.

  An interval timer of 3.33 ms resolution to improve job accounting accuracy is standard. A 16.6 ms resolution timer is provided for Models 40 and 50.

  A time of day clock is included to provide more accurate time of day values than the interval timer. The clock has a 1 microsecond resolution.

  Instruction execution is overlapped with instruction fetching to improve internal performance.

CPU retry of most failing CPU hardware operations is handled automatically by the hardware without programming assistance.

- Functionally improved relocatable emulators are available that operate under operating system control. Concurrent execution of System/370 programs with any combination of 1401, 1440, 1460, 1410, and 7010 programs in a multiprogramming environment is supported. Only one compatibility feature is required for integrated emulation of all these systems.

- The new OS/DOS Compatibility Feature permits emulation of a DOS system under OS concurrent with the execution of other OS jobs. Both DOS and 1400/7010 emulation can operate together on a Model 155 under OS control.

- New operator console devices are provided.

  The 15-cps 3210 Console Printer-Keyboard

  The 85-cps 3215 High-Speed Console Printer-Keyboard

  A remote 3210 Console Printer-Keyboard, which can be installed in addition to either of the above printer-keyboards

- The following channel features are available for the Model 155.

  Up to five high-speed block multiplexer channels can be attached in addition to the standard byte multiplexer channel. Two block multiplexers are standard. A block multiplexer channel can operate at a 1.5-megabyte data rate and can therefore support I/O devices such as the 3420 Model 7 Magnetic Tape Unit - not attachable to the Model 40.

  A special feature permits replacement of channel 4 with a second byte multiplexer channel to provide up to 512 byte multiplexer subchannels in systems with 768K or more and with channel 3 installed.

  A block multiplexer channel is a superset of a selector channel. When used in conjunction with rotational position sensing devices, block multiplexer channels can increase total system throughput by permitting increased amounts of data to enter and leave the system in a given time period. A single block multiplexer channel can support interleaved, concurrent execution of multiple high-speed I/O operations.

  Block multiplexer channels with a data rate of 1.5 MB support attachment to the Model 155 of the 3330 and the 2305 Model 2 facilities, which are not included in Model 40 and 50 configurations.

  Channel retry data is provided when channel errors occur so that error recovery routines can retry I/O operations.

- The following storage features are provided by the Model 155.

  A two-level memory system is implemented, consisting of fast, large-size processor (main) storage used as backing storage for a smaller, very high-speed buffer storage. The CPU works mostly with the buffer so that the effective system storage cycle is one-third to one-quarter of the actual processor storage cycle:

  8K bytes of high-speed monolithic buffer storage is standard. The CPU can fetch four bytes from the buffer in 230 nanoseconds.

256K to 2048K of processor (main) storage is available - four times the maximum main storage available on the Model 50. Processor storage has a cycle time of 2.1 microseconds for consecutive 16-byte references.

Byte boundary alignment is permitted for the operands of non-privileged instructions to eliminate the necessity of adding padding bytes within records or to blocked records for the purpose of aligning fixed- or floating-point data.

Error checking and correction (ECC) hardware, which automatically corrects all single-bit processor storage errors and detects all double-bit and most multiple-bit errors, is standard.

- I/O devices include the following.

  Most currently announced I/O devices for System/360 Models 40 and 50 can be attached.

  The new 3330 facility is available with significantly faster seeks and more than twice the data rate of the 2314 facility, more than three times the capacity of the 2314, and automatic error correction features. The new rotational position sensing and multiple requesting capabilities announced for the 2305 facility are standard.

  The 3330 has an 806 KB data transfer rate, average seek time of 30 ms, and full rotation time of 16.7 ms. Up to 800 million bytes can be contained on an eight drive facility.

  The 2305 facility Model 2, with a maximum module capacity of 11.2 million bytes, a data rate of 1.5 megabytes, and average access of 5 ms can be attached to a Model 155 to be used as a system residence device or as high-speed storage.

  The new high-speed 3211 Printer with a tapeless carriage and print speed of 2000 alphameric lines per minute is available. The tapeless carriage decreases operator intervention by eliminating carriage tape loading and unloading.

  The new 3803/3420 Magnetic Tape Subsystem is attachable. Models 3, 5, and 7 of the 3420 Magnetic Tape Unit, with data rates of 120 KB, 200 KB, and 320 KB, respectively, at 1600-BPI recording density, are provided. Phase-encoded recording, which automatically corrects all single-bit read errors in-flight, is used. This new tape subsystem offers improved price performance; Dual Density and Seven-Track features for compatibility with, and conversion of, 2400-series tape volumes; greatly reduced operator handling through implementation of such features as automatic tape threading and cartridge loading; lower cost tape switching than is currently provided; and enhanced reliability, availability, and serviceability features.

- Extensive hardware and programming systems error recovery and repair features are provided to enhance system reliability, availability, and serviceability.

- Compact physical design reduces Model 155 space requirements. The Model 155 has more than two and one-half times the number of circuits as a Model 50, yet a 512K system is one frame smaller than a 512K Model 50.

As the highlights indicate, Model 40 and 50 users have a broader range of Model 155 configurations to choose from than before when tailoring a growth system with improved throughput and expanded capabilities.

Specifically, the Model 155 offers the following advantages over Models 40 and 50.

Larger Processor (Main) Storage Sizes

Storage sizes of 256K, 384K, 512K, 768K, 1024K, 1536K, and 2048K are provided. The Model 40 can have a maximum of 256K, while 512K is the largest main storage size provided by a Model 50. The Model 155 offers larger storage sizes at smaller cost increments, and additional storage can contribute significantly to system performance and capabilities.

The addition of more storage provides the Model 155 user with the ability to:

- Execute more jobs concurrently, including new application and integrated emulator jobs
- Add and expand applications, such as graphics, teleprocessing, time-sharing, and data-based, that require larger amounts of storage
- Use higher level language translators and linkage editors that provide more functions and execute faster
- Execute larger processing programs without the necessity of overlay structures
- Allocate more storage to language translators and sorts to improve their execution speed
- Use more and larger I/O buffers to speed up input/output operations and optimize use of direct access storage space
- Include system generation options that improve control program performance and support additional functions

Greatly Expanded Channel Capabilities

The fast internal performance of the Model 155, together with expanded use of multiprogramming, requires that more data be available faster.

Two byte multiplexer channels can be installed on a Model 155. Models 40 and 50 are limited to one. The Model 155 also offers more and faster high-speed channels than the Model 50 (five instead of three, 1.5 MB data rate versus .8 MB) and block multiplexer channels not provided for Models 40 and 50.

The channel features of the Model 155 provide:

- Up to 512 byte multiplexer subchannels for large teleprocessing users.
- Attachment of high-speed direct access devices such as the 3330 and 2305 Model 2 facilities
- Potential increases in channel throughput via use of block multiplexing with rotational position sensing to improve effective data transfer rates
- A significantly higher attainable aggregate channel data rate than the Model 50 to balance the high performance capabilities of the Model 155 CPU

Faster I/O Devices with Increased Data Capacity

The 3330 and the 2305 Model 2 facilities offer significantly faster data access than the 2314 facility and 2301 Drum Storage because of higher data transfer rates, faster rotation, and new features. Rotational position sensing and multiple requesting used with block multiplexing can improve I/O throughput by making more efficient use of channel time. These direct access facilities also offer higher availability through use of new hardware-only and program-assisted error correction features.

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The 3330 facility provides high-capacity and fast access for less cost per bit. It is a growth device for the 2314 facility and the 2321 Data Cell Drive that offers increased price performance. The 3330 facility is designed to be used in every area in which direct access storage is needed. For example:

- As a system residence device and for program library storage
- In teleprocessing applications for message queuing and for residence of online applications data
- In online, data-based applications, such as management information systems, airline reservations, etc.
- In time-sharing (or interactive) environments as swap devices and for online work storage (for program and data residence)
- As high-speed work storage for sorting, assembling, and link editing
- For residence of data indices, such as for ISAM data sets

The 2305 Model 2 facility offers faster access than, and more than twice the capacity of, the 2301 drum. For larger Model 155 users, the 2305 facility will be of benefit:

- As system residence devices
- In time-sharing environments as a swap device and for program and data residence
- As high-speed work storage and for residence of data indices

SUMMARY

The combination of new and improved hardware and input/output facilities, enhanced operating system support, integrated 1400/7010 emulation, DOS emulation under OS, and increased system availability provided by the Model 155 offers Model 40 and 50 users expanded computing capabilities without the necessity of a large conversion effort. Little or no time need be spent modifying operational System/360 code or programs currently being emulated. Users of 1400 and 7010 systems can upgrade directly to a Model 155 and an operating system environment with a minimum of reprogramming. DOS users can convert to OS more easily than is possible without the use of DOS emulation. Existing CPU-bound programs can execute faster because of the increased internal performance of the Model 155, while I/O-bound programs can benefit from the use of more storage, more channels, faster I/O devices, and block multiplexing.

The increased power and new functions of the Model 155 provide the base for expanded applications growth and penetration of previously marginal application areas. The increased price performance of the Model 155 offers the user the opportunity to widen his data processing base for less cost.

In conclusion, the major advantages of the System/370 Model 155 are:

- LARGE PROCESSOR STORAGE - At low cost increments
- FAST INTERNAL PERFORMANCE - Approximately three and one-half to four times the Model 50
- CHANNEL ENHANCEMENTS - More, faster, new capability
- INTEGRATED EMULATION - Native mode and second generation processed concurrently
- RELIABILITY, AVAILABILITY, AND SERVICEABILITY - Hardware and programming systems features not available on System/360 Models 40 and 50
- NEW I/O EQUIPMENT - Faster, larger direct access storage with new capabilities and a faster printer, and a new magnetic tape subsystem

SECTION 10: ARCHITECTURE AND SYSTEM COMPONENTS

10:05 ARCHITECTURE DESIGN

The basic design objectives embodied in System/370 Model 155 architecture provide System/360 and 1401/1440/1460 and 1410/7010 emulator users with a growth system in the medium system range that incorporates improvements and additions to System/360 architecture. The Model 155 provides new system capabilities, performance improvements, and features to increase system reliability, availability, and serviceability. This has been achieved under the following conditions:

- System/370 Model 155 architecture is upward compatible with that of System/360 models so that most user programs written for the System/360 will run efficiently on the Model 155 without modification.
- Programming systems support for the Model 155 is based on that provided for System/360 models, namely OS and DOS.
- Most currently announced System/360 I/O devices will operate on the Model 155. (See Section 20:05 for a list of the I/O devices that cannot be included in a Model 155 configuration.)
- The open-ended design characteristic of System/360 has been preserved and extended on System/370.

As a result of the architecture design criteria used for this new system, all programs written for System/360 (Models 25 and up) will operate on a System/370 Model 155 with a comparable hardware configuration, with the following exceptions:

1. Time-dependent programs
2. Programs using machine-dependent data such as that which is logged in the machine-dependent logout area. (OS SER and MCH error-logging routines and the DOS MCRR error-logging routine for System/360 models will not execute correctly.)
3. Programs that use the ASCII mode bit in the PSW
4. Programs that depend on the nonusable lower core storage area being smaller than 1152 bytes. This area can be reduced to 512 bytes by moving the CPU logout area. (See Section 50.)
5. Programs deliberately written to cause certain program checks
6. Programs that depend on devices or architecture not implemented in the Model 155, for example, the native file of the Model 44, relocation implemented in the Model 67, etc.
7. Programs that use model-dependent operations of the System/370 Model 155 that are not necessarily compatible with the same operations on System/360 models

Note that these are the same types of restrictions that exist for compatibility among System/360 models.

The major sections of the Model 155 computing system are the processor (CPU), storage, channels, and the system control panel and console. Each component and its new features are discussed in the subsections that follow. Programming systems support of these new features is covered in Section 30. Reliability, availability, and serviceability (RAS) hardware features are mentioned only briefly. A full discussion of both hardware and programming systems RAS facilities is contained in Section 50.

10:10 THE CENTRAL PROCESSING UNIT (CPU)

The central processing unit contains all the elements necessary to decode and execute the instructions in the System/370 Model 155 instruction set and, optionally, those in the hardware compatibility feature required by the 1401/1440/1460 and 1410/7010 emulator programs. All CPU functions and channel operations are controlled by the microprogram contained in the 72-bit control words in capacitor read-only storage (ROS). The Model 155 CPU has a cycle time of 115 nanoseconds. Among the elements contained in the CPU are a four-byte parallel binary adder, local storage, and instruction fetch hardware.

Local storage, addressable by the microprogram, is used as an intermediate storage area by the CPU and the integrated channels. It consists of two areas. CPU local storage, which contains the general purpose and floating-point registers, is shared by the CPU and the channels. I/O local storage is used exclusively by the channels and is controlled by separate channel hardware so that it can be used for I/O data transfer without interfering with the CPU.

Instruction processing performance is improved by the fact that most instruction fetching is overlapped with instruction execution. Three one-word instruction buffers are provided in the I-Fetch area of the CPU for the prefetching of instructions. One prefetched instruction is decoded at a time but operands are not prefetched.

Imprecise interrupts do not occur on the Model 155. An interrupt is referred to as "imprecise" when not enough information is available to determine which instruction caused the interrupt. Models 40 and 50 do not overlap instruction fetching with instruction execution.

Extensive parity checking is done in the CPU to insure the validity of the data being used. Every data path within and to the CPU is parity-checked, as are every ROS word and all adder sums. Automatic hardware retry of most failing CPU operations, without programming assistance, is provided as an availability feature and is discussed in the RAS section.

The program states in which the Model 155 is operating are reflected in the current program status word (PSW) and in new CPU status indicators called control registers, which are located in the CPU. Up to 16 control registers, 0-15, can be addressed; however, only 4 are implemented in the Model 155. They are program addressable when the CPU is in the supervisor state. A control register can be set with the new LOAD CONTROL instruction and its contents can be placed in processor storage with the STORE CONTROL instruction. Additional status indicators contained in control registers are required in order to support new system functions. A control register is 32 bits in size.

The contents, layout, and function of fixed locations 0-127 in System/370 models are identical to these locations in System/360 models with one exception. Bit 12 in the PSW, which sets EBCDIC or ASCII mode in System/360 models, is not used for this purpose in the Model 155 and must be set to zero. ASCII mode is not implemented in the

Model 155, nor was the mode bit supported by IBM programming systems provided for System/360 models, as the expectation that System/360 ASCII-8 would become the ASCII standard has not been borne out.

The implementation of the machine check level of interrupt on the Model 155 has been considerably altered from its implementation in Models 40 and 50 to enhance system availability and is discussed in Section 50. However, the other four interrupt levels operate in the same manner on Models 40, 50, and 155.

Significant new features of the Model 155 CPU are as follows.

EXPANDED INSTRUCTION SET

The standard instruction set for the System/370 Model 155 is a superset of that provided for System/360 Models 40 and 50. It consists of the System/360 instruction set plus new instructions that support System/370 architecture and provide additional functions. The Model 155 standard instruction set includes all general purpose and I/O instructions and all binary, decimal, and floating-point arithmetic instructions except those that are part of the extended precision optional feature. Storage protect and time of day clock instructions are also standard. The new STORE CPU ID instruction permits a program to determine the model upon which it is operating and provides the system serial number. The new STORE CHANNEL ID instruction can be used to identify the types of channels present in the system. Other new instructions are:

- Extended Precision Floating Point (optional)

  This feature is provided for use in application areas in which the precision provided by the standard floating-point feature is not large enough.

  Precision of up to 28 hexadecimal digits, approximately equal to 34 decimal digits, is provided by the extended precision data format. Extended precision is achieved by using two doublewords (16 bytes) to represent an extended precision floating-point number instead of using one doubleword as is done in long form representation. Fourteen hexadecimal digits, or up to 17 decimal digits, of precision is provided by the long floating-point format.

  Seven floating-point instructions are included in the extended precision feature. They provide addition, subtraction, and multiplication operations for extended precision data, using a pair of floating-point registers, and the ability to round from long to short form or from extended to long form.

- General purpose instructions

  Six general purpose instructions, which will be of benefit to both control and processing program performance, have been added to the Model 155 standard instruction set.

  SHIFT AND ROUND DECIMAL, using a single instruction, provides right or left shifting of packed decimal data. This instruction can save 6 to 18 bytes of instruction storage and instruction execution time for each decimal shift and round operation performed in commercial processing.

  MOVE LONG provides for the movement of up to 16 million bytes from one location in storage to another with a single instruction, thereby removing the current limitation of 256 bytes per move. This instruction can eliminate the necessity of multiple move

instructions or the inclusion of move subroutines. The format and operation of MOVE LONG facilitates efficient record blocking and deblocking, field padding, and storage clearing, frequently performed operations in commercial processing. The new COMPARE LOGICAL LONG instruction can be used to compare logically two fields of up to 16 million bytes in length, thus removing the current 256-byte limit on byte compares. In addition, when an unequal compare occurs, the two characters that caused the inequality are identified.

The MOVE and COMPARE LONG instructions are interruptable. Thus when an I/O operation terminates during their execution, the interrupt is taken and the channel is not held up awaiting termination of what might be a lengthy move or compare.

COMPARE LOGICAL, INSERT, and STORE CHARACTERS UNDER MASK instructions provide byte addressability within the general purpose registers and permit nonword-size data that is not on a word boundary to be compared to data in a register, loaded into a register, and stored from a register. These three instructions can be of most benefit to control program programmers, to compiler writers, and to others who must manipulate processor storage addresses.

ARCHITECTURE IMPLEMENTATION ALTERATIONS

Two alterations have been made to the system action taken on a Model 155 during the execution of certain instructions common to both System/370 and System/360 models. The first involves all instructions that check the validity of operands involved in packed decimal operations. On the Model 155, an invalid sign in an operand causes the instruction to be suppressed (never executed) rather than terminated during execution as is done on System/360 models. Suppression rather than termination of an instruction when an invalid sign occurs insures that the data fields involved remain unchanged. Therefore, a routine can be executed when a program check occurs that inspects the field that has the invalid sign.

For example, when an invalid sign results from packing an entirely blank field, the sign can be corrected by programming, and transaction deletion or program termination is avoided.

The second alteration concerns the recognition of a storage protection exception during the execution of an EDIT or an EDIT AND MARK instruction. On a Model 155 a protection exception always occurs when a pattern character is fetched from a location protected for storing but remains unchanged during the edit operation. This change eliminates unpredictable system operation during editing on a Model 155. The occurrence of a protection exception for the situation described is model-dependent for System/360 models.

INTERVAL TIMER

The interval timer in decimal location 80 in fixed processor storage is a standard feature and has a resolution of 3.33 ms instead of the 16.6 ms resolution (with 60-cycle power) implemented for the timer on Models 40 and 50. Its maximum time period remains 15.5 hours. The higher resolution of this interval timer eliminates many of the problems encountered in accounting routine accuracy caused by task execution durations that are less than the 16.6 ms resolution interval.

TIME OF DAY CLOCK

This new clock is a binary counter of 52 bits with a cycle of approximately 142 years. It is a standard feature. The clock is updated every microsecond. Two new instructions (SET CLOCK and STORE CLOCK) are provided to set the time and to request that the current time be stored in the specified doubleword of processor storage. The time can be set only when the CPU is in supervisor state and only when the clock security switch on the system console panel is in the enable set position.

The time of day clock can be used for more accurate time stamping than the interval timer. Accurate time of day can be maintained because during normal operations the clock stops only when CPU power is turned off. The interval timer cannot be as accurate as the clock for time of day maintenance because it is not updated when the system is in the stopped state and its updating may be omitted under certain conditions of excessive system activity. The 15.5-hour cycle time of the interval timer is also a restriction. The time of day clock better answers the timing needs of teleprocessing and real-time applications.

10:15 STORAGE

PROCESSOR (MAIN) STORAGE

The Model 155 has a two-level memory system, a small high-speed buffer storage backed by a large processor (main) storage. Prior to this time, such a concept was implemented only in very large-scale, high internal performance systems such as System/360 Models 85 and 195. Model 155 processor storage has a 2.1 microsecond cycle time and is buffered by 8K of high-speed monolithic buffer storage.

The use of a two-level memory system, in which the CPU works mostly with the buffer, drastically reduces the effective processor storage cycle of the Model 155 and greatly contributes to the fact that the internal performance of the Model 155 is approximately three and one-half to four times that of the Model 50.

Processor storage is available in the following increments:

Model	Capacity
H	256K
HG	384K
I	512K
IH	768K
J	1024K
JI	1536K
K	2048K

The CPU, the buffer, or a channel has access to 16 bytes of processor storage every 2.1 microseconds for consecutive fetches with no interference.

Error checking and correction (ECC) hardware provides automatic detection and correction of all single-bit processor storage errors and detection, but not correction, of all double-bit and most multiple-bit errors. The ECC feature is discussed fully in the RAS section.

The Model 155 supports a byte-boundary alignment facility for processor storage. The presence of the byte-oriented operand function allows the processor storage operands of unprivileged instructions (RX and RS formats) to appear on any byte boundary without causing

a specification program interrupt. Without this facility, operands must be aligned on integral boundaries, that is, on storage addresses that are integral multiples of operand lengths. Byte orientation is standard and does not apply to alignment of instructions or channel command words (CCW's).

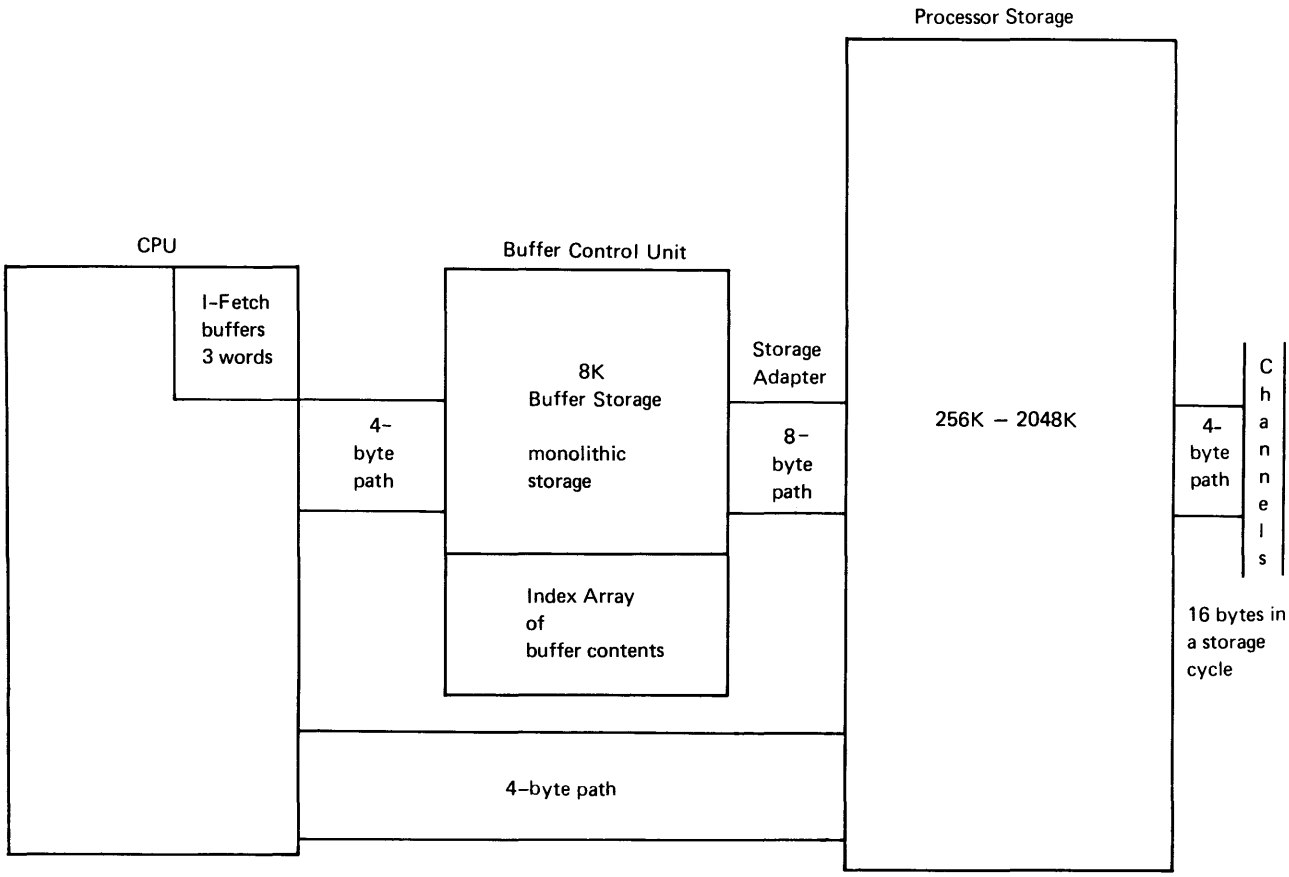
Use of byte alignment in a program degrades instruction execution performance. However, byte orientation can be used effectively in commercial processing to eliminate the padding bytes added within records or to blocked records to insure binary and floating-point field alignment. The smaller physical record that results from the elimination of padding bytes requires less external storage and increases effective I/O data rates. I/O-bound commerical programs, in which throughput is in almost direct proportion to the I/O data rate, can achieve performance improvement by using byte alignment for binary and floating-point data.

A program written to use byte boundary alignment will not necessarily run on a System/360 model that does not have the feature. Therefore, programs that are to run on both the Model 155 and on System/360 models without byte orientation should be written to adhere to integral boundary rules.

HIGH-SPEED BUFFER STORAGE

The increase in the internal performance of the Model 155 is achieved largely by the inclusion of a high-speed buffer storage unit. The 8K buffer is a standard feature and provides high-speed data access for CPU fetches. The CPU can obtain four bytes from the buffer in 230 nanoseconds (two cycles) or eight bytes in 345 nanoseconds (three cycles) if processor storage is not busy. If the buffer does not contain the data needed, the data must be obtained from processor storage. There is a four-byte-wide path between the CPU and processor storage that bypasses the buffer. With no channel interference, the CPU can access 4 bytes in 1.49 microseconds, 8 bytes in 1.61 microseconds, or 16 bytes in 1.96 microseconds from processor storage.

The conceptual data flow in the Model 155 is pictured in Figure 10.15.1. The data path within the CPU is four bytes wide.



CPU fetch from buffer	230 nanoseconds for 4 bytes 345 nanoseconds for 8 bytes
CPU fetch from processor storage	1.49 microseconds for 4 bytes 1.61 microseconds for 8 bytes 1.96 microseconds for 16 bytes
High-speed channels to or from processor storage	2.1 microsecond cycle for every 16 bytes

Figure 10.15.1 Conceptual data flow in the Model 155. Access times shown assume no interference.

The buffer control unit provides the interface between the buffer and the CPU and the buffer and the storage adapter. When a data fetch request is made by the CPU, the buffer control unit determines whether or not the requested data is in the high-speed buffer by interrogating the index array of the buffer's contents. If the data requested is present in the buffer and is valid, it is sent directly to the CPU without a processor storage reference. If the requested data is not currently in the buffer, or is no longer valid, a processor storage fetch is made and the data obtained is sent to the CPU. The data is also assigned a buffer location and stored in the buffer. When data is stored by the CPU, both the buffer and processor storage are updated if the contents of the processor storage location being altered are currently maintained in the buffer.

The channels never access the buffer directly. They read into and write from processor storage only (using the 4-byte path from the CPU to processor storage). When a channel stores data in processor storage, the index array is interrogated. If data from the affected

processor storage address is being maintained in the buffer, appropriate bits are set in the index array to indicate that this buffer data is no longer valid.

The algorithm used to maintain the contents of the high-speed buffer is relatively uncomplicated. It provides close to optimum buffer use at a price performance level consistent with the goals of the Model 155. The algorithm is designed to be transparent to the programmer so that no particular program structure need be adhered to in order to obtain close to optimum performance. Sample job step executions have shown that the data fetched by the CPU is in the buffer approximately 90% of the time.

Processor storage and the buffer are divided into 16-byte halfblocks within 32-byte blocks within 4K-byte rows, as illustrated in Figure 10.15.2. A row contains 128 blocks. The number of rows in processor storage is a function of its size. For example, a 1024K system has 256 rows.

The index array in the buffer control unit is used to maintain knowledge of the contents of the upper and lower compartments of the buffer. Each compartment is 4K bytes, or one row, in size. Each of the 128 block addresses in the index array contains two entries, one to describe a block in the upper 4K compartment and one to describe the corresponding block in the lower 4K compartment. An index array entry contains a processor storage row address, two valid bits, and an OK bit. When data from processor storage is placed in the buffer, its processor storage row address (bits 11-19 of the processor storage address) is placed in the index array entry for its block. The valid bits, one for each halfblock in the block, indicate the presence of valid data in that buffer block location. A valid bit is set on when a buffer halfblock is loaded from processor storage. The OK bit indicates that the corresponding block of the index array and buffer are functioning correctly. The OK bit for a block is set off when a malfunction associated with that block occurs. During system reset and IPL, all OK bits are set on and all valid bits are set off.

A buffer compartment may contain a complete row of processor storage, that is, all 128 blocks of a given row, or, more normally, blocks from several different processor storage rows. Block positions within each 4K row of processor storage are placed in corresponding block positions within the upper or lower compartment in the buffer. Therefore, each block of data within a 4K row of processor storage can be placed in only one of two buffer block locations. That is, the first 32 bytes (block 0) of each processor storage row (say addresses 4096-4127, 8192-8223, 12,188-12,219, etc.) can be placed in the first block location of the upper compartment or in the first block location of the lower compartment.

Buffer space is assigned on a block basis but is loaded a halfblock (16 bytes) at a time. A block in the buffer is assigned when the CPU fetches either halfblock of a corresponding block from a processor storage row. The other halfblock of the processor storage block is placed in the buffer only when (or if) referenced by the CPU. A buffer assignment latch is used in certain instances to determine which compartment of the buffer is to be assigned. The buffer assignment latch is set to indicate the compartment not referenced last; that is, if the CPU fetches data from the upper compartment, the latch is set on to indicate that the lower compartment is to be assigned next. If a CPU fetch causes data to be placed in the buffer, the buffer assignment latch setting is not altered. System reset causes the latch to be set off, indicating the upper compartment.

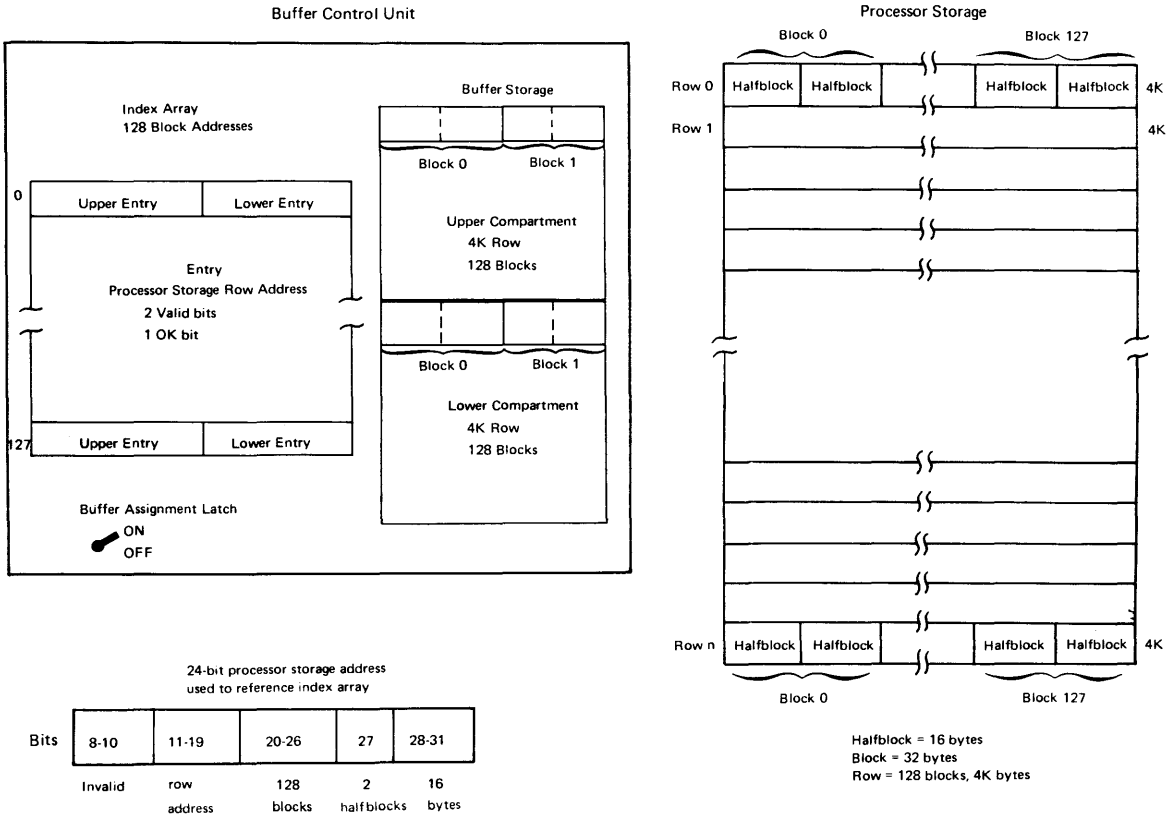


Figure 10.15.2. Buffer contents management

When a halfblock not contained in the buffer is requested by the CPU, it is assigned a buffer block in one compartment or the other, depending on the following conditions:

1. If the row address of the requested data compares equal to the row address in either compartment entry for the corresponding buffer block, that compartment is assigned.

2. If the corresponding blocks in both buffer compartments are totally available (all four validity bits off), the setting of the buffer assignment latch determines which compartment is assigned.

3. If the corresponding blocks in both buffer compartments have at least one halfblock already assigned to another row address (neither block is available), the latch setting determines the compartment used.

4. If the corresponding block of one compartment has at least one halfblock already assigned to another row address and the corresponding block of the other compartment is completely available, the unassigned compartment is used without regard to the latch setting.

See Figures 10.15.3 and 10.15.4 for an example of buffer allocation.

Extensive data validity checking is done on buffer data. Parity checking is performed on both data and control information. Data is checked as it enters and leaves the buffer. If a buffer component fails, the OK bit for that block is set off by the buffer control unit. This causes all subsequent CPU fetches for that block to be made from processor storage. A machine check occurs when a block in the buffer is deleted so that error recording can be done (discussed in the RAS section). A console switch and a microprogram instruction provide the ability to disable the entire buffer so that all data is fetched directly from processor storage, should this be necessary to allow continued system operation.

Sequence I

Assume that the buffer is empty, that the latch is set to the upper compartment, and that the program receives CPU control at processor storage location 102,400 (refer to Figures 10.15.3 and 10.15.4).

1. CPU fetches instruction 1 (102,400-102,403), which is not in the buffer.

2. Processor storage locations 102,400-102,415 are brought into the high-order halfblock of block 0 in the upper compartment (rule 2) and instruction 1 is sent to the CPU.

3. CPU executes instruction 1 - store into row 28, block 10. The buffer is not changed.

4. CPU fetches instruction 2 (102,404-102,407), which is contained in the buffer. The latch is set to the lower compartment.

5. CPU executes instruction 2 - fetch from locations 110,592-110,595, which are not in the buffer.

6. Locations 110,592-110,607 are brought into the high-order halfblock of block 0 in the lower compartment (rule 4) and the required data is sent to the CPU. The latch remains set to the lower compartment.

7. CPU fetches and executes instructions 3, 4, 5, and 6, all of which are register-to-register operations. All fetches are made to block 0 of the upper compartment. The buffer contents and latch setting remain the same.

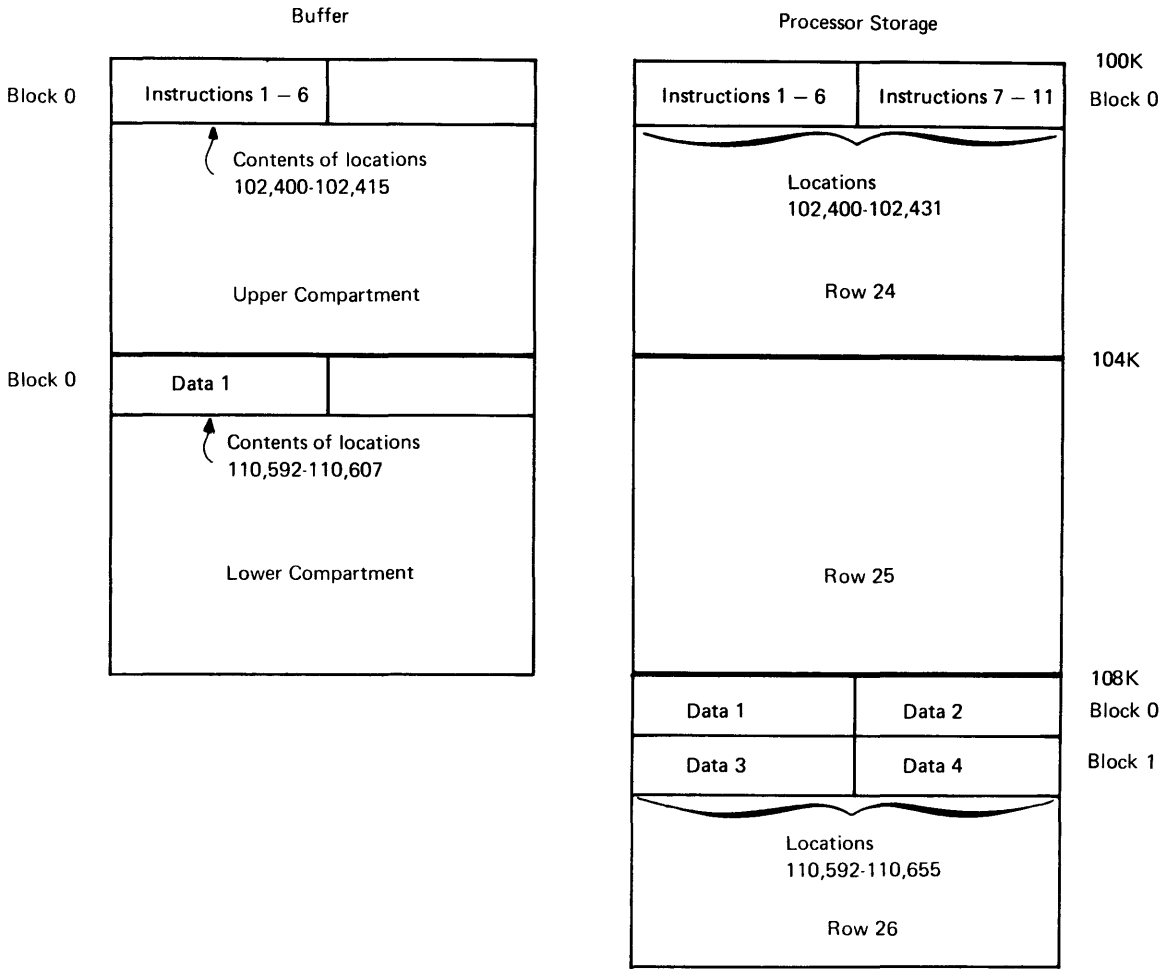


Figure 10.15.3. Buffer allocation example (part I)

Sequence 2

8. CPU fetches instruction 7 (102,416-102,419), which is not in the buffer.

9. Locations 102,416-102,431 are brought into the low-order halfblock of block 0 in the upper compartment (rule 1) and instruction 7 is sent to the CPU. The latch remains set to the lower compartment.

10. CPU executes instruction 7 - store into locations 110,596-110,599. The data is placed in the lower compartment of the buffer (high-order halfblock of block 0) and in processor storage. The latch remains set to the lower compartment.

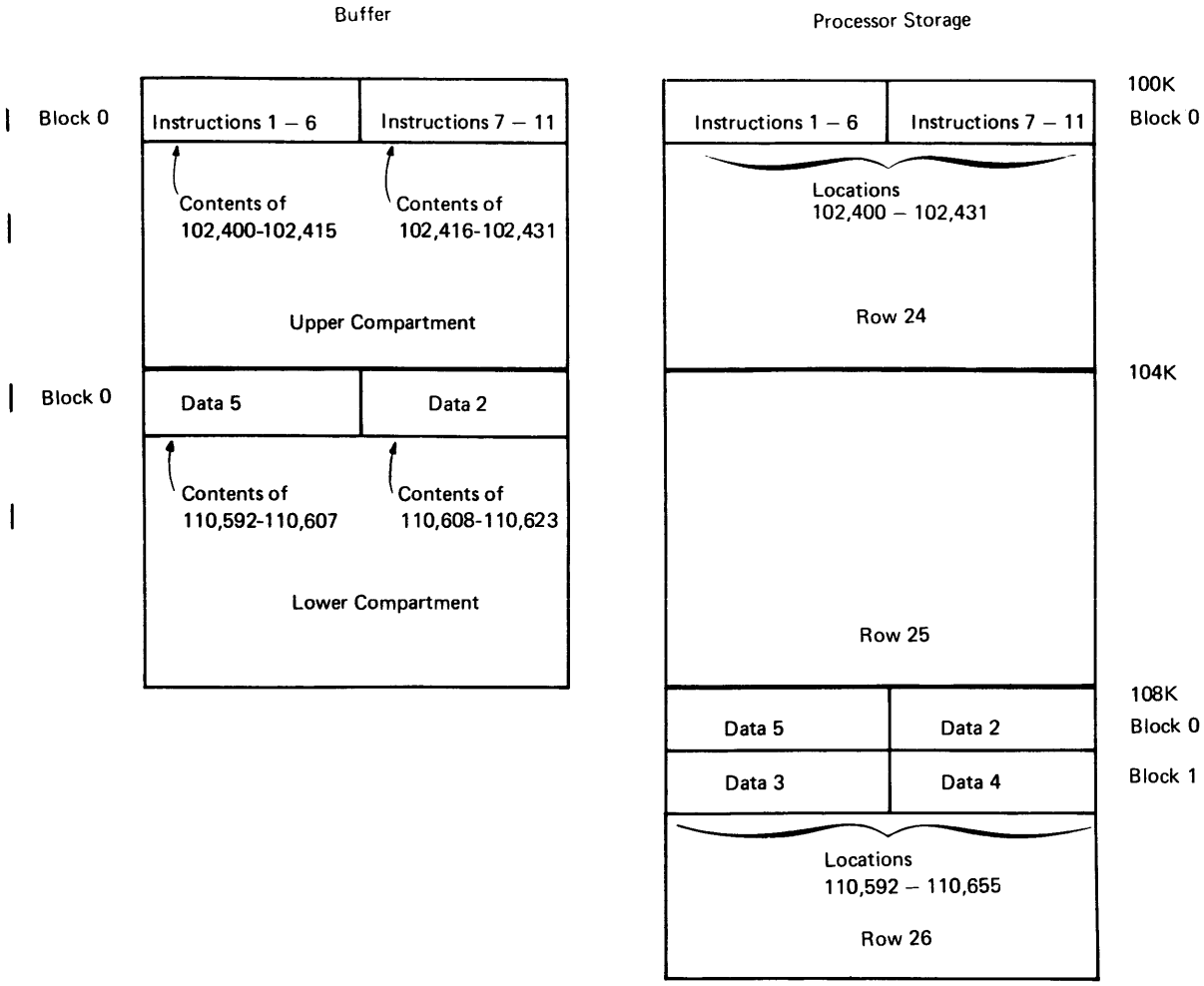
11. CPU fetches instruction 8 (102,420-102,423), which is in the upper compartment. The latch is set to the lower compartment.

12. CPU executes instruction 8 - fetch from locations 110,600-110,603. The data is sent to the CPU from the lower compartment. The latch is set to the upper compartment.

13. CPU fetches instruction 9 (102,424-102,427), which is in the upper compartment. The latch setting is not changed.

14. CPU executes instruction 9 - fetch from locations 110,608-110,611, which are not in the buffer.

15. Locations 110,608-110,623 are brought into the low-order halfblock of block 0 in the lower compartment (rule 1) and the data is sent to the CPU.



●Figure 10.15.4. Buffer allocation example (part II)

10:20 CHANNELS

The channels available on the Model 155 are functionally compatible with those of System/360 models but they can handle much faster data rates. The new block multiplexer channels are standard on the Model 155 and can increase the channel throughput of the system.

Two types of channels are available: byte multiplexer and block multiplexer. A byte multiplexer and block multiplexer channels 1 and 2 are standard on the Model 155. Block multiplexer channels 3, 4, and 5 are optional. A second byte multiplexer can be installed in place of channel 4 to provide up to 512 subchannels in one system.

A block multiplexer channel can operate in selector channel mode. Data is transferred between processor storage and a block multiplexer channel at the rate of 16 bytes in a 2.1 microsecond cycle whether the channel is in block multiplexer or selector mode.

Model 155 channels are integrated. They share with the CPU the use of ROS control storage, use of the CPU and processor storage data flow, and use of the CPU arithmetic logic unit. The byte multiplexer channel can interfere with CPU operations when it requires one of the shared components. Block multiplexer channels can interfere with both the CPU and the byte multiplexer channel. The channels interfere with CPU operations when an I/O operation is started and when it completes, as well as when a data transfer to or from processor storage is required. Sample timings have shown channel interference with CPU operations on a Model 155 to be less than on a Model 50 for any given data rate.

Comprehensive error checking has been incorporated in the basic design of the channel hardware. Checking is performed on the control logic in most areas and standard parity checking is done on the data flow. Improved error recovery hardware has also been included (discussed fully in the RAS section).

The standard instruction set also includes a new I/O instruction called HALT DEVICE. This instruction is specifically designed to stop an I/O operation on a particular device on a byte or block multiplexer channel without interfering with other I/O operations in progress on the channel. HALT DEVICE should always be used, instead of HALT I/O, to stop an I/O operation on a multiplexer channel.

The Channel-to-Channel adapter feature available for System/360 models is also an optional feature for the Model 155. It allows two System/370 channels or a System/370 and System/360 channel to be interconnected. Only one adapter can be installed on a Model 155.

BYTE MULTIPLEXER CHANNELS

The byte multiplexer channel provided for the Model 155 is functionally identical to the one available on System/360 Models 30, 40, and 50. It operates in byte interleave mode, permitting several slow-speed devices to operate concurrently, or in burst mode, allowing one high-speed device to function.

Depending on the size of processor storage, up to 256 subchannels are available on the standard byte multiplexer channel that is assigned channel address 0. The number of subchannels present determines the maximum number of concurrent I/O operations that can operate on the byte multiplexer channel. Each subchannel is associated with a unit control word (UCW), and the number of UCW's present in a Model 155 is related to the size of processor storage. UCW's are contained in "bump" storage, an extension of processor storage not program addressable. They are used to store channel register data in between data transfers to and from processor storage when devices are operating on the byte multiplexer channel.

A significant new optional feature is available for Model 155 systems with channel 3 installed and 768K or more of processor storage. The Second Byte Multiplexer Channel feature permits an additional byte multiplexer channel to be installed, in place of channel 4. Installation of a second byte multiplexer provides a total of 384 subchannels for 768K systems and 512 subchannels for systems with 1024K or more. This feature enhances the teleprocessing capabilities of the Model 155.

The following are examples of configurations that can operate on the Model 155. The second example is oriented toward a larger teleprocessing configuration.

1. Channel	I/O Data Rate
Channel 1 2305 Model 2 facility	1.5 MB
Channel 2 3330 facility	.806 MB
Channel 3 3330 facility	.806 MB
Channel 4 3330 facility	.806 MB
Channel 5 3330 facility	.806 MB
Byte Multiplexer	
Type 2 TELPAK Adapter	6.25 KB
2540 Card Read Punch	1.38 KB
1403 Printer	2.42 KB
Approximate aggregrate data rate	4.7 MB

2. Channel	I/O Data Rate
Channel 1 2305 Model 2 facility	1.5 MB
Channel 2 3330 facility	.806 MB
Channel 3 3420 Model 7 tape	.320 MB
Channel 4 3420 Model 7 tape	.320 MB
Byte Multiplexer	
Type 2 TELPAK Adapter	6.25 KB
Type 2 TELPAK Adapter	6.25 KB
2540 Card Read Punch	1.38 KB
1403 Printer	2.42 KB
Approximate aggregate data rate	3.0 MB

The higher data rates supported by Model 155 block multiplexer channels allow attachment of higher speed I/O devices that cannot be used with Models 40 or 50. For example, the 3330 facility with a data rate of 806 KB cannot be attached to Models 40 or 50.

BLOCK MULTIPLEXER CHANNELS

Block multiplexer channels are standard on the Model 155. Each block multiplexer channel installed can operate as a selector channel. The setting of a channel mode bit in a control register determines whether a high-speed channel operates in block multiplexer or selector mode. The mode bit is set to selector mode at IPL or on system reset and can be altered by programming at any time. When a START I/O instruction is issued to a high-speed channel on the Model 155, the setting of the channel mode bit determines the mode in which the subchannel involved will operate.

The block multiplexer channel is designed to increase system throughput by increasing the amount of data entering and leaving the system in a given period of time (the effective data rate). Better use of channel time is achieved by operating the channel in block multiplexing mode. A single block multiplexer channel can support interleaved, concurrent execution of multiple high-speed channel programs. The block multiplexer channel can be shared by multiple high-speed I/O devices operating concurrently, just as the byte multiplexer can be shared by multiple low-speed devices. Like the byte multiplexer, the block multiplexer channel has multiple

subchannels, each of which has an associated UCW in bump storage and can support one I/O operation.

Shown below is the total number of subchannels and UCW's present in a Model 155 system, based on its processor storage size and the manner in which they are distributed among the byte and block multiplexer channels.

Storage Size	Byte Multiplexer Channels Channel 0	Channel 4*	Block Multiplexer Channels Total Nonshared	Total Shared
256K	128	-	96	16
384K	192	-	160	16
512K	256	-	224	16
768K	256	128 *	352	16
1024K	256	256 *	480	16
1536K	256	256 *	480	16
2048K	256	256 *	480	16

*Optional

A UCW (or a subchannel) is referred to as nonshared if it is associated and can be used with one device only. Examples of Model 155 devices that must be attached to a nonshared subchannel are the following:

- 3330 facilities - one UCW per drive in the facility is required; a block of eight UCW's is always assigned.
- 2305 facilities - eight UCW's per 2305 module are required.
- 2540 Card Read Punch units - one UCW for the reader and one for the punch
- 1403 Printers attached to a 2821 Control Unit - one UCW per printer
- 3211 Printers - one UCW per printer
- 2250 Display Unit Models 1 and 3 - one UCW per unit

A shared UCW can be used by a set of devices, one device at a time. A shared UCW generally is assigned to a control unit that has multiple devices attached, only one of which can be in operation at a time. Therefore, tape units and direct access devices without rotational position sensing, such as the 2311, 2321, 2303, and 2314, are associated with shared UCW's.

The nonshared block multiplexer UCW's in a Model 155 are not hard wired to specific channels. System reset causes all nonshared UCW's to become unassigned and available for dynamic assignment to nonshared devices on any installed block multiplexer channel. When system operation begins, a nonshared UCW is assigned to an I/O device when the first START I/O instruction to the device is given as described below. (A UCW is not assigned unless the device is actually present.)

When the first START I/O is executed for a nonshared device, the channel determines whether a block of eight UCW's has been assigned to the range of eight addresses in which the device falls, 190-197, 230-237, etc. If none are allocated, a block of eight available UCW's is assigned to the channel for that device's address range. When the first START I/O is initiated to another I/O device on the same channel and in that block of addresses, the channel determines that a block of UCW's has already been assigned.

This process continues for all nonshared I/O devices until each device has a UCW assigned. If the pool of nonshared UCW's is empty when a request is made, the START I/O is executed without UCW assignment and the device operates as it would if attached to a selector channel (no disconnection occurs during command chaining, as explained under "Block Multiplexer Channel Operation").

Shared block multiplexer channel UCW's are assigned at system reset. When the Model 155 is installed, the CE assigns an address to each of the 16 shared UCW's in the system, using a set of 16 plug cards. After system reset, these UCW's are assigned to the devices attached to the preestablished shared addresses. The shared assignments can be changed by the CE if necessary, for example, if a nonshared device replaces a shared device.

Dynamic assignment of nonshared block multiplexer UCW's provides more flexibility in I/O configurations than does fixed assignment of an equal number of UCW's to each block multiplexer channel. All nonshared UCW's present are available for assignment no matter how many channels are installed, and UCW's are allocated among channels as needed, based on the I/O configuration and device usage.

BLOCK MULTIPLEXER CHANNEL OPERATION

A block multiplexer channel functions differently from a selector channel in the way in which it handles command-chained channel programs. A selector channel or a block multiplexer channel operating in selector mode executing a command-chained channel program is busy during the entire time the channel program is in operation, whether data transfer is occurring or not. A block multiplexer channel executing a command-chained channel program has the ability to disconnect from the operational channel program during certain non-data transfer operations. That is, a block multiplexer channel can be freed during a nonproductive activity, for example, during disk seeking and most record positioning, thereby allowing more data to be transferred per unit of channel busy time.

Block multiplexing operates as follows. Assume a block multiplexer channel is executing a channel program consisting of multiple command-chained CCW's. When channel end is presented without concurrent device end, the channel disconnects from the channel program and becomes available for an I/O operation on another device - even though the disconnected channel program is not complete. At channel disconnect time the subchannel and the device's control unit retain the information necessary to restart the disconnected channel program.

When the device signals that it is again ready for the channel (by presenting device end), its control unit attempts to regain use of the channel. If the channel is free at this time, the active channel registers are reloaded with the information previously saved (in the device's UCW), and the disconnected channel program is resumed at the appropriate CCW. If the channel is busy when reconnection is requested, the device must wait until it becomes available. Once multiple channel programs have been initiated on one channel, the interleaving of data transfer operations is controlled by block multiplexer channel hardware and the control units of the devices operating in block multiplexing mode.

To facilitate channel scheduling, a new interrupt condition, called channel available, has been defined for block multiplexer channels. At disconnect time for a channel program, the channel is available for the resumption of an uncompleted channel program previously started, or another channel program can be initiated. A channel available

interrupt occurs at disconnect time to indicate channel availability if a START I/O, TEST I/O, TEST CHANNEL, or HALT DEVICE instruction was issued previously while the block multiplexer channel was busy.

Two additional facts should be noted about block multiplexer channel operations:

1. When multiple channel programs are operating concurrently in block multiplexing mode, a device can regain control of the channel only when the channel is not busy. Thus, only cyclic devices (such as direct access devices with rotational position sensing) or buffered devices (such as the 2540 Card Read Punch and the 1403 Printer) can disconnect during the execution of a command-chained channel program on a block multiplexer channel and resume operation later.

2. Data transfer operations for concurrently operating devices on a block multiplexer channel are interleaved on a first-come, first-served basis as the desired records become available. Thus, devices are serviced in the order in which their records become available, not necessarily in the order in which their channel programs are initiated.

10:25 BLOCK MULTIPLEXING OPERATIONS WITH ROTATIONAL POSITION SENSING DEVICES

Rotational position sensing and multiple requesting are standard on 3330 and 2305 facilities. These two functions together with block multiplexing are designed to increase system throughput by increasing channel throughput.

The presence of RPS in the control unit of a direct access device enables it to operate in block multiplexing mode. The use of rotational position sensing reduces the number of channel programs that have to be initiated for direct access devices that require an arm positioning seek (such as the 3330 facility), frees channels more often during direct access device operations - specifically, during most of the time required to position a track to a desired record - and permits disk channel programs to be initiated sooner on block multiplexer channels than is possible with selector channels.

Multiple requesting is implemented in a direct access device control unit to enable it to handle concurrent execution of multiple RPS channel programs. The control unit of the 3330 facility, for example, can simultaneously control eight RPS channel programs, one on each of its drives.

In order to overlap seek operations for current direct access devices without RPS, channel scheduling routines must initiate two channel programs for each record read or write. The first is a stand-alone seek, which frees the channel as soon as the control unit accepts the seek address. (The control unit is also free during arm movement.) At the completion of the seek, a device-end interrupt is presented, and the data transfer channel program is subsequently initiated to search for the desired record and transfer the data. A selector channel is busy during the entire search operation that locates the desired disk record on the track. Search time can be significantly greater than data transfer time for disk records smaller than half a track in size. Search time averages one-half of a rotation for a read or write (8.3 ms for a 3330) and requires a full rotation, less record write time, for a write verification chained from a write.

Use of RPS reduces the time the channel is busy searching for a disk record. It permits the SEARCH command to be initiated just before

the desired record is to come under the read/write heads, that is, when the desired rotational position is reached. To accomplish this, a "sector" concept is employed. The tracks in each cylinder of a direct access device are considered to consist of equally spaced sectors (the number of sectors varies by device). Track formatting is unchanged but each record has a sector location as well as a record address. A sector is not physically indicated on disk tracks, but is the length of the track arc that passes under the read/write heads in one sector time. For the 3330 facility, for example, sector time is defined to be approximately 130 microseconds. Thus, there are 128 sectors per track on the 3330.

A disk control unit with RPS and multiple requesting can determine the sector currently under the heads of each of its drives. A sector counter is contained in each drive. The counter is incremented once every sector time period and set to zero each time the index marker passes under the heads. The sector in which a record falls is a function of the length of all records that precede it and of its sequential position on the track. Therefore, sector location can be calculated for fixed-length records.

Two new disk commands are provided for use with rotational position sensing:

SET SECTOR
READ SECTOR

If the sector address of a record is known or can be calculated, a SET SECTOR command can be included in the disk channel program to cause the control unit to look for the designated sector. Once the control unit accepts the sector number provided by a SET SECTOR command, both the block multiplexer channel and the disk control unit disconnect and are available for another I/O operation. When SET SECTOR is used for positioning, the time the channel is busy searching for a record is reduced from an average of 8.3 ms to an average of 250 microseconds for the 3330 facility. (Allowing for the worst case of speed variation and for disk pack interchange, the search time for a record, from sector found to beginning of desired record, can vary from 120 microseconds to 380 microseconds on a 3330 facility.)

The READ SECTOR command is useful for sequential disk processing and for write verification. When chained from a READ, WRITE, or SEARCH command, READ SECTOR provides the sector number required to access the record processed by the previous CCW. This sector number can be used to reposition the track to the record in order to verify the record just written or in order to read or write the next sequential record. These two new sector commands, used in conjunction with the block multiplexer channel, permit a single command-chained channel program to be initiated for each disk operation that frees the channel and disk control unit during seek and rotational positioning operations.

When record ID is known, the two channel programs shown below can be used to retrieve a record directly from an OS BDAM data set on a direct access device without RPS, such as the 2314. (Key was not written). The seek operation can be overlapped with other seeks and one data transfer operation on the same selector channel.

Channel program 1. Initiate the stand-alone seek to position the disk arm.

Command Chaining Flag	Command		Selector Channel and Disk Control Unit Status
	SEEK	(Seek address)	Free as soon as the control unit accepts the seek address

Channel program 2. Initiate the data transfer operation after the seek is complete.

Command Chaining Flag	Command		Selector Channel and Disk Control Unit Status
CC	SEARCH ID EQ	(ID - sequential position on the track)	Busy (for 12.5 ms on the average for a 2314)
CC	TIC	(Back to search if ID not equal)	
	READ DATA	(Processor storage address of input area)	Busy

When the sector address is known or can be calculated, the channel program below can be used to retrieve a record from the same BDAM data set on a 3330 facility attached to a block multiplexer channel. The records are fixed-length standard format and sector numbers are calculated from record ID (by data management).

Channel program 1. Initiate the seek and data transfer operation.

Command Chaining Flag	Command		Block Multiplexer Channel and Disk Control Unit Status
CC	SEEK	(Seek address)	Free during arm motion
CC	SET SECTOR	(Sector number of sector preceding desired record)	Free until sector found
CC	SEARCH ID EQ	(ID - sequential position on track)	Busy (250 microseconds average for a 3330)
CC	TIC	(Back to search if ID is not equal. With the logic shown, the first ID inspected normally is that of the desired record and the TIC command is not executed.)	Busy
	READ DATA	Processor storage address of input area)	Busy

The preceding example indicates the advantages of rotational position sensing and block multiplexing:

- Only one channel program is required to locate a disk record and transfer the data, thereby eliminating a stand-alone-seek I/O interrupt and the I/O supervisor processing required to schedule a data transfer channel program. A channel available interrupt may occur, however, during channel program execution.
- The channel and disk control unit are free during arm motion and rotational positioning, allowing seek and set sector operations to be overlapped with other I/O operations on that control unit and channel. Implementation of multiple requesting permits a disk control unit to control concurrent execution of multiple RPS channel programs in order to overlap seek and set sector operations for its drives.

Performance improvement gains achieved on block multiplexer channels are not due entirely to the fact that direct access device rotational delays are overlapped. Also important is the ability to initiate seek commands a number of milliseconds earlier, because a block multiplexer channel is free. The initiation of stand-alone seeks on a selector channel is delayed during search and data transfer operations. On a block multiplexer channel, seeks can be initiated during rotational positioning, since the channel and disk control unit are not busy.

The concepts of rotational position sensing as described for the 3330 facility also apply to the 2305 facility. Since an arm positioning seek is not required for the 2305, the channel program issued by an RPS access method or a user can be the same as shown for the 3330 facility except that the first command will not be a seek requiring mechanical motion.

SUMMARY OF BLOCK MULTIPLEXING OPERATIONS WITH I/O DEVICES

The following summarizes how direct access devices without and with RPS and other I/O devices operate on a block multiplexer channel on a Model 155 when executing a command-chained channel program.

1. Direct access devices without RPS (2311, 2321, 2314, 2303) assigned to a shared subchannel operate in the same way whether the channel is in block multiplexer or selector mode. That is, the channel and the disk control unit are busy during the entire time a command-chained disk channel program is in operation. (There is no disconnection after a chained seek.)

2. The 3330 facility executing a command-chained channel program on a block multiplexer channel disconnects after the control unit accepts an arm positioning seek that causes arm movement. Reconnection is attempted when the arm reaches its destination and signals device end. The 3330 facility also disconnects when its control unit accepts a SET SECTOR command. When the sector specified arrives under the read/write heads, the control unit attempts to reconnect and resume the CCW chain. If the channel is busy, the control unit repeats the reconnection procedure each time the specified sector position is reached.

3. The 2305 facility executing a command-chained channel program disconnects when the control unit accepts a SET SECTOR command. Reconnection occurs as described for the 3330 facility.

4. All currently announced tape drives operate exactly the same whether the channel is in block multiplexer or selector mode. That is, the channel is busy during the entire time a command-chained channel program is in operation.

5. Buffered card and print devices (or devices operating with buffered control units) disconnect during the mechanical motion of the device. Reconnection occurs later to fill or empty the associated buffer. For example, a 1403 Printer attached to a 2821 control unit connected to a channel operating in block multiplexing mode disconnects from the channel during print time and carriage motion. Reconnection occurs when the channel is free to transfer the data for the next line to the 2821 buffer in burst mode.

6. Any other I/O device that presents channel end without simultaneous device end disconnects from a block multiplexer channel when command chaining if it is operating on a nonshared subchannel.

Section 60:10 discusses planning for installation of RPS devices on block multiplexer channels.

10:30 SYSTEM CONTROL PANEL AND SYSTEM CONSOLE

SYSTEM CONTROL PANEL

The system control panel attached to the end of the Model 155 CPU contains all the switches and indicators required to operate the system. The console layout - its location and the grouping of controls and indicators - was designed with human factors in mind. The five-foot high CPU frame that contains the control panel permits most operators an unrestricted view of the machine area.

System controls are divided into three sections similar to the control sections of System/360 models. There is an operator control, an operator intervention, and a maintenance section. A CE meter key is not required to unlock any section.

One new item in the operator control section is the clock security lever switch, which is used in conjunction with programmed setting of the time of day clock. The CE intervention and maintenance control section contains two new controls. First, there is a bypass-buffer lever, which can be set to disable the entire high-speed buffer and thereby cause all CPU fetches to be made directly from processor storage. Second, a diagnostic control switch and a START DIAGNOSTIC button are provided to be used together to select and perform microdiagnostic tests for system components: processor storage, CPU and I/O local storage, and buffer storage. (Microdiagnostic tests are discussed in Section 50:15.)

Located beneath the console reading board of the Model 155 is a device that provides read-only storage for nonresident system microdiagnostics that are to be used by customer engineers. The recording medium used for this device is an interchangeable magnetic disk cartridge. Prewritten disk cartridges containing a comprehensive set of microdiagnostics will be shipped to each installation.

The CPU contains a service adapter that provides an interface between the CPU and a diagnostic device. By means of this interface, microdiagnostics can be read into the Model 155 from the magnetic disk cartridge contained on the device. This device is a basic debugging tool for customer engineers. The Model 155 contains a small "hard core" set of circuitry that must be operational in order for diagnostic tests to be executed. Using this basic circuitry, microdiagnostics from the device are executed. A building-block technique of verifying hardware circuitry is employed that enables rapid diagnosis of system malfunctions.

SYSTEM CONSOLE

The new microprogram-controlled 15-cps 3210 Console Printer-Keyboard can be attached to the left-hand or right-hand extension of the Model 155 console reading board for use as the operator console device. Alternately, the 3215 High-Speed Console Printer-Keyboard with a print speed of 85-cps can be used. The 1052 Model 7 Printer-Keyboard cannot be attached as the primary system console device.

The two new printer-keyboards are functionally compatible and program compatible with the 1052. Their keyboards are the same as that of the 1052 except that the alternate coding key has been removed from the new printer-keyboards and the EOB and cancel keys are separate pushbuttons.

Both the 3210 Console and the 3215 High-Speed Console Printer-Keyboards have a new alter/display mode of operation (not implemented for the 1052), which will be of benefit to customer engineers and operators. After the system is placed in manual mode, this new mode is set by pressing the alter/display key, which places the console under microprogram control. In this mode, data can be placed in, or printed from, the following:

- Processor storage
- General, floating-point, and control registers
- The current PSW

A mnemonic is entered to indicate the function to be performed. Other data, such as the starting or ending storage address and the

data to be entered, must be supplied in hexadecimal format. Both uppercase and lowercase may be used. If an error is made (incorrect mnemonic, storage address, or hexadecimal data characters, etc.), the microprogram detects the error and the operation can then be restarted. The microprogram also handles carriage returns automatically during data displays and prints eight words of hexadecimal characters per line until the end key is depressed.

The Second Console Printer-Keyboard optional feature allows a 3210 Console Printer-Keyboard to be connected to the system via a cable up to 50 feet long so that it can function as a remote alternate or additional console (either a 3210 or 3215 printer-keyboard can be the primary console). This remote printer-keyboard cannot be used for alter/display operations. In addition, a 2150 Console and 1052 Model 7 combination can be installed as an alternate or additional console.

10:35 STANDARD AND OPTIONAL SYSTEM FEATURES

STANDARD FEATURES

Standard features for the System/370 Model 155 are:

- Instruction set that includes binary, decimal, and floating-point arithmetic, the new general purpose instructions, and the instructions required to handle the new architecture. New instructions for System/370 Model 155 are:
  - COMPARE LOGICAL CHARACTERS UNDER MASK
  - COMPARE LOGICAL LONG
  - HALT DEVICE
  - INSERT CHARACTERS UNDER MASK
  - LOAD CONTROL
  - MOVE LONG
  - SET CLOCK
  - SHIFT AND ROUND DECIMAL
  - STORE CHANNEL ID
  - STORE CHARACTERS UNDER MASK
  - STORE CLOCK
  - STORE CPU ID
  - STORE CONTROL
- CPU retry
- Interval timer
- Time of day clock
- Expanded machine check interrupt
- ECC on processor storage
- Byte boundary alignment
- Storage and fetch protection
- High-speed buffer storage - 8K bytes
- Byte multiplexer channel 0
- Block multiplexer channels 1 and 2 (includes selector channel mode)
- Channel retry data in ECSW
- Device for microdiagnostic routine loading

OPTIONAL FEATURES

Optional features for the System/370 Model 155, all of which can be field installed, are:

- Extended Precision Floating Point
- 1401/1440/1460, 1410/7010 Compatibility Feature
- OS/DOS Compatibility Feature
- Direct Control
- Block multiplexer channels 3, 4, and 5 (includes selector channel mode)
- Second Byte Multiplexer Channel** - replaces channel 4
- Channel-to-Channel Adapter
- Console Printer-Keyboard Adapter* - for 3210 Console
- Second Console Printer-Keyboard Adapter - for remote 3210 Console
- High-Speed Console Adapter* - for 3215 Printer-Keyboard
- 2150 Console and 1052 Model 7 combination as an alternate or additional console.

*Either the 3210 Console Printer-Keyboard or the 3215 High-Speed Console must be installed as the primary system console.

**Channel 3 is a prerequisite.

SECTION 20: I/O DEVICES

20:05 I/O DEVICE SUPPORT

Most presently announced I/O devices that can be attached to System/360 Models 40 and 50 can be attached to the System/370 Model 155. The following I/O devices are not included in standard Model 155 configurations:

1052 M7 Printer Keyboard - except attached to a 2150 Console
1231 Optical Mark Page Reader
1259 M2 Magnetic Character Reader
1285 Optical Reader
1404 Printer
1418 Optical Character Reader
1428 Alphameric Optical Reader
1827 Data Control Unit (for attachment of 1800 system analog and/or digital control units to the Model 155)
2301 Drum Storage
2302 Disk Storage
7340 Hypertape Drive
7772 Audio Response Unit

The 1287 Optical Reader and 1288 Optical Page Reader can be attached to a byte multiplexer channel only. In addition, 2361 Core Storage cannot be attached to a Model 155.

New I/O devices for the Model 155 are:

- the 3330 facility - attaches only to a block multiplexer channel
- the 2305 facility Model 2 - attaches only to a block multiplexer channel
- the 3211 Printer - attaches to any Model 155 channel
- the 3803/3420 Magnetic Tape Subsystem - attaches to any Model 155 channel

The 3330 and 2305 facilities represent significant advancements in direct access device technology. They provide larger online data capacity, faster data rates and access, and expanded error correction features. Both have rotational position sensing and multiple requesting as standard features.

The 3330 represents the latest direct access device with removable, interchangeable disk packs. It embodies new data recording and access technology. The 2305 facility is a major extension of the nonremovable, high-speed, fixed-head direct access storage concept.

The 3803/3420 tape subsystem incorporates all the latest advances in tape speed, design, and technology. It offers new features and enhanced reliability, availability, and serviceability to 2400-series magnetic tape unit users.

The major new characteristics of the 3330 and 2305 facilities, the 3211 Printer, and the 3803/3420 tape subsystem are discussed in the following subsections.

20:10 3330 DISK STORAGE AND 3830 STORAGE CONTROL

The 3330 facility is a modular, large-capacity, high-performance direct access storage subsystem. The 3330 facility consists of 3830 Storage Control and from one to four 3330 Disk Storage modules. A 3330 module contains a pair of independent disk storage drives, as shown in Figure 20.10.1. The new removable 3336 Disk Pack is used for data storage. Usage meters are contained in the 3830 control unit and in each 3330 module.

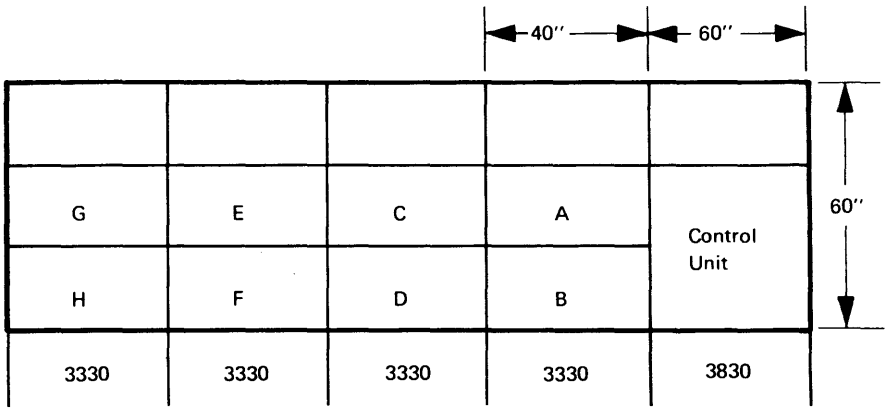


Figure 20.10.1. The 3330 facility

Drives are mounted in powered drawers that are opened and closed by a switch on the operator control panel on the 3330 module. Logical address plugs are supplied, as for the 2314, in addition to a CE service plug. The latter is used when inline diagnostics are to be executed.

Facility configurations and maximum capacities, using full track records, are shown below.

3830 Storage Control + one 3330 module 200 megabytes
3830 Storage Control + two 3330 modules 400 megabytes
3830 Storage Control + three 3330 modules 600 megabytes
3830 Storage Control + four 3330 modules 800 megabytes

Functionally, the 3330 facility provides more capabilities than the 2314, particularly in the areas of performance and availability. The 3330 supports all the standard 2314 commands (except the file scan commands) in addition to several new operations, including RPS and error recovery commands. (Table 20.10.3, at the end of this subsection, compares 3330 and 2314 features.) The 3330 facility also is an attractive growth device for the 2321 Data Cell Drive.

The new, removable 3336 Disk Packs are interchangeable across 3330 disk drives but are not interchangeable with the 2316 Disk Packs used on 2314 disk drives (Table 20.10.2 compares disk pack characteristics). Like 2316 packs, 3336 Disk Packs will be initialized in the factory with home addresses and capacity records (R0). Up to 20 defective tracks per pack will be flagged and have alternates assigned. The quick DASDI routine (part of the IEHDASDR utility), currently available for processing 1316 and 2316 packs, will support 3336 packs. Quick DASDI writes the volume label, the VTOC, and IPL records, if requested, but bypasses track analysis. It also determines the number of flagged tracks and places this data in the VTOC.

Table 20.10.1 compares the capacity and timing characteristics of the 3330 facility with those of the 2314 facility and the 2321 Data

Cell Drive. The increase in capacity achieved by replacing a 2314 or a 2321 with a 3330 depends upon the block size chosen for the data on the 3330. For example, if the 2314 full track block size of 7294 bytes is maintained for a given data set on the 3330 to avoid programming changes, the 3330 yields a 91% increase in full pack capacity (almost twice the capacity). However, reblocking to a full track on the 3330, 13,030 bytes, yields a 242% full pack capacity increase. If there is not enough processor storage available to allocate I/O areas of 13,030 bytes, lowering the 3330 block size used to one half of a 3330 track yields a 239% increase in full pack capacity.

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If a 2321 is replaced by a 3330, six full track blocks of data from the 2321 (2000 bytes/2321 track) can be placed on each 3330 track, if full track blocking is used, for a total of 92,112,000 bytes per 3336 pack (12,000 bytes X 7676 tracks per 3336). Thus, slightly over four 3336 packs provide the capacity equivalent of ten data cells, or a full 2321 drive, if full tracks are used. A full ten data cells, blocked full track, also can be contained in slightly more than four 3336 packs if half-track blocking is used on the 3336.

Table 20.10.1 Capacity and timing characteristics of the 3330 and 2314 facilities and the 2321 Data Cell Drive

Characteristic	3330	2314	2321
Capacity in bytes truncated to the nearest thousand (full track records)			
Pack or cell	100,018,000	29,176,000	39,200,000
Facility or Data Cell Drive			
2 drives/cells	200,036,000	58,352,000	78,400,000
4 drives/cells	400,073,000	116,704,000	156,800,000
6 drives/cells	600,109,000	175,056,000	235,200,000
8 drives/cells	800,146,000	233,408,000	313,600,000
10 cells	-	-	392,000,000
Access time in ms			
Maximum	55	130	600 (for strip select and load)
Average	30	60	175 (minimum for strip select and load)
Average cylinder-to-cylinder	10	25	95 (on a strip)
Rotation time in ms	16.7	25	50 (strip on drum)
Rotation speed (rpm)	3600	2400	1200
Data transfer rate (KB)	806	312	55

Table 20.10.2 3336 and 2316 Disk Pack characteristics

Characteristic	3336	2316
Number of disks per pack	12	13
Number of recording disks	10	11
Number of recording surfaces (recorded tracks per pack)	19	20
Disk thickness in inches	.075	.050
Disk diameter in inches	14	14
Disk pack weight in pounds	20	15
Disk pack maximum capacity in millions of bytes	100	29.1
Full track capacity in bytes	13,030	7,294
Cylinders per pack	404 plus 7 alternates	200 plus 3 alternates
Tracks per cylinder	19	20
Tracks per pack	7,676	4,000

Self-formatting records are written on 3336 packs in the same manner as they are on 2316 packs. However, each physical area written (count, key, and data) has a field of error correction code appended to it

for the purpose of data validity checking by the control unit instead of the cyclic check area used on the 2314.

The 3830 control unit is microprogram controlled. Read/write monolithic storage contained in the control unit is used for microprogram residence. The control unit also contains a device that reads interchangeable magnetic cartridges (like the device under the system console reading board). This device is used for microprogram backup storage and for storage of nonresident diagnostics for the 3330 facility. During a 3330 facility power-on sequence, the functional microprogram is loaded from the device into control storage within the control unit. Therefore, many engineering changes can be installed merely by replacing the magnetic disk cartridge in use with another cartridge that contains the new microprogram.

The 3330 facility also incorporates new error detection, correction, and logging features, designed to improve its availability and serviceability. The following features are implemented in the 3330 that are not provided by previously announced direct access devices:

- I/O error routine correction of recoverable data errors on read operations with data supplied by the control unit in sense bytes
- Command retry initiated by the control unit to attempt hardware correction of certain errors without programming assistance
- Error logging by the control unit in its control storage of successful command retry operations
- Inline diagnostic tests contained on magnetic disk cartridges, which can be run on a single drive to diagnose hardware malfunctions while other drives in the facility continue normal operations. (Inline diagnostics are provided currently only for 2314 facilities.)

Recovery of correctable data area errors. When the control unit detects a correctable data error during the reading of the data portion of a record, it generates the information necessary to correct the erroneous bytes. The sense bytes presented by the control unit contain a pattern of corrective bits and a displacement value to indicate which of the bytes transferred to processor storage contain the errors. The disk error recovery program need only EXCLUSIVE OR (logical operation) the corrective bit pattern with the error bytes in the input area in processor storage to correct the errors.

Command retry. Error correction (without programming assistance) is performed by a channel/control unit command retry procedure without an intervening I/O interrupt in the following five situations:

1. When a correctable data error occurs during a search or read operation on home address, record count, or record key.

   During a search or read operation the home address, count, or key read from the disk track is placed in a buffer in control storage within the control unit. When a correctable data error occurs, the control unit corrects the data in the buffer and reissues the command that caused the error. During reorientation to the record, the control unit disconnects and frees the block multiplexer channel. When the failing search or read command is reexecuted, the corrected data in the buffer is used instead of the data actually on the track.

2. When an uncorrectable data error is detected on any portion of the record during a read or a search operation.

The failing CCW is reissued twice by the control unit. If one of the two retries is successful, the channel program continues normally.

3. When a seek malfunction is detected.

   The control unit retries the command ten times in an attempt to position the arm correctly.

4. When an alternate or defective track condition is recognized before data transfer begins.

   The control unit determines the location of the alternate or defective track (from R0 on the track), initiates a seek to this track, and orients to the index point. When this sequence completes, the original command is reissued by the control unit. This is a programmed procedure for previously announced System/360 direct access devices.

5. When a command overrun (or late command chaining) condition occurs during execution of a channel program because of interference from another channel or the CPU.

   The control unit initiates a retry of the command that was late.

Error logging. Usage and error counters for each drive in the facility are maintained continuously in the control unit. The usage counters are used to accumulate the number of bytes read and seeks issued. The error counters are used to accumulate the number of seek, correctable data, and uncorrectable data errors that were retried successfully by a command retry procedure, as already described. When a counter reaches its threshold or when a pack is removed from a drive, the control unit indicates the condition via a unit check when the next I/O operation is initiated to the drive. Counter data can be obtained and counters can be reset by issuing a SENSE or READ LOG command. These statistics can then be logged in the system error data set for later diagnosis.

Inline diagnostic tests. The 3830 control unit can execute diagnostic tests on a malfunctioning drive while normal operations take place on the remaining drives in the facility. When the CE inserts the service address plug in the malfunctioning drive, diagnostic programs contained on a magnetic disk cartridge are read by the device in the control unit. Diagnostics can be executed on that drive by the customer engineer using the CE panel on the 3830 control unit. Operationally, the drive is offline to the control unit, and physically the drive is offline to the operating system.

Online testing of the 3330 facility can be performed under OLTEP control, as usual. Both OLT's and diagnostic programs contained in the OLT library can be executed on a malfunctioning drive via OLTEP. The diagnostic tests are loaded into control storage in the control unit from the OLT library. Operationally, the 3330 drive is online to the control unit but is logically offline to the operating system.

Inline and online testing allows CE diagnosis and repair of most 3330 failures without the necessity of taking the entire 3330 facility out of the system configuration.

The 3330 facility offers more than additional capacity, faster access, and attractive price performance. The 3330 facility is actually a subsystem in itself. The control unit can control the concurrent execution of one RPS channel program on each of its drives and can handle functions such as error correction and logging, which normally must be programmed, thereby relieving the control program of these

activities. In addition, the availability and serviceability of the 3330 are improved by the implementation of new automatic error correction features, by use of inline diagnostics, and by the speed and ease of engineering change installation. These factors add to the improvement of total system availability.

Table 20.10.3 Hardware features of 3330 and 2314 facilities

Feature	3330	2314
Number of drives per facility	2,4,6, or 8	1,2,3,4,5,6,7, or 8 (A ninth can be included as a spare only.)
Removable interchangeable disk packs	Yes	Yes
Removable address plugs	Yes	Yes
Record overflow feature	Standard	Standard
File scan feature	Not available	Standard
Multiple track operations	Standard	Standard
Two-channel switch	Optional	Optional
Second control unit (to permit two concurrent data transfer operations on a facility)	Not available	Optional (2844 Auxiliary Storage Control)
Rotational position sensing	Standard (128 sectors/track)	Not available
Multiple requesting	The control unit can concurrently handle one channel program on each of its drives.	Not available
Command retry by control unit and channel	Standard	Not implemented
Error correction data presented by control unit	Yes	No
Writable storage in control unit loaded from a magnetic disk cartridge	Yes	No
Inline diagnostic tests initiated via the CE panel in the facility	Standard	Standard
Inline diagnostic tests initiated via the system console	Standard	Not implemented

20:15 THE 2305 FIXED HEAD STORAGE MODULE AND 2835 STORAGE CONTROL MODEL 2

One or two 2305 Fixed Head Storage Modules can be attached to 2835 Storage Control. Each module contains six nonremovable rotating disks on which data is recorded. Read/write heads, called recording elements, are fixed in position to access each track on the twelve recording surfaces so that no arm motion is required. (See Tables 20.15.1 through 20.15.3 at the end of this subsection for a comparison of 2305 Model 2 and 2303 Drum Storage characteristics and capacities.) Up to four 2305 Model 2 facilities can be attached to one Model 155, two on channel 1 and two on channel 2.

Spare, or alternate, tracks are provided in 2305 modules and must be wired in by a customer engineer to replace defective recording tracks. However, one spare track is available for assignment by the

alternate track assignment utility program when a permanent track error occurs on a recording track during processing. Once a spare has been assigned as an alternate track, the hardware automatically accesses the alternate track when the defective recording track is addressed. This is called alternate track sparing. Switching to an assigned alternate track during processing is a programmed action for currently announced direct access devices.

The 2835 control unit provides new error correction facilities similar to those of the 3830 control unit. Recorded data areas within self-formatting records have ten correction code bytes appended to them instead of a two-byte cyclic check code. When certain types of data errors occur during the reading of the data portion of a record, the control unit can determine the bits in error and generate correction data. This recovery information is presented to the error routine via the sense bytes and can be used to correct the invalid record in processor storage (as described for the 3330 facility).

A command retry feature is implemented in the 2835. This feature permits certain types of failing commands to be reissued automatically by the channel, when requested by the control unit, without an intervening I/O interrupt. For example, when a count or key area is read erroneously, the control unit retries the command once. If the error is not corrected by the retry, the control unit corrects the data in its own buffer, reexecutes the failing read, and presents the corrected data from the buffer instead of reading it from the track.

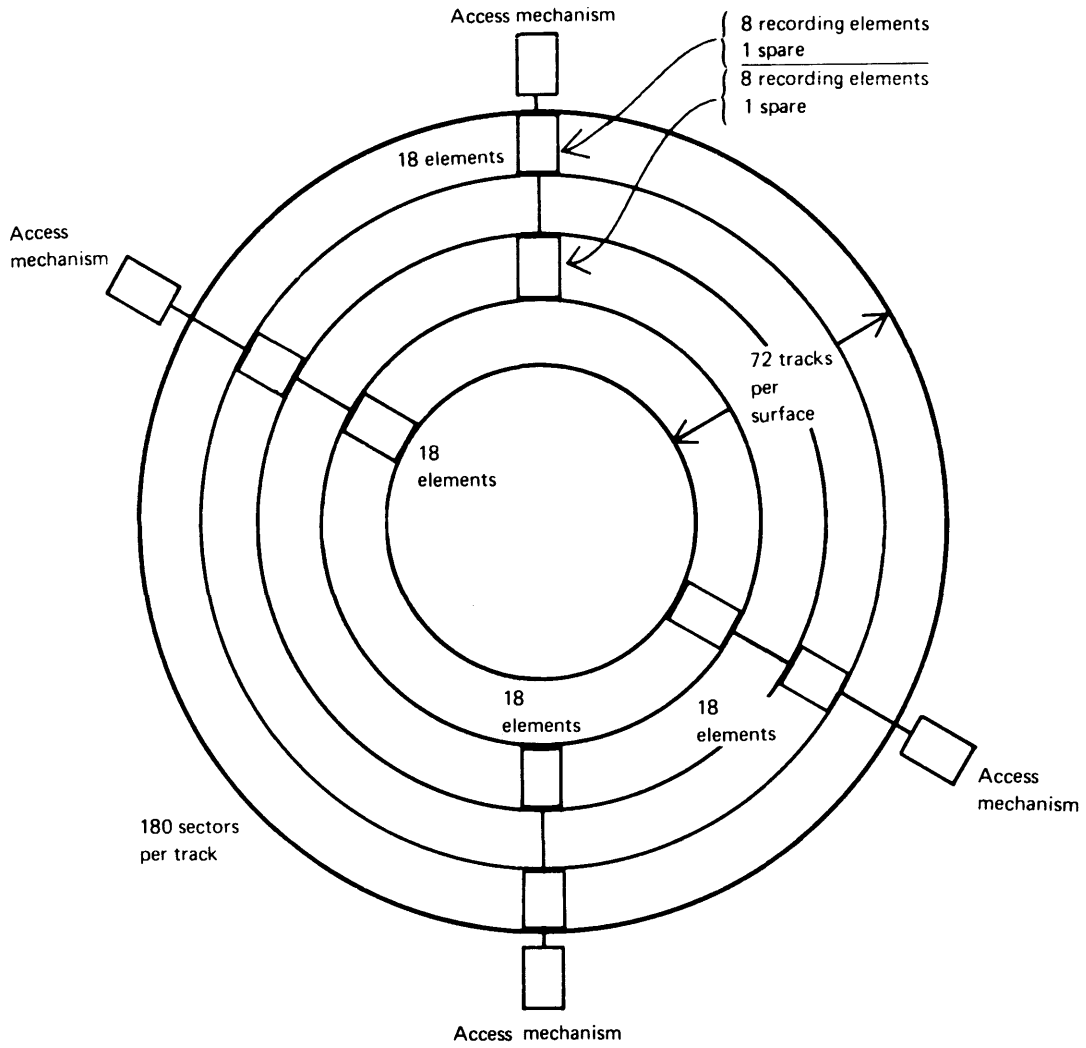
Like the 3830 control unit, the 2835 contains a device that reads magnetic disk cartridges containing the control unit microprogram and diagnostic routines.

DATA RECORDING

Data tracks on the 2305 Model 2 facility are formatted in the same manner as on System/360 direct access devices except for the absence of a home address on each track. There are 768 recording tracks and 96 spare tracks in one module. One recording element is positioned over each track. Each of the twelve surfaces contains 72 tracks, 64 recording and 8 spare. The spare tracks are interspersed among the 72 tracks so that every ninth track is a spare. Data is recorded serially by bit on each track.

Four nonmovable access mechanisms are positioned around the rotating disks as shown in Figure 20.15.1. Each access mechanism contains two groups of 9 recording elements per surface (for a total of 16 recording and 2 spare elements) and accesses one-quarter of the tracks on each surface. A group of 8 recording elements accesses every other track. The outermost element group of the access mechanism at the top of Figure 20.15.1 accesses data tracks 1, 3, 5, ..., 15, while data tracks 2, 4, 6, ..., 16 are accessed by the outermost element group of the access mechanism at the bottom of the diagram.

There are 180 sectors per track on the 2305 Model 2. When RPS is used, the search time, from sector found to beginning of desired record, ranges from a minimum of 114 microseconds to a maximum of 198 microseconds.



64 recording tracks/surface x 12 = 768 recording tracks/module
8 spare tracks/surface x 12 = 96 spare tracks/module
216 recording elements (read/write heads)/access mechanism x 4 = 864 recording elements

Figure 20.15.1. Top view of a 2305 Model 2 disk surface

ROTATIONAL POSITION SENSING AND MULTIPLE REQUESTING

RPS is a standard feature of the 2835 control unit as is the other new capability called multiple requesting, which allows up to eight channel programs to be active concurrently on each of the two 2305 modules that can be attached to the control unit. In other words, a 2305 module can be viewed as eight logical devices, although physically it is only one device.

As described previously, rotational position sensing and block multiplexing permit a direct access device to disconnect during SET SECTOR operations. These facilities, used in conjunction with the multiple requesting feature, permit concurrent operations to take place on each 2305 module in a facility. Thus, the effective data rate of a module can be increased substantially.

The multiple requesting capability is implemented by associating eight logical device addresses (0-7) with a 2305 module. Each logical device address is also assigned to a specific subchannel of a block multiplexer channel and a specific register (0-7) in the 2835 control unit. When a channel program is initiated, it is associated with an available logical device address by data management (I/O supervisor). (Logical device addresses are not permanently assigned to specific tracks or data sets in a module.) When the SET SECTOR command is issued, its specified sector number is stored in the register in the control unit that is assigned to the logical device address being used for the channel program. Then the control unit disconnects from the channel.

At this point, another channel program with a SET SECTOR command can be accepted by the channel and control unit (assuming neither is busy). This channel program will be initiated using another available logical device address and its assigned control unit register. This process can be repeated for up to eight SET SECTOR commands, so that eight channel programs can be executing concurrently per 2305 module.

Whenever the control unit is not executing a command or is not otherwise busy, it monitors the rotational position counter in the 2305 module that is being incremented each sector time period. When the sector number in the counter of a module compares equal with the sector number stored in one of the registers in the control unit and the channel is free, the control unit reconnects and resumes execution of the suspended channel program associated with the logical device address assigned to the control unit register that compared equal (see Figure 20.15.2).

It should be noted that one 2305 module requires eight logical device addresses, each of which requires one subchannel on a block multiplexer channel. Since a 2835 control unit can have two modules, one 2305 facility can use 16 device addresses and 16 nonshared subchannels of a block multiplexer channel.

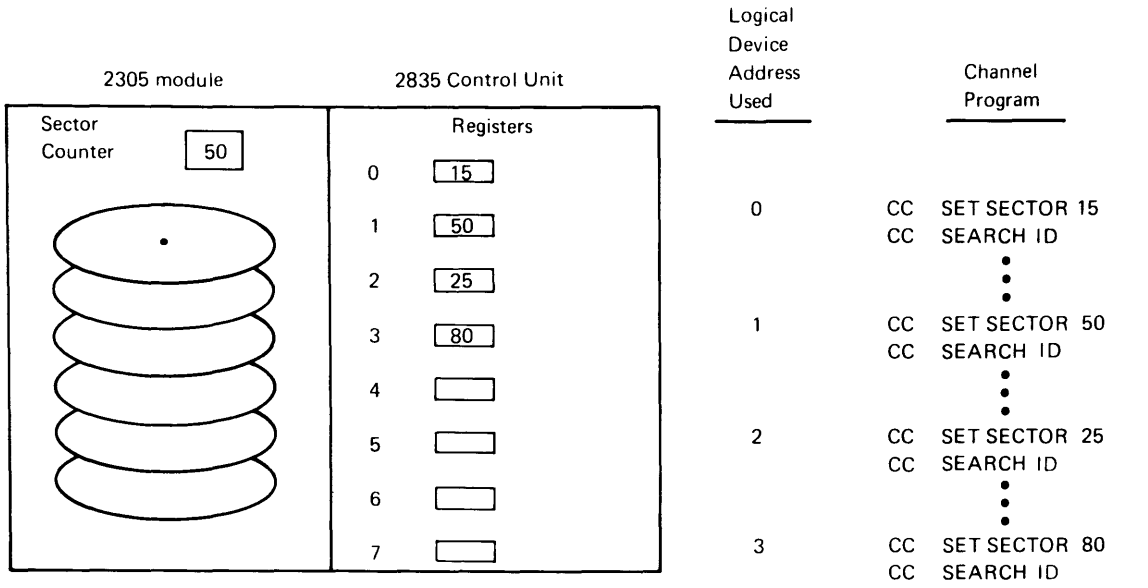


Figure 20.15.2. Multiple requesting on the 2305 facility

Table 20.15.1. 2305 Model 2 facility and 2303 Drum Storage characteristics

Characteristic	2305 Model 2	2303 Drum Storage
Device type	Six rotating disks with twelve recording surfaces	Rotating drum
Module capacity in bytes (full track records, no key)	11,258,880	3,913,000
Number of recording tracks	768	800
Number of bytes per track (R0, R1 written without key)	14,660 Home address is never written on a track	4,892 Home address is always written on each track
Number of read/write heads (recording elements) per module	864 One positioned to access each of 768 recording and 96 spare tracks	880 One positioned to access each of 800 recording and 80 alternate tracks
Rotation time (ms)	10	17.5
Access time (ms) Maximum Average	 10.25 5.0	 17.5 8.6
Time channel busy searching when SET SECTOR is used (ms)	.114 minimum .198 maximum	---
Rotation speed (rpm)	6000	3400
Data transfer rate in MB	1.5	.303
Data validity checking	10 correction code bytes (CCB) appended to each area written	Two-byte cyclic check (CC) code appended to each area written
Error recovery performed by the control unit	1. Command retry to retry a failing command without an I/O interrupt 2. Correction of data errors that occur in the data area of a record possible by programming using information in sense bytes	Not provided
Rotational position sensing	Standard feature (180 sectors per track)	Not available

Table 20.15.1 2305 Model 2 facility and 2303 Drum Storage characteristics (continued)

Characteristic	2305 Model 2	2303 Drum Storage
Multiple requesting (allows concurrent I/O operations on one module)	Up to 8 concurrent operations per 2305 module (up to 7 per module supported by data management)	One I/O operation at a time is supported.
Record overflow	Standard feature	Special feature
Two-Channel Switch	Special feature	Special feature
Device contained in the control unit	Yes to read the control unit microprogram and diagnostic programs	No

Table 20.15.2. Effective capacity of the 2305 Model 2 and the 2303 for various block sizes (DL column) with a 25-byte key

KL = 25 DL in Bytes	Effective Capacity in Bytes 2305 Model 2	2303
100	2,688,000	1,200,000
200	4,300,800	1,760,000
300	5,529,600	1,920,000
400	6,144,000	2,240,000
500	6,912,000	2,400,000
600	7,372,800	2,400,000
700	7,526,400	2,240,000
800	7,987,200	2,560,000
900	8,294,400	2,160,000
1000	8,448,000	2,400,000
2000	9,216,000	1,600,000
3000	9,216,000	2,400,000
4000	9,216,000	3,200,000

Table 20.15.3. Effective capacity of the 2305 Model 2 and the 2303 for various block sizes (DL column) when records are written without key

KL = 0 DL in Bytes	Effective Capacity in Bytes 2305 Model 2	2303
100	3,763,200	1,600,000
200	5,683,200	2,080,000
300	6,681,600	2,400,000
400	7,372,800	2,560,000
500	8,064,000	2,400,000
600	8,294,400	2,400,000
700	8,601,600	2,800,000
800	8,601,600	2,560,000
900	8,895,600	2,880,000
1000	9,216,000	2,400,000
2000	9,216,000	1,600,000
3000	9,216,000	2,400,000
4000	9,216,000	3,200,000

20:20 THE 3211 PRINTER

The 3211 is a high-speed line printer with front printing and new features designed to reduce operator intervention. The 3211 can print 2000 alphameric lines per minute (with a 48-character set) and is designed for industries and applications, such as utilities, aerospace, finance, communications, and fabrication and assembly, that require high print speeds.

The 3211 has a standard 132-print-position line, which can be expanded to 150 positions as an option. The number of print positions does not affect printing speed. The Universal Character Set (UCS) feature is standard and the interchangeable train cartridge contains 432 graphics. The cartridge character arrangement is unrestricted and can be alphabetic, numeric, or special characters in any combination. When the character arrangement is optimized for specific printing loads, speeds of up to 2500 lines per minute can be attained.

The 3211 attaches to a 3811 control unit. Unlike some models of the 2821 control unit which can handle multiple devices, a 3811 controls only one 3211 Printer.

New features of the 3211 include a powered forms stacker, an automatic platen, and a tapeless carriage. The powered stacker mechanism is self-adjusting and automatically rises in increments as the stack of paper mounts. This insures that the stacker mechanism is always the same distance above the top of the stack of forms. The rate of rise during each increment is determined by the setting of the stacker rate knob, which can be adjusted by the operator to produce the best condition for the thickness of the forms being stacked. The stacker also can be raised or lowered manually.

When forms are inserted, the printer platen automatically positions itself close to the train cartridge in accordance with the thickness of the forms. Thus, correct clearance between the platen and the cartridge is achieved without operator intervention. Because of its automatic forms thickness sensing, the 3211 is sensitive to forms with a different degree of thickness at each edge. (For forms limitations, see the Form-Design Considerations-System Printers Manual GA24-3488.)

Forms control paper carriage tape loading and unloading by the operator is eliminated by implementation of a tapeless carriage feature for the 3211. Forms spacing and skipping are controlled by a program-loaded forms control buffer (FCB) contained in the 3811 control unit.

The FCB contains 180 storage positions, each of which corresponds to a print line, that is, a single space of the carriage. Thus, forms up to 22.5 inches in length can be accommodated at eight lines per inch spacing (or 24 inches at six lines per inch). Up to twelve channel codes (1-12), corresponding to the twelve channel positions of the paper carriage tape used on a 1403 Printer, can be stored in the appropriate buffer line positions to control carriage skipping. The FCB can be considered to contain a storage image of a carriage control tape.

A carriage control address register is used to address the FCB and maintain correct line position with respect to the form. This register is incremented as space and skip commands, which cause the form to advance, are issued. When a SKIP TO CHANNEL command is executed, the carriage control address register is incremented and the form moves until the channel specified is sensed in a line position in buffer storage. If the requested channel number is not found in the buffer, forms movement stops after address position 1 (line 1) has been sensed twice. This prevents runaway forms skipping.

A flag in a buffer storage line position is used to indicate the last line of the form for forms shorter than 180 lines. A flag bit is also used in the first buffer storage position to indicate six or eight lines per inch spacing. The FCB is loaded with the desired forms spacing characters via a LOAD FCB command issued by a program. An error indication is given if an end-of-page flag is not present or if an invalid carriage code is loaded.

Serviceability features, in addition to those provided for the 1403 Printer, are incorporated into the design of the 3211. The fact that a 3811 control unit controls only one 3211 Printer instead of multiple devices permits offline repair of the malfunctioning printer or control unit only, without the necessity of removing other operational units from the system.

The 3811 control unit presents six bytes of sense information to identify printer and control unit malfunctions instead of only one byte, as is provided for the 1403. Certain errors (such as a parity check in the print line buffer) that might be corrected by programmed retry of the print operation are identified in the sense bytes, and carriage motion is suppressed. This permits error recovery without operator intervention if the retry is successful. The additional status data presented can be stored for later analysis and should speed the diagnosis of hardware malfunctions.

20:25 THE 3803/3420 MAGNETIC TAPE SUBSYSTEM

The new 3803/3420 Magnetic Tape Subsystem consists of 3803 Tape Control and a family of three 3420 Magnetic Tape Units which read and write nine-track, 1600-BPI, phase-encoded, half-inch magnetic tape. The three tape units, Models 3, 5, and 7, have a data rate of 120 KB, 200 KB, and 320 KB, respectively, and up to eight tape units, in any mixture of models, can be attached to a 3803 control unit. This tape subsystem, which embodies a completely new control unit technology, offers price performance improvements, compatibility with existing seven- and nine-track tape volumes and programs, enhanced reliability, availability, and serviceability features, lower cost tape switching capabilities, and standard automated tape-handling features presently available only on 2420 Magnetic Tape Units. (Table 20.25.2 at the end of this subsection compares 3420, 2420, and 2401 tape unit characteristics.)

The 3803/3420 subsystem can be attached to all System/370 models and to System/360 Models 30 to 195 (Model 67 in 65 mode only) except Model 44 for which there is no program support. The tape commands, status responses, and basic sense data of this tape subsystem are compatible with those of 2400-series tape units. Thus, any correctly written, non-time-dependent System/360 program for 2400-series tape units will operate without change on the Model 155 (subject to restrictions stated in Section 10:05) to handle operations on 3803/3420 subsystems with equivalent features installed. That is, existing nine-track 1600-BPI phase-encoded (PE), nine-track 800-BPI non-return-to-zero (NRZI), and seven-track 556/800-BPI NRZI-encoded tapes can be processed on 3420 tape units using existing programs without change to the tape volumes or programs.

The 3803/3420 tape subsystem offers 2400-series tape users the advantages of the latest significant advances in tape speed and design while maintaining media compatibility with existing tape volumes and providing enhanced RAS features. Specifically, the following are provided:

- Data rates of 120 KB, 200 KB, and 320 KB at 1600-BPI density

- Phase-encoded data recording that automatically detects and corrects single-bit read errors in-flight
- A tape transport design that minimizes tape wear and increases reliability, a single-drive capstan to control tape movement that provides faster data access times and rewinds, and more precise control of motor speed to help minimize damage to tape media
- Cartridge loading of tape, automatic tape threading, and a new automatic tape reel hub latch, all to reduce tape setup time
- Dual Density and Seven-Track (mutually exclusive) features to enable a 3420 tape unit to handle either nine-track 800-BPI NRZI and 1600 BPI PE tape or seven-track 556/800-BPI NRZI (BCD or binary) tape
- Flexible, lower cost tape switching implemented in a new compact physical design - a two-channel switch is available also
- Features such as new technology to improve subsystem reliability and new diagnostic facilities to aid serviceability and thereby increase subsystem availability

Phase-encoded recording. The phase-encoded (PE) recording technique offers superior error detection and reliability as compared with the non-return-to-zero (NRZI) technique. In both cases, magnetic recording of one and zero bits is accomplished by means of flux reversals or changes in polarity. In NRZI recording, only one bits are recorded as magnetized spots, and a flux reversal occurs only for one bits. In PE recording both zero and one bits are recorded (the zero bit and one bit being opposite in polarity), and a flux reversal is required in every bit position. Thus, the PE dual flux recording technique differentiates between no recording and the presence of a zero bit, and the absence of any signal is detected as an error.

The positive recording of all zero and one bits in PE eliminates the need for horizontal parity bits (longitudinal redundancy check used in NRZI recording), and vertical parity bits are used to correct single-bit read errors in-flight. During reading, if a single track fails to respond with a suitable pulse in any bit position, reading of the rest of that track is immediately disabled for the remainder of the data block, and the remaining bits for that track are automatically generated by use of the vertical parity bits. In-flight single-track error correction eliminates the time normally lost in backspacing and rereading NRZI tape for correction of single-track dropouts or defects.

Phase encoding offers other advantages. If a string of zeros is recorded on tape, successful reading in NRZI requires close synchronization to "count" the correct number of zeros. With PE, this synchronization is provided by the flux reversal in every bit position; hence, PE recording (and reading) is self-clocking. In addition, each block written on a PE tape is preceded and followed by a coded burst of bits in all tracks to set up the individual track-clocking rates. The read circuitry is designed to recognize these bursts and thereby minimize the effect of noise in the gap.

The critical nature of vertical skew (alignment of bits within a byte) that is imposed by NRZI recording is minimized by this individual track clocking scheme (one clock per track versus one clock for the entire tape subsystem), and by the use of one-byte (nine-bit) capacity skew buffers that can be in the process of collecting up to four data bytes at the same time, as the tape passes the read head. Because of the positive recording of all bits, once a skew buffer contains

nine bits, one from each horizontal data track, it is an indication that a byte has been read. Thus, the 3420 can handle the situation in which the tape is not exactly aligned, and bits from up to four adjacent bytes can be read concurrently.

Like 2400-series tape units, the 3420 utilizes a two-gap read/write head that performs readback checking during write operations. The 3420 also has a separate erase head that erases the entire width of the tape during any write operation before writing occurs. Full-width erasure reduces the likelihood of leaving extraneous bits in interblock gaps or skip areas and minimizes the interchangeability problems that can occur when tape is written on one tape unit and read on another.

Advanced engineering design. The tape path in the 3420 tape unit is designed for "soft handling" of tape volumes to minimize tape wear and thus improve tape reliability. Other features, such as the single-drive capstan and optical tachometers, result in faster data access and rewind times than those of the 2401 and the 2420, for models with comparable data transfer rates.

On a 3420 tape unit, the tape reel is mounted on the right side of the tape transport as on a 2420, instead of on the left as on a 2401 tape unit, so that an inverted tape path exists. As a result, when the tape is loaded in the columns, the recording side touches only the tape cleaner and read/write head. Friction and tape wear are also reduced by the presence of air bearings in the tape transport that provide a thin film of air between the nonrecording surface and each metal bearing.

Use of a single-drive capstan transport for tape movement and optical tachometers for control of motor speed result in several advantages. First, faster access times than those of 2400-series tape unit models are achieved. Access time is defined as the time interval from initiation of a write or forward read command (given when the tape is not at load point) until the first data byte is read or written, assuming the tape is brought up to speed from stopped status. Nominal access times for 3420 Models 3, 5, and 7 are 4.0 ms, 2.9 ms, and 2.0 ms, respectively.

Second, the single-drive capstan can be made to operate faster than normal read/write speed, and in-column rewind is thus implemented. Full reel rewind speeds average 410, 480, and 640 inches per second for Models 3, 5, and 7, respectively. (The 2420 rewinds at about 500 inches per second execpt for the last 100 feet, which are rewound at the model's rated read speed.) In addition, less time is required to rewind less than a full reel on a 3420 as compared to a 2401 because of faster rewind times achieved by in-column rewinding.

Last, three optical tachometers that monitor motor speed are used to achieve precise control of the speed of both the capstan motor and the tape reel motors. The capstan tachometer measures the size of the interblock gaps (IBG's) created during tape writing. The result is a more consistent IBG size (.6 inches) than is created by 2400-series tape units, which enables more accurate calculation of tape passing time. IBG passing times are 8.0 ms, 4.8 ms, and 3.0 ms for 3420 Models 3, 5, and 7 respectively. These times would be used in calculations for command chained tape operations (reading or writing more than one tape block with a single START I/O instruction). More precise capstan motor speed also results in smoother starts and stops, thereby minimizing tape stretching and breaking.

The two tape reel tachometers measure tape speed as the tape enters and leaves the vacuum columns, and tape speed is adjusted when necessary. The 3420 tape unit is, therefore, less sensitive to voltage changes. More precise control of tape reel motor speed improves rewind

speed and minimizes erratic tape stacking during rewinds so that there is less chance of damaging tape edges.

Automatic threading and cartridge loading. These advanced features are standard on all 3420 models and significantly reduce tape mounting and demounting time. Tape threading is automatic for tape reels not enclosed in a wraparound cartridge once the reel (10.5-inch, 8.5-inch, or minireel) is mounted on the tape unit with the tape end placed in the threading chute and the load-rewind button is depressed. The power window is closed, the tape is threaded on the takeup reel, and the tape is loaded in the columns and positioned at load point within ten seconds after the button is depressed for Models 3 and 5. On the Model 7, only seven seconds are required. In addition, unload and rewind/unload operations cause the tape to be completely rewound on the tape reel and the power window to be lowered so that the reel is ready for immediate demounting.

If the tape is enclosed in a wraparound cartridge (10.5-inch reels only), an operator need only mount the cartridge and does not have to place the tape end on the threader chute. Once the load-rewind button is depressed, ten seconds are required to open the cartridge and perform automatic threading. If automatic threading fails on the first try, the 3420 unit automatically rewinds the tape and retries threading. Unload operations rewind and close the cartridge automatically. In addition to fast tape reel mounting, the use of a wraparound cartridge offers other advantages. Handling of the tape reel itself is not required when the tape is used, because the wraparound cartridge is also the shelf storage container. The only time the cartridge need be opened is when it is opened by the 3420 during use. This enhances the reliability of the tape media.

The 3420 tape unit also has a new automatic reel latch instead of the snap type hub latch implemented on newer 2400-series tape units. The operator places the tape reel on the hub and the automatic latch mechanically aligns the reel and then pneumatically locks it in position.

The advantage of these features can be shown by comparing setup times for tape units with and without the autothread feature. A tape study using experienced operators indicated the total time required to remove a tape reel, mount a new reel, thread the tape, and come to ready status was the following:

2401 tape unit - 40 seconds
Autothread tape unit without cartridge - 29 seconds
Autothread tape unit with cartridge - 13 seconds

Single Density, Dual Density, and Seven-Track features. These three features are provided for both 3803 control units and 3420 tape units. They are mutually exclusive features. Dual Density can be field installed on a 3803; however, the Seven-Track feature is not recommended for field installation. The Dual Density or the Seven-Track NRZI feature can be field installed on a 3420 tape unit only if it is replacing another NRZI feature. (For example, Dual Density can be field installed to replace the Seven-Track but not the Single Density feature.) The Dual Density and Seven-Track features facilitate efficient conversion of existing NRZI-recorded tapes to 1600-BPI phase-encoded format and permit tape volume interchange with other systems that use seven-track 556/800-BPI or nine-track 800-BPI tape. (See Section 60 for a discussion of conversion to 3420 tape units.)

A 3803 control unit with the Single Density feature (without a switching feature) can handle up to eight 3420 tape units (Models 3, 5, and 7) with the companion Single Density feature installed. Only 1600-BPI PE tape can be read and written. When the Dual Density feature is present on the 3803 control unit, both nine-track 1600-BPI PE and

nine-track 800-BPI NRZI tape operations can be performed on 3420 units (Models 3, 5, and 7) with the companion Dual Density feature installed. (Tape units with the Single Density feature still handle only nine-track 1600-BPI PE tape.) When the Seven-Track feature is present on the 3803 control unit, seven-track 556/800-BPI NRZI operations (both BCD and binary format) can be performed on 3420 tape units (Models 3, 5, and 7) with the companion Seven-Track feature installed. The data convert and translate facilities are a standard part of the Seven-Track feature. Table 20.25.1 summarizes 3803 control unit capabilities without and with these features.

Tape mode setting is handled as follows. For write operations on nine-track tape units with the Dual Density feature, a mode set command must be issued to establish 1600-BPI PE or 800-BPI NRZI recording mode prior to the first write. Tapes written in PE mode have a format identification burst recorded at load point that differentiates them from NRZI mode tapes. During reading, sensing of this burst automatically puts the tape unit in PE mode. Failure to sense the burst establishes NRZI mode if both the tape unit and control unit have the Dual Density feature. If an attempt is made to read NRZI-mode tape on a unit without the Dual Density feature, an error indication results. Once PE or NRZI mode is established for read operations, it is retained until the tape returns to load point.

For seven-track read and write operations, NRZI mode, density, parity, and use of the data converter or translator are established by issuing a single MODE SET command.

Table 20.25.1. 3803 control unit configurations and capabilities with Single Density, Dual Density, and Seven-Track features

3803 with Single Density Feature	3803 with Dual Density Feature	3803 with Seven-Track Feature (includes data convert and translate)
1. Nine-track, 1600-BPI, PE tape on 3420 Models 3, 5, and 7 with Single Density feature	1. Nine-Track, 1600-BPI, PE tape on 3420 Models 3, 5, and 7 with Single Density feature	1. Nine-Track, 1600-BPI, PE tape on 3420 Models 3, 5, and 7 with Single Density feature
	2. Nine-track, 800-BPI NRZI tapes and nine-track, 1600-BPI PE tapes on 3420 Models 3, 5, 7 with the Dual Density feature.	2. Seven-track, 556/800-BPI, NRZI BCD and binary tapes on 3420 Models 3, 5, and 7 with the Seven-Track feature.
Note: The Single Density, Dual Density, and Seven-Track features are mutually exclusive on the same control unit or the same tape unit.		

Tape-switching features. Tape subsystem configuration flexibility is provided by field installable tape-switching options that permit up to four control units to be switched among up to 16 tape units. While this capability is provided for 2400-series tape units via the 2816 Switching Unit, tape switching for the 3803/3420 subsystem offers the advantages of compact design, reduced cost, and enhanced subsystem availability.

The switching features are built into the 3803 control unit itself so that space for stand-alone switching units is not required. The

fact that tape switching features are contained in the 3803 control units being switched (rather than in one unit) also enhances tape subsystem availability. When a switch failure occurs in one control unit, that unit can be switched offline, eliminating the necessity of removing the entire tape switching subsystem from the operative system configuration.

Using combinations of the Communicator and the Two-Control Switch, the Three-Control Switch, or the Four-Control Switch optional features, two, three, or four control units can be configured to be switched among up to 8 or up to 16 tape units. The Communicator must be present in all control units that are to be switched. It allows the control unit in which it is installed to address tape units that are attached to an interconnected control unit. Figure 20.25.1 shows the switching

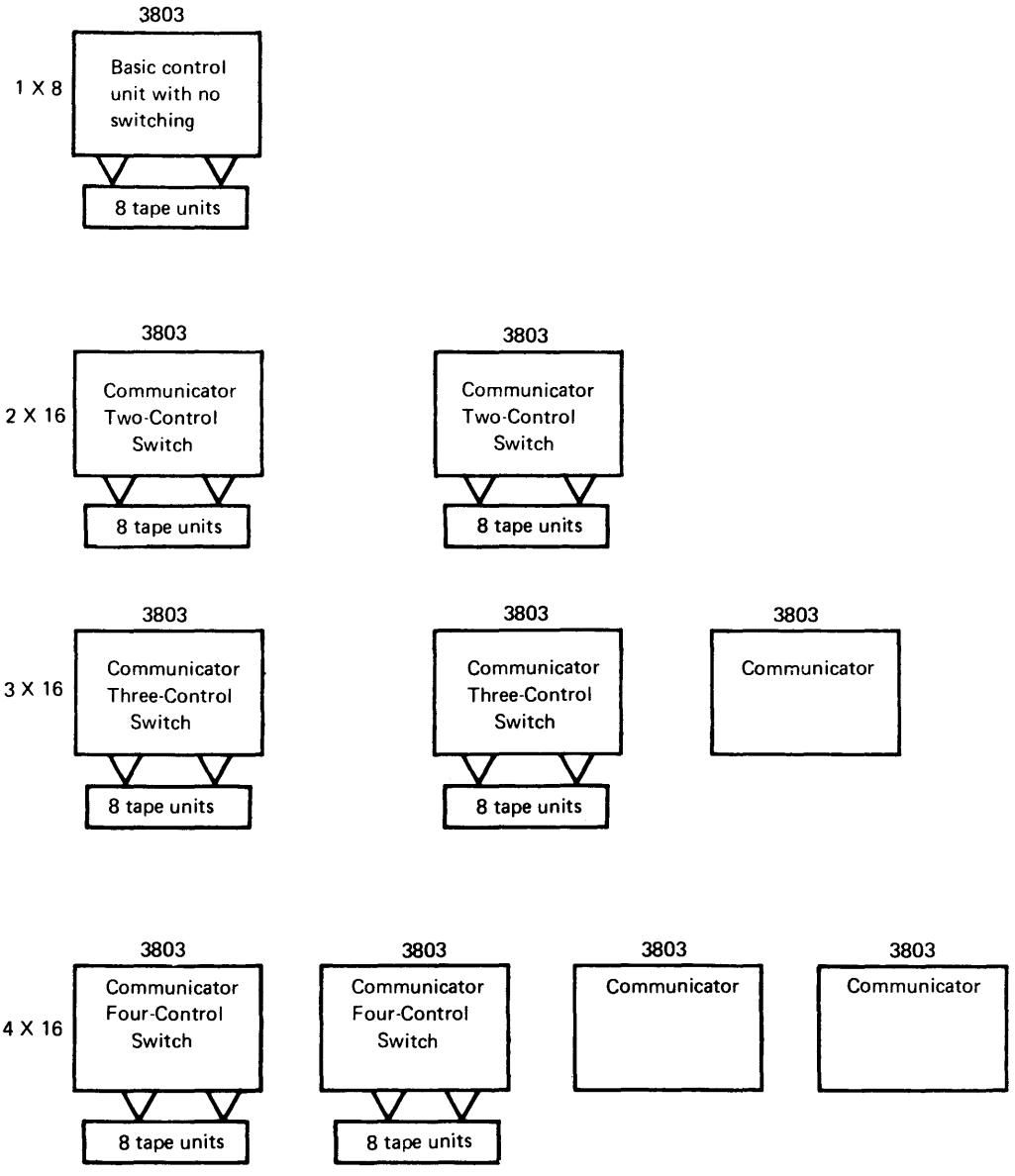


Figure 20.25.1. Tape-switching configurations for the 3803/3420 Magnetic Tape Subsystem

feature requirements for permissible switching combinations,. The switch combinations shown for switching control units among up to 16 tape units are the same that are required for switching control units among up to 8 tape units.

A two control unit switching configuration is required to replace the 2804 and 2404 read-while-write control units. The advantage of the tape switching approach is that for a small price increment better performance is possible. This is true because any two tape operations can be active concurrently in a switched configuration (including two reads or two writes) while the degree of simultaneity achieved using a read-while-write control unit is application dependent. That is, the application must lend itself to reading, then writing (or vice versa).

Two-Channel Switch. This optional feature provides switching functions for tape units similar to those provided by the two-channel switch for direct access devices. A 3803 control unit with the two-channel switch installed can be attached to two channels that are in the same system or in two different systems. Tape units attached to the 3803 can then be accessed via either channel. This feature can be present on a 3803 that also has tape switching features installed.

A 3803 with this switch can be set to allow access to all its tapes by either channel, one channel at a time. If channel A requests an operation when the control unit is busy performing an operation on channel B, then channel A must wait until the control unit becomes available again. If both channels are on the same system, this arrangement essentially provides two channel paths to the tape units on the switched 3803.

A RESERVE CONTROL UNIT command is provided for use with this feature. It permits a channel, via programming, to maintain exclusive use of the control unit and its tapes until the RELEASE CONTROL UNIT command is issued. These two commands are of benefit when the control unit is shared between two systems.

Tape units on a 3803 with a two-channel switch can also be partitioned. Partitioning is the manual assignment of tape units (via switches) to one channel or the other so that access to each unit is limited to one of the two channels. This facility can be used for backup purposes to switch tapes from one system to another or from one channel to another in the same system.

The two-channel switch for the 3803/3420 subsystem offers configuration flexibility not generally available to 2400-series tape unit users. A two-channel switch currently is provided only for a 2803 Model 1 control unit and can be used only in Model 67 and Model 65 multiprocessing configurations.

Reliability, availability, and serviceability features. The 3803/3420 hardware subsystem has several RAS features, in addition to the reliability and availability features already discussed for the tape media itself.

The 3803 control unit embodies a totally new design. The newest monolithic logic technology is used in the 3803 control unit and, therefore, it offers greater reliability and more compact physical design in comparison to the 2803 control unit. (The 3803 is approximately half the size of a 2803 control unit.) In addition, both logic circuitry and mechanical components in the control and tape units are functionally packaged to enable more rapid fault location and faster replacement.

As a diagnostic aid, additional sense bytes are generated by the microprogram-controlled 3803 control unit. The 3803 uses ROS for microprogram residence. Twenty sense bytes are provided, instead of the six generated by the 2803, certain of which can be used in tracing control unit microprogram malfunctions. Some of the other additional sense bytes identify the control unit and tape unit by serial number, optional features, and engineering change (EC) level.

Two other very significant new serviceability features are microdiagnostics resident in the 3803 control unit and radial attachment of 3420 tape units to the 3803.

Resident microdiagnostics in the 3803 enhance test operations for the 3803/3420 subsystem by relieving the CPU of the execution of most time-dependent tests. Diagnostics in the 3803 are executed via use of a diagnostic command issued by a program.

The 3803 also contains diagnostics that are operative during normal tape processing operations. These diagnostics perform operations such as the monitoring of measurement functions of the tape units. If an irregularity is noted, the control unit generates sense bits to inform the executing program of the malfunction.

Tape subsystem availability is improved by radial attachment of 3420 tape units to the 3803 control unit. That is, each 3420 is cabled directly to the control unit so that any malfunctioning tape unit can be disconnected from the tape subsystem for servicing without disturbing the other tape units. When tape units are attached to the control unit in series (each tape unit cabled to the next tape unit), as are 2400-series units, the entire tape subsystem must be taken offline to uncable a tape unit.

These new features, combined with the use of fewer adjustable parts, are designed to provide optimum tape subsystem availability through better reliability and reduced maintenance time.

In conclusion, the 3803/3420 Magnetic Tape Subsystem offers Model 40 and 50 tape unit users the following:

- Fast data rates, fast access times, and faster rewind for short files than on 2401 tape units. In-flight correction of single-bit read errors eliminates a backspace and reread procedure and reduces the number of permanent read errors.
- Automatic tape threading and cartridge loading to reduce tape setup time
- 1600-BPI density to reduce the tape volume requirements for multivolume data files recorded at lower densities.
- Less tape media wear as a result of the transport design and automatic threading and less tape damage caused by handling if wraparound cartridges are used for tape volume mounting and storage
- Reduced maintenance time because of the transport design (fewer adjustable parts), functional packaging of components, expanded sense bytes, and microdiagnostics resident in the control unit
- Increased tape subsystem availability because of reduced maintenance requirements
- Compatibility with existing 2400-series tape volumes and programs

These advantages, combined with lower subsystem cost and compact, flexible tape-switching capability, make the 3803/3420 Magnetic Tape Subsystem the natural growth path for tape users.

• Table 20.25.2. 3420, 2420, and 2401 Magnetic Tape Unit characteristics

Characteristic	3420 Tape Units			2420 Tape Units		2401 Tape Units			
	Model 3	Model 5	Model 7	Model 5	Model 7	Model 2	Model 3	Model 5	Model 6
Data rate (KB)	120	200	320	160	320	60	90	120	180
Density (bytes/inch)	1600	1600	1600	1600	1600	800	800	1600	1600
Tape speed (inches/sec.)	75	125	200	100	200	75	112.5	75	112.5
Norminal interblock gap size in inches (nine-track)	.6	.6	.6	.6	.6	.6	.6	.6	.6
Nominal read access to data (ms)	4.0	2.9	2.0	3.9	2.5	8	5.3	8	5.3
In-column rewind	Yes	Yes	Yes	Yes	Yes	No	No	No	No
Nominal rewind and unload time (secs.)	76	66	51	78	66	90	66	90	66
Nominal rewind to ready status--full 2400-foot reel (secs.)	70	60	45	72	60	84	60	84	60
Automatic threading	Standard	Standard	Standard	Standard	Standard	Not available	Not available	Not available	Not available
Time to ready status after load button pressed (secs.)	10	10	7	10	7	-	-	-	-
Cartridge Loading (10.5-inch reels only)	Standard	Standard	Standard	Standard	Standard	Not available	Not available	Not available	Not available
Automatic reel latch	Yes	Yes	Yes	No	No	No	No	No	No
Recording technique	PE	PE	PE	PE	PE	NRZI	NRZI	PE	PE

Page of GC20-1729-0
Added 11/20/70
By TNL GN20-2276

• Table 20.25.2. 3420, 2420, and 2401 Magnetic Tape Unit characteristics (continued)

Characteristic	3420 Tape Units			2420 Tape Units		2401 Tape Units			
	Model 3	Model 5	Model 7	Model 5	Model 7	Model 2	Model 3	Model 5	Model 6
Recording medium (1/2-inch magnetic tape)	IBM Series/ 500 Dynexcel, Heavy Duty, or equiv-alent 10.5",8.5", 6.5" reels (Use of Mylar* is not recommended.)	Same as Model 3	Same as Model 3	Same as 3420	Same as Model 5	Same as 3420 plus Mylar	Same as Model 2	Same as 3420	Same as 3420
Inverted tape path, single-capstan drive optical tach-ometers	Yes	Yes	Yes	Yes except for optical tachometers	Same as Model 5	No	No	No	No
Error checking									
Single-track corrections during reading	Automatic	Automatic	Automatic	Automatic	Automatic	Programmed	Programmed	Automatic	Automatic
Vertical redundancy check	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Longitudinal redundancy check	No	No	No	No	No	Yes	Yes	No	No
Number of sense bytes	20	20	20	6	6	6	6	6	6
Microdiagnostics in control unit	Yes	Yes	Yes	No	No	No	No	No	No
Separate erase head	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Seven-Track feature	Optional	Optional	Optional	Not available	Not available	Optional	Optional	Not available	Not available
Densities (BPI)	800 556 -	800 556 -	800 556 -	- - -	- - -	800 556 200	800 556 200	- - -	- - -
Data rate (KB) 800 BPI 556 BPI 200 BPI	60 41.7 -	100 69.5 -	160 111.2 -	- - -	- - -	6- 41.7 15	90 62.5 22.5	- - -	- - -

*Trademark of E. I. Dupont deNemours & Co. (Inc.)

• Table 20.25.2. 3420, 2420, and 2401 Magnetic Tape Unit characteristics (continued)

Characteristic	3420 Tape Units			2420 Tape Units		2401 Tape Units			
	Model 3	Model 5	Model 7	Model 5	Model 7	Model 2	Model 3	Model 5	Model 6
Recording technique	NRZI	NRZI	NRZI	-	-	NZRI	NZRI	_	_
IBG size (ins.)	.75	.75	.75	-	-	.75	.75	-	-
Translator	Standard	Standard	Standard	-	-	Optional	Optional		
Data Converter	Standard	Standard	Standard	-	-	Optional	Optional		
Dual Density feature (800/1600 BPI)	Optional	Optional	Optional	Not available	Not available	Not available	Not available	Optional	Optional
Data rate (KB) at 800 BPI	60	100	160	-	-	-	-	60	90
Recording technique at 800 BPI	NRZI	NRZI	NRZI	-	-	-	-	NRZI	NRZI
IBG size at 800 BPI (inches)	.6	.6	.6	-	-	-	-	.6	.6
Control Unit	3803 with optional Seven-Track or Dual Density feature (not both). Read while write (RWW) capability is not provided.	Same as Model 3	Same as Model 3	2803 Model 2. 2420 units can be mixed with 2401 Models 1 to 6 if required attach-ments are present on 2803	Same as Model 5	2803, 2804 (RWW) Model 1 with optional Seven-Track Com-patibility feature 2803, 2804 Model 2 with optional Seven-Track, Nine-Track, or Seven- and Nine-Track Compatibility feature	Same as Model 2	2803, 2804 (RWW) Model 2 with optional Seven-Track, Nine-Track, or Seven- and Nine-Track Com-patibility feature	Same as Model 5
Tape switching	2 x 16 3 x 16 4 x 16 (Switching features in 3803 control units)	Same as Model 3	Same as Model 3	2 x 16 3 x 16 4 x 16 (Requires one or two 2816 units)	Same as Model 5	Same as 2420	Same as 2420	Same as 2420	Same as 2420
Two-Channel Switch	Optional	Optional	Optional	Not available	Not available	Optional on 2803 Model 1 for Model 67 and MP65 systems only	Same as Model 2	Not available	Not available

Page of GC20-1729-0
Added 11/20/70
By TNL GN20-2276

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SECTION 30: PROGRAMMING SYSTEMS SUPPORT

30:05 TRENDS IN DATA PROCESSING AND PROGRAMMING SYSTEMS

The Model 155 and its programming systems support have been designed to operate in the data processing environment that has been emerging since the introduction of System/360.

Significant trends are the following:

- Growth toward more multiprogramming to improve system throughput. Multiprogramming also permits the user to install new applications, such as small teleprocessing inquiry or graphics applications, that otherwise would not justify a dedicated system. Multiprogramming support also has encouraged the growth of new computer environments, as indicated by the items that follow.

- Growth of integrated emulation, that is, concurrent native and emulation mode processing on one system. The execution of emulators under operating system control improves system throughput because emulators can use control program facilities (stacked job execution, data management functions, etc.) and because native mode and emulator jobs can be scheduled to operate concurrently to utilize available system resources more efficiently. The use of integrated emulators eliminates most reprogramming and eases transition from one system to another, permitting the user to expend his efforts extending and adding applications.

- Greater use of high-level languages, such as COBOL, FORTRAN, and PL/I, for applications programming. The cost of programming has been increasing, while the cost of computing hardware has been decreasing. More productive use of programmers can be achieved by the use of high-level languages. Improvements to compile times and to the size and execution speed of code produced by high-level language translators have been made and continue to be made. The support of many more functions within high-level languages has also increased their use, and the growth of interactive computing has stimulated the addition of even more facilities.

- Growth of teleprocessing applications such as remote inquiry, message switching, data collection, and management information systems. The ability of System/360 and System/370 to handle teleprocessing and batch processing in one system eliminates the necessity of dedicated, special purpose systems.

- Growth of remote computing activities, such as remote job entry and interactive computing (or time sharing), in both a nondedicated and a dedicated environment. Remote computing offers (1) fast turnaround for batch work submitted from remote locations, (2) remote user access to the large computing facilities and data base available at the central installation, and (3) interactive problem solving on a regular or a nonscheduled basis for personnel in locations remote from the central computer. In-house interactive computing is growing also as users attempt to use programmer time more efficiently.

- Growth towards large, online data base systems. The growth in the marketplace of remote computing, time-sharing, and real-time applications necessitates the instant availability of more and more data. High-capacity, fast, low-cost, reliable direct access devices supported by appropriate data organizations, access

techniques, and security measures will be required for this type of computing environment.

IBM programming systems support of these trends in data processing has been growing and continues to expand. The System/370 Model 155 offers hardware, I/O devices, and performance capability required by the expanding computing environment.

30:10 OS SUPPORT

It is expected that the majority of the users who upgrade to the Model 155 will use OS as their operating system. The design of OS and the facilities it provides currently make it a particularly suitable base upon which to build additional support of the data processing trends discussed. Some of the major OS features currently available or announced are the following:

- Priority and job class scheduling for better resource utilization
- Multiprogramming support of up to 15 user jobs and multitasking facilities
- Automatic data transcription performed by the control program (reader interpreters and output writers) concurrently with user job execution
- Dynamic resource allocation by the control program
- Multiple console support (MCS) and device-independent display operator console support (DIDOCS)
- Extensive teleprocessing and graphics support
- Remote job entry and conversational remote job entry
- Support of a wide range of interactive (time-sharing) environments

OS will be modified and extended in future releases so that it supports Model 155 hardware. Appropriate alteration of the resident portion of a control program (nucleus) generated for a Model 155 will accommodate the fixed storage area of lower storage in the Model 155. OS for the Model 155 includes currently announced OS facilities and contains additional support to handle new Model 155 hardware features and I/O devices. Emphasis also has been placed on extending error recovery, recording, diagnostic, and repair procedures.

OS support of Model 155 features will be provided as follows. Programming systems support of RAS features is discussed in Section 50.

New instructions. The Assembler F (Type I) and Assembler H (program product) language translators will include mnemonics for the general purpose and other new instructions for the Model 155 so that these instructions can be used in user-written Assembler Language programs. The currently available OS high-level language translators will not generate the six new general purpose instructions.

Extended precision floating point. Assemblers F and H will include support of the extended precision floating-point data format and instructions. In addition, extended precision will be supported by the FORTRAN H and PL/I Optimizing Compiler program products.

The implementation of extended precision support in FORTRAN H and PL/I is such that the language translator and the processing programs

generated to include extended precision operations can operate on a System/370 or a System/360 with or without extended precision hardware. The language translator contains extended precision instructions and generates them for processing programs that use extended precision data. A program check interrupt occurs if an extended precision instruction is executed and the feature is not present in the system. This interrupt causes the processing program to call in a subroutine to handle extended precision operations. Extended precision divide is always simulated as the extended precision feature does not include such an instruction.

Interval timer. The interval timer will be supported for the same functions as it is currently except for time of day values.

Time of day clock. This clock will be supported in MFT and MVT environments for time of day requests made by system and user tasks via the TIME macro. At IPL, the operator will have the option of validating the clock time and correcting an invalid value.

Byte boundary alignment. The programmer can byte-align binary and floating-point data in Assembler Language programs, in ANS COBOL programs (by omitting the SYNCHRONIZED clause), in PL/I programs (by specifying the UNALIGNED attribute), and in FORTRAN programs. However, OS still expects parameters passed to it to be properly aligned and the high-level language translators still align unaligned binary and floating-point data prior to its use.

1401/1440/1460, 1410/7010 Compatibility Feature. Two integrated emulator programs will be provided, one to emulate 1401, 1440, and 1460 programs and the other to emulate 1410 and 7010 programs. (Emulator programs are discussed in Section 40.)

OS/DOS Compatibility Feature. An OS DOS Emulator program will be provided to support emulation of a DOS system. Section 40 discusses this emulator.

New console devices. The 3210 Console and 3215 High-Speed Console are supported as the primary operating system console device. A remote 3210 Console is supported as an alternate or an additional console. (The MCS option is required to support the latter.)

Channels. One or two byte multiplexer channels will be supported for a total of up to 512 subchannels per system. Selector and block multiplexer mode are supported also. During IPL, channel mode for all installed high-speed channels is established via a control register channel mode bit setting based on system generation channel definitions. (The channel mode bit was discussed in Section 10:20.) The operator does not have the option of changing this mode at IPL, nor does the control program change the mode setting during system operation.

The 3330 facility. The 3330 facility will be supported as an I/O device for most of the same functions as is the 2314 facility and by ASP and HASP. The error recovery routine provided for the 3330 will include support of the new hardware error correction features.

RPS will be supported in MFT and MVT environments as follows.

- The stand-alone seek issued within the I/O supervisor (IOS) will be eliminated for RPS devices (3330 facilities). IOS will continue to issue stand-alone seeks for direct access devices without RPS. IOS also will be capable of recognizing the channel available interrupt.

- Access method support of RPS commands (SET SECTOR and READ SECTOR) will be provided by:

QSAM and BSAM for all record formats and functions supported for the 3330 facility except the undefined track overflow record format

ISAM for all updating and verification and QISAM sequential processing
BPAM for directory and member processing operations where possible

BDAM for direct retrieval and update of fixed-length standard and VBS format records without key and for write verification of all BDAM format records

- End-of-volume (EOV) routines will support concatenation of data sets residing on RPS and on non-RPS devices. The control program will ensure that an RPS access method is used for drives with the feature and that a non-RPS method is used for drives without the feature.

- Any system utility, data set utility, or IBM-supplied processing program (such as a language translator) that uses the sequential access methods will support RPS. In addition, IEHMOVE, IEBCOPY, and the initialize/dump/restore utility (IEHDASDR) will include RPS support for 3330 facilities.

- The Sort/Merge (program product) supports RPS for 3330 intermediate work devices.

- Where appropriate, RPS commands for access to SYSRES data sets will be supported by:

  Data set catalog routines
  Direct Access Device Space Management (DADSM) routines (for DSCB processing)
  STOW, BLDL, and FIND processing of program library (PDS) directory entries
  OPEN/CLOSE/EOV processing of JFCB's in the job queue

  Routines that access the job queue

  Note that RPS command support is not provided for:
  Access to TSO swap data sets
  Program fetch
  The telecommunications access method (TCAM) for message queues
  The stand-alone disk initialization and alternate track assignment routines (DASDI and IEHATLAS)

The 2305 facility. The 2305 facility will be supported as an I/O device for most of the same functions as is 2303 Drum Storage.

Rotational position sensing for 2305 facilities will be supported as discussed for the 3330 facility except that an arm positioning seek is not required on 2305 modules and the 2305 is not supported as an intermediate work unit by the Sort/Merge programs. In addition, the 2305 is not supported by ASP, HASP, or for TCAM message queues. Multiple requesting will be handled by the I/O supervisor, which will initiate up to seven channel programs on one 2305 module at a time. (The eighth logical device address is reserved for control purposes.) Multiple I/O operations to the same data set will be initiated if the data set is not being sequentially processed. (One operation must complete successfully before the next can be initiated during sequential processing.)

Note that specification of exchange buffering for a QSAM data set on the 3330 or 2305 facility results in a default to simple buffering.

3211 Printer with tapeless carriage. The 3211 Printer, with or without the 18 additional print positions, will be supported by QSAM and BSAM for exactly the same functions as is the 1403 Printer and by ASP and HASP. The control program will handle loading of the forms control buffer (FCB) with carriage control images. This support is similar to that provided for Universal Character Buffer (UCB) loading.

The user can define one or more default FCB images at system generation time. Two IBM-supplied default images are included automatically. All other FCB images to be used must be defined by the user and placed in SYS1.SVCLIB, as is the case with UCB images. User-supplied default images must be identified as defaults. The FCB image to be used by a processing program can be specified in the 3211 Printer DD statement included for the job step and will be loaded into the FCB by the control program.

The FCB image currently loaded can also be changed by the programmer during execution of the processing program by use of an Assembler Language macro. If the DD statement does not specify an FCB image and the image currently loaded is not one of the defaults specified at system generation, the operator is requested to specify the FCB image to be used.

The FCB image (and the UCS character image) to be loaded for a 3211 Printer used by an output writer can be indicated in the output writer procedure or in the START output writer command issued by the operator. FCB and UCB images can also be specified in the SYSOUT DD statement for a data set that is to be printed by the output writer, and they will be loaded into the 3811 control unit prior to the printing of the data set.

Any time the FCB parameter is used, as described above, the user can specify that operator verification of forms alignment is to be requested by the control program via a console message when the buffer is loaded. The operator must respond to this message.

The 3211 error recovery routine will retry a print operation after a parity check occurs in the UCB or print line buffer if QSAM is used and three I/O buffers are provided for the printer data set. When the operation is retried, the 3811 control unit insures that only the print positions that did not print correctly the first time are reprinted.

The 3803/3420 Magnetic Tape Subsystem. This tape subsystem will be supported as an I/O device for the same functions as 2400-series tape units. This includes support of tape switching, Seven-Track, and Dual Density features. (Note that 200-BPI density tapes are not supported because the Seven-Track feature includes only 556 and 800-BPI densities.) The two-channel switch is supported for alternate paths switching. The RESERVE and RELEASE commands are not supported.

30:15 DOS SUPPORT

DOS will be modified in future releases so that it supports certain Model 155 hardware features. Appropriate alteration of the DOS supervisor generated for a Model 155 will accommodate the fixed storage area of lower storage in the Model 155.

DOS support of Model 155 features will be provided as follows. Programming systems support of RAS features is discussed in Section 50.

New instructions. Assembler D (14K variant) will include mnemonics for all the new instructions so that they can be used in user-written Assembler Language programs. The DOS high-level language translators currently available will not generate the six new general purpose instructions.

Extended precision floating-point. Mnemonics for extended precision instructions and data formats will be added to Assembler D. The DOS high-level language translators currently available do not support extended precision.

Interval timer. The timer will be supported in the same manner as it is currently, for time of day and time intervals.

Time of day clock. This clock is not supported for time of day values.

Byte boundary alignment. The programmer has the ability to byte-align binary and floating-point data in Assembler Language programs, in ANS COBOL programs (by omitting the SYNCHRONIZED clause), and in PL/I programs (by specifying the UNALIGNED attribute). However, the high-level language translators still align unaligned binary and floating-point data prior to its use.

1401/1440/1460, 1410/7010 Compatibility Feature. Two integrated emulator programs will be provided, one to emulate 1401/1440/1460 programs and the other to emulate 1410/7010 programs. (See Section 40 for a complete discussion of these emulator programs.)

New consoles. The 3210 Console and the 3215 High-Speed Console Printer-Keyboards are supported as the DOS console device. A remote 3210 Console is not supported.

Channels. A single byte multiplexer channel with up to 256 subchannels and selector channel mode are supported. A second byte multiplexer channel and block multiplexer mode are not supported.

New direct access devices. The 3330 and 2305 facilities are not supported.

3211 Printer. This printer, with or without the 18 additional print positions, will be supported in the same manner as is the 1403 Printer, including support by DOS POWER. Forms Control Buffer and Universal Character Buffer loading for the 3211 will be handled in the same way. The user must execute an IBM-supplied buffer load utility program (SYSBUFLD) as a job step in order to load the FCB and/or the UCB. No provision has been made for loading the FCB or UCB during execution of a job step. User-defined UCB images must be loaded from the core image library. FCB images can be loaded from cards or the core image library.

If a command retry indication is present, the 3211 error recovery routine supports retry of an operation that failed. This option must be requested by the user in the DTF for the 3211 Printer.

The 3803/3420 Magnetic Tape Subsystem. This tape subsystem will be supported as an I/O device for the same functions as 2400-series tape units. This includes support of tape switching (two control units only), Seven-Track, and Dual Density features. (Note that 200-BPI density tapes are not supported because the Seven-Track feature includes only 556 and 800-BPI densities.) The two-channel switch is supported for alternate path switching. The RESERVE and RELEASE commands are not supported.

40:05 OS 1410/7010 AND 1401/1440/1460 EMULATOR PROGRAMS

FEATURES COMMON TO BOTH EMULATORS

One of the significant new features of the Model 155 for OS users is support of integrated 1400/7010-series emulation. A 1410/7010 Emulator program and a 1401/1440/1460 Emulator program that operate under OS control on the Model 155 are provided. Only stand-alone 1400/7010 emulation is available to Model 40 and 50 OS users.

The emulator programs require the presence of the IBM 1401/1440/1460, 1410/7010 Compatibility Feature. This is the same feature used by the two integrated DOS 1400/7010 Emulator programs for the Model 155. The single feature permits operation of both the 1401/1440/1460 emulator and the 1410/7010 emulator, which operate as processing programs in MFT and MVT environments and are alike in their functional design. Those features common to both are discussed first.

The 1400/7010 emulator programs supplied for the Model 155 are relocatable and thus can operate in one or more MFT partitions or MVT regions. Because both programs use the same compatibility feature, any number of emulator jobs of the same or different types (1401,1440,1460, 1410, and 7010) can execute concurrently with System/370 jobs in the same Model 155, subject to the availability of system resources. Emulator and System/370 jobs can be intermixed in the input stream, since emulator job scheduling, initiation, and resource allocation are handled by OS job management routines. I/O operations are handled by OS data management. Emulator jobs are executed by job priority as is any OS job.

Integrated emulation provides a number of advantages over stand-alone emulation that can increase system throughput. The ability to execute 1400/7010-series jobs under operating system control offers emulation users the benefits of multiprogramming and OS facilities. The advantages of Model 155 integrated emulation are:

- Significantly better resource utilization, since System/370 native mode and 1400/7010-series emulator jobs can be multiprogrammed. Stand-alone emulators normally use only a portion of the hardware resources available in the system.

- Standardized and simplified job accounting and job scheduling. The latter reduces the number of IPL's required because switching from operating system to stand-alone emulation mode of system operation is not required.

- The ability to extend or add applications such as graphics, teleprocessing, time-sharing, etc., because a dedicated emulation environment is no longer required and more system resources are available in a given time period.

- The ability to process certain 1400/7010-series tape and disk data sets, using both System/370 and emulated 1400/7010-series programs. Existing 1400/7010 tape files can be converted to a standard OS data format using the IBM-supplied Tape Preprocessor formatting program. Existing 1400/7010 disk files must be converted.

- More efficient use of direct access space, since both 1400/7010 and System/370 data sets can be placed on the same disk volume.

- Device independence for emulator-supported I/O devices used by emulated 1400/7010-series programs that handle data sets in OS VBS data format. OS access methods are used to handle I/O operations so that new functions and I/O device support added to the access method routines used by the emulator programs are automatically available to emulated 1400/7010-series jobs. Tape and unit record 1400/7010-series files can be emulated on System/370 direct access devices.

The two emulator programs provided for the Model 155 use simulation routines, compatibility feature microprogram instructions, the Model 155 instruction set, and OS supervisor and data management routines to emulate 1400/7010-series program operations. QSAM is used for unit record emulation, BSAM is used for tape emulation, and BDAM is used for disk emulation. Figure 40.05.1 shows the general layout of an emulator program partition or region and indicates the range of processor storage requirements for both emulator programs. Note that 1400/7010 storage is simulated in contiguous Model 155 storage (each 1400/7010 position is simulated by a byte).

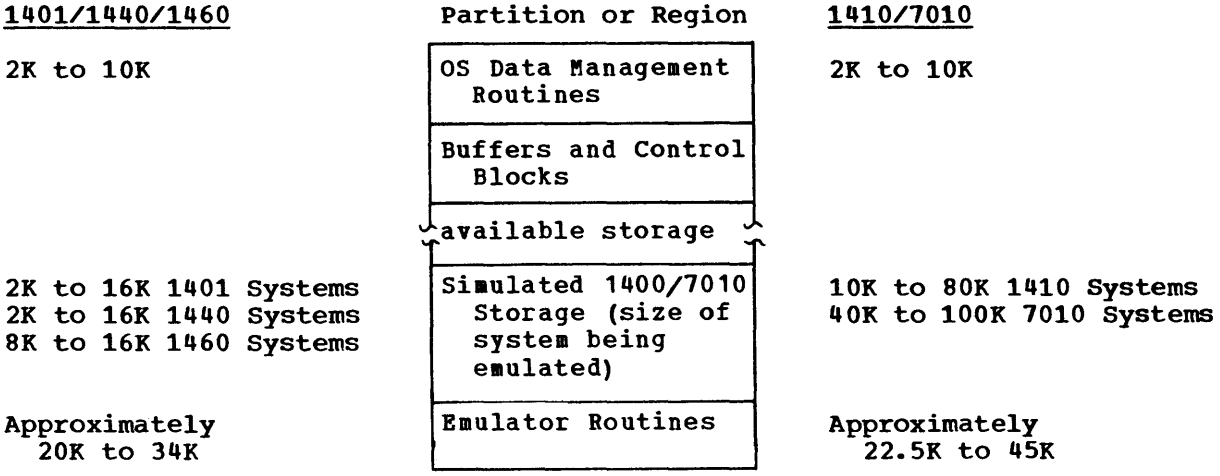


Figure 40.05.1. Partition or region layout for a 1400/7010-series emulator program job step, with general storage requirements indicated

The specific emulator program to be used by an installation must be constructed via an emulator generation procedure, which produces the job control statements required to assemble and link-edit the desired emulator modules and place the emulator program in SYS1.LINKLIB. Emulator program routines and data formatting programs (Tape Preprocessor, Tape Postprocessor, and Format Disk) are distributed on a restore tape independently from regular OS releases. All Model 155 1400/7010-series emulator users receive the same two tape formatting programs. One disk formatting program is supplied. It handles preformatting for 1401/1440/1460 files and 1410/7010 files. The following must be done to include one of the emulators in an OS operating system for the Model 155:

- Certain facts about the emulator program to be used with the operating system generated must be specified in the input required to generate the OS control program.

- The emulator restore tape must be obtained from PID and an emulator program with the desired facilities must be generated and placed in SYS1.LINKLIB. More than one version of a 1400/7010-series emulator program for the same and different systems can exist in an operating system.

The emulator program generated will emulate, without change, 1400/7010 programs that are written in accordance with IBM 1400/7010 Principles of Operation manuals and that are operating on 1400/7010 systems, subject to the following conditions:

1. Time-dependent programs may not execute properly. Provision has been made to allow some time-dependent programs to be emulated correctly. (See the appropriate emulator planning manual for details.)

2. Programs that depend on error conditions or on the absence of a particular feature may not be emulated correctly.

3. Programs with undetected programming errors will give unpredictable results.

4. Only the 64-character BCD set is accepted by the emulators.

5. Programs that use unsupported features or I/O devices (as described for each emulator in this subsection and in the emulator program reference manuals) must be modified to conform to the support provided by the specific emulator program unless a user routine is written to handle the feature.

The Model 155 1400/7010 integrated emulator programs support the same facilities as the stand-alone 1401/1440/1460 and 1410/7010 emulators for System/360 models except for a few special features not supported by the Model 155 emulators. Thus, any 1400/7010 program that is being executed by a stand-alone System/360 emulator and that does not use one of these special features can be emulated on the Model 155 without change.

Tape and Disk Formatting Programs and Data Formats

The Tape Preprocessor and Tape Postprocessor formatting programs supplied to Model 155 1400/7010 series emulator users operate as processing programs and can be executed with any OS control program generated with the emulator macro specified. The Tape Preprocessor operates in a program area of 4K bytes plus I/O buffer requirements and accepts as input seven- and nine-track tape in 1400/7010-series format with or without 1400/7010 labels. It accepts mixed density 1400/7010 files, that is, files with header labels written in a density different from that of the data. The emulator programs consider a change in density to be an error and expect the emulated program to handle this condition. Therefore, it may be desirable to preprocess mixed density 1400/7010-format files.

The preprocessor produces as output spanned variable-length (OS VBS) format data that can be written on seven- or nine-track tape or on direct access storage. Input records longer than 32,755 bytes are reblocked, since OS BSAM cannot handle a physical data block longer than 32K. VBS format tape can be unlabeled or have OS standard labels, in addition to any 1400/7010 labels. The preprocessor converts 1400/7010 labels and tapemarks into data records that are recognized by the emulator program. Thus, if VBS format tapes with 1400/7010 label data records are to be processed by System/370 programs, the tape must be rewritten to remove the label data records or the System/370 program must contain a routine to recognize these records.

The Tape Postprocessor operates in a program area of 5K bytes plus I/O buffer requirements and performs the reverse of the Tape Preprocessor. The postprocessor program is useful when a copy of a data set in OS VBS and another in 1400/7010 format are required or if mixed density 1400/7010-format files are required. (The 1400/7010-series emulator programs accept as input and produce as output both the formats handled by these two tape formatting programs.)

The tape formatting and emulator programs handle 200, 556, 800, and 1600 BPI density, mixed density, and even, odd, and mixed parity seven-track tapes. VBS or 1400/7010-format data written on nine-track tape is coded in EBCDIC. If VBS format tapes are processed on a seven-track tape drive, the tape control unit must have the Seven-Track Compatibility and Data Convert features installed. The alternate mode used by stand-alone System/360 1400/7010 emulators is accepted by the Model 155 emulator programs as well.

While existing tape files with blocks longer than 32K bytes must be preprocessed, conversion to VBS format offers the following advantages:

- The ability to emulate tape data sets on direct access devices for more flexibility in I/O device assignment
- The ability to increase emulator job performance by reblocking 1400/7010-series-format tape files with short blocks
- The ability to reduce processor storage buffer requirements by reblocking files with very large blocks
- The ability to process VBS format tape and move mode disk data sets with both OS and emulated 1400/7010-series programs if the OS programs can handle 1400/7010 label and tapemark records. (Load mode disk data sets are not accepted by OS programs.)

The disk formatting program supplied operates as a processing program, and an area of 2K bytes in addition to buffer requirements is needed for its execution. This program must be used to format System/370 disk volumes that are to contain 1400/7010 disk data. In order to convert 1400/7010 disk files that are being processed on a 1400/7010 system or by a stand-alone System/360 1400/7010 emulator to a format acceptable to the Model 155 emulator program, the following must be done:

1. The contents of the disk must be dumped to tape using a 1400/7010 disk-to-tape utility program. This must be done on a 1400/7010 system if the data was created and is being processed on a 1400/7010 system. A System/360 with a stand-alone 1400/7010 emulator must be used to convert 1400/7010-format data files that are being emulated on System/360 direct access devices.
2. One or more initialized System/370 disk volumes must be formatted by executing the IBM-supplied disk formatting program on a Model 155 under OS MFT or MVT control.
3. A 1400/7010 tape-to-disk utility program must be executed on a Model 155 under emulator program control to restore the 1400/7010 data on tape to the formatted System/370 disk volume(s).

The data records on one 1400/7010 disk track are formatted into one fixed-length record, which is generally placed on one System/370 disk track. If one System/370 track is not large enough to contain the fixed-length record created from one 1400/7010 track, the track overflow feature is required on the System/370 device or another

System/370 disk device type must be used. Depending on the disk devices involved, one System/370 disk track may be large enough to contain the data from more than one 1400/7010 disk track, and use of the track overflow feature is an option. If used, it may result in more efficient use of System/370 direct access space. However, I/O processing time is increased by use of the track overflow feature.

Job Submission and Operator Communication

OS job control and Model 155 1400/7010 emulator program control statements must be present for each emulated 1400/7010-series object program. Subject to the restrictions listed previously, existing 1400/7010 programs need not be modified.

The required emulator control statements for emulated 1400/7010 programs are provided in a card, tape, or disk sequential data set or in the input stream. The 1400/7010 object programs to be emulated can be placed in the input stream, on tape, or in a partitioned data set on disk. An emulator control statement describes their location.

Card input to 1400/7010 programs can be placed in the input stream to be read by the reader/interpreter and placed in a SYSIN data set. Alternately, it can be emulated via a tape or disk sequential data set. Data to be printed or punched can be placed in a sequential tape or disk data set or in a SYSOUT data set on disk for transcription by an output writer. Use of an OS reader interpreter and output writer to handle unit record operations should reduce the execution time required to emulate 1400/7010 programs.

The operator communicates with an emulator partition or region via emulator commands that can be entered using the operating system console. The commands provided allow simulation of 1400/7010 console operations and can also be used in debugging operations. The operator can display I/O assignments, sense switch settings, etc., in effect for an executing 1400/7010 program. In addition, the operator can alter and dump processor storage selectively within the emulator program partition or region.

If multiple console support (MCS) is included in the OS control program generated, emulator program messages can be routed to a specific console device so that emulation messages are isolated.

Installing an Emulator

The following outlines the general procedure required to make the transition from 1400/7010 system operation or stand-alone System/360 1400/7010 emulation to Model 155 emulation under OS.

1. Generate an OS operating system for the Model 155 and specify required parameters about the 1400/7010 emulator program to be used with this operating system. (Generating an operating system for the Model 155 is discussed in Section 60.)

2. Generate the desired 1400/7010 emulator.

3. Add required OS job control and emulator control statements to the existing 1400/7010 programs that are to be emulated on the Model 155. Subject to the conditions stated previously in this section, modification of 1400/7010 programs may or may not be required. Optionally, 1400/7010 programs can be placed in a library (PDS) by using the OS IEBGENER utility program.

4. Tapes in 1400/7010 mode with blocks shorter than 18 bytes or longer than 32K must be preprocessed.

5. Disk files must be transferred to Model 155 direct access devices by using the steps already outlined.

6. Optionally, routines to support features and I/O devices not handled by the emulator program can be written and placed in a library. The generated 1400/7010 emulator program will cause them to be loaded.

When installation of a 1400/7010 emulator is being planned, consideration should be given to the factors that affect the performance of emulated 1400/7010 jobs. Throughput of 1400/7010 jobs is affected by the mix of CPU and I/O operations executed by the compatibility feature and the amount of interference from higher priority partitions or regions. A large factor in performance is the way I/O operations are handled. The following steps can be taken to achieve greater emulator job throughput if enough processor storage is available.

1. Allocate one buffer to each access mechanism simulated instead of sharing buffers among multiple access mechanisms. (Do not use the shared buffer option for disk data sets unless processor storage is limited.)

2. Allocate two buffers to each tape data set instead of one.

3. Convert 1400-format tape files to VBS format for emulator processing.

4. Using the Tape Preprocessor, reblock tape files containing short blocks.

5. Do not use the track overflow feature for emulated disk data sets unless direct access space is at a premium.

OS 1410/7010 EMULATOR PROGRAM SUPPORT

The OS 1410/7010 Emulator program can operate on a 256K Model 155 with the 1400-series compatibility feature and enough I/O devices for the operating system and emulated 1410/7010 devices.

The partition or region size required depends on the features, I/O devices, and buffering used and on the size of the system being emulated. The emulator program size varies from a minimum of approximately 22.5K, for a basic system with unit record I/O device support only, to a maximum of approximately 45K for all special features and unit record, tape, and disk support. A large 7010 system - 100K, 14 tape units, each with a 1K buffer, 4 disk units using two 2K shared buffers, and unit record devices with 400 bytes of buffers - requires a 164K partition or region for emulation. This figure includes 7.5K of access method routines. (For details about processor storage requirements, see Emulating the IBM 1410 and 7010 on the IBM System/370 Model 155 Using OS/360 - GC27-6946.)

Table 40.05.1 lists the 1410/7010 system features supported and not supported by the Model 155 1410/7010 Emulator program. Table 40.05.2 lists 1410/7010 I/O devices and features emulated and their Model 155 I/O device counterparts, while Table 40.05.3 indicates unsupported 1410/7010 devices.

The number of Model 155 direct access devices required to emulate a 1410/7010 disk device is indicated in Table 40.05.4. Requirements with and without use of the track overflow feature are indicated. A pair of numbers is given in each column for a device. The top entry represents the number of drives required. The bottom entry indicates the number of unused cylinders in the last disk pack used, all others

being full (199 cylinders per 2311 and 2314, 403 per 3330). Note that 2311 drives without track overflow cannot be used to emulate 1302 and 2302 Disk Storage.

The Model 155 integrated OS 1410/7010 Emulator program supports the same facilities and I/O devices as the stand-alone 1410/7010 emulator for System/360 models except for the 51-Column Card and Selective Stacker special features on the 1402 Card Read Punch.

Table 40.05.1. 1410/7010 system features supported and unsupported by the Model 155 OS 1410/7010 Emulator program

1410 Features	7010 Features
Supported	Supported
All basic CPU functions	Standard 7010 instruction set with store and restore status
Core storage up to a maximum of 80,000 positions	Main storage up to a maximum of 100,000 positions
Inverted Print Edit	Floating Point Arithmetic
Priority Processing	Processing Overlap
Processing Overlap	Priority Feature
One or two channels	Inverted Print Edit
	One to four channels
Unsupported	Unsupported
The 1400 Diagnostic instruction Branch on Tape Indicate	1401/1410 Compatibility Mode
	Diagnostic instruction branch
	Program Relocation
	Storage Protection
	Interval Timer

Table 40.05.2. IBM 1410/7010 I/O devices and features emulated by the OS 1410/7010 Emulator program and their Model 155 equivalents

1410/7010 I/O Device	Model 155 I/O Device
• 1402 Card Read Punch. 1442 Card Reader. Features not emulated: Select Stacker Column Binary 51-Column Card Programmed reading from more than one reader or punching on more than one punch within a program is not supported.	• Any card reader, card read punch, magnetic tape unit, or direct access device supported by OS QSAM
• 1403 Printer. Programmed printing on more than one printer within a program is not supported.	• Any printer, magnetic tape unit, or direct access device supported by OS QSAM.*
• 729 Model II, IV, V, and VI Magnetic Tape Units. 7330 Magnetic Tape Unit. (Compressed tapes are not supported.)	• Any tape unit or direct access device supported by OS BSAM. VBS format is used for 1410/7010 tape files emulated on a direct access device. Seven-track tapes must be emulated on tape units with a seven-track head. The tape control unit must have the Seven-Track Compatibility and Data Convert features if EBCDIC is used.
• 1415 Console	• Any operator's console supported by OS.
• 1301 Disk Storage Model 1 or 2. 1302 Disk Storage Model 1 or 2. 2302 Disk Storage Model 1 or 2. All features emulated except Write Disk Check (treated as a no-op) and operations involving the CE tracks. Write verification can be requested in the OS job control statement for the emulated disk device.	• Any direct access storage device supported by OS BDAM. A maximum of 20 simulated arms per channel are supported. If two or more System/370 direct access devices are required to emulate one 1410/7010 disk device, all Model 155 disk devices used to emulate that device must be of the same type. The 2311 must have the Track Overflow feature to emulate 1302 or 2302 Disk Storage.
*A printer must have the UCS feature to emulate the Preferred Character Set and Numerical Print features correctly.	

Table 40.05.3. IBM 1410/7010 I/O devices not supported by the Model 155 OS 1410/7010 Emulator program

1311 Disk Storage Drive	1412, 1419 Magnetic Character Reader
1405 Disk Storage	7340 Hypertape Drive
1011 Paper Tape Reader	Teleprocessing devices
1012 Tape Punch	Optical Character Readers

Table 40.05.4. Model 155 direct access device requirements for emulation of 1410/7010 disk devices using OS with and without the track overflow (T.O.) feature. Number of packs required and number of remaining available cylinders on the last pack are shown by the first and second row of figures, respectively, for each entry.

1410/7010 Disk Device	Number of Model 155 Drives Required per 1410/7010 Device					
	2311 Disk Drives		2314 Disk Drives		3330 Disk Drives	
	Without T.O.	With T.O.	Without T.O.	With T.O.	Without T.O.	With T.O.
1301 Disk Storage Model 1	6	5	2	2	1	1
	194	170	148	190	271	283
1301 Disk Storage Model 2	11	9	3	3	1	1
	189	130	97	180	139	164
1302, 2302 Disk Storage Model 1	-	18	6	5	2	2
	-	180	194	150	279	321
1302, 2302 Disk Storage Model 2	-	35	11	9	3	3
	-	156	189	102	156	239

OS 1401/1440/1460 EMULATOR PROGRAM SUPPORT

The OS 1401/1440/1460 Emulator program can operate on a 256K Model 155 with the 1400 Compatibility Feature and enough I/O devices for the operating system and emulated 1400 devices.

The partition or region size required depends on the features, I/O devices, and buffering used and on the size of the system being emulated. The emulator program size varies from a minimum of approximately 20K, for a basic system, with unit record I/O device support only, to a maximum of approximately 34K for all special features and unit record, tape, and 1311/1301 disk support. A 16K 1401 system with unit record devices (400 bytes of buffers) and six tape units (1K buffer per tape unit) can be emulated in a 54K partition or region. This figure includes approximately 3.9K for access method routines. (For details about processor storage requirements see the Emulator Program to Emulate the IBM 1401, 1440, and 1460 on the IBM System/370 Model 155 Manual - GC27-6945.)

Note that a 1401/1440/1460 Emulator program can be generated to handle 1405 Disk Storage or 1311/1301 Disk Storage but not both.

Table 40.05.5 lists the 1401/1440/1460 system features supported and not supported by the Model 155 OS 1401/1440/1460 Emulator program. Table 40.05.6 lists 1401/1440/1460 I/O devices and features emulated and their Model 155 I/O device counterparts, while Table 40.05.7 indicates unsupported 1400 devices.

The number of Model 155 direct access devices required to emulate a 1400-series disk device is indicated in Table 40.05.8. Requirements with and without use of the track overflow feature are indicated. A pair of numbers is given in each column for a device. The top entry represents the number of drives required. The bottom entry indicates

the number of unused cylinders in the last disk pack used, all others being full (199 cylinders per 2311 and 2314, 403 per 3330).

The Model 155 integrated OS 1401/1440/1460 Emulator program supports the same facilities and I/O devices as the stand-alone 1401/1440/1460 emulator for System/360 models except for 51-Column Card, Punch Feed Read, and Selective Stacker on the 1402 Card Read Punch and Column Binary and Binary Transfer in the CPU.

Table 40.05.5. IBM 1401/1440/1460 system features supported by the Model 155 OS 1401/1440/1460 Emulator program

All basic CPU operations 1401 Models A-F, H 1440 Model A 1460 all models	Sense Switches Indexing and Store Address Register (1440,1460)
Core storage up to 16,000 positions	Advanced Programming Bit Test
Expanded Print Edit	Print Storage
Inverted Print Edit	Additional Print Control
High-Low-Equal Compare	Space Suppression
Multiply-Divide	Processing Overlap

Table 40.05.6. IBM 1401/1440/1460 I/O devices and features emulated by the OS 1401/1440/1460 Emulator program and their Model 155 counterparts

1401/1440/1460	Model 155 I/O Device
• 1402, 1442 Card Read Punch 1442 Card Reader. The following features are not emulated: Column Binary (1402) 51-Column Card (1402) Punch-Feed Read (1402) Read-Punch Release (1402) Card Image (1402) Punch-Column-Skip (1442) Read and punch same card (1442) Selective Stacker (1442) Programmed reading from more than one reader or punching on more than one punch within a program is not supported.	• Any card reader, card read punch, magnetic tape unit, or direct access device supported by OS OSAM
• 1443, 1403 Printer. The Selective Tape Listing feature and programmed printing on more than one printer are not supported.	• Any printer, magnetic tape unit, or direct access device supported by OS QSAM.*
• 729 Model II, IV, V, and VI Magnetic Tape Units. 7330, 7335 Magnetic Tape Units. (Compressed tapes are not supported.)	• Any tape unit or direct access device supported by OS BSAM. VBS format is used for 1400 tape files emulated on a direct access device. Seven-track tapes must be emulated on tape units with a seven-track head attached to a tape control unit with the Seven-Track Compatibility and Data Convert features.
• 1407 Console Inquiry Station. 1447 Console. The Branch on Buffer Busy feature (1447) is not supported.	• Any operator's console supported by OS.
• 1301 Disk Storage (only one access arm). 1311 Disk Storage Drive. 1405 Disk Storage Models 1 & 2. Up to five 1311 drives and one 1301 module or one 1405 Model 1 or 2 can be emulated. All features are supported except Write Disk Check (treated as a no-op). Write verification can be requested in the OS job control statement for the emulated disk device.	• Any direct access device supported by OS BDAM. If two or more System/370 direct access devices are required to emulate one 1400 disk device, all Model 155 disk devices used to emulate that device must of the same type.
*A printer must have the UCS feature to emulate the Preferred Character Set and Numerical Print features correctly.	

Table 40.05.7. 1401/1440/1460 I/O devices and features not supported by the Model 155 OS 1401/1440/1460 Emulator program

1400 I/O Device	1400 Feature
1404 Printer 1444 Card Punch 1445 Printer 1011 Paper Tape Reader 1012 Tape Punch Optical readers Magnetic character readers 7340 Hypertape Drive Teleprocessing devices	1401 Model G Binary Transfer

Table 40.05.8. Model 155 direct access device requirements for emulation of 1401/1440/1460 disk devices using OS with and without the track overflow (T.O.) feature. Number of packs required and number of remaining available cylinders on the last pack are shown by the first and second rows of figures, respectively, for each entry. Two figures shown in the number of System/370 drives column indicate that more than one 1400-series device can be emulated on a single Model 155 disk drive.

1401/1440/1460 Disk Device	Number of Model 155 Drives Required per 1400 Device					
	2311 Disk Drives		2314 Disk Drives		3330 Disk Drives	
	Without T.O.	With T.O.	Without T.O.	With T.O.	Without T.O.	With T.O.
1405 Disk (Model 1)	2 64	2 82	2:1 31	2:1 35	8:1 19	8:1 22
1405 Disk (Model 2)	4 131	4 160	1 31	1 35	4:1 2	4:1 22
1311 Disk (Sector mode)	1 99	3:1 6	11:1 12	11:1 12	38:1 3	43:1 4
1311 Disk (Track mode or both track and sector mode)	1 99	2:1 24	7:1 24	8:1 22	30:1 8	33:1 0
1301 Disk (Sector mode)	6 194	4 158	1 32	1 37	3:1 87	4:1 36
1301 Disk (Track mode or both track and sector mode)	6 194	4 48	2 148	1 10	3:1 7	3:1 77

40:10 DOS 1401/1440/1460 AND 1410/7010 EMULATOR PROGRAMS

FEATURES COMMON TO BOTH EMULATORS

The Model 155 continues the advantages of integrated emulation for DOS CS/30 and CS/40 users. In addition, these advantages are now extended to users of 1410/7010 stand-alone emulation.

DOS support for the Model 155 system includes two emulator programs:

- Emulator Program to Emulate the IBM 1401, 1440, and 1460 on the IBM System/370 Model 155
- Emulator Program to Emulate the IBM 1410 and 7010 on the IBM System/370 Model 155

Both emulator programs are common in design and run as problem programs under DOS on a Model 155 equipped with the IBM 1401/1440/1460, 1410/7010 Compatibility Feature. This compatibility feature is also used by the Model 155 OS 1401/1440/1460 and 1410/7010 emulators.

The emulators can be used in a batch-only system environment or can operate in the background and batched foreground partitions of a multiprogramming system. The compatibility feature is reenterable and common to both emulators. Therefore, more than one 1401/1440/1460 or 1410/7010 Emulator program can execute concurrently with each other and with System/370 programs. Additionally, emulated jobs and DOS jobs can be intermixed in a single job stream.

The Model 155 DOS integrated emulators consist of the compatibility feature, simulation routines, and DOS data management routines. They offer Model 155 users the following advantages:

- System resources are more fully utilized.
- Emulators can run concurrently in all three partitions of a multiprogramming system. They are relocatable and can be link-edited to run in any partition.
- 1401/1440/1460 and 1410/7010 Emulator programs and DOS programs can be executed concurrently and intermixed in a single job stream.
- DOS supervisor and data management services are available to the user. This provides for job control facilities, standard disk and tape label processing, and common data formats for emulator files and DOS files.
- 1400/7010 unit record input/output operations are device independent and can be emulated on Model 155 unit record devices, magnetic tape units, or direct access storage devices.

Emulator Program Generation and Execution

The Model 155 DOS emulators are distributed with DOS releases. An emulator is assembled using macro instructions. The macro instructions describe the 1400/7010 CPU, input/output devices, special features, data files, emulator buffers, and the desired user options. When assembled, the macros provide an object module and linkage to preassembled modules stored in the system relocatable library. The preassembled modules are combined with the emulator object module by the linkage editor for cataloging in the core image library. Any number of emulators can be assembled and cataloged in the core image library to run in any partition.

The emulator program generated will emulate, without change, 1400/7010 programs written in accordance with IBM 1400/7010 Principles of Operation manuals, subject to the following conditions:

- 1400/7010 programs that purposely depend on the absence of a 1400/7010 feature or on error conditions may not execute properly.

- Programs with undetected programming errors and those that depend on timing of 1400/7010 I/O operations yield unpredictable results.

An emulator program is handled by DOS in the same manner as is any problem program. When using the 1401/1440/1460 emulator, 1400 programs may be cataloged to, and fetched from, the core image library for execution or loaded from a card, tape, or direct access storage device. 1410/7010 programs can be loaded only from a card, tape, or direct access storage device. Standard DOS job control statements are used to prepare the system for an emulator job. The EXEC job control statement causes the specified emulator program to be loaded and control is passed to the emulator program. Emulator control statements are read by the emulator from the logical unit selected at generation time.

Emulation with the 1401/1440/1460 and 1410/7010 emulators consists of three main steps:

1. Initialization. Emulator control statements supplied by the user are read and interpreted. This information overrides, for the execution of the emulator, information specified at emulator generation.

2. Loading (or fetching - 1401/1440/1460). The 1400/7010 program is loaded from a card reader, magnetic tape, or direct access storage device. For the 1401/1440/1460 emulator, a 1400 program can be fetched from the core image library if it has been cataloged.

3. Execution (or precataloging - 1401/1440/1460). When loaded, the 1400/7010 program is executed. The 1400/7010 instructions are fetched, interpreted, and executed by the emulator until an end-of-job condition is recognized. For the 1401/1440/1460 emulator, the 1400 program can be either executed or converted into a DOS object module (precataloged). This module can be subsequently link-edited and cataloged in the core image library.

Input/output errors are processed by DOS device error recovery procedures. Input/output errors that cannot be corrected, such as permanent input/output errors and wrong-length records, are passed to the 1400/7010 program.

Console simulation and operator communication with the emulators are provided by the exchange of emulator commands and messages between the operator and the emulators. The emulators provide messages to inform the operator of errors or other conditions that require his attention or a response. Emulator commands can be entered from the console printer-keyboard and are handled in the same way as operator communications are currently handled by DOS.

Tape and Disk Emulation

The user has the option of processing tape files in 1400 format or in spanned variable-length record format. Two tape formatting programs - the Tape Preprocessor and Tape Postprocessor - are available to convert tape files from 1400 format to spanned record format, and vice versa; 1400/7010 tapes containing records larger than 32K must be converted to spanned record format prior to emulation.

The emulators accept as input two tape file formats:

1. 1400 format, which is produced by a 1400/7010 system, a stand-alone emulator, CS/30, CS/40, the Tape Postprocessor formatting program, or the Model 155 emulators

2. Spanned variable-length record format, which is produced by the Tape Preprocessor formatting program or the emulators

Either format can be produced as output by the emulators.

Processing tape files in spanned variable-length record format provides several advantages:

- Blocking short records reduces the time for emulating I/O operations.
- The Tape Preprocessor or the Tape Postprocessor program can be run concurrently with the emulators in a multiprogramming system.
- Files in spanned variable-length record format can be used by other Model 155 programs if the programs provide for handling the 1400/7010 label records and 1400/7010 tapemark records.
- The Tape Postprocessor program can be used to convert a file in spanned variable-length record format back to 1400 format for use on a 1400/7010 system.

Tape files in spanned record format have standard DOS labels; 1400/7010 labels are treated as data records, since they are processed by the 1400/7010 program. The 1400/7010 tapemarks appear as special data records and are recognized by the emulators.

The character codes supported by the emulators for magnetic tape data are:

- BCD representation in even and odd parity for seven-track tape (data translator on) in 1400 format
- BCDIC-8 representation for nine-track tapes in either 1400 or spanned record format, and for seven-track tapes (data converter on) in spanned record format. This character code, which is the eight-bit representation of BCD, is used to simulate parity. In normal mode, bit 1 is set to one for even parity, to zero for odd parity. In alternate mode, bit 1 is always set to one and no distinction is made between even and odd parity.

Two tape formatting programs, a preprocessor and a postprocessor, are available for converting tape files. They are distributed to run as problem programs in the background partition under DOS control and require a partition size of 4K and 5K, respectively, plus buffer areas.

The tape preprocessor program converts seven-track or nine-track tapes in 1400 format to seven-track (data converter on) or nine-track tapes in spanned variable-length record format with standard DOS labels. The tape postprocessor converts seven-track or nine-track tapes in spanned record format to seven-track or nine-track tapes in 1400 format.

Disk files in 1400 format, which are created on a 1400/7010 system or under stand-alone emulation, must be converted to a standard fixed-length record format on 2311 or 2314 disk packs before emulation. Disk files created under CS/30 and CS/40 can be processed by the 1401/1440/1460 emulator if the CS option is specified at emulator generation.

Existing 1400 utilities and the DOS Clear Disk utility program are used to convert disk files in 1400 format, and CS/30 and CS/40 files if desired, to the standard record format.

Each Model 155 disk record represents one 1400 disk track. Each Model 155 disk record is a fixed-length record, its length being a

function of the emulated 1400/7010 device and mode rather than the amount of 1400/7010 data on each track. A 1400/7010 disk file can occupy one or more extents on Model 155 disk packs but only one extent per pack. Extents must be allocated complete cylinders. When a file requires more than one Model 155 disk pack, the packs must be the same type. Two different 1400/7010 files may be placed on the same disk pack but this arrangement may increase seek time if both files are processed at the same time.

Character codes supported by the emulators for disk files are:

- EBCDIC representation for disk operations in move mode
- BCDIC-8 representation for disk operations in load mode. (Data written in load mode must be converted to EBCDIC if it is to be used by programs other than the emulators.)

To convert disk files in 1400 format, or CS/30 and CS/40 disks if desired, to a standard format on a Model 155 disk, the user must dump and restore his data as follows:

1. Dump the disk device, using a 1400/7010 disk-to-tape or disk-to-card utility program. When converting files on 1301, 1311, 1405, or 2302 disk devices that were created on a 1400/7010 system, the utility is executed on the system used to create the file. When converting files on 2302, 2311, or 2314 disks that were created under stand-alone emulation, CS/30, or CS/40, the utility is executed on a System/360 under control of the emulator used to create the disk file.
2. Use the DOS Clear Disk utility program to format previously initialized 2311 or 2314 disk pack(s) for the data.
3. Restore the data to a formatted 2311 or 2314 disk pack, using a 1400/7010 tape-to-disk or card-to-disk utility program under control of a Model 155 emulator. The 1401/1440/1460 emulator is used to restore 1401/1440/1460 data; the 1410/7010 emulator to restore 1410/7010 data.

DOS 1401/1440/1460 EMULATOR SUPPORT

For the DOS CS/30 and CS/40 user, the Model 155 DOS 1401/1440/1460 emulator continues the advantages of integrated emulation and provides additional advantages, such as:

- Emulators operating concurrently in all three partitions (now a restriction for the CS/30 user)
- Simulated 1400 storage that can begin at any address (now a restriction for the CS/40 user)
- Support for CS/30 and CS/40 disk and tape files
- System/370 data formats for emulator tape and disk files
- Preformatting of disk packs used for output is not necessary
- Added emulator control available to user at execution time
- DOS data management facilities and standard disk and tape label processing
- Support for CS/30 and CS/40 emulator control statements

The size of the partition required for emulation depends on the 1400 system being emulated, including standard and special features, input/output devices, buffers, etc. The processor storage required for the 1401/1440/1460 emulator is equal to the combined sizes of:

- Simulated 1401/1440/1460 storage. Each position of 1400 storage is simulated in one byte of Model 155 storage (for example, 8000 positions = 8000 bytes).
- Emulator routines required to emulate the 1401/1440/1460 system instructions, features, and I/O operations
- Tape, disk, and unit record buffers. The number and size of tape and disk buffers are specified by the user.

Estimated minimum 1401/1440/1460 emulator processor storage requirements for emulation of a 1400 system with unit record operations only, unit record/tape operations, or unit record/tape/disk operations are shown below.

Emulated Operations	DOS Partition Size (bytes)
1401/1440/1460 unit record	13K + 1401/1440/1460 core size + buffers
1401/1440/1460 unit record/6 tapes	18K + 1401/1440/1460 core size + buffers
1401/1440/1460 unit record/6 tapes/ 4 disks	22K + 1401/1440/1460 core size + buffers

The 1400 CPU features and 1400 I/O devices and special features supported and the Model 155 devices used for 1401/1440/1460 emulation are given in Tables 40.10.1 and 40.10.2. Table 40.10.3 lists the 1400 I/O devices that are not supported.

Table 40.10.1. 1401/1440/1460 I/O device and feature support and corresponding Model 155 devices

1401/1440/1460 Device and Features	Corresponding Model 155 Device
1402, 1442, 1444 Card Read Punch Features supported • Column Binary • Card Image • 51-Column Interchangeable Read Feed • Punch Feed Read • Punch Column Skip • Stacker Select • Processing Overlap Features not supported • Read Punch Release • Multiple card reader/punch operations	1442, 2520, 2540 Card Read Punch and 2501 Card Reader Note: Card reader and card punch operations may be emulated using a magnetic tape or direct access storage device
1403, 1404, 1443 Printer Features supported • Processing Overlap • Space Suppression Features not supported • Selective Tape Listing • Multiple printer operations • Read Compare	1403, 1443 Printer Note: Printer operations may be emulated using a magnetic tape or direct access storage device
1407, 1447 Console	3210 or 3215 console printer-keyboard
729, 7330, 7335 Magnetic Tape Unit Features supported • Column Binary • Processing Overlap Features not supported • Compressed tape	2400- and 3400- series magnetic tape • Seven-Track Compatibility feature is required if processing seven-track tapes
1301, 1311, 1405 Disk Storage Features supported • Direct Seek • Scan Disk • Track Record • Additional access arm (1405) Note: A 1405 cannot be emulated in combination with a 1301 or 1311	2311, 2314 direct access devices

Table 40.10.2. 1401/1440/1460 CPU features supported

Core storage from 1,400 to 16,000 positions. The 1401 Model G is not emulated.	Sense Switches
Expanded Print Edit	Advanced Programming
Inverted Print Edit	Indexing and Store Address Register
High-Low-Equal Compare	Bit Test
Multiply-divide	

Note: Translate feature is not supported

Table 40.10.3. Unsupported 1401/1440/1460 devices

1445 Printer	7340 Hypertape Drive
1011 Paper Tape Reader	1428 Alphameric Optical Reader
1012 Tape Punch	1231 Optical Mark Page Reader
1412 Magnetic Character Reader	1285 Optical Reader
1418 Optical Character Reader	Teleprocessing devices
1419 Magnetic Character Reader	

Emulator performance will vary depending on user options, such as number and size of buffers, the instruction mix of the 1401/1440/1460 programs, the format of tape files, and the priority of the partition in which the emulator is running.

Emulator performance is improved by:

1. Using double buffers and spanned record format for tape files in lieu of single or shared buffers and 1400 record format. (A shared buffer can be used by more than one I/O device.)

2. Using single buffers rather than shared buffers for disk files

3. Specifying device independence for emulating unit record operations on a magnetic tape or direct access storage device

4. Using a card reader that is not equipped with the 51-Column Interchangeable Read Feed and Column Binary features and not using the Select Stacker instruction

DOS 1410/7010 EMULATOR SUPPORT

The Model 155 DOS 1410/7010 emulator offers the 1410/7010 stand-alone emulator user the advantages of integrated emulation already discussed.

Processor Storage Requirements

The size of the partition required for emulation depends on the 1410/7010 system being emulated, including standard and special features, input/output devices, buffers, etc. The processor storage required for the 1410/7010 emulator is equal to the combined sizes of:

- Simulated 1410/7010 storage. Each position of 1410/7010 storage is simulated in one byte of Model 155 storage (for example, 20,000 positions = 20,000 bytes).

- Emulator routines required to emulate the 1410/7010 system instructions, features, and I/O operations

- Tape, disk, and unit record buffers. The size and number of tape and disk buffers are specified by the user.

Estimated minimum 1410/7010 emulator processor storage requirements for emulation of a 1410/7010 system with unit record/tape operations or unit record/tape/disk operations are shown below.

Emulated Operations	DOS Partition Size (bytes)
1410/7010 unit record and 6 tapes	27K + 1410/7010 core size + buffers
1410/7010 unit record, 6 tapes, 4 disks	37K + 1410/7010 core size + buffers

The 1410/7010 CPU features and 1410/7010 I/O devices and special features supported and the Model 155 devices used for 1410/7010 emulation are given in Tables 40.10.4 and 40.10.5. Table 40.10.6 lists the 1410/7010 I/O devices that are not supported.

Table 40.10.4. 1410/7010 I/O devices and features and corresponding Model 155 devices

1410/7010 Device and Features	Corresponding Model 155 Device
1402, 1442 Card Read Punch Features not supported Stacker Select 51-Column Interchangeable Read Feed	1442, 2540, 2520 Card Read Punch and 2501 Card Reader Note: Card reader and card punch operations may be emulated using a magnetic tape or direct access storage device.
1403 Printer All standard operations	1403, 1443 Printer Note: Printer operations may be emulated using a magnetic tape or direct access storage device.
1415 Console All standard operations	3210 or 3215 console printer-keyboard
729, 7330 Magnetic Tape Units All standard operations	2400- and 3400- series magnetic tape units Note: Seven-Track Compatibility feature is required for processing seven-track tapes.
1301, 1302, 2302 Disk Storage All standard operations Note: Any combination of 1301 and 1302/2302 disk storage drives can be emulated.	2311, 2314 direct access devices Note: An emulated 1302/2302 record will not fit on a 2311 disk track.

Table 40.10.5. Supported and unsupported 1410/7010 CPU features

Supported	Unsupported
Main storage up to 80,000 positions (1410) and 100,000 positions (7010) Inverted Print Edit Priority Feature Processing Overlap Channels one through four Floating Point Arithmetic	1401/1410 Compatibility Mode 7010 Diagnostic instruction, Branch on C Bit Diagnostic instruction, Branch if Tape Indicator J(I)K 7010 Memory Protect and Program Relocate 7010 Interval Timer

Table 40.10.6. Unsupported 1410/7010 devices

1311 Disk Storage Drive	1419 Magnetic Character Reader
1405 Disk Storage	7340 Hypertape Drive
1011 Paper Tape Reader	2321 Data Cell Drive
1412 Magnetic Character Reader	Teleprocessing devices

Emulator performance will vary, depending on user options, such as number and size of buffers, the instruction mix of the 1410/7010 program, the format of tape files, and the priority of the partition in which the emulator is running.

Emulator performance is improved by:

1. Using double buffers and spanned record format for tape files in lieu of single or shared buffers and 1400 record format. (A shared buffer can be used by more than one I/O device.)

2. Using single buffers rather than shared buffers for disk files

3. Emulating unit record operations on a magnetic tape or direct access storage device

40:15 OS DOS EMULATOR PROGRAM

The availability of the OS DOS emulator offers current DOS users who upgrade to a Model 155 the opportunity to convert to an OS operating environment more easily than is possible without the use of emulation. In addition, the OS DOS emulator user can benefit from the use of integrated emulation since the OS DOS emulator can execute concurrently with other OS jobs.

The OS DOS emulator for the Model 155 is a combination of the OS DOS emulator processing program and the optional OS/DOS Compatibility feature. This feature provides the relocation necessary for execution of a DOS supervisor and DOS programs under OS control in any processing program storage location. An OS MFT or MVT control program generated for a Model 155 is required also.

The OS DOS emulator and the DOS system being emulated (DOS supervisor and up to three processing program partitions) execute together in an MFT partition or MVT region, which must be a minimum of 38K. The OS DOS emulator program and tables require 22K plus another 4K if I/O staging is used. Additional OS DOS emulator program storage may be required depending on the I/O devices used. Up to ten I/O devices are supported in 22K, and 250 bytes are required for each additional device. The 4K I/O staging figure supports unblocked reader, printer, and punch records and residence of the required QSAM routines in the OS DOS emulator partition or region.

The DOS system being emulated can be 16K, 24K, or 32K and up in 4K increments. The OS DOS emulator is scheduled to operate in the same manner as any other OS job, and one or more OS DOS emulator jobs can execute concurrently with OS jobs if enough I/O devices and processor storage are available. In addition, the Model 155 OS 1401/1440/1460 and 1410/7010 emulator programs can execute concurrently with the OS DOS emulator if enough resources are present.

The user need not make any changes to the existing DOS supervisor, job control statements, tape files, or disk files in order to use the OS DOS emulator. Modification of existing DOS programs is required only for programs that contain features unsupported by the OS DOS emulator.

The major advantages of the OS DOS emulator are the following:

- Transition from a DOS to an OS operating environment is smoother. The conversion of DOS source programs, job control, and data files to OS formats can be done gradually for emulated DOS jobs.

- Model 155 OS DOS emulator users can continue to use most IBM-supplied application programs (Type II and program products) that operate under DOS but not OS and do not use BTAM or QTAM, by emulating them under OS.

- Dedicated emulation is not required, thus allowing the user to take advantage of OS facilities.

- Total system throughput is increased by operation of the OS DOS emulator in a multiprogramming environment and by using the staged I/O option of the OS DOS emulator. The latter permits emulated DOS programs to use the data transcription facilities of the OS reader interpreter and output writer to handle their unit record functions. Use of the staged I/O option of the OS DOS emulator also eliminates the necessity of dedicating unit record devices to DOS emulation.

All operating environments, control program facilities, and I/O devices supported by DOS can be emulated, with the following exceptions:

- Autotest and DOS OLTEP (the latter does not produce meanful results)

- Model-dependent functions such as CS/30, CS/40, and the DIAGNOSE instruction (1400 emulation can be handled using the Model 155 OS 1401/1440/1460 Emulator Program)

- Emulation of emulators that operate under DOS, for example, Model 155 integrated 1400/7010 emulators that operate under DOS

- 1259, 1412, and 1419 Magnetic Character Readers

- Teleprocessing devices (including the 2260 Display Station)

- Storage protection within the DOS system being emulated (among the DOS supervisor and partitions)

- DOS (and OS) direct access volumes having non-unique volume serial numbers online concurrently

- 1287, 1288 Optical Character Readers in document mode

In addition, DOS executable programs cannot be handled that:

- Rely on known timing relationships of the DOS system

- Depend on HALT I/O, READ DIRECT, WRITE DIRECT, AND DIAGNOSE instructions for their operation

- Require more than two bytes of sense data for an I/O device

- Use the PCI flag in a CCW

- Modify or use information in CCW's after the CCW list is initiated with a START I/O instruction and before the I/O operation terminates

- Initiate the same CCW list for an I/O operation on more than one I/O device concurrently

While a pseudo interval timer is maintained at simulated DOS decimal location 80, accurate time of day is not guaranteed because the timer is running only when the OS DOS emulator partition/region is executing and a time lag occurs during the interval required to update the timer.

The following I/O devices are supported by the OS DOS emulator:

- 1403, 1404, 1443, 1445, 3211 Printers
- 1052 Printer-Keyboard
- 1285, 1287, 1288 Optical Readers (the latter two not in document mode)
- 1442, 2520, 2540 Card Read Punches
- 2501 Card Reader
- 2311 Disk Storage Drive
- 2314 Direct Access Storage Facility
- 2321 Data Cell Drive
- 2400- and 3400-series magnetic tape units
- 2671 Paper Tape Reader
- Any new devices that are supported by both DOS and OS, subject to the programming restrictions stated

EMULATOR JOB SUBMISSION AND GENERAL OPERATION

DOS emulation is initiated as a single-step OS job via the input stream. An OS DOS emulator job can consist of one or more DOS jobs. The OS DOS emulator program, which must reside in SYS1.LINKLIB or a user job library, is specified in the EXEC job control statement included in the job control for the OS DOS emulator job. The following also must be identified in the DD job control statements for the OS DOS emulator job:

1. The DOS system residence and operator console devices
2. The location(s) of the DOS input stream(s)
3. I/O assignments for the staging of DOS unit record I/O operations
4. All the I/O devices that will be used by the DOS programs that are emulated as part of this DOS emulator job

The DOS system background partition input stream can be located in the OS input stream or on a separate data set. DOS batch-initiated foreground (BJF) partition input streams must be located in separate data sets.

If enough Model 155 processor storage is available, I/O staging can be used to increase OS DOS emulator job throughput and reduce the number of devices that have to be dedicated to the DOS emulation partition or region. It allows DOS unit record files SYSRDR, SYSPCH, and SYSLST to be emulated on direct access devices using the OS reader interpreter and output writer. DOS job control statements (for the BG partition) and/or card input to DOS programs to be emulated can be placed in the OS input stream and will be transcribed by the reader interpreter to SYSIN data sets on direct access devices. Thus, emulated DOS jobs steps will obtain their card input from OS SYSIN disk data sets. Output from emulated DOS programs can be placed in OS SYSOUT data sets on disk to be transcribed to the printer or punch by an output writer.

The following should be noted about the use of I/O staging. In OS, a job is not placed in the input queue, from which all jobs are scheduled, until the entire job (job control and input stream data for the job) has been read by the reader interpreter. Similarly, SYSOUT data sets produced during job step execution are not placed in the output queue for transcription by an output writer until job termination.

Thus, if all DOS jobs to be emulated are grouped together as a single OS DOS emulator job, DOS emulation cannot begin until all DOS

jobs (and their input stream data) have been read by the reader interpreter, and none of the SYSOUT data sets from completed emulated DOS jobs can be transcribed until the OS DOS emulator job itself terminates (all DOS jobs processed). This negates one advantage of I/O staging, which is the overlapping of unit record input and output data transcription with processing.

Therefore, consideration should be given to grouping DOS jobs into two or more OS DOS emulator jobs that execute one after the other in the OS DOS emulator partition/region. In addition, if the output from a particular DOS job is desired immediately, it should not be staged (written to a SYSOUT data set). The use of multiple OS DOS emulator jobs in an OS DOS emulator partition/region, instead of one, offers an additional advantage in optimizing device usage, as discussed later.

I/O operations and I/O error recovery procedures for emulated DOS programs are handled by the OS control program. All I/O devices to be used by emulated DOS programs must be allocated to the DOS emulation partition or region when the OS DOS emulator job is begun. These devices are dedicated to DOS emulation and cannot be allocated to any other executing OS jobs while DOS emulation is in operation. Thus, direct access devices and their data sets cannot be shared by an OS job step and an emulated DOS program. However, DOS direct access volumes can be shared by DOS partitions being emulated in the same OS DOS emulator partition or region. In addition, the user must ensure that all online OS DOS emulator direct access volumes have unique volume serial numbers with respect to other DOS and OS direct access volumes online at the same time.

Consideration should be given to grouping DOS jobs into multiple OS DOS emulator jobs according to the types and total number of I/O devices required. This can reduce the number of I/O devices that have to be dedicated to a DOS emulation partition or region at any given time, thereby making more devices available to other OS jobs.

When the DOS emulation job is initiated, the DOS emulator program is loaded into the OS DOS emulator partition/region. The DOS emulator program performs control block and table initialization and initiates an IPL from the DOS system residence volume. Once the DOS supervisor has been loaded and has established the DOS partitions, DOS job execution begins. DOS programs are loaded into the defined DOS partitions and emulated. Messages to the operator from the DOS emulator program are issued in standard OS format and include a unique identification to indicate that they are OS DOS emulator messages. If the MCS option is included in the OS control program, all DOS emulation messages can be routed to a specific console, and thus isolated.

The entire OS DOS emulator partition/region operates with a nonzero storage protect key to prevent it from interfering with the OS control program and other executing OS jobs. Therefore, the DOS emulator program, the DOS supervisor, and other DOS jobs in the emulator partition/region are not protected from inadvertent modification by an executing DOS program.

INSTALLATION OF THE OS DOS EMULATOR

The following are the major steps that a DOS user must take to install the OS DOS emulator on a Model 155:

- Data processing personnel -- systems analysts and designers, programmers, operators, etc.-- must be educated on OS

- The installation must decide which level OS control program will be used, MFT or MVT, and which functions and options are to be included.

- The desired OS operating system must be generated using a release of OS that includes Model 155 support. The DOS emulator option must be requested. Installation-designed routines, such as nonstandard tape label processing, accounting, etc., must be written, as required, and added to the generated operating system.

- DOS jobs that cannot be emulated must be converted to OS format. This involves source program changes, conversion of DOS job control statements to OS job control statements, and, depending on data organization, conversion of DOS files to OS data sets. The amount of reprogramming required depends on the source language being used. In general, high-level language programs require much less modification than Assembler Language programs.

- The volume serial numbers of all existing DOS direct access files must be inspected for duplicates and unique serials should be assigned where necessary. Volume serial numbers assigned to newly created DOS files or OS data sets should be unique as well.

- The OS job stream should be planned and consideration should be given to how OS DOS emulator jobs are to be scheduled and executed, as discussed previously in this subsection. Note also that the total storage size of the DOS system being emulated may be reduced. For example, if one DOS processing partition is devoted to teleprocessing, CS/30, or CS/40, which are not emulated by the OS DOS emulator, this DOS partition is no longer required and its storage can be made available for allocation to an OS partition or region.

- Optionally, the size of the emulated DOS system can be reduced by the removal of functions that are now provided by OS. For example, DOS POWER can be removed from a DOS system since data transcription can be handled by the OS reader interpreter and output writer. The model-dependent DOS MCRR and CCH routines can be removed from a DOS supervisor as Model 155 MCH and CCH routines contained in the OS control program will be used for machine and channel error handling.

  Note that alterations affecting the DOS supervisor normally require a system generation to be performed. In addition, any change resulting in a different starting address for a DOS partition means that existing nonrelocatable DOS programs executing in that DOS partition must be link-edited relative to the new address.

Figure 40.15.1 below illustrates a 256K Model 155 configuration that supports one OS processing partition (P2), a transient 44K reader interpreter (in P2), a resident output writer (P0), and emulation of a 128K DOS system (P1) using the staged I/O option.

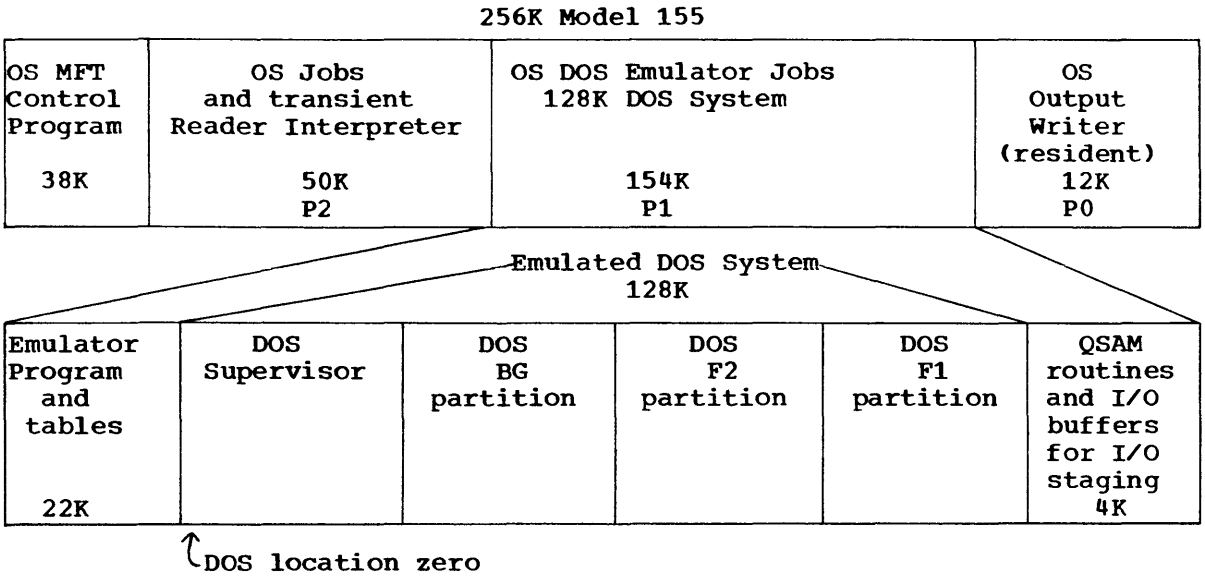


Figure 40.15.1. Sample 256K Model 155 configuration for emulation of a 128K DOS system.

SECTION 50: RELIABILITY, AVAILABILITY, AND SERVICEABILITY (RAS) FEATURES

50:05 INTRODUCTION

With the growth of more and more online data processing activities, as distinguished from traditional batch accounting functions, the availability of a data processing system becomes a very essential factor in company operations, and complete system failure is extremely disruptive. Because of the growing frequency of online processing and the fact that the Model 155 is designed to operate in such an environment, IBM has provided an extensive group of advanced reliability, availability, and serviceability features for the System/370 Model 155. These RAS features are designed to improve the reliability of system hardware, to increase the availability of the computing system, and to improve the serviceability of system hardware components.

The RAS features of the System/370 Model 155 are designed to reduce the frequency and impact of system interruptions that are caused by hardware failure and necessitate a re-IPL as follows.

- Hardware reliability is enhanced through use of more reliable components.
- Recovery facilities, both hardware and programming systems, not available for System/360 Models 40 and 50, are provided to reduce the number of failures that cause a complete system termination. This permits deferred maintenance.
- Repair procedures include more online diagnosis and repair of malfunctions concurrent with normal job execution in a multiprogramming environment in order to reduce the effect of such repairs on system unavailable time.

Each RAS feature, recovery or repair, is discussed in the remainder of this section.

The following recovery features are implemented in hardware:

- CPU retry of most failing CPU operations
- ECC validity checking on processor storage to correct all single-bit errors
- Automatic deletion of malfunctioning buffer blocks
- I/O operation retry facilities, including channel retry data provided in the ECSW and channel/control unit command retry procedures to correct failing I/O operations
- Expanded machine check interrupt facilities to facilitate better error recording and recovery procedures

The following recovery features are provided by programming systems:

- Recovery management support (RMS) to handle the expanded machine check interrupt and channel retry data. MCH and CCH routines are provided for OS (MFT and MVT only). MCAR and CCH routines are provided for DOS.

- Error recovery procedures (ERP) to retry failing I/O device and channel operations (OS and DOS)

- OBR and SDR routines (OS and DOS) to record statistics for I/O errors

- Environment recording, edit, and print program (EREP) for OS and DOS to format and print error log records

- I/O RMS routines (OS), alternate path retry (APR), and dynamic device reconfiguration (DDR) to provide additional recovery procedures after channel or I/O device failures

- Checkpoint/restart (OS and DOS) and warm start facilities (OS) to simplify and speed up system restart procedures after a failure necessitates a re-IPL

The following repair features are provided:

- Online Test Executive program (OLTEP) and Online Tests (OLT's) that execute under operating system control (OS and DOS) and provide online diagnosis of I/O device errors for most devices that attach to the Model 155.

- Processor Logout Analysis program (to operate under OS) to analyze machine check and channel error records in order to determine suspected malfunctioning field-replaceable units

- System Test and Storage Test stand-alone diagnostic programs to identify failing hardware units

- Microdiagnostics for customer engineer use to locate the field-replaceable unit within a malfunctioning component

These aids are designed to enhance system availability. In many cases, the system can run in a degraded mode so that maintenance can be deferred to scheduled maintenance periods. When solid failures do occur, their impact can be reduced by faster isolation and repair of the malfunction than is possible currently.

50:10 RECOVERY FEATURES

Additional hardware, which attempts correction of most hardware errors without programming assistance, has been included as part of the basic Model 155 system. The control program can be notified, via an interrupt, of both intermittent and solid hardware errors so that error recording and recovery procedures can take place.

AUTOMATIC CPU RETRY

All detected CPU hardware errors can be retried automatically by CPU retry hardware except those that occur during the execution of DIAGNOSE, TEST AND SET, READ DIRECT, and WRITE DIRECT instructions. Retry can take place after instruction errors, after failures that occur during interrupt time when status information is being saved, after errors that occur during status saving for I/O instructions, etc. Even an I/O instruction, such as START I/O or TEST I/O can be retried automatically by the hardware without an intervening I/O interrupt if the instruction has not proceeded beyond an established threshold point.

CPU retry is accomplished by additional microprogram routines and hardware included in the Model 155. The failing CPU operation is

retried by the microprogram up to eight times before it is determined that the error is uncorrectable. Checkpoints are taken and data is saved in backup locations during the operation of instructions that alter data as they execute, so that instructions can be retried from the point of correct execution. During retry operations, CPU fetches are made to processor storage, bypassing the buffer. In addition, the buffer is tested to determine whether a block malfunction caused the error.

When enabled, a machine check interrupt takes place after a CPU error occurs and is retried. If CPU retry was successful, the failure need only be recorded; if unsuccessful, programmed recovery procedures are required.

The CPU retry feature provides the Model 155 with the ability to recover from intermittent CPU failures that would otherwise cause a system halt and necessitate a re-IPL or that would cause an executing program to be terminated. Corrected errors are logged for later diagnosis during scheduled maintenance periods, thereby increasing system availability.

Retry of failing CPU operations on Models 40 and 50 is not provided by either system hardware or programming support.

ECC VALIDITY CHECKING ON PROCESSOR STORAGE

The ECC method of validity checking on processor storage provides automatic single-bit error detection and correction. It also detects all double-bit and most multiple-bit processor storage errors but does not correct them. Checking is handled on an eight-byte basis, using an eight-bit modified Hamming code, rather than on a single-byte basis, using a single parity bit. However, parity checking is still used to verify other data in a Model 155 system that is not contained in processor storage. Models 40 and 50 use parity checking for main storage data verification.

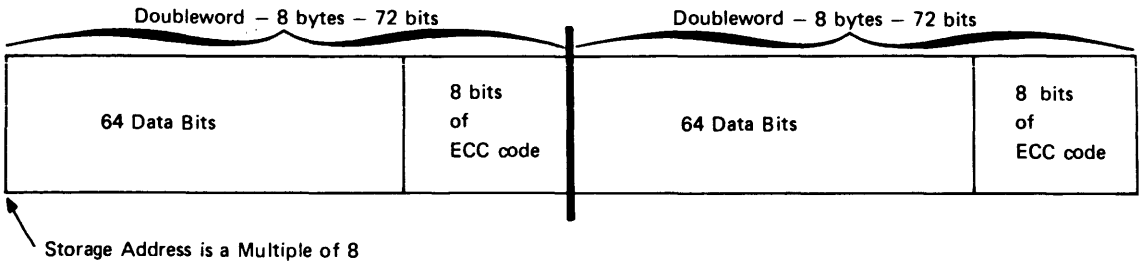
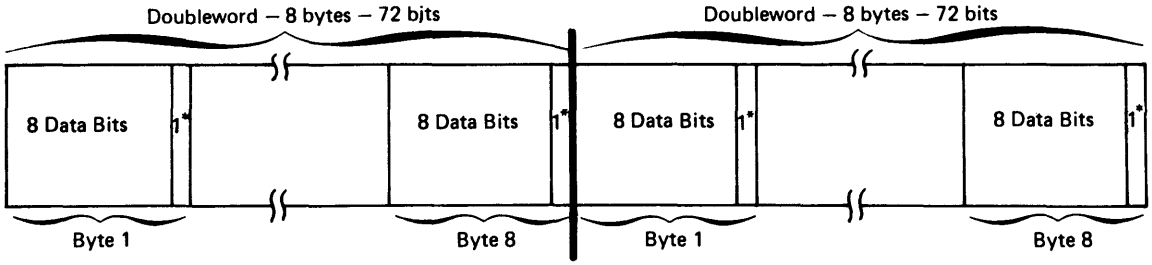


Figure 50.10.1. Data representation used in Model 155 processor storage



*Parity Bit

Figure 50.10.2. Data representation used in Models 40 and 50 processor storage and in the Model 155 in other than processor storage

Data enters and leaves processor storage through the storage adapter unit, which performs ECC validity checking on each doubleword. When a doubleword (72 bits) is fetched from processor storage, the storage adapter unit checks the 8-bit ECC code to validate the 64 data bits. If the data is correct, the adapter unit generates the appropriate parity bit for each of the 8 data bytes and reformats the doubleword to look as shown in Figure 50.10.2. If a single-bit error is detected, the identified data bit in error is corrected automatically by the corrector unit in the storage adapter. The corrected doubleword is sent back to processor storage and on to the buffer control unit. When a doubleword is to be placed in processor storage, the storage adapter unit strips the 8 parity bits, constructs the necessary 8-bit ECC code, and appends the code to the 64 data bits. The 72 bits are then stored as shown in Figure 50.10.1.

When a single-bit storage error is detected and corrected during the execution of an instruction or I/O operation, a machine check pending latch is set on and the operation continues. At the completion of the CPU operation a machine check interrupt occurs to allow error recording to be done unless ECC correction interrupts have been disabled. Identification of the failing storage address and bit in error is provided in a fixed storage area (discussed in the machine check interrupt explanation).

When a double- or multiple-bit storage error involving the CPU is detected, a machine check interrupt occurs and the error location is indicated in fixed storage. Error logging and recovery procedures should then be performed. When a double- or multiple-bit processor storage error occurs during an I/O operation, both a machine check and an I/O interrupt occur so that error recording and I/O retry procedures can be executed.

An ECC mode bit controls whether full recording or quiet mode is in effect for corrected single-bit processor storage errors. When quiet mode is in effect, a machine check interrupt does not occur after the successful correction of a single-bit error.

The ECC feature increases Model 155 system availability by permitting system operation to continue normally after single-bit processor storage errors occur and are corrected. Any processor storage errors on Models 40 and 50 necessitate at least termination of the processing program involved, since neither hardware nor programmed retry of processor storage errors is provided for these systems.

AUTOMATIC BUFFER BLOCK DELETION

When failure of a buffer component causes the buffer control unit to set the OK bit off for that block, a machine check interrupt occurs to permit error recording to occur (handled by the OS MCH or DOS MCAR routine). A buffer degrade counter is stored when the machine check interrupt occurs. It contains a count of the number of OK bits turned off during this interrupt.

I/O OPERATION RETRY

Channel retry, command retry, and CPU retry features are provided to reduce the number of abnormal program terminations and unscheduled system halts that occur because of channel errors.

- Channel Retry

  This feature has been implemented to insure that most failing channel operations can be retried by error-handling routines. When a channel error or a CPU error associated with a channel operation occurs, both the channel status word (CSW) and a new extended channel status word (ECSW) are stored in the fixed area during the I/O interrupt. The ECSW provides additional, more exacting status information about the channel failure. This data is formatted by the CCH routine and passed to a device-dependent error recovery routine to be used in the retry of the failing I/O operation.

  Channel error retry routines (channel check handlers) for System/360 models are provided only for Models 65 and higher. However, after a channel error occurs, these systems do not always present enough information to the error recovery routines to enable them to retry the failing operation. In other cases the channel may be left in a condition in which retry is impossible after a channel malfunction. Model 155 hardware improvements eliminate these two situations in most instances.

- Command Retry

  Command retry is a channel/control unit procedure that can cause an improperly executed command in a channel program to be retried automatically by hardware so that an I/O interrupt and programmed error recovery are not required. An indication is presented when

the control unit recognizes this situation. The byte multiplexer channel will not perform a command retry.

The command retry feature is implemented in the control unit of the 3330 and the 2305 facilities and was discussed in Section 20.

- CPU Retry

  If an error occurs during the execution of an I/O instruction, such as START I/O, TEST I/O, TEST CHANNEL, etc., system hardware determines whether or not the automatic CPU retry threshold for that particular instruction has been passed. If instruction execution has not gone beyond predetermined points, the instruction is retried automatically by the CPU retry hardware without programming assistance. A machine check interrupt is taken for recording purposes at the completion of a successful retry. If the instruction cannot be retried because it has passed beyond the retry threshold point, an I/O interrupt is taken or the condition code is set to indicate that a CSW and ECSW have been stored because the I/O operation was not started. The appropriate device-dependent error recovery routine can be scheduled to take the required recovery action. For example, if an error in the execution of a START I/O instruction occurs before the I/O device becomes involved, a CPU retry is possible.

EXPANDED MACHINE CHECK INTERRUPT FACILITIES

Implementation of the machine check level of interrupt on the System/370 Model 155 has been expanded in order to enhance error recording and error recovery procedures. Programming support of the extended machine check interrupt is provided by the Model 155 MCH and MCAR routines of OS and DOS, respectively.

The machine check interrupt facilities of the Model 155 differ from those of Models 40 and 50 as follows:

- Seven types of machine check are defined. They are grouped into three machine check subclasses: internal, external, and alert.
- A machine check interrupt occurs to permit the recording of errors corrected by the hardware as well as to allow recovery routines to handle errors that cannot be corrected by hardware.
- Machine check interrupt masking is expanded to handle selective disabling and enabling of the interrupt subclasses defined.
- The size of the fixed storage area in lower processor storage is increased to accommodate the storing of additional machine status and diagnostic information when a machine check interrupt occurs.
- Hard stop error conditions are defined that cause the Model 155 system to stop functioning immediately because the nature of the machine malfunction prevents valid processing from continuing.

The Model 155 presents one of seven types of machine check interrupt, depending on the specific machine malfunction. Each type of interrupt belongs to a machine check subclass that is maskable. A machine error causes a soft machine check or a hard machine check interrupt when its subclass is enabled. A soft machine check occurs after the hardware has been successful in correcting an error or after an error has occurred that does not adversely affect the executing

program. This is done so that the failure can be recorded and operation continues after the error is logged. For example, if a soft error occurs during the execution of an instruction and the CPU retry hardware corrects the error by reexecuting the failing instruction, a soft machine check interrupt occurs at the completion of the successful execution.

A hard machine check occurs when hardware retry fails or is not possible. For example, if the CPU retry hardware has been set to retry a failing instruction after eight retries, a hard machine check interrupt occurs after the last unsuccessful retry.

Figure 50.10.3 shows the layout of fixed processor storage for the Model 155. Fixed storage consists of three areas: the fixed logout area in decimal addresses 0-127, the fixed logout area in decimal addresses 128-511, and the CPU extended logout area of 640 bytes, which begins at location 512 and continues to location 1151 unless the starting address is changed by programming.

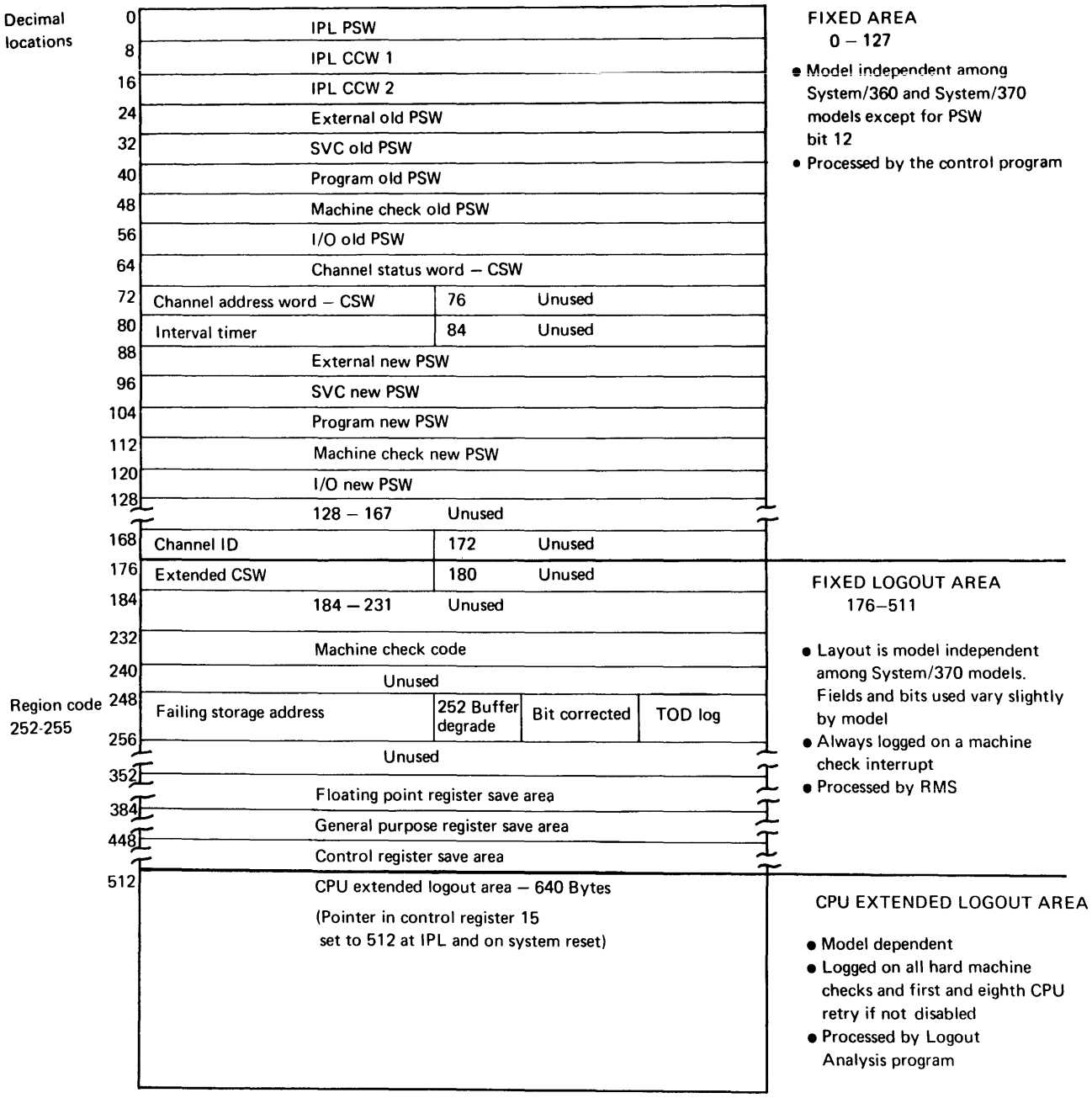


Figure 50.10.3. Model 155 fixed storage locations

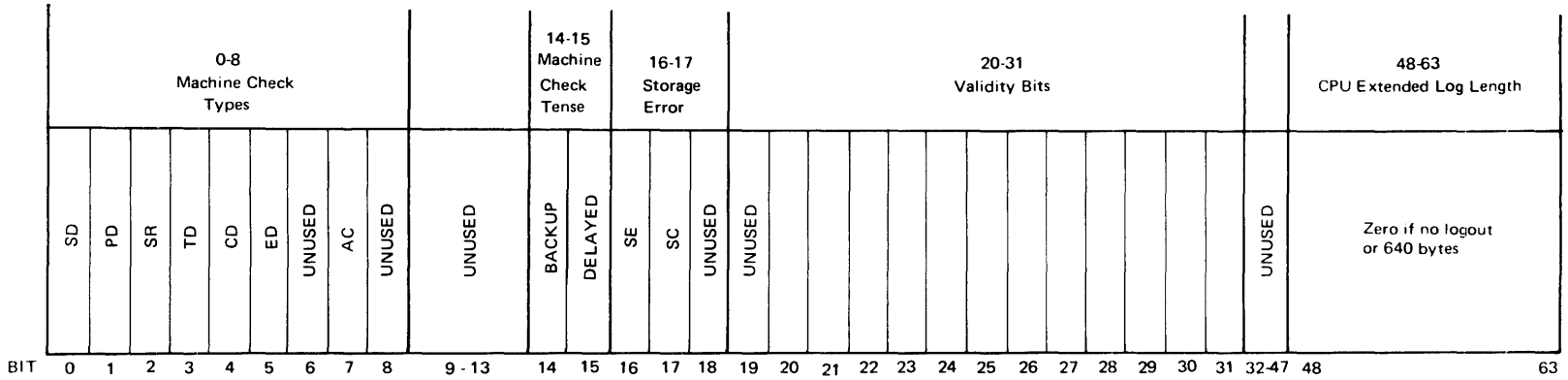
Fixed locations 0-127 are identical in layout and content to these locations in System/360 models, with the exception of the EBCDIC/ASCII bit in the PSW, which must be set to zero.

A logout to the fixed logout area (176-511) occurs when any type of machine check interrupt is taken. The data stored is processed by recovery management routines. The layout of this area is model independent among System/370 models; however, all models do not use every field or bit defined. The fixed logout area data indicates the reason for the interrupt in the machine check code and the region code. The save areas in the logout area preserve the status of the system at the time of the machine check interrupt and contain the contents of the general purpose, the floating-point, and the control registers.

The model-dependent CPU extended logout area begins at the address specified in control register 15, which is set by the hardware to decimal location 512 by an IPL or on a system reset. The length of this extended logout area on the Model 155 is 640 bytes. A logout to the extended area occurs on certain types of machine check errors only if the log suppression mask bit in control register 14 is enabled. This data can be recorded by recovery management routines and the Processor Logout Analysis program can be used to process this information at a later time.

Figure 50.10.4 illustrates the layout and the contents of the eight-byte machine check code stored in processor storage locations 232-239. The machine check code indicates which type of interrupt occurred, the validity of certain fields stored in the fixed logout area, and the length of the stored CPU extended logout area. The region code is used to further describe processor storage, high-speed buffer, and time of day clock errors.

Fixed Logout Area Locations 232-239



Subclass	Bit	Interrupt Type
Internal	0	SD – System Damage
	1	PD – Instruction Processing Damage
	2	SR – System Recovery
External	3	TD – Timer Damage
	4	CD – Time of Day Clock Damage
	5	ED – External Damage
	6	Unused
Alert	7	AC – Automatic Configuration

Bit	Storage Error
16	Storage Error Uncorrected
17	Storage Error Corrected

Bit	Valid Fixed Area Data
20-23	Machine Check Old PSW (48-55) 20 AMWP 21 Masks and Protect Key 22 Program Mask and Condition Code 23 Instruction Address
24	Failing Storage Address (248,249)
25	Region Code (252-255)
26	Unused
27	Floating Point Registers (352-383)
28	General Purpose Registers (384-447)
29	Control Registers (448-511)
30	CPU Extended Logout
31	Storage (Validity of main storage being processed by instructions when interrupt occured)

Figure 50.10.4. Model 155 Machine check code

Table 50.10.1 lists the machine check types defined for the Model 155. They are described in the discussion that follows. The mask bits used to enable or disable interrupts for each subclass are indicated and the setting of the machine check and region codes are discussed. PSW bit 13 and three other mask bits are used to enable and disable machine check interrupts. The recovery mask (R), configuration mask (C), and external mask (E) bits are contained in control register 14 and operate subject to PSW bit 13. If PSW bit 13 is disabled, all machine checks are masked. If PSW bit 13 is enabled, the settings of the three additional mask bits determine whether or not interrupts, other than Instruction Processing Damage and System Damage, will be taken. (Refer to Figure 50.10.4.)

Table 50.10.1. Model 155 machine check interrupts

Subclass	Mask Bit(s)	Interrupt Type and Cause	Machine Check
Internal	PSW 13	System Damage •Irreparable hardware malfunction	Hard
Internal	PSW 13	Instruction Processing Damage (One of the following occurs during instruction execution.) •Unretryable CPU error •Uncorrectable CPU error •Multiple-bit processor storage error •Storage protect key failure	Hard
Internal	PSW 13 and R	System Recovery •CPU error corrected by retry •Single-bit processor storage error corrected by ECC	Soft
External	PSW 13 and E	Interval Timer Damage	Soft
External	PSW 13 and E	Time of Day Clock Damage	Soft
External	PSW 13 and E	External Damage •Error that did not affect the CPU (e.g., multiple-bit processor storage error during I/O operation)	Soft
Alert	PSW 13 and C	Automatic Configuration •Buffer block deletion	Soft

Soft Machine Check Interrupts

- System Recovery - This interrupt occurs if both PSW bit 13 and the recovery mask bit are on. It is caused by a successful CPU retry or a single-bit processor storage error correction.

  The SR bit in the stored machine check code (bit 2) is used to indicate successful hardware recovery. When the SR bit is on without another recovery bit, an error has occurred in the normal functioning of the CPU and the CPU operation has been retried successfully by CPU retry hardware. CPU extended logout data is generated after the first and eighth CPU retry.

The SC bit in the stored machine check code (bit 17) is used together with the SR bit to indicate that the ECC hardware corrected a single-bit processor storage error and passed correct information about the error to the CPU. This information is the failing storage address, which is stored in locations 248-251, and a code to indicate the bit corrected, which is stored in byte location 254. Validity bits 24 and 25 indicate that the failing storage address and bit-corrected fields, respectively, have been stored correctly. An extended CPU logout is not generated after a successful ECC correction. Only error recording is required for this interrupt.

- Automatic Configuration - This interrupt occurs if both PSW bit 13 and the configuration mask bit are on. The AC bit in the stored machine check code (bit 7) is on to indicate that a block of the buffer was deleted because of a malfunction. This error is accompanied by a system recovery, system damage, or instruction processing damage indication.

  A CPU error causes the buffer to be analyzed and any malfunctioning blocks are deleted. A buffer degrade counter is stored in locations 252 and 253 to indicate the number of blocks just deleted. Validity bit 25 indicates whether or not the counter has been stored correctly. The OK bit in the index array entry for any failing block is set to indicate that the corresponding buffer block has been deleted. All future CPU fetches for these blocks will be made directly to processor storage, bypassing the buffer. Only error recording is required for this interrupt if a system recovery indication is present also.

- Interval Timer Damage - This interrupt occurs if PSW bit 13 and the external mask bit are on. It indicates damage to the timer itself or to processor storage location 80. Programmed validation procedures and error logging are required.

- Time of Day Clock Damage - This interrupt occurs if both PSW bit 13 and the external mask bit are on. The CD bit in the stored machine check code (bit 4) is used to indicate that an error occurred in the time of day clock that renders the clock invalid. Once this invalid indication has been given, subsequent STORE CLOCK instructions cause the condition code in the current PSW to indicate the fact that the clock is invalid. The time of day log field in byte 255 is set also. Four bits are stored to indicate the failing replaceable unit of the clock. Error logging is required as a result of clock failure.

- External Damage - This interrupt occurs if both PSW bit 13 and the external mask bit are on. The ED bit of the stored machine check code (bit 5) is used to indicate that damage has been detected but that operations associated with the CPU were not affected because the multiple-bit failure was associated with an I/O or console operation. The failing processor storage address is indicated and the SE bit is on, but a CPU extended logout is not stored. When this type of error occurs, both a soft machine check and an I/O interrupt are taken. A soft machine check interrupt occurs at the completion of the instruction in operation at the time of the error in order to allow error recording to occur. Error recovery procedures are initiated after the I/O interrupt that occurs at the completion of the I/O operation.

Hard Machine Check Interrupts

- Instruction Processing Damage - This interrupt occurs if PSW bit 13 is on. The PD bit in the stored machine check interrupt code (bit 1) is used to indicate that an error occurred during the execution of the instruction indicated by the machine check old PSW. The error was either a multiple-bit processor storage failure, a storage protect key failure, or a CPU error that was unretryable or that could not be corrected by the CPU retry hardware.

  If a multiple-bit processor storage failure caused the interrupt, the SE bit in the stored machine check code (bit 16) is on also and the address of the failing storage area is indicated in locations 248-251. The PD and backup bits are set also when a storage protection failure occurs. The CPU extended logout area indicates a storage protection failure.

  If an unsuccessfully retried CPU failure caused the interrupt, the backup bit in the machine check code (bit 14) indicates the extent of the damage that occurred, if any. If the back-up bit is on, it indicates that no source data has been changed and that the PSW registers and storage reflect the valid state that existed at the beginning of the instruction. A logout to the CPU extended logout area also occurs. (For a CPU error, an extended logout is generated on the first and eighth unsuccessful retry.)

  Error logging and the execution of recovery procedures are required after this interrupt type.

- System Damage - This interrupt occurs if PSW bit 13 is on. The SD bit in the stored machine check code (bit 0) is used to indicate that an irreparable CPU failure occurred that was not a result of the execution of the instruction indicated in the machine check old PSW. An unsuccessful retry of an interrupt or a wait state, microcode failure, control register damage, etc., are examples of system damage errors. System damage also is indicated if the error cannot be identified as one of the other types of machine check interrupt. A CPU extended logout is generated. Programmed error recovery is not possible after this type of failure.

Modes of System Operation

Two modes of system operation are possible: full recording mode and quiet, or nonrecording, mode. In full recording mode all machine check interrupt types cause an interrupt to be taken and logouts to occur. This is the normal mode of Model 155 operation. In quiet mode, all or certain soft machine check interrupts are disabled. Quiet mode can be used to permit system operation without error recording for all or certain soft errors when a large number of transient (correctable) errors are occurring. It also can be used to allow Model 155 operation under the control of an operating system without Model 155 machine check handling routines included.

A hard stop status and a hard stop bit have been defined for the Model 155. The hard stop bit is located in control register 14 with the other three mask bits discussed. If a hard stop condition occurs, the Model 155 system ceases all operations immediately without the occurrence of a logout to the fixed area. Hard stop is initiated by hardware rather than by programming.

Generally speaking, a hard stop situation is caused by the occurrence of a hard machine check type of error during the processing of a previous hard machine check error. Implementation of a hard stop prevents system operations from continuing when the nature of the machine malfunction prevents the system from presenting meaningful status data.

The state of the Model 155 after IPL or a system reset is:

1. Recovery reports are disabled. Successful CPU retries and single-bit processor storage error corrections by ECC hardware do not cause machine check interrupts.

2. Configuration reports are disabled. Buffer block deletions do not cause machine check interrupts.

3. External damage reports are enabled. Interval Timer Damage, Time of Day Clock Damage, or a double- or multiple-bit processor storage failure associated with an I/O operation causes a machine check interrupt.

4. PSW bit 13 normally is set to one by the IPL PSW (it is disabled by system reset) to enable Systems Damage and Instruction Processing Damage interrupts. Therefore, an irreparable system error, an unretryable CPU failure, an unsuccessfully retried CPU failure, or a multiple-bit processor storage error associated with the CPU causes a hard machine check interrupt.

5. Hard stop is enabled.

6. CPU extended logout is enabled and control register 15 points to location 512 as the beginning of the CPU extended logout area.

These status settings cause the Model 155 to run in quiet mode for hardware-corrected errors. If the Model 155 is to operate in full recording mode, the appropriate mask bits must be altered by the control program.

MACHINE CHECKS ON SYSTEM/360 MODELS 40 AND 50

A machine check situation in Models 40 and 50 results from hardware detection of a machine malfunction or of a parity error. Bad parity can occur in main storage, in local storage, in a register, in an adder, etc. Error correction is not attempted by Model 40 or 50 hardware when a machine check occurs. If the machine check mask in the current PSW (bit 13) is enabled, a machine check causes an interrupt and a diagnostic scan-out occurs, starting at location 128. The number of bytes logged is model dependent.

If an SER routine (OS) or the MCRR routine (DOS) is present in the Model 40 or 50 control program, it gains CPU control after the machine check interrupt, and the error is logged. A retry of the failing operation is not provided by these routines and the affected program is terminated abnormally. If MCRR is not present in a DOS supervisor, the system is placed in a wait state when a machine check interrupt occurs. (An OS control program must contain a machine check handling routine, SER0 or SER1 for Models 40 and 50, as of Release 17.)

RECOVERY MANAGEMENT SUPPORT (RMS) FOR OS MFT AND MVT

RMS for the Model 155 consists of extensions to the facilities offered by RMS routines currently provided for Models 65 and up. The

two RMS routines, machine check handler (MCH) to handle machine check interrupts and channel check handler (CCH) to handle certain channel errors, will be included automatically in MFT and MVT control programs generated for the Model 155. Approximately 7000 bytes of resident (nucleus) processor storage is required for Model 155 recovery management. A Model 50 user with a 3K SER1 routine included in the control program will require only a 4000-byte increase in resident control program storage as a result of the inclusion of Model 155 RMS.

The two primary objectives of RMS are (1) to reduce the number of system terminations that result from machine malfunctions and (2) to minimize the impact of such incidents. These objectives are accomplished by programmed recovery to allow system operations to continue whenever possible and by the recording of system status for both transient (corrected) and permanent (uncorrected) hardware errors.

Machine Check Handler

After IPL of a control program containing Model 155 RMS routines, mask bits are enabled and control register values are set to permit all machine check interrupts and logouts to occur.

Soft Machine Checks

MCH receives control after the occurrence of both soft and hard machine check interrupts. When a System Recovery or an Automatic Configuration, accompanied by a System Recovery soft machine check, occurs (successful CPU retry, single-bit processor storage error corrected, or buffer block deleted), MCH formats a recovery report record to be written in the system error recording data set SYS1.LOGREC. This record contains pertinent information about the error, including the data in the fixed logout area, an indication of the recovery that occurred, identification of the job, job step, and program involved in the error, the date, and the time of day. MCH schedules the writing of the recovery report record and informs the operator that a soft machine check has occurred.

Prior to relinquishing CPU control, MCH determines whether or not an automatic mode switch from recording mode to quiet mode should take place if a CPU retry or an ECC correction recovery report has just occurred. The determination of whether to switch to nonrecording (quiet) mode is made on the basis of the number of soft machine checks of a specific type that occur during system operation. Error count thresholds are maintained separately for successful CPU retry and successful processor storage single-bit error corrections. The IBM-supplied threshold values can be altered when the control program is generated or by an operator command during system operation.

MCH switches the system to quiet mode for either ECC corrections only (the DIAGNOSE instruction is used to change the ECC mode bit from full recording to quiet mode) or both CPU retry and ECC corrections (the System Recovery mask bit is disabled). Mode switching occurs if the number of soft machine checks that occur during system operation exceeds the specified error count threshold for that type. The operator is informed of the mode switch and can switch back to recording mode at any time thereafter.

Mode switching is implemented to attempt to prevent SYS1.LOGREC from being filled with recovery reports when a recurring correctable error condition exists that would cause many reports to be generated.

When a buffer block deletion recovery report occurs, MCH records the error and informs the operator but does not maintain a threshold value for implementing quiet mode for this interrupt. The total number of buffer blocks deleted since system operation began is indicated,

and when a significant number of buffer blocks have been deleted, the operator can disable the entire buffer, using the console switch provided, if desired.

The operator is informed of the occurrence of a Time of Day Clock Damage or an Interval Timer Damage machine check interrupt. Error recording is performed. The system is placed in a wait state after a TOD clock error.

Only error recording is required after an External Damage soft machine check interrupt (multiple-bit processor storage error during an I/O operation). I/O error recovery will be performed after the ensuing I/O interrupt. (See Figure 50.10.5 for the general flow of OS MCH processing after soft machine checks.)

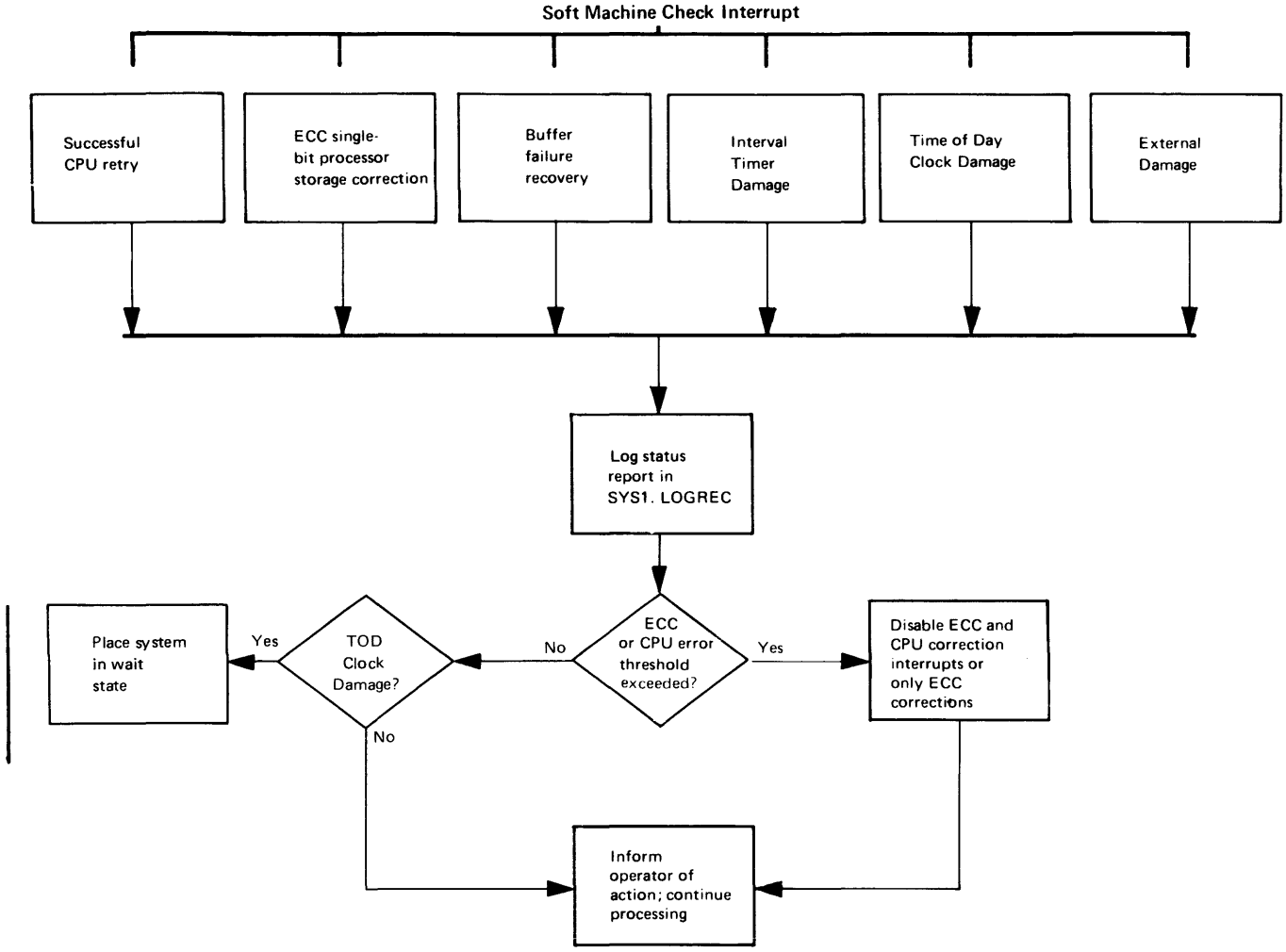


Figure 50.10.5 General flow of OS MCH processing after soft machine check interrupts.

Hard Machine Checks

When an Instruction Processing Damage hard machine check occurs (uncorrectable or unretryable CPU error, multiple-bit processor storage error, or storage protect key failure), MCH determines whether the error is one that is correctable by programming, such as a multiple-bit storage error or a storage protect key failure.

The program damage assessment and repair (PDAR) routine of MCH can repair damaged control program storage areas by loading a new copy

of the affected module if the module is marked reentrant and refreshable (it has been written in a read-only manner that allows reloading of the module at any time without altering execution results). Only refreshable modules residing in the control program nucleus, the link pack area, or an SVC transient area that are damaged are refreshed, if possible. Processing program modules are not refreshed. PDAR also attempts to repair storage protect keys.

If PDAR cannot correct the error or if the error is an uncorrectable type, PDAR attempts to identify the task associated with the error so that the task can be terminated abnormally. A damage report record, which contains both the fixed and CPU extended logout area data, the recovery action taken, the program identification, the date, and the time of day, is prepared and logged. System operation continues if the error is corrected or if the error task associated with an uncorrectable error can be identified and terminated. System operation halts, and a re-IPL is required if an uncorrectable error damages a portion of the control program or if the error cannot be associated with a specific task. The operator is informed of whatever action is taken.

When a System Damage hard machine check occurs, programmed recovery is not possible, and MCH places the system in a wait state after a logout and termination procedures are attempted.

MCH for the Model 155 contains model-dependent routines and will not execute correctly on System/360 models or another System/370 model. (See Section 60:15 for a discussion of operating system portability.)

See Figure 50.10.6 for a general flow of OS MCH processing after hard machine check interrupts.

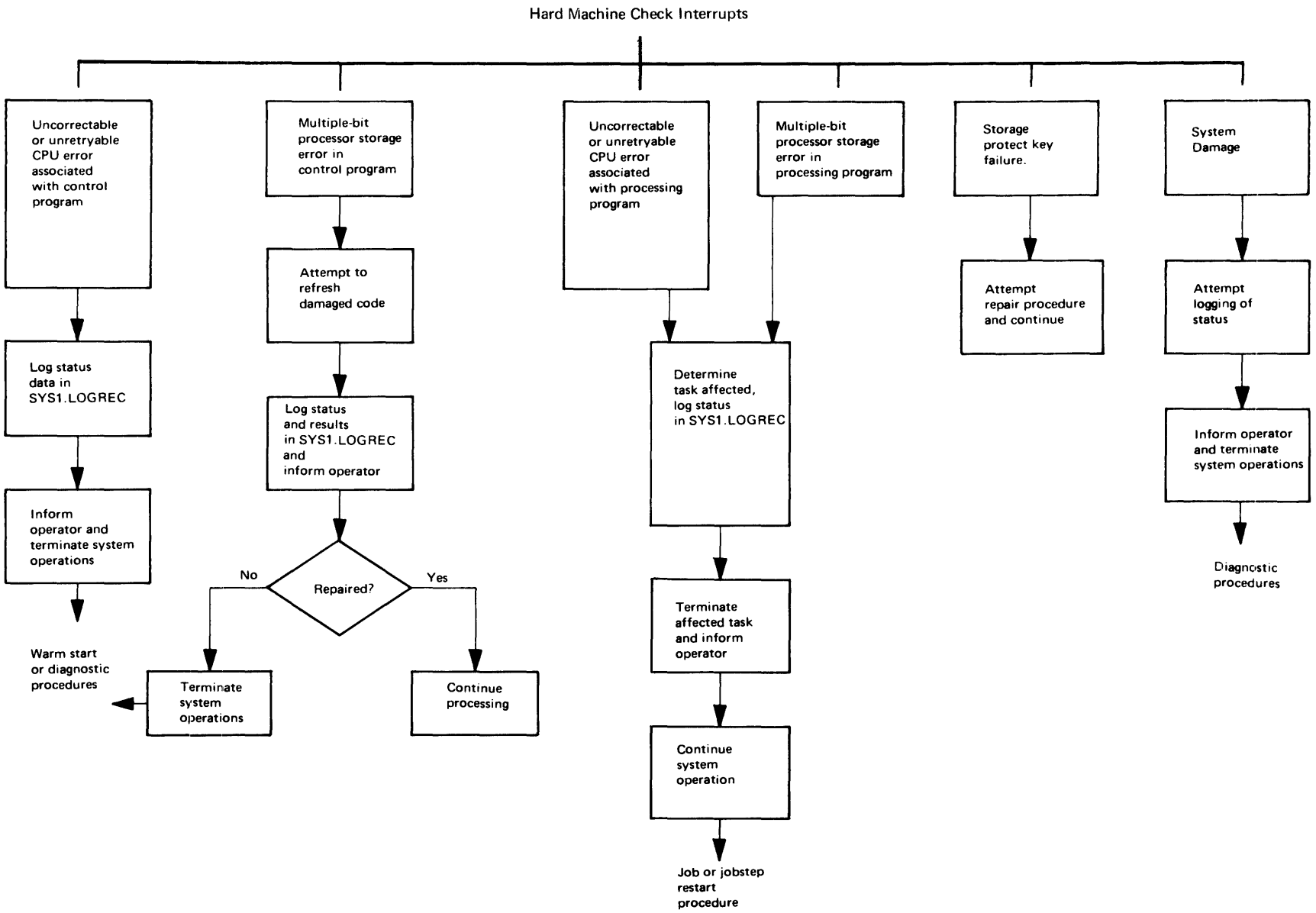


Figure 50.10.6. General flow of OS MCH processing after hard machine check interrupts

Channel Check Handler

CCH receives control after a channel error causes an I/O interrupt. CCH formats both an error information block (containing the ECSW) for use by an ERP routine and a CCH error record for recording in SYS1.LOGREC. The latter contains status information from the logout area, the ECSW, program identification, date, and time of day.

If CCH determines that operating system integrity has been impaired by the channel error, control is given to MCH for error recording, and system operations are terminated. Otherwise, the error information block and error record are passed to the appropriate device-dependent error recovery procedure (ERP), which logs the error record and retries the failing I/O operation, using status information from the error information block. If a successful retry occurs, system operation continues. If the error is deemed permanent (uncorrectable), another error record is prepared and recorded by the outboard recorder routine (OBR), and the task involved is abnormally terminated (unless I/O RMS or a user-written permanent error handling routine is present). The operator is informed of the abnormal termination and system operation continues.

The CCH routine is structured in a manner that makes it model independent. A channel/model-independent module resides in the operating system nucleus. The required channel-dependent modules for the Model 155 included in the operating system at system generation time are loaded during the IPL procedure. The nucleus initialization program (NIP), using channel configuration data specified by the user at system generation time and the new STORE CHANNEL ID instruction, determines the types of channels present in the system. CCH routines are, therefore, compatible for System/370 Models 155 and 165 and for System/360 Models 65, 75, 85, 91, 195, and MP/65 systems.

Figure 50.10.7 at the end of this subsection shows the general flow of programmed error recovery procedures after an I/O interrupt.

RECOVERY MANAGEMENT SUPPORT (RMS) FOR DOS

Machine check analysis and recording (MCAR) and channel check handler (CCH) routines provide support similar to that provided by the OS RMS routines. MCAR, CCH, and the I/O error recording routines OBR and SDR will be included automatically in a DOS supervisor generated for a Model 155. The resident processor storage requirement for these four routines is approximately 6400 bytes in the supervisor area. A Model 50 DOS user with MCRR and OBR/SDR included in the supervisor being used will experience approximately 1100 bytes increase in supervisor size because of the inclusion of Model 155 RMS.

When a System Recovery or Automatic Configuration/System Recovery soft machine check occurs, an environment record (recovery report), containing pertinent status information from the fixed area, recovery action, program identification, date, and time of day, is constructed by MCAR and written in the environmental recording data set (ERDS), whose symbolic unit name is SYSREC (corresponding to the SYS1.LOGREC recording data set of OS). MCAR then determines whether a switch from recording mode to quiet mode should take place for ECC corrections only or for both ECC and CPU retry corrections as discussed for the OS MCH routine. The operator is informed of whatever recovery action is taken, and system operation continues.

If the error damaged the time of day clock, or if damage to the interval timer occurred together with an uncorrectable storage or protection error, the system is placed in a hard wait state after an attempt to record the error is made.

When an Instruction Processing Damage hard machine check occurs during the execution of supervisor (or any privileged) code, the system is placed in a hard wait state after an attempt is made to prepare and record a damage report record. MCAR does not attempt to refresh damaged supervisor code. The occurrence of an Instruction Processing Damage interrupt during processing program execution always results in termination of the program involved (the partition is canceled) after error recording occurs.

MCAR performs repair procedures if a storage protect key failure or multiple-bit processor storage error occurs in a processing program partition. Validation of damaged processor storage is attempted by moving a double-word of binary zeros and then ones into the area.

A System Damage hard machine check interrupt results in an attempt to record the error, followed by system termination (a hard wait state). The operator is informed of whatever action is taken after a hard machine check occurs, including whether or not error recording was successful.

CCH receives control after a channel error occurs. It records the error in SYSREC and passes the ECSW and other pertinent status information to the appropriate error recovery routine (ERP) unless analysis of the error indicates that system operation cannot continue (the error involved SYSRES, for example). If the ERP can correct the error, operations continue. If a permanent channel error exists, CCH records the error and cancels the partition affected. The operator is notified.

The recovery support provided by the MCAR and CCH routines represents an extension of the facilities provided by the optional MCRR routine of DOS, which is available for System/360 models and which does not contain any repair or channel retry procedures.

ERROR RECOVERY PROCEDURES (ERP'S) - OS AND DOS

These device-dependent error routines are a standard part of the control program generated for any OS or DOS environment. OS ERP's will be modified to accept and use channel logout (ECSW) data formatted by the CCH routine after a channel error. The ECSW data provided by the DOS CCH routine will be handled by a set of completely new CCH ERP routines. The DOS CCH ERP's are an addition to the current set of ERP's. The latter will be used without modification.

OS ERP routines written for the 3211 Printer, the 3330 facility, and the 2305 facility will include support of the larger number of sense bytes provided by the control units of these devices. The DOS ERP for the 3211 Printer will also support these sense bytes.

When a channel or an I/O device error occurs on a Model 155, the appropriate ERP is scheduled to perform recovery procedures. If the error is corrected, operations continue normally. If the error cannot be corrected (it is permanent), error recording occurs. If I/O RMS or a user-written permanent error handling routine is not present, the affected OS task or DOS partition is abnormally terminated. The operator is notified of permanent I/O errors. (See Figure 50.10.7.)

STATISTICAL DATA RECORDER (SDR) AND OUTBOARD RECORDER (OBR) - OS AND DOS

OBR and SDR routines are included in all OS control programs. OBR and SDR are included in any DOS supervisor generated for a Model 155.

These routines are requested by the ERP routines during their processing. The SDR routine is requested when one of the error statistics counters becomes full. Counters are maintained in the resident control program storage area for each I/O device in the system configuration. SDR records these statistics in the appropriate SDR summary record for that device contained in the error log data set (SYS1.LOGREC for OS, SYSREC for DOS). This insures recording of temporary I/O device error data. The OBR routine of OS records both temporary and permanent channel errors (handled by the CCH routine in DOS) and writes an outboard record containing pertinent status data whenever a permanent error occurs for a device. SDR is also executed to write accumulated statistics for that device when a permanent error occurs. (See Figure 50.10.7.)

ENVIRONMENT RECORDING, EDIT, AND PRINT PROGRAM (EREP) - OS AND DOS

OS EREP is a standard system utility that can be initiated as a job step via standard job control statements at any time. It contains model-dependent routines and will be extended to handle the status records written by System/370 OS RMS routines. It performs the following:

1. Edits and prints all error records contained in SYS1.LOGREC. These records have been constructed and written by MCH, CCH, OBR, and SDR routines.

2. Accumulates a history of specified record types from SYS1.LOGREC by creating or updating an accumulation data set.

3. Edits and prints a summary of selected records from SYS1.LOGREC or an accumulation data set.

The currently available EREP routine of DOS is a special purpose utility that can be initiated as a job step via job control statements in the input stream or by an operator command typed in on the console. Its function is to edit and print all error records contained in the SYSREC recorder file. EREP will be extended to handle all status records written by DOS Model 155 recovery routines (MCAR, CCH, OBR, SDR) and will be included in all DOS operating systems generated for the Model 155. EREP also will be extended to include support of an accumulation file on tape created from SYSREC records. This tape is formatted to be used as input to the Logout Analysis Program (discussed in Section 50:15). Modifications to the current EREP will enable it to perform the three functions outlined above for the OS EREP routine.

I/O RMS FOR OS

I/O RMS routines are optional, model-independent routines supported in MFT and MVT environments. These reconfiguration procedures attempt to minimize the number of abnormal job terminations and unscheduled system halts that occur because of errors on channels or I/O devices.

The alternate path retry (APR) routine provides for the retry of a failing I/O operation on another channel path to the device involved, if one is available, when an uncorrectable channel error occurs. Thus APR, if present, is entered from a device-dependent ERP when a permanent error is deemed to exist after retry procedures have been attempted.

corrected using the alternate channel path,
If a permanent error still exists, the task is
unless the DDR routine is present. A
path can be varied offline by the operator if

reconfiguration (DDR) routine permits the operator
volume from one device to another of the same
hardware error occurs and provides repositioning
that the failing I/O operation can be retried. A
demounted so that device cleaning procedures can
it can then be remounted on the same device. The
supports demountable system residence devices and unit
DDR is entered from a device-dependent ERP after
either channel or device, occurs on a demountable
nation occurs if the error cannot be corrected and
ment error handling routine is not present. (See

included in DOS support, which handles alternate
for tape drives and does not provide dynamic I/O
by the supervisor.

/RESTART AND WARM START FACILITIES FOR OS

I/O ERE routines fail in their attempt to correct
and the error is one that causes program or system
matically provided advanced checkpoint/restart
ilities of OS can be employed to minimize the impact
on system operation. The automatic restart facility
terminated programs to be rescheduled immediately
on of their job control, so that a minimum of operator
required. The operator must authorize all automatic
If a permanent I/O device or channel failure caused
tion, the device or channel can be varied offline.
llocation of a different device when the program
ed.

ilities of the control program provide automatic
and SYSOUT data sets and input and output work queues
work is not lost when a system termination occurs.
formed of the status of jobs in execution when the
and these jobs should be restarted automatically
or from a checkpoint if the type of processing
such a restart. System design should include planned
for unscheduled terminations of individual programs
(See Figure 50.10.7.)

FACILITIES FOR DOS

ped because of an I/O device or channel error or
system termination can be restarted from a checkpoint
ning of the job step if their job control is
appropriate restart control statements included.
devices can be removed from the table of available
rator, and different devices of the same type can
job steps via their job control or by the operator.
ities are not required as DOS does not build work
should plan program and system restart procedures.

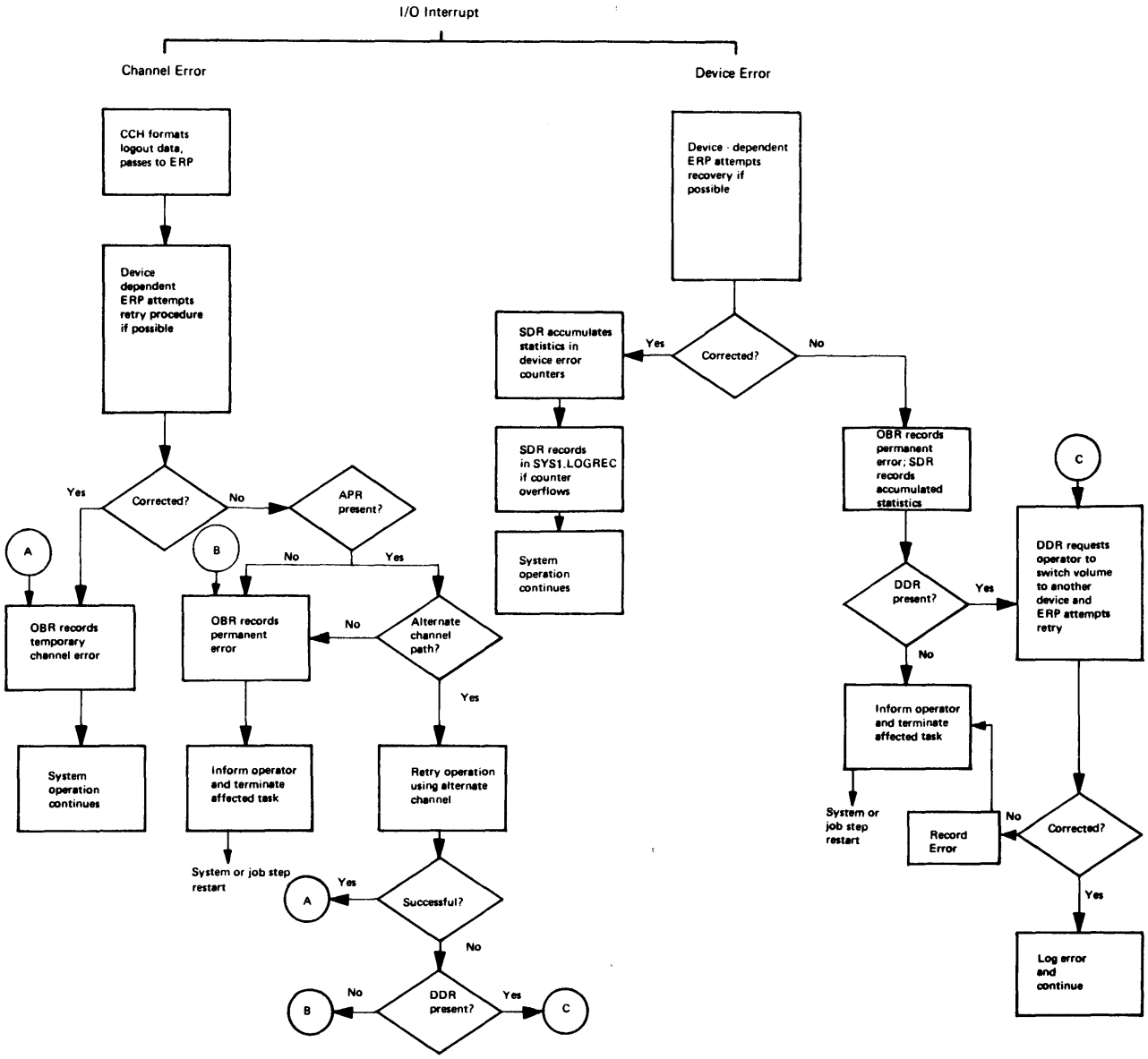


Figure 50.10.7 General flow of OS error recovery procedures after an I/O interrupt

50:15 REPAIR FEATURES

The programmed repair features supplied are designed to minimize the impact of malfunction diagnosis and repair on system availability. Fault location and repair time should be reduced by:

1. Improved error recording - Both intermittent and solid hardware and I/O errors are logged at the time of failure if Model 155 RMS routines are present. More status information will be available than was recorded previously for Models 40 and 50.

2. Online error diagnosis - Error diagnosis and repair can be performed concurrently with system operation in a multiprogramming environment to avoid total system or direct access facility unavailability.

3. CE diagnosis routines - More exacting CE diagnosis routines are available.

   The following maintenance and diagnostic routines will be provided:

   - Online Test Executive program (OLTEP) and Online Tests (OLT's) for operation under OS and DOS control to test malfunctioning I/O devices concurrently with system operation.

   - Processor Logout Analysis program for operation under OS to analyze SYS1.LOGREC MCH records to attempt to identify replaceable malfunctioning hardware components.

   - System Test and Storage Test programs for customer engineer use in identifying malfunctioning hardware units in the system (stand-alone routines).

   - Microdiagnostics for customer engineer use in diagnosing malfunctioning field-replaceable units (stand-alone routines).

OLTEP AND OLT'S - OS AND DOS

OLTEP is designed to operate as a processing program under operating system control. It handles the required interface between the operating system and the device dependent OLT's. One OLTEP will be provided for operation under OS and another for execution under DOS. These two OLTEP's support functions not provided by the currently available OS OLTEP and DOS OLTEP programs.

The inclusion of OLTEP in an operating system is automatic for a DOS control program generated for a Model 155. OLTEP is a system generation option for OS users. A stand-alone version of OLTEP, called OLTSEP, will be available as well. OLT's are obtained from the customer engineer.

OLTEP directs the selection, loading, and execution of device-dependent OLT's for the purpose of I/O device testing and error diagnosis. OLTEP is also designed to verify I/O device repairs and engineering changes.

As with any other job step, OLTEP is invoked with job control and executes with a user-assigned priority. A minimum program area of 16K is required for OLTEP operation in OS environments. DOS OLTEP operates only in the background partition in a minimum of 12K and cannot be run with a 6K supervisor. The input stream or system console device can be used to supply the parameters required for test operations - devices to be tested, options desired, etc. OS OLTEP insures the protection and security of user data files and storage in use while

OLT's are operating. OS OLTEP also insures that the devices to be tested are online or offline (as far as the operating system is concerned) as required by the particular device type.

OLTEP also has the new capability of being able to access history records describing previous I/O errors on the device being tested. In addition, multiple devices can be tested during one OLTEP execution. If a console is used to define the test run, the new prompting facility can be requested as an aid to the user supplying the definition.

OLTEP and the OLT's will reside in the DOS core image library. In OS environments portions of OLTEP will reside in both SYS1.LINKLIB and SYS1.SVCLIB while the OLT's can be placed in a user-designated disk library (partitioned data set).

OLTEP and OLT's operate concurrently with other executing jobs in a multiprogramming environment and provide online I/O device testing and repair, eliminating the necessity for complete system unavailability.

PROCESSOR LOGOUT ANALYSIS PROGRAM

This program can be run as a job under OS. It performs the following:

1. Formats and prints the machine check records written in the error log (SYS1.LOGREC)

2. Creates and maintains a logout history on a secondary data set

3. Analyzes machine check logout data records describing hardware errors and prints the location of suspected malfunctioning replaceable units. The history logout data set can be used in this analysis in an attempt to gain better resolution of the malfunctioning replaceable units.

Since the Logout Analysis program operates under operating system control, it can be run concurrently with other operating jobs in a multiprogramming environment and can be run periodically by the operator when the error log becomes full. It will be used by the customer engineer during scheduled preventive maintenance periods to locate units responsible for intermittent hardware failures.

SYSTEM TEST AND STORAGE TEST PROGRAMS

The System Test and Storage Test programs are stand-alone, model-dependent, diagnostic routines for customer engineer use that reside on magnetic disk cartridges. The System Test performs a functional test of the hardware system components, including the CPU, all channels, and most locally attached I/O devices. The 2701, 2702, and 2703 communication control units are supported in wrap or diagnostic mode only (no outboard operations to remote terminals). The Storage Test performs a functional test of processor storage, buffer storage, and the buffer directory. These routines can be used for the following purposes:

1. To locate a malfunctioning unit in the system. (The specific error component within the unit is not identified.)

2. To determine a working hardware configuration prior to a system IPL

3. To verify correct system operation after a malfunctioning unit has been repaired

These diagnostic tests are designed for simplicity of operation. They are loaded from the device under the console reading board and use the system console for communication purposes. Users can also run these tests at appropriate times, for example, prior to IPLing the system for an extended period of online operation.

MICRODIAGNOSTICS

Microdiagnostics are a set of stand-alone, high-resolution, fault-locating tests that will be contained on several magnetic disk cartridges. They are to be used by customer engineers to locate malfunctioning field-replaceable units when a solid hardware error exists. These tests are designed to reduce the amount of time required to locate malfunctioning cards once the unit containing the solid error has been identified.

50:20 RAS SUMMARY

The degree to which an installation benefits from available RAS features depends in part upon their proper implementation. It is desirable for Model 155 users to design a system that includes RAS features and to become involved in the implementation and use of maintenance procedures and aids. Specifically, the user can:

- Include OLTEP and OLT's in his operating system (optional for OS users)
- Train operators to run the System Test, the Storage Test, and the Processor Logout Analysis program. The conditions under which these programs should be run should be determined jointly by the user and the customer engineer.
- Plan system and program recovery procedures (use of checkpoint/restart and warm start facilities)
- Have operating personnel perform normal hardware maintenance procedures, such as the periodic cleaning of tape drive heads. Proper system hygiene should be maintained, in general.
- Implement an effective program of operator training so that the number of system malfunctions that occur because of operator error is reduced

SECTION 60: PROGRAMMING SYSTEMS PREINSTALLATION PLANNING

Because extensive hardware and programming systems compatibility exists between the System/370 Model 155 and System/360 models, most Model 40 and 50 users can upgrade to a Model 155 with a minimum of effort. This is also true for users of ASP (Attached Support Processor) who wish to upgrade a Model 40 or 50 support processor to a Model 155. Essentially, no more effort may be involved in the Model 155 installation process for OS MFT and MVT and DOS users than is required currently to change from one operating system release to another, or to regenerate an operating system to include new hardware, new I/O devices, and more control program options.

It may also be desirable to expand the design of the system - add new applications, use additional features, etc., as a result of a sizable upgrade in the hardware configuration. In most cases, the fact that an OS MFT or MVT or DOS user is upgrading to a System/370 Model 155 should not add to the effort that would be required if these system changes were to be implemented for a Model 40 or 50 upgrade to another System/360.

60:05 OS MFT AND MVT TRANSITION

A system generation must be performed using an OS release that includes Model 155 support in order to obtain an operating system designed to support new Model 155 features. The existing system generation job stream can be used, with the following modifications as appropriate:

- Direct access space allocation for operating system data sets will have to be adjusted as indicated in the IBM System/360 Operating System, System Generation Manual (GC28-6554). If a 3330 or a 2305 facility is to be used as a system residence device, UNIT parameters in job control statements must be changed where necessary.

- Stage I input must be modified to reflect the Model 155 configuration, including the presence of any new I/O devices or features, such as the 3211 Printer, the 3330 facility, the 2305 facility, integrated emulator programs, etc. Other control program options can be included, such as I/O RMS, OLTEP, and performance improvement features.

- FCB and UCB images should be added to SYS1.SVCLIB if a 3211 Printer is included in the configuration. User-written output writer procedures should be modified to include these specifications.

An OS MFT or MVT operating system generated for the Model 155 includes the following:

- A nucleus designed to operate in the fixed storage area of the Model 155. RMS routines (MCH and CCH) are included that support the expanded machine check interrupt. OBR and SDR are present also.

- Control program support of block multiplexing and rotational position sensing, as discussed in Section 30, if requested

- Support of user-specified new I/O devices and Model 155 operator consoles, including a remote 3210 Console printer-keyboard as an alternate or additional console

- Support of the interval timer and time of day clock
- Support of the new instructions by Assembler F
- The required interface to the integrated emulator program specified at system generation, if any

If integrated emulator programs are to be used, the steps outlined in Section 40 must be taken in order to convert from a 1400/7010 system or current stand-alone emulation procedures.

EXISTING OS PROCESSING PROGRAMS AND JOB CONTROL

IBM-supplied OS program products and Type I processing programs (language translators, utilities, etc.) will run on the System/370 Model 155 without alteration. Subject to the exceptions stated in Section 10:05, user-written OS processing programs that operate on Models 40 and 50 will also execute correctly on the Model 155. Modification and reassembly of existing user-written OS processing programs is not required unless new processing is to be added or existing processing is to be altered. Modification of the job control for these processing programs is required if I/O device type is changed, say from 1403 to 3211, if direct access space allocation changes, if a DCB parameter is to be altered, etc. I/O device type changes do not necessitate processing program alterations unless device-dependent macros have been used, data organization is changed, or a DCB parameter that is specified in a program is to be changed.

CONVERSION TO 3330 AND 2305 FACILITIES

Conversion from current direct access devices to the 3330 facility involves the same procedures as are required now to change from one disk device to another, say from 2311s to a 2314. Existing disk data sets can be placed on 3336 disk packs, using an IBM-supplied utility in most cases. Assuming that data organization is not changed, consideration should be given to altering the block size used and the amount of space allocated to the data set. The location and size of each type area in an ISAM data set should be altered, taking into account 3336 disk pack characteristics. These changes can be made in job control statements.

Sequentially organized data sets (processed by QSAM or BSAM) and partitioned data sets can be copied from the source direct access device directly to the 3330 facility, using the OS IEHMOVE utility. Or they can be copied to tape and then to the 3330 facility, using the same utility (if the source direct access device type is not present in the Model 155 configuration).

Indexed sequential data sets can be copied directly from the source direct access device to the 3330 facility, using the IEBISAM utility. Alternately, they can be unloaded to tape and then reloaded, using the same utility. Changes to space allocation, etc., can be made via job control statements.

Direct organization (BDAM) data sets can be copied on a track-to-track basis from the source direct access device to the 3330 facility, using IEHMOVE or copied to tape and then to the 3330 facility. If more records are to be placed on a 3330 track than are on a source device track, the existing reorganization program can be used to transfer the data to the 3330 facility, and the program may have to be changed. Reprogramming of the randomizing routine used in the reorganization, and in all processing programs that access the BDAM data set, is necessary if a relative track or actual address reference

is used and fewer (or more) 3330 tracks are allocated to the data set than before.

Subject to the restrictions stated in Section 10:05 and those indicated for BDAM data sets, existing executable processing programs can be used without change to process data sets that have been transferred to 3336 packs. Nothing need be done to job control for these programs if the cataloged procedures supplied with the language translators are used, as long as the 3330 facility is specified as a SYSDA device at system generation. Otherwise, job control statements must be changed to request 3330 devices and, optionally, any data set characteristic changes, such as block size. RPS support, as described previously, is provided automatically.

User-written programs that use the EXCP level to access disk data sets that have been transferred to 3336 packs may have to be modified to reflect the characteristics of the data set on the 3336, a different number of records per track, a different number of tracks per cylinder, etc. All 2311 and 2314 CCW lists will operate on 3330 facilities except those that are device or channel time dependent and those that support the file scan feature, which is not available on the 3330 facility. User-written 2311 or 2314 error routines will not execute correctly and must be modified. RPS commands have to be added by the user if this support is desired for programs that use EXCP. (Note that the XDAP macro will include support of RPS commands.)

Data sets currently located on 2303 Drum Storage can be placed on a 2305 facility, using a data set utility program. Unit specification in the job control statements of existing programs that will access the 2305 facility, instead of the 2303 drum, must be changed. Also, to reflect the larger capacity of a 2305 track, it may be necessary to alter the block size used. The latter also can be done via job control statement alterations (without program reassembly) unless block size was specified in the program itself.

CONVERSION TO THE 3803/3420 MAGNETIC TAPE SUBSYSTEM

As stated in Section 20:25, existing tape processing programs and their job control statements and tape volumes need not be modified in order to be used with 3803/3420 subsystems with equivalent features whenever the same recording modes are used.

Whenever possible, seven- and nine-track NRZI mode tape volumes should be converted to 1600-BPI PE format to obtain the benefits of the higher density and the PE recording technique. In cases in which tape volumes must retain seven-track NRZI format, for interchange with other systems for example, use of the 3803/3420 subsystem offers improved tape reliability and subsystem serviceability as already discussed.

Conversion of seven- and nine-track NRZI tape volumes can be done gradually during production processing. That is, the old master input tape volume is read in on a 3420 tape unit with the appropriate compatibility (Dual Density or Seven-Track) feature while the new master output tape is written on a 3420 tape unit in 1600-BPI PE format. Existing programs that process these converted tapes need not be modified unless an altered characteristic (recording mode or block size, for example) is specified in the program DCB. Existing job control for these programs must be altered to request a tape unit with the new recording characteristics and, if desired, to change existing DCB parameters such as block size, number of buffers, etc.

Tapes that cannot be converted on an as-used basis, such as program tapes of active reference tapes that are not rewritten when processed, can be converted by using a copy utility.

60:10 PLANNING OPTIMAL SYSTEM PERFORMANCE, USING BLOCK MULTIPLEXER CHANNELS AND ROTATIONAL POSITION SENSING DEVICES

Block multiplexing, rotational position sensing, and multiple requesting provide the user with another tool that can improve total system throughput in the area of multiprogramming. However, the effectiveness of this tool for a given installation depends largely on proper planning for its use. This section indicates how to use block multiplexer channels and RPS devices more effectively.

The guidelines outlined indicate how best to configure a system with rotational position sensing devices, how to plan job scheduling, and what to consider when determining disk data set characteristics. Explanations follow the statement of each guideline.

All guidelines presented are not necessarily practical for all users. Each item should be evaluated in terms of the processing requirements and hardware configuration of an installation.

SYSTEM CONFIGURATION AND GENERATION

Guidelines for system configuration and generation are as follows:

1. Multiple 3330 facilities should be placed on a single block multiplexer channel.

   Performance improvement occurs (1) as a result of overlapping the rotational positioning time of disk devices and (2) because more I/O requests can be initiated in a given period of time, since the channel is free more often. When many disk devices are active concurrently on a block multiplexer channel, there is more potential for such overlap.

2. Direct access devices with RPS should be placed on separate channels from I/O devices without RPS. Alternatives are as follows:

   a. If it is necessary to place non-RPS devices on the same block multiplexer channel with RPS devices, give first choice to non-RPS devices with a buffered control unit, such as the 2540 Card Read Punch and the 1403 Printer. These devices disconnect from a block multiplexer channel during the relatively long mechanical portion of their cycle, thereby freeing the channel for other operations.

   b. Tape units should not be placed on a block multiplexer channel with RPS devices unless absolutely necessary, because channel disconnection does not occur during any of their channel operations. If this is not possible, try to plan job scheduling to avoid having jobs using tape units and jobs using RPS support active on a block multiplexer channel at the same time. If this is not feasible, try to assign very low-activity data sets to these tape units.

   A device without channel disconnect capability can monopolize the block multiplexer channel for relatively long periods of time, thereby preventing (1) the initiation of other I/O operations on the channel and (2) the reconnection and completion of disk RPS channel programs already in operation on the channel. For example, a direct access device without RPS retains use of the channel during its search operations as well as during its reads and writes. If the device is a 2314 and block size is half a track, the channel is busy for 25 ms on the average (12.5 ms average rotational delay plus 12.5 ms read/write) for each I/O operation started for the non-RPS 2314 facility. Even

if the block size used is relatively small, the channel can still be monopolized by the non-RPS device if there is high activity on the device.

3. The 2305 facility normally should not be placed on a block multiplexer channel with any other device.

   Exclusive use of a channel insures optimum performance of the 2305 facility as a system residence device.

The following should be noted as regards specification of priority and ordered-seek I/O request queuing options for RPS devices at OS system generation. The priority queuing option insures priority I/O request initiation for the device, but because of first-come, first-served handling of I/O operations on the block multiplexer channel, this option does not insure that priority device channel programs will complete sooner than other RPS channel programs that were started later on the channel. However, the objective of specifying the ordered-seek

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queuing option (minimization of arm movement on a disk drive) can still be achieved when using RPS.

JOB SCHEDULING

Guidelines for job scheduling on the System/370 Model 155 are:

1. If total system throughput improvement, rather than maximum individual job performance increase, is the objective, schedule jobs that use RPS together such that the maximum number of RPS devices are active concurrently on each block multiplexer channel.

   Greater overlap potential exists when more RPS devices are active concurrently on a block multiplexer channel. (See item 1 under "System Configuration and Generation".)

2. When jobs that use disk data management functions with RPS support are executed concurrently with jobs that do not use RPS support, the devices assigned to the former should be on different channels from devices assigned to the latter.

   Alternately, if jobs using RPS and jobs not using RPS must access devices on the same block multiplexer channel concurrently, the jobs without RPS support should have high seek activity such that search and read/write time is small compared to seek time.

   Assume sequentially organized data sets and TCAM message queues are allocated to the same 3330 facility on a block multiplexer channel. A QSAM job step and a TCAM job step are executing and access the 3330 facility data sets concurrently. Since RPS commands are not used for TCAM message queue processing, each 3330 disk drive containing TCAM message queues acts like a non-RPS device and can monopolize channel time. Thus, the job steps that use QSAM can be delayed. (See item 2 under "System Configuration and Generation".)

3. Allocate a data set that will be accessed using QSAM or BSAM chained scheduling to a device on a channel without active RPS jobs.

   The chained scheduling technique is designed to keep a device active as long as record processing keeps up with record reading or writing. Thus, the channel can be kept busy for long durations, preventing the execution of any other I/O operation on the channel. Note that while QSAM and BSAM support concurrent use of RPS and chained scheduling for access to a disk data set, the performance attained by using chained scheduling alone will not be improved significantly by using RPS as well.

4. When data sets are being processed by an RPS access method in a multiprogramming or multitasking environment and disk device assignment is handled by the user rather than by the control program, allocate as many separate RPS devices as is practical.

   This approach allows the possibility of having more concurrent operations on these data sets and therefore more seek and rotational positioning overlap.

5. If a response-oriented RPS job operates on a block multiplexer channel concurrently with other RPS jobs, job scheduling should insure that the number of jobs executing simultaneously is such

that the performance desired for the response-oriented job can be attained.

The performance of a block multiplexer channel is affected by the percentage of time the channel is busy searching and reading. The read or write of a particular record may be delayed one rotation because the channel is busy servicing another channel program. The probability of a particular record being delayed is a function of the percentage of channel busy time. As block multiplexer channel utilization increases, the probability that individual channel programs will be delayed increases. It is theoretically possible for the read or write of a particular record to be delayed indefinitely because the block multiplexer channel is busy searching for and reading other records. That is, utilization of more and more block multiplexer channel time will normally result in better overall performance, but will increase the likelihood of delayed response from any one data set.

DATA MANAGEMENT PARAMETERS

1. When organizing direct data sets to be processed using BDAM, use fixed-length standard records and a record reference that includes ID (relative block, relative track and ID, or actual address).

   RPS is supported only for fixed-length standard and VBS formats without key reference because record position must be known in order to calculate the sector number required for positioning. However, if a key reference or a variable record format is used, RPS support is provided for write verification and update (after retrieval) operations.

2. Use a large block size for sequentially processed data sets whenever possible, subject to the availability of processor storage for buffers.

   The use of RPS can provide performance gains for both short and long disk record blocks. However, use of large rather than short blocks reduces the total time required to read or write a given data set because less disk space is required and fewer I/O operations are necessary. Note also that total throughput for a given block multiplexer channel is improved by using blocks of equal (or nearly equal) size for all data sets being processed on the channel.

3. Use fixed standard records for QSAM and BSAM data sets where possible.

   The channel programs used for fixed standard records free the channel more often than when other record formats are used. A search for the previously read record is not used in order to locate the next sequential record when fixed standard records are read sequentially. The sector number of the next sequential record is obtained by including a READ SECTOR command at the end of the channel program used to read each record. Therefore, the SEARCH command specifies the ID of the desired record and the channel is free during the time it would otherwise have been busy searching for the previously read record.

   Channel time is reduced when writing fixed standard records because the operation required to calculate the remaining number of bytes on a track after each write is eliminated. (Note that

the disk control unit is still busy erasing to end of track after formatting write operations even though the channel is freed after the data record has been written.)

4. Use multiple buffers with QSAM and BSAM.

   The availability of multiple buffers per data set lowers the probability that a task will have to wait for a particular record. QSAM is designed to initiate an I/O request whenever a buffer becomes available, thus keeping the channel queue as full as possible. When BSAM is used, the programmer must handle the initiation of I/O requests.

The following summarizes the advantages of rotational position sensing, multiple requesting, and block multiplexing.

- System throughput increases can be achieved when multiple sequential data sets are processed concurrently on a single block multiplexer channel (using QSAM, QISAM, or BSAM) because a higher effective channel data rate results.

- The number of block multiplexer channels required in a given system configuration can be fewer than the number of selector channels that would be required to handle the same amount of data, because more effective channel utilization is achieved by block multiplexing disk operations.

- The performance cost to an installation of verifying disk write operations is sharply reduced.

- The greatest throughput improvement results from use of rotational position sensing with high-activity, transaction-based processing, that is, with applications that include one or more large jobs that:

  1. Use direct processing (BDAM) with fixed-length standard or VBS records and a record reference that includes ID

  2. Require a multiple volume data base of small records

  3. Process many additions and updates and use write verify

60:15 OS PORTABILITY

To avoid multiple system generations, an OS user with multiple Model 155 systems may wish to generate a single operating system that can be used on every Model 155 in the installation. This is possible under the same system hardware and I/O device configuration restraints that exist for System/360 models. During the IPL procedure, channels and I/O devices may have to be varied offline, partition sizes may have to be redefined, etc., when the operating system is used with a different configuration than was specified during system generation.

A user with both a System/370 Model 155 and a System/370 Model 165 or a System/360 model in an installation may also wish to generate one operating system that can be used on both models. This approach provides backup when one system is unavailable and can eliminate the necessity of multiple generations.

Portability of an OS operating system between a Model 155 and a Model 165 or a System/360 model, say 40, 50, or 65, can be achieved by utilizing a multiple nucleus control program under the following general conditions:

1. The system hardware and I/O device configuration of both systems must be similar. For example, a Model 155 OS control program generated to support block multiplexing mode and RPS direct access devices cannot be executed on a system without such channels and devices.

2. The same control program, MFT or MVT, must be used for both systems.

3. Consideration should be given to the processor storage sizes of the two models when determining the size of the scheduler, language translators, and the linkage editor(s) included in the generated system.

4. Processing programs that are to run on both models must use instructions and features common to both systems. An Assembler Language program that uses the new general purpose instructions for the Model 155 or byte orientation can be executed on a Model 165 but not on Models 40, 50, or 65.

In order to generate an operating system that is portable between the Model 155 and the Model 165, 40, 50, or 65, the following steps are required:

1. A complete system generation must be performed to generate an operating system for the Model 155. The IPL-time system/operator communication option must be requested so that options specified can be altered during IPL.

2. A nucleus generation should then be done for the alternate system. The model number specified (in the SUPRVSOR, SECMODS, CENPROCS macros, etc.) will be that of the alternate system, not the Model 155.

3. Additional link-edits must be performed to add model-dependent routines to the generated multiple nucleus operating system. Specifically, MCH or SER and EREP model-dependent routines for the secondary system must be included, as appropriate.

4. If extended precision floating-point divide is used in processing programs, the following steps should be taken. SYS1.LINKLIB contains two divide simulation routines. One uses extended precision hardware, the other does not. When a full generation is performed for the Model 155, a calling mechanism is set to request the divide routine that uses extended precision instructions at execution time, since the Model 155 contains these instructions.

   Therefore, the divide simulation routine that does not use extended precision should be transferred from SYS1.LINKLIB to another library and given the same member name as the divide routine with extended precision instructions. When the operating system is executed on a Model 155, SYS1.LINKLIB should be used by extended precision programs. When the operating system is executed on a Model 40, 50, or 65, the alternate library should be used.

Whenever a new program that is to execute on both systems is added to a library or if the Model 155 hardware configuration changes, the user must consider whether or not portability is affected.

60:20 DOS TRANSITION

A system generation must be performed using a release of DOS that includes Model 155 support in order to obtain a supervisor that supports new Model 155 features. The existing system generation job stream can be used, modified to reflect the Model 155 hardware configuration and the use of integrated emulator programs, as appropriate. Additional supervisor options can be selected as well.

A DOS operating system generated for the Model 155 includes the following:

- MCAR and CCH routines to handle the expanded machine check interrupt. OBR and SDR are included to handle I/O error recording, and OLTEP is present also.
- Support of the new I/O devices specified (3211 Printer and 3803/3420 tape subsystem) and the new Model 155 console specified
- Support of the interval timer, if requested
- Support of the new instructions by Assembler D
- The required interface to the integrated emulator program specified at system generation, if any

In general, the new supervisor will be larger than the one currently in use because of the automatic inclusion of MCAR, CCH, OBR, and SDR routines and user selection of additional options. (The minimum DOS supervisor size for the Model 155 is 14K.) This increase will be less for DOS supervisors that currently contain the optional MCRR, OBR, and SDR routines. A larger supervisor and the availability of additional processor storage in the Model 155 will cause partition starting addresses to change. Therefore, existing user-written, nonrelocatable DOS programs have to be link-edited relative to the new partition starting addresses and placed in the new core image library. If relocatable modules for these nonrelocatable programs are not available, reassembly of the source modules, as well as link editing of the resulting relocatable modules, is required. Existing user-written, self-relocatable DOS program phases can be copied directly from the old core image library to the new one.

Subject to the restrictions stated in Section 10:15, alteration of an existing source program is required only if new processing is added, if existing processing is changed, if there is a change in the I/O device types used in the program (ASSGN job control statements may also require changes), or if the program contains a user-written routine that depends upon a particular release of DOS for communication with the supervisor. (Conversion of emulated programs and files was discussed in Section 40.)

The OS discussion of conversion of existing tape programs and their job control statements and existing tape volumes for use with a 3803/3420 tape subsystem applies to DOS also except that a change in a parameter, such as blocking factor, involves alteration of the program (tape DTF). In addition, recording mode changes involve job control (ASSGN) statement alteration only (not DTF modification).

60:25 DOS PORTABILITY

A DOS user with multiple Model 155 systems can generate a single operating system that can be used on each system, subject to restraints imposed by differences in hardware configurations. If a single control program is to be used for both a System/370 Model 155 and a System/360 model, say 40 or 50, Model 155 should be specified at system generation time so that MCAR and CCH are included. (DOS support is not provided for the System/370 Model 165.)

Model 155 MCAR and CCH routines will not execute properly on a Model 40 or 50. When a DOS supervisor containing them is loaded during IPL, MCAR and CCH are disabled automatically by the initialization routine when the routine determines that it is not operating on a Model 155. (Note that MCAR and CCH cannot be disabled by the operator with the RF parameter when a DOS supervisor containing them operates on a Model 155.) This means that the Model 40 or 50 will run as it would if the optional MCRR routine was not included in the supervisor. That is, there will not be any machine check error recording and the system will go into a wait state when a machine check interrupt occurs. Thus, if the facilities provided by MCRR routines are desired for a Model 40 or 50 supervisor, a system generation must be done for each unique model in the installation so that the appropriate model-dependent machine check routine is included in each supervisor.

As covered in the OS portability discussion, processing programs that are to execute on the Model 155 and a Model 40 or 50 must use instructions, features, and I/O devices common to both systems.

60:30 USE OF OTHER PROGRAMMING SYSTEMS

Subject to the restrictions stated in Section 10:05, users of OS PCP, TOS, BOS, non-IBM supplied control programs, or OS MFT and MVT and DOS control programs not generated for a Model 155 can execute their existing control and processing programs on a Model 155 with a hardware and I/O device configuration comparable to that of the System/360 model now installed. (Certain BPS programs have known timing dependencies that prevent their successful execution on a Model 155.) However, since Model 155 RMS (machine check and channel check routines) are not included in these control programs, the Model 155 will operate under the following conditions:

1. Single-bit processor storage error correction and deletion of malfunctioning buffer block occur; however, they do not cause a machine check interrupt (IPL disables the recovery mask bit).

2. The IPL setting of the recovery mask bit also disables CPU retry correction interrupts. However, the CPU retry facility itself is disabled if a switch on the console (discussed below) is in a certain position.

3. External damage and damage to the time of day clock or the interval timer causes a machine check interrupt condition.

4. A hard machine check error (an unretryable or uncorrectable CPU error, a double- or multiple-bit processor storage error, or a storage protection failure) causes a hard machine check condition and generation of CPU extended logout data.

A machine check control switch, which determines what action is taken when a machine check condition occurs, is present on the system console. When the switch is not in the hard stop position, machine checks cause an interrupt and logout if they are not disabled. This setting is to be used when an operating system containing Model 155 RMS is in operation. When the switch is in the hard stop position, all enabled machine check interrupts cause a hard stop without an interrupt or a logout. In addition, CPU retry is effectively disabled, since detection of a CPU error causes a hard stop before CPU retry is attempted.

If the Model 155 is not set to hard stop after a machine check when an operating system without Model 155 RMS is used, the system takes whatever action was planned for machine checks:

- Any control program without a recovery routine included (for example, SER0, SER1, MCH for OS or MCRR for DOS) will enter the wait state after a machine check interrupt and logout. The logged

data can be printed on the console (using display mode) or printed out with a stand-alone processor storage dump program. The operator can re-IPL and attempt to continue operations or the CE can perform diagnostic procedures.

- Any control program that contains a recovery routine will enter the routine and attempt execution. As stated in Section 10:05, these routines access model-dependent data and will not operate correctly. In addition, the CPU extended logout data stored when the interrupt occurred will have destroyed the code located in locations 512 to 1151. Results are unpredictable.

Therefore, control programs containing non-Model 155 recovery routines should be run with the system set to hard stop on machine checks. After a machine check condition occurs in this situation, the logout data generated is not in processor storage, but is contained in a buffer area in the CPU and can be placed in processor storage by execution of the DIAGNOSE instruction. A stand-alone log dump program, which can be executed to dump the logout to processor storage and write it on a tape, will be available (provided on a magnetic disk cartridge). The data will be written in a form suitable for processing by the Processor Logout Analysis program to obtain hard copy. The operator can re-IPL and attempt to continue operations or the CE can perform diagnostic procedures.

For the following reasons, it is advantageous for Model 155 users to install an operating system that includes recovery management support designed specifically for the Model 155:

- The number of re-IPLs necessary because of machine malfunctions can be reduced. Most hardware errors can be corrected either by Model 155 hardware recovery procedures or RMS routines. The latter insures the continuation of system operation whenever possible if the error cannot be corrected. This is particularly important during online operations. In Model 155 systems without RMS hardware, errors other than single-bit processor storage errors will necessitate a re-IPL.

- Status information recorded by RMS routines will assist the customer engineer in the diagnosis of machine malfunctions. This data will be of greatest benefit in diagnosing intermittent errors.

- Versions of OS control programs that include Model 155 RMS are the only ones that include support of new Model 155 CPU features, channels, direct access devices, and integrated emulators.

- DOS users who install a DOS supervisor that includes Model 155 RMS will also have the advantages of integrated emulation. (CS/30 and CS/40 cannot be executed on a Model 155.)

SECTION 70: COMPARISON TABLE OF HARDWARE FEATURES AND PROGRAMMING SUPPORT - SYSTEM/360 MODELS 40 AND 50 AND SYSTEM/370 MODEL 155

This table has been included for quick reference. It compares the hardware features of Models 40, 50, and 155. It also indicates DOS and OS support of Model 155 features. A dash (-) in a programming system column indicates that the hardware feature does not require programmed support.

Hardware Feature	System/360 Model 40	System/360 Model 50	System/370 Model 155	DOS - Model 155	OS - Model 155
I. CPU					
A. Internal Performance (relative to Model 50)	.44	1	Approximately 3.5 to 4	-	-
B. Instruction set					
1. Standard set (Binary Arithmetic)	Standard	Standard	Standard	All languages	All languages
2. Decimal arithmetic	Optional	Standard	Standard	All languages except FORTRAN	All languages except FORTRAN
3. Floating-point arithmetic	Optional	Standard	Standard	All languages except RPG	All languages except RPG
4. Extended precision floating-point	Not available	Not available	Optional	Mnemonics in Assembler D	Assemblers F and H, PL/I Optimizing & FORTRAN H
5. Six new instructions (MOVE LONG, COMPARE LONG, etc.)	Not available	Not available	Standard	Mnemonics supplied for user use in Assembler D	Mnemonics supplied for user use in Assemblers F and H
6. STORE CPU ID, STORE CHANNEL ID, HALT DEVICE instructions	Not available	Not available	Standard	Used by the control program	Used by the control program
C. Buffered instruction fetch	No	No	Yes Three one-word buffers are provided. (Imprecise interrupts do not occur.) One prefetched instruction decoded, no operand prefetching.	-	-
D. Interval timer	Standard (16.6 ms resolution)	Standard (16.6 ms resolution)	Standard (3.33 ms resolution)	1. Time intervals 2. Time of day	Supported except for time of day requests
E. Time of day clock	Not available	Not available	Standard	Not supported	Supported for time of day requests
F. CPU retry by hardware	No	No	Standard	Both successful and unsuccessful hardware retries logged by MCAR	Both successful and unsuccessful hardware retries logged by MCH

Page of GC20-1729-0
Revised 7/14/70
By TNL GN20-2226

Hardware Feature	System/360 Model 40	System/360 Model 50	System/370 Model 155	DOS - Model 155	OS - Model 155
G. Machine check interrupt	Occurs on CPU, main storage, and certain channel errors. One mask bit controls this interrupt.	Same as the Model 40	Occurs after corrected and uncorrected errors. There are seven types of machine check and many are individually maskable.	Soft and hard machine checks are logged. Recovery procedures are performed.	Same as DOS with some differences in recovery procedures performed.
H. Fixed storage area size in lower storage (including logout area for machine and channel errors)	324 bytes	292 bytes	1152 bytes reducible to 512 if the extended logout area of 640 bytes is moved	Data logged is handled by RMS routines	Data logged is handled by RMS routines
I. Compatibility features (all are optional)	1.1401/1460 2.1410/7010 3.1401/1440/1460 DOS Compatibility (for use with CS/40)	1.1410/7010 2.7070/7074 (mutually exclusive features)	1.1401/40/60, 1410/7010 2.OS/DOS compatibility	1. 1401/1440/1460 and 1410/7010 integrated emulator programs provided -	1. Same as DOS 2. An OS DOS emulator is provided
J. CPU cycle time	625 nanoseconds 2-byte parallel data flow	500 nanoseconds 4-byte parallel data flow	115 nanoseconds 4-byte parallel data flow	-	-
K. Control logic	microprogram in tape ROS	microprogram in capacitor ROS	microprogram in capacitor ROS	-	-
L. Direct Control feature	Optional	Optional	Optional	Not supported	Not supported
II. STORAGE					
A. Processor (main) storage sizes	16K 32K 64K 128K 192K 256K	- - 64K 128K - 256K 384K 512K	- - - - - 256K 384K 512K 768K 1024K 1536K 2048K	All are supported	All are supported

Hardware Feature	System/360 Model 40	System/360 Model 50	System/370 Model 155	DOS - Model 155	OS - Model 155
B. Processor storage cycle in micro-seconds	2.5 for 2 bytes	2 for 4 bytes	2.1 for 16 bytes	-	-
1. CPU fetch from storage in micro-seconds (no channel interference)	1.5 for 2 bytes	1.0 for 4 bytes	1.49 for 4 bytes 1.61 for 8 bytes 1.96 for 16 bytes	-	-
C. High-speed buffer storage	No	No	One 8K buffer is standard	-	-
1. CPU fetch from buffer	-	-	230 ns for 4 bytes 345 ns for 8 bytes		
D. Processor storage validity checking	Parity checking on each byte - errors are not corrected by hardware.	Same as Model 40	ECC checking on a doubleword. Single-bit errors are corrected by hardware.	Corrected single-bit and uncorrected storage errors are logged by MCAR.	MCH logs errors as does DOS. Control program routines are refreshed if possible when double- or multiple-bit errors occur.
E. Byte boundary alignment (nonpriviledged operands)	No	No	Standard	Programmers can use the byte alignment hardware facility in Assembler programs.	Programmers can use the byte alignment hardware facility in Assembler programs.
F. Storage and fetch protection	Storage protect is optional. Fetch protect is not available.	Storage protect is standard and fetch protect is not available.	Standard	Storage protect is supported.	Storage protect is supported.
G. Shared processor storage	Not available	Optional (Model 50 system shares 2361 Core Storage with a Model 50, 65, or 75.)	Not available	-	-
H. 2361 Core Storage	Cannot be attached	Can be attached	Cannot be attached	-	

Hardware Feature	System/360 Model 40	System/360 Model 50	System/370 Model 155	DOS - Model 155	OS - Model 155
III. CHANNELS					
A. Byte multiplexer channel 0 - up to 8 control units	Standard	Standard	Standard	Supported	Supported
1. Subchannels available	16-128	16-128 (256 is an option)	Up to 256	Up to 256 subchannels are supported.	Up to 256 subchannels are supported.
2. Burst mode locks out CPU	Yes	No	No	-	-
B. Second byte multiplexer (channel 4)	No	No	Optional for systems with 768K or more and channel 3 installed	Not supported	Up to 256 subchannels supported for a total of 512 in the system.
C. Block multiplexer channels (up to 8 control units)	Not available	Not available	1 and 2 Standard. 3-5 optional. Channel 4 cannot be installed if the second byte multiplexer is present.	Not supported	Supported
1. Maximum individual channel data rate	312KB	800KB	1.5 MB	-	-
D. Selector channels	Optional 0-2	Optional 0-3	Selector mode standard for all installed block multiplexer channels. 1 and 2 standard. 3-5 optional.	Supported	Supported
E. Channel retry data in an ECSW after channel error	No	No	Yes	CCH routine passes ECSW data to ERP to perform a retry of failing I/O operation	Same as DOS
F. Channel-to-channel adapter	Optional	Optional	Optional	-	-

Hardware Feature	System/360 Model 40	System/360 Model 50	System/370 Model 155	DOS - Model 155	OS - Model 155
IV. OPERATOR CONSOLE DEVICES	1. 1052 M7 Printer-Keyboard 15 cps (No alter/display mode	1. Same as Model 40	1. 3210 Console Printer-Keyboard with alter/display mode (15 cps)	Supported	Supported as the primary or an alternate console.
	2. Additional consoles, such as graphic units, optional	2. Same as Model 40	2. 3215 Console Printer-Keyboard with alter/display mode (85 cps)	Supported	Supported as above
		3. Remote 2150 console with operator control panel and/or 1052 M7 is optional	3. Optional 3210 Console Printer-Keyboard remote with either (1) or (2) - no alter/display	Not supported	Supported as an alternate or an additional console.
		4. Remote 2250 Display Unit containing operator control panel is optional	4. 2150 Console with 1052 M7 Printer-Keyboard is optional	Not supported	Supported as above
			5. Additional consoles, such as graphic units are optional	Not supported	Supported as additional consoles by MCS and DIDOCS options.
V. I/O DEVICES					
A. 3211 Printer with tapeless carriage, UCS, and 18 additional print positions	Yes	Yes	Yes	Supported	Supported
B. 3803/3420 Magnetic Tape Subsystem	Yes except Model 7. Model 5 cannot be attached to the byte multiplexer channel.	Yes	Yes	Supported	Supported
C. Other tape drives currently announced	All except 2420 Model 7	Yes	Yes	Supported	Supported

Page of GC20-1729-0
Revised 11/20/70
By TNL GN20-2276

Hardware Feature	System/360 Model 40	System/360 Model 50	System/370 Model 155	DOS - Model 155	OS - Model 155
D. Direct access devices (2311,2314,2303,2301, and 2321)	All except 2301 drum	All except 2301 drum	All except 2301 drum	2303 and 2301 drums are not supported.	All are supported except 2301 drum
E. 3330 facility with RPS and multiple requesting	No	No	Yes on block multiplexer channels	Not supported	Supported
F. 2305 facility Model 2 with RPS and multiple requesting	No	No	Two on channel 1 and two on channel 2	Not supported	Supported
G. Other devices: 1231,1259 M2,1285, 1404,1418,1428,1827, 2301,2302,7340,7772, 1052 M7 except with 2150 Console	Yes except 2301	Yes except 2301	No	-	-

INDEX

Systems

A Guide to the IBM System/370 Model 155

This guide presents hardware, programming systems, and other pertinent information about the IBM System/370 Model 155 that describes its significant new features and advantages. Its contents are intended to acquaint the reader with the Model 155 and to be of benefit in planning for its installation.

IBM

PREFACE

It is assumed that the reader of this document is familiar with System/360. The reader should have general knowledge of System/360 architecture, channels, I/O devices, and programming systems support. This guide highlights only those Model 155 hardware, I/O, and programming systems features that are different from those of System/360 models and discusses their significance. Additional, more detailed information regarding System/370 Model 155 hardware and programming systems support can be found in the following SRL publications.

IBM System/370 Model 155 Functional Characteristics (GA22-6942)

IBM System/370 Model 155 Channel Characteristics (GA22-6962)

IBM System/370 Model 155 Installation Information - Physical Planning (GA22-6970)

IBM System/370 Principles of Operation (GA22-7000)

IBM System/370 Component Summary:

3830 Storage Control, 3330 Disk Storage (GA26-1592)

IBM System/360 Component Description:

2835 Storage Control and 2305 Fixed Head Storage Module (GA26-1589)

3211 Printer, 3811 Control and 3216 Interchangeable Train Cartridge, Component Description (GA24-3543)

Form-Design Considerations-System Printers (GA24-3488)

Emulating the IBM 1401, 1440, and 1460 on the IBM System/370 Model 155 Using OS/360 (GC27-6945)

Emulating the IBM 1410 and 7010 on the IBM System/370 Model 155 Using OS/360 (GC27-6946)

IBM System/360 Operating System:

Planning for the IBM 3211 Printer Data Management Macro Instructions and Services (GC21-5008)

Emulating the IBM 1410 and 7010 on the IBM System/370 Model 155 Using DOS/360 (GC33-2005)

Emulating the IBM 1401, 1440, and 1460 on the IBM System/370 Model 155 Using DOS/360 (GC33-2004)

IBM System/360 Disk Operating System:

Planning Guide for the IBM 3211 Printer (GC24-5085)

First Edition (June 1970)

This guide is intended for planning purposes only. It will be updated from time to time to reflect system changes; however, the reader should remember that the authoritative sources of system information are the Systems Reference Library (SRL) publications for the Model 155, its associated components and its programming support. These publications will first reflect such changes.

Copies of this and other IBM publications can be obtained through IBM branch offices.

A form has been provided at the back of this publication for readers' comments. If this form has been removed, address comments to: IBM Corporation, Technical Publications Department, 112 East Post Road, White Plains, New York 10601.

CONTENTS

FIGURES

TABLES

SECTION 01: SYSTEM HIGHLIGHTS

The System/370 Model 155 is designed to enhance, extend, and broaden the successful concepts of System/360 architecture. It is a general purpose growth system for System/360 Model 50 and large Model 40 users that provides significant price performance improvement without the necessity of major reprogramming. The System/370 Model 155 retains and extends the wide range of data processing capabilities offered by System/360 Models 40 and 50. It is compatible with the System/370 Model 165.

Transition from System/360 models to the System/370 Model 155 can be accomplished with a minimum of effort because most current System/360 user programs, I/O devices, and programming systems are upward compatible with the new system. Additional capabilities will be added to OS and DOS to support new features of the Model 155, thereby providing proven operating system performance as well as continuity.

Transition with little or no reprogramming also is provided for 1401/1440/1460 and 1410/7010 users who are presently emulating on System/360. Improved emulators are provided for these systems that operate under OS or DOS control on the Model 155.

DOS users who wish to install OS on their Model 155 can ease the transition by installing the new OS/DOS Compatibility Feature. An OS DOS Emulator program is provided that supports emulation of a DOS multiprogramming system under OS control.

Highlights of the Model 155 are as follows:

- Upward compatibility with most System/360 architecture and programming has been maintained.

- Internal performance is approximately three and one-half to four times that of the Model 50 for a typical instruction mix.

- The following are CPU features of the Model 155.

  The Model 155 standard instruction set includes new general purpose instructions in addition to the powerful System/360 instruction set. These instructions enhance decimal arithmetic performance, eliminate the need for multiple move or compare instructions or move subroutines, and facilitate record blocking and deblocking, field padding, and storage clearing.

  Extended precision floating-point is available to provide precision of up to 28 hexadecimal digits, equal to approximately 34 decimal digits.

  An interval timer of 3.33 ms resolution to improve job accounting accuracy is standard. A 16.6 ms resolution timer is provided for Models 40 and 50.

  A time of day clock is included to provide more accurate time of day values than the interval timer. The clock has a 1 microsecond resolution.

  Instruction execution is overlapped with instruction fetching to improve internal performance.

CPU retry of most failing CPU hardware operations is handled automatically by the hardware without programming assistance.

- Functionally improved relocatable emulators are available that operate under operating system control. Concurrent execution of System/370 programs with any combination of 1401, 1440, 1460, 1410, and 7010 programs in a multiprogramming environment is supported. Only one compatibility feature is required for integrated emulation of all these systems.

- The new OS/DOS Compatibility Feature permits emulation of a DOS system under OS concurrent with the execution of other OS jobs. Both DOS and 1400/7010 emulation can operate together on a Model 155 under OS control.

- New operator console devices are provided.

  The 15-cps 3210 Console Printer-Keyboard

  The 85-cps 3215 High-Speed Console Printer-Keyboard

  A remote 3210 Console Printer-Keyboard, which can be installed in addition to either of the above printer-keyboards

- The following channel features are available for the Model 155.

  Up to five high-speed block multiplexer channels can be attached in addition to the standard byte multiplexer channel. Two block multiplexers are standard. A block multiplexer channel can operate at a 1.5-megabyte data rate and can therefore support I/O devices such as the 2420 Model 7 Magnetic Tape Unit - not attachable to the Model 40.

  A special feature permits replacement of channel 4 with a second byte multiplexer channel to provide up to 512 byte multiplexer subchannels in systems with 768K or more and with channel 3 installed.

  A block multiplexer channel is a superset of a selector channel. When used in conjunction with rotational position sensing devices, block multiplexer channels can increase total system throughput by permitting increased amounts of data to enter and leave the system in a given time period. A single block multiplexer channel can support interleaved, concurrent execution of multiple high-speed I/O operations.

  Block multiplexer channels with a data rate of 1.5 MB support attachment to the Model 155 of the 3330 and the 2305 Model 2 facilities, which are not included in Model 40 and 50 configurations.

  Channel retry data is provided when channel errors occur so that error recovery routines can retry I/O operations.

- The following storage features are provided by the Model 155.

  A two-level memory system is implemented, consisting of fast, large-size processor (main) storage used as backing storage for a smaller, very high-speed buffer storage. The CPU works mostly with the buffer so that the effective system storage cycle is one-third to one-quarter of the actual processor storage cycle:

  8K bytes of high-speed monolithic buffer storage is standard. The CPU can fetch four bytes from the buffer in 230 nanoseconds.

256K to 2048K of processor (main) storage is available - four times the maximum main storage available on the Model 50. Processor storage has a cycle time of 2.1 microseconds for consecutive 16-byte references.

Byte boundary alignment is permitted for the operands of non-privileged instructions to eliminate the necessity of adding padding bytes within records or to blocked records for the purpose of aligning fixed- or floating-point data.

Error checking and correction (ECC) hardware, which automatically corrects all single-bit processor storage errors and detects all double-bit and most multiple-bit errors, is standard.

- I/O devices include the following.

  Most currently announced I/O devices for System/360 Models 40 and 50 can be attached.

  The new 3330 facility is available with significantly faster seeks and more than twice the data rate of the 2314 facility, more than three times the capacity of the 2314, and automatic error correction features. The new rotational position sensing and multiple requesting capabilities announced for the 2305 facility are standard.

  The 3330 has an 806 KB data transfer rate, average seek time of 30 ms, and full rotation time of 16.7 ms. Up to 800 million bytes can be contained on an eight drive facility.

  One 2305 facility Model 2, with a maximum module capacity of 11.2 million bytes, a data rate of 1.5 megabytes, and average access of 5 ms can be attached to a Model 155 to be used as a system residence device or as high-speed storage.

  The new high-speed 3211 Printer with a tapeless carriage and print speed of 2000 alphameric lines per minute is available. The tapeless carriage decreases operator intervention by eliminating carriage tape loading and unloading.

- Extensive hardware and programming systems error recovery and repair features are provided to improve system reliability, availability, and serviceability.

- Compact physical design reduces Model 155 space requirements. The Model 155 has more than two and one-half times the number of circuits as a Model 50, yet a 512K system is one frame smaller than a 512K Model 50.

As the highlights indicate, Model 40 and 50 users have a broader range of Model 155 configurations to choose from than before when tailoring a growth system with improved throughput and expanded capabilities.

Specifically, the Model 155 offers the following advantages over Models 40 and 50.

Larger Processor (Main) Storage Sizes

Storage sizes of 256K, 384K, 512K, 768K, 1024K, 1536K, and 2048K are provided. The Model 40 can have a maximum of 256K, while 512K is the largest main storage size provided by a Model 50. The Model 155 offers larger storage sizes at smaller cost increments, and additional storage can contribute significantly to system performance and capabilities.

The addition of more storage provides the Model 155 user with the ability to:

- Execute more jobs concurrently, including new application and integrated emulator jobs
- Add and expand applications, such as graphics, teleprocessing, time-sharing, and data-based, that require larger amounts of storage
- Use higher level language translators and linkage editors that provide more functions and execute faster
- Execute larger processing programs without the necessity of overlay structures
- Allocate more storage to language translators and sorts to improve their execution speed
- Use more and larger I/O buffers to speed up input/output operations and optimize use of direct access storage space
- Include system generation options that improve control program performance and support additional functions

Greatly Expanded Channel Capabilities

The fast internal performance of the Model 155, together with expanded use of multiprogramming, requires that more data be available faster.

Two byte multiplexer channels can be installed on a Model 155. Models 40 and 50 are limited to one. The Model 155 also offers more and faster high-speed channels than the Model 50 (five instead of three, 1.5 MB data rate versus .8 MB) and block multiplexer channels not provided for Models 40 and 50.

The channel features of the Model 155 provide:

- Up to 512 byte multiplexer subchannels for large teleprocessing users.
- Attachment of high-speed direct access devices such as the 3330 and 2305 Model 2 facilities
- Potential increases in channel throughput via use of block multiplexing with rotational position sensing to improve effective data transfer rates
- A significantly higher attainable aggregate channel data rate than the Model 50 to balance the high performance capabilities of the Model 155 CPU

Faster I/O Devices with Increased Data Capacity

The 3330 and the 2305 Model 2 facilities offer significantly faster data access than the 2314 facility and 2301 Drum Storage because of higher data transfer rates, faster rotation, and new features. Rotational position sensing and multiple requesting used with block multiplexing can improve I/O throughput by making more efficient use of channel time. These direct access facilities also offer higher availability through use of new hardware-only and program-assisted error correction features.

The 3330 facility provides high-capacity and fast access for less cost per bit. It is a growth device for the 2314 facility and the 2321 Data Cell Drive that offers increased price performance. The 3330 facility is designed to be used in every area in which direct access storage is needed. For example:

- As a system residence device and for program library storage
- In teleprocessing applications for message queuing and for residence of online applications data
- In online, data-based applications, such as management information systems, airline reservations, etc.
- In time-sharing (or interactive) environments as online work storage (for program and data residence)
- As high-speed work storage for sorting, assembling, and link editing
- For residence of data indices, such as for ISAM data sets

The 2305 Model 2 facility offers faster access than, and more than twice the capacity of, the 2301 drum. For larger Model 155 users, the 2305 facility will be of benefit:

- As the primary system residence device
- In time-sharing environments for program and data residence
- As high-speed work storage and for residence of data indices

SUMMARY

The combination of new and improved hardware and input/output facilities, enhanced operating system support, integrated 1400/7010 emulation, DOS emulation under OS, and increased system availability provided by the Model 155 offers Model 40 and 50 users expanded computing capabilities without the necessity of a large conversion effort. Little or no time need be spent modifying operational System/360 code or programs currently being emulated. Users of 1400 and 7010 systems can upgrade directly to a Model 155 and an operating system environment with a minimum of reprogramming. DOS users can convert to OS more easily than is possible without the use of DOS emulation. Existing CPU-bound programs can execute faster because of the increased internal performance of the Model 155, while I/O-bound programs can benefit from the use of more storage, more channels, faster I/O devices, and block multiplexing.

The increased power and new functions of the Model 155 provide the base for expanded applications growth and penetration of previously marginal application areas. The increased price performance of the Model 155 offers the user the opportunity to widen his data processing base for less cost.

In conclusion, the major advantages of the System/370 Model 155 are:

- LARGE PROCESSOR STORAGE - At low cost increments
- FAST INTERNAL PERFORMANCE - Approximately three and one-half to four times the Model 50
- CHANNEL ENHANCEMENTS - More, faster, new capability
- INTEGRATED EMULATION - Native mode and second generation processed concurrently
- RELIABILITY, AVAILABILITY, AND SERVICEABILITY - Hardware and programming systems features not available on System/360 Models 40 and 50
- NEW I/O EQUIPMENT - Faster, larger direct access storage with new capabilities and a faster printer

SECTION 10: ARCHITECTURE AND SYSTEM COMPONENTS

10:05 ARCHITECTURE DESIGN

The basic design objectives embodied in System/370 Model 155 architecture provide System/360 and 1401/1440/1460 and 1410/7010 emulator users with a growth system in the medium system range that incorporates improvements and additions to System/360 architecture. The Model 155 provides new system capabilities, performance improvements, and features to increase system reliability, availability, and serviceability. This has been achieved under the following conditions:

- System/370 Model 155 architecture is upward compatible with that of System/360 models so that most user programs written for the System/360 will run efficiently on the Model 155 without modification.
- Programming systems support for the Model 155 is based on that provided for System/360 models, namely OS and DOS.
- Most currently announced System/360 I/O devices will operate on the Model 155. (See Section 20:05 for a list of the I/O devices that cannot be included in a Model 155 configuration.)
- The open-ended design characteristic of System/360 has been preserved and extended on System/370.

As a result of the architecture design criteria used for this new system, all programs written for System/360 (Models 25 and up) will operate on a System/370 Model 155 with a comparable hardware configuration, with the following exceptions:

1. Time-dependent programs
2. Programs using machine-dependent data such as that which is logged in the machine-dependent logout area. (OS SER and MCH error-logging routines and the DOS MCRR error-logging routine for System/360 models will not execute correctly.)
3. Programs that use the ASCII mode bit in the PSW
4. Programs that depend on the nonusable lower core storage area being smaller than 1152 bytes. This area can be reduced to 512 bytes by moving the CPU logout area. (See Section 50.)
5. Programs deliberately written to cause certain program checks
6. Programs that depend on devices or architecture not implemented in the Model 155, for example, the native file of the Model 44, relocation implemented in the Model 67, etc.
7. Programs that use model-dependent operations of the System/370 Model 155 that are not necessarily compatible with the same operations on System/360 models

Note that these are the same types of restrictions that exist for compatibility among System/360 models.

The major sections of the Model 155 computing system are the processor (CPU), storage, channels, and the system control panel and console. Each component and its new features are discussed in the subsections that follow. Programming systems support of these new features is covered in Section 30. Reliability, availability, and serviceability (RAS) hardware features are mentioned only briefly. A full discussion of both hardware and programming systems RAS facilities is contained in Section 50.

10:10 THE CENTRAL PROCESSING UNIT (CPU)

The central processing unit contains all the elements necessary to decode and execute the instructions in the System/370 Model 155 instruction set and, optionally, those in the hardware compatibility feature required by the 1401/1440/1460 and 1410/7010 emulator programs. All CPU functions and channel operations are controlled by the microprogram contained in the 72-bit control words in capacitor read-only storage (ROS). The Model 155 CPU has a cycle time of 115 nanoseconds. Among the elements contained in the CPU are a four-byte parallel binary adder, local storage, and instruction fetch hardware.

A single local storage, addressable by the microprogram, is used as an intermediate storage area by the CPU and the integrated channels. It consists of two areas. CPU local storage, which contains the general purpose and floating-point registers, is shared by the CPU and the channels. I/O local storage is used exclusively by the channels and is controlled by separate channel hardware so that it can be used for I/O data transfer without interfering with the CPU.

Instruction processing performance is improved by the fact that most instruction fetching is overlapped with instruction execution. Three one-word instruction buffers are provided in the I-Fetch area of the CPU for the prefetching of instructions. One prefetched instruction is decoded at a time but operands are not prefetched.

Imprecise interrupts do not occur on the Model 155. An interrupt is referred to as "imprecise" when not enough information is available to determine which instruction caused the interrupt. Models 40 and 50 do not overlap instruction fetching with instruction execution.

Extensive parity checking is done in the CPU to insure the validity of the data being used. Every data path within and to the CPU is parity-checked, as are every ROS word and all adder sums. Automatic hardware retry of most failing CPU operations, without programming assistance, is provided as an availability feature and is discussed in the RAS section.

The program states in which the Model 155 is operating are reflected in the current program status word (PSW) and in new CPU status indicators called control registers, which are located in the CPU. Up to 16 control registers, 0-15, can be addressed; however, only 4 are implemented in the Model 155. They are program addressable when the CPU is in the supervisor state. A control register can be set with the new LOAD CONTROL instruction and its contents can be placed in processor storage with the STORE CONTROL instruction. Additional status indicators contained in control registers are required in order to support new system functions.

The contents, layout, and function of fixed locations 0-127 in System/370 models are identical to these locations in System/360 models with one exception. Bit 12 in the PSW, which sets EBCDIC or ASCII mode in System/360 models, is not used for this purpose in the Model 155 and must be set to zero. ASCII mode is not implemented in the

TIME OF DAY CLOCK

This new clock is a binary counter of 52 bits with a cycle of approximately 135 years. It is a standard feature. The clock is updated every microsecond. Two new instructions (SET CLOCK and STORE CLOCK) are provided to set the time and to request that the current time be stored in the specified doubleword of processor storage. The time can be set only when the CPU is in supervisor state and only when the clock security switch on the system console panel is in the enable set position.

The time of day clock can be used for more accurate time stamping than the interval timer. Accurate time of day can be maintained because the clock stops only when CPU power is turned off. The interval timer cannot be as accurate as the clock for time of day maintenance because it is not updated when the system is in the stopped state and its updating may be omitted under certain conditions of excessive system activity. The 15.5-hour cycle time of the interval timer is also a restriction. The time of day clock better answers the timing needs of teleprocessing and real-time applications.

10:15 STORAGE

PROCESSOR (MAIN) STORAGE

The Model 155 has a two-level memory system, a small high-speed buffer storage backed by a large processor (main) storage. Prior to this time, such a concept was implemented only in very large-scale, high internal performance systems such as System/360 Models 85 and 195. Model 155 processor storage has a 2.1 microsecond cycle time and is buffered by 8K of high-speed monolithic buffer storage.

The use of a two-level memory system, in which the CPU works mostly with the buffer, drastically reduces the effective processor storage cycle of the Model 155 and greatly contributes to the fact that the internal performance of the Model 155 is approximately three and one-half to four times that of the Model 50.

Processor storage is available in the following increments:

Model	Capacity
H	256K
HG	384K
I	512K
IH	768K
J	1024K
JI	1536K
K	2048K

The CPU, the buffer, or a channel has access to 16 bytes of processor storage every 2.1 microseconds for consecutive fetches with no interference.

Error checking and correction (ECC) hardware provides automatic detection and correction of all single-bit processor storage errors and detection, but not correction, of all double-bit and most multiple-bit errors. The ECC feature is discussed fully in the RAS section.

The Model 155 supports a byte-boundary alignment facility for processor storage. The presence of the byte-oriented operand function allows the processor storage operands of unprivileged instructions (RX and RS formats) to appear on any byte boundary without causing

a specification program interrupt. Without this facility, operands must be aligned on integral boundaries, that is, on storage addresses that are integral multiples of operand lengths. Byte orientation is standard and does not apply to alignment of instructions or channel command words (CCW's).

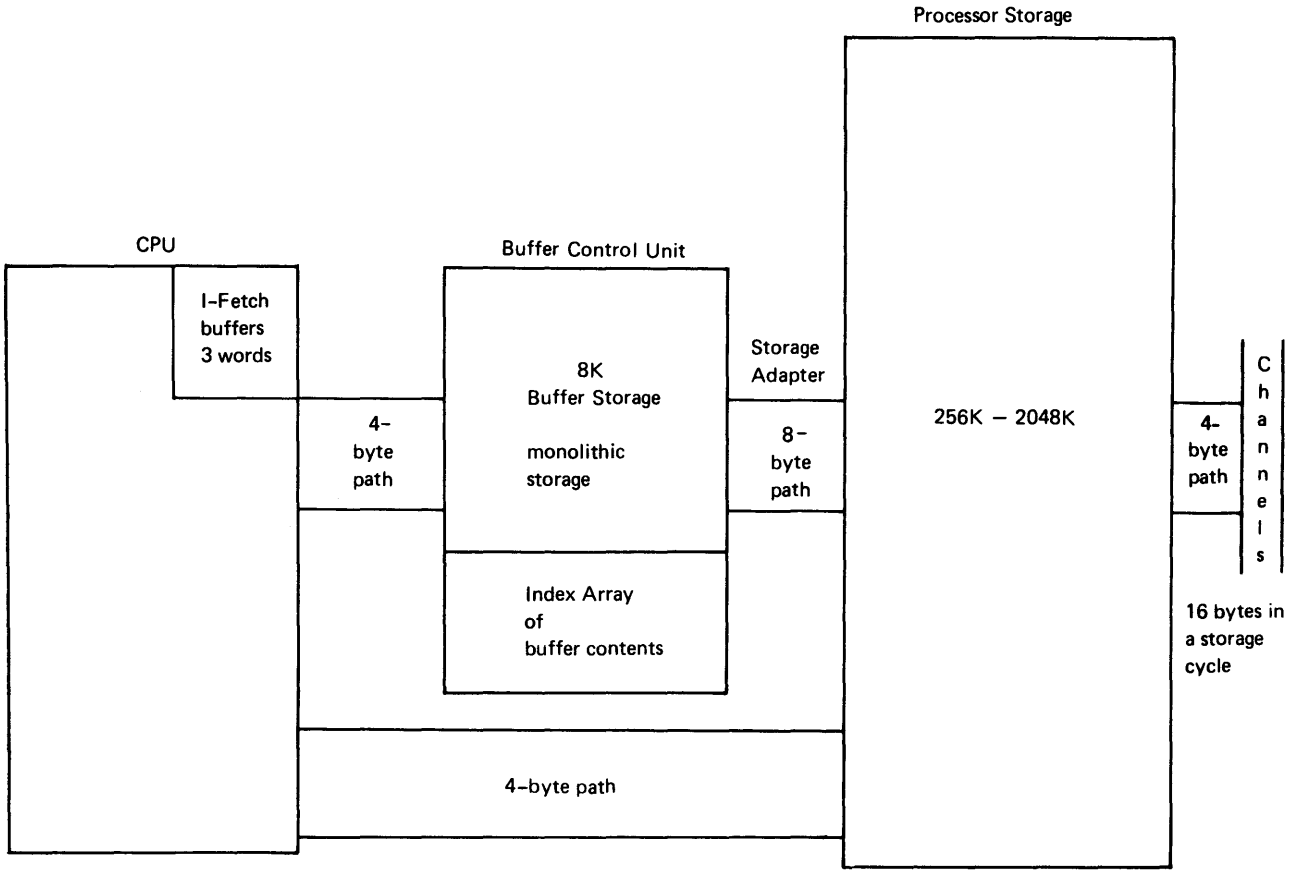
Use of byte alignment in a program degrades instruction execution performance. However, byte orientation can be used effectively in commercial processing to eliminate the padding bytes added within records or to blocked records to insure binary and floating-point field alignment. The smaller physical record that results from the elimination of padding bytes requires less external storage and increases effective I/O data rates. I/O-bound commerical programs, in which throughput is in almost direct proportion to the I/O data rate, can achieve performance improvement by using byte alignment for binary and floating-point data.

A program written to use byte boundary alignment will not necessarily run on a System/360 model that does not have the feature. Therefore, programs that are to run on both the Model 155 and on System/360 models without byte orientation should be written to adhere to integral boundary rules.

HIGH-SPEED BUFFER STORAGE

The increase in the internal performance of the Model 155 is achieved largely by the inclusion of a high-speed buffer storage unit. The 8K buffer is a standard feature and provides high-speed data access for CPU fetches. The CPU can obtain four bytes from the buffer in 230 nanoseconds (two cycles) or eight bytes in 345 nanoseconds (three cycles) if processor storage is not busy. If the buffer does not contain the data needed, the data must be obtained from processor storage. There is a four-byte-wide path between the CPU and processor storage that bypasses the buffer. With no channel interference, the CPU can access 4 bytes in 1.49 microseconds, 8 bytes in 1.61 microseconds, or 16 bytes in 1.96 microseconds from processor storage.

The conceptual data flow in the Model 155 is pictured in Figure 10.15.1. The data path within the CPU is four bytes wide.



CPU fetch from buffer	230 nanoseconds for 4 bytes 345 nanoseconds for 8 bytes
CPU fetch from processor storage	1.49 microseconds for 4 bytes 1.61 microseconds for 8 bytes 1.96 microseconds for 16 bytes
High-speed channels to or from processor storage	2.1 microsecond cycle for every 16 bytes

Figure 10.15.1 Conceptual data flow in the Model 155. Access times shown assume no interference.

The buffer control unit provides the interface between the buffer and the CPU and the buffer and the storage adapter. When a data fetch request is made by the CPU, the buffer control unit determines whether or not the requested data is in the high-speed buffer by interrogating the index array of the buffer's contents. If the data requested is present in the buffer and is valid, it is sent directly to the CPU without a processor storage reference. If the requested data is not currently in the buffer, or is no longer valid, a processor storage fetch is made and the data obtained is sent to the CPU. The data is also assigned a buffer location and stored in the buffer. When data is stored by the CPU, both the buffer and processor storage are updated if the contents of the processor storage location being altered are currently maintained in the buffer.

The channels never access the buffer directly. They read into and write from processor storage only. When a channel stores data in processor storage, the index array is interrogated. If data from the

affected processor storage address is being maintained in the buffer, appropriate bits are set in the index array to indicate that this buffer data is no longer valid.

The algorithm used to maintain the contents of the high-speed buffer is relatively uncomplicated. It provides close to optimum buffer use at a price performance level consistent with the goals of the Model 155. The algorithm is designed to be transparent to the programmer so that no particular program structure need be adhered to in order to obtain close to optimum performance. Sample job step executions have shown that the data fetched by the CPU is in the buffer approximately 90% of the time.

Processor storage and the buffer are divided into 16-byte halfblocks within 32-byte blocks within 4K-byte rows, as illustrated in Figure 10.15.2. A row contains 128 blocks. The number of rows in processor storage is a function of its size. For example, a 1024K system has 256 rows.

The index array in the buffer control unit is used to maintain knowledge of the contents of the upper and lower compartments of the buffer. Each compartment is 4K bytes, or one row, in size. Each of the 128 block addresses in the index array contains two entries, one to describe a block in the upper 4K compartment and one to describe the corresponding block in the lower 4K compartment. An index array entry contains a processor storage row address, two valid bits, and an OK bit. When data from processor storage is placed in the buffer, its processor storage row address (bits 11-19 of the processor storage address) is placed in the index array entry for its block. The valid bits, one for each halfblock in the block, indicate the presence of valid data in that buffer block location. A valid bit is set on when a buffer halfblock is loaded from processor storage. The OK bit indicates that the corresponding block of the index array and buffer are functioning correctly. The OK bit for a block is set off when a malfunction associated with that block occurs.

A buffer compartment may contain a complete row of processor storage, that is, all 128 blocks of a given row, or, more normally, blocks from several different processor storage rows. Block positions within each 4K row of processor storage are placed in corresponding block positions within the upper or lower compartment in the buffer. Therefore, each block of data within a 4K row of processor storage can be placed in only one of two buffer block locations. That is, the first 32 bytes (block 0) of each processor storage row (say addresses 4096-4127, 8192-8223, 12,188-12,219, etc.) can be placed in the first block location of the upper compartment or in the first block location of the lower compartment.

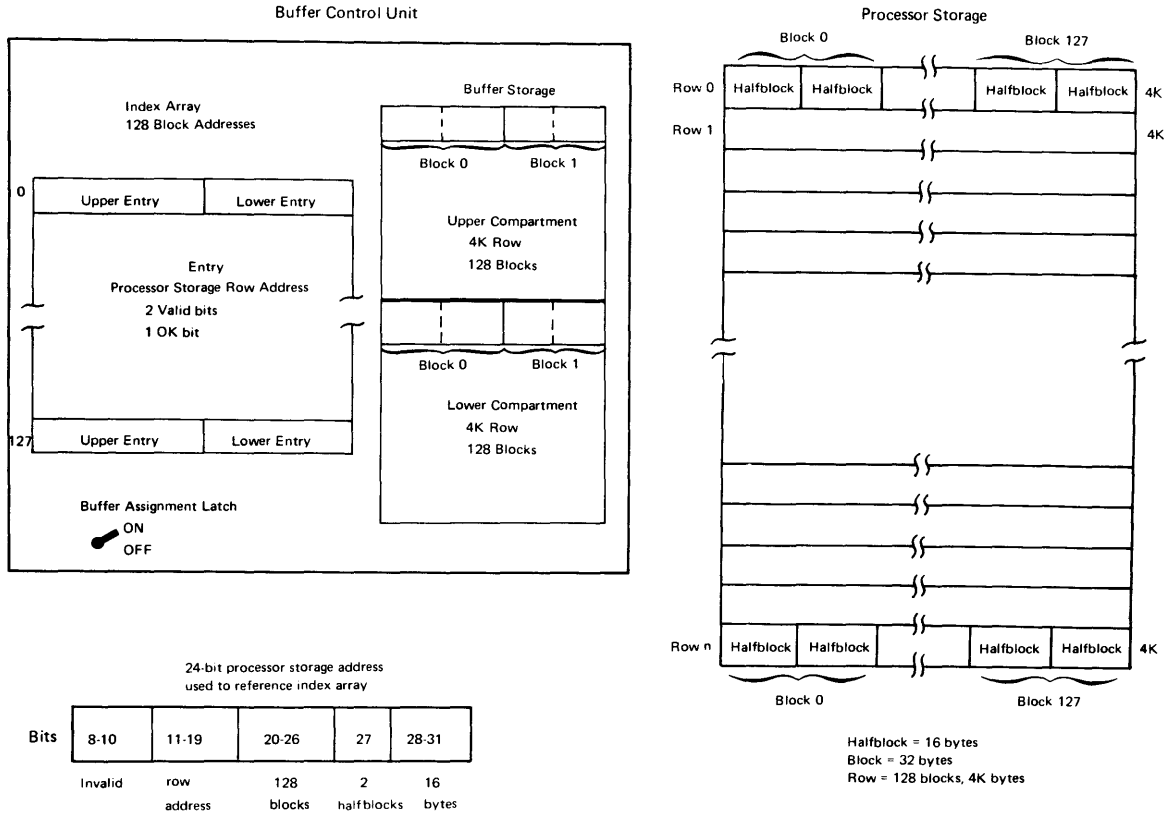


Figure 10.15.2. Buffer contents management

Buffer space is assigned on a block basis but is loaded a halfblock (16 bytes) at a time. A block in the buffer is assigned when the CPU fetches either halfblock of a corresponding block from a processor storage row. The other halfblock of the processor storage block is placed in the buffer only when (or if) referenced by the CPU. A buffer assignment latch is used in certain instances to determine which compartment of the buffer is to be assigned. The buffer assignment latch is set to indicate the compartment not referenced last; that is, if the CPU fetches data from the upper compartment, the latch is set on to indicate that the lower compartment is to be assigned next. If a CPU fetch causes data to be placed in the buffer, the buffer assignment latch setting is not altered. System reset causes the latch to be set off, indicating the upper compartment.

When a halfblock not contained in the buffer is requested by the CPU, it is assigned a buffer block in one compartment or the other, depending on the following conditions:

1. If the corresponding blocks in both buffer compartments are available, the setting of the buffer assignment latch determines which compartment is assigned.

2. If the corresponding blocks in both buffer compartments have at least one halfblock already assigned (neither block is available), the latch setting determines the compartment used.

3. If the corresponding block of one compartment has at least one halfblock already assigned and the corresponding block of the other compartment is completely available, the unassigned compartment is used without regard to the latch setting.

See Figures 10.15.3 and 10.15.4 for an example of buffer allocation.

Extensive data validity checking is done on buffer data. Parity checking is performed on both data and control information. Data is checked as it enters and leaves the buffer. If a buffer component fails, the OK bit for that block is set off by the buffer control unit. This causes all subsequent CPU fetches for that block to be made from processor storage. A machine check occurs when a block in the buffer is deleted so that error recording can be done (discussed in the RAS section). A console switch and a microprogram instruction provide the ability to disable the entire buffer so that all data is fetched directly from processor storage, should this be necessary to allow continued system operation.

Sequence I

Assume that the buffer is empty, that the latch is set to the upper compartment, and that the program receives CPU control at processor storage location 102,400 (refer to Figures 10.15.3 and 10.15.4).

1. CPU fetches instruction 1 (102,400-102,403), which is not in the buffer.

2. Processor storage locations 102,400-102,415 are brought into the high-order halfblock of block 0 in the upper compartment (rule 1) and instruction 1 is sent to the CPU.

3. CPU executes instruction 1 - store into row 28, block 10. The buffer is not changed.

4. CPU fetches instruction 2 (102,404-102,407), which is contained in the buffer. The latch is set to the lower compartment.

5. CPU executes instruction 2 - fetch from locations 110,592-110,595, which are not in the buffer.

6. Locations 110,592-110,607 are brought into the high-order halfblock of block 0 in the lower compartment (rule 3) and the required data is sent to the CPU. The latch remains set to the lower compartment.

7. CPU fetches and executes instructions 3, 4, 5, and 6, all of which are register-to-register operations. All fetches are made to block 0 of the upper compartment. The buffer contents and latch setting remain the same.

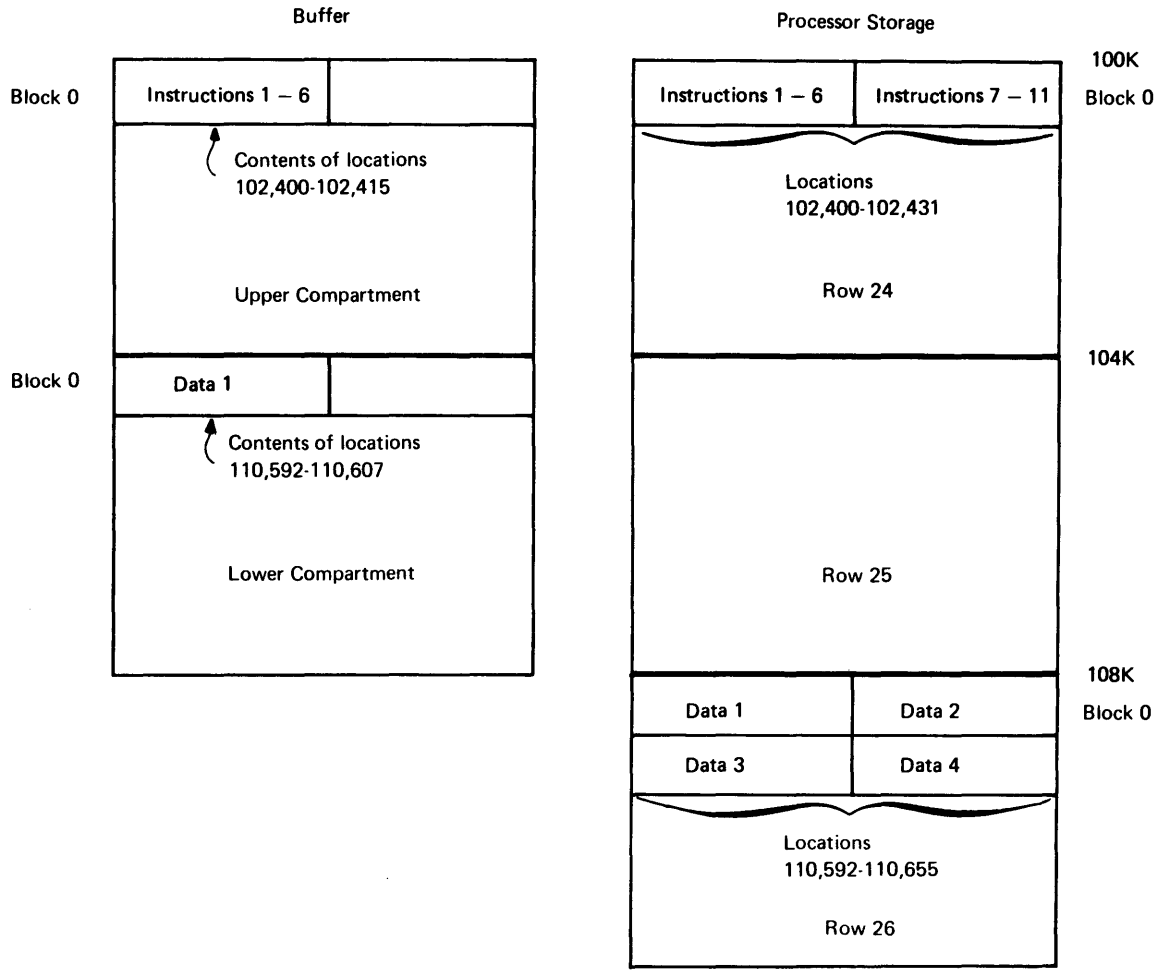


Figure 10.15.3. Buffer allocation example (part I)

Sequence 2

8. CPU fetches instruction 7 (102,416-102,419), which is not in the buffer.

9. Locations 102,416-102,431 are brought into the low-order halfblock of block 0 in the lower compartment (rule 2) and instruction 7 is sent to the CPU. The latch remains set to the lower compartment.

10. CPU executes instruction 7 - store into locations 110,596-110,599. The data is placed in the lower compartment of the buffer (high-order halfblock of block 0) and in processor storage. The latch remains set to the lower compartment.

11. CPU fetches instruction 8 (102,420-102,423), which is in the lower compartment. The latch is set to the upper compartment.

12. CPU executes instruction 8 - fetch from locations 110,600-110,603. The data is sent to the CPU from the lower compartment. The latch remains set to the upper compartment.

13. CPU fetches instruction 9 (102,424-102,427), which is in the lower compartment. The latch setting is not changed.

14. CPU executes instruction 9 - fetch from locations 110,608-110,611, which are not in the buffer.

15. Locations 110,608-110,623 are brought into the low-order halfblock of block 0 in the upper compartment (rule 2) and the data is sent to the CPU.

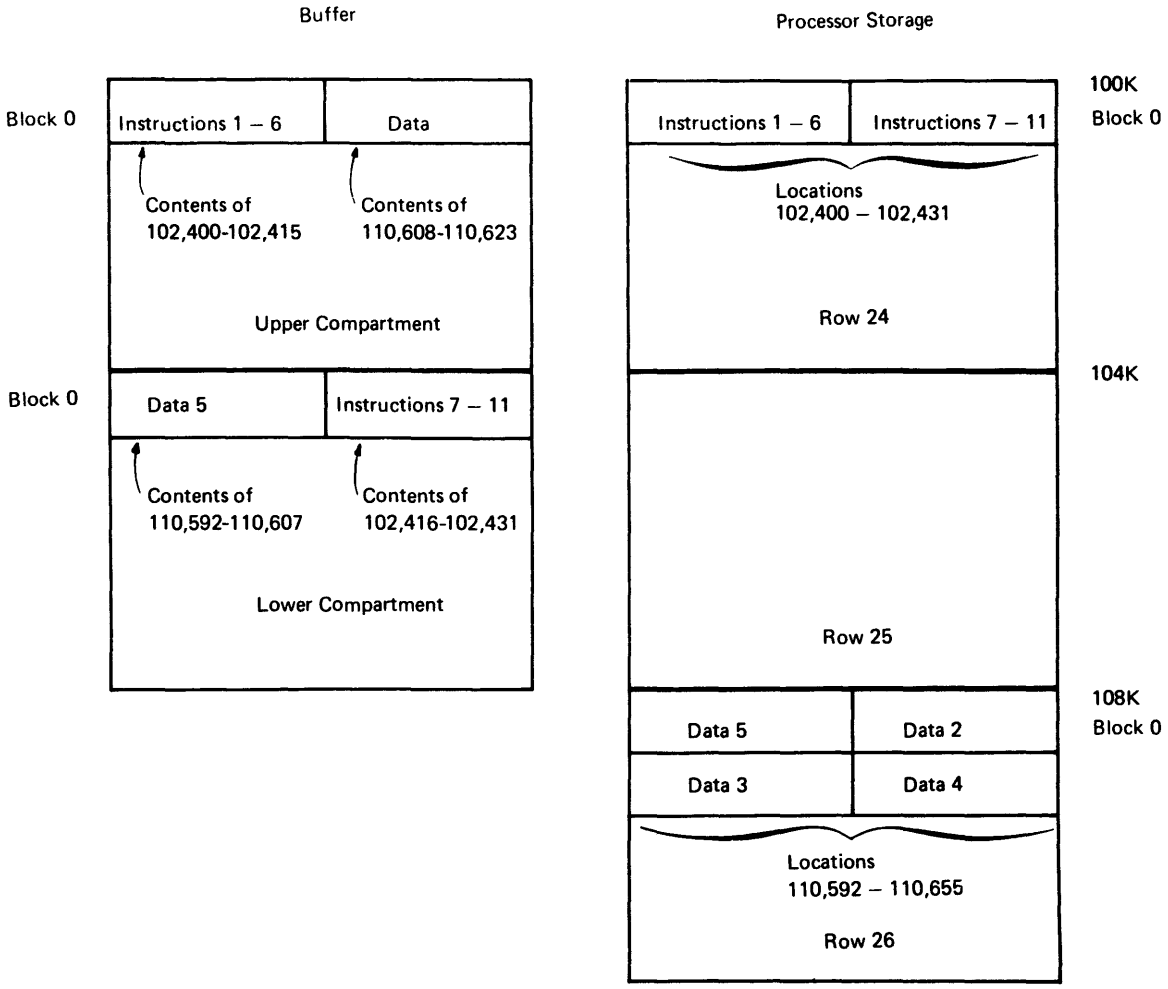


Figure 10.15.4. Buffer allocation example (part II)

10:20 CHANNELS

The channels available on the Model 155 are functionally compatible with those of System/360 models but they can handle much faster data rates. The new block multiplexer channels are standard on the Model 155 and can increase the channel throughput of the system.

Two types of channels are available: byte multiplexer and block multiplexer. A byte multiplexer and block multiplexer channels 1 and 2 are standard on the Model 155. Block multiplexer channels 3, 4, and 5 are optional. A second byte multiplexer can be installed in place of channel 4 to provide up to 512 subchannels in one system.

A block multiplexer channel can operate in selector channel mode. Data is transferred between processor storage and a block multiplexer channel at the rate of 16 bytes in a 2.1 microsecond cycle whether the channel is in block multiplexer or selector mode.

Model 155 channels are integrated. They share with the CPU the use of ROS control storage, use of the CPU and processor storage data flow, and use of the CPU arithmetic logic unit. The byte multiplexer channel can interfere with CPU operations when it requires one of the shared components. Block multiplexer channels can interfere with both the CPU and the byte multiplexer channel. The channels interfere with CPU operations when an I/O operation is started and when it completes, as well as when a data transfer to or from processor storage is required. Sample timings have shown channel interference with CPU operations on a Model 155 to be less than on a Model 50 for any given data rate.

Comprehensive error checking has been incorporated in the basic design of the channel hardware. Checking is performed on the control logic in most areas and standard parity checking is done on the data flow. Improved error recovery hardware has also been included (discussed fully in the RAS section).

The standard instruction set also includes a new I/O instruction called HALT DEVICE. This instruction is specifically designed to stop an I/O operation on a particular device on a byte or block multiplexer channel without interfering with other I/O operations in progress on the channel. HALT DEVICE should always be used, instead of HALT I/O, to stop an I/O operation on a multiplexer channel.

The Channel-to-Channel adapter feature available for System/360 models is also an optional feature for the Model 155. It allows two System/370 channels or a System/370 and System/360 channel to be interconnected. Only one adapter can be installed on a Model 155.

BYTE MULTIPLEXER CHANNELS

The byte multiplexer channel provided for the Model 155 is functionally identical to the one available on System/360 Models 30, 40, and 50. It operates in byte interleave mode, permitting several slow-speed devices to operate concurrently, or in burst mode, allowing one high-speed device to function.

Depending on the size of processor storage, up to 256 subchannels are available on the standard byte multiplexer channel that is assigned channel address 0. The number of subchannels present determines the maximum number of concurrent I/O operations that can operate on the byte multiplexer channel. Each subchannel is associated with a unit control word (UCW), and the number of UCW's present in a Model 155 is related to the size of processor storage. UCW's are contained in "bump" storage, an extension of processor storage not program addressable. They are used to store channel register data in between data transfers to and from processor storage when devices are operating on the byte multiplexer channel.

A significant new optional feature is available for Model 155 systems with channel 3 installed and 768K or more of processor storage. The Second Byte Multiplexer Channel feature permits an additional byte multiplexer channel to be installed, in place of channel 4. Installation of a second byte multiplexer provides a total of 384 subchannels for 768K systems and 512 subchannels for systems with 1024K or more. This feature enhances the teleprocessing capabilities of the Model 155.

The following are examples of configurations that can operate on the Model 155. The second example is oriented toward a larger teleprocessing configuration.

1.

Channel	I/O Data Rate
Channel 1 2305 Model 2 facility	1.5 MB
Channel 2 3330 facility	.806 MB
Channel 3 3330 facility	.806 MB
Channel 4 3330 facility	.806 MB
Channel 5 3330 facility	.806 MB
Byte Multiplexer	
Type 2 TELPAK Adapter	6.25 KB
2540 Card Read Punch	1.38 KB
1403 Printer	2.42 KB
Approximate aggregate data rate	4.7 MB

2.

Channel	I/O Data Rate
Channel 1 2305 Model 2 facility	1.5 MB
Channel 2 3330 facility	.806 MB
Channel 3 2420 Model 7 tape	.320 MB
Channel 4 2420 Model 7 tape	.320 MB
Byte Multiplexer	
Type 2 TELPAK Adapter	6.25 KB
Type 2 TELPAK Adapter	6.25 KB
2540 Card Read Punch	1.38 KB
1403 Printer	2.42 KB
Approximate aggregate data rate	3.0 MB

The higher data rates supported by Model 155 block multiplexer channels allow attachment of higher speed I/O devices that cannot be used with Models 40 or 50. For example, the 3330 facility with a data rate of 806 KB cannot be attached to Models 40 or 50.

BLOCK MULTIPLEXER CHANNELS

Block multiplexer channels are standard on the Model 155. Each block multiplexer channel installed can operate as a selector channel. The setting of a channel mode bit in a control register determines whether a high-speed channel operates in block multiplexer or selector mode. The mode bit is set to selector mode at IPL or on system reset and can be altered by programming at any time. When a START I/O instruction is issued to a high-speed channel on the Model 155, the setting of the channel mode bit determines the mode in which the subchannel involved will operate.

The block multiplexer channel is designed to increase system throughput by increasing the amount of data entering and leaving the system in a given period of time (the effective data rate). Better use of channel time is achieved by operating the channel in block multiplexing mode. A single block multiplexer channel can support interleaved, concurrent execution of multiple high-speed channel programs. The block multiplexer channel can be shared by multiple high-speed I/O devices operating concurrently, just as the byte multiplexer can be shared by multiple low-speed devices. Like the byte multiplexer, the block multiplexer channel has multiple

SECTION 20: I/O DEVICES

20:05 I/O DEVICE SUPPORT

Most presently announced I/O devices that can be attached to System/360 Models 40 and 50 can be attached to the System/370 Model 155. The following I/O devices are not included in standard Model 155 configurations:

1052 M7 Printer Keyboard - except attached to a 2150 Console
1231 Optical Mark Page Reader
1259 M2 Magnetic Character Reader
1285 Optical Reader
1404 Printer
1418 Optical Character Reader
1428 Alphameric Optical Reader
1827 Data Control Unit (for attachment of 1800 system analog and/or digital control units to the Model 155)
2301 Drum Storage
2302 Disk Storage
7340 Hypertape Drive
7772 Audio Response Unit

The 1287 Optical Reader and 1288 Optical Page Reader can be attached to a byte multiplexer channel only.

New I/O devices for the Model 155 are:

- the 3330 facility - attaches only to a block multiplexer channel
- the 2305 facility Model 2 - attaches only to a block multiplexer channel
- the 3211 Printer - attaches to any Model 155 channel

The 3330 and 2305 facilities represent significant advancements in direct access device technology. They provide greater online data capacity, faster data rates and access, and expanded error correction features. Both have rotational position sensing and multiple requesting as standard features.

The 3330 represents the latest generation of direct access device with removable, interchangeable disk packs. The 2305 facility is a major extension of the nonremovable, high-speed, fixed-head direct access storage concept.

The major new characteristics of the 3330 and 2305 facilities and the 3211 Printer are discussed in the following subsections.

20:10 3330 DISK STORAGE AND 3830 STORAGE CONTROL

The 3330 facility is a modular, large-capacity, high-performance direct access storage subsystem. The 3330 facility consists of 3830 Storage Control and from one to four 3330 Disk Storage modules. A 3330 module contains a pair of independent disk storage drives, as shown in Figure 20.10.1. The new removable 3336 Disk Pack is used for data storage.

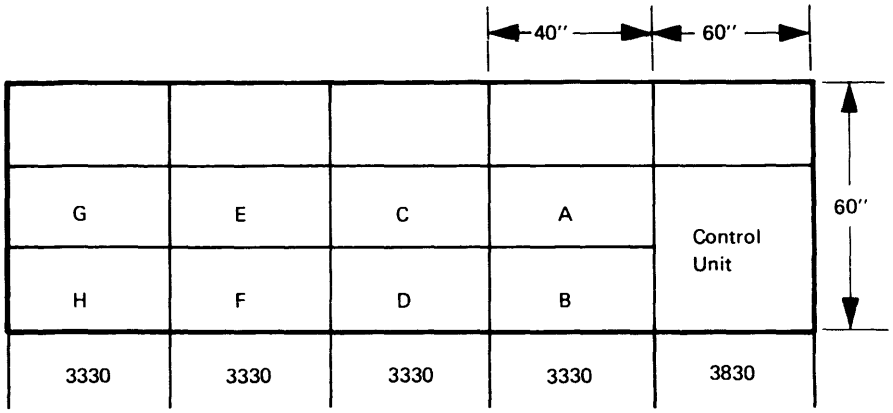


Figure 20.10.1. The 3330 facility

Drives are mounted in powered drawers that are opened and closed by a switch on the operator control panel on the 3330 module. Logical address plugs are supplied, as for the 2314, in addition to a CE service plug. The latter is used when inline diagnostics are to be executed.

Facility configurations and maximum capacities, using full track records, are shown below.

3830 Storage Control + one 3330 module 200 megabytes
3830 Storage Control + two 3330 modules 400 megabytes
3830 Storage Control + three 3330 modules 600 megabytes
3830 Storage Control + four 3330 modules 800 megabytes

Functionally, the 3330 facility provides more capabilities than the 2314, particularly in the areas of performance and availability. The 3330 supports all the standard 2314 commands (except the file scan commands) in addition to several new operations, including RPS and error recovery commands. The 3330 facility also is an attractive growth device for the 2321 Data Cell Drive.

The new, removable 3336 Disk Packs are interchangeable across 3330 disk drives but are not interchangeable with the 2316 Disk Packs used on 2314 disk drives (Table 20.10.2 compares disk pack characteristics). Like 2316 packs, 3336 disk packs will be initialized in the factory with home addresses and capacity records (R0). Up to 20 defective tracks per pack will be flagged and have alternates assigned. The QUICK DASDI utility, currently available for processing 1316 and 2316 packs, will support 3336 packs. QUICK DASDI writes the volume label, the VTOC, and IPL records, if requested, but bypasses track analysis. It also determines the number of flagged tracks and places this data in the VTOC.

Table 20.10.1 compares the capacity and timing characteristics of the 3330 facility with those of the 2314 facility and the 2321 Data Cell Drive. The increase in capacity achieved by replacing a 2314 or a 2321 with a 3330 depends upon the block size chosen for the data on the 3330. For example, if the 2314 full track block size of 7294 bytes is maintained for a given data set on the 3330 to avoid programming changes, the 3330 yields a 91% increase in full pack capacity (almost twice the capacity). However, reblocking to a full track on the 3330, 13,030 bytes, yields a 242% full pack capacity increase. If there is not enough processor storage available to allocate I/O areas of 13,030 bytes, lowering the 3330 block size used to half a 3330 track yields a 239% increase in full pack capacity.

The failing CCW is reissued twice by the control unit. If one of the two retries is successful, the channel program continues normally.

3. When a seek malfunction is detected.

   The control unit retries the command ten times in an attempt to position the arm correctly.

4. When an alternate or defective track condition is recognized before data transfer begins.

   The control unit determines the location of the alternate or defective track (from R0 on the track), initiates a seek to this track, and orients to the index point. When this sequence completes, the original command is reissued by the control unit. This is a programmed procedure for previously announced System/360 direct access devices.

5. When a command overrun (or late command chaining) condition occurs during execution of a channel program because of interference from another channel or the CPU.

   The control unit initiates a retry of the command that was late.

Error logging. Usage and error counters for each drive in the facility are maintained continuously in the control unit. The usage counters are used to accumulate the number of bytes read and seeks issued. The error counters are used to accumulate the number of seek, correctable data, and uncorrectable data errors that were retried successfully by a command retry procedure, as already described. When a counter reaches its threshold or when a pack is removed from a drive, the control unit indicates the condition via a unit check when the next I/O operation is initiated to the drive. Counter data can be obtained and counters can be reset by issuing a SENSE or READ LOG command. These statistics can then be logged in the system error data set for later diagnosis.

Inline diagnostic tests. The 3830 control unit can execute diagnostic tests on a malfunctioning drive while normal operations take place on the remaining drives in the facility. When the CE inserts the service address plug in the malfunctioning drive, diagnostic programs contained on a magnetic disk cartridge are read by the device in the control unit. Diagnostics can be executed on that drive by the customer engineer using the CE panel on the 3830 control unit. Operationally, the drive is offline to the control unit, and physically the drive is offline to the operating system.

Online testing of the 3330 facility can be performed under OLTEP control, as usual. Both OLT's and diagnostic programs contained in the OLT library can be executed on a malfunctioning drive via OLTEP. The diagnostic tests are loaded into control storage in the control unit from the OLT library. Operationally, the 3330 drive is online to the control unit but is logically offline to the operating system.

Inline and online testing allows CE diagnosis and repair of most 3330 failures without the necessity of taking the entire 3330 facility out of the system configuration.

The 3330 facility offers more than additional capacity, faster access, and attractive price performance. The 3330 facility is actually a subsystem in itself. The control unit can control the concurrent execution of one RPS channel program on each of its drives and can handle functions such as error correction and logging, which normally must be programmed, thereby relieving the control program of these

activities. In addition, the availability and serviceability of the 3330 are improved by the implementation of new automatic error correction features, by use of inline diagnostics, and by the speed and ease of engineering change installation. These factors add to the improvement of total system availability.

Table 20.10.3 Hardware features of 3330 and 2314 facilities

Feature	3330	2314
Number of drives per facility	2,4,6, or 8	1,2,3,4,5,6,7, or 8 (A ninth can be included as a spare only.)
Removable interchangeable disk packs	Yes	Yes
Removable address plugs	Yes	Yes
Record overflow feature	Standard	Standard
File scan feature	Not available	Standard
Multiple track operations	Standard	Standard
Two-channel switch	Optional	Optional
Second control unit (to permit two concurrent data transfer operations on a facility)	Not available	Optional (2844 Auxiliary Storage Control)
Rotational position sensing	Standard (128 sectors/track)	Not available
Multiple requesting	The control unit can concurrently handle one channel program on each of its drives.	Not available
Command retry by control unit and channel	Standard	Not implemented
Error correction data presented by control unit	Yes	No
Writable storage in control unit loaded from a magnetic disk cartridge	Yes	No
Inline diagnostic tests initiated via the CE panel in the facility	Standard	Standard
Inline diagnostic tests initiated via the system console	Standard	Not implemented

20:15 THE 2305 FIXED HEAD STORAGE MODULE AND 2835 STORAGE CONTROL MODEL 2

One or two 2305 Fixed Head Storage Modules can be attached to 2835 Storage Control. Each module contains six nonremovable rotating disks on which data is recorded. Read/write heads, called recording elements, are fixed in position to access each track on the twelve recording surfaces so that no arm motion is required. (See Tables 20.15.1 through 20.15.3 at the end of this subsection for a comparison of 2305 Model 2 and 2303 Drum Storage characteristics and capacities.) Only one 2305 facility Model 2 can be attached to the Model 155 and it must be placed on channel 1.

Spare, or alternate, tracks are provided in 2305 modules and must be wired in by a customer engineer to replace defective recording tracks. However, one spare track is available for assignment by the

The multiple requesting capability is implemented by associating eight logical device addresses (0-7) with a 2305 module. Each logical device address is also assigned to a specific subchannel of a block multiplexer channel and a specific register (0-7) in the 2835 control unit. When a channel program is initiated, it is associated with an available logical device address by data management (I/O supervisor). (Logical device addresses are not permanently assigned to specific tracks or data sets in a module.) When the SET SECTOR command is issued, its specified sector number is stored in the register in the control unit that is assigned to the logical device address being used for the channel program. Then the control unit disconnects from the channel.

At this point, another channel program with a SET SECTOR command can be accepted by the channel and control unit (assuming neither is busy). This channel program will be initiated using another available logical device address and its assigned control unit register. This process can be repeated for up to eight SET SECTOR commands, so that eight channel programs can be executing concurrently per 2305 module.

Whenever the control unit is not executing a command or is not otherwise busy, it monitors the rotational position counter in the 2305 module that is being incremented each sector time period. When the sector number in the counter of a module compares equal with the sector number stored in one of the registers in the control unit and the channel is free, the control unit reconnects and resumes execution of the suspended channel program associated with the logical device address assigned to the control unit register that compared equal (see Figure 20.15.2).

It should be noted that one 2305 module requires eight logical device addresses, each of which requires one subchannel on a block multiplexer channel. Since a 2835 control unit can have two modules, one 2305 facility can use 16 device addresses and 16 nonshared subchannels of a block multiplexer channel.

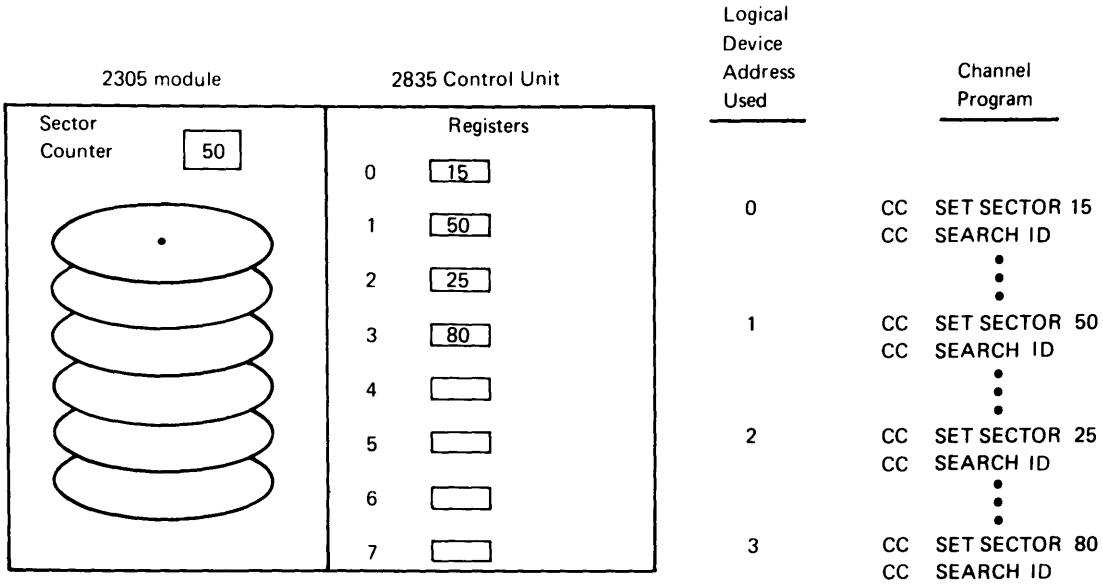


Figure 20.15.2. Multiple requesting on the 2305 facility

Table 20.15.1. 2305 Model 2 facility and 2303 Drum Storage characteristics

Characteristic	2305 Model 2	2303 Drum Storage
Device type	Six rotating disks with twelve recording surfaces	Rotating drum
Module capacity in bytes (full track records, no key)	11,258,880	3,913,000
Number of recording tracks	768	800
Number of bytes per track (R0, R1 written without key)	14,660 Home address is never written on a track	4,892 Home address is always written on each track
Number of read/write heads (recording elements) per module	864 One positioned to access each of 768 recording and 96 spare tracks	880 One positioned to access each of 800 recording and 80 alternate tracks
Rotation time (ms)	10	17.5
Access time (ms) Maximum Average	 10.25 5.0	 17.5 8.6
Time channel busy searching when SET SECTOR is used (ms)	.114 maximum .198 maximum	---
Rotation speed (rpm)	6000	3400
Data transfer rate in MB	1.5	.303
Data validity checking	10 correction code bytes (CCB) appended to each area written	Two-byte cyclic check (CC) code appended to each area written
Error recovery performed by the control unit	1. Command retry to retry a failing command without an I/O interrupt 2. Correction of data errors that occur in the data area of a record possible by programming using information in sense bytes	Not provided
Rotational position sensing	Standard feature (180 sectors per track)	Not available

20:20 THE 3211 PRINTER

The 3211 is a high-speed line printer with front printing and new features designed to reduce operator intervention. The 3211 can print 2000 alphameric lines per minute (with a 48-character set) and is designed for industries and applications, such as utilities, aerospace, finance, communications, and fabrication and assembly, that require high print speeds.

The 3211 has a standard 132-print-position line, which can be expanded to 150 positions as an option. The number of print positions does not affect printing speed. The Universal Character Set (UCS) feature is standard and the interchangeable train cartridge contains 432 graphics. The cartridge character arrangement is unrestricted and can be alphabetic, numeric, or special characters in any combination. When the character arrangement is optimized for specific printing loads, speeds of up to 2500 lines per minute can be attained.

The 3211 attaches to a 3811 control unit. Unlike some models of the 2821 control unit which can handle multiple devices, a 3811 controls only one 3211 Printer.

New features of the 3211 include a powered forms stacker, an automatic platen, and a tapeless carriage. The powered stacker mechanism is self-adjusting and automatically rises in increments as the stack of paper mounts. This insures that the stacker mechanism is always the same distance above the top of the stack of forms. The rate of rise during each increment is determined by the setting of the stacker rate knob, which can be adjusted by the operator to produce the best condition for the thickness of the forms being stacked. The stacker also can be raised or lowered manually.

When forms are inserted, the printer platen automatically positions itself close to the train cartridge in accordance with the thickness of the forms. Thus, correct clearance between the platen and the cartridge is achieved without operator intervention. Because of its automatic forms thickness sensing, the 3211 is sensitive to forms with a different degree of thickness at each edge. (For forms limitations, see the Form-Design Considerations-System Printers Manual GA24-3488.)

Forms control paper carriage tape loading and unloading by the operator is eliminated by implementation of a tapeless carriage feature for the 3211. Forms spacing and skipping are controlled by a program-loaded forms control buffer (FCB) contained in the 3811 control unit.

The FCB contains 180 storage positions, each of which corresponds to a print line, that is, a single space of the carriage. Thus, forms up to 22.5 inches in length can be accommodated at eight lines per inch spacing (or 24 inches at six lines per inch). Up to twelve channel codes (1-12), corresponding to the twelve channel positions of the paper carriage tape used on a 1403 Printer, can be stored in the appropriate buffer line positions to control carriage skipping. The FCB can be considered to contain a storage image of a carriage control tape.

A carriage control address register is used to address the FCB and maintain correct line position with respect to the form. This register is incremented as space and skip commands, which cause the form to advance, are issued. When a SKIP TO CHANNEL command is executed, the carriage control address register is incremented and the form moves until the channel specified is sensed in a line position in buffer storage. If the requested channel number is not found in the buffer, forms movement stops after address position 1 (line 1) has been sensed twice. This prevents runaway forms skipping.

A flag in a buffer storage line position is used to indicate the last line of the form for forms shorter than 180 lines. A flag bit is also used in the first buffer storage position to indicate six or eight lines per inch spacing. The FCB is loaded with the desired forms spacing characters via a LOAD FCB command issued by a program. An error indication is given if an end-of-page flag is not present or if an invalid carriage code is loaded.

Serviceability features, in addition to those provided for the 1403 Printer, are incorporated into the design of the 3211. The fact that a 3811 control unit controls only one 3211 Printer instead of multiple devices permits offline repair of the malfunctioning printer or control unit only, without the necessity of removing other operational units from the system.

The 3811 control unit presents six bytes of sense information to identify printer and control unit malfunctions instead of only one byte, as is provided for the 1403. Certain errors (such as a parity check in the print line buffer) that might be corrected by programmed retry of the print operation are identified in the sense bytes, and carriage motion is suppressed. This permits error recovery without operator intervention if the retry is successful. The additional status data presented can be stored for later analysis and should speed the diagnosis of hardware malfunctions.

30:05 TRENDS IN DATA PROCESSING AND PROGRAMMING SYSTEMS

The Model 155 and its programming systems support have been designed to operate in the data processing environment that has been emerging since the introduction of System/360.

Significant trends are the following:

- Growth toward more multiprogramming to improve system throughput. Multiprogramming also permits the user to install new applications, such as small teleprocessing inquiry or graphics applications, that otherwise would not justify a dedicated system. Multiprogramming support also has encouraged the growth of new computer environments, as indicated by the items that follow.

- Growth of integrated emulation, that is, concurrent native and emulation mode processing on one system. The execution of emulators under operating system control improves system throughput because emulators can use control program facilities (stacked job execution, data management functions, etc.) and because native mode and emulator jobs can be scheduled to operate concurrently to utilize available system resources more efficiently. The use of integrated emulators eliminates most reprogramming and eases transition from one system to another, permitting the user to expend his efforts extending and adding applications.

- Greater use of high-level languages, such as COBOL, FORTRAN, and PL/I, for applications programming. The cost of programming has been increasing, while the cost of computing hardware has been decreasing. More productive use of programmers can be achieved by the use of high-level languages. Improvements to compile times and to the size and execution speed of code produced by high-level language translators have been made and continue to be made. The support of many more functions within high-level languages has also increased their use, and the growth of interactive computing has stimulated the addition of even more facilities.

- Growth of teleprocessing applications such as remote inquiry, message switching, data collection, and management information systems. The ability of System/360 and System/370 to handle teleprocessing and batch processing in one system eliminates the necessity of dedicated, special purpose systems.

- Growth of remote computing activities, such as remote job entry and interactive computing (or time sharing), in both a nondedicated and a dedicated environment. Remote computing offers (1) fast turnaround for batch work submitted from remote locations, (2) remote user access to the large computing facilities and data base available at the central installation, and (3) interactive problem solving on a regular or a nonscheduled basis for personnel in locations remote from the central computer. In-house interactive computing is growing also as users attempt to use programmer time more efficiently.

- Growth towards large, online data base systems. The growth in the marketplace of remote computing, time-sharing, and real-time applications necessitates the instant availability of more and more data. High-capacity, fast, low-cost, reliable direct access devices supported by appropriate data organizations, access

techniques, and security measures will be required for this type of computing environment.

IBM programming systems support of these trends in data processing has been growing and continues to expand. The System/370 Model 155 offers hardware, I/O devices, and performance capability required by the expanding computing environment.

30:10 OS SUPPORT

It is expected that the majority of the users who upgrade to the Model 155 will use OS as their operating system. The design of OS and the facilities it provides currently make it a particularly suitable base upon which to build additional support of the data processing trends discussed. Some of the major OS features currently available or announced are the following:

- Priority and job class scheduling for better resource utilization
- Multiprogramming support of up to 15 user jobs and multitasking facilities
- Automatic data transcription performed by the control program (reader interpreters and output writers) concurrently with user job execution
- Dynamic resource allocation by the control program
- Multiple console support (MCS) and device-independent display operator console support (DIDOCS)
- Extensive teleprocessing and graphics support
- Remote job entry and conversational remote job entry
- Support of a wide range of interactive (time-sharing) environments

OS will be modified and extended in future releases so that it supports Model 155 hardware. Appropriate alteration of the resident portion of a control program (nucleus) generated for a Model 155 will accommodate the fixed storage area of lower storage in the Model 155. OS for the Model 155 includes currently announced OS facilities and contains additional support to handle new Model 155 hardware features and I/O devices. Emphasis also has been placed on extending error recovery, recording, diagnostic, and repair procedures.

OS support of Model 155 features will be provided as follows. Programming systems support of RAS features is discussed in Section 50.

New instructions. The Assembler F (Type I) and Assembler H (program product) language translators will include mnemonics for the general purpose and other new instructions for the Model 155 so that these instructions can be used in user-written Assembler Language programs. The currently available OS high-level language translators will not generate the six new general purpose instructions.

Extended precision floating point. Assemblers F and H will include support of the extended precision floating-point data format and instructions. In addition, extended precision will be supported by the FORTRAN H program product.

The implementation of extended precision support by FORTRAN H is such that the language translator and the processing programs generated

to include extended precision operations can operate on a System/370 or a System/360 with or without extended precision hardware. The language translator contains extended precision instructions and generates them for processing programs that use extended precision data. A program check interrupt occurs if an extended precision instruction is executed and the feature is not present in the system. This interrupt causes the processing program to call in a subroutine to handle extended precision operations. Extended precision divide is always simulated as the extended precision feature does not include such an instruction.

Interval timer. The interval timer will be supported for the same functions as it is currently except for time of day values.

Time of day clock. This clock will be supported in MFT and MVT environments for time of day requests made by system and user tasks via the TIME macro. At IPL, the operator will have the option of validating the clock time and correcting an invalid value.

Byte boundary alignment. The programmer has the ability to byte-align binary and floating-point data in Assembler Language programs, in ANS COBOL programs (by omitting the SYNCHRONIZED clause), in PL/I programs (by specifying the UNALIGNED attribute), and in FORTRAN programs. Note that OS still expects parameters passed to it to be properly aligned.

1401/1440/1460, 1410/7010 Compatibility Feature. Two integrated emulator programs will be provided, one to emulate 1401, 1440, and 1460 programs and the other to emulate 1410 and 7010 programs. (Emulator programs are discussed in Section 40.)

OS/DOS Compatibility Feature. An OS DOS Emulator program will be provided to support emulation of a DOS system. Section 40 discusses this emulator.

New console devices. The 3210 Console and 3215 High-Speed Console are supported as the primary operating system console device. A remote 3210 Console is supported as an alternate or an additional console. (The MCS option is required to support the latter.)

Channels. One or two byte multiplexer channels will be supported for a total of up to 512 subchannels per system. Selector and block multiplexer mode are supported also. During IPL, channel mode for all installed high-speed channels is established via a control register channel mode bit setting based on system generation channel definitions. (The channel mode bit was discussed in Section 10:20.) The operator does not have the option of changing this mode at IPL, nor does the control program change the mode setting during system operation.

The 3330 facility. The 3330 facility will be supported as an I/O device for most of the same functions as is the 2314 facility. The error recovery routine provided for the 3330 will include support of the new hardware error correction features.

RPS will be supported in MFT and MVT environments as follows.

- The stand-alone seek issued within the I/O supervisor (IOS) will be eliminated for RPS devices (3330 facilities). IOS will continue to issue stand-alone seeks for direct access devices without RPS. IOS also will be capable of recognizing the channel available interrupt.

- Access method support of RPS commands (SET SECTOR and READ SECTOR) will be provided by:

QSAM and BSAM for all record formats and functions supported for the 3330 facility except the undefined track overflow record format

ISAM for all updating and verification and QISAM sequential processing
BPAM for directory and member processing operations where possible
BDAM for direct retrieval and update of fixed-length standard and VBS format records without key and for write verification of all BDAM format records

- End-of-volume (EOV) routines will support concatenation of data sets residing on RPS and on non-RPS devices. The control program will ensure that an RPS access method is used for drives with the feature and that a non-RPS method is used for drives without the feature.

- Any system utility, data set utility, or IBM-supplied processing program (such as a language translator) that uses the sequential access methods will support RPS. In addition, IEHMOVE, IEBCOPY, and the initialize/dump/restore utility (IEHDASDR) will include RPS support for 3330 facilities.

- The Sort/Merge (program product) supports RPS for 3330 intermediate work devices.

- Where appropriate, RPS commands for access to certain SYSRES data sets will be supported by:

  Data set catalog routines
  Direct Access Device Space Management (DADSM) routines (for DSCB processing)
  STOW, BLDL, and FIND processing of program library (PDS) directory entries
  OPEN/CLOSE/EOV processing of JFCB's in the job queue
  Routines that access the job queue

  Note that RPS command support is not provided for:

  The telecommunications access method (TCAM) for message queues
  The stand-alone disk initialization and alternate track assignment routines (DASDI and ATLAS)

The 2305 facility. The 2305 facility will be supported as an I/O device for most of the same functions as is 2303 Drum Storage.

Rotational position sensing for 2305 facilities will be supported as discussed for the 3330 facility except that an arm positioning seek is not required on 2305 modules and the 2305 is not supported as an intermediate work unit by the Sort/Merge programs. Multiple requesting will be handled by the I/O supervisor, which will initiate up to seven channel programs on one 2305 module at a time. (The eighth logical device address is reserved for control purposes.) Multiple I/O operations to the same data set will be initiated if the data set is not being sequentially processed. (One operation must complete successfully before the next can be initiated during sequential processing.)

Note that specification of exchange buffering for a QSAM data set on either the 3330 or the 2305 facility results in a default to simple buffering.

3211 Printer with tapeless carriage. The 3211 Printer, with or without the 18 additional print positions, will be supported by QSAM and BSAM for exactly the same functions as is the 1403 Printer. In addition, the control program will handle loading of the forms control buffer (FCB) with carriage control images. This support is similar to that provided for Universal Character Buffer (UCB) loading.

The user can define one or more default FCB images at system generation time. Two IBM-supplied default images are included automatically. All other FCB images to be used must be defined by the user and placed in SYS1.SVCLIB, as is the case with UCB images. User-supplied default images must be identified as defaults. The FCB image to be used by a processing program can be specified in the 3211 Printer DD statement included for the job step and will be loaded into the FCB by the control program.

The FCB image currently loaded can also be changed by the programmer during execution of the processing program by use of an Assembler Language macro. If the DD statement does not specify an FCB image and the image currently loaded is not one of the defaults specified at system generation, the operator is requested to specify the FCB image to be used.

The FCB image (and the UCS character image) to be loaded for a 3211 Printer used by an output writer can be indicated in the output writer procedure or in the START output writer command issued by the operator. FCB and UCB images can also be specified in the SYSOUT DD statement for a data set that is to be printed by the output writer, and they will be loaded into the 3811 control unit prior to the printing of the data set.

Any time the FCB parameter is used, as described above, the user can specify that operator verification of forms alignment is to be requested by the control program via a console message when the buffer is loaded. The operator must respond to this message.

The 3211 error recovery routine will retry a print operation after a parity check occurs in the UCB or print line buffer if QSAM is used and three I/O buffers are provided for the printer data set. When the operation is retried, the 3811 control unit insures that only the print positions that did not print correctly the first time are reprinted.

30:15 DOS SUPPORT

DOS will be modified in future releases so that it supports certain Model 155 hardware features. Appropriate alteration of the DOS supervisor generated for a Model 155 will accommodate the fixed storage area of lower storage in the Model 155.

DOS support of Model 155 features will be provided as follows. Programming systems support of RAS features is discussed in Section 50.

New instructions. Assembler D will include mnemonics for all the new instructions so that they can be used in user-written Assembler Language programs. The DOS high-level language translators currently available will not generate the six new general purpose instructions.

Extended precision floating-point. Mnemonics for extended precision instructions and data formats will be added to Assembler D. The DOS high-level language translators currently available do not support extended precision.

Interval timer. The timer will be supported in the same manner as it is currently, for time of day and time intervals.

Time of day clock. This clock is not supported for time of day values.

Byte boundary alignment. The programmer has the ability to byte-align binary and floating-point data in Assembler Language programs, in ANS COBOL programs (by omitting the SYNCHRONIZED clause), and in PL/I programs (by specifying the UNALIGNED attribute).

1401/1440/1460, 1410/7010 Compatibility Feature. Two integrated emulator programs will be provided, one to emulate 1401/1440/1460 programs and the other to emulate 1410/7010 programs. (See Section 40 for a complete discussion of these emulator programs.)

New consoles. The 3210 Console and the 3215 High-Speed Console Printer-Keyboards are supported as the DOS console device. A remote 3210 Console is not supported.

Channels. A single byte multiplexer channel with up to 256 subchannels and selector channel mode are supported. A second byte multiplexer channel and block multiplexer mode are not supported.

New direct access devices. The 3330 and 2305 facilities are not supported.

3211 Printer. This printer, with or without the 18 additional print positions, will be supported in the same manner as is the 1403 Printer. Forms control Buffer and Universal Character Buffer loading for the 3211 will be handled in the same way. The user must execute an IBM-supplied buffer load utility program (SYSBUFDL) as a job step in order to load the FCB and/or the UCB. No provision has been made for loading the FCB or UCB during execution of a job step. User-defined UCB images must be loaded from the core image library. FCB images can be loaded from cards or the core image library.

If a command retry indication is present, the 3211 error recovery routine supports retry of an operation that failed. This option must be requested by the user in the DTF for the 3211 Printer.

being full (199 cylinders per 2311 and 2314, 403 per 3330). Note that 2311 drives without track overflow cannot be used to emulate 1302 and 2302 Disk Storage.

The Model 155 integrated OS 1410/7010 Emulator program supports the same facilities and I/O devices as the stand-alone 1410/7010 emulator for System/360 models except for the 51-Column Card and Selective Stacker special features on the 1402 Card Read Punch.

Table 40.05.1. 1410/7010 system features supported and unsupported by the Model 155 OS 1410/7010 Emulator program

1410 Features	7010 Features
Supported	Supported
All basic CPU functions	Standard 7010 instruction set with store and restore status
Core storage up to a maximum of 80,000 positions	Main storage up to a maximum of 100,000 positions
Inverted Print Edit	Floating Point Arithmetic
Priority Processing	Processing Overlap
Processing Overlap	Priority Feature
One or two channels	Inverted Print Edit
	One to four channels
Unsupported	Unsupported
The 1400 Diagnostic instruction Branch on Tape Indicate	1401/1410 Compatibility Mode
	Diagnostic instruction branch
	Program Relocation
	Storage Protection
	Interval Timer

Table 40.05.2. IBM 1410/7010 I/O devices and features emulated by the OS 1410/7010 Emulator program and their Model 155 equivalents

1410/7010 I/O Device	Model 155 I/O Device
• 1402 Card Read Punch. The following features are not emulated: Select Stacker Column Binary 51-Column Card Programmed reading from more than one reader or punching on more than one punch within a program is not supported.	• Any card reader, card read punch, magnetic tape unit, or direct access device supported by OS QSAM
• 1403 Printer. Programmed printing on more than one printer within a program is not supported.	• Any printer, magnetic tape unit, or direct access device supported by OS QSAM. A printer must have the UCS feature.
• 729 Model II, IV, V, and VI Magnetic Tape Units. 7330 Magnetic Tape Unit. (Compressed tapes are not supported.)	• Any tape unit or direct access device supported by OS BSAM. VBS format is used for 1410/7010 tape files emulated on a direct access device. Seven-track tapes must be emulated on tape units with a seven-track head. The tape control unit must have the Seven-Track Compatibility and Data Convert features if EBCDIC is used.
• 1415 Console	• Any operator's console supported by OS.
• 1301 Disk Storage Model 1 or 2. 1302 Disk Storage Model 1 or 2. 2302 Disk Storage Model 1 or 2. All features emulated except Write Disk Check (treated as a no-op) and operations involving the CE tracks. Write verification can be requested in the OS job control statement for the emulated disk device.	• Any direct access storage device supported by OS BDAM. A maximum of 20 simulated arms per channel are supported. If two or more System/370 direct access devices are required to emulate one 1410/7010 disk device, all Model 155 disk devices used to emulate that device must be of the same type. The 2311 cannot be used to emulate 1302 or 2302 Disk Storage unless the Track Overflow feature is present.

Table 40.05.3. IBM 1410/7010 I/O devices not supported by the Model 155 OS 1410/7010 Emulator program

1311 Disk Storage Drive	1412, 1419 Magnetic Character Reader
1405 Disk Storage	7340 Hypertape Drive
1011 Paper Tape Reader	Teleprocessing devices
1012 Tape Punch	Audio response units

Table 40.05.6. IBM 1401/1440/1460 I/O devices and features emulated by the OS 1401/1440/1460 Emulator program and their Model 155 counterparts

1401/1440/1460	Model 155 I/O Device
• 1402, 1442 Card Read Punch 1442 Card Reader. The following features are not emulated: Column Binary (1402) 51-Column Card (1402) Punch-Feed Read (1402) Read-Punch Release (1402) Card Image (1402) Punch-Column-Skip (1442) Read and punch same card (1442) Selective Stacker (1442) Programmed reading from more than one reader or punching on more than one punch within a program is not supported.	• Any card reader, card read punch, magnetic tape unit, or direct access device supported by OS OSAM
• 1443, 1403 Printer. The Selective Tape Listing feature and programmed printing on more than one printer are not supported.	• Any printer, magnetic tape unit, or direct access device supported by OS QSAM. A printer must have the UCS feature.
• 729 Model II, IV, V, and VI Magnetic Tape Units. 7330, 7335 Magnetic Tape Units. (Compressed tapes are not supported.)	• Any tape unit or direct access device supported by OS BSAM. VBS format is used for 1400 tape files emulated on a direct access device. Seven-track tapes must be emulated on tape units with a seven-track head attached to a tape control unit with the Seven-Track Compatibility and Data Convert features.
• 1407 Console Inquiry Station. 1447 Console. The Branch on Buffer Busy feature (1447) is not supported.	• Any operator's console supported by OS.
• 1301 Disk Storage (only one access arm). 1311 Disk Storage Drive. 1405 Disk Storage Models 1 and 2. Up to five 1311 drives and one 1301 module or one 1405 Model 1 or 2 can be emulated. All features are supported except Write Disk Check (treated as a no-op). Write verification can be requested in the OS job control statement for the emulated disk device.	• Any direct access device supported by OS BDAM. If two or more System/370 direct access devices are required to emulate one 1400 disk device, all Model 155 disk devices used to emulate that device must of the same type.

Table 40.05.7. 1401/1440/1460 I/O devices and features not supported by the Model 155 OS 1401/1440/1460 Emulator program

1400 I/O Device	1400 Feature
1404 Printer 1444 Card Punch 1445 Printer 1011 Paper Tape Reader 1012 Tape Punch Optical readers Magnetic character readers 7340 Hypertape Drive Teleprocessing devices	1401 Model G Binary Transfer

Table 40.05.8. Model 155 direct access device requirements for emulation of 1401/1440/1460 disk devices using OS with and without the track overflow (T.O.) feature. Number of packs required and number of remaining available cylinders on the last pack are shown by the first and second rows of figures, respectively, for each entry. Two figures shown in the number of System/370 drives column indicate that more than one 1400-series device can be emulated on a single Model 155 disk drive.

1401/1440/1460 Disk Device	Number of Model 155 Drives Required per 1400 Device					
	2311 Disk Drives		2314 Disk Drives		3330 Disk Drives	
	Without T.O.	With T.O.	Without T.O.	With T.O.	Without T.O.	With T.O.
1405 Disk (Model 1)	2 64	2 82	2:1 31	2:1 35	8:1 19	8:1 22
1405 Disk (Model 2)	4 131	4 160	1 31	1 35	4:1 2	4:1 22
1311 Disk (Sector mode)	1 99	3:1 6	11:1 12	11:1 12	38:1 3	43:1 4
1311 Disk (Track mode or both track and sector mode)	1 99	2:1 24	7:1 24	8:1 22	30:1 8	33:1 0
1301 Disk (Sector mode)	6 194	4 158	1 32	1 37	3:1 87	4:1 36
1301 Disk (Track mode or both track and sector mode)	6 194	4 48	2 148	1 10	3:1 7	3:1 77

40:10 DOS 1401/1440/1460 AND 1410/7010 EMULATOR PROGRAMS

FEATURES COMMON TO BOTH EMULATORS

The Model 155 continues the advantages of integrated emulation for DOS CS/30 and CS/40 users. In addition, these advantages are now extended to users of 1410/7010 stand-alone emulation.

2. Spanned variable-length record format, which is produced by the Tape Preprocessor formatting program or the emulators

Either format can be produced as output by the emulators.

Processing tape files in spanned variable-length record format provides several advantages:

- Blocking short records reduces the time for emulating I/O operations.
- The Tape Preprocessor or the Tape Postprocessor program can be run concurrently with the emulators in a multiprogramming system.
- Files in spanned variable-length record format can be used by other Model 155 programs if the programs provide for handling the 1400/7010 label records and 1400/7010 tapemark records.
- The Tape Postprocessor program can be used to convert a file in spanned variable-length record format back to 1400 format for use on a 1400/7010 system.

Tape files in spanned record format have standard DOS labels; 1400/7010 labels are treated as data records, since they are processed by the 1400/7010 program. The 1400/7010 tapemarks appear as special data records and are recognized by the emulators.

The character codes supported by the emulators for magnetic tape data are:

- BCD representation in even and odd parity for seven-track tape (data translator on) in 1400 format
- BCDIC-8 representation for nine-track tapes in either 1400 or spanned record format, and for seven-track tapes (data converter on) in spanned record format. This character code, which is the eight-bit representation of BCD, is used to simulate parity. In normal mode, bit 1 is set to one for even parity, to zero for odd parity. In alternate mode, bit 1 is always set to one and no distinction is made between even and odd parity.

Two tape formatting programs are available for converting tape files to and from spanned record format. They are distributed to run as problem programs in the background partition under DOS control and require a partition size of 6K plus buffer areas.

The tape preprocessor program converts seven-track or nine-track tapes in 1400 format to seven-track (data converter on) or nine-track tapes in spanned variable-length record format with standard DOS labels. The tape postprocessor converts seven-track or nine-track tapes in spanned record format to seven-track or nine-track tapes in 1400 format.

Disk files in 1400 format, which are created on a 1400/7010 system or under stand-alone emulation, must be converted to a standard fixed-length record format on 2311 or 2314 disk packs before emulation. Disk files created under CS/30 and CS/40 can be processed by the 1401/1440/1460 emulator if the CS option is specified at emulator generation.

Existing 1400 utilities and the DOS Clear Disk utility program are used to convert disk files in 1400 format, and CS/30 and CS/40 files if desired, to the standard record format.

Each Model 155 disk record represents one 1400 disk track. Each Model 155 disk record is a fixed-length record, its length being a

function of the emulated 1400/7010 device and mode rather than the amount of 1400/7010 data on each track. A 1400/7010 disk file can occupy one or more extents on Model 155 disk packs but only one extent per pack. Extents must be allocated complete cylinders. When a file requires more than one Model 155 disk pack, the packs must be the same type. Two different 1400/7010 files may be placed on the same disk pack but this arrangement may increase seek time if both files are processed at the same time.

Character codes supported by the emulators for disk files are:

- EBCDIC representation for disk operations in move mode
- BCDIC-8 representation for disk operations in load mode. (Data written in load mode must be converted to EBCDIC if it is to be used by programs other than the emulators.)

To convert disk files in 1400 format, or CS/30 and CS/40 disks if desired, to a standard format on a Model 155 disk, the user must dump and restore his data as follows:

1. Dump the disk device, using a 1400/7010 disk-to-tape or disk-to-card utility program. When converting files on 1301, 1311, 1405, or 2302 disk devices that were created on a 1400/7010 system, the utility is executed on the system used to create the file. When converting files on 2302, 2311, or 2314 disks that were created under stand-alone emulation, CS/30, or CS/40, the utility is executed on a System/360 under control of the emulator used to create the disk file.
2. Use the DOS Clear Disk utility program to format previously initialized 2311 or 2314 disk pack(s) for the data.
3. Restore the data to a formatted 2311 or 2314 disk pack, using a 1400/7010 tape-to-disk or card-to-disk utility program under control of a Model 155 emulator. The 1401/1440/1460 emulator is used to restore 1401/1440/1460 data; the 1410/7010 emulator to restore 1410/7010 data.

DOS 1401/1440/1460 EMULATOR SUPPORT

For the DOS CS/30 and CS/40 user, the Model 155 DOS 1401/1440/1460 emulator continues the advantages of integrated emulation and provides additional advantages, such as:

- Emulators operating concurrently in all three partitions (now a restriction for the CS/30 user)
- Simulated 1400 storage that can begin at any address (now a restriction for the CS/40 user)
- Support for CS/30 and CS/40 disk and tape files
- System/370 data formats for emulator tape and disk files
- Preformatting of disk packs used for output is not necessary
- Added emulator control available to user at execution time
- DOS data management facilities and standard disk and tape label processing

The size of the partition required for emulation depends on the 1400 system being emulated, including standard and special features, input/output devices, buffers, etc. The processor storage required for the 1401/1440/1460 emulator is equal to the combined sizes of:

- Simulated 1401/1440/1460 storage. Each position of 1400 storage is simulated in one byte of Model 155 storage (for example, 8000 positions = 8000 bytes).
- Emulator routines required to emulate the 1401/1440/1460 system instructions, features, and I/O operations
- Tape, disk, and unit record buffers. The number and size of tape and disk buffers are specified by the user.

Estimated minimum 1401/1440/1460 emulator processor storage requirements for emulation of a 1400 system with unit record operations only, unit record/tape operations, or unit record/tape/disk operations are shown below.

Emulated Operations	DOS Partition Size (bytes)
1401/1440/1460 unit record	16K + 1401/1440/1460 core size + buffers
1401/1440/1460 unit record/tape	20K + 1401/1440/1460 core size + buffers
1401/1440/1460 unit record/tape/disk	24K + 1401/1440/1460 core size + buffers

The 1400 CPU features and 1400 I/O devices and special features supported and the Model 155 devices used for 1401/1440/1460 emulation are given in Tables 40.10.1 and 40.10.2. Table 40.10.3 lists the 1400 I/O devices that are not supported.

Table 40.10.1. 1401/1440/1460 I/O device and feature support and corresponding Model 155 devices

1401/1440/1460 Device and Features	Corresponding Model 155 Device
1402, 1442, 1444 Card Read Punch Features supported • Column Binary • Card Image • 51-Column Interchangeable Read Feed • Punch Feed Read • Punch Column Skip • Stacker Select • Processing Overlap Features not supported • Read Punch Release • Multiple card reader/punch operations	1442, 2520, 2540 Card Read Punch and 2501 Card Reader Note: Card reader and card punch operations may be emulated using a magnetic tape or direct access storage device
1403, 1404, 1443 Printer Features supported • Processing Overlap • Space Suppression Features not supported • Selective Tape Listing • Multiple printer operations • Read Compare	1403, 1443 Printer Note: Printer operations may be emulated using a magnetic tape or direct access storage device
1407, 1447 Console	3210 or 3215 console printer-keyboard
729, 7330, 7335 Magnetic Tape Unit Features supported • Column Binary • Processing Overlap Features not supported • Compressed tape	2400 series magnetic tape • Seven-Track Compatibility feature is required if processing seven-track tapes
1301, 1311, 1405 Disk Storage Features supported • Direct Seek • Scan Disk • Track Record • Additional access arm (1405) Note: A 1405 cannot be emulated in combination with a 1301 or 1311	2311, 2314 direct access devices

Table 40.10.2. 1401/1440/1460 CPU features supported

Core storage from 1,400 to 16,000 positions. The 1401 Model G is not emulated.	Column Binary
Expanded Print Edit	Sense Switches
Inverted Print Edit	Advanced Programming
High-Low-Equal Compare	Indexing and Store Address Register
Multiply-divide	Bit Test

Table 40.10.3. Unsupported 1401/1440/1460 devices

1445 Printer	7340 Hypertape Drive
1011 Paper Tape Reader	1428 Alphameric Optical Reader
1012 Tape Punch	1231 Optical Mark Page Reader
1412 Magnetic Character Reader	1285 Optical Reader
1418 Optical Character Reader	Teleprocessing devices
1419 Magnetic Character Reader	

Emulator performance will vary depending on user options, such as number and size of buffers, the instruction mix of the 1401/1440/1460 programs, the format of tape files, and the priority of the partition in which the emulator is running.

Emulator performance is improved by:

1. Using double buffers and spanned record format for tape files in lieu of single or shared buffers and 1400 record format. (A shared buffer can be used by more than one I/O device.)

2. Using single buffers rather than shared buffers for disk files

3. Specifying device independence for emulating unit record operations on a magnetic tape or direct access storage device

4. Using a card reader that is not equipped with the 51-Column Interchangeable Read Feed and Column Binary features and not using the Select Stacker instruction

DOS 1410/7010 EMULATOR SUPPORT

The Model 155 DOS 1410/7010 emulator offers the 1410/7010 stand-alone emulator user the advantages of integrated emulation already discussed.

Main Storage Requirements

The size of the partition required for emulation depends on the 1410/7010 system being emulated, including standard and special features, input/output devices, buffers, etc. The processor storage required for the 1410/7010 emulator is equal to the combined sizes of:

- Simulated 1410/7010 storage. Each position of 1410/7010 storage is simulated in one byte of Model 155 storage (for example, 20,000 positions = 20,000 bytes).

- Emulator routines required to emulate the 1410/7010 system instructions, features, and I/O operations

- Tape, disk, and unit record buffers. The size and number of tape and disk buffers are specified by the user.

Estimated minimum 1410/7010 emulator processor storage requirements for emulation of a 1410/7010 system with unit record/tape operations or unit record/tape/disk operations are shown below.

Emulated Operations	DOS Partition Size (bytes)
1410/7010 unit record/tape	23K + 1410/7010 core size + buffers
1410/7010 unit record/tape/disk	39K + 1410/7010 core size + buffers

The 1410/7010 CPU features and 1410/7010 I/O devices and special features supported and the Model 155 devices used for 1410/7010 emulation are given in Tables 40.10.4 and 40.10.5. Table 40.10.6 lists the 1410/7010 I/O devices that are not supported.

Table 40.10.4. 1410/7010 I/O devices and features and corresponding Model 155 devices

1410/7010 Device and Features	Corresponding Model 155 Device
1402, 1442 Card Read Punch Features not supported Stacker Select 51-Column Interchangeable Read Feed	1442, 2540, 2520 Card Read Punch and 2501 Card Reader Note: Card reader and card punch operations may be emulated using a magnetic tape or direct access storage device.
1403 Printer All standard operations	1403, 1443 Printer Note: Printer operations may be emulated using a magnetic tape or direct access storage device.
1415 Console All standard operations	3210 or 3215 console printer-keyboard
729, 7330 Magnetic Tape Units All standard operations	2400-Series Magnetic Tape Units Note: Seven-Track Compatibility feature is required for processing seven-track tapes.
1301, 1302, 2302 Disk Storage All standard operations Note: Any combination of 1301 and 1302/2302 disk storage drives can be emulated.	2311, 2314 direct access devices Note: An emulated 1302/2302 record will not fit on a 2311 disk track.

Table 40.10.5. Supported and unsupported 1410/7010 CPU features

Supported	Unsupported
Main storage up to 80,000 positions (1410) and 100,000 positions (7010) Inverted Print Edit Priority Feature Processing Overlap Channels one through four Floating Point Arithmetic	1401/1410 Compatibility Mode 7010 Diagnostic instruction, Branch on C Bit Diagnostic instruction, Branch if Tape Indicator J(I)K 7010 Memory Protect and Program Relocate 7010 Interval Timer

Table 40.10.6. Unsupported 1410/7010 devices

1311 Disk Storage Drive	1419 Magnetic Character Reader
1405 Disk Storage	7340 Hypertape Drive
1011 Paper Tape Reader	2321 Data Cell Drive
1412 Magnetic Character Reader	Teleprocessing devices

Emulator performance will vary, depending on user options, such as number and size of buffers, the instruction mix of the 1410/7010 program, the format of tape files, and the priority of the partition in which the emulator is running.

Emulator performance is improved by:

1. Using double buffers and spanned record format for tape files in lieu of single or shared buffers and 1400 record format. (A shared buffer can be used by more than one I/O device.)

2. Using single buffers rather than shared buffers for disk files

3. Emulating unit record operations on a magnetic tape or direct access storage device

40:15 OS DOS EMULATOR PROGRAM

The availability of the OS DOS emulator offers current DOS users who upgrade to a Model 155 the opportunity to convert to an OS operating environment more easily than is possible without the use of emulation. In addition, the OS DOS emulator user can benefit from the use of integrated emulation since the OS DOS emulator can execute concurrently with other OS jobs.

The OS DOS emulator for the Model 155 is a combination of the OS DOS emulator processing program and the optional OS/DOS Compatibility feature. This feature provides the relocation necessary for execution of a DOS supervisor and DOS programs under OS control in any processing program storage location. An OS MFT or MVT control program generated for a Model 155 is required also.

The OS DOS emulator and the DOS system being emulated (DOS supervisor and up to three processing program partitions) execute together in an MFT partition or MVT region, which must be a minimum of 38K. The OS DOS emulator program and tables require 22K plus another 4K if I/O staging is used. Additional OS DOS emulator program storage may be required depending on the I/O devices used. Up to ten I/O devices are supported in 22K, and 250 bytes are required for each additional device. The 4K I/O staging figure supports unblocked reader, printer, and punch records and residence of the required QSAM routines in the OS DOS emulator partition or region.

The DOS system being emulated can be 16K, 24K, or 32K and up in 4K increments. The OS DOS emulator is scheduled to operate in the same manner as any other OS job, and one or more OS DOS emulator jobs can execute concurrently with OS jobs if enough I/O devices and processor storage are available. In addition, the Model 155 OS 1401/1440/1460 and 1410/7010 emulator programs can execute concurrently with the OS DOS emulator if enough resources are present.

The user need not make any changes to the existing DOS supervisor, job control statements, tape files, or disk files in order to use the OS DOS emulator. Modification of existing DOS programs is required only for programs that contain features unsupported by the OS DOS emulator.

The major advantages of the OS DOS emulator are the following:

- Transition from a DOS to an OS operating environment is smoother. The conversion of DOS source programs, job control, and data files to OS formats can be done gradually for emulated DOS jobs.

- Model 155 OS DOS emulator users can continue to use most IBM-supplied application programs (Type II and program products) that operate under DOS but not OS and do not use BTAM or QTAM, by emulating them under OS.

- Dedicated emulation is not required, thus allowing the user to take advantage of OS facilities.

- Total system throughput is increased by operation of the OS DOS emulator in a multiprogramming environment and by using the staged I/O option of the OS DOS emulator. The latter permits emulated DOS programs to use the data transcription facilities of the OS reader interpreter and output writer to handle their unit record functions. Use of the staged I/O option of the OS DOS emulator also eliminates the necessity of dedicating unit record devices to DOS emulation.

All operating environments, control program facilities, and I/O devices supported by DOS can be emulated, with the following exceptions:

- Autotest

- Model-dependent functions such as CS/30, CS/40, and the DIAGNOSE instruction (1400 emulation can be handled using the Model 155 OS 1401/1440/1460 Emulator Program)

- Emulation of emulators that operate under DOS, for example, Model 155 integrated 1400/7010 emulators that operate under DOS

- 1259, 1412, and 1419 Magnetic Character Readers

- Teleprocessing devices (including the 2260 Display Station)

- Storage protection within the DOS system being emulated (among the DOS supervisor and partitions)

- DOS volumes having non-unique volume serial numbers online concurrently

In addition, the OS DOS emulator cannot handle DOS executable programs that:

- Rely on known timing relationships of the DOS system

- Depend on HALT I/O, READ DIRECT, WRITE DIRECT, AND DIAGNOSE instructions for their operation

- Require more than two bytes of sense data for an I/O device

- Use the PCI flag in a CCW

- Modify or use information in CCW's after the CCW list is initiated with a START I/O instruction and before the I/O operation terminates

- Initiate the same CCW list for an I/O operation on more than one I/O device concurrently

While a pseudo interval timer is maintained at simulated DOS decimal location 80, accurate time of day is not guaranteed because the timer is running only when the OS DOS emulator partition/region is executing and a time lag occurs during the interval required to update the timer.

The following I/O devices are supported by the OS DOS emulator:

- 1403, 1404, 1443, 1445 Printers
- 1052 Printer-Keyboard
- 1285, 1287, 1288 Optical Readers
- 1442, 2520, 2540 Card Read Punches
- 2501 Card Reader
- 2311 Disk Storage Drive
- 2314 Direct Access Storage Facility
- 2321 Data Cell Drive
- 2400-series magnetic tape units
- 2671 Paper Tape Reader
- Any new devices that are supported by both DOS and OS, subject to the programming restrictions stated

EMULATOR JOB SUBMISSION AND GENERAL OPERATION

DOS emulation is initiated as a single-step OS job via the input stream. An OS DOS emulator job can consist of one or more DOS jobs. The OS DOS emulator program, which must reside in SYS1.LINKLIB or a user job library, is specified in the EXEC job control statement included in the job control for the OS DOS emulator job. The following also must be identified in the DD job control statements for the OS DOS emulator job:

1. The DOS system residence and operator console devices
2. The location(s) of the DOS input stream(s)
3. I/O assignments for the staging of DOS unit record I/O operations
4. All the I/O devices that will be used by the DOS programs that are emulated as part of this DOS emulator job

The DOS system background partition input stream can be located in the OS input stream or on a separate data set. DOS batch-initiated foreground (BJF) partition input streams must be located in separate data sets.

If enough Model 155 processor storage is available, I/O staging can be used to increase OS DOS emulator job throughput and reduce the number of devices that have to be dedicated to the DOS emulation partition or region. It allows DOS unit record files SYSRDR, SYSPCH, and SYSLST to be emulated on direct access devices using the OS reader interpreter and output writer. DOS job control statements (for the BG partition) and/or card input to DOS programs to be emulated can be placed in the OS input stream and will be transcribed by the reader interpreter to SYSIN data sets on direct access devices. Thus, emulated DOS jobs steps will obtain their card input from OS SYSIN disk data sets. Output from emulated DOS programs can be placed in OS SYSOUT data sets on disk to be transcribed to the printer or punch by an output writer.

The following should be noted about the use of I/O staging. In OS, a job is not placed in the input queue, from which all jobs are scheduled, until the entire job (job control and input stream data for the job) has been read by the reader interpreter. Similarly, SYSOUT data sets produced during job step execution are not placed in the output queue for transcription by an output writer until job termination.

Thus, if all DOS jobs to be emulated are grouped together as a single OS DOS emulator job, DOS emulation cannot begin until all DOS

jobs (and their input stream data) have been read by the reader interpreter, and none of the SYSOUT data sets from completed emulated DOS jobs can be transcribed until the OS DOS emulator job itself terminates (all DOS jobs processed). This negates one advantage of I/O staging, which is the overlapping of unit record input and output data transcription with processing.

Therefore, consideration should be given to grouping DOS jobs into two or more OS DOS emulator jobs that execute one after the other in the OS DOS emulator partition/region. In addition, if the output from a particular DOS job is desired immediately, it should not be staged (written to a SYSOUT data set). The use of multiple OS DOS emulator jobs in an OS DOS emulator partition/region, instead of one, offers an additional advantage in optimizing device usage, as discussed later.

I/O operations and I/O error recovery procedures for emulated DOS programs are handled by the OS control program. All I/O devices to be used by emulated DOS programs must be allocated to the DOS emulation partition or region when the OS DOS emulator job is begun. These devices are dedicated to DOS emulation and cannot be allocated to any other executing OS jobs while DOS emulation is in operation. Thus, direct access devices and their data sets cannot be shared by an OS job step and an emulated DOS program. However, DOS direct access volumes can be shared by DOS partitions being emulated in the same OS DOS emulator partition or region. In addition, the user must ensure that all online OS DOS emulator volumes have unique volume serial numbers with respect to other DOS and OS volumes online at the same time.

Consideration should be given to grouping DOS jobs into multiple OS DOS emulator jobs according to the types and total number of I/O devices required. This can reduce the number of I/O devices that have to be dedicated to a DOS emulation partition or region at any given time, thereby making more devices available to other OS jobs.

When the DOS emulation job is initiated, the DOS emulator program is loaded into the OS DOS emulator partition/region. The DOS emulator program performs control block and table initialization and initiates an IPL from the DOS system residence volume. Once the DOS supervisor has been loaded and has established the DOS partitions, DOS job execution begins. DOS programs are loaded into the defined DOS partitions and emulated. Messages to the operator from the DOS emulator program are issued in standard OS format and include a unique identification to indicate that they are OS DOS emulator messages. If the MCS option is included in the OS control program, all DOS emulation messages can be routed to a specific console, and thus isolated.

The entire OS DOS emulator partition/region operates with a nonzero storage protect key to prevent it from interfering with the OS control program and other executing OS jobs. Therefore, the DOS emulator program, the DOS supervisor, and other DOS jobs in the emulator partition/region are not protected from inadvertent modification by an executing DOS program.

INSTALLATION OF THE OS DOS EMULATOR

The following are the major steps that a DOS user must take to install the OS DOS emulator on a Model 155:

- Data processing personnel -- systems analysts and designers, programmers, operators, etc.-- must be educated on OS

- The installation must decide which level OS control program will be used, MFT or MVT, and which functions and options are to be included.

- The desired OS operating system must be generated using a release of OS that includes Model 155 support. The DOS emulator option must be requested. Installation-designed routines, such as nonstandard tape label processing, accounting, etc., must be written, as required, and added to the generated operating system.

- DOS jobs that cannot be emulated must be converted to OS format. This involves source program changes, conversion of DOS job control statements to OS job control statements, and, depending on data organization, conversion of DOS files to OS data sets. The amount of reprogramming required depends on the source language being used. In general, high-level language programs require much less modification than Assembler Language programs.

- The volume serial numbers of all existing DOS files must be inspected for duplicates and unique serials should be assigned where necessary. Volume serial numbers assigned to newly created DOS files or OS data sets should be unique as well.

- The OS job stream should be planned and consideration should be given to how OS DOS emulator jobs are to be scheduled and executed, as discussed previously in this subsection. Note also that the total storage size of the DOS system being emulated may be reduced. For example, if one DOS processing partition is devoted to teleprocessing, CS/30, or CS/40, which are not emulated by the OS DOS emulator, this DOS partition is no longer required and its storage can be made available for allocation to an OS partition or region.

- Optionally, the size of the emulated DOS system can be reduced by the removal of functions that are now provided by OS. For example, DOS POWER can be removed from a DOS system since data transcription can be handled by the OS reader interpreter and output writer. The model-dependent DOS MCRR and CCH routines can be removed from a DOS supervisor as Model 155 MCH and CCH routines contained in the OS control program will be used for machine and channel error handling.

  Note that alterations affecting the DOS supervisor normally require a system generation to be performed. In addition, any change resulting in a different starting address for a DOS partition means that existing nonrelocatable DOS programs executing in that DOS partition must be link-edited relative to the new address.

Figure 40.15.1 below illustrates a 256K Model 155 configuration that supports one OS processing partition (P2), a transient 44K reader interpreter (in P2), a resident output writer (P0), and emulation of a 128K DOS system (P1) using the staged I/O option.

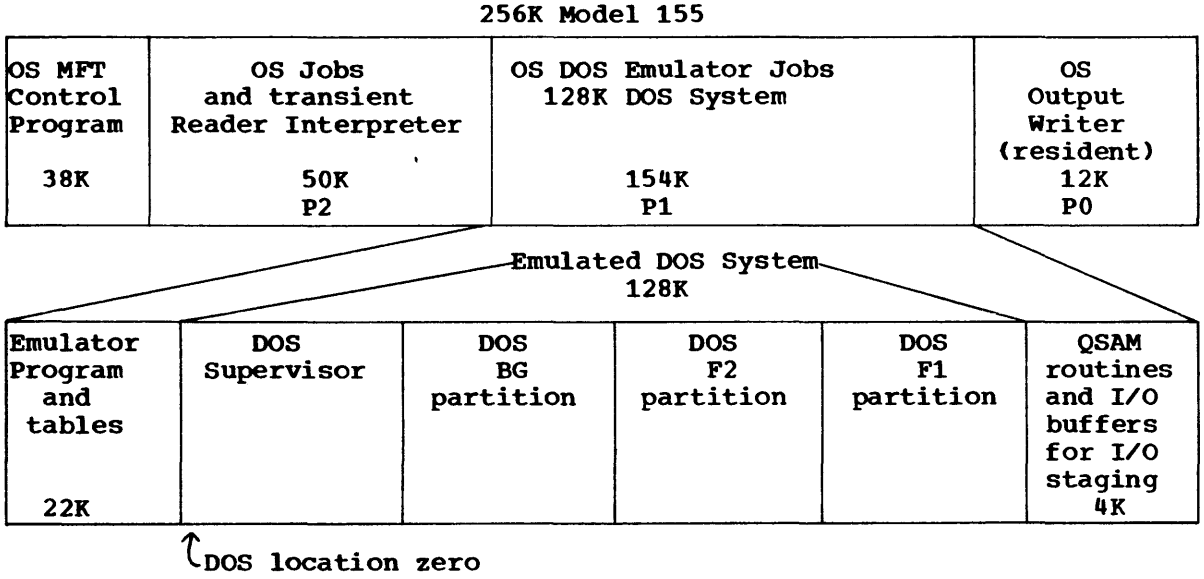


Figure 40.15.1. Sample 256K Model 155 configuration for emulation of a 128K DOS system.

two RMS routines, machine check handler (MCH) to handle machine check interrupts and channel check handler (CCH) to handle certain channel errors, will be included automatically in MFT and MVT control programs generated for the Model 155. Approximately 7000 bytes of resident (nucleus) processor storage is required for Model 155 recovery management. A Model 50 user with a 3K SER1 routine included in the control program will require only a 4000-byte increase in resident control program storage as a result of the inclusion of Model 155 RMS.

The two primary objectives of RMS are (1) to reduce the number of system terminations that result from machine malfunctions and (2) to minimize the impact of such incidents. These objectives are accomplished by programmed recovery to allow system operations to continue whenever possible and by the recording of system status for both transient (corrected) and permanent (uncorrected) hardware errors.

Machine Check Handler

After IPL of a control program containing Model 155 RMS routines, mask bits are enabled and control register values are set to permit all machine check interrupts and logouts to occur.

Soft Machine Checks

MCH receives control after the occurrence of both soft and hard machine check interrupts. When a System Recovery or an Automatic Configuration, accompanied by a System Recovery soft machine check, occurs (successful CPU retry, single-bit processor storage error corrected, or buffer block deleted), MCH formats a recovery report record to be written in the system error recording data set SYS1.LOGREC. This record contains pertinent information about the error, including the data in the fixed logout area, an indication of the recovery that occurred, identification of the job, job step, and program involved in the error, the date, and the time of day. MCH schedules the writing of the recovery report record and informs the operator that a soft machine check has occurred.

Prior to relinquishing CPU control, MCH determines whether or not an automatic mode switch from recording mode to quiet mode should take place if a CPU retry or an ECC correction recovery report has just occurred. The determination of whether to switch to nonrecording (quiet) mode is made on the basis of the number of soft machine checks of a specific type that occur during system operation. Error count thresholds are maintained separately for successful CPU retry and successful processor storage single-bit error corrections. The IBM-supplied threshold values can be altered when the control program is generated or by an operator command during system operation.

MCH switches the system to quiet mode for either ECC corrections only (the DIAGNOSE instruction is used to change the ECC mode bit from full recording to quiet mode) or both CPU retry and ECC corrections (the System Recovery mask bit is disabled). Mode switching occurs if the number of soft machine checks that occur during system operation exceeds the specified error count threshold for that type. The operator is informed of the mode switch and can switch back to recording mode at any time thereafter.

Mode switching is implemented to attempt to prevent SYS1.LOGREC from being filled with recovery reports when a recurring correctable error condition exists that would cause many reports to be generated.

When a buffer block deletion recovery report occurs, MCH records the error and informs the operator but does not maintain a threshold value for implementing quiet mode for this interrupt. The total number of buffer blocks deleted since system operation began is indicated,

and when a significant number of buffer blocks have been deleted, the operator can disable the entire buffer, using the console switch provided, if desired.

The operator also is informed of the occurrence of a Time of Day Clock Damage or an Interval Timer Damage machine check interrupt. Error recording is performed.

Only error recording is required after an External Damage soft machine check interrupt (multiple-bit processor storage error during an I/O operation). I/O error recovery will be performed after the ensuing I/O interrupt. (See Figure 50.10.5 for the general flow of OS MCH processing after soft machine checks.)

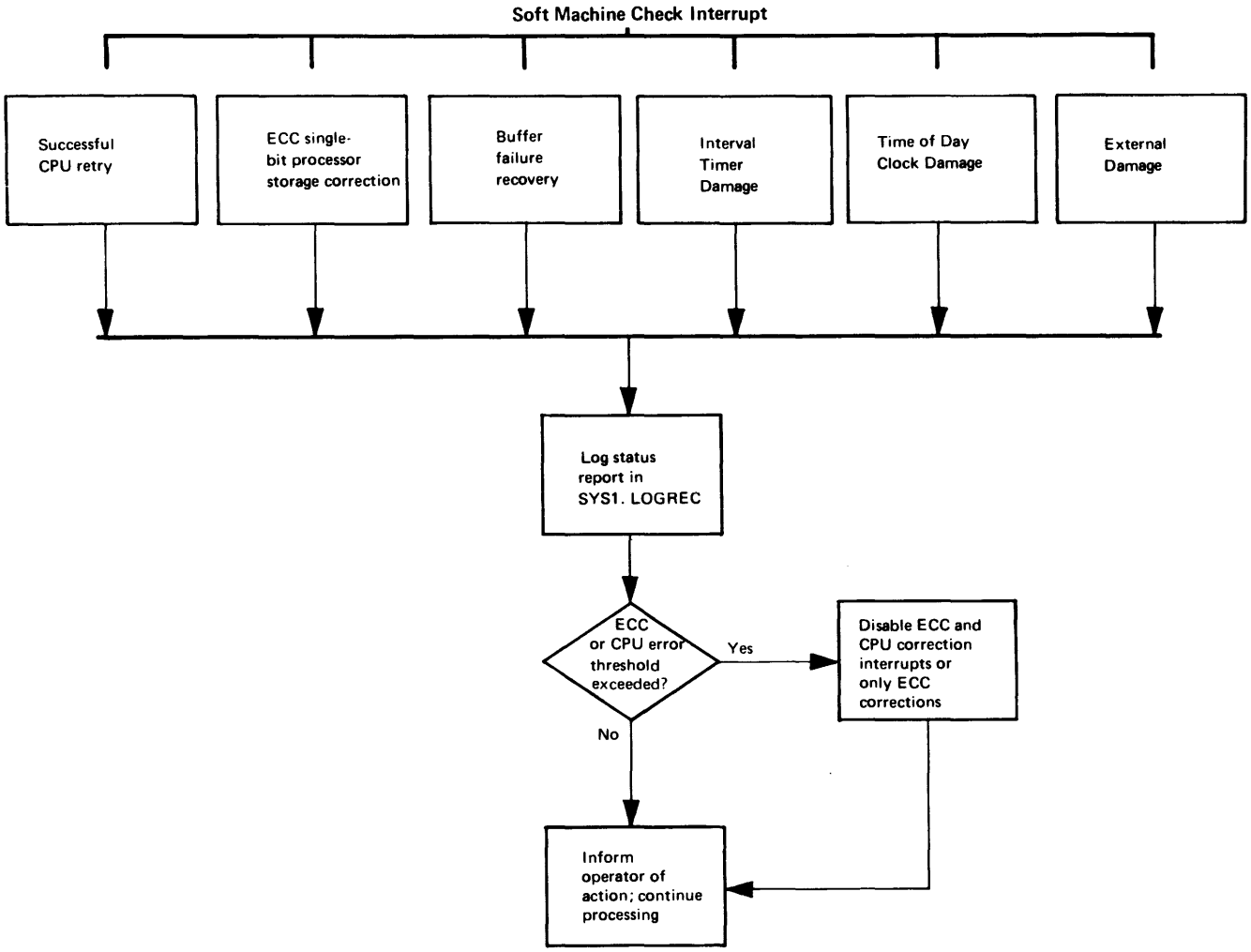


Figure 50.10.5 General flow of OS MCH processing after soft machine check interrupts.

Hard Machine Checks

When an Instruction Processing Damage hard machine check occurs (uncorrectable or unretryable CPU error, multiple-bit processor storage error, or storage protect key failure), MCH determines whether the error is one that is correctable by programming, such as a multiple-bit storage error or a storage protect key failure.

The program damage assessment and repair (PDAR) routine of MCH can repair damaged control program storage areas by loading a new copy

is used and fewer (or more) 3330 tracks are allocated to the data set than before.

Subject to the restrictions stated in Section 10:05 and those indicated for BDAM data sets, existing executable processing programs can be used without change to process data sets that have been transferred to 3336 packs. Nothing need be done to job control for these programs if the cataloged procedures supplied with the language translators are used, as long as the 3330 facility is specified as a SYSDA device at system generation. Otherwise, job control statements must be changed to request 3330 devices and, optionally, any data set characteristic changes, such as block size. RPS support, as described previously, is provided automatically.

User-written programs that use the EXCP level to access disk data sets that have been transferred to 3336 packs may have to be modified to reflect the characteristics of the data set on the 3336, a different number of records per track, a different number of tracks per cylinder, etc. All 2311 and 2314 CCW lists will operate on 3330 facilities except those that are device or channel time dependent and those that support the file scan feature, which is not available on the 3330 facility. User-written 2311 or 2314 error routines will not execute correctly and must be modified. RPS commands have to be added by the user if this support is desired for programs that use EXCP. (Note that the XDAP macro will include support of RPS commands.)

Data sets currently located on 2303 Drum Storage can be placed on a 2305 facility, using a data set utility program. Unit specification in the job control statements of existing programs that will access the 2305 facility, instead of the 2303 drum, must be changed. Also, to reflect the larger capacity of a 2305 track, it may be necessary to alter the block size used. The latter also can be done via job control statement alterations (without program reassembly) unless block size was specified in the program itself.

60:10 PLANNING OPTIMAL SYSTEM PERFORMANCE, USING BLOCK MULTIPLEXER CHANNELS AND ROTATIONAL POSITION SENSING DEVICES

Block multiplexing, rotational position sensing, and multiple requesting provide the user with another tool that can improve total system throughput in the area of multiprogramming. However, the effectiveness of this tool for a given installation depends largely on proper planning for its use. This section indicates how to use block multiplexer channels and RPS devices more effectively.

The guidelines outlined indicate how best to configure a system with rotational position sensing devices, how to plan job scheduling, and what to consider when determining disk data set characteristics. Explanations follow the statement of each guideline.

All guidelines presented are not necessarily practical for all users. Each item should be evaluated in terms of the processing requirements and hardware configuration of an installation.

Guidelines for system configuration and generation are as follows:

1. Multiple 3330 facilities should be placed on a single block multiplexer channel.

   Performance improvement occurs (1) as a result of overlapping the rotational positioning time of disk devices and (2) because more I/O requests can be initiated in a given period of time, since the channel is free more often. When many disk devices are active concurrently on a block multiplexer channel, there is more potential for such overlap.

2. Direct access devices with RPS should be placed on separate channels from I/O devices without RPS. Alternatives are as follows:

   a. If it is necessary to place non-RPS devices on the same block multiplexer channel with RPS devices, give first choice to non-RPS devices with a buffered control unit, such as the 2540 Card Read Punch and the 1403 Printer. These devices disconnect from a block multiplexer channel during the relatively long mechanical portion of their cycle, thereby freeing the channel for other operations.

   b. Tape units should not be placed on a block multiplexer channel with RPS devices unless absolutely necessary, because channel disconnection does not occur during any of their channel operations. If this is not possible, try to plan job scheduling to avoid having jobs using tape units and jobs using RPS support active on a block multiplexer channel at the same time. If this is not feasible, try to assign very low-activity data sets to these tape units.

   A device without channel disconnect capability can monopolize the block multiplexer channel for relatively long periods of time, thereby preventing (1) the initiation of other I/O operations on the channel and (2) the reconnection and completion of disk RPS channel programs already in operation on the channel. For example, a direct access device without RPS retains use of the channel during its search operations as well as during its reads and writes. If the device is a 2314 and block size is half a track, the channel is busy for 25 ms on the average (12.5 ms average rotational delay plus 12.5 ms read/write) for each I/O operation started for the non-RPS 2314 facility. Even if the block size used is relatively small, the channel can still be monopolized by the non-RPS device if there is high activity on the device.

3. The 2305 facility normally should not be placed on a block multiplexer channel with any other device.

   Exclusive use of a channel insures optimum performance of the 2305 facility as a system residence device.

The following should be noted as regards specification of priority and ordered-seek I/O request queuing options for RPS devices at OS system generation. The priority queuing option insures priority I/O request initiation for the device, but because of first-come, first-served handling of I/O operations on the block multiplexer channel, this option does not insure that priority device channel programs will complete sooner than other RPS channel programs that were started later on the channel. However, the objective of specifying the ordered-seek

60:20 DOS TRANSITION

A system generation must be performed using a release of DOS that includes Model 155 support in order to obtain a supervisor that supports new Model 155 features. The existing system generation job stream can be used, modified to reflect the Model 155 hardware configuration and the use of integrated emulator programs, as appropriate. Additional supervisor options can be selected as well.

A DOS operating system generated for the Model 155 includes the following:

- MCAR and CCH routines to handle the expanded machine check interrupt. OBR and SDR are included to handle I/O error recording, and OLTEP is present also.
- Support of the new I/O devices specified (3211 Printer, etc.) and the new Model 155 console specified
- Support of the interval timer, if requested
- Support of the new instructions by Assembler D
- The required interface to the integrated emulator program specified at system generation, if any

In general, the new supervisor will be larger than the one currently in use because of the automatic inclusion of MCAR, CCH, OBR, and SDR routines and user selection of additional options. (The minimum DOS supervisor size for the Model 155 is 14K.) This increase will be less for DOS supervisors that currently contain the optional MCRR, OBR, and SDR routines. A larger supervisor and the availability of additional processor storage in the Model 155 will cause partition starting addresses to change. Therefore, existing user-written, nonrelocatable DOS programs have to be link-edited relative to the new partition starting addresses and placed in the new core image library. If relocatable modules for these nonrelocatable programs are not available, reassembly of the source modules, as well as link editing of the resulting relocatable modules, is required. Existing user-written, self-relocatable DOS program phases can be copied directly from the old core image library to the new one.

Subject to the restrictions stated in Section 10:15, alteration of an existing source program is required only if new processing is added, if existing processing is changed, if there is a change in the I/O device types used in the program (ASSGN job control statements may also require changes), or if the program contains a user-written routine that depends upon a particular release of DOS for communication with the supervisor. (Conversion of emulated programs and files was discussed in Section 40.)

60:25 DOS PORTABILITY

A DOS user with multiple Model 155 systems can generate a single operating system that can be used on each system, subject to restraints imposed by differences in hardware configurations. If a single control program is to be used for both a System/370 Model 155 and a System/360 model, say 40 or 50, Model 155 should be specified at system generation time so that MCAR and CCH are included. (DOS support is not provided for the System/370 Model 165.)

Model 155 MCAR and CCH routines will not execute properly on a Model 40 or 50. When a DOS supervisor containing them is loaded during IPL, MCAR and CCH are disabled automatically by the initialization routine

when the routine determines that it is not operating on a Model 155. (Note that MCAR and CCH cannot be disabled by the operator with the RF parameter when a DOS supervisor containing them operates on a Model 155.) This means that the Model 40 or 50 will run as it would if the optional MCRR routine was not included in the supervisor. That is, there will not be any machine check error recording and the system will go into a wait state when a machine check interrupt occurs. Thus, if the facilities provided by MCRR routines are desired for a Model 40 or 50 supervisor, a system generation must be done for each unique model in the installation so that the appropriate model-dependent machine check routine is included in each supervisor.

As covered in the OS portability discussion, processing programs that are to execute on the Model 155 and a Model 40 or 50 must use instructions, features, and I/O devices common to both systems.

60:30 USE OF OTHER PROGRAMMING SYSTEMS

Subject to the restrictions stated in Section 10:05, users of OS PCP, TOS, BOS, non-IBM supplied control programs, or OS MFT and MVT and DOS control programs not generated for a Model 155 can execute their existing control and processing programs on a Model 155 with a hardware and I/O device configuration comparable to that of the System/360 model now installed. (Certain BPS programs have known timing dependencies that prevent their successful execution on a Model 155.) However, since Model 155 RMS (machine check and channel check routines) are not included in these control programs, the Model 155 will operate under the following conditions:

1. Single-bit processor storage error correction and deletion of malfunctioning buffer block occur; however, they do not cause a machine check interrupt (IPL disables the recovery mask bit).

2. The IPL setting of the recovery mask bit also disables CPU retry correction interrupts. However, the CPU retry facility itself is disabled if a switch on the console (discussed below) is in a certain position.

3. External damage and damage to the time of day clock or the interval timer causes a machine check interrupt condition.

4. A hard machine check error (an unretryable or uncorrectable CPU error, a double- or multiple-bit processor storage error, or a storage protection failure) causes a hard machine check condition and generation of CPU extended logout data.

A machine check control switch, which determines what action is taken when a machine check condition occurs, is present on the system console. When the switch is not in the hard stop position, machine checks cause an interrupt and logout if they are not disabled. This setting is to be used when an operating system containing Model 155 RMS is in operation. When the switch is in the hard stop position, all enabled machine check interrupts cause a hard stop without an interrupt or a logout. In addition, CPU retry is effectively disabled, since detection of a CPU error causes a hard stop before CPU retry is attempted.

If the Model 155 is not set to hard stop after a machine check when an operating system without Model 155 RMS is used, the system takes whatever action was planned for machine checks:

- Any control program without a recovery routine included (for example, SER0, SER1, MCH for OS or MCRR for DOS) will enter the wait state after a machine check interrupt and logout. The logged

Hardware Feature	System/360 Model 40	System/360 Model 50	System/370 Model 155	DOS - Model 155	OS - Model 155
I. CPU					
A. Internal Performance (relative to Model 50)	.44	1	Approximately 3.5 to 4	-	-
B. Instruction set					
1. Standard set (Binary Arithmetic)	Standard	Standard	Standard	All languages	All languages
2. Decimal arithmetic	Optional	Standard	Standard	All languages except FORTRAN	All languages except FORTRAN
3. Floating-point arithmetic	Optional	Standard	Standard	All languages except RPG	All languages except RPG
4. Extended precision floating-point	Not available	Not available	Optional	Mnemonics in Assembler D	Assemblers F and H and FORTRAN H
5. Six new instructions (MOVE LONG, COMPARE LONG, etc.)	Not available	Not available	Standard	Mnemonics supplied for user use in Assembler D	Mnemonics supplied for user use in Assemblers F and H
6. STORE CPU ID, STORE CHANNEL ID, HALT DEVICE instructions	Not available	Not available	Standard	Used by the control program	Used by the control program
C. Buffered instruction fetch	No	No	Yes Three one-word buffers are provided. (Imprecise interrupts do not occur.) One prefetched instruction decoded, no operand prefetching.	-	-
D. Interval timer	Standard (16.6 ms resolution)	Standard (16.6 ms resolution)	Standard (3.33 ms resolution)	1. Time intervals 2. Time of day	Supported except for time of day requests
E. Time of day clock	Not available	Not available	Standard	Not supported	Supported for time of day requests
F. CPU retry by hardware	No	No	Standard	Both successful and unsuccessful hardware retries logged by MCAR	Both successful and unsuccessful hardware retries logged by MCH

Hardware Feature	System/360 Model 40	System/360 Model 50	System/370 Model 155	DOS - Model 155	OS - Model 155
G. Machine check interrupt	Occurs on CPU, main storage, and certain channel errors. One mask bit controls this interrupt.	Same as the Model 40	Occurs after corrected and uncorrected errors. There are seven types of machine check and many are individually maskable.	Soft and hard machine checks are logged. Recovery procedures are performed.	Same as DOS with some differences in recovery procedures performed.
H. Fixed storage area size in lower storage (including logout area for machine and channel errors)	324 bytes	292 bytes	1152 bytes reducible to 512 if the extended logout area of 640 bytes is moved	Data logged is handled by RMS routines	Data logged is handled by RMS routines
I. Compatibility features (all are optional)	1.1401/1460 2.1410/7010 3.1401/1440/1460 DOS Compatibility (for use with CS/40)	1.1410/7010 2.7070/7074 (mutually exclusive features)	1.1401/40/60, 1410/7010 2.OS/DOS compatibility	1. 1401/1440/1460 and 1410/7010 integrated emulator programs provided -	1. Same as DOS 2. An OS DOS emulator is provided
J. CPU cycle time	625 nanoseconds 2-byte parallel data flow	500 nanoseconds 4-byte parallel data flow	115 nanoseconds 4-byte parallel data flow	-	-
K. Control logic	microprogram in tape ROS	microprogram in capacitor ROS	microprogram in capacitor ROS	-	-
L. Direct Control feature	Optional	Optional	Optional	Not supported	Not supported
II. STORAGE					
A. Processor (main) storage sizes	16K 32K 64K 128K 192K 256K	- - 64K 128K - 256K 384K 512K	- - - - - 256K 384K 512K 768K 1024K 1536K 2048K	All are supported	All are supported

Hardware Feature	System/360 Model 40	System/360 Model 50	System/370 Model 155	DOS - Model 155	OS - Model 155
B. Processor storage cycle in micro-seconds	2.5 for 2 bytes	2 for 4 bytes	2.1 for 16 bytes	-	-
1. CPU fetch from storage in micro-seconds (no channel interference)	1.5 for 2 bytes	1.0 for 4 bytes	1.49 for 4 bytes 1.61 for 8 bytes 1.96 for 16 bytes	-	-
C. High-speed buffer storage	No	No	One 8K buffer is standard	-	-
1. CPU fetch from buffer	-	-	230 ns for 4 bytes 345 ns for 8 bytes		
D. Processor storage validity checking	Parity checking on each byte - errors are not corrected by hardware.	Same as Model 40	ECC checking on a doubleword. Single-bit errors are corrected by hardware.	Corrected single-bit and uncorrected storage errors are logged by MCAR.	MCH logs errors as does DOS. Control program routines are refreshed if possible when double- or multiple-bit errors occur.
E. Byte boundary alignment nonpriviledged operands	No	No	Standard	Programmers can use byte alignment in Assembler, PL/I, and ANS COBOL programs.	Programmers can use byte alignment in Assembler, PL/I, ANS COBOL, and FORTRAN programs.
F. Storage and fetch protection	Storage protect is optional. Fetch protect is not available.	Storage protect is standard and fetch protect is not available.	Standard	Storage protect is supported.	Storage protect is supported.
G. Shared processor storage	Not available	Optional (Model 50 system shares 2361 Core Storage with a Model 50, 65, or 75.)	Not available	-	-
H. 2361 Core Storage	Cannot be attached	Can be attached	Cannot be attached	-	

Hardware Feature	System/360 Model 40	System/360 Model 50	System/370 Model 155	DOS - Model 155	OS - Model 155
III. CHANNELS					
A. Byte multiplexer channel 0 - up to 8 control units	Standard	Standard	Standard	Supported	Supported
1. Subchannels available	16-128	16-128 (256 is an option)	Up to 256	Up to 256 subchannels are supported.	Up to 256 subchannels are supported.
2. Burst mode locks out CPU	Yes	No	No	-	-
B. Second byte multiplexer (channel 4)	No	No	Optional for systems with 768K or more and channel 3 installed	Not supported	Up to 256 subchannels supported for a total of 512 in the system.
C. Block multiplexer channels (up to 8 control units)	Not available	Not available	1 and 2 Standard. 3-5 optional. Channel 4 cannot be installed if the second byte multiplexer is present.	Not supported	Supported
1. Maximum individual channel data rate	312KB	800KB	1.5 MB	-	-
D. Selector channels	Optional 0-2	Optional 0-3	Selector mode standard for all installed block multiplexer channels. 1 and 2 standard. 3-5 optional.	Supported	Supported
E. Channel retry data in an ECSW after channel error	No	No	Yes	CCH routine passes ECSW data to ERP to perform a retry of failing I/O operation	Same as DOS
F. Channel-to-channel adapter	Optional	Optional	Optional	-	-

Hardware Feature	System/360 Model 40	System/360 Model 50	System/370 Model 155	DOS - Model 155	OS - Model 155
IV. OPERATOR CONSOLE DEVICES	1. 1052 M7 Printer-Keyboard 15 cps (No alter/display mode	1. Same as Model 40	1. 3210 Console Printer-Keyboard with alter/display mode (15 cps)	Supported	Supported as the primary or an alternate console.
	2. Additional consoles, such as graphic units, optional	2. Same as Model 40	2. 3215 High-Speed Console Printer-Keyboard with alter/display mode (85 cps)	Supported	Supported as above
		3. Remote 2150 console with operator control panel and/or 1052 M7 is optional	3. Optional 3210 Console Printer-Keyboard remote with either (1) or (2) - no alter/display	Not supported	Supported as an alternate or an additional console.
		4. Remote 2250 Display Unit containing operator control panel is optional	4. 2150 Console with 1052 M7 Printer-Keyboard is optional	Not supported	Supported as above
			5. Additional consoles, such as graphic units are optional	Not supported	Supported as additional consoles by MCS and DIDOCS options.
V. I/O DEVICES					
A. 3211 Printer with tapeless carriage, UCS, and 18 additional print positions	Yes	Yes	Yes	Supported	Supported
B. Tape drives currently announced	All except 2420 Model 7	Yes	Yes	Supported	Supported
C. Direct access devices (2311,2314,2303,2301, and 2321)	All except 2301 drum	All except 2301 drum	All except 2301 drum	2303 and 2301 drums are not supported.	All are supported except 2301 drum

Hardware Feature	System/360 Model 40	System/360 Model 50	System/370 Model 155	DOS - Model 155	OS - Model 155
D. 3330 facility with RPS and multiple requesting	No	No	Yes on block multiplexer channels	Not supported	Supported
E. 2305 facility Model 2 with RPS and multiple requesting	No	No	One per system attached to channel 1	Not supported	Supported
F. Other devices: 1231,1259 M2,1285, 1404,1418,1428,1827, 2302,7340,1052 M7 except with 2150 Console	Yes	Yes	No	-	-

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A Guide to the IBM System/370 Model 155

GC20-1729-0

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Systems

A Guide to the IBM System/370 Model 155

This guide presents hardware, programming systems, and other pertinent information about the IBM System/370 Model 155 that describes its significant new features and advantages. Its contents are intended to acquaint the reader with the Model 155 and to be of benefit in planning for its installation.

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PREFACE

It is assumed that the reader of this document is familiar with System/360. The reader should have general knowledge of System/360 architecture, channels, I/O devices, and programming systems support. This guide highlights only those Model 155 hardware, I/O, and programming systems features that are different from those of System/360 models and discusses their significance. Additional, more detailed information regarding System/370 Model 155 hardware and programming systems support can be found in the following SRL publications.

IBM System/370 Model 155 Functional Characteristics (GA22-6942)

IBM System/370 Model 155 Channel Characteristics (GA22-6962)

IBM System/370 Model 155 Installation Information - Physical Planning (GA22-6970)

IBM System/370 Principles of Operation (GA22-7000)

Component Summary: 3830 Storage Control, 3330 Disk Storage (GA26-1592)

IBM System/360 Component Description:

2835 Storage Control and 2305 Fixed Head Storage Module (GA26-1589)

3211 Printer and 3811 Control Unit Component Description (GA24-3543)

Form-Design Considerations-System Printers (GA24-3488)

Emulating the IBM 1401, 1440, and 1460 on the IBM System/370 Model 155 Using OS/360 (GC27-6945)

Emulating the IBM 1410 and 7010 on the IBM System/370 Model 155 Using OS/360 (GC27-6946)

IBM System/360 Operating System:

- Planning for the IBM 3211 Printer Data Management Macro Instructions and Services (GC21-5008)
- Program Planning Guide for DOS Emulator on IBM System/370 Model 155 (GC24-5076)

Emulating the IBM 1410 and 7010 on the IBM System/370 Model 155 Using DOS/360 (GC33-2005)

Emulating the IBM 1401, 1440, and 1460 on the IBM System/370 Model 155 Using DOS/360 (GC33-2004)

IBM System/360 Disk Operating System:

- Planning Guide for the IBM 3211 Printer (GC24-5085)
- Planning Guide for IBM System/370 Model 155 MCAR/CCH Function (GC24-5084)

First Edition (June 1970)

This guide is intended for planning purposes only. It will be updated from time to time to reflect system changes; however, the reader should remember that the authoritative sources of system information are the Systems Reference Library (SRL) publications for the Model 155, its associated components and its programming support. These publications will first reflect such changes.

Copies of this and other IBM publications can be obtained through IBM branch offices.

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IBM **Technical Newsletter**

Re: Order No. GC20-1729-0

This Newsletter No. GN20-2226

Date July 14, 1970

Previous Newsletter Nos. None

A GUIDE TO THE IBM SYSTEM/370 MODEL 155

This Technical Newsletter provides replacement pages for the subject manual. Pages to be inserted and/or removed are listed below.

Title page, Preface	45–50
3–8	57, 58
11–18	61, 62
31, 32	65–76
35, 36	91, 92
39, 40	115–120

A change to the text or a small change to an illustration is indicated by a vertical rule to the left of the change. A changed or added illustration is denoted by the symbol • to the left of the caption.

Summary of Amendments

Minor additions and corrections have been made throughout the text.

Please file this cover letter at the back of the manual to provide a record of changes.

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256K to 2048K of processor (main) storage is available - four times the maximum main storage available on the Model 50. Processor storage has a cycle time of 2.1 microseconds for consecutive 16-byte references.

Byte boundary alignment is permitted for the operands of non-privileged instructions to eliminate the necessity of adding padding bytes within records or to blocked records for the purpose of aligning fixed- or floating-point data.

Error checking and correction (ECC) hardware, which automatically corrects all single-bit processor storage errors and detects all double-bit and most multiple-bit errors, is standard.

- I/O devices include the following.

  Most currently announced I/O devices for System/360 Models 40 and 50 can be attached.

  The new 3330 facility is available with significantly faster seeks and more than twice the data rate of the 2314 facility, more than three times the capacity of the 2314, and automatic error correction features. The new rotational position sensing and multiple requesting capabilities announced for the 2305 facility are standard.

  The 3330 has an 806 KB data transfer rate, average seek time of 30 ms, and full rotation time of 16.7 ms. Up to 800 million bytes can be contained on an eight drive facility.

  The 2305 facility Model 2, with a maximum module capacity of 11.2 million bytes, a data rate of 1.5 megabytes, and average access of 5 ms can be attached to a Model 155 to be used as a system residence device or as high-speed storage.

  The new high-speed 3211 Printer with a tapeless carriage and print speed of 2000 alphameric lines per minute is available. The tapeless carriage decreases operator intervention by eliminating carriage tape loading and unloading.

- Extensive hardware and programming systems error recovery and repair features are provided to enhance system reliability, availability, and serviceability.

- Compact physical design reduces Model 155 space requirements. The Model 155 has more than two and one-half times the number of circuits as a Model 50, yet a 512K system is one frame smaller than a 512K Model 50.

As the highlights indicate, Model 40 and 50 users have a broader range of Model 155 configurations to choose from than before when tailoring a growth system with improved throughput and expanded capabilities.

Specifically, the Model 155 offers the following advantages over Models 40 and 50.

Larger Processor (Main) Storage Sizes

Storage sizes of 256K, 384K, 512K, 768K, 1024K, 1536K, and 2048K are provided. The Model 40 can have a maximum of 256K, while 512K is the largest main storage size provided by a Model 50. The Model 155 offers larger storage sizes at smaller cost increments, and additional storage can contribute significantly to system performance and capabilities.

The addition of more storage provides the Model 155 user with the ability to:

- Execute more jobs concurrently, including new application and integrated emulator jobs
- Add and expand applications, such as graphics, teleprocessing, time-sharing, and data-based, that require larger amounts of storage
- Use higher level language translators and linkage editors that provide more functions and execute faster
- Execute larger processing programs without the necessity of overlay structures
- Allocate more storage to language translators and sorts to improve their execution speed
- Use more and larger I/O buffers to speed up input/output operations and optimize use of direct access storage space
- Include system generation options that improve control program performance and support additional functions

Greatly Expanded Channel Capabilities

The fast internal performance of the Model 155, together with expanded use of multiprogramming, requires that more data be available faster.

Two byte multiplexer channels can be installed on a Model 155. Models 40 and 50 are limited to one. The Model 155 also offers more and faster high-speed channels than the Model 50 (five instead of three, 1.5 MB data rate versus .8 MB) and block multiplexer channels not provided for Models 40 and 50.

The channel features of the Model 155 provide:

- Up to 512 byte multiplexer subchannels for large teleprocessing users.
- Attachment of high-speed direct access devices such as the 3330 and 2305 Model 2 facilities
- Potential increases in channel throughput via use of block multiplexing with rotational position sensing to improve effective data transfer rates
- A significantly higher attainable aggregate channel data rate than the Model 50 to balance the high performance capabilities of the Model 155 CPU

Faster I/O Devices with Increased Data Capacity

The 3330 and the 2305 Model 2 facilities offer significantly faster data access than the 2314 facility and 2301 Drum Storage because of higher data transfer rates, faster rotation, and new features. Rotational position sensing and multiple requesting used with block multiplexing can improve I/O throughput by making more efficient use of channel time. These direct access facilities also offer higher availability through use of new hardware-only and program-assisted error correction features.

The 3330 facility provides high-capacity and fast access for less cost per bit. It is a growth device for the 2314 facility and the 2321 Data Cell Drive that offers increased price performance. The 3330 facility is designed to be used in every area in which direct access storage is needed. For example:

- As a system residence device and for program library storage
- In teleprocessing applications for message queuing and for residence of online applications data
- In online, data-based applications, such as management information systems, airline reservations, etc.
- In time-sharing (or interactive) environments as swap devices and for online work storage (for program and data residence)
- As high-speed work storage for sorting, assembling, and link editing
- For residence of data indices, such as for ISAM data sets

The 2305 Model 2 facility offers faster access than, and more than twice the capacity of, the 2301 drum. For larger Model 155 users, the 2305 facility will be of benefit:

- As system residence devices
- In time-sharing environments as a swap device and for program and data residence
- As high-speed work storage and for residence of data indices

SUMMARY

The combination of new and improved hardware and input/output facilities, enhanced operating system support, integrated 1400/7010 emulation, DOS emulation under OS, and increased system availability provided by the Model 155 offers Model 40 and 50 users expanded computing capabilities without the necessity of a large conversion effort. Little or no time need be spent modifying operational System/360 code or programs currently being emulated. Users of 1400 and 7010 systems can upgrade directly to a Model 155 and an operating system environment with a minimum of reprogramming. DOS users can convert to OS more easily than is possible without the use of DOS emulation. Existing CPU-bound programs can execute faster because of the increased internal performance of the Model 155, while I/O-bound programs can benefit from the use of more storage, more channels, faster I/O devices, and block multiplexing.

The increased power and new functions of the Model 155 provide the base for expanded applications growth and penetration of previously marginal application areas. The increased price performance of the Model 155 offers the user the opportunity to widen his data processing base for less cost.

In conclusion, the major advantages of the System/370 Model 155 are:

- LARGE PROCESSOR STORAGE - At low cost increments
- FAST INTERNAL PERFORMANCE - Approximately three and one-half to four times the Model 50
- CHANNEL ENHANCEMENTS - More, faster, new capability
- INTEGRATED EMULATION - Native mode and second generation processed concurrently
- RELIABILITY, AVAILABILITY, AND SERVICEABILITY - Hardware and programming systems features not available on System/360 Models 40 and 50
- NEW I/O EQUIPMENT - Faster, larger direct access storage with new capabilities and a faster printer

SECTION 20: I/O DEVICES

20:05 I/O DEVICE SUPPORT

Most presently announced I/O devices that can be attached to System/360 Models 40 and 50 can be attached to the System/370 Model 155. The following I/O devices are not included in standard Model 155 configurations:

1052 M7 Printer Keyboard - except attached to a 2150 Console
1231 Optical Mark Page Reader
1259 M2 Magnetic Character Reader
1285 Optical Reader
1404 Printer
1418 Optical Character Reader
1428 Alphameric Optical Reader
1827 Data Control Unit (for attachment of 1800 system analog and/or digital control units to the Model 155)
2301 Drum Storage
2302 Disk Storage
7340 Hypertape Drive
7772 Audio Response Unit

The 1287 Optical Reader and 1288 Optical Page Reader can be attached to a byte multiplexer channel only.

New I/O devices for the Model 155 are:

- the 3330 facility - attaches only to a block multiplexer channel
- the 2305 facility Model 2 - attaches only to a block multiplexer channel
- the 3211 Printer - attaches to any Model 155 channel

The 3330 and 2305 facilities represent significant advancements in direct access device technology. They provide greater online data capacity, faster data rates and access, and expanded error correction features. Both have rotational position sensing and multiple requesting as standard features.

The 3330 represents the latest generation of direct access device with removable, interchangeable disk packs. The 2305 facility is a major extension of the nonremovable, high-speed, fixed-head direct access storage concept.

The major new characteristics of the 3330 and 2305 facilities and the 3211 Printer are discussed in the following subsections.

20:10 3330 DISK STORAGE AND 3830 STORAGE CONTROL

The 3330 facility is a modular, large-capacity, high-performance direct access storage subsystem. The 3330 facility consists of 3830 Storage Control and from one to four 3330 Disk Storage modules. A 3330 module contains a pair of independent disk storage drives, as shown in Figure 20.10.1. The new removable 3336 Disk Pack is used for data storage. Usage meters are contained in the 3830 control unit and in each 3330 module.

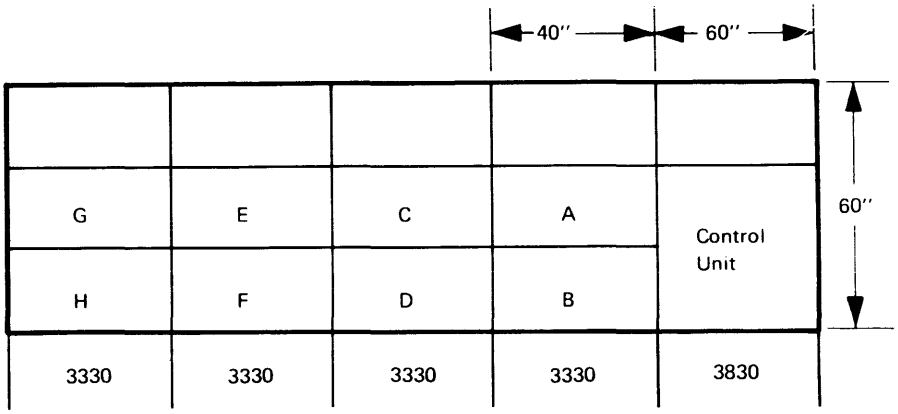

Figure 20.10.1. The 3330 facility

Drives are mounted in powered drawers that are opened and closed by a switch on the operator control panel on the 3330 module. Logical address plugs are supplied, as for the 2314, in addition to a CE service plug. The latter is used when inline diagnostics are to be executed.

Facility configurations and maximum capacities, using full track records, are shown below.

3830 Storage Control + one 3330 module 200 megabytes
3830 Storage Control + two 3330 modules 400 megabytes
3830 Storage Control + three 3330 modules 600 megabytes
3830 Storage Control + four 3330 modules 800 megabytes

Functionally, the 3330 facility provides more capabilities than the 2314, particularly in the areas of performance and availability. The 3330 supports all the standard 2314 commands (except the file scan commands) in addition to several new operations, including RPS and error recovery commands. The 3330 facility also is an attractive growth device for the 2321 Data Cell Drive.

The new, removable 3336 Disk Packs are interchangeable across 3330 disk drives but are not interchangeable with the 2316 Disk Packs used on 2314 disk drives (Table 20.10.2 compares disk pack characteristics). Like 2316 packs, 3336 disk packs will be initialized in the factory with home addresses and capacity records (R0). Up to 20 defective tracks per pack will be flagged and have alternates assigned. The quick DASDI routine (part of the IEHDASDR utility) currently available for processing 1316 and 2316 packs, will support 3336 packs. Quick DASDI writes the volume label, the VTOC, and IPL records, if requested, but bypasses track analysis. It also determines the number of flagged tracks and places this data in the VTOC.

Table 20.10.1 compares the capacity and timing characteristics of the 3330 facility with those of the 2314 facility and the 2321 Data Cell Drive. The increase in capacity achieved by replacing a 2314 or a 2321 with a 3330 depends upon the block size chosen for the data on the 3330. For example, if the 2314 full track block size of 7294 bytes is maintained for a given data set on the 3330 to avoid programming changes, the 3330 yields a 91% increase in full pack capacity (almost twice the capacity). However, reblocking to a full track on the 3330, 13,030 bytes, yields a 242% full pack capacity increase. If there is not enough processor storage available to allocate I/O areas of 13,030 bytes, lowering the 3330 block size used to half a 3330 track yields a 239% increase in full pack capacity.

3211 Printer with tapeless carriage. The 3211 Printer, with or without the 18 additional print positions, will be supported by QSAM and BSAM for exactly the same functions as is the 1403 Printer and by ASP and HASP. The control program will handle loading of the forms control buffer (FCB) with carriage control images. This support is similar to that provided for Universal Character Buffer (UCB) loading.

The user can define one or more default FCB images at system generation time. Two IBM-supplied default images are included automatically. All other FCB images to be used must be defined by the user and placed in SYS1.SVCLIB, as is the case with UCB images. User-supplied default images must be identified as defaults. The FCB image to be used by a processing program can be specified in the 3211 Printer DD statement included for the job step and will be loaded into the FCB by the control program.

The FCB image currently loaded can also be changed by the programmer during execution of the processing program by use of an Assembler Language macro. If the DD statement does not specify an FCB image and the image currently loaded is not one of the defaults specified at system generation, the operator is requested to specify the FCB image to be used.

The FCB image (and the UCS character image) to be loaded for a 3211 Printer used by an output writer can be indicated in the output writer procedure or in the START output writer command issued by the operator. FCB and UCB images can also be specified in the SYSOUT DD statement for a data set that is to be printed by the output writer, and they will be loaded into the 3811 control unit prior to the printing of the data set.

Any time the FCB parameter is used, as described above, the user can specify that operator verification of forms alignment is to be requested by the control program via a console message when the buffer is loaded. The operator must respond to this message.

The 3211 error recovery routine will retry a print operation after a parity check occurs in the UCB or print line buffer if QSAM is used and three I/O buffers are provided for the printer data set. When the operation is retried, the 3811 control unit insures that only the print positions that did not print correctly the first time are reprinted.

30:15 DOS SUPPORT

DOS will be modified in future releases so that it supports certain Model 155 hardware features. Appropriate alteration of the DOS supervisor generated for a Model 155 will accommodate the fixed storage area of lower storage in the Model 155.

DOS support of Model 155 features will be provided as follows. Programming systems support of RAS features is discussed in Section 50.

New instructions. Assembler D (14K variant) will include mnemonics for all the new instructions so that they can be used in user-written Assembler Language programs. The DOS high-level language translators currently available will not generate the six new general purpose instructions.

Extended precision floating-point. Mnemonics for extended precision instructions and data formats will be added to Assembler D. The DOS high-level language translators currently available do not support extended precision.

Interval timer. The timer will be supported in the same manner as it is currently, for time of day and time intervals.

Time of day clock. This clock is not supported for time of day values.

Byte boundary alignment. The programmer has the ability to byte-align binary and floating-point data in Assembler Language programs, in ANS COBOL programs (by omitting the SYNCHRONIZED clause), and in PL/I programs (by specifying the UNALIGNED attribute). However, the high-level language translators still align unaligned binary and floating-point data prior to its use.

1401/1440/1460, 1410/7010 Compatibility Feature. Two integrated emulator programs will be provided, one to emulate 1401/1440/1460 programs and the other to emulate 1410/7010 programs. (See Section 40 for a complete discussion of these emulator programs.)

New consoles. The 3210 Console and the 3215 High-Speed Console Printer-Keyboards are supported as the DOS console device. A remote 3210 Console is not supported.

Channels. A single byte multiplexer channel with up to 256 subchannels and selector channel mode are supported. A second byte multiplexer channel and block multiplexer mode are not supported.

New direct access devices. The 3330 and 2305 facilities are not supported.

3211 Printer. This printer, with or without the 18 additional print positions, will be supported in the same manner as is the 1403 Printer, including support by DOS POWER. Forms Control Buffer and Universal Character Buffer loading for the 3211 will be handled in the same way. The user must execute an IBM-supplied buffer load utility program (SYSBUFLD) as a job step in order to load the FCB and/or the UCB. No provision has been made for loading the FCB or UCB during execution of a job step. User-defined UCB images must be loaded from the core image library. FCB images can be loaded from cards or the core image library.

If a command retry indication is present, the 3211 error recovery routine supports retry of an operation that failed. This option must be requested by the user in the DTF for the 3211 Printer.

The size of the partition required for emulation depends on the 1400 system being emulated, including standard and special features, input/output devices, buffers, etc. The processor storage required for the 1401/1440/1460 emulator is equal to the combined sizes of:

- Simulated 1401/1440/1460 storage. Each position of 1400 storage is simulated in one byte of Model 155 storage (for example, 8000 positions = 8000 bytes).
- Emulator routines required to emulate the 1401/1440/1460 system instructions, features, and I/O operations
- Tape, disk, and unit record buffers. The number and size of tape and disk buffers are specified by the user.

Estimated minimum 1401/1440/1460 emulator processor storage requirements for emulation of a 1400 system with unit record operations only, unit record/tape operations, or unit record/tape/disk operations are shown below.

Emulated Operations	DOS Partition Size (bytes)
1401/1440/1460 unit record	13K + 1401/1440/1460 core size + buffers
1401/1440/1460 unit record/6 tapes	18K + 1401/1440/1460 core size + buffers
1401/1440/1460 unit record/6 tapes/ 4 disks	22K + 1401/1440/1460 core size + buffers

The 1400 CPU features and 1400 I/O devices and special features supported and the Model 155 devices used for 1401/1440/1460 emulation are given in Tables 40.10.1 and 40.10.2. Table 40.10.3 lists the 1400 I/O devices that are not supported.

Table 40.10.1. 1401/1440/1460 I/O device and feature support and corresponding Model 155 devices

1401/1440/1460 Device and Features	Corresponding Model 155 Device
1402, 1442, 1444 Card Read Punch Features supported • Column Binary • Card Image • 51-Column Interchangeable Read Feed • Punch Feed Read • Punch Column Skip • Stacker Select • Processing Overlap Features not supported • Read Punch Release • Multiple card reader/punch operations	1442, 2520, 2540 Card Read Punch and 2501 Card Reader Note: Card reader and card punch operations may be emulated using a magnetic tape or direct access storage device
1403, 1404, 1443 Printer Features supported • Processing Overlap • Space Suppression Features not supported • Selective Tape Listing • Multiple printer operations • Read Compare	1403, 1443 Printer Note: Printer operations may be emulated using a magnetic tape or direct access storage device
1407, 1447 Console	3210 or 3215 console printer-keyboard
729, 7330, 7335 Magnetic Tape Unit Features supported • Column Binary • Processing Overlap Features not supported • Compressed tape	2400 series magnetic tape • Seven-Track Compatibility feature is required if processing seven-track tapes
1301, 1311, 1405 Disk Storage Features supported • Direct Seek • Scan Disk • Track Record • Additional access arm (1405) Note: A 1405 cannot be emulated in combination with a 1301 or 1311	2311, 2314 direct access devices

Table 40.10.2. 1401/1440/1460 CPU features supported

Core storage from 1,400 to 16,000 positions. The 1401 Model G is not emulated.	Sense Switches
Expanded Print Edit	Advanced Programming
Inverted Print Edit	Indexing and Store Address Register
High-Low-Equal Compare	Bit Test
Multiply-divide	

Note: Translate feature is not supported

Table 40.10.3. Unsupported 1401/1440/1460 devices

1445 Printer	7340 Hypertape Drive
1011 Paper Tape Reader	1428 Alphameric Optical Reader
1012 Tape Punch	1231 Optical Mark Page Reader
1412 Magnetic Character Reader	1285 Optical Reader
1418 Optical Character Reader	Teleprocessing devices
1419 Magnetic Character Reader	

Emulator performance will vary depending on user options, such as number and size of buffers, the instruction mix of the 1401/1440/1460 programs, the format of tape files, and the priority of the partition in which the emulator is running.

Emulator performance is improved by:

1. Using double buffers and spanned record format for tape files in lieu of single or shared buffers and 1400 record format. (A shared buffer can be used by more than one I/O device.)

2. Using single buffers rather than shared buffers for disk files

3. Specifying device independence for emulating unit record operations on a magnetic tape or direct access storage device

4. Using a card reader that is not equipped with the 51-Column Interchangeable Read Feed and Column Binary features and not using the Select Stacker instruction

DOS 1410/7010 EMULATOR SUPPORT

The Model 155 DOS 1410/7010 emulator offers the 1410/7010 stand-alone emulator user the advantages of integrated emulation already discussed.

Processor Storage Requirements

The size of the partition required for emulation depends on the 1410/7010 system being emulated, including standard and special features, input/output devices, buffers, etc. The processor storage required for the 1410/7010 emulator is equal to the combined sizes of:

- Simulated 1410/7010 storage. Each position of 1410/7010 storage is simulated in one byte of Model 155 storage (for example, 20,000 positions = 20,000 bytes).

- Emulator routines required to emulate the 1410/7010 system instructions, features, and I/O operations

- Tape, disk, and unit record buffers. The size and number of tape and disk buffers are specified by the user.

Estimated minimum 1410/7010 emulator processor storage requirements for emulation of a 1410/7010 system with unit record/tape operations or unit record/tape/disk operations are shown below.

Emulated Operations	DOS Partition Size (bytes)
1410/7010 unit record and 6 tapes	27K + 1410/7010 core size + buffers
1410/7010 unit record, 6 tapes, 4 disks	37K + 1410/7010 core size + buffers

The 1410/7010 CPU features and 1410/7010 I/O devices and special features supported and the Model 155 devices used for 1410/7010 emulation are given in Tables 40.10.4 and 40.10.5. Table 40.10.6 lists the 1410/7010 I/O devices that are not supported.

Table 40.10.4. 1410/7010 I/O devices and features and corresponding Model 155 devices

1410/7010 Device and Features	Corresponding Model 155 Device
1402, 1442 Card Read Punch Features not supported Stacker Select 51-Column Interchangeable Read Feed	1442, 2540, 2520 Card Read Punch and 2501 Card Reader Note: Card reader and card punch operations may be emulated using a magnetic tape or direct access storage device.
1403 Printer All standard operations	1403, 1443 Printer Note: Printer operations may be emulated using a magnetic tape or direct access storage device.
1415 Console All standard operations	3210 or 3215 console printer-keyboard
729, 7330 Magnetic Tape Units All standard operations	2400-Series Magnetic Tape Units Note: Seven-Track Compatibility feature is required for processing seven-track tapes.
1301, 1302, 2302 Disk Storage All standard operations Note: Any combination of 1301 and 1302/2302 disk storage drives can be emulated.	2311, 2314 direct access devices Note: An emulated 1302/2302 record will not fit on a 2311 disk track.

Table 40.10.5. Supported and unsupported 1410/7010 CPU features

Supported	Unsupported
Main storage up to 80,000 positions (1410) and 100,000 positions (7010) Inverted Print Edit Priority Feature Processing Overlap Channels one through four Floating Point Arithmetic	1401/1410 Compatibility Mode 7010 Diagnostic instruction, Branch on C Bit Diagnostic instruction, Branch if Tape Indicator J(I)K 7010 Memory Protect and Program Relocate 7010 Interval Timer

Table 40.10.6. Unsupported 1410/7010 devices

1311 Disk Storage Drive	1419 Magnetic Character Reader
1405 Disk Storage	7340 Hypertape Drive
1011 Paper Tape Reader	2321 Data Cell Drive
1412 Magnetic Character Reader	Teleprocessing devices

The following I/O devices are supported by the OS DOS emulator:

- 1403, 1404, 1443, 1445, 3211 Printers
- 1052 Printer-Keyboard
- 1285, 1287, 1288 Optical Readers (the latter two not in document mode)
- 1442, 2520, 2540 Card Read Punches
- 2501 Card Reader
- 2311 Disk Storage Drive
- 2314 Direct Access Storage Facility
- 2321 Data Cell Drive
- 2400-series magnetic tape units
- 2671 Paper Tape Reader
- Any new devices that are supported by both DOS and OS, subject to the programming restrictions stated

EMULATOR JOB SUBMISSION AND GENERAL OPERATION

DOS emulation is initiated as a single-step OS job via the input stream. An OS DOS emulator job can consist of one or more DOS jobs. The OS DOS emulator program, which must reside in SYS1.LINKLIB or a user job library, is specified in the EXEC job control statement included in the job control for the OS DOS emulator job. The following also must be identified in the DD job control statements for the OS DOS emulator job:

1. The DOS system residence and operator console devices
2. The location(s) of the DOS input stream(s)
3. I/O assignments for the staging of DOS unit record I/O operations
4. All the I/O devices that will be used by the DOS programs that are emulated as part of this DOS emulator job

The DOS system background partition input stream can be located in the OS input stream or on a separate data set. DOS batch-initiated foreground (BJF) partition input streams must be located in separate data sets.

If enough Model 155 processor storage is available, I/O staging can be used to increase OS DOS emulator job throughput and reduce the number of devices that have to be dedicated to the DOS emulation partition or region. It allows DOS unit record files SYSRDR, SYSPCH, and SYSLST to be emulated on direct access devices using the OS reader interpreter and output writer. DOS job control statements (for the BG partition) and/or card input to DOS programs to be emulated can be placed in the OS input stream and will be transcribed by the reader interpreter to SYSIN data sets on direct access devices. Thus, emulated DOS jobs steps will obtain their card input from OS SYSIN disk data sets. Output from emulated DOS programs can be placed in OS SYSOUT data sets on disk to be transcribed to the printer or punch by an output writer.

The following should be noted about the use of I/O staging. In OS, a job is not placed in the input queue, from which all jobs are scheduled, until the entire job (job control and input stream data for the job) has been read by the reader interpreter. Similarly, SYSOUT data sets produced during job step execution are not placed in the output queue for transcription by an output writer until job termination.

Thus, if all DOS jobs to be emulated are grouped together as a single OS DOS emulator job, DOS emulation cannot begin until all DOS

jobs (and their input stream data) have been read by the reader interpreter, and none of the SYSOUT data sets from completed emulated DOS jobs can be transcribed until the OS DOS emulator job itself terminates (all DOS jobs processed). This negates one advantage of I/O staging, which is the overlapping of unit record input and output data transcription with processing.

Therefore, consideration should be given to grouping DOS jobs into two or more OS DOS emulator jobs that execute one after the other in the OS DOS emulator partition/region. In addition, if the output from a particular DOS job is desired immediately, it should not be staged (written to a SYSOUT data set). The use of multiple OS DOS emulator jobs in an OS DOS emulator partition/region, instead of one, offers an additional advantage in optimizing device usage, as discussed later.

I/O operations and I/O error recovery procedures for emulated DOS programs are handled by the OS control program. All I/O devices to be used by emulated DOS programs must be allocated to the DOS emulation partition or region when the OS DOS emulator job is begun. These devices are dedicated to DOS emulation and cannot be allocated to any other executing OS jobs while DOS emulation is in operation. Thus, direct access devices and their data sets cannot be shared by an OS job step and an emulated DOS program. However, DOS direct access volumes can be shared by DOS partitions being emulated in the same OS DOS emulator partition or region. In addition, the user must ensure that all online OS DOS emulator direct access volumes have unique volume serial numbers with respect to other DOS and OS direct access volumes online at the same time.

Consideration should be given to grouping DOS jobs into multiple OS DOS emulator jobs according to the types and total number of I/O devices required. This can reduce the number of I/O devices that have to be dedicated to a DOS emulation partition or region at any given time, thereby making more devices available to other OS jobs.

When the DOS emulation job is initiated, the DOS emulator program is loaded into the OS DOS emulator partition/region. The DOS emulator program performs control block and table initialization and initiates an IPL from the DOS system residence volume. Once the DOS supervisor has been loaded and has established the DOS partitions, DOS job execution begins. DOS programs are loaded into the defined DOS partitions and emulated. Messages to the operator from the DOS emulator program are issued in standard OS format and include a unique identification to indicate that they are OS DOS emulator messages. If the MCS option is included in the OS control program, all DOS emulation messages can be routed to a specific console, and thus isolated.

The entire OS DOS emulator partition/region operates with a nonzero storage protect key to prevent it from interfering with the OS control program and other executing OS jobs. Therefore, the DOS emulator program, the DOS supervisor, and other DOS jobs in the emulator partition/region are not protected from inadvertent modification by an executing DOS program.

INSTALLATION OF THE OS DOS EMULATOR

The following are the major steps that a DOS user must take to install the OS DOS emulator on a Model 155:

- Data processing personnel -- systems analysts and designers, programmers, operators, etc.-- must be educated on OS

Hardware Feature	System/360 Model 40	System/360 Model 50	System/370 Model 155	DOS - Model 155	OS - Model 155
IV. OPERATOR CONSOLE DEVICES	1. 1052 M7 Printer-Keyboard 15 cps (No alter/display mode	1. Same as Model 40	1. 3210 Console Printer-Keyboard with alter/display mode (15 cps)	Supported	Supported as the primary or an alternate console.
	2. Additional consoles, such as graphic units, optional	2. Same as Model 40	2. 3215 High-Speed Console Printer-Keyboard with alter/display mode (85 cps)	Supported	Supported as above
		3. Remote 2150 console with operator control panel and/or 1052 M7 is optional	3. Optional 3210 Console Printer-Keyboard remote with either (1) or (2) - no alter/display	Not supported	Supported as an alternate or an additional console.
		4. Remote 2250 Display Unit containing operator control panel is optional	4. 2150 Console with 1052 M7 Printer-Keyboard is optional	Not supported	Supported as above
			5. Additional consoles, such as graphic units are optional	Not supported	Supported as additional consoles by MCS and DIDOCS options.
V. I/O DEVICES					
A. 3211 Printer with tapeless carriage, UCS, and 18 additional print positions	Yes	Yes	Yes	Supported	Supported
B. Tape drives currently announced	All except 2420 Model 7	Yes	Yes	Supported	Supported
C. Direct access devices (2311,2314,2303,2301, and 2321)	All except 2301 drum	All except 2301 drum	All except 2301 drum	2303 and 2301 drums are not supported.	All are supported except 2301 drum

Hardware Feature	System/360 Model 40	System/360 Model 50	System/370 Model 155	DOS - Model 155	OS - Model 155
D. 3330 facility with RPS and multiple requesting	No	No	Yes on block multiplexer channels	Not supported	Supported
E. 2305 facility Model 2 with RPS and multiple requesting	No	No	Two on channel 1 and two on channel 2	Not supported	Supported
F. Other devices: 1231,1259 M2,1285, 1404,1418,1428,1827, 2302,7340,1052 M7 except with 2150 Console	Yes	Yes	No	-	-

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A GUIDE TO THE IBM SYSTEM/370 MODEL 155

This Technical Newsletter provides replacement pages for the subject manual. Pages to be inserted and/or removed are listed below.

Title page, Preface	49, 50
Contents	67 – 70
1 – 4.1	73, 74
5, 6	105 – 106.1
19,20	111, 112
31 – 32.1	119, 120
43, 44	127
44.1 – 44.11	

A change to the text or a small change to an illustration is indicated by a vertical rule to the left of the change. A changed or added illustration is denoted by the symbol • to the left of the caption.

Summary of Amendments

Additions and changes have been made to include information about the 3803/3420 Magnetic Tape Subsystem.

Note: Please file this cover letter at the back of the manual to provide a record of changes.

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