IBM Maintenance Library

3705-80 Communications Controller
Theory-Maintenance
Volume II

SY27-0209-1

Preface

This publication is directed to the Customer Engineer assigned to maintain the IBM 3705-80 Communications Controller. He is assumed to be trained on either a System/360, System/370, 4300 Processor, or 3031, 3032, 3033, or 3081 Processor Complex and to have a teleprocessing background.

This publication should be used to locate and replace failing field replaceable units within the controller. Pictures are combined with text to convey basic operational concepts. No attempt is made to provide detailed theory information. Each page contains one topic (although some topics may require more than one page).

The CE should always begin at the "start" section of Volume I when trying to locate a failure. This section contains a flowchart that points to the correct part of the manual for locating the failure.

The 3705-80 FETMM consists of three volumes which are identified by two form numbers. The volumes may be placed in separate binders for ease of use.

Volume I (SY27-0208) contains comprehensive "how to fix information." Information is provided on: (1) maintenance philosophy, (2) internal functional tests (IFTs), (3) diagnostic control module (DCM), (4) power map procedures, and (5) panel line test. The purpose of Volume I is to help the CE test the 3705-80, locate failing hardware components, and repair and return the controller to the user as quickly as possible. Divider tabs provide quick access to the individual sections.

Volume II (SY27-0209, part 1 of 2) contains an abbreviation list, legend, a volume table of contents, introduction to the 3705-80, a description of the control panel switches and lights and procedures for using them, diagnostic aids, IPL, and the theory-maintenance sections on the central control unit, and storage. A composite index of both volumes is at the back of each volume. Divider tabs provide quick access to the individual sections.

Volume III (SY27-0209, part 2 of 2) contains an abbreviation list, legend, a volume table of contents, and the theory-maintenance sections on the type 1 channel adapter, the type 2 communication scanner, the line interface base, the line sets, the power system, the remote program loader (RPL), and the type 4 channel adapter. It also contains information on test tools and equipment, preventive maintenance, and physical locations. A composite index of both volumes is at the back of each volume. Divider tabs provide quick access to the individual sections.

Prerequisite Publication

Introduction to the 3705-80 Communications Controller, GA27-3304.

Related Publications

IBM 3705-80 Communications Controller Principles of Operation, GC30-3074
IBM 3704 and 3705 Communications Controllers Original Equipment Manufacturer's Information, GA27-3053
IBM 3705-80 Parts Catalog, S131-0077
System/360 Operating System Online Test Executive Program, GC28-5086
DOS OLTEP SRL, GC24-5086
System/360 and System/370 I/O Interface Channel to Control Unit Original Equipment Manufacturer's Information, GA22-6974

Guide to Using the IBM 3705 Communications Controller Control Panel, GA27-3087

SUMMARY OF CHANGES FOR SY27-0209-1

This revision contains:

- a new section (Type 4 CA) in Volume III that provides information on the Type 4 Channel Adapter.
- new pages and updated information on existing pages in Volumes II and III to integrate Type 4 CA information.
- minor updates to the Power Section (D pages) of Volume II.
- other minor editorial changes and clarifications.

Second Edition (January 1982)

This edition has important changes. It obsoletes SY27-0209-0. A new section (Type 4 CA) in volume III provides information on the Type 4 Channel Adapter. Other changes and added information have a vertical line at the left side.
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IBM has prepared this maintenance manual for the use of IBM customer engineers in the installation, maintenance, and repair, of the specific machines indicated. IBM makes no representations that it is suitable for any other purpose.

The information in this manual is sometimes change. Any changes will be given in later editions or in Technical Newsletters. Ensure that you have the latest edition and all Technical Newsletters before you use the manual.

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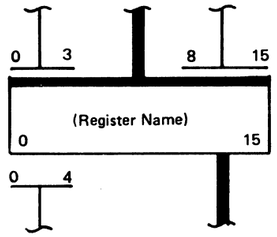
Abbreviations

A	And circuit or ampere
AA	automatic answering
ABAR	attachment buffer address register
ABO	adapter bus out (register)
ac	alternating current
ACO	automatic call originate
ACF/NCP/ VS	Advanced Communications Function for Network Control Program/Virtual Storage
ACR	abandm call and retry
ACU	automatic calling unit
adr	address
AEQ	automatic equalizer
AHR	add halfword register (instruction)
ALD	automated logic diagram
ALU	arithmetic logic unit
AMP	amplifier
APAR	authorized program analysis report
AR	add register (instruction)
ARI	add register immediate (instruction)
B	branch (instruction)
BAL	branch and link (instruction)
BALR	branch and link register (instruction)
BAR	buffer address register
BB	branch on bit (instruction)
BC	bit clock
BCB	bit control block
BCC	bit clock control
BCL	branch on C latch (instruction)
BCT	branch on count (instruction)
BO	bus out
BP	break point
bps	bit per second
BSC	binary synchronous communication
BSM	bridge storage module
BZL	branch on Z latch (instruction)
CA	channel adapter
CACHKR	channel adapter check register
CACR	channel adapter control register
CADB	channel adapter data buffer
CAMR	channel adapter mode register
CASNSR	channel adapter sense register
CASTR	channel adapter status register
CB	circuit breaker
CBAR	CSB buffer address register
CCB	character control block
CCR	compare character register (instruction)
CCT	coupler cut through (modem)
CCU	central control unit
CD	carrier detect
CDS	configuration data set
CE	Channel End (status)
chan	channel
char	character
CHR	compare halfword register (instruction)
ck	check
clk	clock
cm	centimeter
CMDR	channel adapter command register
CMND	command
com	common
COS	Call Originate Status
CP	circuit protector
CPU	central processing unit
CR	compare register (instruction)
CRC	cyclic redundancy check
CRI	compare register immediate (instruction)
CRQ	Call Request
CS	cycle steal
CSAR	cycle steal address register
CSB	communication scanner base
CSCD	clear to send, carrier detect
CSMC	cycle steal message counter
ctrl	control
CTS	Clear To Send
CUE	Control Unit End (status)
CW	control word
CWAR	control word address register
CWCNTR	control word byte count register
DAA	data access arrangement
DA	data modem ready
dB	decibel
DBAR	diagnostic buffer address register
dc	direct current
DCE	data circuit-terminating equipment
DCM	diagnostic control monitor
DCR	data channel ready
DE	Device End (status)
DET	detector
diag	diagnostic
dist	distance
DLO	data line occupied
DOS	Disk Operating System
DPR	digit present
DR	display register or data ring (modem)
DCS	distant station connect (ACO only)
DSR	data set ready
DT	data tip (modem)
DTE	data terminal equipment
DTR	data terminal ready
EC	edge connector
EB	extended buffer
ECP	emulation control program
EIA	Electronic Industries Association
enbl	enable
EON	end of number (ACO only)
EPO	emergency power off
ESC	emulation subchannel
EXT	external
FCS	final control sequence
FET	field effect transistor modem card
FETOM	Field Engineering Theory of Operation Manual
FF	flip flop
FL	flip latch
FRU	field replaceable unit
GB	ground bus
gnd	ground
grp	group
hex	hexadecimal
Hlfwd	halfword
horz	horizontal
HS	heat sink
Hz	Hertz
I	instruction (cycle)
IAR	instruction address register
IC	insert character (instruction)
ICS	initial control sequence
ICT	insert character and count (instruction)
ICW	interface control word
IFT	internal functional test
IN	input (instruction)
INCWAR	inbound control word address register
Init	initial
int	internal
intf	interface
I/O	input/output
IPL	initial program load
IR	interrupt remember
irpt	interrupt
ISACR	initial selection address and command register
L	load (instruction)
LA	load address (instruction)
LAR	lagging address register
LCD	line code definer
LCOR	load character with offset register (instruction)
LCR	load character register (instruction)
LED	light emitting diode
LGF	leading graphics flag
LH	load halfword (instruction)
LHOR	load halfword with offset register (instruction)
LHR	load halfword register (instruction)
LIB	line interface base
lim	limiter
LOR	load with offset register (instruction)
LOSC	last oscillator sample condition
LR	load register (instruction)
LRI	load register immediate (instruction)
LS or ls	local store
lt	latch
L1	level 1
L2	level 2
L3	level 3
L4	level 4
L5	level 5
mA	milliampere
Mem TB	memory terminal board
modem	modulator/demodulator
ms/divn	milliseconds per division
MST	monolithic system technology
mV	millivolt
NB	Digit Signal
N/C	normally closed
NCP	network control program
NCR	and character register (instruction)
NHR	and halfword register (instruction)
N/O	normally open
NR	and register (instruction)
NRI	and register immediate (instruction)
NRZI	non-return-to-zero inverted
ns	nanoseconds
NSC	native subchannel
OBR	outboard recorder
O/C	overcurrent
OCR	or character register (instruction)
OE	exclusive or
OH	off hook (modem)
OHR	or halfword register (instruction)
OLT	on line test
OLTEP	on line test executive program
OLTLIB	on line test library
OLTSEP	on line test standalone executive program
op	operation
op reg	operation register
OR	or register (instruction)
ORI	or register immediate (instruction)
OS	Operating System
OSC	oscillator
OUT	output (instruction)
OUTCWAR	outbound control word address register
OVRN	overrun
O/V	overvoltage
P	parity
PC	parity check
PCF	primary control field
PCI	program controlled interrupt
PDF	parallel data field
PEP	partitioned emulation programming
PG	parity generation
pgm	program
PH	polarity hold
PND	Present Next Digit
P/N	part number
POR	power on reset
pos	position

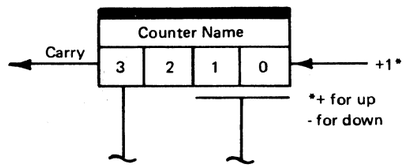
POSC	present oscillator sample condition
pot	potentiometer
P-P	post processor modem card
PPB	prime power box
PUT	programmable unijunction transistor
PWI	power indicator
R	resistance or resistor
rcv	receive
rd	read
rdy	ready
RE	register and external register (instructions)
ref	reference
reg	register
regen	regenerative
req	request
RI	register immediate (instruction) or ring indicator (modem)
RLSD	receive line signal detector
RMS	root mean square
ROS	read-only storage
RPL	remote program loader
RR	register to register (instructions)
RS	register to storage (instructions)
RSA	register and storage with addition (instructions)
RT	register branch or register and branch (instructions)
RTS	Request To Send
rly	relay
SAR	storage address register
SCF	secondary control field
SCR	silicon controlled rectifier or subtract character register (instruction)
SCRID	silicon controlled rectifier indicator driver
SDF	serial data field
SDLC	synchronous data link control
SDR	storage data register
sec	second
sel	selection
SEP	separator (ACO only)
seq	sequence
SG	signal ground
SH	switch hook (modem)
SHR	subtract halfword register (instruction)
SIG	signal
SIO	start I/O
SMS	standard modular system
SR	subtract register (instruction)
SRI	subtract register immediate (instruction)
SRL	Systems Reference Library
S/S	start/stop
ST	store (instruction)
STC	store character (instruction)
STCT	store character and count (instruction)
STH	store halfword (instruction)
stk	stacked
svc	service
sw	switch
SYN	synchronous idle
sync	synchronization or synchronous
TAR	temporary address register
TB	terminal board
TIC	Transfer In Channel
tr	trigger
TRM	test register under mask (instruction)
TSL	Technical Service Letter
T2	test 2
T3	test 3
T4	test 4
UC	Unit Check (status)
UE	Unit Exception (status)
V	volts
V/divn	volts per division
wd	word
wr	write
XCR	exclusive-or character register (instruction)
xfer	transfer
xfmr	transformer
XHR	exclusive-or halfword register (instruction)
xmt	transmit
XR	exclusive-or register (instruction)
XRI	exclusive-or register immediate (instruction)
2W	two-wire line connection (implies half-duplex)
4W	four-wire line connection (implies duplex, but actual duplex depends on the line set type and telephone company equipment).

Legend
(Part 1 of 2)
1. Logic Diagrams

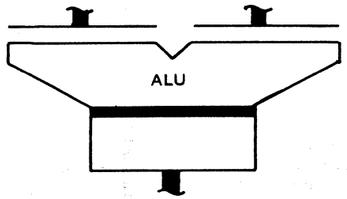


Register

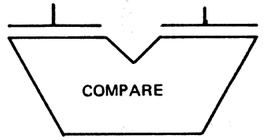
The input side is denoted by a thick line. A partial transfer of contents is shown by numbered input and/or output lines.



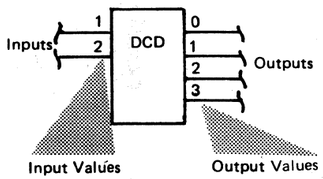
Counter



ALU

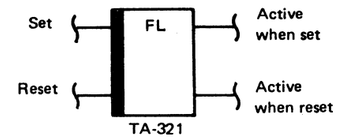


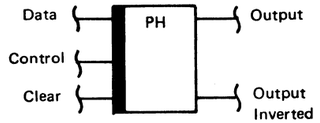
Compare

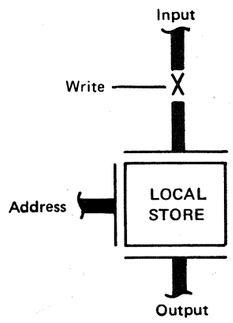


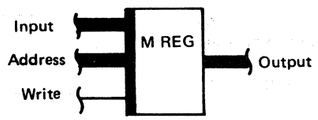
Decode

The active output is the output whose output value equals the sum of the active input values.









Flip Latch

Input side is denoted by a thick line. ALD reference page may be shown beneath.

Polarity Hold

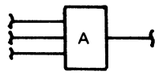
The 'output' of the polarity hold block is at the indicated polarity when both the 'data' and the 'control' lines go to their indicated polarity. When the 'control' line goes to the polarity opposite to that indicated, the 'output' line holds at the polarity it is at. When the 'clear' line goes to its indicated polarity, the 'output' line goes to the polarity opposite to that indicated.

Local Store

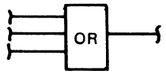
Read---Output from the local store addressed. Contents of local store is not destroyed.
Write---Input contents stored in the local store addressed when 'write' is active.

M REG

See Local Store



AND



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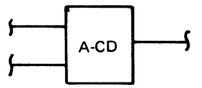
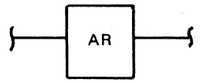
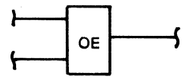


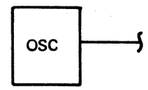
AND Current Driver



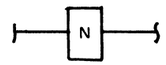
Amplifier



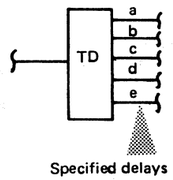
Exclusive OR



Oscillator



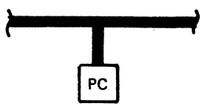
Negator (Inverter)



Time Delay

An input pulse starts the time delay. Each output pulse has the same duration as the input pulse but is delayed by the specified amount.

Legend
(Part 2 of 2)

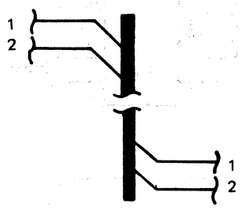


Parity Check

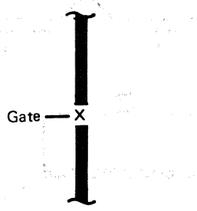
Parity check on the data bus

Parity Generate

Parity generated on the data bus



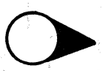
Multiple Line Transfer



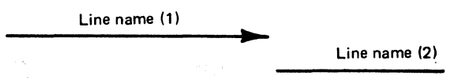
Gated Bus

Gate must be active for data to flow on bus.

Test Point

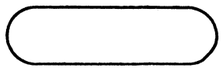


Signal that may be scoped.



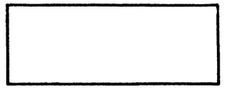
Above symbol indicates change in line name.

2. Flowcharts



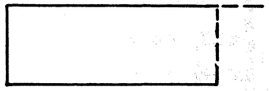
Terminal

Indicates the beginning or end of the event.



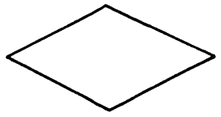
Process

Indicates a major function or event.



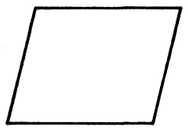
Annotation

Gives descriptive comment or explanatory note.



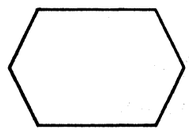
Decision

Indicates a point in a flowchart where a branch to an alternate path is possible.



Input-Output

CCU executes the control program input/output instructions.

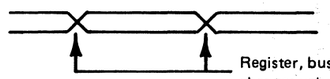


Hardware Process

Type 2 scanner hardware action resulting from input/output instructions or signals from the line/autocall interface.

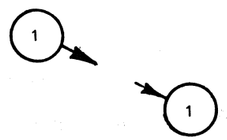
3. Timing Charts

Numerals at the beginning and end of the bar identify the signal(s) (also on the same chart) that activate and deactivate this line. '(Not)' with the number indicates that lack of the signal conditions the line.



Register, bus, or local store content changes value at these points.

4. General



On-page Connector

Indicates a connection between two parts of the same page. The arrow leaving the symbol points (line-of-sight) to a correspondingly-numbered symbol.

Off-page Connector

Indicates a connection between diagrams located on separate pages. The location of the correspondingly-lettered symbol is shown adjacent the symbol.

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CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power AC and DC when removing or assembling major components, working in immediate area of power supplies, performing mechanical inspection of power supplies and installing changes in machine circuity.
3. Wall box power switch when turned off should be locked or tagged in off position. "Do not Operate" tags, form 229-1266, affixed when applicable. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuity anywhere in the machine, the following precautions must be followed.
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Rings, wrist watches, chains, bracelets, metal cuff links, shall not be worn.
   c. Only insulated pliers and screwdrivers shall be used.
   d. Keep one hand in pocket.
   e. When using test instruments be certain controls are set correctly and proper capacity, insulated probes are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc. – use suitable rubber mats purchased locally if necessary).
5. Safety Glasses must be worn when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Parts cleaning, using solvents, sprays, cleaners, chemicals, etc.
   f. All other conditions that may be hazardous to your eyes. REMEMBER, THEY ARE YOUR EYES.
6. Special safety instructions such as handling Cathode Ray Tubes and extreme high voltages, must be followed as outlined in CEM's and Safety Section of the Maintenance Manuals.
7. Do not use solvents, chemicals, greases or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Lift by standing or pushing up with stronger leg muscles–this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
11. All safety devices such as guards, shields, signs, ground wires, etc. shall be restored after maintenance.
12. Each Customer Engineer is responsible to be certain that no action on his part renders product unsafe or exposes hazards to customer personnel.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. All machine covers must be in place before machine is returned to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it (i.e., under desk or table).
16. Avoid touching mechanical moving parts (i.e., when lubricating, checking for play, etc.).
17. When using stroboscope–do not touch ANYTHING–it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CE's and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machine while performing and after completing maintenance.

KNOWING SAFETY RULES IS NOT ENOUGH
AN UNSAFE ACT WILL INEVITABLY LEAD TO AN ACCIDENT
USE GOOD JUDGMENT – ELIMINATE UNSAFE ACTS

229-1264-1

Artificial Respiration
GENERAL CONSIDERATIONS

1. **Start Immediately, Seconds Count**
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim or apply stimulants.
2. **Check Mouth for Obstructions**
   Remove foreign objects–Pull tongue forward.
3. **Loosen Clothing–Keep Warm**
   Take care of these items after victim is breathing by himself or when help is available.
4. **Remain in Position**
   After victim revives, be ready to resume respiration if necessary.
5. **Call a Doctor**
   Have someone summon medical aid.
6. **Don't Give Up**
   Continue without interruption until victim is breathing without help or is certainly dead.

Rescue Breathing for Adults
Victim on His Back Immediately

1. **Clear throat** of water, food, or foreign matter.
2. **Tilt head back** to open air passage.
3. **Lift jaw up** to keep tongue out of air passage.
4. **Pinch nostrils** to prevent air leakage when you blow.
5. **Blow** until you see chest rise.
6. **Remove your lips** and allow lungs to empty.
7. **Listen** for snoring and gurglings, signs of throat obstruction.
8. **Repeat mouth to mouth breathings** 10-20 times a minute.

Continue rescue breathing until he breathes for himself.

NO

Thumb and finger positions

Final mouth to mouth position

Reprint Courtesy Mine Safety Appliances Co.

LOCATION OF LOGIC PAGES BY VOLUME NUMBER

Volume	Logic Pages	Contents
41	YZ	Power supply-installation instruction
42	AA–CV	CCU
A42	CW–CZ	ROS-Type 2 attachment base–CCU
43	DF–DZ	CCU
44	MM	Storage
45	TA–TB	Type 2 scanner
46	VA	LIB-reference material
47	VB	LIB-line sets 1, 2, 3, 4, 5, 8, and 9
48	RA–RS	Type 1 channel adapter
A48	PA–PS	Type 4 channel adapter
49	GA–GC	Remote Program Loader Diskette Controller

Introduction to the 3705-80

The IBM 3705-80 Communications Controller is a transmission control unit with processing capabilities. Its functions are controlled by a program that resides in controller storage.

The 3705 is available in 4 models, based on the maximum line-attachment capability. (The actual number of lines that the 3705-80 can support depends upon such factors as line speed and the throughput capability of the control program.)

3705-80 contains a central control unit, a control panel, 256K of storage, a channel adapter, a communication scanner, and line interface bases and line sets.

Refer to the *Introduction to the IBM 3705-80 Communications Controller,* GA27-3304 for more introductory information.

CENTRAL CONTROL UNIT

The central control unit (CCU) contains the circuits and data flow paths necessary to execute the 3705-80 instruction set and to control 3705-80 storage and the attached adapters. The CCU operates under control of the 3705-80 control program.

CONTROL PANEL

The control panel contains the switches and lights necessary to control many 3705-80 functions manually. The control panel provides such functions as the ability to store and display information in storage and registers, the control and indication of power, the indication of status and error information, and operator and diagnostic controls.

STORAGE

The 3705-80 contains 256K bytes of storage only. This storage features automatic single-bit error correction, double-bit error detection, and a 1.0 microsecond cycle time. A storage protection mechanism in the CCU makes it possible to protect the contents of storage.

TYPE 1 CHANNEL ADAPTER

The type 1 channel adapter (type 1 CA) provides attachment to an IBM System/360, System/370, 4300 Processor, or a 3031, 3032, 3033, or 3081 Processor Complex byte-multiplexer channel. The type 1 CA requires intervention from the 3705-80 control program for each data transfer.

TYPE 2 COMMUNICATION SCANNER

The type 2 communication scanner provides the interface between the line interface bases and the central control unit. The scanner monitors the communication line for service requests.

The type 2 communication scanner hardware assembles and disassembles characters. It interrupts the control program only when an entire character is ready for transfer to or from a line. The type 2 scanner can handle lines at speeds up to 57,600 bps. The 3705-80 contains a single type 2 scanner only.

LINE INTERFACE BASES

Line interface bases (LIBs) attach the lines to the 3705-80. The single available LIB type handles requirements for different types of line terminations. Depending upon the line termination, as many as 8 lines can be attached through one LIB. The number of installed LIBs depends on the model. A maximum of two LIBs can be installed in the 3705-80.

BASIC LINE ATTACHMENT SEGMENT AND LINE SETS

Lines are attached to LIBs through basic line attachment segments and line sets. Depending upon the type of line termination, either one or two lines can be attached to one basic line attachment segment or line set.

REMOTE PROGRAM LOADER

A 3705-80, used only as a remote communications controller, requires a remote program loader instead of a channel adapter. The remote program loader consists of an ROS bootstrap program, a diskette, a diskette drive, and a diskette controller. It is used to load a control program from a local 3705-80 to a remote 3705-80 via an SDLC communication facility. Internal functional tests for the remote 3705 reside on the diskette.

In addition to the RPL feature, the 3705-80 can contain a channel adapter. With both features installed, internal function tests (IFTs) can be run using either the channel or the RPL feature.

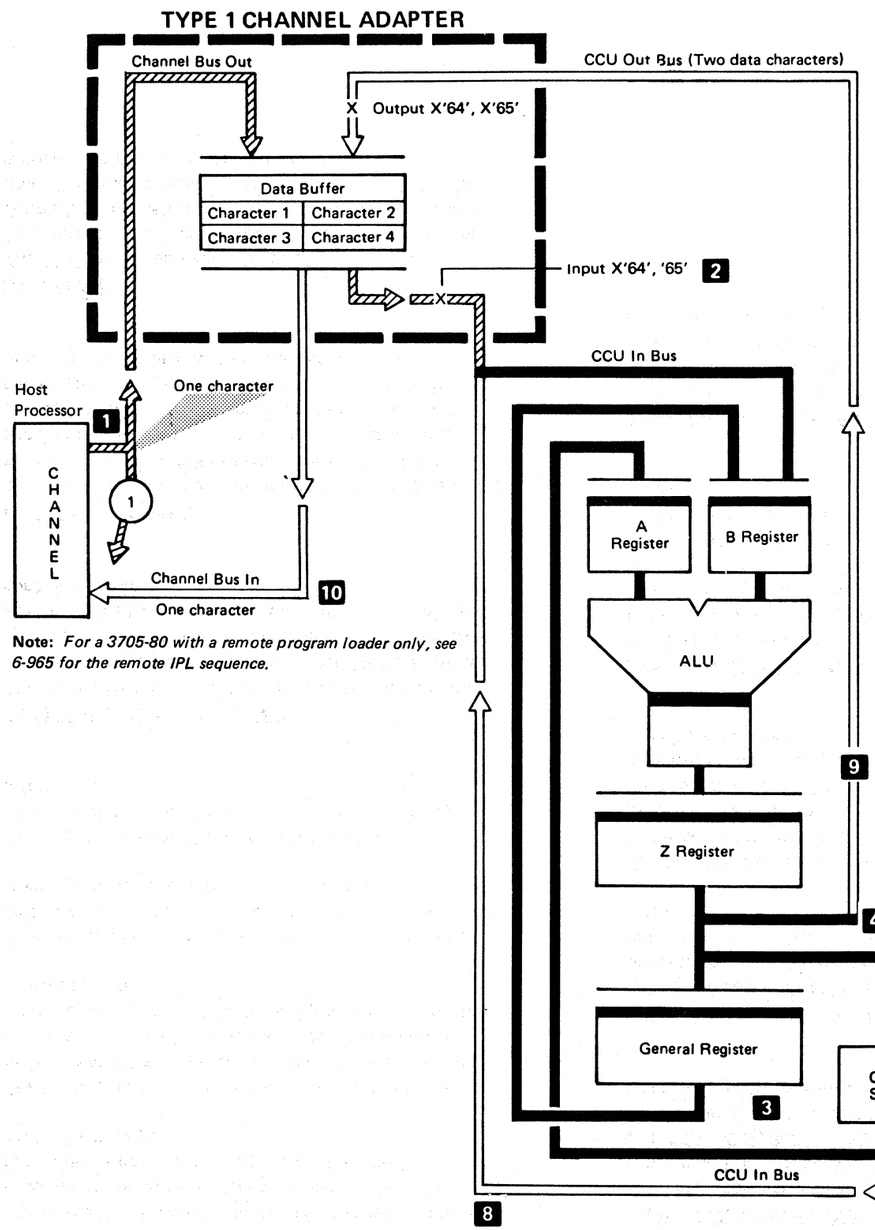
For a 3705-80 containing an RPL feature only (no channels), all IFTs are contained on the diskette.

TYPE 4 CHANNEL ADAPTER

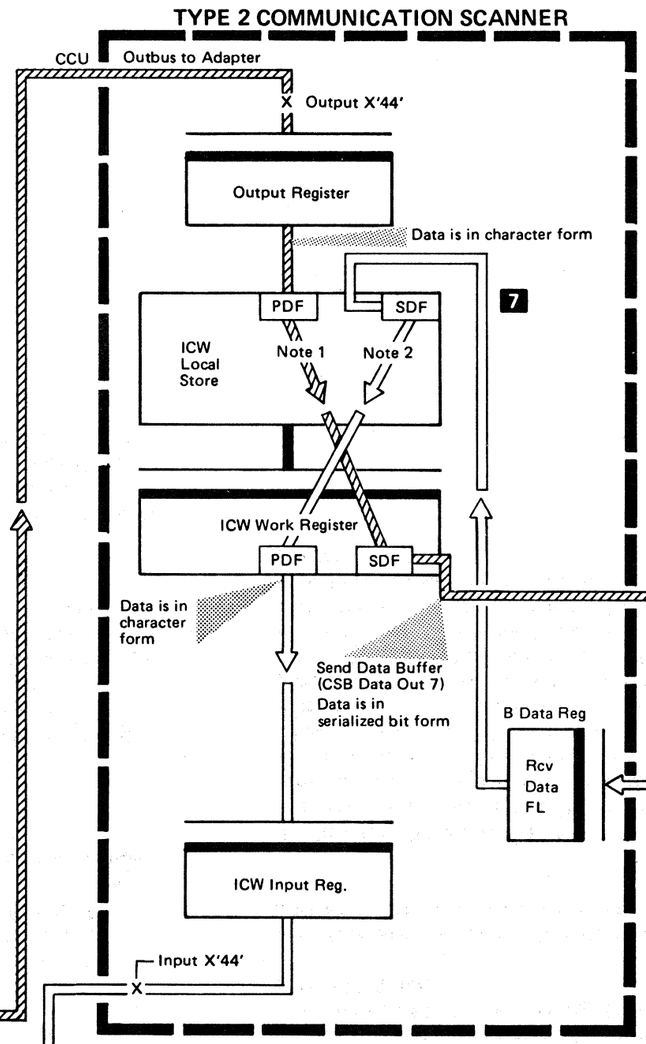
The type 4 channel adapter (type 4 CA) is a modified type 1 CA that enables the control program to transfer across the channel interface multibyte bursts of up to 32 bytes in extended buffer mode with program intervention required only before and after each burst. A plugging option allows the burst to be subdivided into groups of 4, 8, or 16 bytes with the type 4 CA disconnecting from the channel interface and reconnecting for each group to allow other channel activity to occur. The Type 4 CA can also transfer data by cycle steal under program control.

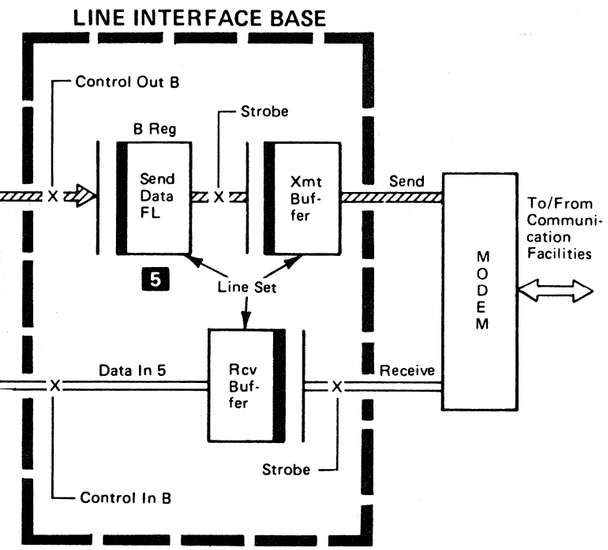
3705-80 DATA FLOW – WITH TYPE 1 CA (PART 1 OF 2)

Refer to page 0-020 for description



Note: *For a 3705-80 with a remote program loader only, see 6-965 for the remote IPL sequence.*





Notes:

1. *During a transmit operation, the character in the PDF is transferred to the SDF as the last bit of the previous character is being transferred from the SDF.*
2. *During a receive operation, the character in the SDF is transferred to the PDF as the last bit of the character is received.*

Note: *The data is transmitted or received one bit at a time through the Line Interface Base. The line 'bit service request' must be active.*

Legend

- Transmit Data Flow
- Receive Data Flow
- Common Data Flow

3705-80 DATA FLOW – WITH TYPE 1 CA (PART 2 OF 2)

THESE DESCRIPTIONS REFER TO PAGE 0-010

High Level Data Flow From the Host Processor to the Communication Facilities (Transmit)

1 The channel adapter issues a request for service to the channel to transfer data into its data buffer.

2 An Input X'64' gates data characters 1 and 2 to the CCU In Bus. An Input X'65' gates data characters 3 and 4 to the CCU In Bus.

3 The two data characters are stored in the general register specified by the input instruction.

The control program places the data to be sent to the scanner in the bytes of a general register.

4 An Output X'44' gates the data character from byte 1 of the general register through CCU logic to the 'output register'. The Output X'44' places the data character in bit positions 8–15 (parallel data field bits 0–7) of the ICW (interface control word) previously selected by the control program. Scanner hardware transfers the data character from the 'parallel data field' to the 'serial data field' where the character is serialized.

5 When the scanner addresses the line and the line's 'bit service request' is active, the serialized bit is buffered in the 'send data' latch of the line set's B register. The strobe, controlled by the transmit oscillator or the modem transmit clock, gates the bit to the transmit buffer where it is sent to the communication facility.

High Level Data Flow From the Communication Facilities to the Host Processor (Receive)

6 The line set strobes the received bit into its receive buffer.

When the type 2 scanner addresses this line interface and 'bit service request' is active, the scanner gates the received data bit (data in 5) to the 'received data' latch.

7 The type 2 scanner assembles the received bits into a character in the ICW 'serial data field' for that line interface. The scanner then transfers the character to the ICW 'parallel data field'. When the CCU accepts the scanner character service interrupt, the scanner gates the character to the ICW 'input register'.

8 An Input X'44' gates the character from the ICW 'input' register to the general register specified by the input instruction.

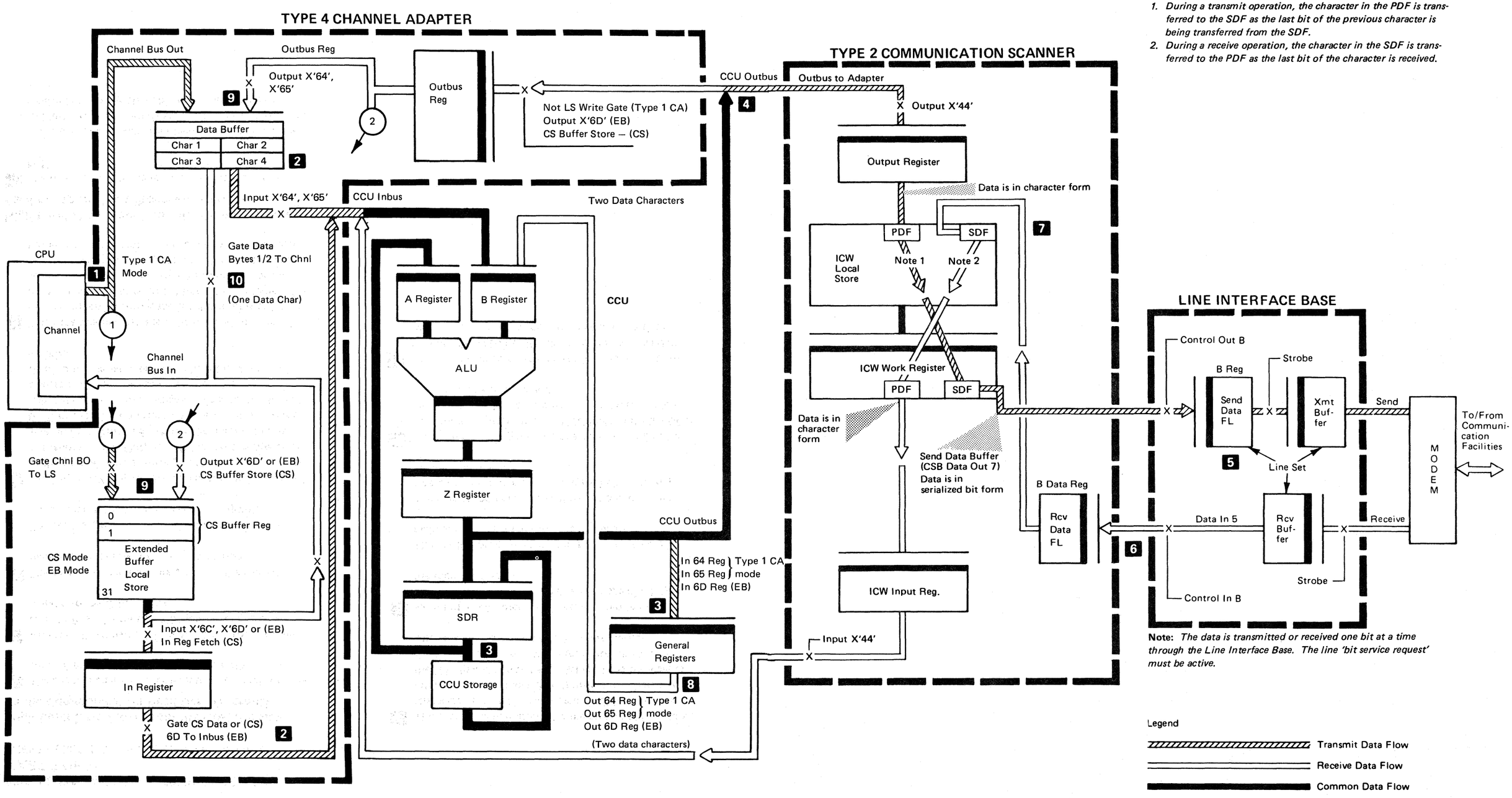
The control program must prepare the data now in main storage for use by the channel adapter.

The control program places the next two data characters to be transferred to the type 1 channel adapter in a general register.

9 An Output X'64' gates data character 1 and 2 out of the general register, through CCU logic, onto the CCU Out Bus to the CA 'data buffers'. An Output X'65' gates data characters 3 and 4.

10 The channel adapter issues a service request to transfer data characters to the Channel Bus In. The data characters are transferred one character at a time.

3705-80 DATA FLOW – WITH TYPE 4 CA (PART 1 OF 2)



Notes:

1. *During a transmit operation, the character in the PDF is transferred to the SDF as the last bit of the previous character is being transferred from the SDF.*
2. *During a receive operation, the character in the SDF is transferred to the PDF as the last bit of the character is received.*

Note: *The data is transmitted or received one bit at a time through the Line Interface Base. The line 'bit service request' must be active.*

3705-80 DATA FLOW WITH TYPE 4 CA (PART 2 OF 2)

THESE DESCRIPTIONS REFER TO PAGE 0-030

High Level Data Flow From the Host Processor to the Communication Facilities (Transmit)

1 After the type 4 CA responds to a Write type command, the CA issues a request for service to the channel to transfer data to the CA data buffer.

2
- Type 1 CA mode – An Input X'64' gates data characters 1 and 2 to the CCU In Bus. An Input X'65' gates data characters 3 and 4 to the CCU In Bus.
- EB mode – The data characters are loaded into the 32 character extended-buffer local store. The CA4 sets data characters 1 and 2 into the In register with an Input X'6C' – the remaining 30 with Input X'6D'. Input X'6D's gate two data characters to the CCU Inbus.
- CS mode – Two data characters are loaded in the two character CS buffer register in the EB local store. Cycle steal timings gate the two data characters to the In register then to the CCU In Bus.

3
- Type 1 CA mode – The two data characters are stored in the general register specified by the Input instruction.
- EB mode – Same as for type 1 CA mode.
- CS mode – The cycle steal operation gates the two data characters through CCU logic to storage.

4 An Output X'44' gates the data character from byte 1 of the general register through CCU logic to the 'output register'. The Output X'44' places the data character in bit positions 8–15 (parallel data field bits 0–7) of the ICW (interface control word) previously selected by the control program. Scanner hardware transfers the data character from the 'parallel data field' to the 'serial data field' where the character is serialized.

5 When the scanner addresses the line and the line's 'bit service request' is active, the serialized bit is buffered in the 'send data' latch of the line set's B register. The strobe, controlled by the transmit oscillator or the modem transmit clock, gates the bit to the transmit buffer where it is sent to the communication facility.

High Level Data Flow From the Communication Facilities to the Host Processor (Receive)

6 The line set strobes the received bit into its receive buffer.

When the type 2 scanner addresses this line interface and 'bit service request' is active, the scanner gates the received data bit (data in 5) to the 'received data' latch.

7 The type 2 scanner assembles the received bits into a character in the ICW 'serial data field' for that line interface. The scanner then transfers the character to the ICW 'parallel data field'. When the CCU accepts the scanner character service interrupt, the scanner gates the character to the ICW 'input register'.

8 The control program must prepare the data now in main storage for use by the type 4 CA depending on the CA mode.
- Type 1 CA mode – the control program places the next two data characters to be transferred to the channel adapter in a general register.
- EB mode – Same as for type 1 CA mode.
- CS mode – The control program places the received data characters into appropriate areas of main storage for subsequent cycle-steal operations and sets up the CA to transfer the data to the channel.

9
- Type 1 CA mode – An Output X'64' gates data characters 1 and 2 from the general register, through CCU logic, onto the CCU Out Bus through the outbus register to the CA 'data buffers'. An Output X'65' gates data characters 3 and 4.
- EB mode – An Output X'6D' gates data characters 1 and 2 from the general register, through CCU logic, onto the CCU Out Bus to set the outbus register. The CA then loads the data into the EB local store where 32 data characters can be buffered.
- CS mode – A cycle-steal operation gates two data characters through CCU logic onto the CCU Out Bus, through the outbus register to the CS buffer register in the EB local store.

10 After the type 4 CA responds to a Read type command, the CA issues a service request to the channel to transfer data characters to the channel Bus In. The data characters are transferred one character at a time.

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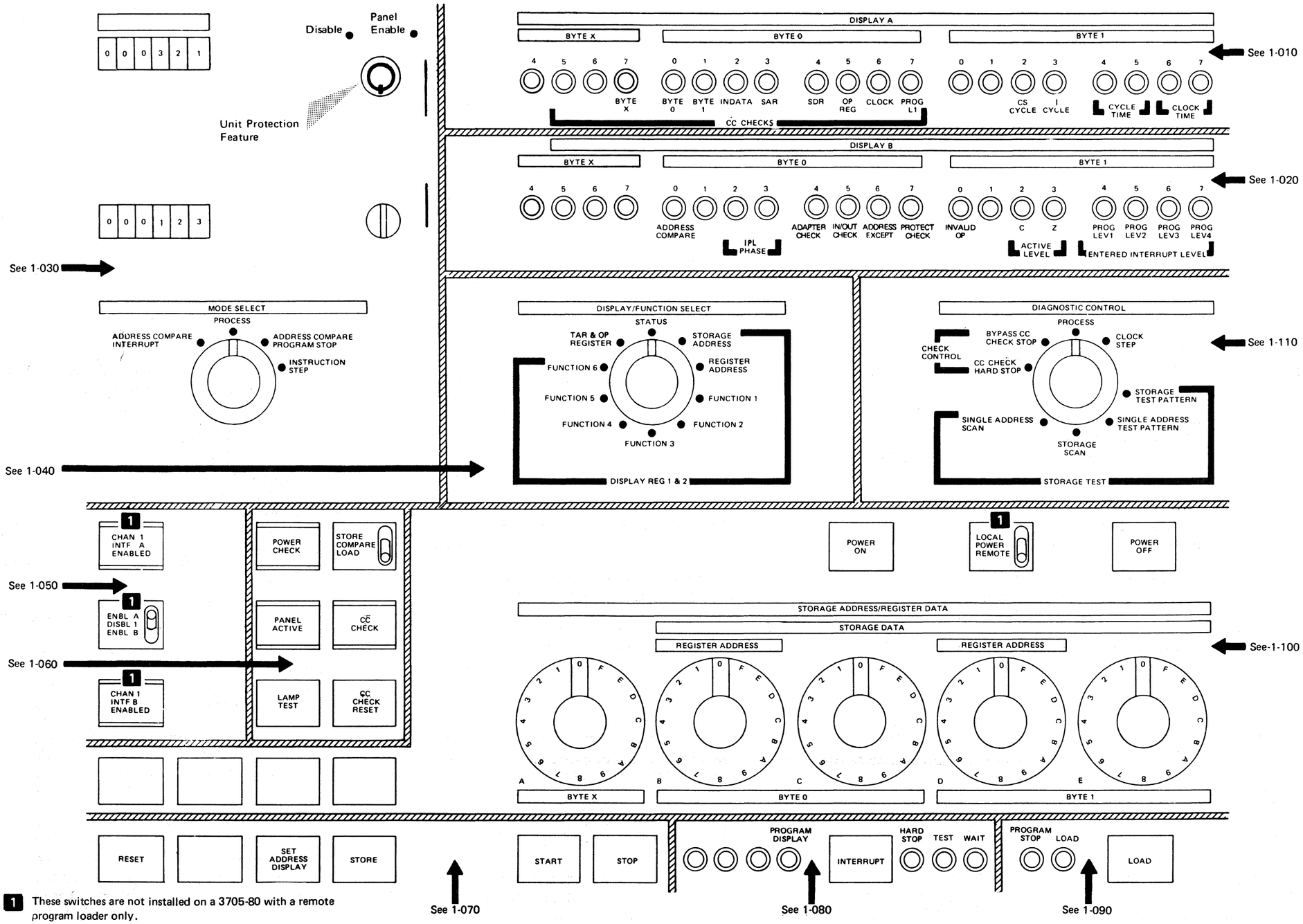
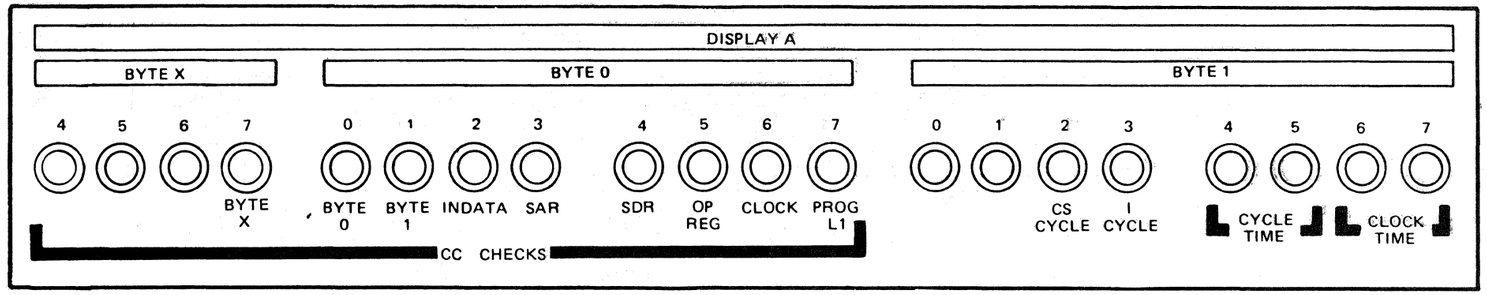
Control Panel Layout



1 These switches are not installed on a 3705-80 with a remote program loader only.

DISPLAY A

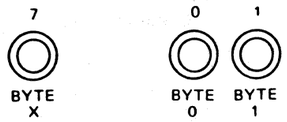


Display A Check Lights

The DISPLAY/FUNCTION SELECT switch must be in STATUS to display check conditions in display A.

- Any of the following turn off the display A check lights if additional checks are not detected:
  a. Pressing the CC CHECK RESET pushbutton.
  b. Pressing the RESET pushbutton.
  c. Executing an Output X'77' instruction with bit 0.1 on in the general register designated by the R field of the instruction (when in bypass CC check stop mode).
  d. Executing an Output X'77' instruction from the control panel by storing a "1" in bit 0.1 of external register X'77'. (See 1-140.) (The 3705-80 must be in program stop mode.)

Byte X, 0, and 1



- Turned on by the CCU (Central Control Unit) check register when a parity check occurs in the data path. If one or more of the BYTE lights are on, but no other CC CHECK light is on, the parity check is in the ALU (arithmetic logic unit), the A register, the B register, or the Z register.

Note: *If the IPL is not successfully completed, the local store registers can cause a parity check because they are not initialized.*

Indata

- Turned on when the CCU detects a parity error on the 'indata' bus.

The BYTE X, BYTE 0, and/or BYTE 1 CHECK light and the CC CHECK light also come on.

SAR

- Turned on when a SAR (storage address register) parity check occurs.

The BYTE X, BYTE 0, and/or BYTE 1 CHECK light and the CC CHECK light also come on.

SDR

- Turned on when an SDR (storage data register) parity check occurs.

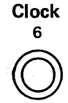
The BYTE 0 and/or BYTE 1 CHECK light and the CC CHECK light also come on.

Op Reg

- Turned on when an OP (operation) register parity check occurs.

The BYTE 0 and/or BYTE 1 CHECK light and the CC CHECK light also come on.

Clock



- Turned on when a CCU or CS (communication scanner) support feature clock check occurs.

Prog L1

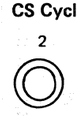
- Turned on when in program level 1, and one of the following occurs, causing a CC check.
  a. In/out check
  b. Protect check
  c. Invalid op check

If any one of these occurs in program level 1, it causes a CC check.

Display A Status Lights

The DISPLAY/FUNCTION SELECT switch must be in STATUS to display status conditions in display A.

CS Cycle



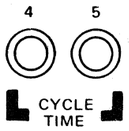
- Turned on at T0 of A time during a cycle steal cycle.
- Turned off after T3 of D time if no other cycle steal is to follow immediately.

I Cycle

- Turned on at T0 of A time during a control panel function cycle steal cycle.
- Turned off after T3 of D time during instruction execution cycles if no other instruction cycle is to follow immediately.

If this light is off for any noticeable length of time, the HARD STOP, PROGRAM STOP, or WAIT light should be on for the same length of time.

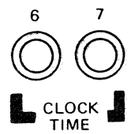
Cycle Time



- Displays a binary designation of the four basic cycle times. (See the chart below.)

During normal operation, the 3705-80 cycle times are 250 nanoseconds in duration and are under the control of the machine oscillator. To observe the stepping of these lights, set the DIAGNOSTIC CONTROL switch to CLOCK STEP and repeatedly press the START pushbutton.

Clock Time



- Displays a binary designation of the four basic clock times. (See the chart below.)

During normal operation the clock times are 62.5 nanoseconds in duration and are under the control of the machine oscillator. To observe the stepping of these lights, set the DIAGNOSTIC CONTROL switch to CLOCK STEP and repeatedly press the START pushbutton.

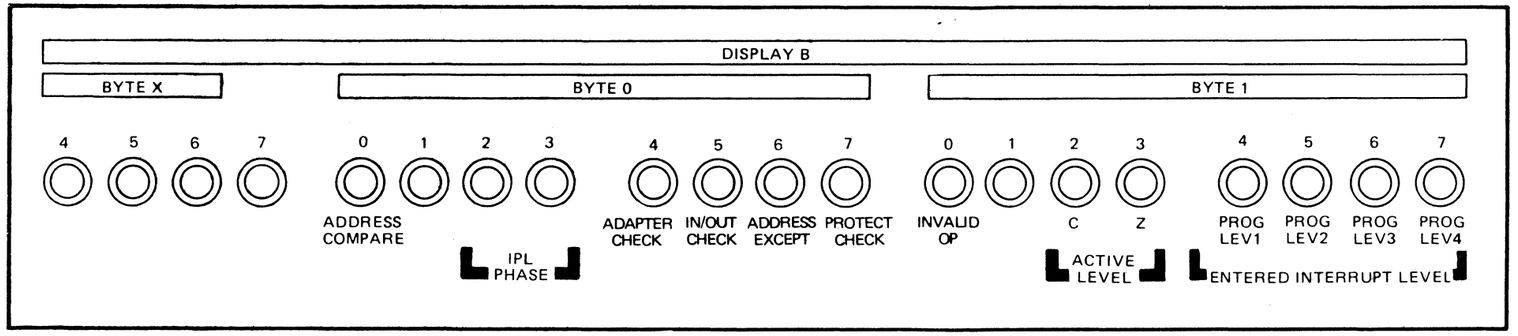
Cycle Time	A				B			
Clock Time	T0	T1	T2	T3	T0	T1	T2	T3
Bit 1.4 light	0				0			
Bit 1.5 light	0				1			
Bit 1.6 light	0	0	1	1	0	0	1	1
Bit 1.7 light	0	1	0	1	0	1	0	1

Cycle Time	C				D			
Clock Time	T0	T1	T2	T3	T0	T1	T2	T3
Bit 1.4 light	1				1			
Bit 1.5 light	0				1			
Bit 1.6 light	0	0	1	1	0	0	1	1
Bit 1.7 light	0	1	0	1	0	1	0	1

Lights indicate the clock time that was just completed.

DISPLAY B

Note: *For control panel storage-address and storage-scan functions. DISPLAY B BYTE X should be ignored because storage operates only on halfwords.*



Display B Status Lights

The DISPLAY/FUNCTION SELECT switch must be in STATUS to display status conditions in display B.

Address Compare

0 ADDRESS COMPARE

- Turned on during instruction cycles when the address compare conditions described under LOAD/STORE ADDRESS COMPARE switch on page 1-060 are met.
- Turned off during the next cycle unless the PROGRAM STOP light is on.

IPL Phase

2 3 IPL PHASE

- Displays a binary designation of the three IPL (Initial Program Load) phases.

  Both lights turn off at the end of IPL initialization when the program executes Output X'77' with bit 0.0 on. Reinitialization of the IPL also turns both lights off.

  Unless the DIAGNOSTIC CONTROL switch is in CLOCK STEP, IPL phases 1 and 2 should be hardly noticeable. If these lights stay on, it indicates a hardware failure.

A persistent IPL phase 3 indication is likely to be caused by either a hardware failure in read-only storage, a program failure, a CCU failure, or the host processor not loading the 3705-80.

The 'IPL phase' latches are on CU010.

IPL Phase	*Display B Light*	
	0.2	*0.3*
1	0	1
2	1	0
3	1	1

C and Z Level

2 3 C Z ACTIVE LEVEL

- Indicates the C and Z condition latches for the active program level.

Entered Interrupt Level

4 5 6 7 PROG LEV1 PROG LEV2 PROG LEV3 PROG LEV4 ENTERED INTERRUPT LEVEL

- Indicates which of the five program levels are active or have interrupt requests entered. (No light indicates that level 5 is active if instructions are being executed.)
- Turned on when an interrupt occurs for that program level.
- Turned off when one of the following occurs:
  a. Exit instruction is executed at that level.
  b. 'Interrupt entered' latch for that level is reset by a machine reset.

If more than one of these lights are on, the highest priority program level indicated is the active level. Program level 5 is active when none of these lights are on and instructions are being executed.

Display B Check Lights

The DISPLAY/FUNCTION SELECT switch must be in STATUS to display check conditions in display B.

Adapter Check

4 ADAPTER CHECK

- Turned on when the type 1 channel adapter, type 4 channel adapter, or type 2 scanner requests a program level 1 interrupt. See page 8-360 (type 1 CA), H-380 (type 4 CA), or B-130 (type 2 scanner). An adapter check causes a level 1 interrupt. An adapter check while in program level 1 causes a CC check.
- Turned off when the interrupt request is reset.

In/Out Check

5 IN/OUT CHECK

- Turned on when the CCU detects one of the following.
  a. Invalid input or output instruction. (See page 6-151.)
  b. Parity check on the 'indata' bus execution of an input instruction.
  c. Execution of an input or output instruction while in program level 5.

An in/out check causes a level 1 interrupt. An in/out check in program level 1 causes a CC check.

- Turned off by one of the following:
  a. Machine reset occurs.
  b. Executing Output X'77' with bit 1.5 on in the register designated by the R field of the instruction (when in bypass CC check stop mode).
  c. Executing Output X'77' from the control panel by displaying register X'77' and then storing a '1' in bit position 1.5. (See 1-140.) (The 3705-80 must be in program stop mode.)

Address Exception

6 ADDRESS EXCEPT

Not Used

Protect Check

7 PROTECT CHECK

- Turned on when an attempt is made to change protected data. A protect check causes a level 1 interrupt. A protect check in program level 1 causes a CC check.
- Turned off by either:
  a. A machine reset.
  b. Executing an Output X'77' with bit 1.5 on in the register designated by the R field (when in bypass CC check stop mode).
  c. Executing Output X'77' from the control panel by displaying register X'77' and then storing a '1' in bit position 1.5. (See 1-140.) (The 3705-80 must be in program stop mode.)

Invalid OP

0 INVALID OP

- Turned on when the CCU detects an invalid OP code. An invalid op check causes a level 1 interrupt. An invalid op check in program level 1 causes a CC check.
- Turned off by any of the following:
  a. A machine reset.
  b. Executing Output X'77' with bit 1.5 on in the register designated by the R field (when in bypass CC check stop mode).
  c. Executing an Output X'77' from the control panel by displaying register X'77' and then storing a '1' in bit position 1.5. (See 1-140.) (The 3705-80 must be in program stop mode.)

CONTROL PANEL SWITCHES AND LIGHTS

Customer and CE Usage Meters

The 3705-80 has a customer usage meter (top meter) and a CE usage meter. The meters show the run time in hours and tenth hours. The CE Key switch position determines which meter is conditioned to run. The minimum usage meter run time is 400 msec. The following list tells when one of the meters should be running.

The 400 msec minimum time is reinitiated when one of the following occurs:

a. An instruction is executed at program level 1, 2, 4, or 5.
b. An instruction is executed at program level 3 after approximately 8ms have elapsed since the interval timer interrupt request was set.
c. An instruction is executed at program level 3 and an interrupt request other than the interval timer level 3 interrupt request is set.
d. A cycle steal cycle occurs.

Neither meter runs during:

a. Idle cycles.
b. IPL phases 1-3.

Note: *The meter will run if the Emulation Program is loaded, the access method is not operating, and the DISPLAY/FUNCTION SELECT switch is set to function 1 or 6. Return the switch to the STATUS position to prevent unnecessary meter time.*

Mode Select Switch

- Controls the 3705-80 mode of operation.

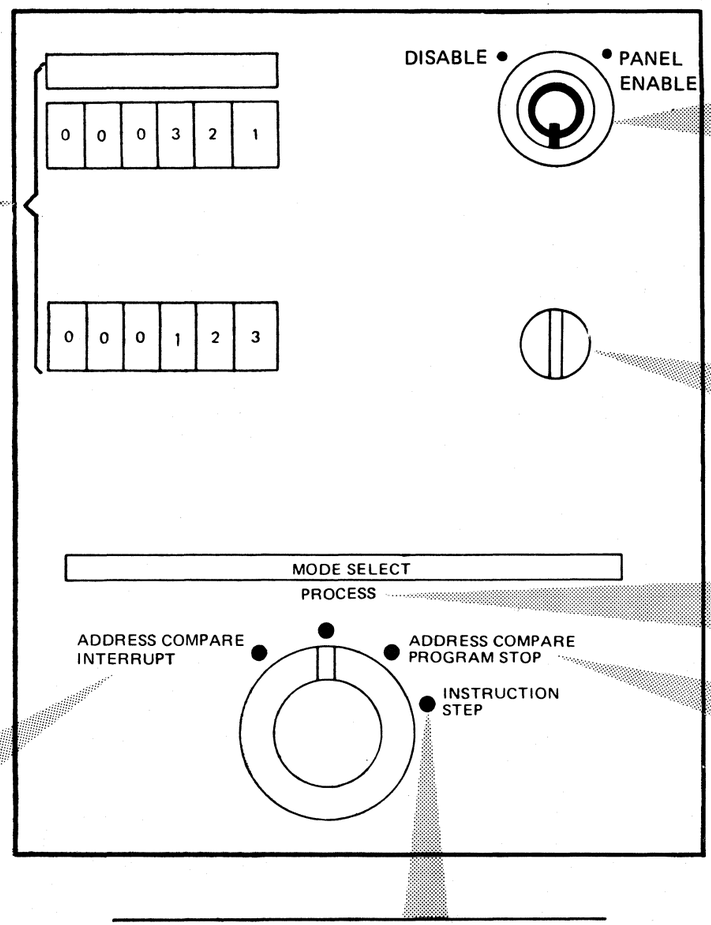
When the PANEL ACTIVE light is off, the 3705-80 runs as if the MODE SELECT switch and the DIAGNOSTIC CONTROL switch were in PROCESS, no matter what position the switches are in.

Note: *If the panel is active and DIAGNOSTIC CONTROL switch is in any one of the STORAGE TEST positions or in the CLOCK STEP position, it overrides the MODE SELECT switch.*

Address Compare Interrupt

- Causes the address compare L1 interrupt request to set at the end of the instruction if the address compare conditions described in *LOAD/STORE ADDRESS COMPARE SWITCH* on page 1-060 are met.

The 3705-80 operates normally except for the interrupt request when an address compare occurs.



Instruction Step

- Causes the 3705-80 to execute one instruction each time the START pushbutton is pressed and released.

The 'program stop' latch sets after the execution of the instruction. All interrupts except program L1 and PCI interrupts to higher program levels are inhibited until an 'exit' instruction is executed. After an 'exit' instruction is executed, the machine cycle priority controls determine which program level is active until the next 'exit' instruction, PCI to a higher level, or program level 1 interrupt.

Unless it is already set, the interval timer L3 interrupt request cannot be set when the MODE SELECT switch is in this position.

Panel Enable/Disable Switch

- Available as the Unit Protection Feature.
- This allows the operator to disable/enable the operator panel switches (except POWER ON/OFF, CHANNEL ENABLE/DISABLE, and DISPLAY/FUNCTION SELECT with a key controlled switch.

The disable position will prevent inadvertent or unauthorized use of the control panel.

When in the disable position the setting of the Storage Address/Register Data switches can be entered as input by the program. When in the disable position and EP (emulation program) mode, the display lights can still be used.

CE Key Switch

- Determines whether the CE or the customer usage meter is conditioned to run.

If the slot is vertical, the customer usage meter is conditioned to run. If it is horizontal, the CE usage meter is conditioned to run.

Process

- Allows the 3705-80 to run normally.

If the MODE SELECT switch is in any other position, the TEST light comes on.

Address Compare Program Stop

- Causes a program stop at the end of the instruction if the address compare conditions described in *LOAD/STORE ADDRESS COMPARE SWITCH* on page 1-060 are met.

With the switch in this position, an address compare detection does not set the address compare L1 interrupt request.

WARNING
When the 'program stop' latch is set, cycle steal operations can cause adapter problems.

Display/Function Select Switch

- Used to display or store in storage or register; to display machine status or TAR and the Op register; and to make on line parameter changes.

In any position, except STATUS or TAR & OP REGISTER, displays A and B show the contents of display registers 1 and 2.

Tar & Op Register

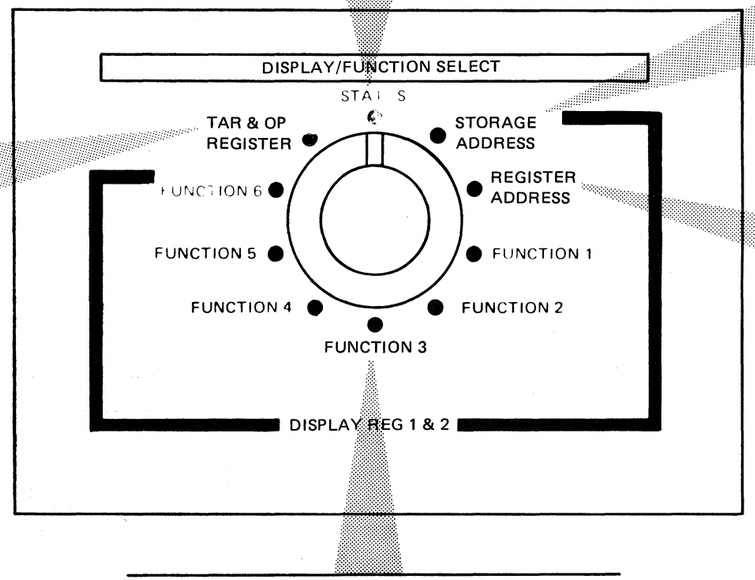
- Causes display A to show the contents of TAR (Temporary Address Register).
- Causes display B, bytes 0 and 1 to show the contents of the Op register. (Ignore byte X.)

Note: *After a REGISTER ADDRESS, STORAGE ADDRESS, or STORAGE TEST function, the TAR & OP REGISTER position will no longer display the last previous TAR and OP code. Therefore, display and record these values before you do any other displaying if you will later need this information.*

Status

- Causes displays A and B to show check and status information.

See page 1-010 and 1-020 for information about the check and status lights.



Functions 1-6
The active program determines the function of the FUNCTION 1-6 positions.

Storage Address

- Used to select a storage address for displaying storage and for storing data in a storage location.

Pressing and releasing the SET ADDRESS/DISPLAY pushbutton with the DISPLAY/FUNCTION SELECT switch in this position causes a display storage CS1 maintenance cycle. (See page 1-120, *Set Address and Display Storage Procedure.)*

Pressing and releasing the STORE pushbutton with the DISPLAY/FUNCTION SELECT switch in this position causes a store storage CS1 maintenance cycle and a store storage CS2 maintenance cycle if the 3705-80 is in a stopped state. (See page 1-130, *Storing Data in Storage Locations.)*

Register Address

- Used to select a register address for displaying a register and for storing data in a register.

Pressing and releasing the SET ADDRESS/DISPLAY pushbutton causes a display register CS1 maintenance cycle. (See page 1-120, *Set Address and Display Register Procedure.)*

Pressing and releasing the STORE pushbutton causes a store register CS1 maintenance cycle if the 3705-80 is in a stopped state.

Channel 1 Interface Enable/Disable Switch (Single Channel Adapter)

WARNING
When operating with a type 1 or type 4 CA in an NCP (PEP included) environment, do not attempt to disable a channel interface unless the 3705-80 network has been quiesced or a system reset has occurred. If this procedure is not followed, the NCP may, while disabled, attempt to send asynchronous status which inhibits the CA1 or CA4 from becoming enabled again.

- Used to enable and disable channel interfaces 1A and 1B. Refer to 8-140 (Type 1 CA) for a description of interfaces 1A and 1B.

If the DIAGNOSTIC CONTROL switch is in one of the four STORAGE TEST positions and the START pushbutton is pressed, any interface that is enabled is disabled abruptly. The CHANNEL INTERFACE ENABLED light stays on until the host processor drops 'clock out', even though the interface is disabled. No channel can become enabled.

Note: *Be sure the channel is disabled before performing storage test operations.*

ENBL A
- Used to enable interface 1A.
- Interface 1B is disabled.

If interface 1B is installed and enabled and the switch is turned to this position, interface 1B is disabled when 'clock out' drops on interface 1B and command chaining stops. Channel 1A is enabled when these conditions are met.

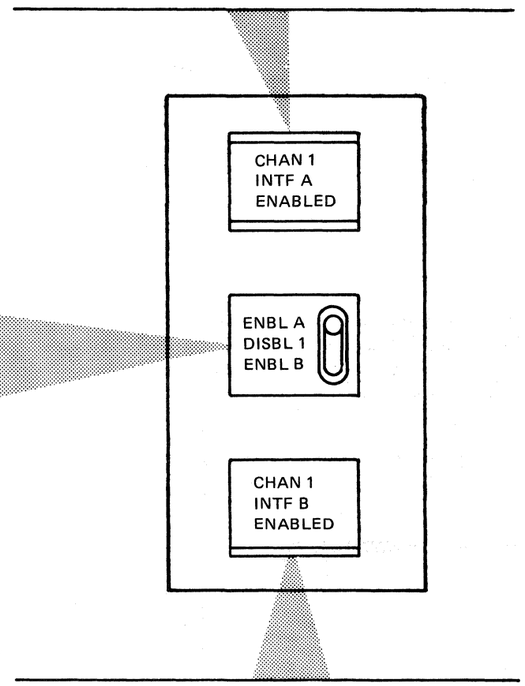
DISBL 1
- Used to disable both interfaces 1A and 1B.

If one of the interfaces is enabled when you set the switch to DISBL 1, the interface is disabled when 'clock out' drops on that interface, and command chaining stops. Pressing the RESET pushbutton with the switch in DISBL 1 also disables the interface.

ENBL B
- Present only if the 3705-80 has the Two-Channel Switch feature for channel interface 1.
- Causes the same results for interface 1B that are described under *ENBL A.*

Channel 1 Interface A Enabled Light
- Turned on when interface 1A is enabled.
- Turned off when interface 1A is disabled.

Note: *The light stays on when the 3705-80 is in hard stop, even though the adapter is disabled.*



Channel 1 Interface B Enabled Light
- Turned on when interface 1B is enabled.
- Turned off when interface 1B is disabled.

Note: *The light stays on when the 3705-80 is in hard stop, even though the adapter is disabled.*

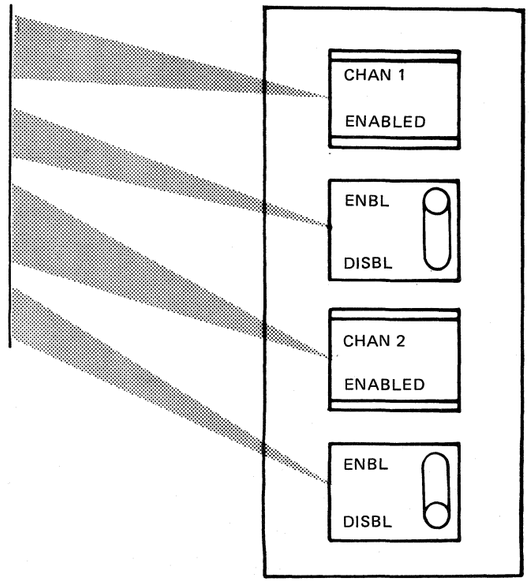
Channel 1/Channel 2 Enable/Disable Switches (Two Type 4 CAs)

Chan 1 Enabled
- Turned on when CA4 #1 is enabled.
- Turned off when CA4 #1 is disabled.

ENBL/DISBL
- Used to enable/disable CA4 #1.

Chan 2 Enabled
- Turned on when CA4 #2 is enabled.
- Turned off when CA4 #2 is disabled.

ENBL/DISBL
- Used to enable/disable CA4 #2.



Power Check Light

- Turned on when a power check occurs. (See D-010 for conditions that cause a power check.)
- Turned off by pressing the POWER-OFF pushbutton on the control panel, if a thermal condition does not exist.
- Also turned on and off during a normal power-on sequence.
- Not turned on by LAMP TEST pushbutton.

If the light is on because of a check condition, you cannot turn power on until you reset the check condition. If the power check resulted from an undervoltage sense, an overvoltage sense, or an overcurrent sense, reset the check by pressing the POWER OFF pushbutton. If the check resulted from an open thermal switch, reset the check by pressing the THERMAL RESET pushbutton located inside the covers of the 3705-80 (See D-520).

Panel Active Light

WARNING
When the PANEL ACTIVE light is on, all the control panel switches and pushbuttons are active.

- Turned on when the MODE SELECT and DIAGNOSTIC CONTROL switches have been in the PROCESS position at least once since the last power-on sequence.

If the light is off and 3705-80 power is on, the 3705-80 operates as if the switches were in the PROCESS position. However, the pushbuttons, except for the power controls, have no effect.

Lamp Test Pushbutton

- Turns on all control panel lights, except POWER CHECK and the spares.

Pressing the LAMP TEST pushbutton does not affect normal operation.

LOAD/STORE ADDRESS COMPARE SWITCH

Store Compare

- Used to determine if data from a general register is stored in a specific byte of storage. (See *Store Address Compare* on 1-140.)

With the switch in this position, the addresses in the ADDRESS/DATA switches and in SAR are compared during each I2 and I3 cycle of a ST, STC, STH or STCT instruction. If the addresses are equal, an address compare occurs, and the ADDRESS COMPARE light in display B comes on if the DISPLAY/FUNCTION SELECT switch is in STATUS.

During I2 cycle for STH and ST instructions, bit 1.7 of the addresses is ignored in the comparison. (Both bytes are stored in the storage halfword.)

During I2 cycle for STC and STCT instructions and I3 cycle for ST instructions, bit 1.7 is included in the comparison. (Only one byte is stored in the addressed storage halfword location.)

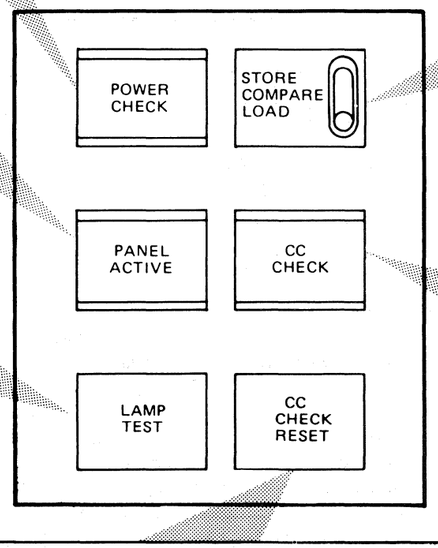
Load Compare

- Used to determine if an instruction loads data from a specific storage location into a general register. (See *Load Address Compare* page 1-140.)

The storage address in ADDRESS/DATA switches A-E is compared with SAR during each I1, I2 or I3 cycle of a load instruction. In this case a load instruction is any instruction except ST, STC, STH, or STCT. If the addresses are equal, an address compare occurs and the ADDRESS COMPARE light in display B comes on if the DISPLAY/FUNCTION SELECT switch is in STATUS.

During all I1 cycles, during I2 cycles for LH instructions, and during I3 cycles for the L instruction, bit 1.7 of the addresses is ignored in the address comparison. (Storage is addressed on a halfword basis.)

During I2 cycles for IC, ICT, and L instructions, bit 1.7 is included in the address comparison. (Storage is addressed on a byte basis.)



CC Check Reset Pushbutton

- Resets the CCU check register and turns off the CC CHECK light, if the CC checks are no longer present.

This pushbutton works only if the PANEL ACTIVE light is on.

CC Check Light

- Turned on when a CC check is detected.
- Turned off by any of the following:
  a. Pressing the CC CHECK RESET pushbutton if there are no more CC checks.
  b. Executing an Output X'77' with bit 0.1 on in the register designated by the R field of the instruction.
  c. Executing an Output X'77' from the control panel by displaying register X'77' and then storing a '1' in bit position 0.1. (See 1-140.)
  d. Pressing the RESET pushbutton if there are no more CC checks.

Use Input X'7D' or turn the DISPLAY/FUNCTION SELECT switch to STATUS to display the specific CC check in display A.

WARNING
MST cards are very sensitive and touching the pin side of certain cards can cause a CC check.

Note: *The CC CHECK light is referred to as the CCU check indicator in logic.*

Reset Pushbutton

Pressing the RESET pushbutton:

1. Sets the 'hard stop' and 'program stop' latches.
2. Sets odd parity in the local store register X'00'. (The data is not affected.)
3. Sets valid parity in the Op register and in SDR.
4. Sends a reset signal across the adapter interface to the 3705-80 adapters.
5. Logically disconnects the type 1 or type 4 channel adapter from the interface by not allowing select out to be trapped.
6. Signals to the adapters that a *not initialized* state exists until the state ends as a result of IPL.
7. Resets the CCU error register.
8. Masks program levels 2-5 and adapter level 1.

Note: *Output X'7F' must be executed to reset the mask bits.*

9. Resets the 'program level entered' latches.
10. Resets all CCU interrupt requests.
11. Sets the 'test mode' latch.
12. Aborts IPL phase 2, if it is active.

Set Address/Display Pushbutton

- Used to:
  a. Display the contents of a storage location, a CCU register, or an adapter external register in display B.
  b. Set the address of a storage location, CCU register, or adapter register for a store operation.

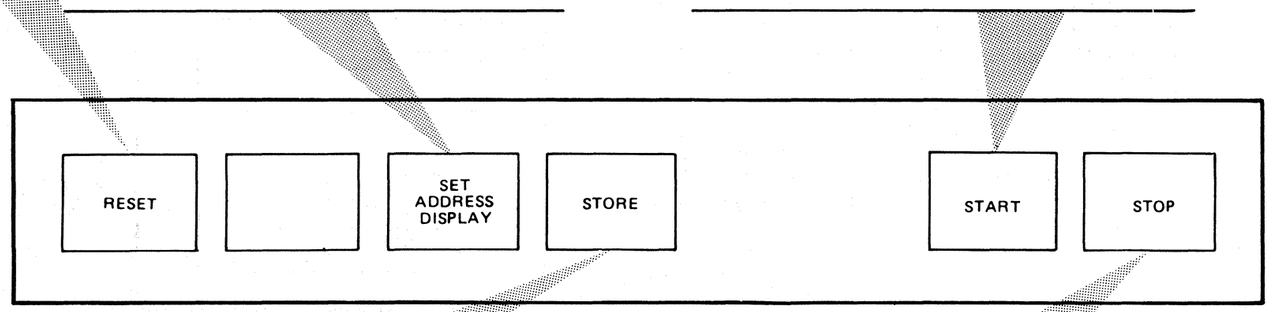
This pushbutton functions only when the PANEL ACTIVE light is on and the DISPLAY/FUNCTION SELECT switch is in REGISTER ADDRESS or STORAGE ADDRESS. It does not function during IPL phase 1 or 2 or when the DIAGNOSTIC CONTROL switch is in one of the four STORAGE TEST positions and you have pressed the START pushbutton (unless the 'hard stop' latch was set previously).

A dynamic display can be done provided a program display is not present.

Start Pushbutton

- Used to:
  a. Restart the program. Reset the 'hard stop' and 'program stop' latches if the DIAGNOSTIC CONTROL switch is in PROCESS, BYPASS CC CHECK STOP, or CC CHECK HARD STOP.
  b. Reset the 'hard stop' latch and start one of the four storage test functions.
  c. Start the clock step function to step the CCU clock when the DIAGNOSTIC CONTROL switch is in CLOCK STEP.

The START pushbutton works only if the PANEL ACTIVE light is on. Pressing the START pushbutton always causes a 1.2 usec CS1 start pushbutton maintenance cycle.



Store Pushbutton

WARNING
Be careful when you perform a store operation. The data stored may alter normal program operation. An adapter check can occur when channel cycle steals and store operations occur at the same time.

- Pressed and released to store data from the ADDRESS/DATA switches in a storage location or in a register.

The STORE pushbutton works only when the PANEL ACTIVE and PROGRAM STOP lights are on and the DISPLAY/FUNCTION SELECT switch is in REGISTER ADDRESS or STORAGE ADDRESS. It does not work during IPL Phase 1 and 2 or when the DIAGNOSTIC CONTROL switch is in one of the four STORAGE TEST positions and you have pressed the START pushbutton. The 'program stop' latch should be set before setting the address for the store operation.

Stop Pushbutton

- Pressed to set the 'program stop' latch and stop program execution at the next instruction boundary.

This pushbutton works only when the PANEL ACTIVE light is on. It does not stop adapter or maintenance cycle steal operations.

WARNING
When the 'program stop' latch is set, cycle steal operations can cause adapter problems.

Program Display Light

- Turned on when display register 1 or 2 contains program output. (CCU executed Output X'71' or X'72'.)
- Turned off when the CCU takes a maintenance cycle, or when you press and release the START pushbutton if the 'hard stop' or 'program stop' latch is on.

If the light is on, turn the DISPLAY/FUNCTION SELECT switch to a position other than TAR & OP REGISTER or STATUS. This causes displays A and B to display the data that is in display registers 1 and 2.

Hard Stop Light

- Turned on when the 'hard stop' latch sets.

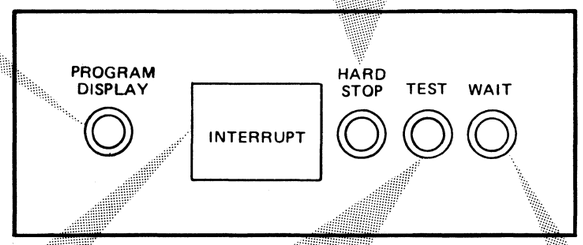
The 'hard stop' latch sets when any of the following happen.

a. The CCU executes Output X'70' when in program level 1, 2, 3, or 4.
b. The control panel is active, the DIAGNOSTIC CONTROL switch is in STORAGE SCAN or STORAGE TEST PATTERN, and a CCU check occurs.
c. The control panel is active, the DIAGNOSTIC CONTROL switch is in CC CHECK HARD STOP, and a CC check occurs.
d. The control panel is active, and you press the RESET pushbutton.
e. The 3705-80 is in IPL phase 2 or 3, and a CC check occurs (unless the 'bypass check stop' latch is set).
f. The control panel is active, and you turn the DIAGNOSTIC CONTROL switch to CLOCK STEP.

- Turned off when the 'hard stop' latch is reset.

The 'hard stop' latch is reset when any of the following happen.

a. A power-on reset occurs.
b. IPL phase 1 reset occurs.
c. The DIAGNOSTIC CONTROL switch is not in any of the four STORAGE TEST positions; none of the conditions that set the 'hard stop' latch are present; and you press the START pushbutton. If the DIAGNOSTIC CONTROL switch is in CLOCK STEP and you press the START pushbutton, the latch is reset during the start cycle, but not immediately.



Interrupt Pushbutton

- Causes a program level 3 interrupt request.

Before you press the INTERRUPT pushbutton, set the DISPLAY/FUNCTION SELECT switch and the ADDRESS/DATA switches according to the convention established by the program handling the request.

To reset the interrupt request, Output X'77' must be executed with bit 0.2 on in the register designated by the R field of the instruction. (The CE can execute this output by using the control panel. See 1-140.)

This pushbutton works only when the PANEL ACTIVE light is on.

Test Light

- Turned on when any of the following occur.
  a. The MODE SELECT switch is not in PROCESS.
  b. The DIAGNOSTIC CONTROL switch is not in PROCESS.
  c. The 'test mode' latch is set. (Note: The 'test mode' latch can be set by the control program via Output X'79' or by pressing the RESET pushbutton.)
- Turned off when all of the following occur.
  a. The MODE SELECT switch is in PROCESS,
  b. The DIAGNOSTIC CONTROL switch is in PROCESS,
  c. The 'test mode' latch is reset by the control program.

Wait Light

- Turned on when the CCU is in the wait state (running, but not taking instruction cycles or cycle steal cycles). Also comes on when the PROGRAM STOP or HARD-STOP light is on.
- Turned off when an interrupt occurs or the CCU takes a cycle steal cycle.

The usage meter does not run when the WAIT light is on.
For an explanation of the wait state, see "Idle Cycle " on 6-050.

Program Stop Light

- Turned on when the 'program stop' latch sets.

The 'program stop' latch sets when one of the following happens.

a. The control panel is active; the MODE SELECT switch is in ADDRESS COMPARE PROGRAM STOP; the LOAD/STORE ADDRESS COMPARE switch is in LOAD or STORE; and the contents of SAR match the address in ADDRESS/DATA switches A-E. (See 1-060.)
b. The panel is active; the MODE SELECT switch is in INSTRUCTION STEP; and the CCU reaches an instruction boundary.
c. The 'hard stop' latch sets.
d. The control panel is active, and you press the STOP pushbutton.
e. The control panel is active, the DIAGNOSTIC CONTROL switch is in one of the STORAGE TEST positions, and you press the START pushbutton.

- Turned off when the 'program stop' latch resets.

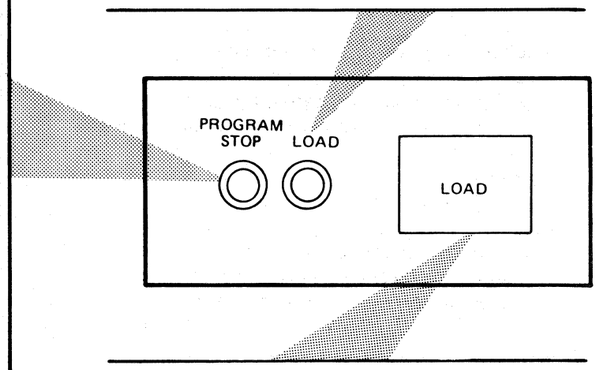
The 'program stop' latch is reset when one of the following happens.

a. A power-on reset occurs.
b. IPL Phase 1 reset occurs.
c. The control panel is active, DIAGNOSTIC CONTROL switch is not in any of the four STORAGE TEST positions, none of the conditions that set the 'program stop' latch are present, and you press the START pushbutton. If the DIAGNOSTIC CONTROL switch is in CLOCK STEP, and you press the START pushbutton, the latch is reset during the start cycle.

WARNING
When the 'program stop' latch is set, cycle steal operations can cause adapter problems.

Load Light

- Turned on when IPL starts.
- Turned off by either:
  a. Executing Output X'79' with bit 1.1 on the register designated by the R field of the instruction.
  b. Executing Output X'79' from the control panel by displaying register X'79' and then storing a '1' in bit position 1.1. (See page 1-140.)



Load Pushbutton

- Causes a machine reset and starts an IPL if the 'panel active' latch is set. (The PANEL ACTIVE light should be on.) See pages 6-960 to 6-964 for information on IPL.

Power On Pushbutton

- Starts a power-on sequence if the LOCAL/REMOTE POWER switch is in LOCAL (Not affected by the Unit Protection Feature).

The POWER CHECK light comes on when you press the POWER ON pushbutton and goes off when the power-on sequence is complete. The light stays on if a failure prevents completion of the power-on sequence.

An IPL starts at the end of a power-on sequence. The MODE SELECT and DIAGNOSTIC CONTROL switches must be in PROCESS so that the channel interface can be enabled during IPL.

Remote/Local Power Switch

- Determines whether the host processor or the 3705-80 controls dc power. (Not affected by the Unit Protection Feature.)

Local

- Dc power can be turned on and off only at the 3705-80 control panel. An emergency power off at any attached host processor turns off 3705-80 power.

Remote

- The host processor controls 3705-80 dc power.

Dc power comes on at the 3705-80 when power is turned on at any attached host processor. Dc power goes off at the 3705-80 when power is off at every attached host processor, when an emergency power off occurs at any attached host processor, or when you press the POWER OFF pushbutton.

Power Off Pushbutton

- Starts a power-off sequence. Resets any power check (except those caused by overheating) and turns off the POWER CHECK light (Not affected by the Unit Protection Feature).

This pushbutton shuts down power with the REMOTE/LOCAL POWER switch in either position.

Note: *Turn the CHANNEL INTERFACE ENABLE/DISABLE switch(es) to DISBL and wait for the INTERFACE ENABLED lights to go off before you press the POWER OFF pushbutton. This prevents interference with the attached CPU.*

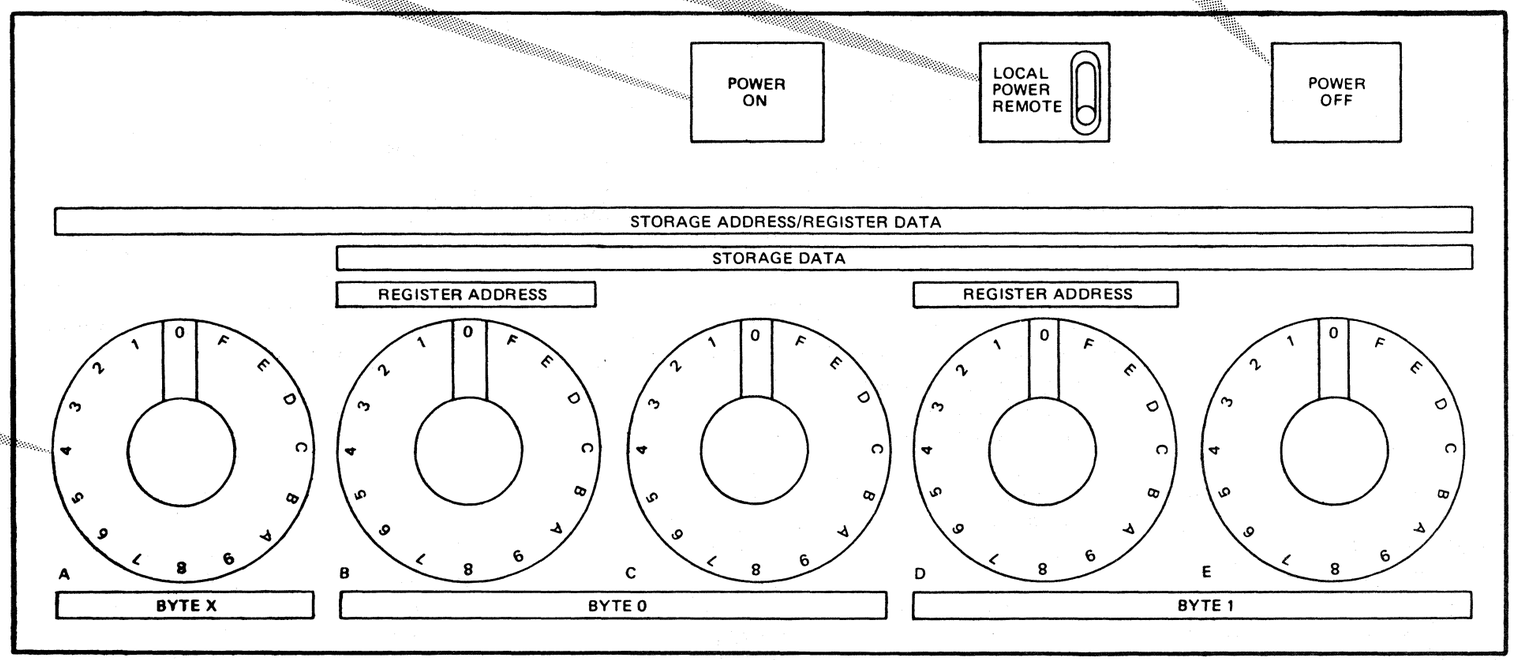
Storage Address/Register Data (Address/Data) Switches

- Sets addresses or enters data to test the 3705-80.

For storage addressing, you should use only positions 0-3 on switch A. For data entry, turning the switch to positions 4-F will also cause data to be entered 4=0, 5=1, 6=2, 7=3, 8=9, 9=1, A=2, B=3, C=4, D=5, E=6, F=7.

When input X'71' is executed, the data in the switches is placed in the general register designated by the R field in the instruction.

Note: *If input X'71' is executed while you are turning the ADDRESS/DATA switches, the data loaded into the general register is unpredictable.*



Diagnostic Control Switch

- Used to perform diagnostic tests on the 3705-80.

If the PANEL ACTIVE light is off, the 3705-80 runs as if the switch were in PROCESS. The TEST light comes on if the switch is in any position other than PROCESS.

WARNING

Before starting a clock step, storage scan, single address scan, storage test pattern, or single address test pattern procedure, perform a program shutdown procedure and disable the channel adapter. If you do not take this precaution, the channel adapter will be suddenly forced to the disabled state, and a system error may occur.

Note: *Certain storage failures are not detected by performing storage scan, single address scan, single address test pattern, and storage test pattern procedures. Storage IFTs must be run to indicate these failures.*

Process

- Allows the 3705-80 to run normally.

Bypass CC Check Stop

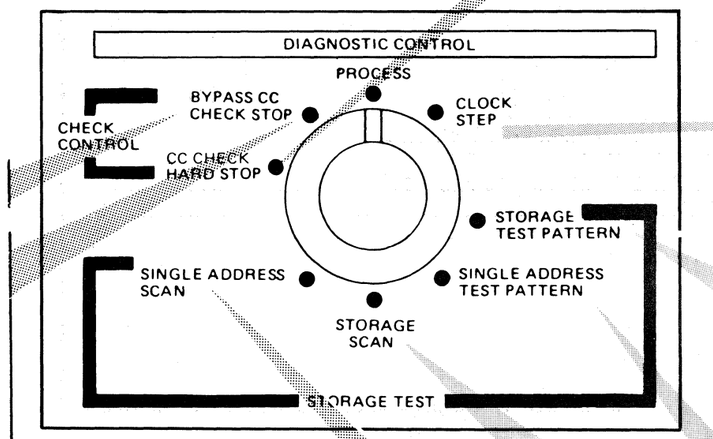
- Allows normal operation except the 'hard stop' latch does not set, and the CCU does not start an IPL sequence when a CC check occurs. Normal operation can be affected if the check alters the program in any way. See chart below.

The 'hard stop' latch does not set, but the appropriate CC check latch sets, and the CC CHECK light comes on.

CC Check Hard Stop

- Allows normal operation except that a CC check causes the 3705-80 to hard stop at the end of that cycle and prevents the latch 'mach ck set IPL'. (See Output X'79' page 6-930.) See chart below.

The 'hard stop' latch sets, the appropriate CCU check latch sets, and the CC CHECK light comes on; but the CCU does not start an IPL sequence.



CCU Action When a Check Condition Occurs

Diagnostic Control Switch Position	Hardstop		Process		Bypass Check Stop	
Error Occurred in Program Level	1	2, 3, 4, 5	1	2, 3, 4, 5	1	2, 3, 4, 5
Hardware Check						
ALU**, INDATA, SAR, SDR, OP REG, CLOCK	hardstops	hardstops	Note[1]	Note[1]	bypasses	bypasses
Program Check						
ADAPTER	hardstops	bids level 1	Note[1]	bids level 1	bypasses	bids level 1
IN/OUT					bypasses	
PROTECT					Note[2]	
INVALID OP					bypasses	

Notes:

1. *A check sets the 'mach ck set IPL' latch and causes the 3705-80 to re-IPL. If another program check occurs before the 3705-80 exits level 1, the 3705-80 will hardstop.*
2. *This type error is not bypassed and program execution does not continue. However, the hardstop latch is not set and the hardstop light is not lit.*

***The check condition is an ALU Check if the byte 0, byte 1, and/or byte X lights are on and the INDATA, SAR, SDR, OP REG, and CLOCK lights are off.*

Clock Step

Note: *During clock step operations, the REFRESH OVERRUN indicator turns on and remains on. This is a false or invalid indication, because the overrun detection logic cannot function normally during clock step operations. You must reset or IPL the 3705-80 after clock step operations to validate the indicator.*

(See also page 1-160)

- Causes the CCU clock to be controlled by the START pushbutton instead of the 3705-80 oscillator. (Refer to *Clock Step Procedure* on page 1-140.)

The 3705-80 stays in process mode until the START pushbutton is pressed and an instruction boundary is reached. Pressing it the first time stops the 3705-80 in T0 of A time.

Each time you press and release the START pushbutton, the CCU clock advances one T time. (This can be observed in the CLOCK TIME lights in display A. See chart A.) Press and release the START pushbutton repeatedly to step the CCU clock through one "dummy" cycle (15 times). Then step the CCU clock through one CS Start cycle (16 times) to set up the following I cycle (observe the CS CYCLE light). Step the CCU clock through the instruction cycle(s). A CS Start cycle occurs before each of the following instruction's I cycle.

In CLOCK STEP the 3705-80 operates normally except:

1. Instead of the machine oscillator, the START pushbutton steps the CCU clock.
2. The Z bus is gated to display register 1 at each AT3 time during maintenance cycles.
3. The Z bus is gated to display register 2 at every T3 time during maintenance cycles.
4. Storage does a complete read call beginning at AT0 time and then, if it is a store-type instruction, does a complete write call at CT0 time.

Storage Test Pattern

- Causes the continuous storing of test data from the ADDRESS/DATA switches in sequential storage locations. (See *Storing a Test Pattern in Storage* page 1-130.) After storing the pattern at a location, the CCU reads that location to check for good parity. The pattern is then stored at the next address. The operation stops when the switch is turned to another position or when the CCU detects an error.

The 3705-80 stays in the process state until the START pushbutton is pressed and released. This sets the 'program stop' latch and starts the operation.

Single Address Test Pattern

- When the DIAGNOSTIC CONTROL switch is in this position, pressing and releasing the START pushbutton causes a continuous store and read operation for the storage location addressed by TAR. (See *Single Address Test Pattern Procedure* page 1-130.)

The 3705-80 stays in the process state until the START pushbutton is pressed and released. This sets the 'program stop' latch and starts the operation. The operation stops when the switch is turned to another position. The operation continues regardless of error indications.

Storage Scan

- When the Diagnostic Control switch is set in this position, pressing and releasing the START pushbutton causes a storage scan operation.

The 3705-80 stays in the process state until the START pushbutton is pressed and released. This sets the 'program stop' latch and starts the operation. The operation stops when the switch is turned to another position or when the CCU detects an error.

Single Address Scan

- When the DIAGNOSTIC CONTROL switch is in this position, pressing and releasing the START pushbutton causes a continuous scan of the storage location addressed by ADDRESS/DATA switches. (See *Single Address Scan* page 1-130.)

The 3705-80 stays in the process state until the START pushbutton is pressed and released. This sets the 'program stop' latch and starts the operation. This operation continues regardless of error indications.

Chart A

Cycle Time	A				B			
Clock Time	T0	T1	T2	T3	T0	T1	T2	T3
Bit 1.4 light	0				0			
Bit 1.5 light	0				1			
Bit 1.6 light	0	0	1	1	0	0	1	1
Bit 1.7 light	0	1	0	1	0	1	0	1

Cycle Time	C				D			
Clock Time	T0	T1	T2	T3	T0	T1	T2	T3
Bit 1.4 light	1				1			
Bit 1.5 light	0				1			
Bit 1.6 light	0	0	1	1	0	0	1	1
Bit 1.7 light	0	1	0	1	0	1	0	1

Lights indicate the clock time that was just completed.

CONTROL PANEL PROCEDURES

Power-On Procedure
1. Set the LOCAL/REMOTE POWER switch to LOCAL.
2. Press the POWER ON pushbutton. The POWER CHECK light should turn on.
3. The POWER CHECK light turns off when the power on sequence ends. See D-500 and Power MAPs in Volume I for power sequence problems.

Note: *The power-on procedure causes an IPL.*

Power-Off Procedure
1. Set the CHANNEL INTERFACE ENABLE/DISABLE switch to DISBL.
2. Wait until the CHANNEL INTERFACE ENABLED light(s) turns off.
3. Press the POWER OFF pushbutton.

Activating the Control Panel
1. Set the MODE SELECT and the DIAGNOSTIC CONTROL switches to PROCESS.
2. The 'panel active' latch is set and the PANEL ACTIVE light turns on.

Enabling a Channel Interface
1. Set the CHANNEL INTERFACE ENABLE/DISABLE switch to ENBL A or ENBL B.
2. When the interface is enabled, the CHANNEL INTERFACE ENABLED light for that interface turns on.

Note: *You may need to stop the host processor momentarily, to satisfy certain enable conditions if the host processor is very busy. Interface enable must also be conditioned by the 3705-80 program.*

Disabling a Channel Interface
1. Set the CHANNEL INTERFACE ENABLE/DISABLE switch to DISBL.
2. When the channel interface is disabled and the 'clock out' line from the host processor is inactive, the CHANNEL INTERFACE ENABLED light for that interface turns off.

Note: *You may need to stop the host processor momentarily to satisfy certain disable conditions if the host processor is very busy.*

IPL Procedure
1. Activate the panel.
2. Press the LOAD pushbutton.
3. The LOAD light turns on when IPL starts.

Resetting the 3705-80

WARNING
Disable the channel interface(s) before pressing the RESET pushbutton.

1. Press the RESET pushbutton.
2. This resets all the 3705-80 hardware. (See *RESET Pushbutton* page 1-070.)
3. Press the LOAD pushbutton to start an IPL sequence.

Resetting a CC Check
1. Press the CC CHECK RESET pushbutton.
2. If no more checks are detected, the CC CHECK light turns off.

Requesting a Program Level 3 Interrupt
1. Set the DISPLAY/FUNCTION SELECT switch and the ADDRESS/DATA switches according to the convention established by the program handling the request.
2. Press and release the INTERRUPT pushbutton.

Displaying 3705-80 Status
1. Set the DISPLAY/FUNCTION SELECT switch to STATUS.
2. The lights in display A and display B show check and status information as indicated by their labeling.

Displaying TAR and the OP Register
1. Set the DISPLAY/FUNCTION SELECT switch to TAR & OP REGISTER.
2. Display A shows the address in TAR. Display B bytes 0 and 1 show the contents of the Op register. Byte X of display B contains all 0s.

Note: *After a register address, storage address or storage test function, the TAR & OP REGISTER position of the DISPLAY/FUNCTION SELECT switch will no longer display the last previous TAR and OP code.*

Set Address and Display Register Procedure

(See page 6-052 for flowchart.)

WARNING

You can display most addressable registers using this procedure with the program running without affecting normal program operation. However, when you address certain registers, control functions occur and affect program operation. Refer to page 8-060 (type 1 CA) and H-040 (type 4 CA) for information on these registers.

1. Set ADDRESS/DATA switches B and D to the address of an input register. (See 6-151 for the register addresses.)
2. Set the DISPLAY/FUNCTION SELECT switch to REGISTER ADDRESS.
3. Press and release the SET ADDRESS/DISPLAY pushbutton.
   - A display register CS1 maintenance cycle is taken on the next instruction boundary.
   - Display A bits 0.0 - 0.3 and bits 1.0 - 1.3 display the contents of ADDRESS/DATA switches B and D. All other bits in display A are 0.
   - The input register address in the ADDRESS/DATA switches is also put in the Op register.
   - Display B shows the register contents. If the register address is unassigned, all zero's, or a CA register address that cannot be displayed, display B shows all 0s. See 8-060 (type 1 CA) and H-040 (type 4 CA) for a description of undisplayable CA registers. The In/Out Check L1 interrupt request is not set.
   - If the PROGRAM STOP light is on, the register address is also placed in TAR. It can then be used as the register address in a subsequent store register operation.

Note: *If the PROGRAM DISPLAY light is on, this operation will not work with the program running.*

Storing Data in a Register

(See page 6-054 for flowchart.)

WARNING

Be careful when using the STORE pushbutton. The data stored may affect normal program and cycle steal operation and destroy program data.

1. If the PROGRAM STOP light is not on, press the STOP pushbutton.
2. Perform a set address and display register operation to set in the Op register the address of the output register in which you desire to store data. Leave the DISPLAY/FUNCTION SELECT switch at REGISTER ADDRESS.
3. Set the data in ADDRESS/DATA switches A-E.
4. Press and release the STORE pushbutton.
   - The PROGRAM DISPLAY light turns off, if it was on.
   - Display A shows the contents of TAR. (TAR and the Op register contain the address entered in the set address and display register operation.)
   - The data in ADDRESS/DATA switches A-E is stored in the output register addressed by the Op register, and is displayed in display B.
   - If the register address in the Op register is unassigned, the store operation has no effect. The In/Out Check L1 interrupt request is not set.

Set Address and Display Storage Procedure

(See page 6-056 for flowchart.)

Note: *Displaying storage locations using this procedure does not affect normal program or cycle steal operation.*

1. Set ADDRESS/DATA switches A-E to the storage address.
2. Set the DISPLAY/FUNCTION SELECT switch to STORAGE ADDRESS.
3. Press and release the SET ADDRESS/DISPLAY pushbutton.
   - A display storage CS1 maintenance cycle is taken on the next instruction boundary.
   - The contents of ADDRESS/DATA switches A-E are placed in SAR and in display A.
   - Display B bytes 0 and 1 shows the contents of the addressed storage halfword location. Because control panel storage-address and storage-scan functions operate only on halfwords, display B byte X should be ignored.
   - If the PROGRAM STOP light is on, the storage address is also placed in TAR. It can then be used as the initial address in a store storage operation.

Note: *If the PROGRAM DISPLAY light is on, this operation will not work with the program running.*

Storing Data in Storage Locations

(See page 6-057 for flowchart.)

Note: *Certain storage failures are not detected by this procedure. Storage IFTs must be executed to indicate these failures.*

1. If the PROGRAM STOP light is not on, press the STOP pushbutton.
2. Perform a set address and display storage operation to set the storage address in TAR. (See page 1-120.) Leave the DISPLAY/FUNCTION SELECT switch at STORAGE ADDRESS.
3. Set the data in ADDRESS/DATA switches B-E.
4. Press and release the STORE pushbutton.
   - The PROGRAM DISPLAY light turns off, if it was on.
   - The contents of ADDRESS/DATA switches B-E are stored at the location addressed by TAR.
   - TAR is incremented to address the next halfword storage location. Display A shows this new address.
   - Display B bytes 0 and 1 displays the data from the addressed storage location. Because control panel storage-address and storage-scan functions operate only on halfwords, display B byte X should be completely ignored.
5. Press the STORE pushbutton each time you want to store data from ADDRESS/DATA switches B-E in the next sequential storage location.

Storing a Test Pattern in Storage

(See page 6-060 for flowchart.)

WARNING
Disable the channel interfaces before you start this procedure.

If a test pattern that is an invalid Op is stored, pressing the START pushbutton will cause an invalid Op CC check.

Note: *Certain storage failures are not detected by this procedure. Storage IFTs must be executed to indicate these failures.*

1. Set the test pattern data in ADDRESS/DATA switches B-E.
2. Set the DIAGNOSTIC CONTROL switch to STORAGE TEST PATTERN.
3. Set the DISPLAY/FUNCTION SELECT switch to any position except TAR and OP Register or STATUS.
4. Press the START pushbutton.
   - The PROGRAM STOP light turns on.
   - The data in ADDRESS/DATA switches B-E is stored in the storage location addressed by TAR.
   - Display A displays the address in TAR. TAR is then incremented to address the next storage halfword location.
   - Display B bytes 0 and 1 displays the data from the storage location. Because control panel storage-address and storage-scan functions operate only on halfwords, display B byte X should be completely ignored.
   - The stored data is checked for parity. A parity check causes the appropriate CC CHECK light to turn on. The 3705-80 stops. To continue the operation: (1) press the CC CHECK RESET pushbutton, and (2) press the START pushbutton. The operation continues until the CCU detects an error.
5. To end the operation, set the DIAGNOSTIC CONTROL switch to another position.

Note: *Because an asynchronous stop occurs when the switch is turned, an indata check may occur. Ignore the check, and press the CC CHECK RESET pushbutton.*

Storage Scan

(See page 6-063 for flowchart.)

WARNING
Disable the channel interfaces before you start this procedure.

Note: *Certain storage failures are not detected by this procedure. Storage IFTs must be executed to indicate these failures.*

1. Set the DIAGNOSTIC CONTROL switch to STORAGE SCAN.
2. Press the START pushbutton.
   - The PROGRAM STOP light turns on.
   - The storage location addressed by TAR is scanned first.
   - Each CS1 cycle increments the address in TAR by two and puts the new address in display A (unless the DISPLAY/FUNCTION SELECT switch is in STATUS.)
   - Display B bytes 0 and 1 shows the last thing set in the Op register if the DISPLAY/FUNCTION SELECT switch is in TAR & OP REGISTER. (The Op register is not changed during this operation.) If the switch is not in the TAR and OP Register or STATUS position, display B shows the contents of the storage location addressed by SAR. Because control panel storage-address and storage-scan functions operate only on halfwords, display B byte X should be completely ignored.
   - A parity check causes the appropriate check light to turn on. The 3705 stops. The address in display A is two greater than the address that caused the parity check. To continue the operation: (1) press the CC CHECK RESET pushbutton, and (2) press the START pushbutton. The operation continues until the CCU detects an error.
3. To end the operation, set the DIAGNOSTIC CONTROL switch to another position.

Note: *Because an asynchronous stop occurs when the switch is turned, an indata check may occur. Ignore the check and press the CC CHECK RESET pushbutton.*

Single Address Test Pattern Procedure

(See page 6-064 for flowchart.)

WARNING

Disable the channel interfaces before you start this procedure.

Note: *Certain storage failures are not detected by this procedure. Storage IFTs must be run to indicate these failures.*

1. Set the address of the storage location in TAR, using the procedure in *Set Address and Display Storage Procedure* or in *Single Address Scan.*
2. Set the test pattern in ADDRESS/DATA switches B-E.
3. Set the DIAGNOSTIC CONTROL switch to SINGLE ADDRESS TEST PATTERN.
4. Set the DISPLAY/FUNCTION SELECT switch to any position except TAR and OP Register or STATUS.
5. Press the START pushbutton.
   - The PROGRAM STOP light turns on.
   - The data in ADDRESS/DATA switches B-E is stored in the storage location addressed by TAR.
   - Display A shows the address in TAR. TAR is not incremented.
   - Display B bytes 0 and 1 shows the data stored in the storage location. The data is checked for parity. Because control panel storage-address and storage-scan functions operate only on halfwords, display B byte X should be ignored.
   - A parity check does not cause the machine to stop, but the appropriate CC CHECK light does turn on.
6. To end the operation, set the DIAGNOSTIC CONTROL switch to another position.

Note: *Because an asynchronous stop occurs when the switch is turned, an indata check may occur. Ignore the check and press the CC CHECK RESET pushbutton.*

Single Address Scan

(See page 6-067 for flowchart.)

1. Set ADDRESS/DATA switches A-E to the address of the storage location that you want to scan.
2. Set the DIAGNOSTIC CONTROL switch to SINGLE ADDRESS SCAN.
3. Set the DISPLAY/FUNCTION SELECT switch to any position except TAR and OP Register or STATUS.
4. Press the START pushbutton.
   - During each CS1 cycle, display A displays the address in the ADDRESS/DATA switches.
   - Display B bytes 0 and 1 shows the data in the addressed location. Because control panel storage-address and storage-scan functions operate only on halfwords, display B byte X should be ignored.
   - The storage address is not incremented.
   - The scanning does not stop if a parity check occurs, but the appropriate CC CHECK light does turn on.
5. The ADDRESS/DATA switches can be rotated to continuously display the contents of the storage locations.
6. To end the operation, set the DIAGNOSTIC CONTROL switch to another position.

Note: *Because an asynchronous stop occurs when the switch is turned, an indata check may occur. Ignore the check and press the CC CHECK RESET pushbutton.*

Store Address Compare

1. Set the LOAD/STORE ADDRESS COMPARE switch to STORE.
2. Set ADDRESS/DATA switches A-E to the storage address.

Note: *To determine if a 'store character' (STC) or 'store character and count' (STCT) instruction stores data from a general register in a storage byte, set the ADDRESS/DATA switches to the address of that byte.*

To determine if a 'store' (ST) or 'store halfword' (STH) stores byte 0 and byte 1 of a general register in a storage halfword, set the ADDRESS/DATA switches to the address of either byte.

   - During I2 and I3 cycles, the storage address in the ADDRESS/DATA switches is compared with the contents of SAR. If the addresses are equal, and the instruction being executed is a ST, STC, STH, or STCT instruction, the ADDRESS COMPARE light in display B turns on, if the DISPLAY/FUNCTION SELECT switch is in STATUS. Bit 1.7 is included in the address comparison only if the instruction is a *byte* instruction.
3. To cause a program stop to occur when the address compare occurs, set the MODE SELECT switch to ADDRESS COMPARE PROGRAM STOP. Pressing and releasing the START pushbutton resets the 'program stop' latch and restarts the program.
4. To cause the address compare L1 interrupt request to set when the address compare occurs, set the MODE SELECT switch to ADDRESS COMPARE INTERRUPT.

Load Address Compare

1. Set the LOAD/STORE ADDRESS COMPARE switch to LOAD.
2. Set ADDRESS/DATA switches A-E to the storage address.

Note: *To determine if an instruction at a specific address is ever executed, the address set in the ADDRESS/DATA switches can be either the address of byte 0 or byte 1 of the instruction.*

To determine if a storage byte is ever loaded into a general register, set the ADDRESS/DATA switches to the address of that byte.

To determine if a storage halfword is ever loaded into byte 0 and 1 of a general register, set the ADDRESS/DATA switches to the address of either byte 0 or byte 1 of the storage location.

   - During I1, I2, and I3 cycles, the storage address in the ADDRESS/DATA switches is compared with the contents of SAR. If the addresses are equal, and the instruction is any instruction other than ST, STC, STH, or STCT, the ADDRESS COMPARE light in display B turns on if the DISPLAY/FUNCTION SELECT switch is in STATUS. Bit 1.7 is included in the address comparison only if the instruction is a *byte* instruction.
   - If the MODE SELECT switch is at ADDRESS COMPARE PROGRAM STOP when the addresses are equal, pressing and releasing the START pushbutton resets the 'program stop' latch and restarts the program.
3. To cause a program stop to occur when the address compare occurs, set the MODE SELECT switch to ADDRESS COMPARE PROGRAM STOP.
4. To cause the address compare L1 interrupt request to set when the address compare occurs, set the MODE SELECT switch to ADDRESS COMPARE INTERRUPT.

Lamp Test

Note: *Pressing the LAMP TEST pushbutton does not affect normal 3705-80 operation.*

1. Press the LAMP TEST pushbutton.
2. All the control panel lights, except the POWER CHECK light and the spares, turn on.

Clock Step Procedure

WARNING
Disable the channel interface before you start this procedure.

Note: *During clock step operations, the REFRESH OVERRUN indicator turns on and remains on. This is a false or invalid indication, because the overrun detection logic cannot function normally during clock step operation. You must reset or IPL the 3705-80 after clock step operations to validate the indicator.*

1. Set the DIAGNOSTIC CONTROL switch to CLOCK STEP.
2. Press the START pushbutton.
   - The 3705-80 stops in T0 of A time.
   - The START pushbutton, instead of the 3705-80 oscillator, provides pulses to drive the CCU clock.
   - If the DISPLAY/FUNCTION SELECT switch is in STATUS, displays A and B show check and status information. If the switch is in TAR & OP REGISTER, display A shows the contents of TAR and display B shows the contents of the Op register. If the switch is in any other position, the contents of the Z bus are gated to display register 1 at each AT3 time and to display register 2 at every T2 time during maintenance cycles.

Rules for observing clock-step operations.

- The first instruction executed in clock-step mode is preceded by an idle cycle (CS indicator off, I indicator off).
- A CS1 start-pushbutton cycle (CS indicator on, I indicator off) is taken before the start of each instruction.
- The I cycle being executed can be determined by observing the Display A status indicators 1.3–1.7. By counting the number of transitions thru IA T0 since the last cycle steal cycle, the I-cycle number is known (be sure to watch the I indictor — ignore the interspersed idle cycles).
- Additional idle cycles may be interspersed depending on the instruction.

In CLOCK STEP the 3705-80 operates normally except:

1. Instead of the machine oscillator, the START pushbutton steps the CCU clock.
2. The Z bus is gated to display register 1 at each AT3 time during maintenance cycles.
3. The Z bus is gated to display register 2 at every T3 time during maintenance cycles.
4. Storage does a complete read call beginning at AT0 time and then, if it is a store-type instruction, does a complete write call at CT0 time.

Instruction Step Procedure

1. Set the MODE SELECT switch to INSTRUCTION STEP.
   - The PROGRAM STOP light turns on.
2. Press and release the START pushbutton to continue with the next instruction.
   - The 3705-80 executes one instruction.
3. Each time you press and release the START pushbutton, the 3705 executes one instruction.

Note: *The CCU handles cycle steal requests normally during this procedure. All interrupts, except program level 1 interrupts and interrupts to higher program levels, are inhibited until the program executes an 'exit' instruction.*

Executing an Input or Output Instruction From the Control Panel

Input instructions can be executed from the control panel by displaying the corresponding external register. See *Set Address and Display Register Procedure* on page 1-120.

Output instructions can be executed from the control panel by displaying the corresponding external register and then storing the desired bits in the register. (The 3705-80 must be in program stop mode.) See *Storing Data in a Register* on page 1-120.

Example: The CC CHECK lights in displays A and B can be turned off by executing an Output X'77' instruction with bit 0.1 on the general register designated by the R field of the instruction. The lights can also be turned off by storing a "1" in bit 0.1 of external register X'77'.

The bits stored in an external register from the control panel have the same hardware function as when they are set on by a program. Therefore, many hardware functions can be checked by simulating input and output instructions from the control panel.

Setting Up and Executing an Instruction

WARNING
Disable the channel interface(s) before starting this procedure.

Note: *This procedure is an example of one method to set up and execute an instruction.*

1. Press the STOP pushbutton.
2. Use the *Set Address and Display Storage Procedure* (page 1-120) to set the storage address that you want to store the instruction in.
3. Use the steps in *Storing Data in a Storage Location* (page 1-130) to store the desired instruction in the storage location.
4. In the next storage location, store a 'branch' instruction to cause a branch back to the preceding storage location.
5. Use the *Set Address and Display Register Procedure* (page 1-120) to set the IAR (register 0) for the program level that you are in. (The current program level can be determined from the status lights in display B.)
6. Follow the steps in *Storing Data in a Register* (page 1-120) to store the address of the storage location from step 3.
7. If you want to step through the instructions:
   a. Turn the MODE SELECT switch to INSTRUCTION STEP.
   b. Press and release the START pushbutton. The CCU executes one instruction. The 3705-80 stops, and the PROGRAM STOP light turns on.
   c. Press and release the START pushbutton to execute the next instruction. Each time you press the START pushbutton, the CCU executes one instruction.

Note: *If the CCU is in level 1 (as it is immediately after ROS is loaded), program execution in levels 2, 3, 4, or 5 requires the following previous steps: (1) reset level 1 requests — Output X'77', (2) unmask appropriate interrupt level — Output X'7F', (3) generate an appropriate interrupt request, and (4) EXIT.*

CONTROL PANEL TEST OF CCU DATA PATH

Part 1. Basic Control and Data Flow

This section tests the part of the data path in the CCU necessary to load ROS and those controls that may be necessary to analyze a failure detected by the ROS test.

Lamp Test

1. Press LAMP TEST. —All panel lights, except POWER CHECK and the spares, should light.
2. Swap any failing lights with lights in working positions to verify that the lights are bad.
3. Replace the lights found to be defective.
4. If the lights tested are good, swap the driver cards located at 01A-B4U2 and 01A-B4U3. Refer to D-210 and ALDs AP009 to AP015 for details.

Panel Active (Required for Further Panel Testing)

The following conditions should activate the PANEL ACTIVE light:

a. DIAGNOSTIC CONTROL switch in PROCESS
b. Not power-on reset
c. MODE SELECT switch in PROCESS

Refer to ALD CU001-BM6.

WARNING

Disable the channel interface(s) before proceeding.

Clock Step

Note: *During clock step operations, the REFRESH OVERRUN indicator turns on and remains on. This is a false or invalid indication, because the overrun detection logic cannot function normally during clock step operation. You must reset or IPL the 3705-80 after clock step operations to validate the indicator.*

1. Set the DIAGNOSTIC CONTROL switch to CLOCK STEP.
2. Press RESET. —Verify that the HARDSTOP, PROGRAM STOP, TEST, and WAIT lights are on.
3. Set the DISPLAY/FUNCTION SELECT switch to STATUS.
4. Press START. —Check CYCLE TIME and CLOCK TIME in display A. CYCLE TIME should equal '00'; CLOCK TIME should equal '00'.
5. Press START repeatedly and observe the stepping of CLOCK TIME and CYCLE TIME. CYCLE TIME should increment each time CLOCK TIME steps from '11' to '00'.

Initial Data Path Test (ALU-B Side, Z bus, Display A)

1. Set the DISPLAY/FUNCTION SELECT switch to STORAGE ADDRESS.
2. Set the DIAGNOSTIC CONTROL switch to SINGLE ADDRESS SCAN.
3. Press START.
4. The address set in ADDRESS/DATA switches should be equal to Display A. Vary the ADDRESS/DATA switches to test various data bit combinations (for example, 0101, 5555, AAAA, etc.)
5. Compare display A with the switch values to check for data bit failures.
6. If data bit failures occur, refer to *CCU DATA BITS/CARD LOCATIONS* (page 1-160) for card swapping.

Note: *This procedure can also be used as convenient way to display multiple storage locations. Data is displayed in display B.*

7. Return the DIAGNOSTIC CONTROL switch to PROCESS.

Storage Data Path Test (ALU-A Side, Display B)

1. Press STOP.
2. Display storage at any valid address using the set address and display storage procedure (page 1-120).
3. Press STORE. —The data in the ADDRESS/DATA switches is stored at the address displayed in step 2.
4. Press STORE again. —Display A should increment by 2 each time STORE is pressed. Display B should be the contents of the address indicated in display A.

Note: *The data being stored is not displayed because TAR is incremented; the next storage location is displayed.*

5. Verify that the correct data was stored by using the display storage procedure.
6. Set the DIAGNOSTIC CONTROL switch to SINGLE ADDRESS TEST PATTERN.
7. Press START. —The contents of display B should equal the value in the ADDRESS/DATA switches. Vary data pattern in the switches as desired.

Storage Test Pattern

1. Set the DIAGNOSTIC CONTROL switch to STORAGE TEST PATTERN.
2. Set the ADDRESS/DATA switches to 'FFFF'.
3. Set the DISPLAY/FUNCTION SELECT switch to STORAGE ADDRESS.
4. Press START.
5. Display A shows the incrementing address; display B shows the data.
6. If the machine stops because of a CC check, record the following:
   a. Falling storage address (equals the address in display A minus 2)
   b. Failing bits (Compare the ADDRESS/DATA switches and display B.)
   c. Set the DISPLAY/FUNCTION SELECT switch to STATUS. —Display A shows the error status.

Note: *If a CC check has occurred, but the ADDRESS/DATA switches and display B are equal, the parity bit has probably failed. (The BYTE lights indicated the byte with the bad parity bit.)*

7. Press CHECK RESET, then press START.
8. Repeat steps 1 through 6 using different data patterns in the ADDRESS/DATA switches (for example, 0000, 0101, 5555, AAAA, etc.)
9. Analyze failures to determine a failing pattern (data or addressing).

ROS Test Control

Verifies that IPL phase 1 and 2 execute correctly.

1. With the channel interface disabled, press LOAD on the local 3705-80. On the Remote 3705-80, press LOAD.
2. The IPL phase lights should equal '11' with the program looping, waiting for the 'interface enabled' signal. Do not enable the interface unless channel data transfer is desired. If trouble is suspected, refer to the ROS listing and to the ROS test section of this manual.
   a. If the IPL PHASE lights are '01', check the hardware reset function.
   b. If the IPL PHASE lights are '10', ROS test transfer to storage is incomplete.
      (1) Press RESET to force IPL phase 3 ('11').
      (2) Run the storage pattern test with data equal to 'FFFF' to establish a background pattern.
      (3) Press LOAD.
      (4) If the same failure occurs: Turn the DISPLAY/FUNCTION SELECT switch to TAR & OP REGISTER. Display A shows the next storage address. Press RESET and display storage starting at X'0000' to determine how much of ROS was loaded (data instead of FFFF).
3. Refer to *ROS TEST,* page 2-000 if a failure occurs in IPL phase '11'. (Local 3705-80.)
4. Refer to RPL section in Vol 1 (SY27-0208) of this set for ROS Testing for a Remote 3705-80.

Address Compare Stop, Instruction Step, and Hard Stop

1. Set the DISPLAY/FUNCTION SELECT switch to TAR and OP REGISTER.
2. Set the LOAD/STORE ADDRESS COMPARE switch to LOAD.
3. Set the MODE SELECT switch to ADDRESS COMPARE PROGRAM STOP.
4. Set the ADDRESS/DATA switches to '00012'.
5. Press LOAD. (The address compare pulse is available at 01A-B3P2-S09. See ALD page CU004.)
6. The 3705-80 should stop with:
   a. PROGRAM STOP light on.
   b. TEST light on.
   c. LOAD light on.
   d. DISPLAY A set to X'00014' (The instruction at address X'0012' was executed).
   e. ADDRESS COMPARE and PROG L1 lights are on, if the DISPLAY/FUNCTION SELECT switch is set to STATUS.
7. Set the MODE SELECT switch to INSTRUCTION STEP.
8. Press START. Verify that DISPLAY A equals X'00016' (IAR incremented).
9. Display register X'70'.
10. Store register X'70' (Ignore the data.) —The HARD-STOP light should be on.

Part 2. Miscellaneous Controls

This section tests the panel functions that are not required for ROS testing and analysis but are used for DCM Diagnostic Control Module control and indications. Note the input and output instructions can be executed from the control panel by displaying and storing into the external register. Refer to *Executing an Input or Output Instruction From the Control Panel* on page 1-140.

Load Light

1. Press LOAD. —Verify that the LOAD light is on.
2. Press RESET.
3. Display register X'79'.
4. Store X'0040' in register X'79'. —Verify that the LOAD light is off.

Set and Reset Test Mode

1. Set the MODE SELECT switch to PROCESS.
2. Set the DIAGNOSTIC CONTROL switch to PROCESS.
3. Display register X'79'.
4. Store X'0010' in register X'79'. —TEST light goes off if it was on.
5. Store X'0020' in register X'79'. —TEST light turns on.

Scope Sync Pulse

1. Display register X'79'.
2. Store X'0002' in register X'79'. —Fires scope sync #1 at 01A-B3M2-P10, ALD page CU015.
3. Store X'0001' in register X'79'. —Fires scope sync #2 at 01A-B3M2-P13, ALD page CU015.

Wait Light

1. Press RESET. —Verify that the WAIT light is on.
2. Set the DIAGNOSTIC CONTROL switch to SINGLE ADDRESS SCAN.
3. Press START. —Verify that the WAIT light is off.
4. Set the DIAGNOSTIC CONTROL switch to PROCESS.

OP Register Data and CC Check

1. Press RESET.
2. Set the MODE SELECT switch to INSTRUCTION STEP.
3. Press LOAD (forces program level 1).
4. Store X'FFFF' in address X'0012' (Branch on Bit using register 7; this will be the first instruction executed).
5. Store X'0000' in address X'0014' (Invalid OP decode).
6. Store X'00000' in register X'07'.
7. Set DISPLAY/FUNCTION SELECT switch to TAR and OP REGISTER.
8. Press START.
   a. DISPLAY B equals X'FFFF' (instruction stored in Step 4).
   b. Repeat steps 4, 6, and 7 varying the data in Step 4 if a hot/cold bit is suspected in the OP REG.
9. Press START again.
10. The lights should indicate:
    a. CC check
    b. Invalid OP
    c. L1 program check
    d. Hardstop
11. Store X'4004' in register X'77'.
    a. CC CHECK lights should be reset.
    b. Invalid OP and L1 program check should be reset.
12. Reset the 3705-80.

Display/Function Select Switch and Program Display

1. Reset the 3705-80.
2. Set the MODE SELECT switch to INSTRUCTION STEP.
3. Press LOAD (forces program level 1).
4. Store the following instructions at the given address:

   Address X'0012' – X'742C' (Puts contents of the DISPLAY/FUNCTION SELECT switch in CCU register 4.)
   Address X'0014' – X'7414' (Output register 4 to display register 1).
   Address X'0016' – X'7424' (Output register 4 to display register 2).
   Address X'0018' – X'A809' (Branch back to first instruction).
5. Set the DISPLAY/FUNCTION SELECT switch to TAR and OP REGISTER.
6. Press START to step through the program.
   a. Verify that the program loops.
   b. The PROGRAM DISPLAY light should turn on and off while the program is stepped.
7. Set the MODE SELECT switch to PROCESS.
8. Press START.
   a. The program should run continuously. (The PROGRAM STOP light should stay off.)
   b. The PROGRAM DISPLAY light should stay on.
9. Rotate the DISPLAY/FUNCTION SELECT switch to the following positions and check the values in both displays A and B bytes 0 and 1.
   a. STORAGE ADDRESS – X'1000'
   b. REGISTER ADDRESS – X'0800'
   c. FUNCTION SELECT 1 – X'0040'
   d. FUNCTION SELECT 2 – X'0020'
   e. FUNCTION SELECT 3 – X'0010'
   f. FUNCTION SELECT 4 – X'0008'
   g. FUNCTION SELECT 5 – X'0004'
   h. FUNCTION SELECT 6 – X'0002'
10. Press STOP to stop the program.

Interrupt Request and Reset

1. Press RESET.
2. Display register X'7F'. –Verify that bit 0.6 is off.
3. Press INTERRUPT.
4. Display register X'7F'. –Verify that bit 0.6 is on (Panel irpt req L3).
5. Store X'2000' in register X'77'. –Reset panel irpt req L3.
6. Display register X'7F'. –Verify that bit 0.6 if off.

Part 3. CCU Data Bits –Card Locations

This section shows cards containing the data bit groups and miscellaneous controls. This information should be useful when running either panel tests or memory IFTs. Logic references are given for further detail.

GENERAL DATA FLOW: Includes B register, LAR, local store, CCU display, ALU, SAR, TAR, A register, and ALU check bits.

Bits	X.P,X.6, X.7	0.P-0.1	0.2-0.4	0.5-0.7	1.P-1.1	1.2-1.4	1.5-1.7
Card	A-B4J2	A-B4K2	A-B4L2	A-B4M2	A-B4N2	A-B4P2	A-B4Q2
ALD Page	DF	DG	DH	DJ	DK	DL001-	DM001-

OP Register and SDR Register

Bits	0.0-0.4	0.5-0.7,0.P	1.0-1.4	1.5-1.7,1.P
Card	A-B4G2	A-B4G2	A-B4H2	A-B4H2
ALD Page	DN001-004	DP001-004	DQ001-004	DR001-004

SAR and SDR Drivers and Receivers (3705-80)

ALD Page	DS001-005
SAR Drivers	A-B4B2
SDR Dr/Rec Byte 0	A-B4A3
SDR Dr/Rec Byte 1	A-B4A2

Miscellaneous Logic References and Card Locations

Functions	*ALD Pages*	*Cards*
ALU Controls	CA001-004	01A-B3J2
Panel Controls	CU001-015	01A-B3N2, B3L2, B3P2
Clock and Controls	CC001-008	01A-B3Q2, B3R2
Data Flow Reg Controls	CS001-007	01A-B3F2, B4E2
Condition Codes	CZ001-005	01A-B3G2
Local Store Controls	CL001-005	01A-B3K2
Instruction Decode	CD001-004	01A-B3H2
Storage Controls	CM001-003	01A-B3T4
Priority Controls	CP001-007	01A-B3M2

DIAGNOSTIC AIDS: SCOPE POINTS AND JUMPERING CAPABILITIES

Scope Points

The following scope points can be used to diagnose problems:

A. '+ diag scope sync point 1' at 01A-B3M2-P10 on ALD page CU015. The DCM controls this sync point by means of an Output X'79' when bit 1.6 is a 1. Scope sync point 1 is used to sync on the beginning of each routine or on the hardware setup block when the DCM is in a scoping loop.

B. '+ diag scope sync point 2' at 01A-B3M2-P13 on ALD page CU015. The DCM controls this sync point by means of an Output X'79' when bit 1.7 is a 1. Scope sync point 2 is used to sync on the test function of a test routine.

Diag scope points 1 and 2 may be used together to count repetitions of the test function. Sync point 1 is used to trigger the scope and the delayed sweep feature is used to count the number of pulses (each pulse represents one repetition) on sync point 2.

See 'Setting Up a Scoping Loop' (below) for information on scoping for a failure while running the IFTs.

C. '+ address compare test pin' at 01A-B3P2-S09 on ALD page CU004. The STORAGE ADDRESS/REGISTER DATA switches on the control panel are used to establish a sync reference on this test pin at any location in any IFT routine or in the DCM. A sync pulse is generated when the address for fetch or store (controlled by the LOAD/STORE ADDRESS COMPARE switch) is the same as the address in the STORAGE ADDRESS/ REGISTER DATA switches.

D. '-A time' at 01A-B3R2-P04 on ALD page CC001.

Setting Up a Scoping Loop (IFT Failures)

After a failure has been detected, the DCM and IFTs provide two looping options.

- The Loop on First Error option selects the smallest possible loop within the IFT. The loop includes the hardware setup, pretest, set scope sync point 2, test, analysis, and error display. The loop for this option normally takes less time to execute than the Restart on First Error option. The loop continues whether or not the error occurs again.
- The Restart Routine on First Error option selects a loop that starts at the beginning of a routine, continues the routine to the point where the error was first detected, and then restarts the routine again. The loop for this option takes longer; however, it may be required for sequence-sensitive failures. The loop continues whether or not the error occurs again.

After selecting the looping option, use the continue function to continue from the error stop. The time required to stop on the error code again gives an indication of the length of the loop. Repeat this process several times and use the longest length of time.

To obtain continuous running loops, the 'bypass error stop' CE sense switch must also be set.

If an error other than the one selected for looping occurs, the DCM stops to display the new error code. To bypass stops for other errors, set the 'bypass new error stop' CE sense switch.

When the scoping loop is running correctly, the scoping indicator (Display B, bit 0.4) blinks at the rate of 3.2 seconds (1.6 seconds on and 1.6 seconds off). Display B (byte 0, bits 5, 6, and 7) is incremented by one for each error detected. This error counter (together with the loop time) indicates the failure is solid or intermittent. Other information is also displayed. Display A shows the adapter, IFT and routine number. Display B (byte 0, bits 0-3 and byte 1) shows the error code being looped on.

Diagnostic Jumpering Capabilities

The following jumpering capabilities can be used to diagnose problems.

Invoke IPL When an Address Compare Occurs

1. Plug the CE MST-1 latch card P/N 5851882 onto a socket position that has no second level wraps on any pin. Probe pins A, F, or M located on latch card according to instructions.

WARNING

The latch card must be plugged onto the board with the component side of the card toward the right or circuit damage will result.

2. Connect 01A-B3P2-S09 to pin A. Refer to ALD page CU004.
3. Connect 01A-B3L2-J09 to pin M. Refer to ALD page CU010.
4. Set the LOAD/STORE ADDRESS COMPARE switch and the ADDRESS/DATA switches as desired.

Invoke IPL When the 'Hard Stop' Latch Sets

1. Same as step 1 of *Invoke IPL When an Address Compare Occurs.*
2. Connect 01A-B3L2-M03 to pin F. Refer to ALD page CU006.
3. Connect 01A-B3L2-J09 to pin M. Refer to ALD page CU010.
4. Press the START pushbutton.

Invoke IPL When the 'Machine Check' Latch Sets

1. Same as step 1 of *Invoke IPL When an Address Compare Occurs.*
2. Connect 01A-B3N2-J06 to pin F. Refer to ALD page CK006.
3. Connect 01A-B3L2-J09 to pin M. Refer to ALD page CU010.
4. Press the START pushbutton.

Cause the 'Clock Step' Latch to Freeze the Clock When an Address Compare Occurs

1. Same as step 1 of *Invoke IPL When an Address Compare Occurs.*
2. Connect 01A-B3P2-S09 to pin A. Refer to ALD page CU004.
3. Connect 01A-B3P2-J09 to pin M. Refer to ALD page CU007.
4. Set the LOAD/STORE ADDRESS COMPARE switch and the ADDRESS/DATA switches as desired.
5. Press the START pushbutton.
6. Set the DIAGNOSTIC CONTROL switch to CLOCK STEP after the address compare stop.

Cause the 'Clock Step' Latch to Freeze the Clock When the 'Hard Stop' Latch Sets

1. Same as step 1 of *Invoke IPL When an Address Compare Occurs.*
2. Connect 01A-B3L2-M03 to pin F. Refer to ALD page CU006.
3. Connect 01A-B3P2-J09 to pin M. Refer to ALD page CU007.
4. Press the START pushbutton.
5. Set the DIAGNOSTIC CONTROL switch to CLOCK STEP after the hard stop.

Prevent Loading of ROS During IPL

Connect 01A-B3L2-U02 to 01A-B3L2-G08. Refer to ALD page CU010.

Cause the 'Clock Step' Latch to Freeze the Clock When the 'Machine Check' Latch Sets

1. Same as step 1 of *Invoke IPL When an Address Compare Occurs.*
2. Connect 01A-B3N2-J06 to pin F. Refer to ALD page CK006.
3. Connect 01A-B3P2-J09 to pin M. Refer to ALD page CU007.
4. Press the START pushbutton.
5. Set the DIAGNOSTIC CONTROL switch to CLOCK STEP after the machine check.

Simulate a Continuous Panel Display Register Operation

1. The 3705-80 must be stopped.
2. Set the DISPLAY/FUNCTION SELECT switch to REGISTER ADDRESS.
3. Set ADDRESS/DATA switches B and D to the desired register address.
4. Press the SET ADDRESS DISPLAY pushbutton.
5. Jumper 01A-B3P2-J03 to ground. Refer to ALD page CU003.

Note: *This operation does not occur every time. Therefore, when scoping, use a cycle steal time as a sync point. (CS1A-B3Q2B10 on CC002)*

Simulate a Continuous Panel Store Register Operation

1. The 3705 must be stopped.
2. Set the DISPLAY/FUNCTION SELECT switch to REGISTER ADDRESS.
3. Set ADDRESS/DATA switches B and D to the desired register address.
4. Press the SET ADDRESS DISPLAY pushbutton.
5. Jumper 01A-B3P2-J06 to ground. Refer to ALD page CU003.
6. Set the ADDRESS/DATA switches B thru E to the desired data.

Note: *This operation does not occur every cycle time. Therefore, when scoping, use a cycle steal time as a sync point.*

Deactivate Interval Time Bids

Jumper 01A-B3M2-G09 to ground. Refer to ALD page CU014.

Note: *If a bid has already been set, that bid will be honored before the interval timer is deactivated.*

Clock Step Thru IPL Phase 2 (Load ROS)

1. Press the RESET pushbutton.
2. Set the DIAGNOSTIC CONTROL switch to CLOCK STEP.
3. Press the START pushbutton.
4. Jumper 01A-B3P2J09 (+ Active clock step) to 01A-B3L2D09 (+IPL 2 Latch). Refer to ALD pages CU007 and CU010.
5. Press the LOAD pushbutton. Observe IPL phase 2 when the LOAD pushbutton is released.
6. You can now clock step thru the loading of ROS by using the START pushbutton.

DIAGNOSTIC AIDS–CE INDICATOR LATCH CARD

MST-1 CE Indicator Latch Card

C.E. Indicator Latch Card P/N 5851882 is available from Mechanicsburg for servicing IBM products using the MST-1 technology.

The Latch Card is a 2-High, 2-Wide card which plugs onto the pin side of an MST-1 board. The card can be plugged onto any two vertically adjacent socket positions except edge connector positions. The Latch Card is intended for use on socket locations with no discrete wiring; however, with care, it can be used on socket positions that have no second level wraps on any pin. If the Latch Card is left on an MST-1 board for an extended period of time, normal machine vibration may cause it to work loose from the pins and lose contact.

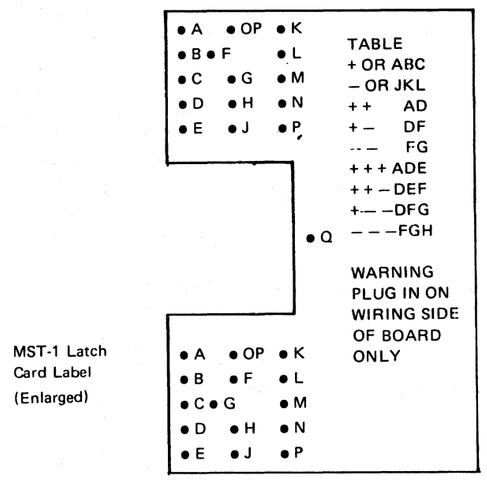
WARNING

The Indicator Latch Card must be plugged onto the MST-1 board with the component side of the card toward the right. If the card is plugged on upside down, or is plugged into the card side of the board, circuit damage will result.

The Latch Card contains two complete latch circuits. Each latch circuit has its own set of input pins, output pins, and latch status indicator lamp.

A reset line which is common to both latch circuits can be activated by the manual reset switch or by a plus signal applied to program pin Q.

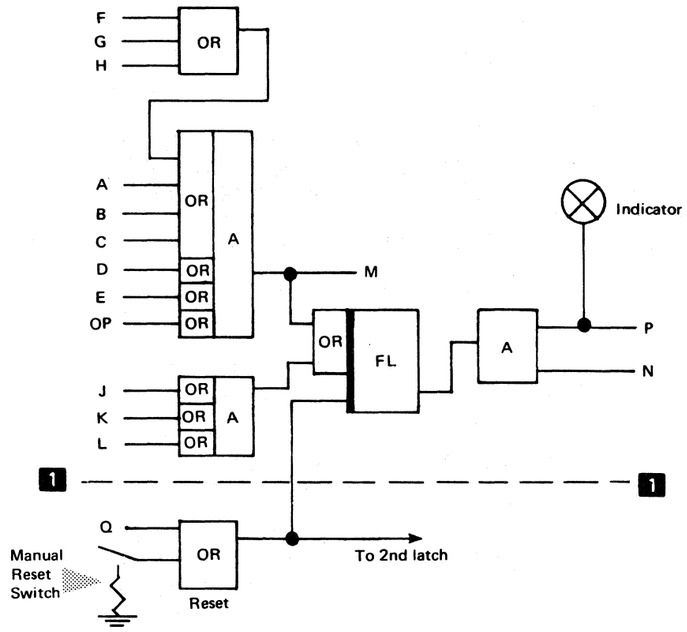
The correlation between active signal levels and input pins to be used is shown below for the various combinations which can be monitored.



Pin OP is an optional, plus level input pin. It can be used in place of, or in addition to, input pins D and E.

Output pin M is a summation of input pins A through H prior to the latch. Pin M will be at a plus level whenever the combination of signals being monitored is active. Thus, the signal occurring at output pin M can be used as an input to the latch circuitry contained on the other half of the latch card.

Output pins P and N provide outputs from the latch. Output pin P will be at a plus level when the latch is set (indicator lamp on) and at a negative level when the latch is reset (indicator lamp off). Pin N provides the inverse level of pin P.



Note: The CE Indicator Card contains two sets of circuitry as shown above line 1 – – 1

Listed below are some of the ways the latch card can be used:

1. Baby Sitter

   To determine if several signal lines are all at their active levels at the same time, plug the card onto the pin side of the MST-1 board and jumper the signal lines to the proper input pins for the ANDing condition being monitored. If all signal lines are at their active level at the same time, the latch will be set and turn on the indicator lamp.

2. One-Time Pulse Detection

   If a signal line should not change during a particular sequence of events, jumper the signal line to an appropriate OR input pin. For example, if the line is plus and should never go minus, jumper it to a -"OR" input pin. If the line goes to a minus level, the latch will be set and turn on the indicator lamp.

3. Scope Sync Point

   The signal lines required to generate the desired sync should be jumpered to appropriate input pins. Jumper a plus level reset signal to pin Q. The latch will be set by the sync condition and reset under control of the reset line. The signal at latch output pin P or N can now be used as a stable scope sync.

Use C.E. Jumper P/N 4110178, cut to required length. The ends of this wire are simply plugged onto the pins to be connected. The plastic insulation coating serves as a receptacle for the pin.

MST-1 Indicator Latch Card P/N 5851882
Indicator Lamp P/N 5353889
Jumper P/N 4110178 Specify length when ordering.
MST-1 Latch Card label P/N 5500728.

Note: *The latch card does not include a label. Always order a label for each latch card.*

DIAGNOSTIC AIDS: TEST BLOCKS (PART 1 OF 2)

These illustrations provide a ready reference to the interface leads available at the interface connector positions on the I/O gate. Some Communication Scanner IFT Manual Intervention Routines refer to wrapping a pair of lines or tying certain lines up or down. The test blocks provide a convenient method of doing this in most cases.

To force an interface lead to the active state, jumper it to 'Data Terminal Ready'. The state of DTR can be determined from the symptom index. If the inactive state of an interface lead is to be tested, allow the lead to float. EIA, CCITT V.35 (except for transmit and receive data), and digital interface lines float to the inactive level.

To wrap data between two compatible line interfaces, jumper all interface leads to their normal operational state. Use the check lists below for typical jumpering.

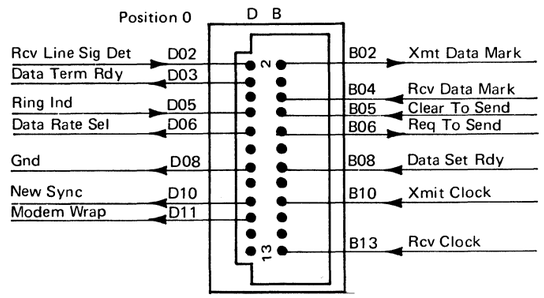
For Interfaces that Connect to Stand-Alone Modems or Local Attachments, Jumper:

a. 'Request to Send' and 'Clear to Send' of the transmit interface to 'Receive Line Signal Detect' (Carrier Detect) of the receive interface using Y jumper P/N 1770810.
b. 'Request to Send' and 'Clear to Send' of the receive interface to 'Receive Line Signal Detect' (Carrier Detect) of the transmit interface using Y jumper P/N 1770810.
c. 'Data Terminal Ready' to 'Data Set Ready' on both interfaces. (See special notes for the LS3 line set on page 1-310).
d. Send data on one line to receive data of the opposite line.
e. Receive data of one line to send data of the opposite line.

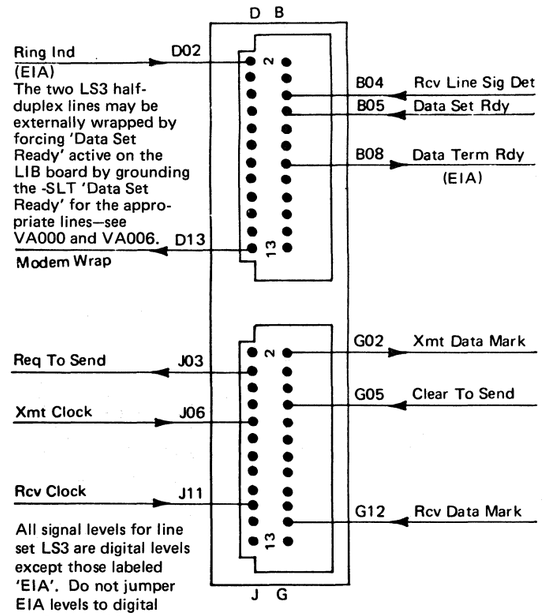
For Interfaces with IBM Limited Distance or Leased Line Adapters or with Leased Line Modems, Jumper:

a. Send data to receive data of the opposite line.
b. Receive data to send data of the opposite line.

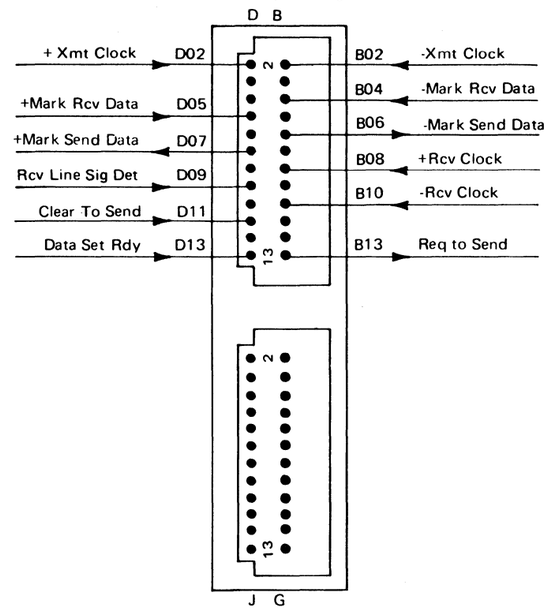
Line Set LS1—Half-Duplex (Logic VA003)
(Note 1) Duplex (Logic VA012)



Line Set LS3—Half-Duplex (Logic VA006)

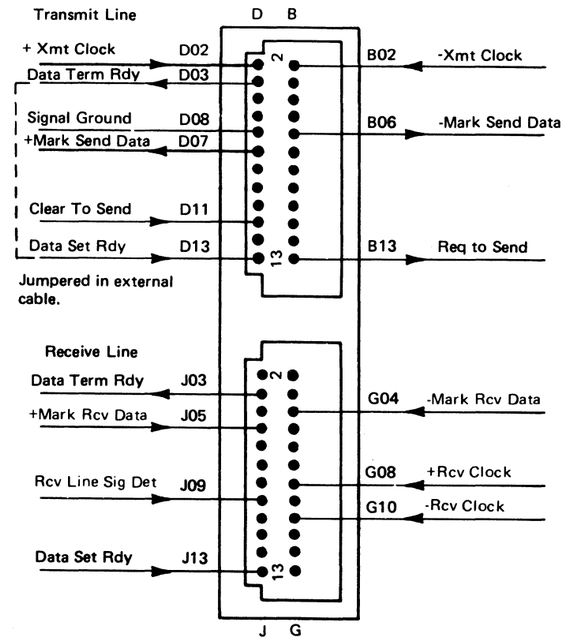


Line Set LS2—Half-Duplex (Logic VA008)

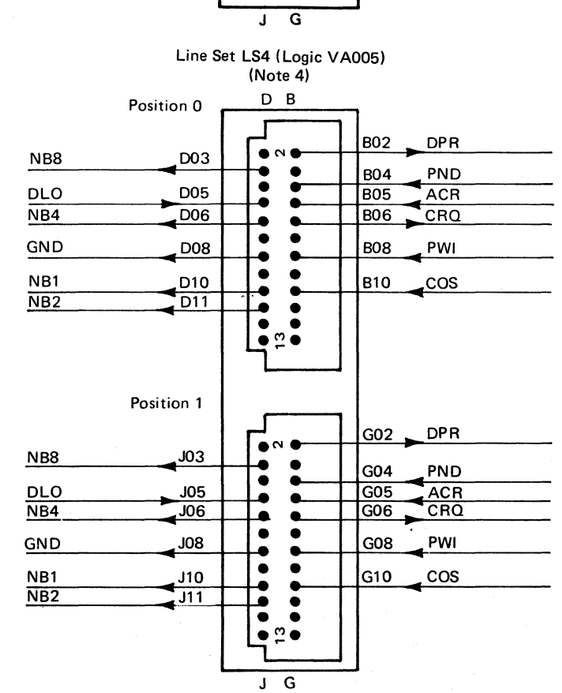


Line Set LS3—Duplex (Logic VA013)

Line Set LS2—Duplex (Logic VA014)



Line Set LS4 (Logic VA005)
(Note 4)



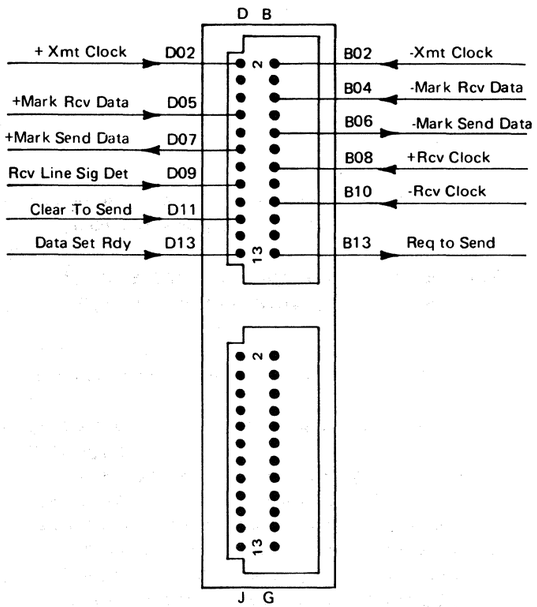
Note: *Test Blocks are shown facing the jumper pin side. See page E-010 for jumper and test block part numbers.*

Notes:

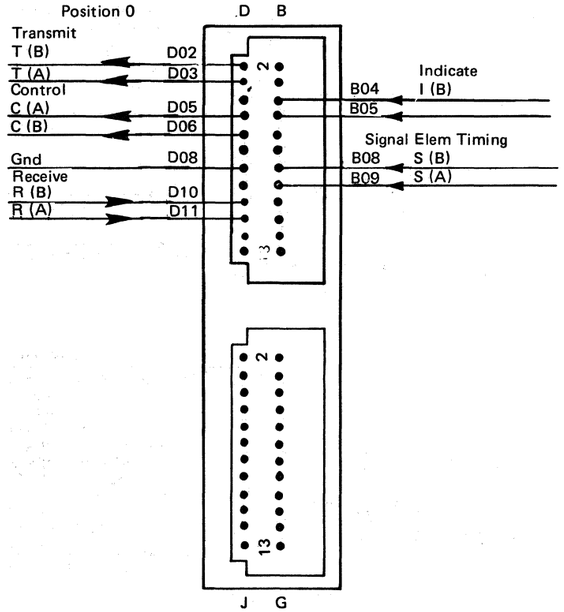
1. *For line set LS1 in duplex mode, use a single wrap block for that line. For LS1 in half-duplex mode, two lines must be wrapped. The 3705-80 ship group contains two LS1 wrap blocks.*
2. *Signals used only by high-address receive line.*
3. *Signals used by both low-address transmit line and high address receive line. Signals not noted are used only by the low-address transmit line.*
4. *Line set LS4 can not be wrapped. Use this test block for reference only.*

DIAGNOSTIC AIDS: TEST BLOCKS (PART 2 OF 2)

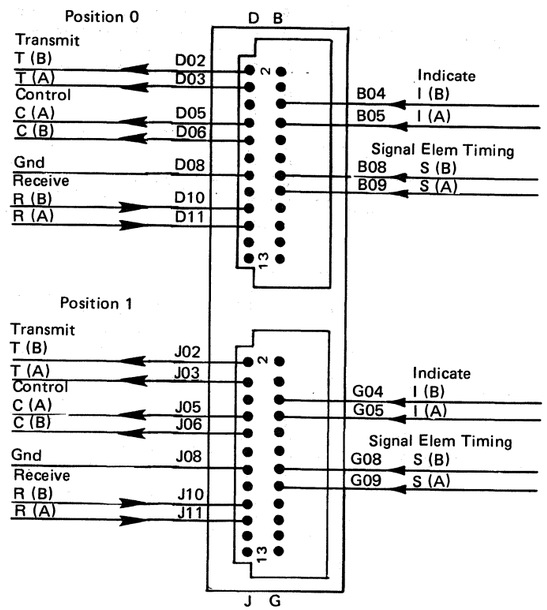
Line Set LS5 (Logic VA015)
(Note 1)



Line Set 8 or 9—Half-Duplex (Logic VA017)
(Note 2)



Line Set 8 or 9—Duplex (Logic VA017)
(Note 3)



Notes:

1. *External clock must be specified to wrap the two half-duplex LS5 lines.*
2. *To wrap the two half-duplex LS8 or LS9 lines, connect T of the transmit line to R of the receive line and C of the transmit line to I of the receive line (connect A to A and B to B). Do not wrap S leads. Internal clock must be specified.*
3. *To wrap the LS8 or LS9 duplex line, connect T (transmit) of position 0 to R (receive) of both positions 0 and 1. Next, connect C (control) of position 0 to I (indicate) of both positions 0 and 1. (Connect A to A and B to B.) Do not wrap S leads. Internal clock must be specified.*

ROS Test

ROS Requirements Depending On Type of Channel Adapter and or Remote Program Loader.

Without Remote Program Loader (RPL)

		CA #2		
		None	CA1	CA4
CA #1	CA1	1	X	X
	CA4	1	X	N

With Remote Program Loader

		RPL
CA #1	CA1	R and 1
	CA4	R and 1

3705-80 with RPL feature only (no type 1 or type 4 CA) uses RPL ROS.

N — Required for two CA4s

1 = CA1 ROS (Mini)

N = CA4 ROS see 2-120

R = RPL ROS

X = Invalid configuration

TYPE 1 AND TYPE 4 CHANNEL ADAPTER

The instructions contained in the ROS program depend upon the type channel adapter that is installed in the 3705-80.

The ROS code enables the controller to load its control program across the channel.

Before the ROS code attempts to transfer the data, it checks the functions and instructions it needs to complete the transfer. The functions tested are:

- Instructions
- Data path
- Channel adapter enable
- Channel adapter selection
- Channel adapter level 3 interrupt
- Receipt of an IPL command on the enabled channel adapter
- That a level 1 or level 3 interrupt was received from the channel adapter

Only the portion of the instructions needed to complete the transfer of the first program module across the channel is tested. The instructions tested are:

- ARI
- LRI
- ORI
- TRM
- LH
- STH
- ST
- BB
- BCL
- BZL
- B
- XR
- IN*, X'60,61,62,64,67,76,77,79,7D,7E'
- OUT*, X'60,62,63,64,66,67,77,79'

*Those input and output instructions associated with the CA and several of those necessary for CCU operation are used but are not thoroughly tested.

ROS checks the data path and uses some of the error detection circuits without testing them.

A listing of the ROS code is in the ALD's beginning on CW101. A flow chart showing the logical flow of ROS-channel adapter operations precedes the ROS listing in the ALDs.

Simulation Run

Immediately following the ROS listing is a simulation run. The simulation run is a listing in instruction execution order showing the contents of the registers used.

Use the simulation run during instruction step procedures in the instruction test portion of ROS as a check for correct operation.

Error Analysis Procedure

Type 1 ROS code presents error indications to the control panel for CCU and channel adapter errors. Observe the error indications and follow the prescribed course of action for each indication.

Control Panel Switches

During the IPL, the MODE SELECT switch and the DIAGNOSTIC CONTROL switch must be in the PROCESS position for the indicators to function correctly.

Instruction Testing

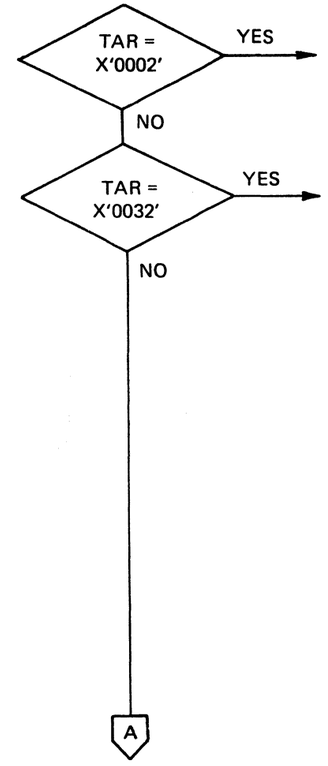
Before trying to load data across the channel, ROS Program code tests the preceding instructions. The general procedure for locating an instruction execution failure is to step the instructions through the failing section of the instruction test portion of the code.

The simulation run following the ROS code listing in the ALD is to be used during the instruction step procedure as a check for correct operation.

The indications that appear on the control panel are:

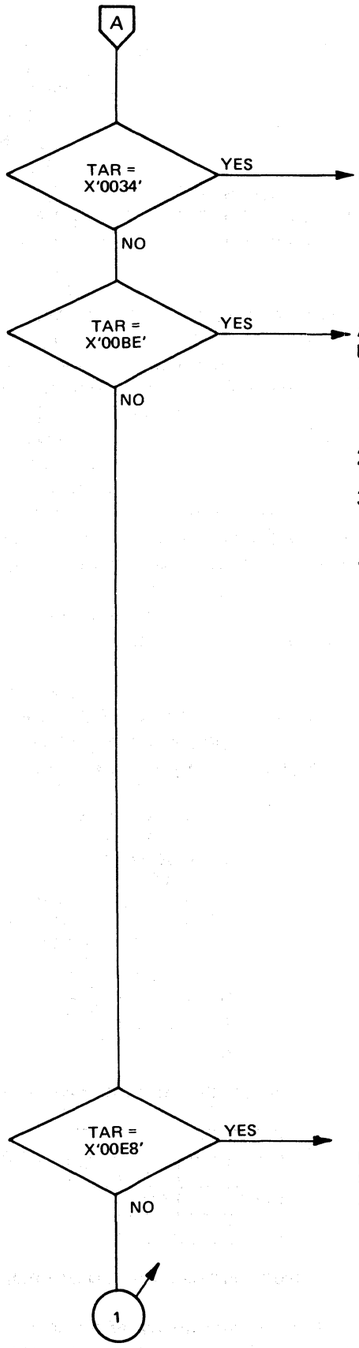
IPL Phase III Program Stop Hard Stop Load Test
This is a CCU failure indication. TAR contains the address of the next instruction to be executed. This value is the address of the stop instruction +2. Check the contents of TAR against the following list; if it is equal to any value given, follow the indicated procedure.

See page 2-020 If these lamps are not on.



An instruction failed to execute. Using the ROS listing and the simulation run, use the *load address compare* procedure with the MODE SELECT switch set to ADDRESS COMPARE PROGRAM STOP to stop at various places in the program. Then use the *instruction step* procedure to step through the program and locate the failure addresses at the beginning of test routines in the listing as stopping points.

1. Set the MODE SELECT switch to ADDRESS COMPARE PROGRAM STOP.
2. Set the beginning address for one of the test routines in the ADDRESS/DATA switches. Refer to the ROS listing for the beginning addresses of the routines.
3. Retry the IPL.
4. If the same error occurs before the program stop, change the address in the ADDRESS/DATA switches to a previous address. The address of the first instruction may be used if necessary.
5. Retry until the program stop occurs.
6. When the program stops at the selected address, set the MODE SELECT switch to INSTRUCTION STEP.
7. Step through the code, following the listing and the simulation run, to locate the error. (See CW000.)



Output instruction failure.

A branch on bit failure or 'Z' latch failing to set caused this hard stop condition.

1 Set up to program stop at the beginning address of the Branch on Bit Test (X'00A4') from the ROS listing.

2 Retry the IPL.

3 When the Program Stop light comes on, set the MODE SELECT switch to INSTRUCTION STEP.

4 Step through the test. Register 1 contains the instruction and indicates what is being tested. Bit 0.7 on indicates that byte 1 is being tested, and bit 0.7 off indicates that byte 0 is being tested. Bits 0.2, 0.3, and 1.0 are a binary indication of the bit being tested within the byte. The bits are being tested for "solid" on and off conditions.

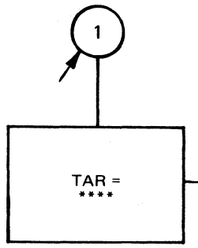
Register 1		Bits Being Tested	
Byte 0	Byte 1	Byte 0	Byte 1
01234567	01234567	01234567	01234567
XX00XXX0	0XXXXXXX	10000000	00000000
XX00XXX0	1XXXXXXX	01000000	00000000
XX01XXX0	0XXXXXXX	00100000	00000000
XX01XXX0	1XXXXXXX	00010000	00000000
XX10XXX0	0XXXXXXX	00001000	00000000
XX10XXX0	1XXXXXXX	00000100	00000000
XX11XXX0	0XXXXXXX	00000010	00000000
XX11XXX0	1XXXXXXX	00000001	00000000
XX00XXX1	0XXXXXXX	00000000	10000000
XX00XXX1	1XXXXXXX	00000000	01000000
XX01XXX1	0XXXXXXX	00000000	00100000
XX01XXX1	1XXXXXXX	00000000	00010000
XX10XXX1	0XXXXXXX	00000000	00001000
XX10XXX1	1XXXXXXX	00000000	00000100
XX11XXX1	0XXXXXXX	00000000	00000010
XX11XXX1	1XXXXXXX	00000000	00000001

X = don't care

A level 1 interrupt was requested by other than an IPL level 1 interrupt request. The IPL request was expected. Other conditions that could have caused the interrupt are:

Condition:

Address compare
Adapter check
In/out check
Address exception
Protect check



If TAR contains an address that has not been previously defined, a program load or execution failure probably occurred. To verify the program was loaded correctly, execute the ROS Data Transfer Test and the ROS Address Generation Test.

ROS Data Transfer Test
Display main storage addresses

1 location X'0032' → All bits should be off in Display B. Suspect any bit that is on in the display as being continuously on from storage (see 7-0030 or 7-260). The bit can also be continuously on from ROS, (see 6-961).

2 location 0056 → All bits should be on in Display B. Suspect any bit that is not on as being continously off from storage (see 7-030 or 7-260). The bit can also be continuously off coming from ROS, (see 6-961).

ROS Address Generation Test
Display main storage addresses

1 X'0000' should contain X'7004' →

If Location X'0000' Contains	*Suspect SAR Bit*	*See*
X'F6FF'	15 on	7-260
X'98B8'	14 on	7-260
X'810B'	13 on	7-260
X'0082'	12 on	7-260
X'0492'	11 on	7-260
X'F1FF'	10 on	7-260
X'1305'	9 on	7-260
X'6174'	8 on	7-260

2 X'01FE' should contain '0404' →

If Location 01FE Contains	*Suspect SAR Bit*	*See*
X'1001'	15 off	7-260
X'81FE'	14 off	7-260
X'6124'	13 off	7-260
X'9813'	12 off	7-260
X'8602'	11 off	7-260
X'A8A3'	10 off	7-260
X'A863'	9 off	7-260
X'8160'	8 off	7-260

Note: *Only SAR bits 8 through 15 are used to address low storage. The other SAR bits are not used.*

If no discrepancy has been found in the ROS Data Transfer or Address Generation Test, verify that the control panel is set up properly and re-try the IPL.

These charts are valid only for intermittent errors. ROS must load into storage correctly at least one time out of a number of Load pushbutton operations, for these charts to be valid. Otherwise, use control panel and display procedures (1-140) to determine if there is an addressing problem.

Channel Checking

IPL Phase III Load
This is an indication that communications between the channel adapter and the host CPU should be checked, using OLTEP or OLTSEP with the initial test, OLTs or IFTs. The customer's first program may be used if desired. Refer to the status and sense information chart at the end of this section if CA operation is possible but the load operation is not successful. If CA operation is not possible, proceed with the CA ROS checkout routines.

If the instruction testing has been completed, try the channel adapter ROS checkout routine when there is a problem.

Type 1 or Type 4 Channel Adapter ROS Checkout Routine

1 Disable all channel interfaces. Verify that the control panel INTERFACE ENABLED lights are off.

2 Press the RESET pushbutton.

3 Press the LOAD pushbutton.

4 Press the STOP pushbutton.

5 Set the MODE SELECT switch to INSTRUCTION STEP.

6 Set the DISPLAY/FUNCTION select switch to TAR & OP REGISTER.

7 Press the START pushbutton. Observe the address in display A.

8 Press the START pushbutton several more times and observe the program looping through addresses X'00E8', '00EA', '00EC', '00EE', '00F0', '00F2', '00F4', and '00F6'.

9 If this loop is not being executed, one of the following problems is indicated:
- An interface remained enabled.
- An incorrect branch occurred.
- Contents of storage is incorrect.

To locate the failure

10 Use the *load address compare* procedure with the MODE SELECT switch set to ADDRESS COMPARE PROGRAM STOP to stop at X'00E4'. Then follow the ROS listing using the instruction step procedure.

Observe the normal program loop while the 3705-80 is waiting for initial selection. The host must be *unable* to select the 3705-80 for an IPL.

1 Enable an interface (more than one interface may be installed; enable only one). When an interface is enabled, ROS code may cause IPL phase 1 and 2 if certain conditions are present.

2 Press the CHECK RESET pushbutton.

3 Press the LOAD pushbutton. Verify that the correct interface enabled light comes on.

4 Press the STOP pushbutton.

5 Set the MODE SELECT switch to INSTRUCTION STEP.

6 Set the DISPLAY/FUNCTION SELECT switch to TAR & OP REGISTER.

7 Press the START pushbutton. Observe the address in display A. With the LOAD light on, continue to press the START pushbutton to display the loop X'0124', '0126', '0128', '012A' and '012E'.

8 Set the MODE SELECT switch to PROCESS.

9 If the loop is incorrect, use the *load address compare* procedure with the MODE SELECT switch set to ADDRESS COMPARE PROGRAM STOP to stop at X'0122'. Then, following the program listing, use the instruction step procedure to locate the failure.

10 If the loop is correct, press the START pushbutton to return to normal operation.

Check
Check to see that the initial test or first program module was loaded correctly. Use the *load address compare* procedure with the MODE SELECT switch set to ADDRESS COMPARE PROGRAM STOP to stop at address X'01FA'. This is the last ROS instruction before control is turned over to the next program. If this program stop occurs, it indicates that ROS is giving control to the next program correctly.

If the instruction test section of ROS is executed correctly, but control is not turned over to the next program correctly, check to see if the program loops within repeating major branches that match the list and indicate general areas of failure.

ROS repeating branches that may be caused by a channel adapter failure:

Repeating Branches	*Probable Cause*	*Check the Contents of*		
		Reg.	*Byte*	*Bit*
00F6-00E8	Interface will not become enabled	67	1	4
010E-0104	Cannot develop a level 1 or level 3 interrupt	60 67 76 77	0 0 1	0 5 4
011A-0124 0126-0110	A solid level 1 interrupt	76	0	5
012A-0144	A solid level 3 initial select interrupt occurred	60 77	0 1	0 4
012C-01AA	A solid level 3 data service interrupt	60 77	0 1	0 4

These steps indicate the general area of the program that should be checked for an apparent type 1 channel adapter failure occurring after the CPU has issued an IPL command.

Use the *load address compare* procedure with the MODE SELECT switch set to ADDRESS COMPARE PROGRAM STOP to stop at the following addresses to determine to what extent the ROS program has completed the transfer of the first program or Initial Test.

Address X'0404'
This is the entry address for the initial test or first program. If this program stop occurs, refer to the initial test description, Vol I (SY27-0208) of the IBM 3705-80 ML (maintenance library), or to the first program description, for additional information. The ROS program is no longer being executed.

Address X'01CA'
At this address, the program checks to verify that the IPL command was received. Register X'61', byte 1 contains the command.

Address X'0138'
Check the address that is requesting service. Register X'61' byte 0 should contain the single subchannel address that is requesting service.

Address X'01EA'
Compare the known byte count with the hardware byte count, after the initial test or first program data transfer. The contents of register 1 should equal the contents of register 5. Register 1 should contain a value of X'400' plus the byte count of the program (located in storage at X'0402'). Register 5 starts with a value of X'400' and increments by 2 as ROS loads the program, two bytes at a time.

The following status and sense combinations are developed by ROS for various conditions that occur when the ROS program is being executed:

0F Channel End, Device End, Unit Check, Unit Exception, and sense of IPL Required.

A byte count error occurred during the initial test or first program module transfer.

0E Channel End, Device End, Unit Check, sense of IPL Required, and Equipment Check

A false level 1 or level 3 interrupt occurred at initial selection time.

06 Device End, Unit Check, and Sense of IPL Required

Either an IPL is required because of normal conditions or a failure to recognize that the single subchannel is active.

00 Sense of IPL Required

A system reset has occurred.

N ROS TEST (PART 1 OF 3)

N-Channel ROS for the Type 4 CA

The N-channel ROS is used when two type 4 CAs are installed.

The N-channel ROS code allows the loading of the control program to occur across either of the installed type 4 CAs. The N-channel ROS code:

1. Tests the CCU instructions.
2. Selects and enables the installed type 4 CAs.
3. Scans the installed type 4 CAs for an IPL command then begins the IPL on the CA with the IPL command.
4. Continuously scans each type 4 CA for interrupts.
5. Prepares each CA having an active command and while no IPL is in progress sends a final ending status of 'CE, DE, UC' with a sense byte of 'not initialized'.
6. Prepares each CA not having an active command and while no IPL is in progress sends an asynchronous status of 'DE, UC' with a sense byte of 'not initialized'.
7. Sends an ending status of 'CE, DE' to a Sense command if an IPL is not in progress.
8. Begins loading the control program through the first type 4 CA that ROS recognizes as having received an IPL command.
9. Prepares the other CA to respond with an ending status OF 'CE, DE, UE' to Sense commands once an IPL is in progress on either CA.
10. Allows a subsequent IPL command to override an existing IPL command in progress. A new IPL operation begins with the subsequent IPL command that can occur on any channel.
11. Handles all type 4 CA interrupts until control is passed to the loader.

Before the ROS code attempts to transfer the data, it checks the functions and instructions it needs to complete the transfer. Tested are:

- Instructions
- Data path
- Channel adapter enable
- Channel adapter selection
- Channel adapter level 3 interrupt
- Receipt of an IPL command on each enabled channel adapter
- That a level 1 or level 3 interrupt was received from the channel adapter

Only the portion of the instructions needed to complete the transfer of the first program module across the channel is tested. The instructions tested are:

- ARI
- LRI
- ORI
- TRM
- LH
- STH
- ST
- BB
- BCL
- BZL
- B
- XR
- IN*, X'60,61,62,64,67,76,77,79,7D,7E'
- OUT*, X'60',62,63,64,66,67,77,79'

*Those input and output instructions associated with the CA and several of those necessary for CCU operation are used but are not thoroughly tested.

ROS checks the data path and uses some of the error detection circuits without testing them.

A listing of the ROS code is in the ALD's beginning on CW501. A flowchart showing the logical flow of ROS-channel adapter operations precedes the ROS listing in the ALDs (CW500).

Simulation Run

The simulation run starts on CW301. The simulation run is a listing in instruction execution order showing the contents of the registers used.

Use the simulation run during instruction step procedures in the instruction test portion of ROS as a check for correct operation.

Error Analysis Procedure

N ROS code presents error indications to the control panel for CCU and channel adapter errors. Observe the error indications and follow the prescribed course of action for each indication.

Control Panel Switches

During the IPL, the MODE SELECT switch and the DIAGNOSTIC CONTROL switch must be in the PROCESS position for the indicators to function correctly.

Instruction Testing

Before trying to load data across the channel, ROS program code tests the proceding instructions. The general procedure for locating an instruction execution failure is to step the instructions through the failing section of the instruction test portion of the code.

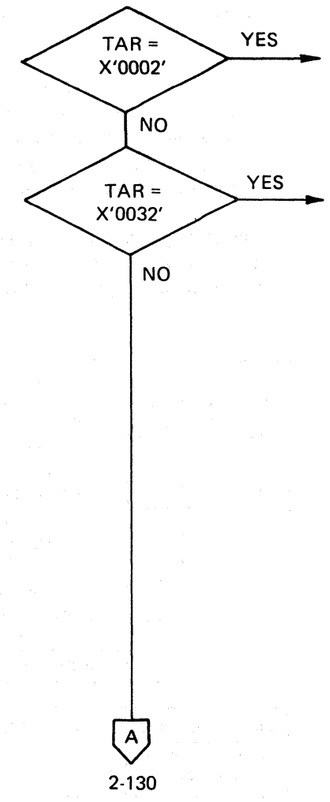
The simulation run following the ROS code listing in the ALD is to be used during the instruction step procedure as a check for correct operation.

The indications that appear on the control panel are:

IPL Phase III
Program Stop
Hard Stop
Load
Test

This is a CCU failure indication. TAR contains the address of the next instruction to be executed. This value is the address of the stop instruction +2. Check the contents of TAR against the following list; if it is equal to any value given, follow the indicated procedure.

See page 2-020
If these lamps are not on.

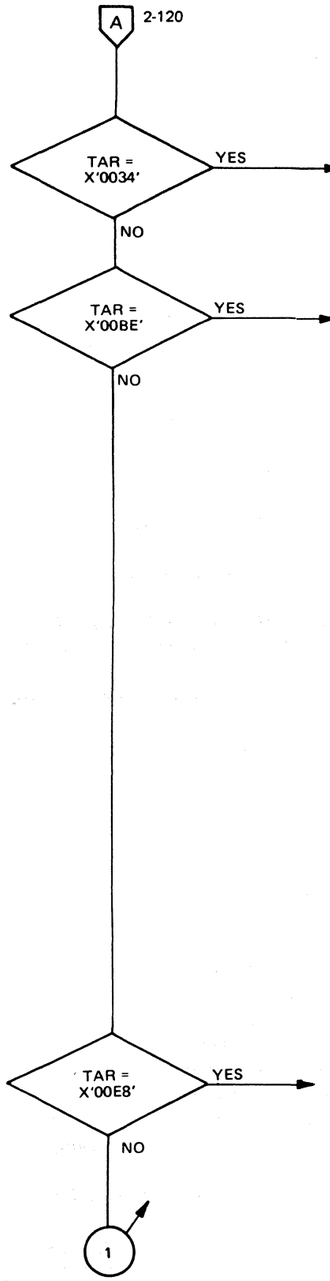


2-130

An instruction failed to execute. Using the ROS listing and the simulation run, use the *load address compare* procedure with the MODE SELECT switch set to ADDRESS COMPARE PROGRAM STOP to stop at various places in the program. Then use the *instruction step* procedure to step through the program and locate the failure addresses at the beginning of test routines in the listing as stopping points.

1. Set the MODE SELECT switch to ADDRESS COMPARE PROGRAM STOP.
2. Set the beginning address for one of the test routines in the ADDRESS/DATA switches. Refer to the ROS listing for the beginning addresses of the routines.
3. Retry the IPL.
4. If the same error occurs before the program stop, change the address in the ADDRESS/DATA switches to a previous address. The address of the first instruction may be used if necessary.
5. Retry until the program stop occurs.
6. When the program stops at the selected address, set the MODE SELECT switch to INSTRUCTION STEP.
7. Step through the code, following the listing and the simulation run, to locate the error. (See CW000.)

N ROS TEST (PART 2 OF 3)



Output instruction failure.

A branch on bit failure or 'Z' latch failing to set caused this hard stop condition.

1 Set up to program stop at the beginning address of the Branch on Bit Test (X'00A4') from the ROS listing.

2 Retry the IPL.

3 When the Program Stop light comes on, set the MODE SELECT switch to INSTRUCTION STEP.

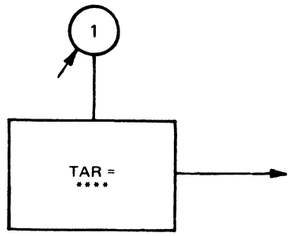
4 Step through the test. Register 1 contains the instruction and indicates what is being tested. Bit 0.7 on indicates that byte 1 is being tested, and bit 0.7 off indicates that byte 0 is being tested. Bits 0.2, 0.3, and 1.0 are a binary indication of the bit being tested within the byte. The bits are being tested for "solid" on and off conditions.

Register 1		Bits Being Tested	
Byte 0 01234567	Byte 1 01234567	Byte 0 01234567	Byte 1 01234567
XX00XXX0	0XXXXXXX	10000000	00000000
XX00XXX0	1XXXXXXX	01000000	00000000
XX01XXX0	0XXXXXXX	00100000	00000000
XX01XXX0	1XXXXXXX	00010000	00000000
XX10XXX0	0XXXXXXX	00001000	00000000
XX10XXX0	1XXXXXXX	00000100	00000000
XX11XXX0	0XXXXXXX	00000010	00000000
XX11XXX0	1XXXXXXX	00000001	00000000
XX00XXX1	0XXXXXXX	00000000	10000000
XX00XXX1	1XXXXXXX	00000000	01000000
XX01XXX1	0XXXXXXX	00000000	00100000
XX01XXX1	1XXXXXXX	00000000	00010000
XX10XXX1	0XXXXXXX	00000000	00001000
XX10XXX1	1XXXXXXX	00000000	00000100
XX11XXX1	0XXXXXXX	00000000	00000010
XX11XXX1	1XXXXXXX	00000000	00000001

X = don't care

A level 1 interrupt was requested by other than an IPL level 1 interrupt request. The IPL request was expected. Other conditions that could have caused the interrupt are:

Address compare
Adapter check
In/out check
Address exception
Protect check



If TAR contains an address that has not been previously defined, a program load or execution failure probably occurred. To verify the program was loaded correctly, execute the ROS Data Transfer Test and the ROS Address Generation Test.

ROS Data Transfer Test

Display main storage addresses

1 location X'0032' → All bits should be off in Display B. Suspect any bit that is on in the display as being continuously on from storage (see 7-260). The bit can also be continuously on from ROS, (see (6-961).

2 location 0056 → All bits should be on in Display B. Suspect any bit that is not on as being continuously off from storage (see 7-260). The bit can also be continuously off coming from ROS, (see 6-961).

ROS Address Generation Test

Display main storage addresses

1 X'0000' should contain X'7004' →

2 X'03FE' should contain X'03E8' →

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If location X'0000' Contains	*Suspect SAR Bit*	*See*
X'F6FF'	15 on	7-260
X'98B8'	14 on	7-260
X'810B'	13 on	7-260
X'0082'	12 on	7-260
X'0492'	11 on	7-260
X'F1FF'	10 on	7-260
X'1305'	9 on	7-260
X'66C8'	8 on	7-260
X'4303'	7 on	7-260
If location X'03FE' Contains	*Suspect SAR Bit*	*See*
X'0708'	15 off	7-260
X'0006'	14 off	7-260
X'0608'	13 off	7-260
X'0002'	12 off	7-260
X'7004'	11 off	7-260
X'7004'	10 off	7-260
X'003C'	9 off	7-260
X'717C'	8 off	7-260
X'88DB'	7 off	7-260

Note: *Only SAR bits 7 through 15 are used to address low storage. The other SAR bits are not used.*

If no discrepancy has been found in the ROS Data Transfer or Address Generation Test, verify that the control panel is set up properly and re-try the IPL.

These charts are valid only for intermittent errors. ROS must load into storage correctly at least one time out of a number of Load pushbutton operations, for these charts to be valid. Otherwise, use control panel and display procedures (1-140) to determine if there is an addressing problem.

N ROS TEST (PART 3 OF 3)

Channel Checking (Part 1)

IPL Phase III Load

This is an indication that communications between the channel adapter and the host processor should be checked, using OLTEP or OLTSEP with the initial test, OLTs or IFTs. The customer's first program may be used if desired. Refer to the status and sense information chart at the end of this section if CA operation is possible but the load operation is not successful. If CA operation is not possible, proceed with the CA ROS checkout routines.

If the instruction testing has been completed, try the type 4 channel adapter N ROS checkout routine when there is a problem.

Type 4 Channel Adapter N ROS Checkout Routine

1 Disable all channel interfaces. Verify that the control panel INTERFACE ENABLED lights are off.

2 Press the RESET PUSH BUTTON.

3 Press the LOAD push button.

4 Press the STOP push button.

5 Set the MODE SELECT switch to INSTRUCTION STEP.

6 Set the DISPLAY/FUNCTION select switch to TAR & OP REGISTER.

7 Press the START push button. Observe the address in display A.

8 Press the START push button several more times and observe the program looping through addresses X'0126', X'0128', X'012A', X'012C', X'012E', X'0130', X'0132', X'0134', X'0136', X'0138', X'013A', X'013C', X'016A' and X'016C'.

9 If this loop is not being executed, one of the following problems is indicated:
- An interface remained enabled.
- An incorrect branch occurred.
- Contents of storage is incorrect.

To locate the failure

10 Use the *load address compare* procedure with the MODE SELECT switch set to ADDRESS COMPARE PROGRAM STOP to stop at X'0126'. Then follow the ROS listing using the instruction step procedure.

Observe the normal program loop while the 3705-80 is waiting for initial selection. The host must be *unable* to select the 3705-80 for an IPL.

1 Enable one of the interfaces. When the interface is enabled, ROS code may cause IPL phase 1 and 2 if certain conditions are present.

2 Press the CHECK RESET push button.

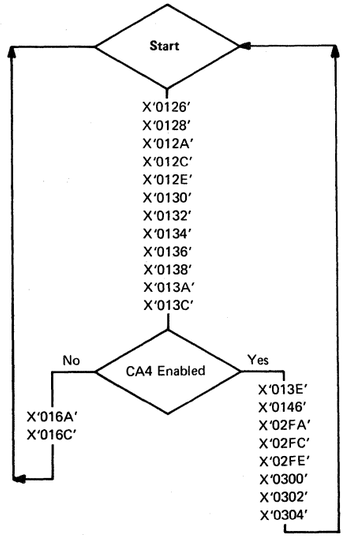
3 Press the LOAD push button. Verify that the correct interface enabled lights come on.

4 Press the STOP push button.

5 Set the MODE SELECT switch to INSTRUCTION STEP.

6 Set the DISPLAY/FUNCTION SELECT switch to TAR & OP REGISTER.

7 Press the START push button. Observe the address in display A. With the LOAD light on, continue to press the START push button to display the loop.



8 Set the MODE SELECT switch to PROCESS.

9 If the loop is incorrect, use the *load address compare* procedure with the MODE SELECT switch set to ADDRESS COMPARE PROGRAM STOP to stop at X'0126'. Then, following the program listing, use the instruction step procedure to locate the failure.

10 If the loop is correct, press the START push button to return to normal operation.

Check
Check to see that the initial test or first program module was loaded correctly. Use the *load address compare* procedure with the MODE SELECT switch set to ADDRESS COMPARE PROGRAM STOP to stop at address X'037C'. This is the last ROS instruction before control is turned over to the next program. If this program stop occurs, it indicates that ROS is giving control to the next program correctly.

Channel Checking (Part 2)

These steps indicate the general area of the program that should be checked for an apparent type 4 channel adapter failure occurring after the processor has issued an IPL command.

Use the *load address compare* procedure with the MODE SELECT switch set to ADDRESS COMPARE PROGRAM STOP to stop at the following addresses to determine to what extent the ROS program has completed the transfer of the first program or Initial Test.

Address X'0404'
This is the entry address for the initial test or first program. If this program stop occurs, refer to the Initial Test description in the *Start* section of this FETMM (Volume 1, SY27-0208). The ROS program is no longer being executed.

Address X'0268'
At this address, the program checks to verify that the IPL command was received. Register X'61', byte 1 contains the command.

Address X'01AE'
Check the address that is requesting service. Register X'61' byte 0 should contain the single subchannel address that is requesting service.

Address X'0364'
Compare the known byte count with the hardware byte count, after the initial test or first program data transfer. The contents of register 1 should equal the contents of register 5. Register 1 should contain a value of X'400' plus the byte count of the program (located in storage at X'0402'). Register 5 starts with a value of X'400' and increments by 2 as ROS loads the program, two bytes at a time.

The following status and sense combinations are developed by ROS for various conditions that occur when the ROS program is being executed:

0F Channel End, Device End, Unit Check, Unit Exception, and sense of IPL Required.

A byte count error occurred during the initial test of first program module transfer.

0E Channel End, Device End, Unit Check, sense of IPL Required, and Equipment Check.

A false level 1 or level 3 interrupt occurred at initial selection time.

06 Device End, Unit Check, and Sense of IPL Required.

Either an IPL is required because of normal conditions or a failure to recognize that the single subchannel is active.

00 Sense of IPL Required.

A system reset has occurred.

Central Control Unit

WARNING
Touching the pin side of the CCU board while the 3705-80 is running can cause CCU errors.

The Central Control Unit (CCU) contains all the circuits and data flow paths necessary to execute the instruction set and to control storage and the attached adapters. The CCU, controlled by a program in storage, contains 32 general registers and various hardware registers that the control program uses for instruction execution and data handling.

The CCU can execute 51 instructions, which can be used to transfer data from one register to another, to store data from a register in 3705-80 storage, to load data from storage into a register, and to perform various arithmetic and hardware functions. Some of the CCU hardware registers can be addressed as external registers by 'input' and 'output' instructions. (The 'input' or 'output' instruction is indicated beside the register in the data flow on page 6-020.)

Each program, CCU, or adapter request has an assigned priority for use of the CCU. When any control program or hardware function requests use of the 3705 (an interrupt request), the priority system determines when the CCU will handle the interrupt request.

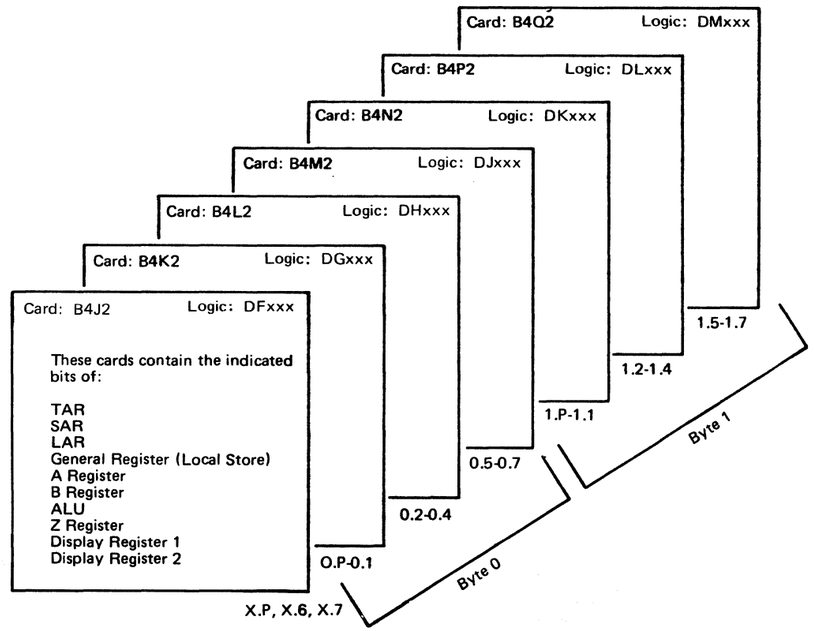
Each of the interrupt requests is assigned to one of five program levels. Program level 1 has the highest priority and program level 5, the lowest. The machine priority controls determine when an interrupt can occur.

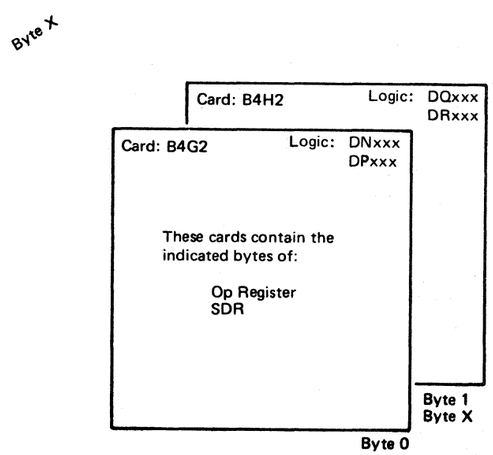
The CCU has a storage protection mechanism that monitors attempts either to modify storage or to execute instructions in protected storage. Storage protection causes a check when the contents of storage are accessed for unauthorized modification.

Page 6-020 shows the general data flow for the CCU. Data flow for a particular operation is determined by the instruction, cycle steal, or control operation being performed.

Abbreviations Used in This Section

ALU — Arithmetic Logic Unit
IAR — Instruction Address Register
LAR — Lagging Address Register
Op Reg — Operation Register
PC — Parity Check
PG — Parity Generation
SAR — Storage Address Register
SDR — Storage Data Register
TAR — Temporary Address Register





Cards That Can Be Swapped in The CCU

- B4J2, B4K2 and B4N2
- B4L2, B4M2, B4P2, and B4Q2
- B4H2 and B4G2
- B4A4, and B4B2
- B4A2 and B4A3
- B3U2, B3U3, and B3U4
- B3T2 and B3T3
- B4U2, B4U3

3705-80 CARD FUNCTIONS

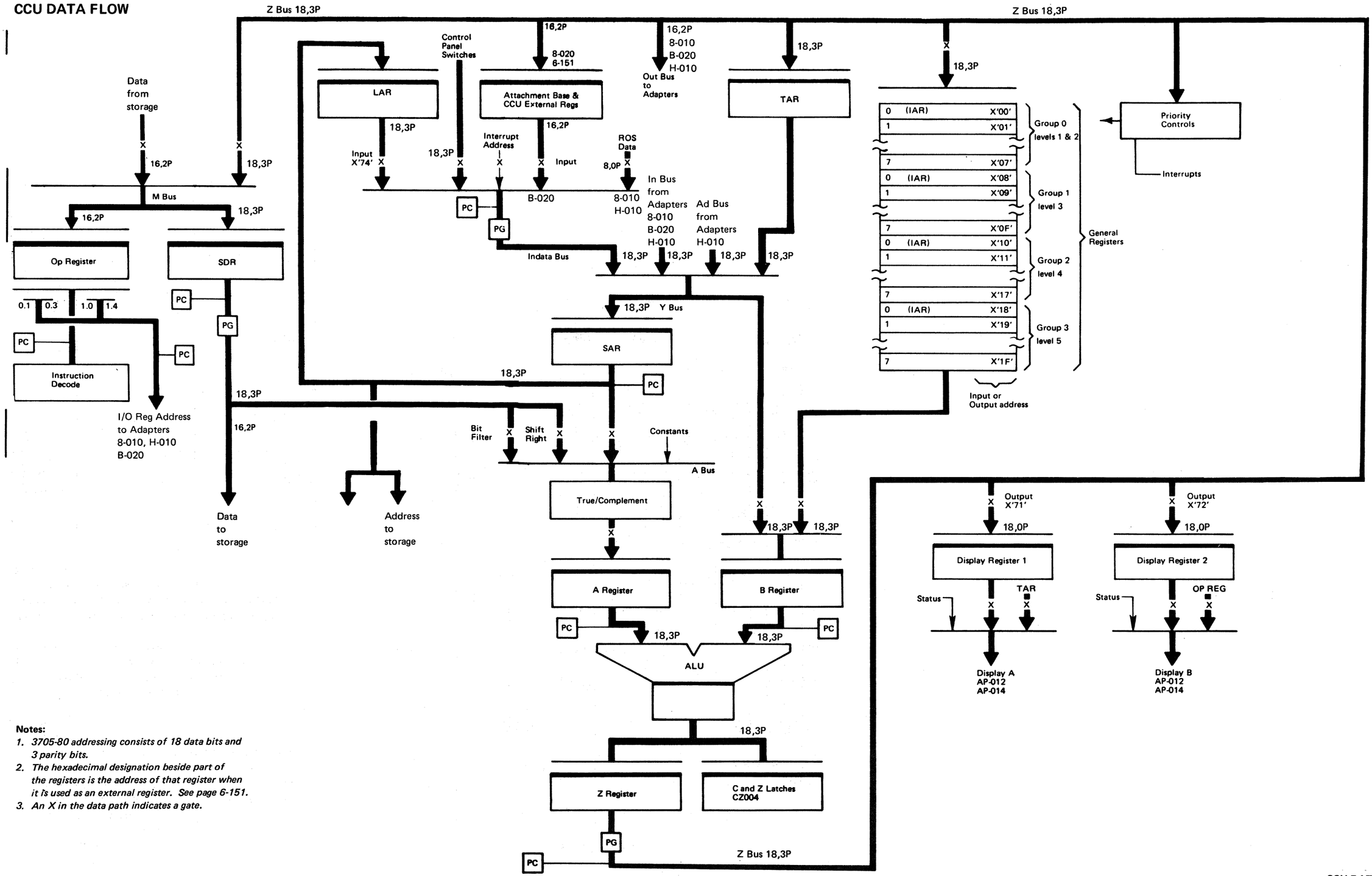
See page 6-000 also.

Card Location	*ALD Pages*	*Card Function*
B3C4	CU0016 CU0017	Power-on Reset Force Storage Test Pattern and Redrive to MEM
B3F2	CS002,CS004 CS006-CS007	Part of Data Flow Register Controls Data Flow Register Control Timing
B3G2	CZ001-CZ005 CQ001 CQ004-CQ005 CD001	C and Z Condition Code Latches and the Generation of Their Sets and Gates Part of Adapter Interface Controls Pulsed Inputs and Outputs Part of Instruction Decode
B3H2	CD001-CD004 CS003	Part of Instruction Decode Part of Data Flow Register Controls
B3J2	CA001-CA004 CD001	ALU Controls Part of Instruction Decode
B3K2	CL001-CL005	Local Store Controls
B3L2	CU005-CU006 CU009-CU010 CU014 CK007 CP006-CP007 CU005	Part of Panel Controls Prog Level 1 Prog Check Detection Meter and Interval Timer Test Mode and Check Stop Mode
B3M2	CU014-CU015 CP002-CP005 CS001	Part of Panel Controls Part of Priority Controls, Program Level Select, Program Level Masks and 'Program Level Entered' Latches Set LAR
B3N2	CK003-CK007 CU001 CU013	Error Detection, Error Register Part of Panel Controls Part of CCU Indata Bus
B3P2	CU003-CU004 CU006-CU007 CS005	Part of Panel Controls M Bus Assembler Control

Card Location	*ALD Pages*	*Card Function*
B3Q2	CC002-CC003 CC004-CC005 CC008 CS001 CQ001-CQ002	Instruction and Cycle-Steal Times Instruction and Cycle-Steal Counter and Cycle Counter Error Detection Instruction Starts and Cycle Stops Maintenance Condition Part of Adapter Interface Controls
B3R2	CS007 CC001 CC006 CC007 CQ001-CQ002	Set SAR, DR1, and DR2 ABCD Counter Local Store Address Register and T Times Clock and machine oscillator Part of Adapter Interface Controls
B3S2	CK001-CK002 CR001-CR008 CU013	Force Errors BSC and SDLC CRC Generation Part of CCU Indata Bus
B3T2	AP001-AP008	Part of Control Panel Switches and Pushbuttons
B3T3	AP001-AP008	Part of Control Panel Switches and Pushbuttons
B3T4	CP001 CM001	Part of Priority Controls Memory Reset
B3U2	AP003-AP015	Part of Control Panel Switches and Pushbuttons
B3U3	AP004-AP011	Part of Control Panel Switches and Pushbuttons
B3U4	AP001-AP008	Part of Control Panel Switches and Pushbuttons
B3U5	CC007 AP008	8 MHz Oscillator Lamp Test
B4A2	DS004	SDR Drivers and Receivers for Byte 1

Card Location	*ALD Pages*	*Card Function*
B4A3	DS002	SDR Drivers and Receivers for Byte 0
B4A4	DB101	Memory Control Cable Drivers
B4B2	DS001	SAR Drivers
B4C2	CG001	Gated Indata Bit X.6
B4D2	CV001-CV061 CM002-CM003	Storage Protect and Error Detection Read Call/Write Call, Storage Size Input and Allow Set Memory Diagnostic Register
B4F2	CW011-CW012	Read-Only Storage
B4F4	CW001	Alternate ROS Feature
B4F5	DW001	Control Signal Terminators
B4R2	CF001-CF002 CF003 CF004 CF004	Force Constants Bit Filter and Parity Generator Shift Right Controls Add Constants
B4U2	AP012-AP015	Part of Panel Indicator Circuits
B4U3	AP009-AP011	Part of Panel Indicator Circuits
B4U4	AP001	Panel Rotor Switches

CCU DATA FLOW



Notes:

1. *3705-80 addressing consists of 18 data bits and 3 parity bits.*
2. *The hexadecimal designation beside part of the registers is the address of that register when it is used as an external register. See page 6-151.*
3. *An X in the data path indicates a gate.*

CLOCK TIMES

3705-80 STORAGE

Each 1.0 microsecond machine cycle is divided into four time slots of 250 ns each. The A, B, C, and D times are used for ALU operations and to:

- Synchronize cycle times with the 'gate A time' signal.
- Generate the 'mem store new time' signal.
- Detect a CCU clock error.

Clock Time Lights in Display A

If the DISPLAY/FUNCTION SELECT switch is in the STATUS position, display A bit lights 1.4, 1.5, 1.6, and 1.7 show the CCU clock times.

Note: *When the 3705-80 is running, the bit 1.7 light does not come on because the firing time is not long enough to heat the light. With the 3705-80 in clock step mode, the light does come on.*

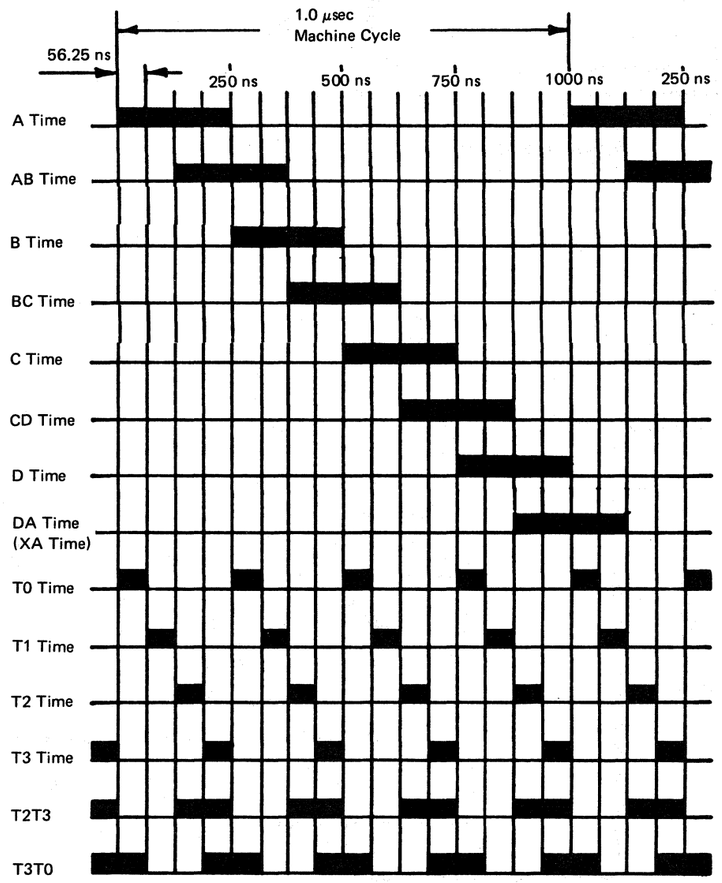
Cycle Time	*A*				*B*			
Clock Time	*T0*	*T1*	*T2*	*T3*	*T0*	*T1*	*T2*	*T3*
Bit 1.4 of Display A	0	0	0	0	0	0	0	0
Bit 1.5 of Display A	0	0	0	0	1	1	1	1
Bit 1.6 of Display A	0	0	1	1	0	0	1	1
Bit 1.7 of Display A	0	1	0	1	0	1	0	1

Cycle Time	*C*				*D*			
Clock Time	*T0*	*T1*	*T2*	*T3*	*T0*	*T1*	*T2*	*T3*
Bit 1.4 of Display A	1	1	1	1	1	1	1	1
Bit 1.5 of Display A	0	0	0	0	1	1	1	1
Bit 1.6 of Display A	0	0	1	1	0	0	1	1
Bit 1.7 of Display A	0	1	0	1	0	1	0	1

Note: *Lights indicate the clock time that was just completed.*

0 = Off
1 = On

3705-80 Storage



ALD Pages CC001 and CC006
Card Location 01A-B3R2

STORAGE PROTECTION

By comparing a three bit protect key with a three bit storage key, storage protection makes it possible to protect the contents of storage from an unauthorized attempt to address storage. Specifically, storage protection does not allow instruction fetching from unauthorized storage and does not allow data modification at an unauthorized address; however it does allow data loading from any storage location any time.

The protect keys are located in an 8 key address bit by 3 key address bit local storage area, and the storage keys are located in a 128 key address bit by 3 key address bit local storage area. One storage key is assigned to each 2,048 bytes of storage. The protect keys and storage keys are set by an Output X'73' instruction containing the respective key address. (For more information on the Output X'73' instruction, see page 6-880.)

To execute an instruction that does not modify storage, the protect key must be equal to the storage key. If the keys do not match, a protection exception L1 interrupt is set.

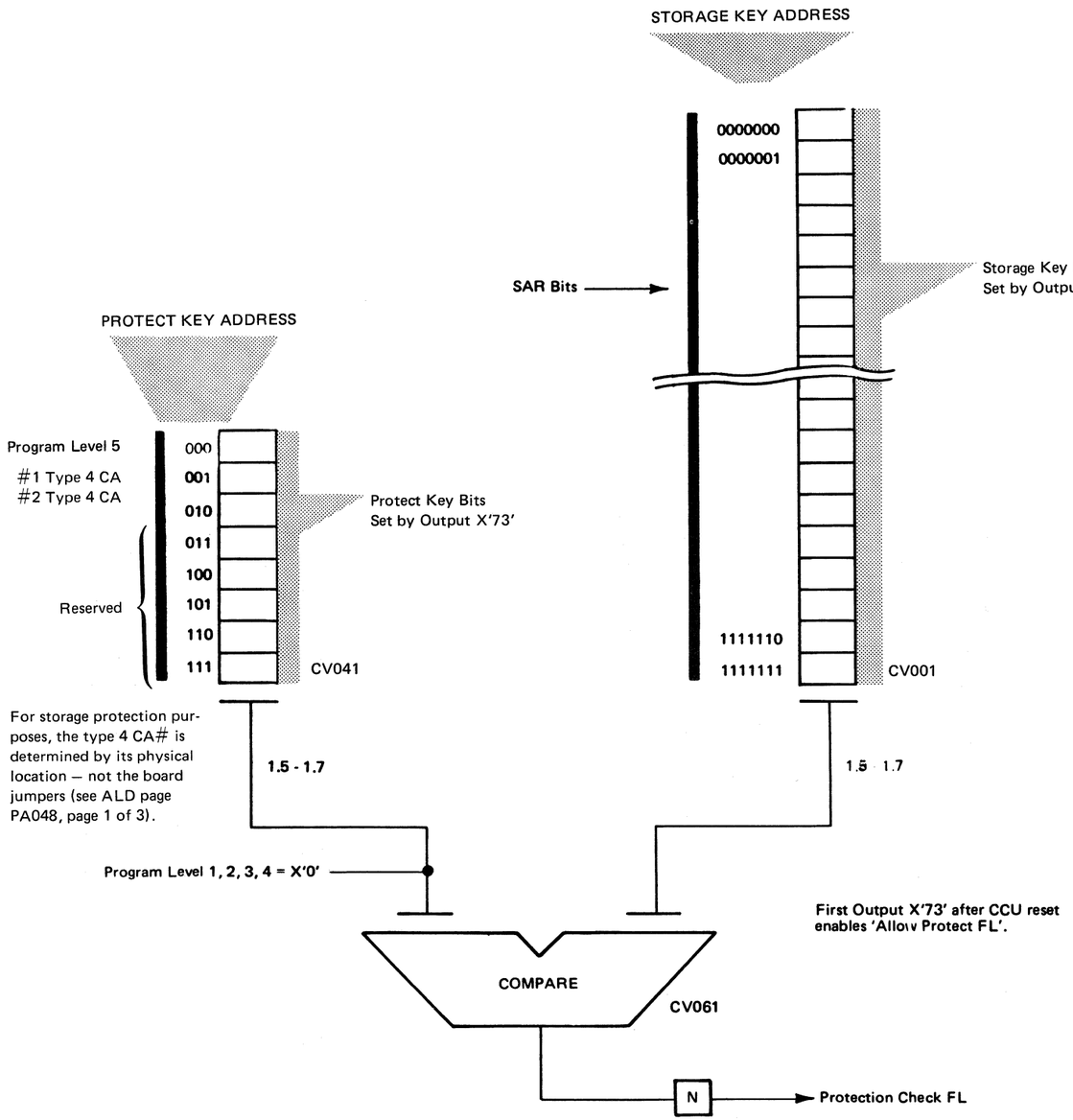
To modify a storage location, one of three conditions must be met:

- The protect key must be equal to the storage key.
- The protect key is X'0', that is, Program Level 1, 2, 3, or 4.
- The storage key is X'7', meaning unprotected storage.
- If none of the conditions are met, the keys are considered not matched, and a protection exception L1 interrupt is set.

When the CCU is reset, storage protection is disabled. Therefore, any instruction fetch is valid, and any attempt to modify storage is permitted. The first Output X'73' instruction executed after a reset enables storage protection. This instruction must set a storage key of X'0' at the key address that corresponds to the storage block where the instruction execution is taking place. Otherwise, a protection check occurs if the storage key is not already X'0'.

When the 3705-80 power is turned on, the bits in the settable protect keys and storage keys assume a random bit pattern. Each key must be initialized by an Output X'73' containing its key address and key type. Until each key is initialized, caution must be used in the control of program levels and I/O activity that may depend on storage protection.

A storage operation from the control panel cannot cause a storage protection check.



MACHINE CYCLES (PART 1 OF 2)

The 3705-80 uses six types of machine cycles: cycle steal 1, cycle steal 2, instruction 1, instruction 2, instruction 3, and idle.

Cycle Steal 1 (CS1) Cycle

CS1 cycles are used for type 4 CA cycle-steal operations. They are also used as maintenance cycles in the following control panel operations.

- ROS boostrap program load (see page 6-961).
- Display register. (See page 6-052.)
  a. In CS1A time, the address in the ADDRESS/DATA switches is placed in the Op register and in display register 1. The address is also placed in TAR if the 3705-80 is stopped.
  b. In CS1C time, the contents of the external register addressed by bits 0.1-0.3 and bits 1.0-1.3 of the Op register are placed in SDR if the external register is a general register.
  c. In CS1D time, the contents of the 'in bus' (for adapter register), of the 'indata bus' (for CCU register), or of SDR (for CCU general register) are placed in display register 2.
- Display storage. (See page 6-056.)
  a. In CS1A time, the address in the ADDRESS/DATA switches is placed in SAR and in display register 1. The address is also placed in TAR if the 3705-80 is stopped. The address in SAR is used to address storage.
  b. In CS1B time, the contents of the storage location addressed by SAR are placed in SDR.
  c. In CS1D time, the contents of SDR are placed in display register 2.
- START pushbutton operations. (See page 6-069.)
  a. In CS1A time, the address in TAR is placed in SAR and in display register 1.
  b. In CS1B time, the contents of the Z bus are placed in SDR. (This occurs by default and has no effect on the start cycle or on the following cycle.)
  c. In CS1D time, the address in the active IAR is placed in TAR and in display register 2.
- Storing in a register. (See page 6-054.)
  a. In CS1A time, the contents of TAR are placed in display register 1. (TAR should contain a register address.)
  b. In CS1C time, the data in the ADDRESS/DATA switches is placed in SDR and on the 'out bus' to the adapters.
  c. In CS1D time, the contents of SDR are placed in display register 2. If the register designated by the set address and display register procedure is a CCU register, the contents of SDR are placed in the register.
- Storing in storage. (See page 6-057.)
  a. In CS1A time, the address in TAR is placed in SAR. The address in TAR is then incremented by 2, and the new address is placed in TAR and in display register 1.
  b. In CS1B time, the data in the ADDRESS/DATA switches is placed in SDR.
  c. In CS1D time, the contents of SDR are placed in display register 2.
- Storage scanning. (See page 6-063.)
  a. In CS1A time, the address in TAR is placed in SAR. The address in TAR is then incremented by 2, and the new address is placed in TAR and in display register 1. The address in SAR is used to address storage.
  b. In CS1B time, the contents of the storage location addressed by SAR are placed in SDR.
  c. In CS1D time, the contents of SDR are placed in display register 2.
- Single address scanning. (See page 6-067.)
  a. In CS1A time, the contents of TAR are placed in display register 1. The address in SAR is used to address storage. (The first cycle does not address the location in the ADDRESS/DATA switches.)
  b. In CS1B time, the contents of the storage location addressed by SAR are placed in SDR.
  c. In CS1C time, the address in the ADDRESS/DATA switches is placed in TAR.
  d. In CS1D time, the contents of SDR are placed in display register 2. The contents of TAR are placed in SAR.
- Storage test pattern (page 6-060) and single address test pattern (page 6-064.)
  a. In CS1A time, the contents of TAR are placed in display register 1.
  b. In CS1B time, the data in the ADDRESS/DATA switches is placed in SDR.
  c. In CS1C time, the contents of SDR are stored in the location addressed by SAR.
  d. In CS1D time, the contents of SDR are placed in display register 2.

CS1 cycles can occur between instruction cycles because CS1 cycles have higher priority.

Cycle Steal 2 (CS2) Cycle

A CS2 cycle is required after each CS1 cycle for the following control panel operations.

- Storing data in a storage location
  a. In CS2A time, the contents of TAR are placed in display register 1 and in SAR. The address in SAR is used to address storage.
  b. In CS2B time, the contents of the storage location addressed by SAR (original +2) are read into SDR.
  c. In CS2D time, the contents of SDR are placed in display register 2.
- Storage test pattern
  a. In CS2A time, the address in TAR is incremented by 2 and placed in TAR and in display register 1. The contents of SAR are used to address storage.
  b. In CS2B time, the contents of the storage location addressed by SAR are placed in SDR.
  c. In CS2D time, the contents of SDR are placed in display register 2.
- Single address test pattern
  a. In CS2A time, the address in TAR is placed in TAR and in display register 1. (The address is not incremented.)
  b. In CS2B time, the contents of SDR are stored at the storage location addressed by SAR.
  c. In CS2D time, the contents of SDR are placed in display register 2.

Instruction 1 (I1) Cycle

An I1 cycle is used as the first machine cycle taken to execute an instruction. The first 16 bits of the instruction are placed in the Op register. Most instructions require only an I1 cycle for execution. Instructions that require additional machine cycles for execution are listed in the next paragraph.

Instruction 2 (I2) Cycle

The I2 cycle is used as the second machine cycle for the following instructions.

- 'Insert character and count' (ICT)
- 'Store character and count' (STCT)
- 'Insert character' (IC)
- 'Store character' (STC)
- 'Load' (L)
- 'Store' (ST)
- 'Branch and link register' (BALR)
- 'Branch and link' (BAL)
- 'Load address' (LA)

Instruction 3 (I3) Cycle

An I3 cycle is required as the third machine cycle for the following instructions.

- 'Load' (L)
- 'Store' (ST)

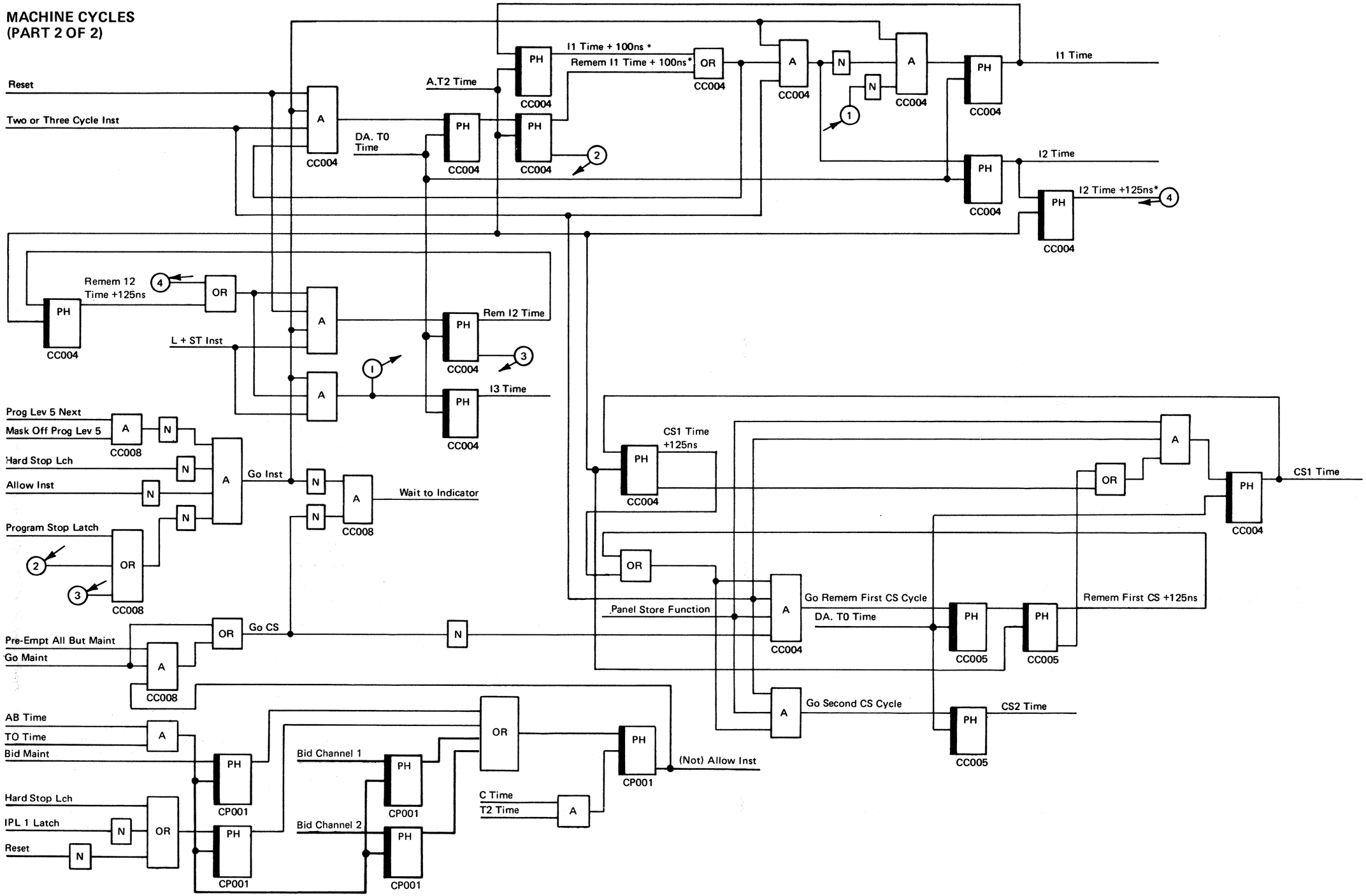
Idle Cycle

An idle cycle occurs whenever CS1, CS2, I1, I2, or I3 cycles are not being executed. When an idle cycle occurs, the WAIT light turns on, and the 3705-80 is in the wait state. The WAIT light turns off when a CS1, CS2, I1, I2, or I3 cycle is executed.

Idle cycles are those cycle time slots that occur:

(1) When the CCU is hardstopped and no panel functions are being used.
(2) When the CCU is program stopped, no panel functions are being used, and no adapter is cycle-stealing.
(3) During the first cycle of a START pushbutton operation (also known as 'dummy' cycles).
(4) After an exit instruction when level 5 is masked off and no bids for any level are pending, until an interrupt occurs.

MACHINE CYCLES (PART 2 OF 2)



Display Register

Procedure on page 1-120

CS1A time:
- Places the register address from the ADDRESS/DATA switches into the Op Register and Display Reg 1.
- Places the address into TAR if the 3705-80 is stopped.

Address/Data Sw

X Gate Hex SW B and D (CS004)
X Gate CCU Indata to Y Bus (CS004)
X Gate Y Bus to B Reg (CS004)
X T0 +T1 Time Set A-B Reg (CS004)

B Register — DF002 DG002

ALU — B Reg Direct

DF008 DG008

Z Register — DF974 DG974

X Set DR1 (CS007) — Display Register 1 — DF003 DG003
X Gate Displ Reg I to Ind (CU001) — Display A — AP011 AP012

X Set Op Reg (CS007) — Op Register — DN001

X Set TAR (CS007) (If Stopped) — TAR — DF971 DG971

I/O Reg Address Bus to all external registers (CCU and adapters)

CS

CS1B

No Action

CS1C time:
- Places the contents of a general register into SDR if the Op Reg addresses X'00'-X'1F'

General Register — Specified by bits 0.1-0.3 and 1.0-1.3 of Op Register

X T0+T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU — B Reg Direct

DF008 DG008

Z Register — DF974 DG974

X Gate Z Bus Byte to M Bus (CS005)
X Set SDR Byte (CS007) (Display Push button)

SDR — DN001

A — To Next Page

CS1C

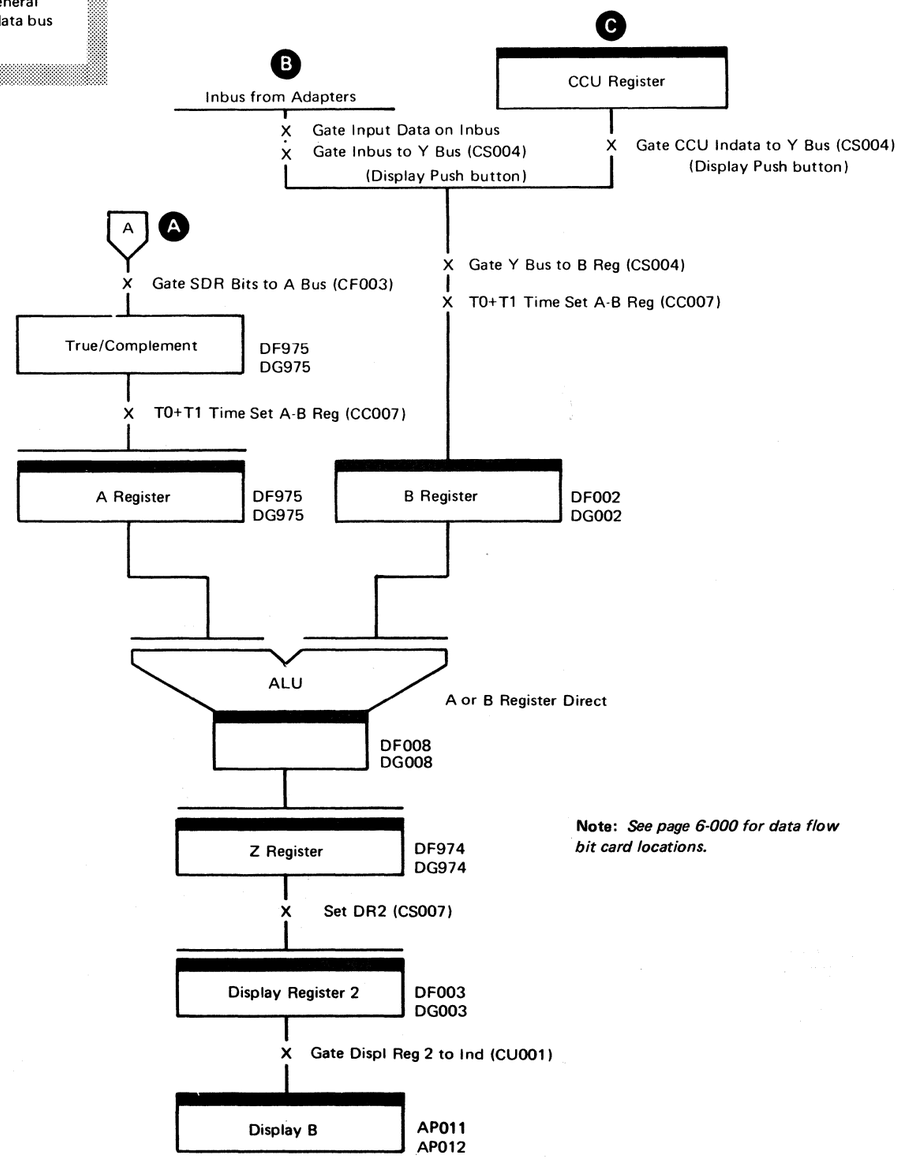
To Next Page

Note: *See Page 6-000 for data flow bit card locations.*

From Preceding Page

One of the following occurs during CS1D time:

- **A** If the addressed register is a general register, the contents of SDR (contents of the register) are placed in Display Register 2.
- **B** If the addressed register is an adapter register, the contents of the register are gated on the Inbus and placed in Display Register 2.
- **C** If the addressed register is a CCU register (other than a general register), the contents of the register are gated on the Indata bus and placed in Display Register 2.



Note: *See page 6-000 for data flow bit card locations.*

CS1D

End of Cycle

Store Register (3705-80 Stopped)

Procedure on page 1-120

CS1A time Places contents of TAR into Display Register 1.

Op Reg and TAR should contain the register address entered in the SET ADDRESS/DISPLAY push button operation. The address in the Op register is placed on the Op Reg I/O Address Bus to all external Registers (CCU and adapter.)

CS1A

TAR — DF971 DG971

X Gate TAR to Y Bus((CS004)

X T0+T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU — B Reg Direct

DF008 DG008

Z Register — DF974 DG974

X Set DR1 (CS007)

Display Register 1 — DF003 DG003

X Gate Displ Reg 1 to Ind (CU001)

Display A — AP011 AP012

CS1B

No Action

To Next Column

CS1C

CS1C time:
- Places data from ADDRESS/DATA switches into SDR.
- Places data from ADDRESS/DATA switches on 'out bus' to adapters

Address/Data SW

X Gate Hex Sw A and C and E (CS004)

X Gate Hex Sw B and D (CS004)

X Gate CCU Indata to Y Bus (CS004)

X Gate Y Bus to B Reg (CS004)

X T0+T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU — B Reg Direct

DF008 DG008

Note: *See page 6-000 for data flow bit card locations.*

Z Register — DF974 DG974

X Set SDR Byte (CS007)

X Sample Output Data (CQ001)

Out bus to Adapter

SDR — DN001

Perform output function specified by value in data switches during CD time (summarized on page 6-151)

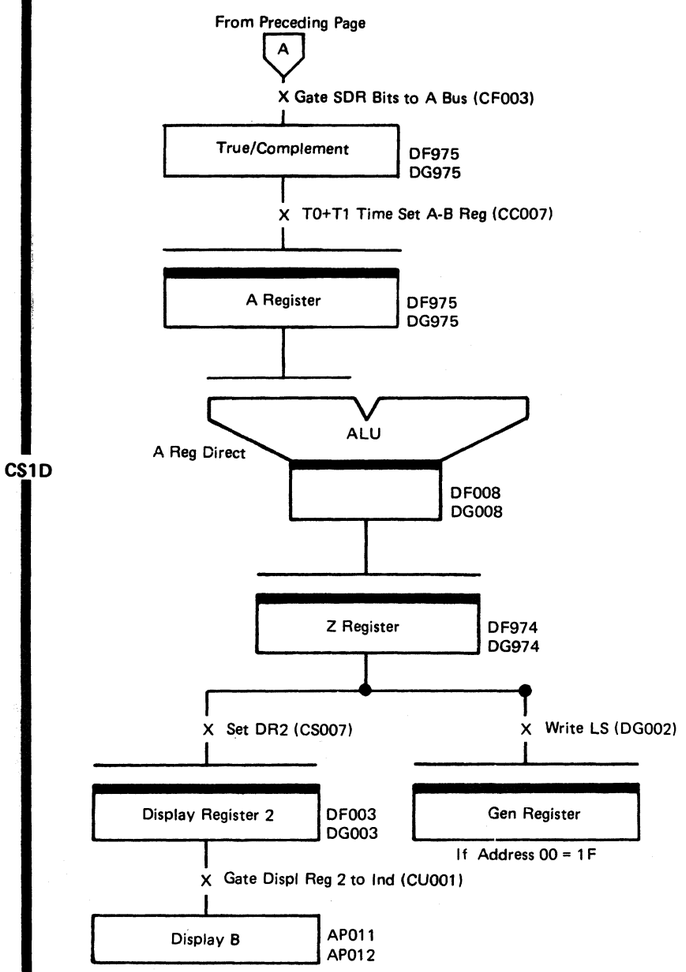
A

To Next Page

To Next Page

From Preceding Page

CS1D time:
- **Places the contents of SDR into Display Register 2.**
- **Places the contents of SDR into the Register designated by TAR.**



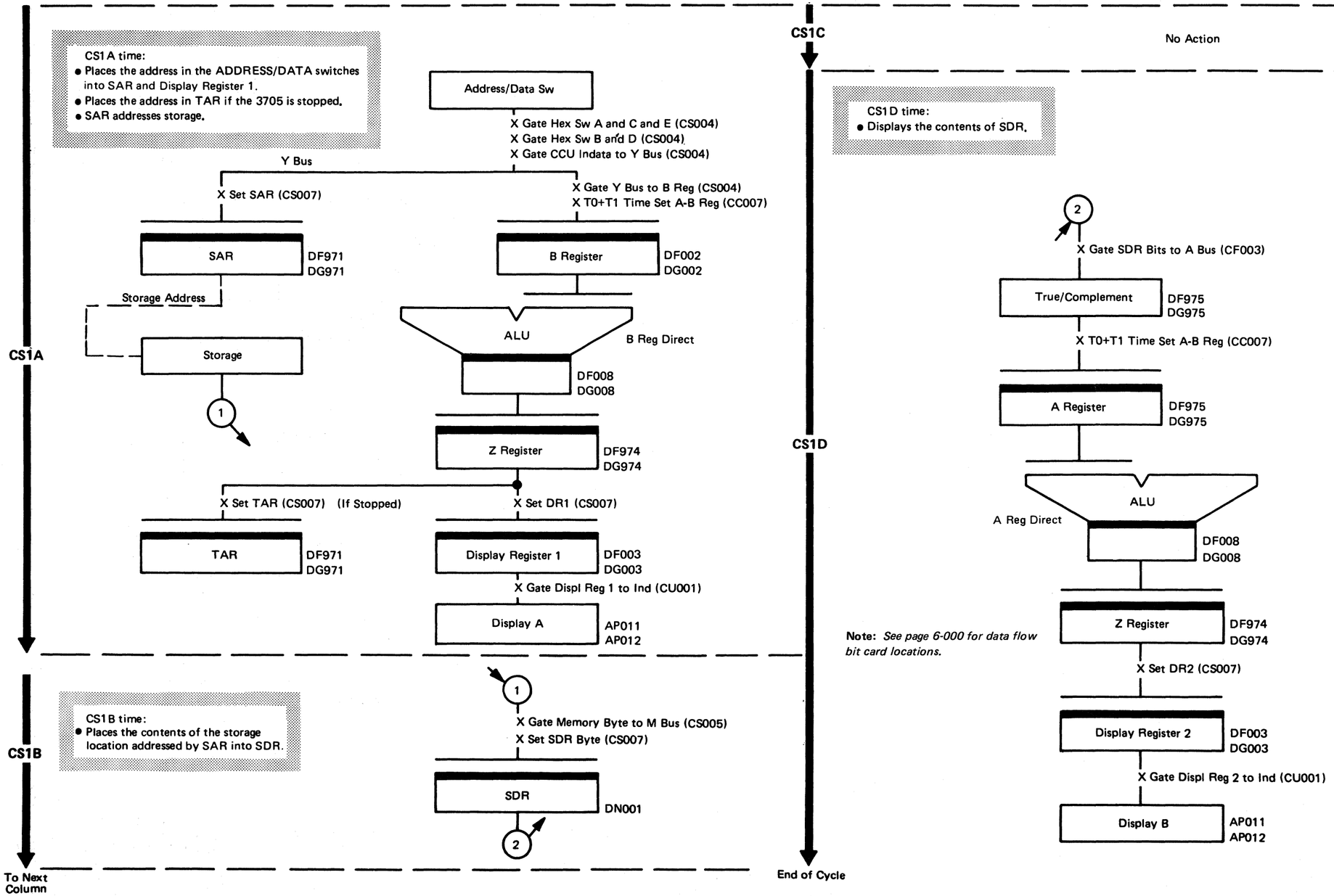
CS1D

Note: *See page 6-000 for data flow bit card locations.*

End of Cycle

Display Storage

Procedure on page 1-120



Note: *See page 6-000 for data flow bit card locations.*

Storing Data in a Storage Location with the 3705-80 Stopped (Part 1 of 3)

Procedure on page 1-130

CS1A time:
- Places the address from TAR into SAR.
- Increments the address in TAR by 2.
- Places the new address into TAR and Display Register 1.

Constant + 2

X Force Constant 0002 (CF001)

True/Complement — DF975 DG975

X T0+T1 Time Set A-B Reg (CC007)

A Register — DF975 DG975

TAR — DF971 DG971

X Gate TAR to Y Bus (CS004)
X Gate Y Bus to B Reg (CS004)
X T0+T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

X Set SAR (CS007)

SAR — DF971 DG971

ALU — Add Operation

DF008 DG008

Z Register — DF974 DG974

X Set TAR (CS007)

TAR — DF971 DG971

(1)

X Set DR1 (CS007)

Display Register 1 — DF003 DG003

X Gate Displ Reg 1 to Ind (CU001)

Display A — AP011 AP012

CS1A

To Next Column

CS1B time:
- Places the data in the ADDRESS/DATA switches into SDR.

ADDRESS/DATA SW

X Gate Hex Sw A and C and E (CS004)
X Gate Hex Sw B and D (CS004)
X Gate CCU Indata to Y Bus (CS004)
X Gate Y Bus to B Reg (CS004)
X T0+T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU — B Reg Direct

DF008 DG008

Z Register — DF974 DG974

X Gate Z Bus Bytes to M Bus (CS005)
X Set SDR Bytes 0, 1 (CS007)

SDR — DN001

Bytes 0, 1

(A)

To Pages 6-058

(1)

CS1B

Note: *See page 6-000 for data flow bit card locations.*

CS1C

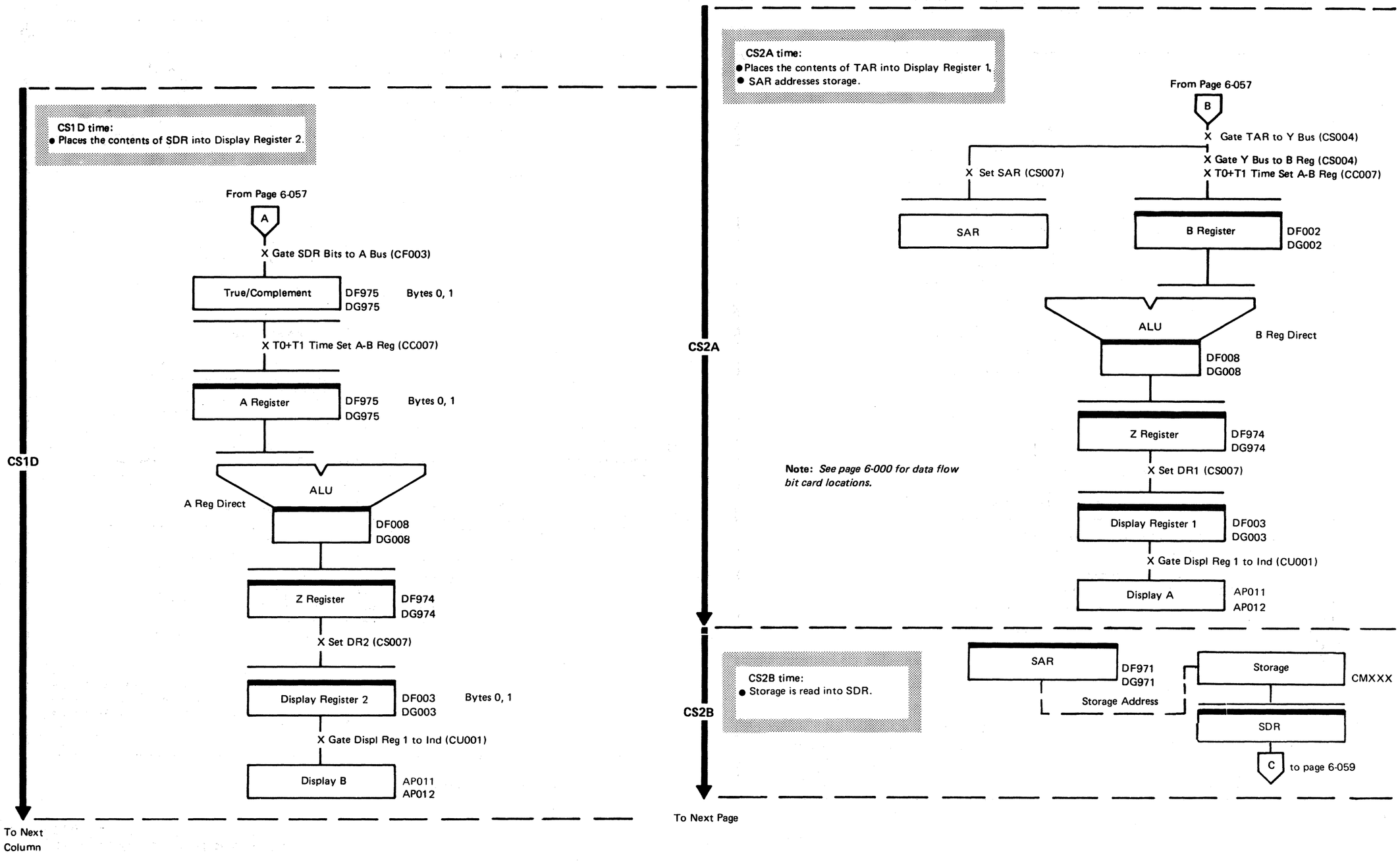
The write cycle begins. The contents of the SDR are stored in the location addressed by SAR.

(B)

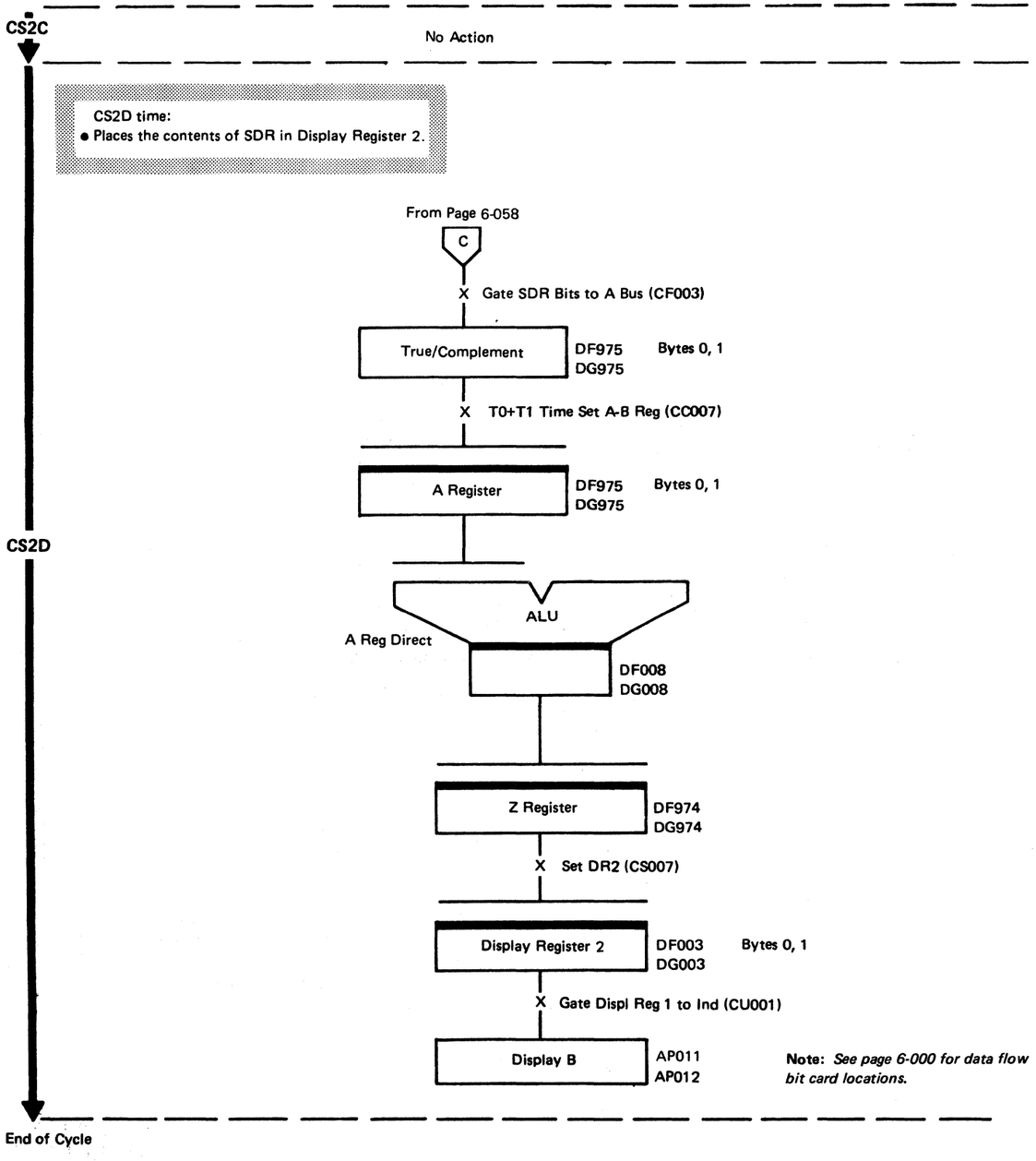
To Next Page

To Next Page

Storing Data in a Storage Location with the 3705-80 Stopped (Part 2 of 3)



Storing Data in a Storage Location with the 3705-80 Stopped (Part 3 of 3)



Storage Test Pattern (Part 1 of 3)

Procedure on page 1-130

CS1A time:
- Places the contents of TAR into SAR.
- Places the contents of TAR into Display Register 1.

CS1A

TAR — DF971 DG971

X Gate TAR to Y Bus (CS004)
X Gate Y Bus to B Reg (CS004)
X T0+T1 Time Set A-B Reg (CC007)

X Set SAR (CS007)

B Register — DF002 DG002

SAR — DF971 DG971

ALU — B Reg Direct

Storage Address

DF008 DG008

Storage — CM002 CM003

Z Register — DF974 DG974

X Set DR1 (CS007)

Display Reg 1 — DF003 DG003

X Gate Displ Reg 1 to Ind (CU001)

Display A — AP011 AP012

To Next Column

CS1B time:
- Places data bytes 0 and 1 of the ADDRESS/DATA switches into SDR.

Note: *See page 6-000 for data flow bit card locations.*

CS1B

ADDRESS/DATA SW

X Gate Hex Sw A and C and E (CS004)
X Gate Hex Sw B and D (CS004)
X Gate CCU Indat to Y Bus (CS004)
X T0+T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU — B Reg Direct

DF008 DG008

Z Register — DF974 DG974

X Set SDR Byte (CS007)

Bytes 0, 1

SDR — DN001 Bytes 0, 1

A

To Pages 6-061 and 6-062

CS1C time:
- Places the contents of SDR into the storage location addressed by SAR.

CS1C

SDR — DN003

SAR — DF971 DG971

Storage Address

Storage — CMXXX

To Next Page

Storage Test Pattern
(Part 2 of 3)

From Preceding Page

CS1D time:
- Places bytes 0 and 1 of SDR into Display Register 2.

A — From page 6-060

X Gate SDR Bits to A Bus (CF003)

True/Complement — DF975 DG975

X T0+T1 Time Set A-B Reg (CC007)

A Register — DF975 DG975

ALU — A Reg Direct

DF008 DG008

Z Register — DF974 DG974

X Set DR2 (CS007)

Display Register 2 — DF003 DG003

X Gate Displ Reg 2 to Ind (CU001)

Display B — AP011 AP012

CS1D

To Next Column

CS2A

CS2A time:
- Increments the address in TAR by 2.
- Places the new address into TAR and Display Register 2.
- Places the contents of TAR into SAR.

Constant + 2

X Force Constant 0002 (CF001)

True/Complement — DF975 DG975

X T0+T1 Time Set A-B Reg (CC007)

TAR — DF971 DG971

X Gate TAR to Y Bus (CS004)
X Gate Y Bus to B Reg (CS004)
X T0+T1 Time Set A-B Reg (CC007)

A Register — DF975 DG975

B Register — DF002 DG002

X Set SAR (CS007)

ALU — Add

DF008 DG008

SAR — DF971 DG971

Storage Address

Storage

Z Register — DF974 DG974

X Set DR1 (CS007)

X Set TAR (CS007)

Disp Reg 2 — DF003 DG003

TAR — DF971 DG971

X Gate Displ Reg 1 to Ind (CU001)

Display B — AP011 AP012

CS2B

CS2B time:
- Places the contents of the storage location addressed by SAR into SDR.

Storage Address

SAR — DF971 DG971

Storage — CMXXX

X Set SDR (CS007)

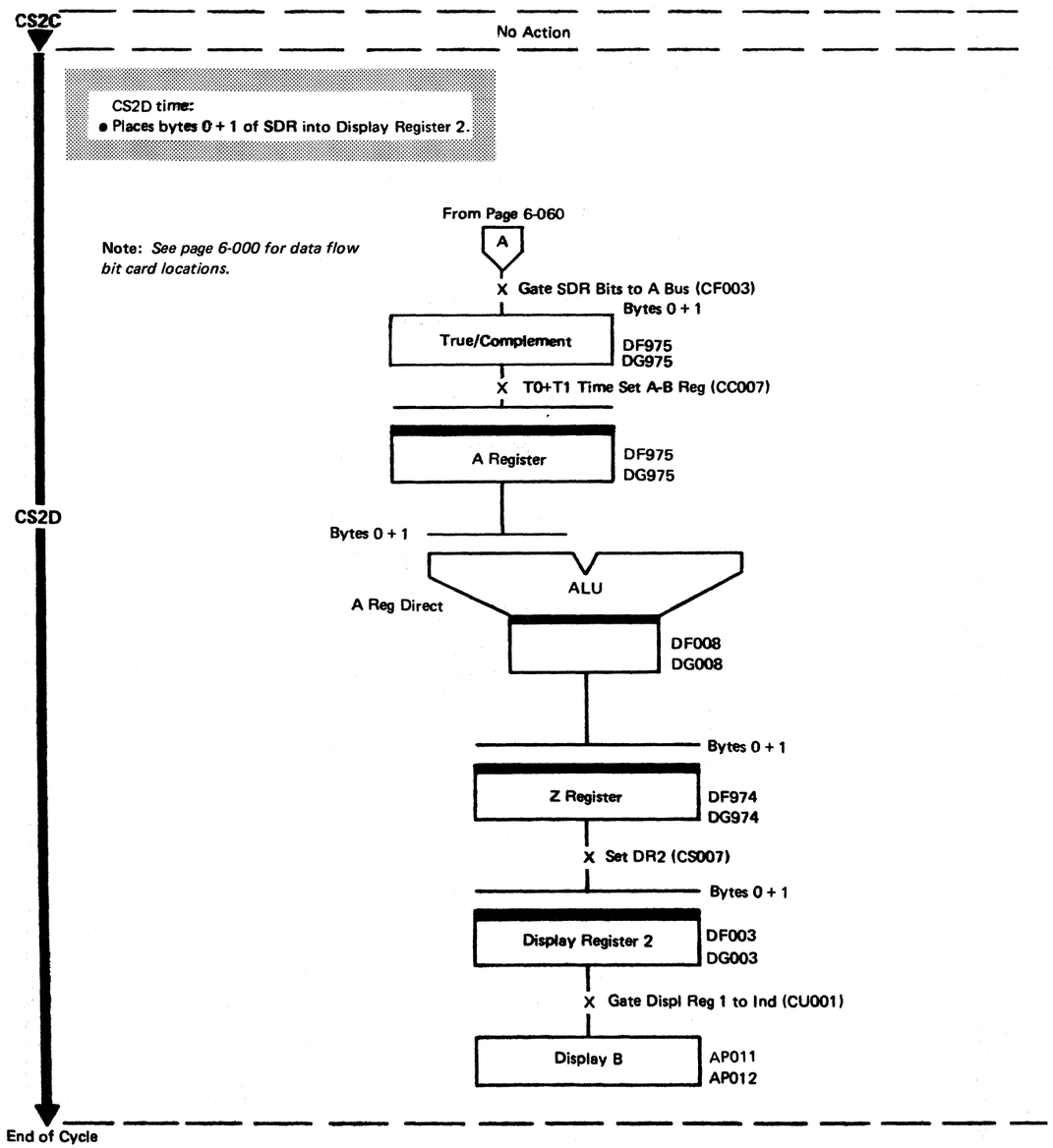
SDR — DN003

To Next Page

Note: *See page 6-000 for data flow bit card locations.*

Storage Test Pattern
(Part 3 of 3)

From Preceding Page



Storage Scanning

Procedure on page 1-130

CS1A time:
- Places address from TAR into SAR.
- Increments TAR by 2.
- Places new address into Display Register 1 and TAR.
- SAR addresses storage.

CS1B time:
- Places the contents of the storage location addressed by SAR into SDR.

CS1D time:
- Places contents of SDR into Display Register 2.

CS1A

CS1B

CS1C

CS1D

TAR DF971 DG971

Constant +2

X Force Constant 0002 (CF001)

True/Complement

X T0+T1 Time Set A-B Reg (CC007)

X Gate TAR to Y Bus (CS004)

X T0+T1 Time Set A-B Reg (CC007)

X Set SAR (CS007)

A Register DF975 DG975

B Register DF002 DG002

SAR DF971 DG971

Storage Address

ALU — Add

DF008 DG008

Storage

CM002 CM003

Z Register DF974 DG974

1

X Set DR1 (CS007)

X Set TAR (CS007)

Display Register 1 DF003 DG003

TAR DF971 DG971

X Gate Displ Reg 1 to Indicator (CU001)

Display A AP011 AP012

To Next Column

1

X Gate Memory Byte to M bus (CS005)

X Set SDR byte (CS007)

SDR DN001

2

No action

2

X Gate SDR bits to A bus (CF003)

True/Complement

X T0+T1 time Set A-B Reg (CC007)

A Register DF975 DG975

A Reg Direct — ALU

DF008 DG008

Z Register DF974 DG974

X Set Displ Reg 1 (CS007)

Display Register 2 DF003 DG003

X Gate Displ Reg 2 to Indicator (CU001)

Display B

Note: *See page 6-000 for data flow bit card locations.*

End of Cycle

Single Address Test Pattern
(Part 1 of 3)

Procedure on page 1-130

CS1A time:
- Places the contents of TAR into Display Register 1.
- Places the contents of TAR into SAR.

TAR — DF971 DG971

X Gate TAR to Y Bus (CS004)
X Gate Y Bus to B Reg (CS004)
X T0+T1 Time Set A-B Reg (CC007)

X Set SAR (CS007)

B Register — DF002 DG002

SAR — DF971 DG971

Storage Address

ALU — B Reg Direct

DF008 DG008

Storage — CMXXX

Z Register — DF974 DG974

X Set DR1 (CS007)

Display Register 1 — DF003 DG003

X Gate Displ Reg 1 to Ind (CU001)

Display A — AP011 AP012

To Next Column

CS1B

CS1B time:
- Places the data bytes 0 and 1 of the ADDRESS/DATA switches into SDR.

Note: *See page 6-000 for data flow bit card locations.*

ADDRESS/DATA SW

X Gate Hex Sw A and C and E (CS004)
X Gate Hex Sw B and D (CS004)
X Gate CCU Indata to Y Bus (CS004)
X T0+T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU — B Reg Direct

DF008 DG008

Z Register — DF974 DG974

X Set SDR Byte (CS007)

Bytes 0, 1

SDR — DN001

Bytes 0,1

A

CS1C time:
- Places the contents of SDR into the storage location addressed by SAR.

CS1C

SDR — DN003

SAR — DF971 DG971

Storage Address

Storage — CMXXX

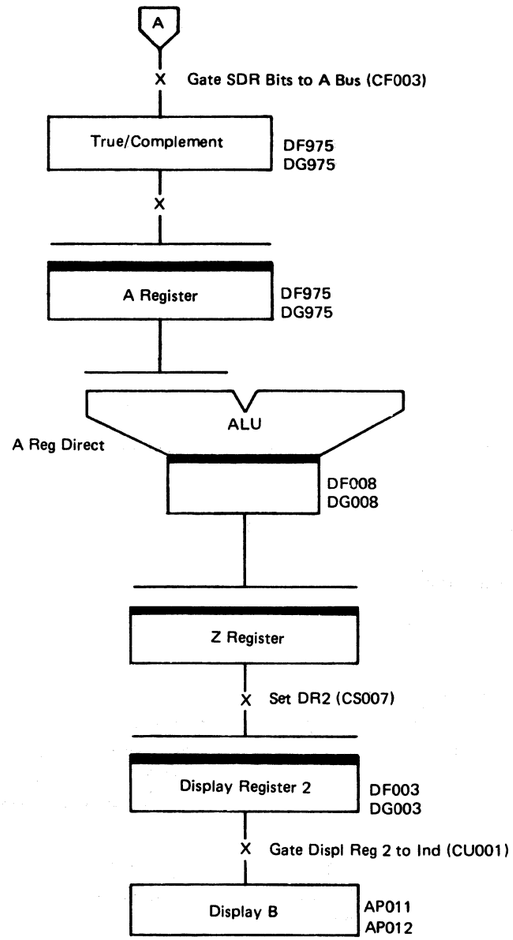
To Next Page

Single Address Test Pattern
(Part 2 of 3)

From Preceding Page

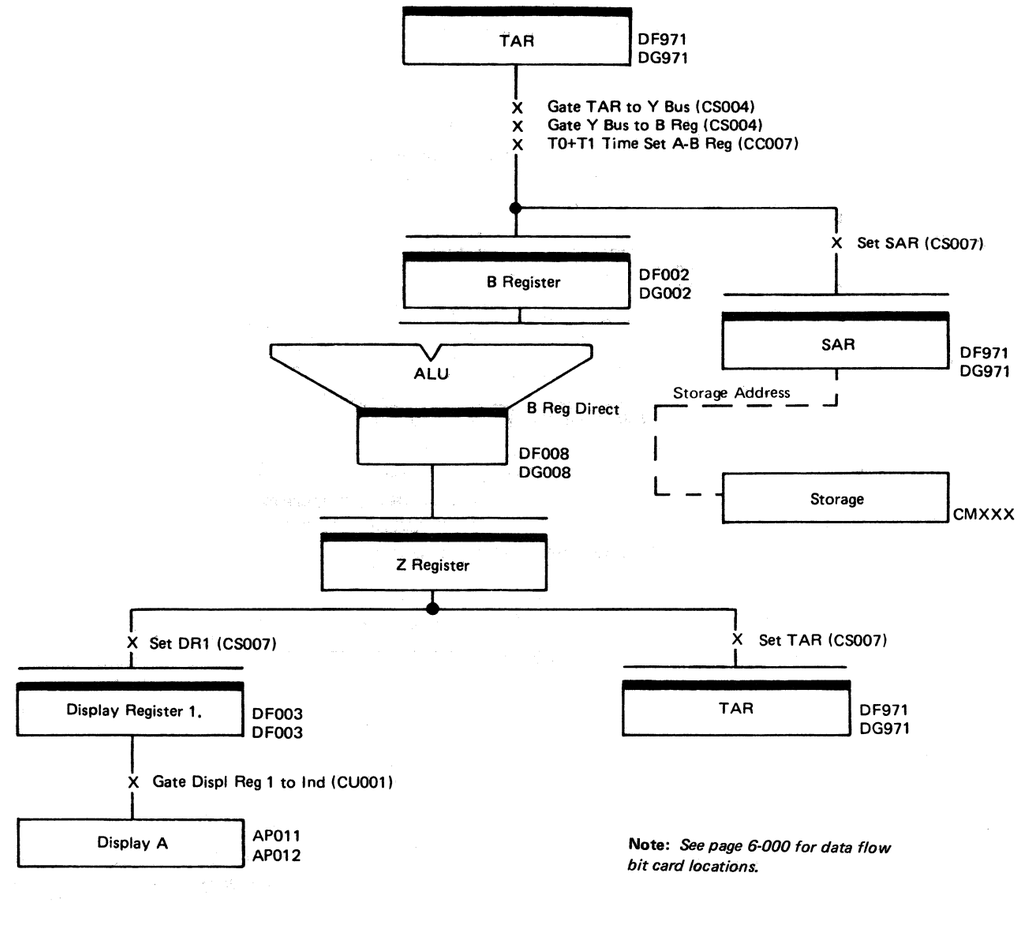
CS1D

CS1D time:
- Places bytes 0 and 1 of SDR into Display Register 2.



CS2A

CS2A time:
- Places the address from TAR into TAR and Display Register 1.
- Places the address from TAR into SAR.



Note: *See page 6-000 for data flow bit card locations.*

To Next Column

Single Address Test Pattern
(Part 3 of 3)

From Preceding Page

CS2B

CS2B time:
- Places the contents of the storage location addressed by SAR in SDR.

SAR — DF971, DG971

Storage Address

Storage — CMXXX

X Set SDR (CS007)

SDR — DN003

Note: Hard stop overridden.

CS2C

No Action

To Next Column

CS2D

CS2D time:
- Places Bytes 0 and 1 of SDR into Display Register 2.

From Page 6-064

A

True/Complement — Bytes 0, 1 — DF975, DG975

X Gate SDR Bits to A Bus (CF003)

A Register — DF975, DG975

X T0+T1 Time Set A-B Reg (CC007)

ALU

A Reg Direct

DF008, DG008

Bytes 0, 1

Z Register

X Set DS2 (CS007)

Bytes 0, 1

Display Register 2 — DF003, DG003

X Gate Displ Reg 2 to Ind (CU001)

Display B — AP011, AP012

End of Cycle

Note: *See page 6-000 for data flow bit card locations.*

Single Address Scanning
(Part 1 of 2)

Procedure on page 1-130

CS1A

CS1A time:
- Places the address from TAR into Display Register 1.
- SAR addresses storage.

TAR — DF971, DG971

X Gate TAR to Y Bus (CS004)
X Gate Y Bus to B Reg (CS004)
X T0+T1 Time Set A-B Reg (CC007)

B Register — DF002, DG002

ALU — B Reg Direct

DF008, DG008

Z Register — DF974, DG974

X Set DR1 (CS007)

Display Register 1 — DF003, DG003

X Gate Displ Reg 1 to Ind (CU001)

Display A — AP011, AP012

X Set SAR (CS007)
DT3, AT0

SAR — DF971, DG971

Storage Address

Storage — CM002, CM003

(1)

CS1B

CS1B time:
- Places the contents of the storage location addressed by SAR in SDR.

(1)

X Gate Memory Byte to M Bus (CS005)
X Set SDR Byte (CS007)

SDR — DN001

(2)

Note: Hard stop overridden.

To Next Column

CS1C

CS1C time:
- Places the storage address from the ADDRESS/DATA switches into TAR.

(2)

ADDRESS/DATA SW

X Gate Hex Sw A and C and E (CS004)
X Gate Hex Sw B and D (CS004)
X Gate Y Bus to B Reg (CS004)
X Gate CCU Indata to Y Bus (CS004)
X T0+T1 Time Set A-B Reg (CC007)

B Register — DF002, DG002

ALU — B Reg Direct

DF008, DG008

Z Register — DF974, DG974

X Set TAR (CS007)

TAR — DF971, DG971

(A)

To Next Page

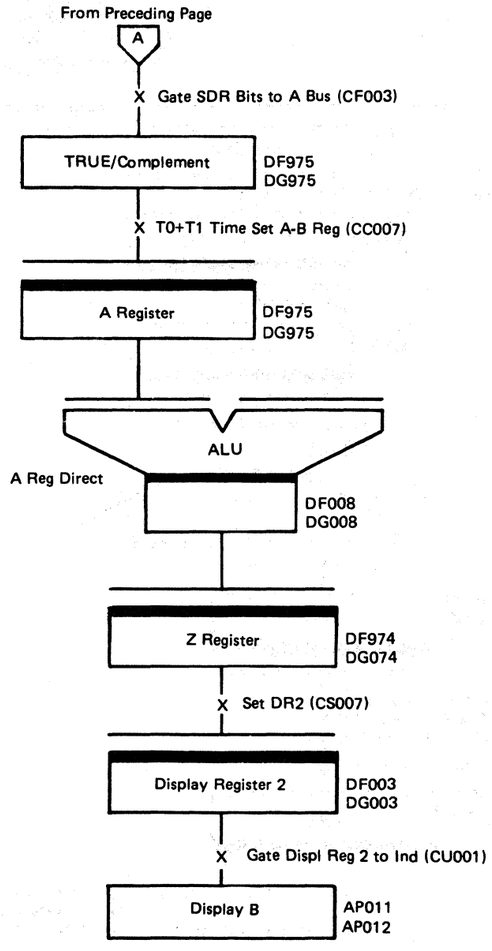
Note: *See page 6-000 for data flow bit card locations.*

To Next Page

Single Address Scanning
(Part 2 of 2)

From Preceding Page

CS1D time:
- Places the contents of SDR into Display Register 2.

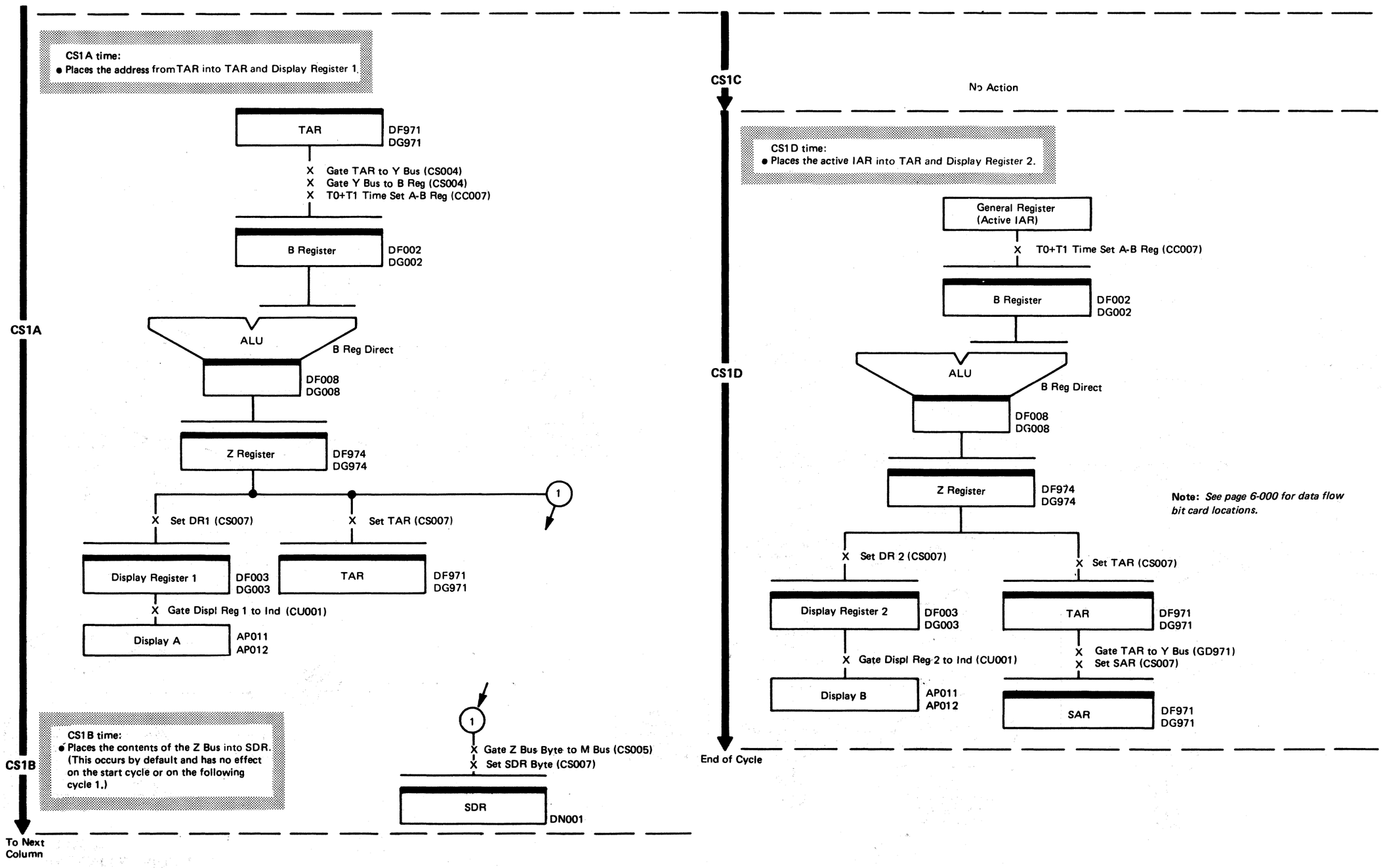


CS1D

End of Cycle

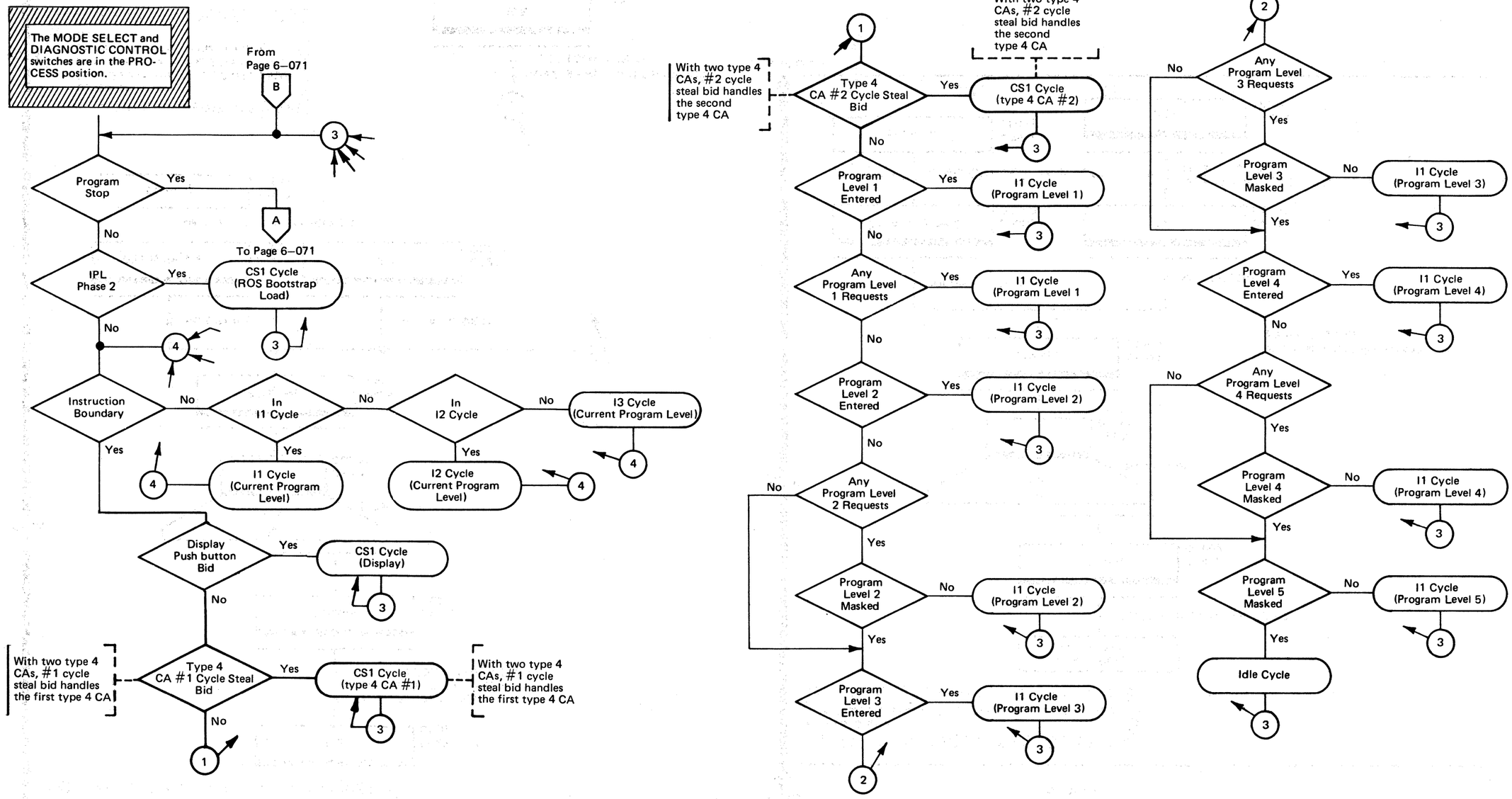
Note: *See page 6-000 for data flow bit card locations.*

Start Pushbutton Operations

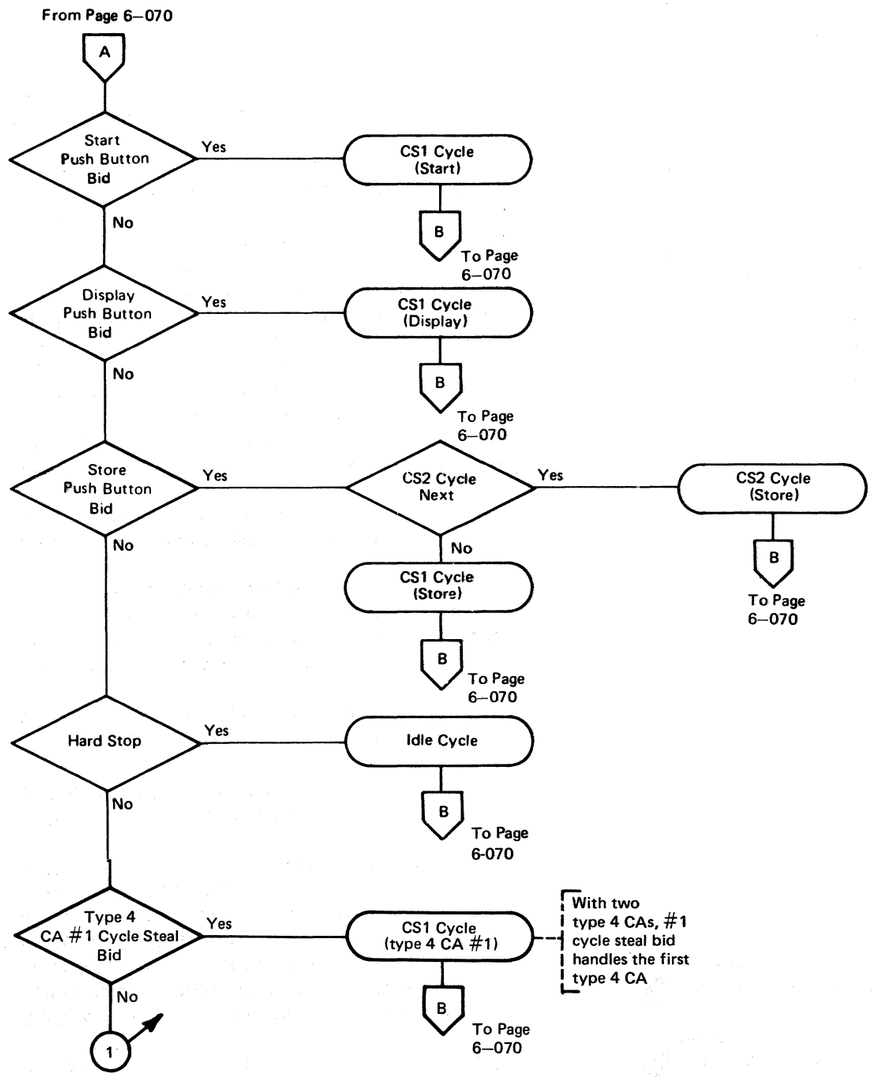


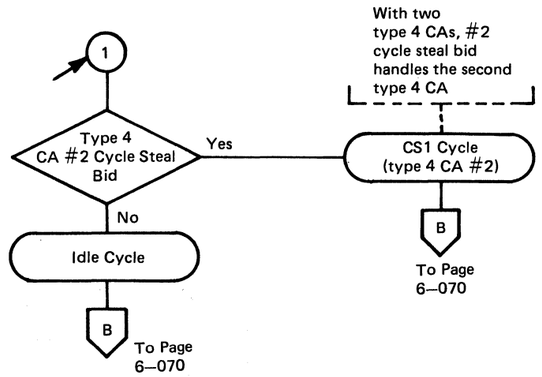
Note: *See page 6-000 for data flow bit card locations.*

MACHINE CYCLE PRIORITIES (PART 1 OF 2)



MACHINE CYCLE PRIORITIES (PART 2 OF 2)





Changing Machine Priorities (Masking Program Levels)

WARNING
Be careful about masking program levels because it disrupts the normal priority structure. It could cause overrun conditions or delay hardware error indications.

Output X'7E' Set Mask Bits (page 6-950) and Output X'7F' Reset Mask Bits (page 6-960) can change the priority structure if they are executed with certain bits on.

When a program level is masked, machine cycles cannot be used for instruction execution at that program level. If level 2, 3, or 4 is active, instruction execution at that program level is allowed to finish before a mask of that level is effective. Only adapter interrupts can be masked in program level 5.

Note: *The CE can execute Outputs X'7E' and X'7F' from the control panel. (See page 1-160.)*

Refresh Storage Cycles

The storage unit in the 3705-80 is dynamic, meaning that the information in storage needs to be renewed or refreshed periodically to maintain validity. The CCU has a basic machine and storage cycle of 1 us. A read storage operation occurs during the first 500ns and a write storage operation, if required, occurs during the second 500ns of a storage cycle. If a write operation is not required, a refresh storage operation can occur during the second 500ns instead of a write operation. During normal 3705-80 operation, a refresh storage operation occurs on an average of one every 8 us or one every 8 machine cycles.

PROGRAM LEVEL PRIORITIES AND INTERRUPTS (PART 1 OF 3)

Interrupts are caused by adapters or programs initiating hardware-forced branches from lower-priority program levels to higher program levels. The interrupts occur because of:

- Hardware errors
- Hardware service requests
- Program errors
- Program service requests

Machine cycle priorities determine when a level n interrupt can occur. A level n interrupt can occur when all of the following conditions are met:

- No cycle-steal requests are present
- The program is at the end of an instruction execution (instruction boundary).
- No interrupt requests at a higher priority level are present.
- Program level n is not masked.
- Program level n is not active.

Note: *Level 1 interrupts in program level 1 cause a re-IPL the first time they occur and a hard stop the second time.*

When a level n interrupt occurs, the 'level n interrupt entered' latch sets. Instruction execution at the interrupted level is temporarily suspended until instruction execution is completed at the higher priority level.

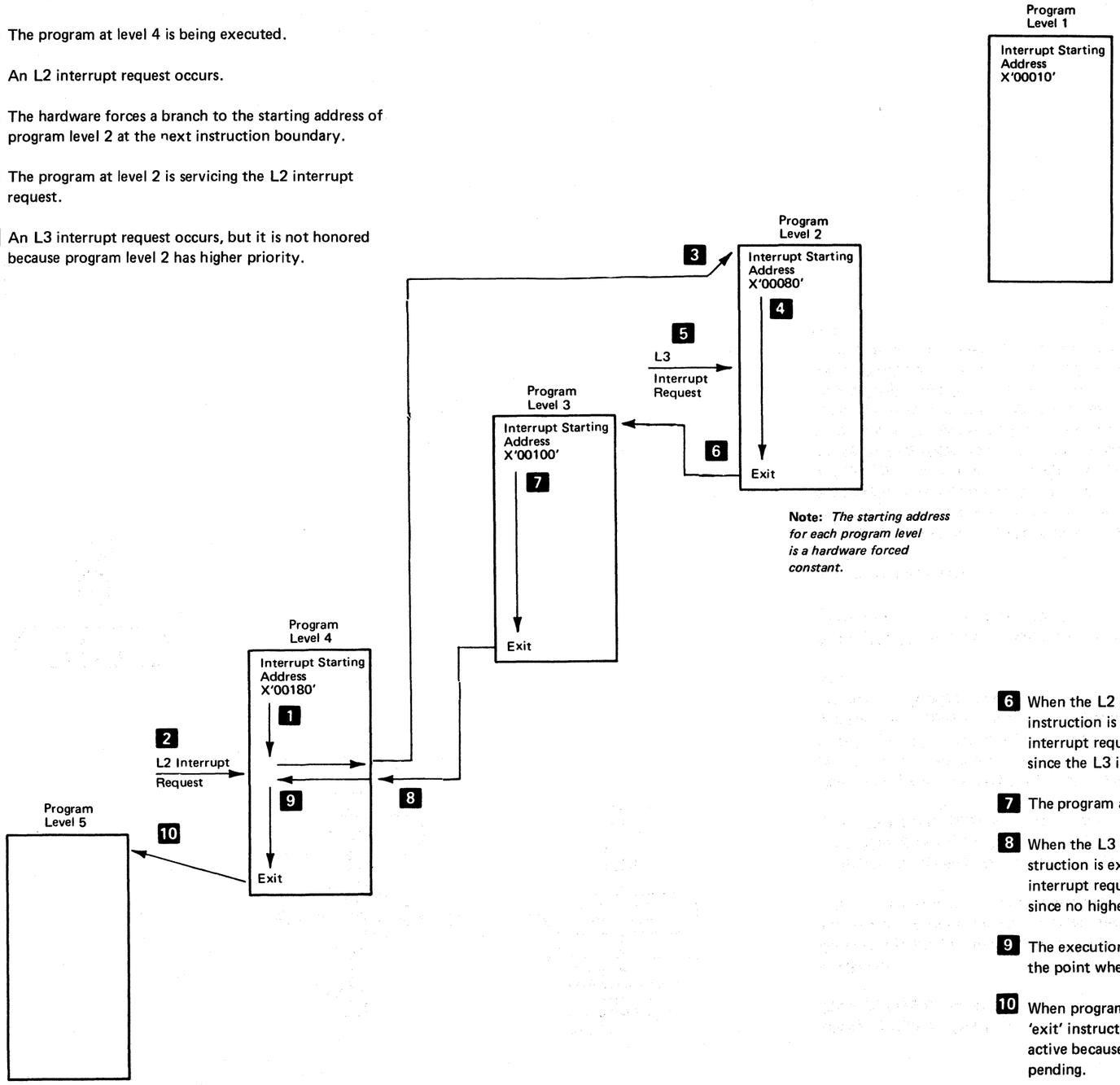
The hardware forces a branch to the storage location that is the starting address for level n.

An 'exit' instruction is executed when the interrupt request has been serviced. The instruction resets the 'level n interrupt entered' latch and allows the machine priority controls to determine which program level should be active next. If no other interrupt requests are pending at a higher priority level, the interrupted program is allowed to continue from the point where it was interrupted. If no interrupt requests are pending at any level, program level 5 becomes active. If level 5 is masked off and no interrupt requests are pending at any level, then an 'exit' instruction will cause the CCU to go into the Wait state (take Idle cycles) until an interrupt occurs. An 'exit' instruction while in level 5 will set a SVC supervisor Call program interrupt to level 4.

The example at the right shows a possible sequence of interrupts.

EXAMPLE:

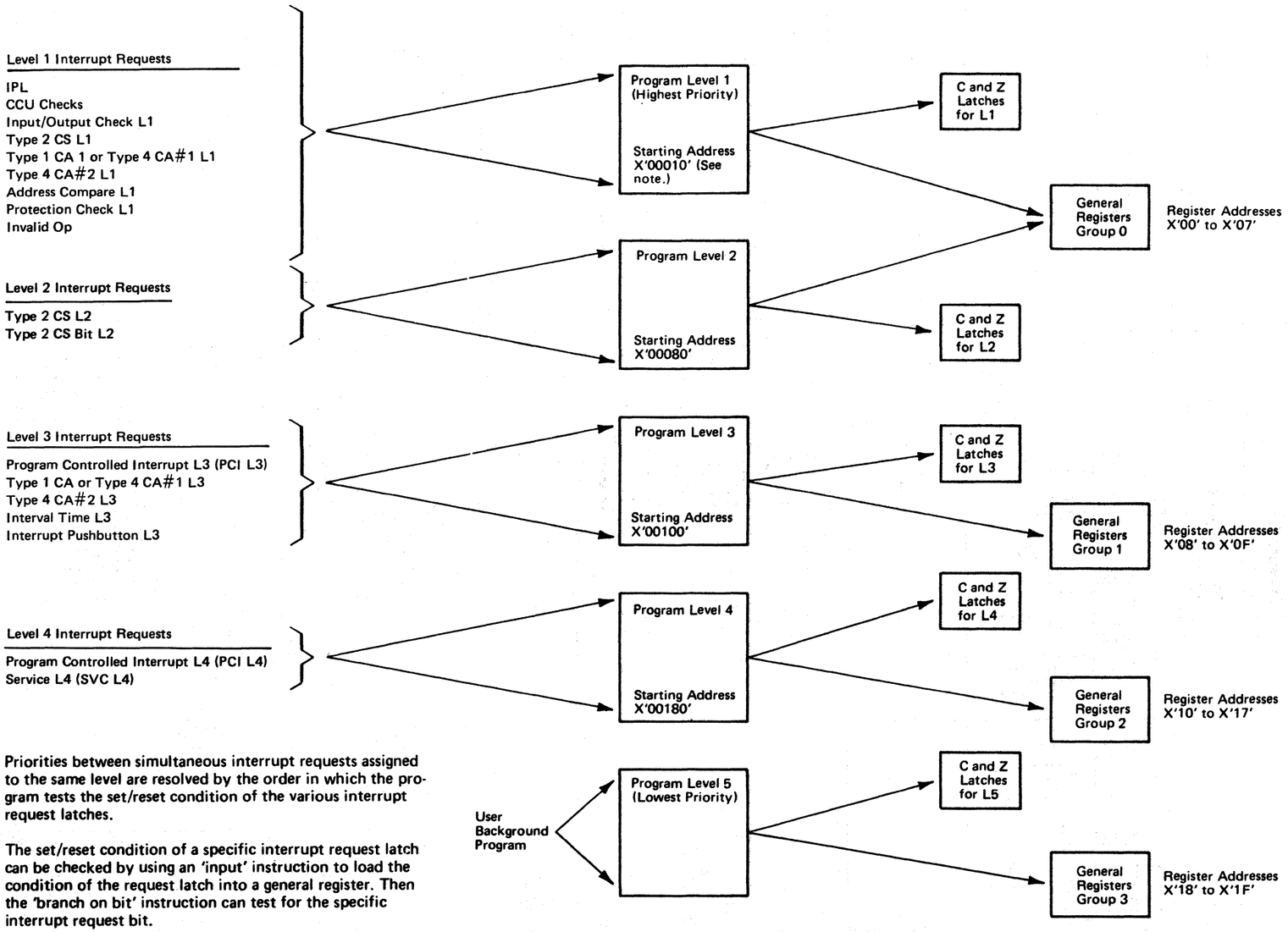
1. The program at level 4 is being executed.
2. An L2 interrupt request occurs.
3. The hardware forces a branch to the starting address of program level 2 at the next instruction boundary.
4. The program at level 2 is servicing the L2 interrupt request.
5. An L3 interrupt request occurs, but it is not honored because program level 2 has higher priority.



Note: *The starting address for each program level is a hardware forced constant.*

6. When the L2 interrupt request is serviced, an 'exit' instruction is executed, and the hardware examines the interrupt requests. Program level 3 becomes active since the L3 interrupt can now be honored.
7. The program at level 3 services the L3 interrupt request.
8. When the L3 interrupt request is serviced, an 'exit' instruction is executed. The hardware examines the interrupt requests, and program level 4 becomes active since no higher interrupt requests exist.
9. The execution of the program at level 4 continues from the point where it was interrupted.
10. When program execution at level 4 is completed, an 'exit' instruction is executed. Program level 5 is now active because no interrupts to a higher level are pending.

PROGRAM LEVEL PRIORITIES AND INTERRUPTS (PART 2 OF 3)



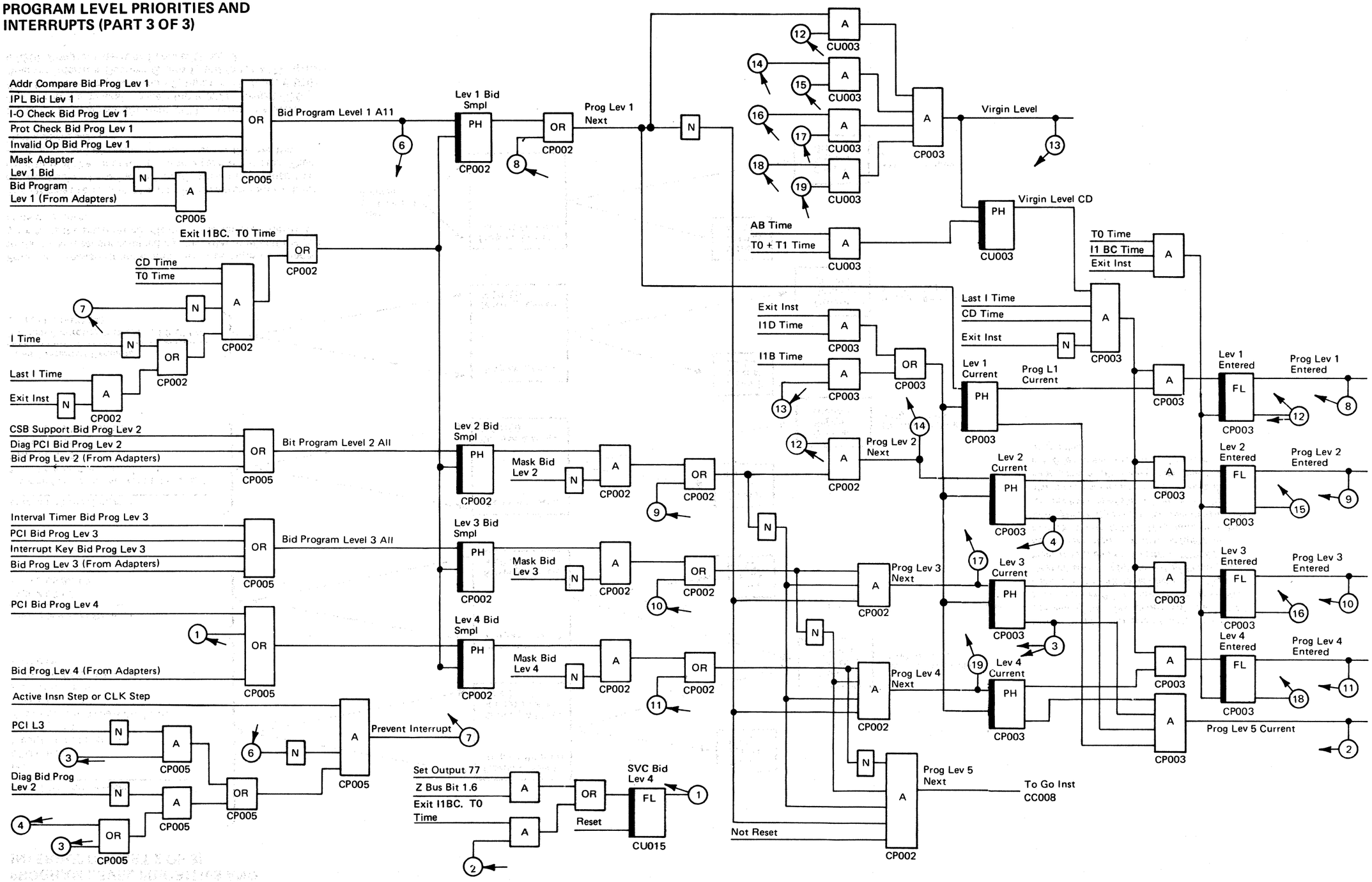
Priorities between simultaneous interrupt requests assigned to the same level are resolved by the order in which the program tests the set/reset condition of the various interrupt request latches.

The set/reset condition of a specific interrupt request latch can be checked by using an 'input' instruction to load the condition of the request latch into a general register. Then the 'branch on bit' instruction can test for the specific interrupt request bit.

Input X'7E' (page 6-850) loads CCU Interrupt Request Group 1 into a general register; Input X'7F' (page 6-860), CCU Interrupt Request Group 2; Input X'76' (page 6-810), Adapter Interrupt Request Group 1; and Input X'77' (page 6-820), Adapter Interrupt Request Group 2.

Note: *On all IBM programs, Address X'00010' contains a 'store' instruction with the R and B fields equal to 0. This instruction causes the address in the IAR to be placed at the storage location specified by the sum of the displacement field D and the constant X'00780'. Seven more 'store' instructions follow the first 'store' instruction. They store the other seven general registers in the next consecutive address because of the D field value. This allows program levels 1 and 2 to share the same group of general registers. See page 6-430 for an explanation of the 'store' instruction.*

PROGRAM LEVEL PRIORITIES AND INTERRUPTS (PART 3 OF 3)



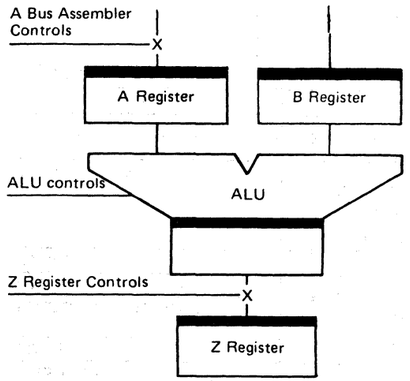
DATA OPERATION CONTROLS

The Arithmetic Logic Unit (ALU) performs all arithmetic and logic functions. It can perform 8, 16, or 18 bit arithmetic in one operation.

The A side of the ALU can be loaded through the A register with the true or the complemented value of SDR, SDR shifted right one bit position, SAR, or hardware generated constants.

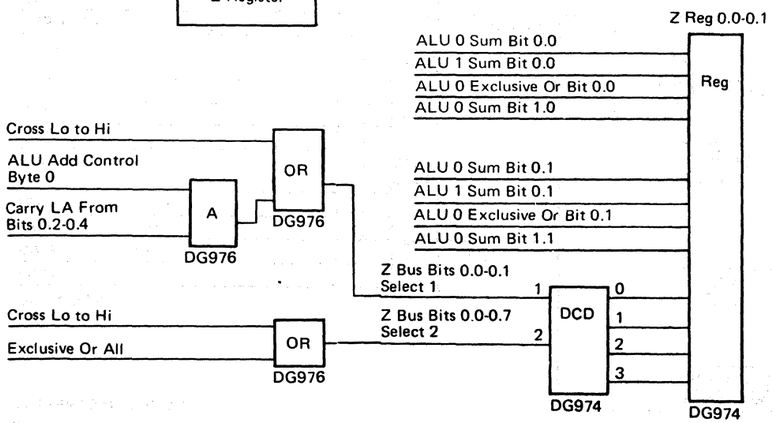
The B side of the ALU can be loaded through the B register with the contents of 1 of the 32 general registers or with data from the Y bus.

The chart on this page shows what control lines are active for specific data operations.



ALU Control Cards

ALU Bits	*Card*
X.P-X.7	B4J2
0.P-0.1	B4K2
0.2-0.4	B4L2
0.5-0.7	B4M2
1.P-1.1	B4N2
1.2-1.4	B4P2
1.5-1.7	B4Q2



Note: *The output of the decode circuit is a binary decode of the two select lines. For example, if 'Z bus bits 0.0-0.7 select 2' is active and 'Z bus bits 0.0-0.1 select 1' is inactive, the binary decode is 2. Therefore, the lines 'ALU 0 exclusive or bit 0.0' and 'ALU 0 exclusive or bit 0.1' are selected to determine the setting of the Z register.*

A Bus Assembler Control Lines Cards B3J2 and B4R2

ALU Control Lines Card B3J2

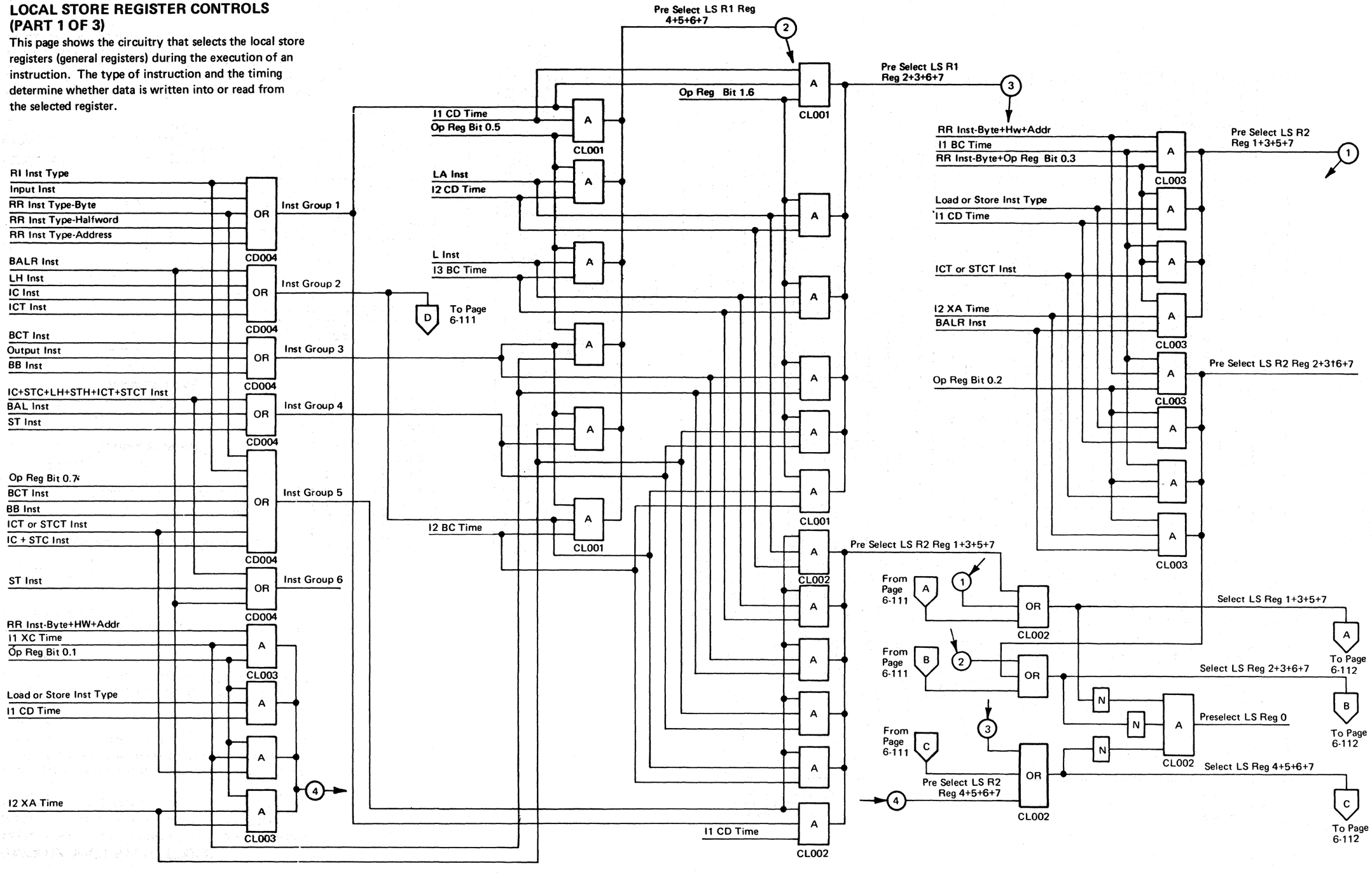
Z Register Control Lines Card B3J2

Operation	*Complement A Bus (CA004)*	*Shift Right (CF004)*	*Shift Right Bit 0.0 (CF004)*	*Shift Right Bit 1.0 (CF004)*	*ALU And Control Byte X (CA004)*	*ALU And Control Byte 0 (CA004)*	*ALU And Control Byte 1 (CA004)*	*ALU Or Control Byte X (CA004)*	*ALU Or Control Byte 0 (CA004)*	*ALU Or Control Byte 1 (CA004)*	*ALU Add Control Byte X (CA004)*	*ALU Add Control Byte 0 (CA004)*	*ALU Add Control Byte 1 (CA004)*	*Cross Hi to Lo (CA003)*	*Cross Lo to Hi (CA003)*	*Exclusive Or All (CA003)*	*ALU Add Control Byte X (CA004)*	*ALU Add Control Byte 0 (CA004)*	*ALU Add Control Byte 1 (CA004)*
A Register Direct (byte 0)	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
A Register Direct (byte 1)	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0
A Register Direct (bytes 0, 1)	0	0	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0
A Register Direct (bytes X, 0, 1)	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
Add (byte 0)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
Add (byte 1)	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1
Add (bytes 0, 1)	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1
Add (bytes X, 0, 1)	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1
And (byte 0)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
And (byte 1)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
And (bytes 0, 1)	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
And (bytes X, 0, 1)	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
B Register Direct	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Compare (byte 0)	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
Compare (byte 1)	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1
Compare (bytes 0, 1)	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1
Compare (bytes X, 0, 1)	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1
Cross Lo to Hi (Byte 1 to Byte 0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Cross Hi to Lo (Byte 0 to Byte 1)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Or (byte 0)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Or (byte 1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Or (bytes 0, 1)	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
Or (bytes X, 0, 1)	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0
Subtract (byte 0)	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
Subtract (byte 1)	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1
Subtract (bytes 0, 1)	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1
Subtract (bytes X, 0, 1)	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1
Xor (byte 0)	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0
Xor (byte 1)	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0	0
Xor (bytes 0, 1)	0	0	0	0	0	1	1	0	1	1	0	0	0	0	0	1	0	0	0
Xor (bytes X, 0, 1)	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	1	0	0	0
Shift Right (byte 0)	0	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
Shift Right (byte 1)	0	1	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0
Shift Right (bytes 0, 1)	0	1	1	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0
Shift Right (bytes X, 0, 1)	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

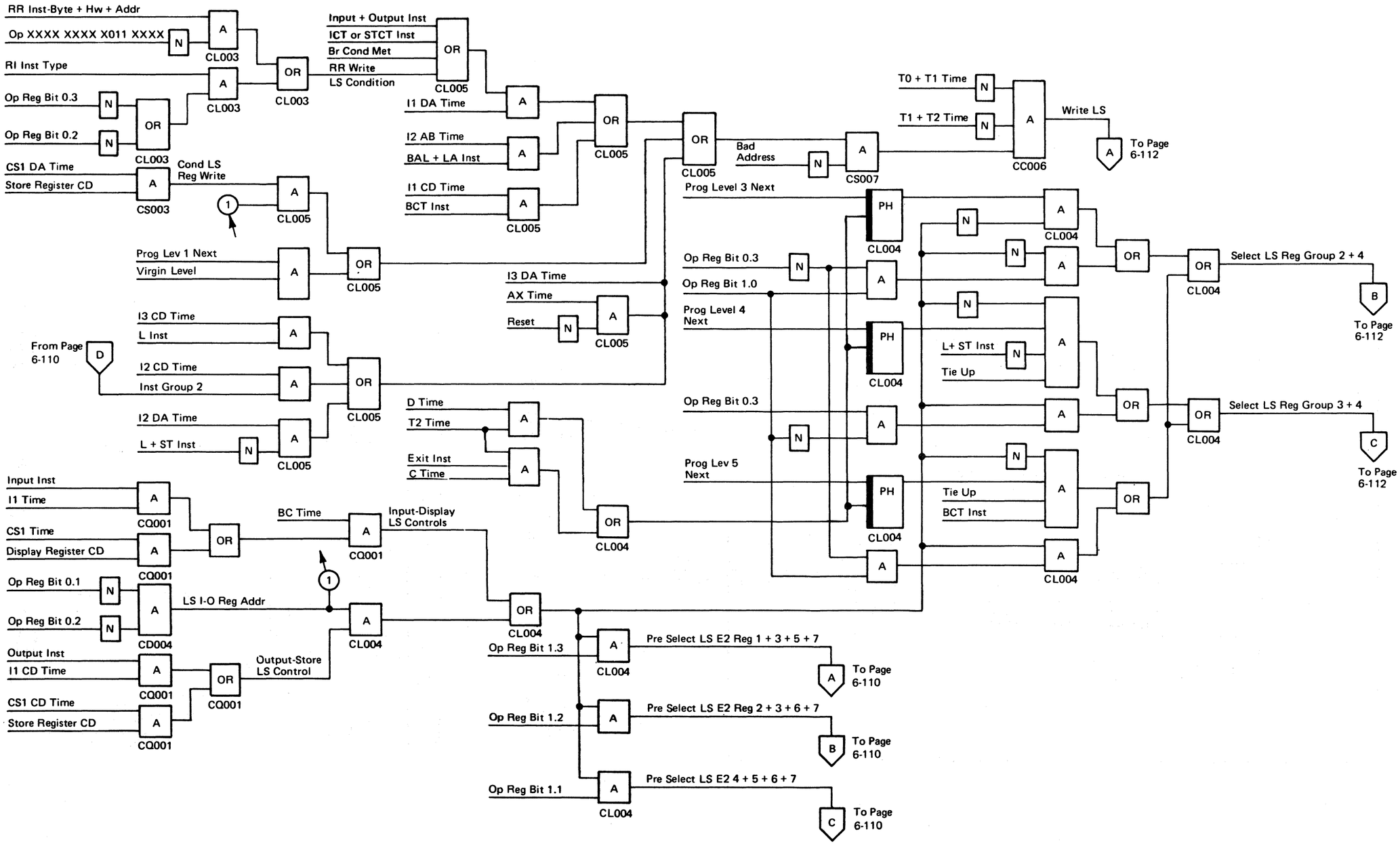
0 = Inactive
1 = Active

LOCAL STORE REGISTER CONTROLS (PART 1 OF 3)

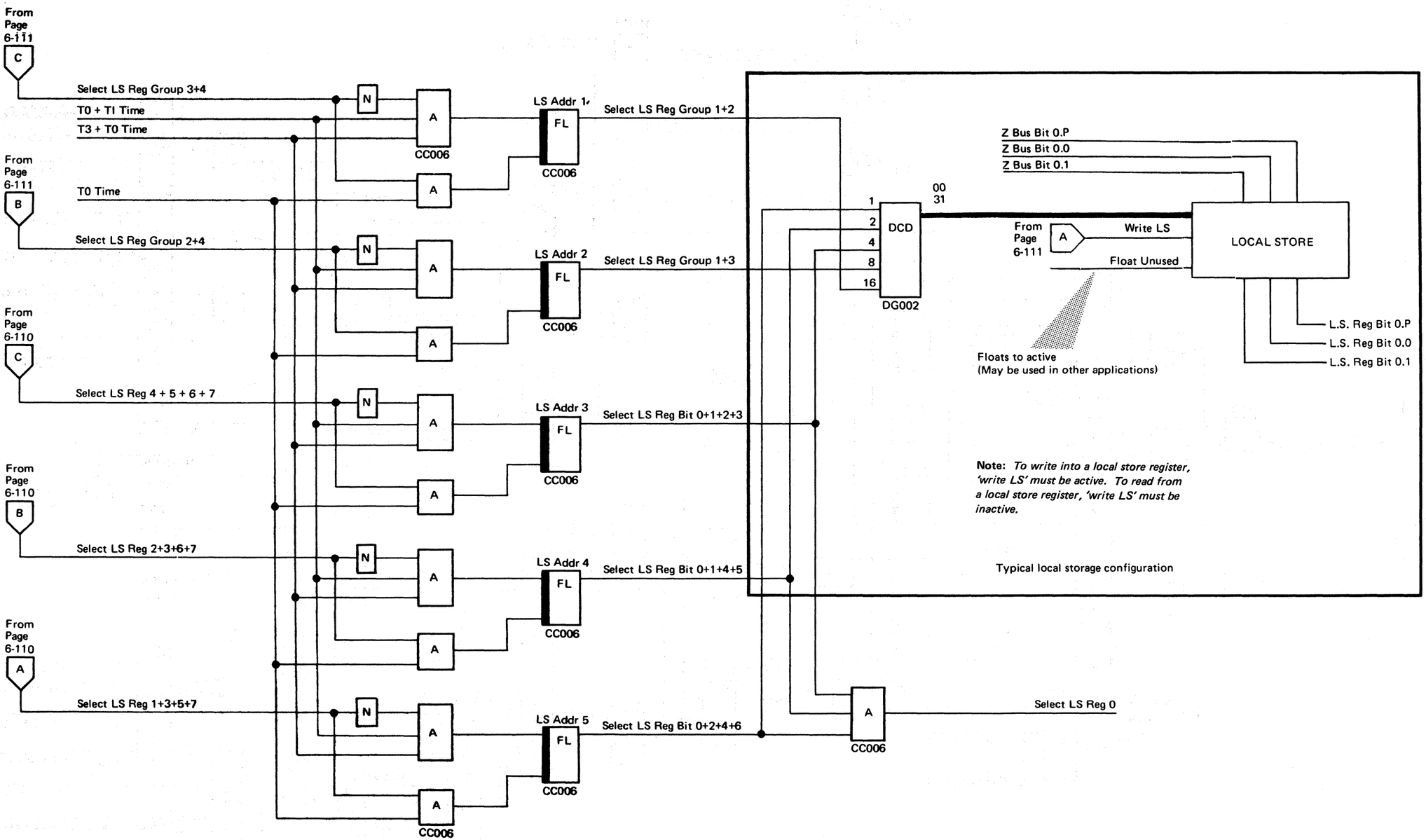
This page shows the circuitry that selects the local store registers (general registers) during the execution of an instruction. The type of instruction and the timing determine whether data is written into or read from the selected register.



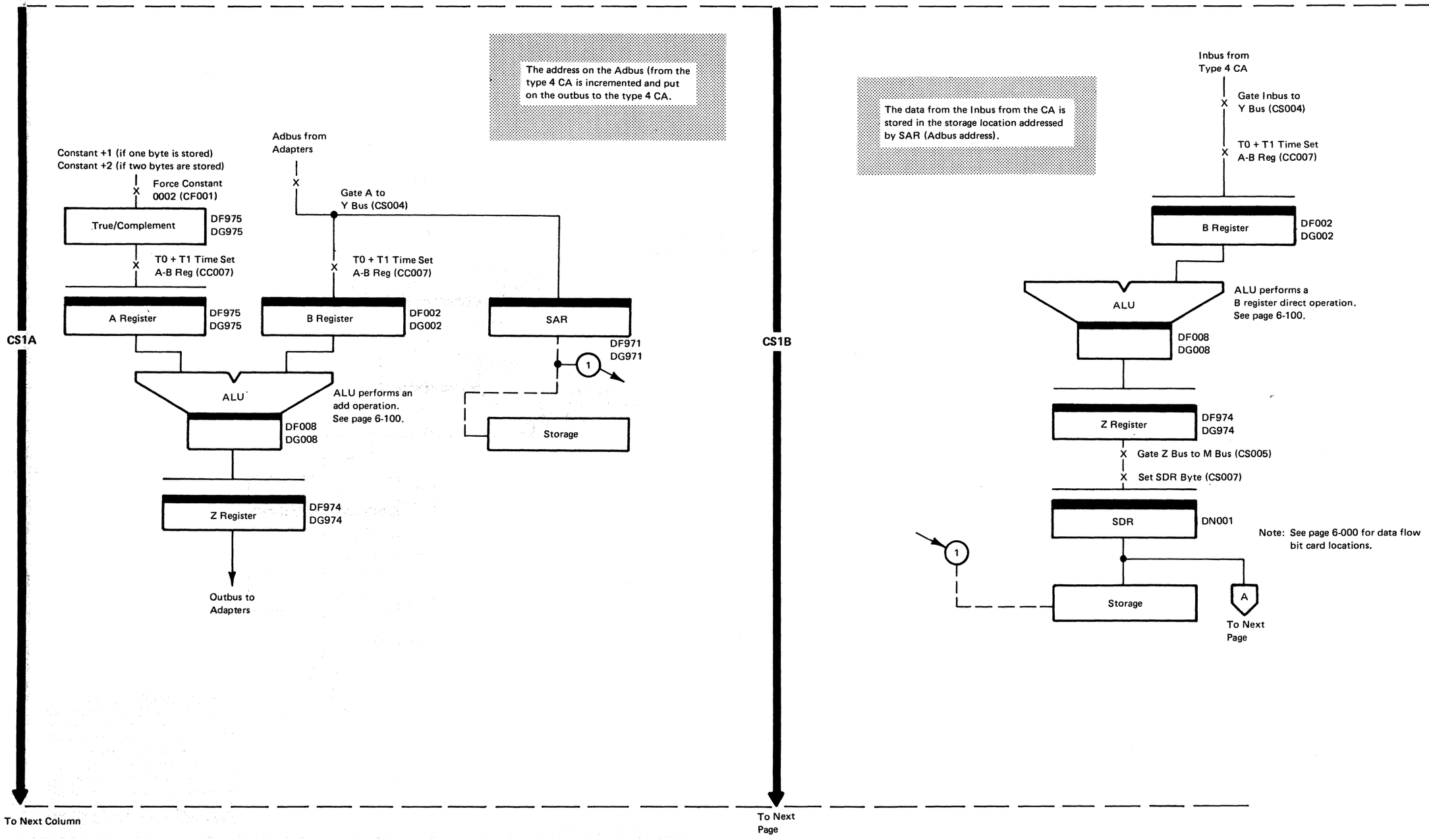
LOCAL STORE REGISTER CONTROLS (PART 2 OF 3)



LOCAL STORE REGISTER CONTROLS (PART 3 OF 3)

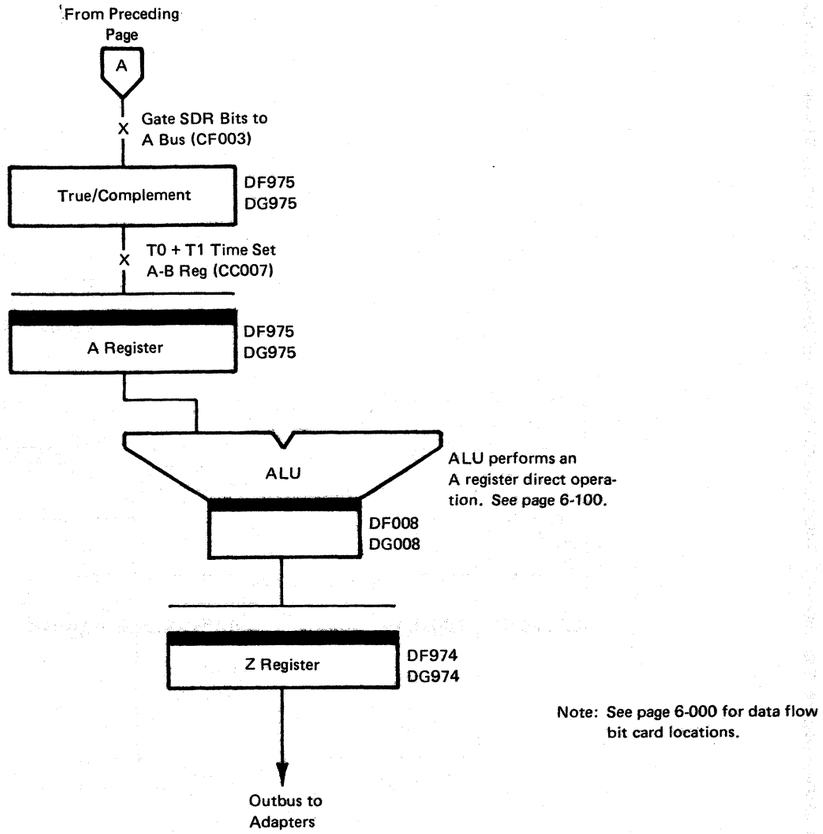


CYCLE STEAL IN (TYPE 4 CA) (PART 1 OF 2)



From Preceding Page

The data in SDR is put on the Outbus to the adapters, but the CA ignores this data. (The CA doesn't need the data because it had sent originally the data to the CCU.)



Note: See page 6-000 for data flow bit card locations.

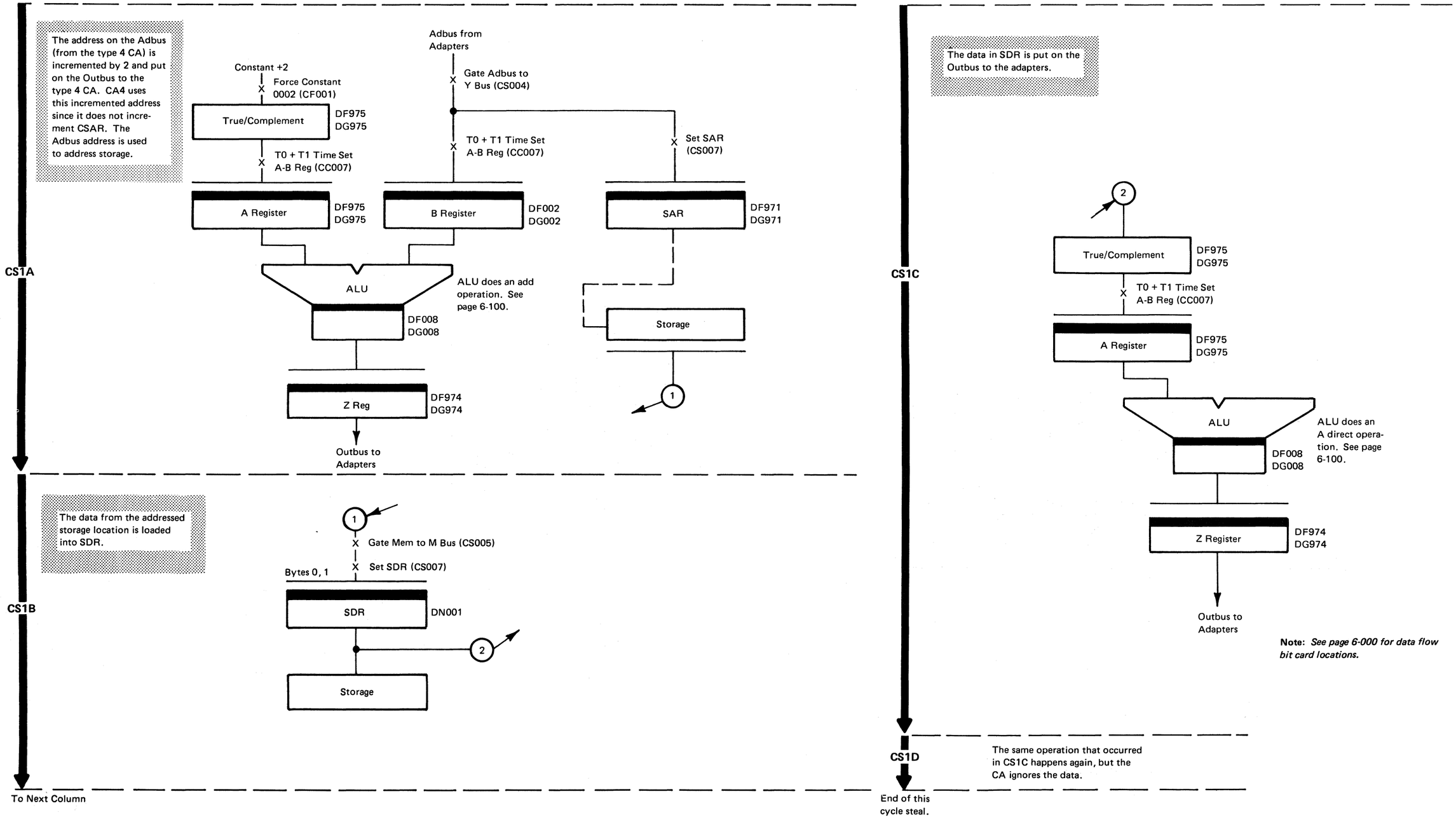
CS1C

CS1D

The same operation that occurred in CS1C happens again.

End of this cycle steal.

CYCLE STEAL OUT (TYPE 4 CA)



Note: *See page 6-000 for data flow bit card locations.*

INSTRUCTION DECODING (PART 1 OF 2)

Abbr.	Instruction	Format Code	FETMM Page	Flow-Chart Page	Cycles	Format
B	Branch	RT	6-630	6-640	1	1 0 1 0 1 T *
BCL	Branch on C Latch	RT	6-630	6-640	1	1 0 0 0 1 T *
BZL	Branch on Z Latch	RT	6-630	6-640	1	1 0 0 0 1 T *
BCT	Branch on Count	RT	6-630	6-680	1	1 0 1 1 1 R N 1 T *
BB***	Branch on Bit	RT	6-630	6-660	1	1 1 M M 1 R N M T *
LRI*	Load Register Immediate	RI	6-160	6-170	1	1 0 0 0 0 R N I
ARI*	Add Register Immediate	RI	6-160	6-170	1	1 0 0 1 0 R N I
SRI*	Subtract Register Immediate	RI	6-160	6-170	1	1 0 1 0 0 R N I
CRI*	Compare Register Immediate	RI	6-160	6-170	1	1 0 1 1 0 R N I
XRI*	Exclusive-Or Register Immediate	RI	6-160	6-170	1	1 1 0 0 0 R N I
ORI*	Or Register Immediate	RI	6-160	6-170	1	1 1 0 1 0 R N I
NRI*	And Register Immediate	RI	6-160	6-170	1	1 1 1 0 0 R N I
TRM*	Test Register Under Mask	RI	6-160	6-170	1	1 1 1 1 0 R N I
LCR*	Load Character Register	RR	6-200	6-220	1	0 R2 N2 0 0 R1 N1 0 0 0 0 1 0 0 0
ACR*	Add Character Register	RR	6-190	6-220	1	0 R2 N2 0 0 R1 N1 0 0 0 1 1 0 0 0
SCR*	Subtract Character Register	RR	6-210	6-220	1	0 R2 N2 0 0 R1 N1 0 0 1 0 1 0 0 0
CCR*	Compare Character Register	RR	6-190	6-220	1	0 R2 N2 0 0 R1 N1 0 0 1 1 1 0 0 0
XCR*	Exclusive Or Character Register	RR	6-200	6-220	1	0 R2 N2 0 0 R1 N1 0 1 0 0 1 0 0 0
OCR*	Or Character Register	RR	6-210	6-220	1	0 R2 N2 0 0 R1 N1 0 1 0 1 1 0 0 0
NCR*	And Character Register	RR	6-190	6-220	1	0 R2 N2 0 0 R1 N1 0 1 1 0 1 0 0 0
LCOR*	Load Character With Offset Reg.	RR	6-200	6-220	1	0 R2 N2 0 0 R1 N1 0 1 1 1 1 0 0 0
ICT	Insert Character and Count	RSA	6-470	6-480	2	0 R2 N2 0 0 R1 N1 0 0 0 1 0 0 0 0
STCT	Store Character and Count	RSA	6-470	6-520	2	0 R2 N2 0 0 R1 N1 0 0 1 1 0 0 0 0
IC*	Insert Character	RS	6-270	6-290	2	0 B 0 R N 0 D
STC	Store Character	RS	6-270	6-330	2	0 B 1 R N 1 D
LH*	Load Halfword	RS	6-270	6-290	2	0 B 0 R 0 D 1
STH	Store Halfword	RS	6-270	6-360	2	0 B 0 R 1 D 1
L*	Load	RS	6-270	6-390	3	0 B 0 R 0 D 1 0
ST	Store	RS	6-270	6-430	3	0 B 0 R 1 D 1 0
LHR*	Load Halfword Register	RR	6-200	6-220	1	0 R2 N2 0 0 R1 N1 1 0 0 0 0 0 0 0
AHR*	Add Halfword Register	RR	6-190	6-220	1	0 R2 N2 0 0 R1 N1 1 0 0 1 0 0 0 0
SHR*	Subtract Halfword Register	RR	6-210	6-220	1	0 R2 N2 0 0 R1 N1 1 0 1 0 0 0 0 0
CHR*	Compare Halfword Register	RR	6-200	6-220	1	0 R2 N2 0 0 R1 N1 1 0 1 1 0 0 0 0
XHR*	Exclusive Or Halfword Register	RR	6-200	6-220	1	0 R2 N2 0 0 R1 N1 1 1 0 0 0 0 0 0
OHR*	Or Halfword Register	RR	6-210	6-220	1	0 R2 N2 0 0 R1 N1 1 1 0 1 0 0 0 0
NHR*	And Halfword Register	RR	6-190	6-220	1	0 R2 N2 0 0 R1 N1 1 1 1 0 0 0 0 0
LHOR*	Load Halfword With Offset Reg.	RR	6-200	6-220	1	0 R2 N2 0 0 R1 N1 1 1 1 1 0 0 0 0
LR*	Load Register	RR	6-210	6-220	1	0 R2 N2 0 0 R1 N1 1 0 0 0 1 0 0 0
AR*	Add Register	RR	6-190	6-220	1	0 R2 N2 0 0 R1 N1 1 0 0 1 1 0 0 0
SR*	Subtract Register	RR	6-210	6-220	1	0 R2 N2 0 0 R1 N1 1 0 1 0 1 0 0 0
CR*	Compare Register	RR	6-200	6-220	1	0 R2 N2 0 0 R1 N1 1 0 1 1 1 0 0 0
XR*	-Exclusive Or Register	RR	6-200	6-220	1	0 R2 N2 0 0 R1 N1 1 1 0 0 1 0 0 0
OR*	Or Register	RR	6-210	6-220	1	0 R2 N2 0 0 R1 N1 1 1 0 1 1 0 0 0
NR*	And Register	RR	6-190	6-220	1	0 R2 N2 0 0 R1 N1 1 1 1 0 1 0 0 0
LOR*	Load With Offset Register	RR	6-210	6-220	1	0 R2 N2 0 0 R1 N1 1 1 1 1 1 0 0 0
BALR	Branch and Link Register	RR	6-190	6-240	2	0 R2 N2 0 0 R1 N1 0 1 0 0 0 0 0 0
IN	Input	RE	6-700	6-710	1	0 E_x** 0 R E_y** 0 1 1 0 0
OUT	Output	RE	6-700	6-730	1	0 E_x** 0 R E_y** 0 1 1 0 0
BAL	Branch and Link	RA	6-560	6-570	2	1 0 1 1 1 R N 0 0 0 0 0 0 A (16 … 31)
LA	Load Address	RA	6-560	6-600	2	1 0 1 1 1 R N 0 0 1 0 0 0 A (16 … 31)
EXIT	Exit	Exit	6-700	6-750	1	1 0 1 1 1 0 0 0 0 1 0 0 0 0 0 0

*	DISP (HW)
0	1 + T
1	1 − T

* These instructions can change the C and Z condition latches.

**See page 6-151 for a decode of the E Field.

*** See page 6-630 for a decode of the M Field

BYTE SELECTION DECODING

Instr. Bits 1 2 3	R2 N2 Fields: LCR, ACR, SCR, CCR, OCR, XCR, NCR, LCOR	B Field: ICT, STCT, IC, STC, LH, STH, L, ST	R2 Field: LR, AR, SR, CR, OR, XR, NR, LOR, BALR	R2 Field: LHR, AHR, SHR, CHR, OHR, XHR, NHR, LHOR
0 0 0	Reg. 1; Byte 0	See Note 1	Reg. 0; Byte 0, 1	Reg. 0; Byte X, 0, 1
0 0 1	1 1	Reg. 1; Byte X, 0, 1	1	1
0 1 0	3 0	2	2	2
0 1 1	3 1	3	3	3
1 0 0	5 0	4	4	4
1 0 1	5 1	5	5	5
1 1 0	7 0	6	6	6
1 1 1	7 1	7	7	7

Notes:

1. *X'000' specifies the address constant for IC, STC, LH, STH, L, and ST instructions. (See the descriptions of these instructions for the value of the address constant.) X'000' specifies register 0, bytes X, 0, and 1 for ICT and STCT instructions.*

Instr. Bits 5 6 7	R, N Fields: LRI, CRI, ORI, XRI, NRI, TRM, BB, ICT, STCT, IC, STC	R1, N1 Fields: LCR, CCR, OCR, XCR, NCR, LCOR	R, N Fields: ARI, SRI, BCT	R1, N1 Fields: ACR, SCR
0 0 0	Reg. 1; Byte 0	Reg. 1; Byte 0	Reg. 1; Byte 0	Reg. 1; Byte 0
0 0 1	1 1	1 1	1 0, 1	1 0,1
0 1 0	3 0	3 0	3 0	3 0
0 1 1	3 1	3 1	3 0, 1	3 0,1
1 0 0	5 0	5 0	5 0	5 0
1 0 1	5 1	5 1	5 0, 1	5 0,1
1 1 0	7 0	7 0	7 0	7 0
1 1 1	7 1	7 1	7 0, 1	7 0,1

Instr. Bits 5 6 7	R Field: LH, STH	R1 Field: LHR, AHR, SHR, CHR, OHR, XHR, NHR, LHOR	R1 Field: LR, AR, SR, CR, OR, XR, NR, LOR, BALR	R Field: BAL, LA, IN, OUT, L, ST
0 0 0	See Note 3	Reg. 0; Bytes 0, 1	Reg. 0; Byte X, 0, 1	See Note 2
0 0 1	Reg. 1; Byte 0, 1	1	1	Reg. 1; Byte X, 0, 1
0 1 0	2	2	2	2
0 1 1	3	3	3	3
1 0 0	4	4	4	4
1 0 1	5	5	5	5
1 1 0	6	6	6	6
1 1 1	7	7	7	7

2. *X'000' specifies register 0, bytes X, 0, and 1 for L, BAL, LA, IN, and OUT instructions. X'000' specifies a 0 constant (18 bits) for ST.*
3. *X'000' specifies register 0, bytes 0 and 1 for LH. X'000' specifies a 0 constant (16 bits) for STH.*

INSTRUCTION DECODING (PART 2 OF 2)

Input Register Addresses

E Field XY	Register/Function		FETMM Page
00	Gen Reg, Group 0	Reg 0	6-770
01		Reg 1	6-770
02		Reg 2	6-770
03		Reg 3	6-770
04		Reg 4	6-770
05		Reg 5	6-770
06		Reg 6	6-770
07		Reg 7	6-770
08	Gen Reg, Group 1	Reg 0	6-770
09		Reg 1	6-770
0A		Reg 2	6-770
0B		Reg 3	6-770
0C		Reg 4	6-770
0D		Reg 5	6-770
0E		Reg 6	6-770
0F		Reg 7	6-770
10	Gen Reg, Group 2	Reg 0	6-770
11		Reg 1	6-770
12		Reg 2	6-770
13		Reg 3	6-770
14		Reg 4	6-770
15		Reg 5	6-770
16		Reg 6	6-770
17		Reg 7	6-770
18	Gen Reg, Group 3	Reg 0	6-770
19		Reg 1	6-770
1A		Reg 2	6-770
1B		Reg 3	6-770
1C		Reg 4	6-770
1D		Reg 5	6-770
1E		Reg 6	6-770
1F		Reg 7	6-770
20-3F	A constant of all zeros is loaded into R, and the CCU sets the input/output check L1 request.		

E Field XY	Register/Function	FETMM Page
48-4F	A constant of all zeros is loaded into R, and the CCU sets the input/output check L1 request.	
*60	Initial Selection Control	8-070,H-050
*61 T	Initial Selection Address & Command	8-070,H-050
*62 1	Data/Status Control	8-090,H-070
*63 C	Address and ESC Status	8-100,H-080
*64 A	Data Buffer Bytes 1, 2	8-110,H-090
*65 &	Data Buffer Bytes 3, 4	8-110,H-090
*66 T	NSC Status Byte	8-120,H-100
*67 4	Control	8-130,H-110
**68 C	Level 1 Status	
**69 A	Level 3 Status	
**6A	Parallel Data Register	
**6B	Control Pgm Load Reg	
***6C	CA4 EB Mode Control Reg	H-130
***6D	CA4 EB Mode Data Buffer	H-150
***6E	CA4-CS Register and CSAR Byte X	H-170
***6F	CA4-CSAR Byte 0/1	H-170
70	Storage Size Installed	6-770
71	Panel Address/Data Digits	6-780
72	Display/Function Select Switch	6-790
73	Insert Key	6-800
74	LAR	6-800
75	A constant of all zeros is loaded into R.	
76 C	Adapter Interrupt Request Group 1	6-810
77 C	Adapter Interrupt Request Group 2	6-820
78 U	A constant of all zeros is loaded into R.	
79	Utility	6-830
7B	BSC CRC Register	6-840
7C	Reserved	
7D	CCU Check Register	6-841
7E	CCU Level 1 Interrupt Requests	6-850
7F	CCU Level 2 Interrupt Requests	6-860

Output Register Addresses

E Field XY	Register/Function		FETMM Page
00	Gen Reg, Group 0	Reg 0	6-870
01		Reg 1	6-870
02		Reg 2	6-870
03		Reg 3	6-870
04		Reg 4	6-870
05		Reg 5	6-870
06		Reg 6	6-870
07		Reg 7	6-870
08	Gen Reg, Group 1	Reg 0	6-870
09		Reg 1	6-870
0A		Reg 2	6-870
0B		Reg 3	6-870
0C		Reg 4	6-870
0D		Reg 5	6-870
0E		Reg 6	6-870
0F		Reg 7	6-870
10	Gen Reg, Group 2	Reg 0	6-870
11		Reg 1	6-870
12		Reg 2	6-870
13		Reg 3	6-870
14		Reg 4	6-870
15		Reg 5	6-870
16		Reg 6	6-870
17		Reg 7	6-870
18	Gen Reg, Group 3	Reg 0	6-870
19		Reg 1	6-870
1A		Reg 2	6-870
1B		Reg 3	6-870
1C		Reg 4	6-870
1D		Reg 5	6-870
1E		Reg 6	6-870
1F		Reg 7	6-870
20-3F	The bits of R are ignored, and the CCU sets the input/output check L1.		

E Field XY	Register/Function	FETMM Pages
*60	Reset Initial Selection	8-070
*61	Unused	
*62 T	Data/Status Control	8-080,H-060
*63 1	Address and ESC Status	8-100,H-080
*64 C	Data Buffer Bytes 1, 2	8-110,H-090
*65 A	Data Buffer Bytes 3, 4	8-110,H-090
*66 &	NSC Status Byte	8-120,H-100
*67 T	Control	8-130,H-120
**68 4	Control	
**69 C	Read/Write	
**6A A	Parallel Data Register	
**6B	Control Pgm Load Reg	
***6C	CA4 EB Mode Control Reg	H-140
***6D	CA4 EB Mode Data Buffer	H-160
***6E	CA4-CSAR Byte X	H-180
***6F	CA4-CSAR Byte 0/1	H-180
70	Hardstop	6-870
71	Display Reg 1	6-870
72	Display Reg 2	6-880
74-76	The bits of R are ignored	
77 C	Miscellaneous Control	6-900
78 C	Force CCU Checks	6-920
79 U	Utility	6-930
7A	The bits of R are ignored.	6-940
7B	The bits of R are ignored.	
7C	Set PCI L3	6-940
7D	Set PCI L4	6-940
7E	Set Mask Bits	6-940
7F	Reset Mask Bits	6-950

E Field XY	Register/Function Type 2 Scanner	FETMM Page
40	Interface Address	B-120
41	Unused	
42	Unused	
43	Check Register	B-130
44	ICW Input Reg 0-15	B-140
45	ICW Input Reg 16-31	B-140
46	Display Register	B-150
47	ICW Input Reg 32-45	B-140
48	Unused	
49	Unused	
4A	Unused	
4B	Unused	
4C	Unused	
4D	Unused	
4E	Unused	
4F	Unused	

*Inputs and Outputs X'60'-X'67' are for the type 1 and type 4 CA.
**Inputs and Outputs X'68, 69, 6A, 6B' are used for the remote loader on a REMOTE 3705-80.
***Inputs and Outputs X'6C'-X'6F' are for the type 4 CA.

E Field XY	Register/Function Type 2 Scanner	FETMM Page
40	Interface Address	B-160
41	Adr Substitution Ctrl	B-160
42	Upper Scan Limit Ctrl	B-170
43	Control	B-170
44	ICW 0-15	B-180
45	ICW 16-23	B-190
46	ICW 24-33, 44	B-200
47	ICW 34-43	B-210
48		
49	The bits of R are ignored and the CCU sets the input/output check L1 request.	
4A		
4B		
4C		
4D		
4E		
4F		

REGISTER IMMEDIATE (RI) INSTRUCTIONS

The CCU takes one I1 cycle to execute each of the eight 'register immediate' instructions. The same sequence occurs during I1A, I1B, and I1C times for each of the instructions; only the sequence during I1D is different.

For all 'register immediate' instructions, the general register designated by the R field in the instruction must be an odd-numbered register.

Add Register Immediate (ARI)

0	1	2	3	4	5-6	7	8-15
1	0	0	1	0	R	N	I

The data in the I field is added to byte 0 (N=0) or bytes 0 and 1 (N=1) of the general register designated by the R field. The register specified must be an odd-numbered register. The result is stored in the selected byte(s) of the general register. If N=0, byte 1 of R remains unchanged.

The 'C' latch sets if N=0 and byte 0 of R overflows, or if N=1 and bytes 0 and 1 overflow. The 'Z' latch sets if N=0 and byte 0 of R equals 0, or if N=1 and bytes 0 and 1 of R equal 0.

Byte X of the general register is included in the addition if N=1, but byte X does not affect the setting of the C and Z latches.

AND Register Immediate (NRI)

0	1	2	3	4	5-6	7	8-15
1	1	1	0	0	R	N	I

The data in the I field is ANDed with byte 0 (N=0) or byte 1 (N=1) of the general register designated by the R field. This register must be an odd-numbered register. The results are stored in the selected byte of R. The non-selected byte of the register remains unchanged.

The 'C' latch sets if the selected byte of R does not equal 0. The 'Z' latch sets if the selected byte of R equals 0.

Compare Register Immediate (CRI)

0	1	2	3	4	5-6	7	8-15
1	0	1	1	0	R	N	I

The data in the I field is compared with byte 0 (N=0) or byte 1 (N=1) of the general register designated by the R field. This register must be an odd-numbered register. The contents of the general register are not changed.

The 'C' latch sets if the selected byte of R is less than I. The 'Z' latch sets if the selected byte of R equals I.

Exclusive-OR Register Immediate (XRI)

0	1	2	3	4	5-6	7	8-15
1	1	0	0	0	R	N	I

The data in the I field is exclusive-ORed with byte 0 (N=0) or byte 1 (N=1) of the general register designated by the R field. The register must be an odd-numbered register. The results are stored in the selected byte of the general register.

The 'C' latch sets if the selected byte of R does not equal 0. The 'Z' latch sets if the selected byte of R equals 0.

Load Register Immediate (LRI)

0	1	2	3	4	5-6	7	8-15
1	0	0	0	0	R	N	I

The data from the I field is loaded into byte 0 (N=0) or byte 1 (N=1) of the general register designated by the R field. This register must be an odd-numbered register. The non-selected byte of the register remains unchanged.

The 'C' latch sets if the selected byte of R is not equal to 0. The 'Z' latch sets if the selected byte of R equals 0.

OR Register Immediate (ORI)

0	1	2	3	4	5-6	7	8-15
1	1	0	1	0	R	N	I

The data in the I field is ORed with byte 0 (N=0) or byte 1 (N=1) of the general register designated by R. The register specified by the R field must be an odd-numbered register. A bit position in the resulting byte is set to 1 if one or both of the corresponding bit positions in the general register and the I field are 1; otherwise, the bit is set to 0. The results are stored in the selected byte of R. The non-selected byte of R remains unchanged.

The 'C' latch sets if the selected byte of R does not equal 0. The 'Z' latch sets if the selected byte of R equals 0.

Subtract Register Immediate (SRI)

0	1	2	3	4	5-6	7	8-15
1	0	1	0	0	R	N	I

The data in the I field is subtracted from byte 0 (N=0) or from bytes 0 and 1 (N=1) of the general register designated by the R field. This register must be an odd-numbered register. The results are stored in the selected byte(s) of R.

Before the subtraction is done, the I field is expanded with high-order zeros to equal the size of the selected byte(s) of the general register.

The subtraction is done by adding the two's complement of the I field to the selected bytes of the general register. If the difference is less than zero, the result is in two's complement form.

The 'C' latch sets if N=0 and byte 0 of R is less than 0, or if N=1 and bytes 0 and 1 of R are less than 0. The 'Z' latch sets if N=0 and byte 0 of R equals 0, or if N=1 and bytes 0 and 1 of R equal 0.

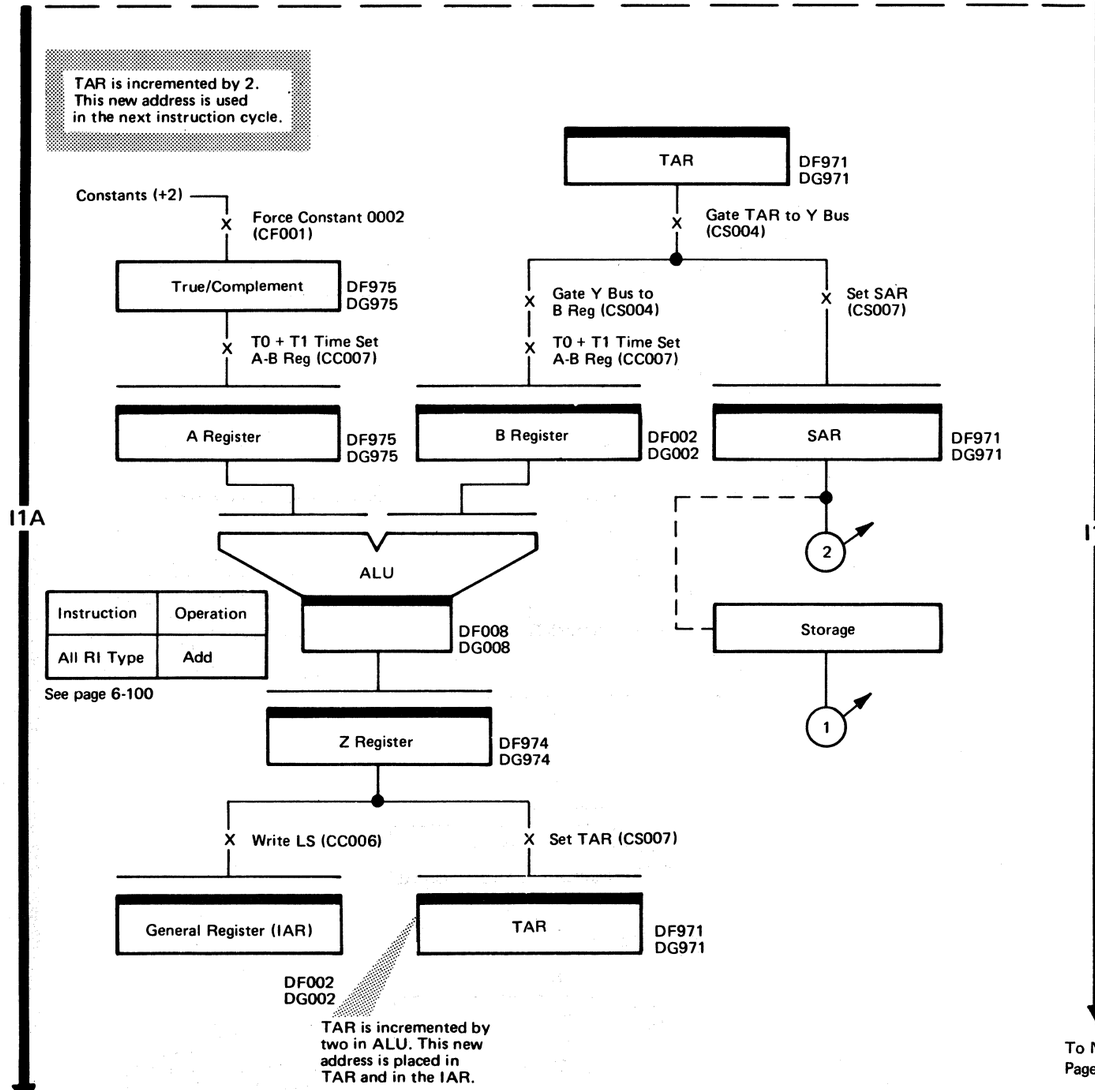
Test Register Under Mask (TRM)

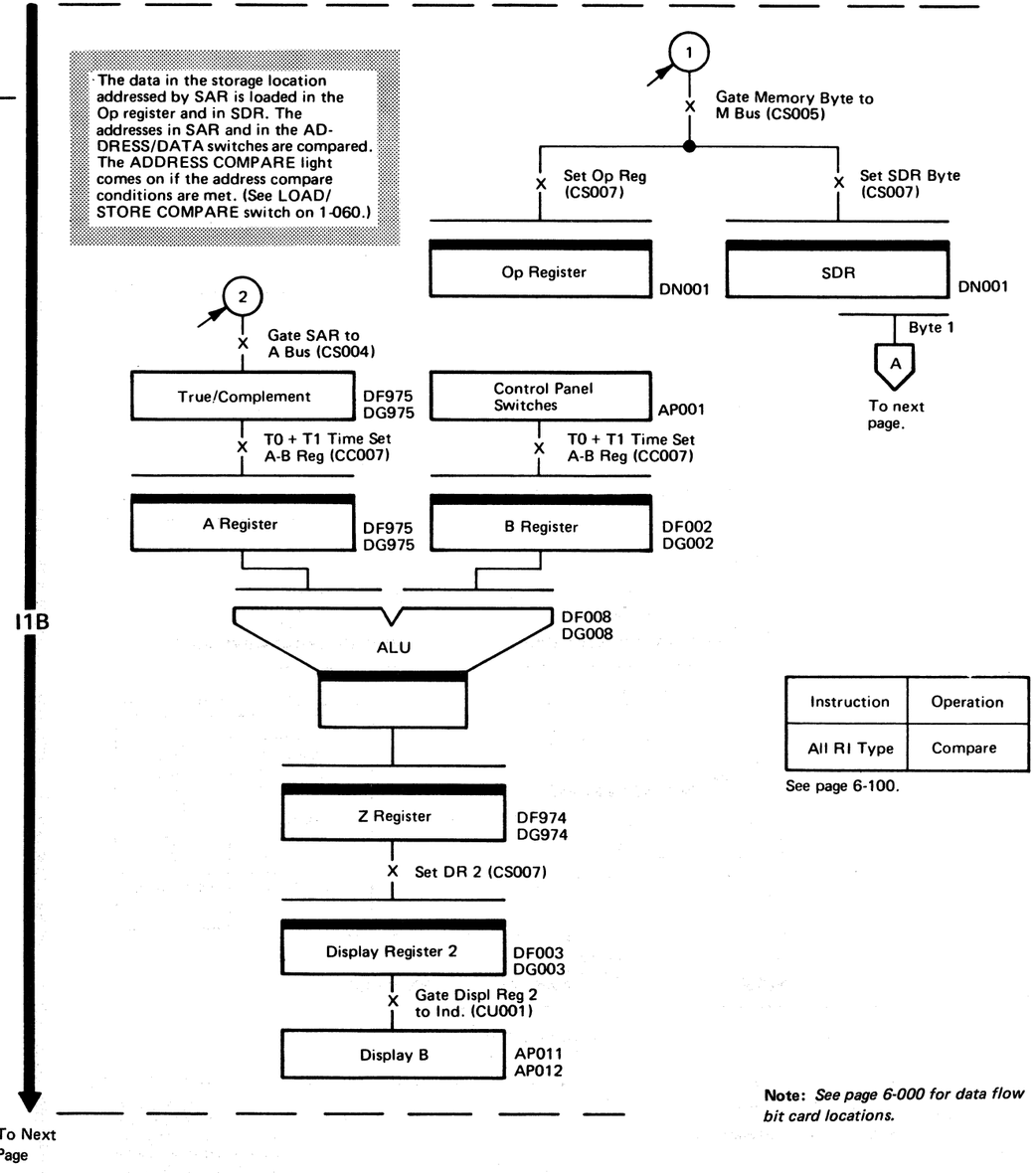
0	1	2	3	4	5-6	7	8-15
1	1	1	1	0	R	N	I

The data in the I field is tested against (ANDed with) byte 0 (N=0) or byte 1 (N=1) of the general register designated by the R field. This register must be an odd-numbered register. The contents of R are not changed.

The 'C' latch sets if the results do not equal 0. The 'Z' latch sets if the results equal 0.

RI Instruction Operation





Instruction	Operation
All RI Type	Compare

See page 6-100.

Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

SDR byte 1 (I field of the instruction) is crossed to byte 0 by ALU and is loaded in byte 0 of SDR. Both bytes 0 and 1 of SDR then contain the I field.

I1C

Instruction	Operation
All RI Type	Cross Lo to Hi

See page 6-100.

From Preceding Page

A

Byte 1

True/Complement — DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

Byte 1

A Register — DF975 DG975

Byte 1

ALU — DF008 DG008

Byte 0

SAR — DF971 DG971

X Set LAR (CS001)

LAR — DF002 DG002

Z Register — DF974 DG974

Byte 0

X Gate Z Bus Byte 0 to M Bus (CS005)

X Set SDR Byte (CS007)

SDR — DN001

1

To Next Column

The specified bytes in SDR and the general register are gated to ALU, and the operation specified by the instruction is performed. The result is stored in the specified bytes of the general register.

I1D

1

X Gate SDR Bits to A Bus (CF003)

True/Complement — DF975 DG975

General Register (R) — DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DF975 DG975

B Register — DF002 DG002

Instruction	Operation
ARI	Add
NRI	And
CRI	Compare
XRI	Xor
LRI	A Reg Direct
ORI	Or
SRI	Subtract
TRM	And

See page 6-100.

ALU — DF008 DG008

C and Z Latches — CZ001

Z Register — DF974 DG975

X Write LS (CC006)

General Register (R) — DF002 DG002

TAR — DF971 DG971

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DF971 DG971

End of Instruction

Note: *See page 6-000 for data flow bit card locations.*

REGISTER TO REGISTER (RR) INSTRUCTIONS (PART 1 OF 3)

The CCU takes one I1 cycle to execute any one of the 25 RR instructions except for the 'branch and link register' (BALR) instruction. The BALR instruction requires an I1 and an I2 cycle for execution.

For halfword, and 18-bit operations, the R1 and R2 fields in the instruction can specify any of the eight general registers in the active group. For byte operations, only an odd-numbered register can be specified, therefore the General Register = (2xR) +1.

Add Character Register (ACR)

0	1-2	3	4	5-6	7	8	9	10	11	12	13	14	15
0	R2	N2	0	R1	N1	0	0	0	1	1	0	0	0

Byte 0 (N2=0) or byte 1 (N2=1) of the general register designated by the R2 field is added to byte 0 (N1=0) or bytes 0 and 1 (N1=1) of the general register designated by the R1 field. The result is placed in the selected byte(s) of R1. The registers specified by R1 and R2 must be odd-numbered registers.

Byte X of the register specified by R1 is included in the operation. However, byte X does not affect the setting of the C and Z latches.

The 'C' latch sets if N1=0 and byte 0 of R1 overflows, or if N1=1 and bytes 0 and 1 overflow.

The 'Z' latch sets if N1=0 and byte 0 of R1 equals 0, or if N1=1 and bytes 0 and 1 of R1, equal 0.

Add Halfword Register (AHR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	0	0	1	0	0	0	0

Bytes 0 and 1 of the general register designated by R2 are added to bytes 0 and 1 of the general register designated by R1. The result is placed in bytes 0 and 1 of R1.

The 'C' latch sets if bytes 0 and 1 overflow. The 'Z' latch sets if bytes 0 and 1 equal 0.

Note: *If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.*

Add Register (AR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	0	0	1	1	0	0	0

Bytes X, 0, and 1 of the general register designated by R2 are added to bytes X, 0, and 1 of the general register designated by R1. The result is placed in R1.

The 'C' latch sets if bytes X, 0, and 1 of R1 overflow.

The 'Z' latch sets if bytes X, 0, and 1 of R1 equal 0.

Note: *If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.*

AND Character Register (NCR)

0	1-2	3	4	5-6	7	8	9	10	11	12	13	14	15
0	R2	N2	0	R1	N1	0	1	1	0	1	0	0	0

Byte 0 (N2=0) or byte 1 (N2=1) of the general register designated by R2 is ANDed with byte 0 (N1=0) or byte 1 (N1=1) of the general register designated by R1. The result is placed in the selected byte of R1. The registers specified by R1 and R2 must be odd-numbered registers.

The 'C' latch sets if the selected byte of R1 does not equal 0. The 'Z' latch sets if the selected byte of R1 equals 0.

AND Halfword Register (NHR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	1	1	0	0	0	0	0

Bytes 0 and 1 of the general register designated by R2 are ANDed with bytes 0 and 1 of the general register designated by R1. The result is placed in bytes 0 and 1 of R1.

The 'C' latch sets if bytes 0 and 1 of R1 are not equal to 0.

The 'Z' latch sets if bytes 0 and 1 of R1 equal 0.

Note: *If general register 0 (IAR) is specified as R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.*

AND Register (NR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	1	1	0	1	0	0	0

Bytes X, 0, and 1 of the general register designated by R2 are ANDed with bytes X, 0, and 1 of the general register designated by R1. The result is placed in R1.

The 'C' latch sets if bytes X, 0, and 1 of R1 are not equal to 0.

The 'Z' latch sets if bytes X, 0, and 1 of R1 equal 0.

Note: *If general register 0 (IAR) is specified as R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.*

Branch and Link Register (BALR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	0	1	0	0	0	0	0	0

This two-cycle instruction causes an unconditional branch to the storage address in the general register designated by R2. After the 'branch to' address is obtained from R2, and before it is placed in register 0 (IAR), the contents of register 0 are moved to the register specified by R1 to provide for subroutine linkage.

Since register 0 is the IAR, no linkage is provided if it is specified as R1. For the same reason, no branch occurs if it is specified as R2.

The 'C' and 'Z' latches are not changed.

Compare Character Register (CCR)

0	1-2	3	4	5-6	7	8	9	10	11	12	13	14	15
0	R2	N2	0	R1	N1	0	0	1	1	1	0	0	0

Byte 0 (N2=0) or byte 1 (N2=1) of the general register designated by R2 is compared with byte 0 (N1=0) or byte 1 (N1=1) of the general register designated by R1. The registers specified by R1 and R2 must be odd-numbered registers. The contents of the registers are not changed.

The 'C' latch sets if the selected byte of R1 is less than the selected byte of R2.

The 'Z' latch sets if the selected byte of R1 equals the selected byte of R2.

REGISTER TO REGISTER (RR) INSTRUCTIONS (PART 2 OF 3)

Compare Halfword Register (CHR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	0	1	1	0	0	0	0

Bytes 0 and 1 of the general register designated by R2 are compared with bytes 0 and 1 of the general register designated by R1. The contents of the registers are not changed.

The 'C' latch sets if bytes 0 and 1 of R1 are less than bytes 0 and 1 of R2.

The 'Z' latch sets if bytes 0 and 1 of R1 are equal to bytes 0 and 1 of R2.

Compare Register (CR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	0	1	1	1	0	0	0

Bytes X, 0, and 1 of R2 are compared with X, 0, and 1 of R1. The contents of the registers are not changed.

The 'C' latch sets if bytes X, 0, and 1 of R1 are less than bytes X, 0, and 1 of R2.

The 'Z' latch sets if bytes X, 0, and 1 are equal to bytes X, 0, and 1 of R2.

Exclusive-OR Character Register (XCR)

0	1-2	3	4	5-6	7	8	9	10	11	12	13	14	15
0	R2	N2	0	R1	N1	0	1	0	0	1	0	0	0

Byte 0 (N2=0) or byte 1 (N2=1) of the general register designated by R2 is exclusive-ORed with byte 0 (N1=0) or byte 1 (N1=1) of the general register designated by R1. The registers specified by R1 and R2 must be odd-numbered registers. The result is placed in the selected byte of R1.

The 'C' latch sets if the selected byte of R1 does not equal 0.

The 'Z' latch sets if the selected byte of R1 equals 0.

Exclusive-OR Halfword Register (XHR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	1	0	0	0	0	0	0

Bytes 0 and 1 of the general register designated by R2 are exclusive-ORed with bytes 0 and 1 of the general register designated by R1. The result is placed in bytes 0 and 1 of R1.

The 'C' latch sets if bytes 0 and 1 of R1 are not equal to 0.

The 'Z' latch sets if bytes 0 and 1 of R1 equal 0.

Note: *If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.*

Exclusive-OR Register (XR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	1	0	0	1	0	0	0

Bytes X, 0, and 1 of the general register designated by R2 are exclusive-ORed with bytes X, 0, and 1 of the general register designated by R1. The result is placed in R1.

The 'C' latch sets if bytes X, 0, and 1 of R1 do not equal 0.

The 'Z' latch sets if bytes X, 0, and 1 of R1 equal 0.

Note: *If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.*

Load Character Register (LCR)

0	1-2	3	4	5-6	7	8	9	10	11	12	13	14	15
0	R2	N2	0	R1	N1	0	0	0	0	1	0	0	0

Byte 0 (N2=0) or byte 1 (N2=1) of the general register designated by R2 is moved to byte 0 (N1=0) or byte 1 (N1=1) of the general register designated by R1. The registers specified by R1 and R2 must be odd-numbered registers.

The 'C' latch sets if the selected byte of R1 has an even number of data bits set to 1.

The 'Z' latch sets if the selected byte of R1 equals 0.

Load Character with Offset Register (LCOR)

0	1-2	3	4	5-6	7	8	9	10	11	12	13	14	15
0	R2	N2	0	R1	N1	0	1	1	1	1	0	0	0

Byte 0 (N2=0) or byte 1 (N2=1) of the register specified by the R2 field is shifted right one bit position and a 0 is inserted in the high-order bit position. The bit shifted out of position 7 is lost. The resulting byte is placed in the selected byte of R1. The non-selected byte of R1 remains unchanged. The registers specified by R1 and R2 must be odd-numbered registers.

The 'C' latch sets if the bit shifted out of bit position 7 of the selected byte of R2 is 1.

The 'Z' latch sets if the selected byte of R1 equals 0.

Load Halfword Register (LHR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	0	0	0	0	0	0	0

Bytes 0 and 1 of the general register designated by R2 are loaded into bytes 0 and 1 of the general register designated by R1.

The 'C' latch sets if bytes 0 and 1 of R1 do not equal 0.

The 'Z' latch sets if bytes 0 and 1 of R1 equal 0.

Note: *If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.*

Load Halfword with Offset Register (LHOR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	1	1	1	0	0	0	0

Bytes 0 and 1 of the general register designated by R2 are shifted right one bit position. A 0 is inserted in the high-order bit position. The resulting halfword is placed in byte 0 and 1 of R1.

The 'C' latch sets if the bit shifted out of bit 1.7 is 1.

The 'Z' latch sets if bytes 0 and 1 of R1 equal 0.

Note: *If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.*

REGISTER TO REGISTER (RR) INSTRUCTIONS (PART 3 OF 3)

Load Register (LR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	0	0	0	1	0	0	0

Bytes X, 0, and 1 of the general register designated by R2 are loaded into bytes X, 0, and 1 of R1.

The 'C' latch sets if bytes X, 0, and 1 of R1 do not equal 0.

The 'Z' latch sets if bytes X, 0, and 1 of R1 equal 0.

Note: *If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.*

Load with Offset Register (LOR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	1	1	1	1	0	0	0

Bytes X, 0, and 1 of the general register designated by R2 are shifted right one bit position. A 0 is inserted in the high-order bit position. The result is placed in bytes X, 0, and 1 of R1.

The 'C' latch sets if the bit shifted out of bit 1.7 is 1.

The 'Z' latch sets if bytes X, 0, and 1 of R1 equal 0.

Note: *If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches do not change.*

OR Character Register (OCR)

0	1-2	3	4	5-6	7	8	9	10	11	12	13	14	15
0	R2	N2	0	R1	N1	0	1	0	1	1	0	0	0

Byte 0 (N2=0) or byte 1 (N2=1) of the general register designated by R2 is ORed with byte 0 (N1=0) or byte 1 (N1=1) of the general register designated by R1. The registers specified by R1 and R2 must be odd-numbered registers. The result is placed in the selected byte of R1. The non-selected byte of R1 remains unchanged.

The 'C' latch sets if the selected byte of R does not equal 0.

The 'Z' latch sets if the selected byte of R1 equals 0.

OR Halfword Register (OHR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	1	0	1	0	0	0	0

Bytes 0 and 1 of the general register designated by R2 are ORed with bytes 0 and 1 of the general register designated by R1. The result is placed in bytes 0 and 1 of R1.

The 'C' latch sets if bytes 0 and 1 of R1 do not equal 0.

The 'Z' latch sets if bytes 0 and 1 of R1 equal 0.

Note: *If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.*

OR Register (OR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	1	0	1	1	0	0	0

Bytes X, 0, and 1 of the general register designated by R2 are ORed with bytes X, 0, and 1 of the general register designated by R1. The result is placed in bytes X, 0, and 1 of R1.

The 'C' latch sets if bytes X, 0, and 1 of R1 do not equal 0.

The 'Z' latch sets if bytes X, 0, and 1 of R1 equal 0.

Note: *If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.*

Subtract Character Register (SCR)

0	1-2	3	4	5-6	7	8	9	10	11	12	13	14	15
0	R2	N2	0	R1	N1	0	0	1	0	1	0	0	0

Byte 0 (N2=0) or byte 1 (N2-1) of the general register designated by R2 is subtracted from byte 0 (N1=0) or bytes 0 and 1 (N1=1) of the general register designated by R1. Before the subtraction is performed, the selected byte of R2 is expanded with high-order zeros to equal the size of the selected byte(s) of R1. The subtraction is performed by adding the two's complement of the selected byte(s) of R2 to the selected byte(s) of R1. The result is stored in the selected byte(s) of R1. If the difference is less than zero, the result is in two's complement form.

The 'C' latch sets if N=0 and the selected byte(s) of R1 are less than 0.

The 'Z' latch sets if N=1 and the selected byte(s) of R1 equal 0.

Subtract Halfword Register (SHR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	0	1	0	0	0	0	0

Bytes 0 and 1 of the general register designated by R2 are subtracted from bytes 0 and 1 of the general register designated by R1. The subtraction is performed by adding the two's complement of bytes 0 and 1 of R2 to bytes 0 and 1 of R1. The result is placed in bytes 0 and 1 of R1. If the difference is less than zero, the result is in two's complement form.

The 'C' latch sets if bytes 0 and 1 of R1 are less than 0.

The 'Z' latch sets if bytes 0 and 1 of R1 equal 0.

Note: *If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.*

Subtract Register (SR)

0	1-3	4	5-7	8	9	10	11	12	13	14	15
0	R2	0	R1	1	0	1	0	1	0	0	0

Bytes X, 0, and 1 of the general register designated by R2 are subtracted from bytes X, 0, and 1 of the general register designated by R1. The subtraction is performed by adding the two's complement of bytes X, 0, and 1 of R2 to bytes X, 0, and 1 of R2. The result is placed in R1. If the difference is less than zero, the result is in two's complement form.

The 'C' latch sets if bytes X, 0, and 1 of R1 are less than 0.

The 'Z' latch sets if bytes X, 0, and 1 of R1 equal 0.

Note: *If general register 0 (IAR) is R1, a branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed.*

RR Instruction Operation (Except BALR)

TAR is incremented by 2. This new address is used in the next instruction cycle.

Constants (+2) → X Force Constant 0002 (CF001) → True/Complement DF975 DG975 → X T0 + T1 Time Set A-B Reg (CC007) → A Register DF975 DG975

TAR DF971 DG971 → X Gate TAR to Y Bus (CS004)

X Gate Y Bus to B Reg (CS004) → X T0 + T1 Time Set A-B Reg (CC007) → B Register DF002 DG002

X Set SAR (CS007) → SAR DF971 DG971

A Register, B Register → ALU → DF008 DG008

SAR → (2) → Storage → (1)

DF008 DG008 → Z Register DF974 DG974

Z Register → X Write LS (CC006) → General Register (IAR)

Z Register → X Set TAR (CS007) → TAR DF971 DG971

DF002 DG002

TAR is incremented by two in ALU. This new address is placed in TAR and in the IAR.

Instruction	Operation
All RR type, except BALR	Add

See page 6-100

To Next Column

I1A

I1B

The data in the storage location addressed by SAR is loaded in the Op register and in SDR. The addresses in SAR and in the ADDRESS/DATA switches are compared. The ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE COMPARE switch on 1-060.)

(1) → X Gate Memory Byte to M Bus (CS005)

X Set Op Reg (CS007) → Op Register DN001

X Set SDR Byte (CS007) → SDR DN001

(2) → X Gate SAR to A Bus (CS004)

True/Complement DF975 DG975 → X T0 + T1 Time Set A-B Reg (CC007) → A Register DF975 DG975

Control Panel Switches AP001 → X T0 + T1 Time Set A-B Reg (CC007) → B Register DF002 DG002

A Register, B Register → ALU → DF008 DG008

ALU → Z Register DF974 DG974

Z Register → X Set DR 2 (CS007) → Display Register 2 DF003 DG003

Display Register 2 → X Gate Displ Reg 2 to Ind. (CU001) → Display B AP011 AP012

Instruction	Operation
All RR type, except BALR	Compare

See page 6-100.

Note: *See page 6-000 for data flow bit card locations.*

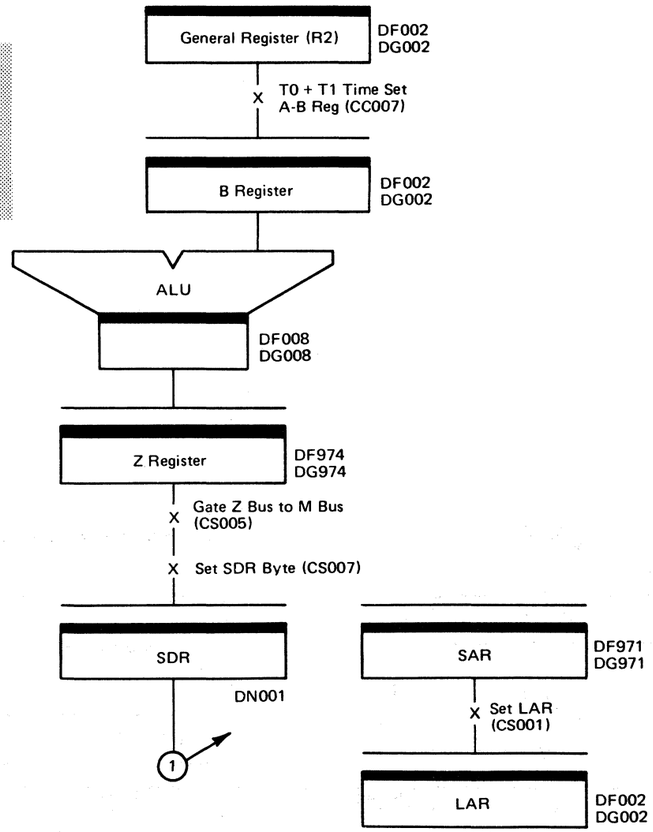
To Next Page

From Preceding Page

Applies to all RR instructions except BALR.

The contents of the general register addressed by the R2 field are loaded into SDR. For cross operations, the bytes are crossed by circuitry between ALU and the Z register.

I1C



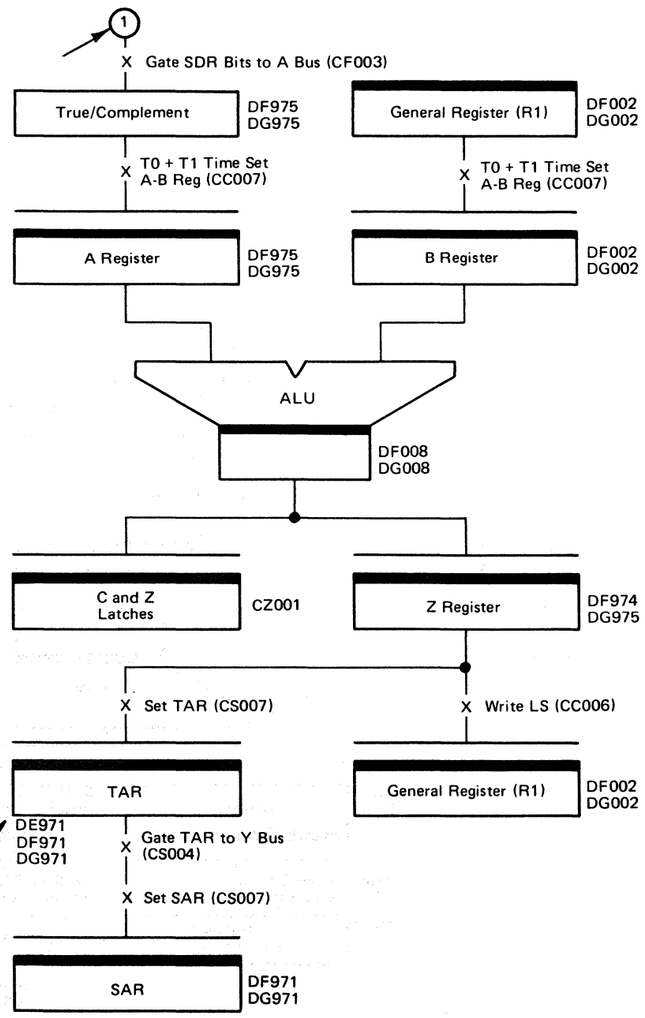
Instruction	Operation
ACR	Cross
AHR	B Reg Direct
AR	B Reg Direct
NCR	Cross
NHR	B Reg Direct
NR	B Reg Direct
CCR	Cross
CHR	B Reg Direct
CR	B Reg Direct
XCR	Cross
XHR	B Reg Direct
XR	B Reg Direct
LCR	Cross
LCOR	B Reg Direct
LHR	B Reg Direct
LHOR	B Reg Direct
LOR	B Reg Direct
LR	B Reg Direct
OCR	Cross
OHR	B Reg Direct
OR	B Reg Direct
SCR	Cross
SHR	B Reg Direct
SR	B Reg Direct

See page 6-100.

To Next Column

The specified bytes in SDR and general register R1 are gated to ALU. The ALU performs the operation specified by the instruction in the Op register and stores the results in the specified bytes of general register R1.

I1D



Instruction	Operation
ACR	Add
AHR	Add
AR	Add
NCR	And
NHR	And
NR	And
CCR	Compare
CHR	Compare
CR	Compare
XCR	Xor
XHR	Xor
XR	Xor
LCR	A Reg Direct
LCOR	Shift Right
LHR	A Reg Direct
LHOR	Shift Right
LOR	Shift Right
LR	A Reg Direct
OCR	Or
OHR	Or
OR	Or
SCR	Subtract
SHR	Subtract
SR	Subtract

See page 6-100

If R1 is general register 0 (IAR), the result is also placed in TAR. A branch to the address formed in register 0 occurs.

End of Instruction

Note: *See page 6-000 for data flow bit card locations.*

BALR Instruction Operation

TAR is incremented by 2. This new address is used in the next instruction cycle.

Constants (+2)
X Force Constant 0002 (CF001)
True/Complement DF975 DG975
X T0 + T1 Time Set A-B Reg (CC007)
A Register DF975 DG975

TAR DF971 DG971
X Gate TAR to Y Bus (CS004)
X Gate Y Bus to B Reg (CS004)
X T0 + T1 Time Set A-B Reg (CC007)
B Register DF002 DG002

X Set SAR (CS007)
SAR DF971 DG971
(2)
Storage
(1)

ALU
DF008 DG008
Z Register DF974 DG974
X Write LS (CC006)
X Set TAR (CS007)
General Register (IAR)
TAR DF971 DG971
DF002 DG002
TAR is incremented by two in ALU. This new address is placed in TAR and in the IAR.

Instruction	Operation
BLAR	Add

See page 6-100

I1A

To Next Column

The data in the storage location addressed by SAR is loaded in the Op register and in SDR. The addresses in SAR and in the ADDRESS/DATA switches are compared. The ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE COMPARE switch on 1-060.)

(1)
X Gate Memory Byte to M Bus (CS005)
X Set Op Reg (CS007)
Op Register DN001
X Set SDR Byte (CS007)
SDR DN001

(2)
X Gate SAR to A Bus (CS004)
True/Complement DF975 DG975
X T0 + T1 Time Set A-B Reg (CC007)
A Register DF975 DG975

Control Panel Switches AP001
X T0 + T1 Time Set A-B Reg (CC007)
B Register DF002 DG002

ALU
DF008 DG008
Z Register DF974 DG974
X Set DR 2 (CS007)
Display Register 2 DF003 DG003
X Gate Displ Reg 2 to Ind. (CU001)
Display B AP011 AP012

I1B

To Next Page

Instruction	Operation
BALR	Compare

See page 6-100.

Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

BALR Only

I1C

The address in SAR is gated to LAR.

SAR — DF971 DG971

X Set LAR (CS001)

LAR — DF002 DG002

BALR Only

I1D

The address in TAR is gated to SAR.

TAR — DF971 DG971

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DF971 DG971

BALR Only

I2A

The contents of general register R2 are placed in bytes X, 0, and 1 of SDR.

General Register (R2) — DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU

DF008 DG008

Instruction	Operation
BALR	B Reg Direct

See page 6-100.

Z Register — DF974 DG974

X Gate Z Bus to M Bus (CS005)

X Set SDR Byte (CS007)

SDR — DN001

BALR Only

I2B

The addresses in SAR and in the ADDRESS/DATA switches are compared, and the ADDRESS COMPARE light comes on if the address compare conditions are met. (See "LOAD/STORE ADDRESS COMPARE Switch" on page 1-060.)

SAR — DF971 DG971

X Gate SAR to A Bus (CS004)

True/Complement — DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

Control Panel Switches — AP001

X T0 + T1 Time Set A-B Reg (CC007)

X Gate Y Bus to B Reg (CS004)

A Register — DF975 DG975

B Register — DF002 DG002

ALU

DF008 DG008

Instruction	Operation
BALR	Compare

See page 6-100.

Z Register — DF974 DG974

X Set DR 2 (CS007)

Display Register 2 — DF003 DG003

X Gate Displ Reg 2 to Ind. (CU001)

Display B — AP011 AP012

Note: *See page 6-000 for data flow bit card locations.*

To Next Page

From Preceding Page

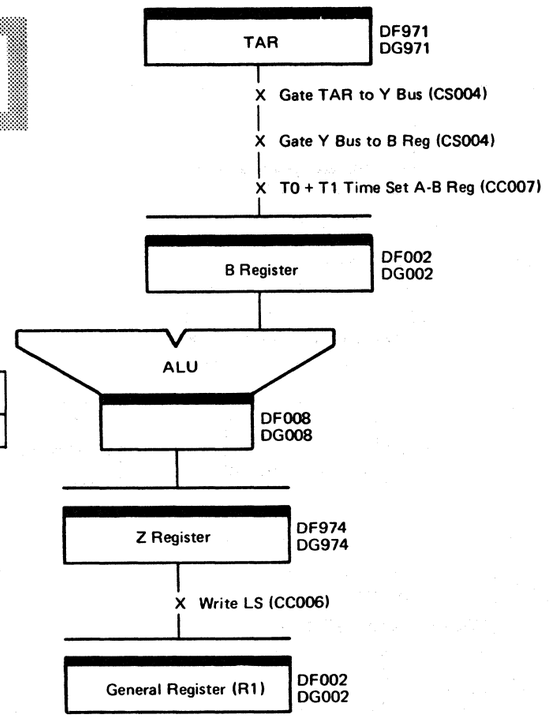
BALR Only

The address in TAR (same address as in IAR) is loaded in general register R1.

I2C

Instruction	Operation
BALR	B Reg Direct

See page 6-100.



To Next Column

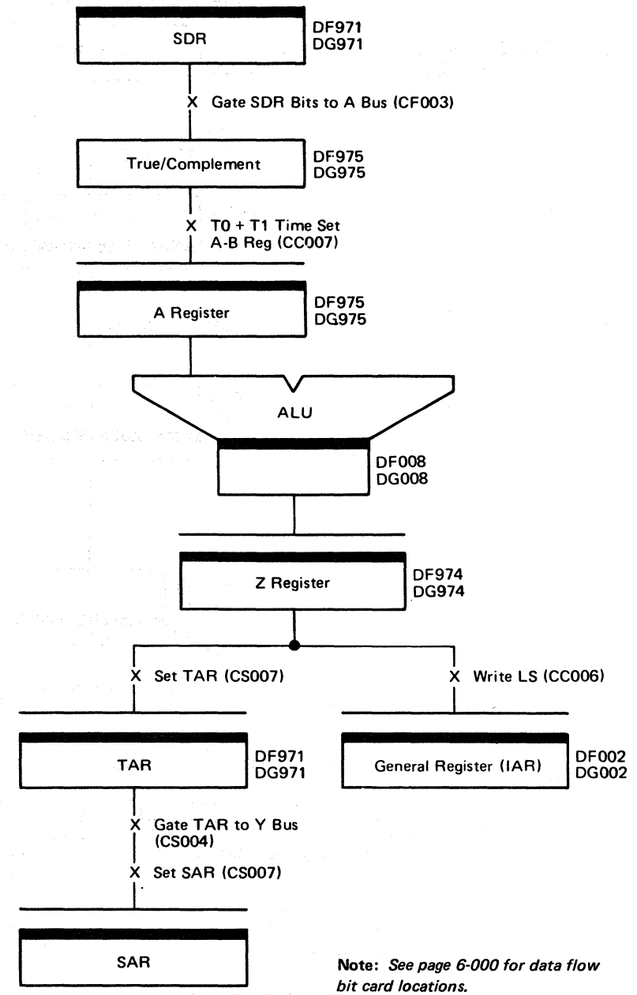
BALR Only

The contents of SDR (same as the contents of R2) are placed in TAR and IAR.

I2D

Instruction	Operation
BALR	A Reg Direct

See page 6-100.



Note: *See page 6-000 for data flow bit card locations.*

End of Instruction

REGISTER AND STORAGE (RS) INSTRUCTIONS

The CCU takes an I1 and an I2 machine cycle to execute the 'insert character', 'load halfword', 'store character', or 'store halfword' instruction. The 'load' and 'store' instructions each require an I1, I2, and I3 cycle.

For the 'insert character' and 'store character' instructions, the general register designated by the R field in the instruction must be odd-numbered, therefore the General Register = (2xR) +1.

Insert Character (IC)

0	1-3	4	5-6	7	8	9-15
0	B	1	R	N	0	D

The 18-bit base address in the general register specified by the B field is added to the displacement specified in the D field. The displacement can be 0 to +127 bytes. The addition forms an effective address that is used to address storage.

The byte at the effective storage address is loaded into byte 0 (N=0) or byte 1 (N=1) of the general register designated by the R field. The remaining bits of the register are unchanged. R must be an odd register.

The 'C' latch sets if the selected byte of R has an even number of 1 bits.

The 'Z' latch sets if the selected byte of R equals 0.

Note: *If general register 0 (IAR) is specified by B, a constant of X'0680' is used as the base address instead of the contents of register 0. This permits direct addressing of the 128 bytes starting at address X'0680' without having to load a base register.*

Load (L)

0	1-3	4	5-7	8	9-13	14	15
0	B	0	R	0	D	1	0

The 18-bit base address in the general register specified by the B field is added to the displacement in the D field. The displacement can be 0 to +31 fullwords. The addition forms an effective address that is used to address storage.

The low-order 18-bits of the fullword at the effective storage address are loaded into the general register specified by the R field. (The high-order 14 bits in the storage address are ignored.) The low-order bit of the effective address is ignored since storage is addressed on halfword boundaries.

The 'C' latch sets if bytes X, 0, and 1 of R do not equal 0.

The 'Z' latch sets if bytes X, 0, and 1 of R equal 0.

Note: *If general register 0 (IAR) is specified by R, an unconditional branch to the address formed in register 0 occurs. The 'C' and 'Z' latches are not changed. If general register 0 is specified by B, X'0780' is used as the base address instead of the contents of register 0. This permits direct addressing of the 32 fullwords starting at address X'0780' without having to load a base register.*

Load Halfword (LH)

0	1-3	4	5-7	8	9-14	15
0	B	0	R	0	D	1

The 18-bit base address in the general register specified by the B field is added to the displacement specified by the D field. The displacement can be 0 to +63 halfwords. This addition forms an effective address that is used to address storage.

The halfword at the effective storage address is loaded into bytes 0 and 1 of the register specified by the R field. The low-order bit of the effective address is ignored since storage is addressed on halfword boundaries.

Byte X of the register specified by R is set to zero during the load operation.

The 'C' latch sets if bytes 0 and 1 of R do not equal 0.

The 'Z' latch sets if bytes 0 and 1 of R equal 0.

The Load Halfword instruction is also used in conjunction with the Input X'7B' instruction to generate the new BSC-CRC character. When this instruction is executed at program level 2, 3, 4, or 5, or level 1 during IPL phase 3, the halfword accessed is loaded into both the specified general register and the BSC-CRC register. For non-CRC operation, the loading of data into the BSC-CRC register serves no purpose.

Note: *If general register 0 (IAR) is specified by the R field, an unconditional branch to the address formed in register 0 occurs. The condition codes are not changed. If general register 0 is specified by B, X'0700' is used as the base address instead of the contents of general register 0. This permits direct addressing of the 64 halfwords starting at address X'0700' without having to load a base register.*

Store (ST)

0	1-3	4	5-7	8	9-13	14	15
0	B	0	R	1	D	1	0

The 18-bit base address in the general register specified by the B field is added to the displacement specified by the D field. The displacement can be 0 to +31 fullwords. The addition forms the effective address used to address storage.

Bytes X, 0, and 1 of the general register specified by the R field are stored in the low-order 18 bits of the fullword located at the effective address. The high-order 14 bits are not affected. The low-order bit of the effective address is ignored since storage is addressed on halfword boundaries.

The 'C' and 'Z' latches are not changed.

Note: *If general register 0 (IAR) is specified by B, X'0780' is used as the base address instead of the contents of register 0. This permits direct addressing of the 32 fullwords starting at address X'0780' without having to load a base register.*

Special Case: A 'store' instruction must be located at storage location X'0010'. The R field and B field of this instruction both equal 0. This is the first instruction executed when a program level 1 interrupt occurs. During I1A time of the store instruction, the gate 'Write LS' is blocked in order to preserve the IAR of program level 2. During I3D time of the instruction, the storage location X'0012' is forced onto the Indata Bus to address the next storage instruction.

Store Character (STC)

0	1-3	4	5-6	7	8	9-15
0	B	1	R	N	1	D

The 18-bit base address in the general register specified by the B field is added to the displacement specified by the D field. The displacement can be 0 to +127 bytes. The addition forms an effective address that is used to address storage.

Byte 0 (N=0) or byte 1 (N=1) of the general register specified by the R field is stored at the effective storage address. R must be an odd register.

The 'C' and 'Z' latches are not changed.

Note: *If general register 0 (IAR) is specified by B, X'0680' is used as the base address instead of the contents of register 0. This permits direct addressing of the 128 bytes starting at address X'0680' without having to load a base register.*

Store Halfword (STH)

0	1-3	4	5-7	8	9-14	15
0	B	0	R	1	D	1

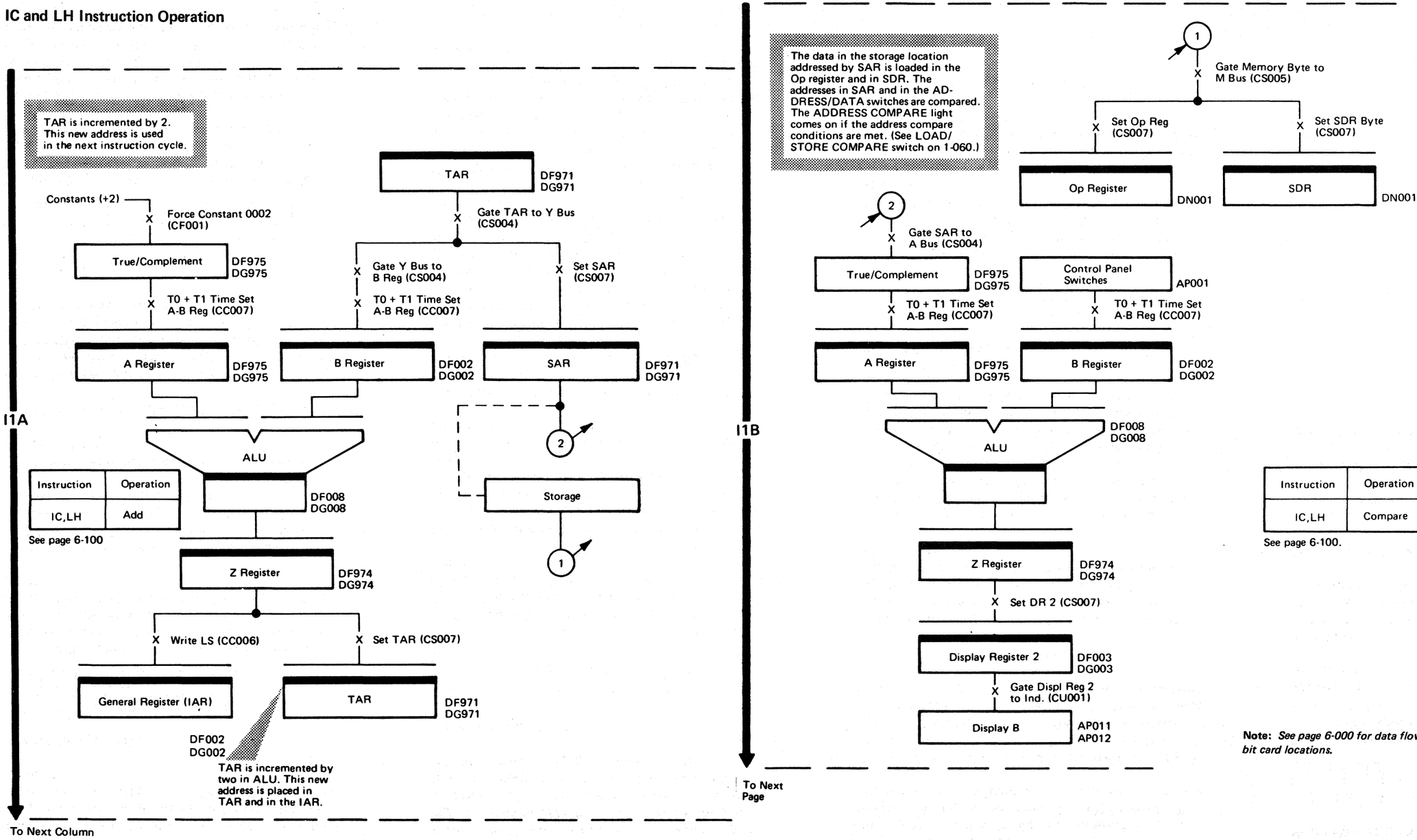
The 18-bit base address in the general register designated by the B field is added to the displacement specified by the D field. The displacement can be 0 to +63 halfwords. The addition forms an effective address that is used to address storage.

Byte 0 and 1 of the general register designated by the R field are stored at the effective address. The low-order bit of the effective address is ignored since storage is addressed on halfword boundaries.

The 'C' and 'Z' latches are not changed.

Note: *If general register 0 (IAR) is specified by B, X'0700' is used as the base address instead of the contents of register 0. This permits direct addressing of the 64 halfwords starting at address X'0700' without having to load a base register. If the R field is zero, X'0000' is stored at the storage address instead of the contents of register 0.*

IC and LH Instruction Operation



Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

IC and LH Only

I1C

The address in SAR is gated to LAR.

SAR — DF971 DG971

X Set LAR (CS001)

LAR — DF002 DG002

IC and LH Only

I1D

The D field (now in SDR) is added to general register B by the ALU. The result is gated to TAR and is used as the next storage address. If general register 0 (IAR) is B, a constant is used as the base address. (See the description of the specific instruction.)

SDR — DN001

X Gate SDR Bits to A Bus (CF003)

True/Complement — DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DF975 DG975

General Register (B) — DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU

DF008 DG008

Z Register — DF974 DG974

X Set TAR (CS007)

TAR — DF971 DG971

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DF971 DG971

(1)

Instruction	Operation
IC	Add
LH	Add

See page 6-100.

To Next Column

IC and LH Only

I2A

For an IC instruction, the byte of general register R that is not specified by N is loaded into the SDR. This byte is duplicated in the other byte of SDR.

For an LH instruction, the contents of general register R are loaded into SDR. (See the description of the specific instruction.)

(1) — Storage

A

To next page.

General Register (R) — DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU

DF008 DG008

Z Register — DF974 DG974

X Gate Z Bus to M Bus (CS005)

X Set SDR Byte (CS007)

SDR — DN001

Instruction	Operation
IC	Cross
LH	B Reg Direct

See page 6-100.

To Next Page

Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

IC and LH Only

The data in the storage location addressed by SAR is loaded into SDR. The addresses in SAR and in the ADDRESS/DATA switches are compared, and the ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE ADDRESS COMPARE switch on 1-060.)

From preceding page

A

X Gate Mem Byte to M Bus (CS005)

X Set SDR Byte (CS007)

SDR — DN001

1

SAR — DF971 DG971

X Gate SAR to A Bus (CS004)

True/Complement — DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DF975 DG975

Control Panel Switches — AP001

X T0 + T1 Time Set A-B Reg (CC007)

X Gate Y Bus to B Reg (CS004)

B Register — DF002 DG002

ALU

DF008 DG008

Instruction	Operation
IC	Compare
LH	Compare

See page 6-100.

Z Register — DF974 DG974

X Set DR 2 (CS007)

Display Register 2 — DF003 DG003

X Gate Displ Reg 2 to Ind (CU001)

Display B — AP011 AP012

Note: *If SAR bit 1.7 is on, set SDR byte 1 (Condition Set SDR Byte 1, CS002). If SAR bit 1.7 is off, set SDR byte 0 (Condition Set SDR Byte 0, CS002).*

I2B

To Next Column

IC and LH Only

The data in SDR is loaded in the selected byte(s) of general register R.

For an IC instruction, ALU does a cross operation if the byte from storage (in SDR) is not the same byte (0 or 1) as the selected byte of general register R.

1

X Gate SDR Bits to A Bus (CF003)

True/Complement — DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DF975 DG975

ALU

DF008 DG008

I2C

Instruction	Operation
IC	A Reg Direct or Cross A Reg Direct
LH	A Reg Direct

See page 6-100.

C and Z Latches — CZ001

Z Register — DF974 DG974

X Write LS (CC006)

General Register (R) — DF002 DG002

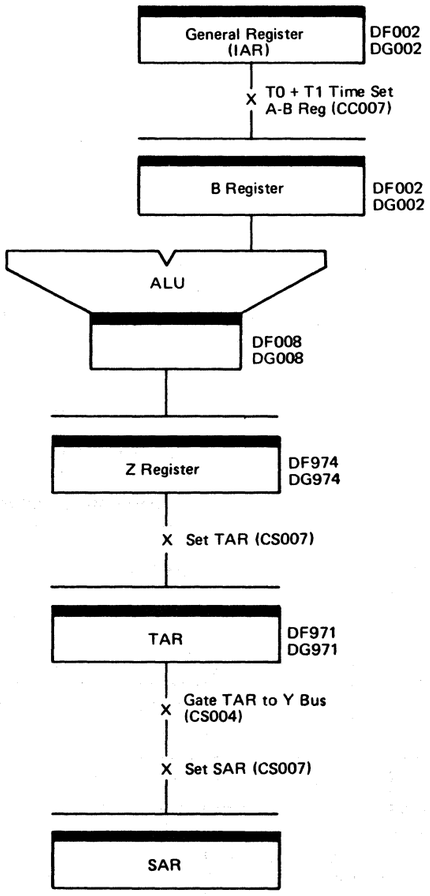
To Next Page

Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

IC and LH Only

The address of the next instruction is loaded into TAR from IAR.



Instruction	Operation
IC	B Reg Direct
LH	B Reg Direct

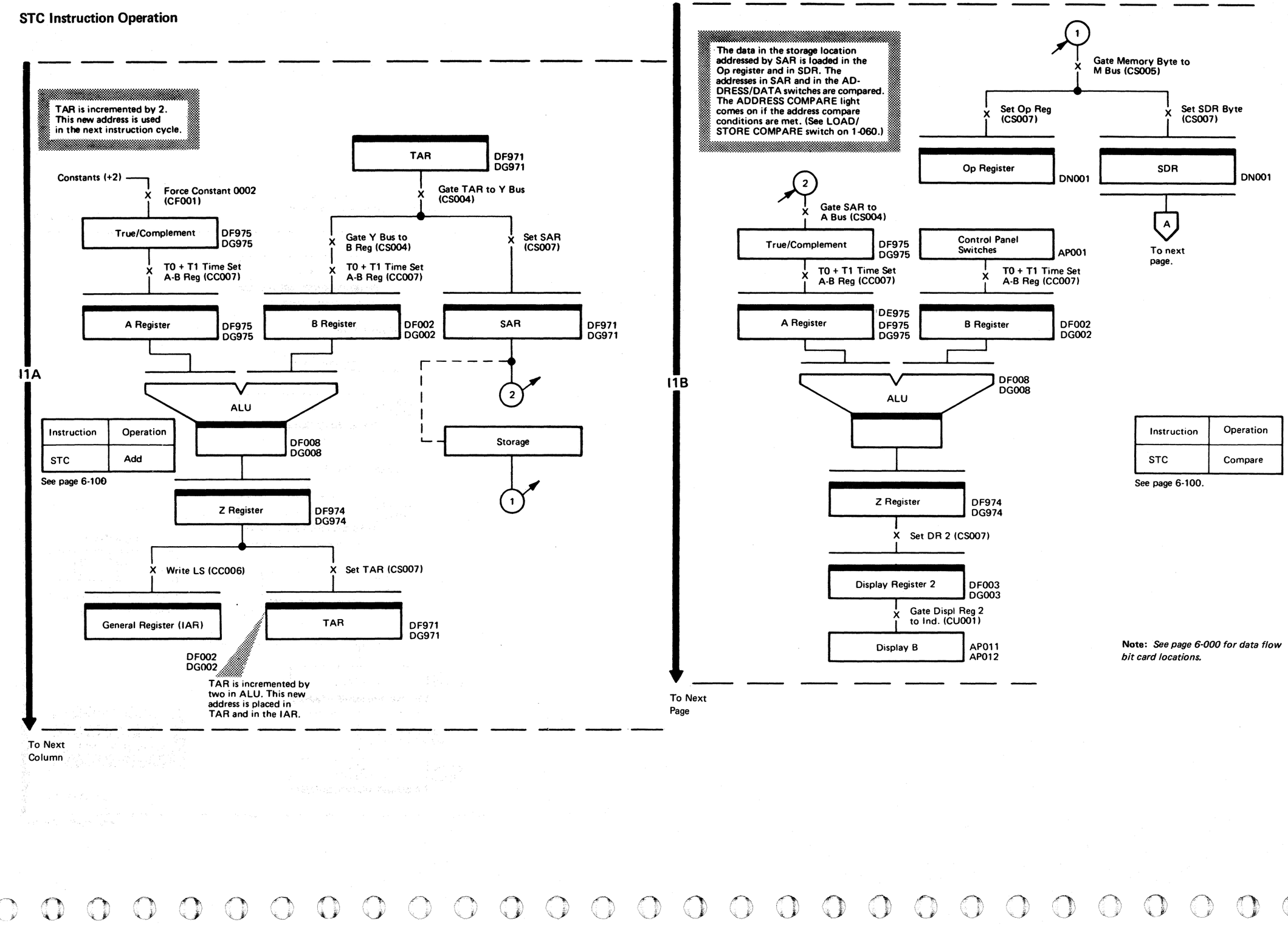
See page 6-100.

I2D

End of Instruction

Note: *See page 6-000 for data flow bit card locations.*

STC Instruction Operation



Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

STC Only

I1C

The address in SAR is gated to LAR.

SAR — DF971 DG971

X Set LAR (CS001)

LAR — DF002 DG002

STC Only

From Preceding Page

The D field (now in SDR) is added to general register B by ALU. The result is gated to TAR and is used as the next storage address. If general 0 (IAR) is specified as B, a constant is used as the base address. (See the description of the specific instruction.)

A

X Gate SDR Bits to A Bus (CF003)

True/Complement — DF975 DG975

General Register (B) — DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DF975 DG975

B Register — DF002 DG002

ALU

DF008 DG008

Z Register — DF974 DG974

X Set TAR (CS007)

TAR — DF971 DG971

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DF971 DG971

1

I1D

Instruction	Operation
STC	Add

See page 6-100.

To Next Column

STC Only

I2A

The byte specified by N is duplicated in both bytes of SDR. (See the description of the instruction for special cases.)

1

Storage

A

To next page

General Register (R) — DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU

DF008 DG008

Z Register — DF974 DG974

X Gate Z Bus to M Bus (CS005)

X Set SDR Byte (CS007)

SDR — DN001

Instruction	Operation
STC	Cross

See page 6-100.

To Next Page

Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

STC Only

The byte of the storage location that is not specified by the B field is placed in the same byte of SDR. Bytes 0 and 1 of SDR are then stored at the storage address. The addresses in SAR and in the ADDRESS/DATA switches are compared, and the ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE ADDRESS COMPARE switch on page 1-060.)

I2B

SAR — DF971 DG971

1 — X Gate SAR to A Bus (CS004)

True/Complement — DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

Control Panel Switches — AP001

X T0 + T1 Time Set A-B Reg (CC007)

X Gate Y Bus to B Reg (CS004)

From Preceding Page — A

X Gate Mem Byte to M Bus (CS005)

X Set SDR Byte (CS007)

A Register — DF975 DG975

B Register — DF002 DG002

SDR — DN001

ALU

DF008 DG008

Instruction	Operation
STC	B Reg Direct

See page 6-100.

Storage — 1

Z Register — DF974 DG974

X Set DR2 (CS007)

Display Register 2 — DF003 DG003

X Gate Displ Reg 2 to Ind (CU001)

Display B — AP011 AP012

To Next Column

I2C

No Action

STC Only

The address of the next instruction is loaded into TAR from IAR.

I2D

Instruction	Operation
STH	B Reg Direct

See page 6-100.

General Register (IAR) — DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU

DF008 DG008

Z Register — DF974 DG974

TAR — DF971 DG971

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

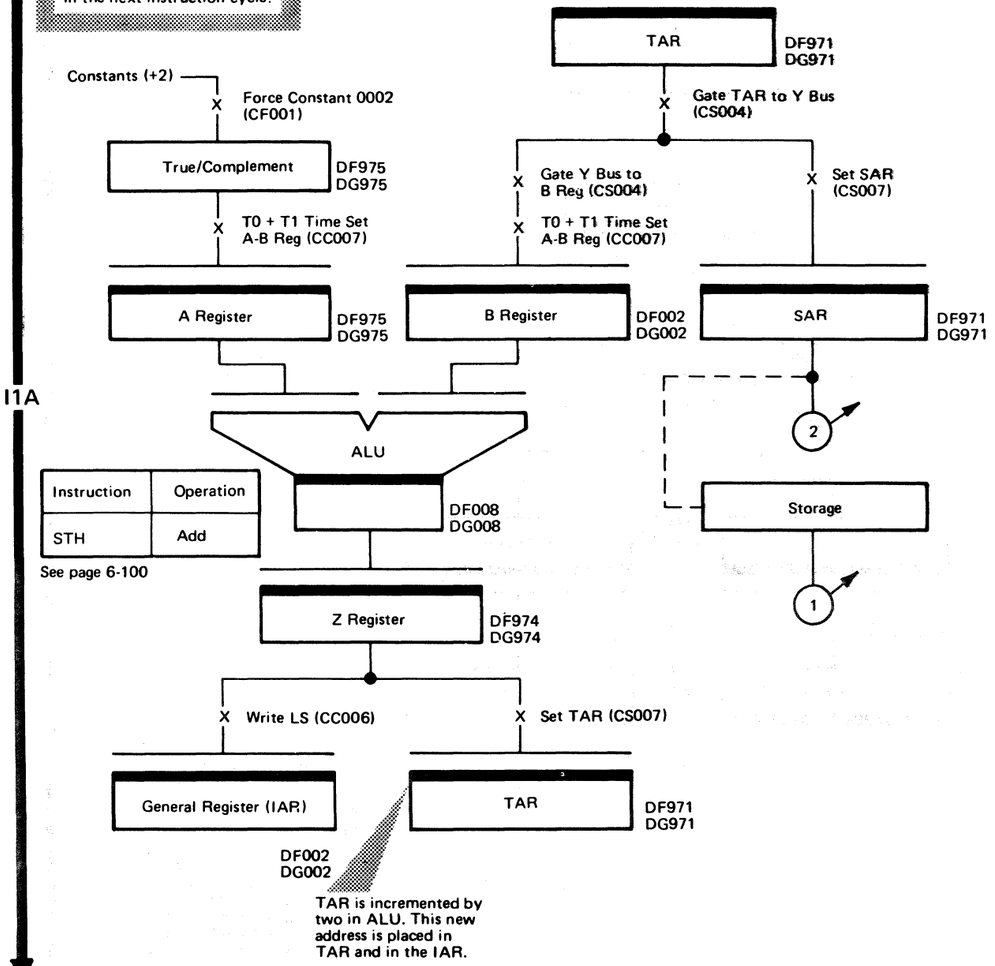
SAR — DF971 DG971

End of Instruction

Note: *See page 6-000 for data flow bit card locations.*

STH Instruction Operation

TAR is incremented by 2. This new address is used in the next instruction cycle.

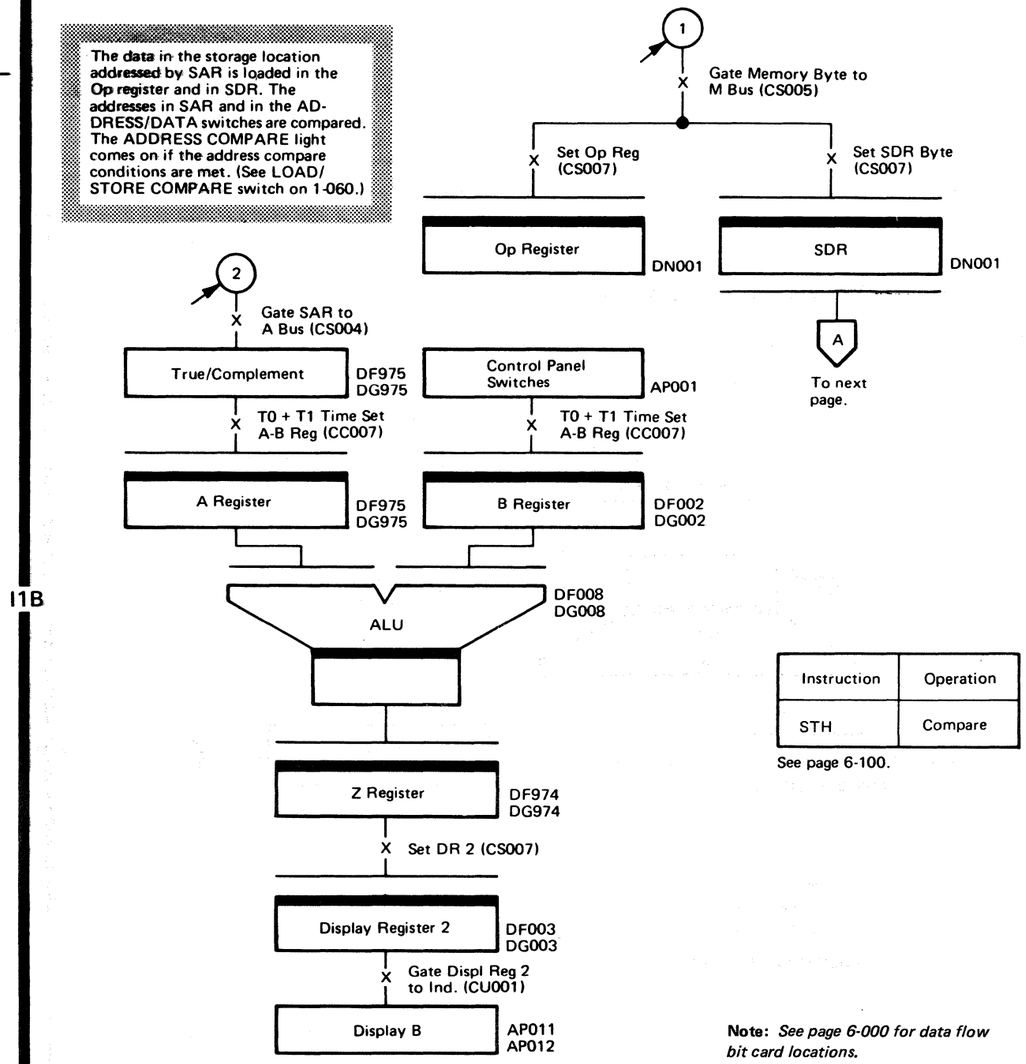


I1A

To Next Column

I1B

The data in the storage location addressed by SAR is loaded in the Op register and in SDR. The addresses in SAR and in the ADDRESS/DATA switches are compared. The ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE COMPARE switch on 1-060.)



To Next Page

Instruction	Operation
STH	Compare

See page 6-100.

Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

STH Only

I1C

No Action

STH Only

The D field (now in SDR) is added to general register B by ALU. The result is gated to TAR and is used as the next storage address. If general register 0 (IAR) is B, a constant is used as the base address. (See the description of the instruction.)

From Preceding Page

A

X Gate SDR Bits to A Bus (CF003)

True/Complement — DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DF975 DG975

General Register (B) — DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU

DF008 DG008

Z Register — DF974 DG974

X Set TAR (CS007)

TAR — DE971 DF971 DG971

X Gate TAR to Y Bus (CS004)

SAR — DF971 DG971

1

Instruction	Operation
STH	Add

See page 6-100.

I1D

To Next Column

STH Only

The data in byte 0 and 1 of the R field is gated to the SDR.

I2A

1

Storage

A

To next page

General Register (R) — DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU

DF008 DG008

Z Register — DF974 DG974

X Gate Z Bus to M Bus (CC005)

Set SDR Byte (CS007)

SDR — DN001

Instruction	Operation
STH	B Reg Direct

See page 6-100.

Note: *See page 6-000 for data flow bit card locations.*

To Next Page

From Preceding Page

STH Only

The data in SDR (from general register R) is stored in the storage location addressed by the effective address. The addresses in SAR and in the ADDRESS/DATA switches are compared, and the ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE ADDRESS COMPARE switch on 1-060.)

From Preceding Page

A

X Gate Mem Byte to M Bus (CS005)

X Set SDR Byte (CS007)

SDR — DN001

Storage

2

SAR — DF971 DG971

2

X Gate SAR to A Bus (CS004)

True/Complement — DF975 DG975

X T0 + T1 Time Set A-B Reg (CS007)

A Register — DF975 DG975

Control Panel Switches — AP001

X T0 + T1 Time Set A-B Reg (CC007)

X Gate Y Bus to B Reg (CS004)

B Register — DF002 DG002

ALU

DF008 DG008

Instruction	Operation
STH	Compare

See page 6-100.

Z Register — DF974 DG974

X Set DR2 (CS007)

Display Register 2 — DF003 DG003

X Gate Displ Reg 2 to Ind (CU001)

Display B — AP011 AP012

I2B

To Next Column

I2C

No Action

STH Only

The address of the next instruction is loaded into TAR from IAR.

Instruction	Operation
STH	B Reg Direct

See page 6-100.

General Register (IAR) — DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU

DF008 DG008

Z-Register — DF974 DG974

TAR — DF971 DG971

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DF971 DG971

I2D

End of Instruction

Note: *See page 6-000 for data flow bit card locations.*

Load Instruction Operation

TAR is incremented by 2. This new address is used in the next instruction cycle.

Constants (+2)
X Force Constant 0002 (CF001)
True/Complement DF975 DG975
X T0 + T1 Time Set A-B Reg (CC007)
A Register DF975 DG975

TAR DF971 DG971
X Gate TAR to Y Bus (CS004)
X Gate Y Bus to B Reg (CS004)
X T0 + T1 Time Set A-B Reg (CC007)
B Register DF002 DG002

X Set SAR (CS007)
SAR DF971 DG971
(2)
Storage
(1)

ALU
DF008 DG008

Instruction	ALU Operation
Load	Add

See page 6-100

Z Register DF974 DG974
X Write LS (CC006)
X Set TAR (CS007)
General Register (IAR)
TAR DF971 DG971
DF002 DG002
TAR is incremented by two in ALU. This new address is placed in TAR and in the IAR.

To Next Column

I1A

I1B

The data in the storage location addressed by SAR is loaded in the Op register and in SDR. The addresses in SAR and in the ADDRESS/DATA switches are compared. The ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE COMPARE switch on 1-060.)

(1)
X Gate Memory Byte to M Bus (CS005)
X Set Op Reg (CS007)
Op Register DN001
X Set SDR Byte (CS007)
SDR DN001

(2)
X Gate SAR to A Bus (CS004)
True/Complement DF975 DG975
X T0 + T1 Time Set A-B Reg (CC007)
A Register DF975 DG975

Control Panel Switches AP001
X T0 + T1 Time Set A-B Reg (CC007)
B Register DF002 DG002

ALU
DF008 DG008

Instruction	ALU Operation
Load	Compare

See page 6-100.

Z Register DF974 DG974
X Set DR 2 (CS007)
Display Register 2 DF003 DG003
X Gate Displ Reg 2 to Ind. (CU001)
Display B AP011 AP012

Note: *See page 6-000 for data flow bit card locations.*

To Next Page

From Preceding Page

I1C

Load Only

The address in SAR is gated to LAR.

SAR — DF971 DG971

X Set LAR (CS001)

LAR — DF002 DG002

I1D

Load Only

The D field (now in SDR) is added to general register B by ALU. The result is gated to TAR and is used as the next storage address. If general register 0 (IAR) is specified by the B field, a constant is used as the base address. (See the description of this instruction.)

SDR — DN001

X Gate SDR Bits to A Bus (CF003)

True/Complement — DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DF975 DG975

General Register (B) — DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU

DF008 DG008

Instruction	Operation
Load	Add

See Page 6-100.

Z Register — DF974 DG974

X Set TAR (CS007)

TAR — DF971 DG971

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DF971 DG971

(1)

To Next Column

I2A

Load Only

The address in SAR is used to address storage.

(1) — Byte X — Storage

(2)

Load Only

The data in byte X of the addressed storage location is loaded into byte X of SDR. The addresses in SAR and in the ADDRESS/DATA switches are compared, and the ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE ADDRESS COMPARE switch on 1-060.)

(2)

X Gate Mem Byte to M Bus (CS005)

X Set SDR Byte (CS007)

SDR — DN001

I2B

(1)

X Gate SAR To A Bus (CS004)

True/Complement — DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DF975 DG975

Control Panel Switches — AP001

X T0 + T1 Time Set A-B Reg (CC007)

X Gate Y Bus to B Reg (CS004)

B Register — DF002 DG002

ALU

DF008 DG008

Instruction	Operation
ST	Add

See Page 6-100.

Z Register — DF974 DG974

X Set DR 2 (CS007)

Display Register 2 — DF003 DG003

X Gate Displ Reg 2 to Ind. (CU001)

Display B — AP011 AP012

To Next Page

Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

I2C Load Only No Action

I2D

Load Only

The address in TAR is incremented by 2.

Constant (+2)
X Force Constant 0002 (CF001)
True/Complement DF975 DG975
X T0 + T1 Time Set A-B Reg (CC007)
A Register DF975 DG975

TAR DF971 DG971
X Gate TAR to Y Bus (CS004)
X Gate Y Bus to B Reg (CS004)
X T0 + T1 Time Set A-B Reg (CC007)
B Register DF002 DG002

ALU
DF008 DG008
Z Register DF974 DG974
X Set TAR (CS007)
TAR DF971 DG971
X Gate TAR to Y Bus (CS004)
X Set SAR (CS007)
SAR DF971 DG971
(1)

Instruction	Operation
Load	Add

See page 6-100.

To Next Column

I3A

Load Only

The address in SAR is used to address storage.

(1) Storage
Bytes 0 and 1
(2)

I3B

Load Only

The data in bytes 0 and 1 of the addressed storage location is loaded into bytes 0 and 1 of SDR. The addresses in SAR and in the ADDRESS/DATA switches are compared, and the ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE ADDRESS COMPARE switch on 1-060.)

(1)
X Gate SAR To A Bus (CS004)
True/Complement DF975 DG975
X T0 + T1 Time Set A-B Reg (CC007)
A Register DF975 DG975

Control Panel Switches AP001
X T0 + T1 Time Set A-B Reg (CC007)
X Gate Y Bus to B Reg (CS004)
B Register DF002 DG002

ALU
DF008 DG008
Z Register DF974 DG974
X Set DR 2 (CS007)
Display Register 2 DF003 DG003
X Gate Displ Reg 2 to Ind. (CU001)
Display B AP011 AP012

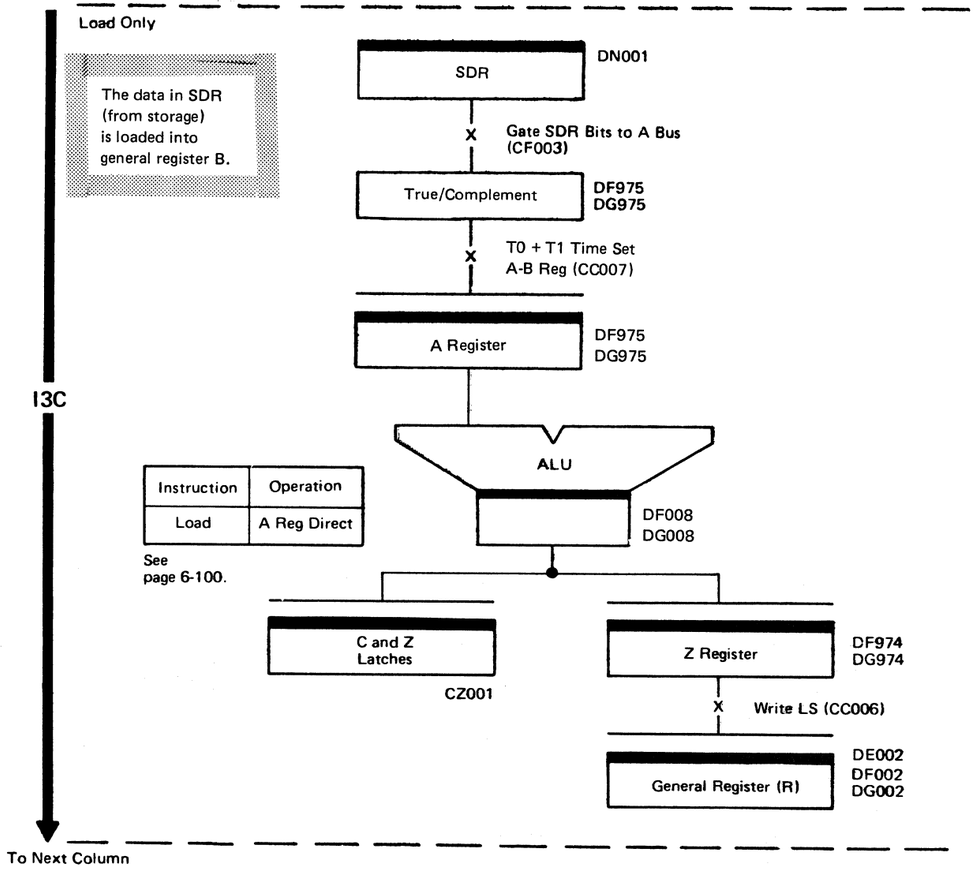
(2)
X Gate Mem Byte to M Bus (CS005)
X Set SDR Byte (CS007)
SDR DN001

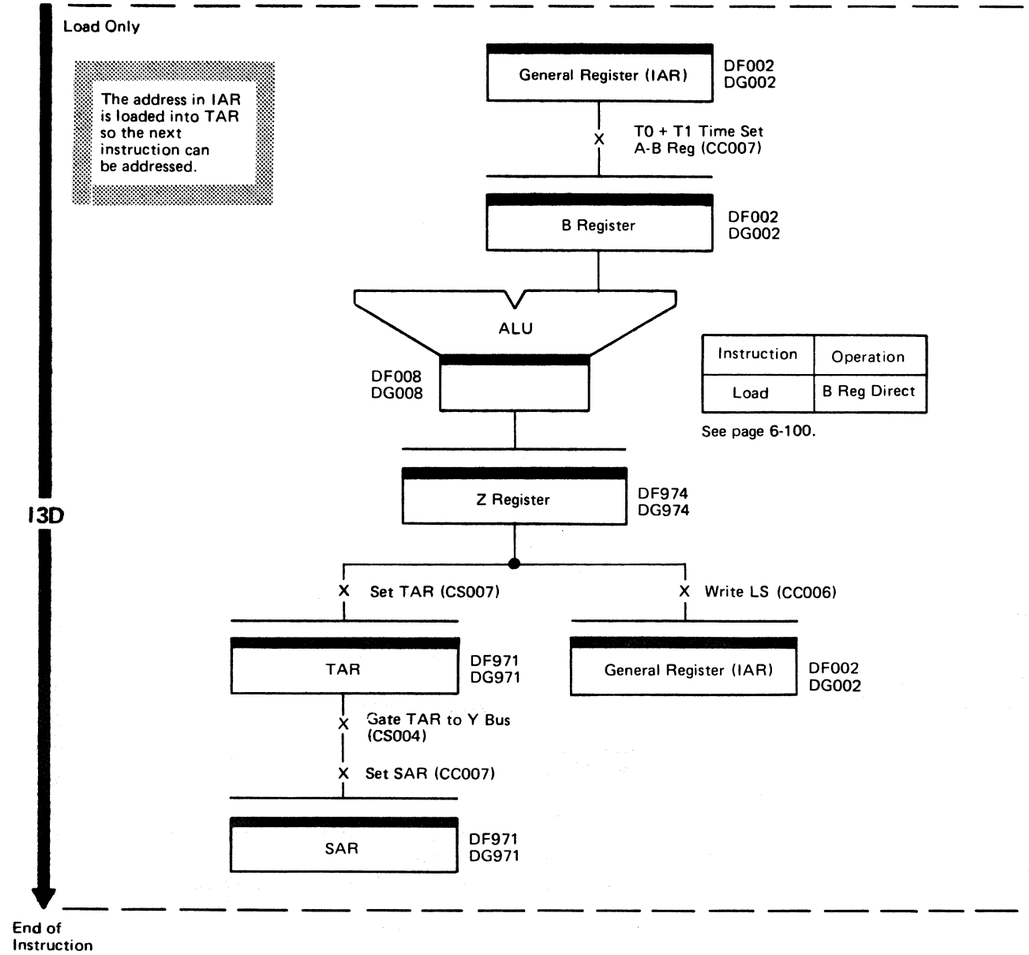
Instruction	Operation
Load	Compare

See page 6-100.

To Next Page

Note: *See page 6-000 for data flow bit card locations.*





Note: *See page 6-000 for data flow bit card locations.*

Store Instruction Operation

TAR is incremented by 2. This new address is used in the next instruction cycle.

The address exception checks made during each instruction cycle are not shown. See ALD pages CM002 and CM003.

TAR — DF971, DG971

Constants (+2) → X Force Constant 0002 (CF001) → True/Complement — DF975, DG975 → X T0 + T1 Time Set A-B Reg (CC007) → A Register — DE975, DF975, DG975

TAR → X Gate TAR to Y Bus (CS004)

X Gate Y Bus to B Reg (CS004) → X T0 + T1 Time Set A-B Reg (CC007) → B Register — DF002, DG002

X Set SAR (CS007) → SAR — DF971, DG971

A Register, B Register → ALU → DF008, DG008

SAR → (2) → Storage → (1)

Instruction	ALU Operation
Store	Add

See page 6-100

DF008, DG008 → Z Register — DF974, DG974

This gate is blocked during the first store instruction of a program level 1 interrupt. (See page 6-270.)

Z Register → X Write LS (CC006) → General Register (IAR) — DE002, DF002, DG002

Z Register → X Set TAR (CS007) → TAR — DF971, DG971

TAR is incremented by two in ALU. This new address is placed in TAR and in the IAR.

I1A

To Next Column

I1B

The data in the storage location addressed by SAR is loaded in the Op register and in SDR. The addresses in SAR and in the ADDRESS/DATA switches are compared. The ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE COMPARE switch on 1-060.)

(1) → X Gate Memory Byte to M Bus (CS005)

X Set Op Reg (CS007) → Op Register — DN001

X Set SDR Byte (CS007) → SDR — DN001

SDR → (A) To next page.

(2) → X Gate SAR to A Bus (CS004)

True/Complement — DF975, DG975 → X T0 + T1 Time Set A-B Reg (CC007) → A Register — DF975, DG975

Control Panel Switches — AP001 → X T0 + T1 Time Set A-B Reg (CC007) → B Register — DF002, DG002

A Register, B Register → ALU — DF008, DG008

ALU → Z Register — DF974, DG974

Z Register → X Set DR 2 (CS007) → Display Register 2 — DF003, DG003

Display Register 2 → X Gate Displ Reg 2 to Ind. (CU001) → Display B — AP011, AP012

Instruction	ALU Operation
Store	Compare

See page 6-100.

To Next Page

Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

I1C

Store Only

The address in SAR is gated to LAR.

SAR — DF971 DG971

X Set LAR (CS001)

LAR — DF002 DG002

Store Only

The D field (now in SDR) is added to general register B by the ALU. The result is gated to TAR and is used as the next storage address. If general register 0 (IAR) is B, a constant is used as the base address. (See the description of the instruction.)

From Preceding Page

A

X Gate SDR Bits to A Bus (CF003)

True/Complement — DE975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DF975 DG975

General Register (B) — DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU

DF008 DG008

Instruction	Operation
ST	Add

See page 6-100.

Z Register — DF974 DG974

X Set TAR (CS007)

TAR — DF971 DG971

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DF971 DG971

1

I1D

To Next Column

Store Only

The data in general register R is loaded in the SDR. See the description of the store instruction for information on what happens if R is the IAR.

1 — Storage

Instruction	Operation
ST	B Reg Direct

See page 6-100.

I2A

To Next Page

General Register (R) — DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU

DF008 DG008

Z Register — DF974 DG974

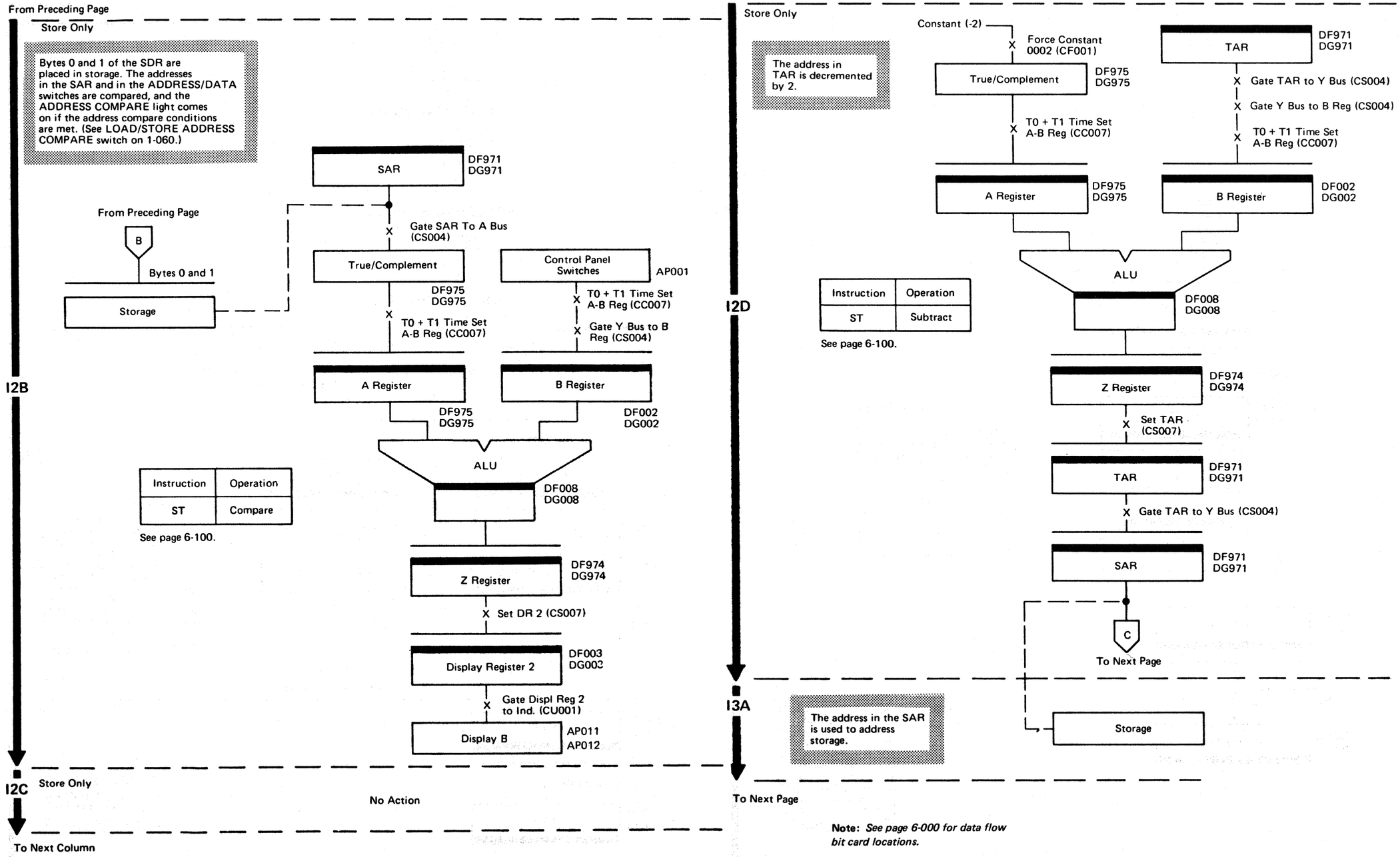
X Set SDR Byte (CS007)

SDR — DN001

Byte X — A — To page 6-460

Bytes 0 and 1 — B — To Next Page

Note: *See page 6-000 for data flow bit card locations.*



Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

Store Only

Byte X of SDR is stored in the storage location addressed by the SAR. The addresses in the SAR and in the ADDRESS/DATA switches are compared, and the ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE ADDRESS COMPARE switch on 1-060.)

From Preceding Page

C

X Gate SAR To A Bus (CS004)

Control Panel Switches — AP001

True/Complement — DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

X T0 + T1 Time Set A-B Reg (CC007)

X Gate Y Bus to B Reg (CS004)

From Page 6-440

A

I3B

A Register — DF975 DG975

B Register — DF002 DG002

Byte X

Storage

ALU

DF008 DG008

Instruction	Operation
ST	Compare

See page 6-100.

Z Register — DF974 DG974

X Set DR 2 (CS007)

Display Register 2 — DF003 DG003

X Gate Displ Reg 2 to Ind. (CU001)

Display B — AP011 AP012

To Next Column

I3C

Store Only

No Action

Store Only

The data in register 0 (IAR) is loaded into the TAR and back into the IAR.

I3D

Instruction	Operation
ST	B Reg Direct

See page 6-100.

General Register (IAR) — DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU

DF008 DG008

Z Register — DF974 DG974

X Set TAR (CS007)

X Write LS (CC006)

TAR — DF971 DG971

General Register (IAR) — DF002 DG002

Force interrupt address X'0012' during program level 1 interrupt (CS004) see page 6-270.

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DF971 DG971

End of Instruction

Note: *See page 6-000 for data flow bit card locations.*

REGISTER AND STORAGE WITH ADDITION (RSA) INSTRUCTIONS

The CCU takes an I1 and an I2 cycle to execute either the 'insert character and count' or 'store character and count' instructions.

For the 'ICT' and 'STCT' instructions, the general register designated by the R field in the instruction must be an odd-numbered register; therefore, the general register = (2xR) +1.

Insert Character and Count (ICT)

0	1-3	4	5-6	7	8	9	10	11	12	13	14	15
0	B	0	R	N	0	0	0	1	0	0	0	0

The B field specifies a general register in the active group. The register contains an address (effective address) that is used to address storage. The content of the register specified by B is incremented by 1 after the effective address has been obtained. The byte at the effective address is placed in byte 0 (N=0) or byte 1 (N=1) of the general register designated by the R field. The register specified by R must be an odd-numbered register. Register 0 should not normally be specified in the B field because it contains the instruction address.

The 'C' and 'Z' latches are not changed.

Note: *If the registers specified by B and R are the same, the contents of byte 1 of the register is incremented before the 8-bit character is inserted. If N=1, the inserted character then overlays byte 1 of the same register, and the previous incrementing has no significance. If N=0, the character is inserted into byte 0 of the register, and byte 1 contains the original value plus 1.*

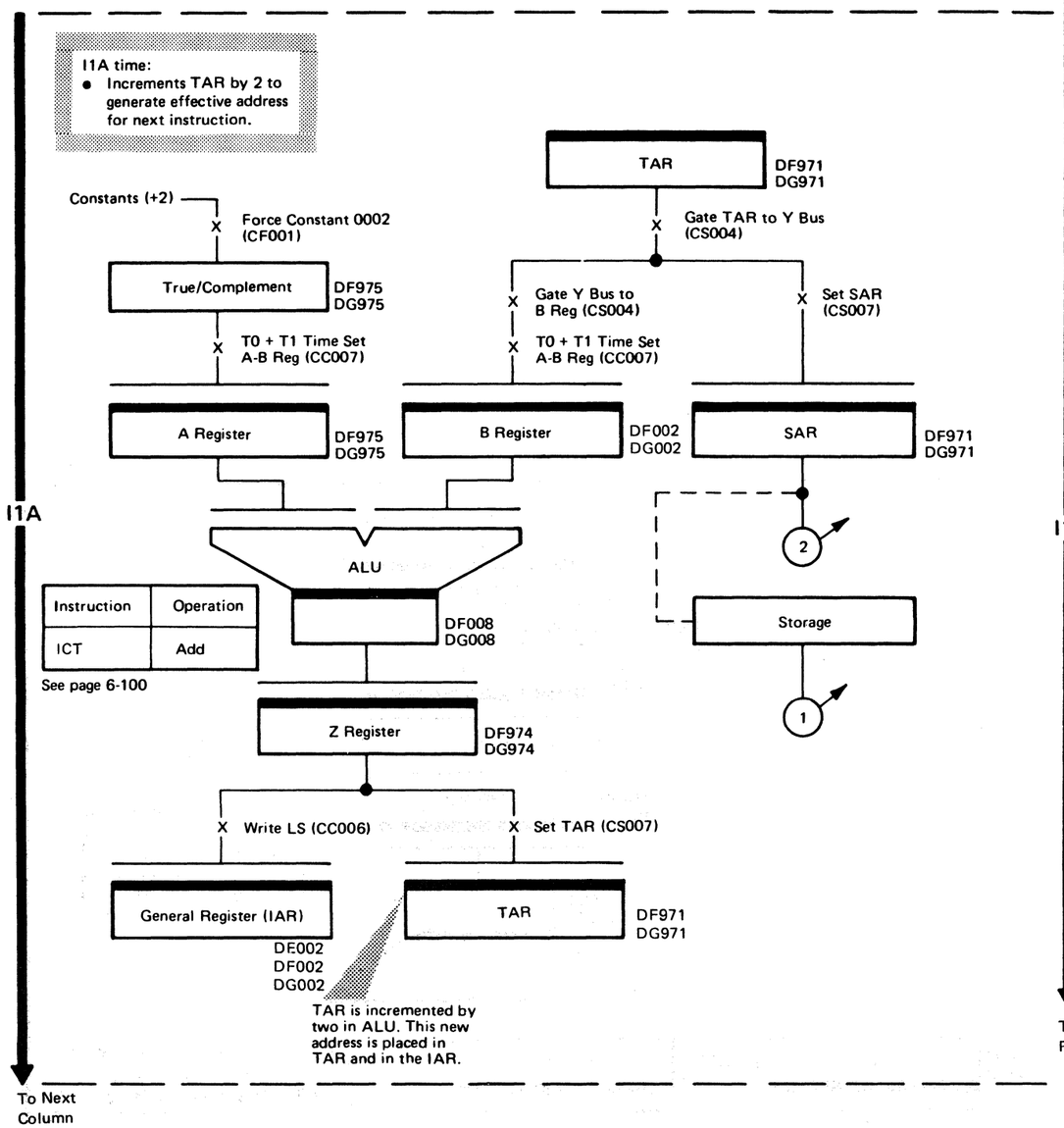
Store Character and Count (STCT)

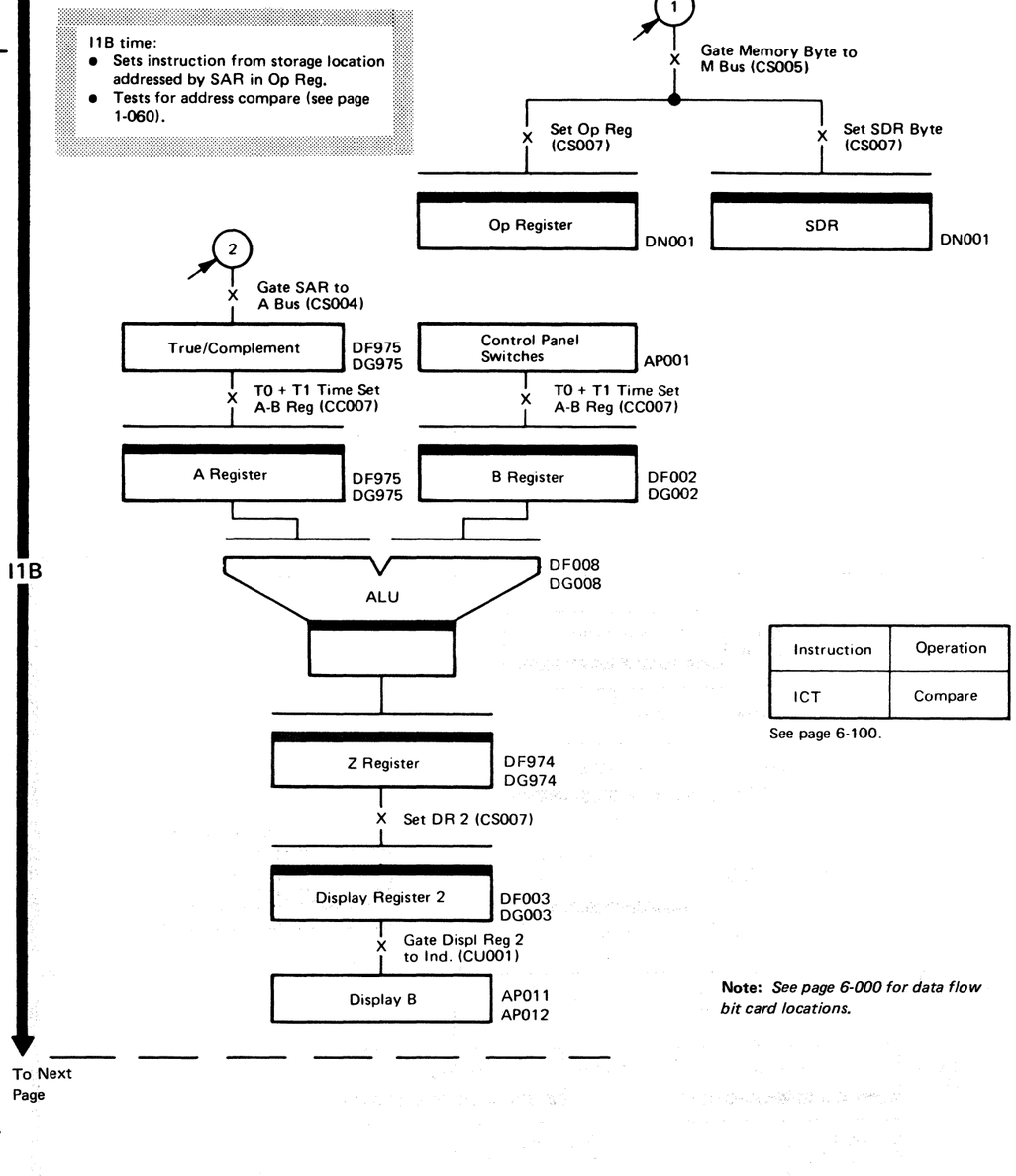
0	1-3	4	5-6	7	8	9	10	11	12	13	14	15
0	B	0	R	N	0	0	1	1	0	0	0	0

The B field specifies a general register in the active group. This register contains an address (effective address) that is used to select a storage location. The content of the register specified by B is incremented by 1. Byte 0 (N=0) or byte 1 (N=1) of the general register specified by R is then stored at the effective address. The register specified by R must be an odd-numbered register. Register 0 should not be specified by the B field because it contains the instruction address.

The 'C' and 'Z' latches are not changed.

ICT Instruction Operation





Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

ICT Only

I1C time:
- Preserves the instruction address in LAR.
- Places the address from General Register (B) into SAR.

Instruction	Operation
ICT	B Reg Direct

See page 6-100.

I1C

General Register (B) — DF002 DG002
X T0 + T1 Time Set A - B Reg (CC007)
B Register — DF002 DG002
ALU
DF974 DG974
Z Register — DF974 DG974
X Set TAR (CS007)
TAR — DF971 DG971
X Gate TAR to Y Bus (CS004)
X Set SAR (CS007)
SAR — DF971 DG971

SAR — DF971 DG971
X Set LAR (CS001)
LAR — DF002 DG002

To Next Column

ICT Only

I1D time:
- Increments the contents of General Register B by 1.

Instruction	Operation
ICT	Add

See page 6-100.

I1D

Constant (+1)
X Force Constant 0001 (CF001)
True/ Complement — DF975 DG975
X T0 + T1 Time Set A - B Reg (CC007)
A Register — DF975 DG975

General Register (B) — DF002 DG002
X T0 + T1 Time Set A -B Reg (CC007)
B Register — DF002 DG002

ALU
DF974 DG974
Z Register — DF974 DG974
X Write LS (CC006)
General Register (B) — DF002 DG002

To Next Page

Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

ICT Only

I2A time:
- Duplicates in both bytes of SDR the byte of general register R not specified by the N Field.

I2A

General Register (R) — DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU — Op. Reg. bit 0.7 ON Cross Hi to Lo OFF Cross Lo to Hi

DF974 DG974

Instruction	Operation
ICT	Cross

See page 6-100.

SAR Address from Gen Reg (B) — DF971 DG971

Z Register — DF974 DG974

X Gate Z Bus to M Bus (CS005)

X Set SDR Byte (CS007)

Storage

SDR — DN001

(1)

To Next Column

ICT Only

I2B time:
- Places the byte of storage specified by the B Field in SDR.
- Tests for address compare (see page 1-060).

I2B

SAR — DF971 DG971

X Gate SAR to A Bus (CS004)

True/ Complement — DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

Control Panel Switches — AP001

X T0 + T1 Time Set A-B Reg (CC007)

X Gate Y Bus to B Reg (CS004)

A Register — DF974 DG974

B Register — DF002 DG002

ALU

DF974 DG974

Instruction	Operation
ICT	Compare

See page 6-100.

(1)

X Gate Mem Byte to M Bus (CS005)

X Set SDR Byte (CS007)

SAR bit 1.7 ON Set SDR byte 1 OFF Set SDR byte 0

SDR — DN001

(A)

To Next Page

Z Register — DF974 DG974

X Set DR 2 (CS007)

Display Register 2 — DF003 DG003

X Gate Displ Reg 2 to Ind (CU001)

Display B — AP011 AP012

To Next Page

Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

ICT Only

I2C time:
- Transfer the bytes A Reg Direct when the N field specifies the same byte as the B field.
- Crosses the bytes when the N field and the B field specify different bytes.

I2C

Instruction	Operation
ICT	*Cross or A Reg Direct

See page 6-100.

***Note:** Cross Hi to Lo and Lo to Hi.*

From Preceding Page

A

X Gate SDR Bits to A Bus (CF003)

True/ Complement — DE975 DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DE975 DF975 DG975

ALU

DE974 DF974 DG974

Z Register — DE974 DF974 DG974

X Write LS (CC006)

General Register (R) — DE002 DF002 DG002

To Next Column

ICT Only

I2D time:
- Loads the address of the next instruction in TAR and SAR.

I2D

Instruction	Operation
ICT	B Reg Direct

See page 6-100.

General Register (IAR) — DE002 DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DE002 DF002 DG002

ALU

DE974 DF974 DG974

Z Register — DE974 DF974 DG974

X Set TAR (CS007)

TAR — DE971 DF971 DG971

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DE971 DF971 DG971

End of Instruction

Note: *See page 6-000 for data flow bit card locations.*

STCT Instruction Operation

TAR is incremented by 2. This new address is used in the next instruction cycle.

TAR DF971 DG971

Constants (+2) → X Force Constant 0002 (CF001)

True/Complement DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register DF975 DG975

X Gate TAR to Y Bus (CS004)

X Gate Y Bus to B Reg (CS004)

X T0 + T1 Time Set A-B Reg (CC007)

B Register DF002 DG002

X Set SAR (CS007)

SAR DF971 DG971

2

Storage

1

ALU

DF008 DG008

Instruction	Operation
STCT	Add

See page 6-100

Z Register DF974 DG974

X Write LS (CC006)

X Set TAR (CS007)

General Register (IAR)

TAR DF971 DG971

DF002 DG002

TAR is incremented by two in ALU. This new address is placed in TAR and in the IAR.

To Next Column

I1A

I1B

The data in the storage location addressed by SAR is loaded in the Op register and in SDR. The addresses in SAR and in the ADDRESS/DATA switches are compared. The ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE COMPARE switch on 1-060.)

1

X Gate Memory Byte to M Bus (CS005)

X Set Op Reg (CS007)

X Set SDR Byte (CS007)

Op Register DN001

SDR DN001

2

X Gate SAR to A Bus (CS004)

True/Complement DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register DF975 DG975

Control Panel Switches AP001

X T0 + T1 Time Set A-B Reg (CC007)

B Register DF002 DG002

ALU

DE008 DF008 DG008

Z Register DF974 DG974

X Set DR 2 (CS007)

Display Register 2 DF003 DG003

X Gate Displ Reg 2 to Ind. (CU001)

Display B AP011 AP012

Instruction	Operation
STCT	Compare

See page 6-100.

To Next Page

Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

STCT Only

The address in general register B is placed in SAR so it can be used to address storage.

General Register (B) — DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU

DF974 DG974

Instruction	Operation
STCT	B Reg Direct

See page 6-100.

Z Register — DF974 DG974

X Set TAR (CS007)

TAR — DF971 DG971

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DF971 DG971

X Set LAR (CS001)

LAR — DF002 DG002

I1C

To Next Column

I1D

STCT Only

The content of general register B is incremented by 1.

Constant (+1)

X Force Constant 0001 (CF001)

True/ Complement — DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DF975 DG975

General Register (B) — DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU

DF974 DG974

Instruction	Operation
STCT	Add

See page 6-100.

Z Register — DF974 DG974

X Write LS (CC006)

General Register (B) — DF002 DG002

To Next Page

Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

STCT Only

The selected byte is duplicated in both bytes of the SDR.

General Register (R) DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register DF002 DG002

ALU

Op Reg bit 1.7
ON Cross Hi to Lo
OFF Cross Lo to Hi

DF974 DG974

Instruction	Operation
STCT	B Reg Direct

See page 6-100.

12A

SAR DE971 DF971 DG971

Z Register DF974 DG974

X Gate Z Bus to M Bus (CS005)

X Set SDR Byte (CS007)

2

Storage

SDR DN001

1

To Next Column

STCT Only

The byte of the storage location not specified by the B field is placed in the same byte of the SDR. Bytes 0 and 1 of the SDR are then stored at the addressed storage location. The addresses in SAR and in the ADDRESS/DATA switches are compared. The ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE ADDRESS COMPARE switch on page 0-060.)

2

X Gate SAR to A Bus (CS004)

True/Complement DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

Control Panel Switches AP001

X T0 + T1 Time Set A-B Reg (CC007)

X Gate Y Bus to B Reg (CS004)

A Register DF975 DG975

B Register DF002 DG002

12B

ALU

DF974 DG974

Instruction	Operation
STCT	Compare

1

SAR bit 1.7
ON Set SDR byte 1
OFF Set SDR byte 0

X Gate Mem Byte to M Bus (CS005)

X Set SDR Byte (CS007)

Z Register DF974 DG974

X Set DR 2 (CS007)

SDR DN001

Storage

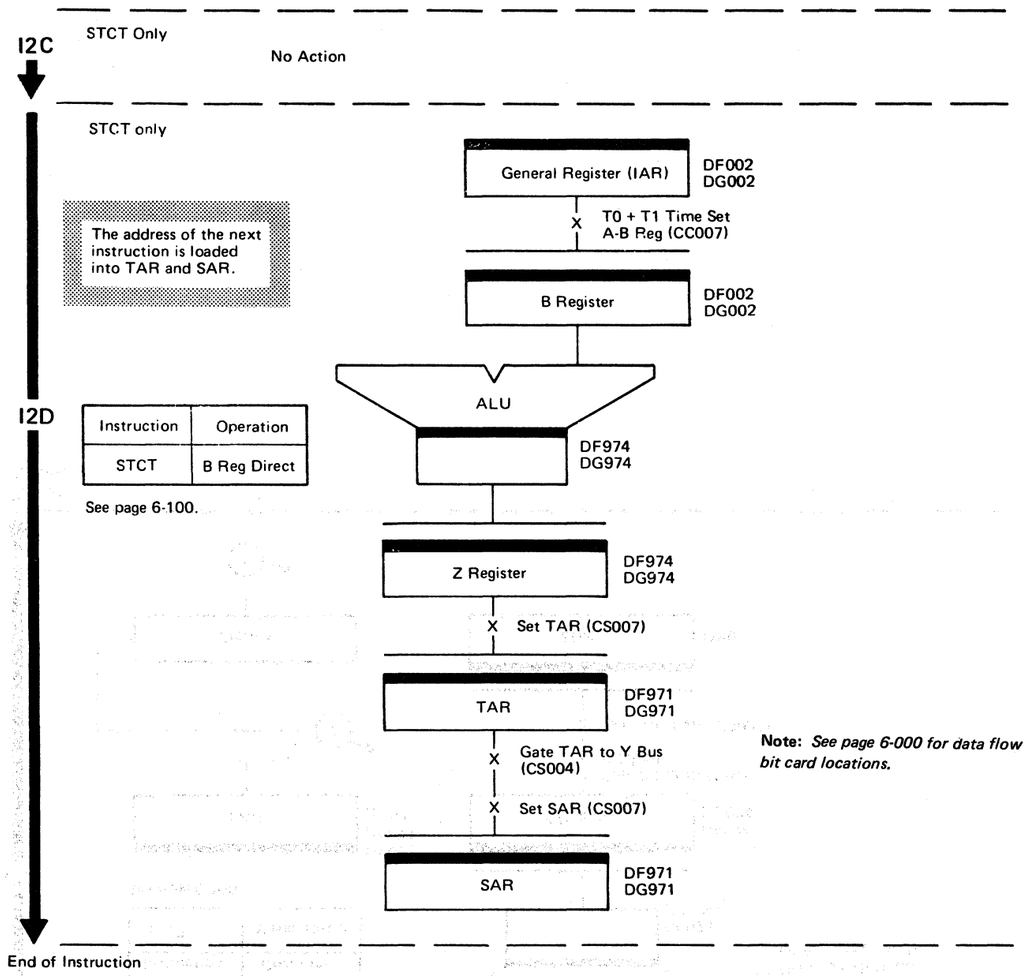
Display Register DF003 DG003

X Gate Displ Reg 2 to Ind (CU001)

Display B AP011 AP012

To Next Page

Note: *See page 6-000 for data flow bit card locations.*



Note: *See page 6-000 for data flow bit card locations.*

REGISTER AND IMMEDIATE ADDRESS (RA) INSTRUCTIONS

The CCU takes an I1 and an I2 cycle to execute either the 'branch and link' or the 'load address' instruction.

The 'branch and link' and 'load address' instructions are the only 32-bit instructions for the 3705-80.

Branch and Link (BAL)

0	1	2	3	4	5-7	8	9	10	11	12	13	14-31
1	0	1	1	1	R	0	0	0	0	0	0	A

This instruction causes an unconditional branch to the storage address specified by the A field. The contents of general register 0 (IAR) are moved to the general register specified by the R field to provide for subroutine linkage. The address in the A field is then placed in register 0. Since register 0 is the IAR, no linkage is provided if it is specified by R.

The 'C' and 'Z' latches are not changed.

Load Address (LA)

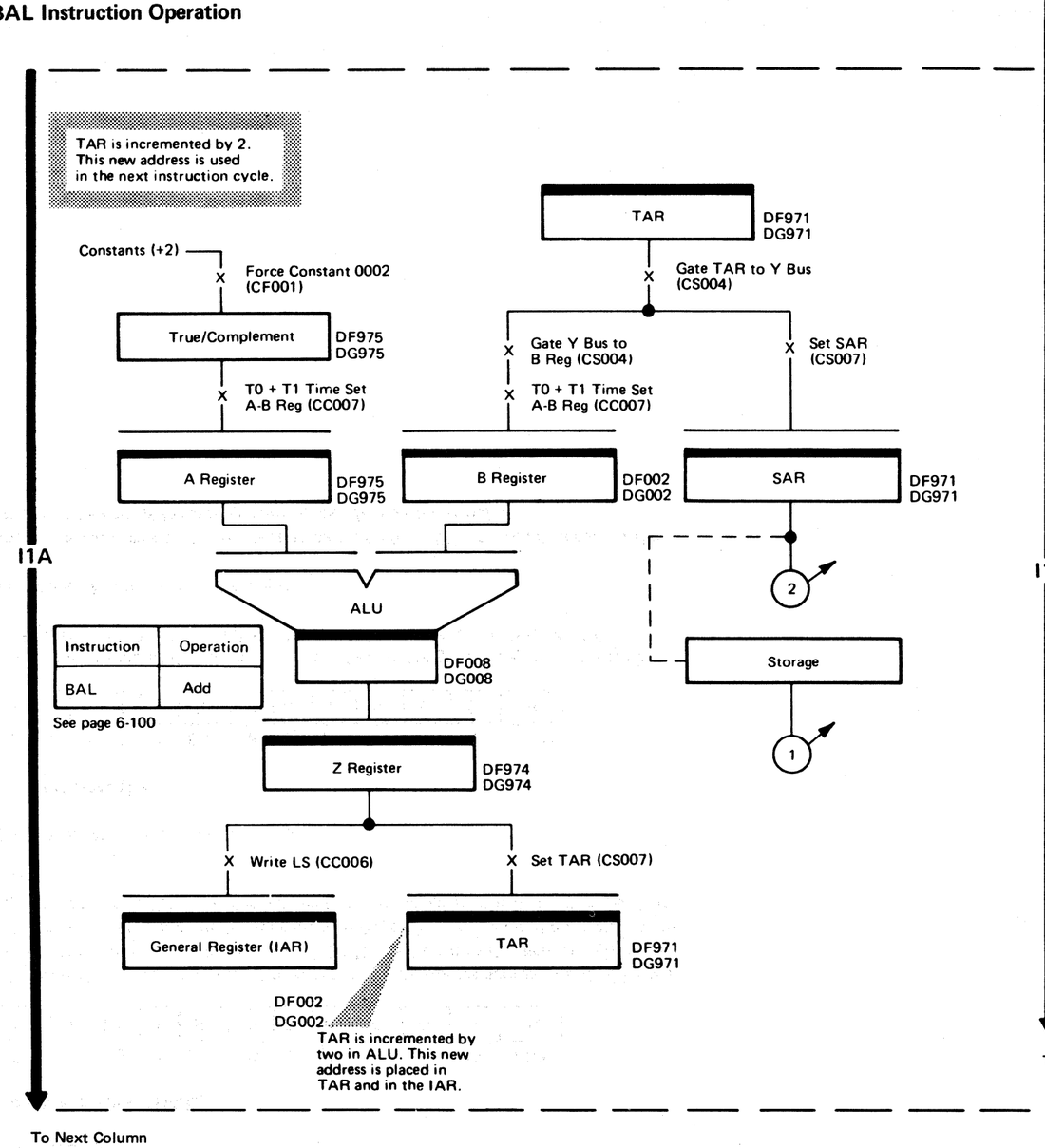
0	1	2	3	4	5-7	8	9	10	11	12	13	14-31
1	0	1	1	1	R	0	0	1	0	0	0	A

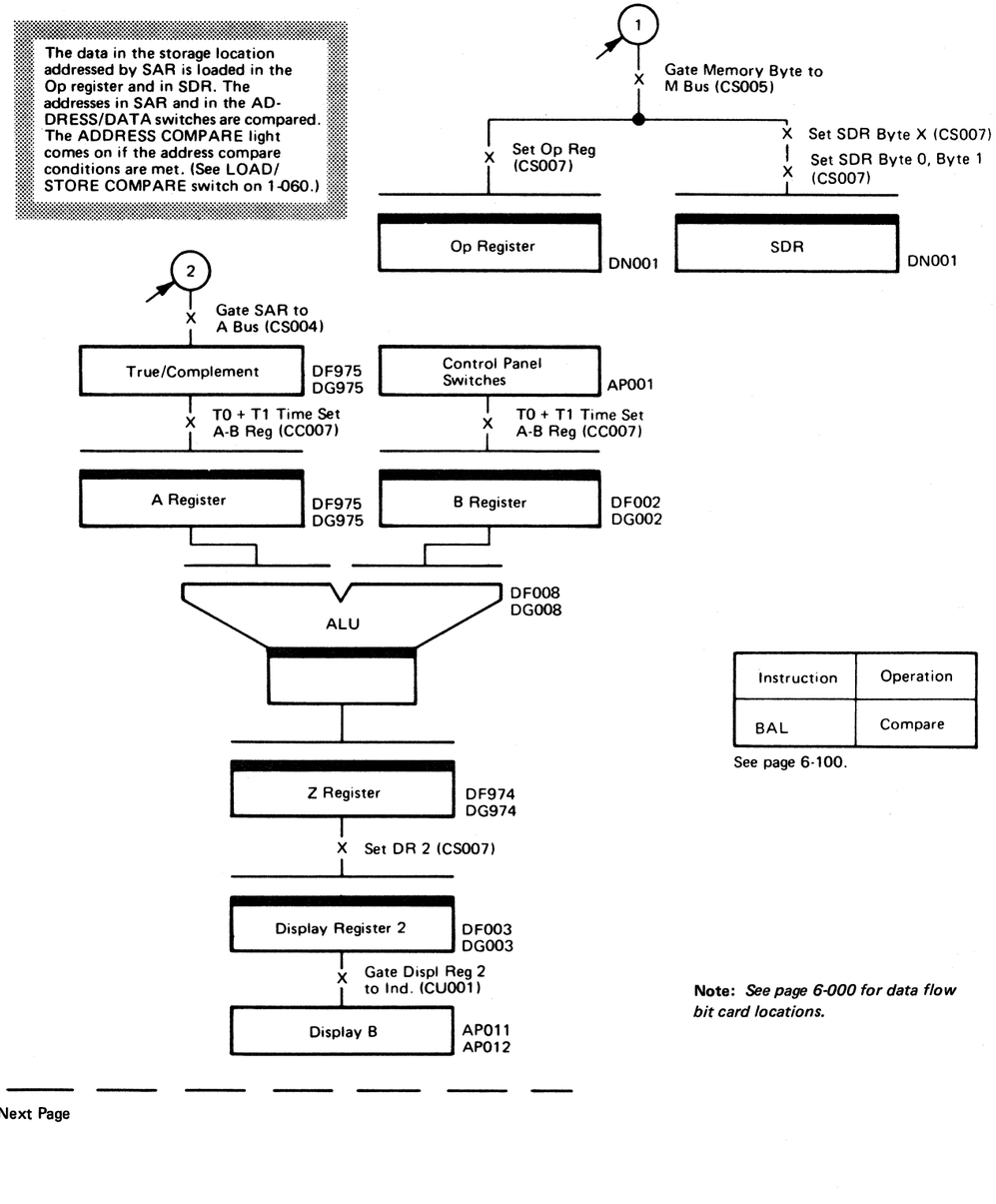
This instruction places the contents of the A field in the general register specified by the R field. Bits 12, 13, 14, and 15 of the A field are loaded into byte X of R.

The 'C' and 'Z' latches are not changed.

Note: *If general register 0 (IAR) is addressed, an unconditional branch occurs to the instruction located at the storage address specified by the A field.*

BAL Instruction Operation





Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

I1C

BAL Only

The address in SAR is placed in LAR.

SAR — DF971 DG971

X Set LAR (CS001)

LAR — DF002 DG002

I1D

BAL Only

The address in TAR is placed in SAR.

TAR — DF971 DG971

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DF971 DG971

(1)

I2A

BAL Only

The address in TAR is incremented by 2 and placed in general register R, and serves as the backward link. A storage fetch operation fetches the second halfword of the BAL instruction.

Constant (+2) → X Force Constant 0002 (CF001)

True/Complement — DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

TAR — DF971 DG971

X Gate TAR to Y Bus (CS004)

X Gate Y Bus to B Reg (CS004)

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DF975 DG975

B Register — DF002 DG002

Instruction	Operation
BAL	Add

See page 6-100.

ALU

DF974 DG974

(1) Storage (2)

Z Register — DF974 DG974

X Write LS (CC006)

General Register (R) — DF002 DG002

To Next Column

I2B

BAL Only

The address in the addressed storage location is loaded into bytes 0 and 1 of the SDR. The addresses in the SAR and in the ADDRESS/DATA switches are compared. The ADDRESS COMPARE light comes on if the address compare conditions are met. (See LOAD/STORE ADDRESS COMPARE switch on page 1-060.)

(1)

X Gate SAR to A Bus (CS004)

True/Complement — DF975 DG975

Control Panel Switches — AP001

X T0 + T1 Time Set A - B Reg (CC007)

X T0 + T1 Time Set A-B Reg (CC007)

X Gate Y Bus to B Reg (CS004)

(2)

X Gate Mem Byte to M Bus (CS005)

A Register — DF975 DG975

B Register — DF002 DG002

X Set SDR Byte (CS007)

ALU

SDR — DN001

DF974 DG974

A

To Next Page

Z Register — DF974 DG974

X Set DR 2 (CS007)

Instruction	Operation
BAL	Compare

See page 6-100.

Display Register 2 — DF003 DG003

X Gate Displ Reg 2 to Ind (CU001)

Display B — AP011 AP012

To Next Page

Note: *See page 6-000 for data flow bit card locations.*

From Previous Page

I2C BAL Only

No Action

BAL Only

From Preceding Page

A

X Gate SDR Bits to A Bus (CF003)

True/Complement — DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DF975 DG975

The contents of SDR are placed in TAR and in the general register 0 (IAR).

ALU

DF974 DG974

Instruction	Operation
BAL	A Reg Direct

See page 6-100.

Z Register — DF974 DG974

X Set TAR (CS007)

X Write LS (CC006)

TAR — DF971 DG971

General Register 0 (IAR) — DF002 DG002

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

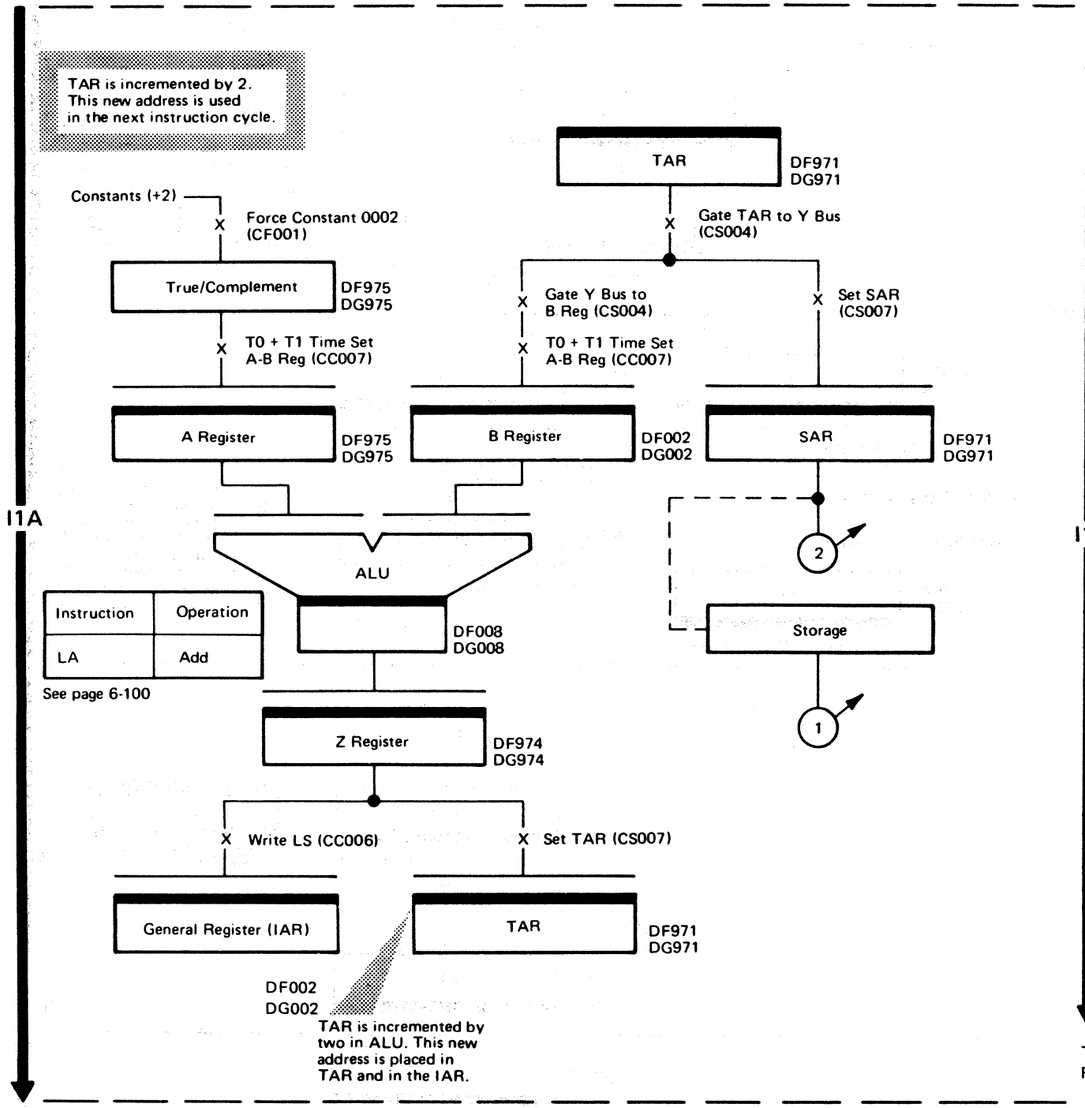
SAR — DF971 DG971

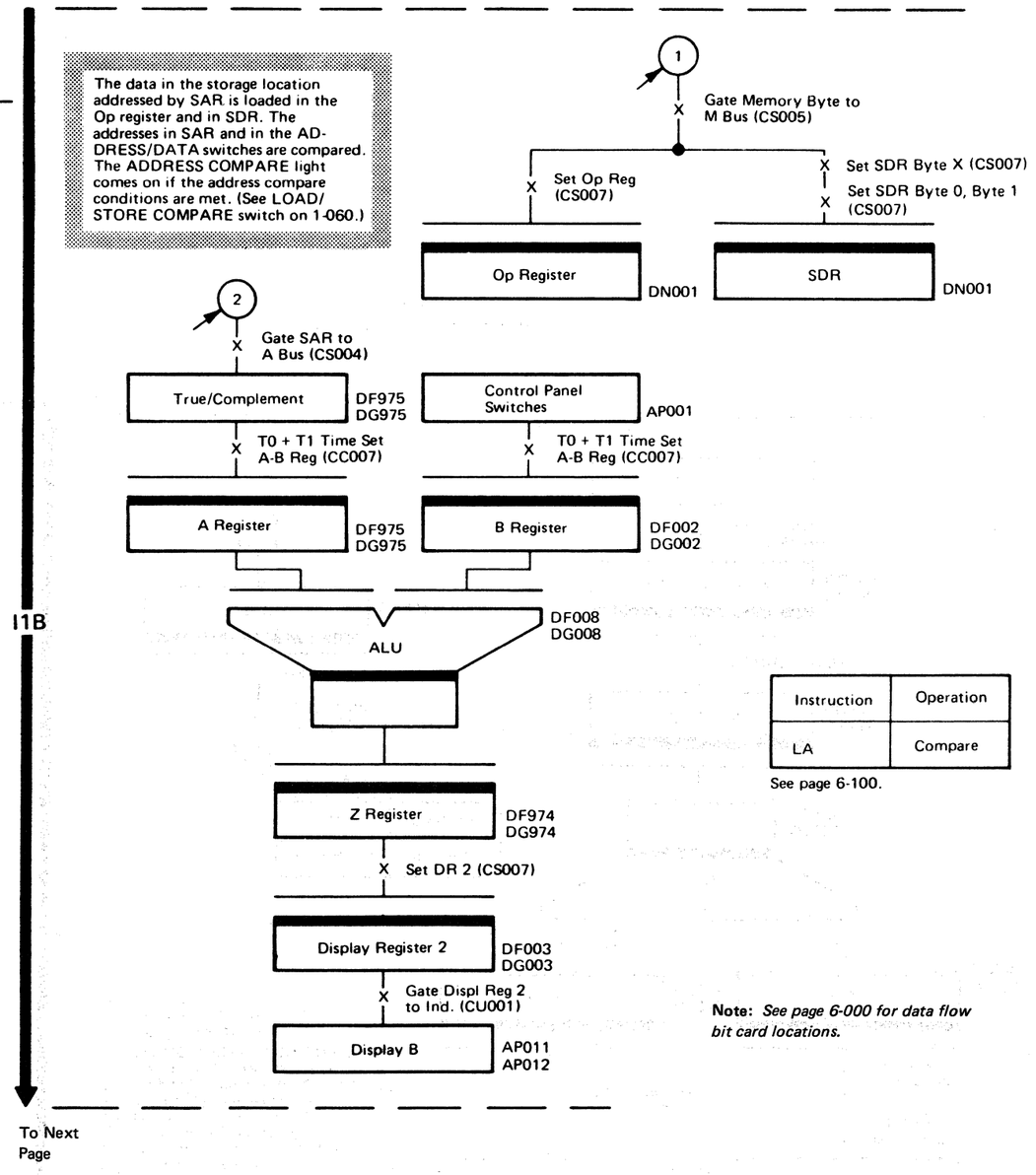
I2D

End of Instruction

Note: *See page 6-000 for data flow bit card locations.*

LA Instruction Operation

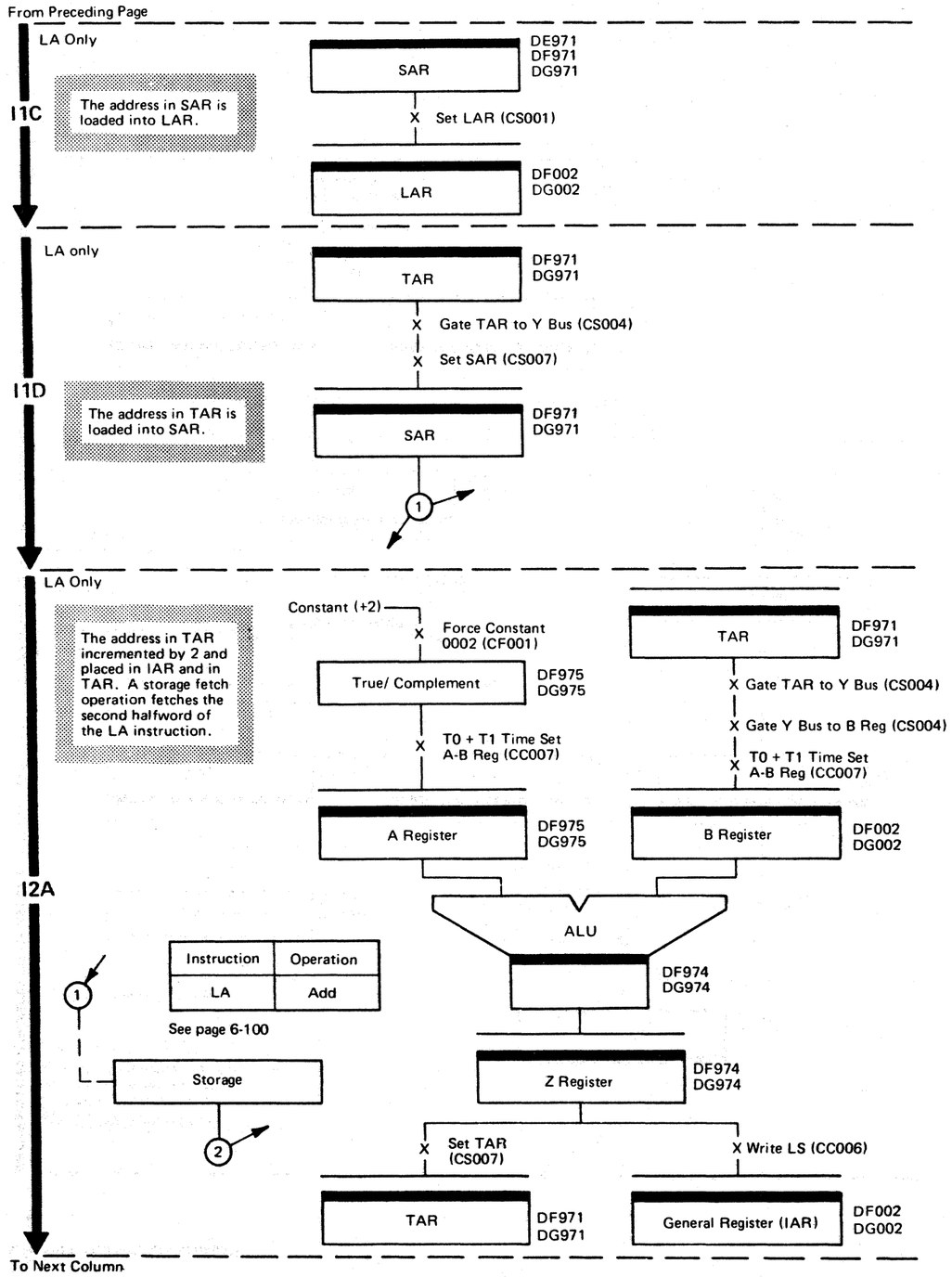




Instruction	Operation
LA	Compare

See page 6-100.

Note: *See page 6-000 for data flow bit card locations.*



Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

I2C LA Only

No Action

LA Only

The contents of SDR are placed in general register R. TAR is also loaded if general register R is the IAR.

Instruction	Operation
LA	A Reg Direct

See page 6-100.

I2D

From Preceding Page

A

X Gate SDR Bits to A Bus (CF003)

True/Complement — DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DF975 DG975

ALU

DF974 DG974

Z Register — DF974 DG974

X Set TAR (CS007)

X Write LS (CC006)

TAR — DF971 DG971

General Register (R) — DF002 DG002

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DF971 DG971

Note: See page 6-000 for data flow bit card locations.

End of Instruction

REGISTER BRANCH OR REGISTER AND BRANCH (RT) INSTRUCTIONS

The CCU takes an I1 cycle to execute any one of the five register branch, or register and branch instructions.

Branch Displacement Calculations

The displacement in halfwords can be calculated as shown below (multiply by 2 for displacement in bytes):

If * = 0, Displacement halfwords = 1 + T
If * = 1, Displacement halfwords = 1 - T

Example: A800 is a NO OP.
A803 is a branch to itself indefinitely.

Branch (B)

0	1	2	3	4	5-14	15
1	0	1	0	1	T	*

*0 = + displacement
1 = - displacement

The displacement in the T field is added to the address in general register 0 (IAR) to form a "branch to" address. The displacement specified by the T field can be -1023 to +1023 halfwords. Bit 15 determines whether the displacement is positive or negative. An unconditional branch to the "branch to" address occurs.

The 'C' and 'Z' latches are not changed.

Note: *Since register 0 is incremented before the instruction is executed, the displacement is with respect to the address of the next sequential instruction. Therefore, the displacement from the B instruction is -1022 to +1024 halfwords.*

Branch On Bit (BB)

0	1	2	3	4	5-6	7	8	9-14	15
1	1	M	M	1	R	N	M	T	*

*0 = + displacement
1 = - displacement

General Register = (2xR) + 1

The displacement in the T field is added to the address in general register 0 (IAR) to form a "branch to" address. The displacement specified by the T field can be -63 to +63 halfwords. Bit 15 determines whether the displacement is positive or negative. An unconditional branch to the "branch to" address occurs.

The M field specifies a bit in byte 0 (N=0) or byte 1 (N=1) of the general register designated by the R field. This bit is tested. If the bit is 0, the next sequential instruction is executed; if the bit is 1, the next instruction to be executed is at the "branch to" address.

The 'C' and 'Z' latches are not changed.

Note: *Since register 0 is incremented before the instruction is executed, the displacement is with respect to the address of the next sequential instruction after the BB instruction. Therefore, the displacement from the BB instruction is -62 to +64 halfwords.*

M field and N field decode

	Instruction	
Bit to Be Tested	*N 7*	*MMM—field 2 3 8—bit*
0.0	0	0 0 0
1	0	0 0 1
2	0	0 1 0
3	0	0 1 1
4	0	1 0 0
5	0	1 0 1
6	0	1 1 0
7	0	1 1 1
1.0	1	0 0 0
1	1	0 0 1
2	1	0 1 0
3	1	0 1 1
4	1	1 0 0
5	1	1 0 1
6	1	1 1 0
7	1	1 1 1

Branch On C Latch (BCL)

0	1	2	3	4	5-14	15
1	0	0	1	1	T	*

*0 = + displacement
1 = - displacement

The displacement in the T field is added to the address in general register 0 (IAR) to form a "branch to" address. The displacement specified by the T field can be -1023 to +1023 halfwords. Bit 15 determines whether the displacement is positive or negative.

The 'C' latch is tested. If it is not set, the next sequential instruction is executed. If it is set, the next instruction to be executed is at the "branch to" address.

The 'C' and 'Z' latches are not changed.

Note: *Since register 0 (IAR) is incremented before the instruction is executed, the displacement is with respect to the next sequential instruction after the BCL instruction. Therefore, the displacement from the BCL instruction is -1022 to +1024 halfwords.*

Branch On Count (BCT)

0	1	2	3	4	5-6	7	8	9-14	15
1	0	1	1	1	R	N	1	T	*

*0 = + displacement
1 = - displacement

General Register = (2xR) + 1

The displacement in the T field is added to the address in general register 0 (IAR) to form a "branch to" address. The displacement specified by the T field can be -63 to +63 halfwords. Bit 15 determines whether the displacement is positive or negative.

The count contained in byte 0 (N=0) or bytes 0 and 1 (N=1) of the general register designated by the R field is decremented by 1 and then is tested. If the result is 0, the next sequential instruction is executed. If the result is not 0, the next instruction to be executed is at the "branch to" address.

If the byte count is X'00' or the halfword count is X'0000' before execution of this instruction, then the effective count value is 256 or 65,536, respectively.

The 'C' and 'Z' latches are not changed when this instruction is executed.

Note: *Since register 0 (IAR) is incremented before the instruction is executed, the displacement is with respect to the next sequential instruction after the BCT instruction. Therefore, the displacement from the BCT instruction is -62 to +64 halfwords.*

Branch On Z Latch (BZL)

0	1	2	3	4	5-14	15
1	0	0	0	1	T	*

*0 = + displacement
1 = - displacement

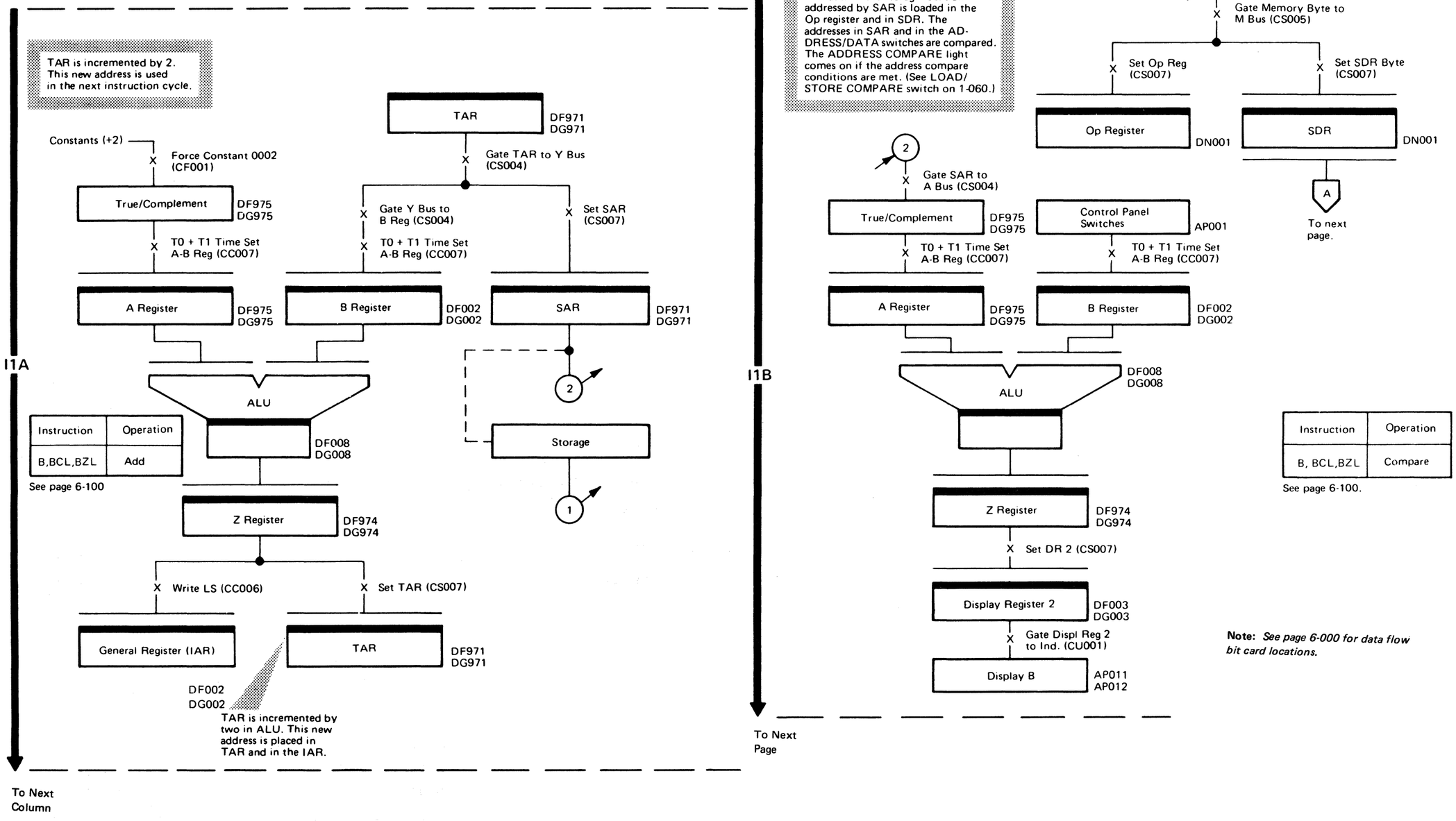
The displacement in the T field is added to the address in general register 0 (IAR) to form a "branch to" address. The displacement specified by the T field can be -1023 to +1023 halfwords. Bit 15 determines whether the displacement is positive or negative.

The 'Z' condition latch is tested. If not set, the next sequential instruction is executed. If set, the next instruction to be executed is at the "branch to" address.

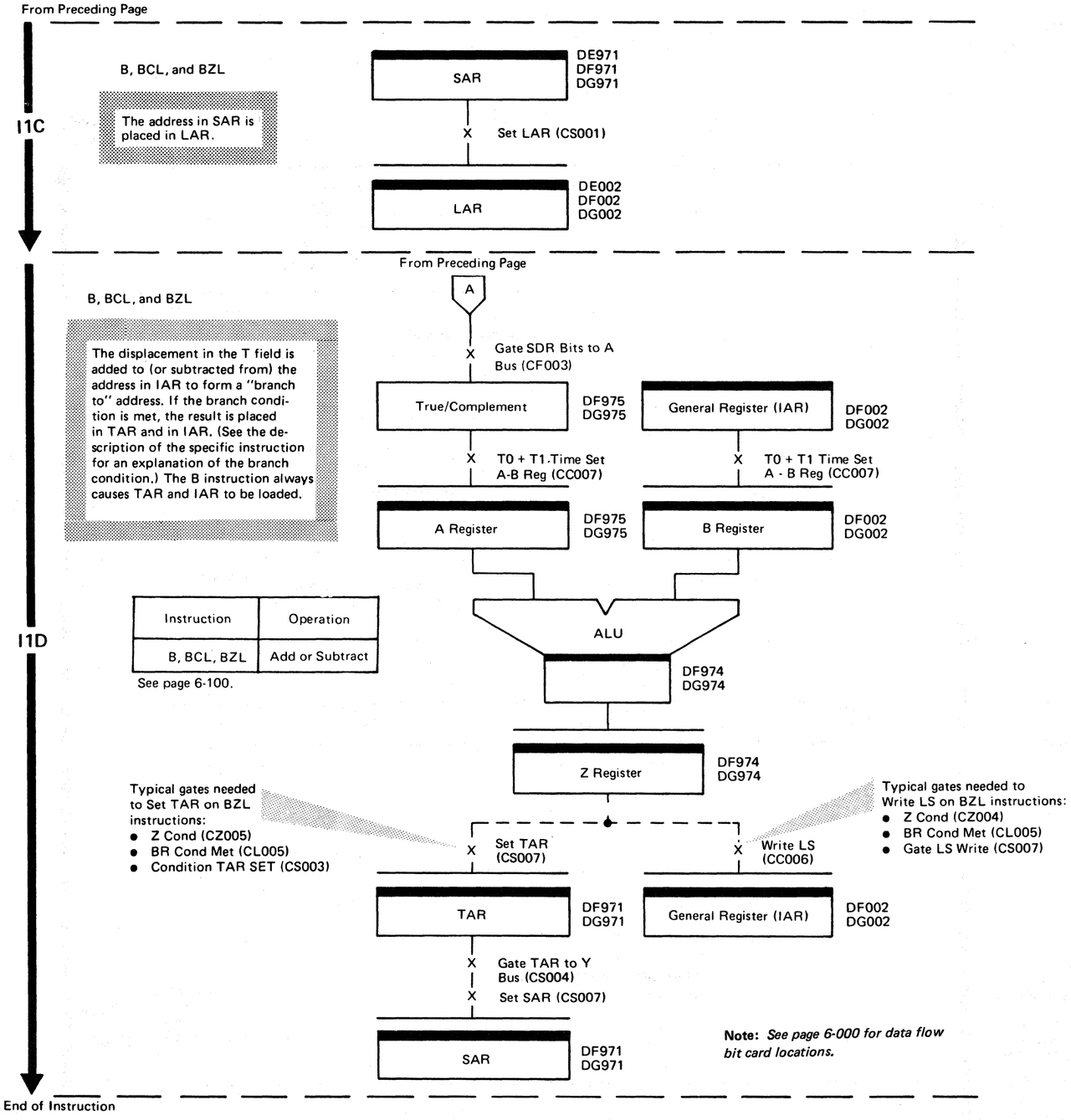
The 'C' and 'Z' latches are not changed.

Note: *Since register 0 is incremented before the instruction is executed, the displacement is with respect to the next sequential instruction after the BZL instruction. Therefore, the displacement from the BZL instruction can be -1022 to +1024 halfwords.*

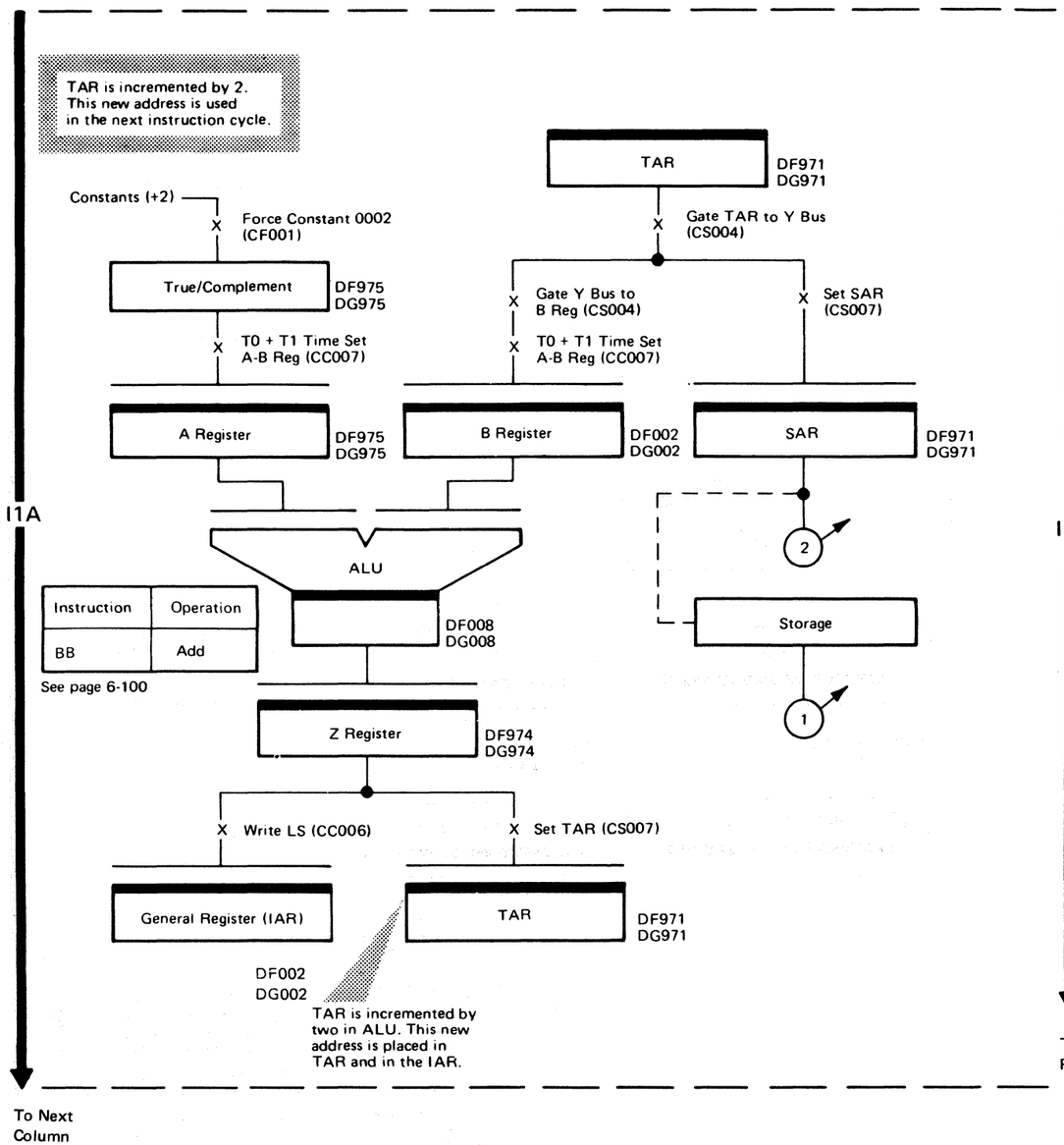
B, BCL, and BZL Instruction Operation

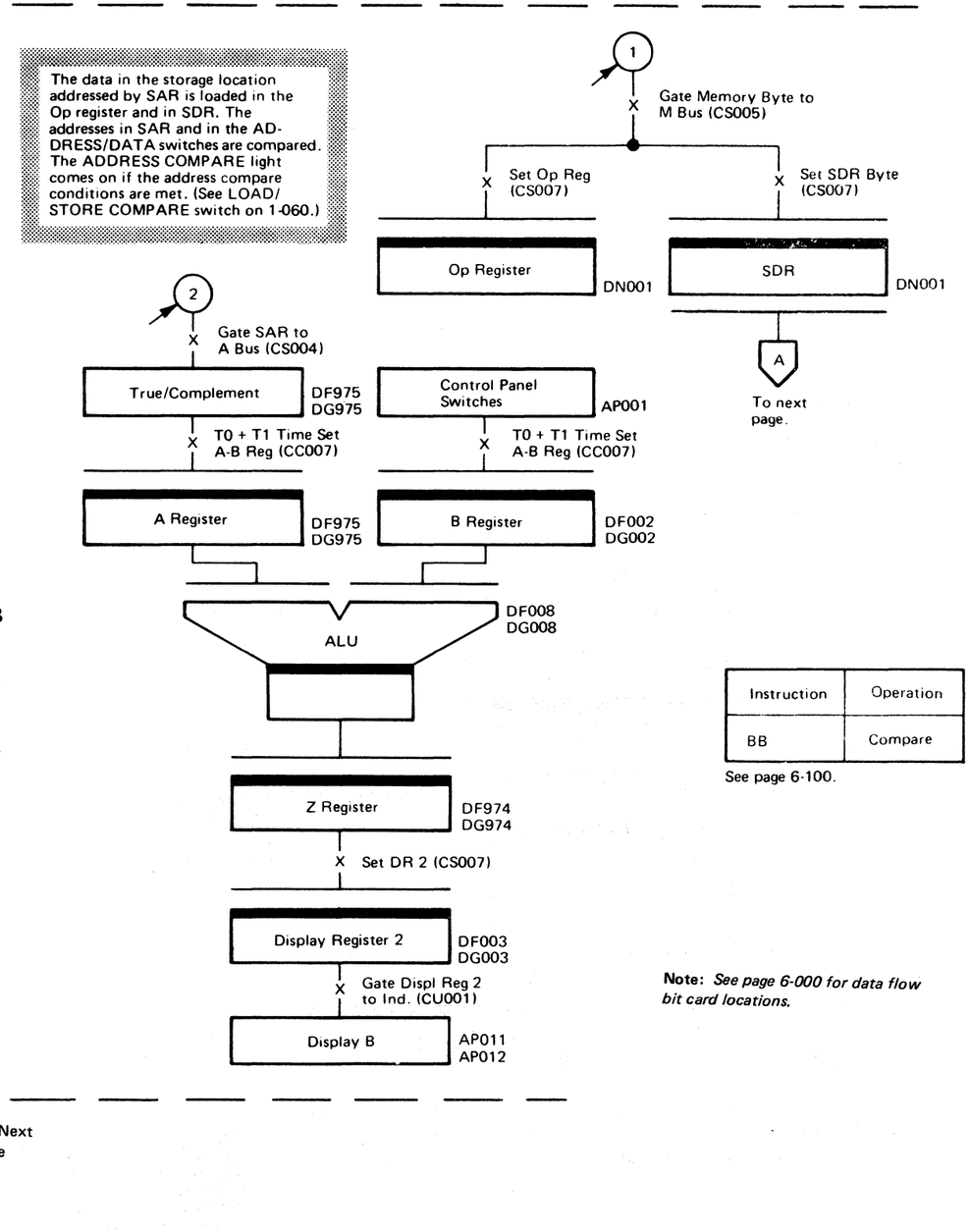


Note: *See page 6-000 for data flow bit card locations.*


From Preceding Page
B, BCL, and BZL
The address in SAR is placed in LAR.
I1C
SAR
DE971
DF971
DG971
X Set LAR (CS001)
LAR
DE002
DF002
DG002
From Preceding Page
A
B, BCL, and BZL
The displacement in the T field is added to (or subtracted from) the address in IAR to form a "branch to" address. If the branch condition is met, the result is placed in TAR and in IAR. (See the description of the specific instruction for an explanation of the branch condition.) The B instruction always causes TAR and IAR to be loaded.
X Gate SDR Bits to A Bus (CF003)
True/Complement
DF975
DG975
General Register (IAR)
DF002
DG002
X T0 + T1 Time Set A-B Reg (CC007)
X T0 + T1 Time Set A - B Reg (CC007)
A Register
DF975
DG975
B Register
DF002
DG002
ALU
DF974
DG974
Z Register
DF974
DG974
I1D
Instruction
Operation
B, BCL, BZL
Add or Subtract
See page 6-100.
Typical gates needed to Set TAR on BZL instructions:
• Z Cond (CZ005)
• BR Cond Met (CL005)
• Condition TAR SET (CS003)
X Set TAR (CS007)
X Write LS (CC006)
Typical gates needed to Write LS on BZL instructions:
• Z Cond (CZ004)
• BR Cond Met (CL005)
• Gate LS Write (CS007)
TAR
DF971
DG971
General Register (IAR)
DF002
DG002
X Gate TAR to Y Bus (CS004)
X Set SAR (CS007)
SAR
DF971
DG971
Note: See page 6-000 for data flow bit card locations.
End of Instruction

BB Instruction Operation





Instruction	Operation
BB	Compare

See page 6-100.

Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

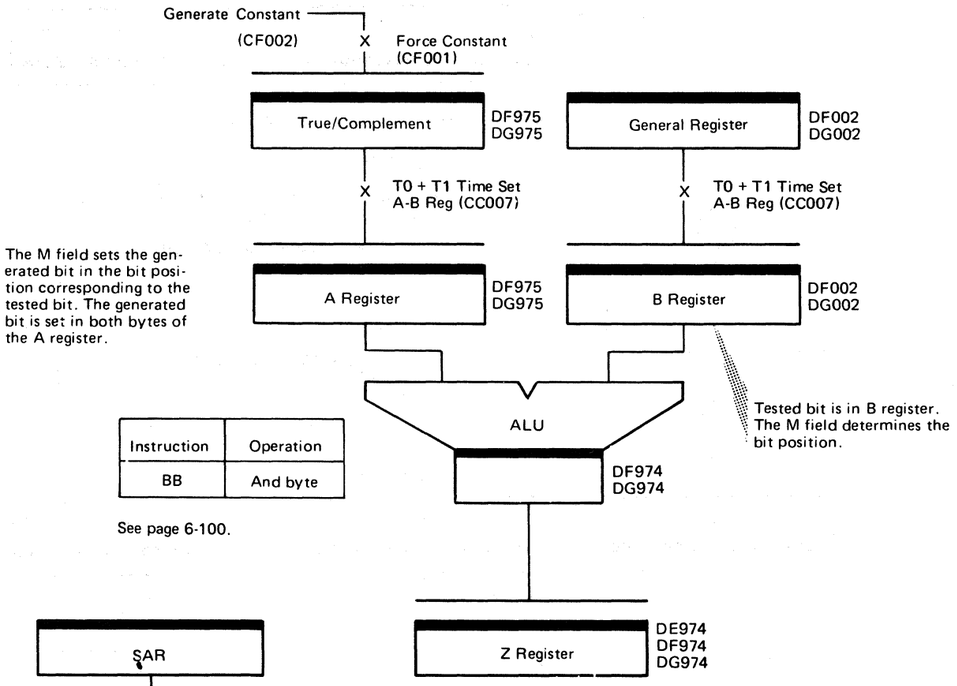
BB only

A one is forced in the bit position (determined by the M field of the Op reg) of both byte 0 and byte 1 of the A reg. The general register content (includes the bit to be tested) is placed in the B reg. ALU performs an 'AND byte 0' or 'AND byte 1' operation (determined by the N field). Test results:

- If the Z bus byte 0 or 1 contains a one, gate the branch to address to TAR and IAR at I1D time.
- If the Z bus byte 0 and 1 both contain zeros, inhibit gating the branch to address to TAR and IAR leaving the next sequential address in TAR and IAR.

I1C

The M field sets the generated bit in the bit position corresponding to the tested bit. The generated bit is set in both bytes of the A register.



Instruction	Operation
BB	And byte

See page 6-100.

Examples: 1. AND byte 0 operation, test bit = 1 at M = 3

	Byte 0		Byte 1		
B Reg	XXX1	XXXX	XXXX	XXXX	(No byte 1
A Reg	0001	0000	0001	0000	operation)
Z Bus	0001	0000	0000	0000	≠BRANCH

2. AND byte 1 operation, test bit = 0 at M = 7

B Reg	XXXX	XXXX	XXXX	XXX0
A Reg	0000	0001	0000	0001
	0000	0000	0000	0000 ≠No BRANCH

No byte 0 operation

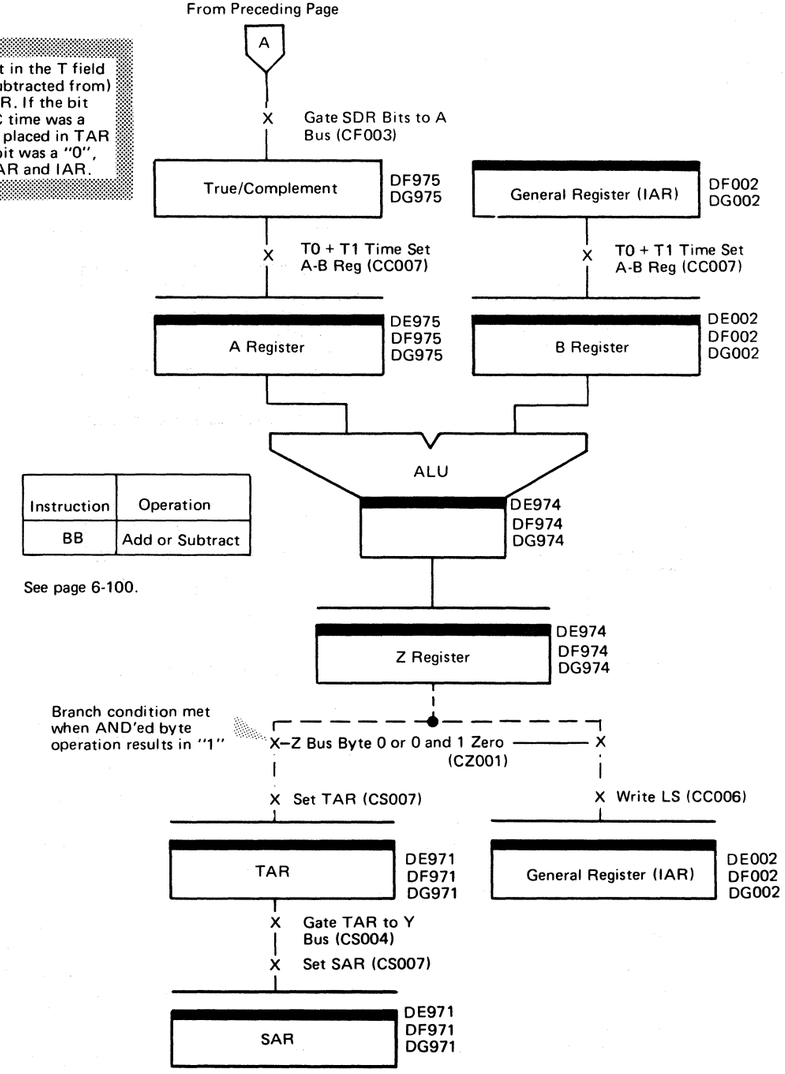
To Next Column

BB only

The displacement in the T field is added to (or subtracted from) the address in IAR. If the bit tested during I1C time was a "1", the result is placed in TAR and IAR. If the bit was a "0", inhibit setting TAR and IAR.

I1D

From Preceding Page



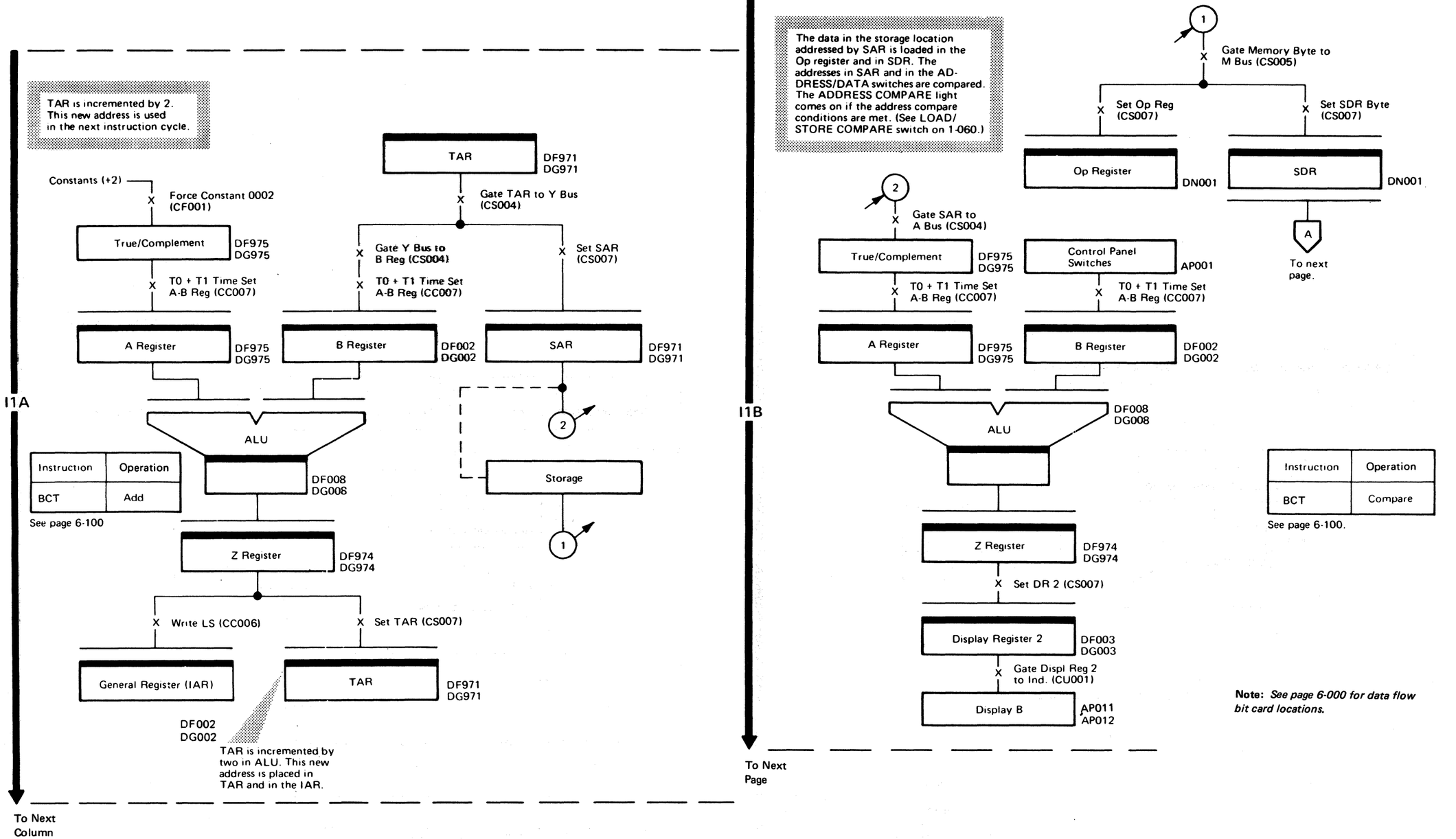
Instruction	Operation
BB	Add or Subtract

See page 6-100.

End of Instruction

Note: *See page 6-000 for data flow bit card locations.*

BCT Instruction Operation



From Preceding Page

BCT only

The contents of the selected byte of general register R are decremented by 1, and the result is tested. If the result is 0, the next sequential instruction is executed. If the result is not 0, the next instruction to be executed is at the "branch to" address.

I1C

Constant (+1)

X Force Constant 0001 (CF001)

True/Complement — DF975 DG975

General Register (R) — DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DF975 DG975

B Register — DF002 DG002

ALU

DF974 DG974

Instruction	Operation
BCT	And

See page 6-100.

Z Register — DF974 DG974

X Set TAR (CS007)

X Write LS (CC006)

SAR — DF971 DG971

TAR — DF971 DG971

General Register (IAR) — DF002 DG002

X Set LAR (CS001)

LAR — DF002 DG002

To Next Column

BCT only

The displacement in the T field is added to (or subtracted from) the address in IAR. If the branch condition was met, the result is loaded in TAR and IAR.

I1D

From Preceding Page

A

X Gate SDR Bits to A Bus (CF003)

True/Complement — DF975 DG975

General Register (IAR) — DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DF975 DG975

B Register — DF002 DG002

ALU

DF974 DG974

Instruction	Operation
BCT	Add or Subtract

See page 6-100.

Z Register — DF974 DG974

X Set TAR (CS007)

X Write LS (CC006)

TAR — DF971 DG971

General Register (IAR) — DF002 DG002

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DF971 DG971

End of Instruction

Note: *See page 6-000 for data flow bit card locations.*

REGISTER AND EXTERNAL REGISTER (RE) INSTRUCTIONS

An 'input' or 'output' or 'exit' instruction takes one I1 cycle for execution.

Input

0	1-3	4	5-7	8-11	12	13	14	15
0	E	0	R	E	1	1	0	0

This instruction loads the general register specified by the R field with the contents of the external register specified by the E field. See 6-151 for the addresses of the 128 input-addressable external registers.

The 'C' and 'Z' latches are not changed when an 'input' instruction is executed.

An 'input' instruction can be executed at program level 1, 2, 3, or 4. An attempt to execute this instruction at program level 5 causes the L1 input/output check interrupt request to be set. The check is also set if the external register address is not assigned or is not recognized by any adapter. It is also set if incorrect parity is detected on the CCU inbus when an input instruction is executed.

Note: *If register 0 (IAR) is specified as R, a branch to the effective address formed in register 0 occurs.*

Output

0	1-3	4	5-7	8-11	12	13	14	15
0	E	0	R	E	0	1	0	0

This instruction places the contents of the general register specified by the R field in the external register specified by the E field. The addresses of the 128 output-addressable registers are shown on 6-151.

The 'C' and 'Z' latches are not changed when an 'output' instruction is executed.

An 'output' instruction can be executed at program level 1, 2, 3, or 4. An attempt to execute this instruction at program level 5 causes the L1 input/output check interrupt request to set. The check also sets if the external register address is not assigned or is not recognized by any adapter. An output instruction executed at program level 2, 3, or 4, or level 1 during IPL phase 3 also causes the CRC data register in the CCU to be loaded with the contents of byte 1 of the register specified by R.

Note: *If register 0 (IAR) is specified by E, a branch to the effective address formed in register 0 occurs. If register 0 is specified by R and one of the general registers is specified by E, the content of the general register is not changed, and parity is regenerated.*

Exit

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0

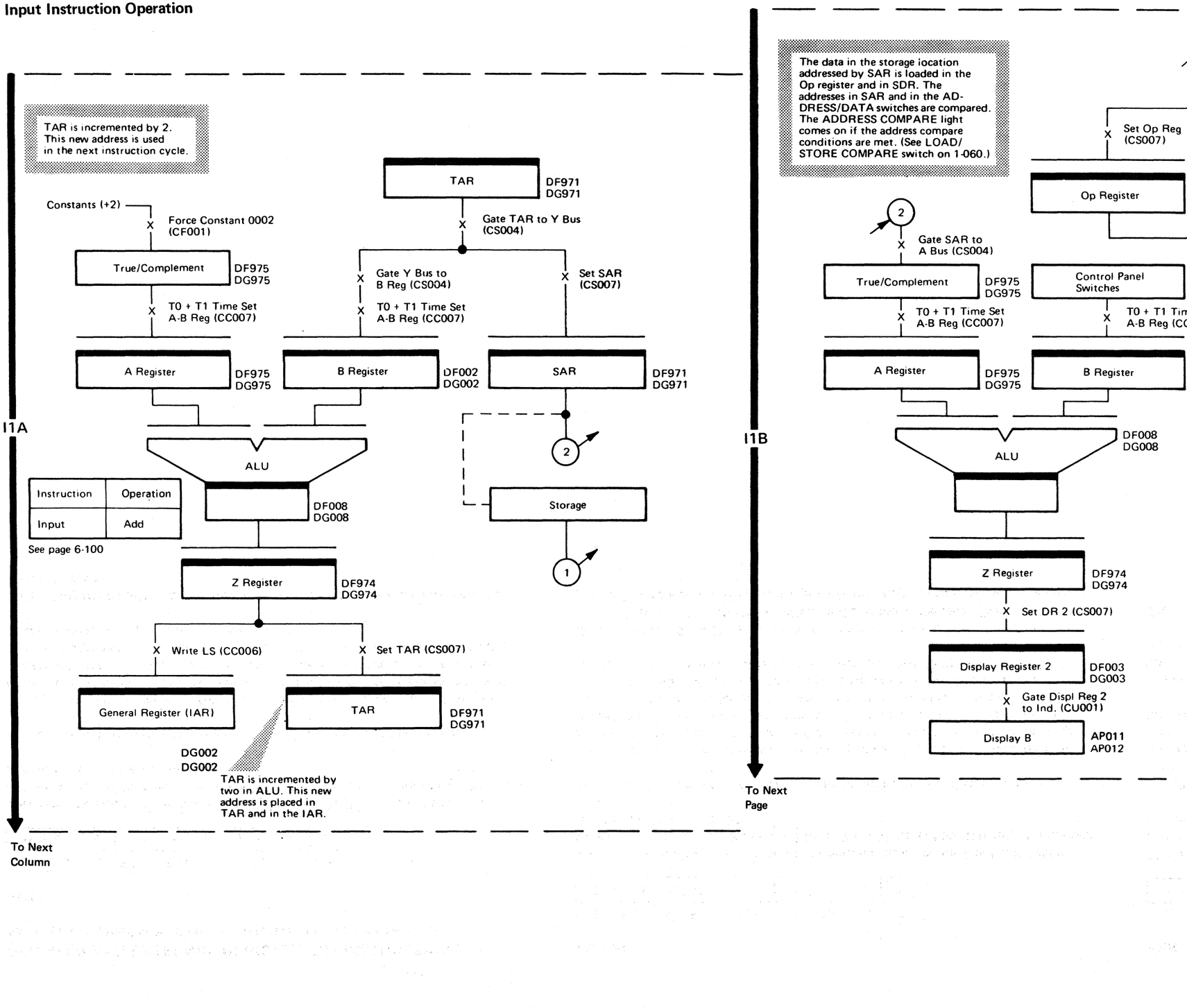
This instruction is used to leave any of the five program levels. When an 'exit' instruction is executed at a program level, the 'interrupt entered' latch for that program level is reset.

If 'exit' is executed at program level 5, the program level 4 supervisor interrupt request is set. If no other interrupt requests are present, the next instruction executed is the instruction at the starting address for program level 4. If other interrupt requests are present, the next instruction executed is the instruction at the starting address of the highest program level requested.

If level 5 is masked off and no interrupt requests are pending at any level, then an 'exit' instruction will cause the CCU to go into the 'Wait' state (take idle cycles) until an interrupt occurs.

The 'C' and 'Z' latches are not changed.

Input Instruction Operation



Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

Input Only

I1C

The contents of the register specified by the E field are placed in the SDR.

CCU External Registers

X Input Instruction (CD003)

X Gate CCU Indata to Y Bus (CS004)

Adapters

X Input Instruction (CD003)

X Gate Inbus to Y Bus (CS004)

General Register

X Gate Y Bus to B Reg (CS004)

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU

DF974 DG974

Instruction	Operation
Input	B Reg Direct

See page 6-100.

SAR

X Set LAR (CS001)

LAR

Z Register — DF974 DG974

X Gate Z Bus to M Bus (CS005)

X Set SDR Byte (CS007)

SDR — DN001

(1)

To Next Column

Input Only

I1D

The contents of the SDR are loaded into the general register specified by the R field. TAR is also loaded if this general register is IAR. The contents of TAR are loaded into SAR.

(1)

X Gate SDR Bits to A Bus (CF003)

True/Complement — DF975 DG975

X T0 + T1 Time Set A-B Reg (CC007)

A Register — DF975 DG975

ALU

DF974 DG974

Instruction	Operation
Input	A Reg Direct

See page 6-100.

Z Register — DF974 DG974

X Set TAR (CS007)

X Write LS (CC006)

TAR — DF971 DG971

General Register (R) — DF002 DG002

X Gate TAR to Y Bus (CS004)

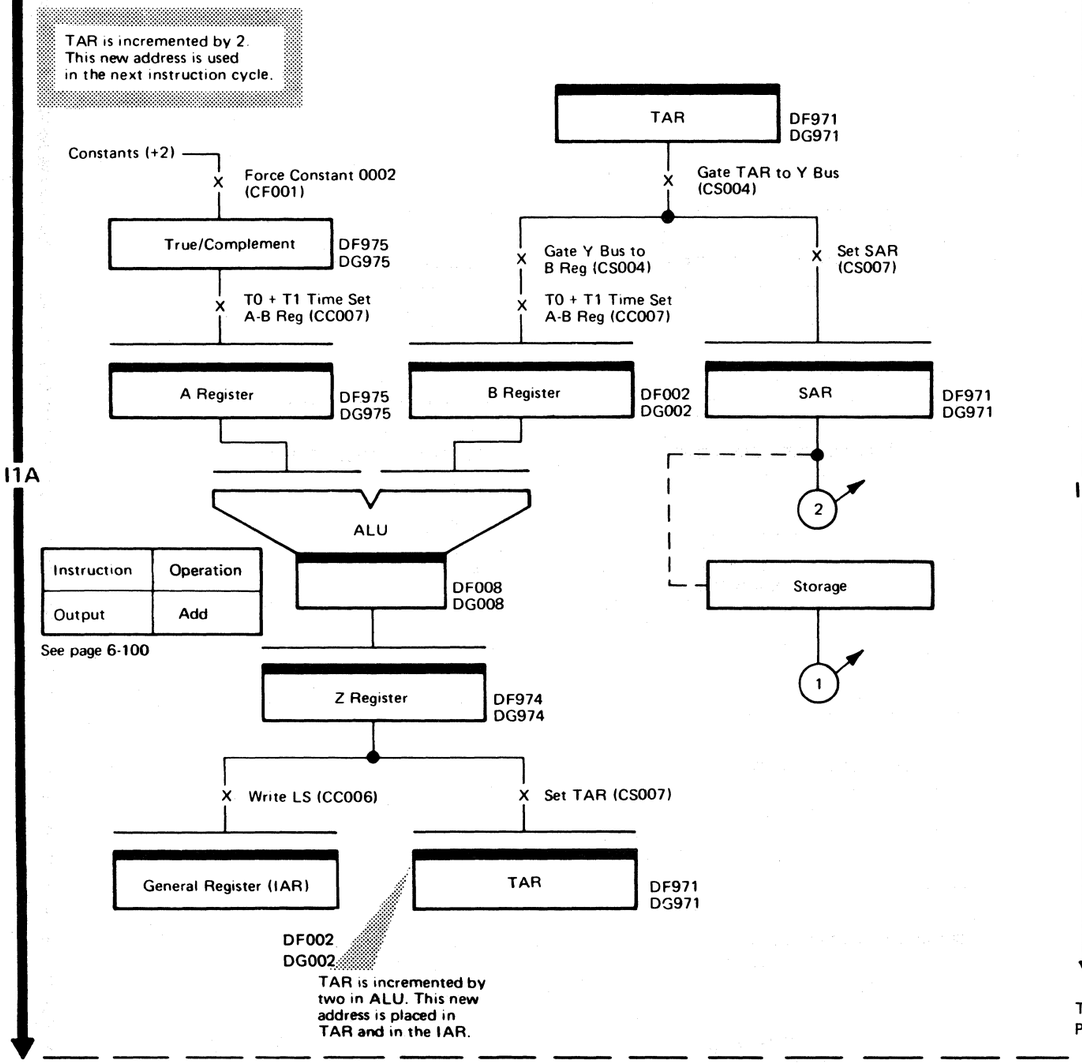
X Set SAR (CS007)

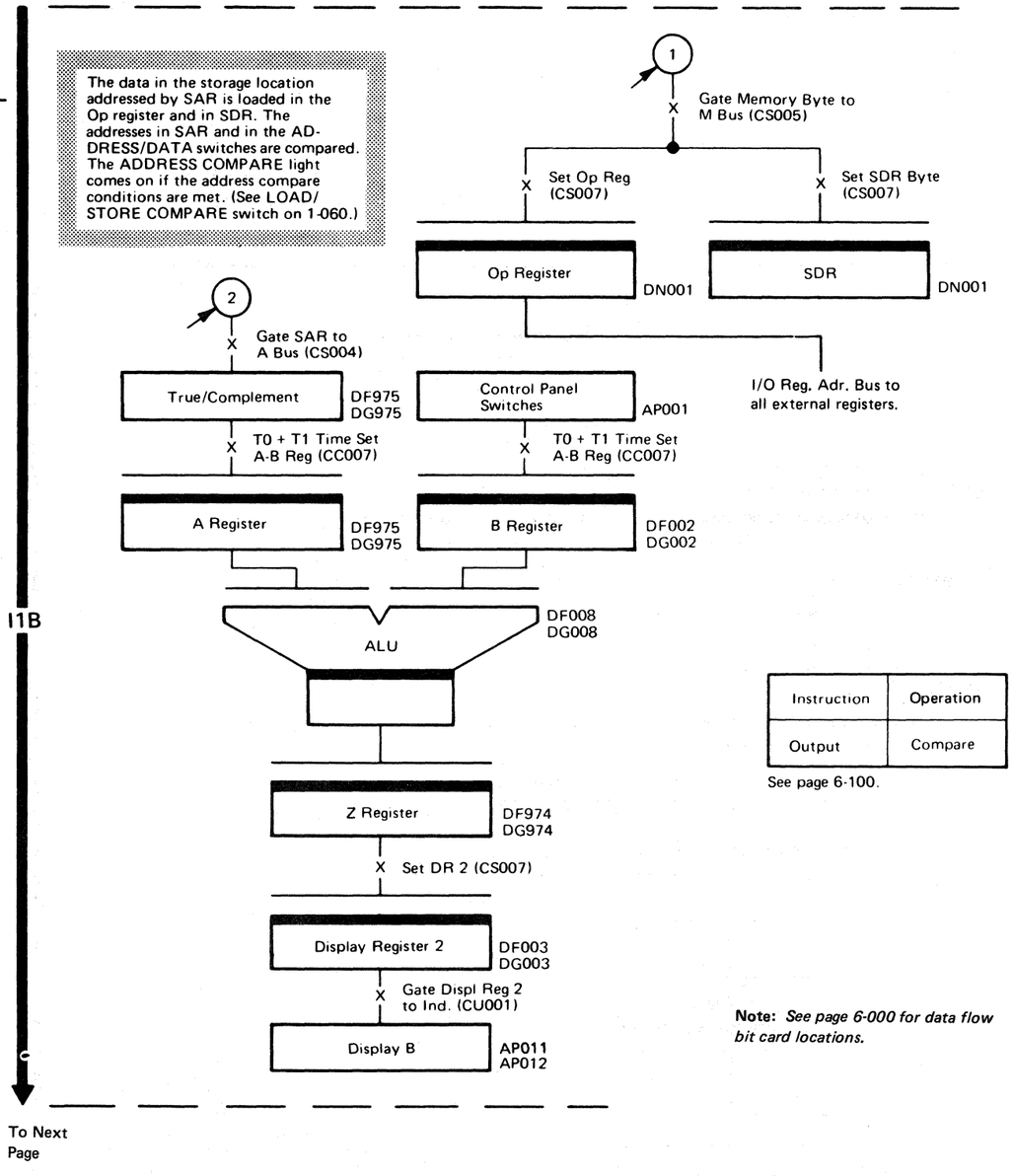
SAR — DF971 DG971

End of Instruction

Note: *See page 6-000 for data flow bit card locations.*

Output Instruction Operation





Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

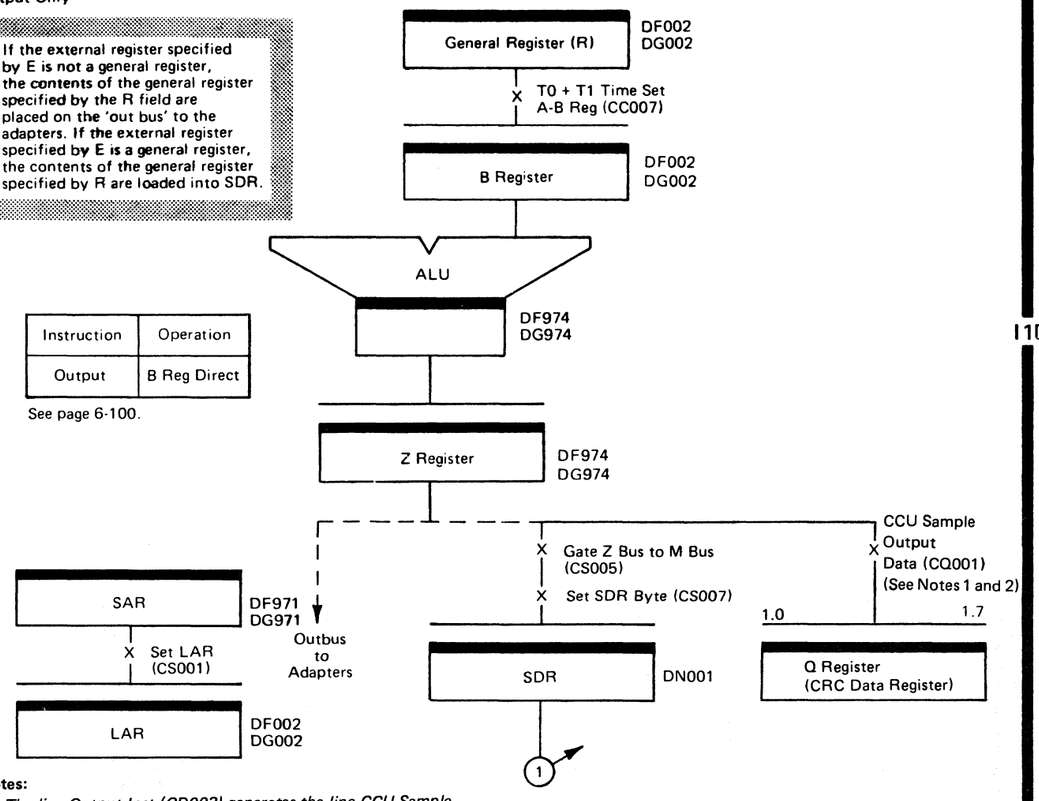
I1C

Output Only

If the external register specified by E is not a general register, the contents of the general register specified by the R field are placed on the 'out bus' to the adapters. If the external register specified by E is a general register, the contents of the general register specified by R are loaded into SDR.

Instruction	Operation
Output	B Reg Direct

See page 6-100.



Notes:

1. *The line Output Inst (CD003) generates the line CCU Sample Output Data (CQ001) which is active during CD time.*
2. *The line CCU Sample Output Data causes the contents of the Z Register byte 1 to be set in the CRC data register.*

To Next Column

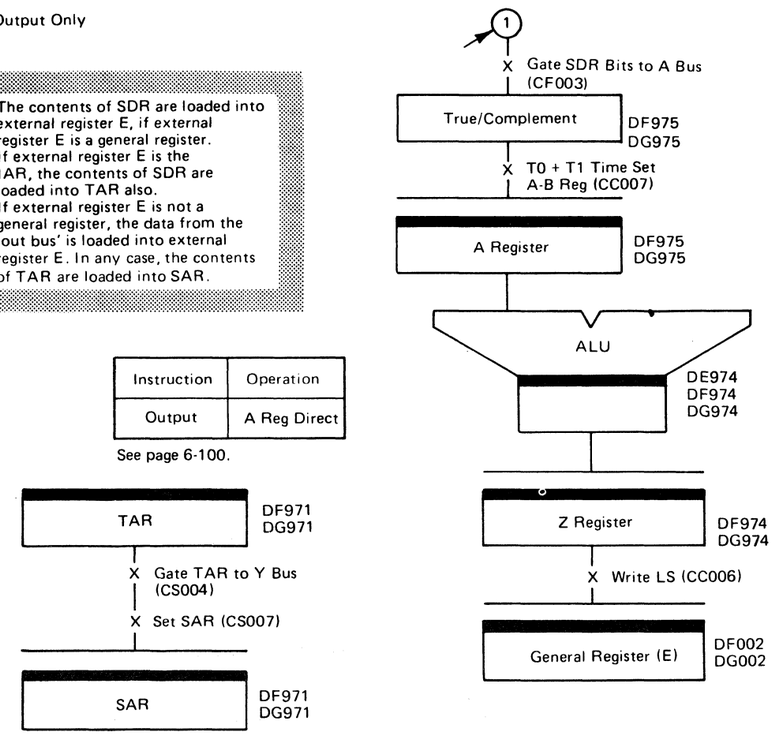
I1D

Output Only

The contents of SDR are loaded into external register E, if external register E is a general register. If external register E is the IAR, the contents of SDR are loaded into TAR also. If external register E is not a general register, the data from the 'out bus' is loaded into external register E. In any case, the contents of TAR are loaded into SAR.

Instruction	Operation
Output	A Reg Direct

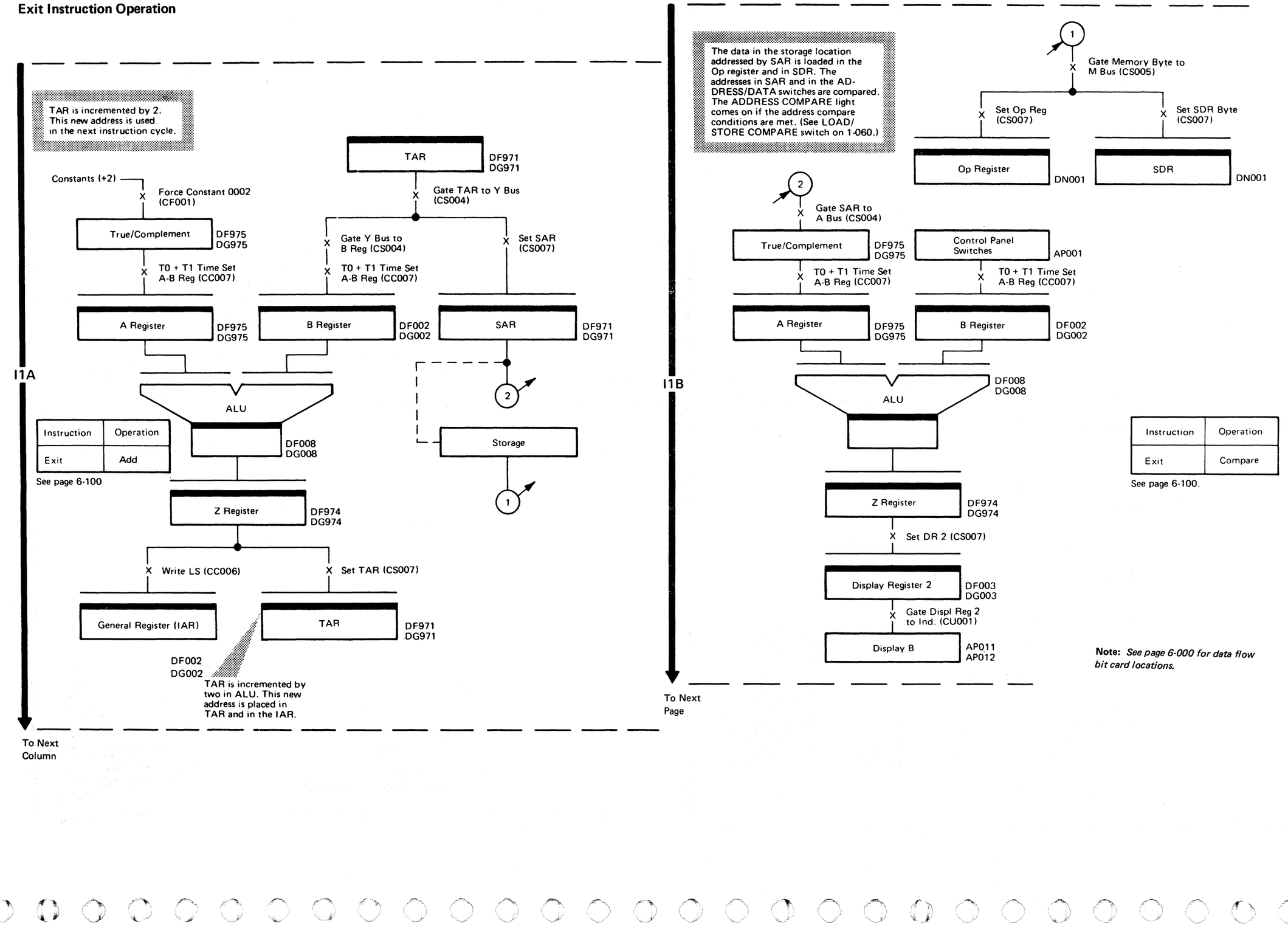
See page 6-100.



End of Instruction

Note: *See page 6-000 for data flow bit card locations.*

Exit Instruction Operation



Note: *See page 6-000 for data flow bit card locations.*

From Preceding Page

I1C

Exit Only

The contents of SAR are loaded into LAR.

SAR — DF971 DG971

X Set LAR (CS001)

LAR — DF002 DG002

I1D

Exit Only

The contents of the IAR for the next program level to be active are loaded into TAR and SAR.

Instruction	Operation
Exit	B Reg Direct

See page 6-100.

General Register (IAR) — DF002 DG002

X T0 + T1 Time Set A-B Reg (CC007)

B Register — DF002 DG002

ALU

DF974 DG974

Z Register — DF974 DG974

X Set TAR (CS007)

TAR — DF971 DG971

X Gate TAR to Y Bus (CS004)

X Set SAR (CS007)

SAR — DF971 DG971

End of Instruction

Note: *See page 6-000 for data flow bit card locations.*

CCU INPUT INSTRUCTIONS

The central control unit (CCU) has 44 assigned input instructions. These input instructions set bits in a general register to indicate various hardware conditions.

Inputs X'00' to X'1F'
General Registers

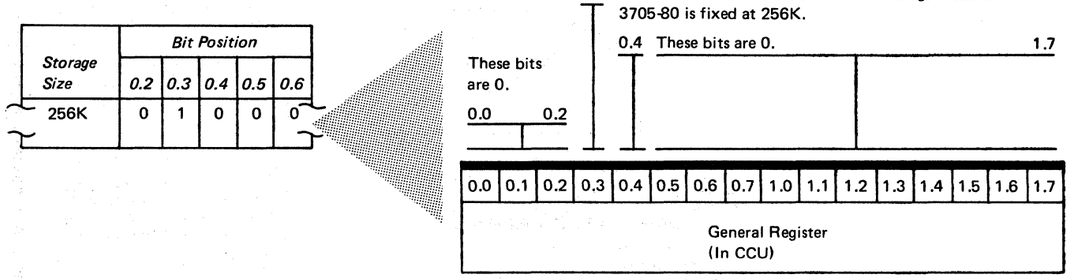
Inputs X'00'—X'1F' load the contents of the general register specified by the E field into the general register specified by the R field.

The contents of the general register specified by the E field are set in the B register at I1C time. Refer to the input instruction on page 6-710.

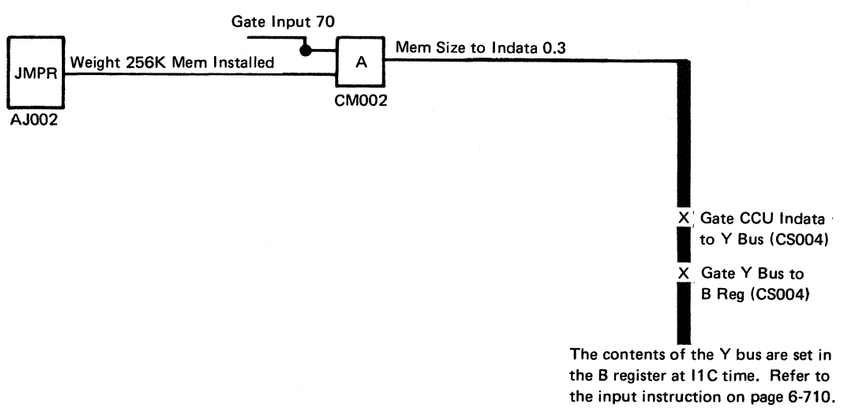
Input X'70' Storage Size Installed

Input X'70' turns on bit 0.3 of the general register specified by the R field. Setting bit 0.3 of the general register to "1" indicates that the 3705-80 contains 256K bytes of storage.

General Register Bit Definitions



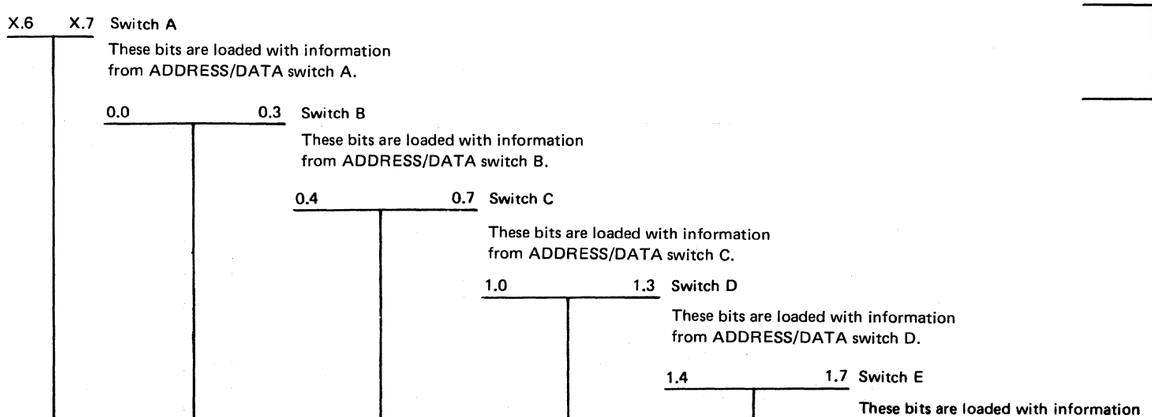
Hardware Function



Input X'71' Panel Addr/Data Entry Digits

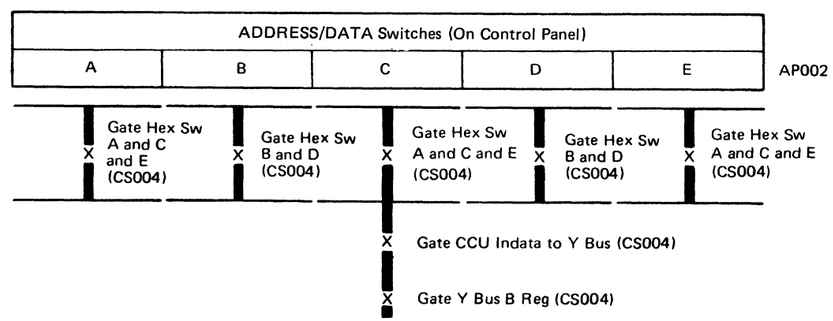
Input X'71' causes the general register specified by the R field to be loaded according to the setting of the ADDRESS/DATA switches on the control panel.

General Register Bit Definitions



X.6	X.7	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7
General Register R (In CCU)																	

Hardware Function



The contents of the Y bus are set in the B register at I1C time. Refer to the input instruction on page 6-710.

Input X'72' Display/Function Select Switch

Input X'72' causes the general register specified by the R field to be loaded with information indicating the position of the DISPLAY/FUNCTION SELECT switch.

General Register Bit Definitions

0.0 — 0.2 These bits are "0".

0.3 Storage Address

A "1" indicates that the DISPLAY/FUNCTION SELECT switch is in STORAGE ADDRESS.

0.4 Register Address

A "1" indicates that the DISPLAY/FUNCTION SELECT switch is in REGISTER ADDRESS.

0.5 — 0.7 These bits are "0".

1.0 This bit is "0".

1.1 Function Select 1

A "1" indicates that the DISPLAY/FUNCTION SELECT switch is in FUNCTION 1.

1.2 Function Select 2

A "1" indicates that the DISPLAY/FUNCTION SELECT switch is in FUNCTION 2.

1.3 Function Select 3

A "1" indicates that the DISPLAY/FUNCTION SELECT switch is in FUNCTION 3.

1.4 Function Select 4

A "1" indicates that the DISPLAY/FUNCTION SELECT switch is in FUNCTION 4.

1.5 Function Select 5

A "1" indicates that the DISPLAY/FUNCTION SELECT switch is in FUNCTION 5.

1.6 Function Select 6

A "1" indicates that the DISPLAY/FUNCTION SELECT switch is in FUNCTION 6.

1.7 This bit is "0".

0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7

General Register
(In CCU)

Hardware Function

DISPLAY/FUNCTION SELECT Switch — AP005

X Gate Input 72 (CQ004)

X Gate CCU Indata to Y Bus (CS004)

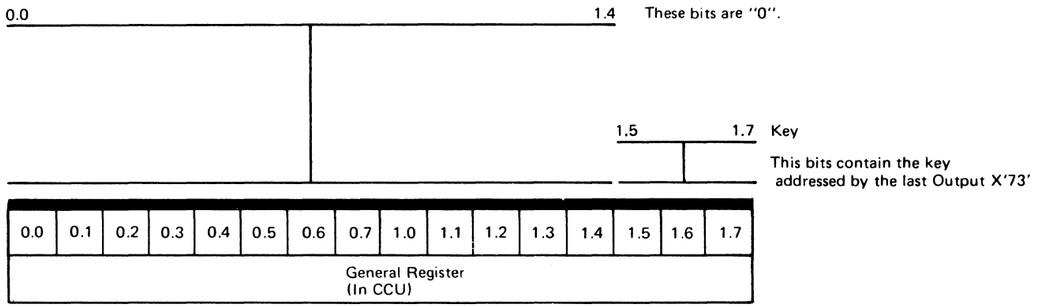
X Gate Y Bus to B Reg (CS004)

The contents of the Y bus are set in the B register at 11C time. Refer to the input instruction on page 6-710.

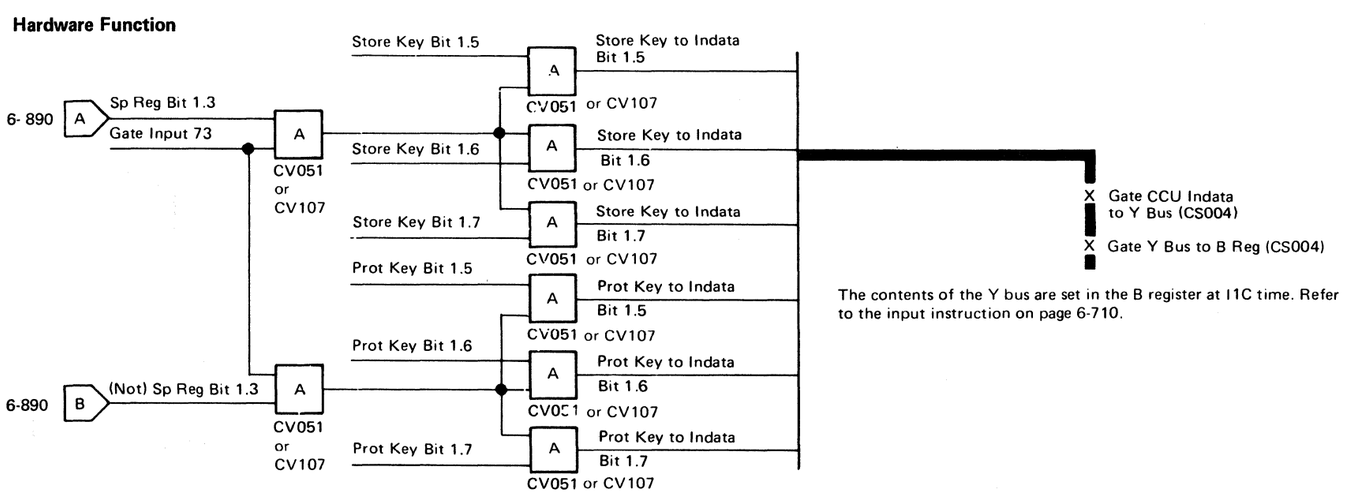
Input X'73' Insert Key

Input X'73' is associated with storage protection. When executed, the key addressed by the last Output X'73' is inserted into bits 1.5-1.7 of the general register specified by the R field.

General Register Bit Definitions



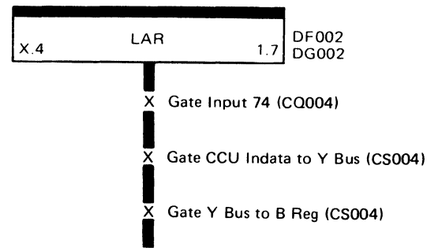
Hardware Function



The contents of the Y bus are set in the B register at I1C time. Refer to the input instruction on page 6-710.

Input X'74' Lagging Address Register

When an Input X'74' is executed, the contents of the lagging address register (LAR) are transferred to the register specified by the R field. If this input is executed at program level 2, 3, or 4, the address from LAR is of the last instruction executed before the input. If this input is executed in program level 1, the address from LAR is of the last instruction executed before entering level 1.



The contents of the Y bus are set in the B register at I1C time. Refer to the input instruction on page 6-710.

Input X'76' Adapter Level 1 Interrupt Requests

Input X'76' is associated with program level 1 interrupt requests. Execution of this instruction loads the general register specified by the R field with bits that indicate the origin of an adapter level 1 interrupt request.

General Register Bit Definitions

0.0 Type 4 CA #1 or #2
A "1" indicates that type 4 CA #1 or #2 has requested a program level 1 interrupt.

0.1 Type 2 Scanner L1
A "1" indicates that the type 2 scanner has requested a program level 1 interrupt.

0.2 This bit is 0.

0.3 This bit is 0.

0.4 This bit is 0.

0.5 Type 1 CA or Selected Type 4 CA L1
A "1" indicates that the type 1 CA or selected type 4 CA has requested a program level 1 interrupt.

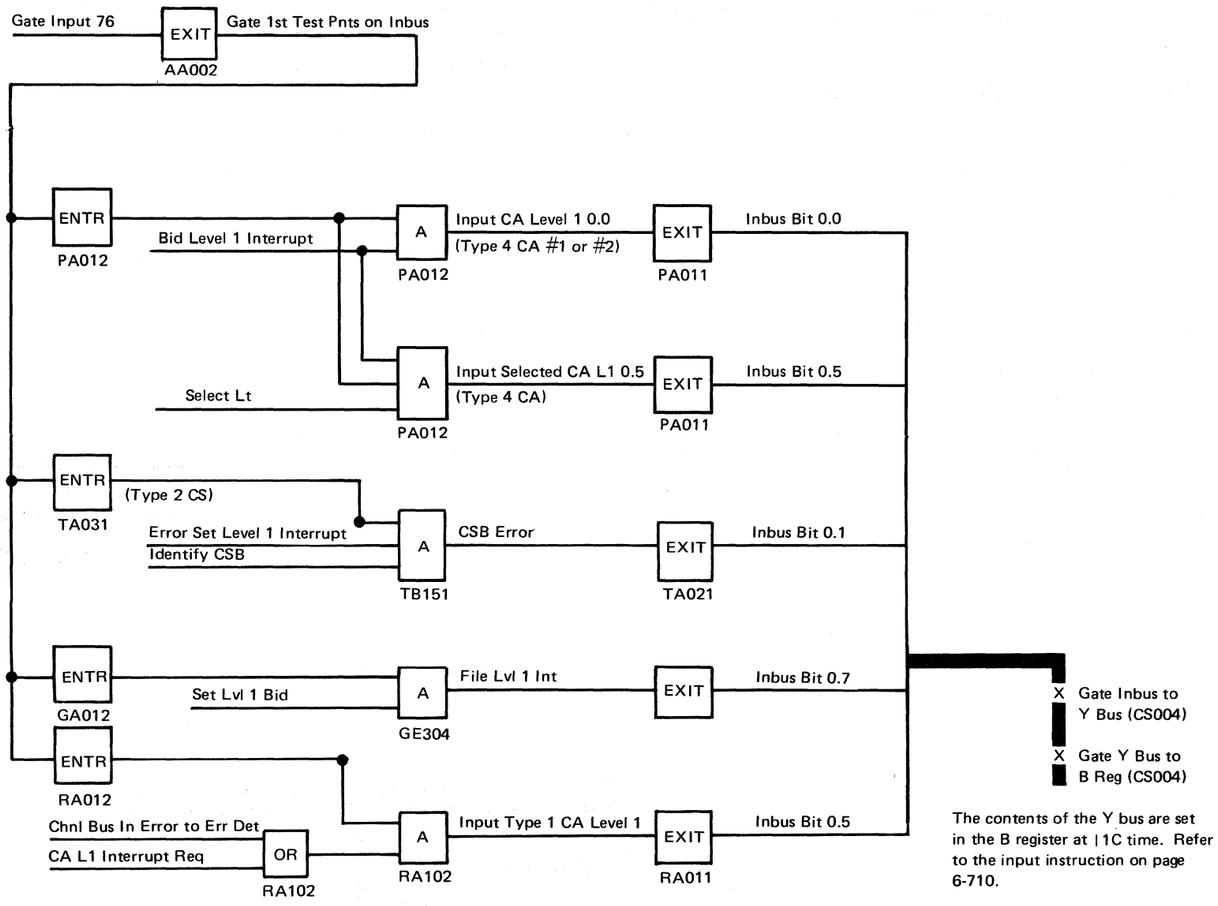
0.6 This bit is 0.

0.7 Remote Program Loader L1
A"1" indicates that the Remote Diskette Controller has requested a program level 1 interrupt.

1.0 These bits are 0

0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7
General Register (In CCU)															

Hardware Function



The contents of the Y bus are set in the B register at I1C time. Refer to the input instruction on page 6-710.

Input 'X77' Adapter Level 2 or 3 Interrupt Requests

Input X'77' is associated with program level 2 and level 3 interrupt requests. Execution of this instruction loads the general register specified by the R field with bits to indicate the origin of an adapter level 2 or 3 interrupt request.

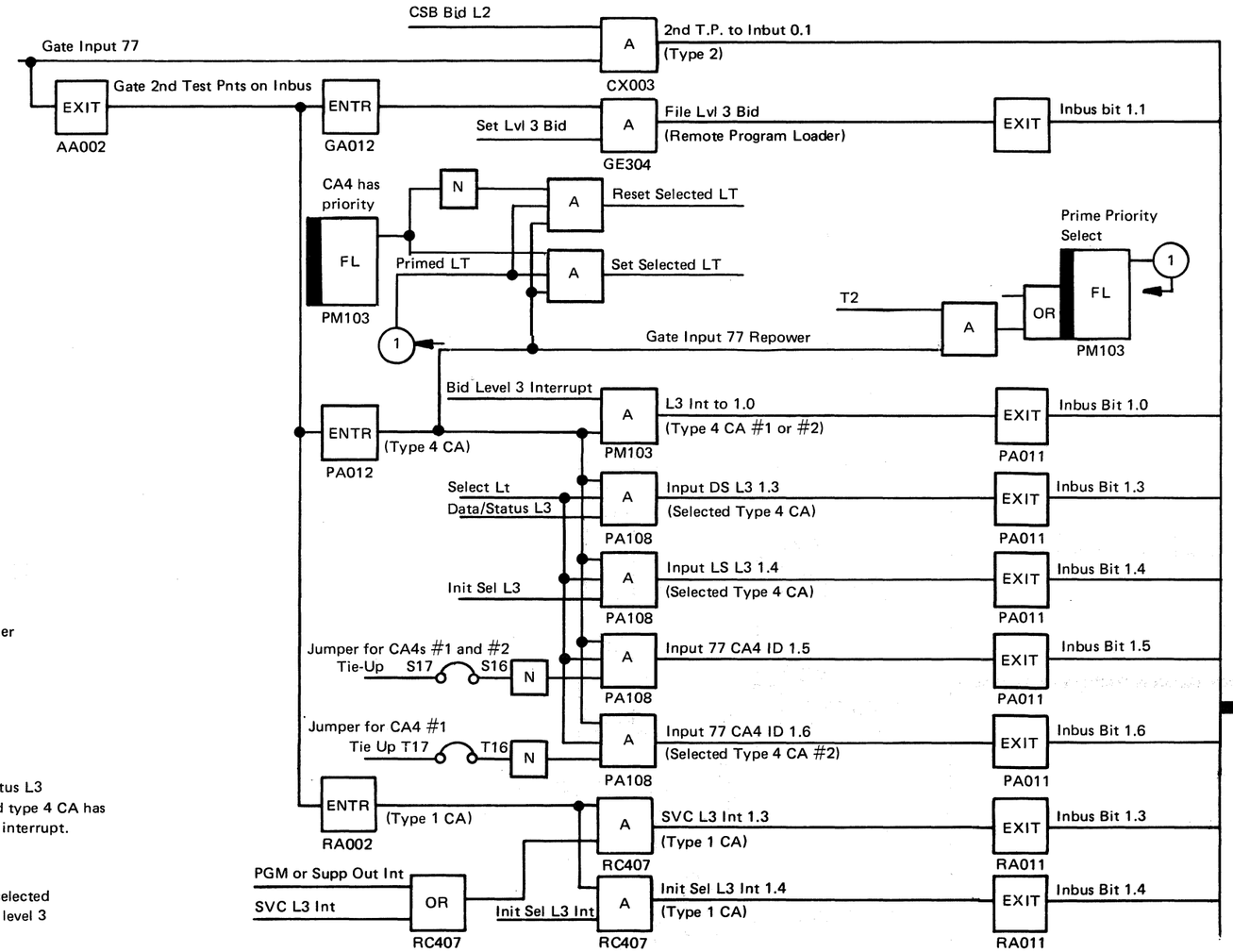
When priority selection is required with two type 4 CAs, this instruction sets or resets the selected latch in each type 4 CA according to the state of the 'CA4 has priority' latch. It also resets the 'prime priority select' latch.

General Register Bit Definitions

- 0.0 This bit is 0.
- 0.1 A "1" indicates that the type 2 scanner has requested a program level 2 interrupt.
- 0.2 – 0.7 These bits are 0
- 1.0 Type 4 CA L3
  A "1" indicates that type 4 CA #1, #2, has requested a program level 3 interrupt.
- 1.1 Remote Program Loader L3
  A "1" indicates that the Remote Diskette Controller has requested a program level 3 interrupt.
- 1.2 This bit is 0.
- 1.3 Type 1 or Selected Type 4 CA Data/Status L3
  A "1" indicates that a type 1 or selected type 4 CA has requested a program level 3 data service interrupt.
- 1.4 Type 1 or Selected Type 4 CA L3
  A "1" indicates that the type 1 or selected type 4 CA has requested a program level 3 initial selection interrupt.
- 1.5, 1.6 00 – Type 4 CA #1 selected
  01 – Type 4 CA #2 selected
- 1.7 This bit is 0.

0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7
General Register R (In CCU)															

Hardware Function

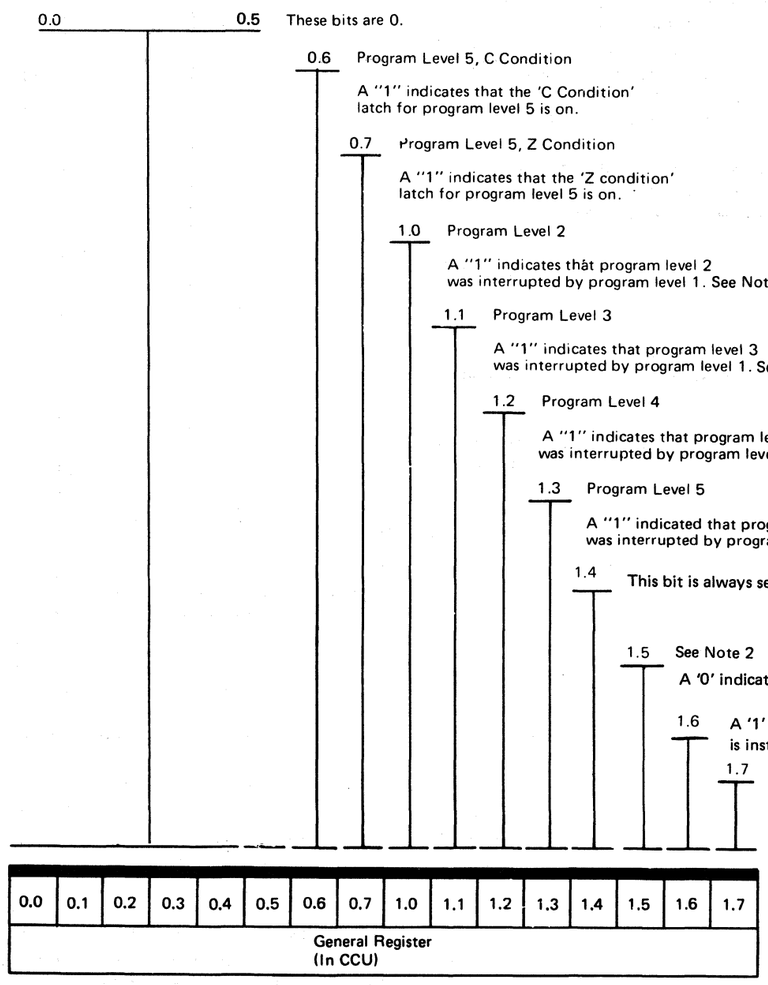


The contents of the Y bus are set in the B register at I1C time. Refer to the input instruction on page 6-710.

Input X'79' Utility

Input X'79' causes the general register specified by the R field to be loaded with information indicating (1) the state of the program level 5 C and Z condition latches, (2) the last program level to be active before a level 1 interrupt, (3) the state of the IPL escape control, and (4) the 3705-80 contains a type 1 or type 4 CA.

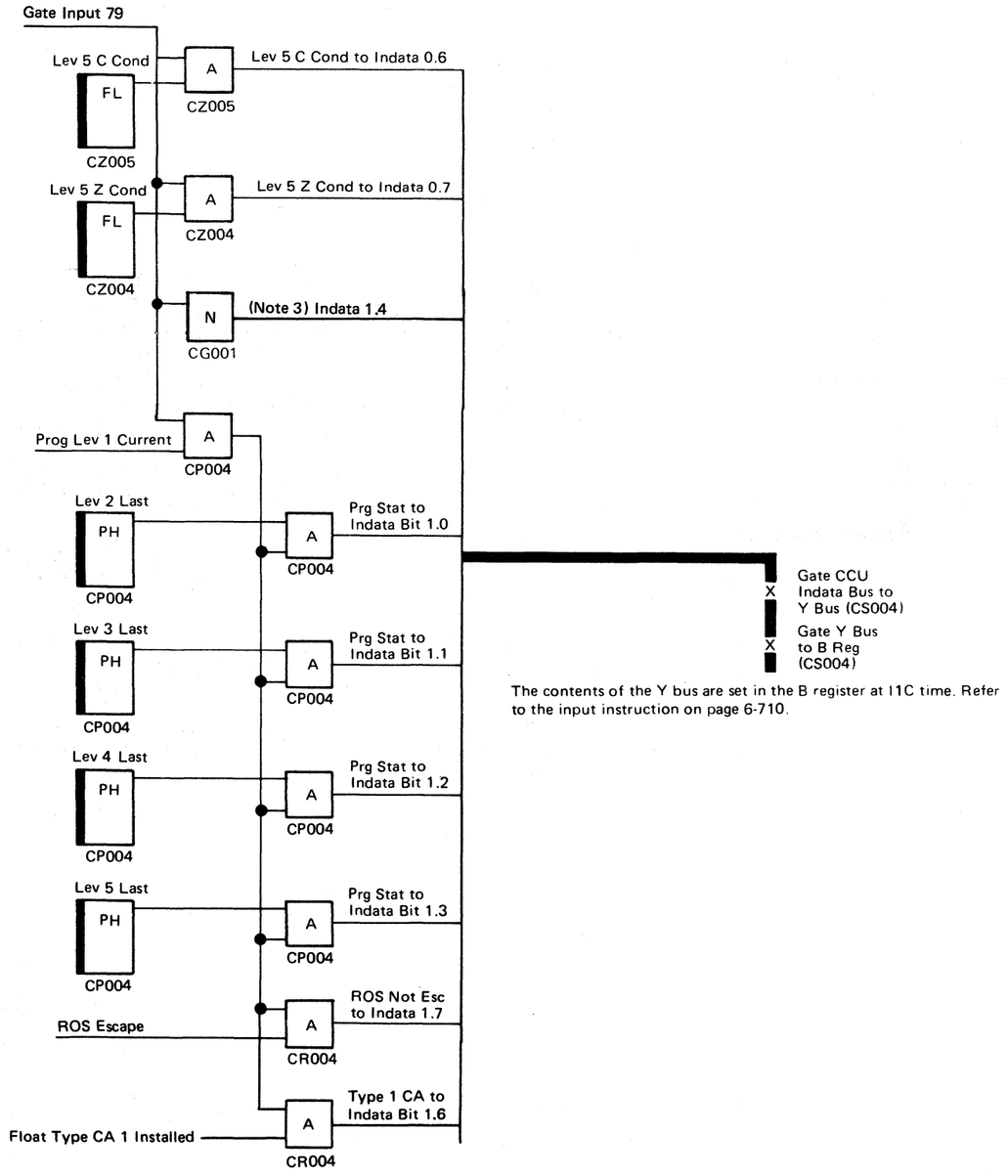
General Register Bit Definitions



Notes:

1. *Bits 1.0-1.3 and 1.6-1.7 are 0 if input X'79' is executed when not in program level 1.*
2. *The 3705-80 Communications Controller has no hardware to force a 0 in bit 1.5- it results as a default condition.*
3. *This bit always equals zero.*

Hardware Function



The contents of the Y bus are set in the B register at I1C time. Refer to the input instruction on page 6-710.

Input X'7B' BSC CRC Register

The old CRC accumulation in the P register and the new character in the Q register are combined in the new CRC generation circuitry. Input X'7B' selects the output lines (S0 to S15) from the new CRC generation circuitry that corresponds to BSC CRC checking.

CRC Generation Example

A typical update of the CRC, located in the Character Control Block area, is provided below.

1 Output X'7E' (Set Mask Bits) — to prevent interrupts.

2 Load Halfword — loads the P register with the old CRC accumulation. Each Load Halfword executed changes the contents of the P register; therefore, a Load Halfword instruction should not be executed again until the new accumulated CRC is loaded into a CCU general register.

3 Insert Character — places the new character in a general register.

4 Any output instruction — places the new character in the Q register when the general register used in step 3 is specified in the 'R' field.

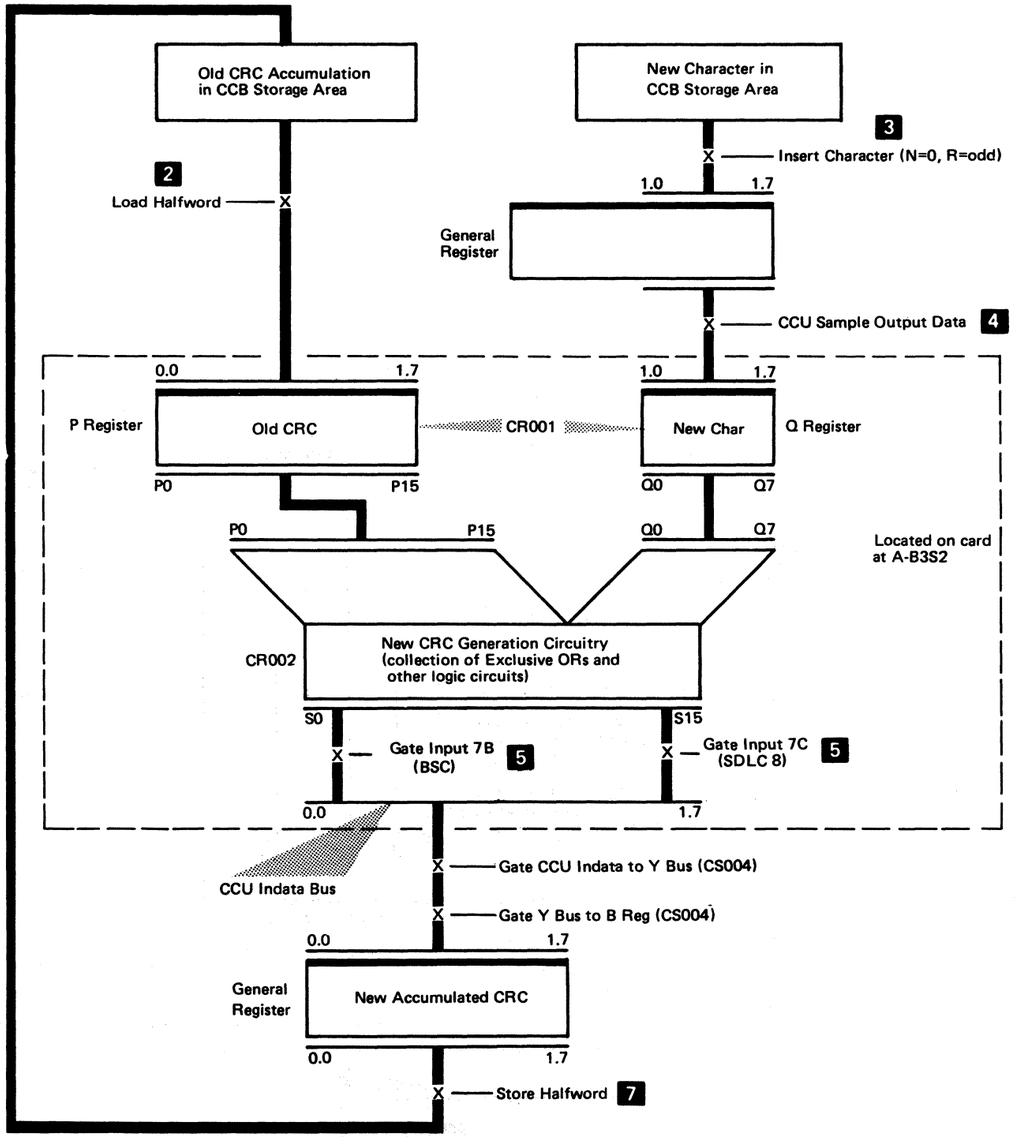
5 Input X'7B' (BSC CRC Register) or
Input X'7C' (SDLC 8 CRC Register) — selects the corresponding outputs of the new CRC generation circuitry and places the new accumulated CRC in the general register specified in the 'R' field.

6 Output X'7F' (Reset Mask Bits) — allows interrupts.

7 Store Halfword — stores new CRC accumulation in the CCB area on storage.

Input X'7C' SDLC 8 CRC Register

The old CRC accumulation in the P register and the new character in the Q register are combined in the new CRC generation circuitry. Input X'7C' selects the output lines (S0 to S15) from the new CRC generation circuitry that corresponds to SDLC 8 CRC checking.



Input X'7D' CCU Check Register

Input X'7D' sets the bits in the general register specified by the R field to correspond to the CCU check register. Pages 6-050 and 6-051 show the CCU check register.

General Register Bit Definition

0.0 Byte X Check

A "1" indicates a parity check in byte X (except for SDR).

0.1 Byte 0 Check

A "1" indicates a parity check in byte 0.

0.2 Byte 1 Check

A "1" indicates a parity check in byte 1 (bytes 1 or X for SDR).

0.3 L1 Program Check

A "1" indicates that a program check occurred while in program level 1.

0.4 SAR Check

A "1" indicates a storage address register parity check. Bit 0.0, 0.1, or 0.2 indicates which byte of the storage address register caused the check.

05. SDR Check

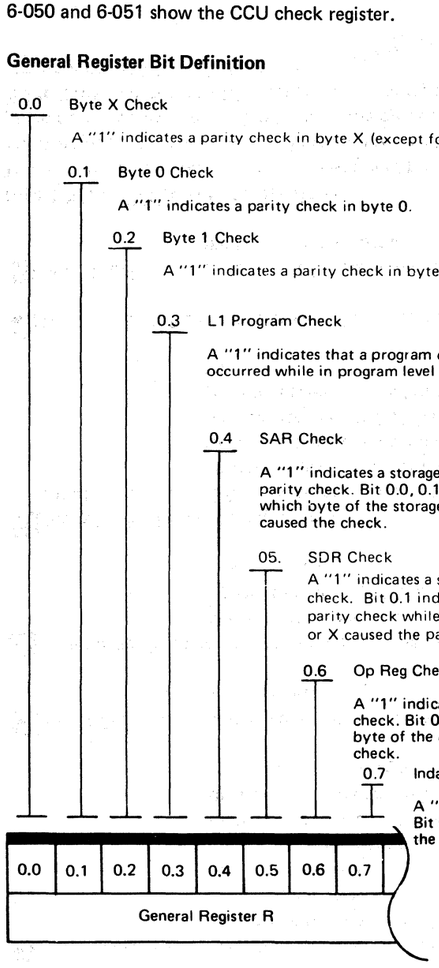
A "1" indicates a storage data register parity check. Bit 0.1 indicates SDR byte 0 caused the parity check while bit 0.2 indicates SDR bytes 1 or X caused the parity check.

0.6 Op Reg Check

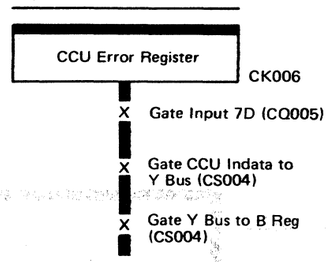
A "1" indicates an operation register parity check. Bit 0.0, 0.1, or 0.2 indicates which byte of the operation register caused the check.

0.7 Indata Bus Check

A "1" indicates an indata bus parity check. Bit 0.0, 0.1, or 0.2 indicates which byte of the indata bus caused the check.



Hardware Function



The contents of the Y bus are set in the B register out I1C time. Refer to the input instruction on page 6-710.

1.0 Cycle Counter Check

A "1" indicates that the CCU cycle counter signaled an even number of time slots to the CCU.

1.1 1.2 These bits are 0.

1.3 IPL Diskette Controller Error (see note)

1.4 IPL Media Error (see note)

1.5 CCU Checks

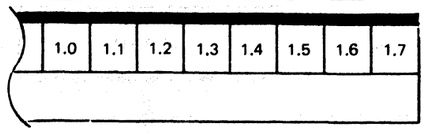
A "1" indicates the presence of a CCU check. This is a summary bit that is set to "1" whenever any of the CCU checks in this input are on. This bit should be checked first when checking for a CCU check condition.

1.6 Attachment Base Clock Check.

A "1" indicates a type 2 attachment base clock check. The type 2 scanner clock signaled an incorrect number of time slots.

1.7 CCU Clock Check

A "1" indicates a central control unit clock check. The CCU clock signaled an incorrect number of time slots.

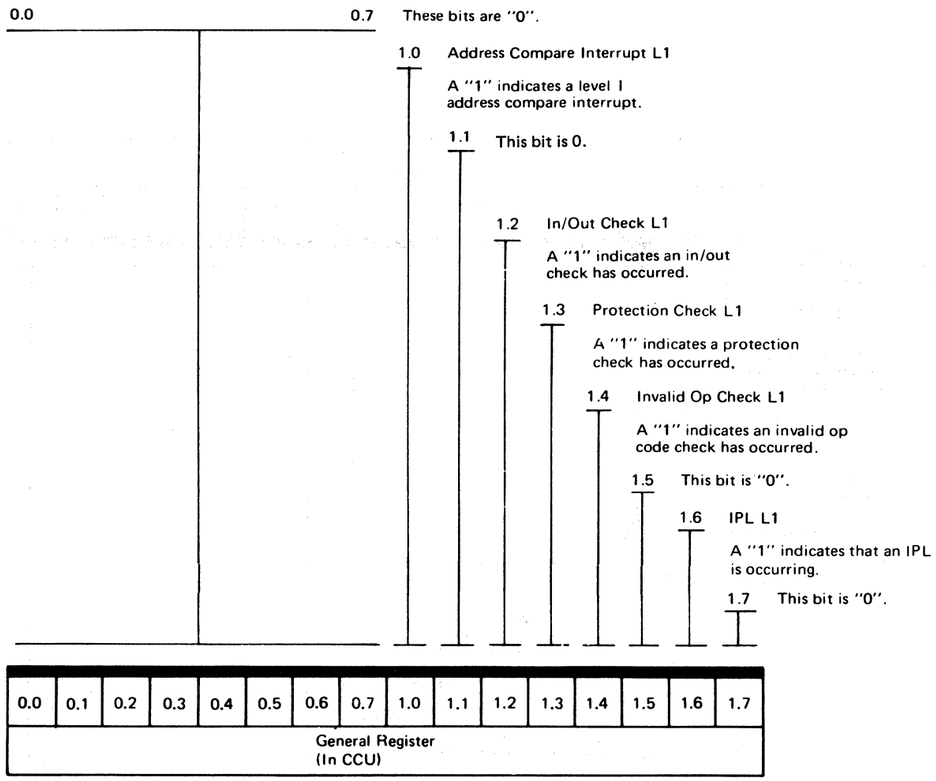


Note: A "1" indicates that an error message is stored at location X'0020'—X'003F'. Load Program 1 sets the indicator when the message is stored.

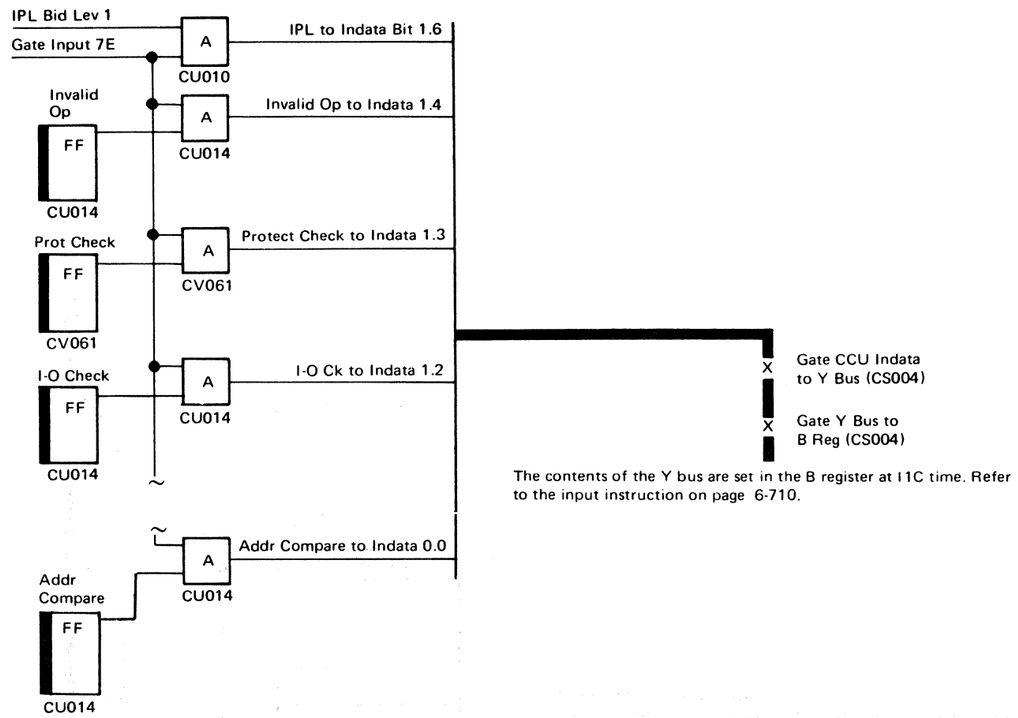
Input X'7E' CCU Level 1 Interrupt Requests

Input X'7E' sets the bits in the register specified by the R field to indicate which level 1 interrupt request is set. Bits 1.1—1.4 are set as the result of a program check in any level and cause a level 1 interrupt if the error occurred in program level 2-5. A program check in program level 1 causes an IPL. If a program check occurs during IPL, it causes a hard stop.

General Register Bit Definitions



Hardware Function

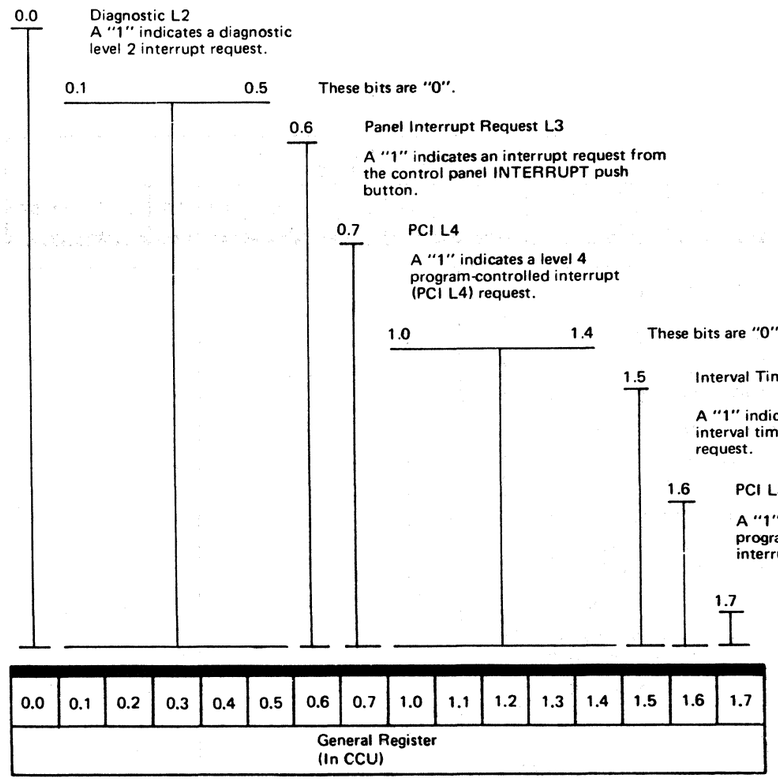


The contents of the Y bus are set in the B register at I1C time. Refer to the input instruction on page 6-710.

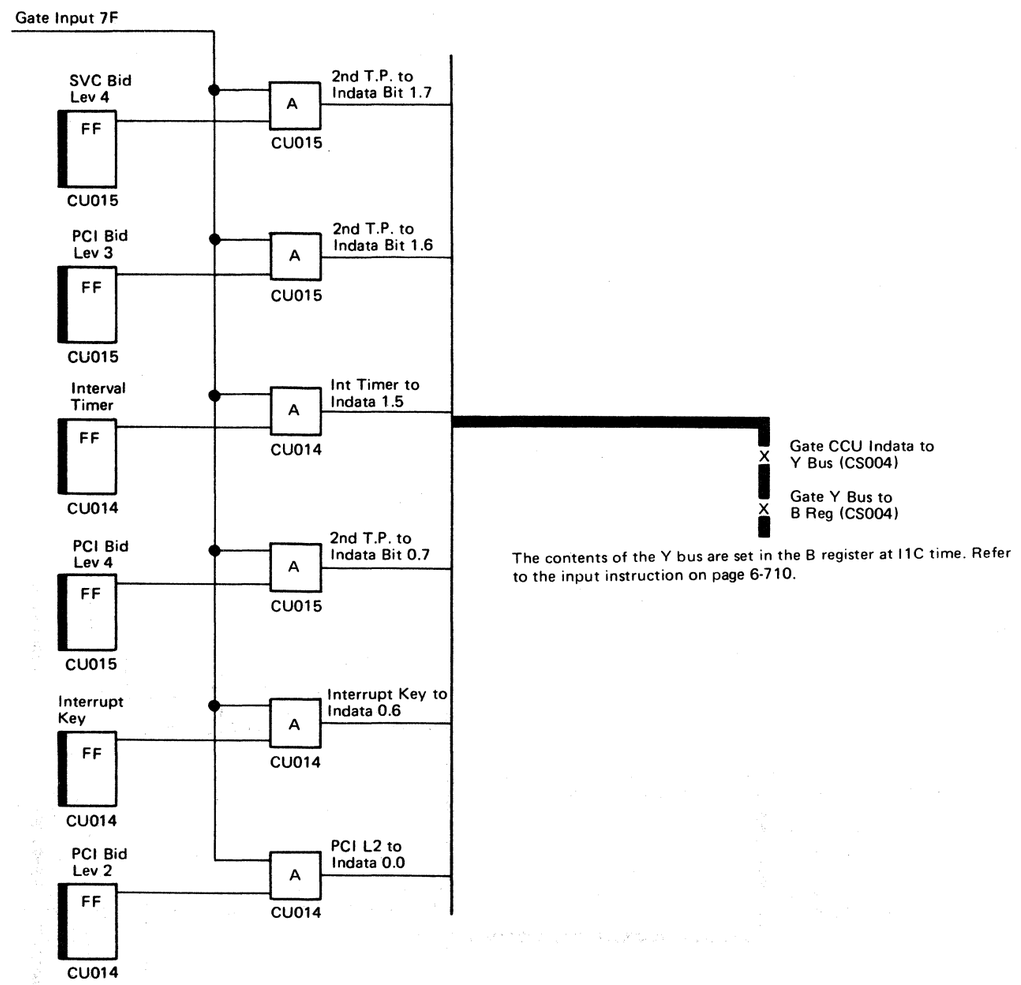
Input X'7F' CCU Level 2, 3, or 4 Interrupt Requests

Input X'7F' sets bits in the general register specified by the R field to indicate which level 2, 3, or 4 interrupt requests are set.

General Register Bit Definitions



Hardware Function



The contents of the Y bus are set in the B register at I1C time. Refer to the input instruction on page 6-710.

CCU OUTPUT INSTRUCTIONS

The CCU has 43 assigned output instructions. These output instructions set and reset various CCU latches and load external registers with data from general registers.

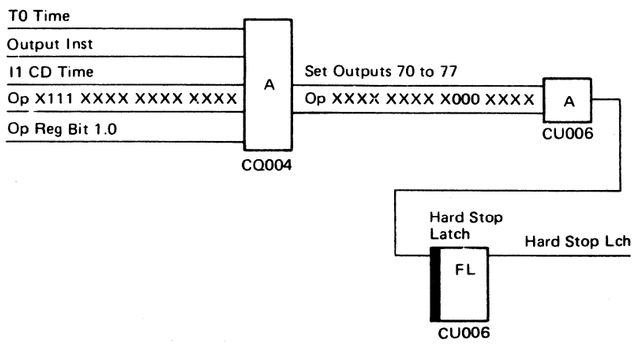
Outputs X'00' to X'1F' General Registers

Outputs X'00'-X'1F' load the contents of the general register specified by the R field into the general register specified by the E field.

At I1D time, the contents of the Z bus (contents of the register specified by the R field) are set in the general register specified by the E field. Refer to the output instruction on page 6-730.

Output X'70' Hardstop

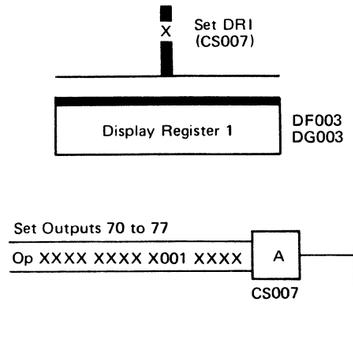
Output X'70' causes the 'hardstop' latch to set. The 3705-80 comes to a complete stop, and IPL is required to continue processing using the adapters. The bit settings are ignored since this output performs a control function.



Output X'71' Display Register 1

Output X'71' causes the contents of the general register designated by the R field to be loaded in display register 1. The PROGRAM DISPLAY light also turns on.

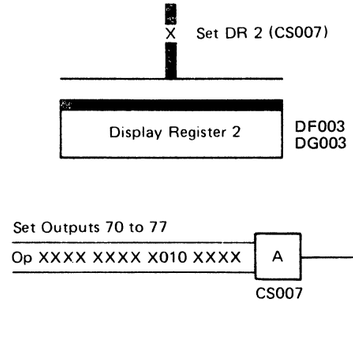
At I1D time, the contents of the Z bus (contents of the general register specified by the R field) are set in display register 1. Refer to the output instruction on page 6-730.



Output X'72' Display Register 2

Executing Output X'72' causes the contents of the general register specified by the R field to be loaded in display register 2. The PROGRAM DISPLAY light also turns on.

At I1D time, the contents of the Z bus (contents of the general register specified by the R field) are set in display register 2. Refer to the output instruction on page 6-730.

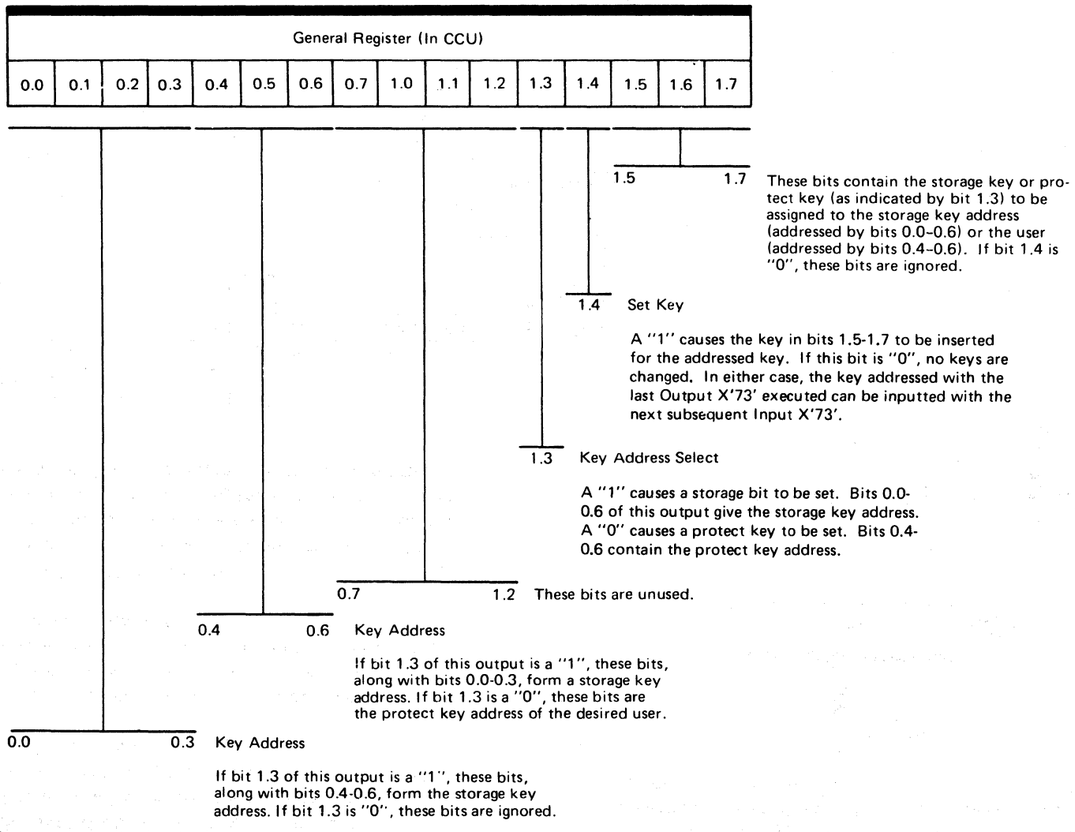


Output X'73' Set Key (Storage Protect) (Part 1 of 2)

Output X'73' is associated with storage protection. It is used to set either a storage key or a protect key with the contents of bits 1.5-1.7 of the general register designated by the R field. Bit 1.3 controls the selection of either a storage key or a protect key. If bit 1.4 is "1", the addressed key is set according to bits 1.5-1.7. If bit 1.4 is "0", the addressed key is not set.

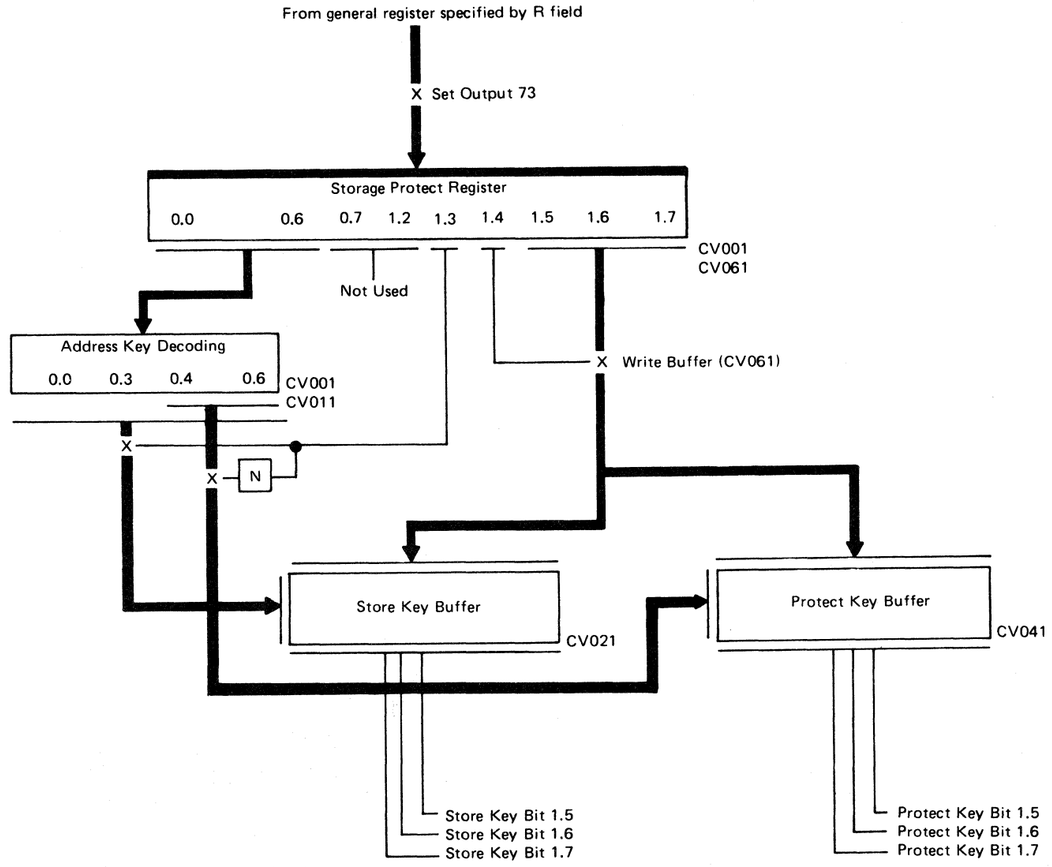
Input X'73' can be used to set bits in a general register according to the key addressed by the last Output X'73'.

General Register Bit Definitions

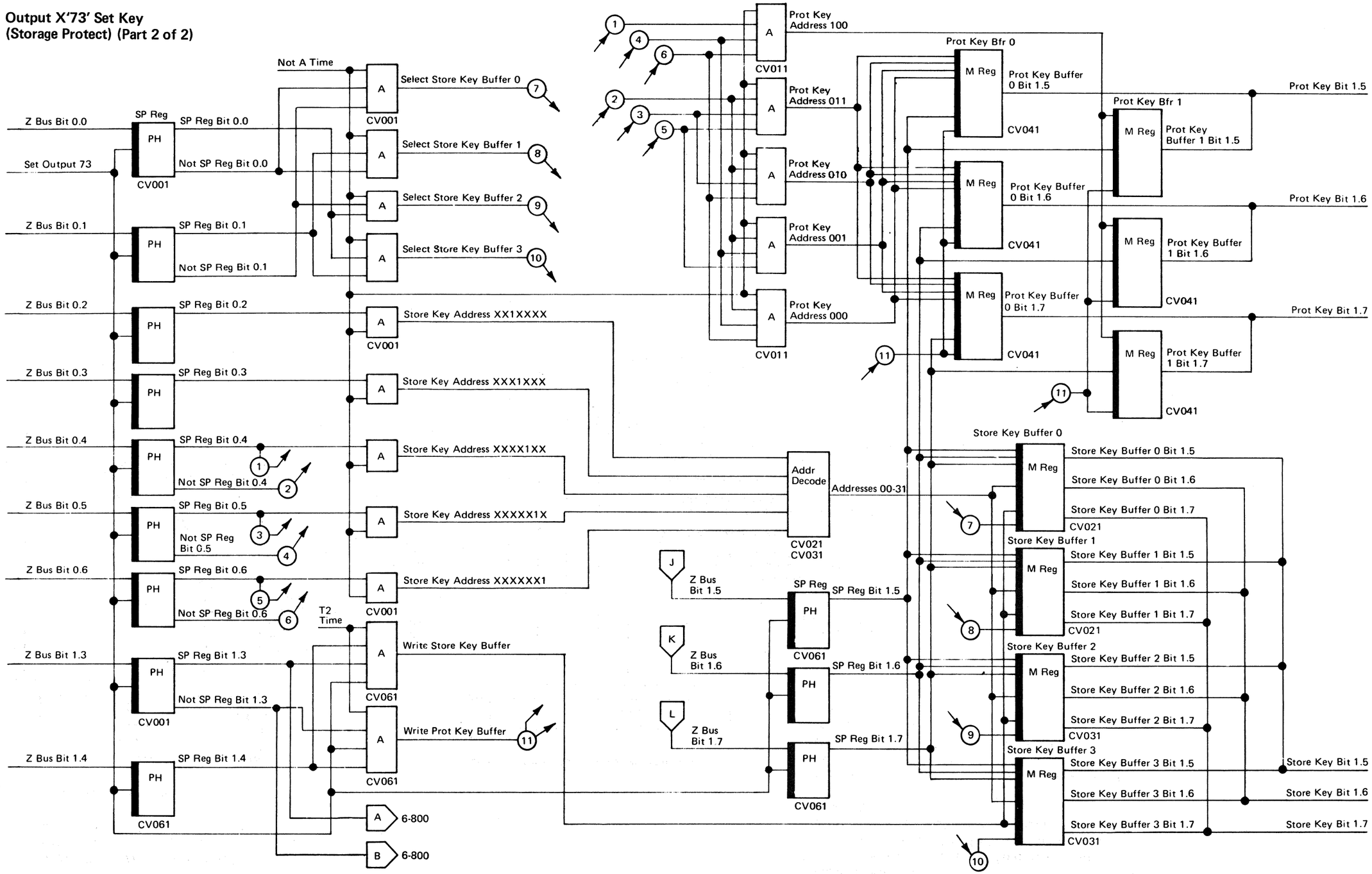


Hardware Function

The contents of the Z bus (contents of the general register specified by the R field) set storage protection at I1D time. Refer to the output instruction on page 6-730.



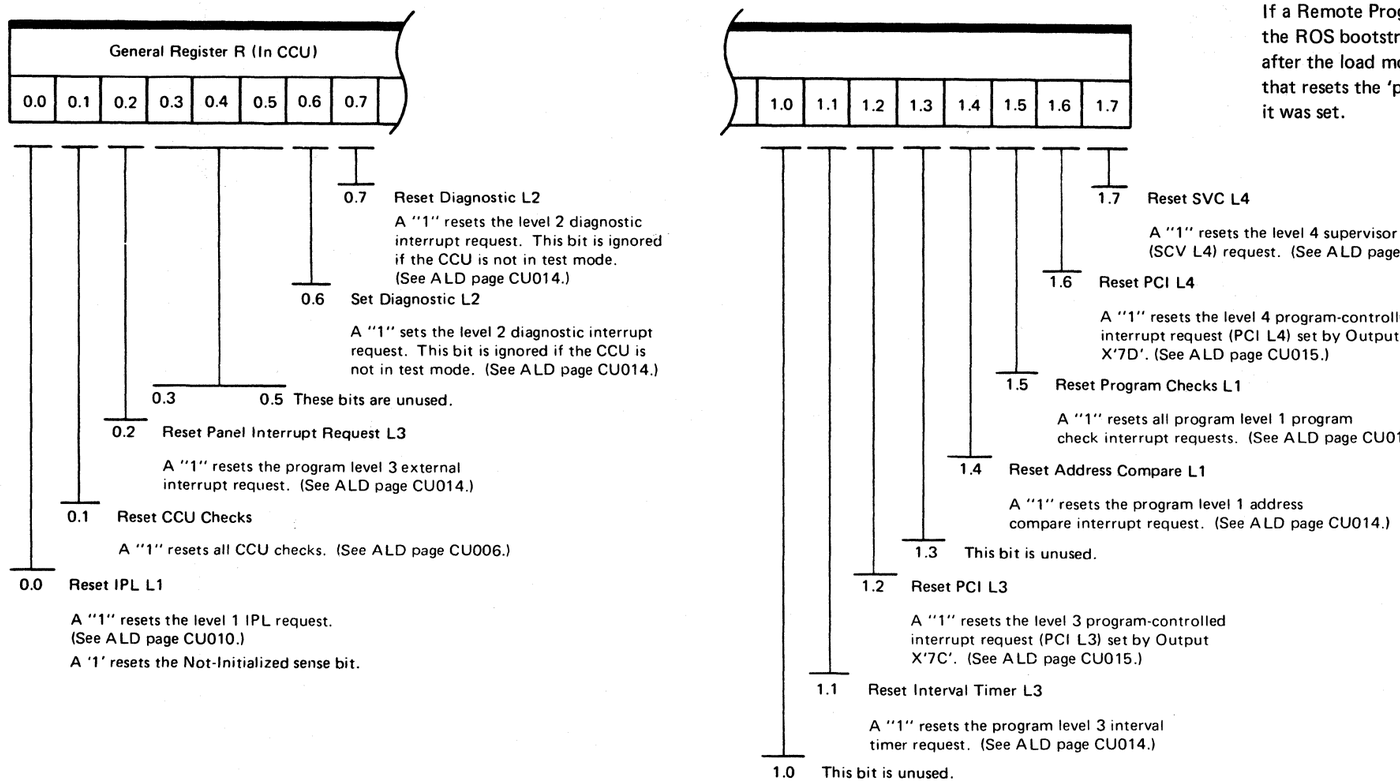
Output X'73' Set Key (Storage Protect) (Part 2 of 2)



Output X'77' Miscellaneous Controls

Output X'77' contains controls used to set or reset various interrupt requests.

General Register Bit Definitions



Hardware Function

At I1D time, the contents of the Z bus (contents of the general register specified by the R field) set the controls shown on this page. Refer to the output instruction on page 6-730.

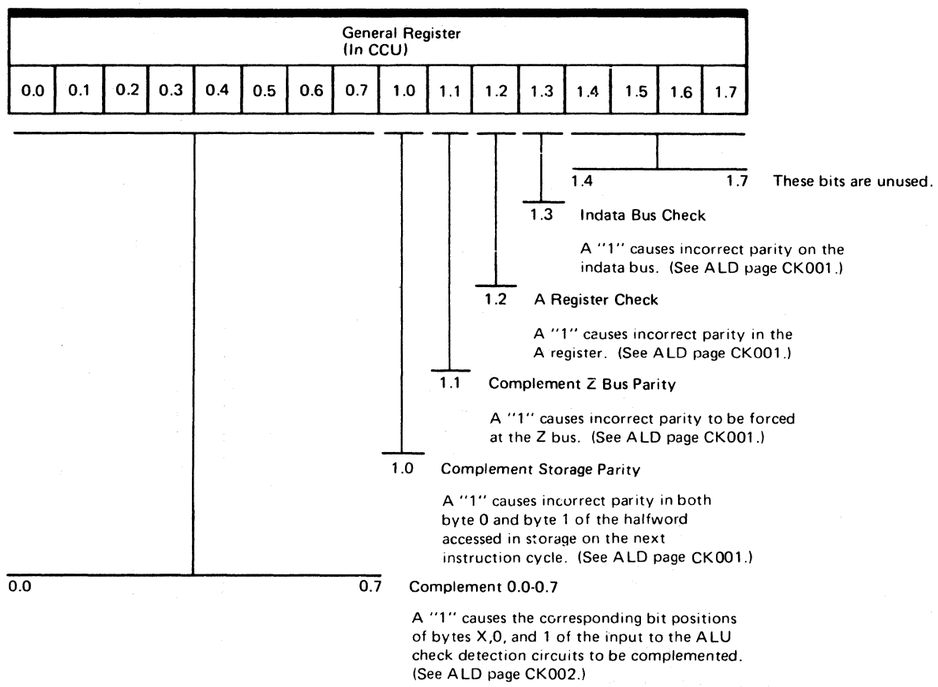
If a Remote Programmer Loader is installed on a 3705-80, the ROS bootstrap program executes an Output X'77', after the load module has been successfully transferred, that resets the 'program initiated IPL' latch (GE102) if it was set.

Output X'78' Force CC Checks

Output X'78' provides a means for testing the CC check circuits under diagnostic control by forcing checks in the CCU data flow. This output is ignored if the CCU is not in test mode.

Note: *You may have to take corrective action after using this output and store data with the correct parity in the affected register or storage location.*

General Register Bit Definitions



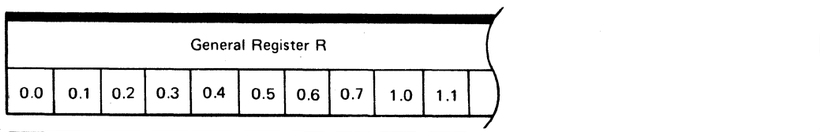
Hardware Function

At I1D time, the contents of the Z bus (contents of the general register specified by the R field) cause the functions shown on this page. Refer to the output instruction on page 6-730.

Output X'79' Utility

Output X'79' sets or resets various CCU latches.

General Register Bit Definitions



1.1 Reset Load Indicator

A "1" sets the 'load' latch that resets the LOAD light on the control panel to indicate that IPL is completed. The 'load' latch is reset and the LOAD light is turned on during IPL. (See ALD page CU006.)

1.0 Reset Check Stop Mode

A "1" resets 'ck stop mode' set during IPL phase 1 and allows the setting of 'mach ck set IPL'.
(See page 6-960 and ALD page CU006).

0.7 Program Level 5, Z Condition

If bit 0.5 of this output is "0", the 'Z condition' latch for program level 5 is set according to the state of this bit. (See ALD page CZ004.)

0.6 Program Level 5, C Condition

If bit 0.5 of this output is "0", the 'C condition' latch for program level 5 is set according to the state of this bit. (See ALD page CZ005.)

0.5 Inhibit Program Level 5, C and Z Replacement

If this bit is "0", the program level 5 'C and Z condition' latches are set according to bits 0.6 and 0.7. If this bit is "1", no action is taken (See ALD page CZ004.)

0.4 These bits are unused.

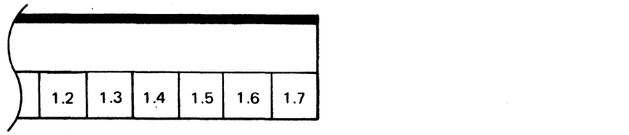
0.3 Set Storage Diagnostic Mode

A "1" sets the 'allow set memory diag reg' latch. At the next 'store new' pulse, store bits for bytes 0 and 1 are set into the FET storage diagnostic registers.

0.2 Set IPL

A "1" initiates an IPL. (See ALD page CU010.) A "1" also selects the ROS to be used as specified by output X'6B' and bit 0.4 if a Remote Program Loader is installed.

0.0 **0.1** These bits are unused.



1.7 Scope Sync Pulse 2

A "1" generates scope sync pulse 2. This is an oscilloscope synchronization pulse of 100 nsec that is used for maintenance purposes. (See ALD page CU015.)

1.6 Scope Sync Pulse 1

A "1" generates scope sync pulse 1. This is a scope synchronization pulse of 100 nsec that is used for maintenance purposes. (See ALD page CU015.)

1.5 Reset Bypass CCU Check Stop Mode

A "1" resets the bypass CCU check stop. This bit should not be on if bit 1.4 of this output is "1". It is ignored if the CCU is not in test mode. (See ALD page CU005.)

1.4 Set Bypass CCU Check Stop Mode

A "1" sets bypass CCU check stop. When this bit is set, operation is the same as if the DIAGNOSTIC CONTROL switch were in the BYPASS CCU CHECK STOP position. This bit should not be on if bit 1.5 of this output is "1". It is ignored if the CCU is not in test mode. (See ALD page CU005.)

1.3 Reset Test Mode

A "1" resets test mode. The TEST light of the control panel is turned off if the MODE SELECT and the DIAGNOSTIC CONTROL switches are in PROCESS. Any test functions allowed by test mode are also reset. This bit should not be on if bit 1.2 of this output is "1". (See ALD page CU005.)

1.2 Set Test Mode

A "1" places the CCU in test mode. This bit turns on the TEST light on the control panel and allows the following diagnostic functions to be performed:

a. Output X'78' Force CCU Checks
b. Set and reset diagnostic level 2.
c. Set and reset bypass CCU check stop.
d. Set and reset adapter level 1 interrupt request mask.

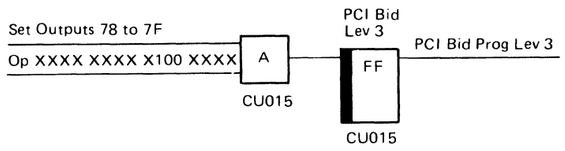
Note: *Although the emulation program does not use X'79' bit 1.0, the Network Control Program does and will re-IPL and check point restart on a machine check.*

Hardware Function

At I1D time, the contents of the Z bus (contents of the general register specified by the B register) cause the functions shown on this page. Refer to the output instruction of page 6-730.

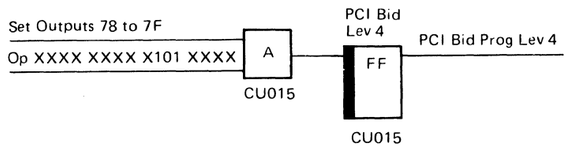
Output X'7C' Set PCI L3

Output X'7C' sets the program controlled interrupt request for level 3. Since this instruction performs a function, the bit settings of the register are ignored.



Output X'7D' Set PCI L4

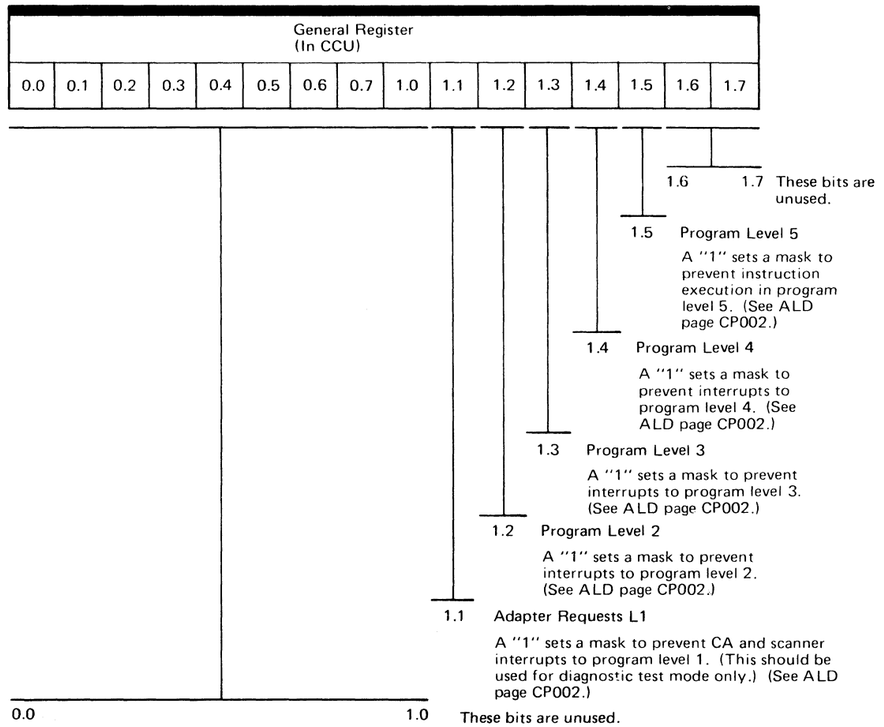
Output X'7D' sets the program controlled interrupt request for level 4. Since this instruction performs a function, the bit settings of the register are ignored.



Output X'7E' Set Mask Bits

Output X'7E' is used to set mask bits to prevent interrupts to certain program levels while processing.

General Register Bit Definitions



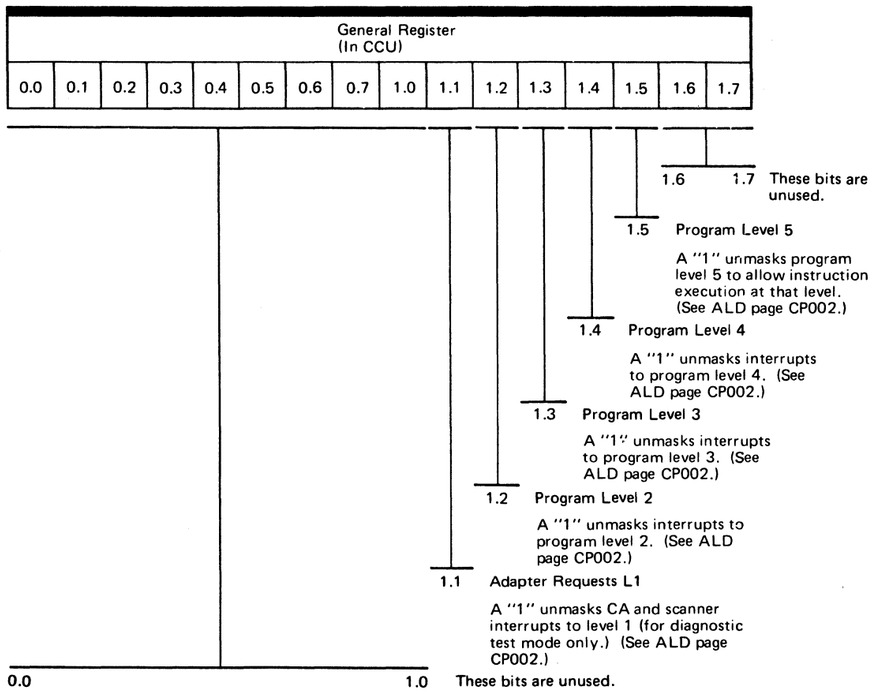
Hardware Function

At I1D time, the contents of the Z bus (contents of the general register specified by the R Field) cause the functions shown on this page. Refer to the output instruction on page 6-730.

Output X'7F' Reset Mask Bits

Output X'7F' is used to reset the mask bits for program level interrupts.

General Register Bit Definitions



Hardware Function

At I1D time, the contents of the Z bus (contents of the general register specified by the R field) cause the functions shown on this page. Refer to the output instruction on page 6-730.

IPL
(PART 1 OF 5)

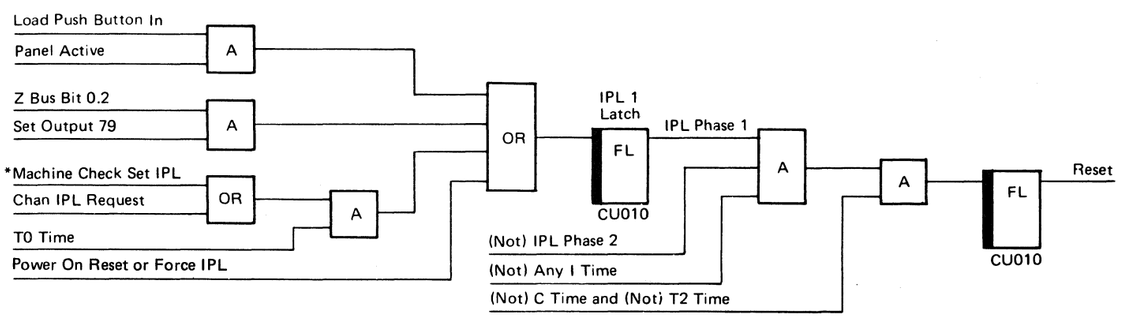
Initial program load (IPL) controls the clearing of storage and the loading of a bootstrap program into storage during a power-on reset sequence or only the loading of a bootstrap program during an IPL not caused by a power-on reset.

Initializing a power-on IPL operation causes: (1) a general reset of the IBM 3705-80, (2) a clear storage operation (the hex value represented by STORAGE DATA switches B, C, D, and E is forced into all storage locations for a period of 300 to 400 milliseconds), (3) automatic loading of a bootstrap program into storage from read only storage (ROS), and (4) passing of control to the bootstrap program. The bootstrap program (1) controls channel operations until the first load module from the host is successfully transferred into storage under a channel I/O Write IPL command or (2) controls remote-program-loader operations until the first load module from the host is successfully transferred into storage via the communication facility. After successful transfer of the first program segment into the 3705-80, the bootstrap program passes control to the loaded program segment which then controls the loading of whatever additional load modules are required to complete the 3705-80 control program load.

IPL is accomplished by successfully completing the three phases of the IPL operation.

Two lights in display B on the control panel indicate the three phases of IPL. The LOAD light on the control panel is turned on when the IPL is initiated, and is not turned off until phase three is completed, and the control program executes an Output X'79' with bit 1.1 on in the CCU general register designated by the R field.

IPL Initialization



*Refer to Output X '79' Bit 1.0 Page 6-930.

IPL Phase 1

During IPL phase 1, the LOAD light turns on, and a general reset occurs in the 3705-80. The duration of the reset depends upon the duration of the action initiating the IPL. For example, if the LOAD pushbutton is held in, the reset lasts until the pushbutton is released.

The general reset:

1. Sets mask bits for program levels 2-5 and adapter level 1 requests.
2. Resets all interrupt entered latches.
3. Resets all CCU interrupt requests.
4. Resets PROGRAM STOP and HARD STOP.
5. Discontinues instruction execution.
6. Disables storage protection.
7. Turns on the control panel TEST light.

Minimal reset occurs in the channel adapter unless the IPL is the result of a power-on-reset. The RESET switch completely resets the channel adapter and makes an IPL necessary. A complete power-on-reset occurs in the remote program loader if it is installed.

When the phase 1 reset ends, phase 2 begins.

Summary of IPL Phase 1 Resets.

Logic Page	*Card Location*	*Function*
CC004	B3Q2	Inhibit I Cycles
CL005	B3K2	Condition LS Write
CM001	B4C2	Inhibit Storage Operations
CP001	B3T4	Inhibit Allow Instructions
CP002	B3M2	Mask Interrupt Levels
CP003	B3M2	Reset Interrupt Entered Latches
CS002	B3F2	Conditions Set SDR byte X, 0, and 1 Inhibit Set Bad Addr
CS003	B3F2	Condition TAR Set
CS004	B3F2	Gate CCU Indata to Y bus Gate TAR to Y bus
CS007	B3F2	Set Op Reg
CU004	B3P2	Reset Address Compare Reset Program Stop
CU005	B3L2	Set Test Mode Reset BP Ck Stp Mode
CU007	B3P2	Reset Clock Step Reset Start, Display, Store
CU014	B3L2	Reset PCI Bid Lev 2 Reset Addr Exception Reset Allow Irpt Reset Interrupt Key
CU015	B3M2	Reset PCI Bid Lev 3 Reset PCI Bid Lev 4 Reset Svc Bid Lev 4
CV061	B4D2	Inhibit Storage Protection
CX002	B3D2	Priority Register Occupied Latches

IPL
(PART 2 OF 5)

IPL Phase 2

During IPL Phase 2, the ROS bootstrap program is automatically loaded into storage sequentially from location X'00000'. (See Notes.) The ROS array for the CA1 or CA4 is mounted on an MST card and is plugged into the socket at 01A-B4F2 (see logic page CW011 and CW012) while the Remote Program Loader II ROS array card is plugged into the socket at 01A-B4F4 (see logic page CW001).

The bootstrap program code is unique to the particular type ROS, and a listing of the code is contained in the logic pages beginning on ALD CW101.

Notes:

1. *If the IPL operation is initiated by a power-on reset (POR), a storage test pattern is forced into all storage locations for a period of 300 to 400 milliseconds. The storage test pattern equals the hexadecimal value represented by STORAGE DATA switches B, C, D, and E. When the forced storage test pattern operation ends, the CCU initiates a power-on reset which causes IPL phase 1 to occur. Following IPL phase 1, entry into IPL phase 2 occurs, and the ROS is loaded into storage.*
2. *See page 1-200 for a procedure to clock step through IPL phase 2 (see Note 3).*
3. *The forced storage test pattern that occurs during IPL phase 2 of an IPL operation initiated by POR cannot be clock stepped. To simulate a POR IPL, follow either procedure A or B.*
   - *A. With the 3705-80 power off, jumper B3C4B13 to B3C4J11. Bring up power on the 3705-80. The 3705-80 will now loop IPL phase 1 and 2. During IPL phase 2, the forced storage test pattern operation will occur. The data pattern loaded into storage equals the hexadecimal value represented by STORAGE DATA switches B, C, D, and E.*
   - *B. With the 3705-80 power on and the control panel active, jumper B3C4B13 to B3C4J11 and press "LOAD." The POR IPL operation will loop as described in Procedure A.*

Phase 2 Data Flow

Note: *This description of the IPL phase 2 data flow applies only to the loading of ROS. For information on the loading of a storage test pattern (occurs only during IPL phase 2 of an IPL operation initiated by a power-on reset), refer to CU016 (control logic) and 6-060 (storage test pattern data flow).*

At the beginning of IPL phase 2, SAR and TAR contain all 0s. Cycle steal cycles are used to load the ROS bootstrap program into storage.

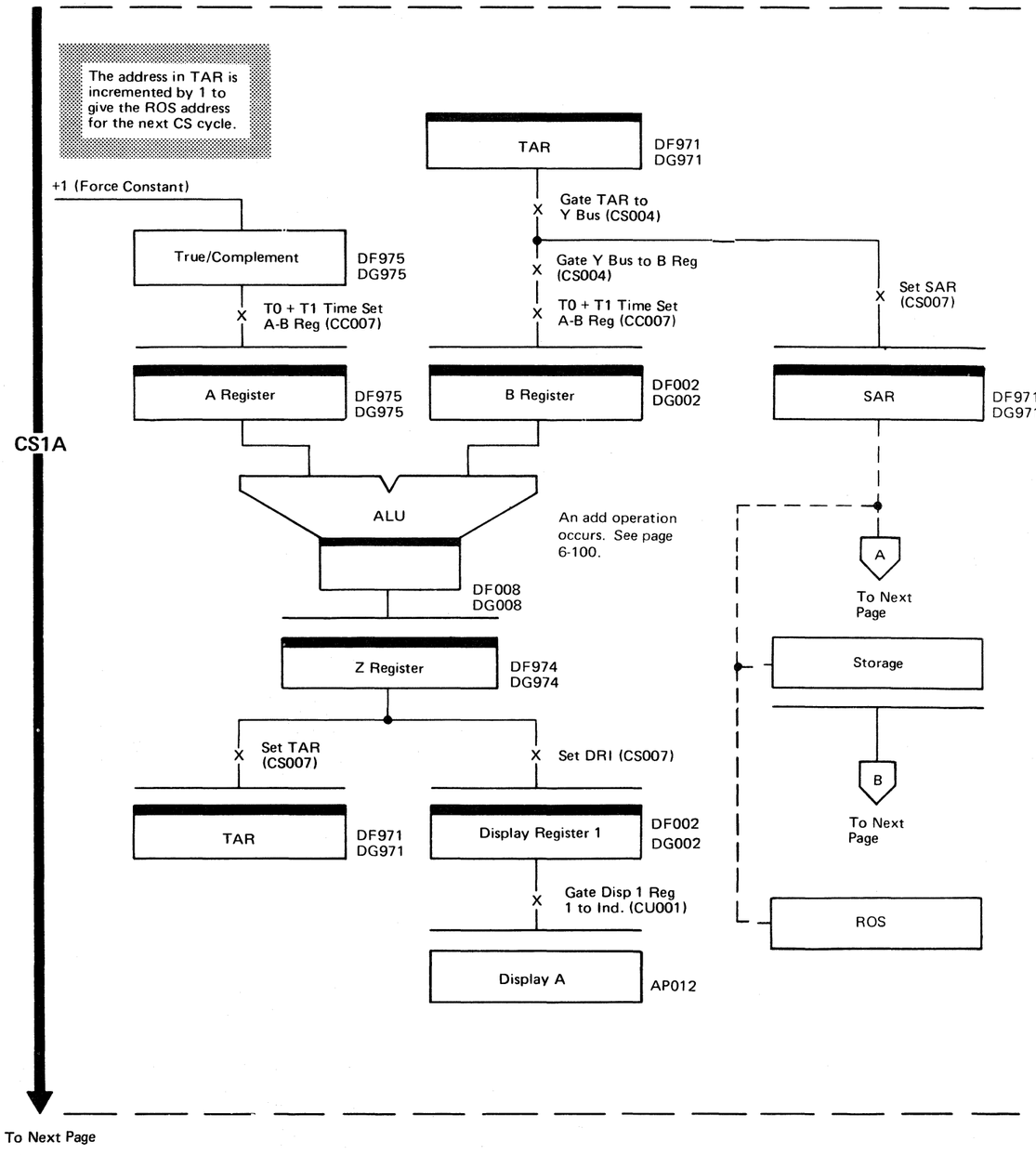
SAR addresses both storage and ROS. ROS is addressed on a byte level. During each cycle steal cycle, the ROS data is placed in byte 1 of the 'indata' bus.

The first cycle steal cycle in IPL phase 2 stores the first byte of ROS data in byte 0 of the first storage location. (A 'cross lo to hi' operation places the ROS data in both bytes 0 and 1. Because SAR bit 1.7 is 0, 'ROS byte 0' and zeros in byte 1 are gated to SDR and loaded into storage.)

The second cycle steal cycle stores the second byte of ROS data in byte 1 of the first storage location. (Because SAR bit 1.7 is 1, 'ROS byte 0, from the store read cycle, and 'ROS byte 1' are gated to SDR and loaded into storage.)

The bootstrap cycle steal operations continue until all of the ROS bootstrap program is loaded. The following data flow charts and pages 6-963 or 6-964 show the ROS bootstrap cycle steal operations.

Note: *Refer to page CW000 for a list of ROS program code, simulation run, and ROS flow charts.*



From Preceding Page

During the read portion of the storage cycle, storage sends the data from the storage location addressed by SAR to the CCU. SAR bit 1.7 determines whether byte 0 or byte 1 is gated to the SDR. The byte of ROS data in the ROS location addressed by SAR is gated to 'indata bus' byte 1. The ROS data is duplicated in both bytes of the Z register by the ALU. SAR bit 1.7 determines whether byte 0 or byte 1 is gated to SDR. The contents of SDR are then stored in the storage location addressed by SAR.

CS1B

ROS

X Gate CCU Indata to Y Bus (CS004)

X Gate Y Bus to B Reg (CS004)

X T0 + T1 Time Set A-B Reg (CC007)

Byte 1

B Register — DF002 DG002 Byte 1

ALU — DF008 DG008

A "cross lo to hi" operation occurs. See page 6-100.

From Preceding Page B

Z Register — DF974 DG974

X If SAR 1.7 = 0: Gate Byte 1 to M Bus (CS005) If SAR 1.7 = 1: Gate Byte 0 to M Bus (CS005)

X If SAR 1.7 = 0: Gate Z Bus Byte 0 to M Bus (CS005) If SAR 1.7 = 1: Gate Z Bus Byte 1 to M Bus (CS005)

X Set SDR Byte (CS007)

The byte of ROS data is only seen in Display B during a clock step operation.

X Set DR 2 (CS007)

Display Register 2 — DE003 DF003 DG003

X Gate Displ Reg 2 to ind. (CU001)

Display B — AP012

From Preceding Page A

SDR — DN001

(1)

Storage

To Next Column

CS1C

No Action

CS1D

The contents of SDR are displayed in display B.

(1)

X Gate SDR Bits to A Bus (CF003)

True/Complement — DF975 DG975

X T0 + T1 Time Set A-B Regs (CC007)

A Register — DF975 DG975

ALU — DF008 DG008

An A register direct operation occurs. See page 6-100.

Z Register — DF974 DG974

X Set DR 2 (CS007)

Display Register 2 — DE003 DF003 DG003

X Gate Displ Reg 2 to Ind. (CU001)

Display B — AP012

The CCU takes CS cycles until all of ROS is placed in storage.

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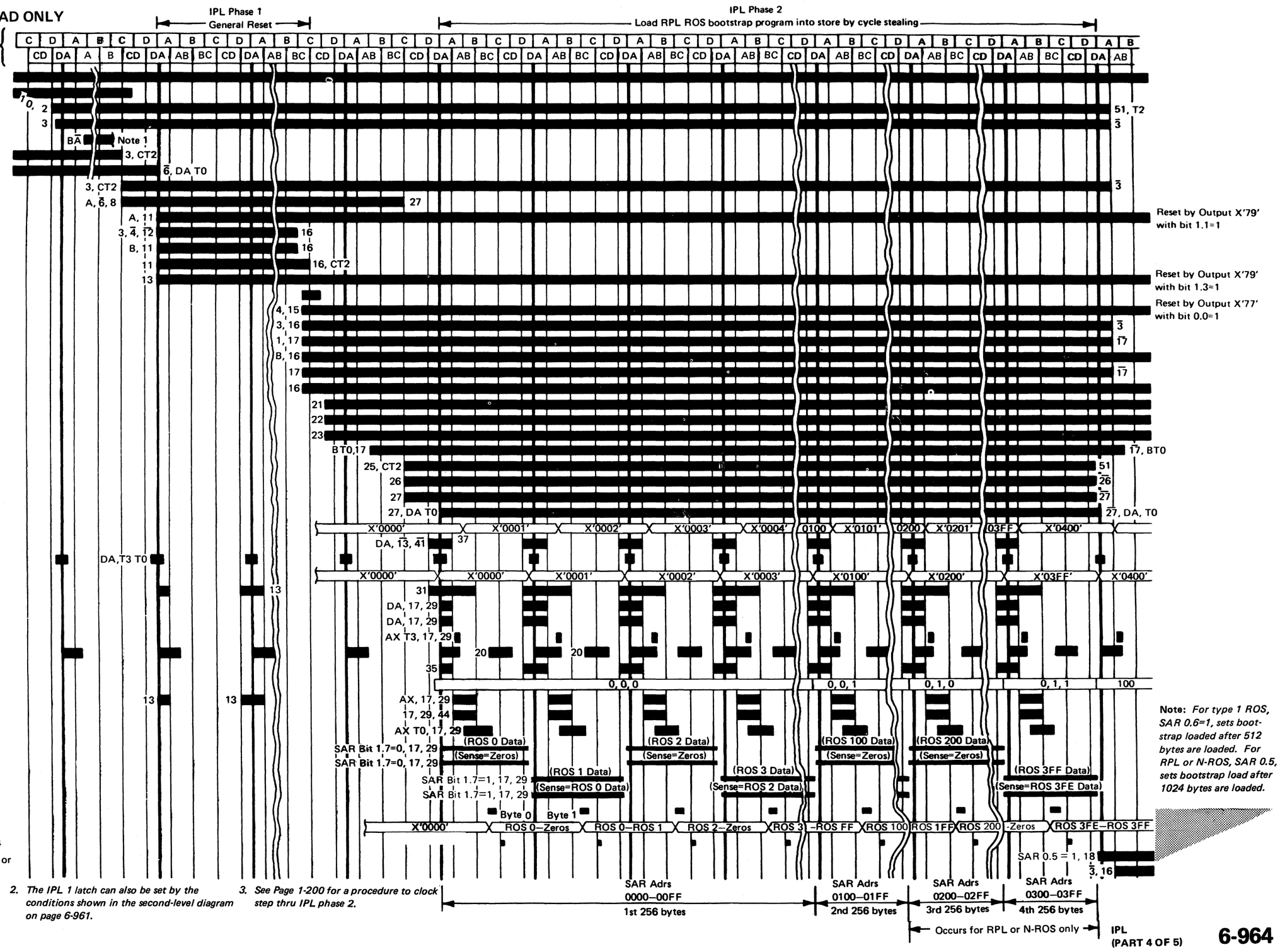
IPL PHASE 1 AND 2 TIMING — ROS LOAD ONLY

Note: *Before using this chart, refer to the IPL description on 6-960 and 6-961.*

	CCU Clock
1 - Panel Active	CU001
2 + Load Push Button In	AP007
3 IPL 1 Latch (Note 2)	CU010
4 - IPL Reset Countdown Started	CP007
5 - Set Int Timer Bid	CP007
6 + Allow Instruction	CP001
7 + Any I Time	CC008
8 + Pre-Empt All But Maint	CP001
9 + Wait to Ind	CC008
10 + Load to Ind	CU006
11 + Power On or IPL Reset	CU010
12 + IPL Phase 1 to Ind	CU010
13 + Reset	CU010
14 - Test Mode Latch (Indicator On)	CU005
15 - IPL Reset Count Down Complete	CP007
16 IPL 2 Latch	CU010
17 + Bootstrap Mode	CU010
18 -Bootstrap ROS 1	CU009
19 + IPL Phase 2 or 3 to Display B	CU010
20 - Latch Store	CQ001
21 + IPL Bid Level 1	CU010
22 - Level 1 Bid Sample	CP002
23 - Prog Level 1 Next	CP002
24 - Virgin Level	CP003
25 + Bid Maint Latch	CP001
26 + Go Maint	CP001
27 + Go CS	CC008
28 - Go First CS Cycle	CC004
29 - CS 1 Time	CC004
30 TAR	DF971
31 - Gate TAR to Y Bus	CS004
32 + Set SAR	CS007
33 SAR	
34 - Gate Y Bus to B Reg	CS004
35 + Force Constant 00001	CF002
36 + Add Bytes X, 0, and 1	CA002
37 + Set TAR	CS007
38 Read Call Wr Call Time	CC007
39 + Block Complete SDR	CF003
40 + SAR Bits 0.5, 0.6, and 0.7	DJ011
41 - Gate CCU Indata to Y Bus	CS004
42 + Select 1st to 4th 256 Bytes	CW001
43 - Cross Lo to Hi	CA003
44 - Gate Z Bus Byte 0 to M Bus	CS005
45 - Gate Byte 1 to M Bus (Sense Data)	CS005
46 - Gate Z Bus Byte 1 to M Bus	CS005
47 - Gate Byte 0 to M Bus (Sense Data)	CS005
48 + Set SDR	CS007
49 SDR	
50 - Write + Read	MM764
51 + Bootstrap Loaded	CW001 or CW011
52 + IPL Phase 3	CU010



Note: *For type 1 ROS, SAR 0.6=1, sets bootstrap loaded after 512 bytes are loaded. For RPL or N-ROS, SAR 0.5, sets bootstrap load after 1024 bytes are loaded.*

Notes:

1. *A B = Phase A and B Sample pulses; therefore these timings may vary. (See page D-570.)*
2. *The IPL 1 latch can also be set by the conditions shown in the second-level diagram on page 6-961.*
3. *See Page 1-200 for a procedure to clock step thru IPL phase 2.*

IPL (PART 4 OF 5)

IPL Phase 3

ROS bootstrap program execution begins with an interrupt to program level 1, and the program is executed entirely at this level. The instruction at storage location X'00010' is the first instruction to be executed. (The branch to storage address X'00010' is hardware forced at the start of IPL phase 3.) Refer to logic page CW000 for the listing of the ROS bootstrap program, ROS flow charts, ROS code, and simulation run.

The first section of the program:

1. Saves the general registers for group 0 starting in location X'00780'.
2. Verifies the operation of the 3705-80 instructions needed by the second part of the bootstrap program; see 2-000, 2-040.
3. Tests to determine whether to continue or branch to the ROS bootstrap escape address X'06FC'.
4. If the branch is not taken, saves external registers X'76', X'7D', and X'7E' starting at storage location X'00702'.

The TEST light turns off on the control panel after the first part of the test is complete.

The second part of the ROS bootstrap program controls channel adapter or remote program loader operations until the first program load module is successfully transferred from the host. If there is no command pending for completion or final status in the CA, the ROS bootstrap program has the CA generate an asynchronous status of Device End (DE) and Unit Check (UC). If a command other than a Write IPL is pending completion, the CA generates a final status of Device End, Unit Check, and Channel End (CE) if CE has not already been generated. In either case, Not Initialized (sense bit 6) is made available for a subsequent channel Sense command. A Write IPL normally follows the channel Sense command. See the *Remote Program Loader* Section in Volume III of this manual for a description of the remote program loader IPL.

The Write IPL command allows the transfer of the first load module from the host processor into the 3705-80. Under the Write IPL command, the load module is stored in sequential storage locations starting at location X'00400'. The maximum size of this load module cannot exceed 768 bytes. When this transfer is successfully completed, the ROS bootstrap program executes an Output X'77', with bit 0.0 on in the general register, to reset the IPL 2 latch, the IPL level 1 interrupt request, and the IPL PHASE lights. The ROS bootstrap program turns control over to the program module just loaded by branching to location X'00404'. The first two halfwords transferred in the load module must contain the IPL source identification and the total number of bytes in the load module in that order:

The IPL operation is complete when the IPL level 1 interrupt request is reset and the IPL PHASE lights turn off. However, the LOAD and TEST lights remain on until an Output X'79' resets them with bits 1.1 and 1.3 on respectively in the general register. When the 3705-80 is completely loaded, the loaded program should execute this instruction.

The IPL completion point in the ROS bootstrap program may not be reached because of one of the following:

1. A CC check hardstop
2. Improper instruction test operation
3. Program continuity check
4. Channel adapter disabled
5. Channel adapter malfunction
6. IPL count transfer check

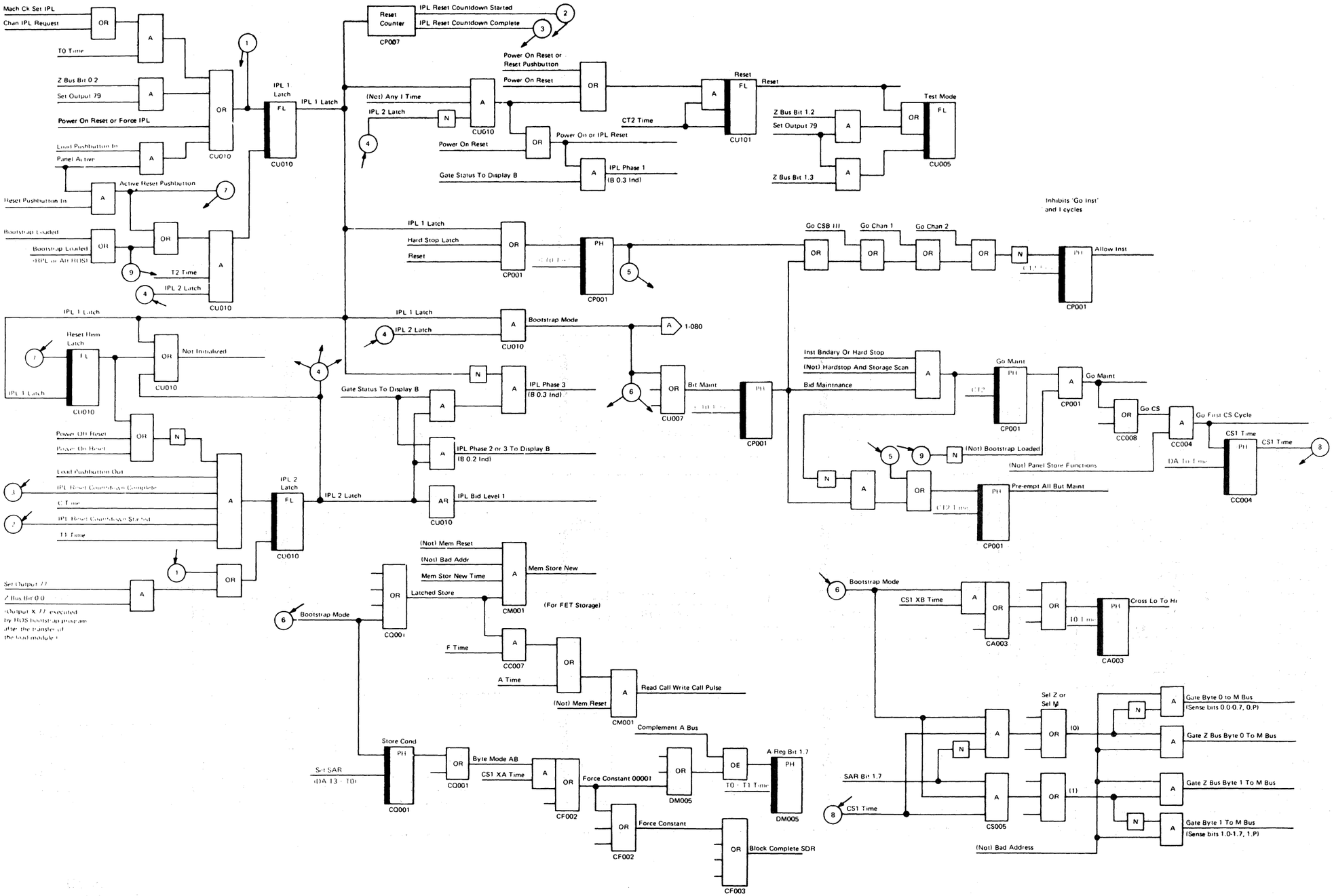
In this case, the ROS bootstrap program either hard-stops or loops and executes a program display function to try to identify the IPL status. See *ROS Testing*, 2-000 and 2-040.

IPL Phase 3 with Type 1 or Type 4 Channel Adapter

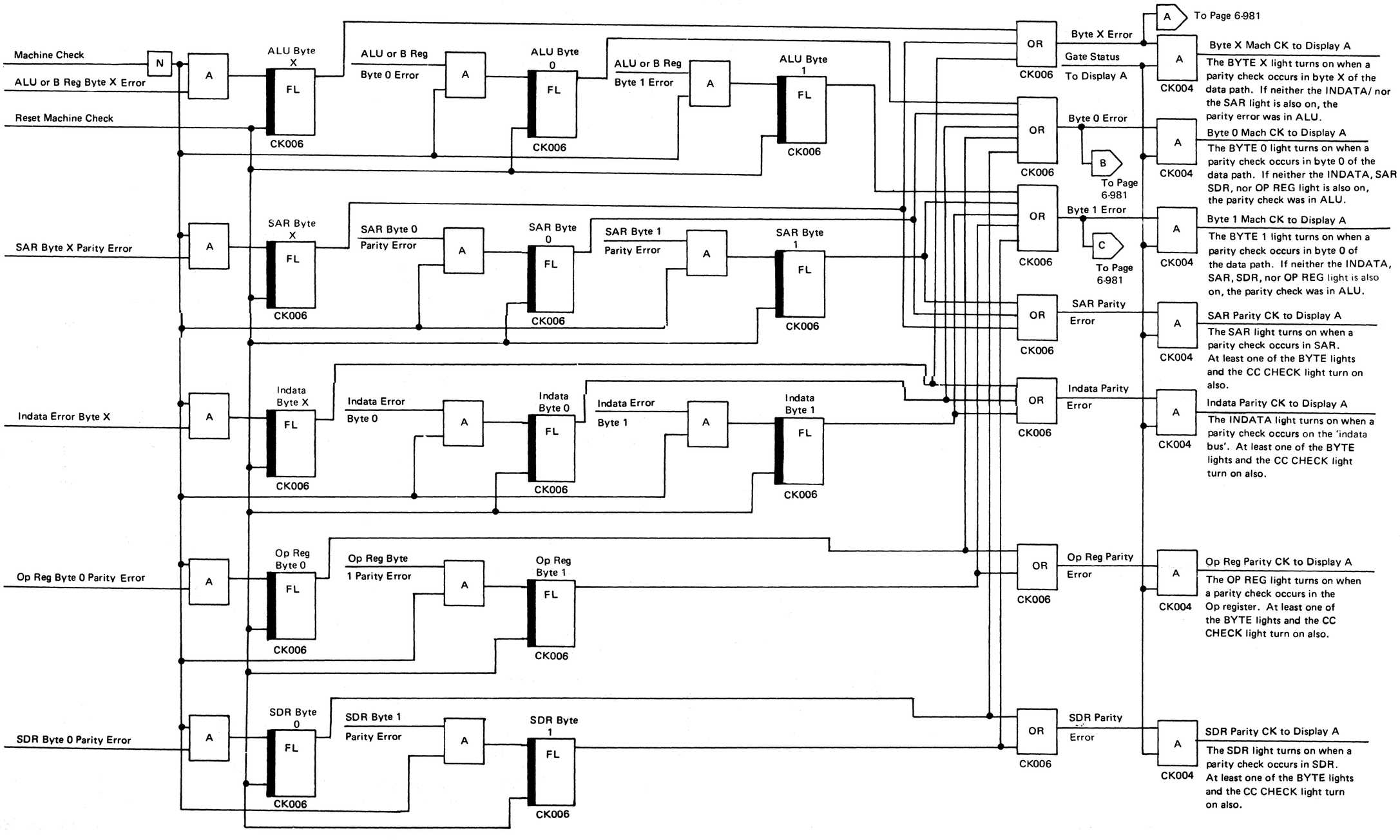
Unless the IPL sequence is started by a power on sequence, the state of the type 1 CA is not affected by the reset performed in IPL phase 1. Therefore, the ROS bootstrap program must handle the following conditions:

1. Channel Interface disabled. The bootstrap program executes Output X'67' with bit 1.4 on in the CCU general register to allow the interface to become enabled. The program loops until the interface becomes enabled.
2. Channel interface enabled. The bootstrap program tests to determine whether or not the native subchannel (NSC) is active with a channel command. Then one of the following actions occurs:
   a. If no command is in progress, the bootstrap program signals the type 1 or type 4 CA to send DE, UC status. When this status transfer is complete, the CA program loops, waiting for an initial selection level 3 interrupt request. When the interrupt request is detected, the bootstrap program responds as described in the type 1 or type 4 channel adapter section of this manual; see 8-140.
   b. If a command is in progress, the bootstrap program signals the CA to end the command with CE, DE, UC status. When this status is successfully transferred, the bootstrap program loops waiting for a type 1 CA initial selection level 3 interrupt request. The bootstrap program responds to the interrupt request as described in the type 1 channel adapter section of this manual; see 8-140.

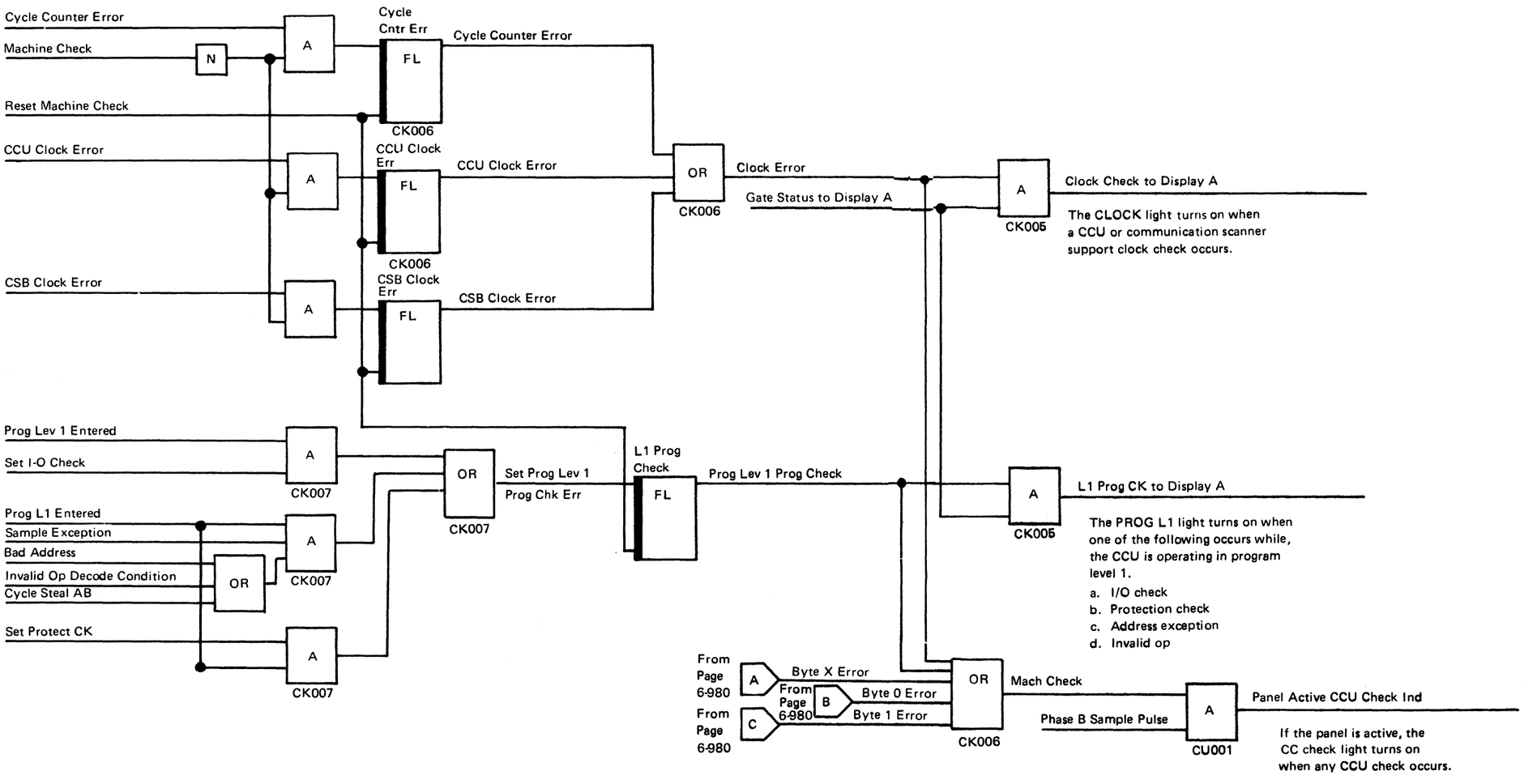
IPL DATA FLOW



ERROR CHECKING
(PART 1 OF 2)



ERROR CHECKING (PART 2 OF 2)



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3705-80 STORAGE MAINTENANCE

STORAGE MAINTENANCE OVERVIEW

Storage Array Cards

3705-80 storage has single-bit error correction. Therefore, array cards with single-bit errors are not replaced. When two errors occur at any address, a double-bit error is detected. An array card with a double-bit error should be replaced. All 3705-80 models contain two storage array cards. Each card contains 128K bytes.

Storage Support Cards

When a failure occurs on one of the 6 storage support cards in a 3705-80, the diagnostic indicators on gate 01B can be used to aid in isolating the failure. Failures that cause a loss of timing signals (such as card select timing or write pulses) may be isolated by card substitution or by the use of an oscilloscope.

Intermittent Problems

Intermittent failure of storage array cards should be a rare occurrance. If the IFTs do not indicate a storage problem but other indications (such as a machine check auto-IPL or hard-stop with SDR or Op Reg CC checks) point to an intermittent problem, the following procedure should be used.

1. Determine the failing address using the maintenance procedure on Page 7-260. If this procedure does not point to the failing address, use the procedure on Page 7-290.
2. Try swapping the array cards, 01A-B2T2 and 01A-B2U2, to isolate the problem.

Intermittent problems are more likely to be caused by failures in the MST support logic.

STORAGE PHYSICAL LOCATIONS

All 3705-80 storage is located in gate 01A-B2. The storage cycle time is one microsecond for all models. A read operation is performed every "A" cycle—even when in a stopped condition. Write operations are performed only when the CCU requires a store operation. The storage controls include automatic single-bit error correction and double-bit error detection. When a double-bit error is detected, the uncorrected bits are sent to the CCU and the parity bits for both bytes are inverted to force parity errors in the CCU. Data bits are not altered when a double-bit error is detected.

The IFTs are the primary means of servicing storage. Diagnostic indicators are located on the pin side of the 01A-B2 storage board (A5 position) to assist you in isolating troubles when the IFTs cannot be loaded, or the trouble cannot be found using the IFTs.

The storage requires two special voltages, +5V and -5V, in addition to the +12V supply used throughout the 3705-80.

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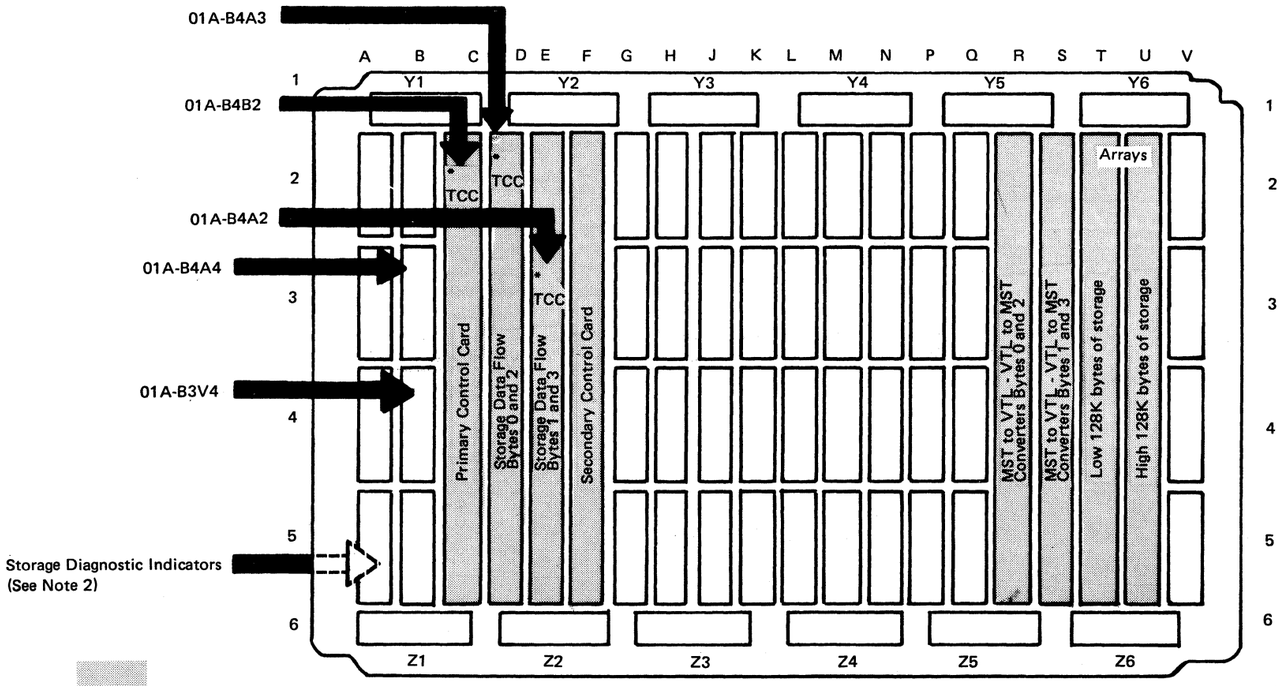
STORAGE BOARD LAYOUT (01A-B2)

CARD LOCATION	ALD PAGE	FUNCTION
01A-B2A5	MM465	LEDs on pin side of storage board
01A-B2B3	MM151	Control cable connection
01A-B2B4	MM151	Control cable connection
01A-B2C2	MM451	SAR connector
	MM452	Refresh address/SAR address
	MM453	Delay line clock and storage control
	MM454	Refresh control
	MM455	Miscellaneous controls
	MM456	Data and diagnostic register controls
01A-B2D2	MM351	Store/Sense TCC byte 0
	MM352	ECC bit correction for bytes 0 and 2
	MM353	Byte 0 terminator
	MM354	Diagnostic register bytes 0 and 2
	MM355	Data and corrected byte 2
	MM356	Data and corrected byte 0
	MM357	ECC check and syndrome generator
	MM358	CCU parity generator for bytes 0 and 2
	MM359	CCU sense byte 0
	MM360	Data to storage byte 2
	MM361	Data to storage byte 0
01A-B2E2	MM371	Store/Sense TCC byte 1
	MM372	ECC bit correction for bytes 1 and 3
	MM373	Byte 1 terminator
	MM374	Diagnostic register bytes 1 and 3
	MM375	Data and corrected byte 3
	MM376	Data and corrected byte 1
	MM377	ECC check and syndrome generator
	MM378	CCU parity generator for bytes 1 and 3
	MM379	CCU sense byte 1
	MM380	Data to storage byte 3
	MM381	Data to storage byte 1
01A-B2F2	MM461	ECC byte and bit error decode
	MM462	ECC correctable error decode
	MM463	Check registers
	MM464	LED drivers for errors
01A-B2R2	MM751	Storage bus driver/receiver converters for byte 0
	MM752	Storage bus driver/receiver converters for bits C1 through C4
	MM753	Storage bus driver/receiver converters for byte 1
	MM754	Converted addresses and special bits to storage
01A-B2S2	MM761	Storage bus driver/receiver converters for byte 2
	MM762	Storage bus driver/receiver converters for bits C5 through C8
	MM763	Storage bus driver/receiver converters for byte 3
	MM764	Converted addresses and special bits to storage
01A-B2T2	MM651	Low 128K bytes of storage
01A-B2U2	MM652	High 128K bytes of storage

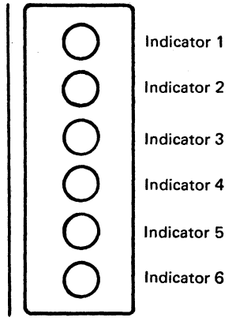
Notes:

1. *See ALD Page MM021 for voltage cable connections to pin side of 01A-B2 board.*
2. *See ALD Page MM465 for storage LED indicators that are located on the pin side of 01A-B2 board A5 position . See also page 7-260 for a description of the LED indicators.*

01A-B2 BOARD (CARD SIDE)



Indicates Card Location

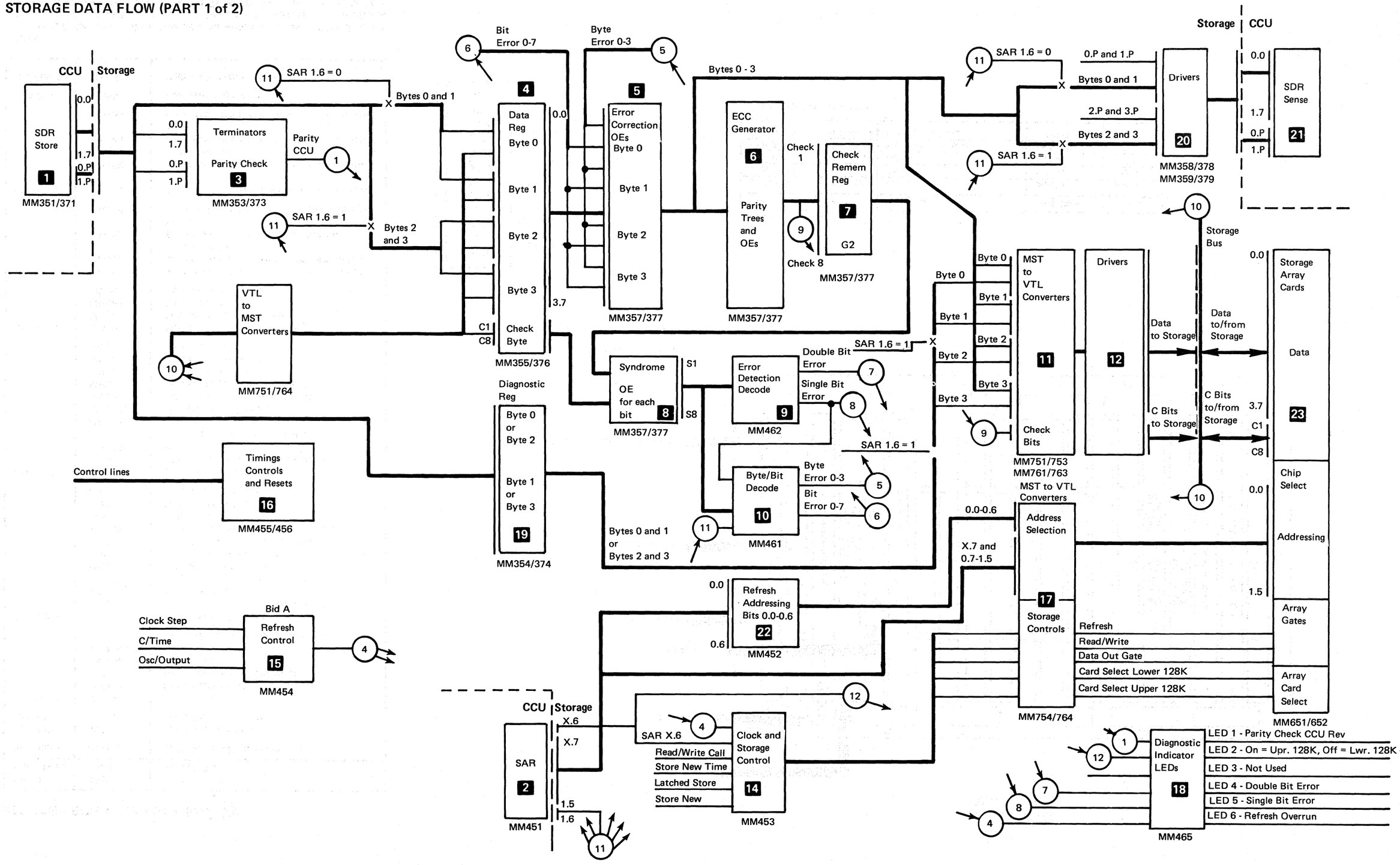


Logic Cable Plug Chart (See Note 1)

From	To	Function	ALD Page	Plugs Into
01A-B2B3	01A-B4A4	Control	MM151	Board
01A-B2B4	01A-B3V4	Control*	MM151	Board
01A-B2C2	01A-B4B2	Address	MM451	TCC*
01A-B2D2	01A-B4A3	Store/Sense byte 0	MM351	TCC*
01A-B2E3	01A-B4A2	Store/Sense byte 1	MM371	TCC*

*Top Card Connector (TCC)

STORAGE DATA FLOW (PART 1 of 2)



STORAGE DATA FLOW (PART 2 of 2)

- Storage is initialized with valid data during power-on reset
- Storage array interface is 40 bits wide-full word (32 data bits plus 8 check bits) 11 and 13
- Storage-to-CCU interface is 18 bits wide-½ word (16 data bits plus 2 parity bits) 1 and 21
- Dynamic storage logic requires refresh cycles (every 8 us during normal operation) to maintain validity of stored information.
- Storage refresh cycles occur every 4 us during initialization to assure valid data
- Single bit storage errors are correctable. Double bit storage errors are uncorrectable

Introduction

The CCU has a basic machine cycle and storage cycle of 1 us. During the first 500 ns of a storage cycle, the CCU reads from storage. During the second 500 ns of a storage cycle, the CCU writes to storage if required. If a write storage operation is not required, a refresh storage operation can occur during the second 500 ns.

Addressing

2 SAR bit X.6 selects the appropriate array card (lower 128K or upper 128K). 14 and 17 SAR bit 1.6 gates the appropriate storage bytes (bytes 0 and 1 or bytes 2 and 3) to the CCU 20 or from the CCU. 4 and 11 SAR bit 1.6 also gates the appropriate correction bits. 10 and 5

22 Storage address bits 0.0 - 0.6 are refresh address bits. The refresh addresses are updated by a ring counter. During a storage refresh cycle, the refresh address bits
17 are gated to the address selection converters, instead of SAR bits 0.0 through 0.6. SAR bits X.7 and 0.7 - 1.5 are gated to the address selection converters on all storage cycles. During refresh storage cycles, both storage array cards are accessed.

Data Register

4 The data register is the holding register for the up/down funneling effect between the halfword CCU interface and the fullword storage array interface.

During a read operation, the data register holds the four data bytes and one check byte that are read from storage. 13 Depending on SAR bit 1.6, the appropriate two bytes with parity are then gated to the CCU. 20 and 21

During a write operation, the appropriate two bytes from the CCU are gated to the data register depending on the setting of SAR bit 1.6. The other two bytes are already in the data register from the read operation in the first half of the storage cycle. (The two "new" bytes from the CCU overlay whatever was read from storage.) During the last half of the storage cycle, the two "new" bytes plus the two other bytes are written to storage.

Read Operation

A read operation occurs during the first 500 ns of any I time or operator panel cycle steal time. The array contents 23 (data bits 0.0 -3.7 and check bits C1 - C8) are gated into the data register. 13 and 4

5 The Error Correction OEs (exclusice ORs) are used to reverse the setting of a bit for a single bit, correctable error. These Error Correction OEs are deactivated until after (1) an ECC (Error Correction Code, check bits 1-8) has been generated 6 on the bits just read from storage, and (2) the newly generated check bits have been saved in the check remember register. 7 After the check bits are saved, the error detection logic 8 , 9 , and 10 determines if an error has occurred and if the error is correctable or not. Single bit errors are correctable 5 double bit errors are not correctable.

6 The ECC (Error Correction Code) generator logic generates eight check bits as shown in the following chart. The X's indicate the bits that are exclusive ORed together to determine whether a check bit should be turned on. For example, C2 = 1 whenever an even number of data bits in its associated group (byte 1, bits 0 -7 and byte 2, bits 0 - 7) are 1s.

Byte								Byte 1								Byte 2								Byte 3								Check Bits							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X																	X							
								X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X										X						
																X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X			X					
X	X	X	X	X	X	X	X																	X	X	X	X	X	X	X	X				X				
X				X	X	X		X				X	X	X		X				X	X	X		X				X	X	X						X			
	X			X	X		X		X			X	X		X		X			X	X		X		X			X	X		X						X		
		X		X		X	X			X		X		X	X			X		X		X	X			X		X		X	X						X	
			X		X	X	X				X		X	X	X				X		X	X	X				X		X	X	X		,					X

The ECC generator also generates check bits for a write operation.

7 The check remember register saves the generated check bits 1 - 8 from the data just read before it is corrected.

8 The syndromes (S1 - S8) are the result of an exclusive OR of the just generated check bits with those read from storage.

9 The error correction decode logic examines the syndromes (S1 - S8) to determine if an error occurred and whether it is correctable (single bit error, no failure) or not correctable (double bit error, failure).

10 Assuming a correctable error, the byte/bit decode logic examines the syndromes (S1 -S8) to determine which bit (0-7) in which byte (0-3) needs correction.

Read, Modify, Write Operation

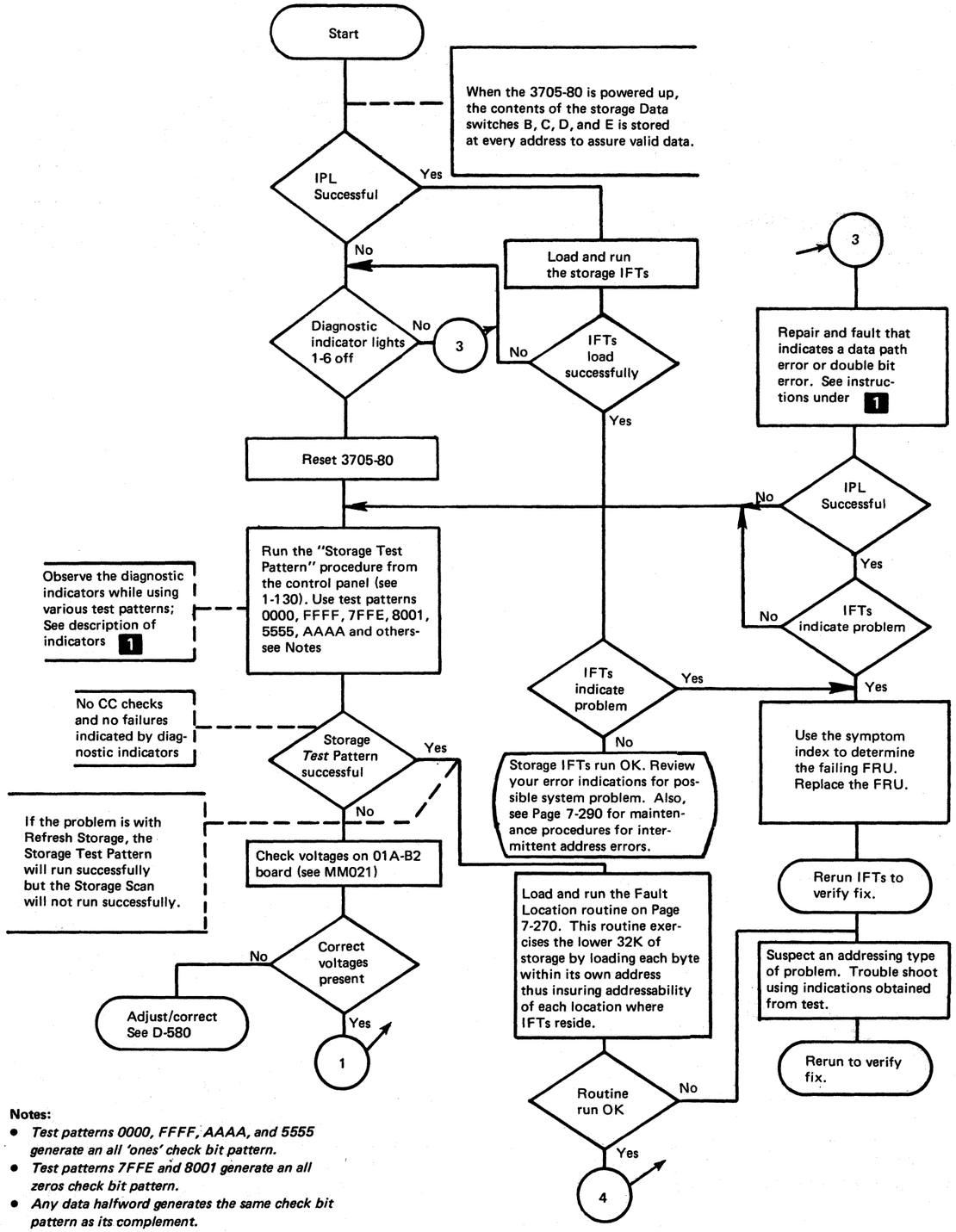
During the second 500 ns of a write storage cycle, the appropriate two bytes (0 and 1 or 2 and 3) from the CCU are gated into the data register 4 depending on the setting of SAR bit 1.6. The other two bytes are already in the data register from the read operation in the first half of the cycle, and have been corrected through the error correction OEs. 5 The ECC generator 6 generates the check bits (1 - 8). The data and check bits are then gated through the MST to VTL converters 11 and the VTL drivers 12 to the storage array.

19 The diagnostic register is used by the diagnostic IFTs to validate the storage and error detection/error correction circuitry and to gather statistics on storage errors. When the diagnostic register is reset (all zeroes), the storage data passes through the exclusive ORs unchanged. When a bit in the diagnostic register is set to a 1, it alters the storage bit until the diagnostic register is reset.

Refresh Storage Operation

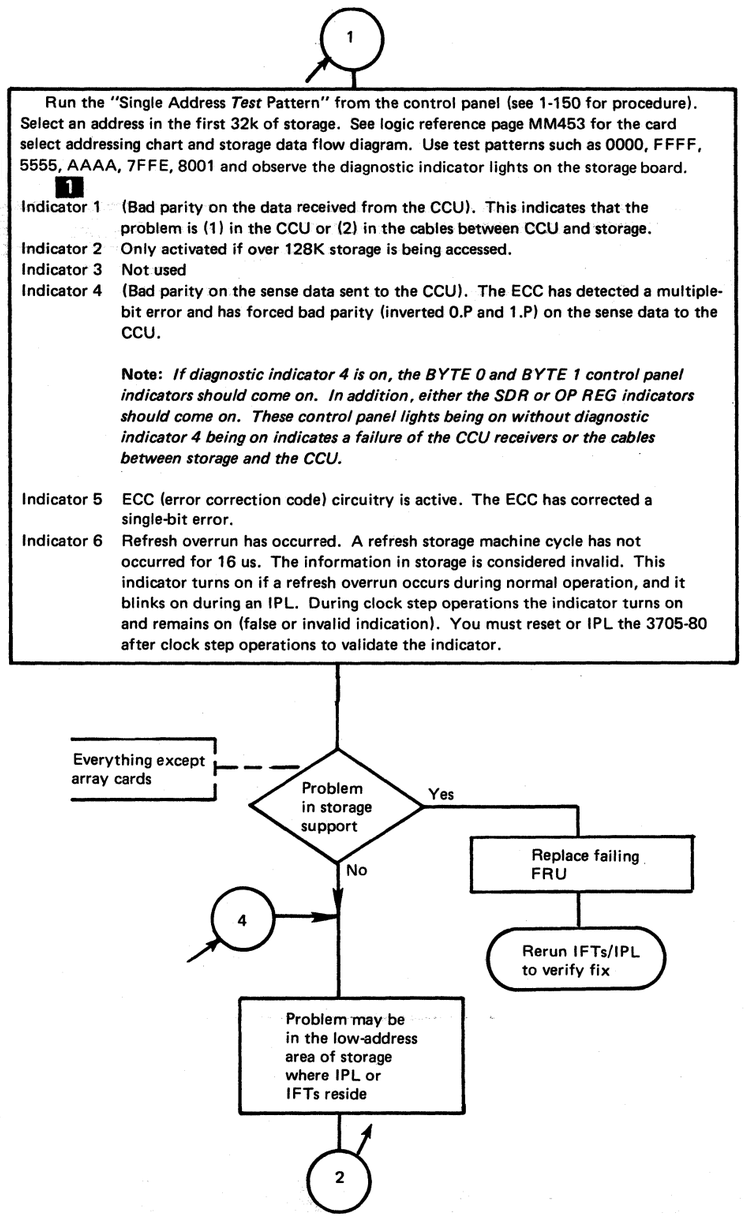
The storage unit in the 3705-80 is dynamic, meaning that the stored information must be renewed or refreshed periodically to maintain its validity. If a write operation is not required, a refresh storage operation can occur during the second 500 ns of a storage cycle. During a power-on IPL, refresh storage cycles occur approximately every four microseconds to assure that storage is initialized with valid data. During normal operation, refresh cycles occur approximately every eight microseconds.

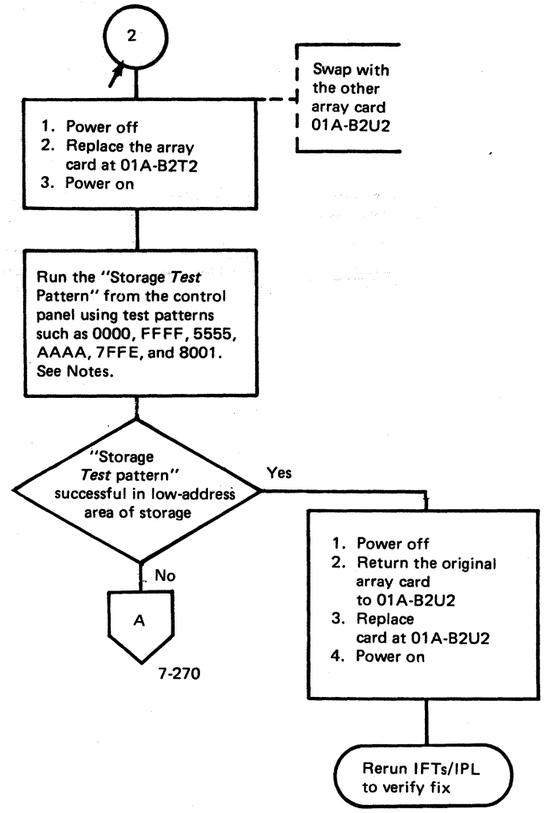
If a refresh storage cycle has not occurred for 16 us, a refresh overrun failure occurs 18 and the information in storage is considered invalid.



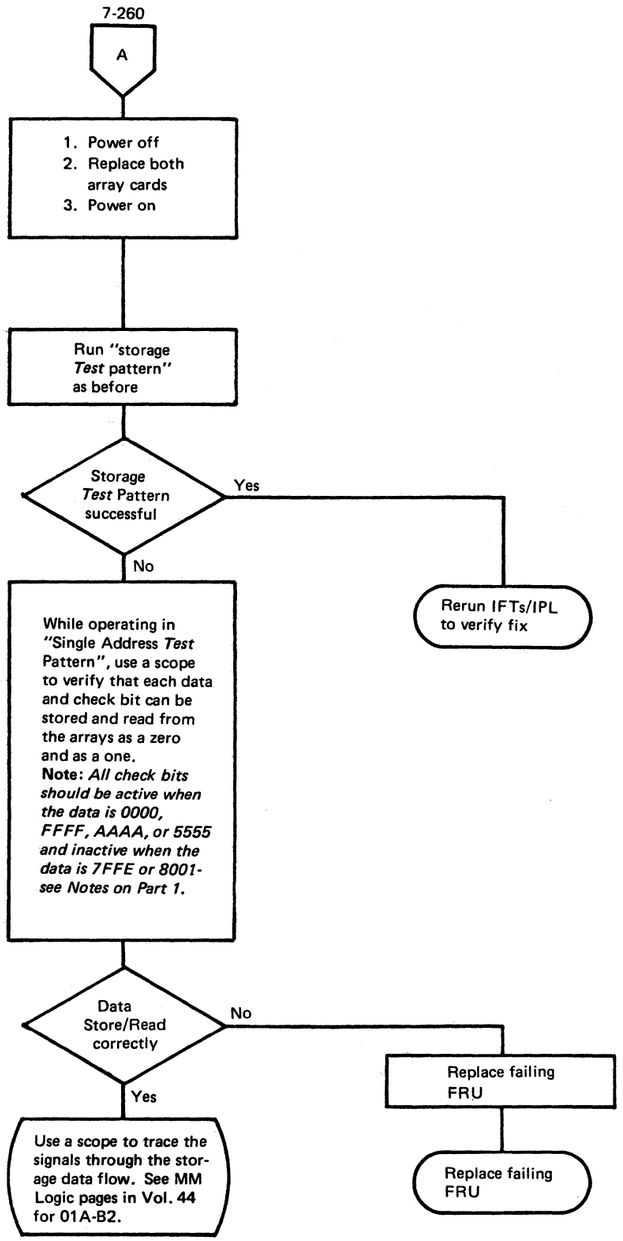
Notes:

- *Test patterns 0000, FFFF, AAAA, and 5555 generate an all 'ones' check bit pattern.*
- *Test patterns 7FFE and 8001 generate an all zeros check bit pattern.*
- *Any data halfword generates the same check bit pattern as its complement.*
- *See ALD pages MM651 and M652*





STORAGE MAINTENANCE PROCEDURE (PART 2 of 2)



Fault Location

The storage diagnostics should be run to establish a failing pattern, if it is not already evident from the reported problem. If the failure is in the first storage locations on the low 128K array card, it may prevent loading and/or executing the storage diagnostics. Manually storing and displaying, or scanning storage may establish the failure pattern. The following procedure may also be used to check low storage.

- Set the MODE SELECT switch to INSTRUCTION STEP.
- Press the RESET then LOAD pushbuttons.
- Store the following program:

Address	*Data*	*Instruction*	
00000	3188	LR	1,3
00002	1181	STH	1, 0 (1)
00004	9102	ARI	1 (1), 2
00006	21B8	CR	1, 2
00008	8802	BZL	X'0000C'
0000A	A80B	B	X'00002'
0000C	A102	SRI	1 (1), 2
0000E	1501	LH	5, 0 (1)
00010	15B0	CHR	5, 1
00012	8806	BZL	X'0001A'
00014	7114	OUT	1, X'71'
00016	7524	OUT	5, X'72'
00018	7004	OUT	0, X'70'
0001A	A102	SRI	1 (1), 2
0001C	13B8	CR	3, 1
0001E	8821	BZL	X'00000'
00020	A815	B	X'0000E'

- Check that storage where program is loaded is functioning correctly by displaying and checking program just loaded.
- Store X'00022' in register X'03'.
- Store X'08000' in register X'02'.
- Store X'00000' in register X'00'.
- Set the MODE SELECT switch to PROCESS.
- Press the START pushbutton.
- The program loads each halfword with its address as data and checks that the proper value is stored. If an error occurs the program will hardstop.
- Set the DISPLAY/FUNCTION SELECT switch to a position other than STATUS or TAR and OP REGISTER.
  DISPLAY A = Address
  DISPLAY B = Data
- Pressing the START pushbutton causes the program to loop until the next failure.
- Continue until a failing pattern is established.

Most problems are associated with component failures such as cards or loose connectors.

WARNING

Turn the power off before removing storage cards for swapping or replacing.

Swappable Storage Cards

The following pairs of cards can be swapped:

01A-B2D2 and B2E2
01A-B2R2 and B2S2
01A-B2T2 and B2U2

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MAINTENANCE PROCEDURE – INTERMITTENT STORAGE ADDRESS ERRORS

Use this procedure to trap the failing storage address if the storage diagnostics and maintenance procedures do not indicate a problem. This procedure should isolate the failing storage address to a 32K increment of storage in the upper or lower 128K bytes of 3705-80 storage.

1. Set the DIAGNOSTIC CONTROL switch to CC CHECK HARDSTOP.
2. Load the EP or NCP and then start the normal operation.
3. If a storage error occures, the 3705-80 will hardstop from a CC check with the OP REG or SDR check light on.
4. If the SDR check light is on, go to step 7.
5. If the OP REG check light is on, the failing storage address is four less than the contents of TAR.
6. If the OP REG contains a "Load Address" or "Branch and Link" instruction, the failing storage address is two less than the contents of TAR. See Page 6-150 for in instruction decoding.
7. The failing instruction will be displayed in the OP REG and should be an ICT, STCT, IC, STC, LH, L, ST, or STH instruction. See Page 6-150 for instruction decoding.
8. If the B field of the instruction (byte 0, bits 1, 2, and 3 of the OP REG) is 000, the failing storage address is in the first 32K increment of the lower 128K bytes of storage. If the B field of the instruction (byte 0, bits 1, 2, and 3 of the OP REG) is 100, the failing storage address is in the first 32K increment of the upper 128K bytes of storage.
9. Record the displacement field from the failing instruction displayed in the OP REG.
10. Determine the current program interrupt level by observing the ENTERRED INTERRUPT LEVEL lights while the DISPLAY/FUNCTION switch is in the STATUS position. If no PROG LEV lights are on, level 5 is the current program level.
11. Use the B field of the instruction (byte 0, bits 1, 2, and 3 of the OP REG) and the current interrupt level to determine, from the following chart, the register address to be used to display the contents of Base Register.
12. The failing storage address is obtained by adding (hex) the displacement field (from step 9) to the base number (from step 11). For the ICT and STCT instrucitons, the failing storage address is one less than the calculated value. For the L instruction, the address may be two more than the calculated value.

Note: *If the R or R, N field specifies the same register as the B field, this procedure will not work.*

Register Address to Display Base Number

	Current Interrupt Level				
B Field	**1**	**2**	**3**	**4**	**5**
001	01	01	09	11	19
010	02	02	0A	12	1A
011	03	03	0B	13	1B
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