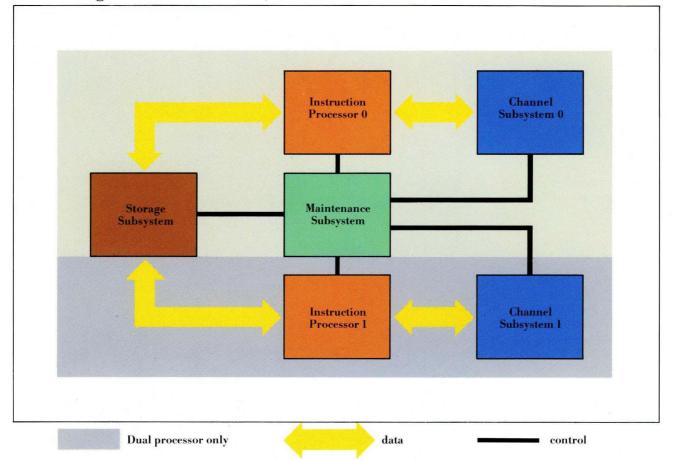# 4381 Processors

IBM

4381 Design

Dual processor only — data — control

IBM 4381 Processor Family
Model Groups 11, 12, 13 and 14

The expanded family of IBM 4381 processors is a versatile range of intermediate processors providing users with up to a five-fold growth path of increasing performance.

The 4381 MG 11, MG 12 and MG 13 are uniprocessors, while the MG 14 is a dual processor consisting of two integrated instruction processors operating under a single control program.

Enhanced logic technology provides sub-nanosecond switching time. This and additional channel functions allow significant performance improvements.

Areas of Use
The performance range and comprehensive features of the 4381 family enable these processors to satisfy a wide variety of computing needs. While highly satisfactory for an extensive range of commercial applications, the 4381 processors are also leaders in compute-intensive jobs involving long and extended precision floating point calculations for many engineering and scientific applications.

Central Site Options
- As growth options from smaller 4300 and 303X or equivalent processors
- As loosely coupled processors to 308X and 3090 installations
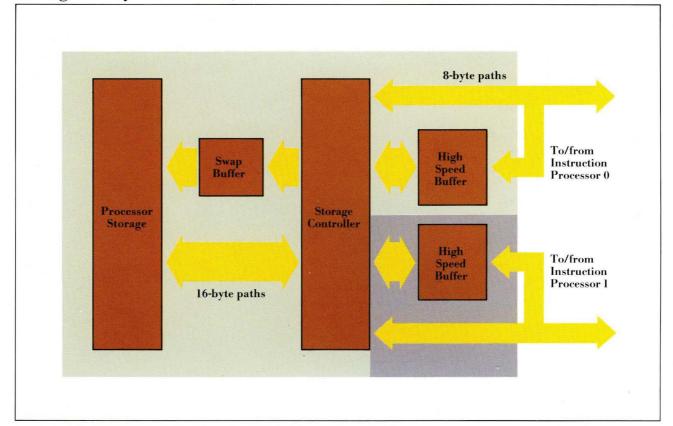- As S/370-XA migration, test or production vehicles

End User Site Options
- As department processors
- As engineering and scientific laboratory processors
- As processors in super-mini environments

All Environments
- As application processors for:
  • Information Centers
  • DP and business professionals
  • Special applications

Storage Subsystem

Two Level Storage Subsystem
- High speed buffer
  - Uniprocessor 4 K to 64 K byte
  - Dual processor 2 x 64 K byte
  - Buffer cycle time matches instruction processor cycle time
  - Store-in buffer design reduces storage accesses
  - Uniprocessors handle 2 Kb (for storage sizes up to 16 Mb) or 4 Kb virtual pages, with automatic switching between 2 Kb and 4 Kb modes under microcode control
  - Dual processor handles 4 Kb virtual pages only
  - Swap buffer writes back modified high speed buffer blocks to storage during high speed buffer reload
- Processor storage
  - Uniprocessors 4 to 32 megabytes
  - Dual processor 16 to 32 megabytes
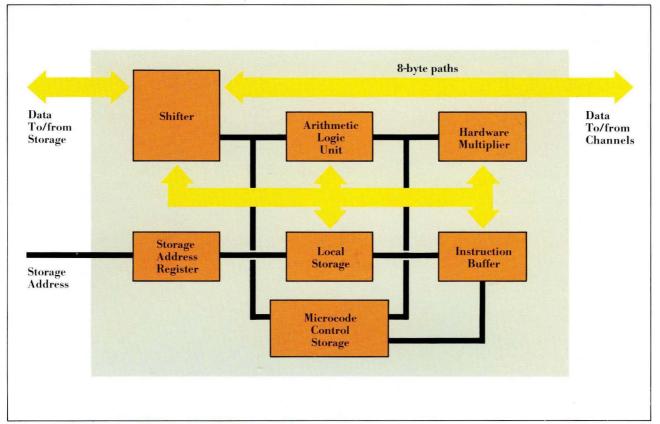- 16-byte-wide data paths within storage subsystem

Storage Controller
- Controls data flow to processor storage and swap buffer
- Performs error checking and correction

Designed for High Availability
- Single bit error correction
- Detection of all double bit errors and correction if one is intermittent via microcode.
- Automatic reconfiguration of buffers and buffer directory under microcode control.

Instruction Processor

High Performance Instruction Processor (s)
- 56/68 nanosecond cycle time
- 8-byte-wide data paths for internal storage and channel interfaces
- 8-bit-wide arithmetic logic unit and shifter
- 18-byte instruction prefetch buffer
- 2 K-byte local storage for registers and control information
- High capacity control storage for fully resident operating microcode
- 56-byte-wide hardware multiplier (except MG 1l)
- Dual processor:
  - Identical design for each processor
  - Operate using a single copy of MVS or VM in shared processor storage

Microcode-Driven
- Full S/370 user instruction set for commercial and scientific processing
- Basic microcode for S/370 and XA modes
- Extended Control Program Support (ECPS) in S/370 mode for VM and MVS including Preferred Machine Assist (PMA)
- PMA microcode enables MVS to run at almost native speed under VM
- ECPS: VM includes enhancements to improve VM/SP performance when using High Performance Option
- SORT Assist enhances DF SORT (Data Facility Sort) performance under MVS/XA
- SIE Assist (Start Interpretive Execution) improves throughput for preferred guest I/O operations under VM/XA System Facility
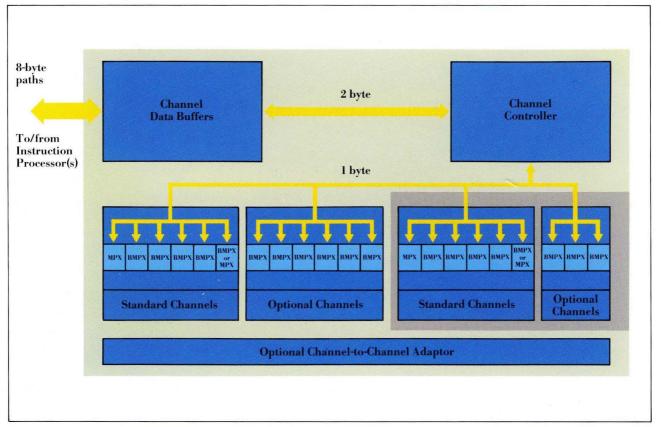- HPO Assist improves performance in S/370 mode for VM/SP High Performance Option

Features for Enhanced Scientific Computing Performance
- High-speed Hardware Multiplier (except MG 1l)
- Mathematical Assists, which reduce processor busy time by up to 65% for the assisted functions
  - Multiply and Add Facility - all models
  - Square Root Facility - all models
  - Mathematical Function Facility (except MG1l), which includes short and long precision versions of exponentiation, common logarithm and natural logarithm

Designed for High Availability
- Automatic reconfiguration of control storage using spare storage capacity
- Macro instruction retry
- Arithmetic logic unit and shifter provide automatic backup for hardware multiplier
- Dual processor:
  - In many cases, either instruction processor can operate as a uniprocessor if the other fails provided that the system is appropriately configured

Channel Subsystem

Channel Subsystem
- Channels operate in S/370 or XA mode
- Full support of dynamic path reconnection XA mode
- 256-byte buffer per channel minimizes interference to instruction processing
- Data streaming capability up to 3 Mb/sec on block multiplexor (BMPX) channels
- One optional Channel-To-Channel Adaptor attachable to any BMPX channel

Uniprocessors
- One channel subsystem each
- Six standard channels
- Six optional channels
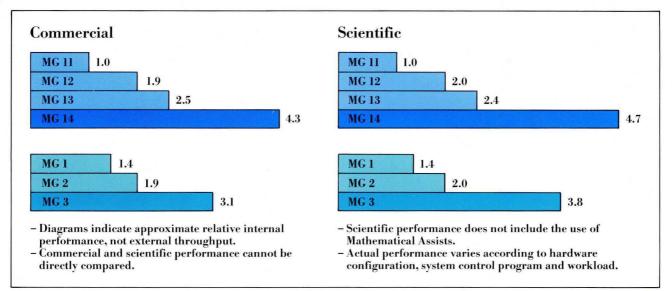- One or two byte multiplexor (MPX) channels

Dual Processor
- Two channel subsystems (one attached to each instruction processor)
- Each subsystem has the same channel characteristics
- 12 standard channels (six per instruction processor)
- Six optional channels (three per instruction processor)
- Standard channels include two, three or four byte multiplexor channels (one or two for each channel subsystem)

Designed for High Availability
- Automatic channel data buffer reconfiguration using spare buffer storage capacity
- Dual processor:
  - Each processor can access those I/O devices that are connected to (or switchable between) the two channel subsystems

Performance

Commercial

MG 11	1.0
MG 12	1.9
MG 13	2.5
MG 14	4.3

MG 1	1.4
MG 2	1.9
MG 3	3.1

– Diagrams indicate approximate relative internal performance, not external throughput.
– Commercial and scientific performance cannot be directly compared.

Scientific

MG 11	1.0
MG 12	2.0
MG 13	2.4
MG 14	4.7

MG 1	1.4
MG 2	2.0
MG 3	3.8

– Scientific performance does not include the use of Mathematical Assists.
– Actual performance varies according to hardware configuration, system control program and workload.

Field Upgrade Paths

MG 11 → MG 12 → MG 13 → MG 14

MG 1, MG 2, MG 3

Operating Modes, System Control Program and Microcode Support

Operating Modes	System Control Program	Microcode Assists
XA Mode	MVS/SP2	MVS/XA Assist DFSORT Assist
	VM/XA SF with VSE, VS1, MVS, VM Guest	SIE Assist
S/370 Mode	MVS/SP1	MVS Assist (1)
	VM/SP or VM/SP + HPO only (3) or with VSE, VS1, VM Guest VM/SP with MVS Guest	VM Assist, ECPS:VM (2, 4)
	VM/SP + HPO with MVS Guest	VM Assist, ECPS:VM (2, 4), PMA
	VSE, VS 1, TPF	–
Mathematical Assists	Multiply-and-Add, Square-Root Facility	
	Mathematical-Function Facilities (4) supported by Elementary Math Library (PRPQ P 81005)	

1. Includes ECPS:MVS functions. 2. Includes VM/HPO assist for HPO functions. 3. HPO reqired for greater than 16Mb storage sizes. 4. Except MG 11.

Configuration

	MG 11	MG 12	MG 13	MG 14
Main Storage (Mb)	4, 8, 16	8, 16, 24, 32	8, 16, 24, 32	16, 24, 32
High Speed Buffer (Kb)	4	32	64	2 x 64
Channels (Total)	6, 12	6, 12	6, 12	12, 18
Maximum Number of 3 Mb/sec Channels	4	6	9	16
Maximum Aggregate Data Rate (Mb/sec)	22	24	30	36 (18 each processor)
Processor Cycle Time (ns)	68	68	56	56

Physical characteristics

Item	Units		Uniprocessors	Dual Processor
Power Consumption	KVA	50 Hz	4.7	7.2
		60 Hz	4.7	7.2
Heat Output	Watts		4 000	6 600
	BTU/hr		13,650	22.500
Space (Footprint)	Sq. metres		1.34	1.34
	Sq. feet		14.33	14.33
Space (including service clearances)	Sq. metres		11.58	11.58
	Sq. feet		125.61	125.61
Operating Environment	°Centigrade		10 to 32	10 to 32
	°Fahrenheit		50 to 90	50 to 90
Relative Humidity	%		8 to 80	8 to 80
Maximum Wett Bulb	°Centigrade		23	23
	°Fahrenheit		73	73
Airflow	m³/min		37	57
	CFM		1300	2 000
Noise level	dB(A)		54.2	55.3
Weight (net)	kg		770	910
	lb		1700	2 000

Publications

IBM 4341/4381 Processor Installation Manual-Physical Planning	GA 24-4017
IBM 4381 Processor Family Steps Forward in Technology	G 580-1003
IBM 4381 Uniprocessor Functional Characteristics	GA 24-3947
IBM 4381 Dual Processor Functional Characteristic	GA 24-4021
Physical Planning Template: Metric	GX 24-3951
English	GX 24-3952
IBM 4381 Processor Operations Manual	GA 24-3982

IBM 4381 Processor Channel Characteristics	GA 24-3948
IBM 4381 IOCP Users Guide	GA 24-3964
IBM 4381 Processors Summary and Input/Output Data Communications Configurator	GA 24-3950
IBM 4381 Processors The clear choice for extended computing growth	G 520-1059
A Guide to the IBM 4381 Processor	GC 20-2021
IBM 4381 Processor Problem Analysis Guide	GA 24-3955

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G 511-0247-0 (02/86)   *Printed in Denmark*

Fair-Print AS, Roskilde