IBM Maintenance Library

This edition includes REA 06-88481.

8100 Information System

(Volume 3 of 4)

8130/8140 Processors

8101 Storage and Input/Output Unit

Maintenance Information

SY27-2521-3

The following listing shows, by volume (binder) number, the basic contents of the *8100 Information System Maintenance Information Manual*. The column not shaded indicates the volume you are using; the shaded columns indicate the contents of the other three volumes.

Chapter 5. MAP Reference Information
Communications Features
(CA)

Introduction

This part of Chapter 5 provides maintenance information to service the communications features used in the IBM 8130/8140/8101 units. When used with IMB's MAP Maintenance Package, the CA MAP diagnoses communications problems and refers to this part of Chapter 5 for information such as hardware locations, possible-cause-of-failure lists, and wiring checks.

This part has nine sections:

1. Quick Reference Guide (CA000–CA070) – Contains quick reference data and summary information on test routines, FACs, cards, cables, and miscellaneous items.
2. Communications General Information (CA100–CA166) – Contains information on communication configuration, operation, repair strategy, and fault isolation.
3. Offline and Online Tests (CA200–CA250) – Contains test information and lists possible causes of failure.
4. Intermittent Failure Repair Strategy (CA300–CA350) – Contains information to repair intermittent failures.
5. Signal Paths and Detailed Operational Description (CA400–CA489) –Contains figures and wiring charts which illustrate wiring and signal paths, and a general description of the hardware components.
6. Adjustment, Removal, and Replacement Information (CA500–CA590) – Contains information on cards, switches, jumpers, straps, board and cable locations, standard and special voltages, and troubleshooting procedures.
7. Cryptographic Devices, Interface and Line Descriptions, and Test Equipment Setup (CA600–CA653) – Contains information on cryptographic devices, line disciplines, and test equipment setup.
8. Word Trade Information (CA700–CA726) – Contains information on line disciplines for countries other than the United States.
9. Communications Specify Code (Minor) Changes (CA800) – Contains information on making Specify Code (Minor) changes.

Contents

Figures

Abbreviations

AA	auto answer
ac	alternating current
adr	address
A/S	adapter status
asm	assembly
B	byte
BA	beaconing address
BCC	block check character
BCLE	buffer control list element
BCW	buffer control word
BOP	basic operator panel
bps	bits per second
B/S	basic status
BSC	binary synchronous communications
BSTAT	basic status register
BU	bringup
C fld	control field
CA	communications attachment
CACX	pseudo cable group type
CAX	pseudo card type
CCITT	Consultative Committee of International Telephone and Telegraph Company
CH	channel
CHIO	channel I/O
clk	clock
CMDR	command reject
conn	connector
CRC	cyclic redundancy check
CSU	customer setup
CTS	clear to send
DA	device address
dBm	decibel per milliwatt
dc	direct current
DC	Direct Connect
DCE	data circuit-terminating equipment
DDD	direct distance dial
DDS	digital data service
DER	daily error rate
DISC	disconnect
DLA	data link adapter
DM	disconnect mode
DR	data ring
DRS	data rate select
drvr	driver
DSFC	data stream flow control
DSR	data set ready
DTR	data terminal ready
EFP	extended field panel
EIA	Electronic Industries Association
FAC	Features for Attaching Communications
FBI	flagged buffer indicator
FCS	frame check sequence field
FDM	function definition module
freq	frequency
FRMR	frame reject
FRU	field-replaceable unit
FX	foreign exchange
GCL	group control list
HW	halfword
Hz	Hertz (cycles per second)
HW	halfword
I/O	input/output
LA	logical address
LF	line frequency
LL	leased line
LSC	loop station connector
LSS	loop surge suppressor
LT	local test
LTST	local test
LU	logical unit
LWC	loop wiring concentrator
MAU	modem adapter unit
MD	maintenance device
MMR	monitor mode recover
MP	multipoint
msg	message
NPRO	nonproductive readout
NRZI	nonreturn to zero
NS	new sync
NSA	nonsequenced acknowledge
NSF	nonsequenced format
NSI	nonsequenced information
NSP	nonsequential poll
NSR	nonsequenced response
NTT	Nippon Telephone and Telegraph Co.
OEM	other equipment manufacturer
OH	off hook
ORP	optional response poll
ovrn	overrun
P	primary
PA	physical address
PD	protective device
P/F	poll/final bit
PSN	Public Switched Network
PTP	point to point
PTT	Postal Telephone and Telegraph
rcv	receive
rcvr	receiver
RD	request disconnect
resp	response
RFT	request for test
RI	ring indicate
RIM	request initialization mode
RLSD	receive line signal detect
RNR	receive not ready
ROI	request online
RQD	request disconnect
RQI	request for initialization
RR	receive ready
RTS	request to send
S	secondary
SCF	system control facilities
SDLC	Synchronous Data Link Control
SDLCB	Synchronous Data Link Control Block
sel	select
SIM	set initialization mode
SMN	system message number
SNBU	switched network backup
SNRM	Set normal response mode
SS	select standby
SSBY	select standby
S-S	start-stop
stdby	standby
SW	switched
TCM	test control monitor
TO	timeout
TP	teleprocessing
UA	unnumbered acknowledgment
UI	unnumbered information frame
UP	unnumbered poll

The following list is an acronym update that shows the relationship between the current acronyms for SDLC commands and responses and ones that a reader may encounter in earlier SDLC documentation.

New Acronym and Meaning		Old Acronym and Meaning	
DISC	disconnect		unchanged
DM	disconnect mode	ROI	request online
FRMR	frame reject	CMDR	command reject
RD	request disconnect	RQD	request disconnect
RIM	request initialization mode	RQI	request for initialization
SIM	set initialization mode		unchanged
SNRM	set normal response mode		unchanged
TEST	test		unchanged
UA	unnumbered acknowledgment	NSA	nonsequenced acknowledgment
UI	unnumbered information frame	NSI	nonsequenced information frame
UP	unnumbered poll	NSP	nonsequential poll

Communications Configuration Data Sheet

You may, if you wish, transfer Features for Attaching Communications (FAC) and addressing data from the customer's configuration data sheets to the tables below. This 8100 system data is useful as ready reference information for identifying system configuration, FACs, and addresses. It is recommended that, during the first communications problem call, you fill in the tables and update them as required.

The tables have four columns:

Column 1: Port Name

Column 2: Physical I/O Address (PA). The physical address of the communications port; see CA116 and CA513.

Column 3: FAC Code. The FAC code for the communications port; see CA111 and CA115.

Column 4: Remarks. Information you may wish to include which may be useful in identifying the configuration, such as feature description, attaching unit, or line type.

Customer Name

8130 or 8140 Model AXX **Serial Number** ____________

Port Name	Physical I/O Address (PA) Check if Used	FAC Code	Remarks
Communications Port 1	81 ________		
Communications Port 2	82 ________		
Communications Port 3	83 ________		
Communications Port 4	84 ________		
Communications Port 5	85 ________		
Communications Port 6	86 ________		

8101 Unit 1 **Serial Number** ____________

Port Name	Physical I/O Address (PA) Check if Used	FAC Code	Remarks
Communications Port 1	10 ________		
Communications Port 2	11 ________		
Communications Port 3	12 ________		
Communications Port 4	13 ________		
Communications Port 5	1C ________		
Communications Port 6	1D ________		
Communications Port 7	1E ________		
Communications Port 8	1F ________		

8140, Model BXX **Serial Number** ____________

Port Name	Physical I/O Address (PA) Check if Used	FAC Code	Remarks
Communications Port 1	80 ________		
Communications Port 2	81 ________		
Communications Port 3	82 ________		
Communications Port 4	83 ________		
Communications Port 5	50 ________		
Communications Port 6	51 ________		
Communications Port 7	52 ________		
Communications Port 8	53 ________		
Communications Port 9	5C ________		
Communications Port 10	5D ________		
Communications Port 11	5E ________		
Communications Port 12	5F ________		

8101 Unit 2 **Serial Number** ____________

Port Name	Physical I/O Address (PA) Check if Used	FAC Code	Remarks
Communications Port 1	20 ________		
Communications Port 2	21 ________		
Communications Port 3	22 ________		
Communications Port 4	23 ________		
Communications Port 5	2C ________		
Communications Port 6	2D ________		
Communications Port 7	2E ________		
Communications Port 8	2F ________		

8101 Unit 3 **Serial Number** ____________

Port Name	Physical I/O Address (PA) Check if Used	FAC Code	Remarks
Communications Port 1	30 ________		
Communications Port 2	31 ________		
Communications Port 3	32 ________		
Communications Port 4	33 ________		
Communications Port 5	3C ________		
Communications Port 6	3D ________		
Communications Port 7	3E ________		
Communications Port 8	3F ________		

8101 Unit 4 **Serial Number** ____________

Port Name	Physical I/O Address (PA) Check if Used	FAC Code	Remarks
Communications Port 1	40 ________		
Communications Port 2	41 ________		
Communications Port 3	42 ________		
Communications Port 4	43 ________		
Communications Port 5	4C ________		
Communications Port 6	4D ________		
Communications Port 7	4E ________		
Communications Port 8	4F ________		

CA000 Quick Reference Guide

This section contains the following quick reference data:

- Communication FAC – Hardware Test Summary, CA010.
- Communications Test Routine Summary, CA020.
- Test Invocation Summary, CA030.
- Test Messages References, CA040.
- Card Summary, CA050.
- 8100 Communications Cable Summary, CA060.
- Miscellaneous Information, CA070:
  - I/O Panel, Card, and Board Location References.
  - Switches, Jumpers, and Straps References.
  - Troubleshooting Diagrams References.
  - Voltage Levels

CA010 Communications FAC — Hardware Test Summary

FAC	Configuration Table Data	Card/Cable Type	Card Jumpers	Board Jumpers	Required Test Routines
8	SDLC. Primary, loop, 1 lobe, loop supplied clock, 38.4 Kbps.	CA1, CA3, CAC3.	Loop - Primary Select - Lobe Operation - Serial - Carrier Select - Data Select	1. Channel request 2. Channel grant	1-15, 18, 51, 73, 75* 76, 88*, 90* — 94.
9	SDLC. Primary, loop, 2 lobe, loop supplied clock, 38.4 Kbps.	CA1, CA3, CA4, CAC3, CAC4.	Loop - Primary Select - Lobe Operation - Serial - Carrier Select - Data Select	1. Channel request 2. Channel grant	1-15, 18, 52, 73, 75*, 76, 89, 90* — 94.
10	SDLC. Primary, loop, 1 lobe, loop supplied clock, 9600 bps.	CA1, CA3, CAC3.	Loop - Primary Select - Lobe Operation - Serial - Carrier Select - Data Select	1. Channel request 2. Channel grant	1-15, 18, 51, 73, 75*, 76, 88, 90* — 94.
11	SDLC. Primary, loop 2 lobe, loop supplied clock, 9600 bps.	CA1, CA3, CA4, CAC3, CAC4.	Loop - Primary Select - Lobe Operation - Serial - Carrier Select - Data Select	1. Channel request 2. Channel grant	1-15, 18, 52, 73, 75*, 76, 89, 90* — 94.
12	SDLC. Primary or Secondary, EIA, adapter clock, external modem, 600, 1200 bps, line variables**.	CA1, CA5, CAC5A	EIA - Internal Wrap - 8100 clock	1. Channel request 2. Channel grant 3. Data rate	1-15, 16, 53*(P), 63, 64(1), 71*(S), 75(P), 90*, 91*, 93*, 94*
13	SDLC. Primary or Secondary, EIA, external modem/DCE, external clock, 2.0, 2.4, 4.8, 7.2, 9.6 Kbps, data-link attached Loop line variables**	CA1, CA5, CAC5A.	EIA - Internal Wrap - DCE clock	1. Channel request 2. Channel grant	1-15, 16, 53*(P), 63, 64(I)*, 71*(S), 75(P), 90*, 91*, 93*, 94*, 95*–99(DL).
15	SDLC. Primary, EIA direct connect, adapter clock, 600, 1200, 2400 bps.	CA1, CA5, CAC5B	EIA - Internal Wrap - 8100 clock	1. Channel request 2. Channel grant 3. Data rate	1-15, 16, 53*, 61, 75*, 90*, 91*, 93*, 94*.
16	SDLC. Primary, EIA direct connect, multi-speed clock, 4.8, 9.6 Kbps	CA1, CA5, CA10, CAC5B	EIA - Internal Wrap - 8100 clock Multispeed clock - LF	1. Channel request 2. Channel grant	1-15, 16, 53*, 61, 75*, 90*, 91*, 93*, 94*.
17	SDLC. Secondary, EIA direct connect, external clock, 2.0, 2.4, 4.8, 7.2, 9.6 Kbps	CA1, CA5 CAC5B	EIA - Internal Wrap - DCE clock	1. Channel request 2. Channel grant	1-15, 16, 61, 71*.
18	SDLC. Primary or secondary, integrated modem, nonswitched, adapter clock, 600, 1200 bps **Line Variables	CA1, CA8, CAC8	Integrated Modem - 2/4 Wire - CTS Set - Echo clamp - Transmit Level - Equalizer	1. Channel request 2. Channel grant 3. Data rate	1-15, 19, 53*(P), 71*(S), 75*(P), 90*, 91*, 93*, 94*(P)
19	SDLC. Secondary, integrated modem, switched line, adapter clock, 600, 1200 bps **Line Variables	CA1, CA9, CAC9	Integrated Modem - Coupler - Equalizer - Normal Ops - Transmit	1. Channel request 2. Channel grant 3. Data rate	1-15, 20, 25, 71(S)
20	SDLC. Primary or secondary, DDS, DDS supplied clock, 2.4, 4.8, 9.6 Kbps	CA1, CA7, CAC7	DDSA - DDL - Data rate	1. Channel request 2. Channel grant	1-15, 21, 22, 53*(P), 66, 71*(S), 75*(P), 90*, 91*, 93*, 94*(P)
21	SDLC. Secondary, DDS, DDS supplied clock, 56 Kbps (8140 only)	CA1, CA7, CAC7	DDSA - DDL - Data rate	1. Channel request 2. Channel grant	1-15, 21, 22, 66, 71*
24	SDLC. Primary, V.35, direct connect, adapter clock, 600, 1200, 2400 bps	CA1, CA6, CAC6B	V.35 - Internal Wrap - 8100 clock	1. Channel request 2. Channel grant 3. Data rate	1-15, 16, 53*, 63, 75*, 90*, 91*, 93*, 94*

Legend:
*Link level test.
**Line variables are dependent on customer operations and data link order. For description, see CA114 and CA115.
DL = Data link attached loop
I = IBM modem
P = Primary
S = Secondary

FAC	Configuration Table Data	Card/Cable Type	Card Jumpers	Board Jumpers	Required Test Routines
25	SDLC. Primary, V.35, direct connect multispeed clock, 4.8, 9.6 Kbps	CA1, CA6, CAC6B	V.35 - Internal Wrap - 8100 clock Multispeed clock - LF	1. Channel request 2. Channel grant	1-15, 16, 53*, 63, 90*, 91*, 93*, 94*
26	SDLC. Primary or secondary, V.35, direct connect multi-speed clock, 56 Kbps	CA1, CA6, CAC6B	V.35 - Internal Wrap - 8100 clock Multispeed clock - LF	1. Channel request 2. Channel grant	1-15, 16, 53*(P), 63, 71*(S), 90*, 91*, 93*, 94*
27	SDLC. Secondary, V.35, direct connect, external clock, 0.6, 1.2, 2.0, 2.4, 4.8, 7.2, 9.6 Kbps	CA1, CA6, CAC6B	V.35 - Internal Wrap - DCE clock	1. Channel request 2. Channel grant	1-15, 16, 63, 71*
28	SDLC. Primary or secondary, V.35, direct connect external clock, 56 Kbps	CA1, CA6 CAC6B	V.35 - Internal Wrap - DCE clock	1. Channel request 2. Channel grant	1-15, 16, 53*(P), 63, 71*, 90*, 91*, 93*, 94*
29	SDLC. Secondary, V.35, external clock, 48, 56 Kbps external modem	CA1, CA6, CAC6B	V.35 - Internal - DCE clock	1. Channel request 2. Channel grant	1-15, 16, 63, 71*(S)
A1 (RPQ 870892)	SDLC. Primary, V.35, direct connect, multispeed clock, 19.2 Kbps	CA1, CA6, CA10, CAC6B	V.35 - Internal Wrap - 8100 clock Multispeed clock - LF	1. Channel request 2. Channel grant	1-15, 16, 53*, 63, 90*, 91*, 93*, 94*
30	SDLC. Primary or secondary, X.21, nonswitched, external clock, 2.4, 4.8, 9.6 Kbps, external DCE	CA1, CA11, CAC11	X.21 - Normal Wrap - Nonswitched Line - Timed DSR Drop - Normal Operation - Error Latch Disable - CTS Delay	1. Channel request 2. Channel grant	1-15, 16, 53*, 67, 68, 71(S), 75*, 90*, 91*, 93*, 94*
31	SDLC. Primary or secondary, X.21, nonswitched, external clock, 48 Kbps, external DCE	CA1, CA11, CAC11	X.21 - Normal Wrap - Nonswitched Line - Timed DSR Drop - Normal Operation - Error Latch Disable - CTS Delay	1. Channel request 2. Channel grant	1-15, 16, 53*, 67, 68, 71(S), 75*, 90*, 91* 93*, 94*
40	BSC. Primary or secondary, EIA, adapter clock external modem, 600, 1200 bps **Line Variables	CA2, CA5, CAC5A	EIA- Internal Wrap - 8100 clock	1. Data rate	1-15, 16, 63, 64, 65, 77*, 78*

FAC	Configuration Table Data	Card/Cable Type	Card Jumpers	Board Jumpers	Required Test Routines
41	BSC. Primary or secondary, EIA, external modem, external clock, 2.0, 2.4, 4.8, 7.2, 9.6 Kbps **Line Variables	CA2, CA5, CAC5A	EIA - Internal Wrap - DCE clock		1-15, 16, 63, 64, 65*, 77*, 78
43	BSC. Primary, EIA, direct connect, adapter clock, 600, 1200 bps	CA2, CA5, CAC5B	EIA - Internal Wrap - 8100 clock	1. Data rate	1-15, 16, 61, 77*, 78*
44	BSC. Primary, EIA direct connect, multispeed clock, 2.4, 4.8, 9.6 Kbps	CA2, CA5, CA10, CAC5B	EIA - Internal Wrap - 8100 clock Multispeed clock - LF		1-15, 16, 61, 77*, 78*.
45	BSC, Primary or secondary, integrated modem, nonswitched, adapter clock, 600, 1200 bps	CA2, CA8, CAC8	Integrated modem - 2/4 wire - CTS set - Echo clamp - Transmit level - Equalizer	1. Data rate	1-15, 19, 77*, 78*
47	BSC. Primary or secondary, DDS, interface supplied clock, 2.4, 4.8, 9.6 Kbps	CA2, CA7, CAC7	DDSA - DDL - Data rate		1-15, 21, 22, 66, 77*, 78*
60	Start/Stop. Primary, EIA, external modem, adapter clock 110, 134.5, 150, 300, 600 bps **Line Variables	CA2, CA5, CAC5A	EIA - Internal Wrap - 8100 clock	1. Data rate 2. Asynchronous	1-15, 16, 63, 64, 79* – 87
61	Start/Stop Primary, EIA, direct connect, adapter clock, 110, 134.5, 150, 300, 600 bps	CA2, CA5, CAC5B	EIA - Internal Wrap - 8100 clock	1. Data rate 2. Asynchronous	1-15, 16, 61, 79 – 87

Legend:
*Link level test.
**Line variables are dependent on customer operations and data link order. For description, see CA114 and CA115.
DL = Data link attached loop
I = IBM modem
P = Primary
S = Secondary

REA 06-88481

CA020 Communications Test Routine Summary

RT	Description	SDLC	BSC S-S	Adr Lvl	Invocation (see Notes): Offline MAPs	Offline F/L	DPCX	CSU	MI
01	Adapter card tests	X	X	1	X	X	X	X	
02	Adapter card tests	X	X	1	X	X	X	X	
03	Adapter card tests	X	X	1	X	X	X	X	
04	Adapter card tests	X	X	1	X	X	X	X	
05	Adapter card tests	X	X	1	X	X	X	X	
06	Adapter card tests	X	X	1	X	X	X	X	
07	Adapter card tests	X	X	1	X	X	X	X	
08	Adapter card tests	X	X	1	X	X	X	X	
09	Adapter card tests	X	B	1	X	X	X	X	
0A	Adapter card tests	X	B	1	X	X	X	X	
0B	Adapter card tests	X	B	1	X	X	X	X	
0C	Adapter card tests	X	B	1	X	X	X	X	
0D	Adapter card tests	X	S	1	X	X	X	X	
0E	Adapter card tests	X	B	1	X	X	X	X	
0F	Adapter card tests	X	B	1	X	X	X	X	
10	Adapter card tests	X	S	1	X	X	X	X	
11	Adapter card tests	X	S	1	X	X	X	X	
12	Adapter card tests	X	B	1	X	X	X	X	
13	Adapter card tests	X	B	1	X	X	X	X	
14	Adapter card tests		S	1	X	X	X	X	
15	Adapter card tests	X	X	1	X	X	X	X	
16	Internal/external data wrap	X	X	1	X	X	X		
18	Loop adapter card test	X		1	X	X		M/8	
19	Integrated modem (nonswitched)	X	X	1	X	X		X	
20	Integrated modem (switched)	X	X	1	X	X		X	
21	DDSA test	X	X	1	X	X			
22	DDSA internal wrap	X	X	1	X	X		X	
25	Auto answer	X	X	1	16	16			17
51	Loop — 1 lobe	X		1	15	15	15		
52	Loop — 2 lobe	X		1	15	15			
53*	Data link group	X		1	P/5	5	5		
61	EIA — direct connect	X	X	1	6	6		M/6	
63	EIA/V.35 — external test	X	X	1	7	7		M/7	
64	IBM modem analyzer	X	X	1	X	X			17
66	DDSA — external	X	X	1	9	9		9	
67	X.21 — external 1	X		1	9	9			
68	X.21 — external 2	X		1	9	9			
71*	SDLC secondary link	X		2		10	11		17
72	Data link loop — poll test	X		2	X	X			17
73	Loop station relay pick	X		1	12	12			
75*	Link/loop group analysis	X		1	5	5	5		17
76	Loop beacon/ordinal sequence	X		1		5	5		17
77*	BSC link — requestor		X	2		13			17
78*	BSC link — responder		X	2		14			17
79*	2741 all characters		X	2		X			17
80*	2741 tilt, rotate, twist		X	2		X			17
81*	2741 special function		X	2		X			17
82*	2741 read		X	2		X			17
83*	2741 echo		X	2		X			17
84*	2741 attention key		X	2		X			17
85*	TTY aux line test		X	2		X			17
86*	TTY aux echo test		X	2		X			17
87*	2741 aux line		X	2		X			17
88	Loop — 1 lobe poll test	X		1		X	X		17
89	Loop — 2 lobe poll test	X		1		X			17
90$	SDLC link test cmd—no data	X		2/3		5	5		
91$	SDLC link test cmd — data	X		2/3		5	5		
92$	Monitor mode	X		2/3		5	5		
93$	SDLC link test — user data	X		2/3		5	5		17
94$	Line analysis	X		2/3		5	5		17
95*	384X SDLC test cmd	X		2		5	X		
96*	384X loop data	X		2		5	X		
97	Configuration self-test to 384X	X		2		5	X		
98	384X loop beacon and ordinal	X		2		5	X		17
99*	384X loop-lobe analysis	X		2		5	X		17

Notes:

* — *Link level test*
$ — *Link level test; level 2 addressing for directly attached loops or data link stations; level 3 addressing for data link attached loop devices.*
B — *BSC only*
F/L — *Free-lance*
M — *Modified*
MI — *Manual Intervention messages*
P — *If Primary*
S — *Start-Stop only*
X — *Normal invocation*

1. *Address level 1*
2. *Address level 2*
3. *Address level 3*
4. *Not used.*
5. *Group stations/devices/units must be in a ready condition before this test is invoked.*
6. *These tests must be run when the EIA-direct connect cable is isolated from the direct-connected host/device using the EIA-direct connect wrap plug.*
7. *Use the V.35 wrap plugs or the EIA modem cable test switch to isolate the EIA modem or V.35 communications cable from the external modem or host connection.*
8. *For CSU only, a loop wrap plug must be installed at the end of the loop cable(s) before running this test.*
9. *This test must be run with the external cable switch in the test position.*
10. *The host or controller must send SDLC link test commands to the 8100 Processor (invoke routine 71). Coordination between the two sites is required for the start and end of test. This test requires manual intervention. See Chapter 2 for routine termination procedures.*
11. *Use DPCX SDLC link test procedure, CA223.*
12. *See CA551/CA653 for setup procedures. See Chapter 2 for termination procedures.*
13. *The responding unit must be ready to respond.*
14. *This test should be initiated before a requesting device/unit issues a test request.*
15. *Loop cable(s) must be plugged into the loop station connector(s) (LSC).*
16. *The external communications cable must be attached to both the 8100 and the telephone line via the Data Access Arrangement.*
17. *Refer to CA210 for Manual Intervention messages.*

CA030 Test Invocation Summary

A summary of standard and unique invocation procedures for communications feature tests is given below. Special invocation notes for each routine and addressing levels are given in the Communications Test Routine Summary.

INVOCATION FOR A GROUP OF TESTS (LEVEL 1 ADDRESSING ONLY)

1. The test control monitor (TCM) has been loaded and is at an 80BC or PA00 wait stop.
2. Enter PAB.
   where:
   PA = Adapter physical address – level 1 only
   B = Enters invocation message – address field section
3. At 81BC wait stop, enter SLB.
   where:
   S = Sense option
   - 0 = Run adapter routines (1–15)
   - 1 = Run adapter and driver card routines (S = 0 tests, and one of the following: 16 or 18 or 19 or 20 or 21 and 22).
   - 2 = Run adapter and driver card routines and basic link level tests (S = 1 tests, and one of the following: 51 or 52 or 53).

   Note: *Default value = 0.*

   L = Looping option
   - 0 = Run routines one time
   - *1 = Loop selected routines; stop on error
   - *2 = Loop selected routines; no stop on error

   Note: *Default value = 0.*

   B = Enters invocation message – option field section and begins test execution.

*In DPCX online, looping is five times.

INVOCATION FOR A SINGLE TEST ROUTINE (ANY LEVEL ADDRESSING)

1. The test control monitor (TCM) has been loaded and is at an 80BC or PA00 wait stop.
2. Enter PASADAB
   Enter address field(s) as required. Address field definition is determined by either the test routine (see CA201 test summary for address levels) and/or by the customer configuration data sheet or the configuration table (see Chapter 2, CP300, on how to obtain the configuration table).
   where:
   PA = Adapter physical address – level 1
   SA = Group or station address – level 2
   DA = Station or device address – level 3
   B = Enters invocation message – address field section
3. At 81BC wait stop, enter SLRRB
   Enter option fields as required.
   where:
   S = Sense option:
   = Always zero (0).
   L = Loop option
   - 0 = Run routine one time
   - *1 = Loop selected routine; stop on error
   - *2 = Loop selected routine; no stop on error

   RR = Routine number
   B = Enters invocation message – option field section and begins test execution.

*In DPCX online, looping is five times.

CA040 Test Messages References

Manual Intervention Messages. Refer to CA210.

Error Messages. Refer to CA241.

CA050 Card Summary

Card ID	Description	MIM CA Reference
CA1	SDLC Adapter	CA451, CA481, CA512
CA2	BSC/S-S Adapter	CA455, CA482, CA512
CA3	Loop Adapter, One-Lobe	CA475, CA487, CA512, CA563
CA4	Loop Adapter, Second Lobe	CA475, CA487, CA512, CA563
CA5	EIA	CA472, CA483, CA512, CA563
CA6	V.35	CA474, CA488, CA512, CA563
CA7	DDS Adapter	CA471, CA486, CA512, CA563
CA8	Integrated Modem, Nonswitched	CA473, CA484, CA512, CA563
CA9	Integrated Modem, Switched	CA473, CA485, CA563
CA10	Multispeed Clock	CA476, CA512, CA563
CA11	X.21, Nonswitched	CA477, CA489, CA512, CA563

CA060 8100 Communications Cable Summary

					External Cable		External Cable	
MIM Cable ID	Cable Description	MIM Reference	Internal Cable Part Number	Plug/ Cable ID Code	Group Number	Option 1 – Cable Part Number	Wrap Plug Part Number	Option 2 – Cable Part Number
CAC3	Loop – Single-lobe	CA435	8269773	E	3709	7389950	7389282 (Note 1)	Same as option 1
CAC3	Loop – Two-lobe (1st)	CA435	8269773	E	3726-A	7389950		
CAC4	Loop – Two-lobe (2nd)	CA435	8269774	E	3726-B	7389950		
CAC5A	EIA – Modem (except Japan)	CA431	8269775 8269784(UK)	C C	3724 3724	8269826* 8269826*	Use Modem Interface Test Set (Note 2)	7389484
CAC5A	EIA – Modem (Japan)	CA431	8269775	C	3729	6835482*		
CAC5B	EIA – Direct Connect-Terminal	CA431	8269775 8269784(UK)	H H	3721 3721	4946680 (EC389171) 4946680 (EC389171)	6835347 or 6835642	Same as option 1
CAC5B	EIA – Direct Connect Peer-to-Peer	CA431	8269775 8269784(UK)	H H	3727 3727	6835405 6835405		
CAC6A	V.35 – External Modem	CA433	8269777 8269783(UK)	G G	3718 3718	8269589 8269589	6835348	Same as option 1
CAC6B	V.35 – Direct Connect-Terminal	CA433	8269777 8269783(UK)	J J	3719 3719	8269590 8269590	6835349	Same as option 1
CAC6B	V.35 – Direct-Connect – Peer-to-Peer	CA433	8269777 8269783(UK)	K K	3720 3720	8269591 8269591	6835353	Same as option 1
CAC7	DDS	CA432	8269774	F	3717	8269827*	6835350	8269540*
CAC8	Integrated Modem-NS – WT except Canada, Japan	CA434	8269774	A	3722	7389482	No	No
CAC8	Integrated Modem-NS – U.S., Canada, Japan	CA434	8269774	B	3723	7389483	No	No
CAC9	Integrated Modem-SW – WT	CA434	7389491	A	3722	7389482	No	No
CAC9	Integrated Modem-SW – U.S., Canada	CA434	8269772	D	3725	7389485	No	No
CAC11	X.21 (Nonswitched) – Japan only	CA436	8269777	P	3728	8269828*	6835379	6835364

*Cable with Wrap Switch Assembly.

Note 1: *Use plug at CSU only.*

Note 2: *Modem clock must be passed to 8100 for CE testing.*

CA070 Miscellaneous Information

Locations.
I/O Panel – Refer to CA420
Card and Board – Refer to CA520

Switches, Jumpers, and Straps. Refer to CA560.

Troubleshooting Diagrams. Refer to CA540.

Voltage Levels.

Voltage	Range	Test Point	
+5V dc	+4.5 to +5.5	D03	On SDLC (CA1) card BSC/S-S (CA2) card
+8.5V dc	+7.7 to +9.3	B11	
-5.0V dc	-4.5 to -5.5	B06	
Ground		D08	
-8.5V dc	-7.7 to -9.3	D07 –	On EIA (CA5) card V.35 (CA6) card

CA100 General Information

This section provides introductory, overview, reference, and summary information to support the communications sections which follow.

CA110 Configuration

CA111 Hardware

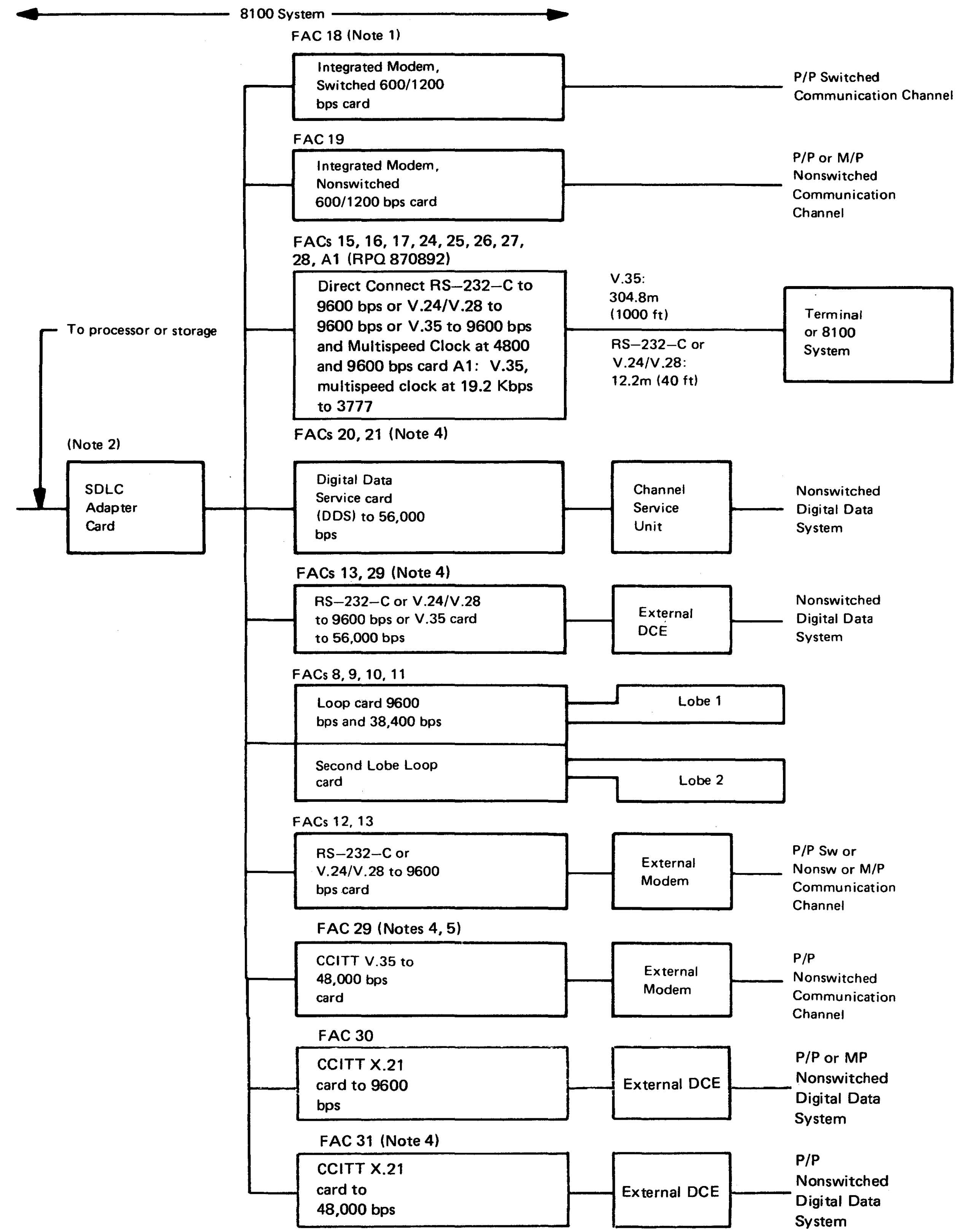
The 8100 system has 11 basic physical hardware configurations, which are the basis for testing and FRU isolation. These configurations are expanded by software and other communications characteristics to over 30 types of communication capabilities. (Each type of communications capability is identified by a two-digit Features for Attaching Communications (FAC) code for ordering purposes.) The 11 basic configurations are:

1. SDLC (CA1) adapter card and EIA/CCITT (CA5)/V.35 (CA6) card – external modem.
2. SDLC (CA1) adapter card and EIA/CCITT (CA5)/V.35 (CA6) card – direct connect.
3. SDLC (CA1) adapter card and integrated modem switched (CA9) or nonswitched (CA8) card.
4. SDLC (CA1) adapter card and DDS (CA7) card.
5. SDLC (CA1) adapter card and X.21 (nonswitched) (CA11) card.
6. SDLC (CA1) adapter card and one loop (CA3) card (one-lobe loop).
7. SDLC (CA1) adapter card and two loop (CA3 and CA4) cards (two-lobe loop).
8. BSC/S-S (CA2) adapter card and EIA/CCITT (CA5) card – external modem.
9. BSC/S-S (CA2) adapter card and EIA/CCITT (CA5) card – direct connect.
10. BSC/S-S (CA2) adapter card and integrated modem (CA8) nonswitched card.
11. BSC/S-S (CA2) adapter card and DDS (CA7) card.

Figures CA111-1, CA111-2, and CA111-3 summarize the hardware configurations and show their relationship to the FAC codes. (FAC codes are detailed in CA115.)

The names of the communications cables and their identification number (CACX) are as follows:

Cable Name	Identification Number
Directly attached loop (first lobe) cable	CAC3
Directly attached loop (second lobe) cable	CAC4
EIA external modem cable	CAC5A
EIA direct connect cable	CAC5B
V.35 external modem cable	CAC6A
V.35 direct connect cable	CAC6B
DDS cable	CAC7
Integrated modem (nonswitched) cable	CAC8
Integrated modem (switched) cable	CAC9
X.21 (nonswitched) cable	CAC11



Notes:

1. The FAC numbers identify SDLC communications capabilities that are described in more detail, including regional capability, in Figure CA115-2.

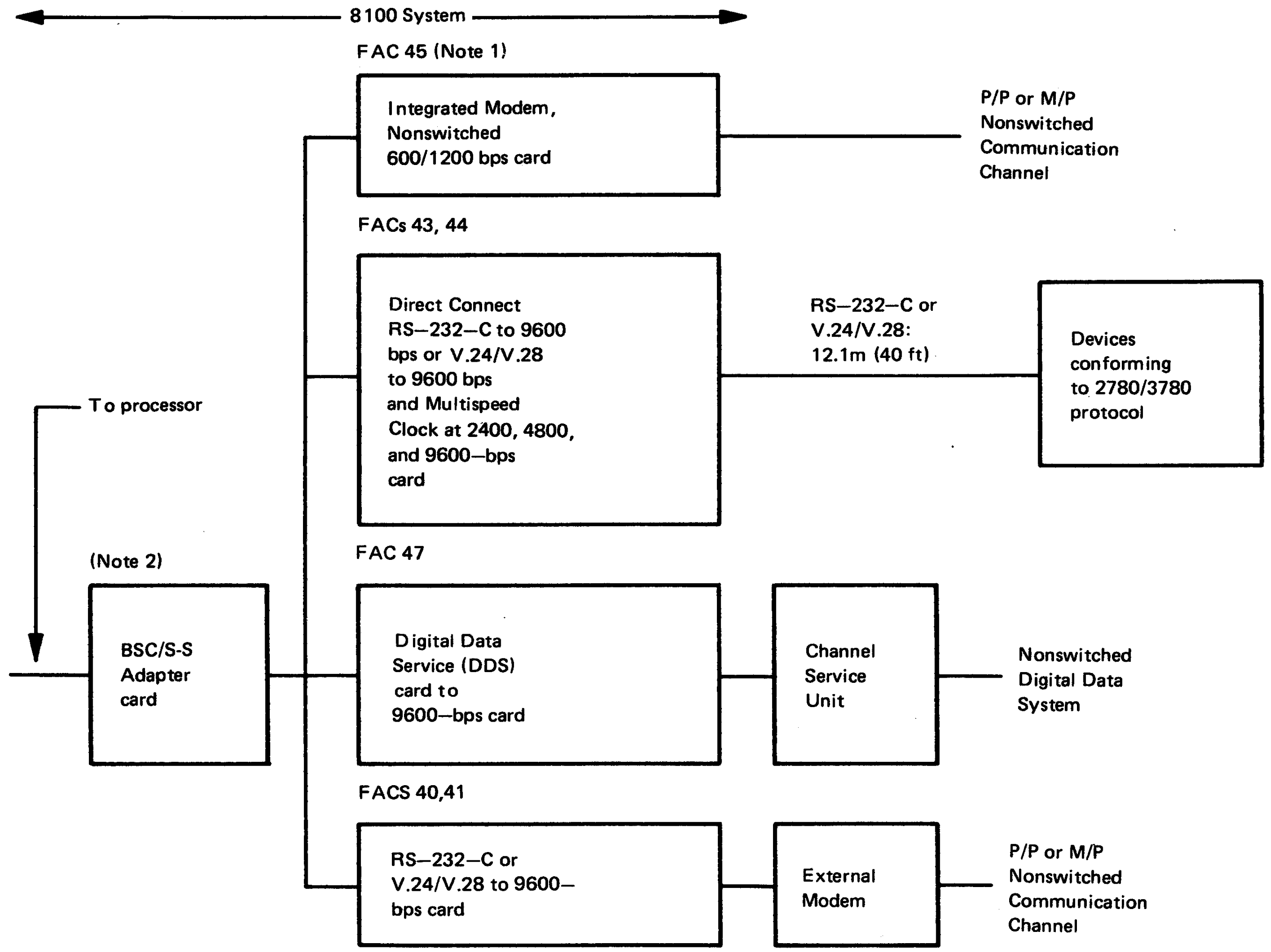
2. One SDLC adapter card is required for each SDLC FAC.

3. Only 10 SDLC loop and communication FACs can be active at one time.

4. FACs 21, 29, and 31 are available only on the 8140 and any 8101s attached to the 8140. Maximum speed for FACs 13 and 20 is 9600 bps.

5. For countries other than the U.S. and Canada, FAC 29 is available at a maximum speed of 48,000 bps.

Figure CA111-1. SDLC Features for Attaching Communications (FACs) Summary



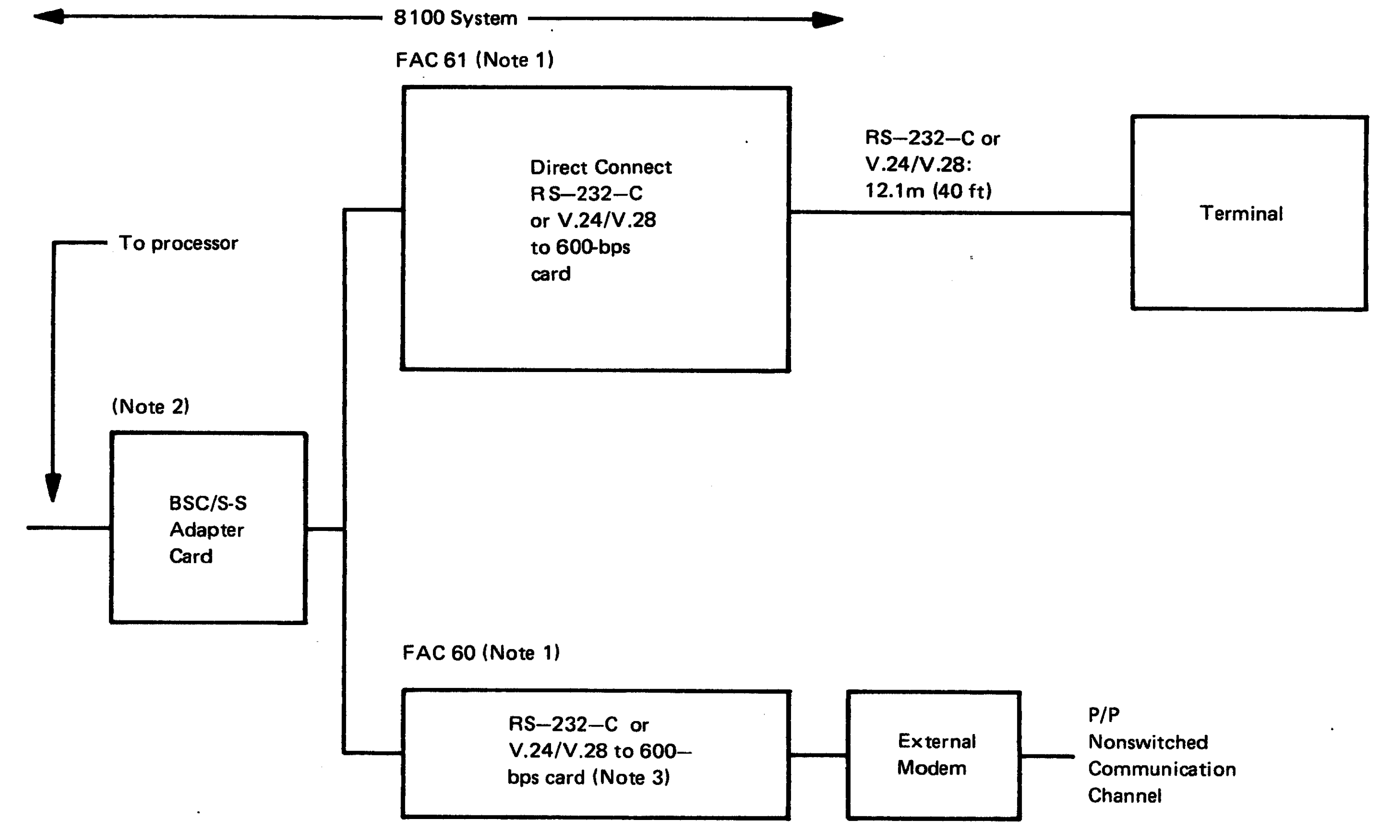
Notes:

1. The FAC numbers identify BSC communications capabilities that are described in more detail, including regional capability, in Figure CA115-2.

2. One BSC/S-S adapter card is required for each BSC FAC.

3. With an 8130 Processor, the maximum aggregate BSC data rate is 9600 bps. With an 8140 Processor, the maximum aggregate BSC data rate is 19,200 bps.

Figure CA111-2. BSC Features for Attaching Communications (FACs) Summary



Notes:

1. The FAC numbers identify S/S communications capabilities that are described in more detail in Figure CA115-2.

2. One BSC/S-S adapter card is required for each S/S FAC.

3. With an 8130 Processor, the maximum aggregate S/S data rate is 330 bps. With an 8140 processor, the maximum aggregate S/S data rate is 660 bps.

Figure CA111-3. S/S Features for Attaching Communications (FACs) Summary

CA112 Addressing

There are up to three levels of software addressing for CA feature tests: Physical Address (PA) for the adapter or port, Station Address (SA) for the group or station, and Device Address (DA) for the station or device. See Figure CA112-1.

- Two hexadecimal characters (PA) define the adapter physical address. The first character (P) specifies the SSCF adapter group address, which is determined by the setting of the SSCF address switches. The second character (A) specifies the adapter address within the adapter group.
- Two hexadecimal characters define the group, station, or device address.

LEVEL	ADDRESSES
Level 1 (PA)	Adapter/Driver Card/Cables
Level 2 (SA)	Data link stations – Multipoint – Point-to-point Directly attached loop stations Data link attached loop groups
Level 3 (DA)	Data link attached loop stations or devices.

See CA116 for the available port addressing by machine type and model; see Chapter 2, CP200, for general 8100 addressing structure.

EXAMPLES:

1. Define the complete address field for adapter PA = 10, group address = 22, and device address = 01. (level-3 addressing).

   Address field = 102201

2. Define the complete address field for adapter PA = 24 and station address = 10. (level-2 addressing).

   Address field = 2410

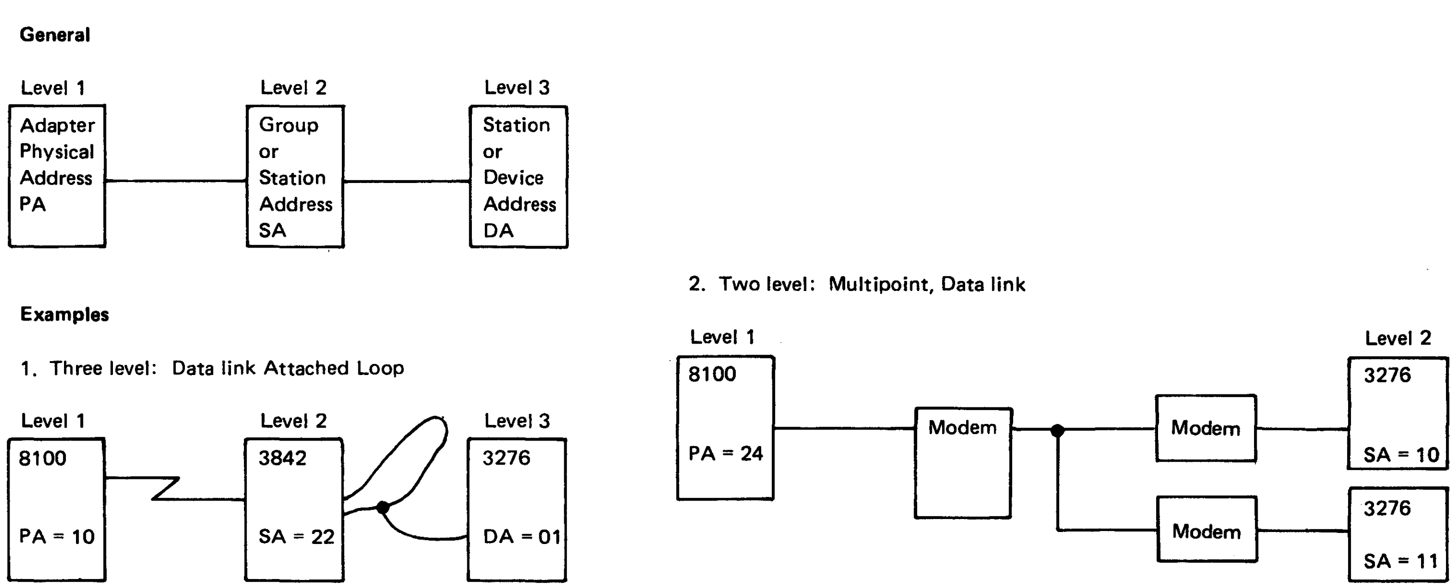


Figure CA112-1. Addressing Levels

CA113 Configuration Table Entries for Installed FACs

The configuration table for the communications feature contains information required for the CA MAP and test control, and specifically identifies the CA feature (hardware, function, physical address, and line discipline). The configuration table resides on the MD diskette 02.

DPCX has no formal configuration table; however, the communication parameters are defined using the SYSIMOD function (see Chapter 2). The CA MAP configuration format is as follows:

LV PA UTUT OPOP OPOP

Where:

LV	=	Addressing level (1 byte)
PA	=	Physical address (1 byte)
UTUT	=	Unit type (2 bytes)
OPOP OPOP	=	Option fields (bytes 1-4)

1 2 3 4 (bytes)

For the CA feature, LV has values 01, 02, or 03 where:

01 is adapter or port address level

02 is group or station address level

03 is station or device address level

PA is the physical address of a given level

UTUT has the values shown in Figure CA113-1.

The option fields are described in Figures CA113-2 and CA113-3.

Figure CA113-4 shows examples of communications configuration tables.

Description	Unit Type (UTUT)	Level (LV)	Options Fields (OPOP OPOP)
SDLC Adapter	0060	01	See Figure CA113-2.
BSC/S-S Adapter	0061	01	See Figure CA113-2.
3277, 3284, 3286, 3287, 3288	0100	03	Not used*
3276, XXXX, 3767	0200	02/03	Not used*
SDLC Secondary (Link Address)	0201	02	Not used*
3641	0240	02/03	Not used*
3842, 3843	0250	02	Not used*
3642	0291	02/03	Not used*
3643	0292	02/03	Not used*
3644	0293	02/03	Not used*
3646	0294	02/03	Not used*
3647	0295	02/03	Not used*
Start/Stop 2741	0300	02	Not used*
Start/Stop TTY 33/35	0301	02	Not used*
BSC (Link Address)	0302	02	Not used*

*Uses level 1 information.

Figure CA113-1. Unit Type (UT) Values

OPOP OPOP has the following values:

1 2 3 4 bytes)

Level 1

Options Byte	Bits	Descriptions
1	0123	Line Discipline:
	0000	SDLC
	0001	S-S
	0010	BSC
1	4567	Driver Hardware:
	0000	EIA
	0001	Integrated modem
	0010	Loop adapter
	0011	V.35
	0100	DDSA
	0101	X.21
2	0123	Driver Hardware:
	0000	External modem (EIA or V.35)
	0001	Direct connect (EIA or V.35)
	0000	1 lobe (loop adapter)
	0001	2 lobes (loop adapter)
	0000	Nonswitched line (integrated modem or X.21)
	0001	Switched line (integrated modem or X.21)
2	4567	Clocking:
	0000	External clock
	0001	Adapter clock
	0010	Multispeed clock
	0011	Loop/DDSA supplied clock
3	0123	Line Discipline:
SDLC	0000	Primary
	0001	Secondary
BSC	0000	Primary multipoint
	0001	Secondary multipoint
	0010	Primary point-to-point
	0011	Secondary point-to-point
S/S	0000	2741 (134.5 bps)
	0001	TTY 11 bit (110 bps)
	0010	TTY 10 bit (150 bps)
	0011	TTY 10 bit (300 bps)
	0100	TTY 10 bit (600 bps)
3	4567	Variable Adapter
		SDLC
	0000	High-channel request priority OFF
	0001	High-channel request priority ON
4	0123	Line Variables:
	1000	Reserved
	0100	Data rate select
	0010	Select standby
	0001	*Non return to zero insertion (NRZI) mode
4	4567	Line Variables:
	1000	Permanent request to send
	0100	101.1
	0010	Tone
	0001	Switched line

*For setting:

- 3842 – NRZI = 1, required
- 3843 – NRZI = optional and modem dependent
- Modem – See modem manual

There must be consistency in NRZI setting in all modems and controllers throughout the network for proper operation. Both software and hardware must be correctly configured.

Figure CA113-2. Option Field Description

Option Field	Explanation*
Byte 1, Bits 0–3	Define the line protocol or discipline of this feature and the communications adapter card.
Byte 1, Bits 4–7	Define the communications driver card used for this feature.
Byte 2, Bits 0–3	Provide additional detail on the communications driver card.
Byte 2, Bits 4–7	Define the clock source for this feature. An external clock is a source external to the 8100 System. An adapter clock is an internal source and is located on the SDLC or BSC/S-S communications adapter. A multispeed clock is an internal source and is located on the multispeed clock card (CA10). A loop/DDS-supplied clock is either derived from or provided by the loop or DDS card.
Byte 3, Bits 0–3	Provide additional detail on the communications feature configuration and line discipline based on Byte 1, Bits 0–3. SDLC defines the primary or secondary status of this feature. BSC defines the multipoint or point-to-point configuration and the primary and secondary status of this feature. Start-stop defines the 2741 or Teletype (TTY) configuration; 10- or 11-bit codes and communications line speed.
Byte 3, Bits 4–7	SDLC adapter is ON or OFF High Channel Request priority; that is, high priority is greater than 9600 bps data rate.
Byte 4, Bits 0–3	Define the line variables of this feature. Bit 0 is reserved. Bit 1 is Data Rate Select, and is set if used by either the modem or loop card. Bit 2 is Select Standby, and is set if used by either the modem or the loop card. Bit 3 is nonreturn to zero Insertion mode, and is set, if used, by the modem; for 3842, bit 3 is 0; for 3843, bit 3 is 1.
Byte 4, Bits 4–7	Define the line variables of this feature. Bit 4 is Permanent Request to Send, and is set if the communications line is nonswitched 4 wire. Bit 5 is 101.1, and is set if the modem requires support of the CCITT Circuit Number 101.1. Bit 6 is the Tone, and is set if the 8100 provides tone (for example, if the auto-answer feature is installed). Bit 7 is the Switched Line, and is set if the external modem is a switched line modem.

*For detailed information on how to build or modify a configuration table, refer to Chapter 2, CP310.

Figure CA113-3. Option Field Explanation

Example 1. FAC 11, Two-Lobe Loop, 9.6K bps, with Three 3276 Stations

0181006002130000
0251020000000000
0252020000000000
0253020000000000

Example 2. FAC 13, Data Link Attached Loop, 3842 with Two 3276 Stations

0182006000000010
0260025000000000
0370020000000000
0371020000000000

Example 3. FAC 41, BSC Secondary, Multipoint, Host Link

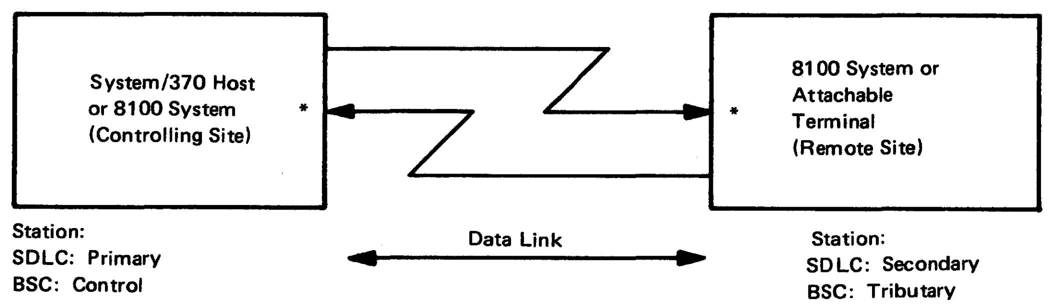
0183006120001000
0201030200000000

Figure CA113-4. Examples of Communications Configuration Table

Data Link

The data link (end-to-end teleprocessing) configuration for the 8100 System is defined as: the remote site (8100 System or an attachable terminal), the data link, and the controlling site (System/370 host or an 8100 system). See Figure CA114-1.

General 8100 Teleprocessing Network Configuration (End-to-End).



* Protection Device - Switched line only, and as required by the country serviced.
US/Canada requires: CBS Data Access Arrangement or CDT Data Coupler.
Japan requires: PDIA.
Certain E/ME/A countries require the PSNA feature for the switched integrated modem.

Figure CA114-1. Data Link Network

The 8100 network configuration depends on the number of remote stations, the data transmission speed, and the data link. The possible network configurations for the IBM 8100 System are: point-point, multipoint, and switched network.

The 8100 System operates only in half-duplex mode, which transmits data alternately in either direction. The modem transmitters may be on permanently or only during transmission.

Point-to-Point Network. The point-to-point configuration is a teleprocessing (TP) network that has a direct 2/4-wire data link (nonswitched) from a single remote station (secondary) to a host station (primary). Data transmission and reception are conducted in half-duplex mode. See Figure CA114-2.

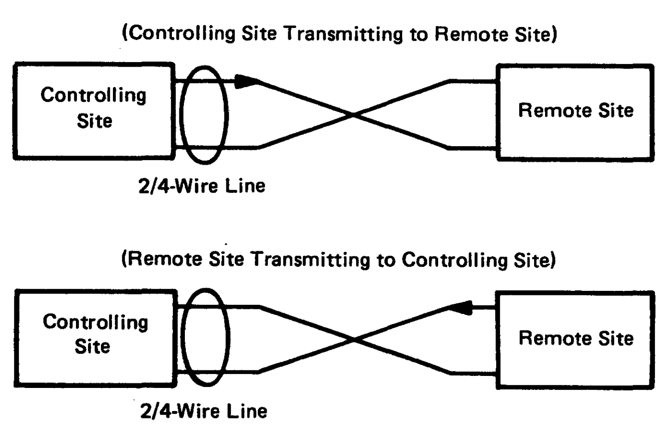


Figure CA114-2. Point-to-Point, Half-Duplex Network

Multipoint Network. The multipoint configuration is a TP network that has 2/4-wire data link (nonswitched) from a controlling site to multiple remote sites. Data transmission and reception are conducted in half-duplex mode between the controlling site and one remote site at a time. See Figure CA114-3.

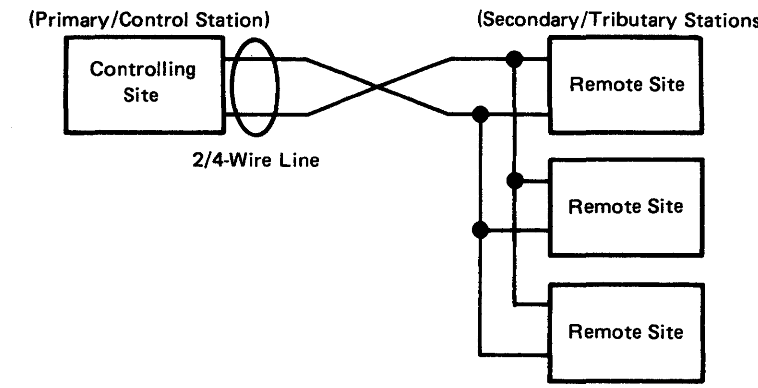


Figure CA114-3. Multipoint, Half-Duplex Network

Switched Network. The switched network configuration is a TP network that has a 2-wire data link on a common-carrier switched network; it is established by a dialing and acknowledgment procedure. Once the link is established, the configuration operates as a point-to-point configuration. In the U.S., Canada, and Japan, protective devices interface with the switched line network. Data transmission and reception are conducted in half-duplex mode. See Figure CA114-4.

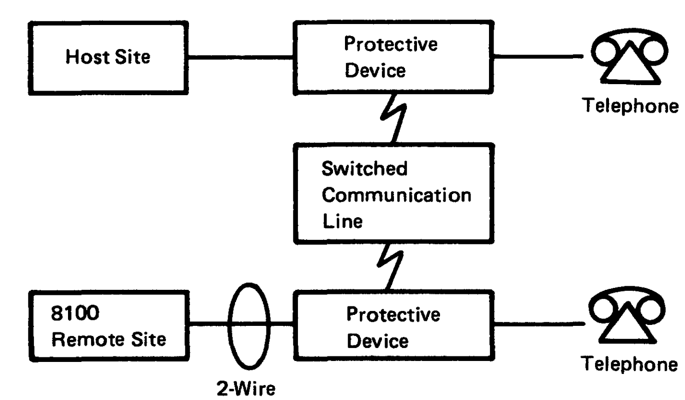
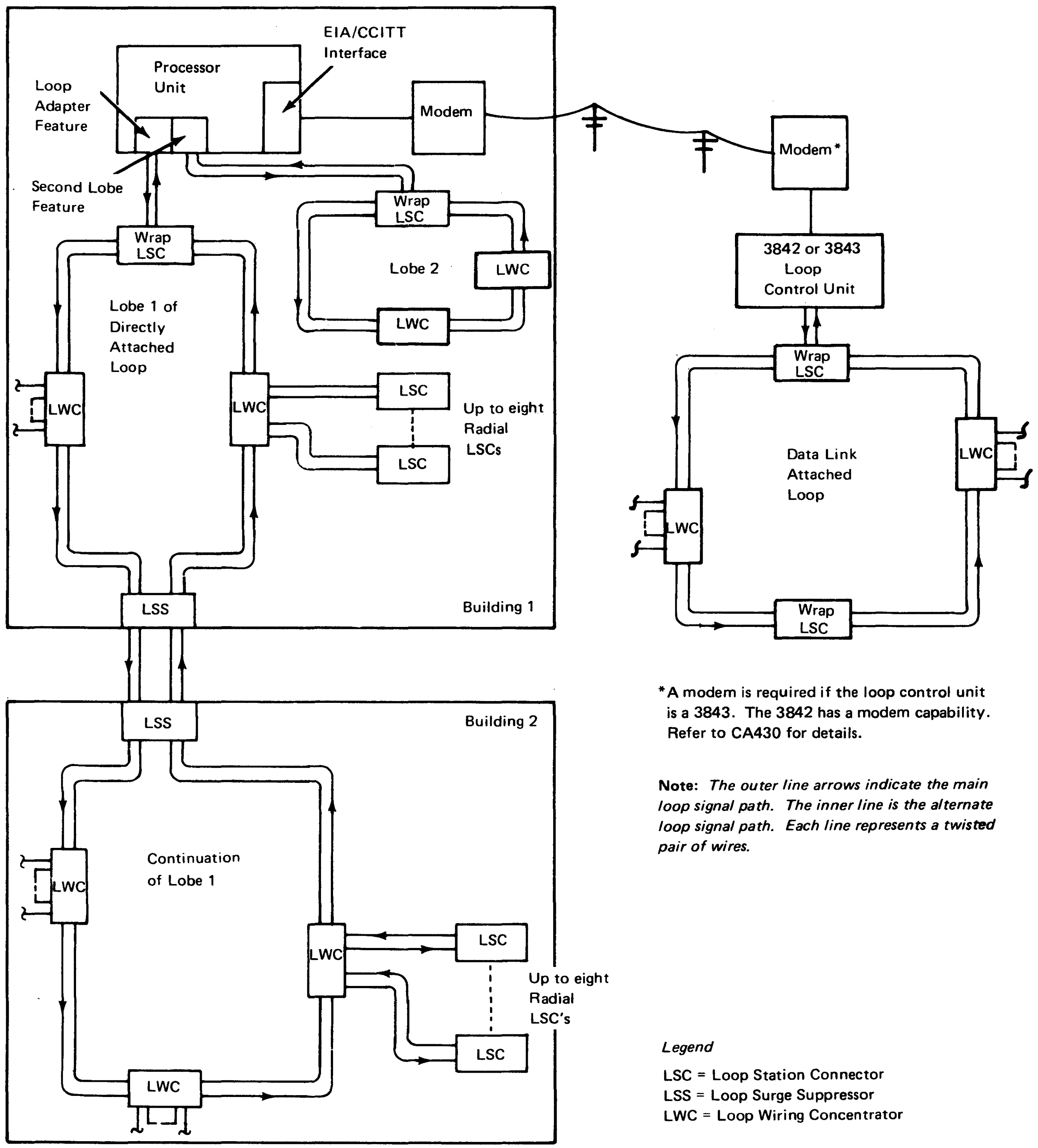


Figure CA114-4. Switched Network, Half-Duplex

Directly Attached and Data-Link Attached Loops

Figure CA114-5 shows a directly attached loop and a data-link attached loop. Although this figure shows only one data-link attached loop, loops can be data-link attached on a multipoint network.



*A modem is required if the loop control unit is a 3843. The 3842 has a modem capability. Refer to CA430 for details.

Note: *The outer line arrows indicate the main loop signal path. The inner line is the alternate loop signal path. Each line represents a twisted pair of wires.*

Legend

LSC = Loop Station Connector
LSS = Loop Surge Suppressor
LWC = Loop Wiring Concentrator

Figure CA114-5. Sample Loop Configuration

CA115 FAC Codes

Figure CA115-1 describes the feature codes, and Figure CA115-2 gives the basic characteristics of the FAC codes. The first column in Figure CA115-2 gives the regional availability of each FAC:

United States

Canada

IBM World Trade Americas/Far East Corporation (A/FE)

IBM World Trade Europe/Middle East/Africa Corporation (E/ME/A)

Japan

Though Canada is served by A/FE, it is listed separately for convenience. Those users who are not sure which corporation serves their country, should contact their IBM Marketing Representative.

Feature Code	Description
1550	CCITT V.35 (CA6) card
1601	SDLC Communications Adapter with Clock (CA1) card
1602	SDLC Communications Adapter without Clock (CA1) card
1603	BSC/S-S Communications Adapter with Clock (CA2) card
1604	BSC/S-S Communications Adapter without Clock (CA2) card
3701	EIA RS-232-C/CCITT V.24/V.28 (CA5) card
4830	Loop (CA3) card
4835	Loop Second Lobe (CA4) card
5200	Multi-speed Clock (CA10) card
5500	Integrated Modem-Nonswitched (CA8) card
5501	Integrated Modem-Switched (CA9) card
5655	CCITT X.21 (nonswitched) (CA11) card
5660	Digital Data Service (CA7) card

Figure CA115-1. Feature Code Numbers and Descriptions

FAC No.	Feature Code Numbers Required	Connection Type*	Speeds Available (BPS)	Local External Communication Equipment Required	Communication Channel Characteristics	8100 Station Type
8	1602, 4830	Loop	38.4K	Loop wire 1 lobe	SDLC protocol	
9	1602, 4830, 4835	Loop	38.4K	Loop wire 2 lobe	SDLC protocol	
10	1602, 4830	Loop	9600	Loop wire 1 lobe	SDLC protocol	
11	1602, 4830, 4835	Loop	9600	Loop wire 2 lobe	SDLC protocol	
12	1601, 3701	EIA/CCITT SDLC analog	600, 1200	External modem without clock	Point-to-point, switched, 2-wire to Sys/370 only. Point-to-point, nonswitched, 2- or 4-wire. Multi-point, nonswitched, 4-wire.	Secondary Primary & Secondary Primary & Secondary
13 All	1602, 3701	EIA/CCITT SDLC analog	2000, 2400, 4800, 7200, 9600	External modem with clock	Point-to-point, switched, 2-wire with auto ans to Sys/370-3704/05 (U.S., CANADA & A/FE is 4800 bps, EMEA is 9600 bps). Point-to-point, nonswitched, 2- or 4-wire. Multi-point, nonswitched, 4-wire.	Secondary Primary & Secondary Primary & Secondary
13 E/ME/A	1602, 3701	EIA/CCITT SDLC digital	2000, 2400, 4800, 7200, 9600	External data communication equipment with clock	Point-to-point, nonswitched, 2- or 4-wire. Multi-point, nonswitched, 4-wire.	Primary & Secondary Primary & Secondary
15 All	1601, 3701	EIA/CCITT SDLC direct connect	600, 1200, 2400	None	Point-to-point, nonswitched, maximum distance 12.1 meters (40 feet). **Note:** *Attached secondary station (8100 or terminal) must not provide clock.*	Primary
16 All	1602, 3701, 5200	EIA/CCITT SDLC direct connect	4800, 9600	None	Point-to-point, maximum distance 12.1 m (40 ft). **Note:** *Attached secondary station (8100 or terminal) must not provide clock.*	Primary
17 All	1602, 3701	EIA/CCITT SDLC direct connect	2000, 2400, 4800, 7200, 9600	None	Point-to-point, nonswitched maximum distance 12.1 m (40 ft). **Note:** *Attached primary station (8100) must provide clock.*	Secondary
18 U.S. CANADA	1601, 5500	EIA SDLC analog	600, 1200	WE type CDT DAA or equivalent for voice command	Point-to-point, nonswitched, 2- or 4-wire. Multi-point, nonswitched, 4-wire.	Primary & Secondary Primary & Secondary
18 A/FE E/ME/A	1601, 5500	EIA/CCITT SDLC analog	600, 1200	None	Point-to-point, nonswitched, 2- or 4-wire. Multi-point, nonswitched, 4-wire.	Primary & Secondary Primary & Secondary

Figure CA115-2 (Part 1 of 2). FAC Chart

FAC No.	Feature Code Numbers Required	Connection Type*	Speeds Available (BPS)	Local External Communication Equipment Required	Communication Channel Characteristics	8100 Station Type
19 U.S. Canada	1601, 5501 with auto answer	EIA SDLC analog	600, 1200	WE type CBS data coupler series 5 or later or equivalent for automatic & manual answer	Point-to-point, switched 2-wire to 3704/05 only.	Secondary
19 A/FE E/ME/A	1601, 5501 with auto answer public switched network adapter (EMEA)	EIA/CCITT SDLC analog	600, 1200	None	Point-to-point, switched, 2-wire to 3704/05 only.	Secondary
20 U.S. Canada	1602, 5660	Digital data service network	2400, 4800, 9600	AT & T Channel Service Unit	Point-to-point, nonswitched, 4-wire. Multi-point, nonswitched, 4-wire.	Primary & Secondary Primary & Secondary
21 U.S. Canada	1602, 5660 (only 8140 and attached 8101s)	Digital data service network	56000	AT & T Channel Service Unit	Point-to-point, nonswitched, 4-wire. Multi-point, nonswitched, 4-wire. **Note:** *Both require 3705 at Sys/370.*	Secondary Secondary
24 All	1601, 1550	CCITT V.35 direct connect	600, 1200, 2400	None	Point-to-point, nonswitched, maximum distance 304.8 m (1000 ft). **Note:** *To another 8100 only, and not Sys/370.*	Primary
25 All	1550, 1602, 5200	CCITT V.35 direct connect	4800, 9600	None	Point-to-point, nonswitched, maximum distance 304.8 (1000 ft.) **Note:** *To another 8100 only, and not Sys/370.*	Primary
26 All	1550, 1602, 5200 (only 8140 and attached 8101s)	CCITT V.35 direct connect	56,000	None	Point-to-point, nonswitched, maximum distance 304.8 m (1000 ft.) or up to a total cable length of 200 ft. to a 3705.	Primary & Secondary
27 All	1550, 1602	CCITT V.35 direct connect	2000, 2400, 4800, 7200, 9600	None	Point-to-point, nonswitched maximum distance 304.8 m (1000 ft.) **Note:** *To another 8100 with clock.*	Secondary
28 All	1550, 1602 (only 8140 and attached 8101s)	CCITT V.35 direct connect	56,000	None	Point-to-point, nonswitched, maximum distance 304.8 m (1000 ft.). **Note:** *To another 8100 with clock.*	Primary & Secondary
29 U.S. Canada	1550, 1602 (only 8140 and attached 8101s)	CCITT V.35 SDLC	56000	External modem with clock	Point-to-point, nonswitched	Secondary
29 A/FE E/ME/A	1550, 1602 (only 8140 and attached 8101s)	CCITT V.35 SDLC	48000	External modem with clock	Point-to-point, nonswitched	Secondary
A1 (RPQ 870892)	1550, 1602, 5200	CCITT V.35 direct connect	19.2 Kbps	None	Point-to-point, nonswitched maximum distance 304.8 m (1000 ft.). **Note:** *To a 3777.*	Primary
30 Japan	1602, 5655	CCITT X.21 SDLC Digital	2400, 4800, 9600	External data communication equipment with clock	Point-to-point, nonswitched, 4-wire. Multi-point, nonswitched, 4-wire.	Primary & Secondary Primary & Secondary
31 Japan	1602, 5655 (only 8140 and attached 8101s)	CCITT X.21 SDLC Digital	48,000	External data communication equipment with clock	Point-to-point, nonswitched, 4-wire.	Primary & Secondary
40 All	1603, 3701	EIA/CCITT BSC analog	600, 1200	External modem without clock	Point-to-point, nonswitched, 2- or 4- wire. Point-to-point, nonswitched, 4-wire.	Primary & Secondary Primary & Secondary

FAC No.	Feature Code Numbers Required	Connection Type*	Speeds Available (BPS)	Local External Communication Equipment Required	Communication Channel Characteristics	8100 Station Type
41 All	1604, 3701	EIA/CCITT BSC analog	2000, 2400, 4800, 7200, 9600	External modem with clock	Point-to-point, nonswitched, 2- or 4-wire. Multi-point, nonswitched, 4-wire.	Primary & Secondary Primary & Secondary
43 All	1603, 3701	EIA/CCITT BSC direct connect	600, 1200,	None	Point-to-point, nonswitched, maximum distance 12.1 m (40 ft). **Note:** *Attached terminal must not provide clock.*	Primary
44 All	1604, 3701, 5200	EIA/CCITT BSC direct connect	2400, 4800, 9600	None	Point-to-point, nonswitched, maximum distance 12.1 m (40 ft). **Note:** *Attached terminal must not provide clock.*	Primary
45 U.S. Canada	1603, 5500	EIA BSC analog	600, 1200	WE type CDT DAA or equivalent for voice command	Point-to-point, nonswitched, 2- or 4-wire. Multi-point, nonswitched, 4-wire.	Primary & Secondary Primary & Secondary
45 A/FE E/ME/A	1603, 5500 with surge prot available	EIA/CCITT BSC analog	600, 1200	None	Point-to-point, nonswitched, 2- or 4-wire. Multi-point, nonswitched, 4-wire.	Primary & Secondary Primary & Secondary
47 U.S. Canada	1604, 5650 or 5651	Digital data service network	2400, 4800, 9600	AT & T Channel Service Unit	Point-to-point, nonswitched. Multi-point, nonswitched.	Primary & Secondary Primary & Secondary
60 U.S. Canada	1603, 3701 **Note:** *600 bps not available with 8130 or 8101 attached to an 8130.*	EAI S/S analog	110, 134.5, 150, 300, 600	External modem without clock	Point-to-point, nonswitched, 2- or 4-wire.	Primary
60 A/FE E/ME/A	1603, 3701 **Note:** *600 bps not available with 8130 or 8101 attached to an 8130.*	EIA/CCITT S/S analog	110, 134.5, 150, 300, 600	External modem without clock	Point-to-point, nonswitched, 2- or 4-wire.	Primary
61 All	1603, 3701 **Note:** *600 bps not available with 8130 or 8101 attached to an 8130.*	EIA/CCITT S/S direct connect	110, 134.5 150, 300, 600	None	Point-to-point, nonswitched, maximum distance 12.1 meters (40 feet).	Primary

*The interface types used are:

- EIA RS-232-C in the United States.
- EIA RS-232-C/CCITT V.24/V.28 in countries serviced by A/FE.
- CCITT V.24/V.28 and CCITT X.21 bis/V.28 in countries serviced by E/ME/A.

Figure CA115-2 (Part 2 of 2). FAC Chart

CA116 Port Addressing and Interrupt Levels

Port numbers determine (1) a part of the I/O address of the associated communications adapter card (SDLC or BSC/S-S), and (2) the position assigned to this adapter card in a programmable interrupt array. The program writes into this array position the primary and secondary interrupt levels assigned to the adapter card.

I/O address bits are:

0–3 = The I/O group address

4–7 = Determined by the port position

The I/O group address (bits 0–3) identifies the I/O group where the communication adapter card resides. Each I/O group has a fixed address that is set in the SCF address selection switches at manufacturing time. For more information on the System Control Facility (SCF), refer to the 8130 or 8140 Processor description manual, GA27-3196 and GA27-2880, respectively.

Figure CA116-1 shows the relationship between port numbers, the communications adapter card address, and the interrupt translate array position assigned to the adapter card.

Mach Type	Port No.	Communications Physical Address (PA) in Hex				Translate Array Position
8130	1	81				1
**	2	82				2
	3	83				3
	4	84				4
	5	85				5
	6	86				6
8140	1	81				1
Models	2	82				2
AXX	3	83				3
8140	1	80				0
Models	2	81				1
BXX	3	82				2
	4	83				3
	5	50				0
	6	51				1
	7	52				2
	8	53				3
	9	5C				4
	10	5D				5
	11	5E				6
	12	5F				7
8101		8101 Position*				
		1st	2nd	3rd	4th	
	1	10	20	30	40	0
	2	11	21	31	41	1
	3	12	22	32	42	2
	4	13	23	33	43	3
	5	1C	2C	3C	4C	4
	6	1D	2D	3D	4D	5
	7	1E	2E	3E	4E	6
	8	1F	2F	3F	4F	7

*8101 positions are determined by specify codes as follows:

Position 1: 9921

Position 2: 9922

Position 3: 9923

Position 4: 9924

**Feature Expansion Type 1 is required for the 8130 to have ports 3, 4, 5, 6. Also, the System Expansion feature is required for the SDLC and BSC/S-S adapters in an 8130 to have programmable interrupt levels, and for 8101s to be attachable to the 8130.

Figure CA116-1. Port Number, Adapter Addresses, and Translate Array Position by Machine Type

CA120 Basic Operational Description

CA121 Loop Operation

A loop consists of cabling and accessories that allow I/O devices to be attached to a system. A loop attaches to the IBM 8100 Information System in one of two ways (see Figure CA114-5):

1. It can be attached directly either to an 8130 or 8140 Processor using the Loop Adapter feature or to an 8101 Storage and I/O Unit.
2. It can be attached via an IBM 3842 Loop Control Unit or 3843 Loop Control Unit, which communicates with the 8100 Information System over a nonswitched communication line.

Complete configuration details for the loop are shown in the *IBM 8100 Information System Configurator,* GA27-2876.

In addition to allowing a wide variety of devices to be attached, the loop design provides for error recovery and problem determination. A wrap capability allows an alternate path to be used to channel the signal around a wiring failure on the loop; the bypass capability allows a failing device to be electrically removed from the loop signal path while allowing the remainder of the loop to operate normally.

Loop Components

The following loop components are the cables and accessories needed to attach the devices to the cable and the accessories needed to connect cables together:

Loop cable (indoor or outdoor)

Loop splice plate (LSP)

Radial and wrap loop station connectors (LSCs)

Loop wiring concentrator (LWC)

Loop surge suppressor (LSS)

Additional components are:

Electrical outlet boxes

Bushings

Conduit adapters

Cable clamps

Electrical enclosure boxes

Ferrule termination for cable

Loop Cable. The loop requires shielded two-twisted-pair (22 AWG) cable. Three types of cable can be ordered from IBM: indoor, outdoor aerial, and outdoor burial. Detailed specifications for the cable are contained in the *IBM Multiuse Communications Loop Planning Guide*, GA23-0038.

Outdoor cable length must be continuous. No procedure is included for splicing outdoor cable.

Loop Splice Plate (LSP). The LSP splices together two segments of indoor cable or provides a connecting point for future expansion of the loop. The LSP consists of a single connector strip (bonded to the cover of the LSP), to which the incoming loop cable and the outgoing loop cable can be attached. It is installed in a conventional outlet box for business office environments or an environmental outlet box for industrial environments.

Loop Station Connector (LSC). Two types of LSC are available: wrap and radial. The wrap LSC attaches a device or a controlling unit directly to the main loop cable; the radial LSC attaches a device through an LWC to the loop. The wrap LSC attaches an incoming and outgoing loop cable; the radial LSC attaches at the end of one loop cable from the LWC (see Figure CA121-1).

The wrap LSC also offers the isolation feature of wrapping. Using the switches on the face of the LSC, the customer can wrap the loop away from a loop wiring failure or can reconfigure the loop during facility alterations. Both wrap and radial LSCs contain relays that channel the signal path away from an attached device and keep the loop cable intact when the device is powered off or disconnected from the LSC. These LSCs are installed in a conventional or environmental outlet box. Normally, the wrap LSC is used when there is insufficient terminal clustering to justify use of the LWC.

Loop Wiring Concentrator (LWC). The LWC allows a cluster of devices to be attached without a large number of drops on the loop cable. It attaches up to eight radial LSCs at the end of loop cables. The point at which a radial line terminates at the LWC is called an LWC port. Not all ports have to be used; unused ports may be reserved for future expansion.

The LWC has the same wrapping capability as the wrap LSC. In addition, the LWC allows the customer to bypass one or more of the radials by setting a corresponding bypass switch located inside the LWC.

The LWC provides an enclosure for normal business office environment.

Loop Surge Suppressor (LSS). The LSS allows the loop to be run outdoors. It attaches two outdoor cables to two indoor cables and provides the proper termination and grounding for each type of cable. The LSS contains four surge suppressors, one for each twisted pair used in the two outdoor cables, to protect against voltage surges caused by near strikes of lightning. There is no protection in the LSS against a direct lightning strike.

The LSS provides an enclosure for normal business office environment.

Environmental Equipment Cabinet for LWC and LSS

If the LWC or LSS are to be installed in locations with harsh or contaminated environments or with high humidities, a NEMA Class 4 environmental equipment cabinet suitable for that environment should be used. The cabinet should also be used if conduit must be directly connected to either accessory. The covers shipped as part of the LWC or LSS do not offer adequate protection for long term operation in contaminated environments. The covers also do not allow for direct conduit connection. An environmental equipment cabinet is available from IBM for harsh or contaminated environments with high humidity.

The NEMA-4X cabinet (environmental equipment cabinet) is a watertight, dusttight, and corrosion-resistant non-ventilated enclosure intended for use indoors or outdoors to protect the enclosed equipment against splashing water, seepage of water, falling of hose-directed water, and severe external condensation. The cabinet is sleet resistant but not ice proof. It has conduit-sealing locknuts or equivalent provision for watertight connection at the conduit entrance and mounting means external to the equipment cavity.

The NEMA-4X cabinet is normally available in the United States and Canada from local suppliers. For convenience, IBM also has available for countries other than United States and Canada an environmental equipment cabinet that meets NEMA Class 4 requirements. The hinged cover cabinet, companion internal mounting plate with environmental cable clamps and sealing locknuts, provide adequate protection for the LWC or LSS when installed in contaminated environments.

Sample Configuration

Figure CA114-5, a sample configuration of the 8100 Information System, shows possible loop arrangements and all of the loop accessories except the LSP.

Loop Concepts

The following loop concepts are essential to the understanding of the loop:

- Loop signal path
- Lobes
- Wrapping
- Bypassing
- Information Rates

Loop Signal Path. The loop uses a cable consisting of shielded two-twisted-pair wiring for all operations. This cable provides two independent signal paths between the main loop LWCs or wrap LSCs. One path is used normally; the other is provided as backup for failures or alterations of the loop wiring or of the facilities through which the wire is routed.

The same type of wire is also used for the LWC radial cables. However, in these cables both pairs of wires are required for normal operation. Figure CA121-1 shows the normal loop signal path.

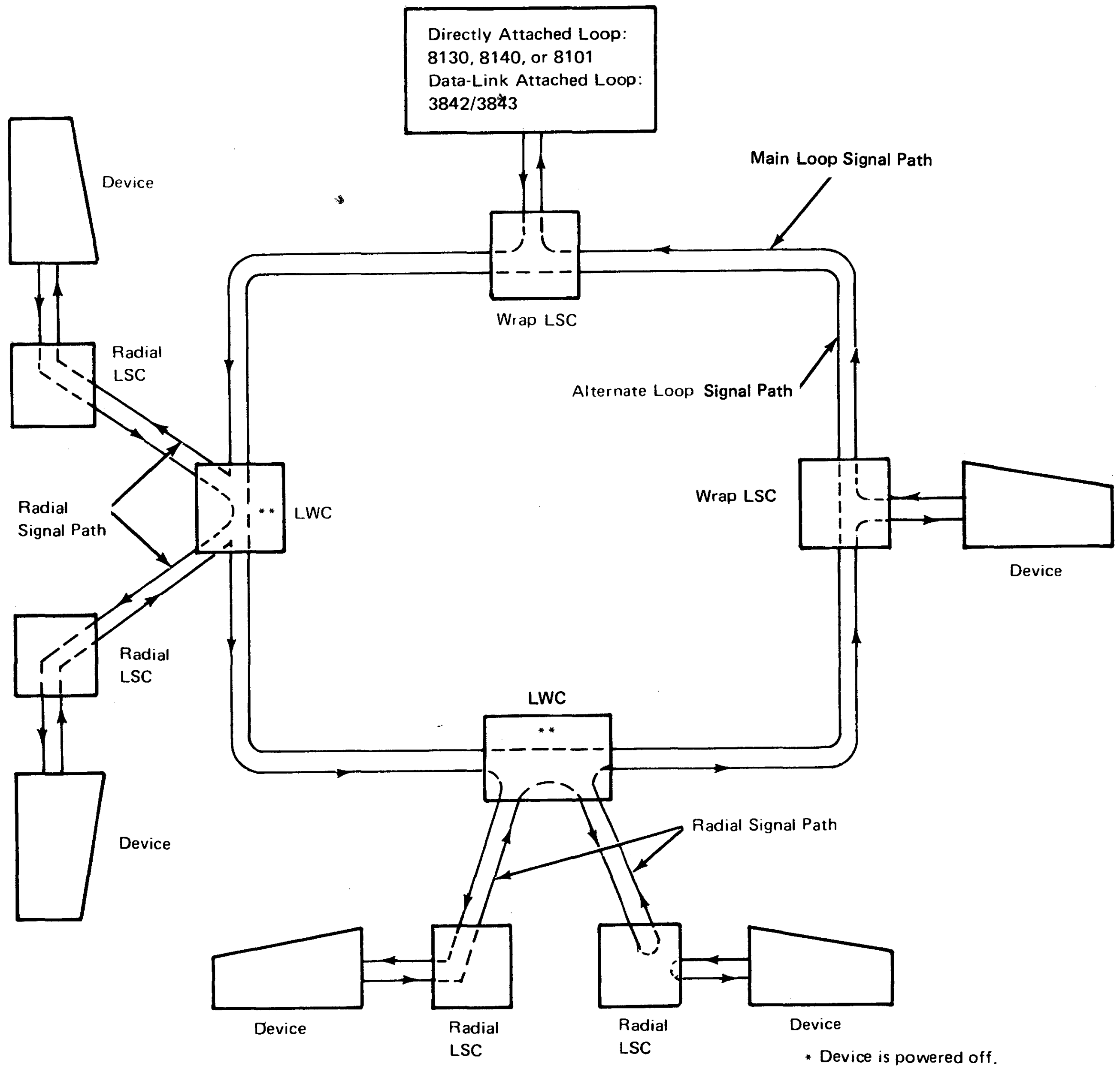
Lobes. For directly attached loops, the loop can be divided into two portions, called lobes. Each lobe is a separate physical cable loop. The two lobes are interconnected within the controlling unit to form one logical loop. Figure CA121-2 illustrates the two lobes and interconnection in the controlling unit. If a disruption occurs on one of the lobes, operations can be resumed on the good lobe after the disrupting lobe has been bypassed at the controlling unit.

Dividing a single loop into lobes also allows the cable length of the loop to be doubled, thus enabling the loop to service a larger area.

Data link attached loops cannot be divided. Only one lobe can be attached to a 3842 or 3843 Loop Control Unit.

Wrapping. When a wiring failure (open, short, or ground) occurs on the loop, the loop signal path is interrupted. To recover from the failure, the wrap LSC and the LWC can be used to switch the main loop signal path to the alternate signal path in the loop cable. When the failure is located, the customer can set switches on the nearest wrap LSC or LWC on each side of the wiring failure to use the second set of twisted-pair wiring in the cable as an alternate signal path to eliminate the broken wire. Wrap switches are also used when altering the business office environment or changing the loop system configuration. The section of the loop being altered is electrically removed from the loop, permitting alterations to the business office environment to be made without disrupting operations.

Bypassing. When devices are attached through radial LSCs to an LWC, *the wire from the LSC to the LWC* can be electrically disconnected without physically removing the wire. The LWC allows the customer to set switches to bypass one or more of the radials attached to the LWC, causing only momentary interruption of the loop operation when the switch is thrown. When the radial LSC is to be reconnected to the loop through the LWC, the customer resets the switch to return the radial LSC to the loop signal path.



Legend

LSC = Loop Station Connector
LWC = Loop Wire Concentrator
——► = Twisted Pair

Figure CA121-1. Loop Signal Paths (Not Wrapped)

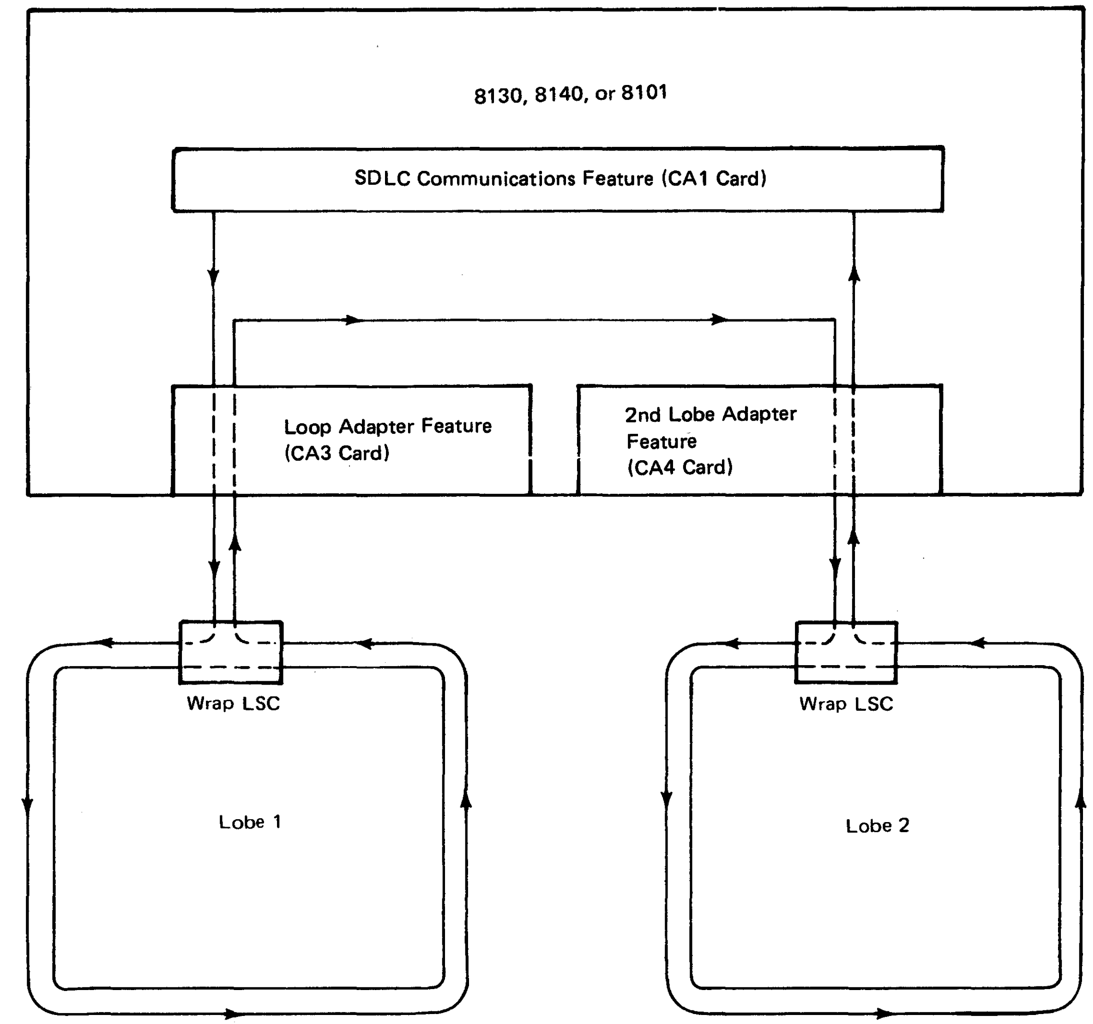


Figure CA121-2. Two-Lobe Signal Paths

Information Rates. The directly attached loop can be operated at bit rates of: 38.4 or 9.6 thousand bits per second (K bps). The data link attached loop can be operated at 2.4K or 1.2K bps with a 3842 and up to 9.6K bps with a 3843. Selection is made at the controlling units and all attachable devices.

Both lobes of one loop must be set to operate at the same bit rate in the controlling unit. All related devices must also be set to the same rate.

The bit rate is a major consideration when planning the lobe configuration limits. When planning the data link attached loop at 2.4K or 1.2K bps, the layout constraints for the 9.6K bps loop apply.

Loop Accessory Operation

Minimum manual intervention is normally required for operation of the loop accessories. Accessory switches that can be used for test and isolation of loop problems are described in this section.

Wrap Loop Station Connector (LSC). On the front of the wrap LSC are two indicators and two keyholes to set and restore the wrap state of the loop at that LSC. The key-actuated wrap switches provide protection from inadvertent operation.

To gain access to these wrap switches, swing the switch cover in the direction of the arrow on the cover until the keyholes and indicators are accessible. Then check the indicator holes to determine the condition of the wrap switches. If both holes display the color black, the LCS is in a normal state, no wrapping. If one of the indicators display the color white, the LCS is wrapped in that direction. If both switches are in the wrapped position (both indicators displaying the color white), the device connected to that LSC will not operate on the loop.

To wrap the loop at the LSC, insert the key into the upper keyhole and turn the key in the direction in which the loop is to be wrapped. The corresponding indicator hole will display the color white.

To restore the system to a normal (not-wrapped state) insert the key into the restore (lower) keyhole and turn it toward the indicator displaying the color white, until the indicator color is black. Now the LSC is in a normal (not-wrapped) condition.

Loop Wiring Concentrator (LWC). The LWC has a switch panel behind a door at the lower center of the unit. This panel contains wrap switches for the LWC and bypass switches for each of the eight ports to which a radial loop cable can be attached. To gain access to the switches, push the black door in and up and then insert the key in the keyhole at the edge of the inner door and turn in the direction of the arrow.

To wrap the LWC, move the appropriate wrap switch on the panel to the position indicating a wrap state, switch pointing up. To restore the LWC to its normal state, return the switch to the not-wrapped position, switch pointing down.

To bypass one of the radial lines from the LWC, move the switch corresponding to that radial port on the LWC to the left (bypassed) position. In this position, the radial cable and LSC are disconnected from the loop. When the radial line is to be reconnected to the loop, move the corresponding bypass switch to the right (not-bypassed) position. In this position, the device attached to the radial line is considered part of the loop and can send and receive signals on the loop. Any number of radial lines can be bypassed in the same manner.

Note: *Any unused radial ports must be bypassed (the corresponding switch must be in bypass position).*

Loop Surge Suppressor (LSS). The LSS has a jumper assembly located just above the lower terminal block. The jumper assembly is used for testing purposes.

CA122 Data Link Operation

Data Link

A data link consists of the physical connection and the connection protocols (SDLC, BSC, or S/S) for the transfer of data between two locations. The physical connection contains data terminal equipment (DTE) data circuits, cables, data circuit-terminating equipment (DCE), and the communication line. A data link attaches to the IBM 8100 Information System in two ways:

1. Direct connection to an 8130 Processor, an 8140 Processor, or an 8101 Storage and I/O Unit.
2. Attachment through data circuit-terminating equipment (DCE).

Figures CA122-1 and CA122-2 show the basic data link configurations. Figure CA122-3 shows SDLC operations, Figures CA122-4 and CA122-5 show BSC operations, and Figures CA122-6 and CA122-7 show Start/Stop operations. Refer to CA110 for configuration descriptions regarding line disciplines, bit rates, and types. Complete configuration details for data link are shown in the *IBM 8100 Information System Configurator*, GA27-2876.

Data Link Components

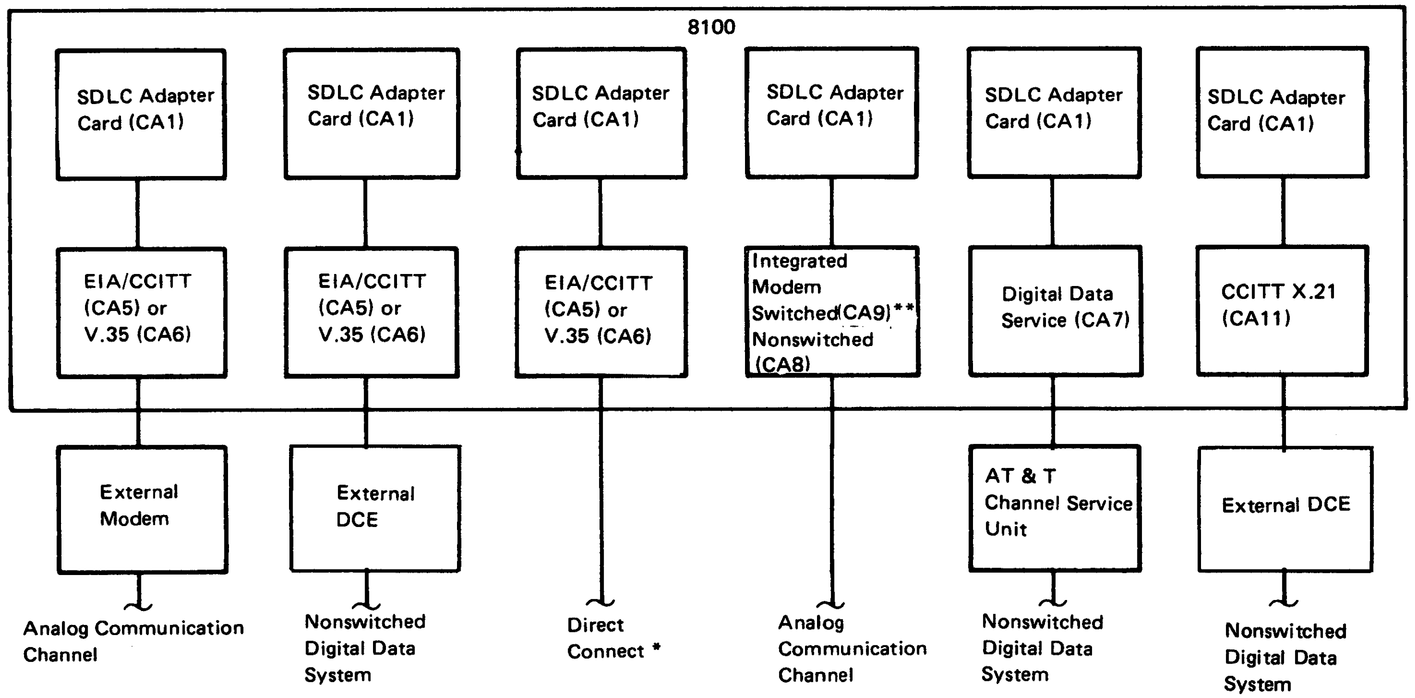
Data link components are configuration-dependent and consist of:

- External cable (standard)
- External cable (direct connect)
- Modem or other DCE
- Data circuit (leased, switched, private)

Equivalent components at the remote location provide a complete system.

Testing

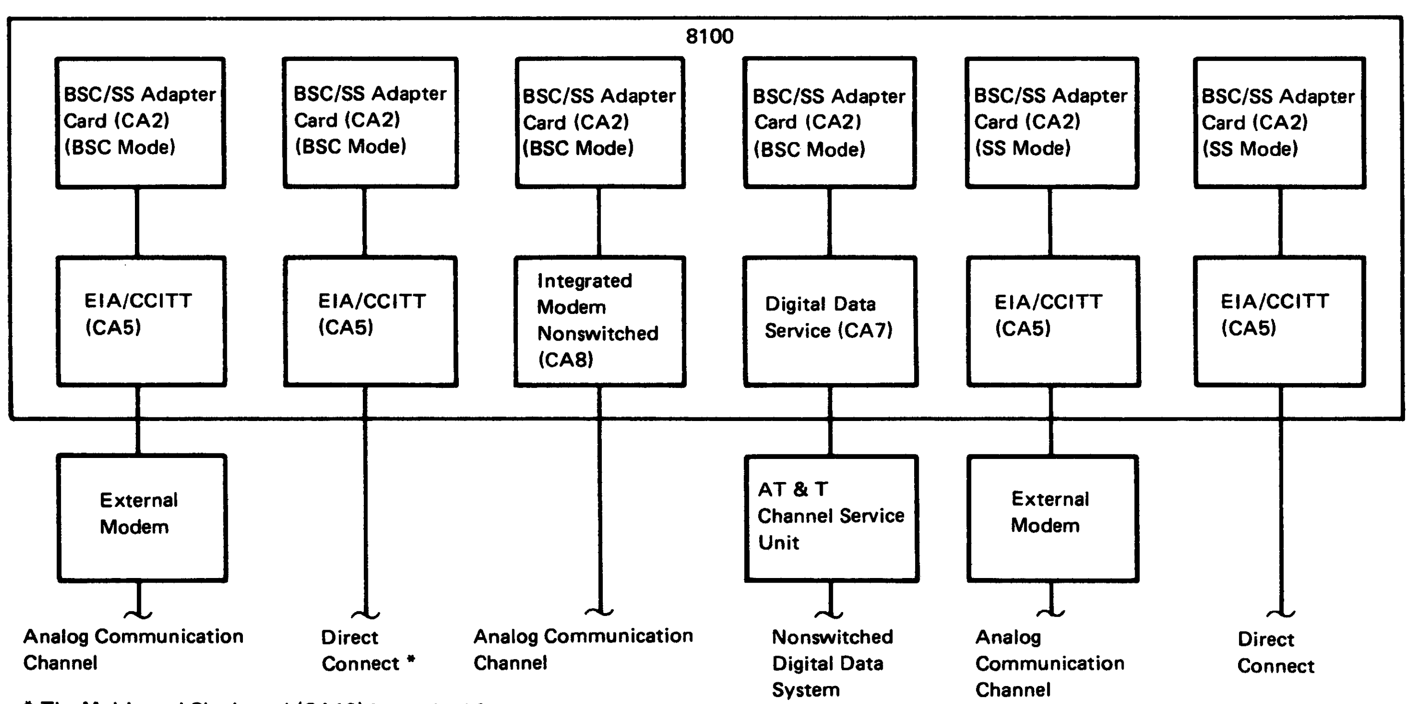
Testing is performed in a sequential manner, starting from the 8100 hardware outbound to where link-level testing and line monitoring is required. Customer problem determination makes use of the hardware wrap capability (wrap plugs and external wrappable cables) and wrap tests which are also used by the service representative in fault isolation.



*The Multispeed Clock card (CA10) is required for direct connect at 4800 bps and 9600 bps.

** For switched operation in the U.S. and Canada, a W.E. Type CBS Automatic Data Coupler, Series 5 or later, or equivalent, is required. In other countries, the IBM Public Switched Network Adapter (PSNA) feature is required.

Figure CA122-1. SDLC Data Link Configurations



* The Multispeed Clock card (CA10) is required for direct connect at 4800 bps and 9600 bps.

Figure CA122-2. BSC and S-S Data Link Configurations

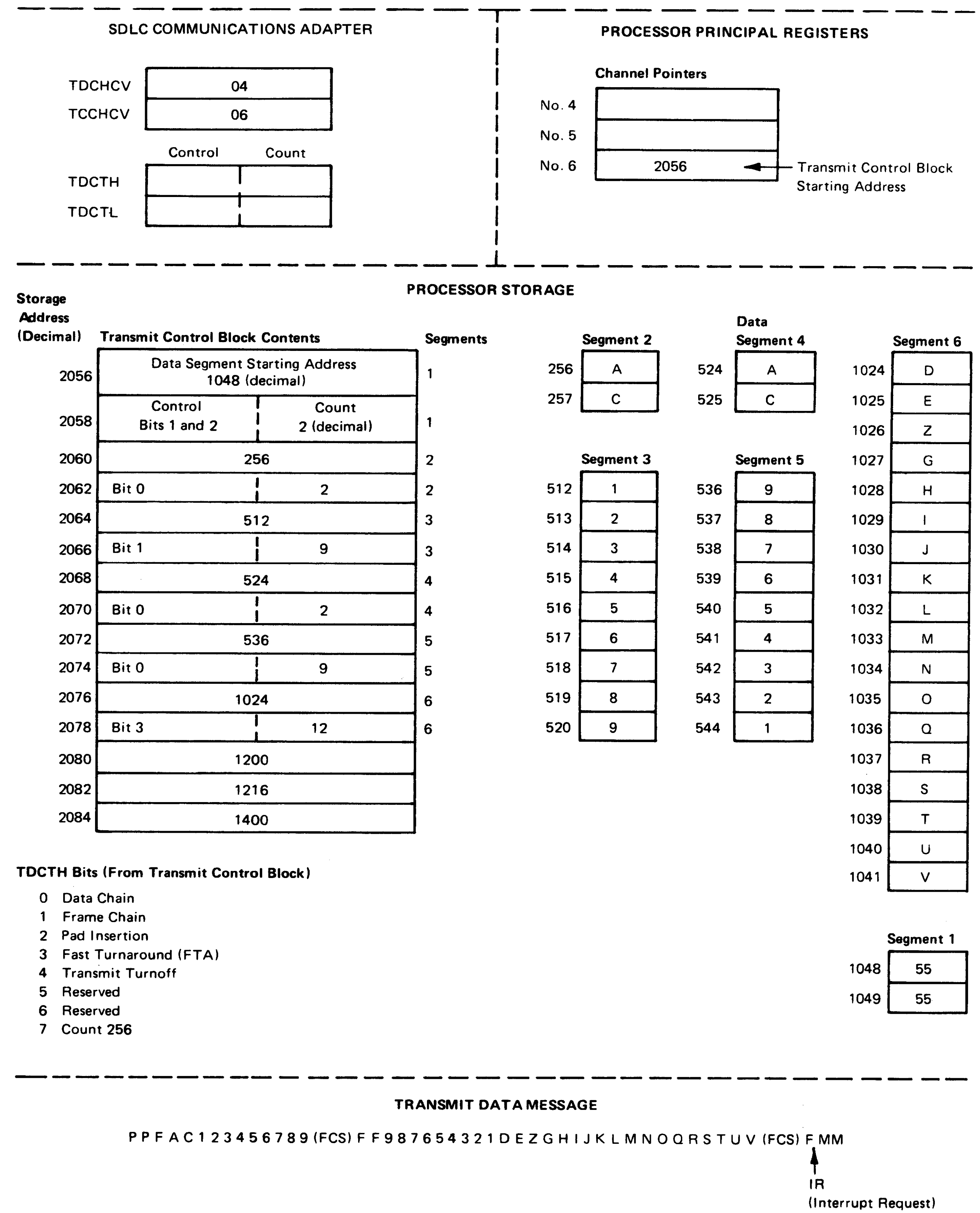


Figure CA122-3 (Part 1 of 4). SDLC Operation

SDLC COMMUNICATIONS ADAPTER

RDCHCV	04	
RCCHCV	06	
	Control	Count
RDCTH		
RDCTL		

PROCESSOR PRINCIPAL REGISTERS

Channel Pointers

No. 4	An address in buffer A
No. 5	An address in buffer B
No. 6	An address in receive control block

PROCESSOR STORAGE

Storage Address (Decimal)	Receive Control Block Contents: Control	Count†	
1400	Bits 0, 2, and 6	3	← IR A
1402	Bit 0	0	← IR B, Buffer Swap A → B
1404	Bits 0 and 3	0	← IR C, Buffer Swap B → A
1406	Bits 0, 2, and 6	4	← IR D
1408			
1410			
•			
•			
•			
1422			

	Receive Buffer A		Receive Buffer B
1200	A (L)	1216	8
1201	C (M)	1217	7
1202	1 (N)	1218	6
1203	2 (O)	1219	5
1204	3 (Q)	1220	4
1205	4 (R)	1221	3
1206	5 (S)	1222	2
1207	6 (T)	1223	1
1208	7 (U)	1224	D
1209	8 (V)	1225	E
1210	9 (FCS)	1226	Z
1211	FCS (FCS)	1227	G
1212	FCS	1228	H
1213	A	1229	I
1214	C	1230	J
1215	9	1231	K

RDCTH Bits (To Receive Control Block)

0 Valid Entry
1 Invalid Sequence
2 FCS Valid
3 Receive Buffer Entry (A = 0, B = 1)
4 Byte Overrun
5 Buffer Overrun
6 Flag Received
7 Count 256

† Count is number of unused locations of buffer in use.

RECEIVE DATA MESSAGE

P P F A C 1 2 3 4 5 6 7 8 9 (FCS) F F A C 9 8 7 6 5 4 3 2 1 D E Z G H I J K L M N O Q R S T U V (FCS) F MM

IR A   IR B   IR C   IR D   IR E

Figure CA122-3 (Part 2 of 4). SDLC Operation

Supervisory Program (Includes Interrupt Handling)	SDLC Program Module: Functions / Commands	Command Code (Hex)	Data/ Mask (Hex)	SDLC Adapter
Open Function Request →				
	Place SDLC Control Logic in known state. Device reset	02	Data byte has no effect	
	Enable control logic to make interrupt requests and channel requests. Set Basic Status	06	02	→ BSTAT bit 6 turns on.
	Establish length of Receive Data Buffers A and B (both of same length) in processor storage. Write Receive Buffer Length (W RBLNG)	B0	10	→ The desired length is placed in the RBLNG register.
	Make control logic aware that channel pointer 6 is being used for CHIOs involving control information (transmit and receive). Write Transmit Control Channel Control Vector (W TCCHCV)	40	06	→ The channel pointer number is placed in TCCHV bits 2–6. Bits 0 and 1 are hardware-controlled.
	Write Receive Control Channel Control Vector (W RCCHCV)	C8	86	→ The channel pointer number is placed in RCCHCV bits 2–6. Bits 0 and 1 fixed at 1 and 0, respectively.
	Program initializes channel pointer 6 to contain decimal 2056, first address of transmit control block.			
	Make control logic aware that channel pointer 4 will point to current transmit data buffer, and that channel pointers 4 and 5 will point to receive data buffers A and B, respectively. Write Transmit Data Channel Control Vector (W TDCHCV)	30	04	→ The channel pointer number is placed in TDCHCV bits 2–6. Bits 0 and 1 are hardware-controlled.
	Write Receive Data Channel Control Vector (W RDCHCV)	A8	84	→ The channel pointer number is placed in RDCHCV bits 2–6. Bit 6 initially set to 0 for channel pointer 4 (Buffer A). After that, it is hardware-controlled. Bits 0 and 1 are fixed at 1 and 0, respectively.
	Make control logic aware of its specific station address. Assume system requires that it have this address. Write Specific Address Decode Register (W SADDR)	98	X	→ Address defined by data byte is placed in SADDR.
	Initialize receive control registers. Reset Data Channel Counter (RS DCT)	B8	No effect	→ RDCTH bits 0–6 reset to off, and receive data length counter (RDCTH bit 7 and RDCTL bits 0–7) set to value in RBLNG.

Supervisory Program (Includes Interrupt Handling)	SDLC Program Module: Functions / Commands	Command Code (Hex)	Data/ Mask (Hex)	SDLC Adapter
	Initialize DCE/loop adapter control. Set DCE Control Register (S MCTRL)	D8	83	DTR bit is set and modem interrupts are disabled.
	Program waits for DSR. At appropriate times it reads DCE status. Read DCE Status (R MSTAT)	D9	No effect	MSTAT is sent back to a register of a processor primary register set.
Write Function Request	Set Transmit Mode Set Transmit Control Register (S TCTRL)	08	80	TCTRL bit 0 (Transmit Mode) turns on.
	Program builds entries for half-word transmit control block starting at location 2056 decimal.			
	Program clears Valid Entry (bit 0) in each halfword location of the receive control block starting at location 1400 decimal.			
	Prepare for events at Fast Turnaround (FTA) time: Activate Buffer A Valid, Buffer B Valid, and Enable Fifteen 1's bits in RCTRL. Set Receive Control Register (S RCTRL)	88	61	RCTRL bits 1, 2, and 7 are turned on.
	Write length of receive control block. Write Receive Control Counter (W RCCNT)	D0	03	Turn on bits 6 and 7 of RCCNT (12 halfwords).
	Turn on Control Valid bit in the TCTRL register to start CHIO operations for message transmission. Set TCTRL	08	40	Turns on Control Valid (bit 1) in TCTRL. Transmission of message data from each of the separated storage buffers is preceded by CHIO operations which (1) transfer the initial address of the storage buffer from the transmit control block to the transmit channel pointer (No. 4), and (2) transfer the control and count information from the next control block location to the TDCTH and TDCTL registers. (The transmit control channel pointer (No. 6) is now stepped by 2 in preparation for transmission from the next buffer segment.) Then, CHIO operations transfer the message, a byte at a time, from the storage buffer segment to the control logic where it is serialized and put on the Send Data line.

Figure CA122-3 (Part 3 of 4). SDLC Operation

Supervisory Program (Includes Interrupt Handling)	SDLC Program Module: Functions / Commands	Command Code (Hex)	Data/ Mask (Hex)	SDLC Adapter
				This transmission procedure continues until an FTA bit is detected in the control information sent to TDCTH at the start of the final message segment. After the final data (or pad) character is transmitted, CHIO operations transfer the starting address of receive buffer A from the transmit control block to channel pointer 4. Similarly, the starting address of receive buffer B is transferred to channel pointer 5, and the starting address of the receive control block is transferred to channel pointer 6. The Receive Mode bit (RCTRL bit 0) now turns on. When the control logic detects the first SDLC flag, Adapter in Sync (RSTAT 7) turns on. The adapter now makes a channel request each time its receive data register is loaded with a character from the Receive Data line. Each CHIO operation transfers a character to receive buffer A. RCTRL bit 1 (Buffer A Valid) turns off at the first of these operations. When the adapter detects the first ending flag (IR A on Part 2): (1) Through CHIO operations, RDCTH and RDCTL are transferred to first location in the receive control block. The Valid Entry and FCS Valid bits will be on, and the count will indicate three remaining unused locations in receive buffer A. (2) The adapter makes an interrupt request Interrupt Request
	Return to SDLC program module. Read Basic Status (R BSTAT)	07	23	Receive Control Entry, Enabled, and IR are on.
	Reset Receive Status (RS RSTAT)	80	20	Turn off RSTAT Receive Control Entry bit.
	Transfer data from first 13 locations of receive buffer A to storage location designated by supervisory program and clear these receive buffer A locations.			
	Determine condition of Valid Entry (bit 0) in location 2 of receive control block. Assume this bit is off (0). Reset Basic Status (RS BSTAT)	04	20	Turn off BSTAT Receive Control Entry bit.

Continual Receive Data CHIO Operations

Supervisory Program (Includes Interrupt Handling)	SDLC Program Module: Functions / Commands	Command Code (Hex)	Data/ Mask (Hex)	SDLC Adapter
				The adapter detects that receive buffer A is full (the data count decrements to zero). A receive control entry with Valid Entry bit on is made to location 2 of receive control block. Receive data CHIO operations start using channel pointer 5 so that received data goes to buffer B. The adapter makes an interrupt request (IR B on Part 2).
				Interrupt Request
	Return to SDLC program module.			
	Read Basic Status (R BSTAT)	07	23	Receive Control Entry, Enabled, and IR are on.
	Reset Receive Status (RS RSTAT)	80	20	Turn off RSTAT Receive Control Entry bit.
	Transfer data from locations 13–16 of receive buffer A to storage location designated by supervisory program, and clear these buffer A locations.			
	Write Buffer A starting address into channel pointer 4.			
	Set Receive Control Register (S RCTRL)	88	40	Tutn on the Buffer A Valid bit.
	Determine condition of Valid Entry bit (bit 0) in location 3 of receive control block. Assume this bit is off.			
	Reset Basic Status (RS BSTAT)	04	20	Turn off BSTAT Receive Control Entry bit.
				The adapter detects that receive buffer B is full (the data count decrements to zero). A receive control entry with Valid Entry bit on is made to location 3 of receive control block. Receive data CHIO operations start using channel pointer 4 so that received data goes to buffer A. The control logic makes an interrupt request (IR C on Part 2).
				Interrupt Request
	Return to SDLC program module.			
	Read Basic Status (R BSTAT)	07	23	Receive Control Entry, Enabled, and IR are on.
	Reset Receive Status (RS RSTAT)	80	20	Turn off RSTAT Receive Control Entry bit.
	Transfer data from locations 1–16 of receive buffer B to storage location designated by supervisory program, and clear buffer B.			
	Write buffer B starting address into channel pointer 5.			
	Set Receive Control Register (S RCTRL)	88	20	Turn on buffer B Valid bit.

Continual Receive Data CHIO Operations

Figure CA122-3 (Part 4 of 4). SDLC Operation

Supervisory Program (Includes Interrupt Handling)	SDLC Program Module: Functions / Commands	Command Code (Hex)	Data/ Mask (Hex)	SDLC Adapter
	Determine condition of Valid Entry bit (bit 0) in location 4 of receive control block. Assume this bit is off.			
	Reset Basic Status (RS BSTAT)	04	20	Turn off BSTAT Receive Control Entry bit.
				The adapter detects a received flag. A receive control entry is made with Valid Entry, FCS Valid, and Flag Received bits on. The control logic makes an interrupt request (IR D on Part 2).
				Interrupt Request
	Return to SDLC program module.			
	Read Basic Status (R BSTAT)	07	23	Receive Control Entry, Enabled, on IR are on.
	Reset Receive Status (RS RSTAT)	80	20	Turn off RSTAT Receive Control Entry bit.
	Transfer data from locations 1 through 12 of receive buffer A to storage location designated by supervisory program, and clear these buffer locations.			
	Determine condition of Valid Entry bit (bit 0) in location 5 of receive control block. Assume this bit is off.			
	Reset Basic Status (RS BSTAT)	04	20	Turn off BSTAT Receive Control Entry bit.
				The receive data CHIO operations continue. After seven consecutive 1 bits, the adapter turns off Adapter in Sync (RSTAT bit 7).
				After 15 consecutive 1 bits, the adapter turns on RSTAT 3 (Fifteen 1's), BSTAT 4 (Exception), BSTAT 7 (IR), and makes an interrupt request (IR E on Part 2).
				Interrupt Request
	Return to SDLC program module.			
	Read Basic Status (R BSTAT)	07	08	Exception, Enabled, and IR are on.
	Read Receive Status (R RSTAT)	81	10	Fifteen 1's bit is on.
	Reset Receive Status (RS RSTAT)	80	10	Turn off Fifteen 1's bit.
	Reset Receive Control Reg (RS RCTRL)	90	80	Turn off Receive Mode.
	Note: *Other events that would cause program to turn off Receive Mode at appropriate time are:* *1. Final bit on in SDLC control character.* *2. A time-out.*			

Continual Receive Data CHIO Operations

Supervisory Program; Includes Interrupt Handler (IH)	BSC/S-S Program Module (BSCSSP) Function	Command Code (Hex)	Data/ Mask (Hex)	BSC/S-S Adapter
	Assume initialization.			
Write Function Request				
	Start a 10-second Clear to Send (CTS) timeout.	30	B2	
	Write a Pad character.	20	55	
	Reset Receive Mode (bit 0) and code length bits 5 and 6 in ACTRL.	38	86	
	Set Transmit Mode (bit 1) in ACTRL.	28	40	
	Return to IH to wait for interrupt.			
				Output Request Interrupt (Pad to serializer. Transmit Data Register ready for next character.)
Read BSTAT		07	43	Output Request, Enabled, and IR are on.
Return to BSCSSP				
	Write a SYN character (EBCDIC).	20	32	
	Return to IH.			
				Output Request Interrupt (SYN to serializer. Transmit Data Register ready for next character.)
Read BSTAT		07	43	Output Request, Enabled, and IR are on.
Return to BSCSSP				
	Write first data character.	20	xx	
	Update data storage address and count.			
	Do BCC accumulation on data.			
	Return to IH to wait for interrupt.			
				Output Request Interrupt (First data character to serializer. Transmit Data Register ready for next character.)
Read BSTAT		07	43	Output Request, Enabled, and IR are on.
Return to BSCSSP				
	Write next data character.	20	xx	
	Update data storage address and count.			
	Do BCC accumulation on data.			

Repeat sequence until all data is transmitted.

Read BSTAT		07	43	Output Request, Enabled, and IR are on.

Figure CA122-4 (Part 1 of 2). BSC Transmit Operation

Supervisory Program Includes Interrupt Handler (IH)	BSC/S-S Program Module (BSCSSP) Function	Command Code (Hex)	Data/ Mask (Hex)	BSC/S-S Adapter
Return to BSCSSP				
	Write End character (ETB or ETX).	20	26 } 20 }	
	Do BCC accumulation on End character.			
	Return to IH.			
				Output Request Interrupt. End character to serializer. Transmit Data Register ready for next character.
Read BSTAT		07	43	Output Request, Enabled, and IR are on.
Return to BSCSSP				
	Write first BCC character.	20	xx	
	Return to IH.			
				Output Request Interrupt. First BCC character to serializer. Transmit Data Register ready for next character.
Read BSTAT		07	43	Output Request, Enabled, and IR are on.
Return to BSCSSP				
	Write second BCC character.	20	xx	
	Return to IH.			
				Output Request Interrupt. Second BCC character to serializer. Transmit Data Register ready for next character.
Read BSTAT		07	43	Output Request, Enabled, and IR are on.
Return to BSCSSP				
	Write trailing Pad.	20	FF	
	Return to IH.			
				Output Request Interrupt. Pad to Serializer.
Read BSTAT		07	43	Output Request, Enabled, and IR are on.
Return to BSCSSP				
	Reset Transmit Mode in ACTRL. (Turn off ACTRL bits 3, 5, and 6, as well as Transmit Mode, so next command can establish 8-bit EBCDIC receive mode.)	38	56	
	Set Receive Mode in ACTRL.	28	88	
	Start a 3-second timeout.	30	8F	
	Return to IH.			
				Hardware deletes first received SYN character.
				Input Request Interrupt. (Second SYN character in Receive Data Reg.)

Supervisory Program; Includes Interrupt Handler (IH)	BSC/S-S Program Module (BSCSSP) Function	Command Code (Hex)	Data/ Mask (Hex)	BSC/S-S Adapter
Return to BSCSSP				
	Read second SYN character.	21	32	
	Verify validity of SYN character.			
	Return to IH.			
				Input Request Interrupt. (First character of ACK (DLE) in Receive Data Reg.)
Read BSTAT		07	83	Input Request, Enabled, and IR are on.
Return to BSCSSP				
	Read first character of ACK.	21	10	
	Return to IH.			
				Input Request Interrupt. (Second character of ACK)
Read BSTAT		07	83	Input Request, Enabled, and IR are on.
Return to BSCSSP			70	
	Read second character of ACK.	21	61	
	If correct ACK was received, update the ACK counter.			
	Post normal completion status to Write Function Request.			

Figure CA122-4 (Part 2 of 2). BSC Transmit Operation

Supervisory Program; Includes Interrupt Handler (IH)	BSC/S-S Program Module (BSCSSP) Function	Command Code (Hex)	Data/ Mask (Hex)	BSC/S-S Adapter
Read Function Request				
	Start a 10-second Clear to Send (CTS) timeout.	30	B2	
	Write a Pad character.	20	55	
	Reset Receive Mode (bit 0) and code-length bits 5 and 6 in ACTRL.	38	86	
	Set Transmit Mode (bit 1) in ACTRL.	28	40	
	Return to IH to wait for interrupt.			
				Output Request Interrupt. (Pad character to serializer. Transmit Data register ready for next interrupt.)
Read BSTAT		07	43	Output Request, Enabled, and IR are on.
Return to BSCSSP				
	Write a SYN character (EBCDIC).	20	32	
	Return to IH.			
				Output Request Interrupt. (SYN character to serializer.)
Read BSTAT		07	43	Output Request, Enabled, and IR are on.
Return to BSCSSP				
	Write a SYN character.	20	32	
	Return to IH.			
				Output Request Interrupt. (Second SYN character to serializer.)
Read BSTAT		07	43	Output Request, Enabled, and IR are on.
Return to BSCSSP				
	Start a 1-second timeout.	30	85	
	Write a DLE (first ACK) character.	20	10	
	Return to IH.			
				Output Request Interrupt. (DLE character to serializer.)
Reqd BSTAT		07	43	Output Request, Enabled, and IR are on.
Return to BSCSSP			61	
	Write correct ACK (ACK-0/ACK-1).	20	70	
	Return to IH.			
				Output Request Interrupt. (ACK-0/ ACK-1 to serializer.)
Read BSTAT		07	43	Output Request, Enabled, and IR are on.
Return to BSCSSP				
	Write trailing Pad.	20	FF	
	Return to IH.			
				Output Request Interrupt. (Pad to serializer.)

Figure CA122-5 (Part 1 of 2). BSC Receive Operation

Supervisory Program; Includes Interrupt Handler (IH)	BSC/S-S Program Module (BSCSSP) Function	Command Code (Hex)	Data/ Mask (Hex)	BSC/S-S Adapter
Read BSTAT →		07	43 →	Output Request, Enabled, and IR are on.
Return to BSCSSP →				
	Reset Transmit Mode in ACTRL. (Turn off ACTRL bits 3, 5, and 6, as well as Transmit Mode, so next command can establish 8-bit EBCDIC receive mode.)	38	56 →	
	Set Receive Mode in ACTRL.	28	88 →	
	Start a 3-second time-out.	30	8F →	
←	Return to IH.			
				Hardware deletes first received SYN character.
←				Input Request Interrupt. (Second SYN character in Receive Data Reg)
Read BSTAT →		07	83 →	Input Request, Enabled, and IR are on.
Return to BSCSSP →				
	Read second SYN character.	21	32 →	
←	Return to IH.			
←				Input Request Interrupt (STX character).
Read BSTAT →		07	83 →	Input Request, Enabled, and IR are on.
Return to BSCSSP →				
	Read STX character.	21	02 →	
	Clear the BCC accumulator.			
	Start a 3-second receive time-out.	30	8F →	
←	Return to IH.			
←				Input Request Interrupt (first data character).
Read BSTAT →		07	83 →	Input Request, Enabled, and IR are on.
Return to BSCSSP →				
	Read Data.	21	xx →	
	Store data, update address, and count.			
	Do BCC accumulation on data.			
←	Return to IH.			
Repeat sequence until end character is received.				
Read BSTAT →		07	43 →	Input Request Interrupt (ETX character).
Return to BSCSSP →				
	Read ETX.	21	03 →	
	Do BCC accumulation on ETX.			
←	Return to IH.			

Figure CA122-5 (Part 2 of 2). BSC Receive Operation

Supervisory Program; Includes Interrupt Handler (IH)	BSC/S-S Program Module (BSCSSP) Function	Command Code (Hex)	Data/ Mask (Hex)	BSC/S-S Adapter
←				Input Request Interrupt (first BCC character).
Read BSTAT →		07	83 →	Input Request, Enabled, and IR are on.
Return to BSCSSP →				
	Read first BCC character.	21	xx →	
	Do accumulation on BCC character.			
←	Return to IH.			
←				Input Request Interrupt (second BCC character).
Read BSTAT →		07	83 →	Input Request, Enabled, and IR are on.
Return to BSCSSP →				
	Read second BCC character.	21	xx →	
	Do accumulation on BCC character.			
	Verify that BCC accumulator is now zero. (If not, there is BCC check.)			
	Update the ACK counter.			
	Post completion status to Read Function Request.			

Supervisory Program; Includes Interrupt Handler (IH)	BSC/S-S Program Module (BSCSSP) Function	Command Code (Hex)	Data/ Mask (Hex)	BSC/S-S Adapter
Write Function Request →				
	Wait one character time.			
	Set Transmit Mode in ACTRL.	28	40 →	
	Start a 9-second Clear to Send (CTS) time-out.	30	AD →	
←	Return to IH to wait for CTS.			
←				Output Request Interrupt. (Transmit Data Reg ready for first character.)
Read BSTAT		07	43 →	Output Request, Enabled, and IR are on.
Return to BSCSSP →				
	Reset CTS timer.	04	10 →	
	If using 7-bit code, "OR" on low-order bit of STX.			
	Write STX. (Hardware adds Start and Stop bits.)	20	2D →	
←	Return to IH to wait for interrupt.			
←				Output Request Interrupt. (STX to serializer. Transmit Data Reg ready for next character.)
Read BSTAT		07	43 →	Output Request, Enabled, and IR are on.
Return to BSCSSP →				
	Fetch data byte to transmit. Check whether cam mode of receiver (upper case/lower case) is in same mode as character to transmit. If not, transmit a shift character, and wait for another output request.			
	If using 7-bit code, "OR" on low-order bit of the data byte.			
	Write the data character. (Hardware adds Start and Stop bits.)	20	xx →	
←	Return to IH to wait for interrupt.			
←				Output Request Interrupt. (Data character to serializer. Transmit Data Reg ready for next character.)
Read BSTAT		07	43 →	Output Request, Enabled, and IR are on.
Return to BSCSSP →				
	If the last character transmitted was a Line Feed, Carriage Return, or Tab, transmit Idle characters (hex BD) each character time until the carriage has had time to complete the function. Otherwise:			
	Fetch data byte to transmit.			
	Check whether cam mode of receiver			

Repeat sequence until all data has been transmitted.

Supervisory Program; Includes Interrupt Handler (IH)	BSC/S-S Program Module (BSCSSP) Function	Command Code (Hex)	Data/ Mask (Hex)	BSC/S-S Adapter
	If using 7-bit code, "OR" on low-order bit of EOT character.			
	Write an EOT character. (Hardware adds Start and Stop bits.)	20	3F →	
←	Post normal completion status to Write Function Request.			
←				Output Request Interrupt (EOT to serializer.)
Read BSTAT		07	43 →	Output Request, Enabled, and IR are on.
Return to BSCSSP →				
	Reset Transmit Mode in ACTRL.	38	40 →	
	Return to IH to wait for new function request.			

Figure CA122-6. S/S Transmit Operation

Supervisory Program; Includes Interrupt Handler (IH)	BSC/S-S Program Module (BSCSSP) Function	Command Code (Hex)	Data/ Mask (Hex)	BSC/S-S Adapter
Read Function Request				
	Set Receive Mode in ACTRL.	28	80	
	Start a 25-second time-out.	30	FD	
	Return to IH to wait for interrupt.			
				Input Request Interrupt. (Receive Data Reg is ready with a character.)
Read BSTAT		07	83	Input Request, Enabled, and IR are on.
Return to BSCSSP				
	Read Data (assume STX).	21		
	If using 7-bit code, shift data byte left one bit.		STX 3E	
	Start a 25-second time-out.	30	FD	
	Return to IH to wait for interrupt.			
				Input Request Interrupt.
Read BSTAT		07	83	Input Request, Enabled, and IR are on.
Return to BSCSSP				
	Read Data	21	xx	
	If using 7-bit code, shift data byte left one bit.			
	If data is an Idle, ignore it, and wait.			
	If data is Upshift or Downshift, record it and wait for next character.			
	If uppercase mode has been established by a previous Upshift, set the uppercase bit (hex 01) in data.			
	Store data, update addresses, and counts.			
	Start a 25-second time-out.	30	FD	
	Return to IH to wait for interrupt.			
				Input Request Interrupt.
Read BSTAT		07	83	Input Request, Enabled, and IR are on.
Return to BSCSSP				
	Read Data	21		
Repeat until EOT is read.				
				Input Request Interrupt.
Read BSTAT		07	83	Input Request, Enabled, and IR are on.
Return to BSCSSP				
	Read EOT.	21		
	If using 7-bit code, shift data left one bit (to check for EOT).		3E	
	Post normal completion status to Read Function Request.			

Figure CA122-7. S/S Receive Operation

CA130 Unique Communications Repair Strategy

Link-level testing under MAP control is not available for offline or online testing of communication features. In a DPPX environment, online tests are not available. In a DPCX environment, most online tests are not available. See Chapter 4, GR500, for information on general repair strategy.

CA134 Unique Communications Intermittent Repair Procedures

Refer to CA300 for detailed information on intermittent failures.

An intermittent failure is defined as:

- An error which occurs so infrequently that looping the test does not detect the error. For this type of error, use the system error log (CA312).
- Errors occurring at random times, which cause generation of different test error messages and make the MAPs ineffective. If the MAPs detect three different test error messages, use the action plans in CA250.
- Errors are detected only after looping the test for more than 5 minutes. Record the test error message and use the free-lance looping option (CA313) and the action plans in CA250.

CA135 Communications General Repair Procedures Using the CA MAPs

This procedure is used in the CA MAP to repair a problem using a FRU list arranged in the order of most probable failure. The MAP directs you to replace the FRU and rerun the test that failed. There is minimal probing, MAP step reading, and action required. However, all listed FRUs must be available.

This procedure may be used when time or conditions do not permit detailed or step-by-step investigation of a communications problem, your TP training is basic, or at your discretion.

Communications Step-by-Step Procedures Using the CA MAPs

This procedure is used in the CA MAP to repair a problem using a detailed step-by-step fault isolation. It provides you with detailed error information and a troubleshooting chart to isolate the fault to the specific FRU. Probing for the correct signal levels with a troubleshooting chart isolates the communications problem to a single FRU.

This procedure may be used when FRUs are difficult to obtain, the communications problem requires detail investigation, your TP training is intermediate/expert level, or at your discretion.

CA137 Communications Link-Level Test Procedures

Link-level testing is used for communications problem determination between the primary and secondary unit on either a data link or a loop (direct or data link attached). This testing is initiated in a free-lance mode. Complete link-level tests are available off-line and are resident on the MD diskette. Limited link-level tests are available with DPCX.

The following 4-step procedure describes how to use link-level tests for communications problem determination.

1. Establish a list of link-level tests for this PA. Link-level tests were suggested and listed before exiting the CA MAP. If in free-lance mode, use the configuration data or FAC code for the PA and the Communications FAC – Hardware Test Summary Table (CA150) to locate and identify the suggested link level tests.
2. Prepare to invoke in sequence the listed link-level tests. Review the test descriptions and invocation procedures in CA212 and CA202, respectively.
3. Invoke the first link-level test in the list. (Refer to Chapter 2, CP610, for standard invocation procedures.) Note any special instructions under CA201.
4. Inspect test messages.

   Caution: Some tests may require manual termination or cancellation. Note any special instructions under CA201.

   a. For a test error message (PAXE), go to CA165 and locate the message in the tables; review and perform the associated action plans.
   b. For a successful test completion (PA00 or 80BC), invoke the next link-level test in the list and reenter step 4 of this procedure. (Refer to Chapter 2, CP610, for standard invocation procedures.) Note any special instructions under CA201.
   c. If the last test in the list completes successfully, either an intermittent failure had occurred or no problem was detected during complete CA feature testing. If an intermittent failure was suspected, obtain the error log for this PA (see CA320 and Chapter 2 (CP830 for DPCX) for procedures on how to obtain the error log). Use the error log for the next action (see CA340, How to Use the Error Log).

CA150 Communications FAC–Hardware Test Summary

FAC	Configuration Table Data	Card/Cable Type	Card Jumpers	Board Jumpers	Required Test Routines
8	SDLC. Primary, loop, 1 lobe, loop supplied clock, 38.4 Kbps.	CA1, CA3, CAC3.	Loop - Primary Select - Lobe Operation - Serial - Carrier Select - Data Select	1. Channel request 2. Channel grant	1-15, 18, 51, 73, 75* 76, 88*, 90* – 94.
9	SDLC. Primary, loop, 2 lobe, loop supplied clock, 38.4 Kbps.	CA1, CA3, CA4, CAC3, CAC4.	Loop - Primary Select - Lobe Operation - Serial - Carrier Select - Data Select	1. Channel request 2. Channel grant	1-15, 18, 52, 73, 75*, 76, 89, 90* – 94.
10	SDLC. Primary, loop, 1 lobe, loop supplied clock, 9600 bps.	CA1, CA3, CAC3.	Loop - Primary Select - Lobe Operation - Serial - Carrier Select - Data Select	1. Channel request 2. Channel grant	1-15, 18, 51, 73, 75*, 76, 88, 90* – 94.
11	SDLC. Primary, loop 2 lobe, loop supplied clock, 9600 bps.	CA1, CA3, CA4, CAC3, CAC4.	Loop - Primary Select - Lobe Operation - Serial - Carrier Select - Data Select	1. Channel request 2. Channel grant	1-15, 18, 52, 73, 75*, 76, 89, 90* – 94.
12	SDLC. Primary or Secondary, EIA, adapter clock, external modem, 600, 1200 bps, line variables**.	CA1, CA5, CAC5A	EIA - Internal Wrap - 8100 clock	1. Channel request 2. Channel grant 3. Data rate	1-15, 16, 53*(P), 63, 64(1), 71*(S), 75(P), 90*, 91*, 93*, 94*
13	SDLC. Primary or Secondary, EIA, external modem/DCE, external clock, 2.0, 2.4, 4.8, 7.2, 9.6 Kbps, data-link attached Loop line variables**	CA1, CA5, CAC5A.	EIA - Internal Wrap - DCE clock	1. Channel request 2. Channel grant	1-15, 16, 53*(P), 63, 64(I)*, 71*(S), 75(P), 90*, 91*, 93*, 94*, 95*–99(DL).
15	SDLC. Primary, EIA direct connect, adapter clock, 600, 1200, 2400 bps.	CA1, CA5, CAC5B	EIA - Internal Wrap - 8100 clock	1. Channel request 2. Channel grant 3. Data rate	1-15, 16, 53*, 61, 75*, 90*, 91*, 93*, 94*.

FAC	Configuration Table Data	Card/Cable Type	Card Jumpers	Board Jumpers	Required Test Routines
16	SDLC. Primary, EIA direct connect, multi-speed clock, 4.8, 9.6 Kbps	CA1, CA5, CA10, CAC5B	EIA - Internal Wrap - 8100 clock Multispeed clock - LF	1. Channel request 2. Channel grant	1-15, 16, 53*, 61, 75*, 90*, 91*, 93*, 94*.
17	SDLC. Secondary, EIA direct connect, external clock, 2.0, 2.4, 4.8, 7.2, 9.6 Kbps	CA1, CA5 CAC5B	EIA - Internal Wrap - DCE clock	1. Channel request 2. Channel grant	1-15, 16, 61, 71*.
18	SDLC. Primary or secondary, integrated modem, nonswitched, adapter clock, 600, 1200 bps **Line Variables	CA1, CA8, CAC8	Integrated Modem - 2/4 Wire - CTS Set - Echo clamp - Transmit Level - Equalizer	1. Channel request 2. Channel grant 3. Data rate	1-15, 19, 53*(P), 71*(S), 75*(P), 90*, 91*, 93*, 94*(P)
19	SDLC. Secondary, integrated modem, switched line, adapter clock, 600, 1200 bps **Line Variables	CA1, CA9, CAC9	Integrated Modem - Coupler - Equalizer - Normal Ops - Transmit	1. Channel request 2. Channel grant 3. Data rate	1-15, 20, 25, 71(S)
20	SDLC. Primary or secondary, DDS, DDS supplied clock, 2.4, 4.8, 9.6 Kbps	CA1, CA7, CAC7	DDSA - DDL - Data rate	1. Channel request 2. Channel grant	1-15, 21, 22, 53*(P), 66, 71*(S), 75*(P), 90*, 91*, 93*, 94*(P)
21	SDLC. Secondary, DDS, DDS supplied clock, 56 Kbps (8140 only)	CA1, CA7, CAC7	DDSA - DDL - Data rate	1. Channel request 2. Channel grant	1-15, 21, 22, 66, 71*
24	SDLC. Primary, V.35, direct connect, adapter clock, 600, 1200, 2400 bps	CA1, CA6, CAC6B	V.35 - Internal Wrap - 8100 clock	1. Channel request 2. Channel grant 3. Data rate	1-15, 16, 53*, 63, 75*, 90*, 91*, 93*, 94*.

Legend:
*Link level test.
**Line variables are dependent on customer operations and data link order. For description, see CA114 and CA115.
DL = Data link attached loop
I = IBM modem
P = Primary
S = Secondary

FAC	Configuration Table Data	Card/Cable Type	Card Jumpers	Board Jumpers	Required Test Routines
25	SDLC. Primary, V.35, direct connect multispeed clock, 4.8, 9.6 Kbps	CA1, CA6, CAC6B	V.35 - Internal Wrap - 8100 clock Multispeed clock - LF	1. Channel request 2. Channel grant	1-15, 16, 53*, 63, 90*, 91*, 93*, 94*.
26	SDLC. Primary or secondary, V.35, direct connect multispeed clock 56 Kbps	CA1, CA6, CAC6B	V.35 - Internal Wrap - 8100 clock Multispeed clock - LF	1. Channel request 2. Channel grant	1-15, 16, 53*(P), 63, 71*(S), 90*, 91*, 93*, 94*
27	SDLC. Secondary, V.35, direct connect, external clock, 2.0, 2.4, 4.8, 7.2, 9.6 Kbps	CA1, CA6, CAC6B	V.35 - Internal Wrap - DCE clock	1. Channel request 2. Channel grant	1-15, 16, 63, 71*
28	SDLC. Secondary, V.35, direct connect, external clock, 56 Kbps	CA1, CA6, CAC6B	V.35 - Internal Wrap - DCE clock	1. Channel request 2. Channel grant	1-15, 16, 53*(P), 63, 71*(S), 90*, 91*, 93*, 94*
29	SDLC. Secondary, V.35, external clock, 48, 56 Kbps external modem	CA1, CA6, CAC6B	V.35 - Internal - DCE clock	1. Channel request 2. Channel grant	1-15, 16, 63, 71*(S)
A1 (RPQ 870892)	SDLC. Primary, V.35, direct connect, multispeed clock 19.2 Kbps	CA1, CA6, CA10, CAC6B	V.35 - Internal Wrap - 8100 clock Multispeed clock - LF	1. Channel request 2. Channel grant	1-15, 16, 53*, 63, 90*, 91*, 93*, 94*
30	SDLC. Primary or secondary, X.21, nonswitched, external clock, 2.4, 4.8, 9.6 Kbps, external DCE	CA1, CA11, CAC11	X.21 - Normal Wrap - Nonswitched Line - Timed DSR Drop - Normal Operation - Error Latch Disable - CTS Delay	1. Channel request 2. Channel grant	1-15, 16, 53*, 67, 68, 71(S), 75*, 90*, 91*, 93*, 94*
31	SDLC. Primary or secondary, X.21, nonswitched, external clock, 48 Kbps, external DCE	CA1, CA11, CAC11	X.21 - Normal Wrap - Nonswitched Line - Timed DSR Drop - Normal Operation - Error Latch Disable - CTS Delay	1. Channel request 2. Channel grant	1-15, 16, 53*, 67, 68, 71(S), 75*, 90*, 91* 93*, 94*
40	BSC. Primary or secondary, EIA, adapter clock external modem, 600, 1200 bps **Line Variables	CA2, CA5, CAC5A	EIA- Internal Wrap - 8100 clock	1. Data rate	1-15, 16, 63, 64, 65, 77*, 78*

FAC	Configuration Table Data	Card/Cable Type	Card Jumpers	Board Jumpers	Required Test Routines
41	BSC. Primary or secondary, EIA, external modem, external clock, 2.0, 2.4, 4.8, 7.2, 9.6 Kbps **Line Variables	CA2, CA5, CAC5A	EIA - Internal Wrap - DCE clock		1-15, 16, 63, 64, 65*, 77*, 78
43	BSC. Primary, EIA, direct connect, adapter clock, 600, 1200 bps	CA2, CA5, CAC5B	EIA - Internal Wrap - 8100 clock	1. Data rate	1-15, 16, 61, 77*, 78*
44	BSC. Primary, EIA direct connect, multispeed clock, 2.4, 4.8, 9.6 Kbps	CA2, CA5, CA10, CAC5B	EIA - Internal Wrap - 8100 clock Multispeed clock - LF		1-15, 16, 61, 77*, 78*.
45	BSC, Primary or secondary, integrated modem, nonswitched, adapter clock, 600, 1200 bps	CA2, CA8, CAC8	Integrated modem - 2/4 wire - CTS set - Echo clamp - Transmit level - Equalizer	1. Data rate	1-15, 19, 77*, 78*
47	BSC. Primary or secondary, DDS, interface supplied clock, 2.4, 4.8, 9.6 Kbps	CA2, CA7, CAC7	DDSA - DDL - Data rate		1-15, 21, 22, 66, 77*, 78*
60	Start/Stop. Primary, EIA, external modem, adapter clock 110, 134.5, 150, 300, 600 bps **Line Variables	CA2, CA5, CAC5A	EIA - Internal Wrap - 8100 clock	1. Data rate 2. Asynchronous	1-15, 16, 63, 64, 79* – 87
61	Start/Stop Primary, EIA, direct connect, adapter clock, 110, 134.5, 150, 300, 600 bps	CA2, CA5, CAC5B	EIA - Internal Wrap - 8100 clock	1. Data rate 2. Asynchronous	1-15, 16, 61, 79 – 87

Legend:
*Link level test.
**Line variables are dependent on customer operations and data link order. For description, see CA114 and CA115.
DL = Data link attached loop
I = IBM modem
P = Primary
S = Secondary

CA160 Communications Fault Isolation

CA161 Introduction

Communications fault isolation is the process of isolating a fault on a communications link/loop after customer problem determination procedures have located/isolated the communications problem to a specific communications subsystem or data link/loop. This process directs you to the appropriate fault isolation technique or to a set of procedures (see Figure CA161-1). The direction is based on messages/indicators provided by DPPX/DPCX, by the customer, or by the 8100 System. These messages may be available at customer setup time, during on-line operations (DPPX/DPCX), or offline.

8100 System/network problem determination is not accomplished in this section; problem determination is detailed in the following documents: *8100 Network Planning Guide; 8100 Subsystem Network Problem Determination Guide; Addendum to SNA System Problem Determination Guide.*

There are four basic types of communications problem determination messages: DPPX, DPCX, test, and other messages/indicators.

1. DPPX messages – These are messages or indicators displayed by DPPX when a communications hardware failure exists or when communications performance degradation occurs. These messages may be System Message Numbers (SMNs), Control Operator messages, or operator panel messages/indicators. See ST110 in Chapter 1 for specific DPPX messages.
2. DPCX messages – These are messages or indicators displayed by DPCX when a communications hardware failure exists or when communications performance degradation occurs. These messages may be System Message Numbers (SMNs), Control Operator messages, or operator panel messages/indicators. See ST210 in Chapter 1 for specific DPCX messages.
3. Test messages – These are test messages from a test routine (online or offline) or the Test Control Monitor (online or offline). These messages indicate error conditions, status, manual intervention stops, completion, or option entry stops. See CA165 for specific test messages.
4. Other messages/indications – These messages/indications may be from any of the following sources: oral/written messages from the customer, hardware/lamp indicators (such as the modem), host/terminal/control operators, physical damage (system, building, circuits), OEM technical representatives, or customer/IBM programmers. These messages may indicate a communications malfunction/failure; the message format is variable. See Section CA166 for possible messages.

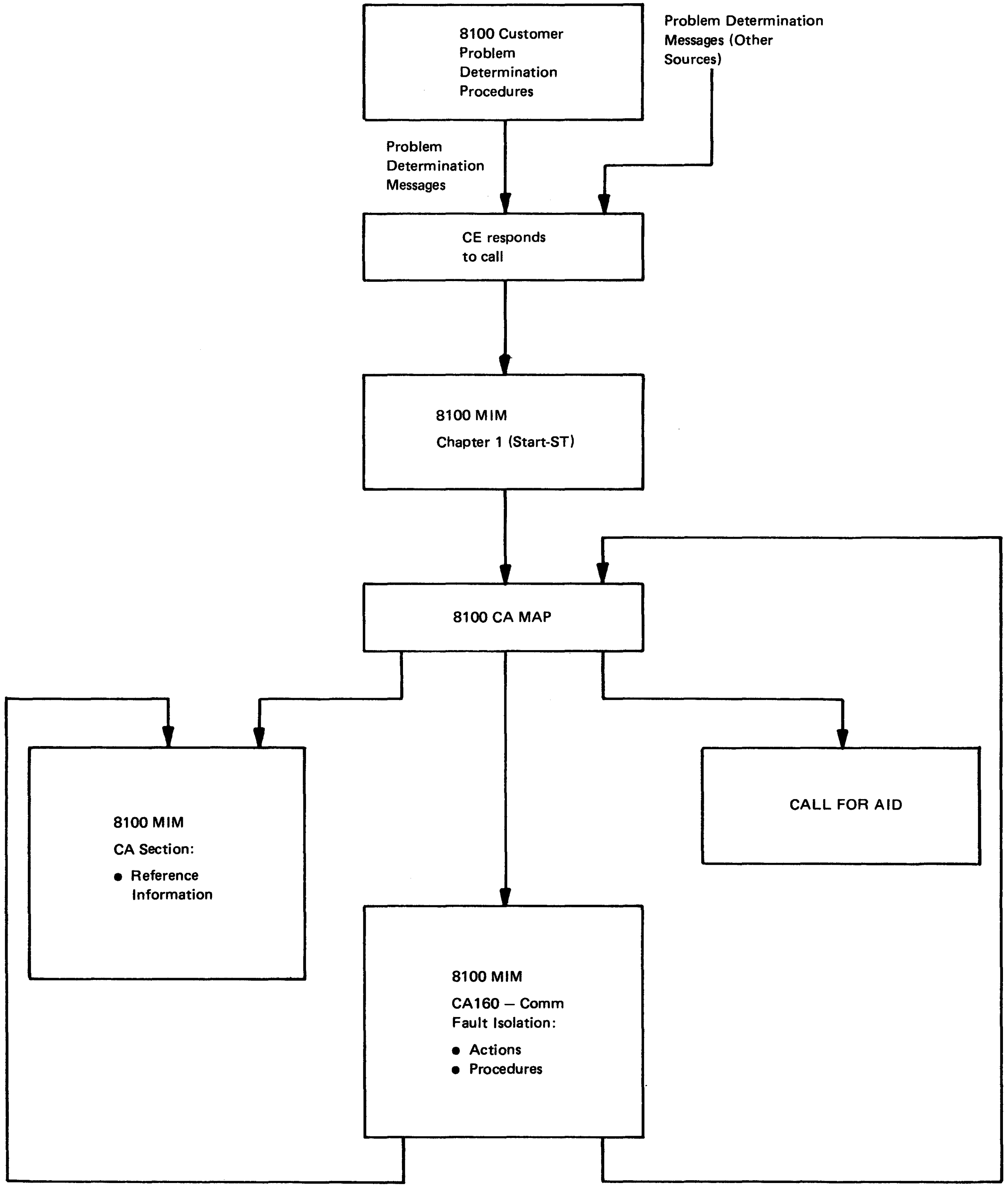


Figure CA161-1. 8100 Communications Fault Isolation Procedure

CA162 How to Use this Section

You should be entering this section with a message/indicator pertaining to a communications problem (see CA161). If you have no message/indicator and suspect a communications problem, go to CA166 and use the No Message entry point.

1. Identify the message type (Test or Other). Review tables in CA165 or CA166.
2. Enter the appropriate table (CA165 or CA166) and locate the message. If you cannot find your message, go to CA166 and use the No Message entry point.
3. Review the message description and associated action plan for your message.
4. Review the 8100 System configuration data for communications. This is available from customer configuration data sheets, customer order, installation records, or physical inspection.
5. Identify the port physical address (PA) for the suspect CA feature. This may be available within the message or derived from a review of the configuration data.
6. Perform the action plans for your message in the order listed. See CA250 for action plans.

CA165 Test Messages

Test error messages are preceded by: PA Y E

where:

PA = Physical Address

Y = 1 or 2

E = Error

Test Message	Action Plan (Refer to CA250.)
01XX through 15XX	15, 14
161C 1630	Do the following steps in sequence: 1. Make sure all system components in the link to be tested are turned on. Rerun the test. 2. Make sure the communication cables are connected. Rerun the test. 3. Perform Action Plans 40, 15, 14.
16XX	40, 15, 14
18XX 19XX 20XX 21XX 22XX	15, 14
2501 2504	15, 14
25AA	Retry Test. Perform Action Plans 15, 14.
2599	Reconfigure MD table.
5101 through 5125	15, 14
5126	Do the following steps in sequence: 1. Make sure the external communication cable is connected to a loop station connector (LSC). Rerun the test. 2. Perform Action Plans 15, 14.
5127	15, 14
5128	Do the following steps in sequence: 1. Have the customer perform loop problem determination procedures. 2. Perform Action Plans 15, 14.
5129 XXSA	Perform terminal problem determination procedure whose address is identified by the SA field.
5135 51FE 5201 through 5225	15, 14
5226	Do the following steps in sequence: 1. Make sure the external cables for both lobes are connected to loop station connectors (LSCs). Rerun the test. 2. Perform Action Plans 15, 14.
5227	15, 14
5228	Same as 5128.
5229 XXSA SAXX	Perform terminal problem determination procedure whose address is identified by the SA field.
5230 5231	Same as 5226.
5232 5233	15, 14
5234	Do the following steps in sequence: 1. Have the customer perform loop problem determination procedure for lobe 2. 2. Perform Action Plans 15, 14.
5235	Do the following steps in sequence: 1. Have the customer perform loop problem determination procedure for lobe 1. 2. Perform Action Plans 15, 14.

Test Message	Action Plan (Refer to CA250.)
5301 through 530B	15, 14
5310	Do the following steps in sequence: 1. Activate downline station or device, rerun test 53. 2. If this is a peer-to-peer link, run test 71 in 8100 peer, and rerun test 53. 3. Perform remote site problem determination, using appropriate maintenance manual. 4. Test the modem (if IBM) using appropriate IBM modem maintenance manual. If DCE is OEM, report possible OEM DCE problem to customer. 5. Report possible data link problem to customer.
5311 531A 531F	15, 14
5320 through 53FE	Do the following steps in sequence: 1. Perform remote site problem determination using appropriate maintenance manual. 2. Test the modem (if IBM) using appropriate IBM modem maintenance manual. If DCE is OEM, report possible OEM DCE problem to customer. 3. Report possible data link problem to customer. 4. Perform Action Plans 15, 14.
6130	Do the following steps in sequence; rerun the test after each step: 1. Make sure the external communication cable has a wrap plug installed on the remote end. Rerun the test. 2. Make sure the external communication cables are correctly plugged. Rerun the test. 3. Perform Action Plans 15, 14.
61XX	15, 14
6330	Do the following steps in sequence; rerun the test after each step: 1. Make sure the switch at the remote end of the external EIA communication cable is in the TEST position. Or, make sure the wrap plug is installed on the remote end of the external V35 communication cable. Rerun the test. 2. Make sure the external communication cables are correctly plugged. Rerun the test. 3. Perform Action Plans 15, 14.

Test Message	Action Plan (Refer to CA250.)
63XX	15, 14
64XX	15, 14, 41
6690	Do the following steps in sequence; rerun the test after each step: 1. Make sure the switch at the remote end of the external DDS communication cable is in the TEST position. Rerun the test. 2. Make sure the external communication cables are correctly plugged. Rerun the test. 3. Perform Action Plans 15, 14.
66XX 67XX 68XX	15, 14
7101 through 7120	15, 14
7121	1. No failure if SDLC primary site stopped sending link tests AND all tests were received. 2. Perform Action Plans 15, 14.
7122	Same as 5320.
7123 7124	15, 14
7125	Same as 5320.
7126 7127	15, 14
7128	Same as 5320.
7129 through 7199	15, 14
72XX 73XX	15, 14
7501	15, 14
7520	Do the following steps in sequence: 1. Verify configuration table has correct station/device address and entries. 2. Perform Action Plans 15, 14.

Test Message	Action Plan (Refer to CA250.)
7521	15, 14
7523	Do the following steps in sequence: 1. Check station for power on, correct address and speed switches. 2. Perform Action Plans 15, 14.
75CE	Invalid data entered. Enter valid data.
75FE	Check configuration table for invalid entries; correct where necessary.
7601	15, 14
7620	Same as 7520.
7623	Same as 7523.
7643 SABA	Perform station problem determination procedure whose address is identified by the SA field.
76FE	Same as 75FE.
7701 through 7714	15, 14
7715	Do the following steps in sequence: 1. Prepare for/verify remote site ready for test. 2. Test the modem (if IBM) using appropriate IBM modem maintenance manual. If DCE is OEM, report possible OEM DCE problem to customer. 3. Report possible data link line problem to customer. 4. Perform Action Plans 15, 14.
771C through 7799	15, 14
7801 through 7814	15, 14
7815	Same as 7715.
781A through 7899	15, 14

Test Message	Action Plan (Refer to CA250.)
79XX 80XX 81XX 82XX 83XX 84XX 85XX 86XX 87XX	Do the following steps in sequence: 1. Perform station local or remote site problem determination procedures. Use appropriate problem determination guide. 2. Test the modem (if IBM) using appropriate IBM modem maintenance manual. If DCE is OEM, report possible OEM DCE problem to customer. 3. Report possible data link line problem to customer. 4. Perform Action Plans 15, 14.
88XX 89XX	15, 14
9001 9021	15, 14, 18
9031	1, 15, 14, 18
90E0	1, 15, 14, 18
90FE	1, 15, 14
9101 9121	15, 14, 18
9131	1, 15, 14, 18
9135	1, 15, 14, 18
91E0	1, 15, 14, 18
91FE	1, 15, 14
9201 9221	15, 14, 18
9231	1, 15, 14, 18
9234	1, 39
9236	1, 39
92E0	1, 15, 14, 18
92FE	1, 15, 14
9301 9321	15, 14, 18
9331	1, 15, 14, 18

Test Message	Action Plan (Refer to CA250.)
9335	1, 15, 14, 18
93E0	1, 15, 14, 18
93FE	1, 15, 14
9401 9421	15, 14, 18
9431	1, 15, 14, 18
94CE	1, 15, 14
94E0	1, 15, 14, 18
94FE	1, 15, 14
9501	15, 14
9520	1, 19
9521	15, 14
9529 SAXX	1, 45
9531	1, 38
9532 9536 9537 9543	46
95E0	1, 15, 14, 18
9601 9621	1, 15, 14
9631	1, 38
9632 9635 9636 9637 9638 9639 9640 9643	46
96E0	1, 15, 14, 18

Test Message	Action Plan (Refer to CA250.)
9701 9721	1, 15, 14
9732 9736 9745	46
97E0	1, 15, 14
9801	15, 14
9820	1, 19
9821	15, 14
9823	45
9832	46
9843	45
98FE	1, 19
9901	15, 14
9920	1, 19
9921	15, 14
9923	45
9932	46
9943	45
99CE	Invalid data input; enter valid data.
99FE	1, 19

CA166 Other Messages/Indicators

Message/Indicator	Problem Category	CA250 Action Plan
Incorrect X.21 signalling Incorrect DDS signalling Incorrect SDLC operations Incorrect BSC operations Incorrect Start/Stop operations	Incorrect line discipline operations/messages	1, 15, 14, 4, 38
No response – Station – Terminal – Controller – Host	Incorrect addressing. See also hardware failure category below.	11, 15, 14, 4, 38
High transmission errors Bad or lower performance High error rate on transmission	Reduced performance	18, 15, 14, 8, 9
*No error detected with customer PDPS. *Error occurs – goes away. *Loop/link error – Can't find with tests/PDPs.	Intermittent errors	5, 15, 14, 7, 13
No message Can't remember message Wrong message Multiple messages	No message; communication problem.	15, 14, 3
External communications cables cut Modem/DCE dropped/damaged 8100 damaged	Physical damage	15, 14, 3
Incorrect modem/DCE – Power lamp – Data lamp Incorrect CBS coupler – Power Incorrect line ready indicators	Physical indicators	1, 9, 41, 15, 14

*With/without DPPX/DPCX message.

Message/Indicator	Problem Category	CA250 Action Plan
Incorrect DTE control lines TELCO ckt/OEM modem checkout OK; still have problem.	OEM technical messages	15, 14
Loop/link is 'BAD'; can not communicate Faulty data Link/Loop No terminal/host/controller communications.	Hardware failure	1, 15, 14
Link test failure 'BAD' link test	Link test failure	1, 15, 14, 3, 38
Bad Data-link attached loop. No contact with data-link loop station	Data-Link attached loop failure	1, 15, 14, 6, 38
Unexpected error condition	System or design failure	43

CA200 Offline and Online Tests

Offline and DPCX online tests are provided to test and repair the CA features. Offline tests reside on the MD diskettes; the online tests are provided only for those systems using DPCX, and are stored on the system resident device.

CA201 Communications Test Routine Summary

RT	Description	SDLC	BSC S-S	Adr Lvl	Invocation (see Notes) Offline MAPs	Offline F/L	DPCX	CSU	MI
01	Adapter card tests	X	X	1	X	X	X	X	
02	Adapter card tests	X	X	1	X	X	X	X	
03	Adapter card tests	X	X	1	X	X	X	X	
04	Adapter card tests	X	X	1	X	X	X	X	
05	Adapter card tests	X	X	1	X	X	X	X	
06	Adapter card tests	X	X	1	X	X	X	X	
07	Adapter card tests	X	X	1	X	X	X	X	
08	Adapter card tests	X	X	1	X	X	X	X	
09	Adapter card tests	X	B	1	X	X	X	X	
0A	Adapter card tests	X	B	1	X	X	X	X	
0B	Adapter card tests	X	B	1	X	X	X	X	
0C	Adapter card tests	X	B	1	X	X	X	X	
0D	Adapter card tests	X	S	1	X	X	X	X	
0E	Adapter card tests	X	B	1	X	X	X	X	
0F	Adapter card tests	X	B	1	X	X	X	X	
10	Adapter card tests	X	S	1	X	X	X	X	
11	Adapter card tests	X	S	1	X	X	X	X	
12	Adapter card tests	X	B	1	X	X	X	X	
13	Adapter card tests	X	B	1	X	X	X	X	
14	Adapter card tests		S	1	X	X	X	X	
15	Adapter card tests	X	X	1	X	X	X	X	
16	Internal/external data wrap	X	X	1	X	X	X		
18	Loop adapter card test	X		1	X	X		M/8	
19	Integrated modem (nonswitched)	X	X	1	X	X		X	
20	Integrated modem (switched)	X	X	1	X	X		X	
21	DDSA test	X	X	1	X	X			
22	DDSA internal wrap	X	X	1	X	X		X	
25	Auto answer	X	X	1	16	16			17
51	Loop – 1 lobe	X		1	15	15	15		
52	Loop – 2 lobe	X		1	15	15			
53*	Data link group	X		1	P/5	5	5		
61	EIA – direct connect	X	X	1	6	6		M/6	
63	EIA/V.35 – external test	X	X	1	7	7		M/7	
64	IBM modem analyzer	X	X	1	X	X			17
66	DDSA – external	X	X	1	9	9		9	
67	X.21 – external 1	X		1	9	9			
68	X.21 – external 2	X		1	9	9			
71*	SDLC secondary link	X		2		10	11		17
72	Data link loop – poll test	X		2	X	X			17
73	Loop station relay pick	X		1	12	12			
75*	Link/loop group analysis	X		1	5	5	5		17
76	Loop beacon/ordinal sequence	X		1		5	5		17
77*	BSC link – requestor		X	2		13			17
78*	BSC link – responder		X	2		14			17
79*	2741 all characters		X	2		X			17

RT	Description	SDLC	BSC S-S	Adr Lvl	Invocation (see Notes) Offline MAPs	Offline F/L	DPCX	CSU	MI
80*	2741 tilt, rotate, twist		X	2		X			17
81*	2741 special function		X	2		X			17
82*	2741 read		X	2		X			17
83*	2741 echo		X	2		X			17
84*	2741 attention key		X	2		X			17
85*	TTY aux line test		X	2		X			17
86*	TTY aux echo test		X	2		X			17
87*	2741 aux line		X	2		X			17
88	Loop – 1 lobe poll test	X		1		X	X		17
89	Loop – 2 lobe poll test	X		1		X			17
90$	SDLC link test cmd–no data	X		2/3		5	5		
91$	SDLC link test cmd – data	X		2/3		5	5		
92$	Monitor mode	X		2/3		5	5		
93$	SDLC link test – user data	X		2/3		5	5		17
94$	Line analysis	X		2/3		5	5		17
95*	384X SDLC test cmd	X		2		5	X		
96*	384X loop data	X		2		5	X		
97	Configuration self-test to 384X	X		2		5	X		
98	384X loop beacon and ordinal	X		2		5	X		17
99*	384X loop-lobe analysis	X		2		5	X		17

Notes:

* – *Link level test*
$ – *Link level test; level 2 addressing for directly attached loops or data link stations; level 3 addressing for data link attached loop devices.*
B – *BSC only*
F/L – *Free-lance*
M – *Modified*
MI – *Manual Intervention messages*
P – *If Primary*
S – *Start-Stop only*
X – *Normal invocation*

1. *Address level 1*
2. *Address level 2*
3. *Address level 3*
4. *Not used.*
5. *Group stations/devices/units must be in a ready condition before this test is invoked.*
6. *These tests must be run when the EIA-direct connect cable is isolated from the direct-connected host/device using the EIA-direct connect wrap plug.*
7. *Use the V.35 wrap plugs or the EIA modem cable test switch to isolate the EIA modem or V.35 communications cable from the external modem or host connection.*
8. *For CSU only, a loop wrap plug must be installed at the end of the loop cable(s) before running this test.*
9. *This test must be run with the external cable switch in the test position.*
10. *The host or controller must send SDLC link test commands to the 8100 Processor (invoke routine 71). Coordination between the two sites is required for the start and end of test. This test requires manual intervention. See Chapter 2 for routine termination procedures.*
11. *Use DPCX SDLC link test procedure, CA223.*
12. *See CA551/CA653 for setup procedures. See Chapter 2 for termination procedures.*
13. *The responding unit must be ready to respond.*
14. *This test should be initiated before a requesting device/unit issues a test request.*
15. *Loop cable(s) must be plugged into the loop station connector(s) (LSC).*
16. *The external communications cable must be attached to both the 8100 and the telephone line via the Data Access Arrangement.*
17. *Refer to CA210 for Manual Intervention messages.*

CA202 Invocation Procedures

A summary of standard and unique invocation procedures for communications feature tests is given below. Special invocation notes for each routine and addressing levels are given in the Communications Test Routine Summary, CA201.

INVOCATION FOR A GROUP OF TESTS (LEVEL 1 ADDRESSING ONLY)

Refer to Figures CA202-1 and CA202-2 for test environment.

1. The test control monitor (TCM) has been loaded and is at an 80BC or PA00 wait stop.
2. Enter PAB.

   where:

   PA = Adapter physical address – level 1 only

   B = Enters invocation message – address field section
3. At 81BC wait stop, enter SLB.

   where:

   S = Sense option

   0 = Run adapter ruoutines (1–15)

   1 = Run adapter and driver card routines (S = 0 tests, and one of the following: 16 or 18 or 19 or 20 or 21 and 22).

   2 = Run adapter and driver card routines and basic link level tests (S = 1 tests, and one of the following: 51 or 52 or 53).

   Note: *Default value = 0.*

   L = Looping option

   0 = Run routines one time

   *1 = Loop selected routines; stop on error

   *2 = Loop selected routines; no stop on error

   Note: *Default value = 0.*

   B = Enters invocation message – option field section and begins test execution.

*In DPCX online, looping is five times.

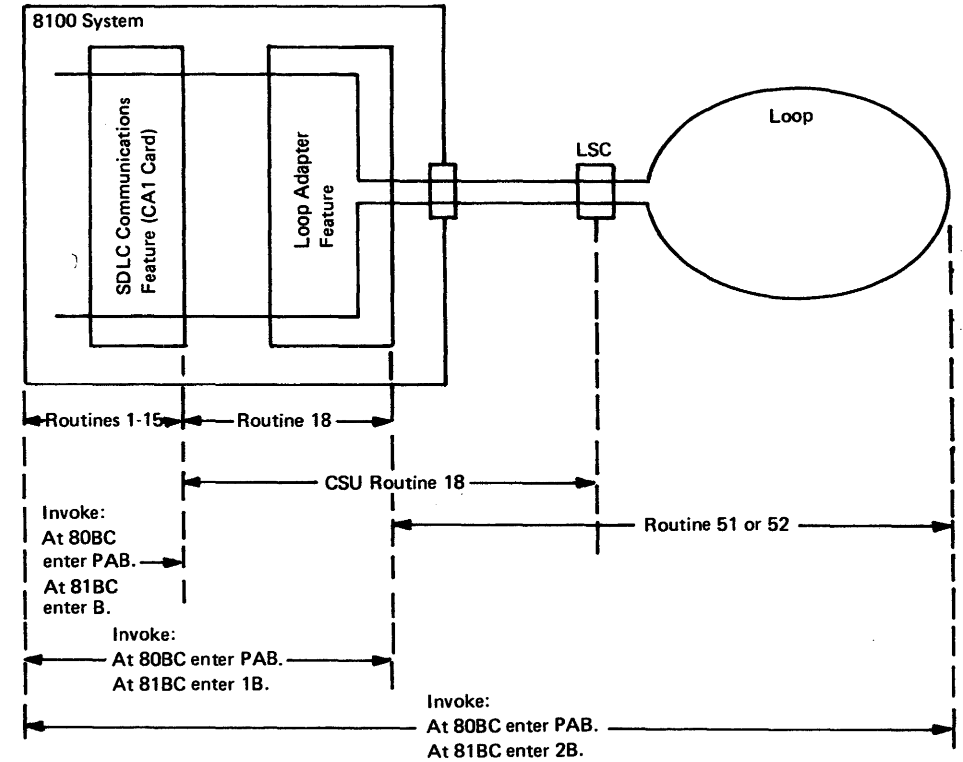


Figure CA202-1. Invocation for a Group of Tests (Level 1 Addressing Only), Loop Feature Example

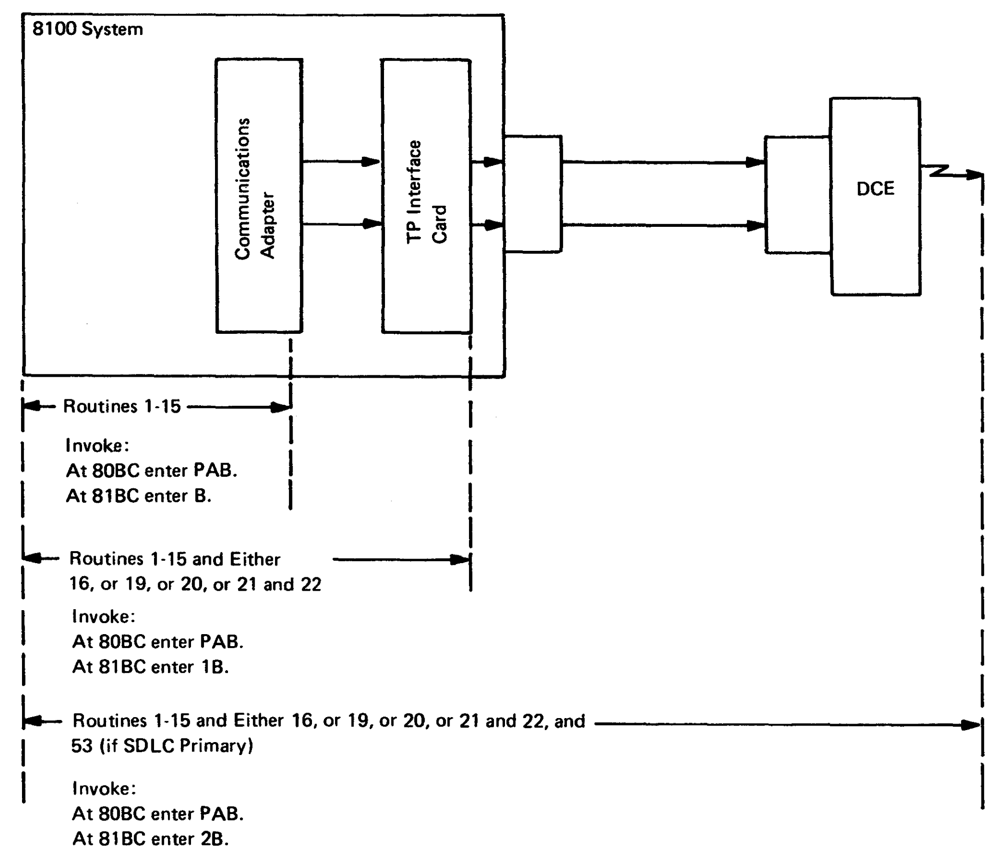


Figure CA202-2. Invocation for a Group of Tests (Level 1 Addressing Only), General TP Feature Example

INVOCATION FOR A GROUP OF TESTS (LEVEL 2 OR 3 ADDRESSING ONLY)

Note: *This procedure applies only to: groups of tests 90, 91, 92* and 95, 96, 97; to data link attached stations; direct attached loop stations; or data link attached loop and stations.*

1. The test control monitor (TCM) has been loaded and is at an 80BC or PA00 wait stop.
2. Enter PASADAB

   Enter address field(s) as required. Address field definition is determined by either the test routine (see CA201 test summary for address levels) and/or by the customer configuration data sheet or the configuration table (see Chapter 2, CP300, on how to obtain the configuration table).

   where:

   PA = Adapter physical address — level 1

   SA = Group or station address — level 2

   DA = Station or device address — level 3

   B = Enters invocation message — address field section
3. At 81BC wait stop, enter SLB.

   where:

   S = Sense option

   = 0, 1, or 2 Run tests 95, 96, 97 if 384X
   90, 91, 92* if group or device

   Note: *Default value = 0.*

   L = Looping option

   0 = Run routines one time

   **1 = Loop selected routines; stop on error

   **2 = Loop selected routines; no stop on error

   Note: *Default value = 0.*

   B = Enters invocation message — option field section and begins test execution.

*Routine 92 is run only if stations are on a direct attached loop or a data link attached loop.
**In DPCX online, looping is five times.

INVOCATION FOR A SINGLE TEST ROUTINE (ANY LEVEL ADDRESSING)

1. The test control monitor (TCM) has been loaded and is at an 80BC or PA00 wait stop.
2. Enter PASADAB

   Enter address field(s) as required. Address field definition is determined by either the test routine (see CA201 test summary for address levels) and/or by the customer configuration data sheet or the configuration table (see Chapter 2, CP300, on how to obtain the configuration table).

   where:

   PA = Adapter physical address — level 1

   SA = Group or station address — level 2

   DA = Station or device address — level 3

   B = Enters invocation message — address field section
3. At 81BC wait stop, enter SLRRB

   Enter option fields as required.

   where:

   S = Sense option:

   = Always zero (0).

   L = Loop option

   0 = Run routine one time

   *1 = Loop selected routine; stop on error

   *2 = Loop selected routine; no stop on error

   RR = Routine number

   B = Enters invocation message — option field section and begins test execution.

*In DPCX online, looping is five times.

CA210 Offline Test Routine Descriptions

Routines 1–15 (adapter card tests) test the SDLC or BSC/S-S adapter card. Routines starting with Routine 16 (device tests) test other communications feature hardware (for example, interface driver card or cables), or exercise the communication link/loop to the host or to stations/devices.

CA211 Adapter Card Tests (Routines 1–15)

The offline communication tests verify the operation of the CA adapter cards with one of its attached driver cards. The test consists of 21 routines located on the MD diskette. The routines are arranged so that they test functions within the adapter card in an order that isolates any failure to the FRU or FRUs most likely to be bad. The test is invoked through the MD, either by the CA MAP or by a free-lance operation. The MAPs automatically invoke the tests as they are required, but the free-lance operation requires a test invocation message.

Routine 1. The tests are different depending on the type of adapter card.

SDLC ADAPTER CARD

- Tests adapter reset command and out-bus parity.
- Tests set, read, and reset basic status commands.
- Tests set, read, and reset of basic status bit 5.

BSC/S-S ADAPTER CARD

- Tests recognition of all valid commands. Results of the I/O instruction are not checked. An error is indicated if a machine check occurs.
- Tests that basic status is clear after adapter reset.

Routine 2. The tests are different depending on the type of adapter card.

SDLC ADAPTER CARD

- Tests that all valid commands can be accepted by the adapter.
- Tests set, read, and reset of diagnostic control register.
- Tests set, reset, and read of DCE control register.

BSC/S-S ADAPTER CARD

- Tests that all invalid commands cause a machine check. Checks that B/S bit (machine check) can be reset.
- Tests that B/S bit (machine check) can be reset.

Routine 3. The tests are different depending on the type of adapter card.

SDLC ADAPTER CARD

- Tests function of DSR and DSR transition.
- Tests function of RTS, CTS, CTS transition, and disable CTS.
- Tests function of select standby, ring indicator, ring indicator transition, and disable ring indicator.
- Tests function of data rate select, receive line signal detected, and disable RLSD.

BSC/S-S ADAPTER CARD

- Tests that all bits of the adapter control register can be set, read, and reset.

Routine 4. The tests are different depending on the type of adapter card.

SDLC ADAPTER CARD

- Tests ability to write, read, and decrement timers.
- Tests that TI1 and TI2 function properly. (TI = Timer Interrupt.)
- Tests that reset T1 and T2 of MSTAT stops timer.
- Tests ability of oscillator to drive timers.

BSC/S-S ADAPTER CARD

- Tests that all bits of modem control register can be written and read.

Routine 5. The tests are different depending on the type of adapter card.

SDLC ADAPTER CARD

- Tests set and reset of BSTAT bit 6.

BSC/S-S ADAPTER CARD

- Tests that bits of modem status register can be set, read, and reset. Bits 2 (RLSD), 3 (RI), 5 (reserved), and 6 (RLSD TRANS) are not tested. Bit 2 (modem interrupt) of basic status register is tested.

Routine 6. The tests are different depending on the type of adapter card.

SDLC ADAPTER CARD

- Tests write and read of specific address decode register.
- Tests write and read of group address decode register.

BSC/S-S ADAPTER CARD

- Tests duration of timer countdown.
- Tests set, read, and reset of bit 3 (timer interrupt), and bit 7 (interrupt request) of basic status register.

Routine 7. The tests are different depending on the type of adapter card.

SDLC ADAPTER CARD

- Tests write and read of transmit data FCB register.
- Tests write and read of transmit FCB register.
- Tests write and read of transmit data channel I/O count high register.
- Tests write and read of transmit data channel I/O count low register.

BSC/S-S ADAPTER CARD

- Tests operation of timer control bits (bus bit 0 for write timer high command and bus bit 7 for write timer low command).

Routine 8. The tests are different depending on the type of adapter card.

SDLC ADAPTER CARD

- Tests write and read of receive data FCB register.
- Tests write and read of receive FCB register.
- Tests write and read of receive buffer length register.
- Tests write and read of receive control count register.

BSC/S-S ADAPTER CARD

- Tests set, read, and reset of basic status bit 6 (enable/disable).

Routine 9. The tests are different depending on the type of adapter card.

SDLC ADAPTER CARD

- Tests set, read, and reset of transmit control register.
- Tests set, read, and reset of receive control register.

BSC/S-S ADAPTER CARD

- Adapter is placed in wrap, transmit, receive and auto modes. Three EBCDIC sync characters are wrapped; then tests:
  1. Set, read, reset of basic status bit 0 (input request).
  2. Set, read, reset of basic status bit 1 (output request).
  3. Set, read, reset of adapter status bit 7 (adapter in sync).
  4. Absence of adapter status bit 2 (receive clock running).
  5. Setting of EBCDIC mode (bit 3 off, bit 4 on in adapter control register).

Routine 0A. The tests are different depending on the type of adapter card.

SDLC ADAPTER CARD

- Tests ability to enter transmit mode and test continuous character transmit (tone TX).
- Tests channel I/O transmit.
- Tests channel I/O transmit with fast turn-around (FTA).
- Tests channel I/O transmit with TTO. (TTO = transmit timeout.)
- Tests channel I/O transmit with frame chain.
- Tests channel I/O transmit with pad insert and frame chain.
- Tests channel I/O transmit – transmit turnoff and pad insert.
- Tests channel I/O transmit – FTA and pad insert FTA.
- Tests channel I/O transmit – data chain.
- Tests channel I/O transmit – count = 0.
- Tests channel I/O transmit – transmit data count high and low.

BSC/S-S ADAPTER CARD – BSC ONLY

- Adapter is placed in wrap, transmit, and auto modes. Three ASCII sync characters are wrapped; then tests:
  1. Set, read, reset of output request.
  2. Set of adapter in sync.
  3. Absence of receive clock running.
  4. Setting of ASCII mode (bit 3 on, bit 4 off in adapter control register).
  5. Input request does not occur with receive mode off.

Routine 0B. The tests are different depending on the type of adapter card.

SDLC ADAPTER CARD

- Tests PIO transmit controls used to test receive path, NRZI mode, and RTS turnoff:
  1. The TX PIO controls used to test the channel I/O receive path.
  2. NRZI mode data conversion.
  3. When TX mode is controlling RTS, RTS stays until the last bit is out of serializer.
- Tests the following:
  1. Receive mode bit.
  2. Ability to achieve character sync.
  3. Set of traffic bit.
  4. Ability to set 15 ones/go ahead.
  5. 15 ones/go ahead resets sync.
  6. 15 ones sets exception and interrupt request.
  7. Ability to reset 15 ones and traffic bit.
  8. Ability to reset exception.

BSC/S-S ADAPTER CARD – BSC ONLY

- Adapter is placed in wrap, transmit, receive, and auto modes. Four SDLC flag byte characters are wrapped; then tests:
  1. Set, read, reset of output request.
  2. Set, read, reset of basic status bit 4 (exception).
  3. Set, read, reset of adapter status bit 4 (SDLC flag).
  4. Set of adapter in sync.
  5. Setting of SDLC mode (bit 3 on, bit 4 on in adapter control register).

Routine 0C. The tests are different depending on the type of adapter card.

SDLC ADAPTER CARD

- Tests 15 ones with receive mode off.
- Tests that flag detect resets 15 ones enable.
- Tests ability to set invalid sequence.
- Tests that flag followed by B'11111110' does not set invalid sequence.
- Tests adapter overrun function.

BSC/S-S ADAPTER CARD

- Adapter is placed in wrap, transmit, receive, and EBCDIC modes. Three sync characters are transmitted. The third output request is not serviced. Then tests:
  1. Set, read, reset of basic status bit 1 (output request).
  2. Set of basic status bit 4 (exception).
  3. Set, read, reset of adapter status bit 1 (underrun).

Routine 0D. The tests are different depending on the type of adapter card.

SDLC ADAPTER CARD

- Tests invalid address.
- Tests specific address decode.
- Tests group address decode.
- Tests general address decode.

BSC/S-S ADAPTER CARD – S-S ONLY

- Adapter is placed in wrap, transmit, and receive modes. Data characters are wrapped; then tests:
  1. Set, read, reset of basic status bit 1 (output request).
  2. Set, read, reset of adapter status bit 2 (receive clock running).
  3. Set of basic status bit 1 (output request).
  4. Set, read, reset of basic status bit 0 (input request).
  5. That input request does not occur with receive mode off.

Routine 0E. The tests are different depending on the type of adapter card.

SDLC ADAPTER CARD

- Tests receive control entry when alternate buffer A is full.
- Tests receive control entry when alternate buffer B is full.
- Tests alternate buffer swapping.

BSC/S-S ADAPTER CARD – BSC ONLY

- Adapter is placed in wrap, transmit, receive, and EBCDIC modes. Four sync characters are transmitted. Input request is not serviced; then tests:
  1. Set, read, reset of basic status bit 1 (output request).
  2. Set of adapter status bit 7 (adapter in sync).
  3. Set of basic status bit 0 (input request).
  4. Set of basic status bit 4 (exception).
  5. Set, read, reset of adapter status bit 0 (overrun).

Routine 0F. The tests are different depending on the type of adapter card.

SDLC ADAPTER CARD

- Tests FCS error detection and end flag recognition.
- Tests good FCS and end flag recognition.

BSC/S-S ADAPTER CARD – BSC ONLY

- Adapter is placed in wrap, inhibit zero insertion, transmit, receive, and SDLC modes. Two flag characters are wrapped; then tests:
  1. Set, read, reset of basic status bit 1 (output request).
  2. Set of basic status bit 4 (exception).
  3. Set, read, reset of SDLC frame.
  4. Set, read, reset of adapter status bit 3 (SDLC invalid sequence).

Routine 10. The tests are different depending on the type of adapter card.

SDLC ADAPTER CARD

- Tests NRZI transmit and receive.

BSC/S-S ADAPTER CARD – S-S ONLY

- Adapter is placed in wrap, transmit, and receive modes. Two data characters are wrapped; then tests:
  1. Set, read, reset of adapter status bit 0 (overrun).
  2. Set, read of basic status bit 0 (input request).
  3. Set, read of basic status bit 1 (output request).
  4. Set, read of basic status bit 4 (exception).

Routine 11. The tests are different depending on the type of adapter card.

SDLC ADAPTER CARD

- Tests receive data counter.
- Tests receive adapter counter.

BSC/S-S ADAPTER CARD – S-S ONLY

- Adapter is placed in wrap, transmit, and receive modes; then tests:
  1. Set, read of basic status bit 7 (interrupt request).
  2. Set, read of basic status bit 0 (input request).
  3. Set, read of basic status bit 1 (output request).
  4. Set, read of basic status bit 4 (exception).
  5. Set, read, reset of adapter status bit 5 (invalid character).

Routine 12. The tests are different depending on the type of adapter card.

SDLC ADAPTER CARD

- Tests that FCS is transmitted and received correctly when last bit is an inserted zero

BSC/S-S ADAPTER CARD – BSC ONLY

- Adapter is placed in wrap, receive, SDLC, and 6-bit modes; then tests:
  1. Set of basic status bit 4 (exception).
  2. Set, read, reset of adapter status bit 3 (SDLC invalid sequence).

Routine 13. The tests are different depending on the type of adapter card.

SDLC ADAPTER CARD

- Tests that only hex 7E is decoded as flag.
- Tests ability to exit continuous flag mode and transmit leading pads.
- Tests that invalid sequence is not detected when adapter is not in sync.
- Tests remaining reset conditions.

BSC/S-S ADAPTER CARD – BSC ONLY

- Adapter is placed in wrap, receive, SDLC, and inhibit zero insertion modes. Transmit buffer is loaded with an SDLC flag character on first output request, inhibit zero insertion mode is set again. Then tests:
  1. Set of basic status bit 1 (output request).
  2. Set of basic status bit 4 (exception).
  3. Set of adapter in sync and SDLC flag.
  4. Set and reset of continuous character transmit mode.

Routine 14. Tests the following adapter card.

BSC/S-S ADAPTER CARD – S-S ONLY

- Adapter is placed in wrap, receive, and break modes; then tests:
  1. Set, read of exception and interrupt request.
  2. Set, read, and reset of adapter status bit 6 (break byte detected).

Routine 15. Tests the following adapter card.

SDLC ADAPTER CARD

This routine sets up and issues a call to function definition module (FDM) with a function request '09'. The FDM return status is tested for return complete without error. The function request '09' causes a adapter card data wrap test to occur.

CA212 Device Tests (Routines 16 and Higher)

The CA offline device routines (16 and up) test communications feature hardware other than the adapter card.

Routine 16, EIA/V.35/X.21 (Nonswitched) Card Wrap. External data wrapping is performed at either the EIA/V.35/X.21 (nonswitched) cards or at the external IBM modem using the local test line. The physical data wrap location is dependent on the wrap jumper position on the EIA/V.35/X.21 (nonswitched) cards.

Examples: If the wrap jumper is set for internal wrapping on the EIA card, data wrap testing is performed on the EIA card. If the wrap jumper is set for external wrapping, data wrap testing is performed at the external IBM modem.

Caution: A modem, X.21 DCE, or direct-connect system must be connected to the 8100 under test.

Routine 18, Loop Adapter. Tests the loop adapter connection lines and loop adapter card. The driver lines are activated from the SDLC adapter card and then the loop adapter card is checked for the proper response. Then five data paths within the loop card are tested by setting three control lines (data rate select, local test, and new sync) and performing a test FDM data wrap through function request 'OD'.

Note: *At CSU time, a loop wrap plug is installed at the end of the loop cable(s) to wrap test the cables.*

Routine 19, Integrated Nonswitched Line Modem Interface Test Routine. Tests the interface lines to the integrated modem nonswitched line. The test checks for grounded or open pins by activating driver lines from the output side of the CA adapter and then checking for proper response through the local test interface. In addition, this routine checks for opens in the data lines by wrapping flags in continuous transmit mode and checking for adapter card dropping out of adapter sync.

Routine 20, Integrated Modem Switched Line and Auto Answer Interface Test Routine. Tests the interface lines to the integrated modem. The test checks for grounded or open pins by setting DTR, RTS, LTST, and Select Standby; then delays seven seconds for internal tests to execute. If the tests were successful, CTS and DSR are on. In addition, this routine checks for opens in the data lines by wrapping flags in continuous transmit mode and checking for adapter dropping out of sync.

Routine 21, DDSA. Tests the interface lines and internal operations of the DDSA. The test checks for grounded or open pins by activating driver lines from the output side of the adapter card and then checking for proper response through local test interface.

Routine 22, DDSA Internal Data Wrap. Sets local test and request to send, delays 50 ms, then checks for clear to send and data set ready. The routine then checks for opens in the data lines by an internal wrap flags subroutine.

Routine 25, Auto Answer Test. This routine enables the adapter and raises the Data Terminal Ready line so that the switched line modem (integrated or external EIA), auto answer circuits, and Data Access Arrangement can be tested. After the routine is started, a phone call must be made to the modem's telephone within 3 minutes using any available telephone. MI PA01 is displayed. If the call is successful, Data Set Ready is on and the originating telephone receives the (data) tone. If unsuccessful, error 25AA is reported.

Routine 51, Loop Test (1-Lobe). This routine is invoked if loop testing is requested. The main part of the routine only runs if the port is a one lobe loop.

This routine tests the one-lobe loop in five steps. It uses the three adapter lines (local test, data rate select, and new sync) to put the loop and loop station connector (LSC) relays in various states so that different data paths are tried. The results of the tests allow the program to localize problems. (See Figures CA475-1 and CA475-2 for data paths.)

The routine consists of five steps:

Step 1 – Test in internal active mode.

LTST inactive; DRS inactive; NS inactive.

Failure turns on C4 and terminates the routine.

Message 5125 is issued.

Step 2 – Test in external wrap mode.

LTST active; DRS active; NS active.

Failure turns on C5 and causes message 5126 to be issued whether or not a failure occurs in later steps.

Step 3 – Test with the line open (no connection).

LTST active; DRS active; NS inactive.

Loop open (signal path not connected) should not allow data to be transmitted around the loop. The wire test should fail in this step. Successful data transfer turns on C6, and, if preceding steps have passed, message 5127 is issued whether or not a failure occurs in later steps.

If there have been no previous errors, reset monitor mode on all stations.

Step 4 – Test in normal mode 1.

LTST inactive; DRS active; NS active.

On success: With no previous errors, go to step 5. If previous errors, issue message and end.

On failure: Set C7.

If previous error, issue error message and end.

If there was a RLSD or wire error and there was no previous error, attempt monitor mode recovery (MMR)

If MMR is successful, SET C7 = 0, address of monitor mode station in SA, and issue message 5129.

If MMR is not successful, try to find any beaconing station address and issue message 5128 with SA = beaconing station address or SA = 0 if no beaconing station; then end.

Step 5 — Test in normal mode 2.

LTST inactive; DRS active; NS inactive.

If successful, the routine exits so that the PA00 message is outputted.

A failure causes message 5135, but no bit is turned on in the C-flag byte.

Note: *C1 through C7 are the bits of the first byte of the extended status.*

MONITOR MODE RECOVERY

Failure in normal mode (RLSD or wire error). A pointer is set to the first station on loop.

The adapter is opened in the internal active mode to avoid a loop error. If there is an adapter level error, the routine is terminated. If there is no failure the loop is activated, and the first station in the configuration list is put in monitor mode. A 5-second wait allows any beaconing station to stop.

The loop is then opened normally to check if the failure is corrected. If there is no failure, the recovery was successful and control is returned to the invoking routine with the station that caused the failure left in monitor mode. If the failure is not corrected, the monitor mode is reset and the above procedure is repeated using the next station in the configuration list.

If there is still a failure after all the stations have been tried, monitor mode recovery is not successful and control is returned to the invoking routine.

Routine 52, Loop Test (2-lobe). This routine is invoked if loop testing is requested. It is executed if the configuration bits of the configuration table indicate that a two-lobe loop is attached to the SDLC port being tested. This routine tests the loop card and wire of the direct attached loop; if a problem is detected, an attempt is made to isolate the problem to the failing loop adapter lobe or station. If step 1 is successful, then all additional steps are run. If step 1 is unsuccessful, then the routine ends.

This routine runs until all configurations have been tested, except on a step 1 failure. A test is made in steps 5 and 6 to see if a wire test failure or receive line signal detect (RLSD) error is received from the loop. If no wire or RLSD error is received, the completion status byte for this configuration is set and the routine continues. If a wire or RLSD error is detected and there have been no errors in steps 1 through 4, then an attempt is made to locate the failing station by putting the stations into monitor mode, one station at a time. (Only two stations at a time can be in monitor mode.) If the failing station is located, that station is left in monitor mode to allow restoration of the loop and at the end of testing an error is reported. The address of the failing station is put into the error message buffer in the station on lobe 1 field (S1) or the station on lobe 2 field (S2). If monitor mode recovery was not successful, a check is made to see if any station is beaconing. If a beaconing station is detected, then the beaconing station address is put into the error message buffer in the station on lobe 1 field (S1) or the station on lobe 2 field (S2). After all configurations have been tested, a message is reported giving the results of the various tests and the condition in which the loop was left.

S1 = Address of station on lobe 1 left in monitor mode or beaconing.

S2 = Address of station on lobe 2 left in monitor mode or beaconing.

The routine consists of seven steps. The three adapter lines (LTST, DRS, and NS) have a total of eight states. Seven of these eight are used in this test. (See Figures CA475-1 and CA475-2 for data paths.)

Step 1 — Test with lobe 1 internal active, lobe 2 internal active.

LTST inactive; DRS inactive; NS inactive.

Internal active: internal wrap in the loop adapter but provides data to the loop.

On failure: set C4 = 1, close adapter, and end routine.
On success: set C4 = 0, continue.

Step 2 — Test with lobe 1 external wrap, lobe 2 external wrap.

LTST active; DRS active; NS active.

External wrap: wraps the data path within the loop station connector (LSC) and back to the loop adapter.

This verifies data flow integrity of the loop adapter to LSC cable and part of the LSC.

On failure, set C5 = 1, continue.
On success, set C5 = 0, continue.

Step 3 — Test with lobe 1 open — lobe 2 internal wrap.

LTST active; DRS active; NS inactive.

With lobe 1 open, data should not be transmitted around the loop. Successful data transfer is considered a failure.

On failure, set C6 = 1, continue.
On success, set C6 = 0, continue.

Step 4 — Test with lobe 1 internal wrap, lobe 2 open.

LTST active; DRS inactive; NS active.

Successful data transfer is considered a failure.

On failure, set C1 = 1, continue.
On success, set C1 = 0, continue.

If there have been no previous errors, reset monitor mode on all stations.

Step 5 — Test with lobe 1 normal, lobe 2 internal active.

LTST inactive; DRS active; NS inactive.

On failure, set C3 = 1, continue.
On success, set C3 = 0, continue.

If RLSD, beacon or timeout failure, and no error in step 2, 3, or 4, save the beaconing address in the error message and attempt monitor mode recovery as described in routine S1. The station is left in monitor mode.

If MMR successful, set C3 = 0, continue.
If MMR not successful, set C3 = 1, continue.

Step 6 — Test with lobe 1 internal active, lobe 2 normal.

LTST inactive; DRS inactive; NS active.

On failure, set C2 = 1, continue.
On success, set C2 = 1, continue.

If RLSD, beacon or timeout failure, and no error in steps 2, 3, or 4, save the beaconing address in the error message and attempt monitor mode recovery as described in routine 51. The station is left in monitor mode.

If MMR successful, set C2 = 0, continue.
If MMR not successful, set C2 = 0, continue.

Step 7 — Test with lobe 1 normal, lobe 2 normal.

LTST inactive; DRS active; NS active.

This is the normal state for the LSA.

If this passes and a following step fails, the station is left in normal mode.

On failure, set C7 = 1, continue.
On success, set C7 = 0, continue.

Routine 53, Remote Data Link (RDL) Test to any Group (Not Loop). This routine is executed only if the configuration bits in the configuration table indicate an SDLC Primary communications feature is installed on this port. This routine tests that it can communicate with at least one group on a data link line. The adapter card feature is opened using the open port function followed by the activate link function. If an error is returned, execution stops and the appropriate error message is displayed. The SDLC test command with an information field of 0 data bytes is issued to each group up to three times, until either all groups fail or a response is received from one group. An error is reported only if no group address responds to the test command.

Routine 61, EIA-Direct Connect Tests. Tests the EIA-direct connect feature and checks for proper control lines and data path. The expected physical wraps for this test are: (1) Transmit Data to Receive Data, (2) Request to Send to Clear to Send, and (3) Data Terminal Ready to Data Set Ready and Receive Line Signal Detect. Any other control lines are not tested and are a 'don't care' condition. A clock for the data test segment must be present from an 8100 internal source. These tests must be run when the EIA-direct connect cable is isolated from the direct connected host/device using the EIA-direct wrap plug.

Routine 63, EIA External Modem and V.35 Tests. Tests the EIA external modem, V.35 — external modem, or V.35 direct connect features for proper control lines and data path. The expected physical wraps for this test are: (1) Transmit Data to Receive Data, (2) Request to Send to Clear to Send and Receive Line Signal Detect, and (3) Data Terminal Ready to Data Set Ready. Any other control lines are not tested and are a 'don't care' condition.

A clock for the data test segment must be present from either an external source or an 8100 internal source. (EIA — External Modem test only.)

Note: *At CSU time, the data test segment is only run if the clock is from an 8100 internal source.*

These tests must be run when the EIA modem or V.35 communications cable is isolated from the external modem or host connection using the V.35 wrap plugs or the EIA modem cable test switch.

Routine 64, Modem Analyzer. The tests are different depending on the type of adapter card.

SDLC ADAPTER CARD

This auxiliary routine is used to isolate defective modems by gathering and reporting information to you.

This routine performs four tasks:

1. Reset all driver lines, read the receive lines, and report the state of these lines.
2. Raise DTR and DRS, and report receive line status.
3. Raise LT, DTR, and DRS, and report receive line status.
4. Raise LT, DTR, DRS, RTS, and report receive line status.

After each task is complete, the information is displayed on the MD; enter a 'C' to continue the test.

The message format for tasks 1—4 is:

PA01, 0506, 0822

PA02, 0506, 0822

PA03, 0506, 0822

PA04, 0506, 0822

where:

00 = Not active.

05 = CTS

06 = DSR

08 = RLSD

22 = RI

BSC/S-S ADAPTER CARD

This auxiliary routine is used to isolate defective modems by gathering and reporting information to you.

This routine performs four tasks:

1. Set data rate select and display control line status.
2. Set data terminal ready and display control line status.
3. Set data terminal ready and local test, then display control line status.
4. Set DTR, LT, and RTS, and then report receive line status.

After each task is complete, the information is displayed on the MD; enter a "B" to continue the test.

The message format for the four tasks is:

PA01, 0506, 0822

PA02, 0506, 0822

PA03, 0506, 0822

PA04, 0506, 0822

Where:

00	=	Not active.
05	=	CTS
06	=	DSR
08	=	RLSD
22	=	RI

Routine 66, DDS External Data Wrap. Sets request to send and not local test, delays 50 ms, then checks for clear to send and data set ready. The routine then checks for opens in the data lines by an external wrap flags subroutine. This test must be run with the DDS cable switch in the TEST position.

Routine 67, X.21 (Nonswitched) External Data Wrap 1. This routine performs a data path check external to the X.21 (nonswitched) card by using the wrap capability of the X.21 cable Test-Operate switch. This test must be run with the X.21 cable switch in the Test position.

This routine performs the following:

– Sets DTR and RTS on
– Checks for DSR and CTS on
– Sends data and receives data
– Compares data.

Note: *Local test line is not on.*

Routine 68, X.21 (Nonswitched) External Data Wrap 2. This routine is a continuation of Routine 67. This routine checks specific control lines and the data path. It reports those specific lines in error. The local test line is not on.

Routine 71, SDLC Secondary Link Test. This manually selected routine is used in an SDLC data link environment. A primary station (host) sends link tests (Routine 53 if an 8100), and a secondary station using Routine 71 counts the number of successful transmissions. When a link test is received from the primary station, the count is incremented and displayed. The routine loops until the first error is detected or until terminated by the user.

The host or controller must send SDLC link test ('F3') commands to the 8130/8140 Processor. Coordination between the two sites is required for the start and end of test.

Note: *This test requires manual termination after receiving all SDLC link test commands. Error 7122 (idle timeout) occurs if not terminated within 20 seconds of transmission completion of all SDLC link test commands.*

MANUAL INTERVENTION STOP

PA01 XXXX Link tests have been executed, where XXXX is the number of link tests (decimal) executed or received.

Routine 72, Data Link Loop – Poll Test. Is run to a 384X loop. The adapter is opened and put in diagnostic mode. This is done three times to insure that diagnostic mode is set. Next a link test is issued. If successful, message PA01 is issued (loop normal) and the routine ends. If the link test is unsuccessful, then message PA02 (test failed) is issued and the routine ends.

This routine is normally run with looping option bit equal to 1. This permits the link test to keep the line ready indicators of the terminals on the data link attached loop active.

MANUAL INTERVENTION STOPS

PA01 Loop normal, polling initiated

PA02 Test failed, polling initiated

Routine 73, Loop Relay Pick Test. This manually selectable routine tests the LSC relays and relay pick circuits. The routine cycles through three states in which you can measure the relay voltages at loop. Loop test tool PN 1657410 is attached to the LSA. The routine goes into the following steps for 10 seconds per step.

	Control Lines			Relay L1		Relay L2	
	LTST	MMS	NS	R1	R2	R1	R2
Step 1	1	1	1	off	off	on	off
Step 2	1	0	0	on	off	off	off
Step 3	0	0	1	on	on	on	on

Legend:

LTST – Local test

MMS – Monitor mode select

NS – New sync

The test setup procedure is described in CA653. You can check each relay to see that it is picking properly.

Routine 75, Group Analysis. Isolates intermittent errors and creates a statistical report. It is run to a data link or direct attached loop. When started, manual intervention stop 'PA01' is displayed indicating Enter Count. The count entered is used as the number of times the data is sent to a group. If 'DEF' is entered, a default count of 100 is assumed. A second manual intervention stop, 'PA02', is then displayed indicating Enter Data. The data entered, up to 31 characters of EBCDIC data, is repeated to fill the transmit buffer with 254 bytes of data. If 'DEF' is entered, the default pattern hex 1B005555AAAA2D2DFFFF is used.

The adapter is opened (failure causes error 7521) and is followed by activate link. The configuration table is then searched to get a list of station addresses to be tested.

If the station is a 384X, the configure command sets the device to 'set wrap' mode. If the station is other than a 384X, a disconnect command is issued to the first station and retried up to 2 times. If a correct response is received, then this station's address is put into the polling list. This ensures that the station is attached, is powered on, and has an available buffer. If communication cannot be established, this station is ignored and the above sequence is followed again until an attempt has been made to communicate with all stations attached to this adapter. If no stations respond, then error 7523 is issued. If there are more than 80 stations, then error 75FE is issued.

Next, for each entry in the polling list, a link test with 254 data bytes is issued to the station. For 384X, an alternate link test is issued so the 384X can handle a link test with data. Then 251 bytes are sent. If on the first pass the link test is successful but no data is returned, the link test is repeated with a 31-byte message. If this works, a flag is set and a 31-byte message is used to that station for the remainder of the routine.

The above sequences are followed until all entries in the following list have been transmitted the specified number of messages.

For each message, the appropriate counts are incremented. If a response has been received, the data is checked. If a response was not received and there was a FCS error, that count is incremented. If a positive response was not received but there was no frame check sequence error, then the timeout count is incremented.

For the 384X, the data returned is repetitions of the first byte sent.

When the messages have all been sent, the message completion statistics for each group are displayed using the manual intervention without response '03' display.

Note: *Enter "B" to continue after the stop or data entry.*

MANUAL INTERVENTION STOPS (OFFLINE)

PA01 Enter count between 1 and 9999; default = 100.

PA02 Enter data up to 31 characters; default data = hex 1B005555AAAA2D2DFFFF

PA03 This MI displays the statistical data provided by Routine 75. The format is as follows:

PA03 STATION = XX

MSG —— ERRORS ——

SNT FCS T/O DATA

000 000 000 000

Where:

XX	=	Station address
MSGSNT	=	Message sent count
FCS	=	Frame check sequence error count
T/O	=	Time out error count
DATA	=	Data compare error count

MANUAL INTERVENTION STOPS (DPCX)

PA01 Enter count between 1 and 999; default = 100.

PA02 Enter data up to 39 characters; default data = hex 00007555AAAA2D2DFFFF

PA03 SA00 MSGC TOFC DATA (This is an analysis report.)

SA	= Station address
MSGC	= Message sent count
TO	= Time out error count
FC	= Frame check error count
DATA	= Data compare error count

Routine 76, Loop Beacon and Ordinal Sequence Test. Tests the ability of each station on a directly attached loop to set and reset the carrier. It tests the ability of each station to beacon, and, if successful, generates an ordinal list of the stations on the loop.

The adapter card is opened (failure causes error 7621) followed by an activate link. The station addresses are obtained from the configuration table. A disconnect command is issued to each station; if no error is received, its address is put into the polling list. If no response is received after two retries, no polling list entry is made. This sequence is repeated until each station in the configuration table has been tested and put into the polling list or bypassed as receiving no response. If no station responds, then error 7623 is issued. If more than 80 stations respond, then error 76FE is issued.

Each station in the polling list is then configured to drop carrier. If no response results from dropping the carrier, then the station address is stored in the table. If a station then beacons, the address of the beaconing station is stored in the table. (This is the next station on the loop after the one which dropped the carrier.) If RLSD was received (indicates last station on the loop) an 'FF' is saved in the table. If a timeout was received, a '00' is saved in the table. A link test is sent to the station and, if successful, the station address is stored in the table. If unsuccessful, then the upstream station failed to beacon and a '00' is stored in the table.

The station is then configured to reset beacon, and a link test with no data is issued to that station to insure that the station is in normal mode. If the link test fails, error 7643 is issued.

The loop adapter lines are then used to drop carrier from the loop adapter. This should cause the first station on the loop to beacon. The address of the station responding is saved in a table. Then the adapter is reset by being closed.

When all stations in the list have been exercised, the sequence of stations as they are on the lobe is displayed using the manual intervention (MI) number 'PA05' and the MI without response function of the FCS. When errors are received which makes it difficult to interpret the sequence, the entire list of station addresses tested is displayed including their responses. This function is provided using the 'PA04' display. Stations having a good beacon response show the beaconing address; those with failures show "00" for no response, 'FF' for RLSD response, and the station address if the carrier failed to drop.

MANUAL INTERVENTION STOPS (OFFLINE)

PA04 SABA SABA SABA This MI is used to display the results of accumulating an ordinal sequence of the stations on the loop when errors are received which make it difficult to interrupt the sequence.

Where:

SA	=	Station address which was configured to drop carrier
	=	00 for loop adapter card
BA	=	Beaconing stations address
	=	FF if RLSD
	=	SA for failure to drop carrier
	=	00 if no response

PA05 SEQ = SA, SA, SA Ordinal sequence display.

Where:

SA = Station address in ordinal sequence

MANUAL INTERVENTION STOPS (DPCX)

PA05 SABA SABA SABA This MI is used to display the results of accumulating an ordinal sequence of the stations on the loop when errors are received, which make it difficult to interrupt the sequence.

Where:

SA	=	Station address which was configured to drop carrier
	=	00 for loop adapter card
BA	=	Beaconing station address
	=	FF if RLSD
	=	SA for failure to drop carrier
	=	00 if no response

PA06 SA00 SA00 SA00 Ordinal sequence display.

Where:

SA	=	Station address in ordinal sequence

Routine 77, BSC Link Test – Requestor. Initiates (requests) a BSC link test from the 8100 system to an upline or a downline unit that is capable of responding to a test message. Routine options provide for the selection of BSC test type 00 or type 01. These are similar to the BTAM request for test (RFT) types 00 or 01.

XX = 00 (BSC Test Type 00)

The 8100 sends an 80-byte test message (A through Z, 0 through 9) YY times, to the responding device; the device acknowledges (ACK) if a good message is received or sends an NAK if there is a data check. This request accumulates errors encountered for presentation at the end of the test (message PA05).

XX = 01 (BSC Test Type 01)

The 8100 sends an 80-byte test message (A through Z, 0 through 9) to the responding device; the device acknowledges (ACK) the test message and then retransmits the message to the 8100 YY times. If error conditions prevail, the appropriate error response is posted. This test accumulates errors encountered for presentation at the end of the test (message PA06).

INVOCATION

Level-2 addressing is required in the standard invocation procedure. (Refer to CA202.) The next normal message to be displayed is the manual intervention message PA01 asking for the XX and YY values to be entered.

Note: *The remote device must be ready to respond (a responder test must be initiated) at the same time this test is invoked.*

MI MESSAGES

PA01 Enter XX and YY

XX = 00 or 01

YY = 01 to 99

This message prompts the invoking device to enter the XX and YY parameters.

PA02 Entry error

Invalid XX and/or YY entered. To retry, enter "C"

Go forward and reenter.

This message informs the invoking device that the XX and YY values were incorrectly entered. After this message, MI message PA01 is reissued to receive XX and YY parameters.

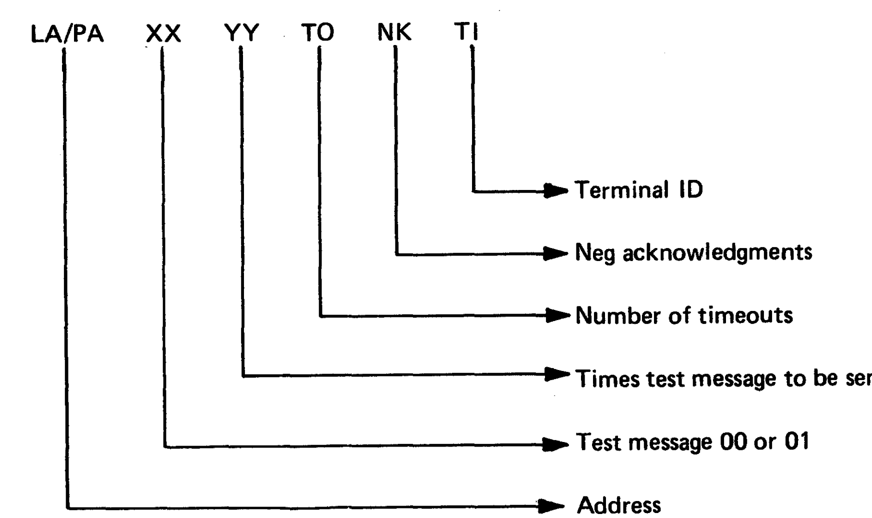
PA03 Waiting for connection to Responder; maximum wait is three minutes.

This message informs the invoking device that 20 timeouts have occurred. These timeouts are logged on a poll, write select, adprep, bidprep, or writebid command. After this message is issued three times, error message 15 is issued and the routine is cancelled.

PA05 XMIT RESULTS

PA XXYY TO LD TI

TRANSMIT OUTPUT MESSAGE



PA06 RECEIVE RESULTS

PA XXYY TO LD DC

RECEIVE OUTPUT MESSAGE

LA/PA XX YY TO LD DC

- DC → Data check count
- LD → Lost data count
- TO → Number of timeouts
- YY → Times test message to be received
- XX → Test message 00 or 01
- LA/PA → Address

Data Check Count:	The number of FCS errors accumulated while in the receive data loop.
Lost Data Count:	The number of compare errors accumulated during the data loop of requester test 01 only. It compares the data sent to the data received from the responder.
Timeouts:	The number of timeouts that occur during the transmit and receive data loops. The timeout counted is a 3-second timeout that has occurred without the required syn syn characters being received (for read) or a valid response received.

ERROR MESSAGES: See also CA240.

Error Messages are written to the invoking device in the following form: PA2E RRNN FRS1 S2S3 S4S5

where:

PA	=	Physical address of the level-2 device
2	=	Address level 2
E	=	Hex E
RR	=	Routine number (77 or 78)
NN	=	Error number
FR	=	Function request code
SX	=	Bytes of sense information

ERROR NUMBER (NN)

NN	Meaning
01	MCPC error
10	INV BSTAT error
11	DCE error
12	Halt error
13	Timeout error
14	Bad data write text/header
15	Connect timeout
16	Write header (routine 77) 10 NAKS or T.O. received
17	Write header and TXT (routine 77) 10 NAKS or T.O. received
18	Read RFT message (routine 78) 10 NAKS or T.O. sent
1A	Invalid RFT header received (routine 78)
1C	Overrun or underrun
99	Configuration error

FUNCTION REQUEST (FR)

FR (Hex)	Function
00	Enable/set mode
01	Sense
03	Send ACK-0 and read
04	Bid prep
0C	Write bid
10	Write EOT
14	Disable
23	Send ACK-1 and read
24	Poll
28	Write select
4C	Adprep
53	Delay 2 seconds
62	Write SOH ETX expect ACK-1 or data
72	Write STX ETX expect ACK-1 or data

SENSE FIELDS (SX)

S1 BSTAT

Bit 0	Input request
Bit 1	Output request
Bit 2	DCE interrupt
Bit 3	Timer interrupt
Bit 4	Exception
Bit 5	MC/PC
Bit 6	Enable/disable
Bit 7	Interrupt request

S2 MSTAT

Bit 0	Data set ready
Bit 1	Clear to send
Bit 2	RLSD
Bit 3	Ring indicator
Bit 4	DSR transition
Bit 5	Reserved
Bit 6	RLSD transition
Bit 7	CTS transition

S3 MCTRL

Bit 0	DTR/connect data set to line
Bit 1	Request to send
Bit 2	Wrap
Bit 3	Test
Bit 4	Select standby
Bit 5	Select half speed
Bit 6	New sync
Bit 7	DCE interrupt disable

S4 ASTAT

Bit 0	Overrun
Bit 1	Underrun
Bit 2	Receive clock running (N/A)
Bit 3	SDLC frame sequence (N/A)
Bit 4	SDLC frame (N/A)
Bit 5	Invalid character (N/A)
Bit 6	Break byte detected (N/A)
Bit 7	Adapter in sync

S5 A CTRL

Bit 0	Receive mode
Bit 1	Transmit mode
Bit 2	Inhibit zero insertion
Bit 3	Mode select*
Bit 4	Mode select*
Bit 5	Code length**
Bit 6	Code length**
Bit 7	NRZI

***Mode Select**

00	Auto
01	EBCDIC
10	ASCII
11	SDLC

****Code Length**

00	8-bit
01	6-bit
10	7-bit
11	5-bit

Routine 78, BSC Link Test — Responder. Responds to a BSC link test message from either another 8100 System (see Routine 77) or another unit that is capable of generating a request for test (RFT) Type 00 or 01 message. Responses by this routine are automatic.

For BSC test type 00, this routine receives the test message YY times from the requester, up to 250 bytes, and acknowledges (ACK) if a good message is received or sends an NAK if there is a data check.

For BSC test type 01, this routine receives the test message from the requester, up to 250 bytes, and acknowledges (ACK) if a good message is received or sends an NAK if there is a data check. Then the test message is retransmitted to the requesting device YY times.

INVOCATION

Level-2 addressing is required in the standard invocation procedure (refer to CP610 in Chapter 2 and CA202). After standard test invocation, the next normal message to be displayed is PA04 which asks if the requester is loaded and ready. When the answer to this question is yes, press Forward, then Enter to run the test. The next normal message to be displayed is either an abnormal termination message or the normal end of test message.

Note: *The remote device must be ready to request (a requester test must be initiated) at the same time this test is invoked.*

MI MESSAGES

PA03 Waiting for connection to requester ; maximum wait is 3 minutes.

This message is to inform the invoking device that 20 timeouts have occurred. These timeouts are logged on a poll, write select, adprep, bidprep, or writebid command. After this message is issued three times, error message 15 is issued and the routine is cancelled.

PA04 When requester is ready, enter "C" to continue.

This message is issued to inform the invoking device that the requester should be loaded and ready before continuing.

PA05 XMIT RESULTS

PA XXYY TO LD TI

TRANSMIT OUTPUT MESSAGE

LA/PA XX YY TO NK TI

- TI → Terminal ID
- NK → Neg acknowledgments
- TO → Number of timeouts
- YY → Times test message to be sent
- XX → Test message 00 or 01
- LA/PA → Address

PA06 RECEIVE RESULTS

PA XXYY TO LD DC

RECEIVE OUTPUT MESSAGE

LA/PA XX YY TO LD DC

- DC → Data check count
- LD → Lost data count
- TO → Number of timeouts
- YY → Times test message to be received
- XX → Test message 00 or 01
- LA/PA → Address

Data Check Count: The number of FCS errors accumulated while in the receive data loop.

Lost Data Count: The number of compare errors accumulated during the data loop of requester test 01 only. It compares the data sent to the data received from the responder.

Timeouts: The number of timeouts that occur during the transmit and receive data loops. The timeout counted is a 3-second timeout that has occurred without the required syn syn characters being received (for read) or a valid response received.

ERROR MESSAGES: See Routine 77 Error messages.

Routine 79, 2741 All Characters Test. Sends a line of characters to the 2741 under test. The test consists of:

1. MI PA06 (at invoking device)
2. Two carrier returns
3. Routine identification line
4. One carrier return
5. All characters line
6. One carrier return

MI MESSAGES (AT THE INVOKING DEVICE)

PA06 — (nonswitched line) enter "9". Switch the device under test (DUT) to Local. Switch to Communicate. Press Carrier Return.

TEST MESSAGES (AT THE 2741 UNDER TEST)

ROUTINE 79 ALL CHARACTERS TEST

0123456789 abcdefghijklmnopqrstuvwxyz

ABCDEFGHIJKLMNOPQRSTUVWXYZ&*()_+-:?—=|;',./

ERROR MESSAGES (AT THE INVOKING DEVICE OR 2741). See CA240.

Routine 80, 2741 Tilt Rotate Twist. Sends a line of tilt, rotate, and twist actions to the 2741 under test. The test consists of:

1. MI PA06 (at invoking device)
2. Two carrier returns
3. Routine identification line
4. One carrier return
5. Tilt, rotate, and twist line
6. One carrier return

MI MESSAGES (AT THE INVOKING DEVICE)

PA06 — (Nonswitched line) enter "9" Switch the device under test (DUT) to Local. Switch to Communicate. Press Carrier Return.

TEST MESSAGES (AT THE 2741 UNDER TEST)

ROUTINE 80 TILT ROTATE TWIST TEST

_9_9_9_9_9_9_9_9_9_9_9_9_9_9_9

ERROR MESSAGES (AT THE INVOKING DEVICE OR 2741). See CA240.

Routine 81, 2741 Special Function Test. Sends test lines with backspaces, underscoring, line feeds, and print characters. The test consists of:

1. MI PA01 or PA06 (at invoking device)
2. Two carrier returns
3. Routine identification line
4. One carrier return
5. Test line backspaces and the underscoring of the '6'
6. One line feed
7. One carrier return
8. A line with '1'
9. One line feed
10. A line with '2'
11. One line feed
12. A line with '3 6 9'
13. One carrier return

MI MESSAGES (AT THE INVOKING DEVICE)

PA06 – (Nonswitched line) enter "9". Switch the device under test (DUT) to Local. Switch to Communicate. Press Carrier Return.

TEST MESSAGES (AT THE 2741 UNDER TEST)

ROUTINE 81 SPECIAL FUNCTION TEST

12345<u>6</u>7890

1

2

3 6 9

ERROR MESSAGES (AT THE INVOKING DEVICE OR 2741). See CA240.

Routine 82, 2741 Read Test. Receives or reads a line of all characters from the 2741 under test. The test consists of:

1. MI PA06 (at invoking device)
2. Two carrier returns
3. Routine identification line
4. One carrier return
5. MI PA02
6. One carrier return

MI MESSAGES (AT THE INVOKING DEVICE)

PA06 – (Nonswitched line) enter "9". Switch the device under test (DUT) to Local. Switch to Communicate. Press Carrier Return.

TEST MESSAGES (AT THE 2741 UNDER TEST)

PA01 – Key in this line.

0123456789ABCDEFGHIJKLMNOPQRSTUVWXYZ
Then press carrier return.

ERROR MESSAGES (AT THE INVOKING DEVICE OR 2741). See CA240.

Routine 83, 2741 Echo Test. Receives a block of test characters from the 2741 under test and echoes them back to the 2741 under test. The test consists of:

1. MI PA06 (at invoking device)
2. Two carrier returns
3. Routine identification line
4. One carrier return
5. MI PA03
6. One carrier return
7. Block of test characters (as input from 2741)
8. One carrier return

MI MESSAGES (AT THE INVOKING DEVICE)

PA06 – (Nonswitched line) enter "9" Switch the device under test (DUT) to Local. Switch to Communicate. Press Carrier Return.

MI MESSAGES (AT THE 2741 UNDER TEST)

PA03 – Key in 1–128 characters
Then press carrier return
System will repeat.

TEST MESSAGES (AT THE 2741 UNDER TEST)

Characters input at MI PA03 are echoed back to the 2741 under test.

ERROR MESSAGES (AT THE INVOKING DEVICE OR 2741). See CA240.

Routine 84, 2741 Attention Key Test.

Caution: This test is valid only for a four-wire nonswitched line configuration.

Receives a block of test characters from the 2741 under test and echoes them back to the 2741 under test. The test consists of:

1. MI PA06 (at invoking device)
2. Two carrier returns
3. Routine identification line
4. One carrier return
5. MI PA04
6. One carrier return
7. Interruptible line(s)
8. One carrier return

MI MESSAGES (AT THE INVOKING DEVICE)

PA06 — (Nonswitched line) enter "9" Switch the device under test (DUT) to Local. Switch to Communicate. Press Carrier Return.

MI MESSAGES (AT THE 2741 UNDER TEST)

PA04 — Press the attention key while the next line is printing.

INTERRUPTIBLE LINES

123456789123456789123456789123456789

123456789123456789123456789123456789

123456789123456789123456789123456789

12345678912345678912

ERROR MESSAGES (AT THE INVOKING DEVICE OR 2741). See CA240.

Routine 85, TTY Auxiliary Line Test. Sends a block of test characters to the TTY under test. The routine sends to the invoking device:

1. MI PA01
2. MI PA02

The routine reads a test message from MI PA02, and sends to the TTY device:

1. Two carrier returns
2. Routine identification line
3. One carrier return
4. The test message from MI PA02
5. One carrier return

MI MESSAGES (AT THE INVOKING DEVICE)

PA01 — Press the control and E keys, then the control and S keys at the DUT.

PA02 — At the invoking device, key in 1—16 characters, then press Carrier Return, or press the Enter key on the MD.

TEST MESSAGES (AT THE TTY DEVICE)

ROUTINE 85 AUXILIARY LINE TEST

Test message (characters from MI PA02)

ERROR MESSAGES (AT THE INVOKING DEVICE OR 2741). See CA240.

Routine 86, TTY Auxiliary Echo Test. Receives a block of test characters from the TTY under test and echoes them back to the TTY DUT. The test consists of:

1. MI PA01 (at the invoking device)
2. Two carrier returns
3. Routine identification line
4. One carrier return
5. Test message from MI PA03
6. One carrier return

MI MESSAGES (AT THE INVOKING DEVICE)

PA01 — Press the control and E keys, then the control and S keys at the DUT.

MI MESSAGES (AT THE TTY DEVICE)

PA02 — Key in 1—80 characters, then press the CNTL and S keys.

TEST MESSAGES (AT THE TTY DEVICE)

The test message is the characters from the MI PA02.

ERROR MESSAGES (AT THE INVOKING OR TTY DEVICE). See CA240.

Routine 87, 2741 Auxiliary Line Test. Sends a line of test characters to the 2741 under test. The routine sends to the invoking device:

1. MI PA06
2. MI PA05

The routine reads a test message from MI PA05, and sends to the 2741 device:

1. Two carrier returns
2. Routine identification line
3. One carrier return
4. The test message from MI PA05
5. One carrier return

MI MESSAGES (AT THE INVOKING DEVICE)

PA05 — Key in 1—16 characters. The system repeats the characters to device under test.

PA06 — (Nonswitched line) enter "9". Switch the device under test (DUT) to Local. Switch to Communicate. Press Carrier Return.

MI MESSAGES (AT THE 2741 UNDER TEST)

ROUTINE 87 — AUXILIARY LINE TEST

Test message (characters from MI PA05)

ERROR MESSAGES (AT THE INVOKING DEVICE OR 2741). See CA240.

Routine 88, One Loop Poll Test. Is run to a one-lobe LSA. The adapter is opened in normal mode. If successful, message MI01 is issued (loop normal). The loop is activated. If unsuccessful, the adapter is then opened in the internal active mode (internal wrap, but data still on loop). If successful in internal active mode, message MI02 is issued (loop bypassed). Then the link is activated so that each station is polled (all station address hex FF). If unsuccessful in opening in internal active mode, then error message 8825 is issued. To keep the line ready indicator on, this routine should be run with the looping bit on so that the stations are polled at least every 8 seconds.

MANUAL INTERVENTION STOPS

PA01 — Loop normal
Polling initiated

PA02 — Loop bypassed
Polling initiated

PA04 — (DPCX) Normal mode wrap failed.
Internal active wrap is set.

Routine 89, Two-Lobe Loop Poll Test. Is run to a two-lobe LSA. The adapter is opened in normal mode. If successful, message MI10 is issued (loop normal). The link is then activated and the routine ends.

If unsuccessful, the adapter is then opened with lobe 1 in internal active mode and lobe 2 in normal mode. If successful, then message MI02 is issued and the link is activated so that each station is polled (all station address hex FF).

If unsuccessful, the adapter is opened with lobe 1 in normal mode and lobe 2 in internal active mode. If successful, message MI03 is issued and the link is activated.

If unsuccessful, the adapter is opened with both lobes in internal active mode. If successful, message MI04 is issued and the link is activated. If unsuccessful, error message 8925 is issued. Then the link is activated so that each station is polled at least every 8 seconds. To keep the line ready indicator on, this routine should be run with the looping bit on so that the stations are polled at least every 8 seconds.

MANUAL INTERVENTION STOPS

PA01 — Loop normal
Polling initiated

PA02 — Lobe 1 bypassed
Polling initiated

PA03 — Lobe 2 bypassed
Polling initiated

PA04 — 2 Lobe bypassed
Polling initiated

Routine 90, SDLC Test Command — No Data. Tests that a station responds to the SDLC test command. A Disconnect SDLC command is issued to the station under test. No check is made to see if this function succeeds. Next a link test (with no data) is issued to the station. If this function fails, error message 9031 is issued. The function is retried twice; if it succeeds on the retry, test message 90E0 is issued.

Routine 91, SDLC Test Command — With Data. Tests that the station responds to an SDLC test command with a data field. A Disconnect SDLC command is issued to the station under test. No check is made to determine if this function succeeds. Next a link test (with 254 data bytes of '1B005555AAAA2D2DFFFF' repeated) is sent to the station. If there is no test response, then error message 9131 is issued. If no data was returned, then a link test with 31 bytes of the data pattern is sent to the station. If the 31-byte link test fails, then error message 9131 is issued. If data was returned for either link test, it is checked and, if not correct, error message 9135 is issued.

Routine 92, Monitor Mode Test. (Loop stations only.) Determines if a loop station can go in and out of monitor mode. This routine first sends a link test with no data. If successful, it sets monitor mode and repeats the link test. If the test is successful, the setting of monitor mode has failed and error message 9234 is issued. If the link test in monitor mode fails, monitor mode is reset and the link test is rerun. If this fails, error message 9236 is issued. Test retry occurs twice; a success on retry causes a 92E0 error.

Routine 93, SDLC Test With User Data. This routine is the same as Routine 91. However, the information field data is supplied by the invoker. A Disconnect SDLC command is issued to the station under test. No check is made to determine if this function succeeds. Next, an MI PA02 stop is issued requesting from 1 to 31 bytes of data for transmission in the link test. If 'DEF' is entered at the MI stop, default data is used. The data is duplicated to 254 bytes. Next, the link test with 254 bytes of user data is issued to the station. If there is no test response, error message 9331 is issued. If the function did not fail but no data was returned, then a link test with 31 data bytes of the data pattern is issued to the station. If this function fails, error message 9331 is issued. If data was returned for either link test, it is compared and, if in error, error message 9335 is issued. Tests are retried two times. If successful, error message 93E0 is issued.

Note: *Enter "B" to continue after MI stop or data entry.*

MANUAL INTERVENTION STOPS (OFFLINE)

PA02 — Enter 1 to 31 characters of data.
Default = 1B005555AAAA2D2DFFFF

MANUAL INTERVENTION STOPS (DPCX)

PA02 — Enter 1 to 39 characters.
Default = hex 00007555AAAA2D2DFFFF.

Routine 94, Line Analysis. This routine sends a link test with user-supplied data to a station the number of times specified by the operator and then provides a statistical report to the operator. A Disconnect SDLC command is issued to the station under test. No check is made to determine if this function succeeds. Next an MI stop is issued requesting that a 1- to 4-digit numeric loop count be entered. Next, an MI stop is issued requesting 1 to 31 bytes of data for transmission in the link test. If either MI stop receives an invalid response, error message 94CE is issued. If 'DEF' is entered at either MI stop, default data/count is used. Next, the link test with 254 or 31 bytes of user data is issued. If this function fails, an error log counter is incremented. The link test is issued the specified number of times, and a statistical report is printed.

Note: *Enter "B" to continue after MI stop or data entry.*

MANUAL INTERVENTION STOPS (OFFLINE)

PA01 – Enter 1 to 9999 digit loop count.
Default = 100

PA02 – Enter 1 to 31 characters of data.
Default = 1B005555AAAA2D2DFFFF

PA03 – Address = SA
Messages Sent = XXXX
Link Failures = XXXX
Data Failures = XXXX
Where:
PA = Address
SA = Station address
XXXX = Decimal value

MANUAL INTERVENTION STOPS (DPCX)

PA01 – Enter 1 to 999 loop count.
Default = 100

PA02 – Enter 1 to 39 characters.
Default = hex 00007555AAAA2D2DFFFF

PA-3 – SA00 TTTT EEEE
Where:
PA = Address
SA = Station address
TTTT = Number of messages sent
EEEE = Number of failures

Routine 95, 384X SDLC Test Command. Performs a link test to the 384X, first with the 384X in wrap mode and then with wrap mode reset. The latter tests the loop attached to the 384X.

On error, each command is retried twice because the remote loop is subject to line hits and one such hit would not stop testing of the 384X. Any such line hits cause error message 95E0 (success with retry) to be issued if no other error has occurred.

First, a Configure command with the information byte indicating Set Wrap function is sent to the 384X. Failure causes error message 9536 to be issued. Then Set Diagnostic Mode Latch is issued to change 384X timeout to 1 second. Failure causes error message 9532 to be issued.

If the Set Diagnostic Mode was successful, an SDLC test command with a 0-byte information field is sent to the 384X. On failure, the wrap is reset and error message 9537 issued. If the SDLC test command receives the expected response, a Configure command with the information byte indicating a "reset wrap" function is sent to the 384X. Failure causes error message 9543 to be issued. If the reset wrap was successful, an SDLC test command with 0-byte information field is sent to the 384X. If the expected response to the SDLC test command was received, the routine ends successfully. If the retries also fail with errors, and if group timeout or beaconing is received during the SDLC test command, each station on the loop is placed in monitor mode. If the error is corrected when one of the stations is placed in monitor mode, that station is left in monitor mode and error message 9529, indicating the failing station, is reported. If the error condition does not stop when all stations have been placed in monitor mode, this test cannot isolate the failing component and error message 9531 is issued.

Routine 96, Remote Loop Data Transfer. Tests that the 384X can send long data messages. On error, each command is retried twice because the remote loop is subject to line hits and one such hit would not stop testing of the 384X. Any such line hits cause error message 96E0 (success with retry) to be issued if no other error has occurred. At the end of the routine, the 384X is cleared, resetting all of the configuration functions set by this routine.

First, a Set Wrap function is sent to the 384X. If this function fails, error message 9636 is issued.

Next, a Configure command with the information byte indicating set diagnostic mode is sent to the 384X. This causes the timeout limit to be set to 1 second instead of 30, speeding up the time of testing.

Five link-test commands with a 251-byte field is sent to the 384X, each time with different data: hex 00, 55, 2D, AA, and FF. All 251 bytes of the information field contain the same data. If a link error occurs, error message 9637 is issued.

The alternate link test command is used so that the 384X sends back the data from the SDLC test command. If this fails, error message 9638 is issued.

The data message received from the 384X is compared with the data sent. If it does not match, error message 9639 is issued. A data compare error is not retried.

The wrap is reset. If this fails, error message 9643 is issued.

The same five sets of SDLC test commands are issued again. Failure causes error message 9631, or, if the data does not match, causes error message 9635.

Routine 97, Configuration Self Test to 384X. Checks for a correct response to a Configure self-test command which is issued to the 384X under test. On error, each command is retried twice because the remote loop is subject to line hits and one such hit would not stop testing of the 384X. Any such line hits cause error message 97E0 (success with retry) to be issued if no other error has occurred.

First, a set wrap command is sent to the 384X; failure causes error message 9736 to be issued. Next, an SDLC Configure command indicating set diagnostic mode is sent to the 384X under test. Failure causes error message 9732 to be issued.

A Configure command with the information byte set to self test is issued to the 384X. If a response is not received within 5 seconds, the self test is retried twice. If the self test is still unsuccessful, error message 9745 is issued.

Routine 98, Beacon and Ordinal Sequences. Tests the ability of each station on a remote loop to set and reset the carrier. It tests the ability of each station to beacon, and, if successful, generates an ordinal list of the stations on the loop.

On error, each operation to the remote loop is retried twice so that a line hit is not interpreted as a station malfunction. If the retries are unsuccessful, the 384X or station being tested is reset.

The adapter is opened (failure causes error message 9821), followed by activate link. The Set Diagnostic Mode command is sent to lower the time for a timeout; this speeds up the execution time of the routine. Failure causes error message 9832 to be issued.

The addresses of the stations of the 384X to be tested are obtained from the configuration table. If no station addresses are in the configuration table, then error message 9820 is issued. A disconnect command is issued to each station. If no error is received, its address is put into a polling list. If no response is received, no polling list entry is made. This sequence is repeated until each station on the loop has been tested and put into the polling list or bypassed as receiving no response. If no stations respond, error message 9823 is issued; if more than 80 stations respond, error message 98FE is issued.

The 384X is sent to a configure-drop carrier. This should cause the first station on the loop to beacon. The address of the station beaconing is saved in a table. If a group timeout is received, then an FF is saved in the table; if an error is returned from the configure command, then a 00 is saved. Then the 384X is restored to its normal mode with a configure-restore beacon. This is sent three times without checking the return code. After waiting 5 seconds, a link test without data is sent to the 384X. If the link test fails, error message 9843 is issued.

The first station in the polling list is then configured to drop the carrier. If a station then beacons, the address of the beaconing station is saved in a table (this is the next station on the loop after the one which dropped carrier). If group timeout was received (for the last station on the loop), FF is saved in the table. If no configure response results from the dropping of carrier, SA is saved in the table.

The station is then configured to reset beacon. This is sent three times without checking the return code. The program waits 5 seconds. Then a link test with no data is issued to that station to ensure that the station is in normal mode. If the link test fails, error message 9843 is issued.

The above sequence is repeated for all stations in the poll list. When all stations in the list have been tested, the 384X is cleared. Then the sequence of stations as they are on the lobe is displayed using MI message PA05.

If the ordinal sequence cannot be determined due to errors, then the entire list of station addresses tested is displayed including their responses. This function is provided using MI message PA04. Stations having a good beacon response show the beaconing address. Those with failures show SA for no response and FF for group timeout response.

PA04 SA BA — This MI displays the results of accumulating an ordinal sequence of the stations on the loop, when errors are received which make it difficult to interpret the sequence.

SA = Station address configured to drop carrier
= 00 for 384X

BA = Beaconing stations address
= FF if group timeout
= 00 if no response

PA05 SEQ = SA, SA, SA — Ordinal sequence display

SA = Station addresses in ordinal sequence

Routine 99, Lobe Analysis. Isolates intermittent errors and creates a statistical report. This routine uses either user-supplied or default data and count for running a link test on the various stations in a group. This test is run for noise or data-dependent problems.

The routine comes to two manual intervention stops. It is then up to the invoker to either supply the count and data or to take the default values. At MI message PA01, the count field is entered. The count is the number of times the data is to be sent to each station (default = 100). At MI message PA02, the data field (up to 31 characters) is entered. The data field is the data to be sent to each station (default = 1B005555AAAA2D2DFFFF).

When the routine continues, the Set Diagnostic Mode command is sent to reduce the time for a timeout; this speeds up the execution time of the routine. Failure causes error message 9932 to be issued. Next, it sends an SDLC test command without data to the 384X. If the SDLC test command fails, error message 9931 is issued.

If the SDLC test command is successful, a disconnect command is sent to each station in the group. If the disconnect command fails, it is retried twice.

If the disconnect command is successful, the station is added to the polling list. Then SDLC test commands with the data specified are sent to each station in the polling list.

If no data was returned for the first successful test command, the byte count is set to 31, the test command is retried, and that value is used for that station for the rest of the run.

If the test command failed, the status is checked to find out if it was an FCS or timeout/error. The appropriate counter is then updated to reflect this error.

If the test command is successful, the data coming back from the station is compared with the data sent. If the data does not compare, a data error counter is incremented. MI message PA03 is issued to report statistical data.

MANUAL INTERVENTION STOPS

PA01 Enter 1 to 4 digit loop count

Default = 100

PA02 Enter 1 to 31 characters of data

Default = 1B005555AAAA2D2DFFFF

PA03 Station = XX

MSG	Errors		
SNT	FCS	T/O	Data
000	000	000	000

Where:

XX = Station address

MSGSNT = Message sent count

FCS = Frame check sequence error count

T/O = Time out error count

Data = Data compare error count

CA213 Link-Level Tests

The purpose of the CA feature link-level tests is to:

- Exercise basic communications from the 8130 or 8140 to another unit. That unit can be a host, peer, or any controller, station, or device attached to the processor.
- Exercise the link/loop communications line.
- Exercise the SDLC, BSC, and Start/Stop line disciplines.
- Provide an expected line discipline test for line monitoring.

Noté: *Unit or FRU isolation is NOT performed by link level tests (exceptions are Routines 51 and 52) for direct attached loop.*

Basic link/loop tests that run under MAP control are:

Line Discipline	Test Routines (See CA212)
SDLC	
• Data link, primary (only)	53
• Loop, direct attached (only)	51 (1 lobe) or 52 (2 lobe)

By line discipline, the following link-level tests are available:

Line Discipline	Test Routines (See CA212)
SDLC	
• Data link	
Primary	53, 75, 90, 91, 93, 94
Secondary	71
• Loop	
Direct-attached	75, 90, 91, 92, 93, 94
Data-link attached	95, 96, 99
BSC	77, 78
Start-Stop	
• 2741	79, 80, 81, 82, 83, 84, 87
• TTY	85, 86

Refer to CA202 for invocation procedure notes, and CA137 for testing procedure.

CA214 Customer Setup (CSU) Tests

There are 8100 communications tests which are run at customer setup (CSU) time. These tests are run by the customer after he has set up the 8100 system using the CSU procedures. These tests check out the 8100 communications hardware (logic and internal cables) and perform certain checks to IBM-supplied external cables.

The tests are invoked automatically from the CSU diskette using customer configuration data. The tests are a subset of the communication offline tests. While test descriptions and error numbers are similar to the offline tests (CA210), there are unique customer recovery action plans for CSU communications errors. Should a customer provide you with an error number received at CSU time, go to CA160 (Communications Fault Isolation). Tests 18, 61, and 63 are modified versions of the regular 8100 Communications tests.

Note: *You should NEVER attempt to maintain NOR diagnose the 8100 System using the CSU diskette and CSU loop wrap plug.*

The following routines are run at CSU time with the listed hardware.

Hardware	Test Routines	Notes
SDLC or BSC/S-S		1
Adapter card and EIA card (modem)	1–15, 63(M)	
SDLC or BSC/S-S		1
Adapter card and EIA card (direct connect)	1–15, 61(M)	
SDLC		1
Adapter card and V.35 card (modem or direct connect)	1–15, 63(M)	

Hardware	Test Routines	Notes
SDLC or BSC/S-S		1
Adapter card and DDS card	1–15, 22, 66	
SDLC adapter card and X.1 (nonswitched) card	1–15	1
SDLC or BSC/S-S		2
Adapter card and integrated modem (nonswitched line)	1–15, 19	
SDLC adapter card and integrated modem (switched line)	1–15, 20	2
SDLC adapter card and loop adapters, lobe 1 and lobe 2	1–15, 18(M)	1

Legend: (M) = Minor modifications to offline tests that result in reduced testing.

Notes:

1. *Required:*
   - *CSU diskette only.*
   - *External communications cable plugged into I/O panel.*
   - *Wrap plug plugged on cable; or cable switch in test position*
2. *No external connections required.*

CA215 Link/Loop Test Requirements

Testing on a data link/loop may vary depending on available hardware for a given physical address (PA).

Complete testing may be accomplished when all communications feature hardware is available at both the local and remote sites; this includes data link/loop cables installed to the DCE equipment or loop(s), and all stations/devices/controllers/hosts that are connected and ready. The invoked tests are dependent on configuration, are first level addressing, and have an invocation message of PAB, 2B. Complete link/loop testing may also be in free-lance mode; that is, after MAP termination and for second/third-level testing. Refer to CA202.

Partial testing may be valuable when communications feature hardware is not available or installed, when there are time considerations, or when either communications adapter or 8100 CA feature hardware need to be verified, but not both. The invoked tests are dependent on configuration, are first level addressing, and have an invocation message of PAB, 1B. Refer to CA202.

CA216 Selectable Tests

In the CA MAPs, the term 'selectable tests' designates those communications tests that require test preparation or manual intervention and run under MAP control. These tests offer additional test capability for a given communications feature. Selectable tests are a subset of the total communications test package.

Selectable Tests	Driver Hardware
16 (See CA548)	EIA – IBM modem
61 (See CA543)	EIA – Direct connect
63 (See CA545)	EIA – Modem; any V.35
64	EIA – IBM modem
66 (See CA547)	DDS
67 (See CA546)	X.21 (nonswitched)
68 (See CA546)	X.21 (nonswitched)

See CA211 and CA212 for test descriptions.

CA220 Online Test Routine Descriptions

DPCX CA online tests can be run with customer operations. These tests are limited and depend on the program.

CA221 Not Used

CA222 DPCX Tests

DPCX contains limited CA online tests which may be run with the customer programs. See CA202 for the invocation procedures. The following tests are provided: 1–16, 51*, 53*, 71* (SDLC link test, see CA223), 75*, 76*, 88*, and 90–94*. See CA211 and CA212 for CA test descriptions. DPCX tests will loop a maximum of five times when the looping option is selected on the invocation message.

CA223 Link-Level Tests

DPCX SDLC Link Test

The host 3704/3705 Communications Controller provides an SDLC Link test that may be used for host data link problem determination and repair verification.

The DPCX SDLC link test is basically an echo test with the 370X sending an SDLC test frame to a 8100. The 8100 echoes the test sequence back to the 370X if it is received without error. There are two levels of the 370X link test: link level 0 requires a dedicated 370X; link level 1 requires only a dedicated link.

The test frame that is sent to the 8100 is the same, regardless of the test, and all frames are structured as shown below. An optional data field can be used, but must not be more than nine bytes for proper operation.

The following illustrates the SDLC test frame format:

Pad Pad F A C dd BC F ee

Where:

Pad = Alternate data transition character for clock correction:

Only those characters between the two flags constitute a frame. The use of the NRZI and the zero Bit insertion modifies the actual bit presentation as seen on the line.

00 = NRZI mode (8100 only transmits pads in NRZI mode)

AA = non-NRZI mode

F = Flag character 7E

A = 8100 address byte. This is the address entered in Option 1 of SYSIMOD as the station ID, and is found in the *DPCX Installation Manual,* SC27-0484.

C = SDLC command byte F3. Used for test command with poll bit active.

dd = Optional data field. Any character combination not exceeding 9 bytes.

BC = Frame check sequence (FCS) characters

ee = Ending idle character FF

The SYSHOST function of the operating code handles the receiving of the SDLC test frames and the echoing back to the 370X. With SYSHOST function selected, the 8100 receives and checks all test frames. Those that are received correctly and have nine or fewer data bytes are transmitted back to the 370X exactly as received. Test frames that are received correctly but have more than nine data bytes cause transmission of a test frame with no data field back to the 370X. The 8100 sends no response to any frame received incorrectly. Link test results are recorded in the 8100 condition/incident Log as Type 4 COND-20 records.

* Link level tests

SDLC Link Test Operational Procedure, DPCX

The 8100 must be in an online condition (Operating Code Initialized). Two functions are used:

- SYSHOST – Receives the test frames, echoes the frame, and causes the condition/incident records to be logged.
- SYSLERR – Displays the contents of the condition/incident log.

1. Ensure that the 8100 is in an online condition; see Condition Changes in Chapter 2.
2. Log on a terminal by using the Control Operator ID instead of the CE ID 255CEDPCX (see Terminal Procedures in Chapter 2). (SYSHOST can be selected only by a terminal that has been logged on using a Control Operator ID.) If this is an initial installation or if the customer has not changed the original ID, use 01 for the Control Operator ID. If the current Control Operator ID is not available to you, control operator assistance is required to log on the terminal.
3. Select SYSLERR Function (978) and record the sequence number from the most current record (see SYSLERR in CP830 of Chapter 2). Option field examples: Field 3 = 3; Field 2 = 2; Field 1 = 10. Use these option field entries to obtain the most recent record. The sequence number identifies the beginning of link test recordings in the condition/incident log.
4. Terminate SYSLERR (type 9 and press ENTER to exit from SYSLERR).
5. Select the SYSHOST Function (959) and establish the host line connection (refer to SYSHOST-1 in Chapter 4 of the *DPCX Operations Manual,* SC27-0492).
   a. At message "SEE SYSHOST OPTION GROUP 1", type 1, press ENTER* (enables Communications).
   b. At message "SEE SYSHOST OPTION GROUP 2", type 21, press ENTER* (enables Communications). The online CA feature tests are now running, and the enable process has been running for approximately 30 seconds.
   c. At message "A081 – ENABLE IN PROCESS – BEFORE PROCEDURE, DISPLAY STATUS SEE HOST OPTION GROUP 1" (the 8100 is now ready to communicate with the HOST and respond to link test frames), type 9 and press ENTER* (releases SYSHOST; SYSHOST is still active in 8100. A new function may now be selected.)
6. Notify the host personnel by voice communication that the link test may now start.
7. After the host runs the link test, select SYSLERR (978) and examine the log for new TYPE 4 COND 20 records. New records have a higher sequence number than those recorded in step 3. Use SYSLERR option fields: Field 3 = 3; Field 2 = 2420; Field 1 = 10. The most recent TYPE 4 COND 20 record is the first record output. See the next paragraph, SDLC Link Test Condition/Incident Recordings, for interpretation.
8. To terminate SYSHOST:
   a. Terminate SYSLERR if still selected (type 9 and press ENTER* to exit from SYSLERR).
   b. At message "SEE SYSHOST OPTION GROUP 1", type 2 and press ENTER* (selects disable operation).

*ENTER is not required on some terminals.

c. At message "SEE SYSHOST OPTION GROUP 2", type 32 and press ENTER* (terminates all sessions).

d. At message "DISABLE COMPLETE SEE SYSHOST OPTION GROUP 1", type 9 and press ENTER* (end SYSHOST).

SYSHOST is not disabled, and the 8100 can no longer respond to Link Test Frames. If logoff is required, type: SYSOFF.

SDLC Link Test Condition/Incident Log Recordings, DPCX

Problem resolution using link test is done primarily by examining the results of the test as output at the host. When 8100 assistance is required for problem resolution, the 8100 condition/incident log is used for link test interpretation. All communications feature link test log records are recorded as TYPE 4 SYS-COND-20.

4-TYPE 1-REC SEQ-XXXX SYS-COND-20.

D01-XX D02-XX D03-XX D04-XX D05-XX

For every test frame received, a log record is made at the time the SDLC command byte F3 (test command) is decoded. The log record is recorded as follows.

4-TYPE 1-REC SEQ-XXXX SYS-COND-20.

D01-01 D02-X1 D03-41 D04-XX D05-XX

where:

D01-01	Indicates read operation
D02-X1	Indicates read operation intermediate completeion.
D03-41	Indicates that a test command with the poll bit on has been decoded.
D04-XX	Not used.
D05-XX	Not used.

If the test frame has been received without error, the message is transmitted back to the 370X. At completion of transmission, a log record is recorded as follows:

4-TYPE 1-REC SEQ-XXXX SYS-COND-20.

D01-01 D02-X1 D03-42 D04-XX D05-XX

where:

D01-01	Indicates read operation
D02-X1	Indicates read operation intermediate completion.
D03-42	Indicates link test and read message available.
D04-XX	Not used.
D05-XX	Not used.

Failures that prevent the SDLC test frame from being received or transmitted correctly cause a log recording to be made exactly as host communication failures are recorded. See CA332 for a description of these recordings. If SYSLERR results are not as expected, see CA332 and CA342.

4-TYPE 1-REC SEQ-XXXX SYS-COND-20.

D01-01 D02-X2 D03-10 D04-XX D05-XX

*ENTER is not required on some terminals.

where:

D01-01	Indicates read operation
D02-X2	Indicates read/write exception.
D03-10	Indicates idle time out.
D04-XX	Not used.
D05-XX	Not used.

CA230 Test Message Types

This section describes general test messages; refer to CA211 and CA212 for MI messages; refer to CA240 for specific CA test error messages; refer to Chapter 4 for general CA test messages.

CA231 Offline and Online CA Test Message Types

Test Error Message Formats

Notes:

1. MI messages are described in CA211 and CA212.

2. When entering data into the MD, enter the data without any blanks.

3. For XXBC, PA80, and PA90 messages, refer to the table in CA241.

The following test error message formats are used for the CA features:

1. PAXE RREN
2. PAXE RREN 0506 0822
3. PAXE RREN 0506 0822 0506 0822
4. PAXE RREN data fields (variable bytes)

Where:

PA	=	Physical address.
X	=	Address level (1, 2, 3).
E	=	Error; indicates that the three preceding digits are an error format and that the next four digits are RREN.
RR	=	Failing routine number (01 through 99).
EN	=	Error number, which defines the type of error (see CA240).

Control Lines:

00	=	Not active
05	=	CTS active
06	=	DSR active
08	=	RLSD active
22	=	RI active

Control Lines:

First field = Actual data

Second field = Expected data

Message Formats by Routine Number

The following lists the format type number used by each routine.

Routine	Format Type (See formats above.)
1–14	1
15	1,4
16	1,4
17	1,3
18	1,3,4
19	1,3
20	1,2,3
21	1
22	1
25	1
51	1,4
52	1,4
53	1
61	1,3
63	1,3
64	1,4
66	1,3
67	1,3
68	1,3
71–99	1,4

CA232 CA MAP Test Messages – Known Test Error Message Format

The 8100 CA MAP has a MAP menu selection called Known Test Error Message, in which you may enter a valid known test error message and start MAP repair actions without running through a portion of the base CA MAP and tests.

Certain test messages cannot be entered under this MAP selection because of repair action requirements that test run and hold certain lines for probing. Also, due to MAP/test restrictions, some tests are not used in the CA MAP (link-level tests).

When entering a PA1E test error message into the MD, MAP Menu Selection C, enter with no spaces.

Correct	Not Correct
PA1ERREN	PA1E RREN

The following test routines are valid for the Known Test Error Message format:

PA1E RREN (data fields).

Where:

PA = Physical address

1E = Level 1 error

RR = Test routine

EN = Error number

Valid test routines are:

1–15

16

21/22

CA240 Test Message, Error Number Descriptions, and Possible Causes

The following tables list the test routine and error number, describe the error, and list possible causes.

CA241 Adapter Test Message, Error Number Descriptions, and Possible Causes

Routines 1 and 2

RREN	Error Description	Possible Causes
0101	Unexpected system check.	1. CA1/CA2
0102	Unexpected interrupt.	2. Cables
0104	Unexpected interrupt.	3. Power
0105	Missing or late interrupt.	4. SC5 card
0106	Active or recurring interrupt.	
010B	System check during routine execution.	
011A	Error detected during routine execution.	
011F	Unknown cause.	
0174	B/S incorrect, all bits except modem interrupt should be off at the end of the test.	
0201	Unexpected system check.	1. CA1/CA2
0202	Unexpected interrupt.	2. Cables
0204	Unexpected interrupt.	3. Power
0205	Missing or late interrupt.	4. SC5 card
0206	Active or recurring interrupt.	
020B	System check during routine execution.	
021A	Error detected during routine execution.	
021F	Unknown cause.	
0274	No M/C occurred for invalid command.	
0275	B/S incorrect; Invalid command did not set M/C bit.	
0276	A bit in B/S will not reset.	

Routines 3, 4, and 5

RREN	Error Description	Possible Causes
0301	Unexpected system check.	1. CA1/CA2
0302	Unexpected interrupt.	2. Cables
0304	Unexpected interrupt.	3. Power
0305	Missing or late interrupt.	4. SC5 card
0306	Active or recurring interrupt.	
030B	System check during routine execution.	
031A	Error detected during routine execution.	
031F	Unknown cause.	
0374	Control reg incorrect; should be 00 after adapter reset.	
0375	Data read failure; data not as expected following reset control reg command.	
0401	Unexpected system check.	1. CA1/CA2
0402	Unexpected interrupt.	2. Cables
0404	Unexpected interrupt.	3. Power
0405	Missing or late interrupt.	4. SC5 card
0406	Active or recurring interrupt.	
040B	System check during routine execution.	
041A	Error detected during routine execution.	
041F	Unknown cause.	
0472	Local test line in error.	1. CA5/CA6
0474	Local test line in error. or Control reg incorrect; should be 00 after adapter reset, or data read failure.	2. CA1/CA2
0475	Control reg incorrect, should be 00 after adapter reset, or data read failure.	
0501	Unexpected system check.	1. CA1/CA2
0502	Unexpected interrupt.	2. Cables
0504	Unexpected interrupt.	3. Power
0505	Missing or late interrupt.	4. SC5 card
0506	Active or recurring interrupt.	
050B	System check during routine execution.	
051A	Error detected during routine execution.	
051F	Unknown cause.	
0574	Modem interrupt should be pending.	
0575	Modem status incorrect.	
0576	Modem interrupt will not reset.	
0577	Transition indicators will not reset.	

Routines 6, 7, and 8

RREN	Error Description	Possible Causes
0601	Unexpected system check.	1. CA1/CA2
0602	Unexpected interrupt.	2. Cables
0604	Unexpected interrupt.	3. Power
0605	Missing or late interrupt.	4. SC5 card
0606	Active or recurring interrupt.	
060B	System check during routine execution.	
061A	Error detected during routine execution.	
061F	Unknown cause.	
0674	Timer high test, no interrupt from timer within max loop time, or timer interval too short.	
0676	Timer interrupt bit in B/S will not reset.	
0678	Timer low test, no interrupt from timer within max loop time, or timer interval too short.	
0679	Timer low test, no interrupt from timer within max loop time, or timer interval too short.	
067A	Timer interrupt should be reset.	
0701	Unexpected system check.	1. CA1/CA2
0702	Unexpected interrupt.	2. Cables
0704	Unexpected interrupt.	3. Power
0705	Missing or late interrupt.	4. SC5 card
0706	Active or recurring interrupt.	
070B	System check during routine execution.	
071A	Error detected during routine execution.	
071F	Unknown cause.	
0774	Timer high control bit error; no interrupt pending.	
0775	Timer low control bit error; interrupt should be off.	
0776	Timer low control bit error; interrupt should be on.	
0778	Interrupt occurred on wrong interrupt level.	

RREN	Error Description	Possible Causes
0801	Unexpected system check.	1. CA1/CA2
0802	Unexpected interrupt.	2. Cables
0804	Unexpected interrupt.	3. Power
0805	Missing or late interrupt.	4. SC5 card
0806	Active or recurring interrupt.	
080B	System check during routine execution.	
081A	Error detected during routine execution.	
081F	Unknown cause.	
0874	B/S incorrect; enable bit should be on.	
0875	B/S incorrect; enable bit will not reset.	

Routines 9 and 0A

RREN	Error Description	Possible Causes
0901	Unexpected system check.	1. CA1/CA2
0902	Unexpected interrupt.	2. Cables
0904	Unexpected interrupt.	3. Power
0905	Missing or late interrupt.	4. SC5 card
0906	Active or recurring interrupt.	
090B	System check during routine execution.	
091A	Error detected during routine execution.	
091F	Unknown cause.	
0974	B/S incorrect; enable bit should be on.	
0975	B/S incorrect; enable bit will not reset.	
0972*	Board not jumpered for data rate. or Wrong adapter or clock option installed. or Basic status incorrect; detected while in "status", XMTPAD or initial character transfer subroutines.	*Check board for correct data rate jumper 1. CA1/CA2 2. Cables 3. Power 4. SC5 card
0973	A/S incorrect; detected while in initial character transfer routine.	1. CA1/CA2 2. Cables 3. Power 4. SC5 card
0974	A/S Incorrect; adapter in sync bit should be on.	
0975	Adapter control reg not as expected.	
0976	B/S incorrect; O/P request should be on.	
0978	B/S incorrect; O/P request should be off.	
0979	A/S incorrect; read clock run bit should be on.	
097A	B/S incorrect; input request should be off.	
097B	A/S incorrect; adapter in sync will not reset.	
0A01	Unexpected system check.	1. CA1/CA2
0A02	Unexpected interrupt.	2. Cables
0A04	Unexpected interrupt.	3. Power
0A05	Missing or late interrupt.	4. SC5 card
0A06	Active or recurring interrupt.	
0A0B	System check during routine execution.	
0A1A	Error detected during routine execution.	
0A1F	Unknown cause.	
0A72	B/S incorrect; detected while in status, XMTPAD or initial character transfer subroutines.	
0A73	A/S incorrect; detected while in initial character transfer subroutine.	
0A74	Adapter control reg not as expected.	
0A75	B/S incorrect; input request bit should be off.	

Routines 0B and 0C

RREN	Error Description	Possible Causes
0B01	Unexpected system check.	1. CA1/CA2
0B02	Unexpected interrupt.	2. Cables
0B04	Unexpected interrupt.	3. Power
0B05	Missing or late interrupt.	4. SC5 card
0B06	Active or recurring interrupt.	
0B0B	System check during routine execution.	
0B1A	Error detected during routine execution.	
0B1F	Unknown cause.	
0B72	B/S incorrect; detected while in status, XMTPAD, or initial character transfer subroutines.	
0B73	A/S incorrect; detected while in initial character transfer subroutine.	
0B74	B/S incorrect; only exception bit should be on.	
0B75	A/S incorrect; adapter in sync and SDLC frame.	
0B76	Adapter control reg not as expected.	
0B78	B/S incorrect; exception interrupt should be on.	
0B79	A/S incorrect; SDLC frame bit should be on.	
0B7A	A/S incorrect; SDLC frame bit will not reset.	
0C01	Unexpected system check.	1. CA1/CA2
0C02	Unexpected interrupt.	2. Cables
0C04	Unexpected interrupt.	3. Power
0C05	Missing or late interrupt.	4. SC5 card
0C06	Active or recurring interrupt.	
0C0B	System check during routine execution.	
0C1A	Error detected during routine execution.	
0C1F	Unknown cause.	
0C72	B/S incorrect; detected while in status, XMTPAD, or initial character transfer subroutines.	
0C73	A/S incorrect; detected while in initial character transfer subroutine.	
0C74	Underrun bit not set. or Underrun bit will not reset.	

Routines 0D and 0E

RREN	Error Description	Possible Causes
0D01	Unexpected system check.	1. CA1/CA2
0D02	Unexpected interrupt.	2. Cables
0D04	Unexpected interrupt.	3. Power
0D05	Missing or late interrupt.	4. SC5 card
0D06	Active or recurring interrupt.	
0D0B	System check during routine execution.	
0D1A	Error detected during routine execution.	
0D1F	Unknown cause.	
0D48	B/S output request bit 1; A/S receive clock running bit 2.	
0D50	B/S output request bit 0.	
0D58	B/S input request on with receive mode off.	
0D72	B/S incorrect, detected while in status, XMTPAD, or initial character transfer subroutines.	
0D73	A/S incorrect; detected while in initial character transfer subroutine.	
0E01	Unexpected system check.	1. CA1/CA2
0E02	Unexpected interrupt.	2. Cables
0E04	Unexpected interrupt.	3. Power
0E05	Missing or late interrupt.	4. SC5 card
0E06	Active or recurring interrupt.	
0E0B	System check during routine execution.	
0E1A	Error detected during routine execution.	
0E1F	Unknown cause.	
0E72	B/S incorrect; detected while in status, XMTPAD, or initial character transfer subroutines.	
0E73	A/S incorrect; detected while in initial character transfer subroutine	
0E74	Underrun bit not set.	
0E74	Underrun bit will not reset.	

Routines 0F and 10

RREN	Error Description	Possible Causes
0F01	Unexpected system check.	1. CA1/CA2
0F02	Unexpected interrupt.	2. Cables
0F04	Unexpected interrupt.	3. Power
0F05	Missing or late interrupt.	4. SC5 card
0F06	Active or recurring interrupt.	
0F0B	System check during routine execution.	
0F1A	Error detected during routine execution.	
0F1F	Unknown cause.	
0F72	B/S incorrect; detected while in status, XMTPAD, or initial character transfer subroutines.	
0F73	A/S incorrect; detected while in initial character transfer subroutine.	
0F74	B/S incorrect; exception not set within time.	
0F75	A/S incorrect; SDLC frame bit should be on.	
0F76	A/S incorrect; invalid sequence should be on.	
0F78	A/S incorrect; invalid sequence will not reset.	
1001	Unexpected system check.	1. CA1/CA2
1002	Unexpected interrupt.	2. Cables
1004	Unexpected interrupt.	3. Power
1005	Missing or late interrupt.	4. SC5 card
1006	Active or recurring interrupt.	
100B	System check during routine execution.	
101A	Error detected during routine execution.	
101F	Unknown cause.	
1068	B/S input request, output request, and exception.	
1072	B/S incorrect; detected while in status, XMTPAD, or initial character transfer subroutines.	
1073	A/S incorrect; detected while in initial character transfer subroutine.	

Routines 11 and 12

RREN	Error Description	Possible Causes
1101	Unexpected system check.	1. CA1/CA2
1102	Unexpected interrupt.	2. Cables
1104	Unexpected interrupt.	3. Power
1105	Missing or late interrupt.	4. SC5 card
1106	Active or recurring interrupt.	
110B	System check during routine execution.	
111A	Error detected during routine execution.	
111F	Unknown cause.	
1172	B/S incorrect; detected while in status, XMTPAD, or initial character transfer subroutines.	
1173	A/S incorrect; detected while in initial character transfer subroutine.	
1180	B/S input request, output request, and exception. A/S invalid character bit 5.	
1201	Unexpected system check.	1. CA1/CA2
1202	Unexpected interrupt.	2. Cables
1204	Unexpected interrupt.	3. Power
1205	Missing or late interrupt.	4. SC5 card
1206	Active or recurring interrupt.	
120B	System check during routine execution.	
121A	Error detected during routine execution.	1. CA1/CA2
121F	Unknown cause.	2. Cables
1272	B/S incorrect; detected while in status, XMTPAD, or initial character transfer subroutines.	3. Power 4. SC5 card
1273	A/S incorrect; detected while in initial character transfer subroutine.	
1274	A/S incorrect; invalid sequence should be on.	
1275	A/S incorrect; invalid sequence will not reset.	

Routines 13 and 14

RREN	Error Description	Possible Causes
1301	Unexpected system check.	1. CA1/CA2
1302	Unexpected interrupt.	2. Cables
1304	Unexpected interrupt.	3. Power
1305	Missing or late interrupt.	4. SC5 card
1306	Active or recurring interrupt.	
130B	System check during routine execution.	
131A	Error detected during routine execution.	
131F	Unknown cause.	
1372	B/S incorrect, detected while in status, XMTPAD or initial character transfer subroutines.	
1373	A/S incorrect, detected while in initial character transfer subroutine.	
1374	B/S incorrect, output request should be on.	
1375	A/S incorrect, adapter in sync frame.	
1401	Unexpected system check.	1. CA1/CA2
1402	Unexpected interrupt.	2. Cables
1404	Unexpected interrupt.	3. Power
1405	Missing or late interrupt.	4. SC5 card
1406	Active or recurring interrupt.	
140B	System check during routine execution.	
141A	Error detected during routine execution.	
141F	Unknown cause.	
1421*	Open failure.	
1422*	Activate link failure.	
1472	B/S incorrect; detected while in status, XMTPAD, or initial character transfer subroutines.	
1473	A/S incorrect; detected while in initial character transfer subroutine.	
1488	B/S exception and interrupt request.	
	A/S break byte detected bit 6.	

*DPCX error message only

Routine 15

RREN	Error Description	Possible Causes
1501	Unexpected system check.	1. CA1/CA2
1502	Unexpected interrupt.	2. Cables
1504	Unexpected interrupt.	3. Power
1505	Missing or late interrupt.	4. SC5 card
1506	Active or recurring interrupt.	
150B	System check.	Check for wrong unit type in configuration table
1510	A timer interrupt occurred prior to CTS turning on. Adapter waited 25 seconds for CTS to become active.	1. CA1/CA2 2. Cables 3. Power 4. SC5 card
151B	Error detected during execution of FDM function request '09' (SDLC wrap).	
151C	Incorrect SC5 switches or data wrap failed	1. Check all SCFA switches 2. CA1/CA2
151D	Error detected during execution of FDM function request '11' (interface selection)	1. CA1/CA2 2. Cables 3. Power 4. SC5 card
151E	Error detected during execution of FDM function request '21' (Clear)	
1520	A timer interrupt occurred after CTS became active. No adapter activity (I/P or O/P) occurred within 1 second of it being expected. Not all transmit data has been sent.	1. CA1/CA2 2. Cables
1521*	Open failure.	
1522*	Activate link failure.	
1530	As code 20 except all data has been transmitted.	
1540	A modem interrupt occurred after CTS became active.	
1550	An output request interrupt occurred and three data characters had already been transmitted and placed in the 'expected data buffers'; an input request has not occurred.	

*DPCX error message only

RREN	Error Description	Possible Causes
1560	An output request interrupt occurred and transmit mode had been off.	1. CA1/CA2 2. SC5 card 3. Cables
1570	An input request interrupt occurred and no data has been transmitted.	
1577	The 30-second timer in the driver program ran out while waiting for an interrupt.	
1580	An input request occurred and there was no data in the 'expected data buffers'.	1. CA1/CA2 2. SC5 card
1590	An input request occurred and RCVD data did not compare with expected data.	
15A0	An input request occurred prior to flag recognition.	
15B0	Invalid basic status.	
15C0	Invalid exception Synchronous. or Adapter status error (start/stop).	
15D0	SDLC flag bit was on and adapter has not been placed in SDLC mode.	
15D0	Adapter status error (start/stop). Invalid character is on and the character is in register 7.	1. CA1/CA2
15E0	Data decoded as SDLC flag.	
15F0	Adapter status error.	

Routine 16, EIA/V.35/X.21 (Nonswitched) Card Wrap

RREN	Error Description	Possible Causes
1601	Unexpected system check.	1. CA1/CA2
1602*	Machine check.	2. CA5/CA6/CA11
1604	Unexpected interrupt.	3. Multispeed clock card
1605	Missing or late interrupt.	4. Cables
1606	Active or recurring interrupt.	5. Board wiring
160B	System check during routine execution.	
1610	A timer interrupt occurred prior to CTS turning on.	
	Adapter waited 25 seconds for CTS to become active.	
161A	Error detected during routine execution function request '09' (SDLC wrap).	

*DPCX error message only

RREN	Error Description	Possible Cause
161C	Error detected during routine exception function request 'OD' (external wrap).	1. CA5/CA6/CA11 2. CA1/CA2 3. Cables
161D	Error detected during routine execution function request '11' (interface selection).	1. CA1/CA2 2. CA5/CA6/CA11 3. Multispeed clock card 4. Board wiring 5. Cables
161E	Error detected during routine execution function request '21' (interface selection).	
161F	Unknown cause.	
1620	A timer interrupt occurred after CTS became active. No adapter input or output occurred within 1 second of its being expected. Not all transmit data has been sent.	1. CA5/CA6/CA11 2. CA1/CA2 3. Cables 4. Board wiring – 1620: No clock board wiring 1630: Card jumpers not correct
1621*	Open failure.	
1622*	Activate link failure.	
1630	As 1620, except all data has been transmitted.	
1640	A modem interrupt occurred after CTS became active or there is a configuration error.	
1650	An output request interrupt occurred and three data characters had already been transmitted and placed in the 'expected data buffers'; an input request has not occurred.	
1660	An output request interrupt occurred and transmit mode had been off.	
1666	An output request interrupt occurred and no data has been transmitted.	
1670	An input request interrupt occurred and no data has been transmitted.	
1677	The 30-second timer in driver program ran out while waiting for an interrupt.	
1680	An input request occurred and there was no data in the 'expected data buffers'.	1. CA5/CA6/CA11 2. CA1/CA2 3. Cables
1690	An input request occurred and RCVD data did not compare with expected data.	
1699	Configuration table error.	MD configuration table incorrect

*DPCX error message only

RREN	Error Description	Possible Causes
16A0	An input request occurred prior to flag recognition.	1. CA5/CA6/CA11 2. CA1/CA2 3. Cables
16B0	Invalid basic status.	
16C0	Invalid exception (BSC). or Adapter status error (start/stop).	
16D0	Flag bit was on and adapter has not been placed in BSC mode. Adapter status error (start/stop). Invalid character is on and the character is in register 7.	
16E0	Data decode error.	
16F0	Adapter status error.	

Routine 18, Loop Adapter

RREN	Error Description	Possible Causes
1801	Unexpected system check.	1. CA1 2. Cables 3. Power 4. SC5 card
1804	Unexpected interrupt.	
1805	Missing or late interrupt.	
1806	Active or recurring interrupt.	
180B	System check during routine execution.	
1811	Adapter reset; all control lines inactive.	
181A	Error detected during routine execution frunction request '09' (SDLC wrap).	
181C	Error detected during routine execution function request '0D' (external wrap).	
181D	Error detected during routine execution function request '11' (line selection).	
181E	Error detected during routine execution function request '21' (line selection).	
181F	Unknown cause.	
1831	Control line(s) not at expected level(s).	1. CA4 2. CA3 3. CA1
1832	Control line(s) not at expected level(s).	
1833	Control line(s) not at expected level(s).	
1834	Control line(s) not at expected level(s).	
1835	Error detected during external data wrap (monitor mode select active).	1. CA3 2. CA4 3. CA1
1836	Error detected during external data wrap with one lobe or with two lobes, test is expecting open data path only. (R1 = ON, LOBE 2)	1. CA4 2. CA3 3. CA1 4. Lobe 2 cables
1837	No error detected during external data wrap with local test active.	1. CA3 2. CA4 3. CA1 4. Lobe 1 cables
1838	Error detected during external data wrap with LT and monitor mode select active.	1. CA3 2. CA4 3. CA1
1840	No loop adapter configured for this SDLC.	MD configuration table incorrect
1841	No lobes configured for this loop device.	
1895	Error at CSU.	Wrap capability
1898	Configuration table error.	MD configuration table incorrect
1899	Configuration error.	

ROUTINE 18, STEPS AND ASSOCIATED ERROR NUMBERS

Steps	Error Number
1. Adapter reset.	11
2. Set Data Rate Select (DRS) and Select Standby (SSBY).	31
3. Set Data Terminal Ready (DTR), DRS, and SSBY.	32
4. Set DTR, DRS.	33
5. Set DTR, DRS, Request to Send (RTS).	34
6. Reset LT, RTS, NS. Set DRS.	35
Data wrap successful – continue.	
Data wrap failure – error.	
7. Set LT, DRS, NS.	35
Data wrap successful and 1 lobe – continue.	

Steps	Error Number
Data wrap successful and 2 lobes — error.	36
Data wrap failure and 1 lobe — error.	36
Data wrap failure and 2 lobes — continue.	
8. Set LT.	37
Data wrap successful — error.	
Data wrap failure — continue.	
9. Set LT, DRS.	38
Data wrap successful — end.	
Data wrap failure — error.	

Routine 19, Integrated Nonswitched Line Modem Interface Test Routine

RREN	Error Description	Possible Causes
1901 1904 1905 1906 190B	Unexpected system check. Unexpected interrupt. Missing or late interrupt. Active or recurring interrupt. System check during routine execution.	1. CA1/CA2 2. Cables 3. Power 4. SC5 card
1911	Control line(s) not at expected level(s).	1. CA1/CA2 2. CA8 3. Cables
191A 191F	Error detected during routine execution function request '09' (SDLC wrap). Unknown cause.	SCFA card
1920 1921 1930 1931	Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s).	1. CA8 2. CA1/CA2 3. Cables 4. Power
1933	Initial CTS not returned.	CA8
1940 1941 1980 1981	Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s).	1. CA8 2. CA1/CA2 3. Cables 4. Power
1988 1990	Transmit data appearing without wrap. Transmit to receive data wrap failed.	1. CA8 2. CA1/CA2
1999	Configuration table error.	MD configuration table incorrect

ROUTINE 19 STEPS AND ASSOCIATED ERROR NUMBERS

Steps	Error Number
1. Adapter reset.	11
2. Set Local Test (LT).	20
3. Reset (LT).	21
4. Set Data Terminal Ready (DTR), LT.	30
5. Reset DTR.	31
6. Set Request to Send (RTS), LT.	40
7. Reset RTS.	41
8. Set LT, DTR, RTS.	80
9. Reset LT, DTR, RTS.	81
10. Test LT interface line.	88
11. Run continuous transmit flags.	90
12. Initial Clear to Send (CTS) not returned.	33

Routine 20, Integrated Modem Switched Lines and Auto Answer Interface Test Routine

RREN	Error Description	Possible Causes
2001 2004 2005 2006 200B 2011 201A 201F	Unexpected system check. Unexpected interrupt. Missing or late interrupt. Active or recurring interrupt. System check during routine execution. Control lines active after adapter reset. Unknown cause. Unknown cause.	1. CA1/CA2 2. Cables 3. Power 4. SC5 card
2030 2032	Control line(s) not at expected level(s). Control line(s) not at expected level(s).	1. CA9 2. CA1/CA2 3. Cables 4. Power
2033 2034 2050	CTS or DSR not active. RLSD not active. Ring indicate was active.	CA9
2040 2041 2080 2081	Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s).	1. CA9 2. CA1/CA2 3. Cables 4. Power

RREN	Error Description	Possible Causes
2088 2090	Local data test always active. Transmit to receive data wrap failed.	1. CA9 2. CA1/CA2
2099	Configuration table error.	MD configuration table incorrect

Routine 21, DDSA

RREN	Error Description	Possible Causes
2101 2104 2105 2106 210B	Unexpected system check. Unexpected interrupt. Missing or late interrupt. Active or recurring interrupt. System check during routine execution.	1. CA1/CA2 2. Cables 3. Power 4. SC5 card
2111	Control lines active after adapter reset.	1. CA7 2. CA1/CA2 3. Board wiring
211A 211F	Unknown cause. Unknown cause.	1. CA1/CA2 2. Cables 3. Power 4. SC5 card
2120 2121 2130 2131 2140 2141	Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s).	1. CA7 2. CA1/CA2 3. Board wiring
2199	Configuration table error.	MD configuration table incorrect

ROUTINE 21, STEPS AND ASSOCIATED ERROR NUMBERS

Steps	Error Number
1. All drivers off.	11
2. Set Local Test (LT).	20
3. Reset Local Test (LT).	21
4. Set Request to Send (RTS).	30
5. Reset Request to Send (RTS).	31
6. Set Local Test and Request to Send.	40
7. Reset Local Test and Request to Send.	41

Routine 22, DDSA Internal Data Wrap

RREN	Error Description	Possible Causes
2201	Unexpected system check.	1. CA1/CA2
2204	Unexpected interrupt.	2. Cables
2205	Missing or late interrupt.	3. Power
2206	Active or recurring interrupt.	4. SC5 card
220B	System check during routine execution.	
221A	Error detected during routine execution.	
2233	CTS or DSR not active.	1. CA7 2. CA1/CA2 3. Board wiring
2240	Configuration table error.	MD configuration table incorrect
2290	Transmit to receive data wrap failed or wrong CA1/CA2 adapter (required without clock).	1. CA7 2. CA1/CA2
2299	Configuration table error.	MD configuration table incorrect

Routine 25, Auto-Answer Test

This routine has Manual Intervention messages, refer to CA212 for descriptions.

RREN	Error Description	Possible Causes
2501	Unexpected system check.	1. CA1/CA2
2504	Unexpected interrupt.	2. Cables 3. Power 4. SC5 card
2599	Configuration table error.	MD configuration table incorrect
25AA	DSR not on; exceeded 3-minute wait for call.	1. Retry 2. Cables 3. DAA failure 4. CA9 or modem failure 5. CA1/CA2

Routine 51, Loop Test (1-Lobe)

RREN	Error Description**	Possible Causes
5101	Unexpected system check.	1. CA1
5104	Unexpected interrupt.	2. Cables
5105	Missing or late interrupt.	3. Power
5106	Active or recurring interrupt.	4. SC5 card
510B	System check during SDLC test FDM.	
5111	Adapter level failure.	
511A	Error detected during SDLC test FDM.	
511F	Unknown Error.	
5121	Open link failed.	1. CA3
5122*	Activate failure.	2. CA1
5125	Internal active failed.	
5126	External wrap failed.	1. Loop cables 2. CA3 3. Master LSC
5127	Open passed, should have failed.	1. Master LSC 2. CA3 3. Loop cables
5128	Normal mode failed.	1. Loop or loop station
5129	Monitor mode recovery succeeded (one station now in monitor mode).	2. Loop station or CA3
5135	Normal mode 2 failed (LTST is grounded).	1. CA3 2. CA1
51FE	Configuration table error.	MD configuration table incorrect

*DPCX error message only

**ADDITIONAL ERROR DATA

51EN Y C SA

SA → Station address of beaconing station or station in monitor mode

C → C Field (Status) C4 to C7

Y → Y=0 for Routine 51

51EN → Error number

Routine 52, Loop Test (2-Lobe)

RREN	Error Description***	Possible Causes
5201	Unexpected system check.	1. CA1
5204	Unexpected interrupt.	2. Cables
5205	Missing or late interrupt.	3. Power
5206	Active or recurring interrupt.	4. SC5 card
520B	System check during SDLC test FDM.	
5211	Adapter level failure.	
521A	Error detected during SDLC test FDM.	
521F	Unknown cause.	
5225	Bad loop adapter card (lobe 1, 2 Internal Inactive).	1. Lobe 1 CA3 2. Lobe 2 CA4 3. CA1
5226	External failure, both lobes.	1. Master LSC lobe 1 2. Master LSC lobe 2
5227	Open test failure, both lobes.	3. Lobe 1 (CA3) or lobe 2 (CA4) 4. Lobe 1 or 2 cable assembly 5. CA1
5229	Successful recovery with monitor mode.	Loop station or LSC
5230	External wrap failure, lobe 1.	1. Lobe 1 cable assembly 2. Lobe 1 CA3 3. Master LSC lobe 1
5231	External wrap failure, lobe 2.	1. Lobe 2 cable assembly 2. Lobe 2 CA4 3. Master LSC lobe 2
5232	Open test failure, lobe 1.	1. Master LSC lobe 1 2. Lobe 1 CA3 3. Lobe 1 cable assembly
5233	Open test failure, lobe 2.	1. Master LSC lobe 2 2. Lobe 2 CA4 3. Lobe 2 cable assembly

RREN	Error Description***	Possible Causes
5234	Loop failure, lobe 2.	Lobe 2 or lobe 2 station
5235	Loop failure, lobe 1.	Lobe 1 or lobe 1 station
5236	Loop failure, both lobes.	Lobe 1 or lobe 1 station and lobe 2 or lobe 2 station
5237	Multiple failures (other than those above).	1. Lobe 1 CA3 2. Lobe 2 CA4 3. CA1 4. Lobe 1 or 2 cable assembly 5. Lobe 1 or 2 master LSC 6. Loop or loop station
52FE	Configuration table error.	MD configuration table incorrect

***ADDITIONAL ERROR DATA

52XX CC SA SA

- SA (second) → Lobe 2 station address of beaconing station or station in monitor mode.
- SA (first) → Lobe 1 station address of beaconing station or station in monitor mode.
- CC → C Field (Status) C0 to C7
- 52XX → Error Number

Routine 53, Remote Data Link (RDL) Test to any Group (Not Loop)

RREN	Error Description	Possible Causes
5301 5304 5305 5306 530B	Unexpected system check. Unexpected interrupt. Missing or late interrupt. Active or recurring interrupt. System check during SDLC test FDM.	1. CA1 2. Cables 3. Power 4. SC5 card
5310	Group or station fails to activate.	1. No group or station active 2. Group or station problem 3. Communications line problem
5311 531A 531F	Adapter level failure. Error detected during SDLC test FDM. Unknown cause.	1. CA1 2. Cables 3. Power 4. SC5 card
5320 5321 5322** 5323 5369 53E0 53FE	No group responds to link test or no stations in configuration table. Open fails. Activate link failure No group responds to link test.* Time out – no response from device Success with retry. System error. *Possible missing clock source.	1. No group or station active 2. Group or station problem 3. NRZI bit mismatch 4. Communications line problem 5. Intermittent problem on CA feature hardware 6. Modem problem

**DPCX error message only

Routines 61, EIA – Direct Connect Tests, and 63, EIA External Modem and V.35 Tests

RREN	Error Description	Possible Causes
RR01 RR04 RR05 RR06 RR0B	Unexpected system check. Unexpected interrupt. Missing or late interrupt. Active or recurring interrupt. System check during routine execution.	1. CA1/CA2 2. Cables 3. Power 4. SC5 card

RREN	Error Description	Possible Causes
RR11	Control lines active after adapter reset.	1. CA5/CA6 2. CA1/CA2 3. Missing –8.5 V dc 4. Missing clock 5. Cables 6. Modem 7. Board wiring
RR1A RR1F	Error detected during routine execution. Unknown cause.	1. CA1/CA2 2. Cables 3. Power 4. SC5 card
RR20 RR21 RR22 RR23 RR24 RR25 RR26 RR27 RR30 RR31 RR33 RR40 RR41 RR80 RR81	Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Initial CTS not returned. Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s).	1. CA5/CA6 2. CA1/CA2 3. Missing –8.5 V dc 4. Missing clock 5. Cables 6. Modem 7. Missing wrap 8. Board wiring
RR90	Transmit to receive data wrap failed.	1. CA1/CA2 2. Cables 3. Power 4. SC5 card 5. Missing wrap
RR99	Configuration table error	MD configuration table incorrect

ROUTINES 61 AND 63, STEPS AND ASSOCIATED ERROR NUMBERS

Steps	Error Number
1. All driver lines off.	11
2. Raise Local Test (LT).	20
3. Drop LT.	21
4. Raise Select Standby (SSBY).	22
5. Drop SSBY.	23
6. Raise New Sync (NS).	24
7. Drop NS.	25
8. Raise Data Rate Select (DRS).	26
9. Drop DRS.	27
10. Raise Data Terminal Ready (DTR).	30
11. Drop DTR.	31
12. Raise Request to Send (RTS).	40
13. Drop RTS.	41
14. Raise DTR and RTS.	80
15. Drop DTR and RTS.	81
16. Run continuous transmit flags.	90
17. Initial Clear to Send (CTS) not returned.	33

Routine 64, Modem Analyzer

This routine has Manual Intervention messages; refer to CA212 for descriptions.

RREN	Error Description	Possible Causes
6401 6404 6405 6406 640B	Unexpected system check. Unexpected interrupt. Missing or late interrupt. Active or recurring interrupt. System check during routine execution.	1. CA1/CA2 2. CA5 3. SC5 card 4. Power 5. Cables
641D 641F 6433	Error detected during routine execution function request '11' (interface selection). Unknown cause. Initial CTS not returned.	1. Modem 2. Modem cables 3. CA5 4. Cables 5. CA1/CA2

Routine 66. DDS External Data Wrap.

RREN	Error Description	Possible Causes
6601 6604 6605 6606 660B 661A 661F	Unexpected system check. Unexpected interrupt. Missing or late interrupt. Active or recurring interrupt. System check during routine execution. Error detected during routine execution function request '09' (SDLC wrap). Unknown cause.	1. CA1/CA2 2. Cables 3. Power 4. SC5 card
6633	Initial CTS not returned, or DSR not active	1. CA7 2. Cables 3. Board wiring
6640	Configuration table error.	MD configuration table incorrect
6690	Transmit to receive data wrap failure.	1. CA7 2. Cables 3. Missing wrap
6699	Configuration table error.	MD configuration table incorrect

Routine 67, X.21 (Nonswitched) External Data Wrap 1

RREN	Error Description	Possible Causes
6701 6704 6705 6706 670B 6710 671A	Unexpected system check. Unexpected interrupt. Missing or late interrupt. Active or recurring interrupt. System check during routine execution. A timer interrupt occurred prior to CTS turning on. Adapter waited 25 seconds for CTS to become active. Error detected during routine execution function request '09' (SDLC wrap).	1. CA1 2. CA11 3. Board wiring 4. Cables
671C	Error detected during routine execution function request '0D' (external wrap).	1. CA11 2. CA1 3. Cables
671D 671E 671F	Error detected during routine execution function request '11' (interface selection). Error detected during routine execution function request '21' (interface selection). Unknown causes.	1. CA1 2. CA11 3. Board wiring 4. Cables
6780 6790	An input request occurred and there was no data in the expected data buffers. An input request occurred and RCVD data did not compare with expected data.	1. CA11 2. CA1 3. Cables
6799	Configuration table error.	MD configuration table incorrect

Routine 68, X.21 (Nonswitched) External Data Wrap 2

RREN	Error Description	Possible Causes
6801 6804 6805 6806 680B	Unexpected system check Unexpected interrupt. Missing or late interrupt. Active or recurring interrupt. System check during routine execution.	1. CA1 2. Cables 3. Power 4. SC5 card
6811	Control lines active after adapter reset.	1. CA11 2. CA1 3. Missing –8.5 V dc 4. Missing clock 5. Cables 6. DCE 7. Board wiring
681A 681F	Error detected during routine execution. Unknown cause.	1. CA1 2. Cables 3. Power 4. SC5 card
6820 6821 6822 6823 6824 6825 6826 6827 6830 6831 6833 6840 6841 6880 6881	Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Initial CTS not returned. Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s). Control line(s) not at expected level(s).	1. CA11 2. CA1 3. Missing –8.5 V dc 4. Missing clock 5. Cables 6. DCE 7. Missing wrap 8. Board wiring
6890	Transmit to receive data wrap failed.	1. CA1 2. Cables 3. Power 4. SC5 card 5. Missing wrap
6899	Configuration table error	MD configuration table incorrect

ROUTINE 68, STEPS AND ASSOCIATED ERROR NUMBERS

Steps	Error Number
1. All driver lines off.	11
2. Raise Local Test (LT).	20
3. Drop LT.	21
4. Raise Select Standby (SSBY).	22
5. Drop SSBY.	23
6. Raise New Sync (NS).	24
7. Drop NS	25
8. Raise Data Rate Select (DRS).	26
9. Drop DRS.	27
10. Raise Data Terminal Ready (DTR).	30
11. Drop DTR.	31
12. Raise Request to Send (RTS).	40
13. Drop RTS.	41
14. Raise DTR and RTS.	80
15. Drop DTR and RTS.	81
16. Run continuous transmit flags.	90
17. Initial Clear to Send (CTS) not returned.	33

Routine 71, SDLC Secondary Link Test

This routine has Manual Intervention messages: see CA212 for descriptions.

RREN	Error Description	Possible Causes
7101 7104 7105 7106	Unexpected system check. Unexpected interrupt. Missing or late interrupt. Active or recurring interrupt.	1. CA1 2. Cables 3. Power 4. SC5 card
7120 7121	Secondary busy due to lack of recv buffer. Receive overrun; read control block overflowed.	CA1
7122	Idle timeout; no flags received for 20 seconds. **Caution: Not a failure if SDLC Primary stopped sending link tests and SDLC secondary received all tests.**	1. Remote controller or station 2. Communications line 3. NRZI bit mismatch 4. Modem or DCE 5. CA1 6. CA5, CA6, CA7, CA8, CA9 7. Cables 8. Board wiring
7123 7124	Overrun; alternate buffers or channel I/O overrun. Underrun; transmit mode.	1. CA1 2. CA5, CA6, CA7, CA8, CA9 3. Cables 4. Board wiring
7125	Cannot establish communications with the remote station. **Caution: Not a failure if SDLC Primary stopped sending link tests and SDLC secondary received all tests.**	1. Remote controller or station 2. Communications line 3. NRZI bit mismatch 4. Modem or DCE 5. CA1 6. CA5, CA6, CA7, CA8, CA9 7. Cables 8. Board wiring
7126	One or more errors occurred.	1. CA1 2. CA5, CA6, CA7, CA8, CA9 3. Cables 4. Board wiring
7127	CRC failed for last message received.	1. Remote controller or station 2. Communications line 3. Modem or DCE 4. CA1 5. CA5, CA6, CA7, CA8, CA9 6. Cables 7. Board wiring

RREN	Error Description	Possible Causes
7128	Abnormal termination of a message by the remote transmitting station.	1. Remote controller or station 2. Communications line 3. Modem or DCE
7129	Command reject illegal NR sequence count.	CA1
7130	Message length too long.	1. Remote controller or station 2. CA1
7131 7132	Invalid command. Invalid status.	1. CA1 2. CA5, CA6, CA7, CA8, CA9 3. Cables 4. Board wiring
7133 7134	Data communication equipment (DCE) error. Lost data.	1. Remote controller or station 2. Communications lines 3. Modem or DCE 4. CA1 5. CA5, CA6, CA7, CA8, CA9 6. Cables 7. Board wiring
7135 7136	Write timeout. Timeout during an open function request.	CA1
7137	Ring indicate at open function request.	1. Remote controller or station 2. Communications line 3. Modem or DCE 4. CA1 5. CA5, CA6, CA7, CA8, CA9 6. Cables 7. Board wiring

RREN	Error Description	Possible Causes
7138	Retry timeout during open function request or timeout while waiting for Data Set Ready.	1. CA1 2. CA5, CA6, CA7, CA8, CA9 3. Cables 4. Remote controller or station 5. Communications line 6. Board wiring
7139	Halt occurred.	1. CA1 2. CA5, CA6, CA7, CA8, CA9 3. Cables 4. Board wiring
7140 7141 7188	Disconnect received. Dump message. Unknown error type.	1. Remote controller or station 2. Communications line 3. Modem or DCE 4. CA1 5. CA5, CA6, CA7, CA8, CA9 6. Cables 7. Board wiring
7199	System check or retry.	1. CA1 2. CA5, CA6, CA7, CA8, CA9 3. Cables 4. Board wiring

Routine 72, Data Link Loop – Poll Test

This routine has Manual Intervention messages; see CA212 for descriptions.

RREN	Error Description	Possible Causes
7201	Unexpected system check.	1. CA1
7204	Unexpected interrupt.	2. Cables
7205	Missing or late interrupt.	3. Power
7206	Active or recurring interrupt.	4. SC5 card
720B	System check during routine execution.	
7221	Open port failure.	384X failure

Routine 73, Loop Relay Pick Test

No errors are reported in this routine.

Routine 75, Group Analysis

This routine has Manual Intervention messages, see CA212 for descriptions.

RREN	Error Description	Possible Causes
7501	Unexpected system check.	1. CA1/CA2 2. Cables 3. Power 4. SC5 card
7520	No stations configured for this port address or communications line failure.	1. Communications line failure 2. MD configuration table incorrect 3. Station not installed
7521 7522*	Open fails. Activate failure.	CA1
7523	No stations on data link respond to disconnect.	1. CA1 2. Station failure 3. NRZI bit mismatch 4. Intermittent CA hardware failure
75CE	Invalid manual response	Invalid response
75FE	Configuration table error.	MD configuration table incorrect

*DPCX error message only

Routine 76, Loop Beacon and Ordinal Sequence Test

This routine has Manual Intervention messages; see CA212 for descriptions.

RREN	Error Description	Possible Causes
7601	Unexpected system check.	1. CA1/CA2 2. Cables 3. Power 4. SC5 card
761F* BA00	Beacon or RLSD not resettable BA = Beaconing station address.	1. CA1 2. Station failure 3. Intermittent CA hardware failure
7620	No stations configured for this port address.	1. MD configuration table incorrect 2. Station not installed
7621 7622*	Open fails. Activate failure.	CA1
7623 7643 SABA	No stations on loop respond to disconnect. Failure to restore loop after beacon test. SA = Station address of station set to beacon. BA = Station address of beaconing station. = 00 if timeout = FF if RLSD	1. CA1 2. Station failure 3. Intermittent CA hardware failure
7660	Time of day clock not set.	TOD clock not set
76FE	Configuration table error.	MD configuration table incorrect

*DPCX error message only

Routine 77, BSC Link Test — Requestor

This routine has Manual Intervention messages; see CA212 for descriptions.

RREN	Error Description	Possible Causes
7701 7710	MCPC error. Invalid basic status.	1. CA2 2. Cables 3. Power 4. SC5 card
7711 7712 7713 7714	DCE error. Halt error. Timeout error. Bad data write text/header.	1. CA5, CA7, CA8 2. CA2 3. Communications line 4. Intermittent on any of the above
7715	Connect timeout.	Systems not ready
7716 7717	Write header (10 NAKs or T.O. received) Write header and test (10 NAKs or T.O. received)	1. Communications line 2. Modem or DCE 3. Intermittent on any of the above
771C	Overrun or underrun.	1. CA2 2. CA5, CA7, CA8 3. Communications line 4. Intermittent on any of the above
7799	Configuration table error.	MD configuration table incorrect

Routine 78, BSC Link Test — Responder

This routine has Manual Intervention messages; see CA212 for descriptions.

RREN	Error Description	Possible Causes
7801 7810	MCPC error. Invalid basic status.	1. CA2 2. Cables 3. Power 4. SC5 card
7811 7812 7813 7814	DCE error. Halt error. Timeout error. Bad data write text/header.	1. CA5, CA7, CA8 2. CA2 3. Communications line 4. Intermittent on any of the above
7815	Connect timeout.	Systems not ready
7818	Read RFT message.	1. Communications line 2. Modem or DCE 3. Intermittent on any of the above
781A 781C	Invalid RFT header received. Overrun or underrun.	1. CA2 2. CA5, CA7, CA8 3. Communications line 4. Intermittent on any of the above
7899	Configuration table error.	MD configuration table incorrect

Routines 79, 80, 81, 82, and 83, 2741 Tests

These routines have Manual Intervention messages; see CA212 for descriptions.

RREN	Error Description	Possible Causes
RR01	MCPC error.	1. CA2 2. Cables 3. Power 4. SC5 card
RR11 RR12 RR13 RR14 RR15 RR16 RR17 RR18 RR19 RR1A RR1B RR1C RR1D RR1E RR1F	Data error. DCE error. Communication line error. Overflow error. Timeout error. Overrun error. Unused error flag on. Function request halt. EOT error. Break signal error. Security error. Unused exception flag on. Error and exception flags on. Input not as expected. Attention never received.	1. CA2 2. CA5, CA8, CA9 3. Cables 4. External modem 5. Communications line 6. Remote station or controller 7. NRZI bit mismatch
RR99	Configuration table error.	MD configuration table incorrect

Routine 84, 2741 Attention Key Test

This routine has Manual Intervention messages; see CA212 for descriptions.

RREN	Error Description	Possible Causes
8401	MCPC error.	1. CA2 2. Cables 3. Power 4. SC5 card
8411 8412 8413 8414 8415 8416 8417 8418 8419 841A 841B 841C 841D 841E 841F	Data error. DCE error. Communication line error. Overflow error. Timeout error. Overrun error. Unused error flag on. Function request halt. EOT error. Break signal error. Security error. Unused exception flag on. Error and exception flags on. Input not as expected. Attention never received.	1. CA2 2. CA5, CA8, CA9 3. Cables 4. External modem 5. Communications line 6. Remote station or controller 7. NRZI bit mismatch
8499	Configuration table error.	MD configuration table incorrect

Routines 85, TTY Auxiliary Line Test, and 86, TTY Auxiliary Echo Test

This routine has Manual Intervention messages; see CA212 for descriptions.

RREN	Error Description	Possible Causes
RR01	MCPC error.	1. CA2 2. Cables 3. Power 4. SC5 card
RR11 RR12 RR13 RR14 RR15 RR16 RR17 RR18 RR19 RR1A RR1B RR1C RR1D	Data error. DCE error. Communication line error. Overflow error. Timeout error. Overrun error. Unused error flag on. Function request halt. EOT error. Break signal error. Security error. Unused exception flag on. Error and exception flags on.	1. CA2 2. CA5, CA8, CA9 3. Cables 4. External modem 5. Communications line 6. Remote station or controller 7. NRZI bit mismatch 1. CA2 2. CA5,CA8,CA9 3. Cables 4. External modem 5. Communications line 6. Remote station or controller

Routine 87, 2741 Auxiliary Line Test

This routine has Manual Intervention messages; see CA212 for descriptions.

RREN	Error Description	Possible Causes
8701	MCPC error.	1. CA2 2. Cables 3. Power 4. SC5 card
8711 8712 8713 8714 8715 8716 8717 8718 8719 871A 871B 871C 871D 871E 871F	Data error. DCE error. Communication line error. Overflow error. Timeout error. Overrun error. Unused error flag on. Function request halt. EOT error. Break signal error. Security error. Unused exception flag on. Error and exception flags on. Input not as expected. Attention never received.	1. CA2 2. CA5, CA8, CA9 3. Cables 4. External modem 5. Communications line 6. Remote station or controller 7. NRZI bit mismatch

Routine 88, One Loop Poll Test

This routine has Manual Intervention messages; see CA212 for descriptions.

RREN	Error Description	Possible Causes
8821* 8822* 8825	Open failure. Activate failure. Open control card in internal active mode failed.	1. CA3 2. Cables 3. CA1

*DPCX error message only

Routine 89, Two-Lobe Bypasser

This routine has Manual Intervention messages; see CA212 for descriptions.

RREN	Error Description	Possible Causes
8925	Open control card in internal active mode failed.	1. CA4 2. CA3 3. Cables 4. CA1

Routine 90, SDLC Test Command — No Data

RREN	Error Description	Possible Causes
9001 9004 9005 9006	Unexpected system check. Unexpected interrupt. Missing or late interrupt. (Offline) Active or recurring interrupt.	1. CA1 2. Cables 3. Power 4. SC5 card
9006	DPCX link test failure without data.	1. CA1 2. Remote station 3. NRZI bit mismatch 4. Cables
900B 901F	System check during routine execution. Unknown cause.	1. CA1 2. Cables 3. Power 4. SCF card
9021 9022* 9031	Open link failed. Activate failure. Link test failed.	1. CA1 2. Remote station 3. NRZI bit mismatch 4. Cables
90E0	Success on retry.	Intermittent hardware or line failure
90FE	Configuration table error.	MD configuration table incorrect

*DPCX error message only

Routine 91, SDLC Test Command -- With Data

RREN	Error Description	Possible Causes
9101 9104 9105 9106	Unexpected system check. Unexpected interrupt. Missing or late interrupt. Active or recurring interrupt.	1. CA1 2. Cables 3. Power 4. SC5 card
9109*	Data compare error.	1. CA1 2. Remote station 3. NRZI bit mismatch 4. Cables
910B	System check during routine execution.	1. CA1 2. Cables 3. Power 4. SCF card
910D*	Link test with data field.	1. CA1 2. Remote station 3. NRZI bit mismatch 4. Cables
911F	Unknown cause.	1. CA1 2. Cables 3. Power 4. SC5 card
9121 9131 9135	Open link failed. Link test failed. Link test failed, data compare error.	1. CA1 2. Remote station 3. NRZI bit mismatch 4. Cables
91E0	Success on retry.	Intermittent hardware or line failure
91FE	Configuration table error.	MD configuration table incorrect

*DPCX error message only

Routine 92, Monitor Mode Test.

RREN	Error Description	Possible Causes
9201 9204 9205 9206	Unexpected system check. Unexpected interrupt. Missing or late interrupt. Active or recurring interrupt.	1. CA1 2. Cables 3. Power 4. SC5 card
9206*	Link test failure.	1. CA1 2. Remote station 3. NRZI bit mismatch 4. Cables
920A* 920B*	No response to set monitor mode. No response to reset monitor mode. or System check during routine execution.	1. Remote station 2. Cables 3. CA1 4. Power 5. SC5 card
920C*	Station not in monitor mode.	1. Remote station 2. Cables
921F	Unknown cause.	1. CA1 2. Cables 3. Power 4. SC5 card
9221 9222* 9230 9231	Open link failed. Activate failure. Disable failed. Link test failed.	1. CA1 2. Remote station 3. NRZI bit mismatch 4. Cables
9234 9236	Monitor mode test failed. Monitor mode not reset.	1. Remote station 2. Cables
92E0	Success on retry.	Intermittent hardware or line failure
92FE	Configuration table error.	MD configuration table incorrect

*DPCX error message only

Routine 93, SDLC Test With User Data.

This routine has Manual Intervention messages; see CA212 for descriptions.

RREN	Error Description	Possible Causes
9301 9304 9305 9306	Unexpected system check. Unexpected interrupt. Missing or late interrupt. Active or recurring interrupt.	1. CA1 2. Cables 3. Power 4. SC5 card
9309*	Data compare error; link test failed.	1. CA1 2. Remote station 3. Cables
930B	System check during routine execution.	1. CA1 2. Cables 3. Power 4. SC5 card
930D*	Link test failed.	1. CA1 2. Remote station 3. Cables
931F	Unknown cause.	1. CA1 2. Cables 3. Power 4. SC5 card
9321 9322* 9331 9335	Open link failed. Activate failure. Link test failed. Link test failed, data compare error.	1. CA1 2. Remote station 3. NRZI bit mismatch 4. Cables
93CE	Data entry error.	Incorrect data
93E0	Success on retry.	Intermittent hardware or line failure
93FE	Configuration table error.	MD configuration table incorrect

*DPCX error message only

Routine 94, Line Analysis

This routine provides a statistical report to the operator and has Manual Intervention messages; see CA212 for descriptions.

RREN	Error Description	Possible Causes
9401 9404 9405 9406 940B 941F	Unexpected system check. Unexpected interrupt. Missing or late interrupt. Active or recurring interrupt. System check during routine execution. Unknown cause.	1. CA1 2. Cables 3. Power 4. SC5 card
9421 9422*	Open link failed. Activate failure.	1. CA1 2. Remote station 3. Cables
94CE	Data entry error.	Incorrect data
94FE	Configuration table error.	MD configuration table incorrect

*DPCX error message only

Routine 95, 384X SDLC Test Command

RREN	Error Description	Possible Causes
9501 9504 9505 9506 950B 951F	Unexpected system check. Unexpected interrupt. Missing or late interrupt. Active or recurring interrupt. System check during routine execution. Unknown cause.	1. CA1 2. Cables 3. Power 4. SC5 card
9520	No stations configured on loop.	MD configuration table incorrect
9521	Open link failed.	1. CA1 2. CA5, CA7, CA8, CA9 3. Cables
9529	Monitor mode recovery on station SA00. SA =FF = Group timeout SA =XX = Beaconing station address	1. 384X loop or station failure 2. 384X failure
9531	Link test failed while not wrapped.	1. 384X failure 2. 384X loop or station failure
9532	Unable to set test mode latch.	384X failure
9536	Set wrap failed.	1. NRZI bit mismatch 2. CA1 3. CA5, CA7, CA8, CA9 4. Cables 5. 384X failure
9537 9543	Link test failed while wrapped. Failure to reset wrap.	384X failure
95E0	Success on retry.	Intermittent hardware or line failure

Routine 96, Remote Loop Data Transfer

RREN	Error Description	Possible Causes
9601 9604 9605 9606 960B 961F	Unexpected system check. Unexpected interrupt. Missing or late interrupt. Active or recurring interrupt. System check during routine execution. Unknown cause.	1. CA1 2. Cables 3. Power 4. SC5 card
9621	Open link failed.	1. CA1 2. CA5, CA7, CA8, CA9 3. Cables
9631	Link test failed while not wrapped.	1. 384X failure 2. 384X loop or station failure
9632	Unable to set test mode latch.	384X failure
9635	Link test failed while not wrapped, data compare error.	1. 384X failure 2. 384X loop or station failure
9636	Wrap failed.	1. CA1 2. CA5, CA7, CA8, CA9 3. Cables 4. 384X failure 5. NRZI bit mismatch
9637 9638 9639	Link test failed while wrapped. Wrapped alternate link test failure. Wrapped link test failure, data compare error.	384X failure
9640	Unwrapped alternate link test failure.	1. CA1 2. CA5, CA7, CA8, CA9 3. Cables 4. 384X failure
9643	Failure to reset wrap.	384X failure
96E0	Success on retry.	Intermittent hardware or line failure

Routine 97, Configuration Self Test to 384X.

RREN	Error Description	Possible Causes
9701 9704 9705 9706 970B 971F	Unexpected system check. Unexpected interrupt. Missing or late interrupt. Active or recurring interrupt. System check during routine execution. Unknown cause.	1. CA1 2. Cables 3. Power 4. SC5 card
9721	Open link failed.	1. CA1 2. CA5, CA7, CA8, CA9 3. Cables
9732	Set test mode failed.	384X failure
9736	Wrap failed.	1. 384X failure 2. NRZI bit mismatch
9745	Configuration self test failed.	384X unit failure
97E0	Success on retry.	Intermittent hardware or line failure

Routine 98, Beacon and Ordinal Sequences

This routine has Manual Intervention messages; see CA212 for descriptions.

RREN	Error Description	Possible Causes
9801 9804 9805 9806 980B 981F	Unexpected system check. Unexpected interrupt. Missing or late interrupt. Active or recurring interrupt. System check during routine execution. Unknown cause.	1. CA1 2. Cables 3. Power 4. SC5 card
9820	No stations in configuration table.	MD configuration table incorrect
9821	Open link failed.	1. CA1 2. CA5, CA7, CA8, CA9 3. Cables
9823	No station responds to disconnect.	1. 384X failure 2. 384X loop or station failure
9832	Failure to set test mode.	1. CA1 2. CA5, CA7, CA8, CA9 3. Cables 4. 384X failure 5. NRZI bit mismatch
9843	Beacon or group timeout not resettable. SABA: SA = Ordinal station address BA = Beaconing station address = FF if group timeout = SA if no configuration response	1. CA1 2. CA5, CA7, CA8, CA9 3. Cables 4. 384X failure 5. 384X loop or station failure
98FE	Configuration table error.	MD configuration table incorrect

Routine 99, Lobe Analysis

RREN	Error Description	Possible Causes
9901 9904 9905 9906 990B 991F	Unexpected system check Unexpected interrupt. Missing or late interrupt. Active or recurring interrupt. System check during routine execution. Unknown cause.	1. CA1 2. Cables 3. Power 4. SC5 card
9920	No stations in configuration table.	MD configuration table incorrect
9921	Open link failed.	1. CA1 2. CA5, CA7, CA8, CA9 3. Cables
9923 9932	No station responds to disconnect. Failure to set test mode.	1. 384X failure 2. 384X loop or station failure 3. NRZI bit mismatch
99CE	Data entry error.	Reenter data
99FE	Configuration table error.	MD configuration table incorrect

Other Messages

Message	Description	CA Feature Possible Cause
XXBC	Test control monitor message denotes status or error.	Refer to ST420.
PA80	Channel I/O hang condition using SDLC adapter card.	1. CA1 2. Channel grant wiring socket SDLC adapter card (CA1)
PA88	Adapter hung condition using BSC/S-S adapter card.	CA2
PA90 YYZZ	With any routine, Selected Device Busy; not available for testing. PA = Address of device YY = Address level ZZ = Address of device; same as PA	Device not available

CA250 Action Plans

1. Verify that the customer has performed the problem recovery procedures specified in the DPPX or DPCX Operators/Operations Guide for the 8100 System.
2. Perform online testing of PA/FAC. Use online TCM and procedures. See CA202 for invocation procedure and CA150 for the FAC test summary.
3. Perform online link-level testing of PA/FAC. Use online TCM and procedures. See CA202 for invocation procedure and CA150 for the FAC test summary.
4. Monitor data link/loop data lines for correct SDLC-BSC/SS line operations. See CA590 for line monitor procedure, CA640 for line discipline descriptions, and CA540 for appropriate line probe points. (**Note:** *Link level tests may be run. See Action Plan 3.*)
5. Obtain the error log for this CA PA and use it for the next action. See CA320 for obtaining the log and CA340 for using the log.
6. Perform online data-link attached loop testing of PA/FAC. Use online TCM and procedures. See CA202 for invocation procedure and CA150 for the FAC test summary. If there is a test error, use the RREN and Action Plan 44 below.
7. Perform online CA test looping with stop on error for PA/FAC. Use online TCM and procedures. See CA202 for invocation procedure and CA150 for the FAC test summary. If there is a test error, use the RREN and Action Plan 44 below.
8. Report to customer that a communications line problem may exist, and that the telephone company/PTT/common carrier/private company should be notified.
9. Report to customer that an OEM modem/communications equipment problem may exist; OEM service representative should be notified.
10. Terminate the service call. Restore the system to normal customer configuration/operation. Advise customer of system condition.
11. Verify the PA of the device/terminal/controller/host is correct. A visual/physical inspection of address wiring should be performed by the local service representative or the remote site personnel. Use appropriate MIMs or service manuals for address wiring locations.
12. Inspect the 8100 System for a duplicate/similar CA feature. Exchange all or component parts of this feature. For a solid failure, use the CA MAP, menu selection A, offline checkout to verify repair action. For an intermittent failure, perform Action Plan 13, offline test looping, to verify repair action.
13. Perform offline free-lance CA test looping with stop on error for PA/FAC. Use offline free-lance invocation procedures (see CA202). See CA150 Communications FAC – Hardware Test Summary for tests.
14. Perform CA MAP, menu selection A, offline for PA/FAC. Use the MD and MD diskette 02. See Chapter 2, CP400, for MD setup and invocation procedures.
15. Not used.
16. Perform CA MAP, menu selection C, Known Test Message for PA/FAC. Use the MD and MD diskette 02. Refer to Chapter 2, CP400, for MD setup and invocation procedures.

    Caution: Prior to starting the CA MAP, compare test message with list of valid messages in CA232. If valid, continue in MAP; if not valid, perform Action Plan 14.

17. Perform CA MAP, menu selection D, Selectable Tests for PA/FAC. Use the MD and MD diskette 02. Refer to Chapter 2, CP400, for MD setup and invocation procedures.

    Caution: If the CA MAP does not have selectable tests for a given PA/FAC, perform Action Plan 14.

18. Loop – use Action Plan 18A.
    Data Link – use Action Plan 18B.

18A. Perform loop analysis.

Routine 75, Group Analysis, is used in conjunction with Routine 76, Loop Beacon and Ordinal Sequence, to isolate intermittent failures in directly attached loops. Routine 76 is run to determine the sequence of the terminals on the loop. With this information, analyze the results of Routine 75 to isolate the failure to a loop segment; that is, two stations and the wire between them.

Group analysis sends an inputted or default message a given number of times to each station and outputs the results, by station, giving:

a. The number of messages sent.
b. The number of FCS errors (errors in messages from station to station).
c. The number of timeout errors (errors in messages to the system from the system).
d. The number of data compare errors (station errors).

The results are compared in the order that the stations are connected on the loop. The point where the majority of errors for a station change from FCS errors to timeout errors indicates the problem area.

If all stations have a majority of FCS errors, it indicates a problem between the last loop station and the loop adapter. If all stations have a majority of timeout errors, it indicates a problem between the loop adapter and the first loop station. Data compare errors indicate a problem in the station not associated with the loop wiring.

Use Figure CA250-1 with the following example:

Routine 76 outputs

PA05 SEQ = 15, 36, 12, 42, 24, 17

Routine 75 outputs

(1) PA01 Station = 12

Msg Sent	Errors		
	FCS	T.O.	Data
100	15	3	0

(2) PA01 Station = 15

Msg Sent	Errors		
	FCS	T.O.	Data
100	20	1	1

(3) PA01 Station = 17

Msg Sent	Errors		
	FCS	T.O.	Data
100	7	15	0

(4) PA01 Station = 24

Msg Sent	Errors		
	FCS	T.O.	Data
100	5	19	0

(5) PA01 Station = 36

Msg Sent	Errors		
	FCS	T.O.	Data
100	18	6	15

(6) PA01 Station = 42

Msg Sent	Errors		
	FCS	T.O.	Data
100	22	4	1

First make a table showing the order of the stations and errors:

	Station	FCS	T.O.	Data
1)	15	20	1	1
2)	36	18	6	15
3)	12	15	3	0
4)	42	22	4	1
5)	24	5	19	0
6)	17	7	15	0

Now analyze the table:

Station 36 has a number of data compare errors. This station has a problem separate from the loop problem.

Stations 15 to 42 have a majority of FCS errors. From station 24 to the end, the majority of errors are timeouts.

This would indicate that the problem was in the transmit portion of station 42, the receive portion of station 24, or the loop between them.

If the problem is in the directly attached loop, go to Action Plan 39.

If the problem is in the data-link attached loop, go to Action Plan 38.

18B. Perform data link analysis.

Group analysis sends an inputted or default message a given number of times to each station and outputs the results, by station, giving:

a. The number of messages sent.

b. The number of FCS errors (errors in messages from station to station).

c. The number of timeout errors (errors in messages to the system from the system).

d. The number of data compare errors (station errors).

The results are compared in the order that the stations are connected on the link. The point where the majority of errors for a station change from FCS errors to timeout errors indicates the problem area.

If all stations have a majority of FCS errors, it indicates a data link problem between the first station and the adapter. If a station has a majority of timeout errors, it indicates a data link problem between the next-to-last station and the last station. Data compare errors indicate a problem in the station not associated with the data link.

Use Figure CA250-2 with the following example:

Routine 75 outputs

(1) PA01 Station = 12

Msg Sent	Errors		
	FCS	T.O.	Data
100	15	3	0

(2) PA01 Station = 15

Msg Sent	Errors		
	FCS	T.O.	Data
100	20	1	1

(3) PA01 Station = 24

Msg Sent	Errors		
	FCS	T.O.	Data
100	15	19	0

(4) PA01 Station = 36

Msg Sent	Errors		
	FCS	T.O.	Data
100	18	6	15

First make a table showing the order of the stations and errors.

	Station	FCS	T.O.	Data
1)	15	20	1	1
2)	36	18	6	15
3)	12	15	3	0
4)	24	15	19	0

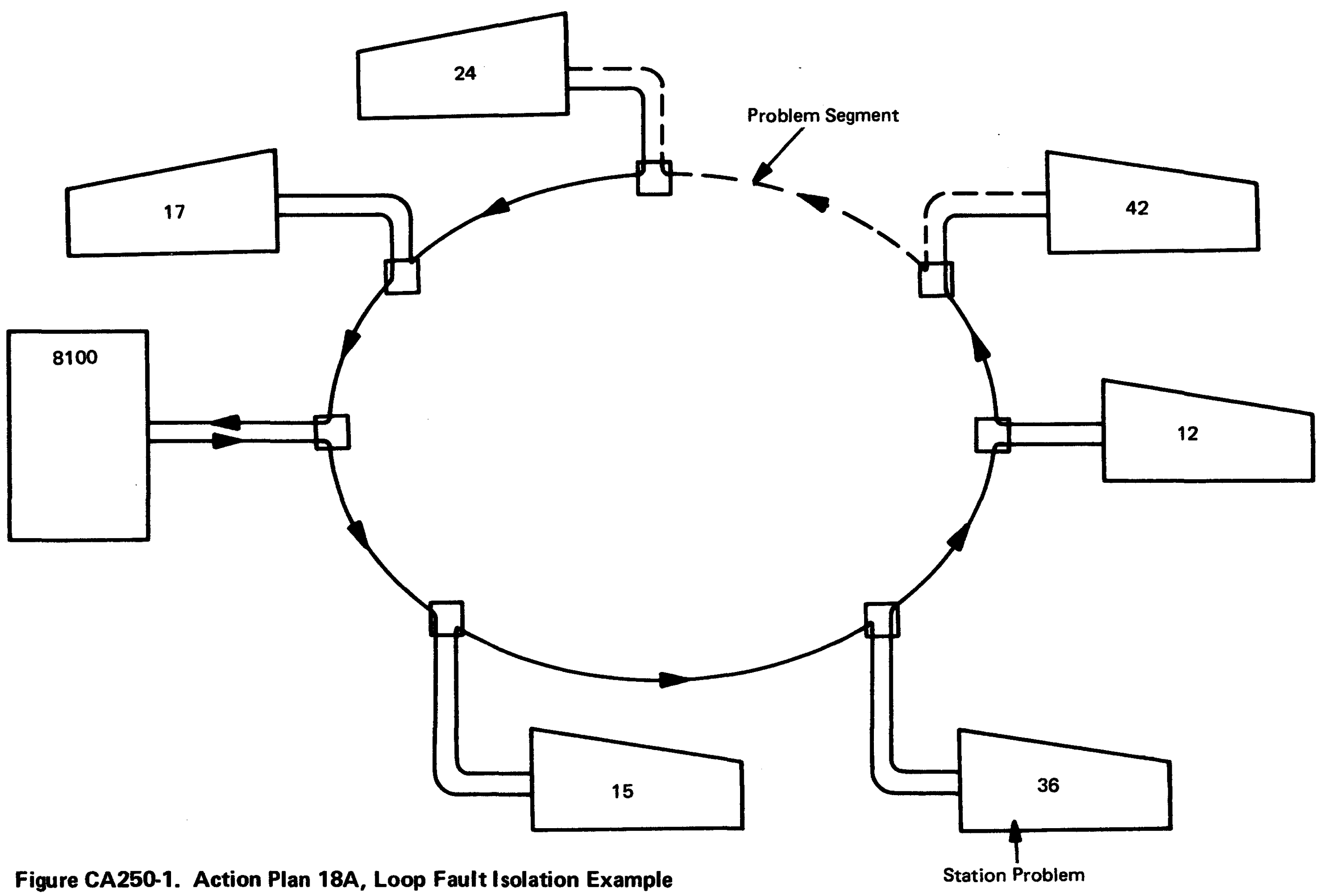


Figure CA250-1. Action Plan 18A, Loop Fault Isolation Example

Now analyze the table:

Station 36 has a number of data compare errors. This station has a problem separate from the data link problem.

Stations 12, 15, 24, and 36 have a majority of FCS errors. This would indicate that the problem is in the data link – problem segment A

Station 24 also has timeout errors, which indicates a problem in the data link – problem segment B

For data compare errors, perform Action Plan 38.

For data link problems, perform Action Plan 8, and, if OEM modems are used at the remote site, perform Action Plan 9. If IBM modems are used at the remote site, perform Action Plan 41.

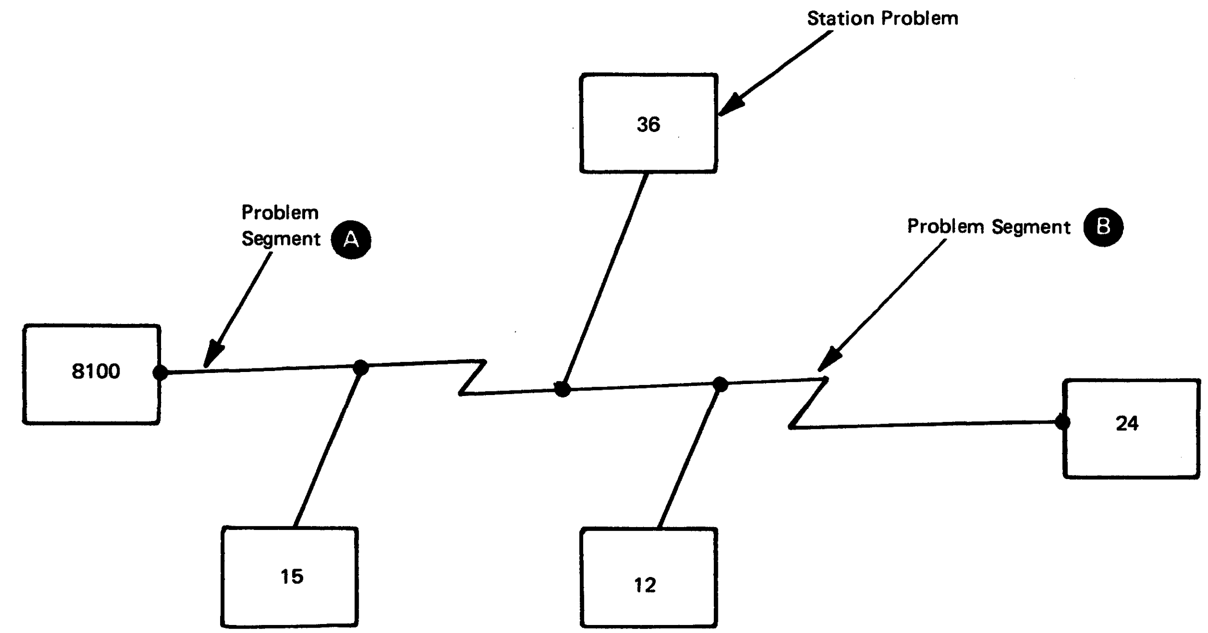


Figure CA250-2. Action Plan 18B, Data Link Fault Isolation Example

19. Perform configuration table check on this CA feature. Compare the hardware configuration table data. See CA150 (FAC hardware summary), CA113 (configuration table), and Chapter 2, CP300, for obtaining/changing the configuration table.
20. Exchange cards CA1 and CA3. See CA511 (card replacement), CA513 (card locations), and CA563 (card jumpers).
21. Repair or replace cable group CAC3. See CA526 (cable replacement), CA525 (cable locations), and CA420/CA430 (cable descriptions).
22. Exchange cards CA1, CA3, and CA4. See CA511 (card replacement), CA513 (card locations), and CA563 (card jumpers).
23. Repair or replace cable groups CAC3 and CAC4. See CA526 (cable replacement), CA525 (cable locations), and CA420/CA430 (cable descriptions).
24. Exchange cards CA1/CA2 and CA5. See CA511 (card replacement), CA513 (card locations), and CA563 (card jumpers).
25. Repair or replace cable group CAC5A. See CA526 (cable replacement), CA525 (cable locations), and CA420/CA430 (cable descriptions).
26. Exchange cards CA1/CA2 and CA5. See CA511 (card replacement), CA513 (card locations), and CA563 (card jumpers).
27. Repair or replace cable group CAC5B. See CA526 (cable replacement), CA525 (cable locations), and CA420/CA430 (cable descriptions).
28. Exchange cards CA1 and CA6. See CA511 (card replacement), CA513 (card locations), and CA563 (card jumpers).
29. Repair or replace cable group CAC6A. See CA526 (cable replacement), CA525 (cable locations), and CA420/CA430 (cable descriptions).
30. Exchange cards CA1 and CA6. See CA511 (card replacement), CA513 (card locations), and CA563 (card jumpers).
31. Repair or replace cable group CAC6B. See CA526 (cable replacement), CA525 (cable locations), and CA420/CA430 (cable descriptions).
32. Exchange cards CA1/CA2 and CA7. See CA511 (card replacement), CA513 (card locations), and CA563 (card jumpers).
33. Repair or replace cable group CAC7. See CA526 (cable replacement), CA525 (cable locations), and CA420/CA430 (cable descriptions).
34. Exchange cards CA1/CA2 and CA8. See CA511 (card replacement), CA513 (card locations), and CA563 (card jumpers).
35. Repair or replace cable group CAC8. See CA526 (cable replacement), CA525 (cable locations), and CA420/CA430 (cable descriptions).
36. Exchange cards CA1/CA2 and CA9. See CA511 (card replacement), CA513 (card locations), and CA563 (card jumpers).
37. Repair or replace cable group CAC9. See CA526 (cable replacement), CA525 (cable locations), and CA420/CA430 (cable descriptions).
38. Perform or request that the customer perform remote site problem determination using remote site problem determination documentation.
39. Perform local site problem determination on the terminal, station, or device using terminal, station, or device local site problem determination documentation.
40. Inspect the data link for an installed cryptographic device (IBM 3845/3846 or similar OEM device). Have the customer remove this device from the data link by either using the bypass switch or physically detaching the device.

    Caution: The data link circuit path must be completed before any further testing.

    Then either restart the CA MAPs or invoke the CA tests that got you to this action plan.
41. Using the IBM modem maintenance manual, perform the IBM modem tests.
42. SCF Action Plan. For SCF address group bus failures, the repair action performed depends upon the machine type in which the communications feature is installed. After determining the machine type, use either the 8130 or the 8140/8101 SCF action plan.

    Caution: Turn power off before removing or installing cards and cables.

    a. 8130 without SCF Expansion Feature Action Plan

       Exchange the SC1 card (see SC111). If the failure still occurs reinstall the original card before continuing.

       Caution: Turn power off before removing or installing cards and cables.

       If the failure still occurs, go to SC section of Chapter 5.

    b. 8130 with SCF Expansion Feature and 8140/8101 SCF Action Plan

       Peform the following action plan steps for suspected SCF problems. If the failure still occurs after exchanging the card, reinstall the original card before continuing.

       Caution: Turn power off before removing or installing cards and cables.

       (1) Check that the SSCF address switches on the card (SC111) are set to the address specified by the PA of the CA control logic (CA112). If the address switches are correct, go to step (2). If the address switches are different, a system configuration problem exists; either the address switches are wrong or the diskette configuration table is wrong. Determine the correct physical address (PA) for customer usage and make the necessary corrections.

       (2) Exchange the SSCF card SC5 (see SC111).

43. Peform the following:
    a. Restart the CA MAPs using the same menu selection.
    b. Perform configuration table inspection and verify with the hardware for this PA/FAC. See Chapter 2, CP300, for how to build a system configuration table.
    c. Perform MD testing using the MD test procedures. See Chapter 2, CP400.
    d. Request aid.
        (1) Obtain and use a new MD diskette 02.
        (2) A MAP design problem may exist.
44. Using the recorded test error message(s), enter CA241 and check/repair/exchange the FRU(s) listed in the Possible Cause column.

    If necessary, refer to the following sections:

    CA511 Card Replacement

    CA513 Card Locations

    CA525 Cable Locations

    CA526 Cable Replacement

    CA530 Standard and Special Voltages

    CA560 Switches, Jumpers, and Straps

    CA412 Net Checks by Error Number Message
45. Perform or request that the customer perform remote site problem determination procedures for a station on the data link attached loop.
46. Perform or request that the customer perform remote site problem determination procedures for the 384X.

CA300 Intermittent Failure Repair Strategy

CA310 General Intermittent Failure Repair Strategy

Intermittent CA feature hardware failures may be detected by looping the CA offline tests or DPPX online tests, or by examining the system error log.

CA311 MAP Test Looping Operation

The CA offline test may be looped using the MAP during offline checkout (MAP menu option A), if you answer YES to the question "DO YOU WANT TO CHECK FOR INTERMITTENT FAILURE BY LOOPING CA TEST?" The test loops continuously, displaying "PAF0 Test Looping" on the MD, until an error is found or until you terminate the test by entering an F at the MD.

If an error is sensed while looping, the MAP diagnoses and isolates the failure in the same manner as a solid failure. After a repair action has been performed, the MAP loops the CA tests to verify the repair.

Note: *If an error is not detected within 5 minutes while looping CA tests, or if the test error message number varies (more than three different error numbers), the MAP operation is ineffective; use the free-lance looping operation described in CA313.*

CA312 System Error Log

DPPX and DPCX record any communication feature failure that occurs during system operation in their error logs.

Using the utility section of the appropriate operating system (see CP700 or CP800 of Chapter 2), obtain all communication-associated error log entries. If no CA errors were recorded in the log, no communication feature hardware failures occurred during system operation.

The information in the log can determine the type of failure that occurred, and the action plan to correct this failure. See CA340 for how to use the error log information, and CA350 for the action plans. The repair action can be verified by running the CA tests using the free-lance operation provided by the MD (see Chapter 2, CP462).

After correcting the problem, return the system to the customer. Again examine the error log for any CA failures, after the customer has used that part of the system that failed. If the error log indicates the same failure, then perform the next step in the action plan. If the error log contains no CA failures, you can end the repair action.

CA313 Free-Lance Looping Operation

The offline tests may be looped using the free-lance operation provided by the MD (see Chapter 2, CP462). The test invocation message is PAB 11B (see CA202). The test loops continuously until an error is detected or until you terminate the test by entering an F on the MD keypad.

If an error is detected while looping, the test error message is displayed on the MD. Record this message and use CA250, Action Plans, to analyze and repair the failure. Once a repair action has been performed, loop the CA test for at least 5 minutes to verify the repair.

If no error is detected by looping to tests, examine the system error log described in CA312.

CA320 How to Obtain Error Log Information

See the utility section of the appropriate operating system in Chapter 2 (CP700 or CP800) for the procedure on how to retrieve an error log. Search the error log for any entries of a failing communications feature using its PA.

CA330 Error Log Formats and Meanings

The format of the error log entries depends on whether the customer is using DPPX or DPCX. For DPPX, see CA331; for DPCX, see CA332.

CA331 DPPX

DPPX Error Log Records

All communications attachment feature (hardware) problems are recorded/reported by DPPX using the class-5, subclass-1 error log record. There are five categories of communications records:

Category	Device Type (Alpha)
SDLC – Primary	M (hex 40D4)
SDLC – Secondary	H (hex 40C8)
BSC	B (hex 40C2)
Start/Stop – 2741	C (hex 40C3)
Start/Stop – TTY	Y (hex 40E8)

Note: *Log record output on a device with a width of 80 characters or greater will cause the record format to be modified; that is, two 40-character lines will be on one 80-character line.*

DPPX SDLC Primary – Device Type M

Header I

CLASS 05 SUBCLASS 01 OPTION (5) If bit 0 of Option = 1

DATE YY.DDD TIME HH/MM/SS

Header II

CLASS 05 SUBCLASS 01 OPTION (5) If bit 0 of Option = 0

DATE YY.DDD SEQ NO. (1)

Record

PA (2) SCA (3) DT (4)

CRC (7) COMPSTAT (8) ARC (9)

DATA (11) RES (12) CNT (13)

IOEP (14) ADWA (15)

CA (16) CPR (17) FRWA (18)

RES (19)

Extended Data

D01 (24,25)	D02 (26,27)	D03 (28,29)	D04 (30,31)
D05 (32,33)	D06 (34,35)	D07 (36,37)	D08 (38,39)
D09 (40,41)	D10 (42,43)	D11 (44,45)	

Content

(1) SEQ NO. Sequence Number of the condition/incident log record. This is part of the header II format which is provided via DISPLAY.ERRLOG if bit 0 of the Option Mask (field 5) = 0. If bit 0 = 1, then header I is provided with a time stamp. The format of the time stamp is hour/minute/second.

With either header, a date field is provided, consisting of the year and Julian date.

Date is only valid when the customer sets the date after every IPL using the SET.DATE command. Time is only valid when the customer runs DPPX with Timer Management and sets the time after every IPL using the SET.TOD command.

(2) PA Physical Adapter address – Byte 0 of the FRB.

(3) SCA Secondary Component Address – physical station address. Bytes 26 and 27 of the FRB. Valid only when COMPSTAT (field 8) = [hex 01 (attention)] *or* [hex 02 (exception) *and* ARC (field 9) has bits 3, 4, 5, and/or 6 set].

(4) DT Device Type – hex 40D4

(5) OPTION Option Mask – Byte 4 of DPPX header:

Bit 0 – 1 Time Stamp (header I)
– 0 Sequence Number (header II)

Bit 1 – 1 BCLE Present

Bit 2 – 1 Extended Data Present

Bits 3–7 – 1 Specifies format for Extended Data

(7) CRC FDM Request Code (hex) – Byte 1 of the FRB:

00 = Open

01 = Sense

04 = Close

06 = Initialize Secondary

08 = Take Group List

0A = Read-Write Turnaround

40 = Activate Link

(8) COMPSTAT Completion Status (hex) – Byte 2 of FRB

and

(9) ARC Adapter Status – Byte 3 of FRB

Status is indicated to the user via completion codes summarized in register 2 (byte 2 of the FRB), register 3 (byte 3 of the FRB), and register 5. This allows for an extended means of reporting status. Registers 30 and 31 contain a valid pointer to the MDLCB at the time any completion status is indicated.

COMPSTAT = hex 08 – Function Request Status

A value of hex 08 in register 2 indicates that register 3 contains status normally pertaining to the completion of a function request or a "system request"; e.g., Quiesce.

The contents of register 3 are defined as:

Bit 0 – Return request interlock (See Note 1 below.)

Bit 1 – Normal Function Request complete

Bit 2 – Reserved – 0

Bit 3 – Reserved – 0

Bit 4 – Link quiesced

Bit 5 – RLSD error (direct-attached loop only)

Bit 6 – Wire test failure (direct-attached loop only)

Bit 7 – Invalid Function Request

COMPSTAT = hex 01 – Data Transfer Status

A value of a hex 01 in register 2 indicates that register 3 contains status pertaining to the transmitting and receiving of data.

Note: *Registers 12 and 13 contain a valid pointer to the SDLCB.*

The contents of register 3 are defined as:

Bit 0 – Return request interlock (See Note 1 below.)

Bit 1 – Write message confirmed

Bit 2 – Write list complete

Bit 3 – Reserved – 0

Bit 4 – Read flag buffer indication

Bit 5 – Read message available

Bit 6 – 0 data "I" frame received

Bit 7 – RD message available, truncated data

COMPSTAT = hex 04 – Recoverable CHIO Errors

A value of hex 04 in register 2 indicates that register 3 contains status pertaining to recoverable channel I/O errors. These errors are most likely the result of system resource allocation and/or system loading problems. The adapter recovers these errors and attempts to continue processing. Some incoming messages may be lost before recovery is completed.

The contents of register 3 are defined as:

Bit 0 – Return request interlock (See Note 1 below.)

Bit 1 – CHIO overrun

Bit 2 – Buffer overrun

Bit 3 – Receive control overrun

Bit 4 – Reserved – 0

Bit 5 – CHIO underrun

Bit 6 – Reserved – 0

Bit 7 – Reserved – 0

COMPSTAT = hex 0C – Unrecoverable Error Status

A value of hex 0C in register 2 indicates that register 3 contains unrecoverable error status. An error condition has been detected from which recovery is not possible within the framework of operational adapter code. At completion time, an automatic "Sense" function is performed by the adapter and is available for logging, except on MCPC. Following the auto sense, an Adapter Reset command is issued to the adapter, thereby ending all adapter activity.

The contents of register 3 are defined as:

- Bit 0 – 0 (return request interlock-not used)
- Bit 1 – 0
- Bit 2 – DCE DSR error
- Bit 3 – 0
- Bit 4 – Reserved – 0
- Bit 5 – Machine check
- Bit 6 – Write failure
- Bit 7 – Invalid hardware status

COMPSTAT = hex 02 – Exception Status

A value of hex 02 in register 2 indicates that the bit setting of register 3 refers to various status conditions in register 5.

Note: *Registers 12 and 13 contain a valid pointer to the SDLCB when register 3, bits 3, 4, 5, or 6 are set.*

The contents of register 3 are defined as:

- Bit 0 – Return request interlock (See Note 1 below.)
- Bit 1 – Status extension 1 – Register 5 contains system T.O. status.

  The contents of register 5 are defined as:
  - Bit 0 – Return request interlock (See Note 1 below.)
  - Bit 1 – "N" group timeouts
  - Bit 2 – Non-productive receive timeout
  - Bit 3 – Intermediate OPEN timeout
  - Bit 4 – Reserved – 0
  - Bit 5 – Reserved – 0
  - Bit 6 – Group "on-line"
  - Bit 7 – All groups timed out – data link only
- Bit 2 – Status extension 2 – Register 5 contains system status.

  The contents of register 5 are defined as:
  - Bit 0 – Return request interlock (See Note 1 below.)
  - Bit 1 – FCS error
  - Bit 2 – Invalid address
  - Bit 3 – Invalid sequence error
  - Bit 4 – Invalid address reason code
  - Bit 5 – Reserved – 0
  - Bit 6 – Reserved – 0
  - Bit 7 – CTS Fell
- Bit 3 – Status Extension 3 – Register 5 contains station status.

  The contents of register 5 are defined as:
  - Bit 0 – Return request interlock (See Note 1 below.)
  - Bit 1 – Disconnect acknowledged
  - Bit 2 – SNRM acknowledged
  - Bit 3 – ROL received
  - Bit 4 – Command reject received
  - Bit 5 – Unexpected or duplicate nonsequenced response
  - Bit 6 – SIM acknowledged
  - Bit 7 – RQI received
- Bit 4 – Status extension 4 – Register 5 contains station status.

  The contents of register 5 are defined as:
  - Bit 0 – Return request interlock (See Note 1 below.)
  - Bit 1 – Primary busy
  - Bit 2 – "N" contact poll retries
  - Bit 3 – "N" write retries
  - Bit 4 – Lost data
  - Bit 5 – Too short I-frame received
  - Bit 6 – "N" Ns errors
  - Bit 7 – No receive buffer
- Bit 5 – Status Extension 5 – Register 5 contains station status.

  The contents of register 5 are defined as:
  - Bit 0 – Return request interlock (See Note 1 below.)
  - Bit 1 – Secondary station moved
  - Bit 2 – Reserved – 0
  - Bit 3 – Reserved – 0
  - Bit 4 – NR sequence error
  - Bit 5 – Reserved – 0
  - Bit 6 – Data with response
  - Bit 7 – Invalid response received
- Bit 6 – Status extension 6 – Register 5 contains diagnostic status.

  The contents of register 5 are defined as:
  - Bit 0 – Return request interlock (See Note 1 below.)
  - Bit 1 – Beacon received
  - Bit 2 – Link test received
  - Bit 3 – Reserved – 0
  - Bit 4 – Configure received
  - Bit 5 – No response received
  - Bit 6 – Configure response with no data
  - Bit 7 – Reserved – 0

Bit 7 — Status extension 7 — Register 5 contains miscellaneous status.

The contents of register 5 are defined as:

Bit 0 — Return request interlock (See Note 1 below.)

Bit 1 — "N" supervisory retries

Bit 2 — WCL available

Bit 3 — Received "A,C" bytes available

Bit 4 — Zero

Bit 5 — Zero

Bit 6 — Zero

Bit 7 — Zero

Note 1: *Return request interlock (Bit 0 of register 3 or 5). This status code provides the adapter a means of returning pertinent status information at intermediate points in the processing when no I/O interrrupt is pending. This bit is set in conjunction with some other status bit in register 3 or register 5. When this bit is set, the adapter requires that the user not turn off the PIRR to this level such that an immediate return will be made to the adapter via a branch to registers 26 and 27.*

(11)	DATA	Bytes 4–7 of the FRB.
(12)	RES	Reserved — Bytes 8 and 9 of the FRB — N/A.
(13)	CNT	Count — Bytes 10 and 11 of the FRB.
(14)	IOEP	I/O Interrupt Entry Point — Bytes 12–15 of the FRB.
(15)	ADWA	Adapter Work Area Address — Bytes 16–19 of the FRB — N/A.
(16)	CA	Channel Address — Byte 24 of the FRB — N/A.
(17)	CPR	Channel Pointer Address — Byte 25 of the FRB — N/A.
(18)	FRWA	Function Request Work Area Address — Bytes 20–23 of the FRB — N/A.
(19)	RES	Reserved — Bytes 28–31 of the FRB — N/A.
(24)	Register 5	The meaning of this field is a function of the values in COMPSTAT (field 8) and ARC (field 9). Decode the ARC (register 3) hex value to binary and review fields 8 and 9, COMPSTAT = hex 02, Exception Status.

This hex field has the following meaning:

COMPSTAT	ARC
02	40/C0 — System T.O. Status
02	20/A0 — System Status
02	10/90 — Station Status
02	08/83 — Station Status
02	08/88 — Station Status
02	04/84 — Station Status
02	02/82 — Diagnostic Status
02	01/81 — Miscellaneous Status

Note: *Fields 25 through 27 contain Command Reject Status and are valid only when COMPSTAT (field 8) = hex 02 (exception) and ARC (field 9) = hex 10 or hex 90 (station status) and register 5 (field 24) has bit 4 set (CMDREJ received).*

(25) Command Reject Status — Command — the control field that caused the CMDR exception to be established.

(26) Command Reject Status — NR, 0, NS, 0 — the secondary station send (NS) and receive (NR) sequence counts that existed immediately prior to detaching the CMDR exception. It is defined as follows:

Bits 0–2— Count of receive frames

Bit 3 — 0

Bits 4–6— Count of send frames

Bit 7 — 0

(27) Command Reject Status — Reason Code — the reason for the CMDR exception, where:

Bits 0–3— 0

Bit 4 — The received (NR) sequence count contained in the control field which is returned in the first byte (field 25) is out of range.

Bit 5 — The information field associated with an error-free frame was too long for the buffer provided. The frame was not accepted. This bit is mutually exclusive with bit 7.

Bit 6 — The control field received and returned in the first byte (field 25) was considered invalid because the frame contained an information field which is not allowed with that specific command. Bit 7 must be on whenever this bit is on.

Bit 7 — The control field received and returned in the first byte (field 25) represents an invalid or nonimplemented command.

Note: *Fields 28 through 39 contain sense data and are valid only when COMPSTAT (field 8) = hex 0C (complete with error) except when ARC (field 9) = hex 04 (machine check).*

(28) Byte 0 of Sense Data

BSTAT has following meanings:

Bit 0 — CS HALT

Bit 1 — Xmit EOL

Bit 2 — Rcv Ctrl Entry

Bit 3 — Modem/Timer

Bit 4 — Exception

Bit 5 — MC/PC

Bit 6 — Enabled

Bit 7 — Intrpt Request

(29) Byte 1 of Sense Data

RCTRL has the following meanings:

Bit 0 — Rcv Mode
Bit 1 — Buffer 1 Valid
Bit 2 — Buffer 2 Valid
Bit 3 — 0
Bit 4 — Specific Addr Valid
Bit 5 — Group Addr Valid
Bit 6 — Intr On Contin Flags
Bit 7 — Enable 15 Ones

(30) Byte 2 of Sense Data

RSTAT has the following meanings:

Bit 0 — Inv Seq/Adr
Bit 1 — Byte Overrun
Bit 2 — Rcv Ctrl Entry
Bit 3 — 15 Ones
Bit 4 — Ctrl Overrun
Bit 5 — Traffic
Bit 6 — Rcv CS Halt
Bit 7 — Ad In Sync

(31) Byte 3 of Sense Data

TCTRL has the following meanings:

Bit 0 — Xmit Mode
Bit 1 — Ctrl Valid
Bit 2 — NRZI
Bit 3 — Load Serializer
Bit 4 — Flag
Bit 5 — Cont Char
Bit 6 — FCS Seq + Flag
Bit 7 — Inhbt Zero Insert

(32) Byte 4 of Sense Data

TSTAT has the following meanings:

Bit 0 — Reserved
Bit 1 — Reserved
Bit 2 — Reserved
Bit 3 — Reserved
Bit 4 — Reserved
Bit 5 — TTO IR
Bit 6 — Xmit CS Halt
Bit 7 — Byte Underrun

(33) Byte 5 of Sense Data

MCTRL has the following meanings:

Bit 0 — DTR
Bit 1 — RTS
Bit 2 — Select Standby
Bit 3 — Data Rate Select
Bit 4 — Local Test
Bit 5 — Disable Ring
Bit 6 — Disable RLSD
Bit 7 — Disable CTS

(34) Byte 6 of Sense Data

MSTAT has the following meanings:

Bit 0 — Timer 1
Bit 1 — Timer 2
Bit 2 — DSR
Bit 3 — CTS
Bit 4 — DSR Trans
Bit 5 — Ring Trans
Bit 6 — RSLD Trans
Bit 7 — CTS Trans

(35) Byte 7 of Sense Data

DCTRL has the following meanings:

Bit 0 — Wrap
Bit 1 — T3/T4 Test
Bit 2 — New Sync
Bit 3 — Xmit New Sync
Bit 4 — Diag Clk
Bit 5 — Diag Timer Ctrl
Bit 6 — RLSD
Bit 7 — Ring

(36) Byte 8 of Sense Data

PROGSTAT 1 = register 26 (I/O Interrupt Entry Point)

(37) Byte 9 of Sense Data

PROGSTAT 1 = register 27 (I/O Interrupt Entry Point)

(38) Byte 10 of Sense Data

PROGSTAT 2 = register 18 (sublink register)

(39) Byte 11 of Sense Data

PROGSTAT 2 = register 19 (sublink register)

(40) Group Address — Assigned — Valid only when COMPSTAT (field 8) = hex 01 (attention) or (hex 02 (exception) and ARC has bits 3, 4, 5, and/or 6 set). This is the assigned address that was expected.

(41) Group Address – Polled – Valid only when Group error has occurred. This is the actual address that was polled.

(42,43) Performance Counter – Total Frames = Good Inbound + Good Outbound + Bad Inbound + Bad Outbound. This field is maintained by station address.

(44,45) Performance Counter – Total Retries = Bad Inbound + Bad Outbound. This field is maintained by station address.

DPPX SDLC Secondary – Device Type H

Header I

CLASS SUBCLASS OPTION (5) If bit 0 of Option = 1

DATE YY.DDD TIME HH/MM/SS

Header II

CLASS SUBCLASS OPTION (5) If bit 0 of Option = 0

DATE YY.DDD SEQ NO. (1)

Record

PA (2) SCA (3) DT (4)

CRC (7) COMPSTAT (8) ARC (9)

DATA (11) RES (12) CNT (13)

IOEP (14) ADWA (15)

CA (16) CPR (17) FRWA (18)

RES (19)

Extended Data

D01 (24,25) D02 (26,27) D03 (28,29) D04 (30,31)

D05 (32,33) D06 (34,35) D07 (36,37) D08 (38,39)

D09 (40,41) D10 (42,43) D11 (44,45)

Content

(1) SEQ NO. Sequence Number of the CIL record.
This is part of the header II format which is provided via DISPLAY.ERRLOG if bit 0 of the Option Mask (field 5) = 0. If bit 0 = 1, then header I is provided with a time stamp. The format of the time stamp is hour/minute/second.

With either header, a date field is provided, consisting of the year and Julian date.

Date is only valid when the customer sets the date after every IPL using the SET.DATE command. Time is only valid when the customer opts to run DPPX with Timer Management and sets the time after every IPL using the SET.TOD command.

(2) PA Physical Adapter address. Byte 0 of the FRB.

(3) SCA Secondary Component Address – physical station address Bytes 26 and 27 of the FRB.

(4) DT Device Type – H (hex 40C8)

(5) OPTION Option Mask – Byte 4 of DPPX header:

Bit 0 – 1 Time Stamp (header I)
– 0 Sequence Number (header II)

Bit 1 – 1 BCLE Present

Bit 2 – 1 Extended Data Present

Bits 3–7 – 1 Specifies format for Extended Data

(7) CRC FDM Request Code – Byte 1 of the FRB in hex:

00 = Open

01 = Sense

02 = Write

04 = Close

05 = Pre-Wrap Test

09 = Wrap Data – Adapter

11 = Interface Select

0D = Wrap Data – DCE

(8) COMPSTAT Completion Status – Byte 2 of FRB

and

(9) ARC Adapter Status – Byte 3 of FRB

COMPSTAT = hex XC (register 2)

Complete With Error	ARC
Invalid Status	Register 3, bit 0
DCE Error	Register 3, bit 2
WRTE T.O.	Register 3, bit 3
MC	Register 3, bit 5

COMPSTAT = hex X2 (register 2)

Exception	ARC
SNRM RCVD (Note 1)	Register 3, bit 0
Overrun	Register 3, bit 4
Underrun	Register 3, bit 5
Conn Prob	Register 3, bit 6
Dump Msg	Register 3, bit 7
Rtry T.O. (Note 2)	Register 3, bit 3

COMPSTAT = hex X1 (register 2)

Attention	ARC
Link Test (Note 3)	Register 3, bit 1
NPRO/RCV Ovrn	Register 3, bit 2
Lost Data	Register 3, bit 3
RD FBI	Register 3, bit 5

COMPSTAT = hex X9 (register 2)

Complete With Attention	ARC
Lost Data	Register 3, bit 3

Notes:

1. Only when in Contact Mode.

2. Log one record after the 40th T.O. is counted on leased line only.

3. On "Link Test" received, register 3, bit 1 is set. After the Link Test has been responded to, "Link Test" (register 3, bit 1) and Rd Msg Avail (register 3, bit 6) are set.

For further bit descriptions, see "Abbreviation Descriptions" at the end of this device type.

(11)	DATA	Bytes 4–7 of the FRB – N/A.
(12)	RES	Reserved – Bytes 8 and 9 of the FRB – N/A.
(13)	CNT	Count – Bytes 10 and 11 of the FRB – N/A.
(14)	IOEP	I/O Interrupt Entry Point – Bytes 12–15 of the FRB.
(15)	ADWA	Adapter Work Area Address – Bytes 16–19 of the FRB – N/A.
(16)	CA	Channel Address – Byte 24 of the FRB – N/A.
(17)	CPR	Channel Pointer Register – Byte 25 of the FRB – N/A.
(18)	FRWA	Function Request Work Area Address – Bytes 20–23 of the FRB – N/A.
(19)	RES	Reserved – Bytes 28–31 of the FRB – N/A.

Note: *Fields (24) through (41) contain Sense Data and are valid only when COMPSTAT (field 8) = hex XC (complete with error) except when ARC (field 9) = hex 04 (machine check).*

(24) Byte 0 of Sense Data.

BSTAT has following meanings:

- Bit 0 – CHIO Halt
- Bit 1 – Xmit EOL
- Bit 2 – RCV CTRL Entry
- Bit 3 – Modem/Timer
- Bit 4 – Exception
- Bit 5 – MC/PC
- Bit 6 – Enabled
- Bit 7 – Intrpt Request

(25) Byte 1 of Sense Data.

RCTRL has the following meanings:

- Bit 0 – RCV Mode
- Bit 1 – Alternate Buffer A Valid
- Bit 2 – Alternate Buffer B Valid
- Bit 3 – Reserved
- Bit 4 – Specific Addr Valid
- Bit 5 – Group Addr Valid
- Bit 6 – Intrpt Cont Flags
- Bit 7 – Enable 15 Ones

(26) Byte 2 of Sense Data.

RSTAT has the following meanings:

- Bit 0 – Inv Seq/Addr
- Bit 1 – Byte Overrun
- Bit 2 – RCV CTRL Entry
- Bit 3 – 15 Ones
- Bit 4 – Ctrl Overrun
- Bit 5 – (FCS Good)/Traffic
- Bit 6 – RCV CHIO Halt
- Bit 7 – AD In Sync

(27) Byte 3 of Sense Data.

TCTRL has the following meanings:

- Bit 0 – Xmit Mode
- Bit 1 – CTRL Valid
- Bit 2 – NRZI
- Bit 3 – Load Serializer
- Bit 4 – Flag
- Bit 5 – Cont Char
- Bit 6 – FCS Seq + Flag
- Bit 7 – Inhbt Zero Insert

(28) Byte 4 of Sense Data.

TSTAT has the following meanings:

- Bit 0 – Reserved
- Bit 1 – Reserved
- Bit 2 – Reserved
- Bit 3 – Reserved
- Bit 4 – Reserved
- Bit 5 – TTO IR
- Bit 6 – Xmit CHIO Halt
- Bit 7 – Byte Underrun

(29) Byte 5 of Sense Data.

MCTRL has the following meaning:

- Bit 0 – DTR
- Bit 1 – RTS
- Bit 2 – Select Standby
- Bit 3 – Data Rate Select
- Bit 4 – Local Test
- Bit 5 – Disable Ring
- Bit 6 – Disable RLSD
- Bit 7 – Disable Xmit CTS

(30) Byte 6 of Sense Data.

MSTAT has the following meanings:

Bit 0 — Timer 1 (Fine)
Bit 1 — Timer 2 (Coarse)
Bit 2 — DSR
Bit 3 — CTS
Bit 4 — DSR Trans
Bit 5 — Ring Trans
Bit 6 — RSLD Trans
Bit 7 — CTS Trans

(31) Byte 7 of Sense Data.

DCTRL has the following meanings:

Bit 0 — Wrap
Bit 1 — T3/T4 Test
Bit 2 — New Sync
Bit 3 — TX New Sync
Bit 4 — Diag Clk
Bit 5 — Diag Timer Ctrl
Bit 6 — RLSD
Bit 7 — Ring

(32) Byte 8 of Sense Data.

TDCHCV has the following meanings:

Bit 0 — X
Bit 1 — X
Bit 2 — PTR Reg 0
Bit 3 — PTR Reg 1
Bit 4 — PTR Reg 2
Bit 5 — PTR Reg 3
Bit 6 — X
Bit 7 — 0

(33) Byte 9 of Sense Data.

TCCHCV has the following meaning:

Bit 0 — X
Bit 1 — X
Bit 2 — PTR Reg 0
Bit 3 — PTR Reg 1
Bit 4 — PTR Reg 2
Bit 5 — PTR Reg 3
Bit 6 — PTR Reg 4
Bit 7 — 0

(34) Byte 10 of Sense Data.

TDCTH has the following meaning:

Bit 0 — Data Chain
Bit 1 — Frame Chain
Bit 2 — Pad Insert
Bit 3 — FTA
Bit 4 — Xmit Trn Off
Bit 5 — 0
Bit 6 — 0
Bit 7 — Count 256

(35) Byte 11 of Sense Data.

TDCTL has the following meaning:

Bit 0 — Count 128
Bit 1 — Count 64
Bit 2 — Count 32
Bit 3 — Count 16
Bit 4 — Count 8
Bit 5 — Count 4
Bit 6 — Count 2
Bit 7 — Count 1

(36) Byte 12 of Sense Data.

RDCHCV has the following meaning:

Bit 0 — 1
Bit 1 — 0
Bit 2 — PTR Reg 0
Bit 3 — PTR Reg 1
Bit 4 — PTR Reg 2
Bit 5 — PTR Reg 3
Bit 6 — X
Bit 7 — 0

(37) Byte 13 of Sense Data.

RCCHCV has the following meaning:

Bit 0 — 1
Bit 1 — 0
Bit 2 — PTR Reg 0
Bit 3 — PTR Reg 1
Bit 4 — PTR Reg 2
Bit 5 — PTR Reg 3
Bit 6 — PTR Reg 4
Bit 7 — 0

(38) Byte 14 of Sense Data.

RDCTH has the following meaning:

- Bit 0 — Valid Entry
- Bit 1 — Invalid Sequence
- Bit 2 — FCS Valid
- Bit 3 — Buffer B Entry
- Bit 4 — Byte Overrun
- Bit 5 — BFR Overrun
- Bit 6 — Flag Received
- Bit 7 — Count 256

(39) Byte 15 of Sense Data.

RDCTL has the following meaning:

- Bit 0 — Count 128
- Bit 1 — Count 64
- Bit 2 — Count 32
- Bit 3 — Count 16
- Bit 4 — Count 8
- Bit 5 — Count 4
- Bit 6 — Count 2
- Bit 7 — Count 1

(40) Byte 16 of Sense Data.

RBLNG has the following meaning:

- Bit 0 — Count 256
- Bit 1 — Count 128
- Bit 2 — Count 64
- Bit 3 — Count 32
- Bit 4 — Count 16
- Bit 5 — Count 8
- Bit 6 — Count 4
- Bit 7 — Count 2

(41) Byte 17 of Sense Data

RCCCNT has the following meanings:

- Bit 0 — Count 512
- Bit 1 — Count 256
- Bit 2 — Count 128
- Bit 3 — Count 64
- Bit 4 — Count 32
- Bit 5 — Count 16
- Bit 6 — Count 8
- Bit 7 — Count 4

(42) Register 13 — This field contains useful information under the following condition:

On a WRITE FR (field 7 = hex 02) with a completion status of exception (field 8 = hex X2) and bit 7 of adapter status (field 9) set (Dump MSG).

For further bit descriptions, see "Abbreviation Descriptions" at the end of this device type.

Register 13 has the following meaning:

- Bit 0 — FCS
- Bit 1 — PMY ABRT
- Bit 2 — Not used
- Bit 3 — Not used
- Bit 4 — NR SEQ ERR**
- Bit 5 — WRNG LNTH MSG
- Bit 6 — DATA W/CMD**
- Bit 7 — INV CMD**

Where ** are command reject conditions.

Note: *Fields (43) through (45) contain command reject status and are valid only when CRC (field 7) = hex 02. (Write Function Request) with a COMPSTAT (field 8) of hex X2 (exception) and bit 7 of adapter status (field 9) is set (Dump MSG) and register 13 has bit 4, 6, or 7 set.*

(43) Command Reject Status — Command — The control field that caused the CMDR exception to be established.

(44) Command Reject Status — NR, 0, NS, 0 — the secondary station send (NS) and receive (NR) sequence counts that existed immediately prior to detaching the CMDR exception.

Defined as follows:

- Bits 0–2 — Count of receive frames
- Bit 3 — 0
- Bits 4–6 — Count of send frames
- Bit 7 — 0

(45) Command Reject Status — Reason Code — the reason for the CMDR exception where:

- Bits 0–3 — 0
- Bit 4 — The received (NR) sequence count contained in the control field which is returned in the first byte (field 43) is out of range.
- Bit 5 — The information field associated with an error-free frame was too long for the buffer provided. The frame was not accepted. This bit is mutually exclusive with bit 7.
- Bit 6 — The control field received and returned in the first byte (field 43) was considered invalid because the frame contained an information field which is not allowed with that specific command. Bit 7 must be on whenever this bit is on.
- Bit 7 — The control field received and returned in the first byte (field 43) represents an invalid or non-implemented command.

Abbreviation Descriptions

Note: *The following abbreviations, described in detail, apply to DPPX record device type H.*

Abbreviation	Description
CONN PROB	Some condition exists in the link that is hindering proper establishment or re-establishment of communication with the remote station. This status is posted following 20 Write Retries, 20 ROL, 20 CMDR, 20 XID, 20 NSA, 20 RQI, or any combination of these. The accumulator is reset whenever a Write (I-Frame) is confirmed.
DATA W/CMD*	(Register 13, Bit 6) – A Command Reject condition resulted from the receipt of a data field with an otherwise valid command, for which no data field is defined. No action is required by the IPC as appropriate recovery action is taken by the adapter. This bit is on in conjunction with INVAL CMD. (Frame had good FCS.)
DCE ERR	A DCE interrupt or other detectable DCE condition of a nonexpected nature has occurred (e.g. DSR dropped when it should be on).
DISC RCVD	Set Disconnect Response Mode command received and acknowledged. (20 "DISC RCVDs" in succession = "CONN PROB".) The NSA response is transmitted before the status is returned.
DUMP MSG	One or more significant errors have occurred, and the actual bit representation may be found in register 13. Bits 4, 6, and 7 are Command Rejectable conditions. Full CMDREJ Status information is available in the DLCB. All data in the buffer is bad due to this condition; buffer is reused by the adapter unless it is reallocated. No action by the system code is taken as appropriate recovery action is taken by the adapter.
FCS	(Register 13, Bit 0) – The CRC check failed for the message last received.
IDLE T.O.	On a switched or leased line, there has been inactivity (no flags received) for at least 20 seconds. If applicable, this status takes priority over Non-Productive Timeout (NPRO/RCV OVRN).
INV CMD*	(Register 13, Bit 7) – A Command Reject condition resulted from receipt of an undefined or nonimplemented command field in a frame which has good FCS. No action is taken by the system code as appropriate recovery action is taken by the adapter.
INV STATUS	The adapter received a Hardware Status Register from the interrupt handler which was not meaningful. The probable cause was a hardware error. Detection of this Inv Status condition causes an "adapter reset" command to be issued to the hardware.

Abbreviation	Description
LINK TEST	Posted at Command time upon receiving and decoding Link Test command. Also indicated along with Rd Msg Avail at END FLAG time (after the response has been transmitted) if valid LINK TEST has been received.
LOST DATA	This bit is set in conjunction with the RD MSG AVAL bit and indicates that a count-exceeded condition exists in an otherwise normal read completion. The address and count fields in registers 4–7 stop incrementing when the count becomes zero. This bit is mutually exclusive with the WRONG LNTH MSG bit.
MC	A nonrecoverable machine check has occurred.
NPRO/RCV OVRN	This completion is posted when either of the following occurs: 1. The read control block overflows, possibly indicating: • insufficient space was allocated to the read control block • line hung at "space" or valid data character 2. No valid (good FCS, valid address, greater than 31 bits in frame) SDLC frames have been received for a period of 20–25 seconds. Note that the IDLE timeout takes priority and resets the NPRO timeout mechanism. This completion is a warning signal. The adapter continues normal operation and continues receiving unless disabled by system code or until normal ending sequence is detected on the line.
NR SEQ ERR*	(Register 13, Bit 4) – A Command Reject condition resulted from receipt of an illegal NR sequence count in an information or supervisory frame containing good FCS. No action is taken by the system code as appropriate recovery action is taken by the adapter.
OVERRUN	One of the following conditions has been detected: Buffer Overrun or CHIO Overrun.
PMY ABRT	(Register 13, Bit 1) – A detected condition indicating abnormal termination of a message by the remote transmitting station.
POLL RCVD	The poll bit has been detected in the command field, and no Write Function Request is outstanding.
RD FBI	The storing of the last character moved from the buffer has caused the count field in the current read BCW to go to zero. This flag is set only if there is additional data in the associated frame to be stored. It is set in Normal or Disconnected mode. Note that "RD MSG AVAL" does not follow in disconnected mode.
RD MSG AVAL	1. A complete message has been received with no detectable errors and is now available for processing in the area(s) pointed to by the READ BCL. Read Initial Ptr has been invalidated by adapter code. The residual BCW data address and count are in registers 4–7 (where next byte would have been stored). 2. A valid Link Test has been received. Adapter has sent the correct response. **Note:** *Read Init Ptr NOT invalidated.*

Abbreviation	Description
RI	A Ring Indicator signal had been detected while the Open Function Request was active.
RTRY T.O.	An indication during an Open Function request that a timeout has occurred while awaiting the data set to become ready. The condition prevails until either the data set becomes ready or a halt request is received (on switched line only).
SEC BUSY	An RNR response has been sent to the primary station due to lack of receive buffers in the secondary.
SIM RCVD	Applies only when &SIMRQI is set to "YES". A valid SIM was received, the Transmit/Receive Sequence Counts resequenced, RQI mode test, unconfirmed portion of a Write dequeued, and the NSA response transmitted. The NSA response is transmitted after the status has been reported. (20 "SIMRCVDs" in succession = "CONN PROB".)
SNRM RCVD	A valid SNRM was received, and the Transmit/Receive Sequence counts resequenced. The adapter automatically sends the NSA response. System code is expected to HALT any outstanding WRITE function request (20 "SNRM RCVDs" in succession = "CONN PROB").
UNDRRUN	An underrun condition has been detected by the hardware (XMIT mode) and the adapter is attempting recovery. (Secondary Abort)
WR RTRY	The adapter is required to retransmit a previously transmitted message (I-Frame) or series of messages, in its entirety, due to lack of confirmation by sequence number from the primary station. (20 "WR RTRYs" = "CONN PROB" and both completions are posted.)
WRNG LNTH MSG	(Register 13, Bit 5) – This condition occurs only if the "Yes" option is selected for the &MAXLEN and/or &MINLEN assembly options. If the Information Frame was longer than the READ COUNT allocated for it in the BCL, this condition results (&MAXLEN=YES). Also, if the Information Frame was too short, as specified by the Minimum Message Length field in the DLCB, this condition results (&MINLEN=YES). The read buffer is reused by the adapter. No action is taken by the system code.
WRTE T.O.	A timeout condition has occurred during a write operation and indicates a potential hardware problem (e.g., xmit clock failure). This condition can also be caused by noise on the transmit clock line during transmit operation. In this situation, constant zeros are transmitted until the condition is detected in the adapter by the timeout.
XID RCVD	A valid XID was received. XID is normally received with no associated data field. If data was received, it was ignored and is not available to the IPC. The count and address fields (registers 4–7) are not meaningful. (20 "XID RCVDs" in succession = "CONN PROB".)

*Adapter recovery attempt consists of establishing a command reject state. The adapter remains in the state until a valid SNRM or DISC command** is received or until the adapter is reopened by the user.
**"SNRM, SIM or DISC" for &SIMRQI = "YES"

DPPX BSC – Device Type B

Header I

CLASS 05 SUBCLASS 01 OPTION (5) If bit 0 of Option = 1

DATE YY.DDD TIME HH/MM/SS

Header II

CLASS 05 SUBCLASS 01 OPTION (5) If bit 0 of Option = 0

DATE YY.DDD SEQ NO. (1)

Record

PA (2) SCA (3) DT (4)

CRC (7) COMPSTAT (8) ARC (9)

DATA (11) RES (12) CNT (13)

IOEP (14) ADWA (15)

CA (16) CPR (17) FRWA (18)

RES (19)

Extended Data

D01 (24,25) D02 (26,27) D03 (28)

Content

(1) SEQ NO. Sequence Number of the condition/incident log record. This is part of the header II format which is provided via DISPLAY.ERRLOG if bit 0 of the Option Mask (field 5) = 0. If bit 0 = 1, then header I is provided with a time stamp. The format of the time stamp is hour/minute/second.

With either header, a date field is provided, consisting of the year and Julian date.

Date is only valid when the customer sets the date after every IPL using the SET.DATE command. Time is only valid when the customer runs DPPX with Timer Management and sets the time after every IPL using the SET.TOD command.

(2) PA Physical Adapter Address – Byte 0 of the FRB.

(3) SCA Secondary Component Address – physical station address Bytes 26 and 27 of the FRB – N/A.

(4) DT Device Type – B (hex 40C2)

(5) OPTION Option Mask – Byte 4 of DPPX header:

Bit 0 – 1 Time Stamp (header I)
– 0 Sequence Number (header II)

Bit 1 – 1 BCLE Present

Bit 2 – 1 Extended Data Present

Bits 3–7 – 1 Specifies format for Extended Data

(7) CRC FDM Request Code – Byte 1 of the FRB in hex:

00	– Enable/Set Mode
01	– Sense – Hardware
02	– Write SOH/ETX/CONV RESP
03	– Read – Normal
04	– BID PREP
05	– Pre-Wrap Test
06	– Write SOH/ETX/NON-CONV
07	– Read – Respond RVI
08	– BID PREP – Respond NAK
09	– Wrap Data – Adapter
0A	– Write SOH/ETB/CONV RESP
0C	– Write BID
0D	– Wrap Data-DCE
0E	– Write SOH/ETB/NON-CONV
10	– Write EOT
12	– Write STX/ETX/CONV RESP
14	– Disable
16	– Write STX/ETX/NON-CONV
18	– Write WACK
1A	– Write STX/ETB/CONV RESP
1C	– Write Bell
1E	– Write STX/ETB/NON-CONV
20	– Write TTD
24	– Write Poll
28	– Write Selection
2C	– Write Station ID – ENQ
30	– Write Station ID – NAK
34	– Write Station ID – ACK0
38	– Read Station ID
3C	– Write DISC
40	– ADPREP
44	– ADPREP – Respond EOT
46	– Write SOH/ETX/EXPECT CONV RESP
48	– ADPREP – Respond RVI
50	– ADPREP – Respond NAK
56	– Write STX/ETX/EXPECT CONV RESP
58	– ADPREP – Respond WACK

(8) COMPSTAT Completion Status – Byte 2 of FRB

and

(9) ARC Adapter Status – Byte 3 of FRB

COMPSTAT = hex XC

Complete with Error	**ARC**
Underrun/overrun	Register 3, bit 2
Inv BSTAT	Register 3, bit 3
DCE	Register 3, bit 4
MC	Register 3, bit 5
T.O.	Register 3, bit 6
Bad Data	Register 3, bit 7

COMPSTAT = hex XA

Complete with Exception	**ARC**
N T.O./INV	Register 3, bit 1
N NAKS RCVD	Register 3, bit 5
N Wrong ACKS	Register 3, bit 6
Count Exceeded	Register 3, bit 4

For further bit descriptions, see "Abbreviation Descriptions" at the end of this device type.

(11)	DATA	Bytes 4–7 of the FRB. Volume and Data Address.
(12)	RES	Reserved – Bytes 8 and 9 of the FRB – N/A.
(13)	CNT	Count – Bytes 10 and 11 of the FRB.
(14)	IOEP	I/O Interrupt Entry Point – Bytes 12–15 of the FRB – N/A.
(15)	ADWA	Adapter Work Area Address – Bytes 16–19 of the FRB – N/A.
(16)	CA	Channel Address – Byte 24 of the FRB – N/A.
(17)	CPR	Channel Pointer Register – Byte 25 of the FRB – N/A.
(18)	FRWA	Function Request Work Area Address – Bytes 20–23 of the FRB – N/A.
(19)	RES	Reserved – Bytes 28–31 of the FRB – N/A.

***Note:** Fields (24) through (28) contain Sense Data and are valid only when COMPSTAT (field 8) = hex XC (complete with error) for the following conditions reported by ARC (field 9): Underrun, DCE, T.O., and Bad Data.*

(24) Byte 0 of Sense Data.

BSTAT has the following meaning:

- Bit 0 — Input Request
- Bit 1 — Output Request
- Bit 2 — DCE Interrupt
- Bit 3 — Timer Interrupt
- Bit 4 — Exception
- Bit 5 — MC/PC
- Bit 6 — Enable/Disable
- Bit 7 — Interrupt Request

(25) Byte 1 of Sense Data.

MSTAT has the following meaning:

- Bit 0 — Data Set Ready
- Bit 1 — Clear to Send
- Bit 2 — RLSD
- Bit 3 — Ring Indicator
- Bit 4 — DSR Transition
- Bit 5 — Reserved
- Bit 6 — RLSD Transition
- Bit 7 — CTS Transition

(26) Byte 2 of Sense Data.

MCTRL has the following meaning:

- Bit 0 — Data Terminal Ready/Connect Data Set to Line
- Bit 1 — Request to Send
- Bit 2 — Wrap
- Bit 3 — Test
- Bit 4 — Select Standby
- Bit 5 — Select Half Speed
- Bit 6 — New Synch
- Bit 7 — DCE Interrupt Disable

(27) Byte 3 of Sense Data.

ASTAT has the following meaning:

- Bit 0 — Overrun
- Bit 1 — Underrun
- Bit 2 — Receive Clock Running (N/A)
- Bit 3 — SDLC Invalid Sequence (N/A)
- Bit 4 — SDLC Frame (N/A)
- Bit 5 — Invalid Character (N/A)
- Bit 6 — Break Byte Detected (N/A)
- Bit 7 — Adapter in Sync

(28) Byte 4 of Sense Data.

ACTRL has the following meaning:

- Bit 0 — Receive Mode
- Bit 1 — Transmit Mode
- Bit 2 — Inhibit Zero Inspection
- Bits 3,4 — 00 Mode Select — Auto
  - — 01 Mode Select — EBCDIC
  - — 10 Mode Select — ASCII
  - — 11 Mode Select — SDLC (N/A)
- Bits 5,6 — 00 Code Length — 8-bit
  - — 01 Code Length — 6-bit
  - — 10 Code Length — 7-bit
  - — 11 Code Length — 5-bit
- Bit 7 — NRZI

Abbreviation Descriptions

Abbreviation	Description
BAD DATA	An ETB, FTX, DLE, or ENQ character was contained as data in the output buffer for a nontransparent write. An ENQ was transmitted in place of the bad data character (STX-TEXT-ENQ=FORWARD ABORT) and, upon receipt of a response, the FR was terminated.
BELL RCVD	A BELL character has been received.
COUNT EXCEED	A block of data has been received that exceeds the buffer area allocated for it.
DCE	An error condition by the data communications equipment; e.g., DSR may not have risen or fallen within its allotted time or an unexpected modem interrupt occurred; i.e., DSR may have glitched or fallen. **Note:** *If, during the course of normal operation, noise glitches similar to those experienced during EMC testing occur, the adapter ignores these short duration glitches and proceeds as normal. If, however, the glitches are long enough so that the condition of the interface line is found to be at the wrong state at the time the adapter examines it, a DCE error is posted.*
DISC	A disconnect sequence (DLE EOT) has been received.
ENQ RCVD	The ENQ character was received as a response.
EOH ATTN	An STX character has been received signifying the end of header.
EOT RCVD	An EOT character was received from the master instead of a block, a message, or a line bid.
ETX = 0 ETB = 1	A 1 in this bit position indicates that the block just read in ended with an ETR. A 0 indicates that the message ended with an ETX.
HALTED	A haltable function request has been halted at the request of the IPC.
(ID) ENQ RCVD	An ENQ been received in response to a Write Station ID-NAK from the station whose ID is stored in the designated ID Store area.
(ID) NAK RCVD	A NAK has been received in response to a Write Station ID-ENQ from the station whose ID is stored in the designated ID Store area.
INV BSTAT	The adapter received a BSTAT from the interrupt handler which was not meaningful. The probable cause was a hardware error; e.g., during a read operation when the transmit latch is reset, BSTAT indicates an output request interrupt. An adapter reset command is issued to the hardware after the INV BSTAT condition.
ITB ATTN	An ITB character has been received.
MC	A nonrecoverable machine check has occurred.
NAK RCVD	The NAK sequence was received as a response.
N ENQS RCVD	This bit is set each time after N (3 or 15) ENQs have been received. After each ENQ, the previous acknowledgment is retransmitted to the master. This action may signify that the ACK counters of master and slave are out of sync, and may continue indefinitely until the master aborts.
N NAKS RCVD	N (3 or 15) NAKs were received. The message block was retransmitted after each NAK until N was reached.
N TO/INV	N (3 or 15) 3-second timeouts have occurred without a valid start character, without the required SYN SYN characters being received (for Read), or a valid response being received.
N WACKS RCVD	N (3 or 15) WACKs were received instead of ACK0 or ACK1.
N WRONG ACKS	N (3 or 15) ACK0s were received instead of ACK1s, or vice-versa.
ONE TO/INV	In Write Bid, Write Select, and Write Station ID-ENQ, three seconds have elapsed without a valid response received. In ADPREP, three seconds have elapsed without the adapter achieving character sync.
RESP RCVD	A NAK has been received in response to TTD, or an ENQ has been received in response to WACK.
RI	A Ring Indicator signal has been detected during the Open Function request.
RVI RCVD	The Reverse Interrupt sequence was received instead of ACK0 or ACK1.
STX = 0 SOH = 1	A 1 in this bit position indicates that the message just read in contains header information. A 0 indicates that it is all text.
T. O.	A timeout condition has occurred. The cause depends upon whether a Write or Read operation was in progress at that time, as indicated by bit 0 (WR = 0, RD = 1). Write – one second has elapsed without an output request from the hardware, asking for the next output byte. (The T. O. is 10 seconds for the initial output request after a line turnaround.) Read – Three seconds have elapsed since achieving character sync without receiving a valid control character.
T.O. ON INITIAL POLL	No response was received from the polled station within 3 seconds.
T.O. (SWITCHED)	An indication during the Enable/Set Mode function request that a timeout has occurred while awaiting DCE to become ready; i.e., waiting for the switched communications line to be established.
TTD RCVD	A TTD sequence has been received instead of data.
UNDER/OVERRUN	An exception interrupt occurred. The probable cause depends upon whether a Write or a Read operation was in progress at that time, as indicated by bit 0 (WR = 0, RD = 1). When bit 0 = 0, the probable cause was an underrun condition; when bit 0 = 1, the probable cause was a hardware overrun condition.

Abbreviation	Description
UNDERRUN	An exception interrupt occurred. The probable cause is that bit 1 of ASTAT (underrun) was on because the next data byte was not ready when the hardware required it.
WACK RCVD	The WACK sequence was received as a response.
WR = 0 RD = 1	A 1 in this bit position indicates that the program flags pertain to actions that occurred during a read portion of the function request; a 0 indicates a write portion.
XPRNCY	The receive operation has entered transparent mode.
1#	The Write Expect Conversational Response FR has entered the conversational portion, and the other program flags relate to the read operation.
1 = POLL 0 = SELECT	When this bit is a 1, it indicates that this station has just been polled; when a 0, this station has just been selected.

DPPX Start/Stop, 2741 — Device Type C

Header I

CLASS 05 SUBCLASS 01 OPTION (5) If bit 0 of Option = 1

DATE YY.DDD TIME HH/MM/SS

Header II

CLASS 05 SUBCLASS 01 OPTION (5) If bit 0 of Option = 0

DATE YY.DDD SEQ NO. (1)

Record

PA (2) SCA (3) DT (4)

CRC (7) COMPSTAT (8) ARC (9)

DATA (11) RES (12) CNT (13)

IOEP (14) ADWA (15)

CA (16) CPR (17) FRWA (18)

RES (19)

Content

(1) SEQ NO. Sequence Number of the condition/incident log record. This is part of the header II format which is provided via DISPLAY.ERRLOG of bit 0 of the Option Mask (field 5) = 0. If bit 0 = 1, then header I is provided with a time stamp. The format of the time stamp is hour/minute/second.

With either header, a date field is provided, consisting of the year and Julian date.

Date is only valid when the customer sets the date after every IPL using the SET.DATE command. Time is only valid when the customer runs DPPX with Timer Management and sets the time after every IPL using the SET.TOD command.

(2) PA Physical Adapter Address — Byte 0 of the FRB.

(3) SCA Secondary Component Address — Bytes 26 and 27 of the FRB — N/A.

(4) DT Device Type — C (hex 40C3)

(5) OPTION Option Mask — Byte 4 of DPPX header:

- Bit 0 — 1 Time Stamp (header I)
  — 0 Sequence Number (header II)
- Bit 1 — 1 BCLE Present
- Bit 2 — 1 Extended Data Present
- Bits 3–7— 1 Specifies Format for Extended Data

(7) CRC FDM Request Code — Byte 1 of the FRB in hex:

- 01 — Sense
- 05 — Prewrap Test
- 09 — Wrap — Adapter Test
- 0D — Wrap — DCE Test
- 30 — Close
- 40 — Open
- 42 — Write Block
- 43 — Receive Block
- 46 — Write Multiple
- 4A — Write Last

(8) COMPSTAT Completion Status — Byte 2 of the FRB.

Bits 0–3— Don't care

Bits 4–7 have the following meaning:

- Bit 4 — Complete
- Bit 5 — Error
- Bit 6 — Exception
- Bit 7 — Not Used

(9) ARC Adapter Status — Byte 3 of the FRB.

When COMPSTAT (8) has bit 5 (Error) = 1, ARC =

- Bit 0 — Data Error
  - Write FR's — the output buffer or register contained an EOT character.
  - Receive Block — the received data has a parity error — a hypen has been stored in the buffer.
- Bit 1 — DCE Error — an abnormal condition occurred on the DCE interface; e.g., an expected condition did not occur within its allotted time.
- Bit 2 — Communications Line at Space — caused either by a fault on the line or an abnormally long break signal received.
- Bit 3 — Overflow — Data received after buffer has been filled.
- Bit 4 — Unused.

Bit 5 — MC Error — a nonrecoverable machine check has occurred.

Bit 6 — Timeout — data has not been received for 25 seconds.

Bit 7 — Overrun — a data byte has been received by the hardware before the adapter accepted the previous byte. The previous byte is lost.

When COMPSTAT (8) has bit 6 (Exception) = 1, ARC =

Bit 0 — Function Request was halted because halt bit was set in R1.

Bit 1 — EOT received during receive block FR prior to entering data mode — STX and possibly data have been lost.

Bit 2 — Break Signal Detected — the 2741 wishes to terminate the adapter transmission.

Bit 3 — Unused.

Bit 4 — Unused.

Bit 5 — Security Detection — a Write type or Receive block FR was issued after the data set ready lead had been detected to glitch.

Bit 6 — Unused.

Bit 7 — Unused.

(11)	DATA	Bytes 4–7 of the FRB.
(12)	RES	Reserved — Bytes 8 and 9 of the FRB — N/A.
(13)	CNT	Count — Bytes 10 and 11 of the FRB.
(14)	IOEP	I/O Interrupt Entry Point — Bytes 12–15 of the FRB.
(15)	ADWA	Adapter Work Area Address — Bytes 16–19 of the FRB — N/A.
(16)	CA	Channel Address — Byte 24 of the FRB — N/A.
(17)	CPR	Channel Pointer Register — Byte 25 of the FRB — N/A.
(18)	FRWA	Function Request Work Area Address — Bytes 20–23 of the FRB — N/A.
(19)	RES	Reserved — Bytes 28–31 of the FRB — N/A.

DPPX Start/Stop, TTY — Device Type Y

Header I

CLASS 05 SUBCLASS 01 OPTION (5) If bit 0 of Option = 1

DATE YY.DDD TIME HH/MM/SS

Header II

CLASS 05 SUBCLASS 01 OPTION (5) If bit 0 of Option = 0

DATE YY.DDD SEQ NO. (1)

Record

PA (2) SCA (3) DT (4)

CRC (7) COMPSTAT (8) ARC (9)

DATA (11) RES (12) CNT (13)

IOEP (14) ADWA (15)

CA (16) CPR (17) FRWA (18)

RES (19)

Content

(1) SEQ NO. Sequence Number of the condition/incident log record. This is part of the header II format which is provided via DISPLAY.ERRLOG if bit 0 of the Option Mask (field 5) = 0. If bit 0 = 1, then header I is provided with a time stamp. The format of the time stamp is hour/minute/second.

With either header, a date field is provided, consisting of the year and Julian date.

Date is only valid when the customer sets the date after every IPL using the SET.DATE command. Time is only valid when the customer runs DPPX with Timer Management and sets the time after every IPL using the SET.TOD command.

(2) PA Physical Adapter Address — Byte 0 of the FRB.

(3) SCA Secondary Component Address — Bytes 26 and 27 of the FRB — N/A.

(4) DT Device Type — Y (hex 40E8)

(5) OPTION Option Mask — Byte 4 of DPPX header:

Bit 0 — 1 Time Date Stamp (header I)
— 0 Sequence Number (header II)

Bit 1 — 1 BCLE Present

Bit 2 — 1 Extended Data Present

Bits 3–7 — 1 Specifies Format for Extended Data

(7) CRC FDM Request Code — Byte 1 of the FRB in hex:

00 — Wrap — DCE Test

01 — Sense Adapter Status

05 — Prewrap Test

09 — Wrap — Adapter Test

30 — Close

40 — Open

42 — Write Block

43 — Read Block

46 — Write Multiple

4A — Write Last

C0 — Halt Open

C3 — Halt Read Block

(8) COMPSTAT Completion Status — Byte 2 of the FRB.

Bits 0–3 — Don't care

Bits 4–7 have the following meaning:

Bit 4 — Complete

Bit 5 — Error

Bit 6 — Exception

Bit 7 — Not used

(9) ARC — Adapter status – Byte 3 of the FRB.

When COMPSTAT (8) has bit 5 (Error) = 1, ARC =

Hex Value	Description
(80) DATA ERROR	Read Block. A parity error has occurred on received data. Byte is tested for even parity. The error byte is replaced by a hyphen character and stored in the receive buffer.
(40) DCE ERROR	Open, Close, Read Block, Writes. This flag is set when an abnormal condition occurs on the data set/DCE interface; e.g., an expected condition did not occur within its allotted time or a DCE interface lead has an unexpected change of state. If condition remains after "N" retries, Close and Reopen the line.
(20) LINE AT SPACE	Read Block, Writes. The receive data line is at a spacing condition caused by either a faulty line or an abnormally long spacing condition. If condition remains after "N" retries, Close and Reopen line.
(10) OVERFLOW	Read Block. At least one data byte was received after code has decremented the Read Count, registers 6 and 7, to zero. Code monitors for the turnaround sequence from the terminal while flushing subsequent data. OVERFLOW is reported to system code only when the turnaround sequence is detected by code. If the turnaround is missed, this FR is terminated by a Text Timeout error status.
(08) EOT RCVD	Read Block and Writes. A disconnect character (EOT) has been received by code. System code should follow this with a Close FR.
(04) MCPC	All FRs. An I/O machine check has occurred for this adapter. A Close and Open sequence resets the adapter and the I/O machine check. Code has no retry for I/O machine checks.
(02) TEXT TIMEOUT	Read Block. During the Read Block FR, no incoming characters have been received for 25 seconds. Reissue the Read Block and, if the timeout occurs "N" times, Close and Reopen the line.
(01) OVERRUN	Read Block. A data byte has been received by the adapter hardware before the code serviced the previous byte, or code has received more than one data byte before a Read FR is issued. The previous byte(s) are lost. Subsequent data is flushed. OVERRUN is reported only after the trunaround sequence is detected by code. If the turnaround is missed by code, this FR is terminated by a TEXT TIMEOUT error status.
Other Values	Don't care.

When COMPSTAT (8) has bit 6 (Exception) = 1, ARC =

Hex Value	Description
(80) HALTED	Open, Read Block. The FR was halted because the halt bit was set in register 1 and the FR issued by system code.
(20) BREAK DETECTED	Writes. The Model 33/35 type terminal has generated a break signal to interrupt the adapter transmission. The system code may honor the receipt of the break by issuing a Write FR which causes code to transmit the turnaround sequence. Or, system code may first reissue the Write which was terminated by the break to finish writing the current message.
(04) SECURITY	Read Block, Writes (on switched lines only). DSR lead of the DCE interface has glitched, but is still on. If the condition exists after "N" retries of reissuing the FR without altering registers 4 and 5 and 6 and 7, a Close and Reopen should be issued.
Other Values	Don't care.

(11)	DATA	Bytes 4–7 of the FRB.
(12)	RES	Reserved – Bytes 8 and 9 of the FRB – N/A.
(13)	CNT	Count – Bytes 10 and 11 of the FRB.
(14)	IOEP	I/O Interrupt Entry Point – Bytes 12–15 of the FRB.
(15)	ADWA	Adapter Work Area Address – Bytes 16–19 of the FRB – N/A.
(16)	CA	Channel Address – Byte 24 of the FRB – N/A.
(17)	CPR	Channel Pointer Register – Byte 25 of the FRB – N/A.
(18)	FRWA	Function Request Work Area Address – Bytes 20–23 of the FRB – N/A.
(19)	RES	Reserved – Bytes 28–31 of the FRB – N/A.

CA332 DPCX Condition/Incident Records

All communications attachment feature (hardware) problems are recorded/reported by DPCX using three record types:

- Type-2 Record — I/O Machine Check problems.
- Type-3 Record — Hardware problems and performance counter data.
- Type-4 Record — System (CA) problems.

Type-2 Error Incident Record

The CA feature uses the type-2 error incident record to indicate CA I/O machine check errors. The CA type-2 record has the same format and field description as the general type-2 record described in Chapter 2, CP830, "DPCX Error Log Utility (SYSLERR) and How to Use It."

Format for Type-2 Record

```
(1)              (2)        (3)    (4)    (5)
2-TYPE  I-REC    SEQ-XXXX   NA-XX  PA-XX  LA-XX
                                   (6)
        D21-XXXX XXXX       LVL-XX C-FR-XX
                            (7)    (8)
        D22-XXXX XXXX       MC-XX  S-FR-XX
        D23-XXXX            D24-XXXX      D25-XXXX
```

Description

(1)	2-TYPE I-REC	— Type-2 incident record.
(2)	SEQ	— Decimal sequence number of the record.
(3)	NA	— Number of functions and programs which were active at the time of failure.
(4)	PA	— Physical address for which the recording was made.
(5)	LA	— Logical address for which the recording was made.
(6)	C-FR	— Control card function request active at the time of failure.
(7)	MC	— Type of machine check that occurred. • Bits 0 and 1 indicate control card failure. • Bits 2 and 3 indicate unit controller logic or control storage failure.
(8)	S-FR	— System function request active at the time of failure.

Type-3 Variable Data Incident Record

The CA feature uses a type-3 variable data incident record to indicate hardware errors, sense and status information, and performance counters.

Format for Type-3 Record

```
(1)                 (2)         (3)
3-TYPE  I-REC       SEQ-XXXX    LA-XX
(4)     (5)     (6)     (7)
D1-XX   D2-XX   D3-XX   D4-XX
(8)     (9)     (10)    (11)    (12)
D5-XX   D6-XX   D7-XX   D8-XX   D9-XX
(13)                    (14)
D10-XXXX                D11-XXXX
(15)                    (16)
D12-XXXX                D13-XXXX
(17)                    (18)
D14-XXXX                D15-XXXX
```

Description

(1)	TYPE	— Type-3 incident (I) record.
(2)	SEQ	— Decimal sequence number of the record.
(3)	LA	— Logical addresses (PA) of the CA adapters.
(4)	D1	— System operation at the time of the error; any hex value = don't care.
(5)	D2	— Adapter operation at time of the error.

SDLC Secondary:

Hex Value	Name	Description
00	Open	Initializes adapter, sets up control blocks and parameters, and initiates receive function.
01	Sense	Senses status of adapter hardware and software.
02	Write	Transmits data to primary station; upon completion, reenters receive mode.
04	Close	Terminates communication with DCE and inhibits adapter from receiving or monitoring any transmission; disables adapter from generating interrupt requests to processor.

SDLC Primary:

Hex Value	Name	Description
00	Open	Initializes adapter, sets up control blocks and parameters; performs wire test if local loop.
01	Sense	Reads and stores status registers (hardware).
04	Close	Terminates all adapter activity, resets DCE control lines, and issues adapter reset.
06	Initialize Secondary Station	Reserves fields in SDLCBs to be initialized as required.
08	Take Group List	Defines location of first group control block of group control list; establishes certain group-related fields.
0A	Read-Write Turnaround	Provides method of recovery when a nonproductive receive timeout condition exists; terminates receive state and proceeds with a normal read-to-write turnaround.
40	Activate Link	Forces entry to operational mode; starts polling or writing according to control lists.

(6) D3 – Completion code in hex:

- 01 – Data Transfer Status
- 02 – Exception Status
- 04 – Recoverable Channel I/O Error
- 08 – Function Request Status
- 0C – Unrecoverable Error Status

(7) D4 – Indicates station or device address.

(8) D5 – Value of the machine check. Valid only when bit 5 of D6 field = 1.

(9) D6 – Status flags.

(10) D7 – Status extension flags.

(11) D8 – Set to zero.

(12) D9 – Reserved (Field = 0).

(13,14) D10,D11 – Error, sense, and status data.

(15) D12 – Error, sense, and status data, or good inbound performance counter (decimal).

(16) D13 – Error, sense, and status data, or bad inbound performance counter (decimal).

(17) D14 – Good outbound performance counter (decimal).

(18) D15 – Bad outbound performance counter (decimal).

Type-3. Record Completion Status Fields: D3, D6, and D7

The following table shows possible completion for system operation. (This table is a summarization only; see D6 and D7 tables that follow for details.) Completions other than shown in the table may indicate problems in DPCX error reporting.

D2 System Operation	D3	D6	D7
00	08	40	–
	08	02	–
	0C	20	–
	0C	04	–
	0C	02	–
	0C	01	–
	02	40 or C0	10
	02	20 or 0A	01
01, 04	08	40	–
	0C	04	–
06, 08, 0A	08	40	–
40	See following tables.		

Type-3 Record D6 Status Flags for D3 = Hex 01

D6 Bit	Name	Description
0	Return Request Interlock	This code allows the 8100 to return status information while processing. No pending I/O interrupt is needed.
1*	Write Message Confirmed	A single write message was transmitted and confirmed.
2*	Write List Complete	The last message of a write request was transmitted and received.
3*	0	–
4*	Read Flag Buffer Indication	Notification that BCW (Buffer Control Word) count equals zero.
5*	Read Message Available	An information field was received without errors. It is now available for processing.
6*	0 Data 'I' Frame Received	A valid 'I' frame was received but contained no data.
7*	Read Message Available; truncated data	An information field was received. Data was truncated for insufficient read buffer area.

*Return Request Interlock is also set.

Type-3 Record D6 Status Flags for D3 = Hex 02

D6 Bit	Name	Description
0	Return Request Interlock	This code allows the processor to return status information while processing. No pending I/O interrupt is requested.
1*	Status Extension 1	
2*	Status Extention 2	
3*	Status Extention 3	
4*	Status Extention 4	See D7, Status Extension Flags.
5*	Status Extention 5	
6*	Status Extention 6	
7*	Status Extention 7	

*Return Request Interlock is also set.

Type-3 Record D6 Status Flags for D3 = Hex 04

D6 Bit	Name	Description
0	Return Request Interlock	This code allows 8100 to return status information. No pending I/O interrupt needed.
1	CHIO Overrun	CHIO mechanism locked out more than one character time when in process of receiving data.
2	Alternate Buffer Overrun	8100 hardware has filled static alternate buffers faster than 8100 can service their contents.
3	Receive Control Overrun	CHIO mechanism tried to store control information beyond control buffer's capacity.
4	0	–
5*	CHIO Underrun	CHIO mechanism was not serviced within one character time during a transmit operation.
6	0	–
7	0	–

*Return Request Interlock is also set.

Type-3 Record D6 Status Flags for D3 = Hex 08

D6 Bit	Name	Description
0	Return Request Interlock	This code allows the 8100 to return status information while processing. No I/O interrupt is pending.
1*	Normal Function Return Complete	The outstanding function request has been successfully completed.
2	0	–
3	0	–
4	Link Quiesced	The adapter has entered the quiesced state.
5	RLSD Error	A carrier failure has been detected.
6	Loop Wire Test Failed	A loop wire error was detected during the open function request.
7	Invalid Function Request	The adapter has been issued an undefined function request.

*Return Request Interlock is also set.

Type-3 Record D6 Status Flags for D3 = Hex 0C

D6 Bit	Name	Description
0	0	–
1	0	–
2	DCE DSR Error	A DCE interrupt or other unexpected DCE condition has occurred (for example, DSR dropped when it should be on).
3	0	–
4	0	–
5	Machine Check	A nonrecoverable machine check has occurred.
6	Write Failure	No characters were transmitted during a timeout interval (approximately 8.2 seconds) while in transmit mode. Probable cause is a clock failure.
7	Invalid Hardware Status	Adapter basic status was not meaningful. The probable cause was a hardware error.

Type-3 Record D7 Status Extension 1 for D6 = Hex 40 or C0

D7 Bit	Name	Description
0	Return Request Interlock	This code allows the 8100 to return status information while processing. No I/O interrupt is pending.
1	'N' Group Timeouts	'N' poll retries to the control units resulted in 'N' timeout retries. No response was received, including ORP.
2	Nonproductive RCV Timeout	Receive line was active for 25 or more poll timeout seconds. No intervening flags were encountered.
3	Control Unit Timeout	A 3-second timeout has occurred during an open function while waiting for the DCE and DSR to become ready.
4	0	–
5	0	–
6*	Control Unit On-Line	An ORP was received from a control unit or an NSA from a device in response to an SNRM, which was formerly offline.
7	Not used	–

*Return Request Interlock is also set.

Type-3 Record D7 Status Extension 2 for D6 = Hex 20 or A0

D7 Bit	Name	Description
0	Return Request Interlock	This code allows the 8100 to return status information while processing. No I/O interrupt is pending.
1*	FCS Error	An SDLC frame was received. The CRC check failed.
2*	Invalid Address	A valid SDLC frame was received with an invalid address character. See bit 4 below.
3*	Invalid Sequence Error	An SDLC frame was terminated by the 8100. Invalid sequence (seven 1's) on the line. Handled as FCS error.
4*	Invalid Address Reason Code	Bit 4 = 0 – No-op flag set in SDLCB referenced by Receive Link Address. Bit 4 = 1 – Receive Link Address not included in range of the mask. No SDLCB pointer exists for the control unit.
5	0	–
6	0	–
7	CTS Fell	DCE clear-to-send fell, or glitched, when the 8100 was in a transmit and request-to-send was on.

*Return Request Interlock is also set.

Type-3 Record D7 Status Extension 3 for D6 = Hex 10 or 90

D7 Bit	Name	Description
0	Return Request Interlock	This code allows the processor to return status information while processing. No pending I/O interrupt is requested.
1*	Disconnect Acknowledged	An NSA to DISC command was received. The SDLCB fields for this control unit are not cleared or reset.
2*	SNRM Acknowledged	An NSA was received from a control unit in response to a 8100 SNRM command.
3*	ROL Received	The control unit is in an asynchronous or normal disconnect mode. A change of mode is required before it can respond to the 8100 command.
4*	Command Reject Received	The control unit rejected a previous command from the 8100.
5*	Unexpected or Duplicate Non-sequenced Response	The status is due to one of the following Mode Command conditions: 1. Two or more responses to a Set Mode command. 2. Asynchronous (unsolicited) receipt of NSA link set.
6*	SIM Acknowledged	An NSA was received from a control unit in response to a 8100 Set Initialization Mode command.
7*	RQI	The control unit is in Request Initialization mode.

*Return Request Interlock is also set.

Type-3 Record D7 Status Extension 4 for D6 = Hex 08 or 88

D7 Bit	Name	Description
0	Return Request Interlock	This code allows the processor to return status information while processing. No pending I/O interrupt is requested.
1	Primary Busy	A Request Not Ready command was sent to the control unit.
2*	'N' Contact Poll Retries	'N' retry attempts were made to contact poll the control unit (SNRM, DISC, or SIM) without a poll acknowledgment.
3	'N' write retries	'N' Retry attempts were made to send a message (I-Frame) to the control unit without proper acknowledgment.
4*	Lost Data	The data contents of a valid I-Frame were lost: 1. No REC buffer available to the 8100 at that time. 2. The allocated Read buffer was exhausted.
5*	Too Short I-Frame Received	A valid I-Frame was received. It was shorter than the minimum acceptable length parameter in SDCLB.
6*	'N' NS Errors	A control unit had invalid NS sequence counts when sending an information frame.
7*	No REC Buffer	Set in conjunction with Lost Data (bit 4). No REC buffer available to the 8100 at that time.

*Return Request Interlock is also set.

Type-3 Record D7 Status Extension 5 for D6 = Hex 04 or 84

D7 Bit	Name	Description
0	Rerun Request Interlock	This code allows the processor to return status information while processing. No I/O interrupt is requested pending.
1*	Control Unit Moved	A valid SDLC frame was received from a control unit that was physically moved from one address to another or from one 8100 communications adapter to another.
2	0	–
3	0	–
4*	Nr Sequence Error	Information or Supervisor frame has good FCS but the Nr Sequence is out of range.
5	0	–
6*	Data With Response	The 8100 does not recognize a control unit response or the associated data field.
7*	Invalid Response Received	The 8100 received a frame with good FCS, but does not recognize the command byte.

*Return Request Interlock is also set.

Type-3 Record D7 Status Extension 6 for D6 = Hex 02 or 82

D7 Bit	Name	Description
0	0	–
1*	Beacon Received	A beacon response was received from a control unit.
2	0	–
3	0	–
4	0	–
5	0	–
6	0	–
7	0	–

*Return Request Interlock is also set.

Type-3 Record D7 Status Extension 7 for D6 = Hex 01 or 81

D7 Bit	Name	Description
0	Return Request Interlock	This code allows the processor to return status information while processing. No pending I/O interrupt is requested.
1*	"N" Supervisory Retries	"N" supervisory frames have been transmitted to the station with no proper acknowledgment.
2*	0	–
3*	0	–
4	0	–
5	0	–
6	0	–
7	0	–

*Return Request Interlock is also set.

Type-3 Record D10 Error, Sense, and Status Data

Bit	Name	Description
BSTAT (Byte 0 Basic Status Adapter		
0	CHIO Halt	Halt occurred during Channel I/O Operation.
1	Xmit EOL	Transmit Control List End was reached.
2	RCV Ctrl Entry	Entry was made in receive control block.
3	Modem/Timer	Modem or timer interrupt occurred.
4	Exception	Exception condition.
5	MC	System Check.
6	Enabled	Adapter interrupt; Enabled (on)/Disabled (off).
7	Intrpt Request	Interrupt request condition.
RCTRL (byte 1, Receive Control)		
0	Rcv Mode	Receive Mode.
1	Buffer 1 Valid	Use Buffer 1.
2	Buffer 2 Valid	Use Buffer 2.
3	Reserved	
4	Specific Addr Valid	Specific address is valid.
5	Group Address Valid	Group address is valid.
6	Intrpt Cont Flags	Interrupt on continuous flags.
7	Enable 15 1's	Enables 15 1's detect logic, inhibits invalid sequence detection.

Type-3 Record D11 Error, Sense, and Status Data

Bit	Name	Description
RSTAT (byte 2 Rec Data Path Status)		
0	Inv Seq/Addr	Detected invalid sequence or address.
1	Byte Overrun	Byte overrun occurred.
2	Rcv Ctrl Entry	Attempt entry in Receive Control Block.
3	15 Ones	Detected 15 contiguous 1's online.
4	Ctrl Overrun	Exceeded Receive CHIO Control buffer.
5	(FCS Good)/Traffic	Detected flag character on receive line.
6	Rcv CHIO Halt	Halt occurred during Receive CHIO operation.
7	Adapter in Sync	Detected Flag and Receive Mode Set.
TCTRL (byte 3, Xmit Control)		
0	Xmit Mode	Transmit mode; enables RTS.
1	Ctrl Valid	Transmit control list is valid.
2	NRZI	NRZI Data.
3	Load Serializer	Transmit data byte loaded into serializer.
4	Flag	Controls flag insertion into transmit data stream.
5	Cont Char	Continuous characters repeatedly transmitted.
6	FCS Seq + Flag	Transmit two FCS characters and flag.
7	Inhbt Zero Insert	Inhibit zero insertion.

Type-3 Record D12 Error, Sense, and Status Data

Bit	Name	Description
TSTAT (byte 4, Xmit Data Path Status)		
0	Reserved	
1	Reserved	
2	Reserved	
3	Reserved	
4	Reserved	
5	TTOIR	Transmit turn off buffer sent.
6	Xmit CHIO Halt	Transmit CHIO halt.
7	Byte Underrun	Second byte requested before first byte sent.
MCTRL (byte 5, DCE Control)		
0	Data Term Rdy	Data Terminal Ready (1 = logical on.)
1	Req to Send	Request to Send (1 = logical on).
2	Select Standby	Select Standby (1 = logical on).
3	Data Rate Select	Data Rate Select (1 = logical off).
4	Local Test	Local Test (1 = logical on).
5	Disable Ring	Inhibit Ring Indicate transitions from causing interrupt requests.
6	Disable Carrier Det	Inhibit Carrier Detect transitions from causing interrupt requests.
7	Disable Xmit Clear to Send	Inhibit Clear to Send transitions detection.

Type-3 Record D13 Error, Sense, and Status Data

Bit	Name	Description
MSTAT (DCE-Adapter Control line Status)		
0	Timer 1 (Fine)	Interval Timer 1 completed time measurement.
1	Timer 2 (Coarse)	Interval Timer 2 completed time measurement.
2	Data Set Rdy	Data Set Ready (1 = logical on).
3	Clear to Send	Clear to Send (1 = logical on).
4	DSR Trans	Data Set Ready changed state.
5	Ring Trans	Ring Indicate changed state.
6	Carrier Det Trans	Carrier Detect changed state.
7	Clear to Send Trans	Clear to Send changed state.
DCTRL (byte 7, Diag Control)		
0	Wrap	Wraps interface lines on logic side of EIA converters.
1	T3/T4 Test	Tests under diagnostic control.
2	New Sync	New Sync.
3	TX New Sync	Control New Sync line is Transmit mode.
4	Diag Clk	Diagnostic Clock.
5	Diag Timer Ctrl	Control timers 1 and 2.
6	Carrier Det	Carrier Detect.
7	Ring	Ring Indicate.

Type-4 System Incident Record

The CA feature uses the type-4 system incident record (SYS-COND-20) to indicate a majority of hardware errors. The format for the type-4 records is:

(1)	(2)	(26)
4 TYPE I-REC	SEQ-XXXX	SYS-COND-20

(27)	(28)	(29)	(30)	(31)
D01-XX	D02-XX	D03-XX	D04-XX	D05-XX

(1) 4 TYPE I-REC = Type-4 incident (I) record.
(2) SEQ = Decimal sequence number of the record.
(26) SYS-COND = The incident was CA - related (System Condition 20).
(27) D01 = Adapter operation.
(28) D02 = Completion code.
(29) D03 = Status flags.
(30) D04 = Extended status.
(31) D05 = Reserved.

	D01 Adapter Operation (Hex)	D02 Completion Code (Hex)	D03 Status Flags 0	1	2	3	4	5	6	7	D04* Extended Status (Hex)
Write Complete	02	X8	X	X	X	X	X	X	X	X	XX
Read Intermediate Completion	01	X1	XID Rcvd	Link Test	NPRO/ Rcv Ovrn	Lost Data	Sec Busy	Rd FBI	Rd Msg Aval	Poll Rcvd	
Write Complete and Read Intermediate Completion	02 01	X9	0	0	0	Lost Data	0	0	Rd Msg Aval	0	
Read/Write Exception	01 02	X2	SNRM Rcvd	Disc Rcvd	Write Retry	Idle Timeout	Over run	Under run	Conn Problem	Dump Msg	
Write — Halted	02	XA	X	X	X	X	X	X	X	X	
Read (Sense) Normal Completion	01	X8	X	X	X	X	X	X	X	X	
Open — Normal Completion	00	X8	0	0	0	RI	0	0	0	0	
Open — Intermediate Completion	00	X2	0	0	0	Rtry T.O.	0	0	0	0	
Open — Halted	00	XA	X	X	X	X	X	X	X	X	
Close — Normal Completion	04	X8	X	X	X	X	X	X	X	X	XX

*D04 field is valid only when Dump Msg Bit on.

Type-4 Record D04 Extended Status. This field is valid only for a read/write exception with DUMP MSG bit on.

Bit	Name	Description
0	Frame Check Sequence (FCS)	The CRC check failed for the last message received.
1	Primary Abort	A detected condition indicating abnormal termination of a message by the remote transmitting station.
2	Not used	–
3	Not used	–
4	NR Sequence Error	A command reject condition resulted from the receipt of an illegal NR sequence count in an information or supervisory frame containing good FCS.
5	Wrong Length Message	1. Information frame was longer than the read count. 2. Information frame was shorter than the minimum message length.
6	Data with Command	A command reject condition resulted from the receipt of a data field with an otherwise valid command for which no data field is defined. This bit will be on in addition to INVAL CMD (frame had good FCS).
7	Invalid Command	A command reject condition resulted from the receipt of an undefined or nonimplemented command field in a frame that has good FCS.

Type-4 System Incident Record. Status flag bits (D03 field) are described below; standard SDLC and data communication terminology apply:

Conn Prob. Some condition exists in the link that is preventing the proper establishment or reestablishment of communication with the remote station. This status is posted following 20 write (information message) retries, 20 ROL8, 20 CMDR, 20 XID, 20 NSA, or any combination of these. The counter is reset whenever a write (I-frame) is confirmed or when SNRM or RR resets.

Disc Rcvd. Set Disconnect Response Mode command received and acknowledged.

Dump Msg. One or more significant errors have occurred and may be command reject conditions. D04 field contains error bits.

Idle Timeout. A switched or nonswitched line has been inactive (no flags received) for 20 seconds, or there has been an incomplete open operation caused by hardware failure, or code error.

Link Test. Posted at command time upon receiving and decoding link test command. (FCS check has not been made yet.) Also indicated along with Rd Msg Aval at end flag time if valid link test has been received.

Lost Data. This bit is set along with the Rd Msg Aval bit. It indicates that a count exceeded condition exists in an otherwise normal read completion.

NPRO/Rcv Ovrn. A read overflow caused by:

1. Insufficient space allocated.
2. Line hung at "space" or valid data character.

This is a warning indicator; control code continues normal operation and receiving until disable or normal terminate sequence is received.

Overrun. An overrun condition has been detected by the hardware (Rcv mode) and the adapter is attempting recovery.

Poll Rcvd. The poll bit has been detected in the command field and no write operation is outstanding. (Poll cannot be verified until end frame time.)

Rd FBI. The storing of the last character read has caused the buffer count to go to 0.

Rd Msg Aval. Indicates that:

1. A complete message has been received with no detectable errors and is now available for processing.
2. A valid link test has been received; 8100 code has sent the correct response.

RI. A ring indicate signal had been detected while open operation was active (on CCITT circuit 108.1).

Rtry T.O. An indication during an open operation that a timeout has occurred during a wait for the data set to become ready. The condition prevails until either the data set becomes ready or SYSHOST is terminated (on switched line only.)

Sec Busy. An RNR response has been sent to the primary station due to lack of receive buffers in the 8100.

SNRM RCVD. A valid SNRM was received and acknowledged. If, after ACPU, the 8100 terminates it before ACPU, NSA is sent.

Underrun. An underrun condition has been detected by the hardware (XMIT mode) and the adapter is attempting recovery (secondary abort).

Write Rtry. The adapter is required to send a previously transmitted message (I-frame) or series of messages, in their entirety, due to lack of confirmation by sequence number from the primary station. (20 Write Retries = Conn Prob and both completions are posted.)

XID Rcvd. A valid XID was received. (XID is normally received with either no associated data field or with a 6-byte data field.) 20 XIDs in succession = Conn Prob.

CA340 How to Use the Error Log

The procedure for examining the error log depends upon whether the customer is using DPPX or DPCX. For DPPX, see CA341; for DPCX, see CA342.

CA341 DPPX

You are entering this section with DPPX incident record, class 5, subclass 1, and one of the following device types:

Incident Record Field 4	Device Type
M	SDLC – Primary
H	SDLC – Secondary
B	BSC
C	Start/Stop – 2741
Y	Start/Stop – TTY

Note: *For other device type values (Field 4), leave this section and refer to DPPX Error Log in Chapter 2, CP748.*

Proceed as follows:

1. Review Field 8, Compstat, for the following values: If Field 8 is hex 01, 04, or 08, go to step 2; if it is hex X2 or XC, go to step 3.
2. Review all record fields (see CA331). This is a software-related record indicating one of the following conditions: system status, software error/problem, command reject, system resource problem, etc. If this is not an intermittent problem (see CA134), restore the system to the customer. If this is an intermittent problem caused by customer-written programs, notify the system operator.
3. A hardware error is suspected. If you have not performed fault isolation using the CA MAP, start the CA MAP using Offline (A) checkout. If you have used the CA MAP, review the record fields and the field descriptions (CA331) for additional error data (such as specific locations, lines in error, interface, and function request performed).
4. At this point, you may perform general troubleshooting based on the information obtained in step 3, or you may follow specific procedures. For general trouble-shooting, go to step 5; for specific procedures, go to step 6.
5. With the error information available from step 3, isolate the failure or problem by probing or line monitoring those suspect lines/areas. Perform necessary repair action and retest.
6. Perform the steps in the Basic Checklist (CA501) and retest.
7. Perform card replacement (CA511) on:
   a. CA1/CA2 – control card
   b. CA3 through CA11 – CA features cards; retest (CA511).
8. Perform board-to-I/O Panel wire checks (CA420). Perform external cable checks (CA430). Repair as necessary; retest.
9. Perform IBM modem checks; see appropriate IBM modem manual. Retest.
10. Have customer check OEM modem; retest.

CA342 DPCX

How to Use the DPCX Condition/Incident Record

You are entering this section with DPCX CA feature record(s): type-2 record(s), type-3 record(s); type-4 system condition XX record(s), or a mixture of the foregoing records. Refer to the following appropriate sections:

Type-2 Records

Enter this section with a type-2 incident record. There is a possible failure in one of the 8100 adapters, the unit controller, or in the feature storage. Perform actions in sequence until the problem is localized and repaired.

1. Using the free-lance mode, loop all offline control card tests for 5 minutes (see the offline test procedures in Chapter 2). Record all failing adapter card PAs. For a single failing PA, go to the GFI for the appropriate action plan. For multiple failing PAs, use the appropriate action plan in the AA MAP. If the failing PA equals the CA feature PA, continue in this action plan.
2. Check all CA board voltages (see CA530).
3. Check all CA feature cables for proper seating (see CA525 for cable locations).
4. Replace the CA control card with a new card (see CA510).
5. Use Action Plan 14 in ST430 in Chapter 1.

Type-3 Records

Enter this section with a type-3 record.

1. If more than one type-3 record exists, reduce the record list, if possible, by deleting repetitive records.
2. Locate the D2, D3, D6, and D7 fields of the record(s) in Figure CA342-2. If you locate the fields in the figure, perform the listed action plans; if not, go to step 3.
3. Review the D3 field (completion code):
   a. D3 = hex XC, where X = any value. This value indicates that an unrecoverable error has occurred. Go to step 4.
   b. D3 = Any other value. This value indicates that customer action (PDPs) may be required or that an exception condition occurred. Action options are:
      (1) Review and analyze the CIL record (refer to CA332). The record content indicates the exception condition and/or the area in which the record condition occurred. Customer PDPs may be required using SMNs, operator messages, and other CIL records.
      (2) The customer should perform PDPs using the DPCX Operations Guide and the recorded SMN/message for system conditions. If no further action can be taken, either clear the CIL or note the contents of the log and restart customer operations. The next failure should provide additional error information in the log, SMNs, or operator messages. With this additional information: (1) the customer may perform additional PDPs, (2) you may enter the GFI (Chapter 1) using the appropriate messages, or (3) you may perform further error log analysis.
4. Convert the D6 status flags in all records from hexadecimal to binary.
5. Identify the active bits by name in the D6 status flags (see Figure CA342-1).
6. Locate the active bits in Figure CA342-1 and take the appropriate action. If more than one bit is active, perform actions in the following sequence:
   a. Machine check (bit 5)
   b. Invalid status (bit 7 or bit 0): Bit 0 is set by the SDLC Secondary code and bit 7 is set by the SDLC Primary code.

c. Intermediate open time out (bit 1)

d. DCE error (bit 2)

e. CTS fell (bit 2)

f. Write failure (bit 6)

g. Write timeout (bit 3)

7. Save the entire CA type-3 record logout for use by the next level of support.

D6 Status Flags		
Active Bit	**Description**	**Action Plans (CA350)**
0	Invalid Status	1, 2, 4
1	Intermediate Open Timeout	1, 2
2	DCE Error	1, 4
3	Write Timeout	2, 1
4	Reserved	
5	Machine Check	2, 6
6	Write Failure	1, 2
7	Invalid Status	1, 2, 4

Figure CA342-1. Field D6 Status Flags

Type-4 Records

You are entering this section with type-4 system condition 20 incident records.

1. If there is more than one type-4 record, reduce the record list, if possible, by deleting repetitive records.
2. Using the completion code D02, list the records in this sequence of priority:

   Completion Code

   X2
   X1
   X9
   X8
   XA
3. Convert the D03 field from hexadecimal to binary in all records.
4. Using the D02 field, then the D01 field of the record, locate the matching record format in Figure CA342-3. Incident Record Action Plan Table. Identify the active bits (D03 Field) of the record using the table. Record the Action Plan numbers from the Action Plan block corresponding with the active bits of the record.
5. Perform step 4 for all listed records, and maintain the sequence order (step 2) in listing the Action Plan numbers.
6. Perform the Action Plans, (CA350) in the order listed. Do not repeat any Action Plan that is listed more than once.

D2 Field	D3 Field	D6 Field	D7 Field	Failure Description	Associated SMN	Action Plans (CA350)
40	40, C0	40, C0	C0	All control units timed out	61A0	2, 1, 4
40	04	40	N/A	CHIO overrun	91A1	3
40	04	04, 84	N/A	CHIO underrun	91A1	3
40	04	20	N/A	Alternate buffer overrun	91A1	3
40	04	10	N/A	Receive control overrun	91A1	3
40	40, C0	40, C0	20	Nonproductive RCV timeout	61A1	4, 5
40	40, C0	40, C0	C0	'N' control units timed out	61A6	7
40	08, 88	08, 88	90	'N' write retries	61B7	4, 5
40	01	C0, 40	N/A	Bad outbound performance counter overflow (D15 field)	61B5	13
40	01	C0, 40	N/A	Good outbound performance counter overflow (D14 field)	61B5	13
40	01	81	N/A	Read message available truncated data (D14 field)	61B1	4, 5
40	01	82	N/A	0 data '1' frame received	61B1	4, 5
40	01	04, 84	N/A	Good inbound performance counter overflow (D12 field)	61B5	13
40	10, 90	10, 90	90	CMD reject received	61B5	4, 5
40	10, 90	10, 90	82	Unexpected or duplicate non-sequenced response	61B5	4, 5
40	08, 88	08, 88	88	Lost data	61B5	4, 5
40	08, 88	08, 88	82	'N' NS errors	61B5	4, 5
40	04, 84	04, 84	88	N_r sequence error	61B5	4, 5
40	04, 84	04, 84	81	Invalid response received	61B5	4, 5
40	02, 82	02, 82	C0	Beacon received	61B5	4, 5
40	02, 20, A0	20, A0	C0, 90	Bad inbound performance counter overflow (D13 field)	61B5	13

Figure CA342-2. Field 9 Equals 40

D01 Field	D02 Field	D03 Field Bit Definition Action Plan Number 0	1	2	3	4	5	6	7
0 0	X 2	0	0	0	Rtry T.O. 1, 2, 4	0	0	0	0
0 1 0 2	X 2	SNRM Rcvd 9, 1	Disconn Rcvd 9, 1, 5	Write Retry 3, 1, 4	Idle Timeout 9, 1, 4	Overrun 3, 1, 5	Underrun 3, 1, 5	Conn Problem 3, 1, 4	Dump Msg 12
0 1 0 2	X 1	XID Rcvd 10, 1	Link Test 10, 1	NPRO/Rcv OVRN 11, 1	Lost Data 3, 4	Sec Busy 3, 11, 1	Rd FBI 10, 1	Rd Msg Aval 10, 1	Poll Rcvd 9, 1
0 1 0 2	X 9	0	0	0	Lost Data 3, 4	0	0	Rd Msg Aval 10, 1	0
0 0	X 8	0	0	0	RI 3, 1, 4	0	0	0	0
0 1 0 2 0 3	X 8	X	X	X	X Normal Completion	X	X	X	X
0 0 0 2	X A	X	X	X	X Any Active Bit, Do Action Plan 8	X	X	X	X

Legend:

X = Any Value

0 = Always zero.

Note: *This table is not listed in numerical sequence, but in the priority order requested in step 2. Action Plan numbers 1 through 12 are in CA350.*

Figure CA342-3. Type-4 Incident Record Action Plan Table

Mixed Records

You are entering this section with a mixture of CA type-2, type-3, and type-4 records:

1. Delete repetitive CA records.
2. Perform repair action plans in priority order.

Mixed record repair action plans are the accumulated individual record type action plans and are to be performed on a record type priority basis. This priority is: first, type-2, second, type-3, third, type-4.

For example, for mixed CA records of types 2 and 4: first, perform the repair action plans for type-2 records, then perform the repair action plans for type-4 records. Because there are no type-3 records, no type-3 action plans can be performed.

CA350 Action Plans to Correct Intermittent Failures

Action plans should be used as follows:

1. Perform the following action plans in the sequence listed. If a problem is not resolved by the action plan, perform the next specified action plan.
2. When a problem is identified, make repair or replacement, or take action as directed. When the problem is corrected, verify the repair by performing the test or procedure that initially failed.
3. Use the references provided in each action plan.

Action Plan 1. Perform CA Offline tests if not already done. Use CA MAPs, menu selection A, Offline.

Action Plan 2. Loop CA Offline control card tests in free-lance mode for 5 minutes (see Chapter 2, CP600 for offline test procedures). If a failure occurs, replace the control card with a new one corresponding to the failing address (see CA513).

Action Plan 3. System overload condition exists. If the failure persists, the system workload should be reduced.

Action Plan 4. Possible modem, communications line, or remote site problem. If an IBM modem is installed, perform IBM modem tests (refer to the appropriate IBM modem maintenance manual). Have the customer do remote site problem determination and testing. The customer should request communications line and modem testing from the appropriate service group (PTT, Telco, private, self) if remote site problem determination detects no problem.

Action Plan 5. Possible host site problem. Use only if the 8100 (PA) is secondary. If not already done, request that the host site service representative or customer personnel:

1. Verify that all host system components (such as S/370, 370X, modems, data couplers, and communications lines) are operational.
2. Check for correct software levels in S/370, 370X.
3. Check for 8100 address and configuration data at S/370 and 370X.
4. Take diagnostic action on S/370 and 370X.

Action Plan 6. Possible unit controller, storage, or adapter problem. Use Action Plan 14 of the ST400 section of Chapter 1.

Action Plan 7.

1. Use SYSLDEV (see CP851 in Chapter 2) to determine that the control units and devices are online and ready.
2. Check all control units for valid OFF condition.
3. Request control units/devices to run subsystem tests to insure hardware integrity.

Action Plan 8. HALT condition.

1. Determine reasons for halt, and correct. Check other incident record bits. Possible reasons for halt are:
   - Customer operating procedure (8100 site).
   - Customer operating procedure (remote site).
   - Noise condition (all equipment).
   - Equipment malfunction (hardware or software), such as 8100, S/370, 370X, modems, data couplers, communication lines.
2. Have the customer retry communications.

Action Plan 9. Normal status condition. Check for other active bits in the field and for other CA incident records.

Action Plan 10. Normal condition, unless frequency of occurrence and/or another incident record indicates an irregular condition. Check for other active bits in the field and for other CA incident records.

Action Plan 11. Possible software problems.

1. Perform control storage dump (see Chapter 2).
2. Initialize the 8100.
3. Request remote site to initialize, if necessary.
4. Have the customer reestablish 8100 communications.

Action Plan 12. Dump Message bit on. When this bit is active, the D04 field is valid.

1. Locate the D04 field (30) in the type-4 CA incident record.
2. Convert the D04 field from hexadecimal to binary.
3. Identify the active bits of the D04 field, and enter the table below to select the corresponding action Plans for the active bits. Record the action plan numbers.

D04 Field 30 Extended Status (Binary)

Bit	Action Plan
0 – FCS	7, 2, 4, 5
1 – Primary Abort	7, 11, 2, 5, 4
2 – Not used	–
3 – Not used	–
4 – NR Sequence Error	7, 11, 2, 5
5 – Wrong Length Message	7, 11, 2, 5
6 – Data with Command	7, 11, 2, 5
7 – Invalid Command	7, 11, 2, 5

Action Plan 13. A performance counter overflow (SMN 61B5) occurred because a counter reached a predetermined total. Predetermined totals were set by SYSIMOD (934) Option A, Part 2, by the customer.

Good Counter Overflow – The customer should be made aware of the overflow and he should reset the predetermined total. This overflow indicates a heavier than normal traffic day.

Bad Counter Overflow – The customer should be made aware of the overflow. This overflow indicates an unusual number of line errors or intermittents have occurred.

Divide the bad messages by the good messages to determine the daily error rate. Recommended performance counter settings should be a ratio of 10 to 1, good messages to bad messages (that is, 1 bad message per 10 good messages). It is a customer decision to establish and modify performance counter settings.

You should:

1. Recommend that the customer modify the overflowed counter setting to a higher value (present value + 25).
2. Recommend that the customer do remote site problem determination.
3. Recommend that the customer request communications line testing from the appropriate service group (PTT, Telco, private, self).
4. Perform CA offline tests if not already done. Use CA MAPs, menu selection A, Offline.
5. Inspect the error log for other CA records which may provide 8100 hardware error information.

CA400 Signal Paths and Detailed Operational Description

CA410 Board Net Check Procedures

Caution: Turn off system power when plugging or unplugging cards or cables and when checking board net continuity.

1. Remove CAX cards and CACX cables at the appropriate board. Inspect the CA section of the board for damage, dirt, coated or broken pins, or any other unusual board condition. See CA513, Card Locations, and CA520, Board and Cable Layout.
2. Test the board nets for continuity as defined by the action plan or the steps in CA411.
3. After board net fault isolation, make the necessary repair action, and then run the CA test that detected the CA failure.

CA411 Adapter Card-to-SSCF Wiring Check

Caution: Turn off system power when plugging or unplugging cards or cables and when checking board net continuity.

1. Remove CAX cards and CACX cables at the appropriate board. Inspect the CA section of the board for damage, dirt, coated or broken pins, or any other unusual board condition. See CA513, Card Locations, and CA520, Board and Cable Layout.
2. Check the continuity between the adapter card test point and the related SSCF test point (see Figure CA411-1). Use machine line names to determine the point-to-point continuity check.
3. If an open circuit is found, determine if the open is in the cable or the board wiring. A temporary fix can be made by wire-wrapping the test points together.
4. To verify the fix: run the CA adapter tests in free-lance mode. Refer to CA211 for test descriptions, and CA202 or Chapter 2, CP462, to invoke tests using the free-lance mode.

Line Name	From SSCF Card (SC5)	To SDLC/BSC/S-S Adapter Card
Data Bit 0	B02	G02
Data Bit 1	B08	J02
Data Bit 2	D11	D10
Data Bit 3	G04	G08
Data Bit 4	J07	J04
Data Bit 5	G09	D09
Data Bit 6	M02	B09
Data Bit 7	P10	D06
Data Bit P0	M12	B02
Data Tag	G02	B05
Halt	J06	G04
Address Tag	G10	D05
Command Tag	J10	B08
System Reset	G12	J05
I/O Tag (B)	G13	B04
Channel Grant High	M04	Note 1
Channel Grant Medium	P12	Note 1
Parity Valid	B04	D07
Valid Byte 0	B09	–
End of Chain	D09	Note 1
Channel Request Medium	G03	Note 1
Channel Request High	M05	Note 1
Int Req RMVD Tag (B)	J13	D02
Valid Byte 1 (B)	J12	G03
Int Req Bus Bit in 0	D02	G09
Int Req Bus Bit in 1	D04	B07
Int Req Bus Bit in 2	B07	G07
Int Req Bus Bit in 3	J04	J07
Int Req Bus Bit in 4	G07	G10
Int Req Bus Bit in 5	P04	J10
Int Req Bus Bit in 6	P05	J11
Int Req Bus Bit in 7	M07	J12
Int Req Bus Bit in P	P07	G12

Note 1: *Refer to CA562, Board Personalization Channel Grant/Request Wiring, for specific wiring.*

Figure CA411-1. Adapter Card to SSCF Wiring Chart

CA412 Net Checks by Error Number Message

For procedures, see CA410. Using the error message, check continuity in the nets indicated.

Caution: Turn off system power when checking continuity.

Test Message or Routine No.	**Net Checks**
RR = 01–15	Use Figure CA411-1, Adapter Card to SSCF Wiring Chart.
RR = 16	EIA – Use Figure CA548-1, Routine 16 Troubleshooting Diagram. V.35 – Use Figure CA545-2, Routine 63 Troubleshooting Diagram for V.35 Modem. X.21 (nonswitched) – Use Figure CA546-1, Routine 67, 68 Troubleshooting Diagram
RR = 18	Use Figure CA550-1, Loop Troubleshooting Diagram – 1 Lobe, or Figure CA550-2, Loop Troubleshooting Diagram – 2 Lobe.
RR = 19	Use Figure CA542-1, Routine 19 Troubleshooting Diagram (Integrated Modem – Nonswitched Line).
RR = 20	Use Figure CA542-2, Routine 20 Troubleshooting Diagram (Integrated Modem – Switched Line).
RR = 21/22	Use Figure CA547-1, Routine 66 Troubleshooting Diagram.
RR = 61	Use Figure CA543-1, Routine 61 Troubleshooting Diagram.
RR = 63	Use Figure CA545-1, Routine 63 Troubleshooting Diagram For EIA Modem. Use Figure CA545-2, Routine 63 Troubleshooting Diagram For V.35 Modem. Use Figure CA545-3, Routine 63 Troubleshooting Diagram For V.35 Direct Connect Terminal. Use Figure CA545-4, Routine 63 Troubleshooting Diagram For V.35 Direct Connect – Peer-to-Peer.
RR = 66	Use Figure CA547-1, Routine 66 Troubleshooting Diagram.
RR = 67 = 68	Use Figure CA546-1, Routines 67 & 68 Troubleshooting Diagram
MSG = PA80	Use Figure CA562-1, Channel Grant Wiring Tables for this PA.

CA413 Not Used

CA414 Driver Card Pin Assignments

Each driver card is a double card. The integrated modem switched versions use D05 and D06 for transmit and receive connections to DT (Data Tip).

Pin	Integrated Modem	EIA/CCITT Interface	DDS Card	Loop Card	V.35	X.21 (NS)
B02	Data Term. Ready	Data Term. Ready		DTR	DTR	DTR
B03	Select Standby	Select Standby		SS		
B04	Modem Type Select	Data Sig. Rate Sel		MMS (DRS)		
B05	Test (Wrap)	Test Control	Wrap	Test (Wrap)	Test Control	Test Control
B06	-5V dc		-5V dc	-5V dc	-5V dc	
B07		Tsm Sig Elem Timing	Transmit Clock	TSET (XMIT CLK)	Tsm Sig Elem Timing	Tsm Sig Elem Timing
B08		Rcv Sig Elem Timing	Receive Clock	RSET (RCV CLK)	Rcv Sig Elem Timing	Rcv Sig Elem Timing
B09		New Sync		NS	NS (RSET)	
B10	Received Data	Received Data	Receive Data Mark	RX (RCV DATA)	Receive Data	Receive Data
B11	+8.5V dc	+8.5V dc	+8.5V dc	+8.5V dc	+8.5V dc	
B12	Carrier Detect	Carrier Detect	Carrier Detect	RLSD	RLSD	RLSD
B13	Data Set Ready	Data Set Ready	Data Set Ready	DSR	DSR	DSR
D02	Request to Send	Request to Send	Request to Send	RTS	RTS	RTS
D03			+5V dc		+5V dc	+5V dc
D04	Send Data	Transmit Data	Send Data Mark	TX (XMIT DATA)	Transmit Data	Transmit Data
D05	DT (tsm or rcv)	Test Point				
D06	DT (rcv or tsm)	Test Point				
D07	-8.5V dc	-8.5V dc			-8.5V dc	
D08	Signal Ground	Signal Ground	Signal Ground		Ground	Ground
D09		Transmit Clock (DTE)		LOOP CLK I/O	TSET (DTE)	
D10	Test Mode	Test Mode	Test Mode		Test Mode	Error Indicate (Not used)
D11		Driver Degate		POR	Antiglitch	
D12	Calling Indicator	Calling Indicator		SMS (RI)	RI	
D13	Clear to Send	Clear to Send	Clear to Send	CTS	CTS	CTS
G02	DT (tsm)		Transmit Line — DT	D+ (+TRANS LINE)	Transmit Data (-TD)	Transmit A (TA)
G03	OH (off hook)	Request to Send			RTS	
G04		Received Data		RLSD CNTL I/O	RSET (+) (DCE)	Indication B (IB)
G05		Select Standby			RSET (+) (DTE)	Control A (CA)
G06	-5V dc		-5V dc	-5V dc	-5V dc	
G07		Transmit Data		Pick Relay 1	TSET (-) (DTE)	
G08		New Sync		Pick Relay 2	TSET (+) (DTE)	
G09	DT (rcv)		Receive Line — DT1	R+ (+REC LINE)	Receive Data (-RD)	Receive A (RA)
G10	SH (switch hook)	Clear to Send		Lobe 2 Cntrl	Clear to Send	
G11	+8.5V dc	+8.5V dc	+8.5V dc	+8.5V dc	+8.5V dc	
G12		Transmit Clock (DTE)		Degate Rec		
G13	RI (Ring Indicate)	Calling Indicator		Degate XMIT I/O	TSET (+) (DCE)	SET B (SB)
J02	DA (modem ready)	Data Term. Ready		Loop Data I/O	DTR	
J03			+5V dc		+5V dc	+5V dc
J04		Tsm Sig Elem Timing			TSET (-) (DCE)	SET A (SA)
J05	DR (tsm)		Transmit Line — DR	D- (-Trans Line)	Transmit Data (+TD)	Transmit B (TB)
J06		Data Sig Rate Sel		Carrier Sel 1	RSET (-) (DTE)	Control B (CB)
J07		Test Control		Carrier Sel 2	Test Control	
J08	Signal Ground	Signal Ground	Signal Ground		Ground	
J09	CCT (coupler cut-through)	Data Set Ready			DSR	
J10		Rcv Sig Elem Timing		Data Sel 1	RSET (-) (DCE)	Indication A (IA)
J11		Test Indicator		Data Sel 2	Test Indicator	
J12		Rcv Line Sig Detect		Half Speed	RLSD	
J13	DR (rcv)		Receive Line — DR1	R- (-REC LINE)	Receive Data (+TD)	Receive B (RB)

CA420 Board-to-I/O Panel Connections

CA421 8130 Board-to-I/O Panel Connections

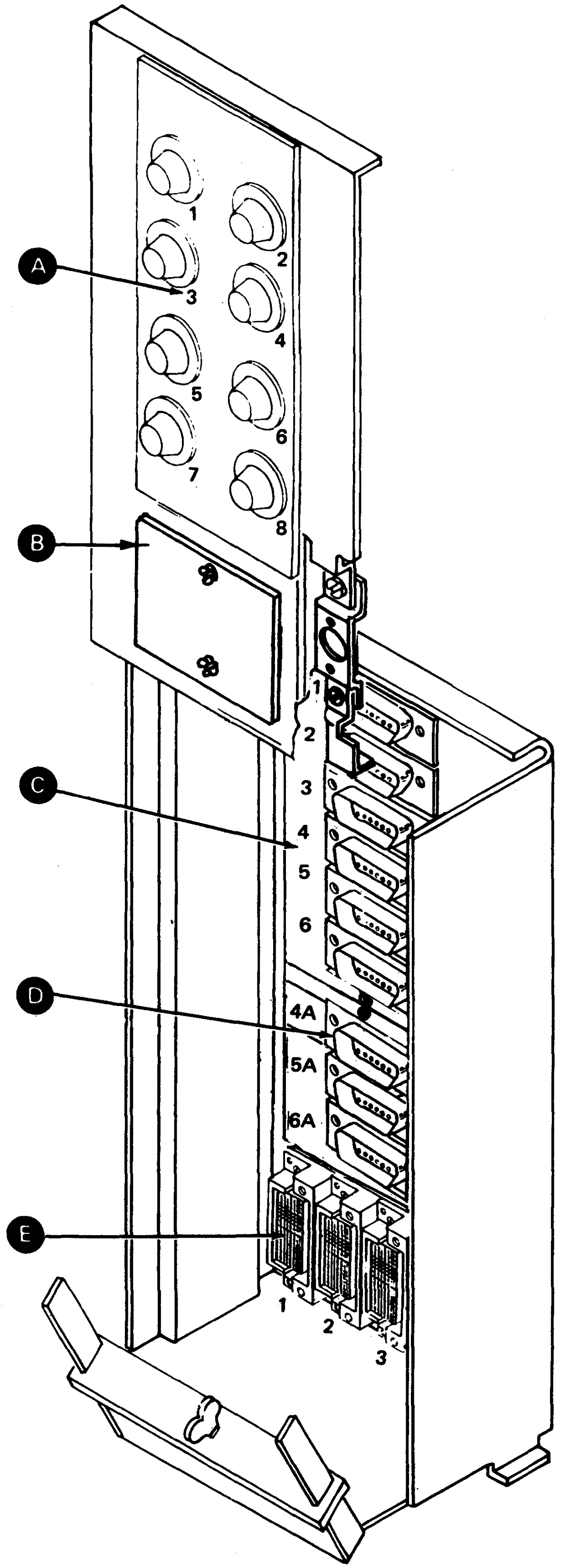


Figure CA421-1. 8130 I/O Panel Connections (Rear View)

A = Integrated modem transmit and operational switches (U.S./Canada). Switch positions 7 and 8 are not used.
B = Not used by the 8130.
C = Communications connectors.
D = For second lobe — loop port number has 'XA' designation.
E = Connectors for cables to 8101 and 8809.

Function	Port No.	8130 Boards	
		From	To
Any CA feature	1*	01A–A2Z2	01T–C1
	2*	01A–A2Z3	01T–C2
	3	01A–A2Z4	01T–C3
	4	01A–A2Z5	01T–C4
	5	01A–A2Z6	01T–C5
	6	01A–A2V5	01T–C6
Loop, second lobe	4	01A–A2V4	01T–D4A
	5	01A–A2V3	01T–D5A
	6	01A–A2V2	01T–D6A

*Not loop

CA422 8140 Model AXX Board-to-I/O Panel Connections

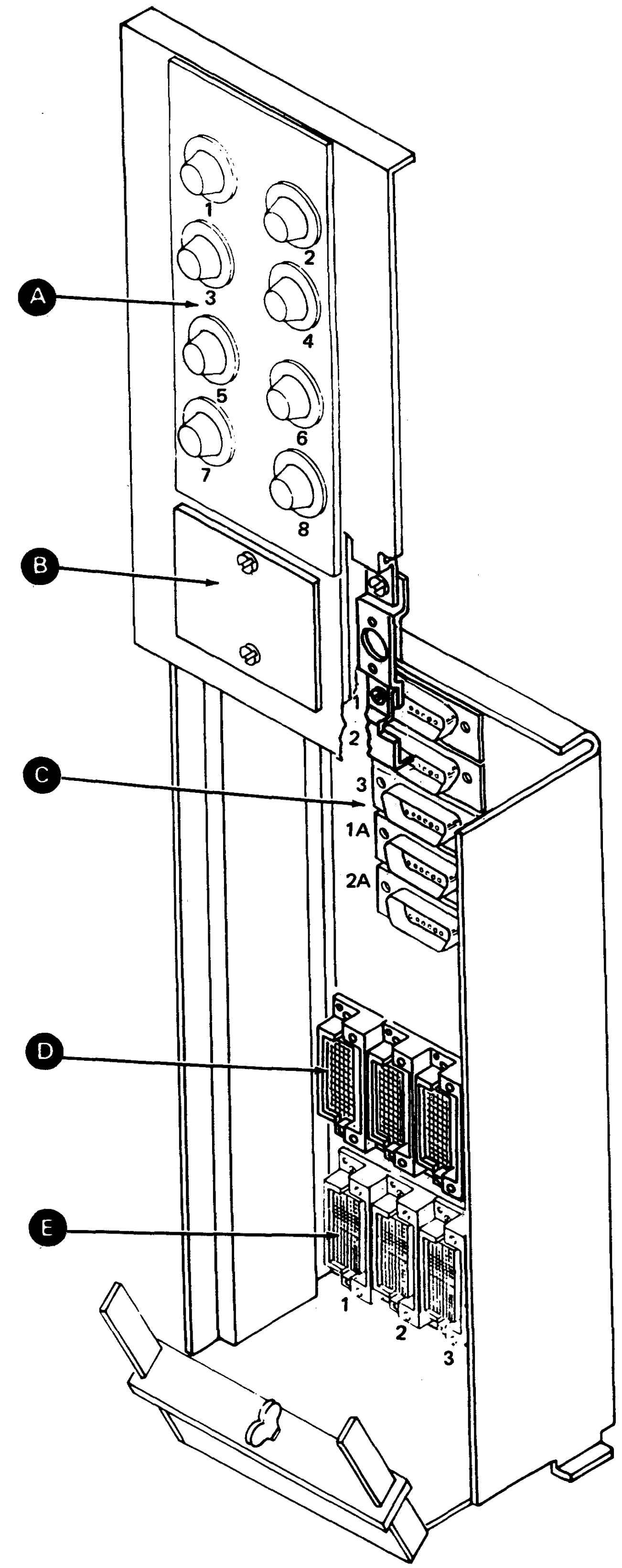


Figure CA422-1. 8140 Model AXX I/O Panel Connections (Rear View)

A = Integrated modem transmit and operational switches (U.S./Canada).
B = Not used by 8140.
C = Communications connectors. For second lobe, loop port number has 'XA' designation.
D = SSCF bus I/O panel
E = Connectors for cables to 8101 and 8809.

Function	Port No.	8140 Boards	
		From	To
Any CA feature	1	01A–A2Y1	01T–C1
	2	01A–A2Y2	01T–C2
	3	01A–A2Y3	01T–C3
Loop, second lobe	1	01A–A2Z1	01T–C1A
	2	01A–A2Z2	01T–C2A

CA423 8140 Model BXX Board-to-I/O Panel Connections

Function	Port No.	From	To
Any CA Feature	1	01A-A2Y3	01T-1
	2	01A-A2Y2	01T-2
	3	01A-A2Z2	01T-3
	4	01A-A2Y1	01T-4
	5	01A-C2Y3	01T-5
	6	01A-C2Y2	01T-6
	7	01A-C2Z2	01T-7
	8	01A-C2Y1	01T-8
	9	01A-D2Y3	01T-9
	10	01A-D2Y2	01T-10
	11	01A-D2Z2	01T-11
	12	01A-D2Y1	01T-12
Loop, second lobe	1-4	01A-A2Z3	01T-13
	5-8	01A-C2Z3	01T-14
	9-12	01A-D2Z3	01T-15

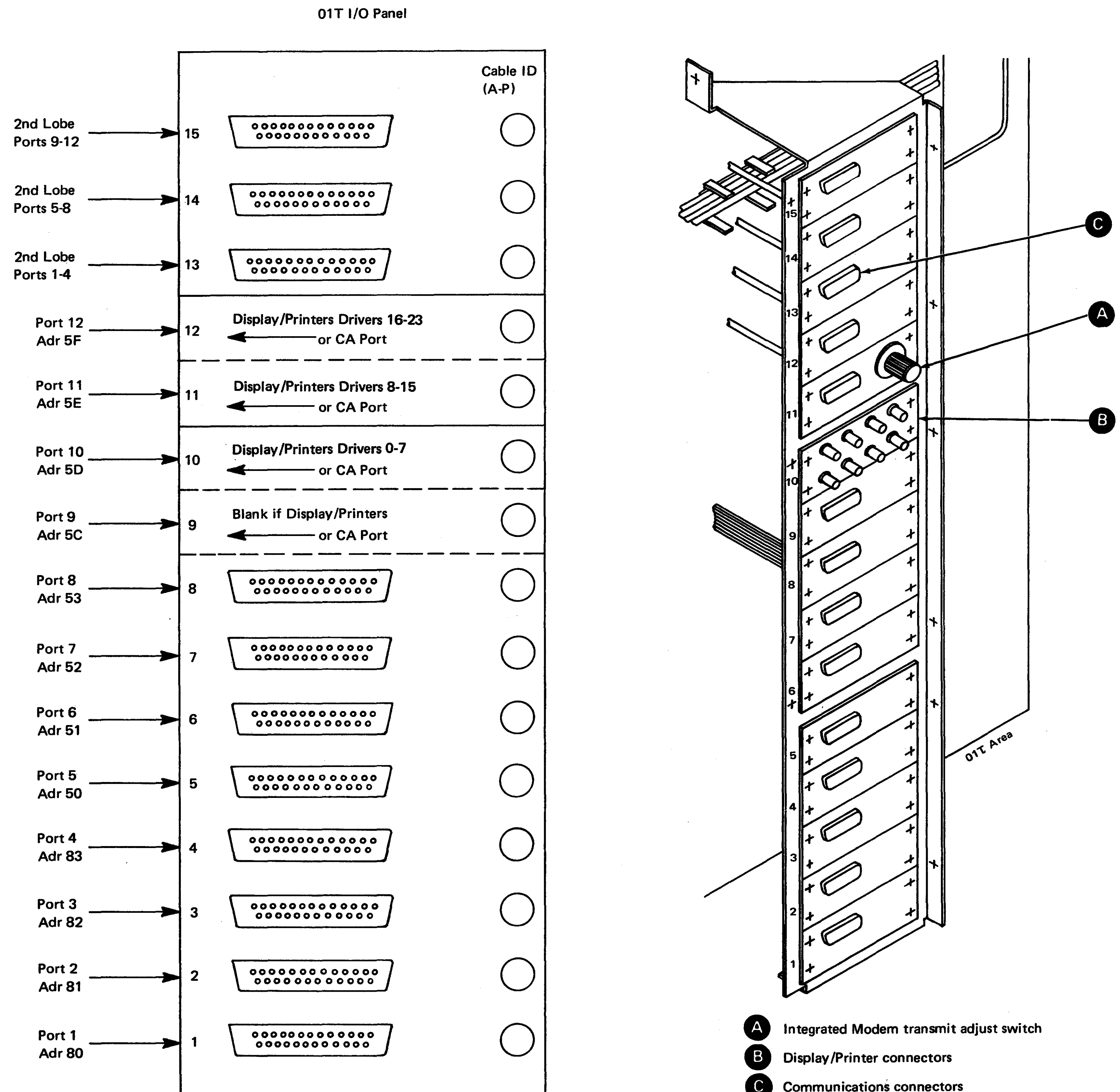
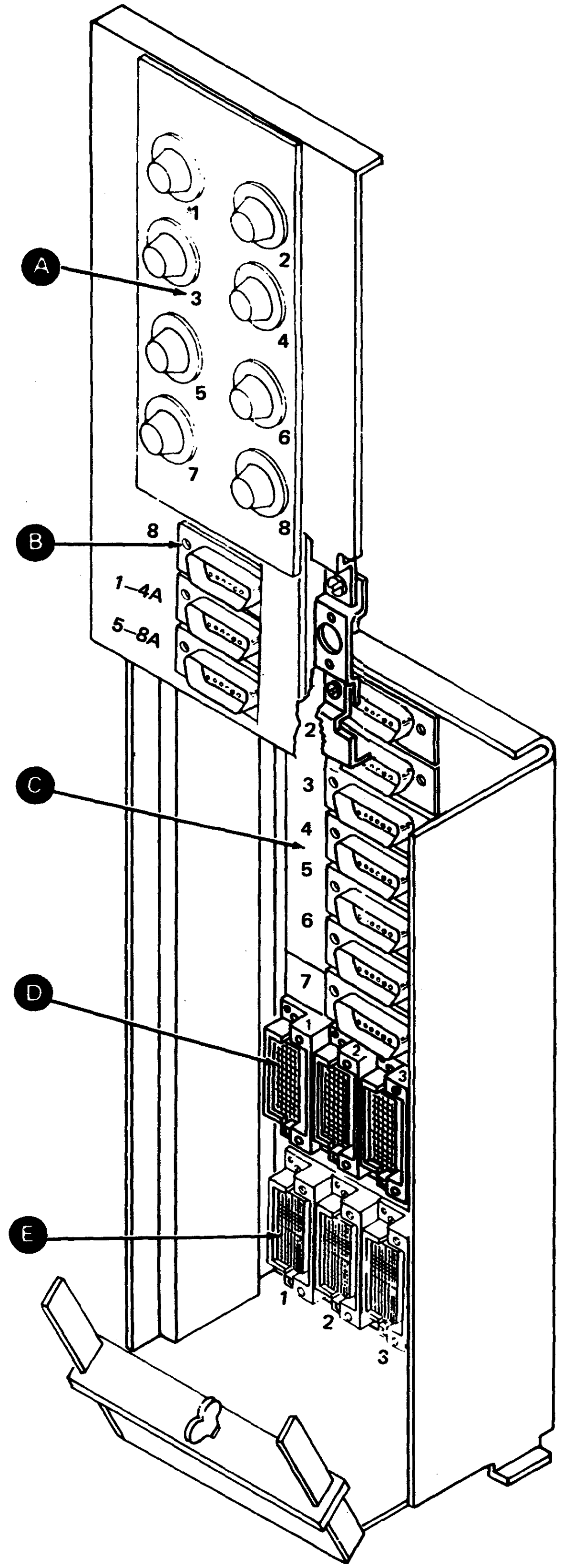


Figure CA423-1. 8140 Model BXX I/O Panel Connections (Rear View)

CA424 8101 Board-to-I/O Panel Connections



A = Integrated modem transmit and operational switches (U.S./Canada)
B = Communications and second lobe loop connectors. For second lobe, loop port number has 'XA' designation.
C = Communications connectors
D = SSCF bus I/O panel
E = Connectors for cables to 8101 and 8809.

Function	Port No.	Board PN 4939821	
		From	To
Any CA feature	1 2 3 4	01A–A1Y3 01A–A1Y2 01A–A1Z2 01A–A1Y1	01T–C1 01T–C2 01T–C3 01T–C4
Loop, second lobe	1–4	01A–A1Z3	01T–(1–4)A
Function	Port No.	Board PN 4939822	
		From	To
Any CA feature	5 6 7 8	01A–B1Y3 01A–B1Y2 01A–B1Z2 01A–B1Y1	01T–C5 01T–C6 01T–C7 01T–C8
Loop, second lobe	5–8	01A–B1Z3	01T–(5–8)A

Figure CA424-1. 8101 I/O Panel Connections (Rear View)

CA430 External Cable Descriptions

Refer to Figure CA430-1 for a summary of 8100 Communications Cables.

MIM Cable ID	Cable Description	MIM Reference	Internal Cable Part Number	Plug/ Cable ID Code	External Cable		External Cable	
					Group Number	Option 1 – Cable Part Number	Wrap Plug Part Number	Option 2 – Cable Part Number
CAC3	Loop – Single-lobe	CA435	8269773	E	3709	7389950	7389282 (Note 1)	Same as option 1
CAC3	Loop – Two-lobe (1st)	CA435	8269773	E	3726-A	7389950		
CAC4	Loop – Two-lobe (2nd)	CA435	8269774	E	3726-B	7389950		
CAC5A	EIA – Modem (except Japan)	CA431	8269775 8269784(UK)	C C	3724 3724	8269826* 8269826*	Use Modem Interface Test Set (Note 2)	7389484
CAC5A	EIA – Modem (Japan)	CA431	8269775	C	3729	6835482*		
CAC5B	EIA – Direct Connect-Terminal	CA431	8269775 8269784(UK)	H H	3721 3721	4946680 (EC389171) 4946680 (EC389171)	6835347 or 6835642	Same as option 1
CAC5B	EIA – Direct Connect Peer-to-Peer	CA431	8269775 8269784(UK)	H H	3727 3727	6835405 6835405		
CAC6A	V.35 – External Modem	CA433	8269777 8269783(UK)	G G	3718 3718	8269589 8269589	6835348	Same as option 1
CAC6B	V.35 – Direct Connect-Terminal	CA433	8269777 8269783(UK)	J J	3719 3719	8269590 8269590	6835349	Same as option 1
CAC6B	V.35 – Direct-Connect – Peer-to-Peer	CA433	8269777 8269783(UK)	K K	3720 3720	8269591 8269591	6835353	Same as option 1
CAC7	DDS	CA432	8269774	F	3717	8269827*	6835350	8269540
CAC8	Integrated Modem-NS – WT except Canada, Japan	CA434	8269774	A	3722	7389482	No	No
CAC8	Integrated Modem-NS – U.S., Canada, Japan	CA434	8269774	B	3723	7389483	No	No
CAC9	Integrated Modem-SW – WT	CA434	7389491	A	3722	7389482	No	No
CAC9	Integrated Modem-SW – U.S., Canada	CA434	8269772	D	3725	7389485	No	No
CAC11	X.21 (Nonswitched) – Japan only	CA436	8269777	P	3728	8269828*	6835379	6835364

*Cable with Wrap Switch Assembly.

Note 1: *Use plug at CSU only.*

Note 2: *Modem clock must be passed to 8100 for CE testing.*

Figure CA430-1. 8100 Communications Cable Summary

CA431 EIA Cables

EIA – External Modem Cable (CAC5A)

The EIA external modem cable has a standard 25-pin female EIA connector on the 8100 end. The cable contains 15 shielded wires and a covered switch assembly; the modem end has a standard 25-pin male EIA connector (see Figure CA431-1)

The switch assembly has two positions – Test and Operate. The Operate position is for normal communication operations; the Test position is used by the customer in problem determination and by the Service Representative for fault isolation. For alternative, see Note 2.

The Test position wraps the following lines:

- Transmit Data (2) to Receive Data (3)
- Transmit Clock (15) to Receive Clock (17)
- Request To Send (4) to Clear To Send (5) and Receive Line Signal Detect (8)
- Data Terminal Ready (20) to Data Set Ready (6)

Except for the clock lines, the line wraps are isolated from the modem when in the Test position.

EIA external modem cable pin assignments and line names follow:

Pin	Common Name*
2	Transmit Data
3	Receive Data
4	Request to Send
5	Clear to Send
6	Data Set Ready
7	Signal Ground
8	Receive Line Signal Detect
11	Select Standby
15	Transmit Clock
17	Receive Clock
18	Test
20	Data Terminal Ready
22	Ring Indicate
23	Data Rate Select

*Refer to CA631 for EIA/CCITT names.

Notes:

1. *The Japanese version has metric screws on the modem connector end.*
2. *Refer to Figure CA430-1 for cable alternative/options.*

EIA – External Modem Cable (CAC5A)
Wrap Switch Shown in Test Position

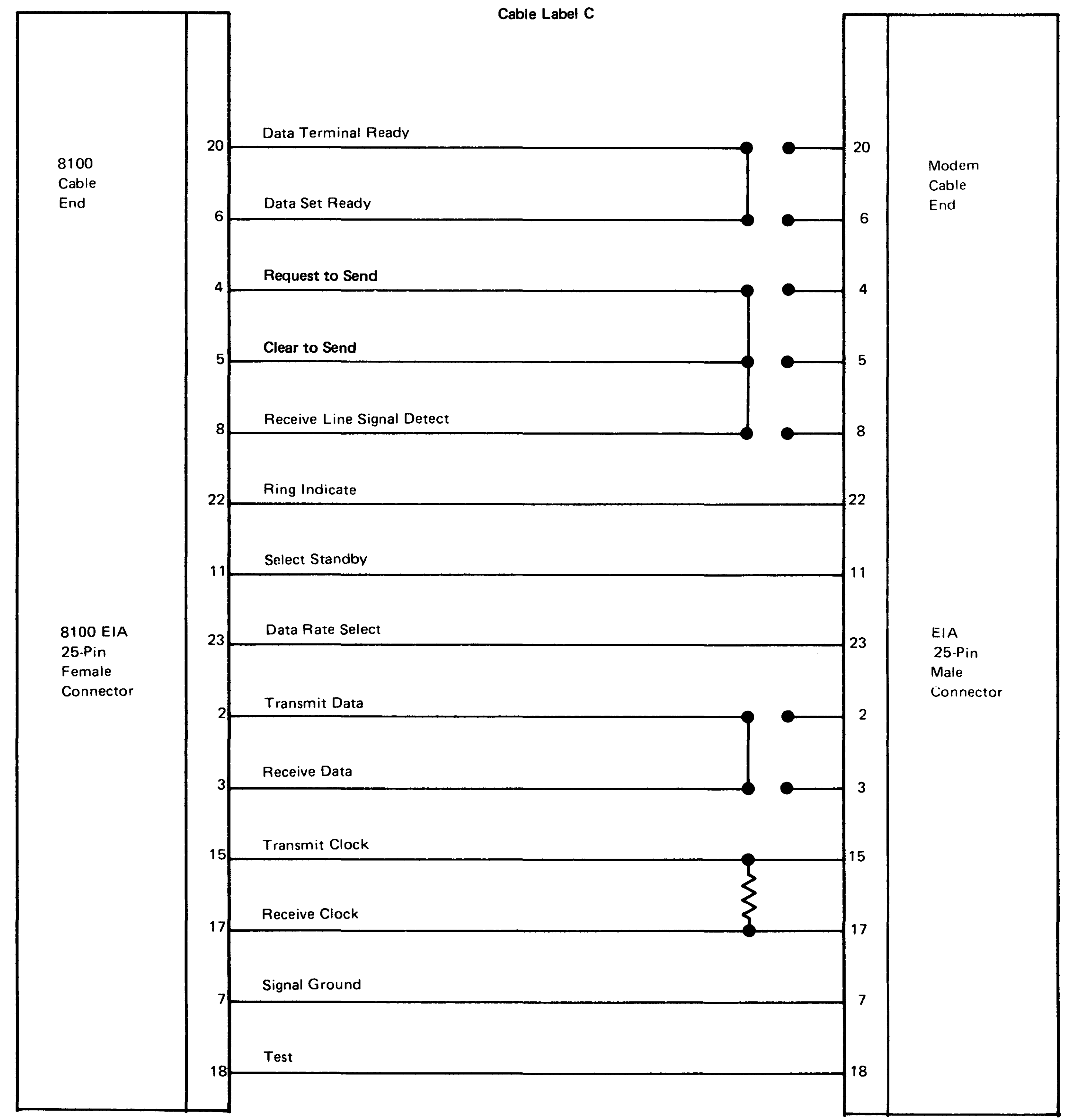


Figure CA431-1. EIA-External Modem Cable (CAC5A)

EIA – Direct-Connect Cable (CAC5B)

The EIA direct-connect cable has a standard 25-pin, female, EIA connector on the 8100 end. The cable contains 15 shielded wires, and the direct-connect attachment end has a **standard 25-pin, female, EIA connector (see Figure CA431-2).**

A wrap plug provides wrap capability for problem determination by the customer and fault isolation by the Service Representative (Figure CA431-2).

The wrap plug wraps the following lines:

- Transmit Data to Receive Data
- Data Terminal Ready to Receive Line Signal Detect

The direct-connect end has additional internal connector wraps:

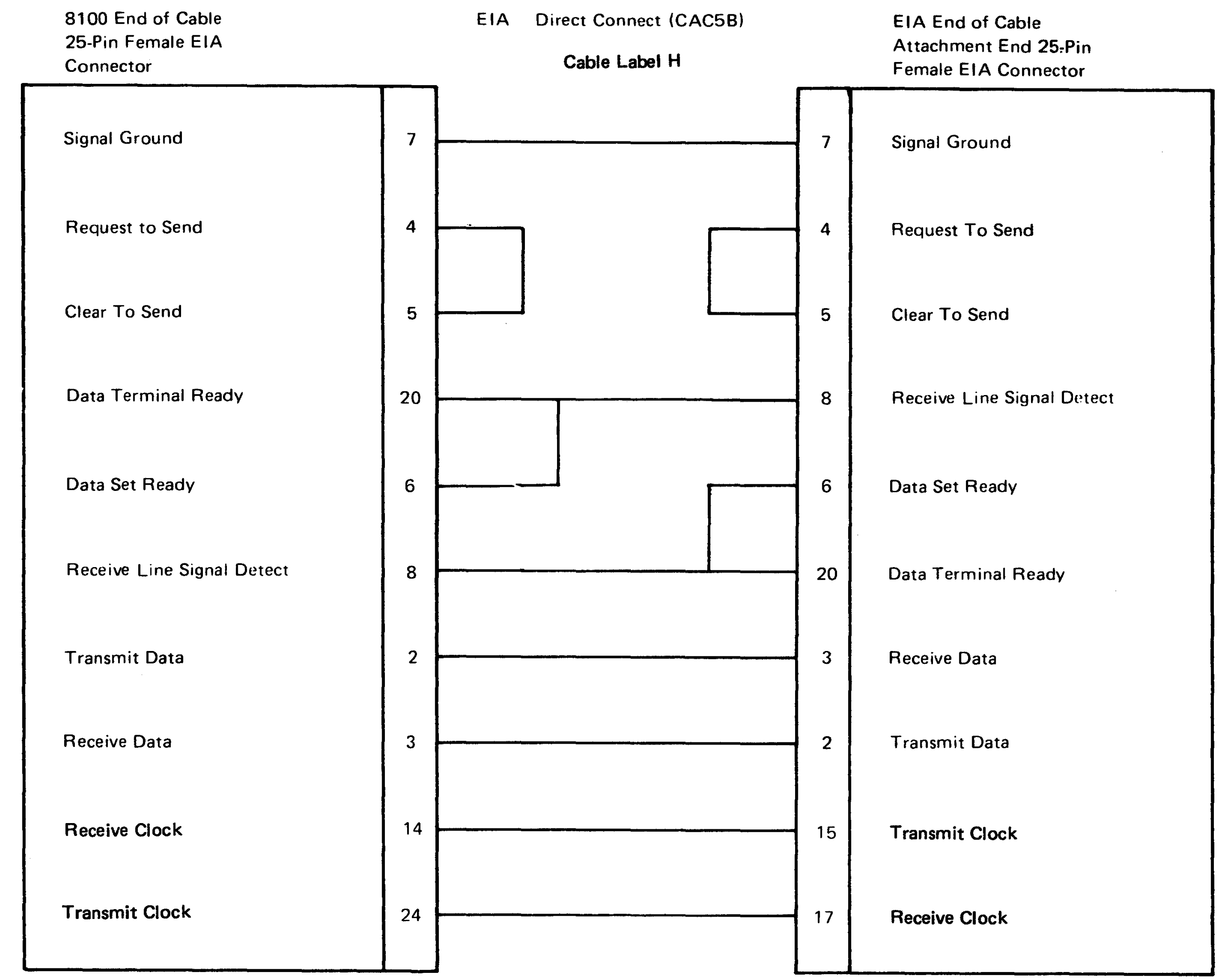
- Request To Send (4) to Clear To Send (5)
- Data Set Ready (6) to Receive Line Signal Detect (8) and Data Terminal Ready (20)

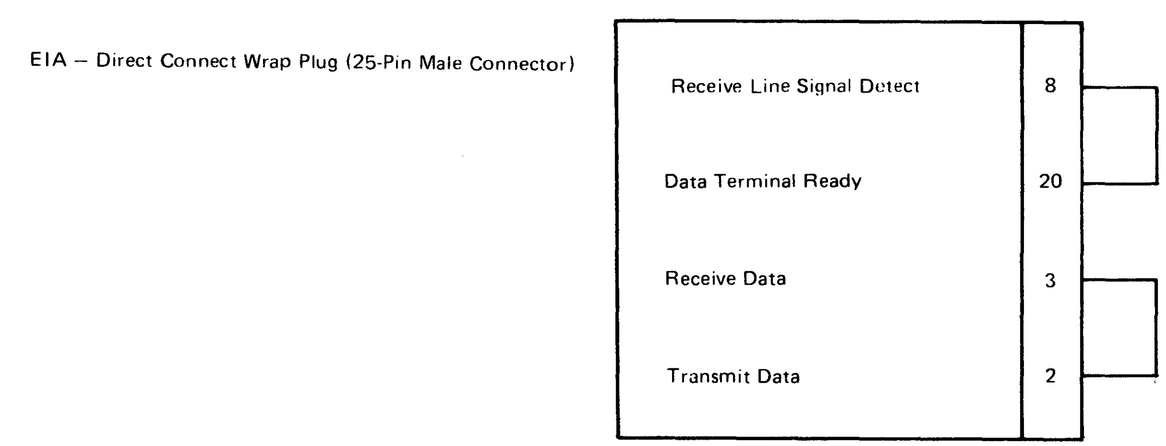
EIA direct-connect cable pin assignments and line names follow:

Pin	Common Name*
2	Transmit Data
3	Receive Data
4	Request to Send
5	Clear to Send
6	Data Set Ready
7	Signal Ground
8	Receive Line Signal Detect
14	**Receive Clock**
24	**Transmit Clock**
20	Data Terminal Ready

*Refer to CA631 for EIA/CCITT names.

Note: *The peer-to-peer version has shielding grounded at both connectors, whereas the terminal version has shielding grounded only at the 8100 connector.*





Plug PN 6835347
Plug Label H

Figure CA431-2. EIA Direct-Connect Cable (CAC5B) and Wrap Plug

CA432 DDS Cable (CAC7)

The DDS cable has a standard 25-pin female EIA connector on the 8100 end. The cable contains eight shielded wires and a covered switch assembly, and the Channel Service Unit Attachment end has a 15-pin, male connector (see Figure CA432-1).

The switch assembly has two positions — Test and Operate. The Operate position is for normal communication operations; the Test position provides wrap capability for problem determination by the customer and fault isolation by the Service Representative. Refer to Figure CA430-1 for cable alternative/options.

The Test position wraps the following lines:

- Data Tip 1 (3) to Data Tip (5)
- Data Ring 1 (4) to Data Ring (6)

The line wraps are isolated from the Channel Service Unit Attachment when in the **Test position.**

DDS cable pin assignments and line names follow:

Pin	Common Name*
1	Ground (not used by the 8100)
2	Status Indicate (not used by 8100)
3	DT1 (Data Tip 1)
4	DR1 (Data Ring 1)
5	DT (Data Tip)
6	DR (Data Ring)
7–15	Reserved

*Refer to CA631 for EIA/CCITT names.

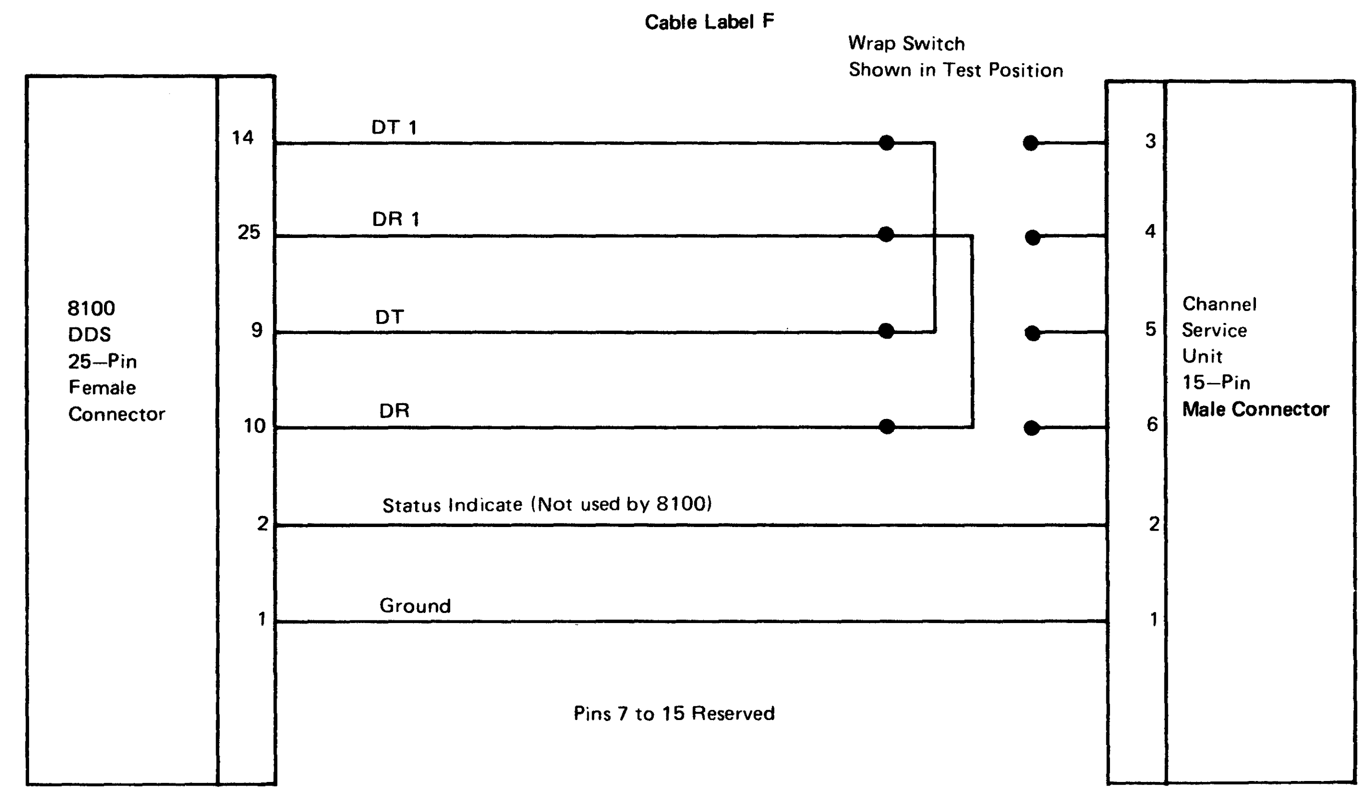


Figure CA432-1. DDS Cable (CAC7)

CA433 V.35 Cables

V.35 External Modem Cable (CAC6A)

The V.35 external modem cable has a standard 25-pin female EIA connector on the 8100 end. The cable contains 15 shielded wires, and the V.35 modem end is a 34-pin **male connector (Figure CA433-1).**

A wrap plug provides wrap capability for problem determination by the customer or fault isolation by the Service Representative (Figure CA433-1).

The wrap plug wraps the following lines:

- Request to Send (C) to Clear to Send (D) and Receive Line Signal Detect (F)
- Data Set Ready (E) to Data Terminal Ready (H)
- Transmit Data A (P) to Receive Data A (R)
- Transmit Data B (S) to Receive Data B (T)

V.35 external modem cable pin assignments and line names are as follows:

Pin	V.35 Pin	Common Name*
1	A	Protective Ground
2	P	Transmit Data A
3	R	Receive Data A
4	C	Request To Send
5	D	Clear to Send
6	E	Data Set Ready
7	B	Signal Ground
8	F	Receive Line Signal Detect
14	S	Transmit Data B
16	T	Receive Data B
17	V	Receive Clock A
18	X	Receive Clock B
20	H	Data Terminal Ready
24	Y	Transmit Clock A
25	a(AA)	Transmit Clock B

*Refer to CA631 for EIA/CCITT names.

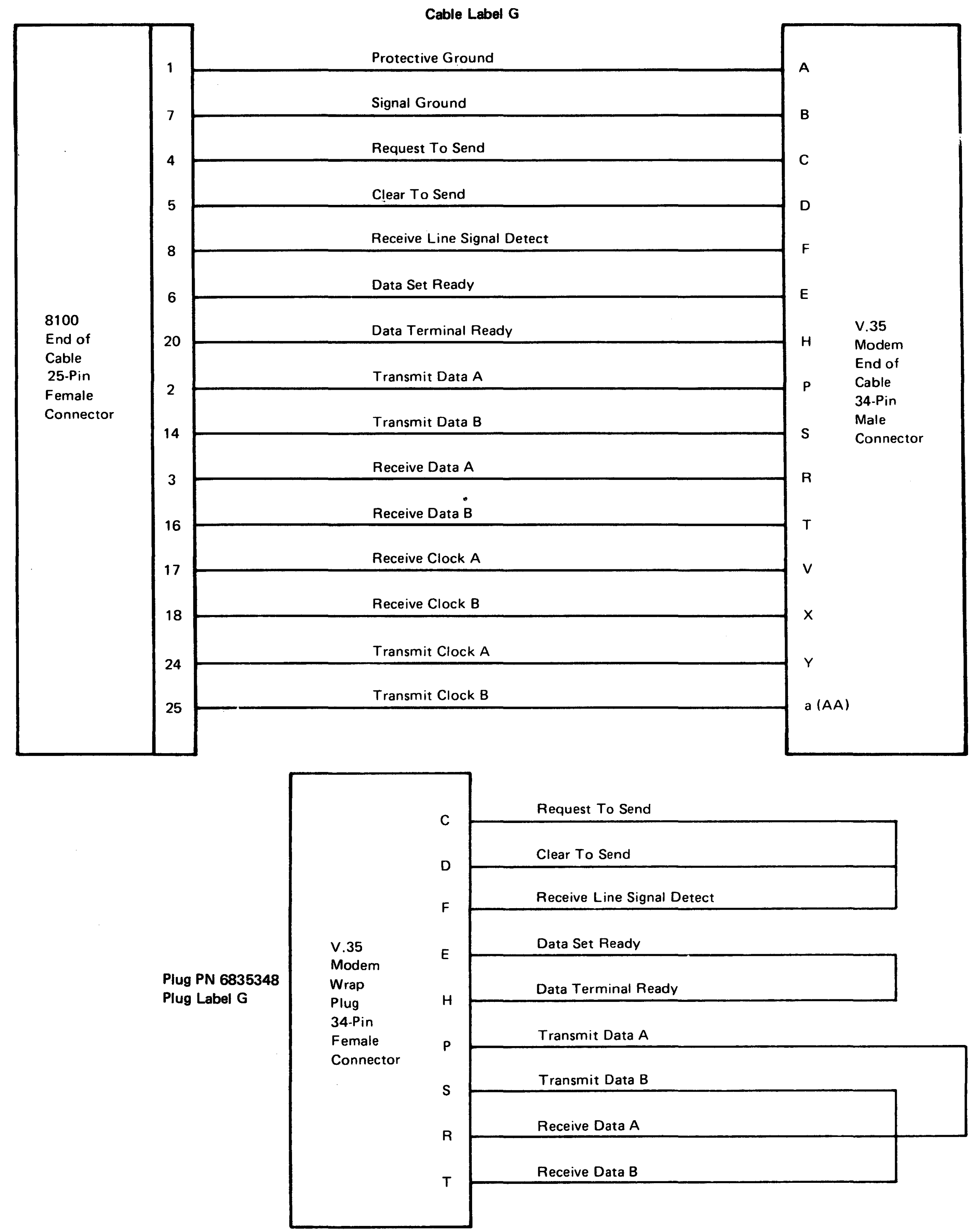


Figure CA433-1. V.35 External Modem Cable (CAC6A) and Wrap Plug

V.35 – Direct-Connect Terminal Cable (CAC6B)

The V.35 direct-connect terminal cable has a standard 25-pin female EIA connector on the 8100 end. The cable contains 15 shielded wires, and the V.35 direct-connect attachment end has a 34-pin female connector **(Figure CA433-2).**

A wrap plug provides wrap capability for problem determination by the customer or fault isolation by the Service Representative (Figure CA433-2).

The wrap plug wraps the following lines:

- Transmit Data A (P) to Receive Data A (R)
- Transmit Data B (S) to Receive Data B (T)

The following are internal line wraps:

The 8100 connector end:

- Data Terminal Ready (20) to Data Set Ready (6)
- Request to Send (4) to Clear to Send (5) and Receive Line Signal Detect (8)

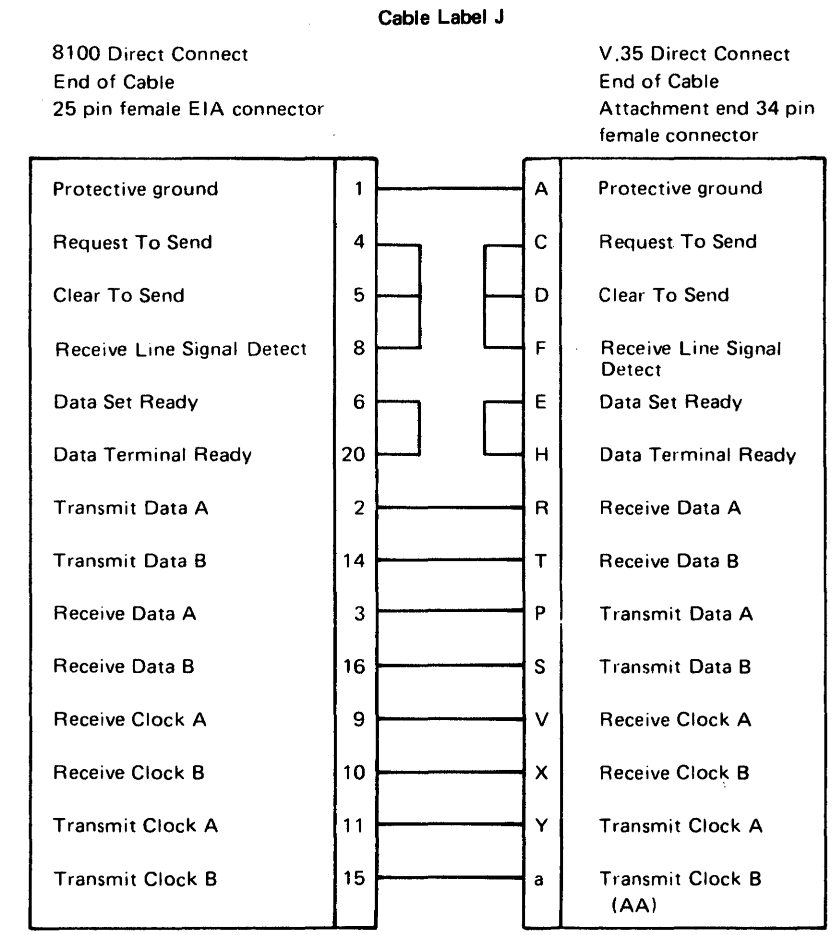
The V.35 direct-connect attachment end:

- Data Terminal Ready (H) to Data Set Ready (E)
- Request to Send (C) to Clear to Send (D) and Receive Line Signal Detect (F)

V.35 direct-connect cable pin assignments and line names are as follows:

EIA Pin	V.35 Pin	Common Name*
1	A	Protective Ground
2	R	Transmit Data A
3	P	Receive Data A
4	C	Request To Send
5	D	Clear To Send
6	E	Data Set Ready
8	F	Receive Line Signal Detect
9	V	Receive Clock A
10	X	Receive Clock B
11	Y	Transmit Clock A
14	T	Transmit Data B
15	a(AA)	Transmit Clock B
16	S	Receive Data B
20	H	Data Terminal Ready

*Refer to CA631 for EIA/CCITT names.



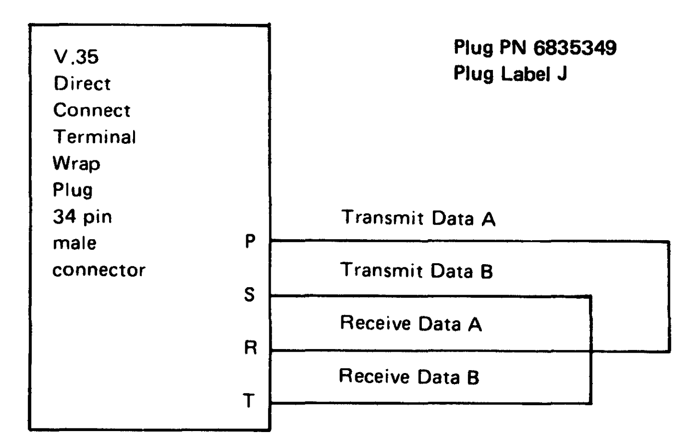


Figure CA433-2. V.35 Direct-Connect Terminal Cable (CAC6B) and Wrap Plug

V.35 — Direct-Connect Peer-to-Peer Cable (CAC6B)

The V.35 direct-connect peer-to-peer cable has a standard 25-pin female EIA connector on the 8100 end. The cable contains 15 shielded wires, and the V.35 direct-connect attachment end has a 25-pin EIA female connector **(Figure CA433-3)**.

A wrap plug provides wrap capability for problem determination by the customer or fault isolation by the Service Representative (Figure CA433-3).

The wrap plug wraps the following lines:

- Transmit Data A (2) to Receive Data A (3)
- Transmit Data B (14) to Receive Data B (16)

The following are internal line wraps:

The 8100 connector end:

- Data Terminal Ready (20) to Data Set Ready (6)
- Request to Send (4) to Clear to Send (5) and Receive Line Signal Detect (8)

The V.35 direct-connect attachment end:

- Data Terminal Ready (20) to Data Set Ready (6)
- Request to Send (4) to Clear to Send (5) and Receive Line Signal Detect (8)

V.35 direct-connect peer-to-peer cable pin assignments and line names follow:

EIA Pin	Common Name*
1	Protective Ground
2	Transmit Data A
3	Receive Data A
4	Request To Send
5	Clear To Send
6	Data Set Ready
8	Receive Line Signal Detect
9	Receive Clock A
10	Receive Clock B
11	Transmit Clock A
14	Transmit Data B
15	Transmit Clock B
16	Receive Data B
20	Data Terminal Ready

*Refer to CA631 for EIA/CCITT names.

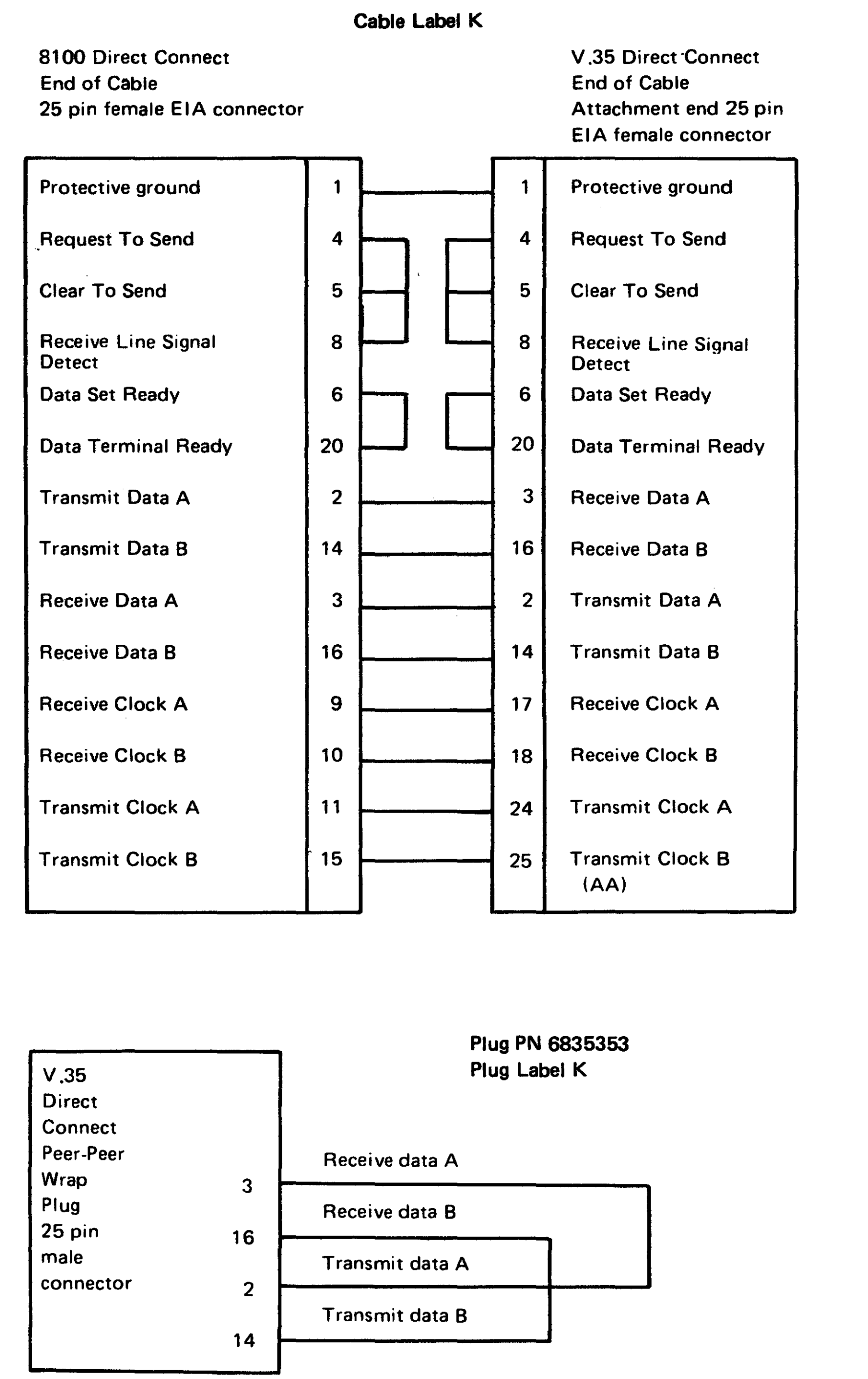


Figure CA433-3. V.35 Direct Connect Peer-to-Peer Cable (CAC6B) and Wrap Plug

CA434 Integrated Modem Cables

Integrated Modem (Nonswitched Line) Cable (CAC8)

The integrated modem (nonswitched) cable has a standard 25-pin female EIA connector on the 8100 end. The cable contains five wires, and the remote end (nonswitched or Type CDT Data Coupler) has either a telephone connecting block or spade terminals on the wire ends (Figure CA434-1).

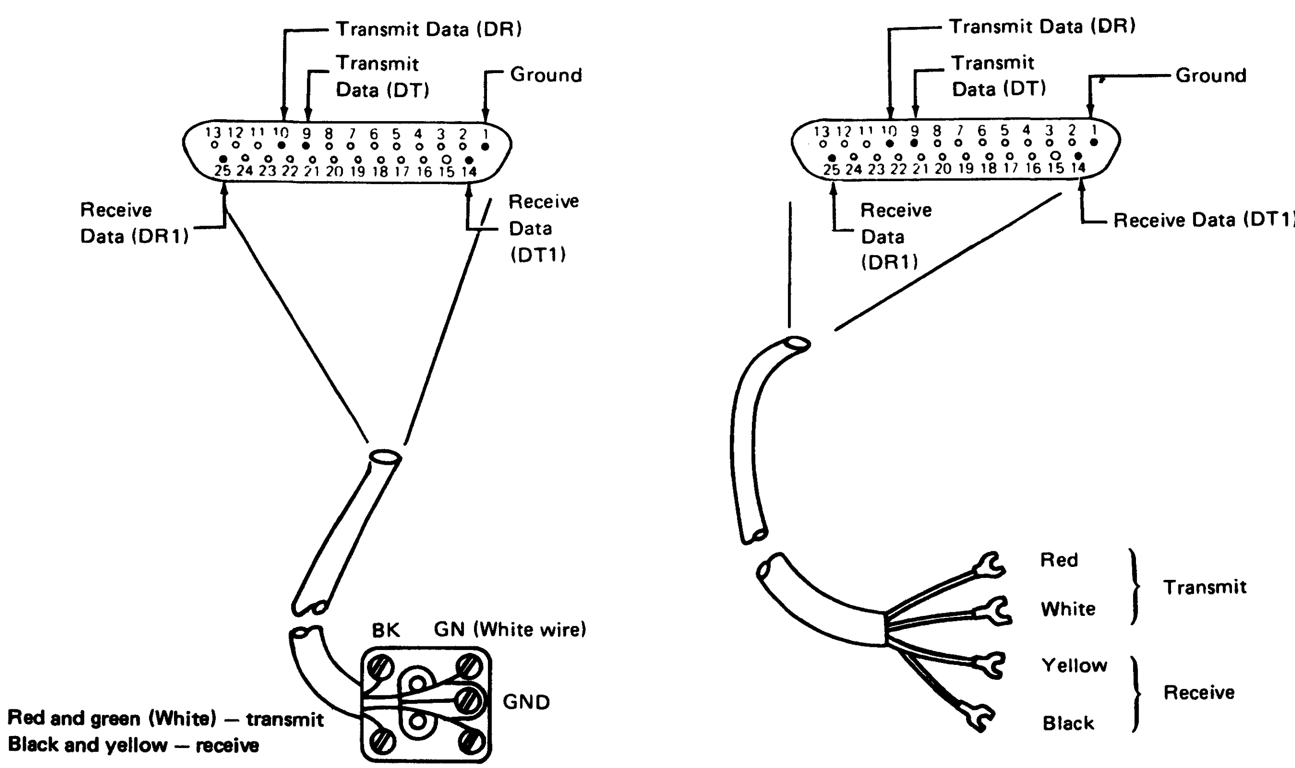
There is no cable wrap capability for this cable. The cable may be tested by continuity checking between the wire end and the appropriate pin in the cable connector.

Integrated modem (nonswitched) cable pin assignments and line names follow:

EIA Pin	Common Name*	Wire Color
1	Protective Ground (Connector block only)	–
9	Transmit Data (DT)	White
10	Transmit Data (DR)	Red
14	Receive Data (DT1)	Black
25	Receive Data (DR1)	Yellow

*Refer to CA631 for EIA/CCITT names.

For cable label, see CA430.



U.S.A. and Canada

Countries Other Than U.S.A. and Canada

Figure CA434-1. Integrated Modem (Nonswitched Line) Cable (CAC8)

Integrated Modem (Switched Line) Cable (CAC9)

The integrated modem (switched line) cable has a standard 25-pin female EIA connector on the 8100 end. The cable contains eight wires, and the remote end (Type CBS Data Access Arrangement or equivalent) has spade terminals on the wire ends (Figure CA434-2).

There is no cable wrap capability for this cable. The cable may be tested by continuity checking between the wire end and the appropriate pin in the cable connector.

Integrated modem (switched line) cable pin assignments and line names follow:

EIA Pin	Common Name*	Wire Color
20	Coupler Cut-Through (CCT)	Brown
4	Switch Hook (SH)	Red
5	Ring Indicate (RI)	Violet
6	Data Modem Ready (DA)	Yellow
7	Signal Ground (SG)	Gray
22	Off Hook (OH)	Blue
3	Data Tip (DT)	White
2	Data Ring (DR)	Black

*Refer to CA631 for EIA/CCITT names.

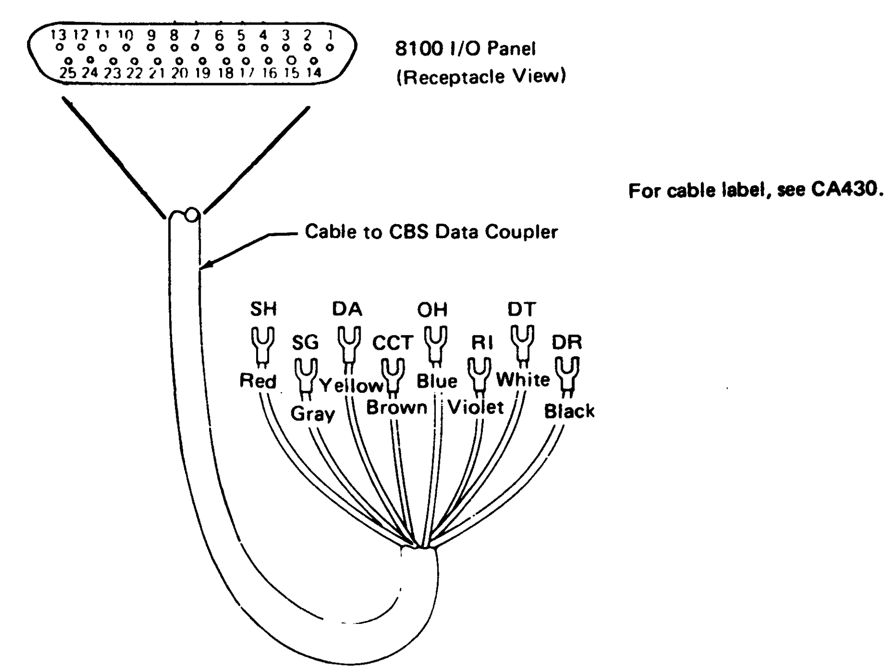


Figure CA434-2. Integrated Modem (Switched Line) Cable (CAC9)

CA435 Loop Cable (CAC3 and CAC4)

The loop cable has a standard 25-pin female EIA connector on the 8100 end. The cable contains seven wires plus a shield wire and, and 8-pin right-angle loop station connector (LSC) on the loop attachment end **(Figure CA435-1).**

The cable may be tested by connecting the cable to either the customer's loop or to the loop test tool, PN 1657410, and running Routine 51 for a one-lobe loop, or Routine 52 for a two-lobe loop. These routines are run under MAP control if the link/loop tests **are selected.**

Figure CA435-2 shows the loop wrap plug which is used only at CSU time.

Loop cable pin assignments and line names follow:

EIA Pin	LSC Pin	Common Name*	Wire Color
1	**	Shield	Shield
10	2	D— (Minus Transmit Data)	Red
9	3	D+ (Plus Transmit Data)	White
25	4	R— (Minus Receive Data)	Orange
14	5	R+ (Plus Receive Data)	Blue
21	6	Pick R1 (Relay 1)	Yellow
24	7	Pick R2 (Relay 2)	Purple
7	8	Relay Common	Black

*Refer to CA631 for EIA/CCITT names.
**No connection.

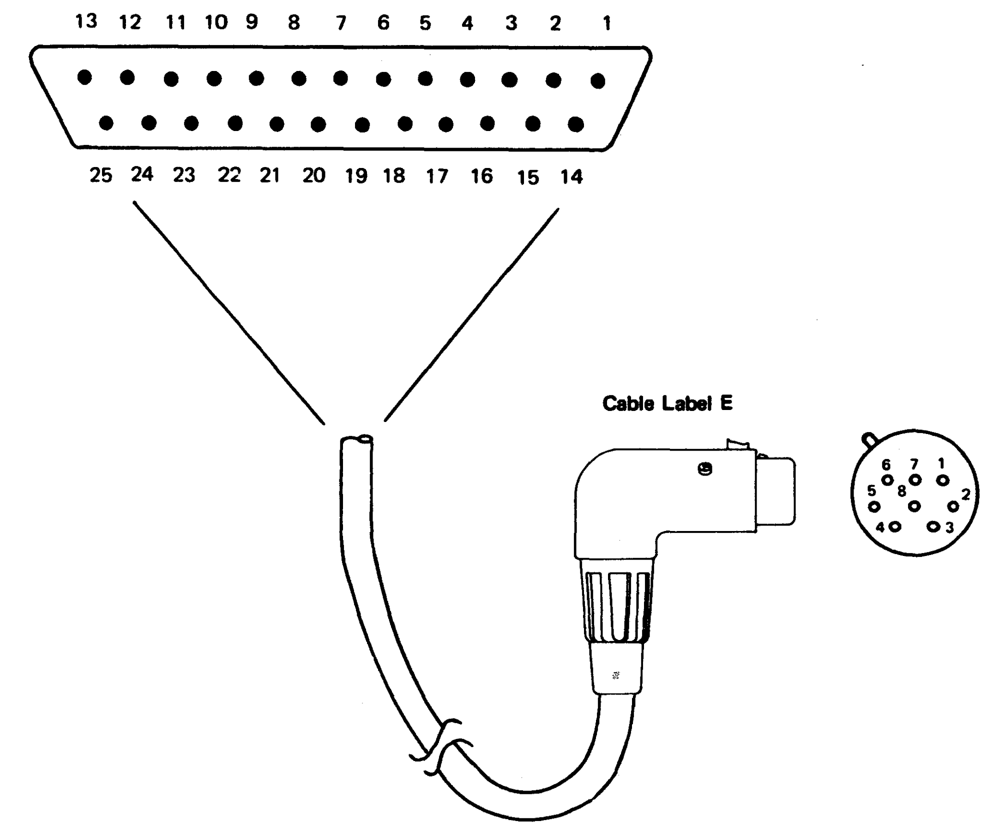
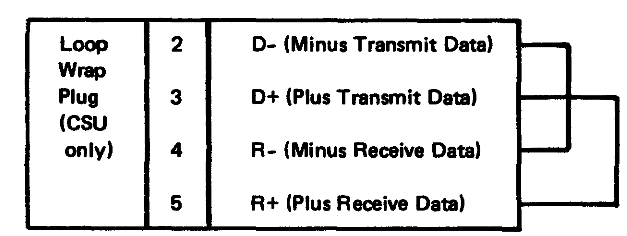


Figure CA435-1. Loop Cable (CAC3 and CAC4)



Plug PN 7389282
Plug Label E

Figure CA435-2. Loop Wrap Plug (CSU only)

CA436 X.21 (Nonswitched) Cable (CAC11)

The X.21 cable has a standard 25-pin female connector on the 8100 end. The cable contains six pairs of shielded wires and a covered switch assembly, and the DCE Attachment end has a 15-pin, male connector (see Figure CA436-1).

The switch assembly has two positions – Test and Operate. The Operate position is for normal communication operations; the Test position provides wrap capability for problem determination by the customer and fault isolation by the Service Representative. Refer to Figure CA430-1 for cable alternative/options.

The Test position wraps the following lines:

- Transmit A (2) to Receive A (3)
- Transmit B (14) to Receive B (16)
- Control A (10) to Indication A (17)
- Control B (9) to Indication B (18)

The lines wraps are isolated from the DCE Attachment when in the Test position.

X.21 cable pin assignments and line names follow:

8100 Pin	DCE Pin	Common Name*
18	12	Indication B
9	10	Control B
3	4	Receive A
14	9	Transmit B
25	13	Signal Element Timing B
7	8	Signal Ground
10	3	Control A
17	5	Indication A
16	11	Receive B
2	2	Transmit A
24	6	Signal Element Timing A

*Refer to CA631 for EIA/CCITT names.

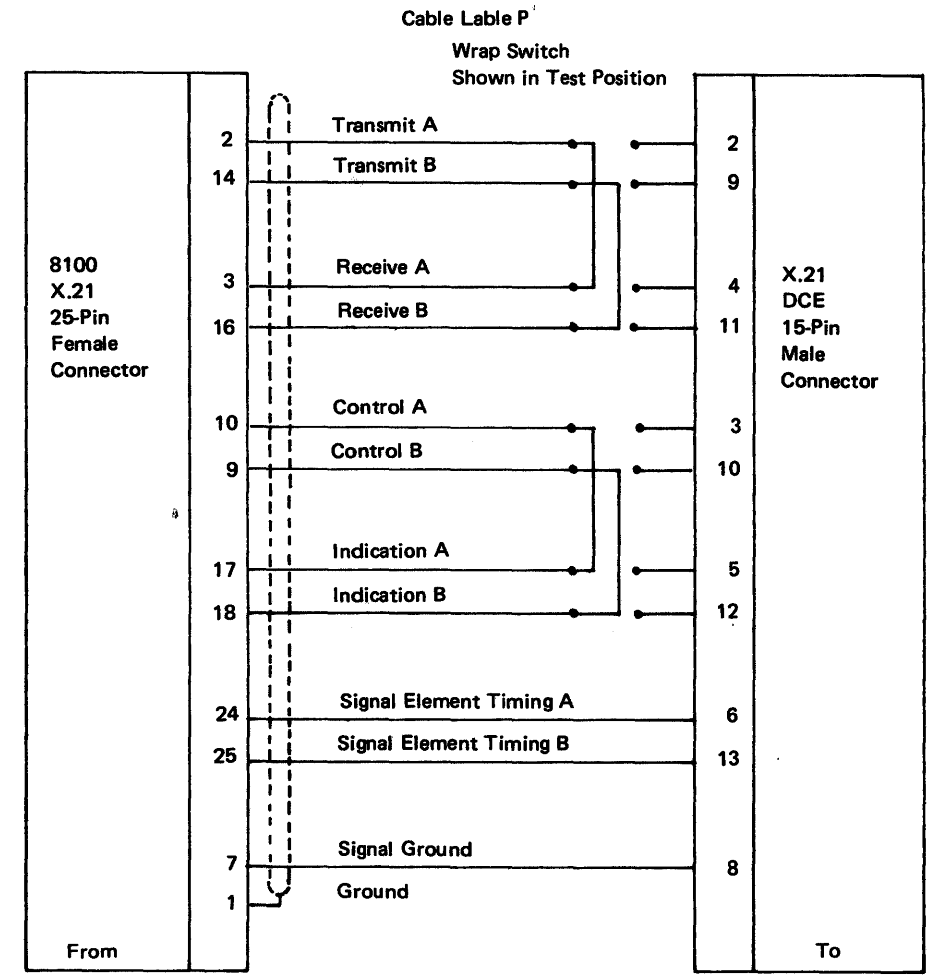


Figure CA436-1. X.21 (Nonswitched) Cable (CAC11)

CA450 Detailed Data Flow

This section describes the major functions of each card; shows all adapter/device cards; and lists I/O pins, signal names, and from/to point designations when multiple FRUs are involved.

CA451 SDLC Adapter Card (CA1)

The SDLC adapter card connects to the 8100 Information System through the I/O bus. The primary purpose of this adapter card, in conjunction with an appropriate program package, is to provide communications with a variety of DCE configurations.

This adapter card performs the general functions common to eight-bit SDLC protocol, and connects to common-carrier lines or the loops. The card has two data buses: the I/O data bus and the DCE data bus (Figure CA451-1). The I/O data bus connects the adapter card to the 8100 system controller through the I/O bus (IOBO/IOBI). The DCE data bus connects the adapter card to the DCE through the appropriate board wiring and/or system cables. In addition, the hardware has personalization lines which are selectively grounded or connected to one another for address decoding.

Basic Data Flow

There are two basic and independent hardware data flow paths: one path transmits byte information and the other path receives byte information.

Transmit Data Flow. The transmit data flow path uses a one-byte buffer, a serializer (a shift register and associated controls), a BCC accumulation shift register and associated controls, and special circuits for manipulation of the serial bit stream for transmitting SDLC information.

The output of the serializer is from the transmit data line of the DCE interface to the connected DCE. The first data bit sent over the transmit data line must be written in the low-order (bit 7) position of the TX data register, and the last data bit in the high-order position (bit 0).

Transmit CHIO Operation. When running in CHIO mode, the SDLC adapter card moves long chains of data (when the processor grants permission), and uses only one interrupt request. The transmitted message in CHIO mode consists of leading pads, two messages, and fast turnaround to drop transmit mode and turn on receive mode.

Receive Data Flow. The receive data path uses a deserializer, a one-byte buffer, and the FCS (and associated controls). The deserializer and FCS (and associated controls) load the bits serially as they are sampled from the receive data line of the DCE interface.

When the deserializer contains a complete byte, it transfers the byte to the receive buffer, where it is held without further manipulation. At 7D time of a read data cycle, it transfers the byte (either by a PIO or CHIO command) to the adapter card program through the I/O interface input data bus. The high-order position (bit 0) contains the first data bit received.

DCE Lines

The SDLC adapter conforms with the functional definition of the lines as given in EIA standard RS-232-C, CCITT recommendation V.24, V.35, X.21 (nonswitched) and functional specifications for the loop adapter. The SDLC adapter card also communicates with the digital data service (DDS) card at speeds of from 2400 bps to 56K bps. The 8130 and attached 8101s can operate only up to 9600 bps with the DDS.

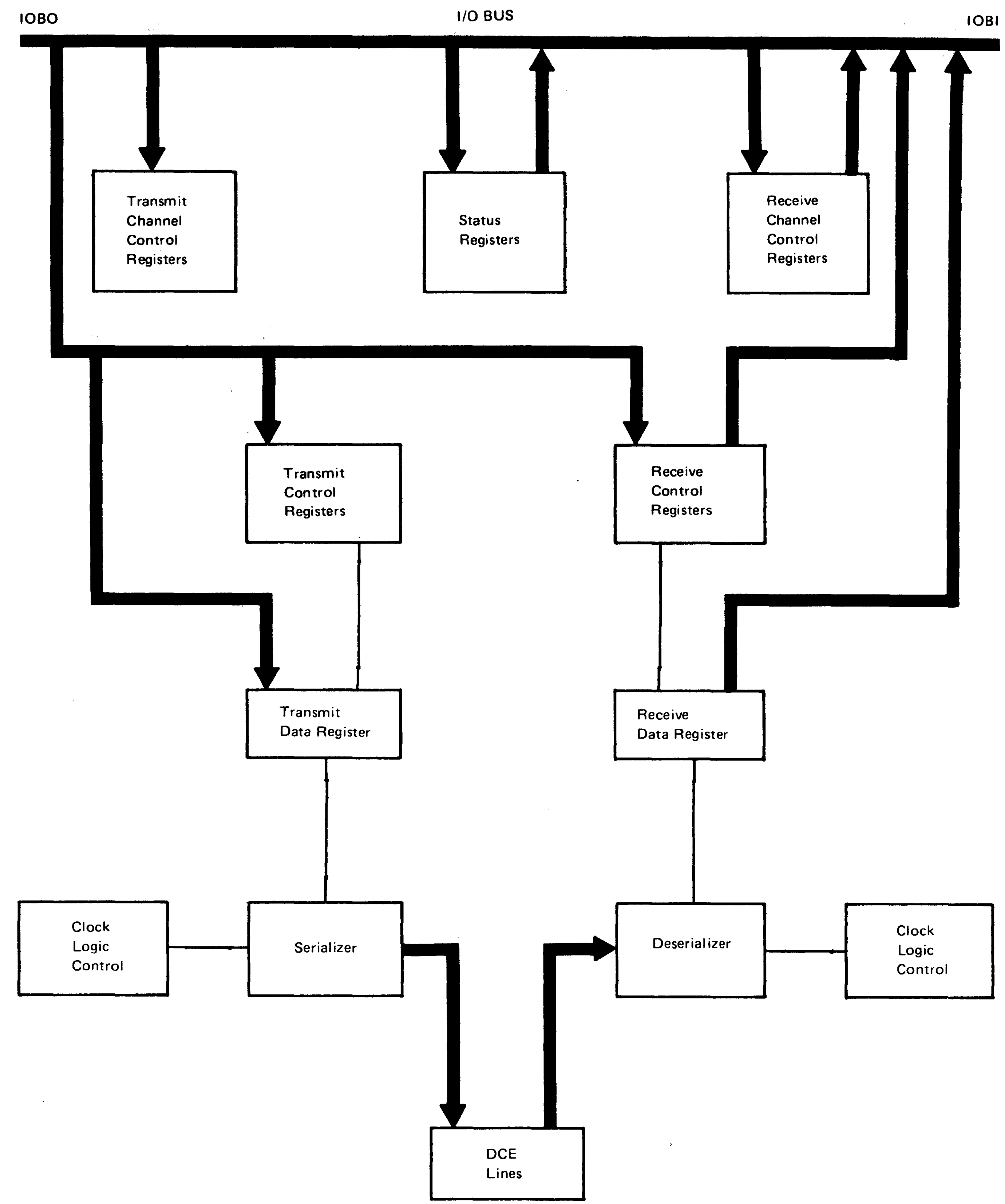


Figure CA451-1. SDLC Adapter Card (CA1) Data Flow

CA455 BSC/S-S Adapter Card (CA2)

The BSC/S-S adapter card connects to the 8100 System identically as does the SDLC adapter card. The BSC/S-S adapter card has the same function as the SDLC adapter card, but it does not operate in CHIO mode. It is a byte adapter card, and operates using bisynchronous and start/stop disciplines. The adapter card interfaces are also identical, and address decode personalization operates similarly to the SDLC adapter card.

Basic Data Flow

There are two separate and independent hardware data flow paths. One path transmits byte information and the other receives byte information (Figure CA-455-1).

Transmit Data Flow. The transmit data flow uses a one-byte buffer, a serializer (a shift register and associated controls), and special circuits for adding start and stop bits (asynchronous operation). The serializer outputs information through the send data lead of the adapter card DS interface to the connected DCE.

Receive Data Flow. The receive data flow path uses only a deserializer and a one-byte buffer. The deserializer (a shift register and associated controls) loads serially as the bits are sampled from the receive data lead of the adapter card DS interface. When the deserializer contains one byte, it transfers the byte to the receive buffer, where it is held without further manipulation. At 7D time of a read data cycle, the byte is transferred to the adapter card program through the I/O data bus.

DCE Lines

The BSC/S-S adapter card conforms with the functional definition of the lines as given in EIA Standard RS232-C, CCITT recommendation V.24. The BSC/S-S adapter card does not operate with the loop card. It also communicates with the digital data service card at speeds from 2400 bps to 9600 bps.

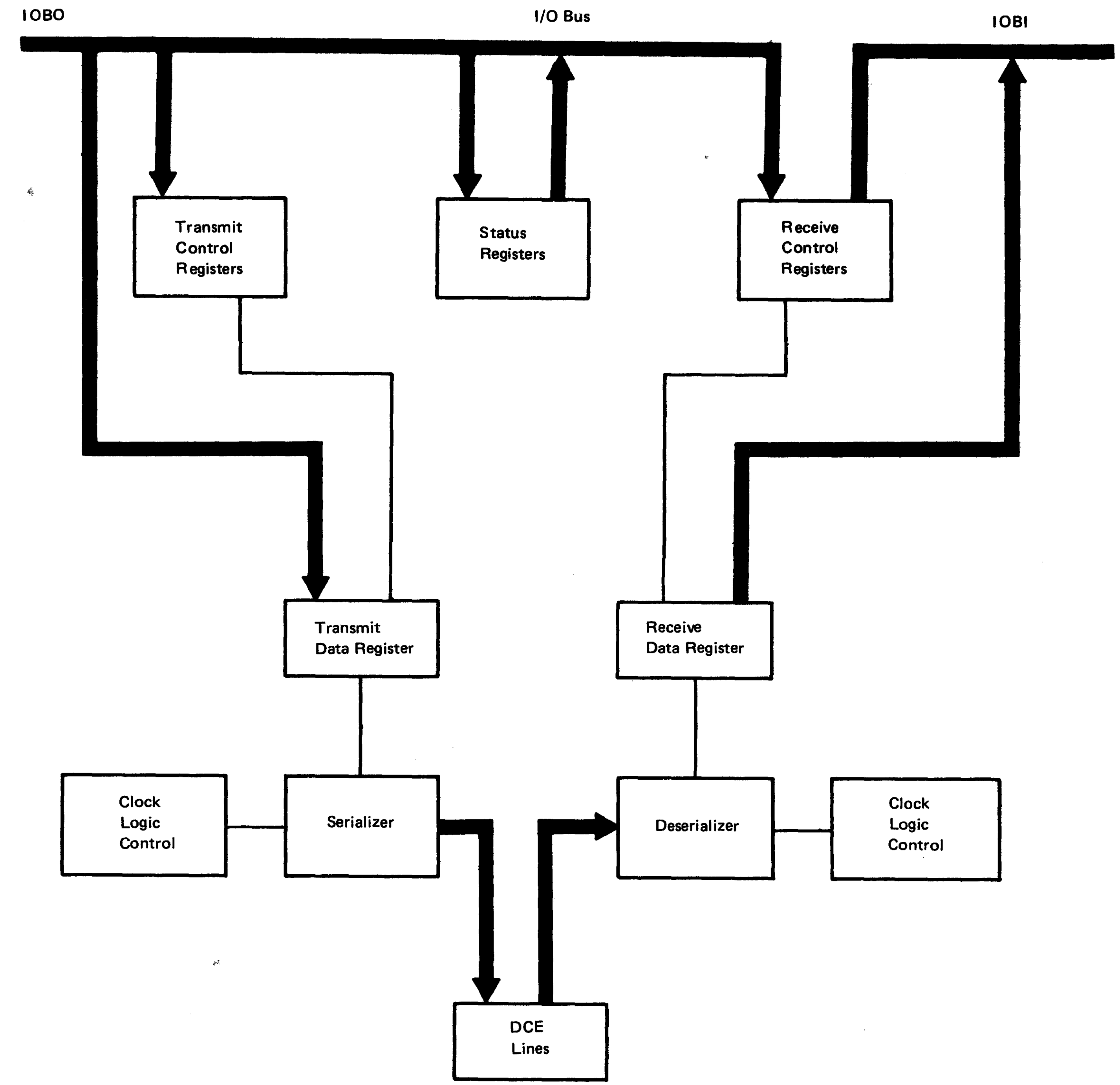


Figure CA455-1. BSC/S-S Adapter Card (CA2) Data Flow

CA470 Driver Cards

CA471 Digital Data Service (DDS) Card (CA7)

The digital data service (DDS) card (Figure CA471-1) is an integrated adapter designed specifically to permit IBM machines to interface to AT&T's nonswitched Dataphone* digital data service through an AT&T Channel Service Unit.

It is a 4-wire duplex adapter that derives power from the 8100. The DDS card handles data serially-by-bit and by character, and operates in synchronization with the communication line signal. It also provides a clock for data transmission, and operates at synchronous speeds of 2.4, 4.8, 9.6 and 56K bps. The maximum speed for the 8130 and attached 8101s is 9600 bps.

The DDS uses a baseband bi-polar return to zero signalling method for transmission over a local loop (from central office to customer location), a binary "0" transmits as a nominal 50-percent duty cycle pulse, either positively or negatively, and is opposite in polarity to the preceding binary "1". The DDS provides transmit and receive clock signals to the 8100. The communication line signal synchronizes the clock pulses, and therefore must be present at all times on the receive input line. The clock is always available, but is synchronized only when the DDS is connected to the network. Line control is accomplished by use of violation characters (bit patterns in which the opposite polarity rule is violated).

*Trademark of American Telephone & Telegraph Co. (AT&T)

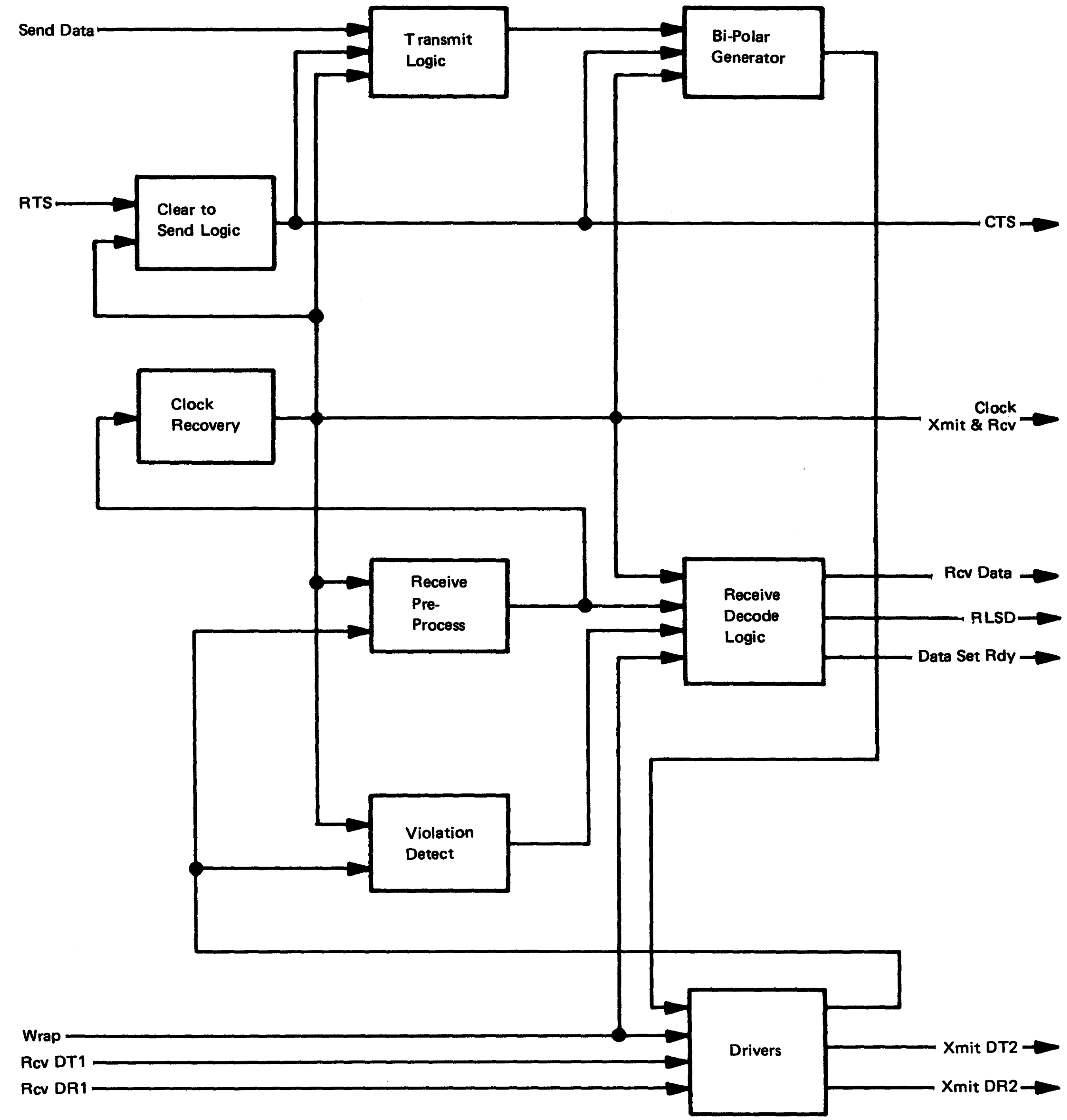


Figure CA471-1. Digital Data Service Card (CA7) Data Flow

CA472 EIA/CCITT Card (CA5)

The EIA/CCITT card (Figure CA472-1) converts signal levels between VTL and the RS232C and CCITT V.28 recommendation from 0 to 9600 bps. The card also conforms to RS334 specifications. It provides eight VTL-to-EIA/CCITT level drivers and eight EIA/CCITT-to-VTL level receivers.

The card supplies eight driver lines which convert and invert the applied signals. Sense of the VTL input interface to the DTE is an active down-level. Sense of the output interface lines (to the DCE) is an active up-level according to the EIA standard RS232C and CCITT V.28 recommendation.

Two of the drivers (input pins B02 and D02) have anti-glitch protection which forces the output of the drivers to the zero-volt level during power-up or power-down condition. These same drivers use 2700-pf capacitors to ground the output so that stray signals are shunted to ground during card power-off conditions.

The card also supplies eight receiver lines which convert and invert the signals from the DCE. Sense of the received signal (EIA side) is an active up-level according to RS232C and CCITT V.24/V.28 recommendations. Sense of the VTL output (DTE interface) is an active down-level.

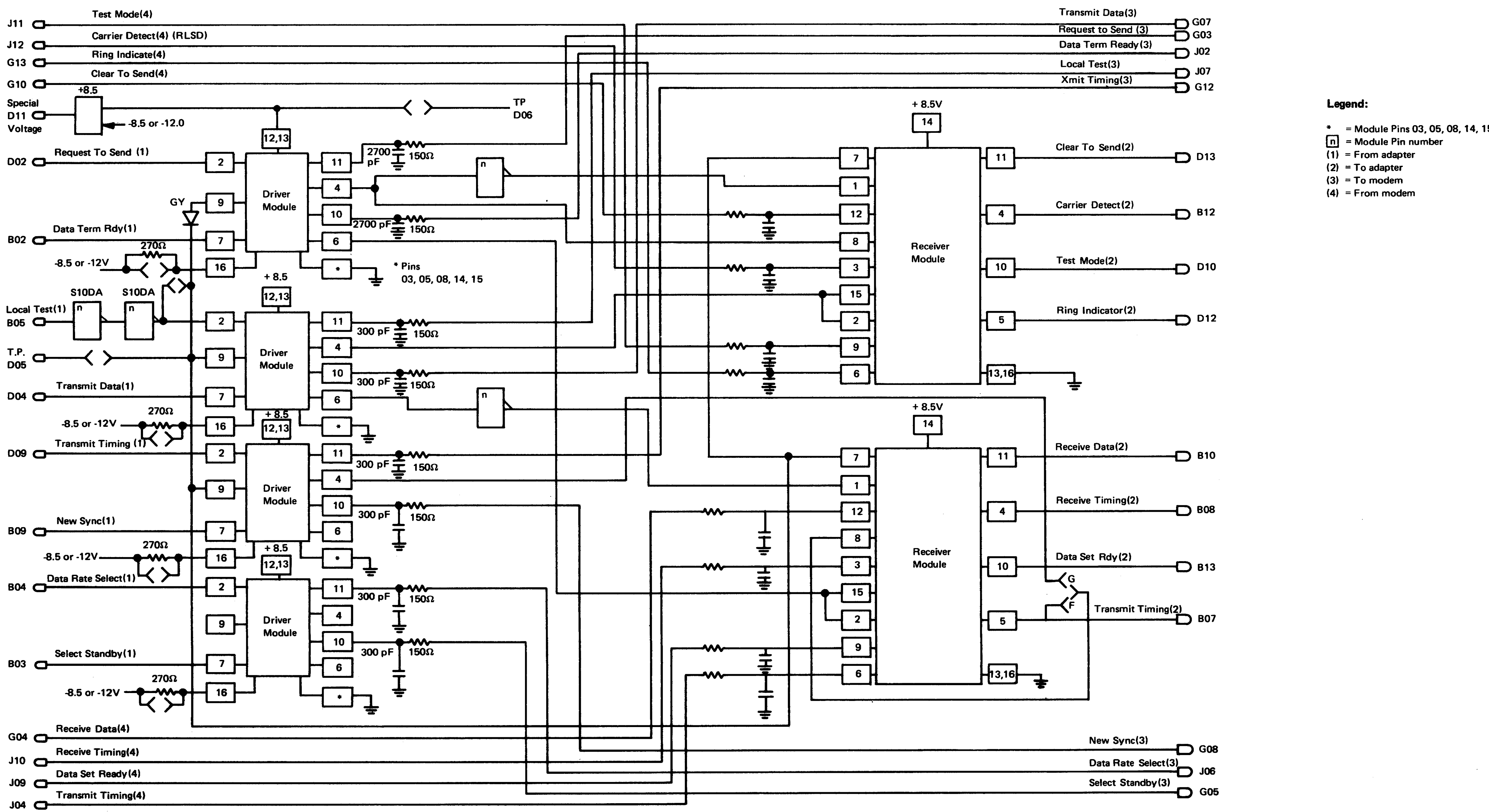


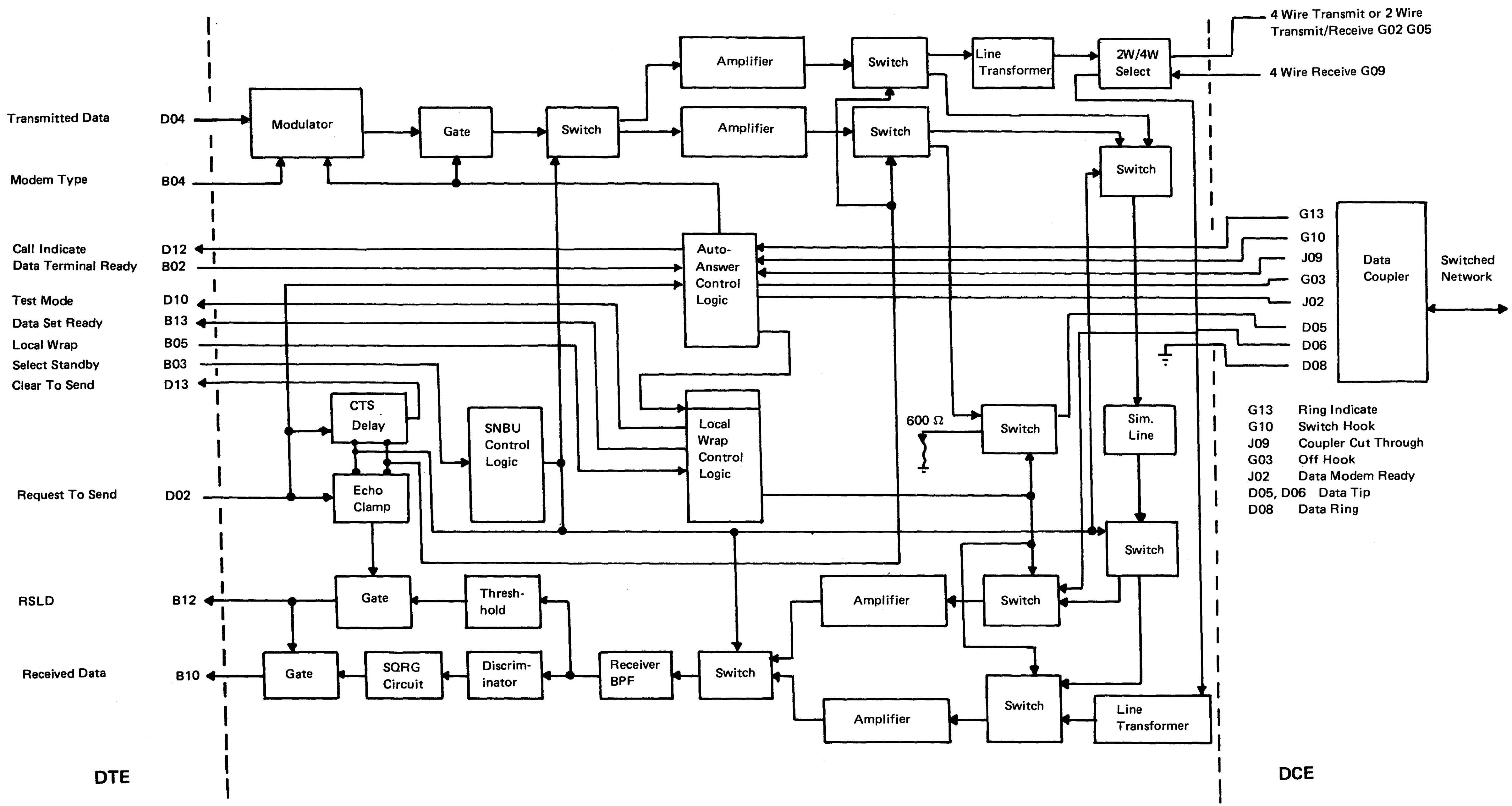
Figure CA472-1. EIA/CCITT Card (CA5) Schematic

CA473 Integrated Modem Card (CA8/CA9)

The integrated modem (Figure CA473-1) is a frequency-shift keying (FSK) modem designed specifically for under-the-cover implementation. It operates on WTC and U.S. leased and switched facilities, and conforms to CCITT recommendation V.23 for operation at 1200 bps.

The modem converts a two-level business machine signal into a frequency-modulated carrier for transmission over a voice-grade telephone channel. Information transfer occurs serially-by-bit and by characters. The send data interface lead and the line signal do not maintain information synchronization.

The host system can test the modem data channel by performing a test command and then transmitting test patterns. The auto-answer function provides self-testing when in the switched network mode. This is done by simulating the interface signals from a CBS coupler or the World Trade line plate to sequence through an auto-answer. The test circuitry attenuates the transmit signal, adds random noise to it, and sends it back through its receive channel for comparison with the transmitted data.



G13	Ring Indicate
G10	Switch Hook
J09	Coupler Cut Through
G03	Off Hook
J02	Data Modem Ready
D05, D06	Data Tip
D08	Data Ring

Figure CA473-1. Integrated Modem Card (CA8/CA9) Schematic

CA474 V.35 Card (CA6)

The V.35 card (Figure CA474-1) converts signal levels between the adapter VTL interface and the CCITT V.35 interface. It contains discrete components and three different analog modules: (1) EIA driver modules, (2) EIA receiver modules, and (3) V.35 driver/receiver modules.

Each EIA driver module contains two driver circuits which operate from VTL levels on the logic side to V.35 levels on the interface side. The driver persents a 300-ohm or greater source impedance to the line.

Each EIA receiver module contains four receiver circuits which derive their voltages from the interface lines and provide VTL level signals to the logic side. The receivers also operate in a fail-safe manner. A positive signal shift does not turn on the receiver until it reaches +2.0V nominally, and turns off when the signal falls to +1.0V nominally. The receiver indicates an off condition with its input floating.

Direct connect applications support data transfer rates from 600 bps to 56K bps, and also support rates from 19.2K bps to 56K bps when attaching to signal converters. The maximum speed for the 8130 and attached 8101s is 9600 bps.

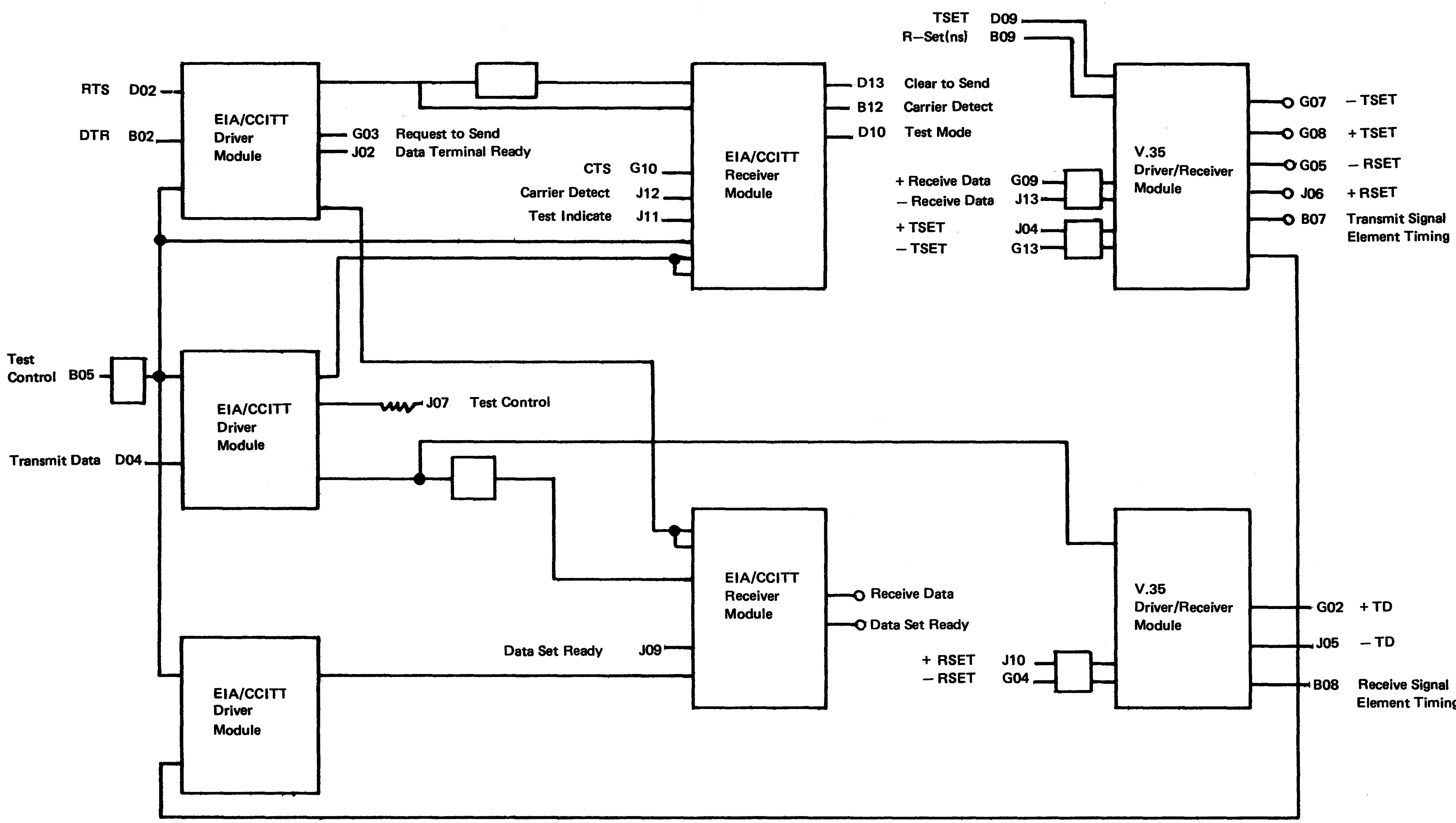


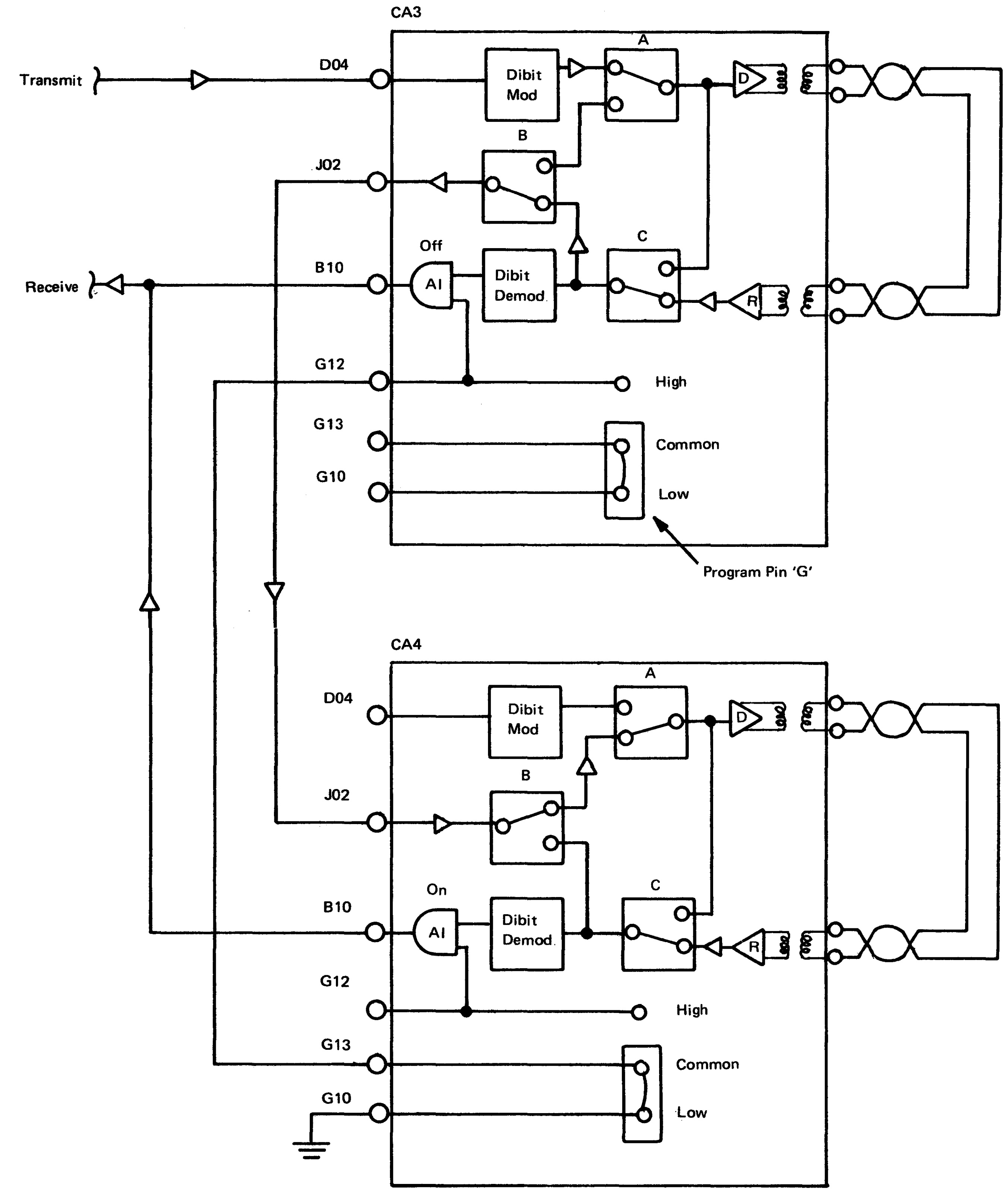
Figure CA474-1. V.35 Card (CA6) Schematic

CA475 Loop Card (CA3/CA4)

The loop card communicates between the SDLC and the loop wire. Up to two loop cards can be connected to one SDLC card, thus dividing the signal path into two separate portions called lobes. See Figure CA475-1 for the two-lobe signal path and Figure CA475-2 for loop wire states.

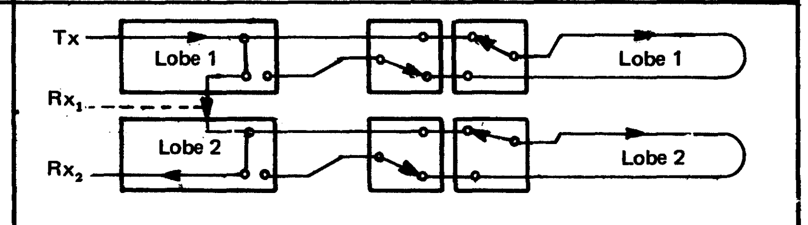
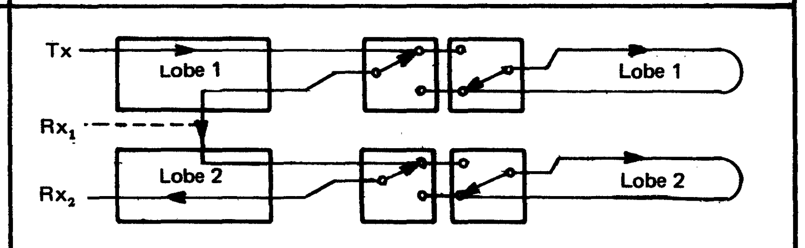
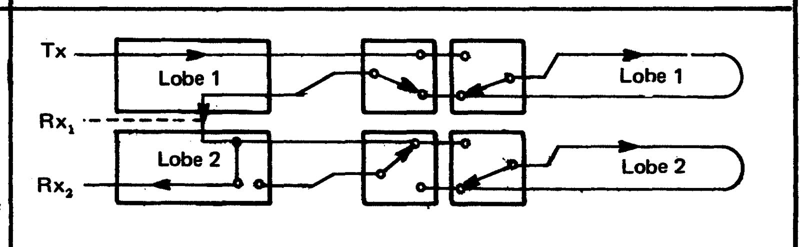
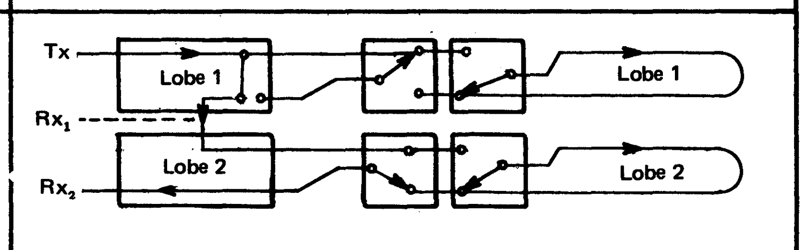
The loop card converts the SDLC adapter card VTL levels to special binary loop signals which it presents to the loop wire. The loop card provides the voltage necessary to pick the LSC (loop station connector) relays, and can be programmed for various signal path configurations for problem determination and error recovery. The loop card can operate at three different carrier rates (9.6K bps, 19.2K bps and 38.4K bps), and each carrier rate can have four different data rates and half-speed functions:

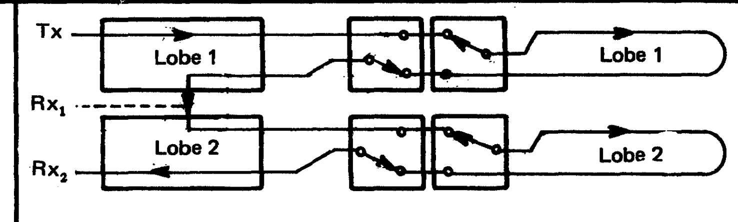
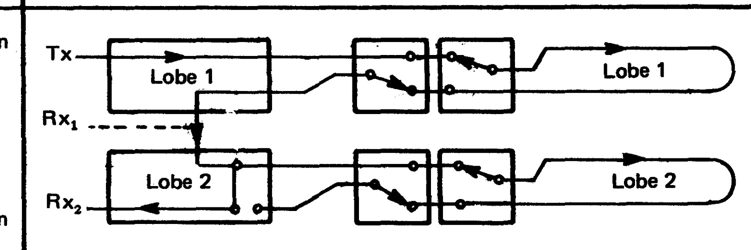
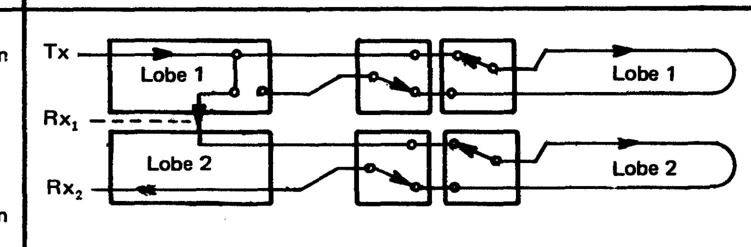
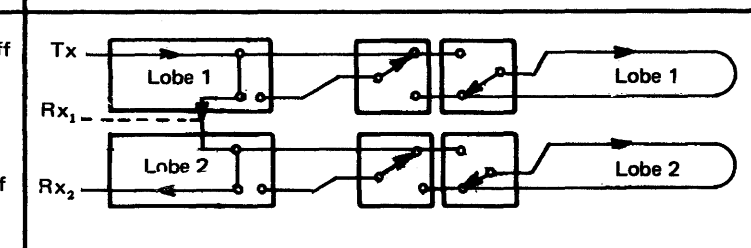
- If the carrier rate is 9.6K bps, the data rate can be from 600 bps to 9.6K bps.
- If the carrier rate is 19.2K bps, the data rate can be from 1.2K bps to 19.2K bps.
- If the carrier rate is 38.4K bps, the data rate can be from 2.4K bps to 38.4K bps.



Note: *Switches A and B are controlled by G10 (Lobe 2 Control). Switch C is controlled by external wrap. (All switches are logical gates; not contact switches.)*

Figure CA475-1. Loop Two-Lobe Signal Path (CA3/CA4)

Loop Wrap State	Control Lines LTST	DRS	NS	LSC Relay R1	R2	Loop Cards / LSC Relay R1 R2 / Loop
Lobe 1 — Internal Active Lobe 2 — Internal Active	I	I	I	On On	On On	
Lobe 1 — External Wrap Lobe 2 — External Wrap	A	A	A	Off Off	Off Off	
Lobe 1 — Open Lobe 2 — Internal Wrap	A	A	I	On Off	Off Off	
Lobe 1 — Internal Wrap Lobe 2 — Open	A	I	A	Off On	Off Off	

Loop Wrap State	Control Lines LTST	DRS	NS	LSC Relay R1	R2	Loop Cards / LSC Relay R1 R2 / Loop
Lobe 1 — Normal Lobe 2 — Normal	I	A	A	On On	On On	
Lobe 1 — Normal Lobe 2 — Internal Active	I	A	I	On On	On On	
Lobe 1 — Internal Active Lobe 2 — Normal	I	I	A	On On	On On	
Lobe 1 — Internal Wrap Lobe 2 — Internal Wrap	A	I	I	Off Off	Off Off	

Legend:

A = 0 to + 0.6 volts
I = + 2.4 to + 5.5 volts

Rx_1 = Receive Data if one-lobe loop
Rx_2 = Receive Data if two-lobe loop
Tx = Transmit Data
LTST = Local Test
DRS = Data Rate Select
NS = New Sync

Note: *Data path from loop card around loop and back to loop card is twisted pair represented by one line on diagrams.*

Loop Wrap State Definitions

External Wrap — Data goes through loop card and is wrapped at LSC.

Internal Active — Data is wrapped at loop card; also, data goes around lobe but data from lobe is not received.

Internal Wrap — Data is wrapped at loop card; data does not go around loop.

Normal — Normal state; data goes through loop card and around lobe.

Open — Data goes through loop card but does not get to lobe; lobe data path is open; no data is received.

Figure CA475-2. Loop Wire States

CA476 Multispeed Clock Card (CA10)

The multispeed clock card (Figure CA476-1) provides a clock source (LF1, 2, 3, 4) to clock data in and out of up to four communications features. The clock card also provides a 64 x LF clock source to clock data in and out of up to four communications adapters.

Selection of a particular clock frequency (LF or 64 x LF) to any of the eight tab pins requires jumpers and switches. FAC codes specified by the customer determine the jumper and switch settings. See CA563 for multispeed clock card layout and jumper settings.

The clock card pin assignments and names follow:

Pin	Name
B06	Reserved for –5V dc
B11	Reserved for +8.5V dc
D03	+5V dc
D05	–LF 1 Driver
D06	–LF 2 Driver
D07	Reserved for –8.5V dc
D08	Ground
D09	–LF 3 Driver
D10	–LF 4 Driver
D12	–64 x LF 3 Driver
G05	–64 x LF 2 Driver
G06	Reserved for –5V dc
G11	Reserved for +8.5V dc
J03	+5V dc
J04	–64 x LF 1 Driver
J08	Ground
J09	–64 x LF 4 Driver

Note: *Those pins not listed are reserved.*

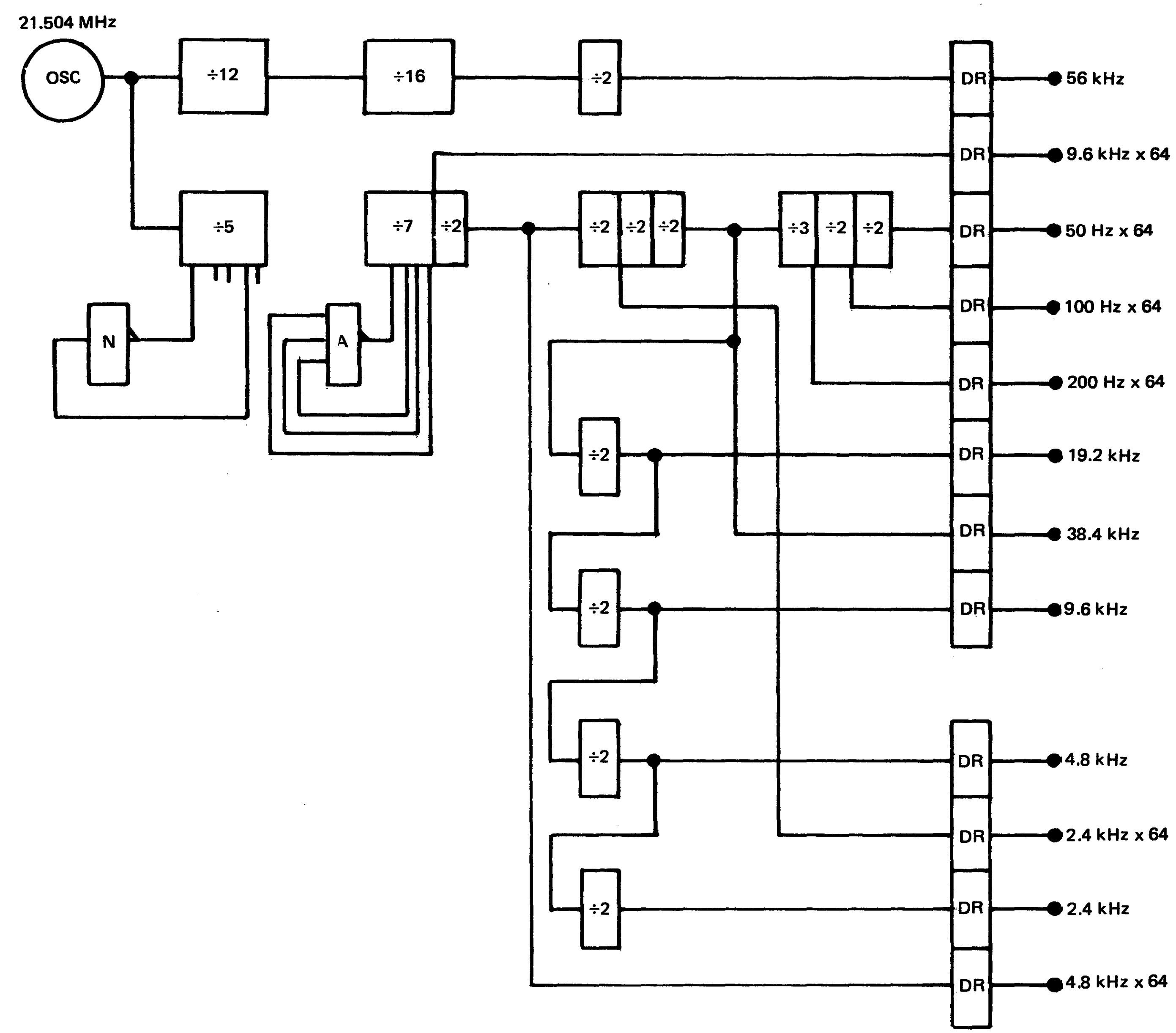


Figure CA476-1. Multispeed Clock Card (CA10) Schematic

CA477 X.21 (Nonswitched) Card (CA11)

The X.21 (nonswitched) card (Figure CA477-1) converts signal levels between the SDLC adapter VTL interface and the CCITT X.21 interface. It contains discrete components and two different VTL modules: (1) X.21 driver modules and (2) X.21 receiver modules.

Each X.21 driver module contains four driver circuits that operate from VTL levels on the logic side to provide X.21 levels on the interface side.

Each X.21 receiver module contains four receiver circuits that derive their voltages from the interface lines and provide VTL level signals to the SDLC adapter. The receivers do not provide for fail-safe operation. A receiver indicates either an off or an on condition with its input floating. The receivers present a 100-ohm or greater impedance to the CCITT interface.

The data transfer rates for the X.21 interface are 2400, 4800, 9600 and 48,000 bps. The maximum rate for the 8130 and attached 8101s is 9600 bps. The maximum rate for the 8140 and attached 8101s is 48,000 bps.

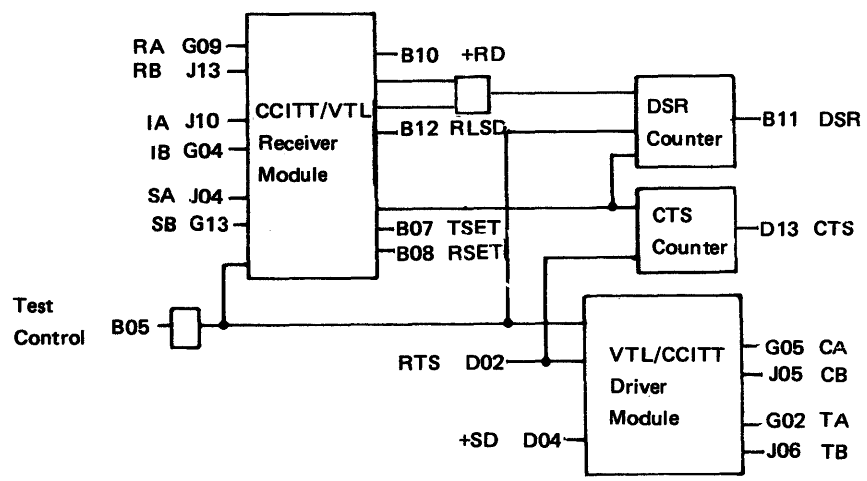


Figure CA477-1. X.21 (Nonswitched) Card (CA11) Schematic

CA480 Adapter/Driver Card – System Logic

CA481 SDLC Adapter Card (CA1) With or Without Clock

XXXX IOBO Bit P	B02		G12 IOBI Bit P	XXXX
XXXX IOBO Bit 0	G02		G09 IOBI Bit 0	XXXX
XXXX IOBO Bit 1	J02		J06 IOBI Bit 1	XXXX
XXXX IOBO Bit 2	D10		G07 IOBI Bit 2	XXXX
XXXX IOBO Bit 3	G08		J07 IOBI Bit 3	XXXX
XXXX IOBO Bit 4	J04		G10 IOBI Bit 4	XXXX
XXXX IOBO Bit 5	D09		J10 IOBI Bit 5	XXXX
XXXX IOBO Bit 6	B09		J11 IOBI Bit 6	XXXX
XXXX IOBO Bit 7	D06		J12 IOBI Bit 7	XXXX
			D12 outbus 0	XXXX
XXXX IO tag	B04		D13 outbus 1	XXXX
XXXX TA tag	D05		D11 outbus 2	XXXX
XXXX TC tag	B08		B10 outbus 3	XXXX
XXXX TD tag	B05		B13 outbus 4	XXXX
XXXX select	B12			
XXXX address 5	J09			
XXXX address 6	B03			
XXXX address 7	D04	SDLC with	G03 valid	XXXX
XXXX halt	G04	or without	B07 bus in IR	XXXX
XXXX IR level	G05	Clock Card	M13 CS request	XXXX
XXXX PIO ops	J13	(CA1)	P04 CS grant	XXXX
XXXX reset	J05		P11 end of chain	XXXX
XXXX sync UC	M07		D02 IRR	XXXX
			D07 parity valid	XXXX
XXXX CS grant	P05			
rate 2400 BPS	M03			
rate 600 BPS	M04		S02 data rate select	1
rate 1200 BPS	M05		S03 new sync	2
			S05 local test	3
			S10 request to send	4
8 RLSD	S04		U04 transmit data	5
9 clear to send	S12		U09 select standby	6
10 data set rdy	S13		U12 data term rdy	7
11 ring indicate	U05			
12 receive clock	U10		P06 osc 38,400 Hz out TP	
13 transmit clock	U11		P07 osc 38,400 Hz out TP	
14 receive data	U13		M09 LF X 64 output TP	54
			P09 LF X 64 input TP	
1280 Hz output TP	M10		P12 RX clock output	
1280 Hz input TP	M12		P13 RX clock input	
			S07 course timer clock out	
RX data out TP	S08		U07 course timer clock in	
RX data in TP	S09		U06 TX clock out TP	
NC. preset TP	P10		U02 TX clock in TP	

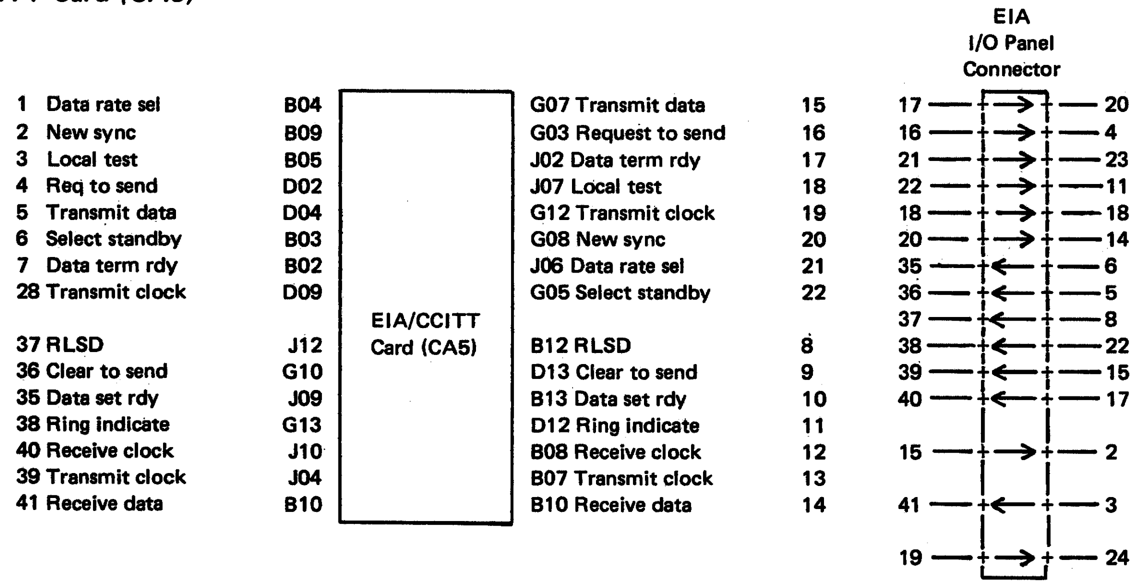
Note: *When using the clocked version of SDLC, ground at least one rate pin. Also jumper: P12 to U10 and U06 to U11.*

CA482 BSC/S-S Adapter Card (CA2)

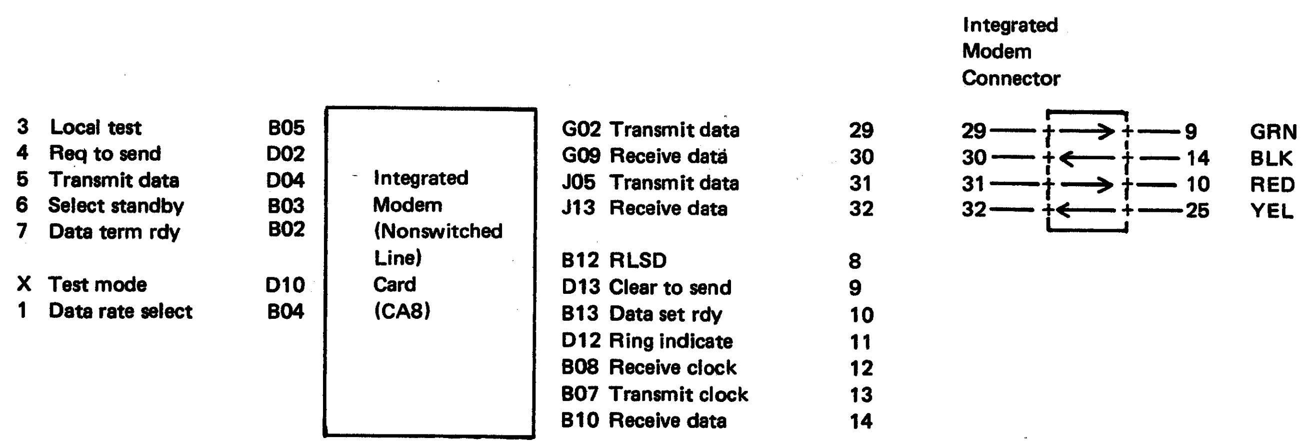
XXXX IOBO Bit P	B02		G12 IOBI Bit P	XXXX
XXXX IOBO Bit 0	G02		G09 IOBI Bit 0	XXXX
XXXX IOBO Bit 1	J02		J06 IOBI Bit 1	XXXX
XXXX IOBO Bit 2	D10		G07 IOBI Bit 2	XXXX
XXXX IOBO Bit 3	G08		J07 IOBI Bit 3	XXXX
XXXX IOBO Bit 4	J04		G10 IOBI Bit 4	XXXX
XXXX IOBO Bit 5	D09		J10 IOBI Bit 5	XXXX
XXXX IOBO Bit 6	B09		J11 IOBI Bit 6	XXXX
XXXX IOBO Bit 7	D06		J12 IOBI Bit 7	XXXX
			D12 outbus 0	XXXX
XXXX IO tag	B04		D13 outbus 1	XXXX
XXXX TA tag	D05		D11 outbus 2	XXXX
XXXX TC tag	B08		B10 outbus 3	XXXX
XXXX TD tag	B05		B13 outbus 4	XXXX
XXXX select	B12			
XXXX address 5	J09			
XXXX address 6	B03			
XXXX address 7	D04	BSC/S-S with	G03 valid	XXXX
XXXX halt	G04	or without	B07 bus in IR	XXXX
XXXX IR level	G05	Clock Card	M13 asyncronous	XXXX
N.C. run tx clk T.P.	J13	(CA2)		
XXXX reset	J05		P11 external rst sync	XXXX
XXXX sync UC	M07		D02 IRR	XXXX
rate 150 BPS	P02		D07 parity valid	XXXX
rate 75 BPS	P04			
rate 110 BPS	P05			
rate 134 BPS	M02			
rate 2400 BPS	M03			
rate 600 BPS	M04		S02 data rate select	1
rate 1200 BPS	M05		S03 new sync	2
rate 300 BPS	G13		S05 local test	3
			S10 request to send	4
8 RLSD	S04		U04 transmit data	5
9 clear to send	S12		U09 select standby	6
10 data set rdy	S13		U12 data term rdy	7
11 ring indicate	U05			
12 receive clock	U10		P06 osc 38,400 Hz out TP	
13 transmit clock	U11		P07 osc 38,400 Hz out TP	
14 receive data	U13		M09 LF X 64 output TP	54
			P09 LF X 64 input TP	
1280 Hz output TP	M10		P12 RX clock output	
1280 Hz input TP	M12		P13 RX clock input	
NC. reset RX clock TP	M08		S07 LO 0 output TP	
RX data out TP	S08		U07 LO 0 input TP	
RX data in TP	S09		U06 TX clock out TP	
NC. preset TP	P10		U02 TX clock in TP	

Note: *When using the clocked version of BSC/S-S, ground at least one rate pin. No other jumpers are required on the board.*

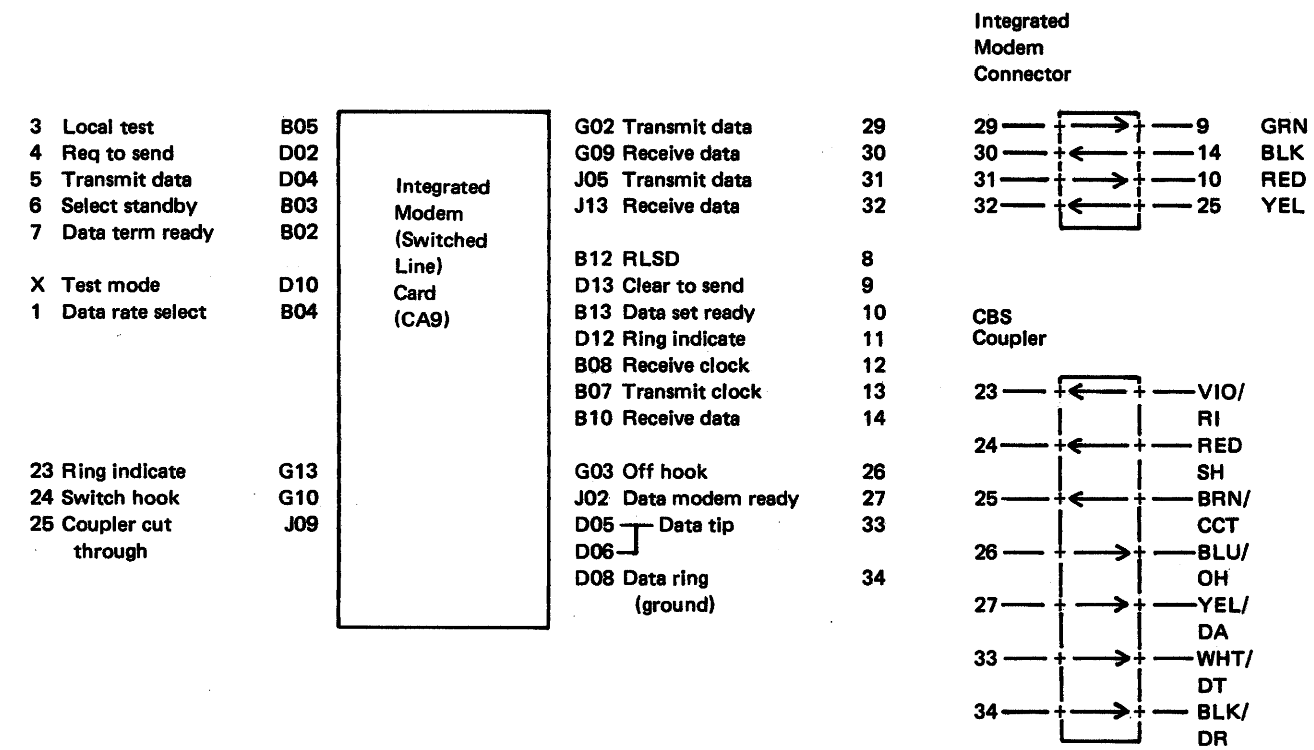
CA483 EIA/CCITT Card (CA5)



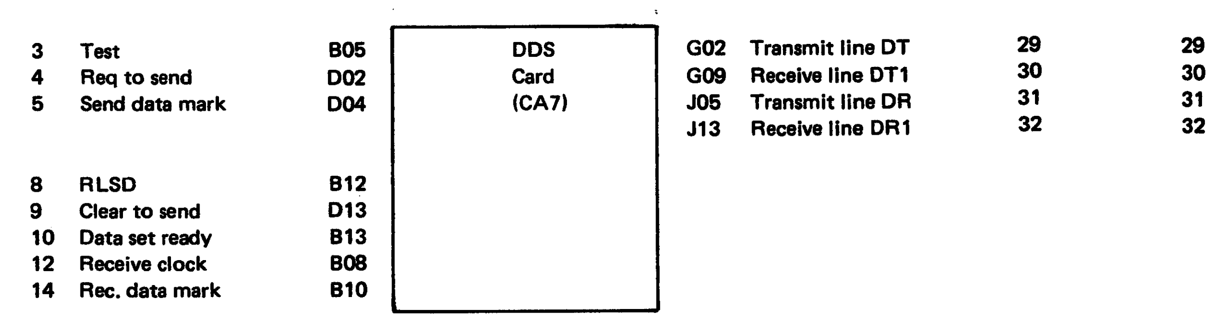
CA484 Integrated Modem (Nonswitched Line) Card (CA8)



CA485 Integrated Modem (Switched Line) Card (CA9)



CA486 DDS Card (CA7)



CA487 Loop Card (CA3/CA4)

Lobe 1

Loop Card (CA3)

1	Data rate select	B04
2	New sync	B09
3	Local test	B05
4	Request to send	D02
5	Transmit data	D04
6	Select standby	B03
7	Data term read	B02
0	+Gt intf drvrs on	D11
63	Degate rec	G12

G02	D+	55
G09	R+	56
J05	D–	57
J13	R–	58
J02	Loop data I/O	61
D09	Loop clock I/O	62
B12	RLSD	8
D13	Clear to send	9
B13	Data set ready	10
D12	Ring indicate	11
B08	R set (rcv clk)	12
B07	T set (tsm clk)	13
B10	Receive data	14
G07	Pick relay 1	59
G08	Pick relay 2	60

Lobe 2

Loop Card (CA4)

7	Data terminal rdy	B02
4	Request to send	D02
3	Local test	B05
2	New sync	B04
1	Data rate select	B09
0	+Gt intf drvrs on	D11
61	Loop data I/O	J02
62	Loop clock I/O	G09
XX	Ground	G10

G02	D+	64
G09	R+	65
J05	D–	66
J13	R–	67
B12	RLSD	8
D13	Clear to send	9
B13	Data set ready	10
J12	Ring indicate	11
B08	R set (rcv clk)	12
B10	RX (receive data)	13
G07	Pick relay 1	59
G08	Pick relay 2	60
G13	Degate transmit	63

CA488 V.35 Card (CA6)

V.35 Card (CA6)

2	R set (NS)	B09
3	Test control	B05
4	Request to send	D02
5	Transmit data	D04
7	Data term ready	B02
28	T set	D09
37	RLSD	J12
36	Clear to send	G10
35	Data set ready	J09
44	T set minus	G13
49	R set plus	J10
45	T set plus	J04
48	R set minus	G04
46	Receive data plus	G09
47	Receive data minus	J13

G07	T set minus	53
G03	Request to send	16
J02	Data term ready	17
J07	Test control	18
G08	T set plus	52
J06	R set plus	51
G05	R set minus	50
G02	Transmit data plus	43
J05	Transmit data minus	42
B12	RLSD	8
D13	Clear to send	9
B13	Data set ready	10
B08	Receive clock	12
B07	Transmit clock	13
B10	Receive data	14
D10	Test mode	

CA489 X.21 (Nonswitched) Card (CA11)

X.21 Card (CA11)

4	Request to send	D02
5	Transmit data	D04
36	Clear to send	D13
7	Data term ready	B02
3	Test control	B05
13	T set	B07
12	R set	B08
14	Receive data	B10
37	RLSD	B12
35	Data set ready	B13

J04	Signal element timing A	70
G13	Signal element timing B	71
G02	Transmit A	29
J05	Transmit B	31
G05	Control A	72
J06	Control B	73
J10	Indication A	74
G04	Indication B	75
G09	Receive A	30
J13	Receive B	32

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CA500 Adjustment, Removal, and Replacement Information

CA501 Basic Checklist

1. Is power on in:
   a. The 8100 system?
   b. All units?
   c. The modem(s), local and remote?
   d. The channel service unit (DDS or X.21)?
   e. The direct connected device/host?
   f. The data coupler/data access arrangement?
2. Cables/connectors:
   a. Are internal and external cable connectors plugged tightly into the correct locations?
   b. Are the correct communications cables installed in the correct locations?
   c. Is there physical damage to the cables and connectors?
3. Operating system:
   Is the correct operating system being used?
4. MD diskette 02:
   Is the correct MD diskette (02) being used?
5. Cards (adapter or driver/receiver):
   Are the cards damaged?

CA510 Card Information

CA511 Card Replacement

Caution: System power must be off when cards or cables are disconnected or connected.

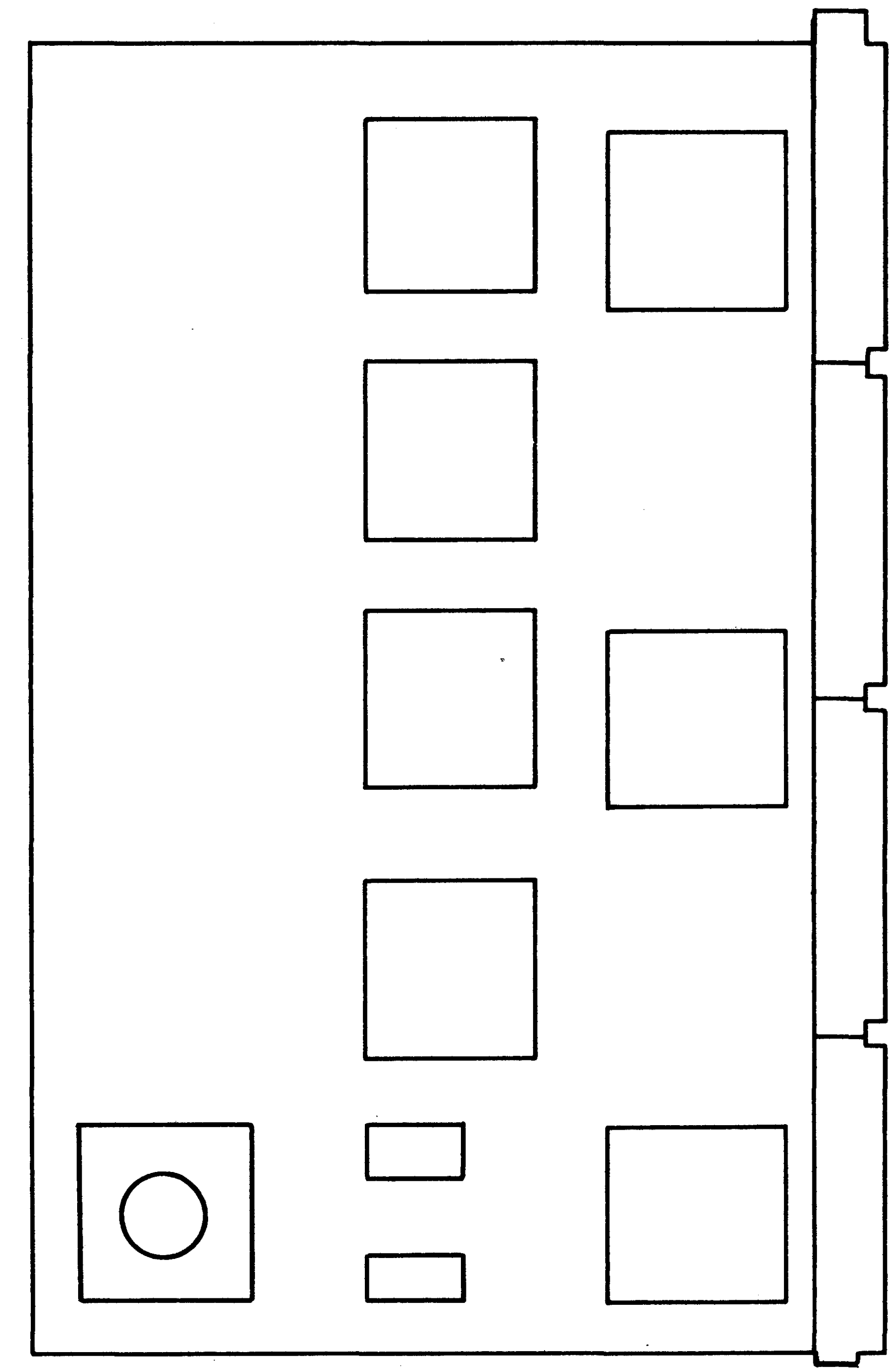
For CA card locations, see CA513.

1. Jumper the card correctly; refer to CA150 and CA563.
2. Replace each card in the card list, one card at a time, and in the sequence listed.
3. Run the CA test that detected the CA failure, or continue the CA MAP by pressing the Forward key (on the MD).
4. Replace cards until all the cards in the list are used, or until the CA test runs successfully, or as directed by the CA MAP.

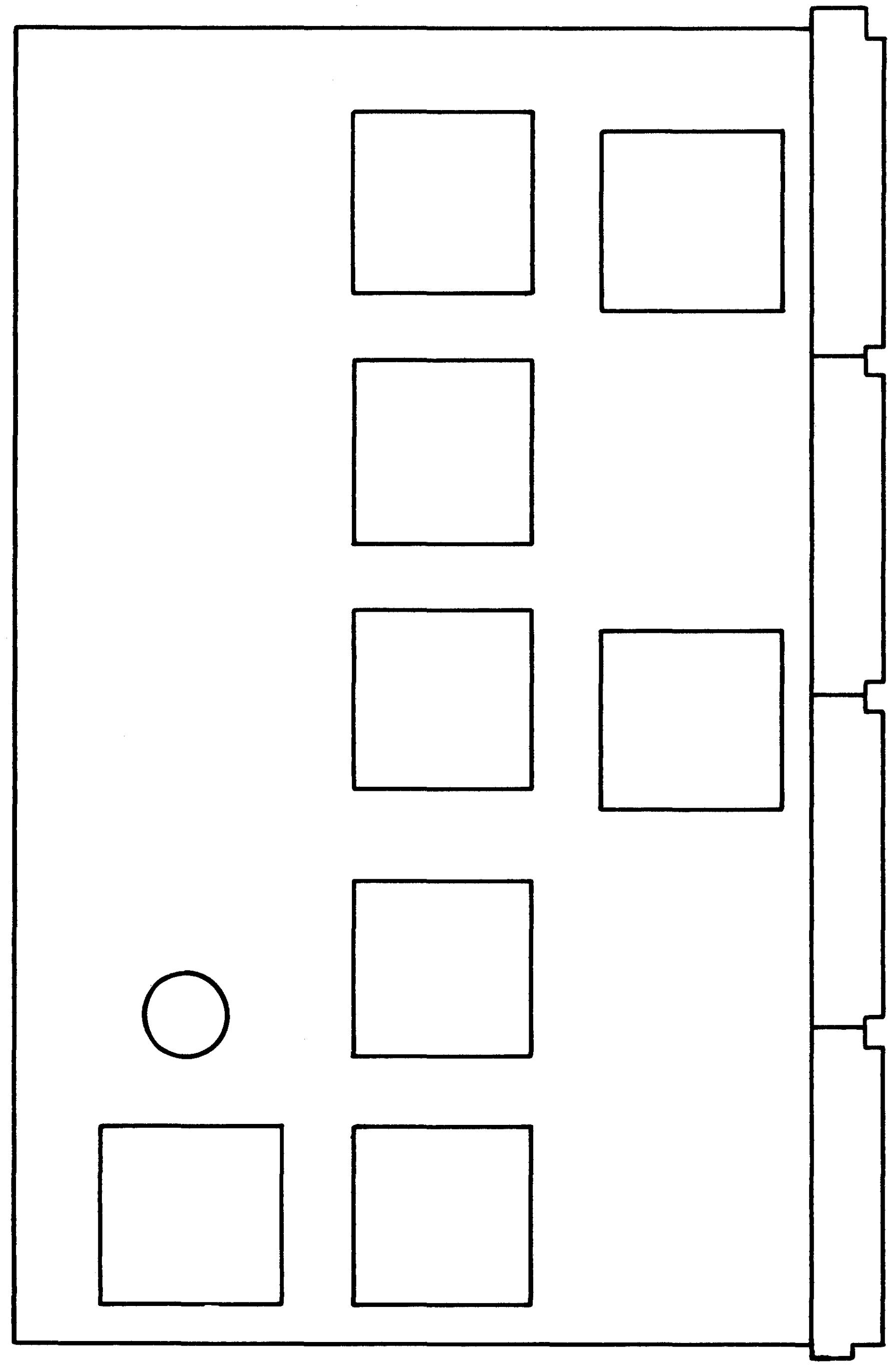
CA512 Card Layout

Refer to CA563 for card layouts of the CA feature cards with jumpers.

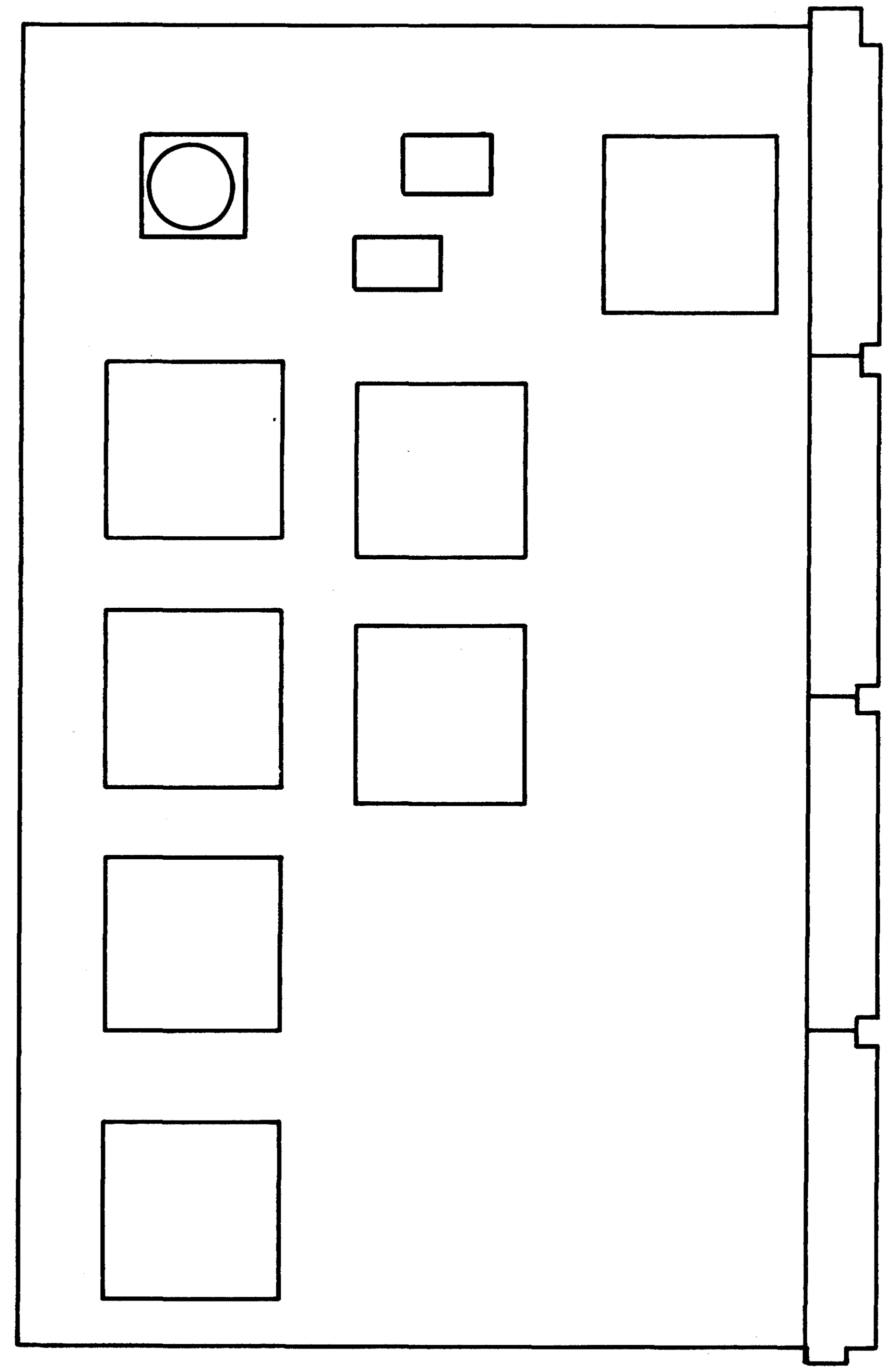
SDLC (CA1) Adapter Card without Clock



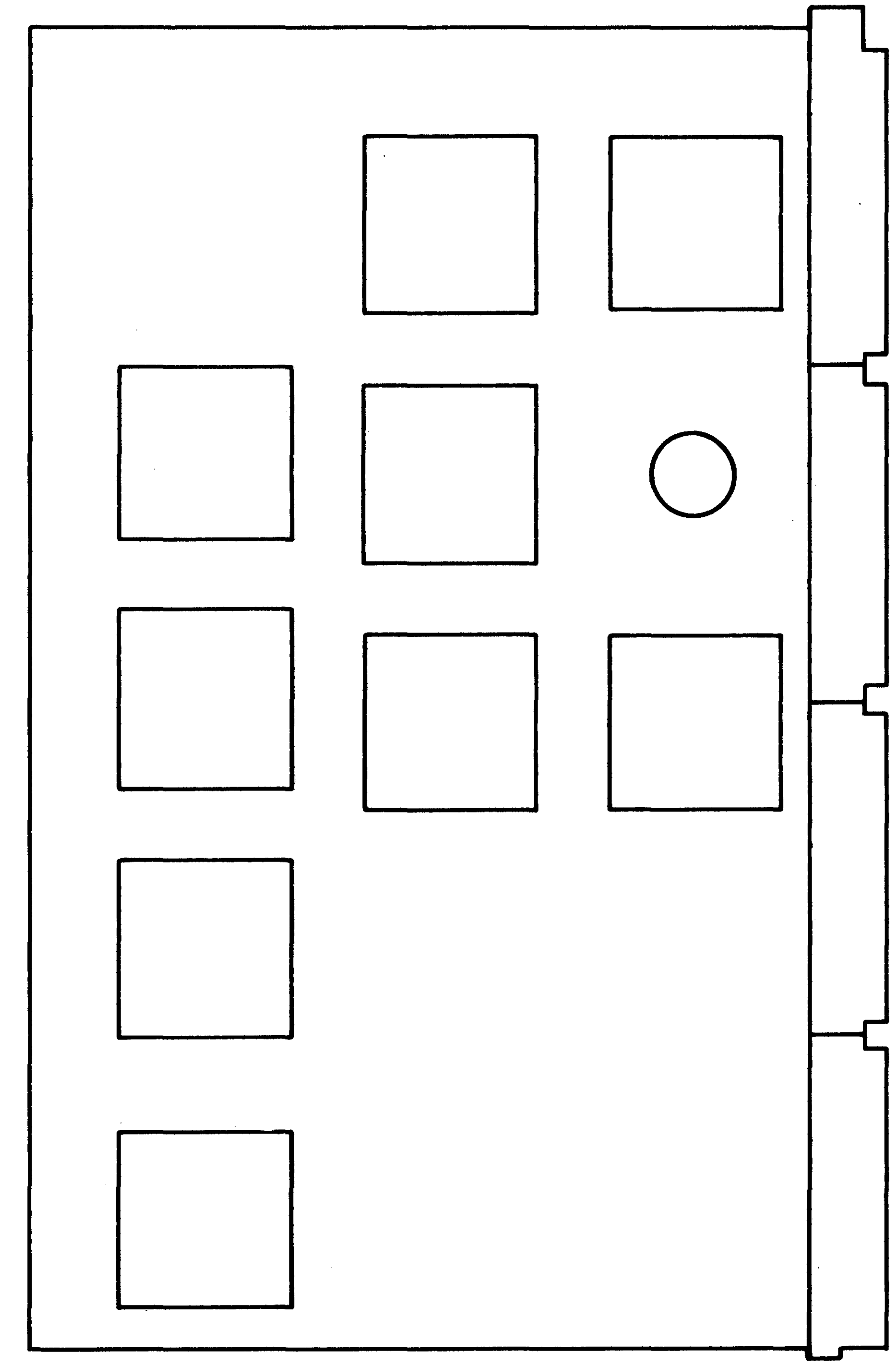
SDLC (CA1) Adapter Card with Clock



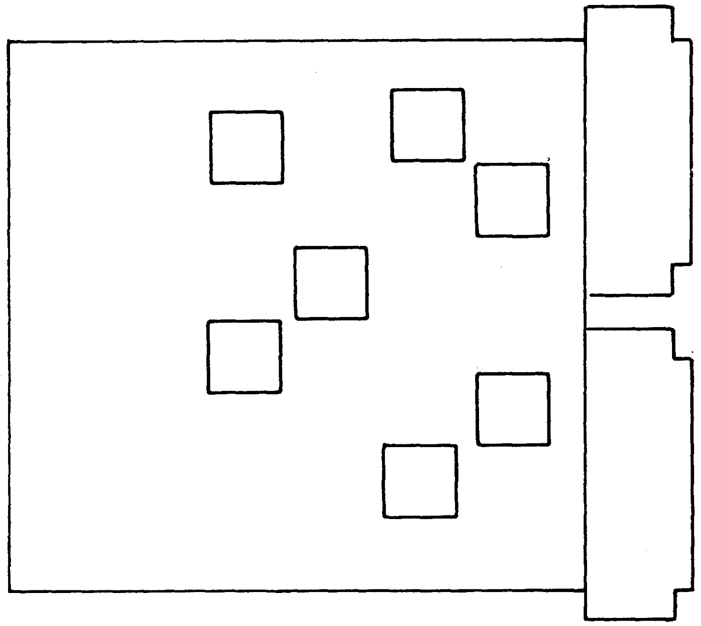
BSC/S-S (CA2) Adapter Card without Clock



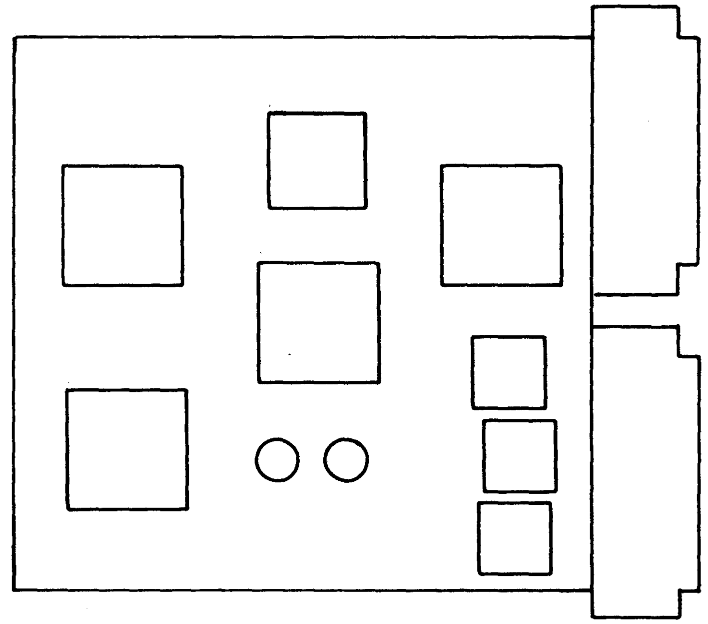
BSC/S-S (CA2) Adapter Card with Clock



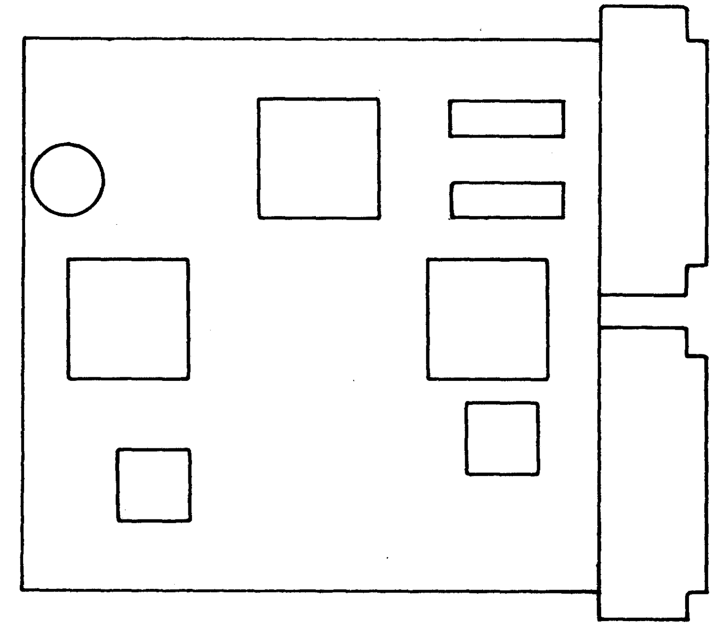
EIA/CCITT (CA5) Card



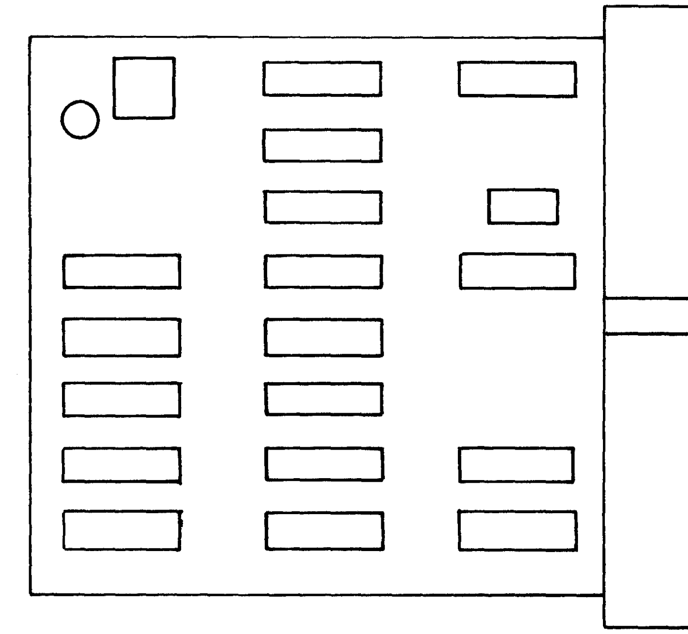
Loop (CA3/CA4) Card



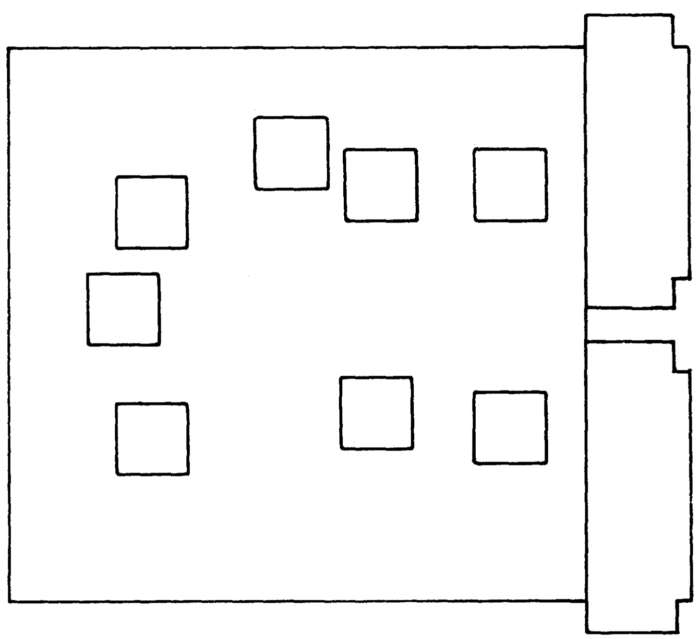
Digital Data Service Driver/Receiver (CA7) Card



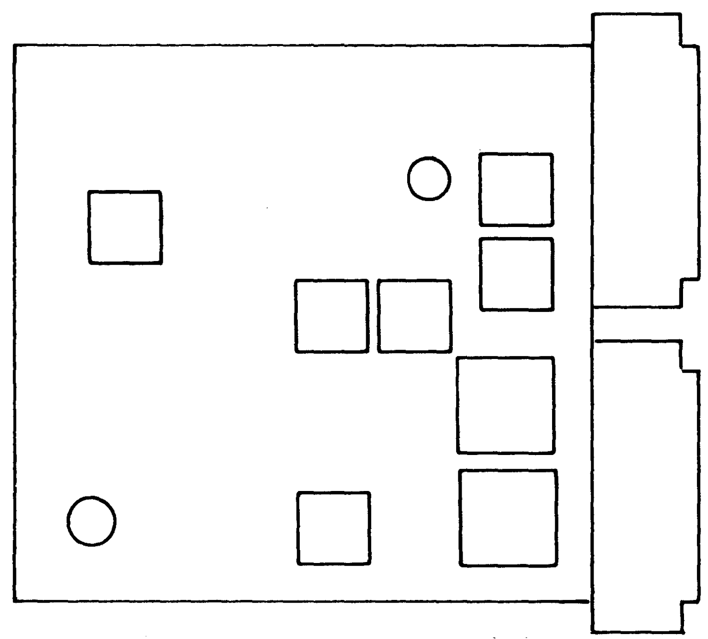
X.21 (Nonswitched) Driver/Receiver (CA11) Card



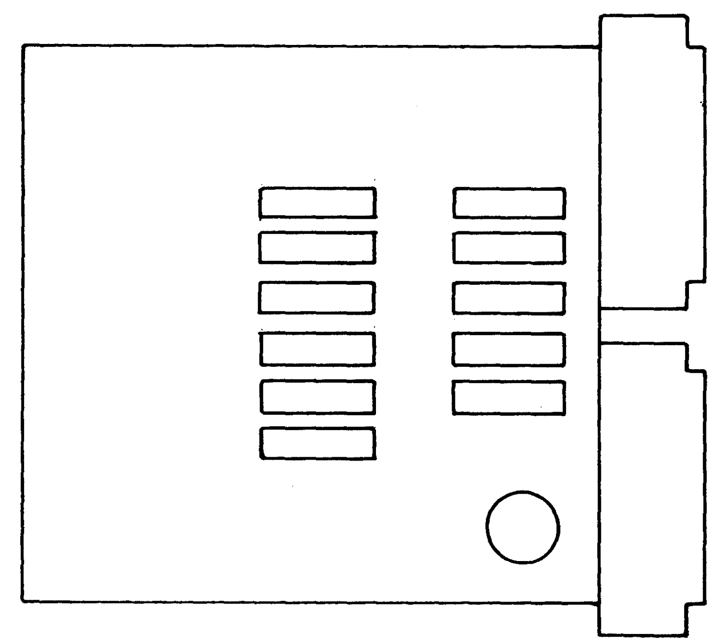
V.35 Driver/Receiver (CA6) Card



Integrated Analog Modem (CA8) – Nonswitched Line Card



Multispeed Clock (CA10) Card



CA513 Card Locations

To locate any adapter card, driver/receiver card, or board cable socket, use the pseudo card identification from Figure CA513-1 and the board layouts in CA520. CA521 through CA524 show the maximum configurations for the 8130, 8140, and 8101 units and the physical address for each card or cable location.

Figure CA513-2 shows the relationship between the physical address and the port number in the 8130/8140 and 8101. Note that the 8101 port number is 1 more than the translate array position, which is equal to the low-order digit of the physical address. The 8130/8140 port number is equal to the translate array position.

The following examples show how to use the tables and board layouts:

1. Find the location of the SDLC adapter card for a physical address of 82 for a system that only has an 8130.

   The SDLC adapter card is a CA1 pseudo-card type, and CA521 shows the board layout for an 8130. The CA1 card for address 82 is in location 01A-A1S2.

2. Find the CA4 card for the sixth port of the fourth 8101.

   Figure 513-2 shows that the physical address is 4D, and CA524 shows the location of the second-lobe driver/receiver card is 01A-B1J4 (XC–XF).

Pseudo Card Identifier	Card Types
CA1	SDLC Adapter Card
CA2	BSC/SS Adapter Card
CA3	Loop Adapter, Lobe 1
CA4	Loop Adapter, Lobe 2
CA5	EIA Card
CA6	V.35 Card
CA7	DDS Card
CA8	Integrated Modem, Nonswitched Line
CA9	Integrated Modem, Switched Line
CA10	**Multispeed Clock Card**
CA11	**X.21 (nonswitched) Card**

Figure CA513-1. Pseudo Card Designation Table

Mach Type	Port No.	Communications Physical Address (PA) in Hex
8130 **	1	81
	2	82
	3	83
	4	84
	5	85
	6	86
8140 Model AXX	1	81
	2	82
	3	83
8140 Model BXX	1	80
	2	81
	3	82
	4	83
	5	50
	6	51
	7	52
	8	53
	9	5C
	10	5D
	11	5E
	12	5F

Mach Type	Port No.	Communications Physical Address (PA) in Hex			
8101		8101 Position*			
		1st	2nd	3rd	4th
	1	10	20	30	40
	2	11	21	31	41
	3	12	22	32	42
	4	13	23	33	43
	5	1C	2C	3C	4C
	6	1D	2D	3D	4D
	7	1E	2E	3E	4E
	8	1F	2F	3F	4F

* 8101 positions are determined by specify codes, as follows:
Position 1: 9921
Position 2: 9922
Position 3: 9923
Position 4: 9924

**Feature Expansion Type 1 is required for the 8130 to have ports 3, 4,5, and 6. Also, the System Expansion Feature is required for the SDLC and BSC/S-S adapters in an 8130 to have programmable interrupt levels, and for 8101s to be attachable to the 8130.

PROCEDURE:

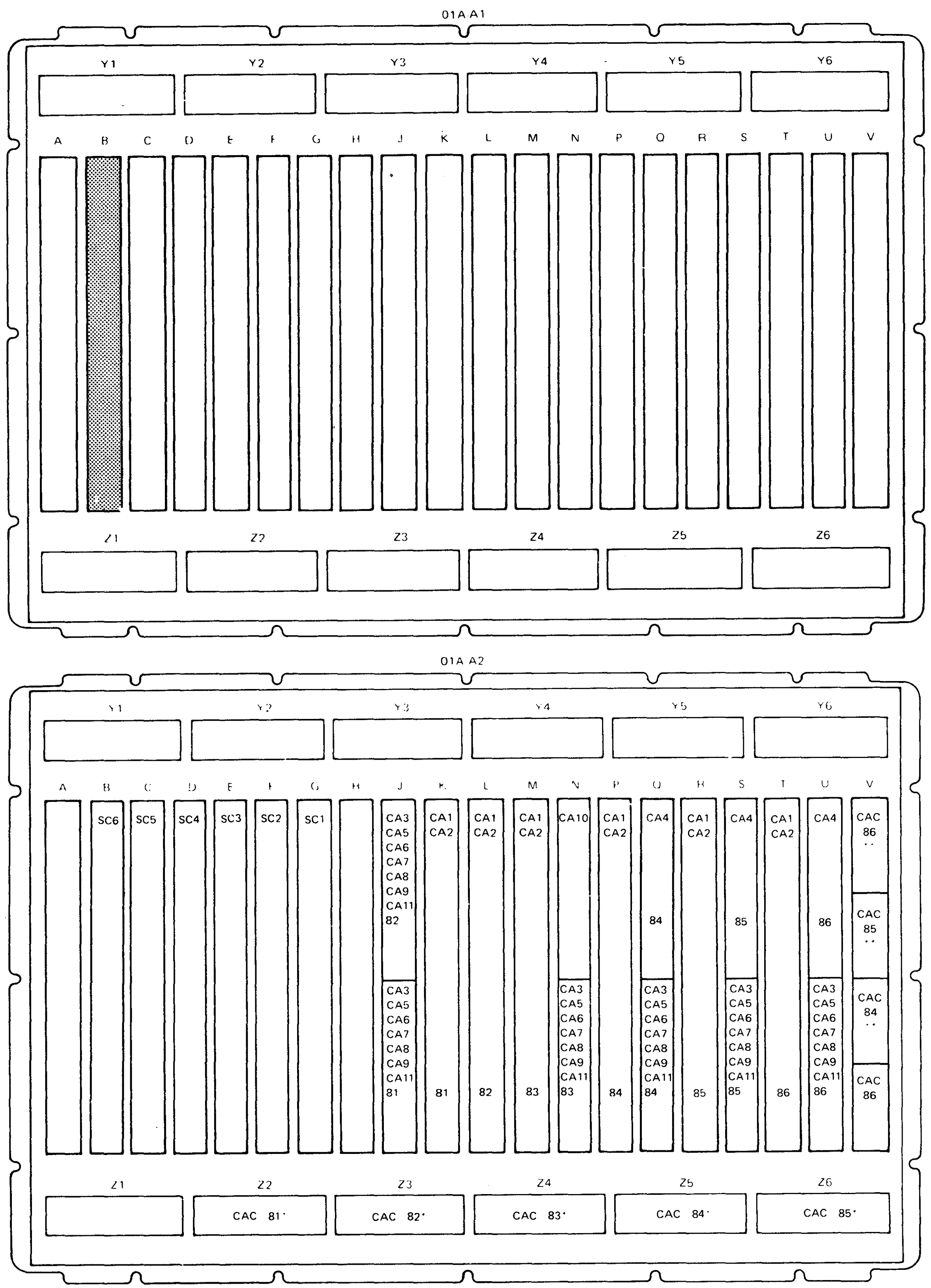
Known: Physical address (PA) and CA card ID

	Use
Determine unit type (8130/8140 or 8101) and position/location and port number of PA	1. Inspect units address plate 2. PA
Determine model number	1. Inspect units model plate
Determine board layout	1. Model number 2. CA520
Determine board socket of card	1. PA 2. Port number 3. CA card ID 4. CA520
Determine card type	1. CA card ID 2. Figure CA513-1
Determine card part number	1. Card type 2. 8130/8140/8101 Parts Catalog

Figure CA513-2. Port Addressing

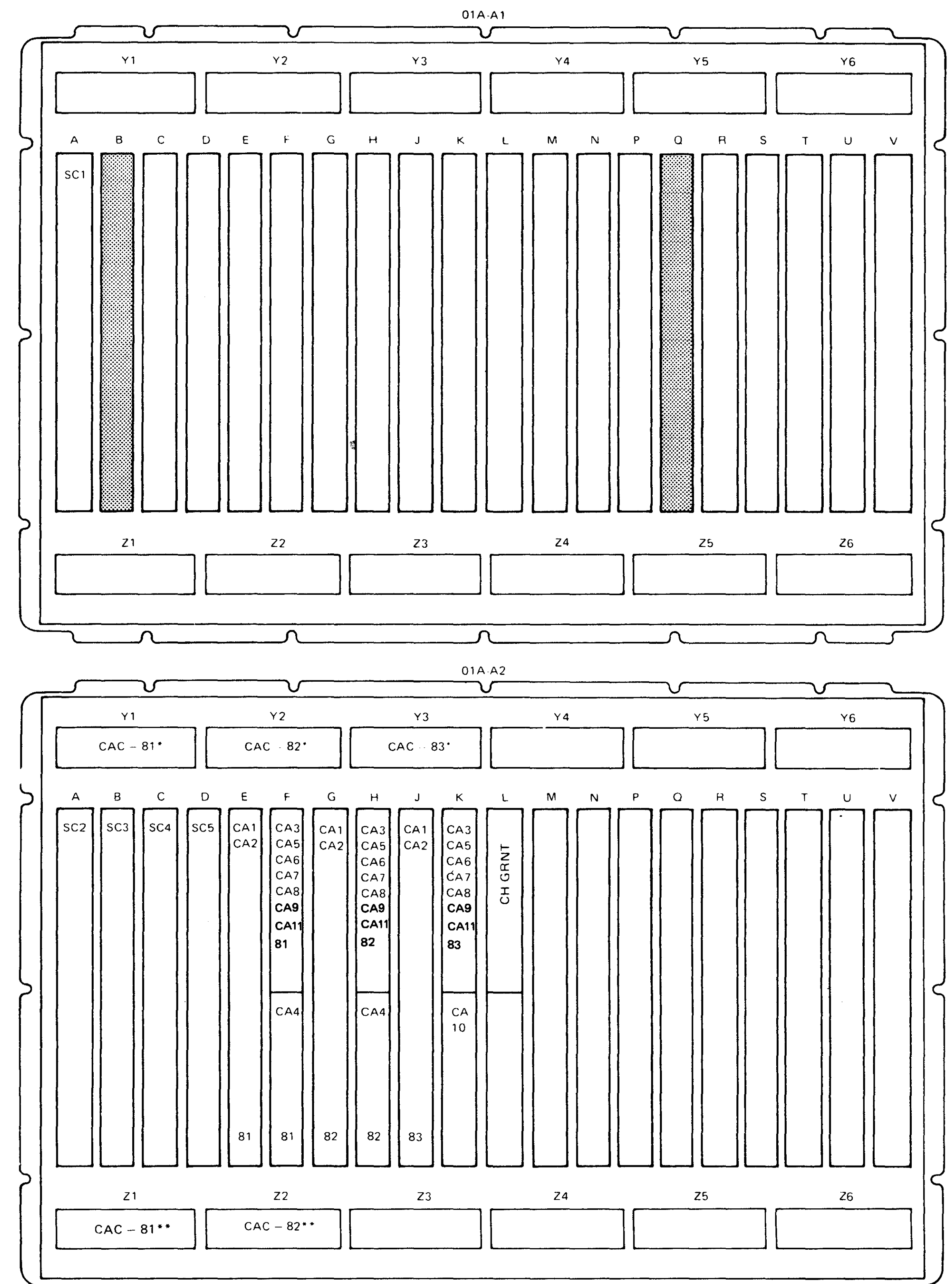
CA520 Board and Cable Layout

CA521 8130 Processor



CAC CA cable group. (* Cable group lobe 1, ** Cable group lobe 2)

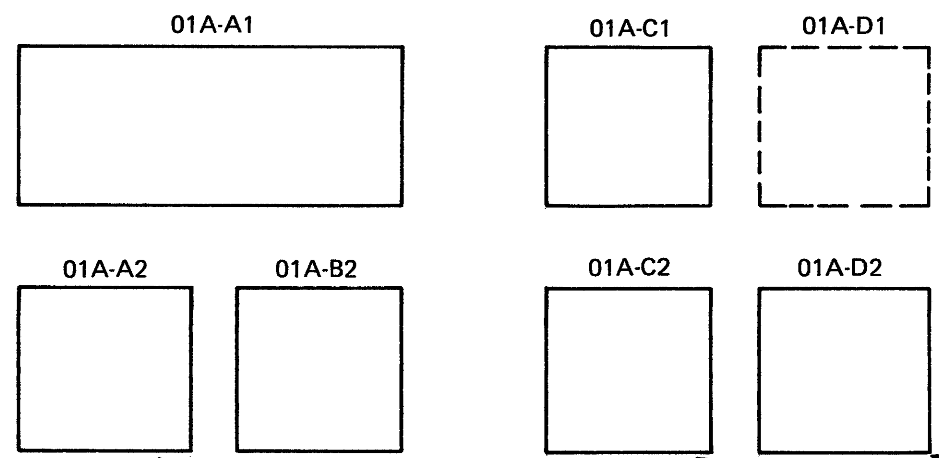
CA522 8140 Processor, Models A31 to A44 Only



CAC CA cable group. * Lobe 1, ** Lobe 2 Models 31 44 only. 51 54 have no FACs.

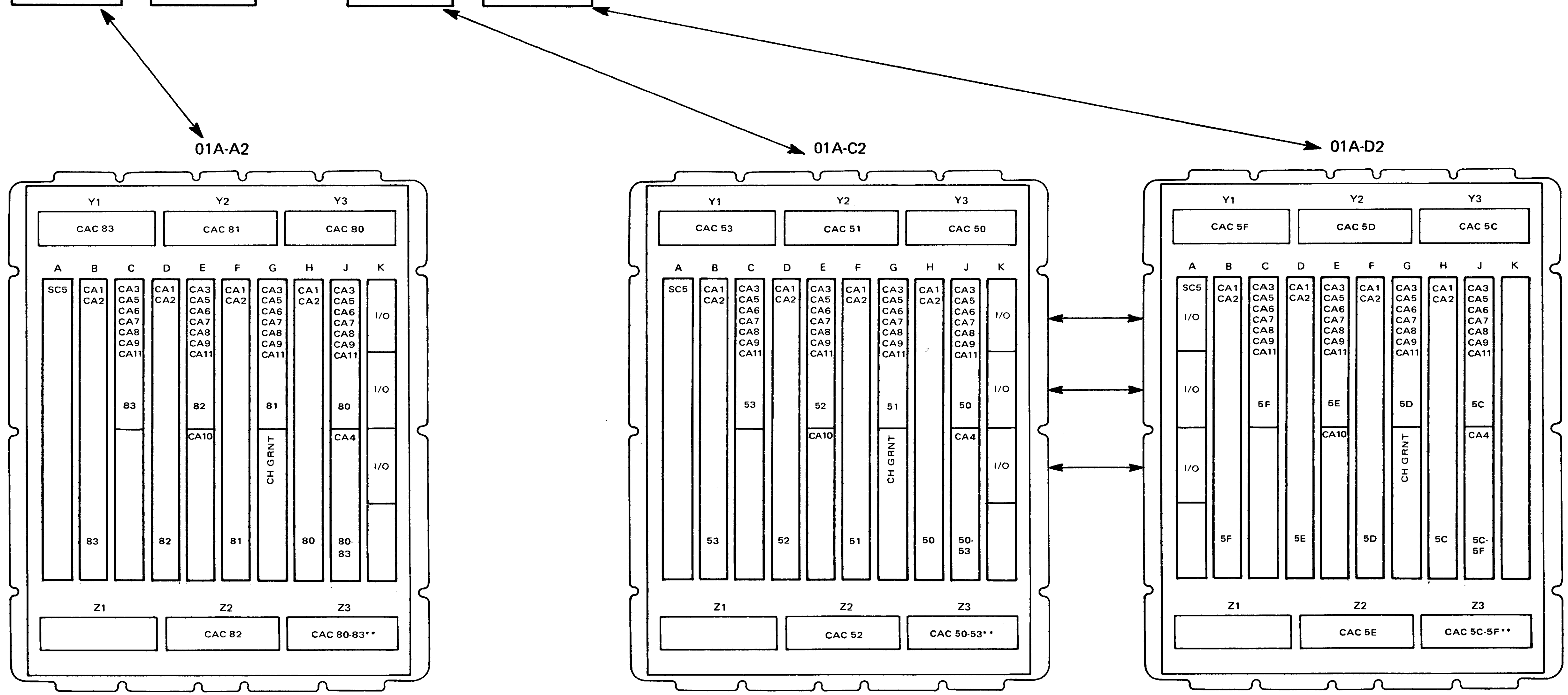
CA523 8140 Processor, Models B51 to B72

Board Configuration



Addressing

SSCF PA = 88		SSCF PA = 58	
PA	Port Number	PA	Port Number
80	1	50	5
81	2	51	6
82	3	52	7
83	4	53	8
		5C	9
		5D	10
		5E	11
		5F	12

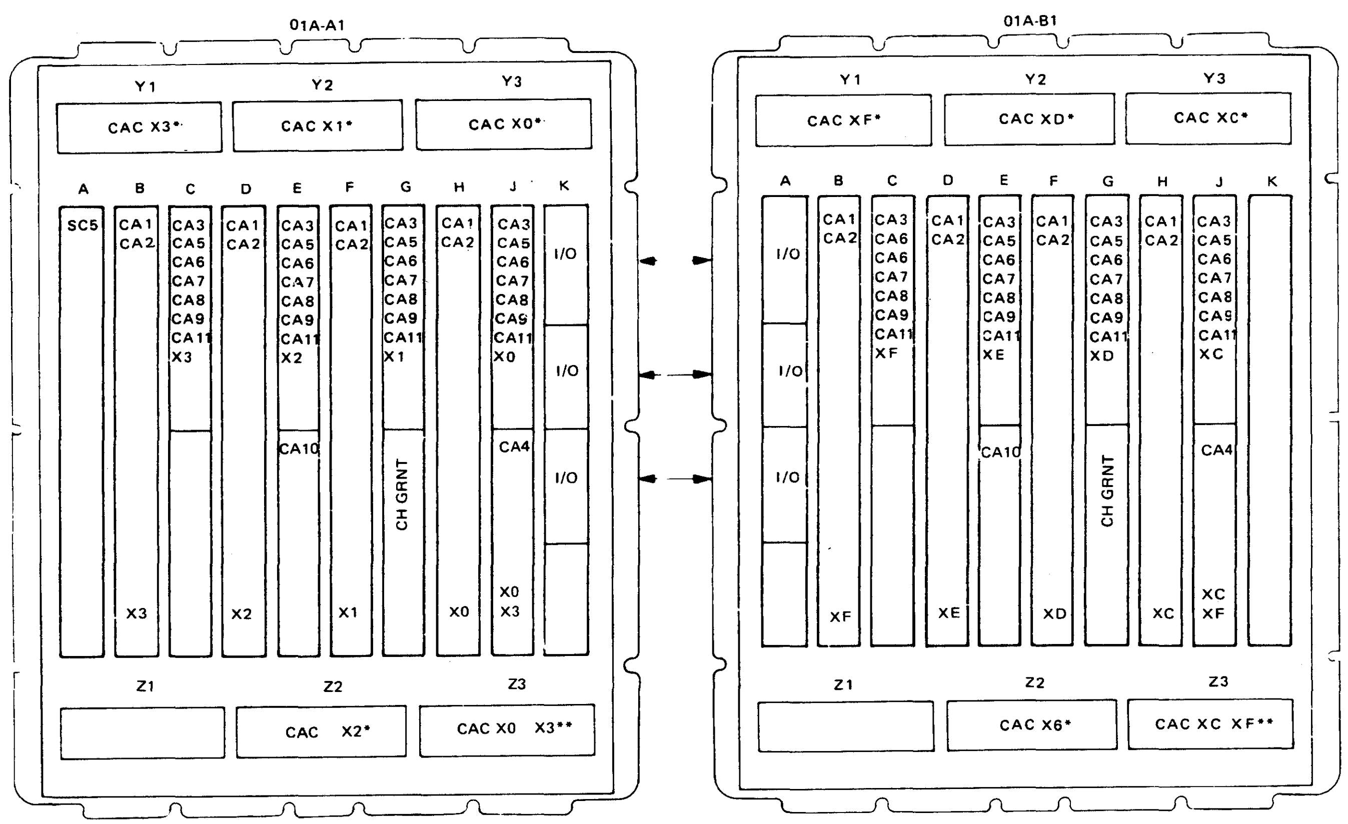


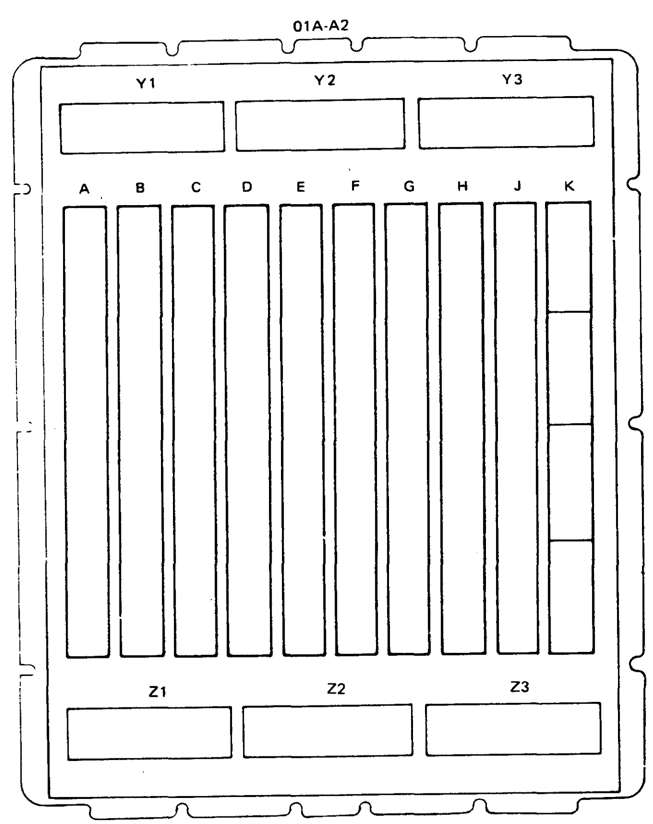
A2 Board - P/N 4939821
C2 Board - P/N 4939821
D2 Board - P/N 4939822

CAC – CA Cable Group

**If present, Lobe 2

CA524 8101 Storage and I/O Unit





A1 Board – P/N 4939821
A2 Board – P/N 6812948
B1 Board – P/N 4939822

CAC – CA cable group.
* Lobe 1, ** lobe 2.

Note: *8101 Physical Addresses are dependent on the number of 8101s in the 8100 system. X represents the first digit in the address of the 1st, 2nd, 3rd, or 4th 8101. Refer to Figure CA513-2.*

Example: Physical address 2E is in the 2nd 8101.

CA525 Cable Locations

Cable locations can be identified by using the following:

1. Board layout (CA521–CA524) shows the maximum configuration for the 8130, 8140, and 8101 units. Locate the cable type by board socket. These layouts show the relationship of the physical address to card location.
2. Figure CA513-2, Port Addressing, shows the relationship between the port address and the port number.
3. Board-to-I/O panel connections (CA420) show the board sockt-to-I/O panel socket connections.

A cable group consists of those cables from the board socket for that CA feature to the I/O panel connector, and from the I/O panel connector to the intermediate device; that is, modem, direct connect device, coupler, etc. Figure CA525-1 shows pseudo cable designations.

Pseudo Cable Group Identifier	Cable Group Types
CAC 3	Loop, lobe 1
CAC 4	Loop, lobe 2
CAC 5A	EIA modem
CAC 5B	EIA direct modem
CAC 6A	V.35 modem
CAC 6B	V.35 - direct connect
CAC 7	DDS
CAC 8	Integrated modem, nonswitched line
CAC 9	Integrated modem, switched line
CAC11	X.21 (nonswitched)

PROCEDURE:

Known: Physical address (PA) and CA cable ID	
Determine unit type (8130/8140 or 8101) and position/location of PA	Use: 1. Inspect unit's address plate 2. PA 3. Figure CA513-2
Determine model number	Use: 1. Inspect unit's model plate
Determine board layout	Use: 1. Model number 2. CA520 (board layout)
Determine board socket of cable	Use: 1. PA 2. CA cable ID 3. CA520 (board layout)
Determine cable type	Use: 1. CA cable ID
Determine cable part number	Use: 1. Cable type 2. 8100 Parts Catalog
Determine board to I/O panel connector	Use 1. Cable type 2. Unit type 3. CA420

Figure CA525-1. Pseudo Cable Designation Table

CA526 Cable Replacement

Caution: System power must be off when cards or cables are disconnected or connected.

For CA cable locations, see CA525.

1. Replace each cable in the cable group one cable at a time.
2. Run the CA test that detected the CA failure, or continue the CA MAP by pressing the Forward (FWD) key on the MD keypad.
3. Replace cables until all the cables of the cable group are used, or until the CA test runs successfully, or as directed by the CA MAP.

CA530 Standard and Special Voltages

Standard Voltages at Board Socket Locations		
Mach Type	**Models**	**Board – Socket**
8130	A2X	A2 – K2, L2, M2, P2, R2, T2
8140	A3X, A4X	A2 – E2, G2, J2
8140	BXX	A2, C2, D2 } B2, D2, F2, H2
8101	A1X	A1 – B2, D2, F2, H2 B1 – B2, D2, F2, H2

Voltage*	Range	Test Point
+5V dc	+4.5 to +5.5V dc	D03
+8.5V dc	+7.7 to +9.3V dc	B11
–5V dc	–4.5 to –5.5V dc	B06
Ground		D08

*Voltages enter the board through voltage bus connectors (pin side).

Special Voltages at Board Socket Locations		
Mach Type	**Models**	**Board – Socket**
8130	A2X	A2 – J2, J4, N4, Q4, S4, U4
8140	A3X, A4X	A2 – F2, H2, K2
8140	BXX	A2, C2, D2 } C2, E2, G2, J2
8101	A1X	A1 –C2, E2, G2, J2 B1 – C2, G2, E2, J2

Voltages	Range	Test Point
–8.5V dc	–7.7 to –9.3V dc	XX D07* EIA/V.35 card CA5/CA6 card

*Voltage enters the board to the XXD07 pin through a single wire.

CA540 Troubleshooting Charts and Diagrams

CA541 General Troubleshooting Chart

Figure CA541-1 shows a general diagram of an 8100 communications attachment feature. In general, this figure represents a data link; a directly attached loop is represented by points A through F only.

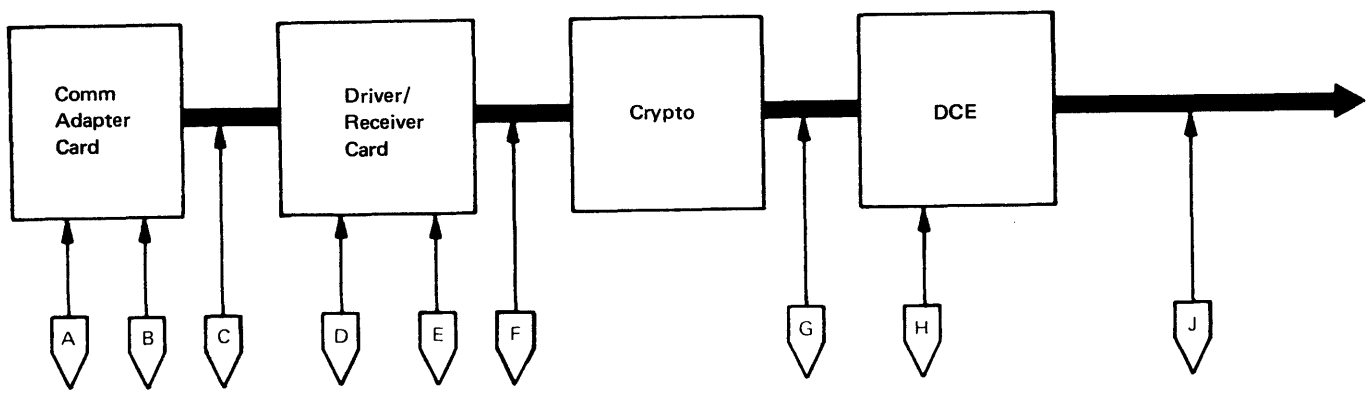


Figure CA541-1. General Diagram for Troubleshooting Purposes

The boxes denote the following:

- **Comm Adapter Card = SDLC (CA1) Adapter Card**
  = BSC/SS (CA2) Adapter Card
- Driver/Receiver Card = EIA (CA5) Card
  = V.35 (CA6) Card
  = Loop (CA3/CA4) Card
  = Integrated Modem (CA8/CA9) Card
  = DDS (CA7) CArd
  = X.21 (nonswitched) (CA11) Card
- Crypto = Cryptographic Unit (IBM 3845/3846 or OEM)
- DCE = Data Circuit-Terminating Equipment
  = Channel Service Unit
  = Modem

The points are described as follows:

- **Point A: Test Routine 1 checks to determine if the adapter can communicate on the I/O Bus. Base adapter card logic is tested.**
- Point B: Test Routines 1–15 check the major portion of the adapter card.
- Point C: Routines 16 and higher test through this point. Driver/Receiver lines are tested using Routines 18, 19, 20, 21, 22, 61, and 63, depending on the configuration. Driver/Receiver lines may be probed or monitored at this point.
- Point D: Routine 16 tests to this point if internal wrap is jumpered and depending on the configuration.
- Point E: Routines 18, 19, 20, and 21 test to this point, depending on the configuration.
- Point F/G: Routines 16 (external wrap jumper) 51, 52, 61, **63, 64, 66, 67, 68 test** through this point, depending on the configuration. Lines may be monitored at this point. This point includes board-to-I/O panel cables, I/O panel connector, and external cable.
- Point H: Routines 16 and 64 (external wrap jumper and IBM Modem) test to this point.
- Point J: Only link-level tests test through this point. If the DCE is an IBM DCE, data lines may be probed or monitored at this point.

CA542 Routines 19 and 20 Troubleshooting Diagram

Caution: Routines 19 and 20 do not run under DPCX.

General. Figures CA542-1 and CA542-2 are troubleshooting diagrams used with Routine 19 for a nonswitched integrated modem, and with Routine 20 for a switched integrated modem. The routines determine and report the lines in error that you can probe; figures provide points and voltage levels.

Equipment Required

1. CA MD diskette 02.
2. General logic probe, or oscilloscope, or volt/ohmmeter (VOM).

Test Description. See CA212, Routines 19 and 20. These test routines may be run under MAP control (offline or online) or invoked free-lance (offline).

Card Locations. See CA513 for card locations.

Test Procedure. You can enter this section under MAP control or in free-lance mode. If under MAP control, go to step 2; if under free-lance mode, go to step 1.

1. Prepare to invoke Routines 19 and 20. Load the TCM (offline) (see CP810 in Chapter 2). The monitor must be at 80BC wait stop.
2. Run routines 19 and 20. If under MAP control, press the FWD key on the MD to run the test. If under free-lance mode, enter the invocation message (PA 00 19 or 20 B) using the appropriate online/offline test invocation procedure (see CP462 in Chapter 2).
3. Review the test results. If under MAP control, the MAP reviews the results and directs necessary action. If under free-lance mode, review the test message; if a routine 19 or 20 error has occurred, identify the lines in error (see Routines 19 and 20 Description, CA212, and Test Message, CA230) and probe these lines to isolate a fault.

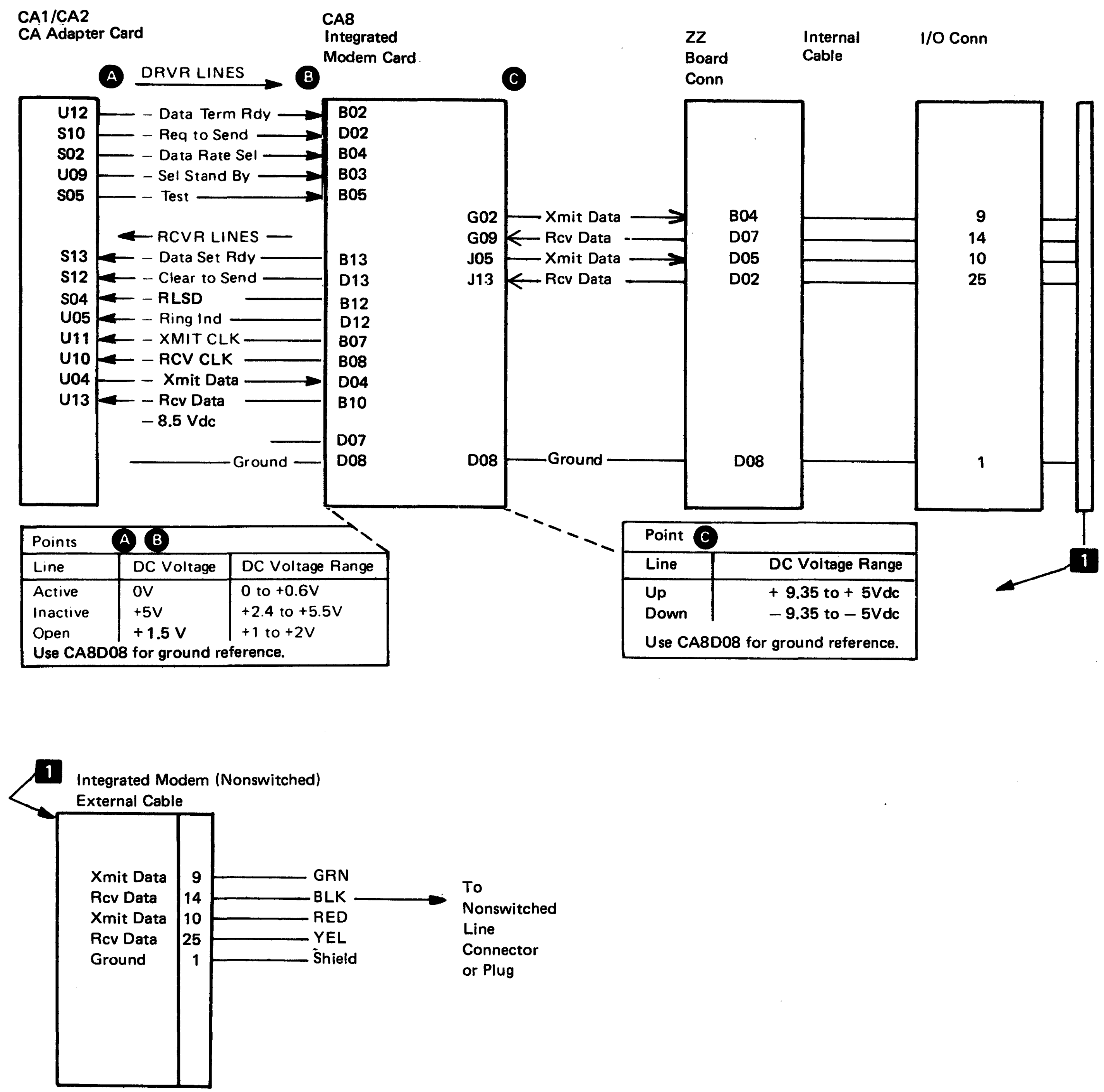


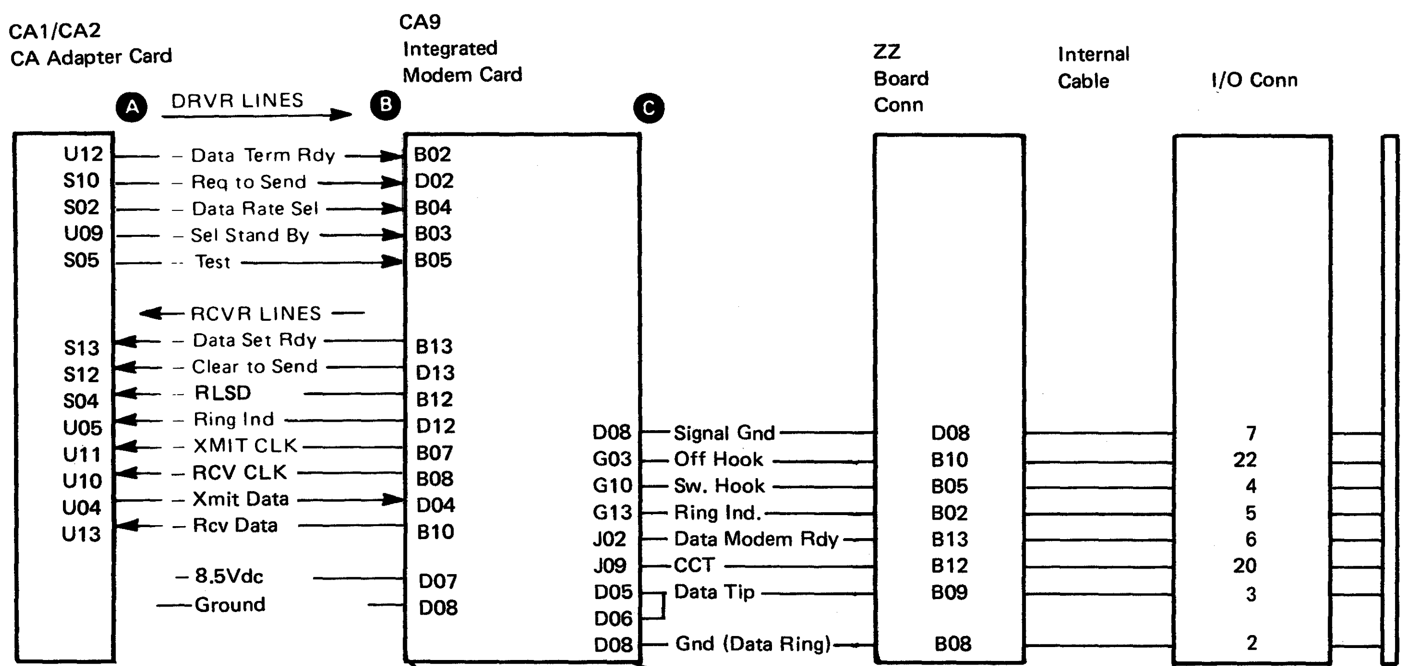
Figure CA542-1. Troubleshooting Diagram for Routine 19, Nonswitched Integrated Modem

Expected Line Status

Error		Drivers					Receivers			
RREN	Test	DTR	RTS	NS	SSB	DRS	DSR	CTS	RLSD	RI
1911	I	I	I	I	I	I	A	I	I	I
1920	A	I	I	I	I	I	A	I	I	I
1921	I	I	I	I	I	I	A	I	I	I
1930	A	A	I	I	I	I	A	I	I	I
1931	A	I	I	I	I	I	A	I	I	I
1933	A	I	A	I	I	I	A	A	A	I
1940	A	I	A	I	I	I	A	A	A	I
1941	A	I	I	I	I	I	A	I	I	I
1980	A	A	A	I	I	I	A	A	A	I
1981	I	I	I	I	I	I	A	I	I	I
1988	I	I	I	I	I	I	A	I	I	
1990	A	There is data on the Xmit Data line; XMIT CLK and RCV CLK are present.					There is data on the Rcv Data line; XMIT CLK and RCV CLK are present.			

Legend:

- A = Active
- I = Inactive
- RR = Routine number
- EN = Error number



Points A B		
Line	DC Voltage	DC Voltage Range
Active	0V	0 to +0.6V
Inactive	+5V	+2.4 to +5.5V
Open	+1.5V	+1 to +2V
Use CA9D08 for ground reference.		

Point C	
Line	DC Voltage Range
Up	+ 9.35 to + 5Vdc
Down	– 9.35 to – 5Vdc
Use CA9D08 for ground reference.	

1

Expected Line Status

Error RREN	Test	Drivers DTR	RTS	NS	SSB	DRS	Receivers DSR	CTS	RLSD	RI
2011	I	I	I	I	I	I	I	I	I	I
2033	A	A	A	I	I	I	A	A	A	A
2034	A	A	A	I	I	I	A	A	A	A
2050	A	A	A	I	I	I	A	A	A	I
2088	I	I	I	I	I	I	I	I	I	I
2090	A	There is data on the Xmit Data line; XMIT CLK and RCV CLK are present.					There is data on the Rcv Data line; XMIT CLK and RCV CLK are present.			

Legend:

A = Active
I = Inactive
RR = Routine number
EN = Error number

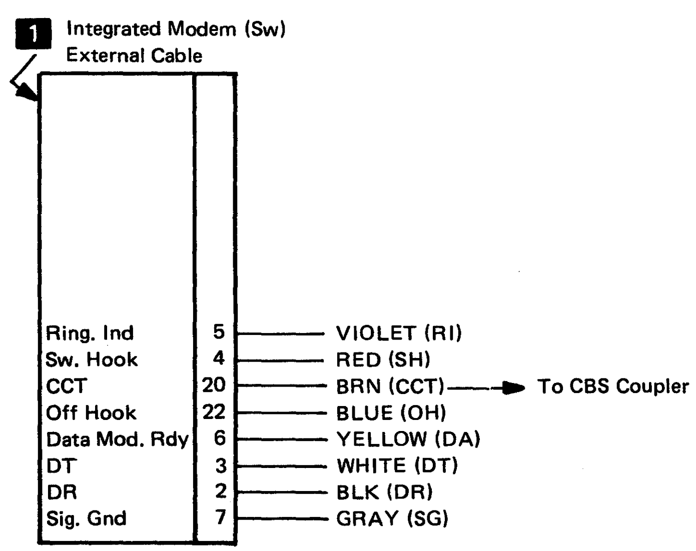


Figure CA542-2. Troubleshooting Diagram for Routine 20, Switched Integrated Modem

CA543 Routine 61 Troubleshooting Diagram

Caution: Routine 61 does not run under DPCX.

General. Figure CA543-1 is a troubleshooting diagram used with Routine 61 and any necessary probing to provide the information needed for fault isolation in the EIA direct-connect feature. Control and data line wrap testing occurs at the external communications cable. The routine determines, reports, and holds the line(s) in error that you can probe for fault isolation. The figure provides probe points and voltage levels.

Equipment Required

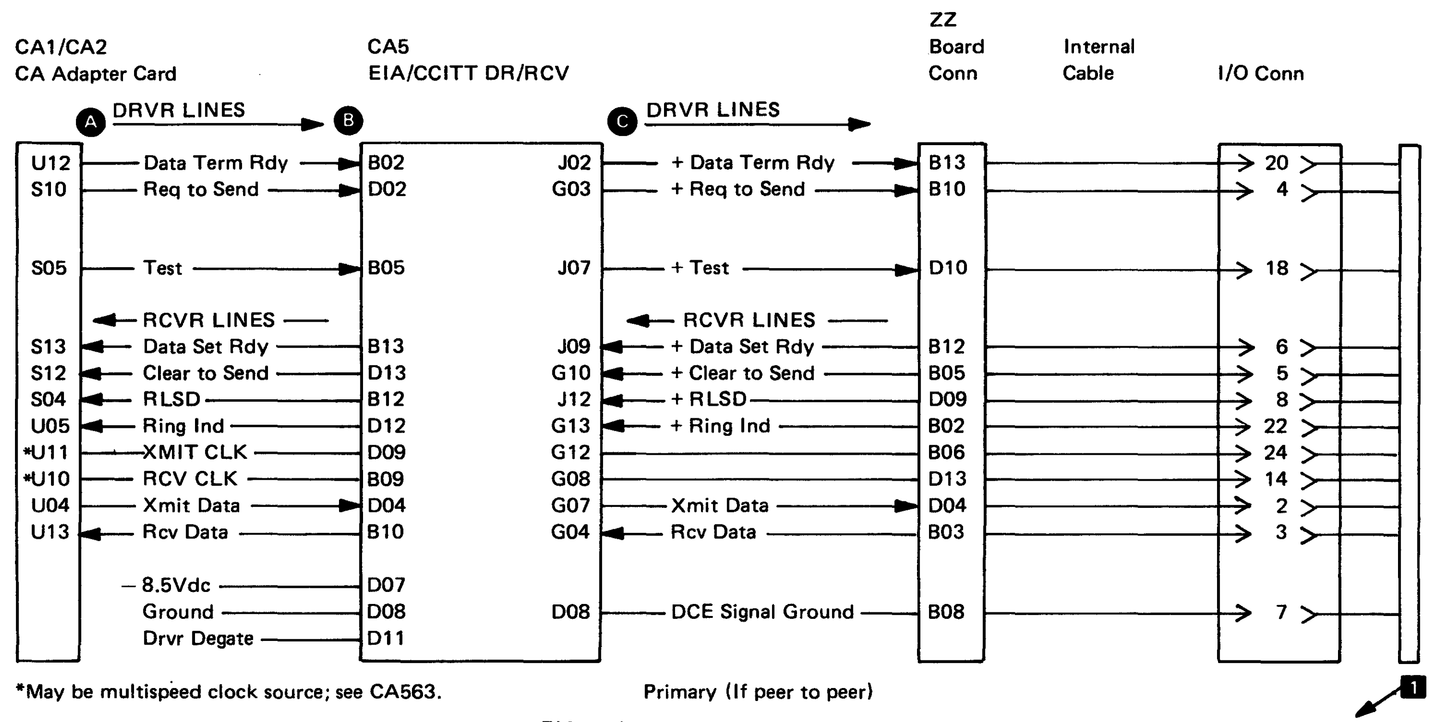
1. EIA direct-connect wrap plug.
2. CA MD diskette 02.
3. General logic probe, or oscilloscope, or volt/ohmmeter (VOM).

Test Description. See CA212, Routine 61. This test routine may be run under MAP control (offline or online) or invoked free-lance (offline).

Card Locations. See CA513 for card locations.

Test Procedure. You can enter this section under MAP control or in free-lance mode. If under MAP control, go to step 2; if under free-lance mode, go to step 1.

1. Prepare to invoke Routine 61. Load the TCM (offline) (see CP810 in Chapter 2). The monitor must be 80BC wait stop.
2. Prepare the external cable for test. Install the wrap plug at the extreme end of the 8100 EIA direct-connect external cable.
3. Run Routine 61. If under MAP control, press the FWD key on the MD to run the test. If under free-lance mode, enter the invocation message (PA 0061 B) using the appropriate online/offline test invocation procedure (see CP462 in Chapter 2).
4. Review the test results. If under MAP control, the MAP reviews the results and directs necessary action. If under free-lance mode, review the test message; if a Routine 61 error has occurred, identify the lines in error (see Routine 61 Description, CA212, and Test Messages, CA230) and probe the lines to isolate the fault.



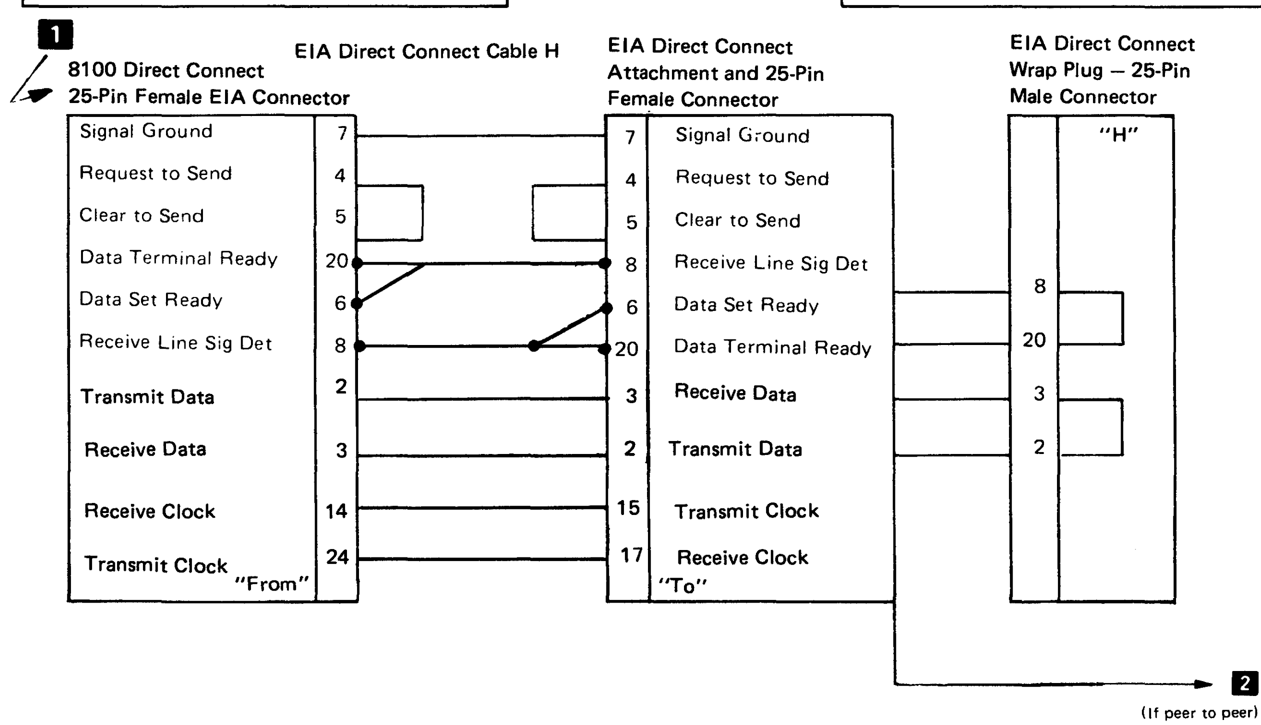
*May be multispeed clock source; see CA563.

Primary (If peer to peer)

EIA card inverts the lines.

Points A B		
Line	DC Voltage	DC Voltage Range
Active	0V	0 to +0.6V
Inactive	+5V	+2.4 to +5.5V
Open	+1.5V	+1 to +2V
Use CA5D08 for ground reference.		

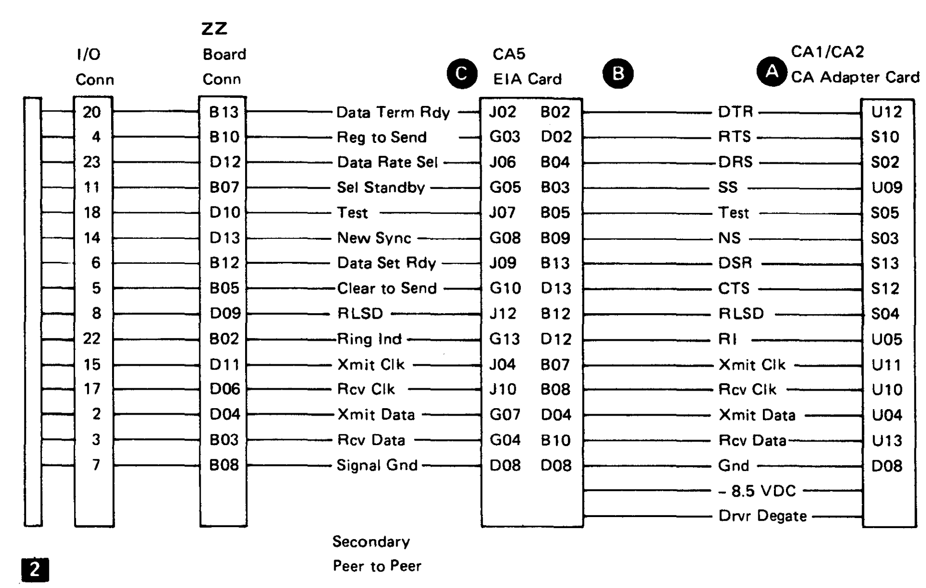
Point C		
Line	DC Voltage	DC Voltage Range
Active	+ 12V	+ 6 to +12.5V
Inactive	–12V	–6 to –12.5V
Open	+ 1V	+ 0.5 to 1.5V
Use CA5D08 for ground reference.		



Expected Line Status

Error RREN	Test	Drivers DTR	RTS	NS	SSB	DRS	Receivers DSR	CTS	RLSD	RI
6111	I	I	I	I	I	I	I	I	I	I
6120	A	I	I	I	I	I	I	I	I	I
6121	I	I	I	I	I	I	I	I	I	I
6122	I	I	I	I	A	I	I	I	I	I
6123	I	I	I	I	I	I	I	I	I	I
6124	I	I	I	A	I	I	I	I	I	I
6125	I	I	I	I	I	I	I	I	I	I
6125	I	I	I	I	I	A	I	I	I	I
6127	I	I	I	I	I	I	I	I	I	I
6130	I	A	I	I	I	I	A	I	A	I
6131	I	I	I	I	I	I	I	I	I	I
6133	I	I	A	I	I	I	I	A	I	I
6140	I	I	A	I	I	I	I	A	I	I
6141	I	I	I	I	I	I	I	I	I	I
6180	I	A	A	I	I	I	A	A	A	I
6181	I	I	I	I	I	I	I	I	I	I
6190	I	There is data on the Xmit Data line; XMIT CLK and RCV CLK are present.					There is data on the Rcv Data line; XMIT CLK and RCV CLK are present.			

Legend:
- A = Active
- I = Inactive
- RR = Routine number
- EN = Error number



EIA Direct Connect – Peer to Peer Installations

Designation	FAC	Clock Type	Cable End Label	Wrap Plug
Primary	15 16	Adapter w/clk Multispeed Clock CD	"From" "H"	"H" at "To" end
Secondary	17	None	"To" "H"	"H" At "From" end

Figure CA543-1. Troubleshooting Diagram for Routine 61, EIA Direct Connect

CA545 Routine 63 Troubleshooting Diagrams

Caution: Routine 63 does not run under DPCX. For V.35, the data path is tested only if the 8100 provides clock. Required configuration bits are: Adapter clock or Multispeed clock.

General. Figures CA545-1 through CA545-4 are troubleshooting diagrams used with Routine 63 under the following configurations: EIA/Modem, V.35/modem, V.35/direct connect terminal, and V.35/direct connect peer-to-peer. These figures provide information needed to probe for fault isolation. Control and data line wrap testing occurs at the external communications cable connector. The routine determines, reports, and holds the line(s) in error that you can probe for fault isolation. The figures provide probe points and voltage levels for the EIA and V.35 features.

Equipment Required

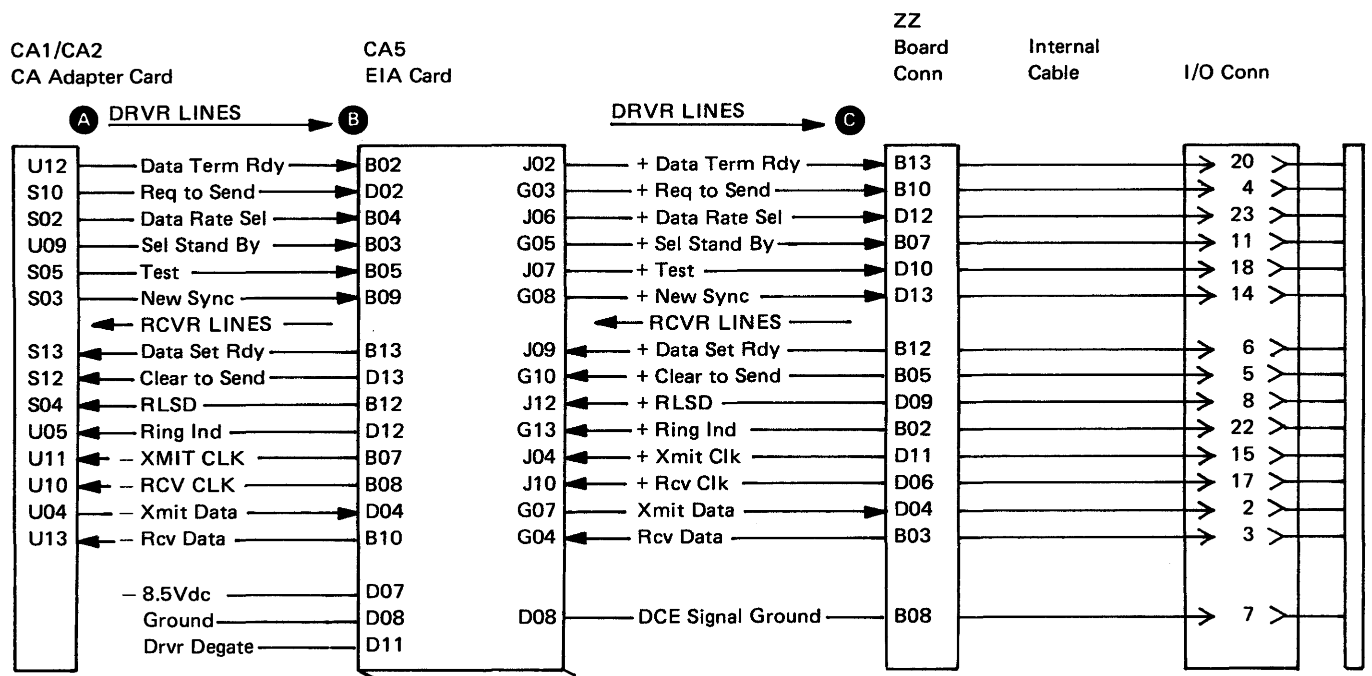
1. EIA modem external cable (C) or Modem Interface Test Set with standard EIA cable or V.35-modem wrap plug (G) or V.35 direct connect wrap plug (J for terminal; K for peer to peer).
2. CA MD diskette 02.
3. General logic probe, or oscilloscope, or volt/ohmmeter (VOM).

Test Description. See CA212, Routine 63. This test routine can be run under MAP control (offline or online) or invoked free-lance (offline).

Card Locations. See CA513 for card locations.

Test Procedure. You can enter this section under MAP control or under free-lance mode. If under MAP control, go to step 2; if under free-lance mode, go to step 1.

1. Prepare to invoke Routine 63. Load the TCM (offline) (see CP810 in Chapter 2). The monitor must be at 80BC wait stop.
2. Prepare the external cable for test. For V.35 install the plug at the extreme end of the 8100 external communications cable. For EIA set the Test-Operate switch on the end of the cable to the Test position or insert the Modem Interface Test Set onto the "To" end, and build the wrap as shown in Figure CA545-1. (The modem must remain connected.
3. Run Routine 63. If under MAP control, press the FWD key on the MD to run the test. If under free-lance mode, enter the invocation message (PA 0063 B) using the appropriate online/offline test invocation procedure (see CP462 in Chapter 2).
4. Review the test results. If under MAP control, the MAP reviews the results and directs the repair action. If under free-lance mode, review the test message; if a Routine 63 error has occurred, identify the tests in error (see Routine 63 Description, CA212, and Test Message, CA230) and probe the lines to isolate the fault.



Points A B		
Line	DC Voltage	DC Voltage Range
Active	0V	0 to +0.6V
Inactive	+5V	+2.4 to +5.5V
Open	+1.5V	+1 to +2V

Use CA5D08 for ground reference.

Point C		
Line	DC Voltage	DC Voltage Range
Active	+12V	+6 to +12.5V
Inactive	–12V	–6 to –12.5V
Open	+1V	+0.5 to +1.5V

Use CA5D08 for ground reference.

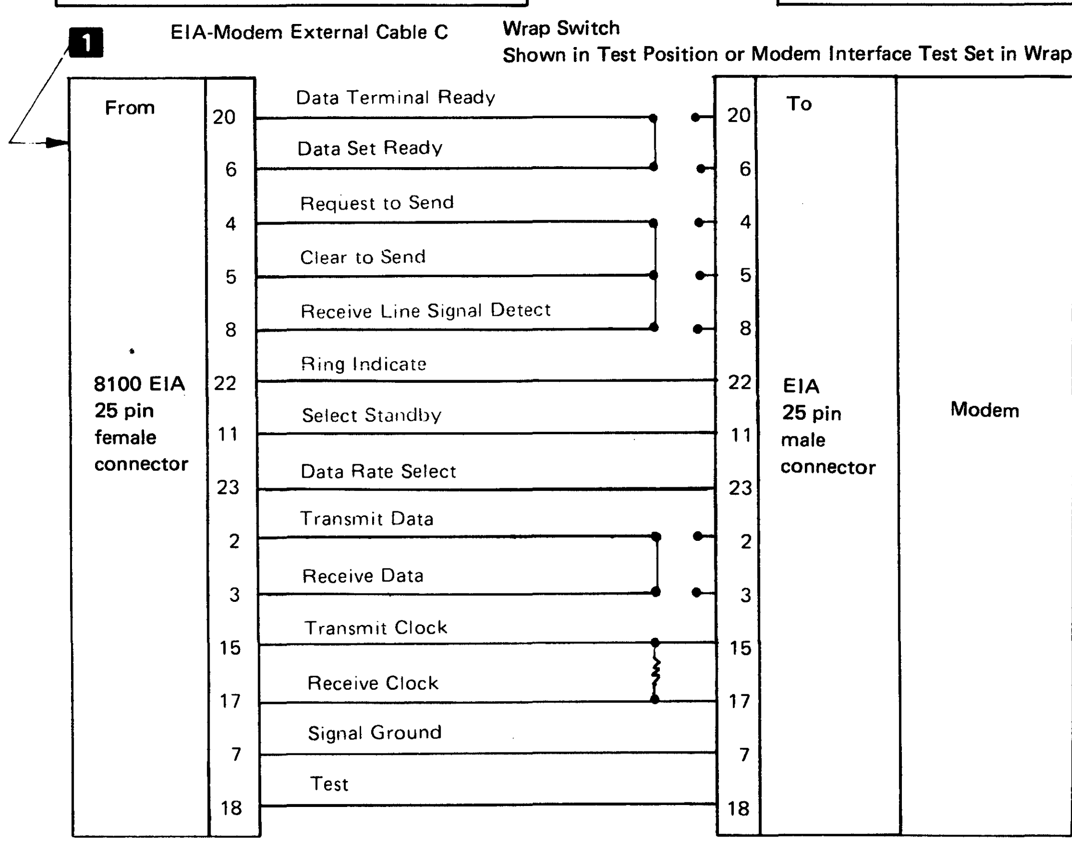


Figure CA545-1. Troubleshooting Diagram for Routine 63, EIA/Modem

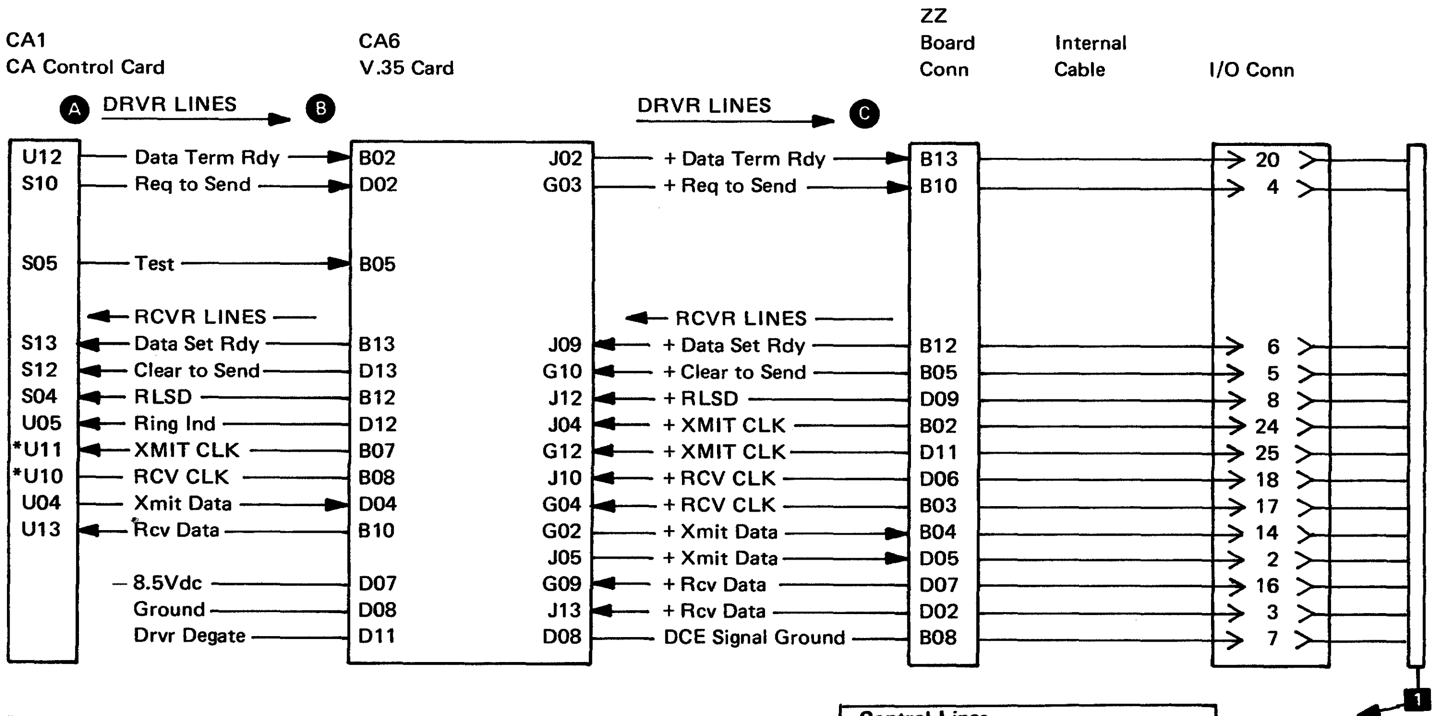
Expected Line Status

Error RREN	Test	Drivers					Receivers			
		DTR	RTS	NS	SSB	DRS	DSR	CTS	RLSD	RI
6311	I	I	I	I	I	I	I	I	I	I
6320	A	I	I	I	I	I	I	I	I	I
6321	I	I	I	I	I	I	I	I	I	I
6322	I	I	I	I	A	I	I	I	I	I
6323	I	I	I	I	I	I	I	I	I	I
6324	I	I	I	A	I	I	I	I	I	I
6325	I	I	I	I	I	I	I	I	I	I
6326	I	I	I	I	I	A	I	I	I	I
6327	I	I	I	I	I	I	I	I	I	I
6330	I	A	I	I	I	I	A	I	I	I
6331	I	I	I	I	I	I	I	I	I	I
6333	I	I	A	I	I	I	I	A	A	I
6340	I	I	A	I	I	I	I	A	A	I
6341	I	I	I	I	I	I	I	I	I	I
6380	I	A	A	I	I	I	A	A	A	I
6381	I	I	I	I	I	I	I	I	I	I
6390	I	There is data on the Xmit Data line; XMIT CLK and RCV CLK are present.					There is data on the Rcv Data line; XMIT CLK and RCV CLK are present.			

Legend:

- A = Active
- I = Inactive
- RR = Routine number
- EN = Error number

Caution: The modem must remain connected for successful test completion; clocking must be received by the 8100 for data path testing.



*May be multispeed clock source; see CA563.

Points A B		
Line	DC Voltage	DC Voltage Range
Active	0V	0 to +0.6V
Inactive	+5V	+2.4 to +5.5V
Open	+1.5V	+1 to 2V
Use CA6D08 for ground reference.		

Control Lines		
Active	−6.0V dc	±1.2V
Inactive	+6.0V dc	±1.2V
Reference Ground		
Data and Clock		
Active	−0.5V dc	±0.1V
Inactive	+0.5V dc	±0.1V
Measured between the balanced pair		
Use CA6D08 for ground reference.		

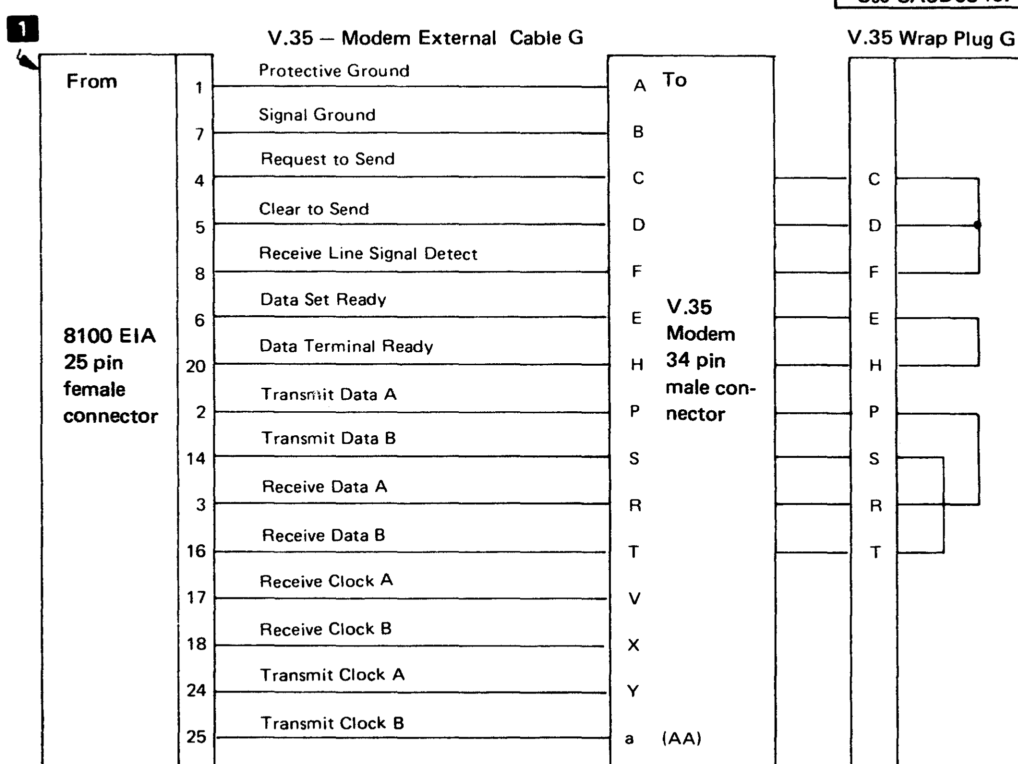


Figure CA545-2. Troubleshooting Diagram for Routine 63, V.35/Modem

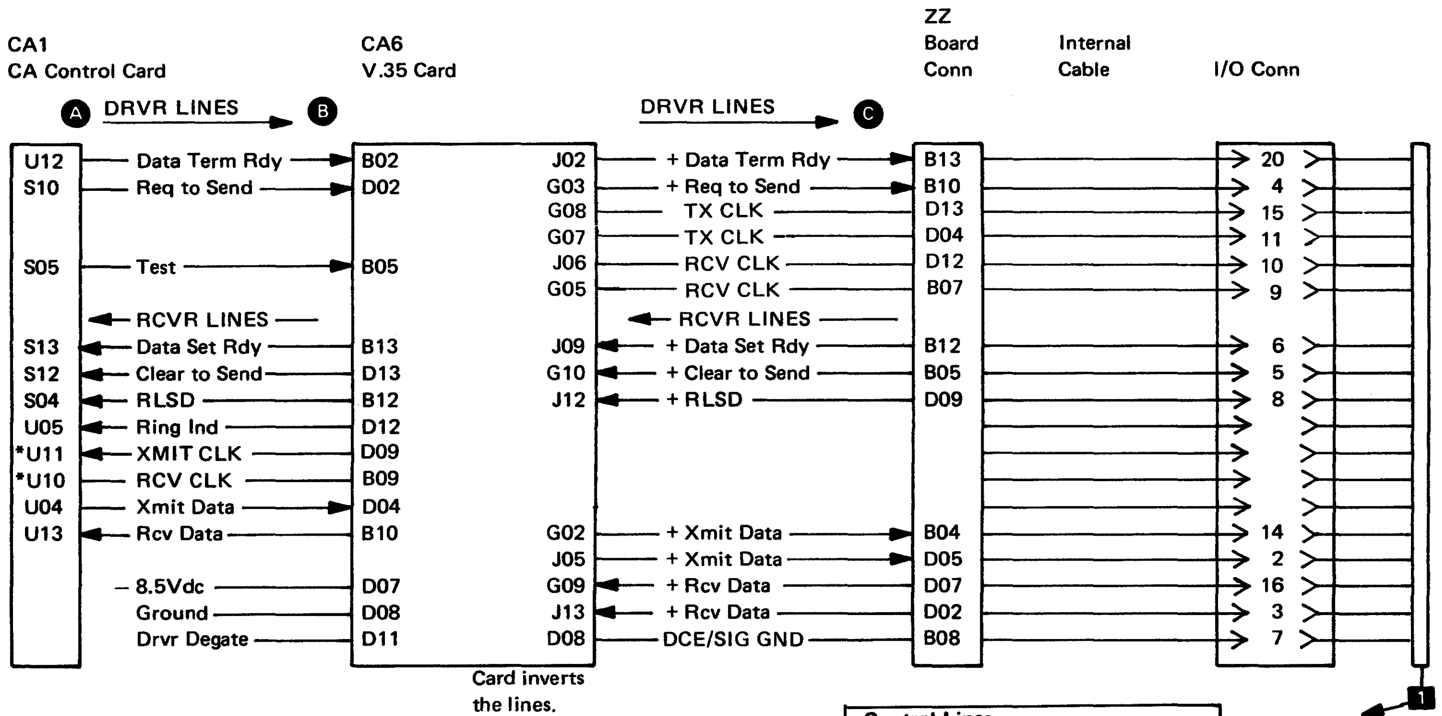
Expected Line Status

Error		Drivers					Receivers			
RREN	Test	DTR	RTS	NS	SSB	DRS	DSR	CTS	RLSD	RI
6311	I	I	I	I	I	I	I	I	I	I
6320	A	I	I	I	I	I	I	I	I	I
6321	I	I	I	I	I	I	I	I	I	I
6322	I	I	I	I	A	I	I	I	I	I
6323	I	I	I	I	I	I	I	I	I	I
6324	I	I	I	A	I	I	I	I	I	I
6325	I	I	I	I	I	I	I	I	I	I
6326	I	I	I	I	I	A	I	I	I	I
6327	I	I	I	I	I	I	I	I	I	I
6330	I	A	I	I	I	I	A	I	I	I
6331	I	I	I	I	I	I	I	I	I	I
6333	I	I	A	I	I	I	I	A	A	I
6340	I	I	A	I	I	I	I	A	A	I
6341	I	I	I	I	I	I	I	I	I	I
6380	I	A	A	I	I	I	A	A	A	I
6381	I	I	I	I	I	I	I	I	I	I
6390		There is data on the Xmit Data line; XMIT CLK and RCV CLK are present.					There is data on the Rcv Data line; XMIT CLK and RCV CLK are present.			

Legend:

- A = Active
- I = Inactive
- RR = Routine number
- EN = Error number

Caution: For V.35, the data path is tested only if the 8100 provides clock.



*May be multispeed clock source; see CA563.

Points A B		
Line	DC Voltage	DC Voltage Range
Active	0V	0 to +0.6V
Inactive	+5V	+2.4 to +5.5V
Open	+1.5V	+1 to +2V
Use CA6D08 for ground reference.		

Control Lines		
Active	–6.0V dc	±1.2V
Inactive	+6.0V dc	±1.2V
Reference Ground		
Data and Clock		
Active	–0.5V dc	±0.1V
Inactive	+0.5V dc	±0.1V
Measured between the balanced pair		
Use CA6D08 for ground reference.		

V.35/Direct Connect Terminal External Cable J

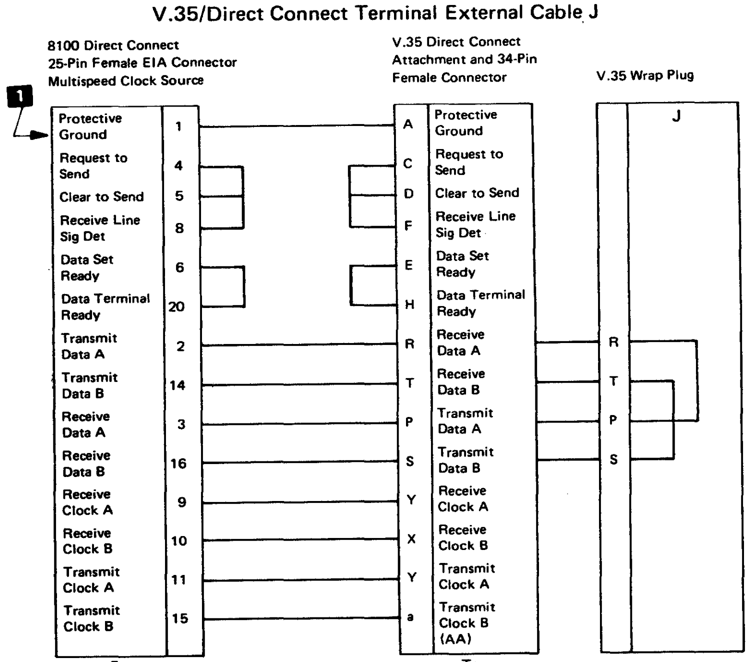


Figure CA545-3. Troubleshooting Diagram for Routine 63, V.35/ Direct Connect Terminal

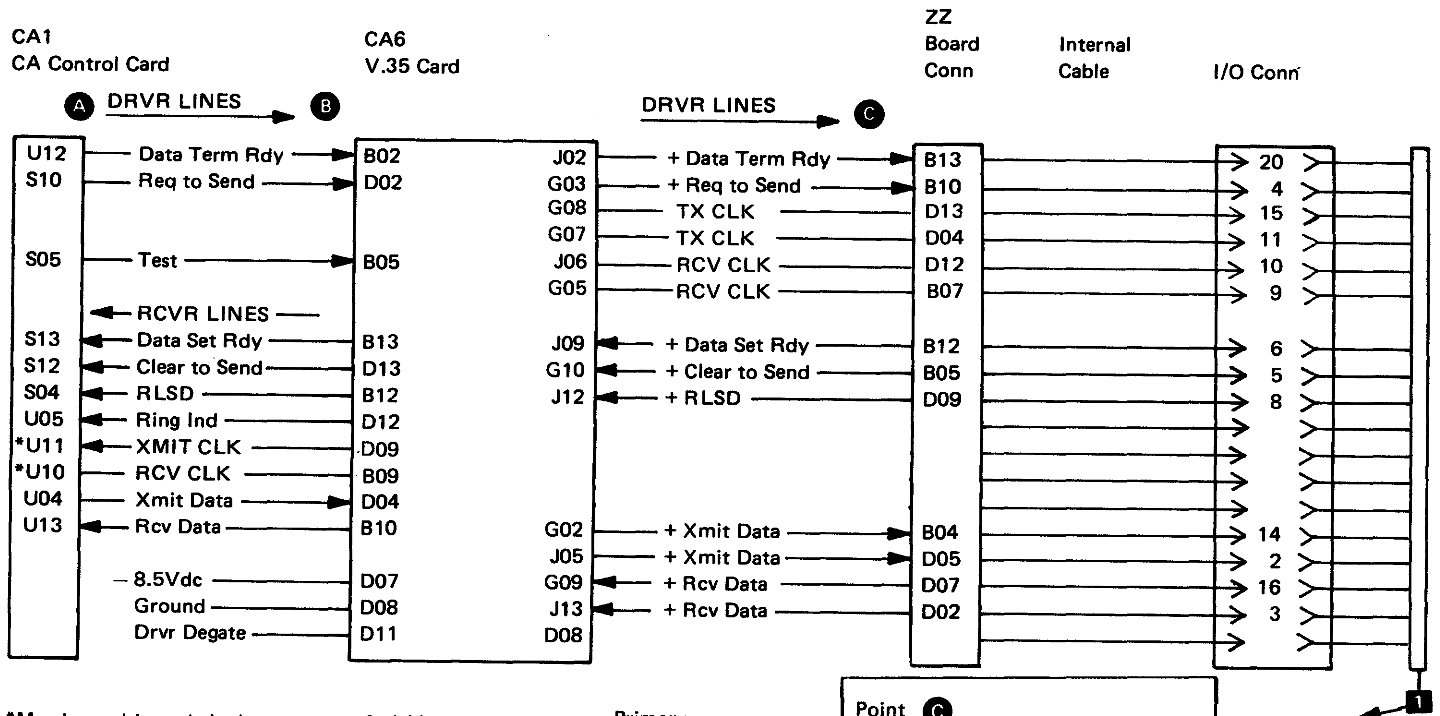
Expected Line Status

Error RREN	Test	Drivers					Receivers			
		DTR	RTS	NS	SSB	DRS	DSR	CTS	RLSD	RI
6311	I	I	I	I	I	I	I	I	I	I
6320	A	I	I	I	I	I	I	I	I	I
6321	I	I	I	I	I	I	I	I	I	I
6322	I	I	I	I	A	I	I	I	I	I
6323	I	I	I	I	I	I	I	I	I	I
6324	I	I	I	A	I	I	I	I	I	I
6325	I	I	I	I	I	I	I	I	I	I
6326	I	I	I	I	I	A	I	I	I	I
6327	I	I	I	I	I	I	I	I	I	I
6330	I	A	I	I	I	I	A	I	I	I
6331	I	I	I	I	I	I	I	I	I	I
6333	I	I	A	I	I	I	I	A	A	I
6340	I	I	A	I	I	I	I	A	A	I
6341	I	I	I	I	I	I	I	I	I	I
6380	I	A	A	I	I	I	A	A	A	I
6381	I	I	I	I	I	I	I	I	I	I
6390	I	There is data on the Xmit Data line; XMIT CLK and RCV CLK are present.					There is data on the Rcv Data line; XMIT CLK and RCV CLK are present.			

Legend:

A = Active
I = Inactive
RR = Routine number
EN = Error number

Caution: For V.35, the data path is tested only if the 8100 provides clock.



*May be multispeed clock source; see CA563.

Primary
Peer to Peer

Points A B		
Line	DC Voltage	DC Voltage Range
Active	0V	0 to +0.6V
Inactive	+5V	+2.4 to +5.5V
Open	+1.5V	+1 to +2V
Use CA6D08 for ground reference.		

Point C

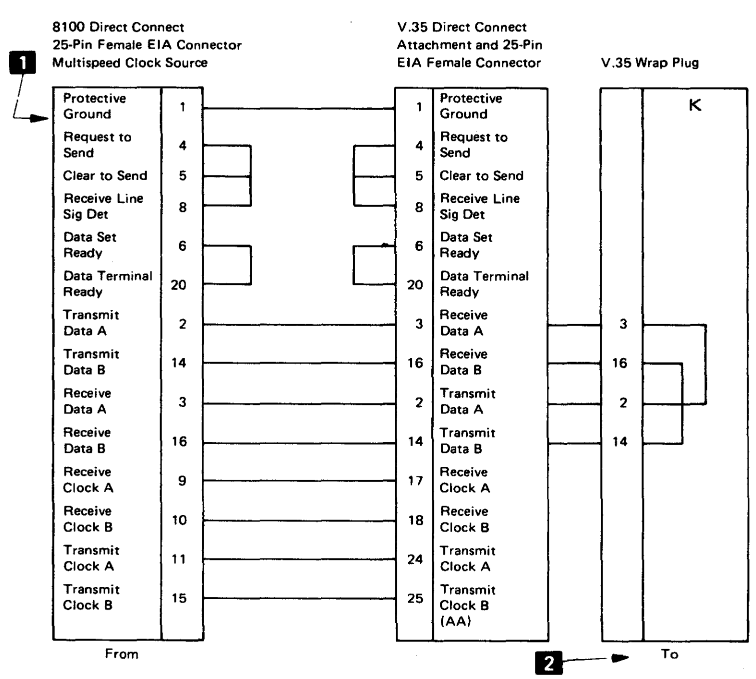
Control Lines		
Active	−6.0V dc	±1.2V
Inactive	+6.0V dc	±1.2V
Reference Ground		
Data and Clock		
Active	−0.5V dc	±0.1V
Inactive	+0.5V dc	±0.1V
Measured between the balanced pair		
Use CA6D08 for ground reference.		

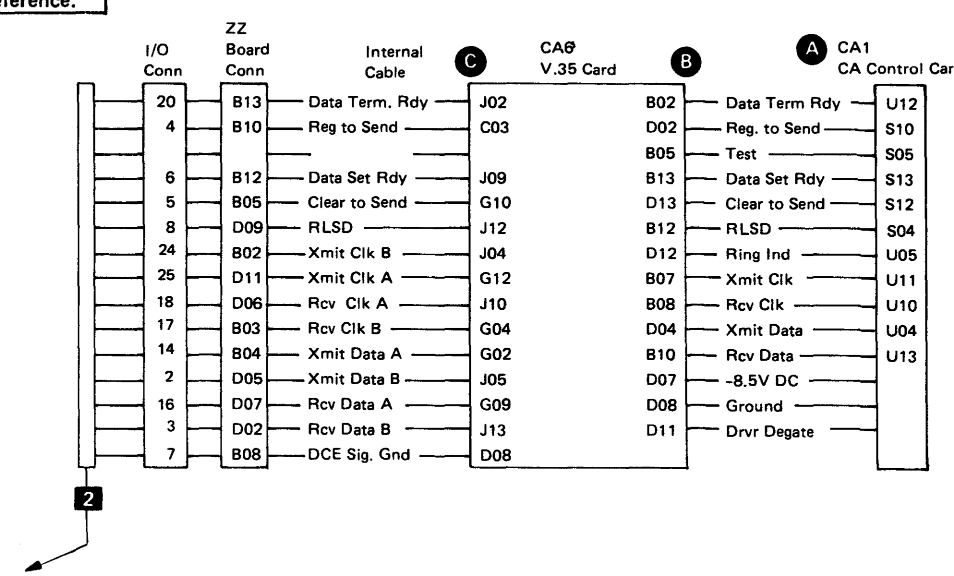
Expected Line Status

Error RREN	Test	Drivers DTR	RTS	NS	SSB	DRS	Receivers DSR	CTS	RLSD	RI
6311	I	I	I	I	I	I	I	I	I	I
6320	A	I	I	I	I	I	I	I	I	I
6321	I	I	I	I	I	I	I	I	I	I
6322	I	I	I	I	A	I	I	I	I	I
6323	I	I	I	I	I	I	I	I	I	I
6324	I	I	I	A	I	I	I	I	I	I
6125	I	I	I	I	I	I	I	I	I	I
6326	I	I	I	I	I	A	I	I	I	I
6327	I	I	I	I	I	I	I	I	I	I
6330	I	A	I	I	I	I	A	I	I	I
6331	I	I	I	I	I	I	I	I	I	I
6333	I	I	A	I	I	I	I	A	A	I
6340	I	I	A	I	I	I	I	A	A	I
6341	I	I	I	I	I	I	I	I	I	I
6380	I	A	A	I	I	I	A	A	A	I
6381	I	I	I	I	I	I	I	I	I	I
6390	I	There is data on the Xmit Data line; XMIT CLK and RCV CLK are present.					There is data on the Rcv Data line; XMIT CLK and RCV CLK are present.			

Legend:
A = Active
I = Inactive
RR = Routine number
EN = Error number

V.35/Direct Connect Peer-to-Peer External Cable K





Caution: For V.35, the data path is tested only if the 8100 provides clock.

V.35 Direct Connect — Peer to Peer Installations

Designation	FAC	Clock Type	Cable End Label	Wrap Plug
Primary	24 25	Adapter W/Clk Multispeed Clk Cd	"From" "K"	"K" At "To" end
Secondary	27	None	"To" "K"	"K" At "From" end

Figure CA545-4. Troubleshooting Diagram for Routine 63, V.35/Direct Connect, Peer-to-Peer

CA546 Routines 67 and 68 Troubleshooting Diagram

Caution: Routines 67 and 68 do not run under a DPCX operating system.

General. Figure CA546-1 is a troubleshooting diagram for use with Routines 67 and 68 and any necessary probing to provide the information for fault isolation of the X.21 feature. Data line wrap-testing occurs at the 8100 external communications cable. The routines determine and report the data line(s) in error that you can probe for fault isolation. The figure provides probe points and voltage levels for this feature.

Equipment Required

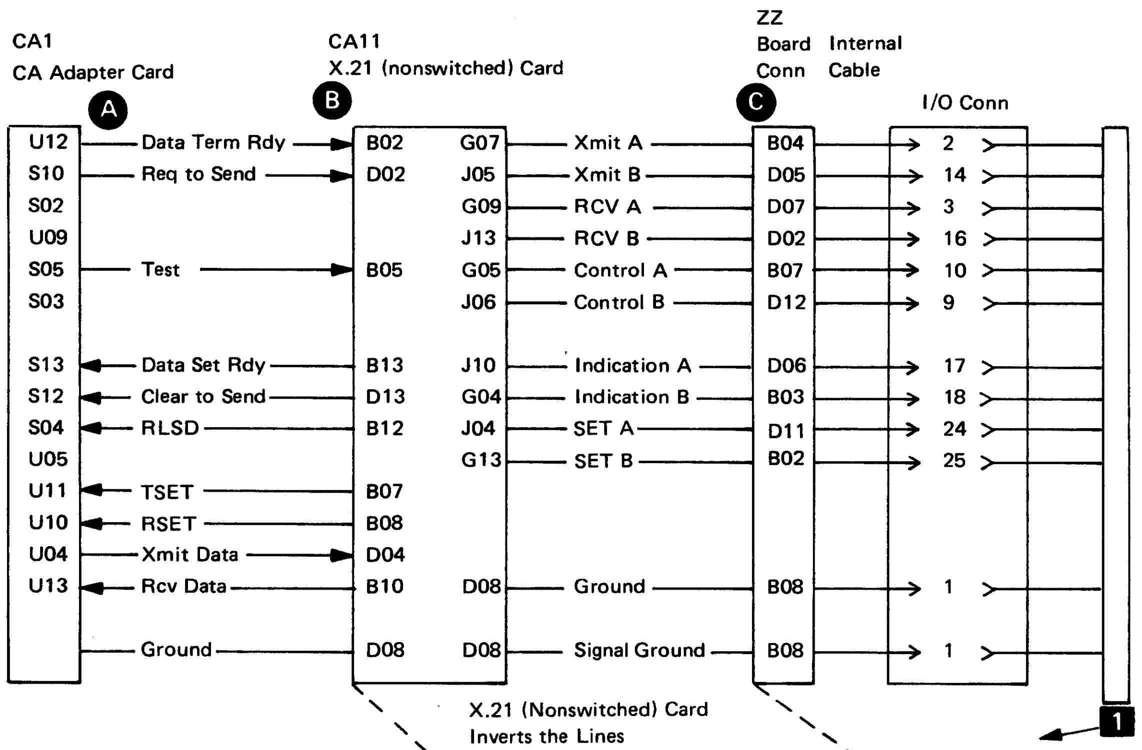
1. X.21 external cable.
2. CA MD diskette 02.
3. General logic probe, or oscilloscope, or volts/ohmmeter (VOM).

Test Description. See CA212 Routines 67 and 68. These test routines can be run under MAP control (offline) or invoked free-lance (offline).

Card Locations. See CA513 for card locations.

Test Procedure. You can enter this section under MAP control or under free-lance mode. If under MAP control go to step 2; if under free-lance mode, go to step 1.

1. Prepare to invoke Routine 67 or 68. Load the TCM (offline) (see CP810 in Chapter 2). The monitor must be at 80BC wait stop.
2. Prepare for test. If the cable has a wrap switch, set the Test/Operate switch to the Test position. If the cable does not have a wrap switch, set Test Switch 1 on the X.21 DCE to the On position.
3. Run Routine 67 or 68. If the routine is to run under MAP control, press the FWD key on the MD to run the test. If under free-lance mode, enter the invocation message; for Routine 67, use PAB 0067B, for Routine 68, use PAB 0068B, using the appropriate offline test invocation procedure (see CP462 in Chapter 2).
4. Review the test results. If the routine ran under MAP control, the MAP reviews the results and directs any necessary action. If the routine ran under free-lance mode, review the test message; if a Routine 67 or 68 error has occurred, you can identify the lines in error (see Routine 67 or 68 (Description, CA212, and Test Messages, CA230) and probe the data lines to isolate the fault.



Points A B		
Line	DC Voltage	DC Voltage Range
Active	0V	0 to +0.6V
Inactive	+5V	+2.4 to +5.5V
Open	+1.5V	+1 to +2V
Use CA 11 D08 for ground reference.		

Note: *Clocking is always provided by the network on SET A and SET B.*

Point C	
Line Pair	Voltage Difference between Line A and Line B
<u>Transmit Data</u>	
Space	$V_A - V_B > +2.0$ V dc
Mark	$V_A - V_B < -2.0$ V dc
<u>Control</u>	
On	$V_A - V_B > +2.0$ V dc
Off	$V_A - V_B < -2.0$ V dc
<u>Receive Data</u>	
Space	$V_A - V_B > +2.0$ V dc
Mark	$V_A - V_B < -2.0$ V dc
<u>Signal Element Timing</u>	
On	$V_A - V_B > +0.2$ V dc
Off	$V_A - V_B < -2.0$ V dc
<u>Indication</u>	
On	$V_A - V_B > +0.2$ V dc
Off	$V_A - V_B < -0.2$ Vdc

Legend:
> = greater than
< = less than

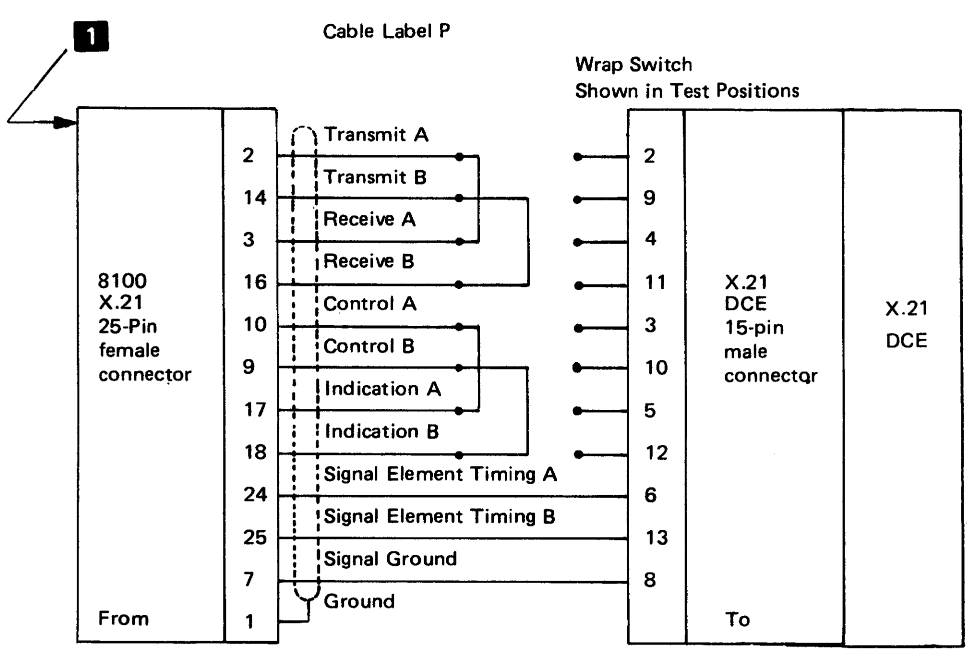


Figure CA546-1. Troubleshooting Diagram for Routine 67 and 68, X.21 (Nonswitched) External Data Wrap

Routine 67
Expected Line Status

Error RREN	Test	Drivers		Receivers		
		DTR	RTS	DSR	CTS	RLSD
671C	I	A	A	A	A	A
				Data on Transmit Data on Receive		

Routine 68
Expected Line Status

Error RREN	Test	Drivers					Receivers		
		DTR	RTS	SS	NS	DRS	DSR	CTS	RLSD
6811	I	I	I	I	I	I	A	I	I
6820	A	I	I	I	I	I	A	I	I
6821	I	I	I	I	I	I	A	I	I
6822	I	I	I	A	I	I	A	I	I
6823	I	I	I	I	I	I	A	I	I
6824	I	I	I	I	A	I	A	I	I
6825	I	I	I	I	I	I	A	I	I
6826	I	I	I	I	I	A	A	I	I
6827	I	I	I	I	I	I	A	I	I
6830	I	A	I	I	I	I	A	I	I
6831	I	I	I	I	I	I	A	I	I
6833	I	I	A	I	I	I	A	A	A
6840	I	I	A	I	I	I	A	A	A
6841	I	I	I	I	I	I	A	I	I
6880	I	A	A	I	I	I	A	A	A
6881	I	I	I	I	I	I	A	I	I
6890	I	I	I	I	I	I	A	I	I
	Data on Transmit and Receive Data lines; clocks are present.								

Legend:
A = Active
I = Inactive
RR = Routine number
EN = Error number

CA547 Routine 66 Troubleshooting Diagram

Caution: Routine 66 does not run under DPCX.

General. Figure CA547-1 is a troubleshooting diagram for use with Routine 66 and any necessary probing to provide the information for fault isolation of the DDS feature. Data line wrap-testing occurs at the 8100 external communications cable. The routine determines and reports the data line(s) in error that you can probe for fault isolation. The figure provides probe points and voltage levels for this feature.

Equipment Required

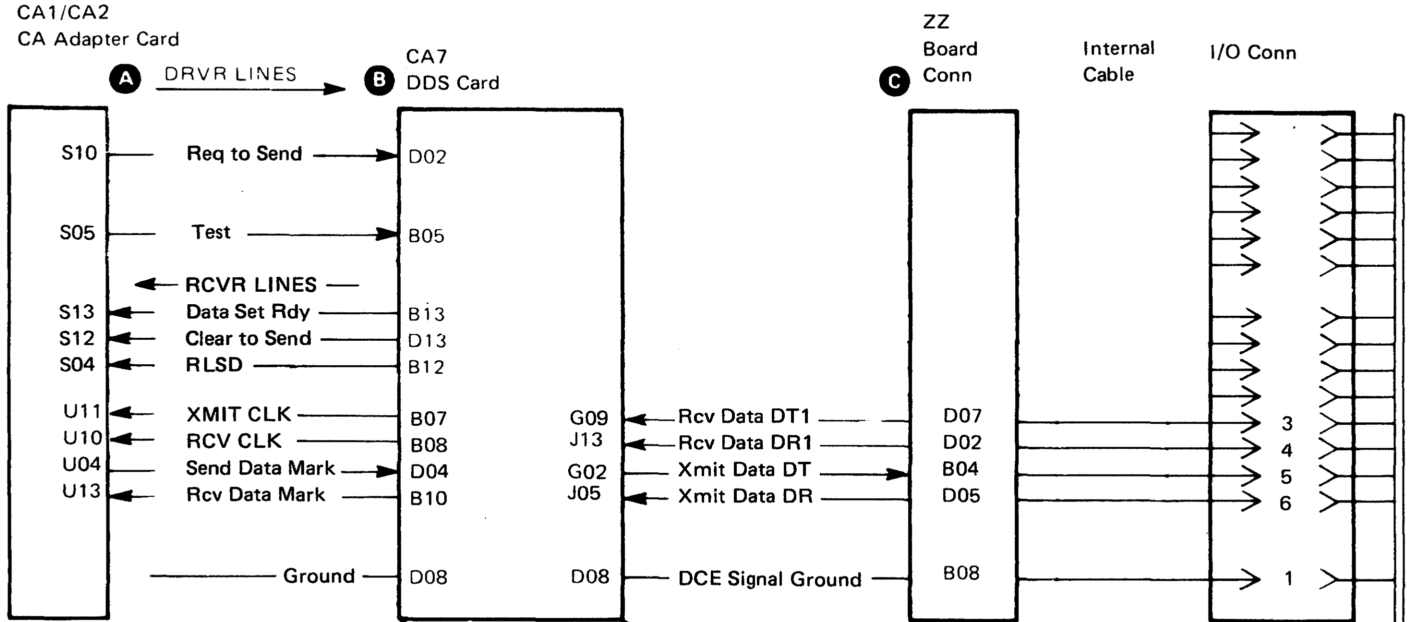
1. **DDS wrap plug F or external cable F.**
2. **CA MD diskette 02.**
3. General logic probe, or oscilloscope, or volt/ohmmeter (VOM).

Test Description. See CA212, Routine 66. This test routine can be run under MAP **control (offline or online) or invoked free-lance (offline).**

Card Locations. See CA513 for card locations.

Test Procedure. You can enter this section under MAP control or under free-lance mode. If under MAP control go to step 2; if under free-lance mode, go to step 1.

1. **Prepare to invoke Routine 66. Load the TCM (offline) (see CP810 in Chapter 2). The monitor must be at 80BC wait stop.**
2. Prepare the external cable for test. If you have a wrap plug, install the plug at the extreme end of the 8100 DDS external cable. If you have an external cable with a Test/Operate switch installed on the extreme end, set the switch to Test position.
3. Run Routine 66. If under MAP control, press the FWD key on the MD to run the test. If under free-lance mode, enter the invocation message (PA 0066B) using the **appropriate online/offline test invocation procedure (see CP462 in Chapter 2).**
4. Review the test results. If under MAP control, the MAP reviews the results and directs any necessary action. If under free-lance mode, review the test message; if a Routine 66 error has occurred, you can identify the lines in error (see Routine 66 Description, CA212, and Test Messages, CA230) and probe the data lines to isolate the fault.



Points A B

Line	DC Voltage	DC Voltage Range
Active	0V	0 to +0.6V
Inactive	+5V	+2.4 to +5.5V
Open	+1.5V	+1 to +2V

Use CA7D08 for ground reference.

Point C

Line	DC Voltage Range
XMIT DATA	
ONE	+ 1.4 to + 2.1V
ZERO	+ 0.0 to + 0.14V
RCV DATA	
ONE	+ 1.05 to + 2.1V
ZERO	+ 0.0 to + 0.35V

Use CA7D08 for ground reference.

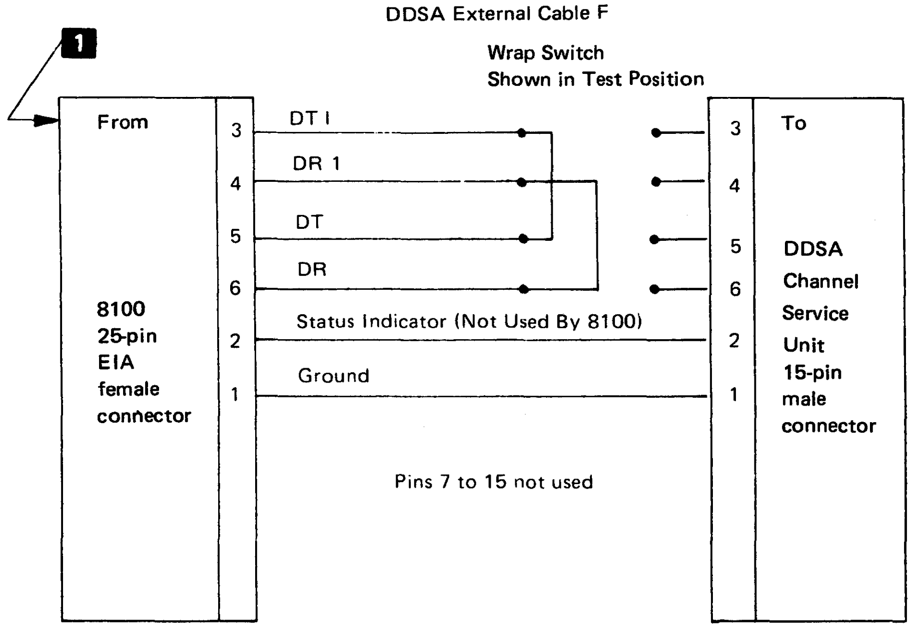


Figure CA547-1. Troubleshooting Diagram for Routine 66, DDS External Data Wrap

Expected Line Status

Error		Drivers					Receivers			
RREN	Test	DTR	RTS	NS	SSB	DRS	DSR	CTS	RLSD	RI
66XX	I	I	I	I	I	I	I	I	I	I
6633	I	A	A	I	I	I	A	A	I	I
6690	I	A	A	I	I	I	A	A	I	I
							Data on Xmit and Receive lines			

Legend:

A = Active
I = Inactive
RR = Routine number
EN = Error number

CA548 Routine 16 Troubleshooting Diagram

Caution: This section should only be used when an IBM modem is attached to the EIA modem feature, and only offline.

General. Figure CA548-1 is a troubleshooting diagram for use with Routine 16 and any necessary probing to provide the information needed for fault isolation between the CA feature and the IBM modem. This routine causes a data wrap to occur in the IBM modem after certain control lines (8100 and modem) are activated. The figure provides probe points, expected results, and voltage levels for the CA feature.

Equipment Required

1. CA MD diskette 02.
2. General logic probe, or oscilloscope, or volt/ohmmeter (VOM).

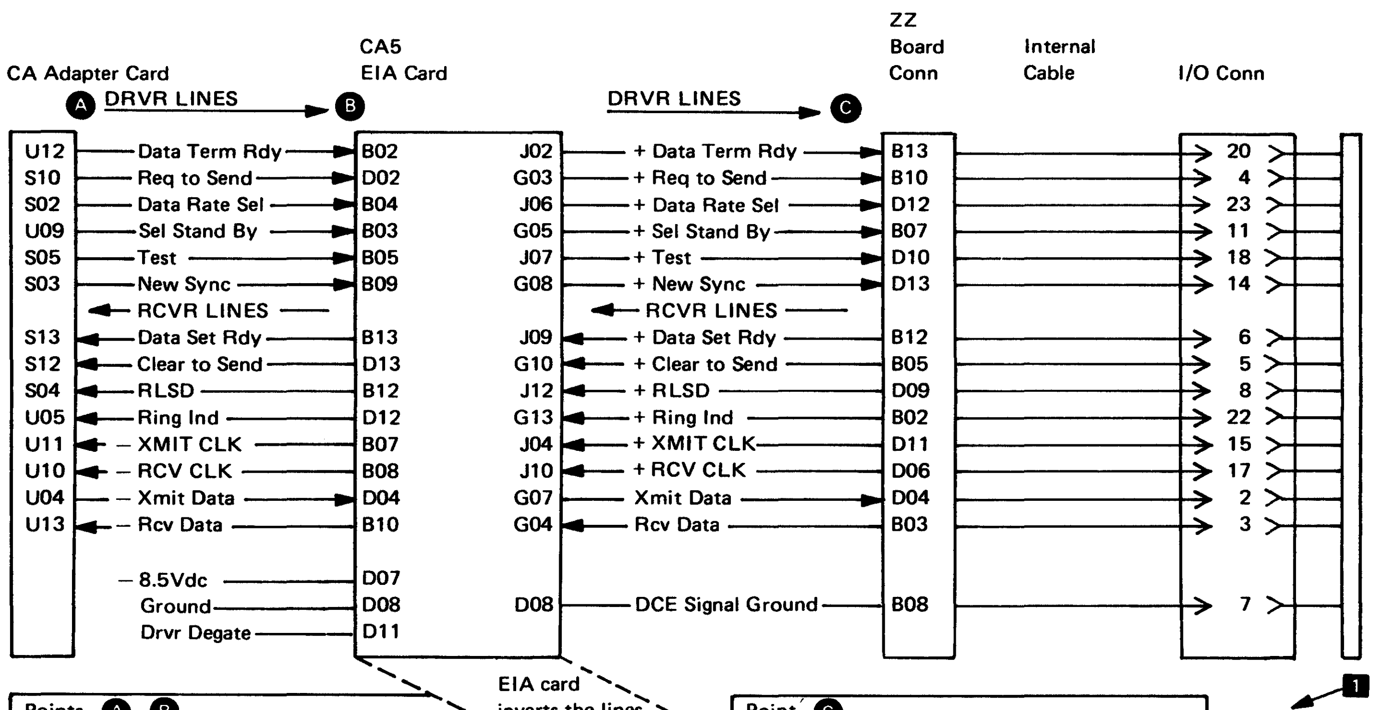
Test Description. See CA212, Routine 16. This test routine can be run under MAP control (offline) or invoked free-lance (offline).

Card Locations. See CA513 for card locations.

Test Procedure

Caution: Turn power off when removing or replacing cards or cables.

1. Locate and remove the EIA card for this PA/FAC. See CA513 for card locations.
2. Move the EIA card jumper from internal wrap to external wrap position. See CA563 for card jumpers.
3. Turn power on. If under MAP control, go to step 5; if under free-lance mode, go to step 4.
4. Prepare to invoke Routine 16. Load the Offline TCM (see CP810 in Chapter 2). The monitor must be at 80BC wait stop.
5. Run Routine 16. If under MAP control, press the FWD key on the MD to run the test. If under free-lance mode, enter the invocation message (PA B 0016B) using the appropriate offline test invocation procedure (see CP462 in Chapter 2).
6. Review the test results. If under MAP control, the MAP reviews the results and directs any necessary action. If under free-lance mode, review the test message if a Routine 16 error has occurred. Probe the control and data lines for expected line conditions (see the chart on Figure CA548-1). See Routine 16 Description, CA212, and Test Messages, CA230.



Points A B		
Line	DC Voltage	DC Voltage Range
Active	0V	0 to +0.6V
Inactive	+5V	+2.4 to +5.5V
Open	+1.5V	+1 to +2V

Use CA5D08 for ground reference.

Point C		
Line	DC Voltage	DC Voltage Range
Active	+ 12V	+6 to + 12.5V
Inactive	–12V	–6 to –12.5V
Open	+ 1V	+0.5 to +1.5V

Use CA5D08 for ground reference.

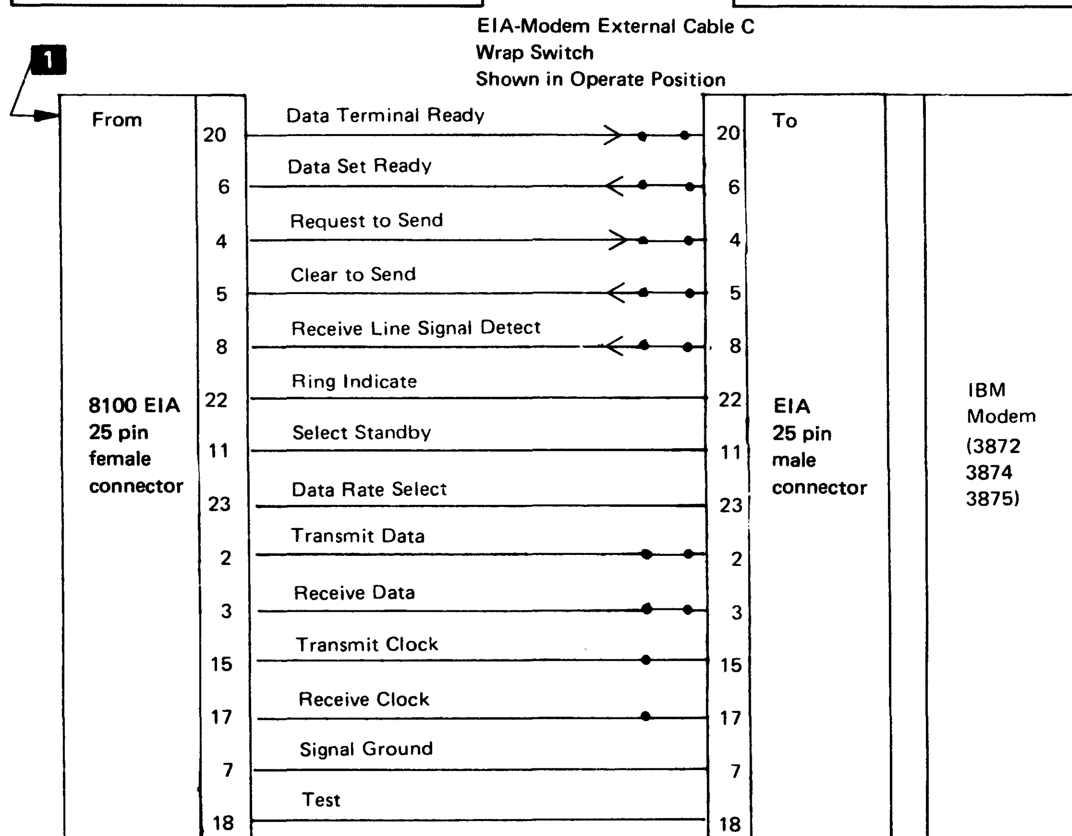


Figure CA548-1. Troubleshooting Diagram for Routine 16, EIA/Modem Data Wrap

Expected Line Status

Error RREN	Test	Drivers DTR	RTS	NS	SSB	DRS	Receivers DSR	CTS	RLSD	RI
161C	A	A	A	I	I	I	A	A	A	I
							Data on Transmit			
							Data on Receive			

Legend:

A = Active
I = Inactive
RR = Routine number
EN = Error number

CA550 Loop Troubleshooting Diagrams

General. Figures CA550-1, CA550-2, and CA550-3 are troubleshooting diagrams for use with Routine 18 and any necessary probing to provide information for fault isolation of the loop and second-lobe loop features. Control and data line wrap-testing occurs at the loop adapter card. The routine determines, reports, and holds the line(s) in error that you can probe for fault isolation. The figure provides probe points and voltage levels for the CA feature.

Equipment Required

1. CA MD diskette 02.
2. General logic probe, or oscilloscope, or volt/ohmmeter (VOM).

Test Description. See CA212, Routine 18. The test routine can be run under MAP control (offline or online) or invoked free-lance (offline).

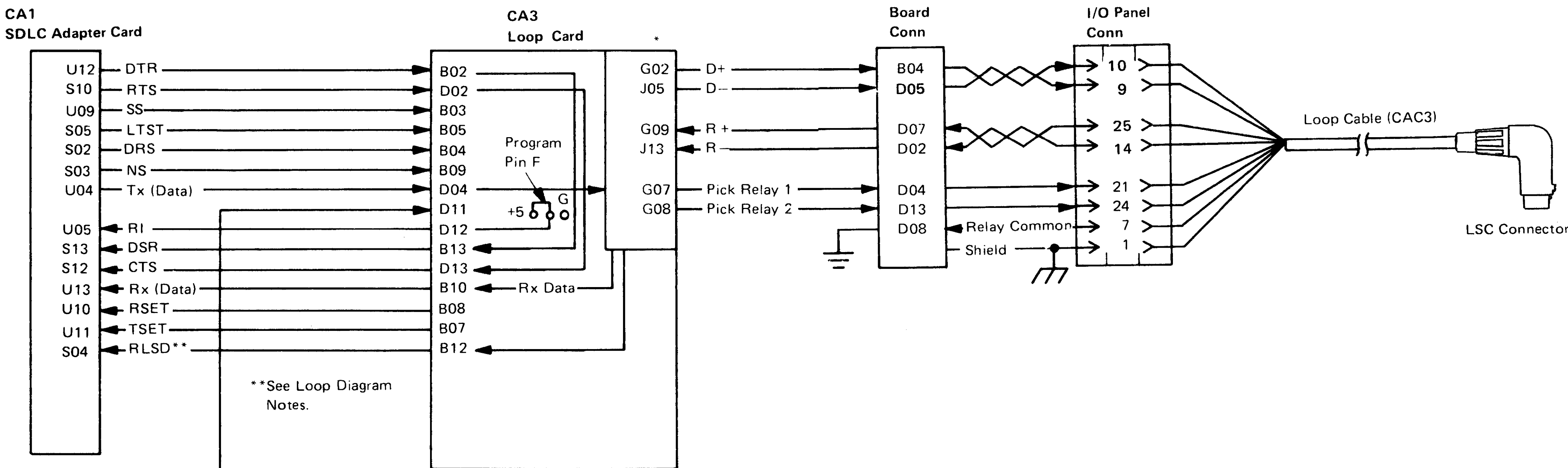
Card Locations. See CA513, for card locations.

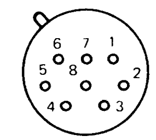
Test Procedure. You can enter this section under MAP control or under free-lance mode. If under MAP control, go to step 4; if under free-lance mode, go to step 1.

1. Prepare to invoke test 18. Load the TCM (offline) (see CP810 in Chapter 2). The monitor must be at 80BC wait stop.
2. Run Routine 18. In free-lance mode, enter the invocation message (PA 0018B) using the appropriate online/offline test invocation procedure (see CP462 in Chapter 2).
3. Review the test results. Under free-lance mode, review the test message; if a Routine 18 error has occurred, you must identify the lines in error. See Figure CA550-3 to compare test Routine 18 results with correct voltage levels; see Routine 18 description in CA212; see Test Messages in CA230; and probe the lines to isolate the fault.
4. Go to the appropriate signal path identification and locations selection for the loop feature:

   One-Lobe, Figures CA550-1 and CA550-3
   Two-Lobe, Figures CA550-2 and CA550-3

   Using the MAP results, probe the lines to isolate the fault.





Connector View

Line Name	Color	I/O Panel	LSC
Shield	–	1	**
D –	Red	10	2
D +	WHT	9	3
R –	ORN	25	4
R +	BLU	14	5
Pick R1	YEL	21	6
Pick R2	PUR	24	7
Relay Common	BLK	7	8

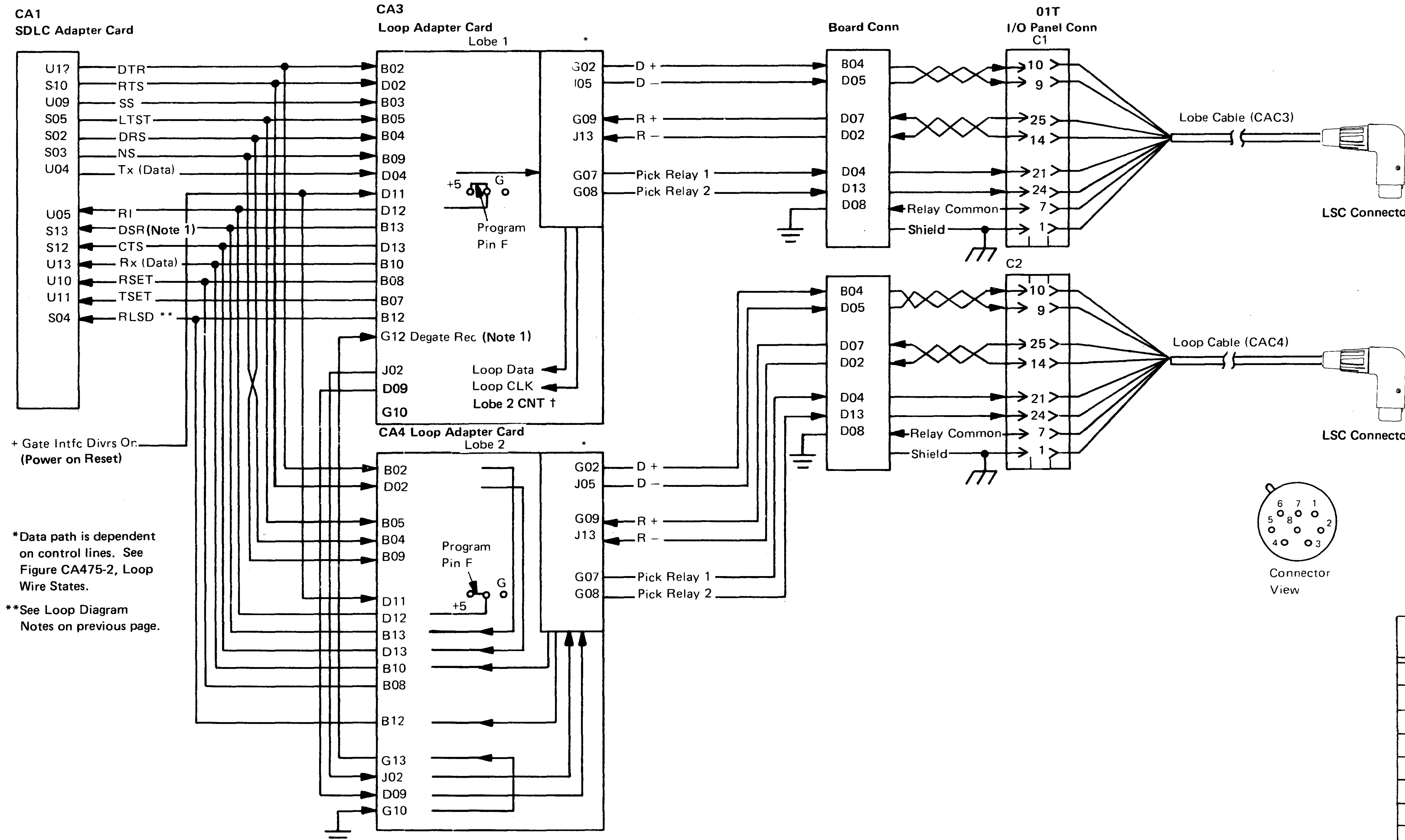
**No connection

Loop Diagram Notes

RLSD is dependent on the following line conditions:

1. One-lobe loop:
   a. Select standby CA3B03 = +2.4 to +5.5V
   b. Power-on reset CA3D11 = +2.4 to +5.5V
   c. Lobe 2 control CA3G10 = +2.4 to +5.5V
   d. Degate transmit I/O CA3G13 = +2.4 to +5.5V
   e. RLSD control CA3G04 = +2.4 to +5.5V
2. Two-lobe loop:
   a. Select standby CA3B03 = +2.4 to +5.5V
   b. Loop clock CA3D09 to CA4D09 = No fault
   c. Power-on reset CA3D11 and CA4D11 = +2.4 to +5.5V (gate intf drivers on)
   d. Lobe 2 control CA3G10 = +2.4 to +5.5V
   e. Degate transmit I/O CA3G13 = +2.4 to +5.5V
   f. Loop data CA3J02 to CA4J02 = No fault
   g. Carrier rates are set the same for both lobes.
   h. RLSD control CA3G04 and CA4G04 = +2.4 to +5.5V.

Figure CA550-1. Loop Troubleshooting Diagram for Test Routine 18, One Lobe



*Data path is dependent on control lines. See Figure CA475-2, Loop Wire States.

**See Loop Diagram Notes on previous page.

†Used in Lobe 2 (CA4 only). (See CA475-1.)

Line Name	Color	I/O Panel	LSC
Shield	–	1	**
D –	RED	10	2
D +	WHT	9	3
R –	ORN	25	4
R +	BLU	14	5
Pick R1	YEL	21	6
Pick R2	PUR	24	7
Relay Common	BLK	7	8

**No connection

Note 1: *DSR is dependent on pin G12, Degate Receive, being at ground level.*

Figure CA550-2. Loop Troubleshooting Diagram for Test Routine 18, Two Lobe

Routine 18 Results. When an error occurs, Routine 18 holds the drive lines to permit fault isolation. Figure CA550-3 gives the correct levels for each error number.

RREN	Drive Lines						Receive Lines				Relays			
											Lobe 1		Lobe 2	
	LTST	DRS	NS	RTS	DTR	SS	CTS	DSR	RLSD	RI	R1	R2	R1	R2
1831	I	I	I	I	I	A	I	I	I	I	–	–	–	–
1832	I	I	I	I	A	A	I	A	I	I	–	–	–	–
1833	I	I	I	I	A	I	I	A	A	I	–	–	–	–
1834	I	I	I	A	A	I	A	A	A	I	–	–	–	–
1835	I	I	I	I	I	I	I	I	A	I	On	On	On	On
1836	A	I	A	I	I	I	I	I	A	I	Off	Off	On	Off
1837	A	A	I	I	I	I	I	I	A	I	On	Off	Off	Off
1838	A	I	I	I	I	I	I	I	A	I	Off	Off	Off	Off

A (Active) = 0 to +0.6V
I (Inactive) = +2.4 to +5.5V
On = +4.0 to +5.7V
Off = 0 to +0.6V
CTS = Clear to Send
DRS = Data Rate Select
DSR = Data Set Ready
DTR = Data Terminal Ready
LTST = Local Test
NS = New Sync
RI = Ring Indicate
RLSD = Receive Line Signal Detect (Carrier Detect)
RTS = Request to Send
R1 = Relay 1
R2 = Relay 2
SS = Select Standby

Figure CA550-3. Correct Voltage Levels and Relay Conditions for Routine 18

CA551 Routine 73 Relay Test Troubleshooting Procedure

General. Troubleshooting diagrams (Figures CA551-1, CA551-2, and CA551-3), routine 73, and probing provide the necessary information for fault isolation on the loop feature of the relays and the relay pick circuits. The routine sets and resets relay voltages for probing. The figures provide probe points, voltage levels, and sequences.

Equipment Required

1. CA MD diskette 02.
2. CE probe or CE meter.

Test Description. See CA212, Routine 73. The test routine may be run under MAP control (offline or online) or invoked free-lance (offline). The test is looped, permitting time to check all steps.

Locations

Board and Cable – CA520
I/O Panel – CA420

Test Procedure. This routine is entered under MAP control or free-lance. If under MAP control, go to step 2; if free-lance, go to step 1.

1. Prepare to invoke Routine 73. Load the TCM (offline) (see CP810 in Chapter 2). The monitor must be at the 80BC stop.
2. Remove the LSC connector from the LSC for the lobe to be tested.
3. Run Routine 73. If in MAP control, press the MD FWD key to start the test. If in free-lance mode, enter the invocation message (PA0173 and then B for begin) using the appropriate offline/online test invocation procedure (see CP462 in Chapter 2).
4. Probe pins on the LSC connector as shown in Figure CA551-2. Check voltage levels and sequences as shown in Figure CA551-3.
5. Review the test results. If in MAP control, the MAP requests the test results and directs any necessary action. If in free-lance mode, the following action is recommended:

   Voltages and sequences are correct:

   Restore the LSC connector to the LSC and:

   - If in an action plan, perform the next step.
   - If not in an action plan, end the repair action.

   Voltages or sequences are not correct:

   With Routine 73 looping, use the loop troubleshooting diagrams of CA550 and Figure CA551-1 to isolate the failing element.

Routine 73 Relay Test Troubleshooting Diagram.

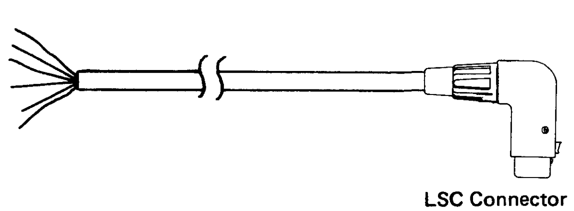
1. DTR must be active (0 to +0.6V) for the relays to function normally.
2. Each step lasts approximately 10 seconds.
3. See Figures CA550-1 (One-Lobe) and CA550-2 (Two-Lobe) for control line locations and LSC connector layout.

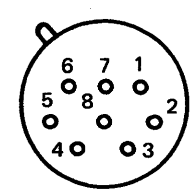
Step No.	Control Lines			Relay States			
				Lobe 1		Lobe 2	
	LTST	DRS	NS	R1	R2	R1	R2
1	A	I	A	OFF	OFF	ON	OFF
2	A	A	I	ON	OFF	OFF	OFF
3	I	A	A	ON	ON	ON	ON

		Min Max	
A (active)	=	0 to +0.6V	R1 = Relay 1
I (inactive)	=	+2.4 to +5.5V	R2 = Relay 2
On	=	+3.8 to +6.0V	
Off	=	0 to +0.6V	

Note: *Voltages are measured with respect to relay common.*

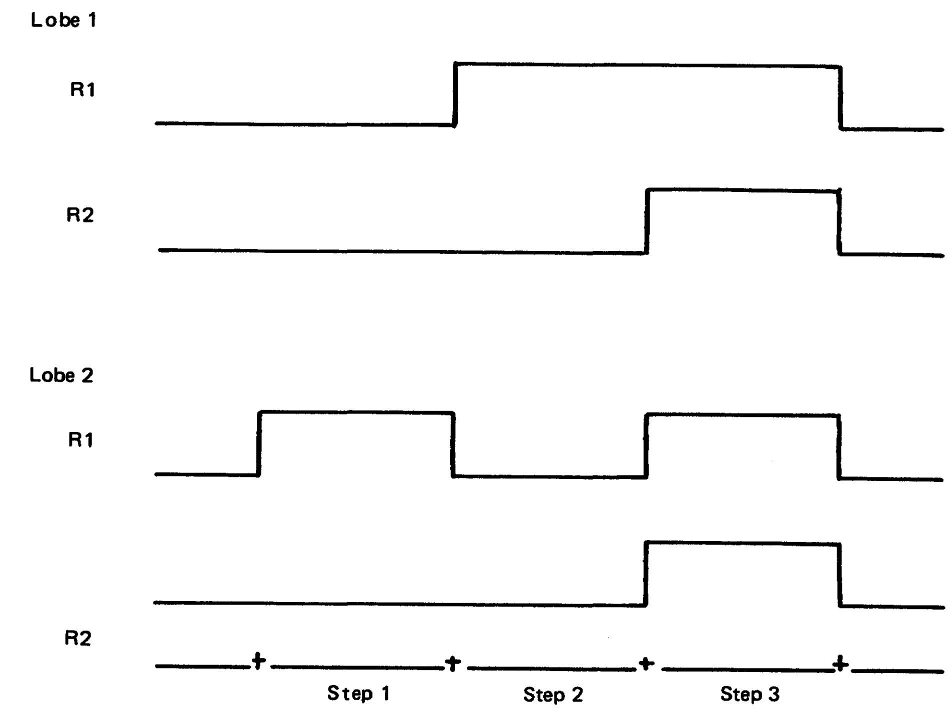
Figure CA551-1. Relay States





Line Name	Color	LSC Pin
Pick R1	Yellow	6
Pick R2	Purple	7
Relay Common	Black	8

Figure CA551-2. LSC Connector Pins and Wire Color



Note: *Voltages are measured with respect to relay common.*

Figure CA551-3. Relay Timing

CA560 Switches, Jumpers, and Straps

CA561 Switches

Integrated Modem Switches

These rotary switches are located on the I/O panels of the 8101, 8130, and 8140 units (U.S./Canada) and serve the function of setting a switched network data links transmit level. In WTC, the transmit level setting is performed by integrated modem card switches (See CA563). The rotary switches are labeled by part number, and switch level setting positions are in dbm (1 dB steps). The U.S. procedure for the transmit level adjustment is CA581. The WTC procedure for the transmit level adjustment is in CA711.

Loop Switches

Minimum manual intervention is normally required for operation of the loop accessories. Accessory switches that can be used for test and isolation of loop problems are described in this section.

Wrap Loop Station Connector (LSC). On the front of the wrap LSC are two indicators and two keyholes to set and restore the wrap state of the loop at that LSC. The key-actuated wrap switches provide protection from inadvertent operation (see Figure CA561-1).

To gain access to these wrap switches, swing the switch cover in the direction of the arrow on the cover until the keyholes and indicators are accessible. Then check the indicator holes to determine the condition of the wrap switches. If both holes display the color black, the LCS is in a normal state, no wrapping. If one of the indicators displays the color white, the LCS is wrapped in that direction. If both switches are in the wrapped position (both indicators displaying the color white), the device connected to that LSC will not operate on the loop. Figure CA561-2 shows an LSC wrapped both left and right.

To wrap the loop at the LSC, insert the key into the upper keyhole and turn the key in the direction in which the loop is to be wrapped. The corresponding indicator hole will display the color white.

To restore the system to a normal (not-wrapped state), insert the key into the restore (lower) keyhole and turn it toward the indicator displaying the color white, until the indicator color is black. Now the LSC is in a normal (not-wrapped) condition. Figure CA561-1 summarizes the wrap and restore operations.

Loop Wiring Concentrator (LWC). The LWC has a switch panel behind a door at the lower center of the unit. This panel contains wrap switches for the LWC and bypass switches for each of the eight ports to which a radial loop cable can be attached. Figure CA561-3 shows this switch panel. To gain access to the switches, push the black door in and up and then insert the key in the keyhole at the edge of the inner door and turn in the direction of the arrow.

To wrap the LWC, move the appropriate wrap switch on the panel to the position indicating a wrap state, switch pointing up (see Figure CA561-3). To restore the LWC to its normal state, return the switch to the not-wrapped position, switch pointing down.

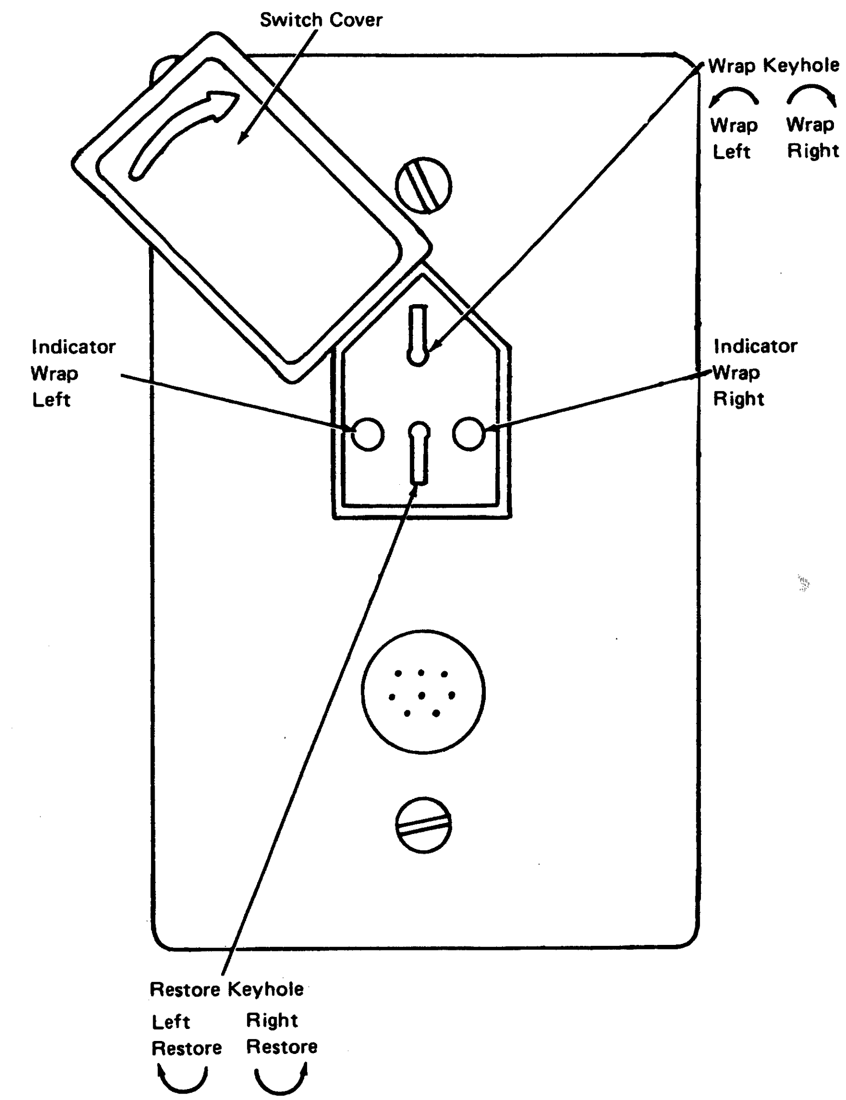


Figure CA561-1. Wrap Operation on Wrap Loop Station Connector

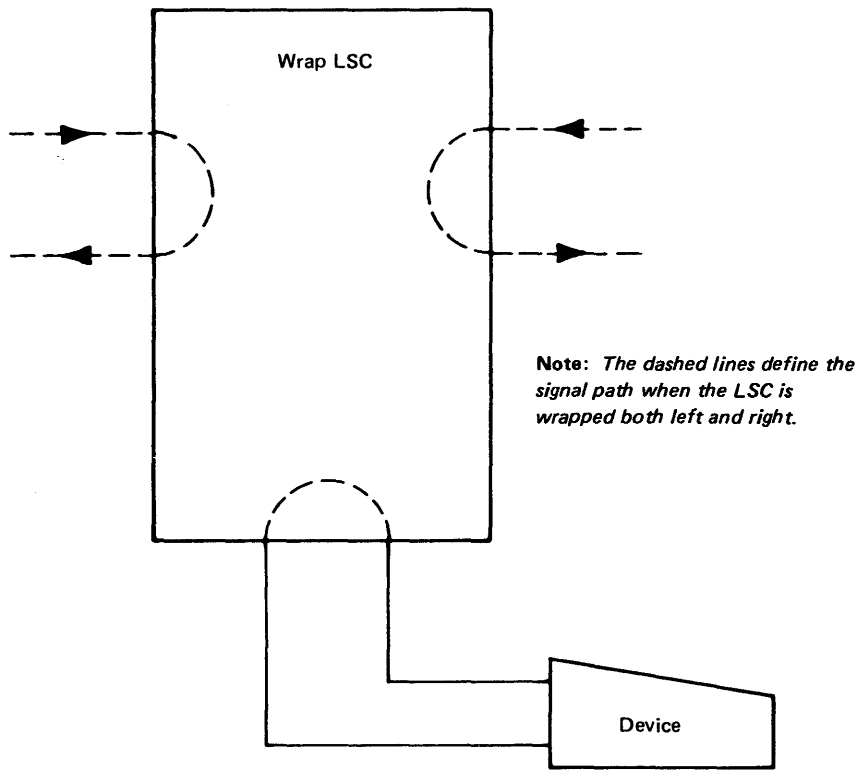


Figure CA561-2. LSC Wrapped Left and Right

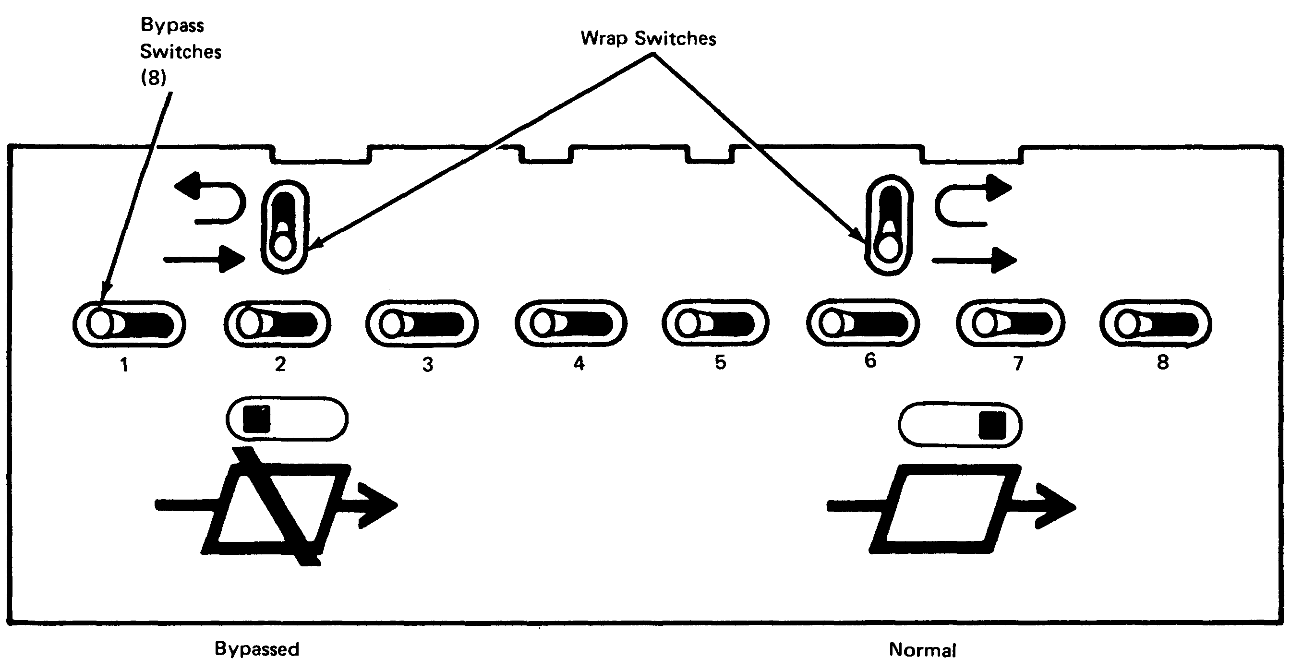


Figure CA561-3. Loop Wiring Concentrator (LWC) Switches

To bypass one of the radial lines from the LWC, move the switch corresponding to that radial port on the LWC to the left (bypassed) position. In this position, the radial cable and LSC are disconnected from the loop. When the radial line is to be reconnected to the loop, move the corresponding bypass switch to the right (not-bypassed) position. In this position, the device attached to the radial line is considered part of the loop and can send and receive signals on the loop. Any number of radial lines can be bypassed in the same manner (see Figure CA561-4).

Note: *Any unused radial ports must be bypassed (the corresponding switch must be in bypass position).*

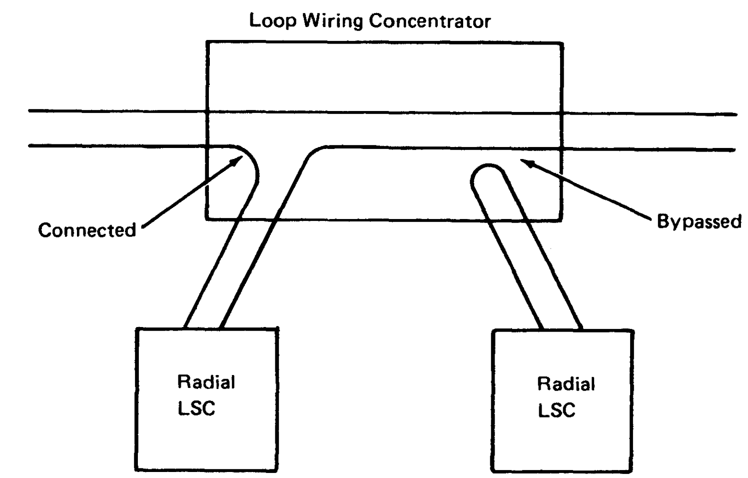


Figure CA561-4. Example of LWC Bypass

CA562 Board Personalization

Board personalization is performed at the time of manufacture for CA features or on-site for updates and additions of CA features.

See CA520 for board locations and CA513 for card locations.

Data Rate – SDLC (CA1) or BSC/S-S (CA2) Adapter Card

BSC/SS Adapter Card (CA2)

Data Rate	Pin Connected to D08 (Ground)
75bps	P04
110bps	P05
134bps	M02
150bps	P02
300bps	G13
600bps	M04
1200bps	M05
2400bps	M03

SDLC Adapter Card (CA1)

Data Rate	Pin Connected to D08 (Ground)
600bps	M04
1200bps	M05
2400bps	M03
	Other rates do not require jumpers.

Synchronous/Asynchronous BSC/S-S Adapter Card (CA2)

Asynchronous Mode – M13 to D08 (Ground) for S/S operations.

Channel Grant/Request Wiring

Caution: Channel grant/request wiring is only valid for SDLC adapter cards.

Channel Grant/Request wiring is dependent on the speed of the communications feature. When the feature is operated at speeds greater than 9600 bps, Channel Grant/Request must be wired for HIGH priority. When the feature is operated at speeds equal to or less than 9600 bps, Channel Grant/Request must be wired for MEDIUM priority. See 8100 system Channel Grant/Request wiring in Chapter 1, ST440, for examples and list of wiring.

CA563 Card Jumpers and Switches

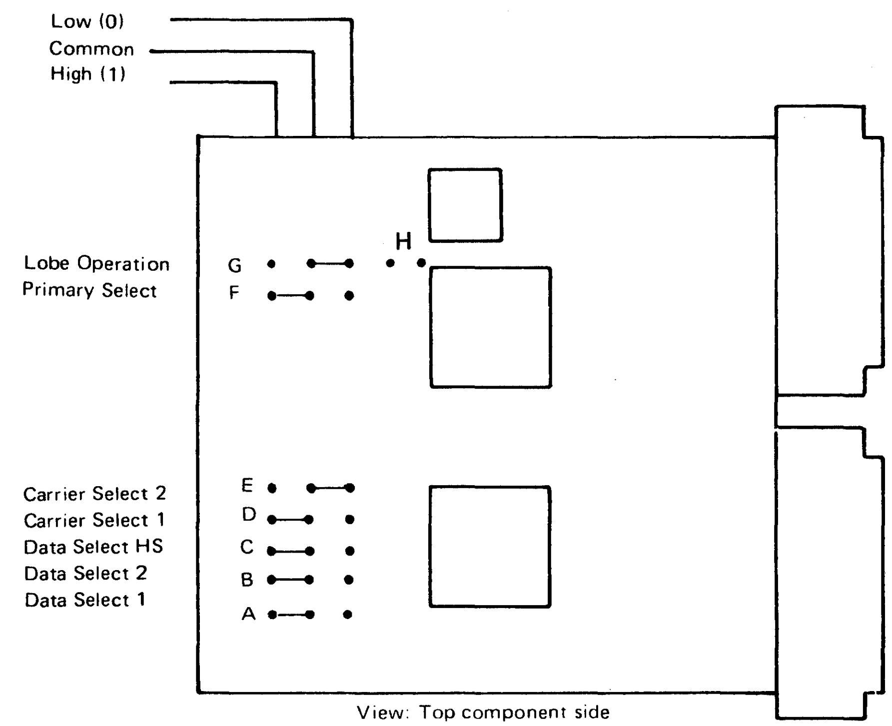
Refer to CA150 for FAC codes and card jumpers. The customer's Configuration Data Sheet will contain communication feature information that relates to FAC codes.

Loop (CA3/CA4) Card Jumpers

Primary Select Jumper is always set to High (1), Primary.

Lobe Operation Jumper is always set to Low (0), Serial Lobe Operation.

Caution: For a two-lobe loop, both loop cards must be jumpered the same.



Jumper PN 1675209

The example shows the card programmed for primary mode, carrier rate = 9.6KBS, data rate = 9.6KBS.

Pin	Comm I/O Tab Pin	Name	Notes
A B C	J10 J11 J12	DS 1 DS 2 HS	Data select lines, see table Half speed
D E	J06 J07	CS 1 CS 2	Carrier select lines see table
F	D12	Prim./Sec.	High primary, low secondary
G	G13	Degate Xmit	Low for lobe 2 control (Lobe operation)
H*	–	Centering	Changes sync. Used for noisy environment

*Jumper may not be present on all level cards.

Carrier Rate kbs	Data Rate kbs	Data Select 1 2 HS A B C	Carrier Select 1 2 D E
9.6	9.6	1 1 1	1 0
38.4	38.4	1 1 1	0 1

0 = Ground = Low

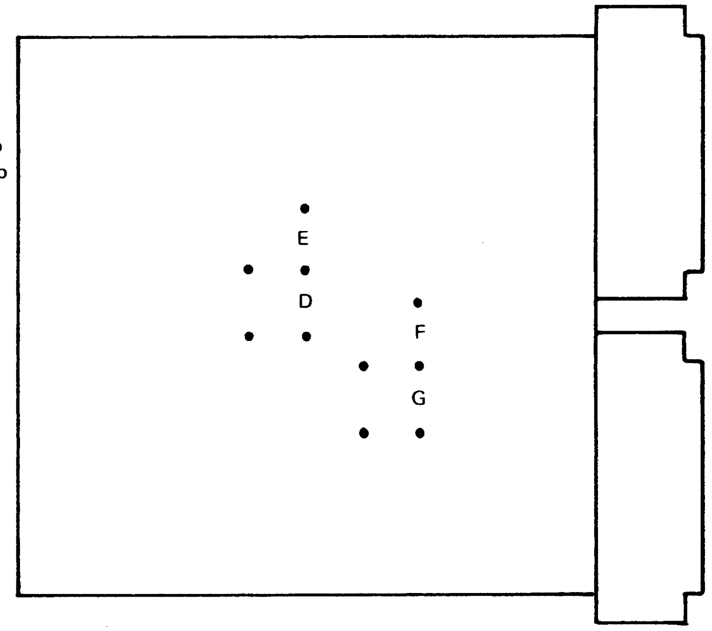
1 = Float = High

Note: *Half Speed (HS), when 0, will switch the data rate to half the indicated value.*

Carrier and Data Select Code Table

EIA (CA5) Card Jumpers

D = Internal wrap
E = External wrap
F = DCE clock
G = 8100 clock

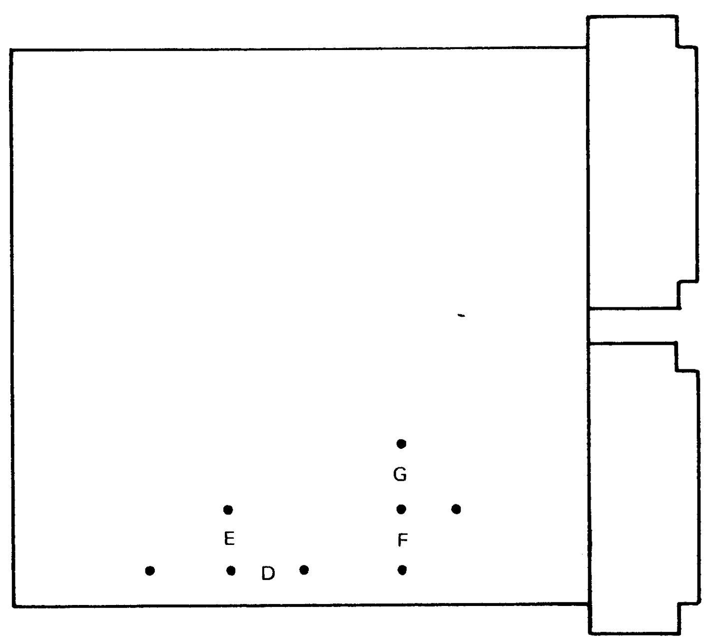


Jumper PN 816645

Note: *Unlabeled card pins are not jumpered.*

V.35 (CA6) Card Jumpers

D = Internal wrap
E = External wrap
F = DCE clock
G = 8100 clock

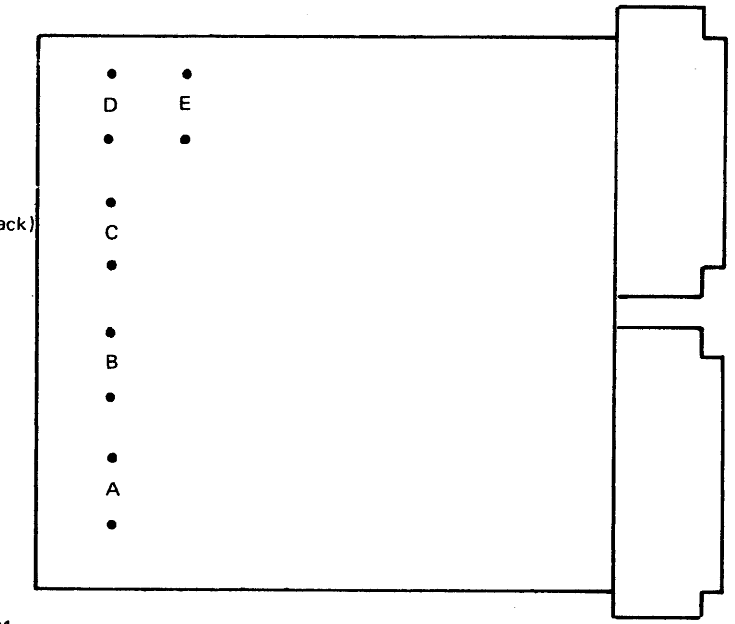


Jumper PN 2731801

Note: *Unlabeled card pins are not jumpered.*

DDS (CA7) Card Jumpers

A = 2.4 K bps
B = 4.8 K bps
C = 9.6 K bps
D = 56.0 K bps
E = DDL (Disable Double Loop Back)



Jumper PN 2731801

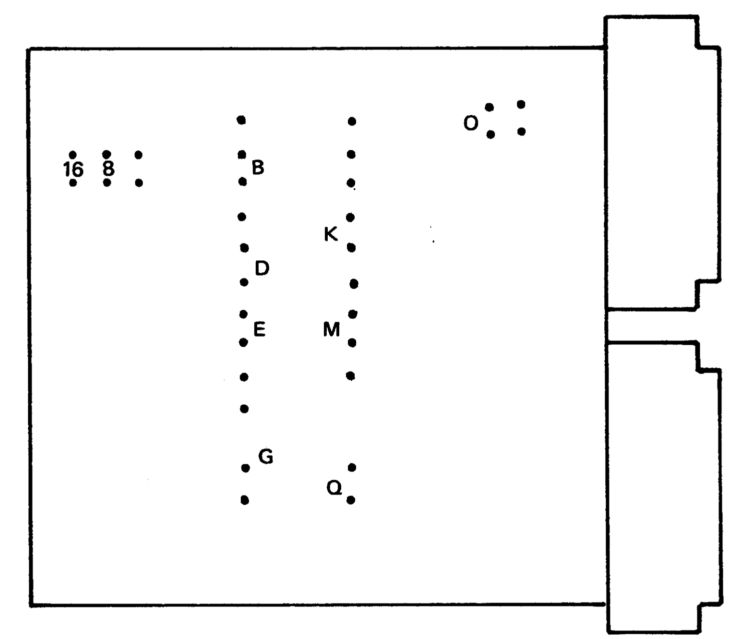
Note: *Unlabeled card pins are not jumpered.*

X.21 (Nonswitched) (CA11) Card Jumpers

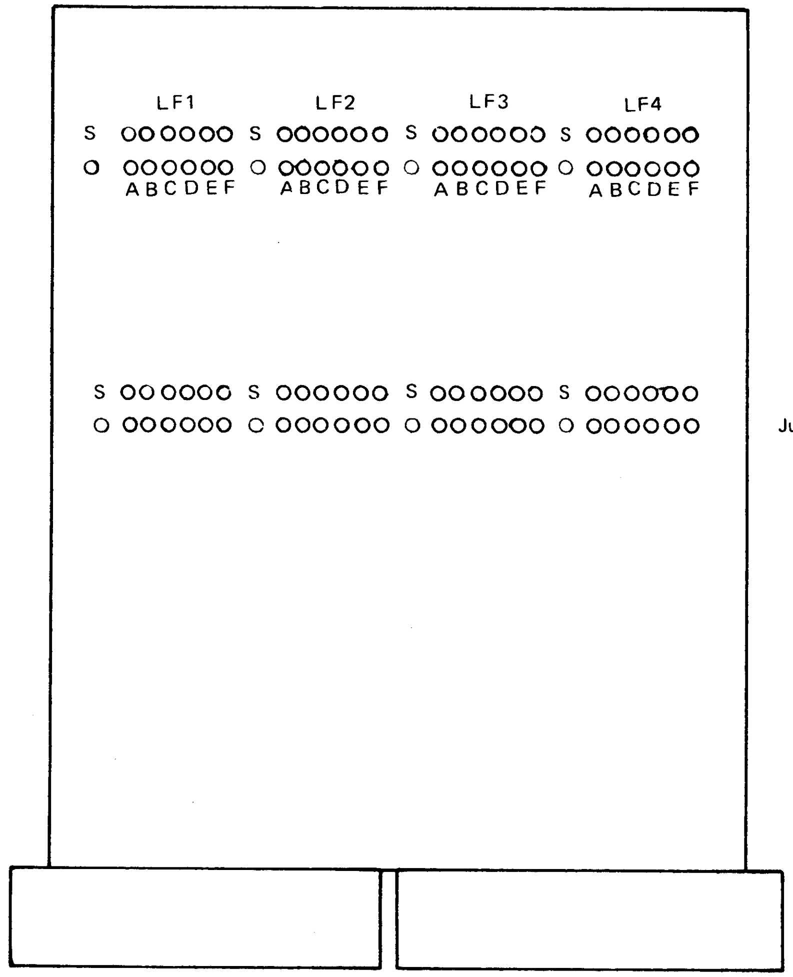
- B = Normal Wrap
- D = Nonswitched
- E = Nonswitched
- G = Nonswitched
- K = Timed DSR
- M = Normal Wrap
- O = Normal Operation
- Q = Error Latch Disable
- 8 = 8 bits CTS delay
- 16 = 16 Bits CTS delay

Jumper PN 2731801

Note: *Unlabeled card pins are not jumpered.*



Multispeed (CA10) Clock Card Jumpers



Jumper PN 2731801

Jumper Instruction

The Multispeed Clock Card may provide a clock source for up to four communications features. Clock frequency is determined by jumper position; this same jumper completes the clock circuit to the communications adapter card.

Line Frequency (LF)	
Jumper Position	LF Value (Khz)
A	2.4
B	4.8
C	9.6
D	19.2
E	38.4
F	56.0

Note: *S jumper position is a storage position for jumpers.*

Physical Address-LF

	LF1	LF2	LF3	LF4
8130	PA=83	PA=84	PA=85	PA=86
8140	–	PA=83	PA=82	PA=81
8101	PA= X3 X7	PA= X2 X6	PA= X1 X5	PA= X0 X4

Board Wiring

	From CA10 Card Pin	To CA1/CA2 Card Pin
LF1	D05	U10 and U11
LF2	D06	
LF3	D09	
LF4	D10	

Integrated Modem (CA8/CA9) Card Jumpers

The Integrated Modem card has card switches instead of jumpers to personalize the card functions and characteristics. Normal switch settings are made at manufacturing time. Transmit level adjustments may be required (refer to CA581 for U.S. and CA711 for W.T.).

U.S. Switched Network Coupler, Card Type A (CA9)

Switch	Condition	Function
J	On	For CBS coupler
	Off	For CDT coupler
M	Off	Normal operation
K	On	Normal operation
A	Off	**Note:** *The transmit level rotary switches are used and mounted on the 01T I/O panel.*
B	Off	
C	Off	
D	Off	
E	Off	
F	Off	
G	Off	
H	Off	
I	Off	
L	–	Not used
N	–	Not used
P	–	Not used
R	–	Not used

World Trade Switched, Network Coupler Public Switched Network Equalizer, Card Type A

Switch	Condition	Function	
		Equalizer Settings:	
N	On*	Normal delay	
J	On*	Disable high-frequency delay	
P	On*	Disable mid-frequency delay	
I	On*	Disable low-frequency delay	
M	Off*	Disable HF amp boost	
K	On	Normal Operation	
A	X	For transmit level	See Figure CA563-1 for card switch settings.
B	X	For transmit level	
C	X	For transmit level	
D	X	For transmit level	
E	X	For transmit level	
F	X	For transmit level	
G	X	For transmit level	
H	X	For transmit level	
I–R	X	For transmit level	
L	–	Not used	

*This is the normal setting.

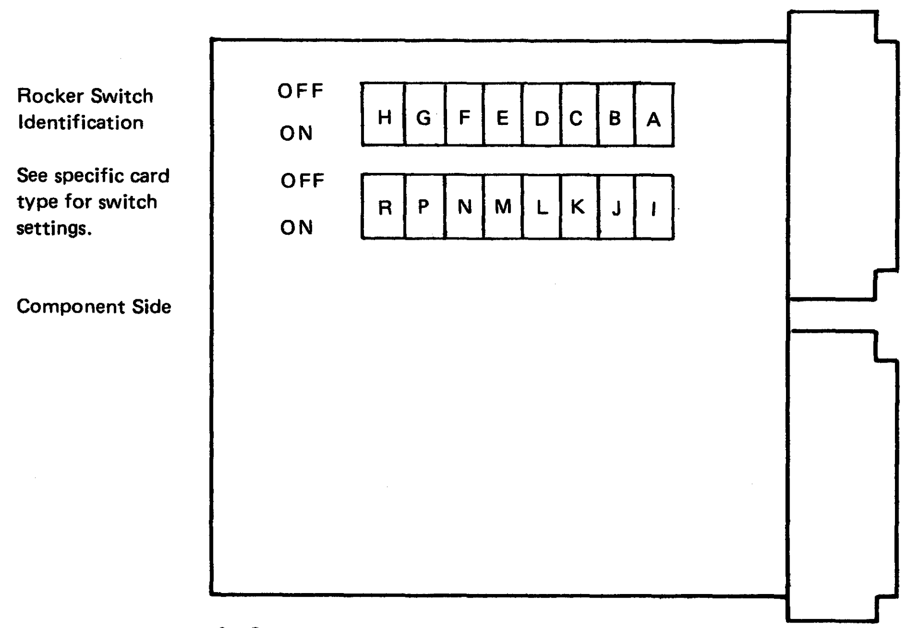
U.S. Nonswitched Line, Manual-Answer, Card Type A (CA8)

Switch	Condition	Function	
		Two-wire/four-wire settings:	
J	Off	Four-wire operation	
K	On		
J	On	Two-wire operation	
K	Off		
		Also board jumpers: G02 to G09, and J05 to J13	
		Clear to Send Settings:	
N	Off	30-ms delay (Note 1)	
P	On	30-ms delay (Note 1)	
N	On	80-ms delay	
P	Off	80-ms delay	
N	Off	230-ms delay (Note 2)	
P	Off	230-ms delay (Note 2)	
		Echo Clamp Delay:	
L	On	50-ms delay	
	Off*	150-ms delay	
A	Off	For transmit level	Not used for nonswitched operations. Rotary switch must be set at zero point.
B	Off	For transmit level	
C	Off	For transmit level	
D	Off	For transmit level	
E	Off	For transmit level	
F	Off	For transmit level	
G	Off	For transmit level	
H	Off	For transmit level	
I	Off	For transmit level	
L	Off	Not used	
M	Off	Not used	
R	Off	Not used	

*This is the normal setting.

Notes:
1. *4-wire operation.*
2. *2-wire operation.*

Integrated Modem Card Type A



A. Switch Layout

Transmit Level (dBm) / Switch

Transmit Level (dBm)	A	B	C	D	E	F	G	H	I/R
0	1								
– 1		1							
– 2			1						
– 3				1					
– 4					1				
– 5						1			
– 6	1						1		
– 7		1					1		
– 8			1				1		
– 9				1			1		
– 10					1		1		
– 11						1	1		
– 12	1							1	
– 13		1						1	
– 14			1					1	
– 15				1				1	
– 16					1			1	
– 17						1		1	
– 18	1								1

Settings:
Blank = Off
1 = On

B. Transmit Level Switch Settings

Figure CA563-1. Integrated Modem Card Type A

World Trade, Nonswitched Line Equalizer, Card Type C (CA8)

Switch	Condition	Function
		Two-wire/four-wire settings:
I	On	Four-wire operation
M	Off	
I	Off	Two-wire operation
M	On	Also board jumper: G02 to G09 and J05 to J13
		Clear to Send Settings:
J	Off	30-ms delay (Note 1)
K	On	30-ms delay (Note 1)
J	On	80-ms delay
K	Off	80-ms delay
J	Off	230-ms delay (Note 2)
K	Off	230-ms delay (Note 2)
		Echo Clamp Delay:
L	On	50-ms delay
	Off*	150-ms delay
		Equalizer Settings:
CC	On*	Normal delay
AA	On*	Disable high-frequency delay
DD	On*	Disable mid-frequency delay
BB	On*	Disable low-frequency delay
N	On*	Disable HF amp boost
A	X	For transmit level — See Figure CA563-2 for card switch settings.
B	X	For transmit level
C	X	For transmit level
D	X	For transmit level
E	X	For transmit level
F	X	For transmit level
G	X	For transmit level
H	X	For transmit level
R	X	For transmit level
Others	Off	Not used

*This is the normal setting.

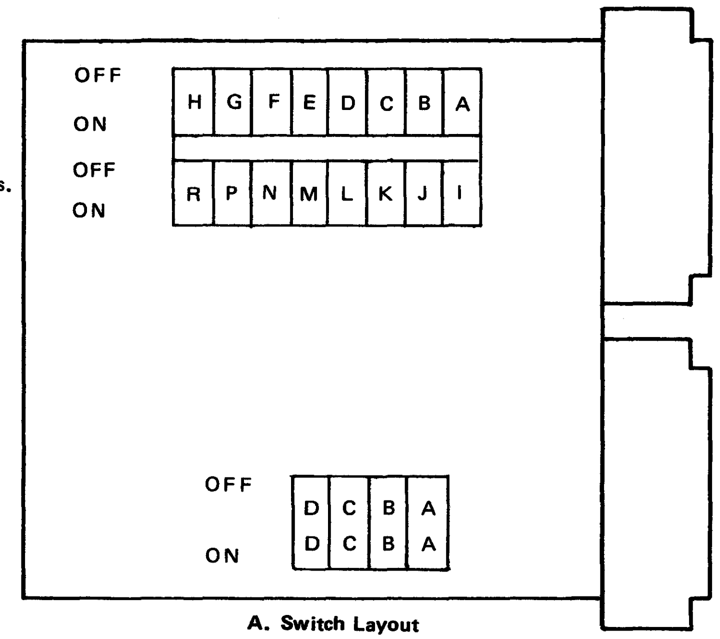
Notes:
1. *4-wire operation.*
2. *2-wire operation.*

Integrated Modem — Card Type C

Rocker Switch Identification

See specific card type for switch settings.

Component Side



A. Switch Layout

Transmit Level (dBm)	A	B	C	D	E	F	G	H	I/R
0	1								
– 1		1							
– 2			1						
– 3				1					
– 4					1				
– 5						1			
– 6	1						1		
– 7		1					1		
– 8			1				1		
– 9				1			1		
– 10					1		1		
– 11						1	1		
– 12	1							1	
– 13		1						1	
– 14			1					1	
– 15				1				1	
– 16					1			1	
– 17						1		1	
– 18	1								1

Switch

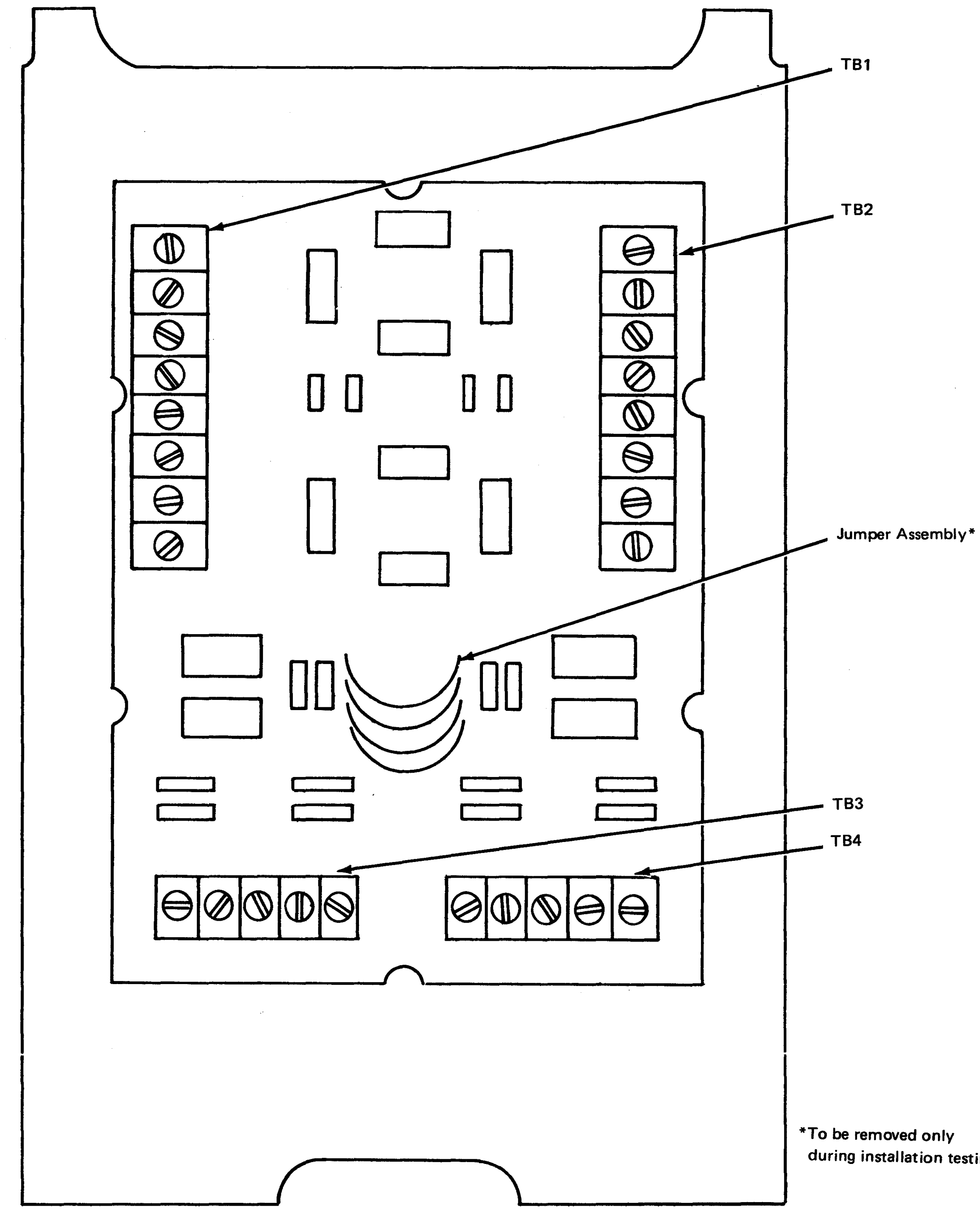
Settings:
Blank = Off
1 = On

B. Transmit Switch Settings

Figure CA563-2. Integrated Modem Card Type C

CA564 Loop Surge Suppressor (LSS) Circuit Board Jumpers

The LSS has a jumper assembly located just above the lower terminal block. The jumper assembly is used for testing purposes (see Figure CA564-1).



*To be removed only during installation testing.

Figure CA564-1. Loop Surge Suppressor (LSS) Circuit Board Assembly

CA565 Modem Strapping

Modem data strapping is performed either during installation or reconfiguration to configure IBM or OEM modems for 8100 system operation. The options strapped are determined by:

1. The 8100 data terminal equipment (DTE) operation.
2. The TP network configuration.

The following configuration information should be specified using the proper modem documentation:

8100 Operations:

- Local test, controlled by 8100 DTE (IBM modem only)
- Request to send, controlled by 8100 DTE
- Data rate select, controlled by 8100 DTE
- Select standby, controlled by 8100 DTE
- Data terminal ready, controlled by 8100 DTE

TP network configuration:

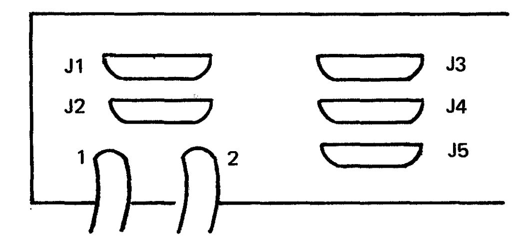
- Point-to-point
- Multipoint (tributary only)
- Switched network
- Switched network backup (SNBU)
- Alternate voice
- Fan out
- 2-wire
- 4-wire
- Alternate levels
- Direct line attachment (World Trade)
- Auto answer (AA)
- Timing
- Distance

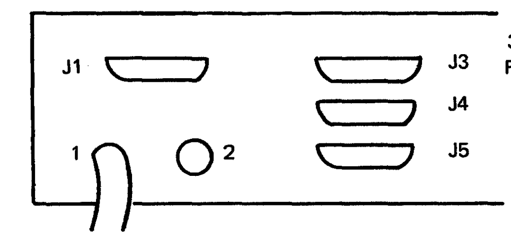
Caution: Connection to Australia's DATEL Nonswitched Service Plan 34F, Modem 46/4800, must not have the new sync option strap installed.

CA570 IBM External Modem Feature Identification

Although some cable connections may not be installed, rear views of the 3872, 3874, and 3875 modems are basically the same.

3872, 3874
Rear View





3875
Rear View

3872 Modem Features

Cable Connectors							Feature Description	Mode
1	2	J1	J2	J3	J4	J5		
	X						Nonswitched Line without SNBU	1
X	X						Nonswitched Line, SNBU without Auto Answer	2
	X						Switched Line without Auto Answer	3
	X		X				Nonswitched Line, SNBU with Auto Answer	4
			X				Switched Line with Auto Answer	5
		X					Basic System Input 8100	

3874 Modem Features

Cable Connectors							Feature Description	Mode
1	2	J1	J2	J3	J4	J5		
X							Nonswitched Line without SNBU	1
X	X						Nonswitched Line, SNBU without Auto Answer	2
	X						Switched Line without Auto Answer	3
X			X				Nonswitched Line, SNBU with Auto Answer	4
			X				Switched Line with Auto Answer	5
						X	Basic System Input 8100	

3875 Modem Features

Cable Connectors							Feature Description	Mode
1	2	J1	J2	J3	J4	J5		
X							Nonswitched Line without SNBU	1
X	X						Nonswitched Line, SNBU without Auto Answer	2
NOT ALLOWED							Switched Line without Auto Answer	3
X						X	Nonswitched Line, SNBU with Auto Answer	4
NOT ALLOWED							Switched Line with Auto Answer	5
		X					Basic System Input 8100	

CA580 Adjustments

CA581 Transmit Level Adjustment — U.S.

Note: *For WTC, refer to CA711.*

The transmit level for switched network operations when using an integrated modem should be adjusted to comply with local common carrier regulations. Contact your TP co-ordinator for current regulations.

The integrated modem uses a rotary switch mounted on the 8100 units I/O panel for transmit level adjustment. This switch provides 18-dBm attenuation (maximum) in 1-dB steps. The integrated modem is factory set for -0.5-dBm output with the rotary switch in off (0) position.

CA590 Line Monitor Procedure

When line operations appear to be questionable or incorrect, line monitoring is required to verify its status or conditions. Line monitoring may be accomplished for any line discipline, that is, SDLC, BSC, or start-stop (TTY or 2741). A line monitoring device may be attached to the data lines (DT — DR) of the selected 8100 CA feature. See CA540 for troubleshooting diagrams of selected CA features. Line monitoring devices may include a datascope, oscilloscope, PT-2, BTDAT, TDAT, CE Probe, meter, or modem interface test set. An appropriate link-level test (see CA212 or CA213) should be run up/down to the host/controller/terminal, and line monitoring should be performed.

Link-level tests to be used offline are:

SDLC Primary	— Routine 53
SDLC Secondary	— Routine 71
BSC	— Routine 77 or 78 (these routines are remote site dependent)
Start-Stop 2741	— Routine 79
Start-Stop TTY	— Routine 85

See CA202 for invocation procedures.

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CA600 Cryptographic Devices, Interface and Line Descriptions, and Test Equipment Setup

CA620 Cryptographic Devices

CA621 IBM 3845/3846

The IBM 3845/3846 is a standalone cryptographic unit which is inserted in the communications link between the 8100 EIA interface and the external modem (IBM or OEM). In operational mode, the 3845/3846 encodes and decodes the data stream of the communications link. Certain EIA control lines are utilized and delayed by the 3845/3846.

In bypass mode (manual switch action), all EIA lines (control and data) bypass the encode/decode section of the 3845/3846.

There is neither error detection, correction, nor recovery in the 3845/3846, and it does not contain wrappable circuitry. There is no programmable bypass mechanism.

The 3845/3846 is customer-planned, installed, setup, and maintained. There are depot repair facilities for unit maintenance which the customer may use.

The overall 8100 maintenance strategy for 3845/3846 is to bypass 3845/3846 for 8100 maintenance. 8100 bypass mechanisms do not permit 8100 tests to test the 3845/3846 (current models) nor test through it.

Customer's problem determination procedures enable the customer to bypass the 3845/3846 under the appropriate error conditions and in a timely manner.

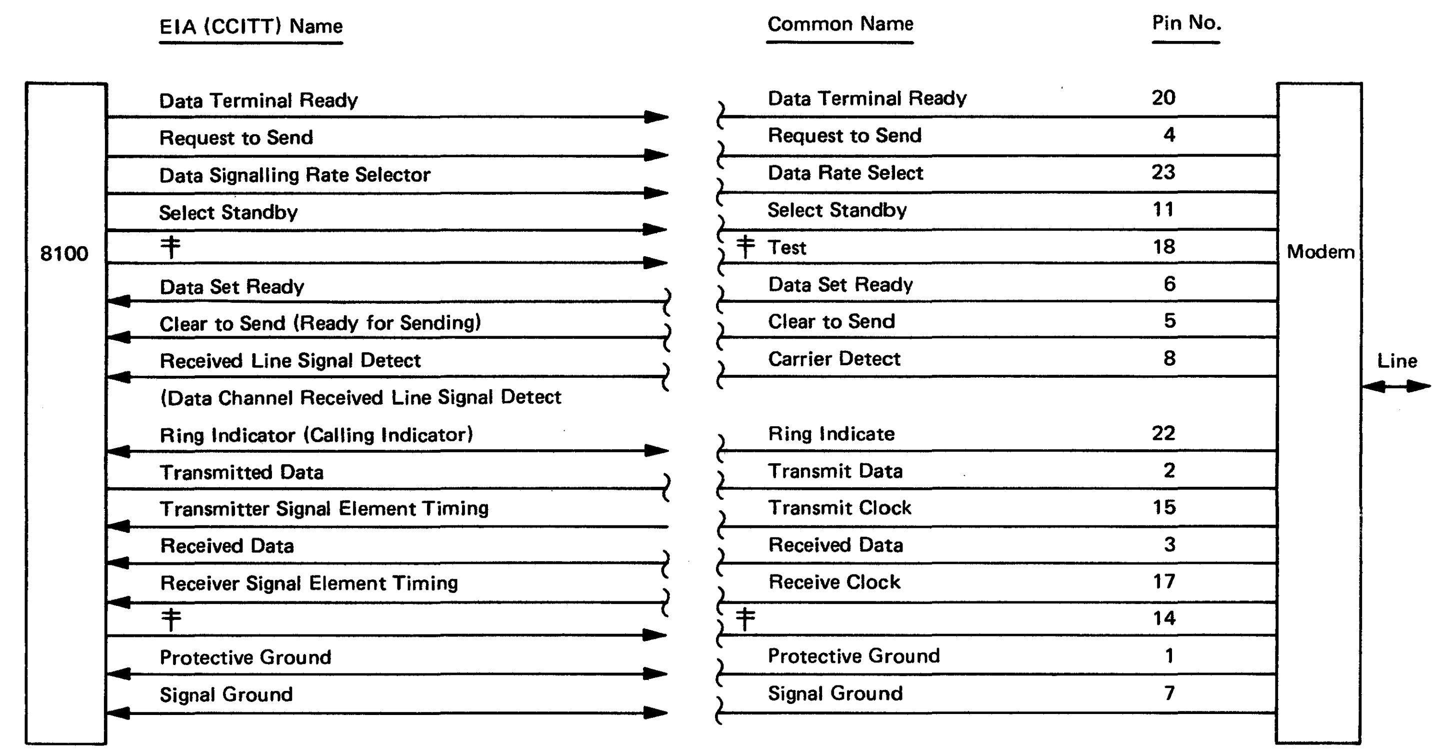
CA622 OEM

OEM cryptographic devices are treated identically to IBM devices. The cryptographic device is bypassed when testing 8100 communications features.

CA630 Interface Descriptions

CA631 EIA/CCITT Interface

The interface between the 8100 system and the external modem is defined as the EIA/CCITT interface. This interface conforms to CCITT recommendation V24 and EIA Standards RS232C and RS234. The sense, voltage levels, and impedances of the interface lines are defined in the relevant CCITT and EIA publications.



EIA/CCITT Interface Signal Summary

Legend:

8100 controls these lines

Modem controls these lines

Common lines

‡ Not an EIA/CCITT standard

When EIA and CCITT nomenclatures differ, the CCITT names are shown in parentheses. The common line name is also given.

Line Name 1 = Common Name 2 = EIA Name 3 = CCITT Name	Pin No. On Connector	Line Origin	Line Description/Specification
1. Data Terminal Ready 2. Data Terminal Ready (CD) 3. Data Terminal Ready (108.2) 3. *Connect Data Set to Line (108.1) (WT only)	20	8100 Up level: On Down level: Off	The 8100 turns on this signal when the CA is activated, indicating the CA adapter is ready. This signal also controls switching of the modem to the communications line subject to other interface lines. *When this circuit is ON, it connects the modem to the communications line regardless of other interface lines.
1. Request to Send 2. Request to Send (CA) 3. Request to Send (105)	4	8100 Up level: On Down level: Off	This circuit conditions the modem for data transmission and, on a half-duplex line, controls the direction of data transfer of the modem.
1. Data Rate Select 2. Data Signaling Rate Selector (CH) 3. Data Signaling Rate Selector (111)	23	8100 Up level: Prime speed Down level: Half speed	When the modem is controlled by the 8100, the 8100 uses this signal to select data rate.
1. Select Standby 2. Select Standby 3. Select Standby (116)	11	8100 Up level: Switched network. Down level: Nonswitched.	When the modem is controlled by the 8100 and has a Switched Network Backup feature, the 8100 uses this signal to select nonswitched line or switched Network Backup operation.
1. Test (Not EIA/CCITT standard. May not be available on all modems.)	18	8100 Up level: On Down level: Off	This circuit activates a test feature on IBM 3872, 3874, 3875 modems. Modem wraps the transmitter back to the receiver on the analog side of the modem.
1. Data Set Ready 2. Data Set Ready (CC) 3. Data Set Ready (107)	6	Modem Up level: On Down level: Off	Switched Network: On condition indicates that the modem is connected to the communications line and is ready to exchange further control signals with the 8100. Nonswitched Network: On condition indicates modem power is on.
1. Clear to Send 2. Clear to Send (CB) 3. Ready for Sending (106)	5	Modem Up level: On Down level: Off	The modem uses this circuit to inform the 8100 that the modem is ready to transmit data. This signal turn on after Request to Send turns on.

Line Name	Pin No.	Line Origin	Line Description/Specification
1. Carrier Detect 2. Received Line Signal Detect (CF) 3. Data Channel Received Line Signal Detect (109)	8	Modem Up level: On Down level: Off	On condition indicates that the modem is receiving a signal suitable for demodulation, and that signals on the receive data line are valid.
1. Ring Indicate 2. Ring Indicator (CE) 3. Calling Indicator (125)	22	Modem Up level: On Down level: Off	This circuit indicates that a calling signal is being received by the modem from the communications line. (Switched Network and CCITT 108.1 option).
1. Transmit Data 2. Transmitted Data (BA) 3. Transmitted Data (103)	2	8100 Up level: 0-bit Down level: 1-bit	This circuit sends data to the modem for transmission over the communications line.
1. Transmit Clock 2. Transmitter Signal Element Timing (DB) 3. Transmitter Signal Element Timing (114)	15	Modem Square Wave	This circuit is used as a clock for the transmitted data. The signal is a square wave that takes the frequency of the modem speed. The signal is normally present when modem has power on.
1. Received Data 2. Received Data (BB) 3. Received Data (104)	3	Modem Up level: 0-bit Down level: 1-bit	Data signals are received by the 8100 on this circuit.
1. Receive Clock 2. Receiver Signal Element Timing (DD) 3. Receiver Signal Element Timing (115)	17	Modem Square Wave	This circuit is used as a clock for the received data. The signal is a square wave that takes the frequency of the modem speed.
1. New Sync (Not EIA/CITT standard)	14	Up level: Active Down level: Inactive	This line is not used for normal operations, or in test.
1. Protective Ground 2. Protective Ground (AA) 3. Protective Ground (101)	1	Common	"Protective ground" is connected to the frame ground of the modem.
1. Signal Ground 2. Signal Ground (AB) 3. Signal Ground (102)	7	Common	"Signal ground", which provides the return in the modem for the interface signals, can be connected to frame ground by a strapping option. Do not use this connection in the modem for CA.

CA635 Modem/Communications Line Interface (US/Canada, Switched Network)

The Data Coupler, type CDT, is connected to the modem through an additional socket on the back panel. The Data Access Arrangement, (DAA), type CBS, is wired directly to the modem. The data coupler and the DAA connections are independent of each other. The appropriate strapping is carried out during installation.

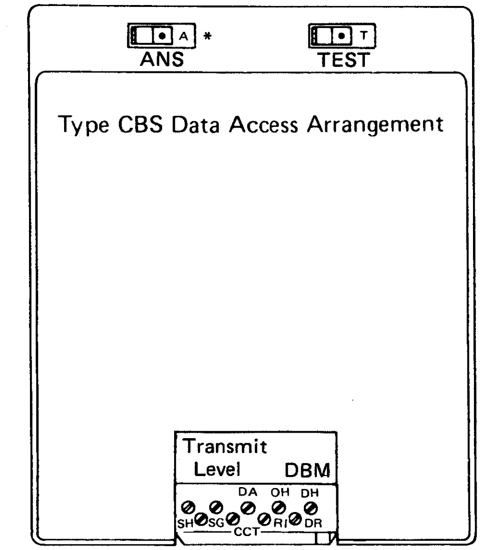
CBS Data Access Arrangement (DAA)

In addition to the two lines that connect the modem transmission path to the DAA, the interface also comprises a number of control lines that carry digital signals (Figure CA635-1). The level and function of the digital signals are in accordance with CCITT Recommendation V24 and EIA Standard RS-232-C. The interface lines are shown in the following table:

Interface Lines	Direction	Function
Data Tip (DT) Data Ring (DR)	Both	Transmission and reception path for modem.
Off Hook (OH)	From modem	Up level causes off-hook relay in DAA to operate.
Data Modem Ready (DA)	From modem	Up permanently when modem is selected for switched network operation.
Ring Indicator (RI)	From DAA	Up level informs modem that a ringing signal is being detected by the DAA.
Signal Ground (SG)	Both	Return path for control signals.
Coupler Cut-Through (CCT)	From DAA	Up level indicates to modem that DAA is ready. Down level indicates that the coupler is inoperative.
Switch Hook (SH)	From DAA	Up level indicates to the modem that the DAA associated handset is off and that the exclusion key has been pulled out.

With the modem and the DAA prepared for auto-answering (see Auto-Answering in the appropriate modem manual), signals are exchanged as follows:

1. The DAA directs the ringing signal and sends RI to the modem.
2. If the 8100 is ready (Data Terminal Ready), the modem signals Off-hook (OH) to the DAA.
3. As soon as the DAA is ready (CCT on), there is an answering tone of 2100 Hz within 3 to 4 seconds.
4. At the end of the transmission of this tone, the auto-answering circuit in the modem transfers the control to the 8100 by raising Data Set Rdy.



*May not be present on all models.

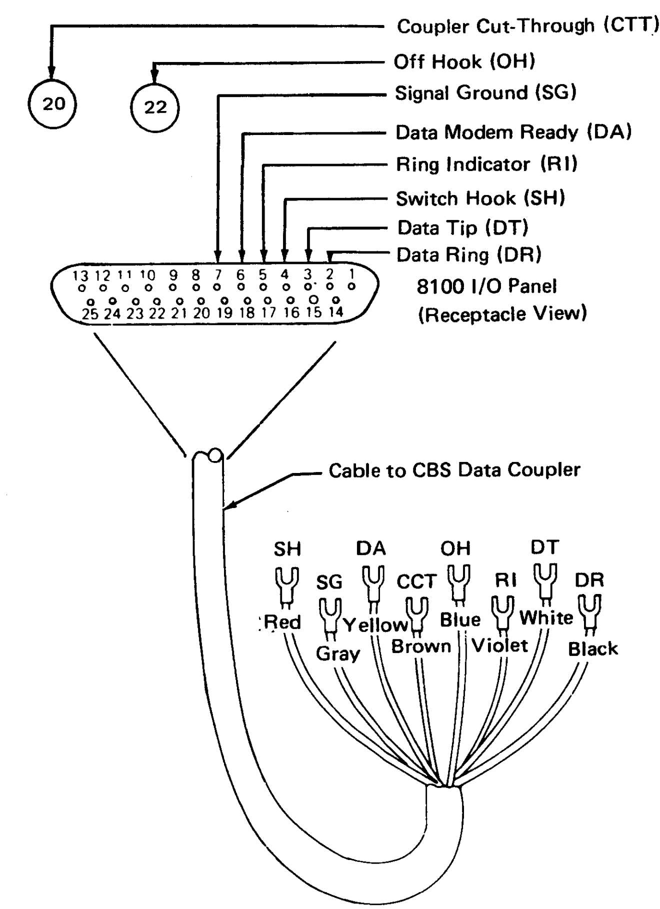


Figure CA635-1. CBS DAA Cable

CDT Data Coupler

The two lines (Data Tip and Data Ring) that connect the modem to the data coupler are used only as a transmission and reception path. They function the same as those for the 8100 or modem lines, and the function of answering and making calls is entirely manual. Figure CA635-2 illustrates the CDT data coupler cable.

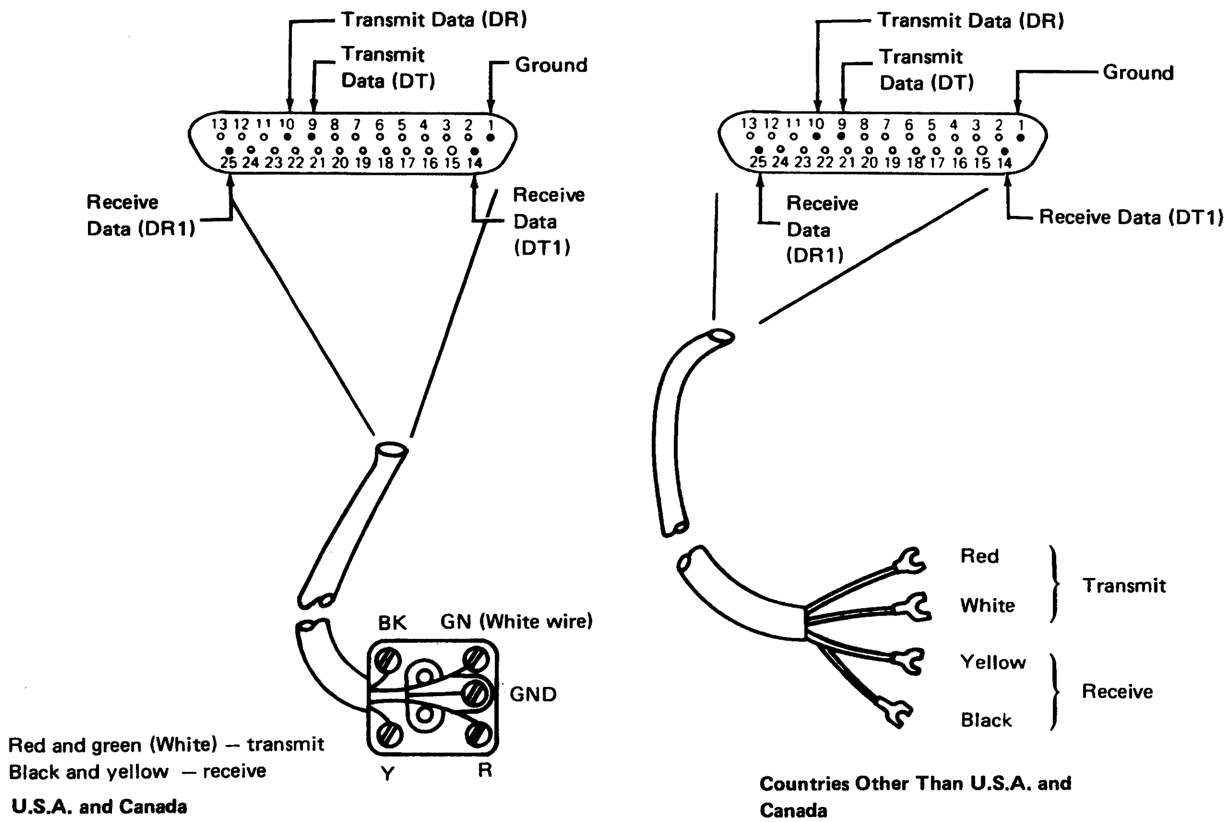


Figure CA635-2. CDT Data Coupler Cable

CA638 How to Establish a Switched Line Connection (DPCX)

CBS DAA or Equivalent Connected to the 8100 Modem

Auto-Answer at 8100

1. Set modem to operate.
2. Set Talk/Data switch (if provided) to Data.
3. Cradle DAA handset (if provided).
4. Activate SYSHOST, enable communications.

At message A081, the 8100 prepares to answer the call automatically. The 8100 automatically disconnects the call when SYSHOST terminates.

The CBS DAA-eight-wire cable between the modem and DAA is used in the U.S. and Canada for auto-answer capability. The handset is optional, and the auto tone is normally provided by the modem.

Manual Answer at 8100

1. Set modem to operate.
2. Set Talk/Data switch (if provided) to Data.
3. Cradle DAA handset (if provided).
4. When telephone rings, lift handset and pull the Exclusion Key up.
5. Activate SYSHOST, enable communications.
6. Wait for message A081.
7. At the request of the calling operator, set the Talk/Data switch (if provided) to Data.
8. Cradle the handset (pushes down the Exclusion Key).
9. After all sessions are complete, the 8100 automatically disconnects the call when SYSHOST terminates.

CDT Coupler or Equivalent Connected to the 8100 Modem

A four-wire cable connects the modem and the CDT coupler. It is used in the U.S. and Canada for Manual Answer only. A handset is required, and the answer tone is not normally provided by the modem or the 8100. The manual answer procedure is as follows:

1. Set modem Talk/Data switch to Talk.
2. Cradle coupler handset.
3. When telephone rings, lift handset. Arrange for communications with the host operator.
4. Activate SYSHOST; enable communications.
5. At message A081, raise Data Key on coupler. Do not cradle the handset.
6. Set modem Talk/Data switch to Data (causes Data Set Ready).
7. After all sessions are complete and SYSHOST has terminated, disconnect the call by cradling the handset.
8. Set modem Talk/Data switch to Talk.

Other Coupler

The Data Access Arrangements for World Trade are not standardized. Connection procedures are similar to those of the CBS or CDT coupler.

CA640 Line Discipline Descriptions

CA641 SDLC Line Operations

The 8100 uses the Synchronous Data Link Control (SDLC) procedures for link control.

Primary and Secondary Stations

A data link or loop uses at least two stations: a primary station and one or more secondary stations. The primary station is responsible for data link control. All transmissions on the link/loop go to and from the primary station. Transmissions do not occur between secondary stations. The primary stations control the link/loop by issuing commands to the secondary stations; the secondary stations respond in a predefined manner.

Frames

The frame is the vehicle for every command, every response, and all information that is transmitted between the primary and secondary stations.

Flag	Address	Control	Data Data	CRC	CRC	Flag

Frame Characters

Flag (0111 1110). A flag byte 7E (hex) encloses each frame transmitted. The starting flag serves as the reference for the address and control bytes. The ending flag serves as the position reference for the CRC bytes. Transmission of characters between the flag characters is adjusted by a unique zero bit insertion/deletion technique to prevent 7E characters from occurring between flags.

Address. Every secondary station has a unique 1-byte address. This secondary address is used in all frames from and to the primary station. A primary address is never used.

Control. The control byte contains the commands, responses, and sequence information required to operate the link. The control byte has three formats.

Control Byte

Bits	0 1 2	3	4 5 6	7
Information Transfer Format	Transmitted Frame Count	Poll/ Final	Receive Frame Count	Format Code
Supervisory Format	Receive Frame Count	Poll/ Final	Command/ Response	Format Code
Unnumbered Format	Command/ Response	Poll/ Final	Command/ Response	Format Code

Command/Response. Command/response is used by the primary and secondary to operate the Link. Commands are transmitted by the primary; responses are sent by the secondary.

Format Code. A receiver determines the format of the frame being received by examining bits 6 and 7 of the control byte. Information transfer format uses only bit 7 for its format code.

Bits	6	7
Information Transfer		0
Supervisory	0	1
Unnumbered	1	1

Poll/Final. The primary station signals the secondary station that a response or confirmation of frames is required by turning on bit 3 (Poll) in the last frame transmitted. The secondary system indicates that it has finished transmitting by turning on bit 3 (Final) in the last frame sent to the primary. The poll/final bit has the same meaning regardless of the format used.

Receive Frame Count. The information and supervisory formats use a receive frame count field inserted by the receiving station to confirm the information frames received.

Transmitted Frame Count. Each information format frame transmitted by the primary or secondary contains a transmitted frame count that is used to sequence information frames.

CRC. Every frame contains a 2-byte check field. The transmitting station generates and inserts the check field into the frame. The receiving station generates the field on the frame received, and compares the result with the received field. The receiver ignores all frames having an incorrect check field.

Frame Formats

Each frame is transmitted in one of three formats: information transfer, supervisory, and unnumbered. The format code in the control byte identifies the format.

Information Transfer Format. The information transfer format transfers data between the secondary and the primary. The station transmitting information transfer format frames counts and numbers each frame. This count (0–7) accompanies the transmitted frame (transmitted frame count). The receiver counts each frame received correctly, and compares its count with the transmitted frame count received. Up to seven frames may be sent before the transmitting station requests the receiver to confirm the count. Received frames that are out of sequence, or otherwise bad, cause the receive count to stop incrementing. The receive count field returned to the transmitting station indicates the last record received correctly. The transmitting station retransmits from that record on. Received counts may be reported by using an information transfer format or a secondary format frame. The receive and transmit counters are incremented only for information transfer frames.

Supervisory Format. The supervisory format is used by the primary and secondary to acknowledge information transfer frames, to request transmission, and to inhibit sending information transfer frames. No data field is used in this format. The received frame count indicates the last frame correctly received. The secondary uses two command/response combinations in this format:

Command/Response Control Bits	4	5
Receive Ready	0	0
Receive Not Ready	0	1

Receive Ready. Confirms frames received, and indicates that the station is ready to receive. Received frame count indicates the last frame received correctly.

Receive Not Ready. Indicates a temporarily busy condition. No Information Transfer Frames can be accepted. The received frame count field indicates the last information transfer frame accepted before the busy condition occurred.

Unnumbered Format. This format is used to set secondary mode of operation, to exchange ID information with the primary, and to support the 370X link test. The secondary uses the following commands/responses in this form.

Control Bits	0 1 2	4 5	Data Field
Set Normal Response Mode	1 0 0	0 0	None
Request On Line	0 0 0	1 1	None
Disconnect	0 1 0	0 0	None
Unnumbered Ack	0 1 1	0 0	None
Command Reject	1 0 0	0 1	3 Sense Bytes
Exchange ID	1 0 1	1 1	6 ID Bytes
Test	1 1 1	0 0	Variable

Command/Response Control Bits

Set Normal Response Mode (Command). Sent by the 370X or primary to place the secondary in Normal Response mode (online to 370X). This command is required before operation with the primary can proceed.

Request On Line (Response). Sent by the secondary when in Disconnect mode as a response to any poll frame other than a Set Normal Response Mode Command.

Disconnect (Command). Sent by the 370X or primary to place the secondary effectively in Disconnect Mode.

Unnumbered Acknowledgment (Response). Sent by the secondary when a Set Normal Response or Disconnect command has been accepted.

Command Reject (Response). Sent by the secondary when it receives an invalid command or incorrect format frame. The secondary remains in a Command Reject condition until a Set Normal Response or Disconnect Mode command is received. All non-mode setting commands receive a command reject response.

Exchange ID (Command/Response). Sent by the secondary response to an Exchange ID command. The data field contains the secondary station ID.

Test (Command/Response). Used to support the link test operation. The data field sent from the primary in the test command frame is echoed by the secondary in a test response frame.

Station Modes. The primary station controls the mode of the secondary station by sending a command to set one of two modes in the secondary station.

Normal Response Mode. This mode is entered after the secondary accepts a Set Normal Response Mode command. This mode is required before informational transfers can occur, and before the full range of SDLC commands can be used for data link operation. The mode is normally maintained until operation with the primary is no longer required.

Normal Disconnected Mode. The secondary assumes this mode when the secondary is first activated. In this mode, only a Test, Set Normal Response Mode, or Exchange ID command is accepted by the secondary. Any other frame with polling specified causes the secondary to send a Request On Line response. Frames with no polling specified are ignored. This mode is also assumed by the secondary after accepting a Disconnect Command.

NRZI Mode. Modems or communications adapters that derive a Receive Clock from data transitions are sensitive to long periods of transitionless data. The zero bit insertion technique of SDLC, which prevents the appearance of flag characters within a frame, also ensures that a series of 1-bits greater than five will never occur. In order to prevent the occurrence of extended periods of transitionless data due to continuous 0 bits, a NRZI mode of operation may be optionally selected for bit transmission. The NRZI mode option causes a transmitter to flip the state of the transmit line each time a 0 bit is to be transmitted. To transmit a 1-bit, the transmit line remains at its previous bit state.

Logical Data	1 1 0 0 0 0 1 1 0 1 1 0 0
Transmitted Data (NRZI Mode)	+ + + + - + - + + + - - - + -

If NRZI mode is selected, all stations connected to the same link must use NRZI mode, NRZI mode may be either responded or prohibited for modems with specific pattern sensitivities. NRZI mode may be specified in the 8100.

SDLC Line Operation Examples

The following examples describe the typical operation of the 8100 using the SDLC line discipline. The 8100 communicates in half-duplex mode at all times even though it may be connected to a link that has simultaneous transmit and receive capability (full duplex). The following symbolic format is used:

Adr	Format	T-Cnt	P/F	R-Cnt	Data
	Info				

Adr	Format	Cmd/Resp	P/F	R-Cnt
	Supr			

Adr	Format	Cmd/Resp	P/F	Optional Data
	Unnmbr			

Legend:

Cmd/Resp	=	Command or response:
DISC	=	Set Disconnect Mode
RNR	=	Not Ready to Receive
ROL	=	Request On Line
RR	=	Ready to Receive
SNRM	=	Set Normal Response Mode
UA	=	Unnumbered Acknowledgment
XID	=	Exchange ID
Info	=	Information Transfer Format
P/F	=	Poll bit if message is from primary Final bit if message is from secondary
R Cnt	=	Received frame count
Supr	=	Supervisory Format
T Cnt	=	Transmitted Frame Count
Unnmbr	=	Unnumbered Format

Example: 8100 (Secondary) to Host (Primary)

HOST — 8100

Switched Line connection made: 8100 is in Disconnect Mode. Host request 8100 I.D.

Adr	Format	Cmd/Resp	P/F
8100	Unnmbr	XID	On

Adr	Format	Cmd/Resp	P/F	Data
8100	Unnmbr	XID	On	6 Bytes

8100 responds with ID information. This sequence is generally unnecessary in a Nonswitched Network.

Host sends a Contact Poll to 8100.

Adr	Format	Cmd/Resp	P/F	R-Cnt
8100	Supr	RR	On	0

8100 in Disconnect Mode sends a Request for Online Status.

Adr	Format	Cmd/Resp	P/F
8100	Unnmbr	ROL	On

Host sends SNRM Command to set 8100 online. Transmit and Receive Counts in 8100 are set to zero.

Adr	Format	Cmd/Resp	P/F
8100	Unnmbr	SNRM	On

8100 accepts SNRM Command, sets itself Online to the Host, and confirms acceptance with an Nonsequenced Acknowledgment response.

Adr	Format	Cmd/Resp	P/F
8100	Unnmbr	UA	On

Host Polls 8100 for transmission.

Adr	Format	Cmd/Resp	P/F	R-Cnt
8100	Supr	RR	On	0

8100 sends three sequenced information messages.

Adr	Format	T-Cnt	P/F	R-Cnt	Data
8100	Info	0	Off	0	Data

Adr	Format	T-Cnt	P/F	R-Cnt	Data
8100	Info	1	Off	0	Data

Adr	Format	T-Cnt	P/F	R-Cnt	Data
8100	Info	2	On	0	Data

Host confirms receiving records (T-Cnt 0, 1, and 2) and Polls the 8100 for further transmissions.

Adr	Format	Cmd/Resp	P/F	R-Cnt
8100	Supr	RR	On	3

8100 sends one additional message.

Adr	Format	T-Cnt	P/F	R-Cnt	Data
8100	Info	3	On	0	Data

Host confirms receiving message T-Cnt 3 and sends two messages to 8100.

Adr	Format	T-Cnt	P/F	R-Cnt	Data
8100	Info	0	Off	4	Data

Adr	Format	T-Cnt	P/F	R-Cnt	Data
8100	Info	1	Off	4	Data

Adr	Format	Cmd/Resp	P/F	R-Cnt
8100	Supr	RNR	On	1

8100 becomes busy after receiving record 0. Only record T-Cnt 0 is confirmed.

Host Polls to see whether the 8100 is still busy.

Adr	Format	Cmd/Resp	P/F	R-Cnt
8100	Supr	RR	On	4

8100 is no longer busy, and expects record T-Cnt to be transmitted.

Adr	Format	Cmd/Resp	P/F	R-Cnt
8100	Supr	RR	On	0

Host retransmits record T-Cnt 1.

Adr	Format	T-Cnt	P/F	R-Cnt	Data
8100	Info	1	On	4	Data

HOST | 8100

8100 confirms record T-Cnt 1, and has nothing further to transmit.

←

Adr	Format	Cmd/Resp	P/F	R-Cnt
8100	Supr	RR	On	2

Host sends three messages to 8100.

Adr	Format	T-Cnt	P/F	R-Cnt	
8100	Info	2	Off	4	Data

→

Adr	Format	T-Cnt	P/F	R-Cnt	
8100	Info	3	Off	4	Data

→

Adr	Format	T-Cnt	P/F	R-Cnt	
8100	Info	4	On	4	Data

→

8100 detects a CRC failure on the second record transmitted (T-Cnt 3). The 8100 confirms T-Cnt 2 and requests that T-Cnt 3 and 4 be retransmitted.

←

Adr	Format	Cmd/Resp	P/F	R-Cnt
8100	Supr	RR	On	3

Host retransmits T-Cnt 3 and 4.

Adr	Format	T-Cnt	P/F	R-Cnt	
8100	Info	3	Off	4	Data

→

Adr	Format	T-Cnt	P/F	R-Cnt	
8100	Info	4	On	4	Data

→

8100 confirms T-Cnt 3 and 4, and has nothing to transmit.

←

Adr	Format	Cmd/Resp	P/F	R-Cnt
8100	Supr	RR	On	5

Host Polls the 8100. The 8100 detects a CRC error, and ignores the message. The Host times out waiting for a response.

Adr	Format	Cmd/Resp	P/F	R-Cnt
8100	Supr	RR	On	4

→

The Host Polls again.

Adr	Format	Cmd/Resp	P/F	R-Cnt
8100	Supr	RR	On	4

→

The 8100 has nothing to transmit.

←

Adr	Format	Cmd/Resp	P/F	R-Cnt
8100	Supr	RR	On	5

Host commands the 8100 to Disconnect (Go to Offline Mode to Host).

Adr	Format	Cmd/Resp	P/F
8100	Unnmbr	Disc	On

→

8100 acknowledges the Disconnect command, and disconnects from the Host.

←

Adr	Format	Cmd/Resp	P/F
8100	Unnmbr	UA	On

SDLC Line Protocol, Primary to Secondary

The following data represents a normal "handshake" between an SDLC primary and an SDLC secondary. The secondary address for this example is hex 21. In operation, the data may be different in some fields. The negative responses are for units that are not physically attached to the secondary.

SDLC Data	Direction "Primary→" "Secondary←"	Command	Description
7E2193BE937E	→	SNRM	
7E2173B0747E	←	UA	
7E2111A4347E	→	RR	
7E2111A4347E	←	RR	
7E21102D000000 00006B8000110101 00000000000066A47E	→	ACTPU	3276 Control Unit
7E21302D000000 0000EB8000110140 404040404040403DF77E	←		Positive response to ACTPU.
7E2131A6157E	→	RR	
7E2131A6157E	←	RR	
7E21322D000200 00006B80000D 101CB87E	→	ACTLU #2	
7E2151A0767E	←	RR	
7E2131A6157E	→	RR	
7E21522D000002 0000EB80000D01 FB817E	←		Positive response to ACTLU #2.
7E2151A0767E	→	RR	
7E2151A0767E	←	RR	
7E21542D0003 0000006B80 000D0101F3BD7C7E	→	ACTLU #3	
7E2171A2577E	←	RR	
7E2151A0767E	→	RR	
7E21742D000003 0000EB80000D 01392C7E	←		Positive response to ACTLU #3.
7E2171A2577E	→	RR	
7E2171A2577E	←	RR	
7E21762D000400 00006B800D0101 FC257E	→	ACTLU #4	

SDLC Data	Direction "Primary ⟶" "Secondary ⟵"	Command	Description
7E21962D0000 040000EF9000 800400000DC76F7E	⟵		Negative response. Unrecognized DAF.
7E2191ACB07E 7E2191ACB07E	⟶ ⟵	RR RR	
7E21982D000500 00006380000D0101 0E297E	⟶	ACTLU #5	
7E21B82D000005 0000EF90008004 00000D109E7E	⟵		Negative response to ACTLU #5.
7E21B1AE917E 7E21B1AE917E	⟶ ⟵	RR RR	
7E21BA2D000600000 6B80000D01019DE37E	⟶	ACTLU #6	
7E21DA2D000006 0000EF90008004 00000D9C267E	⟵		Negative response to ACTLU #6.
7E21D1A8F27E 7E21D1A8F27E	⟶ ⟵	RR RR	
7E21DC2D000700 00006B80000D0101 A5047E	⟶	ACTLU #7	
7E21FC2D000007 0000EF9000800400 000D39867E	⟵		Negative response to ACTLU #7.
7E21F1AAD37E 7E21F1AAD37E	⟶ ⟵	RR RR	
7E21FE2D0008 0000006B8000 0D010183177E	⟶	ACTLU #8	
7E211E2D000008 0000EF90008004 00000D3FE37E	⟵		Negative response to ACTLU #8.
7E2111A4347E 7E2111A4347E	⟶ ⟵	RR RR	

SDLC Data	Direction "Primary ⟶" "Secondary ⟵"	Command	Description
7E21102D00090000 006B80000D0101711B7E	⟶	ACTLU #9	
7E2131A6157E 7E2111A4347E	⟵ ⟶	RR RR	
7E21302D0000 090000EF9000 800400000DE8127E	⟵		Negative response to ACTLU #9.
7E2131A6157E 7E2131A6157E	⟶ ⟵	RR RR	
7E2131A6157E 7E2131A6157E	⟶ ⟵	RR RR	

CA642 BSC Line Operations

A detailed description of the 8100 system BSC line operations is available in the *8100 DPPX Base Programming Guide to System Services* GC27-0405.

BSC Description

Introduction. Binary Synchronous Communications (BSC) is a general-purpose data link control procedure permitting a variety of different devices to communicate with one another over a communications line using a common language. Control of the data link is maintained by the correct interchange of predefined control characters by the devices at each end. A "handshake" always begins the session. Under BSC protocol, the station which successfully bids for the line in a PTP configuration is assigned "primary" status. The other station is assigned "secondary" status. The session continues until it is terminated by either device. Data integrity is maintained by a block check character (BCC) included at the end of each message, and by alternately acknowledging receipt of even/odd (ACK0 or ACK1) messages. A negative acknowledgment (NAK) causes the messages to be retransmitted.

Data appears on the line as a continuous stream of bits (not separated into bytes). Synchronization is maintained by the use of highly accurate oscillators (clocks) which strobe the transmitted and received data bits and also by using a specific character (SYN) at regular intervals within the text, and at the beginning of each transmission.

Two modes of transmission are used: point-to-point and multipoint. In a point-to-point configuration, only one device is at each end of the link. See Figure CA114-2 for an illustration of point-to-point operation. A multipoint configuration consists of a master station (control station) at one end of the link and one or more stations (tributaries) on a common line at the other. Data is transferred by a poll/select procedure under control of the master station. See Figure CA114-3 for an illustration of multipoint operation.

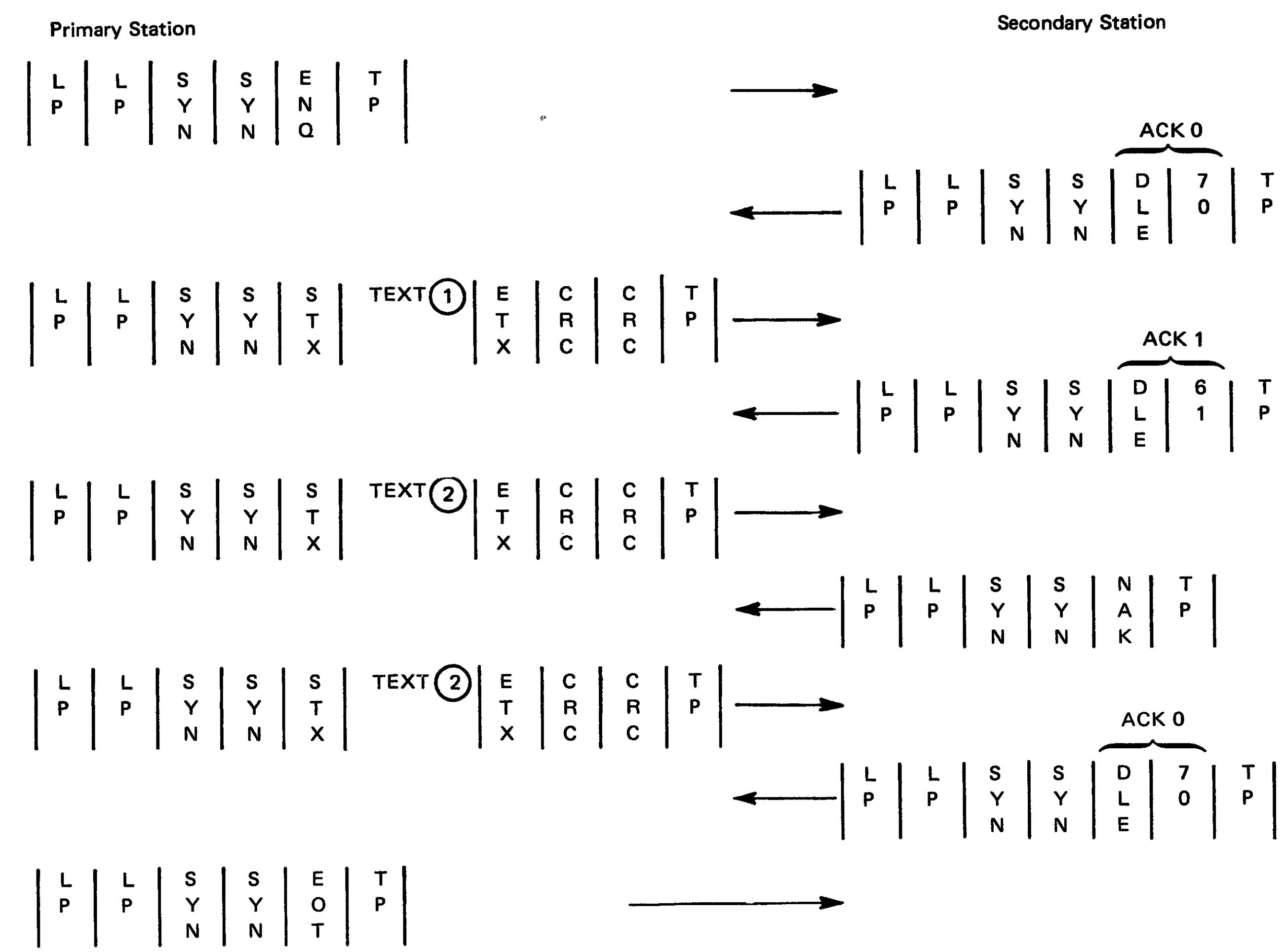
Since the line is normally held at a mark level between transmissions, it is necessary to precede each transmission with several "leading pad" characters ('55'). These Pad characters condition the electronic circuits in the modem to receive the SYN characters. Pad characters are not BSC control characters, nor are they verified for bit content.

Also, immediately following the final character of a transmission a "trailing Pad" character ('FF') is sent. This is necessary to allow all valid information to be transmitted before control lines are dropped in the modem. Two line control characters, EOT and NAK must be followed by a trailing Pad to be properly recognized.

The IBM 8100 may be either primary or secondary in a point-to-point configuration, and may be either a control or a tributary station in a multipoint operation. The 8100 may also be directly connected (no modem) to a larger system or to a terminal through the BSC/S-S adapter. In this case a point-to-point configuration is assumed.

Transparency. Because line control is maintained by the use of specific predefined characters, these line control characters cannot be included within the text portion of a message (for example, if an ETX character was received in the middle of a message, the receiving station would expect the next two characters to be BCC characters and an error would result). The transparency feature enables any of the 256 EBCDIC characters to be used as text. This is done by preventing the receiving station from recognizing a line control character unless it is preceded by a "DLE" character.

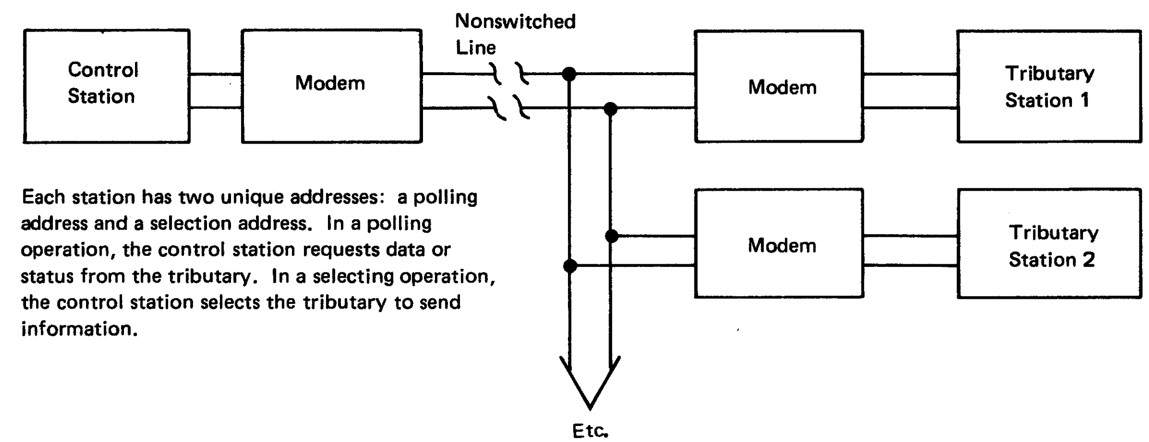
BSC Point-to-Point Operation. The following sequence illustrates a typical point-to-point BSC operation (contention). The information is illustrative only, and many other conditions could occur. The primary station is shown on the left and the secondary station is on the right. Arrows indicate the direction of transmission.



1. The primary station bids for the line by sending "ENQ". Notice framing characters (two leading Pads "LP", two synchronization characters "SYN", and trailing Pad "TP"). All messages will contain the framing sequence.
2. The secondary station receives the "ENQ" character and transmits "ACK0" (DLE 70). This indicates the secondary is ready and can receive data. If the secondary were not ready to receive, a NAK (negative acknowledgment) would have been sent.
3. Upon receipt of the "ACK0", the primary sends a block of data. The "STX" (start of text) character signifies that all information following it is text. The "ETX" (end of text) character signifies that the preceding character was the last text character and the next two characters are the "BCC" (Block Check Character). As the text was being transmitted, a 16-bit BCC was developed in the transmitting station and sent after the "ETX". The receiving station developed a BCC as the data was received. The ETX causes the receiving station to compare the BCC character received with the one that it had developed from the received data. If the two are equal, it is assumed that no transmission errors have occurred and the received message is acknowledged.

4. If the BCC check was good, the secondary sends a positive acknowledgment (ACK1). Notice that the ACK0 was used in step (2). All transmissions are alternately acknowledged with ACK1 for the first text message, ACK0 for the second, ACK1 for the third, etc. This ensures that an entire block of data has not been missed.
5. When the primary receives the proper ACK it sends the next block of data.
6. If the CRC in the secondary does not compare correctly, it sends a NAK (negative acknowledgment).
7. The primary reopens UA and resends the previous block.
8. If the CRC now checks good, the secondary sends ACK0.
9. When the primary has no further data to send, it sends "EOT", and the session is ended.

BSC Multipoint Operation. The following illustrates a typical multipoint operation. The information is illustrative only and many other conditions could occur. The master (control) station is shown on the left and the secondary (tributary) stations are on the right. Arrows indicate the direction of transmission.



Each station has two unique addresses: a polling address and a selection address. In a polling operation, the control station requests data or status from the tributary. In a selecting operation, the control station selects the tributary to send information.

Polling Operation

(1)	LP	LP	SYN	SYN	EOT	TP	SYN	SYN	P1	P1	ENQ	TP	→
(2)	←	LP	LP	SYN	SYN	EOT	TP						
(3)	LP	LP	SYN	SYN	EOT	TP	SYN	SYN	P2	P2	ENQ	TP	→
(4)	←	LP	LP	SYN	SYN	STX	TEXT	ETX	CRC	CRC	TP		
(5)	LP	LP	SYN	SYN	$\overbrace{\text{DLE} \quad \text{70}}^{\text{ACK}}$	TP	→						
(6)	←	LP	LP	SYN	SYN	EOT	TP						
(7)	LP	LP	SYN	SYN	P3	P3	ENQ	TP	→				
(8)	←	LP	LP	SYN	SYN	EOT	TP						

BSC Polling Description.

1. The control station sends initial polling messages to tributary 1. EOT is necessary to "Reset" all tributaries so that they may recognize their own address. "P1 P1" is a two-character address which is only recognized by tributary 1, and decodes as a poll.
2. Station 1 has no data to send, so it returns an EOT.
3. Control station polls station 2.
4. Station 2 has a record to send, and transmits the record as an acknowledgment to the poll.
5. Control station acknowledges receipt of records (good CRC check).
6. Station 2 has no data to send, so it sends an EOT.
7. The control station polls station 3.
8. Etc.

Selection Operation. The purpose of a selection operation is to select a tributary and send information to it. The operation is similar to polling but a differnt (selection) address is used. Upon receipt of a positive acknowledgement from the station (ACK0), a normal transfer ensues.

BSC Line Control Characters

Nmemonic	Name of Function	Actual Sequence	Hex Value
ACK 0	Even Acknowledge	DLE 70	1070
ACK 1	Odd Acknlowledge	DLE 61	1061
DISC**	Mandatory Disconnect	DLE EOT	1037
DLE	Data Link Escape	DLE	10
ENQ	Enquiry	ENQ	2D
EOT*	End of Transmission	EOT + TR PAD	37
ETB	End of Transmission Block	ETB	26
ETX	End of Text	ETX	03
ITB	End of Intermediate Transmission Block	ITB	1F
NAK*	Negative Acknowledge	NAK + TR PAD	3D
RVI	Reverse Interrupt	DLE @	107C
SOH	Start of Heading	SOH	01
STX	Start of Text	STX	02
SYN	Synchronous Idle	SYN	32
TTD	Temporary Text Delay	STX ENQ	022D
WACK	Wait Before Transmit Positive Acknowledge	DLE 9	106B
XDLE*	Data DLE in Transparent Idle	DLE DLE	1010
XENQ*	Transparent Block Cancel	DLE ENQ	102D
XETB*	End of Transmission Block	DLE ETB	1026
XETX*	End of Text	DLE ETX	1003
XITB*	End of Intermediate Transmission Block	DLE ITB	101F
XSTX*	Start of Text	DLE STX	1002
XSYN*	Synchronous Idle	DLE SYN	1032
XTTD*	Temporary Text Delay	DLE STX DLE ENQ	1002102D

Transparent Mode only
*Sw. Line only
**Require 4 Low-Order Bits of Trailing Pad Character (all 1 bits)

BSC Transmission Sequences

This section describes the various BSC transmission sequences used by the 8100. Both the data link BSC sequences and the batch program sequences are described. The data link sequences are presented via flow direction; that is, inbound implies inbound to the 8100 from a host computer, and outbound implies outbound to the host computer from the 8100. A host must support all outbound sequences, but it need send only those inbound sequences relevant to a particular function or task.

These sequences are presented without showing the following:

Leading PAD and SYN characters

Trailing PAD character

Transparency DLE where applicable

ACK0/1 specific designation

For example, a typical poll message would look as follows:

PAD/SYN/SYN/EOT/SYN/SYN/SA/SA/da/ENQ/PAD, with the following interpretations

PAD	= hex 55	SA	= Station address in capitals
SYN	= hex 32	da	= Device Address
EOT	= hex 37	ENQ	= hex 2D

These sequences are shown assuming a BSC3 implementation, that is, poll/select. For BSC2, these sequences would consist of appropriate ENQ–ACK0 bids prior to establishing message transfer state.

Addressing Assumptions. The following station and device addresses will apply for the 8100.

Station address: Any alphabetic character from A–Z, for example, 'A'.

Poll station address: Upper case duplicated, for example, 'AA', that is, hex C1C1.

Select station address: Lower case duplicated, for example, 'aa', that is hex 8181.

Note: *The 8100 performs a simple "anding" off of bit 1 of the address byte to convert from uppercase to lowercase.*

Device Address:

Poll device address:	1 & 2, that is, hex F1 = Batch hex F2 = Inquiry
Select device address batch:	1, that is, hex F1
Select device address inquiry:	2, that is, hex F2

Response Considerations When No I/O Is Pending In 8100

Polling Response:	8100 responds EOT if no write is pending.
Selection Response:	8100 responds NAK if no read is pending.
Within an Outbound Chain:	8100 responds TTD if no write is pending within 2 seconds.
Within an Inbound Chain:	8100 responds WACK if no read is pending within 2 seconds.

BSC2 — Switched Line Support Assumptions

Caller Considerations. Prior to making the physical line connection, the host application program must be started, and the 8100 control operator must enable the batch or inquiry session at the 8100. The line connection may then be completed in several ways.

For batch sessions, the telephone call may be a manual or an auto-call. The 8100 may manually answer or auto-answer. For batch sessions, the host computer always bids for the line first.

For inquiry sessions, the telephone call is always originated manually. The host may manually answer or auto-answer. For inquiry sessions, the 8100 always bids for the line first.

After the line connection is completed, a specific bid null transaction must always be transmitted before normal data can be exchanged.

Batch Sessions

Host		8100
ENQ	→	
	←	ACK0
EOT	→	

Inquiry Sessions

Host		8100
	←	ENQ
ACK0	→	
	←	EOT

Note: *There is never any text transmitted in the initial bid null transaction.*

Intertransaction Sequences. BSC2 is a contention discipline. Thus, at the end of a transaction, either party may attempt to bid for the line. However, 8100 operations do not lend themselves to a contention environment. The programs involved must follow a strict sequence as defined by their design, and the 8100 system itself does not permit asynchronous I/O. Furthermore, the host access method (BTAM) requires an alternating pattern of transactions. That is, when the host sends a transaction, the 8100 must next send a transaction. This requirement does not match the data flow requirements of the 8100. However, it must be dealt with.

Accordingly, the 8100 has adopted the following conventions within BSC2. The 8100 always bids for the line following all transactions (whether host-originated or 8100-originated). The 8100 then maintains a series of TTDs on the line until it has received a specific read or write from its application. For a write, it immediately sends data. For a read, it sends an EOT to relinquish the line and awaits a bid (ENQ) from the host. Thus, in effect, the line is driven by the 8100 and the 8100 application. Bids for the line by the host not following these conventions are ignored by the 8100.

The following sequences apply:

Host Ending a Transaction

Host		8100
EOT	⟶	
	⟵ ENQ	
ACK0	⟶	
[	⟵ TTD]	
[NAK	⟶]	Repeated until specific read or write.

8100 Ending a Transaction

Host		8100
	⟵ EOT	
	⟵ ENQ	
ACK0	⟶	
[	⟵ TTD]	
[NAK	⟶]	Repeated until specific read or write.

8100 Application Initiating a Read

Host		8100
[	⟵ TTD]	
[NAK	⟶]	
	⟵ EOT Application Read	
Application Write ENQ	⟶	
	⟵ ACK0	
Text	⟶	
	⋮	

8100 Application Initiating a Write

Host		8100
[	⟵ TTD]	
[NAK	⟶]	
Application Read	⟵ Text	Application Write
	⋮	

Session Termination. Sessions are terminated either at the end of their operations or prematurely (as a result of some error conditions). The 8100 ends a session prematurely for a variety of reasons. Those having to do with the detection of a BSC protocol violation originating at the host cause the 8100 to disconnect the line. Those having to do with hard errors detected by the 8100 (preventing further transmission) cause the 8100 to disconnect the line.

Cancel Inbound

(Host-Originated)

Host		8100
EOT/SYN/SYN/sa/sa/da/ENQ	⟶	
	⟵ ACK	
STX/Data/ETB	⟶	
	⟵ ACK	
EOT	⟶	

(8100-Originated)

Host		8100
EOT/SYN/SYN/sa/sa/da/ENQ	⟶	
	⟵ ACK	
STX/Data/ETB	⟶	
	⟵ ACK	
STX/Data/ETB	⟶	
	⟵ RVI	
EOT	⟶	

Delay Inbound

(Host-Originated)

Host		8100
EOT/SYN/SYN/sa/sa/da/ENQ	⟶	
	⟵ ACK	
STX/Data/ETB	⟶	
	⟵ ACK	
TTD	⟶	
	⟵ NAK	
TTD	⟶	
	⟵ NAK	
STX/Data/ETB	⟶	
	⟵ ACK	
	⋮	

(8100-Originated)

Host		8100
EOT/SYN/SYN/sa/sa/da/ENQ	⟶	
	⟵ ACK	
STX/Data/ETB	⟶	
	⟵ WACK	
ENQ	⟶	
	⟵ WACK	
ENQ	⟶	
	⋮	
	⟵ ACK	
STX/Data/ETB	⟶	
	⋮	

8100 Inbound BSC Sequences

Program operations that terminate normally do not cause the 8100 to disconnect the line unless the administrative operator has previously attempted to disable the sessions. Thus, if the host program terminates normally and wants the line disconnected, it should do so and not assume the 8100 will. If the host program knows that several 8100 programs may run during one connection, then it should not disconnect the line.

The 8100 attempts to send the BSC disconnect sequence when 8100 is going on-hook. Likewise, it goes on-hook if it detects the disconnect sequence. The disconnect sequence is:

DLE/EOT

Thus, an FP CLOSESS statement causes the line to be disconnected only if the administrative operator has previously issued a SYSHOST disable inquiry session. If there are no sessions outstanding and the operator issues a SYSHOST disable inquiry session, the line will be disconnected, and the 8100 will go on-hook.

In the case of the batch session, if the 8100 is running in unattended mode (that is, the administrative operator has invoked SYSTERM with the Disable All option or the Disable Shutdown option), the 8100 goes on-hook at the end of a batch session. If no power-down message has been received, the 8100 then reenables and monitors for an incoming call. If the 8100 is running in attended mode, it similarly goes on-hook. However, it does not monitor for another incoming call unless the administrative operator reenables batch.

Note: *In the following sequences, all start-of-block and end-of-block controls should be considered in transparent mode, for example, DLE/STX, DLE/ETB, DLE/ETX.*

Normal Receiving of Data

(1 Block - 1 Chain)

Host		8100
EOT/SYN/SYN/sa/sa/da/ENQ	→	
	←	ACK
STX/DATA/ETX	→	
	←	ACK
EOT	→	

(Multiblocks - 1 Chain)

Host		8100
EOT/SYN/SYN/sa/sa/da/ENQ	→	
	←	ACK
STX/Data/ETB	→	
	←	ACK
STX/Data/ETB	→	
	←	ACK
STX/Data/ETX	→	
	←	ACK
EOT	→	

Normal Receiving of Data – Switched

(1 Block)

Host		8100
[	←	TTD]
[NAK	→	]
	←	EOT
ENQ	→	
	←	ACK
DLE/STX/Data/DLE/ETX	→	
	←	ACK
EOT	→	
	←	ENQ
ACK	→	
[	←	TTD]
[NAK	→	]

(Multiblocks)

Host		8100
[	←	TTD]
[NAK	→	]
	←	EOT
ENQ	→	
	←	ACK
DLE/STX/Data/DLE/ETB	→	
	←	ACK
DLE/STX/Data/DLE/ETB	→	
	←	ACK
DLE/STX/Data/DLE/ETX	→	
	←	ACK
EOT	→	
	←	ENQ
ACK	→	
[	←	TTT]
[NAK	→	]

8100 Outbound BSC Sequences

Note: *In the following sequences, all start-of-block and end-of-block controls should be considered in transparent mode, for example, DLE/STX, DLE/ETB, DLE/ETX.*

Normal Sending of Data

(1 Block - 1 Chain)

Host	8100
EOT/SYN/SYN/SA/SA/da/ENQ →	
	← STX/Data/ETX
ACK →	
	← EOT

(Multiblocks - 1 Chain)

Host	8100
EOT/SYN/SYN/SA/SA/da/ENQ →	
	← STX/Data/ETB
ACK →	
	← STX/Data/ETBn−1
ACK →	
	← STX/Data/ETX
ACK →	
	← EOT

Cancel Outbound

(8100 - Originated)

Host	8100
EOT/SYN/SYN/SA/SA/da/ENQ →	
	← STX/Data/ETB
ACK →	
	← EOT

(Host - Originated)

Host	8100
EOT/SYN/SYN/SA/SA/da/ENQ →	
	← STX/Data/ETB
RVI →	
	← EOT

(Host will now transmit)

Delay Outbound

(Host - Originated)

Host	8100
EOT/SYN/SYN/SA/SA/da/ENQ →	
	← STX/Data/ETB
WACK →	
	← ENQ
•	•
•	•
•	•
	← ENQ
ACK →	
	← STX/Data/ETB
	•
	•
	•
	•

(8100 - Originated)

Host	8100
EOT/SYN/SYN/SA/SA/da/ENQ →	
	← STX/Data/ETB
ACK →	
	← TTD
NAK →	
	← TTD
NAK →	
	•
	•
	•
	← STX/Data/ETB
ACK →	
	•
	•
	•

Normal Sending of Data - Switched

(1 Block)

Host	8100
[	← TTD]
[NAK →]	
	← DLE/STX/Data/DLE/ETX
ACK →	
	← EOT
	← ENQ
ACK →	
	← TTD
NCK →	

(Multiblocks)

Host	8100
	← TTD
NAK →	
	← DLE/STX/Data/DLE/ETB
ACK →	
	← DLE/STX/Data/DLE/ETB
ACK →	
	← DLE/STX/Data/DLE/ETX
ACK →	
	← EOT
	← ENQ
ACK →	
	← TTD
NAK →	

Unrecoverable Error

(8100 - Detected)

Host	8100
EOT/SYN/SYN/sa/sa/da/ENQ →	
	← ACK
STX/Data/ETB →	
	Error
	(← EOT)

(Host - Detected)

Host	8100
EOT/SYN/SYN/SA/SA/da/ENQ →	
	← STX/Data/ETB
ACK →	
	← STX/Data/ETB
	Error (time out)

Miscellaneous BSC Sequences

Multipoint Leased — (BSC3). Message transmission between computer and 8100 via a multipoint line is initiated only by the computer, using a Read Initial or Write Initial transparent operation. There are polling and selection sequnces in terminal lists (called "polling lists" for polling sequences and "addressing lists" for selection sequences). (The terms "selection" and "addressing" are used here synonymously.) The DFTRMLST macro instruction is used to create the terminal lists. The READ or WRITE macro instruction that initiates message transmission sends the polling or selection sequences contained in the list.

Polling and selection sequences consist of four characters. The first is the terminal address, which may be any alphabetic character; it identifies an individual terminal and is set by the service representative when the terminal is installed. In a polling sequence, this character must appear in uppercase, for example, "A." When in a selection sequence, it must be lowercase, for example, "a."

The second character is always identical with the first. The third character in the sequence is a component polling or selection character. The character "1" is used for batch sessions, and character "2" is used for inquiry sessions.

The fourth character in the sequence is always ENQ (inquiry); it elicits a response from the terminal control unit, which indicates whether the polled or selected component is ready.

Terminal Polling and Selection for BSC3. To activate a terminal so that data transmission can occur, the center computer (host) transmits on the communications line a specific character sequence that identifies the terminal. The procedure is called "polling" when the 8100 has to send to the host and "selection" when the host has to send to the 8100. The character sequences are called polling sequences and selection sequences. Specific polling and selection sequences are assigned to the 8100 control unit.

Double Addressing (Multipoint Lines). Transient conditions such as lightning impulses or switching pulses can introduce errors in data transmitted over a communication line. Often, such errors consist of inverted bit setting of a character. Errors of this kind occurring in message data are normally detected through checking techniques; however, they are undetected when they occur in polling and addressing (selection) sequences, which are unchecked. An error wherein one valid polling or addressing character is changed to another can result in polling or addressing the wrong station.

To avoid such an occurrence, double-addressing is employed for 8100 stations. In this technique, a remote station is represented by two identical characters rather than by one character as in single addressing.

When polled or addressed, the remote station that recognizes the first character compares it with the second. If the two are identical, the station address is presumed to be correct, and the station returns a positive response. If they differ, a transmission error is presumed to have altered one or both of the characters, and the station does not return a response.

The increased polling and addressing reliability this technique affords stems from the improbability of both of the characters being changed in precisely the same way by a transmission error. For example, the characters BB are far less likely to be converted by an error to CC than they are to be converted to BC, or KB, or FC. (Each of these conversions could result from a single-bit error in each character, where the transmission code is EBCDIC. For example, the letter B, the bit pattern for which is hex C2 (1100 0010). becomes a C (hex C3, 1100 0011) or a K (hex D2, 1101 0010) through a single-bit error.) If a station whose address is K was attached to the line, that station would recognize the first character of the erroneous address KB, but would not respond because the two characters did not match. Thus, a message intended for station B would not be sent to station K instead.

Response Considerations When No I/O Is Pending In 8100:

Polling Response:	8100 responds EOT if no write is pending.
Selection Response:	8100 responds NAK if no read is pending.
Within an Outbound Chain:	8100 responds TTD if no write is pending within 2 seconds.
Within an Inbound Chain:	8100 responds WACK if no read is pending within 2 seconds.

BATCH BSC TRANSMISSION SEQUENCES (BSC3)

Session Initiation/Termination

Session Initiation

1 of the following

Some form of Query

Host 8100

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Query/DLE/ETX →
← ACK
EOT →

or a Ready

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Host Transm. Ready/DLE/ETX →
← ACK
EOT →

Session Termination

Status - Error Message - End this batch session

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Status - Error - End this session/DLE/ETX →
← ACK
EOT →

Batch Sequences

BSC Transaction Record Sequences

Query for Completed Transactions

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Query/DLE/ETX →
← ACK
EOT →

Transmit Completed Transactions

EOT/SYN/SYN/SA/SA/da/ENQ →
← DLE/STX/HDR/DLE/ETB
ACK →
← DLE/STX/BLK/DLE/ETX
ACK →
← EOT
EOT/SYN/SYN/SA/SA/da/ENQ →
← DLE/STX/HDR/DLE/ETB
ACK →
← DLE/STX/BLK1/DLE/ETB
ACK →
← DLE/STX/BLKN/DLE/ETX
ACK →
← EOT

Status - EODT

Host 8100

EOT/SYN/SYN/SA/SA/da/ENQ →
← DLE/STX/EODT/DLE/STX
ACK →
← EOT

Status - Complete

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Complete/DLE/ETX →
← ACK
EOT →

8100 Abend Dump Sequences

Query for 8100 Abend Dumps

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Query/DLE/ETX →
← ACK
EOT →

Transmit 8100 Abend Dump

EOT/SYN/SYN/SA/SA/da/ENQ →
← DLE/STX/HDR/DLE/ETB
ACK →
← DLE/STX/BLK1/DLE/ETB
ACK →
← DLE/STX/BLKN/DLE/ETX
ACK →
← EOT

Status - EODT

EOT/SYN/SYN/SA/SA/da/ENQ →
← DLE/STX/EODT/DLE/ETX
ACK →
← EOT

Status - Complete

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Complete/DLE/ETX →
← ACK
EOT →

8100 Host Message

Host 8100

Query for 8100 Host Messages

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Query/DLE/ETX →
← ACK
EOT →

Transmit 8100 Host Message

EOT/SYN/SYN/SA/SA/da/ENQ →
← DLE/STX/HDR/DLE/ETB
ACK →
← DLE/STX/MSG/DLE/ETX
ACK →
← EOT

Status - EODT

EOT/SYN/SYN/SA/SA/da/ENQ →
← DLE/STX/EODT/DLE/ETX
ACK →
← EOT

Status-Complete

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Complete/DLE/ETX →
← ACK
EOT →

Create DSCB

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Host Transm. Ready/DLE/ETX →
← ACK
EOT →

Create DSCB

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/HDR/DLE/ETB →
← ACK
DLE/STX/BLK1/DLE/ETX →
← ACK
EOT →

Status - EODT

Host 8100

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/EODT/DLE/ETX →
← ACK
EOT →

Status - Complete

EOT/SYN/SYN/SA/SA/da/ENQ →
← DLE/STX/Complete/DLE/ETX
ACK →
← EOT

Delete DSCB

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Host Transm. Ready
DLE/ETX →
← ACK
EOT →

Delete DSCB

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Delete DSCB/DLE/ETX →
← ACK
EOT →

Status - EODT

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/EODT/DLE/ETX →
← ACK
EOT →

Status Complete

EOT/SYN/SYN/SA/SA/da/ENQ →
← DLE/STX/Complete/DLE/ETX
ACK →
← EOT

Host Transmission Ready

Host 8100

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Host Transm. Ready/
DLE/ETX →
← ACK
EOT →

Add Indexed Data Record

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Add Indexed Record
Header/DLE/ETB →
← ACK
DLE/STX/BLK1/DLE/ETB →
← ACK
DLE/STX/BLKN/DLE/ETX →
← ACK
EOT →

Status - EODT

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/EODT/DLE/ETX →
← ACK
EOT →

Status - Complete

EOT/SYN/SYN/SA/SA/da/ENQ →
← DLE/STX/Complete/DLE/ETX
ACK →
← EOT

Delete Indexed Data Records

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Host Transm. Ready/
DLE/ETX →
← ACK
EOT →

Delete Indexed Data Record

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Delete Index Record Header/DLE/ETX →
← ACK
EOT →

Host Transmission Ready

Host 8100

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Ready/DLE/ETX →
← ACK
EOT →

Replace Indexed Data Record

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Replace Index Record HDR/DLE/ETB →
← ACK
DLE/STX/BLK1/DLE/ETB →
← ACK
DLE/STX/BLKN/DLE/ETX →
← ACK
EOT →

Status - EODT

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/EODT/DLE/ETX →
← ACK
EOT →

Status - Complete

EOT/SYN/SYN/SA/SA/da/ENQ →
← DLE/STX/Complete/DLE/ETX
ACK →
← EOT

Host Transmission Ready

Host 8100

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Host Transm. Ready/DLE/ETX →
← ACK
EOT →

Replace Relative Data Record

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/HDR/DLE/ETB →
← ACK
DLE/STX/BLKX/DLE/ETB →
← ACK
EOT →

Status - EODT

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/EODT/DLE/ETX →
← ACK
EOT →

Status - Complete

EOT/SYN/SYN/SA/SA/da/ENQ →
← DLE/STX/Complete/DLE/ETX
ACK →
← EOT

Status - EODT

Host 8100

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/EODT/DLE/ETX →
← ACK
EOT →

Status Complete

EOT/SYN/SYN/SA/SA/da/ENQ →
← DLE/STX/Complete/DLE/ETX
ACK →
← EOT

Send 8100 Print Record

Host Transmission Ready

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Host Transm. Ready/DLE/ETX →
← ACK
EOT →

Send Print Record

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/HDR/DLE/ETB →
← ACK
DLE/STX/BLK1/DLE/ETB →
← ACK
•
•
•
DLE/STX/BLKN/DLE/ETX →
← ACK
EOT →

Status - EODT

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/EODT/DLE/ETX →
← ACK
EOT →

Status - Complete

EOT/SYN/SYN/SA/SA/da/ENQ →
← DLE/STX/Complete/DLE/ETX
ACK →
← EOT

Host Transmission Ready

Host 8100

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Host Transm. Ready/DLE/ETX →
← ACK
EOT →

Add 8100 FP

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/HDR/DLE/ETB →
← ACK
DLE/STX/BLK1/DLE/ETB →
← ACK
•
•
•
DLE/STX/BLKN/DLE/ETX →
← ACK
EOT →

Status - EODT

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/EODT/DLE/ETX →
← ACK
EOT →

Status - Complete

EOT/SYN/SYN/SA/SA/da/ENQ →
← DLE/STX/Complete/DLE/ETX
ACK →
← EOT

Delete FP

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Host Transm. Ready/DLE/ETX →
← ACK
EOT →

Host 8100

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/DeleteFP/DLE/ETX →
← ACK
EOT →

Status - EODT

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/EODT/DLE/ETX →
← ACK
EOT →

Status - Complete

EOT/SYN/SYN/SA/SA/da/ENQ →
← DLE/STX/Complete DLE/ETX
ACK →
← EOT

BSC Sender Program Cancel Message and Error Status

Host Initiated

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/BLK/DLE/ETB →
← ACK
EOT →
EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Error Status/DLE/ETX →
← ACK
EOT →

8100 Initiated

EOT/SYN/SYN/SA/SA/da/ENQ →
← DLE/STX/BLK/DLE/ETB
ACK →
← EOT
EOT/SYN/SYN/SA/SA/da/ENQ →
← DLE/STX/Error Status/DLE/ETX
ACK →
← EOT

BSC Sender Program Cancel Message and Error Status

Host Initiated

Host 8100

EOT/SYN/SYN/Sa/Sa/da/ENQ →
← DLE/STX/HDR/DLE/ETB
ACK →
← DLE/STX/BLK/DLE/ETB
RVI (pos. Ack.) →
← EOT
EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/Error Status /DLE/ETX →
← ACK
EOT →

Note: *In batch mode, it is the RVI Senders responsibility to send the next message. This would normally be a status error message.*

8100 Initiated

EOT/SYN/SYN/sa/sa/da/ENQ →
← ACK
DLE/STX/HDR/DLE/ETB →
← ACK
DLE/STX/BLK/DLF/ETB →
← RVI (pos. ack.)
EOT →
EOT/SYN/SYN/SA/SA/da/ENQ →
← DLE/STX/Error Status/DLE/ETX
ACK →
← EOT

Note: *In the above sequences, the 8100 enforces the flow of an EOT following an RVI. It will always send one following the receipt of an RVI. It will send one EOT as a response to a block if the host fails to send an EOT following the receipt of an RVI.*

CA643 Start/Stop 2741

Start/Stop is an asynchronous method of communications. The data is usually transferred over the communications line one character at a time, and the line is held at a mark level between characters. Since the characters may be sent at random intervals (usually they are entered from a keyboard), there is no synchronization within a block of data. Each character, however, contains a predetermined format which enables the receiving station to maintain synchronization within the character. There are also several unique line control characters which maintain discipline on the link. Each character contains a check bit (parity) to ensure data integrity.

Two ways of transmission are used: point-to-point and multipoint. In a point-to-point configuration, only one device is at each end of the line. (See Figure CA114-2 for an illustration of point-to-point operation.) A multipoint configuration consists of a master station (control station) at one end of the link and one or more stations (tributaries) on a common line at the other. Data is transferred by a poll/select procedure under control of the master station. (See Figure CA114-3 for an illustration of multipoint operation.)

The usual start/stop data link consists of one or more terminals (secondary stations) communicating with a more intelligent device (primary station). In a start/stop configuration, the 8100 will always be the primary device or multipoint control station. The 8100 may also be directly connected (no modem) to a station.

External 2741 Data Flow

Data flow (Figure CA643-1) in an IBM 2741 Communications Terminal can be in either of two directions:

1. From the 2741 through the data set to the multiplexer and computer.
2. From a computer through a multiplexer, through a data set to the 2741.

During the send operation, data is printed by the Selectric typewriter at the same time that it is sent out over the line to the computer.

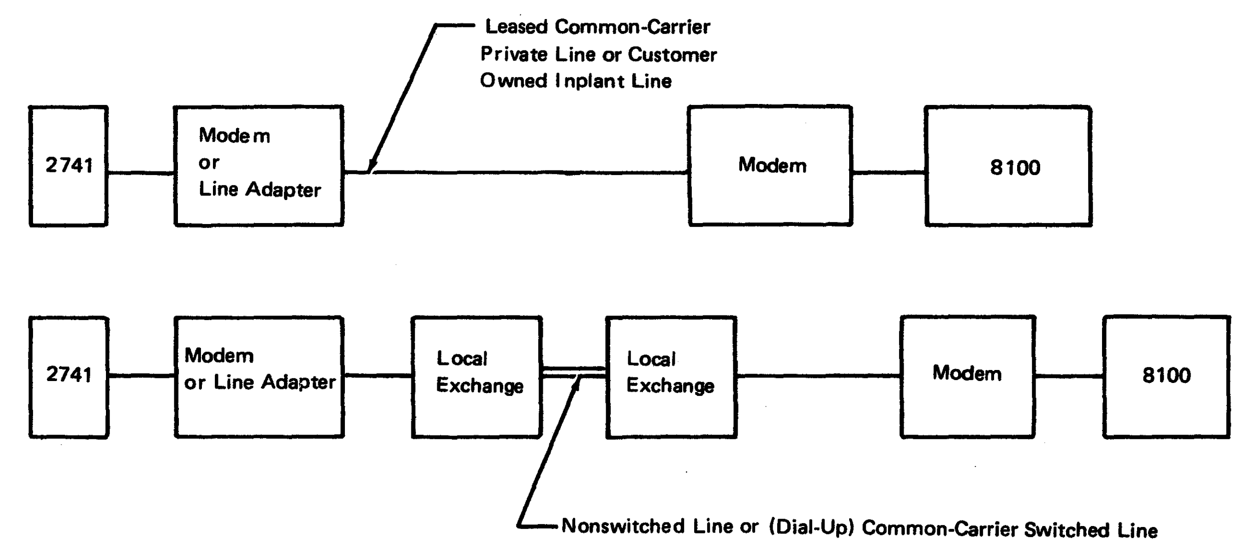


Figure CA643-1. Data Flow In a Point-to-Point Configuration

IBM 2741 Line Control

Line control becomes effective on the 2741 when the terminal power switch is turned on and the terminal mode switch is set to communicate. The terminal is then in a transmit state and a D code is sent to the 8100 (Figures CA643-2 and CA643-3). The operator may transmit by keying as on a typewriter.

Terminal transmission ends when the terminal transmits a C . The C is transmitted when the attention key or the carrier return key is pressed. However, when the carrier return key is pressed, a carrier return code precedes the C code. Transmission of the C code places the terminal in the receive control mode and the keyboard is locked waiting for a D code from the computer.

The computer, after receiving the C code, transmits a D code placing the terminal in the receive mode. Any valid character code then received from the computer causes printing. At the end of transmission, the computer sends a C code to the terminal.

The terminal, after receiving the C code, switches to transmit mode. The keyboard is unlocked and the terminal automatically transmits a D code.

Figure CA643-3 shows a typical line-control sequence. The sequence can be ended only by the terminal. The operator terminates line-control by switching to local mode or by turning the terminal power switch off. Transmissions from the 2741 terminal are not checked for vertical or longitudinal redundancy.

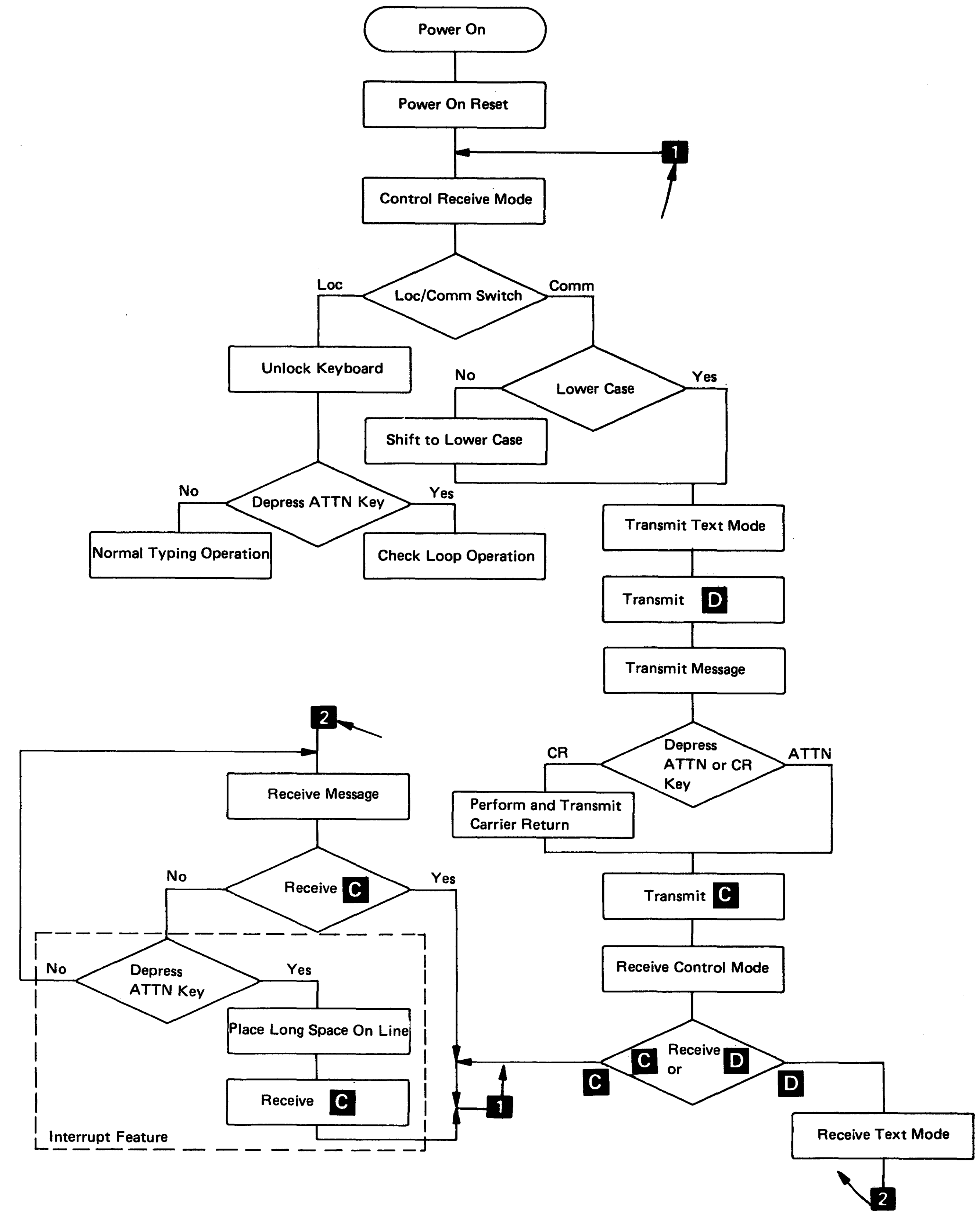


Figure CA643-2. IBM 2741 (with Interrupt Feature) Flow Chart

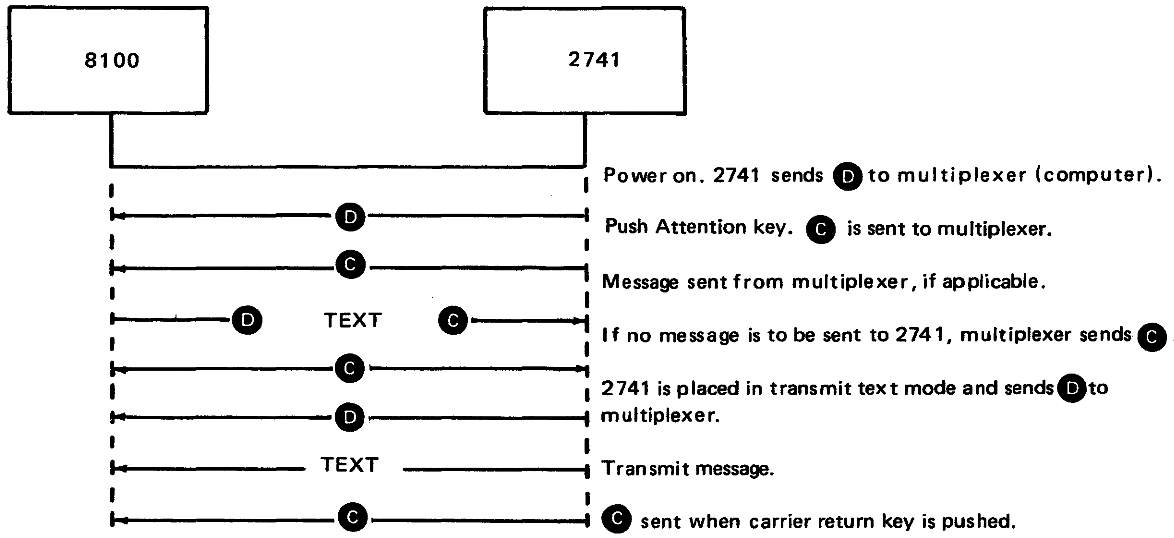


Figure CA643-3. IBM 2741 Line Control

Codes

The standard 2741 uses binary coded decimal (BCD) code consisting of six information bits and a check bit arranged: B, A, 8, 1, 2, 1, C. The six information bits identify all alphanumeric characters for the I/O Selectric as well as all control codes needed for semiautomatic operation while communication is in process. The check bit maintains odd parity. A valid character must contain an odd number of bits and the code for an even-bit character will contain a check bit.

A 2741 character is generated by the I/O transmitting contacts and translated to BCD in a diode matrix before leaving the I/O. BCD from the line is used throughout the 2741. Figure CA643-5 shows the BCD code chart. The standard 2741 uses correspondence code (Figure CA643-4). Characters are transmitted and received by the 2741 in the same bit order as for BCD mode but the bit configuration for the same character may be different. For example, the letter A in BCD code is B, A, 1; in correspondence code an A is B, 4, 2, 1, plus the check bit. Which of the two codes is used in a terminal is determined by mechanical changes within the I/O. No circuit changes are required. The 2741 can be supplied with any of the three codes: correspondence, BCD, or extended BCD. However, all interconnected terminals in a system should use the same code.

Character Format. A BCD character consists of seven bits. In order to use this character as the input or output of the terminal, two bit positions are added. These are the start bit (ST) and stop bit (SP); the ST bit is always a 0-bit and the SP bit is always a 1-bit. The start bit enables the terminal to recognize the start of a new character. (The line is maintained in a marking condition between characters.) The stop bit separates the characters. Without a stop bit, the two BCD characters "C" and "A", for example, would run together as follows:

ST	B	A	8	4	2	1	C	ST	B	A	8	4	2	1	C
0	1	1	0	0	1	1	1	0	1	1	0	0	0	1	0

Because the arrival of a start bit is not easily identified, a stop bit is added at the end of the character: the "A" and "C" now appear:

ST	B	A	8	4	2	1	C	SP	ST	B	A	8	4	2	1	C	SP
0	1	1	0	0	1	1	1	1	0	1	1	0	0	0	1	1	1

The stop bit allows the interval between characters to reset the terminal in preparation for the next character.

Control Codes. The control codes along with the shorthand representation of the codes are shown in Figures CA643-4, CA643-5 and CA643-6. When the terminals are in control mode, the codes do not print. B and C are not printable in any mode. When the terminals are in receive or transmit mode, other codes will print. Thus, for the most part, the machine mode determines the interpretation of the control codes.

LOWER CASE	Bit Value B	A	C	8	4	2	1	UPPER CASE
.	B		C			2		.
;	B	A	C		4		1	:
,	B	A			4	2	1	,
'	B		C		4			"
!	B							°
=	B	A				2		+
-	B	A		8		2	1	−
/	B	A		8				?
1/]							1	±/[
2						2		@
3			C			2	1	#
4				8				$
5					4			%
6			C		4	2		¢
7			C		4		1	&
8					4	2	1	*
*9				8		2	1	(
0			C	8			1	)
a	B		C		4	2	1	A
b		A	C	8		2	1	B
c		A	C		4	2	1	C
d		A			4		1	D
e		A	C		4			E
f	B	A	C			2	1	F
g	B	A					1	G
h		A		8			1	H
i	B				4	2		I
j	B	A	C					J
k		A			4	2		K
l		A	C	8				L
m	B		C				1	M
n		A	C			2		N
o	B		C	8				O
p	B	A			4			P
q	B	A	C		4	2		Q
r	B				4		1	R
s	B			8			1	S
t		A						T
u		A				2	1	U
v	B					2	1	V
w	B		C	8		2	1	W
x		A	C				1	X
y	B	A	C	8			1	Y
z			C	8		2		Z

THE CODES BELOW ARE NOT PRINTABLE								
FUNCTION CODES								MEANING
PN			C	8	4			Punch On
BY		A		8	4			Bypass
RES	B			8	4			Restore
PF	B	A	C	8	4			Punch Off
RS				8	4		1	Reader Stop
LF		A	C	8	4		1	Line Feed
NL	B		C	8	4		1	New Line (Carrier Return and Line Feed)
HT	B	A		8	4		1	Horizontal Tab
UC				8	4	2		Upper Case
EOB		A	C	8	4	2		End of Block
BS	B		C	8	4	2		Backspace
LC	B	A		8	4	2		Lower Case
*EOT			C	8	4	2	1	End of Transmission
PRE		A		8	4	2	1	Prefix
IL	B			8	4	2	1	Idle
DEL	B	A	C	8	4	2	1	Delete
Space			C					Space

Figure CA643-4. IBM 2741 Line Code Chart (Standard Selectric Typewriter Print Element)

LOWER CASE											UPPER CASE			
CHARACTER SET				Bit Value							CHARACTER SET			
Std.	A	H	Typ.	B	A	C	8	4	2	1	Std.	A	H	Typ.
.				B	A		8		2	1	.			
$			;	B		C	8		2	1	!			:
,					A	C	8		2	1	,			
*#		=	'				8		2	1	±	#		"
@		'	1/2		A						¢	Δ		1/4
&		+	=	B	A	C					+	<		+
-				B							—	\		—
/					A	C				1	?			
1										1	=	>		±
2									2		o		)	@
3						C			2	1	;			#
4								4			:	b̸		$
5						C		4		1	%		(	%
6						C		4	2		'	:		¢
7								4	2	1	"			&
8							8				*			
9						C	8			1	(	[		(
0						C	8		2		)	]		)
a				B	A					1	A			
b				B	A				2		B			
c				B	A	C			2	1	C			
d				B	A			4			D			
e				B	A	C		4		1	E			
f				B	A	C		4	2		F			
g				B	A			4	2	1	G			
h				B	A		8				H			
i				B	A	C	8			1	I			
j				B		C				1	J			
k				B		C			2		K			
l				B					2	1	L			
m				B		C		4			M			
n				B				4		1	N			
o				B				4	2		O			
p				B		C		4	2	1	P			
q				B		C	8				Q			
r				B			8			1	R			
s					A	C			2		S			
t					A				2	1	T			
u					A	C		4			U			
v					A			4		1	V			
w					A			4	2		W			
x					A	C		4	2	1	X			
y					A	C	8				Y			
z					A		8			1	Z			

THE CODES BELOW ARE NOT PRINTABLE								
FUNCTION CODES								MEANING
PN			C	8	4			Punch On
BY		A		8	4			Bypass
RES	B			8	4			Restore
PF	B	A	C	8	4			Punch Off
RS				8	4		1	Reader Stop
LF		A	C	8	4		1	Line Feed
NL	B		C	8	4		1	New Line (Carrier Return and Line Feed)
HT	B	A		8	4		1	Horizontal Tab
UC				8	4	2		Upper Case
EOB		A	C	8	4	2		End of Block
BS	B		C	8	4	2		Backspace
LC	B	A		8	4	2		Lower Case
*EOT			C	8	4	2	1	End of Transmission
PRE		A		8	4	2	1	Prefix
IL	B			8	4	2	1	Idle
DEL	B	A	C	8	4	2	1	Delete
Space			C					Space

Figure CA643-5. IBM 2741 Line Code Chart (PTTC/BCD)

LOWER CASE	Bit Value B	A	C	8	4	2	1	UPPER CASE
.	B	A		8		2	1	¬
$	B		C	8		2	1	!
,		A	C	8		2	1	|
*#				8		2	1	"
@		A						¢
&	B	A	C					+
-	B							_
/		A	C				1	?
1							1	=
2						2		<
3			C			2	1	;
4					4			:
5			C		4		1	%
6			C		4	2		'
7					4	2	1	>
8				8				*
9			C	8			1	(
0			C	8		2		)
a	B	A					1	A
b	B	A				2		B
c	B	A	C			2	1	C
d	B	A			4			D
e	B	A	C		4		1	E
f	B	A	C		4	2		F
g	B	A			4	2	1	G
h	B	A		8				H
i	B	A	C	8			1	I
j	B		C				1	J
k	B		C			2		K
l	B					2	1	L
m	B		C		4			M
n	B				4		1	N
o	B				4	2		O
p	B		C		4	2	1	P
q	B		C	8				Q
r	B			8			1	R
s		A	C			2		S
t		A				2	1	T
u		A	C		4			U
v		A			4		1	V
w		A			4	2		W
x		A	C		4	2	1	X
y		A	C	8				Y
z		A		8			1	Z

THE CODES BELOW ARE NOT PRINTABLE								
FUNCTION CODES								MEANING
PN			C	8	4			Punch On
BY		A		8	4			Bypass
RES	B			8	4			Restore
PF	B	A	C	8	4			Punch Off
RS				8	4		1	Reader Stop
LF		A	C	8	4		1	Line Feed
NL	B		C	8	4		1	New Line (Carrier Return and Line Feed)
HT	B	A		8	4		1	Horizontal Tab
UC				8	4	2		Upper Case
EOB		A	C	8	4	2		End of Block
BS	B		C	8	4	2		Backspace
LC	B	A		8	4	2		Lower Case
*EOT			C	8	4	2	1	End of Transmission
PRE		A		8	4	2	1	Prefix
IL	B			8	4	2	1	Idle
DEL	B	A	C	8	4	2	1	Delete
Space			C					Space

Figure CA643-6. IBM 2741 Line Code Chart (PTTC/EBCD)

CA644 Start/Stop TTY

Start/Stop TTY Mod 33/35 line discipline is similar to 2741 line discipline in most respects. Refer to CA643.

35 TTY Char.	Hex
@	03
A	83
B	43
C	C3
D	23
E	A3
F	63
G	E3
H	13
I	93
J	53
K	D3
L	33
M	B3
N	73
O	F3
P	0B
Q	8B
R	4B
S	CB
T	2B
U	AB
V	6B
W	EB
X	1B
Y	9B
Z	5B
[	DB
\	3B
]	BB
↑	7B
←	FB
Space	05
!	85
"	45
#	C5
$	25
%	A5
&	65
'	E5
(	15
)	95
*	55
+	D5
,	35
–	B5
.	75
/	F5
0	0D
1	8D
2	4D
3	CD
4	2D

35 TTY Char.	Hex
5	AD
6	6D
7	ED
8	1D
9	9D
:	5D
;	DD
<	3D
=	BD
>	7D
?	FD
Null	01
SOM	81
EOA	41
EOM	C1
EOT	21
WRU	A1
Bell	E1
Hor Tab	91
Line Feed	51
Vert Tab	D1
Form	31
Return	B1
SO	71
S1	F1
DCo	09
X-On	89
Tape Aux-On	49
X-Off	C9
Tape Aux-Off	29
LEM	E9

Second Hex Digit ↓ / First Hex Digit →		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0							ACK									
0001	1	Null		EOT	Form	EOA	Line Feed		SO	SOM	HOR TAB	WRU	CR Return	EOM	Vert Tab	Bell	S1
0010	2																
0011	3	@	H	D	L	B	J	F	N	A	I	E	M	C	K	G	O
0100	4																
0101	5	SP	(	S	,	"	*	&	.	!	)	%	–	#	+	'	/
0110	6																
0111	7																
1000	8																
1001	9	DCo		Tape Aux Off		Tape Aux On				X-On				X-Off		LEM	
1010	A																
1011	B	P	X	T	\	R	Z	V	↑	Q	Y	U	]	S	[	W	←
1100	C																
1101	D	0	8	4	<	2	:	6	>	1	9	5	=	3	;	7	?
1110	E																
1111	F								Rub-out								Rub-out

0	1	2	3	4	5	6	7			S/360 Bit Positions
1	2	3	4	5	6	7	8			8-Bit Data Interchange Code
Start	1	2	3	4	5	6	7	8	Stop	Stop — Transmitted and Received Character

Line Control Characters

Char.	Hex	Meaning
WRU	A1	Who are you? WRU or Dial requests Identification (ID)
XON	89	Transmitter On
XOFF	C9	Transmitter Off
EOT	21	End of Transmission
DEL		Delete

Models 33 & 35 Teletypewriters Control-Character Sequences

EXAMPLE OF POINT-TO-POINT, DIAL UP (SWITCHED NETWORK)

Keyboard Unattended

		TTY	
Dial TTY	→		WRU Function
	←	ID, ACK	TTY Gives Identification Code and Go-Ahead Signal
Text	→		Message Sent
XOFF, WRU	→		Go-Ahead Signal to TTY
	←	ID, ACK	TTY Identification and Go-Ahead
Text	→		Message Sent
XOFF, EOT	→		Transmission is finished: go on-hook

Keyboard Attended

		TTY	
Dial TTY	→		WRU Function
	←	ID, ACK	Identification Code and Go-Ahead Signal
Text	→		Message Sent
XOFF	→		End of Text
CR LF DEL XOFF	} →		Go-Ahead TTY
	←	Text	Message Sent
	←	XOFF	End of Text
Text	→		Message Sent
XOFF, EOT	→		End of Text, End of Transmission

CA650 Test Equipment Setup

CA651 Modem Interface Test Set PN 453637

The modem interface test set (Figure CA651-1) is a tool that allows you physically to monitor the signals on the external EIA interface between the 8100 and an external modem. The modem monitor set is connected in series between the 8100 I/O panel and the external modem.

Model 921-S, which comes with independent switches, must have these switches always in the down or on position. You must ensure that all the switches are in the on position; otherwise, tests will fail. The 921-S is self-contained, battery-powered, and is transparent to the 8100 and external modem. The input impedance of each display is 33K ohms. All terminals on the patch board are easily accessible to allow probing with an external meter or oscilloscope.

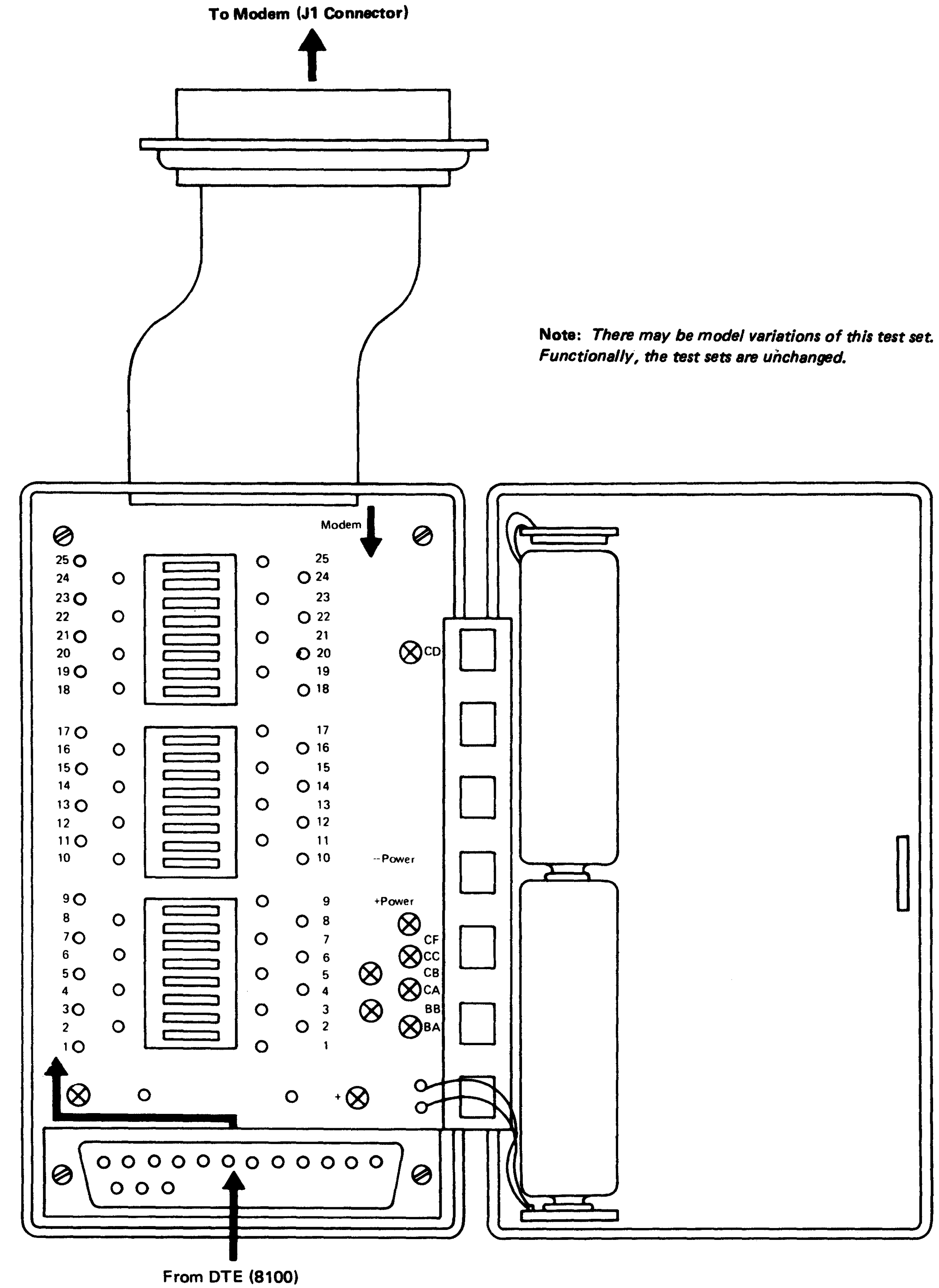
The permanently monitored leads are:

Pin No.	Indicator	Line Title
2	BA	Transmit Data
3	BB	Receive Data
4	CA	Request to Send
5	CB	Clear to Send
6	CC	Data Set Ready
8	CF	Carrier Detect
20	CD	Data Terminal Ready

An interface signal voltage greater than +3V turns on the LED display. Two independent monitor LEDs can also be patched to any interface terminal (either on the modem side or the terminal side.) One of these monitors turns on a positive voltage (+3V to +24V), pin 9. The other turns on a negative voltage (-3V to -24V), pin 10.

The modem interface test set is 4.5 in. (114.3 mm) x 2.5 in. (63.5 mm) x 1.6 in. (40.6 mm). The total weight with batteries (type AA) is 12 oz. (340.2 g).

CA652 Not Used



Note: *There may be model variations of this test set. Functionally, the test sets are unchanged.*

Manufacturer: Nu Data Corporation, 32 Fairview Avenue Little Silver, New Jersey 07739

Figure CA651-1. Modem Interface Test Set PN 453637

CA653 Loop Test Tool PN 1657410

The Loop Test Tool consists of two separate radial LSCs in utility boxes connected to each other by a length of indoor cable (Figure CA653-1). There are connectors on the LSC (relay 1, common, and relay 2) which allow monitoring of the relay pick voltages.

The LSCs are wired in such a way that a lobe is formed when the cable from the controller (for example: 8100 or 384X) is plugged into one of the LSCs; if a terminal is plugged into the other LSC, that terminal is on the lobe.

By monitoring the jacks of the Loop Test Tool, it can be determined if the connected equipment has activated the relays and if the proper sequence was followed. See Figure CA653-2 for relay states and Figure CA653-3 for relay timing.

You use the Loop Test Tool to:

- Isolate problems between IBM equipment (for example, terminals 8100, 384X) and the customer's loop.
- Test the operation of the 8100 or 384X if the customer loop is not available.
- Access the LSC relay voltages to check that the connected equipment can properly exercise the relays.

Use the following procedure to isolate a failure between the loop and the IBM equipment or to test the controller when the customer loop is not available. Plug the cable from the controller into one LSC and a terminal into the other. Run the tests and/or customer programs.

To test the relay pick circuits of the loop adapter:

1. Plug the 8100 loop cable of the lobe to be tested into point A or point B of the Loop Test Tool (See Figure CA653-1).
2. Invoke CA test routine 73 (refer to CA202).
3. Using a CE meter, monitor the relay connector points of the loop test tool LSC to which the controller is connected.
4. Compare the test results (by continuous monitoring) with the expected results in Figures CA653-2 and CA653-3.
   a. If the actual results equal expected results, then the relay pick circuits are correct.
   b. If the results are incorrect, a failure may be suspected in IBM hardware-loop adapter or cabling.

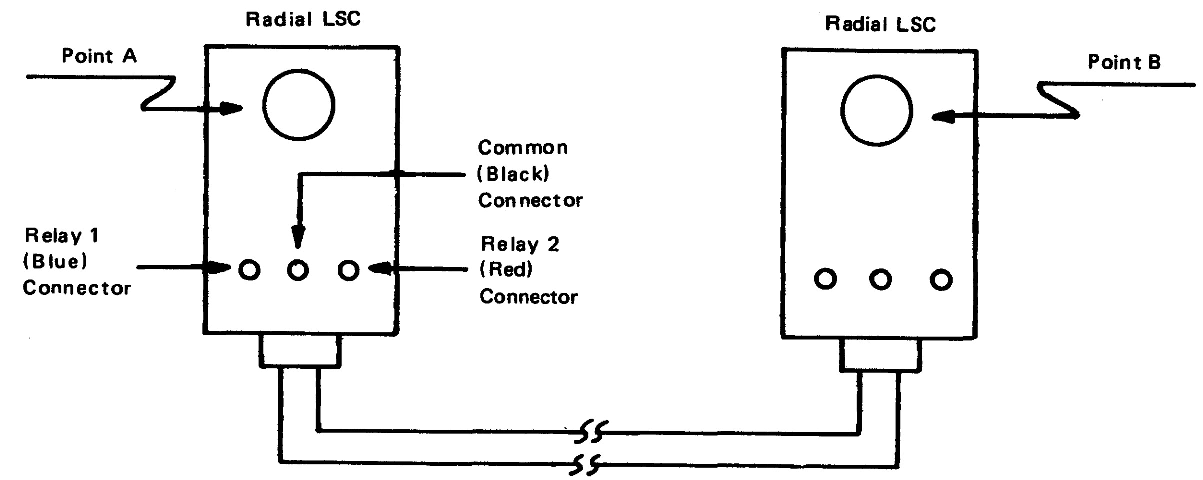


Figure CA653-1. Loop Test Tool PN 1657410

Step No.	Control Lines			Relay States			
				Lobe 1		Lobe 2	
	LTST	DRS	NS	R1	R2	R1	R2
1	A	I	A	Off	Off	On	Off
2	A	A	I	On	Off	Off	Off
3	I	A	A	On	On	On	On

Legend: Min. Max.

A (Active) = 0 to +0.6V

I (Inactive) = +2.4 to +5.5V

On = +3.8 to +6.0V

Off = 0 to +0.6V

The DTR must be active (0 to +0.6V) for the relays to function normally. Each step lasts approximately 10 seconds. See Figures CA550-1 (One-Lobe) and CA550-2 (Two-Lobe) for control line locations and LSC connector layout.

Figure CA653-2. Relay States

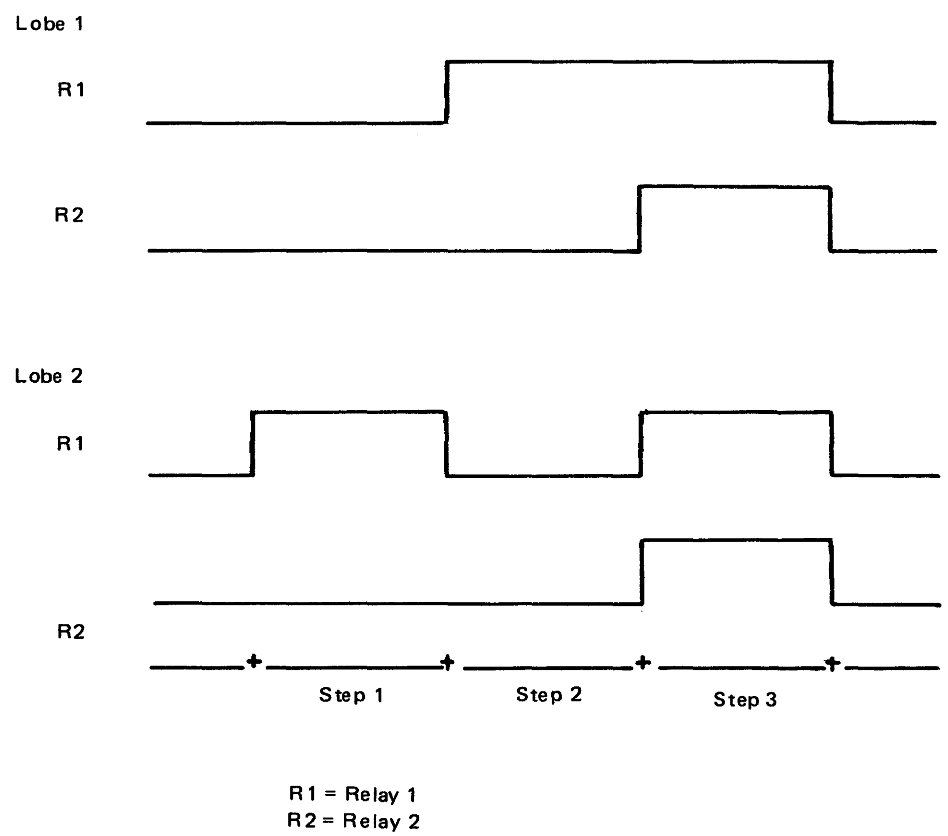


Figure CA653-3. Relay Timing

CA700 World Trade Information

CA701 Line Plate DC Current Adjustment

DC current in the telephone line must be adjusted to a value between 20 and 70 ma. Adjustment is by strappable resistors. The line current should be adjusted (if required) when the line plate is installed.

Measure (+3V dc) between the following test points:

Positive lead to TP1 (diode lead).

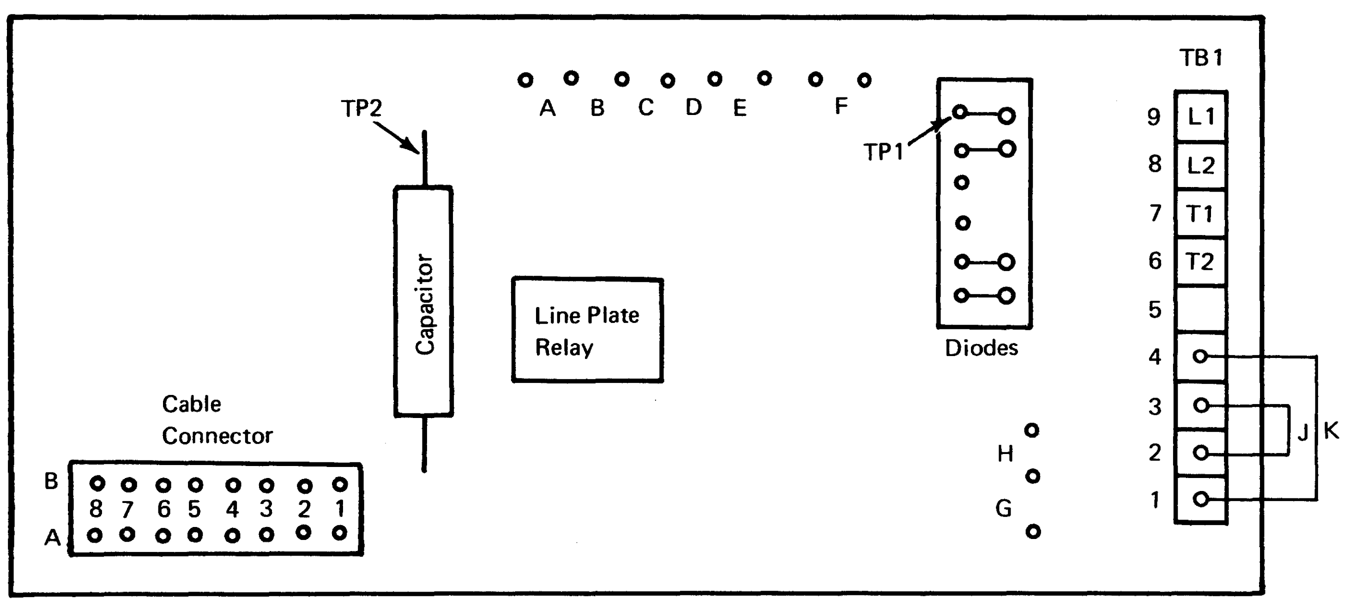
Negative lead to TP2 (capacitor lead).

Enable the modem (pick line plate relay). Move strap from A through F to obtain a reading of 0.5V dc to 1.7V dc.

To adjust transmit level, connect a DB meter to TB1-8 and TB1-9. Use Transmit Level Adjustment procedure (see CA711).

Note: *Line plate has an insertion loss of about 1 db. This must be considered when adjusting modem transmit level using Alternate Procedure.*

LINE PLATE (01 M)



Jumpers:

A	810 Ω	D	480 Ω	G	Handset
B	660 Ω	E	150 Ω	H	No Handset
C	330 Ω	F	0 Ω	J, K	Countries other than Japan

CA711 Transmit Level Adjustment

The transmit level for switched network operations when using an integrated modem should be adjusted to comply with the local PTT regulations. Contact the TP coordinator for current regulations.

In WTC, the integrated modem uses rocker switches mounted on the card for transmit level adjustment. These switches provde 18 dBm attenuation (maximum) in 1 db steps. The integrated modem is factory set for -0.5 ± 0.5 dBm output with all adjustable switches in off (0) position.

CA712 Cable Card and Cable to Line Plate

A2B3

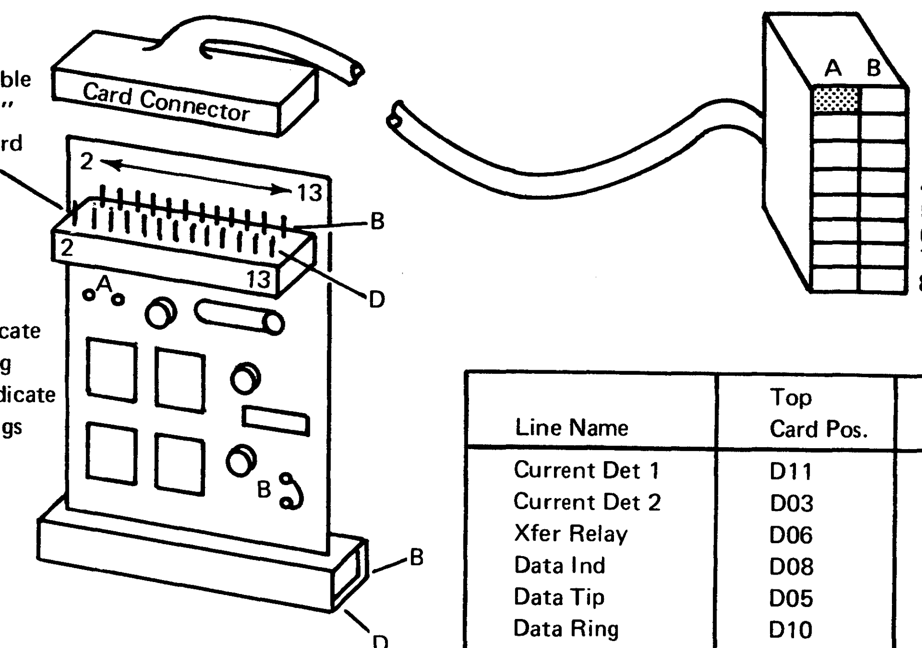
Wire edge of cable connects to "D" row of cable card

Jumpers:

A - in - ring indicate after one ring

A - out - ring indicate after two rings

B mandatory



Line Name	Top Card Pos.	Housing Pos.
Current Det 1	D11	B01
Current Det 2	D03	A02
Xfer Relay	D06	B05
Data Ind	D08	A04
Data Tip	D05	A08
Data Ring	D10	A06
+12V	D04	B03
Sig Gnd	D07	B07

CA715 Manual Answer Operation

Test	Condition	Line Test Point(s)	Signal (See Note 1)	If signal is NOT correct:
1	Handset lifted	A2D2B12/D12	One line ON. One line OFF.	• Exchange line plate with a new line plate.
2	Handset hung up	A2D2B12/D12	Both lines OFF	• Verify line plate jumpers Ref. CA701, Line Plate diagram.
3	Handset lifted	A2D2B09	ON	• Exchange card A2D2 with a new card. • Verify card jumpers Ref. CA712.
4	Handset hung up	A2D2B09	OFF	
5	Jumper A2F5D12 to ground.	A2D2B09	ON	
6	Remove jumper from A2F5D12	A2D2B09	OFF	
7	Handset hung up. Ask for a telephone call.	A2D2D11	ON after one or two rings.	
		A2D2B13	ON after one or two rings.	• Exchange card A2B3 with a new card. • Verify card jumpers Ref. CA712.
8	Jumper A2F5D12 to ground.	A2D2B07	ON (See Note 2).	• Exchange card A2D2 with a new card. • Verify card jumpers Ref. CA712.

Note 1: *Signal ON = +0V dc to +0.7V dc*
Signal OFF = +2.4V dc to +12V dc

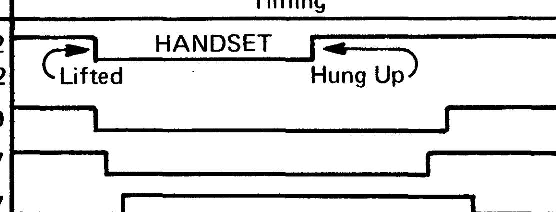
Note 2: *Signal ON = 0.7V dc*
Signal OFF = 0V dc to .3V dc

Manual Answer Operating Sequence (WT-PSN)

1. On hearing the ring pulses at the telephone, the handset is lifted. Lifting the handset starts dc current to flow through the current detect circuit, which turns on the Data Set Ready (DSR) level to the adapter.
2. When enabled, the adapter responds with Connect Data Set to Line (CDSTL), which turns on the Transfer Relay to the Line Plate. The Transfer Relay then connects the Telephone Line to the Line Transformer.

Timing Chart

Line Name	Test Point	Timing	Signal ON	Signal OFF
CD1 or CD2	A2D2E12 A2D2D12	HANDSET Lifted Hung Up	0 to +.7V dc 0 to +.7V dc	+2.4 to +12V dc +2.4 to +12V dc
DSR	A2D2B09		0 to +.4V dc	+2.4 to +12V dc
CDSTL	A2D2B07		0 to +.4V dc	+2.4 to +12V dc
Transfer Relay	A2D2B07		+.7V dc	0V dc



CA716 Auto Answer Operation

Test	Condition	Line Test Point	Signal (See Note 1)	If signal is NOT correct:
1	Signal on during ring pulses (after first ring).	A2D2D12 or A2D2B12	ON	• Exchange Line Plate (01M). • Verify line plate jumpers; Ref. CA701. • End repair action
2	Signal on after first ring pulse.	A2D2B09	ON	• Exchange card A2D2 (PSN) • Verify card jumpers; Ref. CA712. • End repair action
3	Signal on after first ring pulse.	A2D2D11	ON	
4	Signal on after first or second ring pulse.	A2D2B13	ON	• Exchange card A2B3 (cable) • Verify card jumpers; Ref. CA712. • End repair action
5	Signal on after first or second ring pulse.	A2D2D07	ON	• Exchange card A2D2 (PSN) • Verify card jumpers; Ref. CA712. • End repair action
6	CANCEL incoming telephone call. Jumper A2E5D12 to ground.	A2D2B07	ON See Note 2	
7	Disconnect the jumper.	A2D2B07	OFF See Note 2	
8	Jumper A2F5D12 to ground.	Visual Inspection	Line relay PICKED	• Exchange Line Plate (01M). • Verify line plate jumpers; Ref. CA701. • End repair action
	Disconnect the jumper.	Visual Inspection	Line relay NOT picked	
9	NO incoming ring signal.	Same Test Points as Tests 1 through 5	OFF	Same as Tests 1 through 5.

Note 1: *Signal ON = +0.0V dc to +00.7V dc*
Signal OFF = +2.4V dc to +12.0V dc

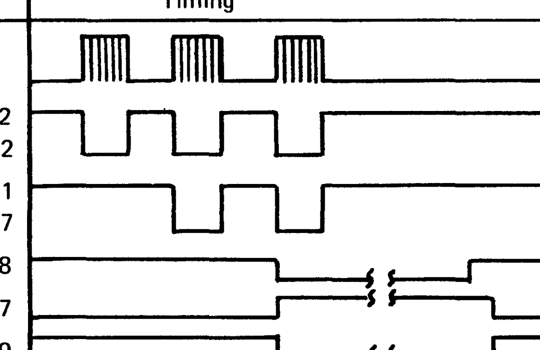
Note 2: *Signal ON = +.7V dc*
Signal OFF = 0 to +.3V dc

Auto Answer Operating Sequence (WT-PSN)

1. Ring Indicate is turned on either with the first incoming ring pulses (Ring Gate Circuit not installed), or with the second or third incoming ring pulses. Frequency of Ring Indicate (RI) is the same as incoming ring pulses.
2. The adapter responds to RI with Connect Data Set to Line (CDSTL), which picks the Line Plate Relay to connect the telephone line to the line transformer.
3. Transfer Relay from the PSN card turns on Data Set Ready (DSR) to the adapter.
4. The adapter then turns on Request to Send (RTS) to the modem. When Ready for Sending is received, it clamps Transmit Data for a 3.5-second (2100Hz) Answer Tone.

Timing Chart

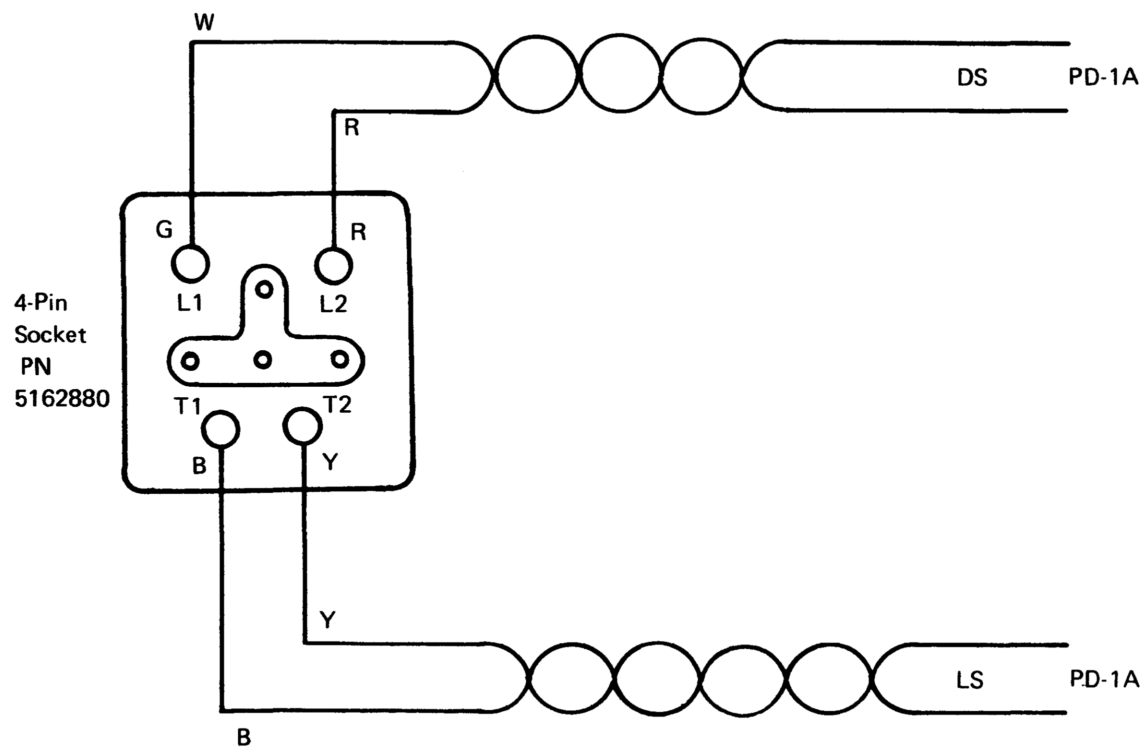
Line Name	Test Point	Timing	Signal ON	Signal OFF
Ring Pulses on Telephone Line	M-TB1-8 M-TB1-9		+20 to +70V ac	0V
CD1 or CD2	A2D2B12 A2D2D12		0 to +.7V dc	+2.4 to +12V dc
RI	A2D2D11 A2D2D07		0 to +.4V dc	+2.4 to +12V dc
CDSTL	A2D2B08		0 to +.4V dc	+2.4 to +12V dc
Transfer Relay	A2D2B07		+.7V dc	0V
DSR	A2D2B09		0 to +.4V dc	+2.4 to +12V dc



CA717 Public Switched Network — Japan

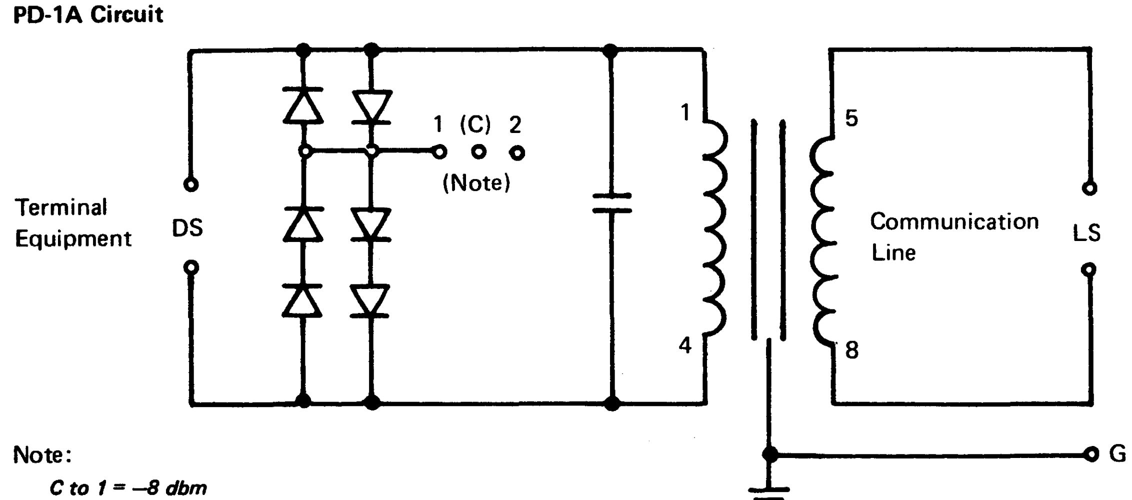
Attachment to the switched network is by two (4-wire) cable assemblies with quick disconnect capability.

PD-1A cable assembly PN 5182523 is provided to the customer for customer installation at a location within 30 cm (12 in.) of NTT-provided PD-1A. The NTT will connect the cable to the PD-1A.



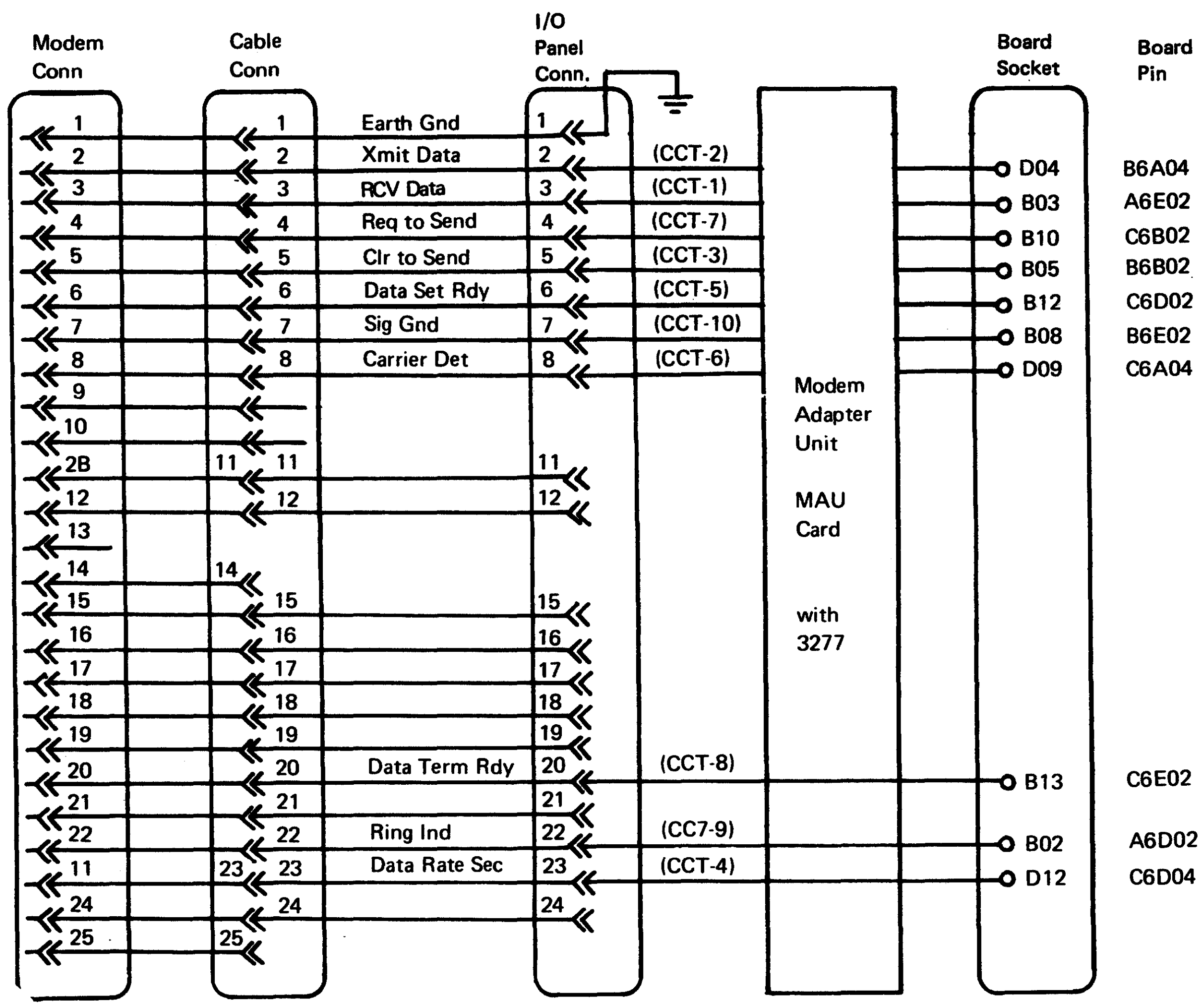
G and R connections to PD-1A terminals DS
B and Y connections to PD-1A terminals LS

PD-1A Circuit

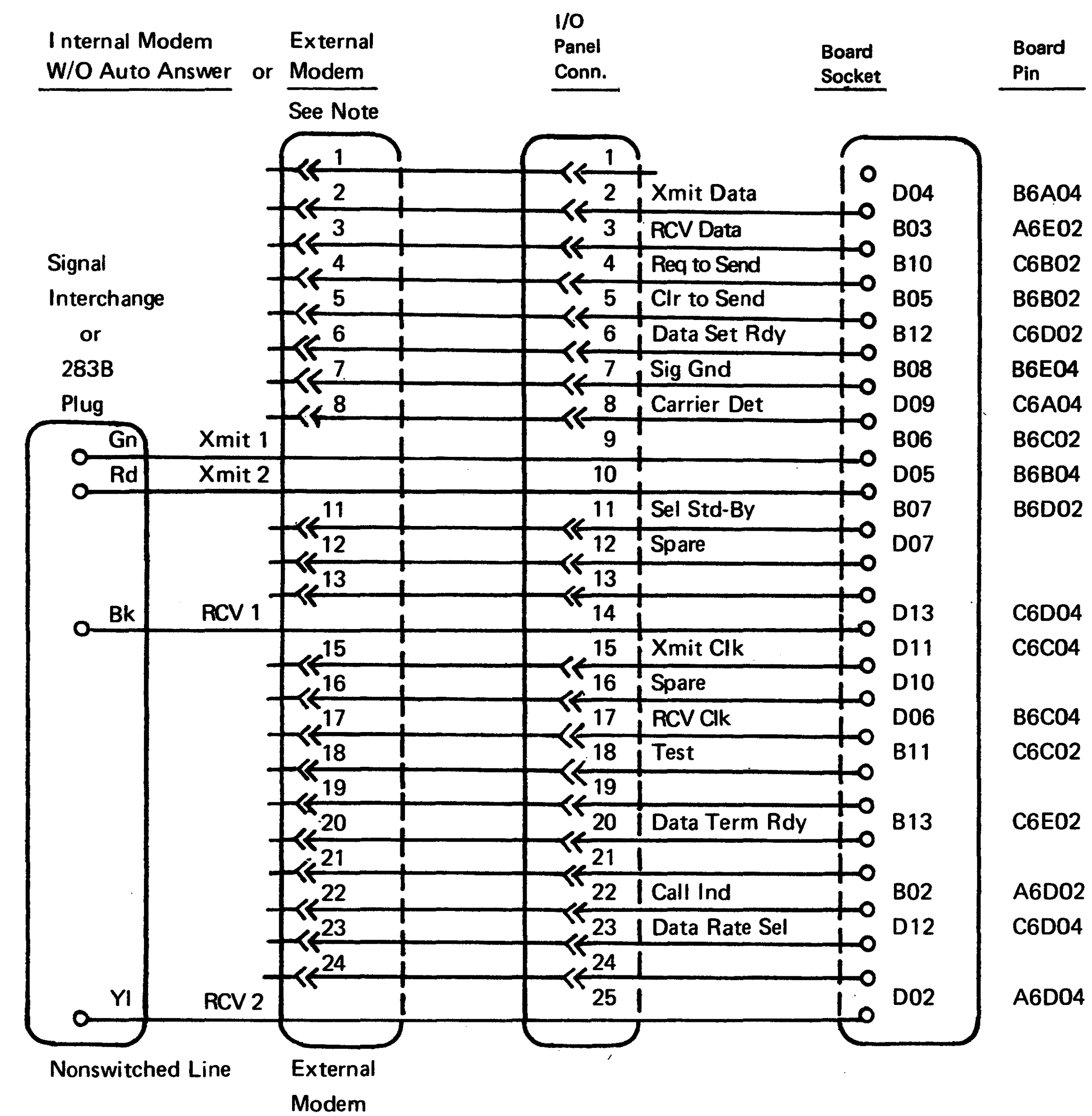


Note:
C to 1 = –8 dbm
C to 2 = 0 dbm

CA719 United Kingdom, External Modem Cables

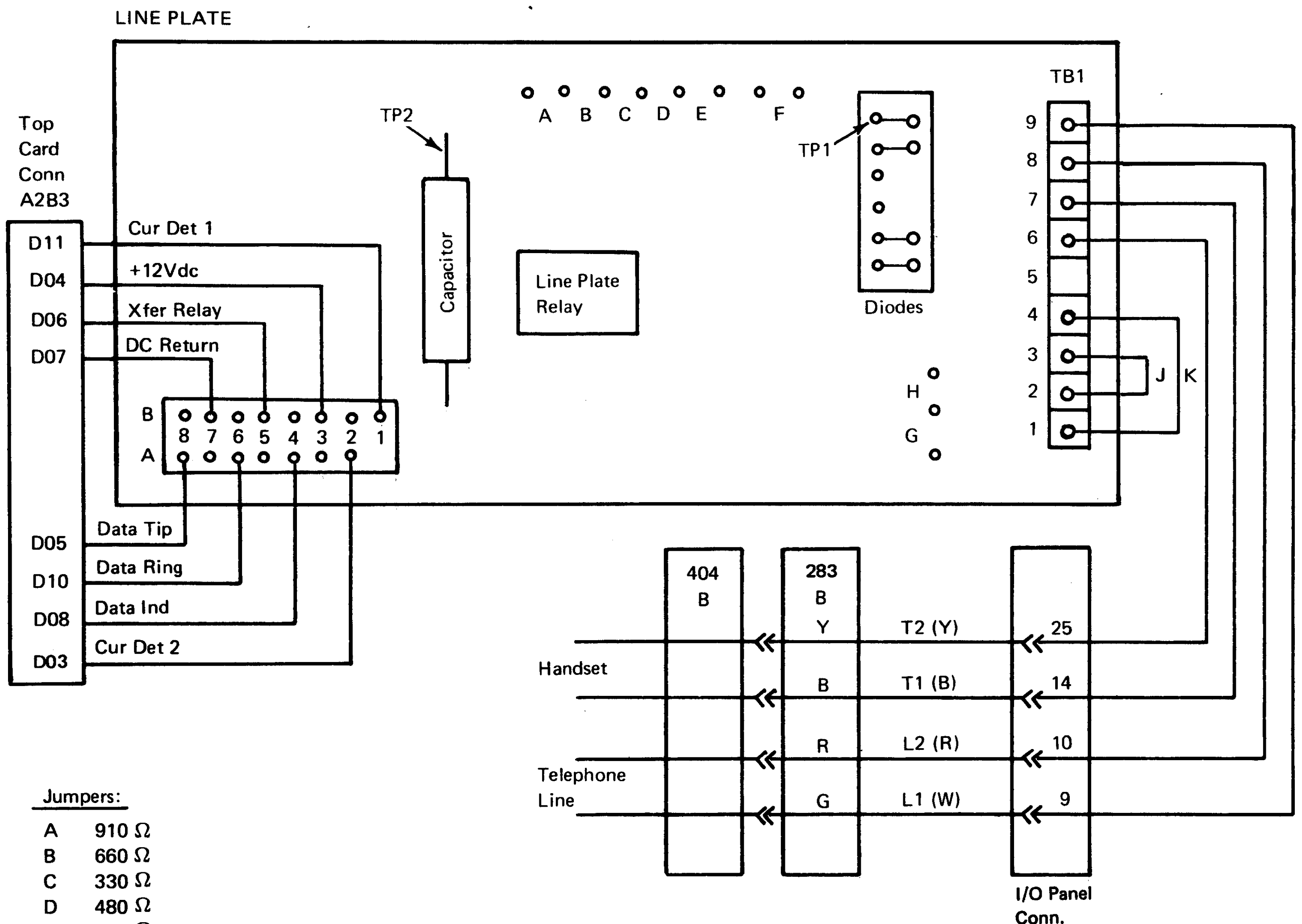


CA720 U.S. and World Trade (Not UK, France, Italy) Modem Cables



Note: West Germany has a short cable (11, 12, 16, 18, 19 wires deleted) connecting modem and cable from 8100 for D1200's modem attachment. See your TP coordinator for current requirements.

CA721 World Trade Switched Line (Except Japan)

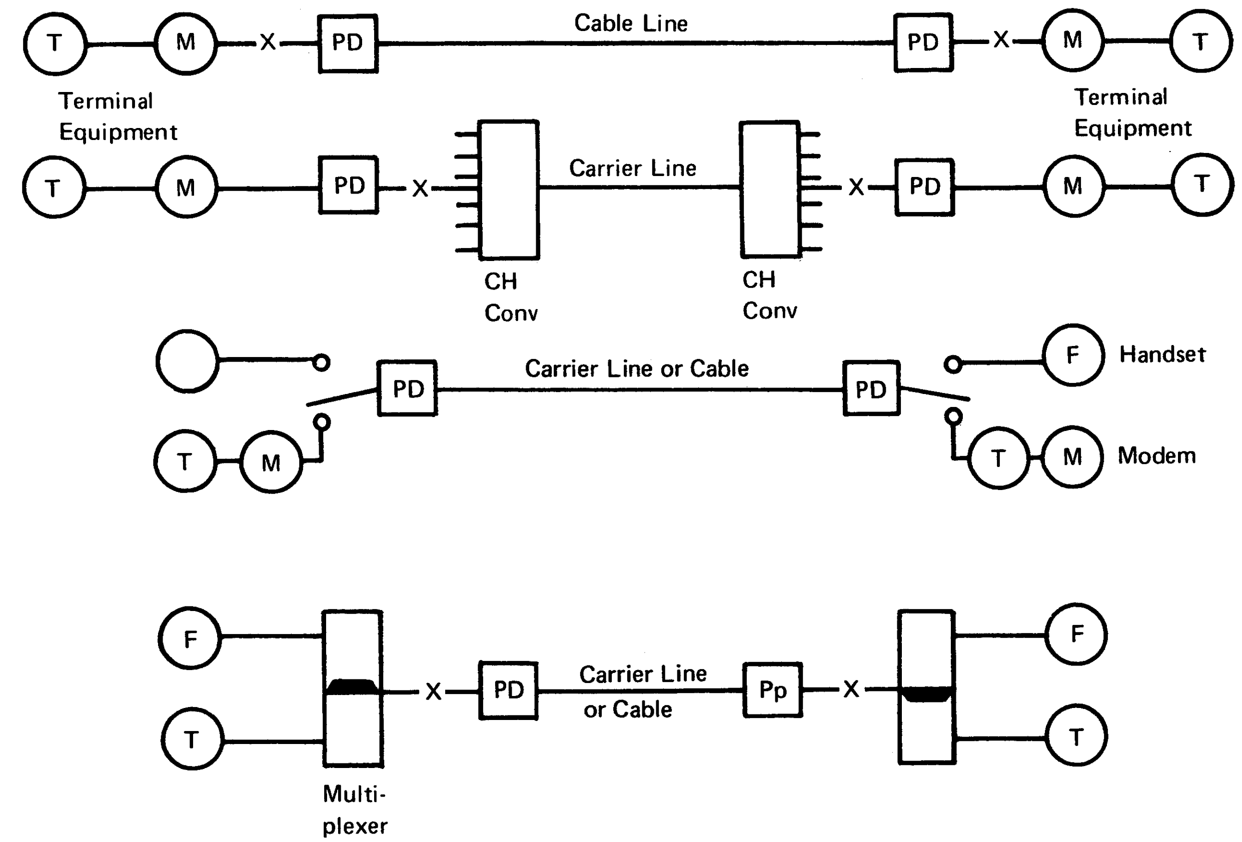


Jumpers:

A	910 Ω
B	660 Ω
C	330 Ω
D	480 Ω
E	150 Ω
F	0 Ω
G	Telephone Handset
H	No Telephone Handset
J } K	All World Trade except Japan.

G or H MUST be plugged.

CA722 Switched Line Configuration (Japan)

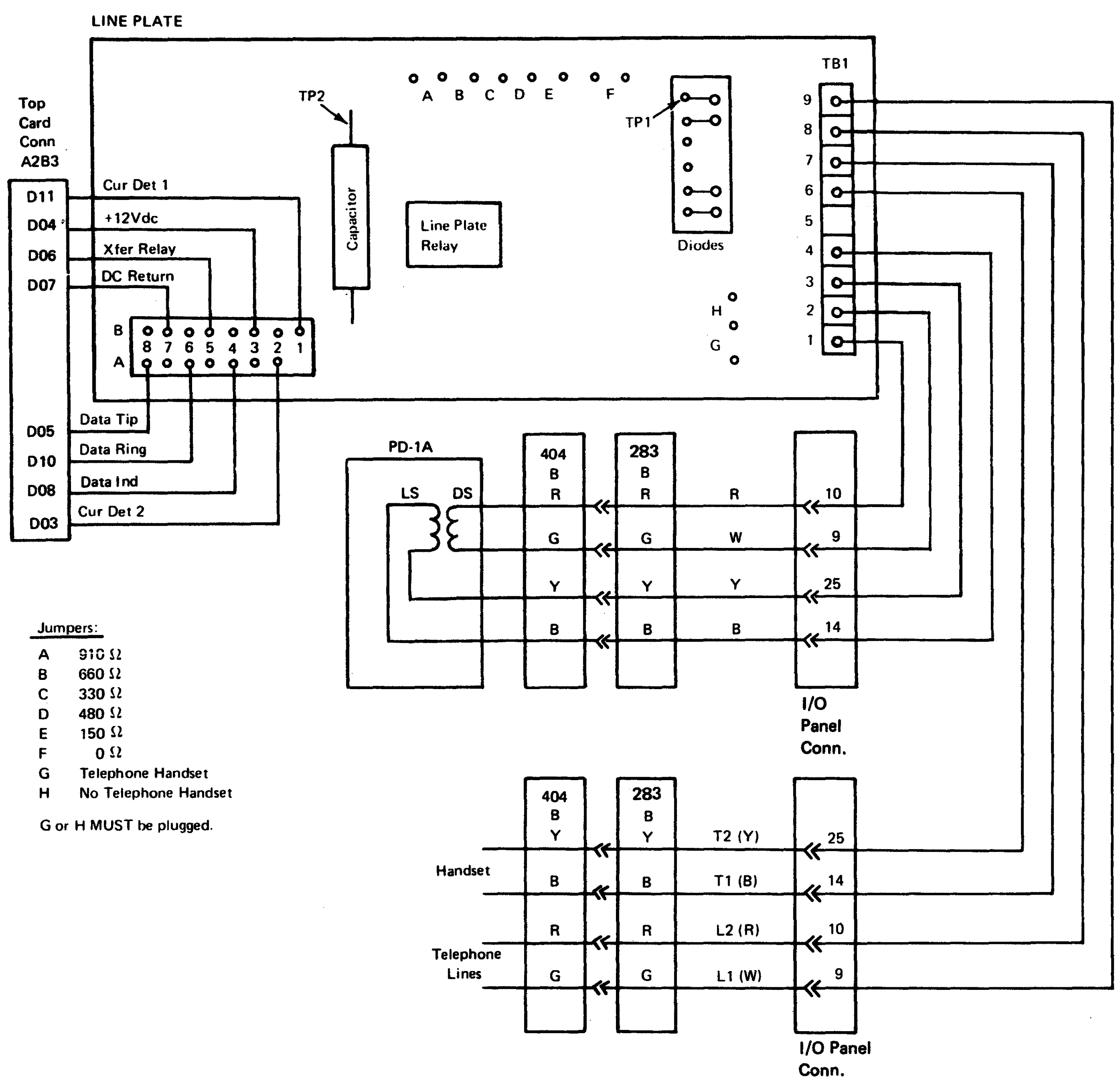


X = Maintenance Demarcation Line
PD installed between Modem & Line.

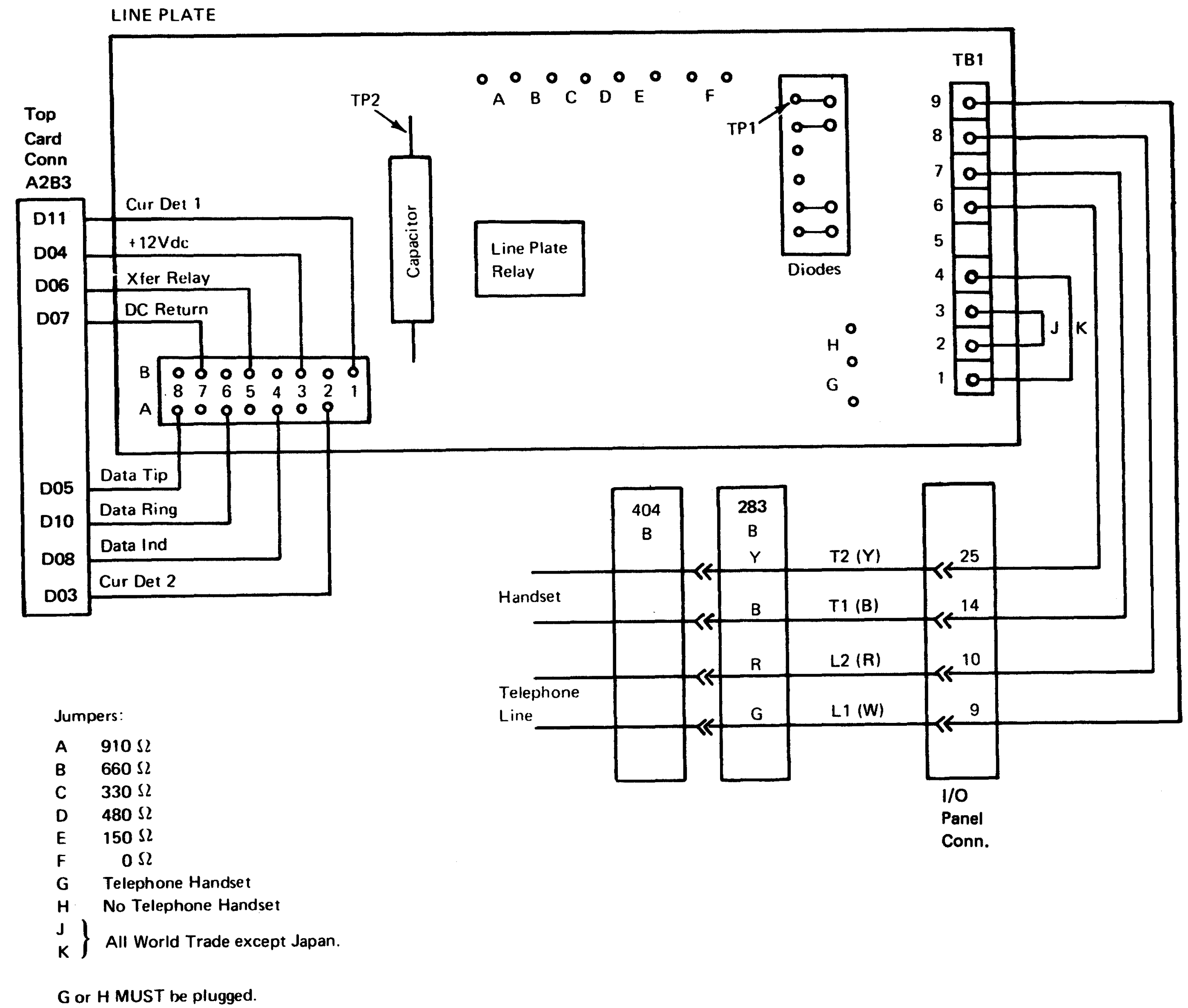
Requirements:

- PD must have quick disconnect (no tools required)
  - 4 pin socket PN 5162880
  - Cable terminated in a 283B type plug (PN 341200)
    - Transmit pair connected to R (red) GN (Green)
    - Receive pair connected to BK (Black) & Y (Yellow)
  - Wire (GN) & (R) to PD-1A terminals marked "DS" (Terminal equipment send) 2 & 4 wire
  - Wire (BK) & (Y) to PD-1A terminals marked "DR" (Terminal equipment Recv) 4 wire
- Self test must exercise DCE – Integrated modem wrap card required.
  – External modems, wrap cable with test Sw.
- NTT local test requires 4 pin loop back plug (PN 1864271) and 4 pin shorting plug (PN 1864272) must be supplied by terminal equipment.

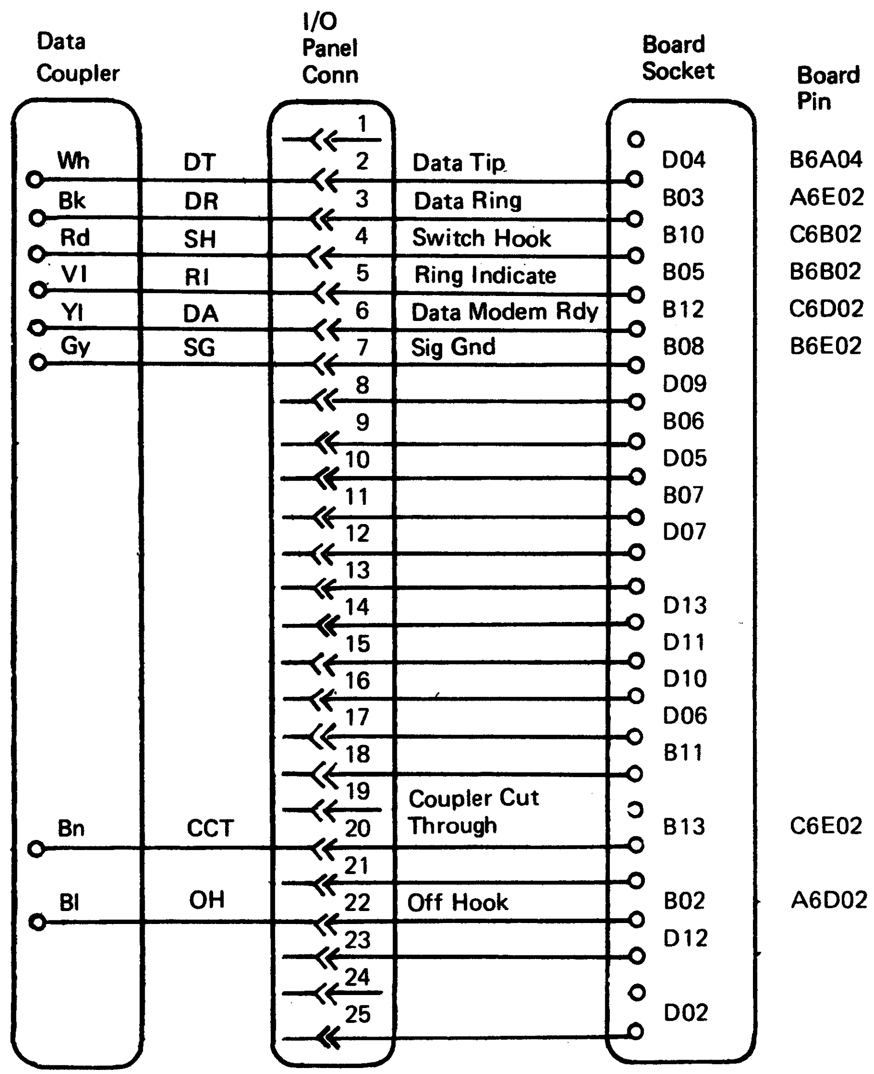
CA723 Japan Switched Line



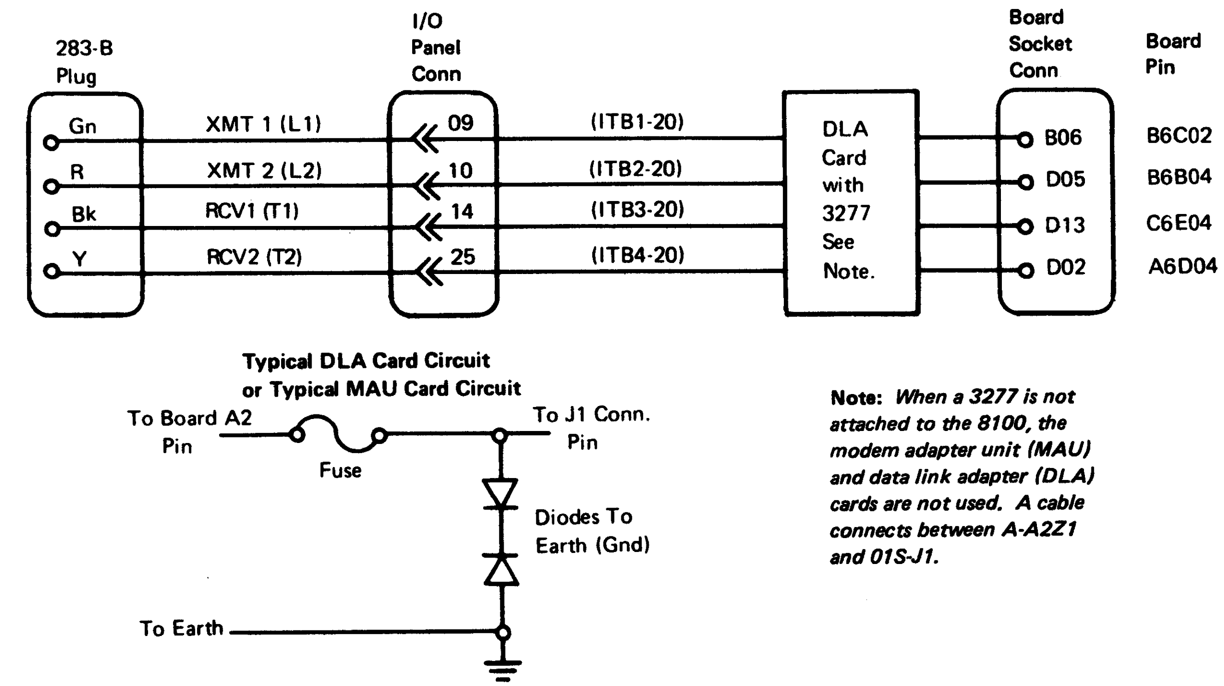
CA724 France and Italy Switched Line



CA725 U.S. and Canada Switched Line



CA726 United Kingdom – Nonswitched Line



Note: *When a 3277 is not attached to the 8100, the modem adapter unit (MAU) and data link adapter (DLA) cards are not used. A cable connects between A-A2Z1 and 01S-J1.*

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CA800 Communications Specify Code (Minor) Changes

Specify Codes (Minor) are a subset of the 8100 Communications FAC Specify Codes. You can modify or change these Specify Codes (Minor) at customer request and without formal Engineering instructions. There are two change categories:

- Speed – Speed changes that require board wiring or card jumper changes.
- Line Type – Communications line changes (2- or 4-wire) that require board wiring or card jumper changes.

Any other changes requested by the customer are not classified as Specify Code (Minor) changes; the customer should refer requests for other changes to his Sales Representative.

Use Service Code 21 to record time spent making Specify Code (Minor) changes; this time is billable to the customer.

Figure CA800-1 shows the procedure for making Specify Code (Minor) changes.

Figure CA800-2, using 8130 Start/Stop communication FAC code 60 as on example, explains communications FAC code table entries that are contained in Figure CA800-4 through CA800-12.

Figure CA800-3 lists the features required by the communications FAC codes.

Figures CA800-4, -5, and -6 show board wiring and card jumpers for 8130 communications FAC Specify Codes (Minor) for SDLC, BSC, and S/S, respectively.

Figures CA800-7, -8, and -9 show board wiring and card jumpers for 8140 communications FAC Specify Codes (Minor) for SDLC, BSC, and S/S, respectively.

Figures CA800-10, -11, and -12 show board wiring and card jumpers for 8101 communications FAC Specify Codes (Minor) for SDLC, BSC, and S/S, respectively.

Procedure Flow		Action/Reference
Customer Contact	Customer provides:	1. Feature identification (physical address, FAC). 2. Minor Code changes.
Pretest (Note)	CE performs CA tests via MAP.	1. Use MD. 2. Use MD diskette 2, Menu Selection A, offline.
Determine Communications Feature Location	CE locates CA feature board/card socket location; Identify FAC/Specify Code.	1. Use 8100 model number. 2. Use Configuration Data Sheet 3. Use physical address (PA). 4. Use board layout (CA52X).
Inspect Current Minor Code	CE checks for current Minor Code board wiring and card jumpers. Identify and verify Minor Code.	1. Use FAC/Specify Code. 2. Use Figures CA800-4 through CA800-12. 3. Use board layout, CA52X. 4. Use card jumpers, CA563.
Review New Minor Code Changes	CE reviews new Minor Code changes; verify valid change.*	1. Use FAC/Specify Code. 2. Customer-requested changes. 3. Use Figures CA800-4 through CA800-12.
Remove Old Minor Code Wires/Jumpers	CE removes old Minor Code wires/jumpers.	1. Use Figures CA800-4 through CA800-12. 2. Use board layout, CA52X. 3. Use card jumpers, CA563.
Add New Minor Code Wires/Jumpers	CE adds new Minor Code wires/jumpers.	1. Use Figures CA800-4 through CA800-12. 2. Use board layout, CA52X. 3. Use card jumpers, CA563.
Verify, Update, and Retest	CE verifies new Minor Code wires/jumpers, updates Configuration Table, **and retest CA feature.**	1. Use Figures CA800-4 through CA800-12. 2. Use board layout, CA52X. 3. Use card jumpers, CA563. 4. Update the Configuration Table as necessary to reflect changes made. See CA113, Configuration Table Data, and Chapter 2, CP300. 5. Use MD. 6. Use MD diskette 2, Menu Selection A, offline.

*If new Minor Code is not valid, contact your Local Branch Office DP Sales Representative for assistance.

Note: *The communications feature must test out satisfactorily before any changes are installed. Basic tests including selectable if applicable must be run on the communications future.*

Figure CA800-1. Procedure for Making Specify Code (Minor) Changes

Facility for Attaching Communications No. 60 (8130 Start/Stop; see Figure CA800-6)

Feature 1603 = BSC/SS Communications Adapter
Feature 3701 = EIA card

	Required Features (Ref Fig. CA800-3)	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Board Wiring Ref CA520	Card Jumpers Ref CA563
FAC 60	1603 3701	9601	9602	9603	9604	9605	9606	CA2 Socket	NA
110 bps		9701	9702	9703	9704	9705	9706	P05-D08	
134.5 bps		9711	9712	9713	9714	9715	9716	M02-D08	
150 bps		9721	9722	9723	9724	9725	9726	P02-D08	
300 bps		9731	9732	9733	9734	9735	9736	G13-D08	
600 bps		9741	9742	9743	9744	9745	9746	M04-D08	

Specify Code (Minor) for Port 2, Speed - 110 bps.

Specify Code (Major) for Port 2.

Board wire required at CA2 board socket from P05 to D08.

No card jumper required for FAC 60, 100 bps.

Figure CA800-2. Explanation of Communications FAC Code Table Entries; Example is for 8130 Start/Stop

Feature Code	Description
1550	CCITT V.35 (CA6) card
1601	SDLC Communication Adapter with Clock (CA1) card
1602	SDLC Communication Adapter without Clock (CA1) card
1603	BSC/S-S Communication Adapter with Clock (CA2) card
1604	BSC/S-S Communication Adapter without Clock (CA2) card
3701	EIA RS-232-C/CCITT V.24/V.28 (CA50) card
4830	Loop (CA3) card
4835	Loop Second-Lobe (CA4) card
5200	Multispeed Clock (CA10) card
5500	Integrated Modem — Nonswitched (CA8) card
5501	Integrated Modem — Switched (CA9) card
5655	X.21 Nonswitched (CA11) Card
5660	Digital Data Service (CA7) card

Figure CA800-3. Features Required by the Communications FAC Codes

	Required Features	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Board Wiring Ref CA520	Card Jumper Ref CA563
FAC 8	1602 4830	9081	9082	9083	9084	9085	9086	NA	NA
FAC 9	1602 4830 4835	NA	NA	NA	9094	9095	9096	NA	NA
FAC 10	1602 4830	9101	9102	9103	9104	9105	9106	NA	NA
FAC 11	1602 4830 4835	NA	NA	NA	9114	9115	9116	NA	NA
FAC 12	1601 3701	9121	9122	9123	9124	9125	9126	CA1 Socket	NA
600 bps		9741	9742	9743	9744	9745	9746	M04 to D08	
1200 bps		9751	9752	9753	9754	9755	9756	M05 to D08	
FAC 13	1602 3701	9131	9132	9133	9134	9135	9136	NA	NA
FAC 15	1601 3701	9151	9152	9153	9154	9155	9156	CA1 Socket	NA
600 bps		9741	9742	9743	9744	9745	9746	M04 to D08	
1200 bps		9751	9752	9753	9754	9755	9756	M05 to D08	
2400 bps		9761	9762	9763	9764	9765	9766	M03 to D08	
FAC 16	1602 3701 5200*	NA	NA	9163	9164	9165	9166	NA	CA10 Card
4800 bps		NA	NA	9773	9774	9775	9776		B
9600 bps		NA	NA	9783	9784	9785	9786		C
FAC 17	1602 3701	9171	9172	9173	9174	9175	9176	NA	NA
FAC 18	1601 5500	9181	9182	9183	9184	9185	9186	CA1 Socket	CA8 Card**
600 bps/2 wire		9851	9852	9853	9854	9855	9856	M04 to D08	J = on, K = off
600 bps/4 wire		9741	9742	9743	9744	9745	9746	M04 to D08	J = off, K = on
1200 bps/2 wire		9861	9862	9863	9864	9865	9866	M05 to D08	J = on, K = off
1200 bps/4 wire		9751	9752	9753	9754	9755	9756	M05 to D08	J = off, K = on
FAC 19	1601 5501	9191	9192	9193	9194	9195	9196	CA1 Socket	NA
600 bps		9741	9742	9743	9744	9745	9746	M04 to D08	
1200 bps		9751	9752	9753	9754	9755	9756	M05 to D08	
FAC 20	1602 5660	9201	9202	9203	9204	9205	9206	NA	CA7 Card
2400 bps		9761	9762	9763	9764	9765	9766		A
4800 bps		9771	9772	9773	9774	9775	9776		B
9600 bps		9781	9782	9783	9784	9785	9786		C
FAC 24	1601 1550	9241	9242	9243	9244	9245	9246	CA1 Socket	NA
600 bps		9741	9742	9743	9744	9745	9746	M04 to D08	
1200 bps		9751	9752	9753	9754	9755	9756	M05 to D08	
2400 bps		9761	9762	9763	9764	9765	9766	M03 to D08	
FAC 25	1602 1550 5200*	NA	NA	9253	9254	9255	9256	NA	CA10 Card
4800 bps		NA	NA	9773	9774	9775	9776		B
9600 bps		NA	NA	9783	9784	9785	9786		C
FAC 27	1602 1550	9271	9272	9273	9274	9275	9276	NA	NA
FAC 30	1602 5655	9301	9302	9303	9304	9305	9306		
2400 bps		9761	9762	9763	9764	9765	9766	NA	NA
4800 bps		9771	9772	9773	9774	9775	9776		
9600 bps		9781	9782	9783	9784	9785	9786		

*Only one 5200 feature is required per 8130.
**Two-wire operation requires board jumpers (CA8 Socket): G02 to G09 and J05 to J13.

Figure CA800-4. Board Wiring and Card Jumpers for 8130 SDLC Communications FAC Specify Codes (Minor)

	Required Features	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Board Wiring Ref CA520	Card Jumpers Ref CA563
FAC 40 600 bps 1200 bps	1603 3701	9401 9741 9751	9402 9742 9752	9403 9743 9753	9404 9744 9754	9405 9745 9755	9406 9746 9756	CA2 Socket M04 to D08 M05 to D08	NA
FAC 41	1604 3701	9411	9412	9413	9414	9415	9416	NA	NA
FAC 43 600 bps 1200 bps	1603 3701	9431 9741 9751	9432 9742 9752	9433 9743 9753	9434 9744 9754	9435 9745 9755	9436 9746 9756	CA2 Socket M04 to D08 M05 to D08	NA
FAC 44 2400 bps 4800 bps 9600 bps	1604 3701 5200*	NA 9761 NA NA	NA 9762 NA NA	9443 9763 9773 9783	9444 9764 9774 9784	9445 9765 9775 9785	9446 9766 9776 9786	NA	CA10 Card A B C
FAC 45 600 bps/2 wire 600 bps/4 wire 1200 bps/2 wire 1200 bps/4 wire	1603 5500	9451 9851 9741 9861 9751	9452 9852 9742 9862 9752	9453 9853 9743 9863 9753	9454 9854 9744 9864 9754	9455 9855 9745 9865 9755	9456 9856 9746 9866 9756	CA2 Socket M04 to D08 M04 to D08 M05 to D08 M05 to D08	CA8 Card** J = on, K = off J = off, K = on J = on, K = off J = off, K = on
FAC 47 2400 bps 4800 bps 9600 bps	1604 5660	9471 9011 9031 9051	9472 9012 9032 9052	9473 9013 9033 9053	9474 9014 9034 9054	9475 9015 9035 9055	9476 9016 9036 9056	NA	CA7 Card A B C

*Only one 5200 feature is required per 8130.
**Two-wire operation requires board jumpers (CA8 Socket): G02 to G09 and J05 to J13.

Figure CA800-5. Board Wiring and Card Jumpers for 8130 BSC Communications FAC Specify Codes (Minor)

	Required Features	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Board Wiring Ref CA520
FAC 60 110 bps 134.5 bps 150 bps 300 bps 600 bps	1603 3701	9601 9701 9711 9721 9731 9741	9602 9702 9712 9722 9732 9742	9603 9703 9713 9723 9733 9743	9604 9704 9714 9724 9734 9744	9605 9705 9715 9725 9735 9745	9606 9706 9716 9726 9736 9746	CA2 Socket P05 to D08 M02 to D08 P02 to D08 G13 to D08 M04 to D08
FAC 61 110 bps 134.5 bps 150 bps 300 bps 600 bps	1603 3701	9611 9701 9711 9721 9731 9741	9612 9702 9712 9722 9732 9742	9613 9703 9713 9723 9733 9743	9614 9704 9714 9724 9734 9744	9615 9705 9715 9725 9735 9745	9616 9706 9716 9726 9736 9746	CA2 Socket P05 to D08 M02 to D08 P02 to D08 G13 to D08 M04 to D08

Figure CA800-6. Board Wiring for 8130 S/S Communications FAC Specify Codes (Minor)

	Required Features	Port 1	Port 2	Port 3	Board Wiring Ref CA520	Card Jumpers Ref CA563
FAC 8	1602 4830	9081	9082	9083	NA	NA
FAC 9	1602 4830 4835	9091	9092	NA	NA	NA
FAC 10	1602 4830	9101	9102	9103	NA	NA
FAC 11	1602 4830 4835	9111	9112	NA	NA	NA
FAC 12 600 bps 1200 bps	1601 3701	9121 9741 9751	9122 9742 9752	9123 9743 9753	M04 to D08 Socket M04 to D08 M05 to D08	NA
FAC 13	1602 3701	9131	9132	9133	NA	NA
FAC 15 600 bps 1200 bps 2400 bps	1601 3701	9151 9741 9751 9761	9152 9742 9752 9762	9153 9743 9753 9763	CA1 Socket M04 to D08 M05 to D08 M03 to D08	NA
FAC 16 4800 bps 9600 bps	1602 3701 5200*	NA 9771 9781	NA 9772 9782	9163 9773 9783	NA	CA10 Card B C
FAC 17	1602 3701	9171	9172	9173	NA	NA
FAC 18 600 bps/2-wire 600 bps/4-wire 1200 bps/2-wire 1200 bps/4-wire	1601 5500	9181 9851 9741 9861 9751	9182 9852 9742 9862 9752	9183 9853 9743 9863 9753	CA1 Socket M02 to D08 M04 to D08 M05 to D08 M05 to D08	CA8 Card** J = on, K = off J = off, K = on J = on, K = off J = off, K = on
FAC 19 600 bps 1200 bps	1601 5501	9191 9741 9751	9192 9742 9752	9193 9743 9753	CA1 Socket M04 to D08 M05 to D08	NA
FAC 20 2400 bps 4800 bps 9600 bps	1602 5660	9201 9761 9771 9781	9202 9762 9772 9782	9203 9763 9773 9783	NA	CA7 Card A B C
FAC 21	1602 5660	9211	9212	9213	NA	CA7 Card D
FAC 24 600 bps 1200 bps 2400 bps	1601 1550	9241 9741 9751 9761	9242 9742 9752 9762	9243 9743 9753 9763	CA1 Socket M04 to D08 M05 to D08 M03 to D08	NA
FAC 27	1602 1550	9271	9272	9273	NA	NA
FAC 29	1602 1505	9291	9292	9293	NA	NA
FAC A1 (RPQ 870892)	1602 1550 5200*		QSC 2262	QSC 2263		CA10 Card
FAC 30 2400 bps 4800 bps 9600 bps	1602 5655	9301 9761 9771 9781	9302 9762 9772 9782	9303 9763 9773 9783	NA	NA
FAC 31 48,000 bps	1602 5665	9311	9312	9313	NA	NA

*Only one 5200 feature is required per 8130.
**Two-wire operation requires board jumpers (CA8 Socket): G02 to G09, J05 to J13.

Figure CA800-7. Board Wiring and Card Jumpers for 8140 SDLC Communications FAC Specify Codes (Minor)

	Required Features	Port 1	Port 2	Port 3	Board Wiring Ref CA520	Card Jumpers Ref CA563
FAC 40	1603 3701	9401	9402	9403	CA2 Socket	NA
600 bps		9741	9742	9743	M04 to D08	
1200 bps		9751	9752	9753	M05 to D08	
FAC 41	1604 3701	9411	9412	9413	NA	NA
FAC 43	1603 3701	9431	9432	9433	CA2 Socket	NA
600 bps		9741	9742	9743	M04 to D08	
1200 bps		9751	9752	9753	M05 to D08	
FAC 44	1604 3701 5200*	9441	9442	9443	NA	CA10 Card
2400 bps		9761	9762	9763		A
4800 bps		9771	9772	9773		B
9600 bps		9781	9782	9783		C
FAC 45	1603 5500	9451	9452	9453	CA2 Socket	CA8 Card**
600 bps/2-wire		9851	9852	9853	M04 to D08	J = on, K = off
600 bps/4-wire		9741	9742	9743	M04 to D08	J = off, K = on
1200 bps/2-wire		9861	9862	9863	M05 to D08	J = on, K = off
1200 bps/4-wire		9751	9752	9753	M05 to D08	J = off, K = on
FAC 47	1604 5660	9471	9472	9473	NA	CA7 Card
2400 bps		9011	9012	9013		A
4800 bps		9031	9032	9033		B
9600 bps		9051	9052	9053		C

*Only one 5200 feature is required per 8140.
**Two-wire operation requires board jumpers (CA8): G02 to G09, J05 to J13.

Figure CA800-8. Board Wiring and Card Jumpers for 8140 BSC Communications FAC Specify Codes (Minor)

	Required Features	Port 1	Port 2	Port 3	Board Wiring Ref CA520
FAC 60	1603 3701	9601	9602	9603	CA2 Socket
110 bps		9701	9702	9703	P05 to D08
134.5 bps		9711	9712	9713	M02 to D08
150 bps		9721	9722	9723	P02 to D08
300 bps		9731	9732	9733	G13 to D08
600 bps		9741	9742	9743	M04 to D08
FAC 61	1603 3701	9611	9612	9613	CA2 Socket
110 bps		9701	9702	9703	P05 to D08
134.5 bps		9711	9712	9713	M02 to D08
150 bps		9721	9722	9723	P02 to D08
300 bps		9731	9732	9733	G13 to D08
600 bps		9741	9742	9743	M04 to D08

Figure CA800-9. Board Wiring for 8140 S/S Communications FAC Specify Codes (Minor)

	Required Features	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Board Wiring Ref CA520	Card Jumpers Ref CA563
FAC 8	1602 4830	9081	9082	9083	9084	9085	9086	9087	9088	NA	NA
FAC 9	1602 4830 4835	9091	9092	9093	9094	9095	9096	9097	9098	NA	NA
FAC 10	1602 4830	9101	9102	9103	9104	9105	9106	9107	9108	NA	NA
FAC 11	1602 4830 4835	9111	9112	9113	9114	9115	9116	9117	9118	NA	NA
FAC 12	1601 3701	9121	9122	9123	9124	9125	9126	9127	9128	CA1 Socket	NA
600 bps		9741	9742	9743	9744	9745	9746	9747	9748	M04 to D08	
1200 bps		9751	9752	9753	9754	9755	9756	9757	9758	M05 to D08	
FAC 13	1602 3701	9131	9132	9133	9134	9135	9136	9137	9138	NA	NA
FAC 15	1601 3701	9151	9152	9153	9154	9155	9156	9157	9158	CA1 Socket	NA
600 bps		9741	9742	9743	9744	9745	9746	9747	9748	M04 to D08	
1200 bps		9751	9752	9753	9754	9755	9756	9757	9758	M05 to D08	
2400 bps		9761	9762	9763	9764	9765	9766	9767	9768	M03 to D08	
FAC 16	1602 3701 5200*	NA	NA	9163	9164	9165	9166	9167	9168	NA	CA10 Card
4800 bps		9771	9772	9773	9774	9775	9776	9777	9778		B
9600 bps		9781	9782	9783	9784	9785	9786	9787	9788		C
FAC 17	1602 3701	9171	9172	9173	9174	9175	9176	9177	9178	NA	NA
FAC 18	1601 5500	9181	9182	9183	9184	9185	9186	9187	9188	CA1 Socket	CA8 Card**
600 bps/2-wire		9851	9852	9853	9854	9855	9856	9857	9858	M04 to D08	J = on, K = off
600 bps/4-wire		9741	9742	9743	9744	9745	9746	9747	9748	M04 to D08	J = off, K = on
1200 bps/2-wire		9861	9862	9863	9864	9865	9866	9867	9868	M05 to D08	J = on, K = off
1200 bps/4-wire		9751	9752	9753	9754	9755	9756	9757	9758	M05 to D08	J = off, K = on
FAC 19	1601 5501	9191	9192	9193	9194	9195	9196	9197	9198	CA1 Socket	NA
600 bps		9741	9742	9743	9744	9745	9746	9747	9748	M04 to D08	
1200 bps		9751	9752	9753	9754	9755	9756	9757	9758	M05 to D08	
FAC 20	1602 5660	9201	9202	9203	9204	9205	9206	9207	9208	NA	CA7 Card
2400 bps		9761	9762	9763	9764	9765	9766	9767	9768		A
4800 bps		9771	9772	9773	9774	9775	9776	9777	9778		B
9600 bps		9781	9782	9783	9784	9785	9786	9787	9788		C
FAC 21	1602 5600	9211	9212	9213	9214	9215	9216	9217	9218	NA	CA7 Card D
FAC 24	1601 1550	9241	9242	9243	9244	9245	9246	9247	9248	CA1 Socket	NA
600 bps		9741	9742	9743	9744	9745	9746	9747	9748	M04 to D08	
1200 bps		9751	9752	9753	9754	9755	9756	9757	9758	M05 to D08	
2400 bps		9761	9762	9763	9764	9765	9766	9767	9768	M03 to D08	
FAC 25	1602 1550 5200*	9251	9252	9253	9254	9255	9256	9257	9258	NA	CA10 Card
4800 bps		9771	9772	9773	9774	9775	9776	9777	9778		B
9600 bps		9781	9782	9783	9784	9785	9786	9787	9788		C
FAC 27	1602 1550	9271	9272	9273	9274	9275	9276	9277	9278	NA	NA
FAC 29	1602 1550	9291	9292	9293	9294	9295	9296	9297	9298	NA	NA
FAC 30	1602 5655	9301	9302	9303	9304	9305	9306	9307	9308	NA	NA
2400 bps		9761	9762	9763	9764	9765	9766	9767	9768		
4800 bps		9771	9772	9773	9774	9775	9776	9777	9778		
9600 bps		9781	9782	9783	9784	9785	9786	9787	9788		
FAC 31 48,000 bps	1602 5655	9311	9312	9313	9314	9315	9316	9317	9318	NA	NA

*Only one 5200 feature is required per 8101 basic or expansion attachment type.
**Two-wire operation required board jumpers (CA8 socket): G02 to G09, J05 to J13.

Figure CA800-10. Board Wiring and Card Jumpers for 8101 SDLC Communications FAC Specify Codes (Minor)

	Required Features	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Board Wiring Ref CA520	Card Jumpers Ref CA563
FAC 40	1603	9401	9402	9403	9404	9405	9406	9407	9408	CA2	NA
	3701									Socket	
600 bps		9741	9742	9743	9744	9745	9746	9747	9748	M04 to D08	
1200 bps		9751	9752	9753	9754	9755	9756	9757	9758	M05 to D08	
FAC 41	1604	9411	9412	9413	9414	9415	9416	9417	9418	NA	NA
	3701										
FAC 43	1603	9431	9432	9433	9434	9435	9436	9437	9438	CA2	NA
	3701									Socket	
600 bps		9741	9742	9743	9744	9745	9746	9747	9748	M04 to D08	
1200 bps		9751	9752	9753	9754	9755	9756	9757	9758	M05 to D08	
FAC 44	1604	9441	9442	9443	9444	9445	9446	9447	9448	NA	CA10
	3701										Card
	5200*										
2400 bps		9761	9762	9763	9764	9765	9766	9767	9768		A
4800 bps		9771	9772	9773	9774	9775	9776	9777	9778		B
9600 bps		9781	9782	9783	9784	9785	9786	9787	9788		C
FAC 45	1603	9451	9452	9453	9454	9455	9456	9457	9458	CA2	CA8
	5500									Socket	Card**
600 bps/2-wire		9851	9852	9853	9854	9855	9856	9857	9858	M04 to D08	J = on, K = off
600 bps/4-wire		9741	9742	9743	9744	9745	9746	9747	9748	M04 to D08	J = off, K = on
1200 bps/2-wire		9861	9862	9863	9864	9865	9866	9867	9868	M05 to D08	J = on, K = off
1200 bps/4-wire		9751	9752	9753	9754	9755	9756	9757	9758	M05 to D08	J = off, K = on
FAC 47	1604	9471	9472	9473	9474	9475	9476	9477	9478	NA	CA7
	5660										Card
2400 bps		9011	9012	9013	9014	9015	9016	9017	9018		A
4800 bps		9031	9032	9033	9034	9035	9036	9037	9038		B
9600 bps		9051	9052	9053	9054	9055	9056	9057	9058		C

*Only one 5200 feature is required per 8101 basic or expansion attachment type.
**Two-wire operation requires board jumpers (CA8 socket): G02 to G09, J05 to J13.

Figure CA800-11. Board Wiring and Card Jumpers for 8101 BSC Communications FAC Specify Codes (Minor)

	Required Features	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Board Wiring Ref CA520
FAC 60	1603	9601	9602	9603	9604	9605	9606	9607	9608	CA2
	3701									Socket
110 bps		9701	9702	9703	9704	9705	9706	9707	9708	P05 to D08
134.5 bps		9711	9712	9713	9714	9715	9716	9717	9718	M02 to D08
150 bps		9721	9722	9723	9724	9725	9726	9727	9728	P02 to D08
300 bps		9731	9732	9733	9734	9735	9736	9737	9738	G13 to D08
600 bps		9741	9742	9743	9744	9745	9746	9747	9748	M04 to D08
FAC 61	1603	9611	9612	9613	9614	9615	9616	9617	9618	CA2
	3701									Socket
110 bps		9701	9702	9703	9704	9705	9706	9707	9708	P05 to D08
134.5 bps		9711	9712	9713	9714	9715	9716	9717	9718	M02 to D08
150 bps		9721	9722	9723	9724	9725	9726	9727	9728	P02 to D08
300 bps		9731	9732	9733	9734	9735	9736	9737	9738	G13 to D08
600 bps		9741	9742	9743	9744	9745	9746	9747	9748	M04 to D08

Figure CA800-12. Board Wiring for 8101 S/S Communications FAC Specify Codes (Minor)

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Chapter 5. MAP Reference Information
Diskette Storage
(DA)

Introduction

This part (DA) of Chapter 5 provides maintenance information to service the diskette storage facility used in the IBM 8130, 8140, and 8101 units. When used with IBM's MAP maintenance package, the DA MAP provides fault isolation for diskette storage problems and refers to this part of Chapter 5 for information such as hardware locations, possible-cause-of-failure lists, and logic net checking.

This part has six sections:

1. General Information (DA100–DA134): Contains information on diskette storage hardware components, basic operation, and repair strategy.
2. Offline Tests (DA200–DA258): Contains diskette test information and action plans.
3. Intermittent Failure Repair Strategy (DA300–DA356): Contains information used to repair intermittent diskette storage facility problems.
4. Signal Paths and Detailed Operational Description (DA400–DA462): Contains information on board and card logic and signal paths, as well as detailed descriptions of diskette storage facility operations.
5. Adjustment, Removal, and Replacement Information (DA500–DA670): Contains information on adjustment, removal, and replacement procedures for the diskette drive assembly and its components, including **DANGER** and **Caution** notices. It also includes diskette handling, insertion, and removal procedures.
6. Voltages and Environmental Characteristics (DA700): Contains information on the standard diskette voltages used and diskette drive environmental characteristics.

Contents

Figures

Abbreviations

ADWA	adapter work area address
ARC	adapter return code
BCLE	buffer control list element
BSTAT	basic status
C-CODE	completion code
CHCV	channel control vector
CHIO	channel I/O
CIL	Condition/Incident Log
Cnt	count
COMPSTAT	completion status
CPR	channel pointer register
CRC	cyclic redundancy check
DPCX	Distributed Processing Control Executive
DPPX	Distributed Processing Programming Executive
DT	device type
EN	error number
FM	frequency modulation
FRB	function request block
FRU	field-replaceable unit
FRWA	function request work area address
FWD	forward
GFI	General Failure Index
hex	hexadecimal
ID	identification
I/O	input/output
IOEP	I/O interrupt entry point
IOIRV	I/O Interrupt Request Vector
IPL	initial program load
LED	light-emitting diode
LV	level
MAP	Maintenance Analysis Procedure
MD	Maintenance Device
MFM	modified frequency modulation
MI	manual intervention
PA	physical address
PIO	programmed I/O
PN	part number
PSCF	Primary System Control Facility
PTX	Phototransistor
RES	reserved
R/W	read/write
SCA	secondary component address
SCF	System Control Facility
SEQ NO	sequence number
SSCF	Secondary System Control Facility
sync	synchronization
TCC	top card connector
TCM	test control monitor
UT	unit type

DA100 General Information

The DA MAP, contained on maintenance device (MD) diskette 03 and used for diskette storage fault isolation, refers to this section for locations, adjustments, service checks, or replacement procedures.

The 53FD diskette drive used in the 8100 needs no scheduled maintenance.

The diskette drive is available by part number for either vertical or side mounting. The procedures that appear in this section refer to a side-mounted diskette drive. When necessary, there are several caution notices for adjustments that must be done with the diskette drive in the side-mounted (vertical) position.

DA110 Components and Addressing

Section DA111 contains information to help you understand the physical configuration of the diskette storage facility. This information varies according to the machine type (8130, 8140, or 8101) that contains the diskette drive. Section DA112 describes the physical addresses (PAs) that must be specified to permit diskette storage information transfer. Section DA113 contains the configuration table entry needed for the diskette storage facility and lists the PA values.

DA111 Hardware Components

Diskette storage is standard in the 8130, 8140, and 8101 and has a physical gate reference of 01D. Because the adapter cards are in different board locations that depend on machine type and model, refer either to Figure DA111-1, DA111-2, or DA111-3 for these locations.

The diskette storage facility consists of two adapter cards (DA1 and DA2) and a diskette drive assembly that contains the diskette drive control card (DA3), the drive mechanism, a read/write head and track access (head/carriage) assembly, and the associated cables needed for control and power.

The diskette drive connects to its adapter through two cable assemblies. The control cable supplies logic signals, read/write data, and dc power; the power cable supplies ac power directly to the diskette drive motor from the power supply of the machine type that contains the drive.

See DA516 for detailed diskette drive assembly locations.

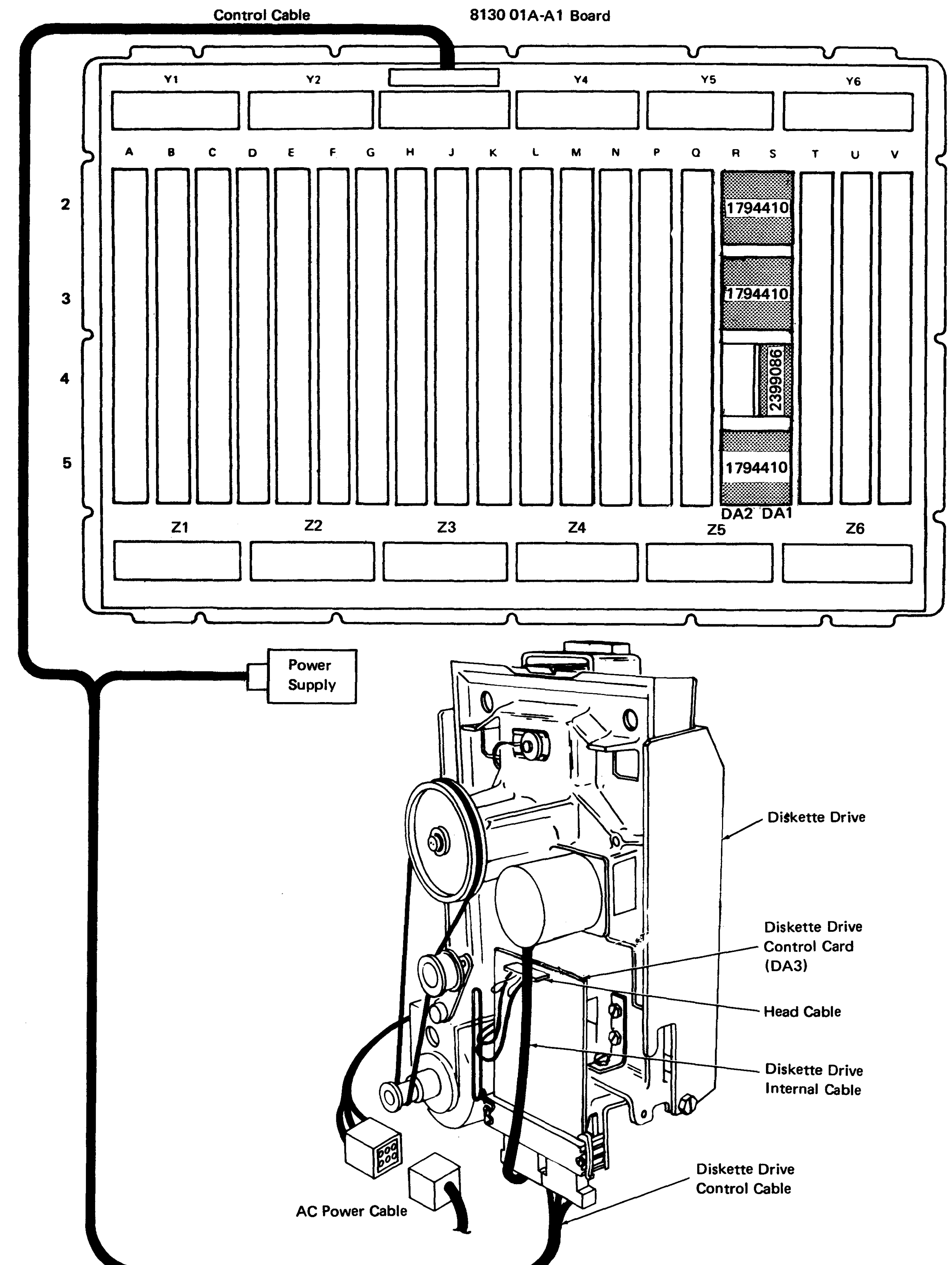


Figure DA111-1. 8130 Diskette Storage Hardware Configuration

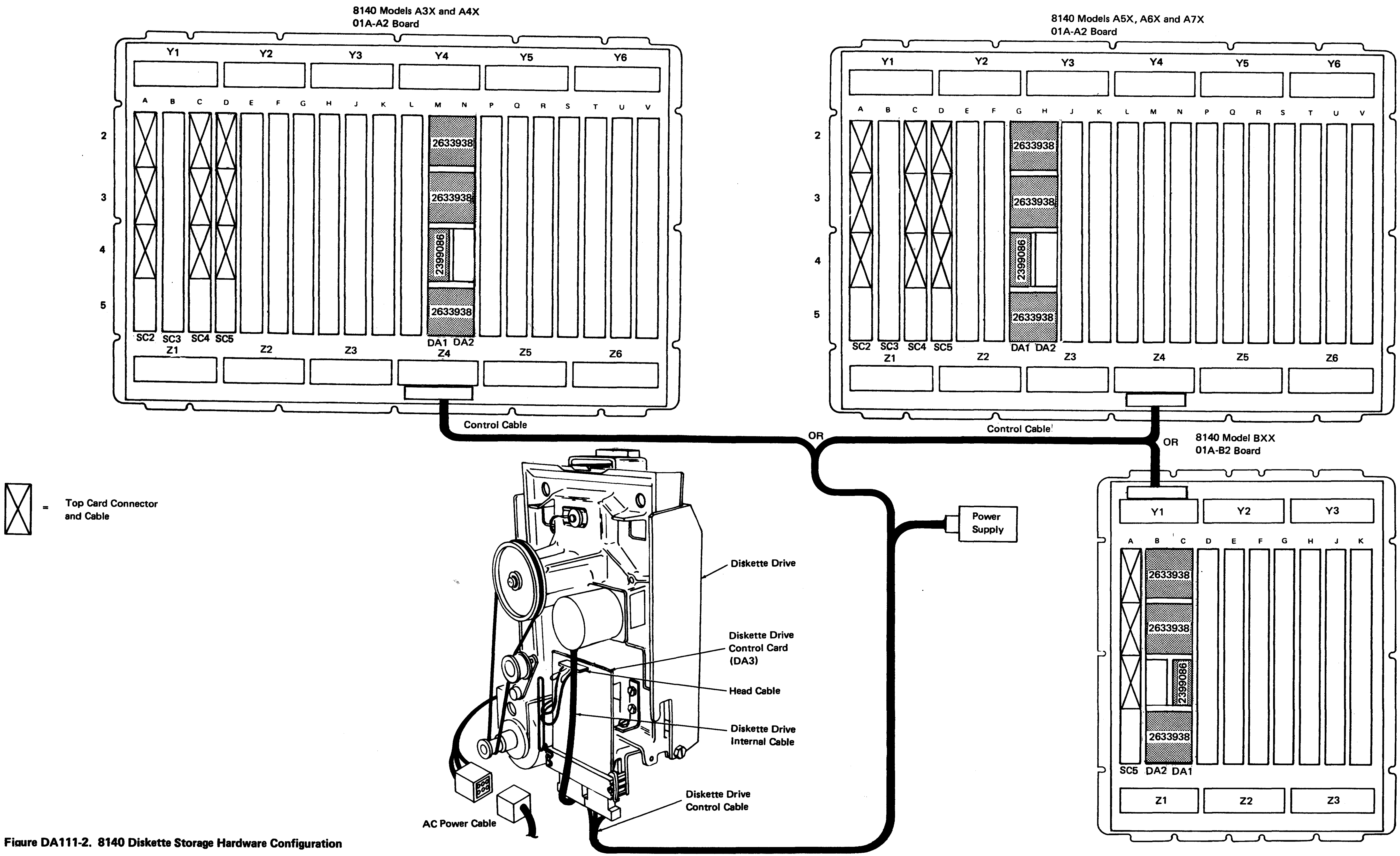


Figure DA111-2. 8140 Diskette Storage Hardware Configuration

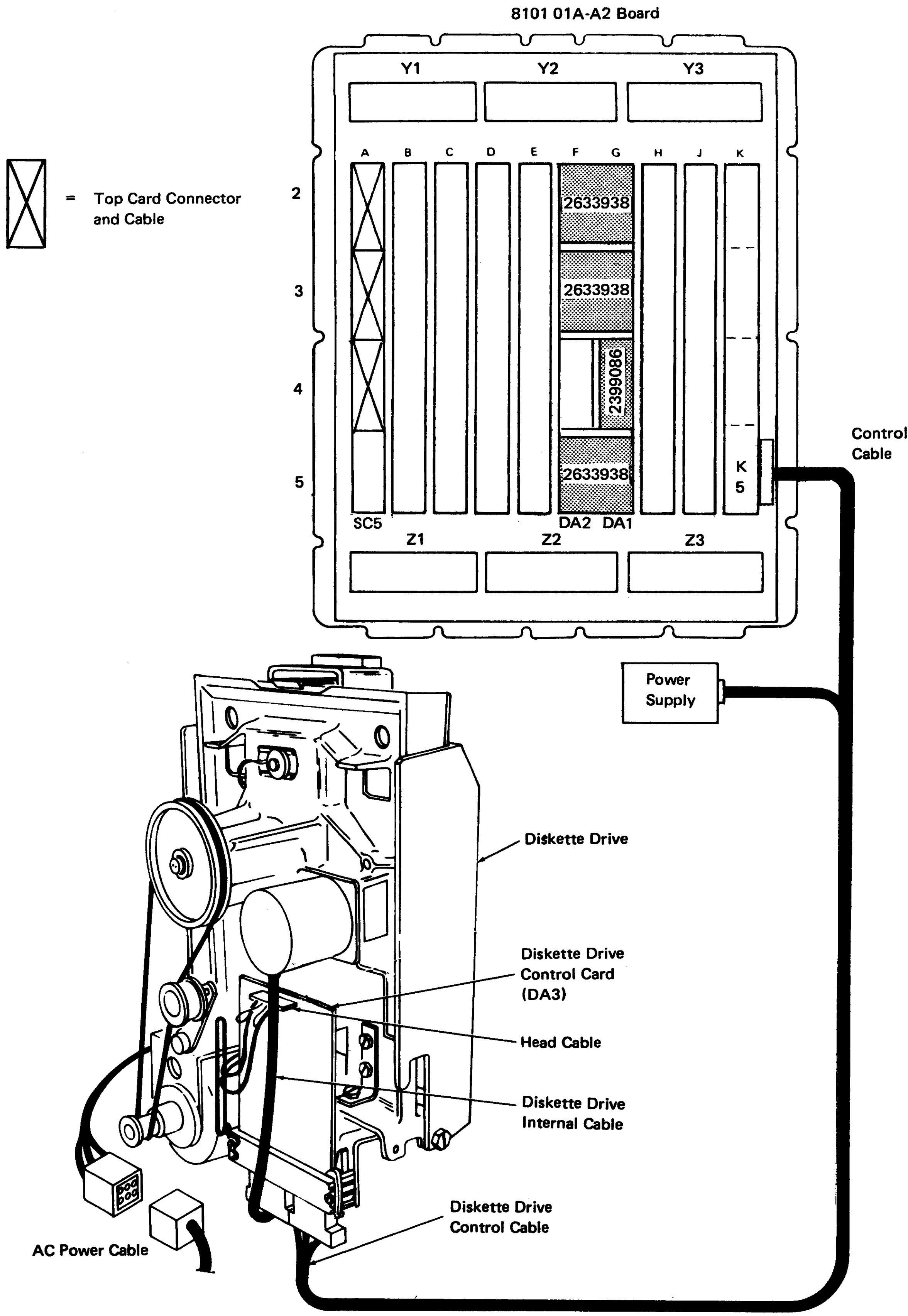


Figure DA111-3. 8101 Diskette Storage Hardware Configuration

DA112 Addressing

Addressable 8100 components, such as the diskette storage facility, require a unique PA to enable information transfer. The PA has two hex characters, each of which determines a separate addressing parameter:

- The "P" value specifies the SCF group address, determined by:
  - Board wiring in an 8130 without the System Expansion Feature.
  - The setting of the SSCF (SC5 card) address switches for 8130s with the System Expansion Feature and for all 8140s and 8101s.
- The "A" value specifies the address within the SSCF group (always 7 for diskette storage).

Refer to CP210 "Addressing Levels" in Chapter 2 for a discussion of addressing. Refer to DA113 for the physical address values, which are part of the configuration table entry. This value depends on the machine type and, for an 8101, the logical system location of the 8101 that contains the diskette storage.

DA113 Configuration Table Entry

In an 8100, the configuration table entry defines the addressing level (LV), physical address (PA), unit type (UTUT), and option parameters (OPOP). The diskette storage facility uses the standard 8100 configuration table entry format, which is:

LV PA UTUT OPOP OPOP

Where:

LV = 01

PA = 87 = 8130/8140
97 = 1st 8101
A7 = 2nd 8101
B7 = 3rd 8101
C7 = 4th 8101

UTUT = 0002

OPOP = Not used

OPOP = Not used

DA120 Basic Description and Operation

DA121 Diskette Drive Basic Description

The diskette drive is a direct-access read/write storage device that records and retrieves data and which generally can be used:

- To initially load the control program.
- As a microprogram storage backup.
- For diagnostic microprogram storage.
- In any application where data exchange media (card, tape, or disk) are presently used.

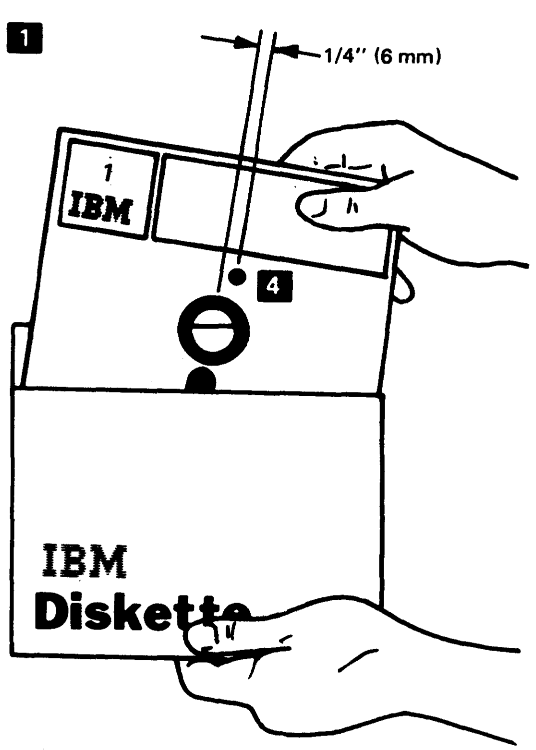
The diskette storage medium used for this device is a thin, flexible disk contained in a protective envelope. A coating of magnetic material on the disk surface enables the reading and writing of information.

The 53FD diskette drive used in the 8100 **3** can read and write single- or double-density information (depending on diskette type) on both sides of a two-sided diskette, and single-density information on side 0 of a single-sided diskette. The diskette type 1 **1** uses only one physical side, while the diskette type 2 **2** uses both. The diskette type 2D is physically identical to the type 2, but can be formatted to have an information density twice that of diskette types 1 and 2.

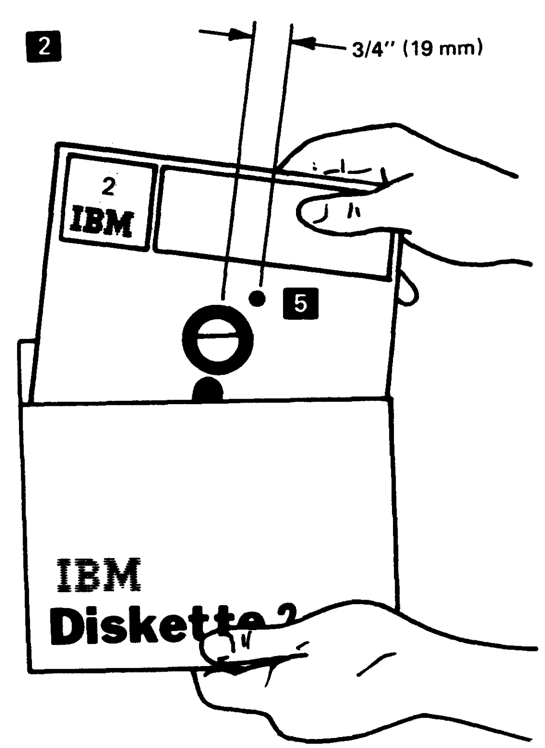
Drive logic senses the physical location of the index holes **4** and **5** to determine the diskette type, and responds with a signal that identifies the type loaded.

The 53FD input/output device provides a low-cost method of data entry, exchange, and storage because its media is compatible with that of any single-sided or double-sided diskette drive. This allows use of the diskettes at other locations to exchange data in the basic data exchange format.

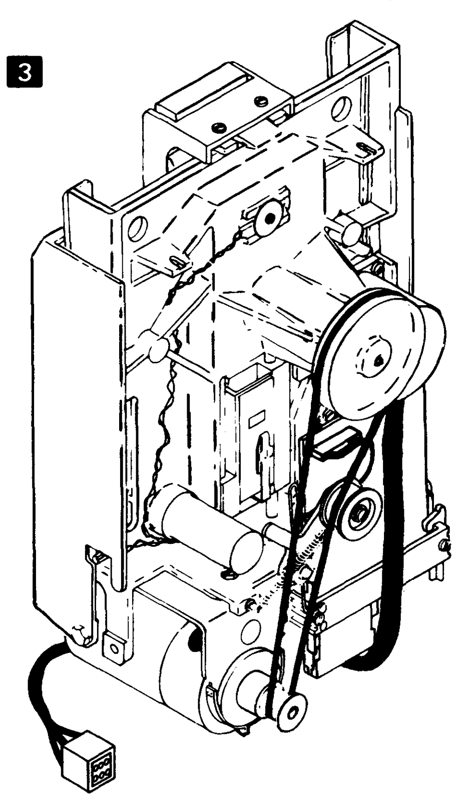
1



2



3



DA122 Diskette Drive Basic Operation

Powering on the machine type that contains the diskette drive permits the diskette drive motor to turn the drive hub at 360 rpm. Inserting the diskette and closing the cover clamps the diskette between the collet and the drive hub, which turns the diskette; opening the cover releases the clamping action, permitting diskette removal.

The diskette drive control card (DA3) sends Index pulses to the diskette adapter DA1 card when the diskette begins rotating. Each rotation generates one Index pulse approximately every 166.7 ms. The diskette adapter can then determine if the drive contains a diskette rotating at the correct speed. The Diskette Sense signal, which is active for a two-sided diskette, determines the diskette type.

The diskette adapter activates the Head Engage signal at the start of any read or write operation. This signal energizes the head load solenoid, causing the bail to load the read/write heads. A data valid condition occurs approximately 80 ms after Head Engage becomes active, which initiates diskette to diskette adapter data transfer.

The diskette adapter determines the read/write head location either by examining the track ID data or by positioning the head/carriage assembly at track 0. The adapter then moves the head/carriage either in (toward the hub) or out by sequencing the four access lines. Activating two sequential access lines moves the stepper motor, which causes the head/carriage to move a distance equal to one track (cylinder). The diskette drive requires 5 ms to access (seek to) each cylinder, and it also requires 35 ms for the head/carriage assembly to stop.

After moving the head/carriage to the selected track, the last two access lines remain active to electrically detent the stepper motor, and the adapter then performs a read or a write operation. The Head Engage signal turns off after completion of the last read, write, or seek operation to reduce head wear.

Single-Sided Diskette Format

A diskette track is a circular path on one side of the diskette surface. On a diskette type 1 surface, there are 77 tracks written in frequency modulation (FM) mode and numbered consecutively from 00 to 76, with 00 located on the outside edge. Only 74 of these can be used for data, as track 00 contains label information and tracks 75 and 76 are reserved for alternate track assignments when others become defective.

Tracks are divided into either 8, 15, or 26 sectors, each of which contains one record. Each sector contains two basic areas: the sector ID field and the data or control record field. Refer to the illustration below for the physical track and sector layout and also for a graphic representation of the hexadecimal sector contents.

Note: *An initialized (formatted) diskette is one that has all sectors written with their respective track and sector ID (address) information.*

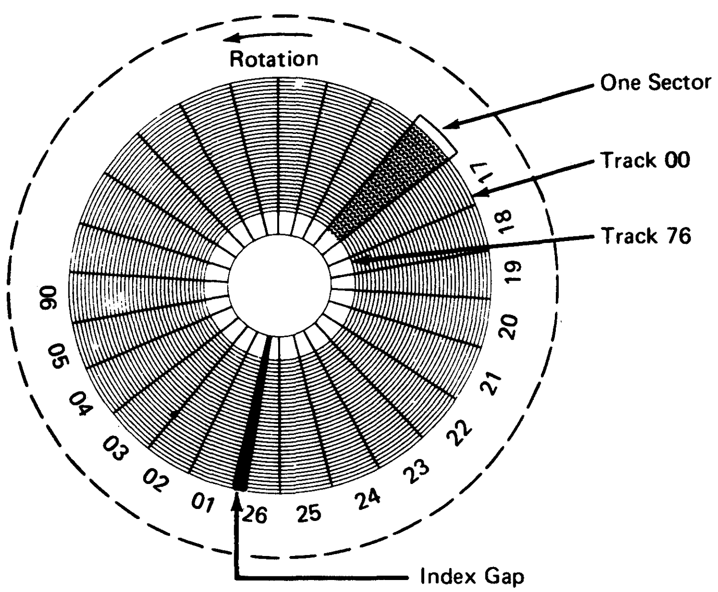
As there are 74 usable data tracks, the diskette type 1 capacity in formatted data bytes is:

Sectors per Track	Bytes per Sector	Diskette Capacity
8	512	303,104
15	256	284,160
26	128	246,272*

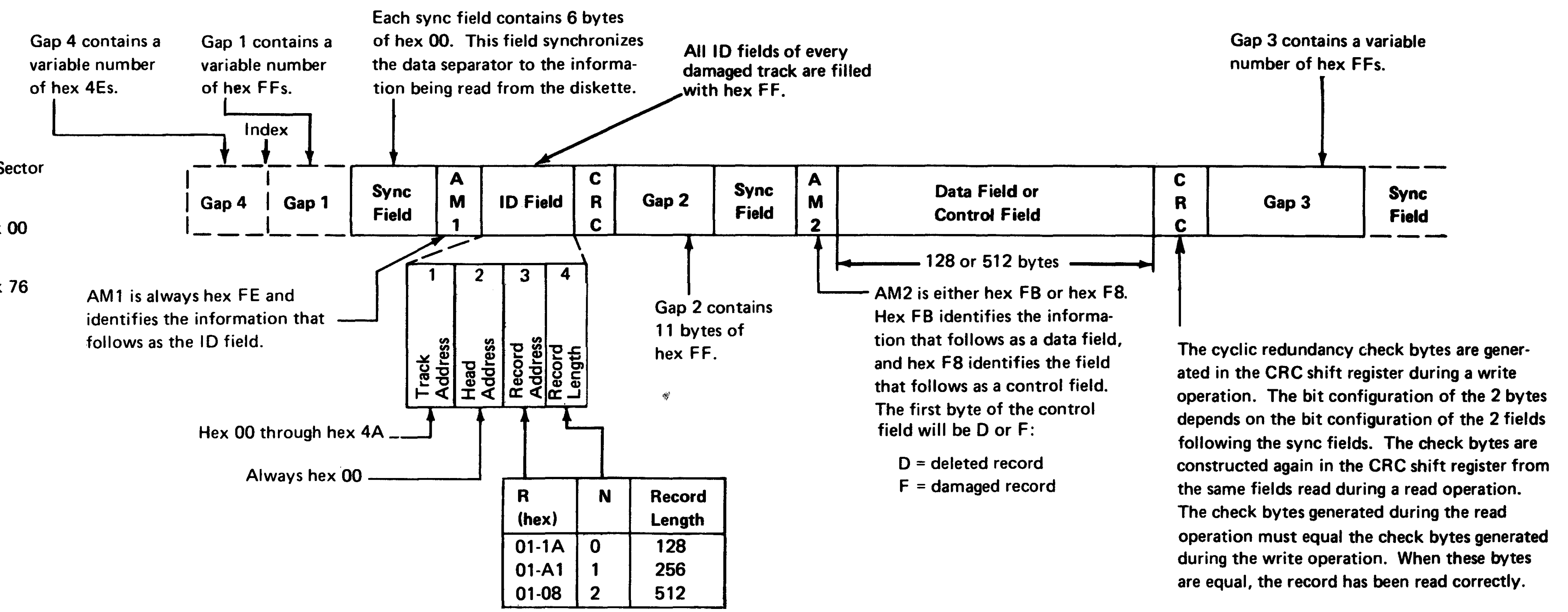
*Basic data exchange for a diskette type 1.

Data transfer for this diskette type occurs at 250,000 bits (31,250 bytes) per second, as it uses only the FM recording mode.

When a defective track condition occurs, the identification (ID) fields of the defective track are written into the ID field of the next higher numbered track, and binary 1's are written into the defective one. Any subsequent access to the defective track results in an automatic seek to the next higher numbered track.



Diskette Track and Sector Layout (Formatted with 26 Sectors)



R (hex)	N	Record Length
01-1A	0	128
01-A1	1	256
01-08	2	512

Hexadecimal Sector Contents

Double-Sided Diskette Format

A diskette track is a circular path on one side of the diskette surface. A diskette cylinder is a circular path on both diskette surfaces. Therefore, a cylinder on diskette types 2 and 2D consists of two tracks, one on each side of the diskette, that can be written or read without moving the head/access assembly.

On a diskette type 2 and 2D surface, there are 77 cylinders. On type 2, the cylinders are written in FM mode, while on type 2D, they can be written either in FM or modified FM (MFM) mode. Both types have the cylinders numbered consecutively from 00 to 76, with 00 located on the outside edge. Only 74 of these can be used for data. Track 00 of cylinder 00 contains label information written in FM mode. Track 01 of cylinder 00 contains extended label information written in MFM mode on a diskette type 2D and in FM mode on diskette type 2. Cylinders 75 and 76 are reserved for alternate cylinder assignments when others become defective.

Tracks are divided into either 8, 15, or 26 sectors, each of which contains one record. Each sector contains two basic areas: the sector ID field and the data or control record field. Refer to the illustration below for the physical cylinder and sector layout and also for a graphic representation of the hexadecimal sector contents.

Note: *An initialized (formatted) diskette is one that has all sectors written with their respective track and sector ID (address) information.*

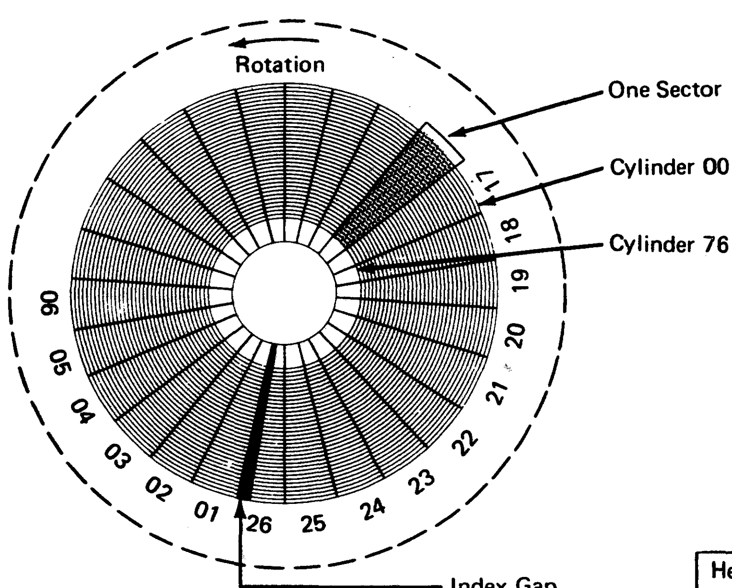
The 53FD diskette drive can record data on both sides of a diskette type 2 in FM mode, or on both sides of a diskette type 2D in either FM or MFM mode. As there are 74 usable data tracks and two tracks per cylinder, the diskette type 2D capacity in formatted data bytes is:

Sectors per Track	Bytes per Sector		Diskette Capacity	
	FM	MFM	FM	MFM
8	512	1024	606,208	1,212,416
15	256	512	568,320	1,136,640
26	128	256	492,544*	985,088**

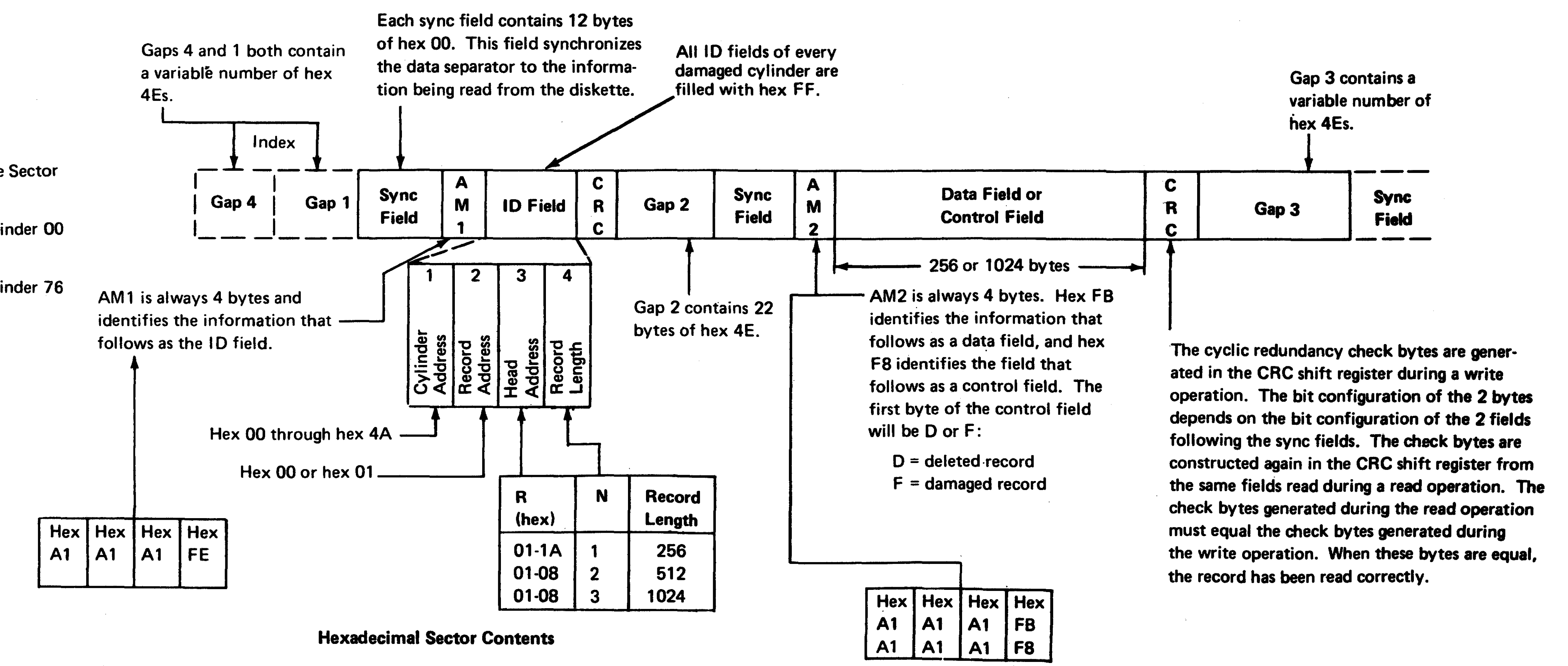
*Basic data exchange for a diskette type 2.
**Data exchange for a diskette type 2D.

Data transfer for these diskette types occurs either at 250,000 bits (31,250 bytes) per second when using the FM recording mode, or at 500,000 bits (62,500 bytes) per second when using the MFM recording mode.

When a defective track condition occurs, both tracks of the cylinder are flagged as defective. The ID fields of the defective cylinder are written into the ID field of the next higher numbered cylinder, and binary 1's are written into the defective one. Any subsequent access to the defective cylinder results in an automatic seek to the next higher numbered cylinder.



Diskette Cylinder and Sector Layout (Formatted with 26 Sectors)



Hexadecimal Sector Contents

DA130 Adapter Unique Repair Strategy

Use the General Failure Index (GFI) in Chapter 1 for initial diskette storage fault isolation. The GFI instructs you to use the DA MAP contained on MD diskette 03 to perform the checks described in DA131, DA132, and DA133. In summary, use the following:

- Option A (offline checkout) to verify diskette storage operation and correct any failures (DA131).
- Option D to perform a diskette surface analysis (DA132).
- Option E to verify diskette head alignment (DA133).

DA131 Offline Repair Strategy

Offline checkout requires use of the entire system. To perform a diskette storage offline checkout, obtain the 8100 system from the customer. Maintenance device (MD) diskette 03 contains the DA MAP and offline diskette storage tests, which are loaded from the MD. Select the offline checkout option A from the DA MAP menu.

The MAP first instructs you to install a correctly formatted diskette in the drive to be tested and then runs the diskette storage offline tests. The MAP isolates the problem to either the diskette adapter, the adapter/diskette drive, or the system control facility (SCF).

If the DA MAP isolates the problem to the diskette adapter, it directs you to replace the FRU(s) causing the problem. If still not corrected or it cannot isolate the problem to a single FRU, the MAP then refers you to procedures in DA250 for further corrective action, such as replacing multiple FRUs and checking logic signals.

If the DA MAP isolates the problem to either the diskette adapter or diskette drive, it directs you to perform a series of checks to further isolate the failure, and then directs you to replace the failing FRU(s). If still not corrected or if it cannot isolate the problem to a single FRU, the MAP refers you to procedures in DA250 for further corrective action, such as replacing multiple FRUs and checking logic signals.

If the DA MAP isolates the problem to the SCF, it directs you to use either an action plan in DA430 or the SC MAP on MD diskette 01 to perform further fault isolation.

DA132 Diskette Surface Analysis

Obtain the 8100 system from the customer. MD diskette 03 contains the diskette surface analysis test, which is loaded from the MD. Select option D from the DA MAP menu to analyze the surface of any formatted (initialized) diskette.

The DA MAP instructs you to install the diskette and enter the cylinder(s) to be checked. You can check from one to all of the diskette cylinders by entering the decimal number of the first and last cylinder numbers to be tested. The MAP then runs the surface analysis program and displays the test results at the MD.

DA133 Read/Write Head Alignment Verification

Obtain the 8100 system from the customer. MD diskette 03 contains the head alignment verification tests, which are loaded from the MD. Select option E from the DA MAP menu to check diskette drive head alignment.

The DA MAP instructs you to install a Test Alignment Diskette, PN 2455026.

Note: *This diskette is not shipped with the system and must be obtained from the Branch Office.*

The MAP then runs the head alignment program and displays the test results at the MD.

DA134 Intermittent Failure Strategy

The following basically explains the diskette storage intermittent failure strategy. For detailed information, see DA300.

- If an error occurs after looping the tests for more than 10 minutes, record the test error message and use the Free-Lance Utility (DA313) and the action plans in DA250.
- If an error occurs so infrequently that looping the tests cannot determine the failure, the DA MAP refers you to the system error log (DA312).
- If an error occurs at random times thus causing different test error messages, all MAPs are ineffective. After receiving three different test error messages, the DA MAP refers you to the action plans in DA250.

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DA200 Offline Tests

There are no online tests provided for the diskette storage facility. Only offline tests, contained on maintenance device (MD) diskette 03, enable you to test and repair diskette storage components. The offline tests verify the operation of the diskette adapter and drive, and run under control of the offline test control monitor (TCM).

The offline diskette storage tests can be invoked only from the MD. The DA MAP automatically invokes these tests when required, or you can invoke them if using the Free-Lance Utility as follows:

1. At either 80BC or PA00, enter PAB.
2. At 81BC, enter SLRRB.

Where:

PA = Physical address (see DA112)

S = Sense option

= 0 = run only adapter Routines 01 through 04.

= 1 = run adapter/device Routines 01 through 26.

= 2 = run adapter/device Routines 01 through 27 with manual intervention.

L = Loop option

= 0 = run the routines specified by the sense option once.

= 1 = loop the routines specified by the sense option and stop on any error.

= 2 = loop the routines specified by the sense option and bypass all errors.

RR = Routine number. If 00 or not specified, run all routines according to the sense option. If specified, run only that routine.

Caution: Do not use an MD or a CSU diskette for Routine 28, as the routine destroys data on cylinders 1, 50, and 72.

Note: *You must use the RR option to select Routines 28 through 31.*

B = Begin execution and enter the invocation message.

DA210 Offline Test Routine Descriptions

The diskette storage offline tests consist of 30 routines:

- The first four routines verify adapter functions only.
- The next 22 (05 through 27 with 24 not assigned) verify both adapter and diskette drive operation by using the adapter and previously tested adapter logic.
- The last four (28 through 31) are selectable only, and aid in performing and verifying diskette head alignment, performing diskette surface analysis, and checking the write current and filter logic.

Caution: The following routines destroy data on the cylinders indicated:

Routine	Cylinder(s)
12	74
13	74
14	73
15	73
16	72
17	72
18	74
19	74
20	73
21	73
22	72
23	72
25	72
26	72, 73, 74
28	1, 50, 72

Sections DA211 and DA212 briefly describe each routine.

DA211 Diskette Adapter Tests

Routine 01, I/O Address Recognition Test. Issues an Adapter Reset command to test the adapter information path. If successful, the routine then reads the adapter status to verify the expected reset condition.

Routine 02, Adapter Status Test. Verifies proper operation of all commands that set, reset, and read the adapter status registers. The routine also verifies that the adapter can enable, disable, and generate an I/O interrupt.

Routine 03, Invalid Command Test. Issues all invalid commands to the diskette adapter. Each command should cause an I/O machine check interrupt and also set the machine check bit in the diskette adapter basic status register.

Routine 04, Channel Control Vector (CHCV) Pointer Test. Issues Write CHCV and |Read CHCV commands, which should set the CHCV to any valid value.

DA212 Diskette Drive Tests

The following summarizes the diskette drive routines:

- Routines 12 through 26 and 28 destroy data on the cylinders as indicated in their routine descriptions.
- Routine 26 should be run after manually selecting any write test routine (12 through 25). This restores the standard information format for normal diskette use.
- Routines 27, 29, 30, and 31 have manual intervention stops; Routine 11 has a manual intervention stop if the diskette label specifies write-protection.
- Routines 28, 29, 30, and 31 are selectable only.
- Not all routines run on all diskette types (see Figure DA212-1).
- Manually selecting any routine from 12 through 25 causes automatic invocation of a previous routine or routines (see Figure DA212-1).

Routine(s)	Runs on Single-Sided Diskette	Runs on Double-Sided Diskette	Manual Selection Automatically Invokes Additional Routine Number(s)
05-11	Yes	Yes	None
12,14,16	Yes	Yes	11
13	Yes	Yes	11,12
15	Yes	Yes	11,14
17	Yes	Yes	11,16
18,20,22	No	Yes	11
19	No	Yes	11,18
21	No	Yes	11,20
23	No	Yes	11,22
25,26,28	Yes	Yes	11
27,29,30,31	Yes	Yes	None

Figure DA212-1. Diskette Drive Test Invocation Summary

Read and Seek Tests

Routine 05, Channel I/O, Buffer, and Drive Ready Test. Uses a unique 256-byte data pattern to ensure the sensing of incorrect data transfers. This routine tests that the diskette adapter can:

- Transfer channel I/O data to and from the processor.
- Set all buffer data and parity bits to both 0's and 1's.
- Sense a parity error and cause an interrupt.
- Sense a drive-not-ready condition.

Routine 06, Recalibrate and Read ID Test. Executes up to two seeks of 80 cylinders each, and performs a Read ID operation after each seek to verify the cylinder. This should move the head/carriage assembly to cylinder 0. If the Read ID operation completes successfully, with the possible exception of a CRC error, the routine next obtains the CRC ID value from the adapter buffer. The routine then determines the actual CRC and compares it to the value read from the buffer. If the ID indicates cylinder 0, the routine terminates; if not, the routine retries the seek and read ID operations.

Routine 07, Record Search Test. Executes a Read ID to the diskette volume label (record 7), which verifies that the adapter can locate a specific record. The routine then issues a Read ID using a value greater than 26, which verifies that the adapter can recognize an invalid record number.

Routine 08, Multiple Sector Test. Executes a multisector Read ID, which verifies that the adapter can perform a multiple sector Read ID operation. The routine then issues a multisector Read ID with a value that exceeds the end of the cylinder (track). This verifies that the adapter can terminate an invalid multiple sector record.

Routine 09, Diskette Revolution Speed Test. Issues multiple Read IDs to sector 1 and measures the time required for command completion. These times are then used to calculate the diskette rotational speed, which should be between 162.5 ms and 170.9 ms.

Routine 10, Seek Test. Determines if the drive can seek to all cylinders from 0 to 71. The routine issues a series of single cylinder seeks both in and out, records any flagged cylinders for later use, and then performs a series of multiple cylinder seeks. After each seek, the routine reads the cylinder ID and compares it to the expected value.

Routine 11, Write Test Preparation. Determines if the loaded diskette is either:

- Single-sided or double-sided.
- Write-protected or can be used for write operations.
- ASCII or EBCDIC.
- FM or MFM encoded.

The routine locates cylinders 72—74 and records their locations relative to cylinder 68, and also checks the data set header label on cylinder 0 to determine if cylinders 72—74 are allocated (write-protected).

Note: *A PA01 manual intervention stop occurs for a write-protected diskette (see DA231).*

Write Tests

Routine 12, 128-Byte FM Format and Read Test.

Caution: This routine destroys data on cylinder 74, head 0.

Routine 12 (see Figure DA212-1) first issues a seek to cylinder 74, head 0, and formats the track with 128-byte data records using FM encoding. All data bytes of all records now contain the record number, and record 5 has an invalid CRC field. After formatting, the routine reads the data written and compares it to the data expected. Record 5 should cause a CRC check. After the read operation, the routine executes a read-back check, which calculates the CRC field and does not place the data in storage. Record 5 should again cause a CRC check.

Routine 13, 128-Byte FM Write Test.

Caution: This routine destroys data on cylinder 74, head 0.

Routine 13 (see Figure DA212-1) twice rewrites record 5 on cylinder 74, head 0. Both data patterns are identical, but the second has a 2-byte offset compared to the first. After each write, the routine reads the data written and compares it to the data expected. No errors should occur. After the read operation, the routine executes a read-back check, which calculates the CRC field and does not place the data in storage. No errors should occur. The routine finally executes a multisector write to sectors 5 and 6 and a multisector read to sectors 5, 6, and 7. The data that was read from sectors 5 and 6 is then compared to the data written, and record 7 should remain unchanged.

Routine 14, 256-Byte FM Format and Read Test.

Caution: This routine destroys data on cylinder 73, head 0.

Routine 14 (see Figure DA212-1) first issues a seek to cylinder 73, head 0, and formats the track with 256-byte data records using FM encoding. All data bytes of all records now contain the record number, and record 5 has an invalid CRC field. After formatting, the routine reads the data written and compares it to the data expected. Record 5 should cause a CRC check. After the read operation, the routine executes a read-back check, which calculates the CRC field and does not place the data in storage. Record 5 should again cause a CRC check.

Routine 15, 256-Byte FM Write Test.

Caution: This routine destroys data on cylinder 73, head 0.

Routine 15 (see Figure DA212-1) twice rewrites record 5 on cylinder 73, head 0. Both data patterns are identical, but the second has a 2-byte offset compared to the first. After each write, the routine reads the data written and compares it to the data expected. No errors should occur. After the read operation, the routine executes a read-back check, which calculates the CRC field and does not place the data in storage. No errors should occur. The routine finally executes a multisector write to sectors 5 and 6 and a multisector read to sectors 5, 6, and 7. The data that was read from sectors 5 and 6 is then compared to the data written, and record 7 should remain unchanged.

Routine 16, 512-Byte FM Format and Read Test.

Caution: This routine destroys data on cylinder 72, head 0.

Routine 16 (see Figure DA212-1) first issues a seek to cylinder 72, head 0, and formats the track with 512-byte data records using FM encoding. All data bytes of all records now contain the record number, and record 5 has an invalid CRC field. After formatting, the routine reads the data written and compares it to the data expected. Record 5 should cause a CRC check. After the read operation, the routine executes a read-back check, which calculates the CRC field and does not place the data in storage. Record 5 should again cause a CRC check.

Routine 17, 512-Byte FM Write Test.

Caution: This routine destroys data on cylinder 72, head 0.

Routine 17 (see Figure DA212-1) twice rewrites record 5 on cylinder 72, head 0. Both data patterns are identical, but the second has a 2-byte offset compared to the first. After each write, the routine reads the data written and compares it to the data expected. No errors should occur. After the read operation, the routine executes a read-back check, which calculates the CRC field and does not place the data in storage. No errors should occur. The routine finally executes a multisector write to sectors 5 and 6 and a multisector read to sectors 5, 6, and 7. The data that was read from sectors 5 and 6 is then compared to the data written, and record 7 should remain unchanged.

Routine 18, 256-Byte MFM Format and Read Test.

Caution: This routine destroys data on cylinder 74, head 1.

Routine 18 (see Figure DA212-1) first issues a seek to cylinder 74, head 1, and formats the track with 256-byte data records using MFM encoding. All data bytes of all records now contain the record number, and record 5 has an invalid CRC field. After formatting, the routine reads the data written and compares it to the data expected. Record 5 should cause a CRC check. After the read operation, the routine executes a read-back check, which calculates the CRC field and does not place the data in storage. Record 5 should again cause a CRC check.

Routine 19, 256-Byte MFM Write Test.

Caution: This routine destroys data on cylinder 74, head 1.

Routine 19 (see Figure DA212-1) twice rewrites record 5 on cylinder 74, head 1. Both data patterns are identical, but the second has a 2-byte offset compared to the first. After each write, the routine reads the data written and compares it to the data expected. No errors should occur. After the read operation, the routine executes a read-back check, which calculates the CRC field and does not place the data in storage. No errors should occur. The routine finally executes a multisector write to sectors 5 and 6 and a multisector read to sectors 5, 6, and 7. The data that was read from sectors 5 and 6 is then compared to the data written, and record 7 should remain unchanged.

Routine 20, 512-Byte MFM Format and Read Test.

Caution: This routine destroys data on cylinder 73, head 1.

Routine 20 (see Figure DA212-1) first issues a seek to cylinder 73, head 1, and formats the track with 512-byte data records using MFM encoding. All data bytes of all records now contain the record number, and record 5 has an invalid CRC field. After formatting, the routine reads the data written and compares it to the data expected. Record 5 should cause a CRC check. After the read operation, the routine executes a read-back check, which calculates the CRC field and does not place the data in storage. Record 5 should again cause a CRC check.

Routine 21, 512-Byte MFM Write Test.

Caution: This routine destroys data on cylinder 73, head 1.

Routine 21 (see Figure DA212-1) twice rewrites record 5 on cylinder 73, head 1. Both data patterns are identical, but the second has a 2-byte offset compared to the first. After each write, the routine reads the data written and compares it to the data expected. No errors should occur. After the read operation, the routine executes a read-back check, which calculates the CRC field and does not place the data in storage. No errors should occur. The routine finally executes a multisector write to sectors 5 and 6 and a multisector read to sectors 5, 6, and 7. The data that was read from sectors 5 and 6 is then compared to the data written, and record 7 should remain unchanged.

Routine 22, 1024-Byte MFM Format and Read Test.

Caution: This routine destroys data on cylinder 72, head 1.

Routine 22 (see Figure DA212-1) first issues a seek to cylinder 72, head 1, and formats the track with 1024-byte data records using MFM encoding. Sectors 1 through 4 and 6 through 8 are written to ensure correct CRC fields. All data bytes of all records now contain the record number, and record 5 has an invalid CRC field. After formatting, the routine reads the data written and compares it to the data expected. Record 5 should cause a CRC check. After the read operation, the routine executes a read-back check, which calculates the CRC field and does not place the data in storage. Record 5 should again cause a CRC check.

Routine 23, 1024-Byte MFM Write Test.

Caution: This routine destroys data on cylinder 72, head 1.

Routine 23 (see Figure DA212-1) twice rewrites record 5 on cylinder 72, head 1. Both data patterns are identical, but the second has a 2-byte offset compared to the first. After each write, the routine reads the data written and compares it to the data expected. No errors should occur. After the read operation, the routine executes a read-back check, which calculates the CRC field and does not place the data in storage. No errors should occur. The routine finally executes a multisector write to sectors 5 and 6 and a multisector read to sectors 5, 6, and 7. The data that was read from sectors 5 and 6 is then compared to the data written, and record 7 should remain unchanged.

Routine 24. Not Assigned.

Routine 25, Overrun and Record Not Found Test.

Caution: This routine destroys data on cylinder 72.

Routine 25 (see Figure DA212-1) formats cylinder 72 with various invalid sector types and then reads them back. This generates all possible overrun and record-not-found conditions, which should be recognized as errors.

Routine 26, Write Test Cleanup.

Caution: This routine destroys data on cylinders 72, 73, and 74.

Routine 26 reformats (reinitializes) cylinders 72, 73, and 74 as "deleted" records using the proper diskette encoding (FM or MFM), record length (128, 256, 512, or 1024), and character type (ASCII or EBCDIC). After formatting, the routine reads the data written and compares it to the data expected.

Note: *You should run this routine if you manually selected any write test routine (12 through 25). This restores the standard information format for normal diskette use. The routine runs automatically if you did not specify a routine option.*

Routine 27, Ready/Not Ready Test. This manual intervention routine first checks the diskette status to determine the diskette type mounted. If single-sided, it selects head 1, which should cause the drive to drop ready status. If this occurs, it then selects head 0 and the drive should again become ready.

When using any diskette type, at message PA11, open the diskette drive cover. The routine should loop on read status until the drive drops ready. After detecting the not-ready status, the routine generates message PA12. Close the cover. The routine should again loop on read status until the drive becomes ready.

Note: *PA11 and PA12 are error indications if the ready status does not change after performing the manual intervention procedure.*

Routine 28, Write Current and Filter Select Test.

Caution: Since this routine destroys data on cylinders 1, 50, and 72, do not use an MD or a CSU diskette; use only a formatted scratch diskette.

This selectable-only routine writes and then reads record 5 on cylinders 1, 50, and 72 using the following write current and filter select combinations:

- Cylinder 72 with both write current and filter select.
- Cylinder 50 with only write current.
- Cylinder 01 with neither.

The routine then reformats head 0 of the above cylinders.

Routine 29, Surface Analysis. This selectable-only routine reads one or more cylinders and has two manual intervention stops. PA21 permits you to change diskettes and/or enter the first and last cylinders to be tested; PA23 TTHX RRII DDAA displays a condition code that indicates the test results.

Routine 29 Description. The routine first seeks to cylinder 0 and reads the diskette volume label, which determines the encoding (FM or MFM), type (single- or double-sided), and record length (128, 256, 512, or 1024 bytes). It then loads the heads, reads the ID, and seeks to the first cylinder specified at the PA21 message.

At this cylinder, the routine reads the ID. This verifies the cylinder address and also determines the record length. If the ID does not compare with the cylinder selected, the routine attempts recovery by moving the head/carriage assembly in the same direction to the next cylinder, reloads the heads, and issues another Read ID. Should the IDs still not compare, the recovery procedure occurs once more. If no ID compare occurs after two recovery attempts, the routine generates a PA23 TTH1 0000 0000 manual intervention stop.

At the first cylinder selected, the routine reads all records on that cylinder and verifies all CRCs for each ID and data field. If the routine senses one or more errors, a PA23 manual intervention stop occurs after reading all records on that cylinder.

If the routine did not sense any errors, it compares the current cylinder number to the last cylinder number specified at PA21. If equal, the test completes; if unequal, the current cylinder number increments by 1 and the head/carriage assembly moves to the next cylinder, where cylinder verification occurs and the read sequence repeats.

Routine 29 Selection and Operation. You can do a diskette surface analysis by using either a DA MAP option or the Free-Lance Utility. Proceed in order as follows:

1. Load MD diskette 03 and either:
   a. Select the DA MAP and use MAP menu option D, or
   b. Use the Free-Lance Utility and select Routine 29 (see DA200).
2. At the PA21 message, you can either change diskettes or use the one already loaded. Enter a four-digit number that specifies the first and last decimal cylinder numbers to be tested. Enter the same number twice for only one cylinder. The routine converts these values to binary.
3. At the PA23 message, refer to the following:

   PA23 TTH0 RRII DDAA = Recoverable errors detected.

   PA23 TTH1 0000 0000 = Unrecoverable seek error; could not locate cylinder.

   PA23 TTH1 RRII DDAA = Unrecoverable ID failure.

   PA23 TTH2 RRII DDAA = Unrecoverable data CRC failure.

   PA23 TTH3 RRII DDAA = Unrecoverable data address mark failure.

   PA23 TTH4 RRII DDAA = Analysis complete if no previous error messages occurred. Diskette good.

   Where:
   TT = last cylinder (track) accessed
   H = last head accessed = 0 = head 0; 1 = head 1
   RR = first sector with error
   II = number of ID errors
   DD = number of data CRC errors
   AA = number of data address mark errors
4. After determining the test results at the PA23 message, enter either a begin (B) or a free (F) function.
   - A begin function continues the test on the next specified cylinder if the last character of the PA23 message is not a 4. If it is, the test terminates.
   - A free function terminates the routine.

Routine 30, Head Alignment Setup. This selectable-only routine aids in performing head alignment by moving the head/carriage assembly to either cylinder 39 or 40 as indicated by the following manual intervention stops:

PA41 = Head positioned at cylinder 40

PA42 = Head positioned at cylinder 39

PA43 = Head positioned at cylinder 40

To select and run this routine, load MD diskette 03, specify the Free-Lance Utility, and select Routine 29 (see DA200). At each stop, enter either a begin (B) or free (F) function.

- A begin function continues to the next stop. If entered at PA43, the head/carriage returns to cylinder 39 and the routine indicates stop PA42.
- A free function terminates the routine.

Routine 31, Head Alignment Verification. This selectable-only routine, which requires head alignment diskette PN 2455026 (obtainable at the Branch Office), reads certain tracks to verify proper head alignment. Two manual intervention stops occur; PA31 permits you to read either one or four tracks, while PA33 indicates the test results.

Routine 31 Description. The routine initially generates the PA31 stop. This allows insertion of the head alignment diskette and selection of either one track from 6 to 9 or all tracks 6 through 9, with track 6 as the default value. The routine then moves the head/carriage assembly to track 0 and reads the volume ID label to ensure that only an alignment diskette is loaded.

After ID verification, the routine moves the head/carriage to the first track specified at the PA31 stop. There, it attempts to read all records on the track. If the PA31 option value specified more than one track, the routine next moves the head/carriage to tracks 7, 8, and 9, and repeats the read, verify, and save sequence at each track.

When the routine reads the last (or only) track specified at PA31, the PA33 stop indicates the test results.

Routine 31 Selection and Operation. You can do a diskette drive head alignment check by using either a DA MAP option or the Free-Lance Utility. Proceed in order as follows:

1. Load MD diskette 03 and either:
   a. Select the DA MAP and use MAP menu option E, or
   b. Use the Free-Lance Utility and select Routine 31 (see DA200). You can use the loop option if necessary.
2. At the PA31 stop, insert and load the head alignment diskette (PN 2455026) and enter either of the following:

   1XB = Read only one track, where X = 6, 7, 8, or 9. If x is not specified, the routine uses track 6.

   2B = Read all tracks 6 through 9.
3. At the PA33 stop, examine the test results as indicated below:

   PA33 XX00 = Test completed using only one track, where:
   XX = decimal number of record pairs read correctly on that track.

   PA33 AABB CCDD = Test completed using four tracks, where:
   AA = decimal number of record pairs read correctly on track 6.
   BB = decimal number of record pairs read correctly on track 7.
   CC = decimal number of record pairs read correctly on track 8.
   DD = decimal number of record pairs read correctly on track 9.

   Note: *The routine should read more than two record pairs on each track if the head alignment is correct and, since the alignment diskette is formatted in 128-byte FM mode, can only read a maximum of 13 pairs.*
4. Enter B to terminate the routine.

DA230 Test Message Formats and Status Information

DA231 Offline Test Messages

The following messages can be generated while running the offline diskette storage tests:

PA00 = Diskette storage tests completed successfully.

PAF0 = Diskette storage tests are running.

PA01 = Diskette label specifies write protection.

Note: *If you enter B, a write operation occurs and the test continues.*

PA11 = Open the diskette drive cover to continue testing.

Note: *This is an error indication if the test does not continue after opening the cover.*

PA12 = Close the diskette drive cover to continue testing.

Note: *This is an error indication if the test does not continue after closing the cover.*

PA80 = I/O operation did not complete.

XXBC = The TCM detected a system error. (See ST420 for XXBC message descriptions.)

PAXE = Test error message.

Note: *When entering a PAXE RREN value into the MD for DA MAP menu option C, enter as PAXERREN (no space).*

The diskette storage PAXE message has two formats:

Format 1 = PAXE RREN
Format 2 = PAXE RREN BSES DSFS

Where:

PA = Diskette storage physical address (see DA112 and DA113)
X = Level = 1
E = Error occurred
RR = Failing routine number from 01 through 31
EN = Error number that defines the error type (see DA240)
BS = Basic status information (see DA233)
ES = Extended status information (see DA233)
DS = Diagnostic sense byte information (see DA233)
FS = Drive sense byte information (see DA233)

DA232 Selectable Routine Manual Intervention Stops

The following describes the manual intervention stops that can be generated while running selectable Routines 29, 30, and 31:

Routine 29 Surface Analysis

PA21 = You can either change diskettes or use the one already loaded. Enter a four-digit number that specifies the first and last decimal cylinder numbers to be tested. Enter the same number twice for only one cylinder. The routine converts these values to binary.

PA23 TTH0 RRII DDAA = Recoverable diskette media errors. Information only. If the system error log indicates a large number of recoverable (soft) errors, this stop assists you to locate the diskette that caused them.

PA23 TTH1 0000 0000 = Unrecoverable seek error. Could not locate cylinder. Diskette is defective.

PA23 TTH1 RRII DDAA = Unrecoverable ID failure. Unable to read the ID of the sector specified by the RR field successfully in ten attempts. Diskette is defective.

PA23 TTH2 RRII DDAA = Unrecoverable data CRC failure. Unable to read the sector specified by the RR field successfully in ten attempts. Diskette is defective.

Note: *Flagged defective sectors are ignored.*

PA23 TTH3 RRII DDAA = Unable to read the sector specified by the RR field successfully in ten attempts. The first error found was either a missing or undetected data address mark (overrun). Diskette is defective.

PA23 TTH4 = Analysis complete if no previous error messages occurred. Diskette is good.

Where:

TT = last cylinder (track) accessed
H = last head accessed = 0 = head 0; 1 = head 1
RR = first sector with error
II = number of ID errors
DD = number of data CRC errors
AA = number of data address mark errors

Routine 30 Head Alignment Setup

PA41 = Head positioned at cylinder 40

PA42 = Head positioned at cylinder 39

PA43 = Head positioned at cylinder 40

Routine 31 Verify Head Alignment

PA31 = Insert and load the head alignment diskette (PN 2455026) and enter either of the following:

1XB = Read only one track, where X = 6, 7, 8, or 9. If X is not specified, the routine uses track 6.

2B = Read all tracks 6 through 9.

PA33 XX00 = Test completed using only one track, where:

XX = decimal number of record pairs read correctly on that track.

PA33 AABB CCDD = Test completed using four tracks, where:

AA = decimal number of record pairs read correctly on track 6.
BB = decimal number of record pairs read correctly on track 7.
CC = decimal number of record pairs read correctly on track 8.
DD = decimal number of record pairs read correctly on track 9.

DA233 Status and Sense Byte Formats

The diskette adapter generates four bytes of status and sense information: basic status, extended status, drive sense, and diagnostic sense. Each bit or bit group of these four bytes defines a particular condition or operation as described in the following paragraphs.

The status and sense bytes in the test error message (DA231) and system error log (DA330) are in hex; therefore, you must convert these hex values to binary for their meaning.

Basic Status Byte Information

Bit	0	1	2	3	4	5	6	7
Meaning	Error Status		OP Status			Machine Check	Enable	Interrupt

Bits 0,1 Error Status

00 = No Error

01 = CRC Error. The CRC byte that was read after the last record did not compare to the CRC generated.

10 = Command Reject. Either the adapter decoded an invalid command, or a command other that Reset Adapter, Read Basic Status, or Read Tests Sense was decoded with an operational status of busy (011).

11 = Hardware Error. Set when either bit 0 or bit 1 of the extended status is set.

Bits 2–4 Operational Status

000 = Op Complete. Normal completion.

001 = Control Complete. A control record was read during a read sector operation.

010 = Drive Error. The diskette drive Erase/Write Current Sense line, which should be off when reading and on when writing, was at the wrong level.

011 = Busy. Adapter/drive operation occurring.

100 = Overrun/Underrun. Either the adapter did not receive sufficient processor time for a CHIO operation or the diskette was formatted incorrectly.

101 = Timeout. A diskette read or write operation did not complete within 26 revolutions.

110 = Record Not Found. Either the record number that was read from the ID field did not compare to the value in the record number compare register or a CRC error occurred for an ID field.

111 = Not Ready. The diskette drive is not generating the correct number of (or any) index pulses.

Bit 5 Machine Check. The diskette adapter detected a processor halt caused either by (1) an invalid command, (2) incorrect parity when either the command tag (TC) or data tag (TD) was active, or (3) the processor receiving incorrect parity during data transfer.

Bit 6 Enable. Permits the diskette adapter to send I/O interrupt signals to the processor. A Set Basic Status command turns this bit on.

Bit 7 Interrupt. The adapter sensed an interrupt condition.

Extended Status Byte Information

Bit	0	1	2	3	4	5	6	7
Meaning	Processor Parity Error	Adapter Parity Error	Record Count/Seek Count					Not Used

Bit 0 Processor Parity Error. The diskette adapter sensed a parity error from the processor.

Bit 1 Adapter Parity Error. The diskette adapter sensed a parity error within its internal data flow.

Bits 2–6 Record Count/Seek Count. Indicates the number of sectors not transferred.

Bit 7 Not used

Drive Sense Byte Information

Bit	0	1	2	3	4	5	6	7
Meaning	Not Used				Diskette Type	Not Used	Head Select	Not Used

Bits 0–3 Not Used

Bit 4 Diskette Type

0 = Two-sided diskette
1 = One-sided diskette

Bit 5 Not Used

Bit 6 Head Select for Read/Write Operations

0 = Use head 1
1 = Use head 0

Bit 7 Not Used

Diagnostic Sense Byte Information

Bit	0	1	2	3	4	5	6	7
Meaning	FM/MFM	Record Length		Operation Bus Command Code				

Bit 0 FM/MFM Encoding

0 = MFM
1 = FM

Bits 1, 2 Record Length (Mode)

00 = 128-byte record
01 = 256-byte record
10 = 512-byte record
11 = 1024-byte record

Bits 3–7 Operation Bus Command Code

00000 = idle
00001 = read ID next
00010 = format
00011 = not used
00100 = write record
00101 = read record
00110 = read back check
00111 = read ID
01000 = select head 1
01001 = select head 0
01010 = seek to cylinder range 0–41, select head 1
01011 = seek to cylinder range 0–41, select head 0
01100 = seek to cylinder range 42–59, select head 1
01101 = seek to cylinder range 42–59, select head 0
01110 = seek to cylinder range 60–76, select head 1
01111 = seek to cylinder range 60–76, select head 0
10000 = write buffer A, odd parity
10001 = read buffer A, odd parity
10010 = write buffer A, even parity
10011 = read buffer A, even parity
10100 = write buffer B, odd parity
10101 = read buffer B, odd parity
10110 = write buffer B, even parity
10111 = read buffer B, even parity
11000 = diagnostic write access
11001 = diagnostic read access
11010 = diagnostic head load
11011 = not used
11100 = diagnostic special output
11101 = not used
11110 = not used
11111 = read drive sense

DA240 Test Error Messages, Descriptions, and Failure Types

All offline diskette storage test error messages use the PAXE RREN format. The following chart shows the routine number (RR) and error number (EN) values for diskette storage failures, and also describes the error meaning and failure type. DA231 lists the message formats and their byte meanings.

To further analyze failures, the RREN format 2 messages have additional status and sense information. DA233 describes the meaning of the format 2 status and sense information.

RREN	Format	Description	Failure Type
0101	1	PIO machine check	Adapter/bus
0107	2	Incorrect basic status	Diskette storage
0121	2	Status field not reset by Reset Adapter command	Diskette storage
0201	1	PIO machine check	Adapter/bus
0207	2	Incorrect basic status	Diskette storage
021A	2	Incorrect extended status	Diskette storage
021C	2	Incorrect diagnostic sense byte	Diskette storage
021D	2	Incorrect read/write test data	Diskette storage
0226	1	Interrupt received on wrong level	Adapter/bus
0227	1	Interrupt received on multiple levels	Adapter/bus
0228	1	Incorrect IOIRV value	Adapter/bus
0301	1	PIO machine check	Adapter/bus
0302	1	Expected machine check did not occur	Adapter/bus
0303	1	Incorrect machine check status	Adapter/bus
0307	2	Incorrect basic status	Diskette storage
0401	1	PIO machine check	Adapter/bus
0407	2	Incorrect basic status	Diskette storage
0425	1	Incorrect pointer number read back	Adapter
0501	1	PIO machine check	Adapter/bus
0502	1	Expected machine check did not occur	Adapter/bus
0506	1	No interrupt after I/O request	Seek
0507	2	Incorrect basic status	Diskette storage
050B	1	Channel I/O machine check	Adapter/bus
050C	1	Device not ready	Not ready
0519	1	Data read not equal to data written	Read/write
051A	2	Incorrect extended status	Diskette storage
051E	2	Incorrect channel pointer value	Diskette storage
053F	1	Error in modifier operation	Adapter/bus
0601	1	PIO machine check	Adapter/bus
0606	1	No interrupt after I/O request	Seek
0607	2	Incorrect basic status	Diskette storage
060B	1	Channel I/O machine check	Adapter/bus
060C	1	Device not ready	Not ready
060D	1	CRC error on ID	Seek
0610	1	Unrecoverable seek error	Seek
0613	2	Incorrect basic status after read ID	Diskette storage
061E	2	Incorrect channel pointer value	Diskette storage
0701	1	PIO machine check	Adapter/bus
0706	1	No interrupt after I/O request	Seek
0707	2	Incorrect basic status	Diskette storage
070A	2	Incorrect basic status after read	Diskette storage
070B	1	Channel I/O machine check	Adapter/bus
070C	1	Device not ready	Not ready
070D	1	CRC error on ID	Seek
0710	1	Unrecoverable seek error	Seek
0711	1	CRC error on cylinder 0	Seek
0713	2	Incorrect basic status after read ID	Diskette storage
071E	2	Incorrect channel pointer value	Diskette storage

RREN	Format	Description	Failure Type
0801	1	PIO machine check	Adapter/bus
0806	1	No interrupt after I/O request	Seek
0807	2	Incorrect basic status	Diskette storage
080A	2	Incorrect basic status after read	Diskette storage
080B	1	Channel I/O machine check	Adapter/bus
080C	1	Device not ready	Not ready
080D	1	CRC error on ID	Seek
0810	1	Unrecoverable seek error	Seek
0811	1	CRC error on cylinder 0	Seek
0813	2	Incorrect basic status after read ID	Diskette storage
081F	1	CHIO error on multisector operation	Read/write
0901	1	PIO machine check	Adapter/bus
0906	1	No interrupt after I/O request	Seek
0907	2	Incorrect basic status	Diskette storage
090A	2	Incorrect basic status after read	Diskette storage
090B	1	Channel I/O machine check	Adapter/bus
090C	1	Device not ready	Not ready
090D	1	CRC error on ID	Seek
0910	1	Unrecoverable seek error	Seek
0911	1	CRC error on cylinder 0	Seek
0913	2	Incorrect basic status after read ID	Diskette storage
091E	2	Incorrect channel pointer value	Diskette storage
0931	1	Diskette revolving too fast	Drive speed
0932	1	Diskette revolving too slow	Drive speed
1001	1	PIO machine check	Adapter/bus
1006	1	No interrupt after I/O request	Seek
1007	2	Incorrect basic status	Diskette storage
100A	2	Incorrect basic status after read	Diskette storage
100B	1	Channel I/O machine check	Adapter/bus
100C	1	Device not ready	Not ready
100D	1	CRC error on ID	Seek
1010	1	Unrecoverable seek error	Seek
1011	1	CRC error on cylinder 0	Seek
1013	2	Incorrect basic status after read ID	Diskette storage
101E	2	Incorrect channel pointer value	Diskette storage
1033	1	Seek tests error	Seek
1050	1	More than two bad cylinders on diskette	Diskette
1101	1	PIO machine check	Adapter/bus
1106	1	No interrupt after I/O request	Seek
1107	2	Incorrect basic status	Diskette storage
1108	2	Incorrect drive sense status	Diskette storage
110A	2	Incorrect basic status after read	Diskette storage
110B	1	Channel I/O machine check	Adapter/bus
110C	1	Device not ready	Not ready
110D	1	CRC error on ID	Seek
1110	1	Unrecoverable seek error	Seek
1111	1	CRC error on cylinder 0	Seek
1113	2	Incorrect channel pointer value	Diskette storage
111E	2	Incorrect channel pointer value	Diskette storage

RREN	Format	Description	Failure Type
1201	1	PIO machine check	Adapter/bus
1206	1	No interrupt after I/O request	Seek
1207	2	Incorrect basic status	Diskette storage
1208	2	Incorrect drive sense status	Diskette storage
1209	2	Incorrect basic status after write track	Diskette storage
120A	2	Incorrect basic status after read	Diskette storage
120B	1	Channel I/O machine check	Adapter/bus
120C	1	Device not ready	Not ready
120D	1	CRC error on ID	Seek
1210	1	Unrecoverable seek error	Seek
1211	1	CRC error on cylinder 0	Seek
1213	2	Incorrect basic status after read ID	Diskette storage
1216	1	Unrecoverable CRC error	Seek
121E	2	Incorrect channel pointer value	Diskette storage
1301	1	PIO machine check	Adapter/bus
1306	1	No interrupt after I/O request	Seek
1307	2	Incorrect basic status	Diskette storage
1308	2	Incorrect drive sense status	Diskette storage
1309	2	Incorrect basic status after write track	Diskette storage
130A	2	Incorrect basic status after read	Diskette storage
130B	1	Channel I/O machine check	Adapter/bus
130C	1	Device not ready	Not ready
130D	1	CRC error on ID	Seek
130E	1	CRC error on data	Seek
1310	1	Unrecoverable seek error	Seek
1311	1	CRC error on cylinder 0	Seek
1313	2	Incorrect basic status after read ID	Diskette storage
1314	2	Incorrect basic status after write record	Diskette storage
1316	1	Unrecoverable CRC error	Seek
1319	1	Data read not equal to data written	Read/write
131E	2	Incorrect channel pointer value	Diskette storage
131F	1	CHIO error on multisector operation	Read/write
1401	1	PIO machine check	Adapter/bus
1406	1	No interrupt after I/O request	Seek
1407	2	Incorrect basic status	Diskette storage
1408	2	Incorrect drive sense status	Diskette storage
1409	2	Incorrect basic status after write track	Diskette storage
140A	2	Incorrect basic status after read	Diskette storage
140B	1	Channel I/O machine check	Adapter/bus
140C	1	Device not ready	Not ready
140D	1	CRC error on ID	Seek
140E	1	CRC error on data	Seek
1410	1	Unrecoverable seek error	Seek
1411	1	CRC error on cylinder 0	Seek
1413	2	Incorrect basic status after read ID	Diskette storage
1416	1	Unrecoverable CRC error	Seek
1419	1	Data read not equal to data written	Read/write
141E	2	Incorrect channel pointer value	Diskette storage

RREN	Format	Description	Failure Type
1501	1	PIO machine check	Adapter/bus
1506	1	No interrupt after I/O request	Seek
1507	2	Incorrect basic status	Diskette storage
1508	2	Incorrect drive sense status	Diskette storage
1509	2	Incorrect basic status after write track	Diskette storage
150A	2	Incorrect basic status after read	Diskette storage
150B	1	Channel I/O machine check	Adapter/bus
150C	1	Device not ready	Not ready
150D	1	CRC error on ID	Seek
150E	1	CRC error on data	Seek
1510	1	Unrecoverable seek error	Seek
1511	1	CRC error on cylinder 0	Seek
1513	2	Incorrect basic status after read ID	Diskette storage
1516	1	Unrecoverable CRC error	Seek
1519	1	Data read not equal to data written	Read/write
151E	2	Incorrect channel pointer value	Diskette storage
151F	1	CHIO error on multisector operation	Read/write
1601	1	PIO machine check	Adapter/bus
1606	1	No interrupt after I/O request	Seek
1607	2	Incorrect basic status	Diskette storage
1608	2	Incorrect drive sense status	Diskette storage
1609	2	Incorrect basic status after write track	Diskette storage
160A	2	Incorrect basic status after read	Diskette storage
160B	1	Channel I/O machine check	Adapter/bus
160C	1	Device not ready	Not ready
160D	1	CRC error on ID	Seek
160E	1	CRC error on data	Seek
1610	1	Unrecoverable seek error	Seek
1611	1	CRC error on cylinder 0	Seek
1613	2	Incorrect basic status after read ID	Diskette storage
1616	1	Unrecoverable CRC error	Seek
1619	1	Data read not equal to data written	Read/write
161E	2	Incorrect channel pointer value	Diskette storage
1701	1	PIO machine check	Adapter/bus
1706	1	No interrupt after I/O request	Seek
1707	2	Incorrect basic status	Diskette storage
1708	2	Incorrect drive sense status	Diskette storage
1709	2	Incorrect basic status after write track	Diskette storage
170A	2	Incorrect basic status after read	Diskette storage
170B	1	Channel I/O machine check	Adapter/bus
170C	1	Device not ready	Not ready
170D	1	CRC error on ID	Seek
170E	1	CRC error on data	Seek
1710	1	Unrecoverable seek error	Seek
1711	1	CRC error on cylinder 0	Seek
1713	2	Incorrect basic status after read ID	Diskette storage
1714	2	Incorrect basic status after write record	Diskette storage
1716	1	Unrecoverable CRC error	Seek
1719	1	Data read not equal to data written	Read/write
171E	2	Incorrect channel pointer value	Diskette storage
171F	1	CHIO error on multisector operation	Read/write

RREN	Format	Description	Failure Type
1801	1	PIO machine check	Adapter/bus
1806	1	No interrupt after I/O request	Seek
1807	2	Incorrect basic status	Diskette storage
1808	2	Incorrect drive sense status	Diskette storage
1809	2	Incorrect basic status after write track	Diskette storage
180A	2	Incorrect basic status after read	Diskette storage
180B	1	Channel I/O machine check	Adapter/bus
180C	1	Device not ready	Not ready
180D	1	CRC error on ID	Seek
180E	1	CRC error on data	Seek
1810	1	Unrecoverable seek error	Seek
1811	1	CRC error on cylinder 0	Seek
1813	2	Incorrect basic status after read ID	Diskette storage
1814	2	Incorrect basic status after write record	Diskette storage
1816	1	Unrecoverable CRC error	Seek
1819	1	Data read not equal to data written	Read/write
181E	2	Incorrect channel pointer value	Diskette storage
1901	1	PIO machine check	Adapter/bus
1906	1	No interrupt after I/O request	Seek
1907	2	Incorrect basic status	Diskette storage
1908	2	Incorrect drive sense status	Diskette storage
1909	2	Incorrect basic status after write track	Diskette storage
190A	2	Incorrect basic status after read	Diskette storage
190B	1	Channel I/O machine check	Adapter/bus
190C	1	Device not ready	Not ready
190D	1	CRC error on ID	Seek
190E	1	CRC error on data	Seek
1910	1	Unrecoverable seek error	Seek
1911	1	CRC error on cylinder 0	Seek
1913	2	Incorrect basic status after read ID	Diskette storage
1914	2	Incorrect basic status after write record	Diskette storage
1916	1	Unrecoverable CRC error	Seek
1919	1	Data read not equal to data written	Read/write
191E	2	Incorrect channel pointer value	Diskette storage
191F	1	CHIO error on multisector operation	Read/write
2001	1	PIO machine check	Adapter/bus
2006	1	No interrupt after I/O request	Seek
2007	2	Incorrect basic status	Diskette storage
2008	2	Incorrect drive sense status	Diskette storage
2009	2	Incorrect basic status after write track	Diskette storage
200A	2	Incorrect basic status after read	Diskette storage
200B	1	Channel I/O machine check	Adapter/bus
200C	1	Device not ready	Not ready
200D	1	CRC error on ID	Seek
200E	1	CRC error on data	Seek
2010	1	Unrecoverable seek error	Seek
2011	1	CRC error on cylinder 0	Seek
2013	2	Incorrect basic status after read ID	Diskette storage
2014	2	Incorrect basic status after write record	Diskette storage
2016	1	Unrecoverable CRC error	Seek
2019	1	Data read not equal to data written	Read/write
201E	2	Incorrect channel pointer value	Diskette storage

RREN	Format	Description	Failure Type
2101	1	PIO machine check	Adapter/bus
2106	1	No interrupt after I/O request	Seek
2107	2	Incorrect basic status	Diskette storage
2108	2	Incorrect drive sense status	Diskette storage
2109	2	Incorrect basic status after write track	Diskette storage
210A	2	Incorrect basic status after read	Diskette storage
210B	1	Channel I/O machine check	Adapter/bus
210C	1	Device not ready	Not ready
210D	1	CRC error on ID	Seek
210E	1	CRC error on data	Seek
2110	1	Unrecoverable seek error	Seek
2111	1	CRC error on cylinder 0	Seek
2113	2	Incorrect basic status after read ID	Diskette storage
2114	2	Incorrect basic status after write record	Diskette storage
2116	1	Unrecoverable CRC error	Seek
2119	1	Data read not equal to data written	Read/write
211E	2	Incorrect channel pointer value	Diskette storage
211F	1	CHIO error on multisector operation	Read/write
2201	1	PIO machine check	Adapter/bus
2206	1	No interrupt after I/O request	Seek
2207	2	Incorrect basic status	Diskette storage
2208	2	Incorrect drive sense status	Diskette storage
2209	2	Incorrect basic status after write track	Diskette storage
220A	2	Incorrect basic status after read	Diskette storage
220B	1	Channel I/O machine check	Adapter/bus
220C	1	Device not ready	Not ready
220D	1	CRC error on ID	Seek
220E	1	CRC error on data	Seek
2210	1	Unrecoverable seek error	Seek
2211	1	CRC error on cylinder 0	Seek
2213	2	Incorrect basic status after read ID	Diskette storage
2214	2	Incorrect basic status after write record	Diskette storage
2216	1	Unrecoverable CRC error	Seek
2219	1	Data read not equal to data written	Read/write
221E	2	Incorrect channel pointer value	Diskette storage
2301	1	PIO machine check	Adapter/bus
2306	1	No interrupt after I/O request	Seek
2307	2	Incorrect basic status	Diskette storage
2308	2	Incorrect drive sense status	Diskette storage
2309	2	Incorrect basic status after write track	Diskette storage
230A	2	Incorrect basic status after read	Diskette storage
230B	1	Channel I/O machine check	Adapter/bus
230C	1	Device not ready	Not ready
230D	1	CRC error on ID	Seek
230E	1	CRC error on data	Seek
2310	1	Unrecoverable seek error	Seek
2311	1	CRC error on cylinder 0	Seek
2313	2	Incorrect basic status after read ID	Diskette storage
2314	2	Incorrect basic status after write record	Diskette storage
2316	1	Unrecoverable CRC error	Seek
2319	1	Data read not equal to data written	Read/write
231E	2	Incorrect channel pointer value	Diskette storage
231F	1	CHIO error on multisector operation	Read/write

RREN	Format	Description	Failure Type
2501	1	PIO machine check	Adapter/bus
2506	1	No interrupt after I/O request	Seek
2507	2	Incorrect basic status	Diskette storage
2508	2	Incorrect drive sense status	Diskette storage
2509	2	Incorrect basic status after write track	Diskette storage
250A	2	Incorrect basic status after read	Diskette storage
250B	1	Channel I/O machine check	Adapter/bus
250C	1	Device not ready	Not ready
250D	1	CRC error on ID	Seek
250E	1	CRC error on data	Seek
2510	1	Unrecoverable seek error	Seek
2511	1	CRC error on cylinder 0	Seek
2513	2	Incorrect basic status after read ID	Diskette storage
2514	2	Incorrect basic status after write record	Diskette storage
2516	1	Unrecoverable CRC error	Seek
2519	1	Data read not equal to data written	Read/write
251E	2	Incorrect channel pointer value	Diskette storage
2537	1	Expected overrun not received	Adapter
2601	1	PIO machine check	Adapter/bus
2606	1	No interrupt after I/O request	Seek
2607	2	Incorrect basic status	Diskette storage
2608	2	Incorrect drive sense status	Diskette storage
2609	2	Incorrect basic status after write track	Diskette storage
260A	2	Incorrect basic status after read	Diskette storage
260B	1	Channel I/O machine check	Adapter/bus
260C	1	Device not ready	Not ready
260D	1	CRC error on ID	Seek
260E	1	CRC error on data	Seek
2610	1	Unrecoverable seek error	Seek
2611	1	CRC error on cylinder 0	Seek
2613	2	Incorrect basic status after read ID	Diskette storage
2614	2	Incorrect basic status after write record	Diskette storage
2616	1	Unrecoverable CRC error	Seek
261E	2	Incorrect channel pointer value	Diskette storage
2701	1	PIO machine check	Adapter/bus
2707	2	Incorrect basic status	Diskette storage
270C	1	Device not ready	Not ready
2710	1	Unrecoverable seek error	Seek
2711	1	CRC error on cylinder 0	Seek
2801	1	PIO machine check	Adapter/bus
280C	1	Device not ready	Not ready
2810	1	Unrecoverable seek error	Seek
2811	1	CRC error on cylinder 0	Seek
2901	1	PIO machine check	Adapter/bus
290C	1	Device not ready	Not ready
2910	1	Unrecoverable seek error	Seek
2911	1	CRC error on cylinder 0	Seek
291B	1	Incorrect entry for MI test stop	Operator
3001	1	PIO machine check	Adapter/bus
300C	1	Device not ready	Not ready
3010	1	Unrecoverable seek error	Seek
3011	1	CRC error on cylinder 0	Seek
3101	1	PIO machine check	Adapter/bus
310C	1	Device not ready	Not ready
3110	1	Unrecoverable seek error	Seek
3111	1	CRC error on cylinder 0	Seek
311B	1	Incorrect entry for MI test stop	Operator
3139	1	Head alignment diskette not loaded	Operator

DA250 Diskette Storage Action Plans

You are using this section because either the DA MAP sent you here or the error is too intermittent to use the MAP.

Note: *If the DA MAP sent you to this section to use an action plan, you can verify a repair action by pressing FWD on the MD to run the tests.*

This section provides action plans for failures detected by the diskette storage tests. Either the EN (error number) portion of the test error message (DA240) or the basic status associated with the message (DA233) categorizes these failures.

The following summarizes the diskette storage failure types and their corresponding action plan sections. To use this section, determine the failure type from the test error message in DA240 and go the action plan section as indicated below:

Note: *If an Operator failure type occurs, perform the action indicated by the test error message description; if a Diskette failure type occurs, exchange the diskette.*

Failure Type	Section
Adapter/bus	DA251
Adapter	DA252
Diskette storage	DA253
Not ready	DA254
Seek	DA255
Read/write	DA256
Drive speed	DA257
Erase/write	DA258

Error Message	Failure Type	Section
XXBC	Adapter/bus	DA251
PA80	Adapter/bus	DA251
PA11	MI status error*	DA253
PA12	MI status error*	DA253

*PA11 and PA12 are error indications if the test does not continue after performing the MI stop procedure.

When using DA251 through DA258, refer to Figure DA250-1 to determine the diskette adapter card locations for all 8100 machine types and models.

Machine Type	Model	DA1	DA2
8130	A2X	A1S2	A1R2
8140	A3X/A4X	A2M2	A2N2
8140	A5X, A6X, A7X	A2G2	A2H2
8140	B5X, B6X, B7X	B2C2	B2B2
8101	A1X, A2X	A2G2	A2F2

Figure DA250-1. Diskette Adapter Card Locations

DA251 Adapter/Bus Failure Action Plan

You are using this action plan because a test failure occurred while using only the adapter and adapter bus and not the diskette drive. Proceed as follows:

1. Measure the dc voltage at the following pins on the board that contains the diskette adapter (see DA111 for board location):
   a. D03 +4.5 to +5.5V
   b. B11 +7.7 to +9.3V
   c. B06 -4.5 to -5.5V

   If any are either missing or out of tolerance, go to the PA MAP.
2. Exchange both the DA1 and DA2 diskette adapter cards. See Figure DA250-1 for locations.
3. Exchange the SCF card associated with the diskette adapter.
   - 01A-A2G2 (SC1) for an 8130 without the System Expansion Feature.
   - 01A-A2C2 (SC5) for an 8130 with the System Expansion Feature.
   - 01A-A2D2 (SC5) for 8140 Models A3X-A7X.
   - 01A-A2A2 (SC5) for 8140 Models B5X—B7X and for all 8101s.
4. Check the adapter logic continuity (DA410). Correct if necessary.
5. Test all adapters having the same group address (the same P value of the adapter PA) as the diskette adapter. Exchange any failing adapter card.
6. Do one of the following:
   - For a 92BC test error message, return to the Chapter 1 GFI action plan that directed you here and continue with the next step.
   - For a PA1E 053F test error message, go to SC250 Action Plan 07 (vol 4).
   - For all other test error messages, request aid.

DA252 Diskette Adapter Failure Action Plan

You are using this action plan because a test failure occurred while using the adapter. The failing operation was not related to either the diskette drive or the adapter bus. Proceed as follows:

1. Measure the dc voltage at the following pins on the board that contains the diskette adapter (see DA111 for board locations):
   a. D03 = +4.5 to +5.5V
   b. B11 = +7.7 to +9.3V
   c. B06 = -4.5 to -5.5V

   If any are either missing or out of tolerance, go to the PA MAP.
2. Exchange both the DA1 and DA2 diskette adapter cards. See Figure DA250-1 for locations.
3. Check the adapter logic continuity (DA410). Correct if necessary.
4. Request aid.

DA253 Diskette Storage Status Failure Action Plan

You are using this action plan because either a PA11 or PA12 manual intervention stop failed or the diskette adapter basic status was incorrect.

- If a PA11 or PA12 failure occurred, use the action plan below.
- If the diskette adapter basic status was incorrect, obtain this status from the test error message (see DA231) and convert it to binary.
  - If the status indicates either bit 0 or 5 active, use the action plan in DA251.
  - If the status indicates bit 1 active, use the action plan in DA255.
  - If 0, 1, and 5 are not active, use bits 2, 3, and 4 to determine the action plan section as follows:

Bits 2 3 4	Failure Type	Section
0 0 0	Diskette storage	DA253
0 0 1	Seek	DA255
0 1 0	Erase/write	DA258
0 1 1	Diskette storage	DA253
1 0 0	Diskette storage	DA253
1 0 1	Diskette storage	DA253
1 1 0	Seek	DA255
1 1 1	Not ready	DA254

For this action plan, proceed as follows:

1. If the diskette basic status bits 2, 3, and 4 value was 100, the diskette could be improperly formatted. Try another diskette. If the bit value was not 100, go to step 2.
2. Exchange both the DA1 and DA2 diskette adapter cards. See Figure DA250-1 for locations.
3. Exchange the DA3 (diskette drive control) card (DA670).
4. Check the adapter logic continuity (DA410). Correct if necessary.
5. Request aid.

DA254 Not Ready Failure Action Plan

You are using this action plan because a failure occurred in the diskette drive index logic. The diskette drive control card should generate an index pulse each time the diskette index hole passes between the phototransistor (PTX) and the light emitting diode (LED). The adapter then determines diskette rotation and speed by checking the pulse timing, and, if correct, indicates a ready condition.

Observe if the diskette turns and proceed in order with the appropriate action plan as follows:

Diskette Not Turning

1. Drive cover not closed properly:
   a. Check for obstructions. Remove or correct the cause.
   b. Check the cover latch operation. Replace if defective (DA530).
   c. Exchange the cover assembly (DA520).
   d. Request aid.
2. Drive motor not turning:
   a. Check the ac drive motor voltage. If missing, go to the PA MAP.
   b. Remove the drive belt and check for binds in the drive hub pulley and the drive belt idler assembly.
      - If the idler binds, replace it (DA590).
      - If the pulley binds, exchange the diskette drive assembly (DA515).
   c. Exchange the diskette drive motor (DA580).
   d. Request aid.
3. Drive motor turning:
   a. Check the drive belt. Replace if defective (DA570).
   b. Check the drive motor pulley. Tighten or replace if defective (DA580).
   c. Remove the drive belt and check for binds in the drive hub pulley and the drive belt idler assembly.
      - If the idler binds, replace it (DA590).
      - If the pulley binds, exchange the diskette drive assembly (DA515).
   d. Request aid.

Diskette Is Turning

1. Check the diskette for damage, such as an enlarged drive hole, multiple index holes, or a torn cover. Exchange if damaged.
2. Check for loose or defective cables and connectors used by the diskette drive (DA111 and DA420).
3. Exchange both the DA1 and DA2 adapter cards. See Figure DA250-1 for locations.
4. Exchange the DA3 (diskette drive control) card (DA670).
5. Perform the LED output service check (DA652). Replace if out of tolerance.
6. Perform the phototransistor amplifier service check (DA661). Replace if out of tolerance.
7. Check the LED and phototransistor alignment (DA651). Adjust if necessary.
8. Perform the solenoid and bail service check (DA561). Adjust or replace as necessary.
9. Perform the drive belt tracking service check (DA571). Correct if necessary.
10. Check the drive motor ac voltage (DA700). If not within tolerance, go the PA MAP.
11. Check the continuity of the +Index signal (see Figure 420-1). Correct if necessary.
12. Exchange the drive motor (DA580).
13. Request aid.

DA255 Seek Failure Action Plan

You are using this action plan because a failure occurred in the diskette drive seek logic. The diskette adapter generates access pulses to the diskette drive control card, which should move the head/carriage assembly to the selected track. The seek operation then reads the track ID to determine the location of the head/carriage. Any error that occurs during this operation is considered a seek failure. Proceed as follows:

1. Exchange the diskette with a known good diskette.
2. Check the head/carriage assembly as follows:
   a. Check the stepper motor adjustment (DA602). Correct if necessary.
   b. Check the stepper motor for binds. Replace if defective (DA601/DA602).
   c. Check the stepper motor drive band. Adjust or replace as necessary (DA620).
   d. Check the drive band idler for binds. Replace if defective (DA630).
3. Check for 24V dc at the DA3 (diskette drive control) card test point TPA8 (see Figure DA420-2). If missing, check the 24V logic signal (see Figure DA420-1). If no trouble found, go to the PA MAP.
4. Exchange both the DA1 and DA2 adapter cards. See Figure DA250-1 for locations.
5. Exchange the DA3 (diskette drive control) card (DA670).
6. Perform the solenoid and bail service check (DA561). Adjust or replace as necessary.
7. Check the drive belt tracking (DA571). Adjust or replace as necessary.
8. Perform the drive band service check (DA621). Adjust or replace as necessary.
9. Check the read and write signal continuity (DA423/DA424). Correct if necessary.
10. Perform the head/carriage service check (DA551). Adjust if necessary.
11. Exchange the head/carriage assembly (DA550).
12. Request aid.

DA256 Read/Write Failure Action Plan

You are using this action plan because the diskette drive read/write logic failed after reading the track ID correctly. Either a CRC error occurred after reading the data, or the data that was read did not compare to the data written. Proceed as follows:

1. Exchange the diskette with a known good diskette.
2. Exchange both the DA1 and DA2 diskette adapter cards. See Figure DA250-1 for locations.
3. Exchange the DA3 (diskette drive control) card (DA670).
4. Perform the solenoid and bail service check (DA561). Adjust or replace as necessary.
5. Check the read and write signal continuity (DA423/DA424). Correct if necessary.
6. Perform the head/carriage serivce check (DA551). Adjust if necessary.
7. Exchange the head/carriage assembly (DA550).
8. Request aid.

DA257 Speed Failure Action Plan

You are using this action plan because the diskette rotational speed is not within the 162.5ms to 170.9ms tolerance permitted. For test error message:

- PA1E 0931 (too fast), go to the DA254 Diskette Is Turning action plan.
- PA1E 0932 (too slow), proceed in order as follows:
  1. Ensure that the cover latches properly. Replace the latch if defective (DA530).
  2. Check the drive motor pulley. Tighten or replace if defective (DA580).
  3. Remove the drive belt and check for binds in the drive hub pulley and the drive belt idler assembly.
     - If the idler binds, replace it (DA590).
     - If the pulley binds, exchange the diskette drive assembly (DA515).

4. Go to DA254 and use the Diskette Is Turning action plan.

DA258 Erase/Write Failure Action Plan

You are using this action plan because a failure occurred in the diskette drive erase/write logic. The Erase/Write Current Sense line, which should be off when reading and on when writing, was at the wrong level. Proceed as follows:

1. Exchange the DA3 (diskette drive control) card (DA670).
2. Exchange both the DA1 and DA2 diskette adapter cards. See Figure DA250-1 for locations.
3. Check the erase/erase gate logic continuity (DA422). Correct if necessary.
4. Exchange the head/carriage assembly (DA550).
5. Request aid.

DA300 Intermittent Failure Repair Strategy

Intermittent failures might be detected either by:

- Looping the offline tests with MAP interaction (DA311).
- Examining the system error log (DA311).
- Looping the offline tests without MAP interaction using the Free-Lance Utility (DA313).

DA310 Adapter-Unique Intermittent Repair Strategy

DA311 Looping with MAP Interaction to Determine Failures

After selecting DA MAP offline checkout option A, you can loop the diskette storage tests with MAP interaction by answering yes when the MD displays the prompt message:

```
DO YOU WANT TO CHECK
FOR INTERMITTENT
FAILURE BY LOOPING
DA TEST?          *Y/N
```

If answering yes, the test loops continuously while displaying:

```
PAFO TEST LOOPING
```

on the MD display until either the test detects an error or you terminate the test by entering an F at the MD.

Note: *If the MAP does not detect an error after looping the tests for 5 minutes or the error message varies (more than three different RREN messages), this looping operation is ineffective; use the procedure in DA313.*

If an error occurs while looping, the MAP performs fault isolation the same as it would for a solid failure. After initiating a repair action, you can again loop the tests and use the MAP to verify the repair by pressing FWD on the MD.

DA312 Using the System Error Log to Determine Failures

DPPX and DPCX generate an error log record for any diskette storage failure that occurs during system operation. You can obtain these error log records (see Chapter 2, CP740 or CP830 in volume 1) and use the information (see DA340) to determine the failure types and the action plan used to correct them. If no error log records exist for diskette storage, no diskette storage failure occurred during system operation.

After initiating a repair action, you must use the Free-Lance Utility (Chapter 2, CP462) to loop the tests and verify the repair as follows:

At 80BC enter PAB; at 81BC, enter 11B (see DA200).

If the tests run correctly, have the customer use the system, then obtain another error log and examine it for diskette storage failures.

- If the log indicates the same failure, perform the next action plan step.
- If the log indicates no failures, end the repair action.

DA313 Using the Free-Lance Utility to Determine Failures

You can loop the offline tests without MAP interaction by using the Free-Lance Utility (Chapter 2, CP462) as follows:

At 80BC enter PAB; at 81BC enter 11B (see DA200).

The test loops continuously until either it detects an error or you terminate it by entering an F at the MD.

- If a test error message occurs (displayed at the MD), find the error in DA240 and use the failure type to determine the appropriate action plan in DA250 for fault isolation and repair.
- If no test error message occurs, use the error log procedure in DA312.

After initiating a repair action, you must again use the Free-Lance Utility and loop the tests for at least 5 minutes to verify the repair.

DA320 Error Log Information Used by the DA MAP

To obtain the error log information used by the DA MAP, refer to Chapter 2, either CP740 (DPPX) or CP830 (DPCX) for procedures. Search for the log records of the failing diskette drive by specifying the PA (see DA112).

DA330 Diskette Error Log Formats and Meanings

The DPPX and DPCX operating systems use a different error log format. For the DPPX Error Log, refer to DA331, for the DPCX Condition/Incident Log, refer to DA332.

DA331 DPPX Error Log Format and Meaning

The DPPX operating system generates certain class and subclass error log records according to the failure type (Chapter 2, CP740). The DA MAP uses only the class 5, subclass 1, hardware record (CP748) for fault isolation, and has an option field value of 66 and a DT (device type) field value of G. The following describes the class 5, subclass 1, DPPX error log format and meaning used for diskette storage.

Note: *The 'x' designations indicate the field size in bytes, where 2 x's = one byte.*

RECORD FORMAT

CLASS 05 SUBCLASS 01 OPTION 66

DATE YY.DDD TIME HH/MM/SS

PA xx SCA xxxx DT G

CRC xx COMPSTAT xx ARC xx

DATA xxxxxxxx RES xxxx CNT xxxx

IOEP xxxxxxxx ADWA xxxxxxxx

CA xx CPR xx FRWA xxxxxxxx

RES xxxxxxxx

BCLE xx xx xxxx xxxxxxxx

Extended Data

D01 xxxx D02 xxxx D03 xxxx D04 xxxx

D05 xxxx D06 xxxx D07 xxxx D08 xxxx

D09 xxxx D10 xxxx D11 xxxx D12 xxxx

D13 xxxx D14 xxxx D15 xxxx D16 xxxx

D17 xxxx D18 xxxx

RECORD MEANING

The following describes the meaning of those DPPX error log fields used to analyze diskette storage hardware errors. For a detailed DPPX error log analysis, refer to Chapter 2, CP740.

CLASS	= 5	= Hardware I/O error
SUBCLASS	= 1	= Hardware I/O error
DATE	= YY.DDD	= The year and Julian date of the log output
TIME	= HH/MM/SS	= The hour/minute/second of the log output
PA	= X7	= Diskette storage physical address = 87 = 8130/8140 = 97 = 1st 8101 = A7 = 2nd 8101 = B7 = 3rd 8101 = C7 = 4th 8101
SCA	= 0000	= Not used
DT	= G	= Diskette storage device type
CRC	= xx	= Function module request code (see DA333)
COMPSTAT	= xx	= Completion status (see DA333)
ARC	= xx	= Adapter return code (see DA333)
DATA	= xxxxxxxx	= Data address
RES	= xxxx	= Not used
CNT	= xxxx	= Byte count
IOEP	= xxxxxxxx	= I/O interrupt entry point
ADWA	= xxxxxxxx	= Adapter work area address
CA	= xx	= Channel address
CPR	= xx	= Channel pointer register
FRWA	= xxxxxxxx	= Function request work area address
RES	= xxxxxxxx	= Not used
BCLE	= 8 bytes Byte 0 Byte 1 Byte 2 and 3 Bytes 4–7	= Buffer control list element = Flag byte = Command byte (see DA333) = Count = number of bytes transmitted = Address or data

Extended Data

D01, D02	= xxxxxxxx	= Not used
D03	= xxxx	= First byte = Extended completion code Bit 0 = Not Used Bit 1 = Error record indicator Bit 2 = Program request interrupt Bit 3 = Not used Bit 4 = Not used Bit 5 = Preemptive request complete Bit 6 = Not used Bit 7 = Not used
D04	= xxxx	= Error record displacement
D05, D06	= xxxxxxxx	= BCLE address
D07	= xxxx	= Residual count
D08	= xxxx	= Not used
D09–D12	= 8 bytes	= Function request work area
D13	= xxxx	= First byte = Error records = Second byte = Retry count of failing operation
D14	= xxxx	= First byte = Not used Second byte = Final ARC
D15	= xxxx	= First byte = Basic status (see DA233) Second byte = Extended status (see DA233)
D16	= xxxx	= First byte = Diagnostic sense (see DA233) Second byte = Drive sense (see DA233)
D17, D18	= xxxxxxxx	= Channel pointer register

DA332 DPCX Condition/Incident Log Formats and Meanings

The DPCX operating system generates five types of Condition/Incident Log (CIL) records according to the failure type (Chapter 2, CP840). The DA MAP uses only the type-1 and type-2 CIL records to analyze diskette storage hardware errors. For a detailed DPCX CIL analysis, refer to Chapter 2, CP840.

Note: *The 'x' designations indicate the field size in bytes, where 2 x's = one byte.*

TYPE-1 RECORD FORMAT

1-TYPE I-REC SEQ xxxx NA xx PA xx LA xx

C-CODE xx	B-STAT xx	C-FR xx
X-STAT1 xx	X-STAT2 xx	S-FR xx
IOCB xxxx xxxx	RC xx	

D1 xxxx D2 xxxx D3 xxxx D4 xxxx

TYPE-2 RECORD FORMAT

2-TYPE I-REC SEQ xxxx NA xx PA xx LA xx

D21 xxxx xxxx	LVL xx	C-FR xx
D22 xxxx xxxx	MC xx	S-FR xx

D23 xxxx D24 xxxx D25 xxxx

RECORD MEANING

1-TYPE	=		CIL record type-1
2-TYPE	=		CIL record type-2
I-REC	=		Incident record
SEQ	= xxxx	=	A four-digit decimal value from 0001 to 4095 that identifies the relative time when the record occurred.
NA	= xx	=	Number of applications active when the error occurred.
PA	= xx	=	87 = Diskette storage physical address (8130/8140)
LA	= xx	=	Logical address (same as PA value)
C-CODE	= xx	=	Completion status (see DA333)
B-STAT	= xx	=	Basic status byte (see DA233)
C-FR	= xx	=	Function module request code (see DA333)
X-STAT1	= xx	=	Diagnostic sense byte (see DA233)
X-STAT2	= xx	=	Drive sense byte (see DA233)
S-FR	= xx	=	System function request
IOCB	= xxxxxxxx	=	First two bytes = data address Second two bytes = track and record number
D1	= xxxx	=	First byte = extended status (see DA233)
D2	= xxxx	=	First byte = BCLE command (see DA333)
D3	= xxxx	=	First byte = the retry count
D4	= xxxx	=	First byte = the initial adapter return code Second byte = the final adapter return code after recovery was attempted (see DA333)

MC = System check code

- 1X = Program check
- 2X = Storage parity error
- 4X = I/O timeout
- 8X = I/O bus parity error

DA333 DPPX and DPCX Common Error Log Byte Meanings

Certain fields in the DPPX Error Log and in the DPCX Condition/Incident Log, although named differently, have identical bit or byte meanings. The following paragraphs explain these fields and their meanings, as well as list the field names as used by each operating system.

Adapter Return Code

You can find the DPPX adapter return code in the ARC field and the final DCPX adapter return code after a recovery attempt in the second byte of the D4 field. The following explains their meanings:

00 Normal completion
02 FRB Busy
09 SCA not open
0A Adapter not open
0B SCA already open
11 FRB program check
12 BCL program check
19 Record not found
20 Equipment check
22 Not ready to ready
23 Ready to not ready
29 Overrun/underrun
2A Adapter timeout
2B Seek check
30 SCA not ready
31 Processor parity error
32 Adapter parity error
33 Data CRC error
39 Adapter CRC error
62 SCA not ready
75 CHIO machine check
76 PIO machine check (non-recursive)
F6 PIO machine check (recursive)

BCLE Command Byte

You can find the DPPX BCLE command byte in byte 1 of the BCLE field and the DPCX command byte in the first byte of the D2 field. The following explains their meanings:

00 Transfer Control
01 Read
02 Write Data
07 No-Op
0E Write Control and Verify
1E Write Control
21 Read IPL
22 Write Data and Verify
2E Format
49 Read Sector Attributes
61 Verify
93 Locate
D3 Locate Diskette
E3 Seek

Completion Status

You can find the DPPX completion status in the COMPSTAT field and the DPCX completion status in the C-CODE field. The following explains their meanings:

Bit 0 Extended status indicator
Bit 1 Reenter
Bit 2 Reenter FRB indicator
Bit 3 Not Used
Bit 4 Complete
Bit 5 Error
Bit 6 Exception
Bit 7 Attention

Function Module Request Code

You can find the DPPX function module request code in the CRC field and the DPCX function module request code in the C-FR field. The following explains their meanings:

00 Execute
05 Read Operational Statistics (acts as a No-op FR)
07 No-op
0D Terminate FRB
25 Read SCA Status Immediate
35 Read SCA Status When Ready
83 Open Adapter
87 Diagnose
A3 Open SCA
AB Close SCA
EB Terminate Adapter

DA340 How to Use the Error Log

You can examine the error log records to determine the failures that occurred since the last log reset procedure. As the DPPX and DPCX error log formats are not identical, the procedures for examining them depend on which log you use. For the DPPX Error Log, refer to DA341; for the DPCX Condition/Incident Log, refer to DA342.

DA341 DPPX Error Log

To analyze diskette failures that occurred while running under DPPX, obtain the error log and refer to DA331 for the log format and meaning. The error log PA field (2) specifies the physical address of the diskette adapter and should be either 87, 97, A7, B7, or C7 for DPPX diskette failures.

To use the DPPX error log for diskette fault isolation and repair:

1. Obtain the two hex characters (one byte) of adapter return code information from the ARC field.
2. Obtain the first byte (basic status) from the log extended data field D15.
3. Use the ARC field value and the basic status byte. Go to DA343 to determine the diskette failure type; then go to the action plan section indicated.

DA342 DPCX Condition/Incident Log (CIL)

To analyze diskette failures that occurred while running under DPCX, obtain the CIL and refer to DA332 for the format and meaning. Note that DPCX uses two log record format types (1 and 2) for diskette errors. The error log PA field specifies the physical address of the diskette adapter and should be 87 for DPCX diskette failures.

To use the DPCX CIL for diskette storage fault isolation and repair:

1. Determine if any Type-2 log records occurred for diskette failures, which indicates a machine check. If so, use the action plan in DA351.
2. If no Type-2 log records exist, obtain the B-STAT value and the ARC field value (first byte of the D4 field) from the Type-1 record, go to DA343 to determine the diskette failure type; then go to the action plan section indicated.

DA343 Using the Basic Status Byte and ARC Field to Determine Failures

This procedure uses the error log basic status and ARC field values to determine the diskette failure type and its associated action plan section. Proceed as follows:

1. Use the ARC field value and the table below to determine the diskette failure type, and go to the action plan section indicated.

ARC	Failure Type	Section
19	Record not found	DA354
20	Equipment check	DA352
29*	Overrun/underrun	DA352
2B	Seek check	DA354
31	Processor parity error	DA351
32	Adapter parity error	DA351
33	Data CRC error	DA354
75	CHIO machine check	DA351
76	PIO machine check	DA351
F6	PIO machine check	DA351

*Can occur with incorrect diskette formatting.

2. If the above table does not list the ARC value, use the basic status information obtained in step 2 of either DA341 or DA342 and convert it to binary.
   a. If the status indicates either bit 0 or 5 active, use the action plan in DA351.
   b. If the status indicates bit 1 active, use the action plan in DA354.
   c. If 0, 1, and 5 are not active, use bits 2, 3, and 4 to determine the action plan section as follows:

Bits 2 3 4	Failure Type	Section
0 0 0	Diskette storage	DA352
0 0 1	Seek/read	DA354
0 1 0	Erase/write	DA355
0 1 1	Diskette storage	DA352
1 0 0*	Diskette storage	DA352
1 0 1	Diskette storage	DA352
1 1 0	Seek/read	DA354
1 1 1	Not ready	DA353

*Can occur with incorrect diskette formatting.

DA350 Action Plans to Correct Intermittent Failures

Use this section only after you have obtained the error log and determined the failure type and its associated action plan section either in DA341, DA342, or DA343. Use DA356 for procedures common to all action plans in DA351 through DA355 as noted.

The failure types and their associated action plan sections are:

Failure Type	Section
Machine check	DA351
Diskette storage	DA352
Not ready	DA353
Seek/read	DA354
Erase/write	DA355

DA351 Machine Check Action Plan

You are using this action plan because either:

- A DPCX Type-2 diskette log record occurred, which indicates that the processor detected a hardware error (such as parity) from the diskette adapter, or
- A DPCX Type-1 diskette log record occurred, which indicates that the adapter detected a hardware error on the adapter bus, or
- A DPPX diskette log record occurred, which indicates that a hardware failure occurred on the adapter bus.

Proceed in the following sequence:

Caution: Turn power off when removing or exchanging cards.

Probable Cause	Action	Comment
1. Incorrect board voltage	Measure diskette adapter board voltages (DA111): a. D03 = +4.5 to +5.5V dc b. B11 = +7.7 to +9.3V dc c. B06 = –4.5 to -5.5V dc	If missing or out of tolerance, go to the PA MAP.
2. Loose or defective SCF cable	Inspect for loose or defective cable (DA111 and DA411).	See DA356, procedure 2.
3. Defective diskette adapter cards	Exchange DA1 and DA2.	See DA356, procedures 1, 2, and 3.
4. Defective SCF card	Exchange SCF card SC1 (8130) or SC5 (8130 with System Expansion Feature and all 8140s and 8101s).	See DA356, procedures 1, 2, 3, and 4.

DA352 Diskette Storage Failure Action Plan

You are using this action plan because the error log indicated that a diskette storage status failure occurred. Proceed in the following sequence:

Caution: Turn power off when removing or exchanging cards.

Probable Cause	Action	Comment
1. Incorrect drive voltage	Measure drive voltages (Figure DA420-2): a. TPB15 = +4.5 to +5.5V dc b. TPA8 = +21.6 to +26.4V dc c. TPA9 = –4.5 to -5.5V dc	If missing, check using Figure DA420-1. If out of tolerance, go go to PA MAP.
2. Defective diskette adapter cards	Exchange DA1 and DA2.	See DA356, procedures 1, 2, and 3.
3. Defective diskette drive control card	Exchange DA3 (DA670).	See DA356, procedures 2, 3, and 4.

DA353 Not Ready Action Plan

You are using this action plan because the error log indicated that a failure occurred in the diskette drive index logic. The diskette drive control card should generate an index pulse each time the diskette index hole passes between the phototransistor (PTX) and the light emitting diode (LED). The adapter then determines diskette rotation and speed by checking the pulse timing, and, if correct, indicates a ready condition. Proceed in the following sequence:

Caution: Turn power off when removing or exchanging cards.

Probable Cause	Action	Comment
1. Incorrect ac voltage	Measure ac drive motor voltage (DA700).	If missing or out of tolerance, go to PA MAP.
2. Incorrect drive voltage	Measure drive voltages (Figure DA420-2): a. TPB15 = +4.5 to +5.5V dc b. TPA8 = +21.6 to +26.4V dc c. TAP9 = –4.5 to -5.5V dc	If missing, check using Figure DA420-1. If out of tolerance, go go to PA MAP.
3. Defective diskette adapter and/or diskette drive control cards	Exchange DA1 and DA2. Exchange DA3 (DA670).	See DA356, procedures 1, 2, and 3.
4. Defective or out of adjustment drive component	Perform the following service checks or adjustments: a. Check phototransistor adjustment (DA651). b. Perform phototransistor service check (DA661). c. Perform LED service check (DA652). d. Perform solenoid and bail service check (DA561). e. Check drive belt tracking and replace if defective (DA570).	Replace defective components and make any necessary adjustments. See DA356, procedure 2.
5. Defective drive motor	Exchange drive motor (DA580).	See DA356, procedures 2 and 4.

DA354 Seek/Read Failure Action Plan

You are using this action plan because the error log indicated that the diskette adapter detected a failure during a seek or read operation. Either a record-not-found condition or a CRC error occurred.

Note: *A defective diskette can cause this failure type. If you suspect the diskette, perform a surface analysis on that diskette using DA MAP menu option D (see DA212, Routing 29 Selection and Operation).*

Proceed in the following sequence:

Caution: Turn power off when removing or exchanging cards.

Probable Cause	Action	Comment
1. Incorrect drive voltage	Measure drive voltages (Figure DA420-2): a. TPB15 = +4.5 to +5.5V dc b. TPA8 = +21.6 to +26.4V dc c. TPA9 = -4.5 to -5.5V dc	If missing, check using Figure DA420-1. If out of tolerance, go to PA MAP.
2. Loose or defective drive grounding jumper.	Inspect for loose or defective grounding jumper (DA520).	See DA356, procedure 2.
3. Defective diskette adapter and/or diskette drive control cards	Exchange DA1 and DA2. Exchange DA3 (DA670).	See DA356, procedures 1, 2, and 3.
4. Head/carriage assembly binding	Check head/carriage assembly for binds: a. Stepper motor (DA601/602). b. Drive band idler (DA630). c. Drive band (DA620).	Correct cause of binding. See DA356, procedure 2.
5. Defective or out of adjustment drive component	Perform the following service checks: a. Drive band (DA621). b. Solenoid and bail (DA561). c. Drive belt tracking. Replace if worn (DA571). d. Head/carriage (DA551).	Replace defective components and make any necessary adjustments. See DA356, procedure 2.
6. Defective head/carriage assembly	Exchange head/carriage assembly (DA550).	See DA356, procedures 2 and 4.

DA355 Erase/Write Failure Action Plan

You are using this action plan because the error log indicated that a failure occurred in the diskette drive erase/write logic. The Erase/Write Current Sense line, which should be off when reading and on when writing, was at the wrong level. Proceed in the following sequence:

Caution: Turn power off when removing or exchanging cards.

Probable Cause	Action	Comment
1. Loose head cable connector	Visually check (Figure DA420-3).	See DA356, procedure 2.
2. Defective diskette drive control card	Exchange DA3 (DA670).	See DA356, procedures 2 and 3.
3. Defective diskette adapter card	Exchange DA1 and DA2.	See DA356, procedures 1, 2, and 3.
4. Defective head/carriage assembly	Exchange head/carriage assembly (DA550).	See DA356, procedures 2 and 4.

DA356 Common Error Log Action Plan Procedures

Use the procedure in this section when referenced by the action plans in DA351 through DA355.

1. Use the following table for the location of the diskette adapter (DA1 and DA2) cards and SCF (SC1 and SC5) cards by machine type and model.

Machine Type	Model	DA1	DA2	*SC1	SC5
8130	A2X	A1S2	A1R2	A2G2	A2C2
8140	A3X/A4X	A2M2	A2N2	---	A2D2
8140	A5X, A6X, A7X	A2G2	A2H2	---	A2D2
8140	B5X, B6X, B7X	B2C2	B2B2	---	A2A2
8101	A1X, A2X	A2G2	A2F2	---	A2A2

*Only applies to the 8130 without the System Expansion Feature.

2. After initiating a repair action, you must use the Free-Lance Utility (Chapter 2, CP462) to loop the tests and verify repair as follows:

   At 80BC enter PAB; at 81BC enter 20B (see DA200).

   a. If the tests fail, use the test error message and DA MAP menu option C to find the failure.
   b. If the tests complete successfully (PA00), have the customer use the system. Obtain another copy of the error log and examine it for diskette storage failures that relate to the action plan you are using.
      (1) If the log indicates the same failure type, perform the next action plan step.
      (2) If the log indicates no failures, end the repair action.

3. If the failure still occurs after exchanging the card(s), reinstall the original card(s) before continuing to the next action plan step.
4. If the failure still occurs after exchanging the FRU and you have performed all action plan steps, request aid.

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DA400 Signal Paths and Detailed Operational Description

This section provides a logical grouping of three types of information:

- DA410 through DA425 permit you to check the point-to-point diskette logic signal continuity from the diskette adapter DA1 card to the SCF card and to the diskette drive control (DA3) card test points. It also permits you to check the connections between the DA3 card and the diskette drive components.
- DA430 and DA440 are action plans. Use DA430 to perform fault isolation on possible SCF failures and DA440 to determine the cause of manual diskette insertion and removal problems.
- DA450 through DA455 provides a detailed diagram and description of the diskette data flow, as well as read, write, and seek principles of operation. They also provide logic diagrams, a typical read/write timing sequence, and show the adapter top card connector signals.

In the following sections, refer to the figure below for the DA1 and SCF card location.

Machine Type	Model	DA1	*SC1	SC5
8130	A2X	A1S2	A2G2	A2C2
8140	A3X/A4X	A2M2	–––	A2D2
8140	A5X, A6X, A7X	A2G2	–––	A2D2
8140	B5X, B6X, B7X	B2C2	–––	A2A2
8101	A1X, A2X	A2G2	–––	A2A2

*Only applies to the 8130 without the System Expansion Feature.

Figure DA400-1. DA1 and SCF Card Locations

DA410 Diskette Adapter Logic Signal Continuity

Use DA411 to check the continuity of logic signals from the diskette adapter DA1 card to the SCF card. Refer also to DA412 to check certain signals used by the DA1 and DA2 cards. The MAP uses these fault isolation procedures when it detects particular diskette adapter errors, including those which indicate test failures within specific routines.

DA411 Adapter to SCF Continuity Check

Use the following table and the procedure below to determine if diskette adapter to SCF continuity exists for the line names specified.

Caution: Turn power off before performing this check.

1. Check the continuity of each line name between the DA1 and SCF card test points according to the failing test error message or indication as shown in the following table. (See Figure DA400-1 for card locations.)
2. For any open circuit, determine if the failing line is either in the board or the cable. (See SC410 in volume 4 for SCF board wiring.)
   a. For board failures, wire-wrap the open pins.
   b. For cable failures, temporarily fix the open line by wire-wrapping the failing points if necessary, then obtain another cable.
3. Run the diskette storage tests to verify the repair. At 80BC enter PAB; at 81BC enter 20B (see DA200).

Test Error Message or Indication	Line Name	DA1 Pin	SC5 Pin	SC1 Pin
PA1E 01XX	–Data Tag (TD)	U05	G02	X22
	–Address Tag (TA)	U06	G10	X30
	–Command Tag (TC)	S05	J10	X10
	–Valid Byte 1 (VB1)	U02	D06	X07
	–PIO Data Bus Bit P0	B12	M12	W27
	–PIO Data Bus Bit 0	G04	B02	W22
	–PIO Data Bus Bit 1	D13	B08	W28
	–PIO Data Bus Bit 2	J02	D11	W11
	–PIO Data Bus Bit 3	G02	G04	W24
	–PIO Data Bus Bit 4	J06	J07	W04
	–PIO Data Bus Bit 5	G07	G09	W27
	–PIO Data Bus Bit 6	G08	M02	W07
	–PIO Data Bus Bit 7	G03	P10	W06
	–PIO Data Bus Bit P1	B10	P13	W33
	–PIO Data Bus Bit 8	D12	D05	W05
	–PIO Data Bus Bit 9	J04	B10	W30
	–PIO Data Bus Bit 11	J07	G05	W09
	–PIO Data Bus Bit 14	G05	P06	W23
PA1E 02XX	–PIO Data Bus Bit 10	G09	D13	W13
	–PIO Data Bus Bit 12	D10	G08	W29
	–PIO Data Bus Bit 13	J09	J09	W10
	–PIO Data Bus Bit 15	J05	P11	W32
PA1E 03XX	–Halt	P02	J06	X09
PA1E 05XX	–End of Chain (EOC)	U13	D09	X04
	–Channel Request Low	M05	J02	X13
	–Interrupt Req Removed (IRR)	P10	B05	X29
	–Modifier	P13	B12	X24
PA80	–Channel Grant	U10	P02	Y02
PA1E 26XX	–Parity Valid	U11	B04	X25
P895	–I/O Tag	S09	J05	X05
P896	+Gate Interface Drive On	P05	B13	Y22
Intermittent Problems	–Exception	U07	D10	X23
	–System Reset	S03	G12	Y13
	–Release	S02	P09	Y09

DA412 Adapter Logic Continuity Check

Use the table and procedure below to determine if diskette adapter logic continuity exists at the test points specified.

Caution: Turn power off before performing this check.

1. Check the continuity between test points A and B according to the failing test error message or indication. (See Figure DA400-1 for card location.) For any open circuit, wire-wrap the test points together.
2. For all errors, check the diskette adapter top card connector continuity.
3. Run the diskette storage tests to verify the repair. At 80BC enter PAB; at 81BC enter 20B (see DA200).

Test Error Message or Indication	DA1 Card	
	Test Point A	Test Point B
PA1E 01XX	M03	D08
	M07	D08
	P09	D08
	S13	U08
	P12	D04
	P06	D04
	M04	D04
PA1E 03XX	M09	P08
PA1E 05XX	D02	D07
	S12	U08
Intermittent Problems	B03	D04
	U09	D04

DA420 Adapter to Control Card Checks and Read Head Cable Continuity

The DA MAP refers you to DA420 through DA425 to check either the continuity or presence of logic signals that could possibly cause diskette storage failures according to the error indication.

Refer to Figure DA400-1 for the DA1 card location, Figure DA420-1 for the point-to-point continuity from the adapter DA1 card to the diskette drive control (DA3) card test points, Figure DA420-2 for the DA3 card test point numbering and line names, and to Figures DA420-3 and DA420-4 for DA3 card logic and card, card connector, and cable pin numbering.

Note: *If an open circuit exists between the DA3 card pin and the test point pin, exchange the DA3 card.*

	DA1 Card Pin Numbers			Diskette Adapter Board-Diskette Drive Control Cable Pin Numbers				Diskette Drive Control (DA3) Card (01D-A1)		
	Mach Type	Models	Card Loc							
Line Name	8130 8140 8140 8140 8101	A2X A3X, A4X A5X, A6X, A7X B5X, B6X, B7X A1X, A2X	A1S2 A2M2 A2G2 B2C2 A2G2	8130 Models A2X A-A1	8140 Models AXX A-A2	8140 Models BXX A-B2	8101 A-A2	Conn Pin	Card Pin	Test Point
+Access 0		J10		H1A13	L6D04	A1D13	K5B02	D02	B02	TPB1
+Access 1		P04		H1B13	L6E04	A1E13	K5B03	D03	B03	TPB2
+Access 2		J13		H1C13	M6A04	B1A13	K5B04	D04	B04	TPB3
+Access 3		P07		H1D13	M6B04	B1B13	K5B05	D05	B05	TPB4
+Write Data		J11		H1A11	L6D02	A1D11	K5D02	B02	D02	TPA1
+Write Gate		J12		H1D11	M6B02	B1B11	K5D05	B05	D05	TPA3
+Erase Gate		S08		H1C11	M6A02	B1A11	K5D04	B04	D04	TPA2
+Erase/Write Current Enable		U12		J1C11	N6A02	C1A11	K5D09	B09	D09	TPA7
+Select Head 1		M10		J1E11	N6C02	B1D11	K5D07	B07	D07	TPA5
+Head Engage		U04		J1D13	N6B04	C1B13	K5B10	D10	B10	TPB7
+Index		B09		K1B13	N6E04	C1E13	K5B13	D13	B13	TPB9
+Drive Data		B08		J1A13	M6D04	B1D13	K5B07	D07	B07	TPB5
+Diskette Sense		B04		J1B13	M6E02	B1E13	K5B08	D08	B08	TPB6
+Inner Tracks		G10		H1E11	M6C02	B1C11	K5D06	B06	D06	TPA4
+Switch Filter		G13		K1A13	N6D04	C1D13	K5B12	D12	B12	TPB8

Line Name	Power Connections to Diskette Drive (see PA440-PA443)	Diskette Drive Control (DA3) Card (01D-A1)		
		Conn Pin	Card Pin	Test Point
Ground	TB1-2	B08	D08	TPA6
+24V dc	PC1-J2-1	B10	D10/J12	TPA8
+5V dc	TB1-7	B03	D03/J03	TPB15
–5V dc	PC1-J2-2	B11	D11/J13	TPA9

Figure DA420-1. DA1 Card to DA3 Card Point-to-Point Continuity

A

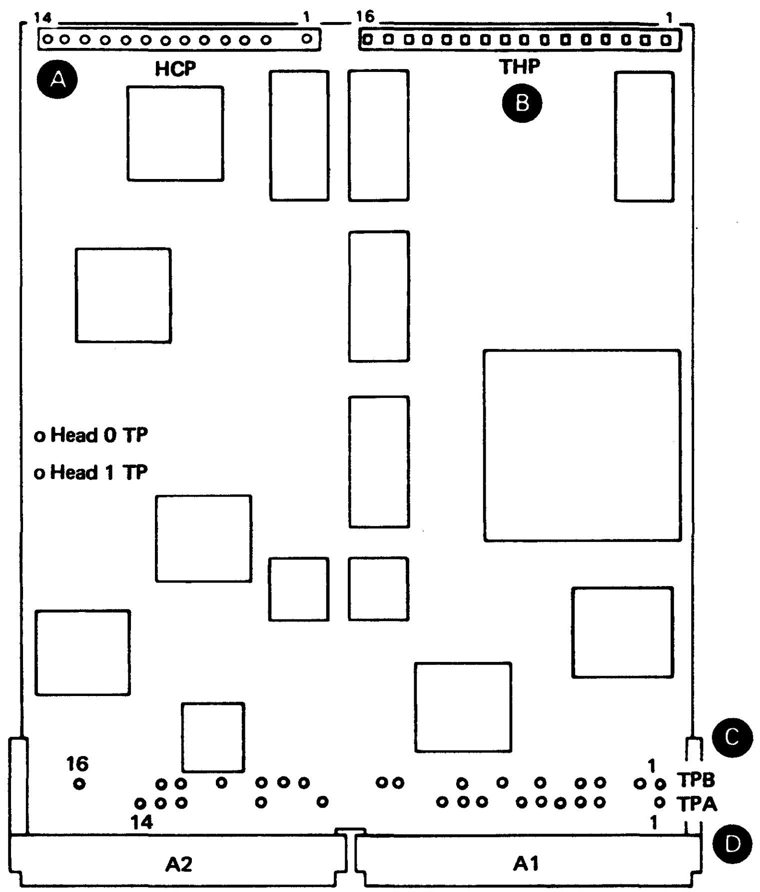
HCP1	Unused
HCP2	Blank
HCP3	R/W Head 0
HCP4	R/W Head 0 Center Tap
HCP5	R/W Head 0
HCP6	Erase Head 0
HCP7	Erase Head 0
HCP8	Cable Shield Head 0
HCP9	Cable Shield Head 1
HCP10	Erase Head 1
HCP11	Erase Head 1
HCP12	R/W Head 1
HCP13	R/W Head 1 Center Tap
HCP14	R/W Head 1

B

THP1	+Diskette Inserted
THP2	-Head Load Osc.
THP3	+14V dc
THP4	Ground
THP5	Ground
THP6	+53FD Index
THP7	+33FD Index
THP8	Diff Read A
THP9	Diff Read B
THP10	-High Gain
THP11	-Align Access 0
THP12	-High Current
THP13	Preamp TP1
THP14	Preamp TP2
THP15	-High Gain A
THP16	-High Gain B

C

TPB1	+Access 0
TPB2	+Access 1
TPB3	+Access 2
TPB4	+Access 3
TPB5	+Drive Data
TPB6	+Diskette Sense
TPB7	+Head Engage
TPB8	+Switch Filter
TPB9	+Index
TPB10	MC-3
TPB11	MC-0
TPB12	MC-2
TPB13	-Head Load
TPB14	53FD LED Voltage
TPB15	+5V dc
TPB16	53FD PTX



D

TPA1	+Write Data
TPA2	+Erase Gate
TPA3	+Write Gate
TPA4	+Inner Tracks
TPA5	+Select Head 1
TPA6	Ground
TPA7	+Erase/Write Current Enable
TPA8	+24V dc
TPA9	-5V dc
TPA10	MC-1
TPA11	+Head Load Solenoid
TPA12	33FD LED Voltage
TPA13	Ground
TPA14	33FD PTX

Figure DA420-2. DA3 Card Test Points and Locations

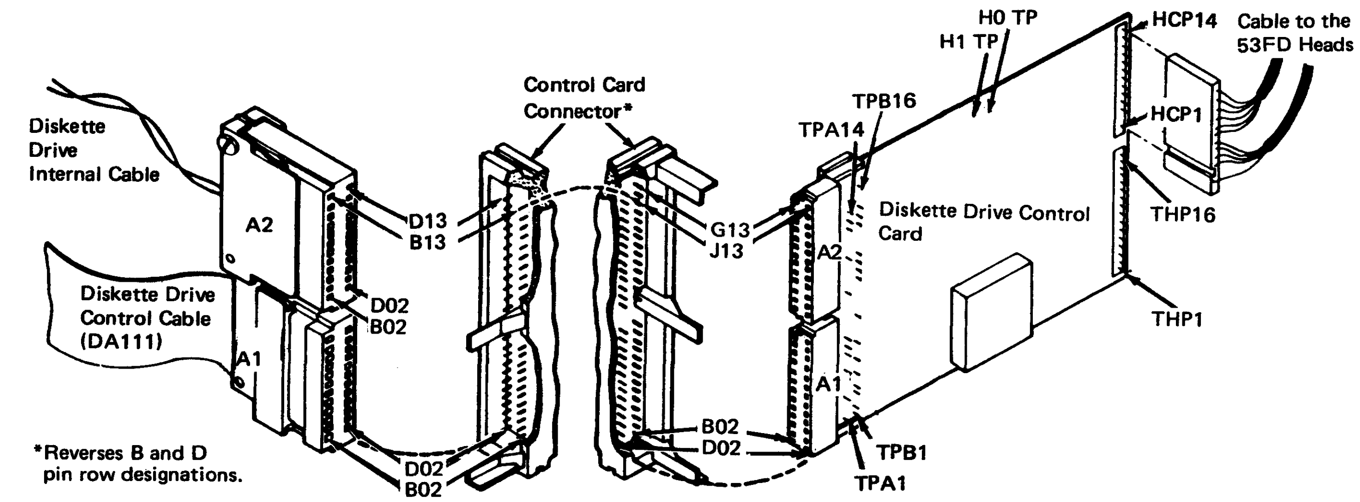
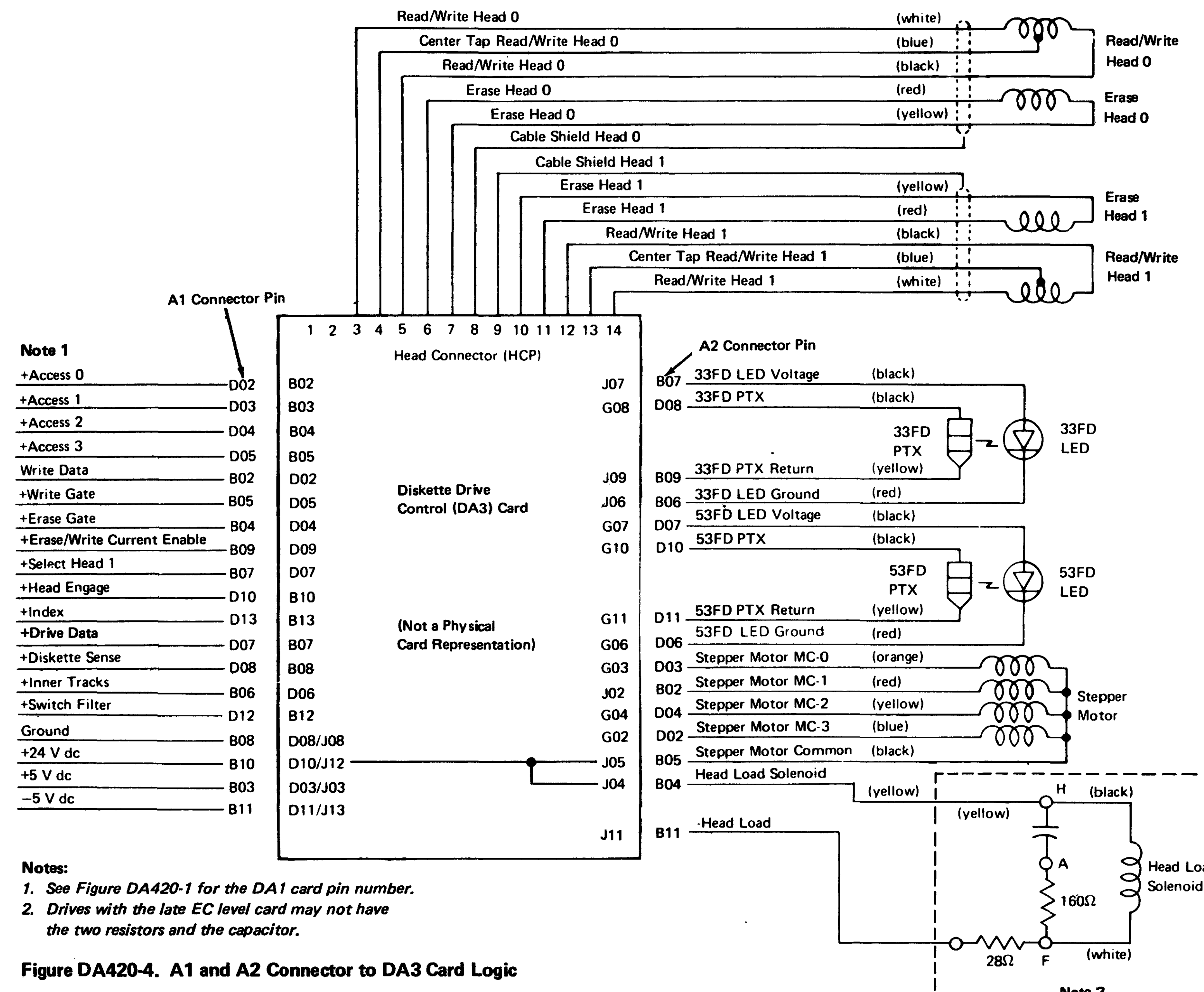


Figure DA420-3. DA3 Card, Connector, and Cable Pin Numbering



Notes:

1. See Figure DA420-1 for the DA1 card pin number.

2. Drives with the late EC level card may not have the two resistors and the capacitor.

Figure DA420-4. A1 and A2 Connector to DA3 Card Logic

DA421 Access Pulse Logic Check

Use the table below to determine the presence of access pulses from the diskette adapter DA1 card pins to the diskette drive control (DA3) card test points.

Note: *Power must be on with the DA3 card inserted to perform this check.*

Refer to Figure DA400-1 for the DA1 card location and to Figure DA420-2 for the DA3 card test point numbering and line names. For any failure, see Figure DA420-1 for the point-to-point wiring and repair accordingly.

Line Name	DA1 Pin	DA3 Test Point
+Access 0	J10	TPB1
+Access 1	P04	TPB2
+Access 2	J13	TPB3
+Access 3	P07	TPB4
Ground	D08	TPA13

DA422 Erase/Erase Gate Logic Continuity Check

Use the table below to determine the continuity of the erase/erase gate logic from the diskette adapter DA1 card pins to the diskette drive control (DA3) card socket pins or card test points. You can perform this check with the DA3 card either inserted or removed.

Caution: Turn power off before performing this check.

Refer to Figure DA400-1 for the DA1 card location, Figure DA420-2 for the DA3 card test point numbering and line names, and to Figure DA420-3 for the DA3 card socket pin numbering. For any failure, see Figure DA420-1 for the point-to-point wiring and repair accordingly.

Line Name	DA1 Pin	DA3 Socket Pin	DA3 Test Point
+Erase Gate	S08	D04	TPA2
+Inner Tracks	G10	D06	TPA4
+Write Gate	J12	D05	TPA3
+Erase/Write Current Enable	U12	D09	TPA7

If no trouble exits for the above lines, check the read head cable continuity in DA425.

DA423 Read Signal Logic Continuity Check

Use the table below to determine the continuity of the read signal logic from the diskette adapter DA1 card pins to the diskette drive control (DA3) card socket pins or card test points. You can perform this check with the DA3 card either inserted or removed.

Caution: Turn power off before performing this check.

Refer to Figure DA400-1 for the DA1 card location, Figure DA420-2 for the DA3 card test point numbering and line names, and to Figure DA420-3 for the DA3 card socket pin numbering. For any failure, see Figure DA420-1 for the point-to-point wiring and repair accordingly.

Line Name	DA1 Pin	DA3 Socket Pin	DA3 Test Point
+Drive Data	B08	B07	TPB5
+Head Engage	U04	B10	TPB7
+Select Head 1	M10	D07	TPA5

If no trouble exists for the above lines, check the read head cable continuity in DA425.

DA424 Write Signal Logic Continuity Check

Use the table below to determine the continuity of the write signal logic from the diskette adapter DA1 card pins to the diskette drive control (DA3) card socket pins or card test points. You can perform this check with the DA3 card either inserted or removed.

Caution: Turn power off before performing this check.

Refer to Figure DA400-1 for the DA1 card location, Figure DA420-2 for the DA3 card test point numbering and line names, and to Figure DA420-3 for the DA3 card socket pin numbering. For any failure, see Figure DA420-1 for the point-to-point wiring and repair accordingly.

Line Name	DA1 Pin	DA3 Socket Pin	DA3 Test Point
+Write Data	J11	D02	TPA1
+Write Gate	J12	D05	TPA3
+Erase Gate	S08	D04	TPA2
+Inner Tracks	G10	D06	TPA4

If no trouble exists for the above lines, check the read head cable continuity in DA425.

DA425 Read Head Cable Continuity Check

Caution: Do not use an ohmmeter to perform this check.

Use the table below and Figures DA420-2 and DA420-3 to visually determine the read head cable continuity.

Head 0

Line Function	From Test Point	Color
Read/Write Signal	HCP3	White
Center Tap	HCP4	Blue
Read/Write Signal	HCP5	Black
Erase Head	HCP6	Red
Erase Head	HCP7	Yellow
Cable Shield	HCP8	–

Head 1

Line Function	From Test Point	Color
Cable Shield	HCP9	–
Erase Head	HCP10	Yellow
Erase Head	HCP11	Red
Read/Write Signal	HCP12	Black
Center Tap	HCP13	Blue
Read/Write Signal	HCP14	White

DA430 System Control Facility (SCF) Action Plans

Certain SCF bus failures that occur on the address group containing the diskette storage facility can appear as a problem within the diskette storage. To determine if the SCF caused this failure, use the action plans in DA431 and DA432 as follows:

- For an 8130 without the System Expansion Feature, use DA431.
- For an 8130 with the System Expansion Feature and for all 8140s and 8101s, use DA432.

DA431 8130 Without the System Expansion Feature

Use this action plan for an 8130 without the System Expansion Feature to determine if the SCF caused an apparent diskette failure. Proceed as follows:

Caution: Turn power off before removing or inserting cards.

1. Ensure that the customer's diskette storage configuration table entry contains the correct PA value as determined by the diskette location (see DA113).
2. Exchange the SC1 card (01A-A2G2).
3. If the failure still occurs, reinstall the original card before continuing.

DA432 8130 with the System Expansion Feature/8140/8101

Use this action plan for an 8130 with the System Expansion Feature and for all 8140s and 8101s to determine if the SCF caused an apparent diskette failure. Proceed as follows:

Caution: Turn power off before removing or inserting cards.

1. Ensure that the address switch settings on the SC5 card are correct for the address group specified by the P value of the diskette adapter PA (see DA112 and SC442). The card locations are:

8130	01A-A2C2
8140 Models A3X-A7X	01A-A2D2
8140 Models B5X-B7X	01A-A2A2
8101	01A-A2A2

   a. If the switches are correct, go to step 2.
   b. If the switches are incorrect, a system configuration problem exists; either the switch setting or the diskette configuration table entry is wrong. Determine the correct PA according to the diskette location and make the necessary corrections.
2. Exchange the SC5 card.
3. If the failure still occurs, reinstall the original card before continuing.
4. If the test error message was PA1E 053F, go to SC250 and use Action Plan 07 for additional fault isolation.
5. For all other errors, return to the DA MAP.

DA440 Diskette Manual Insertion or Removal Failure Action Plan

Use this action plan if the diskette cannot be inserted or removed from the diskette drive. Proceed as follows:

Caution: Turn power off when removing or exchanging cards or cables.

1. Visually check for obstructions in the drive that could prevent diskette insertion or removal.
2. Determine if the problem exists only with power on or off.
   a. If the problem exists only with power on, exchange the DA1 card (see below) and/or the diskette drive control card (DA3).

Machine Type	Model	DA1
8130	A2X	A1S2
8140	A3X/A4X	A2M2
8140	A5X, A6X, A7X	A2G2
8140	B5X, B6X, B7X	B2C2
8101	A1X, A2X	A2G2

   b. If the problem exists only with power off, go to step 3.
3. Perform the solenoid and bail service check (DA561) and adjust if necessary.
4. Request aid.

DA450 Diskette Storage Detailed Description and Operation

The diskette storage facility consists of two adapter cards (DA1 and DA2), a diskette drive control card (DA3), and a 53FD diskette drive assembly.

- The DA1 card logic transfers control and data between the processor and the DA3 card.
- The DA2 card ensures proper operation of the DA1 card.
- The DA3 card controls the operation of the diskette drive.

Refer to Figure DA450-1 for a diagram of the diskette storage facility data flow.

DA451 Adapter Description and Operation

The diskette adapter (DA1 and DA2) automatically loads the wrap test when required, controls all necessary diskette timings and delays, and transfers information to and from the processor through the System Control Facility for either channel I/O (CHIO) or programmed I/O (PIO) operations.

Some PIO commands, such as Set Control Register and Read Basic Status, cause immediate action or data transfer. Others, such as Seek, Read, or Write Record, initiate an action that requires a variable time to complete. Of these, the Read or Write Record commands also cause CHIO transfers to occur. Any command that initiates an action or causes a CHIO transfer also causes an interrupt when the command completes.

Two 128K-byte adapter buffers, each of which operates independently, permit a maximum data transfer rate of 128K bytes per second between the adapter and the drive, but can only operate at 98.3K bytes for a full track transfer. While one buffer is loading, the other transfers the previously loaded data to either the diskette or the processor, depending on the direction of data flow.

DA452 Adapter to Diskette Control Logic Description and Operation

The adapter transfers information with the diskette drive through the diskette drive control cable and control card (DA3). The following paragraphs describe the signals between the adapter and the DA3 card, and are grouped by their function as an adapter output or input. Refer to Figure DA450-1 for the line pin numbers and other related logic, and to Figure DA452-1 for a point-to-point illustration of some of these lines.

Adapter Output Logic Signals

Access 0, 1, 2, and 3. These four lines (see Figure DA452-1), only two of which should be active at any time, drive the stepper motor to move the head/carriage assembly to the selected cylinder (track). The table below shows the sequence and status (0 = off, 1 = active) of these lines necessary to move the head/carriage either in (toward the hub) or out to the selected cylinder. These lines can change status every 5 ms, and the last two used must remain active to electrically detent the stepper motor until performing another access.

	Cylinder Number											
Signal	**0**	**1**	**2**	**3**	**4**	**5**	**–**	**40**	**–**	**74**	**75**	**76**
Access 0	1	0	0	1	1	0	–	1	–	0	1	1
Access 1	1	1	0	0	1	1	–	1	–	0	0	1
Access 2	0	1	1	0	0	1	–	0	–	1	0	0
Access 3	0	0	1	1	0	0	–	0	–	1	1	0

Head Engage. When active, permits the heads to move toward the diskette surface under spring tension (see Figure DA452-1).

Write Gate. When active, conditions the write select and write current source logic to permit a write operation.

Erase Gate. When active, conditions the tunnel erase logic to permit an erase operation, which can only occur during a write.

Write Data. Transmits clock and data information used for a diskette write operation.

Inner Track. Provides the proper write current for a write operation and causes increased signal amplification when using inner tracks (cylinders). The adapter sets the line level (minus for cylinders 00-41 and plus for 42-76) at the start of every seek.

Switch Filter. Conditions the read amplifier logic to read the innermost cylinders with a minimum of bit shift. The adapter sets the line level (minus for cylinders 00-59 and plus for 60-76) at the start of every seek.

Select Head 1. Specifies the head used for a read or write operation and, when active, selects head 1.

Adapter Input Logic Signals

Drive Data. Transmits the diskette data during a read operation. Each magnetic transition on the diskette produces a pulse on this line, which the adapter then separates into clock and data pulses.

Index. When active (see Figure DA452-1), indicates that an index hole is passing between the phototransistor and LED. The adapter uses this line to determine that a diskette is both loaded and rotating at the correct speed.

Diskette Sense. Specifies the diskette type loaded and, when active, indicates a diskette type 2 or 2D (see Figure DA452-1).

Erase/Write Current Enable. When active, indicates only that either the erase or write driver logic is conditioned, and not that an erase or write operation occurred. The adapter determines proper line status, which should be off when not writing.

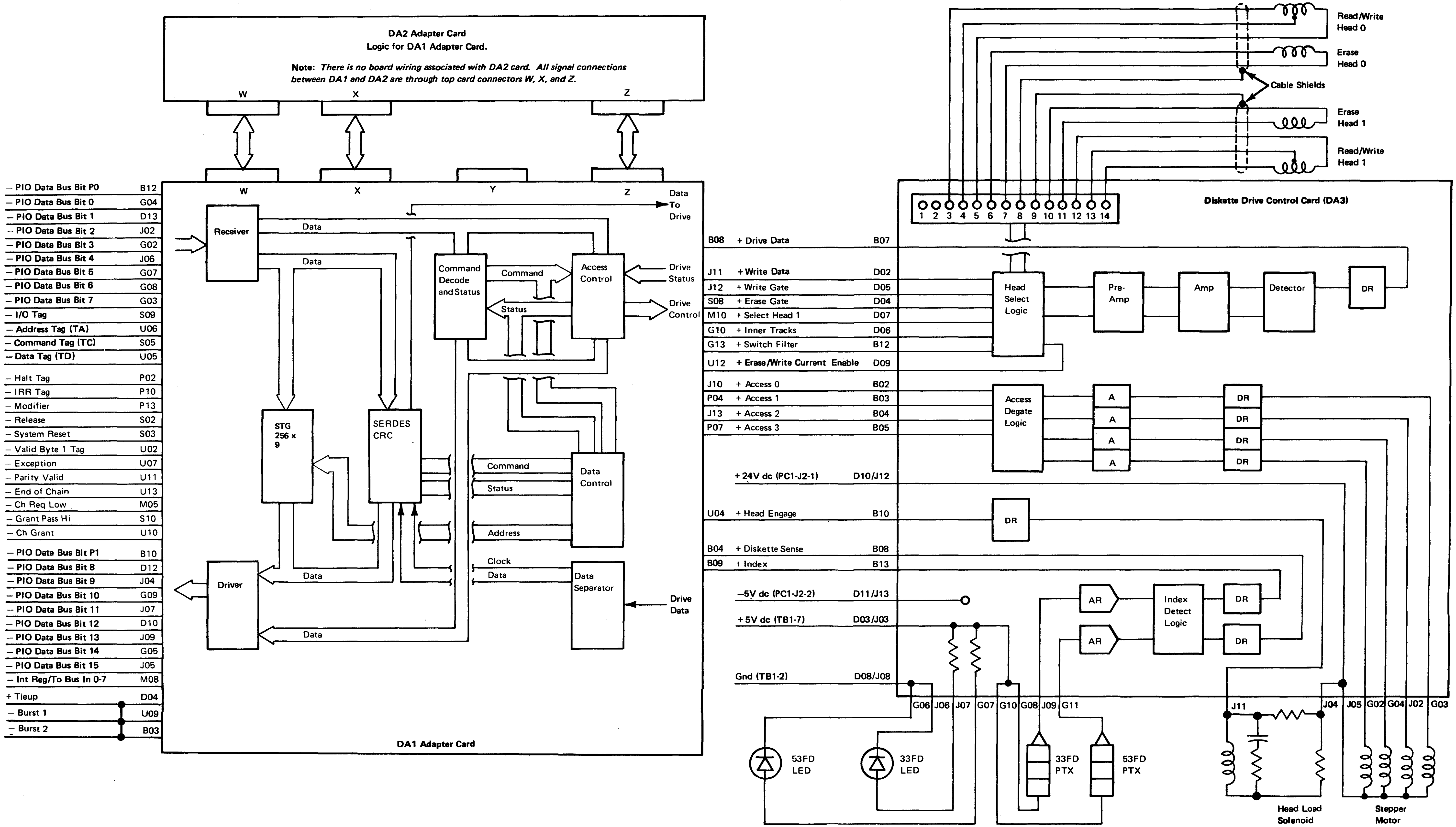
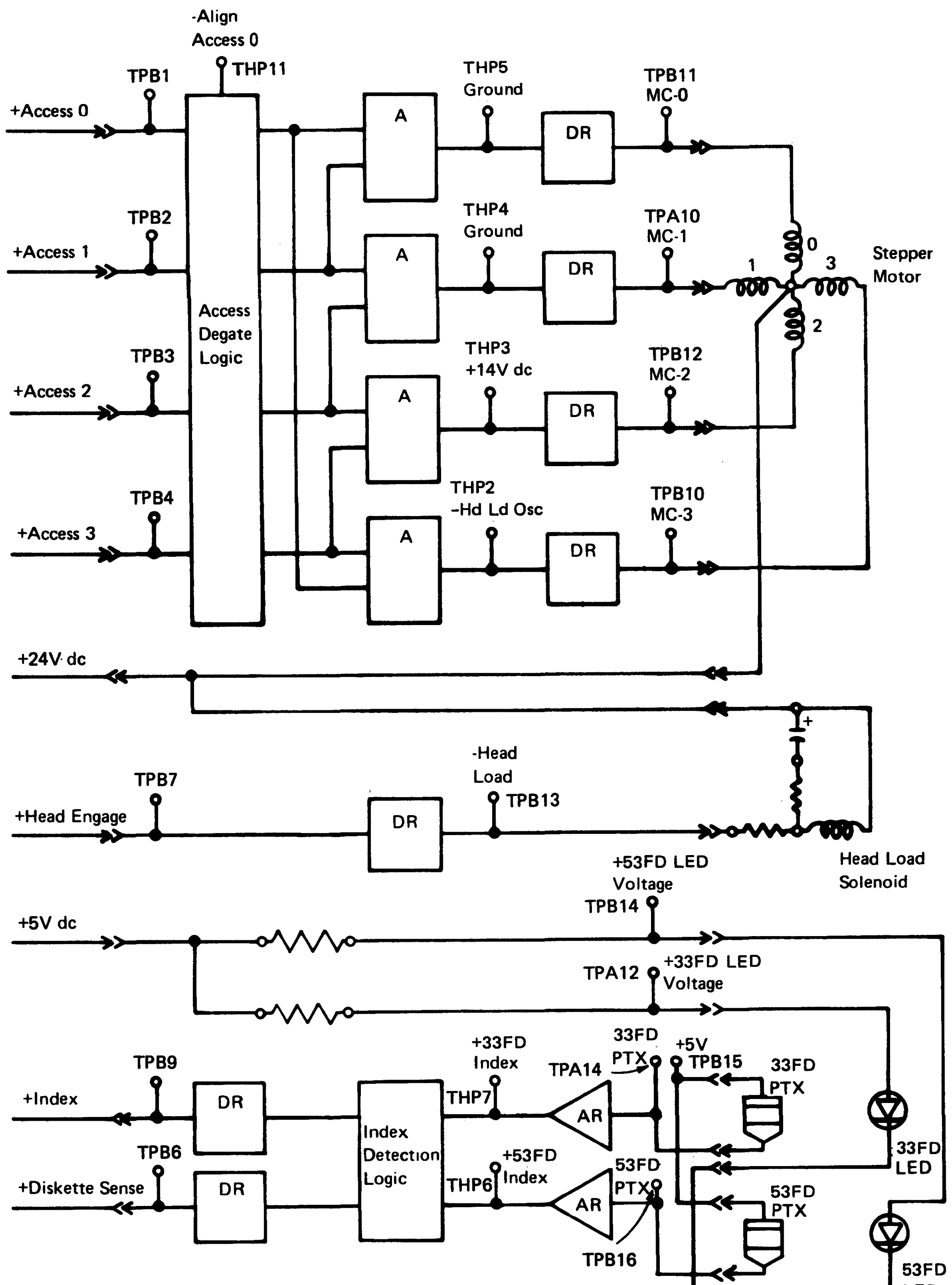


Figure DA450-1. Diskette Storage Data Flow

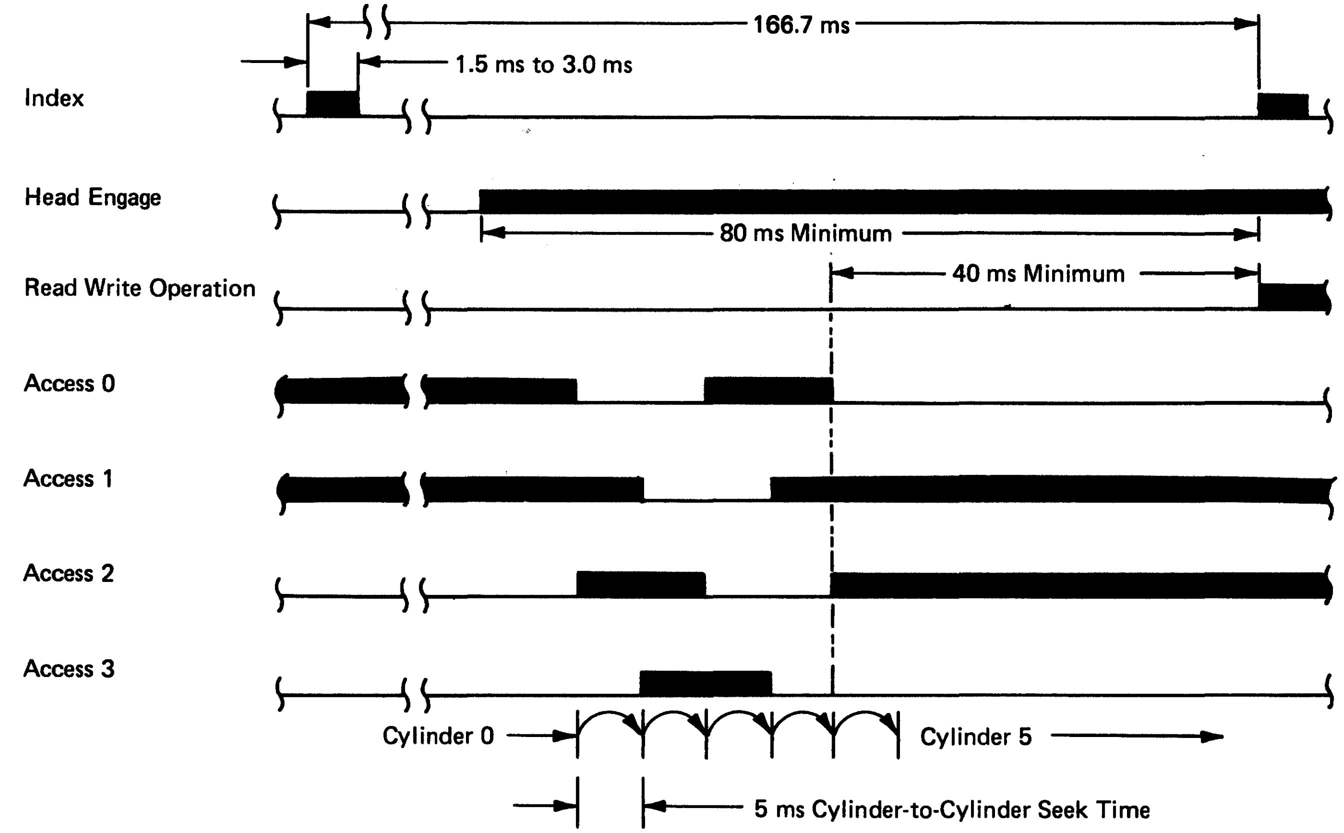


Note: *See Figure DA420-2 for test point locations.*

Figure DA452-1. DA3 Card Access, Head Load, and Index Logic

DA453 Typical Read/Write/Seek Timing

The chart below shows how a read or write operation relates to index and access timing. Note that a read or write cannot begin until at least 40 ms after the last access pulse and at least 80 ms after the rise of the Head Engage signal. Note also that the Index pulse dictates the read and write time but does not control the seek or head load (engage) operations.



DA454 Diskette Adapter Top Card Connector Signals

The following shows the signals present at the diskette adapter top card connectors

Caution: Use only the correct top card connector part numbers (see DA111).

Signal	Pin	Block	Pin	Signal
+Std Clock	W22	W	W02	–Sel VCO
–Sel VCO Gated	W23		W03	Timer IMS
–Dec Filter (TP)	W24		W04	+IMS Timer Gated
–Cmd Valid	W25		W05	–Release
–Halt Sync/Scan	W26		W06	
–Halt Sync (Scan) Gated	W27		W07	–Op Status 2 Bit
–Incr Filter (TP)	W28		W08	Ground
–ID Am Det	W29		W09	–AM Detected
Gate Control/CRC	W30		W10	–Control Bus 3 Gated
–Bit Control Bit 2	W31		W11	Clear CRC SERDES
+I Cycle Index	W32		W12	+I Cycle Index Gated
+SW2 Gated	W33		W13	+SW1 Gated
+SW2	X22	X	X02	+SW1
–Op Bus Valid Gated	X23		X03	Ms Clock 3
–Op Bus Valid to Act L	X24		X04	+Lth Data Window
+Parity Error	X25		X05	+128 Mode
–Burst 1	X26		X06	–Burst 2
–EOC Gated	X27		X07	–EOC Inter
–Gate Control/CRC Gated	X28		X08	Ground
–Control Bus 3	X29		X09	–Special Reset
–Control Bus 2	X30		X10	–Control Bus 0 Gated
–Control Bus 0	X31		X11	–Control Bus 1
+Std Clock Delayed	X32		X12	–Processor Read Type
+Cmd/RAM PE scan	X33		X13	+Cmd/RAM PE (Scan) Gated
		Y	Y02	
			Y03	–4 Meg VCO Out (TP)
			Y04	+A Clock (TP)
			Y05	+A Clock 1 (TP)
			Y06	+Sample Clock (TP)
			Y07	+Sample Clock (TP)
			Y08	Ground
			Y09	+Ms Clock Out (TP)
			Y10	+Ms Clock Out (TP)
			Y11	RAM Clock
			Y12	–4 MHz Osc (TP)
			Y13	T1 SS
–Op Bus 2	Z22	Z	Z02	–Op Bus 0
–Op Bus 1	Z23		Z03	–Op Bus 3
–TC Sync	Z24		Z04	–Op Bus 4
–Op Bus Valid	Z25		Z05	–Op Status 0
–Op Status 2	Z26		Z06	–Op Status 1
–TC Sync	Z27		Z07	+Scan In (TP)
–Load Record Gated	Z28		Z08	Ground
+ Lt Data Window Gated	Z29		Z09	–CHIO Attached
+ Adapter Sel Sync (Scan)	Z30		Z10	
–Parity Odd	Z31		Z11	–Reset
–Control Bus 1 Gated	Z32		Z12	–TD Sync
–Parity Odd Gated	Z33		Z13	

Note: *Dashes within blocks indicate common connections.*

DA455 Read/Write/Erase Principles of Operation and Data Flow

Read Operation

The Drive Data line from the DA3 card to the adapter transmits a series of clock and data pulses from the diskette that represent the diskette data. These pulses, which are from 150 ns to 500 ns long, are separated into clock and data pulses by the data separator.

The frequency (in kHz) and amplitude (in mV) determine the bit structure for both FM and MFM encoding.

- For FM encoding, the all 0's pattern has a higher voltage than an all 1's pattern, and the sine wave signal is:

  125 kHz at 13 to 560 mV for all 0's
  250 kHz at 6.5 to 420 mV for all 1's

- For MFM encoding, the alternate 0's and 1's pattern has a higher voltage and is half the frequency of an all 0's and 1's pattern, and the sine wave signal is:

  125 kHz at 13 to 560 mV for alternate 0's and 1's
  250 kHz at 6.5 to 420 mV for all 0's or all 1's

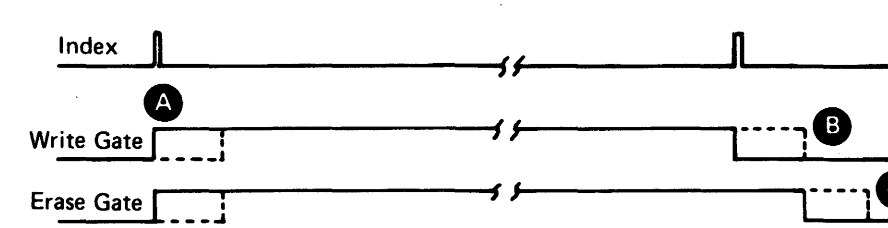
The outer tracks require a higher voltage because of higher track speeds and a lower bit density.

Format Write Operation

The format write operation writes a full track replacing all the ID (identifier) fields, data fields, and gaps. The index to first ID field gap is 73 (146 for MFM) 8-bit bytes.

Write gate is activated within 50 (100 for MFM) bytes from the leading edge of the index pulse A. Write gate is deactivated within 51 (102 for MFM) bytes after the leading edge of the next index pulse B.

Erase gate is activated the same time as write gate. However, erase gate is deactivated 537 μs after write gate is deactivated C.



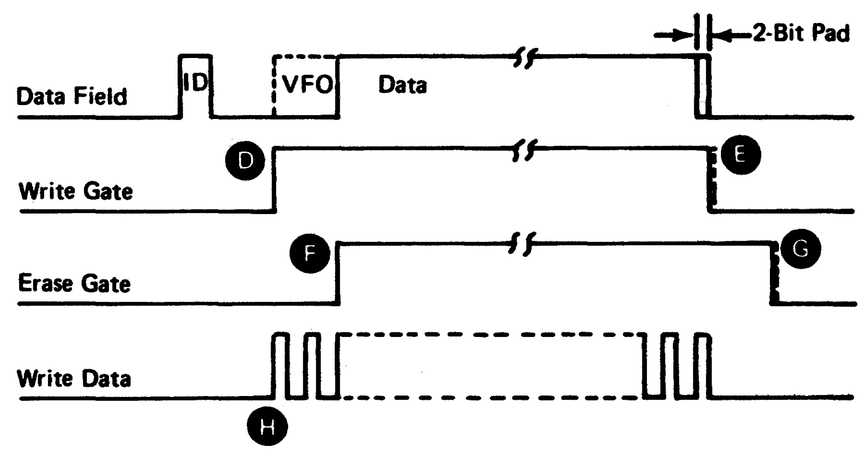
Record (Update) Write Operation

Update operations are performed on a data field and its VFO sync field only. ID fields and gaps are not written.

Write gap is activated within 237 μs after the last ID character is read D . Write gate is deactivated within 5 μs after the last clock of the 2-bit pad is written E .

Erase gate is activated 537 μs after write gate F and is deactivated 537 μs after the fall of write gate G .

The new VFO sync field begins when write gate is activated H .



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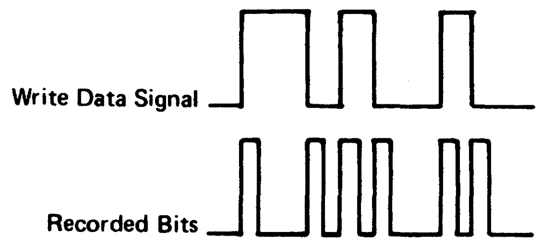
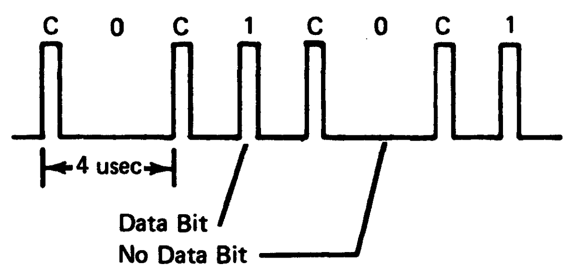
Data Write Operation

The Write Data signal determines the information written on a diskette. Each change in this signal switches the current in the read/write heads and, therefore, alters the recorded bit structure on the diskette as follows:

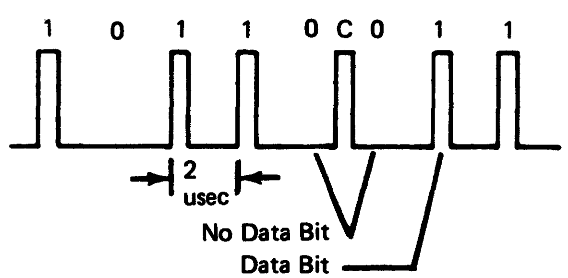


Besides the Write Data signal to determine the bit status, the adapter uses a clock pulse for bit synchronization. As the 53FD can use either FM or MFM encoding, the adapter varies the clock pulse for the encoding difference.

- In FM encoding, a constant clock pulse establishes bit synchronization. The time between the clock pulses is 4 usec. To record a bit, both clock and data pulses must be present in this period as follows:



- If MFM encoding, the adapter does not use a constant clock, but generates a clock pulse only when two consecutive no-data-bit conditions occur. Therefore, the time required between a bit or no bit indication is 2 usec as follows:



The adapter Write Gate signal A determines a read or write operation and, if on, activates the write logic and deactivates the read logic as shown in Figure DA455-1.

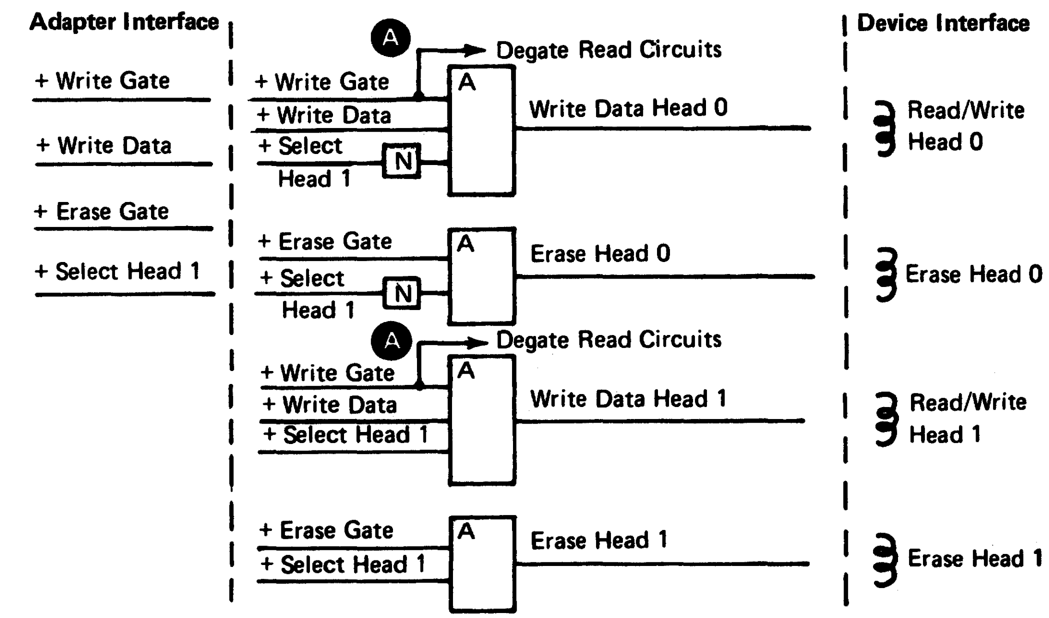
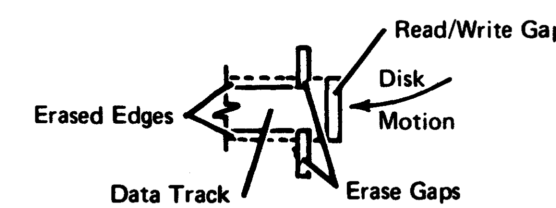


Figure DA455-1. Write Gate and Erase Gate Logic

Erase Operation

Each head contains a read/write coil and an erase coil. Because of the physical location of the erase coil, an erase operation actually erases the edges of the track, not the track itself. The Erase Gate signal (see Figure DA455-1), active during a write operation, erases these outside edges of the recorded data track immediately after writing it (see figure below). This process prevents crosstalk between tracks that could occur for subsequent read operations. Any previously written data within the track must be erased by a write operation.



DA460 Drive Data Scoping

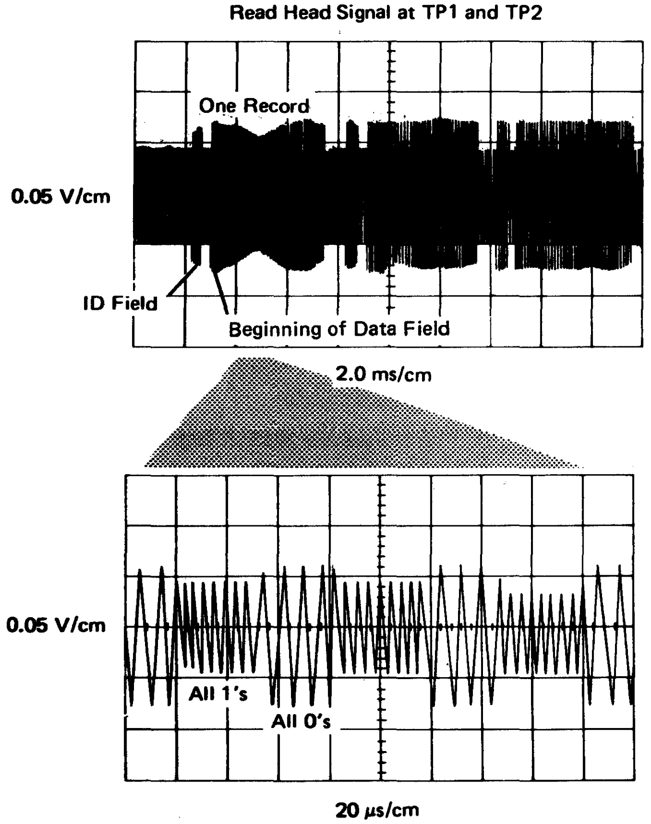
Use the Diagrams and charts in this section to scope the Drive Data signals for bit and no-bit conditions.

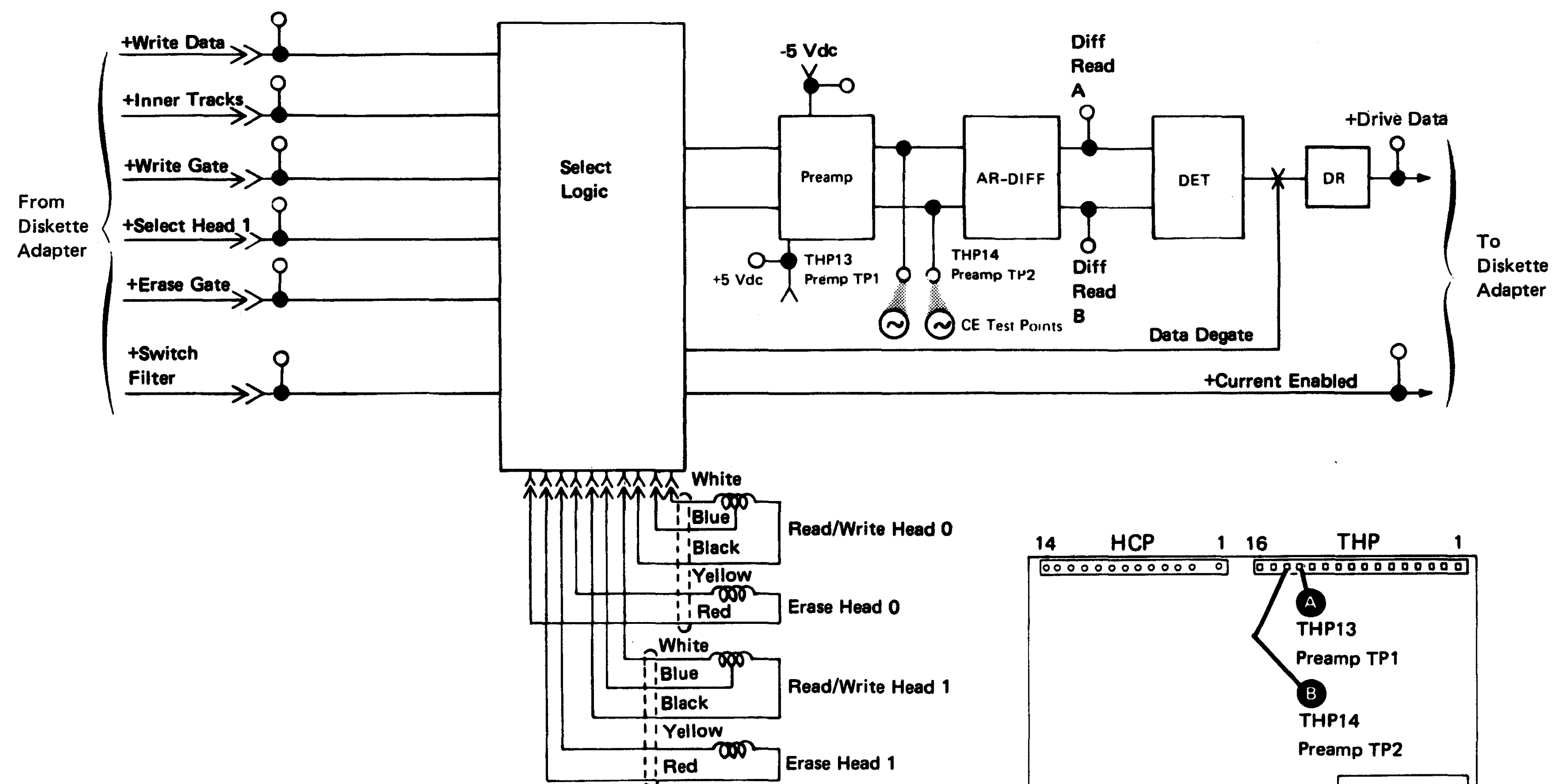
DA461 Scoping FM Drive Data

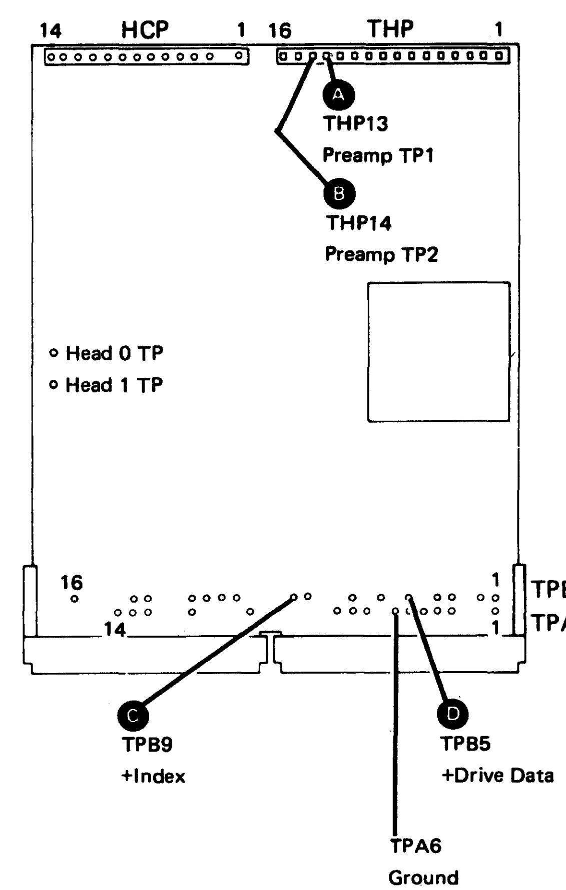
Note: Use Tektronix 453, 454, or similar oscilloscope with x10 probes.

Channel A sweep mode	Normal
Channel A level	+
Channel A coupling	dc
Channel A slope	+
Channel A source	External
Trigger	Normal
Mode	Add
Channel 1 volts/ division	5 mV/cm
Channel 2 volts/division	5 mV/cm
Channel 1 input	ac
Channel 2 input	ac
Invert	Pull out
Times per division	2ms/cm
Connect channel 1 to	Preamp TP1 A
Connect channel 2 to	Preamp TP2 B
Connect trigger to	+Index test pin C
Observe:	The amplitude of the read signal should be between 6.5 to 560 mV.

Read Head Signal at TP1 and TP2



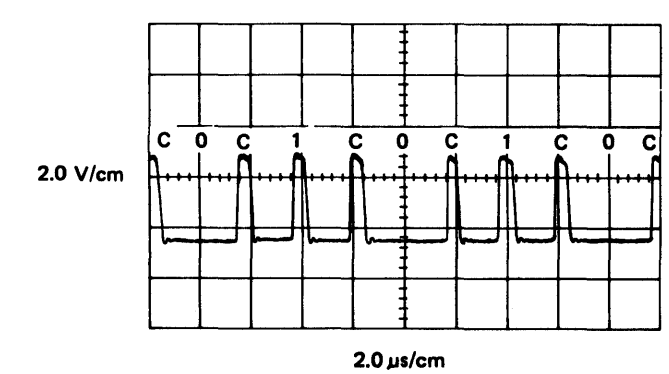




Note: Use Tektronix 453, 454, or similar oscilloscope with x10 probes.

Channel A sweep mode	Normal
Channel A level	+
Channel A coupling	dc
Channel A slope	+
Channel A source	External
Trigger	Normal
Mode	Channel 1
Channel 1 volts/division	2.0 V/cm
Channel 1 input	dc
Times per division	2µs/cm
Connect channel 1 to	+Drive Data D
Connect trigger to	+Index test pin C
Observe:	Clock pulses every 4 µs. Pulse duration should be between 100 and 500 ns. Pulse amplitude should be between 2.4 and 4.2 volts.

Drive Data
Example: 01010

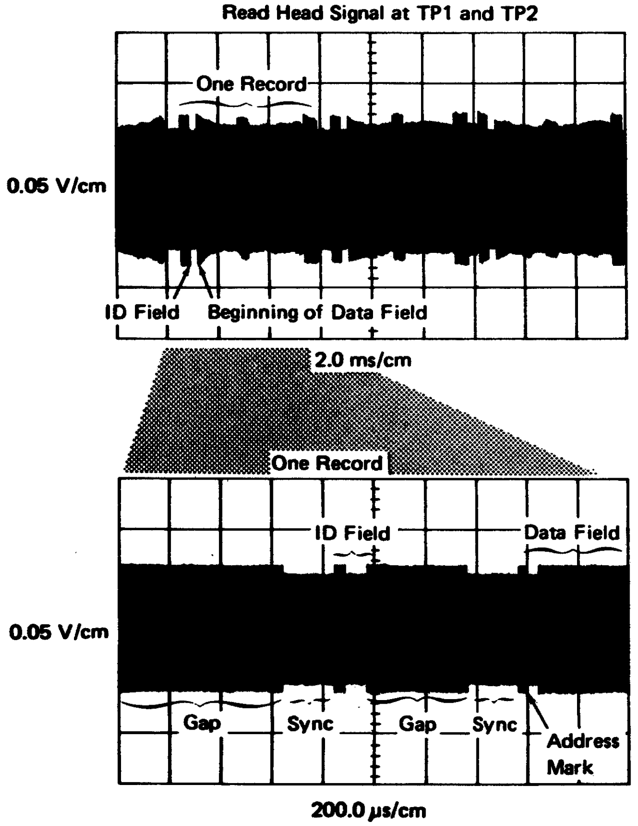


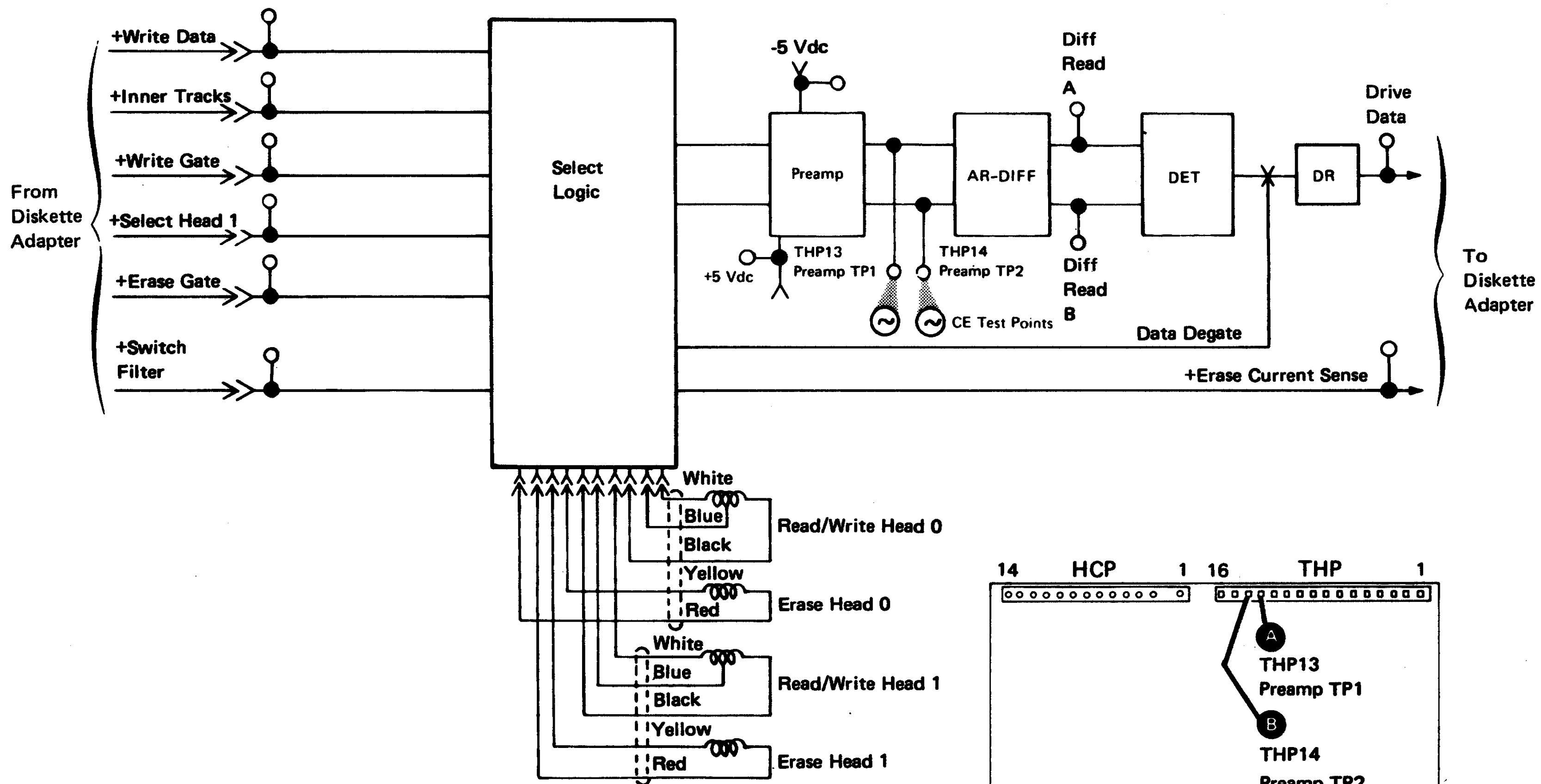
DA462 Scoping MFM Drive Data

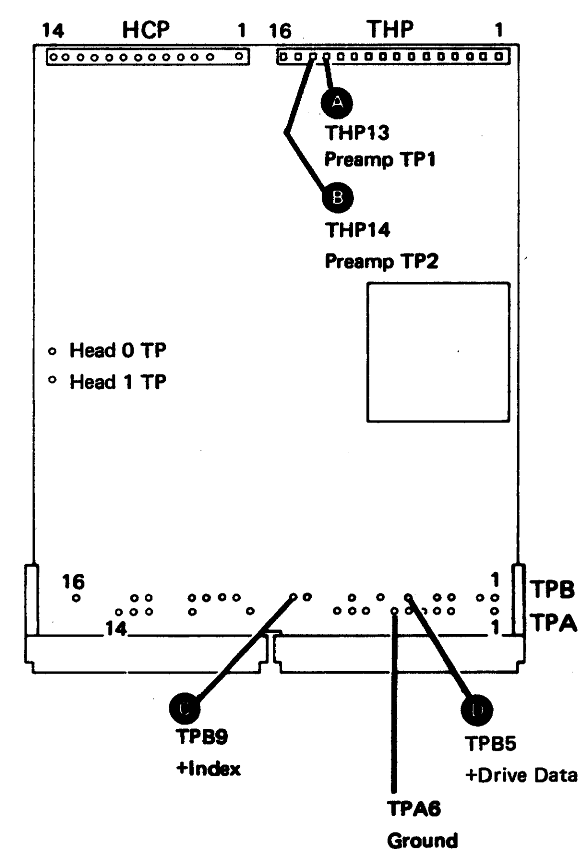
Note: Use Tektronix 453, 454, or similar oscilloscope with x10 probes.

Channel A sweep mode	Normal
Channel A level	+
Channel A coupling	dc
Channel A slope	+
Channel A source	External
Trigger	Normal
Mode	Add
Channel 1 volts/ division	5 mV/cm
Channel 2 volts/division	5 mV/cm
Channel 1 input	ac
Channel 2 input	ac
Invert	Pull out
Times per division	2ms/cm
Connect channel 1 to	Preamp TP1 A
Connect channel 2 to	Preamp TP2 B
Connect trigger to	+Index test pin C
Observe:	The amplitude of the read signal should be between 6.5 to 560 mV.

Read Head Signal at TP1 and TP2



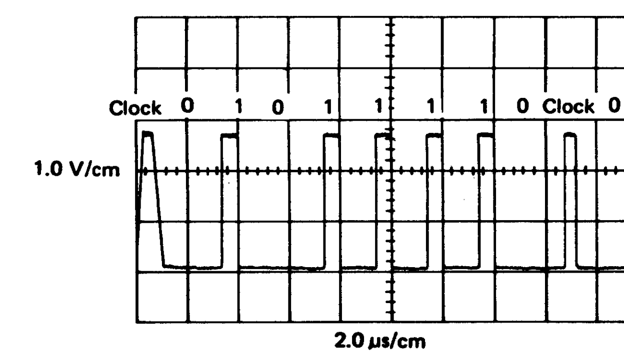




Note: Use Tektronix 453, 454, or similar oscilloscope with x10 probes.

Channel A sweep mode	Normal
Channel A level	+
Channel A coupling	dc
Channel A slope	+
Channel A source	External
Trigger	Normal
Mode	Channel 1
Channel 1 volts/division	1.0 V/cm
Channel 1 input	dc
Times per division	2 µs/cm
Connect channel 1 to	+Drive data D
Connect trigger to	+Index test pin C
Observe:	Clock or data pulses every 2 to 4 µs. Pulse duration should be between 100 and 500 ns. Pulse amplitude should be between 2.4 and 4.2 volts.

Drive Data
Bit Pattern: Hex 'E5E5'
Example: 0101111001



DA500 Adjustment, Removal, and Replacement Information, Part 1

The DA500 and DA600 sections contain information relating to adjustment, removal, and replacement of diskette storage components. Because of size, the information and procedures are divided as follows:

- DA510 through DA515 discuss information relating to diskette protection, removal, and insertion, and contain common hardware information such as special tools and drive assembly locations. They also contain the procedure used to place the drive in the service position and the procedure used to remove and replace it.
- DA520 through DA670 contain specific adjustment, removal, and replacement information.

DANGER

- **The unit that contains the diskette drive supplies the ac and dc power to the drive. The diskette connector terminals have voltage present when the drive motor turns.**
- **Motor and solenoid cases become hot after continuous use. Wait until the parts cool before servicing.**
- **To prevent personal injury on 60-Hz machines having diskette drive motor cases with two large holes (see DA582), ensure that the holes are located under the bracket.**

Caution:

- **Do not use IBM or any other cleaning fluid on or near plastic parts.**
- **Diskette drives can be damaged if they are not operated or serviced properly.**
- **Never use damaged diskettes (see DA511) as they can cause data errors, equipment errors, or head damage.**
- **The head/carriage assembly, head timing block, and drive hub pulley are adjusted and tested at the factory.**
  - **The head/carriage assembly can be replaced in the field, but do not repair or clean any part of the assembly.**
  - **The head timing block and the drive hub pulley are not field-replaceable.**
- **Do not use an ohmmeter to measure head resistance.**
- **Perform the diskette drive adjustments with the drive positioned vertically as it mounts in the machine (side-mounted position).**
- **The following routines destroy data on the cylinders indicated:**

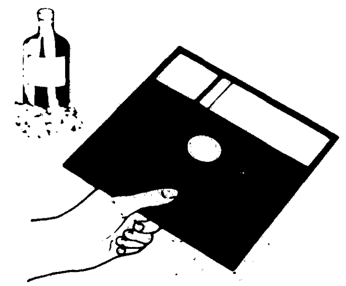
Routine	*Cylinder(s)*
12	**74**
13	**74**
14	**73**
15	**73**
16	**72**
17	**72**
18	**74**
19	**74**
20	**73**
21	**73**
22	**72**
23	**72**
25	**72**
26	**72, 73, 74**
28	**1, 50, 72**

- **Use only the correct top card connector part numbers on the DA1 and DA2 cards (see DA111).**

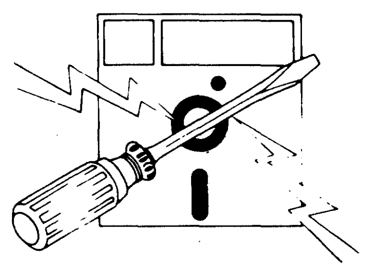
DA510 General Information

DA511 Diskette Protection

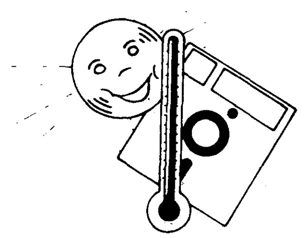
Do not touch or attempt to clean diskette surfaces. Contaminated diskettes will not operate correctly.



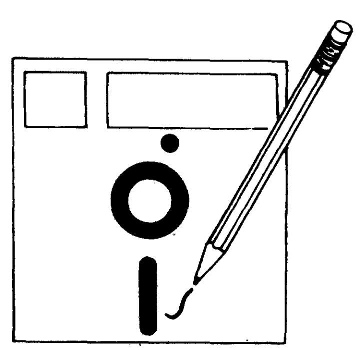
Do not place diskettes near any magnetic field. Data can be lost when exposing a diskette to magnetism.



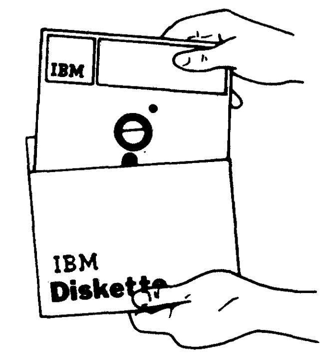
Do not expose diskettes either to heat greater than 51.5°C (125°F) or to direct sunlight.



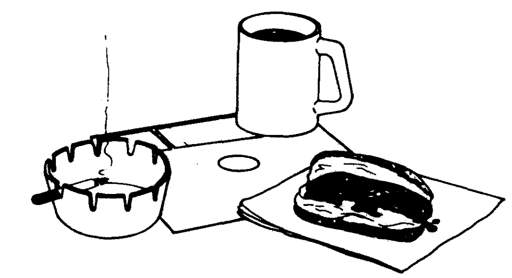
Do not write outside the label area on diskettes.



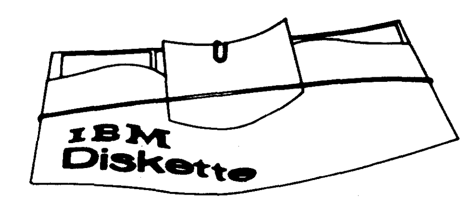
Always return a diskette to its protective envelope after removing the diskette from the drive.



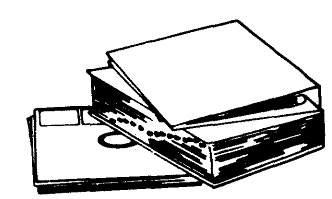
Do not place diskettes near smoke or other objects that could cause diskette contamination.



Do not use clips or rubber bands on diskettes.



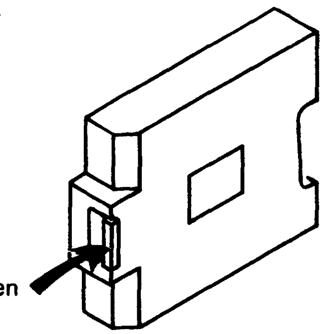
Do not place heavy books on diskettes.



DA512 Diskette Insertion/Removal

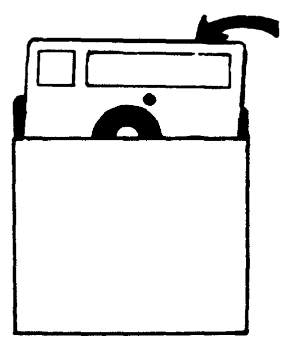
Use the following diskette insertion/removal procedure to prevent damage to the diskette or the diskette drive:

1. Open cover.

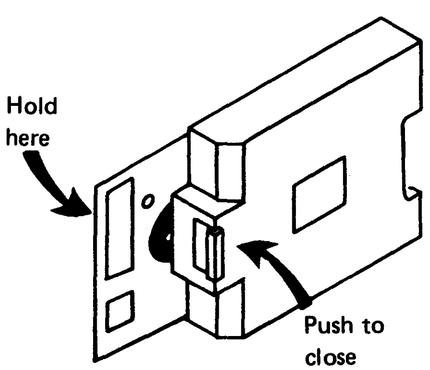


2. Remove diskette from the envelope. Hold the diskette by upper edge.

Caution: Do not insert a damaged diskette.



3. Slide the diskette into the 53FD.

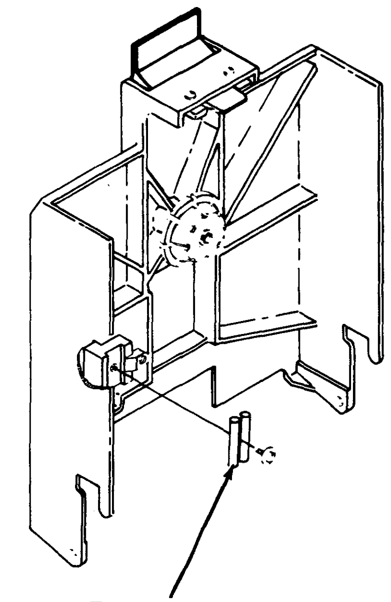


4. Close the cover after fully inserting the diskette.
5. Place the empty envelope in a clean storage area.

To remove the diskette, reverse the above procedure.

DA513 Tools

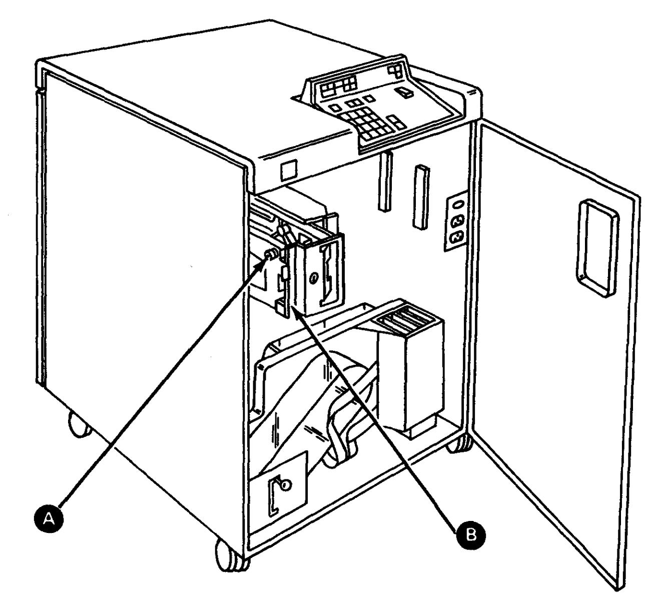
Two timing pins (PN 5562019) are located inside the cover assembly as shown below. Use them to align the stepper motor shaft and pulley to the base casting (multiple procedures) and also to align the LED and PTX assemblies (DA651).



DA514 Diskette Drive Assembly Service Position

1. Open the front cover and the access cover.
2. Loosen the diskette drive retaining screw A.
3. Slide the diskette drive forward until it detents.

To place the diskette drive in the operate position, reverse the above procedure.



DA515 Diskette Drive Assembly Removal and Installation

1. Turn off machine power at the operator panel.
2. Remove the service position stop screw (DA514 B).
3. Place the diskette drive in the service position (DA514).
4. If you do not need power, disconnect the cables and remove the diskette drive assembly from the machine.

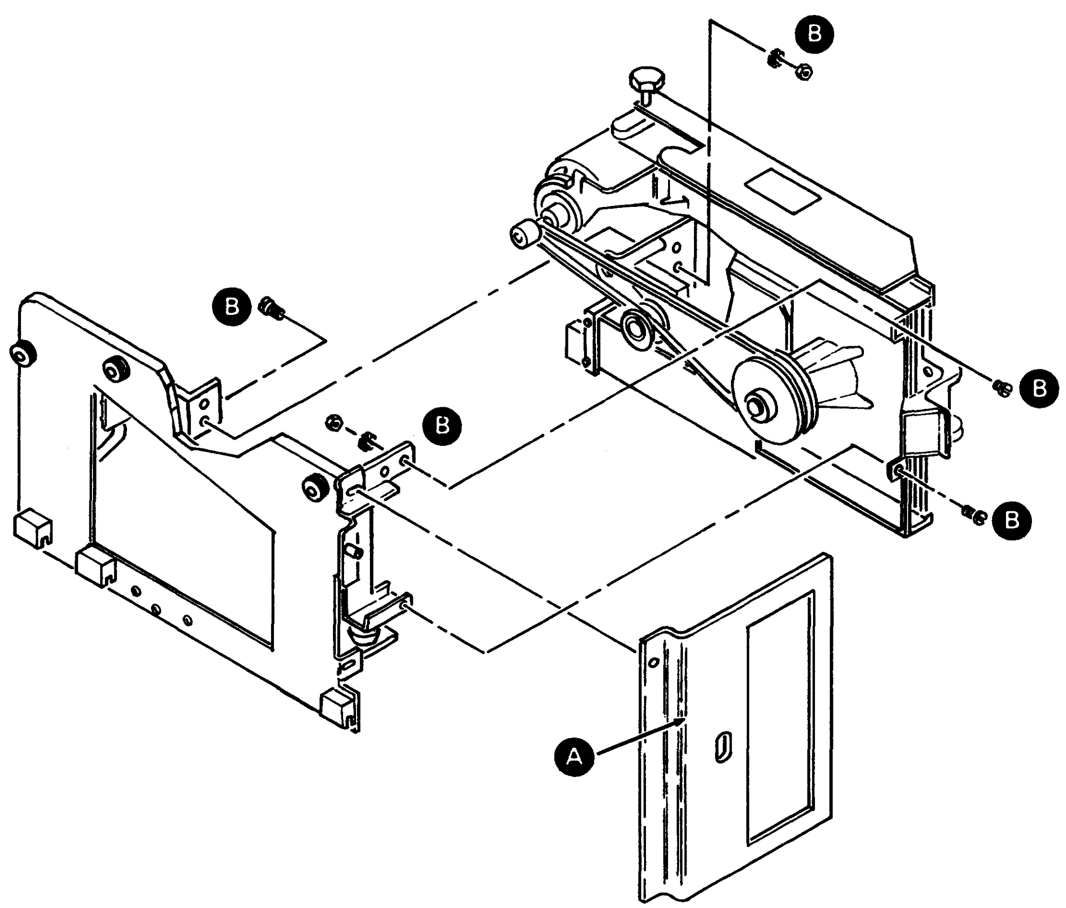
DANGER
Line voltage is always present at the power connector with machine power on.

5. If you need power, remove the cable clamps on the machine frame and move the diskette drive assembly to a convenient location.

To reinstall the diskette drive assembly, reverse the above procedure; to remove the drive from its mounting bracket, go to step 6.

6. Remove the diskette panel cover A.
7. Remove the three screws, washers and nuts B that attach the diskette drive to the mounting bracket and remove the diskette drive. Retain the mounting hardware.

To reinstall a diskette drive to its mounting bracket, reverse steps 6 and 7.



DA516 Diskette Drive Assembly Major Components

The following describes and illustrates the major 53FD drive components. The referenced sections contain service check, adjustment, removal, or replacement information.

Cover Assembly Components

Opening the diskette drive cover to insert a diskette disengages the cover latch assembly. Closing the cover engages the latch assembly, and the drive collet then centers and holds the diskette against the drive hub.

A Cover latch assembly (DA530)
B Drive collet (DA540)

Index Detection Components

The LED (light source) and the PTX (light sensor) detect the index hole.

C Light-emitting diode (LED) assembly (DA650)
D Phototransistor (PTX) assembly (DA660)

Diskette Drive Control Card (DA3)

The DA3 card contains the drive logic for the stepper motor, read head solenoid, and write and erase functions, as well as the amplifiers for the read heads and index sensing logic.

E DA3 (DA670)

AC Drive Components

Used to turn the diskette at 360 rpm.

F Drive motor (DA580)
G Drive belt (DA570)
H Drive belt idler assembly (DA590)
J Drive motor pulley (DA580)

Head Load Components

The solenoid causes the bail to load the heads.

K Head load solenoid (DA560)
L Head load bail (DA560)

Read-Write Components

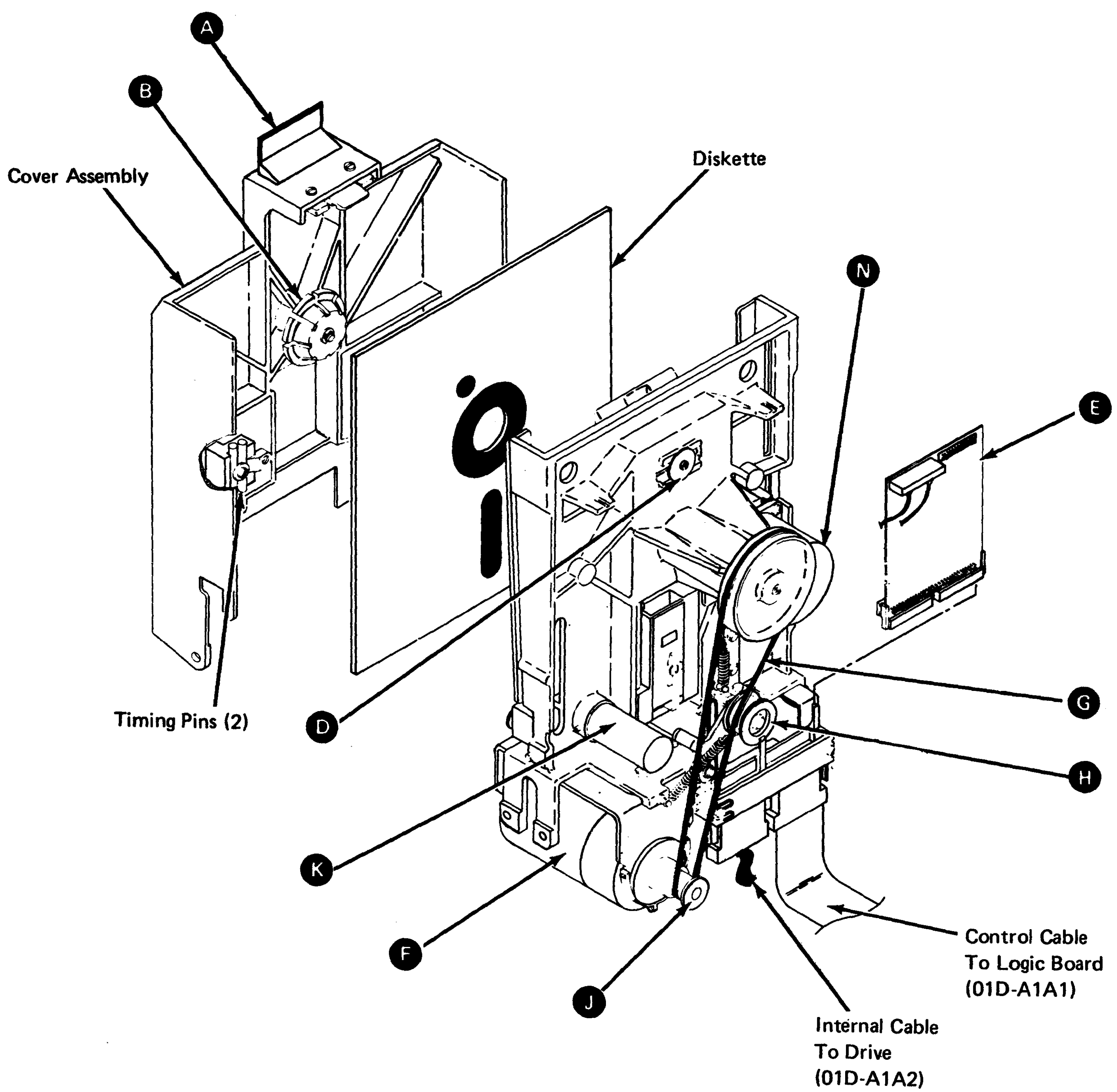
Two read/write heads, which perform the read, write, and erase functions, move under control of the stepper motor and are mounted on the head/carriage assembly.

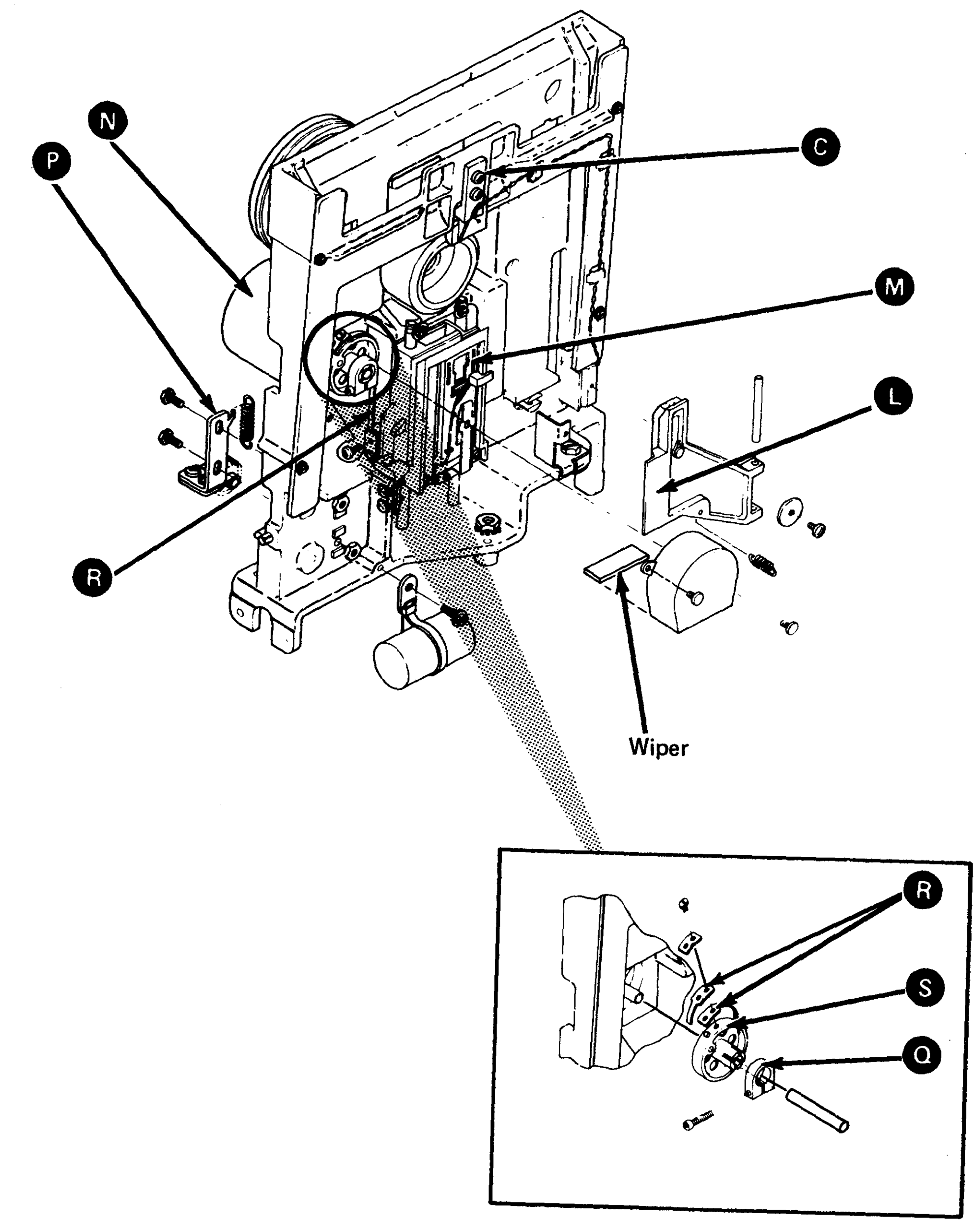
M Head/carriage assembly (DA550)

Stepper Drive Components

Access pulses cause the stepper motor shaft and associated components to turn in either direction, which moves the head/carriage assembly across the diskette surface.

N Stepper motor (DA601/DA602)
P Stepper drive band idler assembly (DA630)
Q Stepper motor pulley clamp (DA610)
R Stepper drive band (DA620)
S Stepper motor pulley (DA610)


A
B
Cover Assembly
Diskette
N
E
Timing Pins (2)
D
G
H
K
F
J
Control Cable
To Logic Board
(01D-A1A1)
Internal Cable
To Drive
(01D-A1A2)


N
P
C
M
L
R
Wiper
R
S
Q

DA520 Drive Cover Assembly

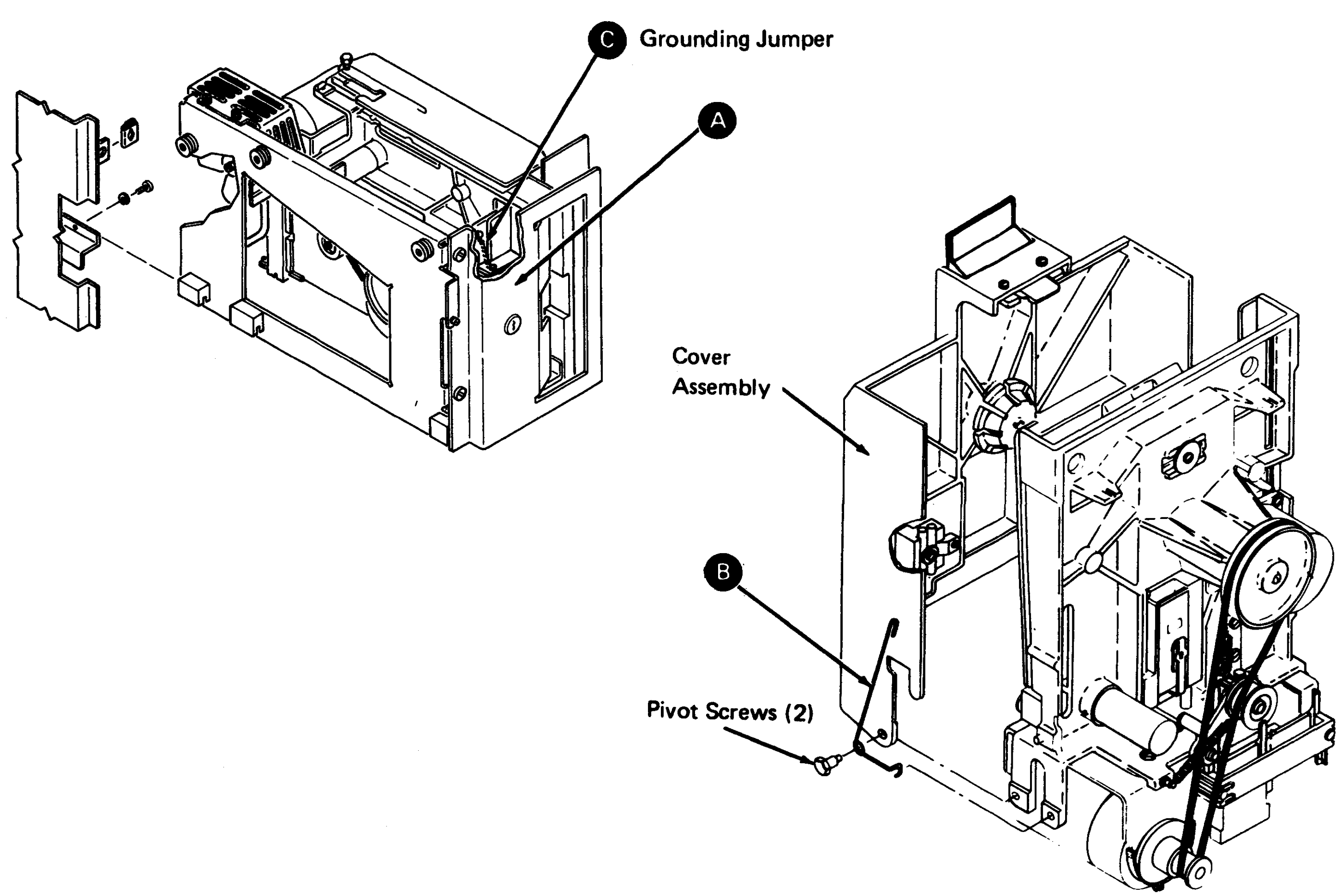
DA521 Drive Cover Assembly Removal

1. Remove the diskette panel cover A.
2. Open the drive cover assembly.
3. Disconnect the spring B from the cover.
4. Loosen the two pivot screws but do not remove them.
5. While holding the cover assembly, remove the pivot screws and spring, and lift the cover assembly away from the diskette drive.

Note: *Ensure that a grounding jumper C is installed near the front of the machine between the drive assembly and the drive mounting plate.*

DA522 Drive Cover Assembly Installation

1. Install one end of the spring B in the casting and align the cover assembly with the casting mounting holes.
2. Reinstall and firmly tighten the two pivot screws.
3. Connect the other end of the spring to the cover.
4. Close the drive cover assembly to ensure that it latches.



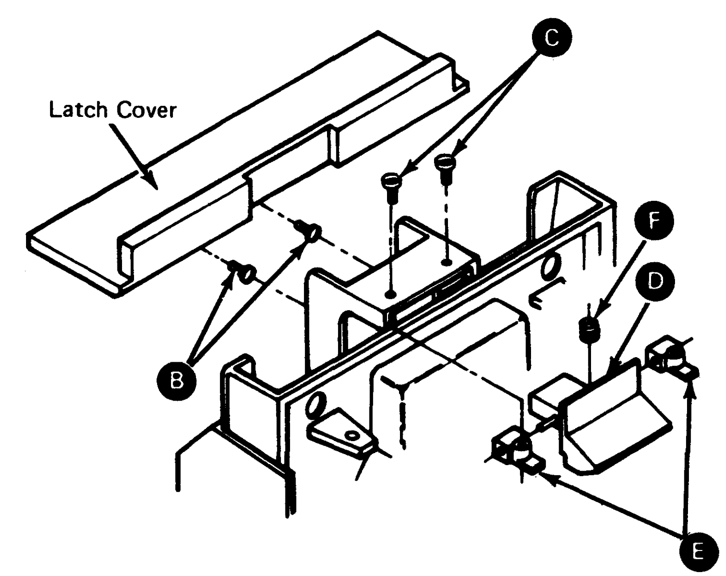
DA530 Cover Latch Assembly

DA531 Cover Latch Assembly Removal

1. Remove the diskette panel cover A (DA520).
2. Loosen the two screws B and remove the latch cover.
3. Open the drive cover and remove the two latch mounting screws C.
4. Carefully remove the latch D and the two pivots E without losing the spring F by pulling the latch toward the rear of the cover assembly.

DA532 Cover Latch Assembly Installation

1. Place the latch D into the cover assembly, then place the two pivots E and the spring F in position.
2. Reinstall the two latch mounting screws C.
3. Reinstall the latch cover and tighten the two screws B.
4. Reinstall the diskette panel cover A (DA520).
5. Close the drive cover assembly to ensure that it latches.



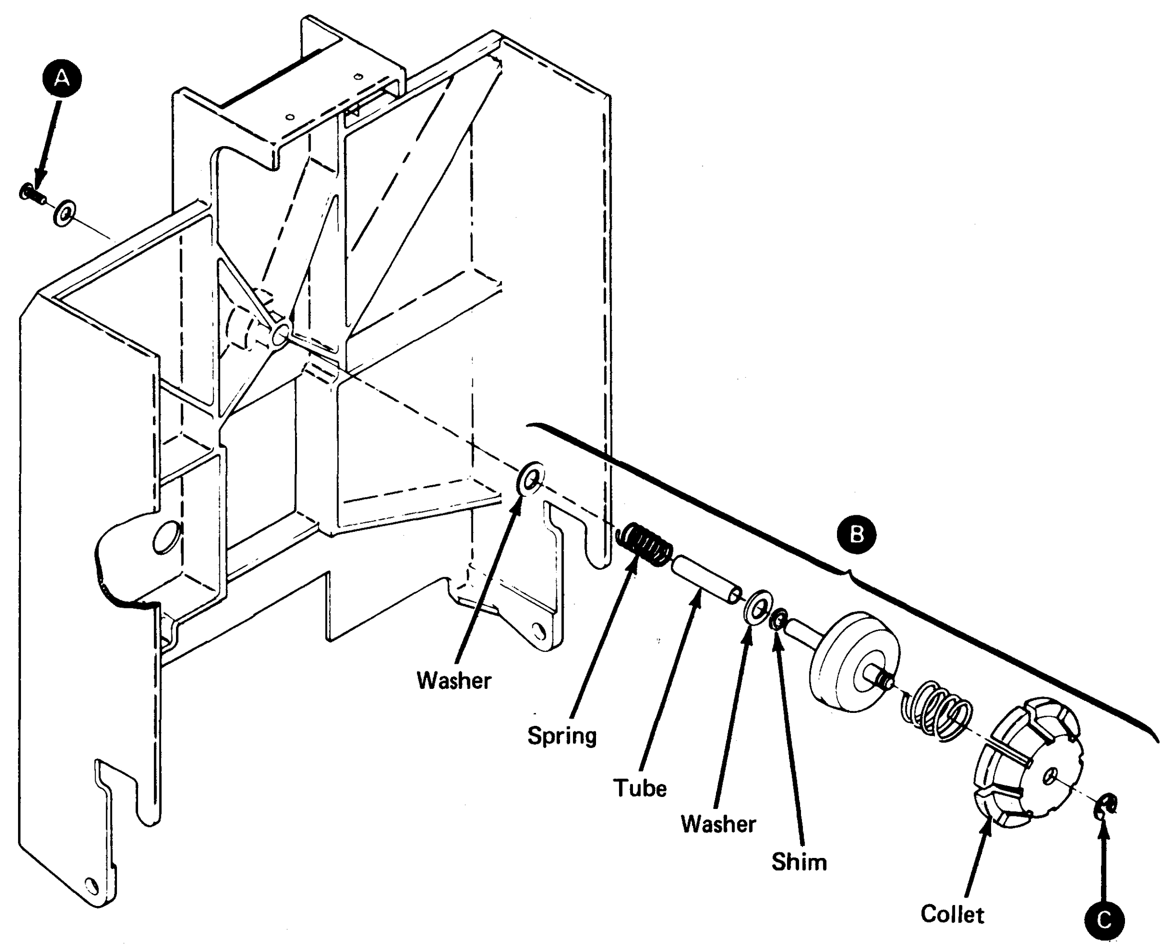
DA540 Drive Collet and Assembly

DA541 Drive Collet and Assembly Removal

1. Remove the drive cover assembly (DA521).
2. Remove the collet assembly mounting screw A.
3. Remove the collet assembly B.
4. Remove the clip C and remove the collet.

DA542 Drive Collet and Assembly Installation

1. Reinstall the collet and clip C.
2. Reinstall the remaining parts on the collet shaft in the order shown B.
3. Reinstall the collet assembly and the mounting screw A.
4. Reinstall the drive cover assembly (DA522).



DA550 Head/Carriage Assembly

DA551 Head/Carriage Assembly Service Check

To perform a head/carriage service check, you must electrically move and detent the head/carriage between cylinders 39 and 40. You can either jumper certain diskette signals or select a diskette storage test routine. As each method uses a common introductory procedure, begin with the following paragraph.

Head/Carriage Service Check, Common Procedure

Caution: The head/carriage assembly timing block is adjusted and tested at the factory. If the timing block holding screws are loosened, the entire diskette drive assembly must be replaced. Do not clean or attempt to repair the head/carriage assembly.

Note: *The head/carriage service check must be performed with the diskette drive in the same position as when installed or the adjustment can be wrong.*

1. Place the diskette drive in the service position (DA514) and leave machine power on.
2. Unplug the drive motor power connector.

DANGER
Line voltage is always present at the power connector with machine power on.

3. Remove the drive cover assembly (DA521).
4. Remove the wiper assembly.
5. Insert a clean strip of paper between the heads to prevent the head surfaces from touching.

To continue, the head/carriage must be moved between cylinders 39 and 40. You can do this either under program control with diskette test Routine 30 (DA212) using MD diskette 03, or by manually jumpering test points on the diskette drive control (DA3) card. Go to the paragraph that describes the procedure that you want to use.

Head/Carriage Service Check Using Diskette Test Routine 30

1. Load MD diskette 03, use the Free-Lance Utility, and select diskette storage test Routine 30 (DA200).

Note: *The PA41 and PA43 stops indicate that the head/carriage is at cylinder 40; PA42 indicates cylinder 39. See DA212 for the routine description.*

2. Using Routine 30, position the head/carriage at cylinder 40 (PA41 or PA43 stop).
3. Use a timing pin, located inside the cover assembly, to determine the stepper motor pulley position. Does the timing pin pass freely through the hole in the stepper motor pulley and into the hole in the casting A ?
   a. If YES, the pulley position is correct. Remove the timing pin and go to step 4.
   b. If NO, perform the head/carriage adjustment (DA552) beginning with step 3 of "Head/Carriage Adjustment Using Diskette Test Routine 30".
4. Using Routine 30, position the head/carriage at cylinder 39 (PA42 stop) and then reposition it at cylinder 40 (PA43).
5. Visually verify the stepper motor pulley position. Do not use a timing pin. Are the holes in the stepper motor pulley and the casting aligned?
   a. If YES, the pulley position is correct. Go to step 6.
   b. If NO, perform the head/carriage adjustment (DA552) beginning with step 3 of "Head/Carriage Adjustment Using Diskette Test Routine 30".
6. Verify that a 0.508 mm (0.020-inch) gap exists between the head/carriage timing pointer and the timing block B as follows:
   a. While carefully inserting a 0.495 mm (0.0195-inch) thickness gauge, visually check that the head/carriage does not move.
   b. While carefully inserting a 0.533 mm (0.021-inch) thickness gauge, visually check that the head/carriage moves slightly.

Note: *Because of stepper motor torque, you can perform step 6 only once. If necessary to perform this step again, return to step 4.*

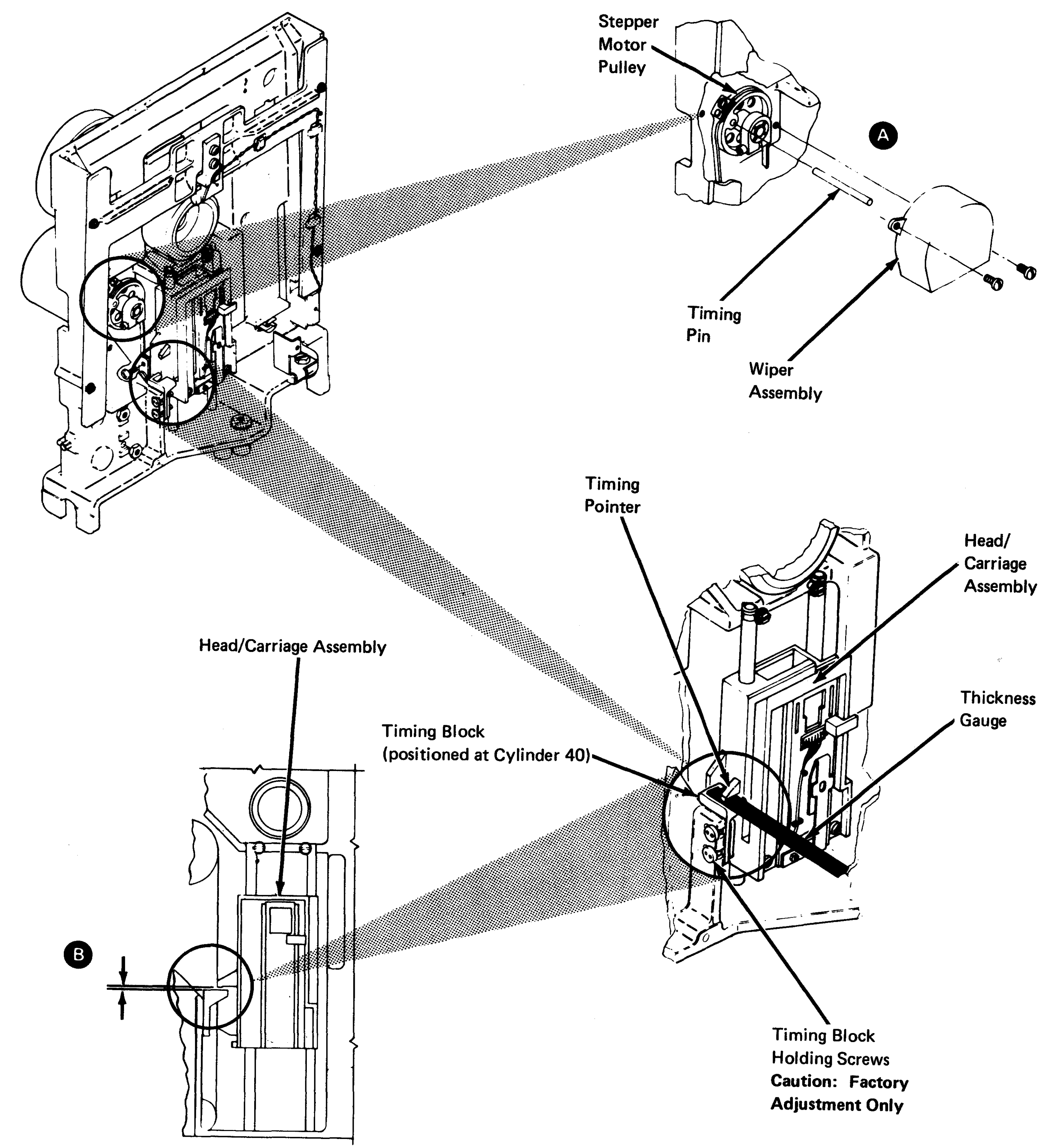
7. Is the adjustment correct?
   a. If YES, install the wiper assembly.
   b. If NO, perform the head/carriage adjustment (DA552) beginning with step 8 of "Head/Carriage Adjustment Using Diskette Test Routine 30".
8. Are you installing a new head/carriage assembly?
   a. If YES, perform the head load solenoid and bail assembly service check (DA561) beginning with step 5.
   b. If NO, install the drive cover assembly (DA522) and connect the drive motor power connector.

Head/Carriage Service Check Using a Jumper

1. Turn off machine power at the operator panel and remove both the DA1 and DA2 diskette adapter cards (see DA111 for locations). This prevents activating the stepper motor access lines from an external source.
2. Position the head/carriage assembly at about cylinder 40 by manually turning the stepper motor pulley until the head/carriage timing pointer is just above the timing block.
3. Turn on machine power at the operator panel.
4. Install a jumper on the DA3 card from TPA13 (Ground) to THP11 (-Align Access 0). See Figure DA420-2 for test point locations. This step electrically detents the head/carriage at cylinder 40.
5. Use a timing pin, located inside the cover assembly, to determine the stepper motor pulley position. Does the timing pin pass freely through the hole in the stepper motor pulley and into the hole in the casting A ?
   a. If YES, the pulley position is correct. Remove the timing pin and go to step 6.
   b. If NO, perform the head/carriage adjustment (DA552) beginning with step 6 of "Head/Carriage Adjustment Using A Jumper".
6. Move the jumper from THP11 to TPB10 (MC-3) to position the head/carriage at cylinder 39; then move the jumper from TPB10 back to THP11 to reposition the head/carriage at cylinder 40.
7. Visually verify the stepper motor pulley position. Do not use a timing pin. Are the holes in the stepper motor pulley and the casting aligned?
   a. If YES, the pulley position is correct. Go to step 8.
   b. If NO, perform the head/carriage adjustment (DA552) beginning with step 5 of "Head/Carriage Adjustment Using a Jumper".
8. Verify that a 0.508-mm (0.020-inch) gap exists between the head/carriage timing pointer and the timing block B as follows:
   a. While carefully inserting a 0.495-mm (0.0195-inch) thickness gauge, visually check that the head/carriage does not move.
   b. While carefully inserting a 0.533-mm (0.021-inch) thickness gauge, visually check that the head/carriage moves slightly.

Note: *Because of stepper motor torque, you can perform step 8 only once. If necessary to perform this step again, return to step 6.*

9. Is the adjustment correct?
   a. If YES, remove the jumper, reinstall the DA1 and DA2 diskette adapter cards (DA111), and install the wiper assembly.
   b. If NO, perform the head/carriage adjustment (DA552) beginning with step 9 of "Head/Carriage Adjustment Using a Jumper".
10. Are you installing a new head/carriage assembly?
    a. If YES, perform the solenoid and bail service check (DA561) beginning with step 5.
    b. If NO, install the drive cover assembly (DA522) and connect the drive motor power connector.



DA552 Head/Carriage Assembly Adjustment

To adjust a head/carriage assembly, you must electrically move and detent the head/carriage between cylinders 39 and 40. You can either jumper certain diskette signals or select a diskette storage test routine. As each method uses a common introductory procedure, begin with the following paragraph.

Head/Carriage Adjustment, Common Procedure

Caution: The head/carriage assembly timing block is adjusted and tested at the factory. If the timing block holding screws are loosened, the entire diskette drive assembly must be replaced. Do not clean or attempt to repair the head/carriage assembly.

Note: *The head/carriage service check must be performed with the diskette drive in the same position as when installed or the adjustment can be wrong.*

1. Place the diskette drive in the service position (DA514) and leave machine power on.
2. Unplug the drive motor power connector.

DANGER
Line voltage is always present at the power connector with machine power on.

3. Remove the drive cover assembly (DA521).
4. Remove the wiper assembly.
5. Insert a clean strip of paper between the heads to prevent the head surfaces from touching.

To continue, the head/carriage must be moved between cylinders 39 and 40. You can do this either under program control with diskette test Routine 30 (DA212) using MD diskette 03, or by manually jumpering test points on the diskette drive control (DA3) card. Go to the paragraph that describes the procedure that you want to use.

Head/Carriage Adjustment Using Diskette Test Routine 30

1. Load MD diskette 03, use the Free-Lance Utility, and select diskette storage test Routine 30 (DA200).

Note: *The PA41 and PA43 stops indicate that the head/carriage is at cylinder 40; PA42 indicates cylinder 39. See DA212 for the routine description.*

2. Using Routine 30, position the head/carriage at cylinder 40 (PA41 or PA43 stop).
3. Measure the gap A between the stepper motor pulley and the casting. Write the measurement here.

   The gap is ________.
4. Loosen the clamp screw B enough so the stepper motor shaft can turn inside the pulley.
5. Ensure that the head/carriage is still at cylinder 40 (PA41 or PA43 stop).
6. Use a timing pin, located inside the cover assembly, and insert in through the hole in the stepper motor pulley and into the hole in the casting.
7. Make gap A the same as the gap recorded in step 3, and tighten the clamp screw B . Ensure that the timing pin still passes freely through the stepper motor pulley and into the hole in the casting; then remove the timing pin.
8. Loosen the two screws C that clamp the stepper drive band to the head/carriage assembly.
9. Using Routine 30, position the head/carriage at cylinder 39 (PA42 stop) and then reposition it at cylinder 40 (PA43).
10. Visually verify the stepper motor pulley position. Do not use a timing pin. Are the holes in the stepper motor pulley and the casting aligned?
    a. If YES, the pulley position is correct. Go to step 11.
    b. If NO, repeat steps 4 through 10.
11. Insert a 0.508-mm (0.020-inch) thickness gauge between the head/carriage timing pointer and the timing block. Put light finger pressure on the head/carriage to hold the thickness gauge in place.
12. Tighten the two band clamping screws C , while ensuring that the drive band remains straight.
13. Perform the head/carriage service check (DA551) beginning with step 4 of "Head/Carriage Service Check Using Diskette Test Routine 30".

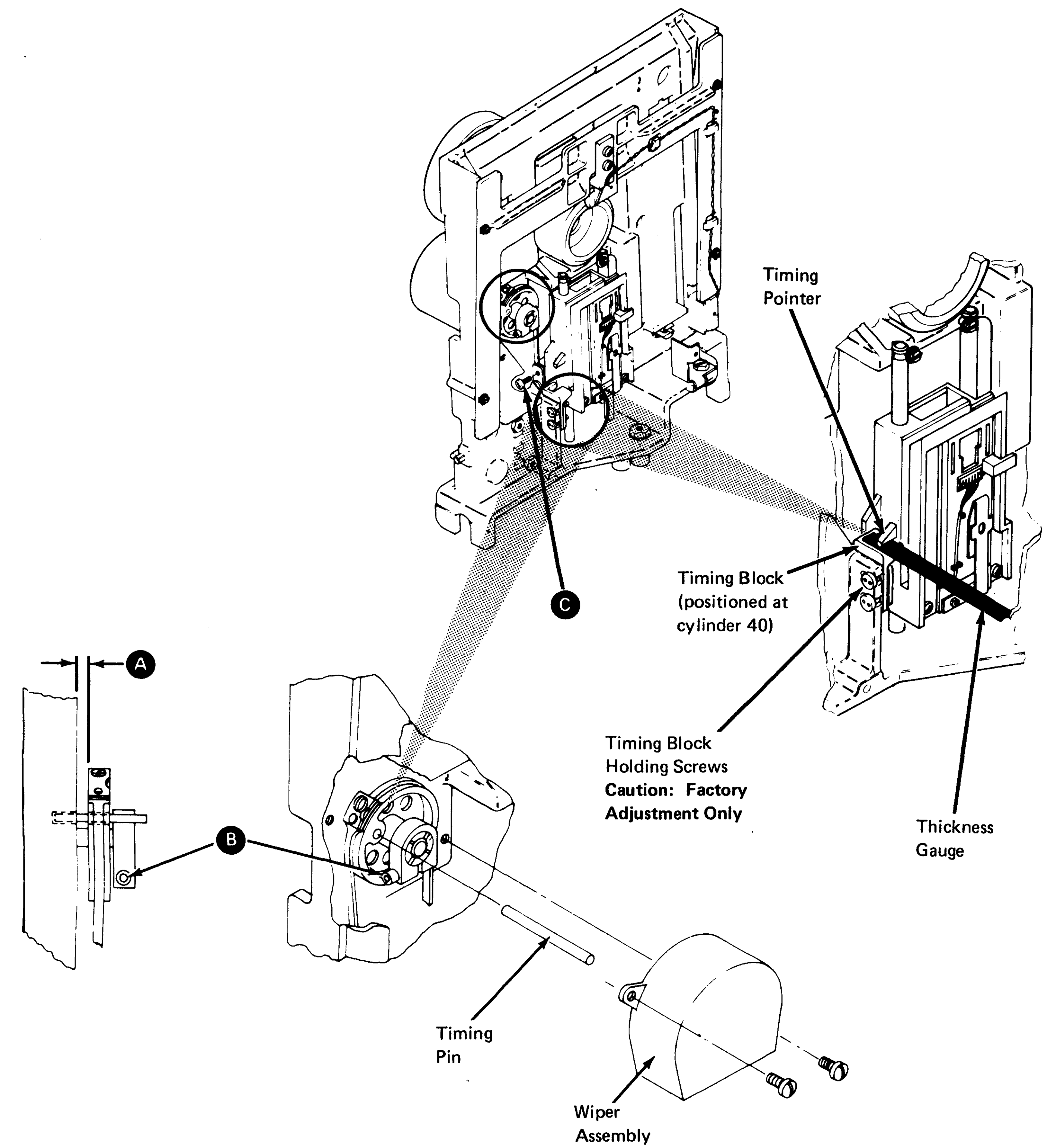
Head/Carriage Adjustment Using a Jumper

1. Turn off machine power at the operator panel and remove both the DA1 and DA2 diskette adapter cards (see DA111 for locations). This prevents activating the stepper motor access lines from an external source.
2. Position the head/carriage assembly at about cylinder 40 by manually turning the stepper motor pulley until the head/carriage timing pointer is just above the timing block.
3. Turn on machine power at the operator panel.
4. Install a jumper on the DA3 card from TPA13 (Ground) to THP11 (-Align Access 0). See Figure DA420-2 for test point locations. This step electrically detents the head/carriage at cylinder 40.
5. Measure the gap A between the stepper motor pulley and the casting. Write the measurement here.

   The gap is __________.
6. Loosen the clamp screw B enough so the stepper motor shaft can turn inside the pulley.
7. Use a timing pin, located inside the cover assembly, and insert in through the hole in the stepper motor pulley and into the hole in the casting.
8. Make gap A the same as the gap recorded in step 5, and tighten the clamp screw B . Ensure that the timing pin still passes freely through the stepper motor pulley and into the hole in the casting; then remove the timing pin.
9. Loosen the two screws C that clamp the stepper drive band to the head/carriage assembly.
10. Move the jumper from THP11 to TPB10 (MC-3) to position the head/carriage at cylinder 39; then move the jumper from TPB10 back to THP11 to reposition the head/carriage at cylinder 40.
11. Visually verify the stepper motor pulley position. Do not use a timing pin. Are the holes in the stepper motor pulley and the casting aligned?

    a. If YES, the pulley position is correct. Go to step 12.

    b. If NO, repeat steps 6 through 11.
12. Insert a 0.508-mm (0.020-inch) thickness gauge between the head/carriage timing pointer and the timing block. Put light finger pressure on the head/carriage to hold the thickness gauge in place.
13. Tighten the two band clamping screws C, while ensuring that the drive band remains straight.
14. Perform the head/carriage service check (DA551) beginning with step 6 of "Head/Carriage Service Check Using a Jumper".



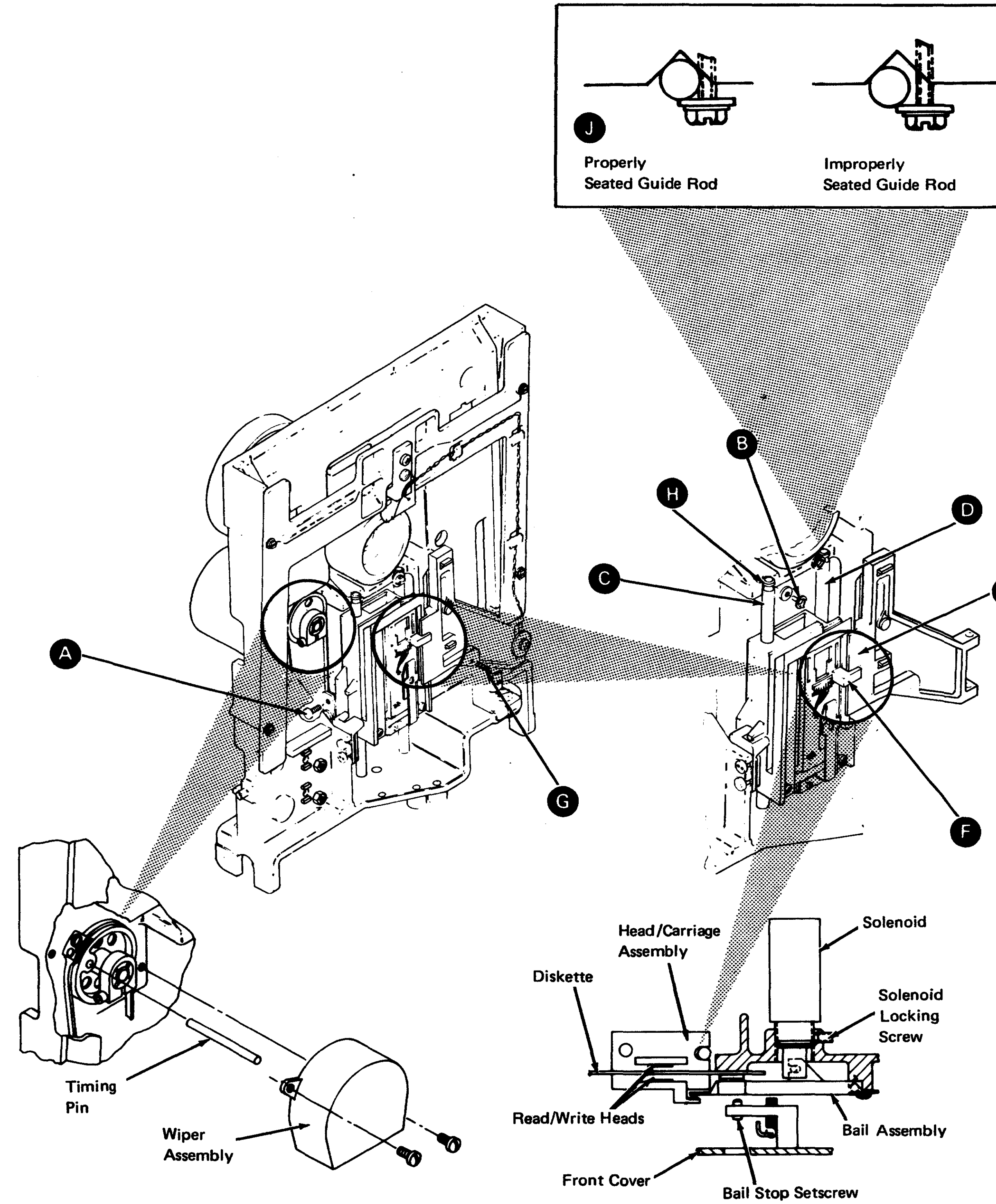
DA553 Head/Carriage Assembly Removal

1. Turn off machine power at the operator panel.
2. Remove the diskette drive from the machine and disconnect the cables, including the drive motor power connector (DA515).
3. Remove the drive cover assembly (DA521).
4. Remove the wiper assembly.
5. Carefully remove the head cable from the diskette drive control (DA3) card. Remember the cable path for the installation procedure.
6. Position the head/carriage assembly at about cylinder 40 by manually turning the stepper motor pulley until the head/carriage timing pointer is just above the timing block. The hole in the stepper motor pulley should be nearly aligned with the hole in the casting.
7. Remove the two screws A and the clamp that attach the stepper drive band to the head/carriage; then place the head/carriage at the lower limit (cylinder 00).
8. Loosen the screw B and remove the guide rod C .
9. Carefully lift and turn the head/carriage assembly to remove it from the other guide rod D .

DA554 Head/Carriage Assembly Installation

Caution: When installing the head/carriage assembly, ensure that the bail E is under the carriage arm tab F . Also, remember to install the bail return spring G .

1. Carefully reinstall the head/carriage assembly on one guide rod D and place the head/carriage at the lower limit (cylinder 00).
2. Reinstall the other guide rod C and tighten the screw B . Ensure that the guide rod notch H is aligned with the screw and is seated as shown J .
3. Reposition the head/carriage assembly at about cylinder 40 by manually turning the stepper motor pulley until the head/carriage timing pointer is just above the timing block. Insert a timing pin through the stepper motor pulley and into the hole in the casting.
4. Reinstall the clamp and the two screws A that attach the stepper drive band to the head/carriage, but do not tighten them; then remove the timing pin.
5. Carefully reposition the head cable and replug the connector into the diskette drive control (DA3) card.
6. Reinstall (DA515) and place the diskette drive in the service position (DA514); then reconnect all cables except the drive motor power connector.
7. Turn on machine power at the operator panel.
8. Perform the head/carriage adjustment (DA552) beginning with step 5 of the "Head/Carriage Adjustment, Common Procedure".



DA560 Head Load Solenoid and Bail Assembly

DA561 Solenoid and Bail Assembly Service Check

1. Place the diskette drive in the service position (DA514) and leave machine power on.
2. Unplug the drive motor power connector.

DANGER
Line voltage is always present at the power connector with machine power on.

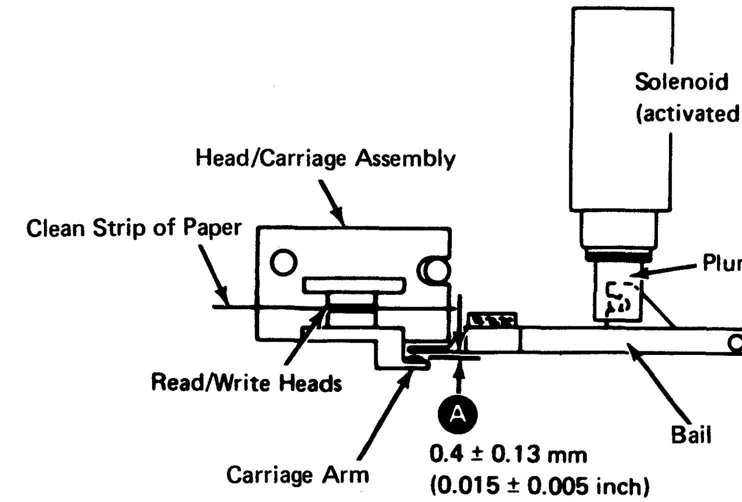
3. Remove the drive cover assembly (DA521).
4. Insert a clean strip of paper between the heads to prevent the head surfaces from touching.
5. Install a jumper on the DA3 card from TPA13 (Ground) to TPB13 (-Head Load) to activate the head load solenoid. See Figure DA420-2 for test point locations.

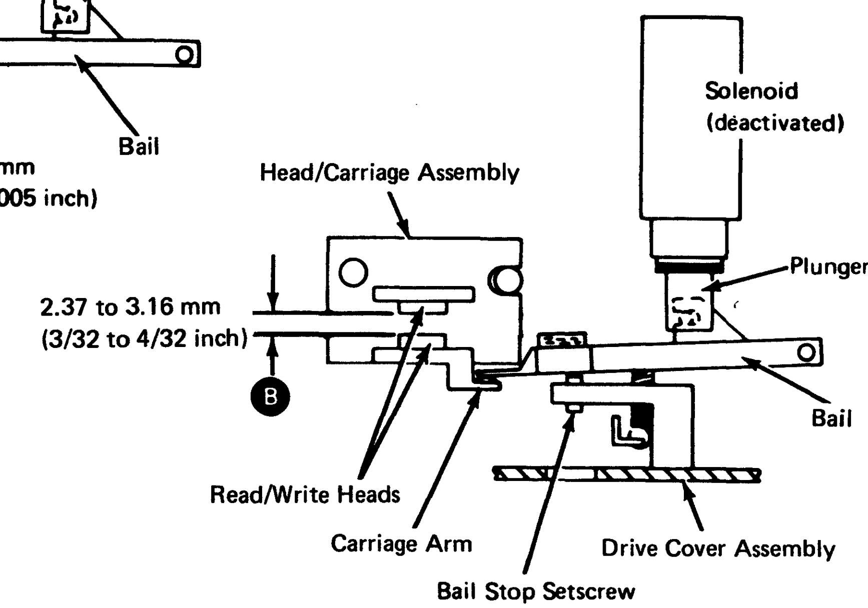
DANGER
The solenoid case becomes hot after continuous use.

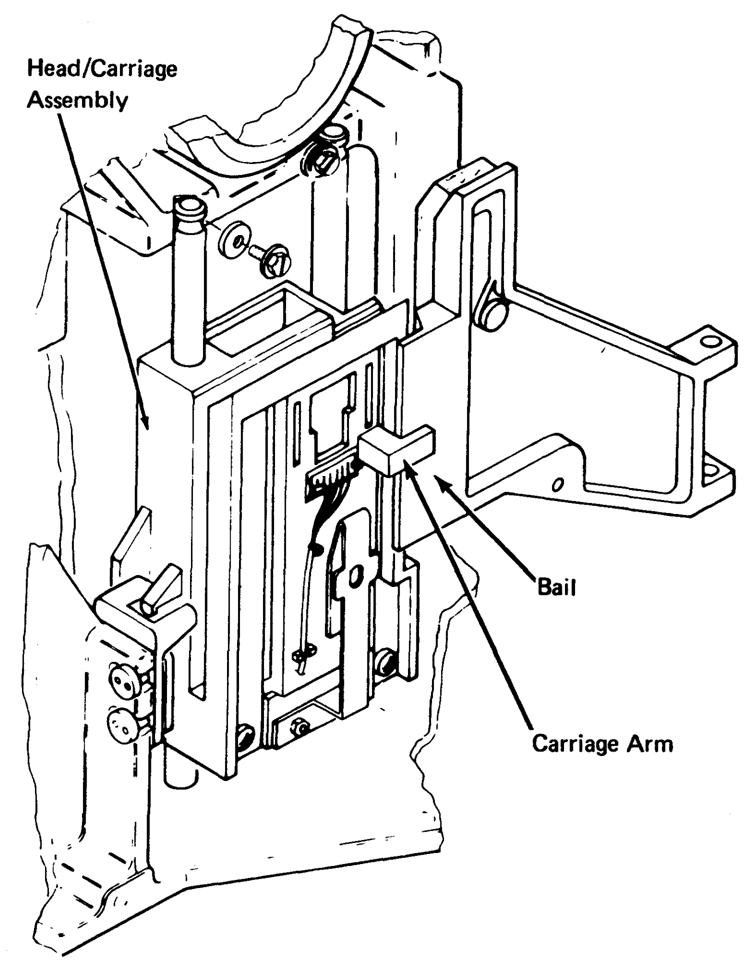
6. Check for a gap A of 0.4 ± 0.13 mm (0.015 ± 0.005 inch) between the bail and the carriage arm for all head/carriage movement from cylinder 00 to cylinder 76.

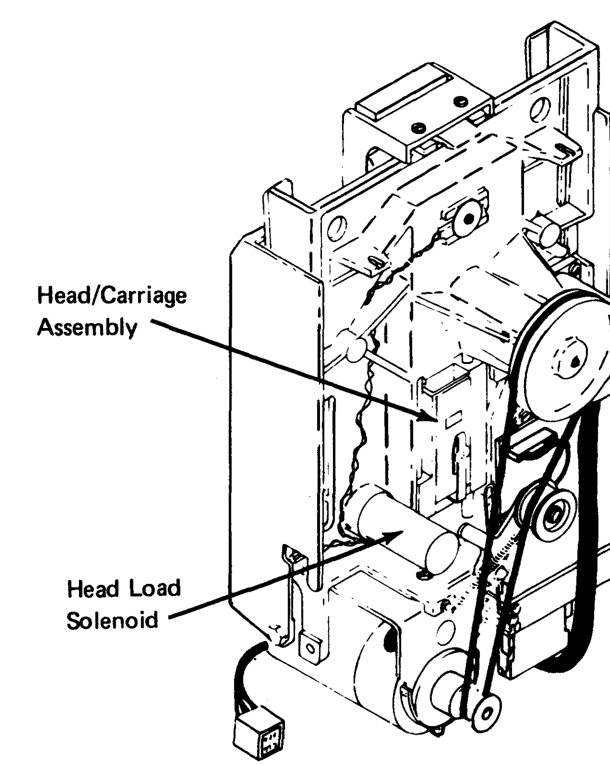
   Note: *You can manually move the head/carriage assembly from cylinder 00 to cylinder 76 by turning off machine power. Turn power on after checking the gap.*

7. Is the gap correct?
   a. If YES, go to step 8.
   b. If NO, perform the solenoid and bail adjustment (DA562) beginning with step 6.
8. Remove the jumper.
9. Remove the paper between the heads.
10. Reinstall the drive cover assembly (DA522).
11. With the head load solenoid deactivated and the drive cover closed, visually check for a gap B of approximately 2.37 to 3.16 mm (3/32 to 4/32 inch) between the head surfaces. This gap cannot be measured.
12. Is the gap correct?
    a. If YES, go to step 13.
    b. If NO, again place the paper between the heads, turn the bail stop setscrew clockwise until the heads just touch, turn the setscrew counterclockwise one complete turn, then remove the paper.
13. Turn off machine power at the operator panel and connect the drive motor power connector.









DA562 Solenoid and Bail Assembly Adjustment

1. Place the diskette drive in the service position (DA514) and leave machine power on.
2. Unplug the drive motor power connector.

DANGER
Line voltage is always present at the power connector with machine power on.

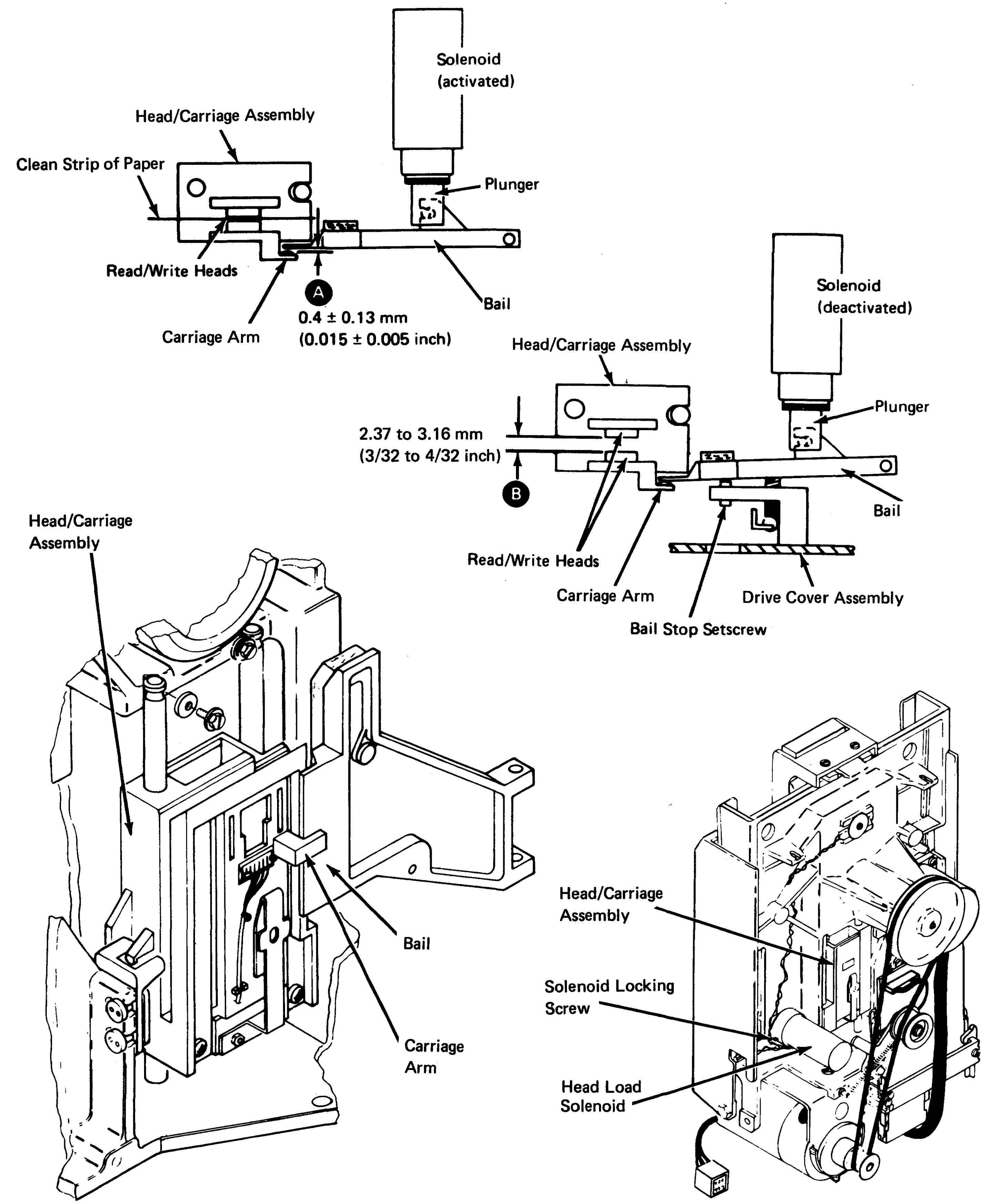
3. Remove the drive cover assembly (DA521).
4. Insert a clean strip of paper between the heads to prevent the head surfaces from touching.
5. Install a jumper on the DA3 card from TPA13 (Ground) to TPB13 (-Head Load) to activate the head load solenoid. See Figure DA420-2 for test point locations.

DANGER
The solenoid case becomes hot after continuous use.

6. Loosen the solenoid locking screw.
7. Turn the solenoid to obtain a gap A of 0.4 ± 0.13 mm (0.015 ± 0.005 inch) between the bail and the carriage arm for all head/carriage movement from cylinder 00 to cylinder 76. Turning the solenoid clockwise decreases the gap.

Note: *You can manually move the head/carriage assembly from cylinder 00 to cylinder 76 by turning off machine power. Turn power on after adjusting the gap.*

8. Is the gap correct?
   a. If YES, go to step 9.
   b. If NO, return to step 6 and readjust the gap.
9. Tighten the solenoid locking screw.
10. Remove the jumper.
11. Remove the paper between the heads.
12. Reinstall the drive cover assembly (DA522).
13. With the head load solenoid deactivated and the drive cover closed, visually check for a gap B of approximately 2.37 to 3.16 mm (3/32 to 4/32 inch) between the head surfaces. This gap cannot be measured.
14. Is the gap correct?
    a. If YES, go to step 15.
    b. If NO, again place the paper between the heads, turn the bail stop setscrew clockwise until the heads just touch, turn the setscrew counterclockwise one complete turn, and remove the paper.
15. Turn off machine power at the operator panel and connect the drive motor power connector.



DA563 Solenoids and Bail Assembly Removal (with Connector Block)

Note: *Use the procedures in DA563 and DA564 if the head load solenoid leads go to a taper pin connector block* **B** *that mounts on the DA3 card socket bracket. If they go to the A2 cable connector, use the procedures in DA565 and DA566.*

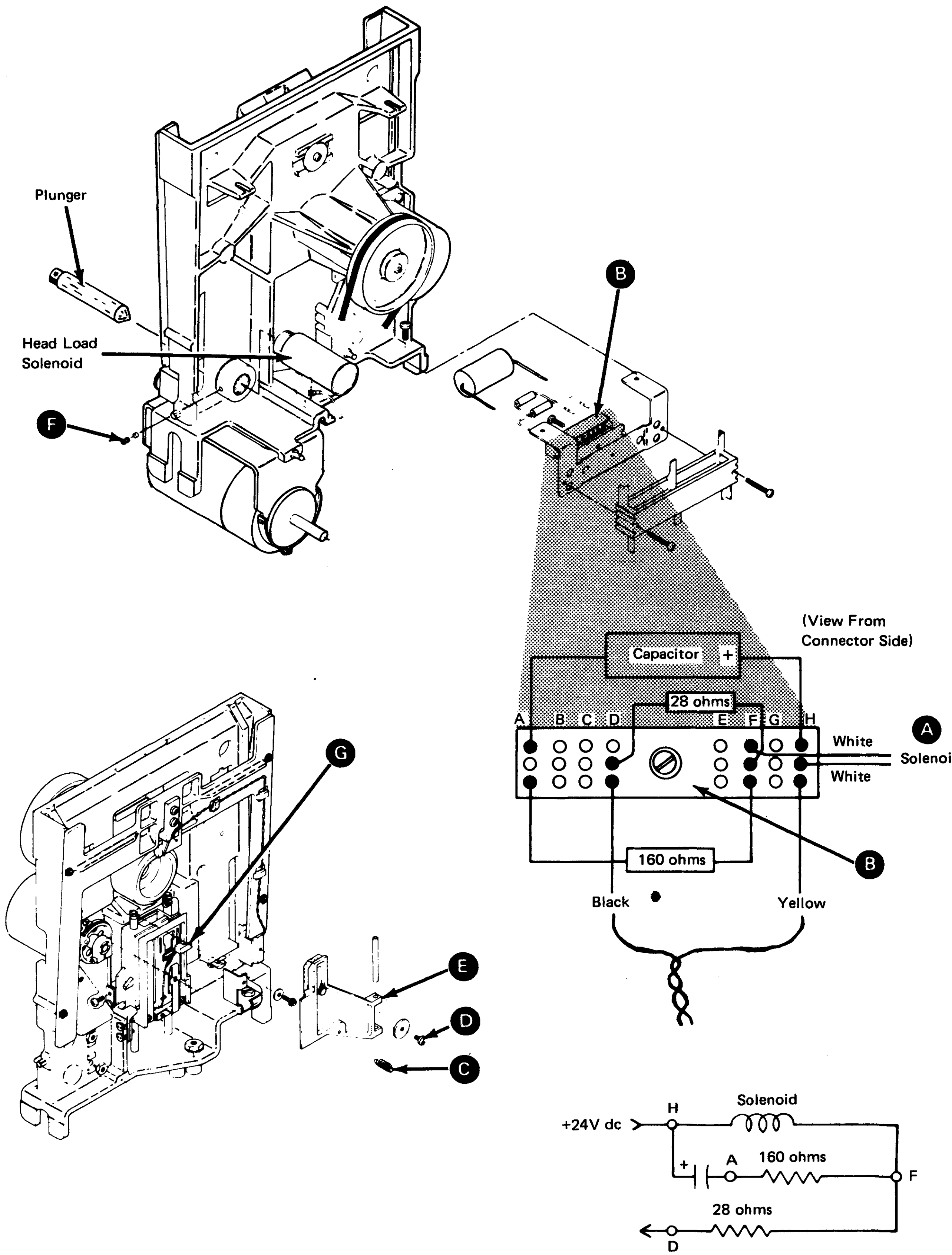
1. Turn off machine power at the operator panel.
2. Remove the diskette drive from the machine and disconnect the cables, including the drive motor power connector (DA515).
3. Remove the drive cover assembly (DA521).
4. Insert a clean strip of paper between the heads to prevent the head surfaces from touching.
5. Remove the solenoid leads **A** from the connector block **B**, while remembering the cable path for the installation procedure.
6. Remove the bail return spring **C**.
7. Remove the mounting screw **D** and the bail **E**.

Note: *This pulls the plunger out of the solenoid. Be careful not to damage the plated surface of the plunger.*

8. Remove the plunger from the bail.
9. Loosen the head load solenoid locking screw **F**.
10. Remove the solenoid by turning it counterclockwise.

DA564 Solenoid and Bail Assembly Installation (with Connector Block)

1. Install the solenoid about four turns clockwise into the casting.
2. Install the plunger into the bail.
3. Reinstall the bail **E** with the mounting screw **D**, while inserting the plunger into the solenoid. Be careful not to damage the plated surface of the plunger. Also ensure that the bail is under the carriage arm tab **G**.
4. Reinstall the bail return spring **C**.
5. Place the solenoid leads **A** in the same cable path as before and insert them into the connector block **B**.
6. Reinstall (DA515) and place the diskette drive in the service position (DA514), then reconnect all cables except the drive motor power connector.
7. Turn on machine power at the operator panel.
8. Perform the solenoid and bail adjustment (DA562) beginning with step 5.



DA565 Solenoid and Bail Assembly Removal (without Connector Block)

Note: *Use the procedures in DA565 and DA566 if the head load solenoid leads go to the A2 cable connector. If they go to a taper pin connector block that mounts on the DA3 card socket bracket, use the procedures in DA563 and DA564.*

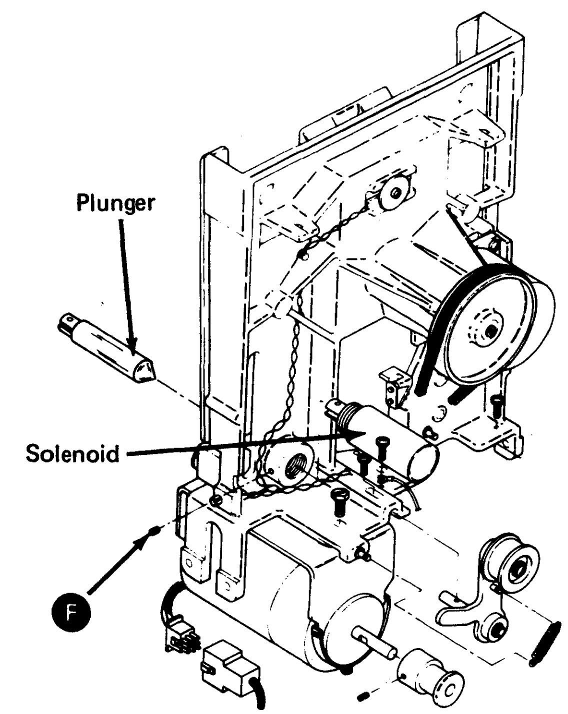
1. Turn off machine power at the operational panel.
2. Remove the diskette drive from the machine and disconnect the cables, including the drive motor power connector (DA515).
3. Remove the drive cover assembly (DA521).
4. Insert a clean strip of paper between the heads to prevent the head surfaces from touching.
5. Remove the bail return spring C.
6. Remove the mounting screw D and the bail E.

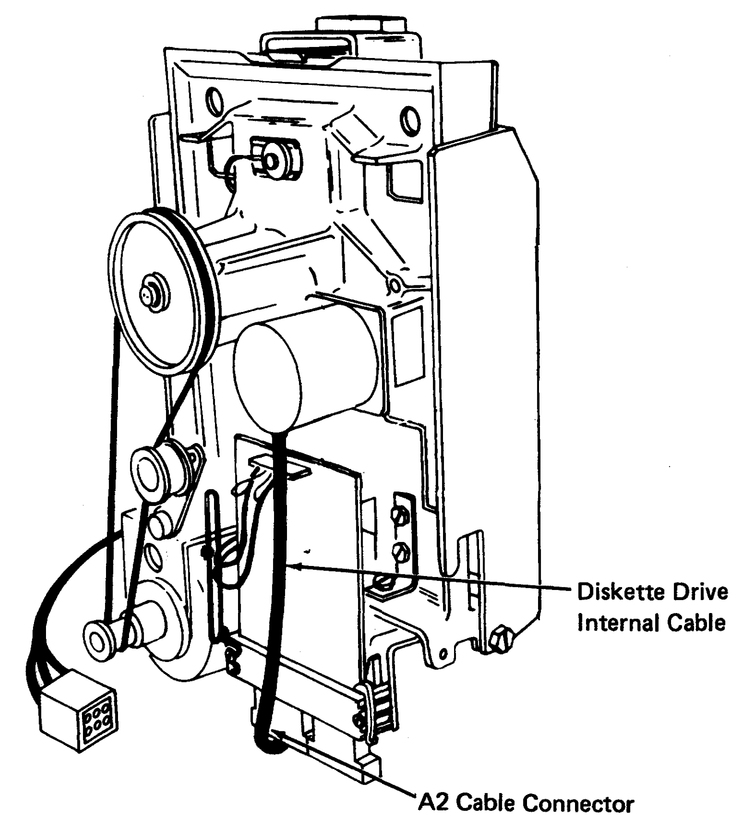
Note: *This pulls the plunger out of the solenoid. Be careful not to damage the plated surface of the plunger.*

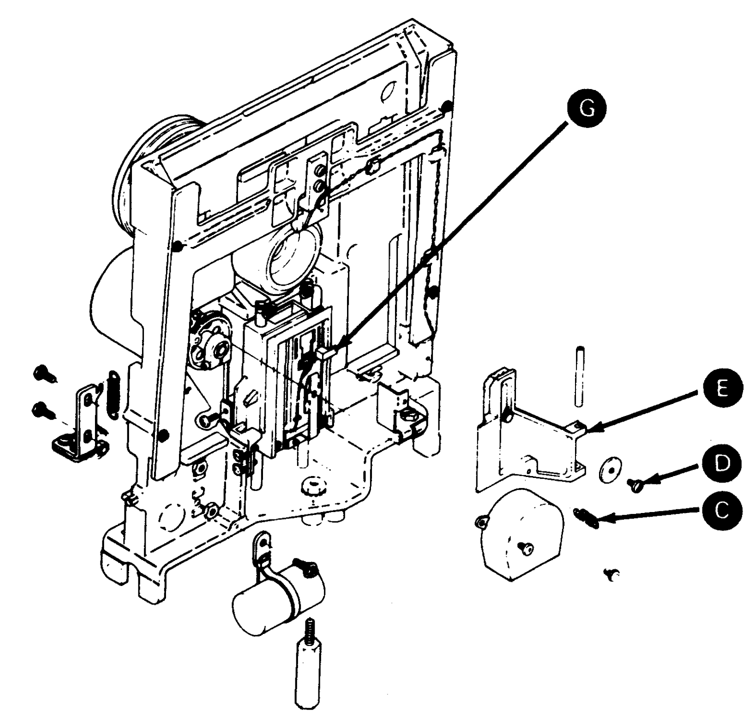
7. Unplug the diskette drive internal cable from the DA3 card A2 cable socket position.
8. Remove the cable connector covers by removing the two screws.
9. Remove the solenoid leads A from the cable connector by pushing in and down on the locking tabs B with a small screwdriver.
10. Remove the plunger from the bail.
11. Loosen the head load solenoid locking screw F.
12. Remove the solenoid by turning it counterclockwise.

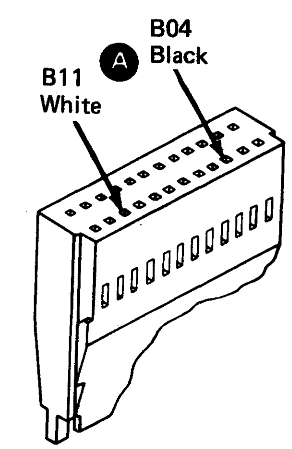
DA566 Solenoid and Bail Assembly Installation (without Connector Block)

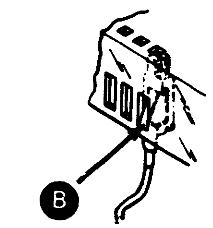
1. Install the solenoid about four turns clockwise into the casting.
2. Install the plunger into the bail.
3. Reinstall the bail E with the mounting screw D, while inserting the plunger into the solenoid. Be careful not to damage the plated surface of the plunger. Also ensure that the bail is under the carriage arm tab G.
4. Reinstall the bail return spring C.
5. Insert the solenoid leads A into the cable connector. Ensure that the terminal tabs B lock into the connector slots.
6. Reinstall the connector covers with the two screws and plug the cable into the DA3 card A2 cable socket position.
7. Reinstall (DA515) and place the diskette drive in the service position (DA514); then reconnect all cables except the drive motor power connector.
8. Turn on machine power at the operator panel.
9. Perform the solenoid and bail adjustment (DA562) beginning with step 5.











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DA570 Drive Belt

DA571 Drive Belt Tracking Service Check

1. Place the diskette drive in the service position (DA514) and leave machine power on.
2. Does the drive belt track in the center of both the hub pulley and the drive pulley?
   a. If YES, return the diskette drive to the operate position and reinstall the diskette panel cover if removed.
   b. If NO, adjust the drive belt tracking (DA572).

DA572 Drive Belt Tracking Adjustment

1. Remove the diskette panel cover if not already removed.
2. Turn off machine power at the operator panel.
3. Loosen the idler locking screw A and the drive pulley setscrew B .
4. Slide the idler assembly and the drive pulley either in or out to center the drive belt on both the hub and drive pulleys when turning the drive pulley counterclockwise.
5. Tighten the idler locking screw.
6. Tighten the drive pulley setscrew on the flat surface of the drive motor shaft.
7. Turn on machine power at the operator panel.
8. Perform the belt tracking service check (DA571).

DA573 Drive Belt Removal

1. Place the diskette drive in the service position (DA514).
2. Turn off machine power at the operator panel.
3. Manually release the idler tension and remove the drive belt.

DA574 Drive Belt Installation

1. Install the belt with the idler in place as shown C .
2. Turn on machine power at the operator panel.
3. Perform the belt tracking service check (DA571).

DA580 Drive Motor and Pulley

DA581 Drive Motor and Pulley Removal

1. Turn off machine power at the operator panel.
2. Remove the diskette drive from the machine and disconnect the cables, including the drive motor power connector (DA515).
3. Remove the drive cover assembly (DA521).
4. Remove the drive belt (DA573).

DANGER
The motor case becomes hot after continuous use.

5. Remove the two motor bracket mounting screws D and remove the drive motor and bracket as an assembly, being careful not to lose the bail return spring and bracket E.
6. Loosen the drive pulley setscrew B and remove the pulley.

DA582 Drive Motor and Pulley Installation

1. Reinstall the drive pulley on the motor, and tighten the setscrew B on the flat surface of the motor shaft.

DANGER
To prevent personal injury on 60-Hz machines having diskette drive motor cases with two large holes, mount the motor with the holes F located under the bracket.

2. While ensuring that the bail return spring and bracket E are installed, attach the motor and bracket assembly with the two screws D .
3. Reinstall the drive cover assembly (DA522).
4. Reinstall (DA515) and place the diskette drive in the service position (DA514); then reconnect all cables including the drive motor power connector.
5. Install the drive belt (DA574).

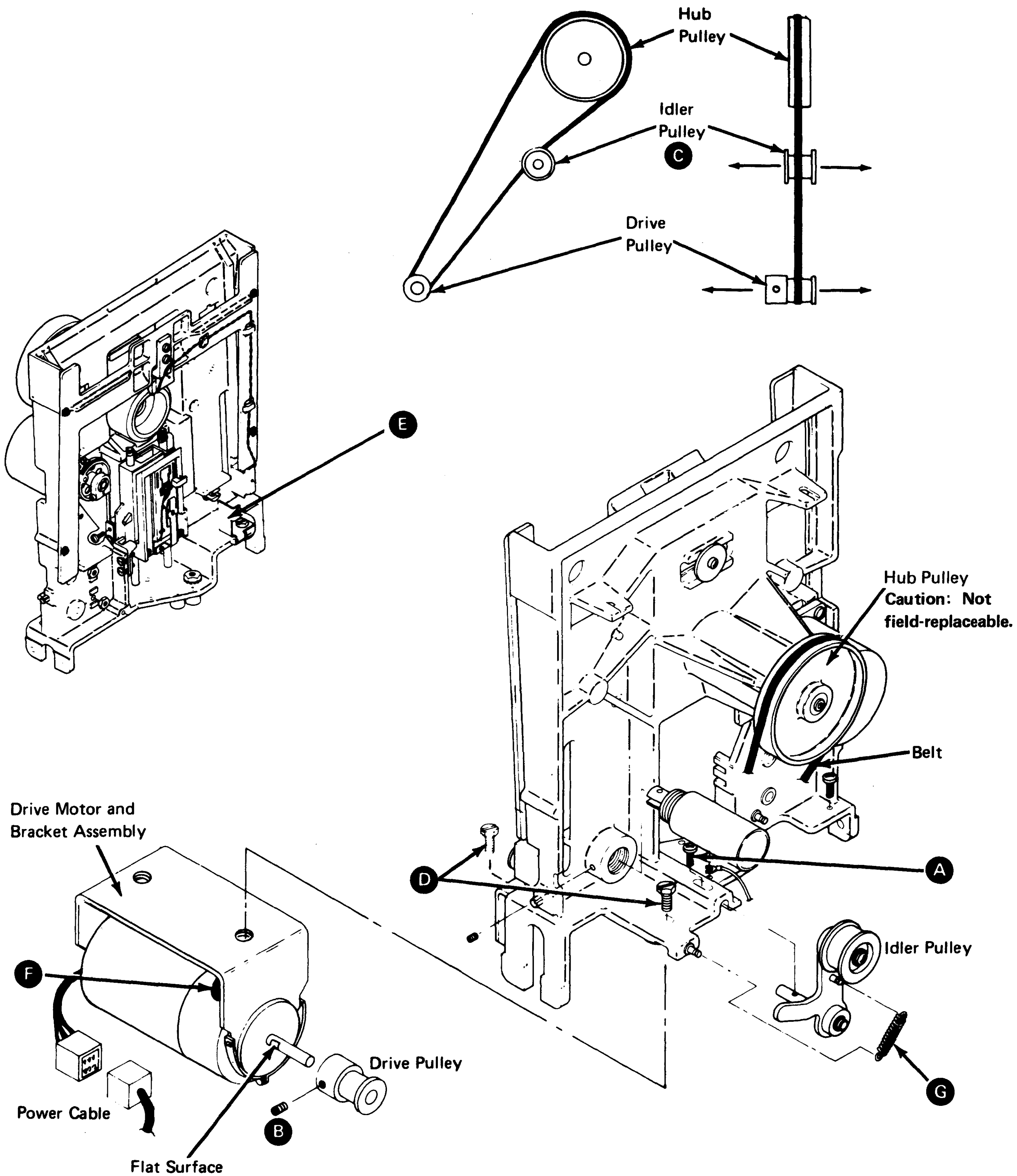
DA590 Drive Belt Idler Assembly

DA591 Drive Belt Idler Assembly Removal

1. Remove the drive belt (DA573).
2. Remove the idler spring G .
3. Remove the locking screw A and the idler assembly.

DA592 Drive Belt Idler Assembly Installation

1. Install the idler assembly with the locking screw A but do not tighten.
2. Install the idler spring G .
3. Install the drive belt (DA574).



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DA600 Adjustment, Removal, and Replacement Information, Part 2

DA601/DA602 Stepper Motor

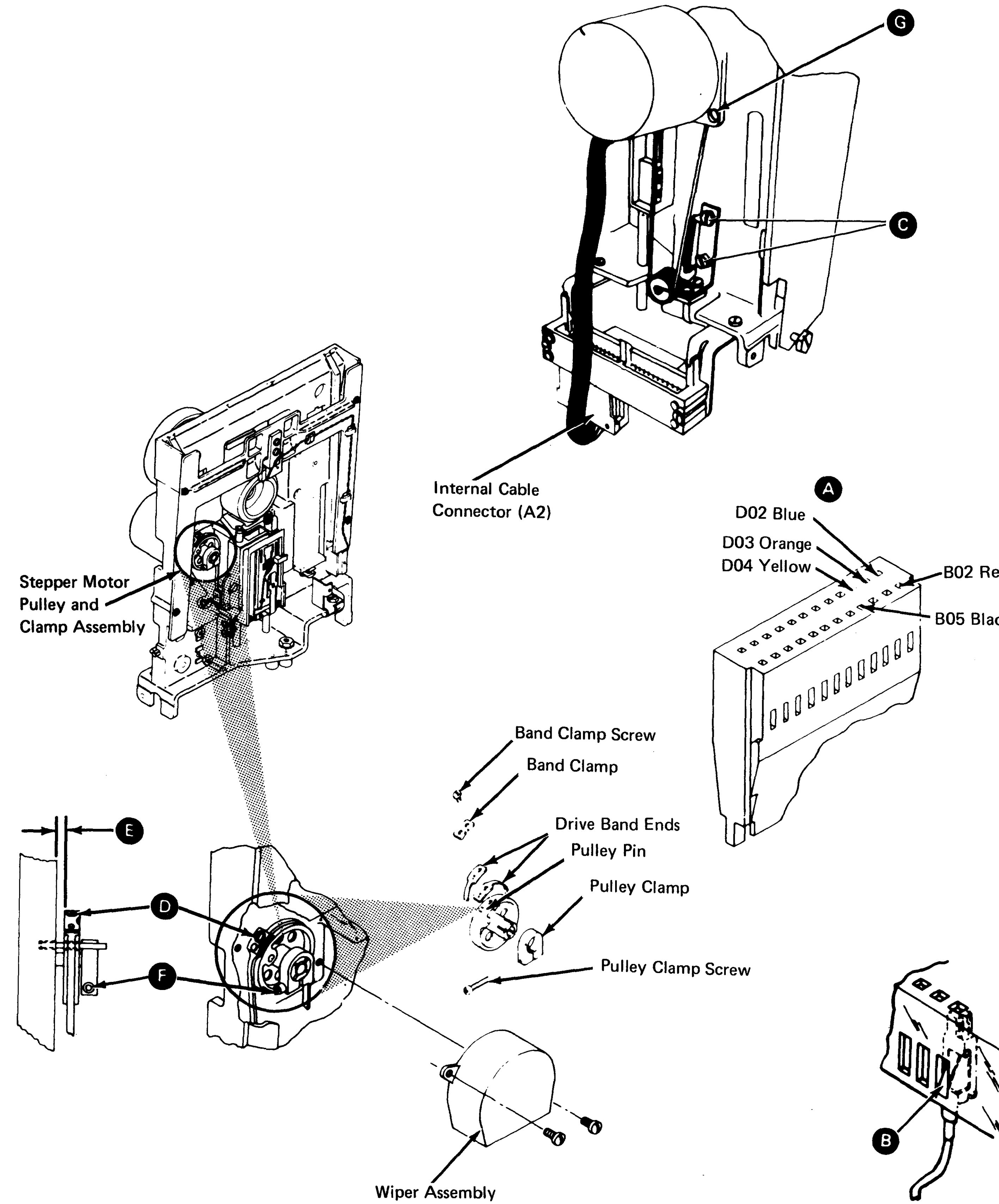
DA601 Stepper Motor Removal

1. Turn off machine power at the operator panel.
2. Remove the diskette drive from the machine and disconnect the cables, including the drive motor power connector (DA515).
3. Remove the drive cover assembly (DA521).
4. Carefully remove the head cable from the diskette drive control (DA3) card. Remember the cable path for the installation procedure.
5. Remove the DA3 card (DA670).
6. Remove the drive internal cable connector from the DA3 card A2 cable socket position.
7. Remove the cable connector covers by removing the two screws.
8. Remove the stepper motor leads A from the cable connector by pushing in and down on the locking tabs B with a small screwdriver.
9. Loosen the two drive band idler mounting screws C. Push the idler assembly against the spring tension and tighten the screws.
10. Remove the wiper assembly.

Caution: Do not damage the drive band while performing the following steps.

11. Remove the band clamp screw D and the band clamp from the stepper drive pulley.
12. Carefully remove the drive band ends from the pulley pin.
13. Measure the gap E between the stepper motor pulley and the casting. Write the measurement here.

    The gap is ________ .
14. Loosen the stepper motor pulley clamp screw F and remove the pulley and the clamp.
15. Remove the three stepper motor mounting screws G and remove the motor.

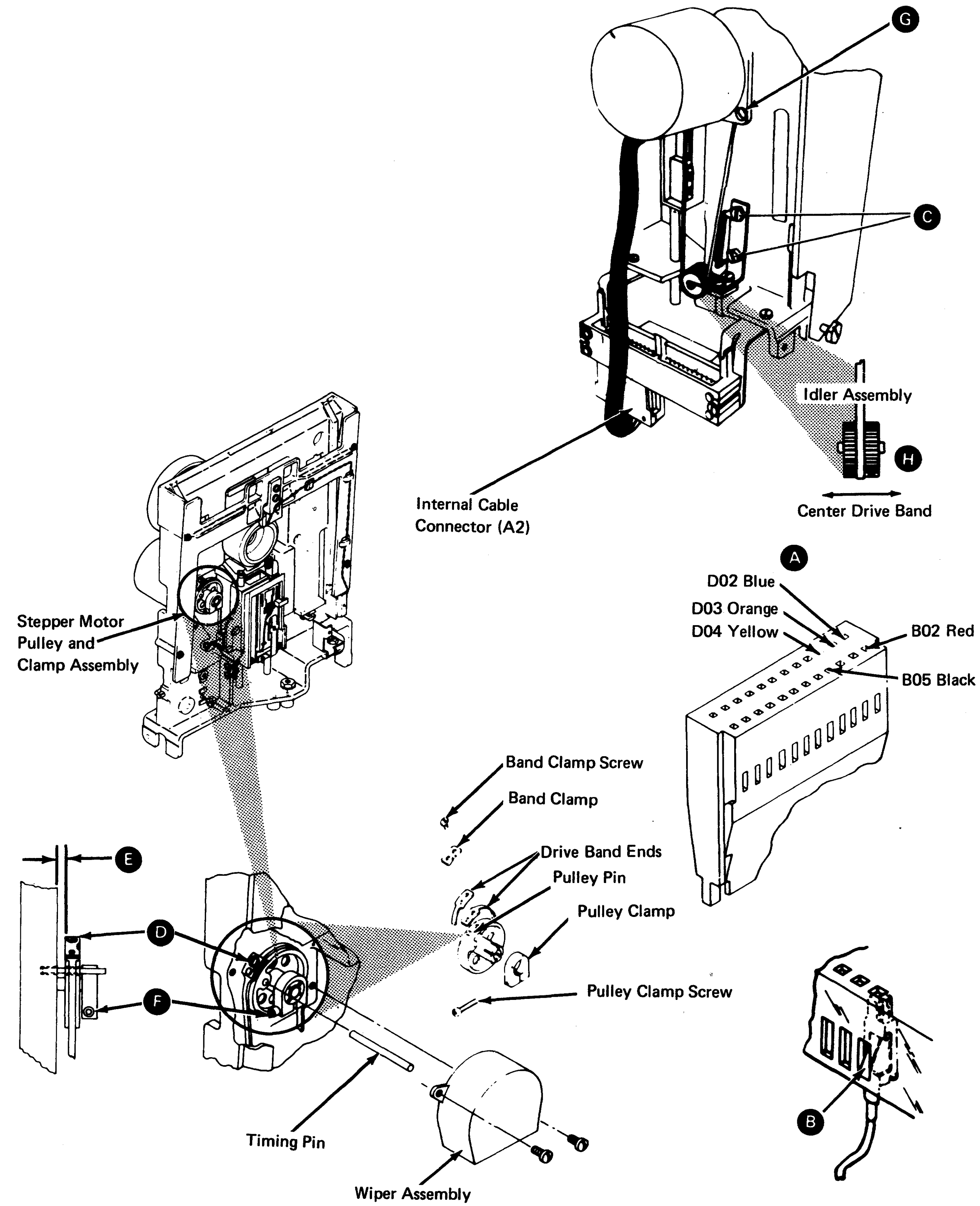


DA602 Stepper Motor Installation

1. Install the stepper motor using the three mounting screws G. Position the motor cable toward the DA3 card.
2. Insert the stepper motor leads A into the cable connector. Ensure that the terminal tabs B lock into the connector slots.
3. Reinstall the cable connector covers with the two screws and insert the cable into the DA3 card A2 cable socket position.
4. Reinstall the stepper motor pulley and clamp. Leave the clamp screw F loose so the stepper motor shaft can turn inside the pulley.
5. Carefully reinstall the drive band ends on the pulley pin. Reinstall the band clamp with the notch facing away from the stepper motor, and reinstall the band clamp screw but do not tighten it.
6. Loosen the two drive band idler mounting screws C and let spring tension position the idler. Tighten the mounting screws and center the drive band on the idler pulley as shown H.
7. Reinstall the DA3 card (DA670).
8. Position the head/carriage at about cylinder 40 by manually turning the stepper motor pulley until the timing hole in the casting and the hole in the pulley are aligned, and insert a timing pin.
9. Remove both the DA1 and DA2 diskette adapter cards (see DA111 for location). This prevents activating the stepper motor access lines from an external source.
10. Reinstall (DA515) and place the diskette drive in the service position (DA514); then reconnect all cables except the drive motor power connector.

DANGER
Line voltage is always present at the power connector with machine power on.

11. Turn on machine power at the operator panel.
12. Install a jumper on the DA3 card from TPA13 (Ground) to THP11 (—Align Access 0). See Figure DA420-2 for test point locations. This step electrically detents the head/carriage at cylinder 40.
13. Make gap E between the pulley and the casting the same as that recorded in DA601, step 13.
14. Tighten the pulley clamp screw F.
15. Remove the timing pin and the jumper.
16. Tighten the band clamp screw D while ensuring that the drive band remains straight.
17. Turn off machine power at the operator panel.
18. Manually turn the stepper motor pulley. Does the drive band remain centered on its idler pulley H for all head/carriage assembly movement from cylinder 00 to cylinder 76?
    a. If YES, perform the head/carriage service check (DA551) beginning with step 2 of "Head/Carriage Service Check Using a Jumper".
    b. If NO, perform the stepper band adjustment (DA622) beginning with step 4.



DA610 Stepper Motor Pulley and Clamp Assembly

DA611 Stepper Motor Pulley and Clamp Assembly Removal

1. Turn off machine power at the operator panel.
2. Remove the diskette drive from the machine and disconnect the cables, including the drive motor power connector (DA515).
3. Remove the drive cover assembly (DA521).
4. Remove the wiper assembly.
5. Carefully remove the head cable from the diskette drive control (DA3) card. Remember the cable path for the installation procedure.
6. Remove the DA3 card (DA670).
7. Loosen the two drive band idler mounting screws C. Push the idler assembly against the spring tension and tighten the screws.

Caution: Do not damage the drive band while performing the following steps.

7. Remove the band clamp screw D and the band clamp from the pulley.
8. Carefully remove the drive band ends from the pulley pin.
9. Measure the gap E between the stepper motor pulley and the casting. Write the measurement here.

   The gap is ______.
10. Loosen the stepper motor pulley clamp screw F and remove the pulley and the clamp.

DA612 Stepper Motor Pulley and Clamp Assembly Installation

1. Reinstall the stepper motor pulley and clamp. Leave the clamp screw F loose so the stepper motor shaft can turn inside the pulley.

Caution: Do not damage the drive band while performing the following steps.

2. Carefully reinstall the drive band ends on the pulley pin. Reinstall the band clamp with the notch facing away from the stepper motor, and reinstall the band clamp screw D but do not tighten it.
3. Loosen the two drive band idler mounting screws C and let spring tension position the idler. Tighten the mounting screws and center the drive band on the idler pulley as shown H.
4. Reinstall the DA3 card, card retainer, and head cable (DA670).
5. Position the head/carriage at about cylinder 40 by manually turning the stepper motor pulley until the timing hole in the casting and the hole in the pulley are aligned, and insert a timing pin.
6. Remove both the DA1 and DA2 diskette adapter cards (see DA111 for locations). This prevents activating the stepper motor access lines from an external source.
7. Reinstall (DA515) and place the diskette drive in the service position (DA514); then reconnect all cables except the drive motor power connector.

Danger
Line voltage is always present at the power connector with machine power on.

8. Turn on machine power at the operator panel.
9. Install a jumper on the DA3 card from TPA13 (Ground) to THP11 (—Align Access 0). See Figure DA420-2 for test point locations. This step electrically detents the head/carriage at cylinder 40.
10. Make gap E between the pulley and the casting the same as that recorded in DA611, step 9.
11. Tighten the pulley clamp screw F.
12. Remove the timing pin and the jumper.
13. Tighten the band clamp screw D while ensuring that the drive band remains straight.
14. Turn off machine power at the operator panel.
15. Manually turn the stepper motor pulley. Does the drive band remain centered on its idler puller H for all head/carriage assembly movement from cylinder 00 to cylinder 76?
    a. If YES, perform the head/carriage service check (DA551) beginning with step 3 of "Head/Carriage Service Check Using a Jumper".
    b. If NO, perform the stepper drive band adjustment (DA622) beginning with step 4.

DA620 Stepper Drive Band

DA621 Stepper Drive Band Service Check

1. Place the diskette drive in the service position (DA514).
2. Remove the drive cover assembly (DA521).
3. Remove the wiper assembly.
4. Turn off machine power at the operator panel.
5. Manually turn the stepper motor pulley. Does the drive band remain centered on its idler puller H for all head/carriage assembly movement from cylinder 00 to cylinder 76?
   a. If YES, go to step 6.
   b. If NO, remove the diskette drive from the machine and disconnect the cables, including the drive motor power connector (DA515). Perform the stepper band drive adjustment (DA622) beginning with step 4.
6. Reinstall the wiper assembly.
7. Reinstall the drive cover assembly (DA522).

DA622 Stepper Drive Band Adjustment

1. Remove the diskette drive from the machine and disconnect the cables, including the drive motor power connector (DA515).
2. Remove the drive cover assembly (DA521).
3. Remove the wiper assembly.
4. Carefully remove the head cable from the diskette drive control (DA3) card. Remember the cable path for the installation procedure.
5. Remove the DA3 card (DA670).
6. Position the head/carriage assembly at about cylinder 40 by manually turning the stepper motor pulley until the head/carriage timing pointer is just above the timing block. The hole in the stepper motor pulley should be nearly aligned with the hole in the casting.
7. Remove the two screws J and the clamp that attach the stepper drive band to the head/carriage.
8. Loosen the two drive band idler mounting screws C. Let spring tension position the idler and tighten the screws.
9. Manually turn the stepper motor pulley to center the drive band on the idler pulley H.
10. Reposition the head carriage to about cylinder 40 and ensure that the carriage band clamp mounting slots K are centered from left to right over the mounting holes on the head/carriage.
11. Repeat step 10 with the head/carriage at cylinder 00 and at cylinder 76. Do the mounting slots remain centered at all three cylinder positions?
    a. If YES, go to step 15.
    b. If NO, go to step 12.
12. Loosen the stepper motor pulley clamp screw F.
13. Loosen the drive band clamp screw D.
14. Move the stepper motor pulley to center the band clamp mounting slots; then tighten the pulley clamp screw F and the band clamp screw D.
15. Reposition the head/carriage at about cylinder 40.
16. Reinstall the carriage band clamp with the two clamp screws J, but do not tighten them.
17. Reinstall the DA3 card, card retainer, and head cable (DA670).
18. Reinstall (DA515) and place the diskette drive in the service position (DA514); then reconnect all cables except the drive motor power connector.

DANGER
Line voltage is always present at the power connector with machine power on.

19. Adjust the head/carriage (DA552) beginning with step 2 of "Head/Carriage Adjustment Using a Jumper".

DA623 Stepper Drive Band Removal

1. Remove the diskette drive from the machine and disconnect the cables, including the drive motor power connector (DA515).
2. Remove the drive cover assembly (DA521).
3. Remove the wiper assembly.
4. Carefully remove the head cable from the diskette drive control (DA3) card. Remember the cable path for the installation procedure.
5. Remove the DA3 card (DA670).
6. Position the head/carriage assembly at about cylinder 40 by manually turning the stepper motor pulley until the head/carriage timing pointer is just above the timing block. The hole in the stepper motor pulley should be nearly aligned with the hole in the casting.
7. Loosen the two drive band idler mounting screws C. Push the idler assembly against the spring tension and tighten the screws.
8. Remove the two screws J and the clamp that attach the stepper drive band to the head/carriage, and place the head/carriage at the lower limit (cylinder 00).
9. Remove the band clamp screw D and the band clamp from the stepper drive pulley.
10. Remove the drive band ends from the pulley pin and remove the drive band.

DA624 Stepper Drive Band Installation

Caution: Do not damage the drive band while performing the following steps.

1. Place the drive band around the drive band idler assembly.
2. Install the drive band ends on the pulley pin.
3. Reinstall the band clamp with the notch facing away from the stepper motor. Reinstall and tighten the band clamp screw D while ensuring that the drive band remains straight.
4. Perform the stepper drive band adjustment (DA622) beginning with step 8.

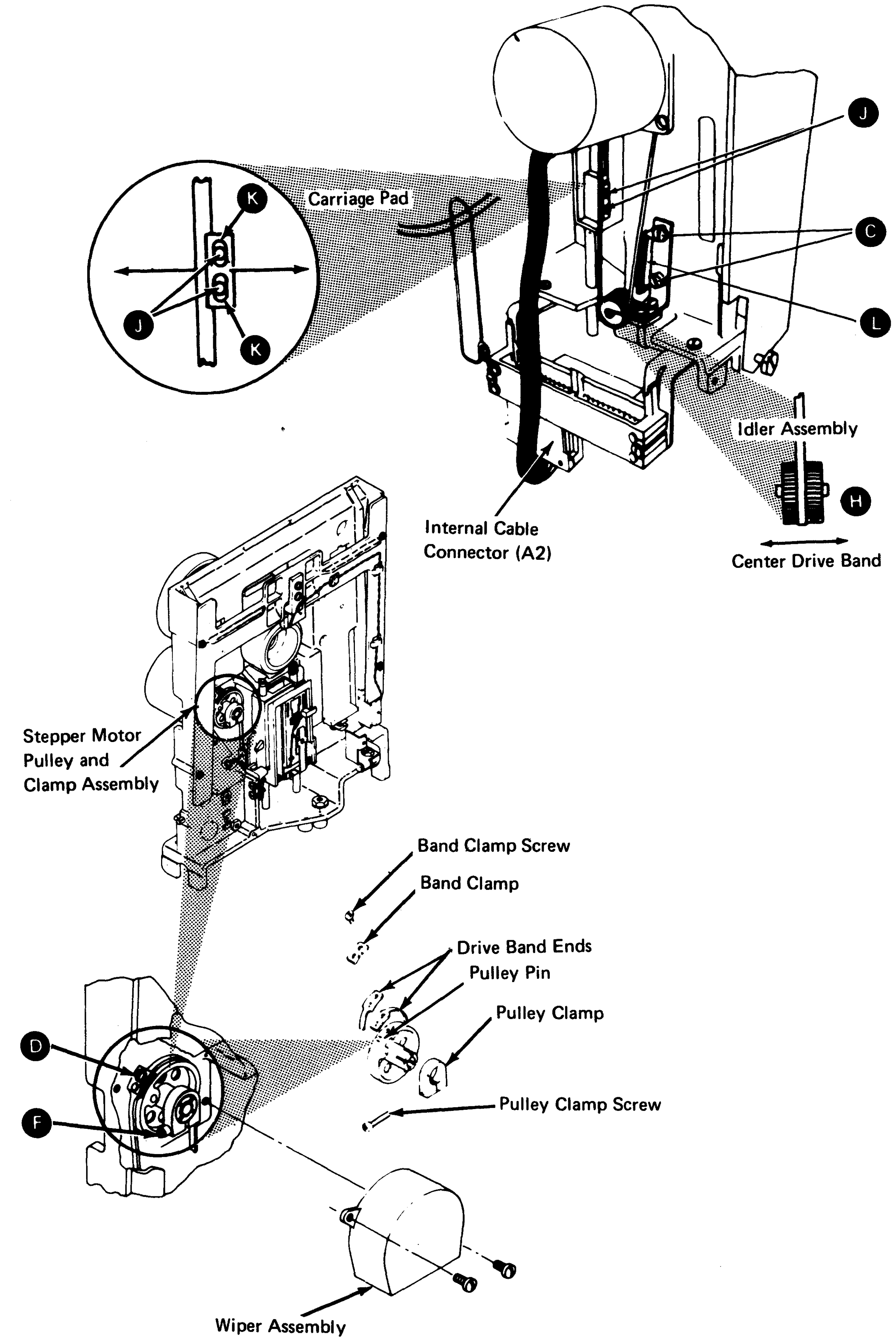
DA630 Stepper Drive Band Idler Assembly

DA631 Stepper Drive Band Idler Assembly Removal

1. Remove the drive band (DA623).
2. Loosen the two drive band idler mounting screws C.
3. Remove the idler spring L.
4. Remove the idler mounting screws C and the idler assembly.

DA632 Stepper Drive Band Idler Assembly Installation

1. Reinstall the idler assembly with the two mounting screws C but do not tighten them.
2. Reinstall the idler spring L.
3. Push the idler assembly against the spring tension and tighten the screws.
4. Install the stepper drive band (DA624).



DA640 Diskette Speed Service Check

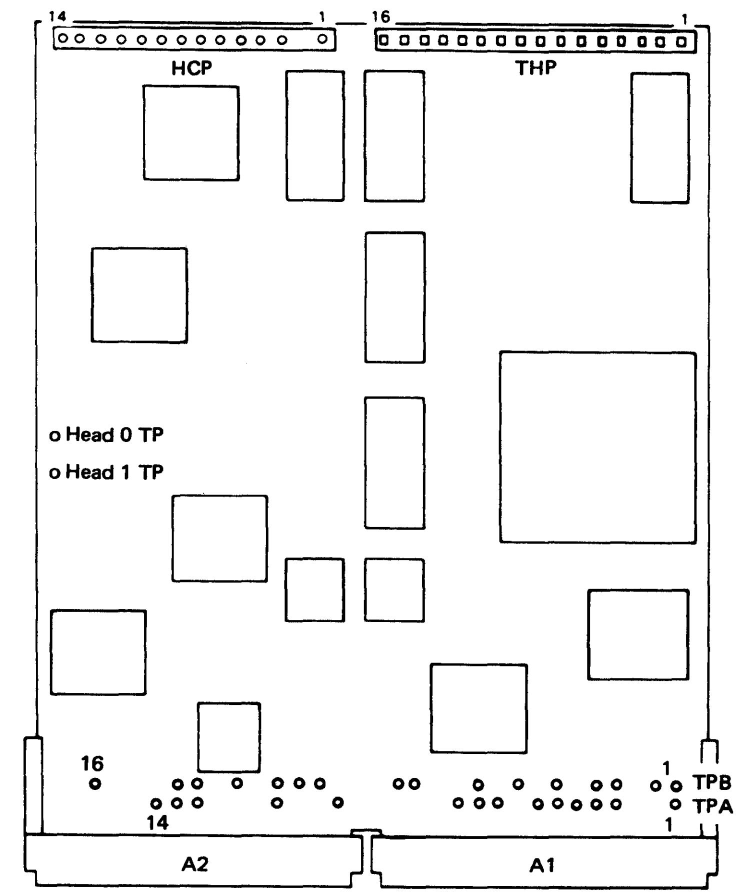
1. Insert a diskette and close the cover assembly.
2. Install a jumper on the diskette drive control (DA3) card from TPA13 (Ground) to TPB13 (–Head Load) to activate the head load solenoid.
3. Set up an oscilloscope as follows:

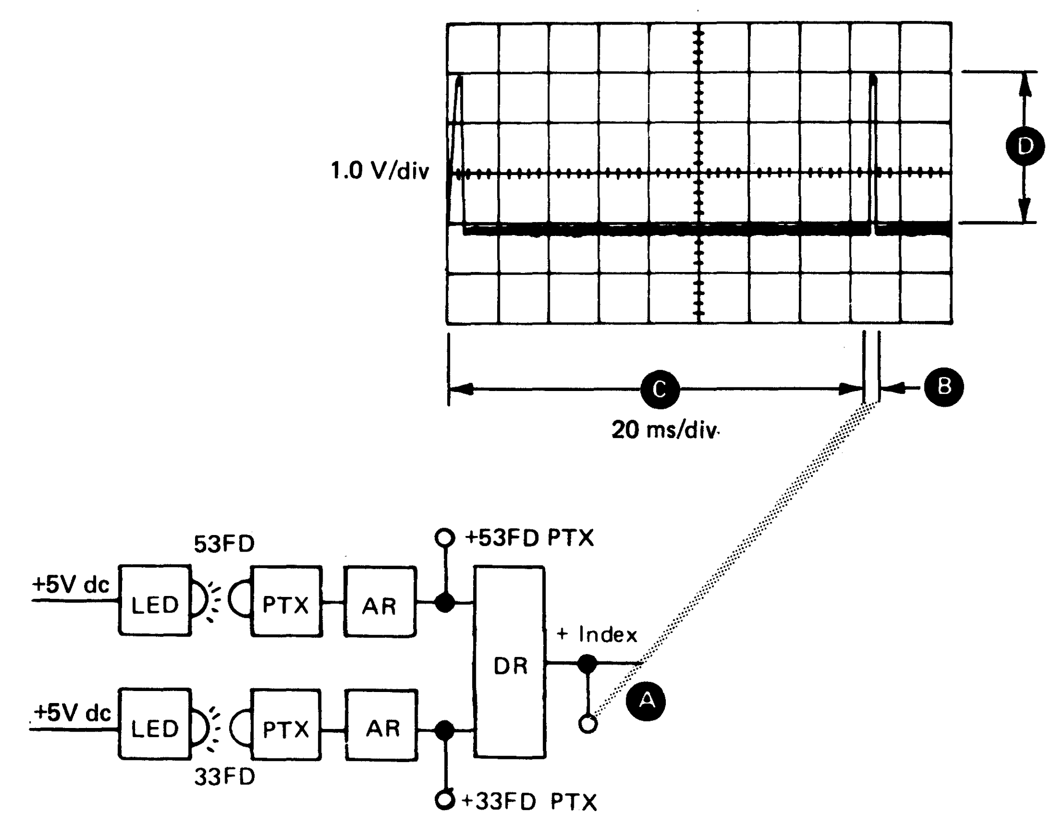
Note: *Use a Tektronix* 453, 454, or similar scope and a times ten (X10) probe.*

Control	Setting
Channel A sweep mode	Normal
Channel A level	+
Channel A coupling	DC
Channel A slope	+
Channel A source	Internal
Trigger	Normal
Mode	Channel 1
Channel 1 volts/division	1.0 V/div
Channel 1 input	DC
Times/division	20 ms

4. Place the channel 1 probe on TPB9 (+Index) A .
5. Observe that an index pulse width of from 1.5 ms to 3.0 ms B occurs each 166.7±4.2 ms C . Pulse amplitude should be between 2.4V and 4.2V dc D .
6. Remove the jumper, the scope probe, and the diskette.

*Trademark of Tektronix, Inc.

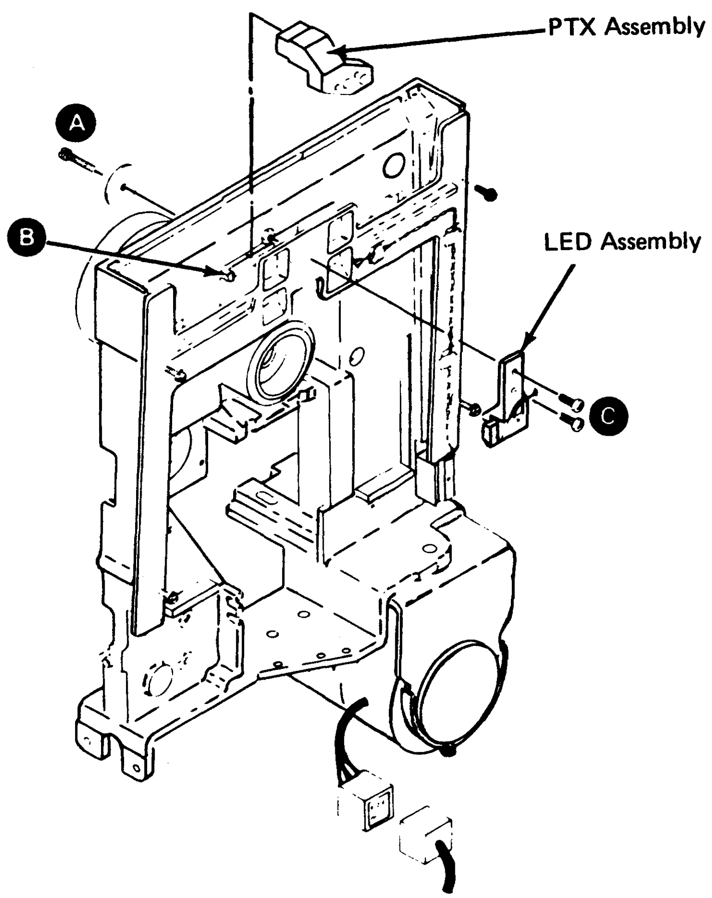


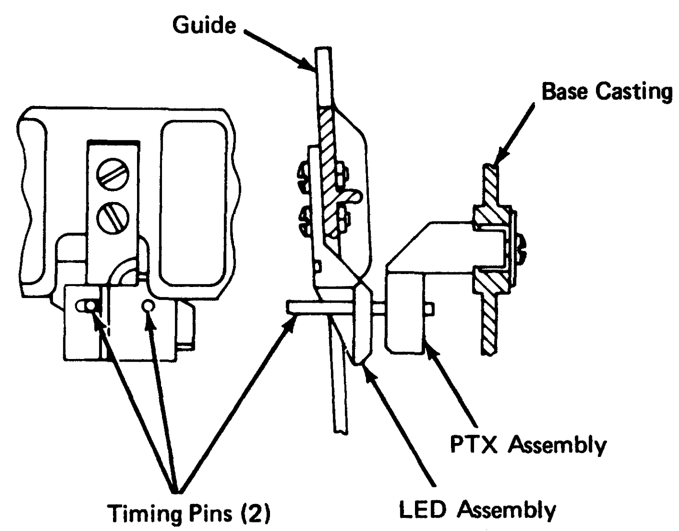


DA650 Light Emitting Diode (LED) Assembly

DA651 LED and Phototransistor (PTX) Assembly Alignment

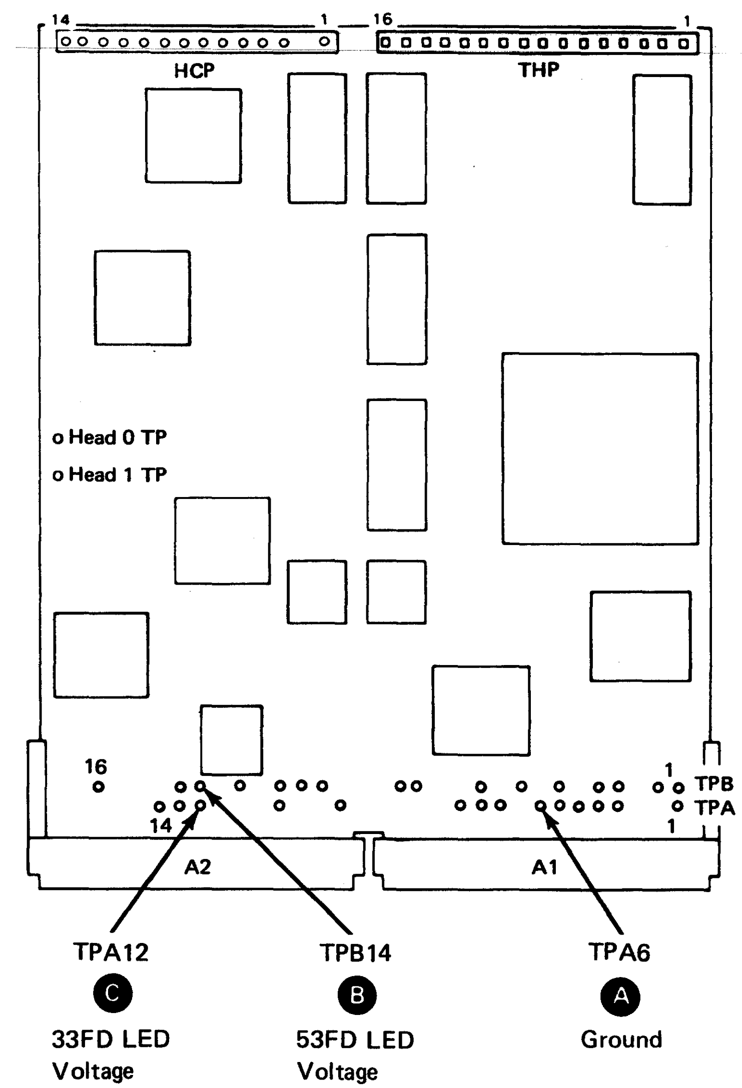
1. Place the diskette drive in the service position (DA514). It is not necessary to turn off machine power.
2. Remove the drive cover assembly (DA521).
3. Loosen the PTX assembly mounting screw A.
4. Place the PTX assembly away from the leads and against the casting stop B, and tighten the mounting screw.
5. Loosen the two LED assembly mounting screws C.
6. Insert two timing pins, located inside the cover assembly, through the LED assembly and into the PTX assembly. Tighten the two LED mounting screws C.
7. Remove the timing pins.
8. Reinstall the drive cover assembly (DA522).





DA652 LED Output Service Check

1. Turn on machine power at the operator panel.
2. Connect your multimeter negative lead to the diskette drive control (DA3) card Ground test point A.
3. Set the meter scale to 5V dc and connect the positive lead to the 53FD LED Voltage test point B. The voltage should be from +1.0V to +2.0V dc.
4. Move the positive lead to the 33FD LED Voltage test point C. The voltage should also be from +1.0V to +2.0V dc.

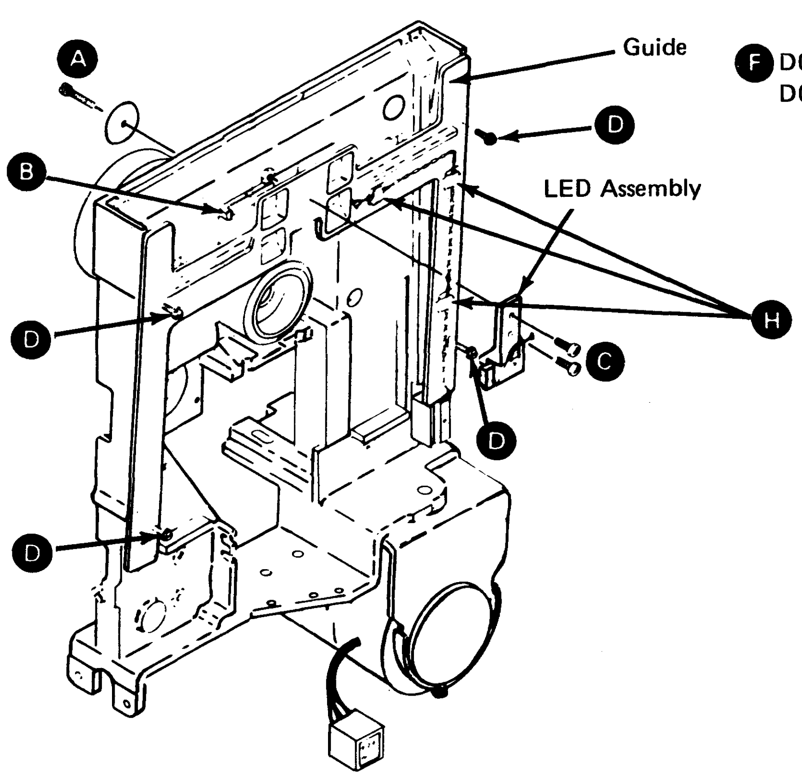


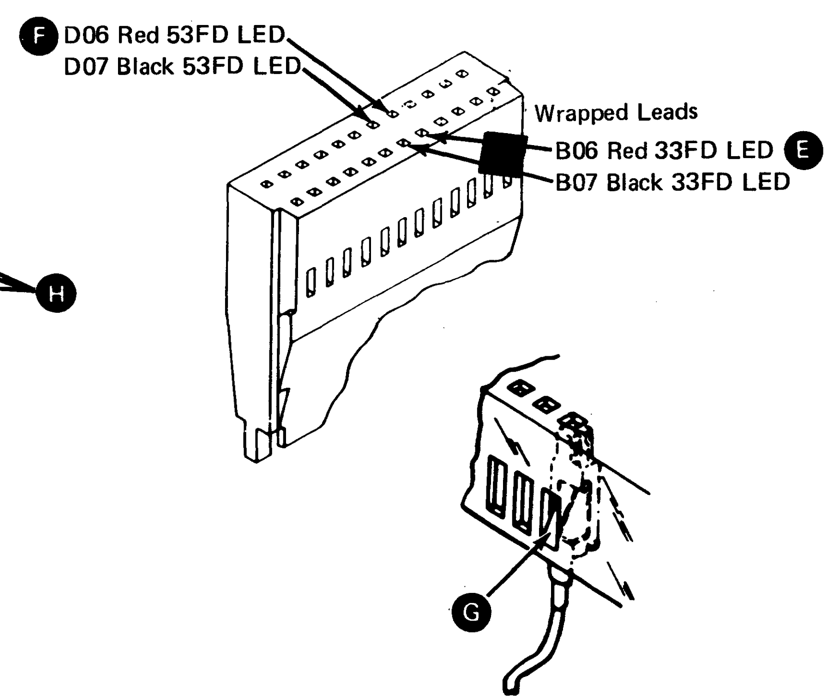
DA653 LED Assembly Removal

1. Turn off power at the machine operator panel.
2. Remove the diskette drive from the machine and disconnect the cables, including the drive motor power connector (DA515).
3. Remove the drive cover assembly (DA521).
4. Remove the diskette drive internal cable from the DA3 card A2 cable socket position.
5. Remove the cable connector covers by removing the two screws.
6. Remove the two wrapped 33FD LED leads E and the two 53FD LED leads F by pushing in and down on the locking tabs G with a small screwdriver.
7. Remove the LED cable from the three guide retainers H . Remember the cable path for the installation procedure.
8. Remove the four guide mounting screws D and the guide.
9. Remove the two LED assembly mounting screws C and nuts and remove the LED assembly.

DA654 LED Assembly Installation

1. Install the LED assembly on the guide using the two mounting screws C and nuts, but do not tighten them. Pass the wires through the three guide retainers H .
2. Reinstall the guide using the four mounting screws D .
3. Insert the two wrapped 33FD LED leads E and the two 53FD leads F into the cable connector. Ensure that the terminal tabs G lock into the connector slots.
4. Reinstall the connector covers with the two screws and replug the cable into the DA3 card A2 cable socket position.
5. Perform the LED and phototransistor alignment (DA651) beginning with step 6.





DA660 Phototransistor (PTX) Assembly

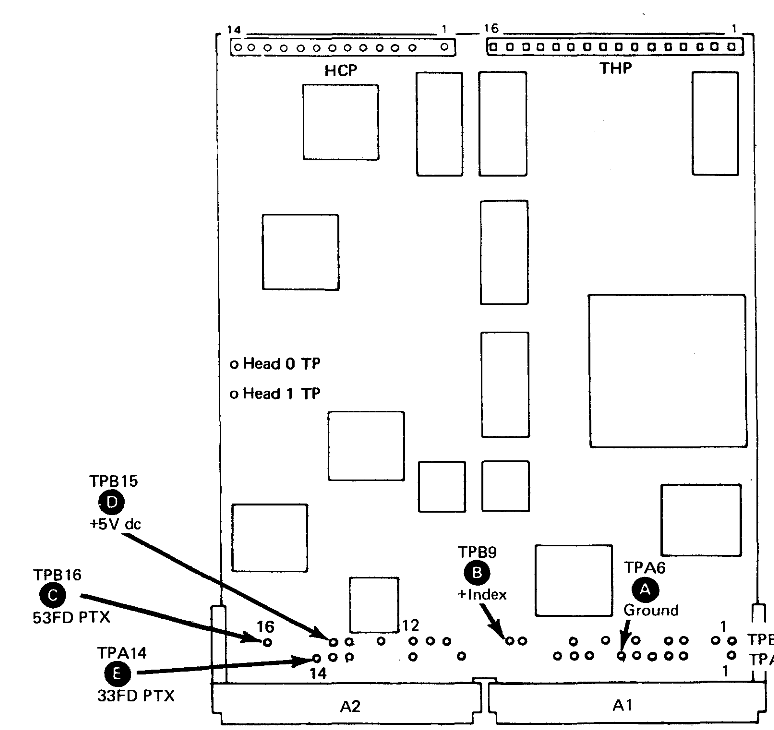
DA661 PTX Amplifier Service Check

1. Place the diskette drive in the service position (DA514) and leave machine power on.
2. Unplug the drive motor power connector.

DANGER
Line voltage is always present at the power connector with machine power on.

Caution: To obtain correct results without damaging the phototransistor, always perform this service check with the diskette inserted backward. (The label should face the hub pulley.)

3. Insert a diskette backward and close the cover assembly.
4. Use the 15V dc scale and connect the positive lead of your multimeter to the +Index test point B on the diskette drive control (DA3) card.
5. Connect the negative lead to the ground test point A . The reading should be less than 1.0V dc.
6. Leave the meter connected and install one end of a jumper on the 53FD PTX test point C .
7. While observing the meter, touch the other end of the jumper to the +5V test point D several times. The meter should read +2.5V or more when touching the test point. (The first reading could be inaccurate.)
8. Repeat steps 6 and 7 with the jumper on the 33FD PTX test point E .
9. Turn off machine power at the operator panel.
10. Remove the jumper, meter leads, and the diskette.
11. Connect the drive motor power connector.



DA662 PTX Assembly Removal

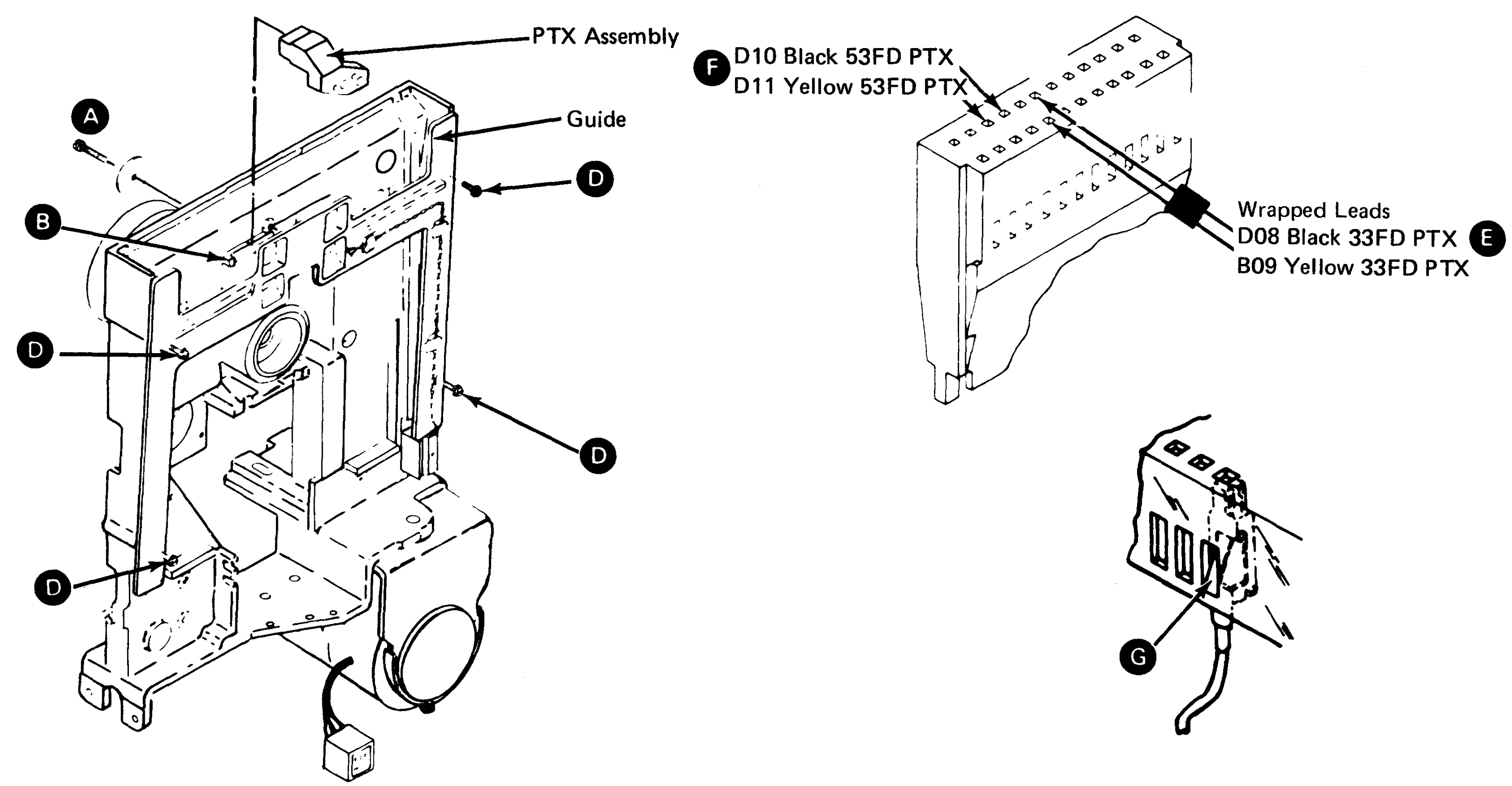
1. Turn off power at the machine operator panel.
2. Remove the diskette drive from the machine and disconnect the cables, including the drive motor power connector (DA515).
3. Remove the drive cover assembly (DA521).

Caution: Do not damage the leads while performing the following steps.

4. Remove the four guide mounting screws D and the guide.
5. Remove the diskette drive internal cable from the DA3 card A2 cable socket position.
6. Remove the cable connector covers by removing the two screws.
7. Remove the two wrapped 33FD PTX leads E and the two 53FD PTX leads F by pushing in and down on the locking tabs G with a small screwdriver.
8. Remove the PTX assembly mounting screw and washer A and remove the PTX assembly. Remember the cable path for the installation procedure.

DA663 PTX Assembly Installation

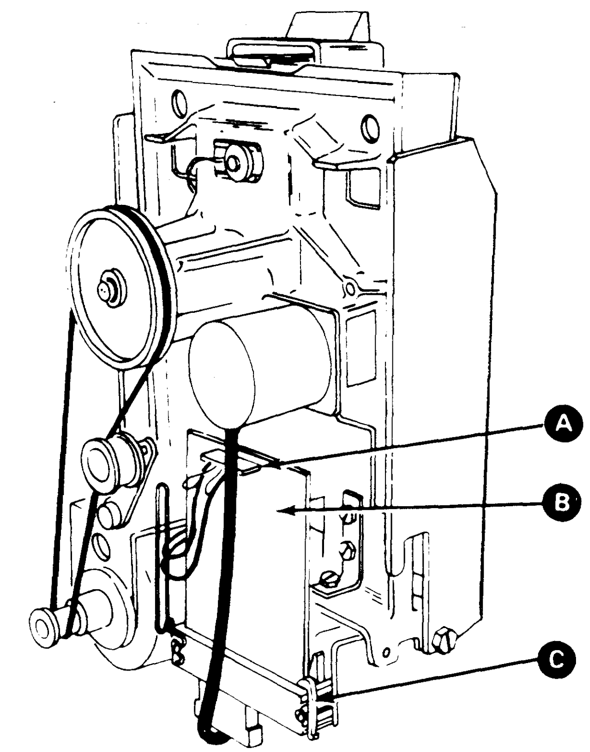
1. Place the PTX assembly away from the leads and against the casting stop B, and reinstall the mounting screw and the washer A.
2. Following the cable path, insert the two wrapped 33FD PTX leads E and the two 53FD PTX leads F into the cable connector. Ensure that the terminal tabs G lock into the connector slots.
3. Reinstall the connector covers with the two screws and replug the cable into the DA3 card A2 cable socket position.
4. Reinstall the guide using the four mounting screws D.
5. Perform the LED and PTX alignment (DA651) beginning with step 5.



DA670 Diskette Drive Control (DA3) Card Removal and Installation

1. Carefully remove the head cable A from the DA3 card B. Remember the cable path for the installation procedure.
2. Remove the card retainer C.
3. Remove the card.

To reinstall the card, reverse the above steps. Ensure that you seat the card firmly before replacing the card retainer.



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DA700 Voltages and Environmental Characteristics

Voltages

The machine type that contains the diskette drive supplies all power required to operate the drive, which includes:

- DC logic voltage distribution for the diskette drive control (DA3) card (see PA440-PA443).

Logic Voltage	Maximum Operating Current
-5V dc	0.10A
+5V dc	0.66A
+24V dc	0.59A

- 60-Hz single phase ac power (see PA410-PA423).

Voltage	Average Operating Current
100V ac	1.0A
115V ac	1.0A
200V ac	0.55A
208V ac	0.55A
230V ac	0.55A

- 50-Hz single phase ac power (see PA430-PA433).

Voltage	Average Operating Current
100V ac	1.0A
110V ac	1.0A
112.5V ac	1.0A
123.5V ac	1.0A
200V ac	0.55A
220V ac	0.55A
235V ac	0.55A

Note: *All voltage tolerances are 10% except +24V dc, which has a tolerance of 12%.*

Environmental Characteristics

IBM diskette drives can be operated or stored in the following temperature and humidity ranges:

	Temperature		Relative Humidity
	Celsius	Fahrenheit	
Operate (Powered On)	10° to 40.4°	50° to 105°	8% to 80%
Stored (Powered Off)	10° to 51.5°	50° to 125°	8% to 80%

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